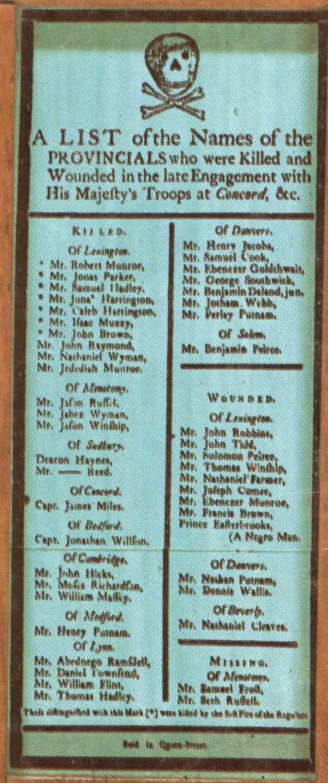
COMPUTER DESIGN

Sample

THE MAGAZINE OF DIGITAL ELECTRONICS

JULY 1975



A LIST of the Names of the PROVINCIALS who were Killed and Wounded in the late Engagement with His Majesty's Troops at *Concord*, &c.

KILLED.

Of Lexington.

* Mr. Robert Munroe,
* Mr. Jonas Parker,
* Mr. Samuel Hadley,
* Mr. Jona^{h} Harrington,
* Mr. Caleb Harrington,
* Mr. Isaac Muzzy,
* Mr. John Brown,
Mr. John Raymond,
Mr. Nathaniel Wyman,
Mr. Jedediah Munroe.

Of Menotomy.

Mr. Jason Russell,
Mr. Jabez Wyman,
Mr. Jason Winship,

Of Sudbury.

Deacon Haynes,
Mr. —— Reed.

Of Concord.

Capt. James Miles.

Of Bedford.

Capt. Jonathan Willson.

Of Cambridge.

Mr. John Hicks,
Mr. Moses Richardson,
Mr. William Mafky.

Of Medford.

Mr. Henry Putnam.

Of Lynn.

Mr. Abednego Ramsdell,
Mr. Daniel Townsend,
Mr. William Flint,
Mr. Thomas Hadley.

Of Danvers.

Mr. Henry Jacobs,
Mr. Samuel Cook,
Mr. Ebenezer Goldthwait,
Mr. George Southwick,
Mr. Benjamin Deland, jun.
Mr. Jotham Webb,
Mr. Perley Putnam.

Of Salem.

Mr. Benjamin Peirce.

WOUNDED.

Of Lexington.

Mr. John Robbins,
Mr. John Tidd,
Mr. Solomon Peirce,
Mr. Thomas Winship,
Mr. Nathaniel Farmer,
Mr. Joseph Comee,
Mr. Ebenezer Munroe,
Mr. Francis Brown,
Prince Easterbrooks,
(A Negro Man.

Of Danvers.

Mr. Nahan Putnam,
Mr. Dennis Wallis.

Of Beverly.

Mr. Nathaniel Cleaves.

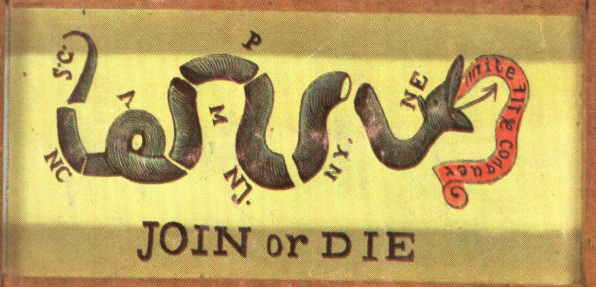
MISSING.

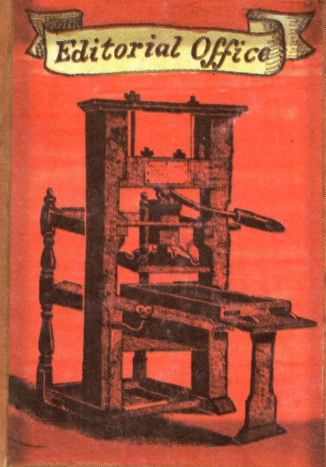
Of Menotomy.

Mr. Samuel Frost,
Mr. Seth Russell.

Those distinguished with this Mark [*] were killed by the 5th Fire of the Regulars

Sold in Queen-Street.

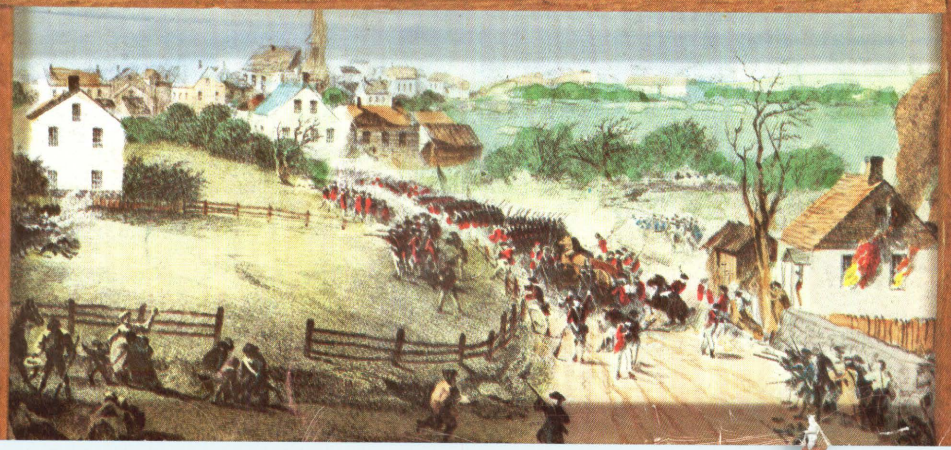




Designing Minicomputer Memory Systems with 4-Kilobit n-MOS Memories

Cyclic Sequence Generator Increases Security of Alarm Systems

Signal Names Help System Understanding



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Universal makes modems any way you want them — as OEM cards, rack-mountable units or free-standing packages. In a word, we combine the latest in modem technology with the ultimate in personalized service and personalized applications engineering.

For example, using CMOS technology, we've put a whole 201 modem on a single card in less than 50 square inches. Of course we also offer many choices of 103s and 202s.

Our custom design capability offers you the performance options you need, as well as complete compatibility with your mechanical layout. Besides cards, rack-mounted or free-standing units, Universal also provides multi-channel packages, with modems in any frequency mix up to 2400 bps.

In addition to our products, we're awfully proud of our customer service. Check us out: Call us on the telephone. You'll like what you hear.

universal data systems

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CIRCLE 1 ON INQUIRY CARD

The First Family in Cartridge Systems. An Official Portrait.

Being the first has become a habit with the Kennedy Company — a habit we can't kick. For instance, our Model 330 was the first to utilize 3M's new one-quarter inch cartridge. We designed it to be fully bi-directional at 25 ips normal speed, with a data transfer rate of 40,000 bits/second at 1600 bpi recording density, and includes features such as CRC generation and checking, error detection and gap generation.

Then, we added our OEM Model 331. All the same features, with the exception of a lower price and no formatting electronics.

Still not satisfied, we designed the first Digital Cartridge Recording System, System 4000. It consists of our Models 4344, 4345 and 4346 and utilizes our proven Model 330 recorder. Models 4344 (one recorder) and 4345 (two recorders) include the 4300 Series Formatter, which formats the 3M cartridge with 1600 bpi phase encoded data in the ANSI compatible format and utilizes simplified I/O commands such as "Write One Block," "Read One Block" etc. Model 4346, with two recorders, provides for system expansion.

In addition, System 4000, coupled with our computer controllers allows direct interface to most popular mini-computers and features compatibility with 1/2" tape software.

Is being first important? We think so. Our decks were designed for the emerging mini-computer data storage field. Being first means more experience, better service, stocked parts and accessories — in other words, all the requirements to stay first.

KENNEDY CO.

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(213) 798-0953

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CIRCLE 2 ON INQUIRY CARD

First came Remex flexible disk drives.

Now, the whole, compact, IBM-compatible, data-packin' system

The new Remex RFS7400 flexible disk system offers all of the high-speed, high-capacity attributes inherent in this technique, plus many outstanding performance advantages unique to the Remex design.

Naturally, the Remex systems are IBM 3740 compatible. We test each system to prove it. They read diskettes prepared in a 3740 system, or write and initialize diskettes that can be read on a 3740 system. The RFS7400 also offers a unique write enable option that gives foolproof operation without modification on any standard IBM compatible media.

Among the many other features, the RFS7400's fail-safe drive design offers Tracks "00" and "76" sensing to prevent machine damage and loss of data at both ends of the media. It offers approximately 50% longer life than competitive drives. And average random access time is more than 30% faster.

The system includes formatter electronics, with up to four separate drives, and power supply. Diagnostic software, I/O drivers and computer compatible interface controllers are available as options for PDP-11 and NOVA minicomputers. Like all other Remex computer interface packages, we guarantee system compatibility.

The Remex flexible disk system offers:

- Multiple drive read-write/seek operation
- File Unsafe
- Write protect
- High data reliability (Read Error Rate: 1×10^9 bits Read/Error, nominal; 1×10^{12} bits Read/Hard Error, nominal
- Storage capacity: 246×10^3 bytes per diskette
- Transfer rate: 31.25×10^3 bytes (8-bit) per second
- Available for 115 VRMS, 60Hz, 230 VRMS, 50Hz.
- DMA and Programmed I/O interface controller (option)

ASK FOR AN EVALUATION UNIT: Write Remex, Ex-Cell-O Corporation, 1733 Alton St., P.O. Box 11926, Santa Ana, Cal. 92711. Or call:

BOSTON: (617) 784-8380 • NEW YORK: (212) 947-0379
ORLANDO: (305) 894-4401 • CHICAGO: (312) 359-1310
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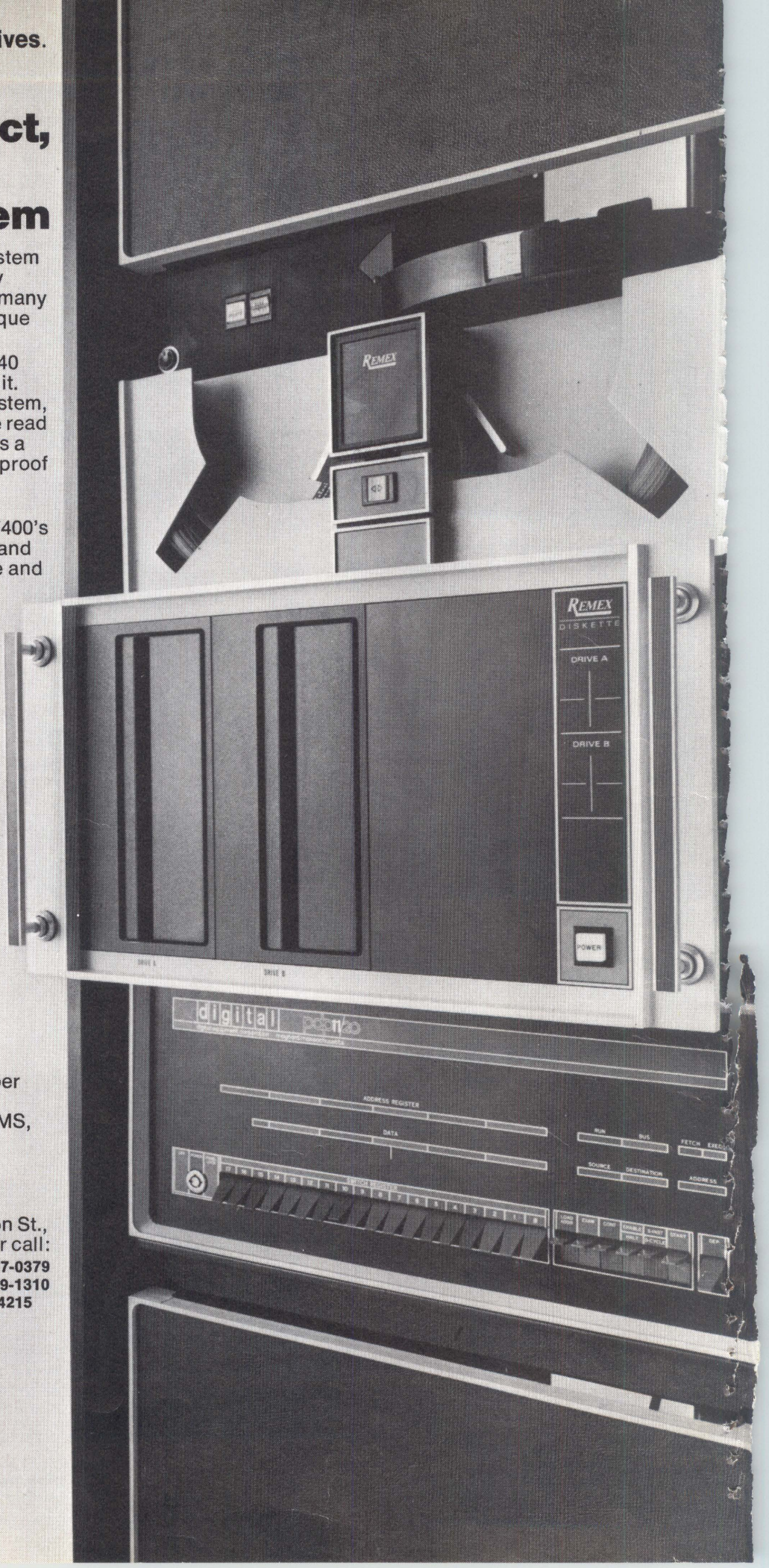
CIRCLE 3 ON INQUIRY CARD



THE MAGAZINE OF DIGITAL ELECTRONICS

COMPUTER DESIGN

JULY 1975 • VOLUME 14 • NUMBER 7

Varying from our usual policy of choosing a front cover that portrays the theme of the lead article in each issue, our cover this month depicts the tie-in between the U.S. Bicentennial and the town "where it all began," Concord, Massachusetts. We at *Computer Design* are honored to be based in this historic town, which, in addition to its unique background, is surrounded by one of the major concentrations of the computer industry. Although we realize that those of our readers who visit Concord during this Bicentennial year will have many historical sites to see, we extend an open invitation to visit our offices while you are in the area.

DEPARTMENTS

BPA CIRCULATION OVER 55,000

FEATURES

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Concord, MA 01742
Tel. (617) 369-6660

Editorial manuscripts should be addressed to Editor, Computer Design, 221 Baker Ave, Concord, MA 01742. For details on the preparation and submission of manuscripts, request a copy of the "Computer Design Author's Guide."

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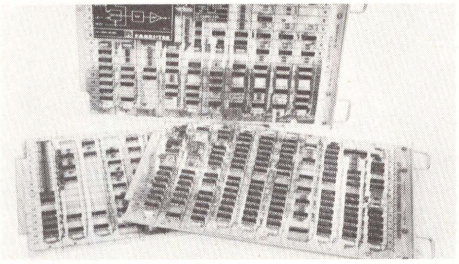
Want to simplify control system design?

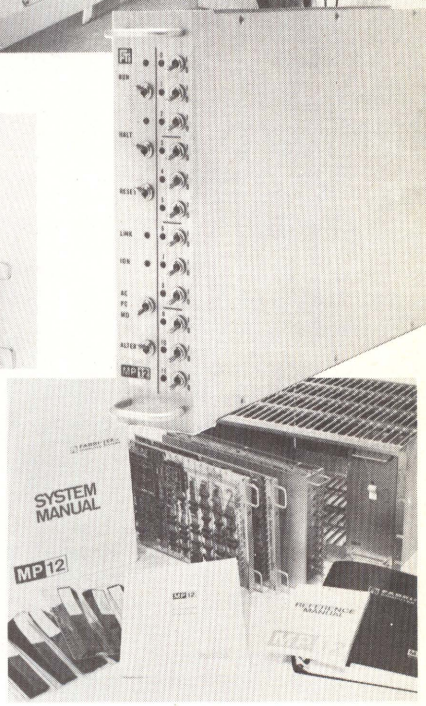
Try the MP12 Microcomputer.

DESIGNED FOR CONTROL — If you're designing control elements into a process or industrial control system, consider the MP12 Microcomputer. It's a highly versatile, powerful system that makes the job easier than ever before. Fully operational CPU. Easy-to-use standard interface cards. Plus a complete basic software package.

LOW COST — The MP12 is ideally priced for dedicated control applications. The CPU, with 4K memory, control panel, DMA channel, interrupt facility, power-fail/auto-restart, and basic software, is $990 in quantities of 100. Peripheral interface cards are as low as $161. Compare price/performance with any other microcomputer or minicomputer on the market. There's no comparison.



EASY INTERFACING — Interfacing to peripheral equipment and process control devices is a snap with the MP12 Microcomputer. Standard interface cards allow you to interface directly to the CPU or wire wrap your own custom interface electronics. Cuts engineering time and money drastically.



REAL-TIME SOFTWARE — The RTX12 Real-Time Operating System, together with a full set of basic software, provides the foundation for writing, debugging, and running control-oriented application programs. Nothing is more important than software — and nothing simplifies the job like the MP12 with RTX12.

Specify the MP12 Microcomputer for your control system. You won't find a simpler solution.

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CIRCLE 5 ON INQUIRY CARD

CALENDAR

CONFERENCES

Aug 12-14—Sym on Simulation of Computer Systems, Nat'l Bureau of Standards, Boulder, Colo. **Information:** Donald Deutsch, Technology Bldg, Rm A265, NBS, Washington, DC 20234

Aug 19-22—Sagamore Computer Conf on Parallel Processing, Sagamore, NY. **Information:** Prof T. Feng, Conf Chrmn, Syracuse U, Dept of Elec & Comp Eng, Link Hall, Syracuse, NY 13210. Tel: (315) 423-4445

Aug 24-30—IFAC/75: 6th Triennial World Congress of the Internat'l Federation of Automatic Control, Boston/Cambridge, Mass. **Information:** IFAC/Secretariat, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

Sept 1-5—2nd World Conf on Computers in Education, Marseilles, France. **Information:** Amer Federation of Information Processing Societies (AFIPS), 210 Summit Ave, Montvale, NJ 07645. Tel: (201) 391-9810

Sept 3-5—Computer Hardware Description Languages & Their Applications, City U of New York. **Information:** Prof Stephen Y. H. Su, Workshop Chrmn, Dept of EE, The City College, City U of New York, New York, NY 10031. Tel: (212) 690-5392

Sept 9-11—COMPCON 75 Fall: IEEE Computer Soc Conf, Mayflower Hotel, Washington, DC. **Information:** Gen'l Chrmn, Dr Richard E. Merwin, Army BMD Prog Office, 1300 Wilson Blvd, Arlington, VA 22209. Tel: (202) 694-5282

Sept 11-12—Nat'l Bureau of Stds 1st Nat'l Conf on Software Engineering (immediately following COMPCON), Mayflower Hotel, Washington, DC. **Information:** Software Engineering, PO Box 639, Silver Spring, MD 20901

Sept 16-19—WESCON: Western Electronic Show & Conv, Brooks Hall/Civic Audit, San Francisco. **Information:** Don Larson, WESCON Gen'l Mgr, 3600 Wilshire Blvd, Los Angeles, CA 90010. Tel: (213) 381-2871

Sept 17-19—ASME Design Automation Conf, Statler-Hilton Hotel, Washington, DC. **Information:** Paul Drummond, Meetings Dept, Amer Soc of Mechanical Engineers, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

Sept 22-23—SIGMICRO/IEEE Comp Soc 8th Annual Workshop on Microprogramming (Micro 8), Palmer House, Chicago. **Information:** Conf Chrmn, William Lidinsky, Argonne Nat'l Labs, Applied Math Div, 9700 S Cass Ave, Argonne, IL 60439. Tel: (312) 739-7711, X4302

Sept 23-25—2nd EUROCOMP (European Computer Conf), Heathrow Hotel, London (England) Airport. **Information:** Online, Brunel U, Uxbridge, Middlesex, England

Sept 23-25—IEEE Cybernetics & Society Internat'l Conf, Hyatt Regency Hotel, San Francisco. **Information:** L. S. Coles, Artificial Intelligence Ctr, Menlo Park, CA 94025

Sept 29-Oct 2—IEEE Canadian Reg Internat'l Electrical/Electronics Conf & Exhibition, Automotive Bldg, Exposition Park, Toronto. **Information:** T. W. Purdy, 237 Parkview Ave, Willowdale, Ont, Canada

Oct 1-3—3rd Internat'l Industrial Electronics Congress, Torino, Italy. **Information:** Chrmn Exec Comm, Dr Ing. Giovanni Villa, Corso Massimo d'Azeglio 15, 10126, Torino, Italy

Oct 5-8—Electronic & Aerospace Systems Conv (EASCON), Twin Bridges Marriott Hotel, Washington, DC. **Information:** IEEE, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

Oct 6-9—ISA-75: Instrument Society of America Conf & Exhibit, Mecca Hall, Milwaukee, Wis. **Information:** ISA, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

Oct 7-8—9th Annual Instrumentation & Computer Fair, Sheraton Inn/Washington-Northeast, Washington, DC. **Information:** Robert Harar, Exec Dir, Instrumentation Fair, Inc, 5012 Herzel Pl, Beltsville, MD 20705. Tel: (301) 937-7177

Oct 7-9—IEEE Computer Soc 4th Data Communications Sym, Hotel Le Concorde, Quebec City, Quebec, Canada. **Information:** Dr Tom B. Grandy, Bell-Northern Research, PO Box 3511, Station C, Ottawa, Ont, Canada K1Y 4H7

Oct 7-9—IEEE Internat'l Sym on Electromagnetic Compatibility, El Tropicano Motor Hotel, San Antonio. **Information:** EMC, PO Drawer 28510, San Antonio, TX 72284

Oct 13-14—Information Processing Assoc of Israel (IPA) 10th Nat'l Data Processing Conf, Binyanei, Ha'ooma, Jerusalem. **Information:** NDPC, c/o Kenes Ltd, PO Box 16271, Tel Aviv, Israel

Oct 13-15—16th Annual Sym on Foundations of Computer Science, Berkeley, Calif. **Information:** Sheldon B. Akers, General Electric Co, Bldg 3, Rm 223, Electronics Park, Syracuse, NY 13210. Tel: (315) 456-3067

Oct 14-16—IEEE Internat'l Conf on Advanced Signal Processing Technology, Lausanne. **Information:** Secretariat "Journées d'Electronique," Ch. de Bellerive 16, 1007 Lausanne, Switzerland

Oct 22-23—8th Annual Connector Sym, Cherry Hill, NJ. **Information:** Electronic Connector Study Group, Inc, PO Box 3104, Philadelphia, PA 19150

SEMINARS

Aug 11-13—Hybrid Microelectronics Institute, U of Pittsburgh. **Information:** Minor C. Hawk, Asst Dean, 231 Benedum Eng Hall, School of Eng, U of Pittsburgh, Pittsburgh, PA 15261. Tel: (412) 624-5253

Aug 12-14—Structured Programming; **Aug 19**—Computerized Conferencing; **Aug 20-21**—Computer Simulation Programming; New Jersey Institute of Technology. **Information:** Remus Klimaski, Div of Cont Ed, NJIT, 323 High St, Newark, NJ 07102. Tel: (201) 645-5235

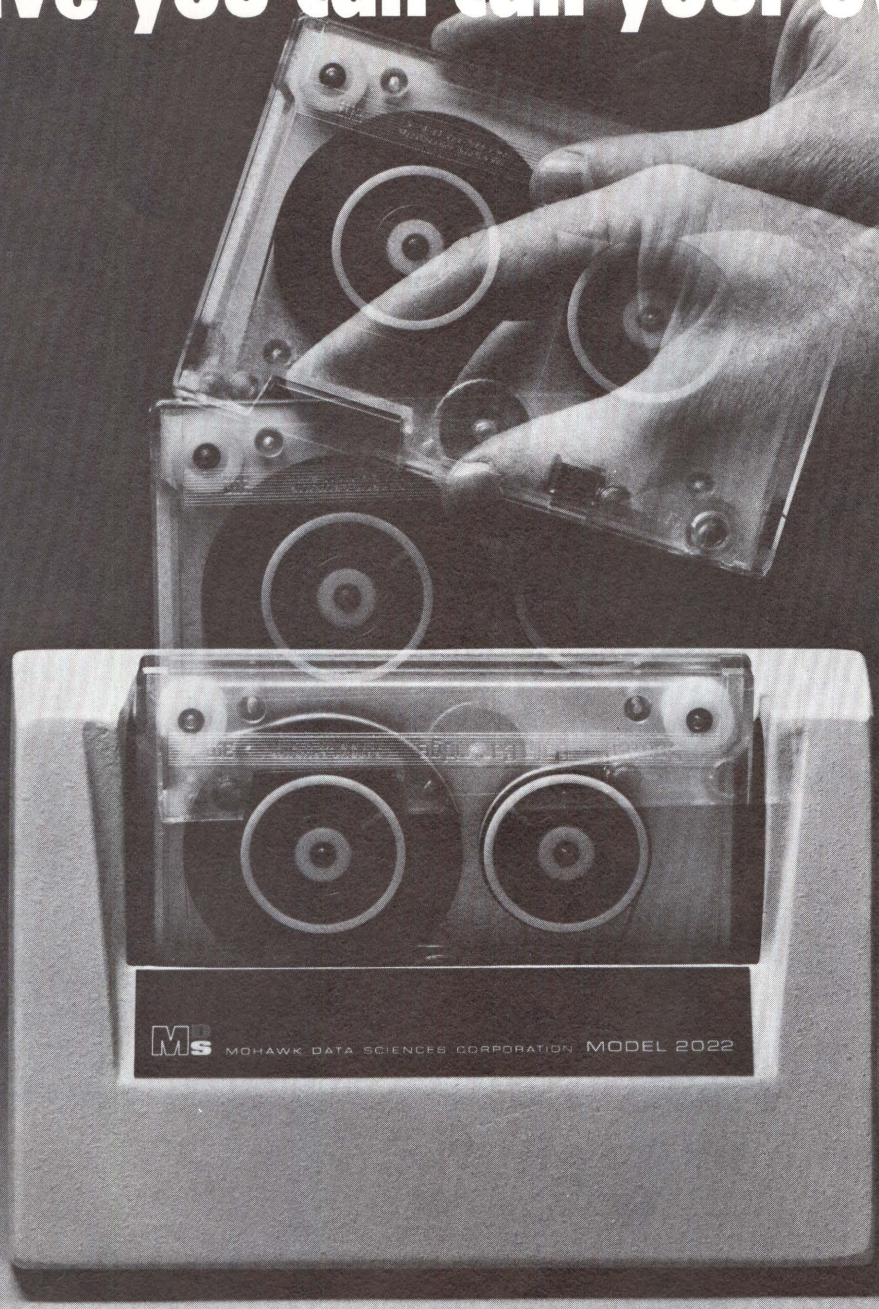
SHORT COURSES

July 28-Aug 1—Modern Digital Communications; **Aug 25-29**—Digital Integrated Circuits; **Sept 8-9**—Minicomputer Programming/Interfacing Techniques; **Sept 10-12**—Engineering Applications of Minicomputers, George Washington U. **Information:** Director, Cont Eng Ed, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

Sept 22-26—Applications of Digital Computers to Process Control, Purdue U. **Information:** Div of Conferences/Continuation Services, Stewart Ctr, Purdue U, West Lafayette, IN 47907. Tel: (317) 749-2062

Sept 22-26—Total Software Management; Programming Language Implementation; **Oct 27-31**—Writing Technical Communications; **Dec 8-12**—Digital Computer Solution of Partial Differential Equations, U of California-Los Angeles. **Information:** Dept of Eng, Short Courses, UCLA Ext, PO Box 24902, Los Angeles, CA 90024. Tel. (213) 825-1295

We make the OEM cartridge tape drive you can call your own.



They're tough on competition and modestly priced. To the engineering excellence of the 3M data cartridge, we added a precision drive, based on high-speed reel-to-reel tape drive technology.

In the current models 2021 and 2022, you can quickly discover the long-needed replacement for paper tape, cassettes, or whatever you've tried for input programs.

You can also discover low-cost intermediate storage for minicomputers, as well as a reliable maintenance-free peripheral for remote data collection, communications terminals, and POS systems.

Performance features include: 30-ips read or write, 90-ips search and rewind, read-after-write check, 250 to 1600 bpi, phase or bi-phase encoding on 1, 2, or 4 tracks, and total capacity of 23 million bits.

Design simplicity in the MDS Cartridge Drive is based on a rugged casting, with a fixed position, dual-gap read-after-write head, interchangeable circuit cards, and a long-life drive motor.

Discover a new standard for low-speed tape drive price/performance. It all starts with your inquiry. Phone 215/337-1910, or write:
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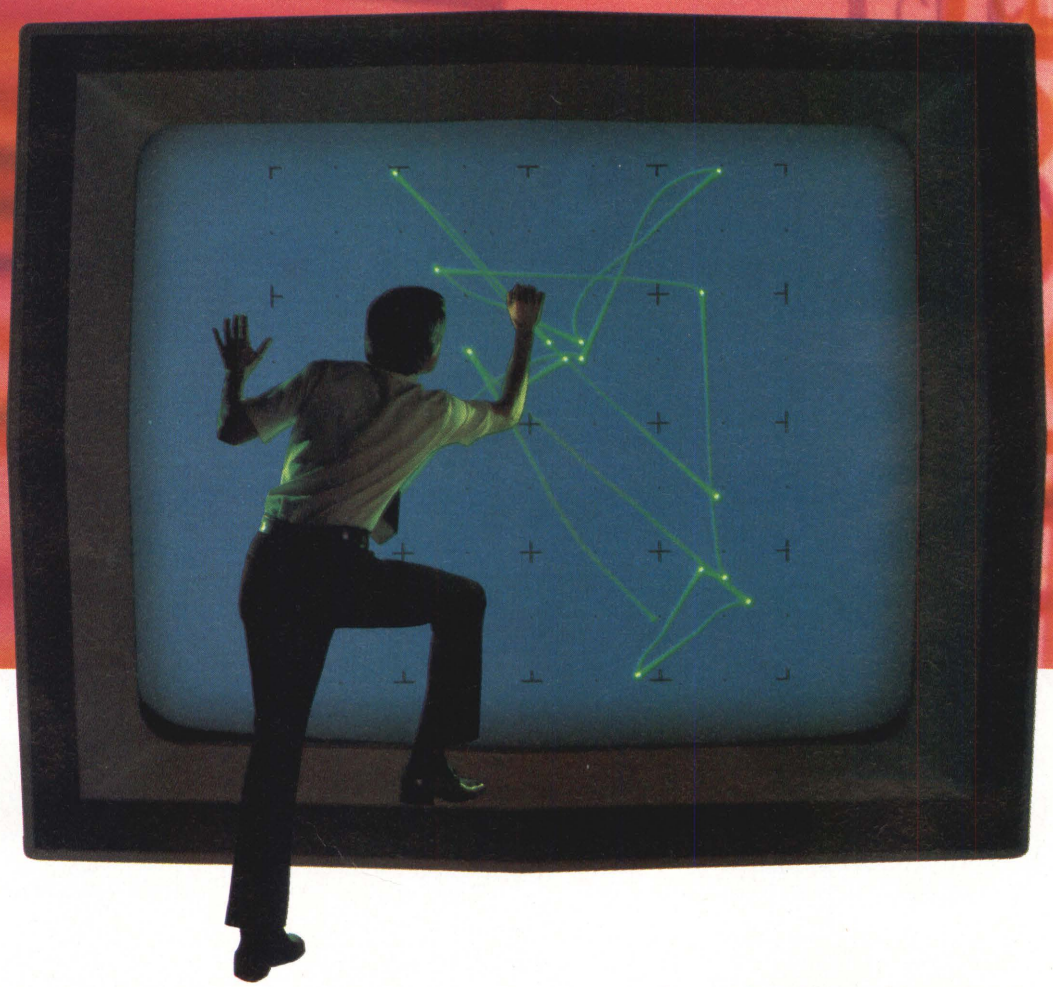
With two new ways to get inside your



HP invites you to step inside your 16-bit parallel circuits for an overall view—and a detailed view—of logic-circuit operation. How? Just connect our new 1600A Logic State Analyzer to an operating circuit, and view actual logic states on the CRT—at clock rates to 20 MHz. Select the data you want to observe with pinpoint accuracy. And choose from two display methods for viewing the data words.

What does this mean to you? It means a better way to see hardware and software in action . . . a faster way to spot problems and find solutions. For example:

In the mapping mode, the 1600A can display all possible combinations of its 16 data-channel inputs—over 65,000 in all. Each input combination or "word" appears as a discrete point whose location on screen identifies its address. Spot intensity shows relative frequency of occurrence, and the vectors show the sequential state locations.

This mode converts parallel data into a pattern that your eye can easily scan to quickly spot changing conditions or unusual events. You can even expand the view to zoom in on data of interest. And, with a curser, locate the address of any spot. You can then use the address as a trigger point for a detailed look with the tabular display, or to trigger your scope for electrical analysis.

In store and compare mode, the 1600A triggers on any preset word up to 16 bits wide. The analyzer then displays the trigger word and 15 sequential words before, after, or surrounding the trigger word, so you can easily analyze logic states in detail. You can store one table of data and compare it with an active data display . . . have the analyzer compare the two tables and give you a display of logic differences on a bit-by-bit basis for easy comparison . . . or you can set the instrument to automatically halt when all the data in one table isn't identical to data in the second—freeing you from the tedious task of waiting and watching for infrequent sequences.

And that's just the beginning. The 1600A gives you qualifier inputs to help locate the specific data you want on a busy bus. It gives you a sequential trigger by providing a trigger arm that inhibits the word trigger until an arming signal is received. You can

hrough

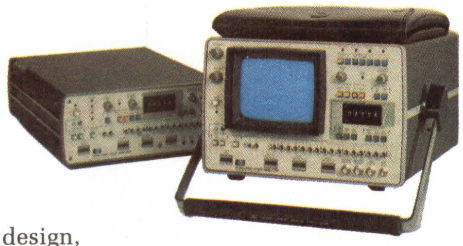
logic designs: Mapping..... Store and compare.

delay the display up to 99,999 clock pulses from the trigger point, which lets you look virtually anywhere in your program flow.

The 1600A, priced at $4,000*, gives you new insight to operating logic circuits. With 16-bit word size, parallel operation, and 20 MHz speed, it's the ideal instrument for designers of minicomputers, peripherals, microcomputers, and microprocessor-based systems.

If 16-bit words aren't enough, our new 1600S, priced at $6,800*, displays words up to 32 bits wide. This powerful system includes both the 1600A and our new 1607A Logic State Analyzers. Hook it up to your 16-bit machine, and in single clock you can look at both the data and address simultaneously. In dual clock, you can view two independent active tables of 16 bits each—synchronized together through the bus triggering capabilities.

When you have all the details, you'll see how these new logic-state analyzers put you inside your logic programs for a better overall picture... and for a clear detailed look. And you'll see how they can save you hours in design, debugging and troubleshooting. For the complete story, just contact your local HP field engineer. Or, write for our new 8-page data sheet on Logic State Analyzers.



For low-cost logic state analysis and electrical measurements too, add HP's new 1607A to your present scope and have a complete digital system ...see the next page for details.

*Domestic USA price only.

085/7

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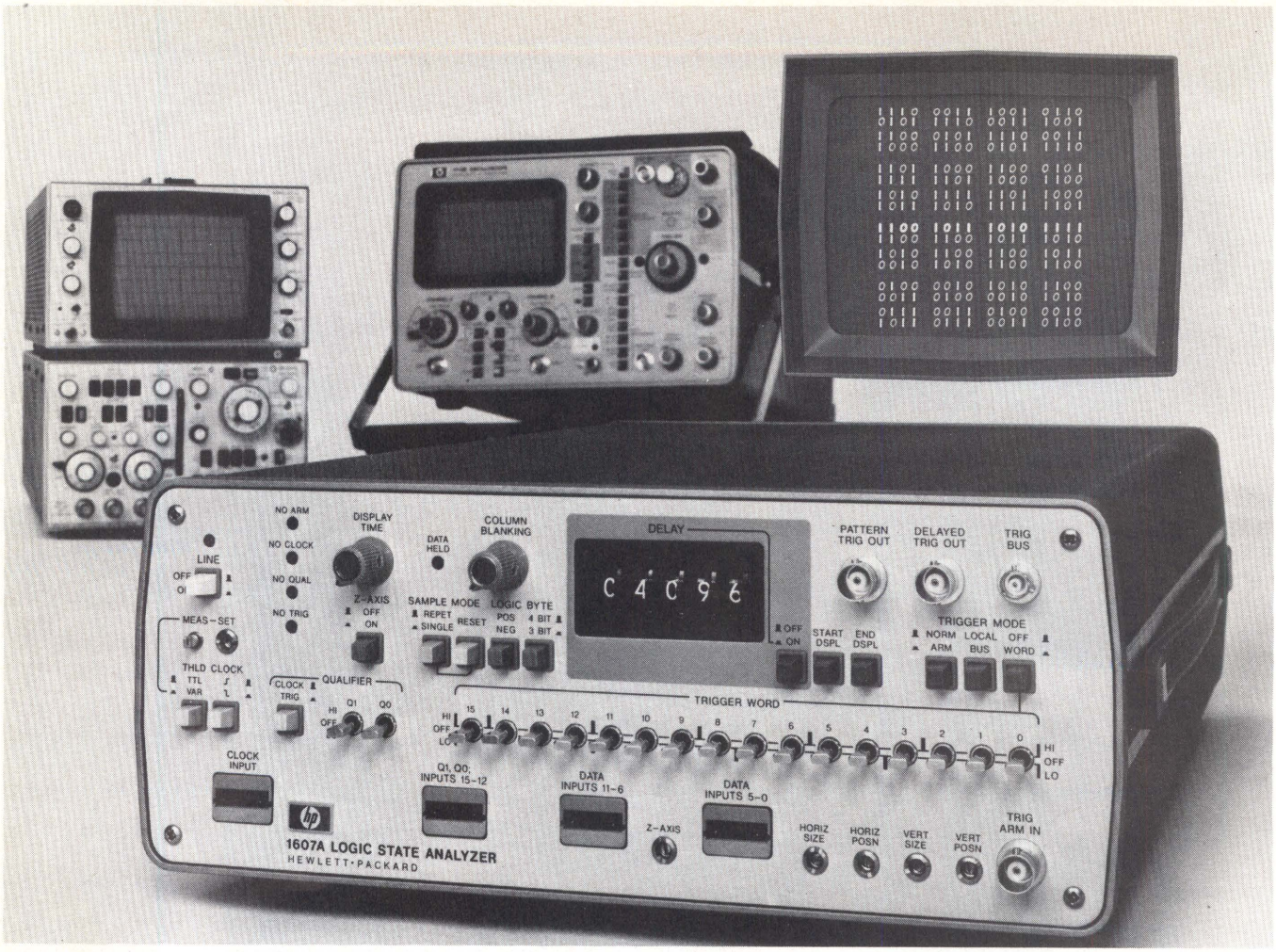
For immediate applications assistance, circle 8 on Inquiry Card.



Introducing a powerful new team to speed logic analysis - HP's 1607A and your present scope.

You already have half of a complete digital-analysis system ... the scope you've been using for level and timing measurements. The other half is HP's new 1607A Logic State Analyzer. Simply make four BNC connections, and you have a combination logic analyzer and oscilloscope—a complete analysis system for the digital designer.

Data domain or time domain. In the data domain, the system shows you a display of logic states in operational circuits so you can pinpoint a program problem. Then, in the time domain, the 1607A triggers your scope at the point where the problem occurs so you can analyze the electrical characteristics of the waveform using the conventional scope input. Now you can really pin down those hardware/software compatibility problems.

Parallel words to 16 bits. The 1607A triggers on any preset word up to 16 bits wide ... and at clock speeds to 20 MHz. In the data domain, it displays—on your scope's CRT—15 sequential words before, after, or surrounding the trigger word. You see the bits as 0's or 1's for easy analysis of your circuits or programs—while they're operating full speed.

Qualifier inputs help locate data. If you're looking for specific data on a busy bus, the 1607A's qualifier inputs let you selectively extract data of interest. In addition, a trigger arm gives you a sequential trigger by inhibiting the word trigger until an arming signal is received. You can delay the display up to 99,999 clock pulses from the trigger point, which lets you look virtually anywhere in your program flow.

With the 1607A, and your scope, you can select the data you want to observe with pinpoint accuracy ... then observe either logic states or electrical parameters.

Drives a scope or display. The 1607A, priced at just $2,750*, drives nearly all modern scopes. You can even combine the logic state analyzer with a large-screen CRT display for easy viewing at a distance, such as a classroom situation.

Put this team to work in program analysis of microprocessor based systems ... for microprogram analysis in minicomputers ... or in situations where flow diagrams are the best way to describe your design. You'll find that its detailed view will result in faster design and debugging. And easier troubleshooting.

There's more to learn about this new logic-state analyzer ... and how it gives you a better way to see hardware and software in action for faster solutions to your digital-design problems. Get all the details by contacting your local HP field sales engineer. Or by writing for the 8-page data sheet on HP's new Logic State Analyzers.

*Domestic U.S.A. price only.

085/5

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Unbundled Communications Services

Data communications customers of both equipment and services are often unsure as to exactly what the cost components are which comprise a stated price or fee. Questioning whether users of a particular device are actually receiving all the services whose costs are included in its price is legitimate; vendors have been known to use revenue from more profitable, less competitive products or services to subsidize those that are less profitable and more competitive.

Not long ago, data processing news headlines reported a series of developments that resulted in a number of manufacturers redefining their pricing structures. Under both direct and indirect government encouragement, some of the major computer manufacturers—particularly IBM—separated equipment, software, and technical support costs into individual pricing elements, while others, such as Univac, decided to retain the traditional single pricing concept. The former group is referred to as "unbundled"; the latter, "bundled" suppliers.

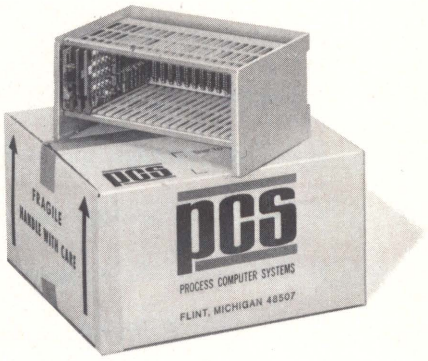
Many arguments eloquently defend the properness of each position. Typically, the more sophisticated, self-reliant user is attracted to the unbundled structure; in this environment he can pick and choose the services he requires to complement his own data processing staff. In the opposite position is usually the user without an extensive internal support organization and who therefore feels that greater value is realized through the bundled approach.

Such considerations are also resident with data communications users as they view the various common carriers. Traditionally, these regulated vendors provide communications services and equipment necessary for the user to accomplish a desired exchange of information with remote locations. Prices they charge are defined in approved tariffs and are based on the costs of providing such equipment and services. In addition, among the numerous items provided by the various telephone companies, a considerable amount of cross-subsidization takes place.

Last month, "Communication Channel" analyzed recent significant changes in rates for switched communications services (DDD [direct distance dial] and WATS [wide area telephone service]). Not only were the rate amounts redefined, but actual rate structure and alignments were modified—with the major burden of the resulting increase appearing to fall on the business-day data communications user. To be able to identify the individual cost components actually applied to justify these new business-day rates would be interesting. Based on past experience, chances are that several relate only indirectly to the services provided.

Recently, communications common carriers—including AT&T—warned that customer-owned communications equipment such as modems, telephones, PBXs (private branch exchanges), and the like, will significantly impact the basic telephone service customer. Reason: part of the revenue from this equipment is used to subsidize or support network services. If this revenue is lost to competition by users purchasing their own data sets, costs of subsidized network services, such as DDD, must then increase. A study conducted by the New York Public Service Commission's Communications Div indicated that by the end of 1973, New York Telephone Co had lost 27.7% of its data set customers and, because of interconnection, was required to increase by over $5.3 million its revenues from

Two reasons why Micro



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switched services. The study projected that with the growth of interconnection continuing, the loss in subsidizing revenue to the switched services would amount to $181 million. It concluded that all New York Telephone switched service subscribers "will probably experience significant increases in the cost of basic service as a result of interconnection." Ironically, the report acknowledged that while interconnection "does provide a choice of alternatives," . . . for "the majority of telephone subscribers there is at present no cost advantage . . . because of the expense of interfacing with the telephone system."

In the context of interconnection impacting traditional revenue/cost cross-subsidization, AT&T had asked the Federal Communications Commission that, under FCC Tariff 263 (Long-Distance Message Telecommunication), certain, smaller interconnecting telephone companies be exempt from having to allow the use of customer-owned equipment such as data sets. The Mebane (NC) Home Telephone Co, identified as the subject telephone company in this test filing, stated that its economic survival would be seriously jeopardized if it had to permit use of customer-owned communications equipment—due to the loss in subsidizing revenue.

These cases illustrate potential problems that have developed during periods of bundled operation. While the studies allude to the root cause being interconnection, one must question if interconnection is not merely the unfortunate catalyst that has created visibility into this impossibly intertwined revenue/cost allocation environment.

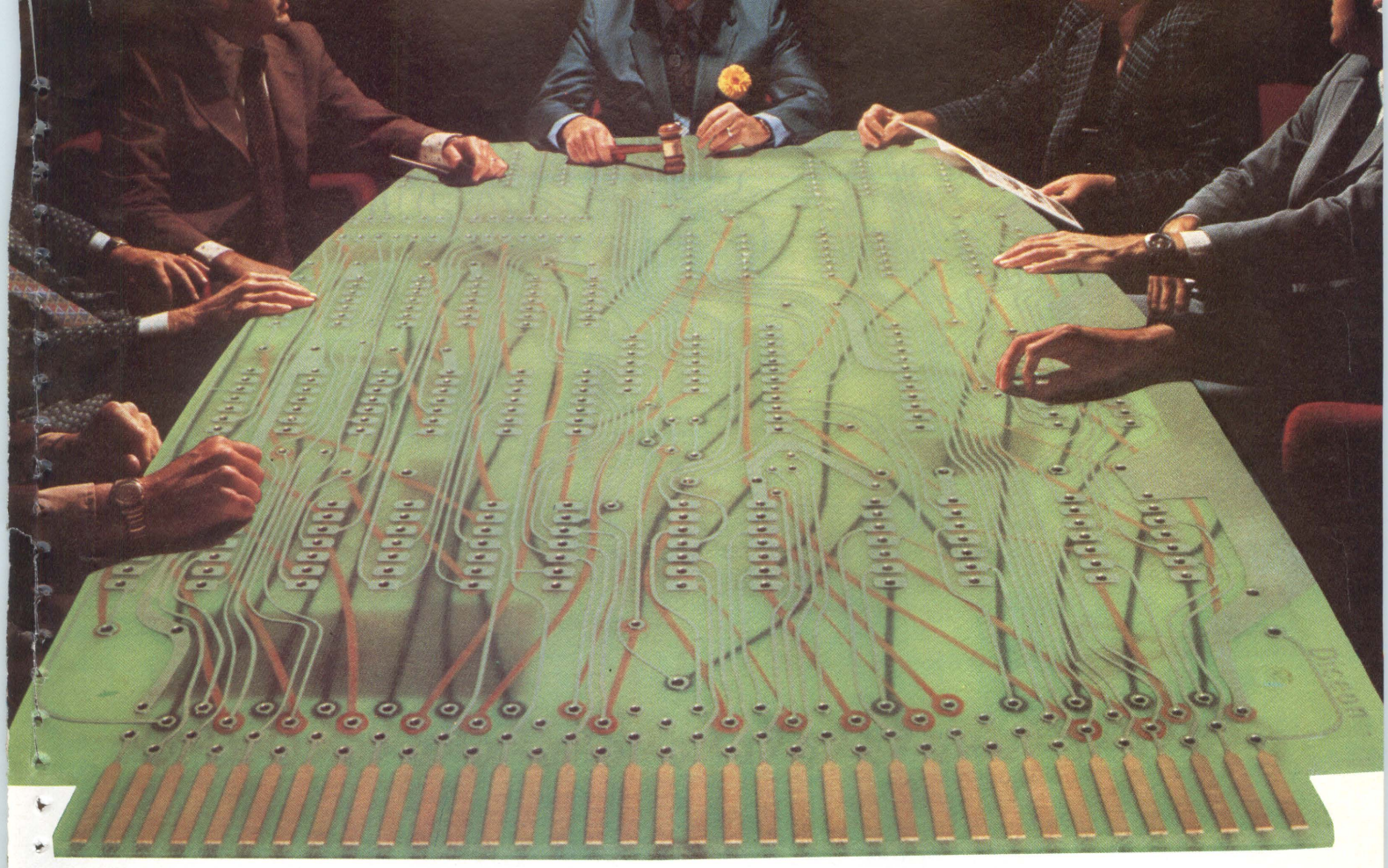
Elimination of the catalyst is hardly the solution to this problem. A parallel situation might be a system pricing scheme whereby half the central processing unit (CPU) revenue subsidizes peripheral costs, half the peripheral revenue subsidizes software costs, half the software revenue subsidizes CPU costs, and so on. Vendor arguments to prohibit customer-provided software might contain the same points we are encountering with interconnection.

Data communications users also find sometimes that the level of technical system support provided by a common carrier can vary significantly, depending on the amount of their monthly bill. Support can range from an occasional customer-initiated conversation with a telephone company data communications expert to on-site staffing of telephone company engineers. These consultation services—from cursory advice to complete network studies and recommendations—mean expenses to the telephone company, and are compensated for by a universal cost element in the tariff rates. As user requirements for expanded system evaluation increase, the telephone companies, stimulated by interconnection, are attempting to provide more comprehensive analysis services, some of which can become so extensive that they begin to approach the scope of facility management activities.

Communications common carriers are essentially bundled, and factor into their rate justifications all of their operating costs, whether universally or selectively available. That the rate paid for a long-distance call in the eastern U. S. is being used in part to pay for a leased-line network study for a California-based company is quite possible. The equitability of this type of arrangement will be the subject of many future debates and rulings, and today's data communications users will be expected to contribute their views and recommendations to the resolution of this developing controversy. The traditional communications common carriers tend to isolate interconnection as the cause of the recent rate increases and suggest that for this reason even more significant economic penalties will be experienced in the future.

As with the data processing industry a few years ago, the requirement to unbundle equipment and services and for direct cost and revenue allocation may be imposed on the telecommunications industry. All of its users—particularly data communications—must directly and intelligently participate in the resulting decision. Only then can a compatible environment for its future growth be insured. □

Opinions expressed are not necessarily those of *Computer Design*.



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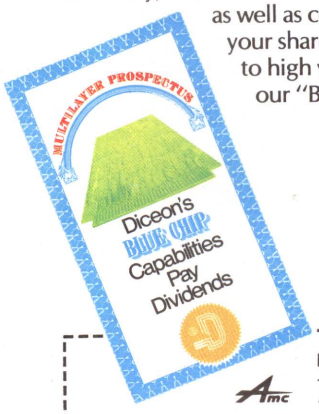

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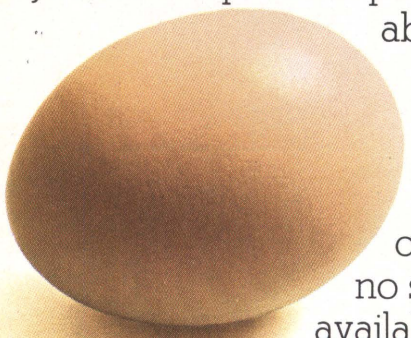
CIRCLE 13 ON INQUIRY CARD

How to buy a m

Which comes first—the hardware or the software? You need both, of course, to create new products with microcomputers. The tougher question is: How do you assure product profitability? That gets you into questions of hardware availability, software support, design assistance and confidence in your supplier. When an electronics publication recently asked readers to rank their microcomputer buying criteria, it came as no surprise to Intel that availability, software support and supplier reputation topped the list.



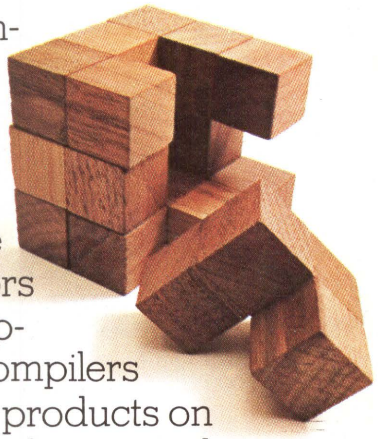
Intel can supply you today with five general-purpose CPUs, supported by numerous peripheral, I/O and memory components, software packages and development manuals, and the industry's largest library of users' applications programs. Our five microcomputers span a 1000:1 performance range and include the lowest cost, highest performance and most popular designs available today. Their applications are equally broad, from electronic games to high speed controllers and processors. We want to make sure that our customers don't begin designing with pieces of the hardware/software puzzle missing. To minimize development and assembly cost, each CPU is backed up by more than a score of performance-matched system components—advanced programmable I/O

INTEL MICROCOMPUTER SYSTEM FAMILIES

MICROCOMPUTER SYSTEM	MCS™-4	MCS™-40	MCS™-8	MCS™-80	Series 3000
CENTRAL PROCESSOR	4004	4040	8008	8080	3001, 3002, 3003
Technology	PMOS	PMOS	PMOS	NMOS	Schottky Bipolar
Parallel Bits	4	4	8	8	2 per 3002 CPE
Instruction Cycle	10.8μS	10.8μS	12.5μS	2μS	100nS
SUPPORT COMPONENTS					
RAMS (including CMOS)	4	4	5	5	8
PROMS	3	3	3	4	7
ROMS	4	4	3	3	6
*Peripheral Interfaces	6	6	6	6	8
Interrupt Unit			1	1	1
Clock Generator	1	1	1	1	TTL
*I/O Units	5	5	3	3	3
Total Component Choices	23	23	22	23	33
SYSTEMS SUPPORT					
Software Packages					
Microassembler					1
Assemblers	2	2	2	2	
Compiler			1	1	
Monitor	1	1	1	1	
Simulator	1	1	1	1	
Text Editor			1	1	
Manuals	6	6	5	6	1
User's Library	Yes	Yes	Yes	Yes	Yes
Intellec® Development System	Yes	Yes	Yes	Yes	In development

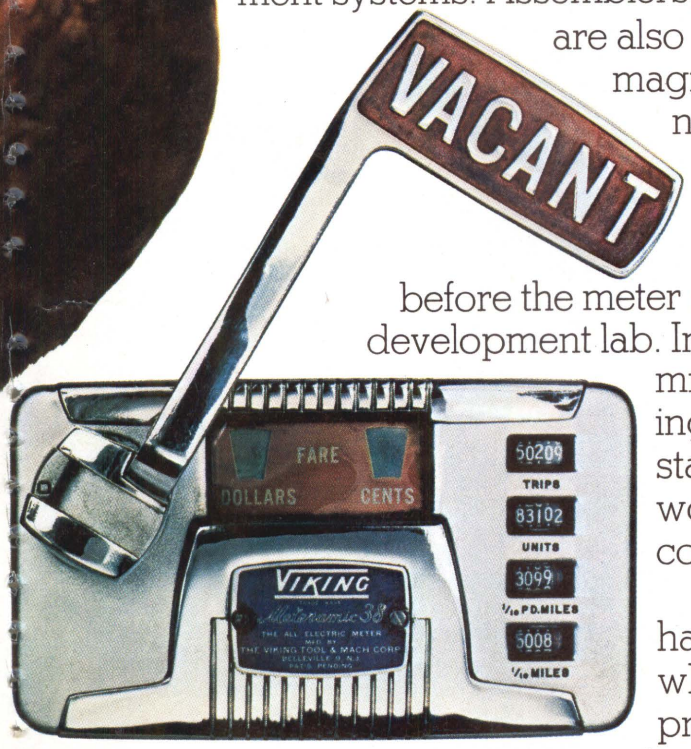
* Five additional I/O and peripheral devices will be available in 2nd half of 1975.

icrocomputer.



subsystems, peripheral interfaces, clock generators, priority interrupt and other control units, and the broadest selection of erasable and bipolar PROMs, compatible metal mask ROMs, CMOS and NMOS RAMs.

Moreover, Intel software packages include resident monitors, assemblers and text editors available on Intellec® microcomputer development systems. Assemblers, simulators and compilers are also available as cross products on magnetic tape or on leading time share networks. With these aids programs can be written and debugged in a fraction of the time required a few years ago.



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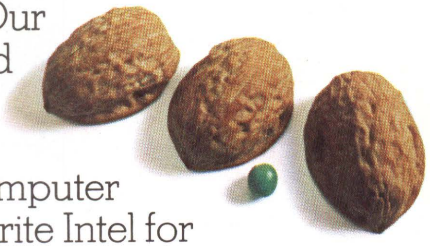

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CIRCLE 14 ON INQUIRY CARD

Mass Storage System Moves Data Directly from Cartridge to Computer

Capable of storing 16 billion characters of online data, the CDC 38500 Mass Storage System is claimed to store and transfer data with the speed and convenience of disc methods at the cost of magnetic tape. Under control of from one to four IBM System/370 computers, the system can transfer data directly to the computers or by way of intermediate disc devices.

Introduced by Control Data Corp, Minneapolis, MN 55440, the system consists basically of a mass storage facility (MSF) and a disc storage subsystem (CDC 38302/3330X or equivalent). Storing 2000 data cartridges in a 10-ft long bank of cells, the MSF includes a selector mechanism, which automatically locates the necessary cartridge; and from two to four automatic read/write stations, which are mechanically coupled to the cartridge storage unit.

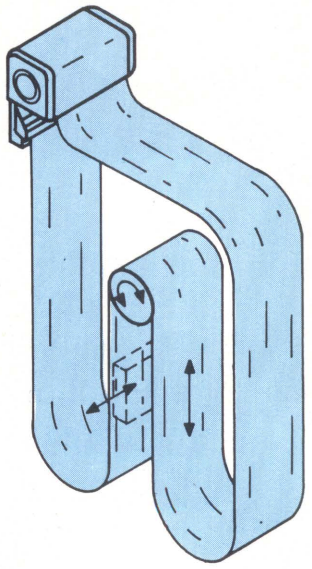
The desired cartridge is selected from the storage magazine by an X-Y selector and is moved to the front of the read/write station. Each read/write station contains two vacuum columns, a single tape drive capstan, and two sets of read/write heads. The cartridge is opened automatically and the magnetic tape is unwound and drawn into a vacuum column. Tape movement can be continuous or incremental. The single capstan motor provides fast start/stop operation, with an 806-kilobyte/s data rate. Tape is moved in alternate directions while the heads read or write. After processing, the station rewinds the tape and transports the cartridge back to its position in the file magazine.

Direct facility-to-computer data transfer is accomplished using Virtual Data Set Access Method (VDAM) software which interacts with the /370 operating system through normal user calls. Its user-sequential capability allows the computer to directly access data sets stored in the cartridges without first staging data to the disc. Data are then processed in sequential operating mode, identical to that used in tape processing. The user-direct-transfer method allows specific blocks to be requested from within a designated data set. VDAM accesses the necessary cartridge, locates the block, and transfers it directly to the computer without intermediate staging to disc.

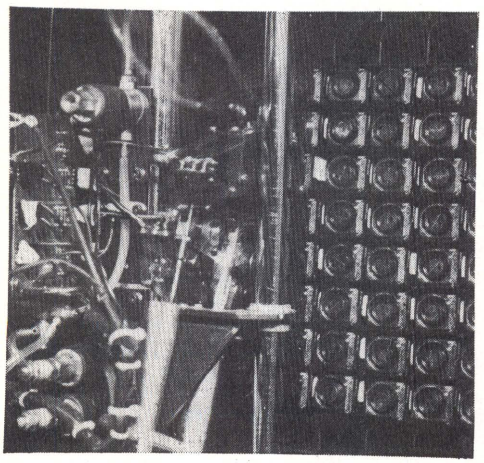
In addition to direct data transfer capabilities, VDAM also performs mass storage facility operating functions to stage and archive data using normal OS/MVT, MFT, or VS1 and VS2 operating system procedures. When a data set within the MSF is needed for a job, VDAM determines data set size and requests the appropriate disc space from the operating system. When disc space is available, the system selects the cartridge, moves it to the read/write station, and reads data from mass storage to disc. Since the job is carried through its initiation function simultaneously with staging operations, job processing is not impeded.

A basic 38500 system includes a 2000-cartridge capacity file unit with two read/write stations, disc storage controller, control adapter unit, and VDAM software; purchase price is $326,335. Increased capacity can be attained by adding individual file units, read/write stations, mass storage adapters, and control units. First customer shipments of the system are scheduled for fourth quarter 1976.

Circle 150 on Inquiry Card



Each cartridge contains approximately 100" of 2.7" wide magnetic tape which is never detached from the protective housing. To read or write data on tape, the cartridge is automatically opened and tape is unwound into two vacuum columns. The two read/write heads cover 18 tracks in one position, moving eight times to fully cover the 144 tracks



Each Control Data mass storage file uses programmed, automatic selector mechanism to pick and move data cartridges to information transfer points, completing a 1-way trip in approximately 2 to 3 s

Virtual Memory Computers Packaged for OEM and Time-Sharing Users

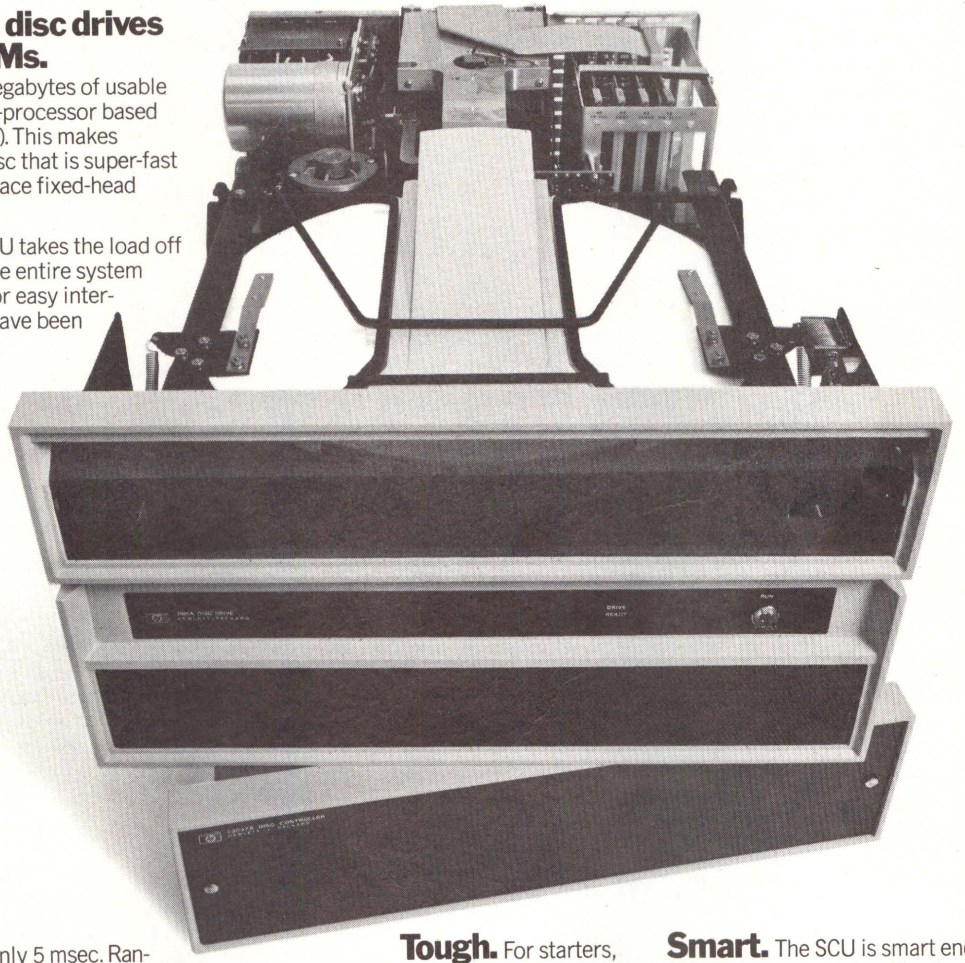
Ranging from a basic OEM building block for dedicated computing functions to a large configuration packaged for systems users who require substantial amounts of memory, virtual memory computer systems, introduced by Harris Corp's Computer Systems Div, 1200 Gateway Dr, Fort Lauderdale, FL 33309, provide numerous internal options and performance-enhanced peripherals to pro-

Hewlett-Packard Introduces: DISCU/15 for OEMs. Fast. Tough. And Smart.

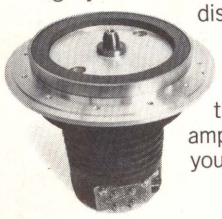
A new concept in disc drives especially for OEMs.

DISCU/15 combines 15 megabytes of usable disc capacity with a micro-processor based Storage Control Unit (SCU). This makes possible a moving head disc that is super-fast and rugged enough to replace fixed-head discs and drums.

And it's smart. The SCU takes the load off your processor to make the entire system faster. Plus it's designed for easy interfacing, something OEMs have been waiting for.

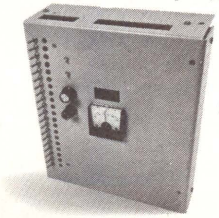


Fast. Track to track in only 5 msec. Random average is 25 msec. The only 3600 RPM cartridge drive. Transfer rate is 937 kilobytes. More capacity in a cartridge: 10 megabytes of removeable storage and 5 megabytes on the fixed disc.

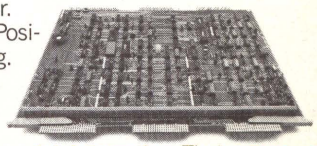


Up to 8 drives per Storage Control Unit give you ample capacity when you need it.

Tough. For starters, a rigid, precision-milled 40 lb. casting really stands up. An integrated spindle and DC Motor eliminates belts and pulleys. And it's designed for use on the open manufacturing floor. A separate blower keeps contaminants out even during cartridge change. The only cartridge disc using track following technology for outstanding reliability. The result: DISCU/15 guarantees interchangeability within the most severe environmental specs available in commercial discs. Easy service too. Even major sub-assemblies are modular for easy replacement. The only equipment you need for major servicing (including head alignment) is a compact Disc Service Unit.



Smart. The SCU is smart enough to be called a minicomputer. Here's what it gives you: multi-CPU capability. Error correction for up to 32 bits per sector. Track switching transparent to processor. Rotational Position Sensing. Command Retry. Plus, a high level interface for quick integration. That means you save time, money and headaches. For all the details, call your nearby HP field sales office.



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CIRCLE 15 ON INQUIRY CARD

vide high performance cost-competitively. Both Series 100 and 200 units operate under the Virtual Core Memory (VULCAN) operating system, which can concurrently support multilevel batch processing, interactive terminal time-sharing, and real-time operation.

S110 and -120 are entry-level systems based on the series 100 processor, which uses single-word addressing, and has a multi-access bus structure and buffered I/O channels. Cycle time is 750 ns. Memories are planar core arrays with 96 or 144 kilobytes capacity, expandable in 48-kilobyte increments to 192 kilobytes.

The -110, a base system, consists of CPU plus 96 kilobytes memory, tape unit, 10.8-megabyte cartridge disc, multiplexer, and console video terminal. Options include multiterminal capability, asynchronous line interface units, scientific arithmetic units, and ability to add a 40/80-megabyte disc system. The S120 with 144 kilobytes of memory adds a low speed printer and high speed card reader to the basic -110, and provides asynchronous/synchronous communications line interfaces, and the ability to add on magnetic tape units, run remote job entry software, and add an 860-kilobyte, fixed-head swapping disc as options.

Series 200 CPUs provide asynchronous operation with a 425-ns minimum cycle time. Standard memories range from 192 to 576 kilobytes capacity and are expandable in 48K increments to from 384 to 768 kilobytes. Internal options include a scientific arithmetic unit, a hardware floating-point processor for high speed execution of double-precision, floating-point arithmetic.

The S210 provides 192 kilobytes of interleaved memory and all equipment of the -120, replacing the 10.8-megabyte disc unit with a 40-megabyte disc and adding an 860-kilobyte fixed-head swapping disc. Single or multiport semiconductor memories are offered as options as are multiported core memory and I/O processor channels in place of chain-block controller channels. Providing effective foreground/background operation, the larger -220 multiprocessing system adds a high speed line printer, high speed card reader, and 1.7-megabyte fixed-head disc to the -210 configuration.

A large-scale multiprocessing system, the S230 is oriented to multi-terminal time-sharing applications. Equipment includes two tape units and multiplexer. Standard hardware on the S240, largest system in the series, includes two 80-megabyte moving-head discs, 2.1-megabyte fixed-head disc, two tape units, two multiplexers, high speed printer, card reader, and console video terminal. Memory is expandable to 768 kilobytes. Like the -230, it functions as host processor and time-sharing system.

Circle 151 on Inquiry Card

Microcomputer Kit Contains Essentials for System Conceptualization

Smoothing the transition from traditional design techniques to those of a microcomputer-based approach, a design package containing microcomputer devices plus all documentation necessary to conceptualize a functional system is being offered in kit form by Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036. The kit contains an MC6800 microprocessor unit (MPU), along with 1K RAM, 8K ROM, peripheral and communications interface adapters, and extensive hardware, programming, and applications documentation.

All devices in the package are TTL compatible, require only a single 5-V supply for operation, and use a single-bus organization that allows memory and I/O elements to share the same address space. (For details, see *Computer Design,* Jan 1975, p 30.) Separate pins are available for all MPU and bus control functions; no multiplexing or decoding is required for operation.

The peripheral interface adapter (PIA) provides a means for connecting the MPU to various peripherals, with data passing between PIA and device over an 8-bit bidirectional bus. The asynchronous communications interface adapter (ACIA) performs serial/parallel data conversion. At the serialized data interface, it is linked to peripheral or modem by three control lines.

RAMs and ROM operate statically and have 3-state outputs. The -L7 version of the mask-programmable ROM that is included in the package is the firmware equivalent of MIKBUG™ and MINIBUG™ software aids. This firmware enables users to interface MPU devices to asynchronous, serial data communications units using PIA or ACIA.

Also provided in the package are a System Reference and Data Sheet Manual, defining device characteristics and system architecture; Programming Manual, detailing specific MPU machine operations and the source language in which programs are normally written, and giving examples of such programs; and descriptions of software aids, including cross-assembler and simulator programs. Techniques associated with data transfer, assigning priorities to service requests, and I/O management are delineated in the Applications Manual, which also details methods for incorporating the microprocessor in peripherals such as point-of-sale and data communications terminals, and considerations and examples of interfacing the devices to keyboards, displays, tape cassettes, floppy discs, and various memories. System development procedures and design techniques such as hardware/software tradeoffs are noted.

The kit will be available for a limited time at $300 in quantities of from one to four.

Circle 152 on Inquiry Card

Solid-State Sensors Provide High Speed, No-Touch Switching

Interfacing directly with industrial logic circuits used in program-controlled systems, solid-state sensing devices operate at increased speeds, provide high reliability, and allow "no-touch" sensing at lower installed system costs. Based on Hall-effect and eddy-current-killed oscillators (ECKOs), the switches, introduced by Micro Switch, a div of Honeywell, Inc, 11 W Spring St, Freeport, IL 61032, include self-contained industrial proximity switches and positioning limit switches.

Two no-touch sensor families, FY and 50FY series, sense all-metal and ferrous-magnetic materials, respectively. All-metals-sensing FY switches are radio-frequency inductive devices operating on the eddy-current principle, whereby eddy currents pro-

15,000,000 bytes plus a 32K word computer:

$17,655.*

The new Hewlett-Packard MX/65 DISComputer.

• The powerful 21MX-M/20 minicomputer and the ultra fast 12962A Disc Subsystem. Now available as a plug-together team.

• No one gives you more for your money at 32K – or anywhere between 8K and 256K.

• Rugged, reliable. Engineering evaluation proves 4K RAM based 21MX minicomputer series is already 50% more reliable than our previous "core" type computers. The MX/65 package delivers rugged performance in almost every environment, permitting stable operation under extremes of temperature, motion and humidity.

• Average access time for the 12962A Disc Subsystem is a fast 25 msec. Transfer rate is 937 kilobytes per second.

• 15,000,000 byte disc storage capacity is expandable to 120,000,000 bytes.

• Because Hewlett-Packard makes its own disc drive, the MX/65 offers you a double bonus: The whole package is discountable. And, because it's a package, your integration costs are reduced.

• Optional new RTE-III operating system gives you multi-lingual, real-time, operating capability.

• Compare, then call or write for full specifications plus your free copy of our latest "Engineering Evaluation Report."

PRODUCT	32K WORDS WITH	AVERAGE ACCESS TIME	TRANSFER RATE	QTY 50 PRICE
HEWLETT-PACKARD MX/65 DISComputer	15 Mbyte disc storage Parity, EAU, and Floating Point standard	25 msec	937K bytes	$17,655*
HEWLETT-PACKARD MX/55 DISComputer	5 Mbyte disc storage Parity, EAU, and Floating Point standard	30 msec	312K bytes	$15,015*
PDP 11/35	5 Mbyte disc storage Parity standard, no EAU or Floating Point	50 msec	180K bytes	$21,945*
NOVA 830	5 Mbyte disc storage Parity (not available) no EAU or Floating Point	70 msec	195K bytes	$20,904*

22530B

***Domestic USA OEM prices quantity 50.**

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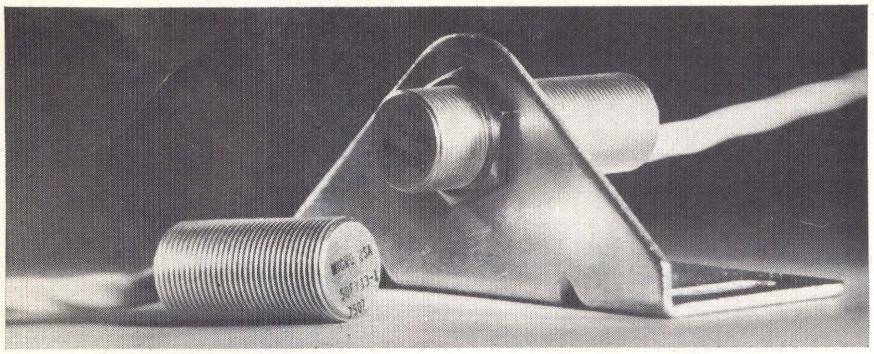
CIRCLE 16 ON INQUIRY CARD



Hall-effect sensors incorporated in Micro Switch's 50FY series proximity switches allow entire unit to be self-contained in 1"-long package. Sensors operate at 25,000 cycles/s, are oiltight, and interface directly with logic level circuitry

duced when any metal surface enters the switching field cause a change in switch output.

Self-contained sensors in the series range from ½ to 3" in diameter; sensing distances increase with size and range from 0.118 to 1.26". The sensors operate in slide-by or head-on mode. All except the 3" model are available with shielding, which, in general, cuts the sensing range in half, but allows the units to be mounted flush with a metal surface. Many of the devices are available with an LED indicator to signal when actuation and release occur.

Operating temperature range is −30 to 85°C. Input voltages range from 8.5 to 30 V and output is either 20 or 170 mA.

50FY Hall-effect proximity devices sense only ferrous metals, operating in head-on or slide-by mode. The magnet-actuated integrated circuit chip used in the sensors allows 1½ x 1" size and provides high reliability and quick response. The 50FY functions at 25,000 operations/s in the −40 to 85°C temperature range. The sensors accept a 7- to 16-Vdc supply voltage and provide either current-sinking or sourcing outputs that range from 20 to 200 mA.

Functioning at speeds up to 100,000 times/s, the solid-state AV vane sensor, a Hall-effect device, can be used as shaft-position encoding sensor, limit switch, or cam-operated programming switch. The sensor is actuated by passage of a ferrous vane through a gap between magnet and Hall sensor. The vane prevents magnetic flux from reaching the integrated circuit chip, causing a digital output. When the space between the vane's ferrous blades appears in the switch gap, the output returns to zero. Both linear and rotary vanes operate equally well.

The vane sensor interfaces directly with most electronic circuitry, providing a 20-mA output to eliminate need for an amplifier in most applications. There is no minimum speed of operation; and both sinking and sourcing outputs are available.

Circle 153 on Inquiry Card

Intelligent Video Terminal Base for Cost-Effective Data Exchange System

To provide cost-effective processing in applications involving high volume, user-interactive transactions, the DXS™ Data Exchange System uses model 960B minicomputers for transaction processing and disc file management, terminal communications, and optional host interface. Introduced by the Digital Systems Div of Texas Instruments Inc, 12203 Southwest Freeway, Houston, TX 77001, the system features a 914A video terminal which enables stand-alone transaction processing or communication to 360/370 host systems.

The 914A incorporates a microprocessor with 8 kilobytes of memory for intelligent data entry and inquiry response to DXS or host 360/370 data files with full 3270/2260 emulation. The 1920-char screen provides programmable field formats, protected and nonprotected fields, and a range of field-editing functions, which minimize data entry errors and reduce data to be transmitted.

Two basic configurations are available: the -20 with up to four 2.2-megabyte cartridge disc storage units, and the -40 with up to four 100-megabyte disc drives. Each system supports up to 64 terminals on a combination of up to 11 local/remote communication lines at 1200- to 9600-baud speeds. System expansion capabilities include support for up to 256 terminals on up to 44 local/remote lines.

System software includes TINDX, an indexed-access disc file management method, which enables virtually any disc record to be searched and located using no more than two disc accesses. Efficient utilities build, sort, and update files through programs written in high level transaction statements. DXS/ST, the high level transaction programming language, allows relatively untrained programmers to write DXS teleprocessing applications programs using transaction statements similar to COBOL.

Peripherals supporting the system include 300- and 600-line/min. printers, KSR console teleprinters, 800- and 1600-bit/in., 9-track tape drives, card readers, and disc drive units. System prices range from $66,000 to $250,000.

Circle 154 on Inquiry Card

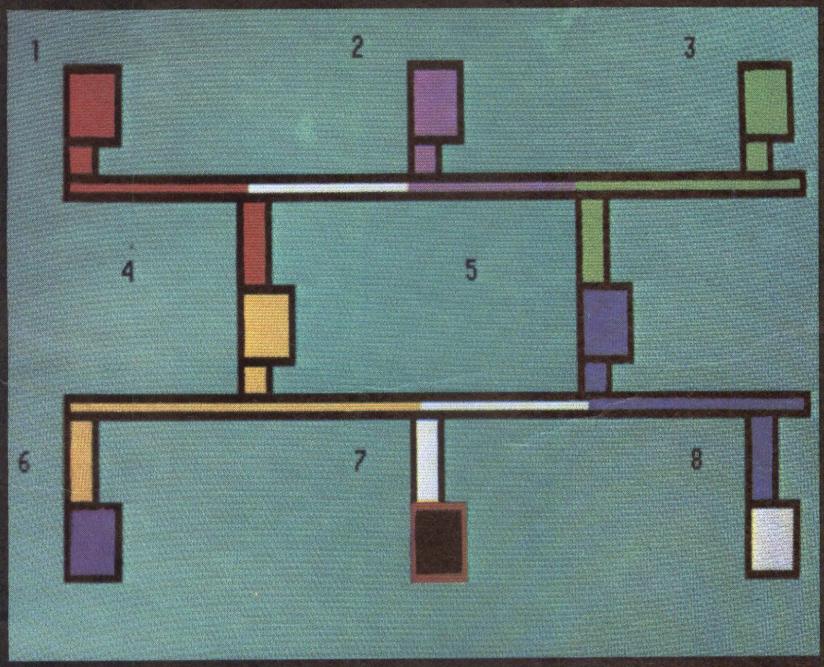
Hand-Held Calculators Provide Special Functions at Lower Prices

Using straightforward algebraic logic, the FX-15, a pocket-sized scientific calculator, allows direct keying of angles in degrees, minutes, and seconds, while the CP-801C Pocket-Mini, comparable in size to a cigarette pack, features automatic constant for addition, subtraction, multiplication, and division, and offers a special percent key for calculating discounts. Developed by Casio, Inc, Consumer Products Div, One World Trade Center, New York, NY 10048, the units derive performance from technological advances and offer lower prices gained from refined production methods.

For student, scientist, or engineer, the FX-15 performs sexagesimal conversion; sine, cosine, and tangent; common and natural logarithms; exponents; square roots; reciprocals; raising to a power; squaring; and calculations involving pi. It incorporates a 4-key memory for storage of intermediate results. The unit dis-

The quality color display that won't put you in the red.

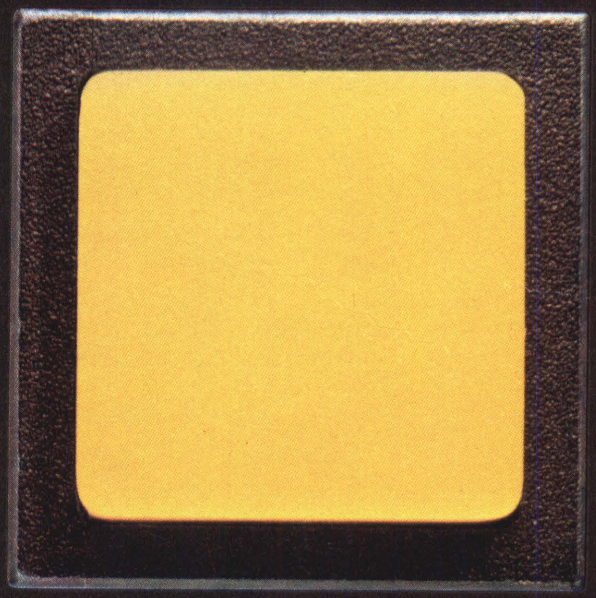
You're looking at a display generated by the ADDS MRD 460. The rack-mountable color display system that makes it easier for the process control industry to get the picture—two ways: First, the high quality of the system itself. Standard features include: eight vibrant colors for both characters and backgrounds. 24 lines with 80 characters per line to drive a standard TV monitor. Patented graphics, blinking, protected formatting and a parallel interface. And with the serial interface and keyboard options, the 460 can be used as a Teletype® compatible terminal. Secondly, consider cost. ADDS quality doesn't come cheap. But the MRD 460 is priced at only $3800. All things considered, that's very high quality at a very low cost. But then again, that's ADDS. Applied Digital Data Systems, 100 Marcus Blvd., Hauppauge, New York 11787 (516) 231-5400.



ADDS

CIRCLE 17 ON INQUIRY CARD

Developing this new pushbutton was a little like coming up with a Ferrari that gets 32 mpg, holds 12 people and costs less than a Pinto.

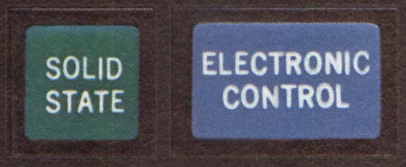


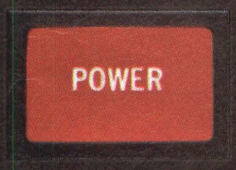
Until now, there have been some good-looking lighted pushbuttons and indicators.

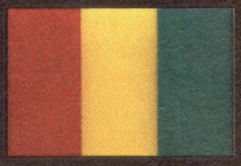
And there have been others with varied electrical capabilities. But there's never been a line that gave you harmonious panel design, electrical flexibility, and low cost. All at the same time. Until now.

Introducing the MICRO SWITCH Advanced Manual Line—AML.

The most sophisticated line of pushbuttons and indicators ever designed. And you can see a few of the reasons why right here. The AML button height, bezel size and visual compatability of the square and rectangular sizes "harmonizes" your panel. To give you a panel with a clean, good-looking geometric face. And a panel with increased efficiency, because it doesn't distract. The low-profile square and rectangular buttons are available in five colors: white, red, yellow, green, and blue. Display capabilities include split screen, hidden color, and a unique three segment lens cap indicator. Illumination can be transmitted or projected. But what you can't see here is what helps to make these the most advanced line of lighted pushbuttons and indicators available: their extreme electrical flexibility.







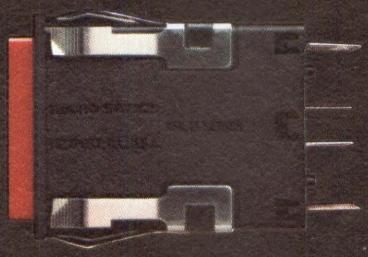
Solid state operates at 5V or 6-16V with a built-in regulator, sink (TTL) and source (CMOS).

Electronic control is capable of handling low energy circuits and has a maximum rating of 3 amps, 120 VAC, with single or double pole double throw.

And power control, DPST, with a rating of 10 amps at 120 VAC.

The AML has snap-in mounting from the front of panel and can also be subpanel mounted. There's a choice of individual or strip mounting.

All devices are the same shallow depth behind the panel to provide a unique single level termination system. The result is ease of wiring and neat appearance.



There are 5 types of terminals available: solder, quick-connect, wire-wrap, push-on or p.c. board mount. Relamping is accomplished from the front of the panel. And it's done without a tool. With a choice of lamps including a T-1¾ wedge base lamp, neon and LED. To provide international acceptance, every AML device has been designed to comply with essential IEC, CEE24, UL and CSA standards.

For more information on the AML, call your nearest MICRO SWITCH Branch Office. Or write for our literature.

What you'll see is a line of lighted pushbuttons and indicators that give you a completely harmonious panel design in the front.

And the utmost in electrical flexibility behind the panel.

All products shown on this page are actual size.

MICRO SWITCH

FREEPORT, ILLINOIS 61032

A DIVISION OF HONEYWELL

Reader Service Card 18 for data; 19 for salesman call

MICRO SWITCH products are available worldwide through Honeywell International.

plays results in scientific notation, with exponents up to plus/minus 40 digits, on a bright green, 8-digit readout. Forty-three hours of continuous use are provided by four penlight alkaline batteries; an ac adapter is optional. The FX-15 will retail for $64.95; the Pocket-Mini, for $19.95, including batteries and carrying case.
Circle 155 on Inquiry Card

Plug-In Module Makes Digital Panel Meters ASCII Compatible

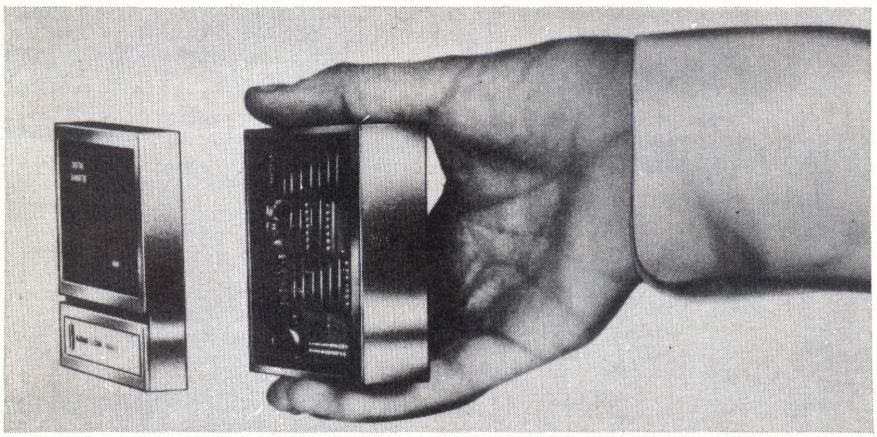
Although BCD data outputs on digital panel instruments have permitted them to be interfaced to printers and computers, they have been limited in use because of the expenses of multi-conductor cabling, distance restrictions, and costs associated with switching data from more than one meter into a single system. Overcoming these limitations, the ASCII Bustle, a plug-in module developed by Nationwide Electronic Systems, Inc, 1536 Brandy Pkwy, Streamwood, IL 60103, makes any of the company's Slimline digital panel instruments compatible in serial ASCII, for direct transfer of data from the meter to printer, CRT, or computer.

The Bustle interfaces to any device that operates in serial ASCII through a single pair of wires or two separate pairs, looped from one bustle to the next, and from there to the terminal. Up to 100 panel instruments can be connected via a single pair of wires. Bustles can be located up to two miles from the terminal without requiring line conditioning when using current-loop interface; using a modem or specially amplified line virtually eliminates any distance restrictions. Any instrument can be interrogated manually from a keyboard or automatically from a computer by transmitting its unique ID number as set using built-in rotary switches.

The device can be triggered to send its identification number and meter reading and an optional programmed message. One method uses a single trigger input on each unit; another, uses two switches on each unit to set a 2-digit ID number. The device monitors the ASCII line, and when it receives a number sign (#) followed immediately by its ID number, it automatically sends data.

Models having programmed message capability can be programmed to self-scan, by having each unit send a number sign plus the 2-digit ID number of the next unit in line as the last three digits of the programmed message. In this way, the system can be programmed to scan all units and stop, or to continuously scan the loop.

Input/output is 10- or 11-bit ASCII (field-selectable) at from 110 to 9600 baud. DTL/TTL, 20-mA, 60-mA, and EIA RS-232-C interfaces are available. Dimensions of the unit are 4.5 x 3.5 x 0.875"; power requirements are 5 Vdc at 500 mA, and ±12 Vdc at 20 mA. Prices range from $195 to $265.
Circle 156 on Inquiry Card



Plugging on the back of any of Nationwide Electronics' Slimline digital panel instruments, the ASCII Bustle provides for ASCII-compatible transfer of data to printer, CRT, or computer

Key-to-Disc System Ups Capability 10% With Fore/Background Editing

Significantly reducing data-verification operations and eliminating the complicated programming necessary to perform editing functions, the System 3300, a large capacity data entry system, consists of a CPU with built-in editing microprocessors, 10-megabyte disc storage unit, 7- and 9-track magnetic tape drives, and up to 16 operator stations. The system is claimed to reduce the use of central processors by 80% in editing data received from data entry devices and to eliminate 50% of the keystrokes normally required to create data entry records from source documents.

Developed by Inforex, Inc, 21 North Ave, Burlington, MA 01803, the system incorporates a foreground/background editing feature that permits operators to edit data as they are keyed, or to key on a non-stop basis for later automatic editing. In foreground mode, the system interrupts operators as errors are detected, enabling them to insert correct information from the source documents. In background mode, operators enter data continuously without regard to error conditions. The system then automatically performs the editing function after the batch has been completed, automatically flagging all error conditions.

Automatic data insertion features further reduce keystroking and error rates. In a typical application, as much as 75% of the actual data needed for computer processing and production of final totaled invoices is stored in or computed by the system. 255 tables provide regularly used information, allowing the operator to enter brief key information and obtain all related information automatically. These data are then inserted in appropriate fields within the record.

Use of the "parameter rule" technique allows data entry personnel to define and create applications programs. Up to 750 different format and reformat sets, each with 15 levels of control, can be stored for instant recall, eliminating substantial setup time on new jobs. □
Circle 157 on Inquiry Card

The article on Mostek's electronic checkbook (*Computer Design*, June 1975, p 22) erroneously states that "standby current must be held under 100 A to prevent reduction in battery life . . ." This should read "must be held under 100 μA . . ." We regret the error.

THERMAL PRINTER AND POWER SOURCE

NOW, TOGETHER FROM NCR.

Now you can offer your customers a "receive only" Thermal Printer that contains its own power source. No extra box. No extra cable. Just one handsome cabinet.

With the new EM-T33 (parallel) or the EM-T44 (serial) unit from NCR you can provide distinct advantages over other terminals.

Quiet . . . almost completely electronic, the only sound comes from the movement of paper and a non-impact printing head.

Fast . . . Up to 30 characters per second is the printing speed—2 to 3 times faster than terminals with conventional impact printers.

Accurate . . . Hard copies of every message means no slips of memory; no mistakes in transcribing which are possible with some units.

Compact . . . One single, light, easy-to-carry unit contains both the thermal printer and the power source in a single attractive cabinet.

Here's a way for you to increase the benefits you offer in the communications system you sell . . . and increase your sales and profits by doing so.

For more information on this and other components for your communication systems, please contact us today.

NCR

Data Entry Division

Director of OEM Marketing, Babcock Hall
Terrace Hill, Ithaca, N.Y. 14850 607-273-5310

CIRCLE 20 ON INQUIRY CARD

Presenting the OEM branch of Digital.

It's a complete family of computer tools. And it's growing every day.

Nine CPU's—from our smallest, the LSI-11, to our biggest and newest, the PDP-11/70—with virtually every meaningful price/performance choice available in between. Choose one of them, and a whole world of possibilities opens up.

Proven operating systems offer real time, time-sharing, and batch capabilities, so you can choose the system that exactly fits your needs. Also you can hook up any of 60 different peripherals including your choice of 4 different disc drives, 5 terminals, 3 tape systems, 6 line printers—among a host of others.

What's more, you can join a special family called DECUS (Digital Equipment Corporation Users' Society) and instantly put at your disposal a whole library comprised of thousands of applications software packages.

And then you can start to plan your future. Your next new product, your next PDP-11 or PDP-8 computer. And to help you along the way, our family includes 2400 field service experts ready to lend a hand when and where you need it. And that means everything from operator training programs that get you quickly up to speed, to the new OEM Referral Program that helps you market your product.

When an OEM chooses a computer company, he makes a big decision with important long-term consequences. The OEM branch of Digital gives you a computer family you'll never outgrow.

To find out more, call or write Digital Equipment Corporation, Maynard, Massachusetts 01754. (617) 897-5111. European headquarters: 81 route de l'Aire, 1211 Geneva 26. Tel: 42 79 50. Digital Equipment of Canada, Ltd.

digital

CIRCLE 21 ON INQUIRY CARD

NEWS BRIEFS

A PROGRAMMED LEARNING COURSE ON MICROCOMPUTERS, based on concepts, uses, design criteria, and implementation of microprocessor-based systems, includes six comprehensive volumes on technology, an applications handbook, and a variety of programming pads and simplified design aids. Priced at $124.50, the course provides over 1700 self-tests, hundreds of illustrations, and details on four commercially available microcomputers (Intel 4004, 4040, 8008, and 8080). Iasis, Inc, 770 Welch Rd, Suite 154, Palo Alto, CA 94304 will deliver the course to U. S. and non-U. S. customers within 15 days and six weeks ARO, respectively. Pay by check or money order in U. S. dollars; orders returned within 15 days will be fully refunded.

A MAINTENANCE PROGRAM FOR OEM CUSTOMERS of Decision Data Computer Corp, Horsham, Pa is enabling them to obtain field engineering service—throughout the U. S. and Canada—on data processing equipment purchased from the company and resold or leased by the OEM to end-users. Available on a contract basis covering both technical service and parts, the program is intended to offer the systems manufacturer a low cost method of implementing card input/output and data entry on new systems as well as service on existing installations.

According to the company, OEM systems marketing potential in North America is frequently limited by a lack of trained field engineers and the high cost of stocking spare parts. "With the industry's growing need for increased-capability data entry equipment plus 96- and 80-col card peripherals, the availability of complete field engineering and parts support can make a significant difference to systems suppliers that compete with IBM."

EXPERIMENTAL TELEX RATE REDUCTIONS for overseas service, filed with the Federal Communications Commission by TRT Telecommunications Corp, Washington, DC, went into effect for six months, beginning May 1. A decrease of 22% on calls from the U. S. to the United Kingdom and the Federal Republic of Germany applies to nights and weekends.

According to the company, some 40,000 organizations in the U. S. presently utilize Telex for overseas communications, having spent more than $136 million in 1974. The TRT filing is the first submitted by a U. S. international communications carrier for "off peak" traffic hours and the first since 1970 for a reduction in rates to Europe.

AN UPDATED POWER SUPPLY STUDY revising projected market sizes and growth rates from conclusions released in 1973 has been published, with forecasts through 1980 for both captive and noncaptive segments of eight major power supply markets. One significant finding is that, due to the availability of new technology such as components for use in switching power supplies, 1974 noncaptive supplier sales exceeded its anticipated amount by $60 million, and is expected to reach $200 million by 1980.

By that year, the total U. S. power supply market is predicted to reach $3.753 billion—almost double the 1974 figure, with data processing the largest single segment. Ac/dc constant voltage supplies will remain the largest selling type, although ac/dc uninterruptible power supplies will exhibit the fastest growth rate.

The updated study is priced at $6000. For information, write on company letterhead to Darling & Alsobrook, 1801 Ave of the Stars, #1101, Los Angeles, CA 90067.

7-/9-CHANNEL DIGITAL MAGNETIC TAPE HEADS can now be refurbished through a service announced by Saki Magnetics, Inc to be performed at its Santa Monica, Calif plant. Through re-contouring to remove tape wear patterns, and reworking tape guides and cleaners, the heads are re-manufactured to meet original specifications, then re-set for correct tape wrap and minimum skew.

The service also includes repair of broken wires in the assembly as well as within the head itself. If repairs are not feasible, the entire head stack can be replaced with an equivalent Saki assembly.

A TELEGRAPH/DIGITAL DATA TRANSMISSION SYSTEM launched in 1973 by Philips Telecommunication Systems, Hilversum, The Netherlands has evidently served as a model to two CCITT (Comite Consultatif Internationale) study groups. Significance of recommendations recently made by them is said to be due to the acceptance of the 3TR 1500, which is compatible on an international level with existing analog frequency-division multiplexer (FDM) networks and pulse-code modulation (PCM) circuits. According to Philips, although the recommendations do not extend beyond transparent telegraph channels of up to 300 baud, they represent a breakthrough of digital transmission into presently available analog networks, and provide promising opportunities for long-haul PCM routes.

A COMPUTER PROGRAM MAINTENANCE TOOL designed to repeatedly save hours and even days of programmer time is now being offered to individual programmers with a double-money-back guarantee. Claimed to be the most powerful system available to help create and modify IBM 360 and 370 computer programs, the DOS-sequential Text Maintenance System (TXTM) consists of several phases which must be cataloged in the core image library. It requires 45K words of memory, is self-relocatable, and operates with 2311, 2314, 3330, or 3340 discs.

TXTM rents for $150/year/programmer. He pays $25 for the first month; if, after meeting the following criteria he rejects it, he receives $50 once the program is returned. He must have placed at least 2000 source statements on a master file, updated that file at least five times, and used some TXTM features. To order the one-month trial, send $25 to Joseph Sider and Associates, 15713 Varden St, Encino, CA 91316.

RECENT PRICE CHANGES include a 50% reduction on memory options for models 21, 31, 31/10, 31/53, and E31 programmable calculators from Tektronix, Inc, Beaverton, Ore . . . Monroe, The Calculator Company, Orange, NJ has cut its Beta 326/392 microcomputer from $1395 to $895

(Continued on p 32)

SAVE TIME

...ways Belden can help you get more profit from every minute.

The right cable saves callback headaches. Belden's broad-line capability can help you meet toughest environmental conditions and application needs.

The handier cable is to use the faster your job gets done. Less foot cost! Ask about our new UNREEL™ packaging concept. A unique cable dispensing system that eliminates snarls, backlash and tangle problems. Pulls easily yet stops instantly when pulling stops. Eliminates reel disposal headaches.

The faster cable is to obtain, the less jobsite delays you'll have. There's a Belden electronic cable Distributor always close at hand. We back his inventory with a big one of our own. This one source of supply saves ordering time, and money.

Quick problem solving capabilities save time, too. Belden's electronic cable Reference Guide contains more standard items than any other. Wire, cable and cord answers that make selection easier.

We have cable specialists, and engineering help available you can call upon for any unusual problems that have to be solved.

And "hot-line" service for problem solving, too. Call 317-966-6681 for engineering assistance on any cable problem that needs immediate attention. You'll get the type of response you need to help protect your bottom line profitability.

Whatever your need in wire, cable cord, let Belden help you save valuable time: Write: Belden Corporation, Electronic Division, P.O. Box 1327, Richmond, Ind. 47374.

BELDEN

...new ideas for moving electrical energy

81-5

CIRCLE 22 ON INQUIRY CARD

NEWS BRIEFS

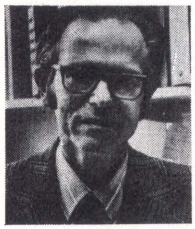
. . . According to Science Accessories, Corp, Southport, Conn, its Graf/Pen sonic digitizer has been raised from $2400 to $2700, while interfaces have been reduced (eg, with the DEC PDP-11 from $1500 to $450, and with a paper-tape punch, from $1025 to $600) . . . DIP relays from Struthers-Dunn, Inc, Pitman, NJ have been dropped in price by 25%; in 500-piece lots, they are available for $1 each . . . Computer Transceiver Systems, Inc, Paramus, NJ has announced reductions of up to 20% on its Execuport line of portable computer terminals.

OEM COMPUTER PRICES, due to the lower cost of metal-oxide semiconductor random-access memories (MOS RAMs), have been sharply lowered—into the microcomputer range—by Computer Automation, Inc, Irvine, Calif. The Naked Milli™—a millicomputer mounted on a 7 x 15-in. half-board—is now available for $395/$489 for a processor with 256/1000 words of 16-bit RAM, in 100-piece quantities. Previously, its lowest price was $519 (512-word memory). Additional memory modules are also being produced: 4K- and 8K-word prices (100-quantity) are $616 and $914, respectively.

RECENT DEVELOPMENTS IN OPTICAL/DIGITAL SYSTEMS were examined at the 1975 International Optical Computing Conference held this spring in Washington, DC. Sponsored by the IEEE Computer Society and the Naval Underwater Systems Center, the Conference emphasized optical computing systems and the joint role of optical and digital processing. Consensus of a panel discussion on optical vs digital computing was that techniques of each are suited to their own specialized tasks; the state-of-the-art favors digital methods for general-purpose computations, while optical methods have their place in special processors performing such applications as pattern recognition. Panelists and audience agreed that at the present stage of technology, they prefer the hybrid optical/digital approach.

PEOPLE

DR MORTON M. ASTRAHAN of International Business Machines Corp's San Jose (Calif) Research Laboratory, for his key role in the formation and growth of the American Federation of Information Processing Societies, Inc, was presented the AFIPS Distinguished Service Award at the National Computer Conference in Anaheim, Calif. Dr Astrahan helped establish the first permanent National Joint Computer Conference Committee (1953) and, since 1969, has served on the JCC Committee (now the National Computer Conference Committee). He was organizer and initial chairman (1952-53) of the Institute of Radio Engineers Professional Group on Electronic Computers (presently the IEEE Computer Society).



With a PhD degree in Electrical Engineering from Northwestern University, Dr Astrahan is a member of the IBM Quarter Century Club. In addition to playing a major role in development of the IBM 701 and the SAGE Air Defense System, he carried out projects involving an associative memory built around a rotating drum and development of the concept for program interrupt, allowing input/output operations and processing to occur simultaneously.

Roger Salava has been appointed chief engineer of Compugraphic Corp, Wilmington, Mass . . . **Thomas J. Connors** has become president of Mirco, Inc, Phoenix, Ariz . . . The Institute of Electrical and Electronics Engineers (IEEE) has honored, for distinguished service to its Solid State Circuits Council, **Murlan S. Corrington** of RCA Corp, Camden, NJ . . . ITT Cannon Electric, Santa Ana, Calif has elected **James H. Anderson** president, and has named **Robert J. Trivison** vice president/director of operations and **Harvey S. Left** general manager-micro products.

At ADL Systems, Inc, sub of Arthur D. Little, Inc, Burlington, Mass, **W. William Acker** is now exec vice president and board member . . . **T. David McFarland** has been appointed acting exec director of the Data Processing Management Association (DPMA), Park Ridge, Ill; **Dr Willis H. Ware,** The Rand Corp, Santa Monica, Calif and **Dr Donald L. Bitzer,** University of Illinois, Urbana have been selected as co-recipients of the DPMA's 1975 Man-of-the-Year award.

New director-OEM marketing for Diablo Systems, Inc, Hayward, Calif is **Charles W. Ryle; Mark L. Siegel** has become vice president-Memory Products Div . . . **Richard S. Rager, Jr** has rejoined Gould, Inc, Newton, Mass as manager of software-Graphic Systems Div . . . **Matt Faletti** is now manager-application engineering at Ampex Corp, Computer Products Div, Redwood City, Calif . . . Election of **Theodore W. Ziehe** as a vice president-information systems has been revealed by MRI Systems Corp, Austin, Tex.

Rockwell International Corp has named **Don A. Mitchell** president of its Microelectronics Group, Anaheim, Calif . . . **Dr William Weksel** has been elected president and board chairman of Information Displays, Inc, Mount Kisco, NY . . . At Siemens Corp, Components Group, Scottsdale, Ariz, the new post of director-research/development has been filled by **Wolfgang Kayser** . . . Computer Automation, Inc, Irvine, Calif has appointed **David Stein** director of marketing.

At Burroughs Corp, Detroit, Mich, **Eugene L. Merlino, Jr** has become director of manufacturing-peripheral products group . . . **Neal B. Dowling** is now marketing manager-thick film circuit products at Centralab Electronics Div, Globe-Union Inc, Milwaukee, Wis . . . Election of **Daniel J. Dooley** to vice president/director of engineering for Precision Monolithics, Inc, Santa Clara, Calif has been disclosed . . . **Harold R. Buchanan** has joined Interdata, Inc, Oceanport, NJ as data communications product line manager.

Promoted by Rapidata, Inc, Fairfield, NJ were **Glenn F. Schafer,** manager-programming services, **Curt Huff,** assistant vice president/operations manager, and **Clark D. Karcher,** vice president-marketing; the company has also selected **Ray W. Harri-**

Benchmark: **standard against which other microprocessing approaches must be measured.**

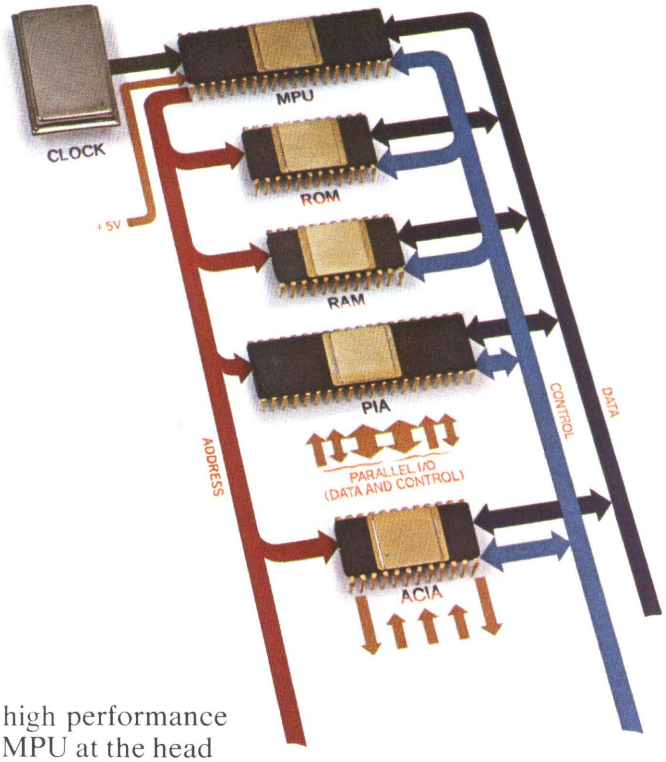
Family: **total of the compatible, synergistic device and support pieces comprising the whole of microprocessor use.**

M6800: **benchmark family for microcomputer systems.**

Everything for your system: All in the M6800 Family

M6800 concept: Optimum system design

No question, the MC6800 microprocessor is head of the family. It is outstanding even as a stand alone part, as demonstrated by the high marks it scores on nearly everybody's benchmark studies. But, from the beginning at Motorola, the end system was our main concern, so the MC6800 is a



high performance MPU at the head of a modular LSI device series, totally bus compatible and fully compatible with each other.

The concept encourages systems of minimum parts, yet allows plenty of design flexibility. And, I/O is super simple with the intelligent programmable logic interface units which make the M6800 Family unique. Finally, for those who require it, the entire series of M6800 LSI devices is already second sourced.

Several MPU clocks are offered by Motorola Inc., Component Products Dept., 2553 N. Edgington, Franklin Pk., IL 60131. MC6870A is a minimum system version, MC6870B has added features, and the MC6871A is for maximum complexity systems.

Motorola's popular MEK6800D-1 introductory special design evaluation kit continues for a limited time. Contact your authorized Motorola distributor or Motorola sales office.

M6800 support: Speeds the design job, makes it easier

Hardware design tools

MEC6800 Evaluation Module. Here's a complete board, all the M6800 LSI devices plugged in so you can evaluate the parts in a basic minimum system. Even connect it to a peripheral and run programs.

M68SDT EXORciser.* The systems development tool, built with M6800 LSI devices and

pre-engineered with modular options for emulation of users' microcomputer system applications. Hardware design and development costs are drastically reduced. Debugs both system hardware and system software.

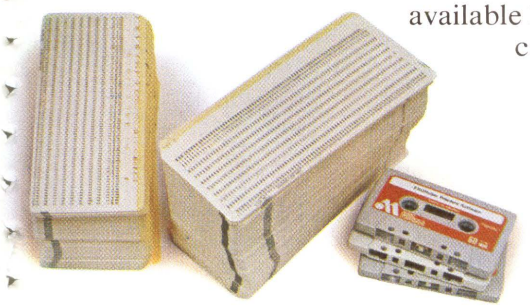
Software choices

Commercial timesharing. M6800 software is presently available on two commercial timesharing services — G.E. and United Computing Service. Others will be added as justified by demand.

MOTOROLA M6800

EXORciser package. A resident software package is available for the EXORciser system development tool.

Host Computer Cross Assembler and Simulators. Three excellent packages are available here in either cards or tapes.



a. Standard package. The type normally supplied by vendors. We send the software; customer sets it up. No frills.

b. Extended Capability package. Includes M6800 Programming Manual. Customer still sets it up.

c. Deluxe package. Complete capability. Motorola does the set up on the customer's premises.

We wrote the book

M6800 Programming Manual. Probably the most vitally utilitarian of our growing M6800 document library.

M6800 Applications Manual. It was here that

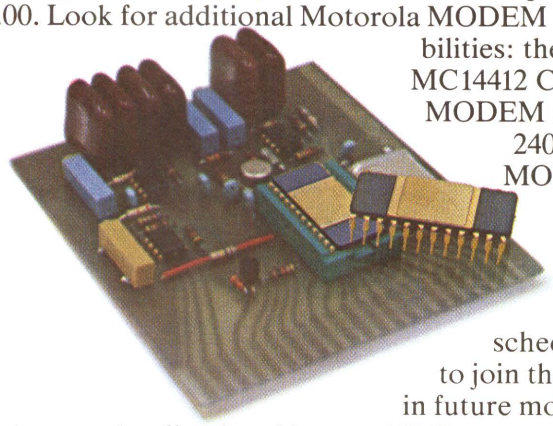
Motorola really wrote the book; and, it's on its way to being the basic microprocessor textbook for the industry.

Low speed digital MODEM: New freedom for terminal designers

The MC6860 Low-Speed Digital MODEM is one of the communications features which makes the M6800 Family unique.

It's also freedom from MODEM slavery for terminal designers who could be building small, simple, inexpensive MODEMs into their own equipment.

The MC6860 is a Full Duplex Answer and Originate MODEM with Auto Answer and Auto Disconnect capability. It is Bell compatible and can operate on a single +5V supply. The new 100-999 price is $24.00. Look for additional Motorola MODEM capabilities: the new MC14412 CMOS MODEM and a 2400 bps MODEM



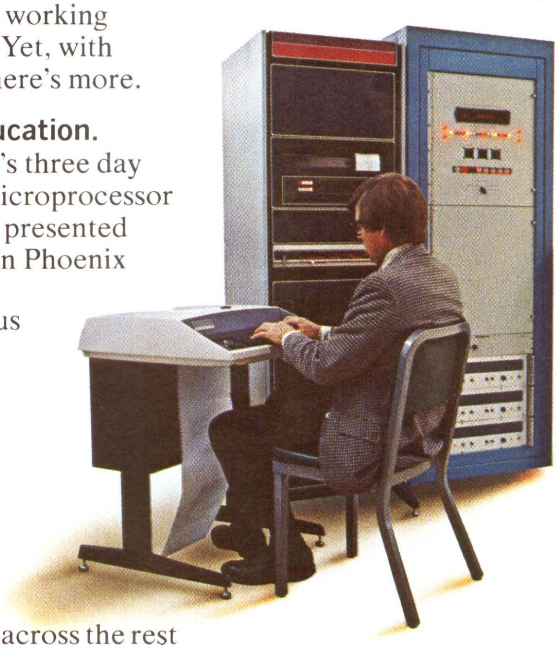
scheduled to join the mix in future months.

A new Application Note, AN747, shows how easy it is to build a space-saving MODEM right into your terminal. It even gives filter design guidelines.

M6800: It's a big family

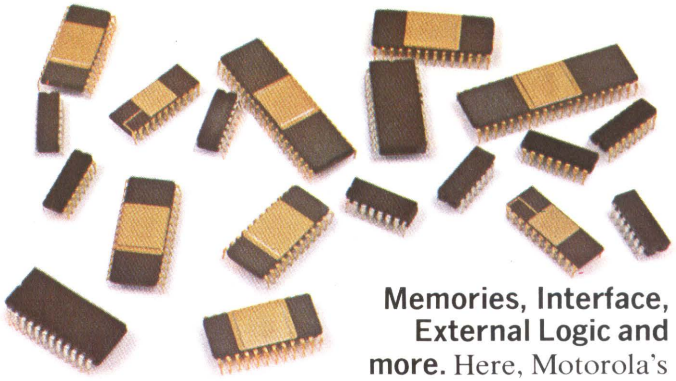
The M6800 was designed from the very beginning to employ the synergistic effect of all these family functions working together. Yet, with all this, there's more.

MPU education. Motorola's three day M6800 Microprocessor Course is presented monthly in Phoenix and on a continuous



schedule across the rest of the nation. No bit of fluff, the course is a complete education in designing with microprocessors, including coverage of hardware and software as well. Hundreds of companies have elected to have their people trained in this course already; and, its popularity is still climbing. Call Ron Bishop (602) 962-2345, for information.

MOTOROLA M6800



Memories, Interface, External Logic and more. Here, Motorola's capability as a broad line supplier contributes. A varied and growing assortment of ROMs and RAMs add options to the basic family memories. There's plenty of logic beyond the MPU-based portion of the system, CMOS for instance, and Motorola's McMOS fits in with parts like the new MC14411 Bit-Rate Generator. Bipolar Linear lines supply MPU and memory interface parts. And, out of Motorola's immense background in silicon discrete devices comes the new MPU clock buffer, the MPQ6842.

Nothing like the M6800 Family

By now it should be clear that there's nothing like the M6800 Family for designing microprocessor-based systems; and, nothing like Motorola's synergistic total package approach to the whole job.

M6800: A growing family still

N-Channel Si Gate Memories

Third Quarter, '75			
MCM6811	1K x 1	Static RAM,	16-pin
MCM6814	4K x 1	Dynamic RAM,	16-pin
MCM6815A	4K x 1	Dynamic RAM,	22-pin
Fourth Quarter, '75			
MCM6812A	256 x 4	Static RAM,	16-pin
MCM6834	16K	Static ROM,	24-pin

Bus Peripherals —Logic

First Quarter, '76	
MC6862	2400 bps MODEM modulator
MC6852	Synchronous Serial Data Adapter
Second Quarter, '76	
MC6863	2400 bps MODEM demodulator
MC6840	Programmable Timer module

Two Phase Clocks

July '75
MC6870A
MC6870B
MC6871A

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MOTOROLA M6800
Benchmark family for microcomputer systems.

I'm very interested in more information on your M6800 Family. Please send me the following technical information:

- ☐ Please send me a copy of your colorful new M6800 Family brochure. I understand it covers the subject matter of this ad in greater detail, plus important related materials.
- ☐ M6800 Applications Manual (my $25.00 check or money order is enclosed)
- ☐ M6800 Programming Manual (my $10.00 check or money order is enclosed)
- ☐ M6800 Systems Reference and Data Sheets
- ☐ G.E. Timesharing brochure ☐ U.C.S. Timesharing brochure
- ☐ AN747-MODEM Application Note
- ☐ MCM6812A Memory Advance Information Sheet
- ☐ MCM6815 Memory Advance Information Sheet
- ☐ M6800 Software Technical Information ☐ EXORciser Information brochure
- ☐ M6800 Clock Application Note — R-29-3-10

Clock Data Sheets ☐ MC6870A ☐ MC6870B ☐ MC6871A

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NEWS BRIEFS

son, Jr as manager-remote access systems . . . New product marketing managers at Advanced Micro Devices are **Stuart Harris,** bipolar and **Steven Thompson,** linear . . . **Thomas O. Harbison** has been named president/chief operating officer of Genesis One Computer Corp, sub of Management Assistance Inc (MAI), New York City.

Elected vice president of Inforex, Inc, Burlington, Mass was **Joseph R. Leonardi,** who will also serve as acting director of engineering . . . Vice president-market development for Varian Data Machines, sub of Varian Associates, Irvine, Calif is now **Lawrence A. Lotito** . . . The newly created position of manager-product marketing at Harris Corp, Computer Systems Div, Fort Lauderdale, Fla has been filled by **Robert E. Kunkle.**

The appointment of **James J. Burns** as exec vice president has been announced by Burr-Brown Research Corp, Tucson, Ariz . . . GTE Information Systems Inc, a sub of General Telephone & Electronics Corp, Stamford, Conn has named **N. H. Hawkins** vice president/general manager-Data Communications Div . . . **Dr Sidney Fernbach,** Computation Dept head, Lawrence Livermore (Calif) Laboratory will serve as general chairman of COMPCON Spring 76, the 12th IEEE Computer Society International Conference, Feb 24-26.

ORGANIZATIONS

Honeywell, Minneapolis, Minn has announced that negotiations are continuing with respect to a possible merger of the general-purpose computer business of its French affiliate, **Compagnie Honeywell Bull,** with French-owned **Compagnie International pour l'Informatique (CII)** . . . **Mohawk Data Sciences Corp** plans to relocate its exec headquarters from Utica, NY to Morristown, NJ; remaining operations occupying the current headquarters building will be consolidated in company-owned facilities in Herkimer, NY.

Cutler-Hammer, Inc, Milwaukee, Wis has become majority owner of **Macrodata Corp,** Woodland Hills, Calif . . . **Information Terminals Corp,** Sunnyvale, Calif and **3M Co,** St. Paul, Minn have signed a nonexclusive licensing agreement granting ITC rights to manufacture the Scotch brand ¼-in. magnetic tape cartridge . . . **Broomall Industries, Inc,** Broomall, Pa has acquired the graphic plotter line of **Electronic Associates, Inc,** West Long Branch, NJ . . . **Weather Science, Inc,** Norman, Okla has merged with and changed its name to **Metrodata, Inc** (also of Norman).

Sorbus Inc, King of Prussia, Pa, sub of **Management Assistance Inc (MAI),** has opened a western-region marketing office at 2070 Business Center Dr, Irvine, CA 92264; the firm has also been selected by **Cincinnati Milacron Co,** Cincinnati, Ohio to maintain its CIP/2000 series minicomputers and related peripherals . . . To service the central U. S. and Canada, **Digital Development Corp** (San Diego, Calif) has opened an office at 1649 Marie Lane, Glenview, IL 60025.

Pinlites, a div of **Refac Technological Corp,** Fairfield, NJ is now a wholly owned sub of the corporation and has been renamed **Refac Electronics Corp;** operations of **Wild Rover Corp,** also owned by Refac Technological, have been combined with Refac Electronics . . . According to **Control Data Corp,** Minneapolis, Minn, first shipments of CYBER 175 computer systems—largest and most powerful in the 170 series—are scheduled for this month . . . **Courier Terminal Systems, Inc,** Phoenix, Ariz has sold its 15,000th unit.

Reorganization of its integrated circuit operations in Wilmington, Mass; Rochester, NY; and Santa Clara, Calif into the **Microcircuits Group** has been announced by **Analog Devices,** Norwood, Mass . . . **Fairchild Camera & Instrument Corp,** Mountain View, Calif has received, from the **Dept of Commerce,** the President's "E" Award for Excellence in Exporting . . . **Boeing Computer Services, Inc,** Dover, NJ has announced formation of **BCS-Manufacturing Services.**

Digital Equipment Corp, Maynard, Mass has delivered its first PDP-11/70 medium-scale computer system—to **Bell Telephone Laboratories,** Whippany, NJ; DEC's **Components Group,** Marlborough, Mass has delivered its first prototype LSI-11 microcomputer —to **General Radio Co,** West Concord, Mass . . . **Semi Processes International,** Santa Clara, Calif has unveiled a mobile wafer fabrication facility, available for sale in the form of a 10 x 45-ft trailer. □

Electron-Beam-Accessed Memory Has Potential for Cache Systems

A technology demonstration prototype memory system with 1.2-megabit capacity, undergoing field evaluation by Control Data Corp on a Star 1B computer, combines metal-oxide semiconductor (MOS) and electron-beam-access technologies. The system, made by Micro-Bit Corp of Lexington, Mass, is configured of nine parallel channels (tubes) of 128 kilobits each. Access to any page takes 16 μs.

Information on the electron-beam-accessed memory (EBAM) is stored in a pattern of charges in the oxide layer of an MOS (Fig. 1). Exposure of a small area of the oxide to a penetrating electron beam under positive gate bias depletes the underlying regions of the semiconductor and drives the surface of the p-type substrate into inversion. This results in the storage of a positive charge, corresponding to a "1;" absence of a charge represents a "0." The charge can be removed, returning the spot to a "0" state by exposing it to the electron beam under negative gate bias.

Reading of stored information is accomplished with the same beam as used for writing. When electrons penetrate the silicon to form a "1" they generate electron-hole pairs by direct excitation of electrons from the valence to the conduction band. The silicon becomes depleted of charge carriers and a high electric field is developed. If the electron beam enters a charged area during readout, the electron-hole pairs are separated by the field and register as current across the read resistor (shown in Fig. 1). Since no depletion region was generated for a "0," no electron-hole separation occurs and there is no readout signal.

Rather than attenuation which occurs in most memory media, the electronic processes occurring in the MOS target provide local amplification during both read and write. During write, about 10 times more charge is stored than is deposited by the electron beam; during read, the signal current is 100 to 300 times greater than the beam current. No noise is added to the fundamental shot noise which is present in the electron beam.

Current development involves EBAM tubes using single-channel optics. An actual memory tube of this type, storing 4.2 megabits, is shown in Fig. 2(a) and is illustrated schematically in Fig. 2(b). The maximum number of bits that can be stored and retrieved by this type of optics is limited principally by deflection electronics accuracy and stability and by deflector aberrations. Size of the MOS target is approximately 1 cm^2.

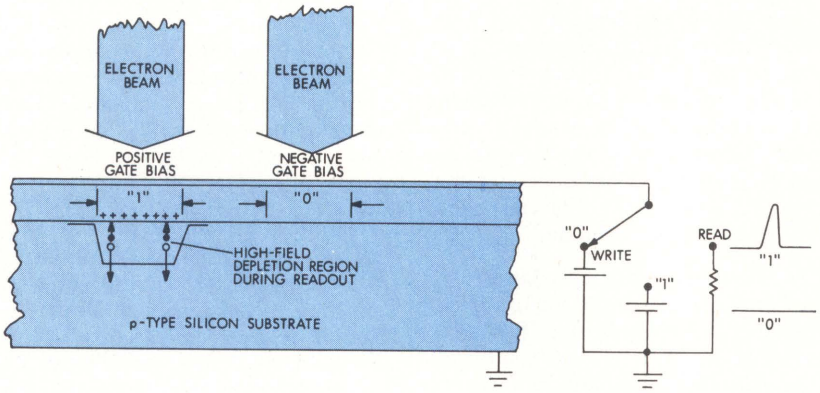

Fig. 1 Basic principle of electron-beam-accessed memory. An electron beam under positive gate bias drives the surface of the MOS substrate into inversion, causing storage of a positive charge (a "1"). Energy of the beam (10 kV) and thickness of gate and oxide permit the beam to penetrate several thousand angstroms into the silicon. By exposing this spot to an electron beam under negative bias, the positive charge is removed. Absence of charge is read as a "0". The same beam is used for reading as for writing

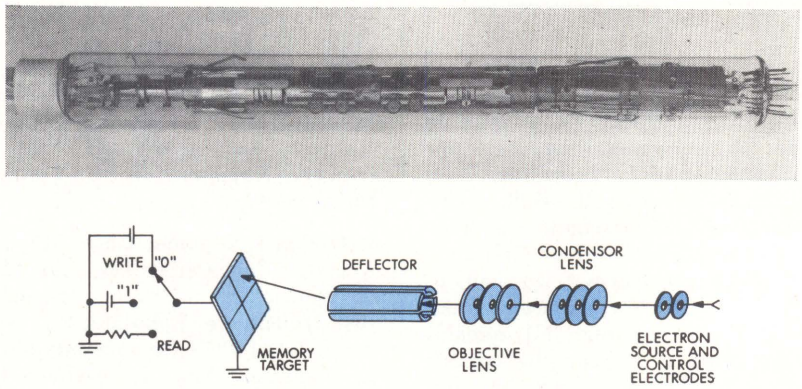

Fig. 2 An actual EBAM tube using single-channel optics (a) can store 4.2 megabits. Tube is shown schematically in (b). Deflection electronics accuracy limitations and deflector aberrations limit the storage capacity. The 30-nA beam is focused into a 2.5-μm spot on the memory target

YOU'VE JUST BEEN TOLD THE MICRO COMPUTER YOU SPECIFIED HAS BEEN DISCONTINUED.

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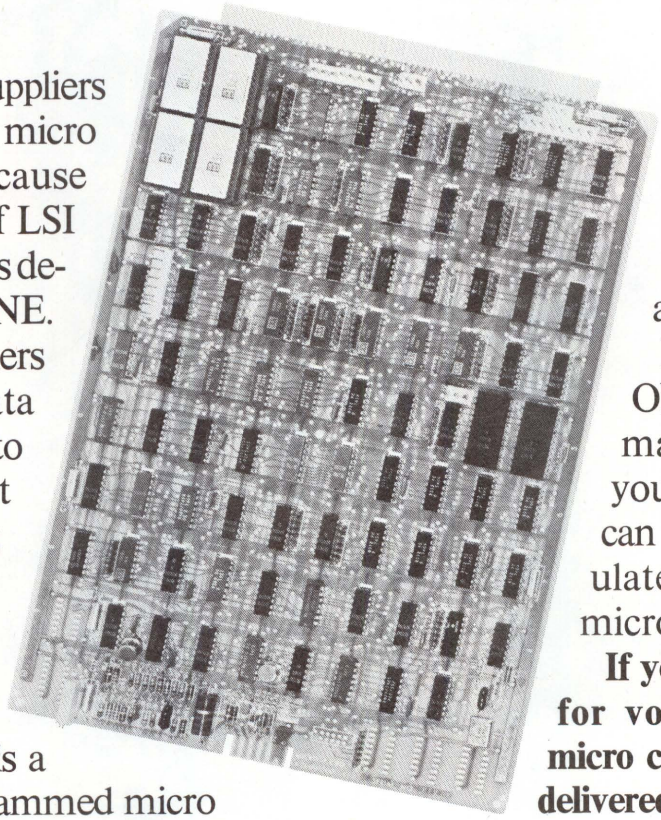

While other OEM suppliers are discontinuing their micro computer models because of the unavailability of LSI CPU chips, Microdata is delivering the MICRO®-ONE.

Smart system designers will use the Microdata computer-on-a-board to open up new market areas while lowering component and assembly costs and increasing profit margins and reliability.

The MICRO-ONE is a high-speed microprogrammed micro computer whose flexibility and functional modularity make it ideally suited for dedicated volume applications.

Because the MICRO-ONE is microprogrammable, that software you've already written can be saved. We'll emulate the discontinued micro computer.

If your requirements are for volume quantities of micro computers that *can be* delivered, write or call:

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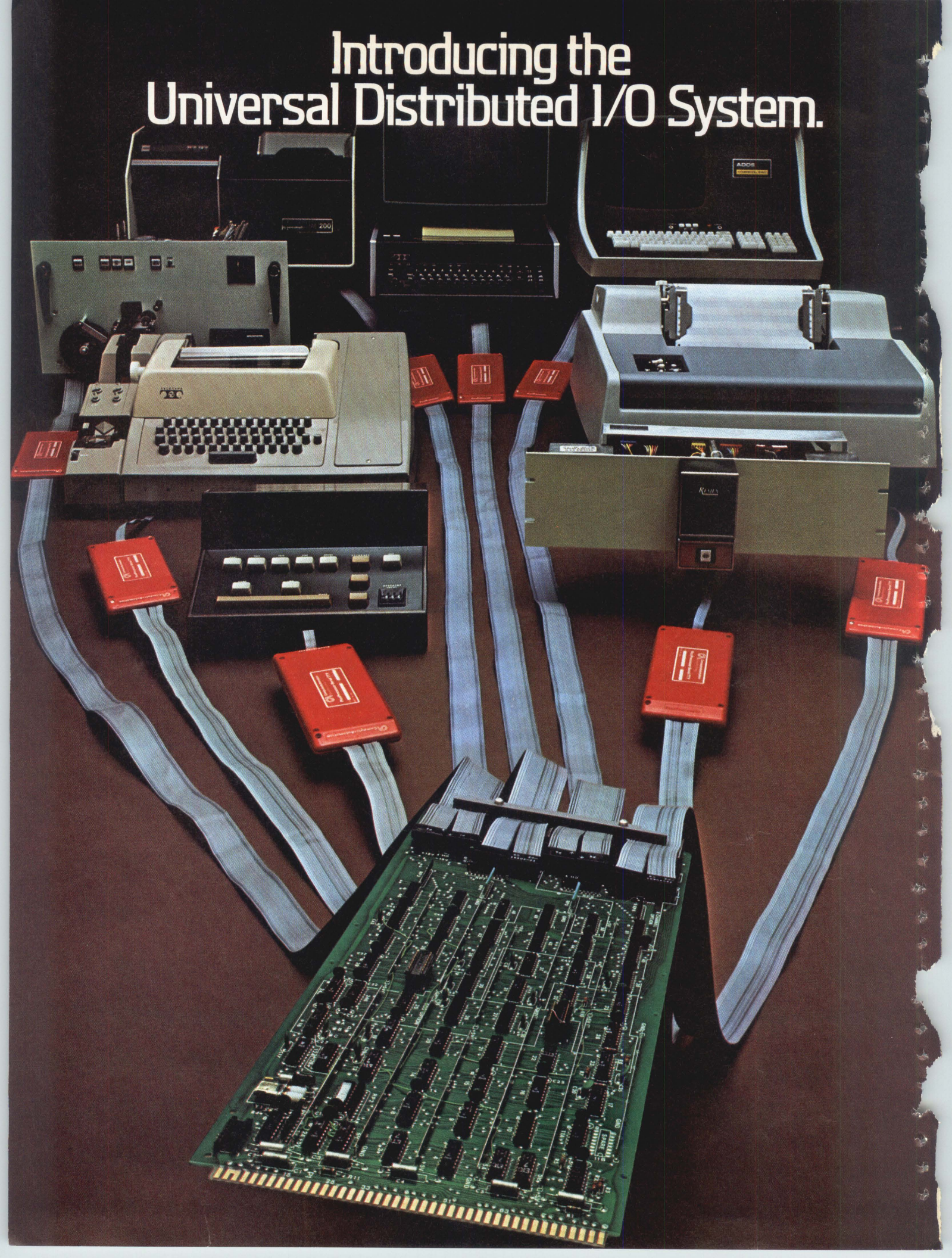


Never again will any of our customers have to design an I/O interface.

The editorial.

There's a lot more to computerizing than computers.

There, we've said it again. No doubt we'll keep on saying it, because besides being a not-always-so-obvious fact, it says everything there is to say about Computer Automation. Who we are and what we do.

So now that we've said it again, we're going to prove it again.

The news.

A bigger-than-life cost breakthrough in I/O interface.

A whole new idea about how to get in and out of the machine.

The death of the black box interface.

It means our customers will never design and build another input/output interface. All of a sudden they can't afford to.

Never? Well, let's put it this way—possibly there are some applications our Distributed I/O System can't handle. It's just that, from an OEM standpoint, we can't imagine what they might be. Talking with dolphins, maybe.

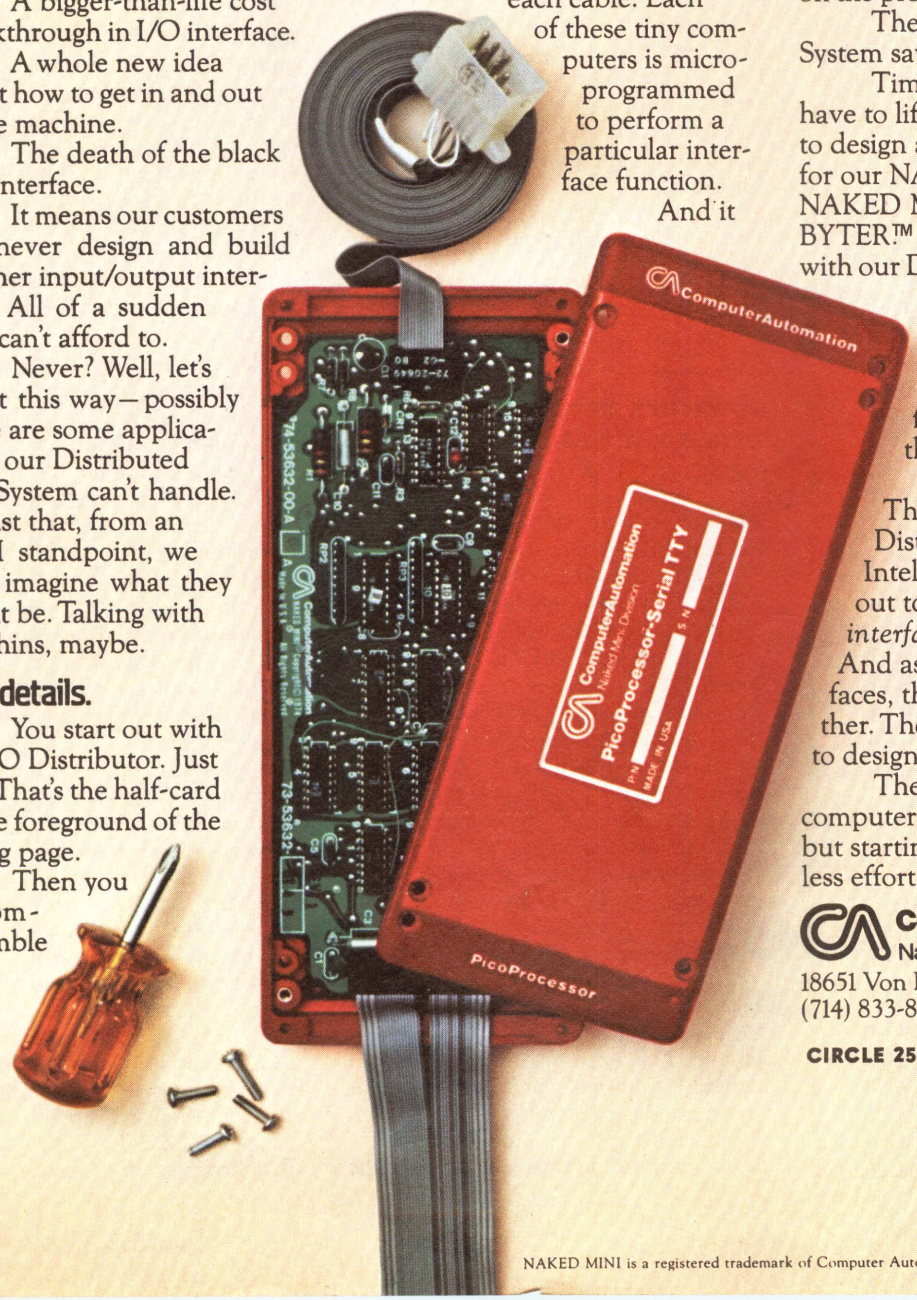
The details.

You start out with an I/O Distributor. Just one. That's the half-card in the foreground of the facing page.

Then you custom-assemble up to eight interfaces (or four in a smaller version) by adding special purpose "Intelligent Cables." There's a cable for general purpose parallel I/O, another for card readers, line printers, paper tape, communications, and so on.

The intriguing part is that there are basically only two cables: one for parallel interfaces and one for serial interfaces. What makes each unique is the PicoProcessor™ molded into each cable. Each of these tiny computers is microprogrammed to perform a particular interface function.

And it works like a charm. A Distributed I/O System can handle any combination of input or output, serial or parallel peripherals, all transferring data directly to or from memory at the same time. Even custom user devices, with special microprogramming.



The bottom line.

There are two things an OEM has to really worry about: beating the competition to market and making a decent profit on the project. Time and money.

The Distributed I/O System saves you both.

Time, because you never have to lift a finger ever again to design an I/O interface. Not for our NAKED MILLI,™ or our NAKED MINI® or our MEGABYTER.™ They're all compatible with our Distributed I/O System.

And money, because there's no way you can design and build interfaces for less then we'll sell them to you.

Here's the proof. The cost for an I/O Distributor and four Intelligent Cables comes out to *less than $200 per interface* for quantity orders. And as you add more interfaces, the cost drops even further. The only thing you have to design is a purchase order.

There's a lot more to computerizing than computers, but starting now, there's a lot less effort involved.

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CIRCLE 25 ON INQUIRY CARD

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A 30-nA beam is focused into a 2.5-μm spot.

The cathode is operated at −10 kV with the deflector and target at ground. Full deflection requires ±180 V from the center position of the beam. Total power dissipation is about 15 W, with 5 W for the cathode heater and 10 W dissipated in a beam-limiting aperature; target power dissipation is 10^{-4} W. Life expectancy of the dispenser-type cathode is said to be at least three years.

Deflection-related limitations are expected to be partially overcome by using two stages of deflection (Fig. 3). Coarse deflectors first select a particular channel in an array of lenses, and fine deflectors provide the second stage. However, this does introduce problems in making accurate lens and deflector arrays.

Memory storage in EBAM is nonvolatile under loss of power or when no accesses are being made. However, when memory accesses are being made, the stored information will be slowly disturbed by repetitive accesses to adjacent storage locations. This will require that the memory be refreshed by algorithm at a rate of less than 10% of the memory activity.

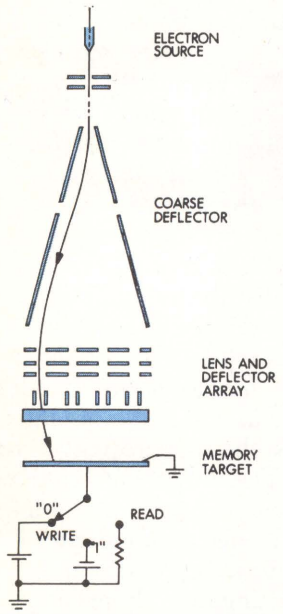

Fig. 3 By using two stages of deflection, limitations inherent to single deflection can be overcome. Accuracy required in fabricating the lens and deflector array adds other problems. However, it is expected that these can be overcome

The first EBAM product, essentially the same as the prototype delivered to Control Data but using a much thinner electron beam and providing higher bit density, will be introduced in mid-1976. It will contain 18 parallel single-channel data tubes, each with 4.2-megabit capacity (a total system capacity of 75.6 megabits). Data organization will be block-addressable, with selectable block size between 8 and 512 bits/channel (16 to 1024 bytes for the 18-channel system). Access to a block will take 5 to 10 μs; system throughput will be 36 megabits/s read, 9 megabits/s write. Model 8500, to be introduced in 1977, will also be an 18-tube system but will develop 33.6 megabits/tube for a total system capacity of 600 megabits. Access time will be 2 to 5 μs, and throughput rates will be 100 and 50 megabits/s read and write, respectively. The company foresees extensions of the technology leading to development of billion-bit tubes.

For further details, see "Bridging the Memory Access Gap," by Dennis E. Speliotis, in the *Proceedings of the 1975 National Computer Conference*, pp 501-508.

Network Processors Streamline Memory Usage at Low Cost

An approach to storage management for multiple processors, developed at Network Systems Corp, St. Paul, Minn, is said to enable much more efficient utilization of large storage systems at cost savings of 75% or more. The approach uses a special-purpose processor and other equipment to monitor the transfer of data to and from a large array of memory devices shared by all processors in a computer network or common to a multiprocessor system.

Functionally, the special-purpose processor, called a network control unit, is a hardware version of the network control software most conventional computers require to interface with a network. Perhaps it can be best described in terms of what it is not. For example, it is not a so-called "front-end" processor such as those used in networks to preprocess input data and monitor communication lines, and thus to relieve the large central processor of these chores. Rather, it is a sort of "back-end" processor to supervise movement of data in and out of the central memory —what company president James E. Thornton calls a "super input/output processor." This task, in some present-day systems, inefficiently occupies most of the time of a general-purpose processor that costs several million dollars, makes growth difficult, and is a bottleneck to the flow of data.

Movement of data is becoming more and more important every day. For one thing, as a user's needs increase, he tends to expand his system. However, economic realities often make installation of a second machine more practical than replacing his present one with a larger machine; later, when more expansion becomes necessary, still more machines of equivalent capability are more economical than the replacement of one of them with a large machine, which would create an unbalanced system.

Furthering this growth is a developing demand for systems that store online data more or less permanently. Such online data have previously been present in only a few highly specialized applications—notably airline reservation systems and bank stock transfer files. In other systems, data came in from a remote terminal, remained only long enough to be processed by a permanently resident program, and were sent back to the same or a different terminal.

Now, with the advent of applications such as point-of-sale and electronic funds transfer systems, online data promise to be in much wider use. They will generate much heavier traffic and place a large burden on the management of the storage medium; Thornton predicts an eventual market of $100 million within five years, for just the control units—in addition to the adapters and other equipment that will be needed. Use of online data will also call for much larger storage capacities; already the production of disc storage units has been growing at 40% per year, and in some large installations the space between processors is practically paved with disc drives—several hundred drives in a single installation is not unusual. To back up these systems, mass storage systems are being developed.

The network control unit is designed to address these problems. A typical system contains two of the units, providing dual redundancy and, consequently, improved reliability for those systems that must remain on the air continuously. Speed is achieved, curiously, by serial transmission of data over a single cable, using con-

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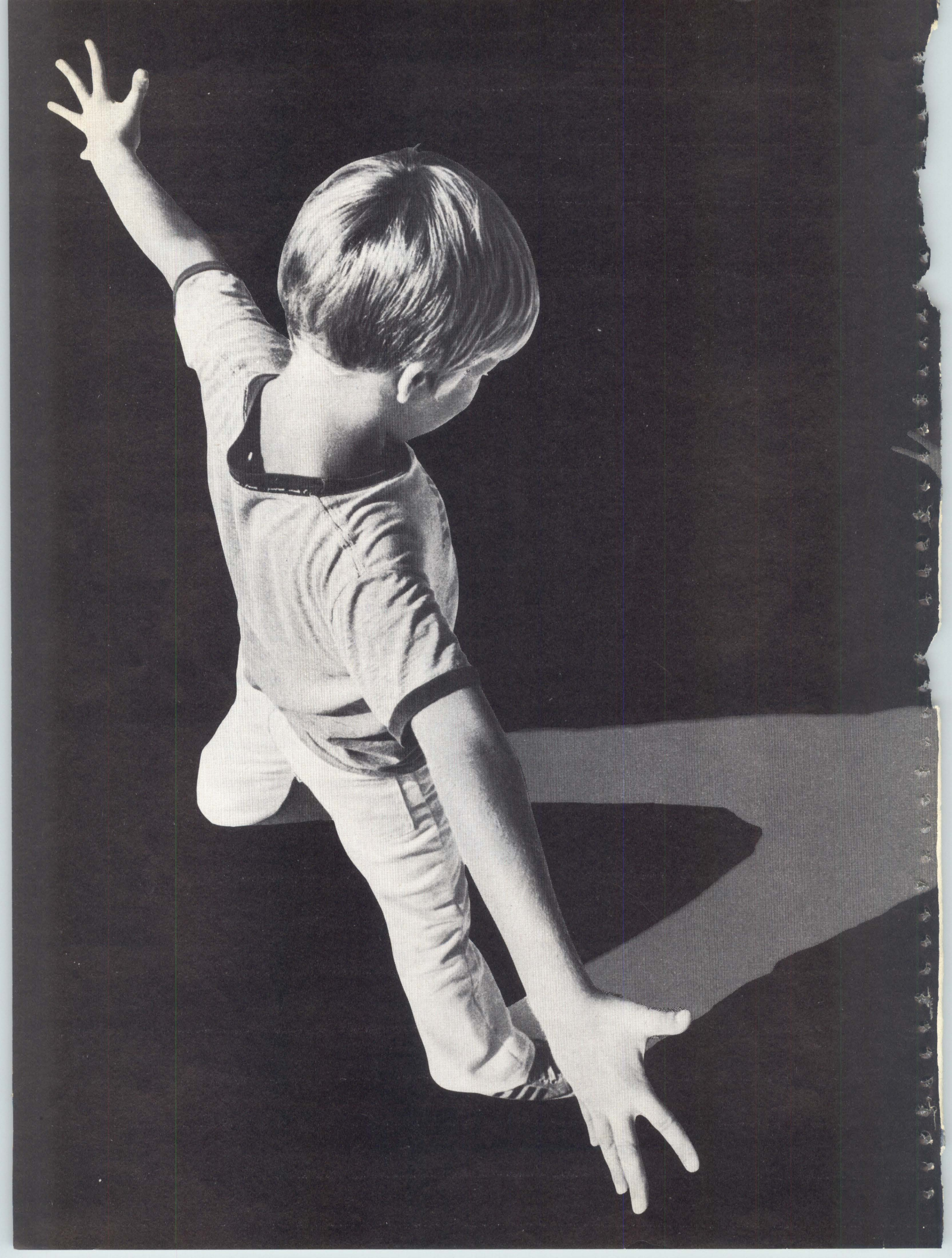

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We delivered our first MAX III operating system in 1971. It was the birth of a new state of the art in minicomputer software.

Since then, while other companies have been laboring to produce their first real-time multiprogramming software, ours has just been getting better.

Today's MAX III, in combination with our MODCOMP II hardware, is just about unbeatable for demanding real-time operations.

Unbeatable in performance. Unbeatable in price.

Hundreds of MODCOMP II/MAX III systems have already proved themselves. Working in every conceivable kind of industrial and scientific measurement and control application.

Consider a few highlights.

In MAX III, 256 execution priority levels give you more flexibility than you're ever likely to need. For everything from highest priority foreground to deferrable background tasks.

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With up to 64K words of directly addressable memory, MODCOMP II gives you a lot more clout than most minicomputers that only let you address 32K 16-bit words at a time.

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Fifteen general purpose registers and overlapped memory enable MODCOMP II to consistently outperform machines that offer only a handful of registers, with a cache memory that is supposed to solve all your problems. But often doesn't.

MODCOMP II/MAX III is fully upward compatible with all other MODCOMP computers, including the 32-bit MODCOMP IV. So you can add on at any time as your needs grow. Even expand into a multiprocessor network system, without reprogramming.

But, like we said. These are merely highlights.

For detailed specs, and benchmark data that shows how MODCOMP II/MAX III stacks up against the best anyone else has to offer, write us.

After all, we're very proud of our young giant. He's already conquered a good part of the world. He's out to beat the rest.

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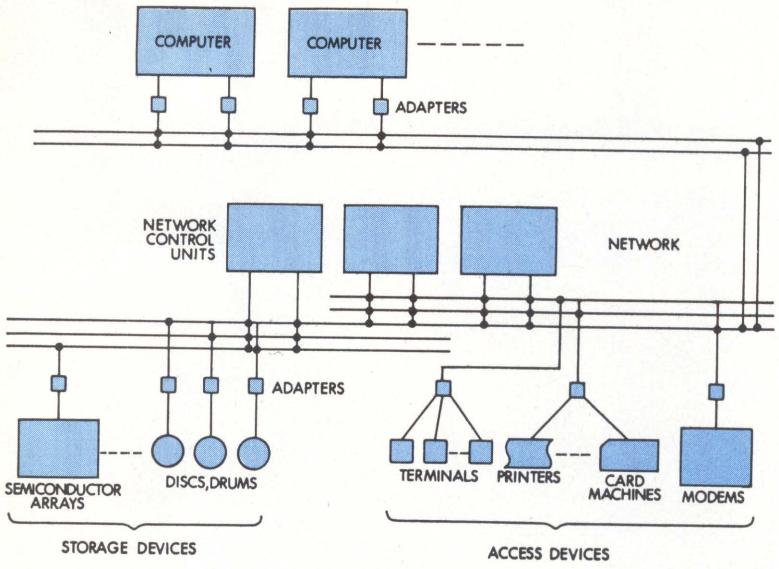
CIRCLE 27 ON INQUIRY CARD



Data transfer manager. When a computer network or multiprocessor communicates with its common storage through a single serial cable monitored by a network control unit—a special-purpose computer—performance is enhanced and cost reduced by as much as a factor of 5. Prospective growth of online data storage calls for this kind of storage management

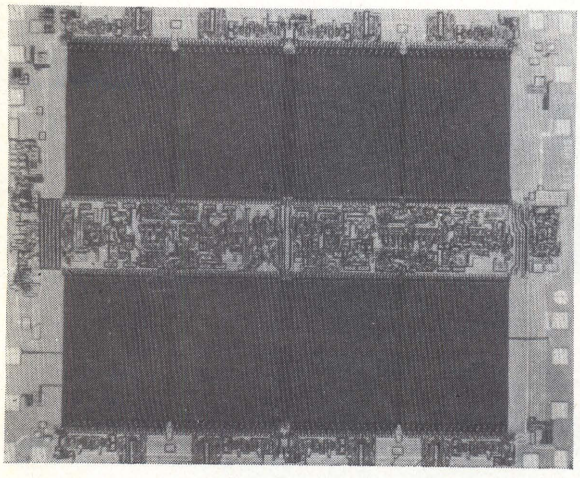
ventional high frequency communication techniques. Adapters perform parallel-to-serial conversion and the reverse, and modulate and demodulate the serial waveform at the interfaces between processor, storage unit, and cable. These techniques permit the cable to be up to 1000 feet long, not the 75 feet of conventional parallel cables; and the cable has a simple connector on each end. (A similar approach has been used elsewhere, notably by Collins Radio Co—now part of Rockwell International Corp—on its C-System, developed several years ago.) Over this cable data are transmitted at 800 megabits/s—exceeding even with serial transmission the performance of conventional parallel transmission. The system designed around the network control unit costs about $800,000, and, according to the manufacturer, surpasses the performance of an IBM 370/168, which sells for about $4 million.

Internally the network control unit consists of several printed circuit cards that control bus interconnections, a series of local processors, up to 131,000 bytes of memory made with 100-ns semiconductor technology, and switches to permit optional configurations to be set up. First installations are planned for the summer of 1976.

High Density 16K CCD Has Applications in Fast Solid-State Memories

Comparable in size to high density 4-kilobit RAMs, a 16-kilobit, 2-level, polysilicon-gate, n-channel charge-coupled-device (CCD) developed by Bell-Northern Research Ltd (BNR), Ottawa, Ontario, Canada is claimed to be considerably smaller than other CCD memory chips of equal capacity. Applications for the 137- x 167-mil device, called the CC16M1, are expected in fast-access solid-state memories that will be competitive with today's head-per-track rotating disc systems. It is said to also be a possible lower cost, higher density replacement part for existing shift registers.

The device requires only two external clocks, each driving 60 pF at one-half the data rate. Organization is quad 4K, with each 4K block functioning as a single shift register at a 1- to 10-MHz data rate. Operating power dissipation at the 10-MHz data rate is <20 μW/bit; standby or idle power is 4 μW/bit. Inputs and outputs are TTL compatible.



A quad 4K configuration is used in the Bell-Northern Research Ltd 16K CCD serial shift register. Specially designed sense amplifiers—one at the output of each 2K array—detect extremely small amounts of charge at high speed, permitting small chip size and high data rate

Each 4K section uses two levels of multiplexing to reduce the rate at which the bulk of the data on chip are shifted. The incoming data stream is split between two equivalent 2K arrays, and then data within each array are further multiplexed by a serial-parallel-serial structure. By reducing the total number of transfers for each data-bit, power dissipation is reduced and internal noise margins are widened.

Packaging is 16-pin DIL with 14 active pins to permit use with standard TTL on a PC board with common busing of ground and 5-V power lines. Timing and voltage levels for inputs and outputs allow serial coupling between 4K sections if desired.

In the near future, BNR, the research and development house of Bell Canada and Northern Electric, will announce a second version having on-chip recirculation with write/recirculation and chip-select inputs. Other possibilities include serially organized 16K x 1-bit and byte-organized 2K x 8-bit configurations. □

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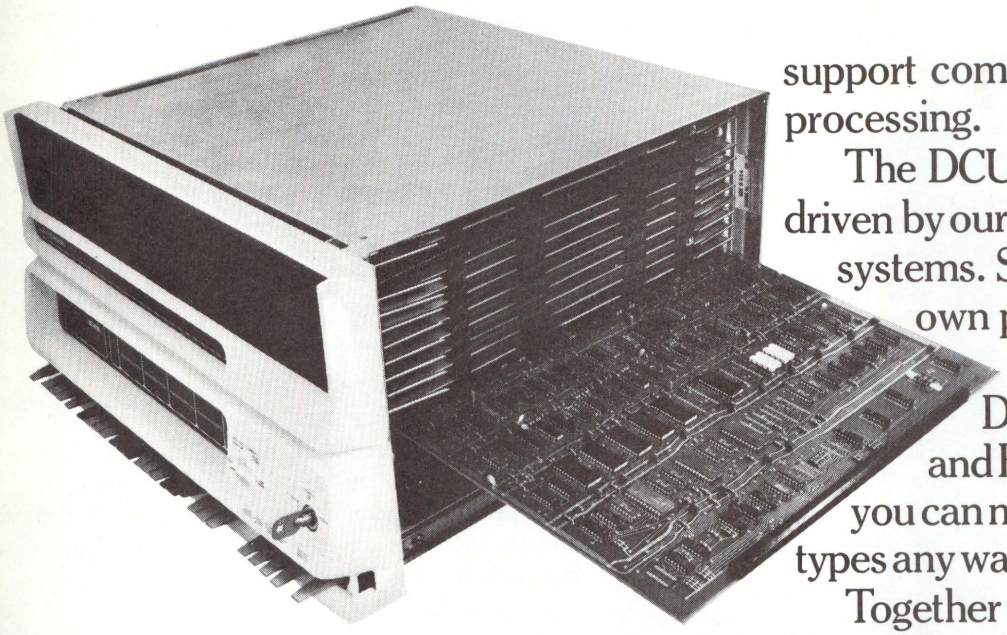

For years, Data General has been the company people have come to for basic communications networks. Because we've always made our computers, peripherals and software completely compatible with each other.

Now you can come to Data General if you want to build big, complex networks.

Because now we have the communications controller board you see here. The DCU/50 (Data Control Unit).

The DCU is designed to work in terminal, switcher, concentrator and front end systems. It takes care of line control and all the character processing. Which leaves the computer free to support communications message processing.

The DCU is programmable and driven by our real-time operating systems. So you can define your own protocols.

Or you can use our Data General teletypewriter and BISYNC protocols. And you can mix your protocols and line types any way you want.

Together with our high density 16, 8, and 2 line synchronous and asynchronous multiplexers, the DCU gives you direct memory access for extremely high throughput, with minimal systems overhead.

And when you need more speed and more lines, you won't have to throw out anything. You can add on to what you already have.

For example, you can start off interfacing our multiplexers directly to the computer. And later on, plug in the DCU.

Which means no matter how big or small you want your network to end up, you can start off communicating with Data General.

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CIRCLE 28 ON INQUIRY CARD

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AMP Latch connectors terminate 10 through 60 leads on multi-conductor flat cable. Simultaneously. They mate with two rows of .025 posts on .100-inch centers. Our 14- and 16-position AMP Latch connectors mate with standard DIP sockets. There's also a family of edge connectors in the line.

Fail-safe. Dual camming and latching ears on the unique AMP Latch folding contacts provide a four-point electrical contact and mechanical grip for each conductor—not just two points—to provide true redundancy. You can inspect the termination itself before the cover is applied. After termination, inspection ports in the connector cover allow visual checkout of each fork-type contact for proper locking and latching. The latching of individual contacts prevents bowing or parting of the covers. The connectors can also be probed under electrical load via the inspection ports. To insure integrity, the cover also locks to both ends of the connector housing with auxiliary latches.

Connects three ways. With AMP Latch, you can interconnect to pc board spring sockets, directly to the board itself, or to DIP sockets—anywhere you want to interface on high-density, .100-inch patterns.

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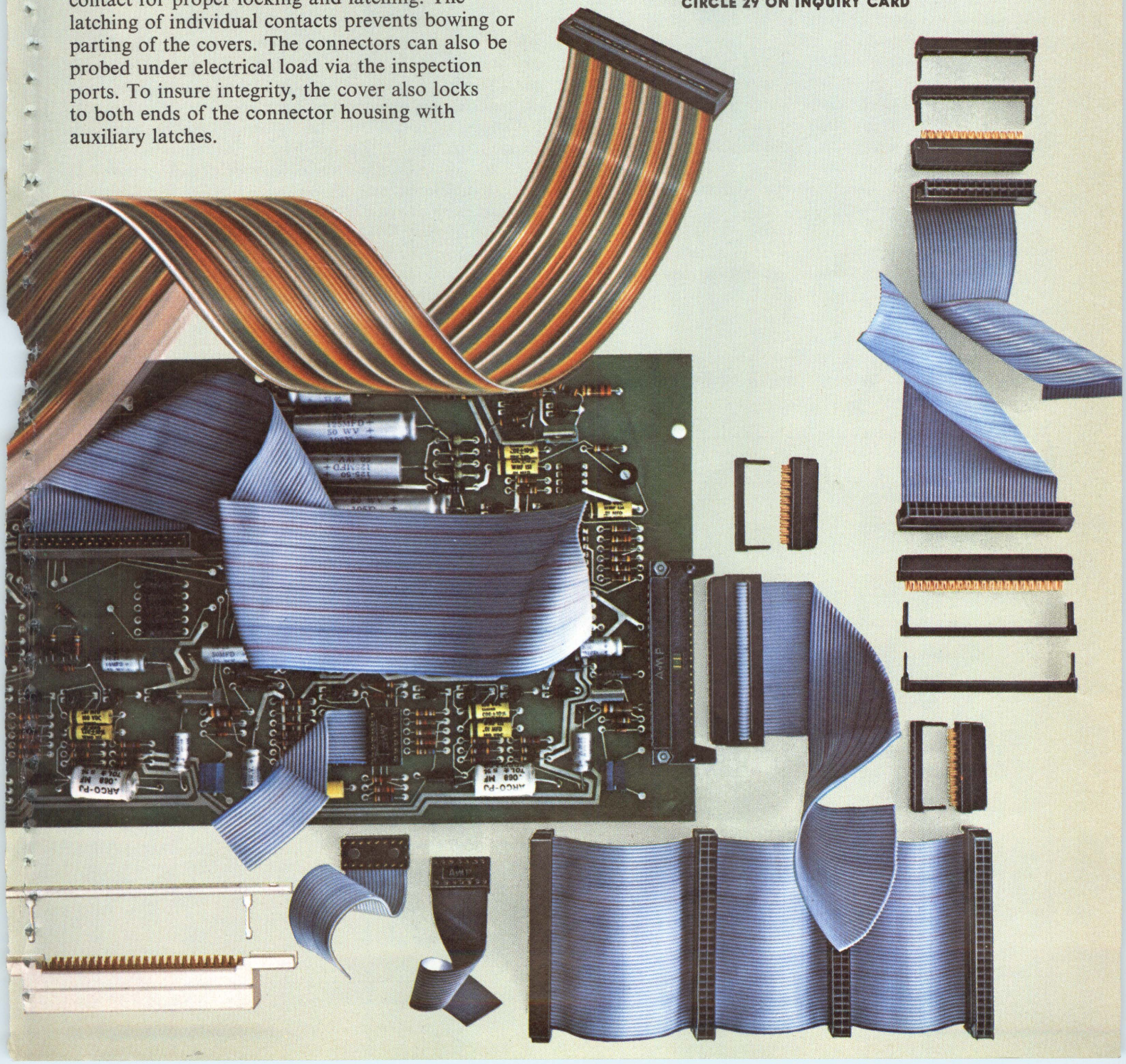

Turbine-Generator Power Systems Operate Under Direct Digital Control

Power generation capacity at one of Pennsylvania Light & Power Co's stations will soon be drastically increased by two turbine-generator systems that will be direct-digitally controlled. The two units, each with 800-MW capability, will bring the Martins Creek facility to a capacity of over 1900 MW.

Design philosophy development for the two additional units began in 1970, at a time when federal, state, and local environmental standards were not yet fully defined. Intensive investigation of labor conditions, equipment availability, and costs of acceptable type fuel resulted in the decision that the primary fuel should be oil and that the system be able to burn either crude or residual.

Currently the system is in startup operation status. Commercial operation will begin after thorough shakedown testing of both power generation and control equipment.

Control System

Direct digital control of the two units is maintained on the turbine and boiler; non-DDC activities include data acquisition, monitoring, storage and retrieval, operator guidance for startup and shutdown, and communications with the power control center via a data link. DDC loops involve turbine, combustion, feedwater, furnace pressure, superheat and reheat temperatures, burner load programming, and eight secondary functions. The non-DDC functions are scanning of plant inputs, alarming, logging, real-time data processing, storing historical data, and displaying information.

Central processor for the system is a Xerox Corp Sigma 3 computer, backed by 64 thousand words of core and 2 million words of auxiliary disc memory. An external input/output processor (EIOP) shares core memory with the CPU through a dual port arrangement such that I/O processing can proceed without interruption (Fig. 1).

Peripherals functioning with the CPU I/O for each unit consist of five trend recorders (four for the operators, one for the engineer), three operator's communications panels, two utility line printers, and a formal logging line printer. In addition, two peripherals are shared by the CPU I/Os of both units: engineer's

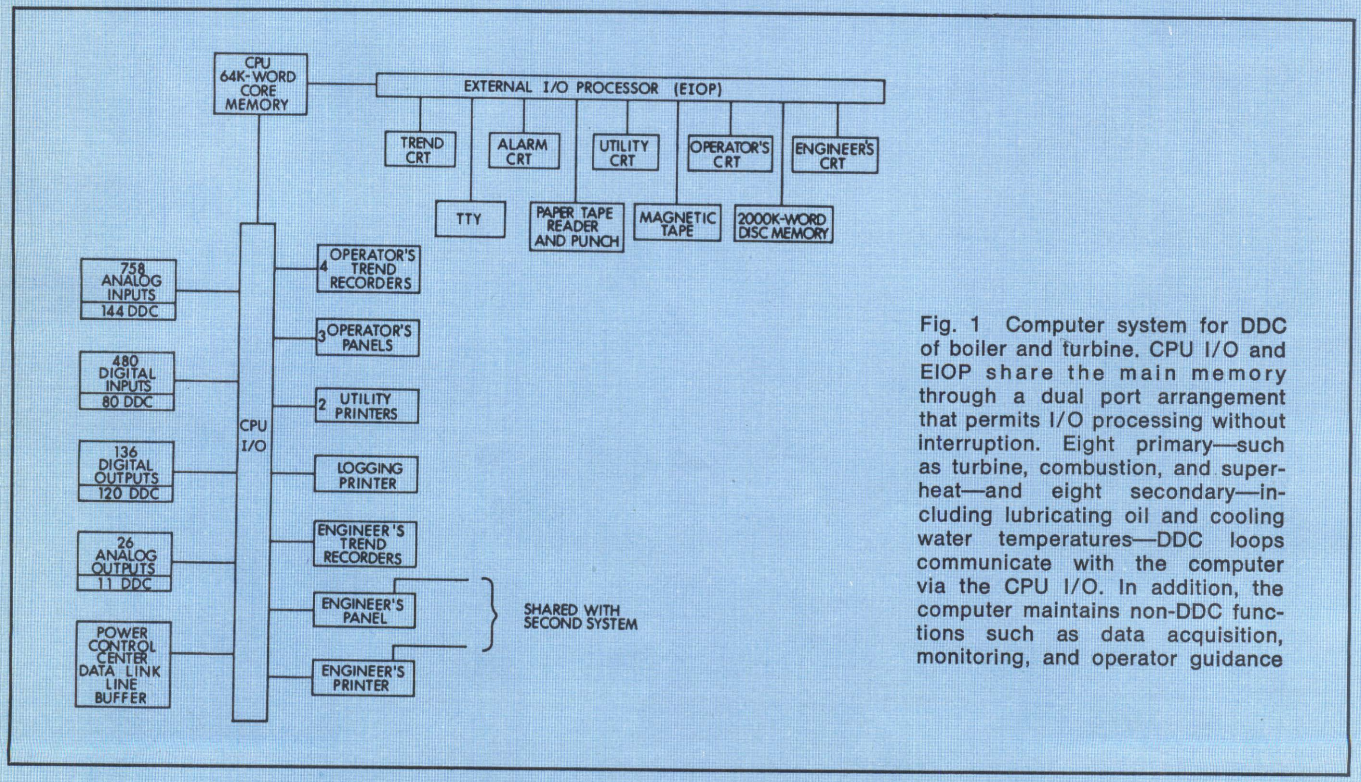

Fig. 1 Computer system for DDC of boiler and turbine. CPU I/O and EIOP share the main memory through a dual port arrangement that permits I/O processing without interruption. Eight primary—such as turbine, combustion, and superheat—and eight secondary—including lubricating oil and cooling water temperatures—DDC loops communicate with the computer via the CPU I/O. In addition, the computer maintains non-DDC functions such as data acquisition, monitoring, and operator guidance

At $1650, You've Never Seen a Portable, 50 MHz Oscilloscope with More Capability and Convenience

New TEKTRONIX 455

• 50 MHz bandwidth. • Dual trace. • Delayed sweep. • Sweep rates to 50 ns/div with 2% accuracy (5 ns/div with 3% accuracy.)
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• Large 8 x 10 cm CRT display.

And that's not all. The 455 offers this performance combined with more convenience features to speed measurements and reduce human error. All at a budget-conscious price. Measurements are made easier and faster with trigger view; trigger holdoff; lighted deflection factor indicators; and a functionally laid out, easily understood control panel.

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For specialized applications, the 455 can be equipped with emi protection or tv sync separator.

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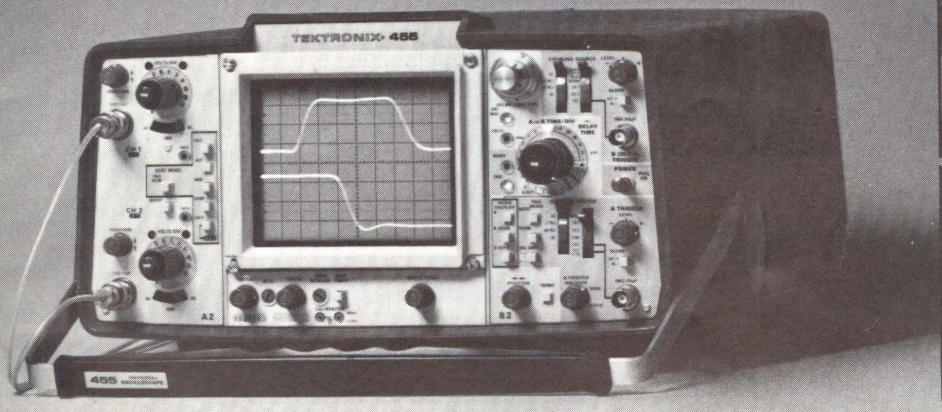

For a demonstration, circle 30 on Inquiry Card.
For more information, circle 31 on Inquiry Card.

communications panel and engineer's utility line printer. The EIOP for each unit, in addition to the disc memory, ties to five CRTs (one of which can be shared with the other unit), programmer's teletypewriter, high speed paper-tape reader and punch, and 800-bit/in., 9-track magnetic tape unit for historical data storage and retrieval. The CRTs display alarm messages, guide the operator, and permit operator/engineer communication with the system.

Combustion control for sliding pressure operation of turbine and boiler is closed loop, as shown in Fig. 2. Target load setter and desired rate of change can be adjusted by either operator or computer. On computer control, the target load setter is set to meet power control center generation requirements transmitted over the data link to the computer. The rate of change limit is operator set, but can be reduced by the computer if an excessive rate of change occurs in boiler or turbine temperatures.

Throttle pressure setpoint is developed by the computer from analog values of generation setpoint, actual generation, frequency bias, and turbine valve position provided by the turbine governor. Turbine valve response to generation requirements is transient, but the valves are reset to a nominal 95% open position over the load range by manipulation of the pressure setpoint.

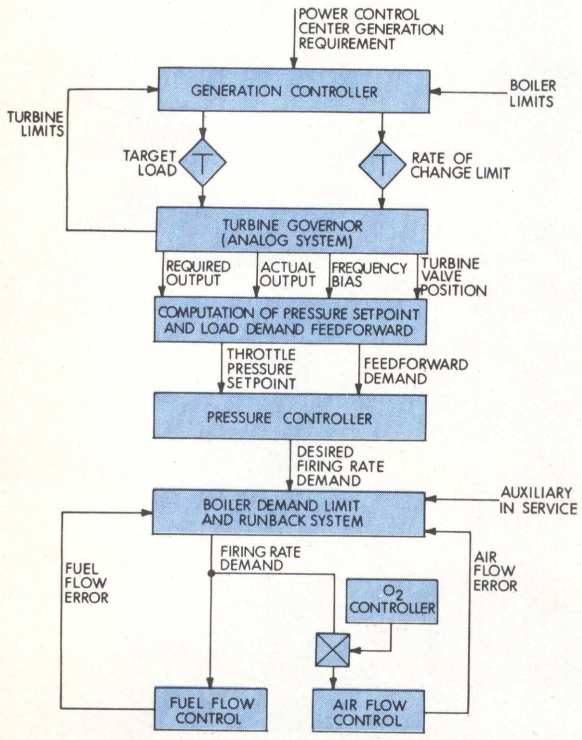

Fig. 2 Combustion control system. Setpoints are developed by the computer from analog measurements made at the turbine. These setpoints together with feedforward demand signals set up demand signals. Limit and runback actions are provided to balance inputs if one is unable to respond

The pressure controller develops firing rate demand from the pressure setpoint and a feedforward demand signal (computed by multiplying steam flow by the ratio of pressure setpoint to actual throttle pressure). Limit and runback actions balance boiler inputs if one input is limited or unable to respond.

Conventional constant pressure mode of operation can also be maintained if desired. In addition, a base input mode of control can be used in which the firing rate is set by the operator (no automatic control of generation or throttle pressure).

Combustion is maintained by control of fuel and air. Fuel flow control consists of high and low range oil flow control valves with corresponding flow meters on each furnace half. At the point of transfer, the two flow measurements are identical, assuring a smooth transfer between meters. Air flow and furnace pressure are controlled by adjusting fan blade pitch.

Feedwater flow control is made up of high and low range valves and meters for the pumps. Both single- and 3-element drum level control, with automatic transfer between the two at a proper load level, are provided.

Four valves are regulated by the superheat control system. Each valve is controlled in a cascade arrangement such that a controller operating from final outlet temperature establishes the setpoint for a desuperheater outlet temperature controller which regulates the desuperheating valves. Reheat is controlled by tilting burners in each furnace half, supplemented by gas recirculation.

Burner load is controlled by computer signals that start or stop elevation of burners to keep fuel oil pressure within limits. Starting the first elevation in service or taking the last out of service can be accomplished only by the operator.

Secondary loop control functions include temperatures of generator stator coolant, main turbine and boiler feedback lubricating oils, air heater cold end, and closed cycle cooling water. Redundant transmitters are provided for critical variables. If two transmitters measuring the same variable show an excessive difference, the computer uses a designated "umpire" to determine the correct input value.

Software

Four basic software modules—controller, software output, end element, and participating—are used for control (Fig. 3). Each module is made up of a common program and an individual data stack to customize the module for a particular application.

Information such as identification, controlled variable name and value, setpoint, constraints, tuning parameters, address and value of feedforward signal, output values, and other required operational data are contained in the data stacks. Required data on loop status are continuously fed to the stacks by a computer input scanning and data processing routine.

(Continued on p 54)

The Elite 1520A Video Terminal.

New from Datamedia.

Conversational. The Elite 1520A speaks your application language, and is ideal for interactive programming, data entry, information retrieval and simply anyplace the need for data communication is important.

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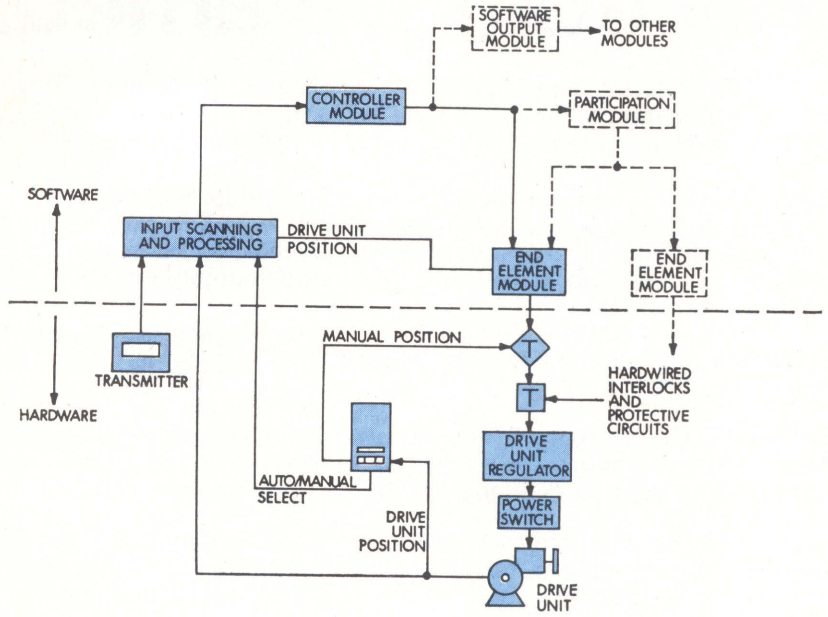

Fig. 3 Typical DDC loop. Hardware elements are shown below dash line and software modules are above. Each of the four software modules is made up of a common program and an individual data stack that customizes that module to a particular application. Data stacks contain pertinent data such as constraints, tuning parameters, and value of feedforward signal required for operation of the loop

A typical program for combustion control (illustrated in Fig. 2) consists of controller modules for throttle pressure, flue gas oxygen, fuel flow, and air flow. These are coordinated by calculations which develop setpoints and feedforward signals for the controllers. Data calculated by the programs are passed to the data stack of the associated controller.

Determination of flow setpoints for fuel and air flows proceed serially from a calculation of pressure setpoint and feedforward demand that is passed to the pressure controller which then produces a desired firing rate demand. This demand is the setpoint for the fuel flow controller and, after correction by the O_2 controller output, the setpoint for the air flow controller.

Summary

A major advantage of DDC over analog systems is the potential for improved operator/engineer communication with the control system. The Martins Creek installation uses CRT displays to input setpoint changes and calibration and tuning adjustments as well as for troubleshooting. Displays are provided for controller, software, and end-element module data stacks.

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DC&AS BRIEFS

DCC Measuring Machine

Double the productivity of previous automated coordinate measuring machines is claimed for a direct computer-controlled (DCC) unit developed by The Bendix Corp's Automation and Measurement Div in Dayton, Ohio. Latest model in the company's Cordax family, the DCC machine uses a measurement drive and computer system to provide fully automatic inspection in three dimensions as well as model tracing, NC tape generation, and mathematical analysis.

In use, the operator simply mounts the part to be measured on the machine and presses a button. A servo drive system moves the gage probe through three axes of motion (X-Y-Z) at a speed of 5 in./s. Probe movement can be either continuous for such items as on-the-fly measurement of contours, or intermittent for discrete measurements of hole and edge locations, diameters, or other geometrical relationships.

Measurements, to 0.0001″ in each axis, are read out on a programmable digital display which also shows computed values of program variables. All data are recorded in hard copy on a high speed printer. A hand-held programmable control box enables complete remote system operation at the measuring site rather than forcing the operator to go to the computer in the display cabinet each time a control change is required.

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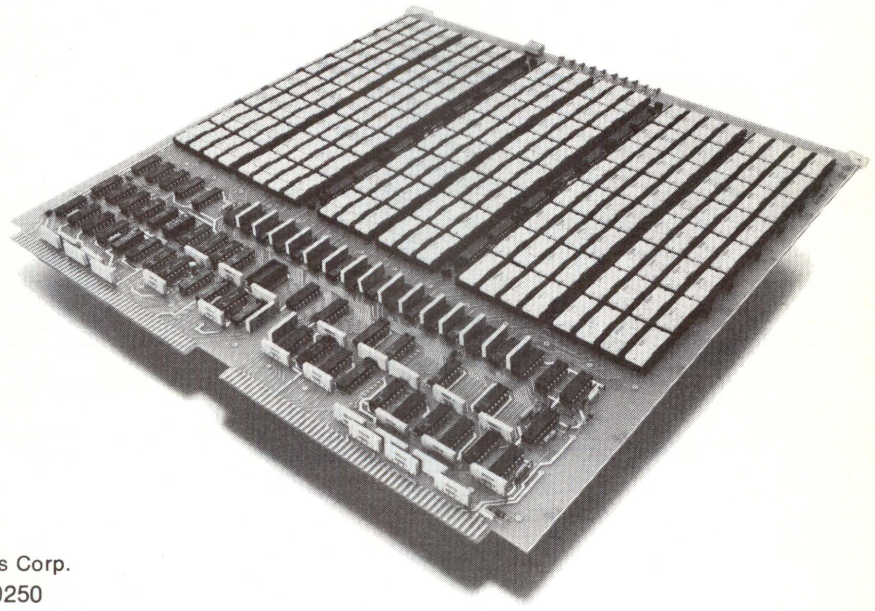

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Compared with conventional SSI/MSI design, for example, Macrologic devices represent a significantly higher level of integration—up to 250 gates per device..

So fewer parts are required.

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93436/93446	512 X 4	NOW
93438/93448	512 X 8	NOW
TTL RAMs		
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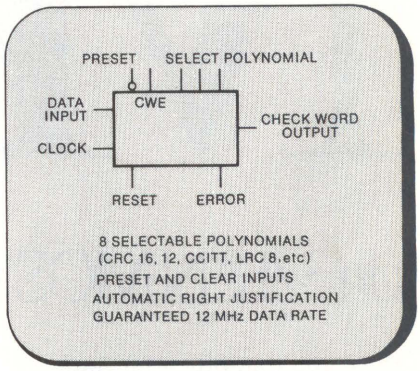
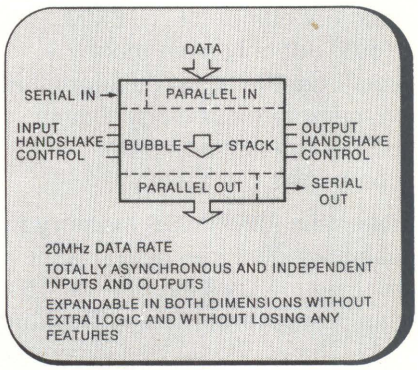
93412/93422	256 X 4	3rd Q
93415/93425	1024 X 1	NOW
93L415/93L425	1024 X 1	NOW

DEDICATED SUBSYSTEMS

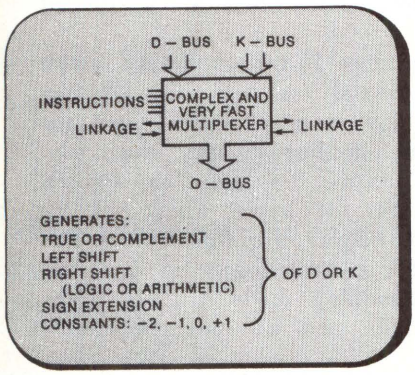


The 9401 Cyclic Redundancy Check Generator/Checker is an advanced tool for implementing the most widely used error-detection scheme in serial digital data handling systems. A 3-bit control input selects eight different generator polynomials, including CRC-16 and CRC-CCITT, as well as their reciprocals (reverse polynomials). Separate Clear and Preset inputs are provided.

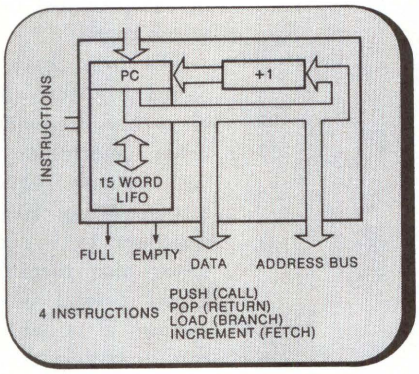


The 9403 FIFO Buffer Memory is a high-speed expandable fall-through type with totally independent and asynchronous inputs and outputs. Organized as a 4-bit wide by 16-word deep "bubble stack," it has four bits parallel and bit-serial data inputs and outputs. Complete "handshake" control signals are provided for unambiguous operation in asynchronous systems. It is intended for disk and high-speed communications applications with data rates of up to 20 MHz.

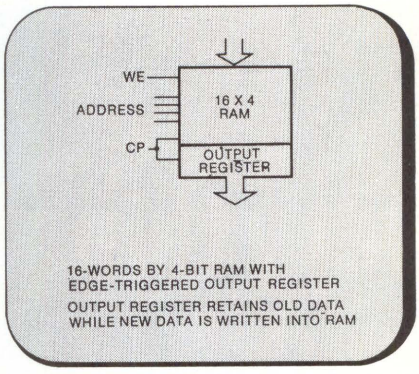
FUNCTIONAL BUILDING BLOCKS



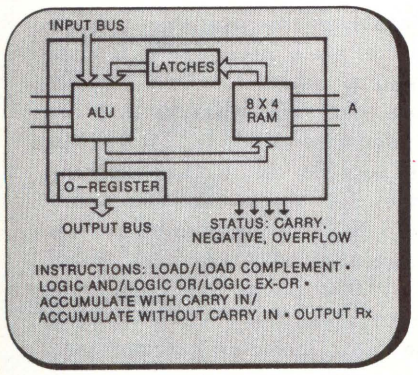
The 9404 Data Path Switch (DPS) is a very fast combinatorial array for closing data path loops around arithmetic logic networks (like the 9405 ALRS). A 5-bit instruction word selects one of the 32 instructions operating on two sets of 4-bit data inputs. Four linkage lines are available for expansion in 4-bit increments. The delay is less than 30ns over 16 bits. Samples available August.



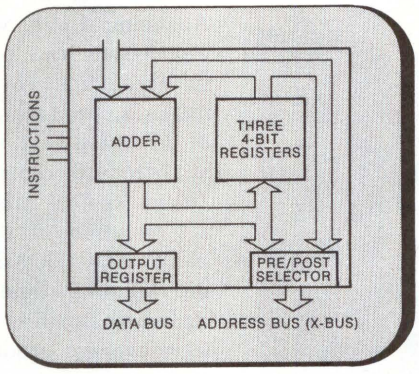
The 9406 16-word by 4-bit "Push Down-Pop Up" Program Stack stores program counter and return addresses for nested subroutines in programmable digital systems. It executes four instructions — Return, Branch, Call, and Fetch as specified by a 2-bit instruction. The 9406 may be expanded to any word length without additional logic and operates at a 10 MHz Microinstruction rate over 16 bits.



The 9410 64-bit Read/Write Memory is a register-oriented high-speed device organized as 16 words by four bits. An edge-triggered 4-bit output register allows new input data to be written while previous data is held. Three-state outputs are provided for maximum versatility. The 9410 operates at a 10 MHz Microinstruction rate.



The 9405 Arithmetic Logic Register Stack contains a 4-bit arithmetic logic unit (ALU), an 8-word by 4-bit RAM, an edge-triggered output register, and associated control logic. The ALU implements eight different arithmetic or logic functions where one of the two 4-bit operands is supplied from the input data bus and the other is supplied from one of the eight registers selected by the Address inputs. The result of the operation is loaded back into the same register and is also loaded into the edge-triggered output register and becomes available on the 3-state output data bus. The 9405 operates at a 10 MHz microinstruction rate over 16 bits.



The 9407 Data Access Register (DAR) performs memory address arithmetic for RAM resident stack applications. It contains three 4-bit registers — program counter, stack pointer and operand address — a 4-bit adder, a 3-state address output buffer and a separate output register with 3-state buffers. The DAR performs 16 instructions, and operates at a 10 MHz Microinstruction rate. Samples available August.

DC&AS BRIEFS

Digital Watch IC Tester

A computerized tester used by American Microsystems, Inc of Santa Clara, Calif to check electronic watch ICs reduces test time by a factor of 18. More than 180 tests involving about 5400 measurements are executed in 4 s; the same tests performed manually would require about 72 s.

Originally developed by Watkins-Johnson, Palo Alto, Calif to test military reconnaissance system components, the automatic digital assembly test equipment (ADATE) is built around a 620L minicomputer made by Varian Data Machines, also of Palo Alto. Testing is performed twice on each IC—once just after it is bonded to the circuit board and again when other circuit components have been added. The tester can be programmed to accommodate each of seven different watch types.

The first check determines if the oscillating circuit containing the quartz crystal can perform within an allowable frequency range near 32 kHz. Then the tester determines if the decoding circuits which convert the raw frequency into minutes, hours, and seconds are operating and whether the drivers which link the decoders to the digital display are functioning. The tester also measures the current drawn to light the liquid crystal or light-emitting diode displays to be certain it is within limits, and will not prematurely run the battery down.

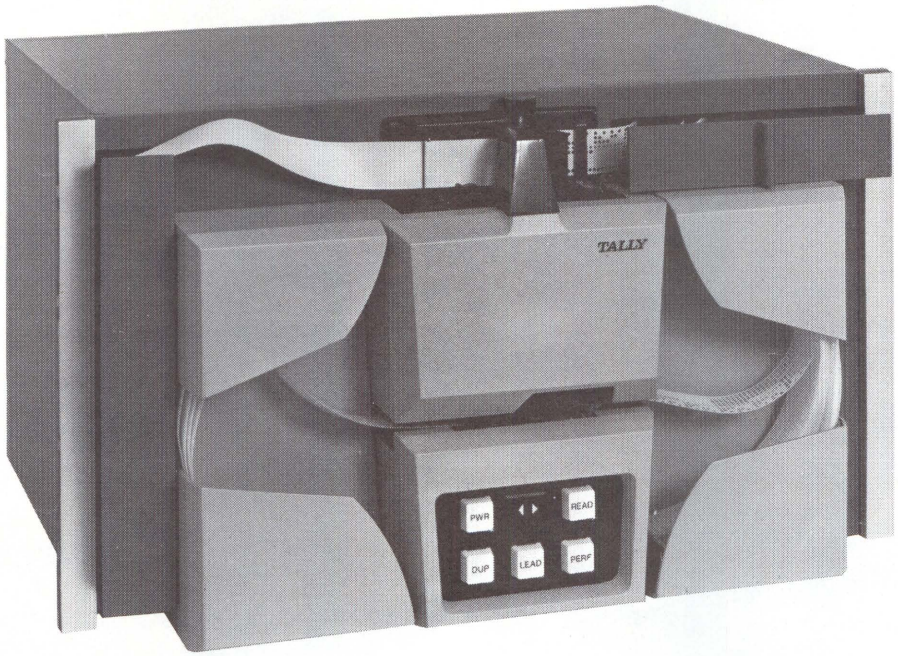
Wire Bonder Control System

Increased productivity and improved uniformity of semiconductor packaging plus lower cost are claimed to result from combining the L101 automated wire bonder control system, made by General Automation, Inc, Anaheim, Calif, with commercially available bonders. The system can provide as much as a 270% increase in throughput over manual ultrasonic ball bonding methods, producing more than 2500 wires/hr at a cost of 0.7 to 0.8 cent/wire, compared to 700 to 900 wires/hr at 1 to 1.3 cents/wire possible on manual machines (using typical labor rates for Mexico and the U.S.).

Resolution of 0.000125 in. with positioning repeatability of 0.000062 in. are attained. Cycle rates excluding bonding time are 10,000 points/hr; burst rates including bonding time are about 3500 wires/hr. Long-term average production rates, including operator setup and parts insertion, removal, and replacement, are about 2500 wires/hr. The system electronically corrects for both die and substrate placement inaccuracies, accommodating X- and Y-axis translation errors up to ±1 in. and rotational errors on any center point up to ±89 deg.

To set up and program or to change an existing routine, the operator steps through the correct positions for the bonding head by moving the X-Y table with a joystick. To check his work he allows the unit to step through the bonding cycle automatically. Depressing a button then initiates continuous operation. □

The price match



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Operation and features of a 4-kilobit semiconductor memory are related to how it can be used in the design of a mainframe memory system for a typical minicomputer. The system contains 16,384 words, each 16 bits long, with the associated electronic circuits that control the memory and interface it with the computer

Designing Minicomputer Memory Systems with 4-Kilobit n-MOS Memories

Dick Brunner

Motorola, Incorporated
Semiconductor Products Division
Phoenix, Arizona

With the advent of advanced design techniques and the perfecting of n-channel semiconductor processes, an entire new breed of metal-oxide semiconductor (MOS) memories has emerged—notably, a series of 4096-word-x-1-bit dynamic memories that overcome many disadvantages of earlier devices. For example, Motorola's MCM6605 requires only one clock pulse that has no critical overlaps with other signals, while all its inputs and outputs are compatible with transistor-transistor logic (TTL), and its access time is only 210 ns. High density, low power, and high speed make it suitable for mainframe memory applications.

The memory's 4096 storage cells are divided into four equal quadrants (Fig. 1). The chip also contains input address latches, row and column decoders, and controls for data input and output. Three internal clock signals—$\phi 1$, $\phi 2$, and $\phi 3$—control reading from or writing into the storage cells; they are controlled by the incoming signals, chip enable (CE) and read/write (R/W).

The $\phi 1$ clock is on whenever CE is low (standby condition). This phase precharges the memory's dynamic circuitry in preparation for the start of a memory cycle. When CE rises (at the beginning of every cycle), it turns off the $\phi 1$ precharge and turns on the $\phi 2$ clock. While $\phi 2$ is on, several things happen. First, it latches the input addresses into buffers that drive the column decoders. The decoders use the five least significant address bits to select two columns of 64 storage cells—one on each side of the chip—and to transfer the 128 stored bits onto individual, precharged bit sense lines. Meanwhile, the row decoders use the remaining seven address bits to select one of the 128 bit sense lines. The selected bit, together with a data control cell, drive an exclusive-NOR, which in turn drives an output buffer and latch. With this done, the $\phi 2$ clock turns off.

If the R/W line is high, writing is inhibited; the cycle is terminated as CE falls, allowing $\phi 1$ to precharge the memory before the next cycle begins. If the R/W line is low, when $\phi 2$ goes off, the $\phi 3$ clock turns on. This clock pulse returns the data on 127 bit sense lines to the storage array. However, the 128th line, selected by the row decoder, has been overridden by an input bit, which replaces the bit stored previously in the addressed cell. The write cycle is terminated at the end of $\phi 3$; CE returns to its low, or standby, state.

The $\phi 2$-to-$\phi 3$ sequence of bringing data from the storage cells onto bit sense lines and then putting those data back into the cells inverts the stored data, polarity of which is kept track of by a row of data control cells added to the array. These cells, identical to the storage cells and driven by the same column decoders

that drive the storage cells, are inverted during each write cycle. By passing both input and output data through an exclusive-NOR gate with the control cell tied to the addressed column, the relative polarity of data in that column is maintained.

As described, the write cycle refreshes 127 cells in two selected columns while it writes new data into one cell. Normal write and read cycles both execute with the chip select (CS) line low (part of the addressing process at the memory system level), permitting data to pass to or from the chip. However, if the CS signal is high, a write cycle merely refreshes all 128 cells. One such refresh cycle on each of the 32 combinations of the five least significant address bits refreshes the entire memory; each address combination must be used at least once every 2 ms.

When memory power is first turned on, the data control cells may not reach a valid logic level until after completion of several refresh cycles. This causes no difficulty, however, since the memory system does not normally write data immediately. For testing, a 200-ns pulse applied to one pin presets the cells; this preset pin should be permanently grounded in most systems.

Memory System

A memory system for a typical minicomputer using 4-kilobit chips can be divided into four sections (Fig. 2): memory-central processing unit (CPU) interface, refresh control, memory timing control, and the memory array itself. An interface with a bus-oriented minicomputer includes addressing logic, line drivers and receivers, and a memory data register, and requires 38 bus lines—18 address, 16 data, and four control. Two control signals specify whether a data transfer is to be a full-word read, full-word write, or a write into one of the two bytes of a 16-bit word (Table 1); the other two synchronize the beginning and end of read and write cycles.

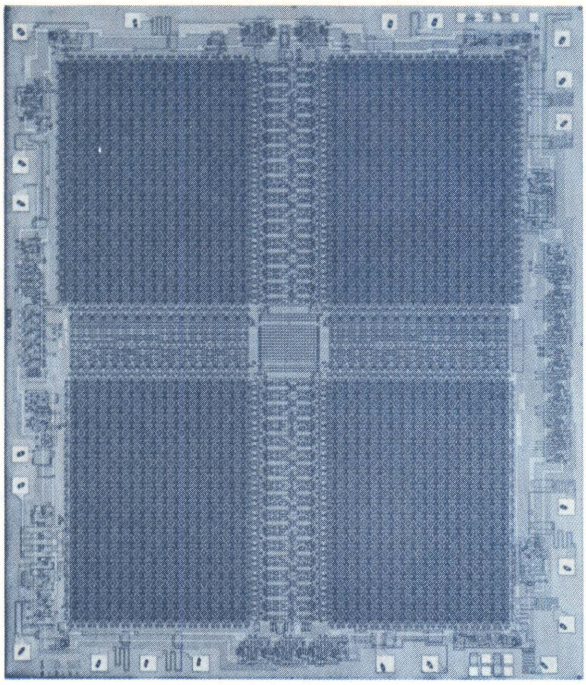
The 18 address lines (Fig. 3), on which the low level is a binary 1 and the high is 0, point to one of 262,144 8-bit bytes; but since the computer and memory are organized around 16-bit words, the least significant address bit, A_{00}, indicates one of the two bytes (bits 0 through 7 or 8 through 15) in a single word. The next 12 bits, A_{01} through A_{12}, are connected in parallel to all of the 4-kilobit memory integrated circuits (ICs) to select one of 4096 words of 16 bits each. One printed circuit (PC) board carries 64 of these ICs, which are addressed in four blocks, each with 16 ICs or 4096 words. Physically, the ICs are arranged in four rows and 16 columns, divided into two groups of eight columns, each with its own R/W control signal. This partitioning scheme permits both byte and word transfer; one row of 16 ICs stores the two bytes of each word in a block of 4096 words. Address bits A_{13} and A_{14} select one of the four blocks.

Thus one board's capacity is 16,384 words. With address bits A_{15}, A_{16}, and A_{17}, which point to one of eight of these 16K memory boards, capacity expands to 131,072 words. These last three address bits are decoded in a jumper box on each board so that the board responds to only one of the eight combinations of these bits. Its response, properly gated, is a signal called memory board enable (MBE).

In any bus-oriented computer, the interface between the bus and memory or any other device requires receiver and driver circuits that match transmission-line characteristics of the bus lines. Important features of receiver circuits include high input impedance, to minimize loading of the line; high noise immunity; and differential inputs to receivers, to provide either true or complementary signals. Commercial receivers meeting these criteria are available with either a 3-state or open-collector output; a single package typically contains four circuits.

When a differential receiver is used with a single-ended signal, one input must be connected to a reference voltage, which, for noise immunity, should be halfway between the minimum high and maximum low voltages specified for that signal. A suitable reference voltage generator (Fig. 4) produces a constant 1.95 V—optimum reference for this system's minimum high of 2.5 V and maximum low of 1.4 V—regardless of line receiver current drain.

Chip Details



A typical dynamic random-access memory, such as the Motorola MCM6605 (photo), stores 4096 individually accessible bits. This device is fabricated in the n-channel silicon-gate process, and stores data in standard 3-transistor cells in order to keep its internal sense amplifiers simple. Besides fast access time and low power dissipation, the chip has TTL-compatible inputs with latching on the address inputs, and 3-state output with chip-select control to permit easy memory expansion. It requires one high-voltage clock and has no critical timing or signal overlaps. Although, like all dynamic memories, it requires refreshing every 2 ms, its columns are refreshed two at a time so that only 32 refresh cycles are required.

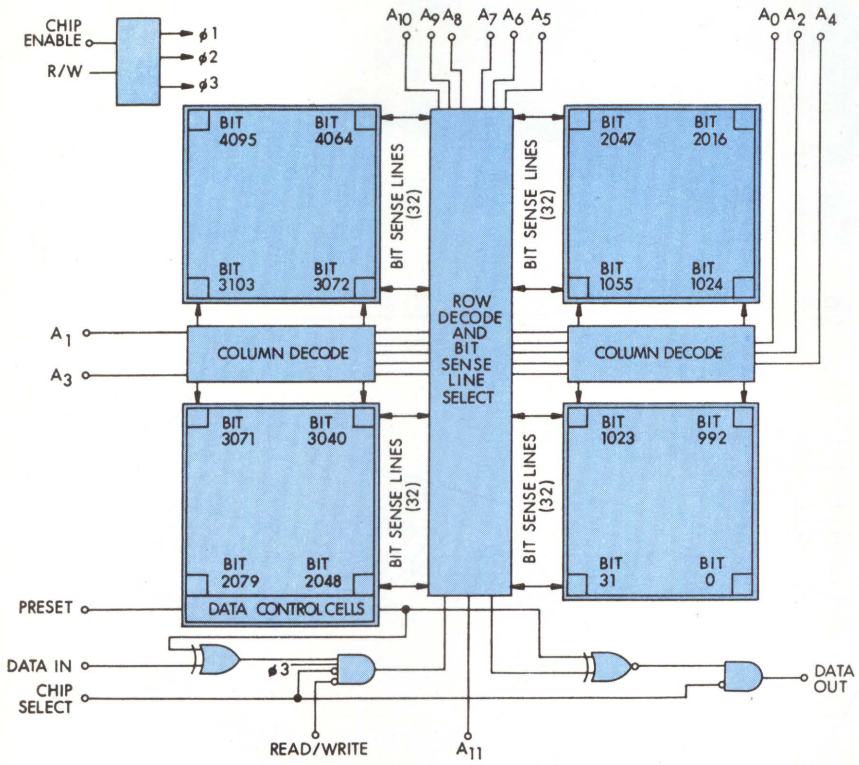


Fig. 1 Storage array. The four quadrants of this 4-kilobit memory are separated by decoders for row and column lines. Column lines are common to quadrants on both sides of column decoder; row decoder picks out one of 128 bits. Every write or refresh cycle inverts the state of all bits in a column; data control cells at bottom of array keep track of which state is which

TABLE 1

Memory Control Truth Table

C_0	C_1	A_{00}	Condition
X	0	X	Read
0	1	X	Write (0-15)
1	1	0	Write (0-7)
1	1	1	Write (8-15)

X = don't care

Only the 16 data lines, which have bidirectional transfer, require special drivers. Data transmission on this data bus requires open-collector drivers with outputs that remain high when not transmitting data, but that also are capable of sinking 50 mA while the out-

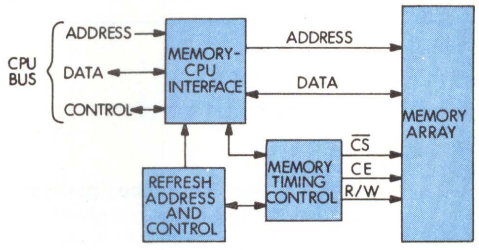


Fig. 2 Memory system. Collection of 4-kilobit memory chips, such as that in Fig. 1, requires other circuits to be used in a computer. They may be classified into interface, timing control, and refresh control

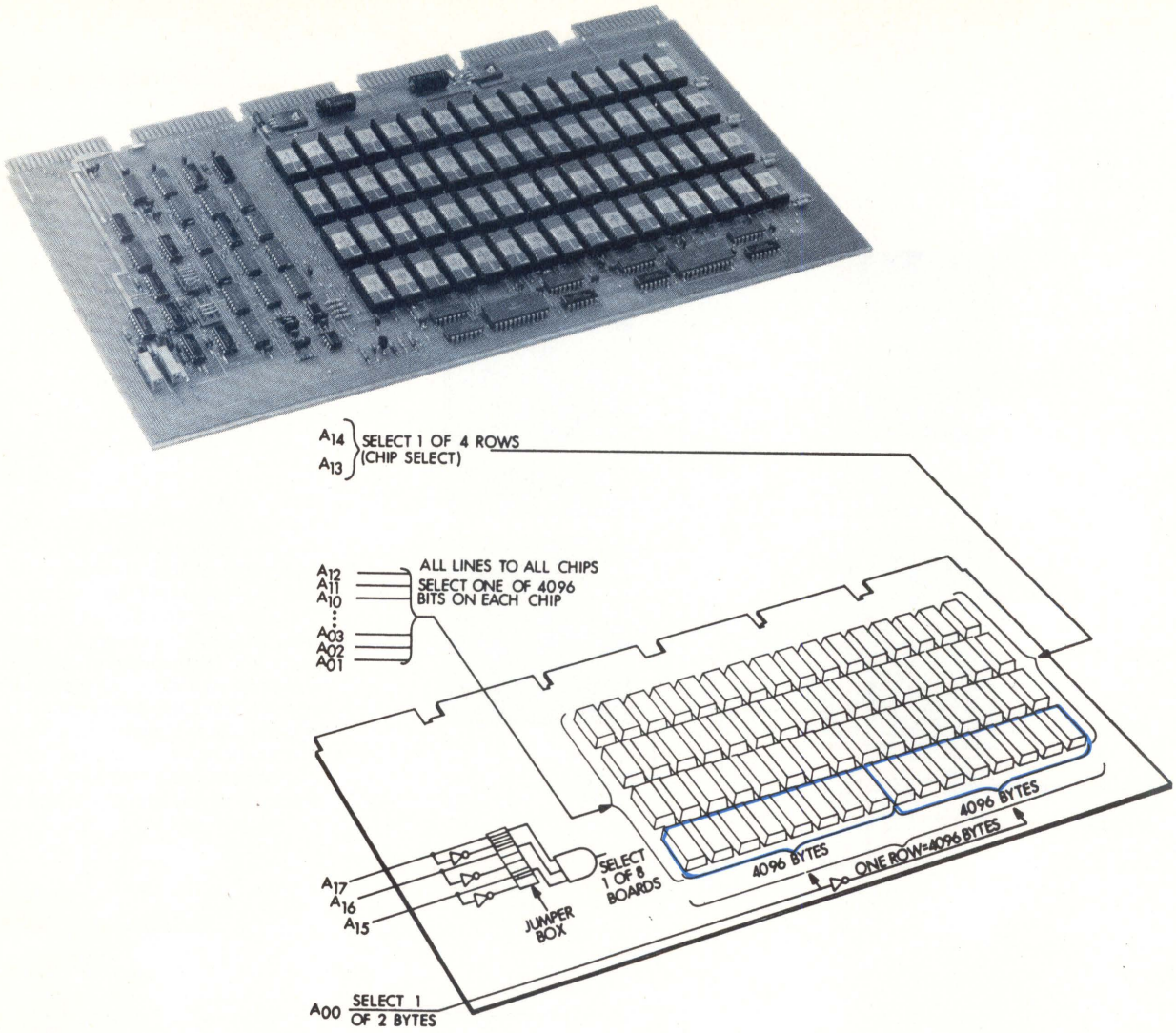


Fig. 3 Board layout. An 18-bit address locates any one of up to 262,144 8-bit bytes. Of the 18, the three most significant bits select one of up to eight boards, and the next two indicate one of four rows of chips on that board. The next 12 address bits locate individual storage cells on a chip, and are common to all the chips on the board. Finally, the least significant bit identifies which of the two bytes in the word addressed by the other 17 bits is the desired one. Photo is one of the eight boards in a system; besides the 64 memory chips, it also carries control circuits and address decoders

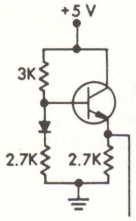


Fig. 4 Reference generator. A voltage halfway between the specified 1 and 0 levels is a comparison level for single-ended signals feeding differential receivers. The diode tracks variations in the transistor's base-emitter voltage that occur as the temperature changes, keeping the output nearly constant

put voltage in the low state is less than 0.8 V. (Ideally, this voltage would be 0, but no circuit is absolutely ideal, and the voltage tends to rise when the driver is carrying a heavy current.)

The memory data register—the last section of the interface—retains data on the bus after the CPU has terminated the CE signal but before the system read cycle is complete.

Memory Timing Control

The memory control section oversees interaction between the CPU and memory system during read and

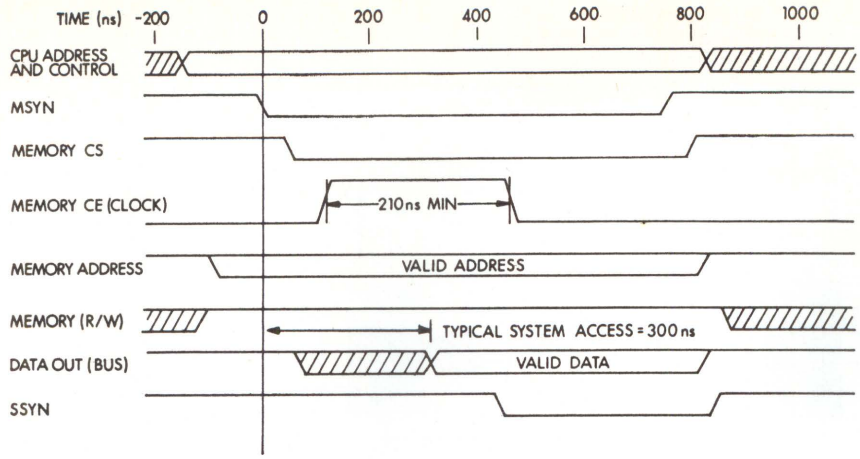


Fig. 5(a) Read cycle timing. Cycle begins with MSYN, 150 ns after placement of the address on the bus; MSYN turns on chip select (CS) and chip enable (CE). After a 330-ns interval, during which data are placed on the bus, SSYN turns on; the processor responds by turning off MSYN

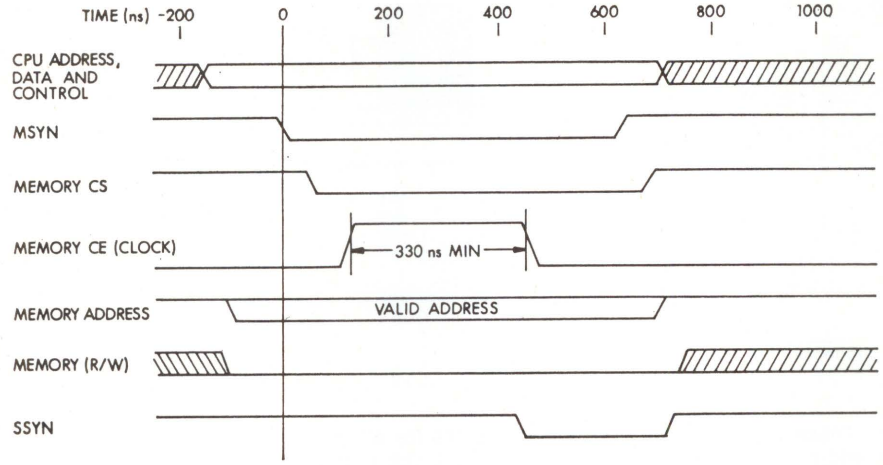


Fig. 5(b) Write cycle timing. This is identical to the read cycle, except for data transfer direction, and quicker response to SSYN by the processor, which now is not required to intersperse a strobe between leading edge of SSYN and trailing edge of MSYN

write cycles. At the start of a read cycle [Fig. 5(a)], the CPU sends out the desired address, together with a 0 level on the control line, C_1, which tells the memory system that the ensuing operation is a read cycle. After waiting 150 ns to allow address deskewing and decoding, the CPU signals the start of the cycle with a master synchronization (MSYN) signal. When the signal arrives at the memory timing control circuits, address, CS, and CE signals are sent to the array. CE lasts for 330 ns; as the $\phi 2$ clock on the memory chip, this is 120 ns longer than necessary, but the memory timing controls are simpler if the same duration is used for a read cycle as for a write (in which the full 330 ns is required). At the end of that interval, the memory controller generates a slave synchronization (SSYN) signal to indicate that data read from the memories have been placed on the bus. When it receives SSYN, the CPU strobes the data into its own register and turns off MSYN, which ends the read cycle.

In a write cycle [Fig. 5(b)], data and address are placed on the bus, together with control signals (C_1 set to 1 indicates a write cycle, while C_0 indicates a full-word or 1-byte write; if the latter exists, A_{00} indicates which byte). As in the read cycle, a 150-ns delay is followed by MSYN, causing the control board to forward the address, data, CS, and CE to the memory array. At the end of the 330-ns CE pulse, the memory controller sends SSYN to the CPU, signaling that the data have been stored. The CPU immediately terminates the write cycle by releasing MSYN.

These sequences show that the timing of both read and write cycles is very simple, requiring no critical overlapping of signals; consequently, the memory control section (Fig. 6) is equally simple. At the start of any cycle, control lines C_0 and C_1 force the R/W lines to all chips into the proper state, as the address arrives on the bus. Later, the MBE signal from the memory-CPU interface circuitry turns on, gated by the MSYN line following the address decoding delay. Two 1-of-4 demultiplexers decode address bits A_{13} and A_{14}. One demultiplexer, gated by MBE, generates a CS signal to one block of 16 memory chips. If the memory board contains fewer than the maximum number of ICs (as it might in a system combining semiconductor and core memory, for example), a jumper box transmits a CS only to the populated part of the board, and prevents an SSYN signal from being generated if a nonexistent word is mistakenly addressed.

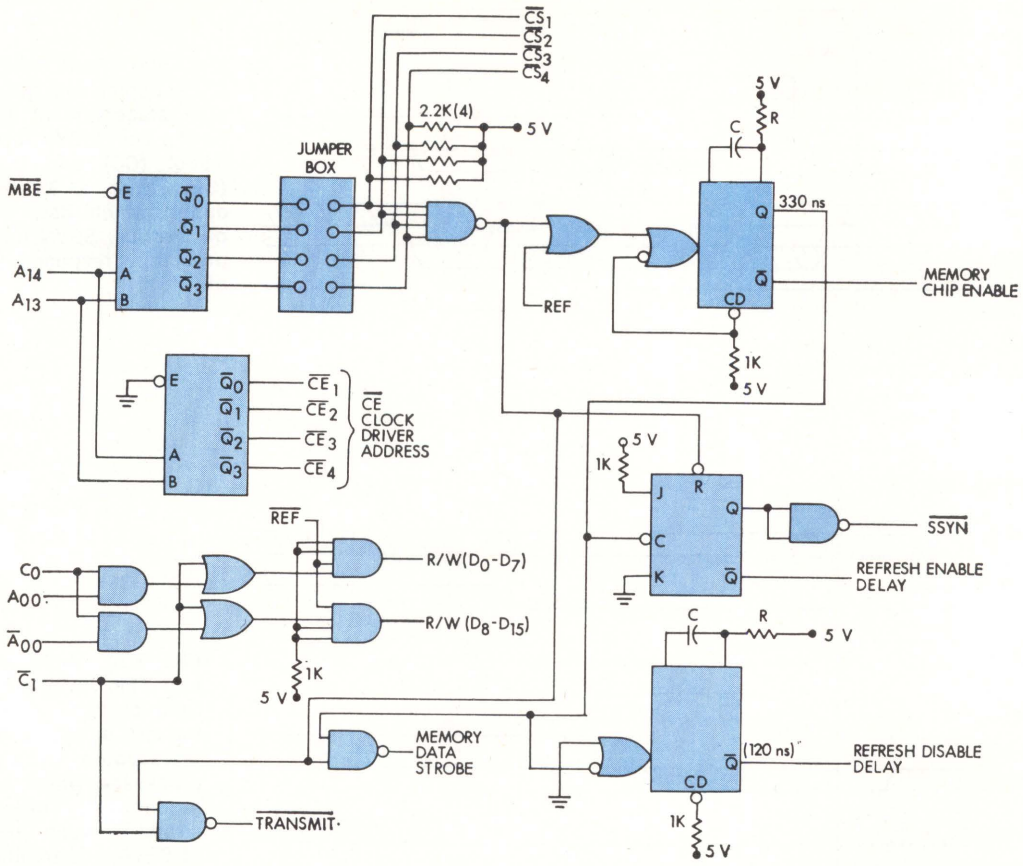


Fig. 6 Memory controls. These are the basic control logic gates for all memory cycles. Two demultiplexers decode the address bits that define which memory block is to be read; one is gated by a signal that acknowledges a board selection, preventing activation of a block on unselected boards. The other does not require gating at its input, because its output is gated by a signal originating at the first demultiplexer

In a read cycle, any one of the four CS signals enables the data bus drivers with a signal called transmit, and triggers a one-shot, which generates the CE signal, 330 ns in duration. To conserve power, CE is gated by the CE clock address lines (outputs of the demultiplexer mentioned previously), so that only one row of memories receives a clock pulse.

On the trailing edge of the CE pulse, when reading, data are strobed into the memory data register and a J-K flip-flop is turned on; this generates the SSYN line to the CPU, which registers the data and responds to SSYN by turning off MSYN. In a write cycle, the CPU turns off MSYN immediately upon receipt of SSYN. Either way, the fall of MSYN in the memory controller turns off MBE, which then resets the flip-flop, terminating SSYN.

As shown in Fig. 6, the complementary output of the flip-flop that generates SSYN is called refresh enable delay. This signal, sent to the refresh control logic, delays the start of a refresh cycle if one is requested during a CPU cycle. The delay insures the minimum interval between successive CE signals.

In the refresh cycle, a refresh request (generated periodically) enables the refresh address and disables the MBE signal. The latter, in turn, disables the CS signal to the memory array and the SSYN signal to the CPU. However, the refresh request itself generates the 330-ns CE pulse, which is sent to the entire array —not gated to particular blocks of ICs, as is the case with read and write cycles. Its trailing edge triggers a 120-ns one-shot, called refresh disable delay (RDD), which prevents a CPU cycle from being requested during a refresh cycle, and again to insure the minimum interval between successive CEs.

Refresh request also prevents the five address bits, A_{01} through A_{05}, from reaching the memory chips, sub-

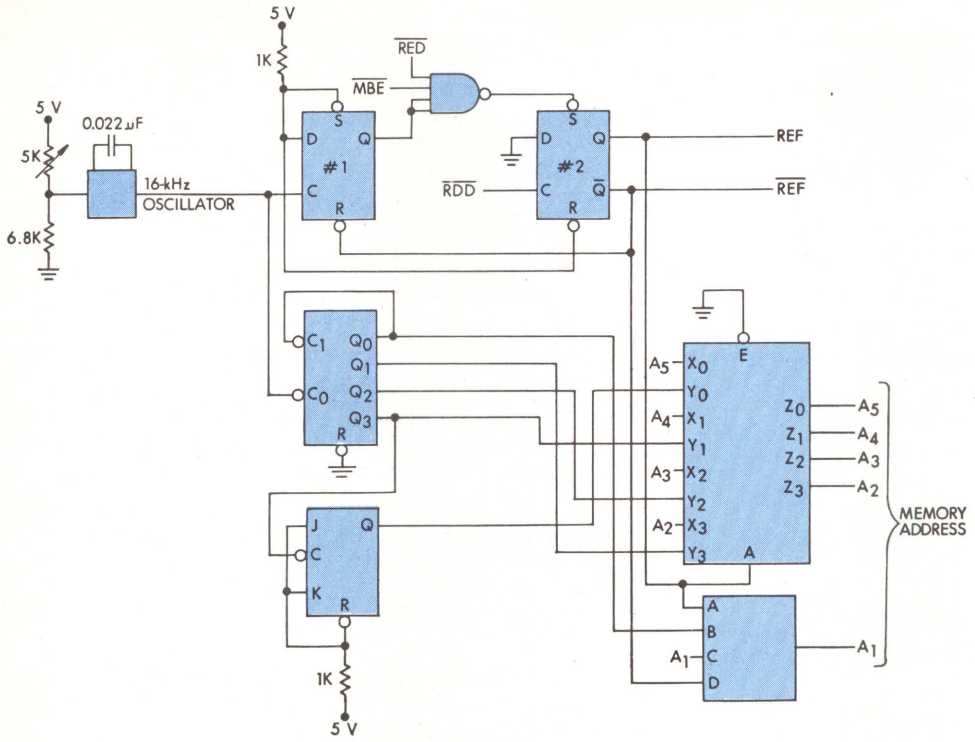


Fig. 7 Refresh controls. One refresh cycle is taken every 62.5 μs, controlled by the 16-kHz clock, so that every column in the memory is refreshed at least once every 2 ms. A refresh address is substituted for the CPU address in every refresh cycle, by the multiplexing arrangement shown

stituting for them five other bits that specify which column is being refreshed.

Refresh Address and Control

The third section of the system—refresh control—insures that data are retained, by refreshing the whole memory once every 2 ms, as noted earlier. This can be accomplished by having a write cycle performed on each of the 32 column addresses at least once during the 2-ms interval. Although refresh could be performed by a burst of 32-column refreshes at the end of 2 ms of normal operation, it could seriously interfere with some CPU functions. A better approach is to steal one column refresh cycle after about 70 normal read and write cycles, or once every 62.5 μs, refreshing a different column each time.

The 62.5-μs refresh interval is the period of oscillation of a 16-kHz clock, set to this frequency with an external capacitor, fixed resistor, and variable resistor (Fig. 7). On each positive transition of the clock signal, a logic 1 propagates through the two flip-flops, the second of which generates the refresh request—provided, of course, that no memory cycle is in process. If MBE is on, the first flip-flop stores the clock's transition until the cycle ends, at which time the second flip-flop is set and a refresh request is made. The request sets a 0, or write, level on the R/W lines to all memory ICs, and switches the refresh column address onto the five lines, A_{01} through A_{05}, replacing the external address from the CPU. This address gating requires five 2-input multiplexers, available packaged as a quad and a single unit, as shown in Fig. 7. The refresh address is generated with a 5-bit counter assembled from a quad unit and one-half a dual unit and incremented by the negative transitions of the 16-kHz clock. The refresh cycle terminates at the trailing edge of the RDD pulse, which turns off the refresh request flip-flop.

Although the address inputs of a particular component may have an input capacitance of no more than 5 pF, their total parallel input capacitance in the array can exceed 300 pF. Such a high load cannot be switched quickly by standard TTL gates (due to insufficient current drive); thus a high speed buffer to provide the current is required in the address lines. This fast switching can cause considerable overshoot, however, which calls for a 10-Ω series damping resistor to be inserted in the buffer's output. The output voltage of the buffer in the high state is likely to be higher, even when heavily loaded, than that of loaded standard TTL gates, thus meeting the memory's high-state input voltage minimum.

A quad clock driver (Fig. 8) is necessary for memory CE input, which must drive 16 chips in the system. Internal logic in the clock driver selects one of the four outputs, for a normal memory cycle, or all four at once, for a refresh cycle. The circuit also has three enable inputs, with which memory expansion to 65,536 words on one PC board is possible.

TABLE 2

Typical Power Requirements for a 16K-Word x 16-Bit Memory Board

Power Supply	Standby Power (W)	Active Power (W)
12 V (V_{DD})	0.84	1.1
−5 V (V_{BB})	0.8	0.8
5 V (V_{CC})	4.5	4.75

System Performance

In a determination of the system's performance under computer program control, access time, measured from the rise of MSYN to the rise of SSYN (data arrival on the bus), was 305 ns; cycle times, from the rise of MSYN to the fall of SSYN, were 830 ns for read, 730 ns for write. The read cycle is longer because of cable delay on the bus and because the rise of SSYN and fall of MSYN at the CPU must be separated by a register strobe. If the SSYN latch were clocked with a one-shot having a pulse output narrower than that of the CE one-shot, it would shorten the write cycle time (some of which is spent waiting for the CPU to acknowledge SSYN), because the SSYN would be sent to the CPU earlier.

Although dynamic memories have essentially zero power dissipation when in standby mode (CE is logic 0), V_{DD} and V_{BB} power lines show considerable dynamic current transients when the memory is active (Fig. 9). To insure that this noise does not exceed 0.35 V on the V_{DD} line, one low-inductance, 0.01-μF capacitor for every two memory chips is required between the V_{DD} line and ground. To maintain a 20-ns rise time for CE, these bypass capacitors should be separated by no more than 1.2 in. A similar capacitor for every four memory devices is required on the V_{BB} line, and one for every eight memory chips on the V_{CC} line (which supplies current only to the output buffer).

Total system power dissipation (Table 2) was measured while running worst-case noise-test patterns. However, certain data transfers—primarily direct memory access by an I/O device—greatly increase V_{DD} power, because they require many active cycles in sustained rapid succession (as opposed to pauses between memory cycles that are characteristic of CPU operation). Maximum active V_{DD} power dissipation for this system in direct memory access operation is 4.46 W—over four times the normal active dissipation. Even with this worst-case figure, however, power per bit is extremely favorable compared to that of other memory systems exhibiting comparable performance. In standby mode with refresh, average dc power figures taken from Table 1 show 23.4 μW/bit typical for this system.

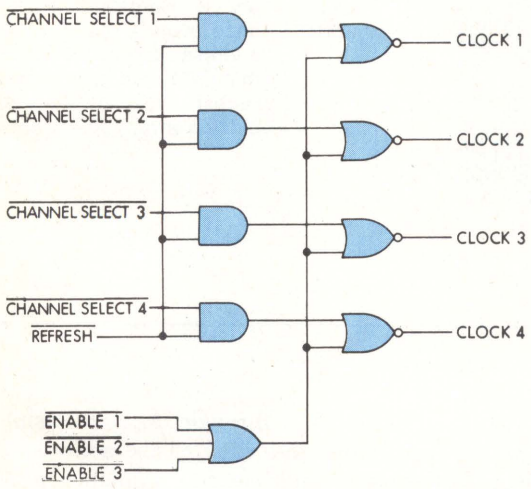


Fig. 8 Current driver for 16 chips. Normal logic block does not produce enough current to switch so many loads quickly, because of their capacitance; this special circuit provides that current

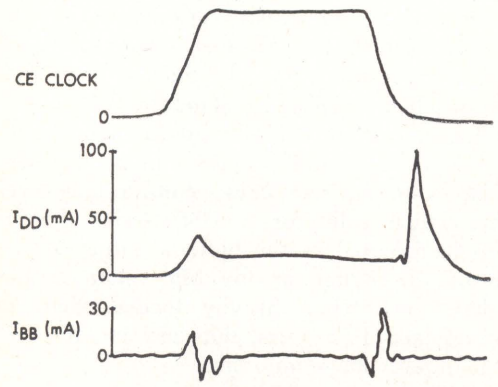


Fig. 9 Power-line transients. Dynamic memories in active mode generate large spikes in their power lines. This calls for adding capacitive bypasses to the lines to prevent obliteration of stored data by such spikes

Summary

The complete design of a minicomputer memory system around a 4-kilobit n-channel MOS memory has been examined. Some recently announced semiconductor memory interface components, incorporated in the design, reduce package count and enhance system performance. Because of the high density, high speed, and low power of these ICs, they should be rapidly and widely accepted for other mainframe memory system applications.

Dick Brunner is a senior computer applications engineer at Motorola's Semiconductor Products Div, with responsibility for design and application of memory systems employing semiconductor memories. He holds a BSEE degree from the University of Colorado and an MSEE degree from Arizona State University.

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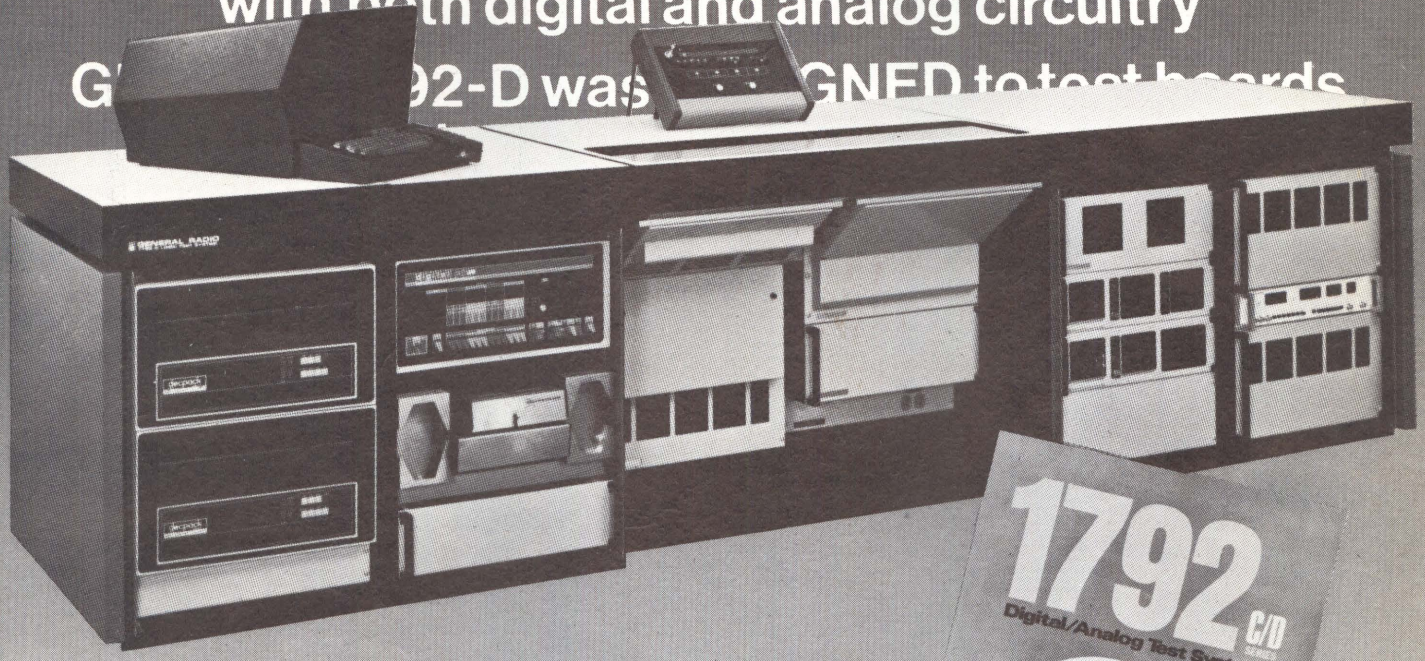

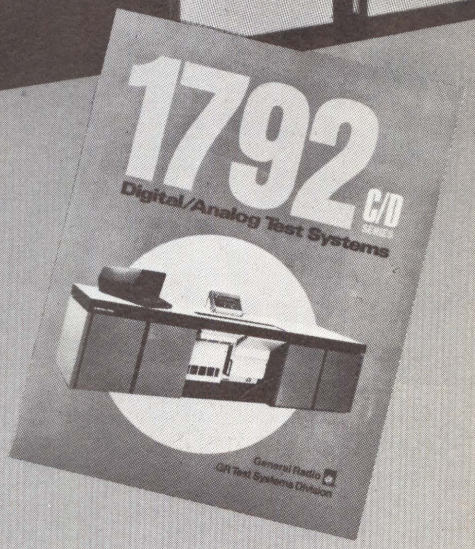

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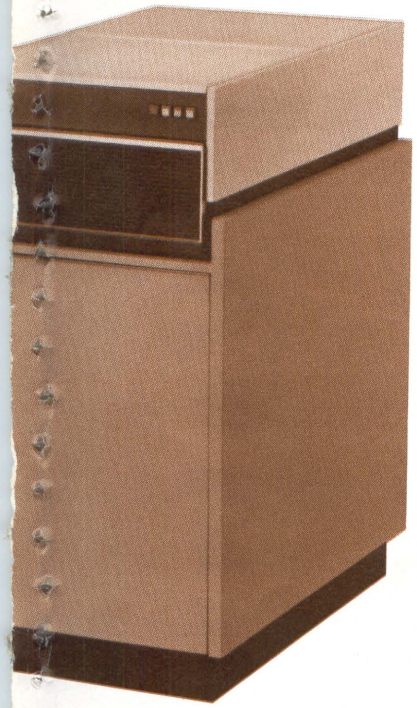

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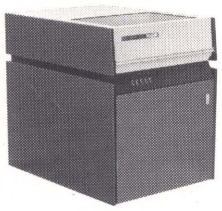

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Pseudorandom binary sequences in an alarm system can themselves disclose an attempt to compromise the system, without making the disclosure evident to the intruder. Furthermore, one sequence can protect many separate areas and their interconnecting lines, while still permitting authorized access and means of testing

Cyclic Sequence Generator Increases Security of Alarm Systems

Ramesh Krishnaiyer and John C. Donovan

Johnson Controls, Incorporated
Milwaukee, Wisconsin

The line of communication between an area protected by an alarm system and its central monitoring area is the most accessible and most vulnerable link in the system. It thus becomes the most difficult part of the whole security system to protect from compromise—that is, from logical intrusion as opposed to physical intrusion, and probably preceding physical intrusion.

Best protection would be an arbitrary signal, unknown to potential attackers, issued from the protected area at frequent intervals. This signal is compared with one identically generated at the central monitoring area; any detected dissimilarity activates an alarm.

An ideal line security system of this type would have two identical, truly random signal generators in the monitoring and secured areas, and would compare their outputs in the central monitoring area. However, this ideal system has a fallacy: two truly random generators cannot be identical.

Digital cyclic sequences that contain all possible combinations of some basic number of binary digits have certain well-defined properties. Since these properties are similar to those of random sequences in many respects, the sequences are called "pseudorandom." They can be generated by connecting various logic circuits to certain stages of a shift register. Identical pseudorandom sequence generators can be placed in the protected area and at the central monitoring area, yielding a basic single-zone line security system. These two generators' pseudorandom binary sequences are compared in the monitoring area; failure to agree results in an alarm (Fig. 1).

To prevent an intruder from knowing that he has been detected, the generator cannot simply be turned off when an intrusion is detected. If the intruder or an accomplice is monitoring the line, this would warn him that he has been detected. To prevent this, the alarm code should be indistinguishable from the pseudorandom security code.

The complementer serves this purpose in the system. It is activated by a signal from a physical intrusion detector, and inverts the generator's output. It also distinguishes between physical intrusion and attacks on the line.

Such paired identical generators are not limited to line security applications. They may also be used in time-division multiplexed supervisory systems or in spread communication systems. In critical decoding or error detecting applications, synchronized redundancy may be necessary.

Simpler alarm systems offer inadequate security. For example, a 2-conductor line that carries direct current to ring a distant bell can easily be cut or broken to prevent transmission of any signal. Closed dc-loop circuits that are sensitive to changes of 40% or more of line current provide reasonable security against simple direct assault on the line, but can be compromised without detection by more sophisticated attack. Newer alarm systems, based on the principle of a balanced-bridge circuit, place matched impedance modules in the protected and the monitoring areas. These impedances are usually complex and nonlinear, and are driven by elaborate waveforms that make undetected interference very difficult. Other systems using

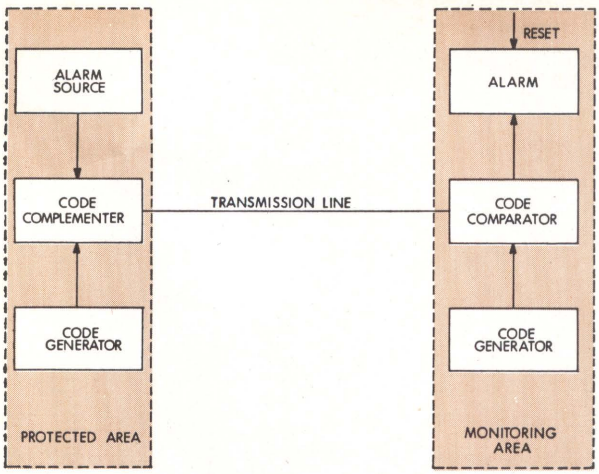


Fig. 1 Single-zone line security system. Outputs of two identical pseudorandom sequence generators are compared at monitoring area. If they are different, either the protected area or the communication line has been tampered with. Complementer assures that a signal is on the line even under intrusion, so that attacker won't know that he has been detected

interrogation circuits and signal conversion or superimposing ac pulses on a dc circuit complicate the attacker's problem, but are still defeatable. When tone signals are superimposed on the standard line circuits and multiplexing techniques are associated with an interrogation/response system, expert electronic knowledge and specific information about individual circuits are required to compromise the system. Thus, the problem of attacking the lines becomes more difficult for the intruder.

Nevertheless, there is no theoretical reason why these systems cannot be overcome. In fact, as a practical matter, no security system is completely invulnerable to compromise. Ultimate success or failure of an attack depends on the skill and strength of the attacker in proportion to the ingenuity and versatility of the defense.

Shift Register as Sequence Generator

A shift register with feedback generates a digital pseudorandom sequence of binary 0's and 1's. If feedback logic consists entirely of modulo-2 adders, output is a linear function of the inputs.[1] One of the binary digits, usually in the last stage, is added modulo 2 to the digits in one or more other stages, and this sum serves as the input to the next stage. If a shift register is connected with a feedback loop in this manner, output from any stage is a function of the initial state of the bits in the register and of the feedback connections. This output forms a pseudorandom digital sequence—"pseudo" because the sequence eventually repeats after a number of bit shifts that depends on the length of the shift register and the feedback connections. Certain sets of feedback paths produce the longest pseudorandom strings for the number of stages in the register; these "maximal length sequences" for a shift register with n stages consist of $2^n - 1$ digits, among which every permutation of n 0's and 1's, except the all-0's sequence, is found.[2]

Conversely, feedback connections of an n-stage pseudorandom sequence generator can be uniquely determined from 2n − 1 digits of its output sequence. Of these, n digits are an initial condition, and n − 1 additional digits uniquely specify which outputs are fed back. From these digits, feedback connections are found by solving n − 1 simultaneous equations. This provides a means of compromising security systems based on such sequences. However, for large values of n, solution of these simultaneous equations becomes extremely cumbersome, even when aided by a computer.

Nonlinearly generated sequences do not exhibit the regularity of their linear counterparts. They can be generated in a multitude of ways, but the generator cannot be reconstructed from a few elements of its sequences, as can a linear generator. This property makes a nonlinear generator extremely attractive as a code generator in a security system.

In general, the pulse rate at which a code generator is driven is much less than the rates with which electronic engineers usually work. Intervals of tens or even hundreds of milliseconds between pulses, with widths measured in milliseconds, are quite adequate. Therefore, neither circuit switching speed nor noise need be a consideration in designing the system. A slow bit rate also means that a particular pseudorandom sequence continues for a long real time before it repeats itself. This makes the sequence more difficult for a would-be attacker to determine—his first step in compromising the system.

However, there is a minimum speed limit, imposed by the need to keep the lines occupied. When the lines are busy transmitting signals, they cannot be cut into between pulses. Thus, the attacker has no means of substituting a recording of a spurious signal, to permit undetected physical intrusion or other mischief.

Multiplexed Security System

A multiplexed security system is a natural, cost-saving extension of multiple point-to-point systems. This system places identical code generators in several protected areas (Fig. 2). Each code generator produces an identical pseudorandom sequence (Fig. 3). All generators are multiplexed by a circuit that returns the first bit from generator 1 to the central monitor, then returns the second bit from generator 2, the third bit from generator 3, and so on up to the nth bit from generator n. Then the cycle repeats, returning the (n + 1)th bit from generator 1 to the monitor. Significantly, the code received by the monitor is identical to that produced by any individual remote code generator and by the reference code generator in the central monitoring area.

Thus, comparing the multiplexed code received from remote equipment with the reference code generated in the central monitoring area simultaneously protects the branch lines to the multiplexer as well as the

main trunk cable from the multiplexer to the central monitoring area. In a sense, security of each branch line is checked once in the same time interval during which the security of the main trunk line is checked n times.

Heart of the multiplexer (Fig. 4) is a simple ring counter or, equivalently, a shift register fed back on itself, driven by the same clock as the pseudorandom sequence generator. A single 1-bit circulates through the counter's n stages, whose outputs are connected to n 2-input AND gates. These gates steer the data lines from the n zones through an OR gate to the main trunk line. As the gating 1-bit progresses through the ring counter, each line from the remote code generators is connected in turn to the central monitoring facility.

Similarly, at the central monitor, a ring counter containing a single 1 drives AND gates, which in turn drive the indicating lights (Fig. 5). The second input to each AND gate is the output of the code comparator circuit. An exclusive OR logic gate, the comparator produces a logical 1 output only when the two codes from the reference and the trunk cable are different. This output is steered by ring counter and AND gates to the appropriate alarm indication. In practice, power line drivers are required, and latch circuits with manual reset prolong an alarm indication until it has been acknowledged.

Several improvements can be made to enhance performance of basic multiplexed systems. For example, a latching circuit or time delay could hold an alarm condition on at the source long enough for at least two cycles of complemented codes to be transmitted. This eliminates the possibility that an alarm might be missed between scans.

Also, several successive code bits could be returned from each zone generator before progressing to the next zone. This would tend to confirm the existence of an intrusion at a zone and reduce momentary false alarms. For example, if four successive bits in the pseudorandom code sequence were returned from each zone, an alarm would be indicated only if a majority of the bits were in disagreement. Exactly how many bits could be ignored as noise without reducing the system's effectiveness remains to be determined.

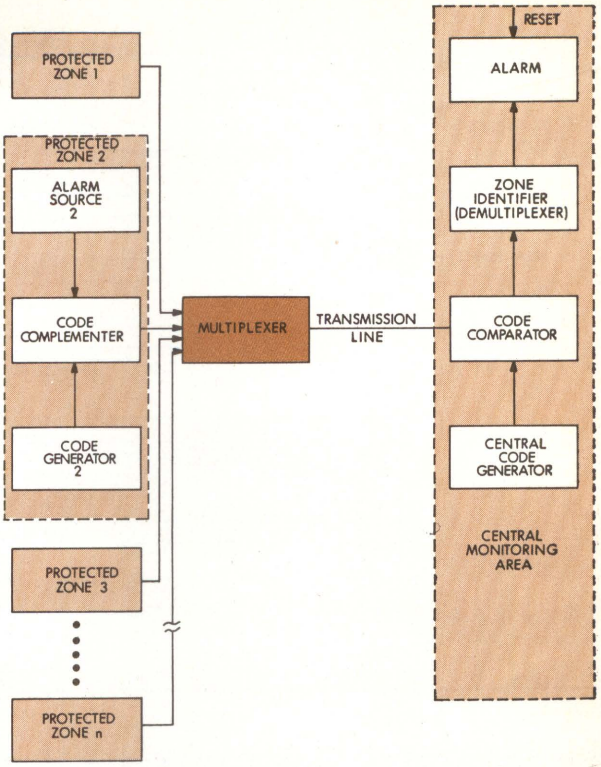


Fig. 2 Multiplexed security system. Identical code generators in several protected areas produce bit streams that are compared at monitoring area as in single-zone system. Individual protected areas are checked less often than main transmission line

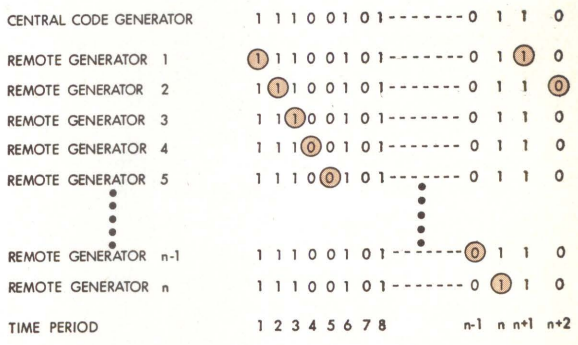


Fig. 3 Interleaving of multiplexed code. All generators produce identical bit streams, but only one of n bits from any particular generator goes to central area. Nevertheless, central monitor receives the same sequence it would receive from a single protected zone

Authorized Access and Alarm Test

To permit access by authorized personnel to a secured area, an access/secure control unit outside the secured area is necessary. This unit has a locked access/secure switch; in the "access" position, when matched by a similar switch at the monitoring facility, it overrides the alarm indication. To relay the status of the remote access/secure switch to the monitoring area, the multiplexing approach described earlier can be used. Instead of monitoring four separate zones with a time-interleaving scheme, a single zone is monitored in a 4-point scan cycle that is looked upon as four time intervals. In three of these intervals, a bit from the pseudorandom sequence is returned to the monitoring area. In the fourth time slot, the status of the access/secure switch is returned as a 1 or a 0, and is compared with the status of the corresponding switch at the monitoring area. The code generator should be clocked during all four time intervals, and its output inhibited during switch-status transmission. This serves to compound the problem of the system attacker, since he now has only three-fourths of the sequence to work with.

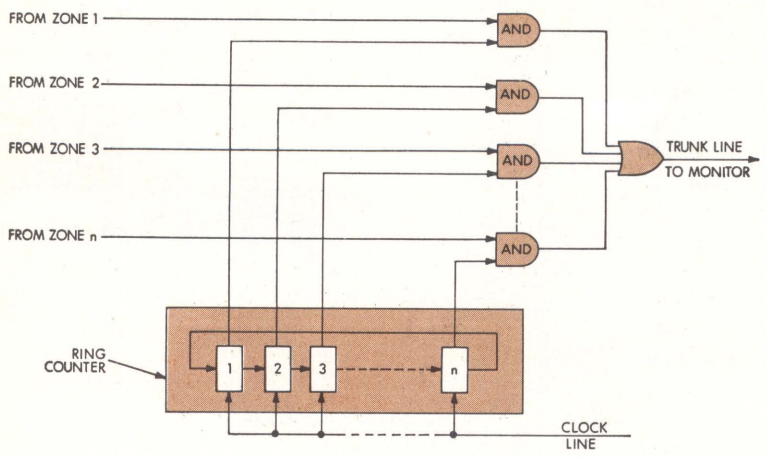


Fig. 4 Multiplexer. Ring counter is synchronized with code generator, admitting successive bits from different protected areas to trunk line. Shift register containing a single 1-bit may be used in place of counter

The number of time intervals in a cycle can be expanded simply by employing longer ring counters; this is analogous to adding zones to the multiplexing system. By expanding the number of time intervals, other types of data can be brought back for display—for example, the transfer to standby power.

As described thus far, the multiplexed system still suffers from a major omission: a shortage of signal channels. For example, a single system clock at the central monitoring point is necessary to maintain system synchronization. This requires information to be transmitted over the main trunk line in a half-duplex mode—that is, in both directions on the line, but not at the same time. Clock pulses sent from the central area are interrogation pulses; individual zones respond to them with the next bit in the code sequence.

With this synchronization scheme, however, interruption of only one sync pulse will cause the system to indicate a virtually continual alarm. This vulnerability also implies a need for some resetting capability, so that all parts of the system start from the same state at the same time. One possibility for a reset pulse would be a pair of pulses in the same interval as a single clock pulse.

To test the alarm system, an intrusion simulator must be activated in the secured area. In the high-security point-to-point system, this function can be met by extending the concept of single and double pulses for clock or reset to four types of signals. One pulse is taken as a clock pulse; two pulses are interpreted as a remote test command; and three equally spaced pulses in the regular clock interval signal a restart operation; while four pulses compose a reload signal.

Suppose the reset command resets all generators to the same starting word—for example, a word of all 1's. Since the generators are identical, they all produce the same bit sequence. This constitutes a vulnerable point in the basic concept. An attacker could, for example, create a synchronization problem, causing the system to be reset. He could then record the pseudo-random sequence for whatever length of time access to the protected area was needed. After desynchronizing the system again, he could cut the alarm lines and connect his recorded sequence to the lines in response to the reset signal, thus gaining undetected access to the protected area.

This example, of course, assumes the most rudimentary implementation of the concept; further, it neglects the degree of security that the presence of a remote test capability adds to the system. However, it does show the vulnerability that arises from using an inadequate resetting method.

A more sophisticated system would have two code generators of the same size in both the monitoring and the protected areas. One, the working generator, produces the actual sequence which assures the line's security. The other, called a reset generator, also produces a sequence, but in response to a restart signal provides only a new starting word to the working generators. When the reset generators are reloaded, it need not be with all 1's, but rather with a sequence of 1's and 0's arbitrarily selected with toggle switches or read from punched cards. The only restriction is that the generator not be loaded with all 0's. A different randomly chosen sequence could be reloaded with every restart. If reset and working generators have different feedback connections, or if the feedback connections are made readily changeable, the working generator's sequence will skip around greatly.

Although these reset capabilities are not necessarily optimum, they do illustrate the capability and flexibility of some concepts that may be incorporated into

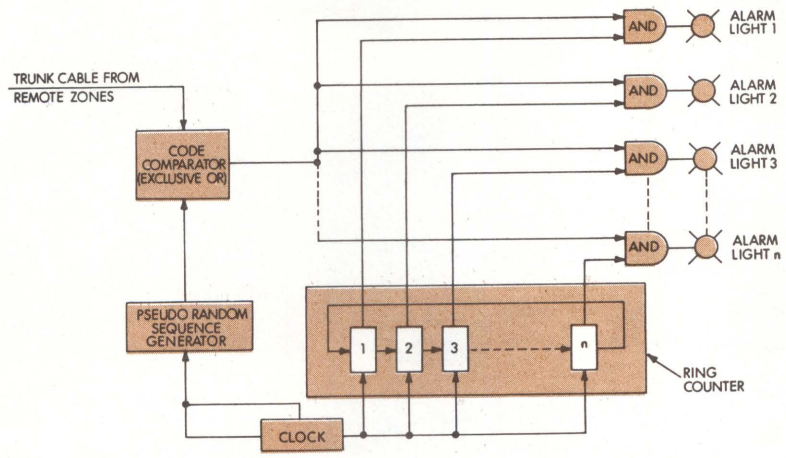


Fig. 5 Alarm indication. Code comparator is an exclusive OR, which has an output whenever the signals from the trunk line and the pseudorandom sequence generator are different. Ring counter synchronized with generator identifies source of errant pulse, and causes alarm light to turn on, indicating place of intrusion

a high security, point-to-point system. Others which could be incorporated into the system include blanking or skipping an occasional bit in the pseudorandom sequence to complicate the decoding process, periodically complementing a code bit or inserting an arbitrary 1 or 0 bit, or switching between two working generators, all done periodically or pseudorandomly as dictated by a third generator.

Defeat Techniques

No security system is inviolable. Given the time and intelligence to accumulate the necessary knowledge and skill, an attacker can always devise a method of compromising any security system. Thus, the means by which an intruder may attempt to overcome a system must be considered.

One approach to compromising the line security concept has already been described—to record a portion of the sequence, create a synchronization problem, and play back the recorded sequence in response to the reset command. This approach is foiled by resetting the system to a new starting point after a synchronization problem.

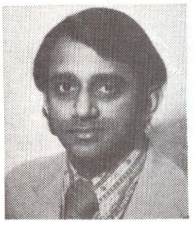
Another approach assumes that the attacker has a code generator identical to that in the secured area. He must identify which of the possible sequences is being generated. In essence, he must decode the sequence.[2] Randomly selecting one of several different maximum-length feedback connections wired on the card is one way to thwart an attempt to trace the generator's connections. Another method is to restart the main generator with a new set of codes from an auxiliary generator as often and as arbitrarily as possible.

This leads to nonlinear generators and nonlinear operations on linear sequences, as suggested previously. Using nonlinear shift-register generators will virtually eliminate any vulnerability to sequence decoding such systems may have.

In conclusion, it can be stated that the pseudorandom code-comparison concept of securing transmission lines does represent an improvement over the state-of-the-art in line security.

References

1. S. W. Golomb, *Shift Register Sequences*, Holden-Day, Inc, 1967
2. R. Krishnaiyer and J. C. Donovan, "Shift Register Generation of Pseudorandom Binary Sequences," *Computer Design*, Apr 1973, pp 69-74



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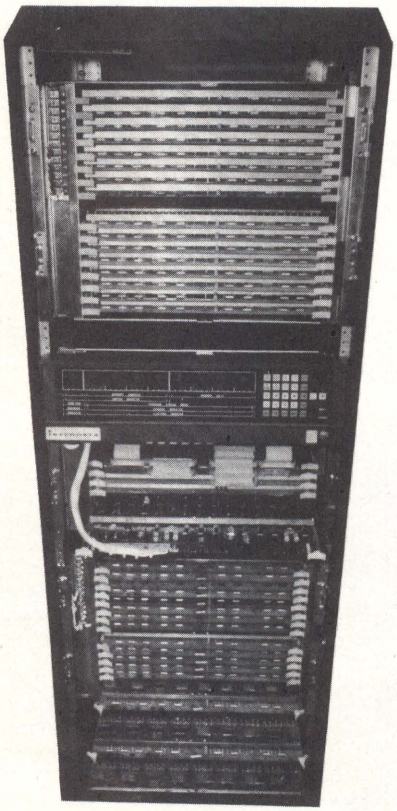

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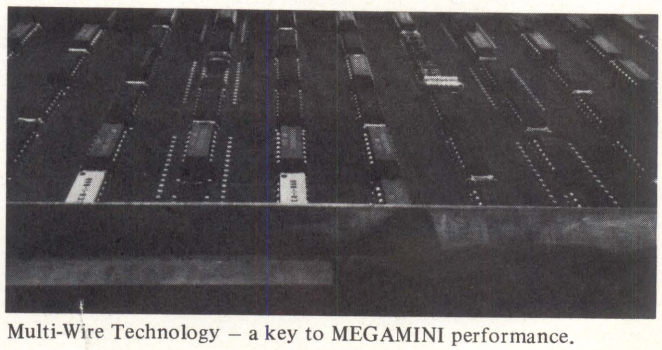

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Floating Point Add	2.3	6.1	2.4	8.25	5.5
Multiply	3.0	9.1	2.3	11.25	7.2
Divide	5.35	23.3	8.9	12.25	7.9
HARDWARE I/O	Yes	Yes	Yes	No	No
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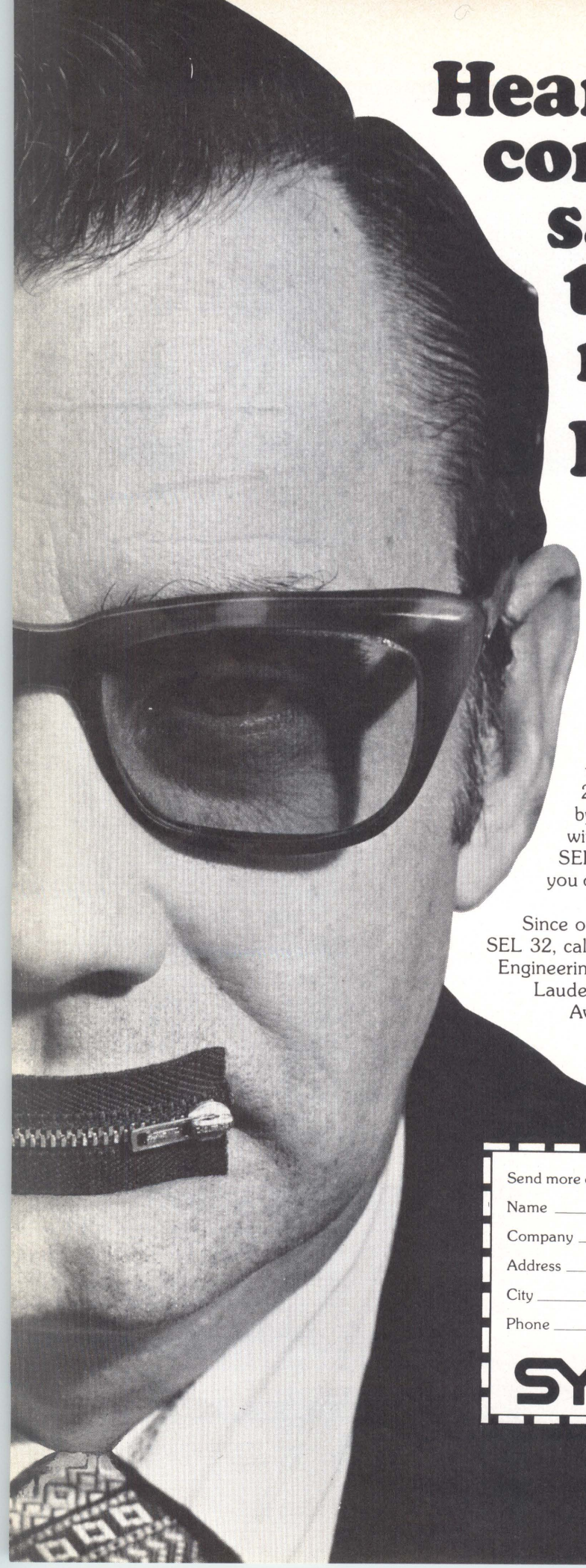

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Well-chosen signal names and convenient mnemonics are invaluable in helping testers, programmers, and servicemen understand a digital system. Here is an orderly technique for devising mnemonics that are clear and consistent—and really do help in remembering

Signal Names Help System Understanding

Ware Myers

Xerox Corporation
Inglewood, California

There is no substitute for a thorough understanding of a digital system—at least by most people engaged in its design, test, and repair. To promote this understanding, there is no substitute for the intelligent naming of signals and derivation of mnemonics.

Self-contained verification programs can pinpoint many failures and relieve the user or field engineer of much of the necessity for detailed troubleshooting based on system understanding, as can diagnostic programs directed from an external computer. However, someone still has to locate faults that escape the verification or diagnostic program, and someone has to repair the trouble.

No automatic program has yet been written that can completely cover every possible malfunction in a complex computer-based digital system. Even at the printed circuit (PC) board level, automatic production testing is seldom completely diagnostic, if only because modules are pin-limited and cannot bring out every significant signal.

Both in test and in the field, some troubleshooting by people is inescapable. To hunt trouble effectively, the people need some understanding of data signal movements and control signal flow.

System Growth

In small first-generation logic systems, a human memory could remember most signal flow patterns. In fact, except in the early computers, signals were not named and mnemonics were unknown. The engineer worked directly from pin and wire numbers and schematics, not logic diagrams; he had no memory aids.

Today's large-scale integration has greatly expanded system size, increasing by an order of magnitude the logic that can fit on a single PC board, and multiplying the load on the memories of individuals who must understand the system.

Intelligently named signals are a great help to these individuals. Carefully named system functions lead to meaningful signal names, and form the basis for easy-to-understand mnemonics—short abbreviations that assist memory. This efficient nomenclature enables users to take hold of the system much more rapidly than with less well-organized signal terminology. In this way, well-designed mnemonics contribute significantly to effective troubleshooting. They also take less time to write, especially repeatedly, and occupy less space on the logic diagrams than fully spelled-out names.

Moreover, these same easy-to-use mnemonics help development personnel, and speed up test-equipment design, test programming, and design of interfaces to related equipment. Good terminology makes technical manuals much easier to understand.

Signal Characteristics

Various approaches have been employed to create signal names and mnemonics; the predominant scheme has been to name the signal after what it does, for example, RESET. Less common is paraphrasing the logic operation embodied in the signal; for example, A00 +

A08 indicates the output of an OR gate that is driven by two bits from a register—perhaps sign bits of two bytes. At other times, a signal has been named for its electrical or locational source. These approaches, although useful, do not incorporate as much valuable information as they might.

Ten characteristics of a signal are useful to persons who need to understand the logic:

(1) The signal's relationship to a major function at the block diagram level

(2) Its function—that is, what the signal does; eg, data, control, addressing

(3) Its type—such as clock, flip-flop output, or power supply level

(4) Its state—that is, true or false, for the active condition

(5) Its source—either a page of the set of logic drawings or a PC board location

(6) Its destination—again either a page or a location

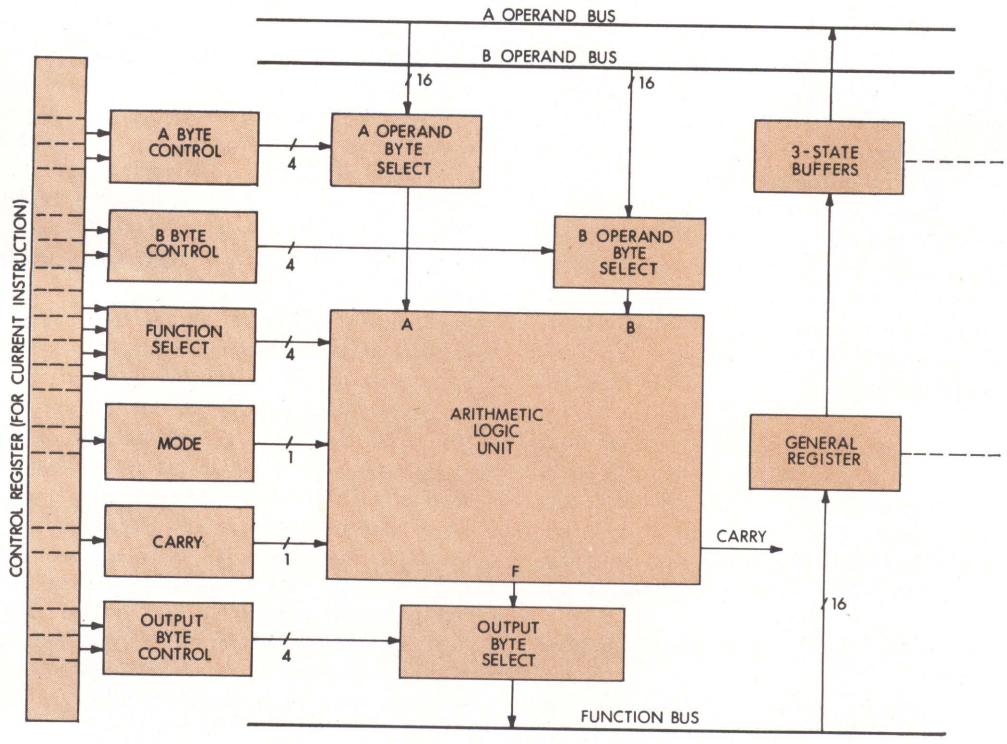
(7) Its actual or possible loading

(8) Its timing or synchronizing relationship to other signals

(9) The stage delays it incorporates relative to a zero time—such as a basic clock

(10) Its current-carrying limitations

Obviously, a very long and complex mnemonic would be required to embody all of this information. Such a mnemonic would be self-defeating, for mnemonics should be easy to remember and interpret. Fortunately, some of these 10 characteristics can be made available on other documentation. For example, signal sources, destinations, and loading can be included in computer-prepared wire lists, while drawing-page sources and destinations can be added to the logic diagrams. That leaves a reasonable amount of information to be carried by the relatively brief mnemonic, having no more than six parts, and often less.



Framework for mnemonics. A simple computer system has these components upon which a well-organized mnemonics system can be based

Mnemonics

The six parts of a mnemonic are state, block-diagram relationship, function, data-bus line identification, signal type, and stage delay.

State

The mnemonic's initial letter signifies the *state* of the signal. If this letter is N, for "not," the signal at that point is logically false, negated, or inverted. If this N is omitted, the signal is in the logically true form. Because N is used in this way to indicate negation, it should not be used as the first letter of a mnemonic itself to mean, perhaps, "next" or "numeric."

Which level is logically true and which false, of course, depends on whether the system uses the positive- or negative-logic signal-level convention. However, in a system that generally uses positive logic (where the higher of two voltage levels represents the true logic state), it is sometimes convenient electrically to report action in some types of lines (such as interface lines between different units) by making the line false; ie, an interrupt would be signaled by pulling the interrupt line to ground. In this case, the mnemonic assigned to the interrupt line should be preceded by N.

Both the signal name and its mnemonic should correspond to the signal's true state. For example, a true (binary 1) output of a memory cell should be assigned a mnemonic in the true form, as MM01L. On the other hand, if the cell's output has arithmetic or logical significance in the system when it is false (binary 0), its assigned mnemonic should then be NMM01L. Of course, the signal itself in true form could be either 1 or 0, depending on the content of the memory cell—as it could also be in false form.

When preceded by N the mnemonic should represent the exact logical inversion of the signal represented by the same mnemonic without the N. If a signal's inversion also gates another term to the original signal, the new output should be assigned a different mnemonic.

Signal names that embody an inherent negative, such as DISABLE or INHIBIT, sometimes require mental somersaults, and are therefore naturally difficult to decipher. If possible, such signal names should be made inherently true; eg, ENABLE can be substituted for NDISABLE, and NENABLE for DISABLE.

Block Diagram

Following the negation letter, the first few characters (no specific limit need be set) of the mnemonic indicate the signal's relationship to system or unit block diagram. For instance, MM might generally identify a signal as part of a main memory. This assumes, of course, that a block diagram of the entire system was prepared before detailed logic was designed. Major system functions can usually be identified by a combination of two or three letters. Related signal names and mnemonics can be derived from the names of principal elements.

TABLE 1

Mnemonics

Mnemonic	Subsystem function
A00T to A15T	A Operand Bus
ABY0L to ABY3L	A Byte
AL00G to AL15G	Arithmetic Logic Unit
CR00F to CR31F	Control Register
F00T to F15T	Function Bus
GR2O00F to GR2O15F	General Register 2
FS0L, FS1L, FS2L, . . .	Function Select

If a large system involves a number of designers, signal or function names of all their block diagrams should be coordinated. For example, if several parts of the system have memories, they can't all be "main memories," even if that name describes their functions. They can be called by various synonyms, however, such as "general memory," for which GM would be a mnemonic.

A sample block diagram (Figure) represents the arithmetic logic unit (ALU) and several related elements of a 16-bit computer, and shows how mnemonics can be related to system diagrams.

From the two operand buses, two words or portions thereof are presented to respective ALU inputs, whose outputs are similarly routed to the function bus. These routings are specified by certain bits of the current instruction, which is held in the control register. In the ALU, which is a combinational logic network, one of 16 operations is performed on these inputs, as specified by four select inputs. These operations are arithmetic or logical, as specified by the mode bit, and may or may not utilize an input carry, both controlled by appropriate bits of the current instructions. At the end of the operation, the contents of the function bus are clocked into one of several general registers not shown in the diagram. From this register, the result is returned to the operand buses for further processing.

Major subsystem functions can be represented by abbreviations, such as those in Table 1. Using mnemonics such as these, a user with only a cursory grasp of the system, and with only a minimum load on his own memory, can at least generally locate the signal in the system and more often than not have some idea of what it is doing.

Function

The next few characters, following the block diagram characters, indicate the signal's function—what the signal does, such as data or control. For example, CS might represent chip select. Several signals are usually

related to a major block, and are distinguished from each other by means of these function mnemonics.

Parallel Lines

Data normally involves a number of parallel lines, buffer outputs, and register outputs, usually grouped into buses. Each line in a bus can be identified by a 1- or 2-digit number, following the block and function characters. Ten or fewer can be labeled with 0 through 9, while 16 lines can be identified either by a single hexadecimal character, 0 through 9 and A through F, or by two digits, 00 through 15.

When numbering, the most significant line is subject to a conflict of conventions. In ordinary arithmetic notation, a number is read from left to right, so that the digit on the left is the most significant one. Its corresponding line is usually numbered 0. On the other hand, in hardware, a counter, for example, is made from a series of flip-flops drawn with the signal flow from left to right, representing a carry propagation. This makes the flip-flop on the left the least significant one. Nevertheless, it is usually labeled 0, or sometimes 1.

Somewhere in the system, between hardware counters and arithmetic buses, line numbering must change from one convention to the other. To minimize misunderstanding, appropriate lines should be labeled MSB or LSB on logic diagrams or logic equation listings, particularly at the point of changeover from one convention to the other.

TABLE 2

Signal Types

Identifier	Signal type
A	Analog signal
B	Bus, usually one of a set of parallel lines
C	Clock
D	Heavy-duty drive capability
F	Flip-flop (clocked) output
H	Shield
K	Relay
L	Logic level
O	Open-collector output
P	Pulse of specified width or period
R	RS flip-flop (not clocked) output
S	Switch, stepping switch
T	Three-state output
V	Voltage, power supply level, including ground

Signal Type

The mnemonic's next-to-last character, which is its last alphabetic character, signifies the signal's type or class. (A number of examples are listed in Table 2.) This letter helps the user observe the signal with an oscilloscope or other instrument. For this purpose, frequency, period, pulse width, voltage levels, clock relationships, and type of output need to be known so that the observation can be rapidly set up and results intelligently interpreted.

For example, to put a signal on the oscilloscope, the signal's time scale must be known. Frequently, this time scale is related to a clock. Using the clock or clock-related signal for synchronizing may show the unknown signal in time relationship to other pertinent signals.

Digital signals use clocks in two ways. In one of these, an oscillator generates the maximum-frequency signal, which is counted down to lower frequencies for slower purposes. If the basic clock period is, for example, 200 ns, the mnemonic might be S200NSC, meaning "System 200 Nanosecond Clock." Clocks derived from the basic clock might then be termed S400NSC, S1.6USC, S6.4USC, and so on. Alternatively, if the basic clock period is taken as unity, it would be labeled S01C. Then the derived clocks with longer periods would be labeled S02C, S08C, and S32C.

The second kind of clock establishes a period long enough to execute all phases of a single instruction, dividing this period into clocked phases during each of which one major step of a single instruction is carried out. These phases might be labeled SP1C, SP2C, . . . , SPnC, meaning System Phase 1 Clock, and so on.

The suffix P signifies a pulse with either a specified period, a specified pulse width, or both. The output of a one-shot, for example, may be either a positive or a negative pulse of defined width, specified in the mnemonic, S100NSP.

Suffixes such as L for "level" and G for "gate" permit mnemonics for similar but not identical signals to use the same beginning and middle characters. In general, these suffixes suggest a signal that changes between true and false, in a less regular pattern than a clock or a pulse.

Outputs of switches (S) and relays (K) in digital systems are usually at standard logic levels. However, they differ from gate outputs in that they operate more slowly, and they may bounce from one level to the other for several milliseconds before settling at the ultimate state.

Although a flip-flop output exhibits the same logic levels as an output from combinational gating, it should be distinguished from other outputs by a suffix letter, alerting the user to the fact that he is dealing

with a bistable element, or a 1-bit storage element. As many types of flip-flops, clocked and unclocked, may be distinguished by suffix letters as seem helpful. As a minimum, the letter F can identify a clocked flip-flop, which changes state on the leading or trailing edge of the clock, and R can identify an unclocked set-reset flip-flop.

In current technology, at least four types of bus lines are common:

(1) Standard TTL or DTL logic levels, with normal capability to drive a few similar circuits; the suffix B, for bus, identifies these levels

(2) Standard TTL or DTL logic levels, with capability to drive many circuits; the suffix D, for driver, identifies these levels

(3) Open-collector outputs, identified by the suffix O, for open—usually one of several connected to a single line, with a single pull-up resistor. If one of the outputs connected to the line is low, the line itself is low; but if all the outputs are high, the line remains high—the wired-OR function in negative logic

(4) Three-state outputs, identified by the suffix T, have two active states compatible with TTL or DTL circuits, and a third state that presents a very high impedance to the line. Many 3-state outputs can be connected to one bus; when in the high-impedance state, they do not significantly load the one output that can be active at any one time. Like the open collector, this circuit provides the negative wired-OR

Some examples of mnemonics for individual bus lines are A00B, for line 00 on bus A; B02D, for driven line 02 on bus B; D15T, for data line 15 on a 3-state bus; F37O, for function 37 on an open-collector bus; and I05B for input 05 on bus B. The last three of these illustrate how assigning meanings to the initial letters provides more information about the bus than merely labeling them in alphabetic order.

Analog inputs from external world to digital system can be labeled with the suffix A, as a flag to the user. This reminds him that these signals may not be observable on the same voltage scale as the standard logic levels and that synchronizing to them may also be difficult.

Voltage

A mnemonic terminating in V indicates a power supply level, including ground; for example, P05V means +5 V, M15V means −15 V, and G00V means ground or 0 V. An initial character P may stand for either plus or positive, but M signifies a minus voltage, because the use of N for negative is proscribed.

Several parallel printed-circuit lines may be necessary for power levels and for ground returns, and sometimes for widely used logic signals, such as clocks. Each separate but parallel line must be identified by a unique mnemonic, capable of being recognized by automatic wirewrap machines. This identification is accomplished with a hyphen followed by a suffix number added to the mnemonic.

Stage Delay

A non-hyphenated number, following the signal letter, indicates the number of stage delays from the basic signal. These delays, arising in buffers and inverters following a timed element, do not change the logical meaning of the signal, but could be of troubleshooting interest. However, if only the original signal and its first inversion are present, the suffix numbers are redundant; basic mnemonics, such as M00L and NM00L, are clear enough by themselves.

Not all signals have or need names or mnemonics. In general, a signal should be given a mnemonic if anyone other than the original designer—test-equipment designer, test programmer, interface designer, manual writer, or service engineer—is likely to refer to it. In particular, inputs and outputs of flip-flops and one-shots, whether discrete or integrated, should be labeled, because they often appear on timing diagrams.

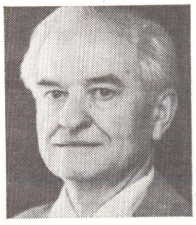
On the other hand, two general classes of signals that need not be named are unused inputs or outputs, and signals for which the mnemonic is obvious. Examples of the latter are the output of an inverter, when the input is labeled, or the false output of a flip-flop, when the true output is named. Omitting these obvious mnemonics saves drawing space and drafting time.

Common Sense

No set of rules can avoid the necessity for the designer to exercise good judgement or for the user to take thought in interpreting the significance of signal names. The art of choosing mnemonics cannot be consigned to a computer program.

The vast number of components, connections, and detailed functions in the average digital system do not easily arrange themselves into an overall block diagram which conveys meaning to the human mind. Much subsidiary information necessarily has to be omitted. General functions broadly representing these details have to be built up and then related to each other in ways that make sense to the block-diagram user.

Similarly, meaningful mnemonics are not necessarily evident from the block diagram. The whole task of naming signals is difficult, but the more meaningfully it is done, the more quickly users can understand the system and solve problems.



Ware Myers is an engineer/writer in the systems engineering group of the Data Systems Div of Xerox. He has earned a BS degree from Case Institute of Technology and an MS degree from the University of Southern California.

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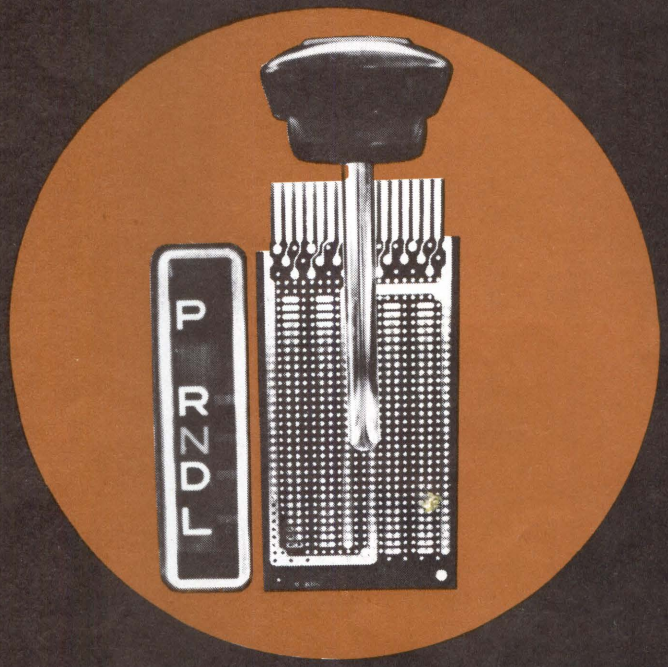

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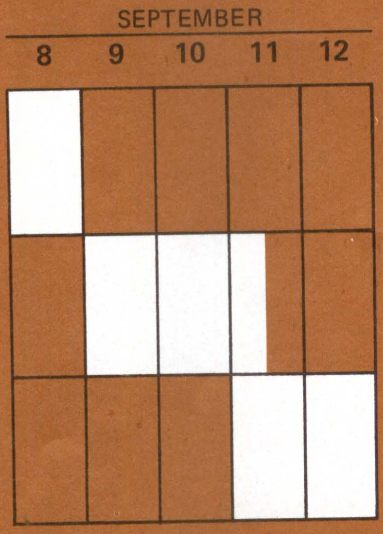

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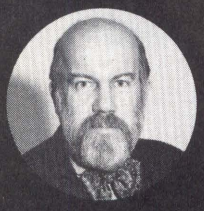

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U.S. Naval Ship Engineering Center

Registration Chairman

Mr. Peter Fodor
Control Data Corporation

fall compcon 75

new this year...

a choice of two pre-conference tutorials

9:00, MONDAY, SEPTEMBER 8, 1975

Rather than the customary single tutorial offered the day before the conference proper, two full-day sessions running in parallel are scheduled. Both are subjects closely related to the main conference theme of "Making Computers Easier to Use," as well as being directly relevant to the First International Conference on Software Engineering which immediately follows Compcon 75 Fall.

PROTECTION OF INFORMATION IN COMPUTER SYSTEMS

Drs. David D. Clark and David D. Redell
of MIT's Project MAC

STRUCTURED PROGRAMMING

Dr. Victor R. Basili
University of Maryland at College Park
Mr. Terry Baker
IBM Federal Systems Center

PROTECTION OF INFORMATION IN COMPUTER SYSTEMS

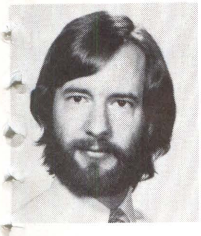
COURSE OUTLINE:

- Basic principles of information protection, including considerations surrounding the study of protection and technical underpinnings.
- Separation of addressing and protection, the capability system, the access-control list system, protecting various types of objects, and protected objects and subsystems.
- The state of the art, current research directions, and concluding remarks.

INSTRUCTORS:

David Clark

A research associate, Dr. Clark has been with the Computer Systems Research Division of Project MAC for the past seven years. During this period he has contributed to the design of many parts of the Multics operating system, a system with advanced features for protection of information. Dr. Clark received his BS from Swarthmore College in 1966 and his MS and PhD from MIT in 1968 and 1973.



David Redell

Dr. Redell, also affiliated with Project MAC, joined the faculty of the Department of Electrical Engineering and Computer Science at MIT in 1974. His current research interests include operating systems, protection, machine architecture, and system programming languages. Dr. Redell received his BA, MA, and PhD degrees from the University of California at Berkeley.

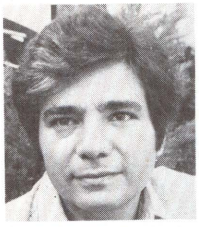
REGISTRATION FOR TUTORIALS AND CONFERENCES ON LAST PAGE

STRUCTURED PROGRAMMING

COURSE OUTLINE:

- Introduction to the major ideas of structured programming, their theoretical and practical foundations.
- Development of a major application program system, together with the quality and productivity results experienced.
- Detailed presentation of the development of a single program, stressing the top-down evolutionary character of the process.
- Concluding summary, the advantages and disadvantages of SP ideas as observed through their installation use by a large programming organization.

INSTRUCTORS:



Victor Basili

Dr. Basili has been on the computer science faculty at the University of Maryland at College Park since 1970; his major interests are the design, modeling, and implementation of programming languages. His major language development efforts have been the graph algorithmic language GRAAL and the SIMPL family of programming languages and compilers.

Dr. Basili received a BS degree in mathematics from Fordham College in 1961, an MS degree in mathematics from Syracuse University in 1963, and a PhD in computer science from the University of Texas at Austin in 1970.

Terry Baker

Mr. Baker, manager of the NSDG Development in the Federal Systems Center, is responsible for the development of a software system for newspaper production for a consortium of eight major newspapers. With IBM since 1956, he has held numerous positions; most recently he was manager of the Development Tools Department, responsible for the guidelines, tools, and support necessary for the introduction of programming support libraries, structured programming, top-down programming, and chief programmer teams at the center.

Baker received his BS in mathematics from Yale University and his MS in applied mathematics from Harvard University.

BOTH TUTORIALS START
9:00 AM, MONDAY, SEPTEMBER 8, 1975

TUESDAY September 9, 1975

9:30 SESSION 1: KEYNOTE SESSION

Opening Ceremony

Richard E. Merwin, COMPCON 75 FALL General Chairman
Lynn Hopewell, COMPCON 75 FALL Program Chairman
Stephen S. Yau, President, IEEE Computer Society

Keynote Address

The Hon. Barry Goldwater Jr., U.S. House of Representatives

TUESDAY MORNING (Parallel Sessions)

11:00 SESSION 2: HARDWARE

Chairman: Joseph Wylen, Burroughs Corporation
"A RATIONALE FOR RANDOM TESTING COMBINATIONAL DIGITAL CIRCUITS," John J. Shedletsky, Stanford University
"DESIGN OF FAIL-SAFE SYNCHRONOUS SEQUENTIAL CIRCUITS BY EXPLICIT STATE TRAPPING," Alan M. Usas, Stanford University
"ARITHMETIC ERROR CORRECTIONS IN BCD SYSTEM," C. K. Liu and T. L. Wang, Bell Telephone Laboratories

11:00 SESSION 3: INNOVATIVE APPROACHES TO SYSTEMS AND HARDWARE

Chairman: Jack Lynch, Burroughs Corporation
"DISTRIBUTED PROCESSOR DESIGN FOR AVIONIC APPLICATION," Michael Moore, Air Force Avionics Lab, Wright-Patterson A.F.B.
"A HARDWARE INDEPENDENT RESOURCE SHARING MECHANISM," George Cowan, Burroughs Corporation
"1980 ARCHITECTURE FOR LARGE SCIENTIFIC PROBLEMS," Joseph Wirsching, Consultant
"A MODULAR APPROACH TO THE DESIGN FOR A SYSTEMS CENTRAL PROCESSING CENTER: PROS & CONS," Daniel Schutzer, Defense Communications Agency

11:00 SESSION 4: PRIVACY AND SECURITY

Chairman: Michael Munter, General Services Administration
"HEW IMPLEMENTATION OF THE PRIVACY ACT OF 1974," Lee Wouters, Department of Health, Education, & Welfare
"HOW TO IMPLEMENT SYSTEMS WHICH COMPLY WITH THE PRIVACY ACT OF 1974," Robert Goldberg, Harvard University
"TECHNICAL PRINCIPLES OF COMPUTER SECURITY," G. Popek, U.C.L.A.

TUESDAY AFTERNOON (Parallel Sessions)

2:00 SESSION 5: MICROPROGRAMMING

Chairman: Gary L. Kratz, IBM
"A MICROPROGRAMMED ENVIRONMENT FOR A SOFTWARE DEVELOPMENT SYSTEM," Charles W. Flink II, Naval Surface Weapons Center/Dahlgren Laboratory
"MPL-85: A HIGH-LEVEL MICROPROGRAMMING LANGUAGE COMPILER," Carol J. Lane and M. R. Ito, University of British Columbia
"EMULATING THE DATA GENERAL NOVA OF THE PDP-11/40: A CASE STUDY," P. Drongowski, S. Fuller and Tom Dopirak, Carnegie-Mellon University

2:00 SESSION 6: ARE BIG MACHINES NECESSARY?

Chairman: Mario J. Gonzalez, Jr., Northwestern University
"CENTRALIZED OR DECENTRALIZED COMPUTING – OR MAYBE SOME OF BOTH?" R. L. Ashenhurst, University of Chicago
"ARE MINICOMPUTERS SUITABLE FOR LARGE SCALE SCIENTIFIC COMPUTATIONS?" Harry F. Schaefer, University of California, Berkeley
"WHY NOT A MINI IN EVERY CUPBOARD?" David P. Jasper, Control Data Corporation

2:00 SESSION 7: OPERATING SYSTEMS

Chairman: Dr. John Benoit, The MITRE Corporation
"CONSTRUCTION OF PRIMITIVES FOR A MULTIPROCESS ENVIRONMENT," C. R. Hollander, Stanford University
"DYNAMIC SCHEDULING OF TASKS REQUIRING MULTIPLE PROCESSORS," A. Thomasian and A. Avizienis, U.C.L.A.
"A COMPARISON OF MEMORY ALLOCATION STRATEGIES FOR PARALLEL PROCESSING SYSTEMS," C. V. Rammamoorthy, University of California, Berkeley, and David Pessel, University of Rochester

4:00 SESSION 8: MEMORIES

Chairman: Harry D. Frankel, Immigration & Naturalization Service, Department of Justice
"MAGNETIC BUBBLE MEMORY INTERFACING," J. Egil Juliussen
"ASSOCIATIVE-SEARCH BUBBLE DEVICES FOR CONTENT ADDRESSABLE MEMORIES," S. Y. Lee and H. Chang
"SYMBOL STRING PATTERN RECOGNITION BY MAGNETIC BUBBLE DEVICES," K. Takahashi and H. Kohara
"THE DESIGN OF FAULT-TOLERANT COMPUTER MOS MEMORIES," Len Levine and Ware Myers, XEROX Corp.

4:00 SESSION 9: STANDARDS

Chairman: Gerald Schutz, Department of Transportation
"INTERNATIONAL DATA COMMUNICATION STANDARDS," John L. Wheeler, XEROX Corporation
"OVERVIEW OF INFORMATION PROCESSING STANDARDS," Vico E. Henriques, CBEMA
"DATA LINK CONTROL PROCEDURE STANDARDS," David E. Carlson, Bell Telephone Laboratories

4:00 SESSION 10: STRUCTURED PROGRAMMING: AN EVALUATION

Chairman: Victor R. Basili, University of Maryland
"SOFTWARE DEVELOPMENT PROCESS REVISIONS," Robert McHenry, IBM
"A CASE STUDY IN STRUCTURED PROGRAMMING: REDESIGN OF A PAYROLL SYSTEM," Edward Yourdon, Yourdon Inc.
"PROGRAMMING MEASUREMENT IN A TIME OF CHANGE," J. W. Patterson, IBM

WEDNESDAY September 10, 1975

WEDNESDAY MORNING (Parallel Sessions)

9:00 SESSION 11: COMPUTER NETWORK SOFTWARE

Chairman: Nathan Teichholtz, DEC
"COMPUTER NETWORKS CAN BE FRIENDLY," Shane Dickey, Hewlett Packard Data Systems
"A USER-ORIENTED MINICOMPUTER NETWORK," William J. Lennon, Northwestern University
"DISTRIBUTED COMPUTING: A MODULAR APPROACH TO COMPLEX SYSTEMS," Nathan Teichholtz, DEC

9:00 SESSION 12: MEDICAL APPLICATIONS

Chairman: Thomas L. Lewis, National Institutes of Health
"AN INTRODUCTION TO THE PROCESSING OF CARDIAC LEFT VENTRICULAR FUNCTION DATA," H. Covvey, S.G. Boughner, R.W. Johnstone and E.D. Wigle, Toronto General Hospital
"THE FOLLOW-UP OF CARDIAC PACEMAKER PATIENTS WITH A MINICOMPUTER SYSTEM: TWO YEARS EXPERIENCE," B.S. Goldman, E.J. Noble, S.G. Boughner and E.D. Wigle, Toronto General Hospital
"COMPUTING IN A DEPARTMENT OF PSYCHIATRY: THE 3×10^9 MICROSECOND HOUR," G.F.D. Heseltine, P. Stenn, and D. Evans, University Hospital, London, Ontario
"DATA MANAGEMENT IN A HOSPITAL ENVIRONMENT. A MINICOMPUTER SYSTEM," R. Cheng, C. Scase, J. Gruer and M. Bennett, University Hospital, London, Ontario

9:00 SESSION 13: MICROPROCESSORS I

Chairman: Jonathan A. Titus, TYCHON, Inc.
"MICROCOMPUTERS – HOW TO PUT THEM TO WORK," David G. Larsen and Peter R. Rony, Virginia Polytechnic Institute and State University
"AN INTEGRATED HARDWARE-SOFTWARE MICROPROCESSOR DEVELOPMENT SYSTEM," D. R. Deuel and J. W. Gault, North Carolina State University
"OPERATING SYSTEM SOFTWARE INTERFACES FOR A MICROPROCESSOR," Alex Sidline, Honeywell

11:00 SESSION 14: COMPUTER NETWORK: A USER'S VIEWPOINT

Chairman: Gene Raichelson, The MITRE Corporation
"RESOURCE MARKET FOR USER COHERENT KNOWLEDGE," Douglas Englebart, Stanford Research Institute
"COLLABORATION SUPPORT," J. Eagle and J. Iseli, The MITRE Corporation
"INTELLIGENT TERMINAL AND NETWORKS," Robert Anderson, Rand Corporation

11:00 SESSION 15: COMPUTER AIDED INSTRUCTION

Chairman: Charles M. Goldstein, Lister Hill National Center for Biomedical Communications, Department of HEW

"MAKING COMPUTERS EASIER TO USE THROUGH DISTRIBUTED MINI/MICRO PROCESSORS: PILOT," John Starkweather, UC Medical School, San Francisco

"SPECIALIZED TERMINAL AND NETWORK: PLATO," Thomas Chen, University of Illinois

"GRAPHICS AND SPECIALIZED USER COMMANDS: TICCITT," C. Victor Bunderson, Brigham Young Unversity

"ANALYSIS OF VERBAL COMMUNICATION IN A CAI ENVIRONMENT," Jane B. Hirsch and Martin Hamburg, Cornell University College of Medicine

:00 SESSION 16: MICROPROCESSORS II

Chairman: Jerry Ogdin, Microcomputer Technique, Inc.

"A SOFTWARE DEVELOPMENT INSTRUMENT," Doug Cozlay and Alan Hastings, Isyx Corporation

"HARDWARE AIDS-SOFTWARE OVERTONES," Jim Moon and Larry Gray, E.S.L. Inc.

"MDS: AN ADVANCED DEVELOPMENT TOOL," William Broderick, INTEL Corp.

WEDNESDAY AFTERNOON (Parallel Sessions)

2:00 SESSION 17: COMMUNICATIONS

Chairman: Robert F. Decker, Systems Research and Development Service

"THE STRUCTURE OF SPECIAL COMPUTER IN SWITCHING PACKETS," J. Cabanel, J. P. Lagasse and Phillipe Puech, Université Paul Sabatier

"ARAMIS – A PROCESSING NETWORK WITH USER DATA BASES INTERACTIVE SYSTEMS," J. P. Lagasse, G. Artaud, and J. Cabanel, Université Paul Sabatier

"A PACKET SWITCHING NETWORK FOR MINICOMPUTERS," David M. McKeown, Jr. and F. H. Orthner, George Washington University Medical Center

"A MICROPROCESSOR CONTROLLED DATA SWITCH," Robert C. Chen, Peter G. Jessel and R. Patterson, The Moore School of Electrical Engineering

2:00 SESSION 18: GRAPHICS

Chairman: Ira W. Cotton, National Bureau of Standards

"COMPUTER GENERATED PICTURES OF GRAPHS," R. B. McGuire, University of Regina

"CALMA'S GPL tm LANGUAGE: A PROGRAMMING LANGUAGE FOR CUSTOM TURNKEY GRAPHICS SYSTEMS," Carl Smith, CALMA

"ATS-6 CONTROL CENTER REAL-TIME GRAPHICS DISPLAYS," R. desJardins and J. Hahn, NASA/Goddard Space Flight Center

2:00 SESSION 19: DATA BASE

Chairman: Thomas C. Lowe, National Bureau of Standards

"A CLOSED SYSTEM OF REPRESENTATION FOR RELATIONALLY-ORGANIZED DATA AND ITS DESCRIPTORS," Clifford R. Hollander, Stanford University

"AN EFFICIENT IMPLEMENTATION OF CODD'S RELATIONAL MODEL DATA BASE," Leon E. Winslow, Wright State Univ.

"A BENCHMARK TEST APPROACH FOR GENERALIZED DATA BASE SOFTWARE," Elizabeth Fong, National Bureau of Standards

4:00 SESSION 20: APPLICATION AUTOMATION

Chairman: N. J. Denil, IBM

"SOFTWARE ORGANIZATION FOR A MULTI-PURPOSE DESIGN AUTOMATION SYSTEM," Robert J. Smith II and Mathew N. Matelan, Lawrence Livermore Laboratory, University of California

"AN AUTOMATIC PROGRAM DESIGN AND GENERATION SYSTEM FOR MINI COMPUTER BASED DATA COMMUNICATION SYSTEMS APDG," N. Sugiura, T. Hayashi and M. Yasuoka, OKI Electric Industry Co., Ltd.

"THE AUTOMATIC TRANSFORMATION OF A SPECIFIC NATURAL LANGUAGE IN A FORMALIZED METALANGUAGE," E. Vaccari, Institute de FISICA

4:00 SESSION 21: HARDWARE DEVELOPMENT TOOLS

Chairman: John A. Darringer, IBM

"AN ARCHITECTURAL DEVELOPMENT TOOL FOR THE IBM SYSTEM/INTERMEDIATE LANGUAGE MACHINE (S/ILM)," Tony Carpino, IBM

"STRUCTURED CONTROL OPERATORS IMPLEMENT ON THE IBM SYSTEM/INTERMEDIATE LANGUAGE MACHINE (S/ILM)," J. P. Dorocak, IBM

"A QUASI PARALLEL HARDWARE LANGUAGE EMULATED BY AN HOST HIGH LEVEL LANGUAGE," Gerard L. M. Noguez, Universite PARIS

THURSDAY September 11, 1975

THURSDAY MORNING (Parallel Sessions)

9:00 SESSION 22: PATTERN RECOGNITION

Chairman: Laveen Kanal, University of Maryland

"MAKING COMPUTERS EASIER TO USE IN BIOMEDICINE," Judith Prewitt, NIH

"INTERACTIVE PATTERN ANALYSIS," Laveen Kanal, University of Maryland

"USING COMPUTERS IN REMOTE SENSING," Michael Hord, Earth Satellite Corporation

"AUTOMATION OF INVESTMENT ANALYSIS – A NEW HORIZON FOR APPLICATIONS OF ARTIFICIAL INTELLIGENCE," Jerry Felsen, University of Southwestern Louisiana

9:00 SESSION 23: PERFORMANCE MEASUREMENT

Chairman: Philip J. Kiviat, Federal Computer Performance Evaluation & Simulation Center

"PRACTICAL CONSIDERATIONS FOR COMPUTER SYSTEM MODELING," Jeffrey Buzen, Harvard University

"MEASUREMENT ORIENTED DESIGN OF COMPUTER SYSTEMS," Dinesh Kumar, Fed. Computer Performance Eval. & Simulation Ctr.

"A MODEL FOR WORKLOAD CHARACTERIZATION," A. K. Agrawala and J. M. Mohr, University of Maryland

"EXPERIMENTAL EVALUATION OF A MULTIPROGRAMMED COMPUTER SYSTEM," Y. V. Reddy, West Virginia University

9:00 SESSION 24: GENERAL SYSTEMS

Chairman: Gilbert Held, U. S. Postal Service

"OBFUSCATION – FREE INTERFACE AMONG THE SMALLBOAT SKIPPER, THE SAILBOAT AND THE ON-BOARD MINICOMPUTER," K. Flose, Consultant

"ENGINE CONSTRUCTION: THE MICROPROGRAMMED DESTRUCTION OF HIGHER-LEVEL LANGUAGES," Michael J. Viehman, TETRA Tech., Inc.

11:00 SESSION 25: VOICE RESPONSE

Chairman: Donald A. Biggar, Systems Development Corporation

"AUTOMATIC SPEECH UNDERSTANDING SYSTEMS," H. B. Ritea, System Development Corporation

"AUTOMATIC SPEECH RECOGNITION EXPERIMENTS," G. M. White, XEROX Palo Alto Research Center

"RECOGNITION OF CONTINUOUS SPEECH," J. K. Baker, L. R. Bahl and F. Jellineck, IBM

11:00 SESSION 26: SOFTWARE TECHNOLOGY FORECAST: 1975-1985

Chairman: Paul Willis, TELEDYNE – Geotech Laboratories

"SOFTWARE AREAS NEEDING FORECASTS," Paul Willis, TELEDYNE – Geotech Laboratories

"FUTURE OF HIGH LEVEL LANGUAGES," H. Maisel and A. Tucker, Georgetown University

"FORECAST OF SOFTWARE RELIABILITY 1975-85," Barry DeRose and Ch. W. Hamby, Automation Industries, Inc.

"EFFECT OF HARDWARE ON SYSTEM SOFTWARE; 1975-1985," Patrick J. Martin, U.S. Department of Agriculture

11:00 SESSION 27: (PANEL) DISTRIBUTED ARCHITECTURE: WHERE ARE WE GOING?

Chairman: David Farber, University of California at Irvine

Panelists: TO BE ANNOUNCED

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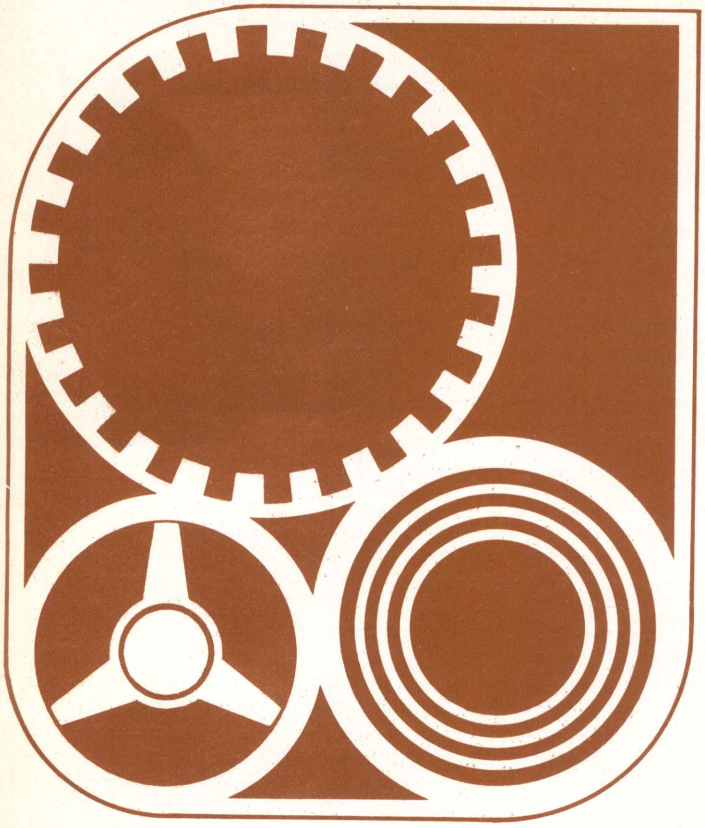

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Vice-Chairman: Dennis Fife, National Bureau of Standards
Program Chairman: Tom Steel, Equitable Life Assurance Society

SEPTEMBER 11 and 12, following COMPCON FALL '75 at the Mayflower Hotel, Washington, D.C.

THURSDAY September 11, 1975

THURSDAY MORNING

8:30 – 9:30: REGISTRATION

9:30 – 10:30: OPENING SESSION

Chairman: Harlan Mills, IBM

Keynote Speaker:
Frederick P. Brooks, Jr., University of North Carolina

11:00 – 12:00: CONCEPTS

Chairman: M. Marcotty, General Motor Research Laboratories

"A TOP-DOWN VIEW OF SOFTWARE ENGINEERING,"
A. I. Wasserman, Univeristy of California, San Francisco
"SOFTWARE TOOLS,"
B. Kernighan and P. J. Plauger, Bell Telephone Laboratories, Murray Hill, New Jersey

THURSDAY AFTERNOON

1:30 – 3:00: TOOLS

Chairman: B. Liskov, MIT

"THE COLUMBUS APPROACH,"
Jan Witt, Siemens Ag., Munich, Germany
"SOFTWARE MONITORS AIDING SYSTEMATIC TESTING AND THEIR OPTIONAL PLACEMENT,"
C. V. Ramamoorthy, University of California, Berkeley, K. H. Kim, University of Southern California
"*STRUCT* PROGRAMMING ANALYSIS SYSTEM,"
J. E. Stockenberg and Andries van Dam, Brown University

3:30 – 5:00: DEVELOPMENT PROCESS CONTROL

Chairman: Donald J. Reifer, Aerospace Corporation

"THE SOURCE CODE CONTROL SYSTEM,"
Marc J. Rochkind, Bell Telephone Laboratories,
"PREDICTING PROGRAMMING GROUP PRODUCTIVITY – A COMMUNICATION MODEL,"
R. F. Scott and D. B. Simmons, University of Texas
"AN EXPERIMENTAL PROGRAM TESTING FACILITY,"
Richard E. Fairley, Texas A&M University

FRIDAY September 12, 1975

FRIDAY MORNING

9:00 – 10:00: EXPERIENCE

Chairman: Robert C. McHenry, IBM

"ITERATIVE ENHANCEMENT: A PRACTICAL TECHNIQUE FOR SOFTWARE DEVELOPMENT," Victor R. Basili and Albert J. Turner, University of Maryland
"PROGRAM DESIGN BY A MULTIDISCIPLINARY TEAM," Susan Voigt, NASA, Langley Research Center
"APPLIED SOFTWARE ENGINEERING: A REAL-TIME SIMULATOR CASE HISTORY," S. R. McCammon, RCA Missile and Surface Radar Division

10:30 – 12:00: METHODOLOGY

Chairman: John Gosden, Equitable Life Insurance Co.

"STRUCTURED PROGRAMMING AND FORMAL SPECIFICATION," R. Noonan, University of Maryland
"SOFTWARE PERFORMANCE MODELING USING COMPUTATION STRUCTURE," Howard A. Shool and Taylor L. Booth, University of Connecticut
"TOP-DOWN, BOTTOM-UP AND STRUCTURED PROGRAMMING," C. L. McClure, Illinois Institute of Technology

FRIDAY AFTERNOON

1:30 – 3:00: SUMMARY PANEL

Chairman: Raymond Yeh, University of Texas

Panelists: M. Marcotty, General Motors Research Laboratories
B. Liskov, MIT
Donald J. Reifer, Aerospace Corporation
J. Gosden, Equitable Life Insurance Co.

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- COMPCON registration fee includes one copy of the Digest of Papers, and provides you with 2 complimentary drink tickets for each of the COMPCON hosted parties, Tuesday and Wednesday nights.
- SOFTWARE ENGINEERING registration fee includes one copy of the conference proceedings.

LATE REGISTRATIONS will be accepted at the Mayflower Hotel beginning Sunday evening, September 7, 1975.

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TECH NOTE

Simplifying Processor Maintenance with a Carefully Designed Maintenance Panel

George Gillow

The National Cash Register Company
Data Processing Division
San Diego, California

A maintenance panel enabling the service engineer to observe and manipulate data patterns in a system and to have manual control of microdiagnostic routines can greatly speed up failure detection and reduce overall repair time

The ideal computer maintenance scheme involves a machine that can completely diagnose itself and isolate all failures; a cathode-ray tube (CRT) display or printout would identify the exact hardware needing replacement. Diagnostic programming has come a long way toward allowing a machine to diagnose its own failures. Since many computers —from small minicomputers to large scientific machines—are microprogrammed, microdiagnostic routines provide an efficient way to exercise a large portion of the hardware and isolate faults to the card, chip, or even gate level.

However, even microdiagnostic techniques cannot as yet locate *all* failures. Well thought-out hardware aids—particularly a straightforward maintenance panel and associated logic—can greatly assist the maintenance engineer in locating failures that could previously be found only with manual techniques.

Microdiagnostics Fault Location

Fig. 1 depicts a portion of a simplified microprogrammed central processing unit (CPU). Microinstructions are stored in a microinstruction memory, or read-only memory (ROM), which is addressed by a ROM address register (ROMAR). The microinstruction is read out of the ROM into an instruction register (IR), outputs of which form control lines, literals, and local storage addresses.

A typical microdiagnostic program (see Table) for checking an arithmetic logic unit would first load the local store with a number of predetermined data patterns, one of which is gated into the adder. Result of the addition is tested against the predetermined sum. If the sum is incorrect, the HALT instruction stops the machine, at which time the engineer can determine the problem area by knowing which portion of the routine has failed. The ability of the microdiagnostic routine to perform many additions with a number of data patterns provides for thorough testing of all logic, and enables isolation to the card or even chip level.

Manual Fault Location

Although in many cases the microdiagnostic routines described can isolate all failures, some occur that

cannot be easily isolated—by any type of programmed diagnostics:

- Failures in control storage (ROM), ROMAR, or IR prohibit execution of any microdiagnostics
- Failures of clocks and clock-generating hardware, since this hardware area is not directly controlled by microinstructions (this applies to any area not directly controlled by microinstructions)
- Some failures of gates that drive buses. Several gates on various printed circuit cards may be wire-ORed together. If one gate is stuck at 1, for example, determining by diagnostics which gate in the series is faulty may be impossible; even card isolation is difficult
- Failures occurring in hardware, such as control store load paths, that must be operational before any microdiagnostics can be loaded; this is known as "hardcore"

These faults require manual isolation by the engineer; a simple, well designed maintenance panel can greatly decrease the amount of time required for performing this task. For example, assume that the machine in Fig. 1 has 8-bit data paths and a 16-bit microinstruction word. On one possible maintenance panel (Fig. 2), the rotating select switches (SELA and SELB) can be set to display the bit patterns of each register, bus, and other important data paths or control lines. For paths having more that eight bits, switch A can select the least significant bits; switch B, the most significant.

Panels may contain more than two display arrays, but in general, the engineer does not need to observe more than two (or perhaps three) at a time. He may display data in the A array and an address in the B array, or display both inputs to the execution unit or one input and the resulting sum. Select switches may be expanded from those in Fig. 2 to include additional functions. Also, the number of display lamps may exceed 8 (16, 24, 32, or more).

Data can be manually loaded into any register or local storage. To load a register, it is selected by a select switch. The data pattern is placed on the address/data switches, and the corresponding ENTER switch pressed. For entering data into local storage, the address is placed on the B switches, data on the A switches; load button A is pressed.

Portion of Typical Microdiagnostic Program

Address	Microinstruction	Comments
1001	LOAD LS1 (100) DEC	Load three local storage locations with predetermined data
1002	LOAD LS2 (500) DEC	
1003	LOAD LS3 (600) DEC	
1004	TRANSFER LS1→ACC	Accumulator contains the number 100 (decimal)
1005	ADD LS2+ACC→ACC	Accumulator should contain the number 600 if adder works properly
1006	COMPARE ACC, LS3	Result in accumulator is compared against known correct result of 600 in LS3
1007	HALT if no compare	If an error occurs, processor clock stops (if HALT switch is on)
1008	LOOP 1005	If LOOP switch is on, program will loop

The panel is also equipped with status indicators for interrupts, parity errors, trap modes, and so on.

When the test switch is placed in CS (control storage) position, predefined patterns of data (set on the address/data switches) are entered into each location of control storage and then read out. Error-detection hardware checks the data for parity and compares them with the address/data switches. By placing the test switch in MONITOR position, a meter checks the frequency of occurrence of an event by selecting data to be monitored and entering the event (data pattern) in the data switches. The NORMAL position is for normal running.

Loop and Halt Functions

LOOP and HALT switches operate in concurrence with LOOP and HALT microinstructions, as illustrated in the previous example. When a HALT instruction is executed, the CPU clock stops if (and only if) the HALT switch is on and a specified condi-

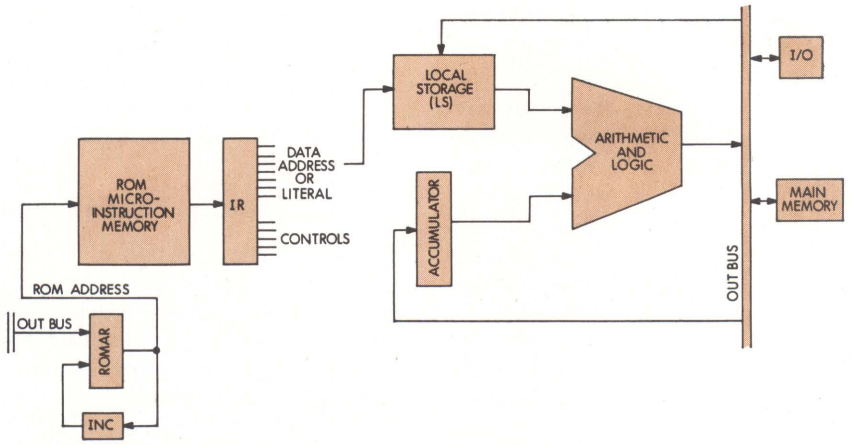
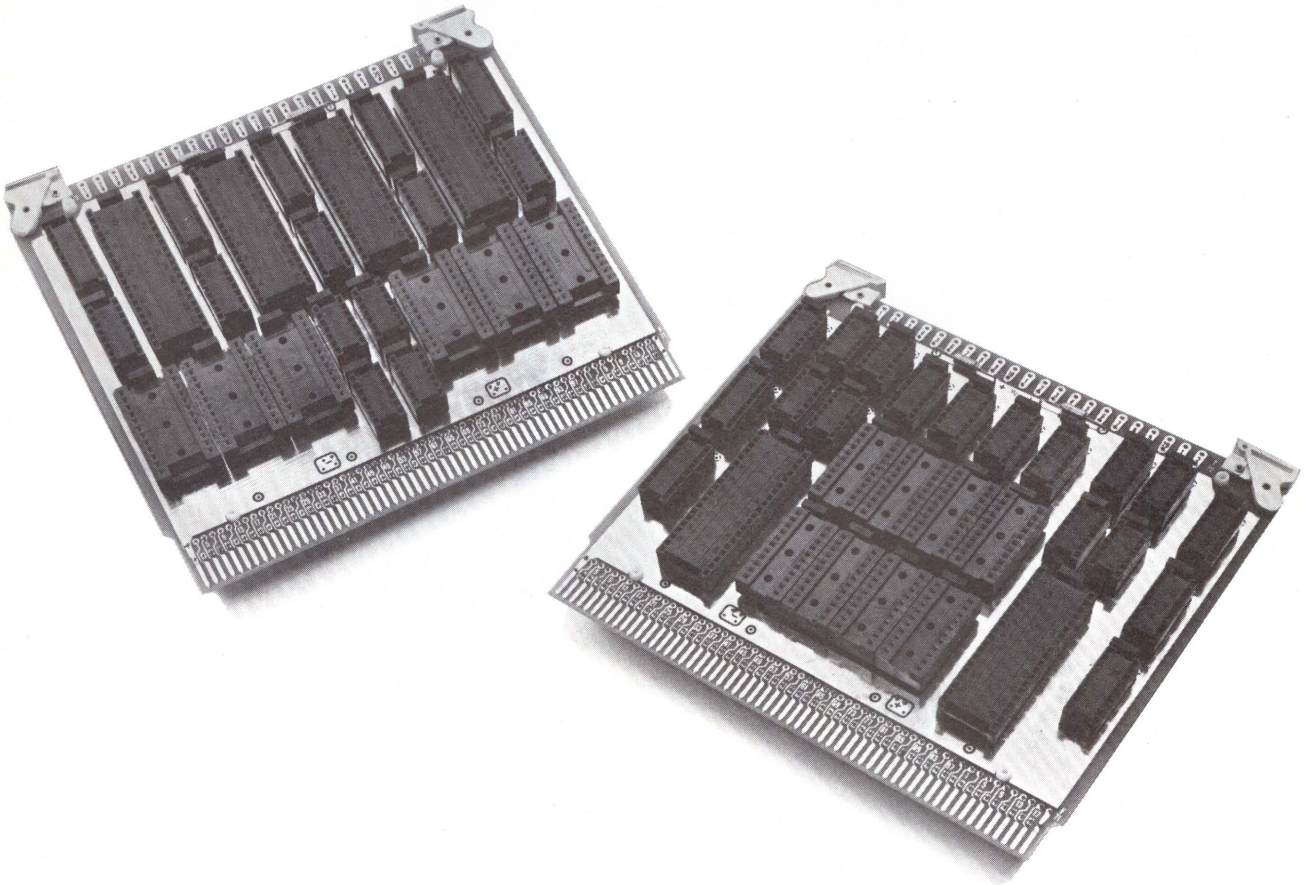


Fig. 1 Microinstructions are stored in a ROM of this simplified CPU. ROM is addressed by the address register, ROMAR. Microinstructions are read out of the ROM and stored in the instruction register (IR). Outputs of the IR form control lines (or are decoded to form control lines) and local storage addresses. Data to the arithmetic and logic unit come from the local storage and the accumulator with results placed in the accumulator via the Out bus

New socket cards for microprocessors.



Instantly available, these two new cards are your answer to second-source problems. They enable you to change ICs and wiring for new pin patterns with great ease.

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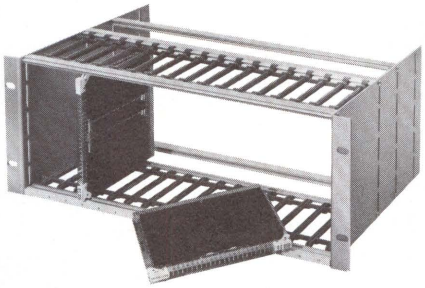

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Fast talk

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They both have interrupt logic and they're both double buffered. This lets the MPU operate much more efficiently, because it's not a slave to its family.

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Features of the S6850 ACIA

- 8 bit bidirectional data bus for communication with MPU.
- False start bit deletion.
- Peripheral/modem control functions.
- Double buffered receiver and transmitter.
- One or two stop bit operation.
- 7 or 8 bit characters with odd, even or no parity.
- Parity, overrun and framing error checking.
- Programmable control register.
- Optional ÷ 1, ÷ 16, and ÷ 64 clock modes.
- Up to 800,000 bps transmission.

Features of the S2350 USRT

- 500 KHz data rates.
- Internal sync detection.
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- Bus oriented outputs.
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- Odd/even or no parity.
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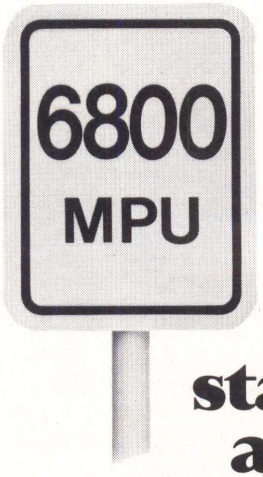

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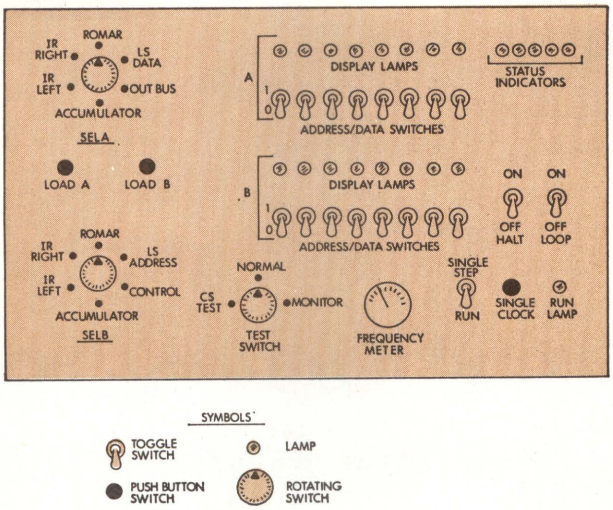

Fig. 2 Maintenance panel allows the service engineer to observe data patterns on all buses, registers, memory locations, and control lines by selecting the appropriate area with the select switches. Data can be loaded into registers and memories with the LOAD A and LOAD B buttons and the (local storage) ADDRESS/DATA switches. The test switch allows for monitoring of particular events and for testing the control storage hardware, Loop and Halt switches are used with special diagnostic microinstructions to control the microdiagnostic routines, and the Single-Step switch enables manual stepping of the system clock

tion (as shown) is met. The LOOP switch acts as an unconditional branch back to a predetermined location in the program when (and only when) the switch is on.

A diagnostic program is initiated by the engineer when the HALT switch has been turned on and the LOOP switch turned off. If an error occurs, the program will halt. The engineer can display various registers to locate the incorrect data pattern. He then turns the HALT switch off and the LOOP on and runs the program again. Only those instructions involving an error are executed, allowing the problem areas to be probed with an oscilloscope.

Another important switch is single step/run (SS/RUN). In RUN position, the machine executes normally; in SS, it executes one clock at a time (when the SS CLOCK button is pressed).

Conclusion

This maintenance panel could be expanded to accommodate testing of main memory, input/output, and so on. Data paths displayed could also be made larger. Additional cost of the switches, display lamps, and associated logic will in most cases enable more rapid repair times, resulting in lower factory debug and field repair costs.

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TECH NOTE

Digital Synthesizers Produce Wide Frequency Range from Single Source

John D. Fogarty

Professional Engineer
Columbia, Maryland

Fine resolution, transientless frequencies can be achieved by using direct digital synthesizers, which create waveforms by stepwise outputting samples of the waveform stored in a ROM. One example of the required calculations is presented here, along with a discussion of error sources inherent in the digital design

A frequency synthesizer differs from a tunable signal generator in that it derives all of its output frequencies from a single frequency source. A direct digital synthesizer does this by performing arithmetic operations at a rate determined by this frequency standard, ie, its digital "clock." Direct synthesis inherently provides fine resolution, transientless frequency changing with amplitude and phase continuity, "instant" phase-jumping for reference lock, and known spectral content.

Basic Concept

Direct digital synthesis of a sine-wave frequency is based on the definition of frequency as a rate of change of phase, ie, rate of rotation of a generating phasor.

$$f = \frac{d\phi}{dt}$$

Here dt is the digital logic clocking period and $d\phi$ is the phase-step size number input to the synthesizer. This input number is, therefore, directly proportional to the frequency output.

Minimum frequency increment or "channel subdivision" is governed by the least-significant bit (LSB) position choice in the phase accumulator and by the logic clocking rate. Absolute maximum frequency is limited to one-half of the logic clocking rate by the fundamental Nyquist criterion for reconstruction of sampled analog signals. In practice, the maximum generated frequency should be kept to about one-quarter of the clocking rate in order to minimize the filtering requirement on the output waveform. Frequency conversion and doubling techniques may, of course, be applied to the baseband output in order to get higher desired frequencies than can be obtained directly.

Implementation

Components of a digital frequency synthesizer are shown in block diagram form in Fig. 1. Central element is the sine/cosine read-only memory (ROM) which is addressed by the phase-count number bein continuously built up in the "ove flowing" phase accumulator. Th phase accumulator consists of a adder and an output register. Phase step size number ($d\phi$) is added int this accumulator at every clock interval (dt).

ROM addressing is walked up (sine) and then down (cosine) by the bits increasing in the phase accumulator; the address count (and hence direction) is flipped over by a complementer (bit inverter) un-

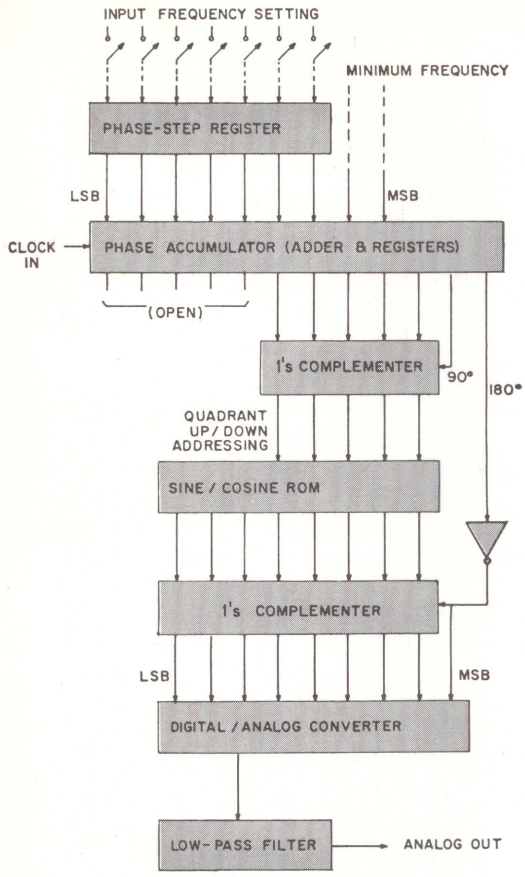


Fig. 1 Direct digital synthesizer. Interconnection of major b'ocks show up/down ROM quadrant addressing, and positive/negative half-sinewave control by the MSBs of the overflowing phase accumulator

der control of the next-most significant bit (quadrant signum) after the address bits. Unipolar binary values of the half-sinewave output by the ROM are themselves complemented, under control of the accumulator bit following the quadrant bit, to form the negative-half-sinewave as required. These binary numbers go to the bipolar digital-to-analog converter (DAC) which produces the sampled-and-held analog waveform. Low-pass filtering (LPF) is all that is needed to complete the synthesis.

Fig. 2 shows this build-up in the phase accumulator with accompanying up/down ROM addressing, number values output by ROM, and bipolar DAC result. Up/down and positive/negative areas of the phase accumulation show the quadrant and halfwave bit-control regions. Although smooth lines are illustrated, they should actually be drawn as very coarse staircases, because of the large phase steps required near the maximum working frequencies.

The phase accumulator need never be cleared unless it is necessary to "instantly" synchronize the phases of two synthesizers by resetting to the same (zero) point for both waveform outputs. Rather, the accumulator keeps on increasing in increments of the phase-step input number. The "carry-out" bit is ignored as the accumulator overflows and the count "folds back" around zero and builds up again. Slope of the build-up is a function of the phase-step size.

Referring back to Fig. 1, ROM addressing is limited and the accumulator's LSBs go nowhere. Thus, it may take many clock times to count up a small phase-step to the point where it steps the ROM addressing one more notch in generating a low frequency. Alternatively, if only a narrow band of frequencies is to be covered, one or more large phase steps may be hardwired into the accumulator as the bottom of the band while the phase-step register holds only the range to be spanned.

If a 90-deg quadrature output is also required from this synthesizer, a second DAC/LPF can be added to the digital output via a multiplexer (MUX), and a 2f clock can be used to toggle the MUX *and* the quadrant/polarity controls between the two DACs for each step of the phase clock. Latches are required for each DAC input.

Frequency Determination

Phase-step/accumulator sizing can best be illustrated by an example. To design a synthesizer that will provide a 1.7- to 1.8-MHz output band with 1.25-kHz channel steps, we first compute the minimum clock frequency. From Nyquist's criterion for the upper frequency limit, we know that this clock must operate at a rate in excess of 2 x 1.8 MHz, or >3.6 MHz. Next, using the minimum frequency step size of 1250 Hz as the LSB value for the phase accumulator, we can size this accumulator as the binary count needed to divide this 3.6-MHz clock down to 1250 Hz: 3.6 MHz ÷ 1250 Hz = 2880. Since the next higher power of 2 is $2^{12} = 4096$, a 12-stage accumulator is needed and the clock should be 1250 Hz x 4096 = 5,120,000. Our Nyquist limit is now 2.56 MHz. Theoretically, this is all right, although it is a little tight for the low-pass filter needed; ie, the folded clock lower-sideband of 1.8 MHz will fall at 5.12 − 1.8 = 3.32 MHz. Since TTL logic should operate at 10.24 MHz, that might be a better choice; however, 12-bit accumulators are efficient to build, so we will pursue the 5.12-MHz example.

Because we are operating in a limited band, we can hardwire some phase accumulator input bits and reduce our phase-step register size. Manipulation of binary numbers reveals that hardwiring bits 2^{10} and 2^8 gives a low limit of (1024 + 256) x 1250 Hz = 1.6 MHz. Adding in bits 2^6 and 2^5 yields (1024 + 256 + 64 + 32) x 1250 Hz = 1.8 MHz. Therefore, we can use a 6-bit phase-step register to achieve the desired range. Setting bits 2^6 and 2^4 starts us off at 1.7 MHz, while setting in *all* bits brings us up to

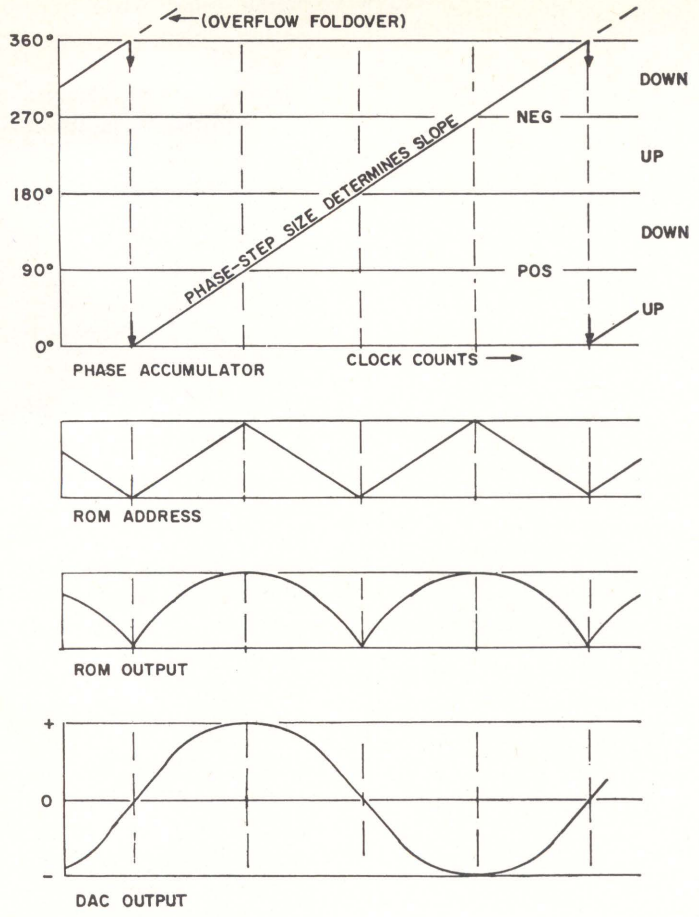


Fig. 2 Digital synthesizer operation. As the count builds up and overflows in the phase accumulator register, the two MSBs control the ROM-addressing direction and the bipolar DAC output polarity

1,838,750 Hz as a top operating limit, nicely bracketing the desired range.

A similar analysis can be used in a synthesizer design for other frequency steps and ranges.

Error Sources

A number of inherent error sources detract from the purity of the sinewave synthesized by this digital construction. Ignoring obvious external errors from clock accuracy and stability, internal errors derive from phase resolution, arithmetic jitter, and analog filtering.

Phase resolution is a function of the number of phase-change steps inherent in the chosen ROM. The DM8598 AA, a 16-pin DIP with 5-bit addressing and 8-bit output resolution from National Semiconductor Corp, breaks the quadrant into $2^5 = 32$ slices or 128 steps for the complete 360-deg sinewave. This means that the phase-positional accuracy of any one sample may be off by ±1.4 deg. Actual phase-step size, of course, may be many multiples of this for the higher frequencies generated. The sinewave function ROM performs a "filtering" action on the sidebands produced by limiting the energy in any one "misstep"—the fundamental *frequency* output is a property of digital counting only. This ±½ LSB in five bits of addressing drops the sideband amplitude to 1/64 or −36 dB. If better spurious frequency suppression is required, more steps must be used in the ROM.

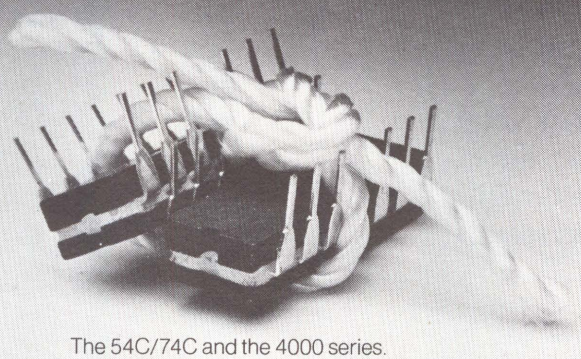
"Arithmetic jitter" is another way of viewing ROM-addressing resolution. The phase accumulator is stepped by adding in another phase-step word at every clock. Accumulated addressing as seen by the ROM's LSB will contain an inherent "pulse position modulation" of a magnitude equal to this LSB. This explains the occurrence of different spurious sidebands for different frequency settings (their amplitude is set by the step size as described above). If the frequency generated happens to be a power-of-2 submultiple of the clock, there will be *no* missteps in phase and hence *no* spurious sidebands.

A second arithmetic error that is built into this particular design proves to be inconsequential. The DAC uses 2's complement binary input numbers, yet the signum inverter, which produces the negative half of the sinewave, actually outputs 1's complement binary numbers. This is done because simple bit-inverter logic is easier to implement than a true 2's complementer, and the 1-bit error in eight bits of output accuracy represents a −54-dB spurious frequency, which is not serious enough to correct. The fact that this is second-harmonic error energy does not really help, since this second harmonic appears on all frequency replications of the sampled spectrum and is amply folded back into the region of interest as an "aliased" frequency.

The last error source (or clean-up) consists of output DAC and low-pass filter. A fundamental principle of sampling is replication of the sampled spectrum around *all* multiples of the sampling frequency. If a frequency *can* be represented by sample amplitudes, it will actually be present. The function of the low-pass filter is to remove all of these spectral components above the Nyquist limit (fs/2). The closer the output is to approximate one-half of the clock rate, the more stringent the filtering cut-off requirement. Therefore, the highest operating clock frequency is the most desirable from the filtering viewpoint.

Samples output by the DAC are "boxcarred" by the ROM step holding. This tends to decay the higher harmonics by the sinc-function spectrum of the boxcar. In addition, the finite response time of the DAC rounds off the "staircase" waveform generated and constitutes part of the low-pass filtering action. □

Look who just tied the knot.



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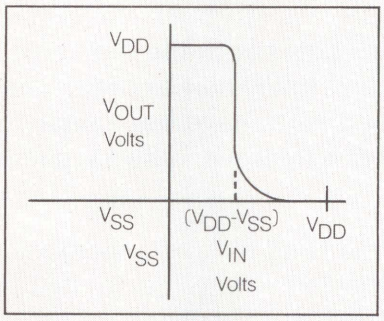
DEVICE	OUTPUT SINK CURRENT	MINIMUM
4002A	I_{OL} (V_{OL} = 0.4V)	0.40 ma
4042A	I_{DN} (V_{OL} = 0.5V)	0.20 ma
4001A	I_{OL} (V_{OL} = 0.4V)	0.30 ma
All 54C/74C	I (V_{OL} = 0.4V)	0.36 ma
4071B	I_{DN} (V_{OL} = 0.4V)	0.40 ma

This illustrates some of the variations in output drive current specified in the 4000 series, and how the 54C/74C fits within the range.



This CMOS transfer characteristic for single level gate functions is for all CMOS logic families. It is the commonality of this characteristic which is the basis of CMOS inter-family compatibility.

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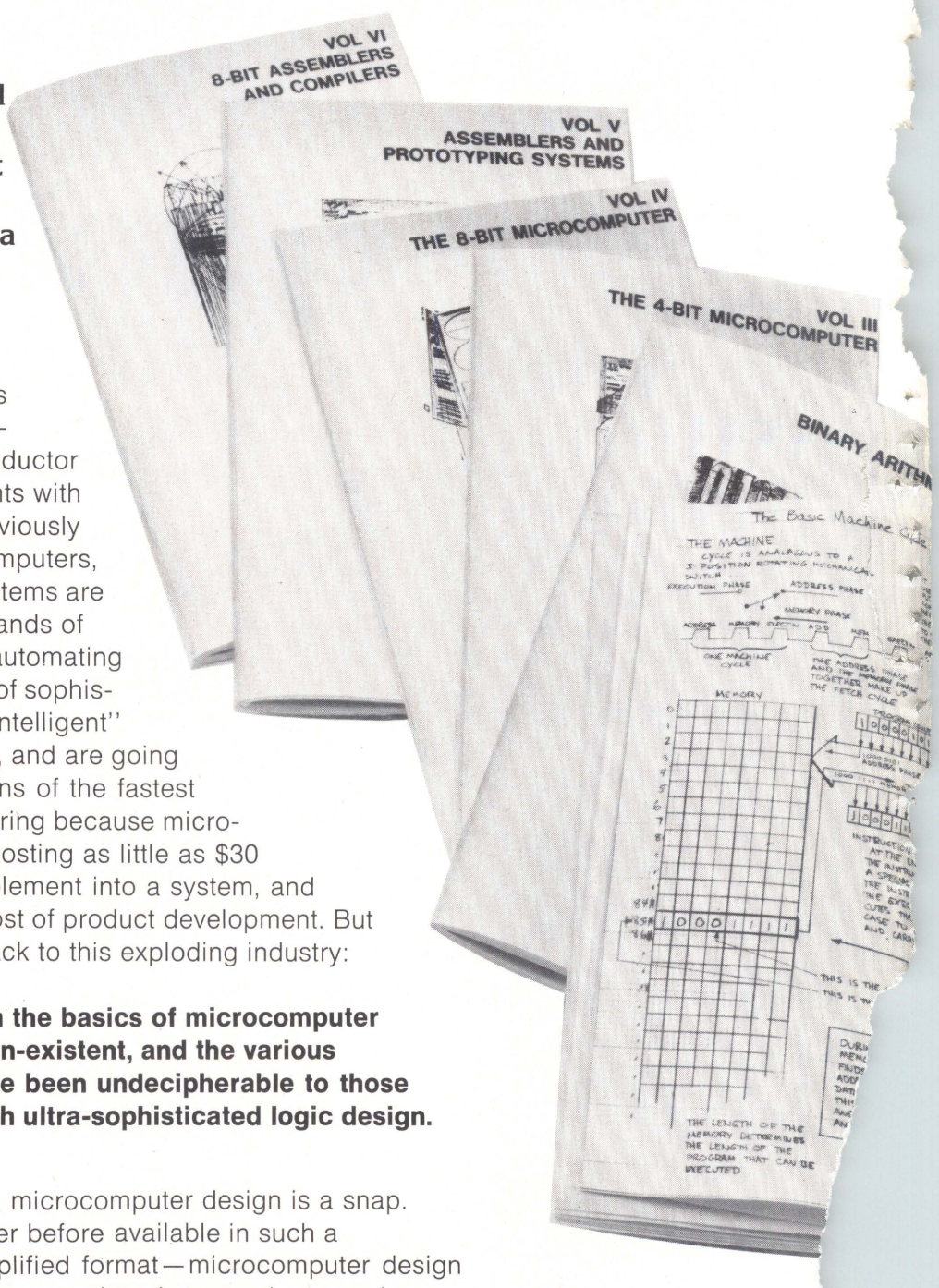

Since the transistor was invented, no single electronics innovation has made such an impact as the microcomputer. Powered by tiny semiconductor chips containing computing elements with the same powers and functions previously found only in large scale digital computers, these dedicated microcomputer systems are now being applied to literally thousands of applications. Microcomputers are automating assembly lines, providing the heart of sophisticated electronic games, making "intelligent" computer peripherals even smarter, and are going so far as streamlining the operations of the fastest food chains. This revolution is occuring because microcomputers are very inexpensive—costing as little as $30 in production volume—easy to implement into a system, and significantly reduce the time and cost of product development. But there has been one serious drawback to this exploding industry:

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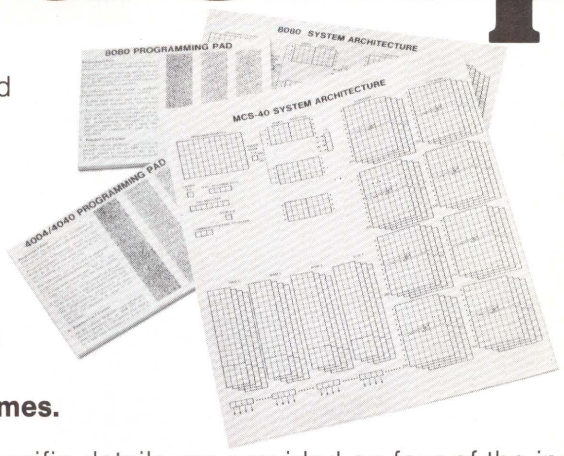

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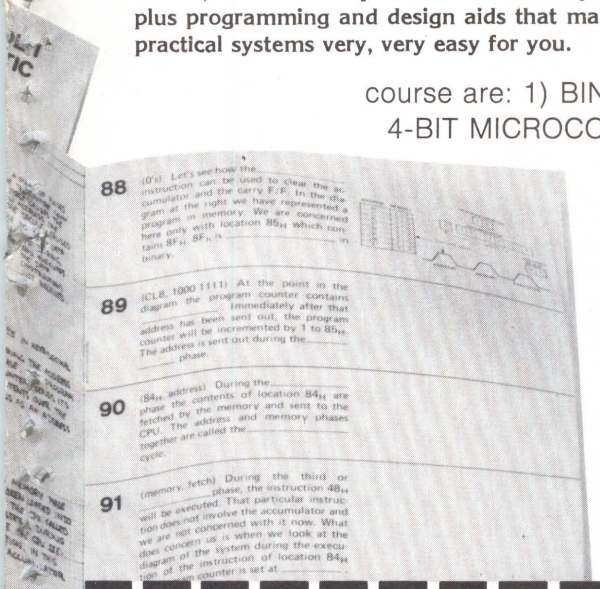

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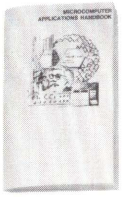

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APPLICATION NOTE

Pattern Analyzer Synchronizes Scope in Presence of Jittery Signal

Ralph Reiser

Hewlett-Packard Company
Colorado Springs, Colorado

For stability, an oscilloscope display of disc waveforms must be synchronized with a reference point more closely linked to the data than any sector pulse, especially when multiple records are being read by the computer. A pattern analyzer can eliminate potential jitter display problems by recognizing a unique record address that is phase-locked with the data, and triggering the oscilloscope when the address is found

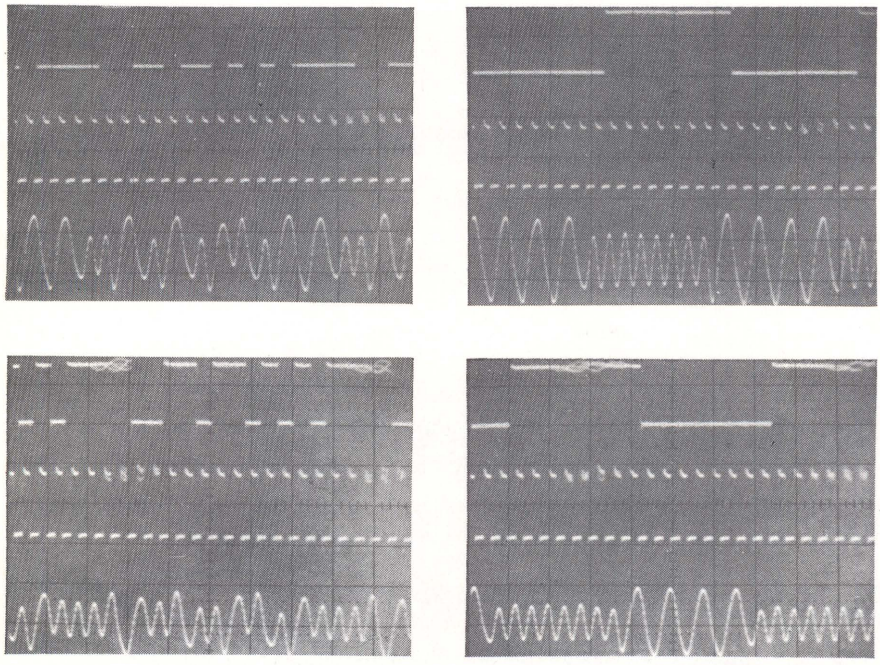


Fig. 1 Timing variations. Three traces in each of these scope photos show, respectively, data signals, clock signals, and analog head output. Two upper photos show data read from outer track of disc, with larger amplitude than inner-track data in lower photos. Randomly mixed 1's and 0's (left) compared with strings of consecutive 1's and 0's (right) show effect of pulse crowding

Although an oscilloscope with a time-delayed sweep is capable of making many measurements, it may be unsatisfactory in instances that require occurrence of a trigger signal at a specific point in time. However, such a signal is easily recognized by a pattern analyzer—a general-purpose instrument that recognizes many possible combinations of digital signals. When used in conjunction with an oscilloscope, it permits unusual digital measurements to be made—without having to depend on a technician's innovational ability or build special-purpose synchronizing devices.

A pattern analyzer generates a trigger signal from any serial or parallel digital pattern it is programmed to recognize. In the Hewlett-Packard 1620A, for example, patterns of up to 16 bits can be selected for recognition and the trigger output signal may be delayed up to 999,999 clock intervals from the recognition point. Parallel operation may be either synchronous

or asynchronous. In serial operation, a separate qualifier line enables bit patterns to be monitored at a specific point in time (by the leading edge of a sample pulse) or during time intervals (duration of the sample pulse). Edge-qualified mode can be selected for either positive- or negative-going transitions; it also permits use of serial frame delay, which selects the time (up to 99 clock intervals) when the analyzer looks for word recognition from the qualifier starting edge.

Triggering Example

A disc storage unit offers an example of a triggering problem that a pattern analyzer can solve with ease. A system may store over 100,000 bits on a single track, with many millions of bits on each recording surface. Small speed variations of the rotating disc, pulse crowding (time displacement arising from certain patterns of data), and an indeterminate inter-record gap contribute to a fluctuating data transfer rate, which results in a jittering oscilloscope display that is difficult to interpret.

Also, disc-reading errors sometimes show up as low-quality analog signals from the disc. Such a signal may be due to a nonuniform coating of magnetic oxide, varying head-to-magnetic-medium spacing, or poor head-to-track alignment. In addition, analog output signals from the inner tracks of the disc are lower in amplitude than are signals from the outer tracks. These variables necessitate synchronizing with the data rate in the phase-locked area rather than with an absolute reference.

With all the possible variations in data timing, some of which are illustrated in Fig. 1, it becomes a challenge to locate one particular bit, and even more so to display this bit stably for electrical analysis. With a wideband oscilloscope triggered by an instrument capable of detecting a particular digital pattern, the task is easily met.

Synchronization Without Jitter

In disc systems where the sector pulses, which define the start of each new record, are synchronous with the data, synchronization is easy. However, in systems where the pulses are otherwise synchronized or when more than one sector on a track is active, synchronizing the oscilloscope from sector pulses may produce a jittering display or a display of the wrong data.

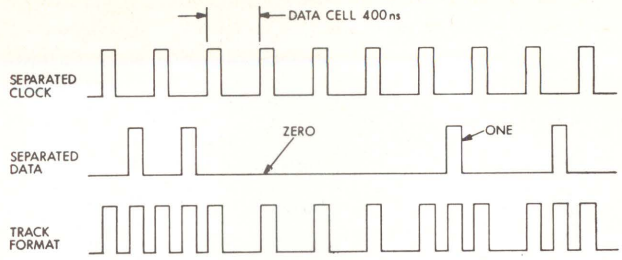


Fig. 2 Track format. Sequence of clock pulses (top) defines data cell boundaries; data, represented by presence or absence of pulses, are timed to fit nearly in center of data cells. Hence, 2-frequency series represents combined data and clock pulses

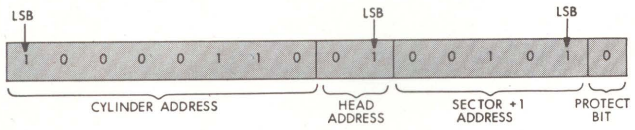
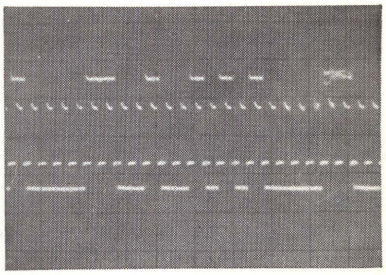
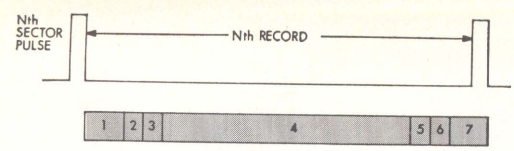


Fig. 3 Real address. A 16-bit word (top), divided into segments to show the various parts of a record address on a disc, appears in a scope trace (right) superimposed on a clock sequence. For example, the single data pulse rising above the clock pulse at the left-hand side of the trace represents the first 1 in the 16-bit address; it is followed by a series of four clock pulses during which the data level is low, representing the next four 0's in the address



Although the synchronization method described here can be used with sector pulses, it was applied in particular to a disc system having a combined data clock, phase-locked loop. The moving-head disc unit rotates at 2400 rpm and mixes data with a series of 2.5-MHz clock pulses in such a way that a 1-bit causes occurrence of a pulse between two clock pulses, and a 0-bit leaves an open space between two clock pulses (Figs. 2 and 3). These are combined into a record in the format shown in Fig. 4; successive records, together with the related control signals, are illustrated in Fig. 5.

Combined data and clock pulses read from the disc are divided into separate pulse trains. Because variations in disc drive speed cause the instantaneous data transfer rate to fluctuate, it is necessary to synchronize with the data rate when reading out information rather than with an absolute mechanical reference. This synchronization starts during the preamble at the beginning of each



1. PREAMBLE	APPROX 192 ZEROS	PHASE-LOCK LOOP
2. SYNC WORD	1 BIT PLUS 15 ZEROS	PHASE-LOCK LOOP
3. ADDRESS WORD	16 BITS	CYLINDER, HEAD, RECORD ADDRESS
4. INFORMATION FIELD	2048 BITS	128 × 16-BIT WORDS
5. CYCLIC CHECKWORD	16 BITS	
6. POSTAMBLE	32 ZEROS	
7. INTER-RECORD GAP	INDETERMINATE LENGTH	

Fig. 4 Record format. Data are recorded in this format on a typical magnetic disc unit. Indeterminate length of inter-record and preamble present ambiguities that preclude synchronizing a display to the sector pulse

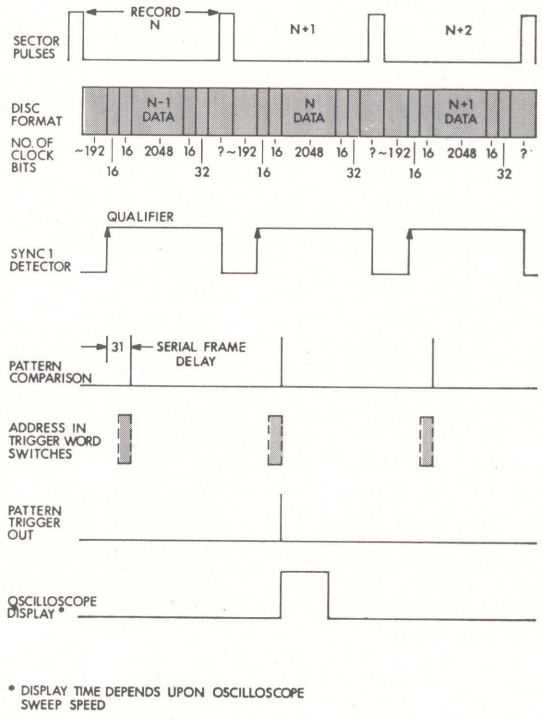


Fig. 5 System format. Pattern analyzer responds to this storage format by qualifying itself on the first synchronizing 1-bit. Serial frame delay puts the sync word and the address word into a shift register for comparison with a desired address, specified manually by trigger word switches. Equal comparison generates a pattern trigger out, which in turn triggers the oscilloscope sweep to display disc contents at that point

record, when the phase-locked loop synchronizes the clock with data from the disc. The address word is read after synchronization is complete; it is unique in the system because it identifies one of many thousands of records.

Sync-Triggering Requirements

An instrument that generates a reliable and stable synchronizing pulse on this unique address requires three sync-triggering features: first, it must look only at the address portion of each record; second, it must compare each record address pattern to the desired record address, selected by the measurement technician; and third, when the desired address is found, it must generate a "pattern trigger out" (PTO) pulse to start the oscilloscope sweep.

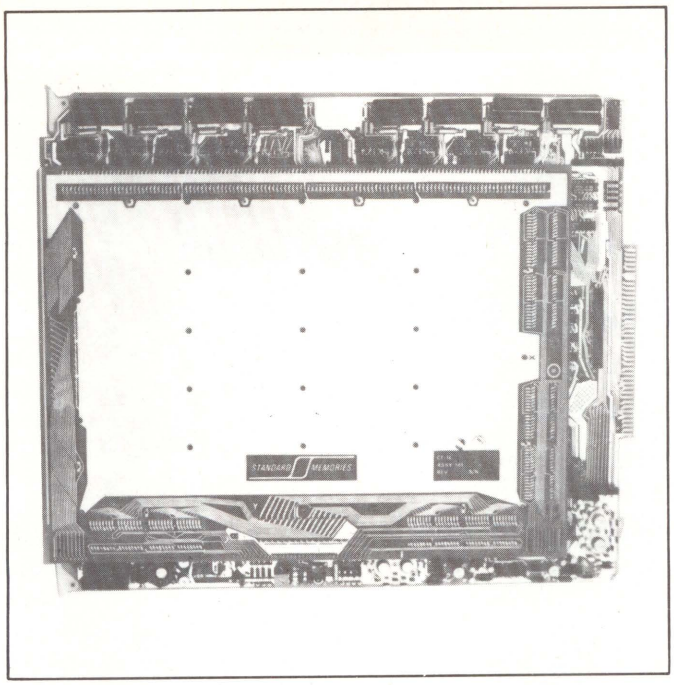
In the pattern analyzer, the data, having been separated from the clock pulses, are sent through a 16-bit shift register. In each record the first 1-bit comes at the beginning of the sync word; its arrival turns on the sync 1 detector signal on the disc interface board. Using the rise of this signal as a positive edge qualifier for the pattern analyzer and counting off a serial frame delay of 31 puts the sync word and the address word in the shift register at the moment a logic pattern comparison is made.

If and when this pattern matches that of the analyzer's trigger-word switches, the pattern analyzer generates the PTO pulse. This triggers the oscilloscope, which then displays waveforms of the record specified by the trigger-word switches. A similar "delayed trigger out" (DTO) pulse can trigger the oscilloscope up to 999,999 clock periods after the pattern has been recognized.

Without changing any disc test connections, the oscilloscope can be synchronized to any record in the system by setting the analyzer trigger word switches to the record address of interest. Meanwhile, digital delay, combined with pattern triggering, permits other areas on the disc to be examined without having to define additional trigger points. Delay also allows a trigger point to be selected in one record while the sweep begins at a location near a troublesome point in another, where a trigger point may not be available. The delayed trigger can also easily obtain the end-of-word pulse or an inter-record gap of indeterminate length.

Conclusion

Digital pattern-triggering can virtually eliminate the effects of speed variations and stabilize a display for analysis. It works for data transfer in either direction, or for any number of active records, and can pick any one sector out of more than 19,000 on a typical disc storage unit. □



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APPLICATION BRIEF

An Asynchronous Time-Division Multiplexing System

C. T. Pardoe and R. L. Appel

Applied Physics Laboratory
The Johns Hopkins University
Silver Spring, Maryland

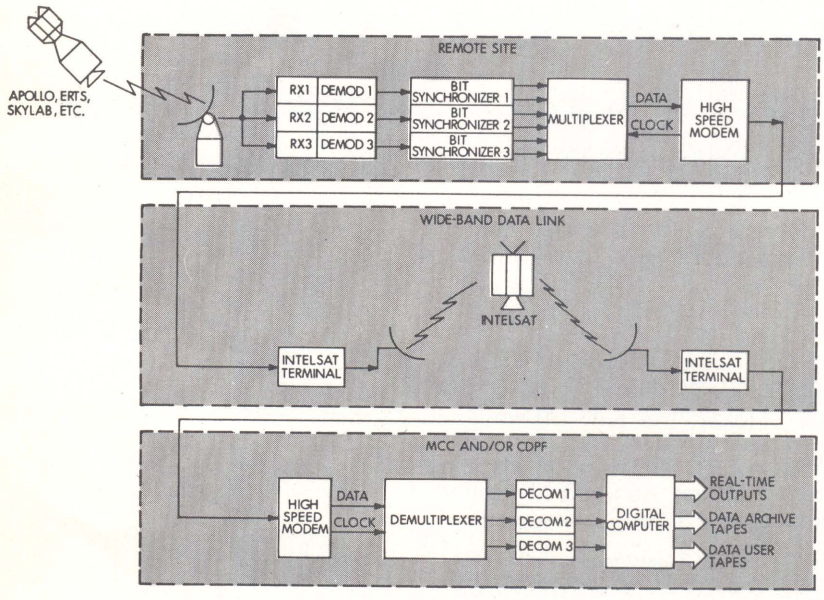
Where synchronization between multiple original data sources is difficult to achieve, the multiplexing/demultiplexing system described provides a cost-effective technique for combining asynchronous serial data systems into a single bit stream

By combining the asynchronous data bit streams from a plurality of independent input data sources and outputting the data as a single, higher rate bit stream, a highly efficient communications system can be achieved. Such a system can relieve the increasingly acute overcrowding of the frequency spectrum, and permit more effective allocation of remote units or terminals in time-shared systems.

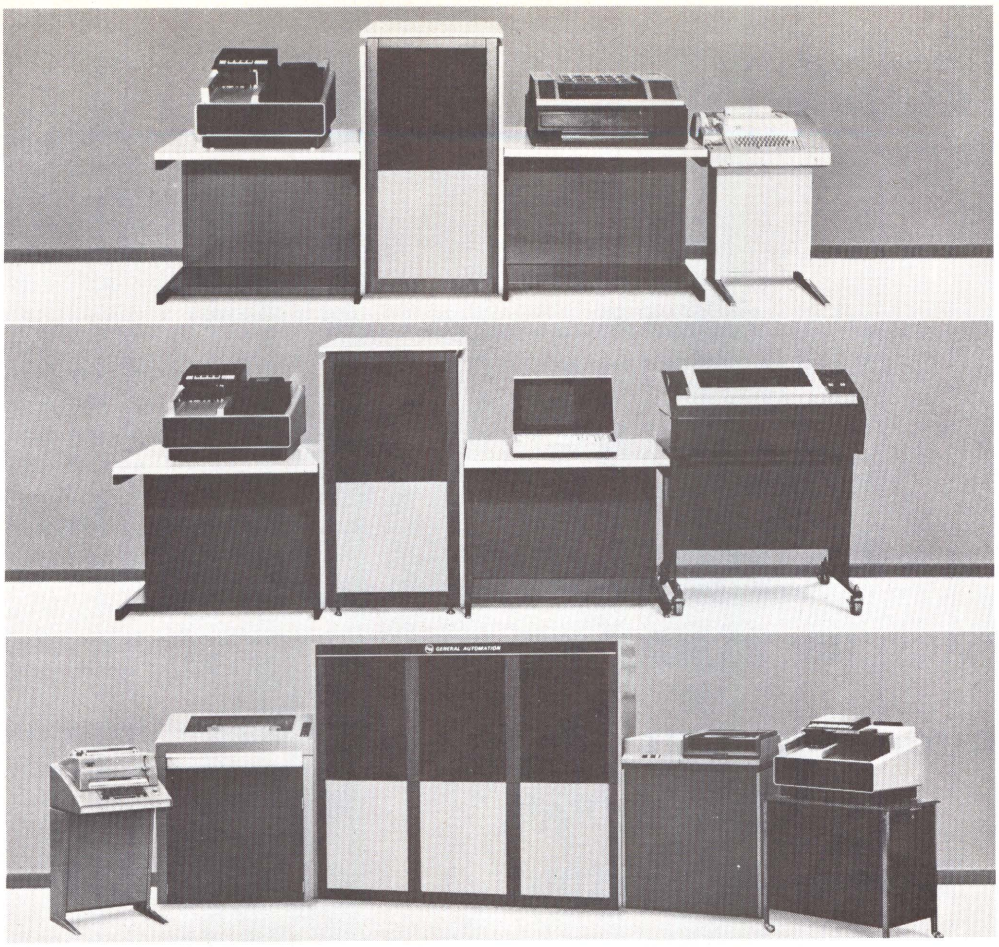
The multiplexing/demultiplexing system stores the data input signal from each input source temporarily until a block of data comprising a predetermined number of bits becomes available for a particular input source. This initial storage is accomplished by using an independent clock signal for each input from a standard bit synchronizer. After storage of a block of input data, a "label" bit pattern, unique to each source, is appended. In this way, the data sources are multiplexed as blocks of information rather than bit-by bit (or character-by character), and the distinctive label permits proper demultiplexing at the reception point. The multiplexing system also has the capability of switching to an operating condition wherein useful overhead data (eg, coding check bits or low priority data) are output when no input channel has sufficient source data to be processed.

Since data are shifted into the multiplexer by their own clock signals, data rate variations have no effect on system operation. In fact, even burst telemetry can easily be accommodated. The system permits up to three pulse-code modulated (PCM) bit streams to be multiplexed and can also be used for any non-return-to-zero (NRZ) coded data, with maximum output rate of 953 kilobits/s and maximum single input channel bit rate of 461 kilobits/s. (These limitations are imposed by selecting an internal clocking rate at 1 megabit/s, and may be increased if desired.) A relatively short (≈100 bits) data block length is utilized in the system.

A number of attractive commercial applications for the time-division multiplexing system exist. For example, the multiplexer could be utilized in a time-shared urban communications system comprising a central communications office, diverse field stations or terminals (eg, police, fire, utilities, transportation facilities), and a central data base. Other possible applications are in a system for transmitting computer input/output information between central data processing facility and remote terminals, and in an air traffic control system for establishing communications between a group of aircraft and a central receiver/processing station via a single communications link (eg, relay satellite). □



Asynchronous time-division multiplexing system can be used to combine digital data transmitted by a spacecraft on several RF downlinks into a single high bit-rate signal for transmission to a mission control center (MCC) or a central data processing facility (CDPF)



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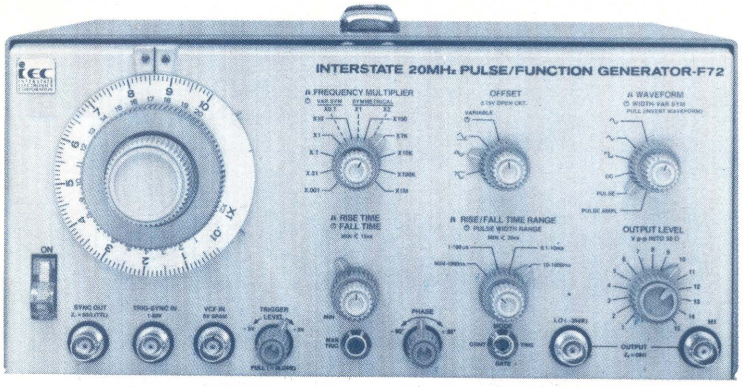

Function Generator Features Variable Rise/Fall, True Pulse Output

Reported to be the only function generator currently available with variable rise/fall "true" pulse output, the model F72 pulse/function generator, introduced by Interstate Electronics Corp, also features a pulse amplifier mode output. Like other models in the series 70 line, this instrument provides high-quality pulses from 20 μHz to 20 MHz in 10-decade ranges with constant width setability and separately adjustable rise/fall slopes.

Pulse rise and fall times are selectable from 15 ns to 1 s (with aberrations $\leq$5%), and adjustments are separately variable within any range up to 100:1 with respect to each other. Constant pulse width can be established from 30 ns to 1 s in four ranges. An advantage of the 1-s pulse width offered by the F72 over the 10-ms pulse width offered by the other models in the series is that it can be used rather conveniently with clip-on logic testers where the lights blink across the case. The eye can follow 1-s time periods, whereas it cannot observe 10-ms variations.

All waveforms may be inverted via a front panel switch without affecting the offset setting. Variable rise/fall trapezoids, 100:1 ramps, and other waveform patterns can be generated for testing magnetic memories, measuring amplifier slew rates, and performing IC tests.

In the pulse amplifier mode, low-level input signals of any random rate and width are regenerated as clean, fast rise/fall pulses with any desired amplitude or offset. With this special capability, any kind of signal can be input that is at least 1 V pk-pk, and the squaring circuit will square the waveshape and make it into a variable rise that will fall with variable offset or unipolar + or − with full attenuator range. In essence, this is a power amplifier for the input signal.

Other capabilities of the instrument include sine, square, and triangle outputs with variable symmetry control to 1 MHz, simultaneous hi/low outputs, constant duty cycle pulses, dc level waveforms, instant complementary pulses, 1000:1 VCF, and external synchronization. Variable symmetry mode allows 5 to 95% time symmetry adjustment of the square waveform (as well as sine and triangle for function generator applications), while maintaining selected duty cycle independent of frequency changes. With the simultaneous output arrangement, the auxiliary "low" output is 30 dB less than primary (hi) amplitude which is determined by the output level pot with a continuous vernier range of 30 dB. Total attenuation is 60 dB, and both ports can be used simultaneously. The instrument is a 50-Ω source and can be connected directly to ECL and other logic circuits without requiring a terminating resistor interface. Since peak voltage is 30 V open circuit, the back-terminated high output can drive MOS circuitry. Trigger and gate modes feature adjustable trigger level and slope controls for oscilloscope-style triggering.

Other Specifications

Dial accuracy varies from 1 to 3% of full scale ±1 or 2% of setting, depending on range chosen. Time symmetry is $\leq$1% to 20 Hz; $\leq$0.5%, 20 Hz to 100 kHz; and $\leq$2%, 100 kHz to 2 MHz.

Offset controls provide unipolar positive, unipolar negative, or bipolar waveforms with variable offset to ±15 V into an open circuit. Combined signal plus offset must lie in the region between + and − 15 V open circuit, ±7.5 V into 50 Ω. Max output of bipolar waveforms is 30 V pk-pk into open circuit or high impedance loads, 15 V pk-pk into 50-Ω loads.

The F72 is offered in both a benchtop model (11¼″ W x 15″ D x 6″ H) and a rack model (fits in 5¼″ rack space; 12¾″ behind the panel; 2¼″ in front of panel). Weight is 16.5 lb. It operates on ac power only, 50 to 400 Hz, 50 W max. A slide switch on the rear of the unit allows selection of four operating voltage ranges: 90 to 110 V, 104 to 126 V, 180 to 220 V, or 208 to 252 V.

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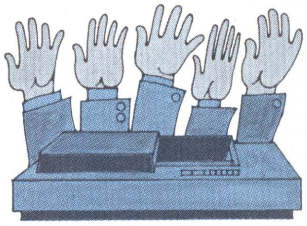

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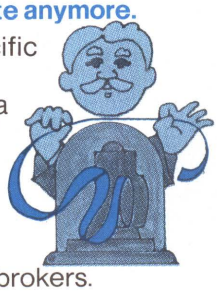

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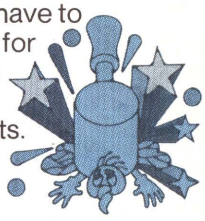

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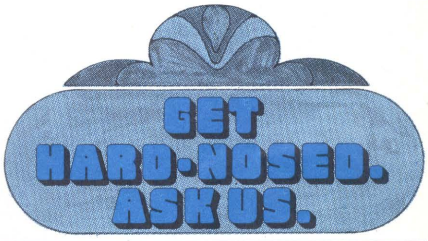

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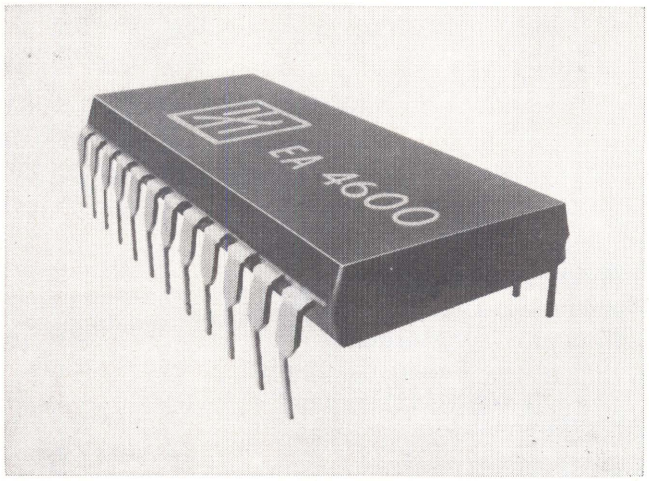
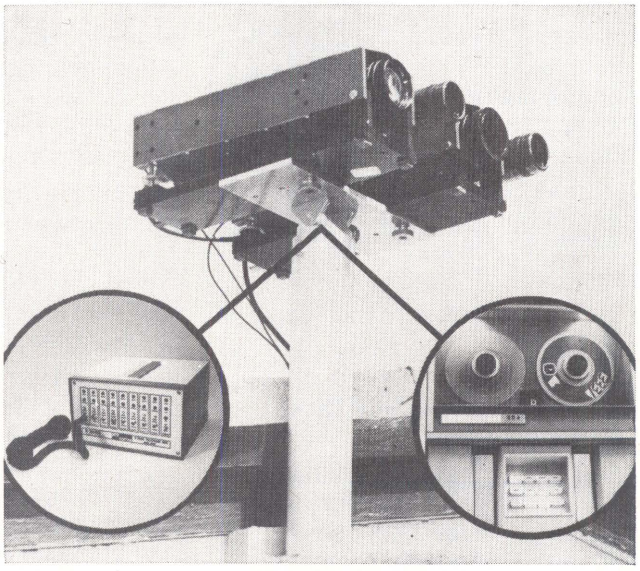
16-Kilobit Static ROM Has 550-ns Access Time



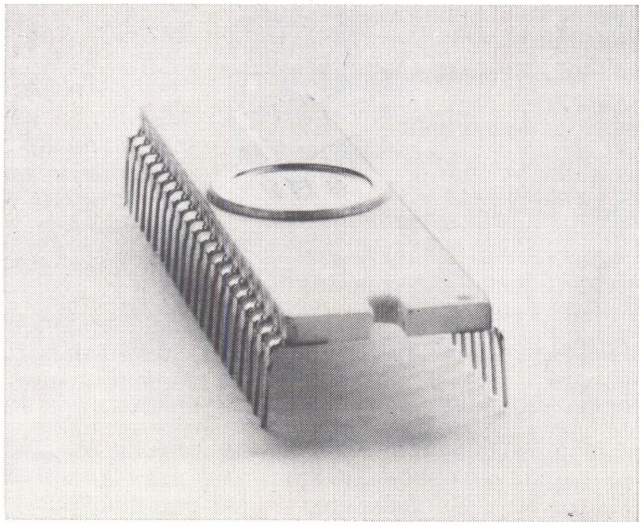
The EA4600 monolithic, n-channel ROM—with a guaranteed worst-case access time of 550 ns—is claimed to be the fastest 16K ROM on the market. Completely static in operation, it can be operated in clocked or unclocked mode. Its 3-state TTL-compatible outputs can be OR-wired. Outputs appear and remain in steady-state condition until a new address is read. Organization is 2048 addresses with eight output lines; the 2048-word x 8-bit organization can be converted to 4096 x 4. TTL compatibility features include ability to operate on a single 5-V power supply. Full address decoding is performed on chip. Programming is accomplished by use of one custom mask during device fabrication. Device size enables usage in high density, fixed memory applications. Power dissipation is as low as 0.03 mW/bit (1.25 W total hermetic, 24-pin DIP; 0.8 W in molded configuration). Ambient op temp range is 0 to 70°C for commercial version, −55 to 125°C for the military. **Electronic Arrays, Inc,** 550 E Middlefield Rd, Mountain View, CA 94043.
Circle 200 on Inquiry Card

Long-Range Laser Data System Is Low Cost Alternative to Microwave



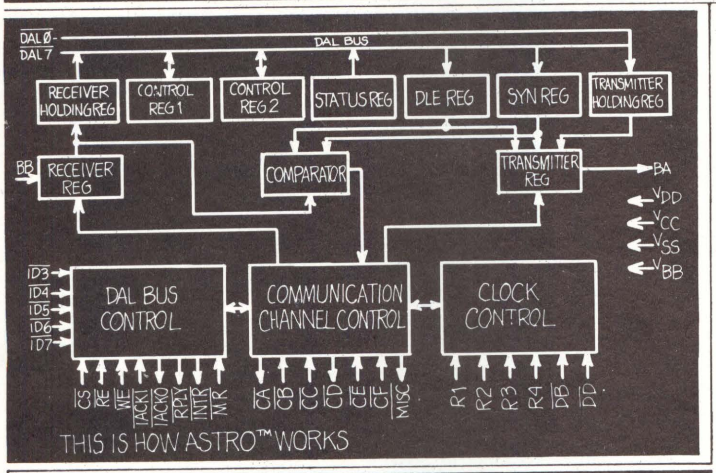
Capable of transmitting information on 120, 4800-baud channels simultaneously, model 741 long-range GaAs laser data communicator system provides data error rates as low as 10^{-10}. An IR-coherent laser beam, operated at 9000 Å, transfers data over line-of-sight distances up to 15 miles at rates to 1.544 megabits/s. This secure method of data or voice communication provides a license-free alternative to microwave in multichannel telephone (24 channels PCM) or high speed computer data transmission. Transmitter and receiver are packaged separately and each unit is supplied with alignment base and telescope; alignment requires about 15 min. Operation can be simplex, duplex, or repeater. Extended range or communication over and around obstacles such as buildings or mountains can be attained by patching the digital output of the receiver to the subsequent transmitter to form a repeater station. The transmitter triggers on the leading edge of the input pulse, and for every pulse into the transmitter, a pulse is produced at the receiver output. Virtually all types of digital data inputs can be accepted. Optical beam width is 2.5 mR. **American Laser Systems, Inc,** 106 James Fowler Rd, Goleta, CA 93017.
Circle 201 on Inquiry Card

8080-Compatible Microprocessor Includes Multibyte Interrupt Instruction Capability



A full 78 instructions for the μCOM-8 provides flexibility for use in control systems, computer peripherals, or communication systems. The device is TTL compatible; complemented by a line of RAMs, ROMs, and I/O circuits; and supported by an effective documentation package. Although the n-channel, Si-gate, 8-bit microprocessor is software compatible with the Intel 8080, it also features BCD subtraction as well as addition, and 2-μs register-to-register transfer. Multibyte interrupt instruction capability permits any address in memory to be used as a starting location for an interrupt processing program; a separate location can be assigned for every interrupt operation. A designer's evaluation kit, including complete documentation package and program card, eases programming. A single PC card in the kit holds CPU, six 8-bit latch drivers, 1 kilobyte of RAM, 1 kilobyte of ROM, crystal-controlled clock, test points, status displays, and other circuitry. Operation can begin after adding dc power supplies and a teletypewriter. **NEC Microcomputers, Inc,** 5 Militia Dr, Lexington, MA 02173.
Circle 202 on Inquiry Card

Thanks to our bright engineers, we may have just cut our datacom chip sales in half.



THIS IS HOW ASTRO™ WORKS

They Made a Universal Interface Chip. Now We're Selling One Chip Instead of Two.

Everyone thought our MOS/LSI UART's were great. Then our engineers thought it would be nice if we also came out with two synchronous/asynchronous devices. One (SAT) was a transmitter; the other (SAR), a receiver.

But people kept telling them two chips were too much trouble. There had to be an easier, more flexible way. We said it couldn't be that difficult to get computers and terminals to talk to each other. They said it was.

So at great expense our brilliant crew produced an Asynchronous/ Synchronous Transmitter/Receiver and cleverly named it ASTRO (UC1671).

Of course, while they were at it, they threw in a few more previously expensive goodies. They gave it full duplex capabilities so nothing had to wait.

After spending all this time to create it, they gave it IBM bisynch compatibility and transparent mode capability so you wouldn't see it anyway.

Details They Said You'd Like

ASTRO had to talk with computers. So they gave it a bus-oriented architecture. They fixed it so 32 ASTRO's could be addressed on bus and gave it a simplified interrupt and priority structure. So the processor wouldn't be slowed down, ASTRO was double buffered. And to top it off, ASTRO can operate at 1 Megahertz. Both modes have selectable 5-8 bit characters. Asynchronous mode allows 1, 1-1/2, or 2-stop bit selection. There are eight selectable clock rates, with up to 40% distortion allowance with 32X clock. Of course, all inputs and outputs are TTL compatible. It's all done using n-channel technology and comes in a 40-pin package.

Actually, It Was All Rather Cunning.

To tell the truth, we are well aware of the fact that not everyone will use an ASTRO to replace a UART, SAR, or SAT. Sometimes, they are all you'll need. And we recognize that ASTRO will take away business from the competition.

But that's how the high cost of technical leadership pays off. The denser the chip, the more problems you can help solve.

The Smart Company with the Dense Chips.

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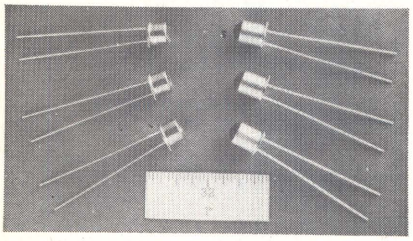
CIRCLE 49 ON INQUIRY CARD

PRODUCTS

INFRARED LEDs

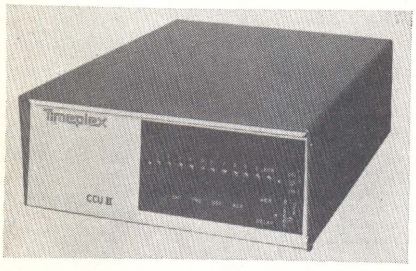


Fabricated with liquid epitaxial GaAs LEDs, LED55 and -56 series produce noncoherent infrared energy at 9400 Å, and are available in hermetically sealed packages with either flat or lens cap configurations. Guaranteed power output is 5.4 mW min at 100 mA; storage and operating temp capability is to 150°C. Both series are exact replacements for SSL55 and -56 series. **General Electric Co, Semiconductor Products Dept,** Electronics Pk, Bldg 7, Syracuse, NY 13201.
Circle 203 on Inquiry Card

FIELD-PROGRAMMABLE LOGIC ARRAY

Allowing high complexity, multiple-level gating to be quickly interconnected in a single monolithic structure, the IM5200 can be electrically programmed in the field. It has 14 inputs and 8 outputs, with a total of 48 product terms, providing a complexity of more than 480, 4-input logic gates. Packaged in a 24-pin Cerdip, the device is pin-compatible with the 7576 mask-programmable logic array, uses a single 5-V supply, and has typ propagation delay of 65 ns. **Intersil, Inc,** 10900 N Tantau Ave, Cupertino, CA 95014.
Circle 204 on Inquiry Card

AUTOMATIC COMPUTER-CALLING UNIT



An 801 replacement, the CCU II, in addition to std 801 features, provides for multiple dial-tone operation, call-progress indicators, built-in 103 or 202 type modems, optional serial-dialing interface, and optional calling-line selection. All features can be obtained in either a desktop (standalone) or rack-mounted card model. **Timeplex, Inc,** 100 Commerce Way, Hackensack, NJ 07601.
Circle 205 on Inquiry Card

TTL COMPARATOR

With 12-ns guaranteed propagation delay, the Am686 offers 5-mV accuracy and permits data rates of >80 MHz. Output skew is <2 ns. An input stage latch circuit provides a direct sample/hold function. The circuit has differential analog inputs and complementary logic outputs compatible with Schottky TTL. Output current capability is adequate to drive five std Schottky inputs. **Advanced Micro Devices Inc,** 901 Thompson Pl, Sunnyvale, CA 94086.
Circle 206 on Inquiry Card

REPACKAGED FLOPPY DISC SYSTEM

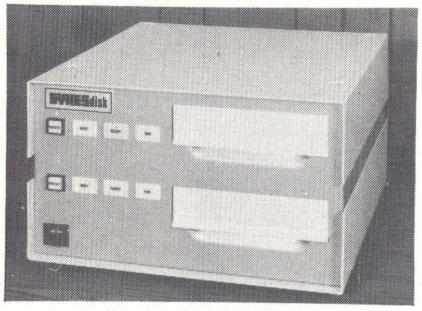
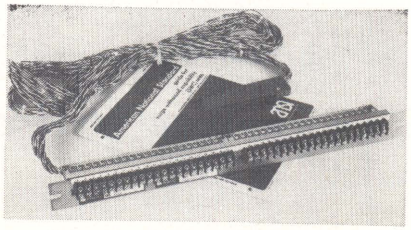


Table-top or rack-mount package for SYKESdisk 7000 family houses up to two disc drives, power supply, computer interface, and a controller which performs automatic sector search, record blocking, generation/check of IBM sync/CRC chars, address verification prior to reading or writing sectors, head unload when not transferring data, and bootstrap command. The system is IBM compatible, with 77 tracks/26 sectors/128 bytes of 8 bits each, 2-megabit capacity per disc, 250-kilobit transfer rate, 360-rpm rotational speed, and double-frequency recording. **Sykes Datatronics Inc,** 375 Orchard St, Rochester, NY 14606.
Circle 207 on Inquiry Card

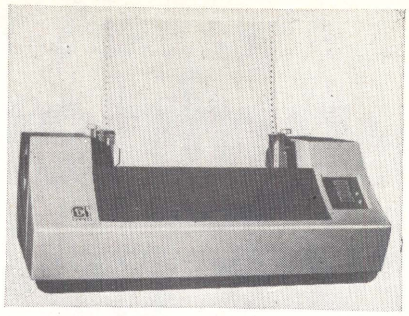
SIGNAL LINE TERMINATOR

RTP7506 barrier-terminal strip cable assemblies meet the 3-kV surge-withstand capability tests as specified by ANSI C37.90a-1974 (IEEE Std 472-1974). Designed for use with -7400 analog/digital input controllers, each cable assembly consists of a 1.75" high, 19" wide panel, 10 ft of interconnecting cable, and a hooded card-edge connector that is plug-compatible with analog and digital input cards. Panel contains surge protection components and barrier terminal strips to terminate sensor signal lines. **Computer Products,** 1400 NW 70th St, Fort Lauderdale, FL 33307.



Circle 208 on Inquiry Card

PLUG-COMPATIBLE PRINTER SYSTEM

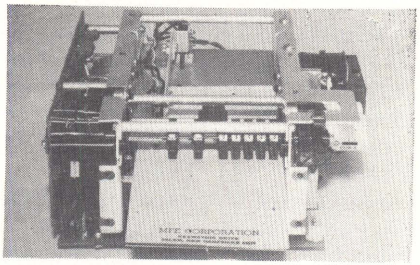


Offering more characters per second than comparable IBM models, the 165 is plug-to-plug compatible with IBM 3270 systems, and is said to offer performance superior to IBM 3284-1,2/3286-1,2 printers. Use of IBM model 3271-72/series 1-2 controllers makes any future software changes or communications protocols totally transparent to the system. Also featured are vertical forms control, line of bold face chars on command, visual/audio alarm system, adjustable platen that accommodates 4 to 14⅞" paper, and a 9 x 7 dot matrix. **Camco Equipment Inc,** 900 Walt Whitman Rd, Melville, NY 11746.
Circle 209 on Inquiry Card

DISC MEMORIES

10/16 series fixed-head magnetic disc memories, with access times that range from 4.2 to 16.8 ms and capacities from 1 to 40 megabits, are plug-compatible with DG Nova 2, 800, 830, 840, 1200, Super Nova, and Eclipse; DCC-116; DEC PDP-8, -11, and -12; and Interdata 70, 74, 80, 7/16, 7/32, 8/32, 80, and 85. A patented, fail-safe head-lifting mechanism eliminates head contact and minimizes crashes. **Alpha Data Inc,** 20750 Marilla St, Chatsworth, CA 91311.
Circle 210 on Inquiry Card

DIGITAL TICKET PRINTERS



Models TK5E and -11E accept ac or 12-Vdc power and convert parallel-entry BCD data inputs into printed form on a ticket that consists of a tab card plus two copies. Peak power of under 70 VA makes the printers particularly suitable for operation in automobiles and trucks. An absolute optical encoder senses drum position; logic is TTL. Printing solenoids are designed for high reliability and speeds to 1 line/s, continuous duty. Total data matrix is 11 col x 28 lines. **MFE Corp,** Keewaydin Dr, Salem, NH 03079.
Circle 211 on Inquiry Card

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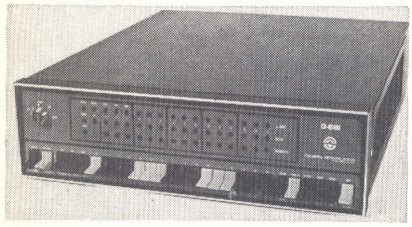
CIRCLE 50 ON INQUIRY CARD

PRODUCTS

CORE MEMORY SYSTEMS

Designed for compatibility with General Automation's SPC-16 CPUs, models A8K16MM (16K bytes) and A16K16MM (32K bytes) are identical in form, fit, and function to core supplied by the mainframe manufacturer and are completely pin compatible with all sub-models in the SPC-16 family. Pin-compatible std core memory systems are also available in a 16-kilobyte format for SPC-18 systems. **Standard Memories Inc,** 2801 E Oakland Pk Blvd, Fort Lauderdale, FL 33306.
Circle 212 on Inquiry Card

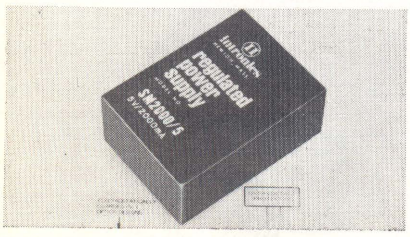
MINICOMPUTERS



D-216, -316, and -416 are available as a computer-on-a-board or as a fully built-up minicomputer. -316 and -416 offer up to 32K words of MOS RAM and core memory, respectively, on a single PC board, along with CPU, power monitor/auto restart, auto program load, and teletypewriter interface. Byte parity checking is std on MOS RAMs. p/ROM-ROM-RAM combinations are available on the -216. 660-ns -616 features multi-bank/multi-ported memories, enabling simultaneous, full-speed memory access by CPU and I/O. **Digital Computer Controls Inc,** 12 Industrial Rd, Fairfield, NJ 07006.
Circle 213 on Inquiry Card

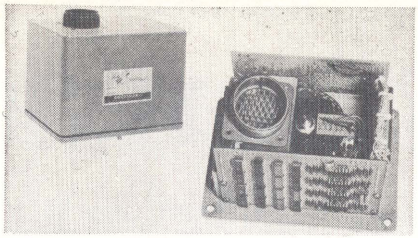
MODULAR POWER SUPPLY

Featuring 2-A output current capability at 5 Vdc in a 2.5 x 3.5 x 1.56" encapsulated module, the SM2000/5 provides static line and load regulation of 0.02 and 0.1%, respectively, making it suitable for reference use in many systems. Added features include output short-circuit protection, foldback current limiting, and overvoltage protection. The unit may be used with plug-in sockets or soldered directly to a PC board. Options include operation from various input voltages. **Intronics, Inc,** 57 Chapel St, Newton, MA 02158.



Circle 214 on Inquiry Card

PROGRAMMABLE OPTICAL ENCODER

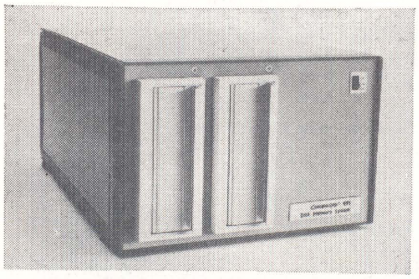


Decitrack[R] POE series encoders permit users to program the BCD output using an external thumbwheel switch. An electronic function within the unit multiplies the BCD output by any 3-decade number of .001 to .999. The programming feature offers speed and flexibility in applying the encoder to a range of industrial control applications. Output is supplied in parallel BCD-format at TTL levels in ranges from 999 to 999999. Each range can be multiplied by a 3-decade number, scaling each output number. **Theta Instrument Corp,** Fairfield, NJ 07006.
Circle 215 on Inquiry Card

FAST 4K NMOS STATIC RAM

Featuring 350-ns cycle time and 200-ns max access time, 4402, organized as 4096 words by 1 bit, uses a fully static memory cell which eliminates need for any refresh or charge-pump circuitry. Device is supplied in a std 22-pin DIP. All inputs are TTL compatible, except for chip select which requires a 12-V level. Two complementary data-out signals are provided to drive a differential amp. **EMM SEMI, a div of Electronic Memories & Magnetics Corp,** 3883 N 28th Ave, Phoenix, AZ 85017.
Circle 216 on Inquiry Card

FLOPPY DISC EXTENDED MEMORY



Developed for the company's 400 series plus Monroe 1800 programmable calculators, internal memory portion uses 4K RAMs to package 8 kilobytes of memory into the machines; external memory interfaces up to four floppy disc drives to provide >1.2 megabytes max available to the computer on a rapid, random-access basis. DOS—a complete file management system —allows the programmer to converse with the disc in terms of files and records, and to access records based on numeric or alphanumeric keys. **Compucorp,** 12401 W Olympic Blvd, Los Angeles, CA 90064.
Circle 217 on Inquiry Card

FREQUENCY CONVERTERS

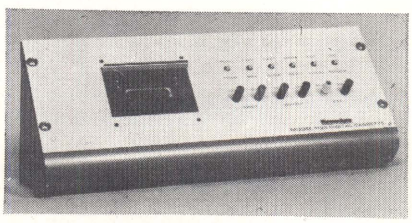
FZ series converters feature a ferroresonant transformer that results in less circuit complexity and greater reliability, and provides a high degree of noise isolation, current limiting, very good waveform shaping, and inherent static-voltage regulation. Changing the available power source frequency to a fixed 50-, 60-, or 400-Hz output, the units are rated from 200 to 3000 VA and offer voltage step-up, step-down, or direct one-to-one conversion for 115- or 230-Vac inputs. **Topaz Electronics,** 3855 Ruffin Rd, San Diego, CA 92123.
Circle 218 on Inquiry Card

SERIAL IMPACT BAR CODE PRINTER

For random-input short runs of black/white bar-coded labels, model 8124 features an integral p/ROM microprocessor for program flexibility and fulfillment of custom requirements. Unit prints on paper labels or perforated tags in continuous-roll form using a dry carbon ribbon to produce bar codes with high visual contrast and sharply defined edges. Printer can be equipped with a 31-char set basic keyboard; a full alphanumeric keyboard can be added. **Interface Mechanisms, Inc,** 5503 232nd St, SW, Mountlake Terrace, WA 98043.
Circle 219 on Inquiry Card

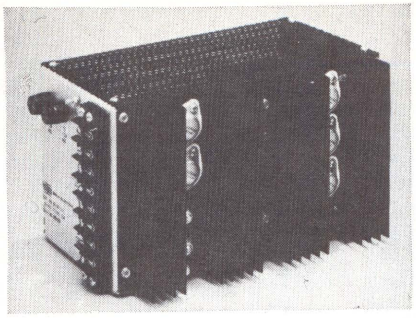
CASSETTE RECORDER BREADBOARD PACKAGE

Philips cassette breadboard package consists of a model 763 transport, all electronic circuitry, power supplies, control switches, and in/out connections for direct interfacing into computer systems and terminals. Circuitry includes a servo drive for moving tape bidirectionally at 20 or 120 in./s and 5% stability; and read/write amps for two channels capable of handling PE, complementary return to bias, NRZI, pulse ratio, and other types of saturation digital coding. **Memodyne Corp,** 375 Elliot St, Newton Upper Falls, MA 02164.



Circle 220 on Inquiry Card

IC-REGULATED POWER SUPPLY

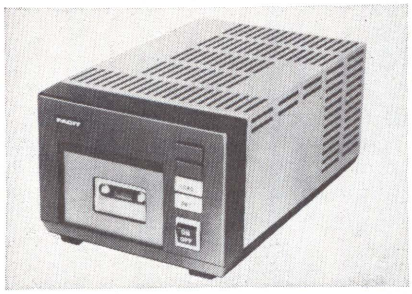


Premier line of class 82 supplies offers a low-priced alternative where less stringent regulation, ripple, and tempcos are required. Nine models in two chassis configurations provide outputs ranging from 4.8 V/25 A to 50 V/3 A. Combined line/load regulation is rated at 0.2%, ripple at 0.1% Vrms, and tempco at 0.03%/°C. Input voltage range is 120/240 Vac ±10% and input frequency range is 47 to 420 Hz. Op temp is 0 to 55°C. **Sola Electric, div of Sola Basic Industries,** 1717 Busse Rd, Elk Grove Village, IL 60007.
Circle 221 on Inquiry Card

FLAT BUS CABLE

Specially designed for electronic and data processing applications, Flurobuss cable is a continuous hot-melt extrusion of a fluorocarbon resin (FEP, Tefzel, and PFA) over copper bus, achieving specific adhesion to copper. Resulting high bond greatly increases resistance to scrape abrasion and notch sensitivity; adhesion makes the cable non-wicking and non-hosing. High heat-dissipation capability provides increased ampacity ratings. **Hitemp Wires, Inc,** 1320 Motor Pkwy, Hauppauge, NY 11787.
Circle 222 on Inquiry Card

CASSETTE TAPE UNIT

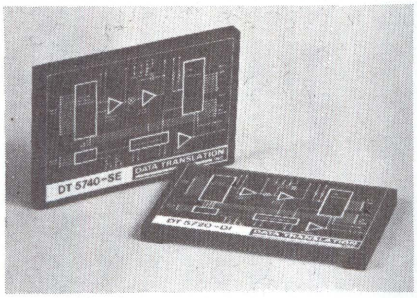


Fully ECMA compatible, the 4203 includes an interface that eliminates a number of transmission lines by transmitting control signals over existing data lines. Both recording format and cassette design follow the ECMA-34 standard. Packing density is 800 bits/in.; tape speeds are 3.75 and 7.5 in./s. The unit can be equipped with 256-char buffer for char-by-char operation. It measures 8½ x 6¼ x 13¾", and weighs 20 lb. **Facit-Addo, Inc,** 501 Winsor Dr, Secaucus, NJ 07094.
Circle 223 on Inquiry Card

DUAL-CHANNEL OPTICAL ISOLATORS

Model 5082-4354/55 incorporates two detectors with common ground and supply voltage pins, and two LEDs in an 8-pin package. Dc electrical insulation between input and output is 2500 V. Separate connections for photodiode bias and output transistor collectors reduce base-collector capacitance, increasing speed up to 100 times. For use in TTL/CMOS, TTL/LTTL, or wide-bandwidth analog applications, the -44 has a current transfer ratio of 7% min for I_F of 16 mA; -55, for TTL/TTL applications, has a CTR of 15% min. **Hewlett-Packard Co,** 1501 Page Mill Rd, Palo Alto, CA 94304.
Circle 224 on Inquiry Card

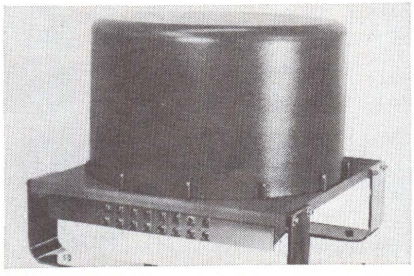
DATA ACQUISITION MODULES



Using laser-trimmed thin-film resistor networks to achieve guaranteed linearity over its entire temp range, DATAX II, models DT5720 and -5740, offer throughput speeds of 50 and 25 kHz, respectively. Intended for use with microcomputers, the device features 3-state outputs in 8-bit bytes, 12-bit resolution, ½ LSB linearity from 0 to 70°C, and system accuracy of 0.03% of full-scale range. Differential nonlinearity is ±2 ppm/°C. **Data Translation Inc,** 109 Concord St, Framingham, MA 01701.
Circle 225 on Inquiry Card

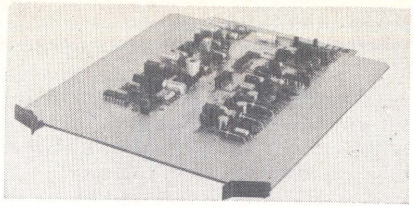
MILITARIZED DISC MEMORY SYSTEM

Storing up to 4 megabytes of data with avg access times of 8.5 to 17 ms, the head-per-track M6000 system is self-contained with electronics for reading, writing, track selection, and timing generation. Rapid on-site expansion or repair is possible because of modular design. The unit is interface and plug-compatible with the company's current products. **Digital Development Corp,** 8615 Balboa Ave, San Diego, CA 92123.



Circle 226 on Inquiry Card

PRODUCTS



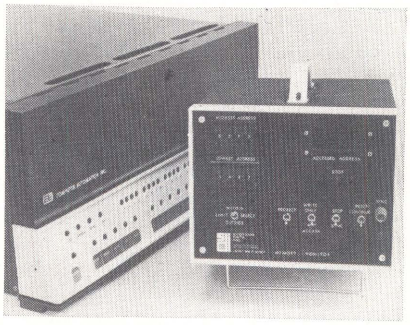
500-KILOBIT COAXIAL-CABLE MODEM

CM-500K allows data transmission at any bit rate from dc to 500 kilobits over distances of 40,000 ft on single-conductor coaxial cable without repeaters. Modems are coupled to the cable such that hundreds of units can be connected without disturbing cable characteristics. Fm-carrier transmission provides immunity to electrical noise in difficult environments; grounding of the cable's output conductor permits safe operation of all devices connected to the transmission link. **Computrol Corp,** Berkshire Industrial Pk, Bethel, CT 06801.
Circle 227 on Inquiry Card

DIGITIZER INTERFACE

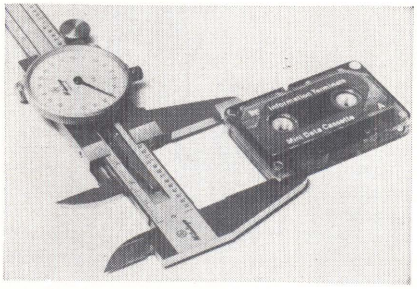
A plug-in card which allows direct communication between the E241 graphic data digitizer and acoustical coupler, modem, terminal, or computer, the E241-11 provides digitizer output in std 7-level ASCII code with both 20-mA current loop and RS-232 signaling provided simultaneously. Board-selectable options include baud rates from 110 to 1200, one or two stop bits, selectable parity, and coordinate pairs per line select. **Elographics, Inc,** 1976 Oak Ridge Tnpk, Oak Ridge, TN 37830.
Circle 228 on Inquiry Card

MINICOMPUTER MEMORY MONITOR



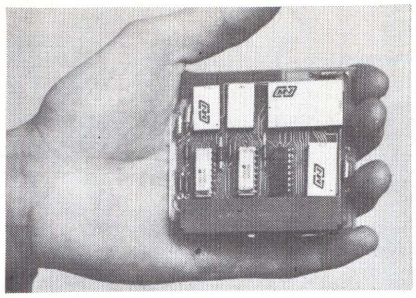
Attaching to the expansion interface connectors of Computer Automation LSI series minicomputers, the model 8000 provides memory protection and monitoring functions on any group of up to 32K words addressed through hexadecimal thumbwheel switches. A hexidecimal LED address display and sync pulse output are provided. Stop mode operation causes the LSI processor to stop if selected memory accesses are executed; sync pulse output permits rapid, accurate timing of program instructions or sequences. **Systems Data, Inc,** 1941 W Market St, Akron, OH 44313.
Circle 229 on Inquiry Card

THUMB-LENGTH DIGITAL CASSETTE



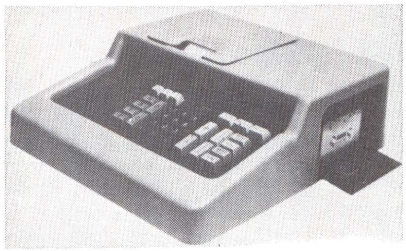
2 x 1.3 x 0.3″ in size, MI-50 Mini Cassette has a plastic case which holds 50′ of usable storage on 0.15 x 0.7-mil tape. A cavity is provided for a read-after-write head. Precision-ground tape guides promote trouble-free recording at 0 to 30 in./s. Data capacity is 32 kilobytes/track, recording at 500 bits/in.; transfer rate is 1 kilobit/s at 2 in./s. **Information Terminals Corp,** 323 Soquel Way, Sunnyvale, CA 94086.
Circle 230 on Inquiry Card

16-CHANNEL, MINIATURE DATA ACQUISITON SYSTEM



Measuring 3.15 x 2.75 x 0.45", 12-bit MNA-7000 and -7000H provide a 40% reduction in board-mounting space. The 7000 is rated for 0 to 70°C operation, while the -H is rated for the full −55 to 125°C range. Both units guarantee linearity to ±1 LSB over the full op temp range, as well as ±½ LSB linearity around 25°C. Users can control mux mode (single-ended or differential) with a logic signal. Mux protection circuitry enhances reliability in event of power failure. **Micro Networks Corp,** 324 Clark St, Worcester, MA 01606.
Circle 231 on Inquiry Card

CASSETTE RECORDER DATA ENTRY DEVICE



The portable, desk-top model 77 KTC is an offline source-data entry device, for use in conjunction with magnetic tape cassette computer system. The unit contains keyboard, display, and optional printer. The std 300′ tape, ECMA-34 compatible cassette accommodates approx 3000, 16-char data blocks on each side. Operator controls include 10-key numeric cluster, negative sign, clear, six non-add and two accumulating terminator keys, two subtotal and two total keys, and two grand-total keys. **Sweda International, OEM Products Div,** 34 Maple Ave, Pine Brook, NJ 07058.
Circle 232 on Inquiry Card

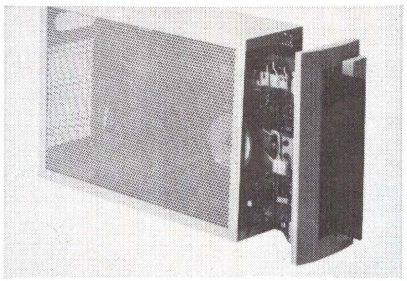
DIGITAL DATA SET

The LDS 309, for local-loop or private-line transmission, is available for point-to-point (or multi-point) applications that do not involve a centrally clocked digital network. Designed to comply with transmission signal levels of Bell 43401 at a transmission speed of 19,200 bits/s, the device is guaranteed to transmit at 9600 baud over 26-gauge wire for a distance of 8 miles. Features include self-test with an artificial line. **Gandalf Data Inc,** 466 Central Ave, #28, Northfield, IL 60093.
Circle 233 on Inquiry Card

MODULAR REAL-TIME CLOCK/ POWER-FAIL INTERRUPT

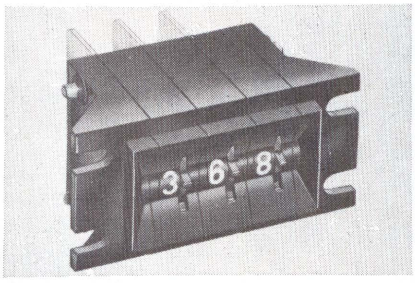
Expanding capabilities of MicroPac microcomputers, real-time clock and power-fail interrupt module detects power failure at least 500 μs before operation halts due to low power, and notifies the CPU so that a systematic shutdown program can be executed. The module also contains a switch allowing either cold start or restart upon resumption of normal power, and can tell the CPU the amount of charge in the backup battery pack. **PCS, Inc,** 5467 Hill 23 Dr, Flint, MI 48507.
Circle 234 on Inquiry Card

COMPACT, FLEXIBLE DISC DRIVE



GSI-105, a rugged, low cost random-access data storage/retrieval computer peripheral device utilizing a single, removable diskette as its storage medium, is designed to utilize the IBM-compatible format used in 3740 data entry systems and System 32, in addition to special formats tailored to user requirements. Incorporated are all analog read, write, and control electronics for performing data transfer operations using only simple control commands. **General Systems International, Inc,** 1440 Allec St, Anaheim, CA 92805.
Circle 235 on Inquiry Card

SUB-SUBMINIATURE THUMBWHEEL SWITCH



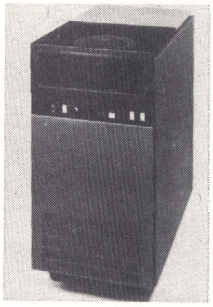
The compact series T-50 takes only 0.315 x 0.709" of front-panel space and 0.984" back-of-panel depth. Available in choice of BCD, 10-position decimal, single-pole repeating (+, −; 0, 1; or 0, 5), BCD with diode provision, and other common codes, its 0.158"-high white characters are easily read. Operating force is 7 to 10 oz, and mechanical life is 1 million detent operations min. Black gloss finish is std; grey or white are available. **Cherry Electrical Products Corp,** 3600 Sunset St, Waukegan, IL 60085.
Circle 236 on Inquiry Card

PRODUCTS

RANDOM ACCESS DISC MEMORY

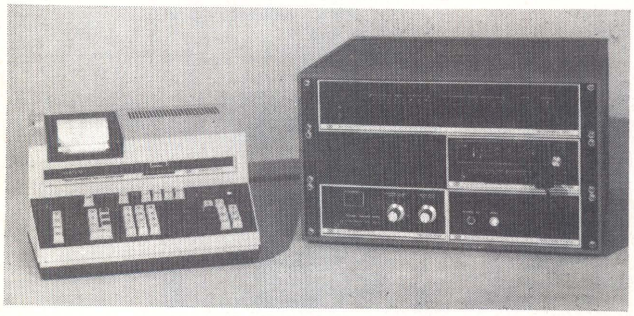
530M (military), designed for rugged use and reliable data storage in the up to 80-megabit range on 1024 data tracks, max, is modularized and can be supplied in incremental versions. It operates at 3600 rpm without sacrificing one-half of its inherent data capacity. 530C (commercial) is available with 40 megabits/512 data tracks max. Std for both are 2.6- to 5.2-MHz transfer rate, 1800/3600-rpm rotational speed, 3320-bit/in. max recording density, 8.5/16.7-ms avg access time, 15/2.5-g max (operating) shock/vibration, −25 to 140°F op temp range, up to 100% humidity with condensation, and 115/208 or 220/380 Vac, 50/60 Hz power requirements. **General Instrument Corp, Rotating Memory Products,** 13040 S Cerise Ave, Hawthorne, CA 90250.
Circle 237 on Inquiry Card

DISC DRIVE



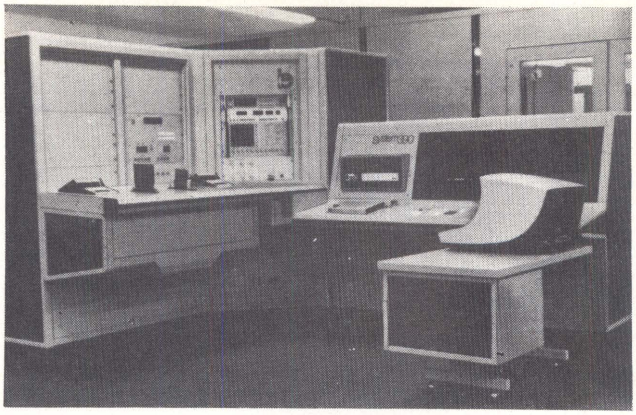
Designed to enhance information processing capabilities of MODCOMP computer systems, 3330-type compact, standalone unit with self-contained, regulated power supply features 28-ms access and 15-s start/stop times. Single-spindle design provides 84 megabytes of storage per drive, permitting increases in 84-megabyte increments by linking as many drives as required; up to four drives can run with each controller. A dual access option allows one drive to be connected to two controllers, enabling two computers to read and write on the same disc. Configurations include the drive alone; one drive and a single controller; a drive coupled with a dual access device; and a single drive, dual access option, and two controllers. **Modular Computer Systems, Inc,** 1650 W McNab Rd, Fort Lauderdale, FL 33309.
Circle 238 on Inquiry Card

CALCULATOR-BASED INSTRUMENT SYSTEMS



Series of plug-to-plug compatible instruments, interfaces, other hardware, and software allows the user to attain online measurement and computation capability at nearly the sophistication of a minicomputer system at a fraction of the cost. Heart of System 1 family is a full-function, fully programmable calculating unit (PCU) with paper-tape printer. With a memory of 512 words, expandable to 4K, PCU is integrally tied to an interface which permits direct connection of peripherals. Family can contain and control up to six DMMs and provide up to 160 channels of low level voltage (μV) and current (pA) input. Mag-card storage is std. System can be altered or expanded, and can be quickly disassembled and instruments used individually. Also, the operator can perform his own programming. **Keithley Instruments, Inc,** 28775 Aurora Rd, Cleveland, OH 44139.
Circle 239 on Inquiry Card

STANDARD AUTOMATIC TEST SYSTEM



Modular peripheral hardware under computer control, user-oriented test language, resident software, and flexible switching are features of System 390 model 70, which performs functional and dynamic digital and parametric tests on analog, digital, and hybrid circuits. A 2-family digital word generator/receiver allows testing of boards containing microprocessors, RAMs, and ROMs. System has access to any pin on a UUT for analog, high frequency, high/low speed digital, multiplexing, and multifixtures; operations are performed under program control without adapter or patch panels. Also included are a resident compiler, digital/analog fault isolation with guided probe, diagnosis of fault signatures, data logging, and online program editing/debugging. **Instrumentation Engineering, Inc,** 769 Susquehanna Ave, Franklin Lakes, NJ 07417.
Circle 240 on Inquiry Card

ADD-ON MEMORY FOR 370/158 COMPUTER

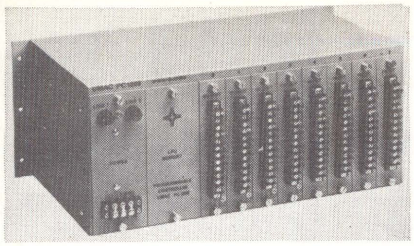
370/STOR 158-3, expandable in increments of 512 or 1024 kilobytes up to 3 megabytes per single chassis, can extend IBM 158 processor models J, JI, and K to their full 4-megabyte storage capacities. Reconfiguration panel capabilities enable users to duplex main storage on a single 158 under operator control, assuring availability of two separate memory systems for critical online applications at a far smaller investment. System speeds (duplicating 370/158) are 1035-ns cycle time (read 16 bytes), and 690 and 920 ns (write 8 and 16 bytes, respectively); other features include 16-byte word length; random access mode; 1024-bit/chip, n-channel MOS, static memory circuitry; and ECL circuitry. **Cambridge Memories, Inc,** 12 Crosby Dr, Bedford, MA 01730.
Circle 241 on Inquiry Card

8080 MICROCOMPUTER SYSTEM DESIGN TOOL

By emulating the Intel 8080 microprocessor, Econ 80 enables the user to develop 8080 programs and system logic needed for support and interfacing. Featured are continuous/single instruction modes, dc to 2-MHz system clock rates, and 8080 I/O-compatible interface. Programmer-oriented aids include built-in utilities for hexadecimal memory dump on TTY, list/modify memory, binary paper-tape dump of memory, load memory from paper tape, and verify paper tape. Engineering-oriented breadboard capabilities are high density prototype boards, multiple-voltage power supplies, and noncritical I/O bus drivers. User-oriented operator's console provides simultaneous display of all 8080 register contents, ability to alter contents of any 8080 register and display or alter contents of any memory location, and sophisticated program breakpoint capability. **Santek Systems,** 6645 Convoy Ct, San Diego, CA 92111.

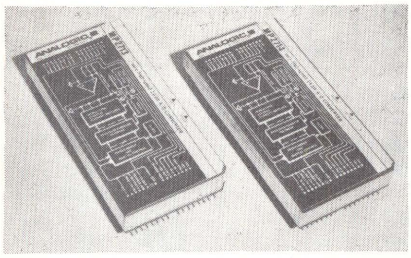
Circle 242 on Inquiry Card

COMPACT PROGRAMMABLE CONTROLLER



PC1200 replaces hardwired relay control panels for industrial machines/processes. It permits system revision/reprogramming without disturbing the equipment's control devices or cables, rewiring the control panel, losing program security, or destroying the old program. Modular system can handle 16 to 256 inputs and 8 to 256 outputs with or without timing and counting. 3-ms scanning during each control cycle eliminates delays associated with conventional relay response time. **Sperry Vickers Div of Sperry Rand Corp,** Troy, MI 48084.
Circle 243 on Inquiry Card

13-, 14-BIT A-D CONVERTERS



MP2713 and -14 feature digitizing rates to 100,000 conversions/s, with accuracies and differential linearities to 0.006% and <3 ppm/°C, respectively, achieved by incorporating three separate ground planes and a strobing comparator. Internal gain/offset adjustments are driven from a built-in precision reference supply. Design also includes low thermal rises, four full-scale, pin-selectable ranges, and Modupac^R construction (5-sided electromagnetic shielding, 6-sided electrostatic shielding for rfi/emi immunity). **Analogic Corp,** Audubon Rd, Wakefield, MA 01880.
Circle 244 on Inquiry Card

8-KILOBIT ERASABLE p/ROM

The 2708 is guaranteed to operate at worst-case access time of 500 ns over the 0 to 70° temp range. Power dissipation is typ 97 μW/bit. Reprogramming is done with a single high-voltage pulse per bit while the device operates at its std supply voltages of 5, −5, and 12 V, making the design fast and easy to program. Typ programming rate is 12 ms/bit; the entire memory can be programmed in approx 100 s. In addition, the design remains TTL compatible during programming. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.
Circle 245 on Inquiry Card

INTERMITTENTLY LAMINATED TWISTED-PAIR CABLE

Line of 3C laminated twisted-pair cable is laminated for approx 0.75", followed by 0.75" of unlaminated film, repeated along the cable length; loose areas of PVC film are left over unlaminated sections. Cutting across unlaminated portions frees twisted pairs of conductors for untwisting and conventional termination; termination is further simplified by the fact that no bonding is used between conductors, or between pairs. **Spectra-Strip Corp,** 7100 Lampson Ave, Garden Grove, CA 92642.
Circle 246 on Inquiry Card

REAL-TIME MICROCOMPUTER OPERATING SYSTEM

RTX12, designed to support the MP12 in dedicated real-time applications, provides comprehensive facilities for multi-task scheduling, function task support, I/O processing, and interactive operator control. Features include task scheduling by system clock, by external events, or by operator command; and ability to vary priority of any task in real-time. Combined with MP12 CPU, I/O routines, and std interface hardware, the system enables users to easily develop microcomputer-based systems. **Fabri-Tek Inc,** 5901 S County Rd 18, Minneapolis, MN 55436.
Circle 247 o nInquiry Card

MINIATURE FEED UNITS FOR LOGIC CIRCUITS

For direct installation on PC boards, units feature 10^{11}-Ω insulation resistance and low capacitance coupling between input and output, due mainly to a built-in current transformer. In conjunction with built-in secondary filter, transformer makes it possible to alternate input pulses with 1-kV amplitude and 2-μs duration by 100 dB and effect a reduction of 80 dB in normal interference up to 1 Hz. Output leakage current is 3 μA. **Ir H Stoet's Radio B V,** c/o The Netherlands Consulate General, Commercial Div 5987, One Rockefeller Plaza, New York, NY 10020.
Circle 248 on Inquiry Card

DISPLAY DRIVER

Combining features of CMOS and bipolar technology, the CD4511 is a BCD decoder/driver with an integral latch on a single chip. CMOS decoding functions and latch allow low input-current requirements and low power consumption. Bipolar output devices permit the circuit to source up to 25 mA of segment current. Logically, the device provides the functions of a 4-bit storage latch, BCD-to-7-segment decoder, and seven high current output drivers. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.
Circle 249 on Inquiry Card

PRODUCTS

SIGNAL GENERATOR WITH MICROPROCESSOR

Model 6010A features a keyboard that allows free-form entry of frequency in hertz, kilohertz, or megahertz. Programmed frequencies are read on a bright, 7-digit LED display. Entire output is programmable; up to 10 preset frequency modulation and amplitude levels can be stored and recalled using the keyboard. Also included is automatic range selection. When an entry is made, the unit automatically justifies the number on the readout to give the greatest possible resolution; frequencies range from 10 Hz to 11 MHz. Frequency selection or tuning is facilitated by a large, dual-concentric rotary knob; outer ring selects decade, inner selects digit. Decade being tuned is clearly indicated through a slightly brighter digit. Additional protection to the DUT is also provided. **John Fluke Mfg Co,** PO Box 7428, Seattle, WA 98133.

Circle 250 on Inquiry Card

INDUSTRY-COMPATIBLE 9-TRACK TAPE DRIVE

Model 2209, which reads and records in universal NRZI mode on reels to 10½" dia, is supplied with factory-supported software, eliminating need to program tape-handling operations and freeing users to concentrate on functional programming. Distributed data processing enables computer files to be run with BASIC programs for processing reports from a shared data base. Users can gather information through a satellite computer for later assimilation/processing by the CPU. Since each reel stores up to 20 million char, the tape drive is an excellent backup storage medium for disc files. Recording density is 800 bytes/in.; reading/recording speed is 12½ in./s, rewind to 150 in./s. Included are a built-in tape cleaner and dual-gap read/write head. **Wang Laboratories, Inc,** 836 North St, Tewksbury, MA 01876.

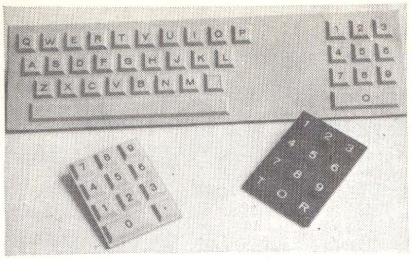
Circle 251 on Inquiry Card

LOGIC PROBE

PLP-550, a programmable, rugged, all-solid-state, hand-sized probe, uses lighted displays to indicate logic levels: red for "1," white for "0," none for the deadband between. Input impedance for all logic families is high enough to negate any loading effects. A pulse capture feature displays, by a blue "P," pulses as fast as 10 ns. Duty cycle information is interpolated by direct relationship to the intensity of the lamps. A std pulse "memory" feature allows the user to "catch" single-shot, short pulses that are nearly impossible to see. The probe exhibits excellent noise rejection and is suited to industrial environments. Frequency response is 50 MHz. **Kurz-Kasch, Inc, Electronics Div,** PO Box 1246, Dayton, OH 45401.

Circle 252 on Inquiry Card

ENVIRONMENT-PROOF KEYBOARDS

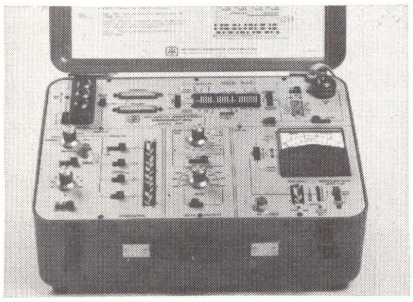


DK-M/MS series are designed for wet, dirty, or abrasive environments. Switching is performed by a patented conductive elastomer technique, whereby the elastomer is flexed through an aperture in a mylar insulation sheet and electrically bridges adjacent precious-metal fingers. Truncated keys and legends are molded in a single sheet of silicone. -M keys are solid for "touch switch" actuation; -MS keys flex for a key travel of 0.08" before switch closure. Switch outputs may be Form A or matrixed. **Flex-Key Corp,** 18 Sargent St, Gloucester, MA 01930.
Circle 253 on Inquiry Card

DIP DELAY LINES

In a std 14-pin DIP, delays ranging from 10 to 1000 ns are provided with 10 equally spaced taps for delays to 200 ns, 5 taps for longer delays. Delay-to-rise-time ratio is approx 6:1 for delays to 200 ns, 4:1 for 300 to 1000 ns. Impedance is 50 to 500 Ω, and op temp range is −55 to 125°C. Units are designed to meet applicable portions of MIL-D-23859 and are supplied for both military and commercial applications. **ESC Electronics Corp,** 534 Bergen Blvd, Palisades Park, NJ 07650.
Circle 254 on Inquiry Card

PORTABLE DATA COMMUNICATIONS TEST SET



Operating asynchronously or isochronously, Datec 9500 transmits up to four switch-selectable chars for terminal addressing and four 64-char test messages (Baudot, ASCII, EBCD, and EBCDIC). Signal distortion may be introduced and measured. At speeds to 9600 baud, unit also tests selectable-line-length printers. Any char may be selected and, when detected, a trap light is illuminated and the next char displayed on LED bit lights, thus giving verification of multiple-char responses. **Atlantic Research Corp,** 5390 Cherokee Ave, Alexandria, VA 22314.
Circle 255 on Inquiry Card

SCIENTIFIC CALCULATOR PLUG-IN CIRCUIT BOARD

A 22-pin, double-sided PCB plug-in module designed around an MPS-2529-002 scientific calculator chip, the SC-440 contains all interface circuitry necessary to access chip computing capability through external circuitry. The externally programmable board accepts ASCII inputs and has multiplexed BCD outputs; 3-state inputs and outputs provide easy access on a common data bus. It functions as microprocessor satellite or standalone calculating programmable controller/computer. **Scarpa Laboratories, Inc,** 46 Liberty St, Brainy Boro Station, Metuchen, NJ 08840.
Circle 256 on Inquiry Card

INTERACTIVE GRAPHIC DISPLAY STATION

Designed to operate with any Data General computer system, 1110 is an intelligent video storage terminal that provides easy viewing under amb lighting conditions. Any portion of the display may be selectively erased from the screen—a 21", high resolution, long life tube. Computer-generated commands are displayed on the screen; a prompting message guides the operator in making the proper command choice from fixed-tablet and dynamic electronic menus. **Algorex Data Corp,** 6901 Jericho Tnpk, Syosset, NY 11791.
Circle 257 on Inquiry Card

BI-PHASE DECODER

Featuring variable-speed, asynchronous operation for use with bi-phase coded data, the UBISYN decoder module accepts data at random rates from printed bar code, magnetic stripes, or transmitted data. The unit decodes while the bit rate is varied over a 100,000% range, allowing the use of hand-held wands, and is universally compatible with std and non-std alphanumeric char codes, fixed- or variable-length words, and random binary-data streams. **Digital Technology Group, div of Bitcil Systems, Inc,** 31218 Pacific Hwy S, Federal Way, WA 98002.
Circle 258 on Inquiry Card

CRYSTAL-CONTROLLED OSCILLATORS

CMOS-compatible, low-power voltage, and resistor-controlled temp-compensated oscillators as well as clock-type and oven-controlled devices are included in the line of TCXOs available in package sizes as small as 1.2 in.^{3} and in temp ranges from −30 to 85°C. Output options include sine wave, square wave, TTL and CMOS compatible. All units are guaranteed to age $<1 \times 10^{-6}$/yr, and, with the exception of the oven-controlled units, require no warm-up time. **Microsonics, a div of Sangamo Electric Co,** 60 Winter St, Weymouth, MA 02188.
Circle 259 on Inquiry Card

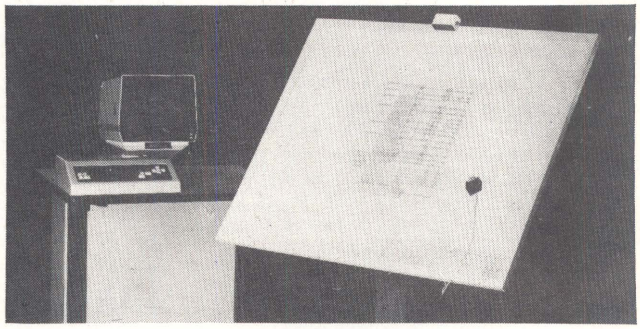
PRODUCTS

MINICOMPUTER WITH HIGH LEVEL LANGUAGE

Hitac 20 employs PL/I, edited for minicomputer applications and renamed PLUS (Programming Language for User's System). Microprogramming control and wide use of LSI are featured; and floating-point arithmetic adapter, hardware debug adapter, and I/O control adapter are all modular. Core memory processor has a 16-bit + 2-parity word length, 650-ns cycle time, and 8K- to 64K-word capacity; ACU has 90 (122 optional) 1- or 2-word instructions, 16 g-p registers, and 64K-word direct/relative/base/index/immediate addressing. Floating-point execution times are 32/64 bits addition/subtraction, 9 to 15 and 10 to 23 μs, respectively; 32/64 bits multiplication/division, 12 to 16 and 17 to 28 μs, respectively. Disc operating system, full utility, debug hardware, and console display are included. **Hitachi Ltd,** New Marunouchi Bldg, No. 5-1, 1-chome, Marunouchi Chiyoda-ku, Tokyo 100, Japan.

Circle 260 on Inquiry Card

LOW COST DIGITIZING TERMINAL



Large Tablet Digitizer (LTD), for input of graphic data to the company's Designer™ interactive graphics systems, has a 35 x 47″ active digitizer surface, including menu area. The head has no mechanical connection to the table, allowing freedom of operator hand movement. Any point on the surface has absolute, permanently defined coordinates. If power is interrupted, or if the operator lifts the cursor from the table, coordinates are not lost. Both puck and pen cursors are available, as are an echo CRT (11 or 19″ diag display screen) for checking and interactive editing; 12″ sq sketch pad tablet; Telewriter™ keyboard/thermal printer for operator commands, error message, and data printing; and a 16-key program function keyboard. **The Computervision Corp,** 201 Burlington Rd, Bedford, MA 01730.

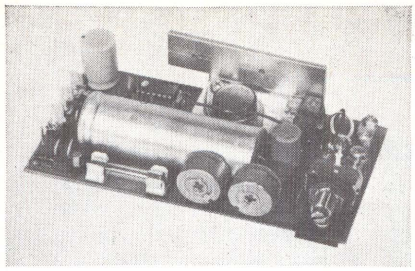
Circle 261 on Inquiry Card

MOS/CMOS PROTECTION DEVICES

TransZorb™ transient voltage suppressors for bipolar, MOS, and Schottky ICs are supplied in nine voltages from 5 to 45 V at std power supply levels and offer subnanosecond response, high surge capabilities (15 kW for 10 μs), and low clamping ratio. With internal system disturbances, devices prevent catastrophic failure or slow degradation of the input circuit. With external, protection is provided by placing a device in the power supply line; having a low "on" resistance, it will effectively short out unwanted transients while maintaining circuit voltage level. Max ratings include 1500-W pk pulse power dissipation at 25°C; op/storage temps of −65 to 175°C; forward surge of 200 A, 1/120 s at 25°C; steady-state power dissipation of 1 W; and repetition rate of 0.01%. **General Semiconductor Industries, Inc,** 2001 W Tenth Pl, Tempe, AZ 85281.

Circle 262 on Inquiry Card

SUB-MODULAR POWER SUPPLIES

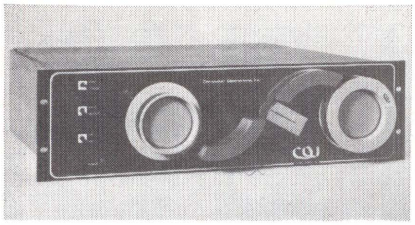


By breaking a power supply into its sub-modular elements and then standardizing these elements, custom power supplies can be economically and rapidly created. SMS series (42 models, 7 package sizes) provide outputs from 0 to 30 V, currents from 0 to 36 A. Features include built-in overvoltage protection, current-limiting overload protection, and adjustable controls. Line/load regulation is better than 0.075%, output ripple better than 1 mV rms. In most models, remote programming/remote sensing are std. **Power/Mate Corp,** 514 S River St, Hackensack, NJ 07601.
Circle 263 on Inquiry Card

SYNCHRO-TO-NON-VARIANT SIN/COS DC CONVERTER

Model STDC accepts 3-wire synchro or 4-wire resolver data and delivers ±10 Vdc at ±5 mA sine and cosine data accurate to ±12 min. (ratio sin/cos), even in the presence of ±3% input power variations and ±10% swing in input signal amplitude and frequency. Converter accepts synchro inputs (line-to-line) of 90 V at 60 or 400 Hz, or 11.8 V at 400 Hz. Synchro input angle rates are 0 to ±360 deg/s for 400-Hz units, 0 to ±60 deg/s for 60-Hz. Initial acquisition time is <25 ms. **ILC Data Device Corp,** Airport International Plaza, Bohemia, NY 11716.
Circle 264 on Inquiry Card

MASS STORAGE DEVICES



Model CO-3000D-11, for DEC PDP-11 computers, includes a built-in ROM bootstrap and is DECtape compatible; an RT-11 driver is optional, and the system requires only one SPC slot. CO-3000N, for Data General's Nova/Eclipse series, is available with software, permitting economical implementation of powerful program development operating systems (SOS/RDOS support), and requires only one device slot in the CPU. Both versions feature redundant phase recording on preformatted mag tape at 8400 bytes/s. Storage capacity is 335 kilobytes/drive. **Computer Operations, Inc,** 10774 Tucker St, Beltsville, MD 20705.
Circle 265 on Inquiry Card

SEMICONDUCTOR MEMORY TEST SYSTEM

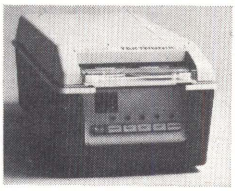
Performing a wide range of memory test patterns at a true 20-MHz rate, the model 203 can be used for functional and dc parametric testing, providing substantial margin of speed to test both current and future devices. Designed specifically for production testing and engineering evaluation of ROMs, RAMs, and shift registers, the system can perform such tests as surround disturb, walking diagonal, and N^2 test, actually exercising the memory at 20 MHz. **Siemens Corp,** 186 Wood Ave S, Iselin, NJ 08830.
Circle 266 on Inquiry Card

DATA ACQUISITION AND CONTROL SYSTEM WITH DMA

The 550-DGC contains a 12-bit A-D converter with high speed sample/hold that has a throughput rate of 100,000 channels/s. This, coupled with the DMA, provides max transfer rates between external devices and computer memory. Software and mechanically compatible with the DG Nova, Eclipse, 800, and 1200 series minicomputers, the device can contain up to 64 channels of single-ended, pseudo-differential multiplexer inputs, or 32 channels of true-differential inputs. **Adac Corp,** 29b Cummings Pk, Woburn, MA 01801.
Circle 267 on Inquiry Card

PRODUCTS

DIGITAL TAPE CARTRIDGE MEMORY



4923, an offline storage instrument that uses 3M's DC 300A tape cartridge, interfaces to computer graphics terminals; Option 1 version interfaces to the RS-232-C data communications line and an alphanumeric terminal. 4923 provides a means of having local program storage capability, supplies audit trail operations for monitoring communications between terminal and host computer, and is a buffer device for storing data from graphic tablets. Read/write speed is 30 in./s, fast forward/rewind 90 in./s, and storage capacity approx 243,000 8-bit bytes formatted into 128-byte records. A self-test feature verifies instrument operation. On the Option 1 model, a local/online switch allows the user to interface with the host computer without the 4923 being online. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97005.
Circle 268 on Inquiry Card

DATA COMMUNICATIONS SUBSYSTEM

Series of programmable data communications components allow the company's computer systems to be configured across all data communications applications. Included are three multiplexers, and the DCU/50 data control unit, which provides high-level data communications throughput with low CPU utilization and includes software for line control and user interface. Controller performs char processing and line protocol functions in parallel with a CPU or dedicated communication processor; it contains a 2048-byte bipolar RAM with 600-ns instruction speed for add/subtract, 900 ns for load/store. Multiplexers consist of the 16-line asynchronous ALM-16, 8-line asynchronous ALM-8 with full modem control, and the 2-line synchronous SLM-2. Components can be implemented singly or in combination. **Data General Corp,** Southboro, MA 01772.
Circle 269 on Inquiry Card

30-CHAR/S PRINTER TERMINAL

300/T is a table-top Diablo printer-based terminal incorporating performance features of the 300/S. A microprocessor with additional ROM controls left and right margins, vertical tab set/reset, bidirectional printing, graphics capabilities, super plot, 2-color ribbon, subscript, superscript, addressable horizontal/vertical tabbing, and variable-pitch and line feed spacing. Features may be controlled from Selectric™-style keyboard or communications line using std ASCII escape and control codes. The size of a Selectric typewriter, unit weighs 53 lb and is supplied in a carrying case. **Data Terminals and Communications,** 1190 Dell Ave, Campbell, CA 95008.
Circle 270 on Inquiry Card

LITERATURE

CMOS ICs

116-page data book contains updated specs on std gates, buffers, flip-flops, shift registers, switches, arithmetic functions, and memories, plus advance information on new products. **Solid State Scientific Inc,** Montgomeryville, Pa.
Circle 300 on Inquiry Card

Data Conversion Products, Product Design

Catalog/handbook on modular data conversion products, logic- and line-powered digital panel instruments, and industrial digitizing systems/instruments includes a designer reference guide. **Analogic,** Wakefield, Mass.
Circle 301 on Inquiry Card

Programmable Calculating Oscilloscope

Brochure explains how the NI 2001, in a single mainframe, combines microprocessor capabilities with digital measurement to provide quick, accurate analysis of even the most complex electrical data. **Norland Instruments,** Fort Atkinson, Wis.
Circle 302 on Inquiry Card

Contact System

Brochure illustrates and describes various uses made of the Dura-Con system, which involves contacts as small as 0.163" long x 0.019" dia for AWG 34 wire and spacing on 0.025" centers. **TRW/Cinch Connectors, an electronic components div of TRW Inc,** Elk Grove Village, Ill.
Circle 303 on Inquiry Card

Thermocompression Bonder

Catalog describes model designed for ease of operation and high production versatility in thermocompression bonding of LSI beam-leaded devices as well as external lead frames, regardless of dimensional variations. **J. and A. Keller Machine Co, Inc,** Buffalo, NY.
Circle 304 on Inquiry Card

Power Transistors

120-page user's guide provides practical information on circuit application, handling/mounting, and reliability for complementary pairs, darlington, and high voltage types, both metal and plastic encapsulated. **General Electric Semiconductor,** Syracuse, NY.
Circle 305 on Inquiry Card

Single-Chip, 16-Bit Microprocessor

PACE, which contains control logic, four working registers (accumulators), 10-word stack, and interrupt control circuitry, is described in brochure which includes photos and functional block diagram. **National Semiconductor Corp,** Santa Clara, Calif.
Circle 306 on Inquiry Card

Automatic Testers

Hustler series for semiconductor devices is detailed in brochure which includes technical background, testing philosophy, principal features, and comparison with competitive devices. **Datatron, Inc,** Santa Ana, Calif.
Circle 307 on Inquiry Card

Custom CMOS Circuit Design

Designing circuits with the company's predesigned/preprocessed MasterMOS array is explained in guide which also cites applications. **International Microcircuits, Inc,** Santa Clara, Calif.
Circle 308 on Inquiry Card

Connector System

Brochure describes capabilities and components of Scotchflex brand Delta system, said to be the first to provide simultaneous assembly of flat, flat-woven, or jacketed cable with up to 25 conductors. **3M Co,** St. Paul, Minn.
Circle 309 on Inquiry Card

Pushbutton Switch Modules

Technical specs, options, and drawings of 2-, 4-, 6-, and 8-pole modules, available with push-push, momentary, interlocking, and blockout switch functions, are detailed in catalog. **Standard Grigsby, Inc,** Aurora, Ill.
Circle 310 on Inquiry Card

Thermoplastic Parts Production Process

Designer's handbook outlining advantages of Rigid Foam process gives comparative properties plus specs regarding stiffness parameters, moment of inertia, modulus of elasticity, and stiffness increase through expansion. **Gulf + Western Manufacturing Co, FCM Div,** Grand Rapids, Mich.
Circle 311 on Inquiry Card

Dual-Density Transports

Illustrated brochure details 9000 series 7- or 9-track, read-after-write transports, which offer a choice of NRZI, PE, or NRZI/PE formats. **Kennedy Co,** Altadena, Calif.
Circle 312 on Inquiry Card

High Performance, Low Cost Microcomputer

MP12, a complete functional unit with 4096 12-bit words of core memory and a comprehensive software set, is detailed in data sheet. **Fabri-Tek Inc,** Minneapolis, Minn.
Circle 313 on Inquiry Card

Card-Edge Connector

Technical bulletin describes 24-contact miniature mono-block connector designed for flat cable or PC board solder terminations. **Hugh H. Eby Corp, div of REDM Corp,** Philadelphia, Pa.
Circle 314 on Inquiry Card

Data Acquisition Front-End

The 5600, which measures up to 1000 low-level inputs with superior noise rejection, and which can be remoted up to 1 mi with a single twisted pair, is described in brochure. **Vidar Autodata, Inc,** Mountain View, Calif.
Circle 315 on Inquiry Card

Op Amps, Converters

Product catalog includes op amps, ADCs, DACs, analog comparators, instrumentation amps, absolute-value modules, 3-mode integrators, analog dividers and multipliers, S/H memories, and more. **Optical Electronics, Inc,** Tucson, Ariz.
Circle 316 on Inquiry Card

Automatic Circuit Card Testing

Booklet on economies to be gained from testing circuit cards automatically, compares manual testing, a computer test system, and an automatic test system. **Technology Marketing Inc,** Costa Mesa, Calif.
Circle 317 on Inquiry Card

Microprocessor Data

First-quarter-1975 update of "Microprocessor Field Survey and Data Book" includes CPU data on 23 products from 21 manufacturers. **AH Systems Inc,** Chatsworth, Calif.
Circle 318 on Inquiry Card

Engineering Products

104-page 1975 reference catalog provides detailed data plus engineering and mil specs for more than 20,000 items. Write Sid Fleischman, Vice President-Sales, **Herman H. Smith, Inc, a North American Philips co,** 812 Snediker Ave, Brooklyn, NY 11207.

GUIDE TO PRODUCT INFORMATION

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