COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

SEPTEMBER 1975
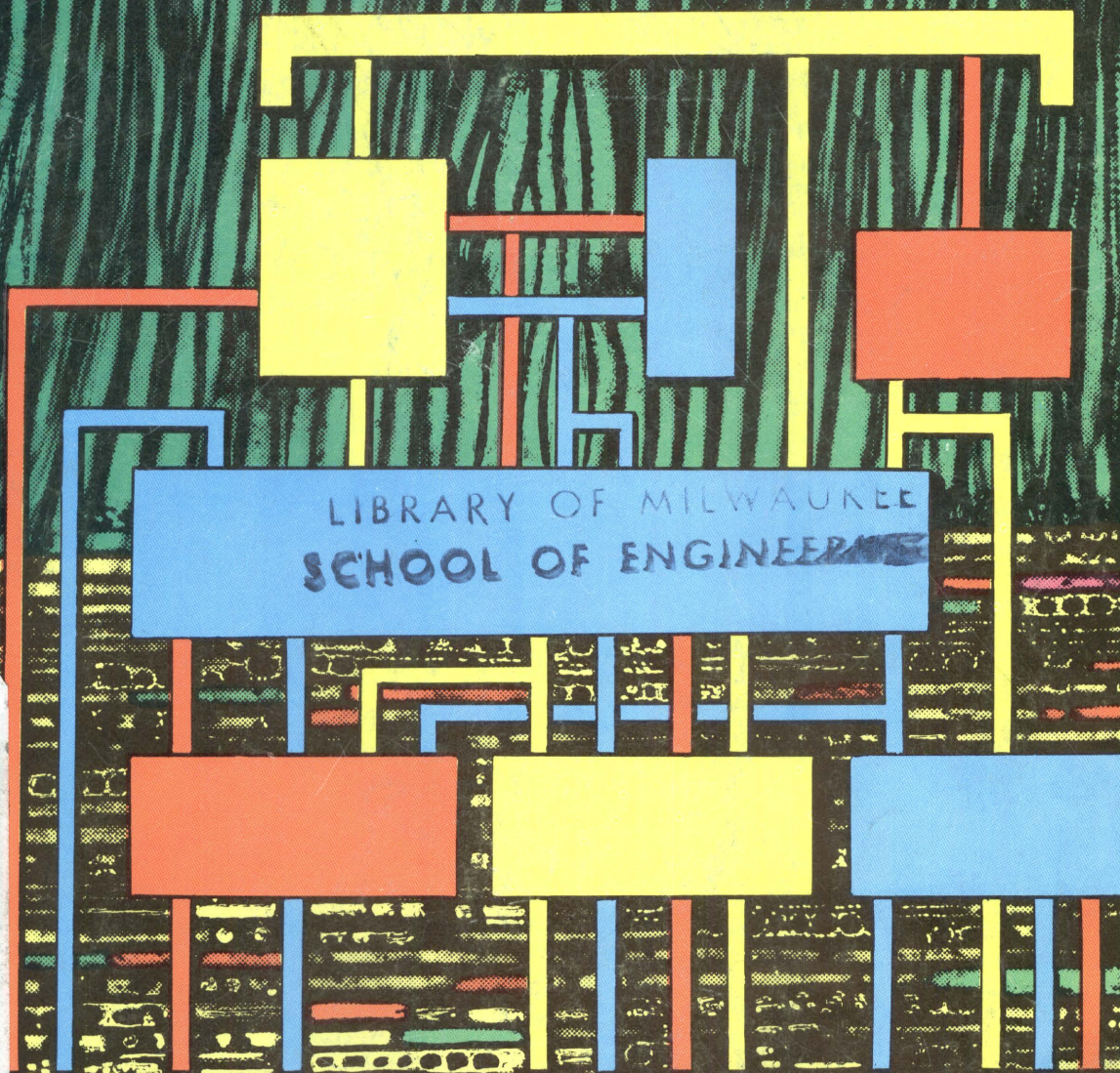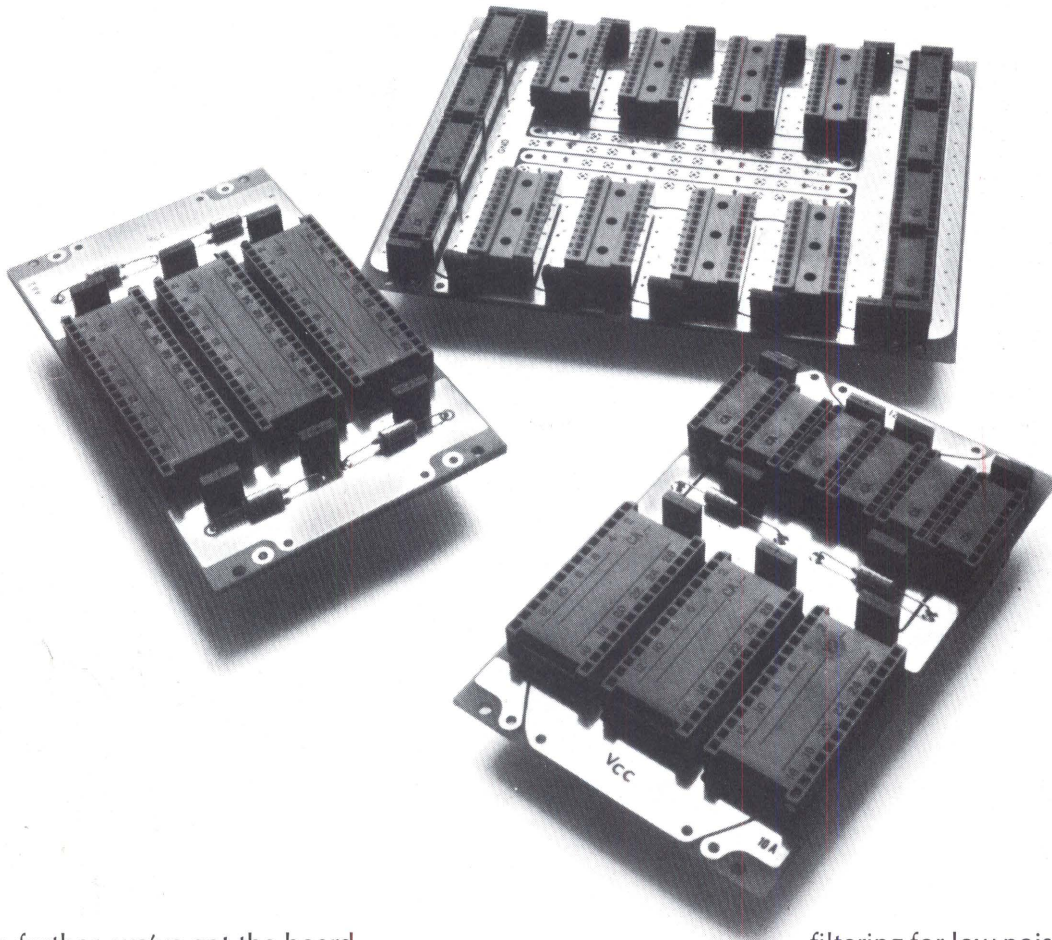
USING A MICROPROCESSOR: A REAL-LIFE APPLICATION • PART 1—HARDWARE

BUILDING TODAY'S TECHNOLOGIES INTO A LARGE-SCALE TIME-SHARING SYSTEM

PARALLEL CRC LETS MANY LINES USE ONE CIRCUIT

THE
MAGAZINE
OF DIGITAL
ELECTRONICS

COMPUTER
DESIGN

SEPTEMBER 1975 ● VOLUME 14 ● NUMBER 9

Reader Service and Subscription Cards pages 143-146

Reduce Your Power Supply Size and Weight By 70%

A new way has been found to substantially reduce power supply size and weight. Consider the large power supply shown at left in the above photo — it uses an input transformer, into a bridge rectifier, to convert 60 Hz to 5 volts DC at 5 amperes. This unit measures 6½″x4″x7½″ and weighs 13 pounds. Abbott's new model Z5T10, shown at right, provides the same performance with 70% less weight and volume. It measures only 2¼″x4″x6″ and weighs just 3 pounds.

This size reduction in the Model Z5T10 is primarily accomplished by eliminating the large input transformer and instead using high voltage, high efficiency, DC to DC conversion circuits. Abbott engineers have been able to control the output ripple to less than 0.02% RMS or 50 millivolts peak-to-peak

maximum. This design approach also allows the unit to operate from 100 to 132 Volts RMS and 47 to 440 Hertz. Close regulation of 0.15% and a typical temperature coefficient of 0.01% per degree Celsius are some of its many outstanding features. This new Model "Z" series is available in output voltages of 2.7 to 31 VDC in 12 days from receipt of order.

Abbott also manufacturers 3,000 other models of power supplies with output voltages from 5 to 740 VDC and with output currents from 2 milliamps to 20 amps. They are all listed with prices in the new Abbott catalog with various inputs:

60 ∿ to DC
400 ∿ to DC
28 VDC to DC
28 VDC to 400 ∿
12-28 VDC to 60 ∿

Please see pages 307-317 Volume 1 of your 1974-75 EEM (ELECTRONIC ENGINEERS MASTER Catalog) or pages 853-860 Volume 3 of your 1974-75 GOLD BOOK for complete information on Abbott Modules.

Send for our new 60 page FREE catalog.

How To Turn On Your Intellec MDS...Today!
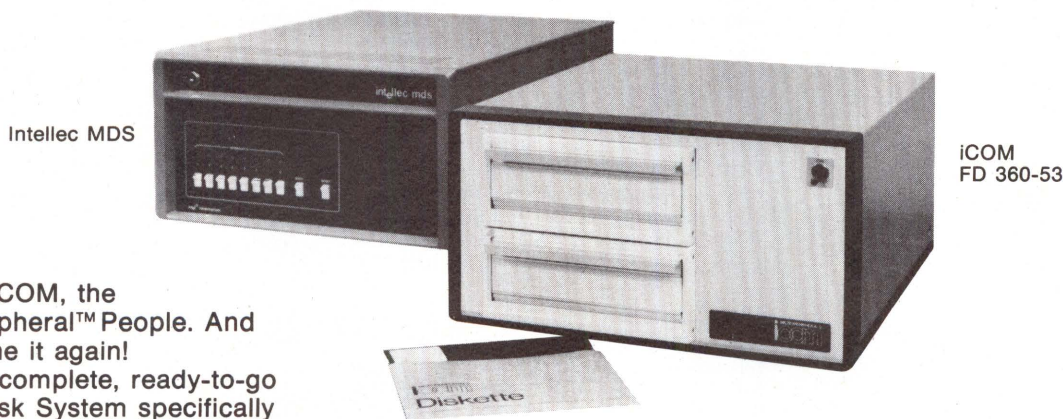
Intellec MDS

iCOM
FD 360-53

We're iCOM, the Microperipheral™ People. And we've done it again!

With a complete, ready-to-go Floppy Disk System specifically designed for Intel's new MDS-800 Microcomputer.

It can be installed in 5 minutes. It's fully hardware and software compatible. And it contains the most powerful Floppy Disk Operating System (FDOS) available anywhere.

FDOS-II on a diskette

The powerful FDOS-II software is supplied on a ready-to-use diskette and includes an assembler and editor along with a sophisticated file manager. Within minutes after unboxing your iCOM system, you'll have available all of the FDOS-II features such as auto file create, open and close; file lengths variable from a single sector up to an entire diskette; named files with attributes; multiple file merge or delete; automatic disk packing; disk-to-disk copy; disk-to-memory load; tape-to-disk and disk-to-tape transfer. Plus lots more.

Easy interface

The iCOM FD360 Floppy Disk System connects easily to the Intel

MDS-800 through our interface card which plugs directly into the MDS chassis. The interface card is furnished with a PROM pre-loaded with the floppy disk driver software. You also get the cable which connects the interface card to the iCOM Floppy Disk System. You might say we've thought of everything.

Some more good news

The controller/formatter portion of the system is fully IBM 3540 and 3740 format *and* media compatible. Special features include separate read & write data buffers, hardware track seek & verification, and complete hardware CRC

generation & verification. Storage capacities range from 256K bytes to over 1 million bytes.

The best news – price & delivery

A single drive system, including all software and the MDS interface card, is just $2650. The dual drive system is only $3300. And delivery is 2 to 4 weeks! We also have a 250 cps paper tape reader (Model R80MDS) for just $895. So why wait? Call or write today for more information. The sooner you order your iCOM Floppy Disk System, the sooner you can "turn on" your Intellec MDS-800.

MICROPERIPHERALS™

icom

6741 Variel Avenue, Canoga Park California 91303 • (213) 348-1391

iCOM Microperipherals™ mate with these microcomputers:

- Intel 8080, 8008, Intellec 8, and MDS-800
- PCS Micropac 80A
- Motorola M6800
- National IMP
- Fairchild F-8

CALENDAR

Sept 22-24—5th Internat'l Sym and Exhibits on Industrial Robots, Illinois Institute of Technology, Chicago. **Information:** Society of Manufacturing Engineers, 20501 Ford Rd, Dearborn, MI 48128. Tel: (313) 271-1500

Sept 30—Invitational Computer Conf, Marriott Motor Hotel, Newton, Mass. **Information:** B. J. Johnson & Assoc, 300 Otero, Newport Beach, CA 92660. Tel: (714) 644-6037

Oct 6-8—NCF/NEC: Nat'l Communications Forum/Nat'l Electronics Conf, Hyatt Regency O'Hare, Chicago. **Information:** NEC, Suite 103, 1301 W 22nd St, Oak Brook, IL 60521. Tel: (312) 325-5700

Oct 6-9—ISA-75: Instrument Soc of America Conf & Exhibit, Mecca Hall, Milwaukee, Wis. **Information:** ISA, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

Oct 7-8—9th Annual Instrumentation & Computer Fair, Sheraton Inn/Washington-Northeast, Washington, DC. **Information:** Robert Harar, Exec Dir, Instrumentation Fair, Inc, 5012 Herzel Pl, Beltsville, MD 20705. Tel: (301) 937-7177

Oct 7-9—IEEE Computer Soc 4th Data Communications Sym, Hotel Le Concorde, Quebec City, Quebec. **Information:** Dr Tom B. Grandy, Bell-Northern Research, PO Box 3511, Station C, Ottawa, Ontario, Canada K1Y 4H7

Oct 7-9—IEEE Internat'l Sym on Electromagnetic Compatibility, El Tropicano Hotel, San Antonio. **Information:** EMC, PO Drawer 28510, San Antonio, TX 72284

Oct 13-14—Information Processing Assoc of Israel (IPA) 10th Nat'l Data Processing Conf, Binyanei, Ha'ooma, Jerusalem. **Information:** NDPC, c/o Kenes Ltd, PO Box 16271, Tel Aviv, Israel

Oct 13-14—16th Annual Sym on Foundations of Computer Science, Claremont Hotel, Berkeley, Calif. **Information:** Sheldon B. Akers, General Electric Co, Bldg 3, Rm 223, Electronics Park, Syracuse, NY 13210. Tel: (315) 456-3067

Oct 14-16—IEEE Internat'l Conf on Advanced Signal Processing Technology, Lausanne, Switzerland. **Information:** Secretariat Journees d'Electronique, Ch de Bellerive 16, 1007 Lausanne, Switzerland

Oct 20-22—Internat'l Security Conf, New York Hilton Hotel, New York City. **Information:** ISC, 2639 S La Cienega Blvd, Los Angeles, CA 90034. Tel: (213) 836-5000

Oct 22-23—8th Annual Connector Sym, Cherry Hill Inn, Cherry Hill, NJ. **Information:** Electronic Connector Study Group, PO Box 1428, Camden, NJ 08101

Oct 23-24—2nd Nat'l Sym on Management of Data Elements in Information Processing, NBS, Gaithersburg, Md. **Information:** Mrs Hazel McEwen, Institute for Computer Sciences and Technology, National Bureau of Standards, Washington, DC 20234. Tel: (301) 921-3157

Oct 24-25—American Society for Quality Control Workshop for Commercial Users of ICs, Downtowner Motor Inn, Durham, NC. **Information:** Dr Ralph A. Evans, IC-QC Workshop, 804 Vickers Ave, Durham, NC 27701. Tel: (919) 688-2860

Oct 27-29—ISHM Technical Sym, Sheraton-Towers Conv Ctr, Orlando, Fla. **Information:** International Society for Hybrid Microelectronics, PO Box 3255, Montgomery, AL 36109. Tel: (205) 272-3191

Oct 28-30—22nd IEEE Machine Tools Conf, Red Carpet Inn, Milwaukee, Wis. **Information:** Robert L. Douglas, Gilman Eng & Mfg Co, 305 W Delavan Dr, Janesville, WI 53545

Nov 11-14—12th Electrical/Electronics Insulation Conf, Sheraton Boston Hotel/Hynes Audit, Boston, Mass. **Information:** E/EIC, PO Box 159, 700 Peterson Rd, Libertyville, IL 60048

Nov 19-20—IEEE Computer Soc Sym on Computer Arithmetic, Dallas, Tex. **Information:** Prof D. E. Atkins, Dept of Elec and Comp Eng, U of Michigan, Ann Arbor, MI 48104. Tel: (313) 763-0038

Dec 1-3—IEEE Internat'l Electron Devices Meeting, Washington Hilton Hotel, Washington, DC. **Information:** Institute of Electrical and Electronics Engineers, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

Dec 1-3—IEEE Nat'l Telecommunications Conf, Fairmont Hotel, New Orleans, La. **Information:** Institute of Electrical and Electronics Engineers, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

Dec 9-12—21st Annual Conf on Magnetism and Magnetic Materials, Benjamin Franklin Hotel, Philadelphia, Pa. **Information:** Conf Chm, R. L. White, 124 McCullough Bldg, Stanford University, Stanford, CA 94305; or Local Comm Chm, B. Stein, Univac div of Sperry Rand, PO Box 500, Blue Bell, PA 19422

Jan 20-23—Computer Soc of India Annual Conv, Hyderabad. **Information:** DVR Vithal, Prog Chm, CSI 76, Computer Group, Tata Institute of Fundamental Research, Bombay 400 005, India

Sept 29-30—(Summit Hotel, New York City), **Oct 20-21**—(Marriott at International Airport, Washington, DC), **Oct 27-28**—(Hyatt Regency O'Hare, Chicago, Ill), **Jan 19-20**—(Dunfey's Royal Coach, San Francisco, Calif), Performance Evaluation and Improvement. **Information:** Stimler Assoc, Computer System Consultants, 33 W Second St, Moorestown, NJ 08057. Tel: (609) 235-5981

Oct 5-7—Prospects for Optical Memories and Recording; **Oct 26-28**—The Future for Printing Technology; **Nov 9-11**—Interactive Computer Graphics, Castle Hill, Ipswich, Mass. **Information:** The Institute for Graphic Communication, Richard D. Murray, Conf Dir, 375 Commonwealth Ave, Boston, MA 02115. Tel: (617) 267-9425

Sept 16—(Denver, Colo), **Sept 18**—(San Francisco, Calif), **Oct 6**—(Washington, DC), **Nov 11** (Dallas, Tex), **Nov 18**—(Boston, Mass), **Nov 24**—(Ottawa, Canada), 6800 vs 8080—A Side-By-Side Comparison; **Sept 26**—(San Diego, Calif), **Oct 8-10**—(Washington, DC), **Nov 12-14**—(Dallas, Tex), **Nov 19-21**—(Boston, Mass), **Nov 25-27**—(Ottawa, Canada), Military Microprocessor Systems. **Information:** Dr David Collins, Integrated Computer Systems, 4445 Overland Ave, Culver City, CA 90230. Tel: (213) 559-9265

Oct 27-Nov 7, Dec 8-19—LSI-11 Training Course, Maynard, Mass. **Information:** Phil Landry, Educational Services Dept, Digital Equipment Corp, 146 Main St, Maynard, MA 01754. Tel: (617) 897-5111; X4900

Dec 8-12—Numerical Methods of Optimization, Engineering Bldg, University of Manitoba, Winnipeg. **Information:** Prof E. O. Anderson, Continuing Education Div, U of Manitoba, Winnipeg, Manitoba, Canada R3T 2N2. Tel: (204) 474-8207

We make the OEM cartridge tape drive you can call your own.

Ms MOHAWK DATA SCIENCES CORPORATION MODEL 2022
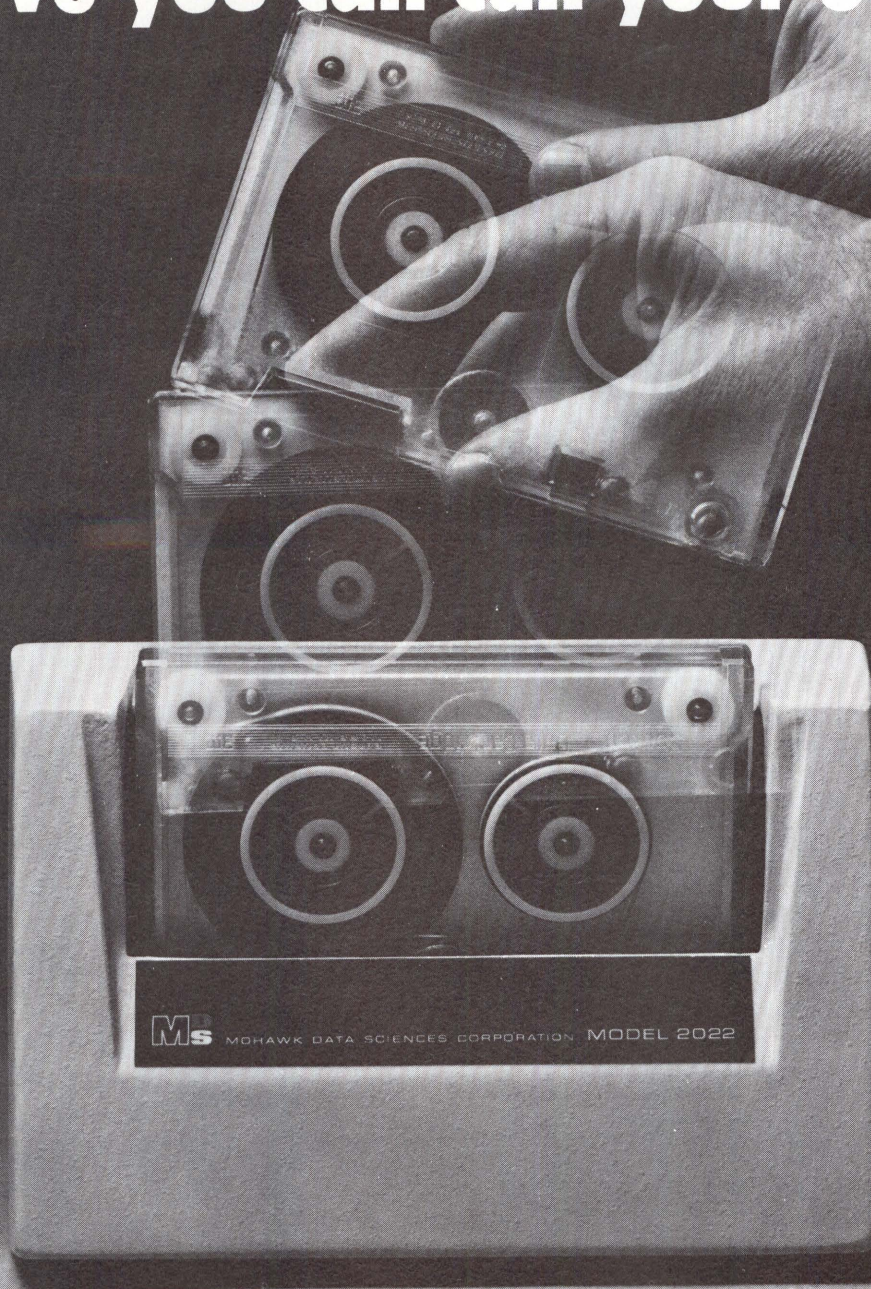
They're tough on competition and modestly priced. To the engineering excellence of the 3M data cartridge, we added a precision drive, based on high-speed reel-to-reel tape drive technology.

In the current models 2021 and 2022, you can quickly discover the long-needed replacement for paper tape, cassettes, or whatever you've tried for input programs.

You can also discover low-cost intermediate storage for minicomputers, as well as a reliable maintenance-free peripheral for remote data collection, communications terminals, and POS systems.

Performance features include: 30-ips read or write, 90-ips search and rewind, read-after-write check, 250 to 1600 bpi, phase or bi-phase encoding on 1, 2, or 4 tracks, and total capacity of 23 million bits.

Design simplicity in the MDS Cartridge Drive is based on a rugged casting, with a fixed position, dual-gap read-after-write head, interchangeable circuit cards, and a long-life drive motor.

Discover a new standard for low-speed tape drive price/performance. It all starts with your inquiry. Phone 215/337-1910, or write:
Mohawk Data Sciences Corp., OEM Marketing,
781 Third Avenue,
King of Prussia, Pa. 19406

MDs.

Mohawk Data Sciences
Quality OEM Products

CIRCLE 6 ON INQUIRY CARD
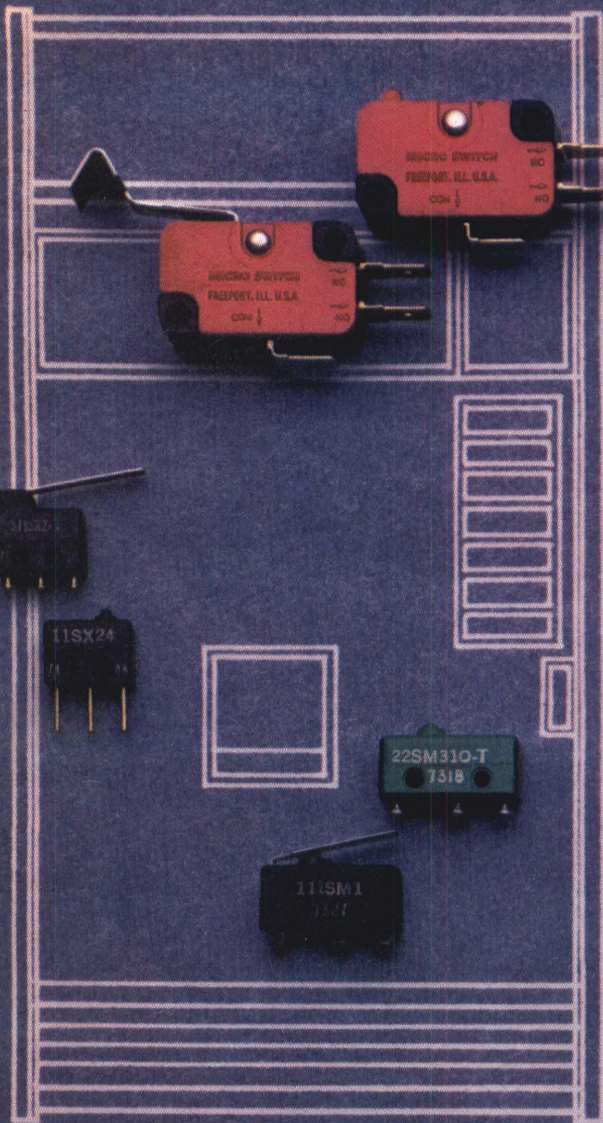
SNAP-ACTION V3, SM AND SX SWITCHES PROVIDE HIGH RELIABILITY AND ARE CAPABLE OF HANDLING HIGH OR LOW ENERGY CIRCUITS; PROVIDE OUTSTANDING PERFORMANCE FOR SELECTION, TIMING AND DISPENSING FUNCTIONS IN VENDING MACHINES.

IDEALLY SUITED FOR DIGITAL CASSETTE RECORDERS AND CARTRIDGE DRIVES, THE 26 EM MOTOR USES A HOLLOW ROTOR TO PROVIDE THE LOWEST POSSIBLE ROTOR MASS, RESULTING IN VERY LOW INERTIA. DIRECTLY INTERCHANGEABLE WITH MOTORS MADE OUTSIDE USA.

MINIATURE SERIES 8 SWITCHES PROVIDE THE ATTRACTIVE APPEARANCE, SMALL SIZE AND RELIABILITY NEEDED FOR HAND-HELD DIGITAL TIMERS. OFFER A WIDE VARIETY OF OPERA-TORS INCLUDING TOGGLES, PADDLES, PUSHBUTTONS LIGHTED AND UN-LIGHTED ROCKERS.
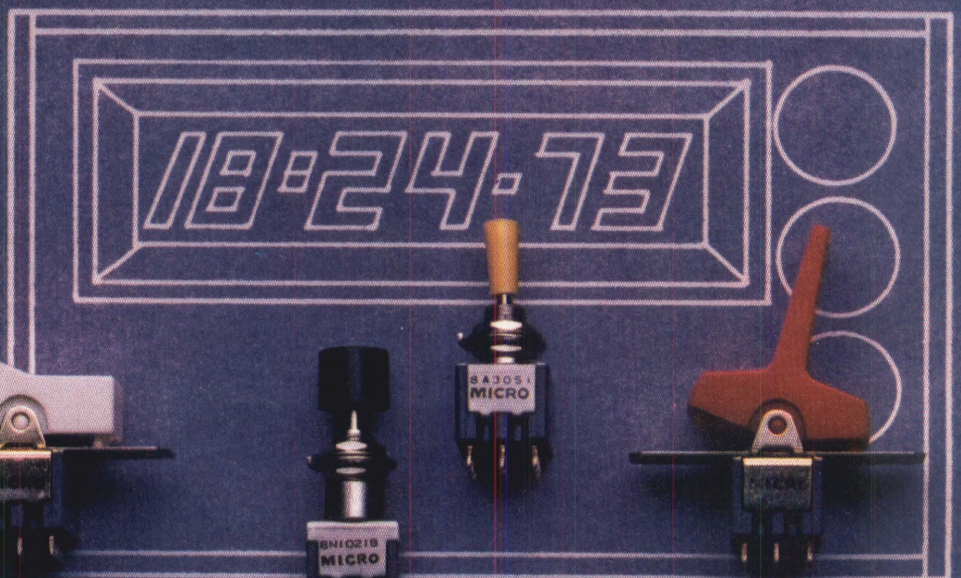
never wear out. The others will just come close.

The solid state keyboard, AML lighted pushbuttons and solid state position sensors you see here will probably never wear out. Because they're all solid state.

Each is based on a Hall effect integrated circuit. A circuit that's been tested through billions of operations without failing. Even once. And proven by performance in a variety of applications. The other components you see here come close. Simply because of the way they're designed and put together.

Like the long-life versions of our snap-action V3, SM and SX precision switches. Available in a wide variety of sizes, electrical capabilities and ratings, terminals, actuators, contact forms and operating characteristics—they've been tested to a mechanical life of over 10,000,000 operations.

Or the Series 8 miniature manual switches. Designed with epoxy-sealed terminals on most versions for extra reliability. And offered with virtually any operator you might need. Plus terminals that include solder, quick-connect, printed circuit or wire-wrap.

The same standards of quality and product flexibility go into the 26EM DC motor. It's a miniature motor designed with low inertia operational characteristics. And just one of a line that ranges up to the 500VM, a motor capable of accelerating to 4000 RPM and stopping over 1000 times per second.

If you'd like more information on any of these components, contact your nearest MICRO SWITCH Branch Office or Authorized Distributor.

And find out how you can get a component that goes on forever. Or at least comes very, very close.

MICRO SWITCH

FREEPORT, ILLINOIS 61032
A DIVISION OF HONEYWELL

MICRO SWITCH COMPONENTS ARE IDEALLY SUITED FOR APPLICATIONS LIKE THIS PRINTER AND OTHER COMPUTER PERIPHERAL EQUIPMENT. FOR INSTANCE, THE SD KEYBOARD OFFERING HIGH RELIABILITY, LOW PROFILE AND LOW COST; THE AML LIGHTED PUSHBUTTONS, FEATURING QUALITY APPEARANCE AT A LOW COST, ELECTRICAL FLEXIBILITY INCLUDING SOLID STATE VERSIONS; PLUS A COMPLETE LINE OF SOLID STATE POSITION SENSORS OFFERING ALMOST INFINITE LIFE AND COMPATIBILITY WITH COMPUTER LOGIC.

Reader Service Card 7 for data;
8 for salesman call

MICRO SWITCH products are available worldwide through Honeywell International.

by John E. Buckley
Telecommunications Management Corp
Cornwells Heights, Pa.

Remote Batch Vs Interactive Processing

The primary decision that must be made when defining an online information system application is the basic architecture of the system's data flow—In what mode and under what motivation will data and information be exchanged among the designated system locations? Regardless of the number of data flow variations, the system designer is confronted with two alternatives. The envisioned system can be structured to collect data using remote batch transmission for subsequent scheduled processing, and to use the same type of data flow for distribution of resulting processed data. Second choice is to create a demand operating mode by initiating processing and communicating the results on a demand basis. Both methods are widely used in today's information systems.

There are, however, significant differences between the two methods, each with important advantages and disadvantages. Which method is selected for a particular application is dictated directly by the impact that these relative advantages and disadvantages have on that application. When an application is first conceived, either architectural philosophy may be applied. Only when the concept takes definable form, such as a predetermined network configuration or an existing processing system and data base, do the relative advantages and disadvantages become evident. To properly design for such an application environment, a hypothetical system design must be detailed for each method; then, when ideal system definitions have been established, final evaluation can be addressed.

Beyond these initial design evaluations, the designer can structure an application toward one of these methods. Even if restricted by an existing data processing system and its associated operational constraints, a specific application can be designed to exhibit many characteristics of one of these methods.

Too often, online applications are implemented without prior thought or decision regarding basic method of data flow. It is sometimes argued that such an analysis is merely an academic exercise if the application must conform with and operate in an existing data processing environment; however, recognition of the fact that data processing systems are constantly changing and in a perpetual state of update makes it imperative to clearly define the advantages and disadvantages of these two methods for every application. Even when an application is currently constricted by an existing data processing system and network configuration or software design, it is important that the optimum method be approached to the greatest degree possible.

The term *remote batch processing* conjures up visions of huge data volumes being exchanged at high rates with a large centralized data processing system. All processing events in that system are carefully and rigidly scheduled. Data are gathered on tape or disc file for later scheduled processing, and processing results are also stored for later scheduled delivery to the designated remote batch terminal. The entire environment is characterized by large volumes and controlled schedules. Deviation from the defined sequence of events is unthinkable and only large volumes of data are ever acceptable or justified.

Interactive processing, on the other hand, connotes an entirely different information system concept. An environment comprising small segments of data that are quickly transmitted to a centralized data processing center for demand processing is characteristic of this mode of data flow. Typically, the results of that segmented processing are returned immediately to the originating remote terminal, where they may form the basis of the next input data segment. Such a system's operation is also called conversational interactive processing or conversational data processing. The network, data processing center, and associated operating software are completely time, rather than volume, oriented. Interactive processing efficiency is expressed in terms of system responsiveness rather than system capacity.

These data flows depict the extremes of the application spectrum. There are many data applications that can be processed only on the basis of a scheduled large-volume data transfer; conversely, system requirements such as programmed instruction must operate on a conversational, demand processing basis. The vast majority of information system application requirements, however, lie somewhere between these extremes. For these, system designers must formulate the proper decisions to achieve optimum data flow.

Should all data transfers operate in a remote batch format or should the demand aspects of interactive processing be emphasized? This often overlooked decision can be properly made only by objectively comparing the advantages and disadvantages of each method of data flow relative to the application's requirements. When such a comparison is not made, the final method of data flow is selected indirectly, usually the result of procuring a particular terminal or installing a specific communications software package. Whatever generalized data flow method was envisioned by the designer of that terminal or that software package is automatically implemented for the application, without regard for alternate methods and techniques.

Six of the best reasons for buying Data General computer systems.

If a computer system can't do a good job of file handling, chances are it won't do your job well either.

So we give you a lot of good ways to handle your files.

We offer six different disc subsystems. From 0.3 to 360 megabytes in size; with transfer rates from 30K to 800K bytes per second; and prices from $2,900 to $110,000. So you can pick out the ones that work the way you work.

And we fully support all our disc drives with our systems software. With RDOS and MRDOS for example, you can keep your high-use data on fast access discs, and data you need less on slower discs. With INFOS, you can logically partition a file across different physical media to get the most efficient use of your system peripherals.

All our operating systems treat all our peripherals like files. Which makes our files device independent. And a lot easier for you to use.

And because all our operating systems share the same file structure, you can maintain and operate your files with any of our languages: FORTRAN, BASIC, ALGOL, RPGII, MACRO assembler.

And you can use any combination of disc drives. So you can manage files from one to one billion bytes and match your file handling to your application.

Yet with all the flexibility we give you, we don't demand a lot in return. You can get an Eclipse S/200 system with 48K bytes of core and a 10 megabyte disc file for under $30,000. (quantity one, list price.)

Write for more information.

You may end up buying our computer systems because of the way we handle your files.

DataGeneral
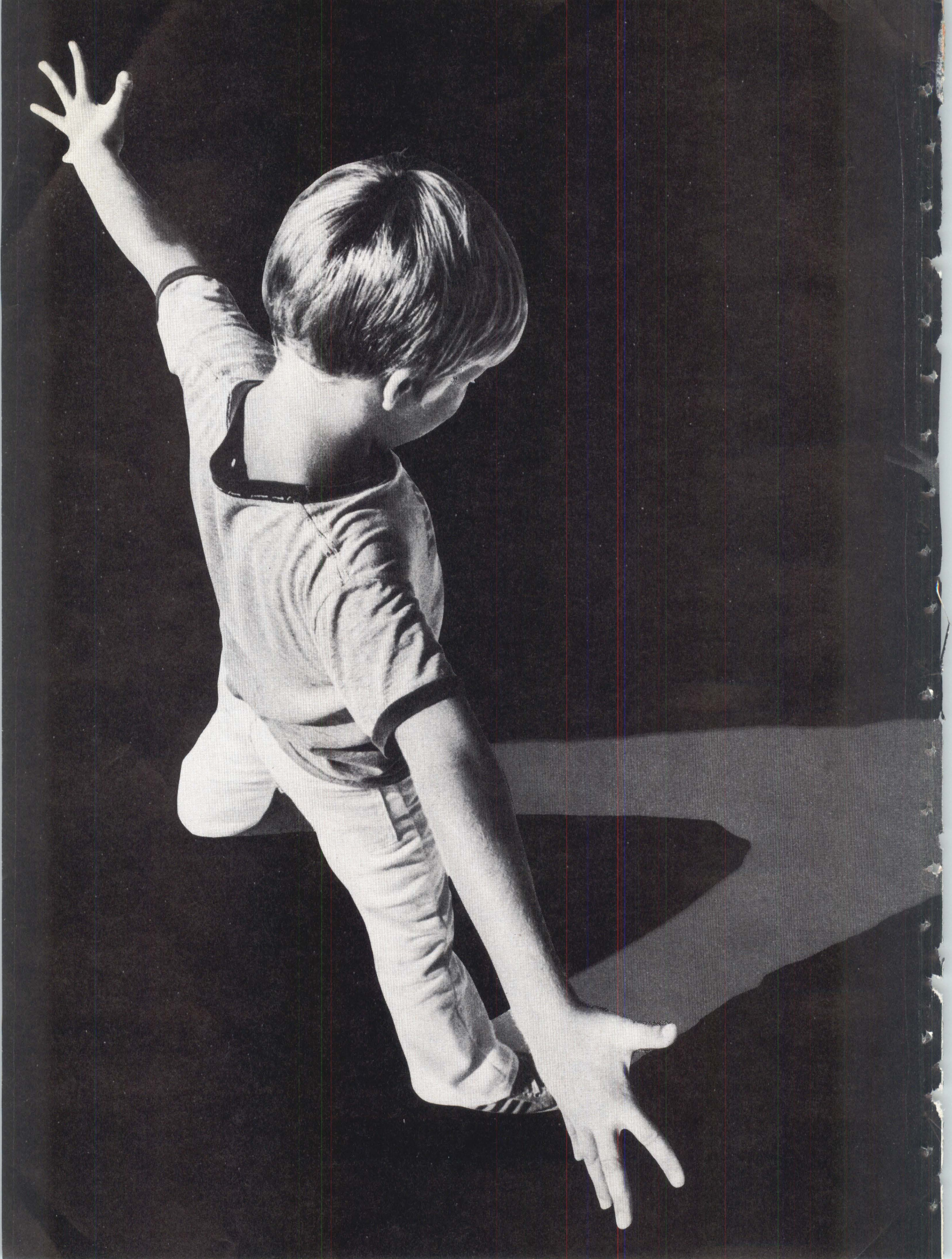
MEET OUR YOUNG GIANT.

MAX III. HE KEEPS GROWING STRONGER.

We delivered our first MAX III operating system in 1971. It was the birth of a new state of the art in minicomputer software.

Since then, while other companies have been laboring to produce their first real-time multiprogramming software, ours has just been getting better.

Today's MAX III, in combination with our MODCOMP II hardware, is just about unbeatable for demanding real-time operations.

Unbeatable in performance. Unbeatable in price.

Hundreds of MODCOMP II/MAX III systems have already proved themselves. Working in every conceivable kind of industrial and scientific measurement and control application.

Consider a few highlights.

In MAX III, 256 execution priority levels give you more flexibility than you're ever likely to need. For everything from highest priority foreground to deferrable background tasks.

Task execution can be changed by the operator, or by other tasks, interrupts and timers. Unlike most systems, new compilations are not needed to change task execution parameters.

When it comes to programming, you can use the language best suited to the job. FORTRAN. Macro assembler. Or a mixture of both. With individual task protection to give you fullest security for all your programs.

Heavy software is only one side of the coin, however. Because none of it does a thing for you without the MODCOMP II hardware to make it all happen.

With up to 64K words of directly addressable memory, MODCOMP II gives you a lot more clout than most minicomputers that only let you address 32K 16-bit words at a time.

Four simultaneous access paths to memory allow non-cycle stealing I/O. Or may be used for multiprocessor configurations. With all four ports in operation, memory bandwidth is five megawords a second.

Fifteen general purpose registers and overlapped memory enable MODCOMP II to consistently outperform machines that offer only a handful of registers, with a cache memory that is supposed to solve all your problems. But often doesn't.

MODCOMP II/MAX III is fully upward compatible with all other MODCOMP computers, including the 32-bit MODCOMP IV. So you can add on at any time as your needs grow. Even expand into a multiprocessor network system, without reprogramming.

But, like we said. These are merely highlights.

For detailed specs, and benchmark data that shows how MODCOMP II/MAX III stacks up against the best anyone else has to offer, write us.

After all, we're very proud of our young giant. He's already conquered a good part of the world. He's out to beat the rest.

Modular Computer Systems, 1650 West McNab Road, Ft. Lauderdale, FL 33309. Phone (305) 974-1380

European Headquarters: 103 Mytchett Road Mytchett, Surrey, England. Phone (0252) 514251

MODCOMP®

SOLVING PROBLEMS WITH COMPUTERS.

Major system characteristics for each data flow method are shown in the Table. Depending upon the specific application, each may be either an advantage or a disadvantage, and must be evaluated in light of the specific application. Although some characteristics tend to imply an absolute disadvantage, such as "Higher System Overhead," final determination can only be made by considering the intended operating system and the characteristics of the alternative to "Higher System Overhead."

A major operational distinction between the data flow methods is their relative impact on the associated system's processing resources. A remote batch processing environment is highly scheduleable. As such, it is totally practical to preallocate system resources among projected processing events, providing only minor flexibility for volume variations and occasional transmission contingencies. With interactive processing, however, system resources must always be fully prepared to handle a worst-case situation. While batch-oriented systems can realistically be designed for average loads, an interactive system must be prepared to process or at least logically defer peak load situations. In the latter situation, excess system capacity is characteristic, yet unexplained system malfunctions occasionally occur when even this excess system capacity is momentarily exceeded.

Advantages of batch processing systems are usually described in terms of data volumes processed, while interactive systems typically assert their value in terms of response or the timeliness of resulting data. Basing system decisions on only one factor can generate some surprising results—A batch system which can process many megabytes of data (but requires excessive time to provide results) or an interactive system that can provide instantaneous response (if only one terminal is active).

Batch-oriented systems usually permit and sometimes require that the system's intelligence or processing capability be shared to a significant degree among its terminals. This capability of distributing some data processing functions among terminals can also reduce central CPU overhead and processing require-

Comparative Data Transmission Characteristics	
Batch Processing	Interactive Processing
Scheduled	Demand
Volume-oriented	Time-oriented
Distributive intelligence	Centralized intelligence
Low system overhead	High system overhead
Data base independent	Data base dependent
CPU controls	Terminal controls
Complex terminals	Simple terminals
High terminal cost	Low terminal cost
Rigid protocol	Minimum protocol
Automatic error control	Manual error control
Isolated human operator	Participating human operator
Maximum diagnostics	Minimum diagnostics

ments. With the alternate interactive processing approach, terminal limitations typically require that all processing and data-content sensitive functions be centrally performed.

Primary causal factor for system utilization is that an interactive terminal, when online and active, creates processing utilization, making an interactive processing environment a demand environment. In many applications, the time such a terminal is active is the main system utilization factor, rather than the dispersed data volume that was exchanged. On the other hand, a batch terminal's utilization of the central processor is universally based on actual data volume exchanged.

Relative complexity of the types of remote terminals is also a significant concern. Batch applications usually require considerably more complex remote devices than interactive applications, since they must provide, as a minimum, the ability to store or buffer data while awaiting a control sequence from a central processor. Another, usually mandatory, requirement is the ability to recognize and logically recover from a wide range of system and network abnormalities. Beyond this degree of complexity, pre- or post-data processing functions may also be imposed. Interactive terminals need only provide a minimal means of keying data onto a communications line and of receiving and displaying digital information from that line.

At the present time, higher complexity tends to equate with higher unit cost. Continued application of microprocessor and semiconductor memory technologies, however, may

diminish this relationship. Terminal complexity will then equate to more critical terminal support requirements and, hence, higher terminal support costs rather than merely higher terminal device costs.

Remaining characteristics in the Table further delineate differences that exist between the data flow methods. Complex and rigid data-transfer protocols typify the batch environment while the virtually protocol-free teletypewriter format is the *de facto* standard among most interactive terminals. While lack of any significant protocol enhances the data flow simplicity, associated disadvantages require that most error control and error correction must involve a human operator. In addition, system malfunctions, delays, or abnormalities are totally visible to interactive terminal operators; depending on the operator, this can be either an application advantage or disadvantage. Ability of the terminal device to participate in system diagnostic procedures is also directly proportional to the degree of terminal complexity.

The proper data flow method will be defined when the optimum combination of these characteristics for each application is achieved. Considerable experience in designing and, perhaps more important, correcting online systems shows optimum data flow to be a hybrid of methods. The remote terminal operator must have the impression and the advantages of operating in an interactive mode, while the data communications network and centralized processing facility should have the control and recoverability of a batch transmission environment. □

UNIVERSAL MODEMS

Universal makes modems any way you want them — as OEM cards, rack-mountable units or free-standing packages. In a word, we combine the latest in modem technology with the ultimate in personalized service and personalized applications engineering.

For example, using CMOS technology, we've put a whole 201 modem on a single card in less than 50 square inches. Of course we also offer many choices of 103s and 202s.

Our custom design capability offers you the performance options you need, as well as complete compatibility with your mechanical layout. Besides cards, rack-mounted or free-standing units, Universal also provides multi-channel packages, with modems in any frequency mix up to 2400 bps.

In addition to our products, we're extremely proud of our customer service. Check us out: Call us on the telephone. You'll like what you hear.

universal data systems

member of IDCMA

2611 Leeman Ferry Road • Huntsville, Alabama 35805 • Telephone (205) 533-4500 • TWX 810 – 726-2100

The ultimate solution to the micro/mini confusion

Just what you needed, right? Another computer to confuse things a bit more. And a millicomputer at that... whatever that is.

Well take heart, pilgrim. Because thanks to the whatever-it-is NAKED MILLI millicomputer, your hardware hardships are over.

Solution No. 1

Start with your price problem: $395 used to buy you a lot of grief in the form of an 8- or 12-bit microprocessor. Which was still a bunch of bucks away from anything you could call a computer.

Now, $395 buys you the NAKED MILLI LSI-3/05 with 256 16-bit words of RAM. A full-blown, full-scale computer with an amazingly powerful instruction set and two standard I/O systems including ComputerAutomation's new Distributed I/O System.™

Solution No. 2

It also buys you membership in the NAKED MINI® LSI Family. Not just a casual relationship, but total hardware and software compatibility.

"Ah ha," you say, as you reach for a purchase order. "That means Maxi-Bus™ compatibility, too. Which means the NAKED MILLI is also compatible with Computer-Automation's standard peripheral controllers and I/O interfaces. Which means..."

Yeah. You're going to save a fortune on interfaces. And software. And everything else. Because the NAKED MILLI really is a genuine, 100% full-fledged member of the LSI Family.

Solution No. 3

Suppose, however, that you need more machine. Okay, how about a computer with 1K words of RAM for $489? Or...

4K for $616?
8K for $914?
16K for $1679?

And that's how it is. No matter where you buy in, the NAKED MILLI is positively the lowest-priced, low-end computer around.

From the people who brought you the NAKED MINI

When ComputerAutomation offered the first NAKED MINI LSI for $990, folks figured that was it...the all-time rock bottom price.

And now we're introducing the NAKED MILLI at $395. True, it's the smallest computer in the LSI Family. But here's something to think about: The NAKED MILLI is more powerful than our original Model 816 minicomputer!

In short, Computer-Automation has done it again.

But then, that's what leadership is all about.

CA ComputerAutomation
NAKED MINI® Division
18651 Von Karman, Irvine, Calif. 92664 (714) 833-8830

All prices shown are for quantities of 100.
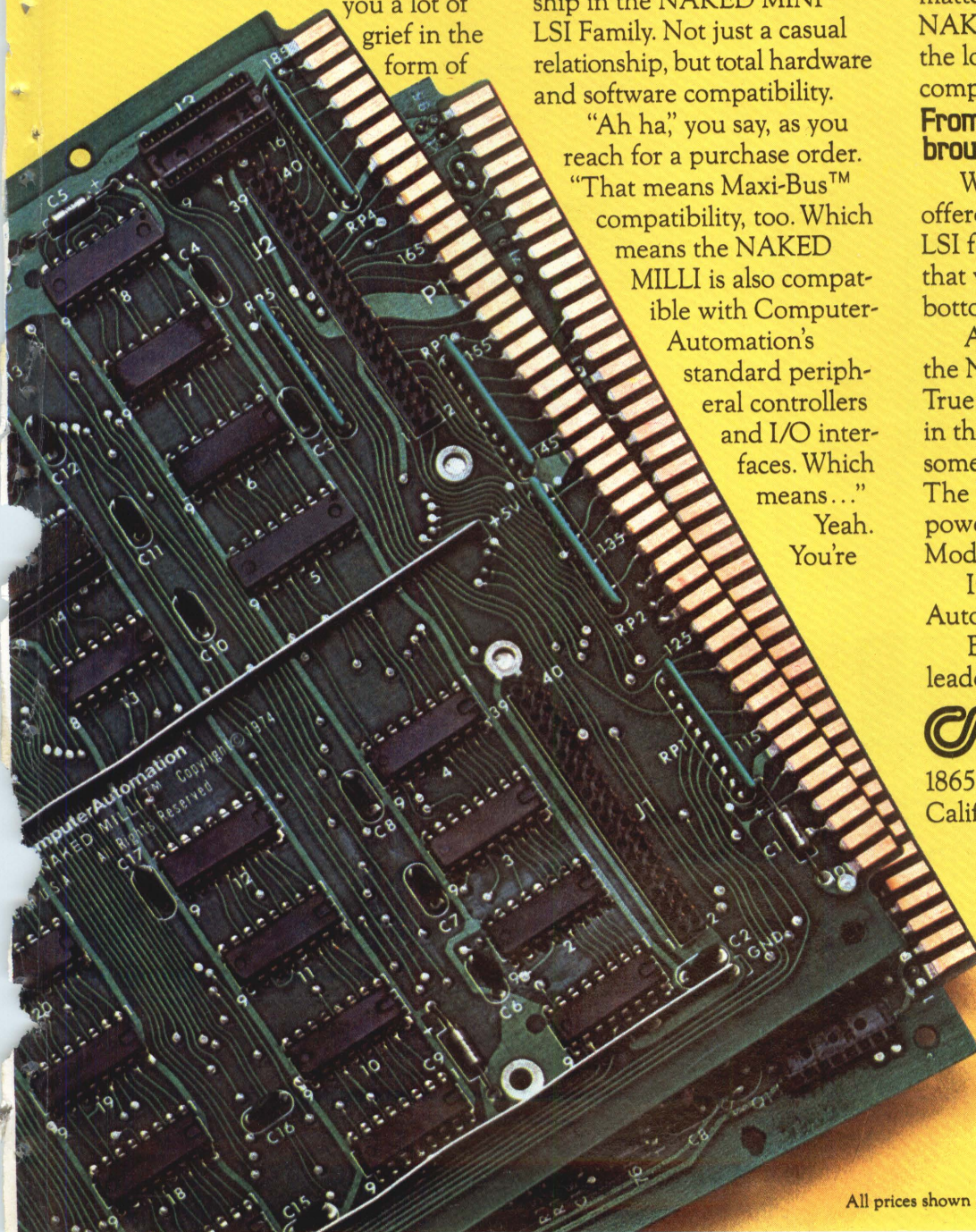
Terminals Automatically Insert Repetitive Data To Speed Transmission

Large volumes of data can be fed into a computer at high speeds by a dual key-entry station that automatically inserts data, such as date and results of arithmetic calculations, as the operator records information. In addition, single keystrokes will initiate frequently required tasks (for example, transferring a record into disc storage). The terminal automatically checks data for accuracy and alerts operators to errors before transferring the data to the computer. A 236-character display located directly above the source material also permits the operator to check accuracy while entering data.

An addition to the 3790 communication system, the 3760 dual key-entry station was announced by International Business Machines Corp, Data Processing Div, 1133 Westchester Ave, White Plains, NY 10604 along with enhancements to the 3767 communication terminal and 3770 data communication system. Other related announcements involve two computer programs that increase data communications flexibility among terminals and applications used with interconnected computers.

Two models of the 3760 can be used in a system. Model 1 contains logic and storage to perform control and display functions, data editing, and checking; model 2 is a functionally identical expansion unit. One model 1 and either one or two model 2s can be linked to form a data entry pool of four or six operator positions, with a keyboard and gas panel display at each position. Up to 12 entry stations can be linked to a 3791 controller which controls the stations simultaneously, provides disc storage for data to be transmitted or received, and handles communications with a System/370 host computer. Although designed primar-
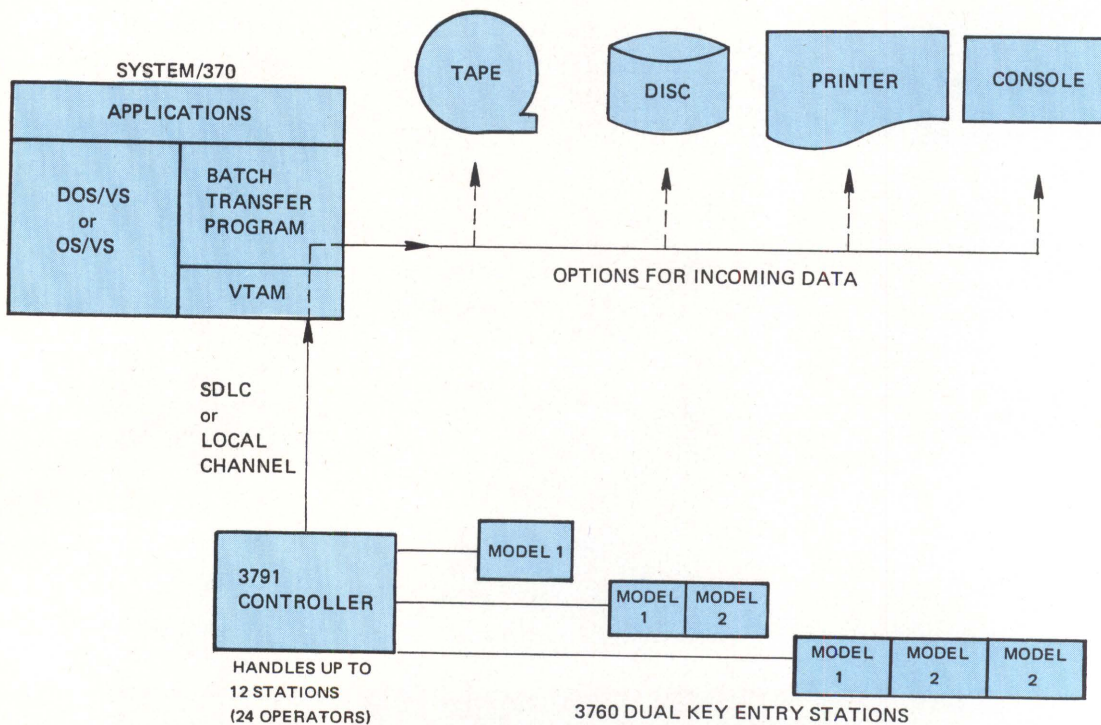
Data from many as 12 IBM 3760 dual key-entry stations can be transmitted over cable (up to 2000 ft) to a 3791 controller for storage on disc and later batch transmission, also over cable, to a byte-multiplexer channel in a vertical storage System/370 computer. Support is provided by Disc Operating System/Virtual Storage (DOS/VS), Operating System/Virtual Storage 1 (OS/VS1) or Operating System/Virtual Storage 2 (OS/VS2). For extended separation, the 3791 can communicate with the computer over a Synchronous Data Link Control (SDLC) line. Interface and control of data flow between computer and key entry system are provided by the batch transfer program, under support of the Virtual Telecommunications Access Method (VTAM)

Hewlett-Packard Introduces: DISCU/15 for OEMs. Fast. Tough. And Smart.

A new concept in disc drives especially for OEMs.

DISCU/15 combines 15 megabytes of usable disc capacity with a micro-processor based Storage Control Unit (SCU). This makes possible a moving head disc that is super-fast and rugged enough to replace fixed-head discs and drums.

And it's smart. The SCU takes the load off your processor to make the entire system faster. Plus it's designed for easy interfacing, something OEMs have been waiting for.
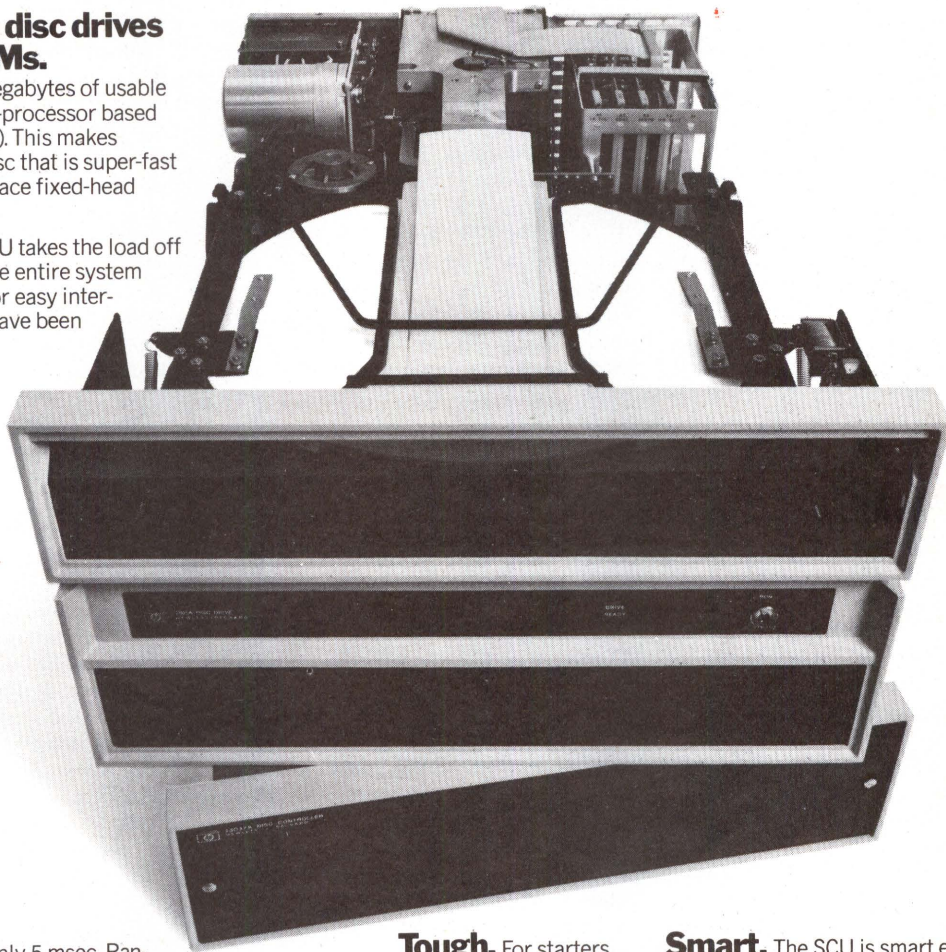
Fast. Track to track in only 5 msec. Random average is 25 msec. The only 3600 RPM cartridge drive. Transfer rate is 937 kilobytes. More capacity in a cartridge: 10 megabytes of removeable storage and 5 megabytes on the fixed disc. Up to 8 drives per Storage Control Unit give you ample capacity when you need it.
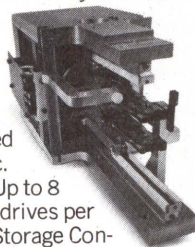
Tough. For starters, a rigid, precision-milled 40 lb. casting really stands up. An integrated spindle and DC Motor eliminates belts and pulleys. And it's designed for use on the open manufacturing floor. A separate blower keeps contaminants out even during cartridge change. The only cartridge disc using track following technology for outstanding reliability. The result: DISCU/15 guarantees interchangeability within the most severe environmental specs available in commercial discs. Easy service too. Even major sub-assemblies are modular for easy replacement. The only equipment you need for major servicing (including head alignment) is a compact Disc Service Unit.

Smart. The SCU is smart enough to be called a minicomputer. Here's what it gives you: multi-CPU capability. Error correction for up to 32 bits per sector. Track switching transparent to processor. Rotational Position Sensing. Command Retry. Plus, a high level interface for quick integration. That means you save time, money and headaches. For all the details, call your nearby HP field sales office.
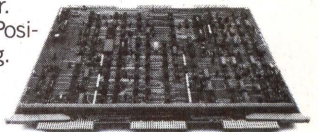
HP Discs. They work for a living.

HEWLETT [hp] PACKARD

Sales and service from 172 offices in 65 countries.
1501 Page Mill Road, Palo Alto, California 94304

22539

CIRCLE 13 ON INQUIRY CARD

19

ily for installations requiring a relatively large number of key-entry stations in one location, the 3760 can also be used in decentralized applications, with one or a few units located in various user departments.

Characters on the gas panel display are formed through a pattern of lighted dots in a 7 x 9 matrix. A panel contains six lines—five for display of data to be checked by the operator before entry, and a tap line for operator messages. When the system detects an error, it flashes a message on the display panel to alert the operator. A keying error can be corrected by backspacing and rekeying; if the error is in the source document and cannot be corrected immediately, the operator presses a key to mark the record for future attention.

After each record is completed, data are transferred to the 3791's disc and stored for later batch transmission to the computer. Error records discovered by a host application program can be returned to the 3791 for checking and correction by an operator.

Each supervisor and operator can be assigned an identification number —or password, if necessary—which is keyed into a station and checked for validity. An operator's number and password can be changed only by a supervisor. Passwords permit supervisor access to the system for determining equipment status, designating jobs that can be extracted by the computer, and routing messages to the computer operator. The supervisor can also request production statistics from the 3791 either for display on a panel or hard copy printout.

First customer shipments of the 3760 are scheduled to begin in the fourth quarter of this year. Purchase prices are $9240 and $5040, respectively, for models 1 and 2. Under the extended term plan, monthly rental charges are $220 and $120; under the standard rental agreement, monthly charges are $258 and $141.

Announced enhancements to existing systems consist of higher speed bidirectional printing for the 3767 communication terminal and some units of the 3770 data communication system as well as user-written programs to control functions of three 3770 series terminals. Speeds of matrix printers on the 3767, 3771, 3773, and 3774 terminals have been increased from 80 to 120 char/s;

speed of the belt printer in the 3776 terminal has been increased from 300 to 400 lines/min. First customer shipments of all terminals with enhanced printing speeds are scheduled for the first quarter of 1976.

User-written programs which enhance programmable terminals 3773, 3774, and 3775 can check entered data for accuracy, control printing on forms, and perform arithmetic operations. They will also permit users in remote locations to handle a variety of tasks, independent of the computer. Storage available for processing programs is 4 to 12 kilobytes on the 3773 and 6 to 22 kilobytes on the 3774 and 3775. In addition, the 3774 and 3775 include 100-kilobyte, non-removable diskettes for data and program storage, and may be equipped with 480-char display units for data checks by operators. These terminals are scheduled for first customer shipments in the second quarter of 1976.
Circle 150 on Inquiry Card

Bipolar Semiconductor Memory Increases Small Memory Capabilities

Ability to perform more simultaneous multiprogramming functions completely within small memory than was possible previously—and more efficient use of the central processor —results from use of bipolar semiconductor small memory in three models of the Cyber 76 computer system. Whereas previous core small-memory capacities for computers in this series were 32K or 64K words, the semiconductor memories contain double those amounts—at two to four times the reliability of core, according to the manufacturer.

Announced by Control Data Corp, Box O, Minneapolis, MN 55440, for scheduled third quarter 1975 deliveries, model 121 contains 64K words of semiconductor small memory and 256K words of core large memory; model 122 has 64K and 512K; and model 142 has 128K and 512K. Both the 121 and 122 can be field-upgraded to a 142. The company also introduced the 7639/819 high capacity disc drive and controller subsystem which it claims will offer 15 to 25% improvement in performance at a price nearly 30% less than the mass

storage disc file first used with the Cyber 76.

The semiconductor small memory features 110- and 165-ns internal read and write cycle times. It provides memory residency for the Scope 2 operating system and for dynamic allocation of user jobs in process. A "phased memory" technique allows independent reference of consecutive memory addresses and therefore reduces potential memory conflicts by allocating references among 16 or 32 independent, phased memory modules. Single-bit error correction, double-bit error detection logic provides greater data integrity. Core large memory acts as a bulk memory interface between the semiconductor small memory and slower mass storage devices.

Average access time to the 819 disc storage subsystem is 50 ms; data transfer rate to and from semiconductor small memory is 6.2 million char/s. The disc uses voice-coil head positioning to read and record data stored at 6 kilobits/in.

Each disc storage subsystem holds 413 million characters of data on a fixed 22-disc pack. Up to four subsystems can be connected to each 7639 controller. Scope operating software currently supports up to three single-controller, 2-drive subsystems, providing a maximum storage capacity of 2.4 billion 6-bit characters; planned future software will connect up to four drives per controller in multiple-controller subsystems.
Circle 151 on Inquiry Card

IR LED Scanners Ease Ambient Light Interference Problems

Infrared light-emitting diode scanners and associated units, introduced by Warner Electric Brake & Clutch Co, 449 Gardner St, Beloit, WI 53511, are intended for industrial sensing applications where ambient light might cause false triggering. Included are retro-reflective, reflective, and 2-part photoelectric scanners, as well as amplifier-power supplies.

The Visolux MCS-620 retro-reflective unit is claimed to be virtually immune to ambient light. It has a maximum operating range of 10 ft, using a 3 in. retro-reflector, and a predicted life span of over 100,000 hr. For unusual applications, the
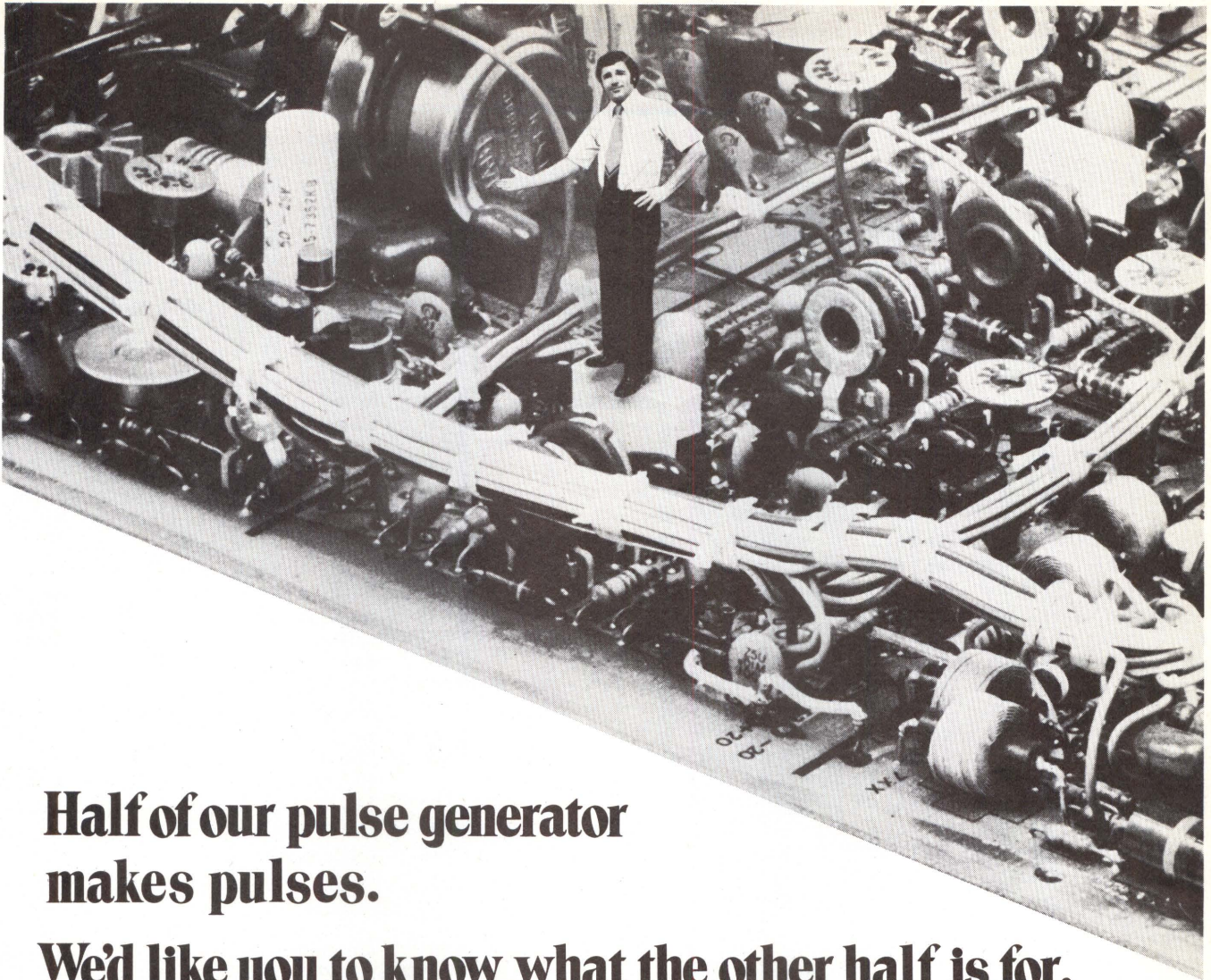
Half of our pulse generator makes pulses.

We'd like you to know what the other half is for.

Pulse generators make pulses — everybody knows that. The half everybody **doesn't** know about is that today's general-purpose pulse generators (like Interstate's SERIES 20) can:

1) **Make your life easier.** With Interstate's constant duty cycle mode, for example, you don't have to reset width and pulse period every time you change the frequency when testing a differential amplifier or an analog computing circuit over a wide range of frequencies. The width-to-period ratio remains constant as you change the frequency. Much easier.

2) **Give you an infinitely more versatile pulse.** Clock and sync outputs on Interstate's SERIES 20 Pulse Generators are squarewaves, instead of those other skinny, 10-nanosecond trigger pulses. So when you're testing low-speed stuff, like electromechanical machines or reed relays, or even some of the new microprocessors, you won't have to keep switching the scope over to high speed to make sure the trigger is there. Interstate's sync pulse is readily visible — and immediately usable.

3) **Allow you to use the pulse generator for other jobs.** SERIES 20's pulse amplifier mode can restore levels and transition times in MECL testing, for instance, so you can avoid having to jerry-rig some complex kluge of equipment.

Put the other half of your pulse generator to work. Interstate has just produced "Today's General-Purpose Pulse Generator Report" in which our SERIES 20 Pulse Generators, together with the major pulse generator models in the 50 MHz, 3.5 ns rise/fall time, 10 V output (into 50 ohms) category, are detailed and cross-compared, and application notes reveal methods and techniques for practical pulse problem-solving. For your free copy, write to:
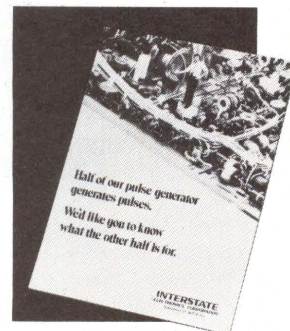
INTERSTATE
ELECTRONICS CORPORATION
Subsidiary of A-T-O Inc.

P.O. Box 3117, Anaheim, California 92803 • (714) 549-8282 • TWX U.S.A. 910-591-1197 TELEX 655443 & 655419
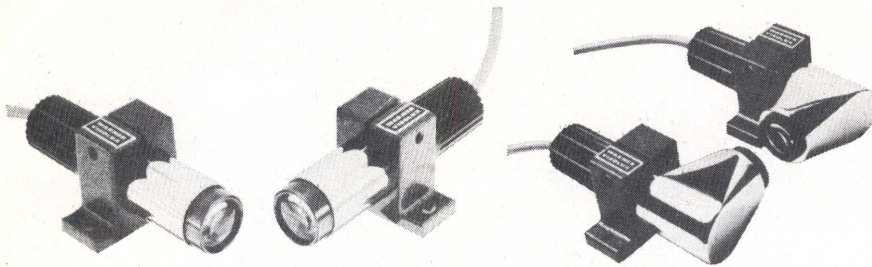
Warner Visolux MCS-622 and -623 LED photoelectric scanners are 2-part light source and sensor sets for straight-line and right-angle mounting, respectively, at 15-ft maximum operating range. False triggering by ambient light is virtually eliminated by synchronization of sensor and light source

scanner may be up to 32 ft from an associated amplifier. Scanner size of 2 x 1¼ x ¾" permits installation where available space is limited. An LED indicator on the rear of the unit eases alignment (lights when scanner's light beam is incomplete). Externally identical to this unit, but designed for applications where the pulsed IR beam reflects from the material being sensed, the -621 has a maximum range of 12 in. (for white paper).

Straight-line (-622) and right-angle (-623) mounting scanners with 15-ft maximum operating range have separate sensors and light sources. Synchronization of the receiver and light source minimizes problems from ambient light.

Amplifier-power supplies (-146 and -147) provide a range of time delays for any of the above scanners. A light/dark switch permits choice of activation by beam complete or interrupt, and a sensitivity adjustment provides for applications requiring decreased amplifier gain. The -147 also permits use of an optional triac or logic output device instead of the standard relay.

Circle 152 on Inquiry Card

Computer Systems Introduced for Data Communications Networks

Compatibility with its existing terminal computer products has been maintained in a series of "intelligent terminal computer systems" announced by Burroughs Corp, Detroit, MI 48232. Programs written in COBOL for the company's present TC series can also be used on the TC 5100 series. Although intended for use in online interactive data communications networks, they can be applied as well for batch data collection and local site processing.

Basic configuration of the four models includes operator's console with matrix printer, 4 kilobytes of memory, and either a "mini-disc" or a magnetic tape cassette for loading interpreter, application programs, and data. The TC 5110, with one cassette station, can also include a second cassette station and a Self-Scan® panel display, which matches the configuration of the 5113. The 5114 contains one mini-disc, but can be expanded to include a second and a panel display, comparable to the 5115. Both 5114 and 5115 can accommodate two data communications lines.

The microprogrammed central processor (CPU) uses an organized group of microinstructions, called the interpreter, which is brought into alterable memory to monitor and direct system functions and to execute user programs. Functions not required by current user programs do not need to be kept in memory. LSI MOS circuits are used in CPU, I/O processors, and modular memories.

CPU operation is at 1 MHz. Throughput is increased by an overlap feature which allows the CPU, during execution of one microinstruction, to look ahead at the next microinstruction to be executed.

Specialized I/O processors and a hardware interrupt system increase efficiency. In interrupt, each I/O channel notifies the CPU when data are ready for processing or transmission, eliminating need for the CPU to scan channels continuously.

User memory is expandable to 16 kilobytes in 4-kilobyte modules. Maximum system memory of 32 kilobytes includes user memory, interpreters, and 4 kilobytes of ROM, which is used to start the system and to store system confidence-test routines. These routines are stored programs which can be activated by the operator to perform tests on the system, including peripherals.

The operator's console features an impact printer which prints a 64-char set in a 7 x 7 dot matrix at 60 char/s, and can be positioned right or left at 160 char-spaces/s. Print format is 150 char/line at 10 char/in. Single or multiple part forms from 3 to 16.75" wide with up to six copies can be printed. Two rows of indicator lights on the console display status of system and peripherals. An electronic keyboard, equipped with special function keys for forms handling and printer control and 16 program keys for handling program options, conforms to ANSI-ECMA standards.

Capacity of 256 char on the panel display enables the system operator to check data entered on the keyboard for transmission to another system and data being processed in his system, as well as to display results from an inquiry by or to another system. The operator can print or not print the data displayed, as desired.

Systems communicate in either asynchronous or synchronous modes at speeds of from 75 to 9600 bits/s over leased, switched, or direct-connect lines. Dedicated transmit and receive buffers have variable capacities to meet user requirements.

Two data communications procedures may be in the system at the same time. The program or a key depression by the operator selects the procedure that will be active through the data communications channel.

Circle 153 on Inquiry Card

Time-Sharing Systems Adaptable to Small or Large Businesses

Datasystem 350 series commercial time-sharing systems are adaptable to use by both small- to medium-sized companies as standalone computer systems and by large companies as dedicated systems or in decentralized facilities. In addition, the top line model can function as the central computer in a distributed processing network. Each of the

DX980...the operable system
from Texas Instruments

The most powerful operating system for a minicomputer is also one of the easiest to use. Why? Check these features... "cookbook" job control language, sophisticated file management for three file types, 400-megabyte disc capacity...and more!

DX980 general-purpose operating system supports TI's Model 980 series minicomputers in various applications including batch processing, interactive terminal processing and real-time applications...simultaneously or each one individually.

System Description

DX980 features a modular organization. General executive functions are included in the nucleus, while specialized functions are embodied in the subsystems.

With this arrangement DX980 can efficiently manage multijob, multitask, memory, and I/O functions...all concurrently. In addition, the system contains a sophisticated file management feature for handling linked sequential, relative record, and key indexed files.

Another important feature of DX980 is system resource management, which includes dynamic memory allocation.

These features combined make DX980 ideal for multiprogramming applications using Fortran IV or assembly language for any number of large arithmetic operations.

Supporting Software

For such applications, supporting software includes a Fortran IV compiler; SAPG, a two-pass assembler; and DXOLE, an overlay link editor, in addition to a number of utility modules.
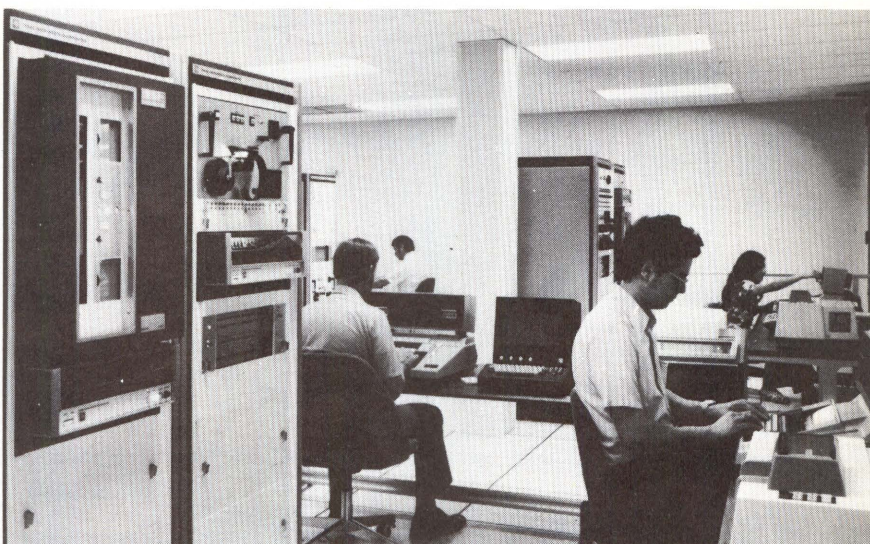
Hardware

The hardware configuration needed for these requirements is designed around a TI Model 980 series minicomputer with supporting peripherals. A general-purpose system capable of interactive terminal processing and batch processing could include four TI Model 912 Video Display Terminals, a moving-head disc with 2.28 million bytes of storage, a TI Model 979 magnetic tape drive, a 980B computer with 48K 16-bit words of error-correcting MOS memory, a "Silent 700*" Model 733 ASR Data Terminal, a 132-column medium duty line printer, a 300-cpm card reader... and, of course, DX980 operating system. This configuration enables users to have a $65,500 minicomputer system that can support tasks normally assigned to computer systems costing $100,000 or more.

This just may be the best bargain you have come across for your application. To find out more, contact the sales office nearest you. Or write Texas Instruments Incorporated, P.O. Box 1444, M/S 784, Houston, Texas 77001. Or call (512) 258-5121, Computer Systems Marketing.

Improving man's effectiveness through electronics

TEXAS INSTRUMENTS
INCORPORATED

*Trademark of Texas Instruments

Data comm spoken here

It's the M6800's native language

Data Comm is native to the MC6800 Microprocessor because the M6800 Family was designed for Data Communications from conception; born to it, you might say. The results speak for themselves.

Our diagram of a hypothetical data communications application suggests a cost-effective way to use specially designed data communications devices to add asynchronous AND synchronous data comm links to microcomputer systems.
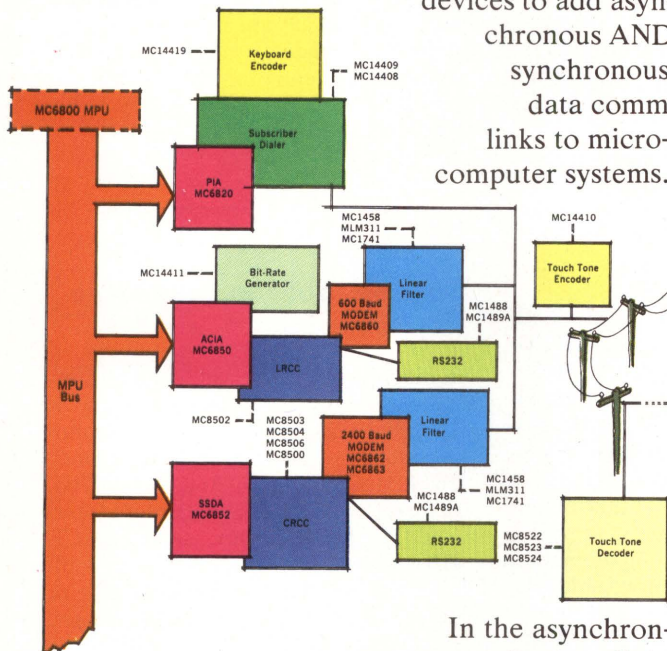
In the asynchronous communications link, the MC6850 ACIA converts parallel data to asynchronous serial format, and vice versa. The MEGALOGIC* LRCC/Data Register, the MC6860 MODEM and a McMOS Bit-Rate Generator fill it out, with EIA standard RS232 Linear circuits handling interface between separated system elements.

In the synchronous system, parallel-to-serial data conversion, and the reverse, is executed by the soon to be announced MC6852 SSDA, with MEGALOGIC CRCC units and the impending two-chip MODEM (MC6862/MC6863) assisting.

The combined capabilities of the MC6820 PIA and several McMOS subsystems are used to establish both dial-pulse and touch-tone telephone links between local and remote sites.

M6800 support: speeds the design job, makes it easier ...at lower cost

The EXORciser *(M68SDT)*. Here's the first systems development tool that lets you completely emulate your system application with significant reductions in hardware design and development costs.

Evaluation Module (MEC6800). It's a complete board, with all of the M6800 LSI circuits. Evaluate the parts in a basic minimum system.

Documentation: we wrote the book

M6800 Manuals. The utilitarian M6800 Programming Manual is complemented in our growing document library by the M6800 Applications Manual, where we truly wrote the book.

Choice of software packages

Commercial timesharing. M6800 software is presently available on three commercial timesharing services — G. E., United Computing Service, and Motorola Timesharing.
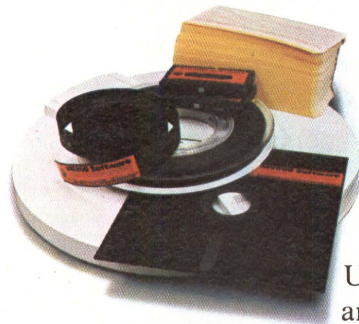
EXORciser and host packages. A resident software package is available for the EXORciser, as are host computer cross assembler and simulators.

A complete program for microcomputer system design

Complete! Yet, there's more...if you need it.

Like memory and I/O modules for the EXORciser. Like floppy disks, disk controllers and tape readers. Like a complete staff of systems applications engineers...in the field and at the factory. And they, indeed, speak Data Comm!

If you'd like to converse with them or peruse our literature on the subject — signal us at: P.O. Box 20912, Phoenix, AZ 85036.

*Trademark of Motorola, Inc.

MOTOROLA M6800
Benchmark family for microcomputer systems.

DEC Datasystem 352, lowest configuration of the disc-based 350 series business time-sharing systems, consists of PDP-11/10 central processor unit with 32 thousand characters of core, two floppy discs with 500 thousand characters, CRT terminal with keyboard, and 30-char/s printer

three disc-based models can support up to four hard-copy or CRT terminals, each on the same data base.

Introduced by Digital Equipment Corp, Maynard, MA 01754, each of the Datasystem 352, 354, and 356 computers uses a PDP-11/10 central processor unit with 32 thousand characters of core, expandable to 56 thousand. Mass storage includes at least two floppy disc drives that provide 512 thousand characters of on-line storage for the 352 (expandable to 1 million); two cartridge disc drives providing 4.8 million characters for the 354 (expandable to 19.2 million); and two disc pack drives providing 40 million characters for the 356 (expandable to 160 million). 352 and 354 can be upgraded in the field to the next higher system.

The series operates under COS (Commercial Operating System) 350, which provides time-sharing with a high speed response. This system features detached jobs, intertask communications, and line printer spooling. Additional features include more than 200 text error messages, a sort utility, a selective data file, and total disc backup utilities. Running under COS 350 is DIBOL (Digital Business Oriented Language)-11, an advanced

version of the industry's first high-level commercial data processing language specifically designed for minicomputers.

An optional 2780 communications protocol package is available. Operating under COS 350, this option emulates the IBM 2780 for telephone transmission of data in a distributed network.

A typical configuration of the 352, consisting of central processor, two floppy discs, video terminal, and 30-char/s printer, will sell for approximately $20,000; the 354, with two cartridge disc drives, central processor, two terminals, and a 165-char/s printer, will be in the $37,000 range; and a 356, with two large disc packs, central processor, any combination of four CRT or hard-copy terminals, and 300-line/min. printer, will be between $65,000 and $70,000. Additional hardware options include a choice of several video or hard-copy terminals in any desired combination up to four per system and any one of four printers ranging in speed from 30 char/s up to 300 lines/min. Also available are a choice of 800- or 1600-bit/in. magnetic tape drives and an 80-col card reader.

Circle 154 on Inquiry Card

partment, and ability to run automatic coin dispensers. It also interfaces with an electric produce scale. (Weight is accurately calculated to hundredths of a pound and shown on the register display. Price is computed, displayed, and printed on the customer receipt tape along with actual weight and price per pound.)

A battery backup system insures continuous operation in case of store or area power source failure. An optional polling subsystem interfaces to two or more registers to form a low cost system as an interim measure before upgrading to a computer-assisted key entry or scan entry system later.
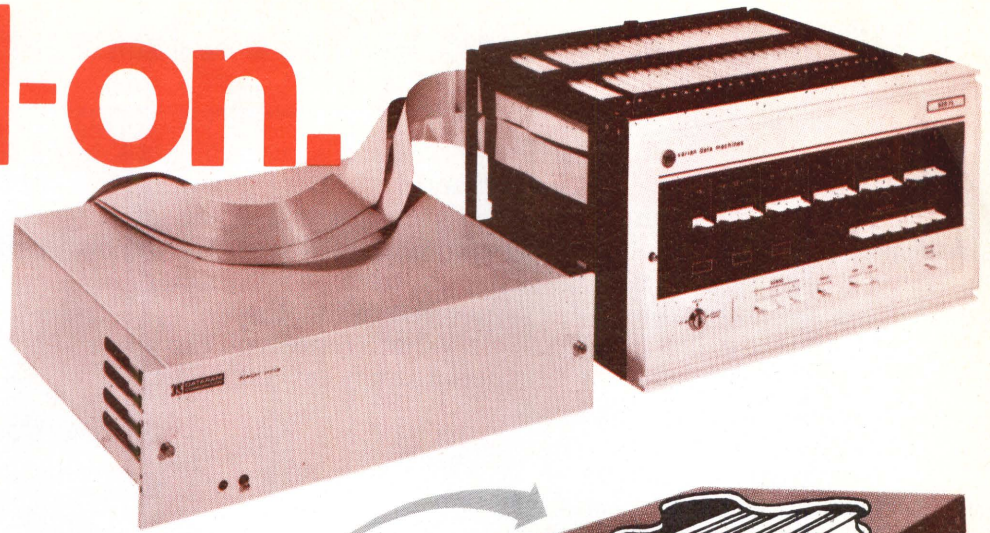
Circle 155 on Inquiry Card

Second Source Available For ECL ICs

A complete range of high-performance, emitter-coupled logic, process III silicon integrated circuits, manufactured by Plessey Semiconductors, 1674 McGaw, Santa Ana, CA 92705, is directly compatible with the Motorola MECL III 1600L series. PECL III circuits (SP 1600 series) are available off-the-shelf in either 14- or 16-pin dual inline ceramic packages. Features include gate switching speeds of 1 ns, capability of driving terminated lines with impedance as low as 50 Ω, a flip-flop toggle and shifting rate greater than 500 MHz, and operation with unused inputs left open.
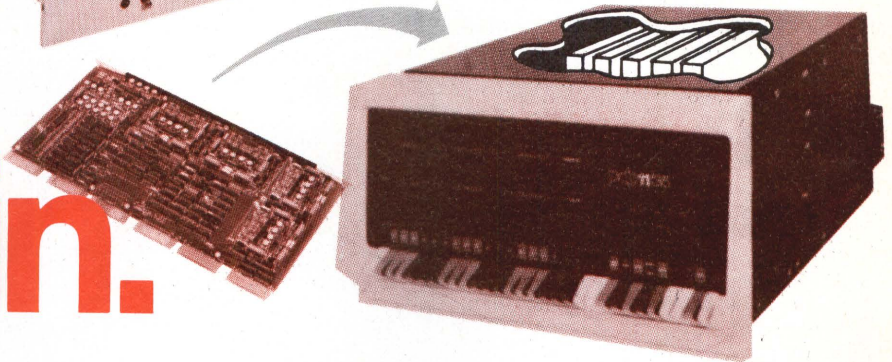
Devices include 1648B voltage controlled oscillator, 1650B and 1651B dual A-D comparators, 1658B voltage-controlled multivibrator, 1660B (high Z) and 1661B (low Z) dual 4-input gates, 1662B (high Z) and 1663B (low Z) quad 2-input NOR gates, 1664B (high Z) and 1665B (low Z) quad 2-input OR gates, 1666B (high Z) and 1667B (low Z) dual clocked R-S flip-flops, 1668B (high Z) and 1669B (low Z) dual clocked-latch flip-flops, 1670B (high Z) and 1671B (low Z) master-slave type D flip-flops, 1672B (high Z) and 1673B (low Z) triple 2-input exclusive-OR gates, 1674B (high Z) and 1675B (low Z) triple 2-input exclusive-NOR gates, 1690B UHF prescaler type D flip-flop, and 1692B quad line receiver.

Circle 156 on Inquiry Card

Low Cost Electronic Cash Register Has Upgrade Capability

All features of higher priced, stand-alone electronic cash registers (ECRs) plus capability of being upgraded to an in-store computerized checkout system are claimed to exist in the Datachecker® T-2500 system. According to Fred Bialek, vice president and general manager of National Semiconductor Corp's Systems

Div, 2900 Semiconductor Dr, Santa Clara, CA 95051, this ECR is priced approximately $1000 below comparable units which cannot be upgraded.

Datachecker ECR can handle over 140 coded items and has a non-tamperable, non-resettable group total. In addition, it offers food stamp eligibility and accounting by department, two clerk totals (clerk accountability), quantity extension (multiplication), split pricing, checks tendered, tax eligibility and accounting by de-

27

Presenting the OEM branch of Digital.

It's a complete family of computer tools. And it's growing every day.

Nine CPU's — from our smallest, the LSI-11, to our biggest and newest, the PDP-11/70 — with virtually every meaningful price/performance choice available in between. Choose one of them, and a whole world of possibilities opens up.

Proven operating systems offer real time, time-sharing, and batch capabilities, so you can choose the system that exactly fits your needs. Also you can hook up any of 60 different peripherals including your choice of 4 different disc drives, 5 terminals, 3 tape systems, 6 line printers — among a host of others.

What's more, you can join a special family called DECUS (Digital Equipment Corporation Users' Society) and instantly put at your disposal a whole library comprised of thousands of applications software packages.

And then you can start to plan your future. Your next new product, your next PDP-11 or PDP-8 computer. And to help you along the way, our family includes 2400 field service experts ready to lend a hand when and where you need it. And that means everything from operator training programs that get you quickly up to speed, to the new OEM Referral Program that helps you market your product.

When an OEM chooses a computer company, he makes a big decision with important long-term consequences. The OEM branch of Digital gives you a computer family you'll never outgrow.

To find out more, call or write Digital Equipment Corporation, Maynard, Massachusetts 01754. (617) 897-5111. European headquarters: 81 route de l'Aire, 1211 Geneva 26. Tel: 42 79 50. Digital Equipment of Canada, Ltd.

digital

Software Package Reduces Disc Storage Requirements

A data compression software package for IBM System/360 or /370 users is claimed to significantly reduce the amount of disc storage required for data in either batch or online applications. The package is designed to use minimal CPU time for compression/expansion. Benchmarks have indicated that Shrink requires about one CPU second per 100 kilobytes of compressed data on a System/370 model 158. To achieve minimal CPU usage, Shrink compiles the compression/expansion code tailored to file characteristics. Shrink modules require 8K of core, plus a variable amount per file.

The Programming Methods Div of GTE Information Systems, 1301 Avenue of the Americas, New York, NY 10019 reports that the package has attained compression results of 50 to 75% on average data files and has resulted in substantial dollar savings. For example, a large user with a file of four disc packs could potentially see a reduction of two or more packs. File storage savings vary depending on the data being compressed. Shrink can compress any type of data and requires no knowledge of the data; however, some knowledge of the data being compressed will achieve a higher compression ratio and increased storage savings.

Shrink consists of a CALLable routine that can be invoked by any program to compress a record before writing and to re-expand the data after reading. The system also includes a utility program to facilitate conversion of a user's existing files to compressed files. Files compressed using Shrink will also be supported by the Intercomm File Handler and other teleprocessing monitors such as CICS.

Circle 157 on Inquiry Card

Program Packages Perform Powerful Statistical Analyses

Four statistical program packages—Analysis of Variation (ANOVA), Nonparametric Statistics, Regression, and Sequential Analysis—have been announced by Wang Laboratories, Inc, 836 North St, Tewksbury, MA 01876 for its family of small computers. All are written in the company's Extended BASIC and are available on magnetic tape cassettes.
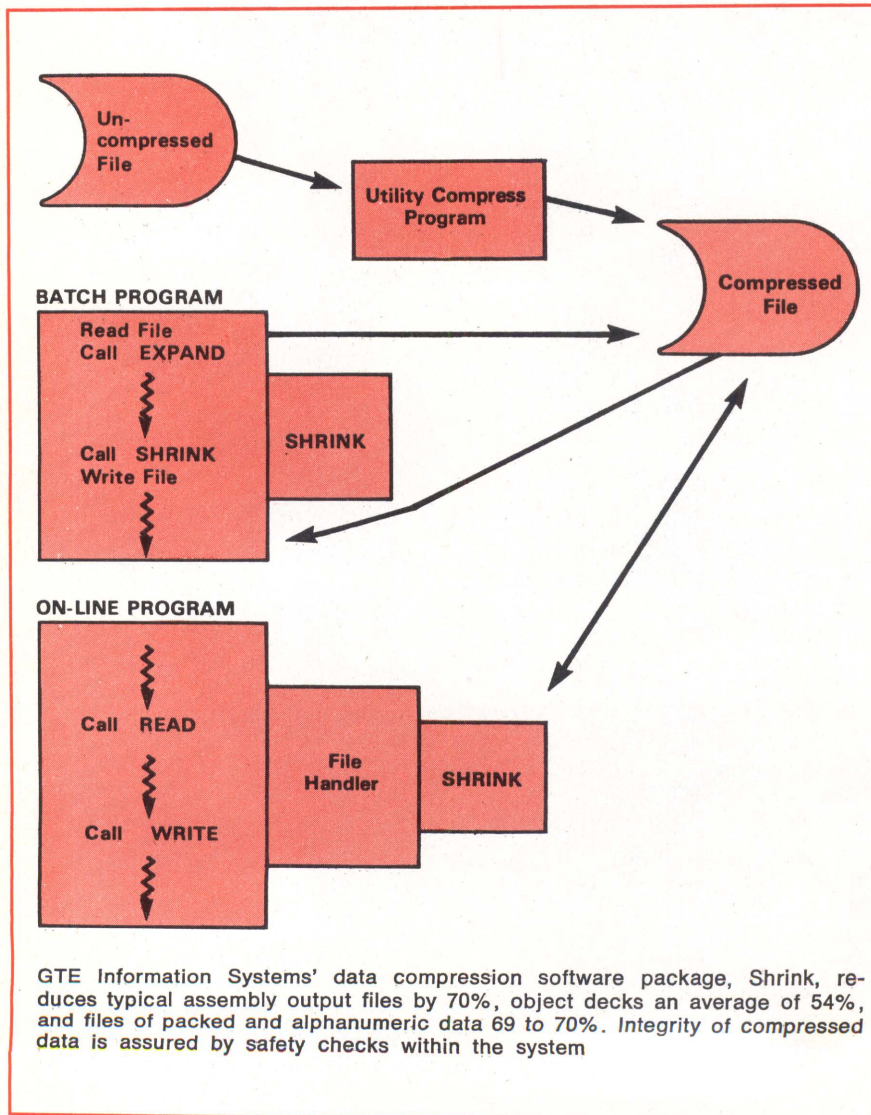
The ANOVA package contains routines to perform statistical analysis using standard ANOVA techniques. Routines perform 1-, 2-, and 3-way ANOVA with equal or unequal cell frequency; Latin Squares analysis; and 2- and 3-factor ANOVA with equal or unequal cell frequency or with repeated measures on the terminal factor. The user can prestore data on tape cassettes.

Nonparametric Statistics contains 25 of the most commonly used nonparametric tests. Programs handle 1-sample as well as 2-sample and K-sample cases with related and independent samples. The user is given options for printed output and data storage.

The Regression package contains 12 routines for both simple and multiple regression analysis. Special features include the ability to prestore data on tape cassettes, to plot data points and the regression curve, and to weight each observation individually. Routines perform linear, geometric, exponential, or polynomial regression by the method of least squares; as well as stepwise regression (simple polynomial and multiple linear).

Sequential Analysis contains seven of the most frequently used sequential probability ratio tests for testing a simple hypothesis against a simple alternative. Options are available for tabular and graphical display of acceptance and rejection numbers and for plots of the operating characteristics and average sample number curves.

Circle 158 on Inquiry Card

GTE Information Systems' data compression software package, Shrink, reduces typical assembly output files by 70%, object decks an average of 54%, and files of packed and alphanumeric data 69 to 70%. Integrity of compressed data is assured by safety checks within the system

Single-Mask Technology Achieves High Yield Bubble Memories

An experimental magnetic bubble memory in which writing, reading, and erasing functions are accomplished by temporary changes of the sense of rotation of the drive field has been fabricated by Philips Research Laboratories, Eindhoven, The Netherlands. Whereas three or more masks are ordinarily required to process one chip for bubble memories that are controlled by current pulses and a rotating magnetic drive field, this prototype memory needs only one mask per chip, resulting in high yield. Permalloy T-bar structures are used for bubble propagation, and special transfer switches perform the writing, erasing, and transfer functions between major and minor loops.

In the organization of the experimental memory (Fig. 1), a bubble originating from the generator can be passed selectively through the generator lock to the major loop. Bits (b_1, . . . , b_n) of a word with bit distance p circulate inside the major loop as a string. They can be stored in parallel in minor loops (L_1, . . . , L_n) by activating input switches ($T_{1,in}$, . . . , $T_{n,in}$) at the right moment. (Note that the distance between corresponding positions in two adjacent minor loops equals the bit distance.) For reading, the bits are again transferred, via output switches ($T_{1,out}$, . . . , $T_{n,out}$), to the major loop. Information can be erased selectively from the major loop by directing the corresponding bubbles through the annihilator lock to the annihilator.

The function of a basic generator lock (Fig. 2) is to pass a bubble selectively from its input to its output Permalloy track, which leads to the major loop. The three parallel paths (a, b, and c) lead to an annihilator. These paths and the output path (d) can be selected by the corresponding transfer switches ($T_a \rightarrow T_{b1}$, $T_{b2} \rightarrow T_{c1}$, and $T_{c2} \rightarrow T_d$), having a length of 1 drive-field periods (1 = 7/4).

Essential elements in the transfer switches are the asymmetric Permalloy Y's. In a counterclockwise (CCW) field, bubbles on path a move from right to left. Changing the sense of rotation to clockwise (CW) at the moment a bubble is in position
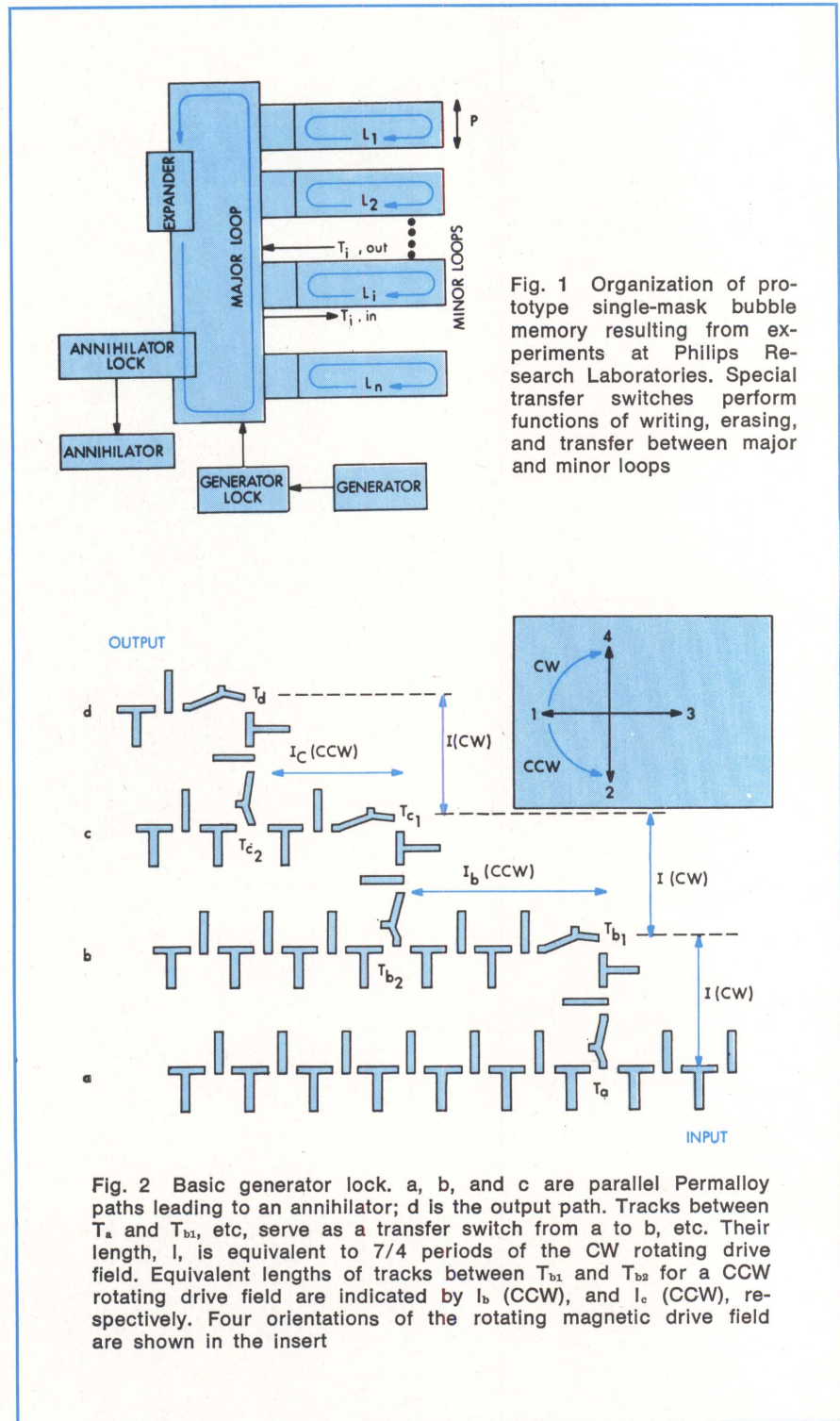
Fig. 1 Organization of prototype single-mask bubble memory resulting from experiments at Philips Research Laboratories. Special transfer switches perform functions of writing, erasing, and transfer between major and minor loops
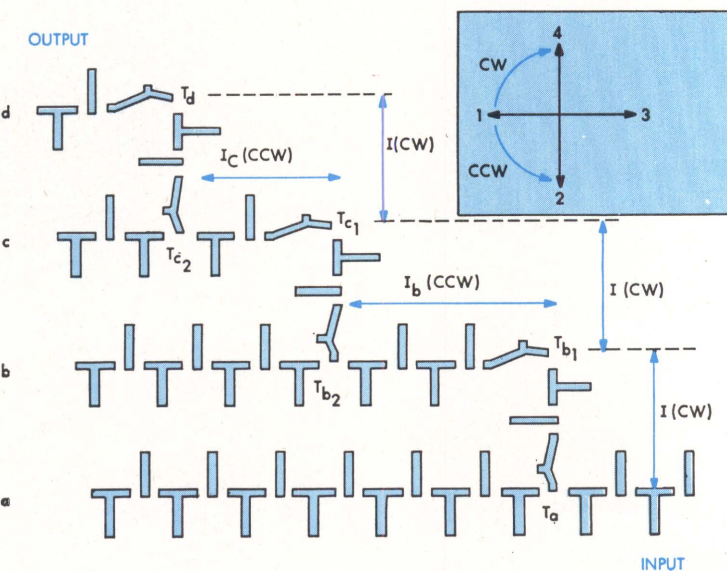
Fig. 2 Basic generator lock. a, b, and c are parallel Permalloy paths leading to an annihilator; d is the output path. Tracks between T_a and T_{b1}, etc, serve as a transfer switch from a to b, etc. Their length, l, is equivalent to 7/4 periods of the CW rotating drive field. Equivalent lengths of tracks between T_{b1} and T_{b2} for a CCW rotating drive field are indicated by l_b (CCW), and l_c (CCW), respectively. Four orientations of the rotating magnetic drive field are shown in the insert

T_a forces the bubble to move upward because the leg of the Y at T_a forms the most attractive pole. After one period, the bubble has arrived at T_{b1}. Again reversing the sense of rotation to CCW at that moment moves the bubble to the left into path b. In this way, the bubble is shifted from path a to output path d by execution of the program (ex-

INTRODUCING µCOM-8.
THE MICROCOMPUTER SYSTEM FROM
A $BILLION COMPANY
YOU'VE NEVER HEARD OF.

INTRODUCING A FAMILY OF 4K RAMS FROM A $BILLION COMPANY YOU'LL HEAR A LOT MORE ABOUT.

Introducing NEC. Japan's giant $1.6 billion Nippon Electric Company Ltd.

And its brand-new American subsidiary— NEC Microcomputers, Inc.

A company that can sell you everything from complete state-of-the-art microprocessor systems to a whole line of semiconductor memories. Direct from its own North American inventory.

NEC microcomputers, inc.

A 150NS RAM.
PLUS A WHOLE LINE OF MEMORIES
WITH A BRAND·NEW FEATURE.
RELIABILITY.

Our line of 22-pin 4K RAMs starts with the fastest in the industry — our 150ns μPD411D-3. But that's only the beginning.

The μPD411 family also includes 4K RAMs with access times of 200, 250, 300 and 350ns.

In addition, we have other RAMs, ROMs, PROMs, both MOS and bipolar, and associated products — all designed to second-source the most popular memories in the business. With one important difference.

We make our components to the highest standards of reliability in the industry.

Here's how:

First, we're not wedded to any one MOS process. We use both metal gate and silicon gate construction — whichever is best for the particular product.
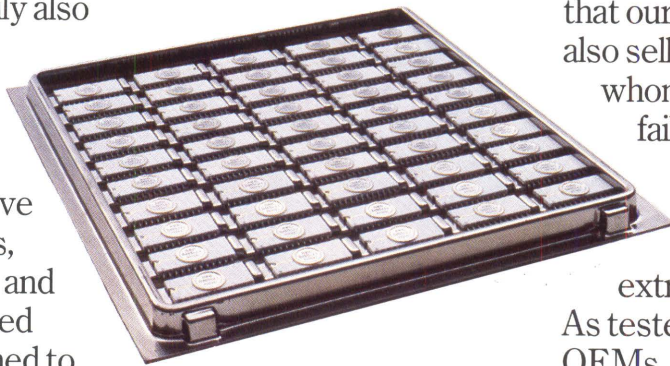
Secondly, on all our components, we use a unique anodized aluminum passivation process, an NEC breakthrough.

Thirdly, we employ 100% dynamic burn-in to virtually eliminate infant mortality.

Fourthly, contamination levels in our processing areas are less than 10 ppm.

All this concern over quality stems from the fact that our parent company also sells to people for whom traditional failure rates are wholly unacceptable. Even the specs are extremely conservative. As tested by American OEMs, the slowest performance to date for our 150ns 4K RAM is 130ns.

It's a whole new concept in semiconductor devices. Reliability. Designed in. Built in. And tested to prove it.

And it's available in large volume. From just one source:

NEC microcomputers, inc.

Five Militia Drive Lexington, MA 02173 617-862-6410

µCOM-8.
THE FIRST MICROCOMPUTER SYSTEM TO BE SOLD LIKE A COMPUTER, INSTEAD OF A BUNCH OF COMPONENTS.

Introducing the world's newest microcomputer system — the µCOM-8.

At its heart is the µPD8080 — a state-of-the-art 40-pin microprocessor that's both software and pin compatible with Intel's new 8080A.

A microprocessor that gives you everything the 8080 does — and more.

And it's complemented by a full line of NEC's own RAMs, ROMs, PROMs, I/O and peripheral circuits.

But what really distinguishes the µCOM-8 from every other microcomputer system on the market is that we sell it like a computer. Instead of a bunch of components.

And that means commitment to total support.

We start with the µCOM-8 EVAKIT — a designer's evaluation kit for those of you who don't have the time to wire up a chip set to start your evaluation. The Kit is a 1K microcomputer that lets you write and execute programs and exercise complete control via a 110 Baud ASR 33 Teletype and a manual break point pushbutton. It comes with a monitor program, a complete documentation package, and a unique instruction reference guide, all to help make you an accomplished programmer — fast.

For those of you who can start designing in the µCOM-8, its processors, memories, etc., right now, we offer even more.

A Software Manual unlike any software manual you've ever seen. It takes a conceptual, problem-solving approach that can get you right into your application, even if you've had no prior programming experience.

Application Notes to help you with overall I/O design and operation.

Cross Assembler and Simulator Programs and a Program Library, available through time sharing services, or installed on your own computer system.

Or, if you don't want to use the Cross Assembler and Simulator Programs, a PDA-8
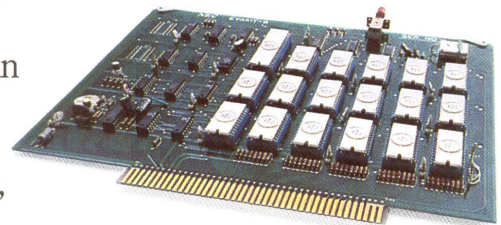
Program Development Aid for assembling, tracing, and debugging programs.

And, finally, a responsive, in-depth applications engineering service, available nationwide.

WHAT WE'VE GOT.

Microprocessor Products

Memories

Product Code	Description	Access Time (n sec)
μPD411D-E	4K Dynamic RAM	350
μPD411D	4K Dynamic RAM	300
μPD411D-1	4K Dynamic RAM	250
μPD411D-2	4K Dynamic RAM	200
μPD411D-3	4K Dynamic RAM	150
μPB2089D/2289D	64 Bit Static RAM	60, 35
μPB2200D/2202D	256 Bit Static RAM	50, 65
μPB2206D	256 Bit Static RAM	50
μPB10142D/10148D*	64 Bit Static RAM	10, 15
μPB10144D*	256 Bit Static RAM	25
μPD404D	1K Dynamic RAM	250
μPD405D	1K Static RAM	85
μPB403D	1K Mask Prog. ROM	60
μPD454D	2K Erasable PROM	800
μPD464D	2K Mask Prog. ROM	800
μPD465D	8K Mask Prog. ROM	600
μPD466D	16K Mask Prog. ROM	500
μPB246D	Quad Clock Driver	30 T_{pd}

*Indicates ECL compatible, all others TTL compatible.

Microprocessor Products list:

- μPD8080D — 8 Bit Central Processing Unit — 2MHz
- μPD8080D-1 — 8 Bit Central Processing Unit — 1MHz
- μPD411D-1 — 4096x1 Bit Dynamic RAM 250ns
- μPD412D — 256x4 Bit Fully Decoded Static RAM — 1.0μs
- μPD454D — 256x8 Bit Elect. Alterable PROM — 800ns
- μPD464D — 256x8 Bit Mask Programmable Static ROM — 800ns
- μPD465D — 1024x8 Bit Mask Programmable Static ROM — 600ns
- μPD466D — 2048x8 Bit Mask Programmable Static ROM — 500ns
- μPB246D — Quad TTL to MOS Clock Driver
- μPD754D — 8 Bit Latch
- μPD369D — Universal Asynchronous Receiver/ Transmitter
- EVAKIT-8 — Microcomputer Evaluation Kit
- PDA-8 — Prototype Development Aid

The above is only a partial listing of our products. For a complete list, including data on compatibility with competitive products, simply call your nearest NEC rep.

WHERE TO BUY THEM.

New England:
Circuit Sales Company
Lexington, MA
617/861-0567

Mid-Atlantic:
Trionic Associates, Inc.
Great Neck, NY
516/466-2300

C.H. Newson & Associates
Philadelphia, PA
215/248-3377

C.H. Newson & Associates
Hershey, PA
717/233-8576 (Harrisburg Area)
301/825-0001 (Baltimore Area)

Southeast:
Perrott Associates, Inc.
Orlando, FL
305/275-1132

Perrott Associates, Inc.
Clearwater, FL
813/726-1549

Midwest:
McFadden Sales, Inc.
Columbus, OH
614/221-3363 (Cleveland Area)
614/221-3363 (Fort Wayne Area)
614/221-3363 (Indianapolis Area)

Bitronics Sales Company
Minneapolis, MN
612/835-7744

RF Specialists
Park Ridge, IL
321/698-2044

Southwest:
Merino Sales Company
Dallas, TX
214/233-6002

No. California:
Trident Associates
Mountain View, CA
415/967-7031

So. California:
Electronic Component Marketing
Woodland Hills, CA
213/340-1745

Electronic Component Marketing
El Toro, CA
714/830-3939

Electronic Component Marketing
San Diego, CA
714/295-6122

NEC microcomputers, inc.

Five Militia Drive Lexington, MA 02173 617-862-6410

pressed in periods of the drive field):
1(CW), 1_b(CCW), 1(CW), 1_c(CCW), 1(CW).

Bubbles are obtained at the proper bit distance in the major loop as long as the difference between the total number of CCW and CW periods equals p. The annihilator lock operates in a similar manner.

Different locks required on different chips are obtained by varying the CCW distances (1_b and 1_c). Furthermore, the corresponding transfer switches are given different orientations so that they start operating at different orientations of the drive field when it is switched from CCW to CW rotation. Therefore, functions can be performed independently on different chips. A thick chevron expander, which gives the bubble a strongly elongated shape, is used for magneto-resistive detection.

As compared to a conventional current-controlled bubble memory, the present prototype (Fig. 3) has some-what longer access times for writing and erasure, while the bit density is somewhat smaller. However, it has the advantage of simple technology, which is of interest for future developments with smaller bubbles. Results described here refer to laboratory experiments; they do not necessarily imply a follow-up in production or marketing by Philips.

10-km Optical Waveguide Eliminates Need for Intermediate Repeaters

Transmission of 100-MHz signals over a 10-km distance using an optical waveguide can now be accomplished without intermediate amplification or enhancement. Fabricators of the 6.2-mi long single strand, the Research Laboratories of Corning Glass Works, Corning, NY, state that capability is equivalent to the transmission of 33.000 telephone conversations one-half the length of Manhattan Island—in a cross-sectional area the diameter of a human hair—without repeaters.

Attenuation in tests has been shown to be 5.4 dB/km at a 799-nm wavelength. Pulse broadening is 1 ns/km. Although an LED laser was used, helium neon or neodymium lasers could also serve as light sources.

The longest optical waveguide previously fabricated by Corning was a 3-km length delivered to the Naval Electronics Laboratory Center in San Diego, Calif. However, the 3-km fiber does not have as much bandwidth capability as the 10-km low-loss optical waveguide which was made by Corning's doped deposited silica process. This process radially grades the index of refraction in the waveguide and provides the precision needed to equalize the path length for light rays traveling at various angles. Pulse dispersion, which limits information-carrying capacity, is thereby reduced. The process also allows tight control of attenuation (light loss).

The 10-km length is significant because that distance is the typical spacing between relay stations in long-line optical communications systems. The most likely potential users in the U. S. would be telephone companies. Overseas applicability includes CATV.

The 10-km optical waveguide was fabricated as a prototype and to prove that it could be accomplished. Although another could be made if the need arose, Corning is not presently marketing a 10-km length.
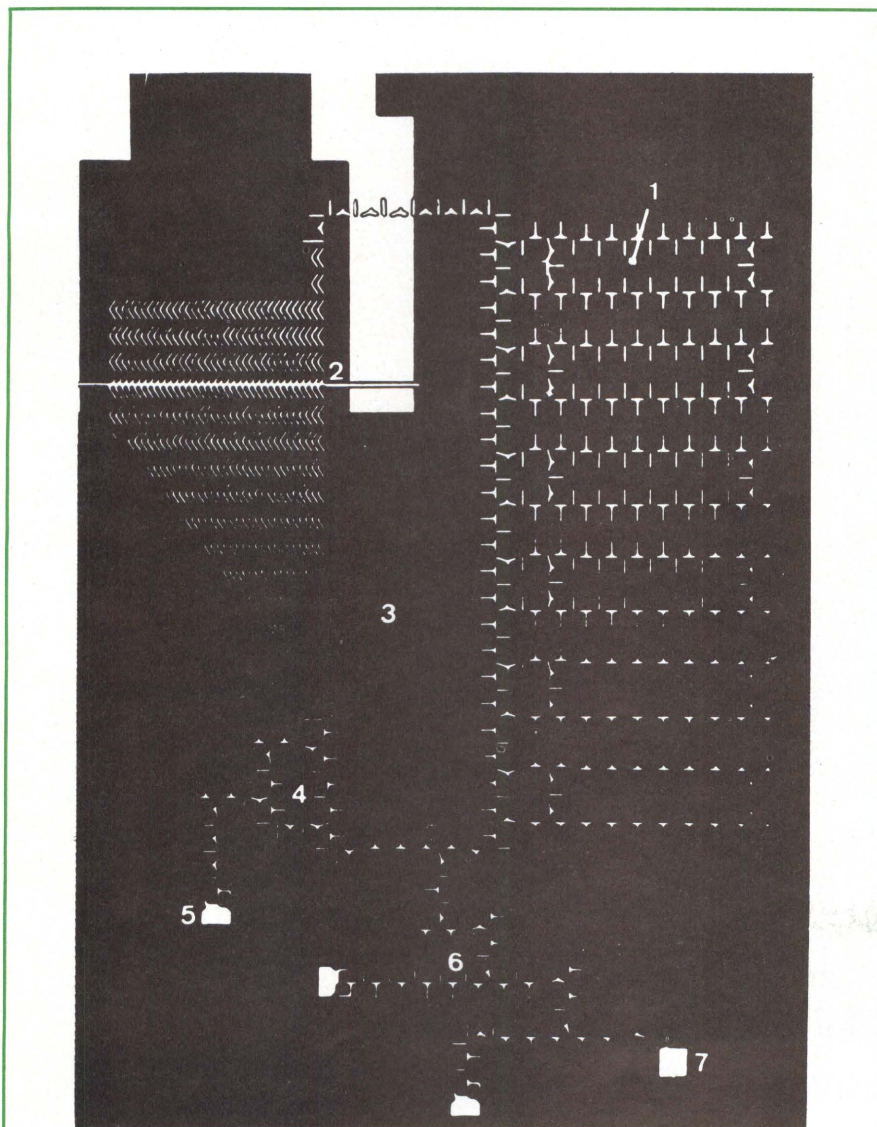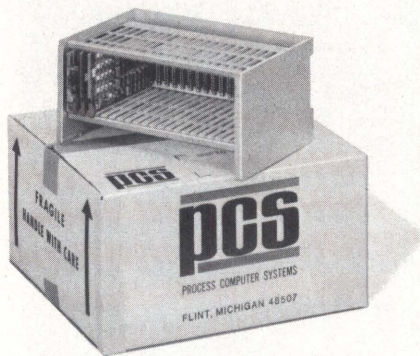

Fig. 3 Photograph of experimental single-mask bubble memory. (1) minor loop; (2) magneto-resistive detector; (3) major loop; (4) annihilator lock; (5) annihilator; (6) generator lock; (7) generator. Functions are accomplished by temporary changes of the sense of rotation of the drive field
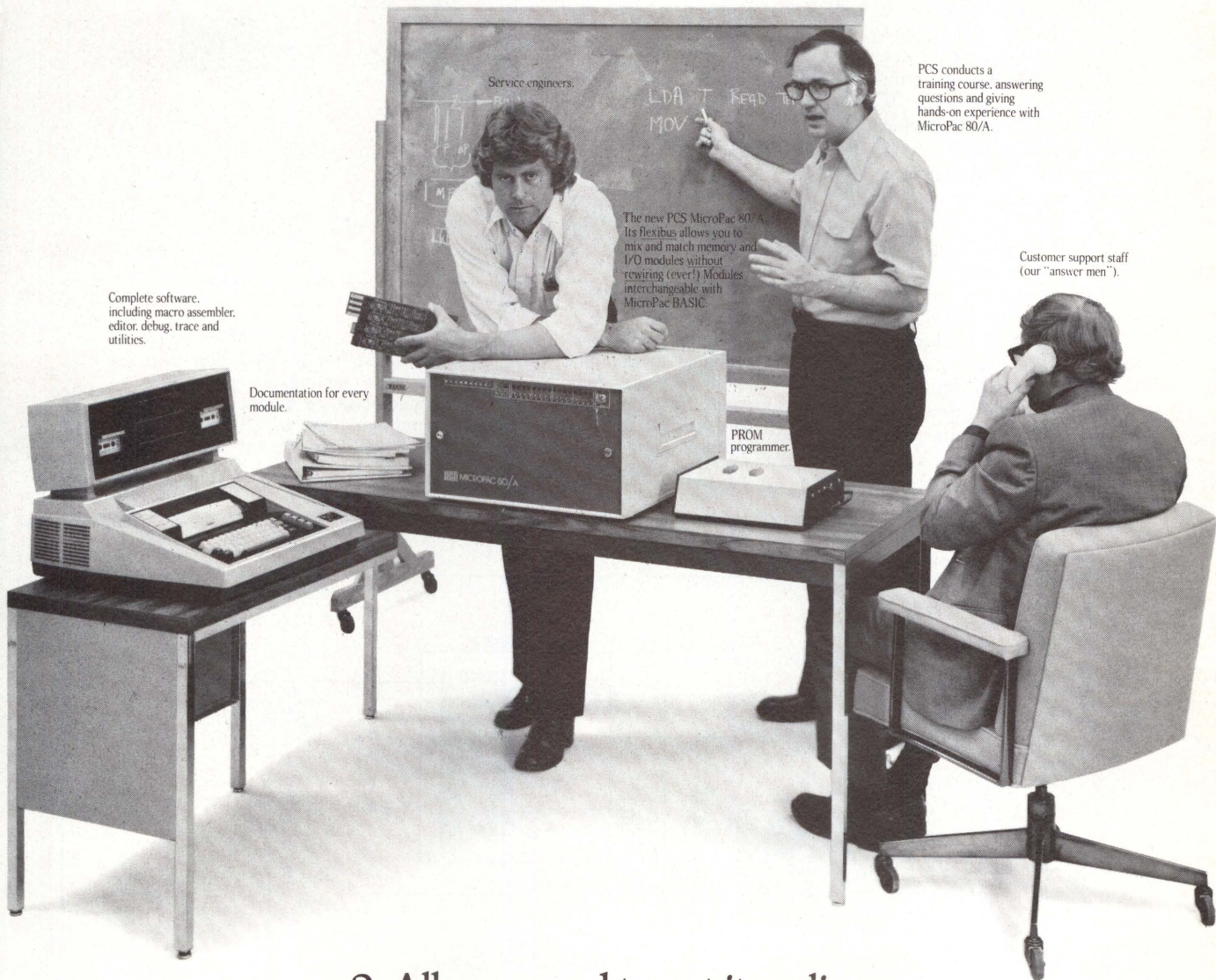
Two reasons why Micro

1. MicroPac BASIC.

A microcomputer control system <u>you</u> configure from inexpensive standard modules. Available in quantity, 30 day delivery.

DI, DO, TTY, TTL, A/D, D/A, communications modules, all exist <u>now</u>. All are factory tested and field proven.

Pac leads the micro pack

Service engineers.

PCS conducts a
training course, answering
questions and giving
hands-on experience with
MicroPac 80/A.

The new PCS MicroPac 80/A.
Its flexibus allows you to
mix and match memory and
I/O modules without
rewiring (ever!) Modules
interchangeable with
MicroPac BASIC.

Customer support staff
(our "answer men").

Complete software,
including macro assembler,
editor, debug, trace and
utilities.

Documentation for every
module.

PROM
programmer.

2. All you need to get it on line.

pcs Suddenly, the whole business
of industrial control has changed.

5467 Hill 23 Drive, Flint, Mich. 48507 Phone (313) 767-8920 TWX 810-235-8667

IN AUSTRALIA: Jacoby, Mitchell Ltd. (02 630 7400) AUSTRIA: Unitechnik (0222 9510 433) BENELUX: Geveke Elektronica en Automatie bv (020-802 802)
CANADA: Cantech Controls Ltd. Calgary (403- 252-8151) Edmonton (403- 425-9810) Vancouver (604- 736-2851) Toronto (416- 438-6907) Montreal
(514- 636- 8364) Halifax (902- 429-9103) Sarnia (519- 862-1911) DENMARK: Erik Ferner A S (01 31 16 07) ENGLAND: Computing Techniques Ltd. (040 381
3171) FINLAND: Erik Ferner OY (90- 88 06 34) FRANCE: Aeromaritime Electronique (533-67-00) GERMANY: Neumueller Messtechnik GmbH (089- 5991-1)
ISRAEL: Information Systems, Ltd. (Tel. 410 565) NORWAY: Erik Ferner A S (02 54 43 26) SPAIN: Neotecnica, S.A.E. (248 96 02) SWEDEN: Erik Ferner AB
(08- 80 25 40) SWITZERLAND: Lacoray S.A. (01 56 56 70)

Multiplexed System Doubles Data Capacity of Transmission Lines

A joint effort of AT&T, Bell Telephone Laboratories, and Western Electric has resulted in development of a transmission system that doubles the amount of data that can be sent over cable connecting telephone switching offices. The 3.152-megabit/s T1C system can provide 48 one-way voice channels over each pair of wires in an exchange cable—twice the capacity of the 24-channel, 1.544-megabit/s T1 system now in use. Error-rate performance objective is to have 95% of the systems with accuracy of better than 10^{-6} in the worst-case 50-pair unit when normalized to a system length of 50 mi.

Design and engineering objectives were to develop a system of higher capacity that would be compatible with the T1 so as to facilitate its acceptance. This necessitated development of a new digital repeater, an improved repeater housing, more flexible office repeater bays and arrangements, an appropriate multi-
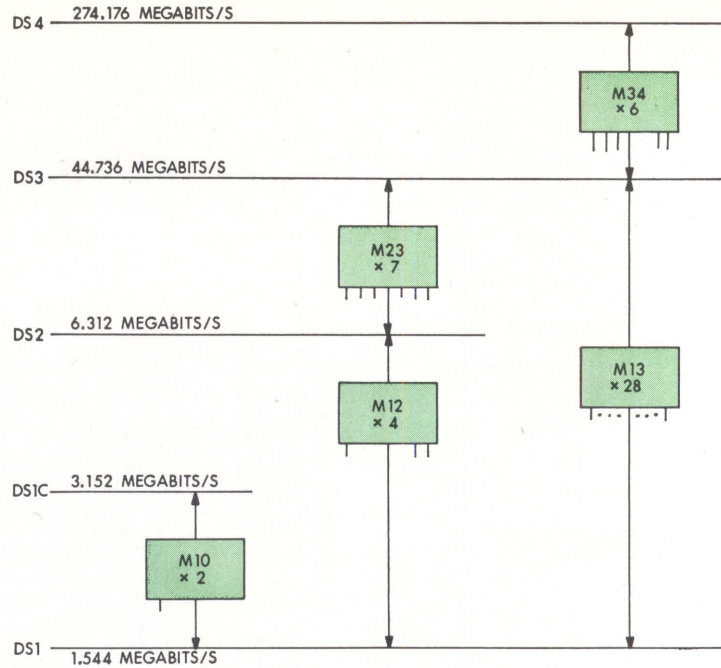
Interconnection of various network transmission levels by multiplex terminals to combine lower bit-rate signals for transmission over higher bit-rate facilities. M1C multiplex combines two 1.544-megabit/s signals into a single 3.152-megabit/s signal for transmission over the T1C line. Positive pulse stuffing synchronizes incoming signals followed by bit-by-bit multiplexing of the synchronized signals
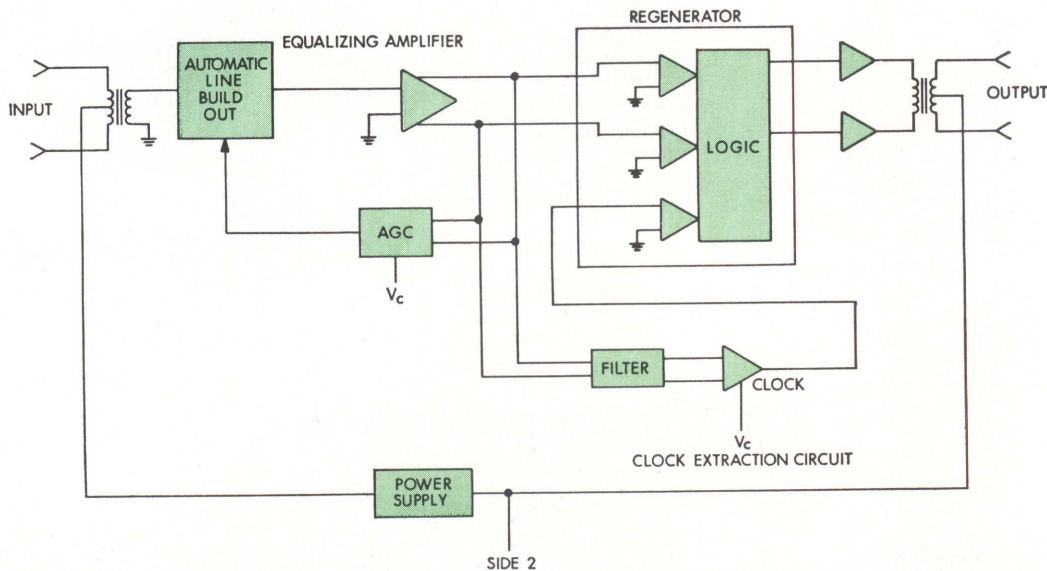
Simplified block diagram of 3.152-megabit/s repeater, consisting of two digital regenerators sharing a common power supply. Distorted and attenuated peak pulses from previous repeater are transformer-coupled into equalizing amplifier which restores their amplitude and compresses most of the pulse energy into two time slots. Clock extraction circuit recovers timing and pulse width information; regenerator makes time and amplitude decisions on the amplifier output and drives the next cable section with pulses of the correct amplitude and width

Granted, our new ADM-3 is basic. Especially if you compare it with all the smart video terminals around (our ADM-1 or -2, for example). But the $995 unit price puts it into a different perspective.

As simple as it is, the ADM-3's one-card brain can help you move a lot of data. And it's compatible with most popular computers. That means, it fits all kinds of applications. Including yours.

Here's what you get for $995. 12" diagonal screen. Full or half duplex operation at 11 selectable data rates. Bright, easy-to-read characters — 960 or 1920,* displayed in 12 or 24 rows of 80 letters. 59 data entry keys arranged like on a typewriter which keeps operator training short and basic, too. What's more, our ADM-3 is alert. It says "beep" when you come to the end of a line. The rest of the time, it just keeps cool and quiet.

Our DUMB TERMINAL also offers you room for

*1920 Characters is an option available at additional cost.

improvements. Its RS 232C interface extension port lets you hook up hard copy printer, magnetic tape recorder or additional (smarter) data terminals. And with a few options, you can make our ADM-3 answer back. Increase its vocabulary by adding upper and lower case. Transmit and receive independently selectable rates. Even enter just numbers on a numeric key pad.

After counting all its limited blessings, you have to admit one thing: you simply couldn't ask for more for $995. At this low level, you can afford to order a dozen or more DUMB TERMINALS (and buy them at our even lower quantity discount price).

DUMB TERMINAL. SMART BUY.

LEAR SIEGLER, INC.
ELECTRONIC INSTRUMENTATION
DIVISION DATA PRODUCTS

LSi

714 N. Brookhurst St.
Anaheim, CA 92803
Telephone:
(714) 774-1010

INTRODUCING THE $995 DUMB TERMINAL.

plex to combine two T1 signals, a family of test sets, and system design guidelines. Both systems operate on a wide variety of types of exchange-grade twisted-pair cable with identical maximum repeater spacings of 6300 ft. Each system has a recommended range of 50 regenerative sections and uses bipolar format, automatic line buildout, self-timed regenerators. However, the T1C requires a multiplex to time-interleave two T1 signals into a single signal.

Digital multiplex M1C, a 2-way digital terminal, time-division multiplexes and combines the signals from two asynchronous 1.544-megabit/s T1 facilities into a composite 3.152-megabit/s signal suitable for transmission over a T1C digital line. In essence, it provides a digital interconnection between the existing T1 level and the new T1C level.

Each of the 1.544-megabit/s signals can originate from a T1 line, a voice or data terminal, or any other equivalent source. T1 bipolar inputs are converted to unipolar signals and bit-by-bit interleaved. Synchronization is achieved by pulse stuffing, and extra pulses are added for framing and destuffing. The resultant 3.152-megabit/s unipolar signal is then converted to bipolar format for transmission over a T1C line.

Multiplexing is performed by circuits known as muldems, (*multiplexer/demultiplexers*) which terminate one end of the T1C line. Each muldem is made up of two synchronizer/desynchronizers (syndes), a transmitter, receiver, and muldem alarm. A multiplex bay contains up to 48 muldem units plus maintenance, protection, and power equipment.

The 3-level, bipolar-coded line format from the multiplex permits achievement of the required line rate with maximum repeater spacings. A line repeater performs the three basic functions of equalization, clock extraction, and regeneration required for digital transmission.

Extensive use of hybrid integrated circuit technology in the line repeater allows for small size and high reliability. Features include automatic line buildout for increased operating margin and a quartz-crystal timing recovery filter for long-term accuracy over wide temperature variations. Office repeaters, in which span lines terminate, provide signal regeneration as well as line current

regulation for simplex powering of the repeater line.

A successful field trial of 50 T1C systems operating in a single cable over a 6-mi span was recently completed in metropolitan Atlanta, Ga. Equipment is being shipped from the Western Electric Co's Merrimack Valley Works for the first T1C installation at the Southern Bell Telephone and Telegraph Co in Miami, Fla, planned for late this year.

For further information on phases of the T1C transmission system, refer to the following papers, published in the *Conference Record of the 1975 IEEE International Conference on Communications*:

J. A. Lombardi, R. E. Maurer, and W. P. Michaud, "The T1C System"

J. P. Fitzsimmons and W. J. Mayback, "Engineering T1C Carrier Systems"

A. Anuff, J. F. Graczyk, J. J. Ludwick, and E. T. Mackey, "A New 3.152 Mb/s Digital Repeater"

J. D. Moore, "M1C Digital Multiplex"

R. S. Burnell, W. A. Janicki, and F. E. Webber, "Central Office Repeater and Equipment Arrangement for T1C"

D. V. Anderson, B. B. Garg, and P. F. Molander, "T1C System Maintenance and Test Equipment"

Gallium Arsenide Used for Low Cost, High Efficiency Solar Cells

A semiconductor material utilized extensively for electronics has been used to fabricate a solar cell that measures only ⅛ in. dia but which produces 10 W of electricity directly from sunlight. According to Varian Associates, Palo Alto, Calif, whose scientists have developed a gallium arsenide (GaAs) solar cell, most solar-electric research, development, and production have been concentrated on silicon-based systems. Ronald L. Bell, director of Varian's Solid State Laboratory, says that "other solar energy materials require 1000 times the surface area to produce the same amount of energy (as GaAs)."

Unlike silicon, which cannot function effectively at high temperatures or with high electric current densities, GaAs operates at 20% efficiency with highly concentrated sunlight. Varian plans to construct a series array of 100 GaAs cells that will produce 1 kW of power; larger series

to obtain megawatt-rated systems are feasible. Installation of such large generating arrays would have negligible environmental side effects because of the high efficiency and reduced space requirement for the arrays. They will function efficiently in any sunny climate during the day, whenever the sky is clear enough for the sun to produce well defined shadows.

In the experimental GaAs solar generator, sunlight is concentrated by a factor of 1000 through a concave reflector which focuses the collected sunlight on the solar cell. An economically practical generating system would use large numbers of GaAs cells, each with its own reflector, arrayed on a frame that would turn slowly from sunrise to sunset to follow the sun. This would permit 40% more sunlight to be utilized each day than with immovable flat panel arrays.

Portions of Ballistic Missile Defense EDP Computer Demonstrated

Major parts of the Parallel Element Processing Ensemble (PEPE) were recently demonstrated to members of the Dept of the Army Ballistic Missile Defense Advanced Technology Center by Burroughs Corp's Federal and Special Systems Group, Paoli, Pa. Hardware for the PEPE system is being developed by Burroughs under subcontract with System Development Corp.

The system includes three input/output control processors generating instructions for multiple processing elements which operate in parallel to achieve ultrahigh computational speeds. Each element will execute 1 million instructions/s, and will have an independent memory capable of storing up to 1 thousand 32-bit words of information. Initially, the system will use medium-scale integrated circuits and emitter-coupled logic; future plans call for use of large-scale integrated circuitry.

Portions of the system demonstrated included the processing element and its software, the power distribution segment with its power supply and associated backplane wiring, and the signal distribution subsystem. In addition, a specially-modified B 1714 computer system, used as the test and maintenance processor, was shown. Delivery and installation of the complete PEPE system is scheduled for 1976. □

CANNON® COST CUTTERS:
FLEXIBLE INTERCONNECTION SYSTEM
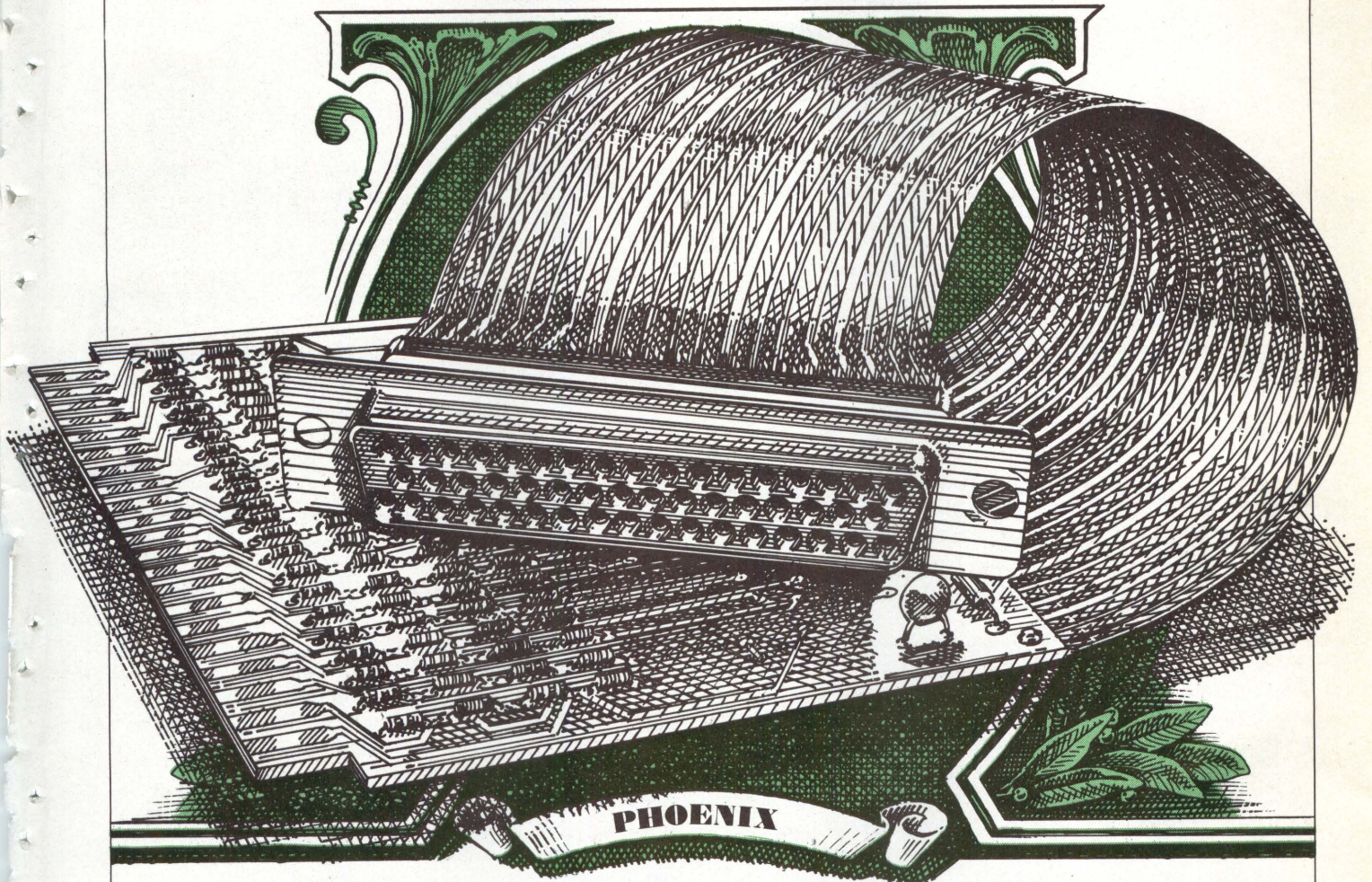
PHOENIX

IT LOWERS YOUR TOTAL INSTALLED COST.

Want to cut your system costs as much as 50%? Reduce your weight and space as much as 80%? And eliminate point-to-point wiring, bundling and lacing? Our Phoenix facility can achieve it, whether you need a printed circuit, flex circuit, components on your printed or flex circuit, or terminations. We can give you any of the components alone, or a complete package.

By combining connector and circuitry capabilities we can offer a complete system, 100% electrically and mechanically checked out, ready to plug into your assembly. All our manufacturing procedures meet latest IPC standards as well as MIL-P-50884. Testing is in accordance with MIL-P-5510. At Phoenix we can do everything — from concept to production. And we do it all under one roof.

Applications: Computer mainframe • Medical instrumentation • Minicomputers • Process controllers • Power plants • Commercial and military aircraft.

Today, find out how Cannon interconnection innovations can lower your installed costs. Send for our "Cannon Cost Cutters" brochure. Contact ITT Cannon Electric, 2801 Air Lane, Phoenix, Arizona 85034. (602) 275-4792.

CANNON ENGINEERING LOWERS YOUR COSTS.

CANNON **ITT**

DDC Automates Chemical Reactor
at Pharmaceutical Manufacturing Plant

Results gathered and studied after one year of operation of a direct digital control (DDC) center in a pharmaceutical manufacturing plant show that the system has already paid for itself in terms of faster and safer production as well as improved product uniformity. The Burroughs Wellcome Co, manufacturer of ethical (prescription) drugs, installed the system in Feb 1974 to automate a 100-gallon Pfaudler-type reactor in the pilot plant section of its Greensville, NC Chemical Development Laboratories. Implementation of the system gave the process engineer precise control over all reaction parameters using only a simple code and a teletypewriter keyboard. After the original installation, the system was expanded to include another reactor, and a distillation column will be added later.

Inherent Process Problems

Pilot plant batch processes must be watched and controlled carefully. New reactions and variables are often involved which can lead to unpredictable, undesirable, or even dangerous results. A typical process in a 100-gallon Pfaudler as well as in other, smaller reactors involves a large number of manual manipulations of valves to carry out alternate steps of heating, refluxing, distillation, cooling, and adding reactants at various process stages.

Reactors are connected through glass piping to reflux and distillation condensers and to receivers which collect various fractions of the distillate. Although the pilot plant is operated on a single-shift schedule, some reactions often require longer than eight hours to complete; in the past, an operator had to be on duty for part or all of the night just to complete one or two operations that might require only a few minutes. In addition, an operator had to remain at the plant for an entire run to change setpoints of analog-controlled temperature, pressure, and flow variables at certain time intervals and to regulate settings on other less critical, uncontrolled switches and valves. The operator also had to switch from one condenser to another, change receiving vessels, and make reactant additions at prescribed intervals.

According to Dr Gabriel Cipau, head of Burroughs Wellcome Co's scientific computing department, DDC was initiated to eliminate these problems as well as to provide more precise control of the processes. In addition, an accurate data collection system required

to carry out sophisticated pilot plant experiments could be achieved only through automation.

System Selection Considerations

Several factors were considered by Burroughs Wellcome Pharmaceutical when choosing from among the several digital computers available in late 1973 that were capable of handling the process variable inputs, processing the information, and producing the output signals necessary to maintain the process program. Among the factors, in addition to price of the basic computer, was the cost of input/output (I/O) interfaces. Inherently incompatible interfaces would require expensive signal converters and conditioners, and would add potential trouble sources if not well matched to the remainder of the system.

The final choice was a dc^2 system made by Fisher Controls Co, Marshalltown, Iowa. Dr Cipau says that this system not only includes the required computer-sensors-controls interfaces but also uses a control-oriented, easily mastered programming language (pc^2, a simplified form of BASIC). The control program is permanently wired into read-only memory.

Solutions Resulting from DDC

As the pilot plant batch reaction proceeds, sensors installed at appropriate locations in the reactor/condenser/receiver system provide the computer with continuous analog inputs on temperatures in the reactor, in the vapor phase, and of the distillate; pressure/vacuum in the reactor; and distillate level in the two receivers. (Since all sensors, with the exception of those used to monitor reactor temperatures, originally supplied 4- to 20-mA signals directly to the computer interface, only the latter sensors had to be converted to provide the required signals.) All inputs are multiplex-scanned and transferred from the input interface into computer memory for future reference and comparison with the prescribed process parameters. Operator access to input data may be gained via a CRT data display, from records provided by a line printer, or from data typed on a teletypewriter at specified intervals, on command, or in alarm situations.

Before a batch process is started, the computer is given the set of instructions necessary for the particular pharmaceutical product or pharmaceutical intermediate to be prepared. These instructions, called the "application program," are entered by a high speed

Local or Remote...Using RTP.

Computer Products, Inc., provides a reliable, low-cost product line for your use in designing or implementing real-time measurement and control systems. We call it RTP...a family of standard subsystems for providing analog and digital inputs and outputs for digital computers. With the addition of PROCOM I, our microprocessor-based communications controller, the RTP products can be located many miles from your host computer.

To be useful to you, RTP should (and does) fulfill several practical requirements:

- It is plug compatible with any popular computer of your choice.
- It is extremely versatile...use it in local or remote applications, in large or small systems.
- It is fully documented.
- Delivery is virtually off-the-shelf.
- It's an established, reliable product line that's being used in hundreds of applications.

But how does it work? How can you use it?

We'd like nothing better than to explain it to you. Just circle our number on the Reader Service card, and we'll send you our brochure "Using RTP When Designing Computer-directed Measurement and Control Systems."

"Using RTP" will provide you with a clear system design overview so that you can order more literature for details about the RTP subsystem in which you may be interested. You'll get some good ballpark cost information, too.

Anxious? Call us at 305-974-5500. Ask for Larry Buck or Randy Dailey.

⏀ ComputerProducts,inc.
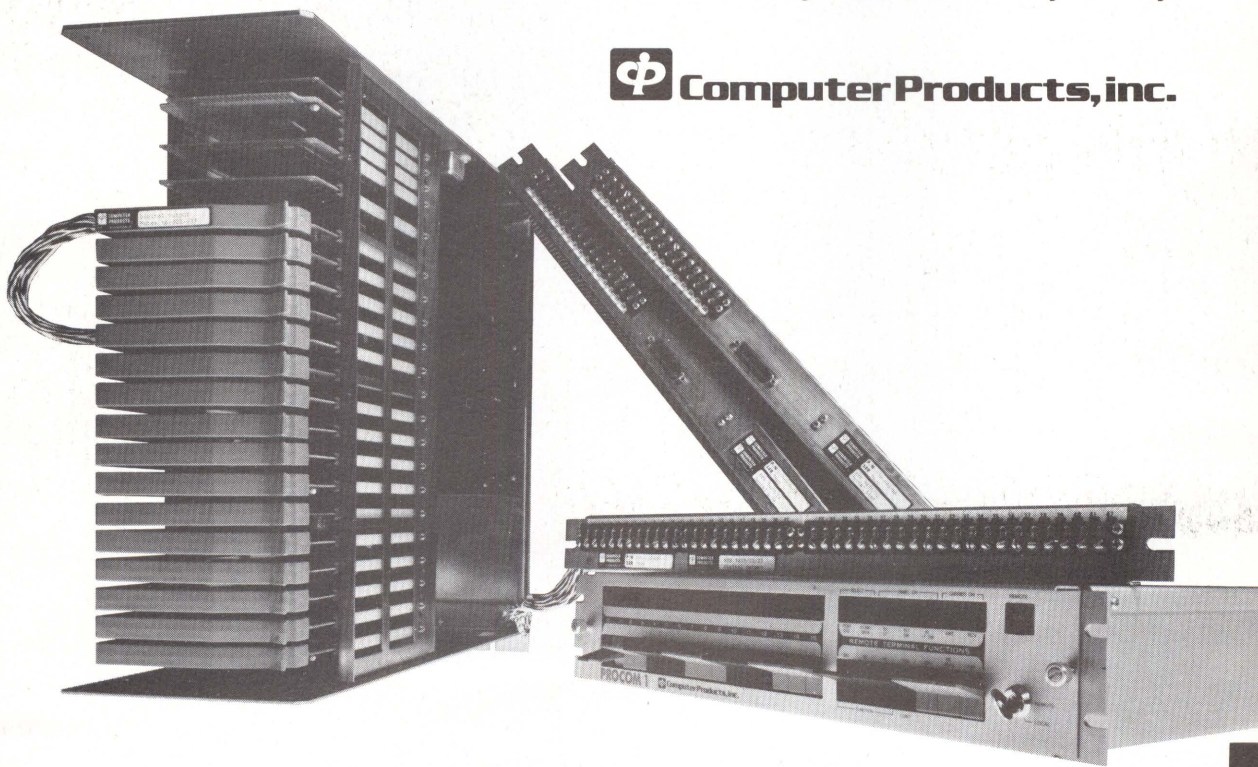
1400 NW 70 Street, Fort Lauderdale, Florida 33309 ● (305) 974-5500, TWX (510) 956-9895.

g3

Measurement & Control.

Unique Action Pins solve panel-production problems.

No more rupturing of plated-thru holes. Fewer rejects.
Wide commercial tolerances on plated-thru hole diameters.
Increased contact area. Higher production yields. Stable
electrical properties. Highest reliability. Low cost.
Now you can get them all with AMP ECONOMATE Panels
loaded with new Action Pins. Or in your panels with our
Action Pin Components.
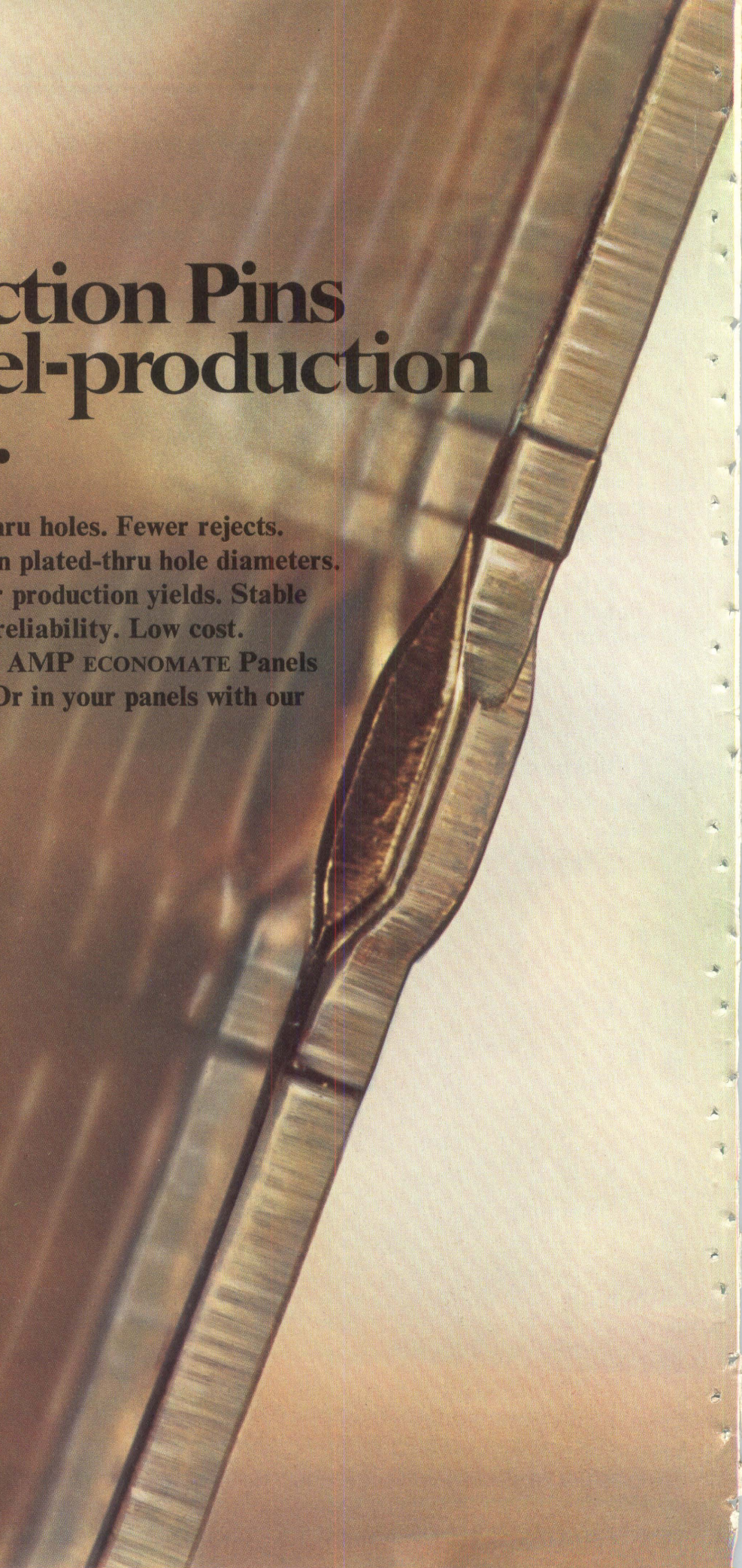
HOW ACTION PINS WORK. AMP Action Pins incorporate a spring section to give a higher degree of compliance than ever before possible. The diagonal measurement of the spring section —before insertion—is larger than the hole diameter (Fig.1). When the Action Pin is inserted, the two opposing spring members readily compress, and after insertion, exert a force sufficient to effect a gas-tight interface with the plated-thru hole walls (Fig. 2). Yet their rounded corners prevent rupture of the plated-thru hole. They come with a variety of configurations: card-edge contacts, .025² feed-to and feed-thru posts, and SEM (NAFI-style) two-piece receptacle-and-blade contacts. All are compatible with wrap-type terminations or I/O connections.
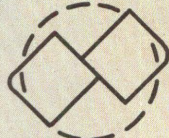
Fig. 1
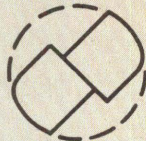
Fig. 2

AMP ECONOMATE panels are made to your specifications and consist of two elements: the pc board—either two-sided or multi-layer with plated-thru holes—and the AMP ECONOMATE Action Pin contacts.

ECONOMATE I card-edge contacts, and ECONOMATE II two-piece receptacle-and-blade, SEM (NAFI-style), contacts both feature snap-on housings for maximum maintainability of panels. Posted panels feature .025² feed-to and feed-thru posts for automatic, semi-automatic, or manual point-to-point wiring. All types hold costs to a minimum through AMP's high-speed automated assembly process.
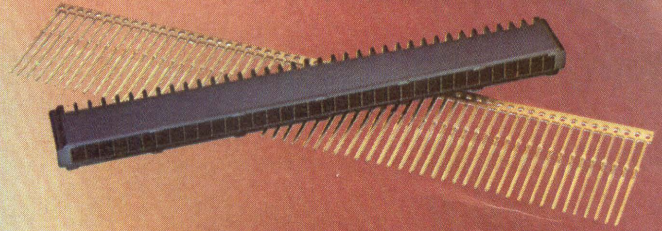
MAKE OR BUY. AMP can supply all your panel requirements. Or, you can make them yourself using our reliable Action Pin components. Contacts come in strip for high-speed, low-cost gang insertion at rates up to 10,000 an hour with our high-productivity assembly tools.

Action Pins solve the problems that bother you most. They won't broach, rupture, tear, distort or damage the plated-thru hole—giving you the ultimate in reliability.

When it comes to panels, AMP is where the action is. Get the whole story. Call (717) 564-0100 or write AMP Incorporated, Harrisburg, PA 17105.

AMP and ECONOMATE are trademarks of AMP Incorporated.

CIRCLE 24 ON INQUIRY CARD

AMP
INCORPORATED
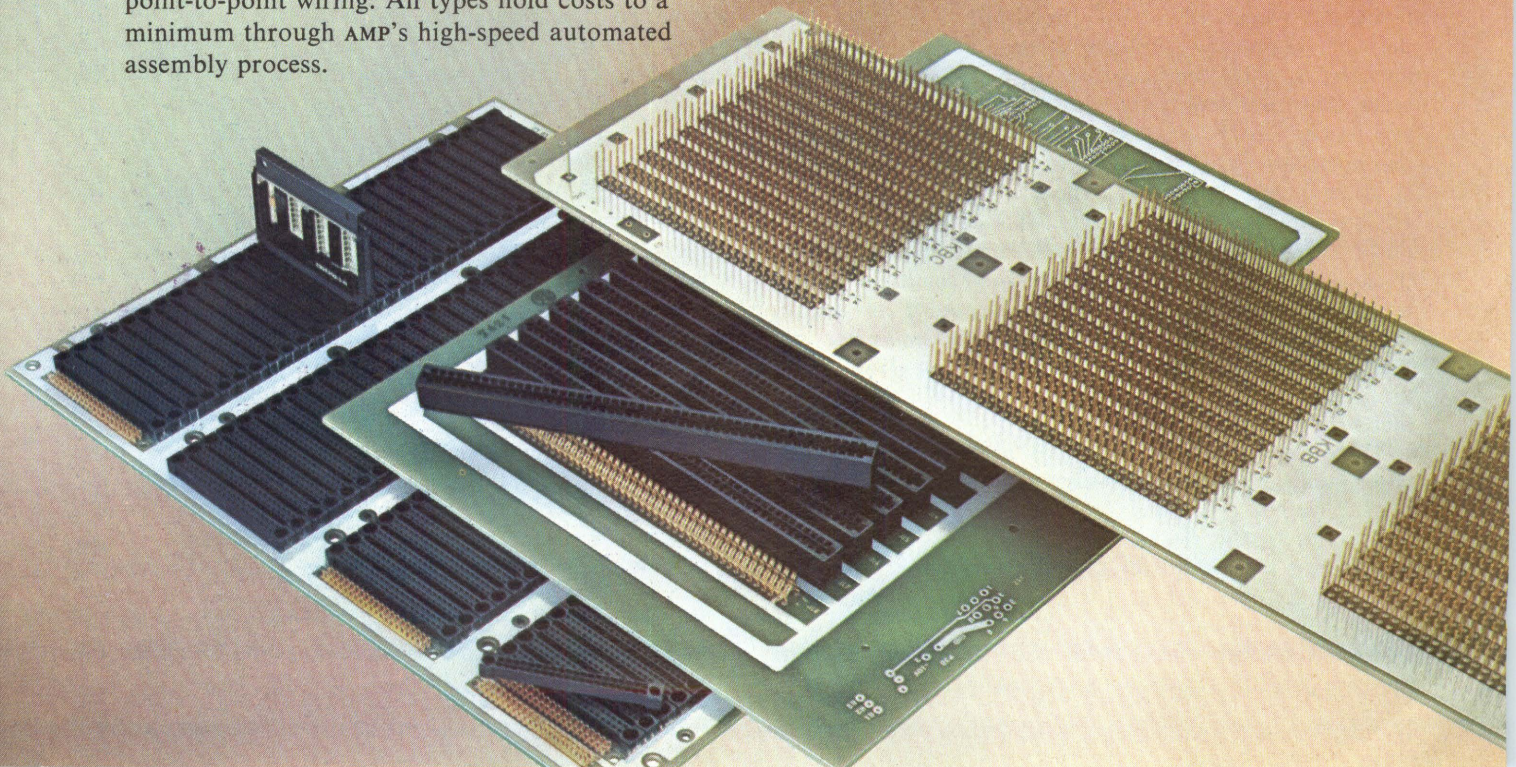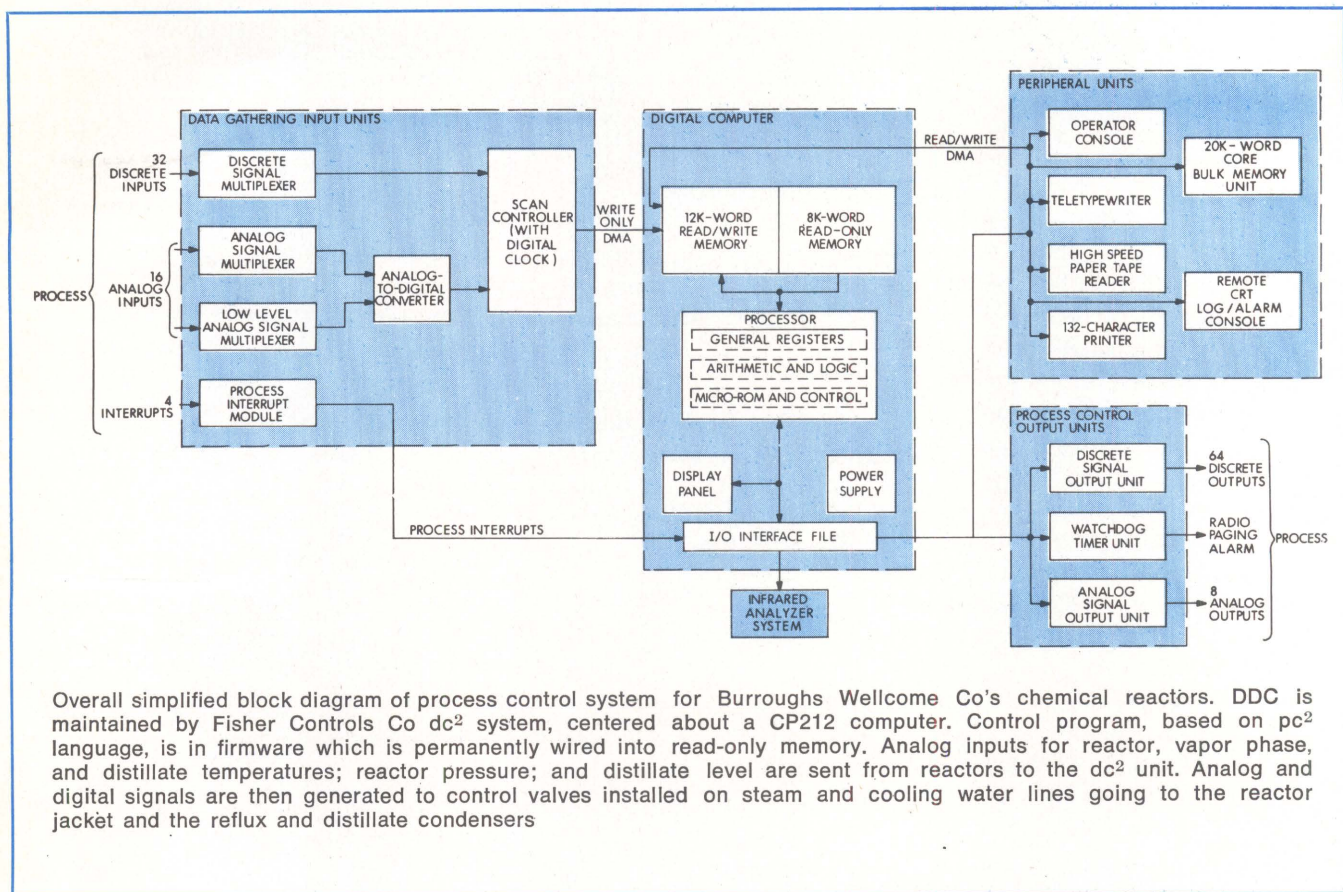
Overall simplified block diagram of process control system for Burroughs Wellcome Co's chemical reactors. DDC is maintained by Fisher Controls Co dc^2 system, centered about a CP212 computer. Control program, based on pc^2 language, is in firmware which is permanently wired into read-only memory. Analog inputs for reactor, vapor phase, and distillate temperatures; reactor pressure; and distillate level are sent from reactors to the dc^2 unit. Analog and digital signals are then generated to control valves installed on steam and cooling water lines going to the reactor jacket and the reflux and distillate condensers

tape reader to computer memory. This program may be one that has been used before, or a new one written from data obtained on small scale runs in lab or pilot plant equipment. Program preparation is such that the succession of operating steps remains essentially unchanged while the program is in use, but the variables that represent setpoints or on/off control valves can be changed at any time during the process—giving the operator great flexibility in modifying the process if at any time he detects a needed change.

Once the process is started, the computer continuously scans all input data and compares them with those called for by the application program. When any input variable reaches a critical point, or a prescribed time interval has elapsed, the computer responds by sending out the necessary control signal to keep process and program variable values properly matched.

Three computer output signals are analog types because they must give precise control for the three control valves regulating flow of steam or heat transfer liquids to the reactor and condensers. Other output signals are merely on/off digital types when 2-position switches are involved or valves are operated in either on or off modes. There are 32 on/off valves in the process lines associated with the 100-gallon reactor.

The computer is also programmed to initiate an emergency procedure if it is unable to bring actual variable values to their prescribed levels after a specified time period has elapsed. It automatically begins printing alarm messages and switches to an emergency shutdown program when this situation is reached, controlling valves, switches, and instruments to the proper settings, in the proper order, to achieve safe shutdown of the process.

If a process malfunction alarm occurs during the day, the process operator can either change the necessary process variables in the program or take over manual control, following written procedures. If the computer were to malfunction, some of the control functions would be shifted to a backup analog system, while others would be shifted to straight manual control. Dr Cipau says, however, that in over a year's operation, use of the backup analog system and/or manual control has not been necessary, except in cases of power failure.

A system alarm feature involves computer control through the watchdog timer of a radio paging system. If trouble occurs during the night or when operating personnel are not on the immediate scene, a "beep" from a small receiver carried by the operator (up to eight miles away) tells him the computer alarm has

been activated for whatever parameter(s) the program has been set up to monitor. The amount of information which the computer can send out by radio depends on the complexity of the coding system set up in the program for this purpose. This paging system is also used during regular shifts to alert the operator when a manual operation, such as adding something to the mix, must be carried out. When the operator performs the operation, he notifies the computer through a panel control, and the computer reassumes control.

Some of the reactions carried out in the 100-gallon reactor involve toxic gases that could endanger operating personnel if concentration levels become too high. An infrared gas analyzer now delivers a 1- to 5-V analog signal to the computer that covers the concentration ranges of interest (zero to extremely hazardous). Air in the vicinity of the reactor is continually sampled and passed through the infrared instrument which is set at one of the major absorption peaks of the toxic material. If the concentration of toxic gas reaches the unsafe limit, an alarm sounds. The whole system can be shifted into automatic shutdown if the level reaches a prescribed value.

Computer System

Processing and data storage section of the system's digital control center is a CP212 computer with 8000 words of read-only memory (ROM) and 12,000 words of read/write (R/W) memory. Both memories are random-access core, with 1-μs cycle time. Word length is 16 bits.

pc^2 firmware handles all input/output (I/O) operations, including process interrupts and data transfers to peripheral units. An average pc^2 statement, when compiled, generates 10 machine instructions from among a repertoire of 113 provided by micro-ROM (with 250-ns cycle time). The operator uses common English words and standard algebraic conventions to instruct the computer to perform a control task.

If line power fails or primary power falls below minimum input voltage, the computer detects the condition within one cycle and maintains dc power to the processor and memory for 1 ms. This is sufficient to allow completion of the current instruction being executed, storage of the contents of registers in protected memory, and protection of memory content. Auto restart hardware and support software automatically restart the processor and transfer program control to the pc^2 program when power is restored.

The computer is a 2's complement, binary, parallel machine with hardware multiply/divide for fixed- and floating-point instructions. It contains 16 general-purpose, 16-bit hardware registers, all used as accumulators (15 may be used for indexing); 8 floating-point, 32-bit memory registers; and 16 hardware registers for specific processor operations.

I/O transfer rates are up to 2.67 megabits/s data out or in, and up to 16 megabits/s direct memory access (DMA) (1 million, 16-bit words). An interrupt

FREE MICRO-PROCESSOR!

The next time you buy a microprocessor, you don't have to sign away your freedom of choice.

The AMI S6800 family is totally unbundled. You can order any part of it with no strings attached.

You're free to take just the MPU and hook it up with somebody else's peripherals. Or you may like the speed and density of our 8K ROM and the organization of our 128 X 8 RAM. If that's the case, you can use our memories with another company's microprocessor. The same goes for our communication and peripheral interface chips, Modem, and 16 or 22 pin 4K RAM.

For software support, you're free to use AMI's new relocating macroassembler, linking loader and simulator —all available on a major time-sharing service. You don't even have to buy the processor to get this support.

So the AMI S6800 doesn't make you a slave to us. It's even second sourced by Motorola, which gives you more independence and keeps us on our toes.

But think about this: our S6800 is the fastest, most cost-effective microprocessor family in the world. And the easiest to get along with, because the whole system goes together

without any TTL. So a funny thing is happening. Although we don't insist on bundling, many of our customers do.

Whether you want the whole bundle or just part of it, feel free to call our sales offices for brochures and information.

SALES OFFICES:
Manhattan Beach CA, (213) 379-2452 • Mountain View CA, (415) 969-0610 • Altamonte Springs FL, (305) 830-8889 • Elk Grove Village IL, (312) 437-6496 • Norwood MA, (617) 762-0726 • Livonia MI, (313) 478-9339 • Minneapolis MN, (612) 546-3354 • Monsey NY, (914) 352-5333 • Cleveland OH, (216) 292-6850 • Ambler PA, (215) 643-0217 • Richardson TX, (214) 231-5721 •

American Microsystems Inc., 3800 Homestead Road, Santa Clara CA 95051. (408) 246-0330.

it's standard at AMI

AMERICAN MICROSYSTEMS, INC.
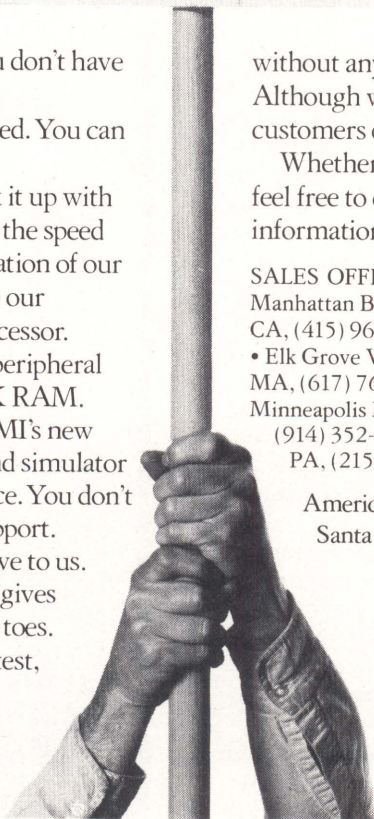
capability detects internal machine malfunctions and recognizes up to 256 distinct external interrupt sources.

Economic and Functional Aspects

Dr Cipau summed up overall system performance in the following comments and conclusions, based on data from a full year of online use.

There has been a 20% savings in process time. In a manual operation there is a lag between the point in time when a particular step or action is due and the point when it is actually performed. For a manually operated, multistep process these lags can be compounded. Also, faster heating/cooling is achieved with computer control.

Labor/kg of product was reduced considerably. Step sequences are automatic; the only labor required is during charging and discharging operations. It is impractical to automate these operations in a pilot plant reactor because of the small size of the equipment involved and because the physical forms of the reactants vary greatly from batch to batch (eg, liquids, powders, flakes).

Computer-controlled pilot plant processes are highly reproducible. Uniform yields and uniform products significantly reduce quality control costs.

The computer gives more control flexibility. Unlike conventional control, several different input parameters can be programmed to activate a given final control element. For example, steam input control in the reactor jacket can be based on several input parameters because control elements are wired to the transmitter through the computer and not directly in a hardwired loop.

Before computer control was used, it was necessary to correlate data from different recording charts in order to assemble process data (eg, times, temperatures, pressures); this was a tedious and inaccurate process. With computer control, data are printed on the teletypewriter and correlated with time, resulting in accurate record-keeping and rapid process analyses.

Overall safety of operations has increased. As many alarm systems as desired can be activated by any critical process parameter, and alarm trigger levels can be changed at any time. The process-interrupt capability eliminates possibilities of wrong action in moments of panic.
Circle 160 on Inquiry Card

Sophisticated System
Tests Gas Content of Vehicle's Exhaust

Computer-controlled systems that are claimed to be the most sophisticated ever built for automotive vehicle emission testing are now in use at three West Coast automotive assembly plants. EPA type 1975-76 engine emission audit test system, designed and built by Ethyl Corp's Air Monitoring Inc Div, Royal Oak, Mich, is

Let's get the facts straight on IC packaging panels.

The IC packaging panel, or "Augat board," has become so widely accepted, you'd think Augat would be happy.

But frankly, we're concerned.

People have gotten so used to IC panels that they may have lost sight of the reason for buying panels in the first place: flexibility in design, production and service. With the result that they may not be getting all the benefits panels can provide.

We'd like to correct this situation by reviewing exactly what's at stake in your choice of a panel supplier.

GETTING THE RIGHT PANEL.

People often select a panel from a limited catalog without realizing the wide selection of stock panels available.

When in fact, they can get exactly what they need right off the shelves of Augat distributors all over the world.

With the largest product line anywhere, we're sure to have a standard board that fits virtually all your development and production needs—including ECL and Schottky.

For really special requirements, though, you should probably consider a custom-designed panel. If you're dealing with an experienced engineering staff like Augat's, it's surprisingly easy. And it won't cost you any premium—it might even save you money.
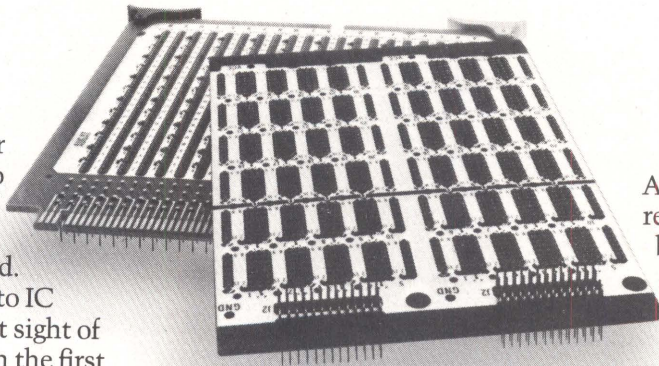
Whatever your requirements, you shouldn't settle for an approximation. Because you don't have to.

HOW GOOD IS GOOD ENOUGH?

The payoff for getting the right panel is faultless performance. No surprises in product development, production, or field service.

It's the reason for Augat's no-compromise approach to quality control. And it's why Augat uses the best precision-machining technology in the world, rather than conventional stamping methods, to produce the contact assemblies that are the heart of Augat panels.

The result speaks for itself. The elimination of these common contact pitfalls:
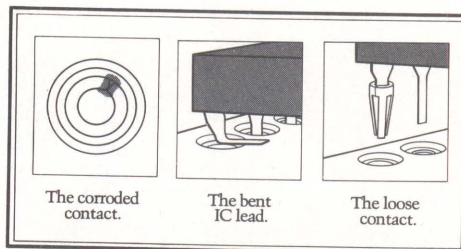
| The corroded contact. | The bent IC lead. | The loose contact. |

When others succeed in duplicating Augat's machining technology, the result will be better panels for everybody. But until then, there's only one place in the world to get this degree of fail-safe protection: Augat.

DELIVERY YOU CAN COUNT ON.

In 1974 Augat completed a multi-million-dollar program to automate production and bring the manufacture of IC panels under 100% in-house control.

Result: The fastest turnaround the industry's ever seen.

Most standard panels are on the shelf. But if the one you want isn't, you can still get it in no more than 2 weeks. And our custom panels are being turned out in volume to meet the most stringent delivery standards in the industry.

So next time you're selecting IC panels, consider all the facts. For full information, send for our new brochure. Or phone George P. Howland, Engineering Manager, at (617) 222-2202. Augat, Inc., 33 Perry Avenue, Attleboro, Massachusetts 02703.
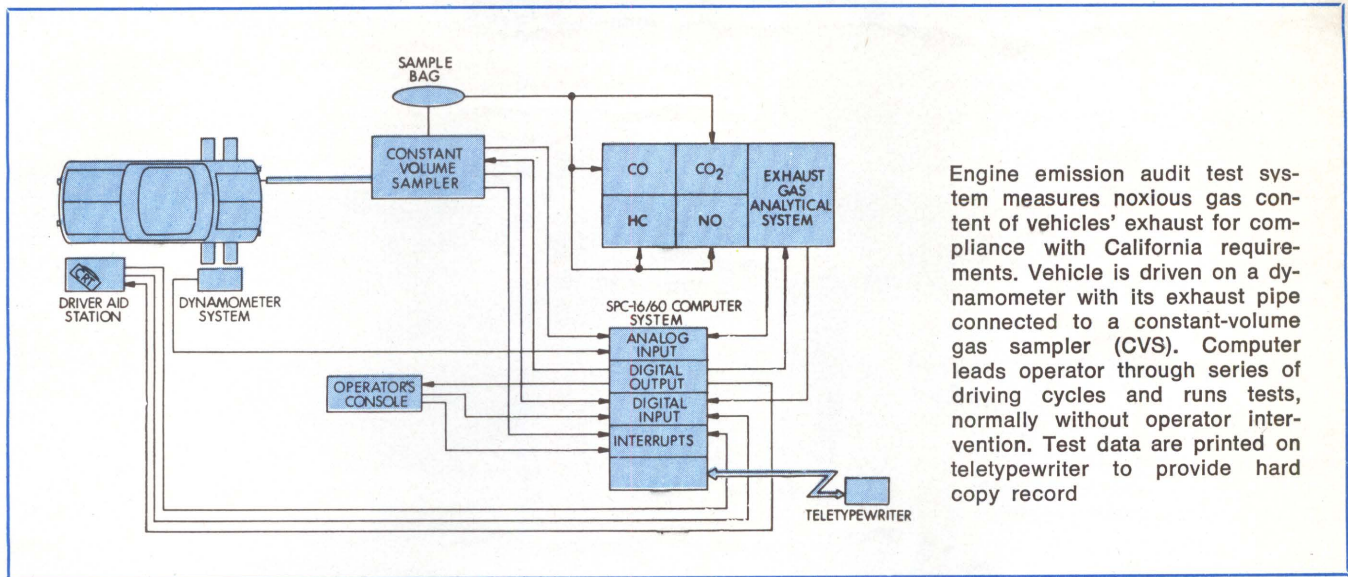
YOU ONLY GET IT ALL FROM AUGAT.

AUGAT®

Europe—Augat N.V., Boulevard A. Reyers, 103, 1040 Brussels, Belgium, Tel. (02) 7369399.
Japan—Kyokuto Boeki Kaisha Ltd., New Otemachi Bldg., 2-1, 2-Chome Otemachi, Chiyoda-Ku, Tokyo 100-91, Japan, Tel. (03) 244-3788.
Canada—A.C. Simmonds & Sons Ltd., 285 Yorkland Blvd., Willowdale, Ont. M2J1S8, Tel. (416) 491-1010.

CIRCLE 30 ON INQUIRY CARD

Engine emission audit test system measures noxious gas content of vehicles' exhaust for compliance with California requirements. Vehicle is driven on a dynamometer with its exhaust pipe connected to a constant-volume gas sampler (CVS). Computer leads operator through series of driving cycles and runs tests, normally without operator intervention. Test data are printed on teletypewriter to provide hard copy record

used by vehicle manufacturers to test compliance with California's 2% audit test requirements.

In a Federal compliance procedure which requires approximately one hour, including vehicle preparation, the system tests for carbon monoxide (CO), hydrocarbons (HC), carbon dioxide (CO_2), and oxides of nitrogen (NO). A constant-volume gas sampler (CVS), connected to the vehicle exhaust pipe, dilutes and preconditions the exhaust gas sample for analysis by an analytical exhaust gas console. Test sampling and data

DIGITAL CONTROL AND AUTOMATION SYSTEMS

acquisition are controlled by a General Automation SPC-16/60 computer which also monitors operation of a dynamometer on which the vehicle is driven. The vehicle driver is directed through a number of 20-s driving cycles by instructions displayed on a CRT in the driver aid station, with the vehicle speed superimposed on the cycle trace. A second CRT displays system status during the test. Hard copy test results are printed on a teletypewriter, which also provides additional operator communication.

Features of the computer (960-ns cycle time, 16K words of core memory) include real-time clock, power fail/auto restart, integer hardware multiply and divide, foreground/background register, and a ROM-IPL loader. Full system capability involves 16 analog input channels, 32 digital inputs and outputs, and 16 process interrupts.

A typical system has eight analog inputs to the computer: one for each of the four exhaust gases, and one each for vehicle speed, CVS blower inlet pressure, CVS blower outlet pressure, and CVS blower inlet temperature. There are 24 digital outputs from the computer: one each for filling three sets of gas sample bags, three for reading dilute sample bags, three for reading the background sample bags, one each for start and stop test signals, two for automatic test signal analyzer calibration, seven for operator status lights, and four for nitrous oxide analyzer converter efficiency.

In addition, there are 24 digital inputs to the computer: 12 for operator communication; one each for test start vehicle crank, test stop vehicle "dieseling," CVS status, and analytical system status; and eight for analyzer range status. Seven digital process interrupts are fed to the computer: one each for read status from the operator's console, abort and hold test, start data acquisition, CVS blower revolution counter, and start and hold test at driver aid station.
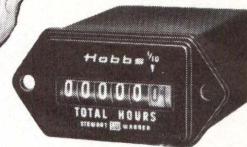
The system operating procedure is:
—operator selects tests and options on operator console
—operator presses read status buttons, initiating test preparation sequence
—depending on type of test, computer may request additional information to be input via teletypewriter
—operator adds data via teletypewriter in conversational mode
—computer interrogates hardware status and performs automatic system calibration
—computer tells operator to initiate test (through either signal lights or teletypewriter
—depending on test, computer waits for process interrupt signal
—computer begins and runs test sequences, normally without operator intervention
—during test, data are acquired, converted to engineering units, accumulated for specific test modes, and printed on teletypewriter by commands from the computer
—at end of test, a summary report is generated on the teletypewriter

Circle 161 on Inquiry Card

Power Generating Plants To Be Placed Under Digital Control

Contracts have been awarded to Leeds & Northrup Co, North Wales, Pa for two separate projects involving generation of power. One project is for three computer data handling, control, and monitoring systems to be installed between mid-1976 and late 1977 on an 850-MW expansion of the Cholla Generating Station near Joseph City, Ariz. Each of three pulverized coal burning, drum-type generating units will be maintained by a system designed for integrated boiler/turbine control with direct energy balance techniques. Loops under control primarily will include fuel, air, feedwater, and steam temperature. In addition, each of three LN5400 digital process control systems will handle data monitoring and display for 1200 analog and digital points. Each system will include three central processors with redundant power supplies, 40K words of main memory for each processor, auxiliary drum memories, teletypewriters, loggers, magnetic tape memory, card readers, operator's console, and nine CRTs.

The second project involves computer monitoring and control equipment for two 550-MW, coal-fired boilers for the Lower Colorado River Authority, headquartered in Austin, Tex. A dual LN5400 digital process control system will monitor and display plant variables for both units. The system will contain two central processors with 40K words main memory, two auxiliary memories, seven CRTs, teletypewriters, process interfacing subsystems, loggers, and high speed paper-tape readers and punches. Installation of the system will begin in late 1976.

Plastic/Rubber Industry Process Measurement/Control System

Depending on the configuration, five or more vinyl or rubber calender lines can be controlled by multiplexing from a single 3000 series system. Strategy can range from simple operator control with measurement only, to complete computer closed-loop control. Designed by Nucleonic Data Systems, Inc, Irvine, Calif specifically for the plastic and rubber industry, the systems are claimed to offer up to 30% savings in raw material and to improve quality control.

In addition to the advantages of digital control, advanced sensor technology is said to provide the potential for major system improvements. An x-ray fluorescence sensor with isotope source can be used for such applications as measuring zinc content of rubber (to 0.1%), measuring depth and cord separation in steel cord directly without the need for interpretation, and measuring additives such as antimony trioxide and titanium dioxide in plastics directly.

ISA-75 Conference and Exhibit

October 6-9
Mecca Hall
Milwaukee, Wisconsin

Supporting the concept of practical applications in industry, the Instrumentation Society of America Conference and Exhibit, under the direction of General Chairman Fred Brengel, Johnson Controls Inc, will examine "The Real World of Instrumentation in Industry." Included on the program, prepared with Robert Middleton, Monsanto Co, as chairman, are technical paper sessions, workshops, clinics, and panels—all at Mecca Hall. In addition, 2-day Short Courses, to be given at nearby Milwaukee Technical School, will offer practicing engineers and technicians an opportunity to update their fundamental knowledge and upgrade their skills. Also of interest are five Symposia to be conducted at the Conference, and presentations of applications papers by manufacturers.

Only sessions and courses of particular interest to *Computer Design* readers are outlined in the following pages. Information is limited to that available at press time.

Special Activities

Events of special interest will include the Keynote Address presented by John H. Stender, Assistant Secretary of Labor for Occupational Safety and Health, which will formally open the Conference on Monday morning. In addition, a Distinguished Lecture Series will consist of one presentation each morning, prior to Conference sessions. Distinguished speakers will include Dr R. L. Bowman, Chief of the Laboratory of Technical Development, National Heart and Lung Institute, speaking on biomedical instrumentation (Tuesday); H. J. C. Kouts, Director of the Office of Nuclear Regulatory Research, U. S. Nuclear Regulatory Commission, covering nuclear safety research (Wednesday); and J. A. Duffie, Director, Solar Energy Laboratory, College of Engineering, University of Wisconsin—Medicine, discussing solar heating and cooling (Thursday).

The ISA President's Reception at the Marc Plaza Hotel, Sunday, October 5 from 4:30 to 6 pm, will lead off the social activities planned for Conference Week, providing an opportunity for ISA members to meet Society officers. This years' recipients of awards for special achievements in the field of instrumentation and automatic control will be honored at the ISA-75 Honors and Awards Luncheon on Wednesday at 12:30 pm in the Marc Plaza Hotel. (Tickets are $10 each.) A luncheon at the Marc Plaza, preceding the Council of Society Delegates Meeting on Thursday at 12:30 pm, will be open to all delegates, alternates, and ISA members. (Tickets are $7 each.) Wednesday evening at 6 pm, attendees and guests are invited to experience Milwaukee's heritage at the ISA German Gemutlichkeit, where they will be fed and entertained by a German band and dancers. (Tickets are $10/person and include bus transportation.)

Registration and Exhibits

Fees for Conference and Exhibit registration are: 4-days, advanced—$30 members ($40 nonmembers), 4-days, at the door—$35 and $45, and 1-day—$10 and $15. Short courses carry a $150 registration fee for nonmembers, $125 for members. Conference papers, including manufacturers application papers, will be available as individual preprints during the Conference, and as bound proceedings later.

Exhibit hours are Monday 12 noon to 6 pm, Tuesday 9 am to 12 noon and 4:30 to 7:30 pm, Wednesday 12 noon to 6 pm, and Thursday 9 am to 5 pm.

Short Courses

Monday and Tuesday

Minicomputer Systems, Programming, and Applications

Course will familiarize attendees with basic computer hardware and options, basics of programming languages, operating systems, and other software routines.

Acceptance Testing of Industrial Process Computers

A methodology of digital computer acceptance testing that lies within the framework of ISA Recommended Practice RP55.1 will be presented during this course.

MEET YOUR TOUGHEST DESIGN CRITERIA
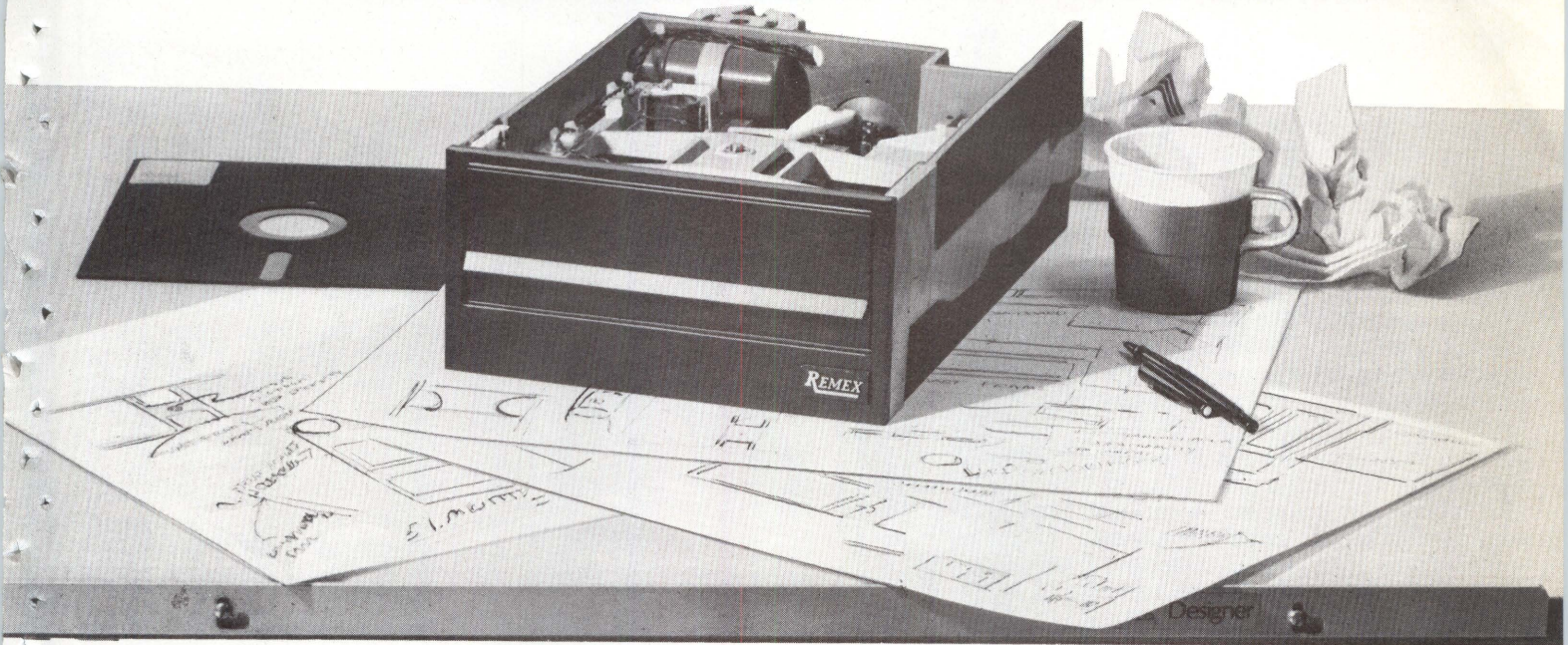
MEET THE REMEX FLOPPY DISK DRIVE

No compromise required. There is one floppy disk drive with the design flexibility to meet all your systems requirements. The REMEX RFD7400.

IBM compatibility? Remex has it. Complete media and data interchange with 3740 Series systems. Guaranteed by Remex because the RFD7400 meets every one of the 3740 floppy disk specifications. We test for them!

Standard media? The RFD7400 provides a unique write enable option that gives fool proof operation on any standard IBM media. No need to pay a premium for specially prepared media. Select from any available source.

Fail safe design features? Our floppy disk drive has Track "00" and track "76" sensing. A unique feature which prevents machine damage and loss of data at *both* ends of diskette media.

Long life? How about 15,000 hours? The RFD7400 construction provides years of reliable operation with only 12 grams of head pressure, utilizing a tungsten-carbide ball bearing stylus. The result; 50% longer life than competitive units.

Extra capacity? You bet! Up to 3.2 megabits with our special hard sectoring and data recording options. And we use standard media too.

Random average access time? The RFD7400 is more than 30% faster than competition. Think of what this can do for your throughput.

Special configurations? The RFD-7400 can be custom designed to fit almost any application. Test us by sending your design headache to our Applications Engineering Manager. Better still, call us direct and order your evaluation unit for immediate delivery. Chances are that our standard unit already meets your requirements.

Write, Remex, a Unit of Ex-Cell-O Corporation, 1733 Alton Street, P.O. Box 11926, Santa Ana, California 92711 or call (714) 557-6860.

We work with you.

REMEX

XLO® | Peripheral Products

Ex-Cell-O Corporation

First came Remex flexible disk drives.

Now, the whole, compact, IBM-compatible, data-packin' system

The new Remex RFS7400 flexible disk system offers all of the high-speed, high-capacity attributes inherent in this technique, plus many outstanding performance advantages unique to the Remex design.

Naturally, the Remex systems are IBM 3740 compatible. We test each system to prove it. They read diskettes prepared in a 3740 system, or write and initialize diskettes that can be read on a 3740 system. The RFS7400 also offers a unique write enable option that gives foolproof operation without modification on any standard IBM compatible media.

Among the many other features, the RFS7400's fail-safe drive design offers Tracks "00" and "76" sensing to prevent machine damage and loss of data at both ends of the media. It offers approximately 50% longer life than competitive drives. And average random access time is more than 30% faster.

The system includes formatter electronics, with up to four separate drives, and power supply. Diagnostic software, I/O drivers and computer compatible interface controllers are available as options for PDP-11 and NOVA minicomputers. Like all other Remex computer interface packages, we guarantee system compatibility.

The Remex flexible disk system offers:
- Multiple drive read-write/seek operation
- File Unsafe
- Write protect
- High data reliability (Read Error Rate: 1×10^9 bits Read/Error, nominal; 1×10^{12} bits Read/Hard Error, nominal
- Storage capacity: 246×10^3 bytes per diskette
- Transfer rate: 31.25×10^3 bytes (8-bit) per second
- Available for 115 VRMS, 60Hz, 230 VRMS, 50Hz.
- DMA and Programmed I/O interface controller (option)

ASK FOR AN EVALUATION UNIT: Write Remex, Ex-Cell-O Corporation, 1733 Alton St., P.O. Box 11926, Santa Ana, Cal. 92711. Or call:

BOSTON: (617) 784-8380 • **NEW YORK:** (212) 947-0379
ORLANDO: (305) 894-4401 • **CHICAGO:** (312) 359-1310
DALLAS: (214) 661-0300 • **PHOENIX:** (602) 946-4215
LOS ANGELES: (714) 557-6860 (Orange County)

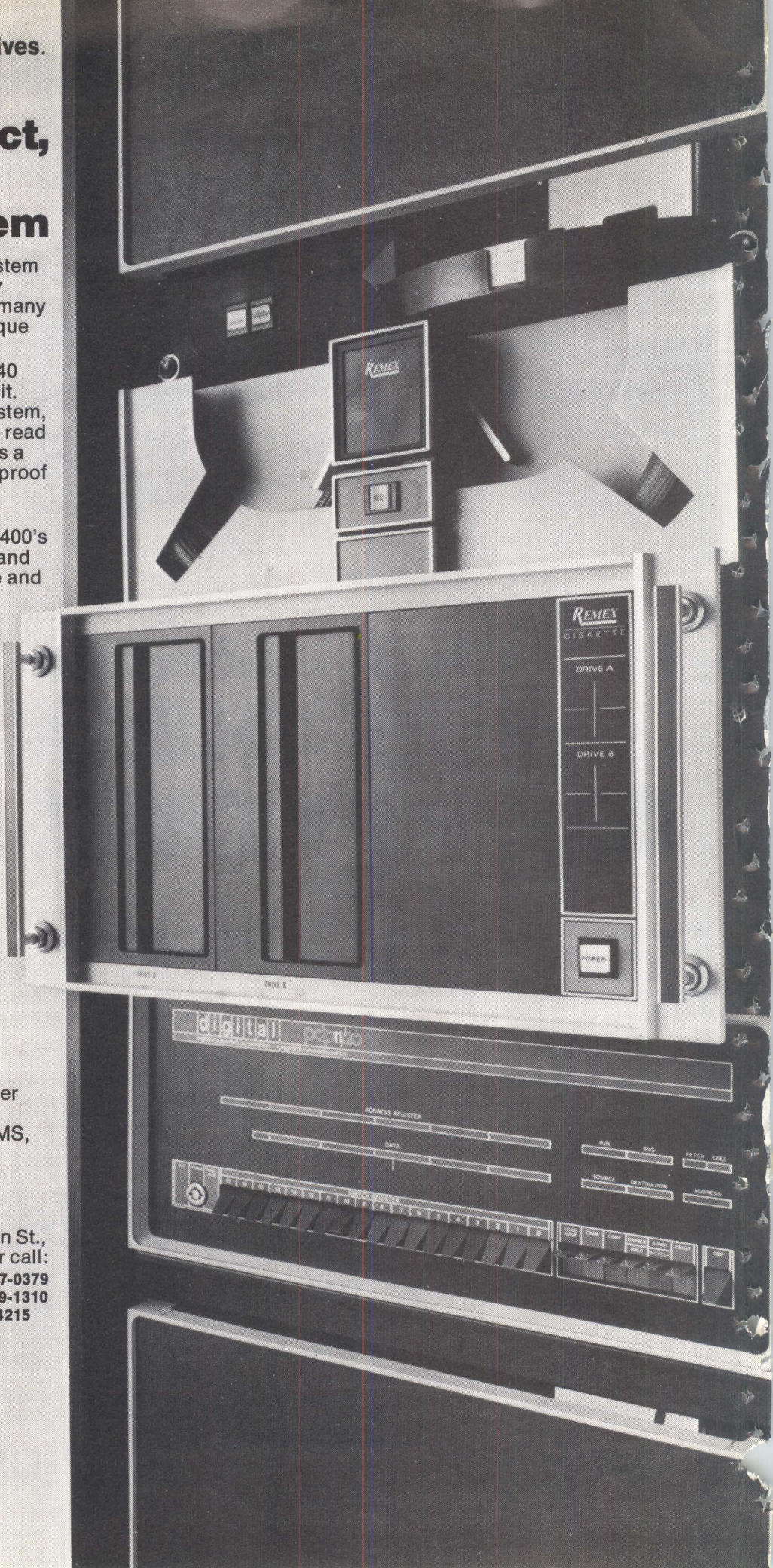## We work with you

REMEX

XLO Peripheral Products

Ex-Cell-O Corporation
CIRCLE 40 ON INQUIRY CARD

Wednesday and Thursday

Computer Process Control

Attendees will be familiarized with several approaches by which the digital computer can be used to achieve control performance exceeding that of conventional control systems and, thus, increase the computer's dollar payout.

Microcomputer and Microprocessor Applications for Process Control

Course covers evolution of microcomputers and microprocessors, hardware, software, and applications.

Software Engineering: Design and Management for Industrial Computer Programming

Students will be introduced to methods for designing and managing the design of industrial automation systems and software for such systems.

Technical Program Excerpts

Monday

| Session 2 | 2:30-5 pm | W3 |

Process Management and Control— Today and Tomorrow

Chairman: R. Ryan, Foxboro Co

"Achieving Today's Promises for Process Control," C. J. Mroz, Foxboro Co

"Future Applications for Computers for Process Control," D. Teale, Fisher Controls Co

"Microprocessor vs Programmable Controller," F. L. Slane, Industrial Solid-State Control

| Session 3 | 2:30-5 pm | W2 |

Clinic: Camac Modular Interface System

Chairman: D. Zobrist, ALCOA

The modular computer interfacing standards and their applications will be discussed. An operating system will be on hand. D. Little, Standard Engineering Corp; T. Radway, Joray Corp; and J. Davis of Lawrence Livermore Laboratories will participate in the clinic.

Tuesday

| Session 13 | 10 am-12:30 pm | E5 |

New Breakthroughs in Digital Systems

Chairman: V. Diehl, Hewlett-Packard Co

"Networking of Computers in Today's Industry," T. E. Smith, Modular Computer Systems

"Potential Impact of LSI on Process Control Systems," H. P. Zinschlag, J. A. Conover, and W. E. Long, Monsanto

"A New Approach to Remote Process I/O—Software Transparent Remote I/O Subsystem," L. Avery and S. Moro, Digital Equipment Corp

"Process Control is Not EDP," J. Copeland, Copeland & Roland Assoc

"Distributed System New Approach to Process Control," L. M. Cartright and J. C. Mayberry, Inland Steel Co

| Session 14 | 10 am-5 pm | E10 |

Clinic: Programmable Logic Controllers

Chairman: A. I. Schwartz, Westinghouse-Bettis

All-day clinic will consider hows, whys, and wherefores of pro-

grammable controllers (cousins to the minicomputer), including how they work, how to apply them, and hands-on use of equipment by all attendees. Simple example applications will be programmed and tested. Instructors are from Allen-Bradley Co. (Clinic will be repeated on Wednesday.)

Session 15 10 am-5 pm W10

Clinic: How to Program Process Control Computers

Chairman: A. C. Lumb, Procter & Gamble

All-day clinic will give hands-on experience in writing and testing a digital computer program for online control of a real industrial process. After a brief introduction, participants will work in 6-man teams to design and implement a control strategy involving interactive pressure, temperature, flow, and level loops. Hands-on computer time will be scheduled for each group during the early afternoon. Luncheon is included. Instructors and equipment are from Fisher Controls Co. (Clinic will be repeated Wednesday.)

Session 18 10 am-12:30 pm W8

Programmable Control Systems

Chairman: S. C. Hu, Cleveland State University

"Programmable Sequence Controller in Multiplex Configuration," O. J. Struger and W. W. Searcy, Allen-Bradley Co

"An Industrial Control Processor for Contouring Numerical Control Applications," E. Dummermuth and R. E. Jerva, Allen-Bradley Co

"Distributed Intelligence Microcomputer Systems," L. H. Anderson, Warner & Swasey Co

Session 24 2:30-5 pm E2

Panel: Microcomputers and Industrial Applications—Their Impact on Instrumentation and Control

Chairman: A. C. Lumb, Proctor & Gamble Co

Each panelist will give a brief "position paper" on the topic in general. Following this there will be interactive discussion between the panel and audience. Panelists are: M. B. Adams, Stanford Research Institute; L. H. Anderson, Comstar Div, Warner & Swasey Co; D. Arndt, Process Systems, Inc; W. A. Coelho, Procter & Gamble Co; and J. E. Heaton, Logicon, Inc

Wednesday

Session 26 10 am-12:30 pm E5

Computer Applications in the Power Industry

Chairmen: J. Adams, Bailey Meter, and H. Long, General Atomic Co

"Power Plant DDC—Where Has It Been and Where Is It Going?" D. R. Clark and R. S. Bilski, Bailey Meter Co

"High Availability Computer System Replaces Conventional Annunciator System for Power Plant Monitoring," C. L. Longenecker, Jr, Gilbert Associates, Inc; and J. M. Dahlquist, Jr, Baltimore Gas & Electric

"The Plant Computer as an Operating Tool," D. E. Bear, General Atomic Co

"On-Line Computer NSS—Performance Calculations on Oconee Unit 1," W. E. Gabler and R. E. Clark, Babcock and Wilcox Co

Session 27 10 am-5 pm E10

Clinic: Programmable Logic Controllers

Chairman: A. I. Schwartz, Westinghouse-Bettis

(Repeat of Session 14)

Session 28 10 am-5 pm W10

Clinic: How to Program Process Control Computers

Chairman: A. C. Lumb, Procter & Gamble

(Repeat of Session 15)

Session 29 10 am-5 pm E3

Clinic: Minicomputer Systems

Chairman: A. I. Schwartz, Westinghouse-Bettis

All-day clinic will introduce attendees to minicomputer hardware and programming and provide some insight into systems design and implementation, cost, and justification considerations, industrial applications, and future trends. An actual operating system will provide an opportunity for hands-on exposure. Instructors and equipment are from Hewlett-Packard Co. (Clinic will be repeated on Thursday.)

Session 33 2:30-5 pm E5

Computerized Systems for Energy Conservation

Chairman: R. C. Risberg, Johnson Controls Inc

"Computer Based Automation's Role in Good Building Management," F. B. Hall, III and G. S. Jones, Robertshaw Controls Co

"Control of a Black Liquor Recovery Boiler," C. W. Warren, R. R. Johnson, and L. N. Harris, Fisher Controls Co

"Application of Computers for Energy Conservation in Buildings," K. Sinnamohideen, Johnson Controls Inc

"Minimizing Cooling Energy Through the Consideration of Outdoor Air Enthalpy," D. E. Miller, Johnson Controls Inc

Thursday

Session 39 10 am-12:30 pm E5

Applications of Digital Computers in the Process Industry

Chairman: R. Bothne, EMC Control

"On-Line Computer Control of Gasoline Blending," G. J. Gustafson, Honeywell Inc, and K. Komatsu, Yamatake-Honeywell

"A Practical Approach to the Selection of Remote Interface Devices," M. A. Curran, Digital Systems Corp

"Economic Benefits from Centralized Control in Petroleum Refineries," C. Watson, Foxboro Co

"The Greatest Relay Ever Made," R. O. Dietz, Miller & Dietz Co

Session 40 10 am-5 pm E3

Clinic: Minicomputer Systems

(Repeat of Session 29)

Session 44 10 am-12:30 pm W8

Application Papers for the Food Industry

Chairman: N. Creswick, T. J. Lipton, Inc

"The Application of In-Line Digital Blending Systems, H. T. Day, Warner Jenkinson Co, and T. J. Hayes, Fischer & Porter Co

Data Handling and Computation Symposium

Monday 2:30-5 pm

Review of the State of the Art in Computer Application to the Process Industry

Tuesday
10 am-12:30 pm

Application of Digital Computers in Process Industries

2:30-5 pm

Application of Digital Computers in the Power Industry

Wednesday
10 am-12:30 pm

New Developments of Computer Applications in Nuclear Plants

2:30-5 pm

Computer Applications for Industry

Thursday
10 am-12:30 pm

New Breakthroughs in Digital Systems

Manufacturers Application Papers
Tuesday

Burr-Brown Research   3:15-3:45 pm   E4

"Remote Data Acquisition: Profits & Problems," C. R. Teeple

Datametrics   2:30-3 pm   W2

"The Programmable Controller's Approach to Implementing Logic Control," P. Carey

Allen-Bradley Co   2:30-3 pm   W4

"Programmable Controllers as Applied to Energy Management," R. H. Anderson

FX Systems   4-4:30 pm   W4

"Applications of a Small Programmable Controller, to the Monitoring of Toxic Gas," W. T. Crist and A. F. Clarke, Jr

Wednesday

Rosemount, Inc   11:30 am-12 noon   E2

"Tower Operators Command Digital Control," G. A. Pettit and D. Whiteford

Integrated Photomatrix Ltd   10:45-11:15 am   E4

"The Use of Solid-State Linescan Cameras as Noncontacting Dimension Monitors in Process Control Systems," G. R. Parsons

Industrial Solid-State Control   11:30 am-12 noon   E4

"Microprocessor vs Programmable Controller," F. L. Slane

ACCO Bristol   11:30 am-12 noon   E6

"Flexible Microprocessor Process Control," B. Allen

Allen-Bradley Co   10-10:30 am   W4

"Multiple System Control Using Remote I/O," B. P. Simon

Metra Instruments Inc   10-10:30 am   E4

"Systemetra: A Systems Approach to Programmable Acquisition and Display of Over 1000 Channels Without Computer Overkill," T. Diepenbrock

Reticon Corp   10-10:30 am   E11

"Solid-State Scanning Image Sensors Offer Reliability Advantages Over Photocells in Electrical Terminal Inspection System," J. P. Spurla   □

Tally's printer line is going places...

Tally's renowned 200 line per minute line printer for the long run is now backed up with 125, 300 and 400 lpm. There's more. The beginning of a line of serial printers. The Series 1000. First off the blocks is a 120 character per second, 132 column, high reliability data processing machine.

Now, with this fine family of printers, you can pick the

Model 2100
125 lines per minute
132 columns
7 x 8 comb matrix print
Multi-part forms to 14⅞"
Up to 8-channel VFU
Many parallel interfaces
1200 Baud communications

Model 2200
200 lines per minute
132 columns
5 x 7 comb matrix print
Multi-part forms to 14⅞"
Up to 8-channel VFU
Printer emulating interfaces
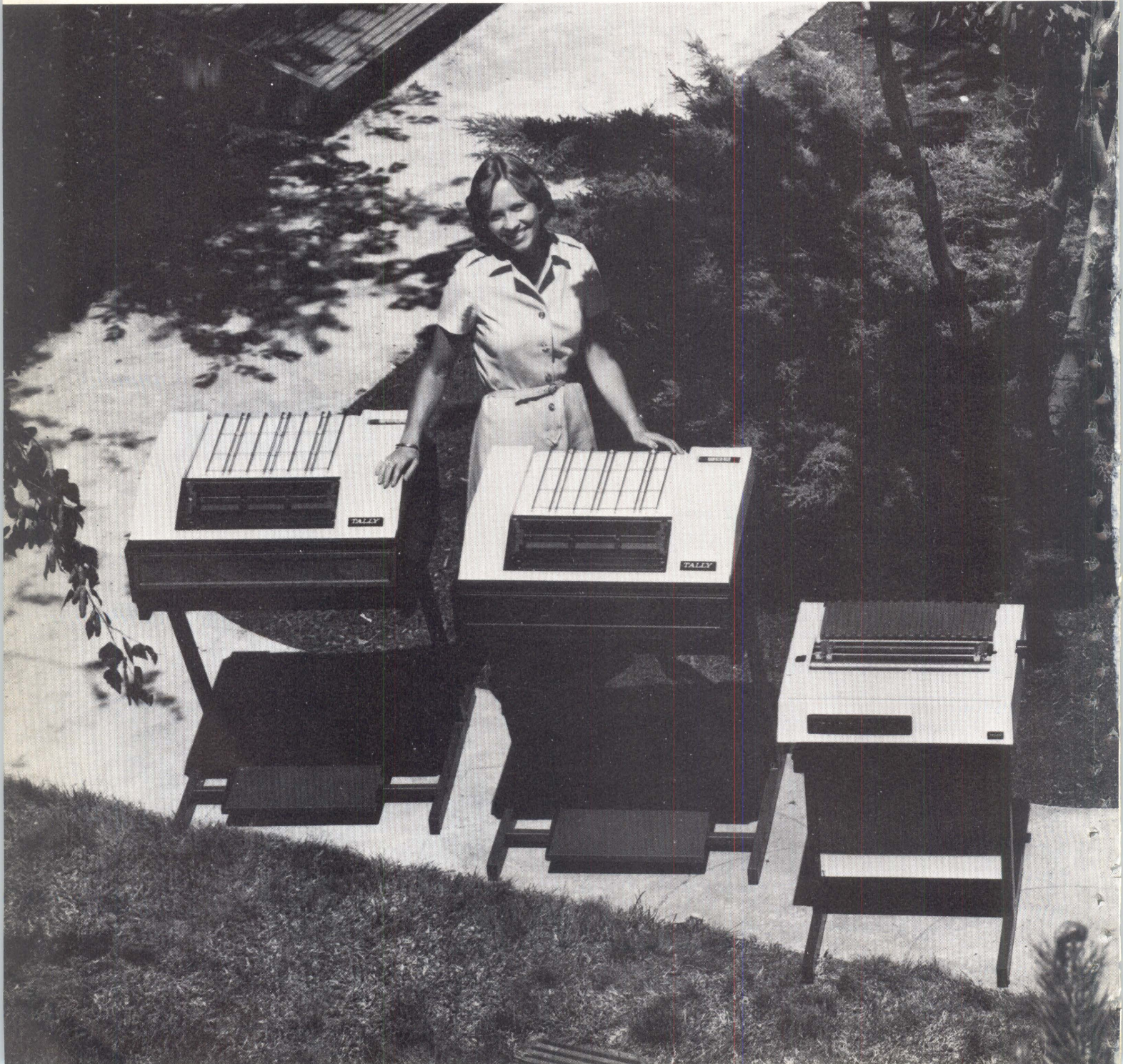Mini controllers

Model 1120
120 characters per second
132 columns
9 x 7 high fidelity print
Multi-part forms to 15"
2-channel VFU
Many parallel interfaces
Asynchronous communications

up to 400 lines per minute...down to 120 characters per second.

price/performance package that best suits your system. And be comfortable in knowing that Tally reliability won't let your customer down in the middle of a print run.

Talk to Tally today about these low cost, high performance printers. You'll enhance the value of your total system package. Tally Corporation, 8301 South 180th Street, Kent, Washington 98031. Phone (206) 251-5645.

Model 4300
300 lines per minute
132 columns
9 x 9 comb matrix print
Multi-part forms to 19"
Up to 12-channel VFU
20 ips slew
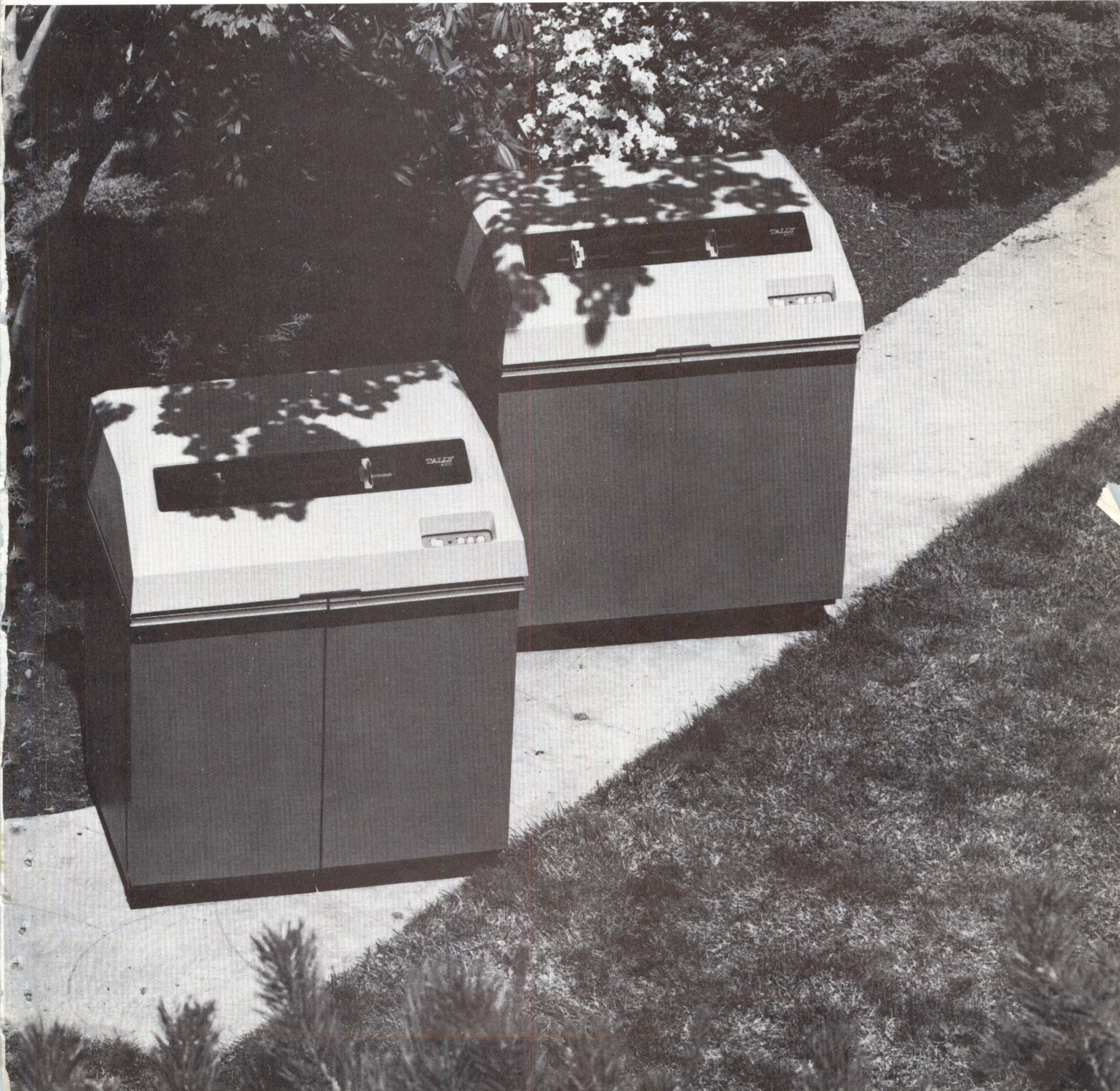Interfaces and controllers

Model 4400
400 lines per minute
132 columns
9 x 7 comb matrix print
Multi-part forms to 19"
Up to 12-channel VFU
20 ips slew
Interfaces and controllers

TALLY
has something new

# TAKE THE LEAD WITH THE 2ND NEW 4K STATIC RAM FROM EMM

TTL-COMPATIBLE; FULLY STATIC.
The new SEMI 4200 is fully static like the 4402 we recently introduced. But in addition it is TTL-compatible, output as well as input. Thus you can not only forget about refresh and charge pump circuitry when designing high performance MOS memory systems, you can also forget about drive amplifiers.
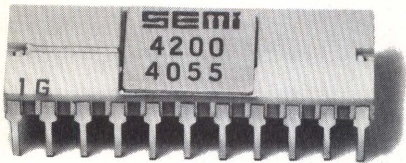
225 NANOSECOND ACCESS. The SEMI 4200 4K static RAM has a worst case access time of 225 nsec, and a worst case cycle time of 400 nsec. *It is the fastest TTL-compatible 4K static RAM in production.*

LOW POWER. The SEMI 4200 requires 450 mw operating power. And, just as with the 4402, power conservation is achieved by the Chip Select Input, which causes the 4200 to enter a low power standby state whenever it is unselected. Normal V_{DD} is 12Vdc, but V_{DD} can be reduced to 4 volts without risking loss of stored data, thus permitting the design of effectively non-volatile systems. Power consumption in this mode is less than $2\mu W/bit$.
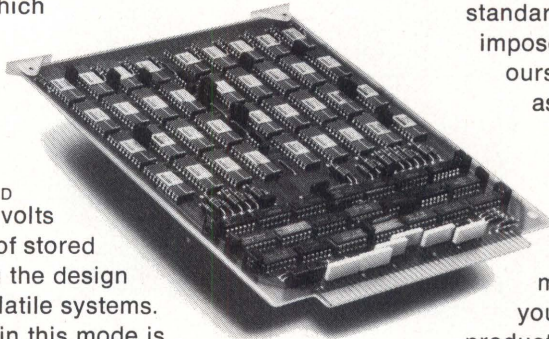
MICRORAM 1240.
16K x 8/9 using
SEMI-4200 4K Static RAM

Ideal for
microprocessor applications.
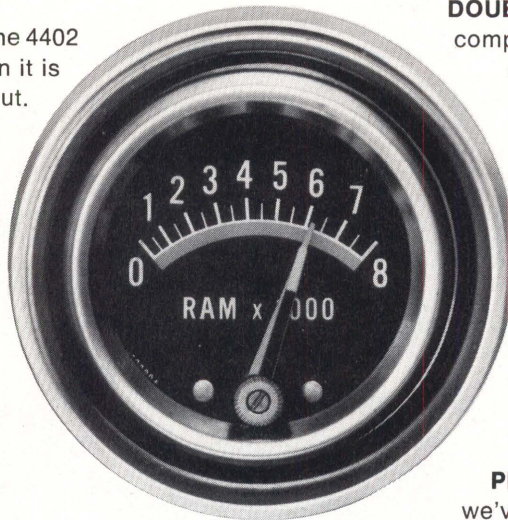
DOUBLE TESTED. Like all SEMI NMOS components, the 4200 TTL-compatible 4K static RAM must meet our own tough test standards, since we use it in our memory systems. In fact, our normal procedure requires 100% ac and dc testing of all components twice — at wafer and again in the package.

MODEL SELECTION. EMM SEMI offers you a growing line of static RAM and ROM components to help you take the design lead. Pick out the one that best meets your needs from the adjacent chart.

PROVEN TRACK RECORD. At EMM we've been making memory components and systems since 1961. Unlike memory suppliers who market components only, all EMM components are performance proven in our own systems. When you buy from EMM, you get the benefit of the unusually high acceptance standards we impose on ourselves, as well as our years of experience in meeting the needs of the memory marketplace. If you'd like further information about any of the products featured here, or any other EMM components or systems, contact your local EMM office today.

Part No.	Bit Org.	Access Time
RAMS		
SEMI-4200	4096 x 1	225 nsec
SEMI-4402	4096 x 1	200 nsec
SEMI-1801	1024 x 1	90 nsec
SEMI-1802	1024 x 1	70 nsec
SEMI RA-3-4256	256 x 4	1 usec
SEMI RA-3-4256B	256 x 4	1 usec
ROMS		
SEMI RO-3-4096	512 x 8	500 nsec
SEMI RO-3-5120	512 x 10	500 nsec
SEMI RO-3-16384	4096 x 4	1 usec
SEMI RO-3-8316A	2048 x 8	850 nsec

More new products to come . . . additional 4K static RAMs, ROMs.

EMM SEMI

A subsidiary of Electronic Memories & Magnetics Corporation
3883 North 28th Avenue, Phoenix, Arizona 85017
Telephone (602) 263-0202
CIRCLE 33 ON INQUIRY CARD

Research project shows microprocessors to be economically feasible, faster than a manual sampling technique, more flexible than an automatic analog approach, and cheaper than a minicomputer, in a lumber testing machine. Part 1 describes the hardware required along with the microprocessor, the interconnections, and the operation of various components

Using a Microprocessor: A Real-Life Application

Part 1—Hardware

James D. Logan and Paul S. Kreager

Washington State University
Pullman, Washington

This 2-part article presents the complete implementation of a microprocessor-based system. Part 1 describes the hardware required, along with the microprocessor, the interconnections, and the operation of the various components. Although the description is based on a specific microprocessor, the system is suited for diverse uses, and the details on its implementation and accompanying description of how problems encountered in its development were overcome should prove helpful to those developing their own systems, whether based on this processor or on others.

Since the software necessary to make a microprocessor-based system perform its intended function is new even to some experienced hardware designers, Part 2 of this article, to be published in the October issue of *Computer Design,* will illustrate how the software for this specific system has been put together. Emphasis is placed on concerns common to most users of microprocessors, with generally applicable details explained in sufficient depth to provide a basic understanding for those interested.

Microprocessor chips are being used in more and more applications that were once thought unsuitable for digital implementation on the basis of cost-effectiveness or complexity. Their ability to perform many different complex functions with a single collection of hardware, simply by altering the software, represents a very large contribution of computer science to society. In particular, the recently developed capability to extend this concept to smaller systems is highly significant. As a result, engineers must educate themselves in applying computer technology to a variety of design problems. These problems are likely to show up in force in any project, regardless of its ultimate goal. While details of their solution may depend on particular applications, the general approach to solution can be shared among projects. Once they have been solved for one project, they will be much easier the next time.

One such project, using a particular microprocessor, shows how some of these problems were overcome. The microprocessor is the Motorola MC6800, chosen because of its second-generation 8-bit architecture, very usable instruction set, versatile addressing modes, device and memory allocation scheme, throughput capability, and availability of alternative sources of supply. The device's flexibility is extended by its requirement for only one power supply and the availability of a family of parts tailored to operate with the microprocessor.

While many other microprocessors are available, only the MC6800 is discussed because it and its associated control and memory adjuncts are generally applicable. Readily available details about the microprocessor are

LUMBER UNDER TEST

ACCELEROMETERS
(STRESS WAVE SENSORS)

SYSTEM
BUS

T-COUNTERS
(10 EA)
(μs TIMERS)

DEVICE 1
T-COUNTER
INTERFACE

DEVICE 2
IMPACTOR
CONTROL

LOAD
CELL

WEIGHT(DPM)

LENGTH

WIDTH

THUMBWHEEL
SWITCHES

FOR DATA ENTRY

THICKNESS

FUNCTION

DEVICE 3
DATA INPUT

DEVICE 4
DISPLAY
INTERFACE

MOE-
LO POINT

7-SEGMENT
DECIMAL DISPLAYS

FOR DATA OUTPUT

MOE-
AVERAGE

LP LOC'N

T-COUNT

DENSITY

DEVICE 5
CONTROL
PANEL

CONTROL
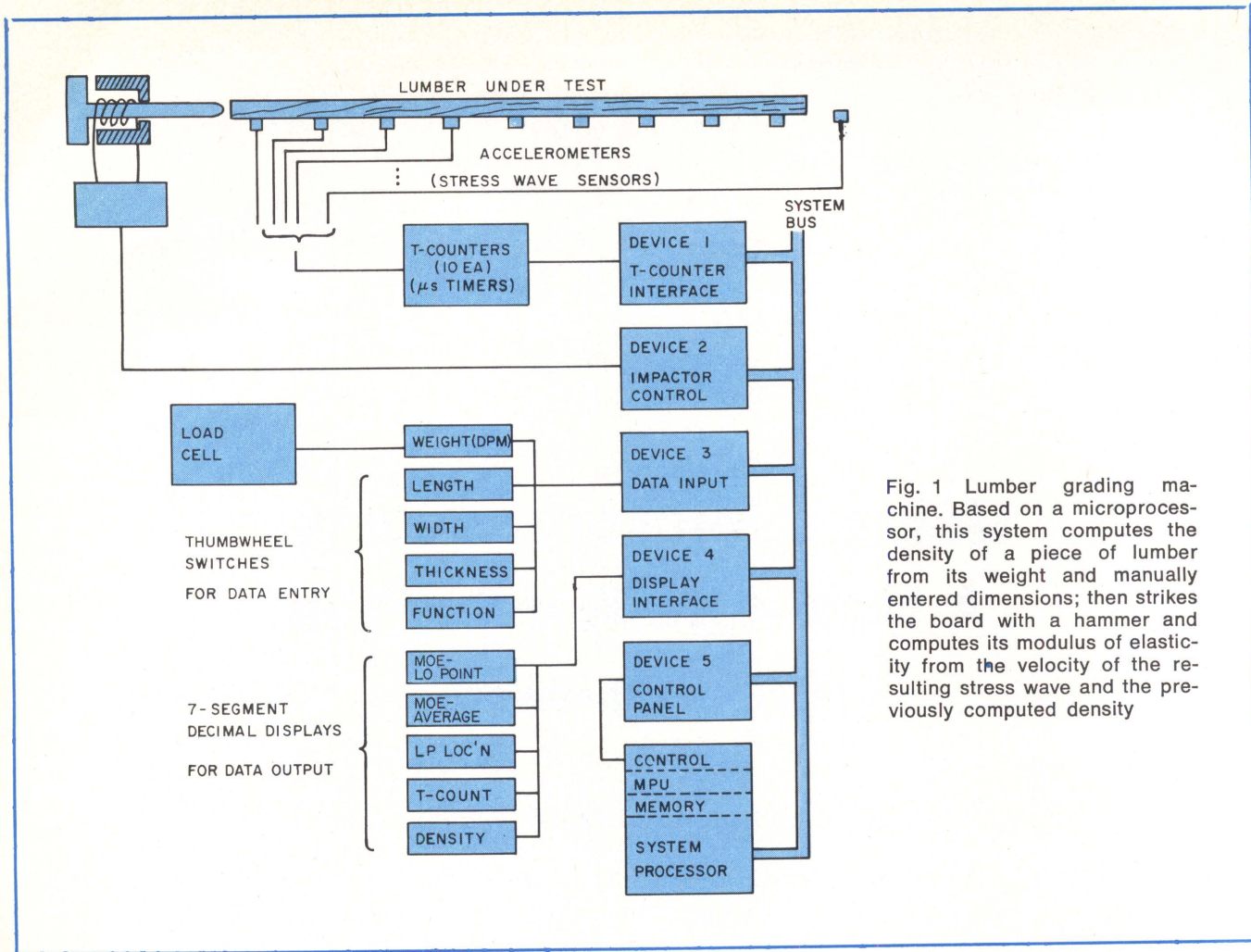
MPU

MEMORY

SYSTEM
PROCESSOR

Fig. 1 Lumber grading machine. Based on a microprocessor, this system computes the density of a piece of lumber from its weight and manually entered dimensions; then strikes the board with a hammer and computes its modulus of elasticity from the velocity of the resulting stress wave and the previously computed density
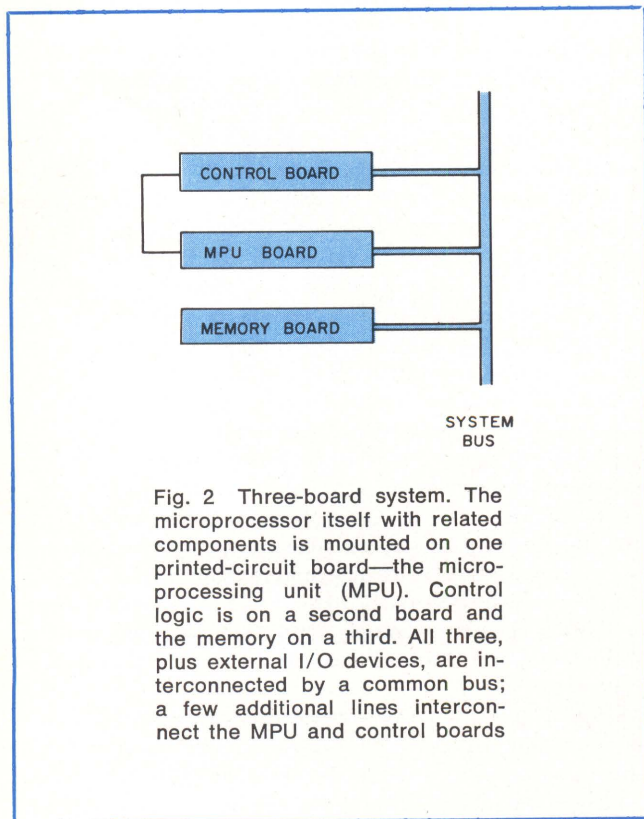

CONTROL BOARD

MPU BOARD

MEMORY BOARD

SYSTEM
BUS

Fig. 2 Three-board system. The microprocessor itself with related components is mounted on one printed-circuit board—the microprocessing unit (MPU). Control logic is on a second board and the memory on a third. All three, plus external I/O devices, are interconnected by a common bus; a few additional lines interconnect the MPU and control boards

not included, except in passing, to allow some more subtle details to be explained more thoroughly.

Design Goals

To evaluate the mechanical properties of lumber, a nondestructive testing machine was developed at Washington State University. Measuring the modulus of elasticity (MOE), a mechanical property of solid material that characterizes the material's stiffness (see "Modulus of Elasticity," p 71), the tester (Fig. 1) consists of a solenoid-driven hammer, or impactor, that induces a longitudinal stress wave in the test specimen through a pneumatically operated clamp mechanism; sensors spaced at 2-foot intervals along the specimen to detect passage of the stress wave; and clock-driven counters that measure the wave's travel time between sensors. The tester's inputs for length, width, and thickness are thumbwheel switches with binary-coded decimal (BCD) outputs. A function switch provides front-panel control over microprocessor program routing. Weight input is an analog signal from a load cell converted to BCD by a digital panel meter, which also displays the weight. T-counters (timers) are 3-stage decade counters driven by a 1-MHz crystal clock and producing BCD outputs. With faster microprocessors, which can incre-

ment a register and test the status of an input line in less than 1 μs, the timing function could be performed internally in firmware.

Processor outputs are displays and a signal to the impactor driver. Displays are 7-segment decimal numbers that indicate density, average MOE, and low-point MOE in engineering units. Location of the weakest segment is displayed as a decimal number from 1 to 10 that identifies the accelerometer that measured the lowest MOE. The T-count displayed is the number corresponding to the weakest segment.

Since the first machine was constructed to provide prototype experience, it provides more versatility than is required of an online machine. In normal operating mode, the machine must:

(1) Reset and enable T-counters, and blank displays, to accept new data;

(2) Release the impactor;

(3) Disable T-counters after the stress wave passes, to prevent noise from introducing errors;

(4) Read in all data (length, width, thickness, function, weight, and T-count for all registers);

(5) Find the specimen's largest T-count and locate the low point (firmware must decide which T-counts to ignore if the specimen is shorter than the full length of the machine);

(6) Compute density (weight/volume);

(7) Compute low-point MOE from the largest T-count;

(8) Compute average MOE from measurements taken by active T-counters; and

(9) Display results.

From this list it is apparent that considerable data handling is required—along with the four basic arithmetic functions, which are performed on decimal (BCD) numbers when solving the basic equations, selecting the low-point modulus, and computing averages. Development of software to perform these basic functions will be discussed in Part 2 of this article.

Processor Requirements

To fulfill several goals, the system was designed to be general-purpose for use in many applications. Packaging the microprocessing unit (MPU) separately allows the most versatile usage and permits rapid construction of a variety of systems. Bus architecture provides sufficient drive capability for system expansion and allows test equipment to be used on the bus without introducing loading problems. The processor is applicable in any system having many interrupting devices.

Memory, control, and MPU boards, connected by a common bus (Fig. 2), make up the system processor. Some applications may not require the control board, which adds features not included on the MPU board. Three lines between the MPU and control boards are not part of the bus; these lines are specific to applications requiring the control board. The MPU board was designed to function without modification for applications that do not require the control board.

The MPU board (Fig. 3) houses the microprocessor chip and the basic peripheral logic that most systems require. All MPU board outputs have been buffered

A Review of Modulus of Elasticity

If a stress, or uniform load, P, measured in pounds per square inch, is applied to a sample of any structural material, the material undergoes a strain, or deflection, measured in microinches (10^{-6} in.) per inch of length. Modulus of elasticity (MOE) is the ratio of stress to strain:

$$MOE = \frac{P(lb/in.^2)}{\Delta(in./in.)}$$

Because strain is a ratio of two lengths, it is itself dimensionless; therefore MOE, like P, is measured in pounds per square inch. In the Washington State University tester, stress is compressive; in other tests, tensile and twisting loads are often used, each with its own value of MOE. In most species of soft wood, the modulus perpendicular to the grain is less by a factor of perhaps 20 than that parallel to the grain.

Modulus of elasticity is used in mechanical structural analysis for many purposes, such as beam deflection and load-sharing calculations. Its value varies in structural materials; for example, aluminum has a modulus of about 10 million lb/in.² and steel about 30 million lb/in.², depending upon the alloy and treatment in both cases. In wood, the modulus ranges from 0.5 million to 3 million lb/in.² Since the modulus of wood varies so widely, and since more wood is used structurally than all other building materials combined, a rapid convenient method for measuring its MOE is economically important.

Although modulus of elasticity can be determined directly by measuring the amount of deflection that results from application of a given force to a sample, a faster method is to strike the sample with a hammer and measure the velocity of the resulting stress wave. This velocity, C, and the density, D, give the modulus, through the relationship:

$$MOE = C^2D$$

For easier measurement, the relationship can also be expressed in terms of inverse velocity, or the number of microseconds, ΔT, per foot of wave travel (for most typical species of wood, ΔT lies in the range 50 to 200):

$$MOE = \left[\frac{1}{\Delta T}\right]^2 D(2.1566 \times 10^8)$$

The multiplying factor accounts for several discrepancies in dimensions. One discrepancy is in density, measured in mass per unit volume, whereas the conveniently measured quantity in lumber is weight, which is a force equal to the mass multiplied by the acceleration of gravity, g = 32.2 ft/s². Also, since MOE is in pounds per square inch, ΔT should be expressed in seconds per inch rather than microseconds per foot, density in pounds per cubic inch instead of the more common pounds per cubic foot, and g in inches per second squared.

An additional advantage of measuring MOE in this way is that it permits multiple measurements of the velocity along the length of the specimen, which locates any weak sections in the lumber and thereby enables automatic defect-trimming operations.

fully to increase fanout above that of the microprocessor itself, which is limited to one TTL load per output. All buffered outputs, except clock ϕ1, ϕ2, and Reset, are under control of the microprocessor's Bus Available (BA) output; this allows those signals that are not controlled by the BA output to be used by devices on the bus in either normal or direct memory access (DMA) mode.

Direct Memory Access

Although the lumber grading application does not require direct memory access (DMA), the MC6800 is capable of this operation in a multiprocessor or controller configuration, where more than one device requires access to system memory.

Direct memory access uses the Bus Available (BA) and Halt signals on the system bus. A device requiring memory access pulls the Halt line to ground and waits for the BA signal to appear, signifying that the microprocessor has completed an instruction and stopped processing. (The microprocessor's clocks remain running.) The DMA device next performs its data transfer and, when finished, releases Halt; this ends the DMA operation.

An alternative DMA implementation uses the three-state control (TSC) input instead of the Halt line. When the clock runs at 1 MHz, TSC stops the processing after a delay of only 0.5 μs rather than at the end of an instruction, which can require up to 12 μs. However, TSC must be activated on the leading edge of clock $\phi 1$, stopping the clocks with $\phi 1$ high and $\phi 2$ low; the subsequent DMA must be completed quickly, because if the clocks are held static for too long a period, the microprocessor, which is a dynamic device, will lose its internal data.

Choice of TSC or Halt depends largely on the application. As a general implementation, the decrease in response time achieved with TSC is not significant in view of the additional complexity required and the small number of anticipated applications that will need this performance.

Reset logic holds the reset condition on (Reset line down) for several milliseconds after power is turned on. A switch on the control panel also controls the Reset logic. At the trailing edge of the Reset signal, the microprocessor automatically begins a power-up routine, which fetches an address stored in the read-only memory (ROM). This address points to a power-on routine elsewhere in the ROM. A branch then is taken to the power-on routine, which initializes all microprogram registers and counters.

Two interrupt inputs are available in the microprocessor: Interrupt Request (IRQ) and Non-Maskable Interrupt (NMI). IRQ usually originates in devices connected to the bus, while NMI is used as a power-failure interrupt (although it can be used for other purposes). Since IRQ is maskable in software, it is useful in controlling device interrupts in systems that require interrupt operation. NMI cannot be controlled by software, since no mask exists to enable or disable it; however, it can be controlled by hardware, and was brought into the control board for applications that require such control.

Two non-overlapping clocks are required as microprocessor inputs. Clock logic on the tester's MPU board provides fixed-frequency and pulse-width clocks; some other applications might need an adjustable frequency to vary processing speed. Since clock design may be difficult, problems overcome in the clock circuit used on the MPU board are discussed later in this article.
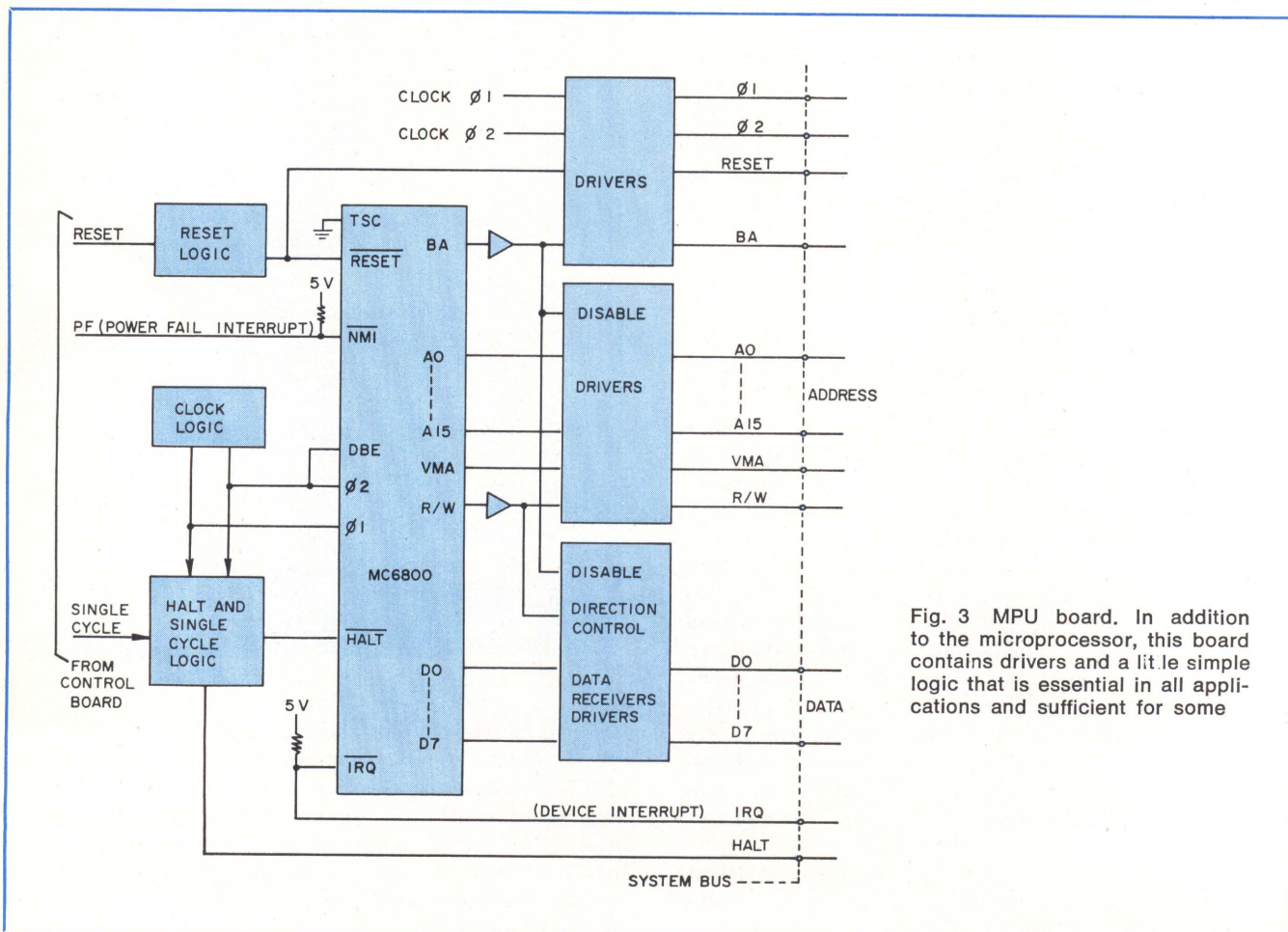

Fig. 3 MPU board. In addition to the microprocessor, this board contains drivers and a little simple logic that is essential in all applications and sufficient for some
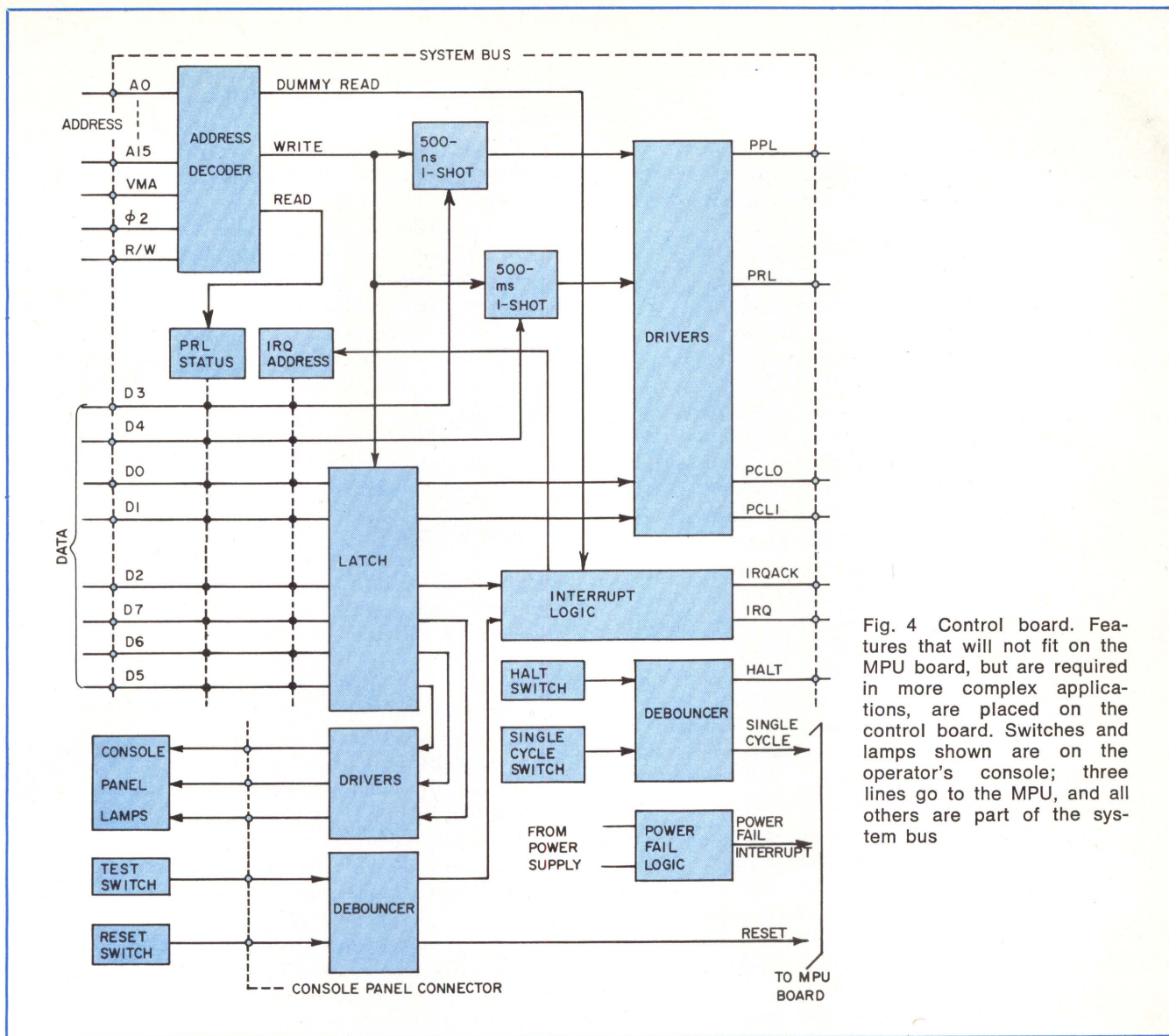
Fig. 4 Control board. Features that will not fit on the MPU board, but are required in more complex applications, are placed on the control board. Switches and lamps shown are on the operator's console; three lines go to the MPU, and all others are part of the system bus

The Halt input can have several uses. In addition to the function implicit in its name and its use in direct memory access (see "Direct Memory Access," p 72), it can step the processor one instruction at a time through routines stored in ROM. A switch input from the control board allows this dual usage. Necessary logic is described in more detail later, because it must be synchronized with the clocks to operate properly.

Efforts were made to design the MPU board as a component that could be used without modification in a variety of applications. Although some uses will not require the bus-buffering or single-cycle logic, both are useful in troubleshooting. When problems arise, test modules (such as data and address trap hardware) can be plugged into the system bus with few loading problems. Buffering also allows easy expansion of an existing system.

Address (A0 through A15), Data (D0 through D7), Valid Memory Address (VMA), and Read/Write (R/W) signals (shown in Fig. 3) are adequately described in MC6800 literature and present no significant problems for the designer.

Control Board

The control board (Fig. 4) provides expanded microprocessing system capability for applications that require it. Although it is difficult to predict which additional features may be desirable in future applications, the control board is designed to function as a general-purpose component, as was the MPU board.

Basically, the control board provides two programmable pulse lines, two programmable control lines, interrupt hardware support, expanded MPU board control (Halt, Single Cycle, Power Fail, and Reset), and limited input/output (I/O) for a system console panel.

When the MPU addresses the control board and "writes" a byte in which bit 3 is a 1, a 500-ns single-shot produces a signal on the Programmed Pulse Line (PPL) on the system bus. This signal starts, terminates, or otherwise controls system processes or states that must take less time than an instruction cycle. Similarly, if bit 4 is a 1, a long 500-ms pulse appears on the Programmed Reset Line (PRL) of the system bus. This is a general reset pulse that is controllable by software,

73

and is long enough to control slow devices such as relays. Because of this long duration, the MPU must sometimes sense the PRL's state after generating it, and before continuing to other tasks. It does this by addressing the control board and "reading" a status byte—the converse of "writing" a PPL or PRL. By grounding selected lines of the data bus, PRL status logic generates a status byte just as a peripheral device sends in a data byte.

Two programmed control lines of the system bus (PCL0 and PCL1) are dc signals, not pulses. They extend the MPU's basic read/write operations. For example, an interface which must respond to both data and command information might be designed to respond to one PCL signal, say PCL1. When true, PCL1 will inform the interface that write operations to it are commands; when false, that operations transfer data. MPU software sends data or command information by first either setting or resetting PCL1; these are themselves commands to the control board, with the proper value in bit 1 of the command byte.

Several lines from the control board support control panel functions. Only the reset switch has a specific use, while the other four lines are general-purpose. The Reset signal is simply debounced; otherwise, it passes directly through the control board to the MPU board to initialize the system while power stays on. The other lines are used, for example in the lumber tester, to control panel lamps that indicate system states and to respond to a test switch that initiates a test sequence within the software.

In systems with several interrupting devices, control and priority become quite cumbersome when using the MC6800 without additional hardware support. If not supported, the microprocessor, when interrupted, fetches an address stored in ROM, which in turn points to the interrupt service routine elsewhere in ROM, in much the same way as the power-on routine is summoned. The service routine then locates the interrupting device by polling, which can take considerable time. Several methods are available to reduce this interrupt response time and lessen the amount of ROM storage required by the software polling code. In the lumber tester, the chosen method is a modified approach that has been used in minicomputers for many years.

In this method, the control board generates an IRQ acknowledgement (IRQACK), which propagates through all interfaces that could have sent the interrupt. The one that did send it stops the propagation. Assume the MPU has been interrupted by device 2, while device 1 is idle and requires no interrupt service. In response to the interrupt, the service routine, instead of polling, sets the IRQACK latch on the control board, and generates a dummy-read instruction together with a dummy address, to which no interface on the bus would normally respond. Because device 1 did not originate the interrupt, it permits IRQACK to pass to device 2. The latter, being the interrupting device, prevents IRQACK from passing further along the bus and responds to the dummy read, even though the dummy address does not refer to it; in response, it dumps its return byte onto the data bus. This information can be an address, a number, an index, or anything that has a specific meaning to that particular interface. The service routine next drops the IRQACK latch, leaves interrupts disabled, and examines the return byte, which identifies device 2 as the source of the interrupt.

When the control board itself interrupts—that is, when the test switch is activated—IRQACK is not propagated and IRQ address logic returns a control-board address byte to the MPU when the dummy read is executed.

The remainder of the control board consists of the power-fail, halt, and single-cycle logic. Power fail as implemented here is a standard circuit which monitors the power supply and, when the voltage drops below a prescribed level, generates a warning signal to the MPU board. Halt and single-cycle switches are on the control board, not on the console; their outputs are debounced and passed to the MPU board, to stop it at the end of the current instruction cycle, and to permit it to execute one instruction, respectively.

Memory Board

As a separate component of the system processor, the memory board allows each application the maximum flexibility in physical space for variations of random-access memory (RAM) and ROM configurations. Its design takes into account several rules and suggestions: The MC6800 microprocessor makes no distinction between device and memory addresses. The first 256 bytes of memory should not be read-only, to take advantage of the MPU's direct-addressing capability; the rest of the memory can be any combination of read-only and read/write. The last eight bytes of ROM are reserved for address pointers to the restart, software interrupt, device interrupt, and non-maskable interrupt routines. In some applications, device I/O is more efficient if the index register can be used to transfer data between the device and MPU. All data transfers on the bus are serial by byte, one 8-bit byte at a time; those I/O devices that transfer two bytes ordinarily require two read instructions to do it. However, if the two bytes can be loaded temporarily into the 16-bit index register (provided that the index register is not otherwise in use at the time), the two bytes can be obtained with only one instruction.

Many applications of the microprocessor are unlikely to utilize the MPU's full 16-bit addressing capacity. Most of them would probably be satisfied with programs residing in 2048 bytes of ROM. A few more bytes of read/write memory plus the I/O devices probably would require only a few more addresses, necessitating at most 12 address bits. Thus, to reduce the extent of address decoding and to maintain similar addresses among different systems implemented with the processor, our preferred allocation of MPU hexadecimal addresses is: 0000 to 077F for the read/write memory, 0780 to 07FF for I/O devices, and 0800 to 0FFF for the read-only memory. This allocation leaves the most significant four bits of the address bus unused, and addresses (in decimal) 1920 bytes of read/write memory, 128 I/O devices, and 2048 bytes of ROM program space.

All system processor components are interconnected by the system bus, plus the power-fail, reset, and single-cycle lines that are connected only to the MPU and
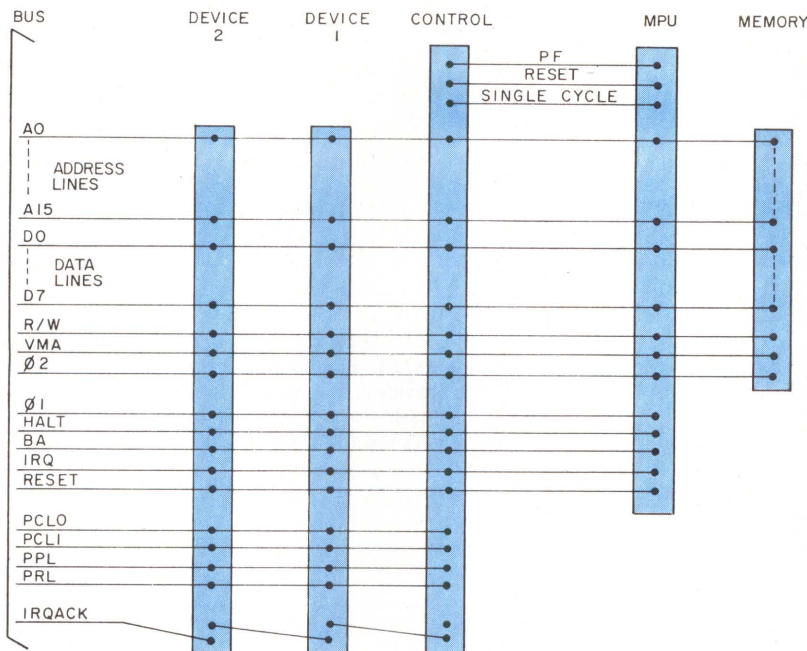
Fig. 5 System bus. A hypothetical system comprising the three boards of Fig. 2 and two external devices would be interconnected in this way. The IRQACK line, which acknowledges and identifies interrupting devices, loops from one to the next in daisy-chain fashion; all other lines are common to all units

control boards. A hypothetical system (Fig. 5) contains a memory, an MPU, a control, and two I/O device interfaces. Each I/O device taps every bus line except IRQACK; the latter enters the device through one pin and leaves from another, so that the device can control the propagation of IRQACK. A 50-pin connector is more than adequate for this bus, including power pins and several spare pins.

In the lumber tester, which has five devices on the bus, the control board services three types of interrupts. One is a control board interrupt, signifying that the system operator has initiated a test operation. It causes a firmware branch into various test modes determined by the function switch.

A second interrupt is a start signal from the control panel, which initializes the system, fires the impactor, and waits for completion of the stress wave measurement—all under firmware control. A data interrupt, the third of these signals, informs the processor that the stress wave has passed the accelerometers, so that the modulus of elasticity for the lumber specimen under test can be computed from the numbers in the T-counters.

Three lamps driven by the control board indicate to the operator that the system is ready for a new command, is in a test mode, or is servicing a previous command. Interrupts are enabled only during the ready state. The test lamp verifies to the operator that a selected hardware test has begun execution.

The 500-kHz clock in the MPU allows use of relatively slow memories; the MC6800 itself can use a 1-MHz clock. This half speed did not appreciably degrade response time goals for computation of the MOE, density, or other values. Considerable error checking is designed into the firmware, with control panel lamps associated with each error. For instance, T-counter information is checked; if one or more counters are not within prescribed limits, another panel lamp indicates a defective T-counter readout. Switch inputs from the operator also are checked for reasonable values; if one shows, for example, zero thickness, the firmware signals the error condition by turning on still another console lamp.

Special Considerations

Since time and money necessary to either construct or purchase special test equipment for the microprocessor system were lacking in this project, the testing machine was designed, implemented, and debugged on a stand-alone basis with only normal shop test equipment. The fact that this was possible in a reasonable amount of time attests to the relative ease of using the MC6800.

One factor that aided the debug phase was a test program that formed an integral part of the firmware residing in ROM. Such a test program is strongly encouraged, especially when MC6800 test equipment is not available. However, it should not be written until some experience has been gained in writing other routines; this will eliminate many errors in instruction coding and usage. Errors can be reduced further by
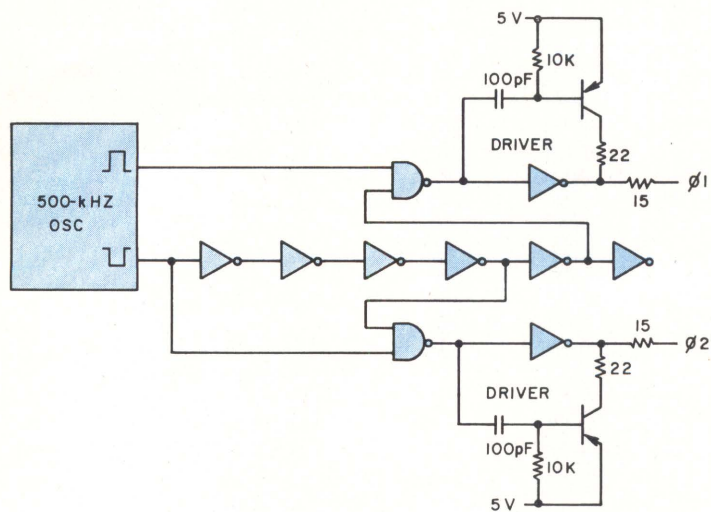
Fig. 6 Clock driver. The microprocessor requires a 2-phase non-overlapping clock, which is provided by one oscillator with complementary outputs and a string of inverters to delay one phase with respect to the other
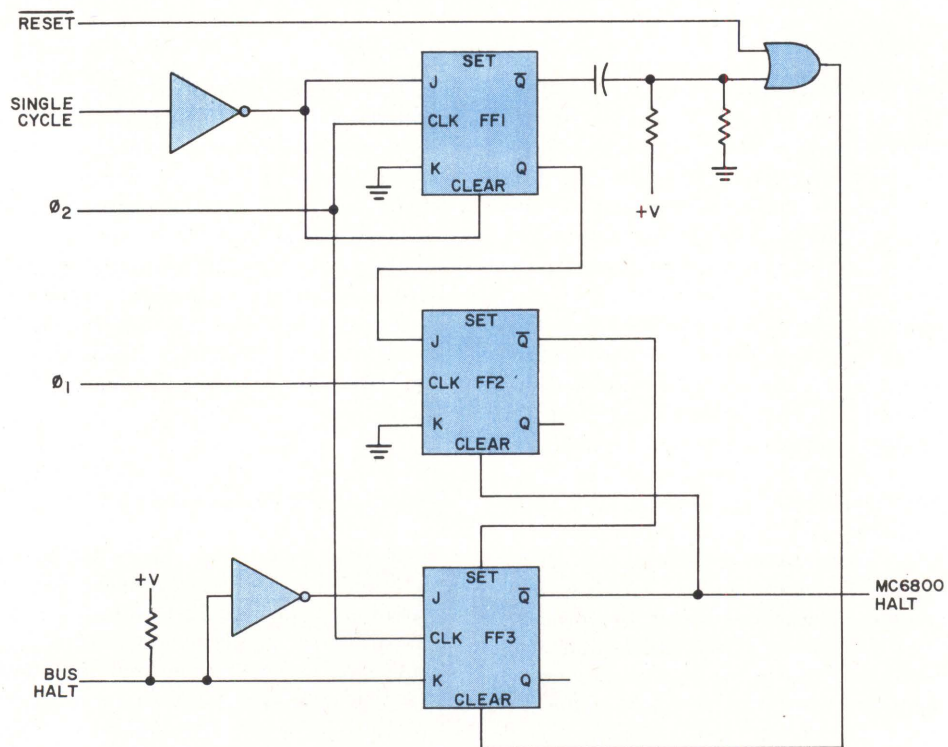
Fig. 7 Halt and single-cycle logic. A Halt signal on the bus, either by itself or in conjunction with a direct memory access by an I/O device, stops the microprocessor. If the single-cycle button is pressed while Halt is present, these three flip-flops permit the microprocessor to step through one instruction

keeping the coding simple and short when writing the test program. Users following this procedure should be able to write enough error-free code for the initial hardware debugging.

Our test program was designed for two purposes: to assure system operators that the system is operating properly, and, secondly, to provide specific test functions for use with an oscilloscope by maintenance personnel. Operator assurance tests consist of routines to read and display switches, load console displays, and test the read-only and read/write memories. Test routines for maintenance contain loops running several seconds so that a scope can be synchronized to various signals in the processor. These tests generally consist of activating programmable lines of the control board.

Clock circuits, as mentioned earlier, often cause difficulty. The lumber tester works well with complementary oscillator outputs, which are introduced to differing delays (Fig. 6) to form non-overlapping $\phi 1$ and $\phi 2$ clock signals to the clock drivers. The delays can be varied by connecting the NAND gates to different locations on the inverter string, provided that $\phi 1$ must be tapped after an odd number of inverters and $\phi 2$ after an even number.

MPU clocks are not TTL-compatible. However, the clock specifications are currently being revised, and specifications should be consulted if a different driver than the one shown here is used. The 100-pF capacitor worked well for 500 kHz but may have to be changed for other clock frequencies.

Single-cycle logic (Fig. 7) is another potential troublespot. It releases the Halt input just before the rise of $\phi 1$ (when $\phi 2$ drops) and then clamps it low again slightly after the fall of $\phi 1$. Single-cycle logic operates only when the halt switch on the control board is active. Therefore, this switch and the single-cycle switch feed an AND gate that produces the single-cycle input shown in the diagram. In single-cycle operation, the bus Halt signal is held low, stopping the microprocessor, until it is manually released by the halt toggle switch. While this switch is on, if the single-cycle pushbutton is pressed, the microprocessor executes one instruction and stops again. When Halt is down, flip-flop 2 is held cleared, ignoring the J input from flip-flop 1. Next, when the single-cycle button is pushed, the true output of flip-flop 1 goes low on the falling edge of $\phi 2$. The resulting negative-going pulse from the RC network, at the complementary output of flip-flop 1, clears flip-flop 3, releasing the Halt input of the microprocessor. This permits flip-flop 2 to turn on at the next falling edge of $\phi 1$ which forces flip-flop 3 to turn on again, restoring the Halt input of the microprocessor. The single-cycle pushbutton has no further effect until released and pushed again.

Conclusions

Design and implementation of processor and supporting software required four man-months of effort. The next project is expected to proceed much faster now that some experience has been gained and the processor

hardware has been designed; it will require only new interfacing circuits and new software. The working software modules for BCD arithmetic will greatly speed up software design as well.

Several alternative methods were examined and rejected before implementing the system using the MC6800 microprocessor. For example, modern analog computing techniques could perform the computation functions with acceptable accuracy. However, the all-digital approach is completely free from drift, and the microprocessor provides data handling capabilities that would be very difficult with analog circuits. Although BCD arithmetic could have been done at low speed by a calculator chip, requirements for moving data would have had to be implemented some other way. The microprocessor does both. A minicomputer was seriously considered, but would have been very expensive and more powerful than necessary. All things considered, the MC6800 microprocessor was tailored nicely to the application in versatility, arithmetic capability, and cost.

The lumber grading machine constructed in this project is a laboratory device which thoroughly analyzes the modulus of elasticity and related properties of a piece of lumber in less than two seconds. It could be installed easily in a cross-transfer conveyer chain for rapid stress wave testing of lumber at the mill.

Acknowledgment

Reference

"MC6800 Microcomputer Reference Mannual," Motorola, Inc, Semiconductor Products Div, 5005 E McDowell Rd, Phoenix, AZ 85008.

James D. Logan, an associate in the electrical engineering dept at Washington State University and vice president of Metriguard, is co-developer of nondestructive testing and quality control methods for grading lumber. He holds BS and MS degrees in electrical engineering from the University of Idaho.

Paul S. Kreager, a member of the engineering staff of Washington State University's computing center, is involved in hardware and software design and in development of computer-related systems. He received a BS degree in mathematics and an MS degree in computer science from Washington State University.

Hear what our competition is saying about the SEL 32 mini?

Nothing.

Can you blame them? After all, the SEL 32 gives you more "bang for the buck" than any other minicomputer. And that's not idle gossip.

Remember Data General's claim that other companies didn't run benchmarks against the Eclipse? We did . . . including their famous Whetstone benchmark. The results? The SEL 32 ran significantly faster.

As for Interdata, they compare prices and specs of their 8/32 against the Xerox 550, IBM 370/158, DEC 11/70 and Eclipse. Why was the SEL 32 omitted? Truth is, the SEL 32 has better specs and lower prices than any of them. For example, the SEL 32 has a throughput rate of 26.67-million bytes per second compared to 6-million bytes per second for Interdata's 8/32. As for price, an 8/32 with 128K bytes of memory will cost you $51,900. An SEL 32 with the same memory and floating point will cost you only $43,900.

Since our competition isn't going to tell you anything about the SEL 32, call us or use the coupon. Our lips aren't sealed. Systems Engineering Laboratories, 6901 West Sunrise Boulevard, Fort Lauderdale, Florida 33313. (305) 587-2900. In Europe, 85 bis, Avenue Albert ler, 92 Rueil-Malmaison, France. Telephone 967-83-17.

CIRCLE 45 ON INQUIRY CARD

Send more detailed info on the SEL 32. K

Name _____

Company _____

Address _____

City _____ State _____ Zip _____

Phone _____ Title _____

SYSTEMS
ENGINEERING LABORATORIES

Although a technology may be familiar to most engineers, it may not find its way into their designs until long after it has been developed. Here is how several such technologies were used in one large computer

Building Today's Technologies Into a Large-Scale Time-Sharing System

Gerald F. Atterbury

Digital Equipment Corporation
Large Computer Group
Marlboro, Massachusetts

George F. Adams

Motorola Semiconductor Products Incorporated
Computer Applications Group
Lexington, Massachusetts

Several sophisticated computer-related technologies are receiving a relatively high degree of attention today. Although most have been known for several years, they have not been widely utilized by computer designers until recently. These include fast emitter-coupled logic (ECL), cache memory, and use of a separate console processor.

For example, the design of the KL10 central processor as part of the DECsystem 1080 was begun in late 1972 when no machine was employing commercially available ECL. As a relatively unknown performer in large-scale use, ECL [Fig. 1(a)] required tradeoffs to be made against the more popular Schottky transistor-transistor logic (TTL), as well as new interconnection rules. The latter were necessary for successfully implementing either ECL or Schottky TTL while retaining the techniques of a conventional production environment. System speeds for both Schottky and ECL are dependent on how these interconnections are made and how well each technology's capabilities are understood.

One particularly significant development in several recent machines—including the KL10—is the cache memory, which minimizes reference time. It is, in general, a small block of high speed memory—usually semiconductor—interposed between the processor and main
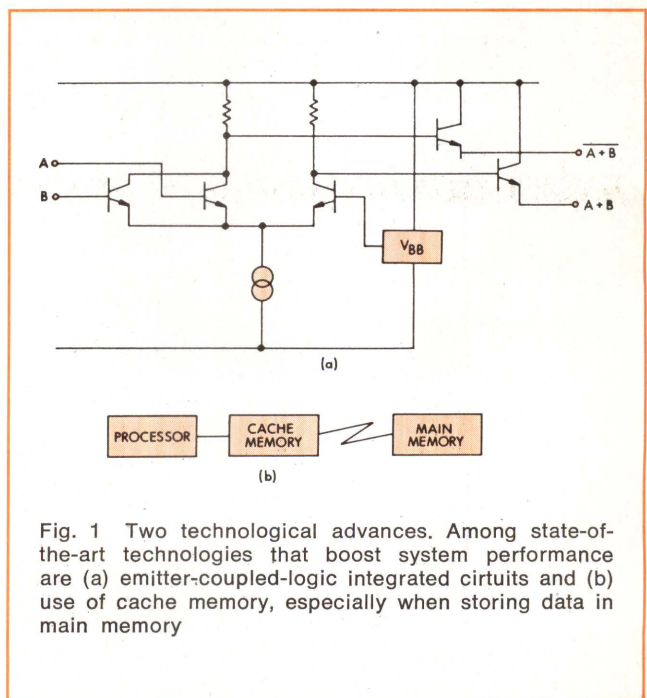
Fig. 1 Two technological advances. Among state-of-the-art technologies that boost system performance are (a) emitter-coupled-logic integrated cirtuits and (b) use of cache memory, especially when storing data in main memory

How Emitter-Coupled Logic Evolved

Various forms of ECL have been available for a number of years. Standard families have been obtainable since 1962, and custom circuits have been used in several large computer systems. IBM, for example, uses a custom family in its Systems 360 and 370 computers. RCA's former computer division (now part of Sperry Univac) uses other custom families in its Spectra 70 series.

ECL was among the first digital integrated circuit lines produced. One of these was Motorola's MECL I, introduced in 1962, having 8-ns gate propagation delays and 30-MHz flip-flop toggle rates, and dissipating 31 mW/gate. These characteristics placed it at the state-of-the-art for standard logic family performance at that time. However, most systems were not ready for 8-ns gate speeds, and several system-oriented features of MECL I prohibited its widespread use. For instance, it required a separately packaged bias voltage driver circuit, which in turn required extra circuit board wiring. Another limitation was its 10-pin package, in which only logic functions at the individual gate and flip-flop level could fit. In addition, it was not designed to operate with transmission lines, which were not necessary for ordinary logic interconnections when the circuits' rise and fall times were as long as 8 ns, but were required for long interconnecting lines, together with special drivers and receivers. In spite of these system constraints, MECL I still found usage in many specialized products and is still being produced.

The more advanced MECL II family, introduced in 1966, was also produced by other semiconductor manufacturers, including Signetics, Plessey, and Stewart-Warner. It included gates with 4-ns propagation delay and flip-flops that would toggle at over 70 MHz. Although its power levels were not lowered (30 to 35 mW/gate) and special drivers were still required for 50-Ω transmission lines, the bias generators for MECL II were internal, and more complex functions such as adders, multiplexers, and decoders became available.

The continuing development of ECL made possible an even faster family, with 1-ns delays and counter rates greater than 1 GHz. Announced in 1968 under the name MECL III, it still represents the fastest performance of any standard logic family. However, its fast rise and fall times required a transmission line environment for all but the smallest systems. For this reason, all MECL III outputs were designed to drive transmission lines, while internal 50-kΩ pulldown resistors were included on the circuit inputs so that unused inputs would not have to be connected to ground. Although the power levels of MECL III (60 mW/Gate) and its fast rise and fall times made its use in large systems difficult, it was widely used in fast instrumentation and communications equipment.

Nevertheless, in spite of their speed and system-oriented improvements, MECL II and III did not find widespread usage in large systems. In the late 1960s, standard TTL logic families met the speed requirements of most systems. By 1970, the TTL price war made the cost of MECL II and III seem relatively high; this, together with these families' system constraints (tighter than standard TTL), contributed to their apparent unpopularity. Then, Texas Instruments introduced Schottky TTL, the gate speeds of which were comparable to those of MECL II. Its direct compatibility with standard TTL made it the choice for many system designers who required 4-ns gates.

By 1971, however, trends in large systems demanded a logic family that was faster than Schottky TTL or MECL II, yet not subject to the system constraints imposed by the speed of MECL III. These circuits, of which MECL 10,000 is an example, were comparatively easy to use, because rise and fall times were slowed to 3.5 ns, while gate propagation delay was held at 2 ns. These rise and fall times permitted the use of standard circuit board packaging techniques, but the circuits could also drive transmission lines where that level of performance was needed. These circuits also dissipated less power than other ECL families—typically 25 mW/gate. This, together with advanced circuit design techniques, led to a new level of complexity in large-scale integrated ECL circuits, ie, inclusion of multiplexers, 4-bit arithmetic units, random-access or programmable read-only memories, 4-bit-by-2-bit multiplier, and a 4-bit slice (coming soon). This family's logic levels were directly compatible with those of MECL III, permitting redesign of critical timing chains in systems that used MECL 10,000 to upgrade them to higher performance levels of later generations of the system.

The circuit family is available from several major semiconductor houses, including TI, Fairchild, and Signetics. It has been used in numerous successful systems including the DECsystem 1080, which is state-of-the-art in machine architecture as well as in its logic family.

memory [Fig. 1(b)]. It holds selected information from main memory, chosen so that the instruction and data which the processor needs are usually in the cache. It boosts system performance because its speed exceeds that of the main memory and because (in large systems, at least) it is usually packaged in close proximity to the processor and therefore is not subject to delays that can occur in a long cable extending between a processor and its main memory when widely separated.

Another important idea is the use of a small console processor, which, in addition to running the console, handles a selection of peripherals and serves as a powerful diagnostic tool.

Performance Tradeoffs

An initial performance goal for any new machine can often be attained with either of two logic families: ECL or Schottky TTL. The choice between them is based on other considerations; for example, if ECL is used, its faster basic gate speed suggests that less complicated logic is possible.

Instruction-time calculations for the most commonly used instructions show that on the shorter ones, such as add or jump, performance is limited by the length of time required to fetch information from memory, while longer instructions such as multiply, divide, or floating-

point arithmetic are limited by logic circuit speed and are performed at a considerably higher speed on the ECL machine.

Although the cache improves performance of both Schottky and ECL machines, the degree of improvement is higher for the ECL because the basic speed of the logic is not masked by the memory. With the scientific Gibson mix of instructions, an overall comparison shows that, relative to the speed of an earlier reference machine (the KI10 processor of the DECsystem 10), the Schottky operates 1.75 times faster, the ECL 3.2 times faster. Thus the ECL machine operates at 1.8 times the speed of the Schottky—in itself a substantial improvement. Without a cache memory, however, the Schottky machine has a performance level of only 0.91, while the ECL's is 1.0—the same as that of the reference machine.

Choice of Technology

Selecting a logic family involves careful analysis of trade-offs concerning maximum performance and minimum cost as well as usage constraints of each logic type. To minimize cost, the choice should be an industry-standard logic family that is readily available and can be used with established packaging techniques, although performance goals may dictate a medium to high speed logic family. High speed logic turned out to be a better choice in the KL10 because medium speed would have required certain functions to be performed in parallel in order to achieve the performance goals, and parallelism would have required a greater number of integrated circuit packages and a physically larger machine. Most likely candidates among present high speed families are ECL and Schottky TTL.

When designing a large system with high speed logic, interconnection lines exceeding 6 to 8 inches in length must be treated as transmission lines. Standard packaging techniques are consistent with a transmission line environment if the line impedance does not exceed about 80 Ω. However, impedance of etched lines on a printed circuit board depends heavily on their widths and the thickness of the board; these factors prohibit controlled impedances greater than 80 Ω when standard manufacturing methods and tolerances are used. Therefore, the logic family used for any large system design should be compatible with such low impedance transmission environments.

ECL circuit structure is well suited for such a transmission line environment. The devices' specifications are given for driving 50-Ω lines, while the open-emitter outputs provide a low output impedance (7 Ω in either high or low state) and current sufficient for the low impedance lines. Their input impedance is high, producing very little loading on interconnection lines. In contrast, Schottky TTL devices have relatively high output impedances (14 Ω in the low state, 54 Ω in high), which can create system problems.

In either logic family, the output impedance forms a voltage divider with the line impedance, so that the voltage step that is created when the circuit turns on is somewhat lower that its ultimate value. Because the output impedance of the Schottky TTL circuit is high, this voltage divider action creates a relatively small step—lower than the threshold of nearby loads. How-ever, the step travels down along the transmission line and encounters an impedance mismatch at the far end; this mismatch causes a positive reflection which travels back to the point of origin. When it arrives, the full transition at the output of that circuit is achieved.

On the other hand, with a low output impedance, as in the case of ECL, the voltage divider makes a higher step at the output—high enough to switch these nearby loads without waiting for the reflection. Of course, the reflection comes eventually, unless the line is terminated in its characteristic impedance; but by the time it arrives, the transition that initiated it is long past.

The effect this has on system performance can be shown for a typical logic interconnection (Fig. 2). Typically, the length of time needed to drive this circuit configuration (which occurs frequently in systems) including a 12-in., 68-Ω line with an ECL driver, is 4.7 ns, whereas a Schottky gate requires 13.7 ns. Thus the ECL delay is only slightly over one-third that of the equivalent Schottky delay—better than predicted on data sheets, which specify 50% less delay. This difference is more pronounced on longer signal lines.

System noise immunity is a parameter of major importance. Both the susceptibility of logic to noise and the generation of noise by the logic—particularly when switching—must be considered. The dc noise margin depends on both power supply voltage and temperature differences between driving and receiving gates. ECL's dc noise margin is smaller than that of Schottky TTL, but dc conditions alone are not sufficient for successful system design; noise margin is also affected by the rate of change of signal edges and the magnitude of signal swing. System noise performance of ECL is superior in the worst case to that of Schottky TTL.

Logic power dissipation affects both system reliability and cost. Of course, reducing ambient temperatures on logic modules reduces the failure rate of active devices, and the logic module temperature is directly related to logic power dissipation. Coping with high power dissipation means increases in power supply, power busing, power line bypassing, and cooling—all of which cost more than they would for a logic family with lower power dissipation—other factors being equal.

Dissipation of a logic gate depends on dc current drain of the gate itself, dc and ac loading on device outputs, and transient currents through the device during switching. In comparing power dissipation figures, ECL power levels must include power dissipated in the line termination resistors. Partly for that reason, the average dc power dissipation of a Schottky gate, which depends on the output logic level, is about one-third less than that of ECL, but increases at higher switching frequencies because of an effect called overlap switching, or totem-pole spiking. Every gate has two transistors in series at its output, in a "totem-pole" configuration that drives current in the output line in both high and low states. In the dc state, only one of these transistors conducts at a time, but as the gate output switches, both transistors conduct simultaneously for a few nanoseconds. Thus Schottky gate power dissipation increases with frequency. At approximately 32 MHz, it equals that of the resistively terminated ECL gate and, at even higher frequencies, the Schottky gate dissipates more power than the ECL gate and its terminator do. The exact crossover frequency depends on the resistor value.
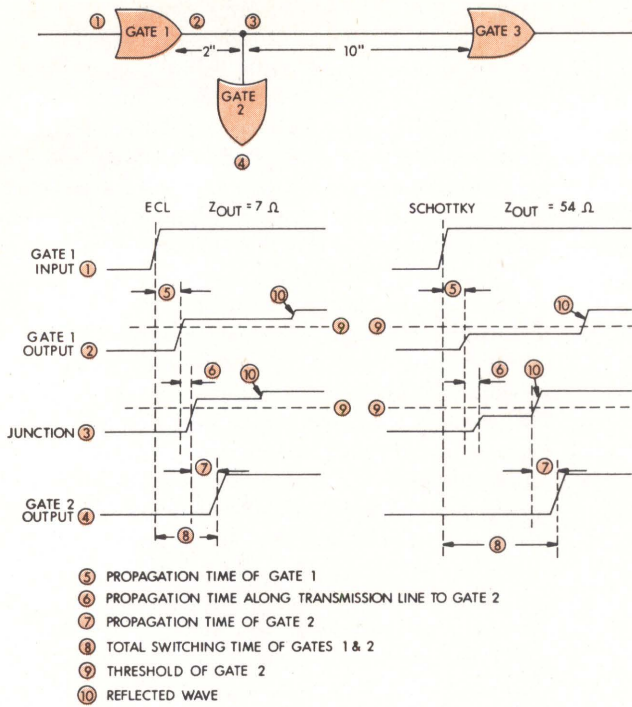
Fig. 2 How output impedance affects switching time. An output voltage step always propagates to the end of the line and is then reflected toward its source. If the source's output impedance is too high, output amplitude may not be sufficient to switch nearby gates before the reflection returns—increasing switching time unacceptably

⑤ PROPAGATION TIME OF GATE 1
⑥ PROPAGATION TIME ALONG TRANSMISSION LINE TO GATE 2
⑦ PROPAGATION TIME OF GATE 2
⑧ TOTAL SWITCHING TIME OF GATES 1 & 2
⑨ THRESHOLD OF GATE 2
⑩ REFLECTED WAVE
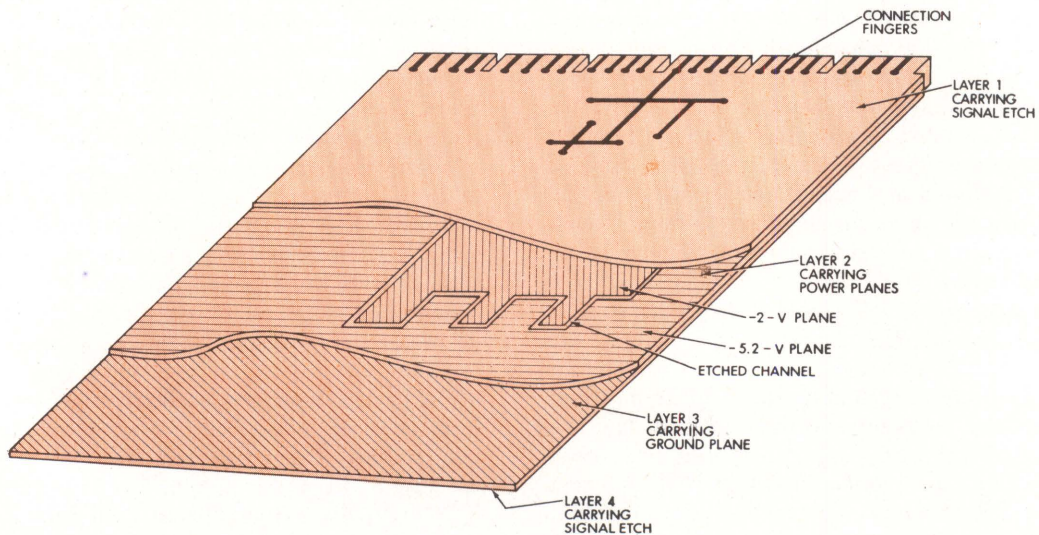
Fig. 3   Four-layer board. Signal lines are routed on the outer surfaces, while power and ground are distributed on the inner layers. Power at two voltages is distributed by dividing one of the two inner layers into two sections

System Packaging

Today's most advanced ECL circuits exhibit typical propagation delays of about 2 ns and rise times of 1 to 3 ns. Application of such high speed logic requires careful attention to crosstalk, reflections, and noise on the power supply and ground lines.

DEC's ECL processor was designed on 4-layer multilayer boards, shown diagrammatically in Fig. 3. These boards permit better component packing density than do double-layer boards because they route only signal lines on the board surfaces and consign power and ground lines to the inner layers. In addition, the impedance of signal lines can be kept close to the selected design value (68 Ω for the KL10—a choice based on the tolerance of the characteristic impedance of the etched lines and the pull-down current that these lines would carry to their termination resistors).

Of the two inner layers, one is a ground layer, while the other is etched into two interdigitated sections to distribute both -5.2 and -2 V on one layer. Since it maximizes the surface area available for signal lines, this is a very practical voltage distribution method, although it does require care in board layout.

Bunching

Because of the way programs are structured, usually any required group of information tends to be in memory locations that are close to information just used. Contributing to this "bunching" tendency is another tendency, ie, for any particular instruction or data word to be re-used. As a result, when a word is brought from main memory to cache memory, and then to the processor, a number of words in nearby locations of the main memory can also be brought to the cache and kept there. Once this is done, there is a strong likelihood that it will be called for within a short period of time—at least once and possibly several times; from the cache, this information is available to the processor much more quickly than from main memory. Furthermore, each such reference to information already in the cache saves one reference to main memory.

The result is that information is stored at a cost per bit that exceeds that of main memory only slightly, but with an average access time almost as short as that of the cache. For this to be true, a fairly high degree of success in finding information in the cache is necessary. This success is measured by the hit rate, ie, the number of processor requests satisfied by the cache divided by the total number of processor requests, including those that go to the main memory. Hit rates of 95% or better are achievable.

In the KL10 the cache holds 2048 words. When it becomes necessary to bring new data from main memory to the cache when the cache is full, the least recently used block of words is supplanted by the new data. The old block is usually destroyed; the exceptions, when they are moved back to main memory, are discussed later.

Cycle time of main memories used on the DECsystem 1080 is 1 μs, while the cache memory has an access time of 160 ns. Since the required information is found in the cache in about 95% of the memory references made by the processor, average access time for the cache/main memory combination is $(0.95)(160 \times 10^{-9}) + (0.05)(1 \times 10^{-6}) = 202 \times 10^{-9}$, or 202 ns—an impressive improvement over the straight 1-μs memories.

A New Use for Cache

In the KL10 the cache memory is used in a manner which is different from how it is used in any other machine announced to date. The KL10 both reads and writes in the cache; it does not update the main memory until space is needed in the cache. In other machines using the cache concept, the cache benefits only the reading of data; when new data are stored by the processor, it updates the contents of the addressed location in both cache and main memory. This is not a serious disadvantage, because in most applications, read cycles outnumber writes by 3 or 4 to 1. Thus in the KL10, write cycles benefit from the cache as much as read cycles do.

This innovation is based on the operation of the entire memory system. Main memory is divided logically into "pages" of 512 words, with each page organized as 128 lines of four words. In the user's program, an address occupies one-half word or 18 bits; this is a virtual address assigned by the programmer and subject to modification in order to obtain access to real memory. Modification takes place in the paging logic, which transforms the nine high-order bits of the virtual address into 13 bits that address a page (Fig. 4), while the other nine bits of the virtual address point to a word within a page.

These nine low-order bits address the data in the cache, which is divided into four sections (Fig. 5). Each section contains 128 locations, each holding four words, or one quadword. Thus total capacity of the cache is four sections by 128 locations by four words, or 2048 words of 36 bits each. Each of the four words also has two status bits appended to it. One, called the write bit, shows whether the word was put in the cache by the processor (in which case the original word in main memory is invalid). The other shows whether the word in the main memory has been changed since it was copied into the cache. If it has, the word in the cache is invalid; thus the second status bit is called the valid bit.

Of the nine bits of the unpaged address, seven address one of the 128 locations in each section, while two bits address one of the four words at that location. Because there are four sections, four words—one in each section —are selected by the nine bits.

One section, and therefore one word, is selected by the cache directory, which contains a number of 13-bit address registers. These in turn contain the main-memory page number from which came each quadword stored in the cache. A 2-bit use count for each quadword shows which of them is the least recently addressed and therefore subject to replacement by current data.

When the processor issues a read request, seven bits of the 18-bit virtual address select four of the 128 locations—one in each section of the cache—together with four registers similarly located in the cache directory. Two bits select one word in each of the four cache sections. The remaining nine bits of the virtual address go to the paging logic, which converts them into a 13-bit
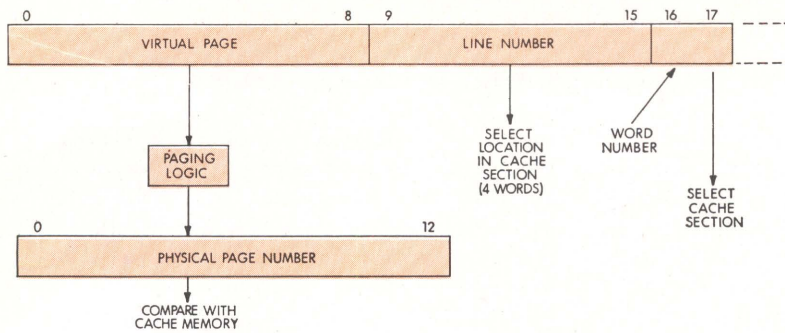
Fig. 4 Address transformation. The KL10 programmer always works with an 18-bit virtual address; its nine high-order bits most be transformed into a physical page number of 13 bits to identify the block of words that actually contains the desired data. Other bits go directly to cache
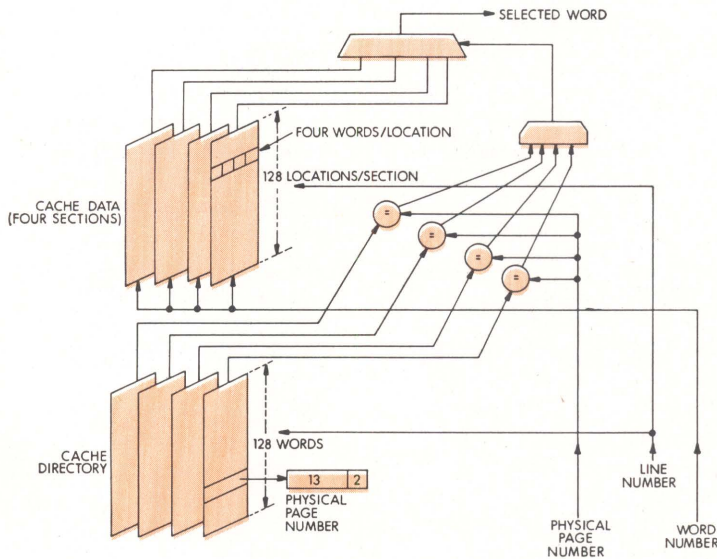
Fig. 5 Cache addressing. Cache memory is divided successively into four sections, 128 locations/section, four words/location. Status bits in each word keep track of independent updating in cache or in main memory, either of which renders the other at least nominally valid. Cache directory identifies the main-memory page, and therefore cache section, in which the desired address is found

physical page number. This is compared simultaneously with the four page numbers coming out of the cache directory.

Only one or none of the four addresses will match the physical page number from the paging logic. If there is a match, the cache directory section from which it came indicates a word from the corresponding section of the cache. If the valid bit of this word is 1, the word is the desired one, and it is transferred to the processor, while the use bits in the cache directory are updated to show that this word is the most recently addressed. If the valid bit of the selected word is 0, a core cycle is taken, updating all words in the quadword which have their valid bits off. Likewise, one or perhaps two core cycles follow if no physical page number from the cache directory matches the one from the paging logic. First, the use bits are checked to find the least recently used quadword. If any write bits in the quadword are 1, these words are written back into main memory, bringing it up to date with the cache. The same quadword is then replaced by a new quadword from the page specified by the paging logic. It is placed in the cache, the use

bits are updated, and the desired word is passed to the processor.

Console Processor

Most previous large computer systems have included a conventional operator's console, from which the system is controlled and data entered by means of switches. By this method, an operator could, for example, enter an instruction and data by the appropriate switches, set the clock frequency at a preselected value, and observe and control a sequence of operations directly. He could view the status of all processor registers, including input/output registers and control flip-flops—all displayed by lights.

Now a significant change in operating technique has been made, bypassing operational problems that arise because lights or switches can fail, particularly in ways that may not be obvious. A console processor (Fig. 6) can be designed into the system to replace the lights and switches, and to perform several other functions as well,
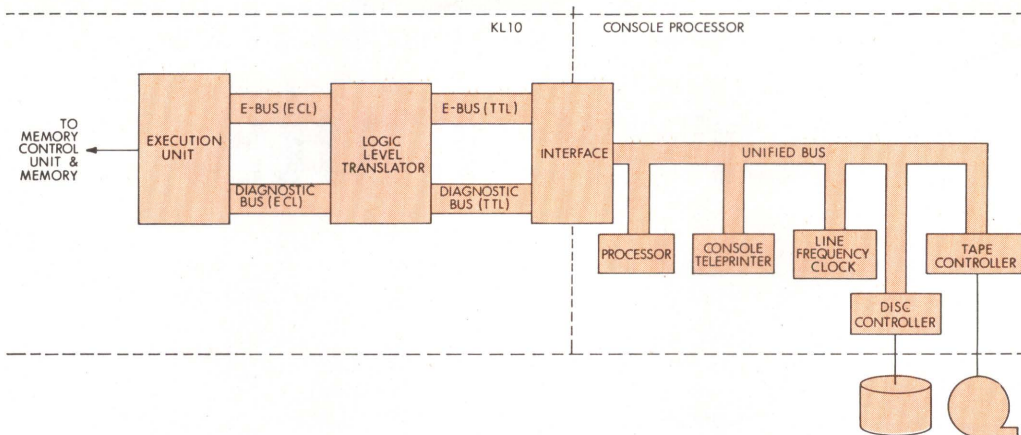
Fig. 6 Console processor. The KL10 has no operator's console in the usual sense; its functions are taken over by a separate minicomputer with its own set of peripherals, communicating with the main processor to control its sequencing and to bootstrap it, change its microprogram, and diagnose its malfunctions

such as loading all diagnostic programs, loading the microcode into the writable control store, bootstrapping the system (starting it from a completely cold or dead start), and providing a long-term power line frequency clock. (In the KL10 the console processor is a DEC PDP-11/40.)

An interactive console command language provides full diagnostic abilities, previously supplied by the lights and switches. With this language an operator can communicate with the system through the console tele-typewriter, obtain a readout of the status of any register, and trace the progress of any instruction or data. Furthermore, the processor can control the number of clock pulses before providing a status readout, or it can have the clock make single steps. In effect, the console processor is a system troubleshooter, as well as con-troller, and can diagnose the central processor and other system components.

The processor's diagnostic functions include the ability, if a cache failure has occurred, to turn off one or more of the four cache sections. Although processor through-put is thus reduced, the system is gracefully degraded rather than shut down completely. Likewise, for a failure in a section of main memory, that section may be ignored and 1- or 2-word fetches made from the remain-ing memory sections. This degrades memory bandwidth, as does turning off part of the cache, but allows the sys-tem to continue operating.

The processor's access to main memory is limited to two areas which are defined by software. One is written by the main processor and read by the console processor; the other is written by the console processor and read by the main processor. Both areas have their own relocation and protection checks, which are controlled by the main processor. Relocation permits the main processor to move these areas from place to place in the main memory, without consulting the console processor but not affecting

the latter's access to them. Protection prevents a user from inadvertently writing in these areas and thus de-stroying control and status information.

Either processor can interrupt the other, permitting both to carry out their appointed tasks asynchronously.

Conclusion

The system demonstrates that sufficient attention paid to design details allows advanced techniques to be com-bined with relatively straightforward packaging, fabri-cation, and manufacturing methods. None of the system's new features compromises the goal of compatibility with earlier systems of its family. It provides a new dimension of growth for large-computer users.

Gerald Atterbury holds a degree in electrical engineering from Brighton College of Technology, England. As Sys-tems Group engineering manager-Large Computer Engineering at Digital Equip-ment Corp, he is responsible for de-velopment of central processors and memories, in addition to circuit design, system packaging, and system interac-tion problems.

George F. Adams is a field applications engineer with Motorola Semiconductor, working with computer-oriented com-panies in development of emitter-coupled logic, microprocessors, and memory systems. He is a graduate of the University of Miami.

Cyclic redundancy codes, widely used in serial data transmission systems, can be implemented in parallel to gain enough speed for sharing by many lines and a consequent sharp reduction in cost

Parallel CRC
Lets Many Lines Use One Circuit

Arun K. Pandeya and Thomas J. Cassa

Interdata, Incorporated
Oceanport, New Jersey

In a data communication system that uses a cyclic redundancy code (CRC) for transmission reliability, a parallel implementation of the code can perform the necessary logic operations much faster than the conventional serial implementation.* Although parallel circuits are usually more expensive than the serial kind, in this case they can be cheaper, because the added speed permits a single circuit to be shared by several transmission lines. Furthermore, the new approach requires little or no redesign of the system using the CRC. All that is necessary is a different placement of the serial-to-parallel converter—before the error-correcting circuit instead of after it—in the receiver, together with a similar new placement of the parallel-to-serial converter in the transmitter.

In its usual form, a cyclic redundancy code operates on the serial bits of a message as if they were the coefficients of a long binary polynomial, $M(x)$. Mathematically, the code divides this polynomial by a fixed generator polynomial, $G(x)$, producing a quotient, $Q(x)$, and a remainder, $R(x)$:

$$\frac{M(x)}{G(x)} = Q(x) + \frac{R(x)}{G(x)}$$

An equivalent expression is

$$M(x) = Q(x)\,G(x) + R(x)$$

In modular arithmetic, this relationship is stated

$$M(x) = R(x) \bmod G(x)$$

When the message is transmitted, the quotient, $Q(x)$, is discarded and the remainder, $R(x)$, which is the check character, immediately follows the message. At the receiver, the division is repeated; an error-free reception is assumed if the check character computed from the message by the receiving station is the same as the one received with the message.

In practice, since the receiver does not know when the message stops and the check character begins in the stream of serial bits, it keeps on computing until the stream ends; if the remainder is 0, the reception is assumed error-free.

On the communication channel, the first message bit is assumed to be the coefficient of the highest power of x, the variable in the polynomial, and successive bits correspond to decreasing powers of x; the last bit goes with the zero power of x. In practice, the least significant data bit is transmitted first, so that it becomes the most significant bit for CRC computations. For example, if 92 in hexadecimal code is transmitted, the message polynomial is $M(x) = x^6 + x^3 + 1$ (see Fig. 1).

The remainder, $R(x)$, always has a fixed length equal to the degree of $G(x)$, the generator polynomial.

If the total number of bits in the message, represented as a polynomial, $M(x)$, is less than or equal to the degree of $G(x)$, the remainder is the message itself. To assure the presence of a check character that is distinct from the message, and for some other reasons as well, industry practice is to multiply the message

---

*Although the proprietary technique is not used in currently available Interdata products, it has been developed for possible use in future systems.

polynomial, $M(x)$, by x^N before dividing by $G(x)$, where N is the order of $G(x)$. This multiplication is equivalent to adding N binary 0's at the end of the message. In practice, multiplication by x^N is performed by both transmitting and receiving stations; no 0's are transmitted between the message and the CRC.

For example, suppose that the sending station, before transmitting polynomial $M(x)$, computes CRC-1 from it. The receiving station receives message $M'(x)$ and computes CRC-2.

CRC-1 $= x^n \ M(x) \mod G(x)$

CRC-2 $= x^n \ M'(x) \mod G(x)$

CRC-1 $-$ CRC-2 $= x^n \ [M(x) - M'(x)] \mod G(x)$

The expression between the square brackets is an error polynomial, $E(x)$, that has the same number of co-efficients as $M(x)$ and $M'(x)$. All coefficients are 0 except where a bit was received in error; therefore, $E(x)$ is a polynomial with only those powers of x that correspond to bits that are received in error. If $E(x) \mod G(x) = 0$, either the transmission was error-free or any errors that did occur were not detected by the code. From this simple fact, three important conclusions follow:

• All errors of n or fewer bits that lie only within n successive bits are detected by the CRC, where n is the degree of the generator polynomial $G(x)$.

• If $G(x)$ has $(1 + x)$ as a factor (ie, if it has an even number of terms), the CRC detects all errors with an odd number of bits in error, even if they are spread out over more than n message bits. All generator polynomials used in the industry have an even number of terms for this reason, because it assures that 50% of all possible random errors will be detected.

• All error patterns that are not divisible by $G(x)$ are detected.

Thus, a properly chosen generator polynomial is far more powerful than traditional vertical or longitudinal redundancy checking. In addition, cyclic codes are far more efficient than vertical redundancy codes (efficiency is the number of data bits divided by the total number of bits transmitted).

Conventional Serial Implementation

A binary division that ignores the quotient but retains the remainder is performed in hardware with an N-stage shift register. From the output of the last stage, a feedback path returns to the inputs of those stages of the register corresponding to the powers of X that have nonzero coefficients in the divisor—that is, in the generator polynomial. At each such input, a modulo-2 adder (exclusive-OR gate) combines the feedback signal with the output of the previous stage.

Cyclic redundancy codes are used in both the widely used binary synchronous (BiSync) communication protocol and the newer synchronous data link control (SDLC), which is just beginning to appear in new equipment. Both protocols can benefit from parallel implementation of CRC.

Two generating polynomials are used in the BiSync protocol. They are of degrees 16 and 12, and are for 8- and 6-bit characters, respectively. Both are governed

DATA = HEX 92

$M(x) = x^0 + x^3 + x^6 = x^6 + x^3 + 1$
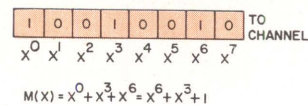
Fig. 1 Least is first. In conventional communication channels, the least significant bit of a binary representation of data is the first one transmitted. Since cyclic codes operate with a division algorithm, this bit is the most significant in the computations that generate the check character before transmittal and detect channel errors after receiving

by the same rules of computation and check, and each polynomial produces two check characters, called jointly a block-check character (BCC), sent immediately following the end-of-text, end-of-block, or intermediate-text-block characters at the end of the message. The polynomials are:

CRC-16 $= G(x) = x^{16} + x^{15} + x^2 + 1$

CRC-12 $= G(x) = x^{12} + x^{11} + x^3 + x^2 + x + 1$

SDLC protocol uses only one generator polynomial:

CRC-16 $= G(x) = x^{16} + x^{12} + x^5 + 1$

The transmitter and the receiver initialize the remainder value to all 1's before CRC accumulation starts. Then the polynomial is multiplied by x^{16} and is divided by $G(x)$. Inserted 0's are not included in the accumulation. Because the generator is of degree 16, the remainder is of degree 15; its complement, called frame check sequence (FCS), is sent after the message with high-order bit first.

Hardware circuits for these three generator polynomials are shown in Fig. 2. Each requires one D flip-flop for each power of x and one exclusive-OR gate for each term in the polynomial. In addition, in the case of SDLC, one inverter is necessary at the input, and, for full-duplex operation, the transmitter and the receiver at one terminal require separate CRC circuits.

New Parallel Implementation

For a given $G(x)$, parallel computation can be faster and cheaper than serial computation. Although, in general, parallel implementation of a function requires more circuits than does serial; in the case of CRC, the increase in the number of *gates* is only marginal (about 14%) and, as commercially available, these reduce to exactly the same number of integrated circuit *packages*. Furthermore, one circuit can be shared for both directions of data movement, as well as for many lines, as noted previously.

(a)

(b)

$G(X) = X^{16} + X^{15} + X^2 + 1$

$G(X) = X^{12} + X^{11} + X^3 + X^2 + X + 1$

$G(X) = X^{16} + X^{12} + X^5 + 1$
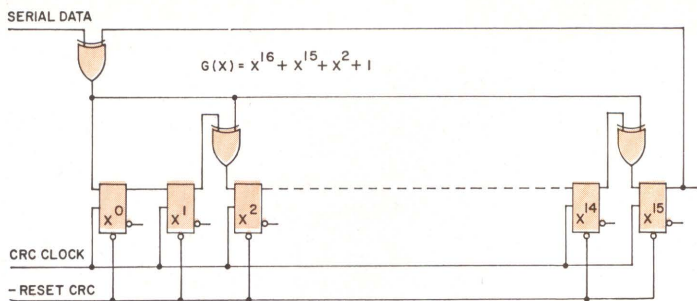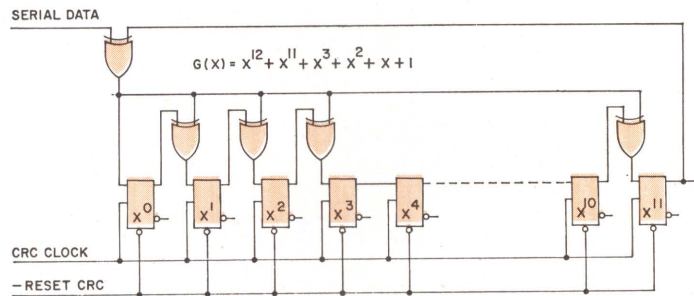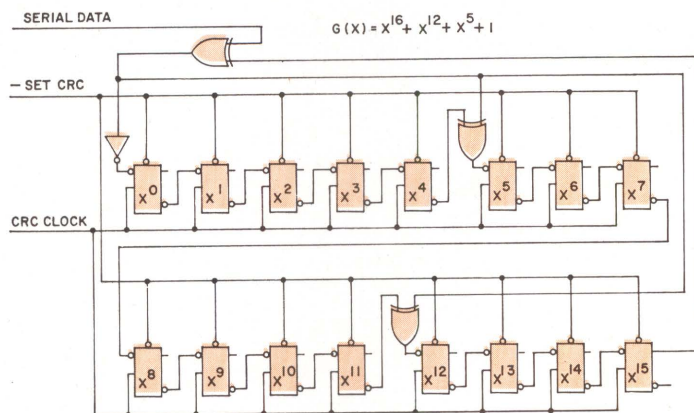
ALL EXCLUSIVE-ORS CAN BE TI 7486, FC 9014, OR MC 1812
ALL D-FLIP FLOPS CAN BE TI 74175
ALL INVERTORS CAN BE TI 7404 OR FC 9016
EVEN PARITY GENERATOR CAN BE TI 74180 OR FC 9348

(c)

Fig. 2 Serial hardware. Most systems compute the cyclic code with feedback shift registers like those shown here. (a) Standard 16-bit BiSync protocol feeds back the register's output to only two of its stages. (b) Slightly more complex pattern is used in 12-bit Bi-Sync, which feeds back to four stages even though the register as a whole is shorter. (c) Growing in use is SDLC, the standard form of which uses this feedback pattern, with one register and an inverter. All these designs, although simple, are expensive and slow in large systems. Suggested component types apply to all schematics in this article

The tradeoff becomes evident in applications where a large number of communication channels are multiplexed. In such systems, the hardware serial computation becomes prohibitively expensive, while relegating the task to software often requires the system to spend 50% of one character-processing time in computing the CRC. In such applications, parallel computation becomes attractive because only one instruction per data character is required, in place of a subroutine which typically contains nine instructions and loops through 50 instruction cycle times each time it is executed.

A given message, when transmitted serially, is not restricted to any particular length, nor is it required to include information about its length at its beginning. Therefore, the CRC computation must always contain the proper check character for whatever part of the message has been transmitted up to any given moment; this interim check character is continuously updated as long as the message keeps coming. This continuous updating is accomplished using the shift register method.

Likewise, a prime requirement of any parallel method is that it continuously update the check character.
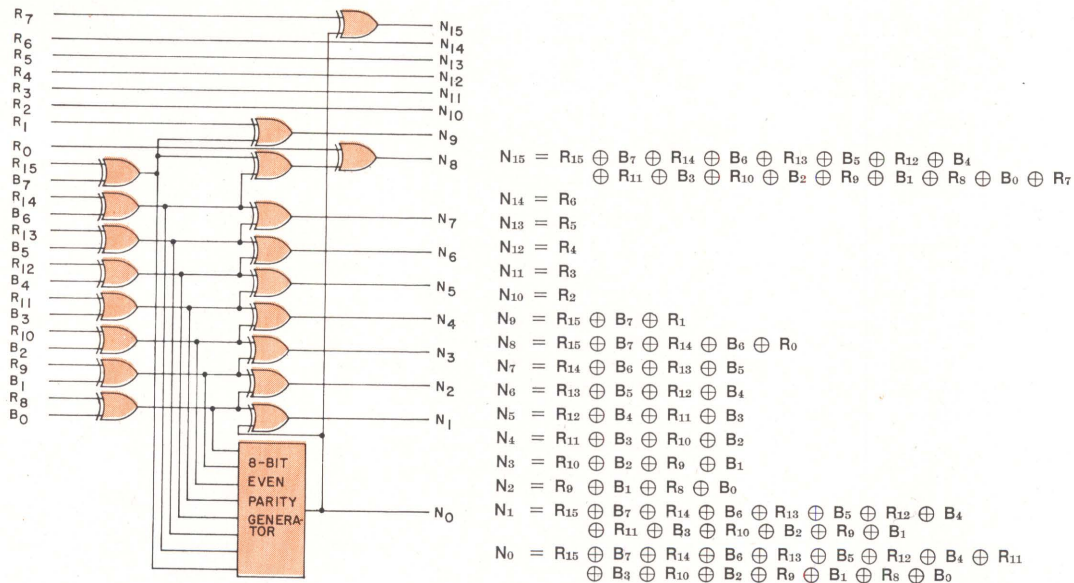
Fig. 3 BiSync 16-bit code in parallel. Standard 16-bit protocol can be checked for errors in transmission more quickly by this logic layout than by the standard feedback shift register [Fig. 2(a)]

$N_{15} = R_{15} \oplus B_7 \oplus R_{14} \oplus B_6 \oplus R_{13} \oplus B_5 \oplus R_{12} \oplus B_4$
$\quad \oplus R_{11} \oplus B_3 \oplus R_{10} \oplus B_2 \oplus R_9 \oplus B_1 \oplus R_8 \oplus B_0 \oplus R_7$

$N_{14} = R_6$

$N_{13} = R_5$

$N_{12} = R_4$

$N_{11} = R_3$

$N_{10} = R_2$

$N_9 = R_{15} \oplus B_7 \oplus R_1$

$N_8 = R_{15} \oplus B_7 \oplus R_{14} \oplus B_6 \oplus R_0$

$N_7 = R_{14} \oplus B_6 \oplus R_{13} \oplus B_5$

$N_6 = R_{13} \oplus B_5 \oplus R_{12} \oplus B_4$

$N_5 = R_{12} \oplus B_4 \oplus R_{11} \oplus B_3$

$N_4 = R_{11} \oplus B_3 \oplus R_{10} \oplus B_2$

$N_3 = R_{10} \oplus B_2 \oplus R_9 \oplus B_1$

$N_2 = R_9 \oplus B_1 \oplus R_8 \oplus B_0$

$N_1 = R_{15} \oplus B_7 \oplus R_{14} \oplus B_6 \oplus R_{13} \oplus B_5 \oplus R_{12} \oplus B_4$
$\quad \oplus R_{11} \oplus B_3 \oplus R_{10} \oplus B_2 \oplus R_9 \oplus B_1$

$N_0 = R_{15} \oplus B_7 \oplus R_{14} \oplus B_6 \oplus R_{13} \oplus B_5 \oplus R_{12} \oplus B_4 \oplus R_{11}$
$\quad \oplus B_3 \oplus R_{10} \oplus B_2 \oplus R_9 \oplus B_1 \oplus R_8 \oplus B_0$

$N_{11} = R_{11} \oplus B_5 \oplus R_{10} \oplus B_4 \oplus R_9 \oplus B_3 \oplus R_8$
$\quad \oplus B_2 \oplus R_7 \oplus B_1 \oplus R_6 \oplus B_0 \oplus R_5$

$N_{10} = R_4$

$N_9 = R_3$

$N_8 = R_{11} \oplus B_5 \oplus R_2$

$N_7 = R_{10} \oplus B_4 \oplus R_1$

$N_6 = R_9 \oplus B_3 \oplus R_0$

$N_5 = R_{11} \oplus B_5 \oplus R_8 \oplus B_2$

$N_4 = R_{11} \oplus B_5 \oplus R_{10} \oplus B_4 \oplus R_7 \oplus B_1$

$N_3 = R_{11} \oplus B_5 \oplus R_{10} \oplus B_4 \oplus R_9 \oplus B_3 \oplus R_6 \oplus B_0$

$N_2 = R_7 \oplus B_1 \oplus R_6 \oplus B_0$

$N_1 = R_{11} \oplus B_5 \oplus R_{10} \oplus B_4 \oplus R_9 \oplus B_3 \oplus R_8$
$\quad \oplus B_2 \oplus R_7 \oplus B_1$

$N_0 = R_{11} \oplus B_5 \oplus R_{10} \oplus B_4 \oplus R_9 \oplus B_3 \oplus R_5$
$\quad \oplus B_2 \oplus R_7 \oplus B_1 \oplus R_6 \oplus B_0$

Fig. 4 BiSync 12-bit code in parallel. Although parallel layout requires a few more individual packages than a shift register does, it can be much less expensive because it is fast enough to be shared by many transmission lines

$$N_{15} = R_{15} \oplus B_7 \oplus R_{11} \oplus B_3 \oplus R_7$$
$$N_{14} = R_{14} \oplus B_6 \oplus R_{10} \oplus B_2 \oplus R_6$$
$$N_{13} = R_{13} \oplus B_5 \oplus R_9 \oplus B_1 \oplus R_5$$
$$N_{12} = R_{15} \oplus R_7 \oplus R_{12} \oplus B_4 \oplus R_8 \oplus B_0 \oplus R_4$$
$$N_{11} = R_{14} \oplus B_6 \oplus R_3$$
$$N_{10} = R_{13} \oplus B_5 \oplus R_2$$
$$N_9 = R_{12} \oplus B_4 \oplus R_1$$
$$N_8 = R_{15} \oplus B_7 \oplus R_{11} \oplus B_3 \oplus R_0$$
$$N_7 = R_{15} \oplus B_7 \oplus R_{14} \oplus B_6 \oplus R_{10} \oplus B_2$$
$$N_6 = R_{14} \oplus B_6 \oplus R_{13} \oplus B_5 \oplus R_9 \oplus B_1$$
$$N_5 = R_{13} \oplus B_5 \oplus R_{12} \oplus B_4 \oplus R_8 \oplus B_0$$
$$N_4 = R_{12} \oplus B_4$$
$$N_3 = R_{15} \oplus B_7 \oplus R_{11} \oplus B_3$$
$$N_2 = R_{14} \oplus B_6 \oplus R_{10} \oplus B_2$$
$$N_1 = R_{13} \oplus B_5 \oplus R_9 \oplus B_1$$
$$N_0 = R_{12} \oplus B_4 \oplus R_8 \oplus B_0$$
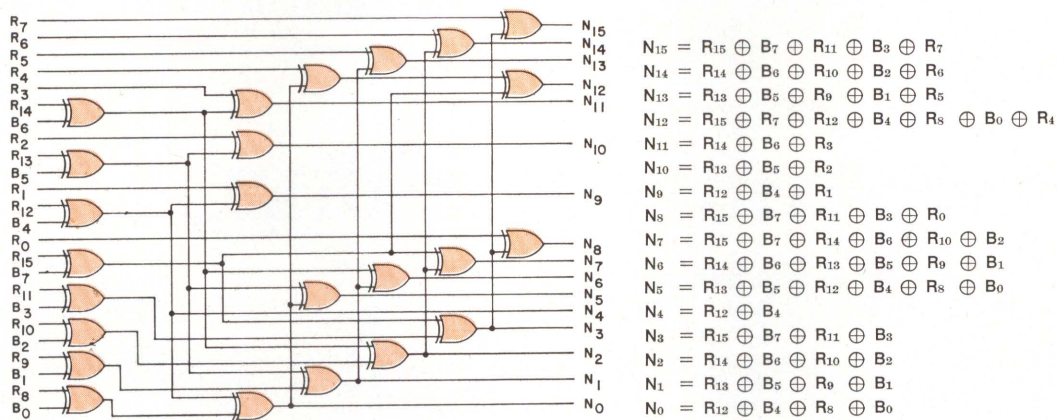
Fig. 5   Parallelism for SDLC. Like parallel computations for other codes, this one accumlates the check character in a much shorter time than is taken to transmit eight bits, so that it can work with several lines

Equations describing the method must therefore show the "old" remainder accumulated to any given point in time, combined with bits of a new character, and generating a "new" remainder. This new remainder becomes the old remainder in the next character cycle; if there is no next character, the accumulated remainder is the check character without further computation or adjustment.

In the equations that meet these requirements for the three protocols cited previously, and a hardware implementation of them (Figs. 3, 4, and 5), the symbols R_0 through R_{15} represent the bits of the old remainder, B_0 through B_7 the bits of a single new character (B_0 is the most significant bit, but the last bit of a character to be transmitted), and N_0 through N_{15} the bits of the new remainder. All operations, indicated by $\oplus$, are the sum modulo 2, or the exclusive-OR.

In BiSync protocol, most nonprinting control characters must be included in the CRC computation. Since most computers transfer data in parallel from one subsystem to another, the serial technique requires either (a) recognition and processing of these control characters on the same hardware component that performs serial-to-parallel or parallel-to-serial conversion, or (b) converting the parallel data back to serial data, within the system, for computing the CRC. Alternative (a) is acceptable only for a very small number of lines, usually four or fewer. Alternative (b) imposes a serious overhead, whether CRC computation is performed by hardware or by system software.

One disadvantage of parallel CRC computation is that once the hardware and/or the instruction is designed for n bits per character, the number of bits in the data block must be a multiple of n. For example, in SDLC, once a parallel CRC is implemented for 8-bit characters, it cannot be used for other character lengths. This disadvantage may not be real, since no one has yet used SDLC with frames that are other than 8-bit multiples in length.

Arun K. Pandeya is a senior development engineer with Interdata Communication Products. He is a graduate of the Indian Institute of Technology in Kanpur, and holds an MSEE from Princeton University and an MBA from Northeastern University.

Thomas J. Cassa is a continuation engineer for Interdata Computer Products. He holds a BEE from the City College of New York.

Memories are

There are two things we'd like you to remember about Ampex cores:

1. UNIBIT™ means absolute uniformity

UNIBIT cores are made by an exclusive Ampex process—they are punched from densified tape by the millions, and the finished product is so uniform that you can't tell the difference between the first core and the millionth core in a given batch.

2. TIN* means temperature independent

Cores made with Ampex temperature-independent material are so insensitive to temperature differences that you get better operating margins over the entire military qualification range, without current compensation (or any other kind of compensation). And only TIN cores permit reliable cross-temperature operation.
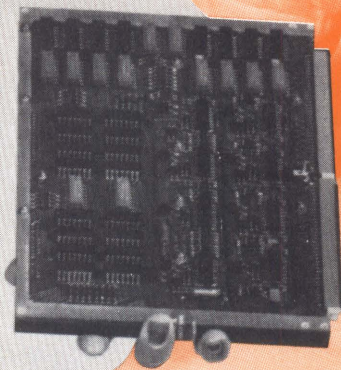
made of these.

Ampex UNIBIT and TIN cores are available as loose cores, as wired stacks, and as complete memory systems. Ampex systems are available in customized and militarized versions, as well as standardized plug-in and add-on modules for the most popular minicomputers.

Remember this: When the chips are down, Ampex core memories keep right on working.

AMPEX

Ampex Memory Products Division
13031 West Jefferson Boulevard
Marina del Rey, California 90291
(213) 821-8933

UNIBIT is an Ampex Trademark
*TIN is a word that Ampex coined to stand for temperature-independent.

93

Smooth Tape Handling
Increases Cassette Drive Reliability

Sidney Davis

Associate Editor

Mechanical simplicity takes many forms; here, in the shape of separate drive motors, standing-start capstans, and reliance on electronic control, it increases the reliability of a cassette drive and extends the life of the tape in the cassettes

In magnetic tape cassette drives, lengthened tape life and increased performance may be achieved by combining electronic capstan control with zero-speed capstan engagement. Reduced magnetic head penetration and elimination of the conventional pressure pad also substantially increase tape life. The mechanical simplicity of the overall system is best judged by its mean time between failures, as supported by field experience.

Possibly the most important requirement made of a cassette-drive tape deck is that it carry out its intended function, accurately and reliably, over its specified service life. Considering the advanced state-of-the-art of today's electronic systems, the principal limitations to achieving required accuracy and reliability are mechanical. Yet it is in the mechanical area that OEM users of peripheral equipment such as tape decks are most deficient.

However, although there is a certain amount of "black magic" in the mechanical design and manufacture of tape decks, the user can go a long way toward obtaining a reliable product by exercising reasonable judgment, and by asking the right questions. An example based on a particular approach to tape deck design illustrates these points.

Although maintaining mechanical simplicity is a common goal when striving for reliable mechanical design, it is not always easy to define. One rough guide is the number of parts, or perhaps the number of moving parts. However, certain parts—clutches and brakes, for example—are far less reliable than others. In spite of some parts' reputation for unreliability, a strong initial awareness of their problems by the designer may lead to the extra margins and testing required to overcome this handicap. This, of course, is a tradeoff for special benefits to be derived from use of the less reliable part.

Probably the best indicator of mechanical simplicity is the mean time between failures (MTBF) for all critical components. Test programs, combined with continuous production sampling, are essential to the determination and maintenance of a satisfactory MTBF.

The process of design simplification is integrally intermeshed with performance requirements. Obviously, the more stringent performance requirements are, the greater the likelihood of failure is, all other factors being equal.
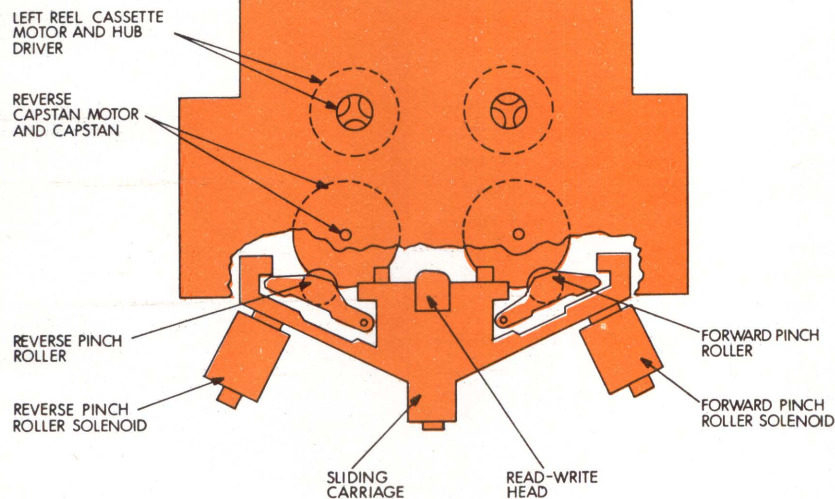
Simple cassette drive design. Four motors, though more complex by some yardsticks than one or two motors, are still more reliable than the mechanical linkages needed when the one or two motors must be connected to both reel shafts and both capstans in a bidirectional tape cassette drive. Head penetration into the cassette, controlled by the sliding carriage, is less than in some other machines, extending head life and improving tape guidance

Thus, performance—as determined by the manufacturer to meet his concept of market requirements—is an important element in tape deck reliability. Consequently, OEM tape deck users should limit performance specifications (with sufficient margins) to realistic needs.

As an example of these points, consider Raymond Engineering, Inc's Raycorder (see diagram). While the manufacturer emphasizes the mechanical simplicity and consequent high reliability of the unit, by many criteria the package is not simple. There are four motors—more than in most tape decks—and two solenoids, generally among the less reliable control components.

Nevertheless, the manufacturer can boast of high reliability, because he

identifies the reliability problem primarily in terms of tape handling without tape damage. Net result is an MTBF of 5000 hr and a system that meets performance requirements over many thousands of tape passes. This is achieved with a capstan drive, and results in exceptionally uniform tape speed, and high and constant data packing density without clock tracks.

Two of the four motors drive the capstans, while the other two control tape tension. During fast forward or reverse operation, only the tension control motors operate. One turns the takeup shaft, which in turn winds the tape inside the cassette; the other maintains tension on the supply reel with a small torque in the opposite direction. This

controlled tension prevents slack loops and tape stretching, and substantially increases tape life and reliability. The capstan motors are stationary.

During reading or writing, one of the two pinch rollers is engaged, depending on the direction of tape motion. The capstan is stationary at the moment of engagement. This avoids the "slamming" start characteristic of cassette drives with continuously rotating capstans (*Computer Design*, Aug 1974, pp 127-138). Capstan acceleration and deceleration are precisely controlled by electronic motor drivers, reducing tape stretching and wear, and eliminating one cause of oxide abrasion and flaking—difficulties found in other cassette drives, which limit tape life to a few hundred passes. Gentle tape handling leads, in addition, to simple tape guiding and less wear on the read/write head.

A properly designed capstan-driven machine may stress the tape less severely than reel-driven types. Capstans distribute drive forces more evenly, and the takeup reel motor's function is to get only the reel, not the entire system, up to speed. Therefore, acceleration forces in the takeup reel are much lighter; their magnitude depends upon the amount of tape on the reel.

There are two drawbacks to the use of standing-start capstans: they reduce tape acceleration compared to that of systems using uniformly but oppositely rotating capstans, and the capstan motors may exhibit the motion irregularities characteristic of conventional dc motors.

Obviously, systems with continuously rotating capstans are faster, since their speed is limited primarily by the response time and impact characteristics of the solenoid, and by possible stretching of tape. However, high tape stresses are inherently present in such systems, indicating a tradeoff of tape life for response time.

When the capstans are driven at a relatively high uniform speed, rotational smoothness is limited only by the precision of the mechanical system; capstan inertia tends to

smooth out most fluctuations. However, for start/stop operation, inertia must be low, so that some irregularities in motor speed may be transmitted to the tape. Fortunately, these irregularities can be minimized by using newer types of dc motors.

In addition, departures from smooth rotation do not necessarily indicate low quality in a digital tape drive. Certain data encoding techniques, such as phase encoding, allow time base instabilities of up to $\pm 25\%$. Therefore, the wow and flutter exhibited even at low speeds may not concern the system designer. Although minimizing the mass in the system may introduce larger instantaneous speed variations, it will also achieve greater capstan control of acceleration and deceleration rates. An optimum acceleration rate, in terms of quick response versus gentle handling, is 250 in./s².

Most tape wear results from motion of the tape across the read/write head. In the Raycorder, such wear is minimized by reducing the depth of head penetration into the cassette, and by omitting the pressure pad in the cassette. Pressure pads compensate for gross variations in dynamic characteristics, such as tape tension, and in static characteristics, such as head penetration. If both static and dynamic parameters can be held sufficiently constant *and* repeatable, the pressure pad may no longer be required. The Raymond drive will operate with cassettes either with or without pressure pads. However, those with pads are more popular and more easily obtainable.

The Raycorder can use cassettes without pads because the drive applies constant forces, and hence maintains constant head-to-tape contact. As a result, it requires less head penetration, with consequent benefits of reduced misguiding and skew caused by the squeegee effect of the pressure pad. Head life is also significantly extended. Head-to-tape contact area, in fact, is only one-third that of conventional cassette drives.

The lighter pressure also decreases wear so substantially that error-free tape life is considerably lengthened. Individual tapes sometimes last for 5000 to 10,000 passes. In addition, the lower friction permits freer, more uniform tape motion, which in turn reduces edge wear on the tape guides. □

Using a Calculator Chip
To Extend a Microprocessor's Capabilities

Patrick H. Stakem

OAO Corporation
Beltsville, Maryland

Microprocessor architectures limited to fixed-point arithmetic can easily be extended to floating-point arithmetic by connecting an inexpensive 4-function calculator chip as a peripheral device to the microprocessor itself

The recent deluge of 8-bit microprocessors on the market provides the logic designer with powerful building blocks for computer systems. Current microprocessors allow for binary fixed-point arithmetic and logical operations on 8-bit data.

Sometimes, however, manipulation of floating-point constants is also desirable, requiring some fairly sophisticated software or hardware to be added; but the hardware already exists in the form of calculator chips. Even the least expensive chips

(available for less than $10) include the four basic mathematical operations on 12-digit decimal data. Although the chip is slower, it provides the microprocessor with a convenient peripheral unit for performing its specialized calculations. The chip can be controlled by the microprocessor, obtaining its data from the microprocessor rather than a keyboard, and supplying data to the microprocessor instead of (or perhaps in addition to) a display.

An alternative is to use a read-only memory (ROM) for floating-point software routines. Although this might be faster than the calculator, it would be more expensive. The calculator chip can be loaded with data and put to work, interrupting the microprocessor when the results are ready.

Basic problem is one of interfacing, ie, enabling the microprocessor and calculator to converse. Details of this process will be unique to each application and to the components selected. The particular

---

Algebraic Versus Polish Notation

Most calculator chips on the market today use one of two general approaches to data entry. One, algebraic notation, calls for data to be entered into the calculator in more or less the same way they are written on paper, so that the problem (2 + 3 = 5) would be worked out by pressing keys 2, +, 3, =, in that order. (Sometimes a calculator has keys += and —=; these are also algebraic, with the convention that the sign of a number is entered after, rather than before, its numerical value, as in conventional handwritten notation.) Among the more widely known algebraic calculators are those manufactured by Texas Instruments.

The other general approach is called reverse Polish notation, devised by Polish mathematician Jan Lukasiewicz. It places the arithmetic operation after, rather than between, the two numbers on which it is executed. It makes parentheses unnecessary and simplifies the design of push-down stacks, which are required in calculators that can "remember" more than one number. Hewlett-Packard calculators use it, as shown by the "enter" key on their keyboards, which indicates the boundary between two successive numeric entries.
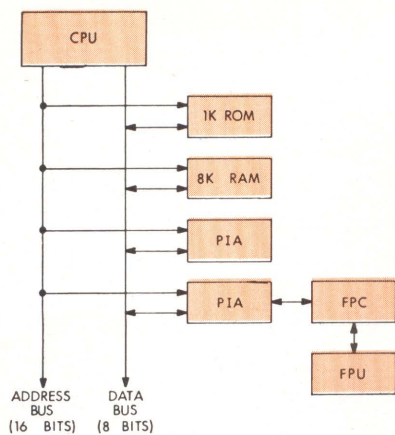
Fig. 1 Microprocessor extension. An ordinary 4-function calculator chip can perform floating-point arithmetic for a nominally fixed-point microprocessor if it is connected as a peripheral unit to the microprocessor

8-Bit Codes in Hexadecimal Notation			
00	number 0	0F	decimal point
01	number 1	10	+ operation
02	number 2	20	− operation
03	number 3	40	x operation
04	number 4	80	÷ operation
05	number 5	FF	clear
06	number 6	F0	=
07	number 7		all other codes invalid
08	number 8		
09	number 9		
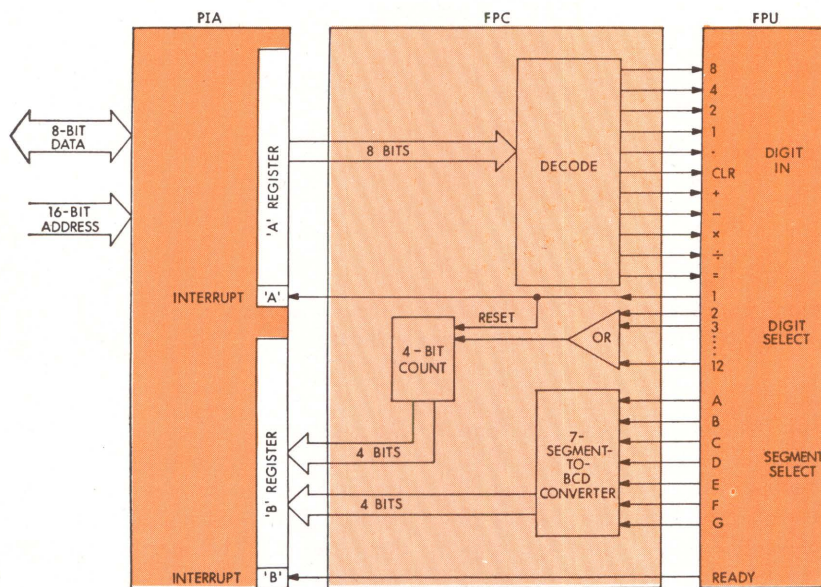
Fig. 2 Floating-point controller. These few simple integrated circuits can provide all interconnections required between a microprocessor's interface adapter and a calculator chip used as a floating-point arithmetic unit

case discussed here involves the Motorola MC6800 microprocessor and a typical 12-digit, 4-function calculator chip that uses algebraic entry (as opposed to reverse Polish notation [RPN], which is used in some calculators).

The microprocessor chip constitutes the system's central processing unit (CPU). The calculator chip is referred to here as the floating-point unit (FPU), while the interface between the FPU and microprocessor is the floating-point controller (FPC). The FPU operates as a peripheral on the main bus (Fig. 1), using interrupts to compensate for the widely differing speeds of calculators and microprocessors; calculator chips, constrained only to human finger speed, typically operate in milliseconds, where the microprocessor operates in microseconds.

In this example, the Motorola MC6820 peripheral interface adapter (PIA) is used as part of the FPC (Fig. 2). Two bidirectional registers are provided by the PIA, one of which is used to supply data to the FPU, the other to read data from the FPU. The interrupt feature of the PIA is used; upon completion of its calculation, the FPU generates an interrupt 'B' to inform the microprocessor that data are available, and another interrupt, 'A,'

when it is ready to accept a digit or an operation code.

Calculator chip input is a string of up to 12 serial binary-coded decimal (BCD) digits, terminated by a load operation. Its output, however, is a 7-segment data format that must be translated to BCD before going to the PIA's input register. Successive steps of the FPU under CPU control are typically as follows. First, the CPU sends the most significant digit of a number to the FPU. When the FPU is ready, the CPU receives an interrupt 'A,' upon which it sends the next digit. This is repeated until the least significant digit and the operator (+, −, x, or ÷) is sent, followed by all of the digits of the second number and the terminator (=) or another operator. Thereafter, the FPC signals "calculation complete, data ready" with an interrupt 'B.' Examples of the coding for these numbers and operators are shown in the Table.

Data format in register 'B,' from FPU to CPU, would be one BCD digit in the four least significant bits, and a BCD digit count in the upper four bits. The digit count, derived from the digit-select lines of the calculator output, tells the CPU where to store the particular digit of the result—two digits in each location of the 8-bit-wide memory under control of a software subroutine. Meanwhile, the FPU keeps the results of the calculation until cleared by the CPU.

For many applications, a calculator chip can serve as a quick and easy approach to performing floating-point calculations in a microprocessor system. It is less complex than software stored in a ROM, and can overlap its processing with that of the CPU, reducing execution time of some CPU programs. □

Adversary Analysis: Computerized Testing of Computers

William S. Holderby

Planning Research Corporation*
Kennedy Space Center, Florida

Just as diverse manufacturers apply computers to test their outputs, so can computer and peripheral designers, installers, and users apply them

Adversary computer analysis is the technique of testing one computer or computer system against another to aid in design or in fault detection. This form of analysis is applicable in many areas of today's expanding computer market. It extends to computers the same advantages of computerized testing that have already been widely recognized in manufacturing areas as diverse as automobiles and integrated circuits—instantaneously analyzing failures and detecting intermittent breakdowns. In addition, the method enables highly intricate devices to be produced with fewer customer-experienced failures and lower testing costs.

Two examples of applied adversary technique are in testing intelligent terminals without human intervention, and in assisting design and checkout of a complex minicomputer system.

Testing a Smart Terminal

Intelligent terminals are defined, for the purposes of this article, as man-machine interfaces. Through these interfaces, the operator changes data stored in the terminal, displays these data, and communicates with a computer system—all under microprocessor control. The terminals present a manufacturing problem in environmental testing or searching for long-term cyclic failures. Such testing is constrained when only a limited number of personnel can do it, and by environmental problems imposed by the need for special equipment, such as vibration tables, altitude chambers, or heat rooms. These problems seriously limit the number of terminals that can be tested at one time.

The adversary technique can circumvent human operator interfacing. It pits a minicomputer against a microcomputer to provide dynamic testing, which enables the manufacturer to determine the reliability and integrity of each terminal before it is shipped.

An adversary system assumes both the role of the operator and that of the computer system testing the terminals. This system (Fig. 1) consists of a 16-bit bus-oriented minicomputer, a serial-to-parallel bidirectional bus interface, and a keyboard simulator. Most keyboards used in manufacturing terminals are standard "off-the-shelf" units which

interface with an internal module through an integral connector. Through this same connector, a keyboard simulator is attached to test the terminal. The electrical connection between keyboard simulator and internal interface consists of a 6- or 8-bit parallel data bus and a single data strobe, which signals the terminal that data are on the bus and stabilized.

The keyboard simulator (Fig. 2) consists of a 16-bit address recognizer, and two 8-bit data interfaces that connect to the adversary system's address and data bus. Data bits D0 through D7 are latched and presented as an address of a programmable read-only memory (p/ROM), which in turn decodes this address and strobes the specific terminal defined by the adversary software. The adversary data interface is connected to data bits D8 through D15 of the adversary data word. This interface presents the data to a 6-bit data latch which gates the information onto a parallel data bus connected

to all terminals. Timing and control circuitry is driven by the adversary address recognizer, providing system bus recognition for the simulator.

The bidirectional serial-to-parallel converter provides a high speed serial data link between terminal and adversary system, which is used by the terminal to transmit and receive data previously stored in the larger computer's data base. Data received through this interface are checked against known data; erroneous information is flagged and printed out for the adversary system's operator.

Software for this system executes a series of cyclic operations:

(1) Load the terminal's data storage through the keyboard simulator.

(2) Perform functional changes on these data, also through the keyboard simulator.

(3) Initiate serial transmission from terminal to adversary system.

(4) Search for errors in the incoming serial data, by checking against a predefined data base.

(5) Repeat the sequence.

By repeatedly cycling the terminals, two months of full-time operation are simulated during every 24 hours of testing under environmental extremes. This is usually long enough to determine the infant mortality rate for the terminals under test. Since this testing does not require human intervention at the terminal, it may be carried out in environmental test chambers and in racks where inconvenience dictates automatic testing.

Testing a Dedicated Mini

The second example deals with test and checkout of a minicomputer system that contains system software written for specific user applications. This type of system is frequently used in today's computer graphics facilities, and in automated newsrooms and banks. Their manufacturers cannot produce a standard product because different parts of their market impose widely varying requirements. Since the specific application software usually requires a great deal more checkout time than is possible before the system must be shipped to the customer, systems are often installed and operating for six months or so before software problems are completely solved—leading
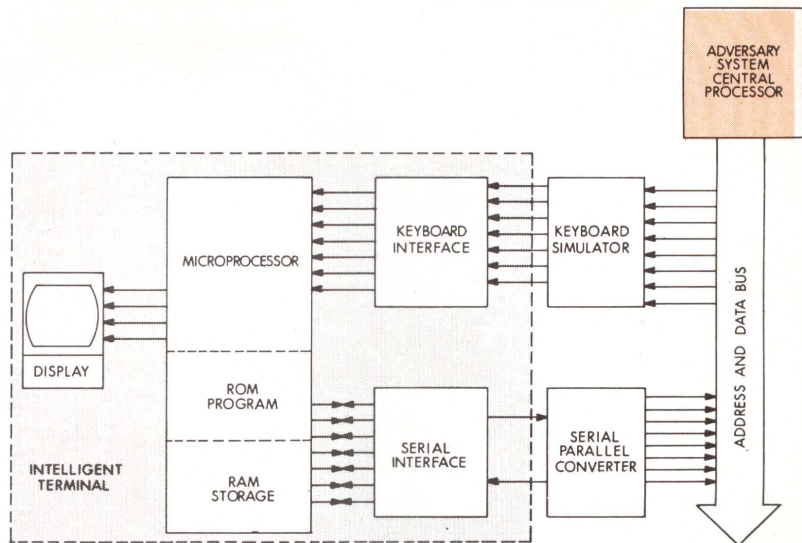
Fig. 1 Adversary interrogation of an intelligent terminal. A 16-bit bus-oriented computer system is connected to a microprocessor-controlled terminal through a keyboard simulator and bidirectional serial-to-parallel interface. This configuration can be extended to as many terminals as desired by busing the outputs of the keyboard simulator and multiplexing the serial data link
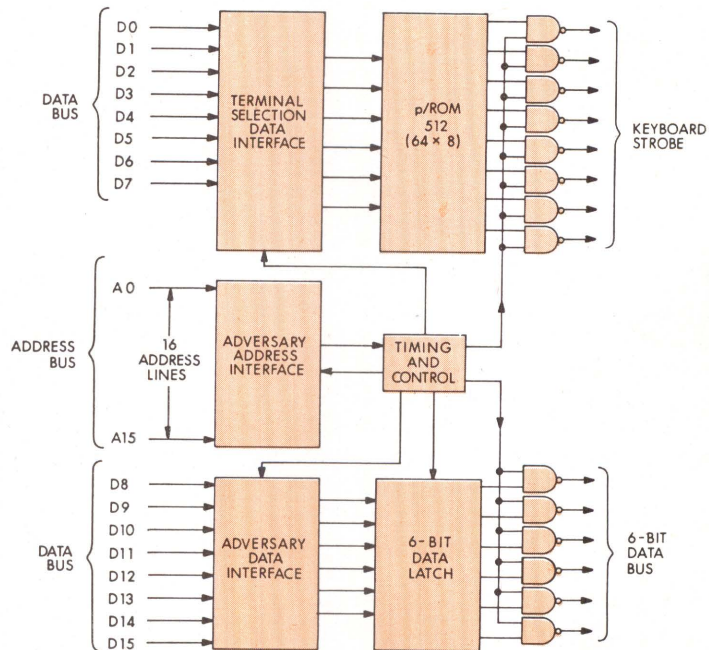
Fig. 2 Keyboard simulator. The simulator interfaces to the adversary system's address and data bus. One data byte is loaded by software with the terminal reference number; the other contains data for the terminal's internal keyboard interface. These data are latched and gated to a 6-bit data bus which interconnects all terminals under test. The keyboard strobe is gated only to the terminal which is to receive the data on the data bus; the terminal's address is determined by the programmable read-only memory, whose own address is specified by software

to considerable customer dissatisfaction. Many system software problems that are encountered after the system is installed can be avoided by using an adversary system.

Most special application systems consist of a central processor unit (CPU) that controls a data base and directs the routing of data between peripherals. Through peripheral man-machine interfaces, operators load new data and direct CPU operation. Such systems may have 10 to 30 such peripherals attached. These systems have extreme software requirements, and often do not work at top efficiency, because of the problems associated with trying to test under conditions that approximate normal customer operations. Such conditions are the design objectives to which the systems were built and may be considered worst-case for testing purposes.

A computerized test system may be constructed and programmed to simulate this worst-case condition (Fig. 3). Such a system acts as an adversary to the primary system under test, and exercises the primary through simulated interfaces.

Most systems employ serial data communication between peripherals and CPU—a relatively simple matter to devise, requiring little unique hardware design. On the other hand, parallel interfacing requires a bidirectional buffer, such as the keyboard interface in Fig. 2. This buffer must appear to the primary system exactly as a peripheral in both hardware and software capacity. In special instances where the hardware design cost becomes too extreme, the keyboard interface itself could be used directly, so that the adversary system interfaces directly through the primary's peripheral instead of bypassing and simulating it.

The adversary system must provide the proper simulated interfaces and the basic utility peripherals, including a man-machine peripheral, mass storage devices, and a permanently recording output device. With these additional peripherals, software personnel can control the adversary system and maintain a record of proven performance while a system is under test.

Adversary Software

The software design effort demands a great deal more preparation than the hardware (Fig. 4). Basic format
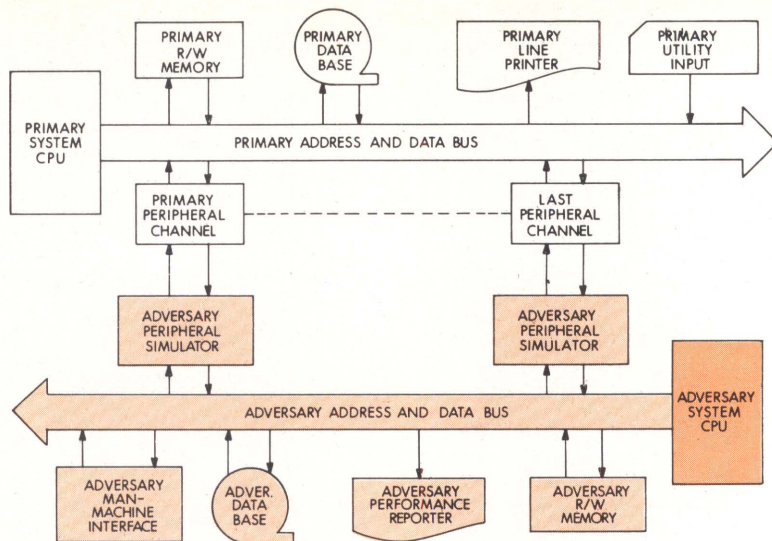
Fig. 3 Primary and adversary hardware interface. Interconnections between the two systems are through serial or parallel peripheral interfaces. The adversary must simulate the primary's peripheral to interrogate the latter system's software. These simulators are under adversary software control
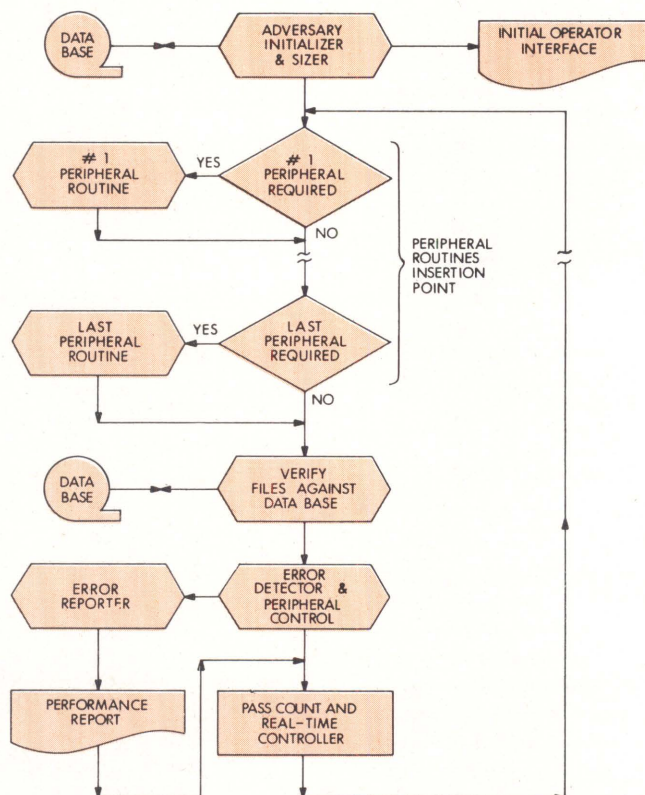
Fig. 4 Adversary system software. This real-time software determines its environment from the operator, then begins interrogating its peripheral simulators. After servicing all simulators, it tests incoming data against a known data base. Any detected errors are reported to the operator. The process is reiterated under real-time constraints imposed by the user

of the adversary's main program consists of a series of subroutine calls that correspond to the quantity and types of peripherals attached to the system. To determine the routines required, the main program begins by requesting from the human operator information upon which the software constructs itself dynamically in a variable environment. With this dynamic construction, the system and its software can test all similar systems regardless of configuration.

Next, the main program initiates real-time counters, or programmable interrupts, and a communication sequence between all peripheral simulation drivers. This requires a special log-in sequence, entered in the normal initial access as if by an operator. Then the main program begins a series of subroutine calls to the peripheral simulation drivers, which cause the peripheral simulators to imitate the primary system's peripherals. There are as many peripheral driver routines as there are types of peripherals being simulated.

Upon activating the last peripheral simulator, the main program verifies any information received from the test system against known-correct information in the adversary's data base. If no errors are detected, the main program determines its real-time position and recycles through the routines.

Real-time control of this loop is the most difficult portion of the main program because the various performance times of the simulated peripherals must be matched. If a peripheral is simulated at a speed exceeding its real performance time, the system under test begins to degrade its response times and the test eventually aborts. Therefore, extreme care must be exercised in the design of this real-time controller.

In addition, the controller must be able to vary real-time performance upon request. This ability provides the programmer with varying levels of activity to test his system software modules, and is extremely beneficial when performance time and efficiency are being tested.

Various peripheral simulator modules utilize the same data base, thus conserving the large portions of memory that would be needed to contain several data bases, with useless redundancy. Each module appends different unique file titles

to the same data, and uses the proper communication codes required by the primary system. With this modularized construction, more than one programmer can work on the adversary software with a minimum of conflicts, while the individuals who know the most about the performance capabilities of the test system software continue to be the programmers who wrote that software.

Coping with Recurrent Chores

Three utility routines are necessary to handle various repetitive tasks that occur while the adversary is operating.

• *Initial Operator Interface* is a utility program that determines the size of the system and the number of the various types of peripherals to be interfaced. It configures the main program from mass storage with the necessary peripheral simulation subroutines. Information is gathered on the real-time performance that is expected from the adversary system, giving the operator the option of establishing the performance that he requires from his software.

• *Error Detector* module verifies data received from the various peripheral simulators by comparing it with the common data base, and reports any deviations to an error reporter module.

• *Error Reporter* documents those errors detected in the main program. It must determine whether the failure is so extensive that the test should be aborted and the system returned to the operator for further instructions, or whether the error should be reported and testing continued. In addition, it maintains a detailed record of all errors and the peripheral activity which led to their detection. After a period of time, determined previously by the operator, it prints a performance report.

Certain economic trade-offs must be weighed carefully before an adversary system is designed and programmed. These include probable extent of future software development, unique interfacing problems that may be encountered, availability of a separate system or test set that can perform in an adversary capacity, and availability of the personnel necessary to construct and program such a system.

Another consideration is the support of field service operations at the customer's facility which require a partial or total shutdown of his operation—whether a failure is in a small terminal or involves the complete system. An adversary system can be designed to support field service operations as well as development work. It requires the use of modems and the telephone network. The adversary system, once connected to a modem, can assist field service personnel in several ways. For example, it can provide an alternative system to interface peripherals for troubleshooting purposes, diagnose trouble by interfacing directly with the customer's system, quickly reload the customer's system software, and gather information for the manufacturer on software problems that are plaguing the customer.

This form of support can rapidly solve on-site problems, and yield design-flaw information to the manufacturer.

Conclusions

The adversary technique offers a reasonable solution to many problems which face computer systems manufacturers. When applied to the manufacturing testing of intelligent terminals, the adversary technique provides for unassisted, rapid, and thorough fault analysis. This form of testing lends itself well to production facilities by affording the manufacturer the opportunity to mass-test terminals. When system-to-system testing is applied, it provides system designers with real-time activity simulation, which points out software flaws not always apparent under normal testing, and permits system programmers to optimize the software to increase efficiency.

On-site problems and software flaws may be more rapidly eliminated by allowing field service people to recreate the conditions that led to their discovery, and enabling them to more rapidly diagnose and repair systems problems. Such online servicing capability leads to better customer relations.

Depending on individual economic trade-offs in hardware and software design costs, adversary analysis adds a badly needed new dimension to automatic system testing. □

Eliminating Glitches From One-Shots in Logic Systems

John Carroll

Analog Devices, Incorporated
Modular Instrumentation Division
Norwood, Massachusetts

Here is a method for inhibiting extraneous output pulses from a logic circuit used in equipment for testing isolation amplifiers. The technique is broad enough, however, to be applied to many circuits which employ one-shots

In logic systems, one-shots are often used for such tasks as detecting the beginning or end of a state and generating a short pulse to initiate the next step in a sequence, or operating only once on the first closure of a switch to mask contact bounce. System logic sometimes necessitates inhibiting operation of the one-shot, so that it will trigger only if specific conditions are satisfied. In this case, extra output pulses—even very short ones—can cause the system to malfunction. The inhibiting action must be absolute and inviolable.

A clear line on a one-shot that allows the output to change states momentarily on a trigger condition does not serve the purpose. Neither does trigger-gating logic that fires the one-shot as soon as the inhibit is removed.

To prevent one-shots such as the 74122 or 74123—when triggered while in the cleared state—from generating short, spurious output pulses, an obvious solution is to connect the $\overline{\text{CLEAR}}$ input to one of the gate inputs. Although this works, it causes the one-shot to fire when the $\overline{\text{CLEAR}}$ line
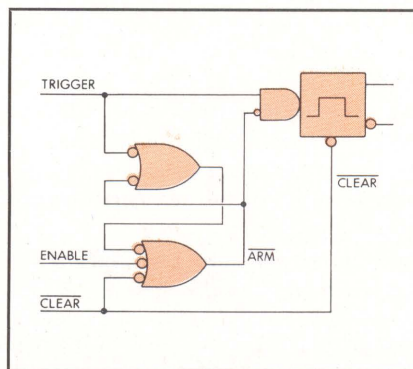
is released, if the remaining inputs happen to be activated. The spurious pulse occurs when the clear condition ends, and lasts for the full time-duration of the one-shot. This only compounds the original problem. A better solution is to connect the one-shot for enabled edge-triggering.

The $\overline{\text{CLEAR}}$ line in the diagram is connected to clear the latch and disarm the one-shot. Before the latch can be set again, the trigger must fall to logic "0" while the clear signal is absent. Extra inputs may be added to the $\overline{\text{CLEAR}}$ side of the latch, to act as trigger edge enables.

In a clocked system, a race condition may arise. If the state of the TRIGGER line changes on the same clock edge as $\overline{\text{CLEAR}}$ or ENABLE, the one-shot may or may not fire, depending on differences in logic delays from the clock to the various inputs. In this case, the designer should analyze these delays, and, if the signals arrive in the wrong order for the application, or there is doubt, extra delays can be added as needed. Such noninverting gates as the 7408, 7411, 7417, 7421, or 7432 are useful for this purpose. □

Computer Design magazine announces CompDesign 76, a unique, new national supermarket of OEM products, services and information.

CompDesign 76 is a series of OEM product supermarkets that will appear in five cities across the country in conjunction with The 1976 Computer Caravan. Adapting the proven success formula of The Computer Caravan and sharing its facilities, CompDesign 76 will be a self-contained show with Designer Forums, Product Seminars and a complete Exhibition of the latest products and services in The OEM market. It will bring thousands of OEM buyers and sellers together in a unique, information-oriented atmosphere designed for serious business. And it will cover key markets across the country.

Here's the schedule:

Boston	March 2-4, 1976
New York	March 9-11
Chicago	April 13-15
Los Angeles	May 4-6
San Francisco	May 11-13

As a user of OEM products and services, you'll find CompDesign 76 to be the most efficient way possible to get detailed information on the latest developments in the industry. You'll exchange information with your peers at our Designer Forums, gather details at exhibitor product seminars, and compare equipment from a variety of companies on our exhibit floor. We'll be sending you complete details and registration forms well in advance of the show.

As an OEM marketer, you'll find that it's surprisingly easy to become an exhibitor in CompDesign 76, because our show manager, The Conference Company, does much of the work for you. They provide a standard booth or display stand, furniture, set-up and tear-down, transportation from city to city, help with your product seminars, all registration procedures — and much more. So it's possible for even the smallest companies to join with industry leaders in effective presentation of their products and services to the industry's decision makers. And the cost can be quite reasonable.

If you'd like more details on exhibiting in CompDesign 76, we'd like to send them to you. Just send in the coupon below. It could be your first step towards a very good new year.

COMPDESIGN/76

Sponsored by **COMPUTER DESIGN**

Managed by The Conference Company
A division of Computerworld, Inc.

Faster Microprocessor Module Available For Industrial Control

Although built around the 4-bit Intel 4040 microprocessor, as were earlier Comstar System 4 CPU modules, the 4B operates at a 7-μs cycle time, 35% faster than the 10.8 μs of the standard 4040. The System 4B, like its predecessors, is designed for industrial control applications and is available both as a module and in a system including 1K-word x 8-bit p/ROM, 1-kilobit RAM, portable front-panel analyzer, and 32-channel digital I/O module.
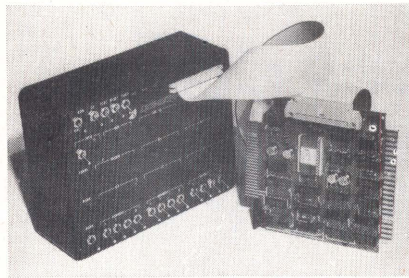
An interrupt control module provides 12 channels of priority interrupt, switch-selectable real-time interrupt, power fail detect, auto restart, and watchdog timer. The front-panel analyzer allows online control and program diagnostic capability.

Manufactured by The Warner & Swasey Co, 30300 Solon Industrial Pkwy, Solon, OH 44139, System 4B interconnects via a data/control bus to p/ROM and RAM modules as well as all of the Comstar 4 family of interface modules and peripherals. These include digital and power switching I/O modules, analog I/O communications interface modules, displays, card and paper tape equipment, CRT displays, magnetic tape, and discs. Operating temperature range is −40 to 80° C.

Circle 170 on Inquiry Card

Peripherals Interface Analog Signals With µComputer System

Printed-circuit-card-mounted analog peripherals, electrically and mechanically compatible with Intel's Intellec[R] 8 microcomputer system, interface analog signals with digital systems. Functionally, they provide analog data acquisition and analog output. A 5 V to ±15 V dc-dc converter on each card permits use with the Intellec's 5-Vdc power supply.

Two analog data acquisition systems are available: the MP8208, for 8-channel differential input; and the MP8216, for 16-channel single-ended input. These systems include input analog multiplexers, instrumentation amplifier, sample/hold amplifier, and 12-bit A-D converter, as well as all necessary timing, decoding, and control logic. Operating temperature range is 0 to 70° C.

The data acquisition systems send a wait request to the CPU during
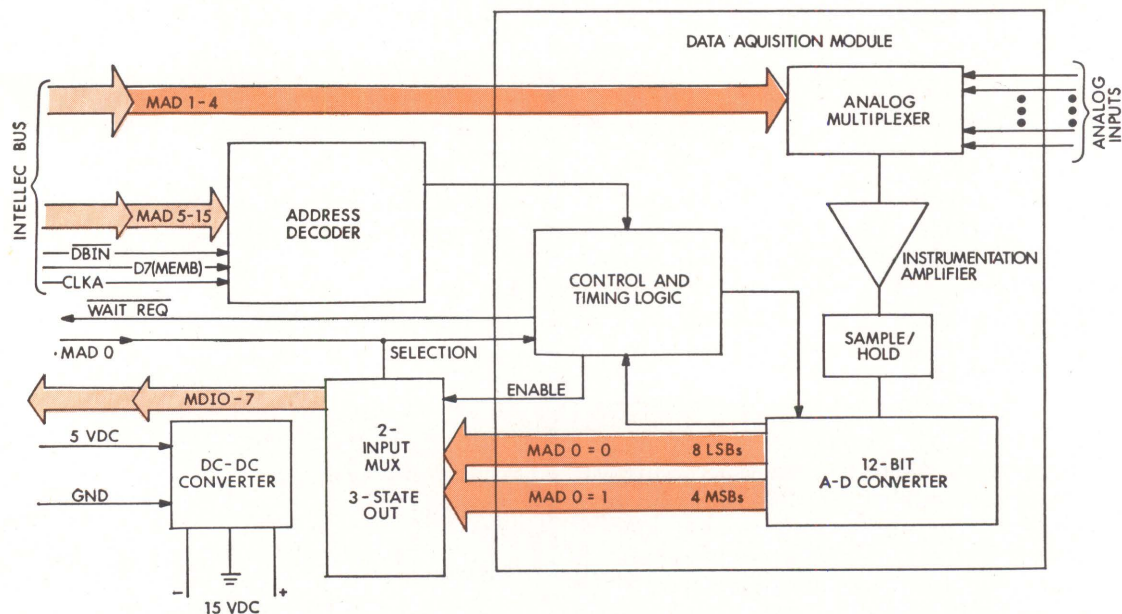
Analog data acquisition system. Conversion of analog inputs to digital outputs starts when MAD 5 through MAD 15 from Intellec bus equals the hardwired address, DBIN and MEMR signals are present, and MAD 0 = 0 (even address). Analog input channel is selected by MAD 1 through MAD 4. Output data bits are read into MDI 0 through MDI 7 (eight LSBs when conversion is complete, followed by four MSBs when MAD 0 = 1.)

NEW 5V/30A SWITCHER FROM ACDC

VOLTS	AMPS	MODEL NO.	PRICE*
5	30	JP5N30	$265
5	60	JP5N60	$436
5	100	JP5N100	$535
5	150	JP5N150	$765
5/±12	50/5	JT301	$491
5/±15	50/4	JT302	$491

*100 piece quantity

This mini-switcher is the newest addition to ACDC's 5 volt power supply line. It operates from a selectable input of 115/230 VAC, 47-63 Hz or 48-60 VDC. Like most power supplies, it's rated for full output at 40°C, but will also deliver over 83% of rated output at 50°C without internal fans or forced air cooling.

THE MOST DEPENDABLE SWITCHERS ON THE MARKET, AND YOU CAN PROVE IT

Just ask for an evaluation unit and put it through its paces…at your plant …under your own supervised test conditions. ACDC switchers will work better, longer and more dependably than any other switcher you can buy.

HOW CAN WE BE SO SURE?

Switchers are complicated devices…tricky, temperamental and tough to build, but we've been building them for over six years and have eliminated all the major problems.

We start with a proven electrical design, proper derating of quality domestic components and rigid, comprehensive, in-process controls. All semiconductors, the most common cause of switcher

failure, are thermally shocked for three cycles from 0°C to 100°C, followed by a 48-hour bake at 150°C. A thorough electrical test eliminates marginal devices and isolates potential failures due to thermal stress and infant mortality.

A second phase of testing occurs after final assembly. Each power supply is subjected to a no load/full load burn-in at elevated temperatures for a minimum of 24 hours, then put through another test cycle before it gets an inspector's stamp of approval.

ACDC switchers are designed to work when you get them and built to last so you can depend on them.

A WIDE RANGE OF POWER SUPPLIES SOLD AND SERVICED INTERNATIONALLY

In addition to these 5 volt switchers, ACDC also offers 12, 15, 20 and 24 volt switchers rated at 150, 300, and 500 watts. These switchers and 200 other conventional power supplies are available from stock and serviced at eighteen service centers throughout the world. The complete line is detailed in our new 72-page catalog. Write for it. It's free.

EMERSON®
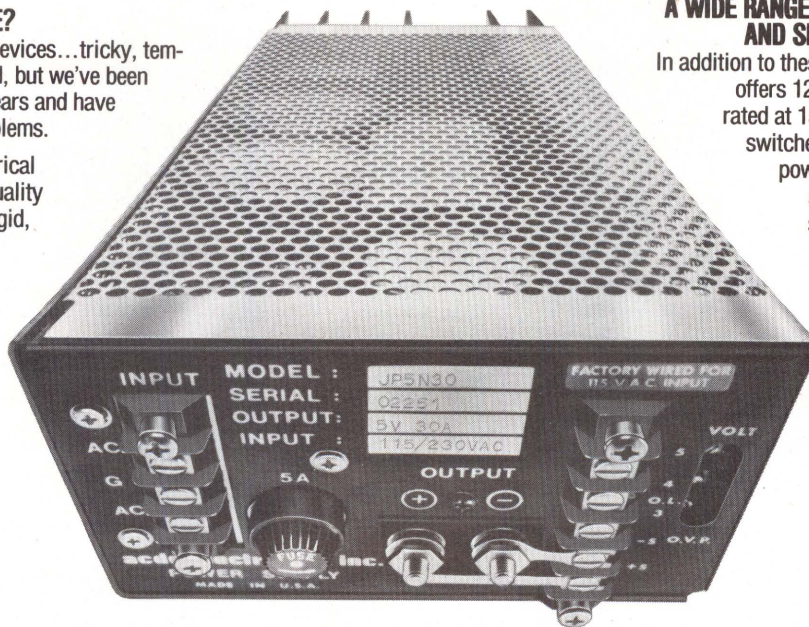
acdc electronics

401 Jones Road Oceanside, California 92054 (714) 757-1880
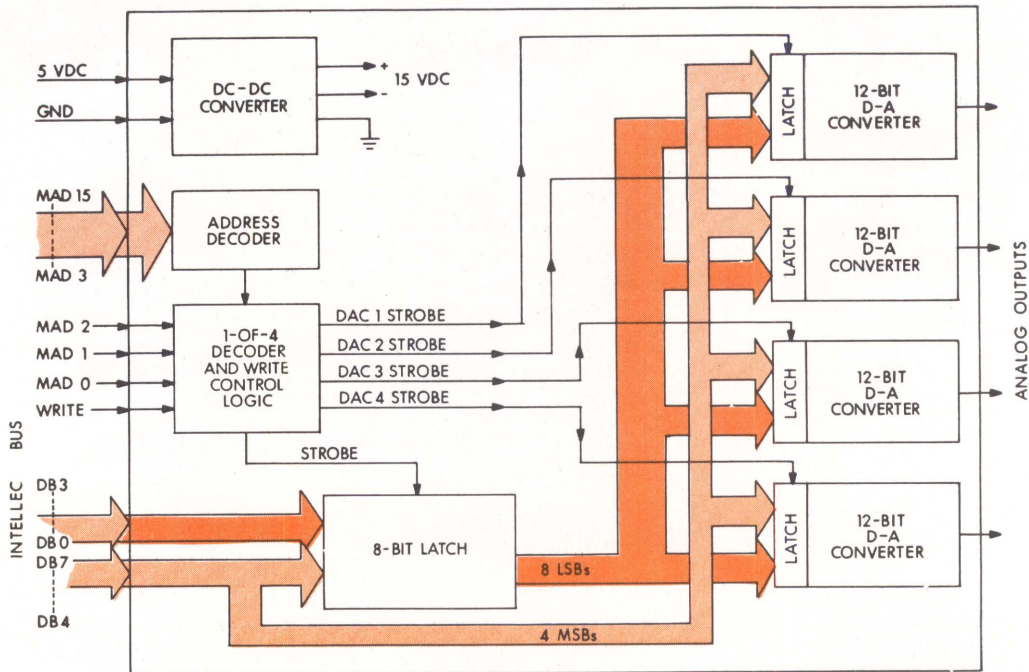
Analog output system. A new data word is strobed to a D-A converter input register when MAD 3 through MAD 15 equals the hardwired address, a write signal is present, and MAD 0 = 1. Analog output channel is selected by MAD 1 and MAD 2, input data bits are read by DB0 through DB7, both via the Intellec bus

conversion (20 μs), holding it until the 12-bit output is ready. All possible timing sequences have been considered to prevent illegal triggering during conversion. Acceptable input voltage ranges are ±10 V, 0 to 10 V, ±2.5 V, and 0 to 5 V. Maximum throughput accuracy is ±0.025% full scale range (FSR); temperature coefficient of accuracy is ±0.002% FSR/°C.

Four 12-bit D-A converters on the MP8104 analog output system card provide individually-controlled outputs. Transients caused by uneven data transfer are minimized by input buffers and other registers which permit simultaneous transfer of all 12 data bits to the D-A converter's input buffer. Output voltage ranges of ±10 V, 0 to 10 V, ±15 V, 0 to 5 V, and ±2.5 V (at 5 mA) are strap selectable. Output settling time is <10 μs for a full scale output change and output impedance is 1 Ω. Temperature coefficient of accuracy is ±0.003% FSR/°C unipolar, ±0.0045% bipolar.

All of the analog peripherals, made by Burr-Brown Research Corp, International Airport Industrial Park, Tucson, AZ 85734, are treated as memory locations by the microcomputer, and may be plugged into any memory or I/O slot of the Intellec 8. Only one load instruction is required (when using the mod 80) to read a 12-bit data word from the data acquisition system, or to transfer a 12-bit data word to the analog output system.
Circle 171 on Inquiry Card

Microcomputer Software Design Aids Available On Time-Share Networks

Software design aids for Motorola's M6800 microcomputer-based systems are now available at key locations within the U. S. and parts of Canada through the United Computing Systems, Inc Network, and at major locations throughout the world on the General Electric Information Services International Network. Software components available on the networks are MPCASM—cross-assembler, converts symbolic source code to machine-language, with listing; MPSSIM—interactive simulation, duplicates the execution of machine-language instructions assembled with the MPCASM cross-assembler; HELP—a program that provides real-time documentation of the software, including abbreviated operating procedures; and MPBVM—a "build virtual-machine" program that simplifies file management problems associated with developing microprocessor programs. The packages are also available via the Motorola Timeshare Service. Information may be obtained from the Technical Information Center, Motorola Inc, Semiconductor Products Div, PO Box 20924, Phoenix, AZ 85036.
Circle 172 on Inquiry Card

Even if you don't use our new ¼-inch data cartridge now, you'll be glad it's there.

Because, no matter what, you've always got Information Terminals Corporation as a source of supply. ☐ And there are good reasons why you'll want to make us your primary source! ☐ ITC produces, by far, the majority of data cassettes in use today. So you can depend on us to know what we're doing. ☐ Then, we've added a few touches of our own to the ¼-inch cartridge: reduced skew and bit jitter; trouble-free running up to 90 ips; improved guiding system; extended cartridge life.

☐ And every cartridge is certified 100% error free after assembly.... an exclusive feature of all ITC computer grade media. ☐ For more about ITC's new TC2000 ¼-inch data cartridge, call Scott Cochran, National Sales Manager.

Information Terminals Corporation
323 Soquel Way
Sunnyvale, California 94086
Telephone: (408) 245-4400
TWX: (910) 339-9381

CIRCLE 57 ON INQUIRY CARD

Microprogrammable Computer-on-a-Board Has 200-ns Cycle Time

Building-block, I/O-oriented architecture of the 200NS microcomputer is designed to reduce system cost, interfacing, and development time. According to the manufacturer, Wintex Computer Corp, 544 Lunt Ave, Schaumburg, IL 60172, capability of the microprogrammable computer-on-a-board's I/O structure to accommodate any hardware element simplifies interfacing to the computer. Interfacing software and firmware can be tailored to users' needs. The 8-bit, bipolar, databyte-oriented machine uses 16-bit instructions.

Basic features include 200-ns instruction cycle time, 16-level priority vectored interrupts, 16-level stack for interrupt and subroutine returns, and 16 general-purpose registers divided into two blocks for independent foreground and background processing. Up to 16K 16-bit words of control store and 65K 8-bit words of external memory can be addressed; as many as 256 I/O devices can be directly addressed through a bidirectional 8-bit bus.

Various types of memory—ROM, RAM, or p/ROM—can be provided due to asynchronous operation. Interface for the 2102 static RAM is available on a separate board. A simulator, connected to the computer by a flat ribbon cable, is available for checking out firmware before programming the p/ROMs.

Firmware building blocks that can be used in various systems permit the user to concern himself only with writing the application software peculiar to his need. These blocks include multiprogramming executive, macroassembly language interpreter, I/O control system, and disc file management. For program development, the user can write, simulate, and debug programs on a microprogramming development package.

Peripherals can be supplied as blocks consisting of hardware interface, peripheral device, firmware/software, diagnostics, documentation, and test procedure. Interfaces are included for moving-head disc drive, dual floppy-disc controller, CRT display, 110-char/s printer and full ASCII keyboard with cursor control keys, and synchronous or asynchronous bit or byte RS-232-C devices.

Control section of the machine consists of a 16-bit instruction register, 14-bit program counter, 16-level stack, dual 1-bit condition code and 1-bit state register, oscillator, and timing circuitry. Each location on an associated control store—a bipolar ROM with <90-ns access time—contains one 16-bit microinstruction. In minimum configuration, control store is made up of four 256 x 4 p/ROMs; up to 16 p/ROMs can be included.

Wintex Computer Corp's 200NS microcomputer is fabricated on a single 11 x 18" PC board. Basic elements are control section, data handler, local memory, interrupt handler, I/O bus interface, and 1K words of control store

Circle 173 on Inquiry Card

µProcessor Attains 60% Power Reduction in Digital Data Repeaters

Low power consumption, a prime consideration for military applications, has led to the inclusion of a microprocessor in a system for retransmitting digital radio messages. Use of the microprocessor provides capabilities approaching those of a minicomputer at a fraction of the cost and power consumption, according to Collins Radio Corp, the system developer. The battery-operated repeating stations—including receiver interface, microprocessor, 2000 words each of RAM and ROM, and teletypewriter interface—function on less than 5 W.

To prevent a message from being retransmitted in the wrong direction by one of several repeaters which might intercept it, each message carries a header that identifies both its destination and the repeater which should retransmit it. The initiating transmitter listens for the retransmission as acknowledgement that the message has been properly processed. In this unit, software routines identify the message and routing and perform other operations according to flags in the header.

Choice of an IMP-16 microprocessor, made by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, resulted from its 16-bit word length and software capabilities. The large word length reduces the number of steps required for processing operations.

Several design steps were taken to reduce power requirements of the microprocessor from its normal 15 to 20 W. Clock rate was reduced from a standard of 175 ns to 500 ns, permissible because of the large word length. In addition, the microprocessor's central processing unit (CPU)—which accounts for 3 to 3.5 W of power—is turned off by a software program during inoperative periods. The program is flagged to turn off the processor after a specific time interval. A second flag checks the system to be certain that the CPU is not being turned off in the middle of an operation, and sets a memory address to receive the next block of transmissions. New incoming transmission triggers the program to turn the CPU back on. Overall, power is reduced by 60%.
Circle 174 on Inquiry Card
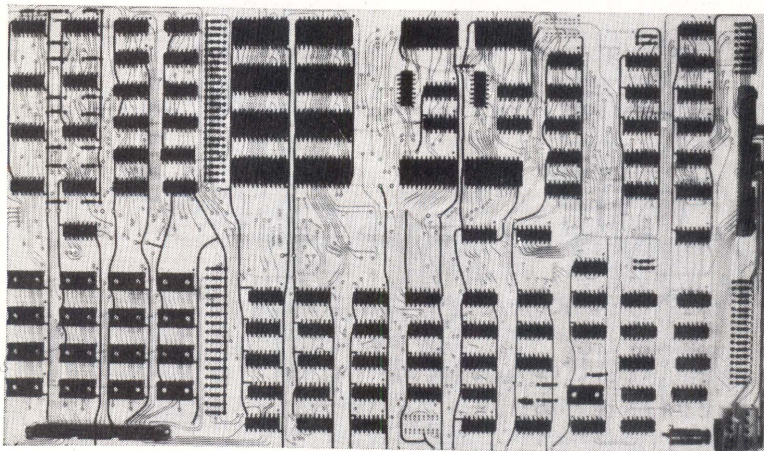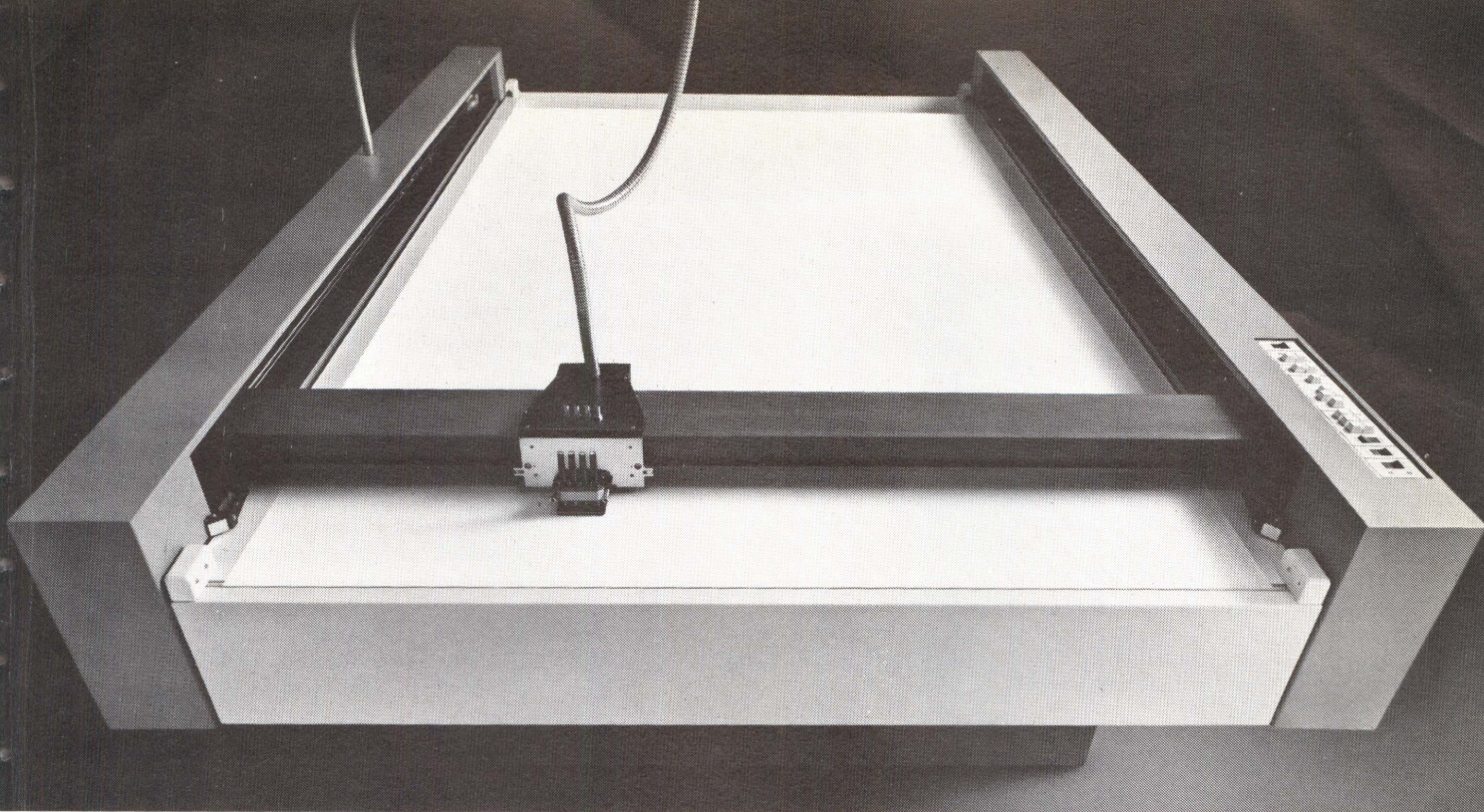
It draws faster than ink flows.

We call it the 748. It's big. And it's fast.

Its 4 inking pens move at speeds over 40 inches a second. That's faster than ink flows, so we had to figure out a pressure inking system that lets the ink catch up to the pens.

If you make integrated circuits or maps. Or if you have precision drafting needs, this is the new tool.

The 748's plotting area is 48"x 82". It can scribe coated materials and cut strippable film. At peak speeds!

The quality of its line is not impaired by its incredible speed. And like all CalComp flatbed plotters, the new 748 offers easy-to-use software for most computers.

We service it in 29 countries. But the way we've made it, you won't be calling us very often.

Do call us to see it. Our number is (714) 821-2011. Or write California Computer Products, Inc., CD-M9-75, 2411 West La Palma Avenue, Anaheim, California 92801.
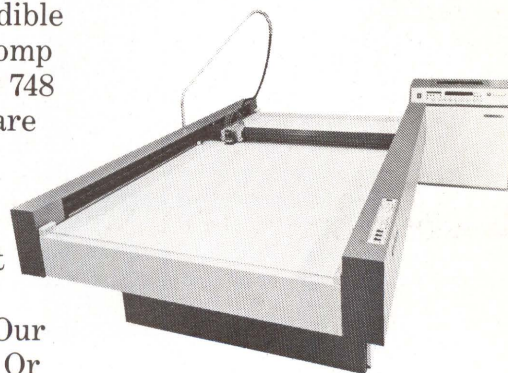
CALCOMP

High Speed, Bipolar μController Contains μProcessor Features

Desirable features of both stored program controllers and high performance microprocessors are included in a bipolar programmable microcontroller designed for use in high speed instruments, control, and data processing/collection systems. The single-board XMC-360, built by Xecon Associates, PO Box 267, Hawthorne, CA 90250, offers a powerful and efficient instruction set, flexible and performance-oriented I/O structure, and versatile machine architecture.

On-board features include 8-bit binary or 4-bit BCD arithmetic; individual bit test and manipulation capability; 32-word x 8-bit general register file; 16-level LIFO stack for subroutine nesting; high speed, low overhead, multi-level interrupt; parallel, serial, and bit I/O; and 1K-word program memory (field programmable ROM). Program memory is expandable externally to 4K words.

Typical register-to-register binary arithmetic, control, and test operations are fully executed in 480 ns; literal orders, bit manipulation, and jump and link instructions in 360 ns. Multi-precision binary arithmetic is performed at a rate of 480 ns/8-bit word group; multi-digit BCD arithmetic at 840 ns/digit. The standard repertoire includes over 50 instructions. Microprogrammed architecture permits instructions to be modified to accommodate special user applications as required. A versatile indexing feature coupled with a uniquely configured I/O instruction set and bus system permits especially high speed scanning and testing of peripheral devices, external bilevels, or data points.

A companion board holds an additional 2K words of program memory,
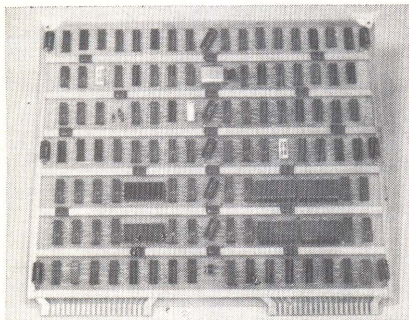
8-level expandable, vectored priority-interrupt system, program-controlled real-time clock, and 1K-word bipolar RAM. System development aids include a program development/control console, high speed paper tape reader, and time-share cross-assembler.
Circle 175 on Inquiry Card

---

n-Channel μProcessor Lowers System Interfacing Cost

Interface problems are reduced and sometimes completely eliminated as a result of the design of the 2650 n-channel microprocessor, according to its manufacturer. Signetics, 811 E Arques Ave, Sunnyvale, CA 94086 says that the architecture and instruction set for this machine, also known as the PIP (for Programmable Integrated Processor), have been shown to further reduce systems cost by reducing program memory in many applications.

PIP is completely TTL compatible on all I/O pins, including the single-phase, TTL clock input. Needs for external level shifters, pull-up resistors, and/or latches are completely eliminated by the interface structure when connected to other TTL or n-MOS devices. This eliminates the need for special I/O and memory devices, allowing minimal system configurations to be designed using only standard multi-source TTL, n-MOS, or CMOS devices.

Bus architecture includes 8-bit bi-directional data bus and separate 15-bit address bus. A fixed instruction set includes 75 arithmetic, logical, branch, and control instructions. The processor has seven general-purpose registers, main arithmetic logic unit and separate address adder, 8-level return address stack, and binary-coded decimal arithmetic capability.

Three I/O modes are provided including a 2-byte parallel mode, a single-byte parallel mode, and a serial I/O mode using the flag and sense lines. This last mode is particularly powerful in minimal system configurations since it provides a means of performing serial I/O under program control. Therefore, a simple and low cost interface can be designed for communicating with teletypewriters

and other serial input devices without memory buffering or reformatting the data. PIP also has a hardware vectored-interrupt capability which can handle up to 64 different I/O devices. This eliminates the need to poll the devices to find out which caused the interrupt, thus reducing the number of memory bytes required to handle interrupts and, at the same time, improving throughput time.

In addition to the usual register-to-register, immediate, and absolute modes, the 2650 provides 128-byte relative and powerful indexed addressing modes. Both relative and absolute modes have an indirect option which provides an efficient means of branching to various areas within the basic 32K of either program or data storage. Absolute indexed and absolute non-indexed modes can be specified with or without indirection, providing a total of eight different addressing modes on arithmetic and logical instructions. Relative and indexed addressing modes can be used to reduce program size and memory requirements compared with other microprocessors that do not have this capability. Indirect addressing capability provides a flexibility typically found only in minicomputer systems.

Because PIP has been designed using static logic only, the clock can be stopped in its low state for indefinite periods of time without any loss of status or data currently on the chip. This provides a convenience in debugging the device during program development, and gives one additional method of implementing direct memory access.

The company is also introducing a number of support prototyping and program development tools, including complete hardware and software manual with application notes, FORTRAN IV cross-assembler, and FORTRAN IV cross-simulator. The assembler and simulator are available both in batch and on NCSS and GE time-sharing services. A prototyping card, the 2650PC1001, which includes a crystal-controlled clock, 1024 bytes of RAM, several interfaces, and 1024 bytes of p/ROM coded with the PIPBUG debugging firmware package, is available. Additional support capabilities, including more application notes, cards, kits, circuits including MOS p/ROMS, a compiler, and a prototyping system, are in development.

Sampling of the 2650 began in May, and small volume production quantities are now being shipped. A full production buildup is underway and large volume shipments are expected toward the end of the third quarter.
Circle 176 on Inquiry Card

Hard-nosed software.

Minicomputer system software is coming of age. A report from Ball Computer Products, Inc., for concerned OEMs, worried systems houses and victimized end-users.

Software that really works.

What the Nova world needs now is software that works. Really.

What the Nova world has, right now, is just that. Ball Computer Products Minicomputer System Software (Ball/MSS).

Software that works on small small systems and large small systems.

Software that works and saves you money by reducing your hardware requirements.

Software that works even after hardware malfunctions (we call it graceful degradation).

Imagine that: software that works. Really.

Four years new: the Ball Disk Operating System.

Here's one you should get to know. A DOS that's been working for over 4 years, yet is new because it's been evolving constantly for that entire 4 years—the Ball Disk Operating System.

It requires less hardware than other Nova disk systems, so it saves you bread. Lots of bread.

It works as well for floppy systems as for fixed disk systems.

It supports FORTRAN IV with random access, and operates in as little as 16K of core.

And it's been doing it for 4 years.
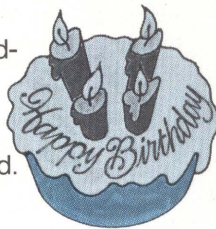
The ayes have it.

No more waiting around while the votes are being counted in the Wisconsin State Legislature.

Not since they installed a unique Ball minicomputer-based vote tabulating system in both houses.

Each legislator simply indicates his vote right at his seat, and the disk-based Nova system —featuring the Ball OMR 6500 mark reader—announces the results. Ball custom-designed the software to make the system work.
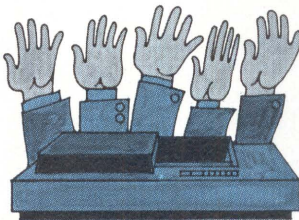
Regardless of the debate, the new voting system is never at issue.

A user in every port.

Ball's Time-Shared Basic is another friend when you're in need.

It supports as many as 64 users, simply by adding multiplexors and their associated connector panels. And additional disk space, for both program and data storage, can be added simply by adding the specific peripherals or peripheral systems.

A friend, indeed.

The ticker isn't late anymore.

Not since the Pacific Coast Stock Exchange installed a Ball Nova-based minicomputer system to keep up with stock-clearing transactions between brokers.

Special softward developed by Ball Computer Products included a multi-tasking monitor with a guaranteed 71-μsec interrupt response time.

Profits we can't guarantee. But at least brokers can now bank their certificates much earlier.

Goodies we got.

Yes, Va., we've got editors. And compilers. And assemblers. And linkers. And debuggers. In fact, we offer the most powerful real-time debugger for Nova systems you can get.

No, Va., you don't have to go anywhere else for software after you come to Ball Computer Products.

Except for the bugs. . . .

GET HARD-NOSED. ASK US.
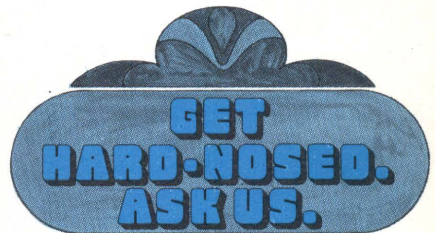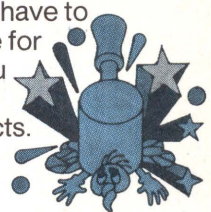
Name_____

Company_____

Address_____

City_____

State/Zip_____

Phone_____

Send me more information on minicomputer software that really works.

☐ Minicomputer system software. My application is_____
☐ Ball Disk Operating System.
☐ Ball Time-Shared Basic.
☐ Ball Fast Sort.
☐ Ball FORTRAN.
☐ Ball editors, compilers, assemblers, linkers and debuggers.

Ball Computer Products, Inc.
SUBSIDIARY OF BALL CORPORATION

5601 College Avenue, Oakland, California 94618. (415) 654-8626.
New York · Boston · Atlanta · Chicago · Los Angeles · San Francisco

Micro/Mini
Short Course

"Microprocessors and Minicomputers —Interfacing and Application" is aimed at scientists and engineers who plan to put such small computer systems to use, as well as managers who want to know the alternatives in control data acquisition and automation design. This course will be taught Dec 14-19 at Virginia Polytechnic Institute and State University, Blacksburg, Va under sponsorship of the American Chemical Society and the VPI Extension Div. Instructors will be Raymond E. Dessy and members of VPI's Chemistry Dept Instrument Design and Automation Research Group. Laboratory participation will involve I/O bus structure as well as hardware and software interfacing to standard components. Separate experiments will be organized to match the needs of both those with no previous knowledge of electronics and those familiar with small computer systems.

For additional information or for reservations contact the Dept of Educational Activities, American Chemical Society, 1155 Sixteenth St NW, Washington, DC 20036. Tel: (202) 872-4508. Registration is limited to 24. Fee is $325 for ACS members or $360 for non-members.

μComputer Development
System Adapts to
Various μProcessors

A complete, standalone system for writing, debugging, and executing programs on the Intel 8080 microprocessor, Microkit-8/16 can also be used as a development tool for new microprocessors. The system, offered by Microkit Inc, 2180 Colorado Ave, Santa Monica, CA 90404, is made up of processor, memory, and peripherals. Universal systems bus design allows memory and peripherals to be used with either 8- or 16-bit processors by adding processor cards and software packages.

Features include 8 kilobytes of RAM, memory write protection under software control for each 1K page, crystal-controlled real-time clock with 32-μs resolution, interrupt driven I/O, memory expansion to 56 kilo-

bytes, interprocessor I/O port for developmental and production testing of microprocessor systems, and bootstrap loader in p/ROM.
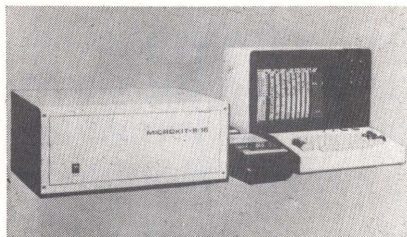
Standard peripherals are alphanumeric CRT display, ascii keyboard, and two cassette units. Software consists of monitor, editor, and assembler.

The CRT display holds 960 characters and can update the screen at 50,000 char/s. Magnetic tape cassette units read and write at an effective rate of 100 char/s including preambles, postambles, and error checking. Keyboard is a full 53-key, reed-switch unit. Basic system includes two RS-232-C interfaces for modem and teleprinter, 8-level vectored interrupt, 1-megabyte/s DMA capability, programmable real-time clock, and six extra card slots for user-designed interfaces.

Circle 177 on Inquiry Card

Training Aid Spans
μProcessor Hardware
and Software Gap

Designed to help hardware-oriented engineers master the software of any 4- or 8-bit microprocessor now on the market, the μ Primer 4/8 contains microprocessor (CPU) memory circuits for program and data storage, front panel with controls and indicators to address and display memory contents and CPU status, and
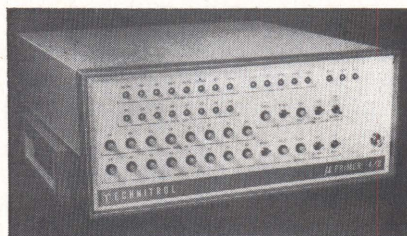
power supplies. Made by Technitrol, Inc, 1952 E Allegheny Ave, Philadelphia, PA 19134, the unit gives its operator a feel for the power of the instruction set and an appreciation of the advantage of software solutions to hardware problems.

Among the teaching capabilities are writing programs in mnemonics, writing subroutines in high-order program memory address locations and jumping them with conditional or unconditional jump instructions, and writing finite and infinite program loops. The unit can also be used to breadboard prototype systems.

The learning aid provides entry of memory address and instructions in machine language (1's and 0's); display of memory address and data by front panel LEDs; increment, decrement, or force-load of program memory address; display of results of CPU operation; and single-step operation to simplify learning and program debugging. Entry to the program memory is by front-panel switches using binary machine language formatted to be compatible with the operation code of the instruction set as published by the CPU manufacturer.

Address and content of the program memory are displayed simultaneously in binary code to facilitate program entry and/or verification. In addition, machine status, indicating the type of operation being performed by the CPU, is displayed on the front panel. Data are output to front-panel output display ports under program control. This feature is used to display the end result of a series of instructions or may be used to check the condition of the CPU accumulator at critical points within a series of instructions. When operated in the single-step mode, this provides a useful tool in debugging short program routines.

All of the CPU manufacturer's instruction set can be executed, including arithmetic operations, logic manipulations, accumulator rotations, register-to-register transfers, and conditional and unconditional jumps. A 4-bit machine may be converted to an 8-bit machine (or vice versa) by changing a personality card containing the microprocessor chip and a front-panel harness assembly. Memory and control devices remain the same.

Circle 178 on Inquiry Card
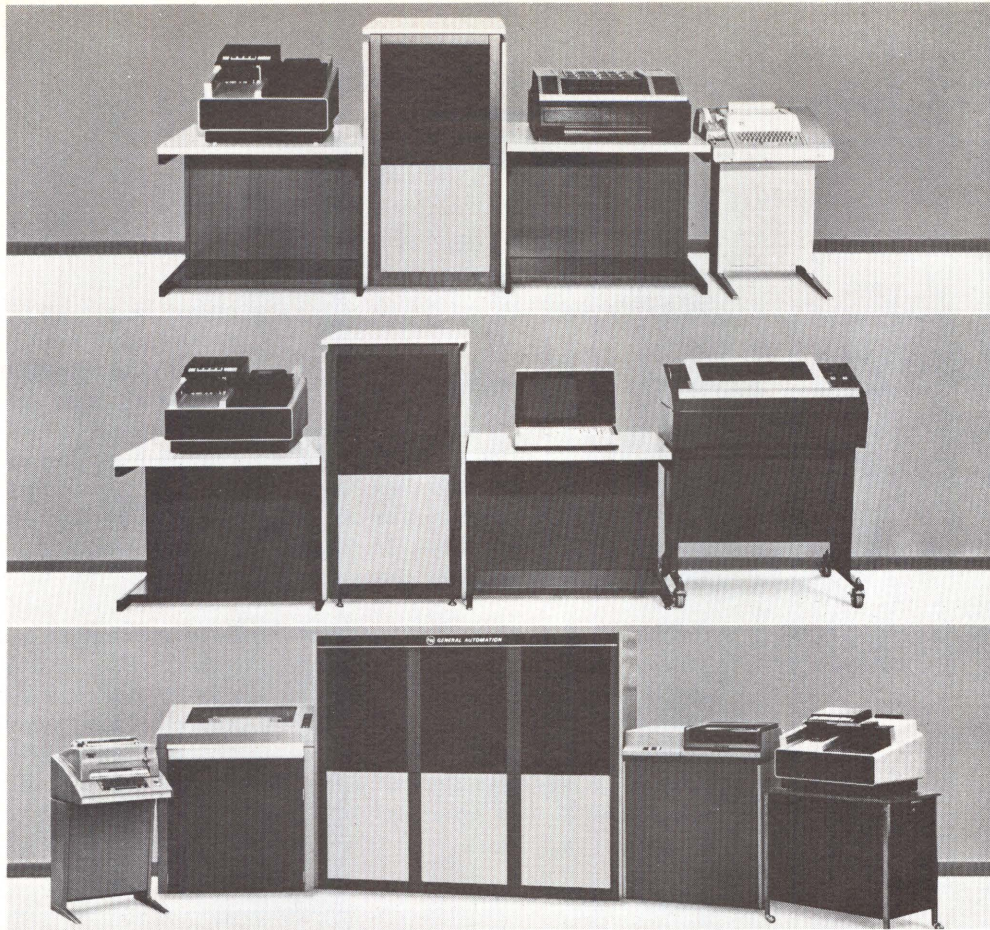
ONLY ALL OF THE ABOVE CAN OFFER ALL OF THE BELOW:

General Automation's new family of low-cost, expandable remote batch terminals offer more capabilities than any competitive systems produced by any terminal or minicomputer manufacturer anywhere.

Here's what we mean by *capabilities:*

Talk to any computer.

Our software emulator packages make our terminals multi-lingual. They can talk to IBM 360/370 HASP or 2780 work stations. They'll also emulate a Control Data User Terminal. Or a UNIVAC 1004 system.

Data spooling included.

Our disk-based emulator packages have data spooling. Which saves you transmission time. Which saves you money.

More operating systems.

Most RBTs have one or two operating systems. Ours have three.

Including Free Standing (FSOS), Disk-Based (DBOS) and Real Time (RTOS) operating systems.

Name your configuration.

We can provide any hardware configuration, including any kind of peripheral equipment you could ask for. Our RBT family consists of three basic communications systems (base prices range from $19,500 to $30,000):

RBT-1 is an intelligent batch communications terminal used for entering, transmitting and receiving data between a remote location and a central computer.

RBT-2 combines communications terminal capabilities with a batch-oriented satellite data processing system.

RBT-3 is a complete communications system plus multi-programming-oriented stand-alone data processing system offering concurrent batch and real-time operations.

Communicate with an expert.

General Automation didn't get into the communications business yesterday. We are already the major supplier of minicomputer systems for front end processors, distributed data systems, Telex message switching systems and PABX control systems for the world's largest international communications companies. We're also the number one solver of tough communications problems in more than a dozen different industries.

We provide virtually everything you need to build or expand a data communications system. We can show you the best ways to get the most out of your communications dollar.

Give us a call at (714) 778-4800. Or write to one of the addresses below.

COMMUNICATIONS SYSTEMS BY GENERAL AUTOMATION

HOME OFFICE: 1055 South East Street, P.O. Box 4883, Anaheim, California 92803. Telephone (714) 778-4800.
EUROPE: General Automation, S.A., 24 rue du Sergent Bauchat, 75012 Paris, France. Telephone (1) 346/7973. CANADA: G.A. Computer Ltd., Ontario.
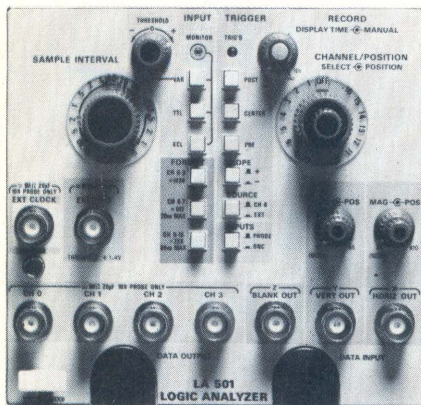
Digital Storage Unit Converts CRT Display Into Logic Analyzer

Any X-Y display having a bandwidth of at least 500 kHz can be used for logic analysis of any bit-, byte-, or word-serial digital system by interfacing the LA 501 logic analyzer; virtually any cathode-ray tube (CRT) monitor or oscilloscope can be utilized to display up to 16 channels of data in the form of a logic timing diagram. Introduced by Tektronix, Inc as a 2-module-wide plug-in for the company's TM 500 line of test and measurement instruments, the LA 501 provides 4096 bits of data storage and sampling rate to 100 MHz. The display need not necessarily be dedicated; eg, if attached to an oscilloscope for fault isolation, the oscilloscope can also be used in its normal mode for in-depth, real-time electrical analysis once the fault has been located,

or for other tasks when not needed as a logic analyzer.

Modes of Operation

Storage capacity can be formatted as 4 channels x 1024 bits, 8 x 512, or 16 x 256, depending on user's application. Up to four units can be master-slaved to achieve 16 channels x 1024 bits or 64 channels x 256 bits.

Choice of pre-, center-, or post-trigger operating modes permits operator selection of where the displayed block of data falls with respect to a trigger taken from his system. In pre-trigger mode, 90% of the displayed data occur before the

trigger (to observe the data sequence preceding a fault, for example). In center-trigger mode, 50% of the displayed data occur before the trigger; and post-trigger mode provides a display (similar to that of a conventional oscilloscope) with 90% of the data occurring after the trigger.

Virtually any logic family can be accommodated. TTL or ECL thresholds can be chosen by two pushbuttons of an input control; a third pushbutton and a rotary control provide a variable threshold from −10 to +10 V for compatibility with other logic families.

A position control allows any one channel of the display to be selected and moved vertically for tim-

Housing for the LA 501 can be portable, benchtop, rackmount, or rollabout, as desired. For instance, it could be placed with an oscilloscope module in a 4-module-wide mainframe; or combined with digital delay and counter-timer modules in a mainframe, using a separate oscilloscope for the display (center). The latter arrangement would allow the trigger point for the display to be delayed by up to 99,999 events following the system trigger point. A rollabout test system (right) could be made up of a mobile cart, portable oscilloscope, and up to six plug-in instruments including the 2-module wide LA 501. If the instruments had to be hand-carried to the test site, a traveler/mainframe could house LA 501, oscilloscope, and one other module (top)

ing comparison with the other channels. Combined with horizontal and vertical magnifiers (adjustable from X1 to X10), this provides a high degree of display resolution.

The operator has a choice of internal or external clocks, which permits synchronous or asynchronous sampling of machine data. Sampling rates are 100 MHz (10 ns/bit) in the 4-channel x 1024-bit mode, 50 MHz for 8 x 512, and 20 MHz for 16 x 256.

Applications

A 16-channel storage capability permits sequential data across a minicomputer's 16-bit word to be displayed for timing comparison or for ready detection of undesired parallel combinations. Input and output of eight channel buffers, interface cables, or control buses can be displayed simultaneously. Adding a digital delay module eliminates mechanical jitter from the display by basing its delayed trigger on a count of clock pulses. Up to 16 channels of any data segment in a disc file can be displayed.

In data communications applications, which involve long trains of data in single-shot bursts, up to 4096 bits of a data burst are stored for display as long as required. Choice of trigger modes permits data display before or after a given trigger point selected from the train. Variable memory format permits use in specific tasks, such as—for example, in the 4-channel x 1024-bit mode—viewing a long segment of a modem's serial data output simultaneously with the clock and frame pulses.

For industrial control operations, which commonly involve high electrical noise environments, the unit's single-shot storage capability can be used to trigger a display whenever a random noise pulse occurs. Location of the pulse in the stored data block can then be found by use of the multi-channel storage capacity and pre-triggering capability.

Other Specifications

In addition to those capabilities already mentioned, the unit provides input impedance choices of 1 MΩ on the first four channels, or 20 kΩ in any mode. Resolution is 10 ns/sample in internally clocked mode. Clocking modes are internal using 100-MHz clock, or external using 50

MHz or less for 4- or 8-channel modes or 20 MHz or less for 16-channel mode. Trigger sources can be internal (channel 1) or external.

Data storage and display time is variable from <1 to ≥10 s. Storage for an indefinite period can be selected. A new data recording cycle can be started at any time by manual reset. Both parallel and serial data outputs are provided.

Line voltage requirements are 100, 110, 120, 200, 220, or 240 Vac ±10%. Power consumption is 32 W.

Price and Delivery

Price of the LA 501 logic analyzer is $3250, including standard probe package, plus $150, $180, $240, or $325, respectively, for the required TM 503, TM 504, TM 506, or TM 515 mainframe. Deliveries will begin in December. Tektronix, Inc, PO Box 500, Beaverton, OR 97005. Tel: (503) 644-0161.

For additional information circle 199 on inquiry card.

PRODUCTS

Time-Domain Oscilloscope With Real-Time Display
Can Also Provide Data-Domain Picture of Same Signal

Real-time display of actual signals is prime capability of the model 1740A 100-MHz oscilloscope. To relate the timing of events to one another and to the triggering event, external trigger is displayed as a third trace, rather than as a substitute for one of the two channels. Center screen is always the trigger threshold. Time relation between external trigger and vertical signals is held steadily at 2.5 ns ±1 ns. 5 mV/div at 100 MHz provides detail to study ECL; sensitivity of 1 mV/div at 40 MHz, obtained with a X5 magnifier, can be used to look directly at tape or disc outputs or at power supply ripple. 1 mV/div is available on both channels simultaneously. Lowest sensitivity is 20 V/div. When associated with a model 1607A logic state analyzer, a data-domain picture can be alternated with time-domain waveforms of the same signal. Frequency response is maintained through a 0 to 50°C range. Power line voltage may be 100, 120, 220, or 240 V (±10%); line frequency 48 to 440 Hz. There are only 44 adjustments inside the fully closed case. **Hewlett-Packard Co,** 1501 Page Mill Rd, Palo Alto, CA 94304. Circle 200 on Inquiry Card
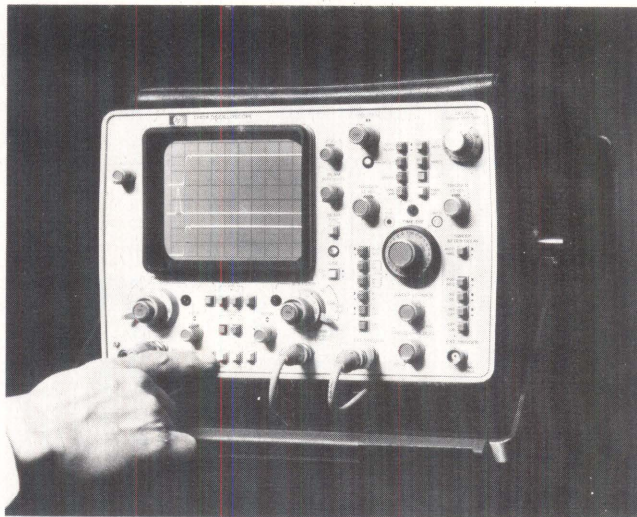
Low Cost CMOS Static RAM
Competes with n-MOS Devices

As fast as many standard n-channel MOS RAMs, the low power P5101-8 CMOS static RAM is also claimed to be more than price competitive when both parts and power supply costs are considered. The 1K (256 x 4) silicon-gate device operates on a single 5-V power supply and costs less than 1¢/bit in production quantities. Max standby current is 50 nA/bit (250 μW or less per package). Worst-case access time is 850 ns. Chip-enable clocking is not required during address transitions; the device can be placed into low power standby mode by applying a logic low level to the second chip-enable input. It can operate on either separate memory system I/O buses or on a common I/O bus without bidirectional bus logic. Four 3-state data outputs with disable control, two chip-enable inputs, R/W control, and address inputs are provided on a 22-pin DIP. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95050. Circle 201 on Inquiry Card
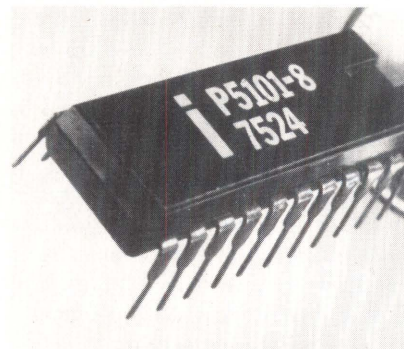
Microprocessor Control in Plasma Display
Graphics Terminal Offers User Flexibility

By combining microprocessor technology with a plasma panel graphics medium, the model 12,000 provides users with flexibility in generating dynamic graphical presentations. There is no screen jitter or flicker since the plasma display does not require refresh. The 512 x 512 matrix display has 60-line resolution. Complete selective write and erase of each dot permits displays to be dynamically altered. Data rates are selectable to 4800 baud, 240 char/s (2400 baud), 80 vectors/s any length (2400 baud). Char generation is 7 x 9 on an 8 x 16 matrix, 32 lines of 64 char/line. Communications interface is std RS-232-C with ASCII format. Firmware microprogram options include APL char set, extended ASCII char, space-overwrite latch, variable writing modes, variable char size, and addressable cursor. Supporting software is written in FORTRAN. A touch panel device, a microfiche rear-projection unit, and a program alterable char set with 2K RAM for constructing special symbols are also available. **The Magnavox Co,** 2131 S Coliseum Blvd, Fort Wayne, IN 46803. Circle 202 on Inquiry Card
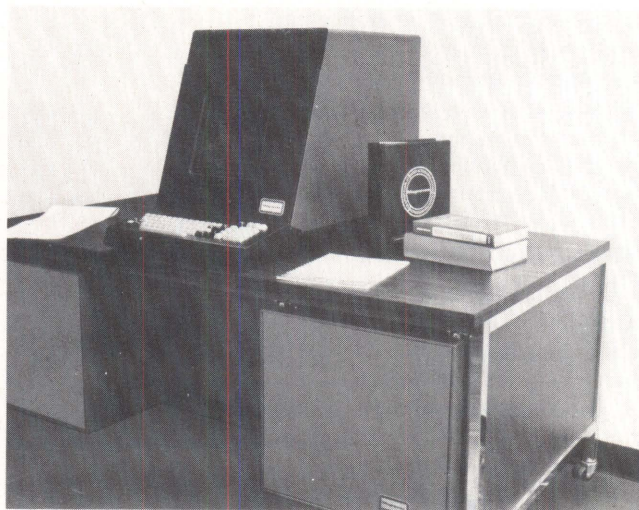
SALES ARE UP PROFITS ARE UP

AND OUR SALES FORCE IS GOING UP 50%

Grow with us. We're looking for more experienced minicomputer salesmen to continue this past *growth*. Salesmen who know the products, competition and markets. In return for this experience we'll pay you the industry's highest bonus for new accounts. As well as our excellent commission plan for existing business. Best of all is the products we'll give you to work with.

New Varian products introduced in just the past few months include: TOTAL Data Base Management, RPG II, FORTRAN IV Level G, COBOL—and top of the V70 series minicomputer line: The V75 handling 32-bit functions. So act now before the positions are filled.

Call collect to the Varian District Sales Manager nearest you for an appointment today.

Orange County, CA (714) 897-9515 J. McNutt
Los Angeles (213) 598-4438 J. McNutt
San Francisco (408) 736-5630 J. Usher
Dallas (214) 231-5145 I. Wardlow
Chicago (312) 692-7184 F. Hirsch
Boston (617) 890-6072 D. McInnis
New Jersey (201) 569-2323 R. Bassin
New York (212) 325-5248 R. Bassin
Washington, D.C. (301) 773-6770 R. Schaper

⊘varian
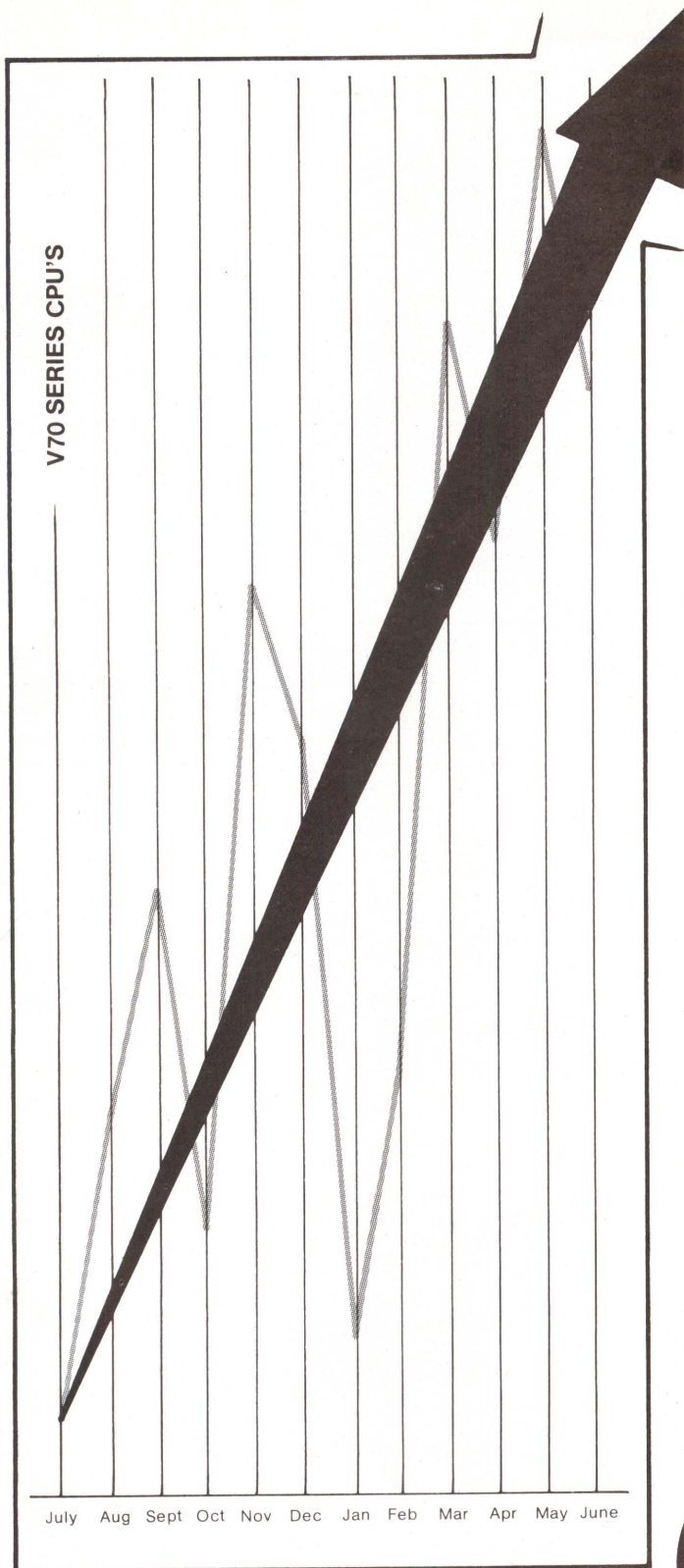
VOICE DATA-ENTRY SYSTEM
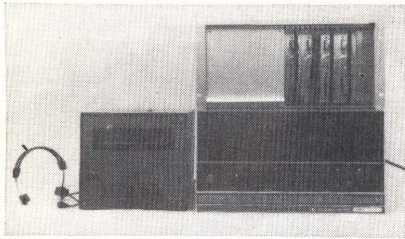
VDETS 1000 series terminals convert spoken utterances to machine-readable code. Input may be words or short phrases and output is std ASCII code, which may be used to enter data into a computer, retrieve stored information, or control machine operations. The system is trained for the individual speaker; vocabulary can be trained on- or offline. It will operate in amb noise conditions up to 90 dB specific avg and 110 dB pk. Min inter-command gap is 200 ms and response time is approx 20 ms. **Scope Electronics Inc,** 1860 Michael Faraday Dr, Reston, VA 22090.
Circle 203 on Inquiry Card

4K RAM, PLUGGABLE PACKAGING ASSEMBLY

A wire-wrappable board, the multilayer IC-pluggable packaging assembly accepts 54 22-pin 4K RAM chips and also has a universal pattern capable of mounting up to 40 std 14- or 16-pin DIPs. The board measures 9.5 x 10". It has a voltage distribution plane (V_{CC}) on the component side of the assembly, an internal plane (V_{DD}), and V_{SS} plane on the wrapping side. **Garry Manufacturing Co,** 1010 Jersey Ave, New Brunswick, NJ 08902.
Circle 204 on Inquiry Card

LOOP CURRENT REGULATOR
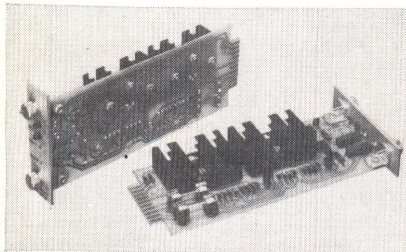
Modules regulate loop current over wide variations in loop resistance and battery voltage. Each contains two independent regulators that are adjustable from 13 to 75 mA over a voltage range of from 15 to 150 V, polar or neutral. LED indicators display circuit conditions. Max power dissipation is 8.5 W at 55°C. 16 modules, 32 circuits, may be housed in a rack-mounted enclosure. **Dataprobe Inc,** 290 Huyler St, Hackensack, NJ 07606.
Circle 205 on Inquiry Card

SWITCHING POWER SUPPLY

OL series open-frame, 4-output supplies for computer peripherals provide 10-, 60-, or 300-W power. All outputs are short-circuit proof and reverse polarity protected; one has overvoltage protection. Customized for each application by modifying the output transformer and filter, outputs up to 300 V and up to 25 A are available. Efficiency is 75 to 80% typ, depending on output voltage. Ripple and spikes are held to 40 mV rms and 100 mV pk-pk. **Boschert Associates,** 3010 Lawrence Expy, Santa Clara, CA 95051.
Circle 206 on Inquiry Card

FORMATTED CARTRIDGE DRIVE SYSTEM
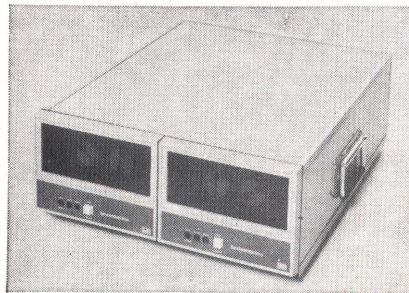
The DCS-5000 data cartridge system combines DCD-3 data cartridge drive with power supply and formatter electronics to provide an ANSI/ECMA-compatible data system of up to eight drives. System features include a register for command inputs, read-while-write error check, status and error flags, automatic generation of the ANSI-required block-formatting including tape mark, automatic search to tape mark at 90 in./s, and a clocked variable-length erase capability. **3M Co, Mincom Div,** 223-5E, 3M Center, St. Paul, MN 55101.
Circle 207 on Inquiry Card

DC SOLID-STATE RELAYS

Modular solid-state series 223 devices are opto-isolated for total I/O isolation, and are directly compatible with DTL/TTL input. Offered in six models, the relays are spst (N.O.) devices rated for loads of 50 Vdc. Load current levels of 2 and 5 A are available in 0.032"-pin, quick-connect, or screw terminals. Switching speed is 100 μs. Dielectric withstanding voltage (60 Hz) is 1500 Vac rms. Insulation resistance is 10^9 Ω. Storage temp ranges from −55 to 100°C, and op temp from −40 to 80°C. **C. P. Clare & Co,** 3101 W Pratt Ave, Chicago, IL 60645.
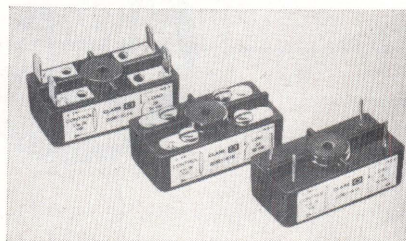
Circle 208 on Inquiry Card

AUTOMATIC S/R DATA TERMINAL
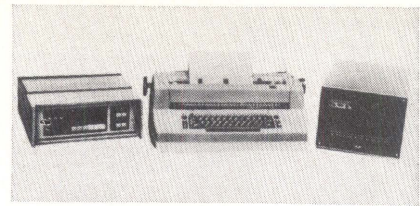
Model 38 KSR terminal, with ASCII-compatible Philips tape cassette unit, permits data transmissions over std telephone lines via a phone coupler. Data can be received at normal typewriter speeds, then batch-processed at 300 baud from the cassette cartridge (1200-baud transmission is optional). Other features include high speed numerical search, remote control of tape from a std IBM Selectric^R typewriter keyboard, hardcopy printout of stored data, and a status display panel for operators. **Tycom Systems Corp,** 26 Just Rd, Fairfield, NJ 07006.
Circle 209 on Inquiry Card

REMOTE DATA ENTRY SIGNALING TERMINAL

Direct access to a computer from any Touch-Tone^R or rotary dial phone is possible with the model 5000 OVERDIAL™ terminal, which provides slow speed data entry for information-handling tasks. For input security of remotely accessed computer systems, the unit disconnects users without the proper access code. The terminal decodes from two to six digits, Touch-Tone signals as low as −30 dBm, or dial pulse input. Std ring detection is 20 Hz, 1.8-s on, and 4.2-s off. **BBL Industries Inc,** 2830 Clearview Pl, Atlanta, GA 30340.
Circle 210 on Inquiry Card

3-D SONIC DIGITIZER
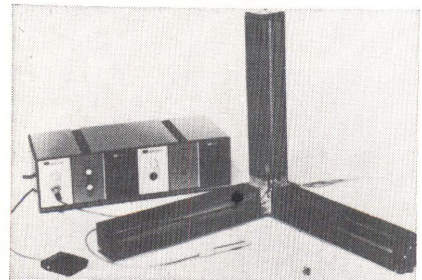
GP-3/3-D converts descriptions of 3-dimensional objects into digital form for input to data processing systems, by generating sets of X-, Y-, and Z-coordinates for points within the space bounded by linear sensors. The operator traces a 3-D object on the unit's operational area with a stylus which generates supersonic pulses. Units are available with English or metric outputs, with 0.01" or 0.1-mm resolutions. Sensor lengths—defining the Graf/Pen's active area—are up to 24". **Science Accessories Corp,** Kings Hwy W, Southport, CT 06490.
Circle 211 on Inquiry Card

AT THE INVITATIONAL COMPUTER CONFERENCES...

You are invited to see and hear everything you need to know about state-of-the-art technology in OEM Computer Equipment and Systems. Plan to attend the technical product seminars and product displays brought to you and presented by:

Ampex, Cipher Data Products, Computer Automation, Control Data Corporation, Data Disc, Data Printer, Dataram, Digi-Data, EMM Computer Products, Facit-Addo, Hewlett Packard, Interdata, ISS/Sperry Univac, MITS, Memorex, Mohawk Data Sciences, Pertec, Plessey Microsystems, REMEX, Rockwell International, Scientific Micro Systems, Sykes Datatronics, Tally, Tektronix, Varian Peripheral Products, and Victor Associates.

Plan to attend the location nearest you
during 1975/76:

September 30, 1975	Newton, Massachusetts
October 21, 1975	Cherry Hill, New Jersey
October 23, 1975	Long Island, New York
November 20, 1975	Palo Alto, California
January 15, 1976	Houston, Texas
February 17, 1976 (tent)	Ft. Lauderdale, Florida
March 25, 1976	Orange County, California
April 13, 1976	Cleveland, Ohio
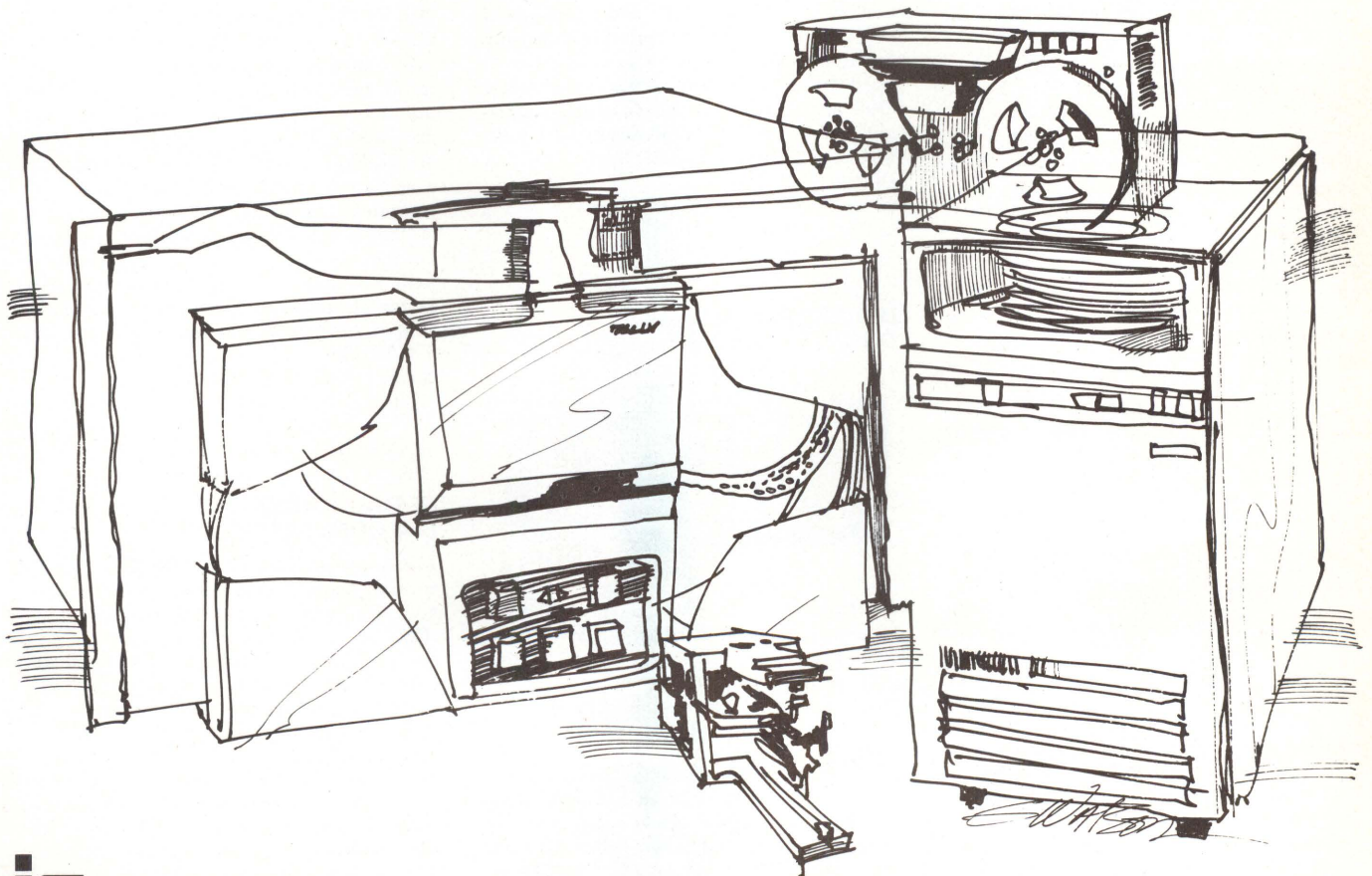
icc For your personal invitation contact one of the participants listed above or B.J. Johnson and Associates, 300 Otero, Newport Beach, California 92660 (714) 644-6037.

PRODUCTS

DIGITAL PROGRAMMABLE PULSE MODULE

A TTL/ECL-compatible one-shot system, model 2141 provides output pulses within 1 ns of selected time in a range of 20 to 1020 ns after TTL or ECL trigger, as well as variable pulse widths from 15 to 1000 ns. Delay and pulse widths are controlled by three decades of remotely generated BCD inputs. External trigger rate is 0 to >15 MHz, input impedance is 50 Ω, insertion delay is <20 ns (including ±500 ps uncertainty), programming time is <100 ns, and worst-case jitter between leading and trailing edge pulse is ±200 ps. **Technitrol, Inc,** 1952 E Allegheny Ave, Philadelphia, PA 19134.
Circle 212 on Inquiry Card

DATA SEND/RECEIVE OPTICAL SYSTEM
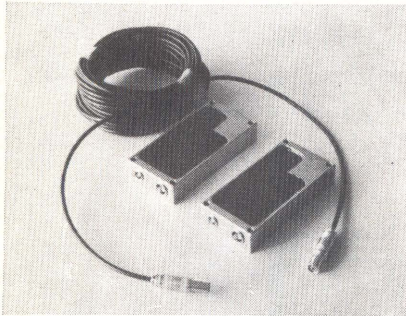
A1, A2, and A3 senders transmit either one channel of digital data or a 0- to 10-V analog signal having 0- to 10-kHz, 0- to 100-kHz, or 0- to 10-MHz frequency. Used with an optical waveguide which is immune to electric and magnetic disturbance, the DU-S-1 single-bit digital sender and DU-E-1 digital receiver, as well as DU-S(E)-1A1, -A2, and -A3 analog senders and receivers permit data to be transmitted in abnormal environments. Std systems operate over distances of up to 60 m. **Triskelion ag,** Fiber-Optic Div, Ch-6317-Oberwil, Switzerland.
Circle 400 on Inquiry Card

p/ROM PROGRAMMER

The Altair 8800 is a complete software development and p/ROM programming system that is equipped with an industrial Altair 8800 processor, 8K dynamic RAM memory, TTY or std RS-232 interface, p/ROM programmer, p/ROM memory card with 256 bytes, loader on p/ROM, and slots for plugging in two additional cards. Room for eight additional slots is provided. Software, on cassette or punched tape, includes resident assembler, text editor, system monitor, BASIC, and diagnostics. **MITS,** 6328 Linn, NE, Albuquerque, NM 87108.
Circle 213 on Inquiry Card

MAGNETIC STRIPE CARD READER

The hand-operated CR-1000 has no moving parts, springs, dampers, or return mechanism; the card is stroked through the slot by hand. Designed to operate at from 2 to 60 in./s, the unit is insensitive to speed changes. Complete with detection and code conversion electronics, the reader provides RZ serial data with a clock. The 7⅜ x 1⅝ x 2½" unit is capable of reading cards encoded with 2-frequency (Aiken) coherent phase recording which conforms to ABA or IATA stds. **Conrac Corp, Cramer Div,** Mill Rock Rd, Old Saybrook, CT 06475.
Circle 214 on Inquiry Card

GRAPHICS DISPLAY SYSTEM

The MEGRAPHIC 6000 contains graphics processor, 8K Nova 2/4 minicomputer, 19" display, and full ASCII keyboard. Heart of the system is the BP-752 graphics processor which can display 6000 flickerfree points and/or vectors with full-screen resolution of ±0.05%. The unit operates from a core-based display list which accepts either 2-word absolute or 1-word relative vector elements. Jump-to-subroutine capability permits up to four levels of display list nesting. **Megatek Corp,** 1055 Shafter St, San Diego, CA 92106.
Circle 215 on Inquiry Card

BIDIRECTIONAL COUNTER-DISPLAY
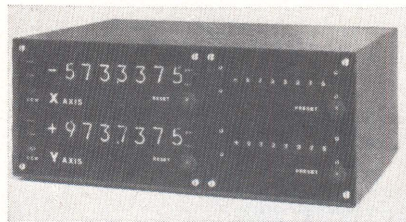
Available in 1-, 2-, or 3-axis models, with from four to seven 200,000-hr cold cathode display units per axis, the DDC features fully floating resettable-zero with automatic display of appropriate (+) or (−) polarity. An automatic data-overflow indicator lamp is also provided; a positive power interruption protection feature stops the counter and triggers an indicator lamp if line voltage drops below rated min for more than 30 ms. A built-in switch matches the unit to either 115 or 220 Vac, 50- to 60-Hz operation. **C-Tek, Inc,** 4 Railroad Ave, Wakefield, MA 01880.
Circle 216 on Inquiry Card

SYNCHRO-DIGITAL CONVERTERS

M series modules convert analog signals from transducers such as synchros, resolvers, and selsyns to binary or BCD digital format. A large number of inputs can be multiplexed into a single converter using a compatible series of input signal-conditioning modules. Accuracy and resolution of 8-, 10-, and 12-bits binary or 0.1-deg BCD are available. Units will accommodate all std synchro frequencies and voltages. Modules will track inputs at a max rate of 2000 deg/s and will respond to a 180-deg step input in <4 ms. **Astrosystems, Inc,** 6 Nevada Dr, Lake Success, NY 11040.
Circle 217 on Inquiry Card

STATIC SEMICONDUCTOR MEMORY
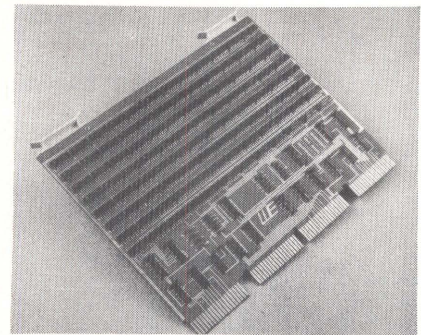
WE-VM8E plugs directly into the DEC PDP-8 Omnibus™ and is completely hardware/software compatible with PDP-8E, F, or M minicomputers. 4K x 12 (-VM8E4) and 8K x 12 (-VM8E8) memory systems are designed around a 1024 x 1 n-MOS static RAM, resulting in fewer components (no refresh circuitry) and low power consumption—18 V max for the 8K memory. A simple field-select jumper matrix printed on the circuit board allows easy memory field assignment in 4K increments. **Computer Extension Systems,** Clear Lake Towers, 16902 El Camino Real, Houston, TX 77058.
Circle 218 on Inquiry Card

ULTRA-STABLE D-A CONVERTERS

1900A series 14-, 15-, and 16-bit D-A converters feature differential linearities of <¼, <⅜, and <½ bit with the MP1914A, -15A, and -16A, respectively, over the full op temp range. Settling time to rated accuracies are 1.5, 2, and 3 μs typ in current mode. Tempcos are specified as: 3-ppm/°C max gain, 2-ppm/°C typ linearity; and 3-ppm/°C max reference voltage. Offset drift in unipolar current mode is 1-ppm/°C max; and offset drift in unipolar voltage mode is 2 ppm/°C max. All are packaged in a 2 x 4 x 0.375" shielded module which can be mounted on 0.5" centers. **Analogic Corp,** Audubon Rd, Wakefield, MA 01880.
Circle 219 on Inquiry Card

NONVOLATILE IC MEMORY SYSTEM
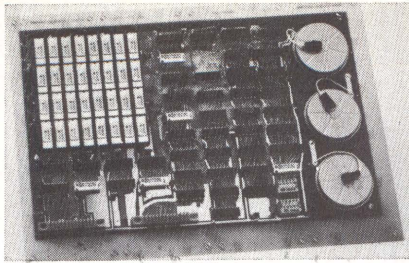
A CMOS memory system with battery backup, the Monostore IX/Planar is designed around a 1024 x 1 CMOS static RAM, providing up to 4K x 8 capacity on a single board; multiple boards can be combined for 64K, 8-bit words on the same bus. Access and cycle times are 450 ns; I/O levels are TTL compatible. Each board includes timing, control, module decode and address register, I/O data register, backup battery, and memory array. A single 5-Vdc supply powers the board. 3.25-Vdc at 120-μA standby power is provided by the battery. **Monolithic Systems Corp,** 14 Inverness Dr E, Englewood, CO 80110.
Circle 220 on Inquiry Card

PORTABLE DATA TEST SET

A fully keyboard-programmable test unit for synchronous and asynchronous data communications equipment, the 1608 may be used with computer terminals operating at speeds to 19,200 baud in either mode. The device incorporates an 8-level keyboard and independent, expandable receive and transmit program stores having 64- and 192-char capacities, respectively. Using an array of LED indicators, the unit displays received and transmitted data for comparison. **Nolton Communications Ltd,** Delamare Rd, Cheshunt, Herts, England.
Circle 401 on Inquiry Card

2000/2400-BIT/S MODEM WITH ANSWER-BACK
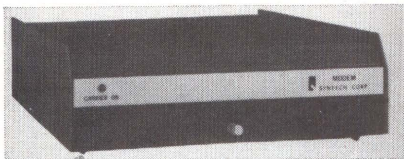
Bell 201C-compatible, the TT-201C is a medium speed, synchronous modem that is capable of operating at either 2000 or 2400 bits/s over the DDD network and features an answer-back tone for use with auto-dial systems. Internal strap options permit users to select from a variety of configurations and operating modes to meet specific requirements. Consisting of two PC cards housed in a standalone enclosure with integral power supply, the modem is also available as a card set, or in a rackmount enclosure that holds four modems plus integral power supply and mounts in a std 19" cabinet. **Syntech Corp,** 11810 Parklawn Dr, Rockville, MD 20852.
Circle 221 on Inquiry Card

LOW POWER DATA LOGGING SYSTEM
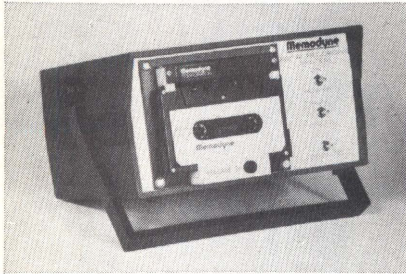
Recording digital information directly in ANSI/ECMA format on Philips cassettes, which can then be read, printed, edited, or copied onto other cassettes, or transmitted at 1200 baud with TI's ASW733 terminal or other ANSI/ECMA compatible devices, the basic 2800 series accepts parallel 8-bit ASCII-char, TTL or CMOS input. It operates on a single 5- to 12-V supply, consuming power only while recording; during standby it requires <100-μA current. An optional expander card provides for up to 40 parallel inputs (five decimal numbers). Input range is 10 V, or $\pm$5 V. **Memodyne Corp**, 375 Elliot St, Newton Upper Falls, MA 02164.
Circle 222 on Inquiry Card

PROGRAMMABLE SCIENTIFIC POCKET CALCULATOR
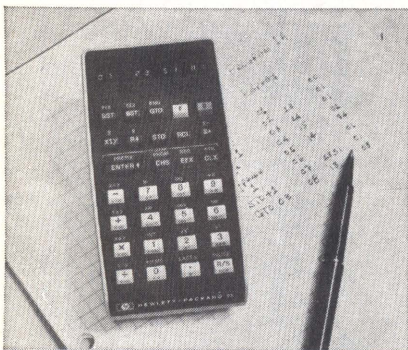
The 6-oz HP-25 offers engineering notation, which displays exponents as multiples of $\pm$3 for ease in working with units of measure [such as kilo (10^3), giga (10^9), pico (10^{-12}), nano (10^{-9})], and also has fixed-decimal format and scientific notation. The calculator has 49 steps of program memory, coupled with merged keycodes that conserve steps to effectively expand memory capacity. An integer/fraction key permits storage of two numbers in a single memory and an absolute value key adds to storage capacity and flexibility. **Hewlett-Packard Co**, 1501 Page Mill Rd, Palo Alto, CA 94303.
Circle 223 on Inquiry Card

KEYBOARD ENCODING IC

EA2030 is a 99-key, 4-mode encoder that identifies each key and mode with a simple binary number. Given that binary input, a p/ROM may be programmed, producing any code the user requires. Features include 10-bit code output, on-chip clock generator, built-in keybounce suppression, complete N-key rollover, electronic shift-lock, error detection for simultaneous key depressions, complete TTL compatability, and operation with std 5- and −12-V supplies. **Electronic Arrays, Inc**, 550 E Middlefield Rd, Mountain View, CA 94043.
Circle 224 on Inquiry Card

TRIPLE-OUTPUT DC POWER SUPPLY
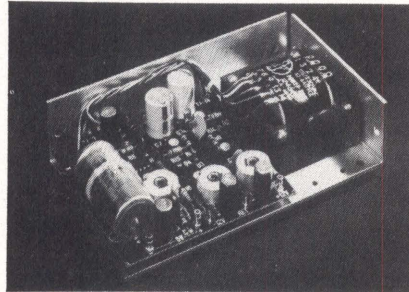
Claimed to be the smallest triple-output open-frame power supply available, model HTAA-16W provides 5 V at 2 A with over-voltage protection and $\pm$9 to 15 V at 0.2 A to power TTL, ECL, IIL, p-MOS, n-MOS, CMOS, and linear devices. Total isolation is provided between outputs to allow the user to arrange polarities to suit his application. Std features include 115/230 Vac $\pm$10% input capability, $\pm$0.05% line/load regulation, and full protection against short circuit and overload. **Power-One, Inc**, 531 Dawson Dr, Camarillo, CA 93010.
Circle 225 on Inquiry Card

DUAL DISC FILE SYSTEM

Providing large volume, inexpensive data storage for RS-232 compatible I/O devices, the D-474 features removable flexible magnetic discs with capacity for 217,000 char in 1000 sectors, and max access time of 1 s/sector. Simplified program control, combined with full I/O buffering, enhances the operational convenience of serial ASCII devices. Dual disc drives are available in the std cabinet; modular design allows direct plug-in expansion for multiple disc file operation. **BRD, Inc**, Box 10237, Bainbridge Island, WA 98110.
Circle 226 on Inquiry Card

HIGH NOISE IMMUNITY LOGIC ICs

Applicable to all present devices in the company's HiNIL family, changed supply voltage specs permit operation over a 10-to 16-V V_{CC} range and ease interface with CMOS in systems operated in the upper supply voltage range. Inputs on the devices (AC/CJ—plastic, AL/CL—ceramic) give 3.5-V min noise immunity and provide input protection for CMOS circuits. They also handle higher current/voltage output interface problems. **Teledyne Semiconductor**, 1300 Terra Bella Ave, Mountain View, CA 94043.
Circle 227 on Inquiry Card

SWITCHING REGULATED POWER SUPPLIES
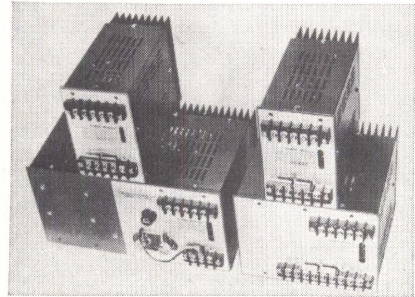
Family of small-size supplies offers from 70 to 80% efficiency, line/load regulation of <1% with an input voltage of 115 Vac $\pm$15% single phase at 40 to 500 Hz. The 24 incremental output voltages available range from 5 to 30 Vdc at 1.5 to 60 A with <50-mV pk-pk ripple (5, 9, 12, 15, 24, or 30 Vdc; 50, 100, 150, or 300 W). All models feature overvoltage and overload protection. Remote sensing is std. Multiple outputs in custom packages are also available. **Electro-Module, Inc**, 2855 Metropolitan Pl, Pomona, CA 91767.
Circle 228 on Inquiry Card

200-LINE/MIN. PRINTER

Model 104, a 132-col impact printer, in addition to an acoustically quiet, fully enclosed cabinet and modular electronics, features a self-test switch which allows offline testing for quick system checkout and for correct line-up of preprinted multiple-part forms. The device is plug-to-plug compatible with the company's entire line of printers and interfaces. Foreign language and u/lc char sets are available as are various others which are not available with std full-char printers. **Centronics Data Computer Corp**, Hudson, NH 03051.
Circle 229 on Inquiry Card

TOUCH-SENSITIVE
MEMBRANE KEYBOARDS
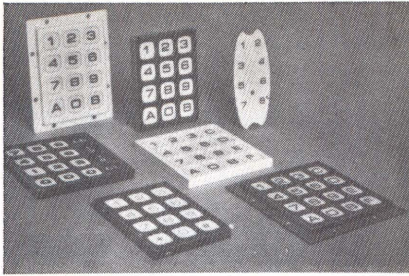
Std and custom Monopanel keyboards have no mechanical linkages. Layer construction incorporates a tough membrane with conductive rear surface which effects contact closure when moved approx 0.005″. Required touch sensitivity is 2 to 4 oz typ. Std series includes 12- and 16-position spst (1200 and 1600 series), black on white nomenclature, and black or white plastic bezel, with or without mounting flange. Contact rating is 50 mA at 30 Vdc, resistive load; max voltage, current, and power are 50 Vdc, 100 mA, and 1.5 W. **Centralab Electronics Div, Globe Union Inc,** 5757 N Green Bay Ave, Milwaukee, WI 53201.
Circle 230 on Inquiry Card

SINGLE-BOARD
TAPE CONTROLLER

A magnetic tape controller that combines PE and NRZ formats on a single board and fits a single slot in Data General Nova computers, the TC-120 includes board and tape drive cabling; it is also available as the TS-120, which includes tape drives and cabling in a fully integrated and tested system. Features include ability to mix up to eight 7- and 9-track NRZ, PE, or dual-density tape units in any combination, and 4-6-6 pack on 7-track, which allows the user to do core memory dump onto tape. **Western Peripherals Corp,** 2893 E La Palma, Anaheim, CA 92806.
Circle 231 on Inquiry Card

UNINTERRUPTIBLE
POWER SYSTEM

Claimed to provide 25% greater reliability than conventional step-wave designs, measured as MTBF, and more than 275% short-circuit current, the Delta-Y 3ϕ system can operate with 100% phase-load imbalance and still put out balanced voltage, can start heavier inrush loads without switching to alternate power lines, and can clear larger faults. Circuitry of the solid-state inverter and a sub-cycle static transfer switch uses approximately one-third fewer components to provide trouble-free service. Std capacities are 30 to 90 kVA; a 15-kVA model and capacities to 180 kVA also can be provided. **Cyberex, Inc,** 7171 Industrial Park Blvd, Mentor, OH 44060.
Circle 232 on Inquiry Card

DATA REGENERATOR/BUFFER
STORAGE

A char-by-char asynchronous data regenerator that can be expanded to perform speed and/or code conversion, serial-to-parallel conversion, or buffer storage by adding optional plug-in subassemblies, the model 1350 can be customized by the communications user to meet specific requirements through choice of PC card building blocks. Optional add-ons include end-of-message code detection, isolated polar-output keying, and a loop power supply. The unit interfaces between circuits employing std TTY signaling circuits. **Plantronics, Inc,** 385 Reed St, Santa Clara, CA 94301.
Circle 233 on Inquiry Card

1K BIPOLAR p/ROMS

Available as 6300-1 (open collector) and 6301-1 (3-state) commercial or 5300-1 (open collector) and 5301-1 (3-state) military versions, the 256 x 4 p/ROMs are fully pin-compatible with the company's H5200/6200 ROM-mates. Low power dissipation is claimed to cut power requirements without sacrifice in speed. Major characteristics of the part have been improved: fan-in is 0.25 mA max; and growback problems have been virtually eliminated. At least 95% of all units program to completion in 2 s. **Monolithic Memories, Inc,** 1165 E Arques Ave, Sunnyvale, CA 94086.
Circle 234 on Inquiry Card

NONIMPACT PRINTER MECHANISM
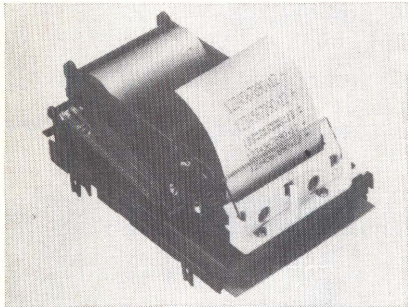
With 20-columns capacity, the NMP prints at 5 lines/s. Its stationary printhead uses 100 electrodes to form the 5 x 7 dot-matrix char. Features include noiseless discharge printing, variable char height, compact design, and automatic paper insertion. Applications include digital and alphanumeric printing for electronic calculators, point-of-sale terminals, test and measuring equipment, data logging and plotting. **Olympia USA Inc,** Box 22, Somerville, NJ 08876.
Circle 235 on Inquiry Card

HEAD-PER-TRACK DRUM MEMORY

Specifically applicable to dirty industrial environments, heads on the model 4000 automatically retract to avoid media contact if the drum slows to a point where air bearing is insufficient to fly them. The 9.5-megabit capacity unit has 128 data tracks with 8 min and 16 max spares. A set of clock tracks plus a spare set are switch selectable. Specs include 74,000 bits/track; 2.96-MHz bit rate at 2400 rpm; 12.5-ms access time; and error rates of 1 in 10^{11} bits transferred, recoverable; 1 in 10^{12} non-recoverable. **Vermont Research Corp,** Precision Park, N Springfield, VT 05150.
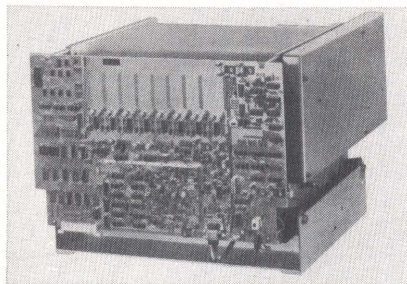
Circle 236 on Inquiry Card

COMPUTER TERMINAL MONITOR
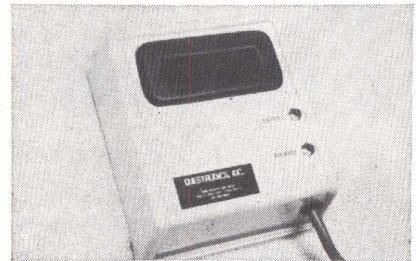
A dedicated microprocessor in this monitor processes and stores transaction information accurate to 0.1 s. On pushbutton command, min, max, and avg response times (0.1 to 9999 s) or number of transactions (0 to 9999) are shown on a 4-digit LED display. An optical coupler system permits attachments near the terminal without internal connections and without interference with terminal operation. An LED indicator shows loss of power. Time base is a crystal oscillator. Unit size is 2 x 5 x 6"; power requirement is 110 Vac at 60 Hz. **Questronics, Inc,** 3596 South 300 West, Salt Lake City, UT 84115.
Circle 237 on Inquiry Card

MODULAR KEYBOARD

Individually encoded keyswitches on low cost keyboard allow almost any key array to be assembled. Keyboard logic is independent of key array, resulting in a universal logic that will operate with a variety of keyboard configurations. Based on a photo-optic encoding technique, the design develops a fully encoded TTL-compatible output without logic. Hardwired logic is available to implement N-key lockout/2-key rollover error protection, while translating the internal code to the full ASCII char set plus 60 additional codes. However, the algorithms may be easily implemented in a microprocessor without significant memory or overhead requirements. Eliminating need for hardwired logic in this way further reduces keyboard costs. **Collimation, Inc,** 4206 Commercial Sq, Austin, TX 78745.
Circle 238 on Inquiry Card
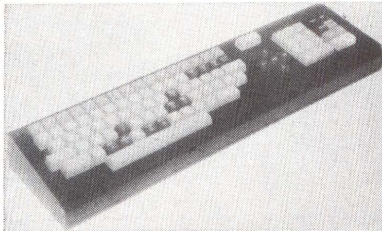
MICROPROCESSOR-CONTROLLED WIRING ANALYZER

A high speed analyzer for backplane panels, card racks, cables and harnesses, and other wired assemblies can be expanded in 64-node increments. Go/no-go indication of good or bad assemblies can be provided in 1 s for a 50,000-point back panel using a 65,000-node or test point system. Programming requires approximately 10 s for a 50,000-point assembly, when using a known-good unit and entering a developed program number into thumbwheel switches; the system can be programmed from an optional cassette or other external source. Go/no-go programming can be done using program number only. Errors are listed at a rate of 1 to 40/s, depending on the printer selected; a known-good unit or cassette input is required. System interfacing to backplane or card rack is accomplished with 2-sided interface cards similar to service-type extender boards; one end fits the user assembly while the other accepts a 72-pin PC connector mounted on a 64-point matrix I/O board. **Algorithm Technology, Inc,** PO Box 1910, Prescott, AZ 86301.
Circle 239 on Inquiry Card

300-CHAR/S TAPE READER

Previously rated at 150 char/s, 260 SAM, a photoelectric reader, has been rerated to 300 char/s. Without any adjustments, it will handle all std 6-, 7-, or 8-level tapes, center or advanced feedhole, paper, paper-polyester, or metallized-polyester. A single light source, fiber-optic distributor, and 9-element phototransistor sensing system perform the reading. A high performance stepping motor and dual-sprocket drive system transport tape through the read head at 0 to 300 char/s, asynchronous, bidirectionally, and stop on char. Dual-sprocket drive eliminates tape skew and assures positive data registration. Both motor drive and output electronic (TTL) functions are included in a single PCB assembly with one edge-board connector. **Decitek, a div of Jamesbury Corp,** 250 Chandler St, Worcester, MA 01602.
Circle 240 on Inquiry Card
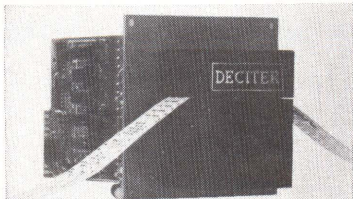
OPTICAL TAPE READERS

A rack-mount unit containing a 4023 optical tape reader and a 4014 servo tape spooler provides full tape handling capability for NC operations. Reader and spooler are designed for use in combination, but may be incorporated individually into any system. Std reader features are light transmissivity of up to 80%, ISO, typesetting, Japanese Telex tapes, and low error rate. Reading direction can be reversed at the desired char. Spooler features include a pushbutton for manual high speed spooling at an average speed of 1200 char/s. **Facit-Addo, Inc**, 501 Winsor Dr, Secaucus, NJ 07094.
Circle 241 on Inquiry Card

MICROMOTORS

Low inertia, zero-cogging dc servo motors provide high efficiency, long life, low noise, and rapid response. Features include stall torques up to 11.4 oz-in., mechanical time constant of 19 ms, and thermal resistance of 9°C/W. Suitable for driving 3M tape cartridges, the motors measure 2.6" long and are 1.378" in dia. **Hitachi America, Ltd,** 100 California St, San Francisco, CA 94111.
Circle 242 on Inquiry Card

SYNCHRONOUS OR STEPPING MOTOR

Low cost, instrument-grade model A motor provides 2-oz-in. output torque at the rotor shaft at 300 rpm. Hardened steel, broached gears and heat-treated steel pinions assure trouble-free gear-train operation at a rating of 150 oz-in. at 1 rpm. A selection of 12 gear-trains is offered, providing choice of speeds from 1 to 120 rpm. The unit is also available in a direct-drive model without gear-head at 300 rpm. **Hurst Manufacturing Corp**, Princeton, IN 47670.
Circle 243 on Inquiry Card

FUNCTION GENERATOR INTERFACE CARD
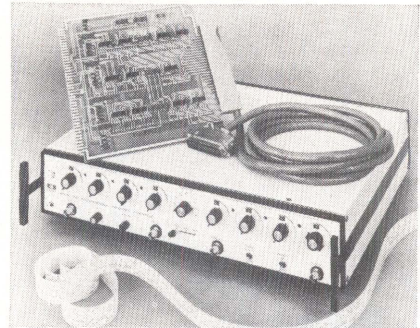
A plug-in and operate interface for model 605 and 606 programmable-function generators, the Model 67 interface card plugs directly into any I/O connector in H-P computers, supplying card, cable, connector, and software. The unit provides 44 binary outputs with storage and is DTL and TTL compatible. Each output bit is strobed with new data each time the subroutine EXACT is called; data are stored until it is recalled. **Dana Exact Electronics, Inc, sub of Dana Electronics, Inc,** PO Box 160, Hillsboro, OR 97123.
Circle 244 on Inquiry Card

MULTIMEDIA, ALPHANUMERIC PRINTERS
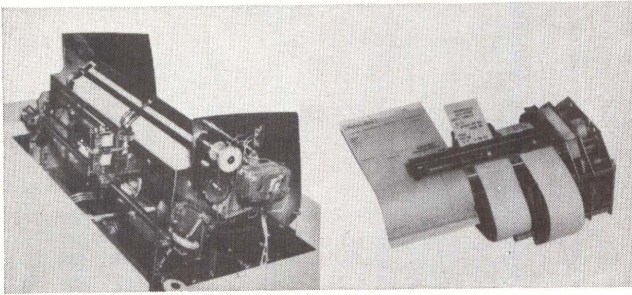
Simultaneously printing different data at each of three independently controlled stations, SV printers achieve 2 lines/s, using a segment matrix-char format. 64 char (10 numerals, 32 alphas, and 22 symbols) are provided. The unit accommodates roll papers and/or cut forms. Forms are inserted at the side, through an open throat, to allow for variable widths. A cartridge ribbon survives 3 million char impressions. Models 700/800, each with different external dimensions for applications flexibility, are 30-col serial units capable of printing up to 44 alphanumeric and special char at 37 char/s. Each can print on multi-copy, front inserted forms. Journal take-up spindle is std. **Sweda International, OEM Products,** 34 Maple Ave, Pine Brook, NJ 07058. Circle 245 on Inquiry Card

HYBRID LIGHT SENSORS

Complete subsystems combining the best qualities of silicon photodiodes and phototransistors with stable hybrid amplifier/digitizer microcircuitry in one package, Opto-Hybrid[R] sensors feature high photosensitivity with pre-adjusted thresholds, low impedance, DTL-, TTL-, MOS-compatible output. Circuitry is optimized to give a speed of response of <1 μs. Supply voltage is specified at 5 $\pm$0.25 Vdc; current requirement (max/channel) is 6 mA. Radiometric threshold values are 2.5, 1, 0.3, 0.03, 0.15, (H_{th}-min) and 10, 3, 1.2, 0.1, 0.6 (H_{th}-max) for OT100, 102, 104, 106A, and 108, respectively. Op temp range is 0 to 75°C; storage temp range is -55 to 125°C. Multichannel arrays with channel-to-channel matching are available on request. **Opto Technology, Inc,** 1001 E Touhy Ave, Des Plaines, IL 60018. Circle 246 on Inquiry Card

600-BAUD DATA TERMINAL
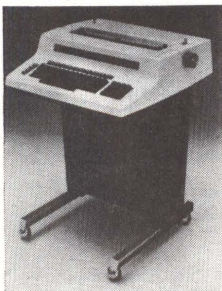
Based on the Qume printer mechanism, the 300-Q, a 30-char/s, wide-carriage impact terminal, features both interchangeable type fonts and snap-in/snap-out ribbon cartridges. 10- or 12-pitch printing is switch-selectable. The unit is available in a 600-baud configuration; 300-baud units in the field may be upgraded by exchanging printer mechanisms. Designed around a microprocessor controller, the terminal has both horizontal and vertical tabbing, super and subscripting, and half-line-feed controls. Proportional text mode allows variable spacing between char down to $1/120$ in. Multidirectional printing forward and backward, up and down is std, as are ASCII and IBM 2741 communication codes. **Gen-Com Systems, Inc,** 2306 Cotner Ave, Los Angeles, CA 90024. Circle 247 on Inquiry Card

MICROPROCESSOR PLOTTER CONTROLLER

MINICOMPUTER INFORMATION SERVICE

Datapro Reports on Minicomputers, a two-volume information service, provides prices, specifications, evaluations, and users' experiences with hundreds of minicomputer and microcomputer systems and their peripherals . . . and the companies that supply them. A useful tool for EDP system designers, mini users and equipment vendors. Information about a $10 trial subscription is available from **Datapro Research Corporation,** 1805 Underwood Blvd., Delran, NJ 08075.

CIRCLE 68 ON INQUIRY CARD

EDP INFORMATION SERVICE
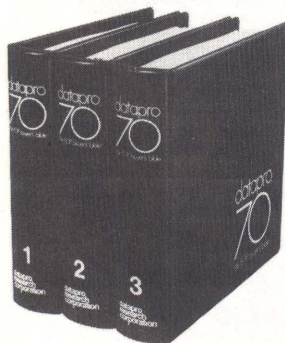
This three-volume EDP information service has become the most widely used in the world, with more than 2,300 pages and 10,000 users. Considered the first and only complete general-purpose information service on EDP hardware, software, services and suppliers, Datapro 70 includes product prices, specifications, operating characteristics, availability, and users' evaluations. Information about a $10 trial subscription is available from **Datapro Research Corporation,** 1805 Underwood Blvd., Delran, NJ 08075.

CIRCLE 69 ON INQUIRY CARD

Automatic detection and transmission error correction as well as increased host computer software efficiency are attained by use of a microprocessor in the PTC-5—with no changes in operating system software. The microprocessor also provides for local generation of alphanumerics, blocked format circular buffer, compressed plot codes, compatibility with wide range of data transmission rates, and implemented 2-way handshake procedure with FORTRAN-level plotting software. Data can be accepted from either EIA RS-232-C or TTY 20-mA loop data sources. **Houston Instrument, div of Bausch & Lomb,** 1 Houston Sq, Austin, TX 78753.
Circle 248 on Inquiry Card

DIGITAL OSCILLOSCOPE
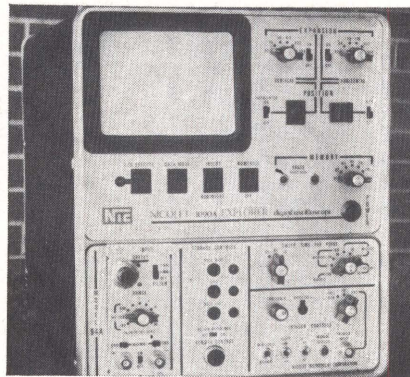
Using an ADC to digitize the input signal and store it in solid-state memory, the second-generation Explorer then reconstructs the stored signal by D-A conversion on the CRT. Storing the signal in memory, rather than on a CRT, allows the waveform to be manipulated during or after recording. Bandwidth is from dc to 5 MHz. Memory is 4096, 12-bit words, which may be used in halves or quarters. One- and 2-input plug-ins are offered with choice of single-ended or differential amps. **Nicolet Instrument Corp,** 5225 Verona Rd, Madison, WI 53711.
Circle 249 on Inquiry Card

INTERACTIVE DISPLAY TERMINAL

A high speed refresh type, interactive graphic display, system 32/2000 is fully buffered and requires no overhead in the computer for refreshing the CRT. It is available with optional 4-color presentation (red, orange, yellow, and green). Vector drawing speed is 1.4 in./μs. Char drawing speed is 4.8 μs avg. Std features include programmed char-generator (96 char and symbols in either ASCII or EBCDIC code), 4096 x 16-bit refresher core memory, 16-key function keyboard, and light pen. Options include interfaces to most 16- and 32-bit minicomputers. **Lundy Electronics & Systems, Inc,** Glen Head, NY 11545.
Circle 250 on Inquiry Card

MINIATURE PRECISION RESISTOR
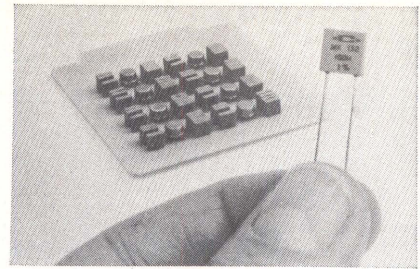
In values from 10 Ω to 100 MΩ in a std CK 06 case, type MK extended-range resistors feature std resistance tolerance of $\pm 1\%$; 0.75-W power rating at 125°C, with derating for operation at temps to 175°C; and tempcos of 50 ppm/°C for values up to 10 MΩ and 80 ppm/°C from 10 to 100 MΩ. Extended life stability is >0.05%/1000 hr typ. Max working voltage is 400 V. Used in resistive divider networks, all values will track to within 40 ppm/°C. **Caddock Electronics, Inc,** 3127 Chicago Ave, Riverside, CA 92507.
Circle 251 on Inquiry Card

FAST 4K STATIC RAM

Featuring complete cycle time of 400 ns, and worst-case access time of 225 ns, the 4200 is claimed to be the fastest TTL-compatible 4K static n-MOS RAM in production. Operating power is <150 mW; since normal V_{DD} can be reduced from 12 to 4 Vdc without risking loss of stored data, standby power consumption can be as low as 2 μW/bit. The memory is available in a std 22-pin DIP. **SEMI, Inc, a sub of Electronic Memories & Magnetics Corp,** 3883 N 28th Ave, Phoenix, AZ 85107.
Circle 252 on Inquiry Card

MINICOMPUTER TAPE CARTRIDGE UNIT

The TCP-1000 directly replaces the DEC TA-11 cassette tape system. Interfacing with the PDP-11 Unibus™, and software compatible with the TA-11, the unit uses 3M DC300A cartridges as storage media and the TCD-300 tape cartridge drive. Features include up to 20.5 megabytes of online storage; one to eight drives per controller; 6-kilobyte/s transfer rate; and 120-in./s independent rewind. **Three Phoenix Co,** 10632 N 21st Ave, Phoenix, AZ 85029.
Circle 253 on Inquiry Card

CARTRIDGE TAPE STORAGE SYSTEM
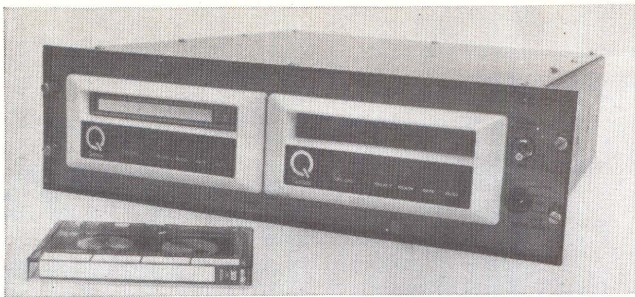
Incorporating 3M data cartridge and the company's model 600 tape drive with read-write speed of 30 in./s, rewind speed of 90 in./s, and packing density of 1600 bits/in. PE, the model 2200 can be provided with either one or two cartridge tape drives for storage capability of up to 5.76 million bytes in a dual-drive system. Drives are available with 1-, 2-, or 4-track read-after-write head. Each track is either computer selectable or manually selectable through a front-panel switch. Built-in ANSI-compatible tape formatter offers high speed search at 90 in./s, command chaining to emulate a disc where no computer interrupt is requested until the proper tape mark is found, hardware CRCC, and phase-encoding of data. Interfaces are available for PDP-11, Nova, Rolm, and Intel 8080 computers. **Qantex, div of North Atlantic Industries, Inc,** 200 Terminal Dr, Plainview, NY 11803.
Circle 254 on Inquiry Card

DUAL OUTPUT, BAUD RATE GENERATOR IC

An n-channel Coplamos^R LSI device, model COM 5016 simultaneously provides any 2 of 16 externally selectable clocked output frequencies required for asynchronous/synchronous data communication devices. Designed to provide universal asynchronous/synchronous receiver-transmitters (UARTs/USRTs) with a clock, the device replaces as many as 15 MSI chips. The only requirement in addition to external power is a crystal or TTL logic-level input frequency. Both timing chain and multiplexer are on the chip. Features include baud rates from 50 to 19,000; direct UART/USRT compatibility, reprogrammable ROMs for other than std frequencies; TTL and MOS compatibility; on-chip input pullup resistors; and accuracy to within 0.01% with 50% duty cycle. **SMC Microsystems Corp,** 35 Marcus Blvd, Hauppauge, NY 11787.
Circle 255 on Inquiry Card

SMART DATA TABLET DIGITIZER

Calcutizer line combines a proprietary data tablet with an advanced programmable calculator to provide a desktop graphic data processing system. Consisting of an integrated hardware and software package, Alpha/Tablet systems provide data tablets and digitizers with active areas from 11"-sq to 44 x 60". A series 200 calculator with printer, or an optional series 300 calculator are interfaced to the digitizer. The data tablet input mechanism features Cybergraphic technology, which is characterized by accuracy, high resolution, environmental immunity, stability, and simple design. **Talos Systems, Inc,** 7311 E Evans Rd, Scottsdale, AZ 85260.
Circle 256 on Inquiry Card

PRODUCTS

HYBRID MICROCIRCUIT SAMPLE/HOLD
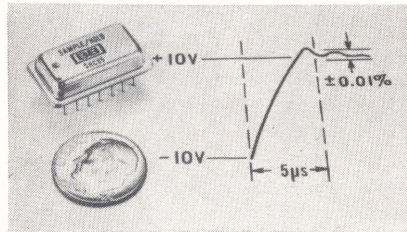
Housed in a 14-pin metal DIP case, the SHC85 acquires and holds up to ±10-V analog data to an accuracy of ±0.01% in 5 μs max. Feedthrough error is ±0.005% of the step-change at the input. Proprietary charge-offset and dielectric-absorption compensation circuits and drift-compensated amps provide throughput offset of 2 mV, 500-μV/ms droop, and ±2-ppm/°C gain drift over the 0 to 70°C op temp range. The unit consumes only 390 mW of ±15-Vdc power. Logic control input levels are TTL compatible. Output range is ±10 V with a drive current of ±10 mA. **Burr-Brown Research Corp,** Box 11400, International Airport Industrial Pk, Tucson, AZ 85734.
Circle 257 on Inquiry Card

PC BOARD PROCESSOR

The EXTRA 80 is compatible with the Intel 8080, yet provides enhanced speed and additional instructions. Hardware multiply/divide instructions are std; user-specified op codes can be added. The processor can execute an 8 x 8-bit multiply in approx 3 μs—about 40 times faster than the 8080. The LSI Schottky bipolar 3000 processor is available on an 8 x 9" PCB with an 86-pin connector. Features include single 5-V supply, 3-state outputs, 10 TTL loads, and TTL-compatible input. **Display & Decision Systems Ltd,** 80 Galaxy Blvd, Unit 11, Rexdale, Toronto, Ontario, Canada M9W 4Y8.
Circle 258 on Inquiry Card

BIPOLAR MICROPROCESSOR

Am2901 is the first of a family of low-power Schottky TTL circuits offering architectural and functional flexibility of MSI circuits with performance and cost advantages of LSI devices. A 4-bit microprogrammable data processor slice, containing an 8-function ALU; a 2-port, 16-word scratchpad memory; an additional accumulator register; and shifting and control logic, the Am2901 can execute a total of 12,992 instructions and performs a read-modify-write cycle in <100 ns. **Advanced Micro Devices Inc,** 901 Thompson Pl, Sunnyvale, CA 94086.
Circle 259 on Inquiry Card

6-DECADE COUNTER AND DISPLAY DECODER

A presettable, 6-decade synchronous, up/down counter/display driver with compare registers and storage latches, MK 50395N has multiplexed 7-segment and BCD outputs, and can count and display frequencies to 1 MHz. Counter contents can be transferred into the 6-digit latch, which is then multiplexed from MSD to LSD in BCD and 7-segment format to the outputs. The device interfaces directly with std CMOS logic families. **Mostek Corp,** 13300 Branch View Lane, Dallas, TX 75234.
Circle 260 on Inquiry Card

PROGRAMMABLE TICKET PRINTER
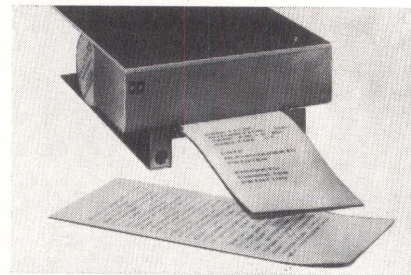
Model DMTP-5 will print alphanumeric information across the width of a std multi-part ticket with variable horizontal and vertical line pitch. Virtually any char or symbol can be printed in almost any position on the ticket, through programming. Operation is fully automatic, requiring that the operator present the ticket to the printer, where it is sensed, captured, and motor-driven to an internal stop. Print rate is approx 2 lines/s, assuming a 25-char line length. Data input is ASCII bit-parallel, serial, parallel-binary, or RS-232-C. **Practical Automation, Inc,** Trap Falls Rd, Shelton, CT 06484.
Circle 261 on Inquiry Card

MICRO DATA SYSTEM MODULE

Built around a single calculator chip, Procal-4, an externally programmable, micro data system, accepts BCD inputs from external keyboard, ROM, switch, or other source, performs arithmetic calculations (+, −, x, ÷), and provides outputs for printers, machine control functions, LED displays, D-A converters, or DPIs, supplying eight latched-BCD decades and a multiplexed 7-segment dynamic display decoder output. The system is TTL compatible and operates from a single 5-V supply. **Elcom Industries, Inc,** Civilian Terminal, Hanscom Field, Bedford, MA 01730.
Circle 262 on Inquiry Card

RETRO-REFECTIVE LED SCANNER
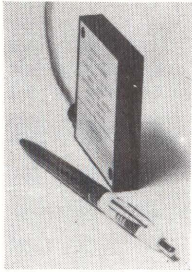
Model SP-510, an LED photoelectric scanner that operates with most photoelectric amplifiers, is totally solid-state for high reliability and long operating life. The LED light source never needs replacement, and will operate with any input voltage from 5 to 30 V. Operating range is up to 6 ft with a 3-in. retro-reflective target. Measuring ½" thick and 2½" square, the unit can be stacked in code reading applications or installed in restricted areas. Response time is <5 ms. Approximate range (using any of the company's B series amplifiers) is from 3 to 6 ft for a 3-in. retro-reflective disc, 1 to 2 ft for a 1-in. disc, and from 2 to 4 in. for a ¼ x ¼-in. retro-reflective tape. **Banner Engineering Corp,** 9714 Tenth Ave N, Minneapolis, MN 55441.
Circle 263 on Inquiry Card

TABLE-MOUNTED LOGIC CIRCUIT TESTER

Series 505 testers, in addition to 500-series features, offer console mounting to permit convenient access to printed wiring boards and troubleshooting aids, tilt-mounting for easy access to the control panel, remote-start switch to speed testing and troubleshooting, and a circuit board connector that can be rotated to three positions to permit full access to either side of the board. Providing comprehensive, automatic testing of all types of digital logic circuit boards, the system incorporates a microprogrammed test processor that executes test language instructions directly, resulting in clock and pin-change rates of up to 500 kHz. Programmed and pseudorandom test patterns are combined to comprehensively test either simple or complex boards having up to 223 edge pins. **Mirco Systems, Inc, a sub of Mirco, Inc,** 2106 W Peoria Ave, Phoenix, AZ 85029.
Circle 264 on Inquiry Card

SERVO-POSITIONING SYSTEM

The Index-Syn™ family of servo-positioning systems features a modular approach to positioning control, offering dc servo motors ranging up to 100-in.-lb in torque output and providing stepping rates to 100,000/s. Interfacing is identical to that associated with stepping-motor positioning systems. Preset servo indexers accept a parallel word command directly from computers and/or digital signals directly from thumbwheel switches or an optional keyboard for manual data entry. Buffered servo translator systems accept serial data command pulses without accel/decel ramp controls up to a specified max value. Electronically determined resolution may be selected within the 20- to 10,000-step/s range. **Control Systems Research, Inc,** 632 Fort Duquesne Blvd, Pittsburgh, PA 15222.

Circle 265 on Inquiry Card

PRODUCTS

SWITCHING POWER SUPPLY

A 5.25-V fully regulated supply, series "A" provides 105 W from a 100 to 130 Vac, 47-1 to 440-Hz line with only 35-W power loss. The conduction-cooled module measures 4 x 6 x 2¼", and weighs 2½ lb, providing double power density over similar-sized competitive units. Combined line/load regulation is ±10 mV from 2-A min. output current to full-load current of 20 A over full-line range. Output ripple is ±50 mV from all sources. **Etatech, Inc,** 187-M W Orangethorpe Ave, Placentia, CA 92670.
Circle 266 on Inquiry Card

FIXED-HEAD DISC MEMORIES

Featuring parallel data-channel operation and offering data rates up to 128 MHz (32-channels parallel), disc memories have capacities up to 40 megabits. Patented, fail-safe head lifting mechanisms eliminate disc/head contact during start and stop operations. Heads and discs are mounted in a dust-free, sealed chamber. Disc electronics are packaged on easily replaced 4½"-sq circuit cards. Std systems have 8.4-ms access time, optional ultra-fast access systems are available. **Alpha Data Inc,** 20750 Marilla St, Chatsworth, CA 91311.
Circle 267 on Inquiry Card

NC TAPE PREPARATION AND EDITING SYSTEM

The NC-7 permits high speed original typing, stores all typewritten material on tape, corrects errors electronically from the typewriter keyboard without erasing, and reads back the tape to produce perfect finished copy at speeds of >15.4 char/s. The typewriter is an IBM Selectric[R] specially modified to include the editing controls on the keyboard. The punch reader features all solid-state ICs for reliability and min maintenance. **International Computer Products, Inc,** 2925 Merrell Rd, Dallas, TX 75229.
Circle 268 on Inquiry Card

MODULAR MEMORY SUBSYSTEM

A modular subsystem of memory cards and systems controllers—STOR 10—enables DECsystem 10 computer users to configure and expand their memories in six ways: increase data ports from four to eight; 2- or 4-way interleaving; simultaneous access to any data ports; plug-in field expansion in 16K- or 32K-word increments; max storage capacity up to 4 million words; and rapid reconfiguring of size, data transfer rates, and throughput of main memory. Access/cycle times are 450/825 ns. **Cambridge Memories, Inc,** 12 Crosby Dr, Bedford, MA 01730.
Circle 269 on Inquiry Card

HIGH PERFORMANCE THIN PROFILE FAN
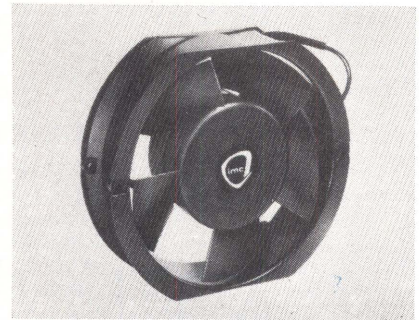
BT2907F IMCool tubeaxial fans meet requirements of increased power-density enclosures with typ operating point of 200 cfm at 0.18 Wg. Mounting requirements are 6¾ x 5²⁹⁄₃₂". Depth is 2". Free-air speed is 3400 rpm. MIL-B-23071/B environmental requirements are met. Specs for types 2516 and 2523 include 115/208 Vac, 400 Hz, 3φ, 45 W (free air), 0.7/0.35 A (free air), and 2.3 lb. Fan can be mounted inside or outside of equipment enclosure. **IMC Magnetics Corp,** 750 Main St, Westbury, NY 11591.
Circle 270 on Inquiry Card

LED INDICATOR MODULE

Designed for use with microprocessors as a control panel indicator, this module consists of eight red LEDs and TTL drivers, with a 4-LED unit optionally available. Interfacing is via ribbon cable and 14-pin DIP connectors with no soldering or wirewrapping. Power requirement is 5 V, with 20 mA per lighted LED (3.6-mA standby). Light output is 1.2 mcd/LED. Viewing angle is 80 deg. Overall dimensions are 5.9 x 1.1 x 0.75". **Electronic Solutions,** 8070 Engineer Rd, San Diego, CA 92111.
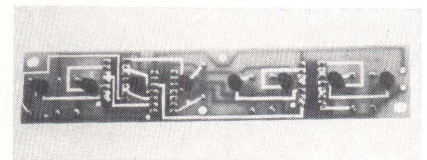
Circle 271 on Inquiry Card

MULTICHANNEL
DATA ACQUISITION SYSTEM

The Dataquire 7000, a microprogrammed data logger/acquisition system, comes equipped with 10 input channels and can be expanded to 1000, a 9-digit real-time clock with independent display, and a multirange timer that ranges from 0.1 s to 99 hr. Independent channel monitoring and random-channel skipping features are std and easily accessed at the front panel. The system can measure from $1 \mu V$ to ± 20 Vdc, as well as inputs from most thermocouples, RTDs, strain gages, and photomultipliers. Digital inputs from contact closures, BCD counters, or other instruments are also accepted. Output to any recording device (teleprinter, 9-track magnetic tape, paper tape punch) or external processor is possible directly or via phone line or terminal. **E-H Research Laboratories, Inc,** 515 11th St, PO Box 1289, Oakland, CA 94604.
Circle 272 on Inquiry Card
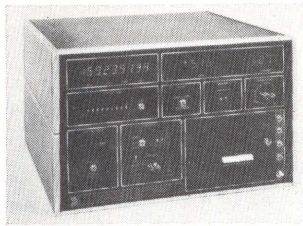
MICROPROCESSOR-GRADE POWER SUPPLIES
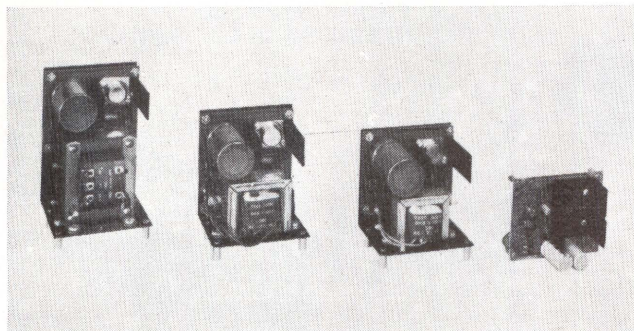
In addition to excellent regulation, open-frame modules feature short-circuit proof operation as well as over-voltage crowbar protection, which is essential to protect microprocessor and memory chips from being wiped out in the event of regulator failure. Specifically designed for chip sets such as Intel 8008 or 8080, Motorola M6800, or Fairchild F-8, the line provides 6 or 10 A at 5 V to operate a substantial memory bank as well as various special voltages. Models include MD-08—5 V at 6 A, −12, −9 V at 200 mA (for the 8008); -80—5 V at 6 A, −12, −5 V at 200 mA (for the 8080); -8—5 V at 6 A, 12 V at 200 mA (for the F-8); and -5—5 V at 6 A (M6800). **Scarpa Laboratories, Inc,** 46 Liberty St, Brainy Boro Station, Metuchen, NJ 08840.
Circle 273 on Inquiry Card

OPTICAL SWITCHES

Featuring hermetically sealed components for long-life operation in harsh environments, CLI-55 and -200 consist of IR LED emitter, coupled with either an npn phototransistor or npn photoDarlington sensor. Available with std gap widths of 0.1 or 0.25″ the switches can be custom-tailored to any size or width. The -55 develops 12-mA output current min; the -200, 1 mA, with rise or fall times as low as 5 μs. With 12″ leads, the -55 is suitable for bracket mounting; it can operate from either a 5- or 10-Vdc supply. The -200 is designed for PC-board mounting. Min reverse voltage of the emitter is 3 V for both; max forward voltage is 1.5 V. Min collector-to-emitter breakdown voltages of the sensor are 30 and 40 V, and max dark currents are 100 and 50 nA, for -55 and -200, respectively. Op temp range is −55 to 100°C. **Clairex Electronics, a div of Clairex Corp,** 560 S Third Ave, Mount Vernon, NY 10550.
Circle 274 on Inquiry Card

PRODUCTS

DUAL-DIGITAL FACSIMILE SYSTEM

Made up of recorder and digitizer at the receive terminal and scanner and digitizer at the transmit terminal, this system handles both ASCII and compressed digital facsimile signals over 3-kHz lines. It may be interfaced with computer, TTY keyboard, or floppy disc. ASCII signals are received at 1200 to 9600 bits/s; at 2400 bits/s, the receive terminal prints the equivalent of three 8½ x 11" pages/min. or compressed digital facsimile at 1½ min./page. **Alden Electronic & Impulse Recording Equipment Co, Inc,** Alden Research Center, Westborough, MA 01581.
Circle 275 on Inquiry Card

PROGRAMMABLE IN-LINE PACKAGE SWITCH
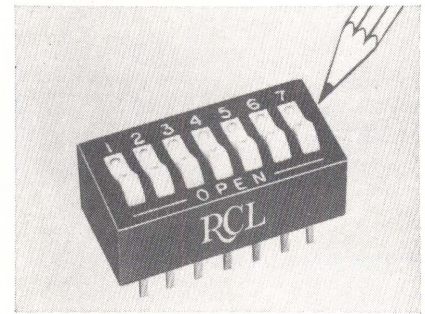
A 2-to-10 station miniature input device, the PIP switch is designed to replace slide, thumbwheel, and toggle switches. Std switching circuits or BCD coding applications include computer peripherals. Features include positive-detent, self-wiping action, long life expectancy, and wave solderability. Op temp range is from −40 to 190°F. Shock wave parameters are 20 g level, 11 ms duration, half-sine pulse shape. **AMF Inc, RCL Electronics Div,** 700 S 21st St, Irvington, NJ 07111.
Circle 276 on Inquiry Card

LOW SPEED ASYNCHRONOUS MODEM

T103A2/3 features abort timer, loss of carrier disconnect, and separate clear-to-send and data-carrier-detector interface leads. It is specifically designed for 2-wire, full-duplex operation over DDD or privately owned switched telephone networks. Speed is variable from 0 to 300 bits/s. Full-duplex operation is achieved on two bands, each with separate mark and space frequency; in operation, stations transmit and receive on opposite bands. **Rixon Inc, a sub of Sangamo,** 2120 Industrial Pkwy, Silver Spring, MD 20904.
Circle 277 on Inquiry Card

LITERATURE

CMOS Logic Circuits

54C/74C and CD4000 series are covered in 246-page paperback handbook that contains data sheets, specs, diagrams, charts, graphs, applications information, and a cross reference. **National Semiconductor Corp**, Santa Clara, Calif.
Circle 300 on Inquiry Card

CRT Monitor

Brochure describes aperture correction circuitry, switchable line rate, switchable video inputs, and video-inhibit control features, and provides detailed specs on the BH-15. **Electronic Display Div, Ball Brothers Research Corp**, St. Paul, Minn.
Circle 301 on Inquiry Card

Open-Frame dc Power Modules

Specs and dimensional diagrams for four DAPS series repairable, dual-output IC-regulated dc power modules are contained in data sheet. **Adtech Power, Inc**, Anaheim, Calif.
Circle 302 on Inquiry Card

Cabinet Air Conditioners

Guide discusses applications, selection, and operation of units, and provides schematic diagram, performance curves, and photos of rack- and rear-panel mounted units. **Kooltronic, Inc**, Princeton, NJ.
Circle 303 on Inquiry Card

OEM Power Supplies

Reference guide contains basic specs on 120 models ranging from 1200 mW to 750 W, including dual and triple output, high current, and PC card and encapsulated modules. **ACDC Electronics**, Oceanside, Calif.
Circle 304 on Inquiry Card

APL Applications Programs

Accounting, engineering, data-base management, financial planning, plotting, and statistical programs in the common libraries of the APL*PLUS time-sharing service are listed in catalog. **Scientific Time Sharing Corp**, Bethesda, Md.
Circle 305 on Inquiry Card

32-Bit Minicomputer

Features, performance, software instructions, and system diagrams of the model 8/32 Megamini™ are included in brochure. **Interdata, Inc**, Oceanport, NJ.
Circle 306 on Inquiry Card

Encapsulated Power Supplies

Catalog describing line of modular single, dual, and triple supplies includes a coupon which enables the customer to buy any two units and get a third free. **Calex Mfg Co, Inc**, Pleasant Hill, Calif.
Circle 307 on Inquiry Card

ATE Systems

Catalog discusses required features, covers factors in determining cost-of-ownership, and contains chart listing specific features available with each model of the System 390. **Instrumentation Engineering, Inc**, Franklin Lakes, NJ.
Circle 308 on Inquiry Card

Microprogrammable Video Display Terminal

Brochure contains chart listing key operating features with associated advantages for five main application categories. **Delta Data Systems Corp**, Cornwells Heights, Pa.
Circle 309 on Inquiry Card

Intelligent Terminals

Brochure covers utilization of Diskette 1100 and Cassette 1100 systems for data entry and communications and as independent processing stations. **Datapoint Corp**, San Antonio, Tex.
Circle 310 on Inquiry Card

Programmable Controller

Operating features, programming steps, and technical specs of the UMAC PC1200 series for automating and monitoring industrial machines and processes are provided in bulletin. **Sperry Vickers, a div of Sperry Rand Corp**, Burlington, Vt.
Circle 311 on Inquiry Card

Miniature, Subminiature Switches

Catalog provides photos, line drawings, and specs on 300 different slide, snap-action, rotary, pushbutton, leaf, rocker, and paddle switches. **Chicago Switch, Inc**, Chicago, Ill.
Circle 312 on Inquiry Card

Data Conversion Modules

Line of A-D and D-A converters, sample/holds, and analog multiplexers is covered in brochure, which lists key specs for each module. **Datel Systems, Inc**, Canton, Mass.
Circle 313 on Inquiry Card

CRT Terminals

Modular logic systems, high resolution scan display, firmware, keyboard, and packaging of the 2640A are described in the *Hewlett-Packard Journal* along with reports on its operation, design, and functions. **Hewlett-Packard Co**, Palo Alto, Calif.
Circle 314 on Inquiry Card

Militarized Mass Memory

Model CL107, a fully militarized controller and rotating disc memory which provides 8 million words of storage, is presented in brochure with performance specs and installation data. **The Singer Co, Librascope Div**, Glendale, Calif.
Circle 315 on Inquiry Card

Hard-Sector Formatting

Method of configuring a hard-sectored format for FD400 and -500 flexible discs is discussed in application note, which describes parameters contributing to sector format timing. **Pertec Corp, Peripheral Equipment Div**, Chatsworth, Calif.
Circle 316 on Inquiry Card

Photoelectric Control

Product sheet lists features, typ applications, specs, and mounting dimensions for the FE-MLS5A, and includes a functional schematic and distance-vs-beam size diagram. **Micro Switch, a div of Honeywell Inc**, Freeport, Ill.
Circle 317 on Inquiry Card

32-Bit, Medium-Scale Computer

Detailing advances in data-handling software and hardware, brochure describes 6024/4 and reports on energy management, weather data gathering, and electronic editing applications. **Harris Corp**, Cleveland, Ohio.
Circle 318 on Inquiry Card

Custom-Designed CRTs

Brochure describes and pictures prototype and production facilities for high performance CRTs as well as quality assurance procedures to meet customer requirements and mil specs. **Raytheon Co, Industrial Components Operation**, Quincy, Mass.
Circle 319 on Inquiry Card

Digital Process Computers

A guide for specifying, testing, and demonstrating hardware performance of process computers, ISA Recommended Practice MC8.1 contains tests and procedures for subsystems and system parameters as well as a glossary of terms. Copies are available at $7 each from **Instrument Society of America**, 400 Stanwix St, Pittsburgh, PA 15222.

Process Control System

Booklet describes VupaK III, which provides online, real-time data acquisition and process control of plant operations in small- to medium-sized industrial applications. **Honeywell Inc, Process Control Div,** Phoenix, Ariz.
Circle 320 on Inquiry Card

Synchros and Resolvers

Characteristics for size 8 and 11, single-speed; size 11, 2-speed; and a size 18, 10-speed unit are tabulated in brochure with supplementary outline drawings and wiring schematics. **Kearfott Div, The Singer Co,** Little Falls, NJ.
Circle 321 on Inquiry Card

3340-Compatible Data Modules

Discussing reliability and performance of Data Mark 70/70F disc packs, brochure also describes disc-substrate preparation, proprietary disc coating and oxide particle alignment technique, and surface shield performance. **Memorex Corp,** Santa Clara, Calif.
Circle 322 on Inquiry Card

Data Communications Products

Test sets for low and medium speed asynchronous, medium and high speed synchronous, and Bell 300 series or equivalent wideband modems, as well as time and frequency division multiplexers are included in catalog. **International Data Sciences, Inc,** Providence, RI.
Circle 323 on Inquiry Card

High Speed Data Transfer Unit

Operational features of the Lineplexer II, which provides full-duplex data communication at rates to 19,200 bits/s over two independent voice-grade channels, are described in brochure. **International Communications Corp,** Miami, Fla.
Circle 324 on Inquiry Card

Circular Connector with Twist-Pin Contacts

Bulletin describes MD73, which uses center-to-center contact spacing of 0.065", enabling 91 contacts to be mounted in a 15 shell size. **Malco, a Microdot co,** South Pasadena, Calif.
Circle 325 on Inquiry Card

LSI Board Test System

Including diagrams of hardware and software and complete system specs, brochure describes typ memory testing as well as real-time random logic testing with the MD-107. **Macrodata Corp,** Woodland Hills, Calif.
Circle 326 on Inquiry Card

Side-Panel Mounting Miniature Connector

"Handbook of Standard Connectors" features GF series connector, which will obtain either male or female contacts or both, positioned for customer requirement. **Positronic Industries, Inc, Connector Div,** Rogersville, Mo.
Circle 327 on Inquiry Card

Linear Circuit Test System

Listing major features of the J273B, brochure discusses many tests that can be performed on each device family as well as its applications in wafer test, final test, manufacturing quality control, component evaluation, and incoming inspection. **Teradyne, Inc,** Boston, Mass.
Circle 328 on Inquiry Card

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the page on which the item appears—not the reader service number. Please do not circle the page number on the reader service card.

It's all over.

Surprisingly enough, the best kept secret in town was patented over eight years ago. That's right. ICC is the largest and oldest independent manufacturer of light pens in the world. So we can offer performance at the right price — right off-the-shelf.

Our fast-response pens work well with vector and alphanumeric computer graphics, radar displays, automated signs, IC mask or schematic designs, and even color graphics.

So if you're looking for light pens, your search is over. Information Control Corporation, (213) 641-8520.

LIGHT PEN SERIES 200
LIGHT PEN SERIES 300
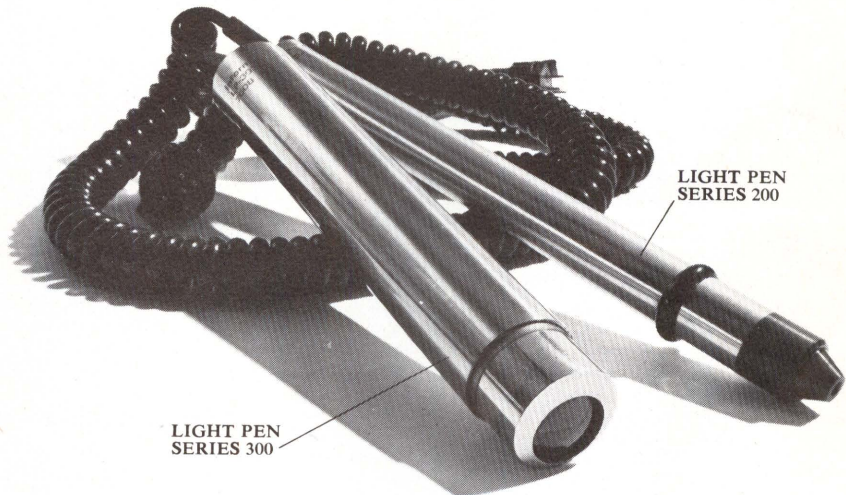
FREE. Go for it.

Send us this coupon now. We'll send you our "Understanding Light Pens" book.

Name_____ Date_____
Company_____ Phone_____
Address_____
City/State/Zip_____
ICC, 9610 Bellanca Avenue, Los Angeles, California 90045