COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

MAY 1977

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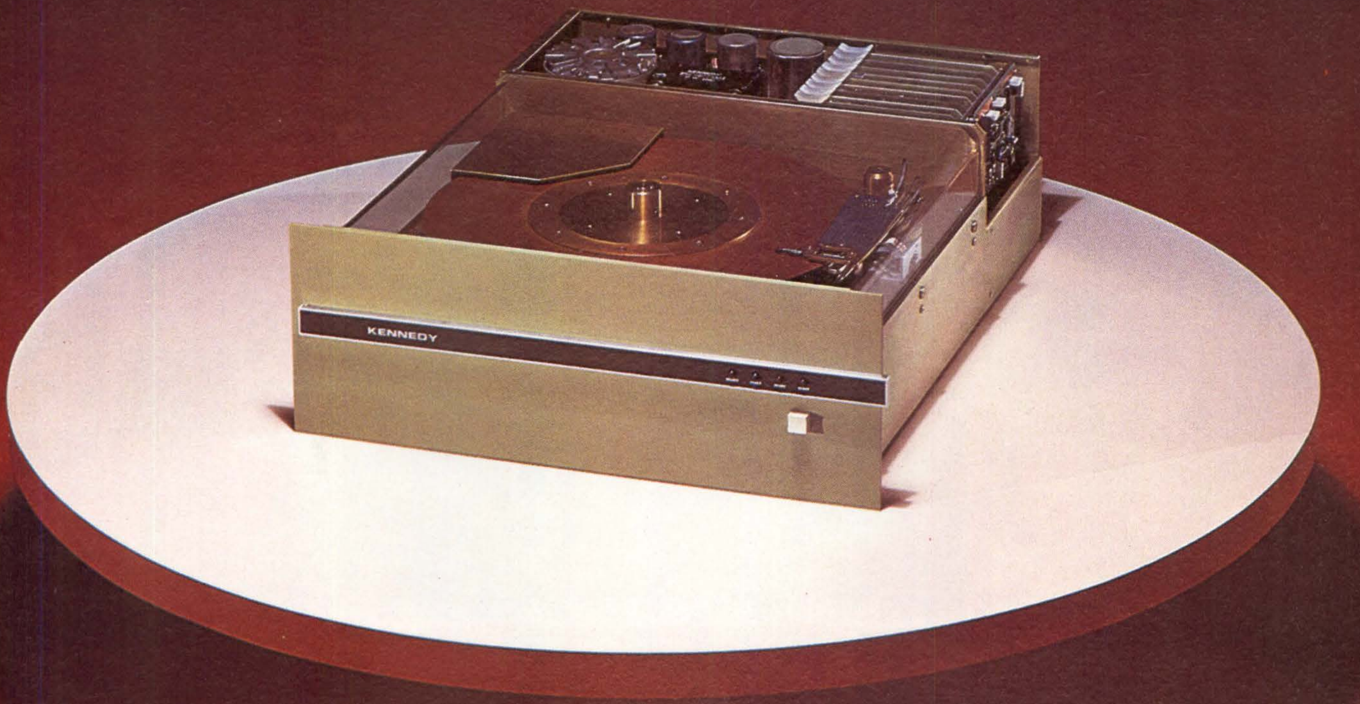

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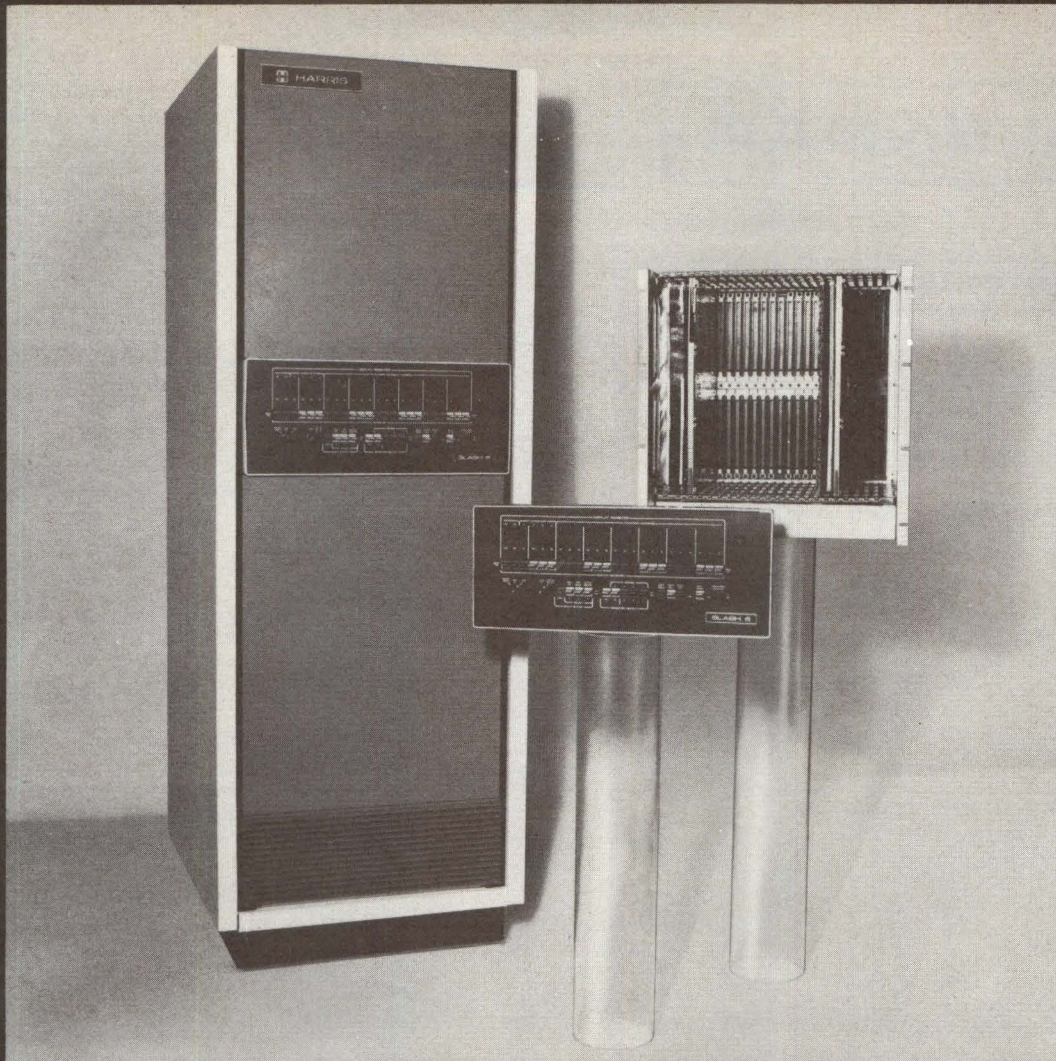

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CALENDAR

CONFERENCES

MAY 24-26—Sixth Annual Sym on Incremental Motion Control Systems and Devices, Urbana, Ill. INFORMATION: Dr B. C. Kuo, U of Illinois, Dept of Electrical Engineering, Urbana, IL 61801. Tel: (217) 333-4341

MAY 24-27—PICA-77 (Power Industry Computer Application Conf), Toronto, Canada. INFORMATION: IEEE, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

MAY 24-27—Seventh Internat'l Sym on Multiple-Valued Logic, Charlotte, NC. INFORMATION: Dr C. M. Allen, Sym Chm, Engineering Analysis and Design Dept, U of North Carolina at Charlotte, Charlotte, NC 28223. Tel: (704) 597-2302

MAY 24-26, MAY 31-JUNE 2, and JUNE 7-9—Computer Caravan, Philadelphia, Pa; Washington, DC; and Boston, Mass. INFORMATION: John C. Forbes & Associates, One Hilltop Rd, Winchester, MA 01890. Tel: (617) 729-9244

JUNE 2—16th Annual Technical Sym, Nat'l Bureau of Stds, Gaithersburg, MD. INFORMATION: Dr Stuart Katzke, Rm A-265, Technology Bldg, National Bureau of Stds, Washington, DC 20234. Tel: (301) 921-3861

JUNE 6-8—Pattern Recognition and Image Processing, Rensselaer Polytechnic Institute, Troy, NY. INFORMATION: Gen'l Chm, Prof H. Freeman, Dept of Electrical and Systems Engineering, Rensselaer Polytechnic Institute, Troy, NY 12181. Tel: (518) 270-6311

JUNE 6-9—15th Internat'l Magnetics Conf, Los Angeles, Calif. INFORMATION: Gen'l Chm, Geoffrey Bate, GPD Laboratory, IBM Corp, PO Box 1900, Boulder, CO 80302. Tel: (303) 447-5634

JUNE 10—Computerfest '77 (2nd Annual Midwest Regional Computer Conf for Hobbyist Computing), Cleveland, Ohio. INFORMATION: Gary Coleman, President, Midwest Affiliation of Computer Clubs, PO Box 83, Cleveland, OH 44141

JUNE 12-15—Internat'l Conf on Communications, Chicago, Ill. INFORMATION: Edward J. Glenner, Systems Research, GTE Automatic Electric Labs, PO Box 2317, Northlake, IL 60164. Tel: (312) 562-7100

JUNE 13-16—NCC (Nat'l Computer Conf), Dallas Convention Ctr, Dallas, Tex. INFORMATION: AFIPS Headquarters, 210 Summit Ave, Montvale, NJ 07645. Tel: (201) 391-9810

JUNE 18-19—Personal Computing Show, Boston, Mass. INFORMATION: Personal Computing, Conf and Exposition Mgmt Co, Box 844, Greenwich, CT 06830

JUNE 20-22—14th Design Automation Conf, New Orleans, La. INFORMATION: Gen'l Chm, Judith G. Brinsfield, Bell Laboratories, Rm 3B-323, Whippany Rd, Whippany, NJ 07981. Tel: (201) 386-3169

JUNE 20-22—IFAC/IFIP Real-Time Programming Workshop, Eindhoven, The Netherlands. INFORMATION: C. H. Smedema, Philips Research Laboratories, Eindhoven, The Netherlands

JUNE 21-23—31st Annual Convention of Armed Forces Communications and Electronics Assoc (AFCEA), Washington, DC. INFORMATION: Judith H. Shreve, Editor, AFCEA, Skyline Ctr, 5205 Leesburg Pike, Falls Church, VA 22041. Tel: (703) 820-5028

JUNE 22-24—Joint Automatic Control Conf, San Francisco, Calif. INFORMATION: Prof J. Meditch, Dept of Electrical Engineering, U of Washington, Seattle, WA 98195. Tel: (206) 543-2170

JUNE 28-30—Internat'l Sym on Fault-Tolerant Computing, Los Angeles, Calif. INFORMATION: Prof A. D. Friedman, Dept of Electrical Engineering and Computer Science, U of Southern California, Los Angeles, CA 90007

JULY 24-29—ISA Sym for Innovation in Measurement Science, Hobart/Smith College, Geneva, NY. INFORMATION: Peter Vestal, Instrument Society of America, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

JULY 28-29—AMC-Pacific 77, San Jose, Calif. INFORMATION: Peter Szego, Ampex Corp, Mailstop 3-22, 401 Broadway, Redwood City, CA 94063. Tel: (415) 367-3126

AUG 8-12—IFIP Congress 77 (Internat'l Federation for Information Processing), Toronto, Canada. INFORMATION: Robert C. Speiker, U.S. Committee for IFIP Congress 77, Registration and Accommodations, Western Electric Co, 222 Broadway, New York, NY 10038

AUG 23-26—Internat'l Conf on Parallel Processing, Bellaire, Mich. INFORMATION: Dr Charles S. Elliot, College of Engineering, Wayne State U, Detroit, MI 48202. Tel: (313) 577-3812

SEPT 6-8—7th Internat'l Congress on Instrumentation in Aerospace Simulation Facilities, Royal Military College of Science, Shrivenham Wiltshire, England. INFORMATION: Gen'l Chm, 7th ICIASF, P W W Fuller, R31 RARDE Fort Halstead, Sevenoaks Kent, England

SEPT 26-28—Internat'l Electrical Electronics Conf and Exhibition, Toronto, Canada. INFORMATION: Internat'l Electrical Electronics Conf and Exposition, 1450 Don Mills Rd, Don Mills, M3B 2X7, Canada

OCT 3-6—EUROMICRO Sym, Amsterdam, The Netherlands. INFORMATION: Ted Holtwijk, Philips Elcoma, Bldg BAE 2, NL-Eindhoven, The Netherlands

JUNE 7-8—The Market Effect and Impact of Digital Transmission, New York, NY. INFORMATION: The Yankee Group, PO Box 43, Cambridge, MA 02138. Tel: (617) 742-2500

JUNE 10-12—Bench Programming of Microprocessors Workshop, Philadelphia, Pa. INFORMATION: Helen B. Yonan, Philadelphia IEEE, Moore School, University of Pa, Philadelphia, PA 19174

JUNE 13-15—Minicomputers; JUNE 27-29—Laser Beam Information Systems, Toronto, Canada; New York, NY. INFORMATION: Heidi Kaplan, Information Services Mgr, New York Mgmt Ctr, 360 Lexington Ave, New York, NY 10017. Tel: (212) 953-7262

SHORT COURSES

MAY 23-27—Computer-Aided Process Planning, Cambridge, Mass. INFORMATION: CAPP Course, Society of Manufacturing Engineers, 20501 Ford Rd, PO Box 930, Dearborn, MI 48128. Tel: (313) 271-1500

JUNE 6-8—Computer Science and Engineering Curricula Tutorial and Workshop, Williamsburg, Va. INFORMATION: Dr David C. Rine, Workshop Chm, Computer Science, University of Texas, San Antonio, TX 78285

JUNE 7; JUNE 21—Microprocessor Project Management: Design, Manufacturing, QA, and Field Service; JUNE 8; JUNE 22—Microprocessors/Microcomputers: A Comprehensive Technical Introduction and Survey; and JUNE 9-10; JUNE 23-24—Hands-On Microcomputer Programming Workshop, Philadelphia, Pa; San Diego, Calif. INFORMATION: Enrollment Secretary, Integrated Computer Systems, Inc, 4445 Overland Ave, Culver City, CA 90230. Tel: (213) 559-9265

JUNE 13-17—Mini/Microcomputer Systems: A Close Look at Mini/Microcomputers and Their Applications to Real World Problems, MIT, Cambridge, Mass. INFORMATION: Director of the Summer Session, Rm E19-356, Massachusetts Institute of Technology, Cambridge, MA 02139. Tel: (617) 253-2101

JUNE 13-24—Computer Techniques for Real-Time Control and Monitoring of Power Systems, Madison, Wisc. INFORMATION: Willis F. Long, Program Director, Dept of Engineering, U of Wisconsin-Extension, 432 N Lake St, Madison, WI 53706. Tel: (608) 262-2061

JUNE 15-17—Microcomputers/Microprocessors in Instrumentation Systems, Baton Rouge, La. INFORMATION: Dr J.L. Hilburn, Electrical Engineering Dept, Louisiana State U, Baton Rouge, LA 70803. Tel: (504) 388-5241

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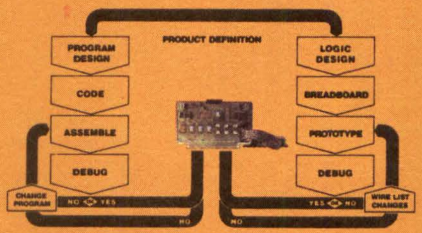

prototype; if the software is to be executed on an 8080 in the prototype, for example, an 8080 micropressor chip is used in the emulator processor.

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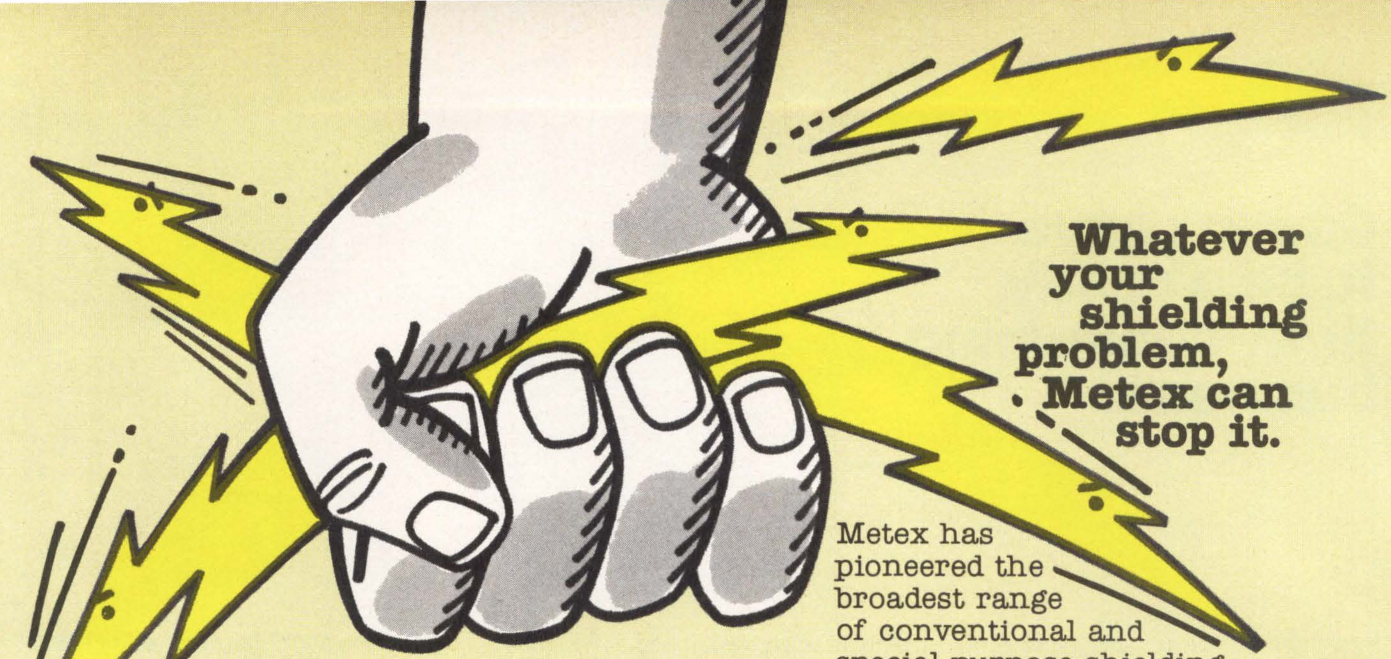

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CIRCLE 10 ON INQUIRY CARD

by John E. Buckley
Telecommunications Management Corp
Cornwells Heights, Pa.

Terminal Storage Systems

The evolution of remote data terminals has been stimulated over the past decade by parallel developments in both component technology and interactive data processing applications. It is reasonable to expect that over the next 10 years, this continued development of terminals and associated applications will be stimulated further by developments of remote data storage capabilities. Early data communication terminals before the advent of the computer were usually direct keyboard entry devices. Early message switching teletypewriters required the terminal operator to directly activate the associated communications line from the keyboard of the terminal. Later, introduction of a terminal storage medium in the form of paper tape improved the transmission efficiency of the associated communication line. Pre-storing data to be transmitted and then transmitting at an automated and consistent rate permitted more terminals to share a common communication channel.

When the first communications computer systems were introduced, remote processing became a major terminal application in which the RJE (remote job entry) terminals were basically an extension of the standard computer I/O peripherals with communications capability. Development and subsequent popularization of interactive information systems caused the remote data terminal to return to direct line entry devices, but with an increased need to store data at the remote location.

Today's major requirement for remote data terminals is in this area of interactive or direct entry applications. The need for practical local storage at the remote terminal site is one of the more important impediments to the future development of interactive data applications.

This need has been further accentuated by the introduction of microprocessor technology to the remote terminal. A microprocessor associated with the remote data terminal is essentially useless unless it is supported by a working memory and has access to a peripheral data storage device. While the same basic components may be used to provide a terminal with both memory and storage, their definitions are considerably different. Memory can be considered the medium within which instructions or computations can be executed on a dynamic basis. A microprocessor and its associated working memory are referred to as a microcomputer; use of that working memory to store data is neither operationally nor economically practical. Data storage can be considered a medium in which bulk data or instructions can reside.

Peripheral data storage has typically been provided by mechanical storage devices which include paper tape, magnetic tape in the form of cassettes or reels, and fixed or removable disc files. Extensive use of these traditional devices creates a disproportionate terminal cost when the cost of the required storage support mechanisms and electronics are considered. For this reason, remote data terminals have made limited use of these data storage peripherals. Practical peripheral storage to a remote data terminal is static storage rather than the conventional movable storage device. Static storage can be either removable or fixed as required by the associated terminal and its intended application. There are basically four major types of static data storage available: magnetic cores, random access memories (RAMs), charged-coupled devices (CCDs), and bubble memory.

Magnetic cores, comprising the most familiar storage devices, have been used almost exclusively for traditional computer memories since the early 1950's. Today's magnetic core technology provides the system designer with reliable storage at a price of approximately $\frac{4}{10}$ of a cent per bit. Magnetic cores offer a considerable advantage in that they can be structured on either a random-access or direct-addressing basis. Data stored in the specific location within a magnetic core array can be accessed by directly addressing that portion of the array. In addition, a storage device based on magnetic cores is non-volatile—loss of external power does not destroy the magnetic field in each of the individual cores which represent the stored data bits.

A significant disadvantage is its destructive read characteristic. In order to read stored information within such a device, the magnetic cores containing the data will be neutralized when the read function takes place. It is therefore necessary that the peripheral electronics associated with this memory have both read and write capability. When a particular segment of information is read from storage, that same information must be written back into storage in order to preserve the data. The speed of a magnetic core storage device is typically in the magnitude of 100 ns per read or write function. If a nondestructive read is desired, the associated electronics must perform both a read and write function resulting in an increased overall access time.

With the evolution of metal-oxide semiconductor (MOS) technology, the development of RAM arrays has produced a data storage alternative. Due to the many variations of RAMs today, the typical cost of this memory is approximately one-half that of a corresponding magnetic core array. RAMs also exhibit the random or direct access capability of selecting data to be read or stored. Unfortunately, a RAM is typically a volatile storage device. If external power is interrupted or removed, the stored data content is lost. However, peripheral power devices can be applied to preserve the stored data in the event that primary power is no longer available. Major advantages of RAMs are nondestructive read characteristics and high access speed. Data from a RAM can be read in one-third the time required for a magnetic core array.

One of the more promising terminal storage systems is the CCD, which assures a storage cost with at least an order of magnitude improvement over magnetic core arrays. CCDs could provide the same storage capacity as magnetic cores at a cost of about $\frac{5}{100}$ of a cent per bit, and they also can be expected to further decrease in cost as associated manufacturing volumes increase. Magnetic core technology on the other hand, can be viewed as exhibiting an essentially level cost per bit. CCDs, like RAMs, are volatile storage devices. Also, a read function from a CCD does not destroy data. This nondestructive read of the CCD tends to simplify its required I/O electronics as compared to control electronics necessary for magnetic core arrays.

CCDs, however, are not random access; they are serial storage devices similar in function to the traditional delay line. Effectively operating as an extensive shift register, the CCD must cycle data through a read point (or points) in order to access the desired stored information. While storage cost is attractively low, the associated control electronics could easily become significant if any extensive attempt is made to compensate for the serial read characteristics. Information can be read from CCDs at a typical rate of 100 ns per bit. This particular parameter, however, cannot be properly compared with other storage alternatives until the maximum access or latency time of a particular CCD array is determined. Maximum latency time is defined as the maximum time required to reach a particular stored bit. If a CCD storage system has a capacity of 64k bits, the maximum latency or access time would be 6.4 ms. The access methodology applicable to traditional mechanical storage devices such as magnetic discs is that actual read time is typically minor compared to associated search time.

A recent potential entry into terminal storage systems is the bubble memory. These devices are similar to CCDs in that they function as shift registers, and exhibit a comparable per bit storage cost. They feature nondestructive read, and if an external magnetic field is maintained, they are also nonvolatile. One known disadvantage is that they typically exhibit a per bit read or write time approximately four times greater than CCDs. At the present time, bubble memory technology has had relatively low manufacturing experience, and to date has exhibited a low manufacturing yield. These negative aspects, however, should be considered as transient characteristics. Further development and application demand for such devices will produce greater experience; hence more reliable manufacturing techniques can be expected. If market acceptance increases, present manufacturing yield statistics can also reasonably be expected to increase.

These four generalized storage technologies are presently competing to become established as tomorrow's standard terminal storage system. The availability of such low cost and reliable terminal storage should lead to additional applications being implemented using remote data terminals. The system designer must recognize that this lower cost objective for a terminal storage system encompasses both the direct costs of the storage media as well as the cost of the supporting electronics. Characteristic of the past evolution of data terminals, as new capabilities become economically practical, applications that had previously been disregarded can now come into the realm of viable automation.

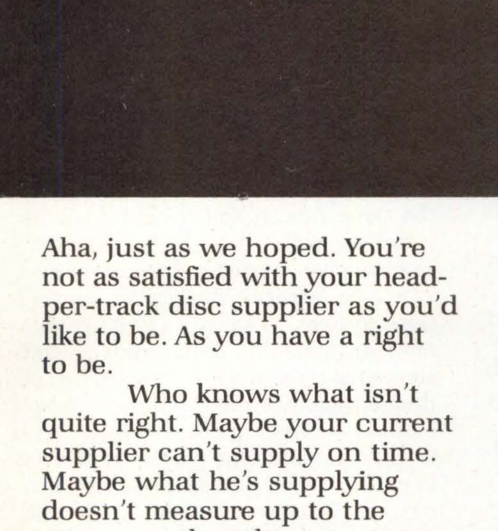
It is also feasible that the advent of such low cost terminal storage systems when coupled with microprocessor technology will cause many application functions to be properly relegated to the remote data terminal. As discussed in previous columns, many tasks presently performed by the central processing software systems have been assigned to it because the remote data terminal cannot economically perform these functions. As more intelligence can be resident within the remote data terminal associated with a large capacity/low cost remote terminal storage capability, many of these functions can be removed from the overhead of the central processor. With such a change of functional responsibility, a corresponding benefit is that the volume of data traditionally exchanged between the remote terminal and central processing system can also be significantly reduced.

The ideal objective of an information system is to permit the remote data terminals to function as a demand data entry interactive device and yet permit the associated data communications network and centralized processing system to operate in a scheduled batch system. It is more accurate to refer to these systems as segment oriented. The central processor and associated network can operate under centralized control in a scheduled environment to exchange and process the data segments of the application. Remote data terminals, however, operate with the appearance of direct data entry and interaction, and yet essentially function independent of the network and centralized processing system. Primary interaction at the terminal is limited to the terminals' local storage system, which is the entity that actually interfaces to the network. By limiting the network and processing system to data segment processing, overall system efficiency and reliability can be significantly improved. The remote data terminal operator can typically perform the application tasks, regardless of the condition and activity existing within the associated network and centralized processing system at that specific point in time. The major advancement that is necessary in order to implement and operate these dual-personality information systems is the availability of low cost, reliable terminal storage systems using one of the previously discussed technologies.

Everyone totally happy with their head-per-track discs may go on to the next page.

Aha, just as we hoped. You're not as satisfied with your head-per-track disc supplier as you'd like to be. As you have a right to be.

Who knows what isn't quite right. Maybe your current supplier can't supply on time. Maybe what he's supplying doesn't measure up to the specs you thought you were buying. Maybe he's conducting his business as if these were the last few days he's going to be in the business.



But what can you do? You're locked into existing designs and production deadlines. And changing suppliers in midstream could put you up that proverbial creek without a paddle, right?

Wrong.

Now you can make a change for the better with very little change to what you're doing right now. By changing to AMCOMP.

That's because our 8400 and 8500 Series Disc Memory Systems come complete with the interfacing that makes them readily-adaptable to your present controller.

And our systems aren't just readily-adaptable; they're better systems to adapt to. Performance that's engineered in before production, and quality that's maintained throughout manufacturing. It's a part of what's making AMCOMP the new standard by which the industry judges itself.

Judge for yourself. Just contact your nearest AMCOMP office, or AMCOMP, INC., 686 West Maude Avenue, Sunnyvale, CA 94086, phone (408) 732-7330.

Now, aren't you happy you didn't turn the page?

AMCOMP

CIRCLE 12 ON INQUIRY CARD

Major Innovations and Product Additions Provide Expanded Service

Innovations involving the leasing/selling and service of ADDS CRTs, Vadic modems, and TermiNet[R] printers, together with the expansion of the company's TermiNet line to include several other products, are designed to provide extended service to users of remote terminals and associated peripheral equipment. Originally servicing TermiNet printers, the General Electric service organization is part of the company's Apparatus Service Div which provides complete repair and maintenance service nationwide.

To minimize terminal downtime, GE retains the concept of performing onsite repairs by having the technician bring a complete set of spare parts for a specific type of terminal. Dispatch and coordination of service people is handled locally.

The TermiNet line has been expanded to include various line printers with several interfaces, employing the company's rotating printbelt concept. A lower speed matrix printer, the TermiNet 30 has a 7 x 9 dot matrix capability in either 80 or 132 character lines. It features impact print with multiple carbon copies.

Enhancements include single or dual magnetic tape accessory with full search and edit features, dual modem option in both originate-only and originate-answer at three lower transmission rates and 1200 baud, TWX/DDD modem for use on dial-up lines and the TWX network, multiple interfaces, and a continuous Mobius loop ribbon cartridge. An OCR-A character set and an APL keyboard-character set combination enhance the 300 and 1200 models.

Agreements Provide Packet-Switched Service Overseas and with Mexico

RCA Global Communications, Inc, New York, NY and Telenet Communications Corp, 1050 17th St, NW, Washington, DC 20036 have agreed to provide service between the United States and overseas points as an economic means of communications between computers and various terminals operating at low and medium speeds. The service will be available on a demand basis with rates based on the volume of data exchanged. Multinational corporations, public data banks, and commercial computing service bureaus are expected to be primary users.

RCA Globcom, which already provides telecommunications service between the U.S. and more than 200 overseas points, will furnish the overseas data transmission facilities and gateway switching equipment linking the Telenet network and its users in the U.S. with packet-switching facilities abroad. Initial service is expected to be furnished to the United Kingdom and several Western European countries, subject to final approval of the Federal Communications Commission (FCC).

Telenet, an FCC-regulated common carrier offering local access in 47 cities in the U.S., Canada, and Mexico, has also recently combined with Teleinformatica de Mexico, S.A. (TIMSA) to inaugurate a computer communications service between the U.S. and Mexico. The interconnection will typically lower the costs of data communications between the two countries by 50%.

In a tariff filed with the FCC, rates for the service are $5.30 per kilopacket, regardless of distance. Each kilopacket contains up to 128k characters of user data.

Network access in Mexico is available over leased line ports at monthly rates established by TIMSA and approved by the Ministry of Communications and Transportation (SCT) of the Mexican Federal Government. Telenet provides access to its network from cities throughout the U.S.

Domestic Network Expansions

In additional announcements, Telenet Communications Corp is planning still further expansion of its packet-switched data communications service with the addition of 38 cities, bringing the number of North American cities served directly by the network to 85. Public dial-in facilities will be added at four new service points by June. With the added service points, subject to FCC approval, the network will provide local access for approximately 80% of the U.S. population.

Also beginning in June, Telenet will offer Hotline Data Service to users of the public packet network. It is designed as a functional equivalent of a private leased line, with a flat monthly rate for unlimited traffic, independent of distance.

When in use, the network will automatically establish a connection between the terminal and a prespecified network address (typically a remote host computer). This connection may be via a Telenet access controller (TAC), synchronous multiconnection channel, or single asynchronous access line.

Price for the service's 110- to 300-bit/s ports will be $50 a month, plus normal port and access line charges. It will be available at all 85 Telenet central offices, as well as on private Telenet access controllers located on customer premises.

Charges for Hotline ports are $125 per month in high density rate cities, $160 in medium density cities, and $205 in low density cities. Ports on private TACs are $75 per month.

Conversion System to Link Incompatible Facsimile Machines

Facsimile communications, which until now could only be accomplished through the use of machines operating in the same machine language and at the same rate of speed, may soon be possible with the ITT Domestic Transmission Systems, Inc's proposed FAX/PAK service. A special conversion system, FAX/PAK will enable most incompatible data terminals and computer-type devices, regardless of design, manufacture, and mode of operation, to communicate. The service is the first offering of the COM/PAK network being developed by ITT-DTS, 2 Broadway, New York, NY 10004 and is expected to be available by mid-1978.

The nationwide packet-switched, data communications network was approved by the FCC late last year. Development of software protocols has been worked on to provide a common link or handshake for varying types of facsimile machines; the network will establish a method of operation acceptable to all data terminals now, as well as in the foreseeable future.

Consisting of 10 computer switching centers and 14 concentrator or smaller switching sites located in 24 cities, the system will use packet-switching and store-and-forward technologies, including communication processors, computer peripherals, and ITTDTS developed interface processors linked by high speed communication channels. Multiple Modular Computer Corp MIV/35/CP computers are to be installed at each switching site to provide fully redundant capabilities for the system.

Operation of an initial 13-city network is scheduled for June 1977, with six cities to be added in 1979. The full 24-city network will be operational in 1980.

The network's variety of other services are to include utilization of

WHEN IT'S FINALLY ON THE SCREEN, YOU DESERVE FAST HARD COPY.

Gould's electrostatic printer/plotter is the fastest graphic hard copy peripheral available today for your Tektronix 4000 Series interactive graphic terminal. You get permanent graphics direct from the terminal in as little as 4 seconds, regardless of image complexity. In an on-line CPU configuration, you can plot at up to 3.25 paper in./sec. and print at up to 1600 lines per minute.

Yet Gould's hard copy still possesses exceptional resolution and extremely high contrast. Only Gould offers you both unmatched speed and unsurpassed image quality.

And Gould lets you select a 0° or 90° image orientation at will. In 90° mode, images are enlarged up to 72%. You are able to select 1024 or 2048 point sampling and high or low speed graphic operation, letting you optimize image size, resolution and speed.

As with all Gould systems, your software is all-Gould. You never need worry about third party variables.

Gould images don't deteriorate. The system requires no warm-up. Gould paper costs a fraction of silver paper. Up to 2 interfaces are accommodated in the plotter, allowing you to use it with up to 8 Tektronix terminals or 4 terminals and a minicomputer, or 2 minicomputer CPU's.

Your CRT work deserves the best hard copy you can get. You get it from Gould.

For more information and a sample graphic output, contact Gould Inc., Instrument Systems Division, 3631 Perkins Ave., Cleveland, Ohio 44114. Or Gould Advance Ltd., Raynham Road, Bishop Stortford, Herts, United Kingdom.

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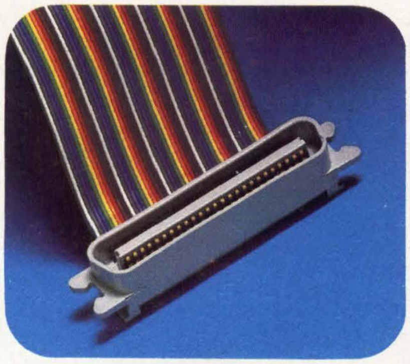
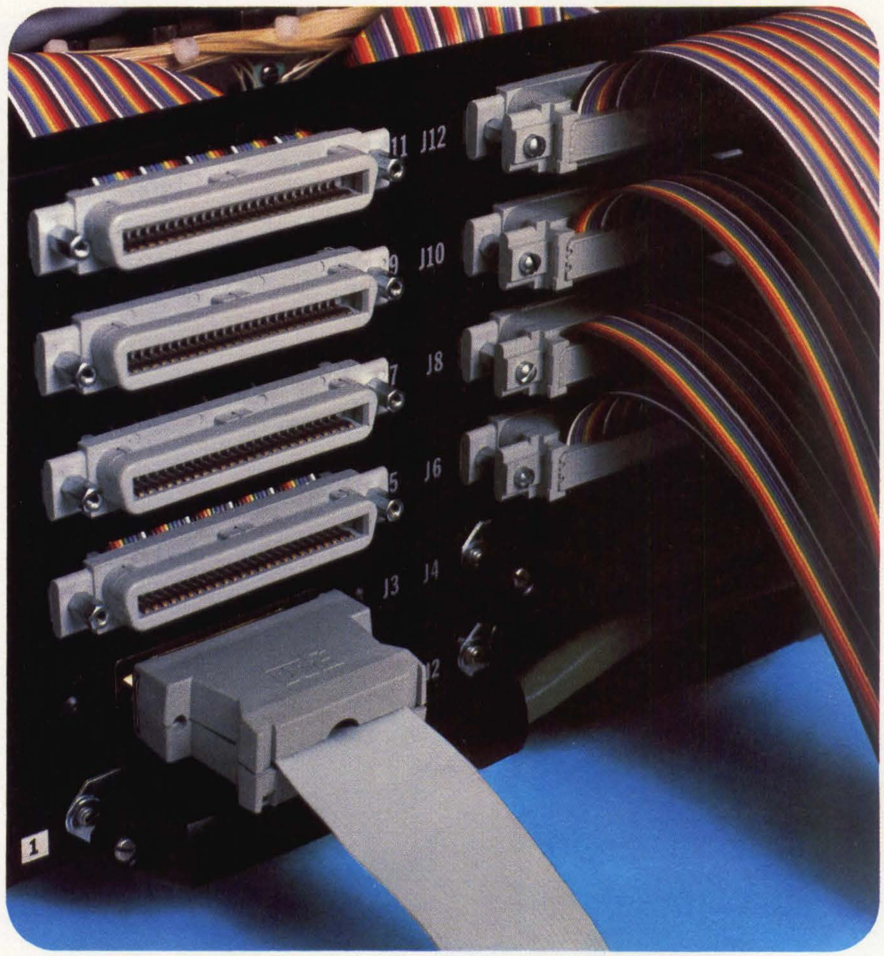
GOULD
The product development company

CIRCLE 13 ON INQUIRY CARD

Now you can mass terminate with ribbon connectors...



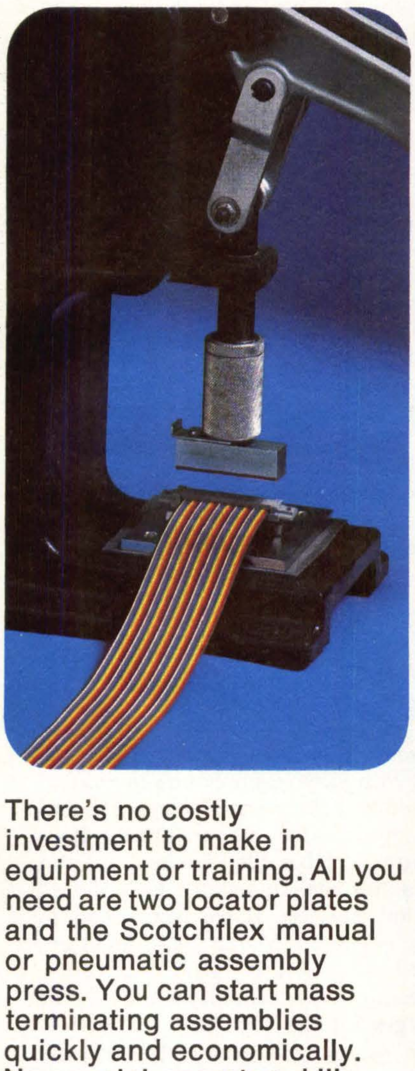
Here's another industry first from 3M that's good news for you: the Scotchflex brand Delta Ribbon Connector System for intra-system or I/O interconnections. In computer applications, in telecommunications, in any place or any way you want to use flat cable and ribbon connectors, this versatile system can do the job at sharply reduced assembly time and labor costs.



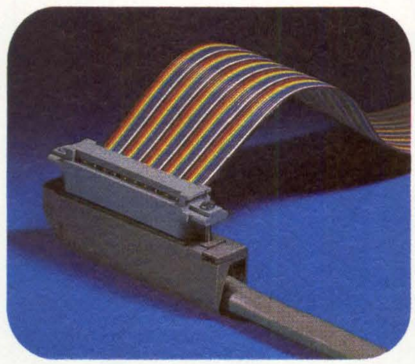
With Scotchflex Delta Ribbon Connectors, no stripping, soldering or other wire preparation is necessary. You can mass terminate a parallel-lay 50-conductor (25-pair) .0425″ center-spaced flat cable in less than 30 seconds with one step. That's about ten times faster than other available methods. And thanks to 3M's field-proven, gold-plated berylium copper U-contacts, all connections are reliably corrosion-resistant and gas-tight.

After termination, there are more savings. You can buss from point to point without disassembling or breaking existing cables. And there's no need to redesign or rework first generation components. This Scotchflex system mates perfectly with all standard miniature ribbon connectors.

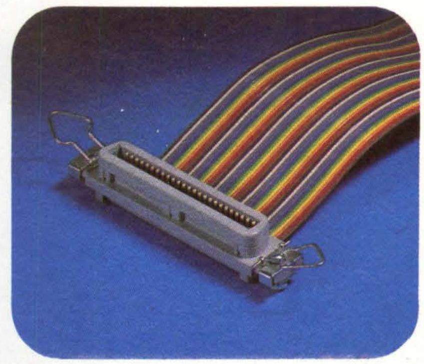
..in 30 seconds or less!



There's no costly investment to make in equipment or training. All you need are two locator plates and the Scotchflex manual or pneumatic assembly press. You can start mass terminating assemblies quickly and economically. No special operator skills are required. Rejects and reworking are greatly minimized.



The Scotchflex Delta Ribbon system includes 50-position male and female connectors, plus appropriate bail mount, screw mount and jack screw kits, strain relief clips and dust covers. Color-coded flat cable is available in parallel-lay conductors #28 AWG stranded or #26 AWG solid.



Only 3M offers you so broad a range of flat cable and system components. A nationwide network of stocking distributors. Best off-the-shelf availability. Proven performance. And the unmatched experience of the people who pioneered mass terminations.

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CIRCLE 14 ON INQUIRY CARD

3M COMPANY

word processing terminals for communication with other processors, as well as for transmission to a facsimile machine or various printer terminals. Communication between two computers or between computers and data terminals will be provided on a phased development basis. Not only will the user have machine compatibility through code, speed, and modulation conversion, but also will be able to store and forward data for delivery at a future time in certain applications.

The proposed network will be interconnected by 56k-bit/s digital data transmission facilities, supplemented by analog data lines up to 48-kHz bandwidths. Transmission facilities of 230k bits/s and 1.54M bits/s would be used to meet further communications demands.

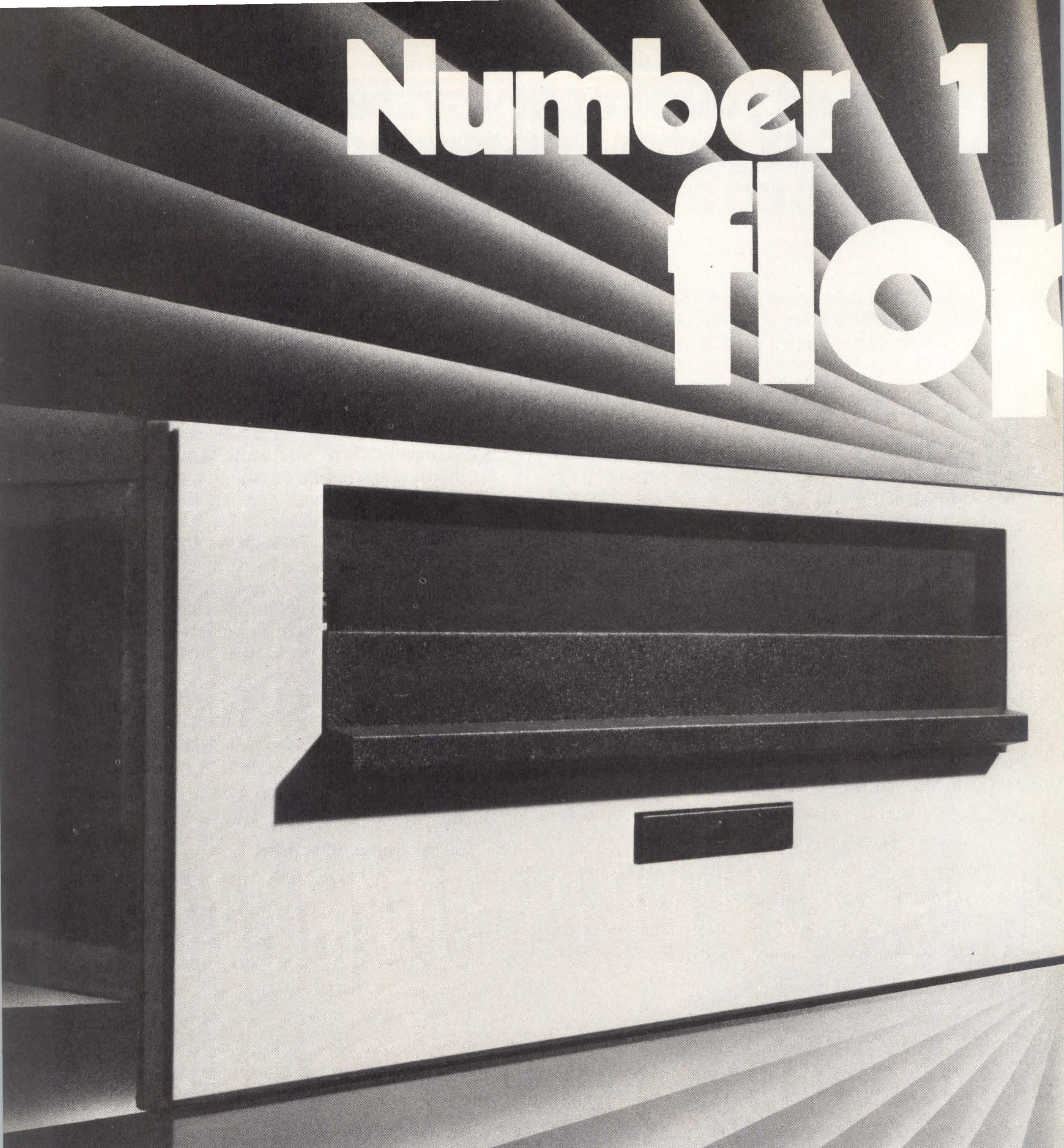
The network is expected to allow systems to communicate with a variety of terminals by offering an economical method of storing, transmitting, and switching data between cities. Dual flexibility permits incompatible terminals to communicate and improves the quality of service through stringent error-control techniques. Once the FAX/PAK facsimile service is introduced, the company plans to introduce other data communications services which will link incompatible terminals and computers.

Interim Rates Increase Cost of Interstate Digital Service

Increasing charges by an average of 20% with varying impact on individual customers, American Telephone and Telegraph Co, Long Lines, Bedminster, NJ has filed revised, interim rates for its interstate Dataphone® Digital Service. Rates, scheduled to take effect on March 24, are in response to a Jan 17, 1977 FCC order directing the company to boost charges for the service.

In general, interim rates will be comparable to those for the company's voice grade private line services. The company is scheduled to file proposed permanent rates by June 8.

First offered in Dec 1974, the service is currently available in 24 cities, providing end-to-end digital data transmission at speeds of 2400, 4800, 9600, 56,000, and 1.544M bits/s. The company also has applications with the FCC to expand the network to 42 additional cities. □



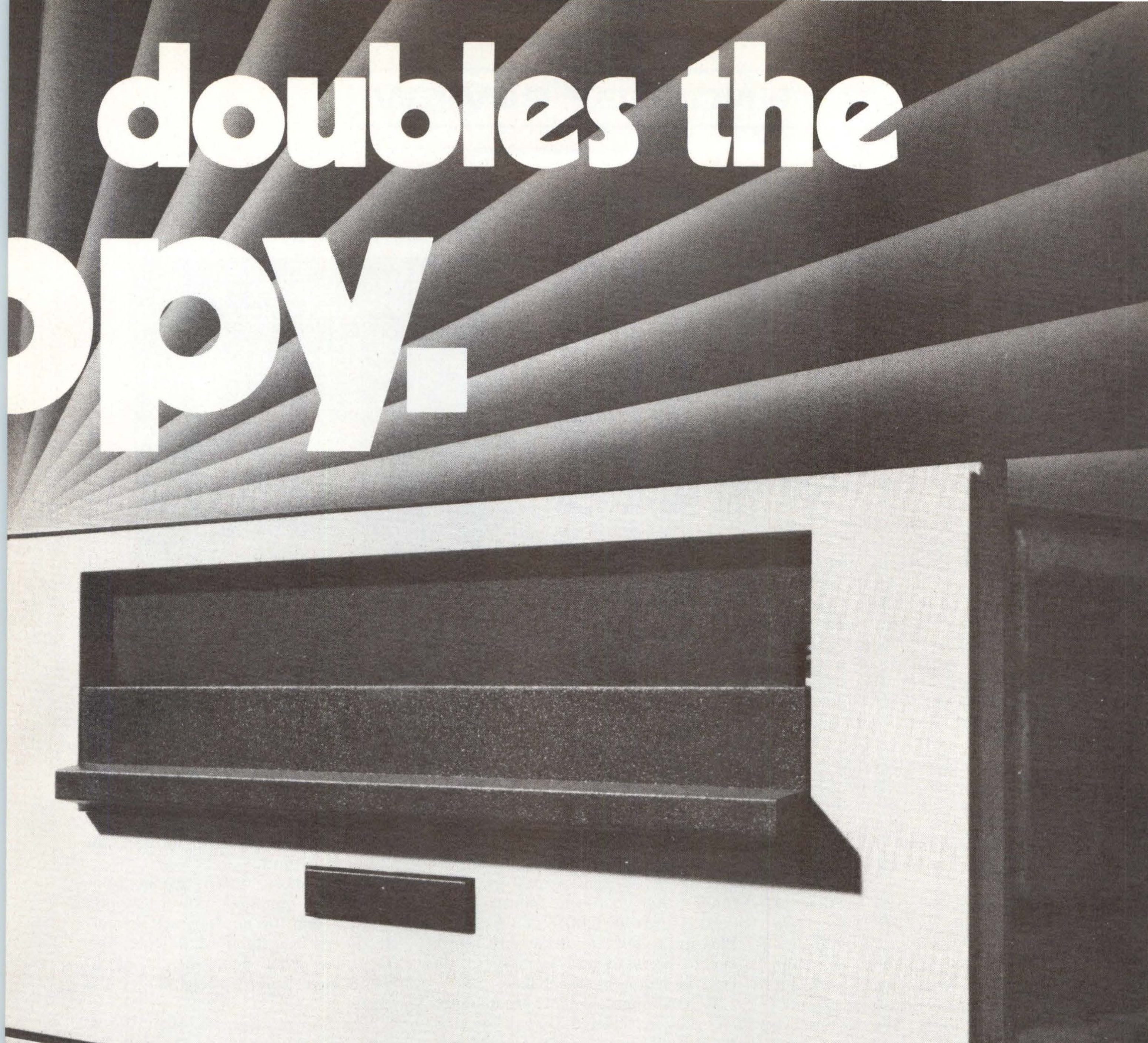
Doubled data storage capacity. Doubled access speed. Doubled floppy media selection. Get it all with the new Shugart double-sided single/double density floppy disk drive. All this for only 25% more than a single-sided floppy.

Data. Data. The new SA850 double-sided floppy packs twice as much data as a standard unit—up to 1600 K bytes (unformatted). Yet the SA850 is identical in physical interface, mechanical outline and package size to the industry-standard—our SA800/801. It's plug-compatible, cabinet-compatible.

Faster. Faster. Access time is more than twice as fast. The SA850 moves from track-to-track in 3 milliseconds, with an average access time of less than 100 milliseconds. The secret is a proprietary Fasflex™ actuator that delivers positive, low-friction head movement.

Media. Media. One drive reads and writes them all. Single or double density. Single or double-sided disks. Industry standard diskettes and IBM Diskette 2, too.

Features. Features. The head carriage assembly allows loading of the two read/write heads simultaneously on both sides of the disk. (No more head load pads!)


doubles the
opy.

Single-Board Memory Stores 128k-Bytes With Error Correction

A single-board memory system with storage capacity of 1.44M bits/board, the in-3000 provides variable storage capacity, built-in error correction, and maintenance by replacement of individual storage elements rather than complete boards. Introduced by Intel Memory Systems, 1302 N Mathilda Ave, Sunnyvale, CA 94086, the system operates as a single-board self-contained memory with system interfaces, controls, and the optional ECC subsystem on the same board.

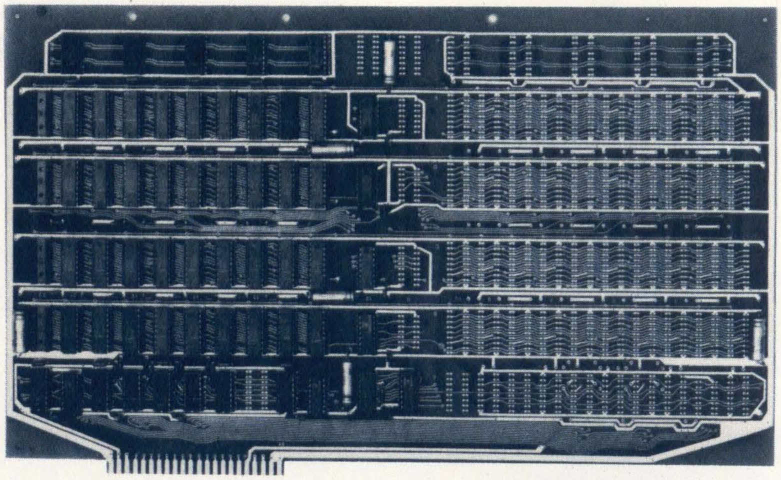
Built using high density plug compatible 8k and 16k-bit RAMs, a single board can expand from 16k to 32k or 65k words. Word lengths range from 16 bits without parity to 22 bits with ECC. Storage capacity of a board can be upgraded in the field by changing the RAM type or by plugging additional RAMs into unused sockets.

Access time of the basic system is 275 ns with cycle time of 450 ns. The ECC option adds 50 ns to access time but provides 10 to 25 times higher data reliability than memory systems with conventional parity checking.

Occupying a reserved section of the basic board, the ECC subsystem adds six check bits to each word during write. During read the check bits are processed on the board to detect data errors. Single bit errors are corrected automatically. The host is automatically notified if any multibit errors are detected.

Each board can replace up to eight conventional micro 3000-core memory boards as well as auxiliary boards, and reduce power dissipation 75% or more per bit. Prices will range from 2 to 3¢/bit in OEM quantities.

Circle 140 on Inquiry Card



Plug-in memory board from Alpha Data's CCD-based semiconductor disc memory has a maximum capacity of 1M bits which can be accessed in 1 ms. (Board shown is half full, providing 0.5M bits storage). Memory system has mounting provisions for eight boards, which can be added in the field, and requires only 80-W operating power

Replacement for Rotating Disc Memories Based on CCDs

A solid-state mass memory, the semiconductor disc memory (SDM) uses charge-coupled devices (CCDs) as the basic memory element. Organized to emulate a block-oriented, random access, serial head/track rotating disc memory, the system uses no moving mechanical parts and provides an average access time of 500 μs, many times faster than the industry standard 8.5 ms at 3600 r/min for discs. Plug-in printed circuit memory boards enable users to add memory in the field as requirements change.

CCD storage elements are mounted on plug-in printed circuit boards. Each board has capacity for 1M bits. Up to eight boards can be added in the field to bring the system up to its full 1M-byte capacity. Data are stored on from 16 to 128 tracks, up to 4096 words/track, 256 words per sector, and can be transferred at rates of 2 to 4MHz.

By organizing the SDM to look like a rotating head/track disc memory, Alpha Data Inc, 20750 Marilla St, Chatsworth, CA 91311 has made the system fully compatible with their other head/track disc memory systems and computer controllers. Basic SDM interface is decoded TTL, including read, write, and address control electronics. This interface is plug-compatible with all of the company's computer controllers, including those for use with Data General and DEC PDP-11 computers. It can also emulate interfaces of other manufacturers' rotating disc memories. Illegal address warning and write protect are integral features.

The memory system comes complete with integral power supply, blower, and frame for rack mount. It mounts in a standard 19" (48 cm) rack, has front panel height of 7" (17.8 cm), and depth of 20" (50.8 cm).

The unit requires less than 100-W operating power for a 1M-byte system. A standby battery supply is optional. Prices range from approximately $6500 to $21,000 depending on storage capacity.

See at NCC Booth 2071

Circle 141 on Inquiry Card

Double-Sided Floppy Disc Doubles Storage, Improves Access Times

The SA 850/851 offers twice the online storage of standard floppy disc drives with what is claimed to be a 210% improvement in access time, yet is priced only 25% higher. A double-sided, single/double-density floppy disc drive, the unit uses the

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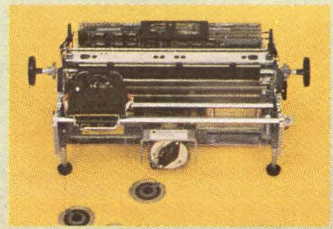
CIRCLE 18 ON INQUIRY CARD



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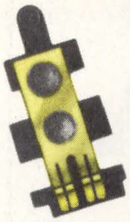
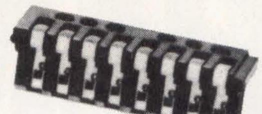
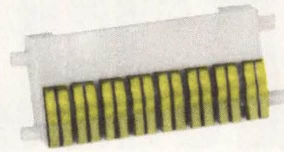


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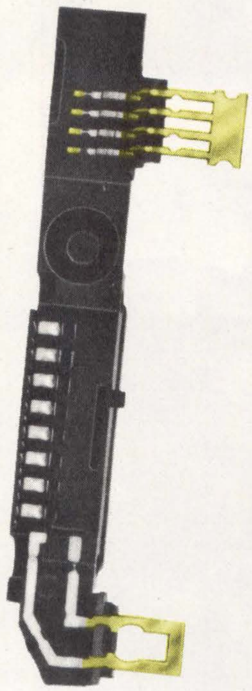
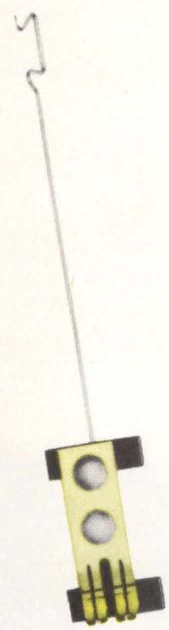

Until recently, Instrument Specialties was known only for the superb quality and performance of our beryllium copper springs and spring contacts. Customers bought the springs, and frequently assembled them into molded blocks in their own plants—with varying degrees of success.

Now, Instrument Specialties can eliminate this divided responsibility. We can supply your contact springs attached to molded bases, and *guarantee to meet the specifications of the entire assembly*! We'll take complete responsibility for producing the plastic block, manufacturing the springs to exact specifications, and then assembling the parts through heat staking, press fitting, or ultrasonic welding. We can also weld or solder springs to other metal components.

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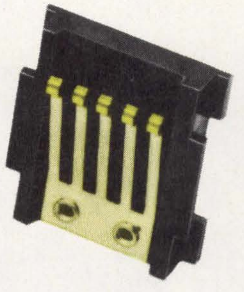
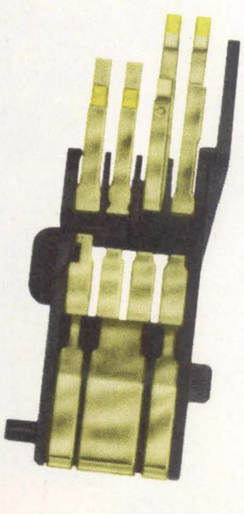
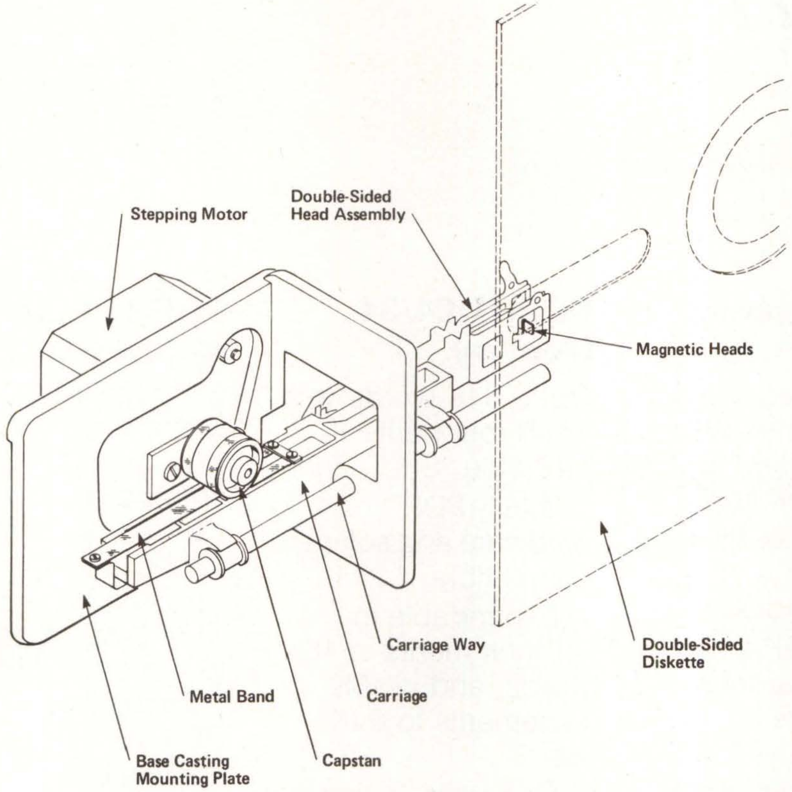





Shugart's SA 850/851 double-sided, single- and double-density floppy disc drives incorporate a band drive stepper/carriage assembly design which eliminates friction and wear of functional parts. Proprietary Fasflex actuator improves access, allowing a claimed 210% improvement in access time

company's proprietary Fasflex™ actuator to improve access time and reduce necessary maintenance by eliminating the head load pad.

Two-headed versions of the standard drives, the units were developed by Shugart Associates, 435 Indio Way, Sunnyvale, CA 94086. Identical in appearance, physical interface, and mechanical outline to the SA 800/801, the drives use two index detectors to distinguish between 1-sided and 2-sided diskettes and to provide index for the SA 850, and index and sector for the hard sectored SA 851.

Two flexure mounted, ceramic read/write heads, each with an integral load area, are lightly loaded toward each other with the disc sandwiched between them. Read/write cores are offset by 0.0833 in (0.2116 cm); the load area is opposite the read/write gap. This combination of light load flexure mount and ceramic load pad provides excellent compliance and minimum wear.

Design of the unique band drive stepper/carriage assembly eliminates friction and wear of functional parts and provides speed, accuracy, and reliability as well as enhanced serviceability since head alignment is not required when the assembly is replaced.

Available with single-density (FM encoding) and double-density (M^2FM) capability as standard features, the unit is the same physical size as the standard floppy (4.62 x 9.50 x 14.25", 11.73 x 24.13 x 36.20 cm). A skinny version measuring (4.26 x 8.55 x 14.25", 11.73 x 21.72 x 36.20 cm) will allow side by side mounting in a 19" (48 cm) RETMA rack.

Units are plug-compatible with standard drives and are media interchangeable with IBM 3740, S/32 single-sided drives as well as IBM Series/1 (model 4964) and 3600 series 2-sided drives using double-sided IBM diskette 2 media or its equivalent.

Capacity is 6.4M bits/disc unformatted, 4.0M bits/disc IBM format. Transfer rate is 250k bits/s and latency is 83 ms average. Track-to-track seek time is 3 ms and head load time is 35 ms. Double-density recording results in 12.8M-bit capacity with a transfer rate of 500k bits/s. Error rates are $1/10^9$ bits read soft, $1/10^{12}$ hard, and $1/10^6$ seek. Media will withstand 3.5 x 10^6 passes/track and 30,000+ insertions.

Circle 142 on Inquiry Card

Remote Control Equipment Provides Smart Interfaces, Fast Processor

Two enhancements to its total distributed control (TDC) architecture —a family of remote process interface units for analog and digital I/O processing, and a process computer—have been announced by Honeywell Inc's Process Control Div, 1100 Virginia Dr, Fort Washington, PA 19034. TDC 7100 process interface units (PIUs), smart remote multiplexer units, are interconnected by a single coaxial cable that serves as the communications link among the elements of a distributed system. The TDC 4500 computer provides all necessary central processing functions in a single compact cabinet, while maintaining compatibility with existing series 4000 computers.

Each PIU functions as an intelligent unit to perform scanning, limit checking, sequence-of-events timekeeping, and automatic reporting of meaningful changes and alarms. Used as a solid-state analog scanner, digital I/O interface, and analog output subsystem, the high level PIU reduces routine limit and status checking, and data conversions by computer software when acting as a computer's process interface. A low level unit handles analog inputs from sensors. When equipped with signal conditioning elements, it can accept current and voltage input signals. The device reduces central processor loading by performing offset correction, reference temperature value compensation, and gain optimization and limit testing. A satellite unit provides remote multiplexers with moderate performance over a wide temperature

Our first DEC compatible memories for 1977!

LSI-11 Memory

16K words in a single quad slot (2 option slots)

Totally LSI-11 hardware and software compatible.

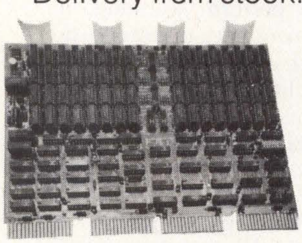
Selectable, on-board refresh modes:

1. Distributive refresh mode. (Monolithic Systems method)
2. Burst refresh mode. (DEC method)

One year warranty on parts and labor.

$1,195* single quantity. OEM discounts available.

Delivery from stock.



MSC 4501
January

PDP-8 Memory

Requires 75% less power than equivalent core memories (8K words requires only 0.6A at +5 volts DC).

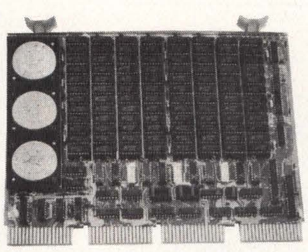
Nonvolatile, 8K words fits in a single OMNIBUS® slot.

Totally PDP-8 A, E, F or M hardware and software compatible.

One year warranty on parts and labor.

$995* single quantity. OEM discounts available.

Delivery from stock.



MSC 3201
February

PDP-11/04/34 Memory

Up to 64K words, with or without parity, in a hex wide "SPC" slot.

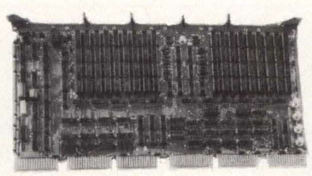
Totally PDP-11/04/34 hardware and software compatible.

Expandable in 4K increments to 16K words, and in 16K increments to 64K words.

One year warranty on parts and labor.

$1495* (16K words) single quantity. OEM discounts available.

Delivery from stock.



MSC 3501
March

PDP-11 Extended Memory Unit

Up to 2.8 megabytes, with parity, in a 10½" high rackmount chassis (includes power supply and forced air cooling).

Expandable in 512K byte increments to 4 megabytes.

Faster than RF-11/RS-11—4 μsec. access time, 1 μsec. transfer rate, selectable.

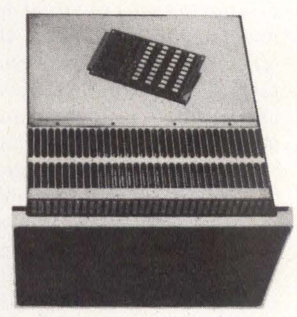
More reliable than disk or comparable core memory.

Nonvolatile with available battery backup.

PDP-11/04 through 70 hardware and software compatible.

One year warranty on parts and labor.

Delivery 45 days ARO.



MSC 3601
April

CIRCLE 20 ON INQUIRY CARD CIRCLE 21 ON INQUIRY CARD CIRCLE 22 ON INQUIRY CARD CIRCLE 23 ON INQUIRY CARD

range as well as handling analog inputs and reducing CPU loading.

Featuring increased throughput, the TDC 4500 process computer provides up to 256k words of MOS memory with 600-ns cycle time; speed and small size are achieved by use of an internal microprocessor and high density integrated circuits. Its 24-bit word length permits control precision and high speed memory I/O. A GENIE I/O bus with a transfer rate of 1M words/s permits a common interface path for communication between central processor arithmetic and main storage functions and the various process I/O and peripheral controller functions.

Circle 143 on Inquiry Card

Mid-Range Computer Adds User Microprogramming to Augment Instruction Set

Bringing microprogramming and multiprogramming to the mid-range market, the Eclipse[R] S/130 offers a user-microprogrammable control processor to meet high speed requirements in dedicated applications and supports concurrent timesharing, batch, and real-time operations for complex multifunction applications. Introduced by Data General Corp, Southboro, MA 01772, the processor incorporates floating point and character handling instruction sets to provide the versatility and high throughput needed in laboratory, scientific, and communications applications.

Packaged in a compact 12-slot chassis with optional expansion chassis, the S/130 features Eclipse architecture and has up to 256k bytes of MOS, core, or mixed main memory. Semiconductor memory modules are 64k bytes with a cycle time of 500 ns. Memories have error correction (ERCC) and optional battery backup. A memory allocation and protection unit (MAP) provides program and data protection in multiuser environments. Peripheral support includes 315k-byte diskettes and 190M-byte disc files as well as magnetic tape drives and cartridge discs, sensor I/O and communications subsystems, and printers and video display terminals.

Standard are bit, byte, word, and block instructions as well as hardware interrupt vectoring and stack facility, multiply/divide instructions, automatic program load, and power fail/auto restart features. In computational applications, users can add a fast floating-point instruction set; a character-handling instruction set augments the standard set for communications or business applications.

Custom instruction set capability is provided through user-microcode storage in RAM (writable control store) or p/ROM (programmable-ROM control store). Writable control store offers 1k 56-bit words for alteration of instructions; p/ROM control store provides 2k 56-bit words of nonvolatile microcode storage. Technical features include 15 independent control fields, 200-ns microcycle time, high speed scratchpad consisting of 256 16-bit registers, and a powerful arithmetic logic unit. Microcode facility offers reentrant interruptible microsubroutining to eliminate the high latency in long microcode sequences. Multiway microcode branching provides efficient decoding of operation codes.

Running under AOS (advanced operating system), the S/130 offers multiprogramming users large computer processing speed, hardware/software system security, and efficient resource management. In addition to AOS, system software includes the realtime disc operating system.

Representative system prices are $11,000 for an S/130 with 32k-bytes core memory, which includes auto-program load, power-fail/auto-restart, and hardware multiply/divide. In a single-bay cabinet with 128k bytes of RAM, battery backup, MAP, floating-point instruction set, real-time clock, 10M-byte disc subsystem, sensor I/O subsystem, and 60-char/s terminal subsystem, the price is $42,150.

See at NCC Booth 1215

Circle 144 on Inquiry Card

Data General's Eclipse S/130 offers up to 256k bytes of core and/or RAM, user-microprogramming, and floating-point and character-handling instructions, as well as multiprogramming capability under AOS

Computer Systems Up Performance 20% Using Faster Disc Drive

HP 3000 series II models 6 and 8 achieve higher performance through the use of the 50M-byte HP 7920A disc drive. The drive, in addition to providing improved system performance, is easier to repair and maintain, and can result in a 59% reduction in maintenance costs per drive. The General Systems Div of Hewlett-Packard Co, 1501 Page Mill Dr, Palo Alto, CA 94304 designed the business computer systems for use by small organizations seeking a general-purpose computer and for large organizations planning to add or expand satellite processing capability.

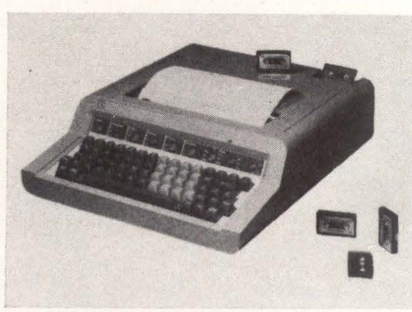
Model 6 has 128k bytes of memory (expandable to 256k bytes), 1600-bit/in tape drive, 2640B CRT console, and terminal controller which can handle up to 15 asynchronous terminals at speeds up to 2400 baud. Model 8 provides 320k bytes of memory, expandable to 512k bytes. Both support a synchronous communication interface operating at speeds to 9600 baud with software capability to emulate an IBM 2780/3780 remote job entry station.

Base price of the model 6 is $110,000; the model 8 starts at $140,000. Additional disc memories are available at $14,000 for a single HP 7920A and $26,000 for a pair of additional drives. Either computer will support up to eight drives.

Circle 145 on Inquiry Card

Desktop ASR Terminal Combines Integral Memory and Removable Storage

Featuring both a built-in Mini-Cassette magnetic tape unit with 68k



With program and data storage in internal RAM and on removable Mini-Cassette magnetic tape units, Computer Devices' Miniterm 1204 ASR terminal also incorporates a thermal printer to allow data preparation, editing, and reporting in a single compact unit

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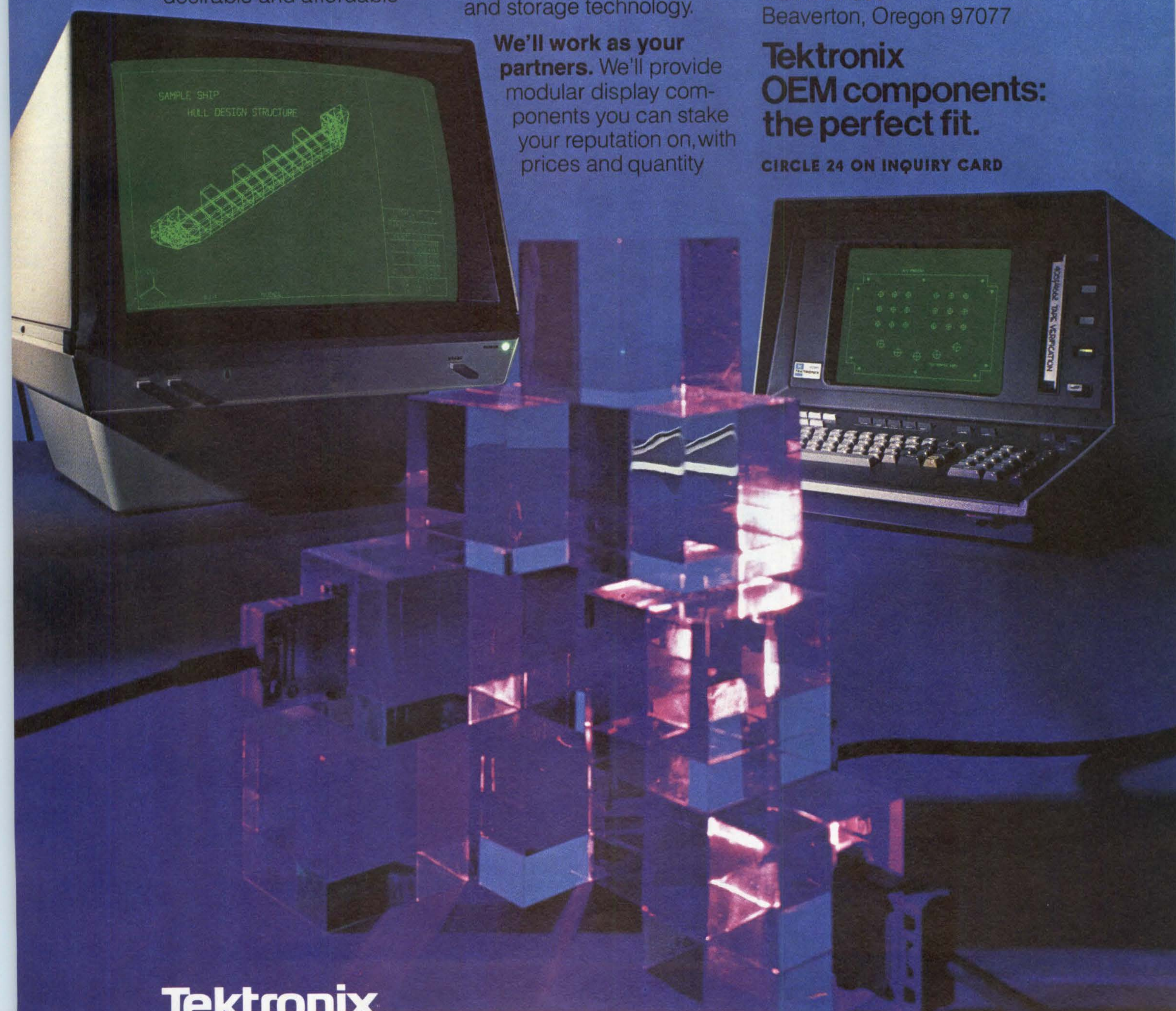

Tektronix
COMMITTED TO EXCELLENCE

The new DAC standard. Analog Devices' complete 10-bit monolithic DAC.

char of removable storage and an integral 8k RAM, the Miniterm 1204 automatic send/receive terminal provides complete simultaneous transmit/receive capability; tape to memory, memory to tape, tape to line, or memory to line transmission; and editing capability for offline data preparation. The completely microprocessor-controlled unit from Computer Devices Inc, 25 North Ave, PO Box 421, Burlington, MA 01803 incorporates a maximum of state-of-the-art electronics and a minimum of moving parts to ensure long life and reliable operation; quiet operation is assured by a solid-state thermal printhead.

Main memory capacity ranges from 7k 8-bit words to 31k words of first-in first-out storage. Random access edit memory ranges in size from 7k to 31k words depending on use of main memory. Cassette units have capacity for 68k char recorded 600 bits/in (236/cm) on a 50-ft (15-m) tape cassette. The transport provides record and playback at 3 in/s (7.62 cm/s) with fast forward and rewind at up to 20 in/s (50.8 cm/s). Internal data transfers (tape to memory or memory to tape) occur at a maximum rate of 1800 bits/s.

The unit's thermal data matrix printer outputs 35 char/s, 80 char/line on 8.75" (22.23 cm) wide paper. Data transmission occurs asynchronously serial by bit and character at switch selectable rate of 110, 300, or 1200 baud. Hardwire compatible with all major minicomputers and central processors, the interface is EIA Standard RS-232; operation in local, full- or half-duplex modes is switch-selectable.

Binary or ASCII code use is selectable, and programmers are provided with complete diagnostic capability for printing control characters. High speed editing capability within the memory allows extensive search, delete, change, append, and file control functions.

Circle 146 on Inquiry Card

Cache Memory Integrated with Microprogramming In Mid-Range Computer

In a fully integrated configuration, the PDP-11/60 consists of central processing unit, two RK06 disc storage units with 28M-byte capacity, and an LA36 terminal. Integral cache memory and floating point processor offer substantially improved performance, while its design incorporates both new combinations of existing computer elements and design extensions of such elements.

The system features 532-ns effective cycle time, 256k bytes of either MOS or core main memory, and low profile cabinetry. Options available from Digital Equipment Corp, Maynard, MA 01754 make it into what is claimed to be the most "generalized" minicomputer in the mid-range. According to project manager Walt Vignault, "the processor was designed to take advantage of cost reductions made possible through microprogramming techniques without degrading system performance; the balance results in a highly cost-effective design." An example is the semiconductor memory, which has an error correction code feature that corrects errors automatically and an MTBF of better than 20,000 hours. This permits the use of lower cost semiconductor memory, rather than core, without degradation in reliability.

Augmenting the unit's built-in floating point processor, an optional high speed floating point processor will perform a double precision (64-bit) multiply between registers in 3.74 μs.

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To make CAPS VIII even more attractive, we're also offering a new Smart Clip, a new pulse-catching logic probe, an IEC buss interface, and diagnosis logging capability.

Of course, to get CAPS VIII's big improvements in fault resolution, setup and troubleshooting speed, and cost, you first

New Smart Clip reduces diagnostic time.

need a GR digital or hybrid circuit board tester. But that's no problem either. The number to call is 617-369-8770 ext. 273.

GenRad, Inc. Test Systems Division, 300 Baker Avenue, Concord, Massachusetts 01742.

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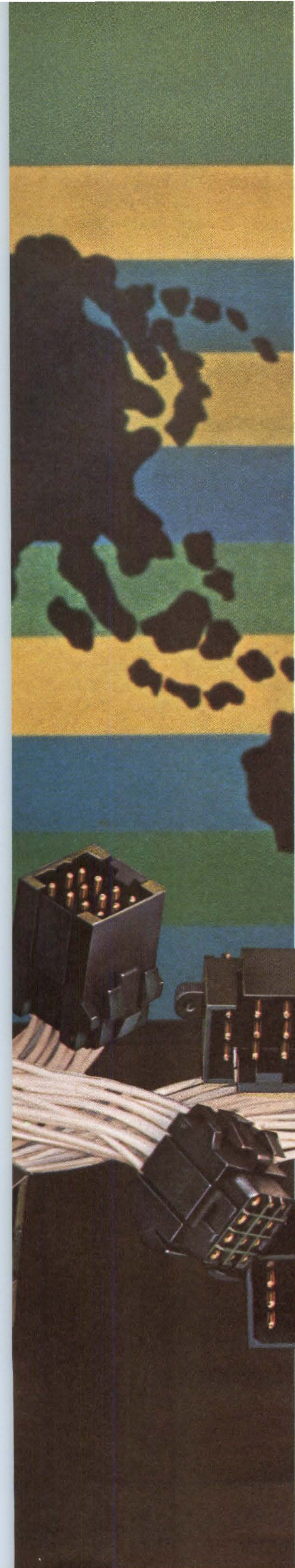
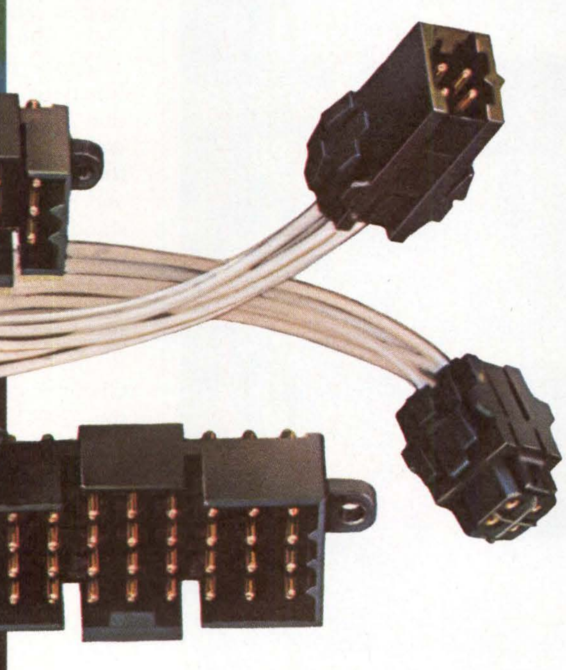




The option provides the means to develop fast-response systems for a variety of operations.

Of particular interest to OEM users are the user control store (UCS) and extended control store (ECS) options. The UCS, which permits access to the inner machine for tailoring performance at the microprogram level, includes a hardware module and software tools for microprogram development; through microprogramming, functions ranging from special purpose I/O functions to emulation of some mini and microcomputers can be achieved. The ECS module permits special functions developed with the UCS to be placed into programmed read-only memories.

For testing, an optional diagnostic control store (DCS) module can reduce MTTR to 2.5 h, lowering both field service charges and downtime. Running under the RSX-11M operating system, the 11/60 will perform maintenance and diagnostic tests on itself.

System prices range from $44,700 to $70,000 in standard configurations. Single unit prices for the central processor alone begin at $25,700. Deliveries are scheduled to begin in June.

Circle 147 on Inquiry Card

Proposed ASCII Standard Augmented to Include CRT Device Controls

Twenty-five additional controls are being standardized for use with the American Standard Code for Information Interchange (ASCII) in 7- and 8-bit environments. Entitled Additional Controls for Use with ASCII, the draft proposed American National Standard is out for public comment as BSR X3.64.

Primary thrust of the standard is to encode the control functions needed by the current technology of 2-dimensional character imaging I/O devices. The standard uses a multiple character structure similar to an escape sequence to obtain 78 distinct functions. A uniform method is used to represent both numeric and selective parameters indicating dimensional quantities and obtaining 88 more subfunctions. Twenty-three modes alter the interpretations of some functions.

Types of controls include editing functions, formatting, and specification and control of input areas, as well as certain status setting and interrogation functions, mode selection, and typesetting composition. The standard is open-ended so that more controls can be incorporated in future revisions.

Copies of the 100-page dpANS BSR X3.64 are available from Mr R. M. Brown, Director of Standards, CBEMA, 1828 L St, NW, Washington, DC 20036 at a charge of $3/copy. Comments should be returned to CBEMA at the address given, prior to May 28.

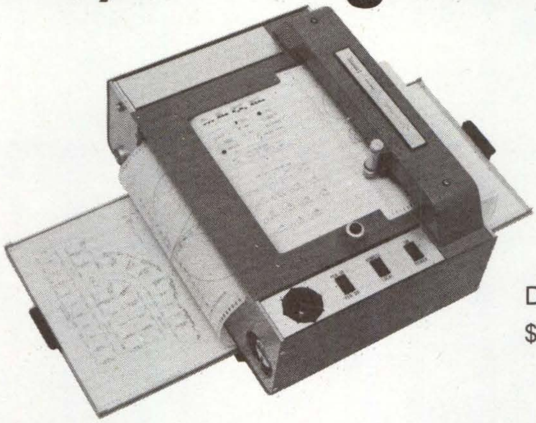
Circle 148 on Inquiry Card

Dual Diskette Unit, Editing Station Expand Word Processing Line

Word Processor 10A, which is a standalone word processing system, and an editing station have been added to the line from Wang Laboratories,

New

Super Fast/Super Quiet
CØMPLØT® Digital Plotter



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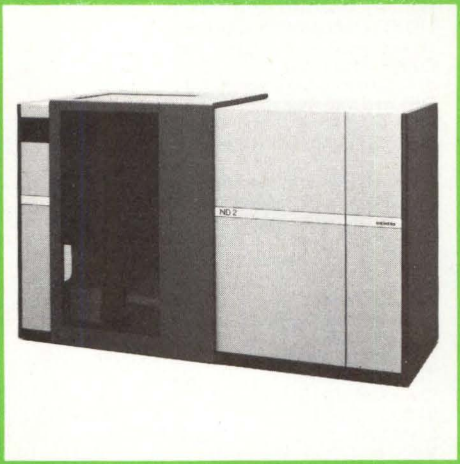
CIRCLE 33 ON INQUIRY CARD

The Siemens ND 2 is the ultimate in hard-copy peripheral systems. It uses a laser and electrophotography to print up to 21,000 lines per minute on plain paper. The ND 2 can output approximately 8,000 12-inch sheets per hour with a forms overlay feature that eliminates the need to preprint computer paper. Even at top speed the character quality is suitable for OCR applications. Designed for high through-put and reliability, the life of the photoconductor drum is an unparalleled three million copies — and the drum is user changeable.

The new PT 80 terminal, with printing speeds of 30-90 characters per second, is similar in design to the Siemens teleprinter 1000. Based on modular building blocks, the PT 80 offers a large variety of different type faces and the ability to adjust to all common paper sizes. The range of 72-132 characters per line make the PT 80 an extremely flexible terminal. Its compact design and quiet operation make the terminal highly suitable for use in office, banks, data processing centers, etc.

The Siemens PS 5 disk storage drive features an average positioning time of 23 ms. It's easily expandable from 72 to 144 to 300 to 500 MB without cabinetry changes. Users can upgrade easily, and your parts inventory stays small. The PS 5 is extremely rugged and reliable with a proven MTBF of 2,500 hours, including the first hour of operation. At 500 MB it is the largest capacity disk unit available – and the most economical per MB.



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To best appreciate the capabilities of these systems, we would like to demonstrate them to you.
We will be at the NCC in Dallas, June 13-16.
You may also call R. Mizrahi directly for an appointment.

Siemens peripherals . . . for your growing data appetite

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Inc, One Industrial Ave, Lowell, MA 01851. Dual diskette storage meets rising demands for increased capacity, duplication capability, and simultaneous input and output; visual CRT-based input and editing allows easy operation.

WP10A is comprised of three basic units: work station (CRT/keyboard), 40-char/s bidirectional daisy printer, and dual diskette drive with a non-removable system diskette that may contain up to 200k char and archive diskettes each containing up to 300k char. Operator prompts appear on the screen and automatic word wrap-around assists operators in producing final documents efficiently.

The document-oriented system allows complete documents, rather than single pages to be created, accessed, and played out. Among its editing capabilities are insertion and deletion of characters, words, lines, paragraphs, or entire sections of text. A glossary serves to reduce the input of commonly used words or phrases to two keystrokes.

Keyboard is a standard typewriter style with additional special function, format, and cursor control keys. The 12" (30.48 cm) diagonal display provides 24 lines of 80 characters each. Whenever text is entered, revised, inserted, or deleted, it is displayed. Continual prompts assist operators through every system function.

Consisting of work station with CRT video screen and a simplified keyboard/storage station using high capacity, rapid access dual diskettes, the editing station is an electronically controlled word processor for use where a printer is not needed. Keyboard is a standard office typewriter with additional operational and cursor control keys.

The editing station, a visual text originator, provides operational features such as operator prompts on the screen and is document-oriented to allow complete documents to be created, stored, retrieved, and edited. Operational features include automatic centering; indenting; decimal alignment; automatic indexing for sub/superscripts; global search, replace, and hyphenation; document assembly; and right margin justification. Telecommunications capability may be added.

All units comprising both systems are portable, allowing them to be located on any standard desk or table. Accessories include a table for work station and dual diskette. With additional electronics both systems can be upgraded to a WP20 eliminating the problem of system obsolescence.

Circle 149 on Inquiry Card

Data Entry Software Permits Independent Use From Three Terminals

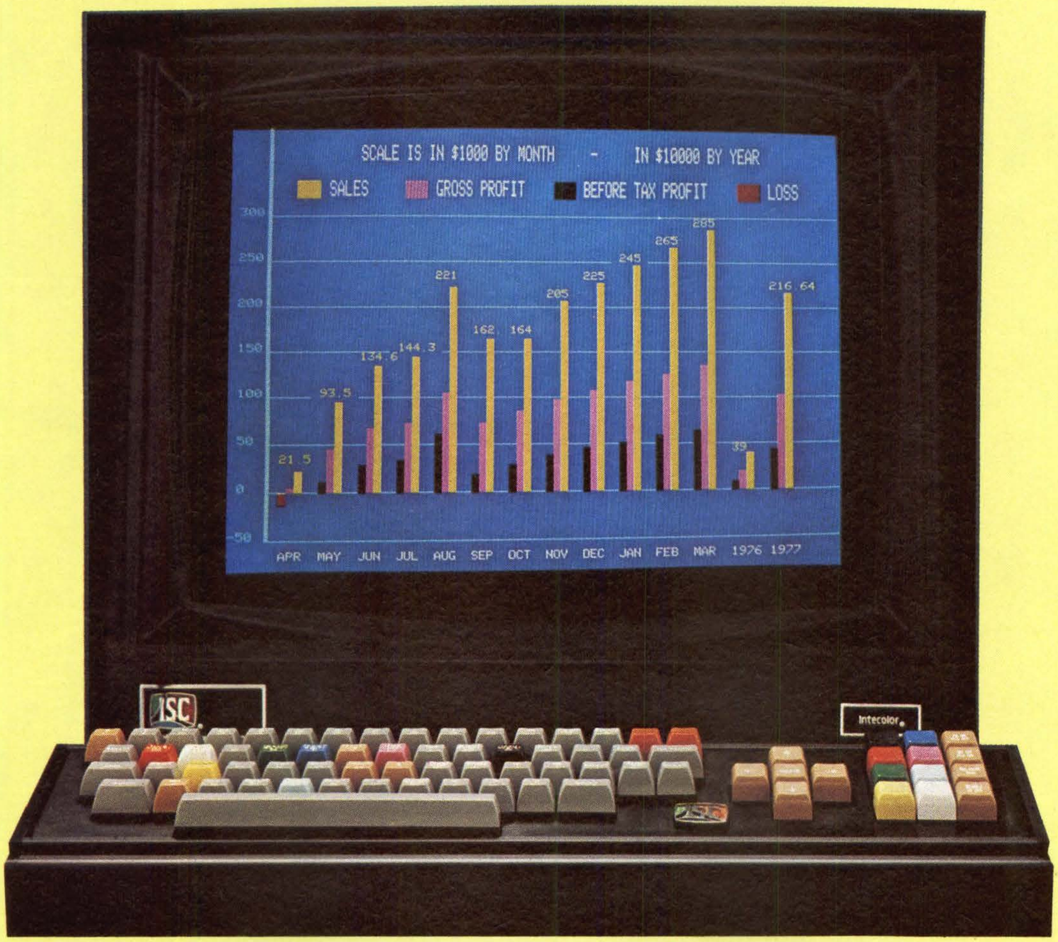
Multiform™ data entry software allows up to three users to independently enter data into pregenerated data entry screen formats, extending the capabilities of Diskette 1100 and 1150 dispersed processors by allowing attachment of two additional data entry terminals. Data entered via the system and stored on diskette or disc may be easily retrieved and modified using interactive control keys on processor or data entry terminals. A print utility allows the operator to print the form image, data in the files, and form of entered data in appropriate places.

The forms-oriented data entry system was developed by Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284 to allow users to create data entry formats with a variety of editing criteria for each field. Criteria include six field types, justification, and numerous entry restrictions. The system's high level English-structured language allows additional edit checks to be programmed on a per-field basis. These field programs permit arithmetic operations, data manipulation, range checking, table lookups, check digits, comparisons, branching, and screen output controls.

Data files created by the system can be processed by other data processing languages such as RPG II, COBOL, DATABUS, DATASHARE and BASIC. These files can also be communicated to other computers by use of an emulator.

A specially coded numeric pad for easy interactive data entry under Multiform control is provided on the 3610 terminal. The data entry station has an 80-character x 24-line display screen, standard upper/lower case typewriter keyboard, 11-key numeric and data entry pad, and five control keys. It can be hardwired to a processor or connected via standard telephone lines using modems and will operate at up to 9600 baud.

Circle 150 on Inquiry Card



Unretouched photograph of screen.

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But if you'd like to see for yourself, look over our rep list on the adjacent page and ask the rep in your area for a demonstration. Whatever your application, he can show you the right Intecolor 8001 CRT at just the right price.

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ALIVE &
SWELL!
SPECTACOLOR
ACT I
Restaurant

The LSI-11 microcomputer gives its regards to Broadway.

Meet Broadway's newest discovery.

Our very own LSI-11. The most powerful, most software-supported microcomputer you can buy.

You'll find it running Times Square's latest attraction – the new Spectacolor animated sign on the Allied Chemical Building.

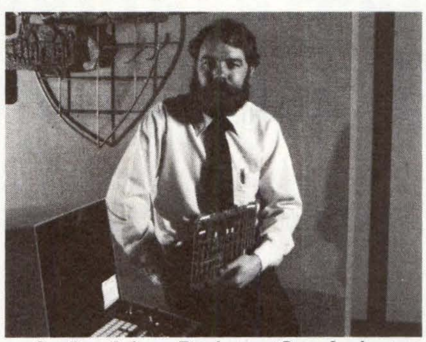
The system was developed for Spectacolor by American Sign and Indicator Corporation, using their new Mark 400 Message Center, powered by the LSI-11.

For AS&I's Software Development Group Leader Gary Berg, anything less than the LSI-11 simply wouldn't have been enough.

"In the Mark 400 we wanted a new top-of-the-line controller for our dynamic visual display systems," says Gary. "The computer that runs it had to be powerful enough to handle all our display services – scoreboards, flip discs, LEDs, lamp banks, multiple signs, and our new UNEX displays. But since the Mark 400 also had to be a standard off-the-shelf product, its computer had to come in at a reasonable cost."

For Gary Berg, the LSI-11 was the only answer: "There is simply no other computer that can touch it in terms of the amount of computing power you get for the money."

Another thing that attracted Gary was the LSI-11's ease of programming. "We use assembly-level language for its greater speed and to conserve core. And, for this application, we found the LSI-11's assembler as easy to use as high-level languages."



Gary Berg, Software Development Group Leader at AS&I, Spokane, Washington.

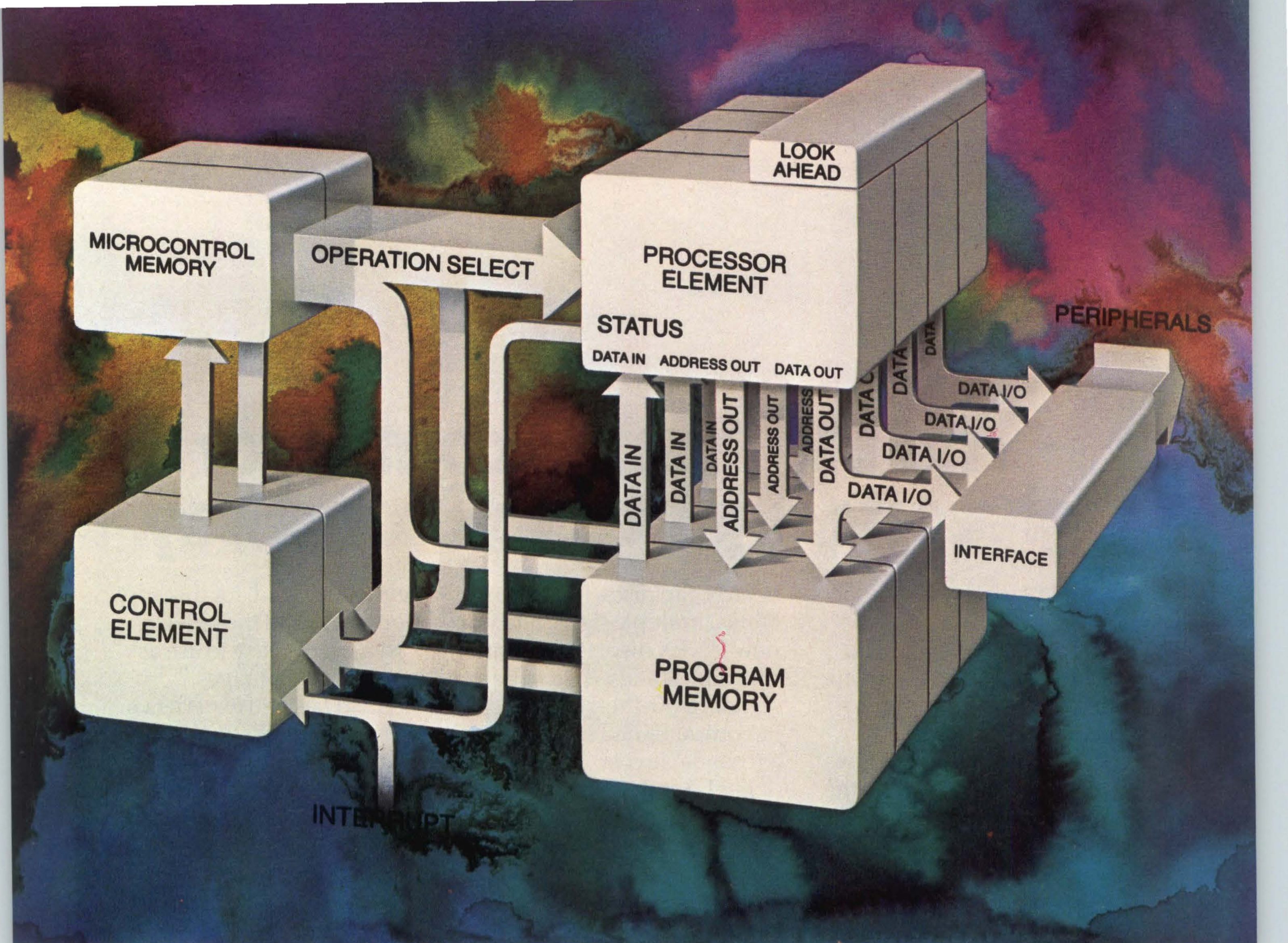
AS&I has had experience with our large PDP-11's for their own data processing and in custom scoreboard applications at Tampa Bay, Florida, and Pontiac, Michigan. And according to Gary Berg, "Being able to use the same software on this full range of computers makes the LSI-11 the clear favorite for us."

The LSI-11.

The world's first microcomputer to become a Broadway hit.

(For 600 pages of solid technical information, plus our new brochure of microcomputer case histories, "Why Anything Less than the LSI-11 Wasn't Enough for Me," just call toll free 800-225-9480 [in Mass. 617-481-7400 ext. 5144], or write Digital Equipment Corp., One Iron Way, Marlborough, MA 01752.)

digital
COMPONENTS GROUP



New S481 microcomputer chip set... from Texas Instruments

Fast. Flexible. Efficient. TI's S481 microcomputer chip set. Newest member of TI's innovative 9900 First Family.

A new series of high-performance Schottky TTL microprogrammable building blocks, the S481 chip set offers a level of performance and flexibility otherwise unavailable. And allows you the greatest degree of precision in matching system designs to applications.

• **Fast throughput**—up to ten times faster than conventional microprocessors. Select and operate on two operands—generate status and store results in a single 100-ns microcycle.

• **Software investment protection**—complete microprogrammability lets you emulate existing instructions.

• **Improved memory efficiency**—you can write tailored instructions suited precisely to your application to use memory more efficiently, reducing hardware costs.

• **Greater flexibility**—with the S481 chip set building blocks, you can tailor your hardware to minimize costs. And permit future expansion or upgrades as desired. For both military and commercial applications.

TI's 9900 First Family

With the addition of the S481 microcomputer chip set, TI's 9900 First Family now offers you a total, standardized capability all the way from components through systems. Having common hardware. Common software. Common support. Allowing you to move over a wide range of applications with greater economy. Greater software retention. Less relearning. Less obsolescence.

The Processor Element... extraordinary capability

A 4-bit slice processor element, the SN54S/74S481 is both micro and macro programmable. Recognizes, decodes, and executes 24,780 instructions. Each within a single 100-ns clock cycle.

For example, the S481 element performs compound operation – select two operands, AND, add, sign protected shift, generate status and update memory – all in a single 100-ns clock cycle. Hardwired algorithms are provided for automatically sequenced iterative, signed or unsigned multiplies and divides. As well as for cyclical-redundancy character calculations.

Behind this outstanding capability: TI's advanced Schottky TTL process technology. Plus TI's advanced 9900 Family memory-to-memory architecture – a computer architecture that places multiple register files in main memory. Result – the number of available general-purpose registers is limited only by the size of program memory. Instructions do more work, using less memory space. Interrupts are handled faster.

Other architectural features:

- Parallel dual input/output ports.
- Full function ALU with carry look-ahead, magnitude, and overflow capabilities.
- Double-length accumulator with full shifting capability and sign-bit handling.
- On-chip dual memory address generators.

The SN54S/74S481 is available now in a high-density 48-pin quad-in-line ceramic package at $29.25 each for the commercial version (100 pieces).

The Control Element... fast next-address generation

The new SN54S/74S482 4-bit slice control element integrates a full adder, four-word push-pop stack, source select multiplexer and address register. It offers next-address generation in 25 ns. All in a space-saving 20-pin package.

In addition to simple loops and forward sequences, the S482 can be used to implement the powerful operations needed to decrement, vector, offset or jump in a single cycle to any address within its domain. Subroutines can be nested up to four levels deep in the push-pop stack and can be retrieved in the reverse order of occurrence. The stack can also be updated without changing the contents of the output register. Available now at $6.30 each for the commercial version (100 pieces).

PROMs and RAMs... broad choice for efficiency

For use with new microcomputer chip set, TI offers a choice of 10 Schottky-clamped programmable read-only memories. All are made with titanium-tungsten fuse links for fast, reliable, low voltage programming. And 11 static, high-performance Schottky random access memories. Enough variety in organizations, speed/power performance and packages to provide efficient, cost-effective solutions to any micro-control or program memory application.

TI Schottky PROM Line Summary

Part Number	Description	Address Access Time	Power Dissipation
SN54S/74S188	32W x 8B, O-C, 16 pins	25ns	400mW
SN54S/74S288	32W x 8B, 3-S, 16 pins	25ns	400 mW
SN54S/74S287	256W x 4B, 3-S, 16 pins	42ns	400mW
SN54S/74S387	256W x 4B, O-C, 16 pins	42ns	500mW
SN54S/74S470	256W x 8B, O-C, 20 pins	50ns	550mW
SN54S/74S471	256W x 8B, 3-S, 20 pins	50ns	550mW
SN54S/74S472	512W x 8B, 3-S, 20 pins	55ns	600mW
SN54S/74S473	512W x 8B, O-C, 20 pins	55ns	600mW
SN54S/74S474	512W x 8B, 3-S, 24 pins	55ns	600mW
SN54S/74S475	512W x 8B, O-C, 24 pins	55ns	600mW

TI Schottky RAM Line Summary

Part Number	Description	Address Access Time	Power Dissipation
SN54S/74S189	16W x 4B, 3-S, 16 pins	25ns	375mW
SN54S/74S200	256W x 1B, 3-S, 16 pins	25ns	500mW
SN54LS/74LS200	256W x 1B, 3-S, 16 pins	35ns	275mW
SN54LS/74LS202	256W x 1B, 3-S, 16 pins	35ns	275/100*mW
SN54S/74S214	1024W x 1B, 3-S, 16 pins	30ns	575mW
SN54LS/74LS214	1024W x 1B, 3-S, 16 pins	65ns	200mW
SN54LS/74LS215	1024W x 1B, 3-S, 16 pins	65ns	200/75*mW
SN54S/74S207	256W x 4B, 3-S, 16 pins	40ns	600mW
SN54LS/74LS207	256W x 4B, 3-S, 16 pins	60ns	300mW
SN54S/74S208	256W x 4B, 3-S, 20 pins	40ns	600mW
SN54LS/74LS208	256W x 4B, 3-S, 20 pins	60ns	300mW

*Power down condition

These PROMs and RAMs are relatively insensitive to temperature and supply-voltage variations. And all have pnp inputs for reduced loading on system buffers/drivers.

Field Programmable Logic Arrays... fast and versatile

The S330/S331 FPLAs provide the means for electrically programming the customized logic patterns that can virtually eliminate the need for SSI/MSI random logic. These high performance FPLAs are organized as 12-input x 50 product terms x 6 outputs in a high-density 20-pin package. They feature an automatic enable which decodes true product terms to permit FPLA expansion without external components. Result – expandable FPLAs with 35-ns typical delay. The three-state output SN54S/74S330 or 2500-ohm passive-pullup output SN54S/74S331 are both priced at $9.00 for commercial version (100 pieces).

Input/Output Functions... simplified interfacing

Also offered are innovative 20-pin high-density interface functions designed specifically to interconnect with the S481 chip set. All functions have bus-driving three-state outputs and high-impedance pnp inputs. Alternatives are available for either synchronous or asynchronous, serial or parallel formats.

These interface functions include:

- SN74S225N – 16w X 5b 10MHz FIFO
- SN74S226N – 4-Bit Bus Transceiver
- SN74S240N – Octal Inv. Bus Driver
- SN74S241N – Octal Bus Driver
- SN74S373N – Octal D-Type Latches
- SN74S374N – Octal D-Type Flip-Flops

All are available now.

Maximum speed. Maximum flexibility. Maximum efficiency. The S481 chip set, the logical choice for implementing advanced mini and midi computers... and super processors.

The components of the S481 chip set are all available now. To order call your local TI sales office or authorized distributor. For your personal copy of TI's Bipolar Microcomputer Components Data Book (LCC-4270), write Texas Instruments Incorporated, P.O. Box 5012, M/S 308, Dallas, TX 75222.

TEXAS INSTRUMENTS
INCORPORATED

63094

CIRCLE 37 ON INQUIRY CARD

Heat Sink Redesign Reduces Costs, Improves Thermal Conductivity

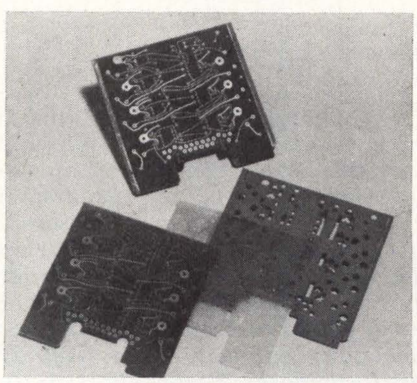
Contracted by Fairchild Industries to produce four aluminum heat sink printed circuits for use in the power switching section of the weapons system in the Navy/Grummon Aerospace Corp, Air Superiority Fighter, The Sibley Co, Bridge St, Haddam, CT 06438 found that the boards were producible only by laboratory techniques. To make production of the boards feasible, they modified the process and design. The resulting design not only reduces the cost by 53% but improves the boards' thermal conductivity.

Original design required a solid sheet of 0.062-in (0.157-cm) aluminum to be drilled with oversized holes that were then filled with an epoxy insulating compound. The drilled and filled aluminum plate was laminated by adding thin copper-clad laminate to either side. After lamination the part was drilled again using smaller diameter drills, and the drilled panels were treated as conventional 2-sided plated-through hole circuit boards. Insulating material was then removed from two edges of the board to expose base aluminum rails to provide thermal conductivity for the heat generated.

Among the problems that the Sibley Co encountered when attempting to produce the boards in quantity were the tendency of the epoxy fill material to shrink and to create air bubbles. Shrinkage caused the area around each hole to assume a dished appearance, making deburring and cleaning impossible. To eliminate the need for this filling operation, three separate items were used: an aluminum anodized heat sink, a 0.010-in (0.025-cm) thick FR-4 unclad insulator, and a 2-sided plated-through hole circuit card having an epoxy mask on one side.

These items are assembled using five eyelets which hold the assembly together tightly and also provide hole to hole alignment of the parts. After several prototypes were constructed, it was learned that the thermal path was shortened because power transistors were mounted directly on the aluminum surface instead of being mounted on etched pads having 0.015 in (0.038 cm) of insulation between them and the aluminum core. While the original version would have required a $69/unit price, the redesigned version is producible at $36.50, a savings of almost 53%.

Circle 151 on Inquiry Card



The Sibley Co's redesign of aluminum heat sink printed circuit boards resulted in both a simplification of the production procedure and improved thermal conductivity. Heat sink, insulator, and 2-sided circuit card (bottom) which make up the boards are assembled using five eyelets, which hold the assembly together and assure hole-to-hole alignment of parts

Intelligent Video Display Terminal Incorporates Thermal Printer

Series 700 model 770 intelligent terminal incorporates reliable, easy to use hardware, including the TMS 9900 microprocessor and semiconductor memory technology, and software. Aimed at significantly reducing mainframe computing and communications costs in distributed processing environments, the unit increases operator productivity by allowing data checking, validation, and data preprocessing at the local site.

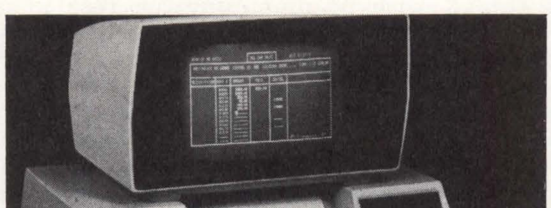
Introduced by Texas Instruments Inc, Digital Systems Div, PO Box 1444, Houston, TX 77001, the 770 terminal incorporates 24k bytes of ROM and from 8k to 24k bytes of RAM, dual 3M DC 100A mini-cartridge magnetic tape drives, a 1920-char video display, and integral communications. Its ASCII typewriter style keyboard has separate numeric, cursor control, and programmable function key clusters.

An alternate configuration provides a built-in 30-char/s, 80-column thermal printer. For applications requiring multicopy printing, the 150-char/s model 810, a multicopy impact printer can be used. This microprocessor-controlled bidirectional printer achieves 150-char/s speed with an effective throughput of from 60 full 132-char length lines/min to 440 lines/min with 10-char average lines. The wire-matrix printhead enables up to six permanent copies to be produced with high clarity and low noise.

Terminal operation is supported by a ROM-resident real-time multitasking executive. The unit's business-oriented terminal processing language TPL 700 simplifies data entry, data processing, and software development functions. A powerful, fill-in-the-blanks forms package features character and field validation using fixed or user-defined range sets, table lookup, substitution, cross-field validation, arithmetic operations, and conditional branching.

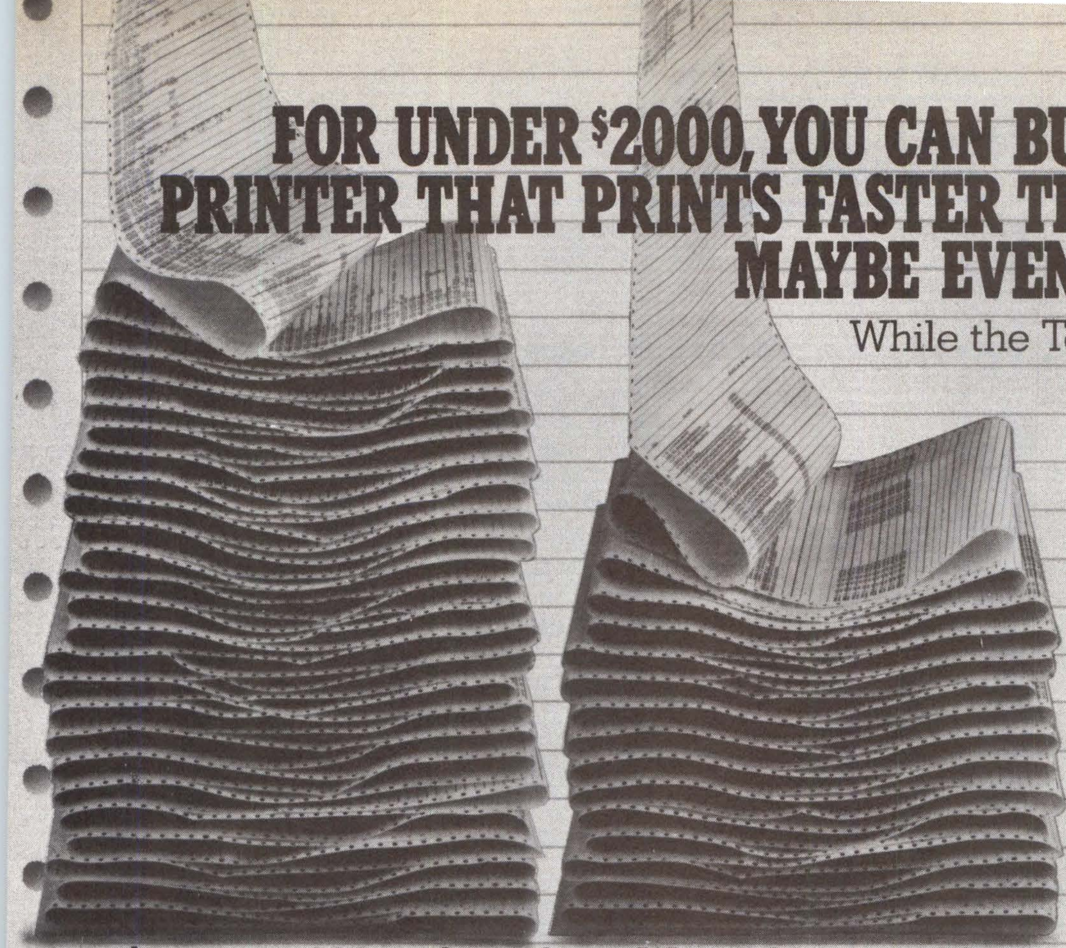
A 3780 emulation package provides direct communication with an IBM host using the EBCDIC code and the binary synchronous communications protocol. Also available are emulators for model 742 programmable terminals and teleprinter terminals using ASCII code. Communications concurrent with data entry and local preprocessing is supported on a 16k-byte system using teleprinter or 742 emulator; with the 3780 emulator a 24k-byte system is necessary.

Standard 770/1 terminal with 8k memory is priced at $6400; the 700/2, which includes thermal printer, has a price of $7500. The 810 impact printer is priced at $2250 with OEM discounts available.



Texas Instrument's 770 intelligent data terminal incorporates a 9900 microcomputer, RAM and ROM, dual minicartridge magnetic tape drives, 1920-char video display, keyboard, and an optional internal 30-char/s printer. Its ROM-resident operating system optimizes terminal operation and makes efficient use of the cartridge media while preventing loss of the operating system during power failure □

Circle 152 on Inquiry Card



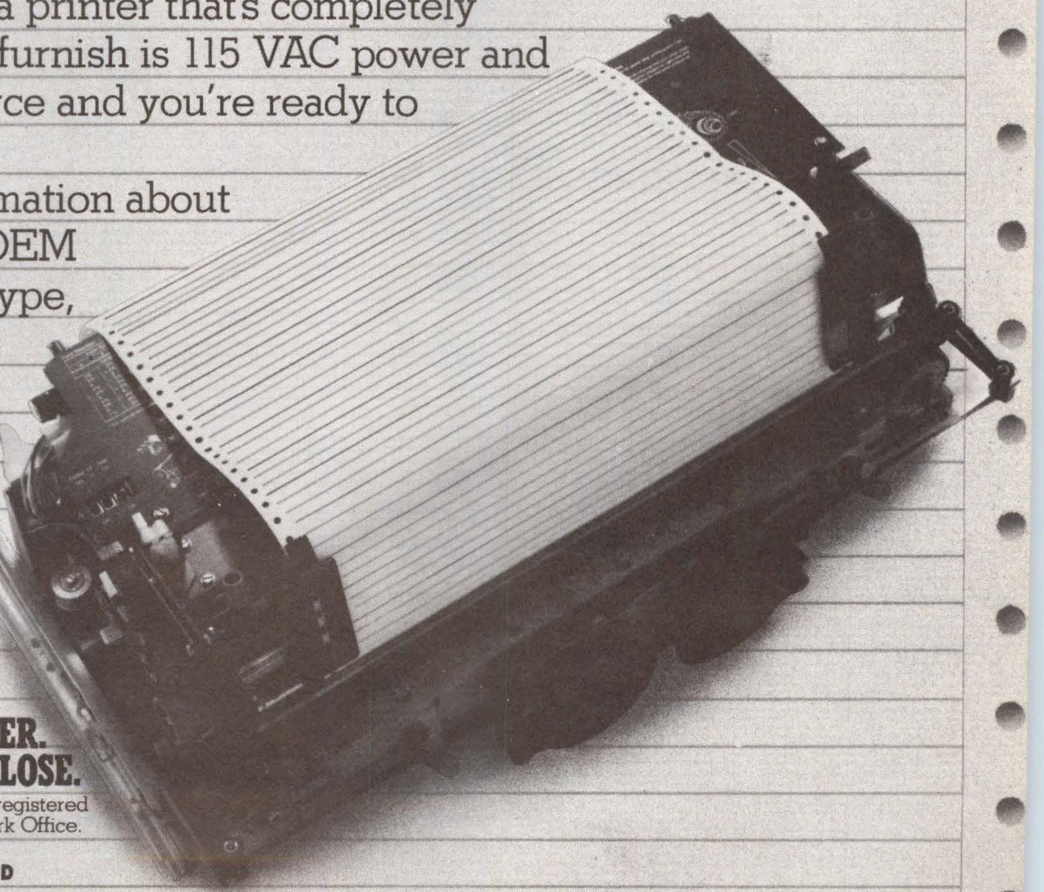
FOR UNDER $2000, YOU CAN BUY A 300 LPM PRINTER THAT PRINTS FASTER THAN 300 LPM. MAYBE EVEN 50% FASTER.

While the Teletype® model 40 132-column printers are rated at 300 lpm (monocase), that figure is somewhat misleading.

Actually, that's quite an understatement since the real printing speed lies somewhere between 300 and 500 lpm. We wish we could pin our speed down tighter, but throughput takes into consideration a couple of variables. Like different character type belts and an almost infinite number of data patterns.

But speed isn't all we offer for less than $2000. Because for that money you also get a printer that's completely operational. All you furnish is 115 VAC power and the serial signal source and you're ready to go on-line.

For more information about Teletype model 40 OEM printers, write: Teletype, Dept. 71-P, 5555 Touhy Ave., Skokie, IL 60076. Or call: 312/982-2000.



TELETYPE

THE TELETYPE® MODEL 40 OEM PRINTER. NOTHING EVEN COMES CLOSE.

CIRCLE 38 ON INQUIRY CARD

Computers Oversee All Activities of Tower Restaurant

Diners at the gourmet restaurant rotating 1150 feet up in the CN Tower in Toronto, Ontario, Canada are never aware—and have no need to be—that two computer systems have controlled nearly every phase of their seating at that restaurant from the time they telephoned for reservations until the maitre d' escorted them to their tables—and will print their checks when they are ready to leave. Even the purchase of food and other items which assure that each diner will be able to order his favorite dishes from the menu are controlled by one of the minicomputers in the system. They handle reservations, cancellations, inventory, menu control, billing, purchasing, accounting, payroll, and security, and even notify when tables are vacant and set up for new diners.

Several Canadian firms were involved in the design and installation, in addition to the CN Tower organization and the component manufacturers. HiTech Canada Ltd of Ottawa and Montreal had responsibility for project management and coordination; Minitech Information Systems Ltd of Montreal and Toronto provided computer hardware and software systems; and Toronto-based Integrant Minicomputers Ltd coordinated and managed site preparation and installation of equipment. In addition, Digital Devices Ltd, a Montreal firm, designed and produced some of the hardware support systems.

System Description

Restaurant operations and management are implemented by two computer systems, each containing a Data General Nova 2/10 minicomputer with 64k bytes of core main memory, a Media III 32k-byte "swapping core" memory, and a Xerox Diablo 44 magnetic disc unit with 10M-byte capacity. One of these systems, designated system "A," normally operates online and interfaces with five Hazeltine 2000 CRT display/keyboard terminals used by reception/reservation clerks (three at the base of the tower and two in the basement), similar CRT terminals at maitre d' and system monitor stations, and two more CRT terminals with associated General Electric Terminet printers at cashier stations. A Dataprinter 300-line/min chain printer provides hardcopy reports.

System "B" performs accounting and other office functions but can be switched online to assume all duties of system A should that computer fail. Three additional 10M-byte disc drives and four more CRT/keyboard terminals (master and three slaves) are attached to system B for dedicated purposes. (One slave CRT can be switched to system A if required.) When system B is placed online, its operations are held in memory on the disc packs until it returns to its accounting functions.

The 1815-ft (553 m) high CN Tower is primarily a TV and FM broadcasting facility and, as such, produces intense electromagnetic radiation. Spikes introduced by the broadcast signals into the ac input of the computer power supplies normally would be detrimental to computer operation. This major problem was overcome by a voltage regulation/filter/isolating transformer system which smooths out potential voltage variations to condition the input line.

In addition, all tower-restaurant data transmission cables from the computers and backup devices (located in the tower basement beneath the pool) to the input/output units in the restaurant and at the base of the tower are fully shielded and grounded. Data links are connected through line drivers, modems, and concentrators to assure signal compatibility. Bell Canada telephone lines which maintain the computer-device interconnections run down the central core of the tower.

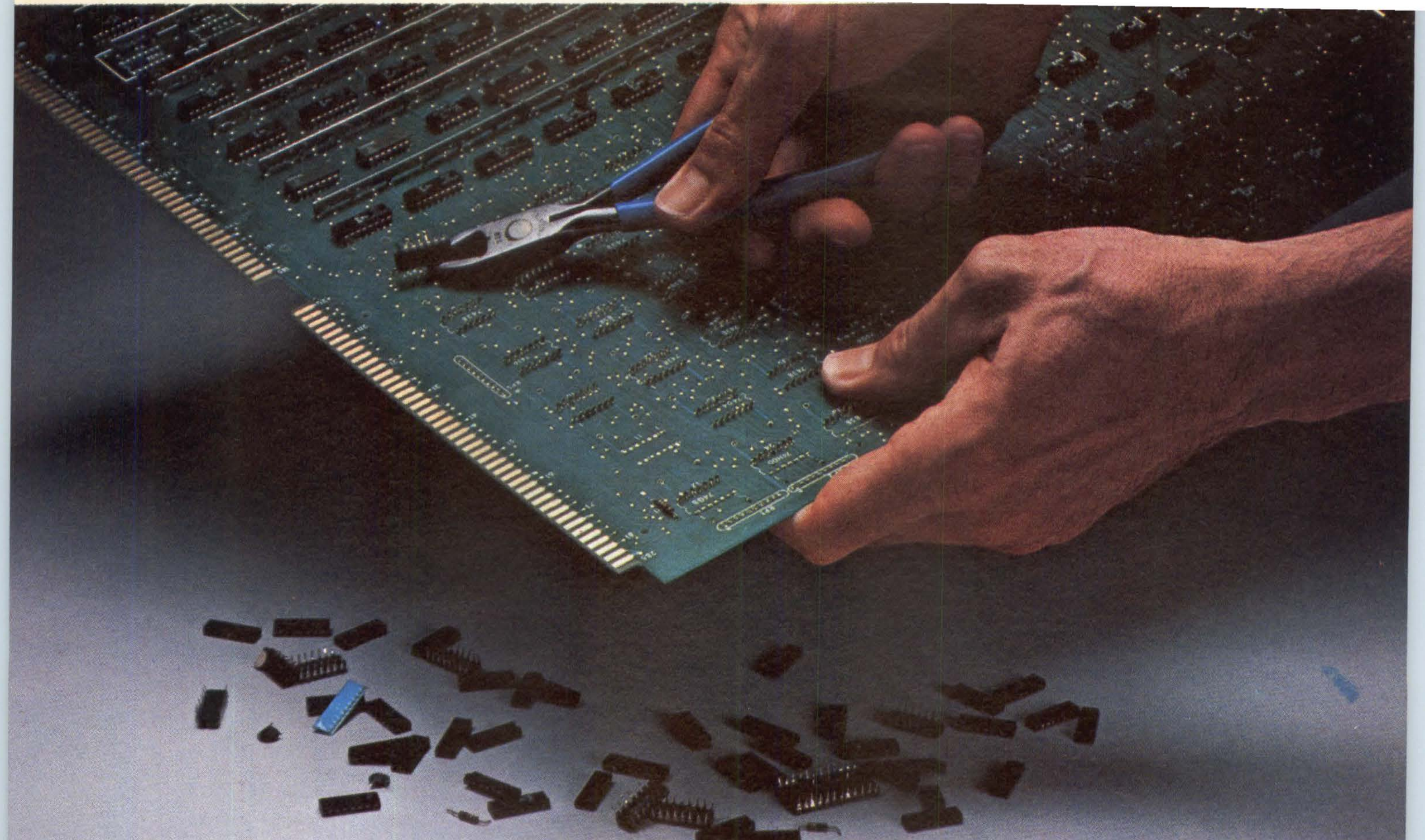
The System in Operation

Other than for summer or special weekends, reservations need not be made far ahead. However, the computer structure permits reservations to be accepted up to one year in advance.

Each of five reception/reservation clerks communicates with the online computer through an interactive CRT terminal with keyboard. When a reservation request is received by telephone, the clerk calls up a formatted display for the desired time period to show which tables are already assigned. If a table is available, the clerk reserves it by entering information on the keyboard.

When guests arrive at the reception area at the base of the tower on the specified date, the receptionist recalls reservation details from the computer to confirm them and assigns a table from a CRT display of currently unoccupied tables. If no tables are available at that time, guests are given a lantern-like paging device and are asked to wait in one of the pool lounge areas. As soon as the display indicates that a table is vacant and set up, the receptionist enters the pager number of the waiting guest into a notification control panel. This transmits a signal along a concealed inductive wire loop surrounding all lounge areas and causes the corresponding lantern pagers to begin blinking. Up to eight pagers can be controlled by the panel at one time. Effective receiving distance is about 20 ft (6.4 m) from wire to pager.

Waiters in the restaurant indicate table availability via TRW keyboard pads located at 10 stations on the rotating ring and two stations in the central bar. When



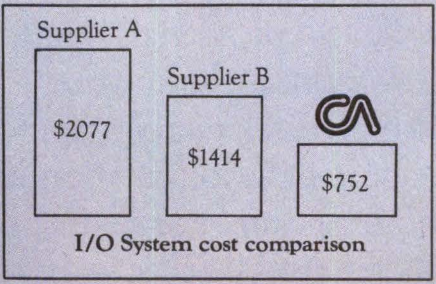
We figured a way to cut the cost of interface in half.

So what?

So OEM's are dancing in the streets, that's so what. At least the pros are.

And what makes it such a big deal is the magnitude of the cost savings—possibly 20% or more per computer system.

One reason is that interfaces are generally long on duplication and short on common sense. Most interfaces, for example, faithfully repeat half or more of the circuitry on all the other interfaces. And with multiple interfaces, that gets to be a pretty expensive proposition.

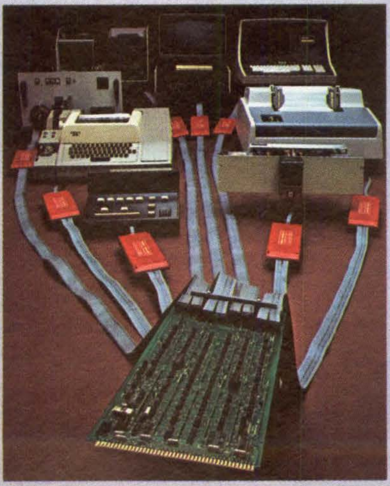


I/O System cost comparison

So we came up with the solution you see here: The Distributed I/O System. Designed to work specifically with our line of NAKED MINI® computers.

And once you get by its unorthodox appearance, the logic of it becomes pretty appealing. As do the cost savings.

All the basic circuitry is located on a single half-card I/O



The Distributed I/O System

Distributor, which can be shared by as many as eight "Intelligent Cables." Packaged into every cable is an integral PicoProcessor, which handles the functional control for each interface.

This arrangement allows much smaller computer packages, since only one I/O board is housed inside the computer cabinet.

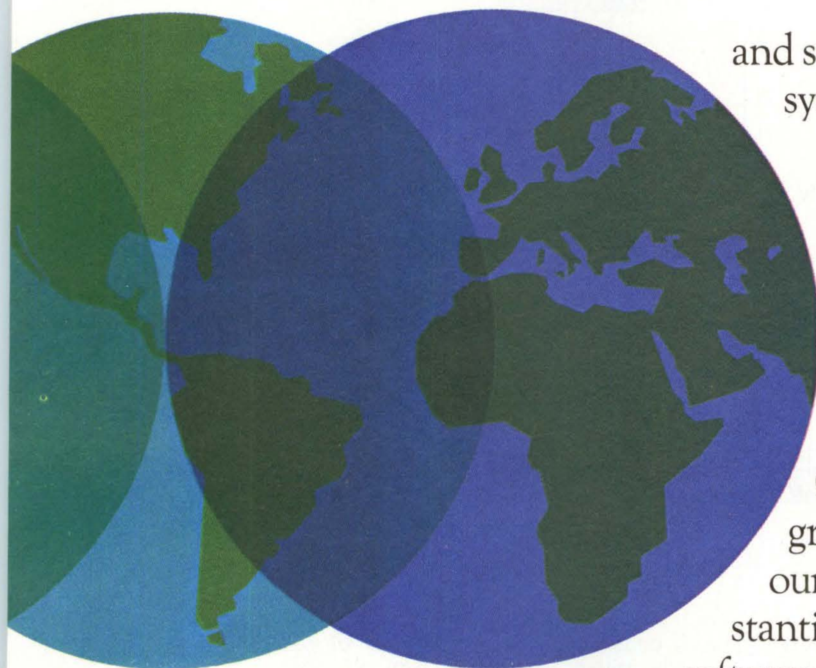
And along with a smaller package, comes a smaller price.

The I/O cost comparison at left shows the savings on a typical four-interface system (2 CRT's, 1 line printer and 1 card reader). And since our System handles up to eight interfaces, imagine your savings using its full capability.

Consider ComputerAutomation's Distributed I/O System. It's an uncommonly sensible solution to a commonplace problem. From the price/performance people who brought you the NAKED MINI®

ComputerAutomation
NAKED MINI® Division
18651 Von Karman, Irvine,
California 92713, (714) 833-8830

computers to keep you changing world.



and symbolic debugging to help reduce system integration and debug time.

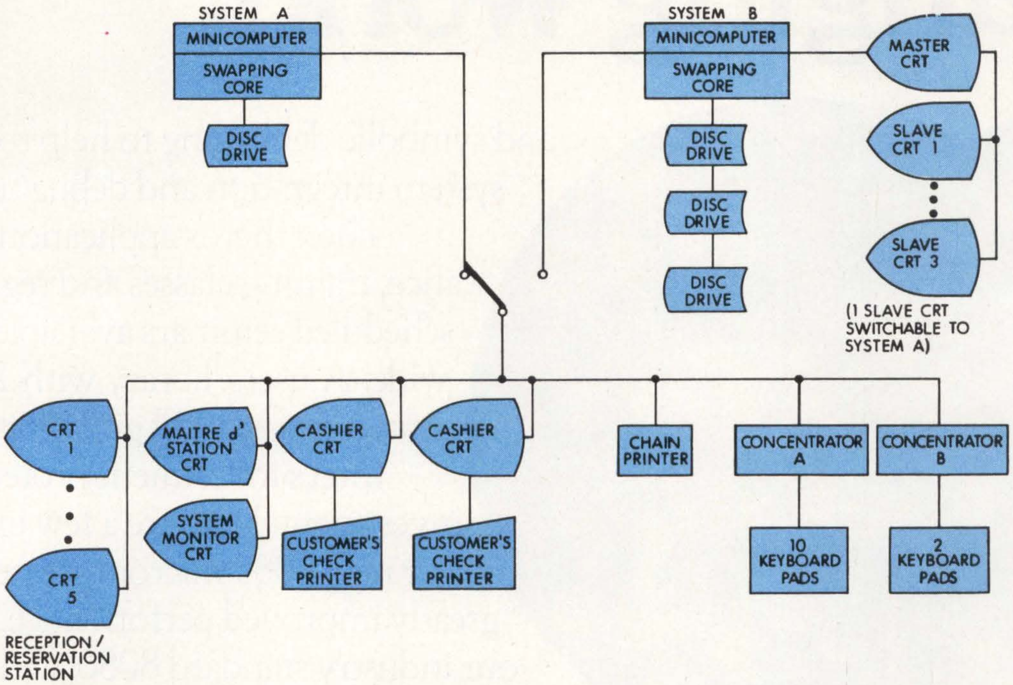
Then there's application assistance, training classes and regularly scheduled seminars available worldwide. A users' library with 235 programs and still growing.

Intel's investment protects your investment. Here are a few examples. Our new 8085 microprocessor offers greatly improved performance over our industry standard 8080, with substantial cost savings. Yet you use the same software, the same peripheral, memory and I/O circuits as the 8080. You don't have to go through a new learning experience or re-invest in software to upgrade your system to 8085 performance. And that same kind of protection comes when you invest in an Intel development system. Last year's investment in an Intellec system is preserved even when we introduce a new microcomputer. Our newest 8085 and 8748 microcomputers are now fully supported with development software for your present Intellec system. And you will soon be able to add low cost ICE-85 and ICE-48 in-circuit emulation modules.

Let Intel help you stay ahead. Get started now by asking for our new microcomputer product line brochure describing the full line of Intel microcomputer products, systems and software. Use the reader service card or write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051.

intel® delivers.

Circle 40 for technical information.
Circle 41 for technical information and a demonstration.



Two complementary but non-redundant computer systems control and record aspects of restaurant in Toronto's CN Tower. One computer is normally online, in contact with all operational phases of the restaurant; the second is then used only for accounting and record keeping. However, the second computer can be switched online if the first unit malfunctions

a table is cleared and reset for new guests, a waiter presses relevant designation keys on one of the pads to notify the receptionists and to identify the table.

Other units located at the restaurant level include a CRT display terminal at the maitre d' station and two CRT terminals with associated printers at cashier locations. Architecture of the tower obscures most of the restaurant area from direct view at any single location. In addition, the restaurant is quite large and most of it is moving relative to the central area. Therefore, the maitre d' station CRT station is provided to enable access to information such as table status, patron location, and current restaurant activity.

Food and beverage orders are recorded by waiters on precoded requisition forms which are then given to one of the cashiers. Order information is transcribed into the system via special displays. The computer opens a bill for the table, redisplays it as additional sales are input, and—on demand—computes the sales tax and orders the printer at the cashier's station to print a completely itemized customer's check, including menu description, amounts ordered, and prices. Payments are entered into memory for processing by shift end and night auditors.

Computer processing by system B continues with both accounting of daily records and predictions for future purchasing. Invoices are automatically generated for credit card transactions. System B operates on a 24 hour/day, 7 day/week basis since much of the auditing is performed at night.

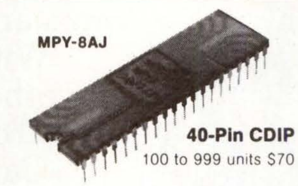
Among the many other accounting and record-keeping duties of the system, sales data are collected by menu item for each shift and converted into units sold and on hand for analysis of future requirements. The computer performs a "menu explosion" in that it determines all complementary items that are needed for preparation of the listed menu items. For example, it predicts the number of each item on the menu that will be needed for a specific period and then determines what smaller items will be required to prepare those menu items. Thus, all necessary particulars will be ordered by the steward, eliminating the chance of human forgetfulness.

Circle 160 on Inquiry Card

the Fastest Biggest Bipolar Multipliers you can buy

130 ns

MPY-8AJ

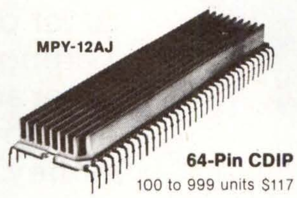


40-Pin CDIP
100 to 999 units $70

8 by 8 Bits – Ideal for on-line multiply in micro and mini computers – operates directly on most data bus lines – consumes only 1.8 watts (typical)
Price $100 each in 1-9 quantities.

150 ns

MPY-12AJ

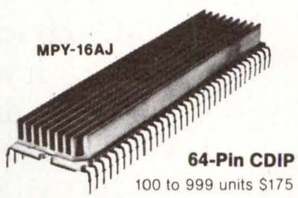


64-Pin CDIP
100 to 999 units $117

12 by 12 Bits – New size multiplier for data communications and Signal Processing – needs only 3-1/2 watts for room temperature operation – single TTL Clock – fully TTL compatible – Price $168 each in 1-9 quantities.

160 ns

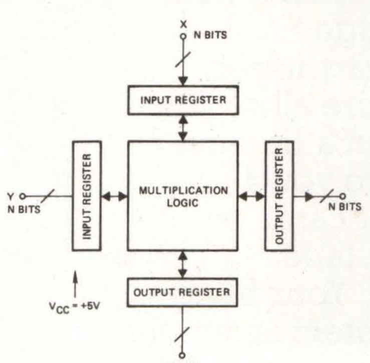
MPY-16AJ



64-Pin CDIP
100 to 999 units $175

16 by 16 Bits – Smaller chip improves performance – 64-pin DIP easy to use – dissipates 5 watts with built-in heat sink – perfect for micro/mini applications – signal processing – price $300 each in 1-9 quantities.

FULL MIL-TEMP RANGE NOW AVAILABLE



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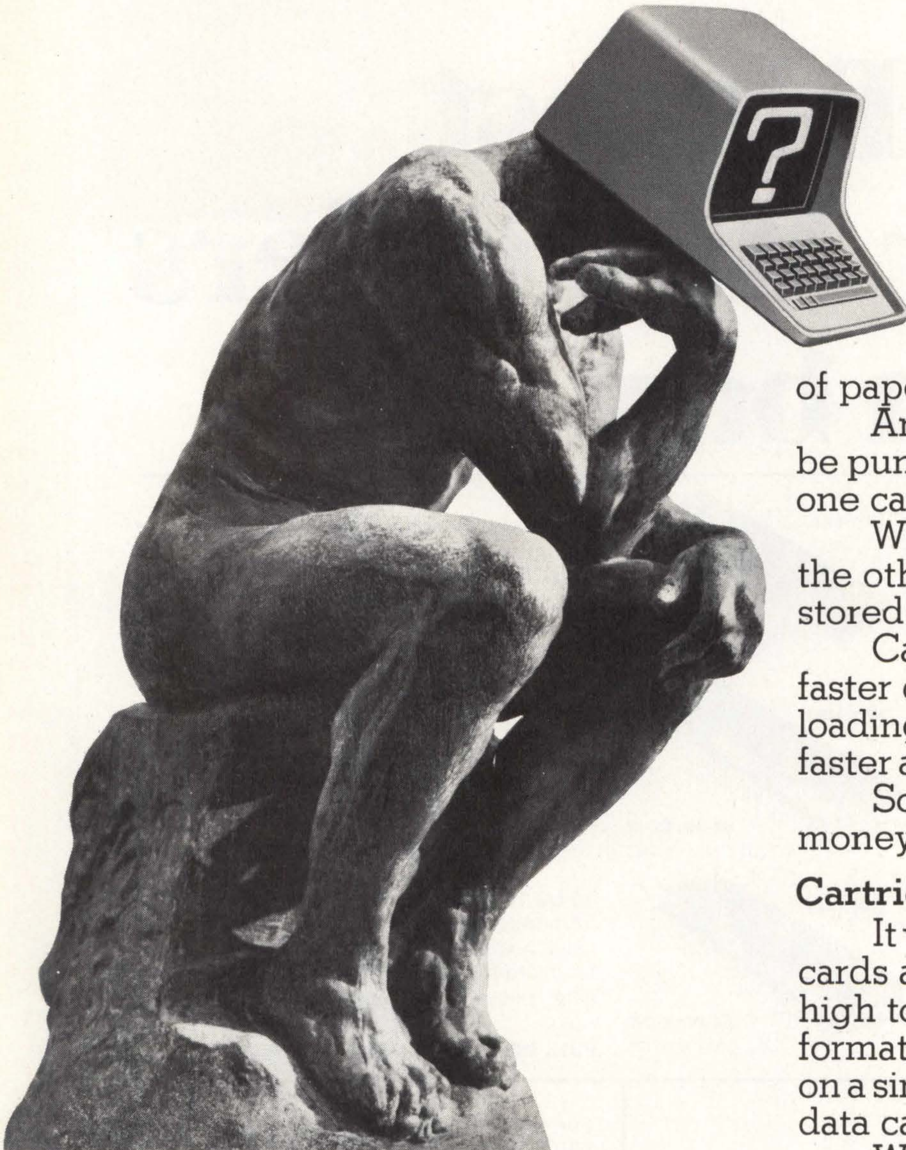
Is your computer smart enough



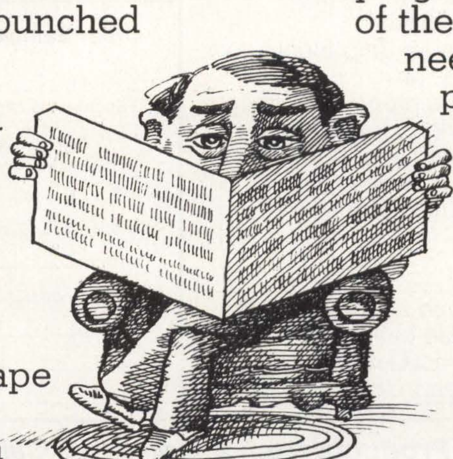
A 3M peripheral drive which uses 3M data cartridges is better than any drive which uses punched cards or paper tape.

And, if you'd take the time to ask it, your computer would probably tell you so.

It's simple logic.

Cartridges are faster than cards.

Cards and paper tape are slow. It takes hundreds of cards for a single computer program.



Cards must be read one at a time.

Or hundreds of feet of paper tape.

And each program must be punched, verified and read one card at a time.

With our drive system, on the other hand, programs are stored on a single tape cartridge.

Cartridges offer much faster data storage, program loading, data transfer and faster access to the computer.

So you save time and money.

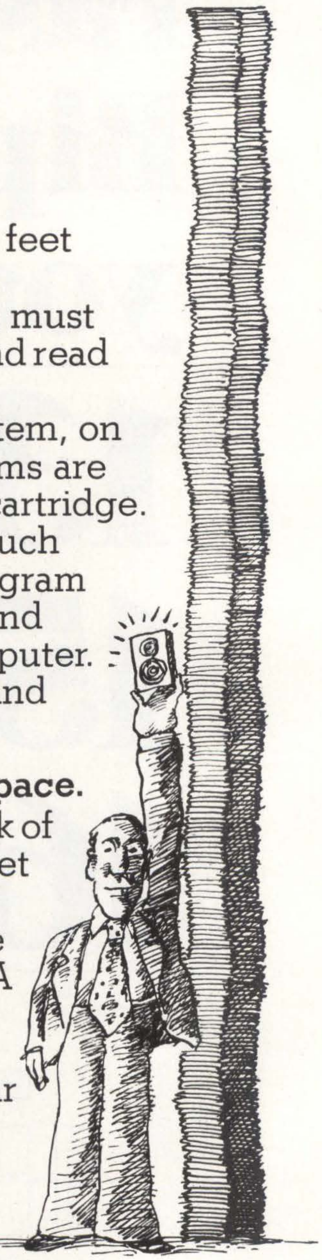
Cartridges take less space.

It would take a stack of cards almost sixteen feet high to store all the information you can store on a single 3M DC-300A data cartridge.

With cartridges, you can store all of your programs in a fraction of the space you'd need for cards or paper tape.

Your filing system is simplified and overhead is greatly reduced.

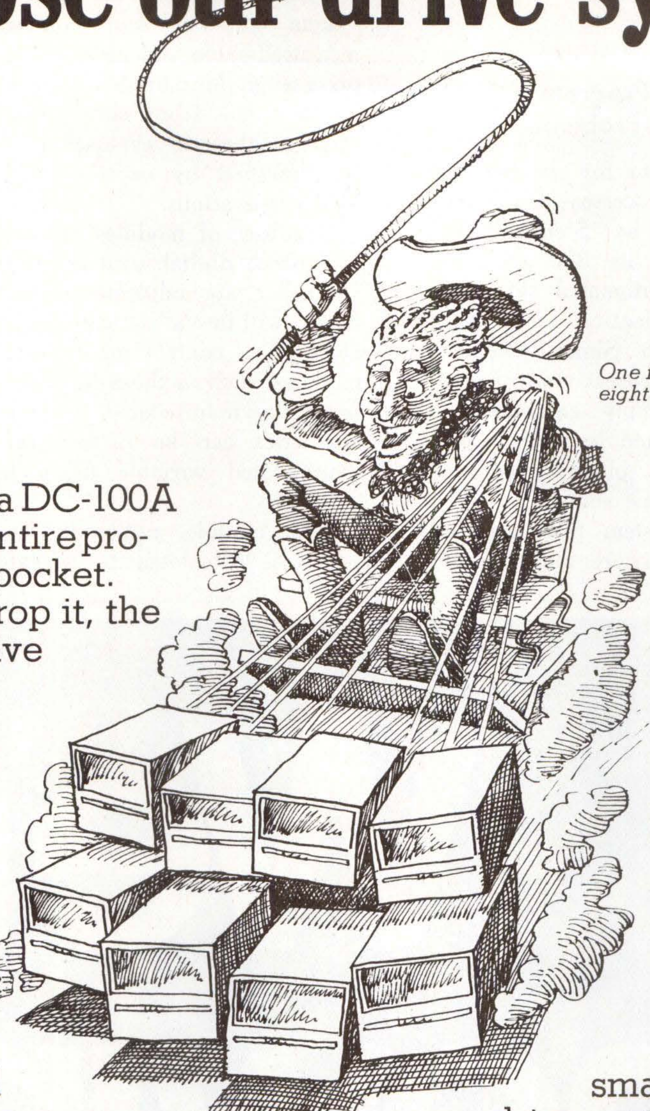
One DC-300A cartridge equals almost 16 feet of cards.



Cartridges won't fold, spindle or mutilate.

Unlike paper cards, you need never touch the media. It's well protected inside the cartridges, so it's virtually impossible to damage.

to choose our drive system?



One formatter can control eight drives at once.

You can carry a DC-100A cartridge with an entire program in your shirt pocket.

Even if you drop it, the program will survive unscathed.

Remember that the next time you drop a stack of cards!

Don't take our word for it. Ask your computer.

If you'll send us the coupon, we'll send you the specifications for all three of our drive systems.

Ask your computer to compare them with any other type of drive system.

We'll bet your computer will prefer ours.

Maybe it'll choose our famous DCD-3 drive. It's people-proof, jam-proof and wear-resistant.

Or maybe your computer will decide upon our DCS-3000 series, an ANSI-formatted system that allows one formatter to control up to eight drives.

The DCS-3000 is extremely easy to integrate into your system. Only one cable to the user's logic is required.

But if you require compact size, your computer will probably choose our unique DCD-1. It offers many of the features of our bigger systems, yet it will fit inside a five-inch cube.

The cartridge alone measures just 2.4 x 3.2 x .5 inches.

See for yourself at the National Computer Conference.

You can see all three of our drive systems at the Dallas Convention Center, June 13-16. You'll find them in booths 1621-1623.

Study them carefully.

If your computer isn't smart enough to choose our drive systems, we'll bet you will be.

Send me more information.

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St. Paul, Minnesota 55101

CIRCLE 43 ON INQUIRY CARD

Modular User-Oriented Program Solves Repetitive Process Problems

A standardized, user software system for the automation of complex, medium speed processes—0.1-s scan cycle time—has been developed by Siemens AG, Federal Republic of Germany for its 320 and 330 process computers. Most such automated processes necessitate repeated solution of identical or similar problems in different plants. With Simat (*Si*emens auto*mat*ion software package) the process control engineer implements a system by simply combining a number of ready-made program modules. Since programming is not necessary, system planning time is reduced, and the system can go online sooner.

Programming is replaced by system planning and implementation with the aid of software modules and components. Once the technological problem has been solved and a function flowchart has been established, system modules and components are selected for measured-value and binary signal acquisition and alarm processing. Measured-value processing includes a range of functions from simple limit checking to sophisticated arithmetic evaluation; binary value processing is simplified by decision table modules for complex logical operations.

A subset of modules allow the computer to be used for direct digital control. Individual steps of such a controller are implemented by a sequence of module calls within a so-called block, whereby specific closed-loop control modules can be mixed with other modules, such as those for open-loop control. Algorithms form the manipulated variables, and controller characteristics can be further refined by calculating the manipulated variable using higher order differential equations.

One module produces an instantaneous setpoint which is calculated by an algorithm from the input setpoint (follow-up controller.) The module is used, for example, for the synchronized startup of plant sections. Each controller is represented by a block and can be activated or deactivated by operator commands.

The system incorporates a comprehensive open-loop control concept with logic and sequence control functions in flexible combination with arbitrary arithmetic operations, monitoring, and closed-loop control functions, as well as flexible message processing and logging. Test functions are also available. Decision table modules and/or logical operators of the universal arithmetic module can be used for the Boolean operations involved in simple interlock schemes.

The main sequence control module is the step control element. A single-step mode of operation is also possible for commissioning purposes to check all the control paths. In this case, each step must be followed by an acknowledgement from the operator. Operator input aids are available for general commissioning purposes.

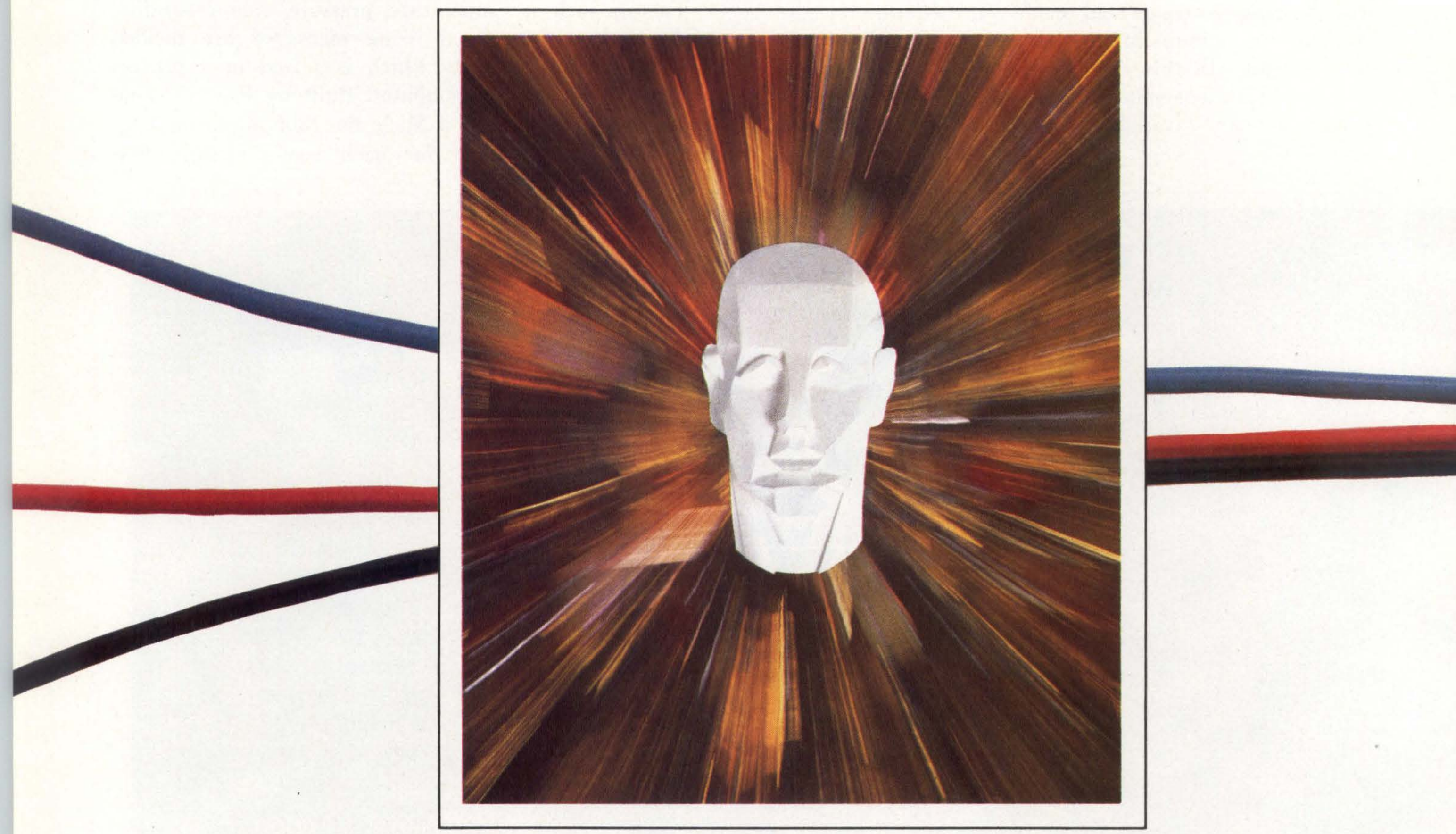
Microcomputer Automates Petroleum Flow Measurement

A microcomputer-based system which automatically measures the flow of liquids, gases, or steam has been developed by UGC Industries, Inc of Shreveport, La for use by petroleum processors. The Microflo system can calculate in units of measurement preferred by the user: eg, volume, mass, or standard 60°F barrels. It is presently being used by major oil and chemical companies including Shell Oil, Phillips Petroleum, Continental Carbon, and Dow Chemical for such applications as measuring ethane-propane mixed streams, measuring crude oil flow through long distance pipelines, and metering at custody transfer points along pipelines.

Factors such as temperature, pressure, compressibility, and gravity of material being measured are melded into a complex equation which is solved in a process automated by a microcomputer. Built by Process Computer Systems, Inc, Saline, Mich, the 1806 microcomputer is custom programmed for each user's specific flow

Stretch your mind. Think Amphenol® connector systems.

Don't back off from your big idea. We can help you make it work. And work right.

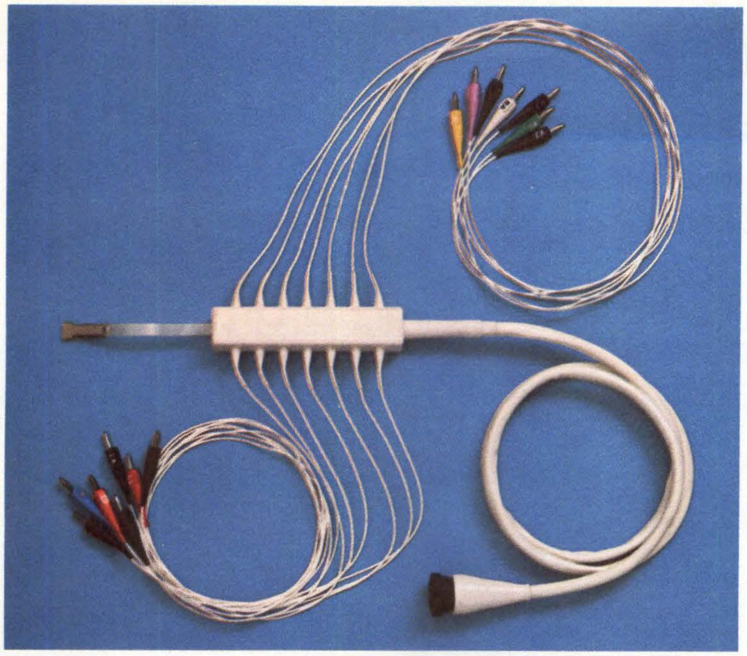


Dare to be different. We'll back you up with Amphenol connectors. We may already have the kind that'll make your big idea work.

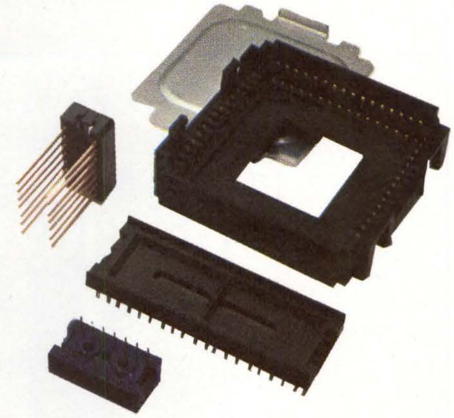
But if we have to create something totally new to match your idea, we'll go all out—even to designing the required termination tooling. Our connector design specialists are known for the way they tackle the unknown. With a spirit that yields the answers.

Think of it this way: we can help you avoid a lot of false starts. And give you measurable quality and economy. The people who use the Amphenol connectors shown here know that's true. They think of us first when they need connectors for consumer and business products, data and word processing equipment, aerospace and military applications, telephony, and more.

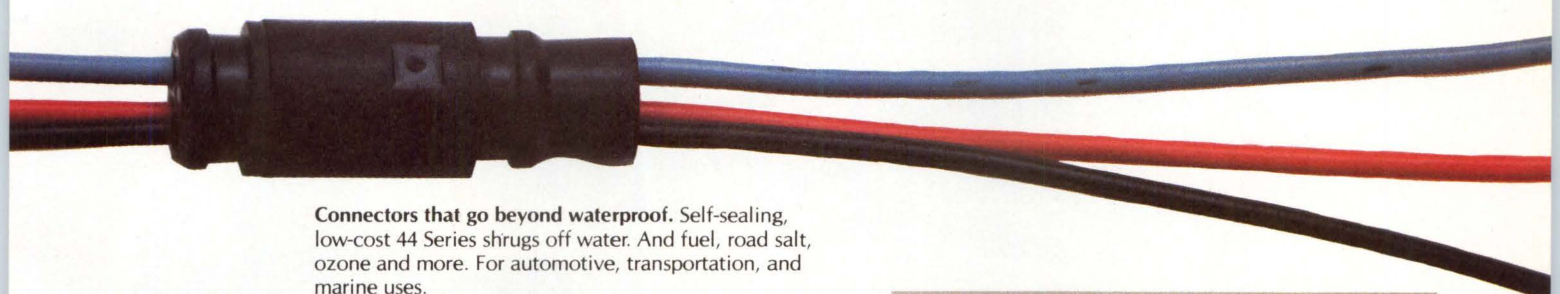
Got a mind-stretching idea? Then include Amphenol connectors in your thinking. To get started on the right track, just call us at (312) 986-2320 or write to: Amphenol North America Division, Bunker Ramo Corporation, Dept. **L-57** 900 Commerce Drive, Oak Brook, Illinois 60521.



Medical interface cables for critical applications. Provide reliable patient monitoring and medical electronics interface. Custom-made for reliability, good looks.

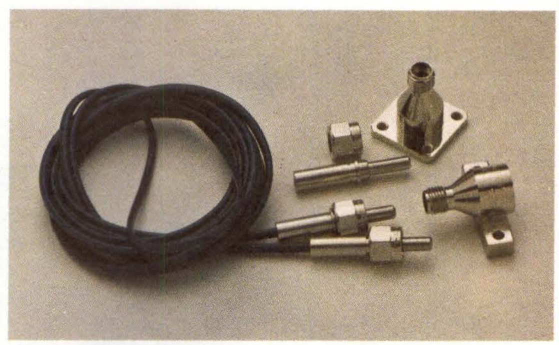


No more unsoldering for IC replacement. Dual-inline IC's or planar leadless MOS/LSI's plug right into 800 Series devices.



Connectors that go beyond waterproof. Self-sealing, low-cost 44 Series shrugs off water. And fuel, road salt, ozone and more. For automotive, transportation, and marine uses.

Rack-and-panel connectors that advance the state of the art. 94 Series environmental connectors utilize polymer-retention discs to retain the 20, 16 and shielded size contacts.



Precision optical connectors from stock. Optimum components for emitter-to-cable, cable-to-detector, and cable-to-cable junctions. All with standard SMA size mating.

A way to slash telephone key-set installation costs. System 66 connectorized blue-field panels are pre-wired. No cables to punch-down.

The right idea at the right time.

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CIRCLE 45 ON INQUIRY CARD

And you'll find our impact is exceptional.

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Compare the new Model 810 Printer with any other printer you are using or considering. We believe you'll find that the 810's reliable, microprocessor-controlled printing results in the highest throughput per dollar and lowest cost of ownership.

The 810 is ideal not only for OEM's but as a peripheral printer for the TI model 770 Intelligent Terminal and the 990 Mini/Micro Computer Family.

Plot our standard features.

The 810 printer has exceptional standard features too. Like bidirectional printing at 150 cps. No paper tape programming. Adjustable tractors for a variety of form widths. A 9 X 7 wire matrix character font for high-quality printing of an original and 5 copies. Bottom and rear paper loading. Speeds from 110 to 9600 baud. And 6 or 8 vertical lines per inch. Add to these the 810's tested reliability and the result is *performance*.

Add a full line of options.

With Vertical Forms Control, you get non-volatile storage of up to 8 different vertical forms. And with Forms Length Control, you can have 11 switch-selectable stored form lengths, from 3 to 14 inches plus 1 programmable form. The compressed printing option lets you print 132 columns in 8½ inch width. And foreign character sets are available as well as interfaces for most applications.

A company you can rely on.

A valuable feature of any Texas Instruments product is after-sale support. When you purchase your 810 Printer, you're getting support from a worldwide network of factory-trained personnel. And maintenance contracts are available.

With the Model 810, you can be sure your total cost of ownership is the lowest possible. And printer performance the highest. For a demonstration of the Model 810, or more information, just mail the coupon. Or call your nearest TI sales office, or (713) 494-5115, ext. 2124.

You'll like the 810's impact.

Yes! I am interested in the new Model 810 Printer.

☐ Please send me more information.

☐ Please have your representative call me.

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See Texas Instruments products at Computer Caravan and NCC.

measurement requirements. When preselected parameters such as pipeline diameter or orifice size are later changed, the microcomputer can be reprogrammed on site with the Microflo's keyboard console. A field replaceable p/ROM in the microcomputer eliminates the need for the user to send hardwired memory back to the manufacturer for reprogramming.

The basic flow calculator accepts any combination of up to 16 analog inputs and provides two analog outputs. Adding I/O modules provides additional analog inputs.

Points along a pipeline can be monitored for variations in basic flow conditions, such as a sudden change in pressure. The system can provide data to downstream processing operations and control such functions as merging the correct mix from multiple streams of liquids or gases. In addition, it can be used to verify costs from outside suppliers, control internal flow operations, and determine the billing to downstream industrial customers.

NC Milling Machines Form Space Shuttle Heat Shield

Five numerically-controlled milling machines will be used by Lockheed Missiles & Space Co in manufacturing the heat shields for NASA's Space Shuttles. Each shield, made up of thousands of all-silica tiles, will comprise 70% of a Shuttle's outer skin. More than 165,000 tiles will be provided for the five spacecraft.

To assure aerodynamic integrity, each tile is assigned to a specific location in the shield and the bottom of the tile is machined to precisely match the Shuttle's surface contour at that point. As a tile travels through the manufacturing process it is always accompanied by a punched paper card containing information pinpointing the tile's intended location on the finished spacecraft.

Milling instructions for all tiles are encoded on a magnetic tape prepared by Rockwell International, the Shuttle's prime contractor. This tape contains a full definition of the spacecraft's geometry. Lockheed has extracted data from the portion concerning differences in contour between closely spaced points on the spacecraft's surface and translated them into a computer language that can be understood by a milling machine's control unit. Those data are then stored in the memory of the minicomputer.

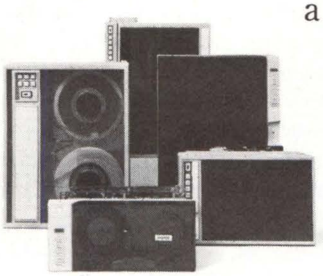
When tiles are to be milled, their associated punched cards identify what portions of the computer's memory relate to the specific milling to be accomplished. Once punched cards are inserted in the machine's control unit, the milling equipment operates in robot fashion with information from the computer directing height, length, and width of the cutter's path. As many as 50 tiles are milled at one time. □

It takes a lot of drive to make ends meet today.

We hate to see OEM frustration—the kind caused when you can't close the gap between advancing computer technology, and your peripherals' ability to fit in with your plans. Just coming "sort of close" won't do anymore.

Getting things together is a specialty at Pertec. We're industry-watchers, as well as seasoned participants—trust us to pinpoint exactly what you're going to need...often even before you do. To help you realize the full potential of state-of-art CPUs. With much greater cost-effectiveness.

Take our tape drives. (Please.) Already available in more than 400 line-variations—but we didn't stop there. Not Pertec. We anticipated your need for a super-fast, sophisticated tape transport, to handle high volume dp throughput.



The result: our new T1000 family, a *new-generation* in vacuum column drives. 75 to 125 ips; dual density for now, but designed to handle GCR high density recording.

We're devoted to your disk demands too. Rigid or flexible. Both fixed-and-removable. From 0.25 Mb to 50 Mb.

And we didn't give you 50 megabytes by forcing a switch in technology. We simply *expanded* our D3000 Series to include 25-50 Mb units. As extensions to an *existing* line. With technology and parts commonality you're already used to. 50 Mb, without major logistic support changes...without special pre-recorded media.

All Pertec drives are built to *stay* together too. Reliability's a big number with us. Like testing at every manufacturing stage, with 40-hour burn-ins. Like setting up the biggest direct sales and service organization of any independent peripherals manufacturer. Like our toll-free 800 line, for 24-hour, 7-day emergency assistance from strategically located parts-and-repair depots around the world.

Pertec's product families are ready when you are. With on-target solutions—regardless of capacity, speed and performance specs...it's a snap with Pertec.

Get together with Pertec peripherals: write Pertec, 9600 Irondale Avenue, Chatsworth, California 91311. Or call the Pertec regional sales office nearest you: Los Angeles (213) 996-1333. Ann Arbor (313) 668-7980. Hudson, New Hampshire (603) 883-2100. London (Reading) 582-115.

PCC PERTEC

a division of Pertec Computer Corporation

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CIRCLE 48 ON INQUIRY CARD

Dr Portia Isaacson
Conference Chairman

Mark Shepherd, Jr.
Keynote Speaker

Dr Robert R. Korfhage
Program Chairman

1977 National Computer Conference

Dallas Convention Center, Dallas, Texas, June 13-16

Key elements of innovation and relevance combine to form the basis of the '77 NCC Great Computer Roundup intended to stimulate the imagination, interest, and interaction of attendees. In consideration of the consumer-oriented aspects and decreasing cost of computing power and its implications, this year's conference has been planned to provide a vital learning experience for users, managers, specialists, and individuals. Under the direction of Dr Portia Isaacson, assistant professor of mathematical sciences at the University of Texas at Dallas, as Conference Chairman, and Dr Robert R. Korfhage of the Dept of Computer Science at Southern Methodist University as Program Chairman, the Technical Program contains approximately 100 sessions featuring indepth coverage of such areas as design, specification, evaluation, and operation of systems; networking; programming; microprocessors/computers; architecture; hardware; education; management; and health care. Special emphasis is being placed on roles, responsibilities, and limitations of persons involved with computers as well as the impact of computers on the individual and society. The conference is sponsored by the American Federation of Information Processing Societies, Inc, the Association for Computing Machinery, the IEEE Computer Society, the Data Processing Management Association, and the Society for Computer Simulation.

The program is divided into four major areas of analysis: computing technology, management issues, data processing applications, and the individual in the computer age. *Technology of computing* includes software engineering, networks, programming, and architecture, with sessions covering design, development, and manufacture of minicomputers, microprocessors, and data base systems. *Management and computing* discusses personnel recruitment and training, as well as the use of computers for management techniques, auditing, accounting, analysis, marketing, and forecasting. *Uses of computing* range from general areas of retail, small businesses, banking, and health care to specialized fields such as petrochemicals. *The individual and computing* deals with the current and future influence of computers; sessions touch on careers, privacy, crime, legislation, errors, and hobbies.

Of particular interest is the Personal Computing Fair and Exposition offering an exhibit of personal computing products, plus two days of paper, panel, and workshop presentations. Reflecting the growth and promise of this field, the Fair will feature operational displays and demonstrations of individually and group-owned noncommercial projects, for which prizes and awards will be presented. A commercial exhibition by equipment manufacturers and suppliers will also display personal computing products and services. The programs on Wednesday and Thursday will feature sessions which examine in depth the personal computing field; in addition, a National Personal Computing Club Congress is planned to allow club representatives to exchange ideas and discuss issues.

A program of eleven one-day professional seminars under the direction of Dr Ronnie G. Ward of the Computer Science Dept of the University of Texas at Arlington will be held during the week. On Tuesday, Adam Osborne of Osborne & Associates, Inc will present Microprocessors; Peter Freeman and Anthony Wasserman of Software Engineering Consultants will discuss Software Design Techniques; and Ira W. Cotton of Computer Network Associates will direct Introduction to Computer Networks. Wednesday's sessions include Introduction to Software Physics lead by Kenneth W. Kolence, Institute for Software Engineering; and Structured Design to be presented by Edward Yourdon, Yourdon, Inc. Completing the sessions on Thursday, Leo J. Cohen, Performance Development Corp, will conduct Distributed Data Base Networks. Attendance will be limited; a separate registration fee of $30 for each seminar includes all course materials as well as access to all four days of the conference exhibit program.

Special Activities

The annual keynote address will be delivered Monday morning by Mark Shepherd, Jr, chairman and chief executive officer of Texas Instruments, Inc. A major theme will be the extension of distributed computing into applications that were not predictable when the computer revolution began some 25 years ago. Mr Shepherd will discuss many of the impacts, implications, and trends associated with present-day computing. On Tuesday at a special plenary session in the Convention Center, Dr Theodore J. Williams, professor of engineering and director of the Purdue Laboratory for Applied Industrial Control, Purdue University, will deliver the AFIPS Presidential Address. In his remarks, Dr Williams will review and assess the increasingly critical role of computers in industrial process monitoring and control. At Wednesday's plenary session, A. Douglas Murch, senior vice president of Prudential Insurance Co of America will speak on "Current Challenges of Data Processing in the Insurance Field."

Major contributions by members of the computing group of the Los Alamos Scientific Laboratory in New Mexico will be given special recognition during the Pioneer Day Program on Tuesday. Attention will be focused on three areas—computer hardware development and usage, software development, and contributions to pure and applied mathematics.

Other notable events will be the presentation of the Harry F. Goode Memorial Award, the annual Conference Reception to be held Monday evening, and a national programming contest designed to provide a test of logic and programming skills.

Exhibits

More than 1100 booths representing over 300 organizations will occupy the Dallas Convention Center to exhibit computer hardware, software, systems, and services—many to be shown for the first time. Attendees will have the opportunity firsthand to compare major offerings in all areas of the computing field, ranging from mainframes, minis, and microprocessors through memory systems, peripherals, and data communications equipment. Exhibit hours will be 11 am to 7 pm on Monday and 10 am to 6 pm on Tuesday, Wednesday, and Thursday. A review of many of the products to be exhibited at NCC will be given in the June issue of *Computer Design*.

Registration

Conference attendees who have not preregistered may register at the Convention Center. Fees are

Full Conference (4-day program, exhibits, and *Conference Proceedings*)	$75
Full Week Exhibits Only	$25
1-Day Program and Exhibits	$25
1-Day Exhibits Only	$10
Students (Full week of exhibits and program)	$10

Additional copies of the *Conference Proceedings* may be purchased at the Conference, or may be obtained after the conference by contacting the AFIPS Press. Price is $60 for nonmembers, $30 for members (of AFIPS constituent societies).

A complimentary shuttle bus service will be maintained between major hotels and the convention center. Travel information is available from the NCC Travel Service by calling (800) 556-6882; additional general information may be obtained by contacting AFIPS, 210 Summit Ave, Montvale, NJ 07645 or by calling (201) 391-9810.

Excerpts of the Technical Program cover only those sessions of particular interest to *Computer Design* readers. Information is necessarily limited to that available at press time.

TECHNICAL PROGRAM EXCERPTS

Monday Afternoon

Session 2 — 2:00-3:30 pm

Computer Systems Architecture

Chairman: Yih-Wu Han, Honeywell, Inc, Minneapolis, Minn

Some interesting observations about computer architecture and theory for computer system analysis and design, and fault tree analysis are presented in this session which also stresses the importance of fault tolerant capability and classification of fault tolerant schemes for computer systems.

"Whither Computer Architecture," John Earle, John Earle, Inc

"Using Fault Tree Analysis for Studying Computer Systems," C. V. Ramamoorthy, University of California at Berkeley and Yih-Wu Han, Honeywell, Inc

"An Overview of Fault Tolerant Digital System Architecture," Stephen Y. H. Su and Richard J. Spillman, Utah State University

Session 5 — 2:00-5:15 pm

Developments in Computer Output Microfilm (COM) and Micrographic Technology—Present and Future

Chairman: Don M. Avedon, National Micrographics Association, Silver Spring, Md

This session will include an up-to-date review of micrographic technology, computer input microfilm (CIM), and computer output microfilm (COM), as well as an indication of the market size and growth rate. Other items of interest that will be covered are indexing and retrieval of microforms; the use of COM and how to manage information; and COM systems.

"Micrographics and COM—A State-of-the-Art and Market Report," Don M. Avedon, National Micrographics Association

"Micrographic Fundamentals and Recording Techniques," George Harmon, Micord Corp

"Indexing and Retrieval Techniques and the Systems Approach to COM," Franklin I. Bolnick, Microfilm Sciences Corp

"COM Applications and Management of Information," Truett E. Airhart, Zytron Corp

Session 8 — 3:45-5:15 pm

Data Models and Their Applications

Chairman: Peter P. S. Chen, Massachusetts Institute of Technology, Cambridge, Mass

Data models are the basis for designing data base systems and for modeling the real world. Many models have been proposed. Examples are network, relational, and entity-relationship models. This session purposes to provide a better understanding of theoretical aspects and practical applications of data models.

"Why Restrict the Modeling Capability of CODASYL Data Structure Sets," Charles W. Bachman, Honeywell Information Systems

"The Entity-Relationship Model: A Basis for the Enterprise View of Data," Peter P. S. Chen, Massachusetts Institute of Technology

"Data Architecture and Data Model Considerations," Edger Sibley and Larry Kerschberg, University of Maryland

Session 9 — 3:45-5:15 pm

Toward the Computer of Tomorrow: A Multi-Faceted Challenge

Chairman: Lowell Amdahl, Northridge, Calif

Most disciplines in computer science tend to interact—technology advances open new application areas, new languages induce architectural changes. What significant advances can we expect to see in computers in the next five to ten years? How can we increase cooperation among the various disciplines in order to develop more effective computer systems? The panel, which consists of Charles Vick, Ballistic Missile Advanced Technology Center; Gordon Moore, Intel Corp; Albert Hoagland, IBM Corp; Gene Amdahl, Amdahl Corp; Herbert Grosch, Consultant; and Harlan Mills, IBM Corp, will address these questions from viewpoints of the user, hardware and software technology, and system architecture.

Tuesday Morning

Session 15 — 9:00 am-12:15 pm

Selection Methods for a Family of Computer Architectures

Chairman: Y. S. Wu, Naval Research Laboratory, Washington, DC

A joint Army/Navy committee was organized to select a proven computer architecture as the basis for a family of software compatible military computers. The six papers that make up this session provide an overview of the work of that committee and a detailed discussion of the technical method used to quantitatively evaluate the alternate computer architectures considered.

"Overview of the Military Computer Family Architecture Selection," William E. Burr and Aaron H. Coleman, U.S. Army Electronics Command, and William R. Smith, Naval Research Laboratory

"Initial Selection and Screening of the CFA Candidate Computer Architectures," Samuel H. Fuller, Carnegie-Mellon University; Harold S. Stone, University of Massachusetts; and William E. Burr, U. S. Army Electronics Command

"Evaluation of Computer Architectures via Test Programs," Samuel H. Fuller, Paul Shaman and David Lamb, Carnegie-Mellon University and William E. Burr, U. S. Army Electronics Command

"An Architectural Research Facility: ISP Descriptions, Simulation, Data Collection," Mario R. Barbacci and Daniel P. Siewiorek, Carnegie-Mellon University; Robert Gordon and Rosemary Howbrigg, Naval Underwater Systems Center; Susan Zukerman, Naval Research Laboratory

"Evaluation of the Software Bases of the Candidate Architectures for the Military Computer Family," James Wagner, Edward Lieblein, Jorge Rodriguez, U. S. Army Electronics Command and Harold Stone, University of Massachusetts

"Two Life Cycle Cost Models for Comparing Computer Architectures," William R. Smith, Naval Research Laboratory; William R. Svirsky, System Development Corp; Aaron H. Coleman, U.S. Army Electronics Command; and John J. Cornyn, Naval Ocean Research & Development Activity

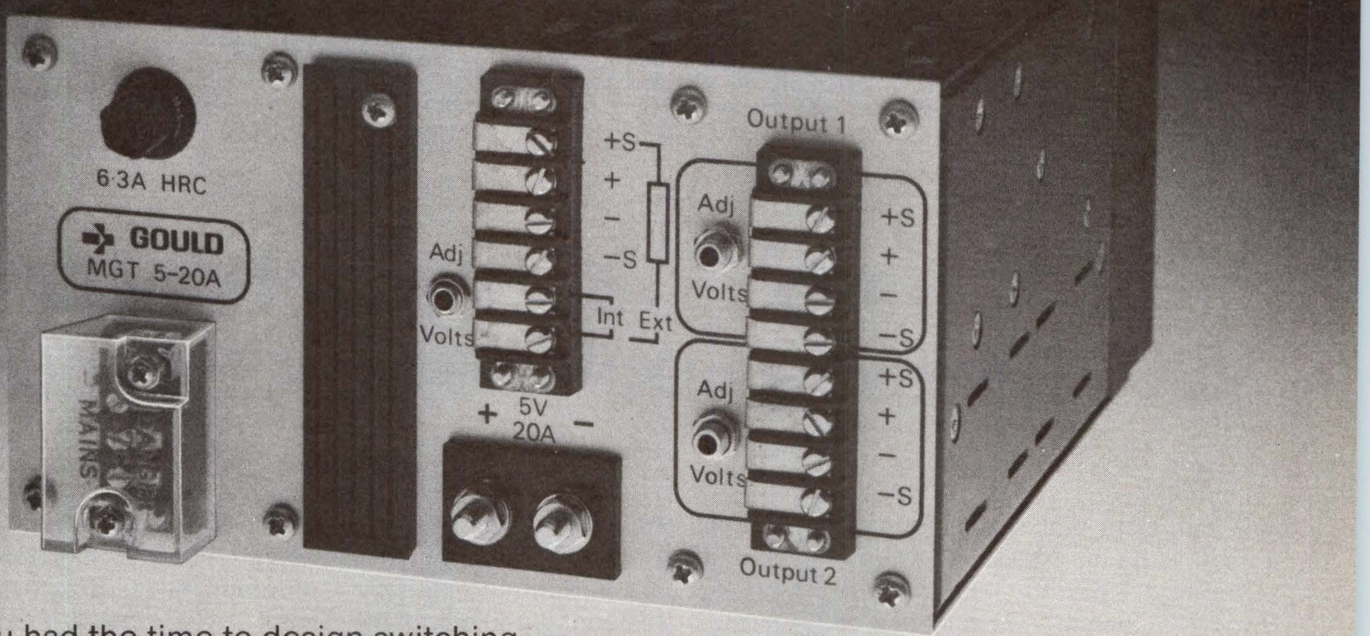
Session 16 — 9:00 am-12:15 pm

Microprocessor Architecture

Chairman: Charles R. Vick, Ballistic Missile Defense Advanced Technology Center, Huntsville, Ala

Addressing improvements in microprocessor hardware and software, presentation topics include novel ideas for programmable optical busing and design considerations for a series of flexible microprocessor modules. Application of microprocessors for realization of digital logic functions and intelligent hybrid interfaces

YOU'D THINK YOU DESIGNED IT YOURSELF.



If you had the time to design switching power supplies, we think your design, like ours, would reflect this basic design precept: achieve greatest efficiency in the least amount of space at a cost comparable to linear supplies.

That's one important reason why over the past four years more than 20,000 Gould units have quietly found their way into the designs of systems engineers all over the world.

Of course there are other important reasons:

- 36,000+ hours MTBF
- Switching at 33,000Hz
- 0.1% line/load regulation
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- full output rating at 50°C ambient
- standard remote sensing and programming

There are still more reasons, but we think you get the idea. Show a good design to a good design engineer and it'll speak for itself. So let us demonstrate to you the smallest and most efficient OEM power supplies yet designed.

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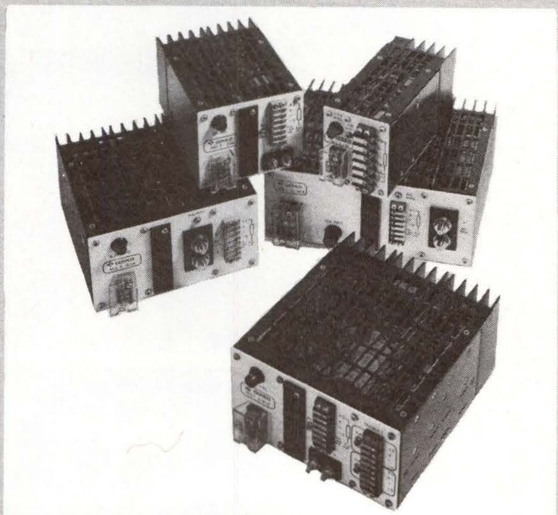

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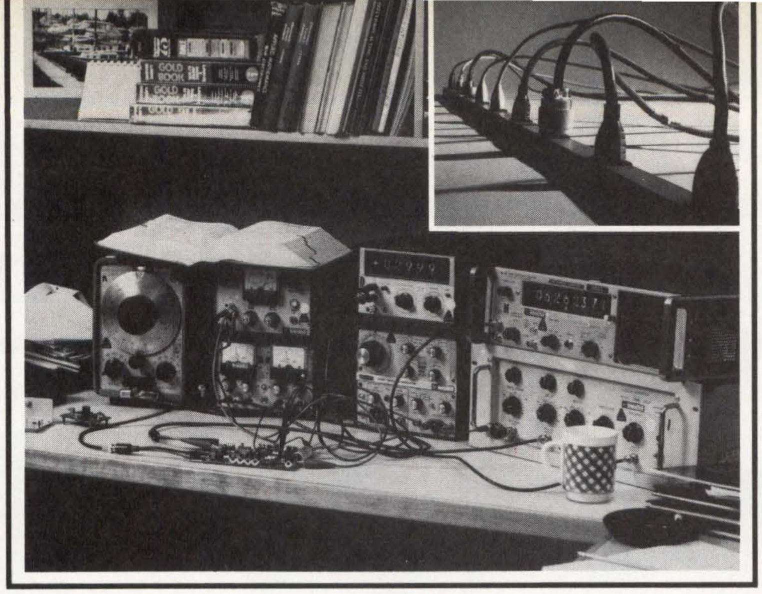
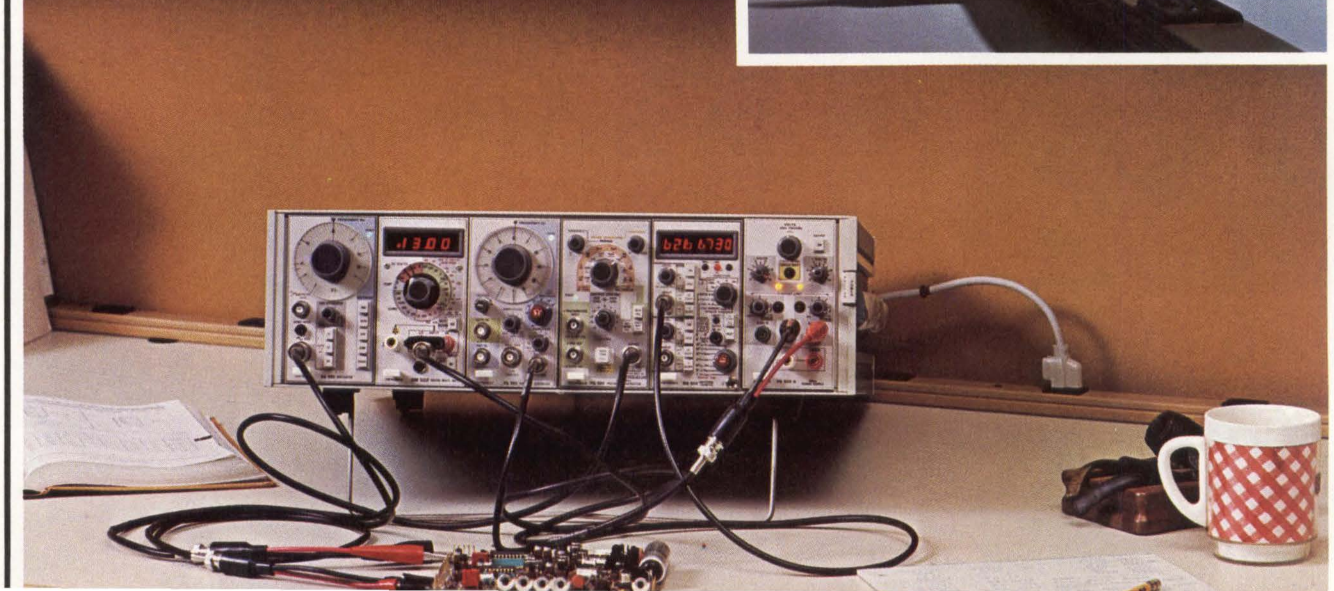
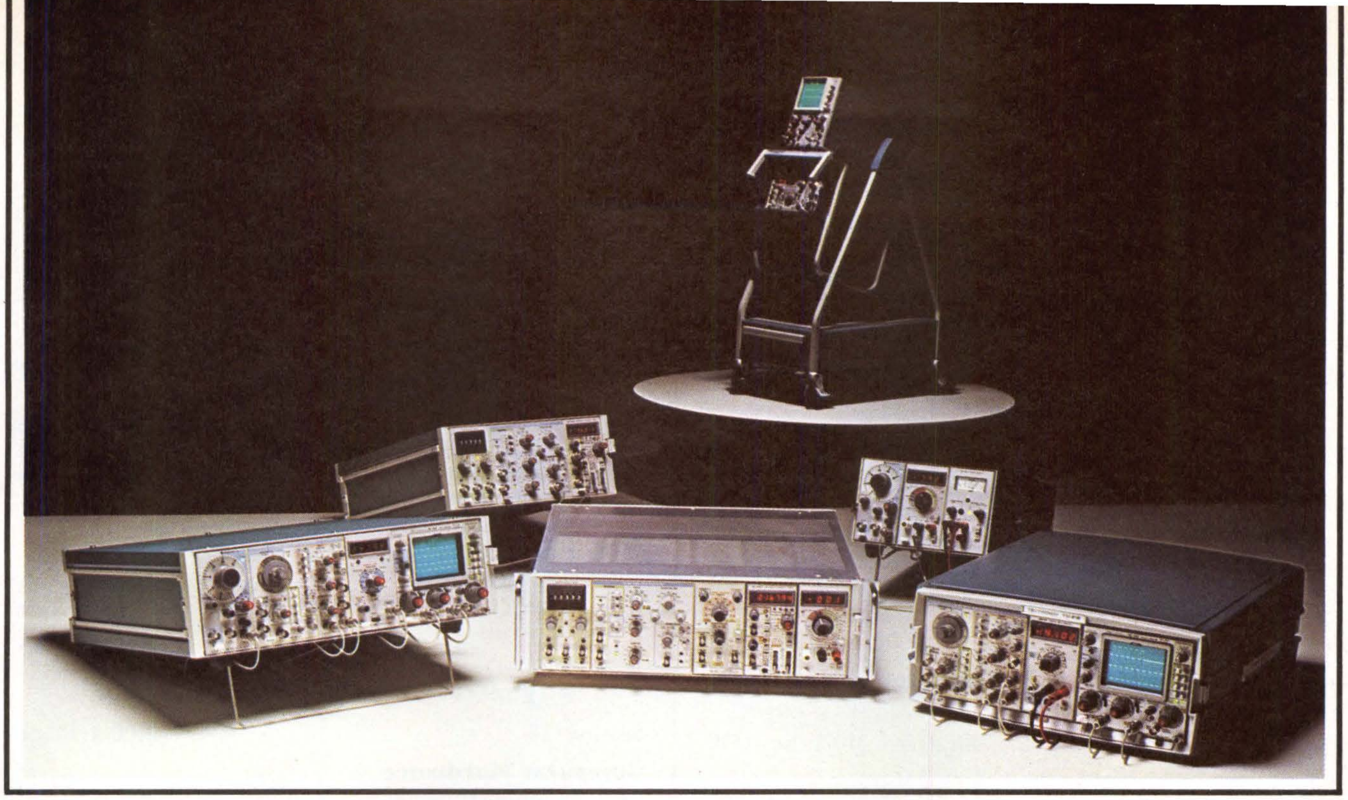


Here's an idea that could change your thinking about test equipment.

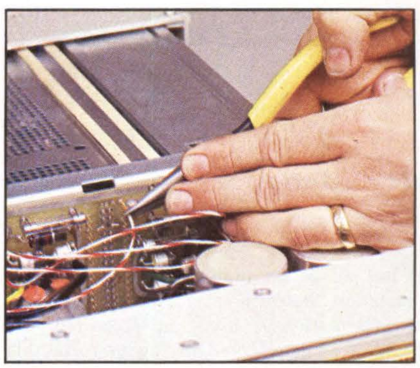
A complete test station doesn't have to be an assortment of special-function instruments. A working workbench doesn't have to be crowded and unhandy. And a truly portable test lab doesn't have to be out of reach.

TM 500 offers you an alternative: a modular line of compact, interchangeable plug-ins and mainframes. Multiconfigurable both in packaging and in performance, TEKTRONIX TM 500 is designed around the idea that test equipment which is compatible in every respect can, in fact, cover a broader range of functions and meet a wider variety of measurement situations. To say nothing of its ability to adapt more readily to new challenges.





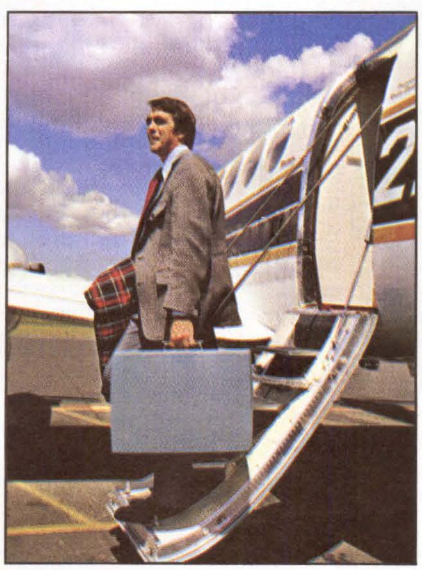
Modular DMMs, counters, generators, amplifiers, power supplies, oscilloscopes, logic analyzers, and word recognizers can be interfaced electrically. Signals



can be routed from one plug-in board to another via the mainframe mother board, thus enabling you to build a test instrument that's more powerful than the sum of its parts.

The plug-ins can be configured together in six widths of mainframe and four types of packages, depending on where and how you'll use them. Select the plug-in modules you need just as you would monolithic instruments, and then combine them in the appropriate mainframe for a convenient, uncluttered bench setup; mount up to 6 functions

side-by-side in a 5¼-inch rack; build a rollabout station that "follows" you around the lab. Or



pack a portable test station in the small-as-a-suitcase TM 515 Traveler Mainframe, which carries up to 5 modules and typically weighs less than 35 pounds, including the modules.

The result is a total test system that looks like a unit . . . works as a unit . . . yet is still configurable to new or changing measurement requirements. So the next time you're looking into test instrumentation, specify the one product line that's designed for configurability.

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For a demonstration, circle 52 on Inquiry Card.

are discussed. Software considerations are presented in a discussion of the design of a microprocessor operating system that allows applications software developed for a general-purpose system to be utilized.

"A Microprocessor Architecture for Digital Device Implementation," Thomas L. Boardman, Jr, University of Colorado

"A Hybrid Computer Interface for Microprocessors," Joseph P. Heid, General Electric, Space Division

"Multiprocessor Oriented Byte-Sliced LSI Processor Modules," M. Tokoro, Keio University, Yokohama, Japan

"An Organization for Optical Linkages Between Integrated Circuits," G. Jack Lipovski, University of Texas at Austin

"UNIX on a Microprocessor," H. Lycklama, Bell Laboratories

Session 17 — 9:00 am-12:15 pm

Software Management: Planning for a New Software Development Project

Chairman: Richard H. Thayer, U.S. Air Force, McClellan AFB, Calif

A key element in the successful completion of any software development project is proper planning. The advancing state-of-the-art in software engineering has given the software development project manager a wide variety of technologies and techniques for managing, developing, and designing a data system. Early identification of an appropriate and complementary set of software engineering and project management procedures, controls, and technologies is essential to good project planning. This session, which is directed to the project manager, identifies and compares many of these new procedures and technologies.

"Organizing and Training for a New Software Development Project—That First Big Step," Daniel Freedman, Donald C. Gause, and Gerald M. Weinberg, Ethnotech

"The Choice of New Software Development Methodologies for Software Development Projects," Edward Yourdon, Yourdon, Inc

"Software Development Tools Acquisition Considerations," Leon G. Stucki, Boeing Computer Services

"What Measurement Methods and Reporting Procedures Should Management Require?" Ray Caudill, Air Force Data Automation Agency

"Management of Large Scale Computer Program Production," H. S. Woodgate, International Computers Ltd, Reading, Berks, England

"Test Planning," R. Dean Hartwick, Logicon

Session 18 — 9:00-10:30 am

Systems Strategic Planning—A View From the Top

Chairman: Harvey L. Poppel, Booz, Allen & Hamilton, Inc, New York, NY

Speaker Harvey L. Poppel, Booz, Allen & Hamilton, will introduce a model for elevating information resource management (IRM) into the "board room" and tying into the strategic planning process of top management. As a backdrop, the practical potential of rapidly blending data, word, and communications processing technologies will be described. Then a four-phased methodology for planning, controlling, and organizing these emerging opportunities will be unveiled.

Session 20 — 9:00-10:30 am

Computer Systems In Health Care Delivery and Medical Laboratories

Chairman: William J. McClain, Oak Ridge National Laboratory, Oak Ridge, Tenn

Effective health care delivery and medical laboratory services are requiring increased dependence upon state-of-the-art digital computer systems. This session includes descriptions of a distributed computing network for data acquisition in a medical multilaboratory environment, a knowledge base for constructing diagnoses and treatment plans by symbolic models of patients and situations using inference rules derived from expert physicians, and an assessment of the impact of microprocessors on health care delivery.

"'NODAS': The Network-Oriented Data Acquisition Systems for the Medical Environment," Shelly I. Saffer, David J. Mishelevick, Shirley J. Fox, and Victor B. Summerour, University of Texas Health Center at Dallas

"A System for a Primary Clinical Knowledge Base," Randal L. Walsher and Bruce H. McCormick, University of Chicago

"The Assessment of the Impact of Microprocessors on Health Care Delivery," William M. Lively and William Hyman, Texas A & M University

Tuesday Afternoon

Session 28 — 2:00-3:30 pm

Computer Hardware

Chairman: William P. Summers, General Dynamics Corp, Fort Worth, Tex

Design oriented topics of general interest to be presented include a noise analysis approach for assessing the status of crosstalk in computer backpanels, advanced semiconductor technology in programmable calculators, and true liquid cooling of computers. The contents, although design oriented, will be of interest to all users as well as designers.

"NAA: An Approach to Analyzing Backpanel Crosstalk," J. S. Hebhardt, C. F. Groves, and R. Bardas, Sperry Rand

"Advanced Semiconductor Technology in Programmable Calculators," Syd Poland and K. Balasubramanian, Texas Instruments

"True Liquid Cooling of Computers," E. A. Wilson, Honeywell Information Systems

Session 29 — 2:00-3:30 pm

Output—Results and Rhetoric

Chairman: James O. Matous, General Dynamics Data Systems Services, Fort Worth, Tex

Data processing systems are no better than the means available to effect 2-way communication between users and computers. Independent of the way information is input or processed, the output must be provided in a form oriented to the user. In this session two methods of providing output from data processing systems are presented. First, by classifying processed information into calculated results and descriptors, a GO (Generate Output) system has been developed providing output which is user-oriented as well as easily maintained. The second method approaches output from a totally new direction, which resulted in a host independent talking computer terminal. The issue of output is addressed in a detailed look at the future of hardcopy output in the computer technology/environment of tomorrow.

"GO System: Design and Implementation of an Output Generator," Roland R. Bonato and Kenneth C. Yang, George Washington University

"A Talking Computer Terminal," James A. Kutsch, Jr, West Virginia University

"The Future of Computer Output to Hard Copy," Irving L. Wieselman, Data Products

Session 32 — 2:00-5:15 pm

Computing at Los Alamos in the 40's and 50's

Chairman: J. B. Harvill, Southern Methodist University, Dallas, Tex

(Information not available at press time.)


DATA CAPTURE
RECORD
MODE
MARKER
TEST
DATA PLAYBACK
REPLAY
SEARCH
BACKSPACE
TAPE POSITION
EPICOM

Session 34 2:00-5:15 pm

Unethical Conduct in Computer Science and Technology

Chairman: Donn B. Parker, Stanford Research Institute, Menlo Park, Calif

An AFIPS-sponsored workshop funded by the National Science Foundation and held at Stanford Research Institute will be described by a panel of computer, law, and philosophy experts. Discussed will be such questions: Were the actors unethical or not? When does a program belong to a programmer and when to the employer? Should unused cycles of an idling computer be used for fun and games? How should a systems analyst feel about developing a system that displaces people out of their jobs? Members of the panel are: Harold Borko, University of California at Los Angeles; Judith Edwards, Northwest Regional Educational Laboratory; Albert Flores, Renssalaer Polytechnic Institute; Bernard A. Galler, University of Michigan; Fred H. Harris, University of Chicago; William J. Horne, Boston College; John McLeod, Society for Computer Simulation; Roger L. Mills, TRW Defense Systems; Susan H. Nycum, Chickering & Gregory; and Richard Waller, Computer Analysts and Programmers, London, England.

Session 35 3:45-5:15 pm

Data Base Design Methodology

Chairman: Philip Y. Chang, University of Texas, Austin

The data base design process is generally recognized as the most important factor in the performance and growth of a data base system. However, there is no widely accepted design methodology despite the researchers' efforts in this area. Panel members Charles W. Bachman, Honeywell Information Systems; Barbara M. Fossum, Sperry Univac; Vincent Y. Lum, IBM Corp; Richard Peebles, University of Waterloo, Ontario, Canada; and Raymond T. Yeh, University of Texas at Austin are currently involved in data base design research and practice and will survey the field and discuss the questions of what are the missing links and how to develop a design methodology.

Session 36 3:45-5:15 pm

Government Panel on Research In Computer Architecture

Chairman: Jimmie R. Suttle, U.S. Army Research Office, Research Triangle Park, NC

During the past few years, rapid advances in solid state devices have had a significant impact on computer architecture. More attention has been devoted to design of processors and computing systems for specific applications such as signal processing, control, and pattern recognition. There is special interest in hardware-software tradeoffs where special purpose microprocessors or other imbedded computers are used as part of a complex system. This panel will discuss the current state of research activity in the above and related fields and will attempt to identify areas of research in computer architecture which are likely to have impact in the future. Members of the panel, John Lehmann, National Science Foundation; George W. McKemie, Air Force Office of Scientific Research; Alan B. Salisbury, U. S. Army Electronics Command; David Carlstrom, Advanced Research Projects Agency; and Joel Trimble, Office of Naval Research represent a broad cross-section of government agencies which are either involved in computer architecture research or sponsor research in architecture. Research areas of interest to the respective agencies will be described.

Session 38 3:45-5:15 pm

Mini and Micro Design Mistakes

Chairman: Helmut E. Thiess, Navy Regional Data Automation Center, Washington, DC

It is a fair assumption that mistakes were made when first- and second-generation microcomputers were sold and used. Hardware architecture changed, system software was nonexistent or cumbersome, or an overwhelmingly predominant vendor emerged.

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National Semiconductor is going into the microcomputer business.

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10% off the Intel 80/10.

To get 10% off Intel's 80/10, don't buy Intel's 80/10. Buy National's 80/10.

We're able to sell the 80/10 for less because of our improved board layout which permits automated assembly (such as using axial leaded components)...the fact that we make not only the 8080, but also—unlike Intel—most of the rest of the ICs on the board...and, of course, National's legendary competence in efficient manufacturing doesn't hurt either.

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Our second-sourcing of the 80/10 clears the way for the 80/10 to be the clear-cut standard of the microcomputer industry.

You can't effectively have an industry-standard without a second-source. Having two suppliers is a healthier competitive situation for you, the customer, and you have the security —and abuse-protection—of an alternate source.

Purpose of this panel, consisting of Helmut E. Thiess, Navy Regional Data Automation Center; John H. Carson, RLG Associates; and James A. Painter, ADP Directorate, is to provide a forum for the discussion of mistakes in the design, software, maintenance, and use of mini- and microcomputers—mistakes that could have been avoided by a decent respect for history.

Wednesday Morning

Session 42 — 9:00 am-12:15 pm

Architecture for Pattern Recognition Applications

Chairman: Tadao Ichikawa, Kokusai Denshin Denwa Co, Ltd, Tokyo, Japan

In most applications of pattern recognition, because of the extremely large volume of data involved, some specialized processors, designed to speed up processing with a high degree of sophistication are now replacing general-purpose computers. Thus, it is important to hold discussions on the interactive problems between computer architecture and pattern recognition. Caxton C. Foster, University of Massachusetts; King Sun Fu, Purdue University; Gale R. Allen, Control Data; D. Raj Reddy, Carnegie-Mellon University; Jack Sklansky, University of California at Irvine; and Michel J. Castelberg, Seiscom Delta, attempt through discussions to discover what form computer architecture should take for pattern recognition applications.

Session 43 — 9:00-10:30 am

Applications of Computer Networks

Chairman: Susan Poh, Mitre Corp, McLean, Va

Computer networks motivate new computer applications and services. Presentations focus on a resource sharing service based on time prediction to assist users in selecting the best resources available, and on a structured data base computer conferencing system which facilitates communications to groups of people.

"Response Time Prediction As A Network Resource Sharing Service," Sandra A. Manrak, Ohio State University and National Bureau of Standards

"Structured Data Base Computer Conferencing System," George W. Arnold, Bell Labs and Stephen H. Unger, Columbia University

Session 44 — 9:00-10:30 am

Computer Systems: A Global View

Chairman: Roger M. Firestone, Sperry Univac, St Paul, Minn

This session will view computer systems as complete functioning entities. Theoretical issues of correctness in multiprocessing systems driven by user requests; economic variables in relation to a system model encompassing hardware architecture and software problem structure; and social interactions in the computing systems are considered with emphasis on the significance that the influence of the real world on the computer system has in the model.

"Correctness in Asynchronous Operating Systems," Abraham Silberschatz, University of Texas

"An Analytic Model For Parallel Computation," Roger M. Firestone, Sperry Univac

"Dominance Relations in Computing Systems," Daniel G. Hays, University of Alabama

Session 47 — 9:00-10:30 am

Continuing Education for the Computer Specialist

Chairman: Ben Knowles

(Information not available at press time.)

Now Norden gives DIGITAL's PDP-11/34 all the muscle it needs to work in any military environment.

New PDP-11/34M uses exactly the same software as commercial PDP-11/34.

First in a new family of militarized computers, the PDP-11/34M combines Norden's experience in military electronics with DIGITAL architecture and DIGITAL software.

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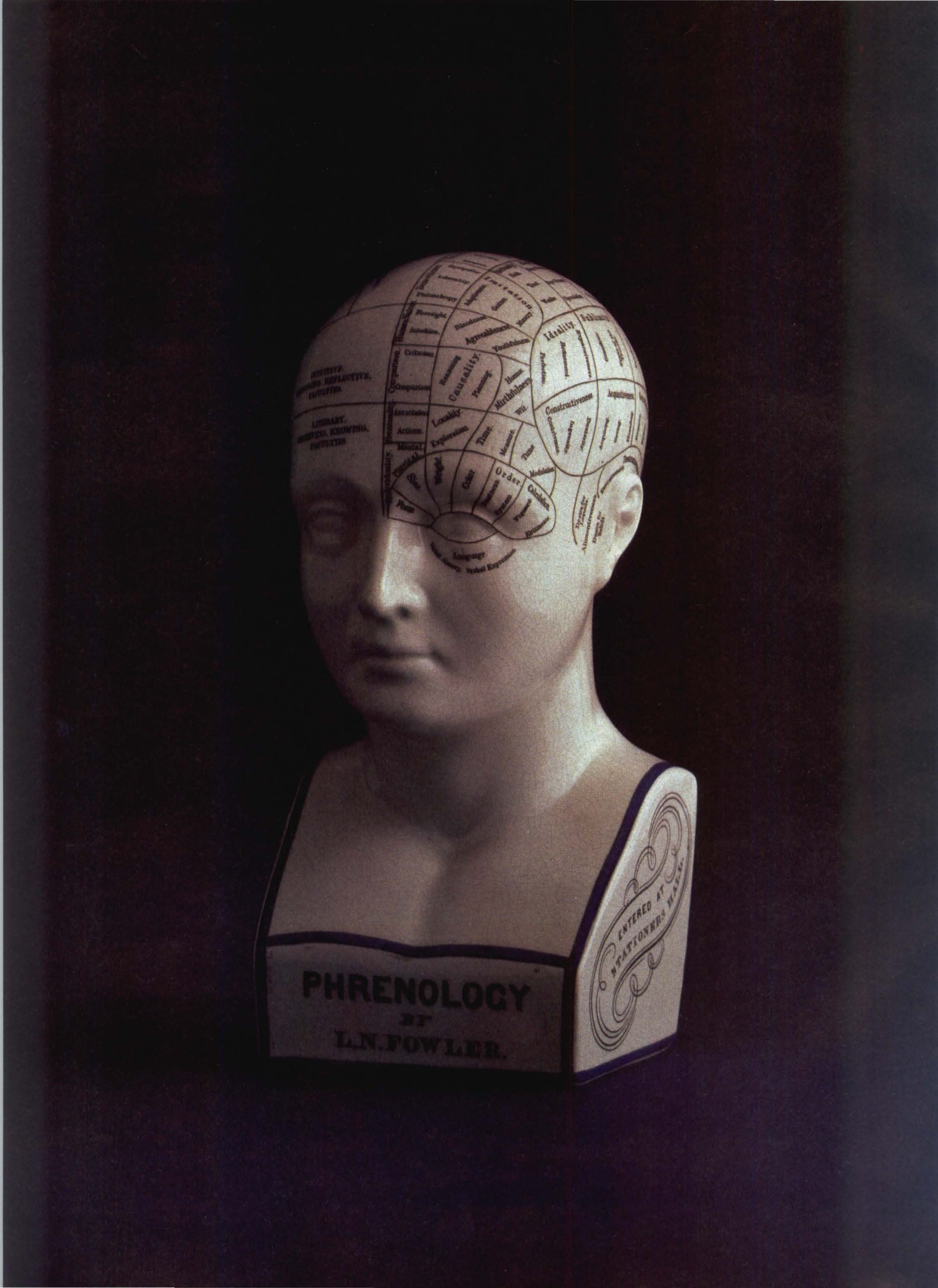
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BY
L.N. FOWLER.
ENTERED AT STATIONERS HALL.

Session 48 9:00 am-12:15 pm

Personal Computing: History and Foreseeable Future

Chairman: Jim C. Warren, *Dr Dobb's Journal of Calisthenics & Orthodontia*, Menlo, Calif

Session is divided into sections that will deal with hardware, software, and applications. The first section is intended to bring computer professionals up to date. A panel presentation of the past, present, and future of home computing will follow formal presentations.

"Personal Computing: An Overview for Computer Professionals," Jim C. Warren, *Dr Dobb's Journal of Calisthenics & Orthodontia*

"Future of Hobby Computers," Leslie Solomon, *Popular Electronics*

"Personal Computing: Who's Doing It Now and What For?" Carl Helmers, *Byte*

"The Impact of Home Computing Systems on Education and Learning Environments," Ludwig Braun, State University of New York at Stoneybrook

"Text Editing and Music Applications of Home Computers," Hal Chamberlin, Hendrix Electronics

"The Computer as a Social Commodity: Community Memory," Lee Felsenstein, LGC Engineering

"Design of a Transcendental Literary Network," Theodor H. Nelson, Swarthmore College

Session 50 10:45 am-12:15 pm

Data Communication Policy and Its Impact on the Consumer

Chairman: Robert R. Korfhage, Southern Methodist University, Dallas, Tex

(Information not available at press time.)

Session 51 10:45 am-12:15 pm

Software Validation

Chairman: Edward V. Resta, E-Systems, Dallas, Tex

(Information not available at press time.)

Session 52 10:45 am-12:15 pm

Why Managers Fail

Chairman: James F. Towsen, The Statesman Group, Harrisburg, Pa

It has been said that many managers and supervisors are not regarded as assets to the organization by their peers and/or subordinates. Since they are not capable of proper management, it is important to discuss the pitfalls that need to be avoided. Speaker James F. Towsen, The Statesman Group, examines the topic of the managers who can't communicate and who can't manage time.

Session 53 10:45 am-12:15 pm

Computer Technology Forecast Through 1985

Chairman: Robert White

(Information not available at press time.)

Wednesday Afternoon

Session 56 2:00-3:30 pm

Distributed Fault-Tolerant Microprocessor Systems

Chairman: Stephen S. Yau, Northwestern University, Evanston, Ill

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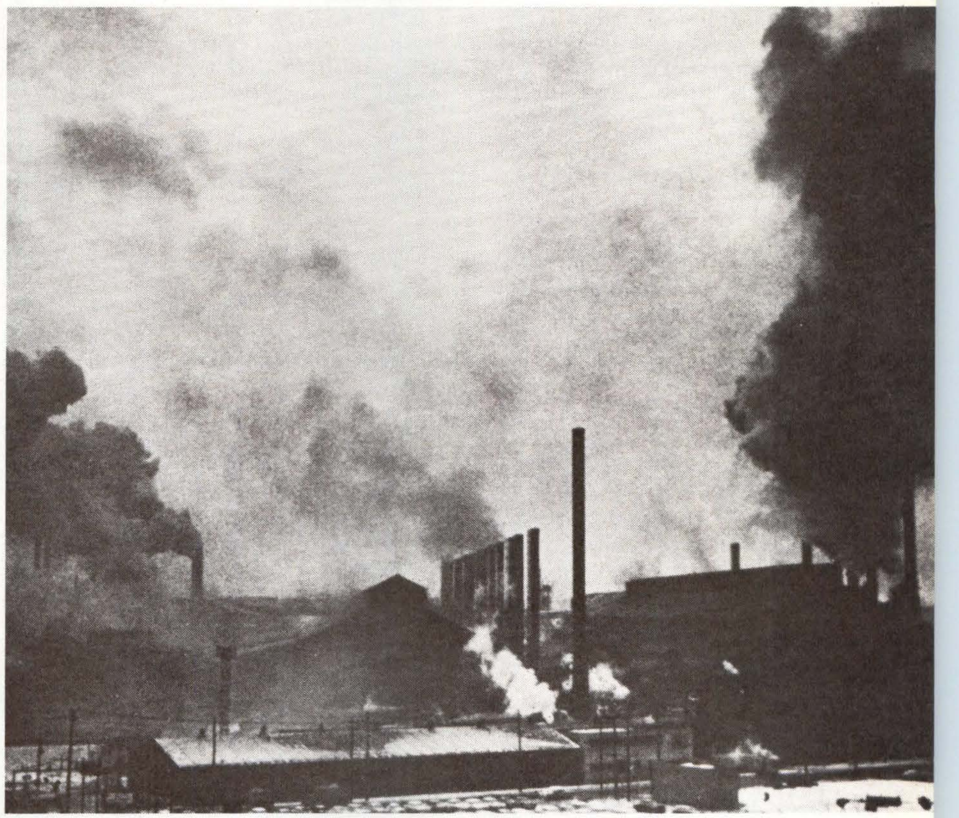
THE ONLY DISK DRIVES THAT DON'T NEED CLEAN AIR TO BREATHE.



Each Trident disk drive has its own enclosed air filtration system. No other removable-pack disk drives do.

This means you can use a Trident just about anywhere. In a warehouse. Or a factory. Even in a smoke-filled room.

This kind of flexibility is just one reason Trident is the choice of growing businesses everywhere.

You find Tridents on the job in department stores—taking care of inventory control right at the point of sale.

Tridents are at the heart of the reservations systems for major hotel chains.

And Tridents are the continuing choice of the nation's leading OEMs.

There are five Trident models. So you have a wide range of capacities to choose from—all the way from 27 to 312 megabytes.

Each Trident model is functionally compatible with every other Trident model. Each gives you track-following servo-technology. And each gives you one of the lowest cost-per-byte ratios in the industry.

TRIDENT FORMATTER

Our 1150A Formatter is very versatile too. It offers the designer of micro/minicomputer systems important features that up to now were available only in large disk controller subsystems—such as ECC, RPS, and overlapped seek.

It can control and format any mix up to eight Trident drives—for a total storage capacity of up to 2.4 billion bytes of on-line data. And it can be attached to virtually any micro/minicomputer by means of a universal CPU interface.

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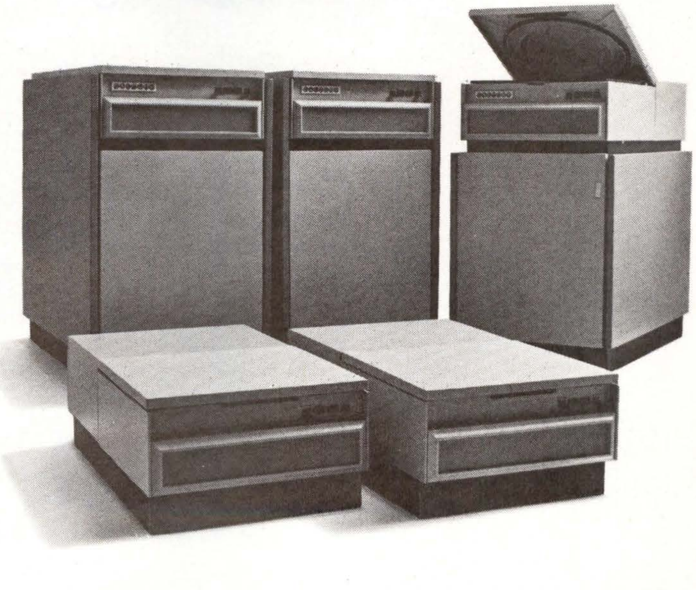


Rapid development of LSI technology and microprocessors has great potential to make fault-tolerant computing systems using the distributed processor systems concept economically feasible. Emphasizing the relationship among distributed processor systems, microprocessors, and fault-tolerant computing systems, the potential advantages and capabilities as well as difficulties in both hardware and software developments for such computing systems using these concepts will be discussed by T. Y. Feng, Wayne State University; William J. Dejka, Naval Electronics Center; Jack Goldberg, Stanford Research Institute; Albert L. Hopkins, Jr, Charles Stark Draper Laboratory; and C. V. Ramamoorthy, University of California at Berkeley.

Session 57 **2:00-3:30 pm**

Packet-Switched Networks

Chairman: Saroj Kar, TCT International, Sunnyvale, Calif

(Information not available at press time.)

Session 58 **2:00-3:30 pm**

Programming Languages: High-Level Programming for Low-Level Machines

Chairman: Dennis J. Frailey, Southern Methodist University, Dallas, Tex

One of the most interesting struggles of the past few years has been the conflict between the emergence of smaller computing devices, with few resources and minimal software, and the increased use of higher-level programming languages, which require strong support in hardware and software. Out of this struggle have come exciting developments in language and complier design which are discussed here.

"Modular Programming Conventions in Assembly Language," Shy-Ming Ju, University of North Carolina at Charlotte

"A BASIC Cross-Compiler for Programmable Calculators," Deane Blazie, Maryland Computer Services

"The Design and Implementation of a Simple Programming Language for Microcomputers," J. C. Cleaveland and C. D. Satten, University of California at Los Angeles

Session 62 **2:00-5:15 pm**

Products of the Retail Computer Market

Chairman: Adam Osborne, Osborne & Associates, Inc, Berkeley, Calif

Covering the computer hobby market from its inception, through its current status, to its probable future, speakers will present an overview of the market and its products. Particular emphasis will be given to identifying the type of individual who is a "computer hobbyist." Detailed analysis of the computer hobby market will come from manufacturing, retailing, and user viewpoints; the future will be considered in a discussion of the entry of established and prestigious manufacturers into home computing.

"The Computer Hobby Market—A Product Overview," Adam Osborne, Osborne & Associates

"The Microcomputer Manufacturer and His Product Line," Mike Stone, IMS Associates

"The Impact of the Retail Outlet on Future Microcomputer Products," Paul Terrill, Byte Shops

"Peripherals in the Computer Hobby Market," Eric Dunstan, Micropolis

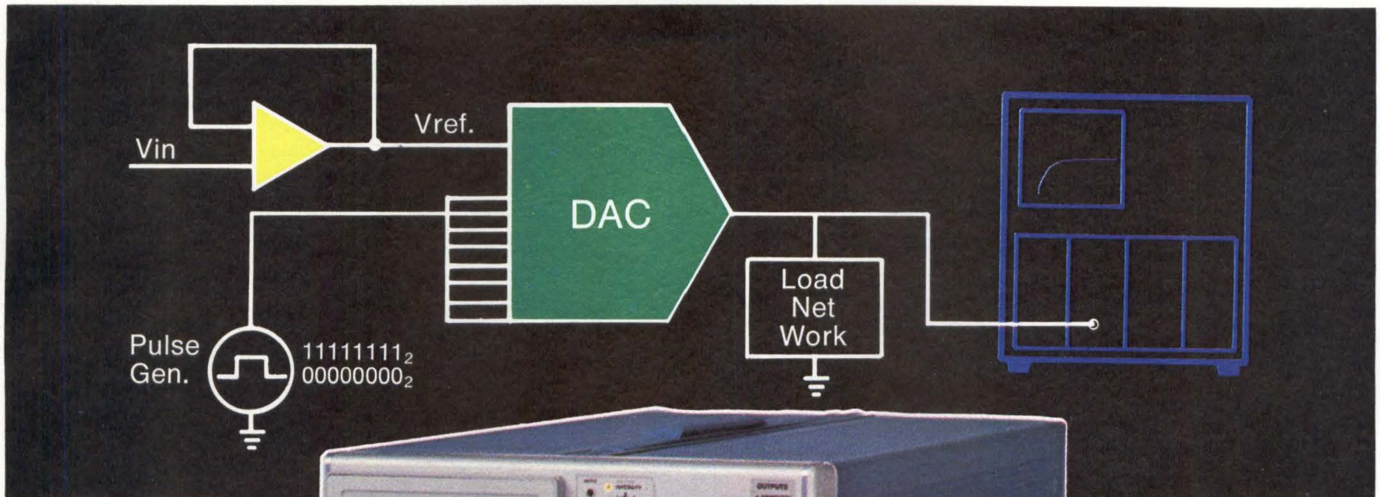
"The Impact of Established Companies Entering the Computer Hobby Market," Lou Frenzel, Heath Co

Session 64 **3:45-5:15 pm**

Cm*: A Multi-Microprocessor Computer System

Chairman: Samuel H. Fuller, Carnegie-Mellon University, Pittsburgh, Pa

For Your D/A Converter Analysis,



Use this dual-trace scope to make easy, accurate D/A converter settling time and amplitude measurements . . . and to analyze and verify the performance characteristics of other high-speed components.

Configured in a 7904 mainframe*, the 7S14 Sampling plug-in lets you examine settling time anomalies as narrow as 500 ps, to vertical sensitivities down to 2 mV/div. The internal delaying time base lets you select the whole waveform, or any portion, for observation.

The 7D12/M2 Strobing Voltmeter and 7B92A Dual Time Base plug-ins help you easily measure the overall amplitude of the device output, and the P6201 Active Probe conveniently captures the DAC's output with minimum circuit loading.

pick this plug-in scope

Get Reliable, Repeatable Settling Time Measurements

No significant distortions will be introduced into your settling time measurement because the 7S14 Sampler minimizes the scope's vertical amplifier recovery time effect. The high-impedance probe minimizes loading the circuit under test.

With high vertical sensitivities, small perturbations can be measured to less than 1 least significant bit depending upon circuit loading.

The result is accurate measurements time after time.

Put Together a Complete System

You can measure overall output amplitude to within 0.25% with the strobing voltmeter and dual time base plug-ins included in the plug-in scope system. And it couldn't be easier: the intensified zone generated by the time base points out which part of the waveform you're measuring and the amplitude is read out digitally on the crt.

Extend Your System's Sampling Performance

This sampler allows you to display time windows as narrow as 500 ps at sweep speeds to 100 ps/div. Choose from 4 other sampling plug-ins and 10 sampling heads for time window measurements ranging from 25 ps to 1 ns. All these sampling plug-ins, including the 7S14, will operate in any 7000 Series Mainframe. All will significantly minimize the recovery time limitations you might encounter with amplifiers in a real-time scope. And some sampling plug-ins include TDR capability.

Expand Your System to Include Real-Time Performance

By adding a 7A24 Dual Channel Amplifier plug-in, you'll have a real-time system with two channels of 350-MHz performance and sweep speeds as fast as 500 ps/div. Or you can also choose from other amplifier plug-ins that will give the full mainframe bandwidth of 500 MHz.

Your oscilloscope needs may change as the speed of system components continues to increase. So whatever your choice may be, a Tektronix plug-in scope can give you unmatched value now and in the future.

To order the plug-in system described here or to receive selection assistance, call your local Tektronix field office.* For a full product demonstration, clip the logo from this ad to your letterhead and send it to us at Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077. We'll have a Field Engineer contact you. **Or circle the bingo number, and we'll send you a copy of our application note, "D/A Converter Measurements: A Sampling Oscilloscope's Approach."**

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7904 Oscilloscope	$4,500.
7S14 Sampler	$2,650.
7D12/M2 Strobing Voltmeter	$1,550.
7B92A Dual Time Base	$1,795.
P6201 Active Probe	$ 680.

U.S. sales prices FOB Beaverton, OR.

*Storage Mainframes are often preferable when the signal repetition rate is below 100 KHz.

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Architecture of a multiprocessor computer system that supports a large number of processors (on the order of 100) will be discussed. The system enables close cooperation between large numbers of inexpensive processors, which share access to a single virtual memory address space. There are no arbitrary limits on the number of processors, memory, or communication bandwidth in the system. Considerable support is provided for low-level operating system primitives and inter-process communications.

"Cm*: A Modular, Multi-Microprocessor," R. J. Swan, S. H. Fuller, and D. P. Siewiorek, Carnegie-Mellon University

"The Implementation of the Cm* Multi-Processor," R. J. Swan, A. Bechtolsheim, Kwok-Woon Lai, and J. K. Ousterhout, Carnegie-Mellon University

"Software Management of Cm*, A Distributed Multiprocessor," A. K. Jones, R. J. Chansler, I. Durham, P. Feiler, and K. Schwans, Carnegie-Mellon University

Session 65 3:45-5:15 pm

International Data Communications—A Management Perspective

Chairman: Noel Zakin, AT&T, Morristown, NJ

The field of data communications has grown within the past few years, with the broadening of techniques and services. This interactive session will envision from a management point of view the differences, problems, pitfalls, considerations, opportunities, expansion, and progress of data communications both domestically and internationally, with concern for a multinational environment. Five panelists consisting of users, consultants, and educators discuss the various directions of data communications.

Session 66 3:45-5:15 pm

Programming Language: Theory

Chairman: Nancy Betz, Oak Ridge National Laboratories, Oak Ridge, Tenn

Three areas of research into programming languages under discussion are time and space optimization of target code, an empirical approach to natural language analysis by machine analysis, and a language for use by management, business, or accounting specialists who do not have computer training. Progress obtained in implementation of theories as well as views on future applications and benefits are considered.

"Using Assertion to Improve Language Translators," Dr Arthur Pyster, University of California at Santa Barbara

"A Parser-Analyzer of Empirical Design for Question-Answering," Dr Abraham Ben David, Xerox

"Automatic Generation of Computer Programs," Noah S. Prywes, Moore School of Engineering, University of Pennsylvania

Session 67 3:45-5:15 pm

Database Design for Decision Support Systems

Chairman: Howard L. Morgan, University of Pennsylvania, Wharton School, Philadelphia, Pa

Decision support systems are increasing in popularity and sophistication. One big element in most of these systems is access to larger data bases. Special features required of a DBMS by the DSS will be discussed by the panelists, William D. Haseman, Carnegie-Mellon University; George Dodd, GM Research Lab, Computer Technology Dept; and Earl Sacerdoti, Stanford Research Institute, who have had experience in implementing or using DSS on DBMS.

Session 68 3:45-5:15 pm

Computers in the Petroleum Industry

Chairman: Olin G. Johnson, University of Houston, Houston, Tex

Each of the four panelists, N. S. Neidell, GeoQuest International Ltd; Donald W. Peaceman, Exxon Production Research; Ross Short, Bonner and Moore Associates; and Toney J. Morelock,

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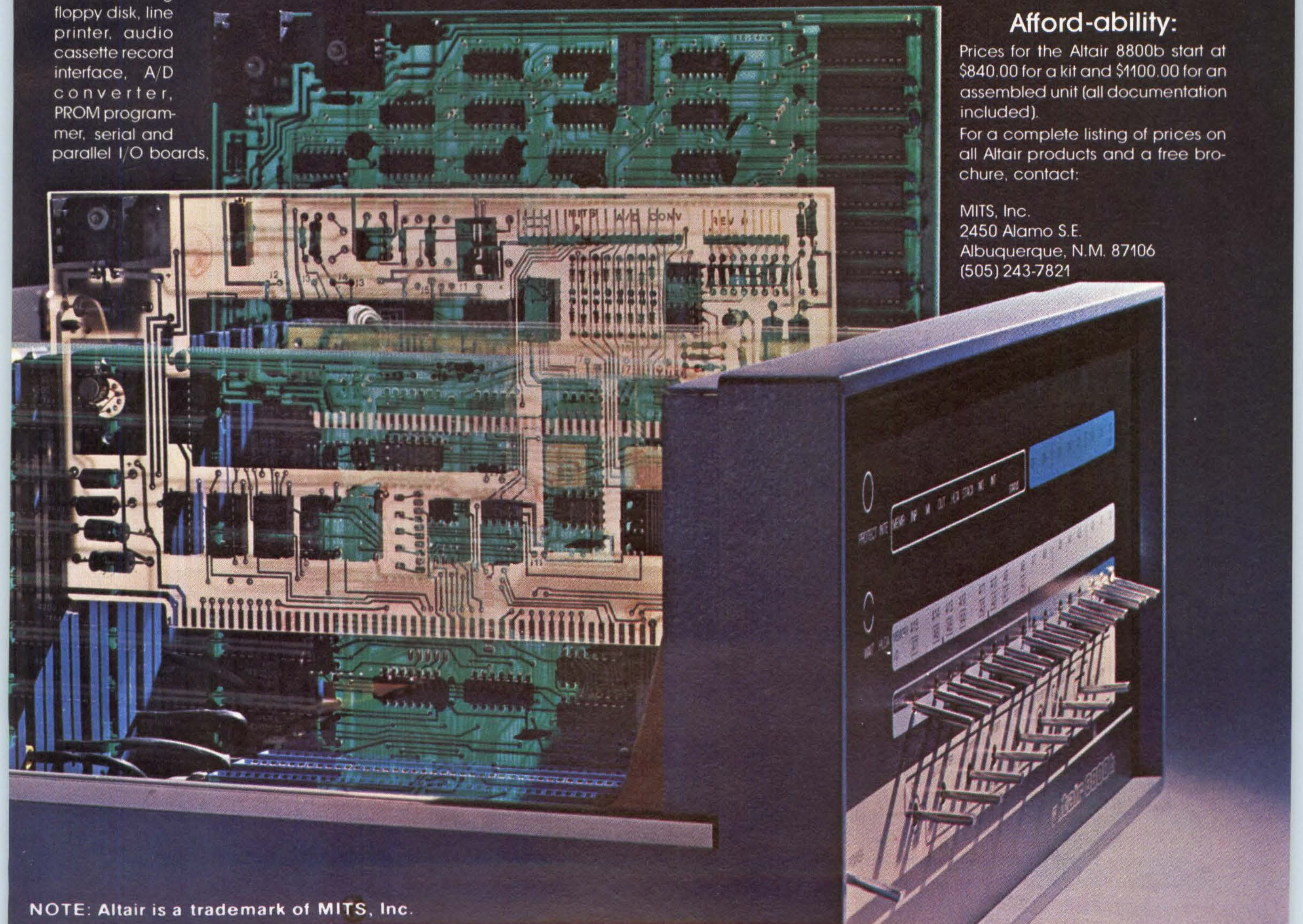

Texas Eastern Transmission has extensive experience in the application of computers in petroleum. Each is an expert in one of the following general areas: exploration, production, refinement, and transmission. The talks will be a mixture of survey and technical discussions.

Thursday Morning

Session 70 — 9:00-10:30 am

Fault-Tolerant Computing—I

Chairman: Francis P. Mathur, Wayne State University, Detroit, Mich

Fault-tolerance as a characteristic of a computing system is that which enables the system to execute all design specified tasks even in the presence of hardware or software failures. Fault-tolerance as a discipline covers a wide area of specialities such as architecture, redundancy structures, fault-diagnosis, error-codes, and software testing and validation. This session presents recent research results in the areas of self-checking, fault-diagnosis, and modular design.

"A Fault-Tolerant Modularized Arithmetic Logic Unit," T. R. N. Rao, Southern Methodist University, and H. J. Reinheimer, IBM Corp

"The Design of Self-Checking Multi-Output Combinational Circuits," D. C. Ko, Burroughs

"Improved Test Generation Algorithm for Combinational Circuit Control," A. N. Airpetian, Polytechnic Institute of Yerevan, Armenia, U.S.S.R. and J. F. McDonald, Rensselaer Polytechnic Institute

Session 71 — 9:00-10:30 am

Remote Terminal Emulation

Chairman: Marshall D. Abrams, National Bureau of Standards, Washington, DC

Remote terminal emulation is a computer measurement and evaluation technique whereby the teleprocessing workload imposed on a computer system is emulated by another computer. This is a relatively recent development applicable to benchmarking and tuning. Beginning with a tutorial survey, the discussion will move to reports from user and vendor viewpoints, and conclude with a panel contemplating the state-of-the-art.

"Remote Terminal Emulation in the Procurement of Teleprocessing Systems," Shirley Ward Watkins and Marshall D. Abrams, National Bureau of Standards

"Application of Remote Terminal Emulation in the Procurement Process," Jerry McFaul, U.S. Geological Survey

"Remote Terminal Emulator Development and Application Criteria," Couley T. Arthur, Honeywell Information Systems

Session 75 — 9:00-10:30 am

Optical Character Recognition—The Impact of a Maturing Technology on Future User Applications

Chairman: Herbert F. Schantz, II, Optical Character Recognition User Association, Hackensack, NJ

In the past 15 years, successful OCR manufacturers have developed significant strengths in a number of key technologies relevant to data. From these technologies, major product families (data entry systems) have evolved which are addressing and solving users' current needs in specific markets. This presentation will cover these applications and explain how mature technologies will continue to respond to the important and costly user data processing requirement of data entry.

"Optical Character Recognition—The Impact of a Maturing Technology on Future User Applications," Herbert F. Schantz, II, Optical Character Recognition User Assoc

Session 76 — 9:00 am-12:15 pm

Personal Computing Software

Chairman: William H. Gates, Microsoft, Albuquerque, NM

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software. In fact, the usefulness of these systems is limited more by the lack of software than by hardware constraints. The importance of software and the demand for it will continue to increase. The type of software needed and the difficulties of distributing it have created many unsolved problems. Current state-of-the-art and projections, hopes, and ideas for the future will be discussed by panel speakers who include Dennis Allison, Stanford University; Dick Whipple, Binary System Corp; Gary Kildall, Digital Research; Robert Uiterwyk, Microcomputer Systems; and Neal Colvin, Technical Design Laboratories.

Session 78 **10:45 am-12:15 pm**

Fault-Tolerant Computing II

Chairman: T. R. N. Rao, Southern Methodist University, Dallas, Tex

Design considerations for fault-tolerant systems, include the topics of design of a diagnosable fault-tolerant input/output controller; the modular redundancy without the use of voters, including a discussion on the complexity and effectiveness of the restoring organ; and a study and analysis of intermittent faults in digital systems.

"Design of a Diagnosable and Fault-Tolerant Input/Output Controller," A. K. Bose and S. A. Szygenga, University of Texas

"Modular Redundancy Without Voters Decreases the Complexity of Restoring Organ," P. T. DeSousa, Rockwell International and F. P. Mathur, Wayne State University

"A Study of Intermittent Faults in Digital Computers," Omur Tasar and Vehbi Tasar, University of Detroit

Session 79 **10:45 am-12:15 pm**

Performance Evaluation

Chairman: Anita Cochran, Bell Laboratories, Murray Hill, NJ

Simulation study papers discuss validation techniques for prediction of increases in performance that will result from modifications to the system; and possibilities of eliminating I/O bottlenecks and associated economies to be attained through the use of CCDs for data storage. A question and answer session will follow formal presentations.

"A 'Calibration-Prediction' Technique for Estimating Computer Performance," C. A. Rose, Naval Electronics Laboratory Center

"CPU-Utilization and Secondary-Storage Performances—The Demand for a New Secondary-Storage Technology," Peter Schneider, Siemens AG, Munich, Germany

Session 80 **10:45 am-12:15 pm**

Discrete Mathematical Models

Chairman: Ranan B. Banerji, Temple University, Philadelphia, Pa

The nature of applied mathematics has changed drastically with the advent of digital control, communication, and computation devices. Because of this, past theoretical results are now being widely applied. This change has affected research in the psychological and biological sciences; paradigms are changing, whenever appropriate, from the physical to the computational sciences. Speakers discuss discrete mathematical models in microbiology, artificial intelligence, and data transmission.

"Non-Linear Parameter Estimation for Probabilistic Finite State Automata," Fred J. Maryanski and Kuong Chan Wu, Kansas State University

"A Comparison Between Two Paradigms of Information Systems—An Example," Abraham Waksman, Temple University

"Concatenated Group Theoretic Codes for Binary Asymmetric Channels," Serban D. Constantin and T. R. N. Rao, Southern Methodist University

Session 82 **10:45 am-12:15 pm**

Industrial Applications of Computer Systems

(Information not available at press time.)

Thursday Afternoon

Session 84 — 2:00-3:30 pm

Computer Architecture Design

Chairman: James E. Brown, U.S. Army Missile Research and Development Command, Somerville, Ala

Consisting of both presentations and a panel discussion, session will deal with external processes which drive design requirements reinforced with historical examples of the interaction over a range of products. The development of a microprocessor organization for continuous system simulation with one for one correspondence with analog functions will be examined and quantitative results revealed. Development of a general-purpose digital emulation facility will be described. Methodology investigations with time and instrumentation validation against a specific hardware system will be presented.

"Techniques for Requirements—Oriented Design," Kenneth J. Thurber, Sperry Univac

"A Multi-Microprocessor Approach to a High Speed and Low-Cost Continuous System Simulation," Ryoicki Yoshikawa, Tatsuo Kimura, Yashuiro Nara, and Hideo Aiso, Keio University, Yokohama, Japan

"Instrumental Architectural Level Emulation Technology," Harrison R. Burris, TRW

Panelists include Dr F. G. Spadaro, TRW Systems; Dr C. Perkins, General Research; and John A. Cornell, System Development

Session 85 — 2:00-3:30 pm

Special Memory Architectures

Chairman: William E. Cantrell, General Dynamics Corp, Fort Worth, Tex

Specialized memory architectures will be presented in set associative problem solving, and in optimum local memory accessing for multiprocessor configurations. The particular memory devices investigated make maximum use of advanced semiconductor technology, modularity, economically structured algorithms, and optimal hardware and software partitioning.

"ARES—A Memory, Capable of Associating Stored Information Through Relevancy Estimation," Tadao Ichikawa, Kokusai Denshin Denwa, Ltd, Tokyo, Japan; and Ken Sakamura and Hideo Aiso, Keio University, Yokohama, Japan

"Cache Memory Systems for Multiprocessor Architecture," O. P. Agrawal, Collins Radio and A. V. Pohm, Iowa State University

"Pseudo Random Access Memory Systems with CCD-SR and MOS RAM on a Chip," Naoya Ohno and Katsuya Hakoyaki, Nippon Electric Co, Kawasaki City, Japan

Session 87 — 2:00-3:30 pm

Simulation Methods

(Information not available at press time.)

Session 88 — 2:00-3:30 pm

Personal Computing Systems

Chairman: Roger L. Mills

Providing the personal computer buff with an evaluation of the tradeoffs (cost vs speed, accuracy, time) which can be made during design of a low cost data acquisition and control system, the session also includes a description of a small system which uses the UNIX philosophy of command processing.

"Low Cost Data Acquisition and Control System," Ralph Tenny, Pavco Electronics

"DISKOMANIA: A Small System Floppy Disc Operating System," Wayne Sewell, Dallas, Tex

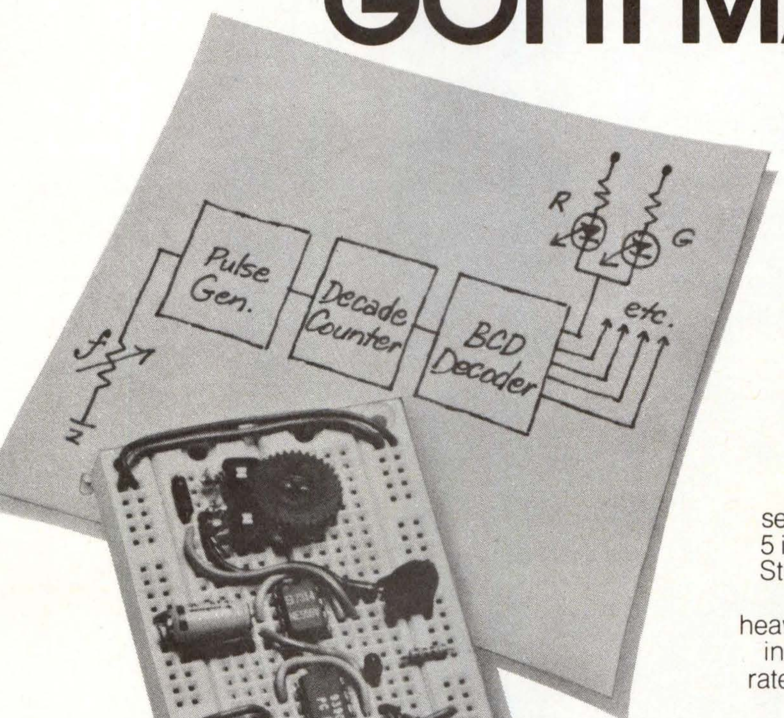
Session 89 — 3:45-5:15 pm

Trends in Computer Stores

Chairman: David Wilson, The Micro Store, Richardson, Tex

(Information not available at press time.) □

ONCE YOU'VE GOT IT DESIGNED, YOU'VE GOT IT MADE.



It's that easy when you use CSC's QT solderless breadboarding Sockets and Bus Strips. Working directly from logic or block diagrams, you plug in IC's, transistors, resistors, capacitors, LED's —virtually any component—and optimize circuits stage-by-stage, literally as fast as you can think. (No special jumpers required, either—just ordinary #22-30 solid hookup wire.)

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You'll find QT Sockets and Bus Strips useful in lots of other ways, too. Mounted on power supplies, test equipment, bench or plug in cards, they're equally at home in lab, on production lines, in QC test jigs or in the field, for on-the-spot emergencies.

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Length / Hole-to-Hole	Length	Hole-to-Hole	Terminals	Unit Price $*
QT-59S	6.5"	6.2"	118	12.50
QT-59B	6.5"	6.2"	20	2.50
QT-47S	5.3"	5.0"	94	10.00
QT-47B	5.3"	5.0"	16	2.25
QT-35S	4.1"	3.8"	70	8.50
QT-35B	4.1"	3.8"	12	2.00
QT-18S	2.4"	2.1"	36	4.75
QT-12S	1.8"	1.5"	24	3.75
QT-8S	1.4"	1.1"	16	3.25
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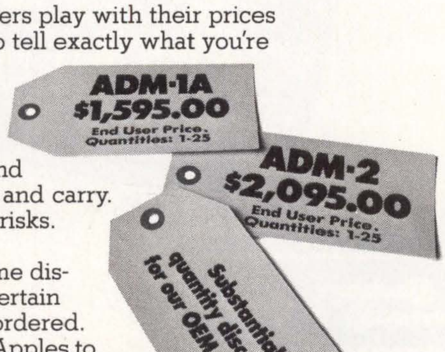
If you're confused about "smart" terminal prices, you're not alone.

The way some terminal builders play with their prices — and misquote ours — it's hard to tell exactly what you're getting. Or when.



To help, we offer the adjacent prices. Prices that reflect what the Lear Siegler ADM-1A and ADM-2 are *really* selling for. To end users. In quantities of one. Cash and carry.

The point is there are no asterisks. No fine print. No games.

And no phony quantity volume discount prices that also assume a certain number of special options were ordered.

Just prices you can compare. Apples to apples. Oranges to oranges. Prices we've recently been able to lower because of our own successes.

Hurry up and wait?

In truth, a good terminal buy means much more than just an attractive purchase price.

Delivery can be just as important. Because waiting 60, 90, even 180 days for someone else's "bargain beauties" to arrive can cost you a small fortune. Not to mention the wasted time.

It's nice to know that ADM-1A's and ADM-2's are now available for immediate delivery. Ready to go to work.

And it's also reassuring to know that both the ADM-1 and ADM-2 have more than 2 years of field-proven performance behind them. In almost every conceivable application.

In place of the just-past-prototype risks you get with recent terminal arrivals, the ADM-1A and ADM-2 deliver field-proven quality and reliability.

Two things an attractive purchase price, alone, can never guarantee.

The lowdown on our highbrow. Our ADM-2.

New price aside, our ADM-2 is probably all the "smarts" you'll ever need.

Offering full editing facilities. Sixteen function keys for up to 32 discrete messages. Eight screen status indicators. A special numeric keypad. Eight selectable baud rates from 110 to 9600. Protected fields. A dual intensity, 12" diagonal screen. Even a keyboard that's detachable, as well as lockable.

All standard.

Or, have it your way. With our ADM-1A.

We call the ADM-1A our "with or without" model.

Because it lets you select the exact combination of options that are just right for your application.

Starting with some pretty smart standard features, like a 12" diagonal screen. New integral numeric keypad. Protected fields. Internal repeat. Block send capabilities. And building up from there.

You add just the "bells and whistles" you need.

Instead of getting stuck with expensive engineering overkill you'll never use.

But then, that's always been our goal at Lear Siegler. Right from the start. To build terminals truly dedicated to the systems they serve. In terms of intelligence, function, and price.

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Programmable Multiline Communications Processor Provides Front-End Flexibility

Kenneth T. Coit

Honeywell Information Systems, Incorporated
Billerica, Massachusetts

Programmability means different things to different people. In its most general sense, it refers to a computer's applicability to any of a wide variety of tasks. At the other extreme, the word describes apparatus that can be configured in a certain way by loading a register under software control (the software being in a different machine) or even by manually plugging a jumper wire into one of several different sockets.

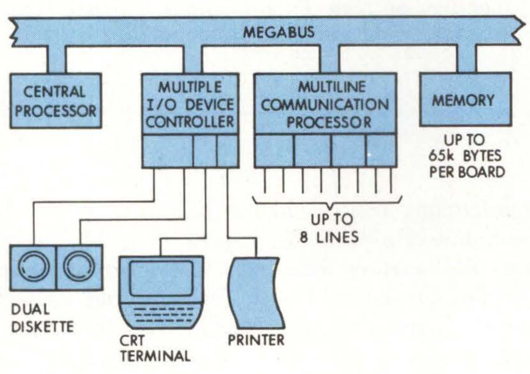

Fig 1 Typical communication-oriented system. Essentials are central processor, memory, multiple device controller, and communications processor. The latter, in the Honeywell Level 6, controls transmission and reception on up to eight lines

Neither of these extremes describes the programmability of the multiline communications processor (MLCP), part of Honeywell's Level 6 computer system (Fig 1). Although it is programmable, in the sense that the user writes a program that tells the processor what to do under various conditions that arise during operation, it cannot operate as a standalone computer. Its instruction set, although extensive, is limited to commands that are useful in controlling communication lines. Nevertheless, it is more sophisticated than a controller, which either is not programmable or is programmable only in a limited sense—most likely at the firmware level.

MLCP users can write channel control programs which the unit will execute. These programs control individual line interfaces, check for status changes, manipulate data, and control scatter/gather activities in main memory with the aid of multiple channel control blocks. Software controls more than the usual number of data communications parameters: speeds, stop bits, mark and space hold, fill characters, sync characters, character size, character parity, four different cyclic redundancy check (CRC) polynomials, loop-back, and direct connect, among others.

General Architecture

The communications processor is based on a commercially available microprocessor, which performs many functions of a modern operating system. It maintains orderly execution of a variety of user programs;

responds to hardware interrupts from line interfaces; and oversees the sharing of resources such as the Megabus* interface, CRC hardware, and the microprocessor itself.

Intent of the architecture (Fig 2) is to maintain modularity and flexibility with careful consideration to cost. Those functions which can be performed most economically during time slices are generally implemented on the MLCP motherboard. Some other functions, which might have been performed by time slicing in earlier technologies, are implemented with large-scale integrated (LSI) circuits to provide higher performance at minimal cost.

For example, cyclic redundancy checking is time sliced. Although an LSI chip could have been placed in each synchronous line interface card, the chip would have been underutilized and the cost of each interface would have increased. Instead, a single implementation on the motherboard performs the CRC operation for all channel control programs, permitting software control of the CRC polynomial and analysis of the residue.

By including character parity generation on the motherboard, the unit can communicate with all types of binary synchronous devices. For example, a bisync terminal that is capable of ASCII transparency (ie, transmits all 7-bit combinations), when operating in a non-transparent mode, must terminate character parity generation before transmitting the block check characters. With LSI implementations, this character parity switching is not possible because the LSI chip is synchronized, not to the communications processor, but only to the modem data clocks.

Those functions which either require full time attention or fast response to real-time events have been placed in the line interfaces, called Communication-Pacs. These functions include operations which must be performed more than once per byte, such as detection of start bit, framing error, sync character, and flag for various protocols. Obviously, line interface units also contain storage, drivers, and receivers to match the data circuit equipment. In addition, they generally include an integrated transmitter/receiver, which converts between parallel and serial data.

Each interface unit contains two line interfaces, one of which is shown in Fig 3. Registers in each unit are directly addressed by MLCP software to transfer control and status information as well as data. To accommodate a larger variety of applications and speeds through modularity and programmability, most of the functionality tradeoffs fall on the side of higher complexity, unlike some other communication controllers. The MLCP can work with synchronous, asynchronous, and bit-oriented interface units at speeds from 50 bits/s to 72 kilobits/s.

Central Processor Interaction

The communications processor is, of course, only part of the computer system. It is controlled by the central processor unit (CPU), and for data it requires access to main memory via the Megabus.

Data are transferred directly to and from memory to minimize the frequency of CPU interaction. CPU efficiency is further improved by storing up to four communications control blocks (CCBs) in the MLCP for each line direction or channel (Fig 4). Each CCB contains the starting memory address for a contiguous data buffer, the buffer length (range), and control and status information for the MLCP. The four CCBs for a single channel form a circular queue, whose corresponding data buffers may be widely separated in the memory. As a result, incoming data can be scattered into these widely spaced buffers, and outgoing data can be gathered from them.

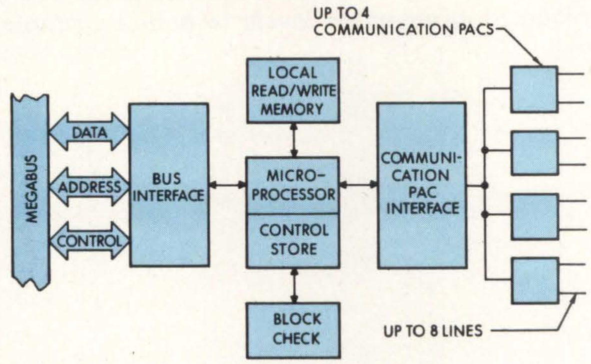

Fig 2 Communications processor. Programmable communication front end is designed around a microprocessor and can have interfaces with any of several kinds of communication lines for direct transfer to and from main memory via the bus

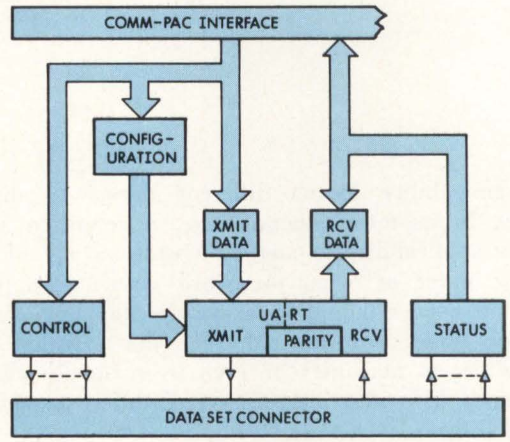

Fig 3 Half a Pac. Typical Communications-Pac contains two interfaces, one of which is diagrammed here. Each interface contains registers for data, status, and control

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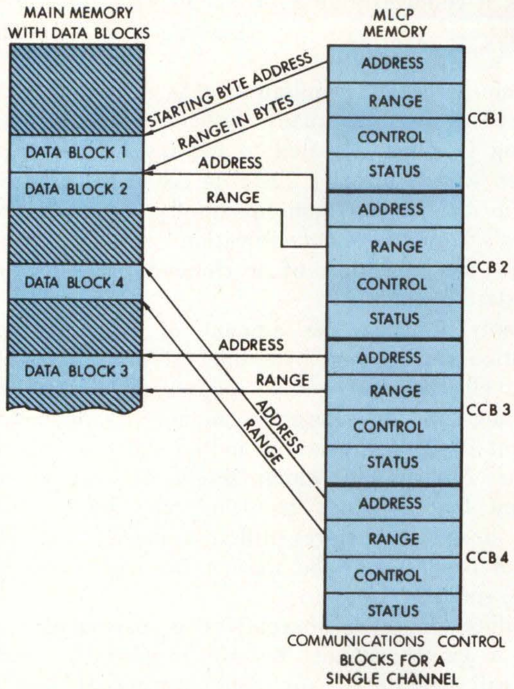

Fig 4 Direct access path. The MLCP uses direct memory access for all data transfers in either direction, monitored by communication control blocks. Four of these blocks are available per channel, permitting scatter/gather operations

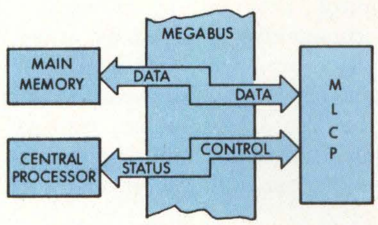

Fig 5 MLCP/CP interaction. Communication processor obtains control information from and sends status information to the central processor, but transfers data directly to and from the memory

Typical Line Control Table (LCT)

LCT Byte Address	Contents
0	Firmware work area
1	Firmware work area
2	Receive configuration
3	Receive CRC residue—byte 1
4	Receive CRC residue—byte 2
5	Firmware work area
6	Receive CCP pointer—8 LSB
7	Receive CCP pointer—4 MSB
8	Receive channel command
9	Firmware work area
10	Receive data—left byte
11	Receive data—right byte
12	Receive return channel number
13	Receive level
14	Receive Comm-Pac status
15	Receive Comm-Pac status mask
16	Receive status—byte 1
17	Receive status—byte 2
18	Receive CCP subroutine pointer—8 LSB
19	Receive CCP subroutine pointer—4 MSB
20	Receive Comm-Pac control
21	Firmware work area
22	Firmware work area
23	CCP work area
24	CCP work area
25	CCP work area
26	CCP work area
27	CCP work area
28	CCP work area
29	CCP work area
30	CCP work area
31	CCP work area

CCP = Channel control program
CRC = Cyclic redundancy code

In the past, a major bottleneck in some communication systems has been the interface to memory and control of the data transfer (Fig 5). Some systems have required one or more memory cycles for every bit received. However, the congestion is relieved by the use of a microprocessor, capitalizing on the communication processor's programmability to permit multiple block transfer capability for each transmission or reception. Thus, the CPU need only set up the buffers, command the channel to transmit or receive (as appropriate), and wait for an interrupt from the MLCP, indicating that the operation has terminated. With 64 levels of vectored interrupt and a channel identification facility, no steps are wasted in determining the cause of the interruption, even at the end of the message.

Line control tables in the communication processor's read/write memory temporarily store control, status, and data for each line direction or channel. "Typical Line Control Table (LCT)" shows a receive channel.

Instruction Set

Most of the tasks associated with data communication can be performed by the communication processor. It controls data circuit equipment, monitors data circuit status, controls character format, delimits the message, performs limited editing, transliterates from one code to another, and branches to any of as many as 128 different routines on any data or control byte. These functions are controlled by the user through its extensive instruction set.

Other communication processors also give the user access to processing power, but in other ways. One manufacturer, for example, does not permit the user any executable code, although the design is based on a microprocessor. Another simply installs one general-purpose central processor in front of another similar one, giving the user more power than a small configuration justifies. In the MLCP, the instruction set is tailored to the communications task alone; it forces the user to write a re-entrant code which every channel can share. Thus, if only one protocol is to be supported, only one copy of the code for it need reside in the MLCP memory for all the channels.

Conversely, if necessary, every channel can be controlled by its own program; there is enough power in each instruction and sufficient space in the memory to permit this individual control. Furthermore, the central processor can load and dump the memory in block mode for easy initialization and debugging.

Line Capacity

Two physical parameters combine to make eight full-duplex lines very practical with current and near-future technology. First, cost of a system is more strongly affected by the number of circuit boards and the number of different types of circuit boards than by the number of components on the boards; and the motherboard has to be the same size as the others in the system. Therefore a single board communication processor is a must.

Second, for most applications several different types of communication lines need to be connected to a single processor. Since the communication line interface units generally occupy one-fourth the space available on a full-sized board, and since synchronous and asynchronous units support two lines each, a basic capacity of eight lines is almost an automatic specification. However, Communication-Pacs for most bit-oriented lines require more space than those for byte-oriented lines, because they implement more complex functions; therefore, in general, they control only one full-duplex line each, reducing the MLCP's total capacity.

Throughput

Any data processing system's throughput depends heavily on the specific application and configuration; communication processors are no exception. In the case under discussion, functionality is distributed among the Communication-Pac, the MLCP, and the central processor. Upper limit of system performance, assuming that software controls only the movement of data between one communication line and the system's main memory, with no local processing, is a continuous rate of 23k bytes/s. Alternatively, for low speed applications, the processor's power can be directed to more complex message processing functions. For example, when configured with eight half-duplex lines operating at 300 bits/s, it could execute approximately 50 times as many instructions per byte as when pushing through 23k bytes/s.

A more realistic configuration is a mix of high and low speed lines. In many systems hardware resource sharing is either adjusted to the fastest line or implemented with a priority interrupt scheme. In the MLCP, a priority scheme nonsequentially processes service requests from the Communication-Pacs, but cannot interrupt the execution of a channel control program, once started.

Simply limiting the amount of code written for execution during one byte interval on the fastest line is not efficient. This either reduces all channel control programs to the lowest common denominator—the amount of code executable in the shortest byte period of the fastest line which might be configured, an amount that is much less than can be executed on other lines—or requires different drivers and channel control programs to be written for each configuration of line speeds.

Neither of these alternatives is particularly attractive. A single channel control program is desirable, that will operate in any configuration of line speeds and that will work as well with the fastest line as with the slowest. An antihogging feature permits the user to write code for a given line procedure and maximum speed without particular concern for other lines connected then or added later. More delicately, antihogging is called Pause, because it scans for higher level service requests while temporarily halting a channel control program in progress, limiting the number of consecutive instructions at each level. The user may write programs that exceed this maximum length without concern; the processor saves the context each time the Pause is imposed, transparently to the channel control program, and restores it later when resuming the program at that level.

Summary

The multiline communications processor provides for modular off-loading of the Level 6 central processor, executing user-written channel control programs for each line. Multiple DMA block capability is provided for each line direction, permitting scatter/gather activities without central processor intervention. Based on a commercially available microprocessor, the unit incorporates the latest in technology to enable cost-effective systems to be configured in any size.

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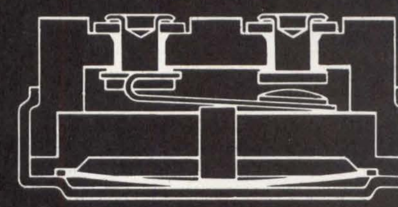

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Previously, computer system simulation was highly complex, time-consuming, and tedious, requiring man-months of software derivation and hours of computer run time. Now it is possible to evaluate and optimize a large number of computer hardware design configurations in minutes, using a simple program and a handheld calculator

Computer Simulation On a Pocket Calculator

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Modeling a proposed computer system helps to specify and document the design. Being forced to ask the right questions is valuable, even if the modeling effort progresses no further. After gathering preliminary specifications, an early simulation model will give the designer a feel for performance, so that hardware can be chosen correctly. As software is written, programmers can use models to make intelligent gross decisions by experimenting with various design alternatives. After the computer system is built, actual performance can be measured to refine earlier estimates and fine-tune the model. Enhancements, modifications, and additions then can be simulated without disturbing or jeopardizing the integrity of the actual system.

Practical analytical models have not been well publicized. Usually scholarly and abstruse, their derivations appear in highly mathematical journals, and involve heavy probability and queuing theory. For the past 12 years, the author has applied classical multiserver queuing equations to computer system design with great success. The simulation model presented is based on this foundation.

Modeling a computer system no longer requires man-months of programming work or hours of computer run time. Specialized programming languages or proprietary software packages are useful tools but are not always necessary. This article describes an understandable analytic model, which is based on queuing theory and is programmed for the Texas Instruments SR-52 pocket calculator. It is ready for immediate and practical application.

Having this computer system model preprogrammed on a pocket calculator will expand the design engineer's decision-making capacity; the ability to immediately evaluate and optimize a large number of computer configuration problems is readily available. Instruction listing and simulation examples for the SR-52 are included; with reprogramming, the simulation model can run on a Hewlett-Packard HP-67.

Model Objectives

An entire computer system has been modeled, including central processor unit (CPU), main memory, peripheral auxiliary storage, and terminals or card readers. Any level of multiprocessing and multiprogramming is accommodated. The model is extremely powerful, and only a few simplifications are necessary. Multiprogramming is taken to operate at a fixed level, M. The model can overlap accesses to peripheral storage devices (I/O) with CPU processing for different jobs, but serializes them within each job. Average access service time, i, is assumed to be independent of the number of outstanding I/O requests. Although this means that a simulation does not explicitly account for I/O queuing or optimization, service time i may be judiciously adjusted so that they are taken into consideration. Such parameter fine-tuning could be part of a validation process.

Three measures of computer system performance are processor utilization, throughput, and response time. CPU utilization is of interest mainly to the designer, while the operations manager and users are more concerned with the job processing rate and in job turnaround. As the model simulates both batch and real-time systems, the terms job, message, and inquiry are used synonymously. Job processing rate is throughput. Average response and turnaround time take on the same meaning: the total time a job spends in the system from input to output.

The objective is to optimize performance at minimal cost. Throughput should be maximized and response time minimized, all within cost constraints. Very low CPU utilizations are undesirable as they show that the processor is not operating anywhere near its rated capacity. On the other hand, allow for future expansion and never attempt to fully utilize a CPU.

Simulation results must be interpreted correctly. Queue sizes are not predicted by the models. However, classic probability and queuing theory indicates that queues grow alarmingly as CPU utilizations exceed 80% (see Martin, p 384). When this occurs, there is the danger of buffers and files overflowing. Operating system performance is also usually severely degraded at very high CPU utilization. In effect, the operating system is so busy that it becomes confused and does not know what to do next. Therefore, when the model predicts CPU utilizations above 80%, recognize this as a danger zone and proceed with caution.

Constant and Exponential Service Times

Derivation of analytic models is so complex that certain compromises must be made for the sake of simplicity. Establishing service times as either constant or exponential is standard procedure in deriving analytic queuing models. These are the two distributions which produce manageable equations.

When service times are constant, there is no variation from the mean. The standard deviation is zero. Probability of service completing is a direct function of what has transpired earlier in time. There is no uncertainty to complicate calculations.

Assuming exponential service time is equivalent to stating that there is a Poisson service pattern. This translates to a fluctuating service rate where the standard deviation squared equals the mean. At any point in time, the probability of completing service is entirely independent of what has occurred earlier. It is this lack of memory that simplifies the derivation.

Think of constant and exponential services as inverses—one always fixed, the other fluctuating. Fortunately, this works out well, because most situations encountered in real systems lie somewhere between the two. Usually, constant and exponential services are both modeled. Then, both models are simulated to establish boundaries. Real system performance lies somewhere between these limits.

Service times are assumed to be either all exponential or all constant. Both models have been programmed for the SR-52. The consequences of an exponential assumption are a lower limit for CPU utilization and throughput, and an upper boundary for response time. Postulating constant service times results in an upper boundary on CPU utilization and throughput, and a lower limit for response time.

Calculator Input Parameters

CPU utilization keys marked Ue and Uc apply to the exponential and constant models, respectively. Throughput (T) and response time (R) keys are used by both models. Simulation requires storing input parameters in calculator memory registers 1 through 7, and depressing the appropriate CPU utilization key. After utilization has been displayed, either throughput (T) or response time (R) can be computed.

Concise user instructions for the SR-52 programmable calculator are listed in Table 1. Inquisitive readers may wish to consult Boyse and Warn for the equations and derivations. However, in a practical sense, the computer designer is given all that he needs to run and use the model in the instructions that follow.

CPU utilization cannot really exceed 100%. However, as a mechanism to indicate the degree of a possible overload, Uc is permitted to display higher values. When this occurs, the model equates Uc to 100% in any following calculations; the user should do the same.

Handheld calculator and preprogrammed card simplify computer system simulation for fast, accurate, and convenient design analysis

TABLE 1

SR-52 User Instructions for Analytic Computer Model

Step	Procedure	Enter	Press	Display
1.0	Load program card (sides A and B)			
2.0	Input parameters, all with same time unit			
2.1	Average CPU time (application + OS) per interaction or job $C=\frac{\text{Total CPU active time}}{\text{Number of jobs}}$	C	STO 0 1	
2.2	Average CPU time period between I/O operations $c \leq C$ $c=\frac{C}{\text{Number of I/Os/job}}$	c	STO 0 2	
2.3	Average service time for an I/O request. You may add in I/O queuing time i=(% I/O drum) x (delay + transfer) + (% I/O disc) x (delay + transfer + seek)	i	STO 0 3	
2.4	Fixed level of multiprogramming Number of jobs simultaneously in main storages of all CPUs	M	STO 0 4	
2.5	Number of active terminals or customers $N \geq M$	N	STO 0 5	
2.6	Average user think time If N=M, Z=O	Z	STO 0 6	
2.7	Number of multiprocessing CPUs. Jobs execute on any CPU $j \leq M$	j	STO 0 7	
3.0	Exponential model: Lower bound on CPU utilization and throughput Upper bound on response time			
3.1			Ue	CPU utilization
3.2	Interactions or jobs processed per unit time		T	Throughput
3.3	Turnaround time		R	Average response time
4.0	Constant model: Upper bound on CPU utilization and throughput Lower bound on response time			
4.1			Uc	CPU utilization
4.2	Interactions or jobs processed per unit time		T	Throughput
4.3	Turnaround time		R	Average response time

Seven input parameters are required for a simulation. They can be determined by reviewing documentation and/or monitoring actual system performance.

The time the processor is active for each job or message is denoted as C, which is a summation of application plus operating system components. Within a representative time period, dividing the total time the CPU is active by the number of jobs processed calculates to C. Store this quotient in calculator memory 1.

TABLE 2

Simulation Model Examples

Example	C	c	i	M	N	Z	j	Ue (%)	T	R (s)	Uc (%)	T	R (s)
	Calculator Input Parameters							Computer System Results — Exponential Model			Constant Model		
1	0.10	0.006	0.035	6	240	10	2	43.21	8.64	17.77	43.90	8.78	17.33
2	0.10	0.006	0.035	8	240	10	2	56.55	11.31	11.22	58.54	11.71	10.50
3	0.10	0.006	0.035	14	240	10	2	87.66	17.53	3.69	100.00 (102.44)	20.00	2.00
4	0.10	0.006	0.035	18	240	10	2	97.15	19.43	2.35	100.00 (131.71)	20.00	2.00
5	0.10	0.006	0.022	6	240	10	2	61.21	12.24	9.61	64.29	12.86	8.67
6	0.10	0.006	0.015	6	240	10	2	76.66	15.33	5.65	85.71	17.14	4.00
7	0.10	0.006	0.012	6	240	10	2	84.44	16.89	4.21	100.00	20.00	2.00
8	0.10	0.006	0.005	6	240	10	2	98.70	19.74	2.16	100.00 (163.64)	20.00	2.00
9	0.20	0.012	0.035	6	240	10	2	70.60	7.06	23.99	76.60	7.66	21.33
10	0.10	0.006	0.035	6	240	10	1	74.69	7.47	22.13	87.80	8.78	17.33
11	0.05	0.003	0.035	6	240	10	1	45.45	9.09	16.40	47.37	9.47	15.33
12	0.10	0.006	0.035	6	240	0	2	43.21	8.64	27.77	43.90	8.78	27.33
13	0.10	0.006	0.035	6	400	10	2	43.21	8.64	36.28	43.90	8.78	35.56

Note: All input parameters are required to be expressed in the same time unit (ie, seconds)

C = (total CPU active time) ÷ (number of jobs processed)

For the same time period, divide the number of accesses to disc and drum by the number of jobs processed. The result is the number of I/O accesses per job. Divide the previously calculated C by this new quantity. The resulting quotient, c, should be stored in calculator memory 2.

c = C ÷ (number of I/O accesses per job)

References to disc and drum take time. Among the factors to be considered are rotational delay, data transfer time, and seek time. All three need to be included for discs. Fixed head drums, by definition, have no arm movement and therefore zero seek time.

Calculator memory 3 must contain the average service time for a peripheral storage access. To determine this quantity, designated by i, compute the service time for each peripheral storage device in the system. This is the sum of its rotational delay, data transfer time, and seek time. Multiply each device's service time by its percentage of I/O accesses. Finally, add these weighted service times. Store the resulting sum of i into memory 3.

Dx = rotational delay for device x

Tx = data transfer time for device x

Sx = seek time for device x

n = number of storage devices in the system

i = (% of accesses to device 1) x (D1 + T1 + S1) +
(% of accesses to device 2) x (D2 + T2 + S2) + ... +
(% of accesses to device n) x (Dn + Tn + Sn)

The number of jobs simultaneously active within a system is the level of multiprogramming, M. Often this is equivalent to the number of specified initiators. Once accepted into main memory, a job is considered active, albeit in queue, in processing, or accessing peripheral storage. Where there is multiprocessing, M includes all jobs active within all processors. Store M in calculator memory 4.

N, indicating the number of system users, is stored in calculator memory 5. For a real-time system, N represents the number of terminals.

How soon after receiving a printout does a programmer submit his next job? What is the time period between a customer's inquiry and his terminal's preceding response? These are "user think" times. The average contemplation time period between a system response and a user's succeeding reply is given notation Z and loaded into calculator memory 6. A user submits jobs or messages with an interarrival time that is the summation of his think time (Z) plus system response time (R).

Multiprocessing level, designated by j, is the number of CPUs embodied in the system. For example, a uniprocessor equates j to 1. This is the last of the model's input parameters and is stored in calculator memory 7.

Simulation Model Examples

Thirteen illustrative simulation model examples (see Table 2) provide useful exercises. Both input parameters and simulation results are tabulated. Actual computer system performance is somewhere between the boundaries indicated by the exponential and constant models. Examples 1 through 4 show the effect of increasing the level of multiprogramming (M). Note that CPU utilization and throughput both rise, but response time falls. Once the CPU reaches saturation, throughput

TABLE 3

SR-52 Coding Form for Analytic Computer Model

Loc	Code	Key	Loc	Code	Key	Loc	Code	Key
000	46	LBL	075	00	0	150	44	SUM
	19	D'		09	9		01	1
	42	STO		58	dsz		02	2
	00	0		00	0		58	dsz
	00	0		07	7		01	1
005	56	rtn	080	03	3	155	01	1
	46	LBL		09	9		05	5
	10	E'		10	E'		43	RCL
	42	STO		44	SUM		01	1
	01	1		00	0		03	3
010	09	9	085	08	8	160	55	÷
	36	IND		43	RCL		07	7
	43	RCL		01	1		10	E'
	01	1		00	0		85	+
	09	9		19	D'		01	1
015	56	rtn	090	01	1	165	95	=
	46	LBL		22	INV		19	D'
	16	A'		44	SUM		81	HLT
	43	RCL		01	1		46	LBL
	00	0		00	0		13	C
020	04	4	095	58	dsz	170	00	0
	75	—		00	0		10	E'
	43	RCL		06	6		75	—
	00	0		09	9		01	1
	00	0		08	8		95	=
025	85	+	100	10	E'	175	22	INV
	01	1		20	1/x		80	if pos
	95	=		94	+/−		01	1
	55	÷		42	STO		08	8
	43	RCL		01	1		01	1
030	00	0	105	03	3	180	00	0
	03	3		07	7		85	+
	65	x		10	E'		01	1
	43	RCL		49	PROD		95	=
	00	0		01	1		65	x
035	02	2	110	03	3	185	07	7
	55	÷		42	STO		10	E'
	53	(		01	1		55	÷
	43	RCL		02	2		01	1
	00	0		19	D'		10	E'
040	00	0	115	08	8	190	95	=
	75	—		10	E'		56	rtn
	07	7		20	1/x		46	LBL
	10	E'		42	STO		14	D
	54	)		01	1		13	C
045	80	if pos	120	01	1	195	20	1/x
	00	0		16	A'		65	x
	05	5		49	PROD		05	5
	03	3		01	1		10	E'
	00	0		01	1		75	—
050	10	E'	125	58	dsz	200	06	6
	95	=		01	1		10	E'
	56	rtn		02	2		95	=
	07	7		01	1		81	HLT
	10	E'		43	RCL		46	LBL
055	95	=	130	01	1	205	12	B
	56	rtn		02	2		04	4
	46	LBL		75	—		10	E'
	11	A		07	7		55	÷
	01	1		10	E'		07	7
060	42	STO	135	95	=	210	10	E'
	00	0		65	x		55	÷
	08	8		43	RCL		53	(
	04	4		01	1		01	1
	10	E'		01	1		85	+
065	42	STO	140	95	=	215	03	3
	01	1		44	SUM		10	E'
	00	0		01	1		55	÷
	19	D'		03	3		02	2
	01	1		43	RCL		10	E'
070	42	STO	145	01	1	220	54	)
	00	0		02	2		95	=
	09	9		19	D'		19	D'
	16	A'		01	1		81	HLT
	49	PROD		22	INV			

Labels: A = Ue, B = Uc, C = T, D = R

Registers: 00 = —, 01 = C, 02 = c, 03 = i, 04 = M,
05 = N, 06 = Z, 07 = j

and response time level off. In examples 5 through 8, average I/O access time (i) is successively decreased. Again, CPU utilization and throughput both increase while response time decreases, that is, until the CPU becomes a bottleneck. Terms C and c are increased 100% in example 9. This means that the CPU is twice as slow as in the preceding examples. Example 10 is a uniprocessor (j = 1) with the same speed CPU as described earlier. Apparently, it is more effective to use one fast CPU than two slow ones. This is verified by example 11. In example 12, user think time (Z) is reduced to zero. The number of terminals (N) is expanded to 400 in example 13. Note the increases in response time.

Summary

Detailed discrete models can execute for hours on full size computers before reaching steady-state results. What can be expected of an analytic model run on a handheld calculator? The SR-52 program listing in Table 3 has been optimized for speed and user convenience. The Uc and throughput values are computed in 2 s, response time takes less than 3 s, and these operating times are always constant. Only the calculation time of CPU utilization for the exponential model is variable, depending on level of multiprogramming (M) and multiprocessing (j). Running times for Ue range from 8 s to several minutes. A complex system, multiprocessing with three computers and multiprogramming a combined total of 21 simultaneously active jobs, simulates in 7 min.

Whenever possible, simulations of existing systems should be validated with empirical measurements. By rerunning the model through many iterations and adjusting earlier estimates to bring results closer to observed performance, greater confidence and better insight into the computer system's operation will be gained. After validation fine-tuning, examine the effects of prospective design changes. With a handheld programmable calculator, and this model on a program card, complex design decisions can be based on simulation results, rather than intuition.

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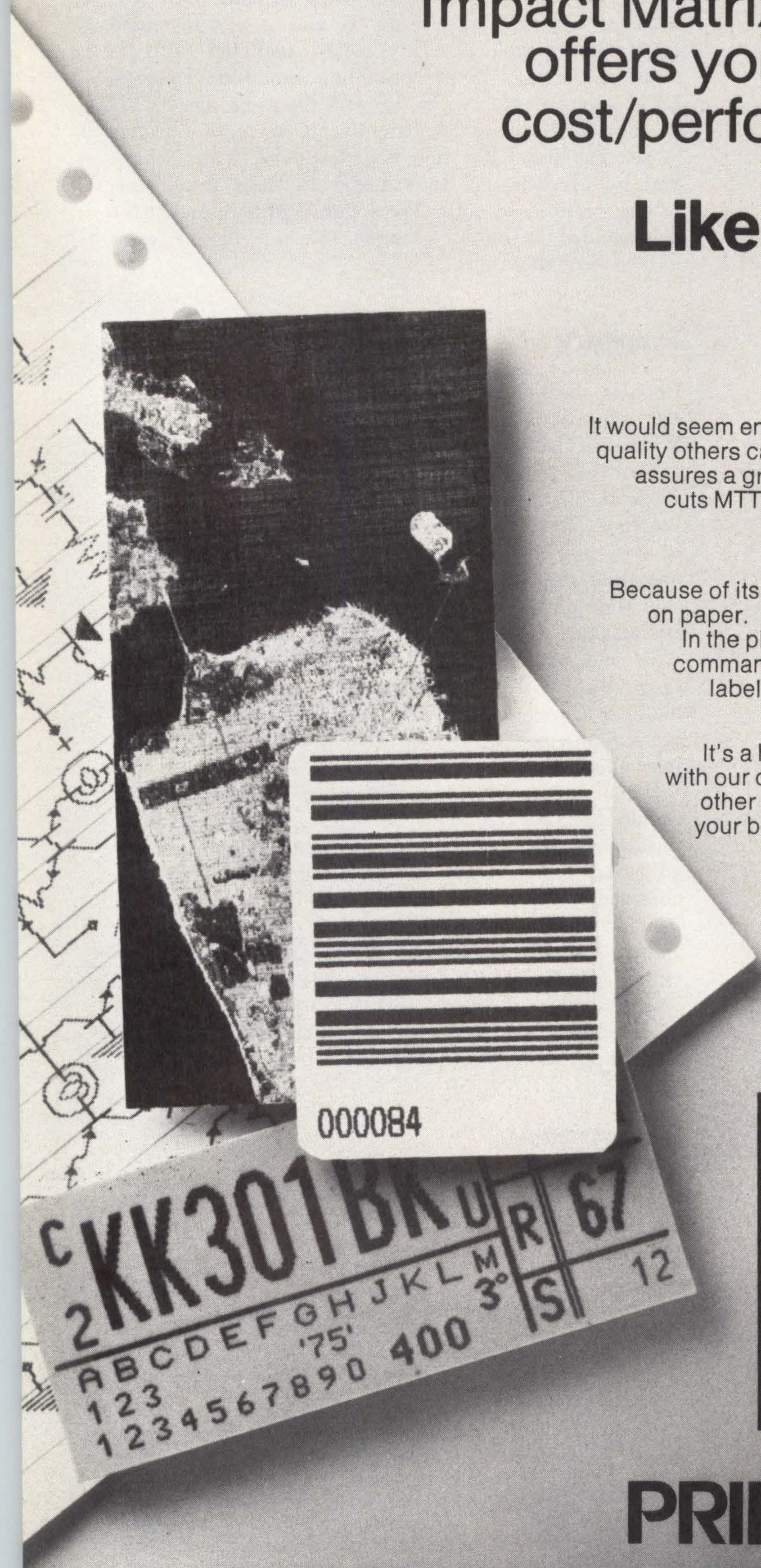

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Mixed Logic Leads to Maximum Clarity With Minimum Hardware

Franklin Prosser and David Winkel

Indiana University
Bloomington, Indiana

Digital design is a challenging task. For designers, efficiency is greatly influenced by the techniques used to develop and implement the designs. The time spent, the clarity of documentation, and the correctness of the result depend heavily on hardware design style. A good design style should be easy to learn, force the designer to think through the total design before construction starts, result in clear, easy to understand circuits, and produce clear documentation as a by-product of the design process. The common thread running through these criteria is *clarity of thinking and presentation.*

Design Style

For several years the authors have used a collection of design techniques that form a particular "style" to meet the criteria given above. This style includes a convenient way to represent a problem-solving algorithm as a hardware flowchart, a powerful circuit convention for developing hardware circuit diagrams from logic equations, and a general method for implementing the next state generator from the flowchart.

Several of these techniques are old, but their power has not been widely appreciated. To help construct and document the algorithms, the Algorithmic State Machine (ASM) Chart notation of Clare[1] is used. To move directly and easily between logic and its hardware implementation, a circuit diagram convention embodying "mixed logic" polarities[2] is used. A universal next-state generator uses multiplexers to route the correct signals to the state flip-flops; a description of this technique was presented earlier,[3] but this document is not generally available to the design community.

Beginning with a clear specification of what problem is to be solved, the design process then moves to a development of a solution to the problem in terms of a data structure (registers, buses, etc) and a control algorithm to perform the necessary movement of data and signals through the structure. The designer then implements the algorithm and data structure with physical devices. The control algorithm results in a set of Boolean logic equations which must be translated into a hardware circuit diagram. Mixed logic notation provides an optimal way to move from logic equations to a representation in terms of the available physical devices.

Editor's Note: Many of the logic designs that the authors discuss are no longer implemented with gates (such as NANDs, NORs, or XORs). However, despite the availability of functional LSI (such as PLAs, p/ROMs, and MUXs), the ideas expressed here remain pertinent to logic design.

Mixed Logic

Logical operations AND, OR, and NOT are familiar tools applied in everyday design activities. So there is strong and justifiable motivation for the digital designer to develop combinatorial logic in terms of these familiar primitives. On the other hand, designers frequently wish to use physical devices—gates—that are named NAND, NOR, and the like. Conventional methods treat these devices as if they were in fact performing logic NANDs and NORs, requiring awkward intermediate transformations of the original logic in order to achieve a physical implementation. This is neither appropriate nor necessary, since mixed logic, as shown in this article, offers significant improvements over conventional methods.

To achieve the stated goal of clarity of thinking and presentation, the notation used for circuit diagrams must have two fundamental properties:

(1) Logic equations must lead directly to physical implementations, without elaborate transformations.

(2) An analysis of a physical implementation must lead directly back to the original logic, without elaborate transformations.

These strong properties, neither of which is met in today's typical circuit diagram, imply that both the digital logic and the physical circuit can be clearly displayed on the same diagram. This leads to three specific circuit conventions: circuit symbols should represent the combinatorial logic in AND-OR-NOT form, since that form is most natural for developing the logic equations; correspondence between a logic value (TRUE or FALSE) and its physical voltage counterpart (HIGH or LOW) should be evident at any point in the circuits; and notation should clearly display the type of physical device used at any point in the diagram.

Mixed logic, an old digital design concept, has proven to be a new, powerful, and elegant method and a fresh, natural approach for establishing the desired circuit conventions.

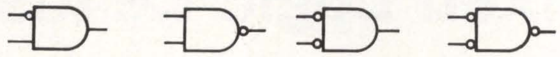
Logic Definitions

The AND and OR logic functions are represented by the customary shapes:

AND OR

Each logic AND and OR in the original equation has such a shape associated with it on the circuit diagram. Inputs and outputs are drawn in customary fashion, with input lines entering from the left and outputs exiting from the right. The maximum number of inputs is governed by the particular device used to implement the logic. With two logic levels (TRUE = T and FALSE = F) and two signal voltage levels (HIGH = H and LOW = L), there are two possibilities: (1) T represented by H (with F represented by L), and (2) T represented by L (with F represented by H). The former, where T = H, is "positive logic," and the latter, where T = L, is "negative logic." The familiar positive logic convention or negative logic convention results from using one of these relationships consistently throughout a design. Only by abandoning such fixed conventions can the designer clearly represent his original logic on the circuit diagram. Conventional methods emphasize a close parallel between logic and voltage; mixed logic emphasizes the distinction between the two, eliminating the confusion that is introduced by forcing a fixed relationship between voltage and logic.

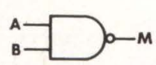
To keep track of which representation is in use at each point in the circuit diagram, a small circle is attached to any input or output that has T = L. Absence of this circle implies that the T = H convention is in use at that point. Thus, the following symbols all represent the logic AND function of two variables and are physical realizations of the same logic truth table.



Inputs		Output
T	T	T
T	F	F
F	T	F
F	F	F

Using A and B as logic input variables, and M as the output variable, each symbol represents the logic equation M = A AND B.

Each symbol defines a particular type of physical device. By recalling the meaning of the notation, one can immediately write the logic table and the voltage table for any symbol, if needed to identify the device. For example:



→

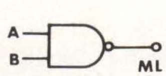
Logic A	B	M
T	T	T
T	F	F
F	T	F
F	F	F

→

Voltage A	B	M
H	H	L
H	L	H
L	H	H
L	L	H

What physical devices behave according to the voltage table? One such device is the transistor-transistor logic (TTL) 7400 integrated circuit, which is the familiar quad 2-input NAND gate chip. Here, a logic AND is implemented with a physical NAND gate.

To enhance clarity on the circuit diagram, the terminal letter "L" is appended to any logic variable name that, at a particular point on the diagram, is represented by the T = L convention. Such augmented names are always associated with the little circles; thus, the previous example is drawn in its final form:



→

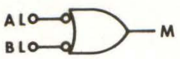
Logic A	B	M
T	T	T
T	F	F
F	T	F
F	F	F

→

Voltage A	B	ML
H	H	L
H	L	H
L	H	H
L	L	H

Note that ML is the logic variable M represented here in the form T = L. This naming convention is valuable for distinguishing the two possible realizations of a given variable, especially when signals are carried from one diagram to another.* A terminal "L" does not mean that the voltage is low, but rather than *if* the voltage is low, *then* the logic signal is true. Consider another example:

*The notation L is arbitrary; use any consistent notation. When using L, be sure *not* to allow a logic variable name to end in L.



Logic A	Logic B	Logic M		Voltage AL	Voltage BL	Voltage M
T	T	T		L	L	H
→ T	F	T	→	L	H	H
F	T	T		H	L	H
F	F	F		H	H	L

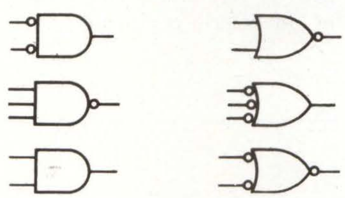
Inspection shows that this voltage table is equivalent to that in the preceding example. Thus, a logic OR has been implemented with the same NAND gate as before. Furthermore, two valid representations have been identified for this NAND gate, one which implements a logic AND and one which implements a logic OR:

Similarly, notations may be derived for other common devices to build up a catalog of circuit symbols. Some illustrations from the TTL line of chips are

7402
Quad 2-input NOR

7410
Triple 3-input NAND

7408
Quad 2-input AND

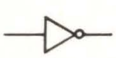


To Invert or Not to Invert

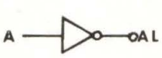
What must be done to change the logic convention for a variable, eg, what does a designer do if he needs to use a physical signal A (T = H) as input to a gate that requires AL to perform the desired logic? This circuit must behave as follows:

Logic A	A				Voltage A	AL
T	T	→	A — ? —o AL	→	H	L
F	F				L	H

Of course, this voltage table corresponds to the inverter, eg, a 7404 hex inverter in TTL. The circuit symbol is



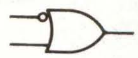
and the particular example is rendered:



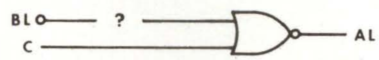
Analogous to the previous illustrations, the "inverter" device has two circuit symbols:

Note carefully that no logic change has occurred; the same logic signal is present on both sides of the inverter. The inverter performs only the identity logic operation, not a logic inversion. Its sole function is to change voltage representations for logic truth. Once again, it inverts voltage, not logic. To avoid using the dangerous term "inverter," the authors call it the "oops" function, implying that the logic signal is satisfactory, but the voltage levels must be switched.

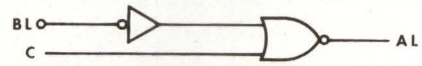
To illustrate this point, consider the logic equation A = B OR C, where B is available only as BL, C is available only as C, and A may be generated in either voltage form. For this purpose, a designer would like to use a device that corresponds to the circuit symbol



If the designer does not have such a device available, he might select a TTL 7402, containing NOR gates:

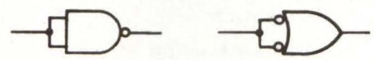


Since BL must be changed into B to perform OR logic with the 7402 gate, the designer inserts an "oops":



This circuit implements A = B OR C, and illustrates the thought process that led directly from the logic equation to a physical realization. Once again, note that the same logic variable B appears on each side of the "oops."

The inverter is of course not the only realization of an "oops." For instance, these circuit symbols are often convenient when surplus NAND gates are available:



Logic NOT

What is the physical implementation of logic NOT? For purposes of this investigation, assume that a device on the left is producing a value of a logic variable X. Also, assume that a device on the right needs for its input a logic variable Y. Logic variable X is implemented either as X or XL on the circuit diagram, and similarly Y is required as either Y or YL, depending on the nature of the devices involved. Now, connect the output of the left device to the input of the right device with a piece of copper wire, and determine what logic is performed. Since logic variables X and Y are now being physically implemented by the same voltage on the wire, there must be a close logic relationship between them. There are four mixed logic situations to consider:

Case	Copper Wire	
1	X ————	Y
2	XL o———o	YL
3	X ———o	YL
4	XL o————	Y

Mixed logic notation implies a definite relationship between voltage level and logic truth for whatever logic variables are utilized. Case 1 describes a situation in which a logic variable X on the left is physically represented by T = H, while at the other end of this same wire a logic variable Y is represented by T = H. Similarly, case 2 has both variables represented by T = L. The situations are described by:

Voltage On Wire		Case 1 Logic X	Y	Case 2 Logic XL	YL
H	→	T	T	F	F
L		F	F	T	T

In both cases, variable Y is identical in its behavior to variable X, and therefore the copper wires are representations of the logic identity operation. In other words, Y = X and no logic operation has occurred for these two cases.

Now examine cases 3 and 4 in a similar manner. By mixed logic notations, whatever variables are at the left and at the right, the representation of truth changes along the wire:

Voltage On Wire	→	Case 3 X	Logic YL	Case 4 XL	Logic Y
H		T	F	F	T
L		F	T	T	F

Inspection of each of these cases shows that logic signal Y behaves like the logical inverse of logic signal X: Y = NOT X (or Y = $\overline{X}$). In case 3, logic signal Y (ie, $\overline{X}$) is represented T = L; therefore, on the circuit diagram, $\overline{X}$L may be substituted for YL, if desired. Analogously, for case 4, NOT X ($\overline{X}$) may be substituted for Y. Therefore, the logic NOT operation occurs over a piece of wire when the designer switches the voltage convention for the representation of logic truth—a "circuitless" NOT. To guard against any tendency to wonder about an error in the circuit diagram, the authors place a slash across any line over which the logic NOT operation is to occur. In this manner, the logic NOT is clearly identified on the diagram, and shows that the logic convention has been switched. Then, the diagram for the four copper wires may be redrawn:

Case		Copper Wire		
1	X	————	X	Logic Identity
2	XL	o————o	XL	Logic Identity
3	X	——/——o	$\overline{X}$L	Logic NOT
4	XL	o——/——	$\overline{X}$	Logic NOT

The concept of a logic operation being performed without a physical device is a stumbling block for many designers, as is the collateral concept of a real device—the inverter—performing no logic operation.

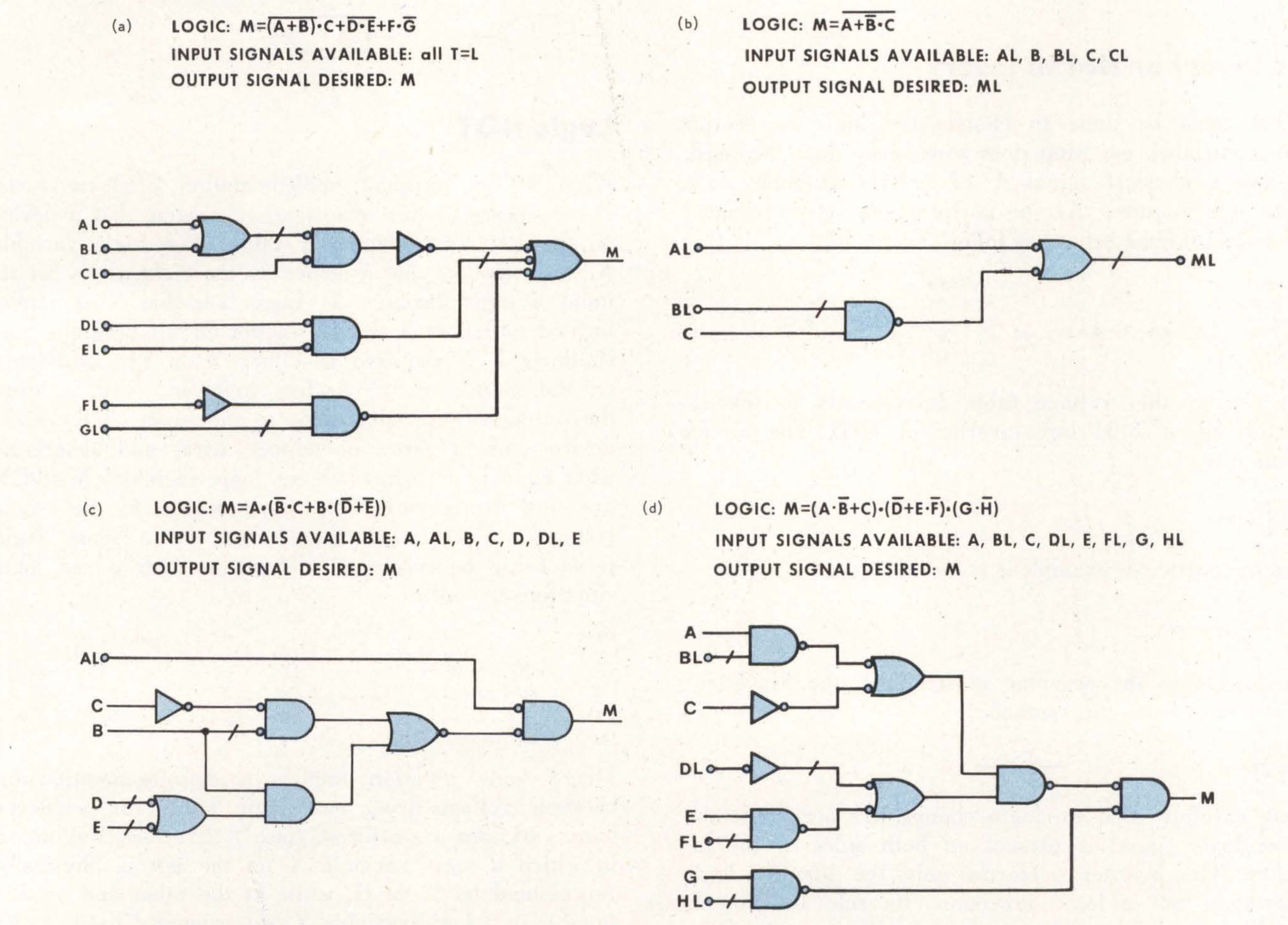
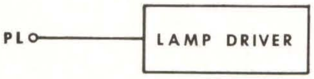


Fig 1 Mixed logic representations of typical logic equations. Assume that 2-, 3-, and 4-input NAND gates, 2-input NOR gates, 2-input AND gates, and inverters are available. Available input signals are given with each example, as is the desired polarity of the output. To read the logic from a circuit diagram, ignore circles and inverters, interpret the slash (/) as logic NOT, and read off the original logic equation

However, mixed logic circuit notation permits direct implementation of logic, and thus supports an enormous improvement in clarity and ease of design.

If the argument given previously for the logic NOT operations seems esoteric, perhaps a more physical analogy will clear up the matter. Suppose a real device—a lamp driver—lights a lamp when its input receives a high voltage. Assume that the burning lamp means "TRUTH." The lamp driver may be represented by a box with its input having no circle. Furthermore, suppose logic signal P, generated with T = L, is connected to the input:



When will the lamp light? When a high voltage is presented to the lamp driver. This requires that the logic signal NOT P be present at the input to the lamp driver. If P is TRUE, the lamp is off and the observer sees "FALSE"; if P is FALSE (ie, NOT P is TRUE), the observer sees "TRUE." Thus, the change of voltage truth convention at the ends of the wire results in a logic NOT. For completeness, a slash is drawn across the wire. Try a similar experiment with another lamp driver that gives "TRUTH" (turns on) only when presented with a low voltage level. You will reach similar conclusions as in the previous case.

Logic Equation Examples

Four examples of logic equations represented by mixed logic circuit diagrams shown in Fig 1 illustrate all the essential elements of the circuit conventions. Observe how straightforward is the analysis of a mixed logic circuit. To read the circuit, ignore inverter gates (since they perform no logic), ignore circles (since, if the slash is used to mark logic NOT, the circles themselves carry no logic), look at the logic shapes and the slashes, and read off the original logic.

Mixed logic diagrams are a boon to the maintenance engineer. An engineer troubleshooting a circuit, suspecting an error at some point in a circuit, will apply a logic probe and observe voltage levels. Working from a mixed logic circuit diagram, he can quickly understand what the designer's logic really is, and can easily observe any discrepancies found in the hardware.

Synthesis of circuit diagrams in mixed logic is straightforward, since the logic translates directly into circuit symbols. In fact, mixed logic yields maximum flexibility. At each point in the circuit, the designer uses his freedom from fixed logic polarities to select the most convenient devices and logic variable polarities, without altering the logic. Of course, if the user does not want to exercise all the available flexibility, selection of gates or logic variable polarities may be restricted.

Note that mixed logic does not control the form of the logic equation that is chosen for implementation. The designer may perform any convenient Boolean algebraic operation, knowing that the final form, whatever it is, may be easily implemented. This means that logic may be simplified, if appropriate. On the other hand, if the designer recognizes some intermediate logic terms that will be useful elsewhere in the design, he may leave those parts of the logic intact, knowing that with mixed logic, these forms will be preserved in the implementation.

With all this flexibility, what is the best procedure? Once the crucial distinction between logic and voltage is fully understood, the designer quickly develops his own techniques for transforming logic into circuits. Some may prefer to build circuits starting from the outputs; others may begin with the inputs.

Other Methods

Other choices for logic polarity—positive or negative logic convention—result in serious impediments to clear thinking. Fig 2 presents two examples taken from current textbooks on digital design. The logic problems ostensibly solved by these examples are the same ones done using mixed logic in Figs 1(c) and 1(d). Try to analyze the circuit diagrams in Fig 2 to recover the designer's original logic. You will see that the notation has quite effectively obscured what the designer originally set out to implement.

Synthesis of circuits from logic is frequently quite awkward with positive or negative logic conventions. Examination of current textbooks in digital design shows three general approaches to logic implementation: (1) DeMorgan's law is repeatedly invoked to force the logic into a format where the fixed logic forms of available gates may be identified; (2) A set of rules for manipulating gates and signal levels is offered to allow the logic equation to be implemented with NAND and NOR gates; and (3) The problem of producing circuit diagrams from logic equations is glossed over, and no practical methods for implementing logic are given.

All these approaches are quite unsatisfactory. For instance, a popular textbook advocates transforming the logic in Fig 2(a) into the following format in order to prepare the circuit diagram:

$$\overline{\bar{A} + \overline{\bar{B} \cdot C + \overline{\overline{\bar{B} + D \cdot E}}}}$$

Although the expression and its derivation are bad enough in themselves, that is not all the difficulty. The author of the above expression has in fact done an incorrect derivation, and has implemented an erroneous circuit. There are one too many bars over the term $\bar{B} + D \cdot E$. This caused Fig 2(a) to have an extra NAND gate used as an inverter. In this figure, this gate is shown with an "*." This is a powerful example of the lack of clarity inherent in many popular techniques.

Note that the version in Fig 1 requires fewer gates than the circuit in Fig 2(b). This is a common experience when mixed logic implementations are compared with others. In many cases, mixed logic results in fewer gates; in the remaining cases, the gate count is the same. Also, mixed logic often produces a solution with fewer stages of gate delay. In virtually no case do the conventional methods produce a more efficient implementation. During the implementation process, when some mental (or computer) gymnastics are in-

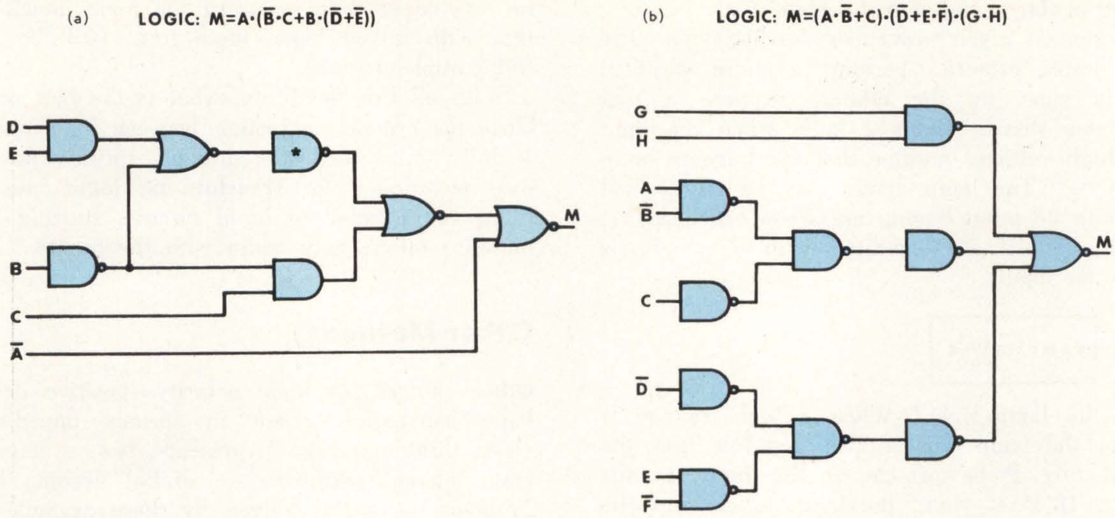


Fig 2 Conventional implementations of logic equations. These examples are taken from current textbooks on digital design. Figs 1(c) and 2(a) are implementations of the same logic, as are Figs 1(d) and 2(b). In the mixed logic versions, the design freedoms stipulated in the textbooks have not been exceeded. The gate labeled "*" in Fig 2(a) is erroneous, and resulted from the textbook author's incorrect transformation of the original logic equation using a cumbersome conventional technique

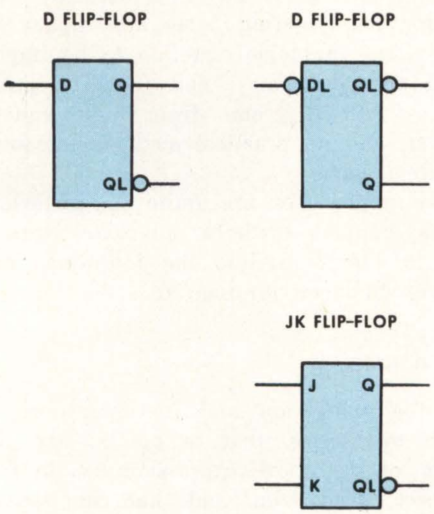
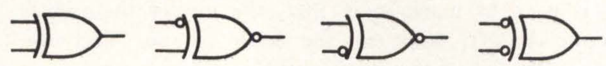


Fig 3 Mixed logic symbols for two common flip-flops. Flip-flop outputs present the same logic variable in two polarities—there is no inversion of the logic. The D flip-flop has two useful mixed logic symbols

voked to fit logic with available physical devices, the mixed logic designer is always working with his original logic equation. Conventional methods involve obscure and awkward transformations on the original logic, to the detriment of clear thinking.

Other Combinatorial and Sequential Elements

Mixed logic also assists the designer when elements other than AND, OR, and NOT are included. For instance, occasionally, the exclusive-OR (EOR or XOR) function enters into digital logic in a natural way. Mixed logic symbols for the 2-input XOR gate are:



Note that the circuit symbols all have an even number of circles. This can be verified by inspecting the logic truth table for XOR and the voltage table for an XOR gate (eg, a TTL 7486).

Logic Inputs		Logic Output
T	T	F
T	F	T
F	T	T
F	F	F

Voltage Inputs		Voltage Output
H	H	L
H	L	H
L	H	H
L	L	L

Four voltage assignments for truth will bring the logic into conformity with the voltage table. For logic inputs A and B, and output M, physical realizations are A XOR B = M, AL XOR B = ML, A XOR BL = ML, and AL XOR BL = M.

Mixed logic circuit symbols for two common flip-flops are shown in Fig 3. The crucial point is that the outputs represent a logic signal (B in this case) that is available in two logic polarities. The "inverting" output of each flip-flop is not inverting the logic, but is just providing a voltage level inversion. It is performing an "oops." The D flip-flop, performing simply a delay or holding action on its input, profitably has two mixed logic representations. Use the one appropriate to the logic polarity for the incoming signal.

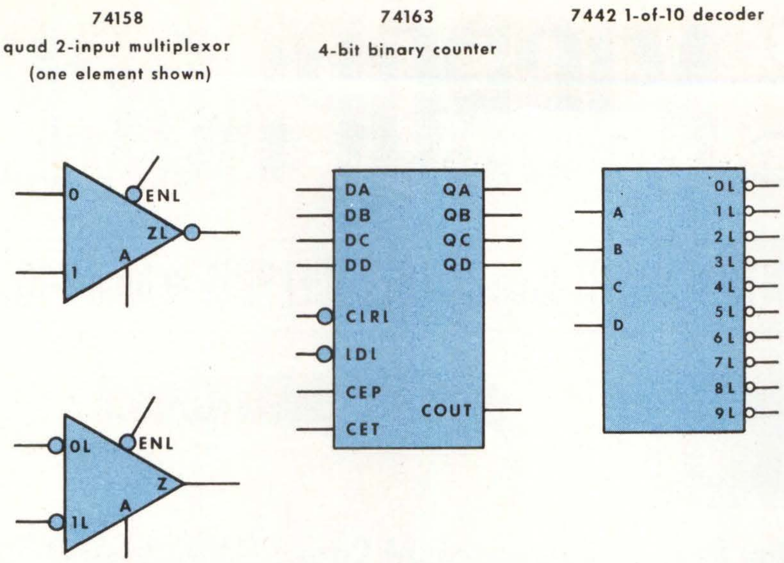


Fig 4 Mixed logic symbols for some TTL integrated circuits. Low-active inputs and outputs have circles. The multiplexer has two useful symbols

Medium-scale integrated (MSI) building blocks have their mixed logic circuit symbols. Fig 4 shows symbols for several common TTL chips. With these models, the appropriate symbols for any MSI or LSI (large-scale integrated) circuit can be derived. Low active inputs and outputs have a circle.

Some additional thoughts: many manufacturers and engineers use the logic inversion notation on their designations for low active control inputs. For example, designation $\overline{LD}$ might be used for the load input to the binary counter in Fig 4. When such a chip is used, the designer almost always desires to provide the chip with a logic signal to load, (with T = L, and perhaps called LOADL). The $\overline{LD}$ notation encourages the thought that the input is a *not load* signal. Surely it is not often desirable to think of the load control input as a "don't load."

Summary

In practice, mixed logic has proven to be a superb aid to clarity, both in the design process and during maintenance of existing circuits. Some engineers have said that mixed logic is too difficult (even confusing) for designers and maintenance personnel; the authors have found the opposite to be true. While there is a necessary period of familiarization and learning, as with any new design simplification tool, mixed logic allows the designer to concentrate on his logic, while preserving all the necessary information about the physical implementation. Since logic-voltage relationships are incorporated rigorously into the notation, the designer expends no wasted energy on the subject of voltage—his notation handles it automatically. The result is a circuit diagram that displays the original intent clearly, and significantly eases the tasks of maintenance and modification of the hardware.

Gates are cheap; clear, correct designs are rare. Some years ago, when the authors established their goal of improving the understandability of hardware designs, they thought that by emphasizing clarity, hardware efficiency would be lost. The opposite has proven to be true. In most cases, the mixed logic style led not only to clearer designs, but also to ones requiring less hardware. Experienced, as well as new, designers are encouraged to investigate these elements of design style. Most will find that an emphasis on clarity results in superior designs.

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Franklin Prosser received his PhD degree from Pennsylvania State University. Currently chairman of the Computer Science Dept at Indiana University, he has worked on computer software systems and digital hardware, with emphasis on operating systems, computer design, and interfacing.

David Winkel, professor of computer science at the University of Wyoming, is currently on leave at Indiana University, where he is continuing his work on methods of teaching digital hardware. He received his PhD degree from Iowa State University, and is president of Logic Design, Inc.

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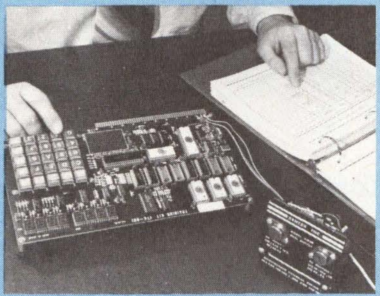

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CIRCLE 113 ON INQUIRY CARD

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MICROPROCESSOR/MICROCOMPUTER APPLICATIONS CONTEST WINNER

Second Prize

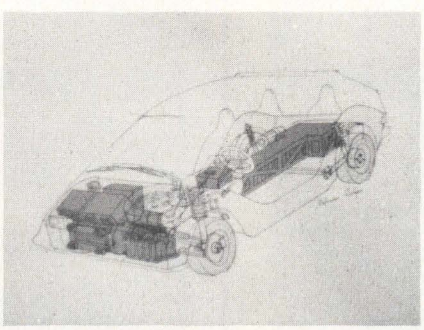
A Microprocessor-Controlled Three-Phase Power Inverter

Peter van der Gracht and Konrad Mauch

UBC Electric Vehicle Project
University of British Columbia
Vancouver, British Columbia, Canada

With potential applications foreseen in transit and rail vehicles and variable speed industrial devices, a technique of using a microprocessor to control the input to a three-phase induction motor provides flexible control of the drive system of an electric car

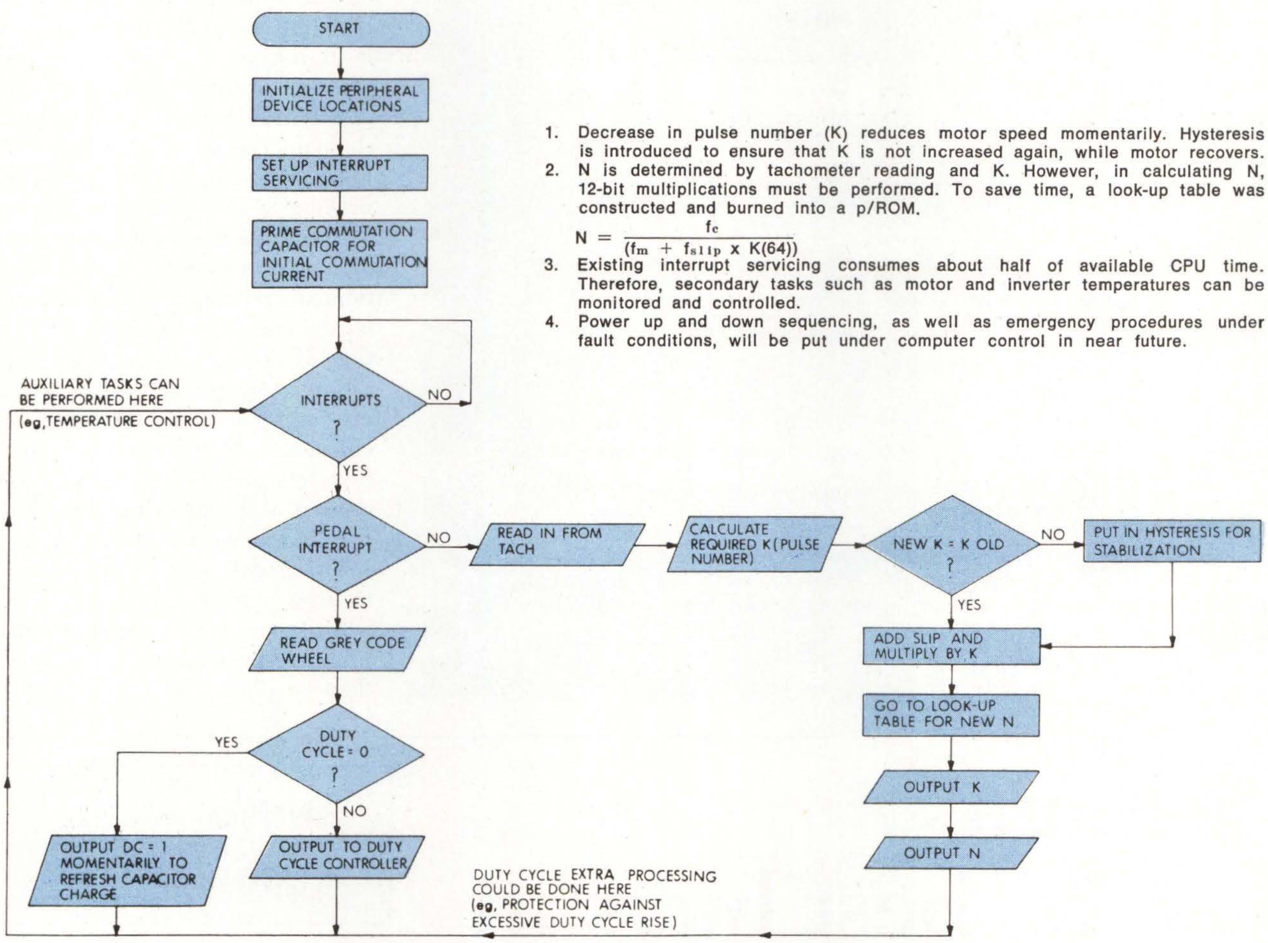
An Intel MCS 80 board containing an 8080 microprocessor with 256 x 8 RAM and 3k x 8 p/ROM is used to control a three-phase induction motor in an electric vehicle designed and built by a group of undergraduates at the University of British Columbia, Vancouver, Canada. The dc battery voltage is converted to three-phase variable-frequency ac voltage by an SCR (silicon controlled rectifier) inverter whose firing is controlled by the microprocessor.



Artist's skeletal view of electric car containing microprocessor-controlled 3-phase induction motor shows major vehicle components

Basic control scheme is the constant-slip frequency-constant horsepower mode described in "The GM High Performance Induction Motor Drive System," P. D. Agarwal, *IEEE Transactions on Power Apparatus and Systems,* Feb 1969. The microprocessor controls the input frequency to the motor (maintaining a constant slip frequency), the voltage (by pulse-width modulation), and the harmonic content of the waveform (by varying the number of pulses per cycle). The system is in operation and the vehicle is presently undergoing performance tests.

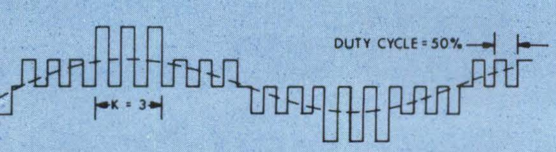
Flowchart



1. Decrease in pulse number (K) reduces motor speed momentarily. Hysteresis is introduced to ensure that K is not increased again, while motor recovers.
2. N is determined by tachometer reading and K. However, in calculating N, 12-bit multiplications must be performed. To save time, a look-up table was constructed and burned into a p/ROM.

$$N = \frac{f_c}{(f_m + f_{slip} \times K(64))}$$

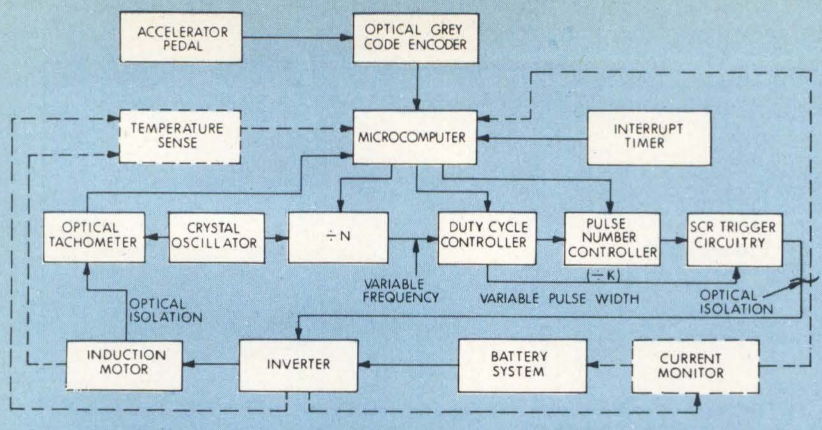
3. Existing interrupt servicing consumes about half of available CPU time. Therefore, secondary tasks such as motor and inverter temperatures can be monitored and controlled.
4. Power up and down sequencing, as well as emergency procedures under fault conditions, will be put under computer control in near future.



Idealized waveform shows one phase for pulse number equal to three and duty cycle equal to 50%

The driver uses the accelerator as in a conventional automobile. The accelerator is linked to a 6-bit grey code encoder that sends a signal to the microprocessor. The microprocessor determines the pulse width and thus the output voltage from this signal. Inverter frequency is determined automatically. A shaft encoder on the motor output shaft acts as a digital tachometer. The microprocessor reads the tachometer period and through a look-up table determines the inverter frequency required (inverter frequency = shaft frequency + slip frequency). In operation, the motor speeds up until the power of the motor is completely used up by drag forces. To speed up further, the driver must depress the accelerator further.

This is the set-up as it stands. Currently under construction is a



Notes:

1. Programmable ÷N counter generates controllable variable frequency source,
   $f_v = \frac{f_c}{N}$
2. Duty-cycle controller outputs 64 possible pulse widths dependent on grey code encoder position.
3. Output of ÷K counter signals inverter to start next step of 6-sep waveform, hence K pulses/step result, or pulse number = K.
4. Final frequency supplied to stator is given by
   $f_m = \frac{f_c}{N+K+64}$
   Hence, motor frequency (f_m) is
   $f_m = \frac{f_c}{N+K+64} - f_{slip}$
5. SCR trigger circuitry fires SCRs on rising edges and initializes commutation on falling edges.
6. Commutation capacitor charge is refreshed after each commutation, however initial charge must be supplied by software.

Diagram shows control system—the constant-slip frequency-constant horsepower mode—of a 3-phase induction motor incorporated in an electric car. Solid lines indicate sections which have already been built; dotted lines indicate those under construction

temperature sensing system that will interrupt the microprocessor and cause it to reduce power when the inverter or motor temperature is too high. Also, a crowbar protection circuit is being built that will interrupt the microprocessor and cause it to initiate a shutdown procedure when an inverter fault occurs. Future possibilities under consideration include microprocessor control of transmission shifting and regenerative braking to extend vehicle range.

Three main advantages to the use of a microprocessor in this application are reduction in the amount of hardwired logic required, elimination of complex mechanical slip addition systems, and easy variation of control parameters by software changes. Microprocessor-controlled inverters also have potential applications in transit and rail vehicles and variable speed industrial drives. The software definition of drive characteristics and the ease of interface with supervisory control computers present particular advantages in these applications. □

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CIRCLE 77 ON INQUIRY CARD

TECH NOTE

An Algorithm for Nonrestoring Division

S. Sanyal

Tata Institute of Fundamental Research
Bombay, India

Highly theoretical accounts of division processes need not hinder designers, who can organize hardware, firmware, or software controls around this algorithm

Designers faced with the task of finding an algorithm for division may discover that much published material consists of lengthy theoretical discussions with little practical or easily understandable information. Thus system programmers writing division routines and system designers working out firmware sequences face a common dilemma. A possible solution is found with an algorithm for dividing a 2-word dividend by a 1-word divisor and producing a 1-word quotient and a 1-word remainder with the same sign as the dividend. It represents numbers in signed 2's-complement notation.

Division is equivalent to repeated subtraction of the divisor from the dividend until the quantity left is smaller in magnitude than the divisor. The number of subtractions is the quotient, and the quantity left is the remainder.

This process, if done straightforwardly, is very time consuming. It is substantially speeded if the most significant digits of the divisor and dividend are aligned before the first subtraction, and the divisor then shifted to the right one position whenever the partial remainder becomes smaller than the divisor before shifting. One shift may be necessary before any subtraction, if the initial alignment makes the divisor larger than the dividend. In binary, at most one subtraction can be made between shifts except as noted below.

Two conventional techniques avoid the need to compare the remainder with the divisor after every subtraction. In restoring division, subtraction continues until the sign of the partial remainder changes; the change causes an immediate addition

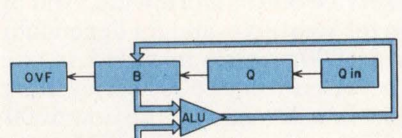


Fig 1 Registers for division. Gate Q_{in} generates quotient, bit by bit, as OVF flag gets old bits of dividend shifted out of B. Initially dividend is in B and Q, and divisor in A; at the end B contains the remainder and Q the quotient

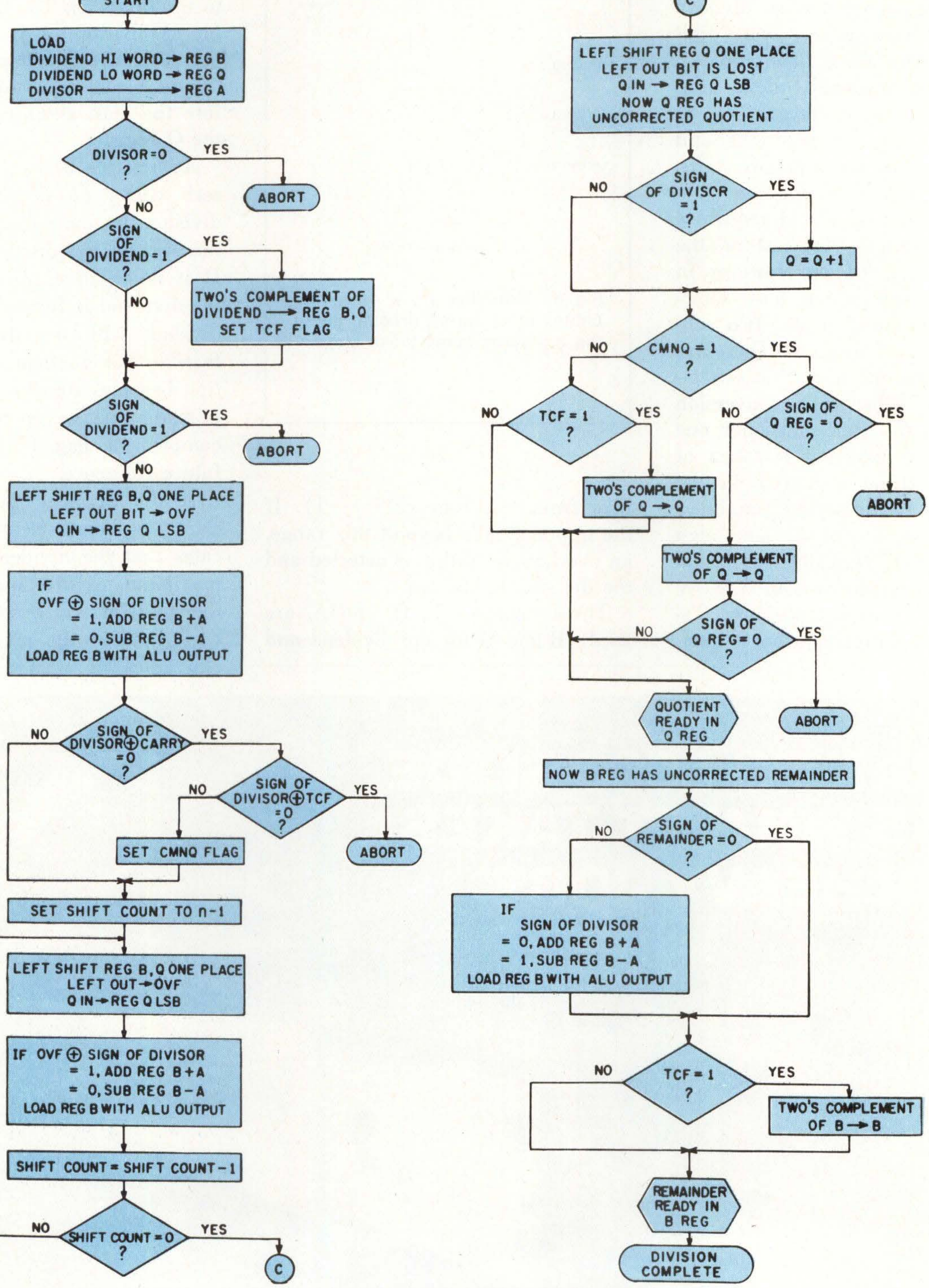


Fig 2 Division algorithm. A 1-word divisor of n bits divides a 2-word (2n-bit) dividend, producing a 1-word quotient and a 1-word remainder. All quotient overflow cases are detected

of the divisor and a corresponding decrement of the accumulating quotient, before the right shift. In nonrestoring division, the sign change causes a shift followed by one or more additions until the sign changes back.

In general, nonrestoring division has the disadvantage that every digit of the quotient must have its own sign and that successive digits have alternating signs, corresponding to alternating series of additions and subtractions between successive shifts. This is equivalent to notation in a negative radix, and would require a conversion routine to restore the quotient to normal form. However, in binary, one subtraction may sometimes change the sign and two subtractions always change it. Therefore in this scheme the operation is simplified, and subsequent conversion avoided, by the rule that only one subtraction or addition is taken at each step, setting a 1 (0) in the quotient if both the partial remainder and the divisor are of the same sign (opposite sign), regardless of which arithmetic operation was used.*

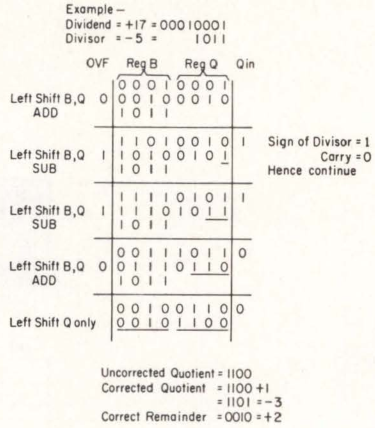


Fig 3 Example. In a 4-bit machine, nonrestoring division under the algorithm takes these steps

With n-bit words, the signed 2's-complement notation represents numbers from -2^{n-1} to $(2^{n-1} - 1)$. If the quotient falls beyond this range, an overflow condition is detected and the division is aborted.

Three registers, B, Q, and A, are used—B and Q for the dividend and A for the divisor (Fig 1). A gate Q_{in} forms the exclusive-NOR of the divisor sign and the arithmetic-logic unit (ALU) output sign. The dividend in B and Q shifts one position to the left, which is equivalent to the right shift of the divisor with respect to the dividend. The most significant bit (MSB) of the B register moves out to the overflow flag (OVF), while the quotient formed by Q_{in} is pushed into the least significant position of the Q register.

At first the divisor is checked for zero value, on detection of which division is aborted (Fig 2). Next, the sign of the dividend is checked. If it is negative, 2's-complement of the dividend is formed. Nonrestoring division with negative dividend is feasible but quotient overflow detection becomes simpler if the dividend is made positive. In this case, a 2's-complement flag (TCF) is set for future reference.

If the dividend is still negative after 2's complementation, it indicates that the dividend is a 2-word maximum negative number and that the quotient will definitely overflow, regardless of the magnitude of the divisor. This prospective overflow aborts the algorithm.

If these initial hurdles are cleared, the first step of division begins. When the dividend shifts left, its MSB goes into the OVF flag. If OVF and the sign of the divisor are the same, the divisor is subtracted from the most significant part of the dividend; if they differ, the divisor is added. The partial remainder replaces the minuend.

In this step, quotient overflow is again anticipated by the carry output of the ALU. If the carry bit is opposite to the divisor sign, no quotient overflow is anticipated and division is continued. (During subtraction, carry out of the ALU is actually a borrow, the complement of the real carry.)

When the carry and divisor sign are the same, there are two possibilities. If the original dividend sign, recorded in TCF, is the same as the divisor sign, the quotient is certain to overflow; hence division is aborted. If the original dividend sign is opposite to that of the divisor, a maximum negative quotient is expected, and a flag called Check for Maximum Negative Quotient, or CMNQ, is set.

Now the preparatory steps are complete, and the division process proper can begin. This requires a series of steps tallied by a shift counter (not shown in the figure). For a word length of n bits, the shift counter is loaded with $n - 1$. Then the dividend shifts left one place and the divisor is subtracted or added, according to the OVF and divisor sign as before. These steps are repeated, decrementing the shift counter each time, until the latter reaches 0. When that happens, the Q register only is shifted to the left once more, to bring in the uncorrected quotient.

The divisor, if negative, produces a negative quotient, because the dividend is known to be positive, following the complement formation (second step of the algorithm). A negative quotient is in 1's-complement form, and must be corrected by adding 1 to transform it to 2's-complement form. After this stage, if the CMNQ is set, the quotient is checked to see whether it is maximum negative. If not, division is aborted.

If the CMNQ is not set, the quotient is ready. If the TCF has been set, the correct quotient is the 2's complement of Q.

Now the B register has the uncorrected remainder. Because the dividend is positive, if the uncorrected remainder is negative, a correction is needed. To make the remainder positive, the divisor is added to or subtracted from it, depending on whether the divisor is positive or negative. If the original dividend is negative (TCF = 1), the corrected remainder is 2's-complemented. This completes the division. Fig 3 is an example of nonrestoring division of a 2-word dividend by a 1-word divisor.

Conclusion

This algorithm was simulated and thoroughly tested on a CDC 3600 computer. In a microprogrammed minicomputer with a divide instruction, the algorithm can be stored in the control memory, thus saving a lot of hardware. The algorithm can also be used for writing a division routine in software. □

*H. W. Gschwind, *Design of Digital Computers*, Springer-Verlag, New York, 1967, pp 226-228

TECH NOTE

Competent Purchase Specifications Help Assure Successful Product

David M. Hamblen

Inforex, Incorporated
Burlington, Massachusetts

Adequate purchase specifications are a necessary part of the documentation for engineering projects; they have appropriate goals and aims, and can be made up in accordance with rules that enhance adequacy

Specification control drawing, or the drawing up of a purchase specification, is a part of most engineers' regular tasks. It will fail its purpose (and adversely affect the engineer's performance) if it is inaccurate, ambiguous, incomplete, or unclear in intent or meaning. Attention to details when building a purchase specification brings recognition to an engineer as one who cares about the quality of his work.

Completeness

A purchase specification defines the necessary characteristics of a part or assembly to be purchased from a vendor. It must include enough information to define unambiguously the necessary characteristics of the device which will qualify it for inclusion in the next higher assembly. Small or simple parts may need only a single A-size (8½ x 11", 27.6 x 27.9 cm) sheet, with pictorial views, dimensions, and notes concerning material characteristics and other miscellaneous data. Such specifications are hard to make improperly or inadequately. On the other hand, larger and more complex assemblies and equipment require multiple pages of text and figures, and require more care in their preparation.

The bare statement "XYZ company model T" is not enough. All characteristics that are necessary to the application should be explicitly mentioned. If an industry standard (ANSI, JEDEC, or the like) exists and is applicable, by all means refer to it; but it need not be reproduced in the specification. Reference to company drawings, on the other hand, should include a copy or reproduction if possible. If it is larger than the sheets used for the specification, perhaps it can be photo-reduced to the proper size, or only the section of interest included.

Terminology

The same term, noun and descriptors, should be used in every reference to a particular object. Conversely, the same term should not refer to more than one thing. This seems elementary, but many times suppliers, purchasing agents, and other engineers have been puzzled and confused when trying to interpret someone else's terminology. If the subject is novel or if some terms are used in a special sense, it is a good idea to include a glossary.

Requirement Categories

This list may be helpful, but not all will be applicable for every specification.

1. Primary power-line voltages, frequencies, currents, maximum demand, line cord length, and connector.
2. Controls, indicators, interlocks.
3. Signal interface—physical connector, pin/signal assignments, signal definitions, signal levels, loading, electrical noise.
4. Reliability and life—MTBF and MTTR, product life, error rates.
5. Environmental limits—operational environment, transportation environment.
6. Configuration control—serialization of units and assemblies, notification of design changes, engineering change and revision levels, notification of effective dates of changes.
7. Options—special features or requirements, cabinetry, color, logotype, terminations or interface, power supply. Even if they appear elsewhere in the performance paragraphs, optional items should be collected into one convenient paragraph.

Statements that are contractual requirements must be distinguished from those that are only descriptive or ancillary. Use of "shall" with the third person is emphatic and has the force of a requirement, whereas "will," "is," or "has" is merely descriptive. Furthermore, an analog numerical dimension or quantity without a tolerance range has no contractual force. (See panel for examples of Requisite and Descriptive Statements.) Both requisite and descriptive clauses have their place in a specification—the requirement describes the necessary parameters, and descriptive material broadens and enhances understanding.

Readers of purchase specifications can be assumed to be technically oriented with a specialized knowledge of the kind of equipment being specified and its applications.

Specific Content and Form

Most companies make available an A-size sheet, printed with a format that has been specifically designated for use in drawing up purchase specifications. Quite often, these formats are for single-sheet drawings, or the first sheet of multiple-sheet drawings, of which continuation sheets are plain.

At any rate, information on this first sheet should include a list of approved sources, and a listing, usually in tabular form, of the manufacturers' model designations. Specifications of large or complex equipment require multiple continuation sheets of text and figures. They should include several general categories of information, including:

Scope of purpose: brief description of the device, and a list of the subjects that the specification covers. This list may be expanded into a table of contents.

References: any documents that apply to the device being specified. Reference to such other documents is not a necessity in a specification, but it is one way to promote better understanding through a more complete explanation. Use of industry standards here is encouraged. If vendor documentation is referred to, it should be introduced with a statement to this effect: "To the extent mentioned herein, the following documents form a part of this specification. If conflict is found between this specification and the reference documents, this specification shall govern."

Requirements: list of parameters necessary to the performance of the device in the intended application. All parameters, and only those parameters, necessary to the performance should be included. (See Requirement Categories listing.)

Engineers should be especially wary of the double specification, which specifies "how to make it" and "what it must do" simultaneously. The "how" and "what" may be self-contradictory, or may be interpreted as such by the vendor. An example is a keyboard specification which calls for a mechanical crossbar switch and requires a maximum bounce time of 500 μs. The vendor may well honor the one and ignore the other—and it is his choice!

All purchase specifications are formal drawings, to which a permanent number should be assigned. They should be released for use in the same way as any engineering drawing, through the company's standard procedure. Similarly, revisions to a purchase specification, after it has been released, should be made only through formal channels for engineering changes.

Summary

The purchase specification, which tells a purchasing agent how to buy a part, assembly, or equipment, is as important a part of a set of engineering drawings as the assembly drawings and parts lists. It deserves an equivalent share of an engineer's professional attention as part of his output, the quality of which is constantly being judged by his management. □

Requisite and Descriptive Statements

Some examples of requisite clauses

1. Output voltage shall be between 10.0 and 12.0 Vdc under the conditions . . . .
2. Material: aluminum alloy 5052-H38.
3. The pack is required to be dynamically balanced within ±4.0 inch-grams.

Some examples of a descriptive nature

1. Each servo track has an index pattern encoded on it.
2. The weight of the unit is 136 pounds.
3. PCB size is 6 by 9 inches.

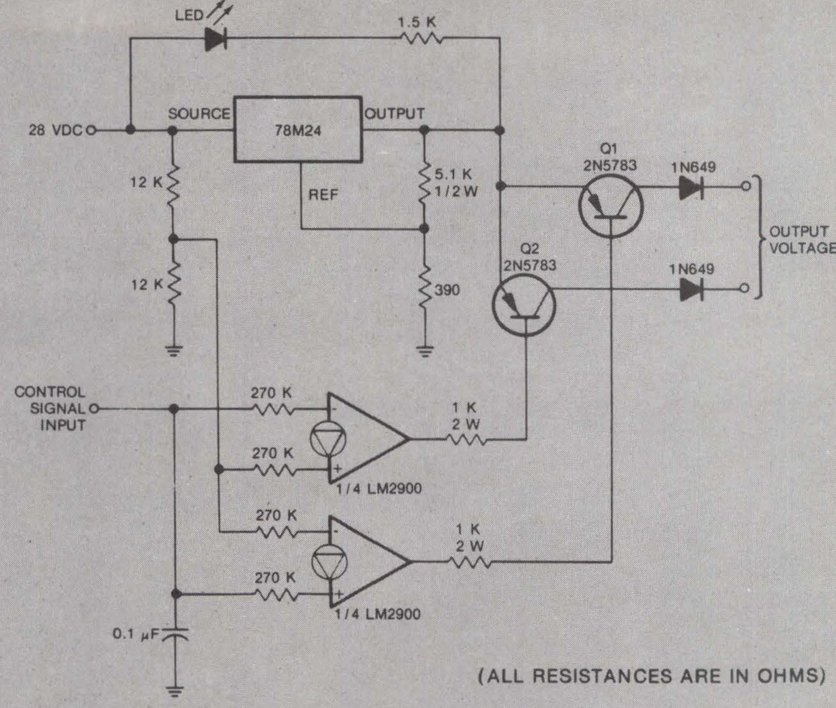
TECH BRIEF

Overload-Protector/Fault-Indicator Circuit

Power driver circuits are protected by a current limiter with status lights

In large installations, status indication circuits may be located far from the equipment being monitored. The power source energizing the status circuits, which are often comprised of power-transistor-driven incandescent indicators, is adversely affected by initially-high surge currents when the lamps are first triggered on. Interconnecting cables and their associated connectors also impose large momentary fault current conditions on the power supply if the cables, upon removal from the connector, are accidentally short circuited while troubleshooting.

To overcome the effects of the current surges a 3-terminal current limiter is incorporated in the power supply to increase its overload current protection. The IC limiter (component 78M24 in the schematic) has a maximum peak current passthrough of approximately 2 A; the limiter provides about 500 mA under steady-state conditions. Since the limiter is internally protected by built-in thermal shutdown, it is not mounted with a heat sink and is therefore self-protecting. Status indicators are sourced from a 28.0-V supply, but the limiter maximum voltage output is 24 V. The reference terminal is biased slightly above ground to permit the limiter to operate at the output voltage requirement.



Overload-protector/fault-indicator circuit incorporates 3-terminal current limiter (78M24) to increase overall reliability, by eliminating transistor burnouts resulting from shorted interconnection lines and other overloads. Fast acting LEDs across limiters show status of transistor output circuits

When the regulator is overloaded, it reduces the output voltage to a safe value via internal current limiting. Output voltage reduction increases the voltage differential across the limiter source/output terminals. The LEDs connected across the terminals turn on, thus indicating a fault in the circuit being powered. After the fault is corrected the circuit returns to normal operation, and the LED is extinguished.

A separate current-control signal from the monitored circuit also can be used to turn off the power supply. The signal is fed to a pair of operational amplifiers, which are connected for complementary output current required by the circuits being powered. The amplifiers, type LM-2900 or equivalent, do not have closed-loop feedback to control gain. This provides full open-loop gain to drive the output transistors Q_1 and Q_2. The 1N649 diodes, in series with each of the transistor collector terminals, are used to prevent high transient currents (resulting from driving inductive loads) from destroying the output transistors. The diodes also protect the circuit if it is connected to a source which is higher than 28 V.

Note

This work was done by John R. Paluka of Caltech/JPL and Stephen F. Moore of Resdel Engineering Corp. For further information, write to: John C. Drane, Technical Utilization Officer, NASA Resident Legal Office-JPL, 4800 Oak Grove Dr, Pasadena, CA 91103. (NPO-13592).

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Dual Processor Support	YES	YES
Interface to Most 3330 Technology Drives	YES	NO

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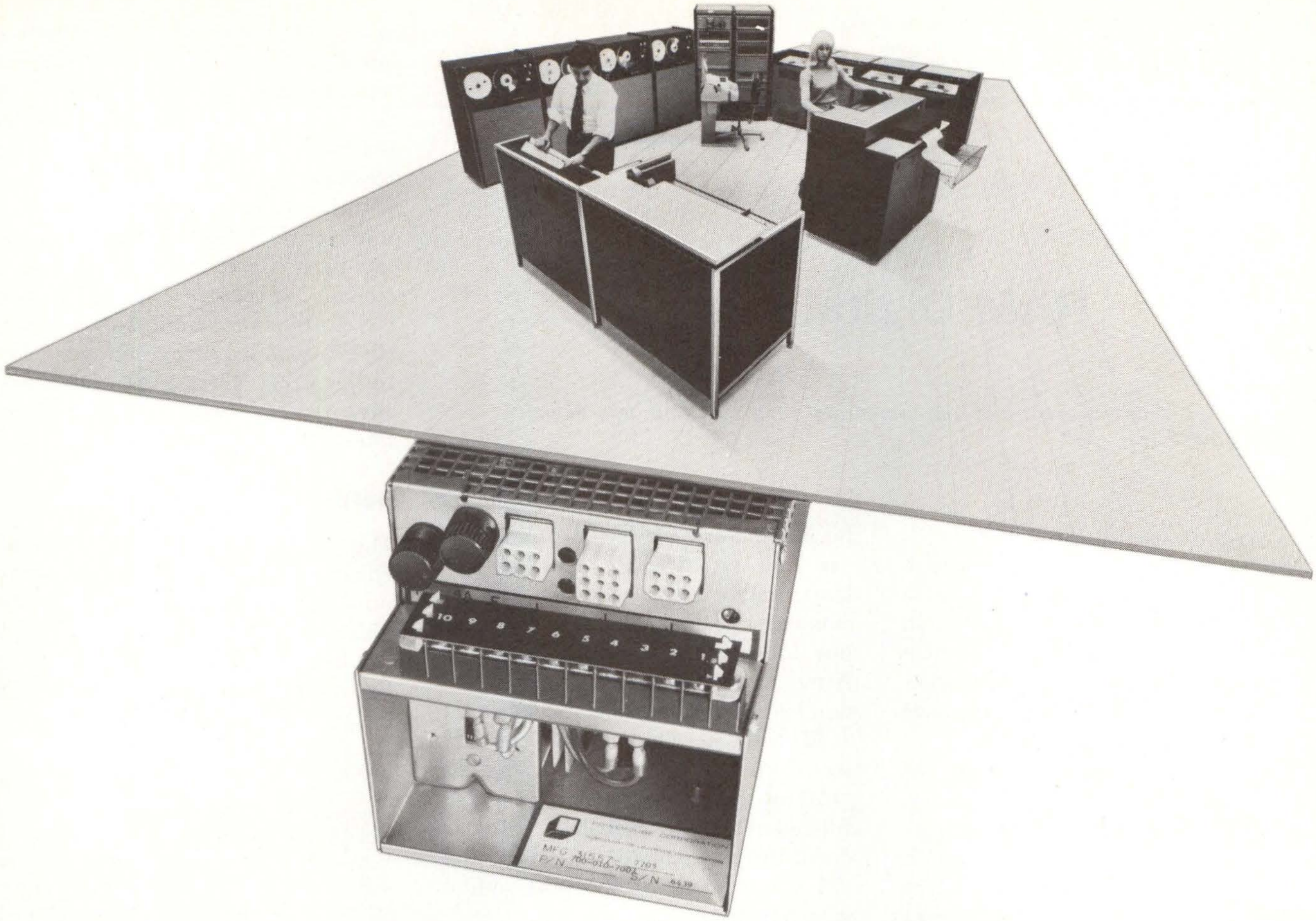

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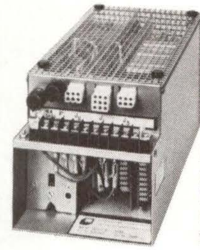

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TECH BRIEF

RAM Digital Filter

A sophisticated means of implementing recursive and nonrecursive digital filters

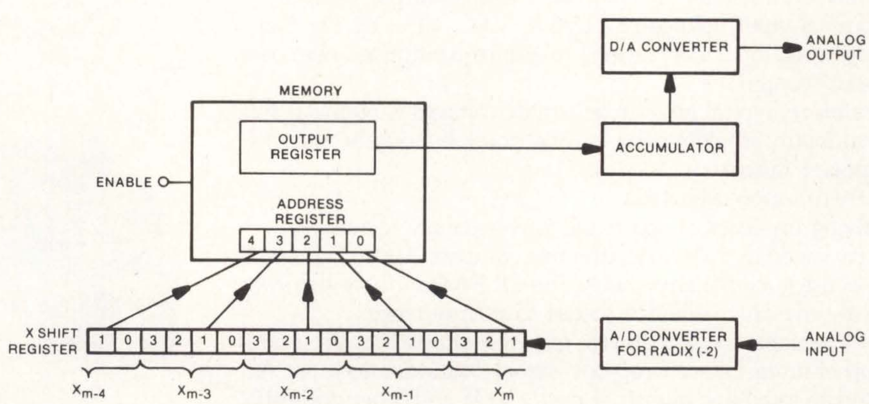
A newly proposed digital filter is designed to store all possible combinations of filter coefficients in a RAM. The filter has a very high speed and hence high cutoff frequencies. Based on this design, low order (seven or less) filters can be made at reduced cost.

The filter as shown includes an ADC, an X shift register, a memory, an accumulator, and a DAC. In operation the analog input signal is sampled. Samples are converted to their representation in radix (−2) and are serially fed to the X shift register which generates a memory address as shown. With each new bit a new word is selected from memory and is added to the accumulator. Following the addition, the accumulator contents are shifted left one bit and their sign is reversed. After J such cycles [J being the number of bits per sample in radix (−2)], the accumulator contents are transferred to a standard (radix 2) DAC which yields the sample of the filtered function (analog output). Next, the accumulator is zeroed, and the construction of the next output sample starts.

The described configuration is a nonrecursive RAM digital filter. It should be noted, however, that the same basic shift register structure can also be applied to the recursive case. Feature of the RAM filter is that it achieves its speed by totally eliminating any computing to get the accumulator inputs. Closely related counting filters are characterized by a longer I/O delay because the accumulator inputs are computed in a pipeline structure. The RAM filter therefore has a definite advantage in applications requiring minimal delay. In low order filters it also has a cost advantage over equal speed counting filters.

Note

This work was done by Shalhav Zohar of Caltech/JPL. For further information, write to John C. Drane, Technology Utilization Officer, NASA Resident Legal Office-JPL, 4800 Oak Grove Dr, Pasadena, CA 91103. Refer to NPO-13659.



This nonrecursive RAM digital filter is a modification of a conventional digital counting filter. The register holding the filter coefficient in the digital counting filter is replaced with a much larger RAM that stores all possible combinations of the coefficients; however, counter and gates required there are eliminated in the RAM implementation

MICRO PROCESSOR COMPUTER DATA STACK

Microcomputer Interfacing: The 8080 Logical Instructions

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Last month the concept of, and one important use for, multibit logical instructions such as AND, OR, exclusive-OR, and complement were discussed. This month we will summarize 28 logical instructions in the 8080A instruction set. It is very important to note that in the case of each logical instruction, the result is stored in the accumulator. The previous contents of the accumulator are one of the logical variables in the 2-variable logical operation, or in the case of the complement instruction, the only logical variable.

Eight different logical AND instructions, each with the mnemonic ANA S, have the general form of

1 0	1 0 0	s s s
Arithmetic and logical class of instructions	AND operation	3-bit binary code for source register

where sss are the three bits that correspond to the register or contents of a memory location that logically operate on the accumulator contents,

Register	Octal Code	3-Bit Register Code
B	0	000
C	1	001
D	2	010
E	3	011
H	4	100
L	5	101
M	6	110
A	7	111

The OR and exclusive-OR instructions, which have the mnemonics ORA S and XRA S, respectively, have the same general form as the ANA S instruction byte. Thus, for the XRA S instruction, the instruction byte is

1 0	1 0 1	s s s
Arithmetic and logical class of instructions	Exclusive-OR operation	3-bit binary code for source register

and for the ORA S instruction

1 0	1 1 0	s s s
Arithmetic and logical class of instructions	OR operation	3-bit binary code for source register

Some examples of these logical instructions include:

Logical Operation	Mnemonic	Octal Instruction Code
$B \cdot A \rightarrow A$	ANA B	240
$M \cdot A \rightarrow A$	ANA M	246
$A \cdot A \rightarrow A$	ANA A	247
$C \oplus A \rightarrow A$	XRA C	251
$L \oplus A \rightarrow A$	XRA L	255
$A \oplus A \rightarrow A$	XRA A	257
$D + A \rightarrow A$	ORA D	262
$E + A \rightarrow A$	ORA E	263
$M + A \rightarrow A$	ORA M	266
$A + A \rightarrow A$	ORA A	267

Another logical instruction is the complement accumulator instruction, which has the mnemonic CMA A and the octal instruction byte 057.

In preceding columns,[1,2] we discussed the concept of an *immediate instruction,* a multibyte instruction that contains the desired data within the instruction. The three immediate logical operations can be summarized as

Logical Operation	Mnemonic	Octal Instruction Code
$<B2> \cdot A \rightarrow A$	ANI <B2>	346 <B2>
$<B2> \oplus A \rightarrow A$	XRI <B2>	356 <B2>
$<B2> + A \rightarrow A$	ORI <B2>	366 <B2>

In the two tables, the symbol ($\rightarrow$) signifies "is replaced by." Thus, the notation $B \cdot A \rightarrow A$ means AND variable B with variable A, and then replace the original contents of A with the result of the logical operation. Within the 8080A microprocessor chip, the logical operation is performed in a temporary accumulator, with the logical result in the temporary accumulator being copied into the accumulator register A.

In last month's column one use demonstrated for logical instructions was the testing of flag or comparator bits associated with the on/off state of external devices. The AND multibit operation is particularly useful to clear, filter, or mask specific bits in an input data byte. For example, consider the ASCII code for the numeric characters 0 through 9:

Program Listing to Mask Specific Bits

LO Memory Address	Octal Instruction Code	Mnemonic	Comments
000	333	IN	Input ASCII numbers from the following device
001	015	015	Device 015
002	346	ANI	AND the accumulator contents with the following data byte
003	017	017	Mask byte that "masks" the four MSBs in the ASCII word
•	•		
•	•		
•	•		

Program to Pack BCD Digits

LO Memory Address	Octal Instruction Code	Mnemonic	Comments
000	333	IN	Input ASCII "5" from the following device
001	015	015	Device 015
002	346	ANI	Mask off the four MSBs
003	017	017	Mask byte
004	007	RLC	Rotate the BCD digit into the four MSBs that have just been cleared
005	007	RLC	
006	007	RLC	
007	007	RLC	
010	107	MOV B,A	Store this result in register B
011	333	IN	Input next ASCII character (in this case ASCII "7") from the following device
012	015	015	Device 015
013	346	ANI	Mask off the four MSBs
014	017	017	Mask byte
015	260	ORA B	OR contents of register B with contents of accumulator
016	167	MOV M,A	Store packed data into memory, the location being specified by the contents of the H,L register pair
•	•		
•	•		
•	•		

Character	Octal ASCII Code	Binary ASCII Code
0	260	10 110 000
1	261	10 110 001
2	262	10 110 010
3	263	10 110 011
4	264	10 110 100
5	265	10 110 101
6	266	10 110 110
7	267	10 110 111
8	270	10 111 000
9	271	10 111 001

Once the ASCII code is input into the microcomputer, the four most significant bits (MSB) are of little use and can be "stripped" away from the data byte. A simple program that accomplishes such a task is contained in the Listing. This program accomplishes the following Boolean operation for ASCII "5"

10110101 •	00001111 =	00000101
ASCII "5"	Mask byte	BCD data of interest

The logical result of the AND operation is 00000101. There now is a single BCD digit per input data byte, with the BCD digit being the four least significant bits (LSB) in the byte, D3 to D0. The remaining four bits, D7 to D4, can be used to store another BCD digit provided there is some way to position this second digit in these open bit positions. If these four bits of storage space are not taken advantage of, 50% of the memory storage space would be wasted.

To "pack" two BCD digits into a single data byte, we must have the capability to rotate the contents of the accumulator. The rotate left instruction is used, which has the mnemonic RLC, the octal instruction byte 007, and can be described as follows: "The content of the accumulator is rotated left one position. The low order bit and the carry flag are both set to the value shifted out of the high order bit position."[3] The four rotate instructions in the 8080 instruction set have been shown previously.[4] The accumulator is the only register that can be rotated in an 8080A chip. Other registers are rotated simply by moving them to the accumulator register, performing the necessary rotation operations, and returning the rotated byte back to the original register. Besides shifting BCD digits back and forth in data bytes, other important uses for the rotate instructions will be discovered when we discuss decision-making operations.

The Program to Pack BCD Digits is a simple demonstration that can be used to "pack" two BCD digits into a single data byte. The result of this sequence of steps is the data byte 01010111 stored in memory. Four MSBs are BCD "5," and four LSBs are BCD "7." Observe the use of the ORA B instruction, enabling two data bytes to be combined into one without changing either. Special 8080 microcomputer programs, called simulators, are available that permit the execution of an 8080 program to be followed step by step by observing changes in the contents of the internal registers.[5] If applied to the above program, the following should be observed *after* the execution of the indicated instruction bytes.

Executed Instruction Bytes	Accumulator	Register B
IN 015	10110101	—
ANI 017	00000101	—
RLC, RLC, RLC, RLC	01010000	—
MOV B,A	01010000	01010000
IN 015	10110111	01010000
ANI 017	00000111	01010000
ORA B	01010111	01010000

This completes our discussion of the more important logical instructions in the 8080A instruction set. Additional examples will be used in following columns, where they will be incorporated into data-manipulation and decision-making tasks.

References

1. D. G. Larsen, J. A. Titus, and P. R. Rony, "Microcomputer Interfacing: The MOV and MVI 8080 Instructions," *Computer Design*, Feb 1977, pp 120, 122
2. J. A. Titus, P. R. Rony, and D. G. Larsen, "Microcomputer Interfacing: Register Pair Instructions," *Computer Design*, Mar 1977, pp 122, 124, 126
3. *Intel 8080 Microcomputer Systems User's Manual*, Intel Corp, Santa Clara, Calif, 1975
4. P. E. Field, P. R. Rony, D. G. Larsen, and J. A. Titus, "Microcomputer Interfacing: A Software UART," *Computer Design*, Oct 1976, pp 118-120
5. One such program called DEBUG, has been developed by Tychon, Inc, in Blacksburg, Va. It requires the use of a teletypewriter or CRT

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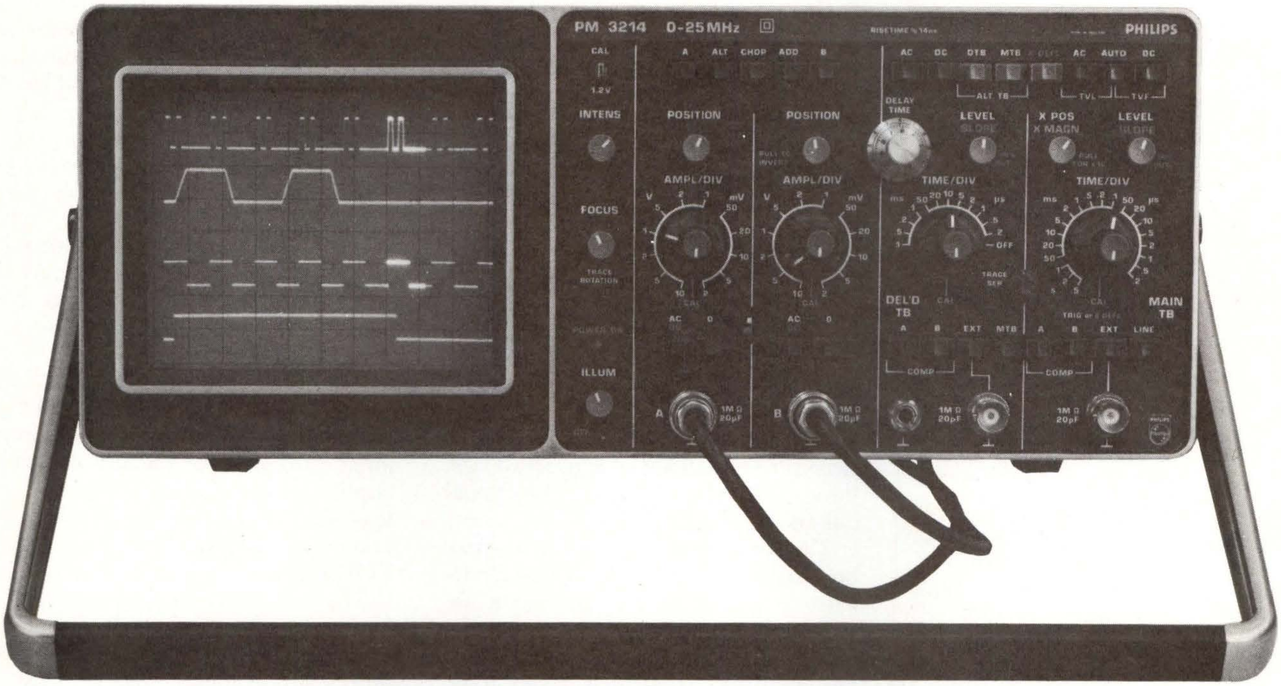

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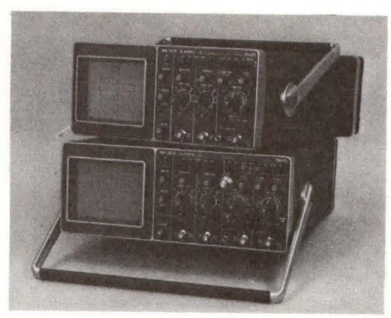

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Software Brings High Level Programming to Microcomputers

As an aid to microprocessor software development, PL/M6800™ is claimed by Intermetrics, Inc, 701 Concord Ave, Cambridge, MA 02138 to be the first high level programming language for the Motorola M6800 (or AMI S6800) microcomputer. It cuts time to a fraction of that required for assembly language without sacrificing direct access to hardware features and assembly language procedures, thereby giving a competitive "edge" to companies developing products for the rapidly evolving microprocessor-based system market.

The 1-pass compiler produces optimized directly loadable object code, taking advantage of almost every instruction on the microprocessor. A user-controlled switch selects whether the emitted code is in the AMI or Motorola loader format. Other user-controlled features include listings of source, object, and/or assembler codes, and symbol table dumps.

Compatible with Intel's PL/M™ language, the compiler is accessible via the NCSS timesharing network, or can be purchased directly for in-house installation on IBM 360 or 370 computers. It is claimed to offer "true software portability" in that it is syntactically identical to PL/M.

Circle 170 on Inquiry Card

Expandable μComputer Evaluation Kit Is Based on the MC6800 MPU

Based on the MC6800 microprocessing unit and its family of associated memory and I/O devices, the M6800 microcomputer evaluation kit, when assembled, is a fully functional microcomputer system. The kit, MEK-6800D2, is made up of two basic units—a microcomputer module (9.75 x 8.3", 24.8 x 21.08 cm) and a keyboard/display module (10 x 6.25", 25.4 x 15.9 cm), the latter containing audio cassette interface circuitry (Kansas City standard).

The microcomputer modules include the MPU, a ROM with JBUG monitor, three 128 x 8 RAMs, two peripheral interface adapters, an asynchronous communications adapter, and a clock generator. The display consists of six 7-segment LED readouts that display address (four units) and data (two units) in hexadecimal format. The keyboard is hexadecimal with eight additional command keys.

The Integrated Circuit Div of Motorola Semiconductor Products, Inc, 3501 Ed Bluestein Blvd, Austin, TX 78721 engineered the board to accept optional devices which include two 128 x 8 RAMs, two EPROMs, three buffers, and two bidirectional buffers.

The kit may be used as is, or may be expanded to a full 65k system. Custom expansion on the microcomputer module is simplified by a wire-wrap area that accommodates two 24-pin and 12 16-pin ICs. In addition, the JBUG monitor ROM can be replaced by a Minibug II ROM for RS-232 interfacing to other peripherals.

Package includes 3-ring binder with assembly manual, an M6800 Programming Reference Manual, and the M6800 Microcomputer System Design Data book. Price is $235 (power supply of 5 V at 2 A and cassette recorder are not included).

Circle 171 on Inquiry Card

Compact Single-Board Computer Features 5k of Resident System Software

Super Jolt combines a development system, prototyping system, and dedicated applications in a compact card measuring 4.25 x 7" (10.8 x 17.78 cm). The easy-to-use single-board computer from Microcomputer Associates, Inc, 2589 Scott Blvd, Santa Clara, CA 95050 contains an 8-bit 6502 microprocessor, 1k bytes static RAM, 32 bidirectional and programmable I/O lines, a 1-MHz crystal controlled clock, an interval timer, four interrupts including a timer and nonmaskable interrupt, and three serial interfaces (20-mA current loop, RS-232, and TTL).

The resident program ROM of 5120 bytes includes a complete single pass resident assembler program (RAP), resident TINY BASIC interpretive language designed for Jolt systems, and a 1024-byte DEMON DEbug MONitor program. The card with RAP can function as a single card development system permitting assemblies to be made with a single pass of a source program from a terminal or via a TTP paper tape reader. Following assembly, programs can be debugged.

A higher level language, TINY BASIC is a subset of Dartmouth BASIC, and permits immediate entry and execution of TINY BASIC language program. ROM software allows most I/O devices to be used.

Removal of the RAP and TINY BASIC ROMs permits the card to become a compact general-purpose microcomputer card suitable for any dedicated application. Vacated ROM sockets may be used for the user's programmed ROMs or 2708 type EPROMs.

The card is further supported by a family of Jolt modules which includes a 4k RAM, 2k 1702A p/ROM, I/O, power supply, and universal card. A 5-slot card cage and 8080 CPU card module substitute are also available. Buffering for all address and data lines provides easy expansion to additional card modules.

Circle 172 on Inquiry Card

Jumper Selections and Software Control Allow Custom Tailoring of ADC

An analog-to-digital converter system for Intel's SBC 80 single-board computers and Intellec MDS-800 microcomputer development systems features analog inputs accommodated by 32 single-ended or 16 differential jumper-selectable channels. Channels occupy 64 adjacent address locations (two per channel) which may be mapped by either memory or I/O via jumpers. Actual address space is also jumper selectable. System channel addressing is program controlled random.

Data channels of the 6.75 x 12" (17.15 x 30.48 cm) board are multiplexed to a high input impedance differential gain amplifier. Eight possible gains are selectable under software control. Gains of 1, 2, 4, 8, 10, 50, and 100 are supplied, and with the addition of two resistors, one user-defined value may be added. Any number of conversions may be accomplished at the same gain setting; once set, the gain value does not have to be redefined until another value is desired. Gain may be changed any time conversion is not taking place. Conversion time is 65 μs, derived from an Intel bus clock (35 μs is optional).

Digital outputs on the 12-bit resolution system are buffered and multiplexed onto the system data bus. Addressing is compatible with the 8080 CPU's convention of storing the least significant byte first, enabling conversions with the single LHLD instruction.

The flexible ADC system, priced at $350 each in quantity from Cybernetic Micro Systems, 2460 Embarcadero Way, Palo Alto, CA 94303, can operate in four jumper-selectable modes —program, status, interrupt, and externally controlled. This enables many system configurations with various hardware and software requirements. Externally triggered signals provide the ability to sample and convert multiple signals simultaneously from one trigger or program command, which requires one A-D board per desired signal. Multiple boards may be triggered in parallel to take simultaneous samples of multiple signals.

Circle 173 on Inquiry Card

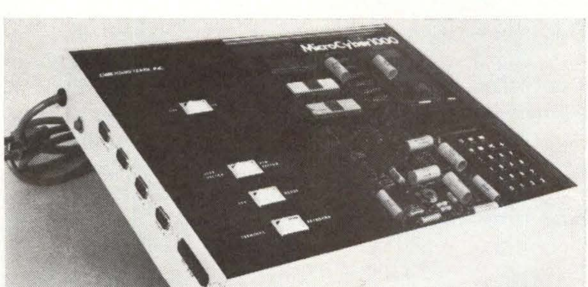
Portable System for Education/Hobbyists Accommodates Growth

Ready to plug into a 110-Vac wall socket to begin computing, the fully assembled MicroCyber 1000 microcomputer system is based on the MOS Technology 6502 chip. MOS Technology memory and I/O boards are compatible with the system bus. Featuring 1k RAM and 2k ROM, the system contains a monitor operating system with cold start bootstrap and TTY, keyboard, display, and audio cassette handlers in the 2k ROM. Software features include 13 addressing modes, bit manipulation instructions, decimal mode operation, 256-word deep stack processing, memory addressing techniques for I/O operations, and multiple interrupt processing capability.

Suited to educators, students, experimenters, and hobbyists for system prototyping, instrumentation, and test systems, the computer comes with a full hex keyboard and 7-digit LED display for address and data. Four external switches located on the system function as an on/off to switch from internal power supply to direct wall plug-in; for user vector/KIM vector to transfer control either to the system monitor program or user memory; for terminal/keyboard; and for TTY/RS-232-C.

Single-board expansion capability is contained within the basic chassis, with a memory or I/O board. For further expansion Cybersystems, Inc, 4306 Governors Dr W, Huntsville, AL 35805 also provides a 72-pin I/O and memory expansion bus connector with the system. Memory and I/O are bused and buffered to permit easy expansion. Memory can be expanded up to 64k bytes, allowing addition of system boards, resident assembler, and interpreter boards.

Measuring 14 x 11 x 2" (35.6 x 27.9 x 5.08 cm), the computer contains a system interval timer allowing real-time clock generation at 1.0 MHz to 4 Hz and time interval measurements of 1.0 μs to hours and days. Input voltage is 120 Vac. Address bus is 16 bits (65,536 words addressable), buffered to drive 25 TTL loads. The data bus has 8-bit words/data, and a buffer with bidirectional 3-state logic drivers/receivers.



Complete with all components necessary to start computing immediately, the Cybersystems microcomputer contains a 6502 CPU, 2k-byte ROM operating system, 1k-byte RAM, 6-digit hex address and data display, and 23-key keyboard, plus I/O and memory expansion capability

Options for the system are a 4k or 8k static RAM; expansion chassis with 10 slots for memory and I/O expansion; 6-ft (1.82-m) cassette cable and connector; complete kit with connectors and cable for cassette, TTY, RS-232, and two I/O port interfaces; complete chassis without KIM 1 CPU board; and custom briefcase. TTY and RS-232 communication interfaces adjust automatically to the terminal baud rate (even nonstandard rates) up to 600 baud.

Extensive hardware and software documentation comes with a complete program listing of the operating system and pin assignments clearly defined. A library of application and game programs including TINY BASIC (requiring 4k RAM) is offered by the company as support.

Circle 174 on Inquiry Card

Speed and Power of the Z80 Are Available In Dedicated Microcomputer

The key features—power and speed—of the Z-2 microcomputer are obtained from the Z80 microprocessor which is its integral component. Cromemco, Inc, 2432 Charleston Rd, Mountain View, CA 94043 has designed the computer for dedicated applications.

Packaged in an all-metal housing for relay-rack or bench cabinet mounting, the unit contains the company's CPU card (with switch selectable 2- or 4-MHz clock rate), a motherboard with 21 card sockets, and a heavy power supply providing 30 A from 8 V, and 15 A from ±18 V to meet most needs including floppy disc drives. The front panel is free of controls and switches to prevent accidental switch flipping.

Peripherals and circuitry can be added to this basic arrangement to meet particular needs. The computer also uses the S-100 bus which is supported with compatible peripherals.

The version of the Z80 used in the computer has a speed of 4 MHz (250-ns cycle time). This higher speed together with the more powerful instruction set provides more throughput for the microcomputer. Dedicated uses which benefit from this are real-time and timesharing operations. These uses are also facilitated with the company's line of memory boards featuring the 4-MHz speed and bank-select which allows up to eight independent banks of memory of up to 64k bytes each for a total memory of 512k bytes.

Designed for reliability as well as speed, the computer features "Blitz Bus."™ This ground-plane design on the motherboard reduces bus cross-coupling and ground-current noise by several decibels.

Other features include a power-on memory-jump which begins automatic program execution when the power is turned on, and a card retaining bar to keep circuit cards firmly in their sockets despite vibration, mechanical shock, etc.

The microcomputer uses 8080 software; in addition, the company offers software support which includes a monitor, assembler, and control-BASIC interpreter for microprocessor control applications.

The company's compatible peripherals include a 7-channel A-D and D-A converter; BYTESAVER which contains a p/ROM programmer and provides capacity for 8k bytes of memory; color graphics interface for using a color TV as a full-color graphics terminal; and digital interface that provides two serial I/O ports, two 8-bit parallel I/O ports, and 10 independent programmable interval times.

The microcomputer is available in kit form or assembled. The kit, priced at $595, comprises the Z-2 for rack-mounting, together with the 4-MHz microprocessor card, full-length 21-slot motherboard, power supply, one card socket and card-guide set, and front panel. The assembled unit, which also has all 21 sockets, card guides, and a cooling fan, costs $995.

Circle 175 on Inquiry Card

Major Additions to Line of Memory and I/O Boards Enhance SBC 80/System 80

In a major expansion of its line of memory and I/O boards, Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 has announced five additions aimed at enhancing the SBC 80 single-board computer and System 80 completely packaged microcomputer systems. Designated SBC 104, 108, 116, 517, and 519, each board interfaces directly with any SBC 80 or System 80 via the system bus to expand RAM and ROM capacity, and serial and parallel I/O capacity.

KEY PRODUCT FEATURES

	SBC 519	SBC 517	SBC 104	SBC 108	SBC 116
PROGRAMMABLE PARALLEL I/O	72 LINES WITH FULL BUFFERING	48 LINES WITH FULL BUFFERING →			
PROGRAMMABLE RS232C SERIAL I/O	NO	YES	YES	YES	YES
RAM MEMORY	–	–	4K BYTES	8K BYTES	16K BYTES
EPROM MEMORY (SOCKETS)	–	–	4K BYTES	4K BYTES	4K BYTES
INTERRUPT HANDLING	8 PROGRAMMABLE LINES WITH HARDWARE PRIORITY RESOLUTION	8 LINES →			

The 104/108/116 series are combination RAM and EPROM, and serial and parallel I/O expansion boards containing 4k, 8k, and 16k bytes of RAM, respectively. Onboard refresh hardware refreshes all eight RAM elements. If a read or write cycle is in progress when refresh is scheduled to begin, the refresh cycle waits until the read or write is completed. Each refresh cycle uses memory for 590 ns. Typical RAM access time is 485 ns; read/write cycle time is 560 ns.

Sockets for up to 4k bytes of nonvolatile ROM reside on board. ROM may be added in 1k-byte increments using Intel 8708 erasable and electrically reprogrammed ROMs or Intel 3808 masked ROMs. Typical ROM/EPROM access time is 440 ns and cycle time is 560 ns.

Both this series and the 517 combination I/O expansion board (with addressing and connectors directly compatible with the series) contain 48 programmable I/O lines implemented using two of the company's 8255 programmable peripheral interfaces. System software configures the I/O lines to meet a variety of requirements. I/O interface flexibility is enhanced by the ability to select appropriate combinations of optional line drivers and terminators to provide necessary sink current, polarity, and drive/termination characteristics.

A programmable RS-232-C communications interface on each board via an Intel 8251 USART (universal synchronous/asynchronous receiver/transmitter) allows almost any serial data transmission technique for interfacing to CRTs, RS-232-compatible cassettes, and modems. Onboard registers contain the status of eight interrupt request lines.

Each board contains a jumper-selectable 1-ms interval timer and interface logic for eight interrupt request lines. Typical I/O read access time is 280 ns and read cycle time is 600 ns. Each board measures 6.75 x 12" (17.15 x 30.48 cm.)

SBC 519, however, has 72 programmable I/O lines which can be expanded via direct bus interface. Three 8255 devices are used with typical read access times of 350 ns and read/write cycle times of 450 ns. An interval timer can generate real-time clocking in systems requiring periodic monitoring of I/O functions. A programmable interrupt controller (PIC) provides vectoring for eight interrupt levels; it accepts interrupt requests from programmable parallel I/O interfaces, the interval timer, or directly from peripheral equipment. The PIC interrupt request output line may be jumper selected to drive any of the nine interrupt lines on the SBC 80 bus. Any of the onboard request lines may also drive any SBC 80 bus interrupt line directly via onboard jumpers and buffers.

Circle 176 on Inquiry Card

Disassemble and Trace Programs Operate on 8080 Machines

Available on iCOM floppy disc or punched paper tape in Intel hex-ASCII object format, the 8080 disassembler and trace programs may be obtained from Cybergrafix, PO Box 430, Glendale, CA 91206. Designed to run on 8080-based machines, the first program disassembles 8080 object code, producing a "source" listing in format identical to that produced by an Intel assembler. It also produces an ASCII listing of object code and a symbol cross reference listing. A source file also is produced on floppy disc or punched paper tape which may be input to an assembler with little or no editing. Up to 10 known data areas may be specified which will be treated as DB statements.

The trace program, designed as a teaching and troubleshooting aid, resides in memory with the subject program, which is executed under trace control. The machine condition is displayed after each subject instruction is executed. Display includes instruction address, instruction in machine code (hexadecimal) and mnemonic, contents of all registers, and latest stack entry; it may be reduced to only instructions causing branch operations. Modes of operation (single step, branch, continuous, etc) may be changed during execution by the operator.

Both programs are specialized to run on user's equipment. Updates resulting from continuous program improvements are automatically supplied to purchasers.

Circle 177 on Inquiry Card

SLAM Compiler Provides Small Intel Systems With High Level Capability

A true, code-emitting compiler for small Intel microcomputer systems, the SLAM compiler is completely source code compatible with the previous SLAM interpreter—the two combining to produce powerful, versatile software. SLAM (Symbolic Language Adapted for Microcomputers) is a high level language which uses signed 16-bit decimal integers to program microcomputers without the need to learn assembly or machine languages (see *Computer Design*, Dec 1976, p 126).

Programs can be created, modified, and debugged rapidly using the interactive interpreter. When the program is verified and running correctly, the compiler can then translate it to hexadecimal 8080 object code in Intel standard format, ready to load in RAM or ROM.

The compiler includes advanced system-oriented features such as provision for parameter-linkage conforming to Intel conventions, absolute memory pointers, and machine-language subroutine calls. Compile-time interaction with the operator customizes run-time storage configuration for individual requirements.

Occupying less than 8k of RAM, the compiler is available from Penn-Micro, PO Box 5073, Lancaster, PA 17604. It requires no large memory boards or bulk storage. Versions are available for the Intellec 8/Mod 80, MDS-800, or SBC 80 systems. Both the compiler and interpreter are available on paper tape in Intel-standard hexadecimal format, ready to load and execute using the system monitor.

Circle 178 on Inquiry Card

Simple Language Ensures Easy Programming of SC/MP Microprocessors

In an effort to provide programming tools that are easy to understand and use, National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051 has developed NIBL (pronounced "nibble"), its National Industrial Basic Language which is similar to BASIC. For use with the 8-bit SC/MP microprocessor system (see *Computer Design*, April 1976, pp 134-138, and Feb 1977, pp 128-130), this microprocessor programming aid is aimed at making SC/MP as easy to use as possible for those trained neither in electronics nor computer programming.

In the past most microprocessors, especially for low cost control applications, have been programmed in assembly language; it produced a fast and efficient code, but was difficult and tedious to read, write, and learn. NIBL requires the user to trade high execution speed and memory efficiency for advantages such as program readability, modifiability, and rapid program generation. Program construction, debug, and documentation are simplified since each NIBL statement equals five to 20 machine language commands. NIBL tasks also tend to take less memory than assembly language equivalents.

The language is an adaptation of TINY BASIC, which was developed as a general-purpose game and control language for microprocessors. TINY BASIC was written interpretively in a language designed for the construction of translators for adaptation to many microprocessors.

To adapt it for SC/MP, a simple interpreter was constructed; improvements in I/O and device control have also been added. NIBL source programs are interpreted by a 4k-byte SC/MP program residing in ROM. The interpreter is divided into two blocks: a program written in an intermediate or interpretive language which deciphers NIBL, and a collection of SC/MP machine language subroutines invoked by the intermediate language.

Minimum hardware required for implementing the language is the SC/MP CPU, crystal, and support logic; 110-baud ASCII terminal interface; 4k x 8 bits of ROM for NIBL; 2k x 8 bits of RAM user space (allowing about 60 average NIBL statements); a teletypewriter or similar terminal; and a 5-V power supply. As an option, the language will support an additional 26k bytes of user memory, giving a total capacity of nearly 1200 average lines of code in 28k x 8 bits of RAM or ROM.

Well suited to control tasks in view of its inherent speed limitations, the language can handle video generation, direct control of fast peripherals, and other uses; the algorithms for these applications should be proved out in NIBL and translated into SC/MP machine code for installation in the final system.

Two versions of NIBL are available, one for the older p-channel MOS SC/MP operating with a 2.0-MHz clock cycle and one for the newer n-MOS SC/MP II with a 4.0-MHz microcycle. To insure its wide dissemination, the language has been placed without charge in the public domain. It is available in paper tape form through COMPUTE, the company's Microprocessor Users Group newsletter. In preparation are a self-teaching manual for NIBL and the SC/MP low cost development system, and a NIBL firmware package in ROM.

6800 Interface Permits Use of ASCII Terminals on Selectric Interfaces

A smart ASCII converter interface has been designed to provide complete plug compatible conversion from the 1980 Selectric™ interface to the standard ASCII EIA and 20-mA loop interface. Output from the interface will drive most standard data printer terminals so that a user can select the printer suited to the application.

The unit consists of a single board 6800 microcomputer system programmed to do the conversion. Memspec Computer Systems, Inc, 6549 Dawson St, Vancouver, BC, Canada V5S 2W2 designed the device to request data as quickly as necessary to keep data flowing at the full output baud rate. A 100% throughput is claimed to be possible with the output baud rate set for 300 baud (30 char/s). Buffer size in the host system may affect throughput rate.

Standard features include upper and lower case output capability and jumper-selectable baud rates. Unit can provide common rates from 67.2 to 9600 baud. A 20-mA plug and EIA control lines provide full control of power-on to host system. Input interface has fail-safe mode to indicate busy and power-off to host system.

Single board which is removable with a screwdriver offers easy maintenance. All large ICs are socket mounted for easy removal and replacement.

Full optical isolation is incorporated on all inputs and outputs for reliability and protection of host system. Input is 48 Vdc with others on request. Maximum load on any input line is 26 mA. There are no power supplies on the input interface.

Output is 20-mA loop current drive up to 1000 ft (304.8 m), or EIA output up to 25 ft (7.62 m). Standard ASCII output includes upper/lower case, numbers, and most other characters.

Power requirements of the 4 x 12.625 x 17.75" (10.16 x 32.07 x 45.09 cm) unit are 120 Vac, 60 Hz input at 40 W. An auxiliary ac outlet socket is available for the printer terminal with maximum of 4 A. Custom programming and other options can be added on request.

Circle 179 on Inquiry Card

Cross Assemblers for μProcessors Available in ANSI FORTRAN IV

Two assembler programs providing microprocessor support software for the Intel 8048 and Zilog/Mostek Z80 are written in ANSI standard FORTRAN IV. The cross assemblers will operate on any computer with a word length greater than or equal to 16 bits, including most minicomputers.

Assemblers are designed by Microtec, PO Box 60337, Sunnyvale, CA 94088 to be manufacture-compatible, providing standard features such as symbolic and relative addressing, and constant generation. Also included is a macro facility, conditional assembly statements, and a cross reference table listing option.

The Z80 assembler assembles both Z80 mnemonics as defined by Zilog/Mostek and 8080 mnemonics as defined by Intel. They can be delivered on several types of computer readable media. Included with each program is a manual, source listing, and test program with its output listing.

Circle 180 on Inquiry Card

Code Card Serves as 8080 Software Reference Aid

The 8080 octal code card is a slide-rule-like aid for programming and debugging 8080 software. Containing all mnemonics and their corresponding octal codes, the card features color-coded instructions to indicate which flags are affected during execution.

The pocket-sized 6.5 x 3" (16.51 x 7.62 cm) card from Tychon, Inc, PO Box 242, Blacksburg, VA 24060 provides the instructions in a logical format for quick reference. An ASCII code chart for all 128 characters plus 8080 status word and register pair codes is printed on the back side of the card. A hexadecimal card will also be available.

Circle 181 on Inquiry Card

Z80 μProcessor Board and Monitor Designed for Intel SBC 80/10

A single-board Z80 microprocessor system and an operating monitor for the Intel SBC 80/10 board have been announced by Mini Micro Mart, 1618 James St, Syracuse, NY 13203. Software compatible with the 80/10 but using the Zilog Z80 CPU, the microprocessor system has provision onboard for three 2708 EPROMs, 1k of static RAM, two 8255 parallel interfaces (providing nine parallel ports), and an 8251 USART for serial interfacing. Both a 20-mA current loop TTY and an RS-232 interface provide for baud rates from 110 to over 9600.

Full address decoding is available for both the onboard memory and I/O devices. Altair, Imsai, and Processor Technology software can also be run with minor modifications. The 7 x 10.5" (17.78 x 26.67 cm) board is plated-through epoxy glass material with gold fingers.

CPU board is available in kit form, or assembled and tested. A complete system in a self-contained table top cabinet, including Teletype™ printer, is available. As an introductory offer, listings for the company's 5k BASIC and operating monitor are included.

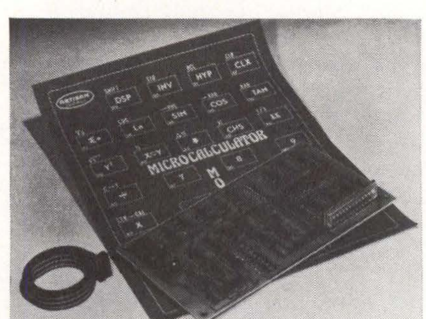
The Monitor 80 SBC 80/10 permits the Intel 80/10 to be used as a standalone development system. It provides for entering and dumping in both symbolic and octal codes. The user can initiate program execution, set or clear breakpoints, copy a block of memory, or translate a program to a new location. An edit mode is also provided.

Occupying approximately 2.5k of memory, the monitor starts at a "0" address. In addition to normal monitor software, there are routines for programming p/ROMs, a checksum routine, and software for loading and dumping to a simple audio cassette recorder interface. It is available with source listings and punched tape in Intel hex loader format, or in the form of three programmed 2708 EPROMs, including manual.

Circle 182 on Inquiry Card

Microcalculator for 8-Bit μProcessors Offers Scientific Capabilities

Intended for direct interface with most 8-bit peripheral interface de-



vices such as the Motorola 6820, Mostek 3820, MOS Technology 6530, and Intel 8255, the model 85 microcalculator requires only 5 V for operation and interfaces with the microprocessor through an 8-bit bidirectional I/O port. Each entry normally made by a key is replaced with an 8-bit instruction from the microprocessor. The number of input instructions is restricted only to the user program or the amount of memory in the microprocessor system.

Instruction entry to the microcalculator is under microprocessor software control. It accepts instructions, provides a means to detect busy status, and outputs the full 14-digit display back to the microprocessor for storage or display. Control software in both a read and write mode requires less than 256 bytes of microprocessor system memory.

Both statistical and scientific calculation capabilities are provided to calculate mean and standard deviation, and to handle scientific, engineering, mathematical, or statistical problems. Developed by Artisan Electronics, 5 Eastmans Rd, Parsippany, NJ 07054, the calculator contains four register stacks with nine memory registers. Problem solving capability includes transcendental functions, polar/rectangular coordinate conversions, multiple storage registers, and constants including four U.S./metric conversion units. The microcalculator together with the microprocessor can aid in achieving an advanced programmable scientific calculator system.

Circle 183 on Inquiry Card

Faster Microprocessor Is Pin and Software Compatible With Z80

Becoming the company standard microprocessor, the Z80A has been announced by Zilog, 10460 Bubb Rd, Cupertino, CA 95014 as a faster microprocessor that is totally pin and software compatible with their present Z80 (see *Computer Design*, Feb 1976, p 132). This microprocessor features a standard clock rate of 4.0 MHz as a result of the company's process technology. The current Z80 will continue to be offered at a clock rate of 2.5 MHz for customers who do not need the faster device.

Considered to be the fastest standard product microprocessor available, the Z80A has an instruction cycle time of 1.0 μs. Users will be able to increase system throughput by 60% over Z80 systems. Pricing of the device will be in the same range as that of the Z80.

Circle 184 on Inquiry Card

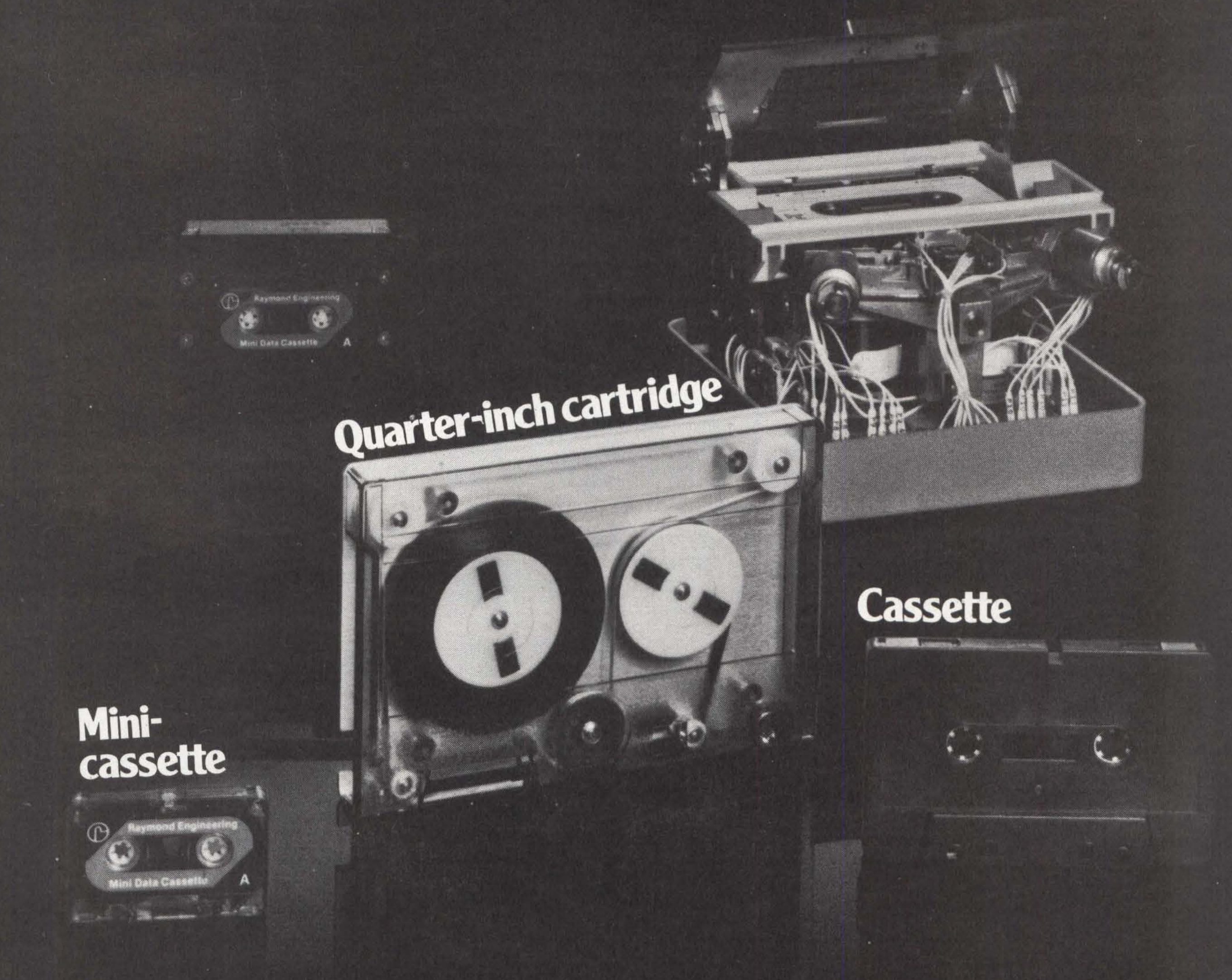
Nonvolatile RAM for MDS 800 and SBC 80/10 Microprocessor Systems

Designed for nonvolatile operation with Intel's Intellec[R] MDS 800 and SBC 80/10 is the MM-8080A 8k x 8 RAM core memory system which eliminates data loss upon power removal. Compatibility with existing processor boards is ensured through use of memory boards that plug directly into existing Intel connectors.

With the memory system from Micro Memory, Inc, 9438 Irondale Ave, Chatsworth, CA 91311, the microcomputer user can fulfill the function of both RAM and p/ROM on the same unit. Data access time is 350 ns; cycle time is 1.0 μs. A power status signal is available as a power interrupt vector or as a power reset signal.

Onboard module expansion is available in 4k increments up to 64k words of memory. The 6.75 x 8.0 x 1.0" (17.15 x 20.32 x 2.54 cm) module contains timing, control, decode, drive circuits, address registers, and data registers.

Circle 185 on Inquiry Card



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Emulator Board Performs Functions of 3870 Microcomputer

To aid in developing and field testing systems which utilize the F8-compatible MK 3870 single-chip microcomputer, Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006 has announced the EMU-70 emulator board. Electrically equivalent to the MK 3870, but field rather than mask programmable, the emulator enables the user to obtain final software verification prior to ordering the MK 3870.

The board performs all functions of the 3870 microcomputer providing 2k bytes of p/ROM, 64 bytes of scratchpad RAM, four 8-bit TTL compatible latched I/O ports, software programmable timer, and vectored interrupts. Operation is 2 MHz from a single 5-V power supply.

Two 1k x 8-bit 2708 UV-erasable p/ROMs provide nonvolatile storage of the user's program. The p/ROMs are programmed with a p/ROM programmer and then are installed on the board. Prototype systems can be converted to final production status by unplugging the emulator and plugging in the corresponding 3870. As a cost-effective solution to low volume logic replacement applications, the board can be used as the final configuration where code changes and volume would not justify ordering a masked programmed microprocessor.

Circle 186 on Inquiry Card

4- to 20-mA Process Control Outputs On Board Result in Compactness

An 8-channel D-A converter system when combined with the compatible Intel SBC 80 microcomputer series forms a complete 8-channel analog output system for computerized control and readout applications in industrial and laboratory processes. Two single-board models—a 12-bit model 1842 and 8-bit 1843—are available in the analog output series.

The analog output system has eight independent D-A converter channels, each fully double buffered to avoid intermediate outputs in the 2-word microcomputer transfer. All eight channels are powered directly off the Intel microcomputer's 5-V power supply through a highly regulated, low noise dc-dc converter.

Data Translation, Inc, 23 Strathmore Rd, Natick, MA 01760 has implemented a compact approach with the board's option of 4- to 20-mA current loop outputs for all channels. By using just two cards, costs are reduced by eliminating the need for separate drivers.

The output system is packaged on the same size card as the SBC 80—6.75 x 12" (17.15 x 30.48 cm). The 0.375" (0.95 cm) high card fits in the standard 0.5" (1.27 cm) spacing of the Intel card cage.

Mechanically, electrically, and software compatible with the SBC 80 series, the 1842 and 1843 have differential linearity of ±½ LSB, gain and offset adjustable to zero for each channel, and settling time of 1 μs to 0.2% and 3 μs to 0.01% FSR. In addition to 4- to 20-mA outputs, pin-strappable analog ranges of ±10 and 0 to 10 V are available with line amplified buffered outputs for driving long cables. Application software can be developed in the MDS 800 system, and subsequently run with the SBC 80 microcomputer for OEM applications.

Circle 187 on Inquiry Card

Versatile A-D/D-A I/O Card Increases Z80 System Throughput

A multiplexed A-D/D-A analog I/O card for use exclusively with Zilog's Z80 microcomputer systems features a commutating memory (patent pending) to increase system throughput by over 25%. Other features include 12-bit A-D conversion; 20-μs conversion speed; programmable gain amplifier with gains of 1, 2, 4, and 8; and an onboard Zilog PIO chip.

Also available from Signal Laboratories, Inc, 202 N State College Blvd, Orange, CA 92668 are options such as a 32-channel analog input capability (16 standard), two DAC output capability, four discrete (1-bit) outputs, and a dc-dc converter for 5-V power only operation. □

Circle 188 on Inquiry Card

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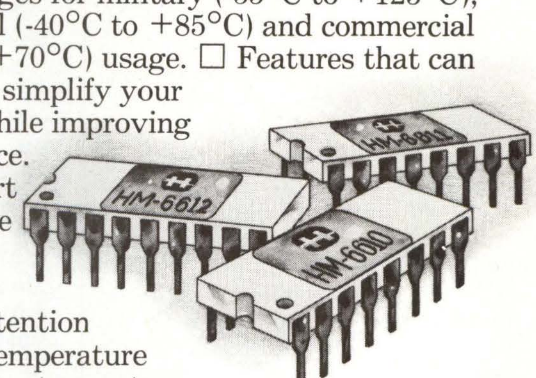

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TYPE NO.	ORGANIZATION	PINS	SPEED	FEATURES
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HM-6611 PROM	256x4	16	450 ns	benefits of low active and standby
HM-6612 PROM	256x4	18	450 ns	power, high noise immunity and fast access time.
HM-6312 ROM	1024x12	18	350 ns	Highest density CMOS ROM available. Ideal for 12 bit microprocessor systems.
HM-6508 RAM	1024x1	16	290 ns	Bipolar RAM pinout
HM-6518 RAM	1024x1	18	290 ns	6100 uP compatible
HM-6501 RAM	256x4	22	285 ns	Popular 5101 pinout
HM-6551 RAM	256x4	22	285 ns	Latched chip select
HM-6561 RAM	256x4	18	285 ns	6100 uP compatible
HM-6562 RAM	256x4	16	285 ns	Smallest 256x4 RAM available.

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CIRCLE 89 ON INQUIRY CARD

AROUND THE IC LOOP

Bubble, CCD, EPROM, and RAM Devices Expand Memory Market

Among the IC devices announced by Texas Instruments Inc, PO Box 5012, Dallas, TX 75222 were a 92k-bit magnetic bubble memory; a 65k-bit charge-coupled device memory; a 16k-bit ultraviolet-light erasable, electrically-programmable read-only memory (EPROM); a 4k-bit dynamic random-access memory (RAM); and four 4k-bit static RAMs. The bubble memory is available now in sample quantities at $200 each, while prototype quantities will be available about mid-year and production quantities will be shipped by the fourth quarter. Prototypes of the CCD have been supplied and samples are expected to be available at $195 each by the time this article is printed. Prototype or production quantities of all the other memories are now being shipped.

Bubble Memory

Microprocessor-compatible TBM0103 has first bit access time of 4 ms at 100-kHz operation. Cycle time is 12.8 ms for the 144-bit page and approximate power consumption is 0.5 W for continuous operation over its 0 to 50°C range. Nonvolatile storage range is —40 to 85°C.

Comprised of magnetic epitaxial film grown on a gadolinium-gallium garnet substrate, the chip contains 5-μm dia magnetic bubble domains. Patterns of permalloy metal are deposited on the epitaxial film to define the path of the bubble domains in the presence of a rotating magnetic field. As the field rotates, the bubble domains move under the permalloy pattern in shift register fashion.

Device architecture is major loop/minor loop. Data bits are written into and read out of the major loop; data bits are transferred to minor loops for storage. A total of 157 minor loops, each consisting of 641 bubble positions, results in a single chip memory storage capacity of 100,637 bits. However, a maximum of any 13 of the 157 minor loops on the chip is allowed to be defective. Therefore, the minimum data capacity of the remaining 144 good loops is 92,304 bits. Bubble control functions such as generate, transfer in, transfer out, replicate, and annihilate are executed by providing current pulses through the appropriate control elements on the chip.

The bubble memory is packaged in a 14-pin DIL module measuring 1.0 x 1.1 x 0.4" (2.54 x 2.8 x 1 cm). The module contains a 92k-bit bubble chip surrounded by two orthogonal coils that provide the rotating magnetic field, a permanent magnet set, and a magnetic shield to protect data from external fields.

Circle 350 on Inquiry Card

Charge-Coupled Device Memory

TMS3064, organized externally as 65,536 1-bit words and internally as 16 addressable 4096-bit serial-parallel-serial (SPS) loops, is fabricated by a combination of 2-phase coplanar electrode CCD structure with the standard double poly n-channel silicon-gate MOS process. Use of ion implant storage wells allows the simple 2-phase non-overlapping clock. The two clock and the chip-enable inputs can be driven by standard MOS-level drivers.

All other inputs have 200 mV of dc noise immunity when interfacing with standard TTL. No pull-up resistors are required. The 3-state output will drive at least two standard series 74, 74S, or 74LS loads without the use of pull-up resistors.

Maximum data rate is 5M bits/s. Maximum access time is 800 μs at 5 MHz. Typical operating power dissipation is 300 mW at 5 MHz; standby power dissipation is <30 mW. Packaging is 16-pin ceramic DIL with pin rows on 400-mil centers. Operating temperature range is 0 to 70°C.

Circle 351 on Inquiry Card

EPROM

A direct plug-in replacement that doubles the capacity of the company's 8k-bit TMS2708 and TMS27L08 as well as other 2708s currently on the market, one TMS2716 EPROM dissipates less total power than most 2708s with half the memory capacity. The UV-light erasable device has the same package and pin-outs, basic chip design and circuitry, and power supplies and power requirements, and fits into the same sockets as all existing 2708s.

Memory circuit organization is 2048 x 8. Maximum access and minimum cycle times are 450 ns. Data outputs are 3-state for OR-tying multiple devices on a common bus. Power consumption is 375 mW typical.

Erasure results from exposing the chip through the transparent quartz lid to high intensity UV-light. Existing p/ROM-EPROM programmers can be used. The DIL ceramic device operates at from 0 to 70°C.

Circle 352 on Inquiry Card

4k RAMs

Dynamic RAM TMS4027 features 150-ns access time, 320-ns cycle time; ±10% power supply tolerance (12, ±5 V); 460-mW active, 27-mW standby maximum power consumption; common I/O capability; gated $\overline{RAS}$, $\overline{RAS}$-only refresh, and page-mode capabilities; TTL-compatible inputs with low capacitance; input latches for addresses, chip select, and data in; 3-state TTL-compatible high drive outputs; and output data latched and valid into next cycle. Multiplexing/latching of address inputs allows the n-MOS device to be packaged in a 16-pin 300 mil-pin-row DIP, reducing memory board space requirements by 40% over 22-pin packages.

Four full static n-MOS RAMs, designated TMS4044 and -4046 in 4096 x 1 and TMS4045 and -4047 in 1024 x 4 configurations, are available with 450-, 300-, 200-, and 150-ns maximum access times. All operate from single 5-V supplies and are fully TTL-compatible. A 3-state output and a chip select permit simple memory expansion.

Typical operating power dissipation for 200-ns versions is <325 mW. TMS4046 and -4047 series offer power down with power consumption of <10 mW. TMS4044 and -4045 are in 18-pin packages; -4046 and -4047 are in 20-pin. All have fully decoded direct addressing and are available in plastic or ceramic DIPs rated over a temperature range of 0 to 70°C.

Circle 353 on Inquiry Card

Ask CONTROL DATA for the new low cost, problem-free OEM companion to Cartridge Disk Drives.

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We have it.

"Falcon" offers superior reliability (6000-hour MTBF) and maintainability. Here are just a few of the reasons why:

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But first, test evaluate it... compare it with competitive drives. Whether large OEM or small, you'll discover you can offer incredible reliability at lower cost—and that's a good offer any time!

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Tell me more about your OEM Falcon Fixed-Media Double-Density Disk Drive.

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Ask the CDC OEM people

CONTROL DATA CORPORATION

CIRCLE 90 ON INQUIRY CARD

Interchangeable 4k/16k RAMs Can Reduce Costs of Systems Design

A family of interchangeable 4k- and 16k-bit dynamic random-access memory devices introduced by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 directly replace the industry standard 16-pin 4k RAMs now used in many production memory systems. Electrical and logical compatibility permits 4k and 16k RAMs to be easily combined in memory systems.

Series 2104A are second-generation versions of the company's 2104 16-pin, 4k dynamic MOS RAM, and can replace the 2104 and similar RAMs with up to a doubling of speed-power performance and sharp reductions in system noise problems. New 2116 types are improved versions of the company's 2116 16-pin, 16k devices and older 16-pin, 4k RAMs with up to a quadrupling of speed-power performance as well as a quadrupling of system storage density. Both use single transistor storage cells and unique circuit designs to improve speed and minimize peak current transients which occur during each operating cycle.

Maximum access times are down to 150 ns for the 2104A and 200 ns for the 2116. These operating speeds are guaranteed over a wide power supply tolerance of ±10% as well as over the full temperature range of 0 to 70°C.

Power reductions allow average power dissipations of microwatts per bit to be achieved in memory systems. Typical power dissipations of the 2104A are 240 mW active and 8 mW on standby.

Compatibility features include industry standard multiplexed address inputs, 64-cycle refresh (plus an alternative 128-cycle refresh for the 2116), industry standard 2-ms refresh intervals, latched, 3-state data output, page-mode as well as word-mode access, on-chip latches for both data and address inputs, ±10% tolerance on all three supplies, and 0.8-V low input maximum and 2.4-V high input maximum to enhance noise immunity. The devices are TTL-compatible, including clock inputs. Power reductions and wide supply tolerance will generally allow older RAMs to be replaced without changing power supplies while giving most system producers the option of using smaller, more economical power and cooling subsystems. The family members require less power than most recently announced types and only one-half to one-quarter as much power per bit as earlier designs.

Circle 354 on Inquiry Card

Block Addressable CCD Memory Aimed at Bulk Memory Market

Samples of a 65,536-bit CCD memory will be available during the second quarter of this year from the MOS/CCD Products Div of Fairchild Camera and Instrument Corp, 464 Ellis St, Mountain View, CA 94042. Production quantities are scheduled for later in the year.

Device CCD464m is organized 65k x 1. Its internal architecture divides the memory into 16 blocks of 4096 bits each.

Typical data rate is 5 MHz, with average latency (retrieval time for an average bit) of 400 μs. Power dissipation is <5 μW/bit in active mode and <1 μW in standby. The device is packaged in a standard 0.300" (0.762 cm) 16-pin DIP.

Circle 355 on Inquiry Card

Quad Comparators Meet Signal Detection/Processing Needs

Two precision monolithic quad comparators, the HA-4900 and HA-4905, introduced by Harris Semiconductor, a division of Harris Corp, PO Box 883, Melbourne, FL 32901, offer 130-ns response time with 5-mV overdrive, 2.0-mV offset voltage, 10-nA offset current, and no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. The comparator can sense signals at ground level while being operated from either a single 5-V supply (digital systems) or from dual supplies (analog networks) up to ±15 V.

Output stage logic levels are controlled by two separate logic supply pins so that the output levels can be made compatible with any logic family without the use of external pull-up resistors. This effectively separates input and output stage ground lines and eliminates coupling between analog and digital grounds in combination analog and digital systems.

HA-4900 operates from −55 to 125°C and HA-4905 operates over a 0 to 75°C temperature range. Both devices are available in 16-pin ceramic DIPs. 100-up prices are $11.25 for the HA1-4900-2 (military) and $4.95 for HA1-4905-5 (commercial).

Circle 356 on Inquiry Card

Hermetic DIP Sample/Hold Amplifiers Available at Low Cost

Claimed to be the first complete 1-μs sample and hold amplifiers in DIPs, 12-bit accurate MN346 has an acquisition time of 1 μs for a 10-V step and an aperture guaranteed to be better than 60 ns. Offset voltage is typically 3 mV including sample to hold change without user adjustment, and gain error is specified to be better than ±0.05% over the full operating temperature range. In addition, power consumption is typically 640 mW from standard ±15-V supplies.

MN347 offers the same features at lower cost for applications requiring 10-bit accuracy. Both devices are available from Micro Networks Corp, 324 Clark St, Worcester, MA 01606 for both the 0 to 70°C commercial and −55 to 125°C military operating temperature ranges. MIL-STD-883, Class B screening may be added for high reliability applications.

Some other typical specifications for the MN346 (MN347) are: gain error at 25°C, ±0.02% max (±0.05%); droop rate at 25°C, 0.5 mV/μs max (1.5 mV/μs); and bandwidth, 1.4 MHz typ. Prices are $70 for the MN346 and $60 for the MN347.

Circle 357 on Inquiry Card

Bipolar Multipliers Available For Military/Commercial Uses

High speed bipolar multipliers in 8-, 12-, and 16-bit configurations for both military and commercial temperature range operation are now available from TRW, 1 Space Park, Redondo Beach, CA 90278. MPY-12 and -16 will be available in 64-pin ceramic flat packages with built-in heat studs as well as in standard 64-pin ceramic DIPs with integrated heat sinks for the military temperature range. The 130-ns MPY-8 will be supplied only in a 40-pin ceramic DIP for both commercial and military temperature ranges.

In addition to the full mil-temp range devices, the company will also supply devices fully qualified to level B of military specification 38510. Prices for these fully qualified multipliers will be quoted upon request.

The multipliers are bipolar, fully TTL-compatible, LSI, 2's complement devices. MPY-16, a 16 x 16-bit parallel multiplier, operates at 160 ns and is capable of performing over 5 million multiplications/s. The 12-bit MPY-12 operates at 150 ns; and the MPY-8, the 8-bit version, has a typical multiply time of 130 ns.

Circle 358 on Inquiry Card

Extended Range ADCs Meet Military Performance Requirements

Series 873-15 TTL-compatible analog-to-digital converters are designed for military, aerospace, and other applications requiring high performance in environmental extremes of temperature, shock, vibration, and humidity. Available off-the-shelf in a choice of 0 to 10, −10 to 10, and −5 to 5 V input voltage range from Beckman Instruments, Helipot Div, PO Box 3100, Fullerton, CA 92634, all models offer complementary straight binary and complementary offset binary digital codes for both parallel and serial data output.

They are hermetically sealed in standard, 24-pin DIPs and offer 12-bit resolution and ±½ LSB in 12 linearity over the full −55 to 125°C temperature range. Gain drift is typically <±10 ppm/°C, and gain drift and offset error are externally adjustable to provide accuracy of ±0.012% full scale reference range ±½ LSB quantizing error. Conversion speed is 30 μs. Power requirements are 15 and 5 Vdc.

Each model in this series contains three quad current switches, a thin-film ladder/scaling/offset resistor network, a dc reference with associated ladder driver and reference control amplifier, a comparator, and a successive approximation register. Price is $185 each in 100-piece lots.

Circle 359 on Inquiry Card

Prices Reduced on 8- and 10-Bit DACs

Improved processing capabilities, increased demand, and second source availability have led to price reductions in a number of 8- and 10-bit digital-to-analog converters produced by Precision Monolithics Inc, 1500 Space Park Dr, Santa Clara, CA 95050. For example, 8-bit DAC-08Q, -08EQ, and -08CQ now sell for $7.95, $5.50, and $4.50 each, respectively, in 100 to 999 quantities. MIL-STD-883A, Class B device DAC08-883-Q is now $10.50 in the same quantities. DAC-03, a 10-bit device, sells now for $7.95 to $18.00 depending on capability provided.

Circle 360 on Inquiry Card

Analog I/O Devices Form Modular Data Acquisition System

A modular data acquisition system for the Micromodular family consists of an 8-channel, differential-input module called Micromodule 5A (MM5A), a 16-channel, single-ended-input module (MM5B), and a 4-channel analog output module (MM5C). Analog input voltage range of MM5A/B is ±10 mV to ±10 V; the input current range is 4 to 20 mA or 10 to 50 mA (resistor programmable). Input impedance is 100 MΩ; amplifier gain range is 1 to 1000 V/V(resistor programmable). Both contain input multiplexer, high gain instrumentation amplifier, sample/hold circuit, 12-bit ADC, timing/control/address decode logic, and 5- to ±15-V dc-dc converter. Throughput accuracy is ±0.025% full scale range (±10 V input); conversion time is 33 μs (±10 V input). Sample/hold aperture time is 30 ns; common mode rejection ratio for differential inputs is 74 dB (dc to 2 kHz).

Analog output range of the MM5C is strap selectable for ±10, 0 to 10, ±5, 0 to 5, or ±2.5 V (at 5 mA). Impedance of the output is 1 Ω; output settling time is less than 10 μs. Throughput accuracy is ±0.0125% full scale range. The device contains four 12-bit hybrid DACs, a 12-bit latch, address decode/write control logic, and a 5- to ±15-V dc-dc converter. Inputs of the DACs are double-buffered to minimize output glitches.

All three are bus-compatible with an EXORciser or Micromodule system and operate over a temperature range of 0 to 70°C. Unit price of each module, from Motorola Semiconductor Products, Inc, PO Box 20294, Phoenix, AZ 85036, is $725.

Circle 361 on Inquiry Card

BIFET Op Amp Prices Reduced

Substantial reductions in the prices of its line of operational amplifiers built using BIFET technology have been announced by National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051. The 15 devices in the series replace expensive hybrid and module devices in such applications as precision high speed integrators, fast A-D and D-A converters, high impedance buffers, logarithmic amplifiers, sample-and-hold circuits, photocell amplifiers, and amplifiers that combine wide bandwidth, low noise, and low drift.

LF 156 series devices feature low noise (12 mV/Hz), high slew rate (12 V/μs), wide bandwidth (5 MHz), and high input impedance (10^{12} Ω). Average offset voltage is <3 mV, and offset temperature drift is typically 5 μV/°C. Offset adjust does not degrade drift or common mode rejection.

Typical new (old) prices, in 100-piece lots, are: $3.50 ($8.50) for −55 to 125°C temperature range hermetic devices; $2.50 ($6.00) for −25 to 85°C hermetic; and $0.75 ($2.10) for 0 to 70°C epoxy.

Single IC Incorporates All Remote Control Servo Amp Functions

Designed for remote control applications in digital proportional systems as well as in many other closed loop position control applications, the NE544 linear circuit integrates all the basic servo amplifier functions, including the motor drive, into a single IC. The circuit was developed by Signetics, 811 E Arques Ave, Sunnyvale, CA 94086 in cooperation with several manufacturers of radio control equipment to provide designers with greater flexibility in adapting amplifier performance to their particular design needs while keeping components count low.

The resulting device is a combined servo amplifier and pulse width demodulator with internal motor drive transistors. It incorporates a linear one-shot for improved positional accuracy and optional outputs for external motor drive transistors. Although motor drive, deadband, and minimum output pulse are integrated, the device can be modified over a wide range through the use of external transistors or padding resistors.

Design features include internal voltage regulator for improved power supply rejection, or highly accurate monostable multivibrator, and adjustable deadband and trigger thresholds. Operating characteristics are standby power drain of typically <6 mA; 500-mA load current capability; maximum supply voltage of 6.0 V; and high linearity, with 0.5% maximum error.

Circle 362 on Inquiry Card

Second Source Available for BIFET Op Amp

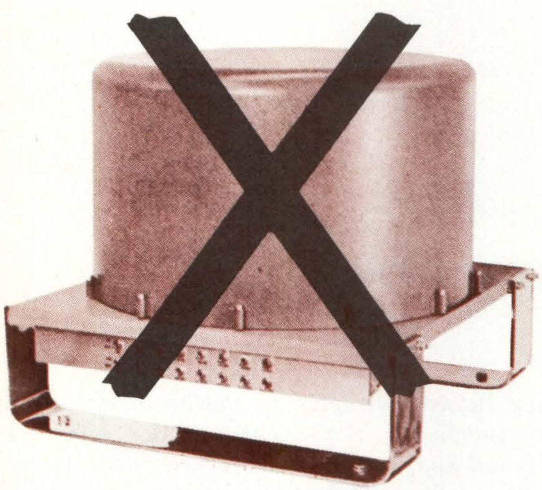
Intersil, Inc, 10900 N Tantau Ave, Cupertino, CA 95014 has entered the BIFET operational amplifier market along with Texas Instruments and Fairchild in second sourcing National Semiconductor's LF 155/156A/155A and LF 355/356A/355A linear circuits. Prices for 100-999 quantities are $2.50 for the LF 355 and 356; $8 for the 155 and 156; $28 for the 155A and 156A; and $15 for the 355A and 356A. All devices are packaged in TO-5 cans. □

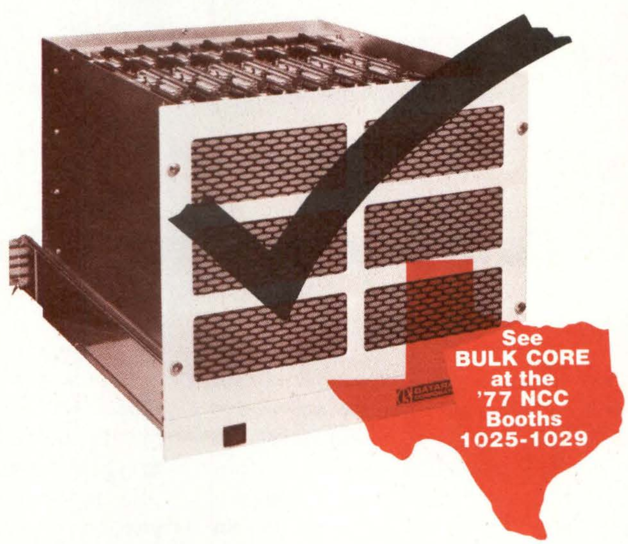
Circle 363 on Inquiry Card


Edelweiss

DEC® RC-11 and RF-11 fixed-head disc...and Data General Novadisc® users:

Replace Fixed-Head Disc with Dataram BULK CORE





Now, all the remarkable features of Dataram's BULK CORE memory system are available to you in a unique storage peripheral with complete interfaces to emulate DEC and Data General fixed-head discs.

Basic building block of this dramatic, new peripheral is Dataram's BULK CORE module, which provides 256 kilobytes of storage on a single board. Eight of these modules can be packaged in a standard 19" chassis to provide two megabytes of storage.

To give you more of what you can't get from fixed-head discs. BULK CORE gives you microsecond-range access time, high reliability, and greatly improved maintainability. And at a price unheard of for core or semiconductor memory. Until now.

Until Dataram made its BULK CORE memory system plug-compatible with PDP-11 and Nova® minicomputers. To provide:

- **Access time 1/10,000 of FHD**
- **High Throughput**
- **Zero Error Rate**
- **Self-Test for Fault Isolation**
- **Hardware & Software Transparent**
- **LED-spotlighted Fault Isolation**
- **256 KB Modularity**
- **Non-Volatile**
- **Non-Mechanical**
- **High MTBF/Low MTTR**
- **Low Power**
- **Parity Check**

Reasons enough to find out more about BULK CORE. If you use a DEC or Data General minicomputer—or any kind—and want to move ahead in performance, move a BULK CORE into your system.

DATARAM CORPORATION
PRINCETON-HIGHTSTOWN ROAD
CRANBURY, NEW JERSEY 08512
TEL:609-799-0071 TWX:510-685-2542

I'd like to learn more about BULK CORE for my
☐ PDP-11 ☐ Nova ☐ ____________
☐ Please send information.
☐ Please have a salesman contact me.

Name ______________________________
Title ______________ Phone ______________
Company ______________________________
Address ______________________________
City ____________ State ____________ Zip ____________

☐ Please send me information about Dataram's ADD-ON/ADD-IN memory for minicomputers.

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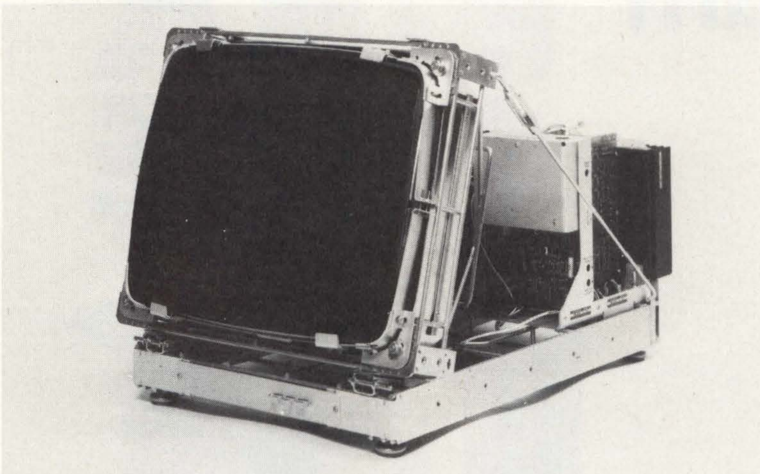
PRODUCT FEATURE

Computer Display Monitor Combines Benefits



# of Both Storage and Refresh Graphics

Two technologies—integrated circuit and cathode-ray tube storage—have now been merged by Tektronix, Inc to provide an OEM-configured 19-in (48-cm) storage-refresh graphics monitor. The first offering in an expected series, the GMA101A allows storage of more than 8500 alphanumeric characters in over 3200 in (8100 cm) of vector.

Capability to combine refresh and storage techniques enables use in applications requiring high information density with moderate user interactivity. Modular nature of the unit and a mix of performance, packaging, and support options permit tailoring by the OEM to meet a number of performance and packaging requirements of varied systems.

Operating Description and Features

Three display modes—store, store-refresh, and non-store—are provided. In *store* all elements of the display are stored on the screen; *store-refresh* is a write-through mode; and in *non-store* the effect of the storage flood guns is disabled. The user can write on the screen but the image is not stored, essentially providing a pure directed beam refresh mode.

Inclusion of a direct view storage tube (DVST), previously supplied by the company only on its end-user graphics terminals and graphics display monitors as a pure storage device, permits display of high density graphics at relatively low computer overhead—since the image is stored on the phosphor of the screen instead of in memory. It also incurs fewer time constraints in the development of graphic programs.

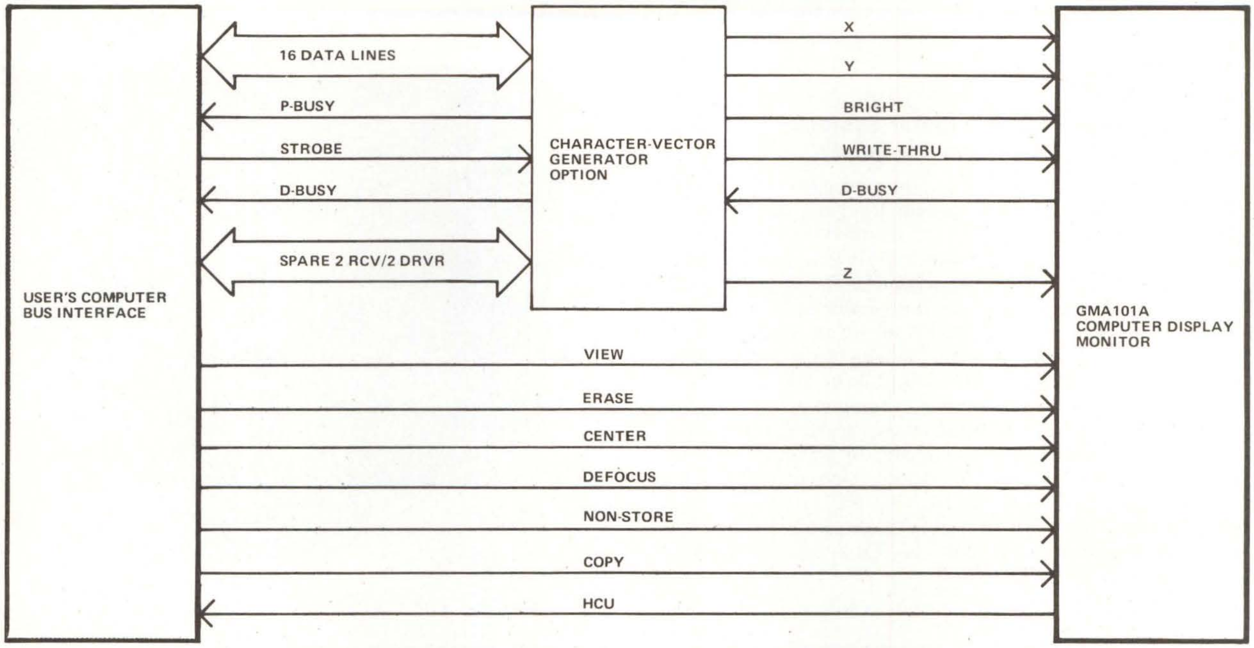
However, it has also previously had the disadvantage of necessitating erasure of an entire image and rewriting when editing was required. This has been remedied by the write-through capability which enables both stored and refreshed information to be stored simultaneously. The technique slightly reduces electron beam intensity at the screen so that the user can write on the phosphor without causing the image to be stored. This is similar to a random refresh screen.

Basic unit modules consist of CRT, low voltage power supply, and card cage—all mounted on a wireform chassis. The CRT module can be oriented either level or tilted back 15 degrees. Line voltage selection can be made in the low voltage power supply by moving internal jumpers. High voltage power supply, Z-axis amplifier, storage board, X- and Y-deflection amplifier board, and mounting slots for three additional option boards are contained in the card cage. Cables can easily be threaded throughout the unit and card cage.

Display functions are view, erase, copy, center, non-store, write-through, bright, defocus, and G-busy. All are completely programmable and TTL-compatible. X-Y inputs are analog and the beam rests at center screen with 0 V applied.

After 112 s of display inactivity, a hold mode stores data at a low brightness to extend storage time; however, the *view* function switches the display back to a full brightness view mode when desired. *Erase* causes a full screen erase, *copy* initiates a hard copy when attached to a printer, and *center* resets the origin shifter that protects the CRT in applications of repeated overwrite operation.

Non-store permits the unit to function as an XY-directed beam display, while *write-through* displays non-stored information on the screen concurrently with stored data. *Bright* and



Example of hardware interfacing simplicity for GMA101A computer display monitor. Character/vector generator—whether supplied by Tektronix or developed by the user—necessitates design by user of a digital interface for particular computer. All normally used signals, as shown, are TTL, negative true, with 74LS241 receiver/drivers.

defocus increase spot size and brightness slightly when necessary. *G-busy* is a signal that can be optionally selected, in place of the Z-axis line, to prevent the display from dropping into hold mode. In addition, *SLU* and *D-busy* status signals inform the system whether or not another function is taking place and, therefore, whether or not to send additional data to the display.

A CRT anti-burn circuit prevents damage to the phosphor if either X- or Y-deflection is lost, and an auto erase cycle wipes the screen clean 30 min after the last Z-axis pulse or view initiate. This eliminates residual images and prolongs CRT life.

Several performance, support, and packaging options are available. One of the support options is a display exerciser for use in designing the unit into a system and for meeting interfacing requirements.

Specifications

Display size on the 19-in (48-cm) DVST is 10.5 x 14 in (26.7 x 35.6 cm). Resolution is 80 picture elements/in (31.5/cm), 133 char/line with 64 char lines. Stored dot writing time is ≤5 μs, stored vector writing rate is 3937 in/s (10 cm/ms), and refreshed vector writing rate (write-through and non-store) is 19,685 in/s (50,000 cm/s), 650 vector inches max (1651 cm) at 30 frames/s. Viewing time is at least 15 min at specified resolution; erase time is 1.5 s ±20%.

Origin (X = 0 V, Y = 0 V) of the deflection amplifiers is center screen ±2%. Sensitivity of X-Y inputs is long axis, ±5.00 V differential, 10 V pk-pk full screen; short axis, 3.75 V differential, 7.5 V pk-pk full screen; both ±2.5% of long axis. Max input voltage is 18 V (dc + peak ac); input impedance is 10 kΩ paralleled by 70 pF. Full screen bandwidth is 5 kHz (−3 dB); slew rate (non-linear) is 5 μs/cm; and settling time is 10 μs to within one spot diameter.

Z-axis amplifier specifications include 50-Ω input impedance, and 50-μs rise time with current limited to a 1-MHz continuous repetition rate. Voltage level is TTL-compatible; LO true (strap selectable to HI true); <0.08-V turn on; at least 2.0-V turn off.

Selectable input power requirements are 90 to 110, 108 to 132, 198 to 242, and 216 to 264 Vac at 48 to 66 Hz. Temperature ranges are 0 to 50°C operating, −40 to 65°C non-operating, at 90 to 95% relative humidity (non-condensing) per MIL-T-28800B. Altitude ratings are 15,000 ft (4572 m) operating, 50,000 ft (15,240 m) non-operating.

Unit dimensions are 16.75″ W x 24.00″ L (42.54 x 60.96 cm). Weight is approx 90 lb (40.8 kg), 130 lb (59 kg) shipping.

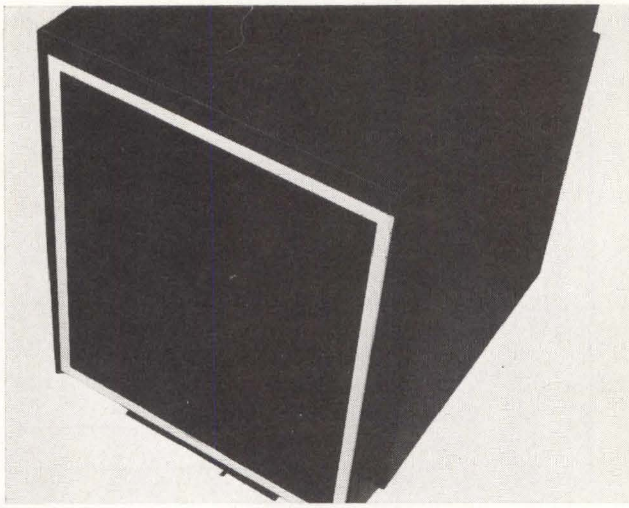
Price and Delivery

A completely stripped down but functionally operational version of the GMA101A (only display tube, power supplies, and X- and Y-deflection amplifiers) costs $4775. Units will be available this month. Tektronix, Inc, Information Display Group, PO Box 500, Beaverton, OR 97077. Telephone: (503) 638-3411.

See at NCC Booth 1354

For additional information circle 199 on inquiry card.

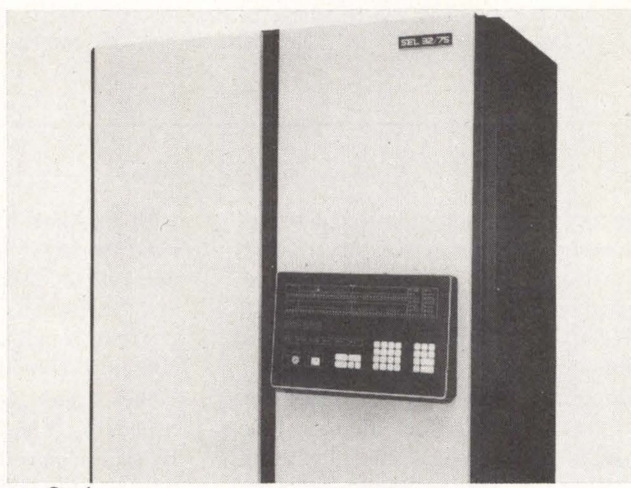
PRODUCTS



Power Distribution to Minicomputer Systems Is Programmable and Designed for Safety

Eliminating problems associated with powering computer systems, the PowerMite MK I isolates the system from the outside world and provides all voltages and currents required by the systems' components. The cost-effective computer peripheral automatically shuts down the system in case of emergency. The 25 x 30 x 30" (63.5 x 76.2 x 76.2 cm) device is reprogrammable to provide different power requirements. Capable of being specified from 5 to 45 kVA, the peripheral is completely shielded; it can accept input voltages of 480, 460, 440, 240, 230, 220, or 208 Vac. Power is fed to an electrostatically-shielded, computer-grade isolation transformer with compensating taps on its secondary to adjust for voltage variation. Up to 30 single-phase, 10 3-phase lines, or a combination, can be run from the device. Output voltages are 3- or 4-wire and ground. Unit weighs from 250 to 500 lb (113.4 to 226.8 kg) depending on kVA rating. **Computer Power Systems Corp,** 3303 Harbor Blvd, Bldg H-5, Costa Mesa, CA 92626.

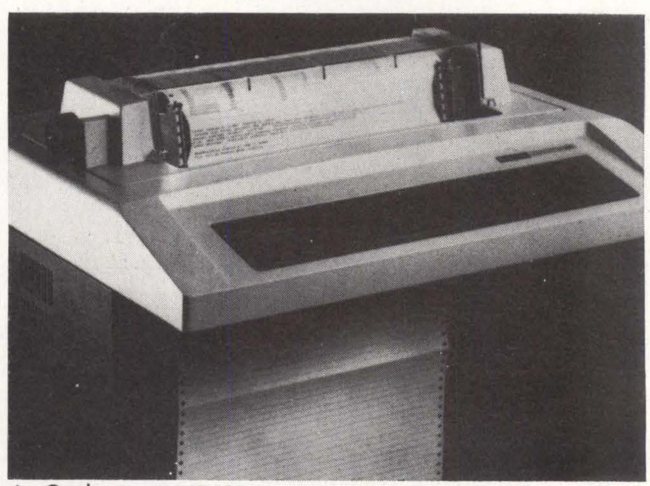
Circle 200 on Inquiry Card



Powerful Computer System Offers Large-Scale Features at Minicomputer Prices

The 32/75 system, an entry into the high performance end of the minicomputer market, has power and architectural features associated with large-scale computers but is priced within the minicomputer range. It combines a 26M-byte throughput with capacity for 16M bytes of mapped main memory. With a word size of 32 bits plus four parity bits, memory has speeds of 600 and/or 900 ns. Expansion increments are 32k bytes at 600 ns and 64k bytes at 900 ns. The 2.4M-byte/s regional processing unit simplifies interfaces to complex devices, distributing many processing tasks to the I/O level. RAM is 4k x 32 bits and p/ROM is 2k x 32 bits. Instruction execution time is 150 ns. In complex processing situations, up to 20 systems can share a common memory pool. High speed floating-point hardware and writable control storage are available as options. Software to handle memory management hardware and I/O controllers will be available with first deliveries. **Systems Engineering Laboratories,** 6901 W Sunrise Blvd, Ft Lauderdale, FL 33313.

Circle 201 on Inquiry Card



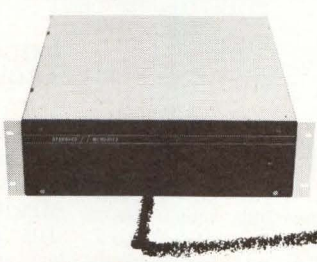
Reliable Keyboard Printer Operates at 1200 Baud for Communications and Interactive Console Uses

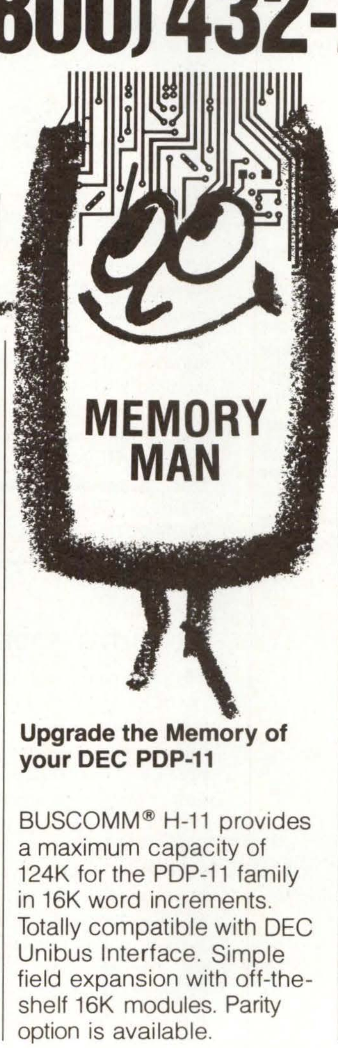
The LS120 DECwriter III is a low cost, interactive hardcopy serial data communications terminal designed for reliable and flexible operation at 1200 baud. Field-proven subassemblies, as well as a microprocessor-based controller board, are incorporated in the device. Std features include a 180-char/s print rate; 110, 300, or 1200 baud plus additional operator-selectable rates up to 9600 baud; 1k-char buffer to minimize throughput; EIA interface; automatic "paper out" switch; last-character visibility; and self-test capability. Printing is 132-col, 10 char/in (4/cm) horizontal, 6 lines/in (2.4/cm) vertical spacing. The 128-char u/lc ASCII set is impact printed with a 7 x 7 dot matrix. Featuring an ANSI keyboard with multikey rollover, the terminal is compatible with full- and half-duplex protocols. Options include a forms handling package, communications package, APL alternate character set, compressed font, and 300-baud integral acoustic coupler. **Digital Equipment Corp, Digital Components Group,** One Iron Way, Marlborough, MA 01752.

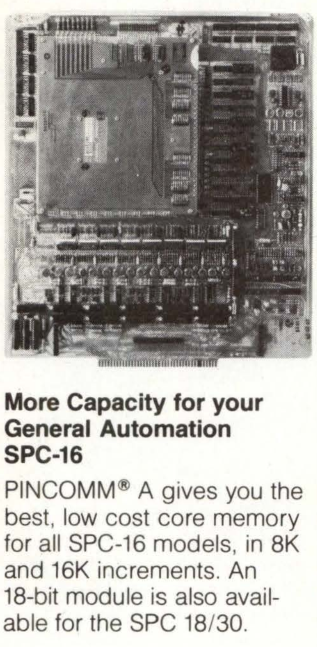
Circle 202 on Inquiry Card

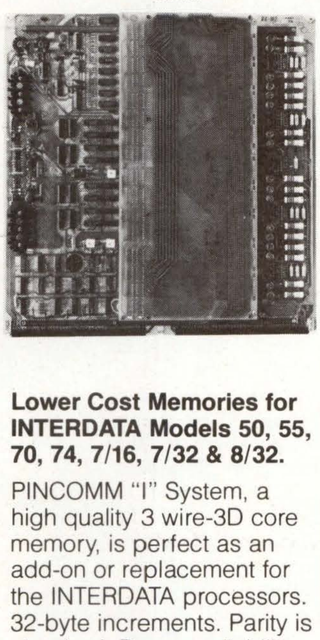
Before You Pay More For Plug Compatible Memory, Call The Memory Man (800) 854-3792.

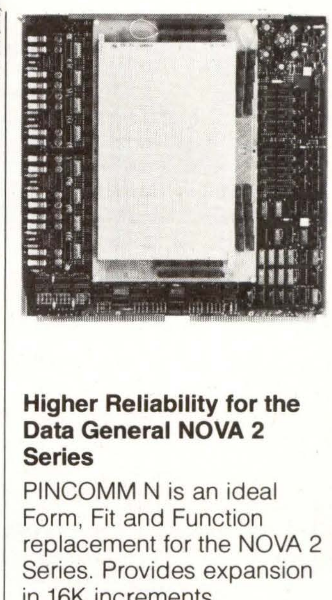
In California, (800) 432-7271.











More Capacity for your General Automation SPC-16

PINCOMM® A gives you the best, low cost core memory for all SPC-16 models, in 8K and 16K increments. An 18-bit module is also available for the SPC 18/30.

Lower Cost Memories for INTERDATA Models 50, 55, 70, 74, 7/16, 7/32 & 8/32.

PINCOMM "I" System, a high quality 3 wire-3D core memory, is perfect as an add-on or replacement for the INTERDATA processors. 32-byte increments. Parity is standard. Proven reliability.

Upgrade the Memory of your DEC PDP-11

BUSCOMM® H-11 provides a maximum capacity of 124K for the PDP-11 family in 16K word increments. Totally compatible with DEC Unibus Interface. Simple field expansion with off-the-shelf 16K modules. Parity option is available.

Higher Reliability for the Data General NOVA 2 Series

PINCOMM N is an ideal Form, Fit and Function replacement for the NOVA 2 Series. Provides expansion in 16K increments.

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AN APPLIED MAGNETICS COMPANY

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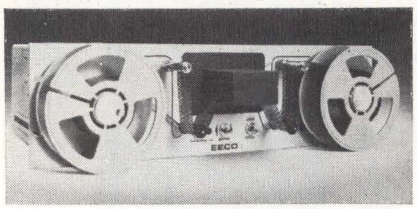
CIRCLE 95 ON INQUIRY CARD

PRODUCTS

PUNCHED TAPE READER/SPOOLER

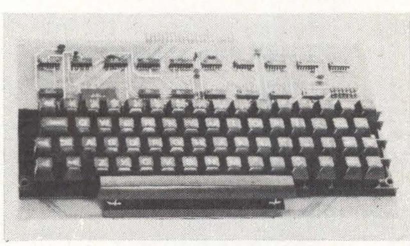


The 2001-4 reader/spooler for numerical and automatic machine control reads bidirectionally at speeds up to 200 chars/s in step or priority interrupt mode, and searches and rewinds at 400 chars/s. The unit can operate in loop or spool mode, reading 5-, 6-, 7-, and 8-level tapes, up to 0.0045" (0.0114 cm) thick, that are at least 40% opaque. The 5.5" (13.97-cm) reels can hold up to 600 ft (183 m) of 2.7 mil (0.0027") tape. **EECO,** 1441 E Chestnut Ave, Santa Ana, CA 92701.
Circle 203 on Inquiry Card

LINEAR IC AUTOMATIC TEST SYSTEM

Designated LTS/5, the high speed system is designed to test linear ICs, as well as diodes, ADCs, and DACs. Power sources are full V/I programmable as constant voltage or current with forcing accuracy of 0.1% and 0.05% measurement accuracy. Numerical data can be converted with 16-bit accuracy in <40 μs. Software supports up to eight stations. System uses a PDP-11 and dual floppy disc unit. Video or hardcopy terminal provides operator interface and 300-line/min printer outputs test results. **Lorlin Industries, Inc,** Precision Rd, Danbury, CT 06810.
Circle 204 on Inquiry Card

ASCII KEYBOARD ENCODER

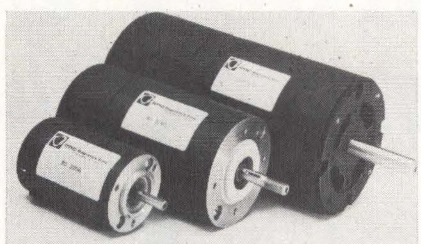


Available in Archer Project-Board kit form, the 63-key keyboard encoder features repeat key to control characters and symbols, a negative- or positive-going data valid strobe, latch outputs, shift and shift-lock capacity, and six extra control keys. Unit has output capacity rate of 833 char/min and repeat key rate of 208 char/min. External power source of 5 Vdc at 500 mA is required. **Radio Shack, a Tandy Corp Co,** 2617 W Seventh St, Fort Worth, TX 76107.
Circle 205 on Inquiry Card

CARTRIDGE TAPE DRIVE

As a 440 System option dedicated to providing low cost dump/restore medium for fixed disc storage, the 4455 high speed tape cartridge drive uses a 4-track, 0.25" (0.635 cm) wide magnetic tape in 3M type cartridge case. Drive is enclosed in a 26 x 11 x 22.5" (66.04 x 27.94 x 57.15 cm) free-standing cabinet. Device can store 5.76M characters and has a R/W speed of 60 in/s (152.4 cm/s) with a 3200-bit/in (1260/cm) recording density, achieved with a double-density encoding technique and a phase lock data separator. **Sycor, Inc,** 100 Phoenix Dr, Ann Arbor, MI 48104.
Circle 206 on Inquiry Card

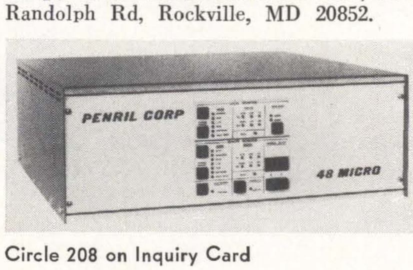
HIGH PERFORMANCE DC MOTORS



Motor for aerospace military and high performance applications is rated for 1 hp at 10,500 r/min, continuous duty, and 2 hp for intermittent duty. Available in series, shunt, or compound wound versions, the 4" (10.16-cm) dia unit includes large brushes and diamond turned commutators for long brush life, and dynamically balanced armature assemblies for extended bearing life. Wound armature and fields permit field control of motor characteristics and speed-torque outputs. **IMC Magnetics Corp,** Eastern Div, 570 Main St, Westbury, NY 11590.
Circle 207 on Inquiry Card

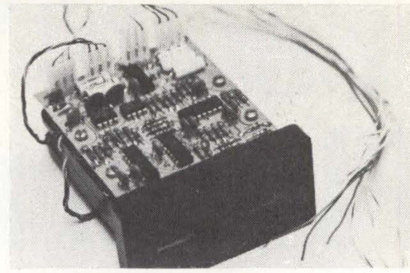
4800-BIT/S MODEM

The self-contained 48 Micro data modem operates at 4800 bits/s for use on point-to-point and multipoint leased lines, and dial networks. Incorporating a 12-bit microprocessor for adaptive equalization, the unit provides diagnostics, meets European CCITT requirements, and is claimed to offer the fastest acquisition time with its Fast Pool option, available on the multipoint version to minimize synchronization of the receiver. A full-duplex 110-bit/s asynchronous secondary channel is used for transmission of diagnostics. **Penril Corp, Data Communications Div,** 5520 Randolph Rd, Rockville, MD 20852.



Circle 208 on Inquiry Card

BADGE READER MODULE

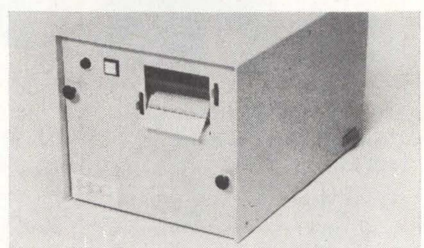


Featuring 12-digit (decimal or hex) data capacity, buffered TTL outputs, 300-μs clock output pulses, and only one moving part (limit switch), the Mark I is a handdriven dynamic card reader. The unit can read mag-stripe ID cards coded with six to 12 BCD or hex digits, and having up to 5 mils of polyester over the stripe. The self-contained module consists of a molded high impact resistant reinforced plastic card guide to which the read head amplifier PC board, card limit switch, and read head are mounted. **R D Products, Inc,** 6132 Rt 96, Victor, NY 14564.
Circle 209 on Inquiry Card

MODULAR DATA ACQUISITION SYSTEM

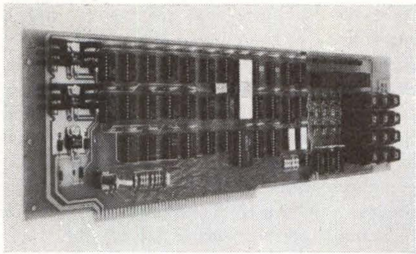
Model MP6912 is offered in 75-Hz versions, replacing 30- and 60-kHz versions; model MP6812 (30 kHz) has been reduced greatly in price, as has the 100-kHz MP6912. Both are self-contained modular data acquisition systems consisting of input multiplexers, high speed sample and hold, and 12-bit ADCs. The MP6912 has 3-state bus outputs for easy interfacing to standard microcomputers. Both feature 0.025% accuracy with low temperature coefficients. **Analogic Corp,** Audubon Rd, Wakefield, MA 01880.
Circle 210 on Inquiry Card

21-COLUMN PRINTER



The 300 series 21-column digital printer is a general-purpose, benchtop printer which includes power supplies and complete control electronics. Standard model accepts up to 14 columns of BCD data and is DTL/TTL-compatible. Incorporating the Hermes-Precisa printhead, the device has a life of 5M printed lines. Two-color printing is accomplished on standard paper rolls, at a rate of 3 lines/s. Up to 12 characters can be selected to print in each column; special characters and symbols can be incorporated for a custom printing format. **Master Digital Corp,** 1308-F Logan Ave, Costa Mesa, CA 92626.
Circle 211 on Inquiry Card

CPU BOARD/FRONT PANEL



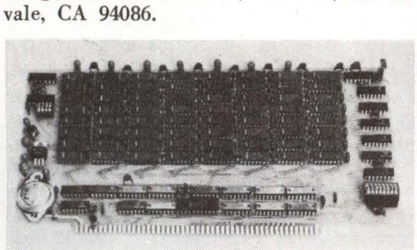
Fully compatible with the S-100 bus, this single board can replace the CPU board and front panel of existing microcomputer systems to achieve minicomputer performance, or form the basis of a custom system, using S-100 bus peripherals and a motherboard. Two operating modes are Slow Step™ which steps through the program at a variable rate from 1k to 65k steps/min, and Control Halt™ which prevents the 8080A CPU from shutting off after a Halt instruction. A 12-pad keyboard and ten 7-segment readouts simplify data logging and examination. **Morrow's Micro-Stuff,** Box 6194, Albany, CA 94706.
Circle 212 on Inquiry Card

LINE PRINTERS

Models 9325 and 9326 printers, furnished with a 132-col print line, are rated respectively at 250 lines/min using a 64-char ASCII font, and 180 lines/min using a 96-char ASCII font. Featuring belt print mechanisms, units are plug-compatible with the company's printers, and may be added to the System 99. Adaptive control logic constantly monitors and adjusts lines for maximum speeds, based upon character content. Dual paper feed tractors are adjustable; max paper slew rate is 30 in/s (76.2 cm/s). **GRI Computer Corp,** 870 Georges Rd, North Brunswick, NJ 08902.
Circle 213 on Inquiry Card

64K RAM BOARD

A fully-tested 64k RAM board meets S-100 computer interface specifications, including those for Altair and Imsai units, and allows memory addition up to 1024k bytes. The 5 x 10" (12.7 x 25.4 cm) PC board contains 64k bytes and has hardware provision for bank switching to add over 1M bytes. It allows memory address to be set in 8k-byte increments and provides hardware-write protection in 16k-byte increments. Voltages are 12 at 300 mA, 5 at 750 mA, and −5 at 1 mA. Cycle time is 500 ns, with 400-ns access time. **Extensys Corp,** 592 Weddell Dr, Suite 3, Sunnyvale, CA 94086.



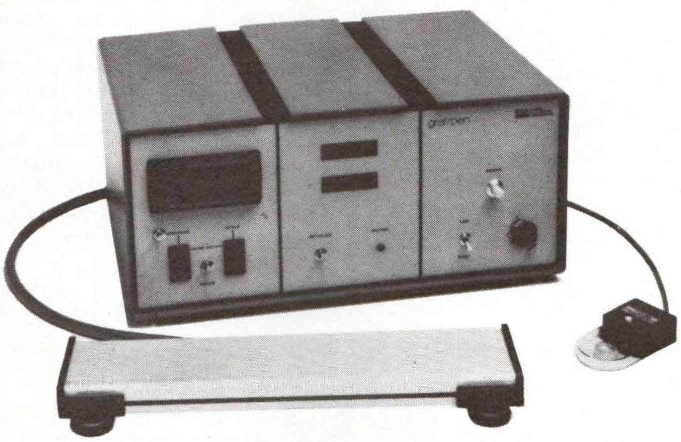
Circle 214 on Inquiry Card

REGULATED POWER SUPPLY

Supplying ±15 V at ±50 mA the model 22-40 regulated modular power supply is claimed to be the smallest of its type. It offers line and load regulations of ±0.1% and noise and ripple of <1 mV in a miniature 6-oz (170-g) package. The unit measures 1 x 1.75 x 2.25" (2.54 x 4.445 x 5.715 cm) and has pins for PC board mounting. Powered by 115 Vac, it can operate over a temperature range of −25 to 70°C. Short circuit protection by foldback current limiting prevents damage from continuous shorting of the outputs to common. **Calex Mfg Co, Inc,** 3305 Vincent Rd, Pleasant Hill, CA 94523.
Circle 215 on Inquiry Card

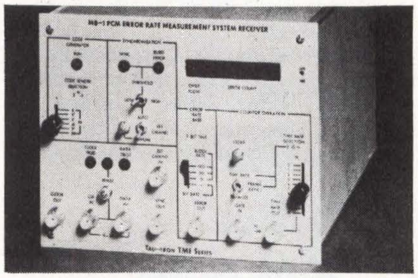
SMALL SYSTEM DISC DRIVE

Proximity recording, disc coating technique, and surface shield are the key features of the 601 OEM fixed media disc storage device designed for small computer systems. Storage capacities are 25M, 50M, or 75M bytes, with a data transfer rate of 885k bytes/s, and an average access time of 32 ms. An option provides 500k to 1000k bytes of fixed head storage. With proximity recording, low mass (0.25 g), low load (10 g) heads operate with disc surfaces, allowing either horizontal or vertical configuration. **Memorex Corp,** San Tomas at Central Expwy, Santa Clara, CA 95052.
Circle 216 on Inquiry Card



PRODUCTS

WORD GENERATOR



MN-1 and MB-1 combine to provide a high performance BERT which operates from 1 to 75M bits/s for use in testing communications channels, twisted pair wires, coaxial cables, or optical fibers. Transmitter is the MN-1 data generator, which generates six switch-selectable pseudorandom sequences from 63 to >1M bits long; receiver section is the MB-1 which will synchronize its internal code generator automatically to the received sequence and make bit by bit error measurements. Error measurements are displayed on a 4-digit LED display. **Tau-Tron Inc,** 11 Esquire Rd, North Billerica, MA 01862.

Circle 218 on Inquiry Card

UNIVERSAL COMMUNICATIONS PRINTER

A microprocessor-based communications controller for the company's series 2000 line printers emulates IBM, CDC, Univac, Honeywell, Burroughs, or any other remote print station. The 2000 is a 200-line/min, 132-col, multicopy data processing printer. Interface provides synchronous or asynchronous data transmission, full- or half-duplex operations, point-to-point or multidrop, speeds up to 9600 baud, 1000-char single or double buffering, full error correction and ASCII or EBCDIC code transmission. Unit is designed for heavy duty continuous runs. **Tally Corp,** 8301 S 180th St, Kent, WA 98031.

Circle 217 on Inquiry Card

DATA DISPLAY LOGGING DEVICE

The ready-to-use Datalogger 1000 with 10 channels is applicable for surveillance and alarm as well as digital data logging. Interchangeable parameter modules provide a variety of measurement capabilities. The instrument furnishes a continuous display of time, channel number, and measured data to 20,000 counts (full 4½ digits) for instant visual analysis. Printout is 2-color hard copy. Selection of ranges and functions, as well as expansion to 100 channels, is possible. **United Systems Corp,** 918 Woodley Rd, Dayton, OH 45403.

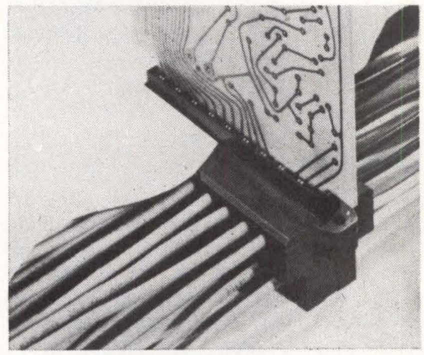
Circle 219 on Inquiry Card

DATA INPUT PERIPHERALS

As table-top units that do not require a controlled environment, the card reader and paper tape reader/punch can be connected to the company's timesharing series 4000 and other terminals. The tab card reader reads std 80-col tab cards punched in Hollerith code, translating it into ASCII communication code. The paper tape reader and punch handles 5-, 6-, 7-, or 8-channel tape, including Mylar and Mylar laminated. Speeds are selectable between 110 and 300 baud. Unit is suited to computer-generated numerical control applications. **Trendata, an Applied Magnetics Co,** 610 Palomar Ave, Sunnyvale, CA 94086.

Circle 220 on Inquiry Card

PCB CONNECTOR FOR 2-SIDED BOARDS



The PCB5 features bifurcated, cantilever PC contacts to provide two contact points for each circuit. Cantilever design cushions board-to-contact mating, and allows frequent removal and insertion of PC boards without scoring printed circuit etching. Contacts are arranged in rows of 18 on each side of the connection socket, providing a total of 36 independent circuits on 2-sided boards. Optional temperature stabilization keeps contacts on each side of the connector at the same relative temperature using electrically insulated copper bars in the connector molding. **Amerace Corp, Control Products Div,** 2330 Vauxhall Rd, Union, NJ 07083.

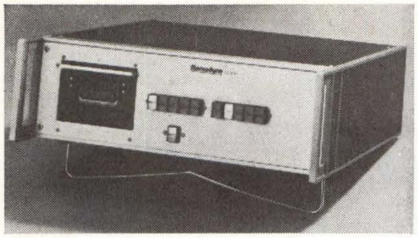
Circle 221 on Inquiry Card

POWER REGULATOR

Designed to prevent malfunction and damage caused by brownouts and other line voltage irregularities, the minicomputer regulator is also intended for use with microprocessors. It is built around the company's sinusoidal constant voltage transformer which corrects for voltage dips and surges. Available for 60-Hz single-phase operation, four models have max ratings of 500, 750, 1000, and 2000 VA, with nominal output of 120 V; five have ratings of 3000, 5000, and 7500 VA, with outputs of 120/240 V. **Sola Basic Industries, Sola Electric,** 1717 Busse Rd, Elk Grove Village, IL 60007.

Circle 222 on Inquiry Card

CASSETTE RECORDER

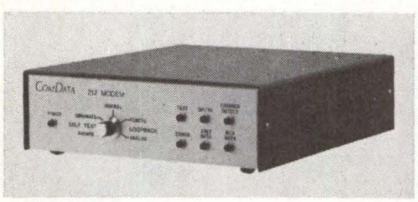


Capable of accepting and transmitting RS-232-C data at up to 9600 baud, the 3783HV read/write recorder is a complete stand-alone system containing a patented high speed continuous transport, control circuits, buffer cards, UART card, power supplies, front panel controls, and I/O connectors. With a storage capacity of up to 150k characters/300-ft (91.44-m) cassette, the unit has four baud rates, a search and rewind speed of 100 in/s (254 cm/s), and an error rate of 1 bit in 10^7. In parallel mode the throughput rate is 1000 words/s. **Memodyne Corp,** 385 Elliot St, Newton Upper Falls, MA 02164.
Circle 223 on Inquiry Card

BAUD RATE CONVERTER

BRC 1200 allows any 10- or 30-char/s RS-232-compatible ASCII terminal with magnetic paper tape, or electronic storage, capable of 120-char/s operation to communicate at 1200 baud. Data may be recorded offline at the lower rate, then connected to the host computer via a 1200 baud full-duplex modem. A 256-char receiving buffer permits sign-on messages and handshaking interaction between the host computer and the terminal keyboard/printer. High speed transmission can then occur between the host computer and storage device. Buffer control is also available. **Western Telematic, Inc,** 3001 Red Hill Ave, Costa Mesa, CA 92626.
Circle 224 on Inquiry Card

1200-BAUD MODEM



Providing full duplex 1200-baud operation over unconditioned lines, the 212 allows 1200-baud synchronous operation, asynchronous operation at 1200 baud, or any integral submultiple rate such as 300 or 600 baud. Full-duplex transmission is achieved using the modulation technique standard to the 2400-baud Bell series 201. Both bandwidth and speed are halved to create two 1200-baud frequency bands. The station originating a call transmits on one band and receives on the other while the answering station operates in the reverse mode. **ComData Corp,** 8115 N Monticello, Skokie, IL 60076.
Circle 225 on Inquiry Card

MULTICOLOR GRAPHIC DISPLAY

The 2 x 2" (5.08 x 5.08 cm) LEDscreen™ display contains 1000 LEDs/in² (155/cm²) to rapidly change and create any multicolor graphic display. Less than 0.25" (0.639 cm) thick including pins, and weighing 2 oz. (56.7 g), the solid-state display has no filament to burn out and can withstand military shock, vibration, and other harsh environments. Display is limited only by its resolution of up to 50 lines/in (19.7/cm); it can show any pattern the CRT creates, with an illusion of smooth, continuous motion. **Integrated Microsystems, Inc,** 1215 Terra Bella Ave, Mountain View, CA 94043.
Circle 226 on Inquiry Card

PDP-8 COMPATIBLE ADD-IN MEMORY

The 8k-word, nonvolatile, plug-compatible add-in memory for the PDP-8/A, /E, /F or /M requires only 0.6 A maximum at 5 Vdc and provides the user with additional Omnibus® slot space and power to drive peripherals. A 4k-word configuration board is also available. The memory achieves improved reliability through extremely low power levels and fewer components. Predicted MTBF is over 60k h or 6.5 years of continuous operation. **Monolithic Systems Corp,** 14 Inverness Dr E, Englewood, CO 80110.
Circle 227 on Inquiry Card

21MX COMPATIBLE ADD-IN MEMORIES

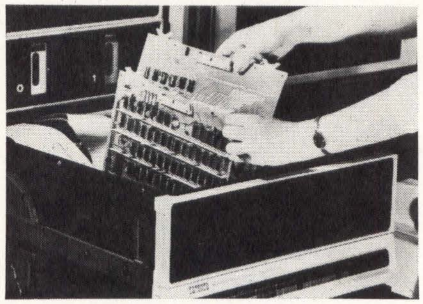
Add-in double-density memory storage cards for use with the H-P 21MX and 21MXE family of computers have a capacity of 16k words of 17 bits each, and are completely compatible with the H-P systems models 2105, 2108, 2112, and 2113. The NS-21 boards are used with a company control card or with the 21MX series control card; one card can communicate with up to 12 16k memory storage cards, for a total storage capability of 192k words. Also available is a depopulated 8k version. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

MICROPROCESSOR CORE MEMORY SYSTEM

The Micro 3800, an 8k x 16 random access core system, interfaces with National's Pace for applications where nonvolatile memory is required in programmable process controllers. Complete with timing, control, decode drive circuitry, and address/data registers on an 8.5 x 11" (21.59 x 27.94 cm) PC card, the memory is designed to mount on 0.75" (1.905-cm) centers. The system features a 400-ns access time, and operates from unregulated voltages typically encountered in industrial environments. It requires inputs of ±15 and 5 V. **Electronic Memories & Magnetics Corp,** 12621 Chadron Ave, Hawthorne, CA 90250.
Circle 228 on Inquiry Card

PRODUCTS

COLOR VIDEO GENERATOR



Designed for use with DEC PDP-11 computers, model 11 color graphics video generator is configured as two quad size boards which plug directly into a DD-11 backplane and operate at main memory speed for fast video update. Unit features std ASCII alphanumerics, paint-up/down bar graphics, reverse video, blink, and 128 microprogrammable (patent pending) symbol graphics. Foreground/background selection in any of eight colors may be made on a char-by-char basis. **Industrial Data Terminals Corp,** 1550 W Henderson Rd, Suite 176E, Columbus, OH 43220.
Circle 229 on Inquiry Card

ILLUMINATED ROCKER SWITCHES

Designed for snap-in mounting, these 3-position switches are available in either spdt or dpdt models with a variety of contact configurations. Rated at 5 A with resistive load at 120 Vac or 28 Vdc; 2 A at 250 Vac, they accept a midget screw base lamp bulb, size T-1½ and 1¾. Actuator lens is removable from the front for easy bulb replacement, and a separate lamp circuit provides added flexibility. Lens colors are white, red, orange, yellow, and green. **Raytheon Co, Distributor Products Operation,** Fourth Ave, Burlington, MA 01803.
Circle 230 on Inquiry Card

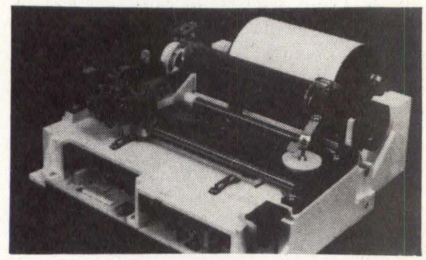
PORTABLE MODEM TESTER

The self-contained 7914B simulates data communication control functions, evaluates system performance, and isolates equipment failures. Testing either synchronous or asynchronous modems in simplex, half-duplex, or full-duplex mode, the unit determines overall condition of a data channel consisting of a telephone line with a modem at each end. The tester transmits a 511-bit pseudo-random test pattern and measures the bit error rate of the received signal. A 2-digit display indicates the bit error count up to 99 and another shows when it exceeds 99. **Tele-Dynamics Div of Ambac Industries, Inc,** Fort Washington, PA 19034.
Circle 231 on Inquiry Card

MINIATURE SPARK GAP SOCKET

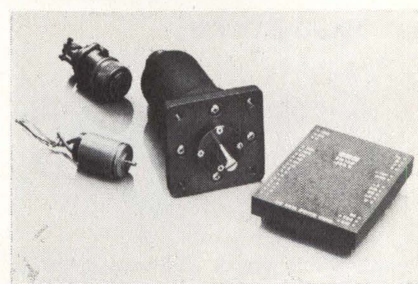
Type 546, a 7-pin socket with a spark discharge device, prevents damage to CRTs from voltage surges and circuitry breakdown. The device mates with JEDEC E7-91 tube base having 0.040" (0.10 cm) diameter pins on a 0.375" (0.95 cm) pin circle. If desired the socket is available without the spark gap. Spark or arc gap material is UL/FR approved copper clad laminate and never needs replacing. Molded thermoplastic socket material is also UL/FR approved. **Connector Corp,** 6025 N Keystone Ave, Chicago, IL 60646.
Circle 232 on Inquiry Card

DOT MATRIX PRINTER



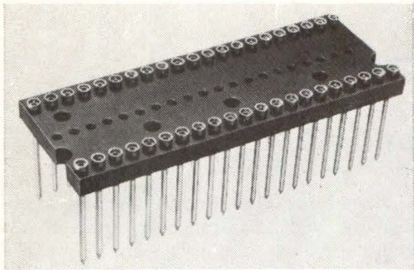
Powered by a single 12 Vdc supply, the DX486 produces up to 40 columns of alphanumeric or graphic information. Characters are 0.11" high x 0.08" wide (0.28 x 0.20 cm) using a 7 x 5 matrix. Printer produces 40 characters in a 4" (10.16 cm) space on 4.5" (11.43 cm) paper, with a reversible ribbon. Two additional copies can be made using self-acting paper or carbon. Paper advance allows continuous printing of dots, one under the other for producing graphics. **Amperex Electronic Corp, Hicksville Div,** 230 Duffy Ave, Hicksville, NY 11802.
Circle 233 on Inquiry Card

INDUSTRIAL SHAFT-ANGLE ENCODER



The EN 100 encoder continuously measures the angular position of machine shaft and produces both BCD digital and analog output representing shaft angle and velocity, respectively. Device employs tracking converter with type II servo loop and high level CMOS logic for absolute position measurement for input rates to 100,000 counts/s. An 11- to 17-Vdc main supply and a logic supply are required with total power consumption of 33 mW typ. **ILC Data Device Corp,** Airport International Plaza, Bohemia, NY 11716.
Circle 234 on Inquiry Card

LOW PROFILE DIP SOCKETS



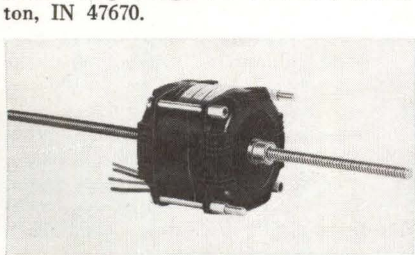
Containing from four to 116 pin sockets, the 0.125" (0.318-cm) DIPs have a header body made of FR-4 glass epoxy, offering UL acceptance as well as withstanding acids, fluxes, and cleaners. DIPs withstand the same heat, moisture, electrical, tensile, elongation, and other requirements as the PC board. The 800 series offers precision-machined wirewrap sockets or dummies, solder tail posts, solder cup, feed-through and bifurcated pins in gold plate over nickel plate or electrolytic tin plate. **Excel Products Co,** 401 Joyce Kilmer Ave, New Brunswick, NJ 08903.
Circle 235 on Inquiry Card

DC-DC REGULATED CONVERTERS

Series L regulated dc-dc converters are available in single and dual outputs, 3 W out. Power supplies come in several output voltages (fixed ±1%) and load currents. Low weight (<100 g) enables onboard applications. Features include input filtering and a short circuit protection. Specs include 150-Vdc isolation (input to output); 60% typ efficiency, low E_{in}; 100% encapsulation; ±0.05% line regulation; ±0.2% load regulation; and −55 to 100°C storage temperature. **Wall Industries Inc,** 175 Middlesex Tpk, Bedford, MA 01730.
Circle 236 on Inquiry Card

LINEAR MOTION MOTOR

A permanent magnet synchronous or stepper reversible motor, the model LA is suitable for applications requiring accurate linear motion. Specs include thrust, 10 lb; thread, 0.25" (0.635 cm) dia, 8" (20.32 cm) length, standard Acme thread, 16 threads/in (6/cm). Case length is 2.125" (5.4 cm), diameter 2.375" (6.03 cm). Synchronous operation is 0.3125 in/s (0.794 cm/s). The unit is available with bifilar coils for stepper applications providing 768 steps/in (302/cm). Voltage is 115 Vac, 60 Hz, 7.5 W, with reversible rotation. **Hurst Mfg Corp,** PO Box 326, Princeton, IN 47670.



Circle 237 on Inquiry Card

PROCESS CONTROL D-A CONVERTERS

A series of D-A signal converters can be customized in OEM quantities for process control applications requiring temperature and long term stability. Providing medium-to-high resolution, CY2547 and CY2647 offer 2- and 3-digit BCD, respectively; CY2047, CY2147, and CY2247 offer 8-, 10-, and 12-bit resolution, respectively. Std features include stable thin film resistor networks, guaranteed monotonicity, linearity of ±½ LSB from 0 to 70°C, (±¼ LSB at 25°C), low scale factor drift, low zero offset drift, and DTL/TTL compatibility. **CPS, Inc, Converter Products,** 722 E Evelyn Ave, Sunnyvale, CA 94086.
Circle 238 on Inquiry Card

LINE SURGE PROTECTOR

Defense of sensitive electronic equipment from destructive line voltage surges and spikes is provided by the ac line surge protector. This unit contains a surge suppressor which absorbs energy from transients that exceed the protection level, and a ferrite filter which suppresses spikes and transients that fall below the level of the protector. Power line hash, glitches, and interference are reduced to a minimum. Models are available for 20-A loads on 117-Vac branch circuits, 2- and 3-pin. **Dyma Engineering,** 213 Pueblo Del Sur, PO Box 1697, Taos, NM 87571.
Circle 239 on Inquiry Card

WAVEFORM AND DATA ANALYSIS SYSTEM

The N12001A waveform and data analysis system is an expanded version of the programmable, digital oscilloscope with additional capabilities of nine added frequency domain operators, and 17 additional directly addressable, operable, and displayable floating point registers. Five transcendental operators are also available, as well as a statistics package with linear regression, mean, and standard deviation; and cursor search routines for searching left and right. **Norland Instruments,** Norland Dr, Fort Atkinson, WI 53538.
Circle 240 on Inquiry Card

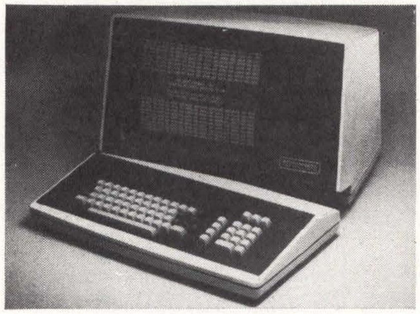
DOT MATRIX IMPACT TABLE PRINTER

Presenting flexible symbol-generating capabilities, design simplicity, easy interfacing, and low noise, model 7022T printer features 22-col capacity at 12 char/in (4.7/cm), 1.58 lines/s, 1.86" (4.72-cm) print line capacity, and top of form sensor option, and accepts multicopy forms up to 0.015" (0.38 mm) thick. Unit uses printing element of seven print solenoids and wires; external electronics generate print pulses to solenoids to form character fonts and densities. Max size is 6.4 x 6.85 x 4.62" (16.26 x 17.40 x 11.73 cm). **C. Itoh Electronics, Inc,** 280 Park Ave, New York, NY 10017.
Circle 241 on Inquiry Card

CIRCLE 100 ON INQUIRY CARD

PRODUCTS

SWITCHABLE INTERFACE OPTION FOR CRT TERMINALS



Allowing external switch-selection of either RS-232 or 20-mA current-loop interface, option for the company's 2480 terminals allows only one interface to be enabled at any time, depending on the setting of the switch. If the RS-232 interface is selected, input and output current loops are maintained through the AUX1 connector, but the terminal will not accept data from or send data on the current loops. If the 20-mA interface is selected, RS-232 outputs RTS and DTR remain at space, but data output is held at mark and data input is ignored. **Ann Arbor Terminals, Inc,** 6107 Jackson Rd, Ann Arbor, MI 48103.
Circle 242 on Inquiry Card

ASYNCHRONOUS MULTIPLEXER

Each of the 16 I/O channels includes nine status indicators for monitoring system status of the PI 510 multiplexer. Functions monitored include data in, data out, and std control signals for 103 and 202 series data sets. The device is functionally equivalent to and software-compatible with DEC's DH11 with modem control. Built-in fault indicators identify failed channel modules. Modem interfaces are available at mixed rates to 9600 bits/s. **Infotron Systems Corp,** 7300 N Cresent Blvd, Pennsauken, NJ 08110.
Circle 243 on Inquiry Card

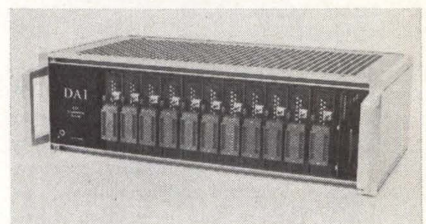
HEX BREADBOARDS

A line of breadboards in the hex pattern is designed for compatibility with DEC PDP-11 and -8/A minicomputers, to facilitate development and expansion of mini-based systems. The boards are all FR-4 glass epoxy with electroplated solder circuits and gold connector tabs. A variety of configurations and options are available including extender boards with sockets, wirewrap boards, breadboards for LSI and SSI use, and I/O transfers. **Douglas Electronics, Inc,** 718 Marina Blvd, San Leandro, CA 94577.
Circle 244 on Inquiry Card

DYNAMIC MEMORY BURN-IN SYSTEM

Designed for high density burn-in of all memory and microprocessor devices, dynamic systems and device trays can also perform static burn-in concurrent with or exclusive of dynamic burn-in. Each system includes power supply and control console with integral system fault interlocking circuits. Feedthrough backplane allows device trays inside the oven to be interfaced directly to exerciser cards outside the oven. Since cards and devices are in close proximity, signal paths are short and signal integrity is maintained. **Wakefield-Systems, a div of Wakefield Engineering, Inc,** Wakefield, MA 01880.
Circle 245 on Inquiry Card

MULTIPLE-p/ROM PROGRAMMING SYSTEM

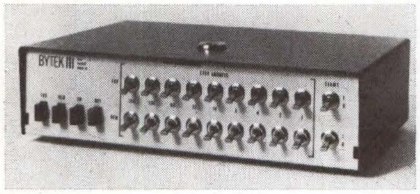


Based on the DCE-2 microprocessor, DCE-MPRG simultaneously programs ten 2708 EPROMs in 200 s. Full paper tape I/O and memory commands include instructions for production programming and for data manipulations. Microprogram automatically performs compare operation after programming and lists errors if any. 2k EPROM and 2k RAM are available to the user for use in implementing custom functions. **N. V. Data Applications International S. A.,** Dreve des Renards 6, Bte 8, 1180 Bruxelles, Belgique.
Circle 246 on Inquiry Card

LOW FREQUENCY CRYSTAL OSCILLATORS

Low cost versions of crystal oscillators operating at 10, 32.768, and 100 kHz are claimed to be the only ones that can be packaged in TO-5 cans. The oscillator includes a company crystal, chip CMOS amplifiers mounted on thin-film substrate, chip capacitors, and resistors. Supply and calibration voltages for the LQXO-3 are both 5 $\pm$0.5 Vdc. Supply current required at 250-kHz and 5-V calibration voltage is 150 μA into a 10-pF and 10-MΩ load. Shock resistance is 1000 g for 1 ms with 0.5 sinewave shock input. A tuning fork configuration of the crystal provides ruggedness. **Statek Corp,** 512 S Main, Orange, CA 92668.
Circle 247 on Inquiry Card

DISC PROTECT SYSTEM



For use on Wang and Diablo disc-based systems, model 22 disc protect system allows users to protect either fixed and/or removable portions of the disc drive, or through switch selection, a given data field beginning at any user designated address. Unit responds with an error message when attempt is made to write in protected field. It utilizes the disc drive power supply, thus eliminating the need for additional power supplies. **Bytek, Inc,** PO Box 1413, Nashua, NH 03061.
Circle 248 on Inquiry Card

SINGLE MODULE 12-BIT DAC

The low cost DAC-DG 12B consists of a digital input register, 12-bit current DAC, stable zener reference circuit, deglitching switch, and an output op amp in a 4 x 2 x 0.4" (10.16 x 5.08 x 1.016 cm) module. Voltage output gives a 10-V change to 1 LSB within 600 ns and to 1% within 250 ns. For changes of ±4 LSBs the time is 100 ns with an update rate of up to 10 MHz. Max output glitch amplitude is ±2 LSBs and glitch voltage-time area is 250 mV/ns. Three output ranges are 0 to −10 V, ±5 V, and ±10 V. Two models accept complementary binary and offset binary coding, or 2's complement coding. **Datel Systems, Inc,** 1020 Turnpike St, Canton, MA 02021.
Circle 249 on Inquiry Card

ENVIRONMENT-SEALED SWITCHES

Available in 500 std variations H11 series switches feature a building block approach to switch expansion, allowing custom design by choice of header type, circuit arrangement, actuator style, termination configuration, and wire lead length. Consisting of small basic switches enclosed in a sealed cylindrical tube with a threaded mounting bushing at one end and wire leads or connectors at the other end, devices are rated at 28-Vdc and 24-A inrush, 4-A motor, 7-A res, and 4-A ind. Temp range is 65 to 185°F. **Control Switch, a Cutler-Hammer Co,** 1420 Delmar Dr, Folcroft, PA 19032.
Circle 250 on Inquiry Card

SPECTRUM ANALYZER

Combining four capabilities in a single instrument, FFT 512/S series III is a real-time narrow-band spectrum analyzer covering the 0- to 100-kHz range. It also performs 1/3- and full-octave analysis, both implemented by banks of precise digital filters, and provides tunable rms voltage/power measurements displayable as V rms (V rms)², and db V (relative to 1 V or to a selected reference). This combination enables the unit to provide 27 modes of operation. Analysis ranges are selectable from dc-20 Hz to dc-100 kHz, and input signal range is from 0.33 μV to 32 V rms. **Rockland Systems Corp,** 230 W Nyack Rd, West Nyack, NY 10994.

Circle 251 on Inquiry Card

BAR CODE READER

Plug-compatible with most CRTs and other asynchronous communications terminals, the model 9210 offers dual connectors for ease of interface to allow tandem operation with any online RS-232-C equipped terminal. External switches allow selection of baud rate, parity, and half- or full-duplex mode. The unit is compatible with bit serial rates from 110 through 9600 baud. The Ruby Wand® lightpen reads bar codes, bidirectionally scanning them at 3 to 50 in/s (7.62 to 127 cm/s). Messages of 32 char (std) or 64 char (optional), can be read. **Interface Mechanisms, Inc,** 5503 232nd St SW, Mountainlake Terrace, WA 98043.
Circle 252 on Inquiry Card

PRODUCTS

THERMAL PRINTER

ANP-9 panel mounting thermal numeric printer provides seven numeric columns (or six with a plus/minus sign) and two columns of engineering symbols, characters, and letters for proper data identification. Electronics provide interface to digital panel meters. Print rate is 2.5 lines/s. Features include the use of only one moving part, (the paper drive motor) and quiet operation. Printer measures approximately 3.75 x 6 x 9" (9.525 x 15.24 x 22.86 cm), and weighs 6 lb (2.72 kg). **Gulton Industries, Inc, Measurement & Control Systems Div,** East Greenwich, RI 02818.
Circle 253 on Inquiry Card

ASCII TEST PATTERN GENERATOR

For modem, printer, and video terminal testing in production and in the field, the "Fox Box" generates the std "quick brown fox" message in both parallel and serial form with the parallel output consisting of the seven lines necessary for std ASCII chars and a data available line. All parallel signals are TTL-compatible. Three serial outputs are provided: RS-232-C, 20-mA current loop, and TTL. Both parity and number of stop bits are switch selectable. An internal bit rate generator is also controllable from the front panel. Baud rates of 110 and 300 are std. **Syntest Corp,** 169 Millham St, Marlboro, MA 01752.
Circle 254 on Inquiry Card

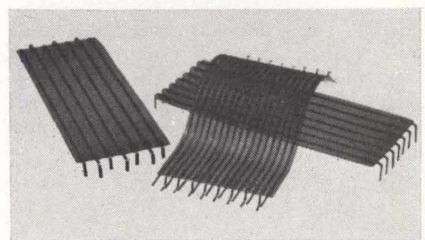
BACK-LIGHTED DIGITIZERS

Back-lighted digitizers with 11 x 11" (27.94 x 27.94 cm), 14 x 14" (35.56 x 35.56 cm), and 22 x 22" (55.88 x 55.88 cm) active surface areas feature 1000-line/in (394/cm) resolution, and ±0.01" (±0.254 mm) standard accuracy with ±0.005" (± 0.127 mm) optional. Device offers the capability of accurately tracing x-rays and other negatives to convert them into computer or calculator language for processing. Digitizing is achieved by tracing the desired graphics with the pen or optional 12-button cursor. **Talos Systems, Inc,** 7419 E Helm Dr, Scottsdale, AZ 85260.
Circle 255 on Inquiry Card

VMOS PERIPHERAL DRIVERS

Containing 12 types, the S55V01/S75V01 and S55V02/S75V02 series of power peripheral drivers are fabricated with the vertical MOS field-effect transistor technology. They provide continuous current ratings up to 2.0 A, standoff voltages to 90 V, and power dissipation ratings of 25 or 4 W in military and commercial temp ranges. Key features include greater current switching capability and higher speed than other drivers, immunity to current hogging and secondary breakdown damage, and CMOS as well as TTL and MOS compatibility. **Siliconix, Inc,** 2201 Laurelwood Rd, Santa Clara, CA 95054.
Circle 256 on Inquiry Card

FLEXIBLE PC JUMPER CABLES

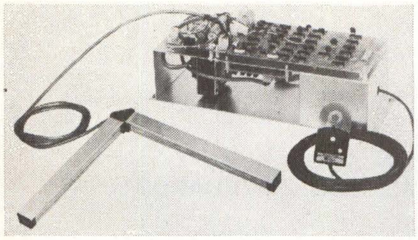


"Sculptured™" cables are PC board interconnection devices with conductors and integral terminals that appear to be carved to the user's specs. Unlimited choice of terminations allows one end of the jumper to be terminated in a series of lugs and straight fingers, and the other in staggered right angle fingers. Completely integral fingers, lugs, or other termination eliminates problems of possible cold solder joints or defective connections. Terminals may be as stiff as required. **Advanced Circuit Technology, Inc,** Congress Industrial Pk, Merrimack, NH 03054.
Circle 257 on Inquiry Card

SWITCHING POWER SUPPLY

A 20-kHz switching power supply, producing 5 V at 120 A, delivers 600 W without paralleling power transistors. Model 712 comes in a 3.5 x 8 x 13" (8.89 x 20.32 x 33.02 cm) package producing 1.6 W/in^3 (0.098 W/cm^3) due to its 75% efficiency. It has 115/230-Vac input, 47-60 Hz. 208-Vac inputs and 400-Hz operation are also available. Brown-out protection to below 95 Vac is included. Units can be paralleled simply by connecting outputs. All units have short-circuit and overvoltage protection. **RO Associates, Inc,** 3705 Haven Ave, Menlo Park, CA 94025.
Circle 258 on Inquiry Card

SONIC DIGITIZER PACKAGE

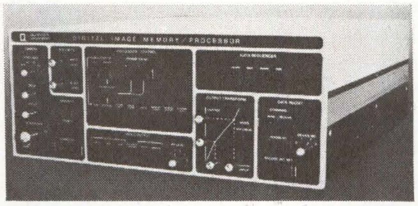


GP-211 employs two sensors mounted on a rigid aluminum L-frame up to 60" (152 cm) long. Sensor assembly can be moved without recalibration or realignment. Outputs are in binary form and are compensated to correct for differences in the speed of sound because of air temp variations. The unit generates 140 points/s and 100 points/in (10 points/mm). Supplied with the digitizer are stylus or cursor; electronics package consisting of logic board, pulse generator, and temp compensation board; and two mounted sensors. **Science Accessories Corp,** 970 Kings Hwy W, Southport, CT 06490.
Circle 259 on Inquiry Card

INSTRUMENT/BUS INTERFACE COUPLER

The microprocessor-based model 4880 couplers allow programmable benchtop instrumentation hardware built within the last five years to be interconnected to IEEE 488 compatible terminals or programmable calculators to form testing and measuring systems. They contain bus drivers, microprocessors, and memory needed to convert ASCII coded data to BCD or straight binary formats. Three versions of the data coupler are a talker, listener, and talker/listener. **Fairchild Camera and Instrument Corp, Instrumentation and Systems Group,** 1725 Technology Dr, San Jose, CA 95110.
Circle 260 on Inquiry Card

ONLINE IMAGE MEMORY/PROCESSOR



The model DS-12 digital image memory/processor performs difficult image detection, recording, processing, and display functions in real time. The unit combines fast A-D conversion, RAM, and arithmetic unit under microprocessor control. It has input/output ports for TV-compatible analog signals and random-access digital I/O capabilities for simultaneous use via a memory timesharing technique. Resolution is 256 x 256. **Quantex Corp,** 1011 Commercial St, San Carlos, CA 94070.
Circle 261 on Inquiry Card

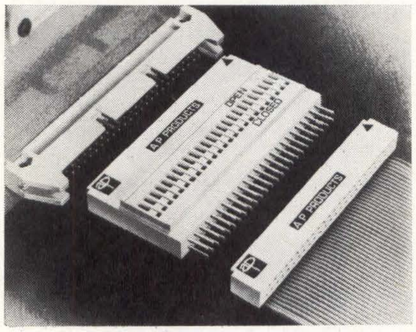
CHANNEL INTERFACE

Designed to handle all high speed line sequences required when transferring data and status between a peripheral device controller and either the IBM 360/370 multiplexer or selector channels, the 3837 reduces IBM interface problems to a simple request/response I/O function which may be controlled by hardwired logic, microprocessor, or minicomputer. Channel interface may be programmed to any number of channel addresses; device controller interface incorporates a std TTL voltage level, a 16-bit input bus, and a 16-bit output bus. **Information Products Systems, Inc,** 6565 Rookin, Houston, TX 77074.
Circle 262 on Inquiry Card

p/ROM-RAM QUAD CARDS

The 20-108 series of DEC PDP-8/E compatible p/ROM-RAM cards provide up to 2k of reprogrammable ROM and up to 2k of RAM on a single quad board. Card has provision for a total of 4k 12-bit words of memory. RAM starts at the first word in the field and is in 256-word modules up to 2k; ROM is in 1k-word increments starting at the mid-point of a field. Jumpers on the p/ROM-RAM card position the card starting address from field 0 to field 7. **Applied Data Communications,** 1509 E McFadden Ave, Santa Ana, CA 92705.
Circle 263 on Inquiry Card

FLAT CABLE SYSTEM TEST SWITCH

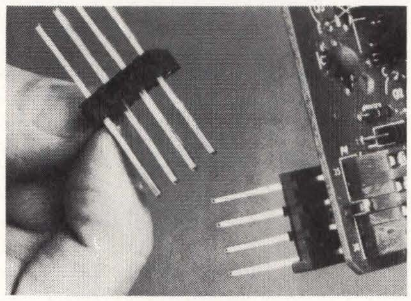


Intra-Switch™ comes in 20-, 26-, 34,- 40-, or 50-contact widths. It has a female connector at one end, a male at the other, and line-by-line discrete switching in between. It can plug directly into the line at any point where a connector is incorporated into the ribbon jumper system. Then, as a probe point or pen point moves each switch toward the molded in open or closed label, each line is selectively opened or closed. **A P Products, Inc,** Box 110, 72 Corwin Dr, Painesville, OH 44077.

Circle 264 on Inquiry Card

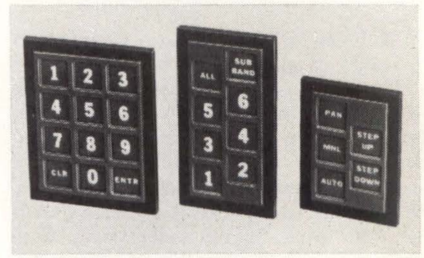
MINIATURE PCB CONNECTORS

The Term-Acon line of connectors includes the series 1000 with 0.025" (0.0635-cm) square pin headers, PC mounted connectors and crimp connectors on 0.100" (0.254-cm) centers. Series 2000 utilizes 0.045" (0.114-cm) square pins on 0.200" (0.508-cm) centers. Series 3000 provides a building block modular approach to interconnections with either 0.045" (0.114-cm) round or square pins on 0.156" (0.396-cm) centers. Dielectric strength between adjacent terminals is 1500 V rms (60-s duration) and max rated voltage is 250 Vac. **Methode Electronics, Inc,** 1700 Hicks Rd, Rolling Meadows, IL 60008.



Circle 265 on Inquiry Card

INDUSTRIAL AND MILITARY KEYBOARDS

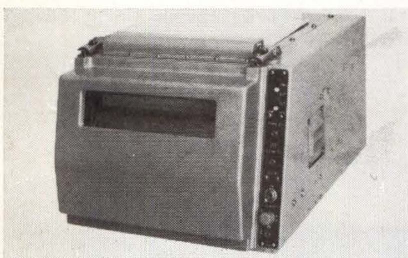


MK series 5-, 8-, and 12-key Wild Rover® keyboards are designed for industrial use while MKM series are appropriate for military applications. The rugged touch switch assemblies are produced of lightweight material. A fiberglass-reinforced high impact housing, epoxy glass PC board, and Lexan overlay are laminated together to form a monolithic assembly well protected against harsh environments. The spst NO switches have a life expectancy of 1M operations. Switch design requires no additional power supply. **Refac Electronics Corp,** PO Box 809, Winsted, CT 06098.

Circle 266 on Inquiry Card

MILITARIZED HIGH SPEED LINE PRINTER

Designed to meet military requirements, HSP3609-212A is suited for shelter and confined space operation. Unit features switch selectable 80- or 132-col printout, and provides 64, 96-, or 128-char ASCII alphanumeric subset plus graphics capability at speeds to 400 lines/min. Incorporating 14 voice coil transducers and a rotating helical scanner, unit generates 9 x 7 dot matrix pattern. Lower case characters, foreign alphabets, and custom graphics are provided in 9 x 9 matrix pattern via EPROM programming. **Miltope Corp,** 9 Fairchild Ave, Plainview, NY 11803.



Circle 267 on Inquiry Card

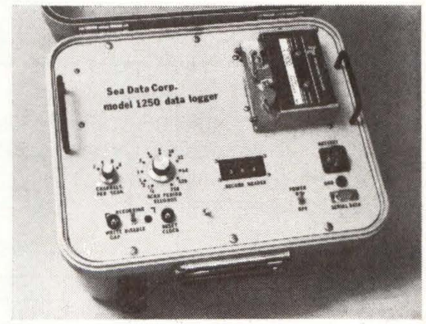
UNIVERSAL EMULATING TERMINAL SYSTEM

Containing a 15" (38-cm) diag display screen and 126-station keyboard, the 700/UETS terminal can communicate with most minicomputers and emulates many terminals. Via the 12-bit microprocessor, unit has resident data line discipline and protocol as well as forms and data handling software routines, making it plug-to-plug compatible. Program storage system, comprised of MOS p/ROMs or RAM loaded from diskettes, stores all operating parameters and telecommunications routines. **Megadata Corp,** 35 Orville Dr, Bohemia, NY 11716.

Circle 268 on Inquiry Card

PORTABLE DATA LOGGER

Lightweight, all-weather, battery-operated systems have operating speeds of up to 32 samples/s and storage capacities that exceed 10M bits on a std 300-ft (90 m) Philips-type digital cassette. An 8-phase driver for the high resolution stepping motor in the incremental tape recorder enables high scanning rates. The recorder allows an 8-channel scan interval of 250 ms, and can record 536k 12-bit data words, plus 67k 36-bit heads (including elapsed time). **Sea Data Corp,** 153 California St, Newton, MA 02158.



Circle 269 on Inquiry Card

PRODUCTS

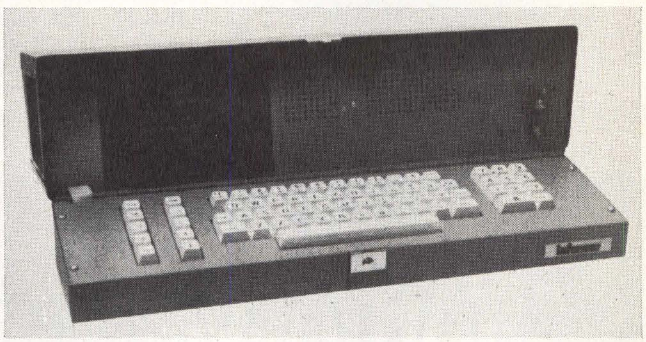
OCR READER

Model 501 optically reads alphanumeric printed price tags and automatically inputs the data to electronic cash registers where they are visible to the customer. It also logs the transaction transmission to a computer station or network that interfaces with inventory control. The lightweight handheld reader measures

4 x 3.5 x 1" (10.2 x 8.9 x 2.5 cm) and is connected to the control unit by a 10 ft (3 m) retractile cable. Under normal conditions with std OCR-A print specs, read rejects will be <1% and substitutions will be <0.01% The eye of the unit is a full 0.5" (1.3 cm) high to maximize ALT and ICI advantages in terms of drift angle and skew. Depth of field is 0.125" (0.318 cm) and read speed is 3 to 13 in/s (7.6 to 33 cm/s) (30 to 130 char/s). **Caere Corp,** 345 E Middlefield Rd, Mountain View, CA 94043.

Circle 270 on Inquiry Card

PORTABLE CRT DISPLAY TERMINAL



Providing mobile communications capability with virtually any computer system for temporary local or remote data access, the P300 portable visual display uses the same basic keyboards and CRT displays as the company's std line of terminals but is configured for easy carrying and setup in field situations. The unit contains a 5.5" (14 cm) CRT screen and control electronics in its primary cabinet, with a foldout keyboard connected by flat cabling. Keyboard may have std alphanumeric keys only, or optional numeric pad and function keys. Control electronics may be either in std character-interactive mode, in polled block mode, or for use under microprocessor control. **Informer, Inc,** 8332 Osage Ave, Los Angeles, CA 90045.

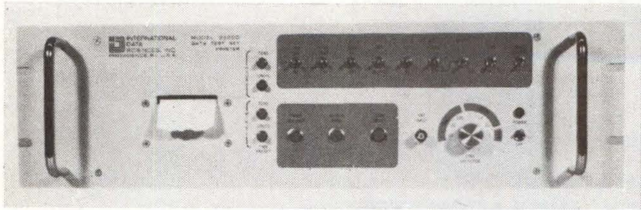
Circle 271 on Inquiry Card

MINICASSETTE TAPE TRANSPORT

Model CM 600 Mini Dek, measuring 3.5" (8.9 cm) sq and less than 2.5" (6.4 cm) deep, contains all motor control and read/write electronics. The drive uses 100 ft (30 m) certified digital mini-cassettes with a capacity of 1.6M bits, or 200k 8-bit bytes at a density of 800 bits/in (315 bit/cm). A 2400-baud data rate is specified. Power supply requirement is 5 Vdc, with a max current of 600 mA in the rewind mode. Operational modes include read/write forward, search forward, and rewind. The unit can handle long term, low speed data logging, and other portable or remote applications because of low battery drain. Power consumption is 0.85 W in read/write mode. **Braemar Computer Devices, Inc,** 11950 Twelfth Ave, S, Burnsville, MN 55337.

Circle 272 on Inquiry Card

DATA TEST SET PRINTER



Designed to operate with the company's 3000D high speed, synchronous data transmission test set to provide a hardcopy record of V.24 (RS-232), V.35, Bell 301/303, RS-422, or MIL-188 data interface test results, the 2900D records errored seconds, total seconds, errored bits, and total bits tallied by the four event counters in the test set. An internal presettable 24-h real-time clock provides the time in hours and minutes for inclusion on the printout. Printouts may be programmed to occur whenever the interface signals SCT, SCR, DCD, RD, CTS, DSR, SQ, AGC, or RI exhibit transitions. Time of occurrence of sync lost and sync recovered may also be recorded. **International Data Sciences, Inc,** 100 Nashua St, Providence, RI 02904.
Circle 273 on Inquiry Card

RIBBON CONNECTOR SYSTEM

Superibbon connectors are mated by snapping the two halves together, requiring no separate hardware to assure a vibration-proof mating. The female connector is equipped with spring clips at each end that engage windows in the male. When male and female are pressed together, an audible click indicates that the pair is fully engaged and secure. A wire restraint device eliminates need for cable clamps for panel installations and other special applications. When restraints are attached to the connector, each wire is individually restrained at point of termination to provide pull resistance. The solderless termination system is the same as that used in the company's solderless ribbon connector. Connectors are available in 14, 24, 36, 50, and 64 contact sizes, each with a 90-deg hood. **TRW Cinch Connectors,** 1501 Morse Ave, Elk Grove Village, IL 60007.
Circle 274 on Inquiry Card

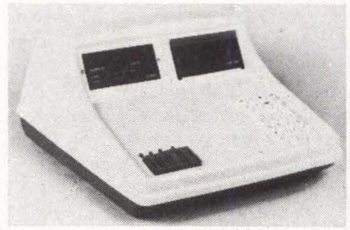
REMOTE DATA COMMUNICATIONS TEST INSTRUMENT

The microprocessor-based D-502 facilitates local and remote data communications diagnostics with interactive capabilities. It incorporates an output buffer and an output instruction to permit interactive operation and transfer of programs to and from a T-511 high speed tape unit or another D-502 or a communication line through any standard modem. The instrument provides a dynamic, real-time display of all information sent or received, yet is able to stop on a specific event or sequence, count occurrences, or measure time between them. A 2000-char buffer allows data surrounding a captured event to be scrolled backward and forward in large char on a 5" (12.7 cm) 375-char screen. Human language and hexadecimal display are switch-selectable. **Spectron Corp,** Church Rd & Roland Ave, Mt Laurel, NJ 08057.
Circle 275 on Inquiry Card

PRODUCTS

MULTIPURPOSE ROM SIMULATION SYSTEM

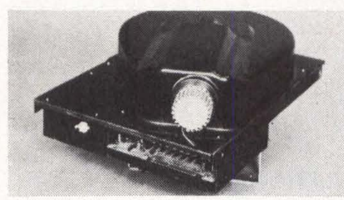
Combining ROM simulation, p/ROM programming, and storage, the self-contained ED6001 is designed for use with TTL-compatible p/ROMs and ROMS, and provides simulation for most 16- to 24-pin ROMs and p/ROMs. Data are entered by way of any 8-bit data bus, RS-232, or TTY system as well as from the hex keyboard. Both data and address, also in hex format, are displayed on a front panel LED readout. Options include expansion to include programming of all std fusible or ultraviolet p/ROMs, and a read/write cassette transport. Address incrementing can be done automatically after data entry or manually from the keyboard, with decrement being accomplished manually from the keyboard. Both address and data selection are displayed and randomly accessed in ½-byte increments to facilitate lookup. **Electro Designs, Inc,** 7364 Convoy Ct, San Diego, CA 92111.



Circle 276 on Inquiry Card

COMPACT DISC MEMORIES

A moving-head, fixed-disc unit and a multi-purpose combination of moving head and fixed head that permits high speed access have been added to the company's DK-62 and MFD 90 series. DK-10 and -20 have moving head capacity of 10.8M and 21.7M bytes, respectively, and avg access time of 50 ms. DK-10F and -20F each have, in addition to a moving head, fixed head capacity of 0.122M bytes that permits high speed access time of 10 ms. MFD 90-F and -F2 both have a moving head capacity of 1.95M bytes with average access time of 190 ms, as well as built-in fixed head capacity of 0.061M and 0.143M bytes, respectively, with average access time of 10.3 ms (50 Hz) or 8.8 ms (60 Hz). The combination of moving head and fixed head permits use of one disc memory for data filing and for a virtual system. **Hitachi, Ltd,** c/o Manning, Selvage & Lee, 666 Fifth Ave, New York, NY 10019.



Circle 277 on Inquiry Card

FLOPPY-DISC BASED SOFTWARE DEVELOPMENT SYSTEMS

FS990/4 and FS990/10 combine performance of the 990/4 and /10 computers, respectively, with floppy discs to provide a software design facility to support development, testing, and maintenance of applications programs. This includes capability for software and firmware development for the TMS 9900 microprocessor, 990/4 microcomputer, and 990/10 minicomputer. System software includes TX990 executive operating system and TXDS development utilities. Packaged in a single-bay desk enclosure, the FS 990/4 system includes 990/4 with 24k 16-bit words of memory with parity, dual floppy discs with 484k bytes of storage, and 913 video display terminal. **Texas Instruments Inc, Digital Systems Div,** M/S 784, PO Box 1444, Houston, TX 77001.

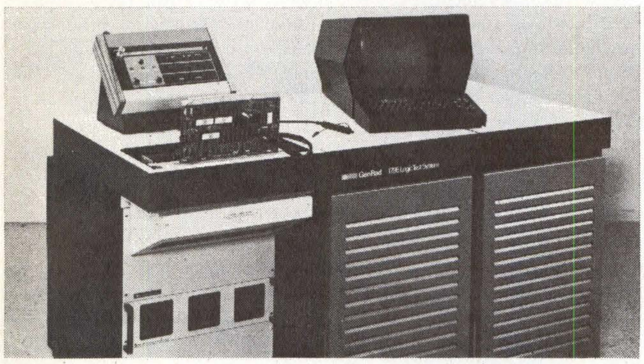
Circle 278 on Inquiry Card

MATRIX PRINTER HEAD

Featuring a proprietary solenoid design that enables high available duty cycle and operation speed, the printer head is available in configurations for 120, 160, or 200 char/s continuous print speeds. It can be adapted to most dot matrix data printers and is a direct replacement for the Victor unit used by many manufacturers. Lightweight and compact, the units have excellent heat dissipation characteristics. Duty cycle rating is up to 200 char/s, in a 9 x 7 dot matrix. A solenoid allows the seven vertical matrix striker wires to be mounted close together with only an 11-deg bend, overcoming reliability problems associated with flexing of the print wires in conventional units. Rated life of the printer head is 200 x 10^6 char min continuous operation. **Information Magnetics Corp,** 5743 Thornwood Dr, Goleta, CA 93017.

Circle 279 on Inquiry Card

LOGIC CIRCUIT TESTER



The 1795-HD incorporates large hard disc storage, and a unique driver/sensor board design which allows it to handle boards having up to 480 pins, providing programming flexibility, fault simulation, and high speed automatic diagnostics. Basic system contains 16k of core memory, single disc drive and controller, terminal, teletypewriter, 72 driver/sensors, and other hardware. Optional hardware includes additional driver/sensors (in groups of 24), power supplies, a second hard disc drive, and additional 16k of memory, high speed printer, high speed reader, high speed punch, diagnostic resolution module, and other items. Among the software options is the CAPS test system software, with or without automated program generation. **GenRad, Inc,** 300 Baker Ave, Concord, MA 01742.

Circle 280 on Inquiry Card

TURNKEY DATA ACQUISITION SYSTEM

System 620S consists of the company's 620 analog processor interfaced to the HP 9825A desktop calculator. The processor selects a channel for measurement, amplifies and filters the analog signal, and provides A-D conversion. The calculator has the computational capability and 24k semiconductor memory to provide system control and data processing. The amplifier-per-channel series 100 or series 400 differential multiplexer may be used as the processor, offering programmed input sensitivity of 5 mV to 10 V on up to 64 or 256 channels (expandable to 2048 channels). Both systems use solid-state multiplexer switches and provide common mode rejection of 120 dB. Input signals are converted to 12-, 14-, or 15-bit digital words. Channel sequence, input sensitivity, constants, and limit values may be entered from the keyboard. **Neff Instrument Corp,** 1088 E Hamilton Rd, Duarte, CA 91010.

Circle 281 on Inquiry Card

PRODUCTS

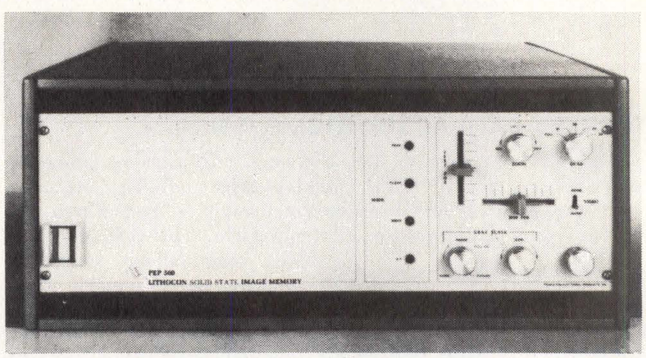
MAGNETIC TAPE TERMINAL

Available in either single or dual cassette configurations, the free-standing MTT (magnetic tape terminal) is equipped with two RS-232-C interfaces to accommodate a data set and a printer, CRT, or other auxiliary device. Complementing TermiNet^{TM} 300 and 1200 printers, the unit can be used with any device which has an RS-232-C interface. Features include character string search, high speed data transfer, and flexible editing. The ANSI-compatible digital cassette has read/write rates that are switch selectable at 10, 20, 30, 120, and 240 char/s. Transparency permits recording of non-ASCII 8-bit codes. Block lengths of 88, 144, or 166 char can be selected and data storage capacity ranges from 100k to 125k char/cassette depending on block length selection. **General Electric Co,** Data Communication Products Dept, Waynesboro, VA 22980.
Circle 282 on Inquiry Card

BLOCK FLOATING POINT ARRAY SIGNAL PROCESSOR

MSP-2, a single 15" (38.1 cm) sq plug-in board designed for Data General's line of Nova^{R} and Eclipse^{R} computers, will perform array calculations 10 to 50 times faster than minicomputers used for array calculation applications. It is capable of performing 1024-point real fast Fourier transforms on data resident in Nova memory in <7 ms, including I/O. Users may increase power by plugging in more than one board. Requiring only 5 V at 6.5 A, the board derives its dc power from the host computer. 2048 real words of memory reside on the processor board for storage of intermediate results. The unit handles all data internally as 24-bit words. All boards are p/ROM driven but can be reprogrammed to change the application. **Computer Design and Applications, Inc,** 375 Elliot, Newton, MA 02158.
Circle 283 on Inquiry Card

IMAGE MEMORY/SCAN CONVERTER



PEP-500 is a beam-addressed image memory designed for visual display of electronic signals from any source. Using advanced IC devices and the Lithocon TX-100 solid-state image memory, the device features high image gray scale resolution coupled with high image stability; operating specs are guaranteed regardless of extremes in temp, vibration, or magnetic ambience. The single-ended scan converter is operable in any of four modes: read, write, selective erase, and full screen clear. Beam address of the target can be driven either by internal raster generators or external X, Y signals. Image writing may be accomplished in either integration or equilibrium modes. **Princeton Electronic Products, Inc,** PO Box 101, North Brunswick, NJ 08902.
Circle 284 on Inquiry Card

LITERATURE

Teleprocessing Diagnostic System

Full color illustrated folder describing the microprocessor-based Pacer-103, which monitors data links or simulates hardware components, includes complete specs and test configurations. **Digitech Data Industries, Inc,** Ridgefield, Conn.
Circle 300 on Inquiry Card

TTL ICs

Data book contains specs and pin assignment drawings of all TTL ICs, sockets, and interconnection panels, and includes cross-reference tables and glossary of RIA and EIC approved terms and symbols. Price is $4.95/copy. **Texas Instruments, Inc,** Dallas, Tex.
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CRT Terminals

Dealing with models 3380-1102 and -1202 general-purpose CRT terminals, data sheets list features, applications, specs, and interfacing information, with illustrations and diagrams. **General Automation, Inc,** Anaheim, Calif.
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Data Communications

Basics of the line of modems, multiplexers, line drivers, enclosures, and accessories are featured in catalog containing specification charts. **Prentice Corp,** Palo Alto, Calif.
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Switching Power Supplies

Catalog details power supplies which feature 50 to 300 W of power and up to six output voltages for computer peripheral applications. **Boschert Associates,** Sunnyvale, Calif.
Circle 304 on Inquiry Card

Rotary Switch

Brochure illustrates the programmable Communicator series rotary switch, including features, specs, options, and dimensional drawings. **Oak Industries, Inc, Switch Div,** Crystal Lake, Ill.
Circle 305 on Inquiry Card

Data Converters

Consisting of photos, charts, and outline drawings, short-form catalog lists specs, features, and operational characteristics of ADCs, DACs, and data acquisition systems. **Micro Networks Corp,** Worcester, Mass.
Circle 306 on Inquiry Card

Precision Measurement and Control

Short-form guide provides technical specs and application data for such analog devices as ADCs, DACs, analog interface subsystems, thin-film networks, and power supplies. **Analog Devices,** Norwood, Mass.
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Programmable Digital Interface

Bulletin defines IEEE 488 or GPIB std interface system, lists parts, and explains programming procedures, operations, and applications. **Electronic Development Corp,** Boston, Mass.
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Motors and Speed/Torque Controls

Complete with specs, application data, and design summaries, reference catalog presents company's line of fractional horsepower motors, gearmotors, and adjustable speed/torque controls. **Bodine Electric Co,** Chicago, Ill.
Circle 309 on Inquiry Card

Digital Valves

Containing physical and engineering specs, outline drawings, and diagrams, handbook includes data on Q-series industrial microprocessor controller, digital control valves, and systems. **Digital Dynamics, Inc, A Dillingham Co,** Sunnyvale, Calif.
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Linear Motion Bearings

Color-coded catalog features installation data, engineering specs, and applications of company's line of Ball Bushings,® accessories, and components for friction-free linear motion. **Thomson Industries, Inc,** Manhasset, NY.
Circle 311 on Inquiry Card

Stock Relays

Handbook complete with specs, selection data, dimensional drawings, and wiring diagrams covers relays for wide range of general-purpose, industrial, and military applications. **Magnecraft Electric Co,** Chicago, Ill.
Circle 312 on Inquiry Card

Multiport Memory Systems

Colorful 12-page brochure with diagrams examines the memory system which enables up to 14 CPUs to share one memory bank and increase overall system throughput. **Interdata, Inc,** Oceanport, NJ.
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Cassette Recorders

Catalog includes descriptions, specs, and application information on company's line of data loggers, incremental and continuous R/W cassette systems, and readers, together with ASCII code chart, recording techniques, and tape formats. **Memodyne Corp,** Newton Upper Falls, Mass.
Circle 314 on Inquiry Card

CRT Display Station

The 2654A station is presented in user's manual which discusses operations, applications, keyboard functions, terminal maintenance, and trouble-shooting, and offers a programmer's reference table. **Hewlett-Packard Co,** Palo Alto, Calif.
Circle 315 on Inquiry Card

IC Packaging

Complete with photos and diagrams, catalog provides application information and specs on custom and std sockets, cards, and panels, and includes a section on solving custom packaging problems. **Scanbe, div of Zero Mfg Co,** El Monte, Calif.
Circle 316 on Inquiry Card

Miniature Switches

A variety of rocker and toggle-handled miniature switches are described in illustrated catalog which lists complete electrical and dimensional specs of line for industrial and commercial use. **Break-On Engineering Co,** Temple City, Calif.
Circle 317 on Inquiry Card

Solid-State Relays

Theory, performance, and applications of hybrid and all-solid-state devices are furnished in handbook, illustrated with performance graphs and parameter diagrams. Write on company letterhead to: **Gordos/Grigsby-Barton, Inc,** 1000 N Second St, Rogers, AR 72756.

Microcircuit Reliability

Microcircuit Reliability Bibliography, April 1976 portrays indexed abstracts and source information on gov't and industry reports, literature, and conference proceedings dealing with research, design, and application of microcircuit technology. Set costs $50 ($60 non-U.S.) (or vol IB and IV only at $40, $48 non-U.S.). **Reliability Analysis Center, RADC/RBRAC,** Griffiss AFB, NY 13441.

EDP Safety Standard

The third edition of the *Safety Standard for Electronic Data Processing Units and Systems* (UL 478) covers requirements for electrically operated, separate or assembled, machine units that accumulate, process, and store data. Send $3.50, or $9 for current edition plus subscription service to revisions, to: **Underwriters Laboratories, Inc,** Attn: Publications Stock Dept, 333 Pfingsten Rd, Northbrook, IL 60062.

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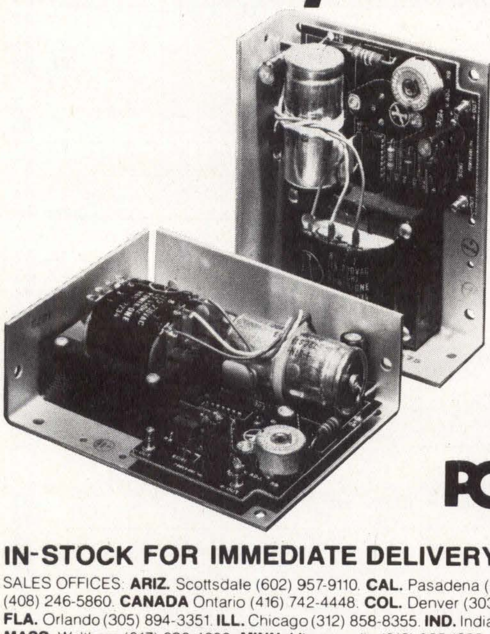

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