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THE MAGAZINE OF DIGITAL ELECTRONICS

FEBRUARY 1978

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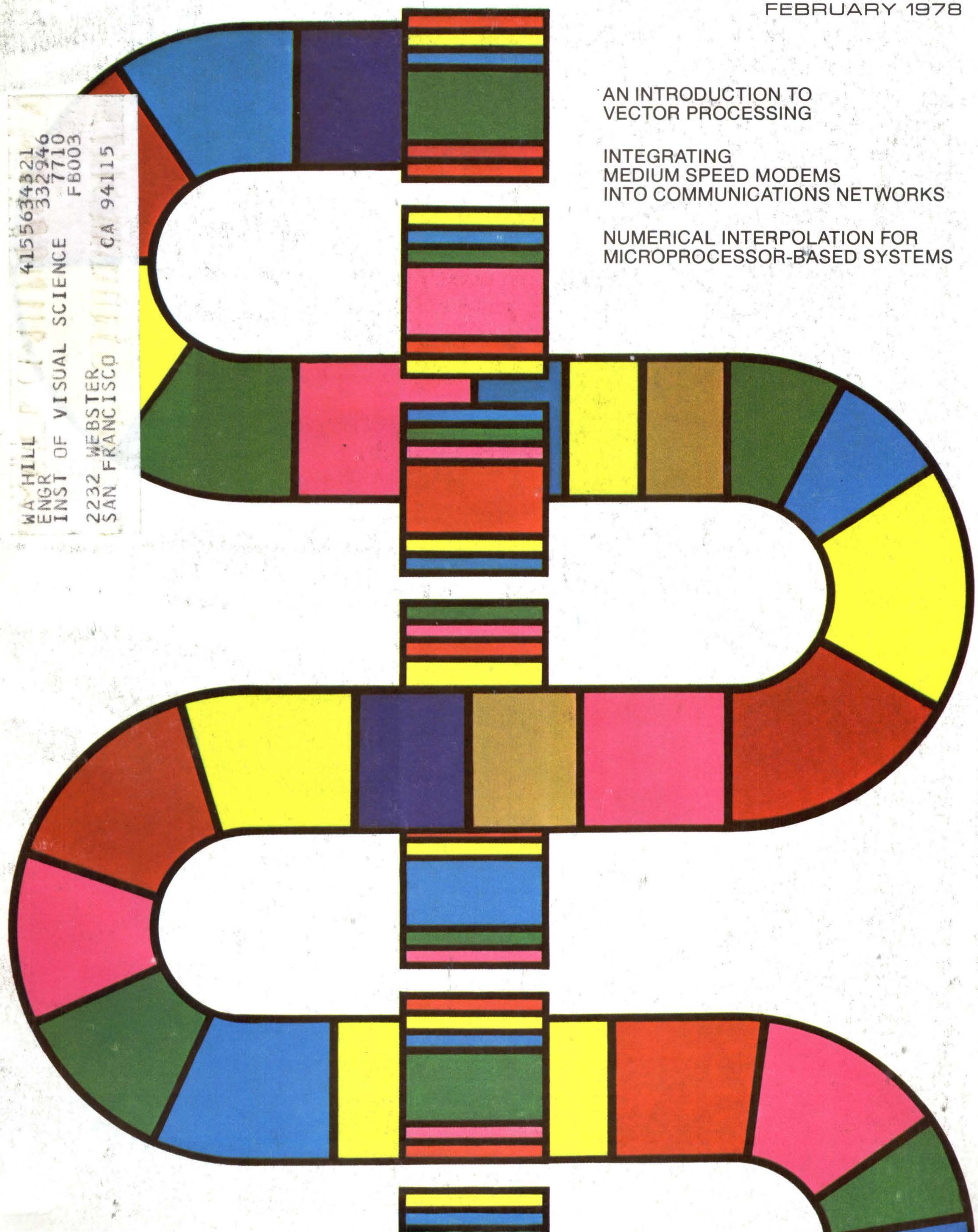

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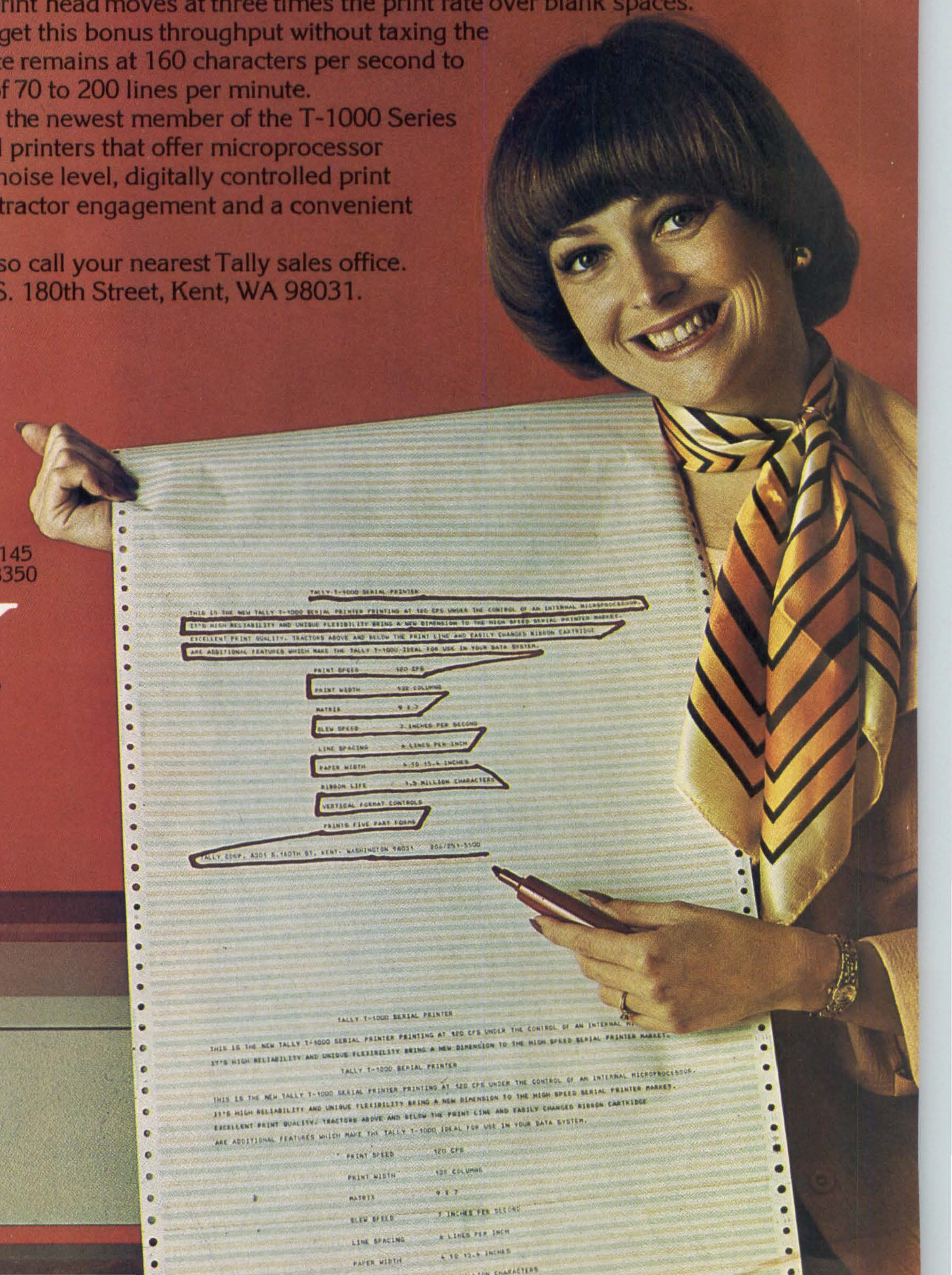

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COMPUTER DESIGN

FEBRUARY 1978

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FEATURES

CONFERENCE

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CALENDAR

CONFERENCES

FEB 28-MAR 2—COMPCON Spring '78, San Francisco, Calif. INFORMATION: COMPCON Spring '78, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

MAR 6-9—INTERFACE '78, Las Vegas, Nev. INFORMATION: Sheldon G. Adelson, Conf Dir, Datacomm Interface, Inc, 160 Speen St, Framingham, MA 01701

MAR 13-17—IEA/ELECTREX (Internat'l Electrical, Electronic, and Instrument Exhibition), Nat'l Exhibition Ctr, Birmingham, England. INFORMATION: Industrial and Trade Fair Ltd, Radcliffe House, Blenheim Ct, Solihull, West Midlands BN91 2BG, England

MAR 15-17—11th Annual Simulation Sym, Tampa, Fla. INFORMATION: Victor P. Boyd, U.S. Postal Service, 2009 Powhatan St, Falls Church, VA 22043. Tel: (301) 443-4137

MAR 20-22—IECI '78 Industrial Applications of Microprocessors, Sheraton Hotel, Philadelphia, Pa. INFORMATION: Dr S. J. Vahaviolos, Engineering Research Ctr, Western Electric, PO Box 900, Princeton, NJ 08540

MAR 22-24—Internat'l Topical Conf on the Physics of SiO_2 and Its Interfaces, IBM Thomas J. Watson Research Ctr, Yorktown Heights, NY. INFORMATION: Dr Sokrates T. Pantelides, Conf Chm, IBM Thomas J. Watson Research Ctr, PO Box 218, Yorktown Heights, NY 10598. Tel: (914) 945-1207 or 945-3000

APR 4 and 6—Invitational Computer Conf, Sheraton Heights, Hasbrouck Heights, NJ; and Valley Forge, Pa. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: (714) 644-6037

APR 12-14—Pattern Recognition and Artificial Intelligence, Nassau Inn, Princeton, NJ. INFORMATION: Prof Y. T. Chien, Dept of Computer Science, U of Conn, Storrs, CT 06268. Tel: (203) 486-4816

APR 17-20—Design Engineering Show, McCormick Pl, Chicago, Ill. INFORMATION: Clapp & Poliak, Inc, 245 Park Ave, New York, NY 10017. Tel: (212) 661-8410

APR 18-20—Mini/Micro Computer Conf and Expo, Philadelphia, Pa. INFORMATION: Robert D. Rankin, 5528 E LaPalma Ave, Suite 1, Anaheim, CA 92807

APR 18-20—The Society for Information Display Internat'l Sym, Hyatt Regency Hotel, San Francisco, Calif. INFORMATION: Lewis Winner, 152 W 42nd St, New York, NY 10036. Tel: (212) 279-3125

APR 24-26—28th Electronic Components Conf, Disneyland Hotel, Anaheim, Calif. INFORMATION: J. A. Bruorton, Mktg Administration Dept, Union Carbide Corp, PO Box 5928, Greenville, SC 29606. Tel: (803) 963-6348

APR 25-26—26th Annual National Relay Conf, Oklahoma State U, Stillwater, Okla. INFORMATION: School of Electrical Engineering, Engineering Ext 301 EN, Oklahoma State U, Stillwater, OK 74074

APR 28-30—PERCOMP '78, Long Beach Conv Ctr, Long Beach, Calif. INFORMATION: Royal Exposition Mgmt Corp, 1833 E 17th St, Suite 108, Santa Ana, CA 92701. Tel: (714) 973-0880

MAY 9-12—Internat'l Magnetics (INTERMAG) Conf, Palazzo Dei Congressi, Florence, Italy. INFORMATION: E. Della Torre, Dept of Electrical Engineering, McMaster U, Hamilton, Ontario L8S 4L7, Canada

MAY 10-12—3rd Internat'l Conf on Software Engineering, Hyatt Regency Hotel, Atlanta, Ga. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

MAY 22-26—7th Annual Sym on Incremental Motion Control Systems and Devices, Hyatt Regency O'Hare, Chicago, Ill. INFORMATION: Prof B. C. Kuo, Dept of Electrical Engineering, U of Illinois at Urbana-Champagne, Urbana, IL 61801. Tel: (217) 333-4341

MAY 23-25—ELECTRO '78, Boston-Sheraton, Hynes Auditorium, Boston, Mass. INFORMATION: W. C. Weber, Jr, IEEE ELECTRO, 31 Channing St, Newton, MA 02158. Tel: (617) 527-5151

MAY 29-JUNE 7—INTERNEPCON MOSCOW '78 (Internat'l Electronics Production Conf), Expo-Ctr, Pavilion 1, Krasnaja Presnaja Pk, Moscow. INFORMATION: Harry Lepinske, Industrial & Scientific Conf Mgmt, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

JUNE 12-15—MIMI '78 (4th Internat'l Sym and Exhibition of Mini and Microcomputers and their Applications), Zurich, Switzerland. INFORMATION: Secretariat MIMI '78 Interconvention, c/o Swissair Postfach, 8058 Zurich, Switzerland

JUNE 12-16—7th Triennial IFAC World Congress, Helsinki, Finland. INFORMATION: IFAC '78 Secretariat, POB 192, 00101 Helsinki 10, Finland

JUNE 20-22—Internat'l Microcomputers, Minicomputers, Microprocessors '78 Conf, Palais des Exposition, Geneva, Switzerland. INFORMATION: Joseph C. Maurer, Industrial & Scientific Conf Mgmt, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

JUNE 21-23—Internat'l Sym on Fault Tolerant Computing, Toulouse, France. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901

SEMINARS

MAR 7-9—Nat'l Zurich Seminar on Digital Communications, Zurich, Switzerland. INFORMATION: R. Aaron, Bell Laboratories, Holmdel, NJ 07763

MAR 20-22—Data Communications Services and Protocols; MAR 29-31—Understanding Performance Evaluation; and APR 3-5—Computer Networks, Americana Hotel, New York, NY; Arlington Hyatt House, Arlington, Va; and Stouffer's Nat'l Ctr Hotel, Arlington, Va. INFORMATION: Technology Transfer Inc, PO Box 49765, Los Angeles, CA 90049. Tel: (213) 476-1331

MAR 22-23—Implementing a Transparent Data/Voice/Image Communications Net—Packet Switching and Its Alternatives, New York, NY. INFORMATION: Kate Cogswell, The Yankee Group, Harvard Sq, PO Box 43, Cambridge, MA 02138. Tel: (617) 742-2500

APR 3-5—5th Annual Sym on Computer Architecture, Rickey's Hyatt House, Palo Alto, Calif. INFORMATION: E. J. McCluskey, Digital Systems Lab, Stanford U, Stanford, CA 94305. Tel: (415) 497-1451

APR 17-19, MAY 15-17, and JUNE 21-23—Minicomputers and Distributed Processing, Chicago, Ill; Toronto, Canada; and San Francisco, Calif. INFORMATION: Heidi E. Kaplan, Dept 14NR, New York Mgmt Ctr, 360 Lexington Ave, New York, NY 10017. Tel: (212) 953-7262

SHORT COURSES

MAR 6-7—Program Testing Tutorials, San Francisco, Calif. INFORMATION: Dr E. F. Miller, Software Research Associates, PO Box 2432, San Francisco, CA 94126. Tel: (415) 921-1155

JUNE 17-24—Advanced Microcomputer Interfacing and Programming Workshop, TSS Carnivale, Carribean. INFORMATION: Dr Norris Bell, Virginia Polytechnic Institute and State U, Continuing Education Ctr, Blacksburg, VA 24061. Tel: (703) 951-6208

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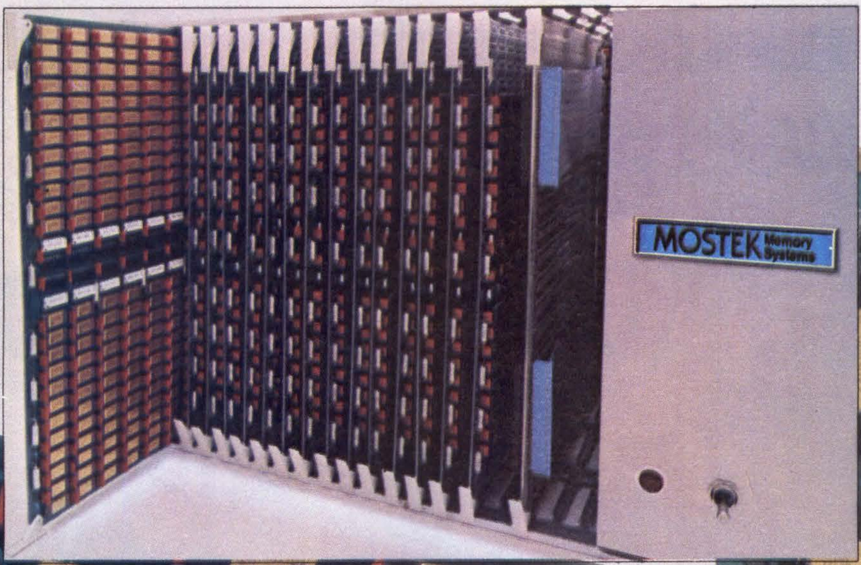

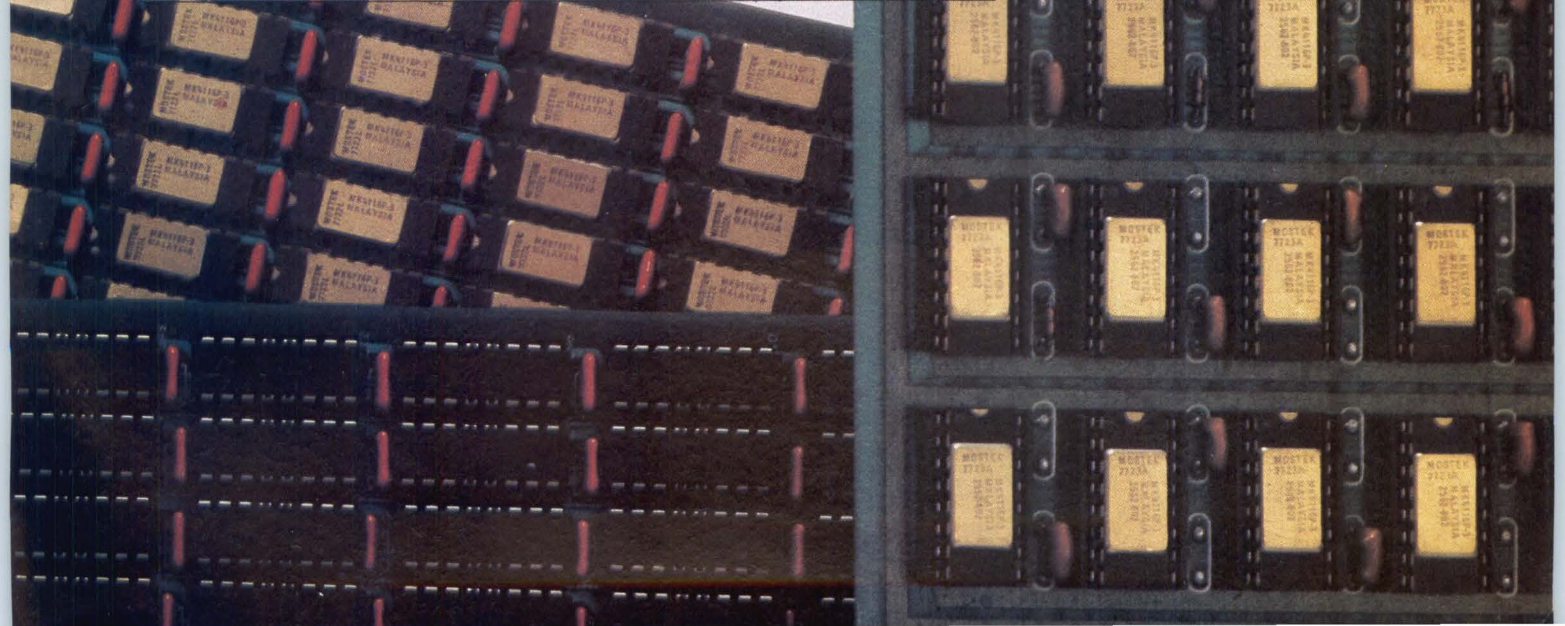

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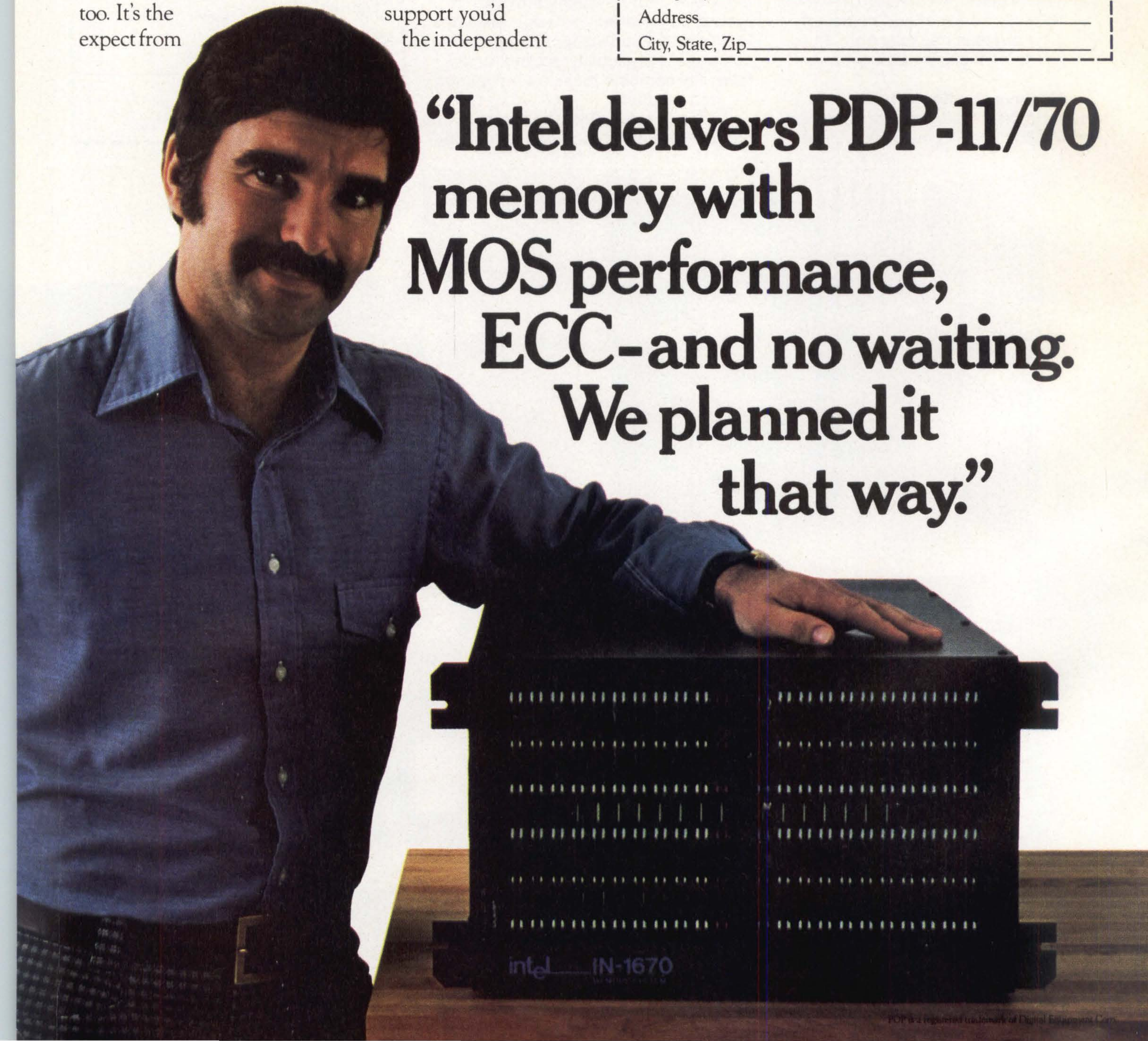

LETTERS TO THE EDITOR

To the Editor:

I enjoyed Ronald Zussman's article "Computer Queuing Analysis On a Handheld Calculator" (*Computer Design*, Nov 1977, pp 85-94). Since I own an HP-67 programmable calculator, I decided to try to program the analysis routines on it. I have enclosed a copy for interested readers.*

As you can see, my program takes only 182 program steps. I found that I did not need Mr Zussman's subroutine D', so I used LBL d (equivalent to LBL D') for the T, σ(T) calculations, and used LBL D for a routine that allows the user to enter the variables λ, u, and s when prompted, and have the calculator store them away. The prompts are numerical: 1 for λ, 2 for u, and 3 for s.

My key definitions are as follow: A: $\underline{P}(0)$, B: P(n), C: TW, D: data, E: $\overline{Q}$, a: U, $\underline{b}$: B, c: P(TW > t), d: T, σ(T), e: $\overline{N}$.

There are two other items of interest about my program. One is that in the calculation of TW, average waiting time, the probability of all servers busy, B, is calculated only if it previously has not been. Also, in the calculation of T, the average system response time, TW is calculated only if it previously has not been.

Basil Treppa
Siliconix, Inc
Santa Clara, Calif

*Interested readers may obtain a copy of Mr Treppa's program by requesting it in writing from The Editor, *Computer Design* Magazine.

Letters to the Editor should be addressed:

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11 Goldsmith St
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ASYNCHRONOUS TIMING ERROR CHARACTERISTICS

John E. Buckley

Telecommunications Management Corporation
Cornwells Heights, Pennsylvania

Data communications systems, seeking to reliably exchange information between two distant points, encounter ensuing complexities in the form of error correction codes, procedures, and protocols. In many cases these have created a probability of data errors greater than those that the techniques were intended to resolve. Two basic causes of data errors are data content permutations and loss of data flow synchronization.

Data content permutations are caused by external data transmission noise that damages or changes the state and characteristics of the transmitted information signal to such a point that the data receiver (demodulator) is unable to accurately recover the transmitted signal. The data transmitter and receiver maintain their relative synchronization and are therefore correctly transmitting and receiving the same information sample (ie, the first bit value of the character), yet the data content, and hence the information represented by that sample, is sufficiently distorted during transmission to result in a data error. In a simple passive data transmission system, the first bit of a character is transmitted as a 1 value, but due to spurious external energy sources, it is erroneously interpreted as a 0 by the data receiver. Error detection and correction coding schemes, such as the use of parity, are intended to compensate for these data content error conditions.

Loss of timing synchronization between the transmitter and receiver also results in the same data character error manifestations. Without data flow synchronization, the data transmitter generates the first bit value of a character while the receiver interprets the correctly recovered data bit value as the second, or some other, bit position of the data character. Correction of these transmission timing error situations is beyond the scope of any error coding scheme; they can be corrected only by adjustments within the data transmission equipment, predicated on an understanding of data transmission timing methods and their probable error characteristics.

The two data transmission timing methods are asynchronous and synchronous, each having advantages and disadvantages. Neither is inherently more dependable or effective than the other; hence, both methods have been used successfully. At the present level of technology, the asynchronous timing method is associated with data rates at or below 1800 bits/s, and synchronous with 2000 bits/s or above.

Asynchronous timing permits randomized generation of data characters by the transmitter. Continuous maintenance of a timing synchronization exchange between the data transmitter and receiver is not required when actual data characters are not being transmitted. When each data character is prepared for transmission, it is provided with sufficient timing synchronization information to permit the receiver to recognize the beginning of a data character and the correct value of each of that character's bits. With an asynchronous data communications system, the data transmitter and receiver must each be preset to the same data rate (bits/s) and the same number of bits comprising a data character. The inverse of the data rate defines the bit length, which becomes the basic element in the successful application of an asynchronously timed system.

When a data character is to be transmitted, the data transmitter generates a single bit length of a value opposite to the idle state value of the communications channel. The data receiver, upon recognizing the change in the channel's state, times one bit length interval, and then assumes that the next bit length interval represents the value of the first bit of the data character being transmitted. Each successive data bit is generated and recovered in the same manner. When the last data bit of the character is transmitted, the transmitter returns the communications channel to its idle state value for a minimum period of time before beginning the next data character. This minimum period is usually one or two bit length intervals. If no additional data characters are to be transmitted, the transmitter keeps the channel at this idle state value.

Since a data communications channel can only have two possible state values (1 or 0), the value of some data bits of a transmitted character will be the same as the idle state value of the communications channel. The first bit interval, transmitted before any of a character's data bits, is known as the start bit, and the minimum period of idle state value following each data character is known as the stop bit(s). With asynchronous timing, each data character is individually "synchronized" between the data transmitter and receiver. While there is admittedly a significant amount of noninformation overhead, the efficiency of asynchronous transmission is generally low. However, the advantage of being able to easily transmit randomly occurring data characters, such as from a keyboard, without the need and complexity of data storage more than offsets this efficiency limitation.

Both data transmitter and receiver may have compatible data rate clocks, thus generally limiting the occurrence of data transmission errors to single character errors, due to the same sensitivities experienced with data content error characteristics. If the channel permutation source results in mutilation of the start bit, the data receiver continues to detect an idle communications channel. When the first data bit of the character with a value that is the inverse of the channel's idle state is received, the data receiver assumes this bit interval to be the start bit, and begins to time and recover the "following" data bits. This results in at least one errored data character.

If the transmitter is transmitting from a data buffer or media, successive characters may also be errored; if the transmitter is being driven from a CRT buffer or magnetic tape, the interval between the transmitted characters would be only the minimum length of stop bit(s). When the data receiver does not detect an erroneous state bit until the last portion of the data character, the receiver could easily interpret the stop bits and following start bit as data bits, resulting in the second data character being recovered in error. Depending on the actual bit configurations that comprise a series of asynchronously transmitted data characters, it is possible to encounter a situation that would result in all data characters being lost. The present ASCII data code is constructed to prevent this. Examination of the bit patterns for each ASCII character shows the use of a data bit that has the same value as the start bit early in the transmitted bit sequence. In this situation, it is more desirable to utilize two stop bits. The increase in the minimum channel idle state value between the actual data characters greatly decreases the probability of an overflow effect due to loss of a single stop bit.

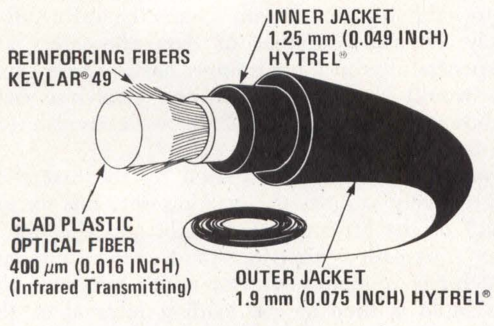
This data flow synchronization is about the limit of data transmission problems, if the data transmitter and receiver are adjusted to the same data rate. In reality, however, it is rare to find both the transmitter's and receiver's data clocks exactly the same. Slight tolerance differences do exist in the data clocks and should reasonably be expected. Normally minor discrepancies will be absorbed by the wide tolerances of the asynchronous timing method, but there are limitations.

Occurrence of the following symptoms should not be dismissed even if all or one of the data devices was measured and its data clock rate found to comply with the manufacturer's specifications. It is possible to have two devices that meet the same tolerance specification, but are incompatible with one another. A data transmitter could be at the higher tolerance limit of its data clock while the data receiver is at the slower tolerance limit of the same stated data clock value. These two devices are prone to demonstrate a data character error after approximately a certain number of data characters are exchanged successfully on a continuous basis. These same two devices would be able to exchange error-free data characters, however, if those characters were transmitted in a randomized manner.

The slower data receiver is initiated by the first start bit and progressively samples the ensuing data bits during the latter half of the bit interval. If only one stop bit is utilized, the progressive slippage tends to accumulate until the last bit of a data character is not sampled, and the actual sample is then at the leading interval of the stop bit. As a result, the following start bit is missed, resulting in an additional errored character. If two stop bits are used, the lost start bit does not occur and only a single data character is found to be in error at predictable intervals throughout a continuous data character transmission. Another situation requiring data clock adjustment is if these periodically errored data characters are being damaged in their last and/or next to last data bit values.

As a continuation, next month's column will discuss error characteristics that are experienced with synchronously timed data transmissions.

Infrared Transmitting Fiber-Optic Cable Uses Plastic Fiber For Improved Optical Performance



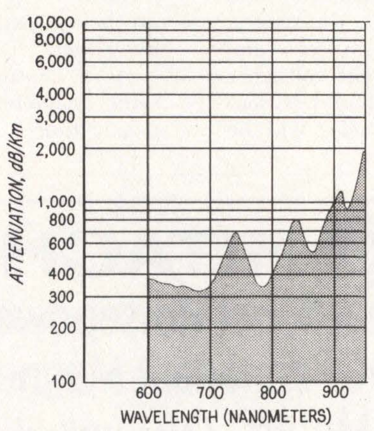
PFX-PIR infrared transmitting fiber-optic cable containing plastic optical fiber unifies properties of silica and plastic. Fiber is reinforced with Du Pont's Kevlar 49 aramid fiber in protective jacket of Hytrel polyester elastomer

Infrared transmitting capability of silica is combined with the ductility and durability of plastic in the PFX-PIR 140 all-plastic fiber-optic cable developed by E. I. du Pont de Nemours & Co, Plastic Products and Resins Dept, Wilmington, DE 19898. A chemical process has replaced the hydrogen in the plastic core with deuterium, a heavy isotope of hydrogen, resulting in improved optical performance; high speed, high power GaAlAs LEDs emit light in the 780 to 850-nm region which is absorbed by conventional plastics, but which is transmitted well by certain plastics containing deuterium. Calculations indicate that systems of 75 m or more can be achieved.

The cable has four times the run length capability of other plastic cables now available. Features include higher data rates and ruggedness, adapting the cable for such applications as computers, military, chemical plant or refinery control instrumentation, and mining communications.

Designed for use with higher speed, more powerful IR emitting diodes and solid-state lasers, the cable has a max attenuation of 320 dB/km at 690 nm and 340 dB at 780 nm. The large 368-μm core diameter permits easy alignment to emitters and low loss connections between cables.

The cable is reinforced with the company's Kevlar 49 aramid fiber in a protective jacket of Hytrel polyester elastomer. Clad fiber diameter is 400 μm; outer jacket diameter is 1.9 ±0.2 mm. Cable is available at $2.25 per meter (minimum quantity of 100 m).



Designed for higher speed, more powerful IR emitting diodes and solid-state lasers, plastic fiber-optic cable has max spectral attenuation of 320 dB/km at 690 nm, and 340 dB/km at 780 nm (measured with monochromator)

In addition, dimensional precision and run length improvements to the PFX-P140 and PFX-P240 single- and dual-channel all-plastic fiber-optic cables have been announced. Maximum attenuation rate is now 385 dB/km at 650 mm. Prices have also been lowered to $1.50 and $3 per meter, respectively.

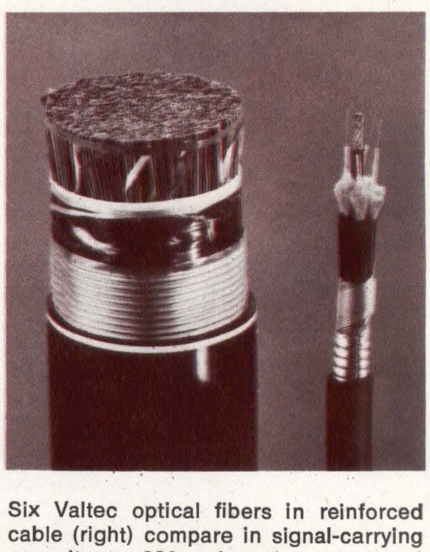
Circle 400 on Inquiry Card

System Connection Transmits Phone Calls By Light Impulses

Light waves instead of wire are being used to place thousands of telephone calls or several studio quality video tape transmissions simultaneously from the MGM Grand Hotel, Las Vegas, Nev. The 4.2-km fiber-optic system connecting the hotel to the Central Telephone Company's main switching office was developed and manufactured jointly by Valtec Corp, West Boylston, MA 01583 and Comm/Scope Co, Catawba, NC 28609 to provide increased operating efficiency, lower production costs, and greater capacity than conventional telephone equipment. The two companies have also announced an agreement-in-principle for Valtec, a public firm, to acquire the privately-owned Comm/Scope.

Employed in the system are Valtec fibers, laser diodes, and detectors with ruggedized cable developed and manufactured by Comm/Scope. Advantages of fiber-optics are elimination of cross talk and power line interference.

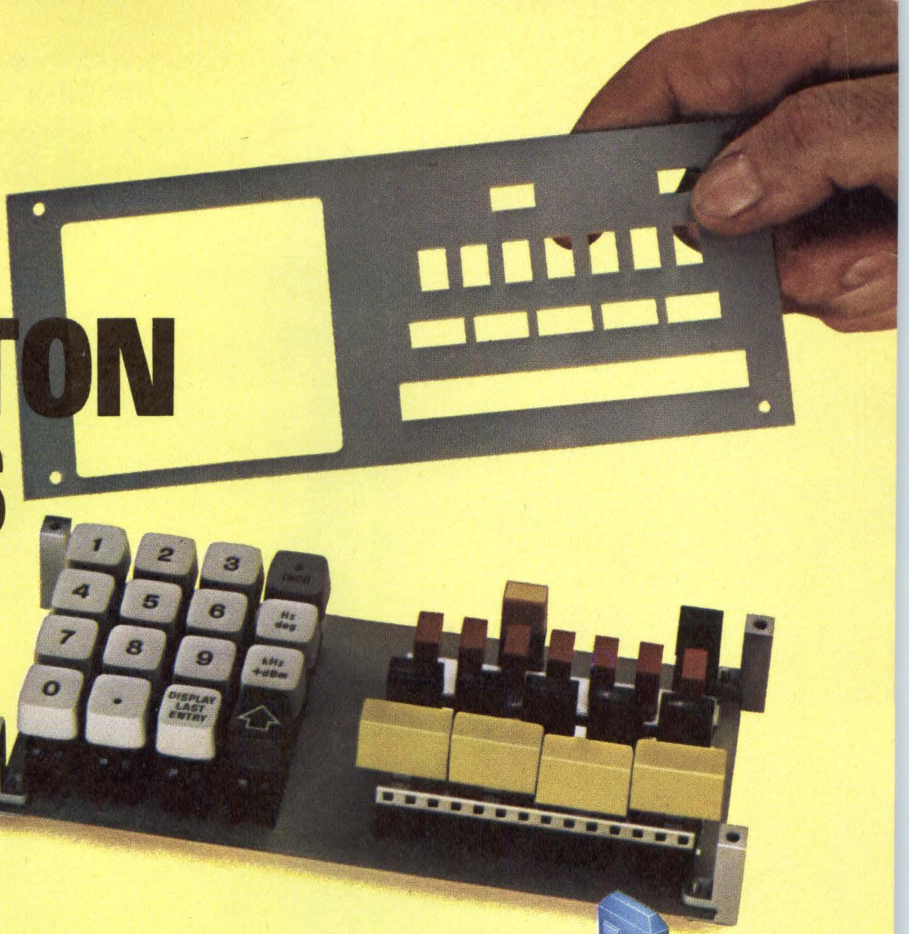
The system works with interfaces between the carrier (already standard equipment with wire systems) and fiber-optic cable. The carrier combines the many phones into the signal which is normally transmitted over copper cable. Then the bipolar signal is converted into a unipolar signal, and sent into the laser diode and driver that emits light into the fibers. Light is transmitted to the other



Six Valtec optical fibers in reinforced cable (right) compare in signal-carrying capacity to 900 pairs of conventional copper telephone wires (left)

New from Centralab...

MPS PUSHBUTTON SWITCHES

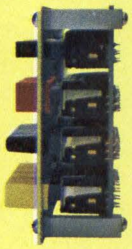


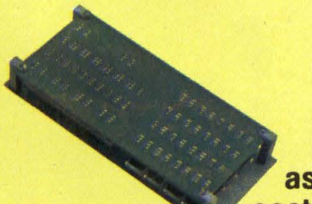
A new miniature modular building block system that offers microprocessor control designers more of what they need.

To meet the special digital and analog needs of today's μP-based controls, Centralab offers design engineers a whole new system of modular pushbutton switch building blocks. We call it MPS—integrated Modular Panel System. MPS saves PC board and panel area and simplifies front panel design, cuts assembly costs, reduces back-panel space requirements, and meets the digital-analog needs of μP-based controls. Check these space saving, cost-cutting features.

Simplify front panel interface.

All MPS switches regardless of function, are uniform in size, simplifying design and selection of front panel hardware. They have high volumetric efficiency, occupying .505" x .388" PC board area and require only .608" of space between PC board and front panel.





Cut assembly costs.

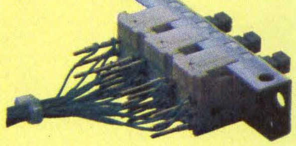
MPS switches may be mounted on the front panel, and are designed for automatic wave soldering installation and PC board cleaning. Insert molded terminals prevent flux and solder wicking and contact contamination. Integral PC board stand-offs provide for efficient board cleaning.

Meet analog and digital needs.

MPS switches are available with momentary, push-push and interlocking actions, with a long-life contact system that switches both digital and analog signals. To accommodate critical signal requirements, housings are high-insulation molded plastic with UL 94V-0 rating.

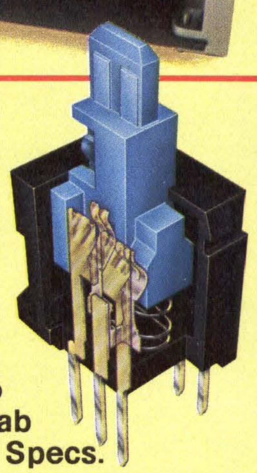
Available options.

Optional installations include ganged assemblies, front-panel mounting and wire-wrapping.



All MPS pushbutton switches are built to Centralab's highest quality standards (see specifications at right). They're priced as low as 41 cents in 1,000 quantity. For full technical details, samples and quotation, call (515) 955-3770, or write to the address below.

CENTRALAB
ELECTRONIC DIVISION
GLOBE-UNION INC.
P.O. Box 858
Fort Dodge, Iowa 50501

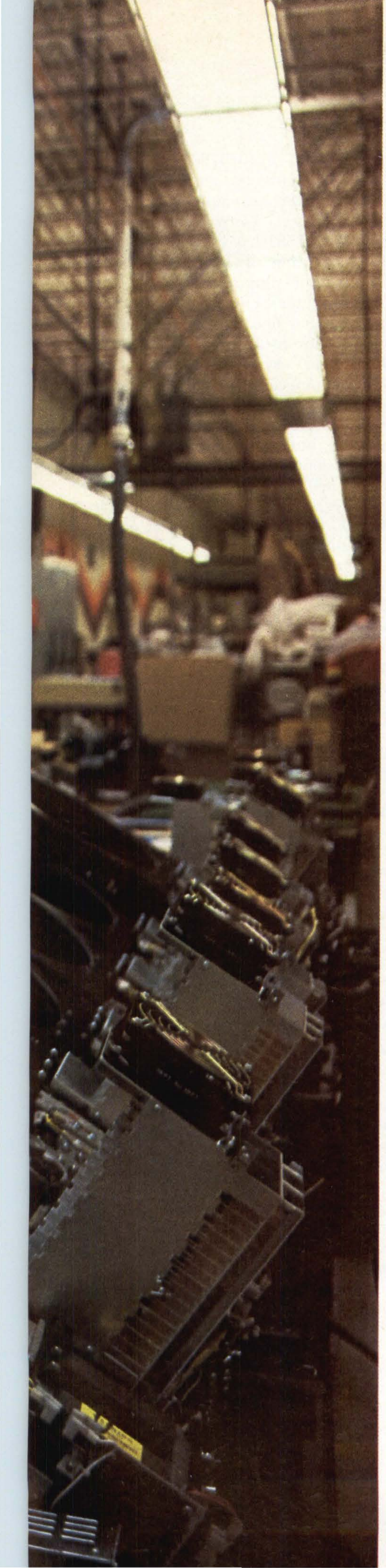


Built To Centralab Quality Specs.

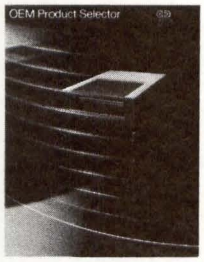
MPS Pushbutton Switches combine compact size, low cost and highest quality throughout.

- Silver or gold inlay wiping contacts for long-life and low-contact resistance.
- Less than 2 milliseconds contact bounce.
- SPST, SPDT, DPST, and DPDT switch contacts.
- Printed circuit, DIL socket or wire-wrap terminations available.
- 2.5 to 3.5 oz. actuation force (momentary).
- Choice of button interface—square or blade shaft (shown)—permits use of a variety of Centralab and industry standard buttons and keycaps.
- 10, 15, 20 or 25mm center-to-center spacing.

CIRCLE 11 ON INQUIRY CARD



"We can help you put quality behind your nameplate."



"Our new OEM Product Selector shows you how we can do that. It's a representative cross-section of our OEM product line, and it features some of our most popular products.

"As one of the world's largest suppliers of OEM equipment, Control Data knows what your customer is looking for.

"Quality, price, performance, reliability and support service.

"Control Data products are built with high-quality components, designed with advanced technology and engineered for performance.

"But prove for yourself that Control Data quality—built into every product we manufacture—delivers price/performance advantages that give your products the competitive edge. Test. Evaluate. Compare.

"Then check our OEM Financing, Maintenance and Spare Parts—all designed to make it even easier to put our experience behind your nameplate. And to help you establish a quality marketing position for your entire line.

"So send for your OEM Product Selector today. The sooner you do, the sooner we can work together on putting our quality behind your nameplate. Write us at HQN11I, P.O. Box O, Minneapolis, Minnesota 55440. Or call us at 612/853-7600."

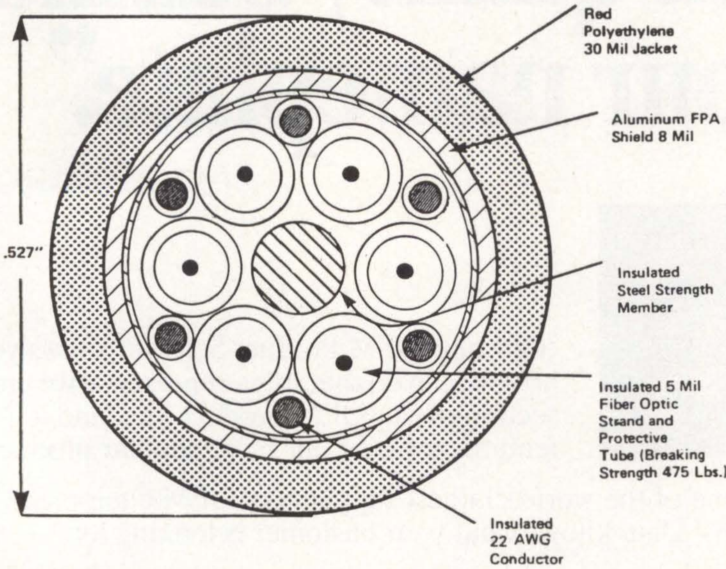
CONTROL DATA CORPORATION

More than a computer company

Dale C. Showers
Vice President O.E.M. Marketing

CIRCLE 12 ON INQUIRY CARD

CENTEL FIBER OPTIC CABLE CONFIGURATION



Optical cable cutaway shows center insulated with 0.09" (2.3-mm) steel strength member (also used to pull cable through duct) fitted with polyethylene jacket. Surrounding steel are six fibers, each covered with polypropylene tubing and then by flame-resistant strength member. Copper wires surround six subcables; wires are covered by mylar tape for thermal barrier. Aluminum sheeting serves as strength member and moisture/rodent barrier. Covering is water-resistant red polyethylene shield

end, and received by the avalanche photodiode and amplifier/comparator to extract the voice signal. Then the signal is reconverted with a unipolar converter and sent anywhere by conventional equipment. The optical system is fully compatible with existing telephone equipment.

At the center of each cable is a stranded steel strength member [tested for 1200-lb (544-kg) pull over a 370-ft (113-m) length without fiber breakage] fitted with a polyethylene jacket. Each of the six low loss graded index fibers surrounding this core is covered by a polypropylene tubing, then a Kevlar strength member. Color-coded 22-gauge copper wires surround these subcables to provide an electrical supply if repeaters are necessary, and for fieldphone communication during installation and splicing. The cable, available in lengths of 4000 to 5000 ft (1.2 to 1.5 km), is finished with a thin layer of mylar tape, aluminum sheeting, and a red polyethylene shield for moisture resistance and easy identification.

Circle 401 on Inquiry Card

Data Communications Capabilities Enhance Microcomputer Family

Hardware interfaces, software support utilities, and communications packages comprise a group of enhancements enabling the microNOVA family of 16-bit NOVA[R] compatible microcomputers to be configured for a broad range of data communications applications. Users gain the ability to implement asynchronous and synchronous protocols and to run RJE80 (IBM 2780/3780) and IBM HASP II emulation packages on a microcomputer system.

Data General Corp, Rte 9, Westboro, MA 01581 has introduced hardware consisting of board-level components that plug directly into the microcomputer's chassis. Model 4226 synchronous line controller interfaces to up to four medium speed (9600-baud) synchronous/bisynchronous communications lines. It provides full- and half-duplex EIA RS-232-C/CCITT V.24 interface and full character buffering on reception and transmission. Coupled with the optional model 4228 hardware CRC generator, the controller selects either CRC16 or CCITT16 standard check polynomials.

Controlling up to four asynchronous communications lines, model 4227 asynchronous line multiplexer configures each line for RS-232-C or 20-mA current loop operation. Bits/character, number of stop bits, line speed, and parity are individually programmed.

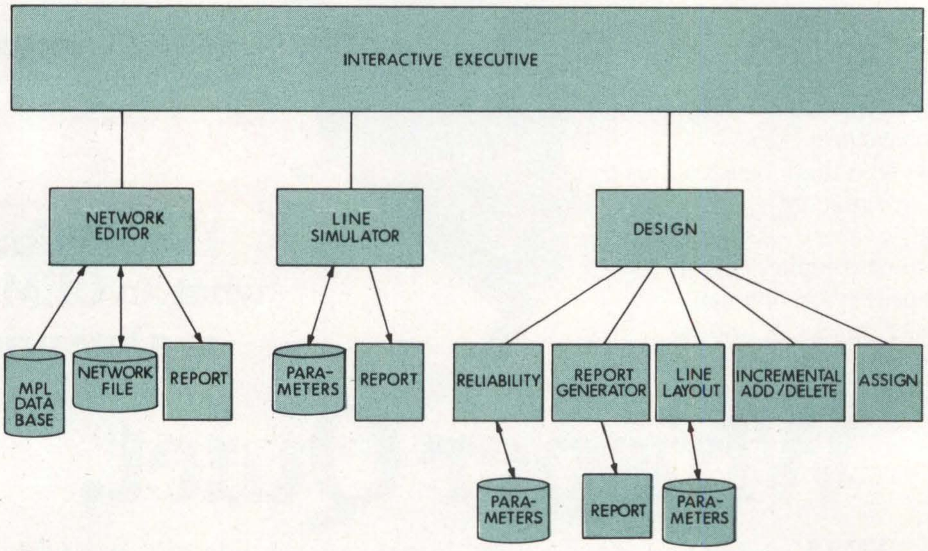
Software support is provided by the communications access manager operating under diskette-based DOS and RTOS. It supplies a utility for implementing application programs requiring asynchronous teletypewriter and synchronous/bisynchronous protocols. A COMGEN utility is also included.

Circle 402 on Inquiry Card

Self-Teaching Design and Analysis Tools Offered on Timeshared Basis

A standalone, interactive system of computerized tools for designing data networks, analyzing performance, and maintaining centralized telecommunications networks is offered to communications managers on a timeshared basis. Heart of the Network Design Service is a family of programs called MIND (modular interactive network designer) which are structured for operation by users with little computer or timesharing experience.

Network Analysis Corp, 130 Steamboat Rd, Great Neck, NY 11024 started with basic software tools, adding prompts, instructions, and diagnostics to provide network managers with tools that enable them to work faster and more precisely,



High level structure diagrams interrelations of functional blocks of MIND network design service. All communication with user is via interactive executive program that maintains dialogue with user and controls execution of background applications. Two groups of applications are network editor and design modules, and multipoint line simulator. Respectively, these allow users to generate and maintain centralized networks, and study response time/throughput performance of centralized networks by modeling traffic loading and details of line protocol

and to investigate a wider array of alternatives. The service offers full-time dial-up access to the programs through facilities of a timeshared computer service organization. It can be reached via Telenet or through phone company dial or leased lines. Any ASCII terminal (hardcopy or CRT) can be used. The company also provides user training, manuals, and several hours each month of online design consultation.

Three basic modules comprise the MIND package. Supervising dialogue between the user and modules is an executive program with "handholding" features that provide information at each step to guide selection of proper commands and input data about the network. Commands are hierarchically organized into bases, ie, logical groupings of commands with related functions.

The network editor module is a data base system into which the user enters data describing the network. Providing information for the optimization and simulation modules, this module also maintains a dynamic record of an existing network's nodes, links, and traffic loads.

The topological optimization module automatically designs a centralized multipoint line layout using node locations, operating characteristics, and desired performance constraints; it satisfies user requirements at lowest possible cost, based on AT&T's MPL interstate private line tariff. It also contains a network reliability submodule.

Throughput/response time analysis of any network configuration to be modeled is obtained from the multipoint line simulation system module. Effects on network performance created by such varying parameters as terminals/line, traffic load, and device characteristics are reported.

Circle 403 on Inquiry Card

Three Processors Connect Computers Handling Data Center Communications

Three programmable 1380 communications processors, replacing previous hardwired terminal control units, control communications for an IBM System/370 model 168, System/370 model 158, and two Amdahl 470/V6 computers at the Western Electric Co data center location in Warrenville, IL 60555. Installed by Memorex Corp, San Tomas at Central Exwy, Santa Clara, CA 95052, the computers support an Information Management System data base, a timeshare option, and management information and text system for report generation and sophisticated word processing.

The units function as frontend processors for as many as four mainframes. Each features a CRT control console; communications programs reside on a flexible disc storage system. The processors are connected to provide backup in case a CPU has to be taken out of service.

Circle 404 on Inquiry Card

Program Provides Emulation for Data Communications System

Multiple terminal emulator (MTE) is a software program that can be executed on the company's 1100, 2200, 5500, or 6600 disc or diskette-based processors with a minimum of 16k bytes of memory, enabling a more uniform operating procedure. The systems from Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284 are then able to emulate most IBM remote job entry terminals, including HASP, RES, and JES workstations.

Three methods of implementation are a disc-operating system that initiates the package in a point-to-point system; a partition supervisor that allows the emulator to run under either partition, while two programs are executed at once; and a Chain facility, which is a job control library function used to execute the software package sequentially with other programs. Choice of emulator, as well as assignment of peripherals according to job requirements, is made by keyboard instructions.

Software operates at up to 4800 baud on 1130 and 2200 processors using the 9404, 9405, or 9481 communications interface and modem. With the 9481 interface on the 1150, 1170, 5500, or 6600 processors, speeds of up to 9600 baud are possible; the 9404 or 9405 interface on these same processors allows up to 4800 baud.

Circle 405 on Inquiry Card

Computer-Controlled Switch Reduces Telephone Expenses

Monthly telephone expenses of Browning-Ferris Industries, Inc's Corporate Offices, Houston, TX 77001 have dropped by an average of 24 to 28% after having installed a computer-controlled PBX. The computerized branch exchange (CBX) from Rolm Corp, 4900 Old Ironsides Dr, Santa Clara, CA 95050, which went online last year, is equipped with toll restriction, route optimization, and call detail recording features. The company with 26 central office trunks was able to reduce them to 20 trunks without any detectable system degradation.

The company is now investigating such options as call queuing, which would also provide toll restriction to automatically prevent abuse or misuse, route optimization to select most economical lines for outgoing calls, call queuing to smooth demand, and call detail recording to provide inhouse visibility on system usage.

Terminal Translates Between Caller and Paging Terminals

Model 810 voice-input terminal is an end-to-end signaling decoder that allows page-number entry by a caller speaking digits directly to the terminal over telephone lines with no operator interface. Dialog Systems, Inc, 32 Locust St, Belmont, MA 02178 has provided the system with automatic end-to-end signaling; it handles up to eight telephone lines simultaneously, for tone and voice as well as tone-only paging. Standard interfaces are RS-232 and 20-mA serial current loop. Touch-Tone[R] input and parallel interfaces are optional.

Circle 406 on Inquiry Card

Standard Features and Combined Option Package Are Added to Simulator

The Pacer-103 programmable data line monitor/interactive simulator for data communications testing has been supplemented by a combined options package (E009) that includes capture memory (one increment of 2k characters and 2k status), remote program load/storage, expanded hexadecimal/binary package, one additional language, and two additional 4-digit (C and D) counters. Price is $750. Digitech Data Industries, Inc, 66 Grove St, Ridgefield, CT 06877 has added three functions as standard features: LRC-8/no parity check character selection, reverse hexadecimal display for BCD and Selectric codes, and dump capability for data output without language translation or parity correction. □

Circle 407 on Inquiry Card

There isn't a process control system in the industry that our Intecolor 8001G can't improve, because color communicates faster.

Bailey Meter, Taylor Instruments, Dow Chemical, International Paper, ACCO Bristol, PPG Industries come from a long list of industry leaders who have integrated our Intecolor 8001 color data terminal into their systems—sophisticated systems that demand critical control. Now we can bring you the Intecolor 8001G, the same precision terminal with a special color graphics package as a standard feature, at considerable savings over the separate option cost. Look at some of the advanced Intecolor 8001G features:

• Expanded hardware and software graphics • 48 lines by 80 characters with two different character heights • Eight foreground colors, plus eight background colors for additional definition • Character and line insert and delete • Page roll-up • 64 Standard Instrument Society of America characters • Plotting capability on a 160 by 192 matrix • Expanded keyboard with cursor and color controls • 19" display

A 25" unit with the same standard features is available at slightly extra cost.

We guarantee delivery of your Intecolor 8001G evaluation unit for $1,925* (cash-with-order) within 30 days or your money back. The same $1,925 price goes for orders of 100 units or more. Get the jump on your competition without outspending your competition. Get the Intecolor 8001G.

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CIRCLE 15 ON INQUIRY CARD

Meet HP's new Logic Analyzer that captures state, timing and glitch information simultaneously.

Now you can approach logic debugging from a timing or state point of view.

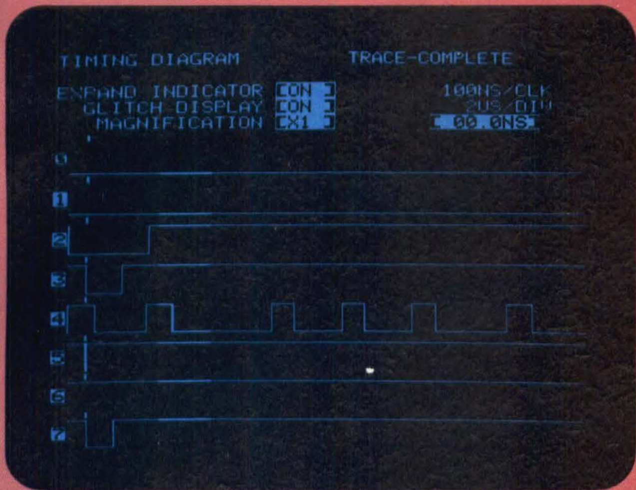
HP's new 1615A Logic Analyzer now gives you unmatched capability for system logic analysis. Use it as a 24-bit state analyzer for real-time monitoring of program execution. Use it as an 8-bit timing analyzer for locating problems on control lines or other asynchronous system elements. Or, with its cross triggering and arming capability between timing and state modes, use it as a combination of state and timing analyzers to debug interaction problems between synchronous and asynchronous system elements.

This powerful new logic analyzer lets you perform many tasks such as evaluating system performance at the time of a glitch; verifying I/O data stability prior to reading a port; monitoring handshake sequences at specific points in a program where a problem exists; and more. Using simple keyboard entries to pinpoint areas of interest in system activity you save both development and debugging time of synchronous and asynchronous digital systems.

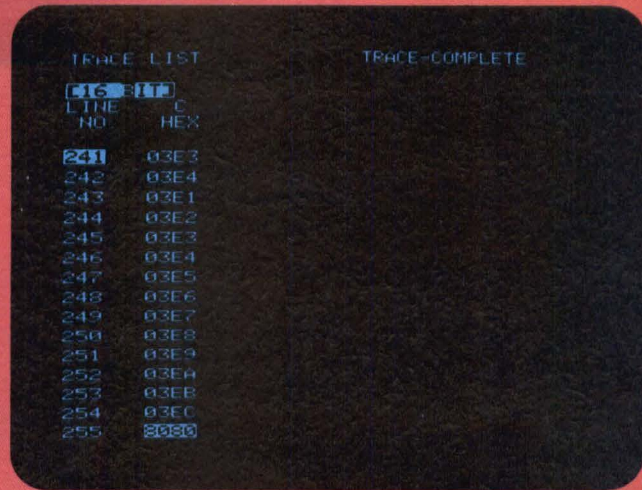
If you're designing digital systems, this combination state and timing analyzer, priced at $6800*, will help you reduce development costs and troubleshooting time. Your local HP field engineer has all the details. Give him a call today.

* Domestic U.S.A. prices only.

Timing Analysis—The hardware approach

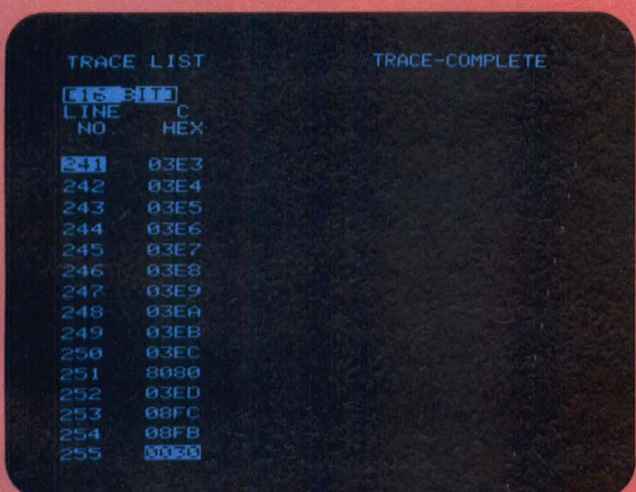


Trigger on glitches. A glitch on an input to a one shot (channel 5) is causing a false interrupt (channel 7). This glitch (which is intensified to distinguish it from data) can be used to trigger state as well as time displays.

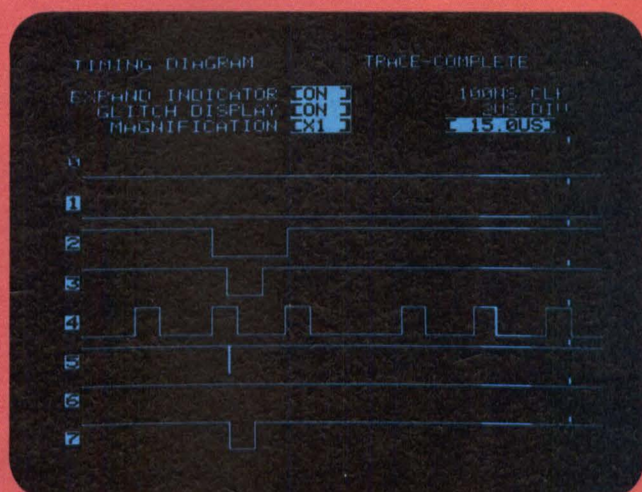


Observing state display shows address flow at the moment the glitch occurs and reveals that the I/O port address 8080 always accurs at the same time. This would lead you to observe I/O related signals for transitions occurring simultaneously with the glitch.

State Analysis—The "Software" approach



Trigger on state. The interrupt vector (0030) can be used as the trigger point to observe address flow prior to the false interrupt. Evaluation shows that the I/O port address 8080 always appears four machine cycles prior to the interrupt vector.



Observing timing display of signals on I/O and one-shot shows that the glitch on the input to the one shot (channel 5) occurs four machine cycles before the trigger point and is coincident with the transition on I/O read (line 3) indicating possible capacitive coupling.

088/2

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CIRCLE 16 ON INQUIRY CARD

CENTRAL INTELLIGENCE:

The data formatter that came in out of the cold.

Tape drive intelligence has crossed the iron walls. And taken up residence *inside* a broad series of transports—through a special Microformatter™ that Pertec installs internally.

A real technology breakthrough for sure. But it's the hot savings potential that intrigues OEMs most.

Eliminates the need for any external formatter to control the reading and writing of data. Makes interface chores much easier.

Now add in the convenience and cost-efficiencies you'll realize with just one system to handle (and ship), instead of two separate devices.

Saves integration time. With the Microformatter built-in, a single interface can be used for 800 cpi NRZI, 1600 cpi PE, or dual formats.

Saves redesign. Formatted Tape Transports use the same Pertec industry-standard formatter interface. And the same Microformatter, to maintain parts commonality.

Saves daisy-chain hassles. Every master Formatted Transport can daisy-chain up to 3 more tape drives—either Pertec standards or our new Formatted models.

Saves rack costs. You free up former external-mount slots. And the single-board LSI Microformatter is so compact it fits into each drive without restructuring standard rack mounts.

Internal Formatting. Deep down inside, you know it's right! And it's available in a flexible configuration range.

Formatted tension-arm: *FT7000*—compact 7″ reel, NRZI or PE, 12.5 to 25 ips. *FT8000*—10½″ reel; NRZI, PE, or dual NRZI/PE to 45 ips.

Formatted vacuum-column: *FT9000*—10½″ reel, 37.5 to 75 ips NRZI, PE or dual. And *FT1000*—10½″ reel, our vacuum column 125 ips high speed auto-thread, auto-load series, dual NRZI/PE.

Fully proven product. All are microformatted extensions of field-proven drives, produced by the world's largest independent manufacturer of peripheral equipment.

And backed by international sales/service facilities, with a long-term commitment to responsiveness. Making emergency assistance available on a 24-hour, 7-day basis, accessed through our toll-free 800 line.

At every level—product, sales, maintenance—Pertec intelligence has always recognized that cost-effectiveness is the central issue with OEMs.

☐ Please send full details on the Pertec Formatted Tape Transport Series.
☐ Send pricing information as indicated on the RFQ below (no obligation or cost).

Request for Quote

Formatted Series #	Reel Size	Tape Velocity (ips)	Recording Mode	Quantity Required	Date Wanted	Send Specs
FT7000	7″	12.5-25	PE or NRZI			
FT8000	10½″	12.5-45	PE, NRZI, Dual			
FT9000 Vacuum Column	10½″	37.5-75	PE, NRZI, Dual			
FT1000 Vacuum Column	10½″	75-125	Dual NRZI/PE			

Name____________________

Title__________ Phone__________ Ext______

Please attach coupon/RFQ to company letterhead and return to Pertec, 9600 Irondale Avenue, Chatsworth, CA 91311.

For immediate requirements, call your nearest Pertec regional sales office: Los Angeles (213) 996-1333. Ann Arbor, Michigan (313) 668-7980. Hudson, New Hampshire (603) 883-2100. England (Reading) 582115.

PCC PERTEC

a division of Pertec Computer Corporation

CIRCLE 17 ON INQUIRY CARD

Modular Business Computer System Can Be Modified, Increased, or Reduced Without Interrupting Operation

What the manufacturer says is a totally integrated computing facility, one which "will dramatically alter the way the business world thinks about and uses computers," has been announced by Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284. In this facility a number of functionally dispersed small computers are linked by a high speed bus and a library of systems software. Data processing units, data base facilities, peripherals, and all other system components are completely accessible to all users.

There are three basic components in any ARC™ (attached resource computer) system: applications processors, file processors that manage the data base, and interprocessor bus. Configuration can be matched to the specific needs of a user by choice of modules incorporated in the system. Then, as tasks change or requirements increase, the system can be reconfigured—without interrupting system operations—by simply adding modules.

There is no central processor; the system will continue to function even if an individual processor is removed. When any system unit fails or is taken offline, operations of all other units continue. Modules currently available are 6000 and 3800 series attached processors, a resource interface module (RIM), active and passive hubs, and a direct channel interface option (DCIO) that allows an IBM System/360 or /370 to act as an applications processor.

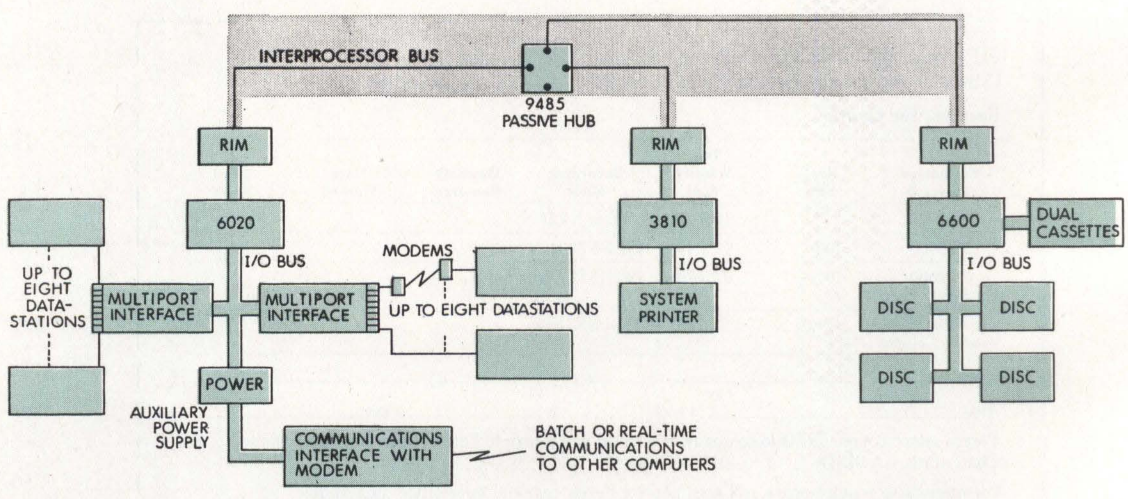
The 6000 series processors are available with 60k- or 120k-word user memory and feature 600-ns memory cycle time, enhanced instruction set, multiple-byte I/O transfers, segmented and protected memory, state saving and restoring, and privileged instructions. A 4k-word read-only memory allows system initialization from a file processor. This series supports virtually all of the company's software and peripherals designed to execute on their predecessor, the 6600 advanced business processor.

A 6020 (120k) processor can support up to 24 video display user workstations; a 6010 (60k) can support up to 16. Each workstation can concurrently access the system's common data base, enter data, and direct execution of the same or different programs. Processors also support batch or real-time communications to other computers or systems.

Video display is 80 columns by 12 rows (960 character positions) in a 7 x 3.5" (17.8 x 8.9-cm) viewing area. Characters are formed in a 5 x 7 dot matrix. Programmable display memory allows for generation of 128 characters under program control.

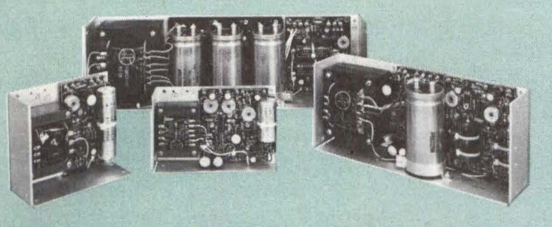
Series 3800 processors are also available with 60k (3810) and 120k (3820) of user memory. They enter, process, store, and communicate data using the common system data base. Memory access time is 300 ns.

Batch or real-time communications are supported using synchronous or asynchronous communications interfaces and modems. Communications software is also supported, including



Basic configuration of Datapoint's attached resource computer (ARC) system. Key feature is modular construction. System can grow in power and tasks performed as requirements increase. Processors can be added and more disc drives can be attached when needed. If any system component fails or is otherwise taken offline, system continues to function

"Talk about
OPEN FRAMES



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SERVICE • 83 Standard Stocked Models — the industry's largest selection • Local Stocking Centers Nationwide — stocked for immediate delivery
ECONOMY • The industry's most cost-effective D.C. power supplies • Liberal discounts for quantity buyers

SINGLE OUTPUT — STANDARD
±.02% REGULATION • REMOTE SENSING

VOLTS	AMPS	MODEL	PRICE 1-9	VOLTS	AMPS	MODEL	PRICE 1-9	VOLTS	AMPS	MODEL	PRICE 1-9	VOLTS	AMPS	MODEL	PRICE 1-9
5	3.0	B5-3	$24.95	12	1.7	B15-1.5	$24.95	18	1.3	B24-1.2	$24.95	24	1.2	B24-1.2	$24.95
	6.0	C5-6	44.95		3.4	C15-3	44.95		2.6	C24-2.4	44.95		2.4	C24-2.4	44.95
	12.0	D5-12	74.95		6.8	D15-6	74.95		5.2	D24-4.8	74.95		4.8	D24-4.8	74.95
	18.0	E5-18	104.95		10.2	E15-9	104.95		7.8	E24-7.2	104.95		7.2	E24-7.2	104.95
6	3.0	B5-3	$24.95	15	1.5	B15-1.5	$24.95	20	1.3	B24-1.2	$24.95	—	—	—	—
	6.0	C5-6	44.95		3.0	C15-3	44.95		2.6	C24-2.4	44.95				
	12.0	D5-12	74.95		6.0	D15-6	74.95		5.2	D24-4.8	74.95				
	18.0	E5-18	104.95		9.0	E15-9	104.95		7.8	E24-7.2	104.95				

SINGLE OUTPUT — HI-VOL
115/230 VAC INPUT • OVP ON 5V MODELS

VOLTS	AMPS	MODEL	PRICE 1-9	VOLTS	AMPS	MODEL	PRICE 1-9	VOLTS	AMPS	MODEL	PRICE 1-9	VOLTS	AMPS	MODEL	PRICE 1-9
2	3.0	HB2-3	$29.95	12	0.5	HA15-0.5	$22.95	24	1.2	HB24-1.2	$24.95	48	0.5	HB48-0.5	$29.95
	6.0	HC2-6	49.95		1.7	HB12-1.7	24.95		2.4	HC24-2.4	44.95		1.0	HC48-1	49.95
	12.0	HD2-12	79.95		3.4	HC12-3.4	44.95		3.6	HN24-3.6	64.95		3.0	HD48-3	79.95
	18.0	HE2-18	109.95		5.1	HN12-5.1	64.95		4.8	HD24-4.8	74.95		4.0	HE48-4	109.95
5	1.2	HA5-1.2/OVP*	$22.95		6.8	HD12-6.8	74.95		7.2	HE24-7.2	104.95				
	3.0	HB5-3/OVP*	24.95		10.2	HE12-10.2	104.95								
	6.0	HC5-6/OVP*	49.95	15	0.5	HA15-0.5	$22.95	28	1.0	HB24-1.2	$24.95	180, 200	0.12	HB200-0.12	$34.95
	9.0	HN5-9/OVP*	69.95		1.5	HB15-1.5	24.95		2.0	HC28-2	44.95				
	12.0	HD5-12/OVP*	79.95		3.0	HC15-3	44.95		3.0	HN28-3.0	64.95				
	18.0	HE5-18/OVP*	114.95		4.5	HN15-4.5	64.95		4.0	HD28-4	74.95	250	0.1	HB250-0.1	$34.95
					6.0	HD15-6	74.95		6.0	HE28-6	104.95				
					9.0	HE15-9	104.95								

SINGLE OUTPUT — HIGH POWER
115/230 VAC INPUT • OVP ON 5V MODELS

VOLTS	AMPS	MODEL	PRICE 1-9
5	25.0 35.0	F5-25/OVP* G5-35/OVP*	$149.00 185.00
12	16.0	F15-15	$149.00
15	15.0	F15-15	$149.00
24	12.0	F24-12	$149.00
28	10.0	F24-12	$149.00

SINGLE OUTPUT — HIGH EFFICIENCY
EFFICIENCY UP TO 66% • RELIABLE LINEAR DESIGN

VOLTS	AMPS	EFFICIENCY @ NOMINAL LINE	MODEL	PRICE 1-9
5	9 12 15	66% 63% 60%	RD5-15/OVP*	$ 99.95
5	14 18 23	63% 60% 57%	RE5-23/OVP*	$130.00
5	25 32 40	63% 60% 57%	RG5-40/OVP*	$220.00

DUAL OUTPUT — STANDARD
TRACKING REGULATORS • ±.02% REGULATION

MODEL	OUTPUT #1	OUTPUT #2	PRICE 1-9
AA15-0.8	12V @ 1.0A or 15V @ 0.8A	−12V @ 1.0A or −15V @ 0.8A	$42.95
BB15-1.5	12V @ 1.7A or 15V @ 1.5A	−12V @ 1.7A or −15V @ 1.5A	$53.95
CC15-3.0	12V @ 3.4A or 15V @ 3.0A	−12V @ 3.4A or −15V @ 3.0A	$84.95

DUAL OUTPUT — HI-VOL
115/230 VAC INPUT • OVP ON 5V MODELS

MODEL	OUTPUT #1	OUTPUT #2	PRICE 1-9
±12 to 15V HAA15-0.8 HBB15-1.5 HCC15-3.0	 12V @ 1.0A or 15V @ 0.8A 12V @ 1.7A or 15V @ 1.5A 12V @ 3.4A or 15V @ 3.0A	 −12V @ 1.0A or −15V @ 0.8A or −5V @ 0.4A −12V @ 1.7A or −15V @ 1.5A or −5V @ 0.7A −12V @ 3.4A or −15V @ 3.0A	 $39.95 49.95 79.95
±18 to 24V HAA24-0.6	 18-20V @ 0.4A or 24V @ 0.6A	 (−)18-20V @ 0.4A or −24V @ 0.6A	 $39.95
±5V HBB5-3/OVP HCC5-6/OVP	 5V @ 3.0A* 5V @ 6.0A*	 −5V @ 3.0A* −5V @ 6.0A*	 $61.95 92.95
5V and 9-15V (Isolated Outputs) HAA512 HBB512 HCC512	 5V @ 2.0A* 5V @ 3.0A* 5V @ 6.0A*	 9-15V @ 0.5A 9-15V @ 1.25A 9-15V @ 2.5A	 $44.95 54.95 86.95

TRIPLE OUTPUT — STANDARD
TRACKING REGULATORS • ±.02% REGULATION

MODEL	OUTPUT #1	OUTPUT #2	OUTPUT #3	PRICE 1-9
BAA-40W	5V @ 3.0A	12V @ 1.0A or 15V @ 0.8A	−12V @ 1.0A or −15V @ 0.8A	$ 69.95
CBB-75W	5V @ 6.0A	12V @ 1.7A or 15V @ 1.5A	−12V @1.7A or −15V @ 1.5A	$ 91.95
DBB-105W	5V @ 12.0A	12V @ 1.7A or 15V @ 1.5A	−12V @ 1.7A or −15V @ 1.5A	$126.95

TRIPLE OUTPUT — HI-VOL
115/230 VAC INPUT • OVP ON 5V MODELS

MODEL	OUTPUT #1	OUTPUT #2	OUTPUT #3	PRICE 1-9
HTAA-16W	5V @ 2.0A*	9-15V @ 0.4A	(−)9-15V @ 0.4A or −5V @ 0.2A	$ 49.95
HBAA-40W	5V @ 3.0A*	12V @ 1.0A or 15V @ 0.8A	−12V @ 1.0A or −15V @ 0.8A or −5V @ 0.4A	$ 69.95
HCBB-75W	5V @ 6.0A*	12V @ 1.7A or 15V @ 1.5A	−12V @ 1.7A or −15V @ 1.5A or −5V @ 0.7A	$ 91.95
CP-131	5V @ 8.0A*	12V @ 1.7A or 15V @ 1.5A	−12V @ 1.7A or −15V @ 1.5A or −5V @ 0.7A	$110.00
HDBB-105W	5V @ 12A*	12V @ 1.7A or 15V @ 1.5A	−12V @ 1.7A or −15V @ 1.5A or −5V @ 0.7A	$126.95
HDCC-150W	5V @ 12A*	12V @ 3.4A or 15V @ 3.0A	−12V @ 3.4A or −15V @ 3.0A	$149.00

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DISK-DRIVE MODEL	OUTPUT RATINGS				PRICE 1-9
	+5V*	−5V*	+12V AVG./PK	+24V AVG./PK	
+5V and +12V CP-249	 0.7A		 1.1A/1.7A		 $ 39.95
+24V and ±5V CP-205 CP-206 CP-162	 1A 2.5A 3A	 0.5A 0.5A 0.6A		 1.5A/1.7A 3.0A/3.4A 5A/6A	 $ 69.95 $ 91.95 $120.00

*INCLUDES BUILT-IN OVP, SET @ 6.2V ±0.4V.

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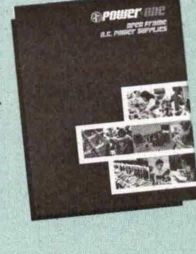

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CIRCLE 18 ON INQUIRY CARD

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A complete model 4645 DCIO combines hardware and software–including a 6010 attached processor, RIM, channel adapter, or DCIO software package. This option attaches directly to the IBM 360/370 mainframe and the high speed system interprocessor bus; it requires no modification of either operating system. Transfer of data from an ARC system common data base is always initiated by the IBM mainframe, and can be accommodated over an IBM byte-multiplexer channel.

With the DCIO, any IBM 360/370 mainframe can be used as an applications processor within the system. Although the IBM mainframe retains the capability of performing data processing and other tasks independently of system operations, any requests for access to the system data base and other resources are communicated at high speeds through the DCIO. When the IBM mainframe is not functioning within the system, the DCIO processor may be used for other data processing operations.

With DCIO, the IBM computer can partition up to as many as eight applications programs to run concurrently using data from the system common data base. The DCIO processor is capable of supporting all eight IBM partitioned programs in a full duplex mode, with no operating system modifications to the IBM mainframe.

An interprocessor bus includes a number of hardware and software components which connect applications processors and file processors into one totally integrated computer system. A coaxial cable physically connects all other components of the bus. The RIM, a component of the interprocessor bus, is a special-purpose data transfer module which connects directly to a processor I/O bus. It provides a unique address for the processor in the system and allows data to be transferred over the system bus at exceptionally high speeds.

RIMS, in turn, are linked to the system interprocessor bus via passive or active hubs. A passive hub acts as a common junction point for connection of up to four RIMS within the system. An active hub is a switching and amplification device used for connection of up to eight (16 optionally) system RIMS or other active hubs. Cable lengths between an active hub and a RIM (or another active hub) may reach up to 2000 ft (610 m). Up to ten active hubs may be attached in tandem to the same cable to permit system lengths of up to four miles (6.4 km).

Circle 140 on Inquiry Card

Add-On Semiconductor Memories Increase IBM System Capacities

IBM-compatible semiconductor add-on memories now available include the in-7730–the first for model 3031, 3032, and 3033 large scale computers–and the in-7700 for several System/370 model computers. Both have been introduced by Intel Memory Systems, 1302 N Mathilda Ave, Sunnyvale, CA 94086 and are based on that company's 4k 2147 static RAM.

Compatibility of the in-7730 with all three 3000 series processors is achieved through an interface unit which converts logic levels for the address, data, and controls between the in-7730 and the CPU. Because speed of the add-on memory is significantly faster than that of the IBM memory, each memory system is timed precisely to the IBM system timing. RAM speed is more than adequate to meet the needs of all 3000 series CPUs. An automatic power-down feature provides extremely low power dissipation when the RAM is not accessed.

The memory system is able to utilize IBM's single-bit error correction and double-bit error detection logic because it is fast enough to interface to the CPU at the IBM memory interface point. High voltage drivers, clocking circuitry, and refresh control logic are eliminated. A memory reconfiguration panel allows maximum memory utilization in the event of a malfunction and the storage module's socket design allows easy removal and replacement of memory storage elements in the field.

The in-7730 can provide up to 8M bytes of add-on memory, depending on the CPU. It measures 60 x 40 x 27" (1.5 x 1.0 x 0.7 m) and includes its own cooling and power systems.

The in-7700 adapts to System/370 models 135, 138, 145, and 148 by changing a set of interface cards. With appropriate cards, this add-on memory is fully hardware and software compatible with the host CPU. Memory upgrades for the 135 and 145 are provided in 128k increments up to a total system capacity of 512k, and in 256k increments beyond that. Increments of 256k are standard for the 138 and 148. Total memory range for the in-7700 is from 128k to 4M bytes, depending on the CPU to which it is attached and the amount of IBM memory installed. A memory reconfiguration panel allows maximum possible memory utilization if a malfunction occurs.

Circle 141 on Inquiry Card

8-Bit ADC Based On Hybrid Building Blocks

A 2-step parallel conversion technique is used in the ADC-TV8B to provide an 8-bit analog-digital conversion. Said to be the first ADC to be based on a hybrid building block concept, the system is fabricated on a single circuit board. Components include a 3-bit parallel decoded A-D, a 15-line (4-bit) D-A, an ultrafast sample-hold, and an ultrafast inverting op amp.

Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021 says that the unit meets requirements of such diverse video applications as digital time-base correctors, frame synchronizers, communications, special effects processors, and digital radar systems. Customer supplied start conversion pulses adjust throughput for any rate up to and including 20 MHz. Characteristics can be optimized at popular conversion rates of 14.3 MHz (17.72 MHz, PAL), four times the color subcarrier frequency rate. No time delays are required externally by the device. Choices of analog input ranges are 0 to 1, 0 to 5, ±1, ±2, or ±5 V. Power requirement is ±15 and ±5 V and operating temperature range is 0 to 70°C. For

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Highly trained operators are not needed. Programming procedures are so easy to pick up. And an interactive display system makes operation easier still. Test systems are stored on solid-state cards, providing reusable data memory.

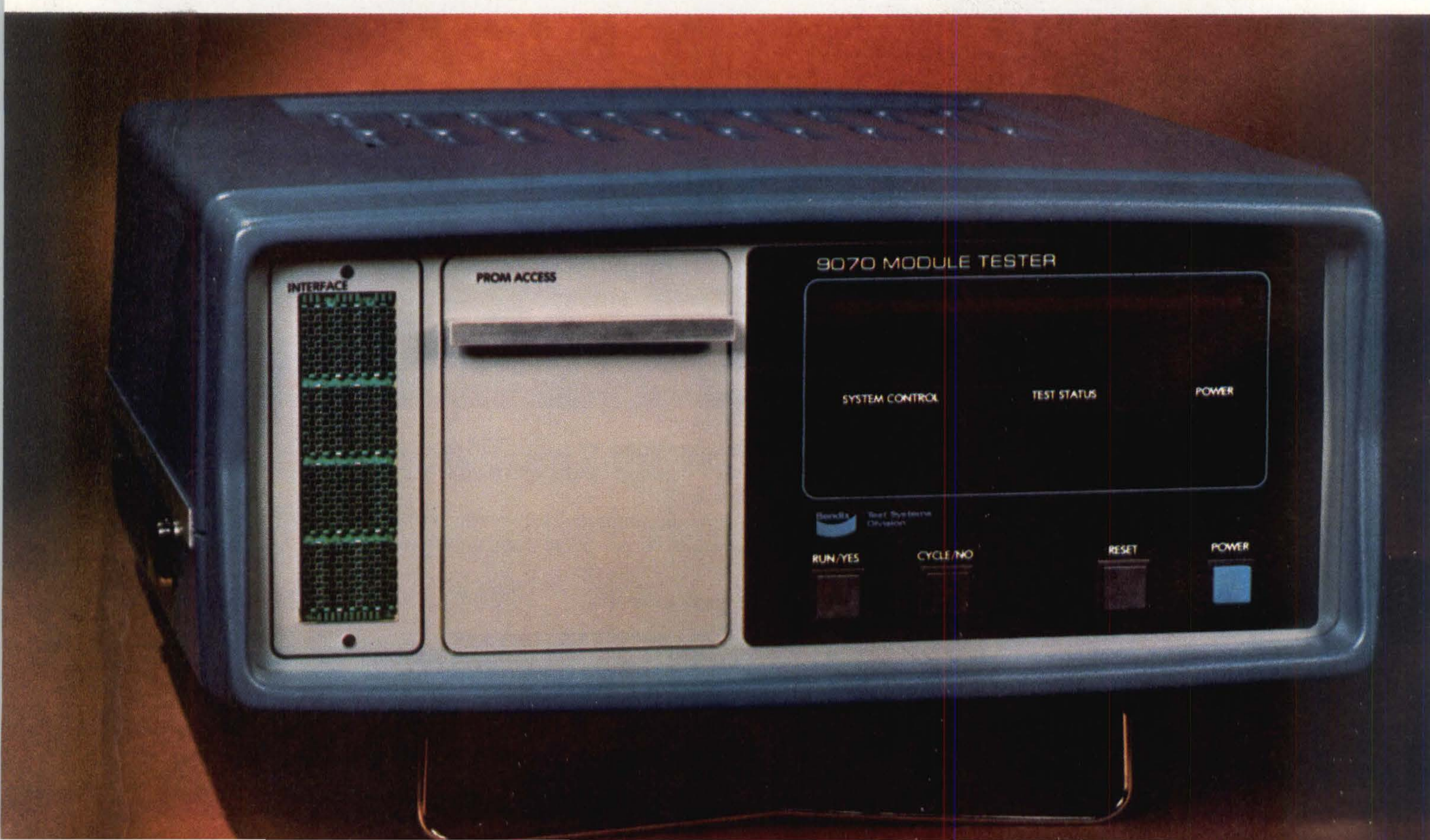
The Basic Bendix unit is capable of testing cards to 64 pins and has the capacity to expand to 256. Additional options are available including:

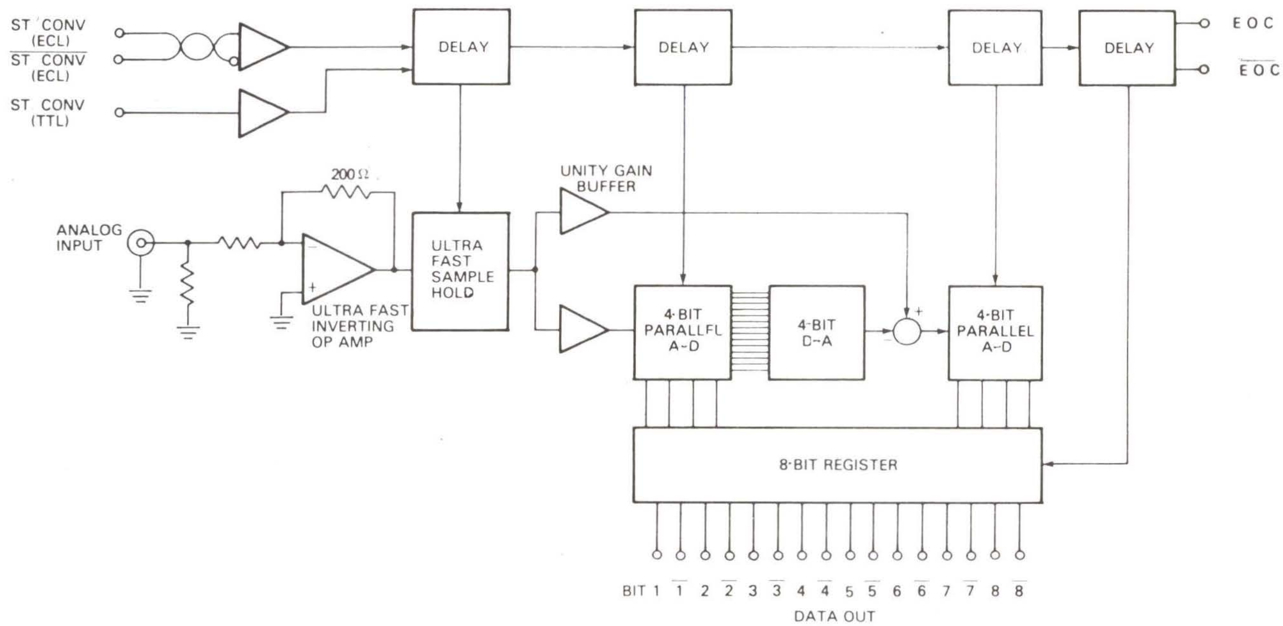
- **Fault Isolation Testing**
- **Digital Voltmeter/Frequency Counter**
- **Teletype Interface and Advanced Software Aids.**

For more information, contact: Bendix Corporation, Test Systems Division, Teterboro, N.J. 07608. Or call (201) 288-2000, extension 1789.

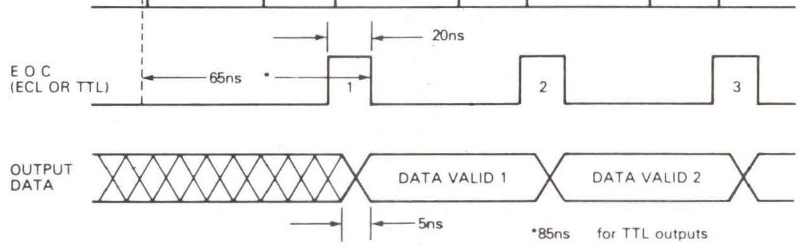
Bendix

CIRCLE 20 ON INQUIRY CARD





Block diagram of Datel Systems' 8-bit, 20-MHz video ADC. Analog input comes from terminated rf connector to ultrafast inverting op amp which scales input to desired level for sample hold and ADC



Timing diagram of ADC-TV8B. 50-ns max time between conversions provides 20-MHz conversion rate. Conversion delay (time from start convert pulse to time data are valid) is 6.5 ns for ECL version and 85 ns for TTL

military radar applications the 7.5 x 4.25 x 0.875" (19.1 x 10.8 x 2.2-cm) package can be supplied with −55 to 85°C operation with hermetically sealed components.

External interface may be either ECL or TTL. Analog input termination impedance may be 50, 75, or 93 Ω, depending on model chosen.

A conversion is initiated by an input start convert pulse which begins a timing sequence determined by four ECL digital delay circuits. The first delay causes the sample-hold to go from the tracking mode to the hold mode for about 30 ns. Output of the sample-hold is buffered and goes to the first 4-bit A-D where the four most significant bits are converted and decoded into binary form. This A-D simultaneously drives a 4-bit D-A by means of a 15-line output.

The D-A output is subtracted from the buffered sample-hold output and the analog remainder goes to the second 4-bit A-D which converts the four least significant bits into decoded binary form. The last delay circuit puts out a 20-ns pulse, indicating that data are ready at the output of the 8-bit register.

Circle 142 on Inquiry Card


PDP 11/03-L

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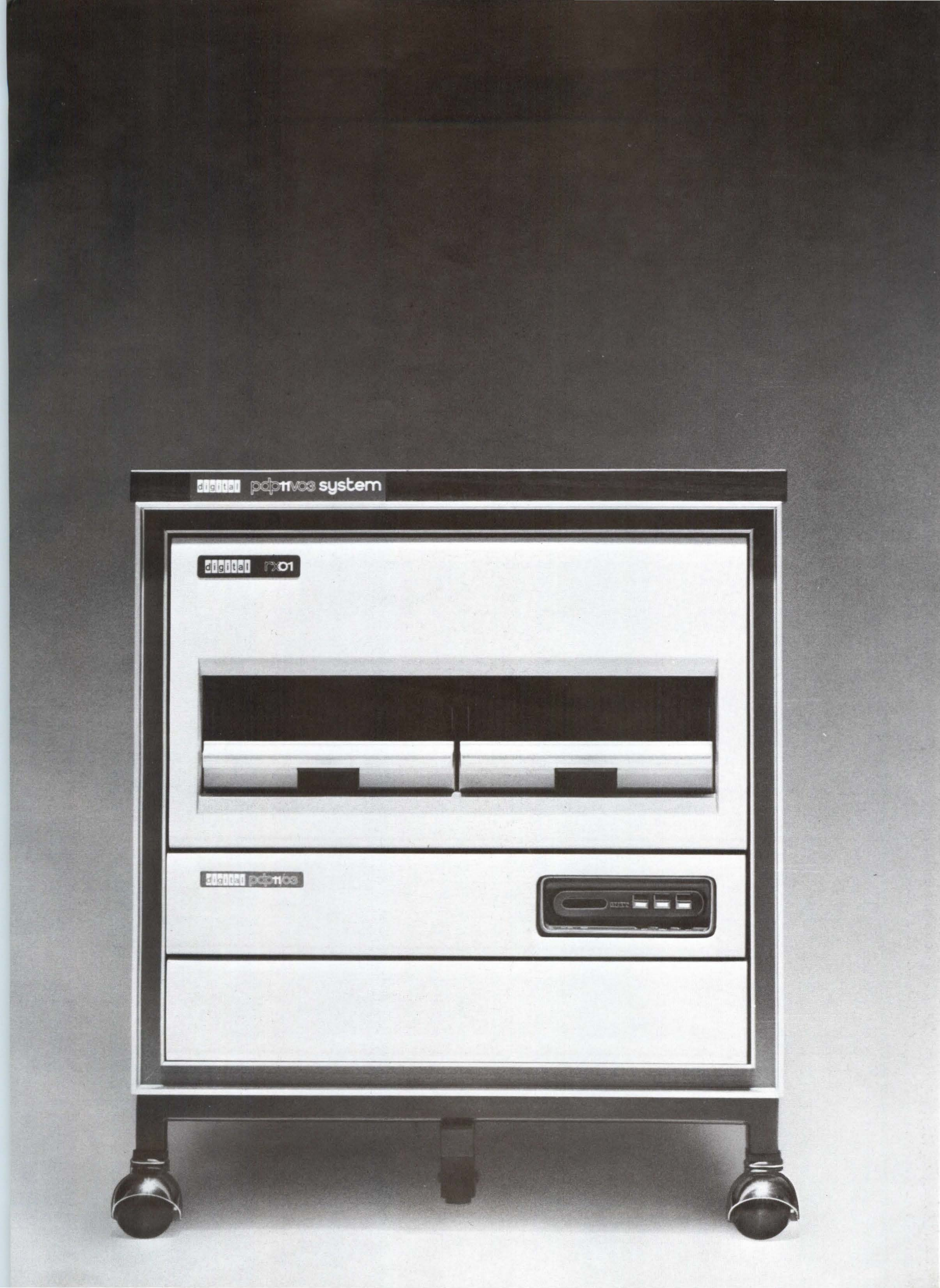

digital pdp11v03 system
digital rx01
digital pdp11/03

Data Encryption Devices Protect Transmission Of Sensitive Data

Data security products using the National Bureau of Standards Data Encryption Standard help safeguard private and valuable information stored and transmitted by computer systems. These products make information appear meaningless by enciphering it in secret code, and decipher it by using a variable number called a "key." Sensitive information can be protected from unauthorized disclosure or alteration even if the enciphered data passes out of the user's possession or control.

The products "scramble" data with a sophisticated algorithm which can use any one of more than 70×10^{15} keys of 56 binary digits each to encipher and decipher data. Only the key need be kept secret after the information is enciphered. Keys can be changed frequently, providing increased protection.

International Business Machines Corp, Data Processing Div, 1133 Westchester Ave, White Plains, NY 10604 has introduced two software data encryption devices, the 3845 and 3846, and a cryptographic subsystem. The tabletop 3845 and 3846 can be used for point-to-point communications to encipher data transmitted between a variety of IBM and/or other manufacturers' computers and terminals; the cryptographic subsystem is designed for use in System/370 computers and data processing networks.

A data encryption device on each end of a communications line enciphers and deciphers information as it is sent and received. They can operate with a variety of line protocols and codes that can be selected and changed by users with a handheld entry unit, which also can be used to enter and change keys. Speeds up to 19.2k bits/s can be achieved. The devices are user-installable and compatible with frequently-used carrier interfaces.

The cryptographic subsystem can be used to encrypt data stored in magnetic tape and disc files or when it is being transmitted. It includes three separate products: programmed cryptographic facility program product, advanced communications function for virtual telecommunications access method encrypt/decrypt feature, and the encrypt/decrypt feature for the company's 3276 control unit display. The first two products are software; the third is a hardware feature.

When used to encipher/decipher transmitted data, the cryptographic program product can make a unique key for each communication "session" between a computer and terminal. Once produced in the computer, this session key is itself encrypted using another key called a "device" key—stored in the computer and terminal. Transmitted in this encrypted form, the session key is received, deciphered, and stored by the terminal, using the device key and the terminal encryption/decryption feature. In this way, the unique session key is never transmitted in unciphered form.

After the session key is used to send encrypted information between the computer and terminal, it is erased by both devices. When the cryptographic program product is used to encipher information sent to another System/370, the session key is enciphered with an intermediate key used by both computers.

In a telecommunications network, each display system with the encryption/decryption feature can have its own device key. Data can be sent over a common, unprotected line, enciphered with different device and session keys. Each display system can decipher only the data enciphered under its own set of keys. Terminals without the feature on the same line will not decipher data. Using this method, enciphered information can be passed through an intermediate controller or computer in "scrambled" form to another device where the message can be deciphered with the proper key.

Enciphered and deciphered messages can be mixed in a network, and encrypted data can be sent and received without the need for operators' knowledge or intervention. These telecommunications and network handling functions are performed by the ACF/VTAM encrypt/decrypt feature.

The Cryptographic Program Product also can be used to help protect data files stored on tape reels and disc packs. In this case, data are written on the file enciphered with a special key produced by the program. Enciphered files are unintelligible without this "file" key.

Circle 143 on Inquiry Card

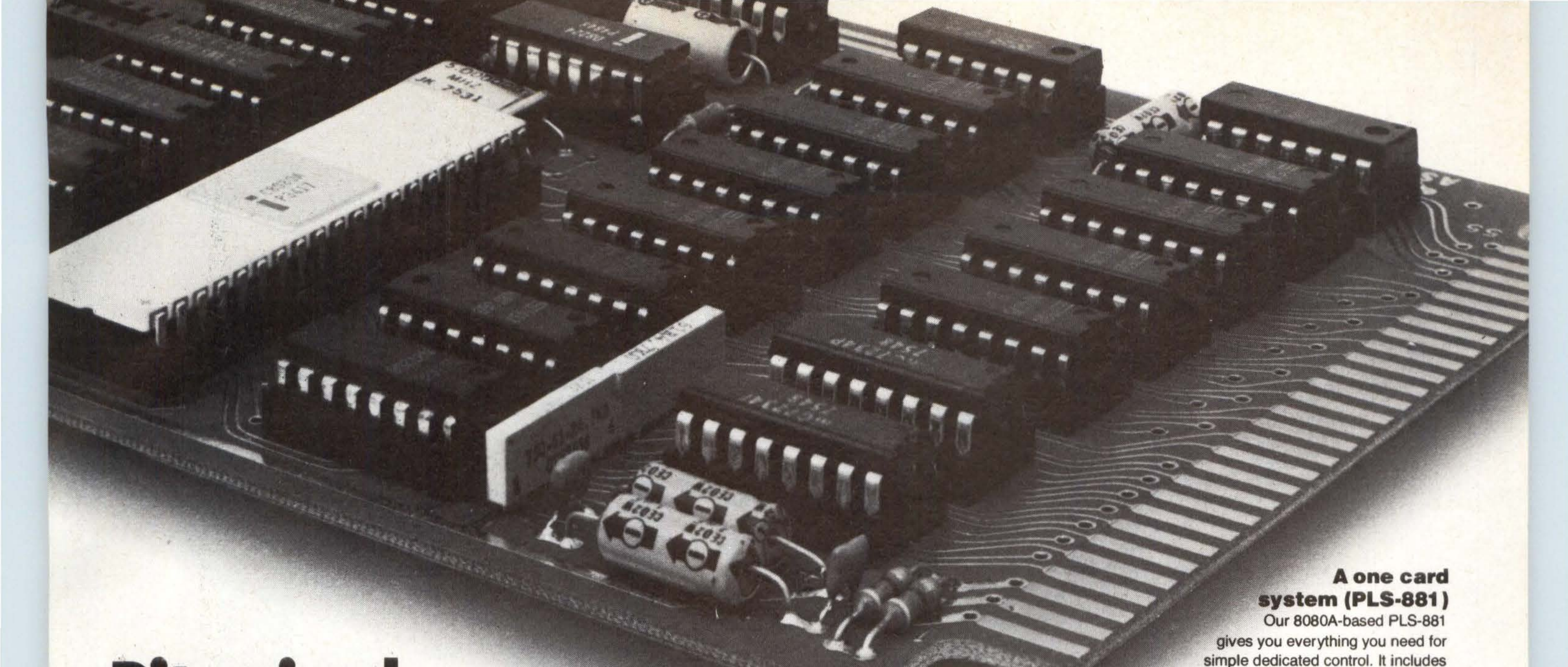
Dark Trace Image Techniques Permit Bright Large Screen Displays

A video projection technology that uses "dark-trace" imagery techniques, Data Beam™ permits high resolution display of computer-generated alphanumerics with selective erase at high picture brightness on large screens. The system, made possible by an agreement between Advent Corp, 195 Albany St, Cambridge, MA 02139 and Cathodochromic Technology, Inc of Lexington, Ky, incorporates the dark trace technology in a version of Advent's LightGuide® projection tube. It is expected to find primary use in the large screen display of business and financial data which are slow scan transmitted as alphanumerics over voice grade telephone lines.

At the heart of the projector is a catadioptric projection CRT using a dark-trace target. The target is coated with sodalite rather than a conventional television phosphor. When written on by an electron beam, this white powder turns magenta in a stable transformation requiring no video refresh to sustain the image. The target is continuously illuminated by white light which projects the image to the viewing screen through an aspheric corrector lens. Target size is approximately 2 x 3" (5 x 7.6 cm) and the optical system has a 25X magnification, thus providing a 7' (2-m) diagonal image.

The optical configuration allows projection of an image that is written on the cathodochromic screen surface nearest the electron gun (rear surface). This provides distinct advantages of higher resolution and contrast, improved erasure, shorter erase time, and longer device life time over front surface projection techniques. Since the rear surface is nearest to the impinging electron beam, it gets the hottest during erasure and erases best. Improved erase time is achieved because only the particles comprising the rear surface need be erased, rather than the entire thickness of the screen. Higher resolution is attained because the spot size of the beam is preserved and is not subject to scattering as with a front surface technique.

Three modes of operation are used: write, full screen erase, and selective erase. In full screen erase, the electron beam current is set to max-



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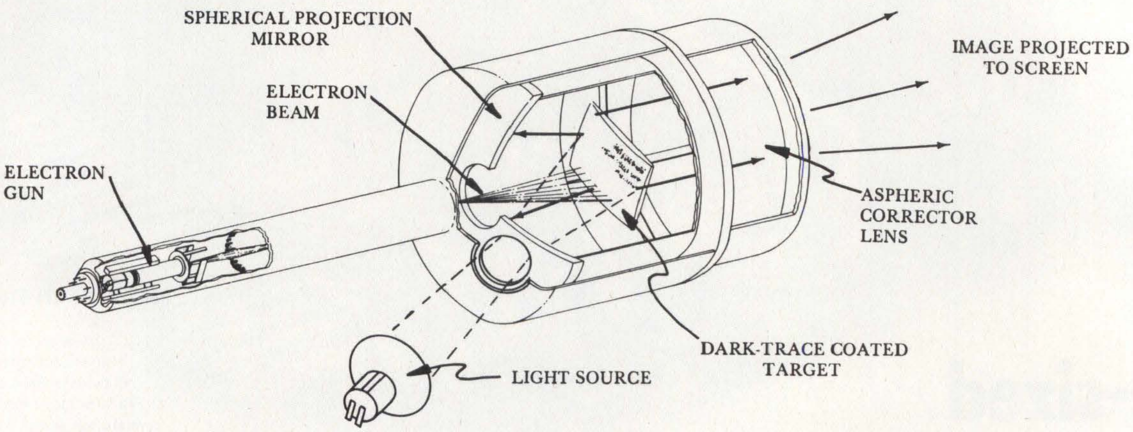
CIRCLE 22 ON INQUIRY CARD



Catadioptric projection CRT used in Advent Corp's computer graphic video projector system. Normal 30-image/s flicker is not present since refresh is not required (which also eliminates need for refresh memory)

imum value and the focus is adjusted to give a 10-mil spot size. Vertical and horizontal deflection amplitudes are adjusted to provide slight overlap of adjacent erased points and spot dwell time is adjusted to insure sufficient heating to exceed the erase threshold. Using these settings with a sodalite:Br target, the entire screen may be erased in 3 s.

Writing rate depends on type of information and method of writing. In the case of 9 x 7 dot matrix characters, a speed of 240 char/s is possible, writing dark characters on a light field; 480 char/s write is possible with light characters on a dark field.

Selective erasure is achieved by overlaying the character matrix with a 5 x 4 erase matrix. A single character may be erased in 0.7 ms.

A completely flat image plane is possible with the projector because the image forming target is an unstressed machined aluminum billet. Since the image is "real" (not virtual), it can be enlarged, diverted, or used to expose sensitized copy material of any size.

Light output of the projector can be selected at will. The present Schmidt tube system has a mirror aperture of f 0.7 and an efficiency of about 20%. A light input of 4000 1m will result in a projector output of 800 1m. With the 7 ft (2-m) screen, the picture brightness of such a projector would be 300 fL.

Circle 144 on Inquiry Card

Digital Image Processor Implemented by Language Techniques

Software development and installation have been completed by Forth, Inc, 815 Manhattan Ave, Manhattan Beach, CA 90266 on a sophisticated digital imaging display control system based on a Digital Equipment Corp PDP-11/40 minicomputer. The system is installed at NASA's Greenbelt, MD facilities.

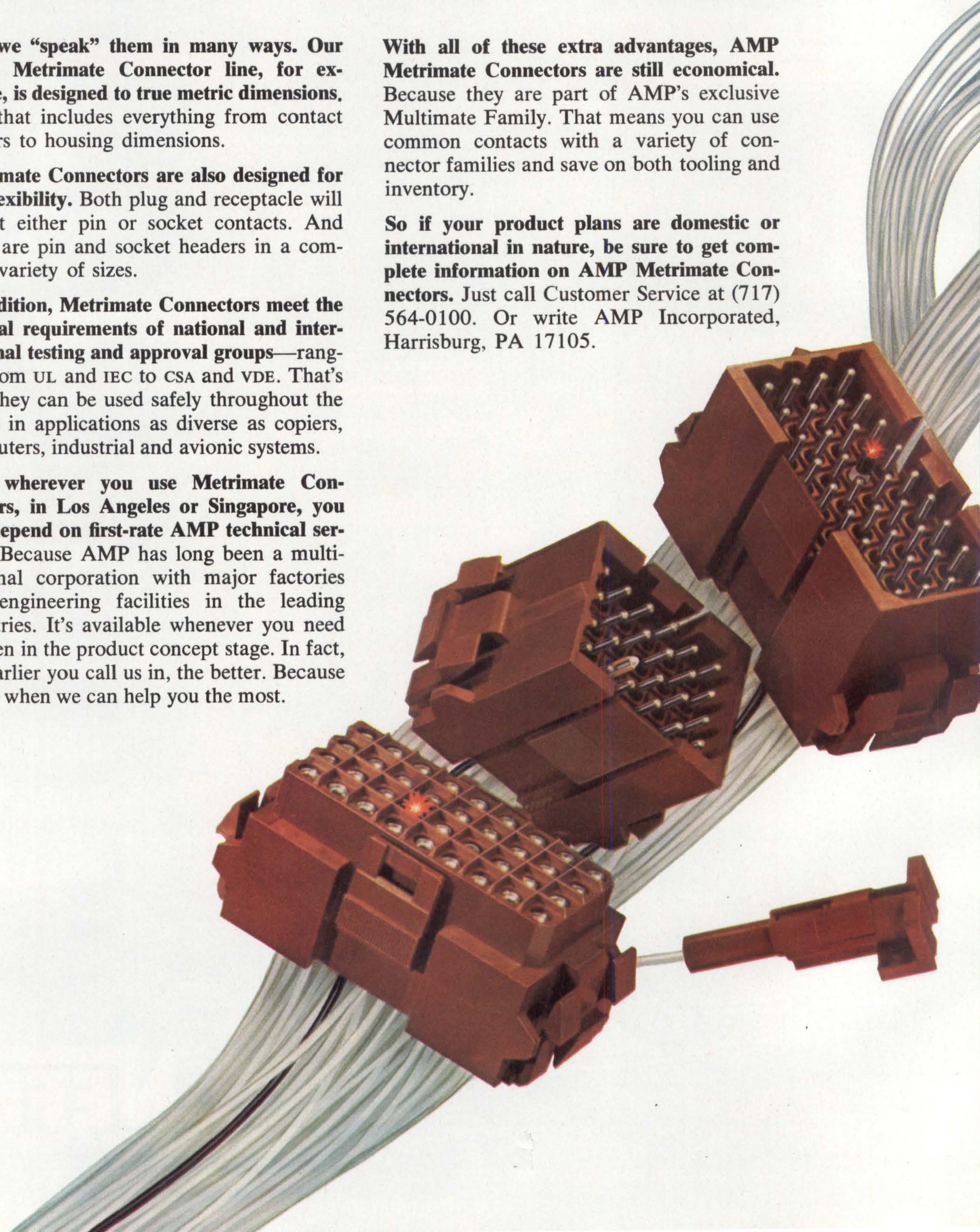
The system requires only 8k words of memory to accommodate the image FORTH development package, including all hardware, standard utilities, and options; multiprogrammed executive; and data base and file management packages. Applications support includes general-purpose 2D graphics, image library maintenance, and image processing functions such as windowing, combinations, histograms, density maps, scaling, enhancements, and rotation.

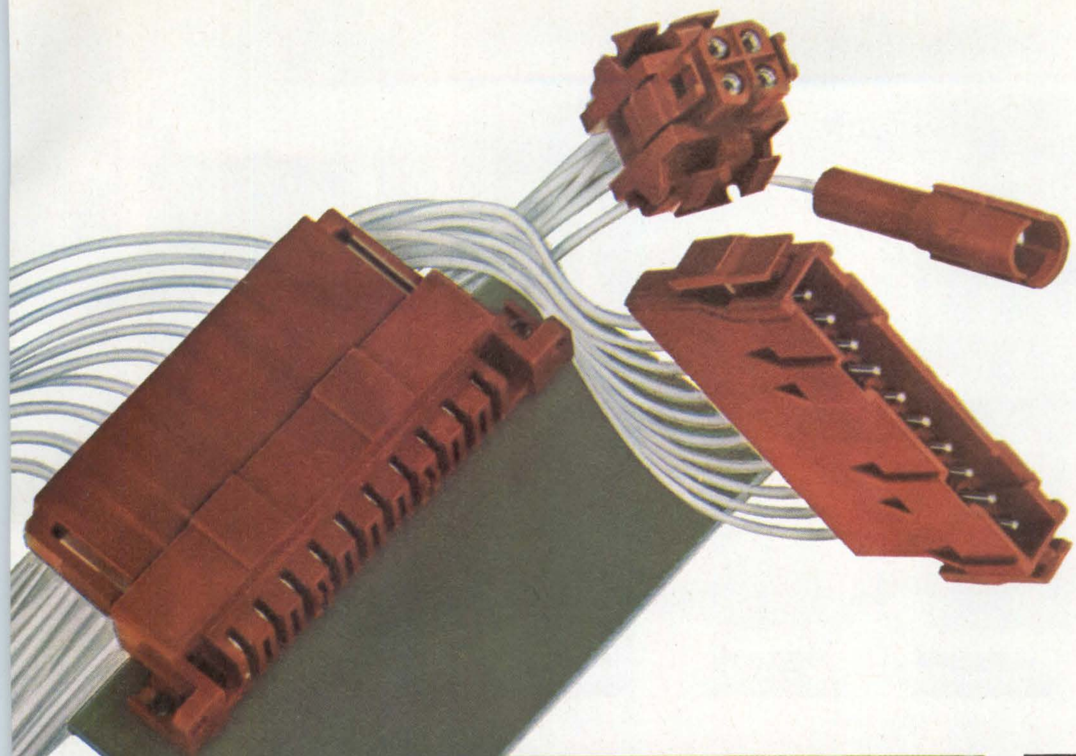
Standard devices supported include the CPU, terminal, two disc drives, and two magnetic tape transports. In addition, application-oriented special devices concurrently supported include a Comtal digital image processing system, a graphics display unit, and a multichannel data acquisition controller. All devices can be driven at maximum speed consistent with hardware specifications.

Circle 145 on Inquiry Card

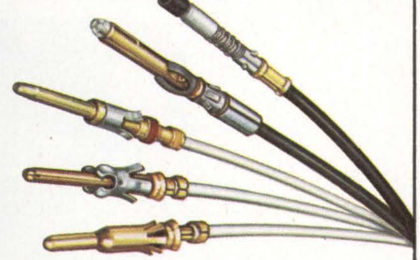
NVRAMs, EAROMs, and μPs Featured in Expandable POS Terminals

Performance of recently announced electronic point-of-sale terminals can be increased drastically by adding plug-in modules. The 2140 retail system is based on control by an MED-80 microprocessor and uses nonvolatile random-access memory (NVRAM) for storage of changeable data as well as electrically alterable read-only memory (EAROM) for high programmability. With NVRAM there is no requirement for battery backup memory protection. Instead of using a single microprocessor to control all of its functions, the terminal can





AMP has a better way... The Multimate System.



It means that the wide range of Multimate connector families can accommodate a variety of common contacts to handle signal, power, coax, and even fiber optics. And you save on both inventory and tooling. In addition to Metrimate Connectors, some of the other families that are part of Multimate include: Circular Plastic Connectors . . . Low Cost Sealed Connectors . . . "M" Series Connectors . . . and several more.

For additional information on these Multimate products, just call Customer Service at (717) 564-0100 or write AMP Incorporated, Harrisburg, PA 17105.

CIRCLE 24 ON INQUIRY CARD

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The SEL BUS transfers data at the rate of 26 megabytes per second. No other computer system in this class offers this performance—the SEL BUS is the industry standard for speed. And only the SEL 32 employs microprogrammable, independent I/O; I/O processing doesn't steal CPU cycles.

2. A Family From Which To Choose

SEL offers a family of true 32-bit computers:

- SEL 32/35—processor with 900-nanosecond memory and floating-point arithmetic;
- SEL 32/55—flexible single and multiple CPU configurations with up to one million bytes of 600-nanosecond memory;
- SEL 32/75—supports up to 16 million bytes of memory. And the only computer with independent, intelligent I/O to process and transfer data directly to and from memory.

3. Sharp-Pencil Pricing

Whether you buy one CPU or a hundred, we'll give you more computer performance for each dollar you spend.

4. Reliability

Hundreds of SEL 32 systems are operating in critical applications which demand availability, such as simulation, power plant monitoring, and telemetry.

5. On Time Delivery

When you schedule the delivery of an SEL 32 computer, we know it's an important date. So when we say it will be there... it will be there.

6. Support

Our computers are in operation on land and sea in most parts of the world. Parts depots and support services are located worldwide at strategic locations. You will find our offices in major cities abroad and in most industrial centers in the United States. This is extremely important when your computers are employed in critical real-time, on-line applications.

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use several, each performing a specialized task in the total system.

Introduced by NCR Corp, Dayton, OH 45479, the system can grow from a basic electronic cash register to a fully featured retail terminal, depending on user requirements. When the retailer needs greater performance, such as the ability to record data on magnetic cassette tapes so that it can be automatically processed later, all that is required is the insertion of a second circuit board in the system and plugging in the required peripherals. Other performance features, such as the ability to automatically read merchandise tags with a scanning device or the ability to automatically read information encoded on the magnetic stripe of a plastic card, can be added in the same manner.

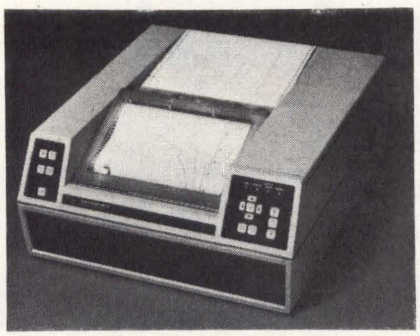
Data communication can be maintained also with a computer system at another location, and one master terminal can automatically summarize totals for up to 15 other connected units. Memory capacity of 128k bytes can be shared by other linked terminals. As many as three facsimile-type matrix printers can be included.

The two first models of the family are for general-purpose use. The basic version of the first model, the 2140-2000, features a 17-column, twin-station alphanumeric printer for journal, receipt and forms validation, the choice of two display panels, and up to 50 totals. Basic versions of the second model, the -7000, offer additional features including a choice of printer combinations, larger electronic memory providing up to 225 totals, and the ability to display instruction messages to lead operators through complex transactions.

Circle 146 on Inquiry Card

Printer/Plotter Combines True Vector Graphics And Fast Text Printing

A microprocessor-controlled desktop hardcopy unit, the HP 7245A printer/plotter, announced by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, links to systems that interconnect with the HPIB/IEEE-488 interface bus. It contains



Desktop HP 7245A printer/plotter measures 19.1 x 17.5 x 7.9" (48.5 x 44.3 x 20 cm). It interfaces to systems interconnected with HPIB/IEEE-488 interface bus. 12-resistor thin-film printhead prints 7 x 9 half-shifted matrix characters; 14 x 9 matrix font is used for printing titles

both printer and plotter functions and features bidirectional paper drive for long axis plots and unattended plotting, moving thermal printhead, and such features as user unit-scaling, graph rotation, point digitizing, seven dash-line fonts, 13 character sets, and user-definable characters.

A bidirectional paper drive advances the chart for plots with Y-axes as long as 16.4 ft (5 m). Charts can then be returned to the starting point with high accuracy.

Bidirectional sprocket paper drive and microstep motor drive provide a plotting repeatability of 0.010" (±0.25 mm) maximum from any point in any direction and a minimum addressable resolution of 0.004" (0.102 mm). The smallest step is 0.001" (0.025 mm). Highest speed is 20 in/s (50.8 cm/s) in each axis for positioning and 10 in/s (25.4 cm/s) when plotting.

A thin-film printhead with 12 resistors prints 7 x 9 half-shifted matrix characters at 38 char/s in four orthogonal directions. This font allows 80 columns to be printed across the 8.5" (21.6-cm) wide paper. A larger 14 x 9 matrix font is used to print titles at 19 char/s in a 44-column format. A single larger resistor in the printhead is used to draw all vectors and the five available drawn character fonts in variable sizes, slants, and directions.

The 128-character ASCII set has 96 upper and lower case characters and 32 printable control characters to ease program debugging. In all, there are eight matrix fonts, including six foreign character sets. All matrix fonts can underline characters while printing.

Included are 44 built-in programmable instructions for point digitizing, user unit-scaling, window plotting, graph rotation, seven dash-line fonts, and user-definable characters. Standard printer escape code sequences enable the user to set and clear tabs, feed or reverse forms, change character size, select character sets, and print all 128 ASCII characters. Other features include paper and top-of-the-page sensors for both metric and English-sized pages, a variable left margin, a 120-character buffer, and a built-in diagnostic self test.

Estimated delivery for the printer/plotter is four to six weeks ARO. U.S. price is $4600.

Circle 147 on Inquiry Card

μP Business Computer System Promises High Performance at Low Cost

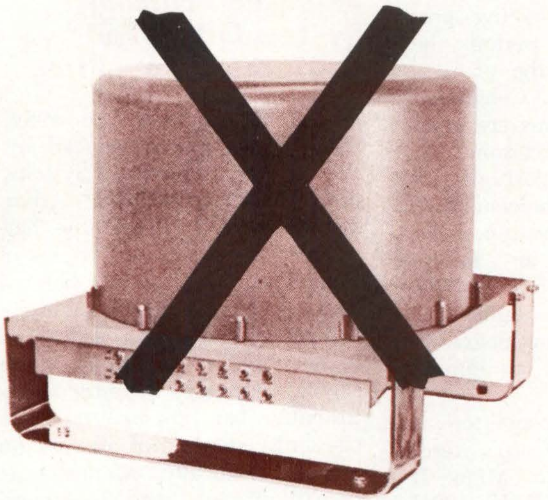
Performance and functional capability of a Z80-based computer system for small business data processing are said to be competitive with those of minicomputer systems selling for over 50% more. Announced by Info 200 Corp, 20630 S Leapwood Ave, Carson, CA 90746, the complete system consists of microcomputer, dual flexible disc drives, high speed printer, video terminal, and business applications software. It features S-100 bus architecture and contains up to 56k of RAM, 8k of EPROM, a filtered forced-air cooling system, and heavy duty power supply.

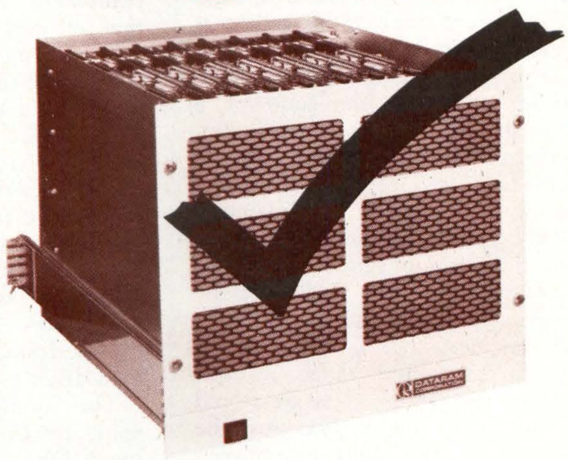
Mass storage is provided with Per-Sci dual flexible disc drives. The 160-char/s, 132-column line printer provides all 96 ASCII upper/lower case alphanumeric and graphic characters, including true lower case letters with descenders. Printer capabilities include graphing and charting. The video console uses a commercial quality keyboard with numeric keypad and displays all ASCII characters.

Circle 148 on Inquiry Card

DEC® RC-11 and RF-11 fixed-head disc...and Data General Novadisc® users:

Replace Fixed-Head Disc with Dataram BULK CORE





Now, all the remarkable features of Dataram's BULK CORE memory system are available to you in a unique storage peripheral with complete interfaces to emulate DEC and Data General fixed-head discs.

Basic building block of this dramatic, new peripheral is Dataram's BULK CORE module, which provides 256 kilobytes of storage on a single board. Eight of these modules can be packaged in a standard 19" chassis to provide two megabytes of storage.

To give you more of what you can't get from fixed-head discs. BULK CORE gives you microsecond-range access time, high reliability, and greatly improved maintainability. And at a price unheard of for core or semiconductor memory. Until now.

Until Dataram made its BULK CORE memory system plug-compatible with PDP-11 and Nova® minicomputers. To provide:

- **Access time 1/10,000 of FHD**
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Reasons enough to find out more about BULK CORE. If you use a DEC or Data General minicomputer—or any kind—and want to move ahead in performance, move a BULK CORE into your system.

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Canada: Tracan Electronics Corporation, Ontario/Quebec/British Columbia • **Belgium/Luxembourg/Netherlands:** Synelec Information Systems, (02) 647-67-12 • **France:** YREL, 950-2224 • **Italy:** Telcom, s.r.l. 422-8646 • **Sweden/Finland/Norway:** Teleinstrument AB, 08-380370 • **Spain:** Aupoca, (01) 457-53-12 • **Switzerland:** Intertest AG, 031-224481 • **United Kingdom:** Sintrom Ellinor Ltd., (0734) 85464 • **West Germany/Austria:** O.E.M. Elektronik GmbH, 0711-798047 • **India:** Industrial Electronic Instruments, 79281 • **Israel:** K.D.M. Electronics Ltd., (03) 58232 • **Japan:** Matsushita Electric Trading Co. Ltd., (03) 435-4552 • **Australia/New Zealand:** Anderson Digital Electronics, (03) 543-2077.

Digital Data Converter Gives Airborne Radar Automatic Acquisition

Fully automatic overland tracking capability has been provided to the Navy Grumman E2C Hawkeye by addition of a digital signal converter to the AN/APS-125 radar system. This is the only airborne early warning system to have automatic acquisition.

In operation, each radar return is processed to reduce ground clutter and is presented to the digital signal converter (DSC) in the form of a vector in rectangular coordinates. The DSC converts the vector to polar coordinates to reduce storage requirements, and then stores it in memory, a 1.7M-bit shift register that allows return data to be stored in one or more range increments that cover the full operating range of the radar.

The memory holds data derived from 16 successive radar returns. Whenever new return data are stored in memory, the DSC processes the Doppler frequency shift information in the new return and in the 15 preceding returns. A Fourier analysis is performed on the Doppler shift information at every range increment by a 16-point, radix-4, fast Fourier transform (FFT) processor. Output of the FFT processor for every range increment is a set of 16 complex coefficients that represent the target velocity at that range. These outputs are converted to amplitude, rounded, and transmitted external to the DSC for further processing.

Correct operation of the DSC is continually verified by its built-in test equipment. During the inactive portion of each interpulse period, the test equipment initiates the processing of 16 test problems. Calculated solutions to those problems are compared to the known correct solutions, and results of the comparisons are reported to the flight technician. Two reports are provided. One report informs the technician if any failure is present; the other informs the technician whether any failure or combination of failures has degraded the performance of the equipment by 3 dB or more.

The digital signal converter is made by Control Data Corp's Aerospace Div in Minneapolis, Minn. It meets requirements of MIL-E-5400H for Class 1AX equipment.

Circle 149 on Inquiry Card

Business Computer System Has Flexible Configuration

A powerful distributed data entry and processing system, said to offer business management users flexibility in power, ease of use, configurability, and data security, has been introduced by Sycor, Inc, 100 Phoenix Dr, Ann Arbor, MI 48104. The 445 system will support up to 256k bytes of main memory, 70M bytes of disc storage, eight 2000-character video data stations, and a combination of bidirectional matrix and line printers. Sycorlink™ provides convenient linking of multiple processors. Disc files on any system can be accessed by any other system in this network. The link also allows any processor in a network to share peripherals such as magnetic tape drives, printers, and modems.

A data station incorporates an easy-to-read, glare-resistant, 15" (38-cm) screen, housed in a compact, desktop unit which can be located up to 2000 ft (610 m) from the processor. An optional display stand enables the operator to adjust the angle of the screen for maximum eye comfort. The data station also has three screen intensities so that data fields may be highlighted.

Multiple processor architecture increases system throughput. In addition to the main processor, additional processors are used in each peripheral controller, freeing the main processor to carry on its chief function.

Five printer speeds are available. The Sprinter™, a bidirectional, microprocessor-controlled matrix printer, operates at 60, 120 or 180 char/s and can be located up to 2000 ft (610 m) from the processor. In addition, 300- and 600-line/min printers may be used. Other peripherals include a built-in high-speed cartridge tape for disc backup, and cassette, diskette, and magnetic tape drives for interchange media.

The system is designed for data communications and offers bisynchronous and synchronous data link control (SDLC) transmission modes at speeds up to 9600 bits/s. Various communications programs are available.

Circle 150 on Inquiry Card

µP-Based Drafting System Offers Full Features at Low Price

An interactive design, drafting, and mapping system announced by The Bendix Corp, Aerospace Systems Div, 3621 S State Rd, Ann Arbor, MI 48107 is said to sell for half the price of other typical systems of this type. The microprocessor-based Datagrid II system allows interactive placement and editing of lines, circles, arcs, symbols, and text. A rough sketch, drawing, or map source information can be converted to a precise finished piece of artwork quickly and economically. Memory consists of 20k of RAM and is expandable.

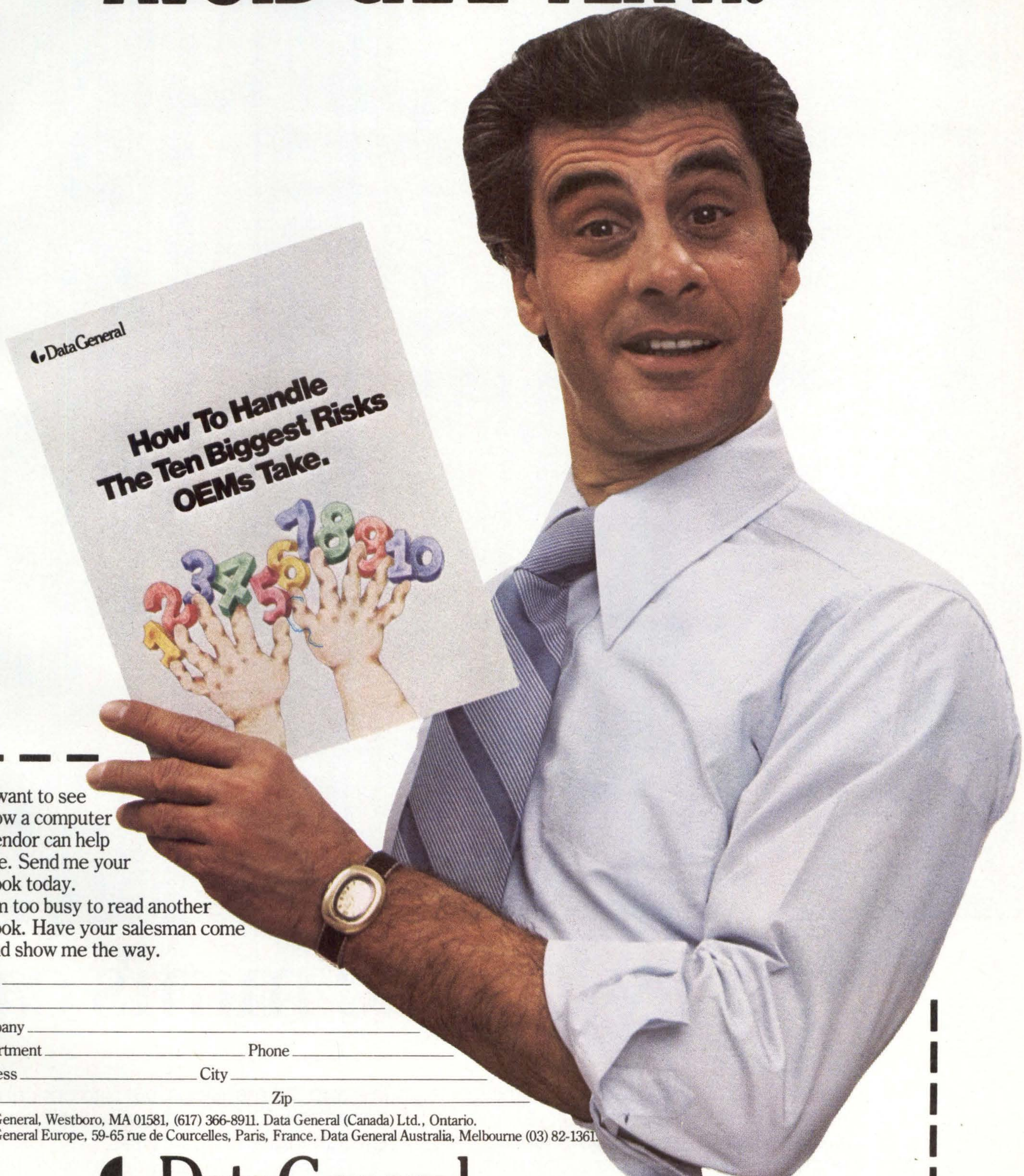
By use of "menu" picking techniques and a free moving cursor, the operator merely points to the operating instruction, then to the picture of the selected symbol, and finally to the place on the drawing where the symbol is to be placed. A CRT terminal displays the drawing as it is entered and permits editing and annotating via a keyboard.

A free cursor precision digitizer incorporates a 16-bit, microprocessor with 8k of RAM. This digitizer includes features such as a large grid work surface on a powered lift pedestal base, keyboard display console, cassette-loaded software, and an applications software library.

A digitizing program guides the operator, step-by-step, through the setup procedure. It then monitors the work for format and procedural errors with instantaneous display of prompting messages, digitizing conditions, and true map or drawing coordinate data in values recognizable by the operator. Capabilities can be extended through operator-tailored programs or expanded to a fully interactive drafting and mapping system adding a CRT display, dual floppy disc, 12k RAM, and interactive graphics software program.

Circle 151 on Inquiry Card

READ THESE TEN CHAPTERS. AVOID CHAPTER 11.



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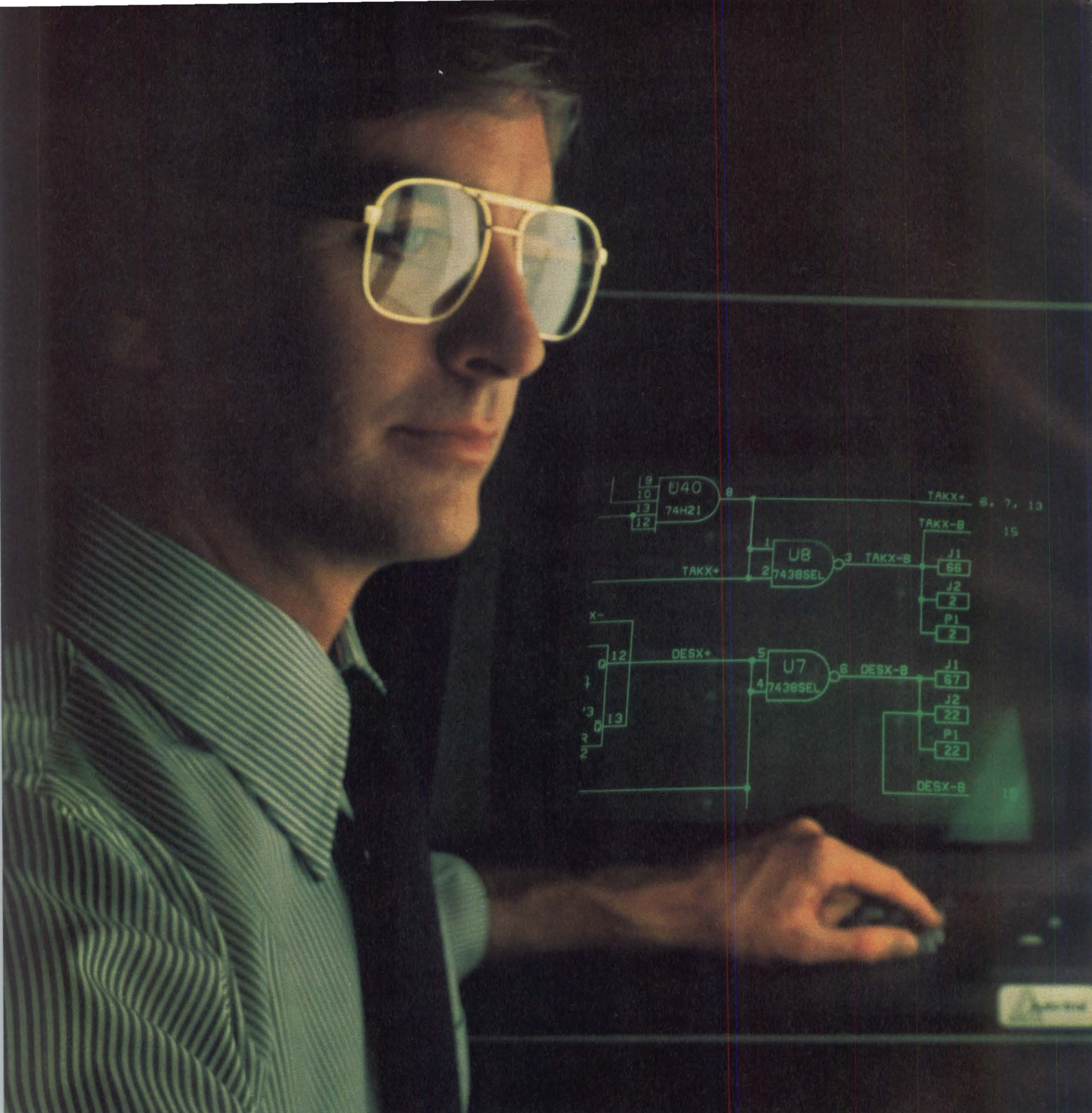
U40
74H21
U8
7438SEL
TAKX+
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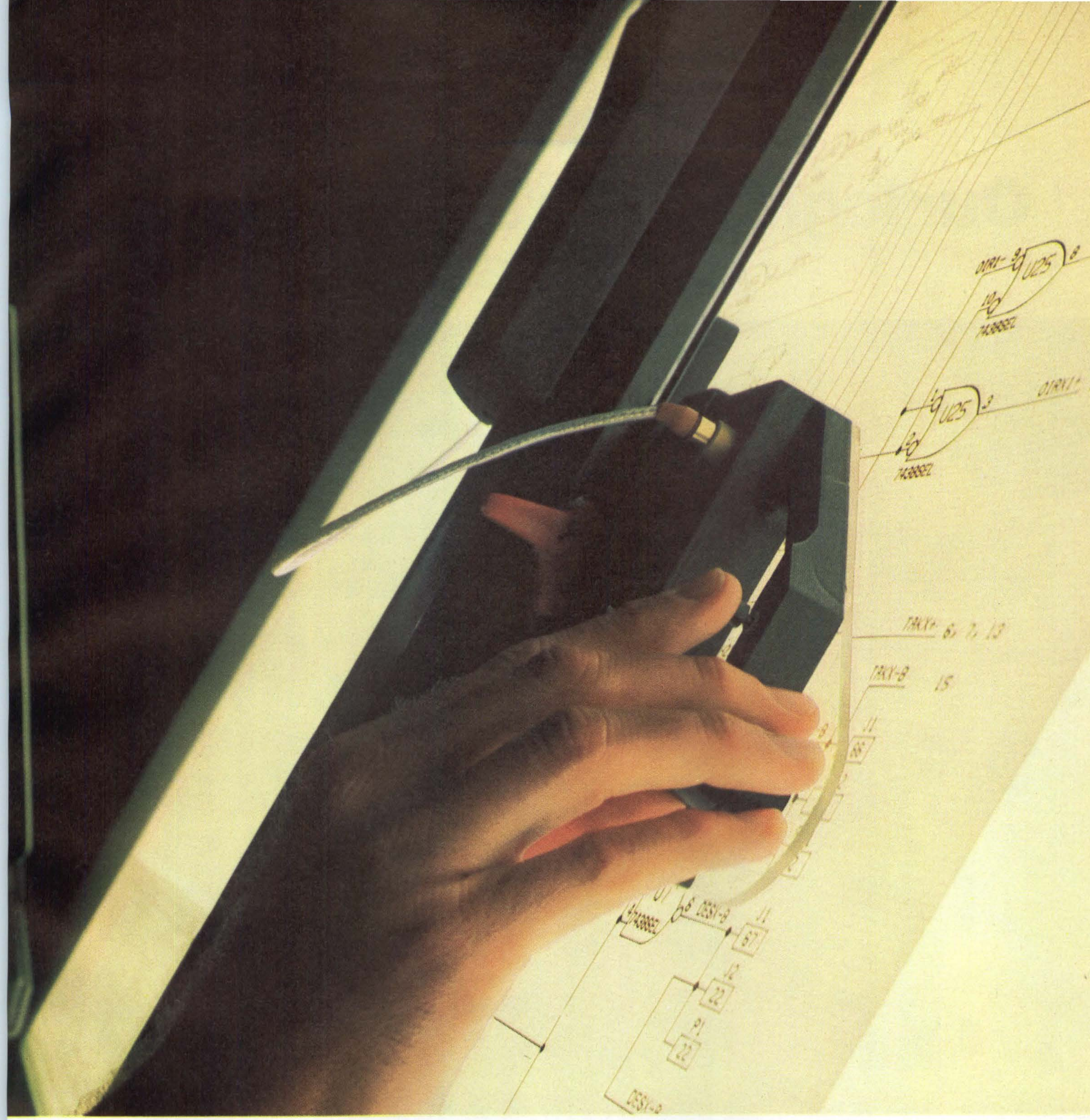

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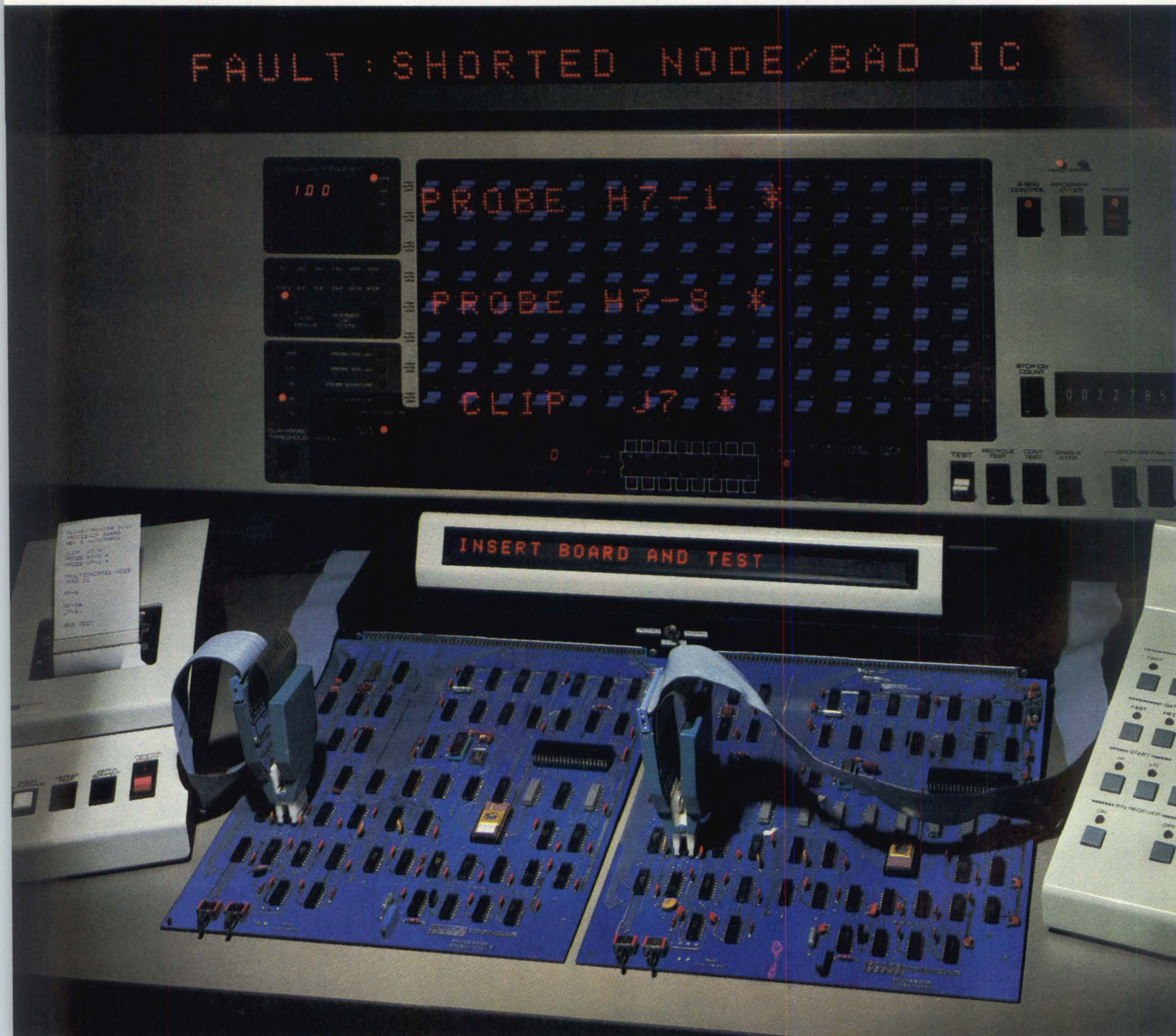


And you can make it downright brilliant.

Fluke logic testers are ahead of their time—the first to test µP boards at rated speed.

We've gone beyond simply handling µPs in circuit. Take our computer-guided probing system; we call it "Autotrack,™" you'll call it *indispensible.*

Autotrack minimizes the back-probing necessary to find the defect, and automatically directs your operator's probing. A powerful built-in algorithm is the secret.

Simply put, our testers have smarts. And, we help other ways. Our 3040A system features a large alphanumeric LED display squarely in front of the operator's nose to eliminate back-and-forth neck fatigue, "CRT-squint" and resulting misprobes.

And there's more, like automatic thresholds by pin. Loop breaking routines. Special diagnostics for wired-or and bus structures. Time savers. *Cost* savers.

We've minimized programming requirements too. Simply load the IC library and describe IC locations and pin connections with the intelligent 3041A programming station. It's complete with CRT, keyboard line printer and dual floppy disks.

Smart as our Autotrack is, you can make it even smarter through priority tables that further reduce diagnostic time.

Yes, with *your* help, our bright logic testers can be brilliant. CALL (415) 965-0350 COLLECT for details. For a complete technical package, write on your company letterhead to Don Harter, Fluke Trendar Corp., 630 Clyde Ave. Mountain View, CA 94043. Europe: Fluke (Nederland) B.V., P.O. Box 5053, Tilburg, The Netherlands. Phone: (013) 673973. Telex: 52237.

FLUKE®

For literature, circle 29 on Inquiry Card.
For a demonstration, circle 30 on Inquiry Card.

Power-Up Feature Increases Add-On Memory Capabilities

An automatic power-up feature for use on its 370/STOR 135 add-on memories for IBM System/370 model 135 computer systems has been announced by Cambridge Memories, Inc, 12 Crosby Dr, Bedford, MA 01730. This feature permits users of 3135 processors to perform online initial microprogram loading (IMPL) of the mainframe system without the need to switch the memory offline, and is included at no cost on all STOR/135 memory systems. When combined with the manufacturer's online automatic diagnostic testing of the mainframe in both real and virtual memory modes, the feature is said to save users up to 25 minutes of equipment testing and program loading time at the start of each day's processing work.

Special circuitry detects and corrects all single-bit errors automatically, and detects all others, assuring virtually error-free operation. The add-on memory is available in size increments duplicating most IBM increments, and can be installed or upgraded at a user site in just several hours, with minimal processor change.

Two switches provide extensive back-up to memory operations. A reconfiguration switch enables failed add-on memory sectors to be removed from operation; an offline switch removes IBM resident memory from operation. In each case, the remaining memory continues to operate at peak performance.

Modular design enables users to install any memory size in either 64k- or 128k-byte sizes. Expansion of the system at the user site is made possible by the use of plug-in memory cards. All error checking, including the automatic power-up feature, diagnostic circuitry, power supplies, and maintenance panels are incorporated in each system.

Circle 152 on Inquiry Card

Turnkey Computer System Designed for Accountants

Version 5B of GIS-ABLE, a turnkey minicomputer financial control system for accountants and corporate financial officers, has been released by General Information Systems, Inc, 2024 N Broadway, Santa Ana, CA 92706. It features a complete hardware and software general ledger package designed for use on PDP-11 series minicomputers and is expandable to 64 CRT terminals. Operation can be for single jobs or in timesharing mode.

Program flexibility permits completely individualized reports derived from any chart of accounts. Reports can be generated in dollars as well as non-monetary readouts such as product units. Payroll recording and analysis can be performed separately or as an integral part of ledger posting.

Communication with the system is done through a special accounting language which permits an accountant to take full advantage of the capabilities of the computer without having to learn much about computer technology.

The system can perform mathematical calculations automatically on account balances in its memory. This allows the computer to calculate such data as allocations, accruals, ratios, percent changes, depreciation, or distribution of costs. It also offers features such as year-end processing to close out accounts, computation of retained earnings for inclusion in the balance sheet, and year-to-date and month-to-month comparisons. Current figures can automatically be moved to historical files for use in comparisons the following year.

Circle 153 on Inquiry Card

Word Processing Systems Meet Mid-Range Needs

A series of expandable, multiterminal word processing systems introduced by Digital Equipment Corp's Word Processing Computer Systems group, Nashua, NH 03060 are based on the company's PDP-8 minicomputers. The WS200 series of multistation systems provides mid-range offerings between the company's WS78 single-user, standalone systems and larger PDP-11-based, shared logic configurations. All capabilities of the company's other word processing systems are incorporated, including interterminal communications, automatic document send/receive to and from unattended WS202 systems, prestored "boilerplate" libraries, prestored command sequences, and multiple column printing.

Basic system of the series is the WS202 which includes two text editing terminals, printer, word processing computer, four flexible diskettes in a 4-ft high cabinet, and communications software. Addition of higher capacity, removable-cartridge disc units expands this system to handle as many as nine full-time word processing terminals, three printers, and up to 8000 pages of document storage.

Circle 154 on Inquiry Card

Word Processing Systems Upgradeable Through Software Modifications

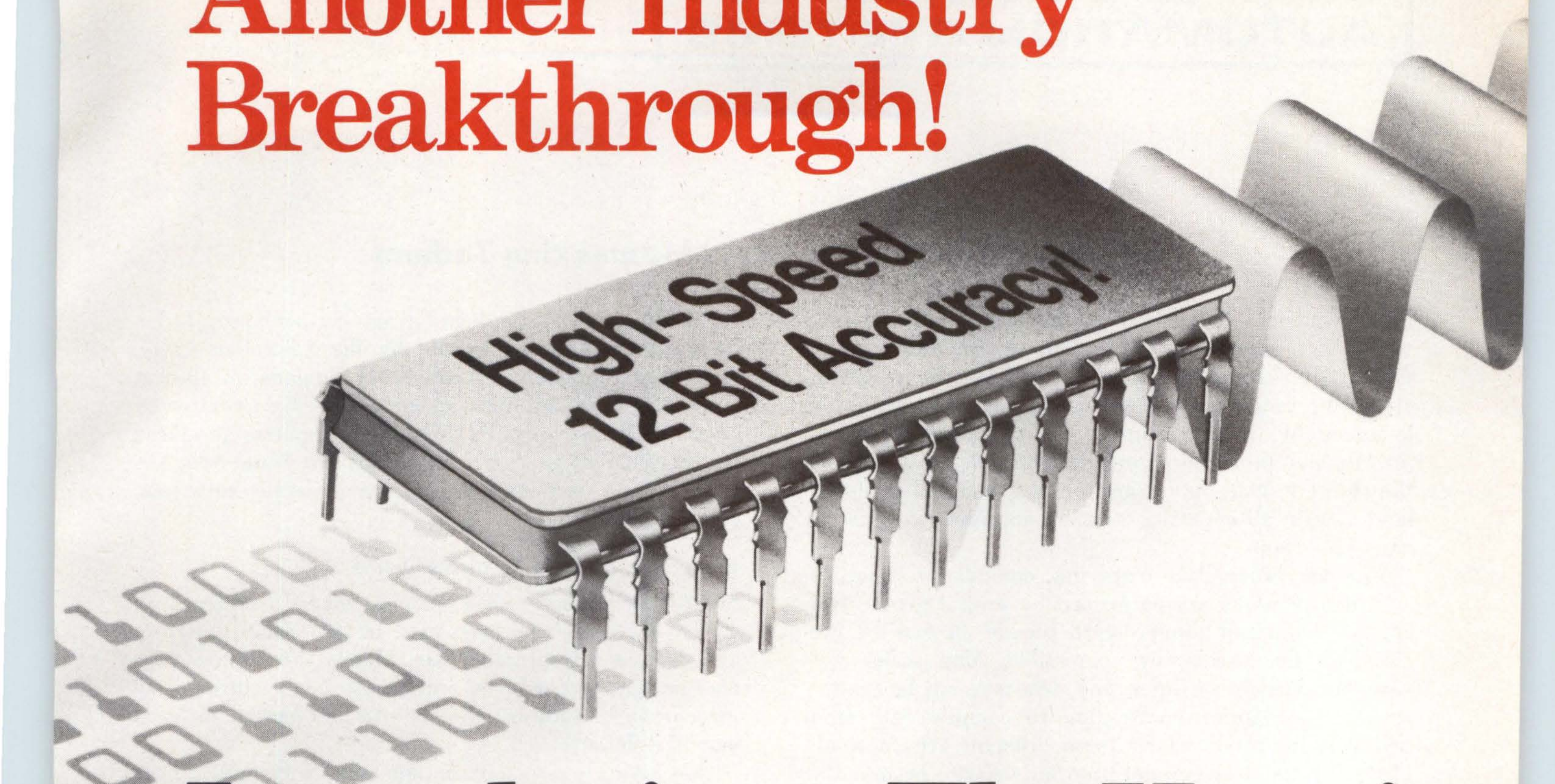
System I, a software-based word processing system, offers application flexibility as well as hardware-based performance at low prices. NBI, Inc, 5595 E Arapahoe Ave, Boulder, CO 80303 designed the system specifically to provide an economical means of upgrading to the automatic production of high volume correspondence as well as document editing and production.

Hardware elements include a typewriter keyboard with special function keys, CRT video display screen, 30-char/s daisywheel printer, and 250k-char floppy disc unit. Applications are updated by simply entering software changes on the standard diskette; this ability eliminates the need for added hardware, or system replacement.

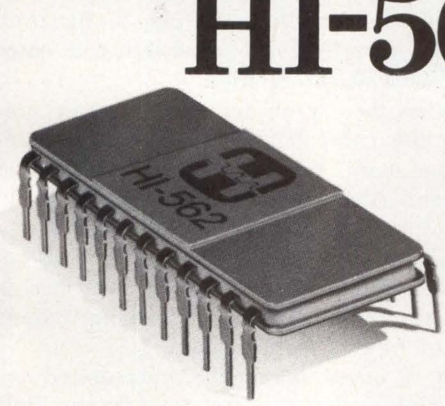
The system is organized by page-length (4000-char) documents. Text editing and revision are performed by the operator through the video display screen. System capabilities allow one document to be printed out concurrent with the entry of another. Other features include automatic centering, decimal tabulation, stop/switch codes for repetitive letters, and ability to type directly to the printer. □

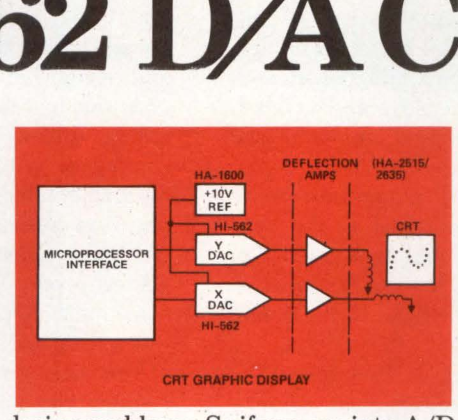
Circle 155 on Inquiry Card

Another Industry Breakthrough!

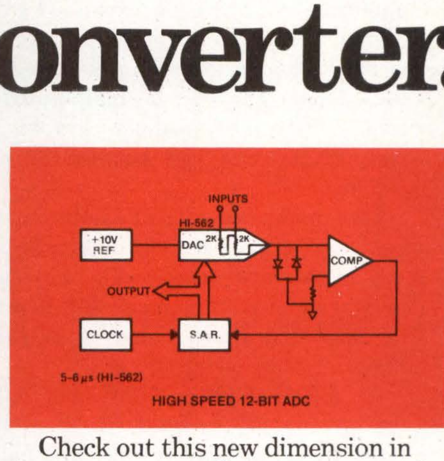


Introducing...The Harris HI-562 D/A Converter.





CRT GRAPHIC DISPLAY



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Minicomputer Control Eases Mapmaking Tedium

Most countries—both those that have already made good use of their natural wealth and those that must develop potential resources—are placing more and more emphasis on the preparation of precision maps that define the locations of those resources. In addition, population growth and rapid corporate development have strained the ability to plan the integration of urban and industrial land uses in all countries, making accurate maps all the more important.

However, when data gathering, compilation, analysis, and map planning are performed by several groups concurrently, the end results—even though all may be precise—are not necessarily compatible. Map scales may vary, standards may differ, and data may not be centralized. Any organization needing to compile data from several maps produced by these different groups would likely find the drafting and proofing tasks to be immense in scope.

Facilities for photogrammetric and survey calculations and for automated drafting have been available for some time. Also, over the past few years, computer applications have been expanded to include most phases of map compilation, and aerial photographs can be interpreted and coded directly into digital form. Resultant digital data files can be maintained and updated at any time, can be used to derive graphic displays and printed map sheets, and can be reorganized and analyzed directly.

One computer-controlled automated mapping system now in use performs map preparation equal to the output of ten draftsmen using conventional methods. Not only are topographic maps that formerly required months of manual drafting prepared in a fraction of the time, they are more accurate.

In the Australian Army installation at Bendigo, Victoria, about 85 miles north of Melbourne, data on features in aerial photographs are fed into the system via digitizer-equipped stereoplotters. These data are edited and verified automatically, and hardcopy checkprints are produced. After data on all map overlays are fed in, photographic separations are prepared for printing complete maps.

Applications include topographic map sheet production at all required scales from local to national base mapping, air navigation charts for both civilian and military purposes, and integration of base topographic reference data with specific map uses. Data also can be integrated from existing, older maps or such maps can be either updated or converted to different scales. For instance, known height contours from existing maps can be added automatically to the data from aerial photographs by use of an optical line follower.

An Ottawa, Ontario based firm—Systemhouse, Ltd—designed the Automap system for the Australian Army, as well as a number of Automap II versions installed at Canadian locations. Each system is based on control by several HP2100 or HP21MX minicomputers produced by Hewlett-Packard, 1501 Page Mill Rd, Palo Alto, CA 94304. Each computer controls a separate subsystem processing function.

Basic System Solves Problems Online

Several techniques—some manual, others automated in varied degrees—have been used in the past to interpret and capture cartographic data. Manual procedures were always long and tedious, and—most importantly—often inaccurate. In addition, they had to be repeated for each map of different scale.

One option was to obtain equivalent incremental tracing data by encoding X, Y, and Z motions of a plotter in digital formats. Such data were stored on punched cards or magnetic tape for offline processing by a computer to determine exact locations of control points. However, even this involved problems because the operator had difficulty in correcting, editing, or updating the data. There also were long delays between data entry and receipt of corrected information.

Automap remedies these problems and others by providing direct, online computer processing. Five minicomputers are time-shared by seven stereo plotters and digitizing tables and other system components. The output is a series of precision overlays—each containing specific groups of cartographic data—which printed together produce complete maps. Subsystem interface is accomplished via transfer of data between magnetic tape units that are part of each subsystem.

The basic system offers interactive, time-shared encoding, editing, and compilation of data for multiple users, seven on the input subsystem alone. Data are captured from aerial photographs, old maps, and field documents. A library of software routines enables map sheet compilation, high speed verification plotting, and final production of high quality films with the full range of cartographic symbols for printing multicolor maps.

Five separate subsystems are included (Fig 1): *input* for data entry and editing, *general-purpose* for batch or offline processing and hardware backup for the other subsystems, *verification* for high speed plotting of proofs, *automatic digitizer* for rapid digitizing of information from previously prepared maps, and *output* for precision plotting of final overlays and for scribing. All subsystems have dedicated computers that control and automate operation. Data transfer between subsystems is conducted via magnetic tape units.

(*Continued on p 61*)

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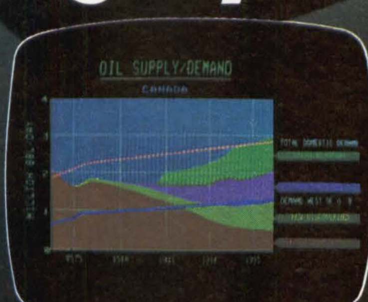

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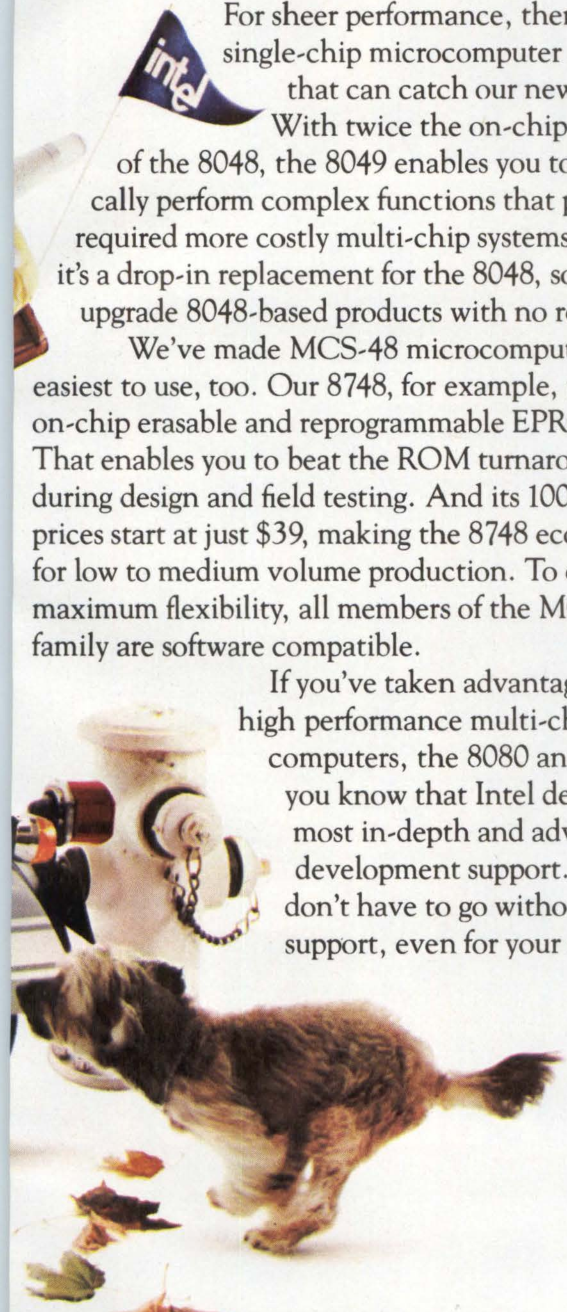

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8048*	1K Bytes ROM	64 Bytes	27	96	40 Pin
8748*	1K Bytes EPROM	64 Bytes	27	96	40 Pin
8035*	(External)	64 Bytes	27	96	40 Pin
8049*	2K Bytes ROM	128 Bytes	27	96	40 Pin
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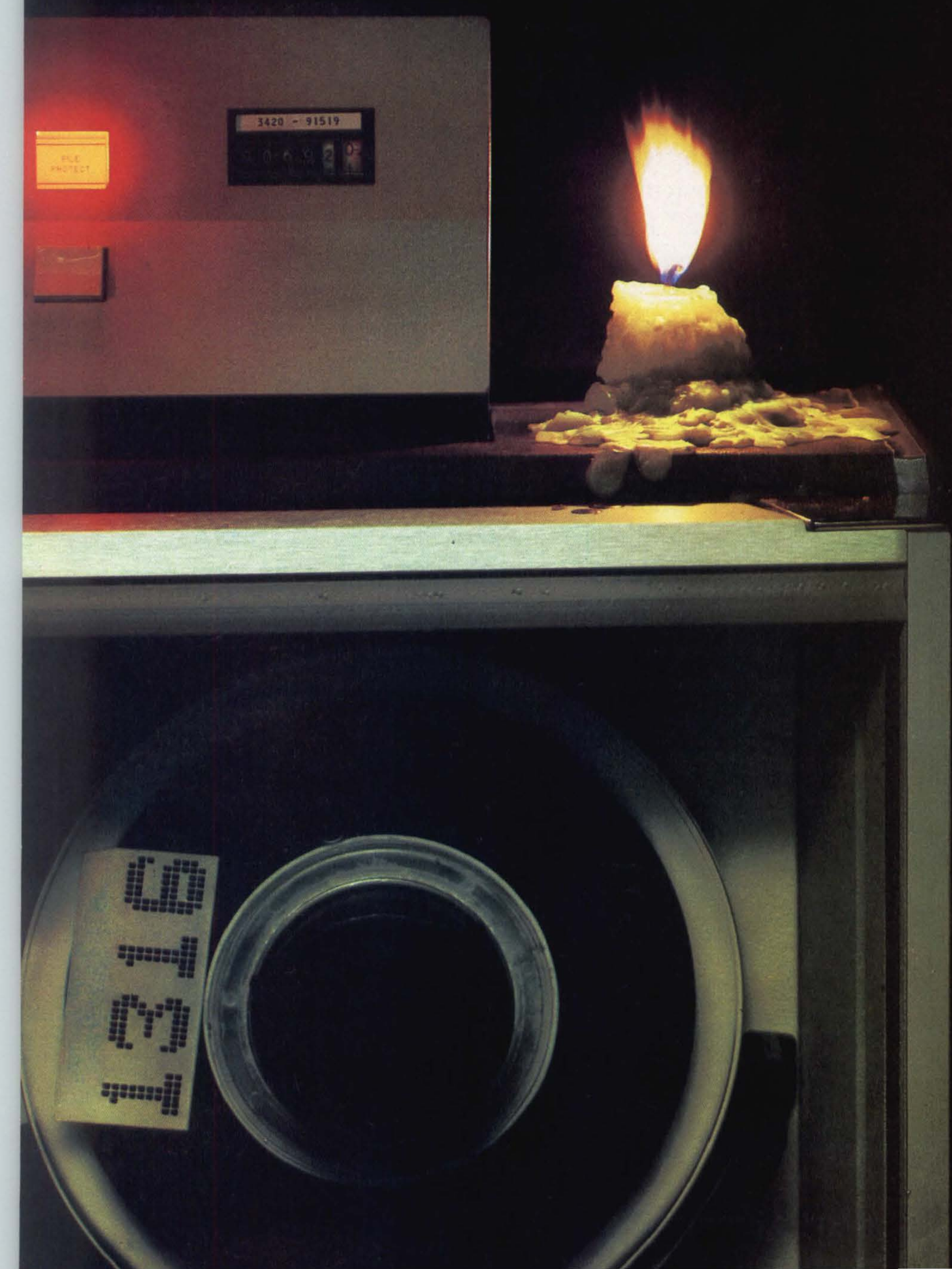

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CIRCLE 35 ON INQUIRY CARD

Input Subsystem

Actually the system management control center, this subsystem provides for entry and storage of data on topographic features onto magnetic disc files; the recall, editing, and updating of those data; and creation of appropriate control files for the other subsystems. Four stereoplotters and three table digitizers operate concurrently under control of an HP2100 minicomputer and RTE-II real-time executive operating software (Fig 2).

The stereo plotters are used for encoding data from aerial photographs; table digitizers edit, update, and input data from manuscripts or older maps. Each has an associated CRT terminal that prompts the operator or provides commands. The computer contains 32k words of internal memory and is backed up by five 5M-byte HP79000 disc drives (Fig 3), magnetic tape unit, system CRT console, and paper tape reader.

Special viewers on each stereo plotter enable an operator to examine aerial photographs in three dimensions. Controls permit movement in both X and Y directions to change the terrain being viewed. Depth is varied by a focus control.

Table digitizers are comparable to drafting tables and operate like the stereoplotters except that they have only X and Y outputs, without depth control. First coordinates are oriented to known ground positions, then digitized coordinates are converted directly into map grid locations. All positional data are therefore reported to the operator in true ground coordinates, regardless of the scale and orientation of the original map or photo.

Stereoplotter and table digitizer operators control input of data in a conversational mode with simple English-language commands entered through the CRT display terminals. In response to each command that specifies a feature, the subsystem displays the appropriate interpretation and asks the operator to confirm the choice before coordinates are entered.

An extremely flexible set of data-capture parameters for continuous digitizing allows up to 100 points/s to be captured and stored, or the subsystem can be ordered to retain only points which are more than a predetermined distance apart. Normally, cursor travel speed—a blend of time and distance—determines coordinate storage. Both sample frequency and minimum point separation can be set or altered by the operator at any time.

General-Purpose Subsystem

Encoded data on features from each aerial photograph are transferred from the disc file to the input subsystem magnetic tape unit, and then are forwarded to a magnetic tape unit in the general-purpose subsystem. In the latter subsystem the photographic data are combined with previously proven topographic data.

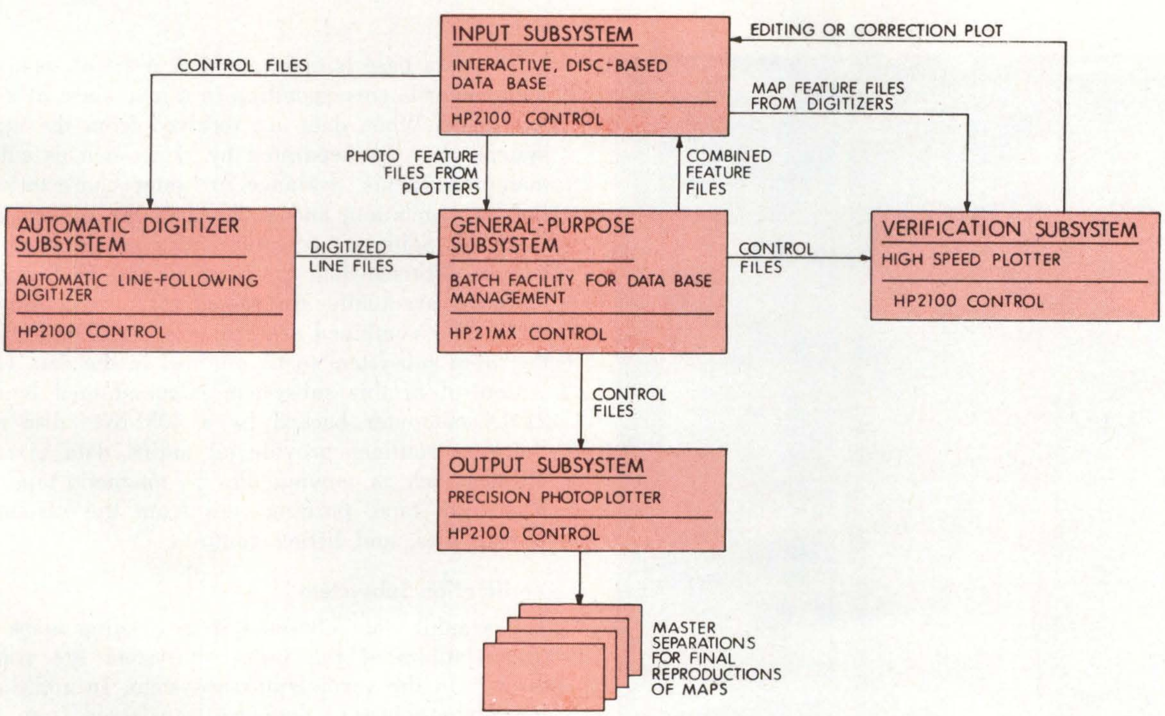

Fig 1 Overall block diagram of Automap system showing basic flow of data. Each subsystem includes magnetic tape unit which accepts data from or transfers data to other subsystems. Usual flow of data is from input to general-purpose to output subsystems; however, in some situations, flow could be directly from input subsystem to output subsystem

(*Continued on p 62*)

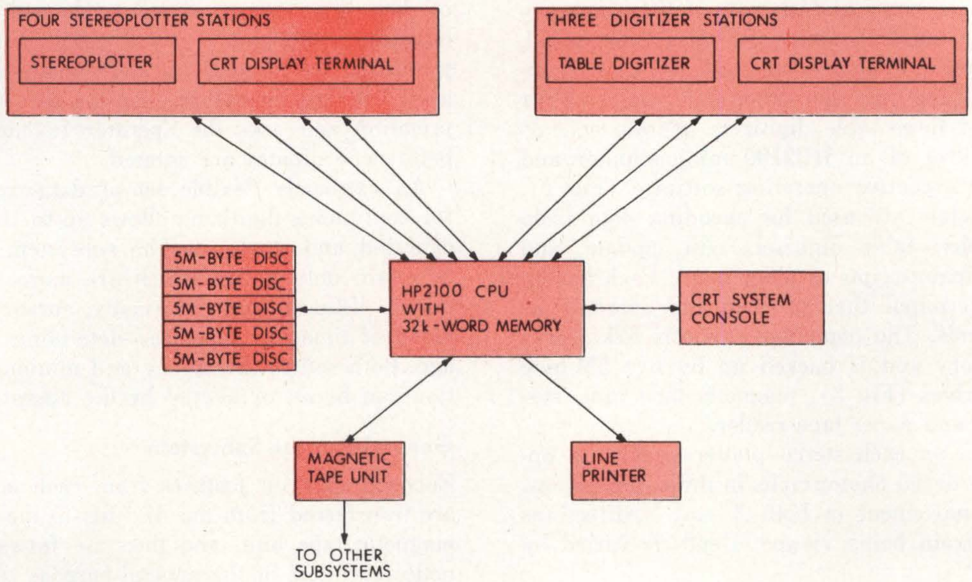

Fig 2 Detailed block diagram of input subsystem. Mapping features on aerial photographs are entered through stereoplotters. Table digitizers enter data from existing maps. Station CRTs can provide instructions to operators or can question validity of any data that control computer does not accept. Data base is maintained on 25M bytes of disc memory

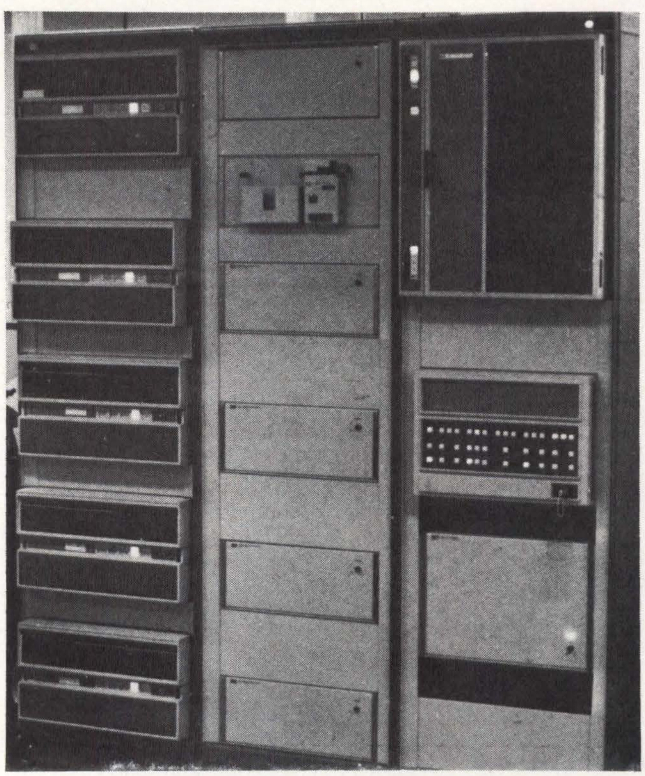

Fig 3 Portion of input subsystem hardware shown in Fig 2. HP2100 with 32k memory controls subsystem. Data base is maintained in five 5M-byte HP79000 disc drives

The data base is maintained as a set of separate files, with each file corresponding to a map sheet at a production scale. When data are received from the input subsystem, they are separated by type, such as cultural or man-made items, drainage or water characteristics, relief, or vegetation, and assigned to the proper files.

At this point, some features may not be complete, but as new digitized data are received and filed, portions of all items eventually are joined to form continuous entities. The combined feature files are then returned to the input subsystem to be retained in the data base.

Control of this subsystem is maintained by an HP-21MX computer backed by a 30M-byte disc memory. Software routines provide all online data management utilities such as copying files on magnetic tape, loading files from tape, purging files from the system, transferring files, and listing routines.

Verification Subsystem

Topographic data obtained from existing maps at digitizer stations of the input subsystem are transferred directly to the verification subsystem. In addition, combined photo feature data are transferred from the general-purpose subsystem after processing there.

At the verification subsystem a Gerber high speed plotter, controlled by an HP2100 computer, provides a hardcopy checkprint of the map data. Symbols and text are drawn under software control to display every feature, and are directly related to the encoding performed

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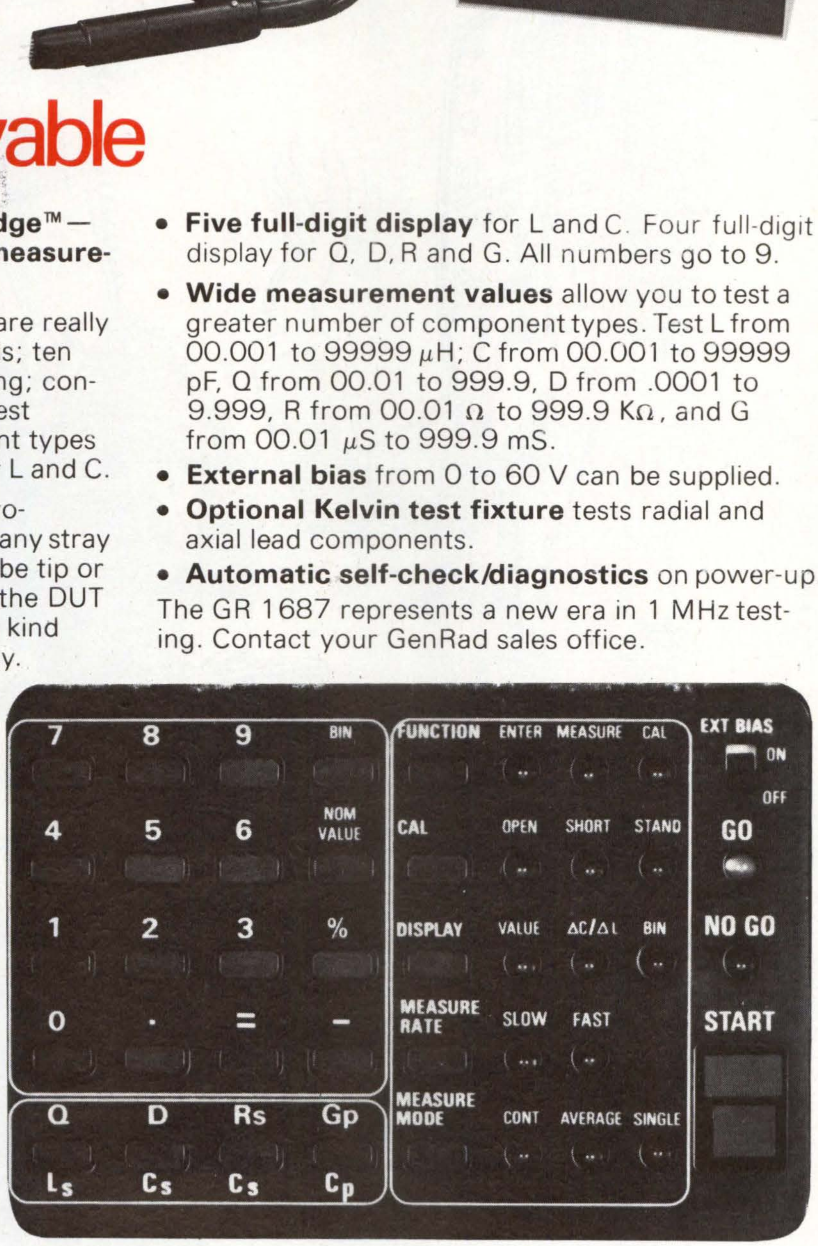

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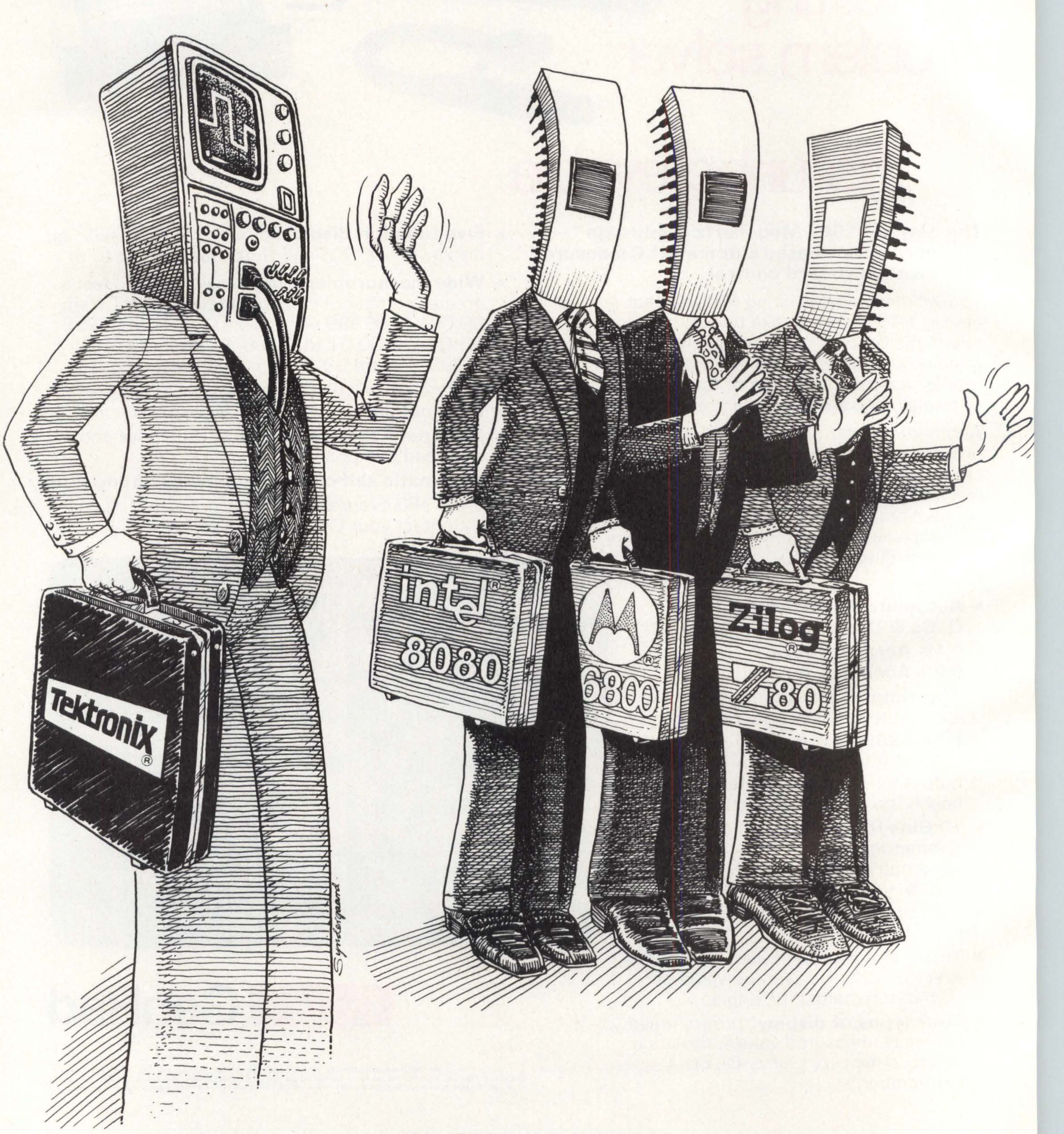

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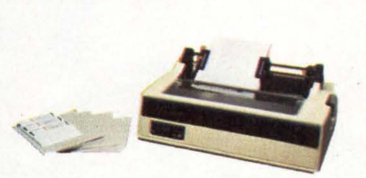

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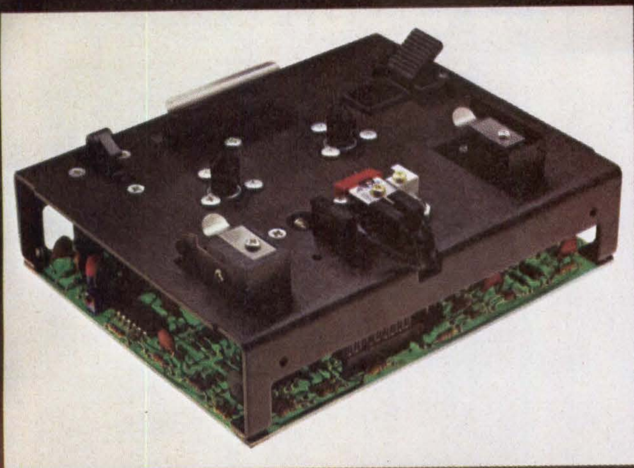

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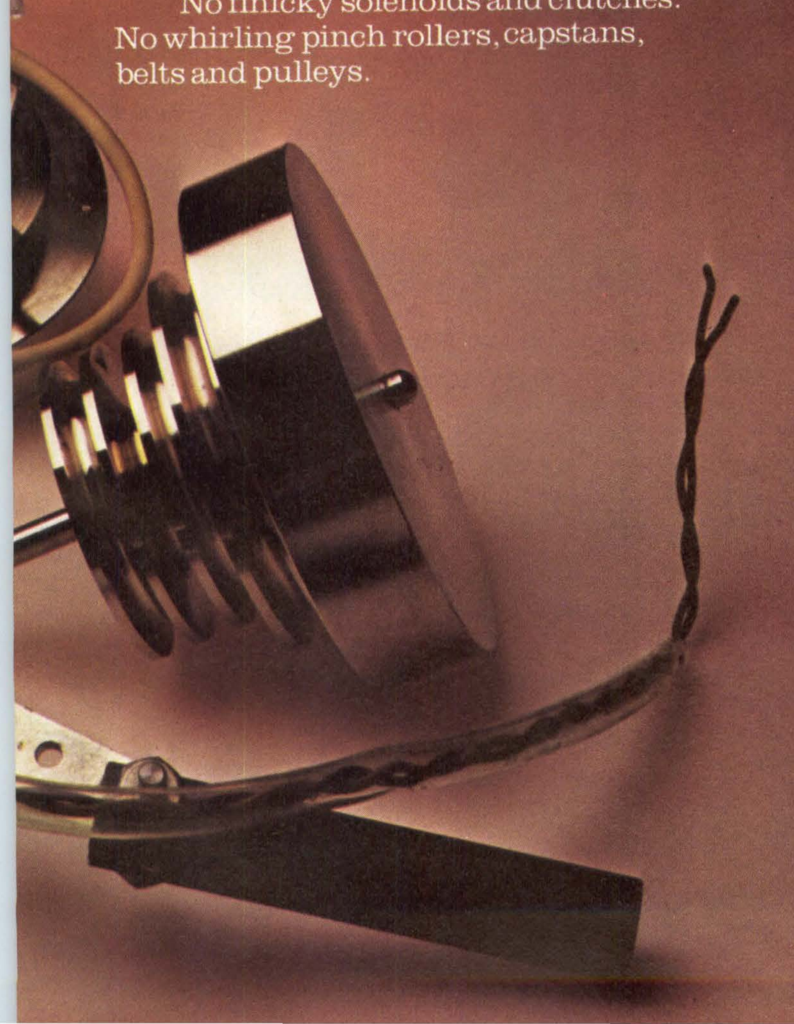
CIRCLE 38 ON INQUIRY CARD



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CIRCLE 39 ON INQUIRY CARD

at the input subsystem or on the data scored in the data base.

Line quality and registration of the checkprint are not precision but are adequate for error detection. Different classes of features can be superimposed to check relationships. Any errors on these prints are corrected through a digitizer and the new information supplied directly to the data bank.

Once features have been fully verified, corresponding data files are copied onto magnetic tape for temporary storage. Tape files are grouped until all data sets related to a specific map are complete. The number of such data sets will vary according to the scale and complexity of the required map sheet.

Automatic Digitizer Subsystem

In this station, an optical line follower or automatic digitizer is used to capture contour information from existing correct maps. The map is placed on the digitizer table, an optical viewer is set into precise position, and the line follower automatically moves along the contours printed on the map under control of an HP2100 computer. Points on X and Y coordinates are sampled at set frequencies with very fine resolution.

Discrete start points are determined for each contour on a map at one of the input subsystem table digitizers. Then the map is placed in the automatic digitizer and the map is aligned. The line follower automatically moves to the first start point, follows that contour, moves to the next contour, follows that one, and so forth until all contours have been digitized. Output of the line follower is combined on magnetic tape with manually-entered data and then processed to the input subsystem for integration in the data base.

Output Subsystem

Once verification of all map sheets has been completed—with all editing and corrections included—the resultant files are ready for final plotting. This is accomplished with an HP2100-controlled Gerber precision photoplotter that operates offline from information stored on magnetic tapes.

This plotter does not produce complete maps. Instead, it produces four overlays containing opaque map features on clear mylar or other stable film base material. Ordinarily the features on each overlay are produced photographically on the base film, but the plotter can be equipped with scribing tools to cut other types of base material. Overlays are then used to produce color separation negatives for lithographic printing of complete maps.

Sophistication Added for Future Systems

Automap II, presently used or soon to be used by several agencies of the Canadian Federal Government, enables a greater range of interactive encoding, editing, and analysis capabilities. Specifically, it provides area (polygon) coding and linkage, text processing, and user land code editing as well as data file structures and conversions among the wide range of formats now used for national geographic data files.

One system will be used by the Forest Management Institute primarily for coding and analysis of wooded areas over a wide range of map scales. The Lands Directorate, a part of Environment Canada, will use its system for entry and editing of land use and resource coding to produce maps for the Canadian Geo-Information System. Other applications include property registration and urban planning, utility mapping, and inventory management.

A major feature is the online graphic display of stored coordinate data using large screen CRT units associated with data entry stations to display and identify data records as they are digitized and to permit interactive editing and manipulation of these records. In addition to the existing commands available to the operators for encoding, recalling, and manipulating coordinate data, this development provides commands specific to the interactive graphic reviewing of the data and its modification. For example, commands permit the graphic enlargement of selected areas by windowing and by zooming, the identification and selection of displayed map features by highlighting, and the selective display of map features by individual or group identification. Other commands permit the immediate computation of perimeters, map feature lengths, and areas of closed map features.

Facilities for text processing permit the processing of both label and feature classification texts. Handling of label text permits the placement and orientation of character strings with reference to the map documents, the coding of desired text size and print font, and the editing and maintenance of the resultant textual records. Classification text handling additionally provides for automatic checks of the classification codes.

A macro facility enables the predefinition, storage, and simple execution of combined standard command sequences as a single command. Each user creates a dedicated command library or, alternatively, adds macros to the system library.

Network mode of digitizing is specifically implemented for area digitizing. Network facilities ensure exact intersections of area boundaries using common points of line intersections or nodes. Facilities automatically complete those line junctions which are within user-selected tolerances, while warning of those situations where connections are outside of tolerances or cannot be carried out.

This system enables flexible and rapid editing of digitized data without the need for hardcopy proof plotting, permits the placement and editing of labels and other textual information in a graphic mode, and otherwise provides the mapmaker with tools necessary for map layout and final composition beyond those required simply for automation of the drafting and production of topographic maps. In addition, it emphasizes data management with a view to subsequent data analysis, manipulation, and integration with appropriate data from other sources.

A compatible system developed by Systemhouse, called Autochart, includes specific user procedures and techniques for encoding and compiling nautical charts and maps for marine applications. It is intended to interface with and enhance current charting procedures for coastal and ocean navigation and marine development.

Supermarket Terminal Network Processes Bank Withdrawals and Deposits

A minicomputer with 80k bytes of memory performs file and communications processing for a network of terminals that permit supermarket customers to cash checks and make savings account deposits and withdrawals. This electronic fund transfer (EFT) service is available to depositors of six different savings and loan associations in three Florida counties surrounding Tampa and St Petersburg. Terminals are located in 26 chain supermarkets.

A depositor accesses the system by inserting a plastic card containing magnetically encoded information. Then he or she must enter a secret identification code through the terminal's keyboard before the system will accept or verify the desired transaction.

All such transactions are electronically transmitted over 1200-baud asynchronous phone lines to a shared data processing center that maintains master files for all depositors. The EFT terminal transactions are identical in form to savings and loan transactions. Withdrawals are immediately deducted from savings balances, deposits are credited subject to collection, and checks are cashed against savings account balances until the checks clear.

Secret personal identification number, account status, card expiration date, listing of valid transactions and allowable limits, and a 7-day total of allowable transactions are maintained on a 92M-byte disc. An online CRT provides file updating of information after telephone inputs are received from the banking associations. Terminal transactions are processed by the minicomputer on a time-sharing basis before being relayed to the data processing center.

Hardcopy records are still maintained. Each savings and loan association daily receives a statement of each of its customers' accounts and a complete listing of all transactions, each supermarket manager receives a complete report of every transaction (for balancing cash accounting) and a weekly summary (to monitor store patterns), and each depositor receives a record of supermarket terminal transactions.

Florida S & L Development Corp of Orlando, a firm owned by 82 of the state's savings and loan associations, developed the cooperative fund transfer system. Software was provided by Transaction Data Systems and network design was accomplished by Systems Technology, both Orlando-based companies. The minicomputer, a Nova® 3, and a Dasher™ printer were supplied by Data General Corp, Rt 9, Westboro, MA 01581. Other system components include 1600-bit/in magnetic tape subsystem, 300-line/min printer, and DCU/50 data channel interface. A second Nova 3 minicomputer, to be installed within a few months, will extend the network capacity to 500 terminals shared by the two computers.

Circle 161 on Inquiry Card

Rare bird.

An editing CRT that's ideal for transaction processing.

Lower software costs. Easier programming.

System builders say our Model 1200 Editing Terminal is ideal for transaction processing. We agree.

The Model 1200 makes programming easier because it tells the programmer (and the host computer) the status at the terminal. Communications strap setting, printer errors, operator mode key setting, and more.

The Model 1200 also cuts down on host computer loading by automatically setting modified data "tags," whenever a field is updated, so the host computer can request only modified fields, and skip thousands of needless compare operations.

To further lighten the load on the host computer, the Model 1200 has programmable send keys that let the program regulate the amount of data returned to the computer as terminal loading varies.

More productive operators.

Thanks to a 9 x 12 character matrix, the Model 1200 has crisp, clear, strikingly sharp characters. So operators see their work better and make fewer mistakes. Data entry is incredibly accurate due to field attributes like low intensity, numeric only, blink, and inverse video.

Editing is fast and easy, too. Single keystrokes insert and delete characters and lines.

All our standard goodies. Only $1383.*

A big, 12-inch screen, 128-character ASCII set, upper and lower case, 15 cps Typamatic repeat on all keys, and a 24-line display are standard. So is our exclusive No Hassle toll-free 800 number for service. One call gets you service. Where you need it. When you need it. World-wide.

So go ahead. Get a CRT terminal that's specifically designed for transaction processing. Perkin-Elmer's Model 1200 Editing Terminal.

For more information, write Perkin-Elmer Data Systems Sales and Service Division, 106 Apple Street, Tinton Falls, New Jersey 07724 or telephone toll-free 1-800-631-2154.

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*Quantity 75.

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DC&AS BRIEFS

Microprocessors Monitor and Calculate Gas Flow and Line Conditions

An advanced gas flow monitoring device functions in tandem with a Turbo-Meter to convert meter output at line conditions into volume at base conditions. It uses both data from the meter and pressure and temperature sensors. Microprocessors instantly and continually calculate supercompressibility factor according to a program that accounts for all contributing variables such as line pressure and temperature.

The MPB gas flow computer, introduced by Rockwell International's Municipal & Utility Div, 400 N Lexington Ave, Pittsburgh, PA 15208, operates off standard line voltage. The operator dials in specific gravity, meter factor, and other constant parameters at front panel controls. All variables can be selected and displayed on a digital readout. Actual line conditions and calculated data can be monitored or parameters can be recalled at will.

Circle 162 on Inquiry Card

Feasibility of Computer-Controlled Laser Cutting Studied for Shoe Industry

A research study has been conducted for the past year at the Industrial Products Div of Hughes Aircraft Co, 6155 El Camino Real, Carlsbad, CA 92008 to determine if automated laser cutting systems such as those now built by that company for clothes and aircraft parts manufacturers can be developed for the shoe industry. Although that industry now uses laser cutters to fashion shoe patterns out of cardboard and plastic material, the suggested systems would mark, scan, and cut the actual leather hides.

Objective of the study is to determine if the design of an integrated computer-based system with capabilities for order entry, fabric defect detection, real-time marking and hide scanning, and automated cutting is both technically and economically feasible. Concepts of the leather system were disclosed in a paper presented by Walter T. Wilhelm, associate manager of Hughes' industrial automation systems, at the Automated Cutting Concepts Conference held in Atlanta, Ga in late October 1977.

Peculiarities of working with animal skins pose unique problems for an automated system. The hide must be optically scanned and several conditions such as the irregular boundaries of the skin, the shape and location of defects and flaws, the orientation of the fiber, and the variances in skin quality taken into consideration by the computer to determine how the shoe pattern could be laid out.

Techniques similar to those used in the AM-1 apparel graphics system appear to overcome these obstacles and be applicable to leather cutting. While the earlier system uses an interactive mode of operation to grade patterns and construct markers, the leather cutting system would use a laser beam to do the actual cutting, much as present systems do in cutting cloth. In each case, the beam from a carbon-dioxide laser is directed to the material to be cut by a series of mirrors mounted on a fast-moving X-Y positioning device controlled by the computer.

The laser's efficiency when cutting one layer at a time is particularly applicable in footwear manufacture. Since each skin is unique, cutting on this "one-high" basis is required. If the study shows the project to be feasible, the first leather cutting system could be operating by mid-1979.

Circle 163 on Inquiry Card

Dual Computer Systems Share Functions But Provide Backup

Dual 32-bit CPU, FORTRAN language industrial control (FLIC) systems are being installed in three refineries in the U.S. and Venezuela to gather data, monitor utility services, and control unit operations. Although loads are normally shared between CPUs, either CPU automatically assumes control of critical functions if the other unit fails.

According to Metromation, Inc, 1101 State Rd, Princeton, NJ 08540, the systems provide uninterrupted process control and monitoring in the event of component failure, load sharing to assure adequate CPU capacity for the continual performance of required tasks in real time, large computing power to handle current demand with the flexibility of being expanded to handle future requirements, and operator control of CPU status to permit online maintenance. Load sharing is based on splitting of functions rather than having a redundant CPU on standby. For example, the first CPU might handle real-time functions, the second, batch/interactive ones. The first might include scan, conversion, loop control, reports, displays, material balances, combustion monitoring, and utility balances. The second might handle control, optimization, production-related reports, lab data, utility balances, blend modeling, and program development and maintenance services.

In a typical system, a fixed head disc would be dedicated to each CPU; moving head discs and a multiplexer interface to process operator work stations would be tied to both CPUs. Switched controllers would allow either CPU to access a variety of peripheral devices such as line printers, card readers, magnetic tape drives, and floppy discs. □

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Pussycat. Perkin-Elmer's $795,* 100 cps CRT Page Printer.

Pussycat. That's what we call our new 100 cps thermal printer, The Model 650 CRT Page Printer.

Pussycat. People who make 30 cps printers will think it's an incredibly funny name. Until they realize our meek little Model 650 is half the price of their machines, three times faster, and a whole lot quieter and easier to maintain.

In quantity 75, the Model 650 is only $795 each. Which means you can buy a CRT and a Pussycat printer for what you're now paying for a printing terminal alone.

The Model 650 is fast. It prints an entire screen full of characters in 20 seconds. And, because it's the only printer in its class with a full-screen buffer, the Model 650 can free the CRT in 2 seconds or less. So the operator can go back to work while the printer is printing.

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And no need to worry about noise or maintenance. The Model 650 has only one moving part – the platen.

Check out The Pussycat from Perkin-Elmer. It's a great little printer at a very reasonable price.

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*Quantity 75.

PERKIN-ELMER
Data Systems

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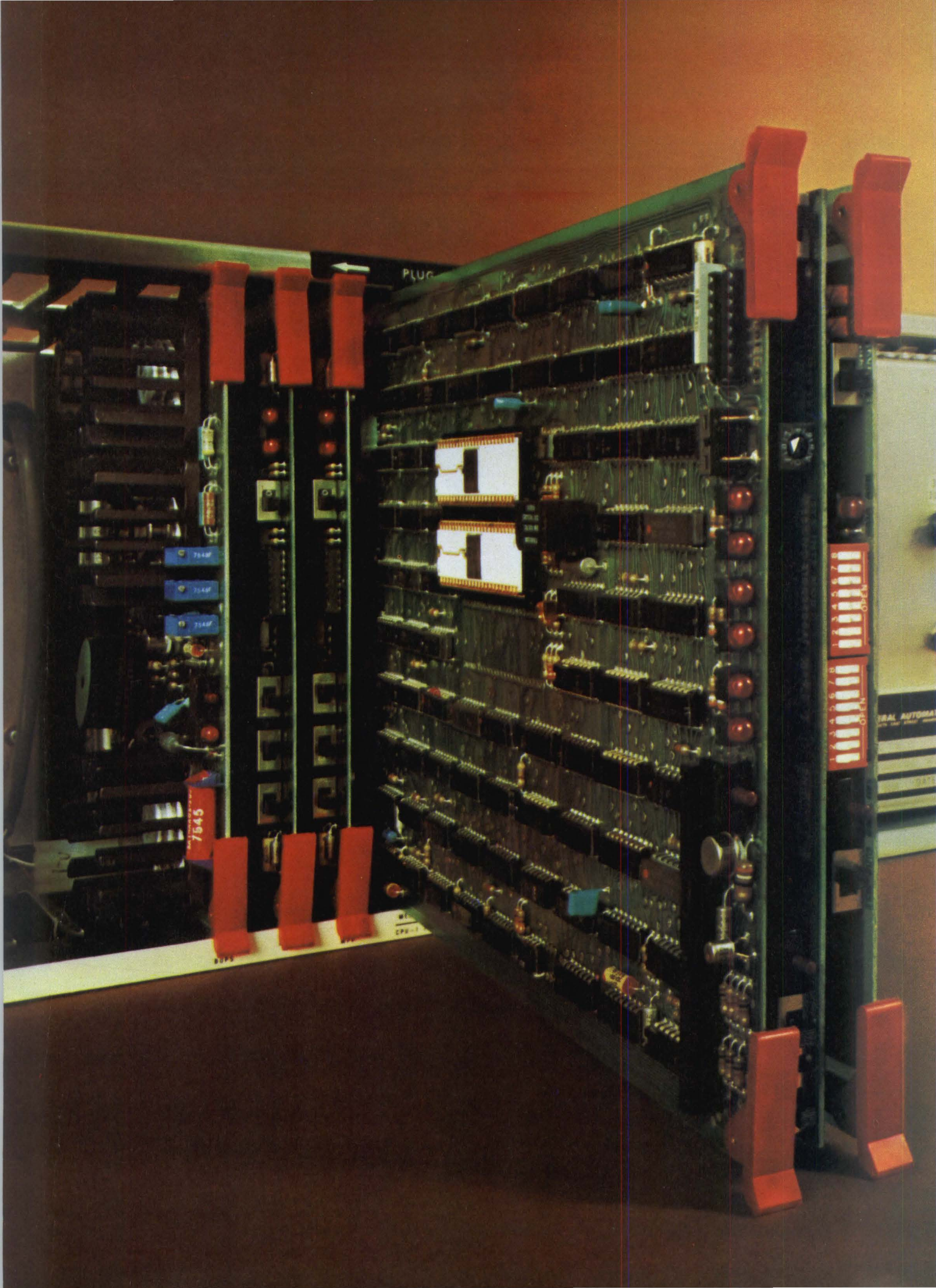
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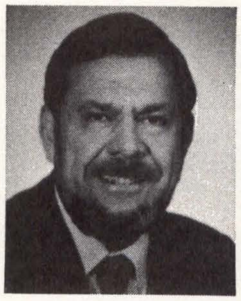
IECI '78

Sheraton Philadelphia Hotel
Philadelphia, Pennsylvania
March 20-22

Wellington W. Koepsel
General Chairman



Harry W. Mergler
Program Chairman

C. Lester Hogan
Keynote Speaker

Featuring eleven sessions and two evening panel discussions, IECI '78, the fourth annual conference and exhibit on Industrial Applications of Microprocessors, offers attendees the opportunity to obtain first-hand information on applications of microprocessor systems in worldwide industrial environments. The conference, sponsored by the IEEE Industrial Electronics and Control Instrumentation Group, will be led by general chairman, Wellington W. Koepsel of Kansas State University, and program chairman, Harry W. Mergler of Case Western Reserve University. The conference program will include such topics as data acquisition; signal processing; monitoring and industrial control applications; testing; energy, consumer, and motor control systems; and other special topics. There will be opportunities for discussions of each paper by conference attendees. The morning panel session will center around testing problems in bus oriented systems, with emphasis placed on the impact that these problems have on business. The two evening panel sessions will focus on I/O analog interfaces and new devices for industrial controls.

Highlighting IECI '78 will be the Tuesday awards luncheon and keynote address. In the Grand Ballroom East at 12 noon on Tuesday, March 21, Dr C. Lester Hogan, vice president of the board at Fairchild Camera and Instrument Corp, will deliver the keynote address. Also scheduled during the conference will be industrial microprocessor systems exhibits.

Advance registration fees, which must be received by March 3, are $65 (members), $75 (nonmembers), $20 (students), and $35 (speakers, authors, committee, and session chairman). Registration form and remittance should be sent to: IECI '78 Treasurer, W. Spencer Bloor, Leeds & Northrup Co, Sumneytown Pike, North Wales, PA 19454. At-conference registration will occur on Sunday (6-8 pm), Monday (8 am-6 pm), and Tuesday and Wednesday (8 am-2 pm). Fees at this time will be $75 (members), $85 (nonmembers), $20 (students), and $40 (speakers, authors, committee, and session chairmen). All registration fees include the conference proceedings and the Tuesday awards luncheon. The fee for one-day registration without luncheon will be $35; additional luncheon ticket price will be $15. Extra copies of the proceedings will be available for $15 during the conference; prices after the conference will be $20 (members) and $25 (nonmembers).

Details on the technical program that follows are limited to information available at press time.

Technical Program

Monday Morning

Session I 9-11 am Pennsylvania Ballroom (E)

Data Acquisition

Chairman: K. Schroeder, RCA Corp

"A Microprocessor Controlled Substation Alarm Logger," Dr M. C. Mulder, Bonneville Power Administration, and Dr P. P. Fasang, University of Portland

"An Absolute Position Encoder System," D. Elms, Duane Elms Associates, Inc

The HP 2649A is what you make it.

A controller. *It's a natural. Just program the built-in 8080 microprocessor to do your thing, and get it into your system. The HP 2649A has a variety of synchronous, asynchronous, serial and parallel interfaces (including HP-IB, our IEEE Interface Standard 488). This makes it easy to hook up with instruments and peripherals. In short, it's a complete controller system in a single package.*

A terminal. *Terrific! Great editing ability, a choice of keyboards, flexible data communications, and a variety of baud rates make it an excellent fit in an RJE situation. Preprogrammed firmware is available to get you off to a head start.*

A microcomputer. *Why not? The microprocessor gives you a lot of power. Then you can add ROM memory, interface with a disc, control peripherals, and access other systems via a modem. So the HP 2649A acts like a small computer, even if it doesn't look like one.*

A graphics display station. *Sure. You can put a window in your system and see exactly what's going on. Alphanumerics, auto-plot, and full graphics, including Area Shading, Pattern Definition and Rubber-band line, give you the whole picture.*

You can really make a lot with the HP 2649A.

You start with the basics — a CRT, power supply, backplane, I/O cards, MPU, and versatile, modular architecture.

You program it to do your specific job, and pick only the memory, keyboard, I/O, breadboard, and other modules you need. These include RAM (up to 32K bytes on one module), ROM, and PROM boards, which all simply slip into the chassis. (There are slots for your own boards as well.) You can also add 220K bytes of mass storage on dual plug-in cartridges.

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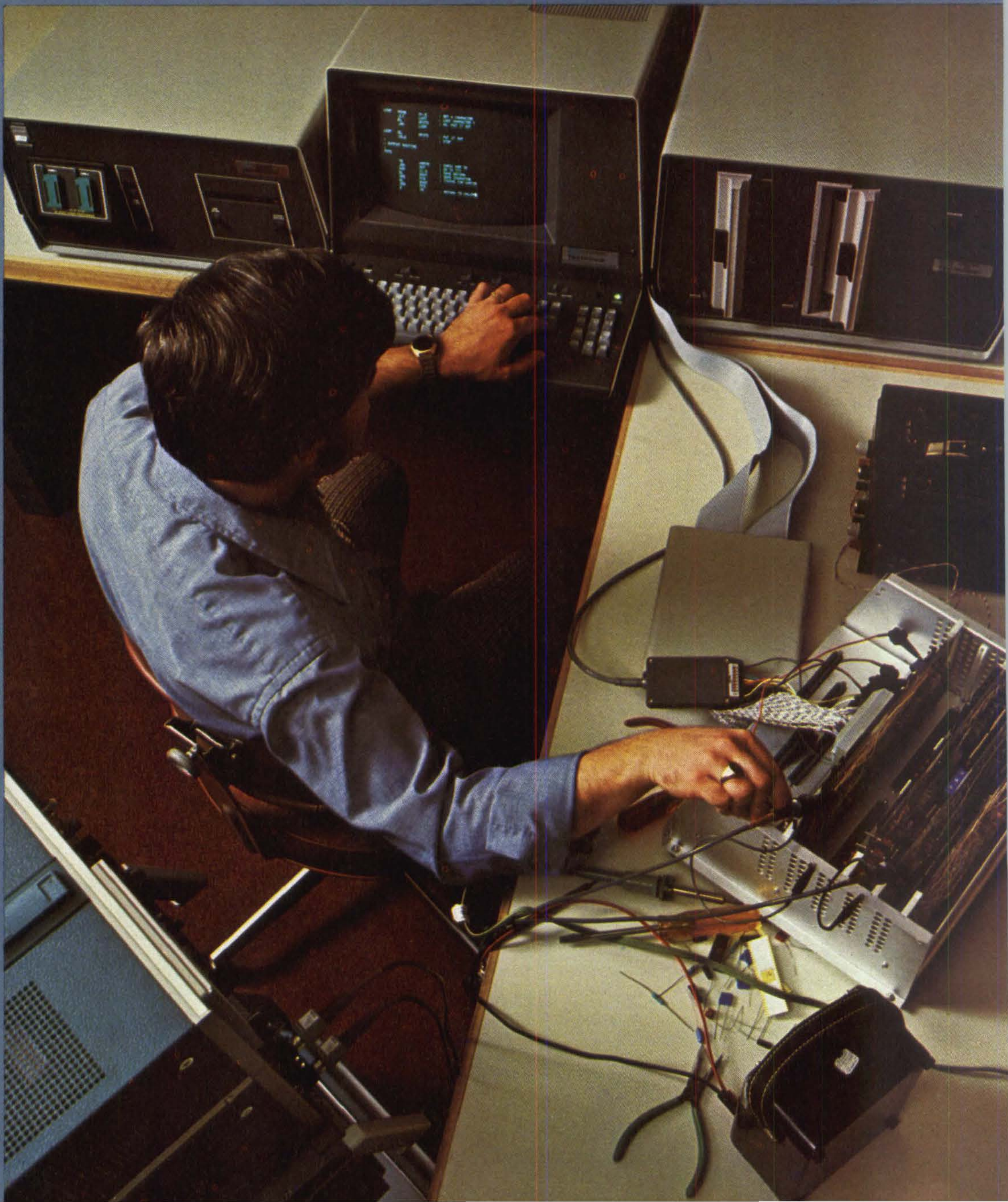

"Automatic Service Monitor for Telephone Switching Systems," P. D. G. Jennings, Mid-Continent Telephone Corp

"New Generation Components and Techniques for Microprocessor Analog Interfaces," R. L. Morrison, Burr-Brown Corp

Session II (Panel) 9-11 am Pennsylvania Ballroom (W)

Testing Bus Oriented Microprocessor Systems

Chairmen: M. D. Lippman and E. S. Donn, Fluke Trendar Corp

"Testing Bus Oriented Systems," E. S. Donn and M. D. Lippman, Fluke Trendar Corp

Monday Afternoon

Session III 2-4 pm Pennsylvania Ballroom (E)

Signal Processing

Chairman: J. Cook, University of Virginia

"A Simple Microcomputer for Biomedical Signal Processing," A. Caprihan, Universidade Federal do Rio de Janeiro, Brazil

"A Microprocessor Random Motion Equalizer for Vibration Testing," Dr A. G. Ratz, Vibration Instruments Co

"Driving Control Method of Automated Vehicle with Artificial Eye," T. Yatabe, T. Hirose, S. Tsugawa, and S. Matsumoto, Automobile Div, Mechanical Engineering Laboratory, Japan

"Microprocessor-Based Frequency Response Analyzer," P. J. Zsombor-Murray and L. J. Vroomen, McGill University, Canada; and V. R. Stefanovic, Concordia University, Canada

Session IV 2-4 pm Pennsylvania Ballroom (W)

Monitoring and Control Applications

Chairman: J. D. Irwin, Auburn University

"A Microcomputer-Based Supervisory System for a Mercury-Cathode Chlorine Plant," J. L. Hilburn and P. M. Julich, Electrical Engineering Department, Louisiana State University; and R. L. Mitchell, Microcomputer Systems Inc

"A Microprocessor-Based Demand Limit Control," R. F. Herrman

"Multi-Microprocessor Terminal for Energy Systems Monitoring," A. L. Bogado Fernandes, O. Appel, and M. Moszkowicz, Centro de Pesquisas de Energia Electrica (CEPEL), Rio de Janeiro, Brazil

"Design of a Microcomputer Controlling a Group of Parallel Tap Changing Transformers," P. Girard and R. Grondin, Electronics and Control Systems, Canada

Monday Evening

Panel Session I 7-9 pm Pennsylvania Ballroom

I/O Analog Interfaces

Moderator: R. L. Morrison, Burr-Brown Corp

Tuesday Morning

Session V 9-11 am Grand Ballroom (W)

Industrial Control Applications

Chairman: F. Harashima, Institute of Industrial Sciences, University of Tokyo, Japan

"MECA—A Modular Approach to Microprocessor-Based Industrial Controls," M. F. MacDonald, GTE Sylvania

"Microprocessor Data-Input-Control Unit for Mark Century Numerical Contouring Control," C. D. Ethridge and B. Seifert, University of California, Los Alamos Scientific Laboratory

"Design of a Psychrometric Computer," G. Gogates, S. Klein, C. Rupp, and R. P. Jefferis, Widener College

"A Microprocessor Approach to a Rod Coiling Wobble Control System," R. D. DeWitt, Reliance Electric Co

Tuesday Afternoon

Session VI 2-4 pm Grand Ballroom (E)

Testing

Chairman: J. Giachino, Ford Motor Company

"Microprocessor-Based Printed Circuit Board Tester," A. R. Marcantonio, RCA/David Sarnoff Research Center

"Automotive Wheel Alignment Measuring Instrument," A. K. Chang, J. E. Peterson and R. F. Quintana, FMC Corp

"A Microprocessor-Controlled Automatic Test and Diagnostic System for Use on Electronic Automotive Engine Control Systems," E. R. Pelta, FMC Corp; and K. S. Gold, Consulting Engineer

"The VTAC. A Dedicated Microprocessor for CRT Control," D. R. Lewis and G. Gollub, Standard Microsystems Corp

Session VII 2-4 pm Grand Ballroom (W)

Energy Systems

Chairman: C. W. Einolf, Westinghouse Research Center

"Microprocessor and Simulator Combination Improve Fossil Power Plant Training Program," T. P. Enright and D. A. Esakov, Combustion Engineering Inc

"Hierarchical Power System Protection Scheme for Distance Relaying and Fault Location Using Microprocessors," M. Tsunoda, K. Mochizuki, I. Sugiyama, K. Sato, and S. Narita, Department of Electrical Engineering, Waseda University, Japan

"A Microcomputer Applied Programmable Controller for Hydro Electric Power Generation," S. Ryusawa, S. Haratani, and T. Yanagisawa, Toshiba, Tokyo-Shibaura Electric Co Ltd, Japan

"Uninterruptible Power Supply for the Gentilly Nuclear Power Station," G. Govas, A. Kefalas, and A. Kiamos, Canadian General Electric; and V. R. Stefanovic, Concordia University, Canada

"Microprocessor Control of a Wind Turbine Generator," A. J. Gnecco, NASA, LERC

Tuesday Evening

Panel Session II 7-9 pm Pennsylvania Ballroom

New Devices for Industrial Controls

Moderator: Max Schindler, *Electronic Design*

Wednesday Morning

Session VIII 9-11 am Pennsylvania Ballroom (E)

Consumer Systems

Chairman: P. Russo, RCA Laboratories

"A Solar Heating System Simulated, Controlled, and Instrumented by a Microcomputer," S. C. Peek, GTE Sylvania

"Solid-State Sotware 'BASIC' in Automation," E. R. Fisher, Lawrence Livermore Laboratory

"Microprocessor Control for Microwave Ovens," T. Yoshioka, T. Matsumura, S. Watanabe, and Y. Tanji, Matsushita Industrial Equipment Co Ltd, Japan

"A Microcomputer Controlled Filmstrip Projector," J. D. Garland and J. V. Landau, The Singer Co, Corporate R & D Laboratory

Session IX 9-11 am Pennsylvania Ballroom (W)

Motor Control Systems I

Chairman: P. C. Sen, Queen's University, Canada

"Development of a Power Drive Controller using the TMS 9900 Microprocessor and the AN/UYK-30 Military Microcomputer," D. L. Chenoweth, Electrical Engineering, University of Louisville; and L. J. Smith and J. D. Johnson, Naval Ordnance Station

"Applications of the Microprocessors on Some Electrical Vari-

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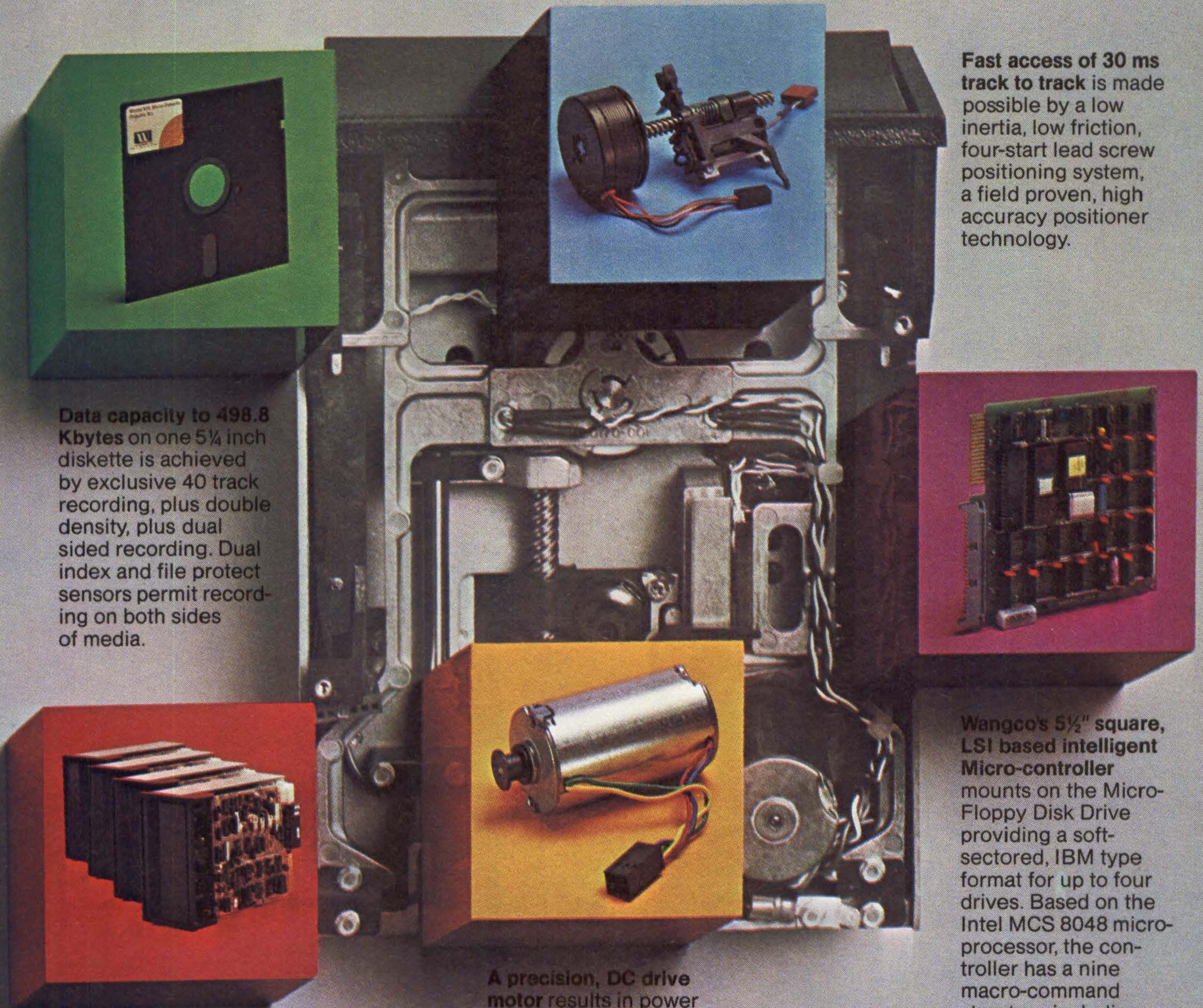

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Data capacity to 498.8 Kbytes on one 5¼ inch diskette is achieved by exclusive 40 track recording, plus double density, plus dual sided recording. Dual index and file protect sensors permit recording on both sides of media.

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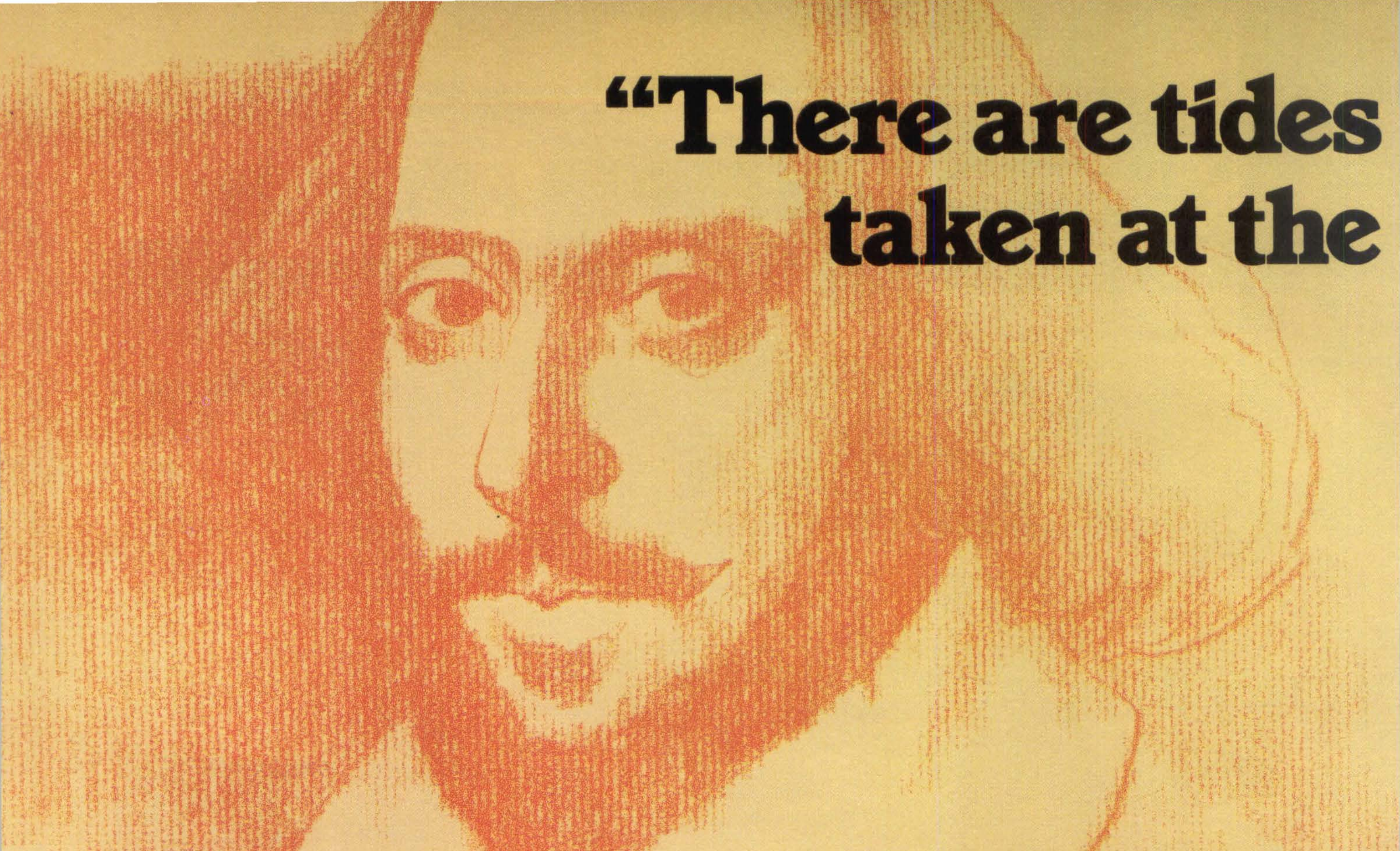

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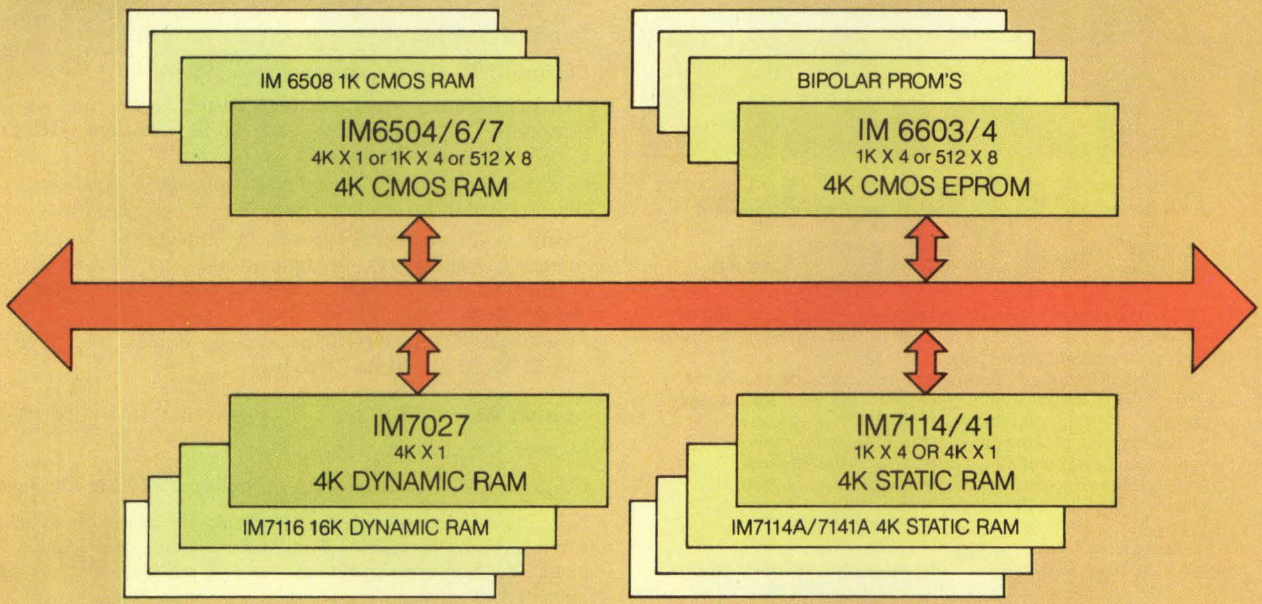
in the affairs of men which, flood, lead on to fortune."

William Shakespeare, 1564-1616



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able Speed Drive," B. de Fornel, M. Grandpierre, and J. C. Hapiot, Institut National Polytechnique De Toulouse, France

"Microprocessor Application in an Inverter-Fed Air Flow Control System," K. Katsuki, K. Igura, K. Ikeda, and I. Hosono, Development Dept of Itami Works, Mitsubishi Electric Corp, Japan

"A Microprocessor-Based Phase-Locked Loop Control System of Inverter-Fed Induction Motor Drive," F. Harashima and T. Haneyoshi, Institute of Industrial Science, University of Tokyo, Japan

Wednesday Afternoon

Session X 2-4 pm Pennsylvania Ballroom (E)

Special Topics

Chairman: R. Gentile, Babcock and Wilcox Co

"An Interpolating Algorithm for Control Applications on Microprocessors," A. Abramovich and T. R. Crawford, RCA/David Sarnoff Research Center

"Finite-State Machine Techniques for Control Applications," A. Bloch, Chestel Inc

"Software Production Improvement Activity of Recent Microcomputer Applications in Industrial Power Control Systems," S. Nishimura and T. Sumi, Industrial and Public Facility Control System Department, Fuchu Works, Japan

"Use of the Z-80 in Data Collection and Control," A. W. Winston and T. B. Smith, New IKOR Inc

Session XI 2-4 pm Pennsylvania Ballroom (W)

Motor Control Systems II

Chairman: Y. Matsumoto, Tokyo Shibaura Electric Co, Japan

"Microprocessor-Controlled High-Response Speed Regulator for Thyristorized Reversible Regenerative DCM Drives," K. Kamiyama, N. Azusawa, I. Masuda, and T. Ohmae, Ohmika Works, Hitachi Ltd, Japan

"A Microprocessor-Controlled PWM Inverter," H. Le-Huy, Engineering Department, Universite du Quebec a Trois-Rivières, Canada

"Microprocessor-Based Supervising System of High-Speed Electric Rail-Cars," S. Yasukawa and H. Kaneda, Car Performance Laboratory, Railway Technical Research Institute, Japan; and T. Kitayama, Rolling Stock Design Office, Japan

"Multi-Microcomputer System for Industrial Sequence Control," M. S. Hsieh and V. I. H. Sun, Lafarge Consultants Ltd, Canada

CONFERENCE AT A GLANCE

TIME	MONDAY, MARCH 20	TUESDAY, MARCH 21	WEDNESDAY, MARCH 22
9-11 am	*(E) Pennsylvania Ballroom (W)* Session I: DATA ACQUISITION Session II: TESTING BUS ORIENTED MICROPROCESSOR SYSTEMS	*Grand Ballroom West* Session V INDUSTRIAL CONTROL APPLICATIONS	*(E) Pennsylvania Ballroom (W)* Session VIII: CONSUMER SYSTEMS Session IX: MOTOR CONTROL SYSTEMS I
11 am-2 pm	Industrial Microprocessor Systems Exhibit	*Grand Ballroom East* Awards Luncheon 12 noon	Industrial Microprocessor Systems Exhibit
2-4 pm	*(E) Pennsylvania Ballroom (W)* Session III: SIGNAL PROCESSING Session IV: MONITORING AND CONTROL APPLICATIONS	*(E) Grand Ballroom (W)* Session VI: TESTING Session VII: ENERGY SYSTEMS	*(E) Pennsylvania Ballroom (W)* Session X: SPECIAL TOPICS Session XI: MOTOR CONTROL SYSTEMS II
4-7 pm	Industrial Microprocessor Systems Exhibit	Industrial Microprocessor Systems Exhibit	(Room assignments are subject to change.)
7-9 pm	*Pennsylvania Ballroom* Panel Session I I/O ANALOG INTERFACES	*Pennsylvania Ballroom* Panel Session II NEW DEVICES FOR INDUSTRIAL CONTROLS	

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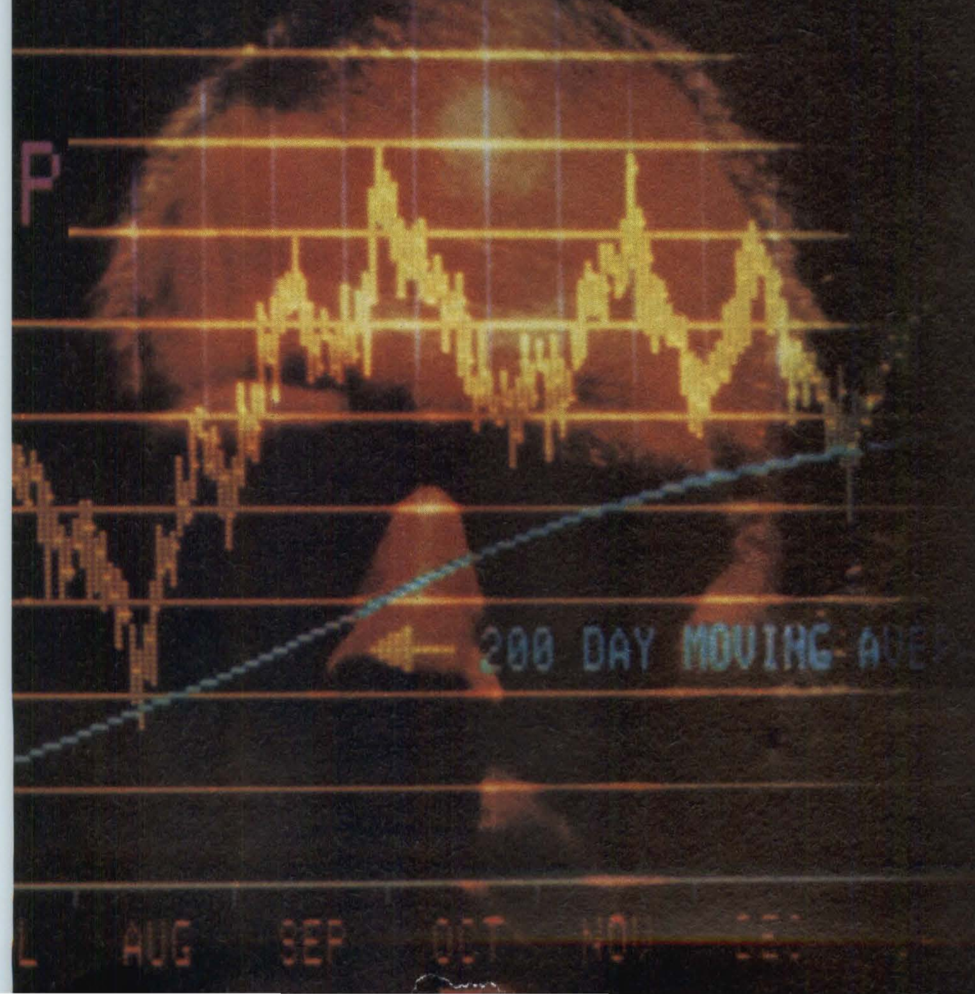

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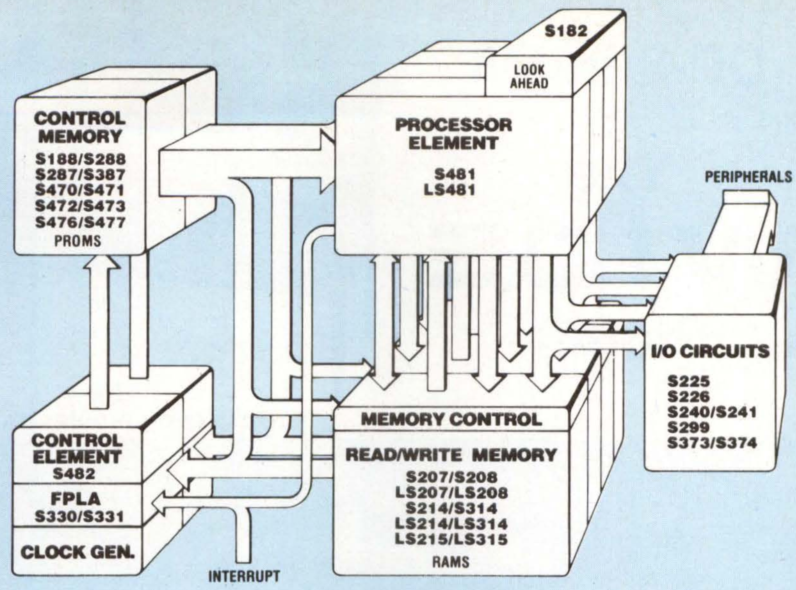

S481/LS481 Microcomputer Chip Set can be assembled from building block components to tailor performance to your application.

Processor performance choices

Both the S481 and LS481 are expandable, 4-bit slice processor elements. Both are micro and macroprogrammable.

Where maximum performance is your driving design criterion, use TI's S481 processor element. Clock frequency: up to 10 MHz for automatic multiply/divide.

For more power-conscious applications, use the LS481 processor element to cut supply current by 40 percent.

Choice of packages

Both processor elements come in a choice of packages. The space-saving, quad-in-line ceramic package (J suffix) permits maximum board density. The new 48-pin, dual-in-line plastic package (N suffix) offers a more economical cost.

Commercial-temperature (0°C to 70°C) versions of both the S and LS processor elements are available in either package. The low-power Schottky processor element is also available in a full-temperature (–55°C to 125°C) version in the ceramic quad-in-line package – the SN54LS481J.

Extraordinary capability

Each processor element recognizes, decodes, and executes 24,780 instructions.

For example, either element performs compound operations – select two operands, add, sign protected shift, generate status and update memory – all within a single clock cycle.

Only the S481/LS481 bit slice provides on-chip algorithms for automatically sequencing the iterative multiply and divide – both signed and unsigned. And cyclical-redundancy character update is also provided.

Advanced architecture

Behind this outstanding capability: TI's advanced Schottky TTL process technology. Plus TI's advanced 9900 Family memory-to-memory architecture.

This is a complete architecture that places register files in main memory. As a result, the number of available general-purpose registers is limited only by the size of the program memory. Instructions do more work, use less memory space. Interrupts are handled faster.

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- Parallel dual input/output ports.
- Full function ALU with carry look-ahead capability and magnitude status generation.
- Double-length accumulator with full shifting capability, sign-bit handling, and impending overflow signal.
- On-chip dual memory address generators.

Performance-matched support functions

Complementing the speed and efficiency of the processor elements are these Schottky TTL support functions:

Device No.	Function	Package
S225	16W x 5B FIFO	N,J
S226	Latched transceiver	N,J
S240,S241	Octal bus drivers	N,J
S330,S331	12 input, 50 term, 6 output FPLAs	N,J
S373	Octal latch	N,J
S374	Octal flip flop	N,J
S482	Control element	N,J

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CIRCLE 51 ON INQUIRY CARD

AN INTRODUCTION TO VECTOR PROCESSING

Execution speed of scientific problems can be considerably enhanced by hardware and software design that provides for efficient execution of program loops. A large scale scientific computer incorporates vector processing for high speed execution of loops without sacrifice of processing speed in nonloop situations

Paul M. Johnson Cray Research, Incorporated, Minneapolis, Minnesota

Since program loops occur so frequently in scientific processing, providing for their efficient execution in both hardware and software design can considerably enhance the execution speeds of scientific problems. Within a loop, array indices are typically linear functions of the loop control variable. For example, the FORTRAN statements

```
    DO 100 I=1,21,2
100 A(I) = B(I+3) + 10
```

define a simple program loop that adds 10 to elements of array B and stores the sums in array A. The array indices—I in the case of array A and I+3 in the case of array B—are linear functions of I, the loop control variable; I ranges from 1 to 21 in steps of 2.

For most computers, the machine language equivalent of this FORTRAN loop is a sequence of instructions that reads a single element of the B array, adds the constant 10, and writes the result into the A array. The loop control variable is incremented and these steps are repeated until the variable equals the limit value. A single number, such as the individual elements of the B array or the constant 10, is called a scalar. Scalar processing is the application of arithmetic and logical operations on scalars. Some computers exploit the repetitive nature of loops through use of instructions that operate on series of numbers. One instruction reads a series of elements of the B array, another adds 10 to the elements, and yet another writes the series of sums into the A array. Such a series of numbers is called a vector, and vector processing is the application of arithmetic and logical operations on vectors. One major advantage of vector processing over scalar processing is elimination of overhead associated with maintenance of the loop control variable. In many cases, loops reduce to a simple sequence of instructions without backward branching.

However, not all aspects of a problem lend themselves to vector processing and, for these, scalar techniques should still be applied. Thus, one failing of early vector processors is their inability to compete successfully in scalar applications. Moreover, some vector processors require long vectors in order to show an advantage over conventional scalar processors (this is called the "start-up" time). Another failing is that memory conflicts due to the simultaneous reading of operand vectors from memory and writing of result vectors to memory often degraded vector performance.

Computer Architecture

Architecture of the CRAY-1[R] computer exhibits none of these objectionable traits. Conceptually, the machine is both a scalar and a vector processor, with instructions and registers for both applications. Start-up time for vector operations is short enough so that vector processing is more efficient than scalar processing for vectors containing as few as two elements. Register to register vector instructions eliminate the problem of memory conflicts. Scalar and vector processing capabilities of the computer are characterized by high processing rates in vector applications.

Operating Registers

Primary operating registers are the scalar and vector registers, called S and V registers, respectively (see Fig 1). Each of the eight S registers has a single element; each of the eight V registers has 64 elements. Scalar instructions perform some function, such as addition, by obtaining operands from two S registers and entering the result into another S register. The analogous vector instruction repetitively performs the same function, obtaining new pairs of operands from elements of two V registers during each clock period (12.5 ns). Results are entered into elements of another V register. Contents of the vector length (VL) register determine the number of operations performed by vector instructions.

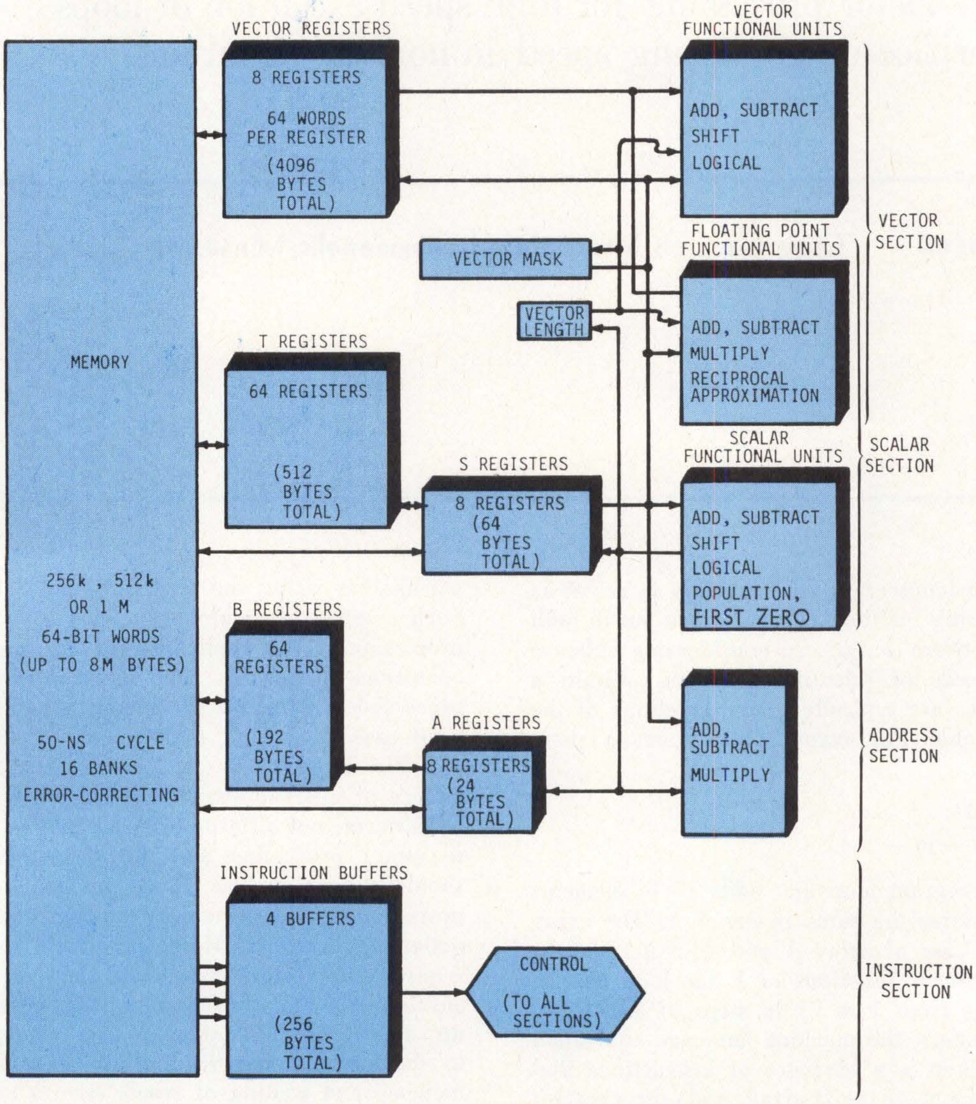


Fig 1 Register block diagram. Primary operating registers are scalar and vector registers, called S and V registers, respectively. Eight A registers are used as address registers for memory references and as index registers. A and S registers are each supported by 64 rapid-access temporary storage registers, called B and T registers, respectively. All registers can receive data from or send data to 1M-word bipolar memory. Instructions are executed from four instruction buffers. Arithmetic, logical, and shift operations are performed by 12 specialized functional units

Eight 24-bit A registers are used as address registers for memory references and as index registers. A and S registers are each supported by 64 rapid-access temporary storage registers, called B and T registers, respectively. All registers can receive data from or send data to memory.

Memory

Memory is constructed of bipolar 1024-bit large-scale integrated (LSI) chips. Up to 1 million 64-bit words are arranged in 16 banks with a bank cycle time of four clock periods. The short cycle time provides an extremely efficient random-access memory. Circuitry is provided for correction of all single-bit errors and detection of all double-bit errors.

Instruction Buffers

All instructions, which are 16- or 32-bits long, are executed from four instruction buffers, each consisting of sixty-four 16-bit registers. Since the four instruction buffers are large, substantial program segments may be stored. Forward and backward branching within the buffers is possible and program segments may be discontiguous. When the current instruction does not reside in a buffer, one instruction buffer is filled from memory. Four memory words are read per clock period to the least recently filled instruction buffer. To allow the current instruction to issue as soon as possible, the memory word containing the current instruction is the first to be read.

Input/Output

Any number of the 12 input and 12 output channels may be active at a given time. Each channel has a maximum transfer rate of 80M bytes/s. At most, one 64-bit word can be transferred to or from memory during each clock period; this is attained when four input channels and four output channels are operating simultaneously at their maximum rates. In practice, this theoretical transfer rate is limited by the speed of peripheral devices and by memory reference activity of the central processing unit (CPU).

Functional Units

Twelve specialized functional units in the CPU handle the arithmetic, logical, and shift operations. Each unit is independent of the others, and any number of functional units may be in operation at the same time. A functional unit receives operands from registers and delivers the result to a register when the function has been performed. These units operate essentially in a 3-address mode, with source and destination addressing limited to certain registers.

Three functional units, integer add, integer multiply, and population count, provide 24-bit results to A registers only. Integer add, shift, and logical units provide 64-bit results to S registers only. Sixty-four-bit results are provided to V registers only by integer add, shift, and logical units. Floating add, floating multiply, and reciprocal approximation units provide 64-bit results to either S or V registers.

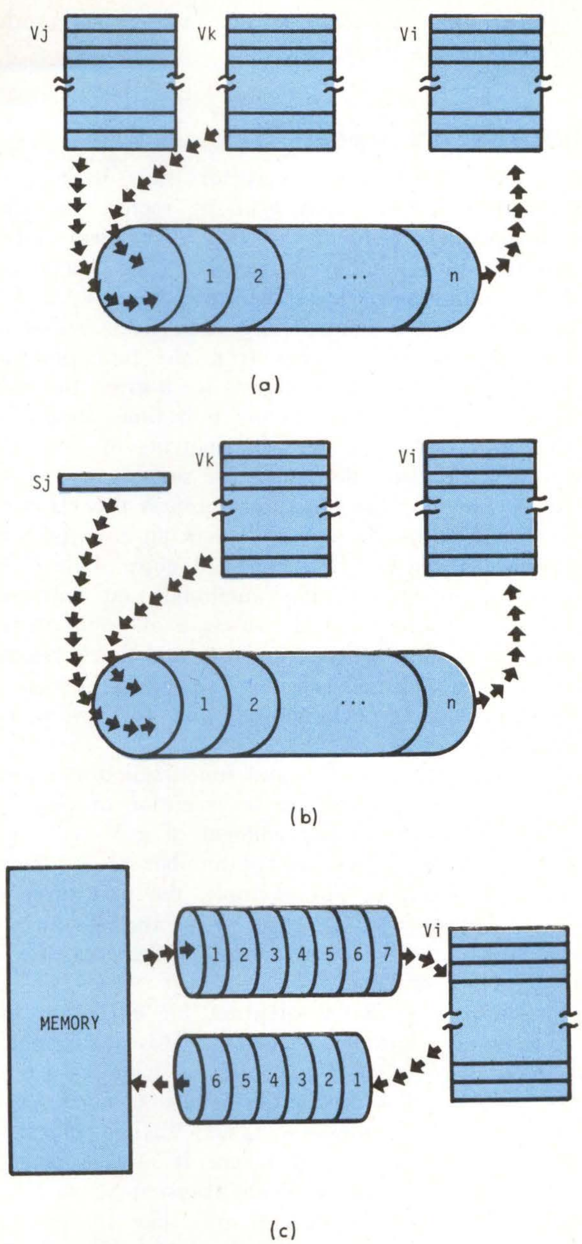


Fig 2 Vector instructions. Type I (a) instructions take operands from one or two vector registers. Type II (b) instructions take one operand, a constant, from scalar register, and second operand from vector register. Type III and IV instructions (c) read operands from memory or write operands to memory. Operands need not be contiguous and increment can be either positive or negative

All functional units are fully segmented. This means that information arriving at the unit or moving within it is captured and held in a new set of registers at the end of each clock period. Therefore, it is possible to start a new set of operands for unrelated computation into a functional unit each clock period even though the unit may require more than one clock period to complete the calculation. All functional units perform their algorithms in a fixed amount of time. No delays are possible once operands have been delivered to the unit. Functional units servicing vector instructions produce one result per clock period.

Vector Instructions

Instructions that operate on vectors may be classified into four types. The first type of vector instruction obtains operands from one or two V registers and enters results into another V register [Fig 2(a)]. Successive operand pairs are transmitted from Vj and Vk to the segmented functional unit each clock period and corresponding results emerge from the functional unit n clock periods later. n is constant for a given functional unit and is called the functional unit time. Results are entered into result register Vi. Contents of the vector length (VL) register determine the number of operand pairs processed by the functional unit. A type II vector instruction obtains one operand from an S register and one from a V register [Fig 2(b)]. A copy of the S register is transmitted to the functional unit with each V-register operand. The last two types of vector instructions transmit data between memory and the V registers [Fig 2(c)]. A path between memory and the V registers may be considered a functional unit for timing considerations.

It is important to understand functional unit segmentation, especially as it relates to execution of vector instructions. Let a particular element of a V register be specified by adding the element number as a subscript to the register name. For example, the first three elements of register V1 are $V1_0$, $V1_1$, and $V1_2$, respectively. Since a vector register has 64 elements, the last element of V1 is $V1_{63}$.

Fig 3 shows a timing diagram for execution of a floating point addition instruction. This instruction is type I, since operands are obtained from two vector registers. When the instruction issues at clock period t_0, the first pair of elements ($V1_0$ and $V2_0$) is transmitted to the add functional unit where it arrives at clock period t_1. Dashed lines indicate transmit to and from the functional unit. Functional unit time for this unit is six clock periods; therefore, the first result, which is the sum of $V1_0$ and $V2_0$, exits from the functional unit at clock period t_7. The sum is transmitted to the first element of the result register V0, arriving at clock period t_8. Because the functional unit is fully segmented, the second pair of elements ($V1_1$ and $V2_1$) is transmitted to the add functional unit at clock period t_1. At clock period t_2 the functional unit is in the process of performing two additions simultaneously since addition of $V1_0$ and $V2_0$ was begun in the previous clock period. The second result, which is the sum of $V1_1$ and $V2_1$, is entered into the second element of result register V0 at clock period t_9. Continuing in this manner, a new pair of elements enters the functional unit each clock period and the corresponding sum emerges from the unit six clock periods later and is transmitted to the result register. Since a new addition is begun each clock period, six additions may be in progress at one time. In general, the number of operations that can be performed simultaneously by a functional unit is equal to the functional unit time.

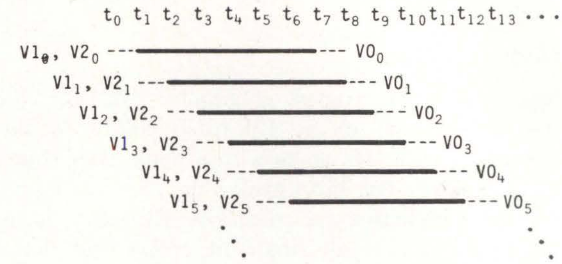


Fig 3 Vector instruction timing example (V0←V1+V2). New pair of operands is sent to functional unit each clock period. After first result emerges from functional unit, new result is sent to result register each clock period

Vector length determines the total number of operations performed by a functional unit. Although each vector register has 64 elements, only the number of elements specified by the vector length register is processed by a vector instruction. Vectors that have more than 64 elements are processed under program control in groups of 64 (with a possible residue). A later section on vector loops will illustrate the processing of long vectors.

Functional Unit and Operand Register Reservations

When a vector instruction issues, the required functional unit and operand registers are reserved for the number of clock periods determined by the vector length. A subsequent vector instruction that requires the same functional unit or operand register cannot be issued until the reservations are released. When two vector instructions use different functional units and vector registers, they are independent and may issue in consecutive clock periods. Some examples follow. Ex (1) shows two independent instructions. Both execute concurrently with a one clock period difference in their issue times. Ex (2) through (4) illustrate the effect of functional unit and operand register reservation when two instructions are not independent. Ex (2) shows two add instructions. When the first instruction issues, the floating add functional unit and operand registers V1 and V2 are reserved. Issue of a second add instruction is delayed until the functional unit is free. Ex (3) shows an add instruction followed by a multiply instruction. As in Ex (2), the floating add functional unit and operand registers V1 and V2 are reserved when the first instruction issues. Issue of the second instruction is delayed until operand register V1 is free. The second instruc-

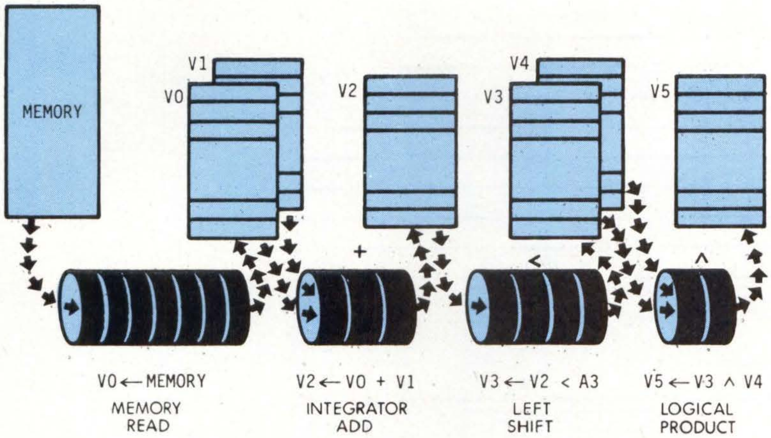


Fig 4 Chaining example. Chain of four instructions reads vector of integers from memory, adds that vector to another, shifts sum, and finally forms logical product of shifted sum and mask vector. Diagram illustrates how functional units may be considered links in chain which works as a whole to produce first result

tion in Ex (4) is delayed because of both functional unit and operand register reservations.

(1) Independent Instructions
V0 ← V1 + V2
V3 ← V4 * V5

(2) Functional Unit Reservation
V3 ← V1 + V2
V6 ← V4 + V5

(3) Operand Register Reservation
V3 ← V1 + V2
V6 ← V1 * V5

(4) Functional Unit and Operand Register Reservation
V0 ← V1 + V2
V3 ← V1 + V5

Result Register Reservations and Chaining

When a vector instruction issues, the result register is reserved for the number of clock periods determined by the vector length and functional unit time. This reservation allows the final operand pair to be processed by the functional unit and the corresponding result to be transmitted to the result register.

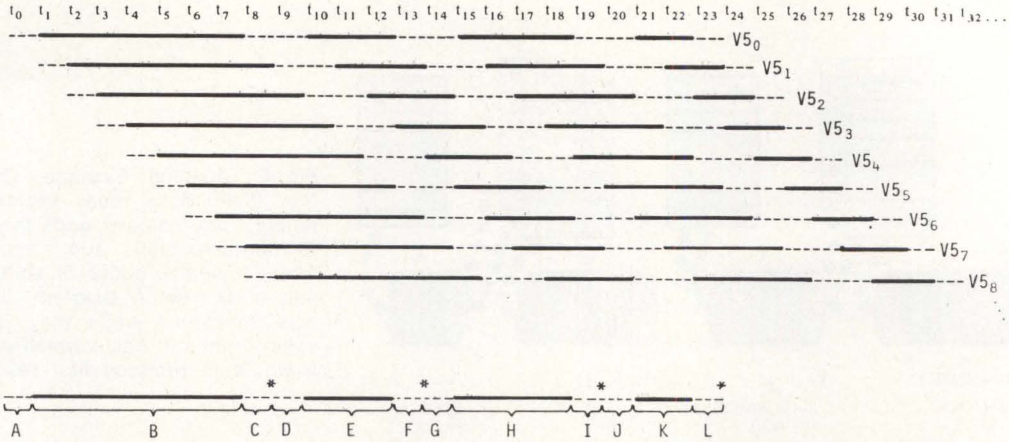
A result register becomes the operand register of a succeeding instruction. In the process called "chaining," the succeeding instruction issues as soon as the first result arrives for use as an operand. This clock period is termed "chain slot time"; it occurs only once for each vector instruction. If the succeeding instruction cannot issue at chain slot time because of a prior functional unit or operand register reservation, it must wait until the result register reservation is released.

Fig 4 shows a chain of four instructions which read a vector of integers from memory, add that vector to another, shift the sum, and finally form the logical product of the shifted sum and a mask vector. The result of the four instructions is in vector register V5. The diagram depicts passage of information through functional units, and illustrates the idea that functional units may be considered links in a chain which works as a whole to produce the final result.

The timing diagram in Fig 5 clarifies the concept of chaining. Graduations along the horizontal axis represent clock periods. The memory read instruction issues at clock period t_0. Each horizontal line shows the production of one element of the V5 result vector. Time spent in passing through each of the four functional units used in the instruction sequence (see Fig 4) is indicated by bars of corresponding length in the timing diagram (Fig 5). Note that the production of a new element of V5 begins each clock period. Production of the first element of V5 begins at clock period t_0 with the reading of the first word from memory, production of the second element of V5 begins at clock period t_1 with the reading of the second word from memory, and so on. The first result enters V5 at clock period t_{24} and a new result enters V5 each clock period thereafter. The first horizontal line, which shows production of the first element of V5 ($V5_0$), is reproduced below the timing diagram with segments lettered for identification. Chain slot times for each functional unit are indicated by asterisks.

A detailed description of the production of $V5_0$ serves for illustration; production of other elements of the result vector is identical except for the staggered start times.

The vector read instruction issues at clock period t_0. The first word arrives in element 0 of register V0 at



A - TRANSIT OF MEMORY WORD TO "READ FUNCTIONAL UNIT"

B - TRANSIT OF MEMORY WORD THROUGH "READ FUNCTIONAL UNIT"

C - TRANSIT OF MEMORY WORD FROM "READ FUNCTIONAL UNIT" TO ELEMENT OF V0

D - TRANSIT OF OPERAND ELEMENTS IN V0 AND V1 TO INTEGER ADD FUNCTIONAL UNIT

E - COMPUTATION OF SUM BY INTEGER ADD FUNCTIONAL UNIT

F - TRANSIT OF SUM FROM INTEGER ADD FUNCTIONAL UNIT TO ELEMENT OF V2

G - TRANSIT OF OPERAND ELEMENT IN V2 TO SHIFT FUNCTIONAL UNIT

H - SHIFT OPERATION PERFORMED BY SHIFT FUNCTIONAL UNIT

I - TRANSIT OF SHIFTED SUM FROM SHIFT FUNCTIONAL UNIT TO ELEMENT OF V3

J - TRANSIT OF OPERAND ELEMENTS IN V3 AND V4 TO LOGICAL FUNCTIONAL UNIT

K - LOGICAL OPERATION PERFORMED BY LOGICAL FUNCTIONAL UNIT

L - TRANSIT OF FINAL RESULT TO ELEMENT OF V5

Fig 5 Timing diagram for chaining. Each horizontal line shows production of one element of V5 vector result. Time spent in passing through each function unit used in instruction sequence is indicated by bar of corresponding length. Chain slot times for each functional unit are indicated by asterisks

clock period t_9, and is immediately transmitted along with element 0 of register V_1 as an operand to the integer add functional unit. When the two operands arrive at the integer add functional unit at clock period t_{10}, computation of the sum of $V0_0$ and $V1_1$ is begun. Three clock periods later (t_{13}) the sum is sent from the functional unit to element 0 of V2. It arrives at clock period t_{14} and is immediately transmitted as an operand to the shift functional unit. At clock period t_{15} the operand arrives at the shift functional unit and the shift operation is begun. The operation is completed four clock periods later (t_{13}) and the shifted sum is sent from the functional unit to element 0 of V3, arriving at the next clock period. It is immediately transmitted, along with element 0 of V4, as an operand to the logical functional unit. When the two operands arrive at the logical functional unit at clock period t_{21}, computation of the logical product of $V3_0$ and $V4_0$ is begun. Two clock periods later (t_{23}) the final result is sent from the functional unit to element 0 of V5, arriving at clock period t_{24}. While all this has been going on, production of the second element of V5 has been tracing the same path through the vector registers and functional units with a one clock period lag. Production of the third element of V5 lags one more clock period behind, and so on. A new result arrives at the V5 result register each clock period.

Vector Loops

Long vectors are processed in segments since the vector registers of the computer cannot accommodate vectors with more than 64 elements. The program construct created to process long vectors is called a vector loop. Each pass through the loop processes a 64-element (or smaller) segment of the long vectors. The general procedure is to compute the loop count based on the vector length before entering the loop. Inside the loop the program takes full advantage of the 12 independent functional units and chaining to read current vector segments from memory, execute required functions, and return results to memory. Loop control is performed in the scalar registers concurrently with vector processing. Loop branch time is hidden by vector operations.

Processing of long vectors is illustrated by the following simple FORTRAN loop.

```
    DO 100 I=1,N
100 A(I) = 5. * B(I) + C
```

The loop computes the Ith element of A by adding C to five times the Ith element of B, where I ranges from 1 to N. When N is 64 or less, all elements of the A array can be assigned a value with the following sequence of seven instructions.

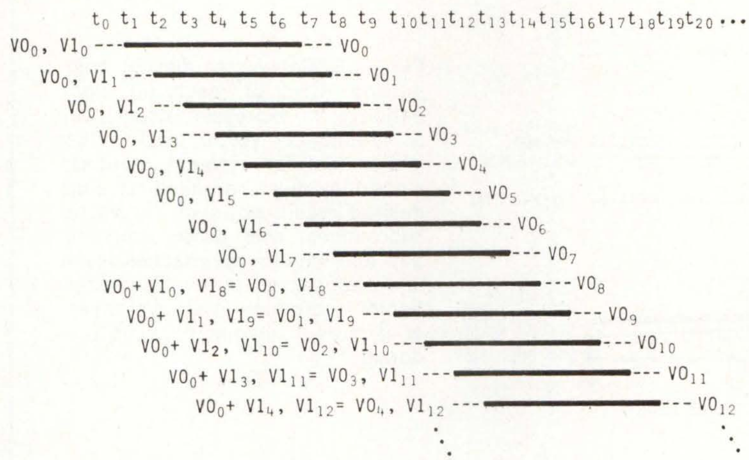


Fig 6 Timing diagram for recursive vector sum. Early results are re-sent to functional unit as operands. At instruction completion, dot product's 64 partial sums will have been reduced to eight, which will be held in elements $V0_{56}$ through $V0_{63}$

(1)	S1 ← 5.	Set constant 5	
(2)	S2 ← C	Set constant C	
(3)	VL ← N	Set vector length	
(4)	V0 ← B array	Read B array	chain
(5)	V1 ← S1*V0	Multiply elements by 5	chain
(6)	V2 ← S2+V1	Add C	chain
(7)	A array ← V2	Store A array	

Instructions (4) to (6) use different functional units ("memory," multiply, and add, respectively); therefore, they can be chained. When the V2 result register is free, results are stored in the A array.

When N exceeds 64, a vector loop is required to generate the entire A array. Before entering the loop, N is divided by 64 to determine the loop count. If there is a remainder, less than 64 elements of A are generated in one pass through the loop. The loop performs instructions (4) to (7) for a segment of the A and B arrays. The last vector operation at the bottom of the loop stores the current segment of the A array in memory. This operation must be completed before the next segment of the B array can be read in the next pass through the vector loop. The time required to decrement the loop counter, increment the current position in the arrays, and branch to the top of the loop is hidden because it is done in parallel with the store operation.

Dot Product and Recursive Vector Operations

The dot product of two vectors, $A = (a_0,a_1,...,a_N)$ and $B = (b_0,b_1,...,b_N)$ is defined by

$$A \cdot B = \sum_n a_n \cdot b_n$$

Computation of the dot product is achieved by a vector loop and a scalar loop. The vector loop, which contains a multiply-add chain, first computes 64 partial sums; element n of the result vector register contains the sum of every sixty-fourth product, $a_i \cdot b_i$, starting with $a_n \cdot b_n$. The scalar loop then adds partial sums to compute the complete dot product. An intermediate step that reduces the number of partial sums from 64 to eight may be interposed between the vector and scalar loops. This step executes a vector add instruction that has the register of partial sums as both operand and result register.

To see how this is done, observe that there is an element counter associated with each vector register. When a vector instruction issues, counters for its operand and result registers are zeroed. Normally, sending an operand from an operand register to a functional unit causes the counter associated with that register to be incremented; the counter always points to the next available operand. Similarly, a result arriving at the result register from a functional unit causes the counter

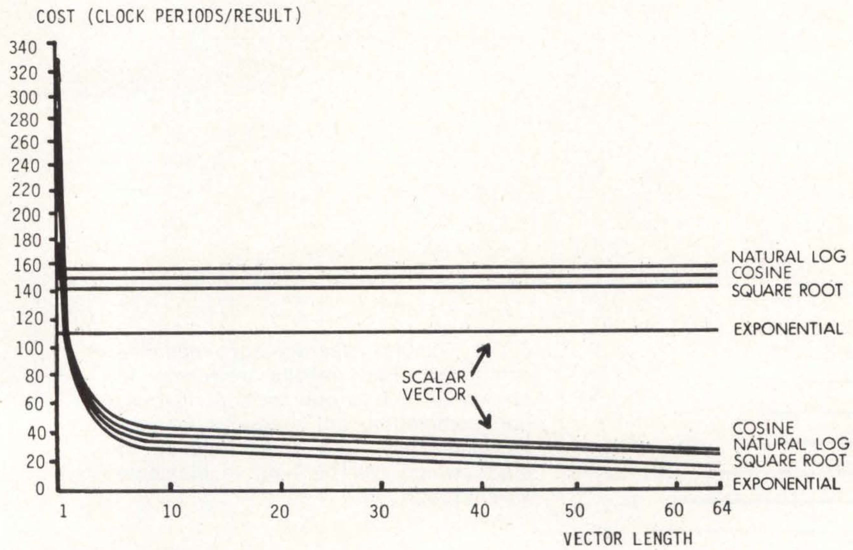


Fig 7 Scalar/vector timing comparison. Cost of result (in clock periods) is expressed graphically as function of vector length. Cost is constant for scalar subroutines since they must be called for each desired result; however, for vector subroutines, cost drops dramatically and rapidly approaches lower limit as vector length increases. Vector subroutine is always cheaper if more than one result is produced

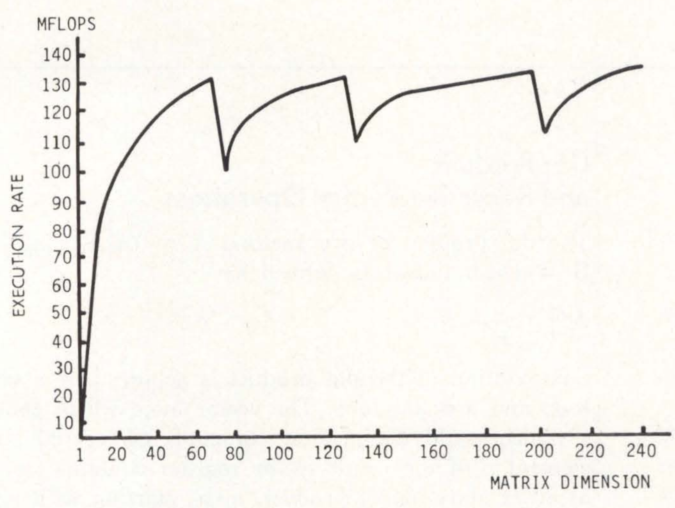


Fig 8 Matrix multiplication timing. Execution rate, expressed as millions of floating point operations per second, is plotted as function of vector length. Typical of problems that can be vectorized, matrix multiplication can be performed with significant increase in speed over conventional scalar processing

associated with that register to be incremented. However, when a register serves as both operand and result register, its counter does not begin advancing until the first result arrives from the functional unit. While the counter is held at 0, the contents of element 0 are repeatedly sent to the functional unit. Consider what happens if element 0 of register V0 is cleared and then V0 is used as both operand and result register for an add instruction. The register of partial sums, eg, V1, is used as the other operand register.

Refer to the timing diagram in Fig 6. When the add instruction issues at clock period t_0, operands from elements $V0_0$ and $V1_0$ are sent to the add functional unit. One clock period later, when the first addition begins, elements $V0_0$ and $V1_1$ are sent to the add functional unit. Note that, because V0 is both operand and result register, the element counter associated with V0 does not increment. Thus, the element of V0 that is sent at clock period t_0, $V0_0=0$, is sent again at clock period t_1. This holds true for six more clock periods. The counter for

V1 advances, but the counter for V0 remains at 0. Finally, at clock period t_8, the first sum arrives at element 0 of the result register, V0. The element counter for V0 now begins to advance once each clock period. At clock period t_8, elements $V0_0$ and $V1_8$ are sent to the add functional unit. Note that $V0_0$ is the sum of the original $V0_0$ and $V1_0$. Thus, since $V0_0$ was initially 0, summation of $V1_0$ and $V1_8$ is beginning. At clock period t_9, elements $V0_1$ and $V1_9$ are sent to the functional unit; since $V0_1$ is the sum of the original $V0_0$ and $V1_1$, summation of V_1 and $V1_9$ is beginning. The recursive character of the instruction should be becoming clear; as results are produced, they are re-sent to the functional unit as operands. At instruction completion, elements $V0_{56}$ through $V0_{63}$ contain the dot product's eight partial sums, reduced in number from the original 64. In this example, a vector length of 64 was assumed; however, the same technique is applicable for vectors of shorter length.

FORTRAN Library

The following performance study of matrix multiplication and several subroutines from the CRAY-1 FORTRAN library illustrates the high processing rates attainable through vector processing. Each scalar FORTRAN library subroutine has a vector analog which employs the same algorithm in vector mode to produce several results at a time. Scalar subroutines must be called for each desired result, while vector subroutines process an argument vector to obtain a vector of results. Performance studies on the CRAY-1 indicate that a vector subroutine outperforms its scalar counterpart whenever a vector of two or more results is required. Fig 7 depicts the behavior of the scalar and vector subroutines for several library functions. Cost of a result (in clock periods) is plotted as a function of vector length. Cost is constant for scalar subroutines since they must be called for each desired result; however, for vector subroutines, the cost drops dramatically and rapidly approaches a lower limit as vector length increases. In all cases vector cost is less than scalar cost when more than one result is produced.

Matrix Multiplication

Let [X] denote a matrix and let the element in row i, column j be denoted by x_{ij}. Given matrix [A] of dimension K by N and matrix [B] of dimension N by M, the product matrix [C] = [A] • [B] is defined by

$$c_{ij} = \sum_{n=1}^{N} a_{in} \bullet b_{nj}$$

Calculation of the product matrix is amenable to vector processing. The combination of multiplication and addition lends itself well to chaining. Fig 8 shows the computer's execution rate for multiplication of square matrices as a function of matrix dimension. Execution rate is defined in terms of "millions of floating point operations per second" (MFLOPS). This measure is more meaningful than the classical "millions of instructions per second" (MIPS), especially when comparing relative speeds of scalar and vector machines; a single vector instruction is equivalent to a loop of several scalar instructions. The number of floating point operations required to multiply two n-dimensional square matrices is $n^2(2n - 1)$, since each of the n^2 elements of the result matrix is formed by summing n products.

Matrix multiplication is typical of the large class of problems that can be vectorized. For these problems a significant increase in processing speed can be achieved over conventional scalar processing. Register to register vector instructions and the large amount of concurrency attainable through use of the 12 independent functional units and chaining provide high processing speeds presently unmatched. Fields such as weather forecasting, nuclear research, and seismic data analysis provide typical applications.

Summary

Capabilities of the CRAY-1 that contribute to its high processing rates for both scalar and vector applications include its large, fast random-access memory, instruction buffers, high bandwidth input/output channels, and full segmentation of the 12 independent functional units. Chaining techniques and the use of register to register vector instructions help eliminate the problem of speed degradation associated with memory to memory vector instructions. Additionally, start-up times for vector operations are nominal and the advantages of vector processing can be realized even for short vectors. Thus, the computer system's architecture meets its design goal for efficient execution of program loops by using vector processing, yet does not sacrifice scalar performance.

Bibliography

Cray Research, Inc, *CRAY-1 Computer System Hardware Reference Manual*, Minneapolis, Minn, Nov 1977

P. H. Enslow, Jr, "Multiprocessor Organization—A Survey," *ACM Computing Surveys*, Mar 1977, pp 103-129

P. M. Johnson, "An Introduction to Vector Processing," Cray Research, Inc, Minneapolis, Minn, 1975

D. J. Kuck, "A Survey of Parallel Machine Organization and Programming," *ACM Computing Surveys*, Mar 1977, pp 29-60

C. V. Ramamoorthy and H. F. Li, "Pipeline Architecture," *ACM Computing Surveys*, Mar 1977, pp 61-102

R. M. Russell, "The CRAY-1 Computer System," *Communications of the ACM*, Jan 1978, pp 63-72

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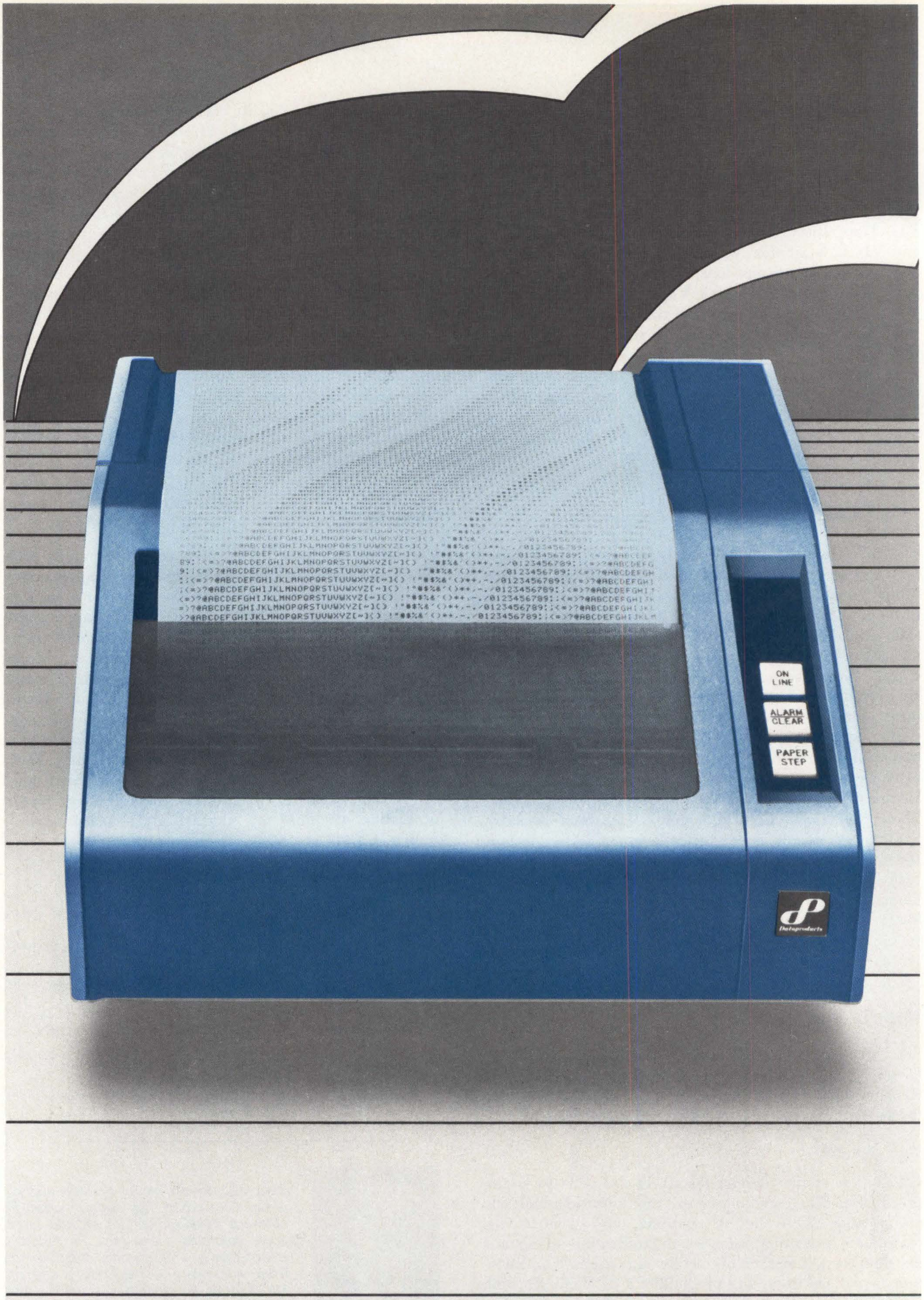
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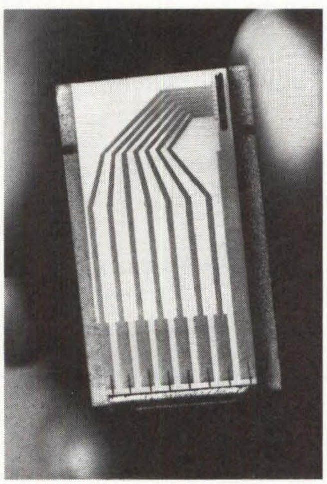

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INTEGRATING MEDIUM SPEED MODEMS INTO COMMUNICATIONS NETWORKS

Medium speed modems are being designed into computer terminals, communications frontends, and data communication multiplexers for transmitting serial-bit information over telephone lines. Hardware, interface, and diagnostic protocols are examined for effective and efficient communications

Ken Krechmer The Vadic Corporation, Sunnyvale, California

Directly integrating a modem into a host device eliminates separate requirements for power supply, enclosure, and generalized support capabilities. When the host device is to be operator controlled and data are to be transmitted over telephone lines, 1200-bit/s modems adequately fulfill the information handling needs for data entry terminals, since human reading speed is rarely faster than 120 char/s for technical information, and since one character is equivalent to 10 bits. Customizing 1200-bit/s modems for dedicated applications minimizes costs and excludes functional clutter for the host device.

Modem Operation

Medium speed (1200-bit/s) modems use frequency shift keying (FSK) modulation, which employs a mark frequency to designate a logical 1 state and space frequency for logical 0. Telephone companies use a mark frequency of 1200 Hz and a space frequency of 2200 Hz. Since the telephone line bandwidth is from 300 to 3300 Hz, a centering of the mark and space frequencies around 1700 Hz allows transmissions to take place in the least distorted part of the band. However, in FSK design, as long as the center frequency (average of mark and space frequencies) remains the same, differing choices of mark and space frequencies can be allowed without impacting compatibility with telephone company modems. The modem receiver receives spectral energy, not particular frequencies. For 1200-bit/s modem operation, 1300 and 2100 Hz are better choices for mark and space frequencies, respectively, than 1200 and 2200 Hz. In many applications, this choice provides a 2 to 1 improvement in system performance over leased or dial-up lines without any impact on cost. Fig 1 shows the performance improvement possible.

FSK modems are characterized by manufacturing simplicity, low power dissipation, and low cost. Frequency modulation, although more complex than amplitude modulation, offers greater scope for adjusting the signal-to-noise (S-N) ratio since the range over which the frequency is modulated can be varied. When a wide frequency range is used, the power required is decreased. In addition, for a given transmission power, a higher S-N ratio can be obtained (noise energy is constant) when the range over which the frequency is modulated is wide. Thus, improved performance is acquired at the expense of increased bandwidth. Because of the inefficient use of available bandwidth, however, FSK modems are not useful above 1200 bits/s on dial-up lines, although they can be on conditioned, leased lines.

FSK modems provide the lowest cost as a function of bit rate. Modem speeds of 1200 bits/s are prevalent since the integrated cost is about the same from 300 through 1200 bits/s. As a modem's bit rate increases above 1200 bits/s, cost increases significantly and the need for ad-

Modem Basics

A contraction of the words modulator-demodulator, a modem is an electronic device that converts signals for transmission or reception over telephone lines. Since telephone lines were designed for analog voice transmission, it is not possible to transmit digital information from a terminal or a computer in its binary form. Telephone line networks have a bandwidth of approximately 3000 Hz; thus, modems used on the telephone lines must condition signals to fit within this band (Fig A).

For transmission over phone lines, digital signals are translated into either amplitude- or frequency-modulated audio signals (Fig B).

EIA Interface Signals

TXD	Transmit data (103)
RXD	Receive data (104)
RTS	Request to send (105)
CTS	Clear to send (106)
DSR	Data set ready (107)
DTR	Data terminal ready (108/2)
RI	Ring indicator (125)
CXR	Carrier detector (109)

International designations per CCITT standards are in parentheses.

Specifications

Interface—Computer or Terminal

- EIA RS-232-C
- Bell Telephone
- IBM
- MIL-188
- CCITT
- Other

Interface—Telephone Line

- Dial or switched network
- Private, leased, or dedicated line
  - 2-wire
  - 4-wire
- Conditioning
- DDS (digital data service)
- Special carrier

Speed

- Low speed—0 to 300 bits/s
- Medium speed—0 to 1800 bits/s
- High speed—2000 to 9600 bits/s
- Very high speed—19.2k to 250k bits/s

Communication Mode on 2-Wire Service

- Simplex—Transmission in one direction only
- Half-duplex—Transmission in two directions, but only one direction at a time
- Full-duplex—Transmission in both directions simultaneously

Modem specifications include business machine and telephone line interfaces as well as speed, communications mode, and performance criteria.

Standards

Common CCITT standards are:

V.21	0 to 200 (300) bit/s (similar to Bell 103). Defined for full-duplex (FDX) switched network operation.
V.23	600/1200 bit/s (similar to Bell 202). Defined for half-duplex (HDX) switched network operation. 75-bit/s channel optional
V.24	Definition of interchange circuits (similar to EIA RS-232-C)
V.25	Automatic calling units (similar to Bell 801)
V.26	2400 bit/s (identical to Bell 201B). Defined for 4-wire leased circuits
V.26 bis	2400/1200 bit/s (similar to Bell 201C). Defined for switched network
V.27	4800 bit/s (similar to Bell 208A). Defined for leased circuits using manual equalizers
V.28	Electrical characteristics for interchange circuits (similar to RS-232-C)

Inside the U.S., data interface standards are set by the Electronic Industries Association (EIA). Data transmission standards are only broadly defined by the Federal Communications Commission (FCC), so that considerable user choice is possible. In practice, users tend to adhere to telephone company standards.

Outside the U.S., data transmission standards are set by the International Telegraph & Telephone Consultative Committee (CCITT), which is a part of the International Telecommunications Union in Geneva, Switzerland.

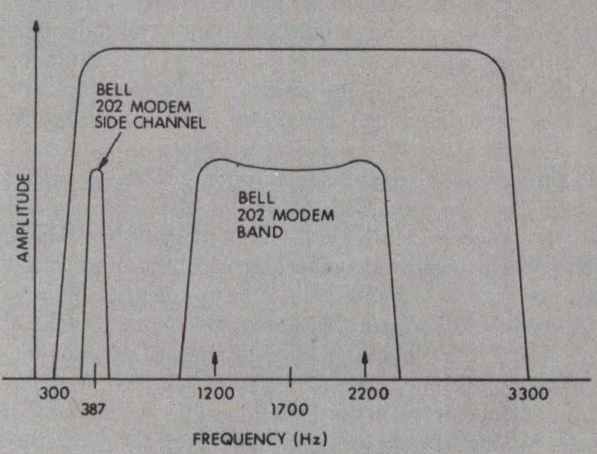


Fig A Telephone line bandwidth

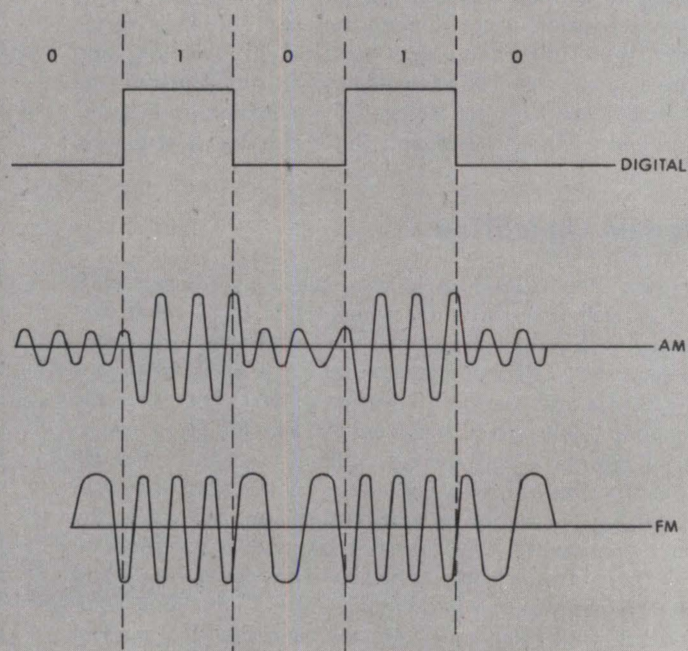


Fig B Digital signal translation

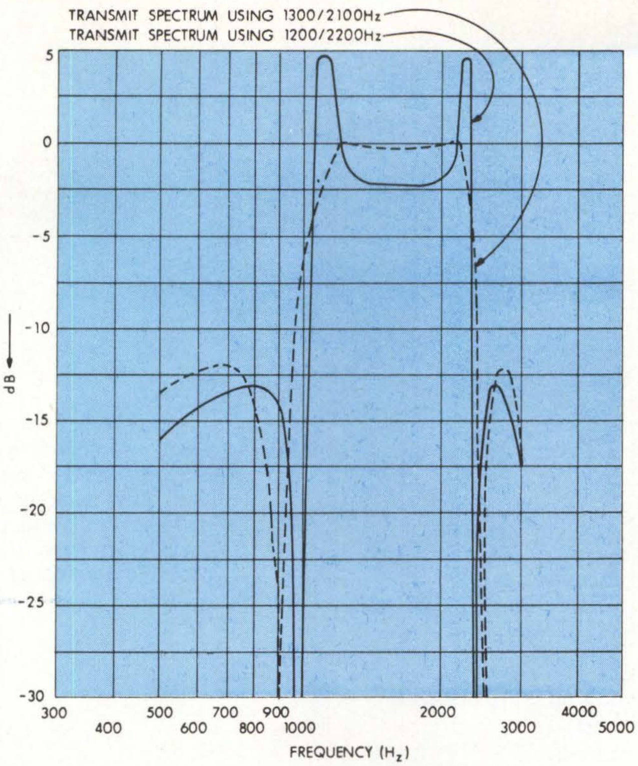


Fig 1 Transmit spectrum. Transmit spectrum (solid line) is highly peaked at 1200- and 2200-Hz frequencies. Transmit spectrum using 1300/2100 Hz, shown with dotted lines, provides 2 to 1 improvement in system performance without any impact on cost. Narrower bandwidth transmitter delivers more energy to receiver with less distortion (no peaks at mark and space frequencies)

ditional bandwidth also increases. Conversely, the modem's S-N performance deteriorates when noise is averaged over the band utilized.

The frequency band used by medium speed modems is restricted to that available on telephone company lines. Such modems can only operate half-duplex, since there is not enough usable bandwidth remaining for another full channel. Over one pair of wires, these modems can either send or receive, but they cannot do both at the same time. Because of the simple, half-duplex modulation, however, 1200-bit/s modems can be manufactured on printed circuit (PC) boards having an area of less than 20 in^2 (129 cm^2) and with power consumption as low as 0.2 W. These modems therefore offer an excellent design compromise in terms of error-free performance, size, and cost for inclusion into compact data processing terminals.

Dial-Up Telephone Networks

Dial-up telephone networks consist of two simplex transmission paths between central offices and a full-duplex transmission path in each subscriber loop (Fig 2). From central office A to central office B, one simplex channel is provided for transmitting and a second channel for receiving. The outbound signal from office A is sent to office B on what is referred to as the transmit pair; from office B the outbound signal is transmitted to office A on the so-called receive pair. Amplifiers in the transmit and receive pairs prohibit 2-way communications in the channel. At the central office, a balancing network combines the full-duplex subscriber loop into transmit and receive pairs. In telephone company terminology, the interexchange system is called a 4-wire line and the subscriber loop, a 2-wire line.

In transmit and receive paths, echo suppressors may be installed to prevent transmission signals from coupling into the other path when no signals are present in the opposite direction. If echo suppressors are present (4-wire leased lines should always be specified without echo suppressors), the answer tone (2025 or 2225 Hz, depending on modem type) is used to disable them for full-duplex operation. Half-duplex modems must delay transmission of data long enough to ensure that the echo suppressor is out of the circuit.

Leased-Line Telephone Networks

The subscriber loop is basically a pair of wires without amplifiers. At the central office, the transmitted signal is sent to the far-end office on a unidirectional channel called the transmit pair. This channel is simplex, 1-way-only due to audio amplifiers. The far-end transmitted signal appears at the near-end of the receive pair. Transmit and receive pairs are referred to by telephone companies as 4-wire lines. Leased circuits can be provided on either a 4- or a 2-wire basis. The latter case involves combining the signals in a 2/4-wire terminating set (see Fig 3).

Leased lines are full-term lines allocated to a single subscriber at a specified conditioning. Since these lines are not switched like dial-up lines, they are available in

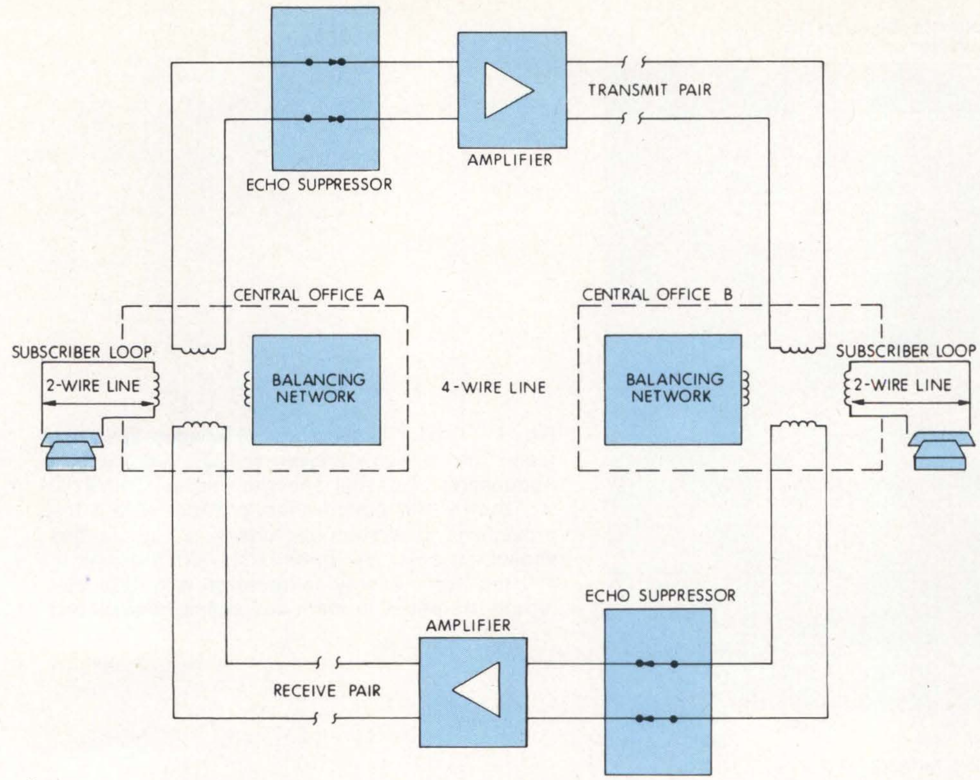


Fig 2 Typical long distance telephone connection. Key parts of dial-up telephone system that are shown have significant effect on data transmission

four conditioned grades from the telephone companies—C1, C2, C4, and D1. Grade C1 is unconditioned, while the others are increasingly tighter specified variations of C1. Conditioning refers to the specified electrical characteristics of voice-grade telephone lines.

Leased-Line Multidrop Networks

A leased-line multidrop (multiterminal) network (Fig 4) for 1200-bit/s custom FSK modems is useful where the central processing unit (CPU) communicates with many modems scattered throughout a large geographical area. This approach minimizes line costs while providing each remote operator with a reasonable approximation of an online interactive environment. Central host site (CPU or concentrator) is connected string-fashion to many remote terminals so that the data path emanates from the central site, goes to the first remote site, then to the second, etc. Properly locating terminal sites on the string permits remote sites to be connected to the central site with a shorter total line length than when separate lines are run to each remote site from the central site. Since telephone companies charge by the wire-mile/month, reduced wire length means lower monthly communications cost. The system operates under central site control with the central site signaling (polling) each remote site in sequence to receive and/or transmit information. Typically, an operator on a polled network will receive a response within 0.1 to 4 s after a request.

Multidrop networks are available in 2- and 4-wire configurations (Fig 5). Two-wire networks require a complicated 2-wire bridge configuration at each drop point. This bridge must generate gain in two directions, because a 2-wire system uses the same pair of wires for both transmitted and received signals at the modem. Four-wire systems have a dedicated pair of wires for transmission in each direction.

Bridge configurations in 2-wire networks are generally useful when the number of drops or terminals is five or less. In larger networks, line impedance-matching problems evolve, oscillations arise on the lines, and the system ceases to function correctly. As a result, 4-wire systems are more common since they require no bi-directional bridge networks and have no oscillation problems, but do permit a large number of drops to be controlled from a single central site.

Polling Sequence

A leased-line multidrop network operates when the central site, made up of computer and modem, sends out a short series of characters—a code referred to as a poll—that uniquely identifies one particular remote site, consisting of modem and associated terminal. The poll sequence is received by the modem and passed to its terminal. In common use is a polling sequence requiring 16 discrete steps.

(1) Host computer raises request to send (RTS)
(2) Mark frequency is transmitted from host modem to remote modem
(3) Remote modem raises carrier detector (CXR)
(4) Host modem raises clear to send (CTS)
(5) Host computer sends poll to host modem on transmit data (TXD) lead

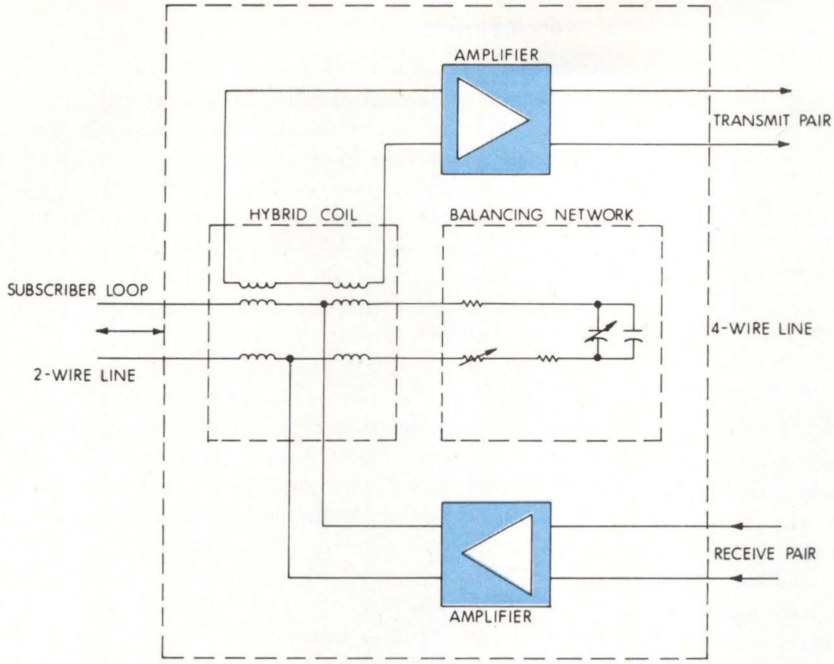


Fig 3 2/4-wire terminating set. Circuits that comprise equipment shown in Fig 2 at central office A and B are shown in greater detail

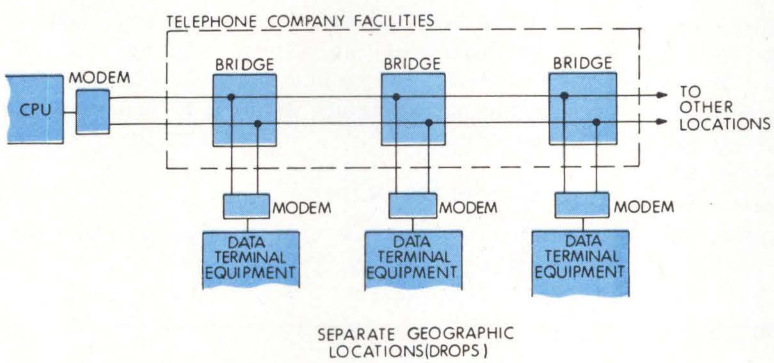


Fig 4 Leased-line multidrop network. Leased-line multidrop network is ideal for large-scale systems where CPU communicates with many modems scattered throughout large geographical area. Data terminal equipment is coupled to main line through modems and bridges

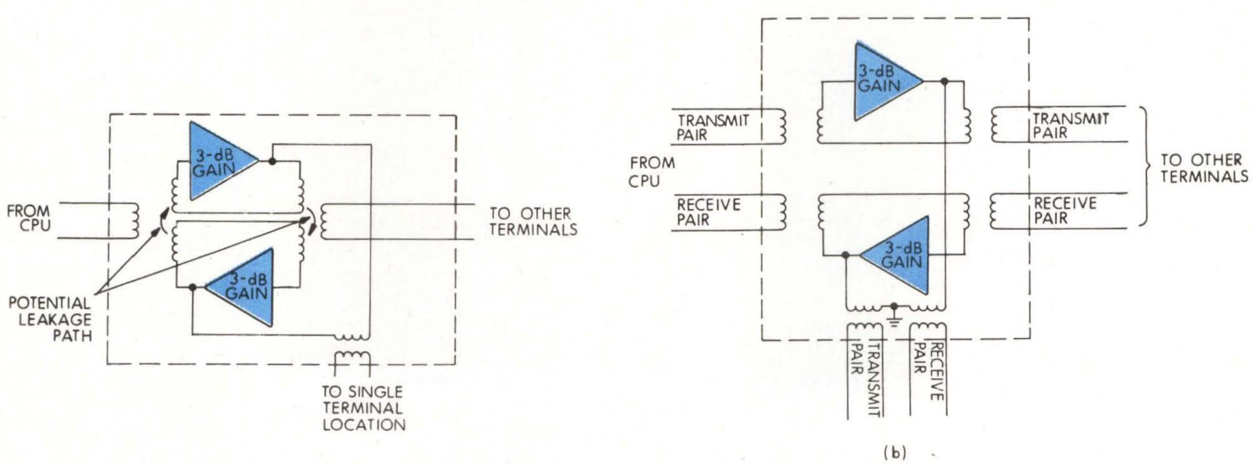


Fig 5 Simplified 2- and 4-wire bridges. 2-wire bridge (a) is used in 2-wire leased-line multidrop network to couple single terminal location to main line. (Bridge circuit is shown in detail in Fig 3.) 4-wire bridge (b) is used in 4-wire leased-line multidrop network where dedicated pair of wires is available for transmission in each direction. Completely separate amplifier is used for each direction, eliminating need for balancing network and its attendant drift problem

(6) Host modem transmits poll on telephone line
(7) Remote modem receives poll and relays it on receive data (RXD) lead to remote terminal (TERM)
(8) Remote terminal receives and decodes poll
(9) Remote terminal raises RTS
(10) Mark frequency is transmitted on line from remote modem to host modem
(11) Host modem raises CXR
(12) Remote modem raises CTS
(13) Remote terminal sends response to poll to remote modem on TXD lead
(14) Remote modem transmits response to poll on telephone line
(15) Host modem receives response to poll and relays it on RXD lead to host computer
(16) Host computer receives response to poll. Then host computer repeats polling sequence

Remote terminal logic decodes and recognizes the preset poll code. If data follow the correct poll code, they are accepted by the remote terminal. If the terminal has data to transmit, these data are passed to the remote modem for transmission to the central (polling) site. If no information is ready, the remote terminal sends a negative acknowledgement, and the central site polls the next remote modem-terminal on its polling list. Exact operation of a polling system is determined by its software and hardware. Therefore, many operating variations are possible in a specific leased-line multidrop network.

Because the central (host) site computer is continually polling remote terminals for messages, line traffic on the system consists of 70 to 80% polls and acknowledgements, with the remainder taken up by message traffic. Thus, whatever time is available for message traffic must be used efficiently. To increase efficiency, dead or inactive time between the beginning of one transmission and the beginning of the next must be minimized.

Poll Timing

Dead time is displayed graphically in Fig 6. In a 4-wire network, the central site always transmits by a continuous carrier signal to all remote modem-terminal sites. Each remote site is then continuously receiving the carrier (no delays are imposed). When a remote site receives its particular poll code, it enters transmit mode. For transmission to begin (data flow), the T1 delay [Request to Send/Clear to Send (RTS/CTS)] must take place to assure that the central-site receiving-end modem has sufficient initializing energy to turn on its carrier detector. In Fig 6, carrier detector and received data signals of the transmitting remote modem are depicted as if the remote modem were receiving its own transmitted signal (local copy). Although this condition is not true in a 4-wire multidrop network, it simplifies the timing diagram. At the end of remote data transmission, a central site receiver-off signal (soft carrier) is turned on for time period T4 to allow the carrier detector sufficient time to turn off (T3). Minimum time delay in a 4-wire multidrop system, before a new poll can be sent, is T1 plus T3. For successful operation of 1200-bit/s modems on leased lines, the fastest T1 time is approximately 10 ms and the minimum T3 time is approximately 5 ms. These two time delays provide a total poll-to-poll delay in this configuration (not counting data) of approximately 15 ms. To improve upon this delay, alternate design approaches are required to better optimize system performance.

Carrier Detector

Carrier detector turn-on time in the central site modem

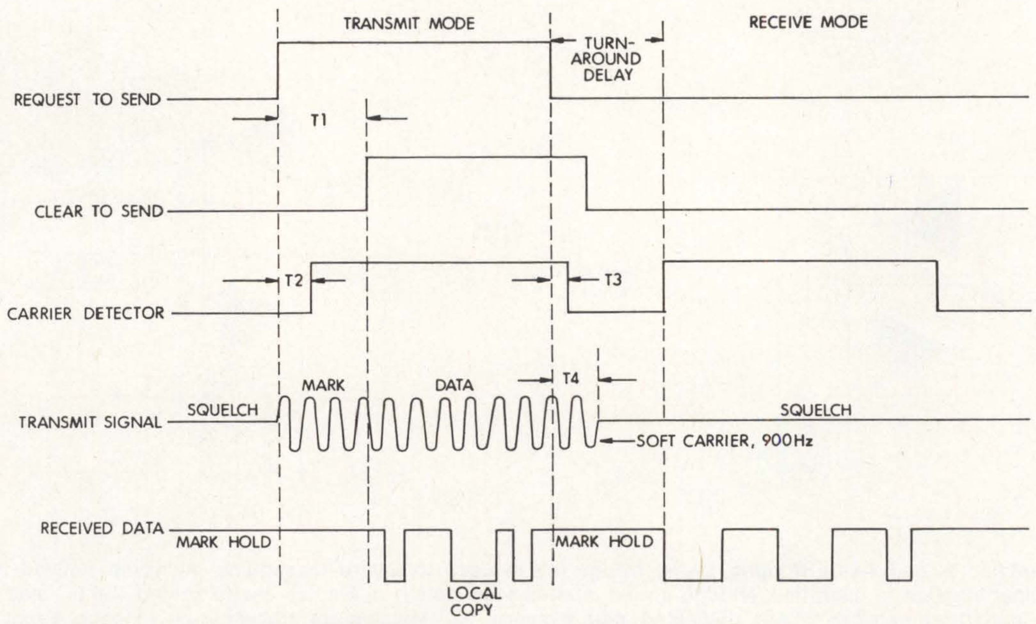


Fig 6 Basic timing diagram. Key interface signals and their interrelationships are shown for single remote modem in 4-wire multidrop network

receiver is a critical component of RTS/CTS delay. In fact, this delay allows the central-site modem receiver sufficient time to sense the incoming signal and to enable its output to the CPU. If this is not done and the modem receiver is always left on, it will sense any stray noise on the line, since receivers have gains of 20 or more. Different carrier detector designs can be used to maximize performance or to minimize cost. In its simplest design, the carrier detector senses energy over time. More complex designs examine the ratio of inband to outband energy or look for mark-only energy as the initiating signal. Other design variations can optimize performance when particular types of line distortions are present.

Leased lines usually have excellent low distortion characteristics, and utilize a simple carrier detector. However, for dial-up lines, a complex carrier detector is necessary to overcome the noise prevalent in a massive, switched, direct distance dialing network.

Soft Carrier

Carrier detector off-time (T3 in Fig 6) is a problem in system operation. Since the communications line tends to ring (damped oscillations) after the remote site transmitted signal has been removed, the central modem receiver is unable to determine the exact instant when the opposite-end remote modem transmitter has turned off. This effect can cause potential delays in carrier signal turn-off. In the worst-case condition, it can prevent the carrier from turning off at all, thereby allowing the CPU to receive erroneous data (line noise). A common technique used to solve carrier turn-off problems is to employ a soft-carrier tone—a 900-Hz signal sent from the remote modem transmitter at the end of a data transmission. When the remote-end transmitter is turned off, the soft-carrier tone is automatically turned on for a short span of time (10 to 25 ms). This signal causes two effects in the central modem receiver: it forces received data signal to mark and causes carrier detector to turn off more rapidly.

In leased-line networks, carrier detector turn-off time can also be minimized by decreasing the sensitivity of the central site modem receiver. This is practical since telephone company leased lines have a maximum signal loss of 18 dBm from end to end.

An alternate approach is transmission of an end of transmission (ETX) code at the end of each transmitted message. When host logic (not part of modem) receives ETX, received data can be gated off for a span of time equal to T4 (Fig 6). This function is more fail-safe than use of a soft-carrier tone and allows better performance than decreasing the host modem receiver sensitivity. In addition, ETX allows time delays to be set via logic circuitry and eliminates time wasted due to carrier detector-off delay. ETX delay is not a part of the poll-to-poll delay, since the time required for noise on the communication line to settle down (T4 or less) will occur while the next poll code is sent from the central site.

Diagnostic Loopbacks

Medium speed modems in 4-wire data communications networks can be checked either at the modem or from the central site computer when problems occur. The technique used for diagnosing problems involves looping signals back toward their origins at various sites in the system. However, this technique works only when the system is capable of full-duplex operation. Since loopbacks of both analog (operating on the analog side of the media) and digital (operating on the modem's digital side) forms can occur either toward or away from the modem, four potential loopbacks exist at each end. Therefore, in any operating communications system with two ends, a total of eight loopbacks are possible (see Table 1).

A multipoint network is usually tested by checking each remote site under control of the central-site computer. Although loopbacks initiated at the test site are simply called loopbacks, those that are initiated over the communications link from another site are called remote loopbacks. Remote loopbacks offer considerable advantages in 4-wire multidrop networks that use 1200-bit/s modems. They allow all diagnostic operations to occur at the remote site without operator intervention. Using loopbacks at both sides of the modem allows any single equipment failure—modem, data terminal, or CPU—or degradation in telephone company facilities to be isolated and identified.

The most extensive backup and diagnostics are required at the central site modem, which communicates with all other modems on each leased line. In this application, a single failure can cause the whole line to suffer an outage. To minimize problems at the central site, backup systems (such as redundant power supplies operating in a standby mode) should be available; extensive diagnostic indicators and loopbacks, as well as test pattern generators, should be provided; patch panels for jumpering over and switching out inoperative modems, ports, and cables may be necessary; and the option of switching to dial backup service when leased lines fail may be provided. Dial backup service can be complicated and expensive, but it may be necessary when outages are intolerable.

Side Channels

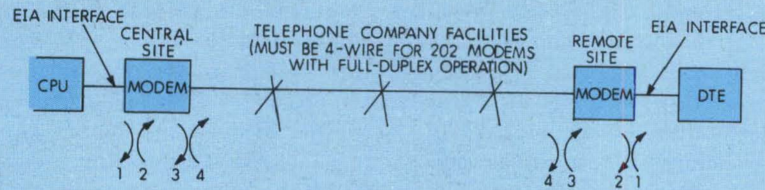
Commands that turn remote loopbacks on and off in a 4-wire leased-line network are often sent over frequency-multiplexed channels that reside on the side of the bands adjacent to the main channel (see Modem Basics), where data are transmitted. Through these side channels pass specifically addressed commands to each remote terminal, much the same as poll commands. Problems encountered with side channels are due to their location within the band, which is the part most likely to be impacted by line distortions, such as phase, frequency, and amplitude distortions. Transmission line changes due to temperature and humidity variations cause further distortion at the upper and lower ends of the band. Thus, with system problems that tend to be the most difficult to troubleshoot, such as increased error rates, side channels tend to fail and the diagnostic mechanism subsequently fails.

In-Band Signals

A better solution makes use of in-band signaling. Certain variations in the standard modem-to-modem handshake (Fig 6) maintain transparency of main chan-

TABLE 1

Diagnostic Loopbacks



Loopback	Function	Comments
CS1	Test CPU	Usually self-contained in CPU
CS2 (digital loopback)	Allows remote site to test through both modems and telephone company facilities	Usually manually initiated at central site to avoid remote sites controlling CPU port utilization
CS3 (analog loopback)	Test CPU and central site modem	If this test operates, problem is in telco facilities or remote site
CS4 (line loopback)	Allows remote site to test through one modem and telco facilities	This test can create ambiguous results. Loopback without signal regeneration effectively sums line distortions in both directions
RS1	Test DTE	Usually self-contained in DTE
RS2 (digital loopback)	Allows central site to test through both modems and remote facilities	May be automatically initiated from central site to allow complete diagnostic control at central site
RS3 (analog loopback)	Test DTE and remote modem	If this test operates, problem is in telco facilities or central site
RS4 (line loopback)	Allows central site to test through one modem and telco facilities	Can be powerful test in multidrop systems, but requires sophisticated central site due to problems of CS4

Note:

CS defines central site loopbacks, while RS defines remote site loopbacks. Loopbacks 1 and 2 occur on the digital side of the modem while loopbacks 3 and 4 occur on the telephone company (analog) side of the modem.

TABLE 2

Microprocessor/Modem Interface Signals and Functions

Modem Function	Signal Direction	Processor Function
Transmit data (TD)	→	Serial Data In
Receive data (RD)	←	Serial Data Out
Carrier detect (CD)	→	Interrupt (set receive data mode)
Test	→	Interrupt (set test mode)
Transmit squelch	←	Control
Remote line loopback (optional)	←	Control

1. Test true and CD true are normal at remote site in constant carrier operation
2. Test true, CD false, and no data on RD indicate modem receiver failure and cause DTE logic to send poll code back to central site through modem transmitter
3. Line Loopback is a confusing test due to the summation of occurring line distortions. However, it can be helpful in diagnosing 4-wire multidrop systems

nel data and, at the same time, allow diagnostic information to be transmitted (eg, carrier detector turn-on handshaking sequence). When a request-to-send at the central site is raised, the central site modem sends mark (data) information; the remote-site carrier detector will turn on only if it receives mark information. The system will not operate if data are not in mark when the carrier detector turns on. Using this protocol, one mechanism for notifying remote modems that they are in test mode is to drop transmit data at the central site and then bring it up with transmit data in space condition. In this way, all remote terminals on the line would be notified that following data are for test purposes only.

This technique also enables easy system recovery if a line failure occurs in the midst of troubleshooting. Turning off the transmit data signal again, and then turning on data in mark condition, resets every remote modem. After the remote site has been put into test mode by the presence of space after carrier detector, the normal carrier detector through the logical interface is turned off, but a special test lead is turned on (Table 2).

If logic in the data terminal equipment is appropriately designed to detect when the test lead is on, the received data coming from the central site modem can be examined by remote terminal logic to decode a poll sequence and determine whether it is the proper poll. If the poll is proper, the three commands after the poll are analyzed to determine what test operation should take place. Test operations include remote analog loopback on the line toward the computer, transmitter squelch to turn off a transmitter that would not otherwise turn off, and remote digital loopback. Using these test commands, any major portion of the remote site and associated lines can be diagnosed successfully. This approach requires little additional logic at the remote site and only minor changes and additions to the remote site modems.

To test telecommunication networks, the central site must include the capability to initiate test commands and controls. In networks where test/maintenance facility has not been incorporated into central site software and hardware, a busing technique through the central site modems can be implemented to control the central modem diagnostics from a separate port that is operated by an intelligent terminal. In this manner, changes are not necessary in central site software. Using this central-site control approach, the logic interface for the remote modem consists of transmit data, receive data, carrier detect, test, transmit squelch, and line loopback (see Table 2). These interface leads can be provided to the remote modem either on Electronic Industries Association, transistor-transistor logic, or complementary metal-oxide semiconductor levels, as required, to minimize the cost of interface-to-terminal logic.

Remote-Site Microprocessor Control

By placing the complete burden for remote site modem and diagnostic control on the logic behind the modem with microprocessor-oriented logic, rather than on the modem itself, this approach can be easily implemented at minimum cost. Logical functions for soft-carrier tone, RTS/CTS delay, and remote-controlled diagnostics are a minimum number of instructions for a microprocessor. The microprocessor interface to the modem described in Table 2 is based on the concept that the only timing inherent in the modem is the carrier-on and -off delay. Request-to-send delay is generated in the terminal (microprocessor) logic. The function-send mark for the appropriate span of time (T1, Fig 6) provides the effect of RTS/CTS delay. Soft-carrier is not needed since the ETX function is utilized instead. The test lead goes true when the modem receives carrier followed by space. The diagnostics transmit squelch (turn-off transmitter) is a control command from the microprocessor.

Remote line loopback is also controlled via the microprocessor, and remote digital loopback is done in the microprocessor by connecting transmit data to receive data. Utilizing this approach, 1200-bit/s modems with extensive diagnostics can be constructed on a 15- to 20-in^2 (97- to 129-cm^2) printed circuit board for less than \$75, in volume. These modems offer expanded diagnostic control and high reliability because of low component count, and run on a wide range of supply voltages.

Summary

Due to users' reliance on telephone company practices, little effort has been made to optimize performance of the data communication system related to modems and telephone company facilities. Specialized common carriers are now offering users optimized data communication line facilities. Specialized modems, such as those examined here, can further increase performance.

Proposed operational changes, such as the use of ETX and inband diagnostic signaling, require implementation at all points in the network. Therefore, they are most easily implemented in systems where a single user has control of the entire network. Leased-line systems are the most common examples. Since these changes require specific hardware and/or software modifications throughout the system, users installing new systems should thoroughly evaluate the overall network implications.

Bibliography

N. Abramson and F. F. Kuo, *Computer-Communication Networks,* Prentice-Hall, 1973

Bell Telephone Laboratories, "Analog Parameters Affecting Voiceband Data Transmission," Bell System Technical Reference, Pub 41008, Oct 1971

Bell Telephone Laboratories, "Data Communications Using the Switched Telecommunications Network," Bell System Technical Reference, Pub 41005, May 1971

Bell Telephone Laboratories, "Data Communications Using Voiceband Private Line Channels," Bell System Technical Reference, Pub 41004, Oct 1973

Bell Telephone Laboratories, "Data Sets 202C and D Interface Specifications," Bell System Technical Reference, Pub 41202, May 1964

Bell Telephone Laboratories, "Data Set 202R Interface Specification," Bell System Technical Reference, Pub 41208, June 1971

Bell Telephone Laboratories, "Data Sets 202S and T Interface Specification," Bell System Technical Reference, Pub 41212, Aug 1974

Bell Telephone Laboratories Technical Staff, "Transmission Systems for Communications," Bell Telephone Laboratories, 1964

J. Martin, *Design of Man-Computer Dialogues,* Prentice-Hall, 1973

J. Martin, *Design of Real Time Computer Systems,* Prentice-Hall, 1967

J. Martin, *Systems Analysis for Data Transmission,* Prentice-Hall, 1972

J. Martin, *Telecommunications and the Computer,* Prentice-Hall, 1976

Schwartz, Bennett, Stein, *Communication Systems and Techniques,* McGraw-Hall, 1966

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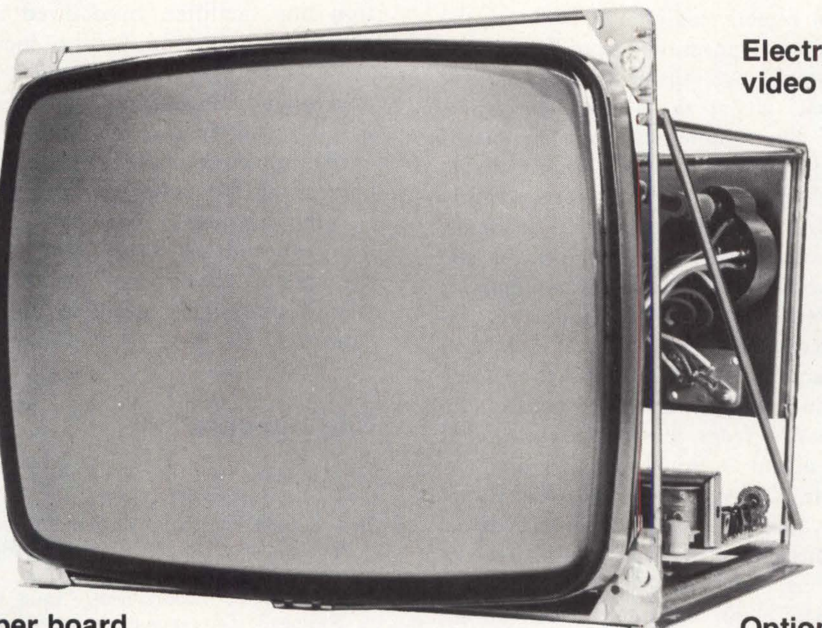

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NUMERICAL INTERPOLATION FOR MICROPROCESSOR-BASED SYSTEMS

A basic mathematical approach to a second-order forward interpolation of function values which lie between tabulated numbers is programmed as a subroutine in order to process data for a microprocessor-based temperature data acquisition system

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Microprocessors programmed for data acquisition and control applications often require computing the value of a function; for example, linearizing thermocouple emf voltages by a calibration curve to derive junction temperatures. While most designers are aware of the programming technique of storing the function as a table of ordinant values in memory, many may not be familiar with the methods of "looking up" specific values and interpolating between entries, except for linear interpolation. One numerical interpolation method is explained with basic mathematics, along with the necessary programming for efficient data processing.

Representation of a function as a table of numbers is an alternative to computing the function, eg, a Taylor series expansion. Indeed, the function may not be available as a Taylor, or any other, series. The brute force method of constructing table stores has a separate entry for every discrete input value. For example, if entries are made for thermocouple linearization every 25 μV for a 50-mV range, the table will have 2000 entries. Furthermore, each entry needs two bytes [the 2500°F (1371°C) output range can be represented by 12 bits, but this is an inconvenient format for a byte-structured memory]. The large table size prompted the investigation of interpolation techniques that would reduce the number of entries by estimating the function value between them.

The need for a table lookup procedure arose during the design of an automatic data acquisition system for a materials research experiment.[1] Originally, data were recorded on strip charts in millivolts and manually converted to temperature. This step was replaced by software that looked up the temperature from a table stored in programmable read-only memory (p/ROM). The table was accurate to ±4°F (±2°C) and contained 600 entries. Later, the system was upgraded and the precision improved to ±1°F (±0.56°C). A table using the same technique now would require 2400 entries—an excessive amount of memory. Instead, a table with fewer entries is used and interpolation between entries extends the table's resolution. Finally, temperature feedback control was added to the system, requiring a conversion from Fahrenheit temperature to thermocouple emf, with a second table making the reverse conversion with the same interpolation software.

Mathematical Approach

Linear interpolation approximates the function with a first-order (linear) polynomial.[2] The value of $f(x)$ between two known points, $f(x_1)$ and $f(x_2)$, is estimated to be

$$f(x) = f(x_1) + (x - x_1)\frac{f(x_2) - f(x_1)}{x_2 - x_1}$$

This computation can be simplified by making table entries at constant intervals, $\Delta x = x_{n+1} - x_n$. While this appears to eliminate only one subtraction, Δx and $1/\Delta x$ are constants. If Δx is a power of two, division can be performed as an arithmetic shift, which enables a significant reduction in data processing.

Selection of the number of table entries (or, indirectly, Δx) is a tradeoff between the number of bytes and the worst case error. Fig 1(a) illustrates the error resulting from a linear approximation of a plotted curve. Spacing the plotted points closer together reduces the error, but also requires more points and, hence, more memory. Maximum error for one segment of the curve is illustrated in Fig 1(b). The problem encountered is how to determine the worst case error for any input. If the curve can be described as a finite or infinite series, the error can be bounded analytically. The error function for linear interpolation is

$$E(x) = \tfrac{1}{2} f^{(2)}(\xi)\, \pi(x) \quad (1)$$

where

$f^{(2)}$ = second derivative of the function being interpolated

ξ = any argument in the interval being interpolated

$\pi(x) = (x - x_i)(x - x_{i+1})$,

where i depends upon which interval ξ is in.

For example, suppose sine x is represented for the interval of 0 to $\pi/2$ with 17 points; therefore,

$f^{(2)}(x) = -\sin(x)$, for $0 < \xi < \pi/2$

Obviously, sine x is maximum for $\xi = \pi/2$, which is the last interval (i = 15)

$$x_{15} = \frac{\pi}{2} \cdot \frac{15}{16} = 1.47262; \; x_{16} = \frac{\pi}{2} = 1.57080$$

Thus,

$$E(x) = \tfrac{1}{2}\left[-\sin\frac{\pi}{2}\right](x - 1.47262)(x - 1.57080)$$

$$E(x) = -0.5(x - 1.47262)(x - 1.57080) \quad (2)$$

Examining E(x) reveals that the error, through the interval, varies from zero at the data points to a maximum midway between the x_{15} and x_{16} data points at x = 1.52171. Computing the error yields

$$E(x) = -0.5(1.52171 - 1.47262)(1.52171 - 1.57080) = 0.0012$$

This result indicates that the approximation approach is accurate to three digits, or about 0.1% (presuming no computation errors). If an approximation must be accurate to eight bits, linear interpolation will be more than adequate. However, if the arithmetic used in the computation is also eight bits, truncation errors will swallow the error budget. Another observation is that the greatest error is close to $\pi/2$, where sine x is changing the slowest. The assumption might be that the error would be greatest near zero where sine x is changing rapidly. In fact, the error in the first interval is less than 0.0006, about one-half the last interval error, because error is a function of the rate of change (the first derivative). Linear approximation contains a factor for the first derivative, but not the second, which is maximum at $x = \pi/2$.

Error has been computed as a function of the data spacing or interval. It is also useful to compute the interval required for a given error:

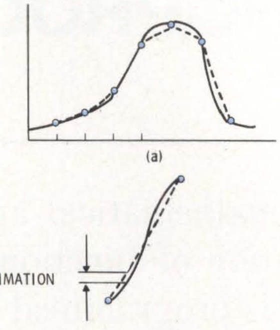

Fig 1 Linear approximation of plotted curve. Arbitrary curve (solid line) is approximated by discrete points and linear interpolation between points (a). Enlargement of one segment (b) identifies maximum error due to approximation

$$E(x) = \tfrac{1}{2} f^{(2)}(\xi)(x - x_i)(x - x_{i+1})$$

$$= \tfrac{1}{2} f^{(2)}(\xi)(h/2)(-h/2)$$

$$E(x) = -\tfrac{1}{8} h^2 f^{(2)}(\xi),$$

$$\text{where } h^2 = -\frac{8\,E(x)}{f^{(2)}(\xi)} \quad (3)$$

Consider again the sine x table where the error is adequate for 12 bits, or 0.00025. Using 0.00025 for E(x),

$$h^2 = -\frac{8(0.00025)}{-\sin\left[\frac{\pi}{2}\right]} = 0.002,$$

and h = 0.0447

To find the number of data points required, h is divided into the range, $\pi/2$; thus, in this case, 36 points are required. By slightly more than doubling the number of data points, error is reduced by a factor of greater than four. Also, E(x) is proportional to h^2, or inversely proportional to the number of data points squared. Error can be further reduced by using higher order interpolation methods.

Higher Order Interpolation

Linear interpolation causes errors by ignoring the derivatives of the function past the first. Second-order interpolation approximates the function with a quadratic; thus, better performance is expected (but not without more computations, unfortunately). Until now, it has been assumed that data points are spaced at constant intervals; hereafter, only constant spacing will be considered. It has been shown that constant spacing

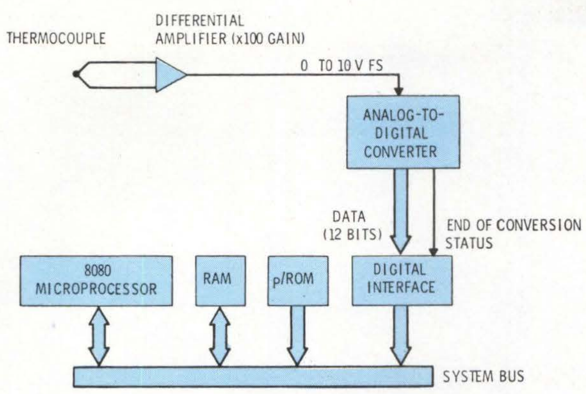

Fig 2 Design application. Temperature data acquisition system based on 8080 microprocessor amplifies low level thermocouple signals for A-D conversion. System accuracy of 12 bits results in temperature measurement errors of less than ±1°F (±0.56°C) for Chromel-Alumel thermocouples

simplifies arithmetic. With higher order interpolation, it is essential to have short computation times. Storage requirements also are cut in half because x is implied by the position in the table; otherwise, it would have to be stored as well. Uneven spacings are justified only when data points can be concentrated at places of greatest error, and spaced farther apart when the approximation is accurate. In this situation, a better solution is to break the function into more than one table.

The general class of interpolation formulas using constant differences is termed "finite difference interpolation." Notation in the formulas uses the Δ (delta) operator, defined as

$$\Delta f(x_i) = f(x_i + h) - f(x_i) \tag{4}$$

also written as Δf_i. Second differences are defined as

$$\Delta^2 f_i = \Delta f_{i+1} - \Delta f_i, \tag{5}$$

and in general,

$$\Delta^{k+1} f_i = \Delta^k f_{i+1} - \Delta^k f_i \tag{6}$$

Three types of interpolation formulas considered are forward, backward, and central, referring to the relative position of the interpolation point and entries in the table. All formulas require the nearest two data points. A second-order forward interpolation would require a third data point forward of the other two. The significance of the different types is the area in the table in which the interpolation is taking place; a forward formula is used near the start of the table, backward near the end, and central anywhere else. A typical formula is Newton's forward difference formula:

$$f(x) = f_i + (x - x_i)\frac{\Delta f_i}{h} + (x - x_i)(x - x_{i+1})\frac{\Delta^2 f_i}{2h^2} \ldots + (x - x_i)(x - x_{i+1}) \ldots (x - x_{i+n-1})\frac{\Delta^n f_i}{n!h^n} \tag{7}$$

where $x_i < x < x_{i+1}$

Using only the first two terms of Eq (7) results in the linear form described earlier. A second-order interpolation formula uses the third term as well; an interpolation formula of order n uses n + 1 terms.

As an example of the use of the second-order form, Table 1 lists the last two entries of the 17-entry sine x table, plus one additional data point required by the forward interpolation formula; also included are the first and second differences. Substituting these values into Eq (7) and interpolating to the midway point,

$$f(1.52171) = 0.99518 + (1.52171 - 1.47262)\left[\frac{0.004815}{0.098175}\right] + (1.52171 - 1.47262)(1.52171 - 1.57080)\left[\frac{-0.009631}{2 \cdot 0.098175^2}\right]$$

$$f(1.52171) = 0.99518 + 0.00240762 + 0.0012039 = 0.9987915;\ \text{Error} = -0.000004$$

By including just one more term, the error drops dramatically from 0.0012 to −0.000004, an improvement factor of 3000. Remember that all computations are performed to at least six decimal places, which requires floating-point arithmetic. The same computations can be performed as 16-bit fixed-point arithmetic, yielding accuracies of about four digits in much less time.

Interpolation Subroutine

These basic interpolation formulas can be implemented in a subroutine for a widely used microprocessor, the 8080. The first decision is to choose which formula to use, the number of terms (order), and the data format. The design application studied required a minimum 12-bit accuracy; therefore, a 16-bit integer format and second-order interpolation formula were selected. Interpolation was not necessary near the end of the table, but was necessary near the beginning, pointing to a forward formula. Newton's forward difference formula [Eq (6)] proved to be satisfactory.

Fig 2 is a simplified diagram of the temperature data acquisition system. Low level thermocouple outputs are amplified by 100 and converted by a unipolar converter with a 10-V full scale range and a binary output suitable

TABLE 1

Use of Second-Order Form

x	f(x)	Δf	$\Delta^2 f$
1.47262	0.99518		
		0.004815	
1.57080	1		−0.009631
		−0.004815	
1.66897	0.99518		

Microprocessor Interpolation Subroutine Listing

```
;-----------------------------------------------
;
; COMPUTE NEWTON'S FORWARD INTERPOLATION
;
; F(X) = F(0) + (X-X(0))*DL0/H + (X-X(0))*(X-X(1))*DL20/(2*H**2)
;        (H = 1/64)
;
; ENTER--
;       D,E     POINTER TO FUNCTION TABLE
;       H,L     RIGHT JUSTIFIED DATA
;
; RETURN--
;       H,L     INTERPOLATED FUNCTION
;
;-----------------------------------------------
HEXP=6                  ; EXPONENT OF ABCISSA SPACING
MASK=77                 ; 2**H - 1
LOOKUP: PUSH    D       ; SAVE TABLE BASE ADDRESS
        SHLD    X       ; SAVE DATA
; THE ABCISSA SPACING IS A POWER OF 2.
; THE INTERVAL WHICH X FALLS IN CAN BE FOUND BY
;  DIVIDING X BY THE ABCISSA SPACING,
;  OR SHIFTING BY THE EXPONENT OF THE SPACING
        MVI     B,HEXP  ; USE MSB'S AS INDEX
        LXI     D,0
        CALL    ARS32
; INDEX IS MULTIPLIED BY 2 FOR ADDRESSING A
;  DOUBLE PRECISION TABLE
        DAD     H       ; H,L = H,L*2
        POP     D
; TABLE POINTER = TABLE BASE ADDRESS + INDEX
        DAD     D
; FIND F(0) AND F(1)
;
        MOV     E,M     ; GET F(0)--  2 CONSECUTIVE BYTES
        INX     H       ; D,E REGISTER PAIR = F(0)
        MOV     D,M
        INX     H
        MOV     C,M     ; GET F(1)
        INX     H       ; B,C REGISTER PAIR = F(1)
        MOV     B,M
        INX     H
; SAVE TABLE POINTER
        PUSH    H
        XCHG
; OUTPUT RESULT IS INITIALIZED TO THE FIRST TERM OF FORMULA
        SHLD    FX      ; INITIALIZE RESULT=F(0)
; COMPUTE FIRST DIFFERENCES (DL0 AND DL1)
        XCHG            ; D,E = F(0)
        MOV     L,C     ; H,L = F(1)
        MOV     H,B
        CALL    DCMPD   ; F(0) = -F(0)
        DAD     D       ; H,L=F(1)-F(0)
        SHLD    DL0     ; SAVE 1ST DIFFERENCE
; UNSTACK TABLE POINTER
        POP     H
        MOV     E,C
        MOV     D,B     ; D,E = F(1)
        MOV     C,M     ; H,L = F(2)
        INX     H
        MOV     H,M
        MOV     L,C
        CALL    DCMPD   ; D,E = -F(1)
        DAD     D       ; H,L=F(2)-F(1)
        SHLD    DL1     ; SAVE 1ST DIFFERENCE
; COMPUTE SECOND DIFFERENCE (DL1 - DL0)
        XCHG
        LHLD    DL0
        XCHG            ; H,L = DL1
        CALL    DCMPD   ; D,E = -DL0
        DAD     D       ; H,L=DL1-DL0
        SHLD    DL20    ; SAVE 2ND DIFFERENCE
; COMPUTE SECOND TERM OF FORMULA-- (X-X(0)*DL0/H
        LHLD    X       ; GET X
        MOV     A,L     ; X-X(0) IS CALCULATED BY STRIPPING THE
        ANI     MASK    ;  MOST SIG. BITS (VALID BECAUSE THE
        MOV     E,A     ;  ABCISSA SPACING IS A POWER OF 2)
        MVI     D,0     ; D,E=(X-X(0))
        LHLD    DL0
        CALL    DMULR   ; (X-X(0))*DL0
; DIVISION BY H DONE WITH RIGHT SHIFT
        MVI     B,HEXP
        CALL    ARS32   ; H,L=(X-X(0))*DL0/H
; FX = FX + SECOND TERM
        XCHG
        LHLD    FX      ; ACCUMULATE TERMS
        DAD     D
        SHLD    FX
;-----------------------------------------------
; IF ONLY LINEAR INTERPOLATION IS NECESSARY THE SUBROUTINE
;  MAY BE EXITED HERE (INSERT 'RET' INSTRUCTION)
;-----------------------------------------------
; COMPUTE THIRD TERM OF FORMULA
        LHLD    X
        MOV     A,L
        ANI     <377-MASK> ; X-X(1) COMPUTED BY STRIPPING LOW
        MOV     E,A     ;  ORDER BITS
        MVI     D,377   ; D,E=(X-X(1))
        LHLD    DL20
        CALL    DMULR   ; H,L = (X-X(1))*DL20
        XCHG
        LHLD    X
        MOV     A,L
        ANI     MASK
        MOV     L,A
        MVI     H,0     ; H,L=(X-X(0))
        CALL    DMULR   ; H,L = (X-X(0))*(X-X(1))*DL20
        MVI     B,<HEXP*2+1>
        CALL    ARS32   ; H,L=H,L/(2*H**2)
        LHLD    FX      ; ACCUMULATE LAST TERM
        DAD     D
        RET

;-----------------------------------------------
; 16 X 16 SIGNED MULTIPLICATION (32 BIT RESULT)
;
; ENTRY: D,E    MULTIPLICAND
;        H,L    MULTIPLIER
; RETURN: D,E,H,L       PRODUCT
;-----------------------------------------------
DMULR:  (REFER TO INTEL USER'S LIBRARY FOR A
         DOUBLE PRECISION MULTIPLY SUBROUTINE)

;-----------------------------------------------
;
;       32 BIT RIGHT SHIFT
;
;       D,E,H,L = (D,E,H,L)*2
;       B       SHIFT COUNT
;-----------------------------------------------
ARS32:  MOV     A,D
        RAL             ; SET CARRY=SIGN
        MOV     A,D
        RAR
        MOV     D,A
        MOV     A,E
        RAR
        MOV     E,A
        MOV     A,H
        RAR
        MOV     H,A
        MOV     A,L
        RAR
        MOV     L,A
        DCR     B
        JNZ     ARS32
        RET

;-----------------------------------------------
;
; 2'S COMPLEMENT D,E (STATUS UNCHANGED)
;
;-----------------------------------------------
DCMPD:  MOV     A,D
        CMA
        MOV     D,A
        MOV     A,E
        CMA
        MOV     E,A
        INX     D
        RET

;-----------------------------------------------
;       INTERPOLATION SUBROUTINE VARIABLES
;-----------------------------------------------
X:      .BLKB 2         ; INTERPOLATION INDEPENDENT VARIABLE
FX:     .BLKB 2         ;       OUTPUT RESULT
DL0:    .BLKB 2         ;       1ST DIFFERENCE
DL1:    .BLKB 2         ;       1ST DIFFERENCE
DL20:   .BLKB 2         ;       2ND DIFFERENCE
;-----------------------------------------------
```

for use by a 12-bit analog-to-digital converter (ADC). Data are transferred from the ADC to the microprocessor in two bytes, as follow:

```
Byte 1          8 7 6 5 4 3 2 1
                ↑             ↑
              Bit 8         Bit 1
                            (LSB)

Byte 2          0 0 0 0|12 11 10 9
                        ↑
                      Bit 12
                      (MSB)
```

A representative selection of the 4096 possible converted binary output values, as well as thermocouple input and intermediate amplified voltages, is summarized in Table 2. The least significant bit (LSB) has a weight (or conversion constant) of 0.0244 mV, the first entry in Table 2. Other entries tabulate the weights of other bits, which are important in relating millivolt levels to binary values.

The 4096 range of 12 bits is divided into 64 data points with a constant spacing of 64. Note that in Table 2

TABLE 2

Summary of Converted Binary Output Values

Thermocouple Input (mV)	Amplified Input (V)	Converted Output (Binary)
0.0244	0.00244	1
0.0488	0.00488	10
0.0977	0.00977	100
0.1953	0.01953	1000
0.3906	0.03906	10000
0.7813	0.07813	100000
1.5625	0.15625	1000000
3.125	0.31250	10000000
6.25	0.62500	100000000
12.5	1.25000	1000000000
25.0	2.50000	10000000000
50.0	5.0000	100000000000
75.0	7.5000	110000000000
99.976	9.9976	111111111111

the millivolt values have been scaled to integer values by virtue of amplification and the scale factor of the ADC. Of course, a table of data points will have to be constructed, and knowledge of the conversion constant is a must. Data point spacing of 64, in this application, translates to 1.5616 mV (0.0244 mV x 64). Interpolation table values are determined by looking up the Fahrenheit equivalents for the thermocouple outputs in a National Bureau of Standards conversion table, in this case for Chromel-Alumel (ANSI Symbol K) thermocouples. As type K thermocouples have an output limited to 52 mV, only 35 entries are needed in the interpolation table (52 mV/1.5616 mV $< 35 - 1$).

Suitable means for passing arguments to and from the interpolation subroutine and for processing data within the subroutine are defined in the next subroutine design step. Register pairs in the 8080 microprocessor are used for argument passing as follows.

Input

D,E Pointer to interpolation table

H,L Interpolation point (x)

Output

H,L Interpolated values [f(x)]

Fig 3 illustrates usage of internal registers for argument passing. The 8080 uses pairs of 8-bit registers for memory addressing and 16-bit arithmetic operations. Two pairs are used to "feed" the interpolation subroutine 12-bit input data and 16-bit starting address of the interpolation table. When the subroutine completes the interpolation computation, the result is stored in registers H and L. This selection makes the subroutine general-purpose, and the user can have any number of interpolation tables.

Data are processed by the following steps (Fig 4) with respect to Eq (7).

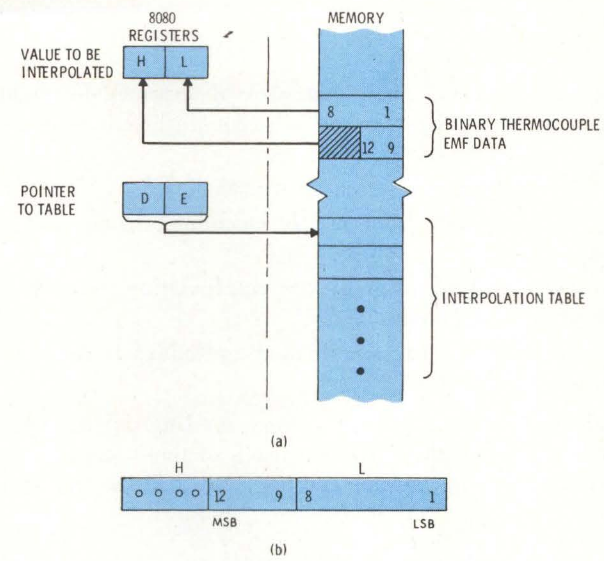

Fig 3 Argument passing in internal registers. Data are transferred to and from interpolation subroutine using four 8080 registers. Before calling subroutine, value to be interpolated is loaded into H and L, and address of start of interpolation table into D and E (a). Interpolated value (temperature) is in H and L when subroutine returns (b)

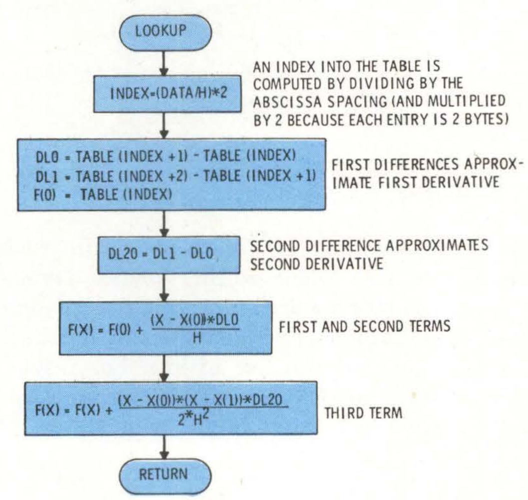

Fig 4 Interpolation subroutine. Flowchart shows sequence of computations. Code is strictly computational—no decisions are made in subroutine

(1) The interval (table entry) is determined by dividing x by h (division by 64 is accomplished by shifting right six places).

(2) The two first differences are calculated.

(3) The second difference is calculated from the two first differences.

(4) The second term of the interpolation formula is computed and added to f(0).

(5) The third term is computed and added to the intermediate result.

Comments in the 8080 Microprocessor Interpolation Subroutine Listing identify where each of these steps is performed. Formula parameters are labeled in the listing as

Parameter	Listing	Comment
x	X	Independent variable x
$f(x)$	FX	Interpolated value as a function of x
$\Delta(f_0)$	DL0	First difference at point 0 $[f(x_{i+1}) - f(x_i)]$
$\Delta(f_1)$	DL1	First difference at point 1 $[f(x_{i+2}) - f(x_i)]$
$\Delta^2(f_0)$	DL20	Second difference at point 0 $[\Delta(f_1) - \Delta(f_0)]$

The subroutine is easily modified to accommodate linear interpolation. Comments in the listing indicate where to insert an RET instruction if only linear interpolation is required (step 5 is omitted). This will approximately double the computation speed.

The routines used by the interpolation subroutine (see Listing) are

ARS32 — Contents registers D, E, H, and L are shifted right by the count in B. If sign bit is set, ones are shifted into most significant bits (MSBS).

DCMPD — Register pair D,E is negated as a 16-bit number.

DMULR — Register pair D,E is multiplied by register pair H,L using 16-bit signed format. The 32-bit signed result is stored in registers D, E, H, and L.

Average computation time of the interpolation subroutine is 5 ms with a 2-MHz clock.

Data Scaling

As noted, theoretical error limits of an interpolation formula may not be achieved in practice because of truncation errors that result from trying to represent real numbers—data represented in computers by floating-point notation—with a finite number of bits. For instance, if a number format stored in memory is integer, any fractional information is lost. Thus, the computation

$$1 + \frac{2}{4} + \frac{2}{4} = 1$$

yields an erroneous result. Yet, the order of the computation can be rearranged to

$$1 + \frac{2 + 2}{4} = 1 + \frac{4}{4} = 2$$

and will produce a correct result since no fractional information was lost due to truncation. If an order of magnitude, or more, in speed can be sacrificed, floating-point arithmetic can greatly reduce, and possibly eliminate, the truncation problem.

An alternative to floating-point arithmetic scales the integer number to include both integer and fractional data. One format for an 8-bit number might be

7 6 5 4 3 2 1 0

• ↖ Binary point

This format allows representation of numbers to the nearest 1/8, but limits the magnitude to 31 7/8 (15 7/8 for signed numbers). This same concept can be applied to double-precision (16-bit) integers. Only the integer part of the interpolation is needed, but scaling reduces errors due to truncation because intermediate results maintain a fractional part.

Summary

Numerical interpolation is useful in applications other than scientific computation. Computations to near 16-bit accuracy can be performed easily with an 8080 microprocessor, without paying a speed penalty of series expansion and floating-point arithmetic (some functions may not be available as a series expansion, eg, thermocouple linearization). Furthermore, computation time can be halved at a small decrease in accuracy by computing only the first two terms of the interpolation formula (linear interpolation). Other interpolation formulas are available (eg, cubic spline) for use with certain types of data.

References

1. T. A. Seim, "Microprocessors Aid Experimentation in Scientific Laboratory," *Computer Design*, Sept 1976, pp 83-89
2. F. B. Hildebrand, *Introduction to Numerical Analysis*, McGraw-Hill, New York, 1956

Acknowledgement

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Thomas Seim is a development engineer in computers and information systems with Battelle-Northwest Laboratory. His interests involve sampled data control systems and information networks applied to mini and microcomputers. He has received BS degrees from Oregon State University and an MSEE degree from Washington State University.

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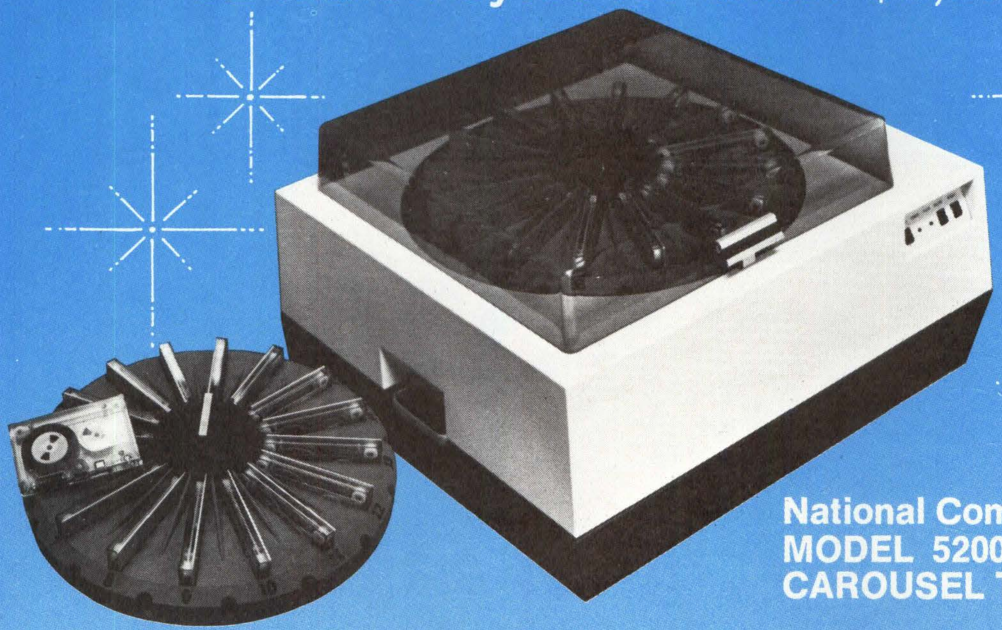

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APPLICATION NOTE

Small Stepping Motors Meet Varied Application Requirements

Advanced motor designs and solid-state driver circuits have made small, permanent-magnet stepping motors affordable for solving performance, complexity, and packaging problems in widely diverse digital drive and positional applications

William Riggs North American Philips Controls Corporation, Cheshire, Connecticut

Small, permanent-magnet stepping motors are achieving substantial usage in differing digital equipment applications, such as desk calculators, chart recorders, terminal printers, and floppy disc drives, where digital control signals are readily available. These motors offer an inexpensive, small, and highly reliable method for providing adjustable speed at low torque levels. In equipment applications where the cost-competitive factor is crucial, a small permanent-magnet stepping motor costs less than $3 in large quantities, and the solid-state step-drive logic package is less than $5. Positional and drive alternatives—all higher priced and less versatile—include synchronous motors with gear changers, dc drives, frequency-controlled ac motors, and solenoid and ratchet drives.

Stepping motor application advantages include: a wide range of low torque levels—from 0.20 to 25 oz-in (0.0014 to 0.175 N•m) without gearing, small step angle for accurate step resolution, and simplicity of design for light weight, ruggedness, and long-term reliability. The permanent magnet rotor provides damping for minimizing overshoot. The motors accommodate light, medium, and heavy industrial-type duty cycles. Other characteristics are low internal temperature rise—no cooling fans, fins, or similar devices are needed; detent torque action, which holds rotor in equilibrium position when power is interrupted; step-angle tolerance of ±10%, which is noncumulative due to symmetrical construction and magnetic pole averaging; and small size—from 0.75 to 2.75 in (19.1 to 69.9 mm) in diameter for saving space.

Stepping Motor Characteristics

Basically, a permanent-magnet type of stepping motor comprises a movable rotor within a fixed stator (Fig 1). The cylinder-shaped stator contains a preset number of electromagnetic poles distributed around the circumference; each pole piece has lengthwise, teeth-shaped members for flux distribution. The permanent magnet rotor is also cylindrical with multiple poles and an extended drive shaft. Interactions between the magnetomotive forces, generated by the applied current to the stator windings, and the rotor magnetic biasing flux cause motor operation. By furnishing a predetermined sequence of stator winding current pulses, a series of discrete rotor rotations is accomplished (Fig 2).

If a field is set up in both stator halves, the rotor poles are attracted by opposite poles of both stators. In this stationary position, the force on the rotor is called the holding torque. If the field direction in one of the stators is reversed by switch A or B, the pole of the stator concerned changes polarity. The rotor takes a step in a direction depending upon which switch is operated.

Stepping motors operate well in an open-loop configuration—no feedback

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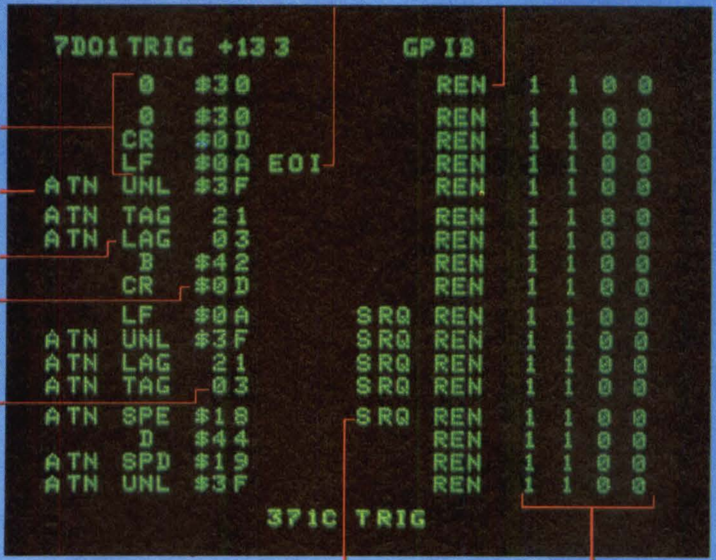

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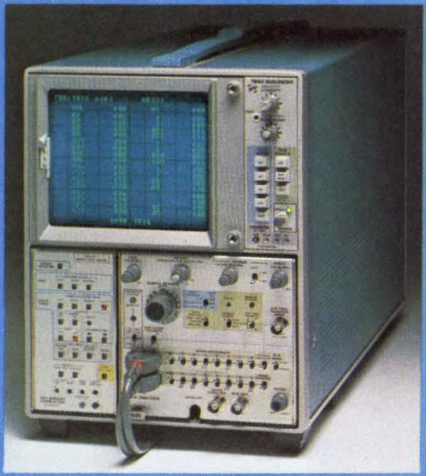

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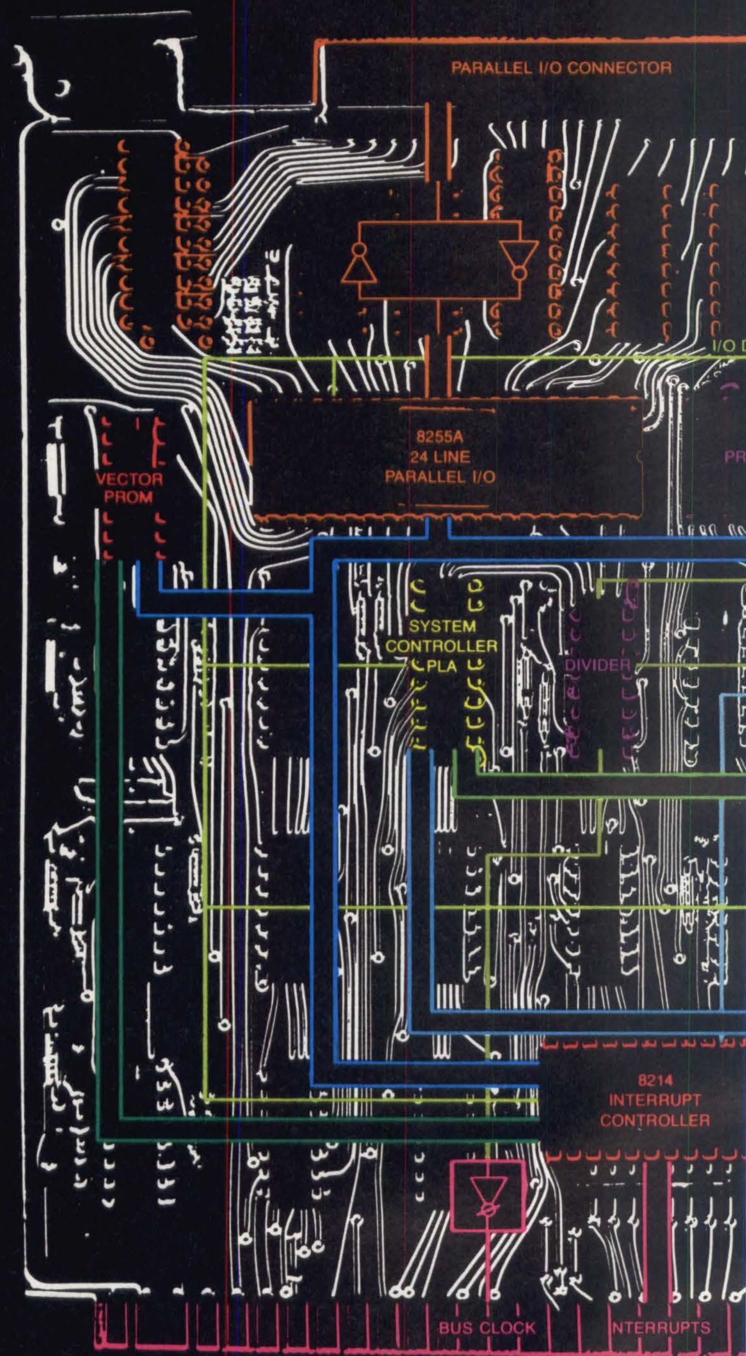

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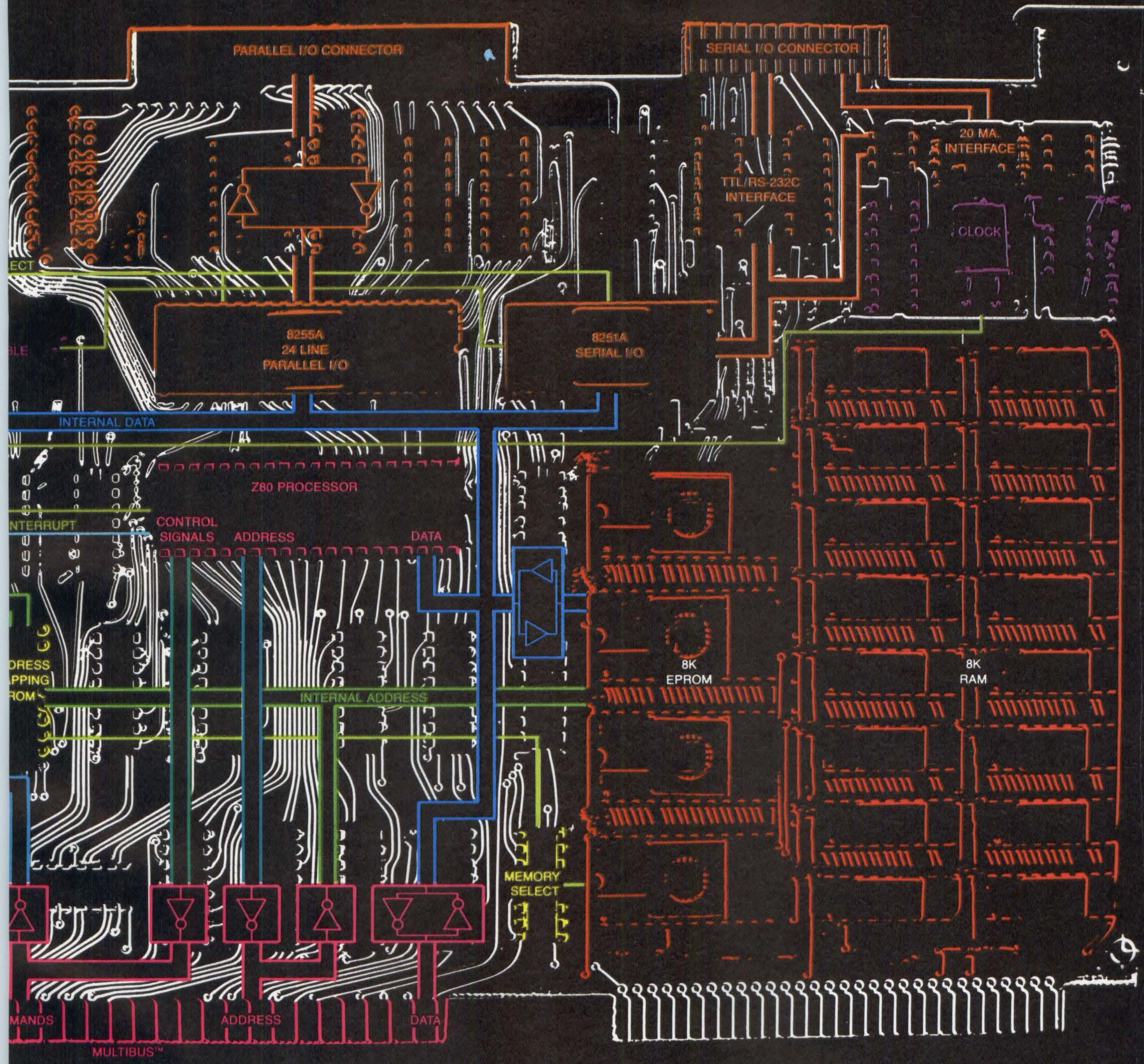
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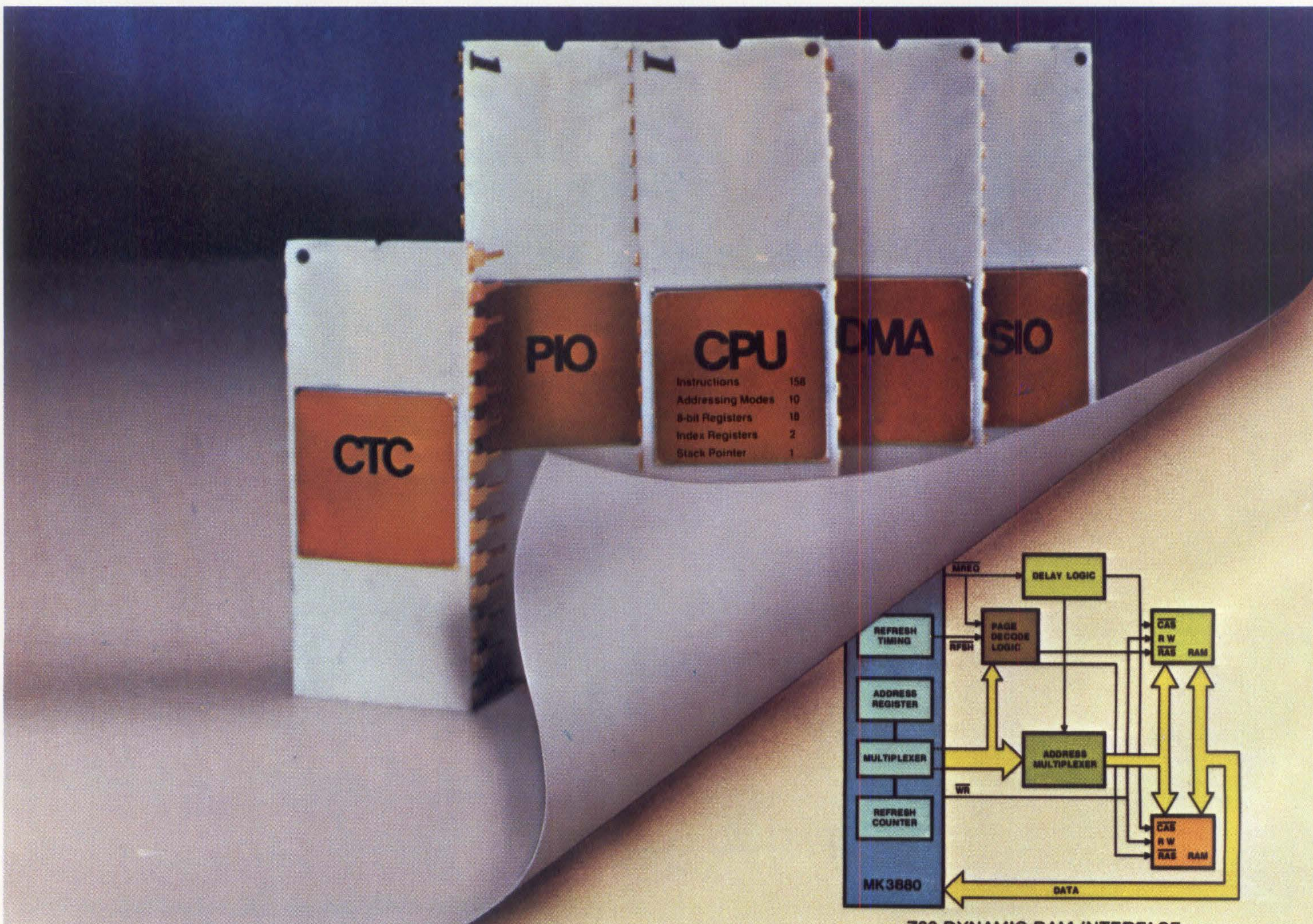

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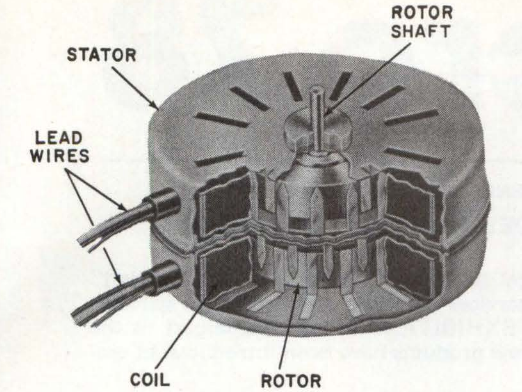


Fig 1 Cutaway view of small, 4-phase, permanent-magnet stepping motor showing major parts

control is necessary—unlike dc motors and other nonstepping types that require optical encoders or other feedback elements to monitor speed and position. Another stepper property is low average power consumption; some applications need less than 200 mW, making stepping motors useful in portable instruments. Steppers can operate from batteries and line power, and in some applications can easily switch from line power to batteries during power failure.

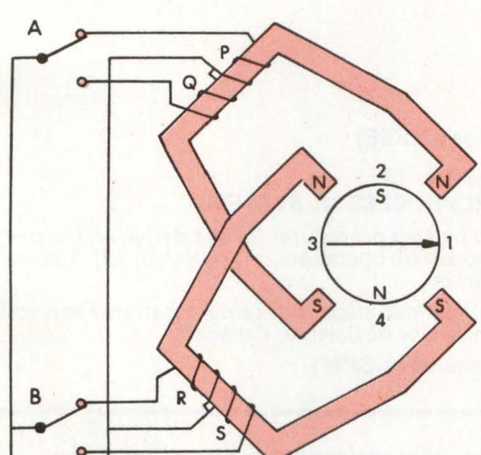
Where quiet operation is essential, the stepping motor is ideal because it does not make the "clunk" sounds associated with solenoids and ratchet drives. Nor is brush life a problem, as it is with dc motors. Also, gears, ratchets, and commutated motors have parts that wear and create noise. Performance life in steppers is limited by bearing wear, which should outlast the application. Although frequency-controlled ac drives can operate as reliably and quietly as steppers, they are less versatile and more costly. Solenoid-operated ratchets resemble steppers in function, but are monotonously noisy and do not have the speed range.

Mechanical construction of small stepping motors accounts for their low cost. The coil is bobbin-wound, the magnetic circuit drawn sheet steel, and the rotor a ferrite magnet, all of which contain no critical materials. These stepping motors have a step accuracy of 10%, which is noncumulative and tolerable for most applications. Logic-driven steppers can operate directly from solid-state 5-V logic, or they can be supplied for operation at other voltages, such as 12 Vdc.

Equipment Applications

Following are typical equipment applications that have incorporated small stepping motors.

Desk Calculators—Because of their quiet operation and small size, steppers serve well as paper feed drives in these calculators. Low power drain also allows the use of batteries.



PHASES ENERGIZED	RESULTANT ROTOR STEP POSITION	ROTOR DIRECTION	
P, R	1	COUNTERCLOCKWISE ↓	CLOCKWISE ↑
R, Q	2		
Q, S	3		
S, P	4		

DIAGRAMMATIC REPRESENTATION OF A 4-PHASE 2-POLE MOTOR.
THE DIRECTION OF ROTATION CAN BE REVERSED AT ANY POINT.

Fig 2 High speed permanent-magnet stepping motors, in general, have four stator phases. For simplicity, rotor is shown as a 2-pole magnet with mechanical switching; however, solid-state switching dominates present designs. Switching A from P to Q reverses magnetic field developed in stator PQ. Resultant change in magnetic field causes rotor to take a 90-deg counterclockwise (CCW) step from position 1 to 2. Switching B from R to S causes 90-deg CCW step to position 3, switching A back to P causes another 90-deg CCW step, and switching B back to R returns rotor to original starting position. Reversed switching sequence, starting with B then going to A, causes clockwise stepping movement

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COURSE OUTLINE:

1. Reminder on current minicomputer characteristics and capabilities.
2. Review of microcomputer hardware and software.
3. The software development process.
4. Development of the hardware system.
5. Hardware, software tradeoffs.
6. Interfacing.
7. System Specification.
8. Some Development Case Studies.

Sponsor: The Institute of Electrical and Electronics Engineers (IEEE)

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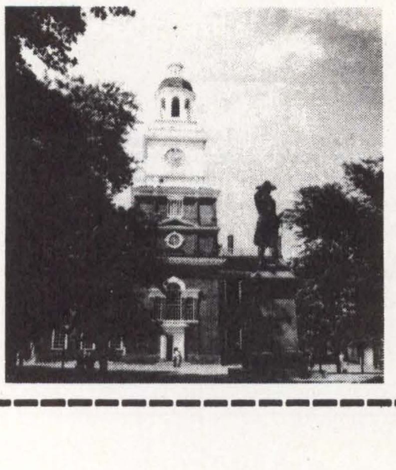

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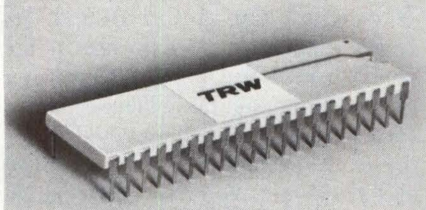

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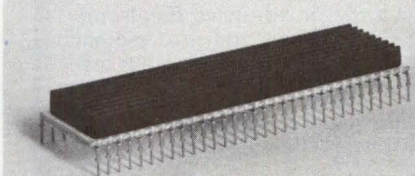

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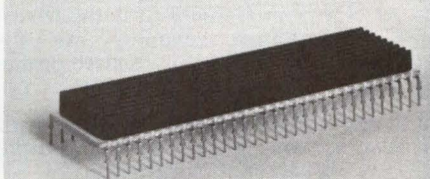

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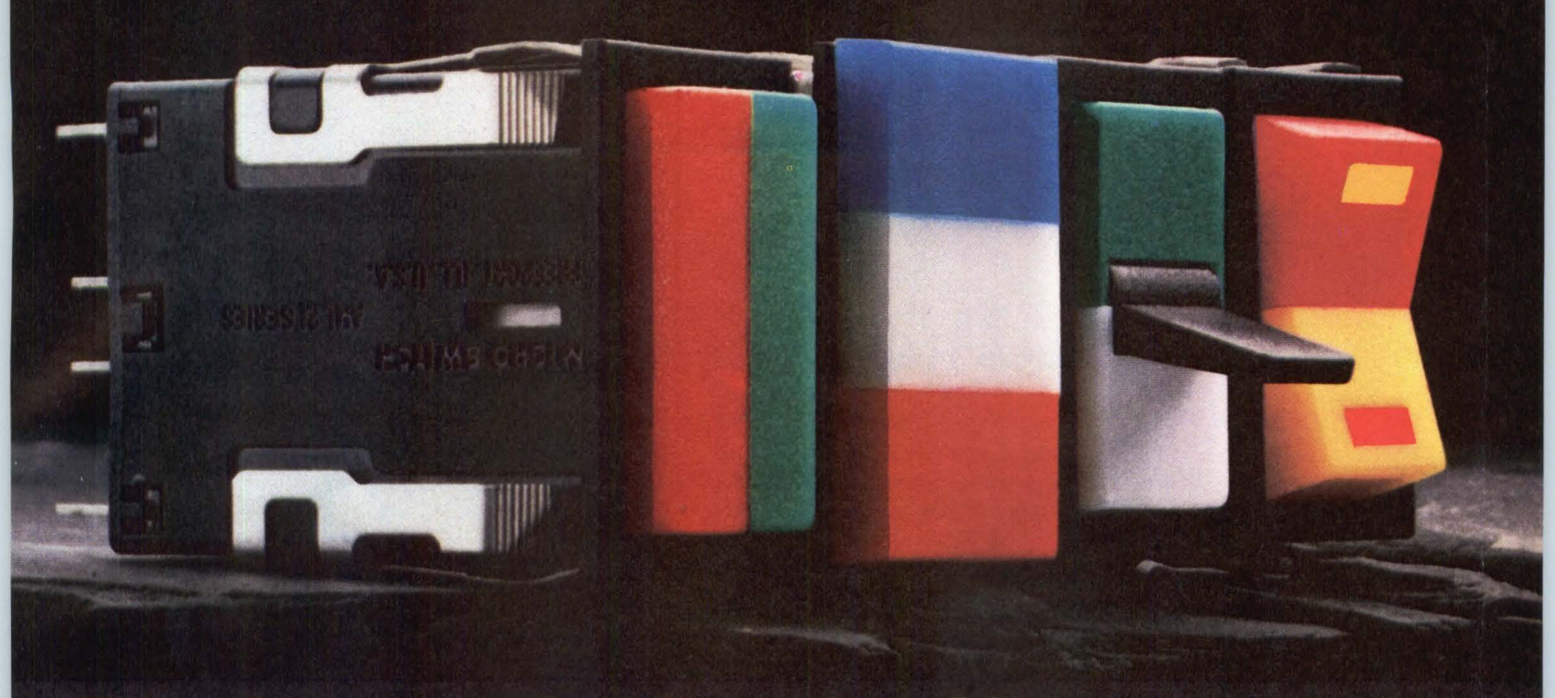
Design cost, time, and size advantages of incorporating small stepping motors should assure increased implementations in future digital drive and positional applications, particularly in analytical instrumentation, business machines, and computer peripherals. □



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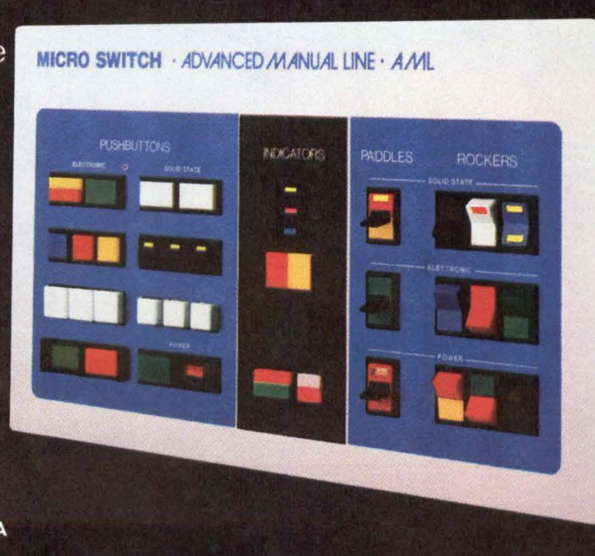


CIRCLE 63 FOR DATA

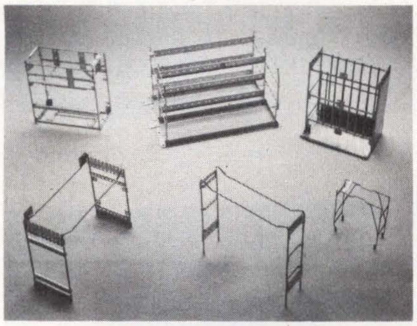
DESIGN BRIEF

Steel Wire Frames Reduce Computer Equipment Costs

Wide-open wireframe construction is substituted for solid metal housings in computer equipment, trimming product costs and weight

Substitution of steel wire chassis for sheet metal to be used as support frames for electronic circuits, outer cabinets, and mechanical components constitutes a major trend in minicomputer and related equipment manufacturing, according to industry sources. The conversion has been away from solid metal housings originally used by manufacturers, and has been redirected toward welded wire, with more than 500,000 units produced during 1977. Manufacturers have adopted the simpler, less costly, wire fixture to cut structural cost and component weight. In addition, more efficient cooling, better accessibility, and reduced assembly time have been achieved.

Composed primarily of steel wire from 0.125 to 0.1875" (0.318 to 0.476 cm) in diameter, the wireform chassis is a welded assembly. Strip steel may be used where fastener holes or flat surfaces for light mounting are necessary. If heavy mounting or radio frequency shielding is required, sheet steel can be affixed to the assembly.



Typical minicomputer wireframe chassis illustrate open access inherent in wire construction to facilitate assembly, access, and service of electronic components. Concept is amenable to variety of computer equipment sizes and shapes and to addition of strip or sheet sections

All elements of a minicomputer, including logic cards and all solid-state circuits, backplane or motherboard, transformers, power supplies, cooling fans, and enveloping outer cabinet, are held by the sturdy wire structure. Components and cabinet are fastened mechanically with screws, rivets, or clinch nuts to the wire frame, which is constructed of low carbon steel wire because of its forming and welding characteristics. The wire tensile strength-to-weight ratio is superior to all other forms of the metal. Welds are as strong as the parent material, and are highly reliable with regard to nonbreakage.

After chassis fabrication, it is possible to plate the wire that is mill-produced for an extra smooth, clean bright finish. One coating option is an electrolytically-applied zinc-bleached chromate combination to supply corrosion protection and a chrome-like appearance. Also available for color coatings are lacquers, paints, and plastisols. The latter is a heat-cured, polyvinyl-chloride finish that provides a rubber-like, shock-resistant surface.

Cost savings have been one of the prime factors in this switch to wire frames. Economies of from 25 to 50% can be realized, with the latter figure being obtained when the wire frame assembly simplifies a more complex design. In fact, the saving can involve reduced costs on three levels—a lower per unit price, reduced tooling charges, and since the frame comes completely prefabricated, elimination of in-plant chassis production or parts inventory—on the part of minicomputer manufacturers.

For a typical chassis measuring 2 x 1.5 x 0.4 ft (0.6 x 0.46 x 0.12 m), the steel wire version weighs 5 lb (2.3 kg) and costs $28, compared to a solid metal design weighing 12 lb (5.4 kg) and costing $53. Similarly, for a typical frame of 10 x 12 x 3" (25 x 30 x 7.6 cm), the wire frame is 1 lb (0.45 kg) at $2.47, while the solid metal version is 2 lb (0.9 kg) at $5.50. Such savings are possible due to the economies of high speed wire fabrication by automatic operating machinery.

A wide-open frame design also facilitates faster assembly of components onto the chassis and eases access to electronics for servicing. In addition, the design permits maximum packing density of components and optimum passage of cooling air and heat dissipation.

Introduction of wire frames into minicomputers has prompted applications in closely-allied products. For example, steel wire is being utilized as tape cartridge receivers for disc drives, and can be combined with a sheet top and tubular legs to produce a low cost cart for logic arrays and computer test equipment. Furthermore, wire-processing racks have been adapted to hold printed circuit cards during etching processes. Line printers are using wire-and-sheet exit guides in place of machined guides, saving 85% in weight and frequently more than $300 in unit cost. Continued progress is expected by computer equipment manufacturers in cost savings and widespread wireframe applications. □

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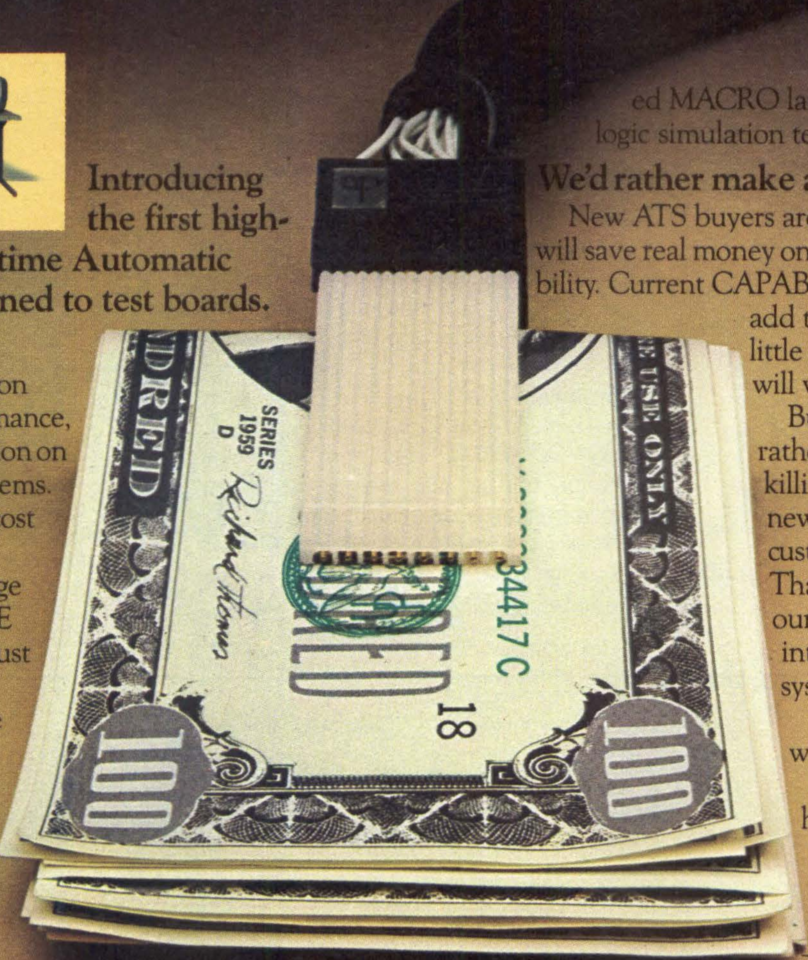

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CIRCLE 64 ON INQUIRY CARD

TECH BRIEF

Counting Digital Filter

Radix (—2) is utilized for more efficient manipulation of data

In this method, negative numbers are represented by a negative radix number. Hardware is much less complex than for conventional sign/magnitude or 2's-complement systems. Letting a_i and x_i represent filter coefficients and input data samples, respectively, where i takes on values between 1 and K, an output word then has the form

$$y_m = \sum_{i=0}^{K-1} x_{m-i} a_i \qquad (1)$$

J_x bits are assigned to each input data word, and J_a bits to each filter coefficient. Using negative radix number representation

$$\left.\begin{aligned} a_i &= \sum_{j=0}^{J_a-1} u_{ij}(-2)^j \quad (u_{ij}=0,1) \\ x_i &= \sum_{j=0}^{J_x-1} v_{ij}(-2)^j \quad (v_{ij}=0,1) \end{aligned}\right\} \qquad (2)$$

Substituting in the original equation gives

$$y_m = \sum_{r=0}^{J-1} h_r (-2)^r \qquad (3)$$

where

$J = J_a + J_x - 1$

$$h_r = \sum_{j=0}^{K-1} \sum_{i=0}^{J_a-1} u_{ji} v_{m-j,r-i} \qquad (4)$$

or, rearranging via the polynomial algorithm

$$y_m = (\ldots(h_{J-1}(-2) + h_{J-2})(-2) + \ldots + h_1)(-2) + h_0 \qquad (5)$$

Equations (4) and (5) embody the basic strategy of the proposed machine. Each element of the double sum in (4) is a product of two 1-bit entities. Such a product is either 0 or 1, and practically speaking, no multiplication is involved in its evaluation. A dual input AND gate is all that is needed. Equation (4) is a summation of KJ_a such terms. Thus, if a system is designed in which KJ_a dual input gates are fed by pairs of bits specified in (4), a count of the number of TRUE gates will equal h_r.

Realization of (5) can now be carried out in the following sequence of operations in an accumulator: shift, change sign, add, shift, etc. Both the counter and accumulator are standard positive radix devices, and the output y_m is obtained in positive binary representation.

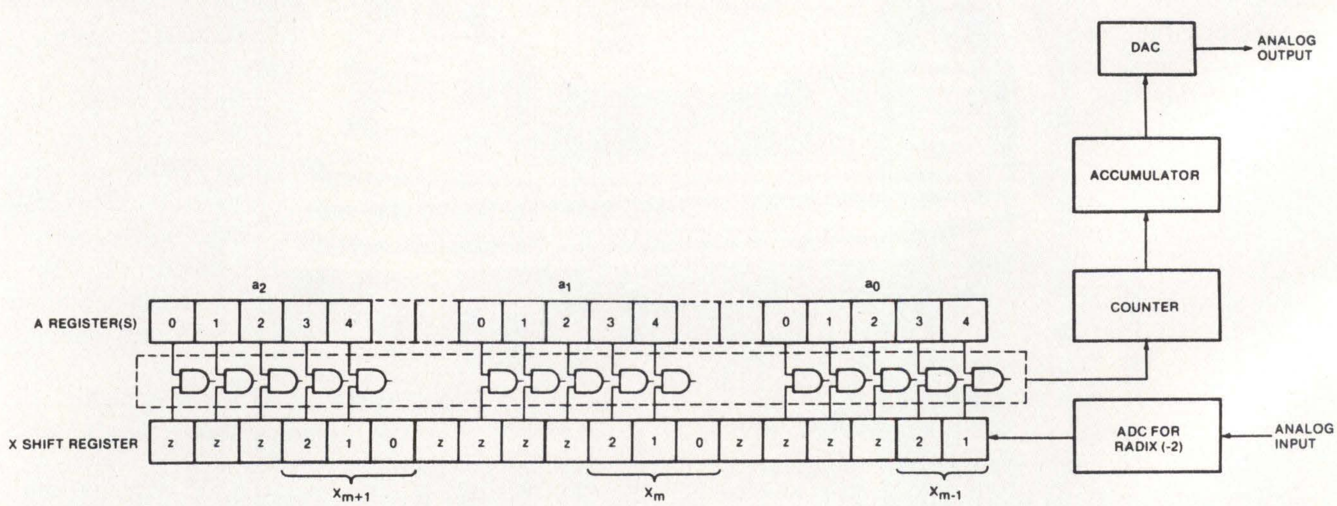
Overall design of the filter is shown in the Figure. The negative radix converter is combined with the analog-to-digital converter in a single functional unit that directly converts analog input to its negative binary representation.

Note

This work was done by Shalhav Zohar of Caltech/JPL. For further information, write to: John C. Drane, Technology Utilization Officer, NASA Resident Legal Office-JPL, 4800 Oak Grove Dr, Pasadena, CA 91103.

Patent

This invention has been patented by NASA (U.S. Patent No 3,732,409). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to: Monte F. Mott, Patent Counsel, NASA Resident Legal Office-JPL, 4800 Oak Grove Dr, Pasadena, CA 91103. Refer to NPO-11821.



Four basic elements: *fixed register* (A) holds coefficients a_i prescribing filter transfer function; *shift register* (X) holds input words x_i; *counter* computes number of TRUE gates after every shift of register X; and *accumulator* combines J counter outputs through shift-and-add sequence to generate output word y_m

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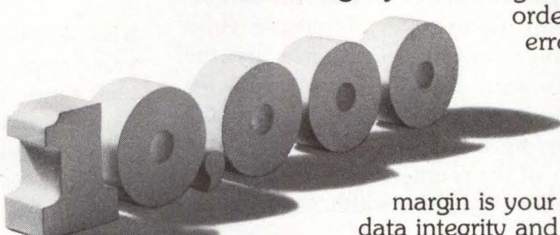

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TECH BRIEF

Low Cost Pressure-Data Encoder

A simple method of linearly translating pressure variations to pulse-width changes

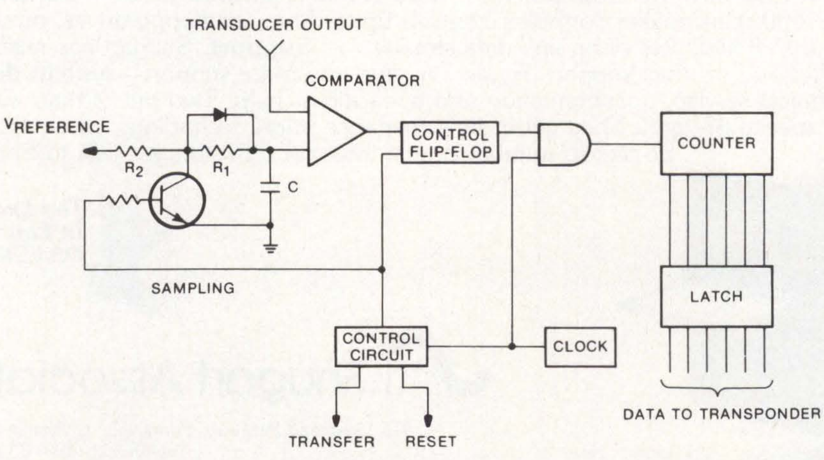
Regenerative switches, used in conventional regulators and dc converters, are similar to those shown in the schematic, with the exception of the new encoder. Simpler and less expensive than its electromechanical counterpart, it directs a digitally encoded signal to the radar transponder which, when queried, transmits the ship's altitude automatically.

Encoder output is linearly proportional to altitude. It compares a pressure-proportional voltage to an exponentially decaying voltage generated by a simple resistance-capacitance timing circuit. A pulse is thereby generated; pulse width is proportional to altitude. This pulse gates a counter which outputs a digital word in a specified altitude code to the transponder.

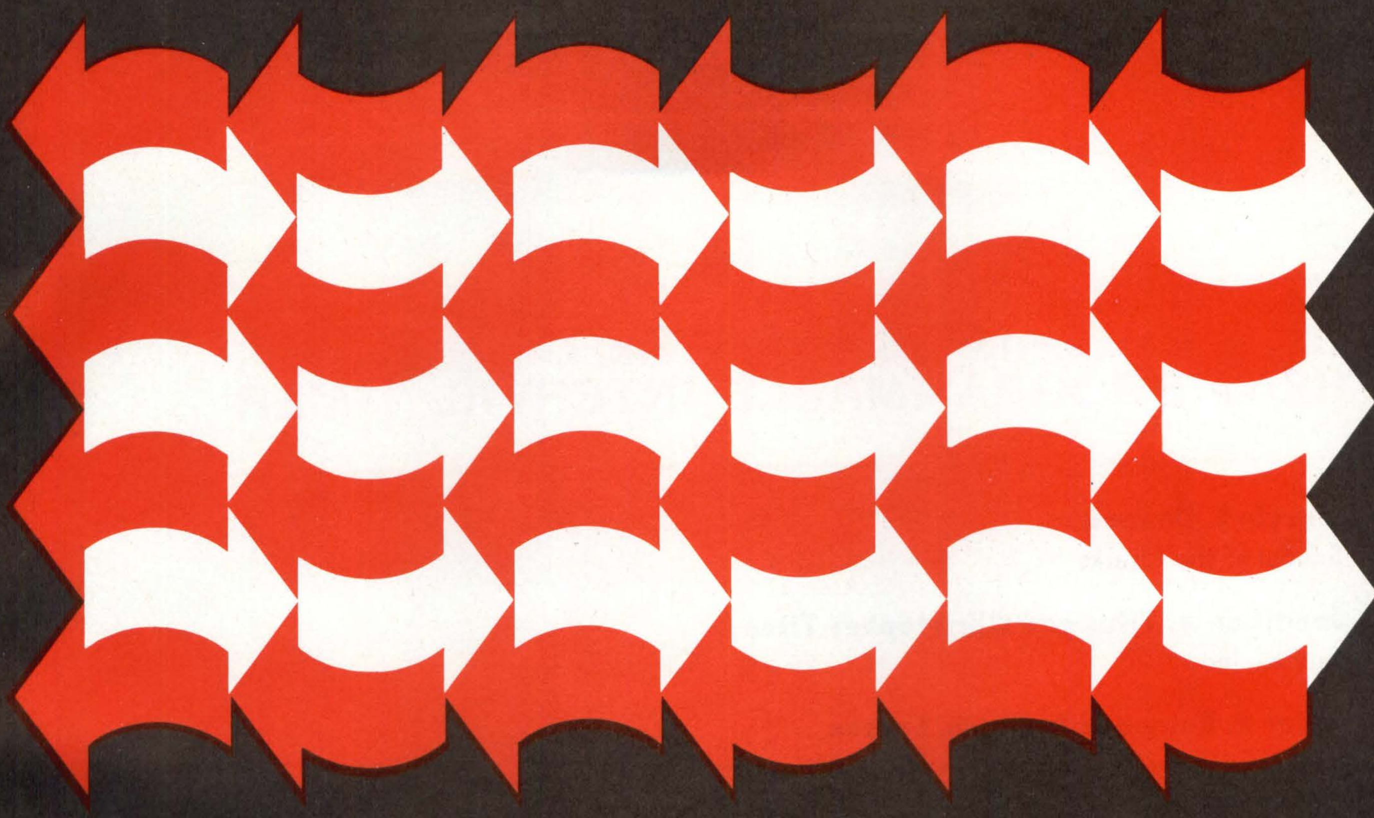
A simplified schematic of the encoder is shown. The time constant generated by R_2 and C is less than one-tenth that of the sample time to assure accuracy. The control circuit clocks the transistor which determines the charging rate of the capacitor. Comparator output is a pulse having a width determined by the transducer. The control circuit, besides sourcing a clock pulse to the sampling transistor, also controls the start of the counter. Total count is determined by pulse width.

Note

This work was done by Richard B. Kolbly and Solomon R. Hedges of Caltech/JPL. For further information, write to: John C. Drane, Technology Utilization Officer, NASA Resident Legal Office-JPL, 4800 Oak Grove Dr, Pasadena, CA 91103. (NPO-13692).



Comparator of altitude encoder is fed fixed exponentially decaying pulse and transducer output which is proportional to pressure. As altitude varies, comparator output pulse width changes similarly. Counter encodes variable-width pulse in modified gray code for radar transponder and in binary-coded decimal for readout circuit



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CIRCLE 66 ON INQUIRY CARD

MICROCOMPUTER INTERFACING: CHARACTERISTICS OF THE 8253 PROGRAMMABLE INTERVAL TIMER

Marvin L. DeJong
School of the Ozarks

Jonathan A. Titus and Christopher Titus
Tychon, Inc

Peter R. Rony and David G. Larsen
Virginia Polytechnic Institute and State University

As a preliminary discussion, some characteristics of the Intel 8253 programmable interval timer are presented. This extremely versatile input/output chip has various potential uses such as a real-time clock, event counter, and period counter, in addition to replacing software-implemented timing loops. For example, interval timers have been used in a digital cardiotachometer, a data-logging timer that employed several phototransistors to measure velocities and accelerations, and a program to sample nonperiodic waveforms for subsequent display on an oscilloscope.*

The 8253 is a 24-pin integrated circuit that requires a single 5-V supply and contains three independent 16-bit interval timers, each of which can be operated in six different modes. An interval timer is a device for measuring the time interval between two actions, or a timer that switches electrical circuits on or off for the duration

*Dr DeJong of the Dept of Mathematics/Physics at the School of the Ozarks, Point Lookout, Mo has implemented the timers in these simple, but diverse, applications.

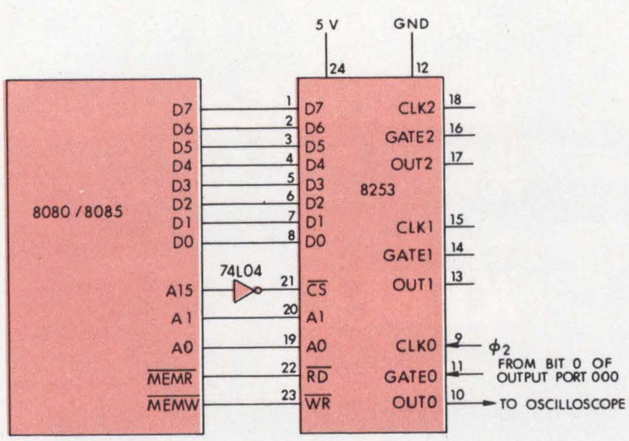

Fig 1 Interface circuit between 8253 programmable interval timer and 8080/8085 microcomputer. Timer uses four locations of memory in this memory-mapped interface circuit

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Anadex

TABLE 1

Addressing the 8253 Programmable Interval Timer

Control Inputs						Memory Address in Demonstration Program and Interface Circuit
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0		
0	1	0	0	0	Load counter #0	200 000
0	1	0	0	1	Load counter #1	200 001
0	1	0	1	0	Load counter #2	200 002
0	1	0	1	1	Load control register	200 003
0	0	1	0	0	Read counter #0	200 000
0	0	1	0	1	Read counter #1	200 001
0	0	1	1	0	Read counter #2	200 002
0	0	1	1	1	No operation (3-state)	—
1	X	X	X	X	Disable chip (3-state)	—
0	1	1	X	X	No operation (3-state)	—

Note: X = don't care (logic 0 *or* logic 1)

of the preset time interval.[1] Fig 1 serves the dual purpose of giving the pin diagram of the 8253 chip, while showing how the chip can be interfaced with an 8080A/8085 based microcomputer system using memory-mapped input/output (I/O).[2]

Four internal registers—three interval timers and a control register—that are decoded as memory locations 200 000 through 200 003 with the aid of the address bus signals A0, A1, and A15 (see Fig 1 and Table 1) are contained on the 8253 chip. In Table 1, the $\overline{RD}$ and $\overline{WR}$ control inputs determine whether a specific register is being loaded or read. It is not possible to read the contents of the control register.

Table 2 summarizes the coding for the 8-bit control register within the chip. Bits D7 and D6 determine the selection of the interval timer; bits D5 and D4 determine the nature of the read/write operation associated with the chosen timer; bits D3, D2, and D1, the mode of operation of the timer; and bit D0, whether the timer counts down in binary or binary-coded decimal (BCD).

Fig 2 provides a block diagram for a typical counter in the chip. The microcomputer loads the 16-bit down

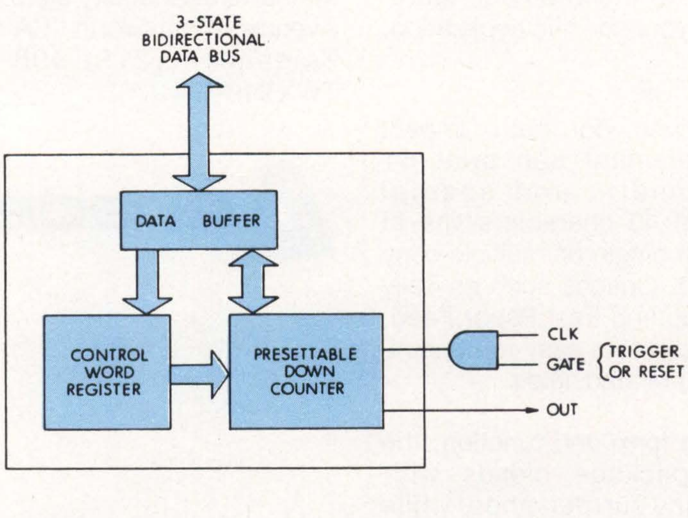

Fig 2 Functional diagram of each of three 16-bit interval timers in 8253 chip. Gate input acts alternatively as gate, trigger, or reset input, depending upon mode chosen

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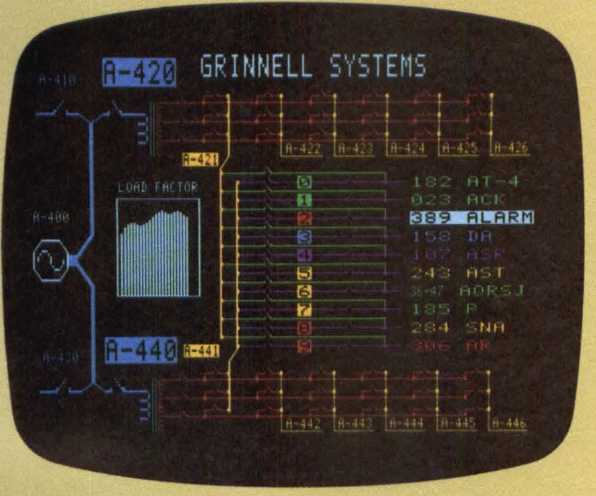

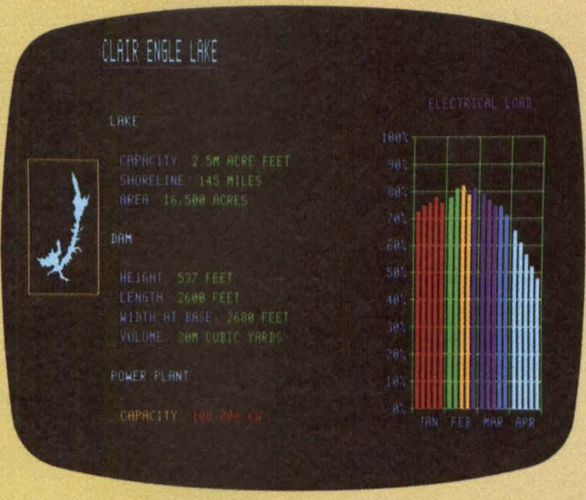

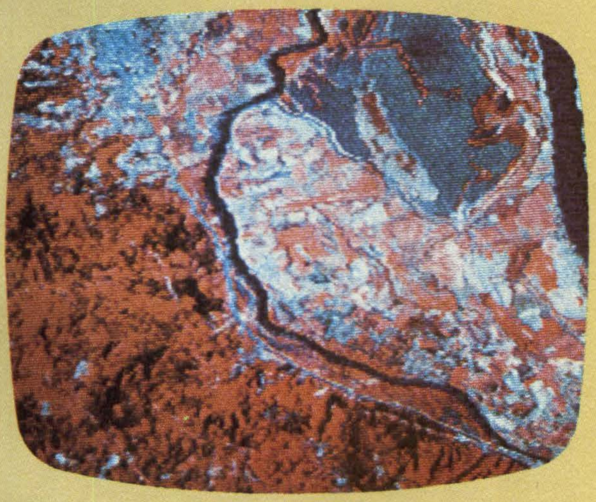

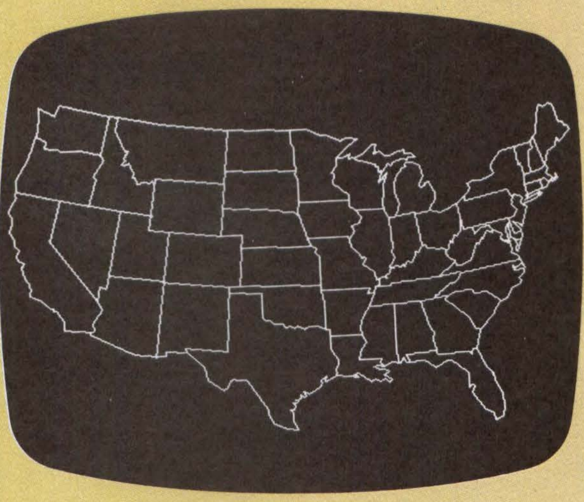

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counter as two successive bytes, a HI and LO byte, via the bidirectional data bus, D0 through D7. If the gate line, GATE, is active, negative edge transitions at the CLK input decrement the counter. When the counter reaches zero, OUT becomes active, its actual behavior depending upon the mode programmed into the control register for the counter (see Table 2). The three 16-bit counters on the chip can each be programmed independently in any one of the six modes of operation. Counter inputs and outputs—CLK, GATE, and OUT—for the chosen counter are independent of the CLK, GATE, and OUT I/O of the remaining two counters on the chip.

In addition to the address, data, and control bus connections shown in Fig 1, the CLK0 and GATE0 inputs to counter 0 are respectively connected to the $\phi 2$ [transistor-transistor logic (TTL)] microcomputer clock output (typically 2 MHz) and to bit 0 of accumulator output port 000. Any TTL level clock with a frequency of less than 2 MHz can be used as input to CLK0, and any suitably debounced switch or source of strobe pulses can be used to control the timer at GATE0. The output of the counter, OUT0, can be connected to an oscilloscope to permit observation of each of the six timer modes of operation.

Next month's discussion will focus on the behavior of a demonstration program for the 8253 programmable peripheral interface chips, which are further described in Refs 3 and 4. This program will illustrate the loading, latching, and reading of counter 0 as well as the various output modes.

TABLE 2

Coding for 8-Bit Control Register in 8253 Chip

Bits			Control Function
	D7	D6	
	0	0	Control word is for counter #0
	0	1	Control word is for counter #1
	1	0	Control word is for counter #2
	1	1	———
	D5	D4	
	0	0	Latch both bytes of chosen counter for read operation
	0	1	Load or read only most significant byte (MSB) of chosen counter
	1	0	Load or read only least significant byte (LSB) of chosen counter
	1	1	Load or read LSB first, then MSB of chosen counter
D3	D2	D1	
0	0	0	Mode 0: Output = 1 on zero counter
0	0	1	Mode 1: Retriggerable variable-width one-shot
X	1	0	Mode 2: Programmable rate generator
X	1	1	Mode 3: Programmable square wave generator
1	0	0	Mode 4: Delayed strobe (software triggered strobe)
1	0	1	Mode 5: Triggered strobe (hardware triggered strobe)
		D0	
		0	Count down in binary
		1	Count down in BCD

Note: X = don't care (logic 0 *or* logic 1)

References

1. R. F. Graf, *Modern Dictionary of Electronics,* Howard W. Sams & Co, Indianapolis, Ind, 1972, p 298
2. D. G. Larsen, P. R. Rony, and J. A. Titus, *The Bugbook[R] VI. 8080A Microcomputer Programming and Interfacing,* E & L Instruments, Inc, Derby, Conn, 1977, p 21-1
3. *Intel Data Catalog 1977,* Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, pp 10-159 (Price, $2.50)
4. A. Osborne, *An Introduction to Microcomputers, Vol II. Some Real Products,* Osborne and Associates, Berkeley, Calif, 1976, pp 4-106

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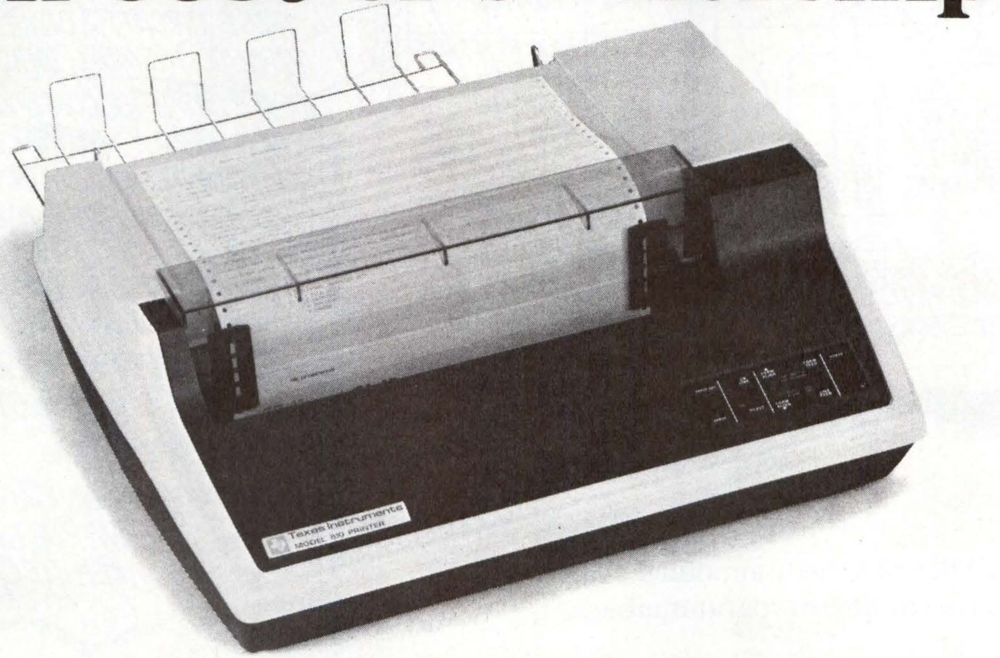

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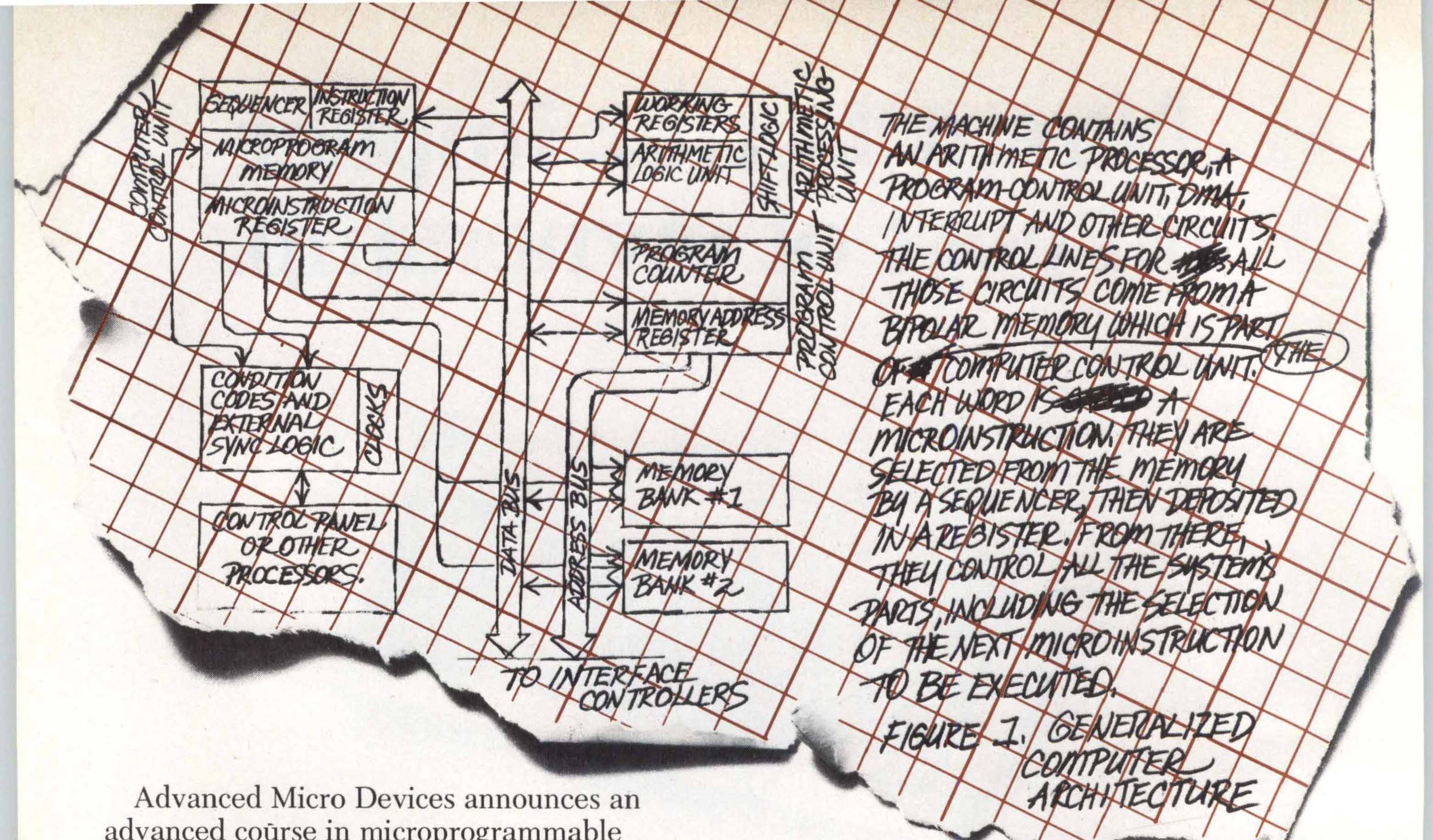
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THE MACHINE CONTAINS AN ARITHMETIC PROCESSOR, A PROGRAM-CONTROL UNIT, DMA, INTERRUPT AND OTHER CIRCUITS. THE CONTROL LINES FOR ALL THOSE CIRCUITS COME FROM A BIPOLAR MEMORY WHICH IS PART OF THE COMPUTER CONTROL UNIT. EACH WORD IS A MICROINSTRUCTION. THEY ARE SELECTED FROM THE MEMORY BY A SEQUENCER, THEN DEPOSITED IN A REGISTER. FROM THERE, THEY CONTROL ALL THE SYSTEM'S PARTS, INCLUDING THE SELECTION OF THE NEXT MICROINSTRUCTION TO BE EXECUTED.
FIGURE 1. GENERALIZED COMPUTER ARCHITECTURE

Powerful Analog Output Subsystem Provides Simplified 8080 Data Conversion

Ready-to-use digital-to-analog converter board RTI-1201 provides all hardware and software necessary to interface the Intel SBC-80 series of single-board computers, with which it is electrically and mechanically compatible. The complete 2- or 4-channel analog output subsystem includes four digital outputs and is also compatible with the company's RTI-1200 I/O interface board (see *Computer Design*, Jan 1977, pp 128-129), the Intel System 80 microcomputer series, Intel MDS microcomputer development system, and National Semiconductor BLC-80/10 board-level computer.

Designed by Analog Devices, Inc, PO Box 280, Rte 1 Industrial Pk, Norwood, MA 02062 with ease of application as the key design goal, the single PC board combines features and capabilities to reduce hardware and software efforts required to interface a microcomputer. The system fills applications ranging from process control and laboratory automation to graphic plotting, automatic test equipment, and electromechanical positioning.

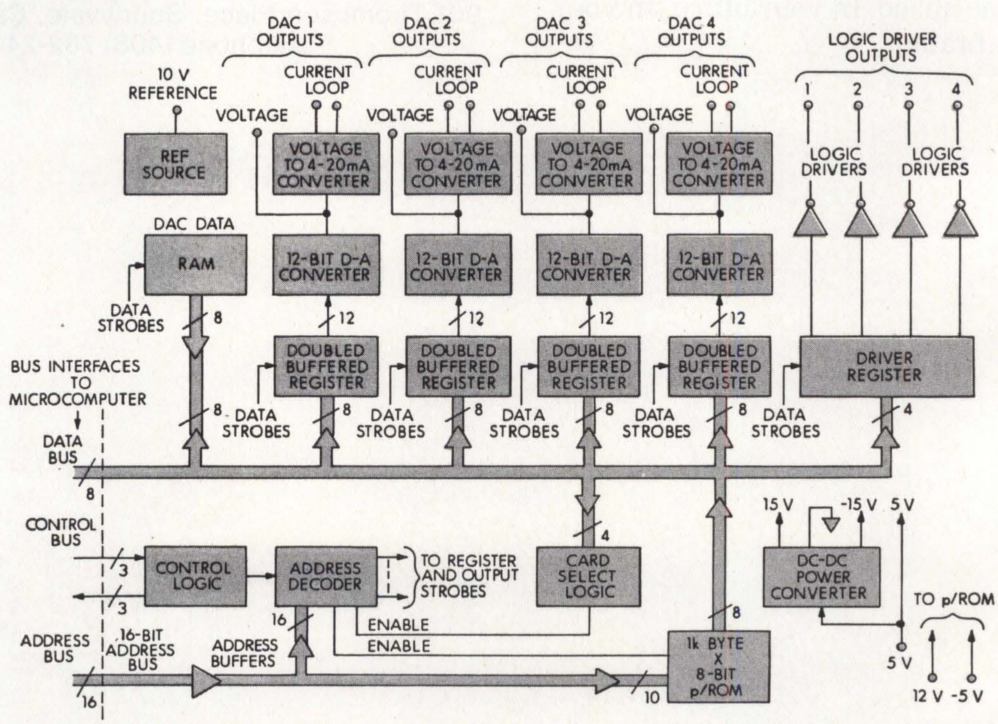
Plugging directly into the bus connector of the user's card cage, the card makes all analog interfaces through a pin connector mounted at the opposite board edge. Features are selected through wirewrap connections, and may be reconfigured if the application changes.

The system interfaces to the microcomputer as a 1k block (1024 bytes) of memory; it can be configured by the user to occupy any one of 16 selected blocks of memory spread throughout the SBC's 65k address space. The memory-mapped interface feature allows the designer to use all of the 8080 memory reference instructions for greater software sophistication.

Data conversion occurs through 12-bit DACs which are software driven using double buffered registers. The buffers allow two data bytes to be loaded simultaneously into the DAC. By using the 10-V onboard reference, each DAC can be user set to any of five output ranges. The D-A input code for each channel can also be set for natural binary, offset binary, or two's complement.

In addition to analog outputs, the board contains four high current logic drivers for system control functions. These open collector driver outputs are software controlled with 30-V, 300-mA capability.

Other features of the 6.75 x 12" (17 x 30-cm) board include D-A data readback, which eliminates the need



Analog Devices' RTI-1201 Intel SBC 80 compatible output subsystem contains four digital and four analog channels. Components are contained on single board to reduce hardware and software efforts required to interface microcomputers

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for scratchpad memories or software overhead; a flash reset for resetting any or all DACs by a single-byte instruction; memory overlay for RAM and ROM inhibit; and card select, which allows up to 16 of the boards to share the same 1k block of memory locations. An onboard p/ROM socket and 4- to 20-mA current loop outputs are also included. Power is from ±15 V where available; an optional single 5-V supply can be obtained.

Prices begin at $298 for the 2-DAC version and $379 for the 4-DAC version. A manual is included with each board.

Circle 420 on Inquiry Card

File System Adds To 8080 Multitasking Operating System

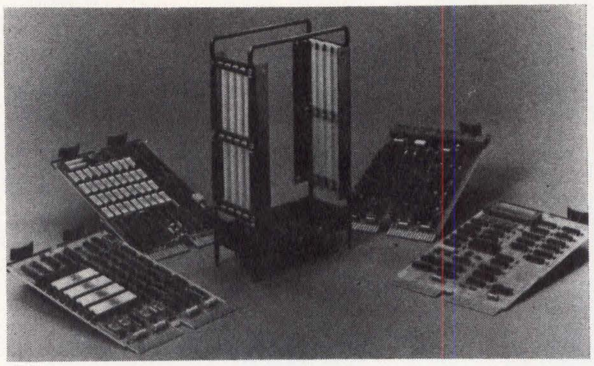
A file system has been added to FAMOS multitasking 8080 DOS by MVT Microcomputer Systems, 21822 Sherman Way, Canoga Park, CA 91303 to support all file access methods including ISAM and random access. File record lockouts are automatically set. The system is totally device dependent, enabling any mix of disc drives (floppy and hard) to be simultaneously supported. Any random access storage device (RAM, drum, core memory) can be included in the file structure, providing microcomputers with virtually unlimited memory capability.

Features include variable block sizes, record blocking, and block manipulation in BASIC. Sector allocation scheme for files is augmented with an automatic file system integrity maintenance feature. A new version of MVT-BASIC, a multi-user BASIC compiler, also has been released with the inclusion of powerful I/O extensions to the language for applications programming.

Circle 421 on Inquiry Card

Space/Cost Critical Applications Are Served By μComputer Modules

Measuring half the physical size of, and offering performance equal to current LSI-11 products, LSI-11/2 modules are software compatible with the LSI-11, and offer configuration price savings to 44% below existing products. Key element of the family is the LSI-11/2 CPU, which like other family members is mounted on a 5 x 8.5" (12.7 x 21.6 cm) module. The family includes various memory modules, as well as a matching-width card guide and backplane assembly. Interface options are also available.



LSI-11 computer-on-a-board offers full power of DEC's LSI-11 microcomputer in half physical width. Microcomputer is fully bus compatible with older-width version; it can be installed as internal component in many instruments, permitting development of "intelligent" devices, such as laboratory instrumentation and industrial controllers

The microcomputer is available in 4k, 8k, 16k, and 32k-word memory configurations, with optional byte parity. The CPU (KD11-HA) is also available by itself in quantities of 50 for applications requiring custom RAM or ROM configurations. Hardware options include a serial line interface card with four RS 422/423 independently programmable channels, and a foundation kit for interfacing and control applications.

A software package, a subset of the RT-11 operating system, has been developed by Digital Equipment Corp's Components Group, One Iron Way, Marlborough, MA 01752 to permit execution of programs developed on a full RT-11 system. Called RunTime RT-11, the system permits programs developed in MACRO-11, FORTRAN, BASIC-11, APL, and FOCAL™ to operate on LSI-11/2 systems.

Circle 422 on Inquiry Card

Enhanced μComputer and Development System Facilitate Software Use

Using the SuperPac microcomputer as a base system, Process Computer Systems, Inc, 750 N Maple Rd, Saline, MI 48176 has developed a BASIC Interpreter Package (BIP) which resides in 8k bytes of EPROM and uses 8k bytes of RAM for program storage. This enhanced version, known as Protopac, permits fast prototyping of software for demonstration setups, as well as easy software modification in dynamic environments where software requirements must be continually modified by those who may be unfamiliar with them.

The interpreter has an extensive array of I/O interfacing and is compatible with existing SuperPac and 180 series I/O modules. A SuperPac can be converted to a Protopac by plugging in the integrated package. Capabilities include Dim, Let, If . . . Then NN, For/Next, Gosub/Return, logical ANDs and ORs permitted in expressions, and memory reference facilities.

The company has also announced a microcomputer software development system SPDS for SuperPac 8080 and Z80 based microcomputers to ease the creation of software. (If used with the Protopac, the system's BASIC module would not be utilized.) Features include a FORTRAN compiler; cross-reference generator which lists constants, labels, and addresses; a relocatable assembler with full macro capability; and up/down loader that passes software directly into the target system which can be up to 1000 ft (305 m) away.

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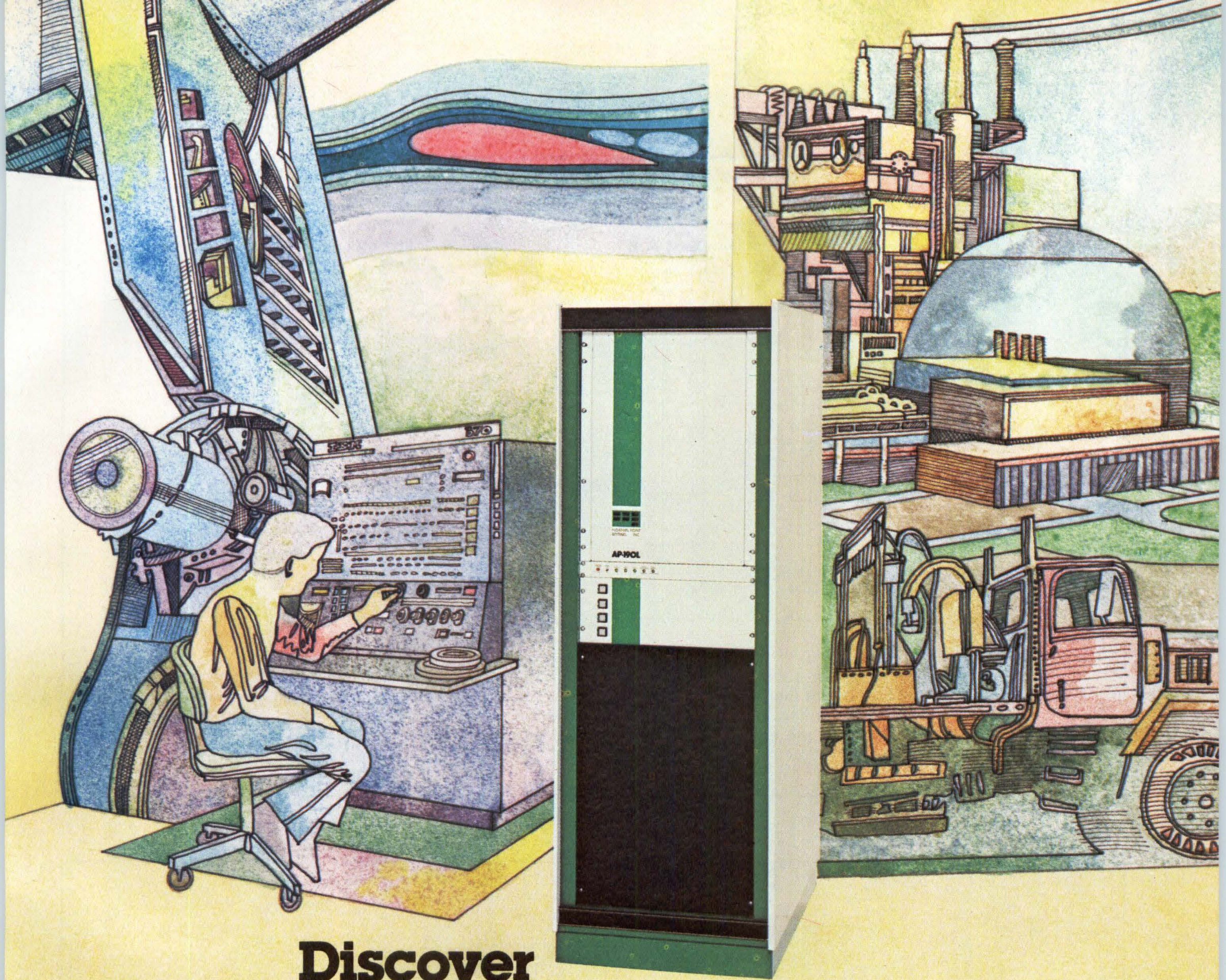
Data Acquisition System Saves Space In μProcessor Applications

A 2-package system combining the MN7130 multiplexed sample/hold



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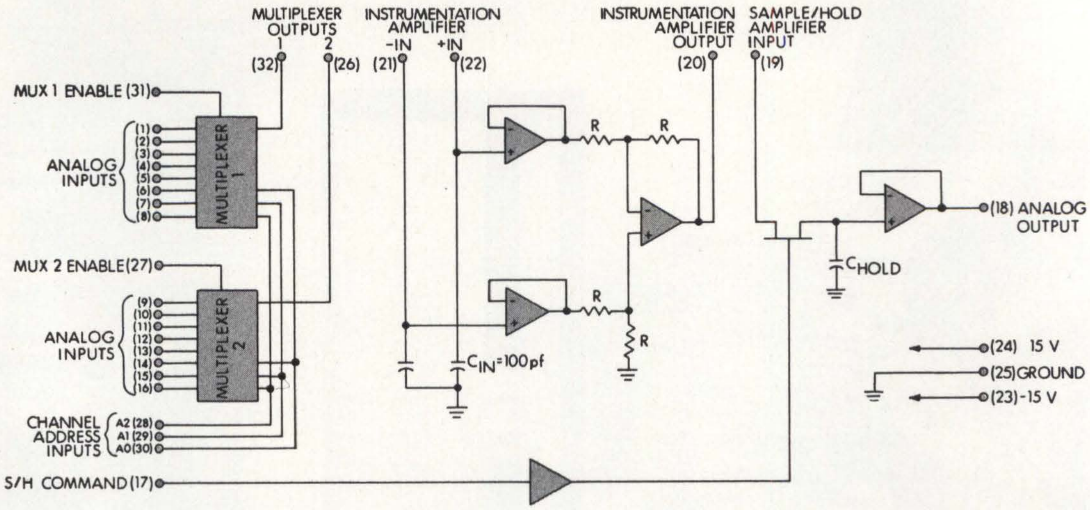
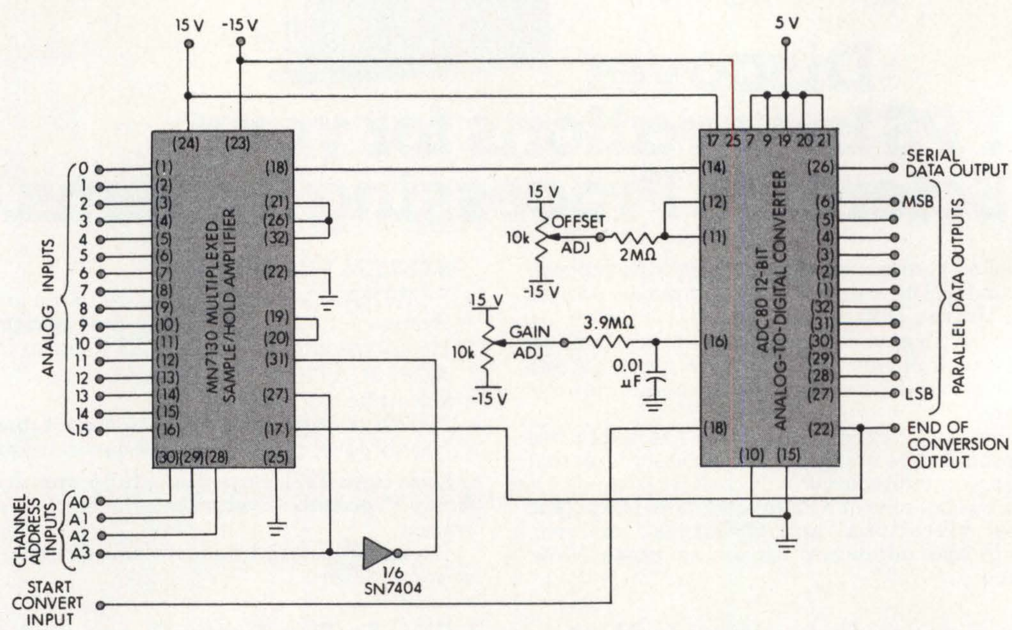


Analog output subsystem consists of either two or four 12-bit DACs and four digital output channels, comprised of high current logic drivers for system control functions. Memory-mapped interface allows use of 8080 memory reference instructions. Board plugs into bus connector of card cage; analog interfaces are made through pin connector mounted at opposite board edge



Micro Networks' MN7130 amplifier can be used in conjunction with ADC80 or MN5240 ADCs to configure an inexpensive data acquisition system in minimum board space. Throughputs of 30k channels/s are achieved with the ADC80. Typical 16-channel single-ended input data acquisition system operates in ±10-V input range. In data acquisition applications, sample/hold command input can usually be driven directly from ADC end-of-conversion output

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CIRCLE 73 FOR NOVA, 74 FOR PDP-11, 75 FOR CUSTOM APPLICATIONS amplifier and ADC80 12-bit A-D converter is the basis of a complete 12-bit, 16-channel data acquisition system that is both physically and electrically compatible with microprocessor technology. The two DIPS are easily mounted on the same board as the controlling microprocessor, thus saving space and the cost of special connectors and mounting hardware.

Heart of the system is the amplifier package, which provides 16 single-ended or eight differential input channels and has an 8-μs acquisition time. It contains multiplexers, instrumentation amplifier, and sample/hold amplifier. Use of differential inputs provides elimination of ground return offsets.

The internal instrumentation amplifier provides 250-MΩ input impedance and over 80 dB of common mode rejection in the differential input configuration. Input range is ±10 V, and droop rate is 4 mV/ms. Contained in a 32-pin hermetic DIP, the hybrid IC is CMOS compatible and binary addressable with a 3- or 4-bit word.

The system may be used with a variety of DIL ADCs offered by Micro Networks Corp, 324 Clark St, Worcester, MA 01606. When combined with the ADC80, the system costs less than $140 in OEM quantities.
Circle 424 on Inquiry Card

Switching Regulated Power Supplies Are Designed for μP Use

The ES line of openframe, multiple output, switching-regulated power supplies has been expanded with the introduction of a special series designed for microprocessor applications. Providing up to five outputs (with 5, 9, 12, 15, 18, 24, and 28 V as std), the 4.5-lb (2-kg) packages are available in various voltage/current combinations totaling up to 200 W of power.

Power/Mate Corp, 514 S River St, Hackensack, NJ 07601 has used LSI circuitry to provide efficiencies to 78%, operation in ambient temperatures to 50°C without derating, and a holdup time of 30 ms after loss of input power from nominal line.
Circle 425 on Inquiry Card

Laboratory Data Acquisition System Is Based on LSI-11

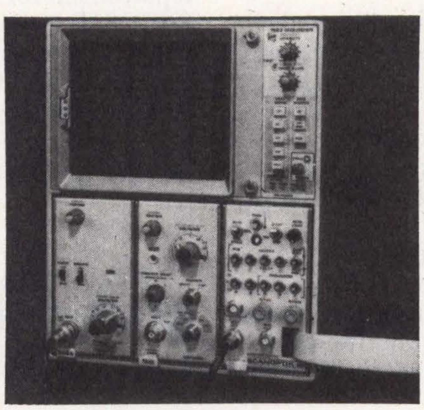
The GRC 11/X3 computer system forms the heart of the LAB/X3 laboratory data acquisition system, which is a 28k-word LSI-11 microcomputer system with 16 channels of 12-bit A-D conversion, a throughput of 35 kHz, and two channels of 12-bit D-A conversion. A crystal-controlled programmable real-time clock is provided for precise control of sampling intervals.

System uses a dual drive, double density flexible disc subsystem, for total data storage exceeding 1.2M bytes and transfer rates as high as 500k bits/s. A DMA interface relieves the processor of time consuming data transfers.

General Robotics Corp, 57 N Main St, Hartford, WI 53027 also provides the system with digital I/O capability; all signal levels are TTL compatible. A software package is included. System options such as a graphics terminal, 20M-byte cartridge disc subsystem, and additional software also are available.
Circle 426 on Inquiry Card

μProcessor Oriented Logic State Analyzer Is Plug-In for Oscilloscope

LC-732 is a logic state analyzer packaged as a plug-in to Tektronix, Inc's 7000 series oscilloscopes. Its single module size with 32-channel capability allows use in a 4-wide scope (horizontal position) without affecting normal scope operation; the modes can be switched back and



forth between scope and analyzer without swapping plug-ins. It can also be used with 3-wide scopes.

For triggering, the analyzer matches either 16-bit address bus or 8-bit data bus, or both, for a 24-bit word trigger on the system under test. Scanoptik, Inc, PO Box 1745, Rockville, MD 20850 has also built in a digital delay feature. Memory stores 64 words of 32 inputs, presenting the information in hexadecimal characters on the scope.

The device provides general-purpose connections to any microprocessor or digital system (up to 10-MHz clock rate). A 40-pin clip-on input cable assembly can be used to match the 40-pin connector directly with the 8080A, 6800, Z80, or any other microprocessor.
Circle 427 on Inquiry Card

Four Channels From Interface Board Act As One Load to I/O Bus

The QuadrAsync/LSI™ interface board gives LSI-11 users four asynchronous EIA and/or 200-mA serial communications channels while presenting only one load to the I/O bus. The board from Able Computer Technology, 1616 S Lyon St, Santa Ana, CA 92705 has critical isolators, and can drive either active or passive current loops.

Condensed onto a single quad board, the unit is an alternative to the DLV-11 and is completely software compatible with the DEC unit. Operation is full or half duplex with transmitter and receiver for each channel operating at the same baud rate.
Circle 428 on Inquiry Card

Three Low Cost Modules Are Compatible With Established Family

The TM 990 family of 16-bit microprocessor-based CPU and peripheral circuit modules has been expanded by Texas Instruments Inc, PO Box 5012, Dallas, TX 75222 with the addition of one I/O and two memory expansion boards, each of which is a preassembled, pretested, and ready-to-use single PC board. These additions further expand the 990 family software compatible concept, providing additional cost versus capability level between the TMS 9900 com-

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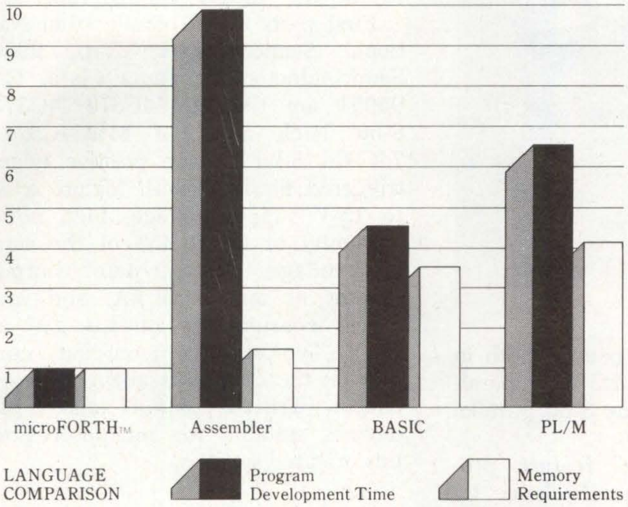

Units of time and memory required are averages provided by microFORTH users, based on actual application experience and/or specification estimates.

Find it hard to believe that FORTH software tools can short-cut microsystem development that much? Or that you don't have to give in to those old time/memory trade-offs which bog down so many microprocessor projects?

Skeptics, take note: microFORTH software has turned the corner in microsystem implementation, for the likes of AT&T, G.E., Monsanto, RCA and Hughes as well as the U.S. Army and Navy (and more).

Fully user-proven, microFORTH provides much more than an interactive multi-level language: a disk-based operating system, plus assembler, compiler, interpreters, text editor (and your entire program) are all concurrently resident. The more we could put in the package, the less you're put out.

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Less memory required: half the bite of assembler code; 60-80% less than other high-level languages. microFORTH's dictionary structure provides modularity of coding and uses precompiled definitions via indirect threaded code.

Less overhead. microFORTH run time is not only faster than other high-level languages, it's controllable too – with full machine-speed capability available when you need it. Intersperse machine-code subroutines without calling sequence expense.

And more transportable programs. microFORTH provides a consistent software interface between you and a broad range of different manufacturers' hardware. Application programs are easy to transfer to a variety of μP systems.

But no matter whose microprocessor is in place, microFORTH minimizes your hardware investment, since it requires less memory capacity, permits simpler hardware logic.

In short, FORTH softens your total investment. Off-the-shelf microFORTH is package-priced at $2500, plus options. (Contract application programming services are also available.)

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ponent level and 990 series microcomputers.

The TM-990/201 memory expansion board has 4k x 16 words of EPROM and 2k x 16 words of static RAM, expandable respectively to 16k x 16 words (with 2716 EPROMS) and 8k x 16 words (with 4045 static RAMS). The -990/206 memory board with 4k x 16 words of static RAM is expandable to 8k x 16 by plugging in 4045 RAMS. The -990/310 is a 48-bit I/O expansion module. All are intended for use with the TMS 9900-based CPU which includes 1k x 16 words of EPROM.

The series works with the AMPL™ prototyping system. A user's manual of hardware and software is supplied with each unit. Additional accessories and peripherals are offered.

Circle 429 on Inquiry Card

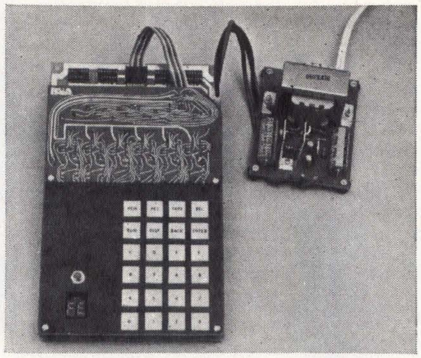
Hardware Board Gives Fast Floating Point Processing to SBC 80

Compatible with the SBC 80, the FPB-B hardware floating point board is said by North Star Computers, Inc, 2465 Fourth St, Berkeley, CA 94710 to be up to 50 times faster than 8080 software. Approximately 1k of memory is saved over using software arithmetic. Number representation is BCD; precision is software selectable up to 14 digits. The 8080 or Z80 processor passes arguments and specifies operation and precision to the board, which executes the operation and returns results to the processor.

Circle 430 on Inquiry Card

Computer System Is Used As Processor Board and Development System

The 8700 computer/controller—an OEM microprocessor development system—acts as a microprocessor familiarization and training system and as a low cost entry point to microprocessor-based products for the smaller manufacturer. PAIA Electronics, Inc, 1020 W Wilshire Blvd, Oklahoma City, OK 73116 based the unit on the 650x family of processors. The fully socketed, plated-through board provides space for 1k bytes of



RAM and 1k bytes of p/ROM, both in 256-byte increments; five 8-bit parallel input ports; and one 8-bit parallel output port.

A "microdiagnostic" feature provides simple system checkout by floating the MPU data bus while forcing the execution of an address-incrementing NOP instruction. The interactive editor debugger (PIEBUG) monitor program provides complete control of code entry and debugging. Various options are available for the system.

Circle 431 on Inquiry Card

BASIC is Available to OEMs, With Termination of Exclusive License

Altair™ BASIC for the 8080 and Z80, said by Microsoft, 819 Two Park Central Tower, Albuquerque, NM 87108 to be the first resident high level language for a microprocessor, is now generally available on both a single copy and OEM basis. It includes extended features for operational ease in commercial applications. BASIC became the subject of an extended legal dispute that resulted in the termination of an exclusive license to MITS, Inc.

Circle 432 on Inquiry Card

CMOS Family of Octal Interface Devices Is Planned for μProcessors

A CMOS version of the industry-standard 20-pin octal interface devices incorporates a circuit design allowing them to drive high capacitive loads and to have a fanout of one when driving standard TTL loads. The key is a drive transistor configuration on the output circuitry in which an npn emitter-follower structure is used in parallel with a p-channel transistor to source the 20-mA drive current and to pull the output voltage up to the V_{cc} supply voltage rail.

First parts in the family from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051 are the MM54C373/74C373 8-bit latch and the MM54C374/74C374 8-bit D-type positive edge-triggered flip-flop. Both feature a 3- to 15-V supply voltage, high noise immunity of about 45% of the supply voltage, low Tristate® output current of approx 5 nA, and low power consumption of 1.0 μW at 15 V. Typical drive (sourcing) current on the devices is about 20 mA/output. Tristate outputs make the devices suitable for microprocessor-bus oriented systems.

Assembled or Kit Form Microcomputer Is Contained on Single Board

The 8080A-MU-1000 single-board microcomputer, designed to provide onboard power for most processing applications, contains an 8080A CPU set; 4k RAM/4k ROM module with automatic power-on address relocation to any jumper selected address; I/O module with two independent USARTS, six parallel ports, eight buffer/drivers, and I/O interrupts; a bus driver/buffer module; and user design module with ten 16-pin wirewrap areas for special-purpose implementations. Systemathica Consulting Group, Ltd, PO Box 10154, Pittsburgh, PA 15232 has included a power supply of 5, 12, or −12 V.

Serial I/O simultaneously operates 20-mA current loop and RS-232 with baud rates from 75 to 19,200 through independent edge connectors. Parallel I/O has 48 lines through a separate edge connector. The ROM monitor contains the standard 1k operating system.

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Flexible Computer Operates From 8080 CPU Using S-100 Bus

A compact desktop computer, the Attache™ is a 25-lb (11-kg) unit built around the 8080 MPU, with a

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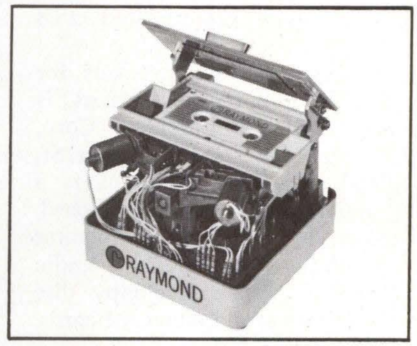
shipped over 10,000 small digital tape drives last year. To more than 100 customers!

We manufacture:

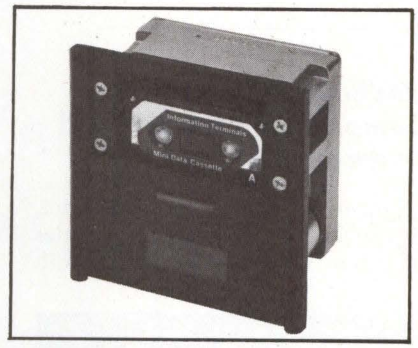
Model 6406 **Raycorder**

for Philips cassettes — the industry standard for more than 6 years.



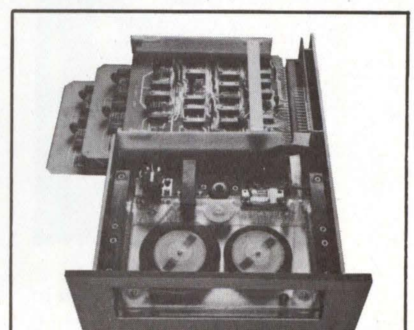
Model 6409 **Mini-Raycorder**

for ANSI X3B5/77-22 Mini-Data cassettes — the first in the industry. Now added features make it even better — the runaway leader in its class.



Model 6413 **Cartridge Raycorder**

for ¼-inch data cartridges. A new offering this year from Raymond — a new package with a proven track record.



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full ASCII keyboard (u/lc). Its circuitry uses the S-100 bus configuration with a 10-slot board capability.

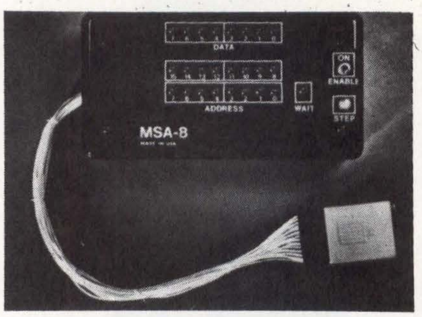
Standard features include LED indicators for on/off and systems status, a reset switch which returns to p/ROM monitor, a monitor p/ROM that controls operation of the computer from the keyboard, and a video output jack (75 Ω). The video output provides 16 lines of 64 characters. Forced air cooling occurs over the vertically mounted cards. The heavy-duty power supply provides 10 V at 10 A (regulated to 5 V on boards), with preregulated ±18 V at 2 A.

A 1k RAM plus extra sockets for p/ROMs on the turnkey board is standard. Pertec Computer Corp, Microsystems Div, 21111 Erwin St, Woodland Hills, CA 91367 offers a basic configuration with keyboard, and CPU, video, and turnkey monitor boards. Options include an audio cassette recorder board, floppy disc systems, software, and memory boards.

Circle 434 on Inquiry Card

Handheld Unit Performs µComputer Firmware and Hardware Debugging

Single step, hardware breakpoint, and oscilloscope trigger capabilities combine to make the MSA-8 a suit-



able tool for microprocessor system checkout. It connects directly to such microprocessors as the 8080A, 8085, and Z80. Data, address, and ready displays are featured. Computer System Dynamics, 2780 S Main, Salt Lake City, UT 84115 has provided single step, single step enable, trace enable, and breakpoint thumbwheel switches for control.

Circle 435 on Inquiry Card

Single Instruction Controls Data Acquisition System

Problems associated with interfacing A-D and D-A boards to a microcomputer system are solved by the memory implemented data acquisition systems (MIDAS), which are aimed at the industrial process control market. The ASC1080 analog input board, electrically and mechanically compatible with Texas Instruments' TM 990 microcomputer family, and ASC1081 analog output boards are operated with a single instruction.

Analogic Corp, Audubon Rd, Wakefield, MA 01880 achieves this versatility by offering memory-mapped and CRU (communications register unit) interface operation; the system can be used to serially receive converted data. In memory-mapped mode, each converter channel appears to the processor as a unique memory address. All modes of operation are selectable under program control.

With the analog input board, the processor addresses the memory location initiating the conversion, and then enters a series of wait states until conversion is complete. The processor takes these data, finishes operating on them, and stores the result in another memory location.

The board is built around the company's MP6812 DAS; it incorporates 16 single-ended and 16 pseudo-differential or 8 true-differential channels, expandable to 64 and 32, respectively. Components are a 12-bit successive approximation ADC; differential buffer with two gains giving 0 to 5, 0 to 10, ±5, and ±10-V input ranges; sample/hold circuit; and onboard dc-dc converter for 5-V supply operation.

The output board is configured as write-only memory. Any memory reference instruction can initiate a D-A conversion on a selected channel. No wait states are involved, and the DAC can be updated as desired, limited only by the computer's cycle time and DAC settling time.

It offers four channels of 12-bit digital output; 0 to 5, 0 to 10, ±5, and ±10-V output ranges; a 10-V/µs output slew rate; 4 to 20-mA current range; and compatibility with industrial control ISA type 4 Transmitter Class L and U requirements.

Circle 436 on Inquiry Card

Peripheral Circuits Cover Interface Needs of 8080-Class µComputers

Two intelligent devices that can operate most manual input and display output peripherals when given simple commands by an 8-bit microprocessor are claimed by Intel Corp's Microcomputer Components Div, 3065 Bowers Ave, Santa Clara, CA 95051 to be the first peripheral circuits to cover the "human interface" or "man-machine" peripheral interface and control needs of CPUs such as the 8080A and 8085 microprocessors, and the 8048 single-chip microcomputer. Attaching directly to the 8080/8085 system bus, the 40-pin devices begin a series of single-chip LSI subsystems with logic functions dedicated to operation of specific classes of peripherals. IBM-compatible controllers for floppy discs and communications links are planned.

The 8275 programmable CRT controller and 8279 programmable keyboard/display interface reduce system component counts and free execution time that is normally consumed in peripheral operating overhead, allowing enhanced system program processing and control functions. Thus, the microprocessors can operate at high throughput.

The 8275 CRT controller operates most raster-scan displays, including CRT screens and self-scanning types of display panels. In addition to scan control and operation of character-generator ROM, the chip handles refreshing, transfer of data from main memory, limited graphics generation, cursor control, lightpen detection, and other auxiliary functions.

Programmable display format and control functions are governed by simple program commands transmitted to the chip over the system bus by the CPU. Formats vary from a single character up to 64 rows of 80 characters, and up to 16 horizontal lines/row.

The device buffers two rows of data on the basic chip and couples to an 8257 programmable DMA controller for DMA, using it to load the buffer memory from main memory at high speed.

The 8279 keyboard/display interface handles control applications, and can be combined with the 8085 and 8048 processors to build a range

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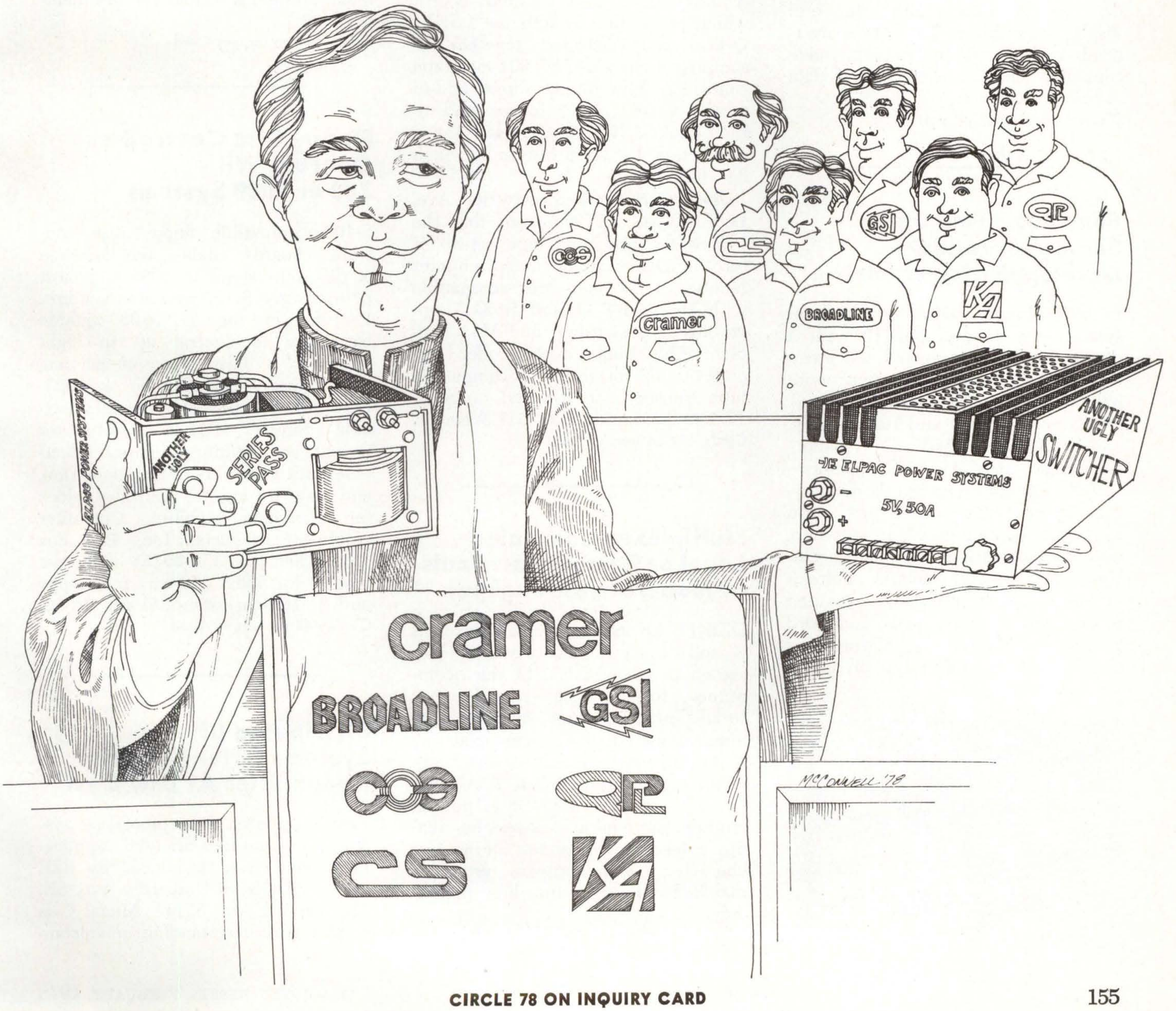


of systems with as few as two to four chips. It can be programmed with a few command words to operate a 64-key keyboard and up to 32 numeric or 16 alphanumeric character readouts.

Electromechanical, Hall effect, and ferrite keyboards can be operated by the chip, as can LED, incandescent, or other displays. The keyboard portion interfaces up to 64 sensors or random switches, and the display interfaces up to 128 discrete indicators, alarms, and on/off output devices.

Built-in functions replace subroutines. For the keyboard these are buffering up to eight bytes of input data, scanning, debouncing, 2-key or N-key rollover, error detection, encoding, and decoding; for the display, buffering 16 bytes of output data and handling multiplexing and display refreshing. The CPU's overhead is reduced by issuing mode commands and transferring I/O data at convenient times.

Circle 437 on Inquiry Card

Four Z80 Based Units Serve As Product Development Systems

Four Z80 based product development systems—the Microsystem/12 with a dual cassette tape unit and 16k memory, /15 tape-based system with 32k RAM, /20 with dual 5" (13-cm) minifloppy disc unit and 16k memory, and /30 with dual 8" (20-cm) floppy disc unit and 16k memory—include a CPU with up to 56k memory, high speed 960-character CRT, ASCII keyboard, operating system software, and documentation. Optional accessories and software include in-circuit emulator, line printers, extended BASIC, BASIC compiler, RDOS, and word processor. Futuredata Computer Corp, 11205 S La Cienega Blvd, Los Angeles, CA 90045 also supplies low cost plug-in modules to permit the systems to be converted to 8080 or 6800 processors.

Features include two RS-232 serial ports, 8-bit parallel TTL I/O port, real-time clock, bootstrap in P/ROM, memory write-protect under software control, 8-level vectored interrupts, DMA capability, and complete disc and tape operating systems with monitor, debugger, editor, assembler, and copy utility.

Circle 438 on Inquiry Card

Imbedded Mag Tape Controller Operates With LSI-11 μComputer

A hex board and a dual board, which plugs directly into the LSI-11 Q-Bus, are packaged together to comprise the model TFC 901 mag tape controller. This allows direct add-in to the Quad LSI-11 format and to the dual LSI-11/2 format. Interconnection between boards is via a flat ribbon cable.

Aviv Corp, 300 Sweetwater Ave, Bedford, MA 01730 claims that the unit is the first mag tape controller for the DEC LSI-11 microcomputer family; it is software compatible with DEC's RT-11 and RSX-11 operating systems using the TM11 handler. The buffered controller operates with all industry compatible tape transports in a speed range of 12.5 to 125" (31.75 to 317.5 cm)/s.

Circle 439 on Inquiry Card

Multiplexer Connects Local or Remote Terminals at Moderate Throughput

DZK-11 asynchronous multiplexer is a software-controlled interface designed to connect LSI-11 microcomputers to multiple asynchronous serial lines. Features of the communications device, developed by K. O. Mair Associates Ltd, 346 Richmond Rd, Ottawa, Ontario K2A OE8, Canada, include four lines/plug-in module, automatic answer on dial up, a 64-char silo buffer for no lost characters, and software programmable baud rates and line parameters.

Circle 440 on Inquiry Card

Add-on RAM Board Delivers 16k to 65k for Development Board

Memory capability of the SDB-80 Z80-based software development board can be upgraded with the addition of the RAM-80B (MK 78108) memory board. The board from Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006 uses their MK 4116 RAM to offer 16k, 32k, 48k, or 65k bytes of RAM. As a combination memory and I/O expansion board, it also provides strapping options.

Four 8-bit I/O ports from the two onboard MK 3881 Z80 PIO circuits are each fully TTL buffered and have two handshake lines. Logic for page mode operation permits up to 1M bytes to be used in a single SDB-80 system. An expansion package contains eight additional RAMs plus a blank strapping header for the memory board.

Circle 441 on Inquiry Card

Floppy Disc Controllers Operate With Z80 or 8080 Systems

S-100 compatible floppy disc controller boards enable the addition of disc subsystems to 8080 and most Z80 powered S-100 computer systems. Features of the FDC-108 include capability to control up to eight drives in a daisy chain connection, all necessary software in a 1024-byte onboard P/ROM, jumper selectable addresses, IBM 3740 soft sector format compatibility, jumper selectable wait state for 4-MHz operation, and onboard crystal-controlled clock for maximum stability. Computer Hobbyist Products, Inc, PO Box 18113, San Jose, CA 95158 offers two models for 5.25" (13-cm) minifloppy and 8" (20-cm) standard size drives.

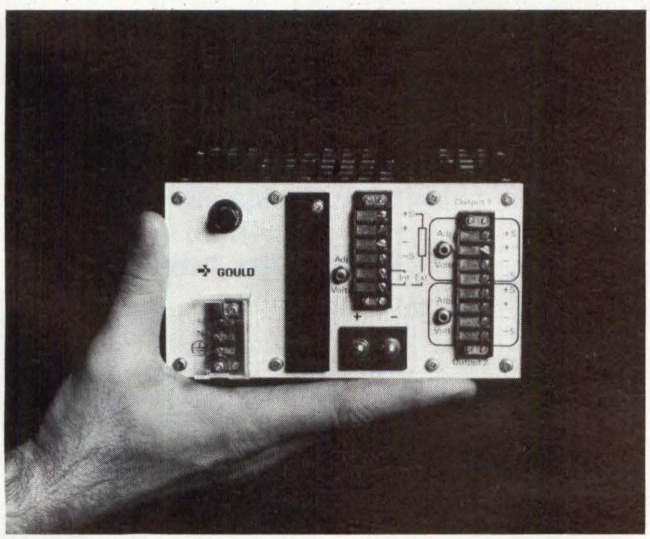
Circle 442 on Inquiry Card

Distributed DP Systems Offer Powerful Capabilities At Low Cost

Two distributed data processing systems for business-oriented applications have been introduced by R2E of America, 3406 University Ave, SE, Minneapolis, MN 55414. Micral C is a powerful, freestanding microcom-

The big switch

...is to smaller, lighter switchers.



The 100 watt MGT 5-20A: 7" x 6.4" x 3.5", 7.5 lbs.

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puter system that includes a dual minifloppy disc drive (160k bytes of storage each), CPU with up to 64k of RAM, magnetic tape units, CRT/keyboard, and several types of printers. Featuring a 920k-byte/s transfer rate and 75-ms average access time, the 10M-byte cartridge disc unit provides massive online file capabilities.

The Mical V system consists of a suitcase containing CPU with 32k bytes of RAM (expandable to 64k) plus 1k bytes ROM, keyboard and display offering 12 lines of 40 characters, alphanumerical 32-column printer, and minifloppy disc unit offering 160k bytes of random access storage. A second minifloppy disc unit, located outside the suitcase, can be connected to the system, as can a 30- to 180-char/s printer. It can be used for onsite data collection, file consulting, and processing for business and scientific applications. Power supplies are normal 220 V or car cigarette lighters (12 or 24 V).

Software for both systems includes business application BASIC language (BAL), with sequential and random access file management system; assembly language; FORTRAN IV compiler, and utilities. The Micral V supports all basic software of the Micral family.

Circle 443 on Inquiry Card

Cross Assembler for 9900 µProcessor Runs on 16-bit Host Computer

Relocatable cross assembler and linking loader for Texas Instruments 9900 microprocessor are available from MicroTec, PO Box 60337, Sunnyvale, CA 94088. Written in ANSI std FORTRAN IV, it operates on any computer with a word length greater than or equal to 16 bits, including most minicomputers.

The assembler features symbolic and relative addressing, constant generation, a macro facility, conditional assembly statements, and cross reference table listing option. The linking loader allows independently assembled relocatable object modules to be combined into a single absolute object module.

Circle 444 on Inquiry Card

Dual Z80A Based Microsystem Features 80k RAM Capacity

A high performance dual Z80A based multifunction workstation, the desktop Microterm II system features 80k RAM, dual 4-MHz processors,

and an interactive diskette operating system. The package also holds a 24 x 80-character 12" (30-cm) CRT, a 2200-char/s nonimpact printer, and single or dual minidiskettes. Internal printer, dual diskettes, and memory expansion beyond 32k are optional. An external printer is also available.

Benchmark tests conducted by Digi-Log Systems, Inc, Babylon Rd, Horsham, PA 19044 indicate that the system is faster than 21 other microcomputers tested. User software for the system, designed for the volume user OEM, can be developed directly from the keyboard in either assembly language or extended BASIC.

Circle 445 on Inquiry Card

Low Cost Data Cassette Is Developed for Home Computing Users

The Pilon-30™ data cassette, providing orders-of-magnitude improvement over audio cassette data integrity, is designed with an extra large pilon-coated pressure pad rather than a fiber pad. The pad provides more uniform tape-to-head contact, eliminates dropout data errors, and assures smooth movement because of low friction. The pad leaf spring of ordinary cassettes has been replaced with an energy absorbing foam spring to reduce flutter.

The magnetic coated tape selected by PerCom Data Co, Inc, 4021 Windsor, Garland, TX 75042 gives low noise, low dropout, and splice free operation. An additional advantage of the cassette is a 5-screw housing that precludes case deformation during assembly.

Intended for home computing uses, the cassette holds 150 ft (45.7 m) of tape, and retails for $2.49. Data storage is 50k bytes of 30-byte/s data or 200k bytes of 120-byte/s data.

Circle 446 on Inquiry Card

Microcomputer Provides Low Cost Hardware and Software Development

Design engineers, experimenters, and hobbyists now have an F8 development board (model 1080) consisting of an F8 CPU, Fairbug PSU, 2k x 8 RAM, 2.0-MHz crystal, and interfacing components on an 8 x 13" (20 x 33-cm) PC board. Comptronics, 19824 Ventura Blvd, Woodland Hills, CA 91364 designed the board for low cost hardware and software development and evaluation. The board contains a buffered address and data bus to an S-100 memory expansion connector, and provides sockets for 4k of 2708 memory. I/O consists of 32 bits arranged in four 8-bit ports.

Circle 447 on Inquiry Card

Microcomputer Features Onboard Floppy Disc Interface

The MLZ-80 general-purpose microcomputer board introduced by Heurikon Corp, 700 W Badger Rd, Madison, WI 53713 provides 4k of RAM, and up to 8k of ROM with oncard floppy disc interface for standard or minifloppy disc drives. Features include Intel SBC bus compatibility, dual serial asynchronous/synchronous ports with separate software controllable baud rates to 19,200, RS-232-C or current loop interface, four 8-bit parallel ports, and DMA logic.

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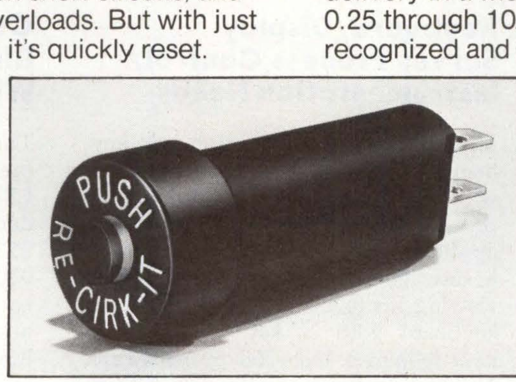

Re-Cirk-It can only be electrically tripped. It can't be turned off, and it can't be held on against a fault.

The Re-Cirk-It protector is cost-competitive with fuses and fuseholders, installs in the same panel space as a conventional ⅝"-diameter fuseholder, and is attractive enough to be on your front panel.

This new protector is available for quick delivery in a wide range of current ratings from 0.25 through 10A. And, of course, it's UL-recognized and CSA-approved as a component circuit protector.

Before you (or your customer) blow another fuse, send for a sample. Heinemann Electric Company, Special Re-Cirk-It Offer, P.O. Box CN 01908, Trenton, New Jersey 08608.

*Other ratings available under this offer on special request. Offer expires December 31, 1978

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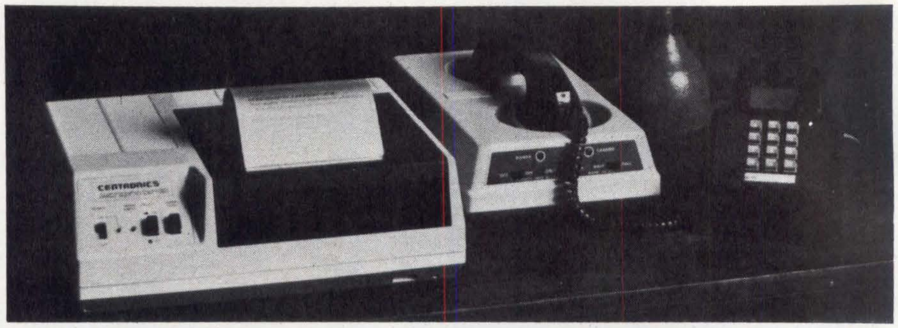
4k and 8k RAM Boards Are Compatible With 80/10 Microcomputers

Low power static RAMs are the basis of the 4k and 8k memory boards released by Electronic Solutions, Inc, 7969 Engineer Rd, San Diego, CA 92111. Compatible with Intel's SBC 80/10 and National's BLC 80/10 microcomputers, the boards feature a memory cycle time of 630 ns; typical power consumption for 8k board is 9.5 W. Single power supply is 5 Vdc, ±5%. Address selection is done via jumpers.
Circle 449 on Inquiry Card

6800-Based μProcessor System Is Designed for Control/Data Processing

The PLS-868 single-card, programmable logic system executes all instructions of the 6800 microprocessor, suiting it for small-scale data processing use and for high speed bit manipulation in control applications. RAM or I/O can be jumper set for use with the 6800's Memory Direct instructions. Pro-Log Corp, 2411 Garden Rd, Monterey, CA 93940 has provided the card with 1k of RAM (with sockets for an additional 1k), and sockets for up to 8k of EPROM. Also included are a crystal clock, two interrupt inputs, power-on and external reset, and three 8-bit output and two 8-bit input ports, both expandable to eight ports. System operates from a 5-Vdc supply and is fully TTL compatible.
Circle 450 on Inquiry Card

Serial Interface Allows Use of Microprinter As Remotely Placed Printer



For use as remotely placed message printer, Centronics Microprinter S1 with serial interface allows user selection of baud rates, parity, and number of stop bits

Aimed at home, hobby, and other microprocessor markets, the Microprinter-S1 features a serial interface suiting it for use in diagnostic systems, CRT hardcopy applications, industrial instrumentation, and demand message printing; however, since many CRT terminals require the RS-232 interface, the printer should see frequent use as a remotely placed message printer.

Featuring a 7-bit serial RS-232 interface and standard ASCII 96-character set, the printer operates at from 50 to 9600 baud. It produces copy on aluminum-coated paper by discharging an electric arc to penetrate the coating. The printed characters are impervious to light, temperature, and humidity.

Production units will be available from Centronics Data Computer Corp, Hudson, NH 03051 during the first calendar quarter of 1978. Features include a 192-char FIFO buffer; 5, 10, or 20 char/in; 96-char u/lc printout; and either 115- or 230-V configurations. The factory set 1200 baud, no parity, and one stop bit are user selectable.
Circle 451 on Inquiry Card

Incremental X-Y Plotter Interface For LSI-11 Microprocessor Bus

A parallel interface to Houston Instruments, Calcomp X-Y plotters, or equivalents from the DEC LSI-11 microprocessor bus is provided by the MLSI-XYV-11 dual-module interface board that includes data, control, and status registers. Adjustment of a potentiometer controls stepping speed. MDB Systems, 1995 N Batavia St, Orange, CA 92665 has supplied the board with jumper selection of 5 or 12 V to provide power to eight control lines through onboard differential of TTL line drivers, permitting plotter operation at distances up to 100 ft (30 m) from the LSI-11 bus.
Circle 452 on Inquiry Card

Keyboard/Display Serves Process Control/ Instrumentation Needs

Model 150-406, a peripheral keyboard/display unit, interfaces easily with most microprocessor systems for process control and instrumentation applications. Features include a full hexadecimal 8-digit display with viewing up to 20 ft (6 m), a 32-key keyboard with N key rollover, and key debounce included in hardware. Amatech Instrumentation, Inc, 5 Marc Lane, Westport, CT 06880 is also offering an 8080A microprocessor interface software package.
Circle 453 on Inquiry Card

Card Interfaces Floppy Disc System to LSI-11 With More Capabilities

The 210-LIIA card for interfacing the 210 floppy disc system to DEC's LSI-11 microcomputer has been introduced by Data Systems Design, Inc, 3130 Coronado Dr, Santa Clara, CA 95051. Increased features include a hardware bootstrap, DMA logic, and bus termination circuitry. The combination of features of DEC's REV-11 card with those of the company's 210-LII interface card eliminates the need for the DEC card and saves one Q-bus slot in the LSI-11. □
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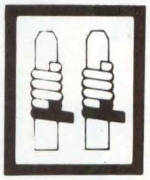

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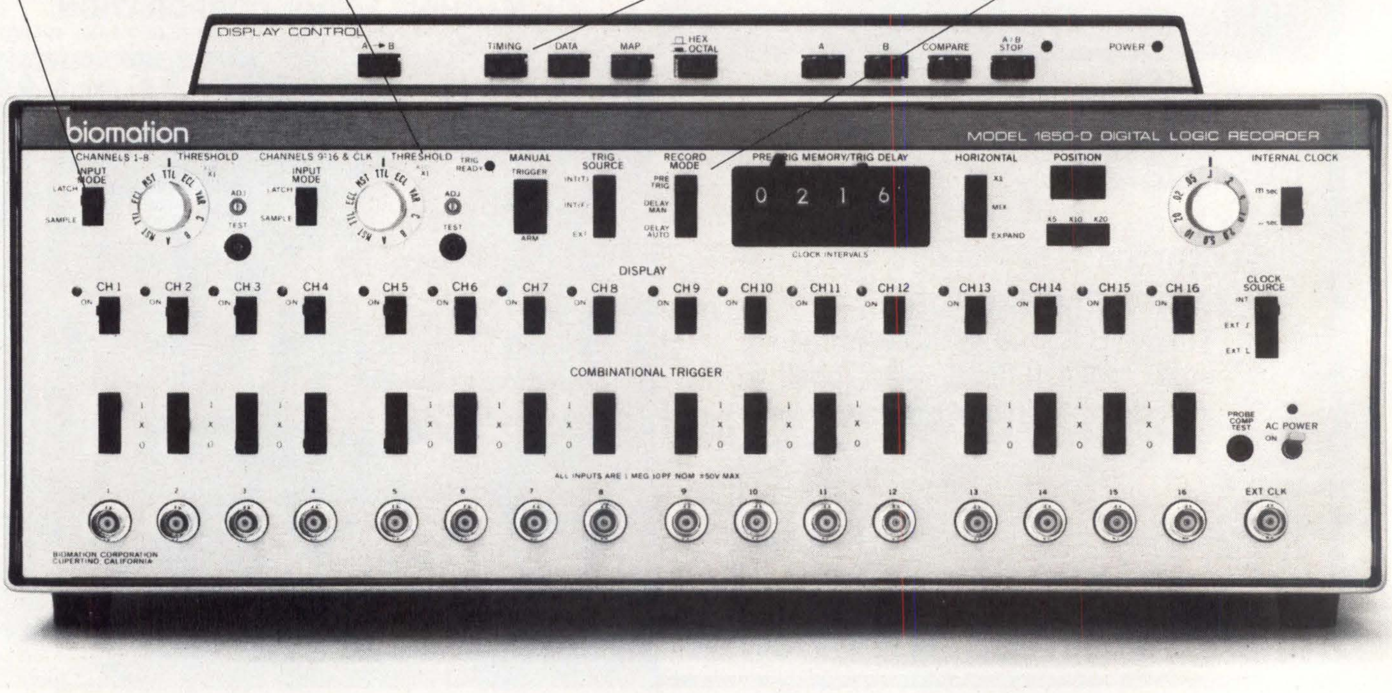

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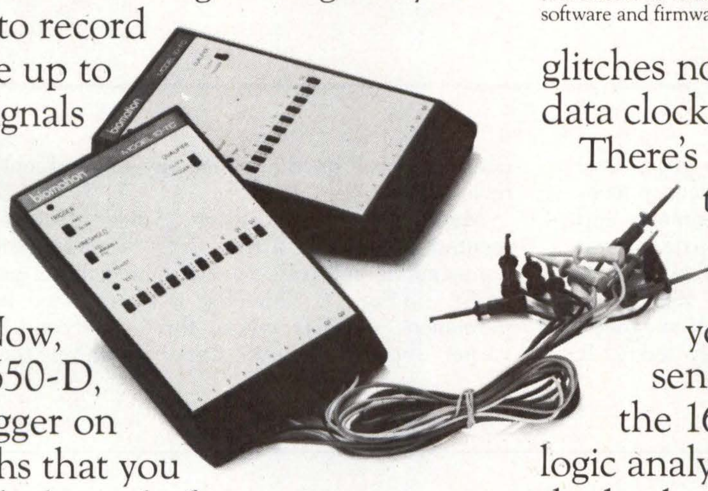

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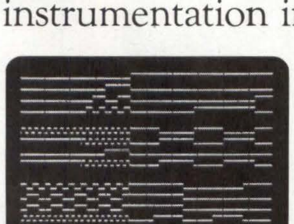

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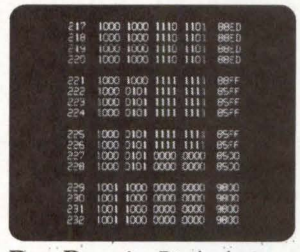

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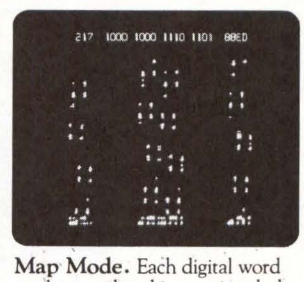

Map Mode. Each digital word can be translated into a singularly positioned dot in this graphic representation of recorded data. Especially useful for spotting illogical or illegal memory addresses.

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AROUND THE IC LOOP

MAGNETIC BUBBLE MEMORY DEVICES AND APPLICATIONS

Eric R. Garen

Integrated Computer Systems, Inc
Santa Monica, California

Many articles published during the last two years have presented the principles of magnetic bubble memory technology, and the tradeoffs between that technology and other memory technologies, including metal-oxide semiconductor random-access memory, charge-coupled devices, and various rotating magnetic memories (eg, Ref 1 and 2). This month's column describes the state of magnetic bubble memory devices available commercially today. It does not dwell on the technology itself except for a short review.

Magnetic bubble memory (MBM) devices are implemented by growing a thin sheet of magnetic garnet on a nonmagnetic substrate [gadolinium gallium garnet (GGG or G^3)] (Fig 1). This chip is then placed between two permanent magnets whose flux is perpendicular to the garnet sheet. Magnetic domains within the sheet are

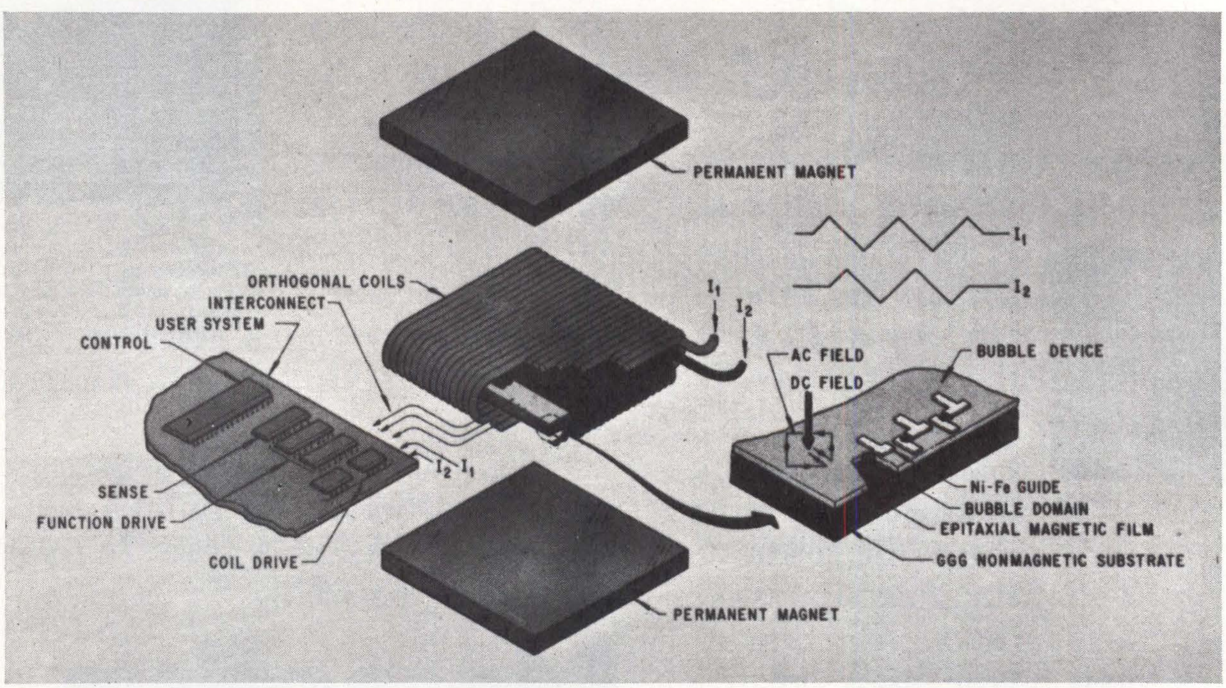

Fig 1 Construction of magnetic bubble memory (MBM). Bubbles form as flux reversals on nonmagnetic substrate positioned between two permanent magnets. They are then propagated in shift register fashion by changes in magnetization of permalloy magnets above substrate (Courtesy Texas Instruments Inc)

therefore aligned in the direction of this external field. However, by introducing a small localized magnetic flux in the opposite direction (eg, by a tiny current loop above the garnet surface), a local flux reversal is introduced in the magnetic garnet. The external field is strong enough to contain this flux reversal as a small cylindrical "bubble," but is not so strong that the bubble will be annihilated once the current in the "generating" loop is removed. The bubble is then propagated in shift register fashion by changing the magnetization of tiny permalloy magnets on top of the garnet to attract the bubble from one permalloy magnet to another.

Many magnetic patterns have been proposed, but the T-I bar configuration has been most used to date (Fig 2). By rotating an external magnetic field, the flux within the permalloy pattern rotates so that bubbles are repeatedly attracted first to the right end of the T-bar, then to the top of the "I", next to the left of the "T," and then to the center of the "T." To achieve the rotating magnetic field, current is cyclically reversed in two perpendicular coils that surround the chip (Fig 1).

Binary information is represented as the presence or absence of a bubble. To read the data, the bubbles are detected by passing them across a permalloy strip whose magnetoresistance is changed by the bubble's field. This resistance makes up one leg of an external resistor bridge network, and the change in resistance creates signal differentials of several millivolts which are amplified, level detected, and converted to TTL levels by external circuitry.

One of the first commercially available MBM devices is Texas Instruments Inc's TIB-0103. This device stores 92,304 bits on a single chip inside a 14-pin dual-in-line package 1.0 x 1.1 x 0.4" (2.54 x 2.8 x 1 cm) in size. Organization of the data is shown in Fig 3. Data are stored in 157 "minor" loops of 641 bits each, and are written and read via a "major" loop which transfers data from a "generate" station to the minor loops, and from the minor loops to a detection track.

While more complex than a single shift register organization, this major/minor loop configuration substantially reduces access time. A maximum of 1042 shifts is required to access data (640 maximum to move the minor loops into position, plus 402 to move data from the top of the most remote minor loop to the detector). Shifting is performed at 100 kHz; therefore maximum access time is 10.4 ms and average access time is 5.2 ms. (Note that maximum access time for a single 92k register shifting at the same rate would be nearly 1 s.)

A further advantage of this configuration is that a chip with a few defective minor loops is still generally usable. MBM devices are fabricated using fine geometries which make it difficult to manufacture perfect units. In order to enhance production yields and achieve correspondingly lower costs, devices with up to 13 defective minor loops out of the 157 on the chip are considered acceptable. Therefore, the minimum data capacity of the remaining 144 good loops is 92,304 bits (144 x 641). Defective loops are determined at final test, and the resulting map is supplied to the end user so that the defective loops can be masked out in the memory system. The recommended approach is to store the map in a p/ROM. Each bit in a page of data would then be gated with the contents of the p/ROM, thus preventing bad data bits from reaching the data buffer.

Data are written into the major loop of the MBM via the generating current loop. Creation of a bubble constitutes a logic 1 and, conversely, the absence of a bubble is defined as a logic 0. The major loop is essentially a unidirectional circular shift register with parallel transfer capability to the top bit position of the 157 minor loops.

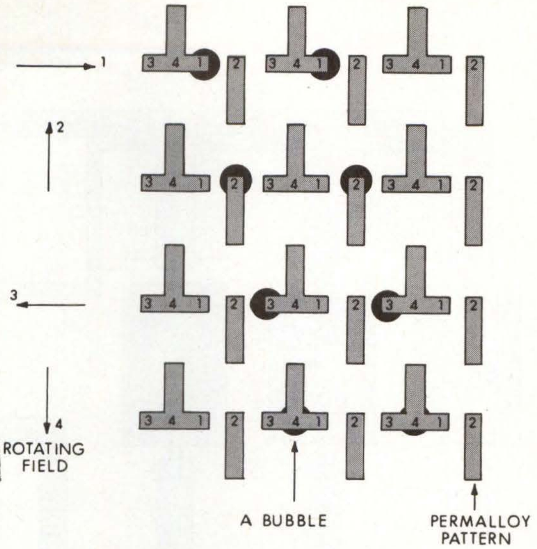

Fig 2 T-I bar MBM propagation technique.[1] As external magnetic field rotates, bubbles move through film medium controlled by field concentrations created by permalloy patterns. Field rotates counterclockwise for left-to-right propagation

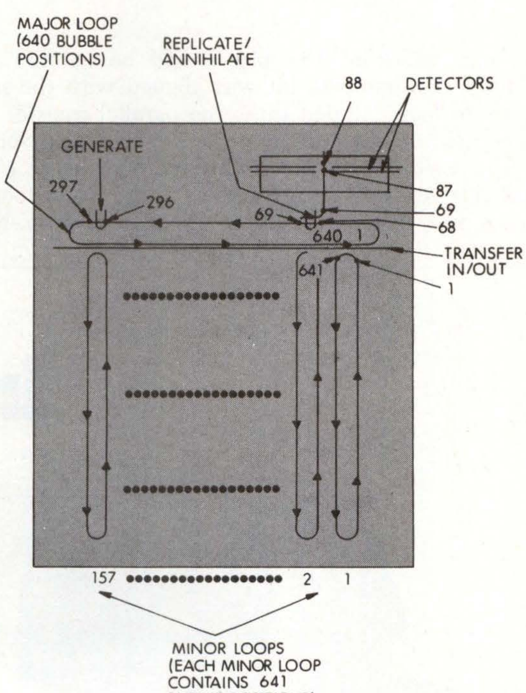

Fig 3 Major/minor loop architecture. Data are stored in 157 minor loops of 641 bits each and are written and read via major loop (Courtesy Texas Instruments Inc)

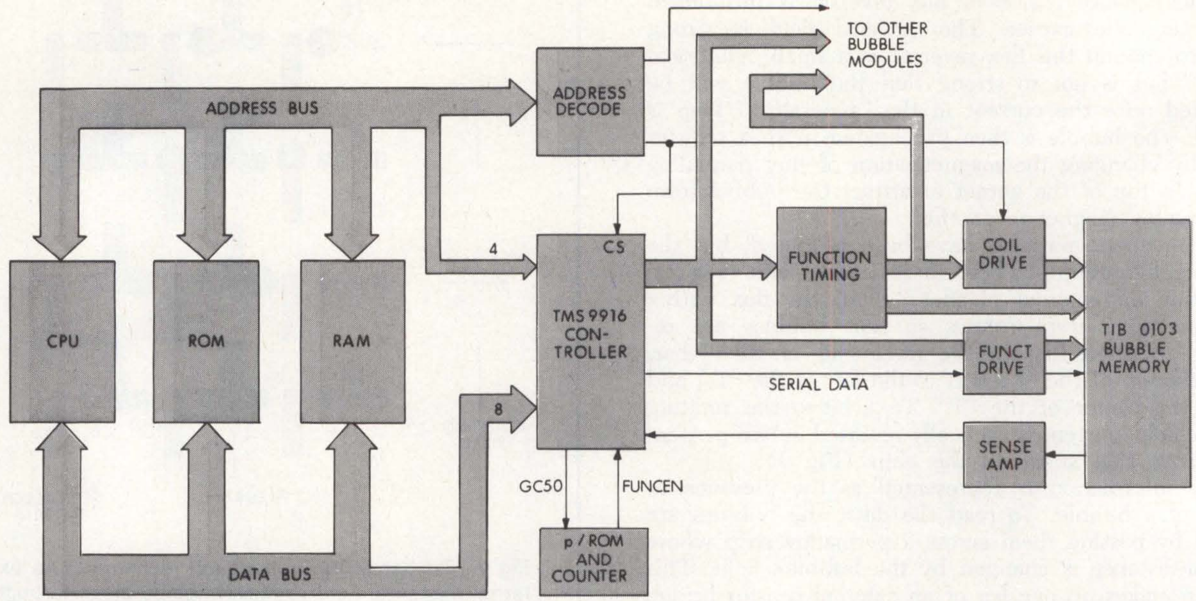

Fig 4 Block diagram of typical bubble memory interfaced to a microcomputer. Single controller handles entire system (Courtesy Texas Instruments Inc)

Thus, a data block of 157 bits would be entered and shifted until the first data bit was aligned with the most remote minor loop. At that time, the parallel transfer element would receive a current pulse which would set up localized magnetic forces on the bubble domains to effect the parallel transfer of all the bubbles in the major loop to the top bit position of the corresponding minor loop. Note that the input data must be expanded by inserting logic zeros in the bit positions where factory testing has revealed a defective minor loop to be present. The input data must also be expanded to provide a logic 0 between each input data bit, compensating for the data position created in the major loop between each minor loop due to the physical geometry of the chip. Once data are written into

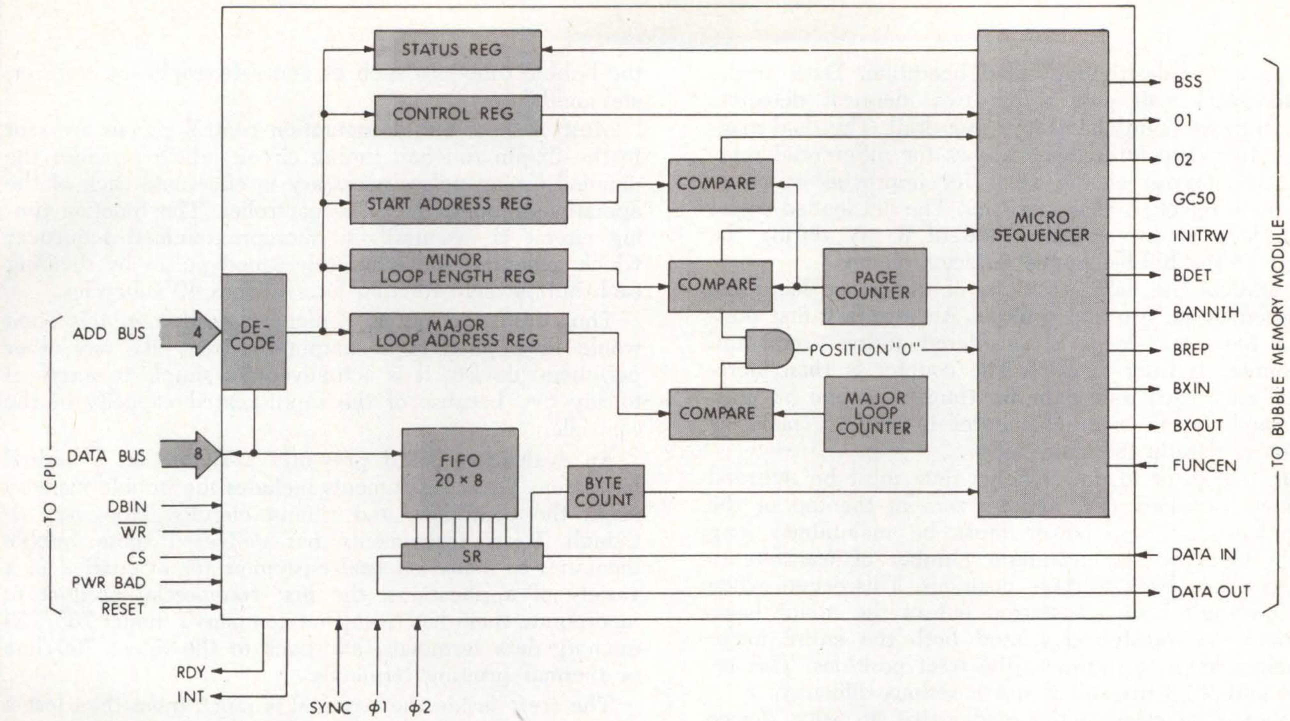

Fig 5 Simplified block diagram of TMS 9916 controller in Fig 4. Directly compatible with both 8080 and 9900 microprocessors, this controller interfaces MBM to most CPUs (Courtesy Texas Instruments Inc)

the MBM, new data may be written only after first removing the old data by doing a destructive read.

To accomplish a read operation, desired data in the minor loops are rotated until they are at the top position. Then they are transferred to the major loop by applying a current pulse to the transfer loop at the proper time. After that, the major loop is rotated 68 positions until the first data bit reaches the replicator. By adjusting the amplitude and timing of the pulse in the replicate circuit, the bubbles can then either be diverted to the detector track (from which they are eventually shifted into a guardrail and annihilated) or be duplicated both in the detector track for reading and in the downstream section of the major loop for transfer back to the minor loops in a "nondestructive" read operation. Data in the detector track will pass across two identical detectors before they are annihilated in a guardrail. The dual magnetoresistive detector scheme allows for differential sensing at the output of the MBM for improved common-mode noise rejection characteristics. The net loaded signal amplitude is in the neighborhood of 3 mV during the passage of the bubble in the detector region.

To address the data, positions of the minor loops are monitored by an external counter. An arbitrary first position of the minor loops is considered address zero, and the counter is reset to zero. The counter is then incremented once each time data are transferred one bit position. Similarly, an external counter is used to track the position of data in the major loop.

Note that prior to power down data must be returned to known positions (eg, address zero at the top of the minor loops). Thus, power must be maintained long enough to allow the maximum number of transfers to bring the data back to these positions. This occurs when data have just been transferred out of the minor loops and must be transferred around both the entire major and minor loops to return to the reset positions. This requires only 12.8 ms and is not a serious difficulty.

It should be clear to the reader that an MBM device such as this one is not used as easily as an MOS RAM, which requires only external chip select circuitry. The MBM requires accurate current pulses for the generate, replicate, and transfer elements, as well as triangular waveform currents to each of the two orthogonal coils to create the rotating field. Furthermore, the addressing scheme and necessity to destructively read before write requires a sophisticated controller. However, this is not as difficult as it might seem, because most of the addressing and timing control functions are handled completely by special interface circuits designed specifically for this chip. A block diagram of a typical system is shown in Fig 4. Each individual 92k MBM module requires the following support ICs: one function driver, two coil drivers, one diode array, one RC network, and one sense amplifier. The entire system is controlled by a single TMS 9916 controller, which provides the user with a high level computer-compatible interface, together with a function timing circuit, which decodes the bubble control signals defined by the controller and performs the high speed control functions needed to operate the MBM devices.

The TMS 9916 controller is a 40-pin n-MOS circuit designed to interface the MBM to most CPUs (Fig 5), and is directly compatible with both 8080 and 9900 microprocessor systems. It keeps track of the locations of data in the MBM, and allows the CPU to perform byte-oriented I/O to the bubble memory system. Internally, the controller has 20 bytes of FIFO data buffering, so that the CPU is completely free from coordinating the timing of actual read and write operations. The controller simply buffers the data and interrupts the CPU when the entire transfer has been completed. It also has a multipage mode in which longer blocks of data can be accessed. In this mode an interrupt is generated after each byte is read or written until the transfer is complete. The controller is responsible for starting and stopping bubble shifting, maintaining page position information, and ensuring synchronization with the bubble module. At the proper bubble field rotation period, the controller generates signals to external circuits to enable or disable the bubble functions such as generate, replicate, transfer, and annihilate.

Most of these bubble operation control signals are sent to the 22-pin function timing circuit which provides the detailed timing pulses necessary to effectuate each of the operations requested by the controller. The function timing circuit is essentially a microprogrammed sequencer which generates the accurately timed pulses by dividing each bubble field rotation interval into 40 subcycles.

Thus, from the system designers standpoint, this MBM would be applied in a computer system like any other peripheral device. It is actually quite simple to interface to any CPU because of the sophisticated capacity of the controller.

An evaluation board presently available on a limited basis from Texas Instruments includes the bubble memory itself, the controller, and timing circuits. However, although Texas Instruments has delivered these bubble memories to many external customers for evaluation in a variety of applications, the first commercial product to incorporate them has been that company's model 765/763 memory data terminals, additions to the Silent 700 line of thermal printing terminals.

The MBM inside the terminal is much more than just a replacement for the cassette tapes found in other Silent 700 terminals. Because of the much higher speed of the MBM, complete file control becomes feasible. Thus the terminals actually include a small MBM operating system software package similar in capability to a disc operating system. These portable terminals are intended primarily for field data collection applications in which the operator would enter and edit data, store them in nonvolatile MBM, and then transmit them to a remote computer in high speed burst mode by playing back the files.

These terminals include dual-processor microcomputer systems: an 8080 to control the keyboard and printer, and a 9980 to control the bubble memory subsystem. Twenty thousand bytes of MBM are included (expandable to 80k bytes). The processors are programmed to allow the user to easily create, edit, play back, and delete files of data in the MBM. Complete file control and editing commands are initiated simply by pressing special function keys on the terminal so that the user is free from the tedious task of typing long command names.

Reasons for using MBM in this terminal are indicative of the expected applications for MBM over the next several years. Because their price is not expected to drop sharply until 1980 or beyond, one would expect initial applications to be those that require nonvolatility together with both fast access time and small volume. That is, first applications will be those for which neither RAM nor magnetic rotating media are attractive. As the system-level price drops toward an expected 15 millicents/bit, the range of applications will expand to replace more and more rotating memory, and to permit the development of new products that were simply not feasible without the compact, inexpensive, high speed, nonvolatile magnetic bubble memory.

References

1. J. E. Juliussen, "Magnetic Bubble Systems Approach Practical Use," *Computer Design*, Oct 1976, pp 81-91
2. E. J. Hoffman, R. C. Moore, and T. L. McGovern, "Designing a Magnetic Bubble Data Recorder, Part 1—The Component Level," *Computer Design*, Mar 1976, pp 80-81

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Research Program Results in Radiation Hardened MNOS RAMs with Fast Write Speeds

Random-access memory integrated circuits with write speeds 300% faster than common metal nitride oxide silicon electrically-alterable ROMs and 30 times harder to nuclear radiation than commercial integrated circuits have been developed and delivered by Sperry Rand Corp. Each 256-bit memory has a write cycle time of 2.8 μs, read access time of 1.0 μs, and data retention of 24 hours, even if power is removed from the chips. Longer write periods yield substantially longer retention periods. The memory circuit is operational for a minimum of 10^{11} clear write cycles.

These advanced nonvolatile semiconductor circuits were developed under a contract from the U.S. Air Force Weapons Laboratory and the Defense Nuclear Agency. The research program, started in 1966, was structured to develop a radiation-hardened MNOS RAM IC which could be used as a scratch or data collection memory in applications where it must survive the disabling effects of severe nuclear radiation environments. Flash x-ray tests were conducted in the Air Force Weapons Laboratory.

Program participants were the Sperry Div, Great Neck, NY; the Sperry Research Center, Sudbury, Mass; and the Sperry integrated circuit facility, St Paul, Minn. Details on performance of the radiation-hardened MNOS RAM circuits were presented at the IEEE Nonvolatile Semiconductor Workshop in August of 1977.

TABLE 1

SR 2256 Power Consumption*

Mode	Nominal Voltages ±15, ±5	Reduced Voltages +15, −10, ±5
Standby	10.7 mW	10.7 mW
Read	780 mW	430 mW
Clear	780 mW	430 mW
Write	710 mW	380 mW
Power Down	0 mW**	0 mW**

*Measured at 25°C
**Added access time would be required

TABLE 2

Radiation Test Results

Transient Flash X-Ray	
Read Disturb*	4×10^8 rads/s
Write Disturb	2.4×10^{11} rads/s
Bit Survival	10^{12} rads/s
Total Dose Hardness**	
No Parameter Change	1×10^5 rads
Degraded Access Time	2×10^5 rads
Failure	3×10^5 rads

*In read disturb test the memory was read 10^6 times before x-ray pulse was fired
**Biased and cycling in Co60 cell. Source—Air Force Weapons Laboratory

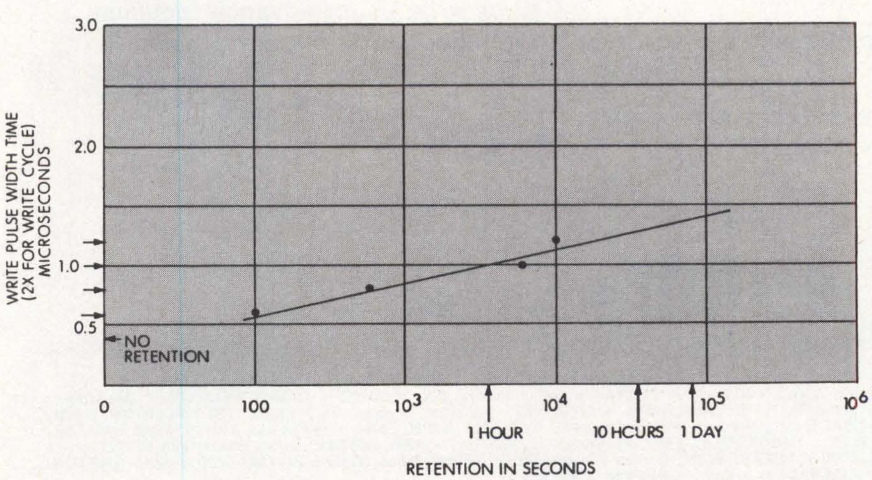


Fig 1 Retention vs write speed on a radiation hardened MNOS IC

Characterization of the SR 2256 chip required chip exercise with patterns, write speeds, and access times that were different from those for commercial memories and over longer periods of time. A Macrodata Memory Exerciser was used to run a high speed program across the full memory chip and acquire a pass or fail condition. Write period and read access time conditions for the test were initially loaded onto a personality card. A minicomputer, used to sequence the test from one access time to another and collect a block of pass/fail conditions, also acted as an executive controller to interleave characterization, retention, and endurance stress programs.

Write cycle times which would hold data for 10 min were typically 1.8 to 2.0 μs. A typical write cycle time of 2.6 to 2.8 μs would be required for 24-h retention.

Fig 1 shows what the minimum write speed could be for different retention times on a given device. If 100-s retention were acceptable, this device would write with a 1.4-μs write cycle. Similarly, for 55-h retention, a 3.5-μs write cycle was typically required. That type of data could allow a user on a cycle to cycle basis to store data for longer or shorter periods.

Typical power consumption at 25°C for different modes of operation of the MNOS RAM chip is shown in Table 1. Since only the row of chips which is enabled will consume read or write power, system power is usually driven by the standby power level.

Radiation data at cobalt 60 and flash x-ray sources was taken by personnel at the Air Force Weapons Laboratory (summarized in Table 2). The read disturb x-ray pulse was placed at the worst case point in the

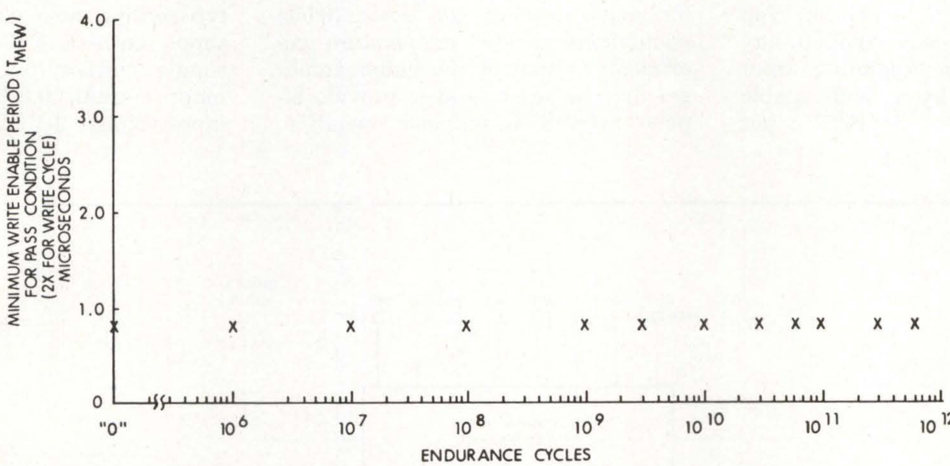


Fig 2 Endurance data for minimum write enable period. Endurance stress was for 2.2-μs write cycle at 30 V with alternating bit pattern on word 15. Test period was 23 days

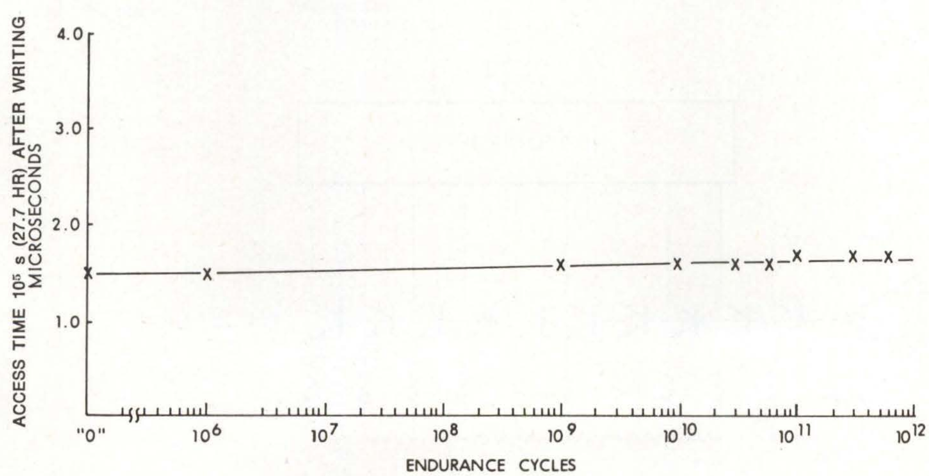


Fig 3 Endurance data after 27 hours of retention. Write cycle was 3 μs at 30 V for retention measurement. Endurance stress was same as for Fig 2

access period but after the memory array had been read 10^6 times. Total dose data was taken with the device in the test cell under bias and also cycling during the exposure. Higher hardness levels are expected with additional processing.

Endurance data are of great interest on MNOS RAM arrays. The automated tester was programmed to characterize and stress an array for a 23-day period. An alternating bit pattern was cleared and written into word 15 of the chip during the stress period. Periodically, the endurance stress was removed and the chip was characterized including retention for 27 h (10^5 s). Fig 2 shows that no degradation occurred to the memory chip write cycle time after 6 x 10^{11} endurance cycles.

Fig 3 shows access time after 10^5 s of retention vs endurance stress. A very slight shift in access time occurred over this period. The array was still fully functional and usable at the end of the test.

Circle 350 on Inquiry Card

Entire µP-Compatible DAC Function Provided On Single Chip

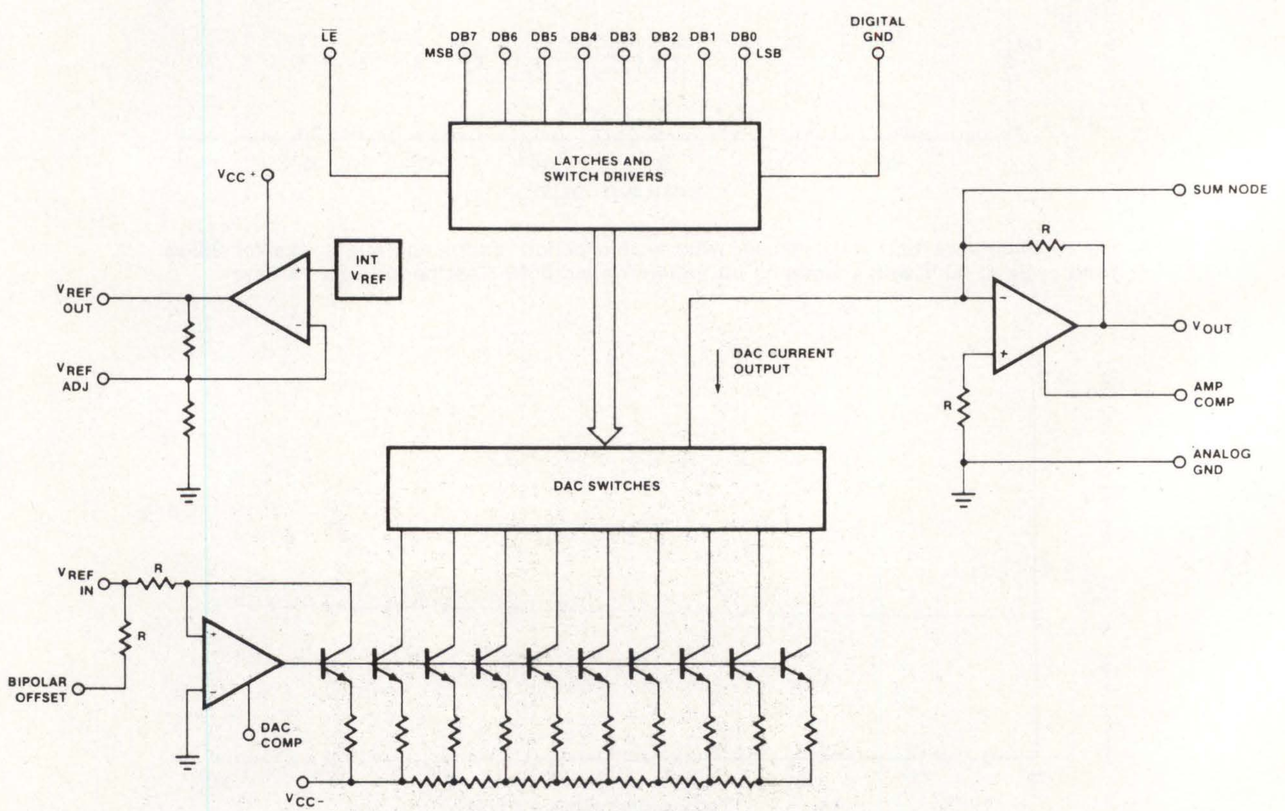
A complete 8-bit D-A converter subsystem, the NE5018 monolithic chip achieves microprocessor compatibility as the result of incorporating input latches controlled by a latch enable pin. In addition to the 8-bit input latch, the large-scale linear circuit includes a stable voltage reference (5 V nom), a high slew rate buffer amplifier, and a DAC.

The voltage reference may be externally trimmed with a potentiometer for adjustment of full scale, while maintaining a low temperature coefficient. Output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

Data and latch enable inputs (Fig) are ultra-low loading for easy interfacing with all logic systems. Latches appear transparent when the $\overline{LE}$ input is in the low state; when $\overline{LE}$ goes high, the input data present at the moment of transition are latched and retained until $\overline{LE}$ again goes low. This allows compatibility with 2650, 8080, and other popular microprocessors.

Absolute maximum ratings of this device from Signetics, 811 E Arques Ave, Sunnyvale, CA 94086 include 18-V positive power supply, −18-V negative power supply, 0- to 18-V logic input, 5-mA reference input current, 800- or 1000-mW power dissipations, −55 to 125 or 0 to 70°C operating temperature ranges, and −65 to 150°C storage temperature range.

Dc electrical characteristics include 15-V typ positive power supply, −15-V typ negative power supply, ±0.19% max relative accuracy, 2-µs typ settling time, 8-mA typ positive supply current, −10-mA typ negative supply current, 5-µA typ logic "0" input current, 0.8-V max logic "0" input voltage, 2-V min logic "1" input



Block diagram of Signetics microprocessor compatible, single chip DAC subsystem. All input latches are controlled by latch enable pin ($\overline{LE}$). Ultra-low loading of data and latch enable pins results in easy interfacing with all logic systems

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CIRCLE 86 ON INQUIRY CARD

voltage, and 400-ns typ latch enable pulse width (300 ns min). Short circuit protection for both amplifier and voltage reference is incorporated on the chip.
Circle 351 on Inquiry Card

Schottky 4-Bit Register Uses 75% Less Power

Typical clock-to-output delay offered by the Am25LS2518, 4-bit Schottky register is 18 ns, 55% longer than that of the high speed Am25S18—but with 75% less power consumption. Available from Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086, the device has both 3-state and standard TTL outputs.

It can be used in computer or computer peripheral equipment as an address register, a status register, or an instruction register, as well as for various other data or microword register applications. It is said to be suited for real-time signal processing systems where the standard continuous outputs are used in a recursive or nonrecursive algorithm. The 3-state outputs provide bus access to the data for interrogation as required.

Both DIL and flat packages, in 16-pin molded and ceramic hermetic configurations, will be available. The device is expected to be alternate sourced by Texas Instruments Inc as the 54/74LS388.
Circle 352 on Inquiry Card

64k VMOS ROM Now In Production

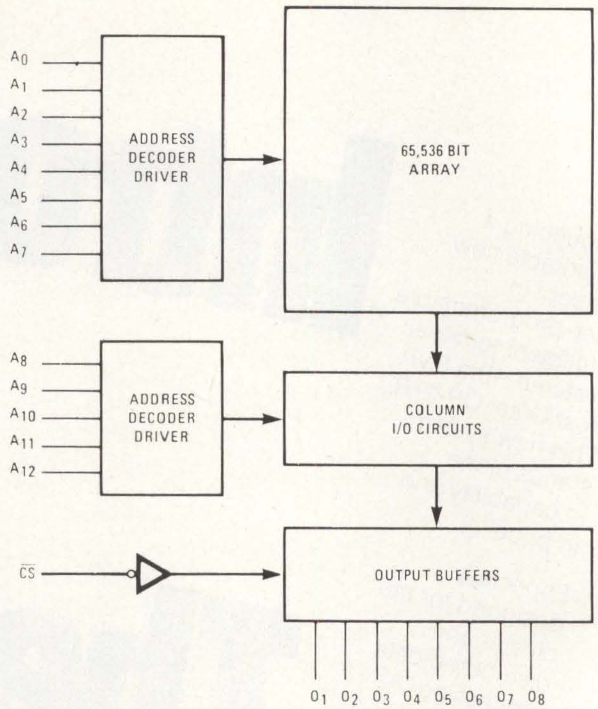
Evaluation units are now available of a 65,536-bit mask programmable ROM fabricated with VMOS technology. Configured as 8k words x 8 bits, the S4264 has a maximum access time of 350 ns; power requirements are 145 mW max. The device is fully TTL compatible on all inputs and outputs and has a single 5-V power supply. Three-state outputs ease memory expansion by allowing outputs to be OR-tied to other devices.

No clocks are required for operation; the device is fully static. No address setup times are required, thereby simplifying data access. Byte organization enables use of the device in microprocessor applications.

American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051 reports that deliveries have already begun on this 24-pin package. The high density device uses 5-μm design rules; yet chip size is only 169 x 177 mils, less than 0.5 mil²/bit. Price will be about $50 in quantities of 500.

Software adapted for the company's Microcomputer Development Center is available on diskette to assist design engineers in evaluating programs for fabrication into the ROM. Program patterns are computer drawn from data transferred to the MDC's floppy disc data storage. This software permits a full simulation of a design's performance as programs are being developed.

Circle 353 on Inquiry Card



American Microsystems 64k mask programmable ROM requires less than 30,000-mil² area. Inputs are directly TTL compatible, outputs are 3-state

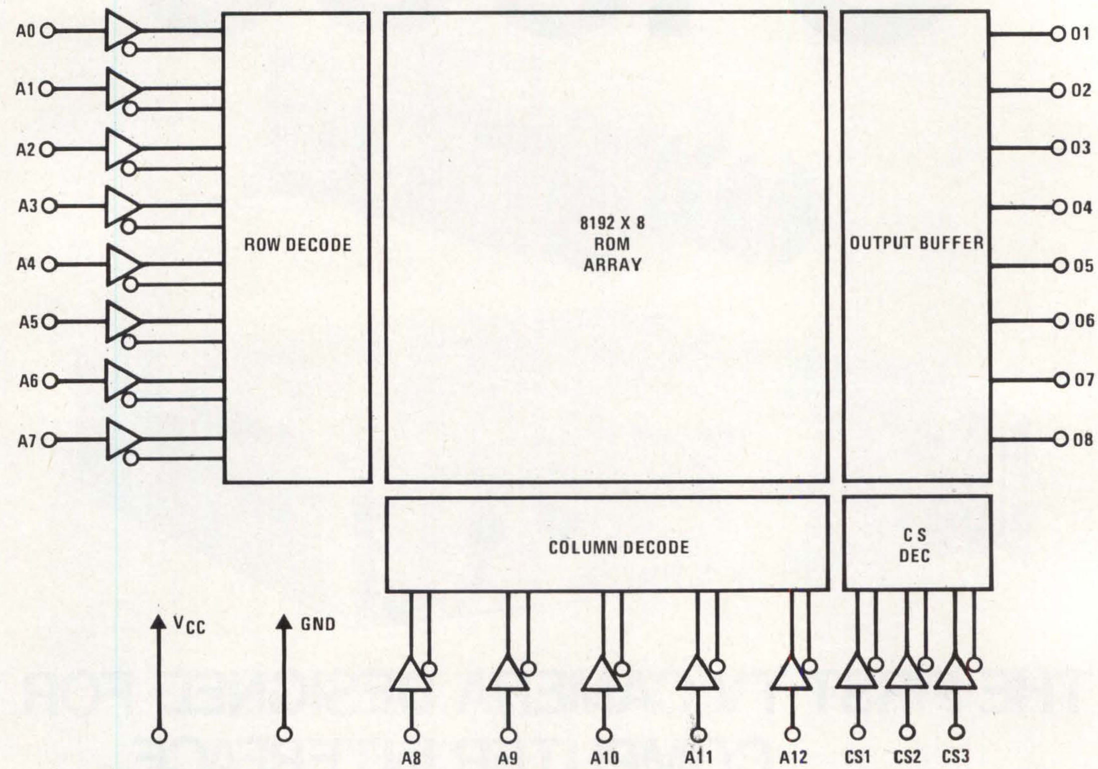
64k n-MOS ROM Available In Sample Quantities

MM5235, a 65,536-bit ROM array with a typical access time of 450 ns is now available in sample quantities. It is based on a self-aligning triple ion-implant metal gate n-MOS process and requires a single 5-V supply with less than 130-mA supply current; total power consumption is less than 700 mW.

Organization of the MAXI-ROM™ device from National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051 is 8k words x 8 bits. Operation is completely static and all inputs and outputs are TTL compatible.

Three programmable chip select lines allow simple memory expansion in a wired-OR configuration. Any combination of active high or low level chip select inputs can be defined by the designer; the desired chip-select logic level is fixed during the masking process. Chip area is about 39,000 mils², about five to ten percent larger than ROMs having half as many bits.

According to the company, use of these devices makes programming computers in such high level languages as APL or BASIC practical, and



Block diagram of National Semiconductor's 64k n-MOS ROM. Typ access time is 450 ns and total power consumption is less than 700 mW

high level language interpreters are possible in a single ROM. In volume quantities, the price is expected to be competitive with present designs. In sample quantities, the price of the commercial version is $32 each when purchased in lots of 250. In large volume, the price will be about 0.025 cent/bit.

16k Dynamic RAM Designed for System Storage Applications

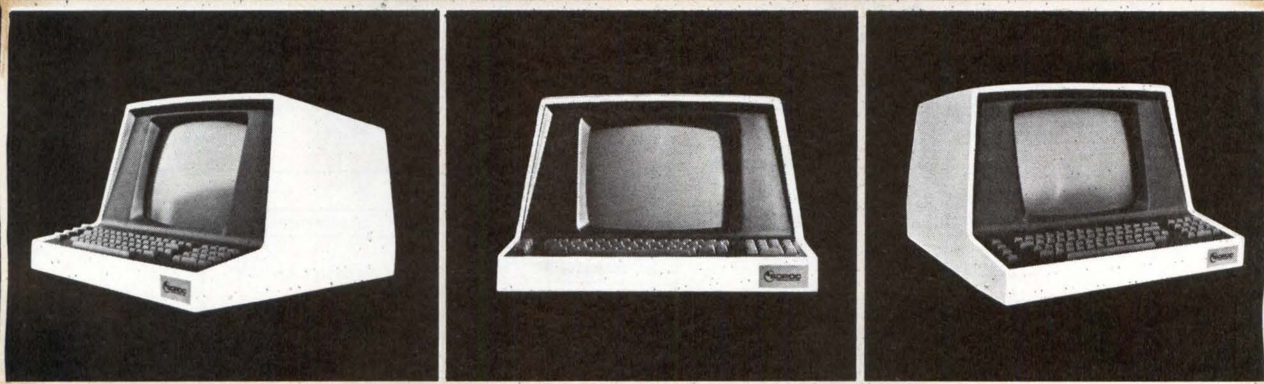
Z-6116, a 16k x 1-bit RAM from Zilog, Inc, 10460 Bubb Rd, Cupertino, CA 95014 based on that company's double-poly, n-channel, ion-implanted, silicon gate process, is pin compatible with Mostek's MK 4116 and Intel's 2117 dynamic memories. Three versions are available: the -2 with 150-ns access time and 375-ns cycle time, the -3 with 200- and 375-ns times, and the -4 with 250- and 410-ns times.

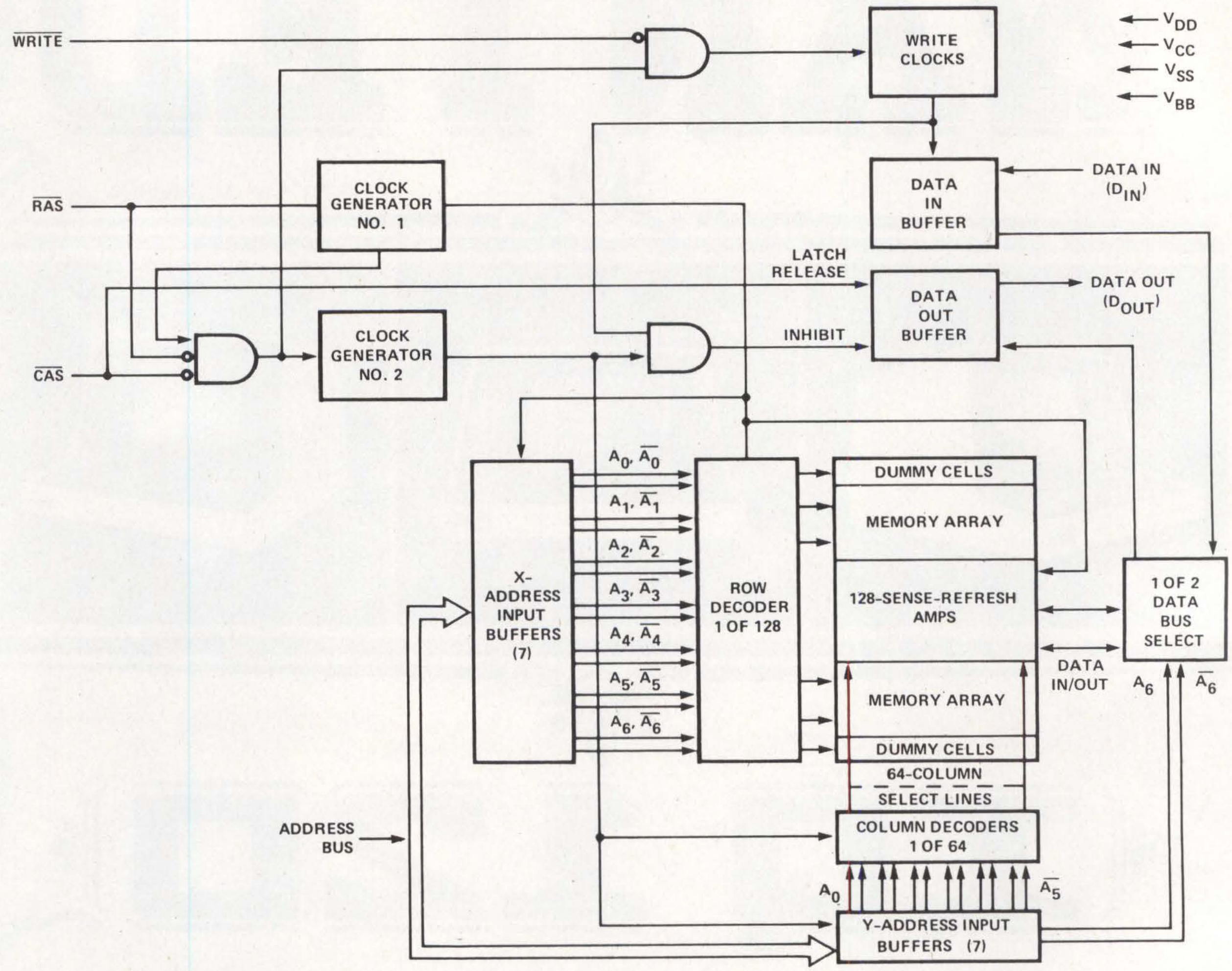
System oriented features include ±10% tolerance on all power supplies, onchip address and data registers which eliminate the need for interface registers, and direct TTL interface capability. In addition to the usual read, write, and read-modify-write cycles, the device is capable of delayed write cycles, page-mode operation, and row address strobe ($\overline{RAS}$) only refresh. Proper control of $\overline{RAS}$, column address strobe ($\overline{CAS}$), and $\overline{WRITE}$ also permits common I/O capability, 2-dimensional chip selection, and extended page boundaries.

Fourteen address bits required to decode one of the cell locations are multiplexed onto the seven address inputs (Fig) and latched into the onchip address latches by externally applying two negative going TTL level clocks. The first clock, $\overline{RAS}$, latches the seven row address bits into the chip; the second clock, $\overline{CAS}$, subsequently latches the seven column address bits into the chip.

Each of these external address strobe signals triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically such that the address multiplexing operation is done outside of the critical path timing sequence for read data access. Later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the row address hold time specification has been satisfied and the seven address inputs have been changed from row to column address information.

For data I/O an onchip register latches information on the data-in pin —whenever RAS is active and both





Internal block diagram for Zilog's 16k x 1 MOS dynamic RAM. All inputs, including clocks, are TTL compatible and are protected against static charge

$\overline{\text{CAS}}$ and $\overline{\text{WRITE}}$ have made their negative transitions. Whichever of these signals makes its negative transition later generates the strobe for the data-in register.

Page mode operation allows for successive memory cycles at multiple column locations of the same row address. This mode is achieved by latching the row address into the chip and maintaining the $\overline{\text{RAS}}$ signal active (low) throughout all successive memory cycles in which the row address is unchanged.

The page boundary of a single device is limited to the 128 column locations determined by all combinations of the seven column address bits. However, in system applications which utilize more than 16k data words, the page boundary can be extended by using $\overline{\text{CAS}}$ rather than $\overline{\text{RAS}}$ as the chip select signal. $\overline{\text{RAS}}$ is applied to all devices to latch the row address into each device, and then $\overline{\text{CAS}}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals will execute a read or write cycle.

Circle 354 on Inquiry Card

8-Bit Monolithic CMOS DAC Features Low Price But High Performance

A high performance multiplying D-A converter, the first device designed at this company's Limerick, Ireland operation, has been announced by Analog Devices Semiconductor, 829 Woburn St, Wilmington, MA 01887. The AD7523 monolithic device uses thin-film-on-CMOS technology to provide 8-bit resolution with accuracy to 10 bits and very low power dissipation (670 mW absolute max to 70°C, derated above 70° by 8.3 mW/°C).

Max feedthrough errors are ±½ LSB at 25°C, ±1 LSB over the 0 to 70°C range; respective max output current settling times are 150 and 200 ns. For these same temperatures, max output leakage currents are ±50 and ±200 nA; gain errors are −1.5% of FSR min, 1.5% max, and −1.8% min, 1.8% max; and max power supply re-

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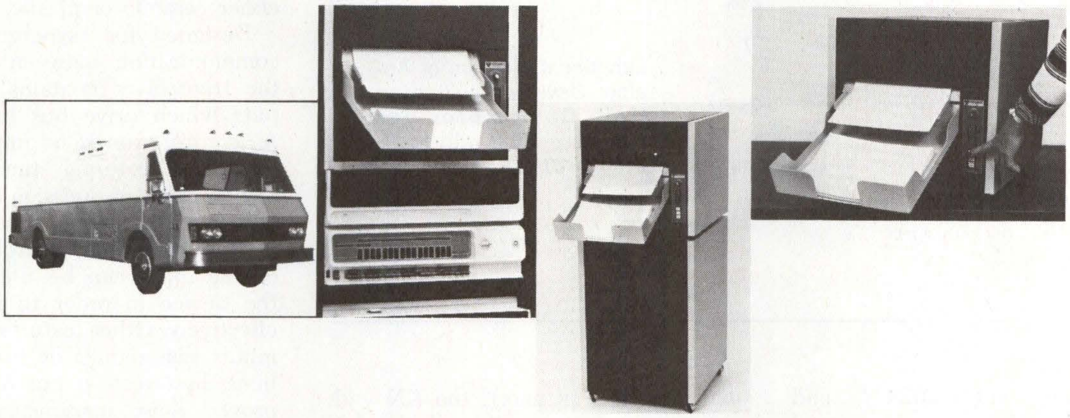

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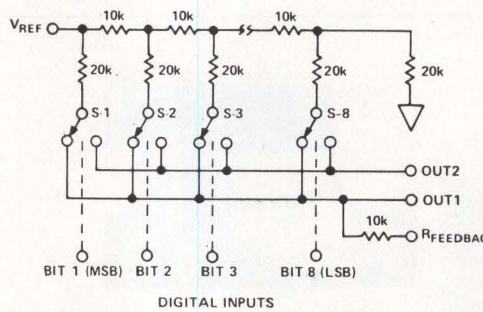

Functional diagram of Analog Devices multiplying DAC. Device provides 8-bit resolution with accuracy to 10 bits

jections (gain) of 0.02%/% and 0.03%/%. Monotonicity is guaranteed over the full 0 to 70°C range. For all temperatures, power requirements are 5 V min, 16 V max, and 100 μA max.

Three versions are offered: the AD7523JN with linearity of ±½ LSB max (±0.2% FSR max), the KN with ±¼ LSB (±0.1% FSR), and the LN with ±⅛ LSB (±0.05% FSR). Prices for these 16-pin plastic DIPs in 1000 quantities are, respectively, $2, $5, and $7.50.

Circle 355 on Inquiry Card

Monolithic Sample/Hold Is DTL, TTL, and p-MOS Compatible

Twelve-bit throughput accuracy with a 6-μs acquisition time, wideband noise of less than 20 μV rms, and droop rate as low as 5 mV/min can be achieved by the SHC298 sample/hold amplifier with the addition of a single external holding capacitor. The monolithic device has fully differential logic inputs for mode control, improving noise immunity and allowing inputs to be driven with a twisted pair. Input logic levels are DTL, TTL, and p-MOS compatible; input impedance is 10^{10} Ω; and acquisition time is less than 10 μs.

Input offset adjustments for this device, which is produced by Burr-Brown, PO Box 11400, Tucson, AZ 85734, can be made by adding an external potentiometer and a resistor. Adjustments do not degrade input offset drift.

Specifications for the device include gain errors of ±0.004% typ, ±0.010% max; gain drifts of 3 ppm/°C typ, 4 ppm/°C max; full power bandwidths of 125 kHz typ, 75 kHz min with a 1000-pF holding capacitor, 16 kHz typ, 10 kHz min with a 10,000-pF capacitor; acquisition times of 6 μs typ, 10 μs max to ±0.01% at 10-V step and 1000-pF capacitor, 8 μs typ, 12 μs max at 20-V step; and 160-mV peak amplitude sample-to-hold transient. Temperature ranges are −55 to 125°C operating, −55 to 150°C storage.

The device is available in an 8-lead, low profile TO-99 package. Typical rated power supply is ±15 V; full supply range is ±4.75 to ±18 V. Current range is ±4.5 mA typ to ±6.5 mA max.

Circle 356 on Inquiry Card

Low Power Schottky TTL Devices Have 3-State Outputs

An octal bus transceiver (the SN54LS/74LS245), an octal D-type transparent latch (the SN54LS/74LS373), and an octal edge-triggered flip-flop (the SN54LS/74LS374) are among the low power Schottky TTL devices announced by Texas Instruments Inc, PO Box 5012, Dallas, TX 75222. Versions with 54 designations are offered in 20-pin ceramic DIPs; those with 74 are available in either ceramic or plastic.

Designed for asynchronous 2-way communication between data buses, the transceiver contains 3-state outputs which drive bus lines directly. A control function implementation minimizes external timing requirements. Data transmission from one bus to another depends upon logic level at the direction control input. An enable input can be used to disable the device in order to isolate buses effectively. Other features include pnp inputs that reduce dc loading on bus lines; hysteresis at bus inputs for improved noise margins; typical port-to-port propagation delay times of 8 ns, and typical enable/disable times of 17 ns.

Both latch and flip-flop feature 3-state outputs designed specifically for driving highly capacitive or relatively low impedance loads. The high impedance third state and increased high logic level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

The eight latches are D-type in that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data setup.

For the flip-flops, on the positive transition of the clock, the Q outputs will be set to the logic states that were setup at the D inputs. Schmitt-trigger buffered inputs at the enable/clock lines simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high impedance state the outputs neither load nor drive the bus lines significantly.

Circle 357 on Inquiry Card

12-Bit Hybrid ADC Has All CMOS Circuitry

Said to be the first low power hybrid A-D converter specifically designed for portable and remote instrumentation, the ADC-HC12B consumes only 10 μA of supply current when in standby mode. Maximum power consumption is 120 mW. An internal energy storage circuit develops the negative voltage required for operation, permitting this device to operate from a single 9- or 12-V battery.

Circuitry consists of an input amplifier with protection diodes, 12 CMOS switches, CMOS successive approximation register, clock circuit, precision zener reference, and energy storage circuit. Tracking characteristics of the nichrome R-2R resistor ladder network result in 1-ppm/°C typ tracking coefficient and guaranteed monotonicity (no missing codes) over the entire operating temperature range.

The device generates its own negative supply. In interrupt power mode, the converter normally resets in a standby state (power turned off to analog section); upon receipt of a convert command signal, the converter will turn on, stabilize in 50 μs, make a complete conversion, and return to standby state.

Six input voltage ranges are provided by external pin connections: 0 to 5, 0 to 10, 0 to 20, ±2.5, ±5, and ±10 V. Nonlinearity is specified at ±½ LSB max. Output coding is straight binary, offset binary, or 2's complement. Serial data are also brought out.

The converter operates from either a single 9- to 15-Vdc power source (interrupt power mode) or a ±9- to ±15-Vdc power source (continuous power mode). Power consumption is a function of conversion rate. For 100, 1000, and 2000 conversions/s, the average power drain is approximately 3.5, 26, and 50 mW, respectively.

Four 32-pin DIPs available from Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021 cover three temperature ranges. The lowest cost version, the GC, is epoxy sealed and has a temperature range of 0 to 70°C. MC, MR, and MM versions are hermetically sealed with temperature ranges of 0 to 70, −25 to 85, and −55 to 125°C, respectively.

Circle 358 on Inquiry Card

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- This is A COMPLETE SYSTEM with BUILT-IN KEYBOARD AND DISPLAY (it is NOT a useless "start-up" system requiring expensive peripherals such as a TTY or CRT).
- This course is based on the 8080A MICROPROCESSOR (it is NOT an unpopular microprocessor of little value for future work).
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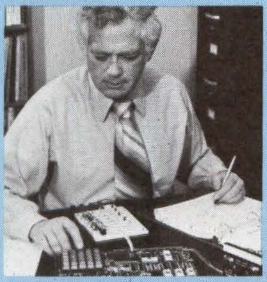

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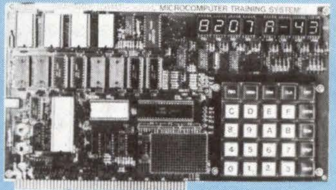

Furthermore, the computer is easily expandable (see Course 536 below).

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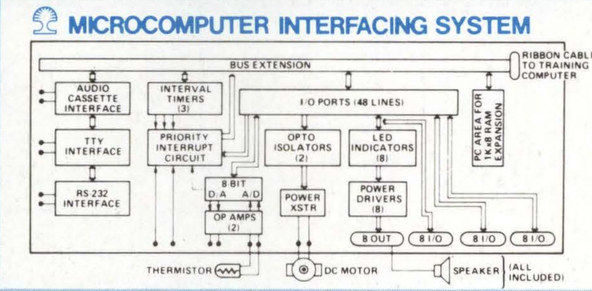

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Programmable Filtering Done in Frequency Rather Than Time Domain

One solution to the fundamental problem of programmable transversal filters in analog signal processing functions is filtering by convolution in the frequency domain rather than in the time domain. The programmable filtering is accomplished through the use of the chirp z-transform (CZT) with charge-coupled devices (CCDs).

CZT, an algorithm for computing the discrete Fourier transform (DFT), gets its name from the fact that it can be implemented by premultiplying the time signal with a chirp (linear fm) waveform, filtering in a chirp convolution filter, and postmultiplying with a chirp waveform. Convolution can be achieved with the DFT, using the CZT algorithm, multiplying by the transform of the desired impulse response, and performing the inverse DFT (shown schematically in Fig 1). When the DFT is implemented, using the CZT, Fig 2 results. However, two of the multiplication operations "cancel," resulting in Fig 3.

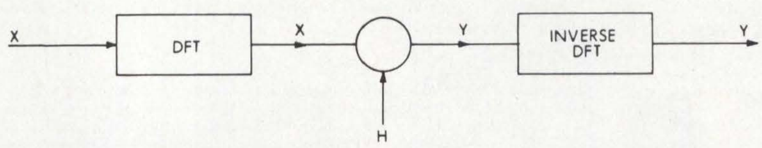


Fig 1 Convolution filtering in frequency domain can be performed using discrete Fourier transforms (DFTs). Time-domain signal is operated upon with DFT and is multiplied by transform of desired impulse response (H). Signal is reconverted to time domain by inverse DFT

The DFT can be performed using the CZT and employing either CCDs or acoustic surface-wave devices. However, the CZT lends itself naturally to implementation with CCD transversal filters.

Work on this subject was carried out by Texas Instruments Inc, Dallas, TX 75222 for Langley Research Center, Hampton, Va. Under provisions of the National Aeronautics and Space Act, title has been waived to Texas Instruments. It is expected that, with further refinements in modularity and onchip multiplication of I/O data through the use of D-A multipliers, the CCD/CZT could become a general-purpose, standard, off-the-shelf component.

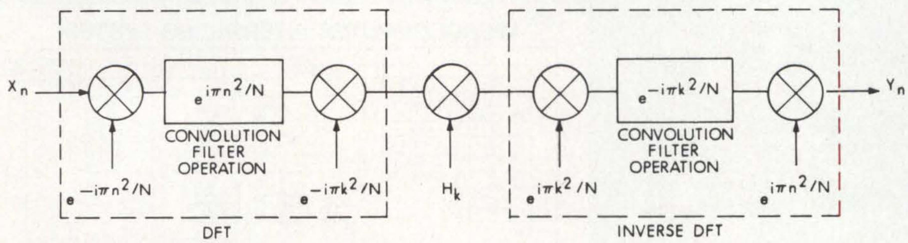


Fig 2 Chirp z-transform can be used to compute DFT in Fig 1. Time signal is multiplied by linear fm waveform, filtered in chirp convolution filter, and multiplied by another fm waveform. Inverse DFT is performed similarly

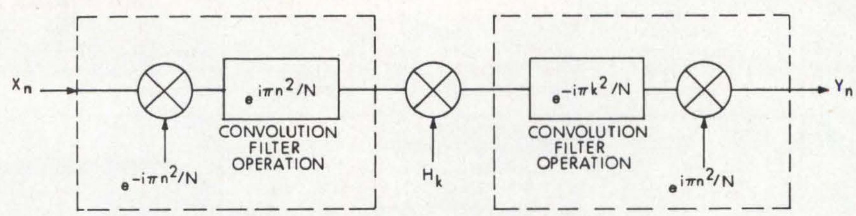


Fig 3 Reduced expression derives from expression in Fig 2. Multiplication operations commute, and complex conjugates multiply to equal 1, or "cancel out"

14-Bit Hybrid DAC Meets Both Commercial and Military Requirements

DAC-U, a high resolution 14-bit hybrid multiplying D-A converter, has a linearity of up to 0.0125% with a settling time of less than 20 μs. It maintains full resolution for both 2- and 4-quadrant operation. Features include differential input and remote ground and sense output capability, as well as low temperature coefficients and low feedthrough capacitance.

Two linearity grades are available from ILC Data Device Corp, Airport International Plaza, Bohemia, NY 11716: the -11 with ±0.025% and the -12 with ±0.0125% of full scale range. The reference frequency range is 0 to 400 Hz for full accuracy, with reduced accuracy at higher frequencies. Digital input coding is binary (2-quadrant operation) or offset binary (4-quadrant operation). Frequency for full output is 100 kHz and small signal bandwidth is 500 kHz.

All units are in hermetically sealed 24-pin DIPs processed to MIL-STD-883 Class C; Class B is a standard option. Standard temperature ranges are 0 to 70 and −55 to 125°C, for commercial as well as military and aerospace applications.

Circle 359 on Inquiry Card

Per Channel CODEC Promises Improvements Over Multichannel Types

A 2-chip set, said by the manufacturers to be the industry's first per channel coder-decoder (CODEC), has been announced jointly by Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054—the developer—and Nitron Corp, 10420 Bubb Rd, Cupertino, CA 95014—under license to second source the devices. Complete A-D and D-A converter subsystems respectively, DF331 and DF332 (NC331 and 332 for Nitron chips) conform to all Bell μ-255 specifications for communications applications.

Digital output and input is in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 1.544M-bit/s rate with analog signal sampling occurring at an 8-kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multichannel information being multiplexed over a single transmission line.

A single resistor is required on the coder output as a pull-up to its drain configuration while a single uncritical capacitor of 20 pF or greater is required on the decoder output. No other external components are needed.

Fabrication in two 14-pin DIPs provides better isolation between A-D and D-A than with a single device. It also allows application of either chip alone.

CMOS construction results in low power consumption, typically 135 mW total for both devices, which is considerably less than that of usual multichannel CODEC types. In addition, the logarithm used eliminates the need to trim internal components, further reducing cost.

12-Bit Hybrid ADC Consumes 570 mW

ADC581 series 12-bit hybrid A-D converters are direct plug-in replacements for Burr-Brown's ADC85-12ET and Datel Systems' ADC-HZ12BMM, but are said to consume approximately 70% less power. Total power consumption is typically 570 mW. Conversion time is 30 μs to a ±½ LSB of 12 bits. Each model can be short-cycled where less resolution is required. The design provides an internal clock rate control and the option to use an external clock for synchronization.

All models, from Hybrid Systems Corp, Crosby Dr, Bedford, MA 01730, are specified for the −25 to 85°C temperature range. A "B" version is screened to MIL-STD-883A, Class B.

The series features a low gain tempco of ±15 ppm/°C (max) and operates off a wide range of power supplies (±11 to ±18 V). Five input ranges can be selected and three output codes are available.

Each model is packaged in a 32-pin hermetically sealed, DIL metal case. The metal package shields the converter from noisy environments, and its hermetic construction makes it immune to environmental factors.

Circle 360 on Inquiry Card

FET Input Op Amp Has ±600-V/μs Slew Rate

Model 9932, a differential input, single ended output hybrid operational amplifier features FET input devices for low input bias currents and has been optimized for high gain bandwidth product and high slewing rate capability. It may be used as a differential amplifier, voltage follower, or inverting amplifier, all with the same high frequency characteristics.

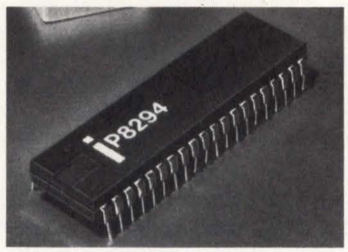
Key specifications of this device, announced by Optical Electronics, Inc, PO Box 11140, Tucson, AZ 85734, include ±600-V/μs min slewing rate at unity gain; 150-MHz typ, 40-MHz min unity gain frequency; ±10-V min swing into a 1-kΩ load at ±10-mA min, ±50-mA typ output load current; ±100-pA typ, ±300-pA max input bias currents; and 100-ns max settling time to 0.1% error for a 10-V step. Power requirements are ±6 V min, ±15 V nom rated, and ±18 V max with ±30-mA max quiescent supply current. Quiescent power dissipation is 900 mW max.

The 16-pin DIP is electrically similar to the National Semiconductor LH0032. It has input differential and common mode resistances of 100 GΩ min, differential and common mode capacitances of 3 pF max, noise voltage of 20 nV/Hz^{-2} max, noise current of 200 fA/Hz^{-2} max, and max differential voltage of ±15 V. Input offset voltage is adjustable to zero, voltage drift is ±500 μV/°C max, current is ±100 pA max, and power supply rejection is ±1 mV/V max. □

Circle 361 on Inquiry Card

PRODUCT FEATURE

Data Encryption Device Contains NBS Approved Algorithm



Encryption and decryption of data are carried out by the Intel Corp 8294 DEU using the NBS approved algorithm. This device, a peripheral to MCS-85, -80, and -48 microprocessors, operates on 64-bit text words using a 56-bit user-specified key to produce 64-bit cipher words. For decryption, the cipher word is operated on to produce the original text word. Although the algorithm is maintained permanently in the device, the key can be changed at any time by the user.

Initial steps to develop a standard for computer data encryption were begun by the U.S. Commerce Dept's National Bureau of Standards (NBS) in 1972, but the Privacy Act of 1974 increased pressure to complete the development. A proposed algorithm developed by IBM was approved by NBS in 1975 as the Data Encryption Standard (DES). (The General Services Administration predicts that DES will be incorporated in several thousand secured data terminals and computers by 1980.)

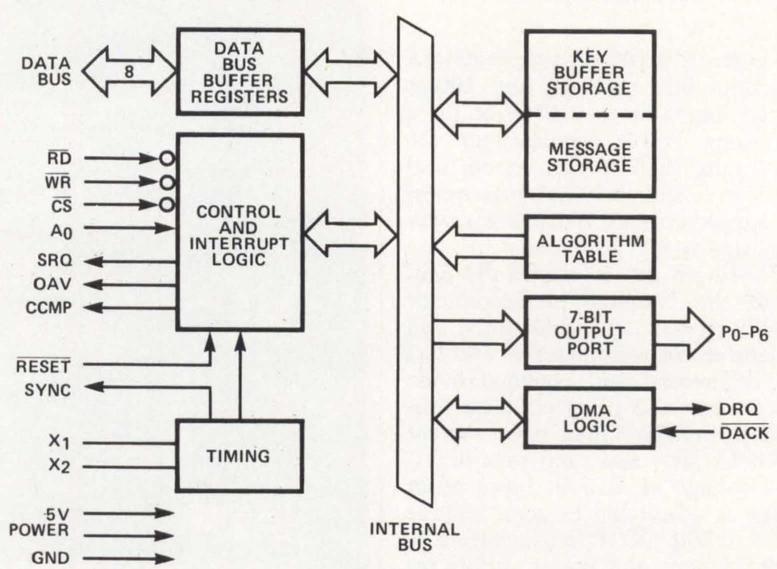
Functional Description

Both key and message data are transferred to and from the data encryption unit (DEU) in 8-bit bytes via an internal data bus (block diagram). A direct memory access (DMA) interface and three interrupt outputs which aid in loading and unloading data are available to minimize software overhead associated with data transfer. By using the DMA interface, two or more DEUs may be operated in parallel to achieve effective system conversion rates which are virtually any multiple of 80 bytes/s. The DEU also has a 7-bit TTL compatible output port for user-specified functions.

For a conversion sequence in non-DMA mode, a mode command is issued first to enable the desired interrupt outputs. Then a new key command is issued followed by eight data inputs to initialize the key. Each byte must have odd parity. Finally the encrypt data or decrypt data command is issued to set the DEU in the desired mode.

Data conversions are made by writing eight data bytes and then reading back eight converted data bytes. Any of the commands may be issued between data conversions to change the basic operation of the DEU; eg, a decrypt data command could be issued to change the DEU from encrypt mode to decrypt mode without changing either the key or the interrupt outputs enabled.

Four internal registers are addressable by the master, two each for input and output. Data written to a data input buffer register are interpreted as part of a key, as data to be encrypted/decrypted, or as a DMA block count, depending on the command sequence preceding the write; data read from a data output buffer register will be the output of the encrypter/decrypter function. DEU status is available in a status output buffer register at all times; and commands to the DEU are written to a command input buffer register.

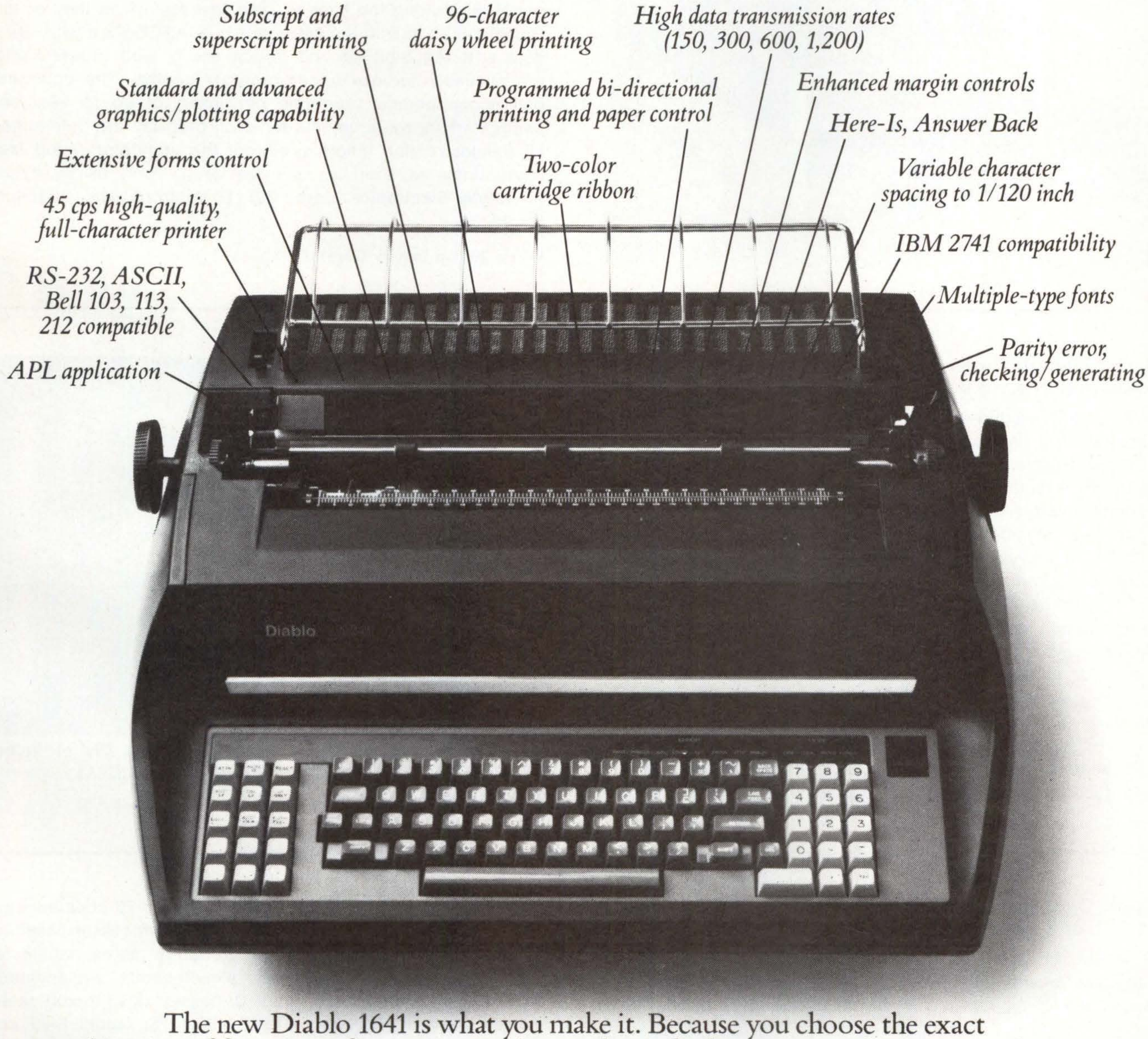


Price and Delivery

Single 8294 data encryption units sell for $45 in plastic packages; in 1000 quantities, the devices are $15 each. Samples will be available this month; regular deliveries after that time will be 90 days ARO. Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. Tel: (408) 246-7501.

For additional information circle 199 on inquiry card.

You can't judge this Diablo terminal by its cover.



The new Diablo 1641 is what you make it. Because you choose the exact combination of features to fit your particular needs. To find out more, call Joan Gruenbaum at (408) 733-2300, or write her at 545 Oakmead Parkway, Sunnyvale, CA 94082. When you get a Diablo terminal you also get Xerox quality, reliability, and availability. So you see, there's a lot more to the 1641 than meets the eye.

Diablo Systems

XEROX

Instrumentation Controller Provides Automatic Test Capability to Small Applications

The model A-1000 Autoprogrammer, although specifically designed for use with the company's SPG-800 programmable generator, can also interface as an instrumentation controller with other equipment capable of accepting commands in ASCII format. It is available with 2k bytes of EPROM or fusible-link p/ROMs, or with sockets only. Programming permits time delays to be inserted into test procedures in multiples of 25 or 250 ms for specific delay requirements; time delays from 1 to 10 s are controllable from the front panel, permitting the user to view test results as they occur. Communication with the generator is in ASCII via a byte-serial data port. An 8-bit latched output and a 1-bit trigger signal are available for use under program control. The controller can accommodate programs consisting of up to 99 steps each. Memory requirements for each program are determined by the instruction length required; the generator recognizes instructions as short as 3 bytes or as long as 65 bytes. **Interstate Electronics Corp,** 707 E Vermont Ave, Anaheim, CA 92803.

Circle 200 on Inquiry Card

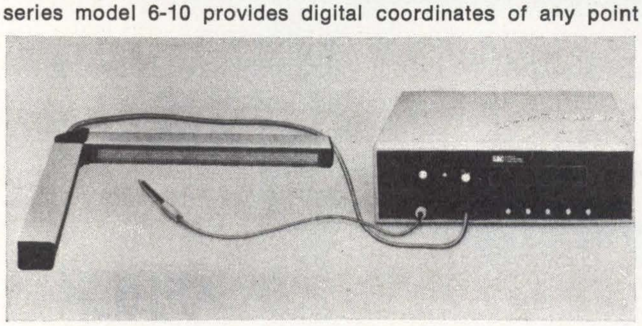
Programmable Timer Automates Procedures Requiring Precise Spacings of Events

"UP-Timer," a solid-state programmable sequencer, provides simultaneous control for up to 10 parallel, time-based operations. Programming and program editing are accomplished with only a soft pencil and IBM card. Card "timing" tracks, 1/control channel, enable 10 independent operations to be controlled simultaneously. Each track represents a complete timing cycle for its respective control output. To program a desired sequence or a single event, segments of a timing cycle that require an "on" output are darkened with a soft pencil (areas left unmarked represent the "off" condition). Cycle durations are selectable from 10 ms to 100 hours (or longer upon special request) through thumbwheel switches. Choices of output circuits include reed relay contacts or high speed solid-state relays. Any combination of output circuits may be specified. Once a card is programmed and checked for program accuracy, it is placed in a tray and inserted into the unit's reader. This causes the unit to memorize the program. **Xanadu Controls Div of Valcor Engineering,** 45 Fadem Rd, Springfield, NJ 07081.

Circle 201 on Inquiry Card

Sonic Digitizers Convert Positional Information In 1, 2, or 3 Dimensions

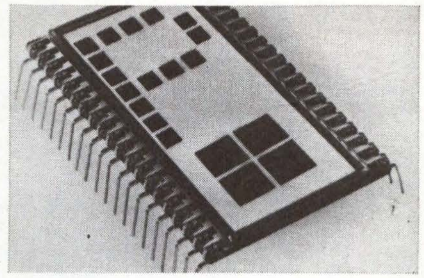
A family of 5 Graf/Pen sonic digitizers, 3 of which are microprocessor-based, eliminates the need for data tablets. GP-series model 6-10 provides digital coordinates of any point on a plane in parallel 14-bit binary output; 6-20 adds environmental temperature compensation. Microprocessor-based 6-30 establishes an origin anywhere on a plane, eliminates redundant data, and provides simultaneous alphanumeric data entry; output is in BCD Cartesian (X,Y) coordinates, compatible with RS-232 or IEEE 488-1975. Model 6-40 calculates the area beneath or within a figure on a plane, calculates the length of traced lines, digitizes 2 points, and makes derived scale selection by menu instruction; 6-50 adds axis rotation and slope calculation, and enables the user to work in polar as well as 3-dimensional Cartesian (X,Y,Z) coordinates. All microprocessor models automatically perform mathematical computations that previously required external processors or hand calculation. **Science Accessories Corp,** 970 Kings Highway W, Southport, CT 06490.



Circle 202 on Inquiry Card

PRODUCTS

5 x 7 DOT MATRIX LIQUID CRYSTAL DISPLAY

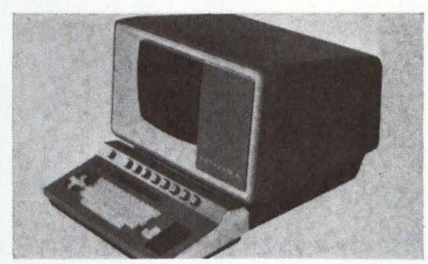


As a readout for alphanumeric applications, LCD includes a 5 x 7 dot matrix plus 4 annunciators and is used as part of point-of-sale or online terminals. Matrix viewing area is 0.9 x 0.6" (2.3 x 1.5 cm). DIP is directly solderable into PC boards. Characteristics are 3.0 V operation and reflective background. **Perkins, Inc,** 127 E Alton Ave, Santa Ana, CA 92707.
Circle 203 on Inquiry Card

MULTILINE CRT TERMINAL BUFFER

Single model 8 buffer permits CRTs and other RS-232-C compatible terminals to be located up to 4000 ft (1.2 km) from the computer without the use of modems. The Intensifier™ includes 8 fully buffered lines, permitting buffering of up to 4 terminals. Model 18 includes 18 fully buffered lines conforming to all signals described in the EIA specs. **BPI Electronics, Inc,** 4470 SW 74 Ave, Miami, FL 33155.
Circle 204 on Inquiry Card

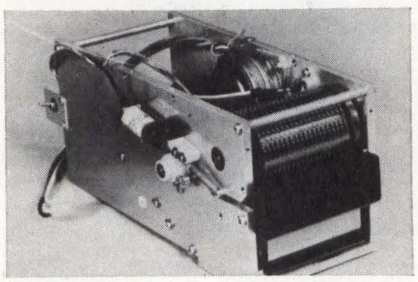
DUAL LANGUAGE TERMINAL



Terminal operates in English plus any other language, displaying two char sets on the same screen. Operator can enter data from right to left or vice versa. Char representation is accomplished on a 10 x 15 matrix. Terminal includes insert, delete, and text editing features; a memory of up to 73k; a 126-station keyboard; and a 15" (38-cm) diag display. Transmission rates are 50 baud to 38.4k baud serial, 10,000 char/s parallel. **Megadata Corp,** 35 Orville Dr, Bohemia, NY 11716.
Circle 205 on Inquiry Card

PRODUCTS

IMPACT PRINTER MECHANISMS



Two drum-type form printer mechanisms—FPM-600 numeric and -700 alphanumeric—print up to 19 col on std medical forms [3.25" (8.3 cm) wide] or on forms of varying widths. A variety of std center-to-center line spacings and special configurations can be provided; ribbon-type models are also available. Printing rates are 2.4 lines/s for 19 col of 16 char (10 numeric), and 4 lines/s for 19 col of 42 alphanumeric and symbol char for the -600 and -700, respectively. Mechanism design has been life tested to >5M lines of print. **Anadex, Inc,** 9825 DeSoto Ave, Chatsworth, CA 91311.
Circle 206 on Inquiry Card

NOVA 3 SERIES ADD-ON MEMORY

Pincomm N3, a plug-in mainframe memory system, has storage capacity of 16,384 words by 16 bits. System gives NOVA 3/12 max capacity of 256k bytes. Memory access and full cycle times are 350 ns and 1.0 μs max. With 3 operating modes—read/restore, clear write, and read/modify/write—memory meets or exceeds operating parameters required when inserted in any memory allocated connector position in all CPU models. **Standard Memories/Trendata,** 3400 W Segerstrom Ave, Santa Ana, CA 92704.
Circle 207 on Inquiry Card

7.5-mA VOLTAGE REFERENCE DIODES

PRD 7530, a precision reference diode equivalent to Motorola's MZ 605, has a nom op current of 7.5 mA and time stability of 30 μV or 5 ppm/1000 h. Series is also offered with guaranteed stability up to 5 ppm/year. Features include noise of 1 ppm of output, and 1-ppm tempco at 0 tempco op current over a temp range of 25 to 45°C. Each unit can be supplied with test data to assist in solving specific dc voltage reference problems. **CODI Corp,** Pollitt Dr S, Fair Lawn, NJ 07410.
Circle 208 on Inquiry Card

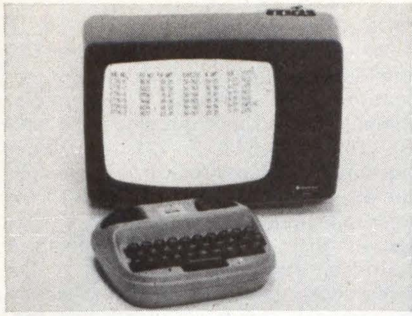
OPTICALLY COUPLED ISOLATORS

Providing high voltage isolation, devices feature input-to-output steady state isolation voltage of >6000 V in free air and >10,000 V when encapsulated. They consist of a high efficiency solution grown GaAs IR LED coupled with either a silicon phototransistor or photodarlington in a molded plastic package. Std pin spacing of 0.300 x 0.100" (0.762 x 0.254 cm) is compatible with that of DIL sockets. **Optron, Inc,** 1201 Tappan Cir, Carrollton, TX 75006.
Circle 209 on Inquiry Card

UTILITY SYSTEM

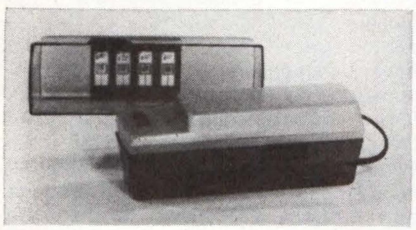
Written in Business BASIC for operation on Data General NOVA and ECLIPSE, the spooler utility provides a means of efficiently controlling output of print files to various printing devices available. Services provided include elimination of conflict caused by more than one program needing the printer at the same time, printing on other than the system printer, support of multiple printers connected to the terminal multiplexer, and printing any number of copies under program control or through a control program. **Technical Analysis Corp,** 120 W Wieuca Rd, NE, Atlanta, GA 30342.
Circle 210 on Inquiry Card

TV-DISPLAY TERMINAL



TIGER (Television Interface General-purpose Economy Remote terminal) contains acoustic coupler for communications with remote timeshare computers, full ASCII keyboard, and TV electronics that interconnect to std TV set via antenna input. Up to 1024 char may be simultaneously displayed in switch-selectable formats for 8 or 16 lines of 32 or 64 char/line. The unit has a built-in power supply, measures 8 x 10 x 3" (20 x 25 x 7.6 cm), and weighs 4 lb (1.8 kg). **Micon Industries,** 252 Oak St, Oakland, CA 94607.
Circle 211 on Inquiry Card

p/ROM ERASING LAMP



Short wave lamp features simple operation and safety features for small system user and computer hobbyist. Lamp erases up to 4 chips at a time in 14 min. Safety interlock system protects user against accidental UV exposure. Lightweight and compact system comes with holding tray for maintaining constant exposure distance of 1" (2.54 cm), and is available in 115- or 220-V models. **Ultra-Violet Products, Inc,** 5100 Walnut Grove Ave, San Gabriel, CA 91778.
Circle 212 on Inquiry Card

DIGITAL PROCESS MONITOR

Capable of being programmed to accept inputs from linear or nonlinear transducers, 700 series meter handles multiple-valued transfer functions. All linearization is done by digital processing. The 3½-digit instrument accepts current inputs of 0 to 1, 4 to 20, and 10 to 50 mA; and voltage inputs of 0 to 1, 1 to 5, and 0 to 10 V. Sampling rate is factory set at 3 to 5/s; this is field adjustable from 40/s to 1/10 s. Accuracy is 0.1% FS ±1 LSD. **Dynamic Sciences, Inc,** 16150 Stagg St, Van Nuys, CA 91406.
Circle 213 on Inquiry Card

TAPE CONTROLLER

5191-I, an embedded magnetic tape controller for Interdata computers, provides an interface between computer and industry std magnetic tape drive. The single 15" (38-cm) PC board plugs into one full-card slot of the computer, and is transparent to existing operational and diagnostic software. As many as four tape drives can be connected, each with individual speed and density configurations. Interface is to multiplexer bus or selector channel. **Datum Inc,** 1363 S State College Blvd, Anaheim, CA 92806.
Circle 214 on Inquiry Card

EPOXY DIPPED TANTALUM CAPACITORS

The ST841, 842 series of economy miniature capacitors have capacity ranges form 0.1 to 680 μF in 8 voltage categories from 3 to 50 V. Tolerances of 5, 10, or 20% are available. Both series have radial leads and are available with straight or lock-in crimp leads for easy PC board insertion. Epoxy dipped solid tantalum devices are intended for applications with high volume production requirements. **Siemens Corp, Components Group,** 186 Wood Ave S, Iselin, NJ 08830.
Circle 215 on Inquiry Card

DATA CARTRIDGE RECORDER

Designed with a built-in baud rate converter, the model 300C recorder connects between a modem/CPU and a terminal with an on/offline storage capacity of 1.5M char. It is equipped with dual RS-232 ports, dual UARTs, and a 512-char buffer to accomplish baud rate conversion. Speeds are selectable from 110 through 19.2k baud with current loop capability in the terminal port. In online mode, char received on one port is immediately retransmitted on the other port at the preselected baud rate. **Columbia Data Products, Inc,** 6655 Amberton Dr, Baltimore, MD 21227.

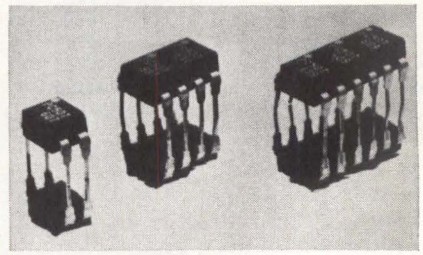
Circle 216 on Inquiry Card

VOICE DATA ENTRY TERMINAL

As a direct replacement for either a video or teleprinter terminal, the 600 terminal requires no modification of host-computer software. The microcomputer-based unit is compatible with EIA RS-232-C, CCITT-V24, or 20-mA current loop teleprinters. It features full-duplex communications via ASCII or other commonly used codes, and is configured with a mag tape miniature cartridge storage device. All voice recognition functions are controlled by the terminal. **Threshold Technology, Inc,** 1829 Underwood Blvd, Delran, NJ 08075.

Circle 217 on Inquiry Card

SINGLE, DUAL, AND TRIPLE DIP PHOTOCOUPLERS

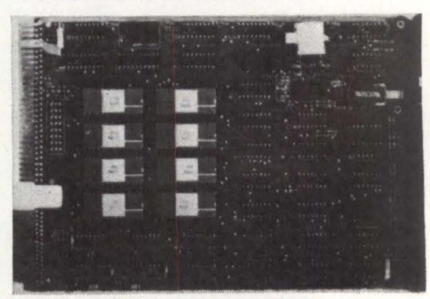


Provided in plastic DIPs for high density requirements, PC-507 series photocouplers are TTL compatible and have a response time of 2 μs. Typ applications include computer I/O interfaces, noise reduction for systems and measuring instruments, and signal transmission in circuits with different impedances. Collector-emitter voltage runs 0.4 V max; current transfer ratio is 50%; and reverse isolation voltage is 1500 V. Typ dark current is 1×10^{-9} at V_{CE}=20 V. **Quantrad Corp,** 19900 S Normandie Ave, Torrance, CA 90502.

Circle 218 on Inquiry Card

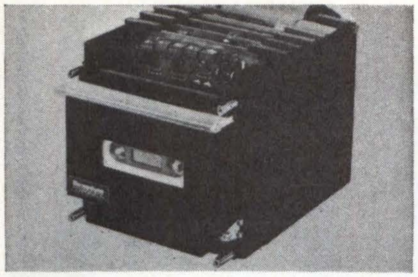
MULTILINE COMMUNICATIONS INTERFACE

Up to 6 multiline modules can be installed on a single 40 series microcomputer system. Each module contains eight EIA RS-232 communications interfaces, each with speed and code level individually selectable under program control. Rear-mounted 25-pin connector panel is included with the module. **Micom Systems, Inc,** 9551 Irondale Ave, Chatsworth, CA 91311.



Circle 219 on Inquiry Card

ANSI COMPATIBLE CASSETTE RECORDER



Model 765-8 contains all necessary electronic circuits for accepting parallel data and formatting them into correct number of char as well as adding preamble and postamble. Unit features circuits for controlling required operating functions of high speed transport along with R/W, drive, and servo cards. TTL compatible, recorder stores up to 2.2M bits, has a record/playback speed of 20 in/s (51 cm/s), and rewind and search at 100 in/s (254 cm/s). Unit measures 5 x 4.75 x 7" (13 x 12.07 x 18 cm) and weighs 4 lbs (1.8 kg). **Memodyne Corp,** 385 Elliot St, Newton Upper Falls, MA 02164.
Circle 220 on Inquiry Card

GENERAL-PURPOSE BREADBOARDS

Designed to hold 147 16-pin wirewrap sockets, the 126E breadboard measures 7.9 x 12.20" (20 x 30.99 cm). The 100-pin board with a 0.125" (3.175-mm) gold-plated connector and patterns on both sides is intended for industrial applications. Power and ground are std. Several S-100 compatible microprocessor boards for home and industrial use are also offered; the single-card 32k-100, an 8k to 32k expandable memory board, is designed to be DMA compatible. **Artec Electronics, Inc,** 605 Old County Rd, San Carlos, CA 94070.
Circle 223 on Inquiry Card

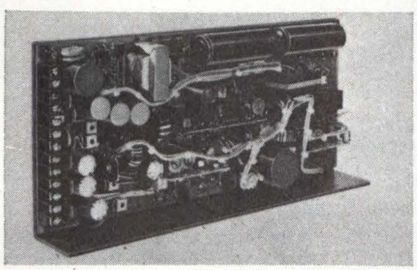
PROGRAMMABLE KEYBOARD

The ASR 33 solid-state keyboard achieves max flexibility due to p/ROM encoding. It is available fully encoded or without p/ROM for customer programming. Std features are the company's "Super Switch" ferrite core keystations, N-key rollover, working life >100M operations/keystation, and low profile. Keyboards are available in 53- or 57-key array. Encoding is USASCII, 7-bit with parity. Input power is 5 Vdc ±5% at 500 mA max, and −12 Vdc ±10% at 50 mA max. **Cortron, div of Illinois Tool Works, Inc,** 6601 W Irving Pk Rd, Chicago, IL 60634.
Circle 224 on Inquiry Card

T-¾ LED LAMPS

High intensity LLL-series miniature GaP LED lamps for portable and high density applications are available in 4 colors. All types are encapsulated in rugged epoxy lenses. Lens dia is 0.090" (2.3 mm), overall lens length is 0.150" (3.8 mm), and base flange dia is 0.120" (3.05 mm). Typ luminous intensities range to 4 mcd at forward current of 12 mA with viewing angles of up to 30 deg. **OPCOA, div of IDS, Inc,** 330 Talmadge Rd, Edison, NJ 08817.
Circle 221 on Inquiry Card

4-OUTPUT SWITCHER



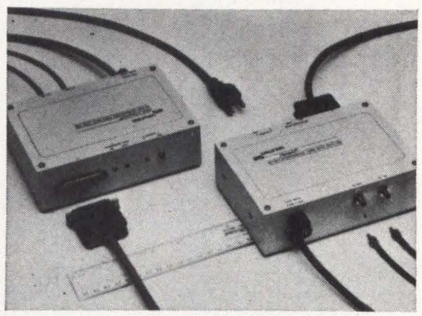
Tiny-MITE model TM-34 offers 175 W of power in a package measuring 13.0 x 6.0 x 2.75" (33.0 x 15.2 x 6.99 cm) and weighing less than 4.5 lb (2.0 kg), and achieves 70% nom efficiency. Four output voltages from 5 through 28 V are adjustable ±5% at 175 W. Main output is 5 V at 20 A; second and third outputs are 5 V at 5 A, 12 V at 5 A, 15 V at 4 A, 18 V at 3 A, 24 V at 2 A, or 28 V at 2 A. Fourth output can be 5, 12, or 15 V at 1.5 A. **LH Research, Inc,** 1821 Langley Ave, Irvine, CA 92714.
Circle 222 on Inquiry Card

PRODUCTS

CCD SERIAL MEMORY SYSTEM

PSM5463, a 64k x 8-bit single card memory system, offers improved packing density and power consumption. Compatible with both 8- and 16-bit high speed microprocessors, store operates in read, write, or read/modify/write modes and has a multiplexed I/O structure enabling it to operate up to 64M bits/s. A special refresh interrupt priority can further minimize std access time. System is offered on a double Eurocard or in a 19" (48-cm) chassis-mounted system incorporating all electronics for controlling and storing 16M bits of data. **Plessey Microsystems,** Water Lane, Towcester, Northants NN12 7JN, England.
Circle 225 on Inquiry Card

RS-232-C FIBER-OPTIC DUPLEX DATA LINK

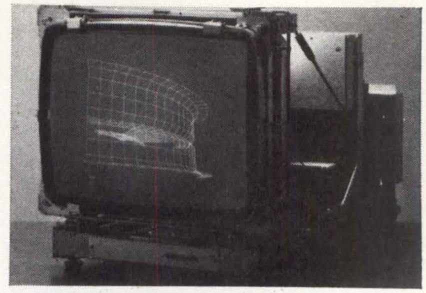


Data link accepts 25-pin RS-232-C electrical plug as input and converts directly to optical digital data transmission. Output is directly connected to preterminated fiber-optic duplex cable. Each end of link contains a receiver, transmitter, power supply, and power cord with wall plug. Transmission capability from dc to 20k bits/s over distances up to 3000 ft (1 km) is built-in. RS-232-C link provides users with option of modem elimination, low cost cable installation, secure lines, safety in hazardous environments, and immunity to emi. **Valtec Corp,** West Boylston, MA 01583.
Circle 226 on Inquiry Card

480-CHAR DISPLAY

Organized into 12 lines of 40 char each, model 0771 is plug compatible with IBM units. Display enhancements include local display-to-print, 10-key numeric pad, lightpen, OCR wand, operator prompting line, cursor position display, cluster diagnostics, and response time indicator. Response time threshold is variable from 0 to 30 s. **Trivex, Inc,** 3180 Red Hill Ave, Costa Mesa, CA 92626.
Circle 227 on Inquiry Card

STORAGE-REFRESH GRAPHIC DISPLAY



High speed 19" (48-cm) GMA102A displays up to 1575" (40 m) of refreshed vector in combined store-refresh mode. Features of directed-beam refresh display are combined with those of direct view storage tube display, resulting in high resolution graphics, dynamic movement, and selective erase. Permanent parts of graphics and alphanumeric image are stored on display phosphor; simultaneously interactive picture elements are displayed in refresh. CRT and PC board modules are arranged on wireform chassis. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.
Circle 228 on Inquiry Card

MICRO-MINIATURE CAPACITORS

Metallized polycarbonate capacitors with voltage rating of 50 Vdc have capacitance values ranging from 0.001 to 0.10 μF. Typ X440 units, measuring 0.095 x 0.245 x 0.290" (2.4 x 6.2 x 7.3 mm), are packaged in an epoxy case with standoffs; they comply with Mil Spec C-27287. Capable of replacing mica or ceramic devices, the units are suitable for tight-fitting aerospace applications. Specs include tolerances to $\pm$1%, and a dissipation factor of $<$0.3% at 1 kHz at 25°C. **TRW Capacitors, an Electronic Components Div of TRW, Inc,** 301 W "O" St, Ogallala, NE 69153.
Circle 229 on Inquiry Card

MODEM ADAPTER

Model VA861 allows 4800- and 9600-baud modems to be used in multiline automatic calling systems (MACS). Using VA1616 multichassis, 1-card slot accepts dialer and 2-card slots accept adapter. A bus system in chassis connects controlling dialer with each modem in system. All signaling takes place through characters sent from computer on transmit data and received by computer on received data. Adapter responds to bus system like a compatible modem. It may be used in any of VA1616 card slots and intermixed with any combination of MACS compatible modems. **Vadic Corp,** 222 Caspian Dr, Sunnyvale, CA 94086.
Circle 230 on Inquiry Card

S/R-D CONVERTERS

Low profile, miniature converters incorporate zero-lag tracking performance, ruggedness, and reliability. Available in 10-, 12-, and 14-bit configurations with industry std pinouts, units operate as single modules over the 50- to 1200-Hz frequency range. Features include 1000% overvoltage damage immunity, high input impedance at all input levels, complete frequency independence, insensitivity to harmonic distortions, and common mode rejection of 80 dB. **Control Sciences Inc,** 8399 Topanga Canyon Blvd, Suite 303, Canoga Park, CA 91304.
Circle 231 on Inquiry Card

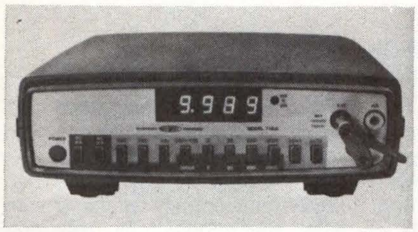
GREEN LED LAMPS

With guaranteed brightness in both T-1 and T-1¾ sizes, GaP lamps can be powered directly by std TTL and MOS IC circuitry, and are available with snap-in mounting clips to simplify panel mounting. GL-4950, a T-1¾ size, is equivalent to HP5082-4950. It has a large full-flood radiating surface and is visible over a wide viewing angle. At 20-mA current, it provides 1 mcd min and 1.8 mcd typ. GL-211, a T-1 unit, is equivalent to TIL-211. It produces 0.8 mcd min and 1.5 mcd typ at 20 mA. **Litronix, Inc,** 19000 Homestead Rd, Cupertino, CA 95014.
Circle 234 on Inquiry Card

TIME DIVISION MULTIPLEXER

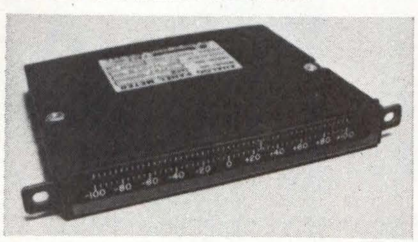
TDM 1256 multiplexes six 230.4k-bit/s data streams, six 256k-bit/s data streams, or a mixture of these up to a max of 6 derived channels into 1.544M bits/s. Its primary application is to derive digital channels from a T1 class transmission facility at 1.544M bits/s. The bit interleaving technique used provides a high level of multiplexing efficiency and a low transmission delay. It interfaces with an AT&T channel service unit. Channel interfaces are compatible with the company's other TDMs. **General DataComm Industries, Inc,** 131 Danbury Rd, Wilton, CT 06897.
Circle 235 on Inquiry Card

4½-DIGIT MULTIMETERS



Models for bench and portable field use are available with dc accuracies of 0.02 or 0.05%, current or dBm measuring modes, and auto and manual range selection. Dc voltage from ±10 mV to ±1000 V is measured in 5 ranges, as are ac voltage measurements made from 10 mV to 750 V. Resistance mode offers 6 ranges from 0.01 Ω to 20 MΩ. Portable multimeter measures dBm from −60 to 60 dBm in 5 manual ranges. Circuit and components minimize and eliminate drift. **Systron-Donner Corp, Instrument Div,** 10 Systron Dr, Concord, CA 94518.
Circle 232 on Inquiry Card

SOLID-STATE ANALOG PANEL METERS



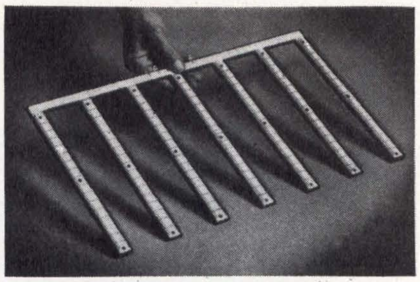
Vertical or horizontal meters feature a 3" (8 cm) scale with 1% accuracy; a thermoplastic case 4.125 x 0.57 x 3.75" (10.478 x 1.45 x 9.53 cm); excellent visibility except in direct sunlight; and 100-kΩ input impedance. Panel meter lights one LED in a row of 100, contains 0 and FS adjust electronics, and over- and under-range indicators. Drawing 0.75 W, meter has 14 std dc voltage and ampere ranges. Options include ac input signal, center 0, front panel mounting, and various front ends. **Bowmar/ALI, Inc,** 531 Main St, Acton, MA 01720.
Circle 233 on Inquiry Card

PRODUCTS

MINIATURE IRONLESS ROTOR DC MOTOR

12 Vdc, 3 W motor offers low cogging, rapid acceleration, and low noise levels. Use of an ironless rotor and oblique winding design results in a low rotor moment of inertia (9 gm²), high starting torque (310 gcm), and low mechanical time constant (11.5 ms). Motor achieves efficiencies of >70%. Typ uses include reel and capstan drives in audio or digital cassette tape recorders, printer ribbon drives, and chart and pen drives in XY plotters. **North American Philips Controls Corp,** Cheshire Industrial Pk, Cheshire, CT 06410.
Circle 236 on Inquiry Card

MULTILAYER BUS BARS



Building multilayer bus bars using staked and soldered pins permits reliable automatic wirewraps when employed in communication, industrial control, and electrical/electronic equipment. Square pins of 0.025" (0.635 mm) dia are press fitted into round holes and electrically soldered to insure positive connection. Bus bars have passed all mechanical and environmental tests required for shipboard applications. Conductor layers are electrical grade copper. **Methode Electronics, Inc,** 1700 Hicks Rd, Rolling Meadows, IL 60008.
Circle 237 on Inquiry Card

MAG TAPE DATA TRANSFER LINK

A high speed mag tape system functions as a supplementary data transfer link between SyFa network processing systems and IBM 360 and 370 mainframes. Comprising all drive and controller hardware, operator's panel, and utility software, the system is available in an 800-bit/in (315/cm) version (MAG-800), or as switch-selectable 800/1600 bits/in (315/630 bits/cm) (MAG-1600). Both operate at 25 in (63.5 cm)/s and use industry-std 10.5" (25.4-cm) reels. Recording is carried out using NRZ format. **Computer Automation,** 18651 Von Karman, Irvine, CA 92713.
Circle 238 on Inquiry Card

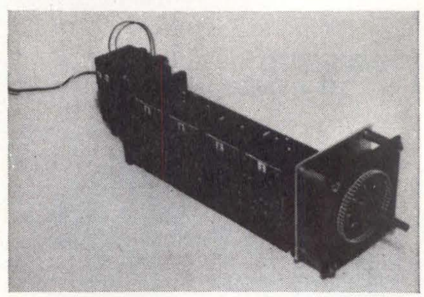
11-POSITION MOTHERBOARD

Model 8803 allows fast interconnection of microcomputer CPU, memory, and interface boards using S-100 bus configuration. It etches traces for 96 bus lines as well as heavy buses for ground, 5 V, and ±12 V. Ground and 5-V buses are rated at 10 A, while ±12-V buses are rated 7 A. Pre-established points for power supply sense lines permit remote monitoring to insure proper voltage regulation. Positions for 11 connectors with 100 contacts, 50 each side, with 0.125-in (0.318-cm) centers and 0.25-in (0.63-cm) row spacing are on board. **Vector Electronic Co,** 12460 Gladstone Ave, Sylmar, CA 91342.
Circle 239 on Inquiry Card

SORT/MERGE SOFTWARE PACKAGE

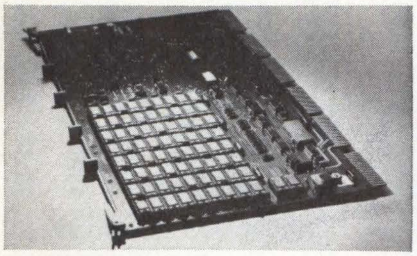
Efficiency of sorting is increased with the architecture of the company's 32-bit processors by permitting up to 1M bytes of in-core work space. SORT/MERGE II is aimed at minicomputer users with large data file applications requiring high performance. Features include unlimited number of keys in mixed sequence; multiple input files; IBM and ANSI std labeling and blocking; and computational, display, packed decimal, and floating-point key fields. Software requires 15k bytes of main memory. **Interdata, Inc, div of Perkin-Elmer Data Systems,** 2 Crescent P1, Oceanport, NJ 07757.
Circle 240 on Inquiry Card

INTERLOCKED PROGRAM SEQUENCER



Sequencer allows programming of up to 42 inductive loads in any combination over 60 sequential steps. By repositioning individual actuator pegs program may be readily modified. A simple contact closure controls sequential step advance from remote endpoint control sensors. With optional commutator switch, each step command may be interlocked to provide drum advance when predetermined conditions are satisfied. Steps occur at rates up to 3/s; programs of <60 steps are accommodated through built-in homing circuit. **Programming Devices Div of Sealectro Corp,** Mamaroneck, NY 10543.
Circle 241 on Inquiry Card

PDP-11 COMPATIBLE MEMORY CARD



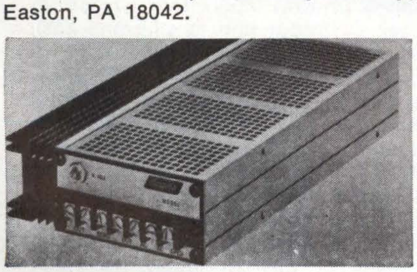
Hardware and software compatible with DEC PDP-11/04 and -11/34 computers, in-5034 add-in memory system uses high speed 8k/16k MOS RAMs to provide 32k, 48k, or 64k x 18-bit capacity on a card that measures 15.4 x 0.375 x 8.4" (39.1 x 0.95 x 21.3 cm) and fits a single hex-height card slot. Reliability features include parity checking and generation and control status register. Pretested onboard spare memory devices are provided. **Intel Memory Systems,** 1302 N Mathilda Ave, Sunnyvale, CA 94086.
Circle 242 on Inquiry Card

MINIATURE POWER SUPPLIES

Micro-Supply family consists of ac adapter plus regulated converters. Ac adapter is a wall plug-in unit measuring 2 x 2 x 1.8" (5 x 5 x 4.6 cm). Regulated converters with dual or triple outputs measure 2.2 x 3.2 x 0.5" (5.6 x 8.1 x 1.3 cm) and are encapsulated. Supplies provide 3 output voltages in an overall height of <0.5" (1.3 cm), making them suitable for PC board mounting on small systems. **Scientific Programming Inc,** 1499 Bayshore Hwy, Suite 126, Burlingame, CA 94010.
Circle 243 on Inquiry Card

NARROW PROFILE POWER SUPPLIES

Output voltage ranges from 0 to 7 and 0 to 150 Vdc, as well as output current ratings to 2.1 A, are provided by 1.68" (4.3-cm) thick power supplies for narrow space mountings. Outputs may be adjusted from 0 to max rated output voltage by front panel controls or with external programming resistance. Line and load regulation are ±0.005% or 2 mV; ripple is 0.25 mV rms. Std input is 105 to 125 Vac, 50 to 400 Hz. Overvoltage protection and 210- to 250-Vac input are available as options. **Acopian Corp,** Easton, PA 18042.



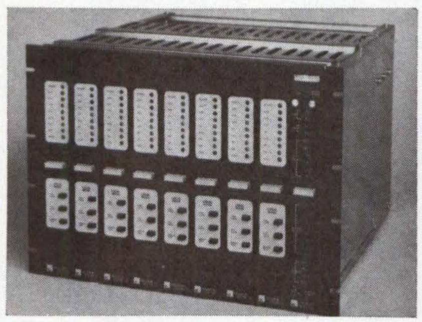
Circle 244 on Inquiry Card

LA36/TWX COMPATIBLE MODEM

Model 4911 operates with DECwriter LA36, providing users 4 choices of transmission with its output dial touchtone keyboard. It has capability for timesharing terminals through DDD or 10- or 30-char/s transmission speeds; access to TWX networks for multiple add-on terminals is through a special RS-232 interface. Automatic answer and originate answer, rotary or touchtone line capability, restraint, automatic answerback, and totally unattended operation are features. **Omnitec Data,** 2405 S 20th St, Phoenix, AZ 85034.
Circle 245 on Inquiry Card

2400-BIT/s CENTRAL-SITE MODEM

The CS 24 LSI modem operates at 2400 bits/s over unconditioned 2-wire



dial or 4-wire dedicated point-to-point or multidrop circuits. Size allows 9 modems to fit on 1 shelf of a std 19" (48-cm) rack, and 36 in a std 6' (1.8-m) equipment cabinet. Modems can be plugged in and removed from racks even while power supply is on without disrupting other modems in the rack. Each has separate rectifiers, filters, and power regulators, with 9-LED display and front panel pushbuttons for self-test modes. **Racal-Milgo, Inc,** 8600 NW 41st St, Miami, FL 33166.
Circle 246 on Inquiry Card

ELECTRONIC DATA SWITCHING SYSTEM

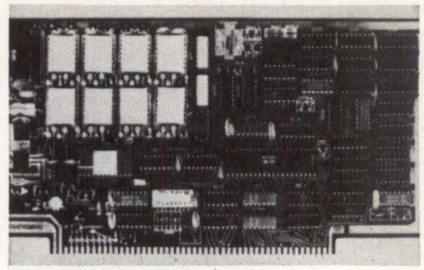
The Front End Switch automatically switches one or several terminals from a computer source that has failed to a backup computer or other preselected source. System is available in std configurations capable of handling up to 254 incoming terminals; switching is controlled by the DTR signal of the connected service and occurs automatically when DTR goes false. Unit is equipped with a system control panel that provides facilities for full manual control and monitoring for test purposes. Speeds are up to 9.6k bits/s asynchronous and 19.2k bits/s synchronous. **Gandalf Data, Inc,** 1019 S Noel St, Wheeling, IL 60090.
Circle 247 on Inquiry Card

ALPHANUMERIC PRINTERS

DigiTec printers, using an electrosensitive technique, have an internal microprocessor that simplifies system interfacing and reduces component count. Double font (bold face) printing and variable formatting are featured; crystal-controlled, 24-h clock and day/month calendar are provided on the 6320 and 6330. The 6310 and 6320 are designed for RS-232-C or 20-mA current loop inputs at data rates from 110 to 600, and 1200 baud, respectively; the 6330 has an 8-bit parallel bus input, accepting data rates up to 1k char/s with higher rates available. **United Systems Corp,** 918 Woodley Rd, Dayton, OH 45403.

Circle 248 on Inquiry Card

103A COMPATIBLE MODEM



Communications over the switched telephone network or private lines at software selected rates between 66 and 600 baud are provided by the 88-modem. Compatible with Bell System type 103A modems, it operates in half- or full-duplex mode. The S-100 bus compatible unit includes a serial I/O port and an originate/answer modem on one board. Features such as pulse code dialing in originate mode and automatic break/disconnect are implemented in hardware. The device contains an 8-pole transmit and 8-pole receive filter, self-test circuitry, and dial-tone detect filter. **International Data Systems, Inc,** 400 N Washington St, Suite 200, Falls Church, VA 22046.

Circle 249 on Inquiry Card

TERMINAL CLUSTER CONTROLLER

The cluster controller 8660 enables a group of terminals, both visual display keystations (4800 baud) and printers (up to 150 char/s), to share a common communications link to a remote system running the company's MODUS operating system. With no user programming required, the controller provides each of the terminals on the remote cluster with the same facilities that are available on locally connected terminals. A total of eight terminals may be directly connected to a single unit at distances up to 100 m. **Computer Technology Ltd,** Eaton Rd, Hemel, Hempstead, Hertfordshire HP2 7EQ, England.

Circle 250 on Inquiry Card

SYNCHRO/RESOLVER TO DC CONVERTERS

The SD-100 series of solid-state converters convert std 11.8- or 90-V 3-phase synchro (3-wire) or 2-phase resolver (4-wire) inputs into two dc voltages corresponding to sine and cosine of the rotor shaft angle. Rate is 400 conversions/s, with a peak angular error of ± 2 min. Input is transformer isolated and balanced line-to-line. Synchro input quadrature is rejected. Power required is ± 15 Vdc, $\pm 5\%$ at 12 mA each max. Output load is 2 kΩ min, and output voltage is 0 to ± 10 Vdc. **Computer Conversions Corp,** 6 Dunton Ct, East Northport, NY 11731.

Circle 251 on Inquiry Card

LOW PROFILE THICK FILM RESISTOR NETWORK

Providing up to nine resistors for high density packaging, and an aboveboard height of 0.195" (0.495 cm), network features tough, uniform molded coating and is available in 6-, 8-, and 10-pin models. Individual resistors in MSP series have a max power rating of 0.18 W with max rating of 1.70 W/10-pin package. Std resistance range is from 10 Ω to 1 mΩ with ±2% tolerance std. **Dale Electronics, Inc,** Box 74, Norfolk, NE 68701.

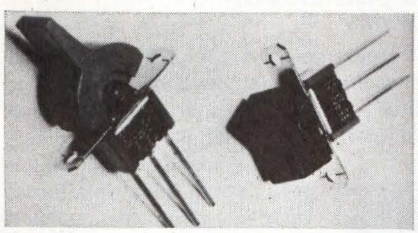
Circle 252 on Inquiry Card

FLAT CABLE ASSEMBLIES

D subminiature connectors in 9-, 15-, 25-, 37-, and 50-pin configurations are available as ready-to-install jumpers featuring soldered connections. Potting of backshell provides cable strain relief. Exiting from back or sides of connector, cable is EIA color-coded 26 AWG; however, other sizes and types of wire can be accommodated. Cable end can be furnished stripped and tinned, or terminated into a covered DIP header in any of several configurations. **Aries Electronics, Inc,** PO Box 231, Frenchtown, NJ 08825.

Circle 253 on Inquiry Card

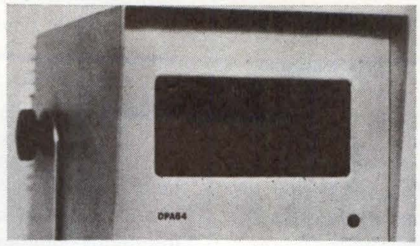
MINIATURE ROCKER AND LEVER-OPERATED SWITCHES



572 series includes 2 sizes of rockers and levers—0.365 x 0.648" (0.927 x 1.646 cm), and 0.595 x 1.036" (1.511 x 2.631 cm); and 0.365 x 0.740" (0.927 x 1.879 cm), and 0.595 x 1.174" (1.511 x 2.982 cm), respectively. Molded nylon actuators are available in 7 colors. Other options include 6 types of terminals, 9 different switching functions, and std, low level, or combination std/low level contact rating. **Dialight, a North American Philips Co,** 203 Harrison Pl, Brooklyn, NY 11237.

Circle 254 on Inquiry Card

SMALL ALPHANUMERIC PLASMA DISPLAY



Desk-mountable DPA64 is a p/ROM-operated unit that is easy to read in high amb light over a 120-deg viewing angle. Plug compatible with most minicomputers and modems by 20-mA current loop or RS-232-C interface, the UL listed unit handles up to a 9600-baud rate. Self-test diagnostics indicate if display and communication line are operating properly. Up to 15 displays operate on a single high speed line or units may be polled individually. RAM buffers up to 128 char and refreshes itself. **Pichler Associates,** 410 Great Rd, Littleton, MA 01460.

Circle 255 on Inquiry Card

FUSELESS UPS BRANCH CIRCUITS

Circuit-breaker, branch-circuit panelboards can be used without fuses on the output of this ac UPS. Implementation of an extra high, surge-rated static switch permits the system to deliver sufficient current to trip a 100-A conventional thermal mag circuit breaker in minimal operating time. Main bus voltage may drop more than desired for critical loads due to source impedance; this drop can be reduced with faster operating, branch circuit-breaker or faster fused-switch panelboards. System ratings are 2 to 250 kVA, single or 3-phase. **Cyberex, Inc,** 7171 Industrial Pk Blvd, Mentor, OH 44060.

Circle 256 on Inquiry Card

PRINTER/PLOTTER GRAPHIC DISPLAY INTERFACE

Hardware interface produces graphic hard copies on 1100A and 1200A matrix printer/plotters. Minicomputer-based systems support 3 modes of interface operation. High resolution copies (100 dots/in) of CRT display are produced in <13 s by activating a button. Interface converts random to raster scan formatted data and no time-consuming software routines are needed. Because systems employ a stroke-drawn char technique, alphanumerics and special symbols of any size can be plotted directly. **Imlac Corp,** 150 A St, Needham Heights, MA 02194.

Circle 257 on Inquiry Card

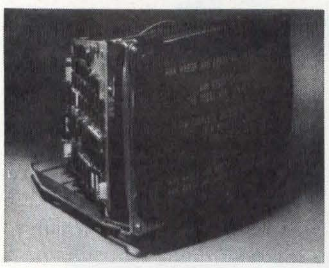
PRODUCTS

LOW POWER CARTRIDGE TRANSPORT

Requiring only a dual-voltage power supply, model 631 dissipates 22.6 W max during start; when running, consumption drops to 8.2 W. Transport electronics require only 1 W while a high accuracy Swiss shell-wound motor consumes 22.6 W during ramps and 7.2 W while running. The device eliminates warping on new media, while a multipoint cartridge suspension system realigns previously used media. Top surfaces of cartridge guides are machined true to the transport's heavy aluminum foundation plate. Spring loaded nylon rollers, bearing on the underside of cartridge base plate, force tape into proper head alignment. The bidirectional transport can be equipped with 1, 2, or 4 read, write, and erase heads to give unformatted capacity of 2.88M bytes/cartridge. **Kennedy Co,** 540 W Woodbury Rd, Altadena, CA 91001.
Circle 258 on Inquiry Card

CRT DISPLAY CAPABILITY OPTION

400W display modules have a 40-char line option which provides double-wide characters for readability. The unit's memory stores 2000 char in a 50-line x 40-char format. 24 lines of data are viewable at one time; the remaining 26 are hidden and can be accessed in roll or scroll mode.



Optional upper/lower case char display writes in a 7 x 10 dot matrix in a 10 x 12 dot field, displaying 20 lines of 80-char alphanumerics, with 5 additional lines that can be accessed in roll or scroll mode. Three character accents are std—blink, dim, and reverse video; cursor is displayed as a blinking field. RS-232 data interface is std, with 20-mA interface optional. Unit has RS-170 compatible video output. **Ann Arbor Terminals, Inc,** 6107 Jackson Rd, Ann Arbor, MI 48103.
Circle 259 on Inquiry Card

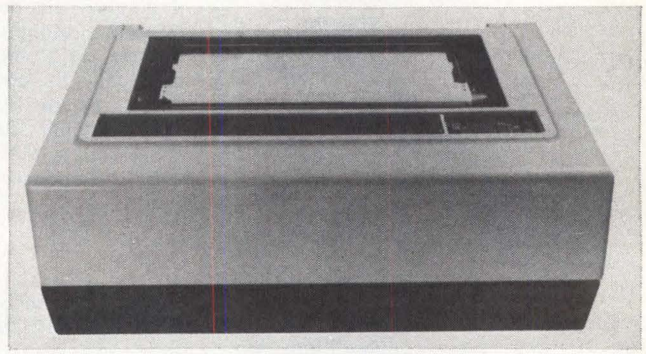
LOGIC CARD WITH ON-DELAY TIMERS

Consisting of four adjustable, multirange, on-delay timers, solid-state logic card performs functions of four separate cards. Each timer has four timing ranges: 0.02 to 2, 0.05 to 9, 0.1 to 75, and 0.5 to 600 s. Desired range for each is selected by means of a 2-pole rocker DIP switch. Timing within each range is adjusted with a potentiometer which is mounted on the card and accessible from the front of the card rack. In addition to a true and inverted output, the card has an interval output. Fanout for each output is 25 loads. Repeat accuracy (with variations in temp and cycle time) is ±1% typ and ±5% max. Reset time is 100 μs. The unit can also be used as a square wave oscillator. **Tenor Co, Inc,** 17020 W Rogers Dr, New Berlin, WI 53151.
Circle 260 on Inquiry Card

MICROPROCESSOR-BASED UHF MULTICOUPLER

Approximately one-third the size and weight of units currently in service, device meets all applicable military specs, and incorporates built-in test equipment. Basic 4-port unit can be reconfigured to combine from 2 to 8 radio sets into a common antenna, and is designed to interface with the AN/SRC-20 radio set and the AN/WSC-3 line-of-sight and satellite terminal. Changing single card makes the device compatible with the Navy Telecommunications System interface. Improved filter selectivity reduces mutual interference. A frequency management feature prevents operation of two or more radios at or near the same frequency. **E-Systems Inc, ECI Div,** Box 12248, St Petersburg, FL 33733.
Circle 261 on Inquiry Card

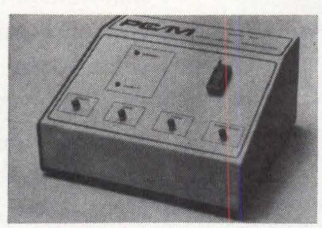
SERIAL PAGE PRINTER



Model 4540 uses a printhead that has hammers instead of needles or wires, and is based on a stored-force principle in which print hammers are mounted on flexible arms held back by electromagnets. For each impact, holding current is cut off and the hammer snaps forward. Using a pull-back impulse instead of a print impulse allows an extremely tight, small head, guaranteed to produce 500M characters. Mechanical print force reduces effective power consumption. With microprocessor control and a variety of interface options, the unit fits any application needing serial printout in volume. There are 12 character sets, including OCR-A numerics and Katakana. **Facit-Addo, Inc,** 66 Field Point Rd, Greenwich, CT 06830.
Circle 262 on Inquiry Card

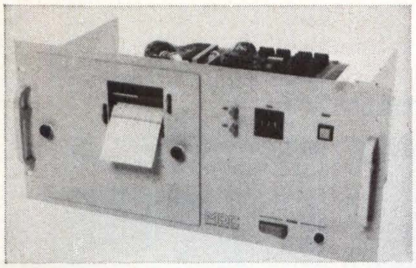
INTELLIGENT PROGRAMMER FOR CMOS ERASABLE ROMs

A terminal-interactive programmer for Intersil's 6603 and 6604 4096-bit p/ROMs, model 66 contains a microprocessor and 4096-bit RAM buffer, and can be operated standalone from its front panel or interactively with CRT or TTY terminal through RS-232 or 20-mA current loop interfaces.



It can also communicate with a computer and/or automatic IC test equipment for automated online p/ROM programming. Built-in features include a full complement of editing capabilities for loading and checking the RAM buffer and/or 660X EPROM, ability to accept all popular paper tape formats, firmware for p/ROM copying and verifying, and a front panel erase-check capability. **Pacific Cyber/Metrix, Inc,** 3120 Crow Canyon Rd, San Ramon, CA 94583.
Circle 263 on Inquiry Card

PRINTER FOR DIGITAL MULTIMETERS AND COUNTERS



For use with Data Precision model 3400 and 3500 multimeters, 300 series 16- or 21-col printers are available in benchtop or rackmount packages. Quiet operation is achieved using a pressure printing technique; 2-color printing is provided by using an easy-to-load ink ribbon cassette. Units are available with up to 6 col of floating decimal points, and can include a date/time clock and event counter as options. **Master Digital Corp,** 1308-F Logan Ave, Costa Mesa, CA 92626.
Circle 264 on Inquiry Card

PRINTED CIRCUIT BOARD FAULT FINDER

Capable of locating shorted runs buried in multilayer circuit boards, the model 911 Short Sniffer enables technicians to locate and patch around defective runs, and serves as a diagnostic tool to aid in circuit board failure analysis. The device indicates the direction of shorted conductors and pinpoints the location of the short. Indication is by audible clicks that increase in frequency as the short is approached, as well as meter indication. **Idlewild Associates,** PO Box 41, McMinnville, OR 97128.
Circle 265 on Inquiry Card

ROUND CONDUCTOR RIBBON CABLE

Jet-Flecs, precision center-to-center controlled cables of predictable and consistent electrical characteristics, are available in #28 AWG stranded (7/36) conductors. Design allows separation of individual or groups of conductors from cable. UL listed at 105°C and 300 V rms, they are FR-1 rated under UL flammability specs. Cables mate with 4700 connector system and compatible insulation displacement systems. **Molex Inc,** 2222 Wellington Ct, Lisle, IL 60532.
Circle 266 on Inquiry Card

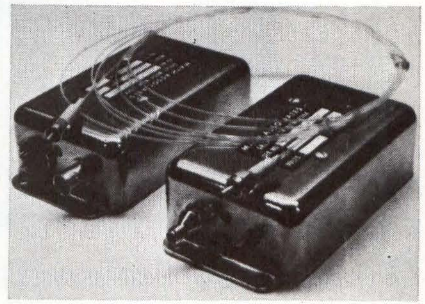
750-LINE/MIN SYSTEM/3 PRINTER

Heavy duty, precision 132-col printer possesses chaintrain print quality and performance. Character links which ride on a monorail track compose chaintrain and assure alignment and print quality. Std features include a sound deadening cabinet, static eliminator, paper puller, single line memory buffer, EBCDIC (lc) 48-char set and coding, and open Gothic char style. Spacing is 10 char/in and 6 or 8 lines/in selectable. Single line advance is 20 ms with a paper slew rate of 20 in/s (50.8 cm/s). **Digital Associates Corp,** 1039 E Main St, Stamford, CT 06902.
Circle 267 on Inquiry Card

PDP-11 FLEXIBLE DISC UTILITY PROGRAM

Translator-11 program is applicable to any PDP-11 installation with 8k memory, peripherals required to support RT-11 operating system, and compatible IBM 3740 flexible disc system. Program allows preparation of source material on data entry equipment, then transscribes material into RT-11 usable files; reverse transcription from RT-11 files to IBM 3740 data sets is supported. Special program features support multiple volume data sets, record blocking and deblocking, variable length data management, and spanned record management. **Ex-Cell-O Corp, Remex Div,** 1733 Alton St, PO Box C-19533, Irvine, CA 92713.
Circle 268 on Inquiry Card

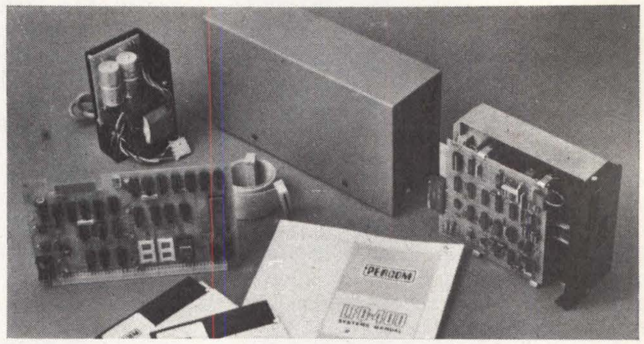
FIBER-OPTIC DATA TRANSMISSION SYSTEMS



Consisting of separate, self-contained transmitters and receivers, three analog links cover the range of dc through 30 MHz and encompass most industrial applications, audio and video transmissions, and wideband analog signal needs; while three digital links cover the range of 0 through 30 x 10^6 pulses/s. Units feature integral power supplies and operate from low voltage ac or dc, or from 115/230 V, 50-60 Hz with an external plug-in transformer. **Math Associates, Inc,** 320 Northern Blvd, Great Neck, NY 11021.
Circle 269 on Inquiry Card

PRODUCTS

SMALL FLOPPY STORAGE SYSTEM



A complete 1-drive LFD-400 system for the SS-50 bus includes a controller PC board, PROMware disc operating system, disc drive and drive power supply, interconnecting cable, two minidiskettes®, and a compact enclosure to house drive and drive power supply. Controller board, which is installed in an SS-50 bus slot of the host computer, includes low voltage drop regulators, proprietary bit shifting compensation circuit, inactivity time-out circuit to increase drive motor life, and provision for 3k bytes of p/ROM. Controller p/ROM may be used completely independent of disc and operating system. DOS and miniDOS™ operating systems allow existing software to be used with simple patches. **Per-Com Data Co, Inc,** 318 Barnes, Garland, TX 75042.
Circle 270 on Inquiry Card

μP-BASED SMALL BUSINESS COMPUTER

Two configurations of a microprocessor-based integrated business system provide computer capabilities to small businesses. A hard disc system, the MITS 300/55, includes a MITS/Altair™ 8800b turnkey processor with 64k words of dynamic RAM, 1k of p/ROM, B-100 CRT terminal, C-700 printer, serial I/O interface, and BASIC language software. The CRT is a 12" (30.5-cm) nonglare monitor which displays 24 lines of 80 char/line with a memory page of 1920 characters. Printer speed is 60 char/s, 26 lines/min. The 125 is identical except that it includes two floppy discs in place of the hard disc. **Pertec Computer Corp, Microsystems Div,** 21111 Erwin St, Woodland Hills, CA 91367.
Circle 271 on Inquiry Card

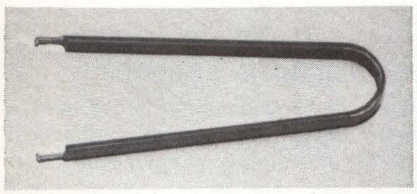
APL/ASCII CRT DISPLAY TERMINAL

Concept APL terminal combines full true APL overstrike capability with ability to implement powerful microprocessor-based capabilities. Features include a software-controlled display partitioning technique called windowing, shared printer capability, line drawing graphics, up to 19 function keys, character accents, text editing capabilities, CPU driven ASCII/APL run mode control, tilt/swivel screen, and detached keyboard. Unit design emphasizes human engineering, ease of programming, and ease of use, while capabilities expand options available to the APL programmer. **Human Designed Systems, Inc,** 3700 Market St, Philadelphia, PA 19104.
Circle 272 on Inquiry Card

PDP-11 SYSTEM INTERFACE

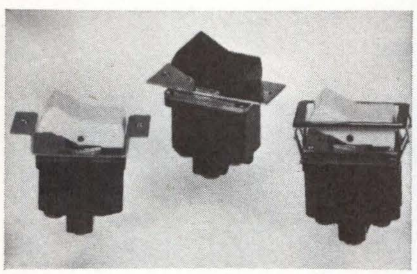
Model 2041-01 provides address selection, interrupt control, and device interface logic for use between PDP-11 and a peripheral device. It features DIP switch address and vector selection; no jumpers are necessary. Interface is fully hardware and software compatible with DEC™ systems. Packaged on a single quad module, it uses program I/O facility, provides 16-bit data out and in plus 6 bits of control and status information, and utilizes two onboard flat cable connectors for data transfer to external device. **Gen/Comp Inc,** 6 Algonquin Rd, Canton, MA 02021.
Circle 273 on Inquiry Card

DIP/IC EXTRACTOR TOOL

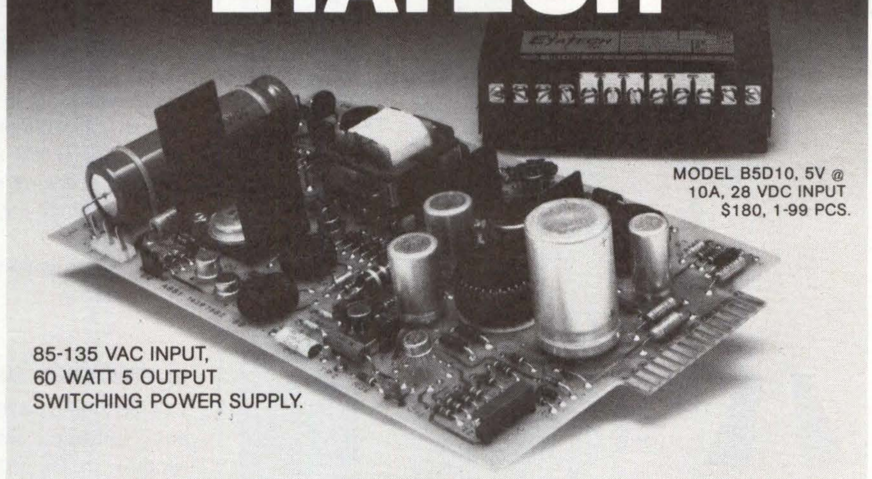


EX-1 Extractor, suited for hobbyists or lab engineers, features 1-piece spring steel construction. Tool will extract all LSI, MSI, and SSI devices of from 8 to 24 pins. **O K Machine and Tool Corp,** 3455 Conner St, Bronx, NY 10475.
Circle 274 on Inquiry Card

ENVIRONMENTALLY-SEALED ROCKER SWITCHES

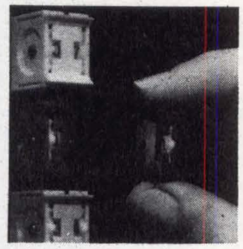


Available in snap-in bezel, flush, or subpanel mounting; and in 1-, 2-, and 4-pole circuit configurations, commercial switches resist dust, dirt, and liquid contaminants found in harsh environments. They are rated for 20k electrical operations, and have a flame retardant mineral-filled melamine phenolic base, die cast aluminum frame, high impact nylon rocker, and screw-type terminals. Seals are located around the bushing and between the base and frame. Special options are available. **Cutler-Hammer,** PO Box 463, Milwaukee, WI 53201.
Circle 275 on Inquiry Card



PRODUCTS

MINIATURE THUMBWHEEL SWITCHES



To simplify installation, while reducing weight and size, switch rotors and housings are provided; the stator is artwork used to produce the photoetch PC board master. Through-holes are used to locate and secure switch housing to board. This concept reduces material and manufacturing costs, and eliminates need for electrical connections to stator contacts. Factory-assembled switch housing is molded from a thermoplastic acetal resin with a concealment flange and stabilizers for secure mounting. Single 0.850 x 0.830 x 0.300" (2.159 x 2.108 x 0.762-cm) housing contains rotating contacts. Current ratings are 1.5 A (nonswitching) and 0.125 A (switching). **AMP Inc,** Harrisburg, PA 17105.

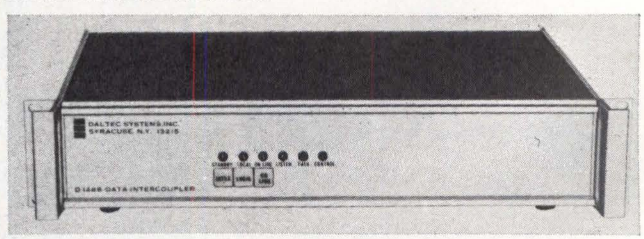
Circle 276 on Inquiry Card

IR-EMITTING DIODE FIBER-OPTIC SOURCES

TXES475 and -476 series GaAlAs IR-emitting diodes have a peak emission wavelength of 790 nm to match an optical window in Du Pont's PFX-PIR IR-transmitting plastic fiberoptic cable, and achieves two times higher optical output powers than shorter wavelength emitters. Mounted in a modified TO-18 type package, devices have an integral PFX-PIR140 fiber-optic cable for coupling optical power from emitter chip. Output end of integral cable is terminated in an AMP std fiber-optic cable connector. Core diameter of the single plastic fiber is 368 μm. This is compatible with coupling to various commercially available 7- and 19-strand glass fiber bundles. **Texas Instruments Inc,** PO Box 5012, MS 308, Dallas, TX 75222.

Circle 277 on Inquiry Card

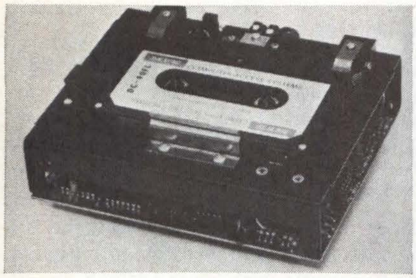
DATA INTERCOUPLER



Capable of transferring BCD and binary data to and from computer I/Os at rates to 30k bytes/s, D1488 allows any digital instrument to become compatible with the IEEE 488-1975 bus. It can act as a controller and the data format is programmable. As a 10-digit talk and/or listen device interface, simple control functions may be included to eliminate the need for an external controller. An internal Z-80 microprocessor executes a program stored in p/ROM to implement interface operation. All data movement and decision functions are under microprocessor control. Program modifications can be downloaded from controller into internal RAM, permitting functions to be modified to meet requirements. **Daltec Systems, Inc,** PO Box 157, Syracuse, NY 13215.

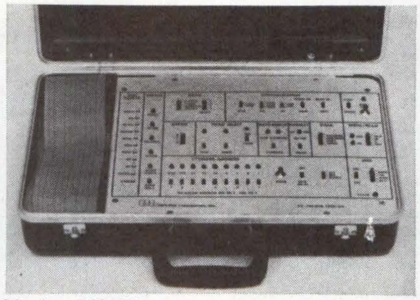
Circle 278 on Inquiry Card

DIGITAL CASSETTE TRANSPORT



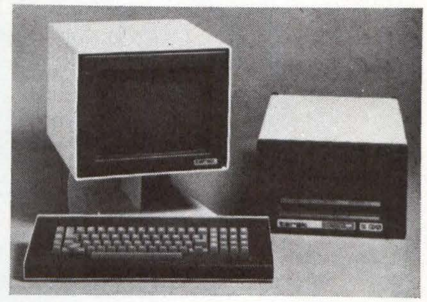
Model 450B incorporates a speed control system providing 1% long term accuracy at the heads in a reel-to-reel transport without use of a prerecorded digital clock track. Fully ANSI/ECMA compatible, transport allows interchange of cassette tapes with any ANSI/ECMA compatible system. 2 data tracks are available, allowing data storage up to 720k bytes/cassette. R/W speeds from 10 to 40 in/s (25 to 102 cm/s) provide data transfer rates up to 32,000 bits/s using bi-phase level encoding std. Read after write heads and optical EOT/BOT sensing are std. **MFE Corp,** Keewaydin Dr, Salem, NH 03079.
Circle 279 on Inquiry Card

DISC EXERCISER



Model DX-500 possesses essential testing features of larger DX-1000 except digital readout of r/min, seek time, and sector count. Series of switch selectable, preprogrammed exercises is provided for isolation and identification of data, format, and seek errors in linked systems of 1 to 4 disc drives. Functions include restore, manual and incrementing seek, and random patterns of incrementing. Exerciser stops on error, or indicates an error and keeps on running to allow continuation of overnight burn-in. **Wilson Laboratories, Inc,** 2536-D E Fender Ave, Fullerton, CA 92631.
Circle 280 on Inquiry Card

GRAPHICS COMPUTER SYSTEM



Standalone tabletop computer system features raster-scan graphics capability. System includes LSI-11 microcomputer, single floppy disc drive and controller to handle up to 4 drives, 56k bytes of R/W MOS RAM, single asynchronous serial interface, video electronics, 12" (30-cm) CRT display, and keyboard. Graphics are displayed in bit-map fashion using a 320 x 240 dot matrix refreshed directly from main memory. Text and graphics are independently controlled and simultaneously displayed. **Terak Corp,** 14425 N Scottsdale Rd, Suite 100, Scottsdale, AZ 85260.
Circle 281 on Inquiry Card

CIRCLE 116 ON INQUIRY CARD

PRODUCTS

BUFFERED MAGNETIC TAPE TERMINAL

An intelligent data terminal, 3801 uses an ANSI/ECMA Philips cassette drive and is RS-232-C compatible. Its fully editable data buffer holds up to 260 char; block rewrite capability is provided and insertion of blocks or entire paragraphs into previously written text is possible. Automatic high speed block search and verify capability can be controlled either by tape information or operator input. 30 ASCII remote commands control the unit which presents 13 plain English messages. Other features include 0.5M-byte storage/cassette, switch-selectable asynchronous baud rates from 110 to 19,200, ASCII text as well as transparent binary modes, fixed or variable block length, and auto error-check and retry. **Interdyne Co,** 14761 Califa St, Van Nuys, CA 91411.
Circle 282 on Inquiry Card

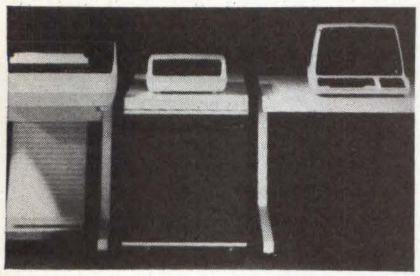
DUAL-HEADED FLEXIBLE DISC DRIVE

Incorporating two ceramic read/write heads which allow recording or reading of data on both sides of a dual-sided flexible disc, the 552 significantly reduces operator handling of disc media, and improves accessibility of data. Interface, dimensional characteristics, and 80% parts commonality with 550 single-head disc drive allow simple conversion. The unit uses Markette™ 2 media, recording 492k bytes in IBM 4964 format or up to 1600k bytes unformatted. Access time is 3 ms/track. Data transfer rate is 250k bytes/s in single density recording mode. With an appropriate controller, the unit can be operated in double-density mode without modification or additional electronics. **Memorex Corp,** San Tomas at Central Expwy, Santa Clara, CA 95052.
Circle 283 on Inquiry Card

16-BIT INTELLIGENT TERMINAL

Operating within the text management system, the Ph.D offers 16-bit processing power and architectural compatibility with large minis. System is based on the DEC PDP-11/03 processor with 4k 16-bit words of random access storage, serial I/O interface, and CRT for use as standalone system and component in distributed network. Std software includes PDP-11 operating systems and languages. Communications options include asynchronous, synchronous, SDLC, and programmable communications interfaces. System options include front-mounted microcassette, 32 16-bit words of user-available RAM, 4 dual-density floppy discs, and 600-line/min printer. **Computer Products Unlimited, Inc,** 4 Professonal Dr, Ste 130, Gaithersburg, MD 20760.
Circle 284 on Inquiry Card

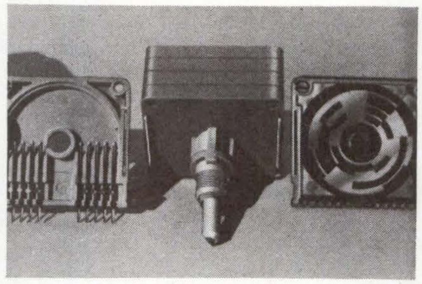
HARD DISC, BUNDLED BUSINESS COMPUTER



CPU, 32k memory, 10M-byte fixed media Winchester-type drive, interactive video display terminal, cartridge tape drive, and 120-char/s bidirectional printer comprise the system 200 business computer. Features include random-access, large storage capability, and simultaneous updating of files. A 9-module application package is available with the system; the software, based on modules and parameters, accommodates variations while eliminating costly programming changes. **Basic/Four Corp,** PO Box C-11921, Santa Ana, CA 92711.

Circle 285 on Inquiry Card

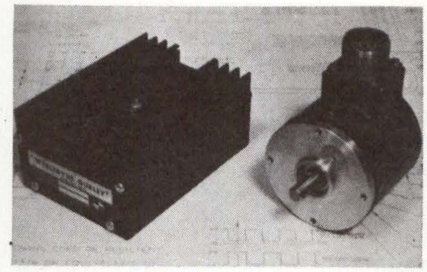
PROGRAMMABLE ROTARY ENCODED LOGIC SWITCH



For use as a "digital pot" or shaft encoder with or without a detent, thereby eliminating the ADC required with a std potentiometer, the switch senses the angular position of the shaft and digitally informs the interface of the shaft's position. Programmable to any code, the device features a plastic shaft and bushing; metal shaft and bushing or concentric shaft are also available. Resistive load switching is 0.125 A at 115 Vac; operating force is 14 to 24 in-oz (0.098 to 0.168 N•m). **Standard Grigsby, Inc,** 920 Rathbone Ave, Aurora, IL 60507.

Circle 286 on Inquiry Card

HIGH RESOLUTION ROTARY ENCODER



With resolution of up to 144,000 pulses/rev, model 8626 consists of size 29 encoder and a separate electronics package. Salient features include output data rates up to 500 kHz; quadrature square waves, or direction-sensed pulse outputs; complete DTL, TTL, HTL, or CMOS compatibility; and optional once-per-revolution marker pulse. Unit also includes resolution as fine as 9 arcseconds; choice of LED or 50,000-h lamp light source; synchro-groove, or flatface mounting; and optional shaft oil seal. **Teledyne Gurley,** 514 Fulton St, Troy, NY 12181.

Circle 287 on Inquiry Card

LITERATURE

Ball Bearing Slides

Selector guide differentiates chassis and drawer slides and includes data depicting dimensioned sections, special designs, and shock and vibration control components. **Grant Hardware Co, div of Buildex Inc,** Haverstraw, NY.
Circle 300 on Inquiry Card

Standard Line Connectors

Catalog covers materials and finishes, electrical data, contact arrangements, and tooling accessories with cutaway drawings and photos on circular, audio, rectangular, and microminiature connectors. **ITT Cannon Electric, div of International Telephone and Telegraph Corp,** Santa Ana, Calif.
Circle 301 on Inquiry Card

Cassettes

Physical, operating, magnetic, and environmental data; dimensions; and performance for Verbatim™ cassette series are detailed and pictured in brochure. **Information Terminals Corp,** Sunnyvale, Calif.
Circle 302 on Inquiry Card

GPIB Interface

Pamphlet features comprehensive description of M6800-based interface that explains design, program listing, and schematics, and serves to educate industry on IEEE 488 applications. **Tektronix, Inc, Information Display Group,** Beaverton, Ore.
Circle 303 on Inquiry Card

Memory Testing

Colorfully illustrated booklet outlines factors for selection of semiconductor memory test equipment, including timing resolution, automatic calibration, software, and analog performance. **Teradyne, Inc,** Boston, Mass.
Circle 304 on Inquiry Card

Measurements/Computations

1978 Electronic Instruments and Systems catalog includes photos, product descriptions, specs, tables, and charts for those concerned with measurement or computation. Write on company letterhead to **Hewlett-Packard Co,** 1501 Page Mill Rd, Palo Alto, CA 94304.

Single-Board Computer

Advantages, operation, and features of the MSC 8001 Z80/SBC 80 Multibus computer are detailed with colored block diagrams and descriptions that illustrate functions and interaction among its elements and buses. **Monolithic Systems Corp,** Englewood, Colo.
Circle 305 on Inquiry Card

Modular Power Supplies

Catalog describes over 200 encapsulated ac-dc and dc-dc power supplies, including four latest additions. **Wall Industries, Inc,** Bedford, Mass.
Circle 306 on Inquiry Card

MOS Circuits

Detailing over 80 std LSI circuits, catalog furnishes descriptions and functional diagrams of VMOS memory devices, microprocessor families, and communications and consumer products. **American Microsystems, Inc,** Santa Clara, Calif.
Circle 307 on Inquiry Card

Spectrum Analysis

Theory of FFT instrumentation is presented in 48-page handbook, "Spectrum Analysis —Theory, Implementation, & Applications," which provides an introduction followed by expository sections. **Rockland Systems Corp,** West Nyack, NY.
Circle 308 on Inquiry Card

Decoder/Driver

Bulletin on model DD-700 contains tabular diagrams and condensed information such as performance specs, max ratings, truth table, and output current ratio and pin designations. **Beckman Instruments, Inc, Information Displays Operations,** Scottsdale, Ariz.
Circle 309 on Inquiry Card

Rotary Lever Switches

Diagrams and std circuit configuration drawings for types 184 and 187 std switches, along with description of Acorn 12-position switch for PC board insertion, are presented in 4-page brochure. **Oak Industries, Inc, Switch Div,** Crystal Lake, Ill.
Circle 310 on Inquiry Card

Chip Capacitors

Reference handbook, illustrated with performance graphs and comprehensive tables, covers such areas as electrical properties, classes of dielectrics, and testing parameters of ceramic chip capacitors. **Johanson Dielectrics Inc,** Burbank, Calif.
Circle 311 on Inquiry Card

Minicomputers

With topics including computation abilities, languages, operating systems, programming aids, peripherals, and typ system configurations, brochure details hardware and software features of Eclipse S/130 systems. **Data General Corp,** Westboro, Mass.
Circle 312 on Inquiry Card

Miniature Rectangular Connectors

Containing full physical and electrical specs, catalog covers free hanging, panel mount, and PC board versions along with strain reliefs, commoning bars, and application tooling of MR series of connectors. **AMP Inc,** Harrisburg, Pa.
Circle 313 on Inquiry Card

Solid-State Modems

Data sheet describes and illustrates GDC 212A modem, which transmits and receives serial data at two rates, and features local and remote signal loopback diagnostics. **General DataComm Industries, Inc,** Wilton, Conn.
Circle 314 on Inquiry Card

Add-On Memories

Ability of 370/158 and /168 memory packages, which are IBM compatible, to attain higher reliability is detailed in brochure containing specs on each model. **Electronic Memories and Magnetics Corp, Computer Products Div,** Hawthorne, Calif.
Circle 315 on Inquiry Card

Interface Standard

RS-449, a std developed to provide functional interface between data terminal equipment and circuit-terminating equipment, is interpreted in bulletins available for $13.75 from the **Standards Sales Office, EIA,** 2001 Eye St, NW, Washington, DC 20006.

Data Conversion Components

Handbook gives tabular selection guides, application information, and data sheets concerning monolithic, hybrid, and modular components and interface systems. **Datel Systems, Inc,** Canton, Mass.
Circle 316 on Inquiry Card

Signal Processing Circuits

Product brochure presents key specs and features of LSI bipolar, high performance digital multipliers, and multipliers with onchip accumulators. **TRW Inc, LSI Products,** Redondo Beach, Calif.
Circle 317 on Inquiry Card

Acoustic Couplers

Catalog acquaints user with logistics and mechanics of timesharing with acoustic couplers and display or hardcopy terminals. **Omnitec Corp,** Phoenix, Ariz.
Circle 318 on Inquiry Card

Breadboards

Describing a line of breadboards, connectors, racks, and interface boards, 32-page catalog includes dimensional diagrams, accessories, and load options. **Douglas Electronics Inc,** San Leandro, Calif.
Circle 319 on Inquiry Card

Fault Tracers

Descriptions of modes and features of 2220 Bug Hound, such as its current-tracing probe, are illustrated in brochure through graphs and diagrams. **GenRad, Inc,** Concord, Mass.
Circle 320 on Inquiry Card

Data Communications

Including full product information, two charts are available on RS-232-C and current loop data communications, and ASCII code. **Termiflex Corp,** Nashua, NH.
Circle 321 on Inquiry Card

Panel Indicators

Catalog provides detailed specs and outline dimensions on digital panel meters and detectors for process control and measurement applications. **Anadex,** Chatsworth, Calif.
Circle 322 on Inquiry Card

Wire Line Modems

Modem 263A, a digital data set that transmits and receives data at rates of 2.4, 4.8, 9.6, or 56k bits/s, is depicted in brochure containing features and installation diagrams. **GTE Lenkurt Inc,** San Carlos, Calif.
Circle 323 on Inquiry Card

Signal Processors

With a separate section devoted to multiprocessor systems, a list of FFT computation times, and block diagrams, brochure features SPS-61 and -81 programmable digital processors. **Signal Processing Systems, Inc,** Waltham, Mass.
Circle 324 on Inquiry Card

Keyboards

"PRO" keyboard for personal computer, hobbyist, and OEM users is detailed in catalog that includes schematic drawings, charts, diagrams, and complete std and optional specs. **Cherry Electrical Products Corp,** Waukegan, Ill.
Circle 325 on Inquiry Card

Workstations

Illustrated brochure on Deskware™ line contains self-planning guide for selection of workstations which combine modular design concept with options for expansion and modification. **Mini-Computer Systems, Inc,** Anaheim, Calif.
Circle 326 on Inquiry Card

Technical Publications

Catalog entitled *Publications of the National Bureau of Standards* (number 003-003-01743-4) includes complete listing of scientific, technical, and consumer publications of 1976. Price is $8.25. **Superintendent of Documents, U.S. Government Printing Office,** Washington, DC 20402.

Digital Logic Design

Conference proceedings publication covering recent developments in digital logic involving spectral and symmetry techniques, universal logic modules, and fault diagnosis of combinatorial and sequential systems is available for $10, including postage. **School of Electrical Engineering, U of Bath,** Bath BA2 7AY, England.

Backpanels

Brochure offers photos and specs of system that features precision circuit boards, pin connectors, and custom backpanel assembly components. **Kalmus & Associates, Inc,** Broadview, Ill.
Circle 327 on Inquiry Card

Power Converters

Catalog gives full specs on dc-dc, miniature hybrid, and 400-Hz ac-dc single- and triple-phase converters, as well as additional product lines. **Tecnetics, Inc,** Boulder, Colo.
Circle 328 on Inquiry Card

Coaxial Cables

Featuring descriptive data, nominal loss characteristic charts, and cable specs, short-form catalog describes subminiature communication and control cables and assemblies. **American Components Inc,** Conshohocken, Pa.
Circle 329 on Inquiry Card

Crystal Testing

Application note discusses characterization of quartz crystals for use in filters or oscillators using a conventional spectrum analyzer and tracking generator. **Marconi Instruments, div of Marconi Electronics, Inc,** Northvale, NJ.
Circle 330 on Inquiry Card

Oscillators

Technical discussions and application notes comprise catalog on high stability frequency stds, frequency synthesizers, and crystal and voltage controlled oscillators. **Greenray Industries, Inc,** Mechanicsburg, Pa.
Circle 331 on Inquiry Card

Test Instruments

Short-form catalog features test instrument developments in nine product categories, designed for utilization in such areas as industry, quality control, and communications. **Leader Instruments Corp,** Plainview, NY.
Circle 332 on Inquiry Card

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

GUIDE TO PRODUCT INFORMATION

SALES OFFICES

NEW ENGLAND, NEW YORK STATE

Lindsay H. Caldwell
129 Cedar Hill Road
East Dennis, MA 02641
phone: (617) 385-2533

MIDDLE AND SOUTH ATLANTIC STATES

Hajar Assoc., Inc.
Emile H. Hajar
Paul Hajar
Silvio Mandino
521 5th Avenue
New York, NY 10017
phone: (212) 682-5844

MIDWESTERN STATES

Hajar Assoc., Inc.
Emile H. Hajar
Paul Hajar
Silvio Mandino
664 North Michigan Avenue
Suite 1010
Chicago, IL 60611
phone: (312) 337-8008

SOUTHWESTERN STATES

Lindsay H. Caldwell
129 Cedar Hill Road
East Dennis, MA 02641
phone: (617) 385-2533

WEST COAST STATES

Buckley Boris Assoc.
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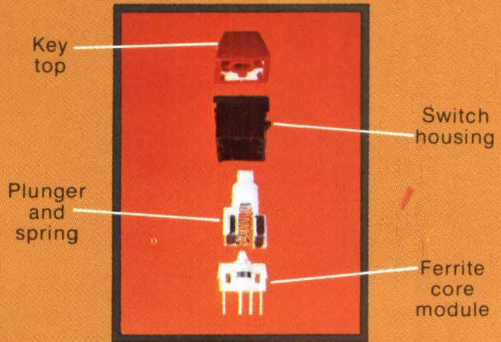
ADVERTISERS' INDEX

Cost efficiency you can put your finger on . . . CORTRON® SOLID STATE KEYBOARDS

Get your hands on a CORTRON Solid State Keyboard, and you'll soon find out why you can't judge all keyboards on initial price alone.

It's after installation that cost efficiency becomes most important. In life expectancy, ability to endure extreme environments, high speed operation without "misses," accuracy, downtime caused by beverage spillages, reliability, serviceability and human engineered features. That's where a CORTRON Solid State Keyboard really pays off.



Unique contactless key switch makes the difference. Utilizing ferrite core switching technology, the CORTRON Key Switch is mechanically simple (only 4 basic parts!) and has an ultra reliable 100 million cycle life test rating. CORTRON Keyboard Professionals can translate what this can mean to you in cost efficiency terms of MTBF (mean time before failure). CORTRON has actual customer experience of MTBF in excess of 40,000 hours.

They'll also explain other advantages you'll gain over competitive technologies such as Hall effect, reed switch, and capacitive switching. All in all, you'll find the CORTRON Key Switch offers unusual built-in protection against costly service calls and the hardship of downtime.

"Human engineered" keytops and key placement options give CORTRON low profile alpha numeric keyboards the familiar "typewriter feel" that promotes operator productivity and efficiency.

Nothing left to chance. CORTRON solid state keyboard materials, components, subassemblies, and final assembly are 100% inspected and tested to assure your specifications are met with plenty of room to spare.

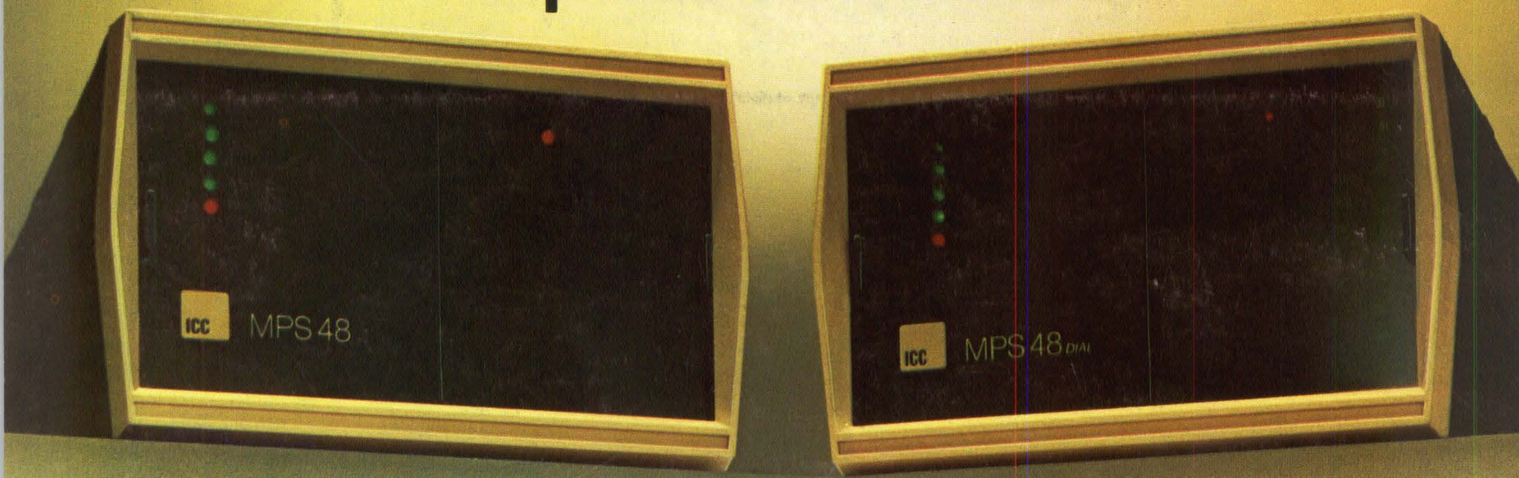
These are just a few of the cost efficiency benefits CORTRON offers you and your customers.

Cost efficiency you can put your finger on. For a greater insight into the cost efficiencies attainable with a CORTRON Solid State Keyboard, write or call for details: CORTRON, A Division of Illinois Tool Works Inc., 6601 West Irving Park Road, Chicago, Illinois 60634. Phone (312) 282-4040. TWX 910-221-0275.

itw CORTRON
A DIVISION OF ILLINOIS TOOL WORKS INC
THE KEYBOARD PROFESSIONALS

CIRCLE 120 ON INQUIRY CARD

These modems transmit at least 108 bits of data while other 4800 bps modems are still trying to equalize the line.



Data communication stops every time a modem switches between sending and receiving. That's normal. But since this switching often occurs more than once a second, the length of this "turnaround time" is very significant to the user.
That's where our MPS 48 modems offer a special advantage.
Equalization time is only 26 milliseconds—about half that of conventional modems.
So, while other 4800 bps modems are waiting for a Clear to Send signal, the MPS 48 transmits at least 108 bits of information.
With this ultra-fast turnaround time, you get maximum data throughput, even over poor quality lines.

There are 10 more advantages described in our new 16-page booklet.
We'll gladly send you a copy.

Racal-Milgo™ – the new name for ICC

Racal-Milgo, Inc., 8600 N.W. 41st Street, Miami, Florida 33166, Telephone (305) 592-8600
In Europe: Racal-Milgo Limited, Reading, Berks, England

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CIRCLE 121 ON INQUIRY CARD