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THE MAGAZINE OF DIGITAL ELECTRONICS

MARCH 1978

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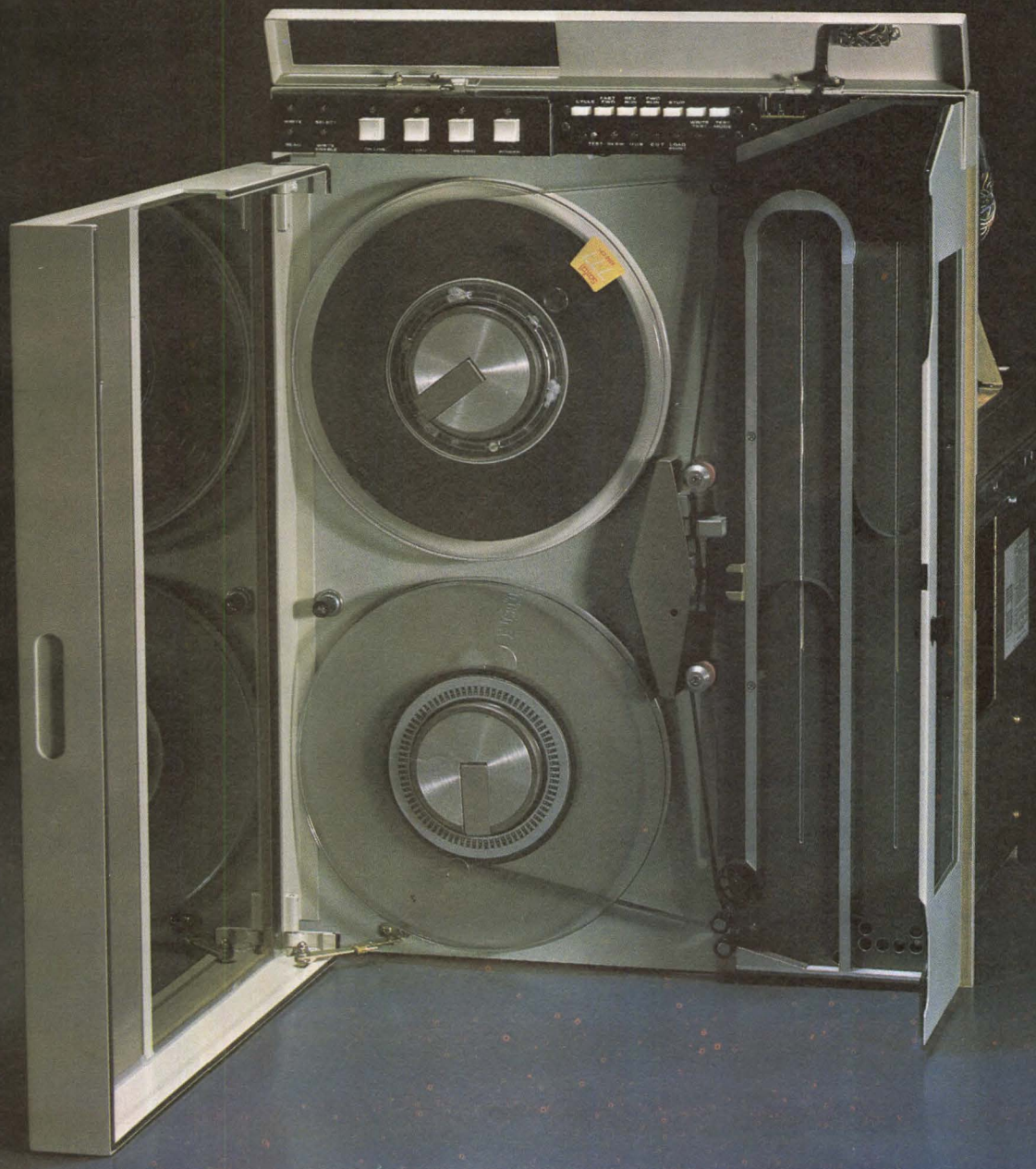

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COMPUTER DESIGN

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MARCH 1978

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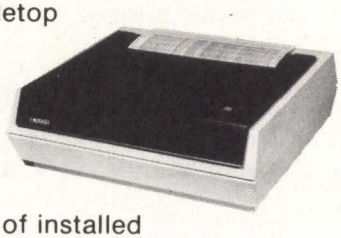

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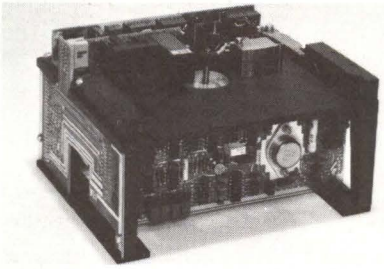

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LETTERS TO THE EDITOR

To the Editor:

I have many complaints about A. Scott McPhillips's article "Magnetic Tape Formatter Design Reduces Hardware/Software Requirements" (*Computer Design*, Nov 1977, pp 99-104). McPhillips has focused entirely on the formatter to tape drive data path; he ignored the input data path. This latter path sharply restricts the utility of the formatter.

For each input byte, the 8080 microprocessor must compute the parity of the byte and the byte's contribution to the block's CRCC. How long does this take? If he could do it in 20 instructions/character (I doubt it), then every byte would need 55 μs of processing before it could be written on the tape. At best his throughput would be 20k bytes/s; he need only use tape drives that match this throughput. The most common magnetic tape is 9-track recorded at 800 bits/in—a 25-in/s drive will give a 20k-byte/s throughput. A 45-in/s drive will sit idle about half the time—so why pay more for a faster drive?

Another complaint is that the formatter does not overlap bus input and tape output operations. When the microprocessor is writing on tape it does not look at the bus—consequently some data can be lost. At 25 in/s and 800 bits/in it takes at least 50 ms to write a 1k-byte block. (This 50-ms dead time also slows down the throughput.)

The formatter is of questionable utility. The 8080 is not fast enough to play character I/O for high speed peripherals. The formatter's architecture slows throughput without adding features like double buffering. Microprocessors have many applications in high speed peripherals—but be sure they can do the whole job: there's no reason to make a 25-in/s controller for a 45-in/s drive unless you like to throw money away.

Gerald Roylance
26A Surrey St
Cambridge, Mass

To the Editor:

The article "Design Guidelines for a Computer Voice Response System" by Paul Thordarson (see *Computer Design*, Nov 1977, pp 73-82) was interesting and informative, but not as complete a discussion as would be expected from its title and introduction. Although it may have been desirable to eliminate discussion of the fundamental technique used for many years by the earliest voice-response manufacturers, it seems strange that this technique was not mentioned in passing, since many vendors still market voice response devices based upon it. This technique, for reference, simply involved direct recording (either magnetic or photographic) of words or word segments on parallel tracks of a rotating drum. Access was very simple, of course, as long as simple messages with small vocabularies (typically 32-64 words) were desired. This technique has the great advantage of very little interaction with the processor, since outputs of seconds in duration could be provided with only one to two bytes of information (ie, the track number) rather than the tens of thousands required by the digital sampling techniques described by Thordarson.

The major disadvantage of this direct recording technique, other than vocabulary size, was the fact that audio or voice output was quantized in time segments equal to a fixed fraction of the rotation time of the drum, and was typically 0.5 or 0.6 s. A smooth, continuous message is very difficult to provide using this technique.

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This voice-response technique (Voicepac 2000) cannot be disregarded in any serious discussion of state-of-the-art voice response systems.

W. Dwain Simpson
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APR 12-14—Pattern Recognition and Artificial Intelligence, Nassau Inn, Princeton, NJ. INFORMATION: Prof Y. T. Chien, Dept of Computer Science, U of Conn, Storrs, CT 06268. Tel: (203) 486-4816

APR 17-20—Design Engineering Show, McCormick Pl, Chicago, Ill. INFORMATION: Clapp & Poliak, Inc, 245 Park Ave, New York, NY 10017. Tel: (212) 661-8410

APR 18-20—16th Annual Internat'l Reliability Physics Sym, Town and Country Hotel, San Diego, Calif. INFORMATION: Jerome Sohn, Publicity Committee, Charles Stark Draper Laboratories, 555 Technology Sq, MS 55, Cambridge, MA 02139. Tel: (617) 258-4637

APR 18-20—Mini/Micro Computer Conf and Expo, Philadelphia, Pa. INFORMATION: Robert D. Rankin, 5528 E LaPalma Ave, Suite 1, Anaheim, CA 92807

APR 18-20—The Society for Information Display Internat'l Sym, Hyatt Regency Hotel, San Francisco, Calif. INFORMATION: Lewis Winner, 152 W 42nd St, New York, NY 10036. Tel: (212) 279-3125

APR 24-26—28th Electronic Components Conf, Disneyland Hotel, Anaheim, Calif. INFORMATION: J. A. Bruorton, Mktg Administration Dept, Union Carbide Corp, PO Box 5928, Greenville, SC 29606. Tel: (803) 963-6348

APR 25-26—26th Annual National Relay Conf, Oklahoma State U, Stillwater, Okla. INFORMATION: School of Electrical Engineering, Engineering Ext 301 EN, Oklahoma State U, Stillwater, OK 74074

APR 28-30—PERCOMP '78, Long Beach Conv Ctr, Long Beach, Calif. INFORMATION: Royal Exposition Mgmt Corp, 1833 E 17th St, Suite 108, Santa Ana, CA 92701. Tel: (714) 973-0880

MAY 9-12—Internat'l Magnetics (INTERMAG) Conf, Palazzo Dei Congressi, Florence, Italy. INFORMATION: E. Della Torre, Dept of Electrical Engineering, McMaster U, Hamilton, Ontario L8S 4L7, Canada

MAY 10-12—3rd Internat'l Conf on Software Engineering, Hyatt Regency Hotel, Atlanta, Ga. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

MAY 15-16—2nd Internat'l Sym on Large Engineering Systems, U of Waterloo, Waterloo, Ontario, Canada. INFORMATION: Prof G. J. Savage, Dept of Systems Design, U of Waterloo, Waterloo, Ontario N2L 3G1, Canada

MAY 18—Trends and Applications: Distributed Processing, Gaithersburg, Md. INFORMATION: Distributed Processing, PO Box 639, Silver Spring, MD 20901

MAY 22-26—7th Annual Sym on Incremental Motion Control Systems and Devices, Hyatt Regency O'Hare, Chicago, Ill. INFORMATION: Prof B. C. Kuo, Dept of Electrical Engineering, U of Illinois at Urbana-Champagne, Urbana, IL 61801. Tel: (217) 333-4341

MAY 23-25—ELECTRO '78, Boston-Sheraton, Hynes Auditorium, Boston, Mass. INFORMATION: W. C. Weber, Jr, IEEE ELECTRO, 31 Channing St, Newton, MA 02158. Tel: (617) 527-5151

MAY 29-JUNE 7—INTERNEPCON MOSCOW '78 (Internat'l Electronics Production Conf), Expo-Ctr, Pavilion 1, Krasnaja Presnaja Pk, Moscow. INFORMATION: Harry Lepinske, Industrial & Scientific Conf Mgmt, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

JUNE 4-7—Internat'l Conf on Communications, Sheraton Hotel, Toronto, Ontario, Canada. INFORMATION: F. J. Heath, Power System Operation Dept, Ontario Hydro Electric Power System, 700 University Ave, Toronto M5G 1X6, Canada

JUNE 5-8—1978 Nat'l Computer Conf (NCC), Anaheim Conv Ctr, The Disneyland Hotel Comp, Anaheim, Calif. INFORMATION: AFIPS, 210 Summit Ave, Montvale, NJ 07645

JUNE 12-13—Microcomputer-Based Instrumentation Sym, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: Dr Helmut Hellwig, Nat'l Bureau of Standards, Rm A-1002 Administration, Washington, DC 20234. Tel: (301) 921-3181

JUNE 12-15—MIMI '78 (4th Internat'l Sym and Exhibition of Mini and Microcomputers and their Applications), Zurich, Switzerland. INFORMATION: Secretariat MIMI '78 Interconvention, c/o Swissair Postfach, 8058 Zurich, Switzerland

JUNE 12-16—7th Triennial IFAC World Congress, Helsinki, Finland. INFORMATION: IFAC '78 Secretariat, POB 192, 00101 Helsinki 10, Finland

JUNE 15—17th Annual Technical Sym of ACM and NBS, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: U.S. Dept of Commerce, Nat'l Bureau of Standards, Washington, DC 20234

JUNE 20-22—Internat'l Microcomputers, Minicomputers, Microprocessors '78 Conf, Palais des Exposition, Geneva, Switzerland. INFORMATION: Joseph C. Maurer, Industrial & Scientific Conf Mgmt, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

JUNE 21-23—Internat'l Sym on Fault Tolerant Computing, Toulouse, France. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901

SEMINARS

MAY 1-3—Plastic Part Design, Royal Inn/Airport, Atlanta, Ga. INFORMATION: Plastic Design Form Seminars, 1701 N Damen Ave, Chicago, IL 60647. Tel: (312) 278-9311

MAY 15-17—Computer-Communication Network Design and Analysis, Chicago, Ill. INFORMATION: Heidi E. Kaplan, Dept I4NR, New York Mgmt Ctr, 360 Lexington Ave, New York, NY 10017. Tel: (212) 953-7262

SHORT COURSES

APR 10-14—Data Communications Systems and Networks, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

APR 12-14—4th Annual Asilomar Workshop on Microprocessors, Pacific Grove, Calif. INFORMATION: Ted Laliotis, ASI, Inc, 840 Del Rey Ave, Sunnyvale, CA 94086. Tel: (408) 739-6700

JUNE 17-24—Advanced Microcomputer Interfacing and Programming Workshop, TSS Carnivale, Carribean. INFORMATION: Dr Norris Bell, Virginia Polytechnic Institute and State U, Continuing Education Ctr, Blacksburg, VA 24061. Tel: (703) 951-6208

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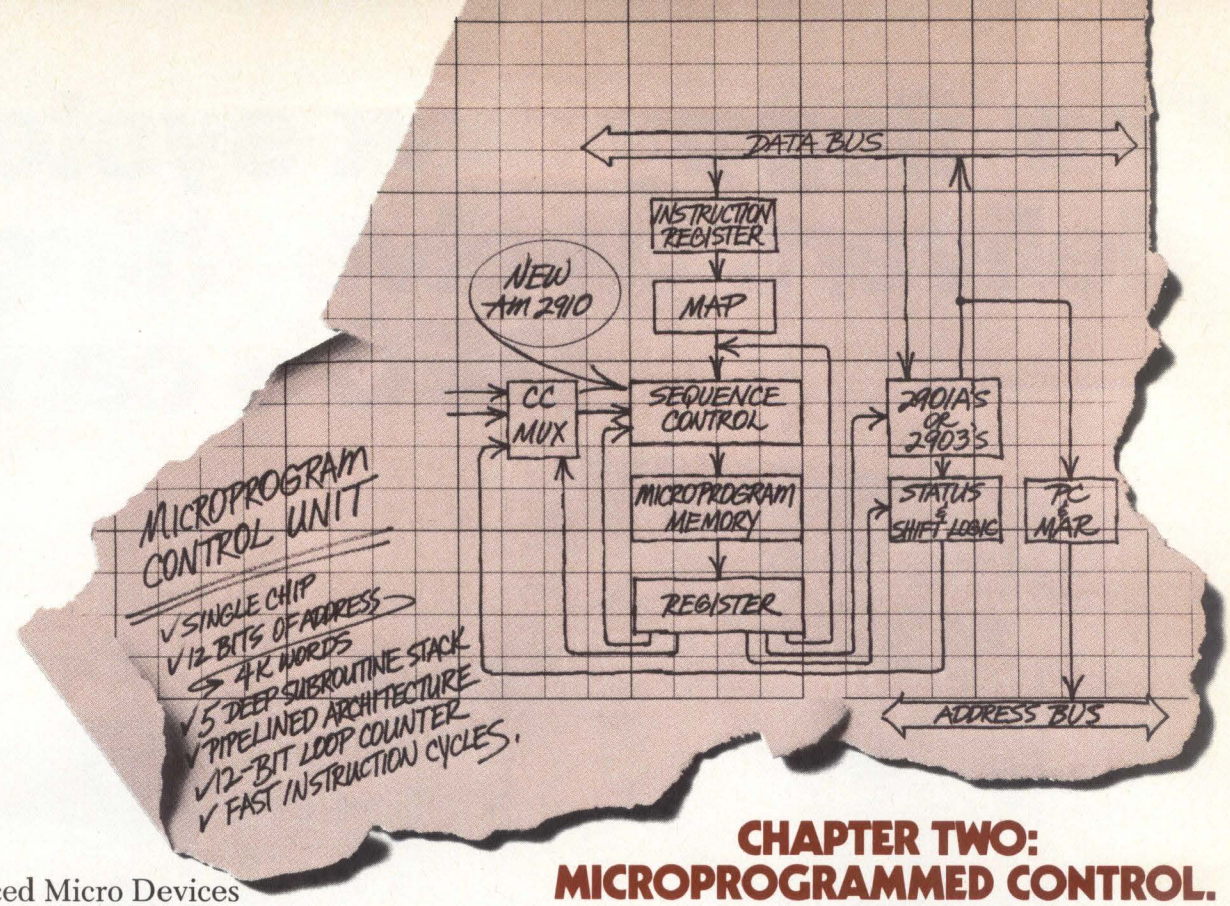

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Next, Chapter Three: The CPU.

SYNCHRONOUS TIMING ERROR CHARACTERISTICS

John E. Buckley

Telecommunications Management Corporation
Cornwells Heights, Pennsylvania

Data communications errors can result from incompatibilities between receiver and transmitter timings when asynchronously timed transmissions are being used, as last month's column revealed. Asynchronous timing generally is used for data transmissions of 1800 bits/s and less; synchronous timing is used almost universally over 1800 bits/s. Qualification of these timing methods and data rate ranges is necessary, however, since technically it is possible to use synchronous timing at low data rates. Most current interactive display terminals (CRTs) use asynchronous timing and are electronically capable of exchanging data at rates up to 9600 bits/s. However, they cannot have their inherent timing method easily modified; therefore, they simply retain the asynchronous timing even at data rates that are thought to be indicative of synchronous timing.

The modulator/demodulator (modem) and its associated data terminal are vital to the execution of the synchronous method, since both are active components that must be coordinated in order to generate and recover the transmitted signal. Error probabilities can therefore result from potential incompatibilities between each of these component areas, as well as between the transmitted signal and either of these components. Even if the two modems are each compatible with the transmitted signal, it is still possible to experience data errors because of a basic incongruity between the modem and its data terminal. With asynchronous timing, the passive modem is not involved in signal timing considerations. It merely converts analog and digital signal patterns into their counterparts at rates up to the designed linear bandpass of the modulator and demodulator sections.

This perspective of synchronous timing assigns the occurrence of data errors exclusively to the data receiver. It is important to realize that an actual data error does not exist in a data transmission until the signal is recovered erroneously. Adjustments in the data transmitter may correct some errors. Since actual data error occurrence, however, is a function of the data receiver, this discussion of synchronous timing error characteristics will focus on the data receiver perspective.

When data are transmitted using this method, a continuous time spectrum of data signals is treated as a unit. The timing aspects are generated and recovered with respect to the entire time spectrum, without regard to the individual segments that comprise that spectrum. While asynchronous transmission focuses on each data segment (ie, character) as an independent unit, synchronous transmission deals with multiple segments as a unit, and hence refers to data blocks that are made up of a number of characters.

To recover a synchronous data transmission, both of the modems must first be synchronized with respect to the occurrence and duration of each transmission sample, as well as the digital data bits represented by that sample. This level of signal compatibility is typically within the jurisdiction of the modems. The second level of timing compatibility, which is the responsibility of the digital data terminal devices, addresses the proper recovery of the individual data bytes or characters in addition to the value of the separate bits comprising those bytes. A compatible and synchronized exchange of digital bit streams and timing clock signals must be maintained between the modem and data terminal. If these areas of required timing compatibility are all achieved, data reception will be free of timing related errors. Even with compatibility among all these timing factors, it is still possible to have data errors due to actual transmission signal permutations.

Synchronized recovery of the transmitted information sample must first be achieved and maintained. Most data sets or modems operating over 1800 bits/s are multilevel devices. At lower transmision rates, a unique

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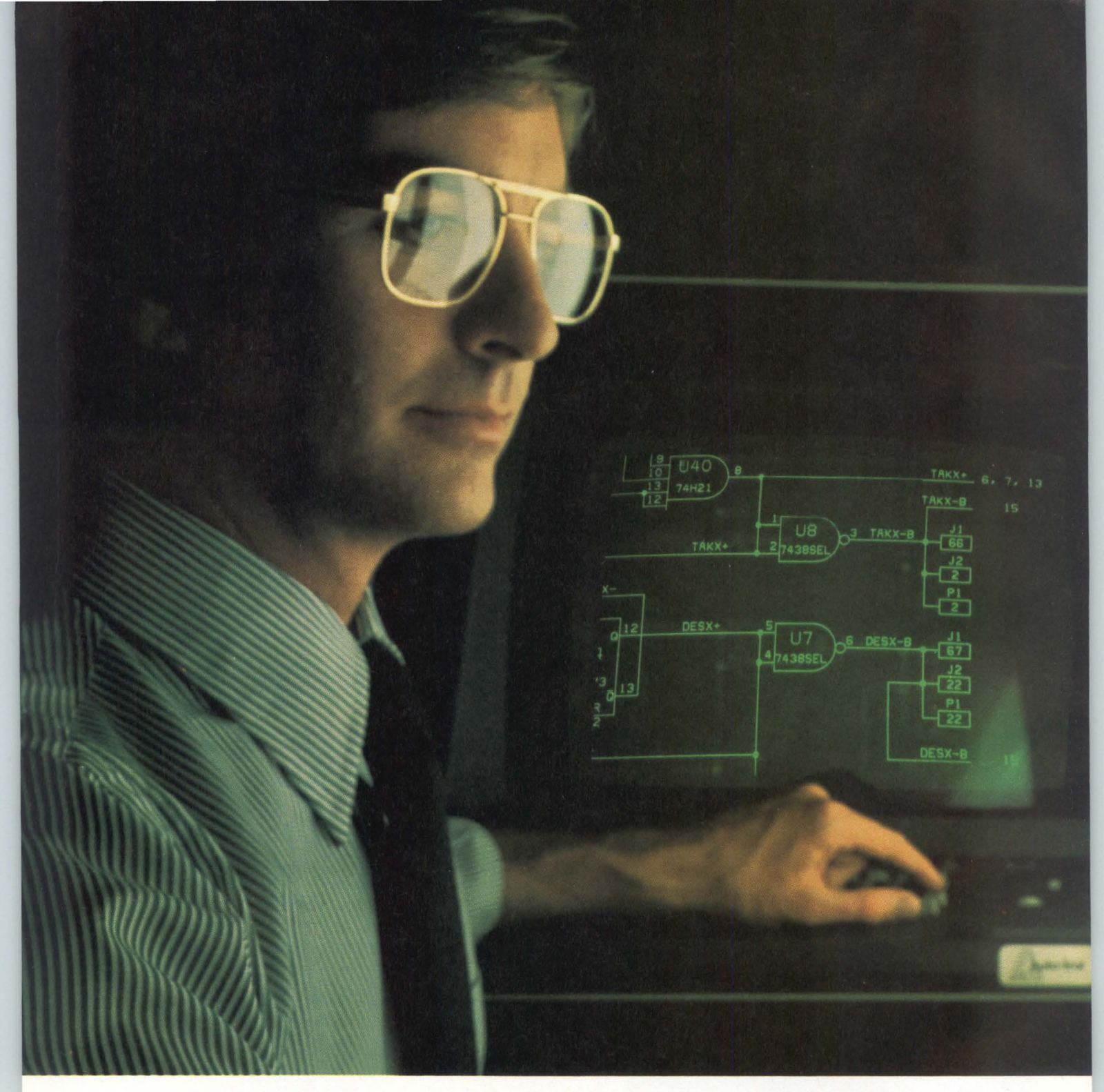

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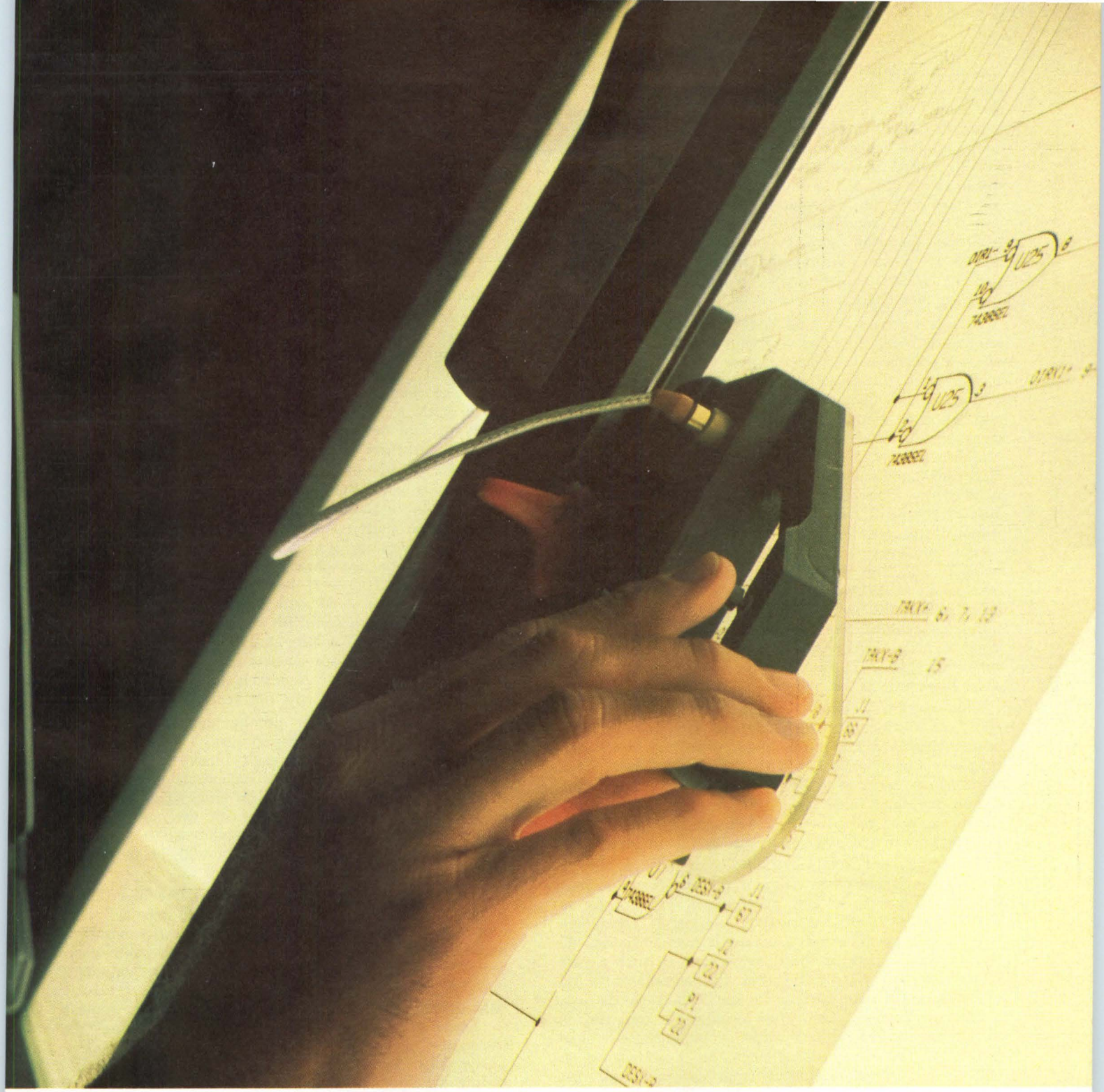

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CIRCLE 11 ON INQUIRY CARD

analog information sample or state is generated by the modulator for each digital state maintained on the Send Data lead of the EIA interface to the modem. With multilevel modems, this sample represents the actual digital values of two or more consecutive data bits presented in sequence to the Send Data lead of the modem's digital interface. With a dibit modem, one of four different information samples may be generated by the modulator to the transmission channel; tribit or quadrabit modems generate one of eight or one of 16 possible information samples. This data compression technique accounts for a lower baud rate (analog) being generated by a higher bit rate (digital).

Both the generating modulator and receiving demodulator must be coordinated with respect to the occurrence of each specific information sample. This can be accomplished with the initial transmission of a synchronizing pattern to the demodulator. While this pattern has no correlation to actual data content, it does contain sufficient signal transitions to permit the demodulator to establish a framing reference of the transmission sample. It is exchanged solely between the two modems, typically occurring between the activation of the modulator's Request to Send EIA lead and the Clear to Send lead response for controlled carrier modems. With continuous carrier modems, this procedure is performed automatically on the initial power on and channel connection state. Whenever there is a period of nondata transmission, this synchronizing procedure is again performed to insure that information sample synchronization is maintained. During actual data transmission, sufficient signal transitions occur to maintain the required synchronization.

This pattern's actual content and recovery parameters are distinct for each modem manufacturer. Use of modems of different manufacture on the same channel, a common practice with lower data rate transmissions, is not possible with higher data rates. While some exceptions may exist, the user is unknowingly risking a potential timing incompatibility. It is more prudent to use the same modems on the same channel.

The modulator establishes the framing synchronization of the transmission sample; the demodulator must detect and adjust to this synchronization in order to properly recover the information sample. If initial synchronization between two modems is being experienced, the problem usually is the demodulator. In such a case, it is important to confirm that the modulator is not generating an inconsistency in the timing of the synchronizing pattern. This jitter occurrence can also be introduced by the interconnection communications channel; thus the demodulator may be experiencing inconsistent framing references from successive information samples.

Once the synchronizing pattern is properly recovered and the demodulator has adjusted its internal timing to meet the timing of the remote modulator, the actual data transmission can occur. As each data information sample is recovered by the modem, the actual digital bit value sequence represented by that information sample can be reconstructed and sent to the associated digital device at the EIA interface. At the same time, a digital clocking signal that is in phase with the generation of the digital data bits is sent to the data device.

In more sophisticated modems, the digital clocking signal is generated by an independent digital timing source associated with the demodulator. Only the relative phase of this clocking signal is adjusted with respect to the generation sequence of the reconstructed digital data bits. Some less expensive synchronous modems do not utilize an independent timing source at the demodulator. In these modems, the clocking signal is derived directly by signal changes of the received information sample, making it possible to properly reconstruct the digital data bit sequence with respect to bit value and duration, and to generate a clocking signal which has jitter or is momentarily out of phase due to a permutation of the analog characteristics of the recovered information sample. The result is that the data device associated with the modem recovers an erroneous bit(s).

Beyond this point in the transmission, the responsibility for synchronization becomes associated primarily with the receiving data device rather than the modem. The information sample timing has been synchronized, the digital data bits have been reconstructed properly, and a clocking signal has been generated that is in phase with the digital data bits being sent to the receiving data device. The data device must now determine the structure of a data byte or character.

For correct identification of the beginning and ending bits of each data byte, a series of synchronizing characters or bytes must precede each transmitted unit or block. These patterns are distinct from those required by the modems. A synchronizing character contains a known bit sequence that has been prestored in the receiving data device. It receives each bit, adds it to the previously received data bits, and makes a comparison with the prestored bit sequence. If the comparison is valid, the following number bits that are known to comprise a byte are accepted, and the comparison is performed again. If a match is found, byte synchronization is declared by the receiving data device.

Byte synchronization is usually dependent on two successive valid byte comparisons. The transmitting data device must precede each block or transmitted unit with a minimum of three synchronizing characters. It is recommended that more than three such characters be transmitted in actual practice. In this manner data bit errors or occasional recovery latency at the demodulator can be overcome automatically without the actual occurrence of a data block error.

Once the byte synchronization status is achieved, the receiving data device merely counts the received data bits and determines a byte each time the established number of bits/byte has been reached. Synchronously timed data transmission has an inherent requirement: the data content must somehow instruct the receiving data device that the block has ended, reverting it back to search for byte synchronization. Terminating the transmitted data block with an End character accomplishes this. The End character is similar to the preceding synchronizing characters in that it is of a fixed and known bit pattern. The receiving data device begins to search for the End character with each successive character once byte synchronization has been achieved. When the End character is detected, the receiving data device reverts to searching for the next synchronizing character.

Every data communications system utilizes data error correction schemes. From the simple parity detection method to polynominal self-correcting codes, these procedures are intended to protect against transmission-induced data errors. Unless timing compatibility is achieved and maintained, these traditional error protection procedures are ineffective. Timing compatibility is realized during the initial application design and implementation periods—not after the network has begun its attempted data transmissions.

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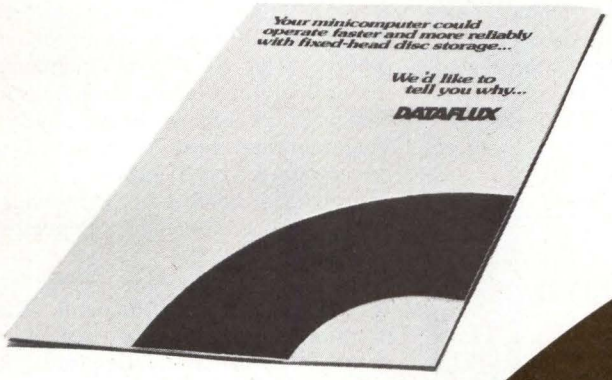

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Network Processing Systems Provide Support For SNA/SDLC Users With 3790 Emulation

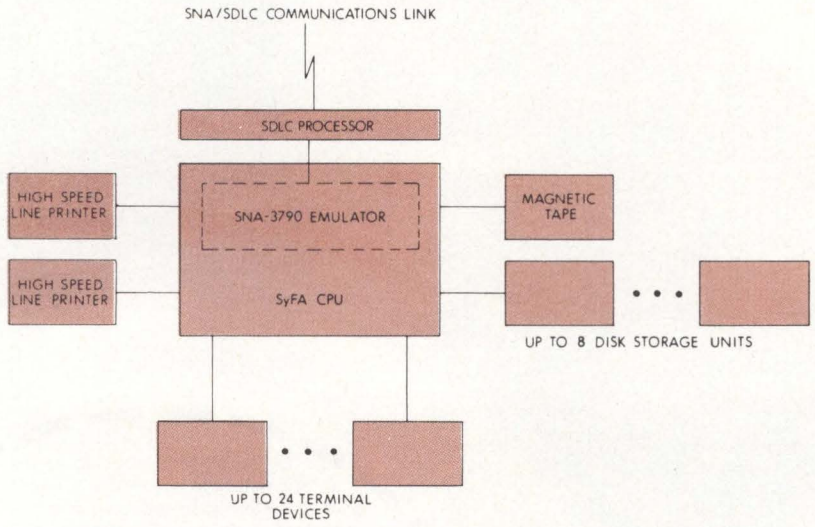
To meet the increasing user demand for batch and interactive mainframe communications on the same synchronous communications line, Computer Automation, Inc, 18651 Von Karman, Irvine, CA 92713 will offer its SyFA network processing systems with full Systems Network Architecture (SNA) compatibility, including an IBM 3790 communications controller emulation package using synchronous data link control (SDLC) line protocol. Expected to be delivered by the third quarter of this year, the emulation package enables a SyFA system to appear to an IBM mainframe as a 3790 communications controller, while offering additional features of powerful local processing and mass storage capability.

A programmable controller containing a microprocessor is used to implement SDLC. SNA/SDLC overhead functions from the system's CPU are offloaded to the microprocessor, which has its own 16k dedicated RAM. The system thus has inherent flexibility to adapt to future changes by IBM in network protocol details.

The 3790 communications capability will support proper error recovery and all SNA commands with proper responses and handshaking. SDLC protocol including bit stuffing, CRC checking, and message framing will be fully supported. Transmission speeds will be up to 9600 baud, full-duplex operation.

These capabilities are provided by the SDLC processor operating with an SNA-3790 software emulator executing in the system CPU's main memory. The facility allows SyFA systems to communicate in a multidrop configuration with the mainframe system.

SNA communications are initiated or received via any of 24 terminals running applications on the system. Application programs, written in high level SyFA Business-Oriented Language (SYBOL), may be developed on local systems, or centrally developed and down-line loaded to all distributed systems.



Combined software/microprocessor approach of SNA-3790 emulation package for SyFA network processing systems allows Computer Automation to emulate future IBM SNA products by writing additional software emulators to operate in conjunction with SDLC processor

The system currently supports IBM 2780 and 3780 RJE and interactive 3270 terminal emulation; under development are an IBM 360/20 HASP workstation emulator and ICL 7020 emulator. All emulators operate under the SYCLOPS operating system.

Circle 170 on Inquiry Card

Study Recommends Optical Fibers for Navy Communications

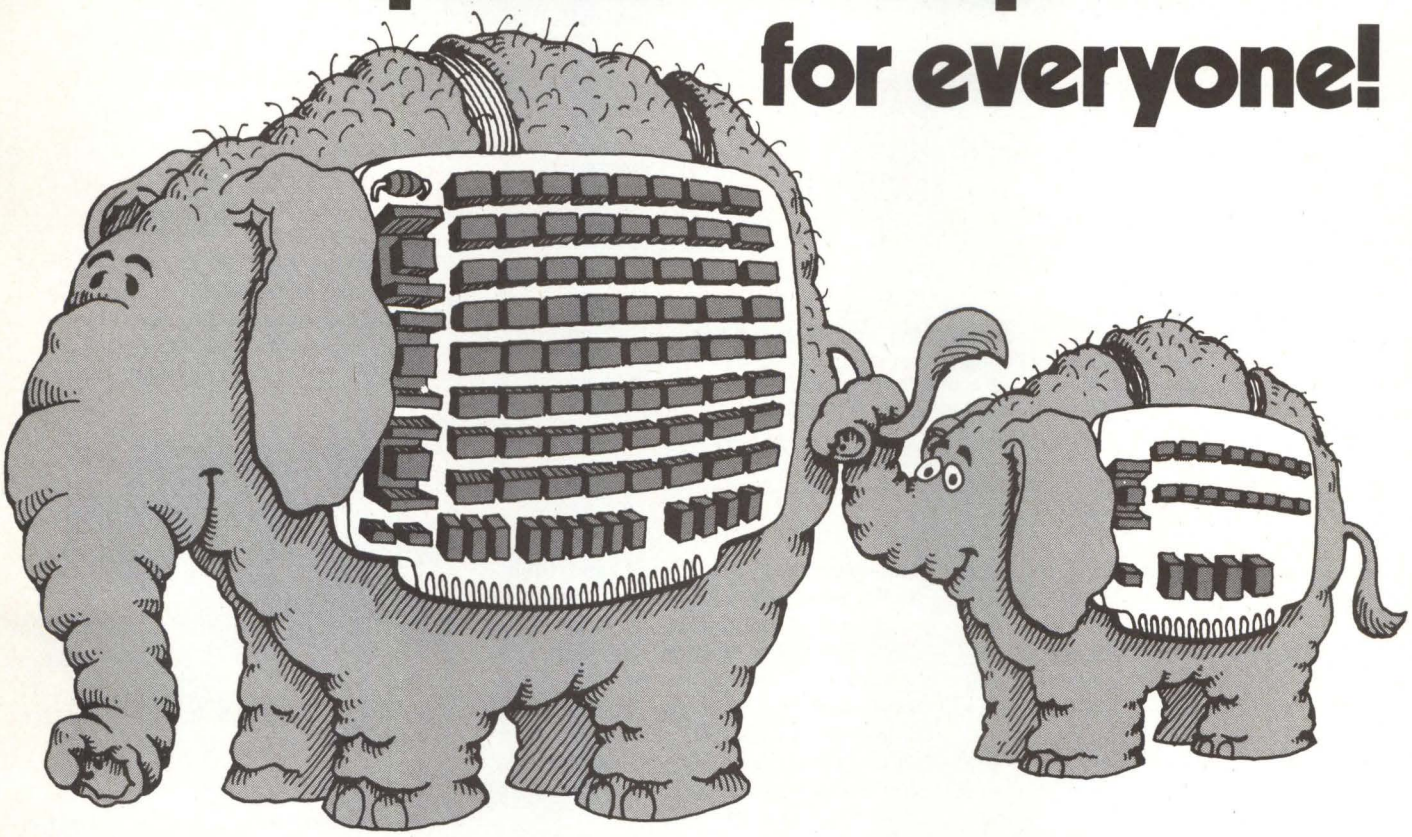
A recently-completed 10-month study has recommended the use of optical fibers as a means of upgrading U.S. Navy Shore communications, according to GTE Sylvania, Inc, General Telephone and Electronics Corp, One Stamford Forum, Stamford, CT 06904. The fibers are immune to natural and man-made electrical interference, are highly reliable, easy to maintain, and most secure. Other major military considerations are large bandwidth, small size, light weight, and tolerance to high temperatures and vibrations.

Undertaking the study for the Navy Electronic Systems Command, Washington, DC 20360, the company investigated several existing radio and cable links for replacement by optical fibers. Among initial recommendations was a cable that carries computer information between key terminals in Hawaii, as well as microwave links at facilities in that state. The study also suggests ways to continue communications after partial loss or disruption to the systems, to increase speed in processing telephone calls, and to make further use of available frequencies while reducing manpower requirements.

Unit Connects Four Polled Terminals to Single Synchronous Modem

Model 500 modem sharing unit allows four terminals to be connected to and share a single modem EIA RS-232 digital input. Unit op-

Now, Artec has an expandable elephant for everyone!



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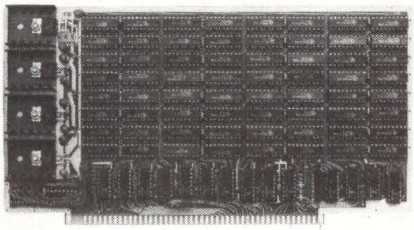

Kit: Board &
8K of memory—$285.00
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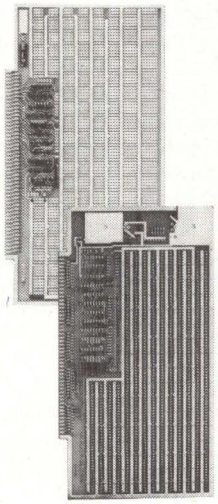
Maximum design versatility along with standard address decoding and buffering for S100 systems. Room for 32 uncommitted 16 pin IC's, 5 bus buffer & decoding chips, 1 DIP address select switch, a 5 volt regulator and more. High quality FR4 epoxy. All holes plated through. Reflowed solder circuitry.



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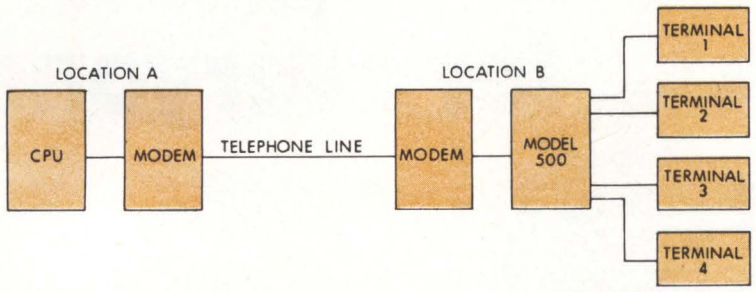


In application of Avanti's modem sharing unit, distance between A and B can be coast to coast, building to building, or city to city; CPU at A polls terminals at B. Modems are any long haul types. Model 500 is up to 50 ft (15 m) max from terminals, or 1000 ft (305 m) max when equipped with optional drivers

erates as a regenerative repeater mode for typical multidrop polled terminal environment. All connected terminals have continuous and simultaneous access to the modem being shared, with terminals located up to 50 ft (15 m) away.

Throughput is increased since the carrier is always established and presented to all terminals simultaneously. The unit is completely transparent to data format, and functions with any synchronous modem.

Avanti Communications Corp, Box 205, Broadway Station, Newport, RI 02840 has allowed for future expansion since the units can be branched together. Model 501 (internal) and 502 (standalone) driver options allow terminals to be located 1000 ft (305 m) from the unit.

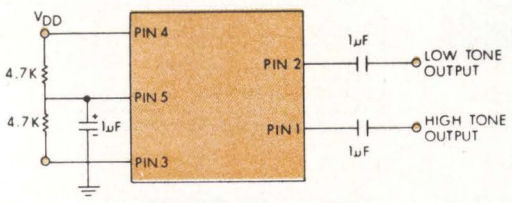
Circle 171 on Inquiry Card

Tone Separation Filter Supplies High and Low Frequency Outputs

The model 6300-001 tone separation filter features a low power hybrid IC design consisting of three independent operational amplifier stages that separate composite low and high frequencies into two independent high and low group tone outputs. Contained in a 6-pin, hermetically-sealed package, the device has been developed by Data Signal Corp, 40-44 Hunt St, Watertown, MA 02172 for systems requiring an interface with communication systems using Touch-Tone® decoders, as well as for mobile communications, transceiver applications, and modem interfaces.

Dual or single power supply operation is possible. Input impedance is 20 kΩ typical, input voltage range is ±12 Vdc, and gain is ±0.25 dB at 941 Hz (for low group output) and ±0.25 dB at 2909 Hz (for high group output). Additional specifications are power dissipation of 60 mW at ±12 Vdc, and separation between bands of 30 dB.

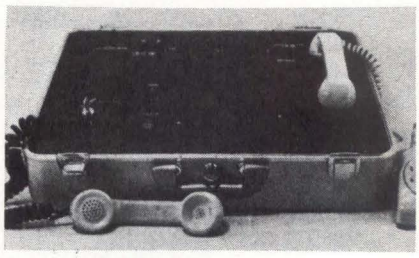
Circle 172 on Inquiry Card



If single-ended power supply operation is required with Data Signal's dual tone separation filter, V_{SS} input should be connected to ground; grounded input should then be connected to half voltage reference point. It is recommended that 1-μF ceramic capacitor be connected in series with each tone output

Portable Security Device Permits Telephone Conversation Privacy

The portable XL-280 TA acoustically coupled communications security device for use with telephones provides a high level of security with 18G nonlinear code combinations and a



code depth of 1165 h. The unit is completely self-contained in a carrying case and has both NiCd batteries and an ac power supply.

Technical Communications Corp, 56 Winthrop St, PO Box 1070, Concord, MA 01742 has utilized a wide deviation frequency displacement scrambling technique that cannot be decoded by conventional methods; the encryption process takes place in both time and frequency domains and is controlled by digital codes. Features such as antitamper lockout, dual synchronization, and excellent recovered voice quality are incorporated.

Circle 173 on Inquiry Card

Report Concludes International Satellite Communication Experiment

Comprehensive final and summary reports on the recently-completed international experiment in high speed computer communications via satellite have been submitted by Communications Satellite Corp (COMSAT), 950 L'Enfant Plaza, SW, Washington, DC 20024 to the Federal Communications Commission. COMSAT Laboratories, IBM Corp, the French Ministry of Posts and Telecommunications (PTT), and Symphonie, the

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TELEX: 348467 STANTECH SUVL
14, Avenue Industrielle—1227 Carouge, P.O. Box 52, 1211 Geneva 24, Switzerland. Telephone is 937-724 (Area 022), Telex 289160.

I²S
IMAGE PROCESSING SYSTEMS

CIRCLE 14 ON INQUIRY CARD

What engineering about using micro

Microcomputers are changing the competitive picture in hundreds of industries, in thousands of applications.

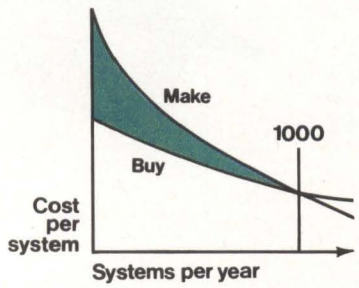
Designers are using microcomputers to create new products, even new markets. Microcomputers are breathing new life into existing products and providing competitive advantages in both price and performance.

For management, there's an added challenge. What's the most *profitable* way to take advantage of the microcomputer revolution? Should you start from scratch, dedicating time and resources to component-level design? Or should you take advantage of fully assembled and tested "computers-on-a-board"?

You didn't have a choice until just two years ago. That's when we introduced the first single board computer. Like "super components," single board computers have made it easy to add intelligence to any system.

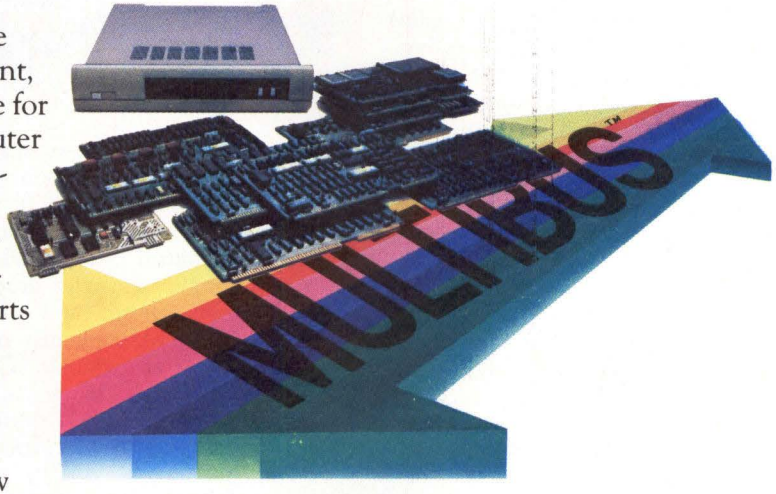
Sheer economics is one reason why. Up to 1,000 systems a year, you're money ahead with single board computers. That's based on a tradeoff formula that carefully considers amortized development and testing expenses, as well as direct material and labor costs.

Then, when production volume makes it more economical for you to switch to components, we'll provide all you need to do the job yourself—manufacturing drawings, pc artwork and a volume source for all the essential LSI components.

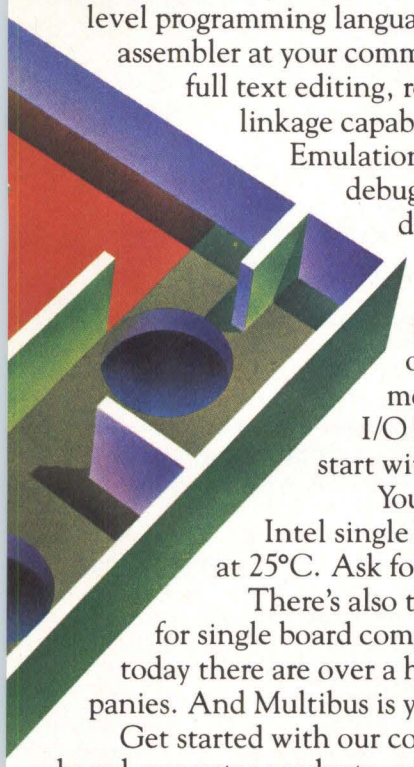


Time saved is another important reason single board computers make sense. You're into production sooner, without time spent developing the computer sub-system. Your engineers can go directly to the design of application-dependent hardware.

managers should know computers profitably.



RMX-80™ Real-time Multitasking Executive gives you a head start in software development, without the need to reinvent system software for every application. Intellec,® our microcomputer development system, speeds application software development. It puts PL/M and FORTRAN-80 (ANS FORTRAN 77) high-level programming languages and a macro-assembler at your command. And supports full text editing, relocation and linkage capability. In-Circuit Emulation, with symbolic debugging, provides a diagnostic window into your prototype to speed and simplify system development.



Our growing selection of iSBC™ products gives you the flexibility to tailor a system to your specific application, without compromise. Choose one of our five single board computers, starting at $99.* There's a full selection of memory expansion boards, communication interface boards, digital and analog I/O boards, mass storage systems and a high speed math processor. Or you can start with one of our packaged System 80's.

You're assured of the highest reliability when you build your system around an Intel single board computer. For example, MTBF for our iSBC 80/10 is 91,739 hours at 25°C. Ask for your copy of our iSBC Reliability Report.

There's also the security of Multibus,™ the multi-processing bus architecture we developed for single board computers. Multibus has become such a widely accepted industry standard that today there are over a hundred Multibus-compatible products available from 42 independent companies. And Multibus is your guarantee of compatibility with future Intel iSBC products.

Get started with our comprehensive iSBC System Configuration Kit. It's a catalog of Intel single board computer products, with detailed configuration instructions and worksheets to help you define the optimum iSBC solution for your needs.

For your kit, or for on-site assistance in configuring and pricing your iSBC system, contact your Intel representative or distributor. Or write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051. Telephone: (408) 987-8080. In Europe contact: Intel International, Rue du Moulin a Pàpier, 51-Boite 1, B-1160, Brussels, Belgium. Telex 24814. In Japan contact: Intel Japan, K.K., Flower Hill-Shinmachi East Bldg. 1-23-9, Shinmachi, Setagaya-ku, Tokyo 154. Telex 781-28426.

intel® delivers.

*iSBC 80/04, domestic U.S. price, 100 quantity.

Circle 15 for iSBC Configuration Planning Kit.
Circle 16 for pricing and configuration assistance.

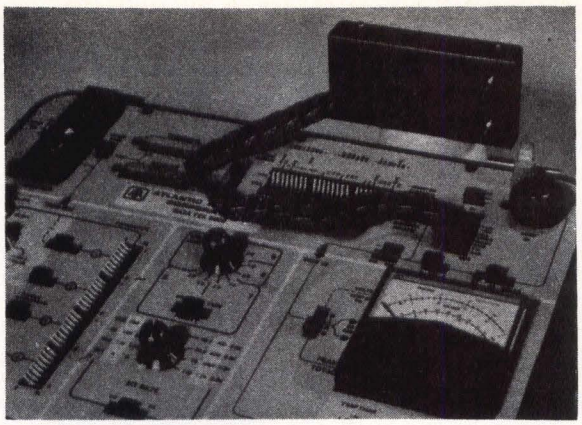
French/German communications satellite program, jointly conducted the study.

The experimental program involved transmission of data at 1.544M bits/s between an IBM 370/158 computer in LaGaude, France and a similar computer in Gaithersburg, Md, using 15-ft (4.6-m) antennas and the Symphonie satellite. Copies of the reports may be obtained by sending a $10 check (payable to "Communications Satellite Corporation") to Laboratory Records, COMSAT Laboratories, PO Box 115, Clarksburg, MD 20734.

Plug-In Modules Expand Test Unit's Timing Capabilities

Expanding the usefulness of asynchronous Data Tech 9600™ test units into some applications in synchronous networks, two plug-in modules from Atlantic Research Corp, 5390 Cherokee Ave, Alexandria, VA 22314 permit measuring and generating of on/off times. Time measurement module (ATM-1-1) allows the test unit to measure on- or off-time to any RS-232/V.24 control lead, while measuring duration of carrier dropout on a full-duplex circuit and providing time delay measurements between any two interface signals. Common measurements are ready to send/clear to send (RTS/CTS) turnaround time, the reverse from carrier on to CTS/RTS, or signal quality training time on Bell 208/209 data sets.

Time generating module ATG-1-1 provides flexibility in inserting delays where needed in various applications.



Data Tech 9600 test unit is connected to Atlantic Research's plug-in time generator module that allows delays to be inserted as necessary for specific applications

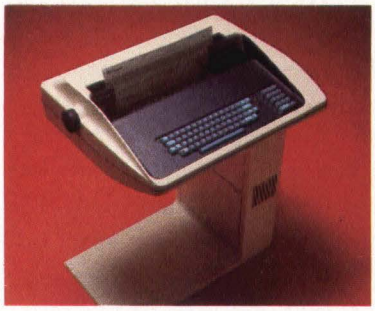
It allows the test unit to perform such tasks as full- or half-duplex automatic polling, with return message capability. A delay can also be inserted to allow a printhead to return before another message is sent.
Circle 174 on Inquiry Card

Third Generation and Mini Version of Exchange System Are Offered

PACX III, a third generation private automatic computer exchange system, features two enhancements. The first is that terminal users may use the terminal keyboard class select system to request a specific service class. The unit searches for a free port of the requested class—if it is found, the connection is made; if no service is available, the terminal is disconnected.

The second addition is a statistics port which replaces the standard control/monitor facility of models I and II. Connected to the CPU or other data handling device, the port accepts commands and generates statistical data at 2400 bits/s asynchronous, accompanied by time of day. Messages are in ASCII and use mixed radix port and terminal numbering system.

Gandalf Data, Inc, 1019 S Noel St, Wheeling, IL 60090 is also offering a miniature version of the system (MINI-PACX) for high speed asynchronous and synchronous operation up to 9600 and 19.2k bits/s, respectively. Easily reconfigured, the system handles up to 48 terminals and 32 computer ports of varying speeds and communications codes allowing terminal switching port selection and contention. Features provide use of dedicated lines which can be owned or rented with no business line charges, fast response to request for service, and availability of statistical data on usage of terminals and ports.
Circle 175 on Inquiry Card



Data General. A la Carte.

Now, you can order our DASHER™ terminals, even if you don't own a Data General computer system. Both our fast impact printer and our user-oriented video display are interface-compatible with any standard computer system.

60 or 30 cps versions of the DASHER printer, with a standard typewriter keyboard, u/l case, 132 columns.

DASHER display features a 1920 character screen, u/l case, detached keyboard, programmable function keys, and a monitor that tilts and swivels.

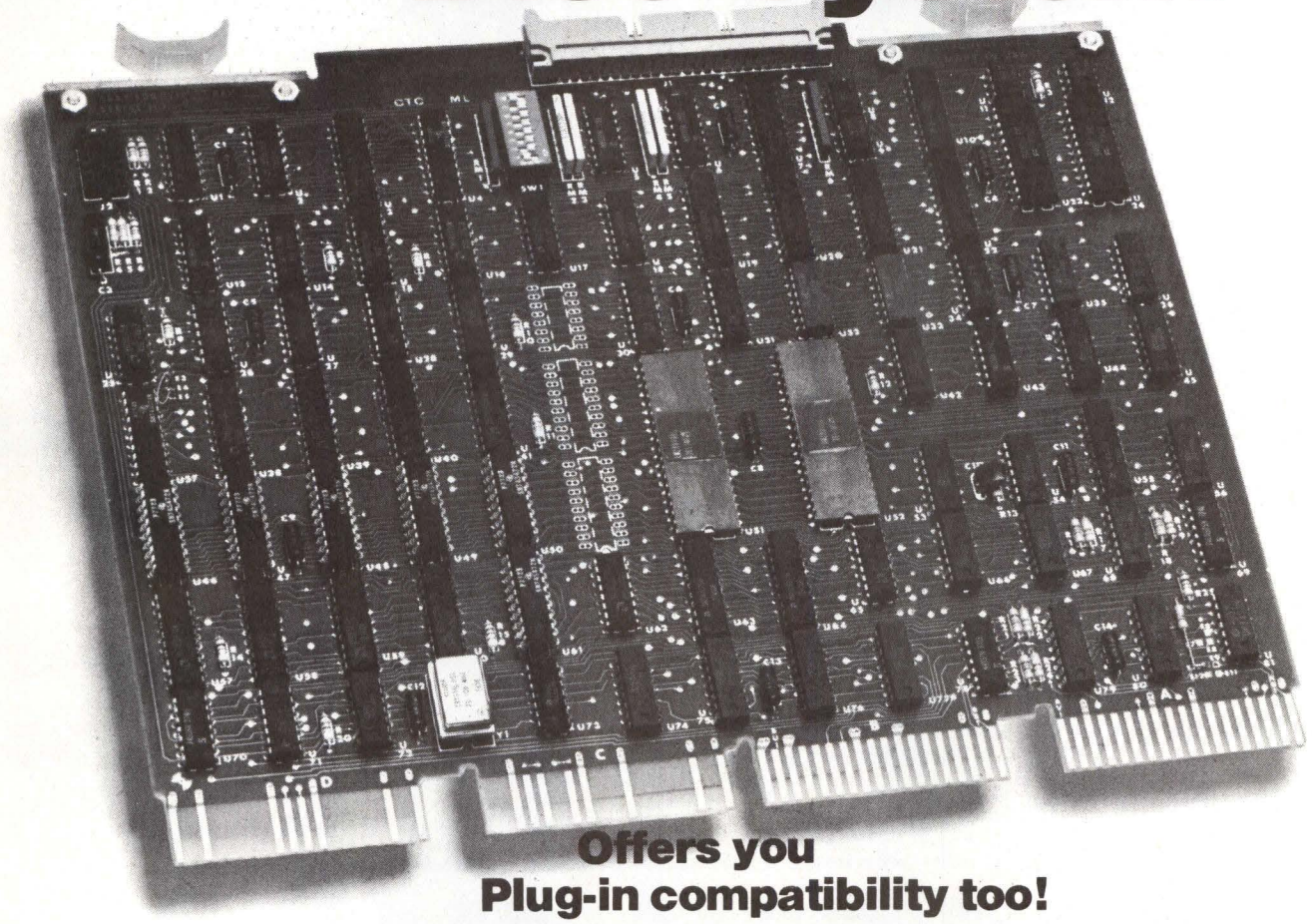
For more details call your Data General sales office or nearest independent supplier of Data General terminals. Or write. Even a bit of Data General in your computer system is better than none.

DASHER is a trademark of Data General Corporation
© Data General Corporation, 1977

Data General
It's smart business.

Data General, Westboro, MA 01581, (617) 366-8911. Data General (Canada) Ltd., Ontario.
Data General Europe, 15 Rue Le Sueur, Paris 75116, France. Data General Australia, Melbourne (03) 82-1361.

Controls your DEC LSI-11* Moving Head Disc System



Offers you Plug-in compatibility too!

Moving Head Disc Controllers are not new. But this one is . . . it's the Model DI-C03. What makes it new is its single quad size, made possible with a bipolar microprocessor and other exclusive Dynus circuitry. The module provides direct interface with your new or existing LSI-11. . . and it's transparent to DEC's RT-11* & RSX-11S* operating systems.

Capabilities offered by the Dynus Controller include control of up to 20 megabytes of online storage • compatibility with standard 2315 or 5540 cartridge drives • storage of 2.5 to 5.0 megabytes per cartridge • DMA transfer rate of 6.4 microseconds per word • an eight word FIFO buffer for DMA latency • and two additional address bits for 128K words of direct addressing for upward compatibility to future LSI-11s .

In addition to complete interface compatibility with the LSI-11, the DI-C03 mates with any industry standard 1500 to 2400 RPM disc drive having 100 or 200 TPI capability.

Write or call for complete details or a demonstration. Discover how easily you can control your DEC LSI-11 Moving Head Disc System.

3198 G Airport Loop Dr., Costa Mesa, CA 92626
Telephone: (714) 979-6811

*Trademark Digital Equipment Corp.

Dynus INCORPORATED

CIRCLE 18 ON INQUIRY CARD

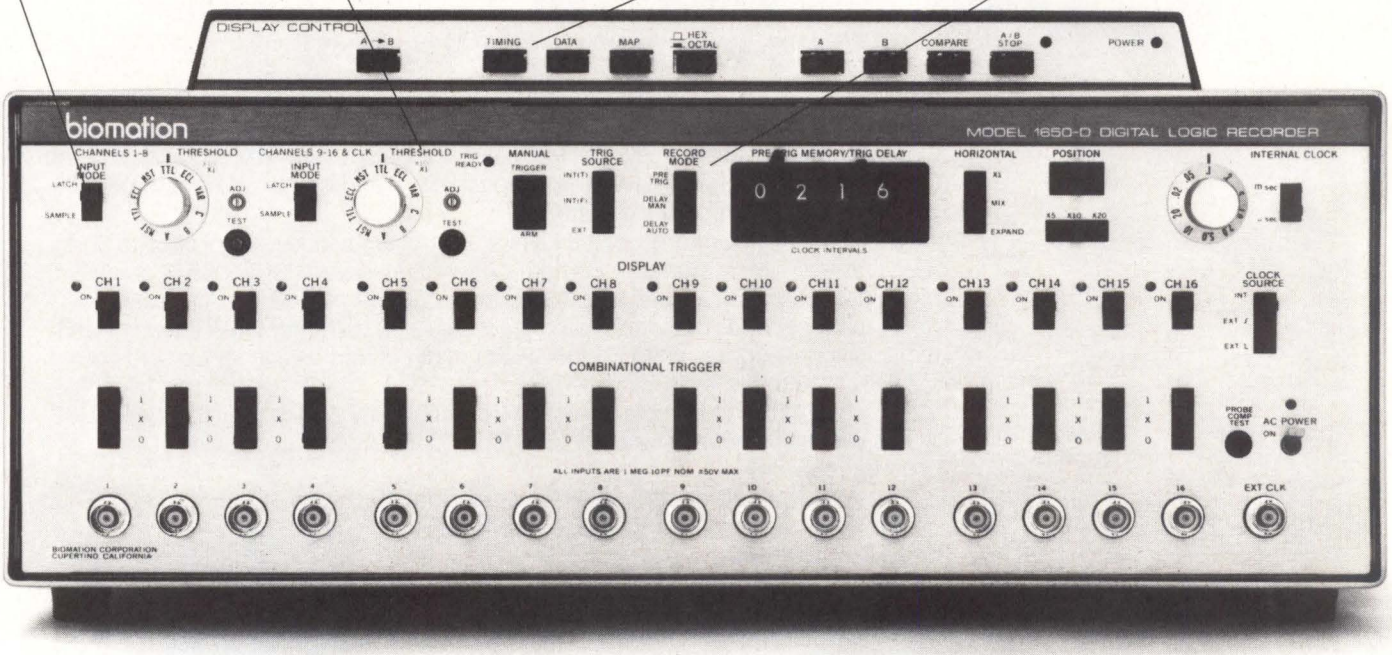
How 36 trigger points can simplify analysis of your microprocessor-based systems.

5ns Glitch Capture. Latch mode for glitch detection, or sample mode, can be independently selected for channels 1-8 and 9-16. Wide bandwidth BNC input allows capture of pulses as narrow as 5ns.

Mixed Logic Thresholds. Select one threshold voltage for channels 1-8, another for 9-16. Dial in ECL, TTL, MST, any of three user-preset values or continuously variable level.

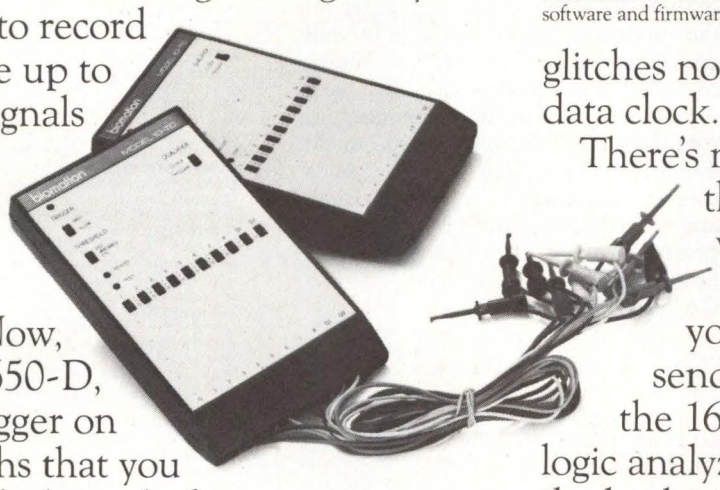
Display Control. Select timing diagram, data domain logic state display or map mode dot pattern of system operation, using the accessory 116 Display Control. Memory feature permits comparison of current and stored system characteristics.

Precise Memory Control. Pretrigger recording enables you to split the 512-word memory to capture data on both sides of the trigger event. Or, with Delay Mode, start of recording can be delayed as long as 9999 clock intervals after the trigger.

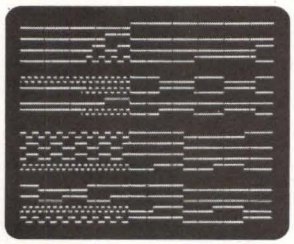


Designing a microprocessor-based system? There's no better way to get a precise, detailed look at both 8-bit and 16-bit microprocessor system operation than our 16-channel, 50 MHz logic analyzer.

Plug in two of our 10-TC active probe pods and the 1650-D's combinational trigger capability is expanded to trigger on words up to 36 bits long. That gives you the power to record and analyze up to 16 digital signals triggering from up to 20 additional locations. Now, with the 1650-D, you can trigger on word lengths that you just couldn't detect before.

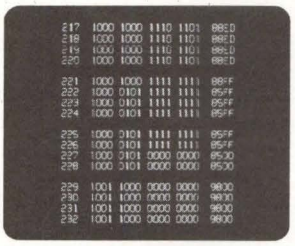


Versatility is the key to the 1650-D's popularity with designers working on microprocessor system development, instrumentation interfacing or analysis of real-time digital circuits. With the 116 Display Control, the 1650-D gives you the capability to analyze both timing and logic state displays. That's the key to simplified hardware/software debugging and integration.



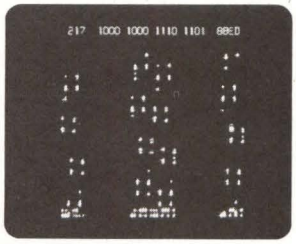
Time Domain. Timing diagram lets you see the sequential and simultaneous relationship between digital signals, to simplify hardware troubleshooting.

A Latch Mode on the input signal enables the 1650-D to detect and record glitches or pulses as narrow as 5ns — vital information when troubleshooting the operation of digital circuits. Or, for data analysis, Sample Mode ignores synchronous glitches not coincident with the data clock.



Data Domain. Display logic states (1's and 0's) with hex or octal translation. That's essential information for troubleshooting software and firmware.

There's not space here to give you all the details on how our 1650-D, with 10-TC probe pods and 36-bit trigger, can simplify your task. But we'll gladly send you detailed information on the 1650-D and our entire line of logic analyzers, from the budget-priced 920-D to the ultra-fast, 200 MHz 8200. And, at your convenience, we'll arrange a demonstration of Biomation's logic analyzers in your lab, capturing and displaying the data you work with.



Map Mode. Each digital word can be translated into a singularly positioned dot in this graphic representation of recorded data. Especially useful for spotting illogical or illegal memory addresses.

Write, call or use the reader service card. Biomation, 4600 Old Ironsides Drive, Santa Clara, CA 95050. (408) 988-6800. TWX: 910-338-0226.

biomation

Digital Multiplexing Transmission System Suits Military Use

Better means of scrambling calls and other signals is available with the Delta modulation multiplex system DX 15-60, developed jointly by Siemens AG, Postfach 103, D-8000 München 1, Federal Republic of Germany and AEG Telefunken. It complies with EUROCOM recommendations and is suitable for mobile and stationary use in military communications networks.

Between 15 and 60 voice circuits in the frequency range of 300 to 3400 Hz can be transmitted over physical circuits or radio paths. The continuously variable slope delta modulation method of digitizing analog speech signals is used. In spite of the 32k-bit/s rate per voice channel, good intelligibility is guaranteed under poor transmission conditions.

In addition to the multiplexer, the system consists of a terminal circuit unit for connection of 2-wire subscribers, and a line connecting unit enabling the multiplex signal to be transmitted via cable links longer than 4 km. Shorter cable paths use a simplified line section incorporated in the multiplexer.

Circle 176 on Inquiry Card

Communications Growth and Achievements Are To Continue Through 1980's

Launching of a "super satellite" in the mid to late 1980's, capable of direct communications with portable handheld telephones, and the introduction of a nationwide packet switching all-Bell system network (probably by 1979) are developments predicted by A. Terrence Easton, president of International Communications Management, Inc, 680 Beach St, Suite 428, San Francisco, CA 94109. This would drop the price of 1-min nationwide calls to 0.1 to 0.15¢, billed in 6-s increments.

Addressing the Bell Systems Services forum at the Interface West Conference, Easton said that development of AT&T network services—"mini-CCSA networks," nationwide automatic call queuing, usage-sensitive leased lines, and switched 56k-bit digital circuits—"will be the technological fallout of the super-satellite and computer based 4E toll exchange 'marriage.' " The communications revolution will have a great impact on business and the American society. Moving toward the 1980's, the four competing "super carriers" will be AT&T, ITT, IBM, and SPCC.

Network Interface Packages Are Offered for Additional Systems

Software packet network interfaces for Burroughs 6700 and 7700 systems and Univac 1100 series systems are available from Telenet Communications Corp, 1050 17th St, NW, Washington, DC 20036 under a licensing arrangement. Many simultaneous virtual connections can be handled over a single full-duplex access channel connecting the computer to the network. Features include full error control and statistical multiplexing. The Burroughs interface supports asynchronous terminals and uses the CCITT X.25 packet protocol; the Univac interface operates as a user program at the real-time level, and uses the company's host interface protocol to handle asynchronous terminals.

Circle 177 on Inquiry Card

Distributed Processing Expansion Adds 3270 Compatibility

Providing remote job entry and clustered 3270-type interaction with a host data base, the 1670 distributed processing system with 3270 compatible display terminal performs a mix of local functions ranging from interactive data entry to batch COBOL applications. Hardware includes up to 98,304 bytes of 750-ns main memory, up to 96M bytes of disc storage, and use of up to 28 CRT terminals in a single system.

Harris Corp's Data Communications Div, 11262 Indian Trail, PO Box 44076, Dallas, TX 75234 has designed the system to be fully hardware and software compatible with all 1600 remote batch terminals and distributed processing systems. Modem speeds for the switchable terminals are up to 9600 bits/s; non-switchable 1675 terminals can operate up to 4800 bits/s into the processor. □

Circle 178 on Inquiry Card

Call your nearest ISC sales representative

Alabama (also Mississippi):
W. A. Brown Inst. Inc.
Huntsville 205/883-8660
Arizona (also Nevada):
The Thorson Co.
Phoenix 602/956-5300
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The Thorson Co.
Los Angeles 213/476-1241
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Resource Data Sys.
Northbrook 312/564-5440
Kansas (also W. Missouri, Nebraska):
Inland Assoc.
Shawnee Mission 913/362-2366
Louisiana: W. A. Brown Inst. Inc.
Mandeville 504/626-9701
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Bartlett Assoc.
Bethesda 301/656-3061
Massachusetts (also Maine, N. Hampshire, Rhode Island, Vermont):
Bartlett Assoc.
Framingham 617/879-7530
Michigan: WKM Assoc.
Madison Heights 313/588-2300
Minnesota: Cost Reduction Services
Minneapolis 612/822-2119
Missouri (E.) (also S. Illinois, Iowa):
Inland Assoc.
St. Louis 314/821-3742
New Mexico: The Thorson Co.
Albuquerque 505/265-5655
New York (also Connecticut, New Jersey):
Bartlett Assoc.
White Plains 914/949-6476
North Carolina: W. A. Brown Inst. Inc.
Durham 919/682-2383
Ohio (also Kentucky): WKM Assoc.
Cleveland 216/267-0445
Dayton 513/434-7500
Oklahoma: Data Marketing Assoc.
Oklahoma City 405/528-6071
Pennsylvania (E.) (also Delaware):
Bartlett Assoc.
Wayne 215/688-7325
Pennsylvania (W.) (also West Virginia):
WKM Assoc.
Pittsburgh 412/892-2953
South Carolina: W. A. Brown Inst. Inc.
Columbia 803/798-3297
Tennessee: McCoin Elec. Equip. Co.
Knoxville 615/588-2417
Texas (also Arkansas):
Data Marketing Assoc.
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Los Angeles, CA 213/382-1107

ISC
Intelligent Systems Corp.®

Intecolor 8031
Unretouched photo of screen.

Two very sophisticated desk top computers with two very unsophisticated price tags.

We're Intelligent Systems Corporation and we've developed two brand-new stand-alone desk top systems. Both are capable of handling an incredibly diverse range of business, control, research and financial applications—in color. Both have a better price/performance ratio than any other compact computer system on the market.

Take a look at the Intecolor 8031. A compact 13-inch 8-color CRT, it comes complete with graphics hardware and software, a built-in mini disk drive for extra storage, plus "File Handling BASIC" which lets you create, delete, and retrieve program segments from storage, by name.

Now take a look at the Intecolor 8051. Perfect if your needs call for a large-screen format. It comes with the same standard features as the 8031, but it has a big 19-inch diagonal screen and external mini disk drive.

We also have a variety of options available for both units. including a convenient bi-directional desk top printer and a new 2708/2716 PROM programmer.

Contact the ISC representative nearest you for a working demonstration of these two highly sophisticated, versatile and dependable desk top systems. Prices are based on a one unit, cash-with-order basis. Guaranteed 30-day delivery or your money back.

ISC

Intelligent Systems Corp.®
5965 Peachtree Corners East
Norcross, Georgia 30071
Telephone 404-449-5961 TWX: 810-766-1581

Intecolor 8051
Unretouched photo of screen.

HEATHKIT

It took the LSI-11 microcomputer to put real processing power at a kit-builder's fingertips.

For years now, lots of people have wanted their own personal computers.

Well now they can have one.

The Heath Company of Benton Harbor, Michigan has just announced a powerful personal computer in kit form.

It's designed around the LSI-11—the most powerful, most software-supported microcomputer ever made.

For Harry Archer, Heath Design Engineer, anything less just wouldn't have been enough.

"We took a long hard look at every 16-bit computer, including minis. Nothing compared with the LSI-11. Either the price was too high, or the performance was too low.

"With the LSI-11 we can give hobbyists as much performance as they could ever use.

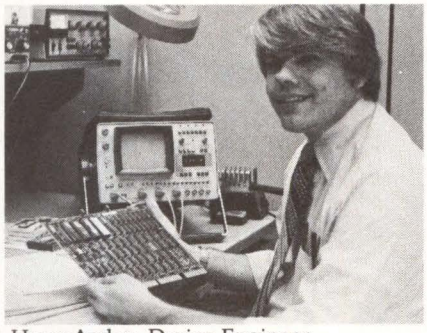
"And the LSI-11's low price allows us to offer a complete package for only $1295."

The basic kit includes a fully-wired and tested 16-bit LSI-11 CPU with 4K expandable RAM. Flexible I/O interface accessories. Complete system software package and high-level BASIC and FOCAL.

Since the instruction set is virtually the same as the PDP-11/34, the new Heathkit H11 is capable of generating highly sophisticated programs.

And because the LSI-11 is part of the PDP-11 family, the H11 can draw from a large array of peripherals and a huge library of applications software.

"The applications software and ease of programming really turned us on. In fact, it was the deciding factor," says Archer.



Harry Archer, Design Engineer at Heath Company, Benton Harbor, Mich.

"There are plenty of game-oriented programs available to the hobbyist. Now with our LSI-11-based kit, they've got some very sophisticated scientific and financial oriented software."

Although the new kit is aimed at the hobbyist market, the LSI-11's power, peripherals and software also make it ideal for education, small business and industrial applications.

When the Heath Company wanted to build the best computer kit available, they knew exactly what to do.

Build it around the LSI-11.

For 900 pages of solid technical information, plus our new brochure of microcomputer case histories, "Why Anything Less than the LSI-11 Wasn't Enough for Me," just call toll free 800-225-9220, (In Mass. 617-481-7400, ext. 5144), or write: Digital Equipment Corporation, One Iron Way, Marlborough, MA 01752.

digital
COMPONENTS
GROUP

CIRCLE 21 ON INQUIRY CARD

Multiuser Computer Systems Designed to Offer Enhanced Throughput and Response Characteristics

The ECLIPSE M/600 minicomputer is claimed to provide performance comparable to that of mid-range mainframes. To accomplish this, Data General Corp, Rt 9, Westboro, MA 01581 designed the system with advanced architectural features. Comprehensive I/O, demand paged memory management, and processing speed enhance throughput and response characteristics and fit the machine to multiuser environments.

Among the system's features are capacity for up to 1M-bytes of semiconductor memory, and a demand paging facility to optimize memory utilization in large online applications. A 3-level I/O management system (IOMS) includes an independent I/O processor with 64k bytes of local memory, a standard data channel, and a burst multiplexer channel (BMC) that allows a 10M-byte/s transfer rate. This feature provides hierarchical control for low, medium, and high speed peripherals. First level of IOMS, the BMS is a high speed direct communication pathway between main memory and high performance peripherals like fixed-head disc subsystems and 96- or 190M-byte disc storage subsystems. Data transfer rates on the BMC can attain the full main memory system bandwidth, resulting in a very fast aggregate rate—10M-bytes/s. Up to eight high speed controllers can connect to the BMC, resulting in a potential system expandability of up to 6G bytes.

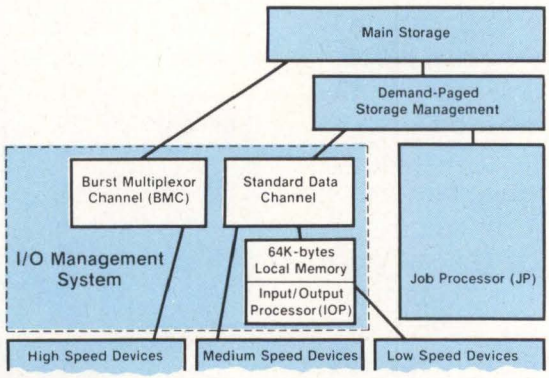
A standard data channel comprises the second level of the I/O control hierarchy. It handles communications between the system's job processor and medium speed peripheral equipment such as magnetic tape and cartridge disc drives. It also acts as a high speed—up to 2.5M bytes/s—interface between the job processor and the third-level I/O processor (IOP) for low speed peripheral devices.

The IOP is an independent processor with an Eclipse instruction set and 64k bytes of local memory. It processes and buffers data input from low speed peripherals such as display and printer terminals, card readers, and asynchronous communications devices. The IOP acts as a frontend processor for the M/600, off-loading the job processor by buffering all low speed input, checking it for errors, and sending it to the job processor one logical record at a time. It also receives all terminal output from the job processor and transmits the data back to as many as 64 terminals at the speeds they require. By absorbing the character-handling overhead in large multiterminal applications, the IOP frees up the job processor for high speed processing.

System processor is a job processor having a 200-ns microcycle and a microprogrammed architecture that incorporates the standard Eclipse instruction set along with extensions. Instructions include both 16-bit single word instructions for efficient memory utilization as well as 32-bit double word instructions for extended addressing range. Single word and block move instructions transfer large amounts of data. System instruction sets include four source data processing instructions for business and scientific applications.

Systems are available with MOS memory expandable to 1M byte in 64k-byte increments and core expandable to 512k bytes in 32k-byte increments. MOS has read and write cycles of 500 and 700 ns, respectively, while core has an 800-ns cycle time. All semiconductor memory has error checking and correction (ERCC) to maintain maximum data integrity.

A demand-paged memory management facility under control of the advanced operating system (AOS) executive optimizes multiple-user access to main memory by reducing individual requirements at any given time. This is done by automatically dividing each user's memory space into "pages," and keeping only active pages in main memory, while other pages are stored on fast access devices. Working with an AOS page-



Hardware composing Data General's ECLIPSE M/600 multiuser minicomputer is divided into three functional elements. Major sections—main storage with demand-paged memory management facility, 3-level I/O management system, and main processing unit—are organized to provide responsiveness and throughput that are comparable to those of medium-scale mainframes

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UNRETOUCHED

MICROPHOTOS

Your IC lead frames look like this at 30X enlargement (unretouched). Because they are punched out of metal, the edges are rough, jagged and irregular. In contrast, the flat sides of the lead frame are smooth, even and perfectly plated.

Arrows indicate scars and abrasions made by rough edge of lead frame.

22X magnification, unretouched.

THEIRS

An ordinary edge-bearing socket contact after 5 insertions of DIP lead frame. Contact has been spread apart to show inside faces of contact. Notice how the contact has scars and abrasions from *rough, irregular edge of IC lead frame.* Electrical contact is degraded and resistance is increased. Reliability is obviously reduced.

Lead frame in place in an ordinary edge-bearing contact.

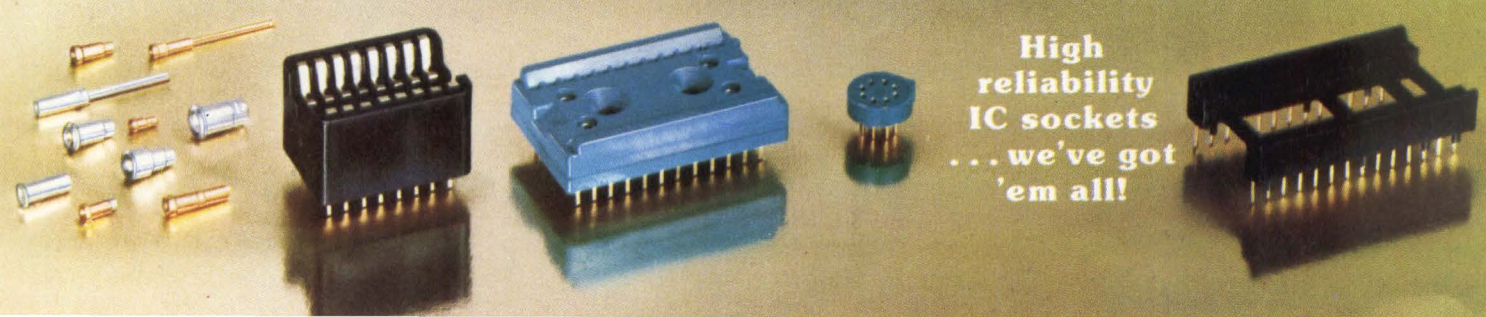
Arrows indicate contact surface still smooth, clean, free from abrasions.

22X magnification, unretouched.

OURS

ROBINSON-NUGENT "side-wipe" socket contact after 5 insertions of DIP lead frame. Contact has been spread apart to show inside faces of contact. See how the RN contact—because it mates with the *smooth, flat side of the IC lead frame*—retains its surface integrity. This 100% greater lead frame contact results in continued high reliability.

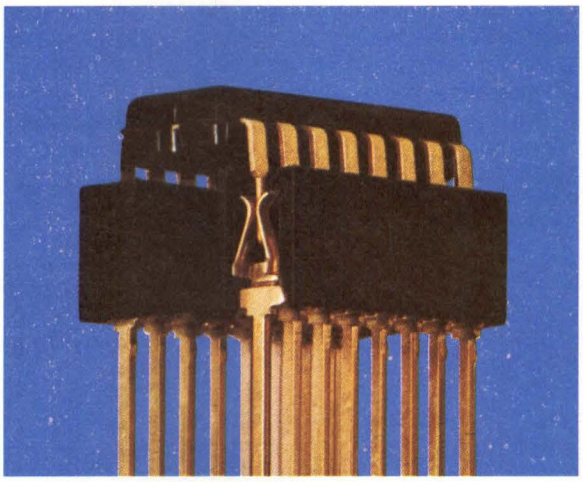
Lead frame in place in RN "side-wipe" contact.



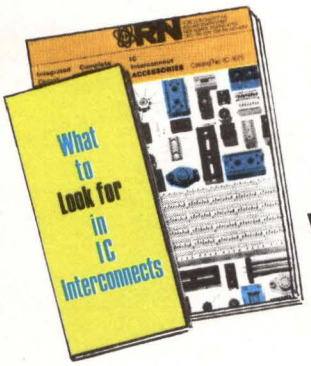
expose 'junk' socket problems

Secret of RN high reliability 'side-wipe' DIP sockets revealed by microphotos

Here's microscopic proof that high reliability Robinson-Nugent "side-wipe" DIP sockets make 100% greater contact than any edge-bearing socket on the market. This advance design provides constant low contact resistance, long term dependability—trouble-free IC interconnects. Yet RN high reliability DIP sockets cost no more than ordinary sockets!

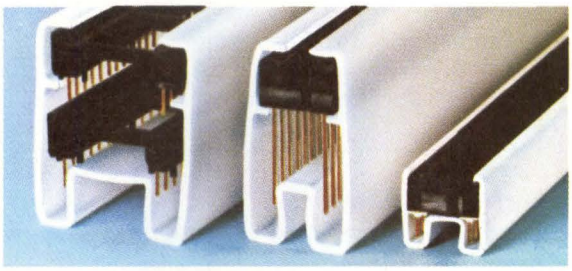


Get the high reliability that eliminates trouble. RN "side-wipe" DIP sockets make contact with the wide, flat sides of your IC leads. You get 100% greater surface contact for positive, trouble-free electrical connection.



WRITE TODAY

for catalog and informative book "What to Look for in IC Interconnects." Free from Robinson-Nugent—the people who make more kinds of high reliability IC sockets than anyone.



They're even packaged for high reliability. "Protecto-pak"® packaging delivers consistently perfect RN sockets to your production line—for automated or manual assembly.

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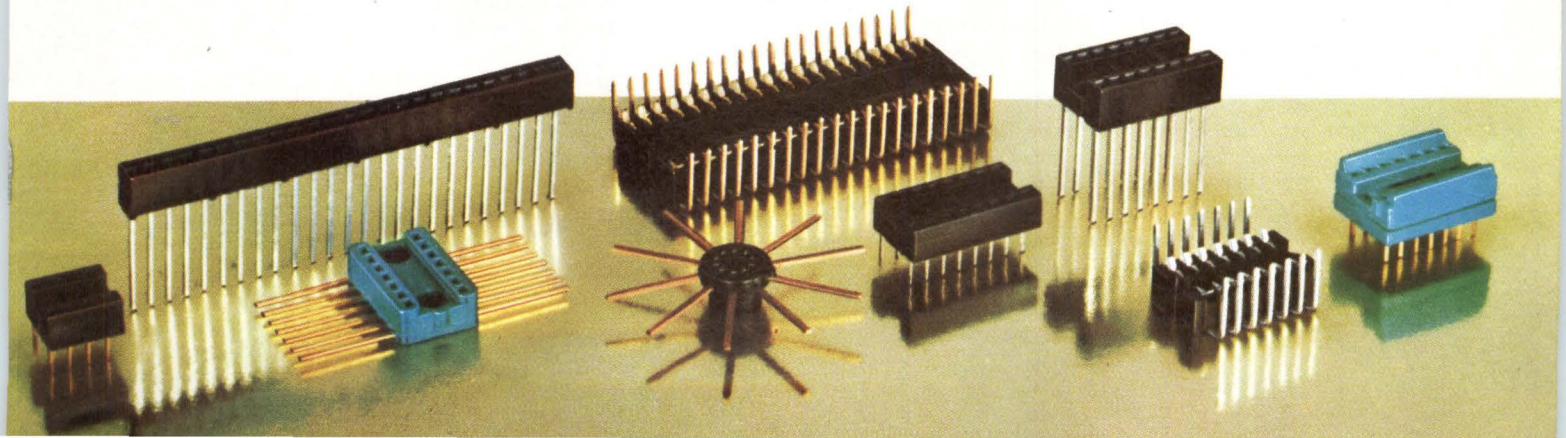


replacement algorithm in the executive, the memory management facility is a predictive tool transparent to system users. Software analyzes and predicts what pages will be needed at any given time by any user, and system hardware moves the pages into main memory. Hardware maintains information on page validity and page usage, as well as the type of information on these pages (procedures or data). The executive uses this information, together with user priority data and other resource requirements for each user to determine the best overall mix of users at any given time.

Support is provided for communication with other Data General computers and with IBM-compatible computers through RJE80 and HASP II workstation emulator software packages. In addition, up to 15 M/600s or other Nova or Eclipse systems may be interconnected by a multiprocessor communications adapter to distribute large processing loads.

To ensure system reliability, the design incorporates error control techniques throughout main memory, disc storage devices, IOP memory, block multiplexer channel, and main processor control store. Online diagnostic routines run continually under multiprogramming AOS, monitoring processor logic, memory, and peripherals.

Prices will range from about $160,000 to $395,000, with deliveries scheduled to begin in May. Representative configurations include a system with 320k-byte core storage, 96M-byte disc, 1600-bit/in (630/cm) magnetic tape, 60-char/s DASHER terminal printer, 300-line/min printer, eight asynchronous ports, 1200/2400-baud synchronous line interface, AOS, PL/1, FORTRAN IV, FORTRAN V, BASIC, and RJE80. A high end system would have 512k-byte MOS storage, four 190M-byte discs, two 2M-byte fixed-head discs, two 1600-bit/in (630/cm) magnetic tapes, 600-line/min printer, 600-char/min reader, 60-char/s terminal printer console, 32 asynchronous ports, and two high speed synchronous line interfaces.

Circle 140 on Inquiry Card

Computer Systems Fill Needs of Small and Medium Size Businesses

Two business computers, Visual I and Visual II are, respectively, an electronic accounting system and a minicomputer system powerful enough to handle up to four CRT terminals. Developed by Philips Business Systems' Data Systems Div, 175 Froehlich Farm Blvd, Woodbury, NY 11797, the systems are tailored to special requirements of small and medium size companies through fully integrated software and hardware.

Basic configuration of the Visual I includes CRT visual display for conversational interaction with the operator, both alphanumeric and numeric keyboards for fast input, and matrix printer for high throughput. Mass file storage is provided on flexible discs; and users have a choice of any two applications software packages with their system.

The more powerful Visual II, for use standalone or in a distributed processing network, consists basically of processor with 32k bytes of semiconductor main memory, 10M bytes of auxiliary storage on cartridge discs, CRT display, and matrix printer. This system can easily accommodate additional optional I/O devices such as CRT terminal and outboard printers; memory is expandable in 16k increments and auxiliary disc storage is available in 10M-byte modules.

Circle 141 on Inquiry Card

Portable Terminal Provides Voice Response and Hardcopy Output

Micro-VIP series units utilize a modular approach to provide terminal models which feature voice response only, voice plus a built-in 30-char/s printer, and voice plus print plus a plug-in keyboard. Packaged in a briefcase for portability, the intelligent terminals can output complete formatted reports and transmit data to a central computer.

Because they are designed for nontechnical personnel, the units are easy to use. Input data and specific questions for transmission to a computer are set up through a series of thumbwheel switches. Headings appear on plastic templates which fit over the number switches. Each program has its own template, which instructs the user in how to enter information necessary to the computer.

When the numbers have been set, the user simply places the handset of an ordinary telephone into the terminal's acoustic coupler, dials a number to connect with a central computer, and presses a button. After a few seconds, the host computer replies to the questions either verbally or by printing its reply.

The terminal contains a microprocessor that is used solely to control the printing function. This leaves approximately 3000 bytes of memory available to add standalone capability in the future. This could allow preprocessing of data before going online to the computer, which could include editing functions, control totals, and error correction routines.

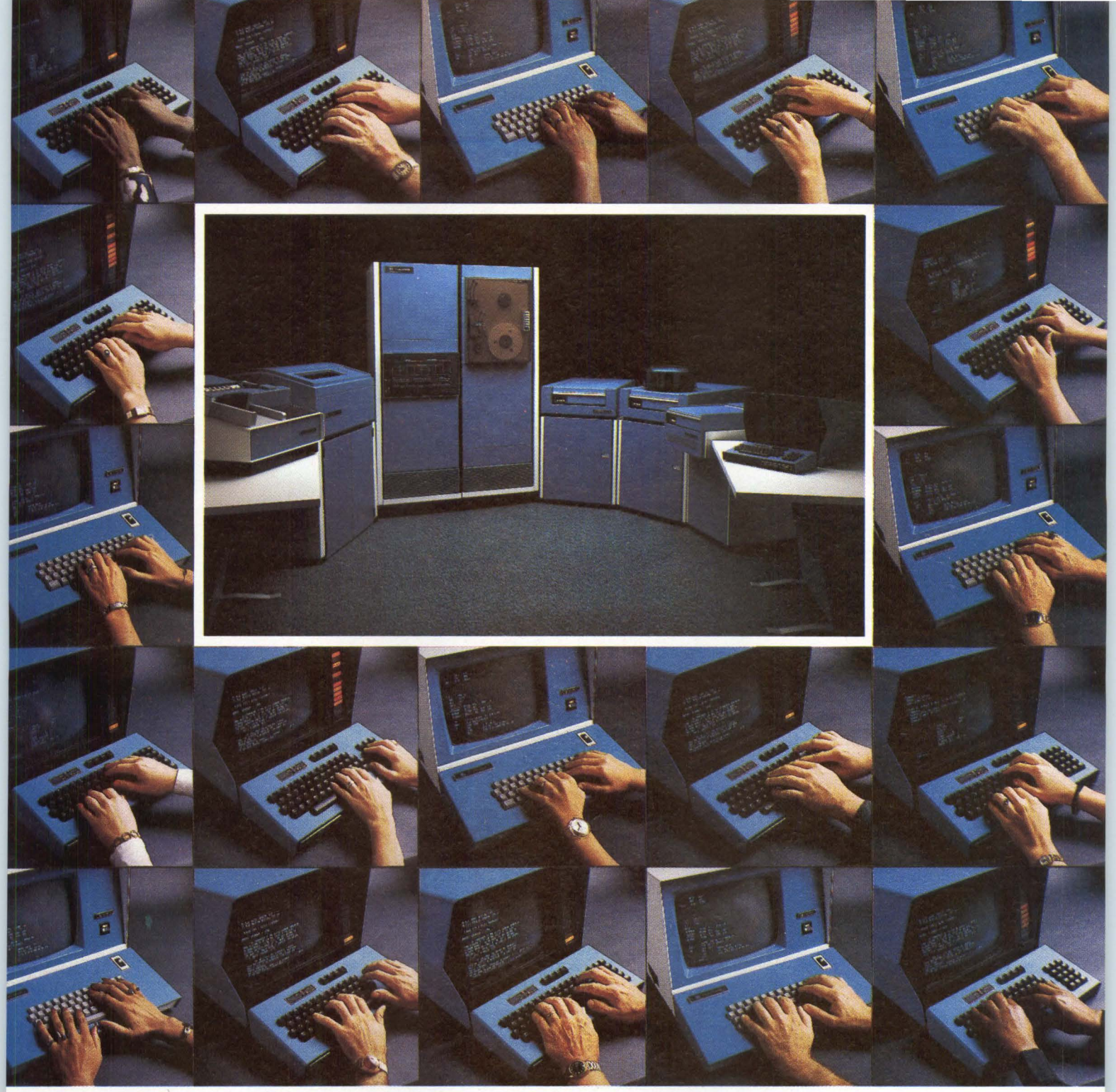
Designed specifically for life underwriters and financial planners by Computone Systems, Inc, 1 Dunwoody Pk, Atlanta, GA 30338, the terminal is supplied with forms, instruction manuals, and programs covering estate planning, income tax planning, retirement planning, and 30 other subjects relating to personal and business financial planning.

Circle 142 on Inquiry Card

Mass Termination System Increases Productivity of Discrete Wire Harnesses

A concept that permits discrete wires to be mass terminated with automatic harness-making machines, the mass termination system (MTS) can result in labor savings as great as 90%, while assuring a reliable system. Introduced by AMP Inc, Harrisburg, PA 17105, MTS is a complete wire-to-post interconnection system for 0.100 and 0.156" (0.254 and 0.396 cm) centerlines, including PC board headers.

Key feature of the system is the insulation displacement technique applied to the connector. Connectors are preloaded with dual-beam contacts, providing a simple, one-step operation for terminating unstripped wires into the connector. Insulated wire is simply positioned in the con-



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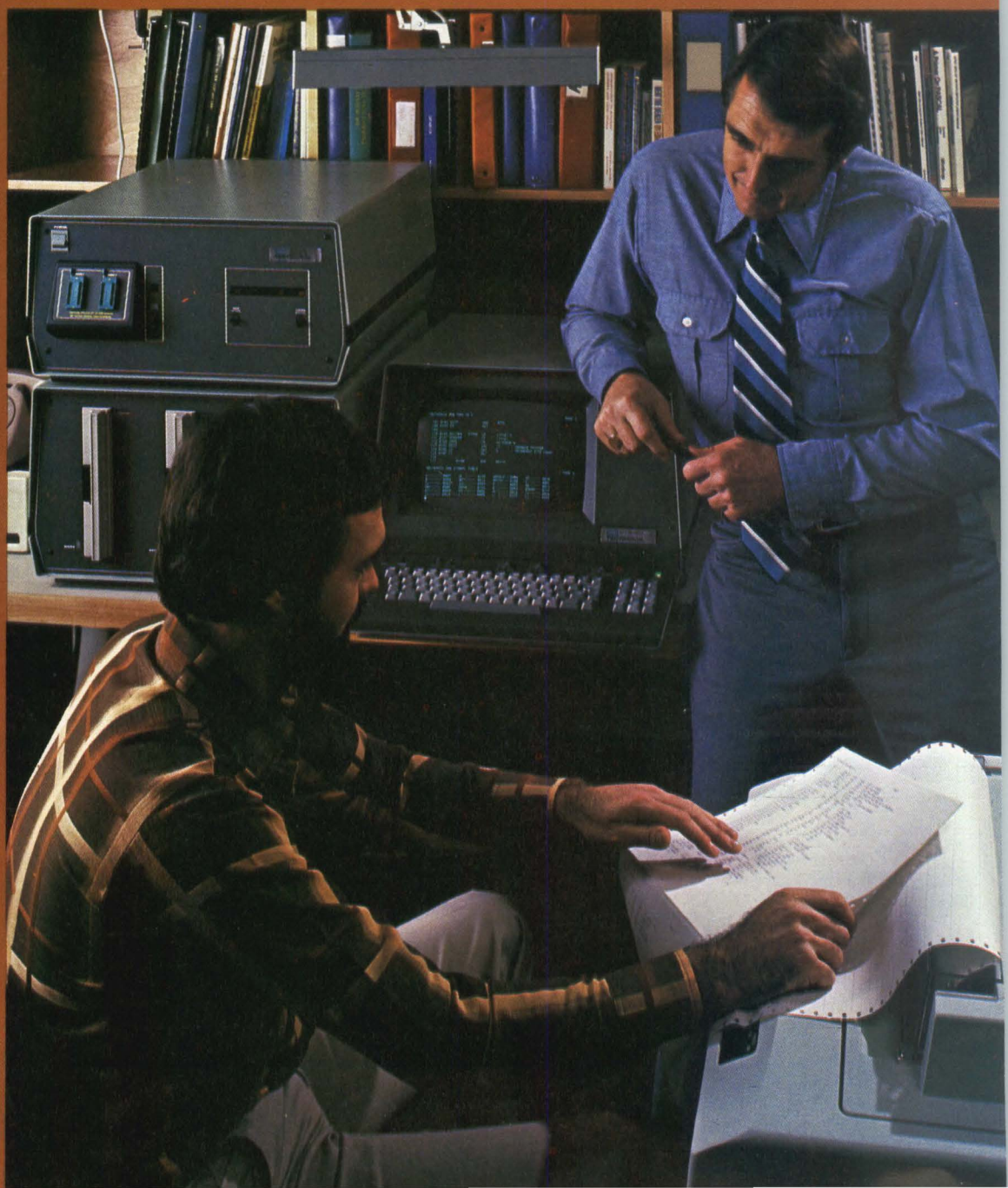

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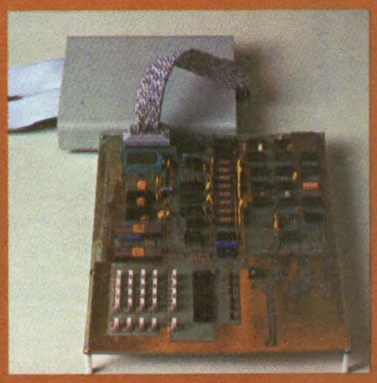
Prototype control probe runs prototype hardware and software under control of the microprocessor lab while you maintain access to program activity.



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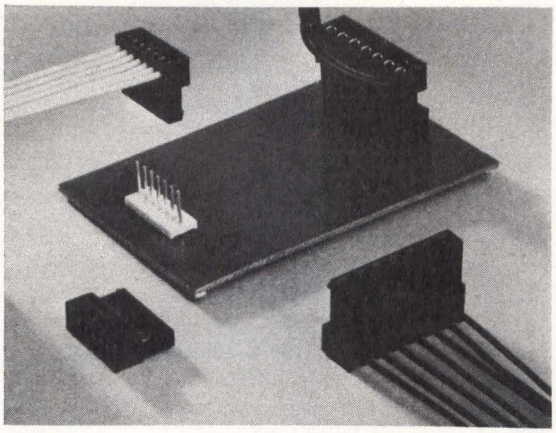
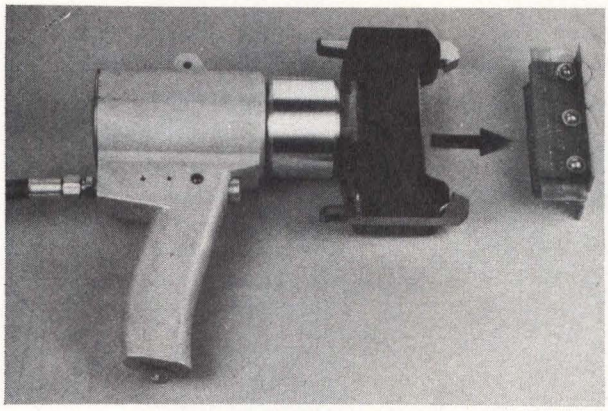


Components for wire-to-post interconnection on 0.100 to 0.156" centerlines allow mass termination of discrete, ribbon, or jacketed cable without wire stripping, using the slotted beam contact principle



Among the tools that AMP supplies for its Mass Termination System is an air-powered self-indexing hand tool that snaps onto a special comb mounted on the harness board to mass terminate discrete wire cabling directly on the harness board

tact slot area where the application tooling pushes the wire into the slot to the proper depth. Contacts have two wire slots for termination redundancy and secure wire retention.

When terminating, the slotted beam is deflected by the wire, and slot contact force displaces the insulation to make electrical contact at four areas of the wire. Wire diameter is compressed under beam spring load until equilibrium is reached. Residual or stored energy normal force against the wire provides contact reliability through wire creep conditions during heat age or thermal cycling.

Connector housings are color coded to a particular wire size and applicable for wire sizes 18 through 28. Housings are equipped with strain relief wires molded into each wire location to provide retention and pull-out protection. Housings are end-to-end stackable and compatible with flat, polarizing, and polarizing with friction lock headers in vertical and right angle configurations. Additional wire support plastic retainers are molded into the connector housing. Dual wipe contacts provide a normal force of 200 g and are post lubricated to prevent fretting corrosion.

Application tools for the system include a simple T-handled tool for maintenance or repair, a manually operated self-indexing tool for low volume work, and an airpowered version for intermediate volumes where portability is necessary. A semiautomatic machine can mass terminate both ends of up to 7000 wires/h and can produce single- or double-ended cable assemblies. In making cable and wire harness assemblies, the system can improve productivity by up to 75%. The pneumatic harness board tool is especially designed to lock onto combs or fixtures already mounted to the harness board and preloaded with connectors. The connector is mass terminated by simply squeezing the trigger.

Circle 143 on Inquiry Card

Magnetoresistive Effect Promises Application In Thin-Film Read Heads

Two elements of current technological development have influenced research into practical applications of the magnetoresistance effect: increasingly high information densities and need for greater sensitivity for detection of that information. Magnetic sensors must be constructed to a degree of compactness that may not be attainable with conventional magnetic induction types despite continuous refinement and miniaturization.

Magnetic induction heads are constructed of tiny coils wound around a ferrite yoke with extremely small gap dimensions. Philips Research Laboratories in Eindhoven, The Netherlands believes that development in such heads is now close to the limit imposed by properties and workability of the materials used. Therefore, personnel at that establishment have been conducting extensive investigations into the use of thin-film heads for both writing and reading data, particularly data recorded on magnetic tapes and bubble memories.

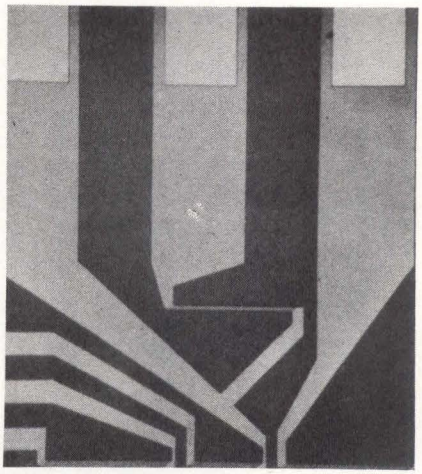


Fig 1 Photomicrograph of magnetoresistive head with "barber poles," invented at Philips Research Laboratories. Three such ferromagnetic read strips, provided with oblique gold bands, can be seen side by side on substrate. Fourth barber pole (somewhat higher, in middle of photo) does not react to variations in magnetic field, but serves for compensating interference signals detected by middle read strip. Light areas are conductors. Before use, underside of this construction is ground away up to just below three lead strips

(Continued on p 46)

One company can cut keyboard costs. Even when their keyboards cost more.

The most expensive mistake you'll ever make selecting a keyboard could be spending too little. In the long run, that adds up to cutting corners, not costs.

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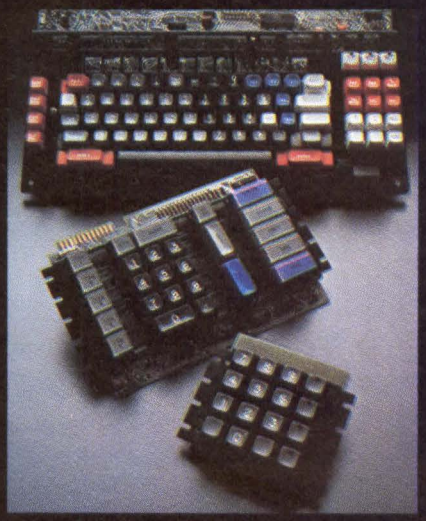

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CIRCLE 26 FOR DATA

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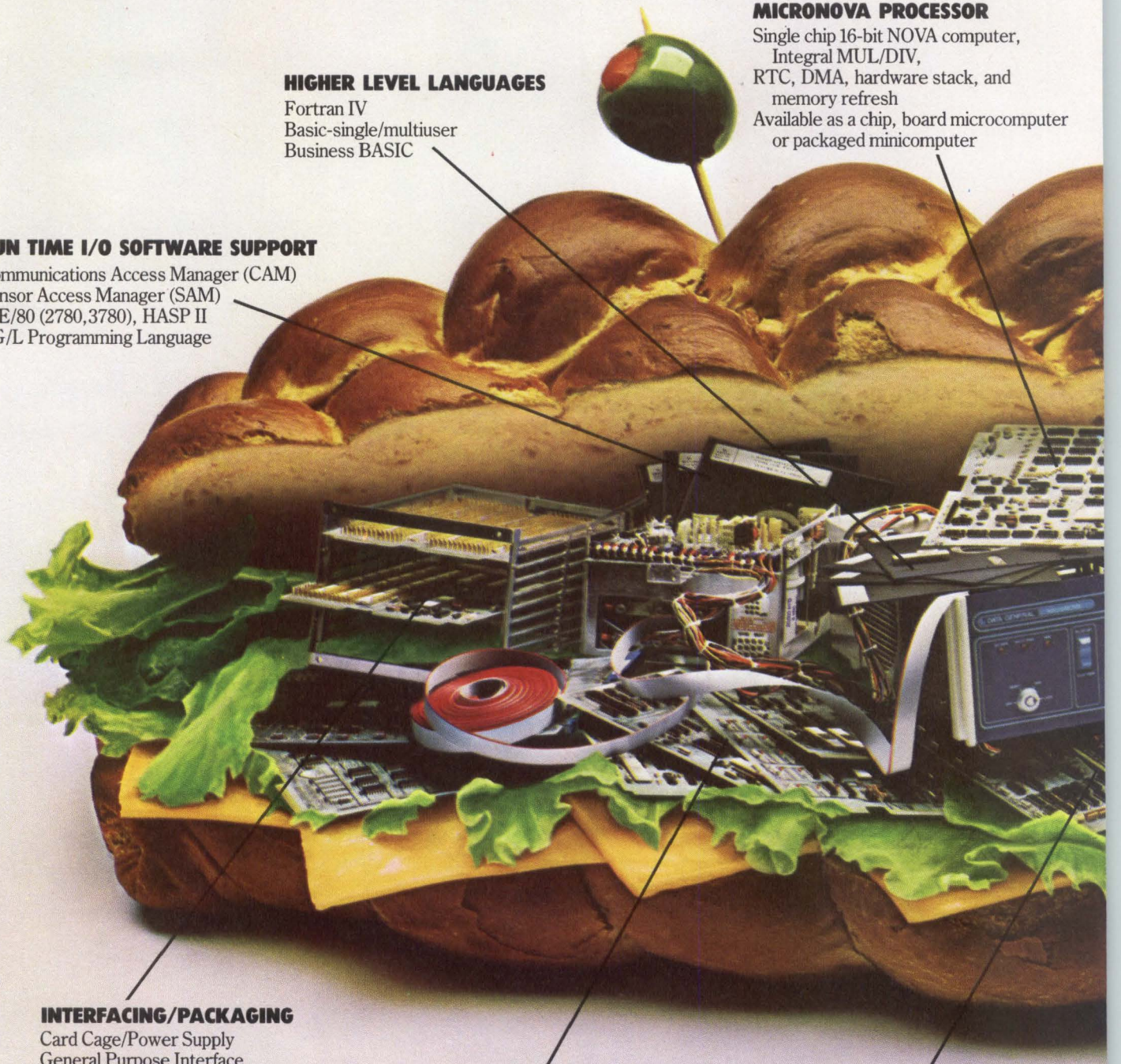

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CIRCLE 27 ON INQUIRY CARD

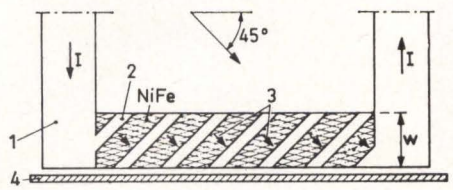

Fig 2 Schematic structure of thin-film pattern for barber pole, showing gold input leads (1), highly conductive gold bands deposited on NiFe strip (2), direction of current (I) through barber pole (3), and cross-section of magnetic tape (4), which is perpendicular to the plane of the drawing. Because of application of gold bands, current direction is rotated 45 deg

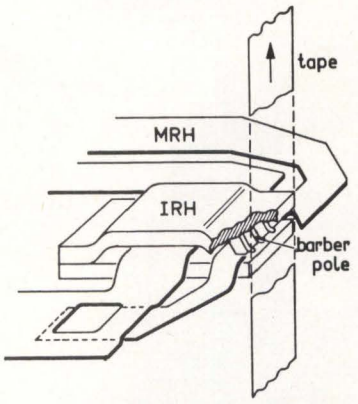

Fig 3 Sketch of combined read-write head, comprising MRH with barber pole and thin-film IRH

Two types of thin-film heads exist: inductive and magnetoresistive. The thin-film inductive recording head (IRH) is basically a miniature coil of only a few turns. It is well suited for writing information on magnetic discs and tape, but it is not really sensitive enough for readout. On the other hand, the magnetoresistive recording head (MRH) is more sensitive, but cannot be used for writing. An MRH usually consists of simply a nickel-iron (NiFe) strip. The output signal from this strip is a quadratic function of the magnetic field strength and, therefore, special measures must be taken to linearize its input/output characteristics. Since the working point on this characteristic is determined by the angle which the measuring current makes with the magnetic lines of force, it is essential to give this angle the correct value. A familiar method of doing this is to incorporate a permanent magnet in the head.

However, because the magnetoresistive effect is essentially nonlinear—an obstacle to applications requiring nondistorted reproduction of recorded information—a "barber pole" MRH construction has been developed. This consists of depositing a series of oblique bands of highly conductive material, such as gold, on a NiFe magnetoresistive strip which has a much lower conductivity (Figs 1 and 2). The input current (I) therefore no longer flows in the long axis of the strip but makes an angle with it—in this case 45 deg. Because of the preferred direction of the premagnetization, the NiFe strip is magnetized in the direction of its long axis, so that the current in the barber pole now also makes a 45-deg angle with the magnetic field to be read out. It has been found that this results in good linearization of the characteristic and maximum sensitivity.

Although the barber pole, as explained, can be used only as a read head and not as a write head, structurally it can readily be combined with an inductive write head provided the latter is also produced by the thin-film technique. A sketch illustrating such integration is shown in Fig 3, and Fig 4 shows a photomicrograph of a combined read-write head with barber pole. To realize these constructions, special etching techniques have been designed which produce thin-film patterns with chamfered edges. This facilitates the application of different patterns one above the other by greatly reducing the risk of interruptions in the upper layers.

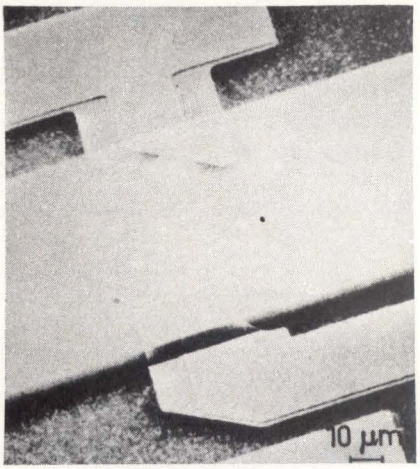

Fig 4 Electron photomicrograph of combined read-write head with barber pole

In the combined head, the barber pole is located in the gap of the magnetic yoke of the inductive head. Compared with an inductive read and write head, this combination has the advantage of a much greater read-out sensitivity, even at higher frequencies.

Results of these laboratory experiments do not necessarily imply a follow-up in production or marketing.

Transaction Processing System Offers 105M-bytes Disc Capacity

System 610, a transaction processing system for users who require large storage capacity, offers 35M bytes of disc storage in a basic system and is expandable to 105M bytes in a 3-drive system. Introduced by Basic/Four Corp, PO Box C-11921, Santa Ana, CA 92711, the system meets the needs of data processing sophisticated users who want to keep their files online.

The microprogrammed CPU is designed for execution of instructions written in BUSINESS BASIC language. Its speed is enhanced through use of semiconductor memory having a full cycle time of 600 ns. System features include an enhanced operating system; exception analysis system (EASY), an inquiry/reporting system specifically designed to produce special reports; and a Tri-State Language Processor™ which offers the

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online programming advantages of an interpreter, while providing the execution speed of a compiler.

The disc subsystem is organized around a programmable bipolar LSI processor which takes care of housekeeping chores normally performed by the CPU. This lessens the load on the CPU and offers greater system throughput. The disc system processor is also capable of performing selected error checking/correction routines which are built into the operating system, and can automatically execute test routines during the power-up sequence and during system initialization.

A spooling capability that allows the user to create print files quickly and easily is accomplished through use of a special serial file and associated buffer. When the buffer becomes full, it is automatically written to the serial file. This results in more efficient disc utilization, since data for several print lines is transferred in a single disc access.

Minimum configuration is a microprogrammed CPU with 40k semiconductor memory, video display terminal, 35M-byte disc drive, and 165-char/s printer. A maximum configuration has three disc drives totaling 105M bytes, 95k memory, eight display terminals, and up to two printers.

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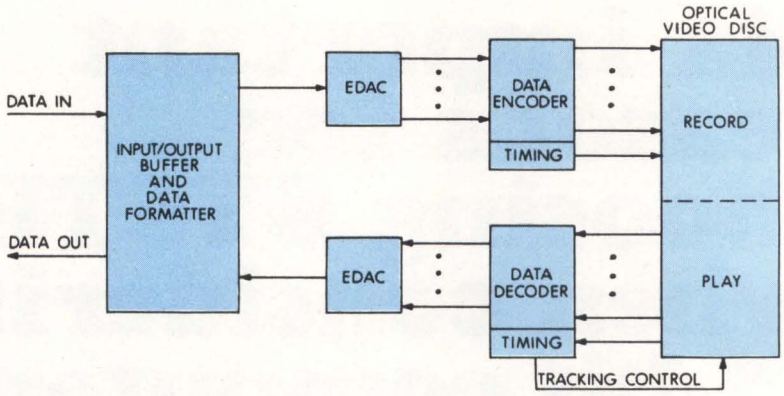

Block diagram of digital signal processing for RCA's optical video disc system. Error detection and correction (EDAC) recovers original input data even though various undesired changes are made in data during recording, storing, and/or reading data

Optical Video Disc Shows Promise For Mass Data Storage*

Because of their inherent capabilities for storing large amounts of data, discs have become basic media for TV programming storage and retrieval systems. Two different such disc storage based systems were developed at RCA's Advanced Technology Laboratories, Camden, NJ 08101. One, a capacitive pickup system that uses an electron beam for record and playback, was developed to meet home entertainment requirements. However, the second, although originally developed for broadcast studio use, is expected to find applications also in mass data storage and expanded memories for mini- and microcomputers. This optical video disc (OVD) system uses a laser for both write and read processes. The proprietary record/playback medium can be deposited on a number of different substrates, the one now used is a vinyl similar to ungrooved phonograph records.

During playback the disc rotates at 1800 r/min and stores the equivalent of 30 minutes of programming when used as a video recorder/reproducer. A blank disc is inserted onto the turntable and recorded live, using a modulated laser beam. Playback can be accomplished immediately or at any time thereafter by operating the laser at lower power and using a photodetector to pick up the reflected modulation.

Use of the OVD system for recording digital information requires the optimum selection of modulation, coding format, and error detection and correction (EDAC) codes. Information is recorded on the OVD as a 2-level signal (binary coded), due to the fact that recording is accomplished by using the "write" laser to remove material from the disc. Recorded signals are formed in a series of spots of varying length and spacing. Therefore, pulse coding must be employed to efficiently store information on the disc, and a complementary form of decoding must be used to recover the information during playback.

Serial input information must first be buffered to accommodate nonsynchronous data entry and then formatted into appropriate data blocks. Buffering handles both asynchronous data and data rates lower than the maximum rate of the OVD. Data blocking and the addition of appropriate header information facilitate organizing the data into convenient segments for addressing and error control.

Adding EDAC information is most important in digital recording systems where bit error rates (BER) of 10^{-7} and lower are desired. In record mode, check bits are added to the data and the resulting information is redistributed with respect to itself. In some EDAC systems a 1000-to-1 improvement in BER can be achieved with check bits comprising only a 10% overhead.

Several encoding formats are being examined for applicability to the OVD system. Some formats require addition of timing information to ensure proper decoding upon playback. The encoding portion of the system can also be set up to feed data into the disc on parallel tracks. The number of tracks used here can be different than that used in demultiplexing and EDAC.

Retrieving information recorded on a disc involves performing the inverse of the processing used for recording. Information read out of the

*Information in this article is abstracted from the paper "Optical Video Disc For High Rate Digital Data Recording" presented at the 1977 Electro-Optics/Laser Conference and Exposition by G. J. Ammon, R. F. Kenville, and C. W. Reno.

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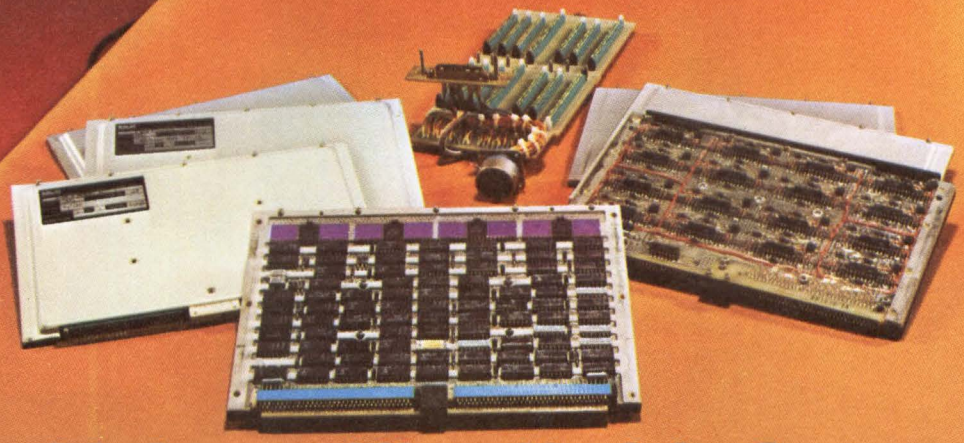

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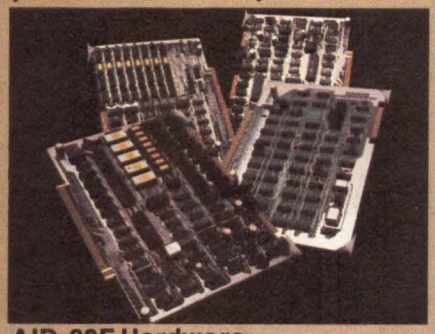

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AID-80F is priced at just $5995 and each board is also available separately. To get a complete descriptive package on the AID-80F Microcomputer, contact your sales representative or write Mostek Corporation; 1215 W. Crosby Road; Carrollton, Texas 75006; (214) 242-0444. Mostek GmbH; West Germany; Telephone: (0711) 701096

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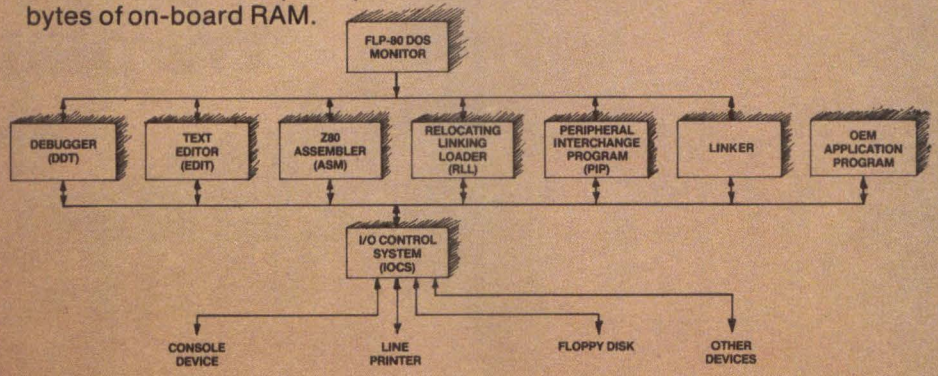

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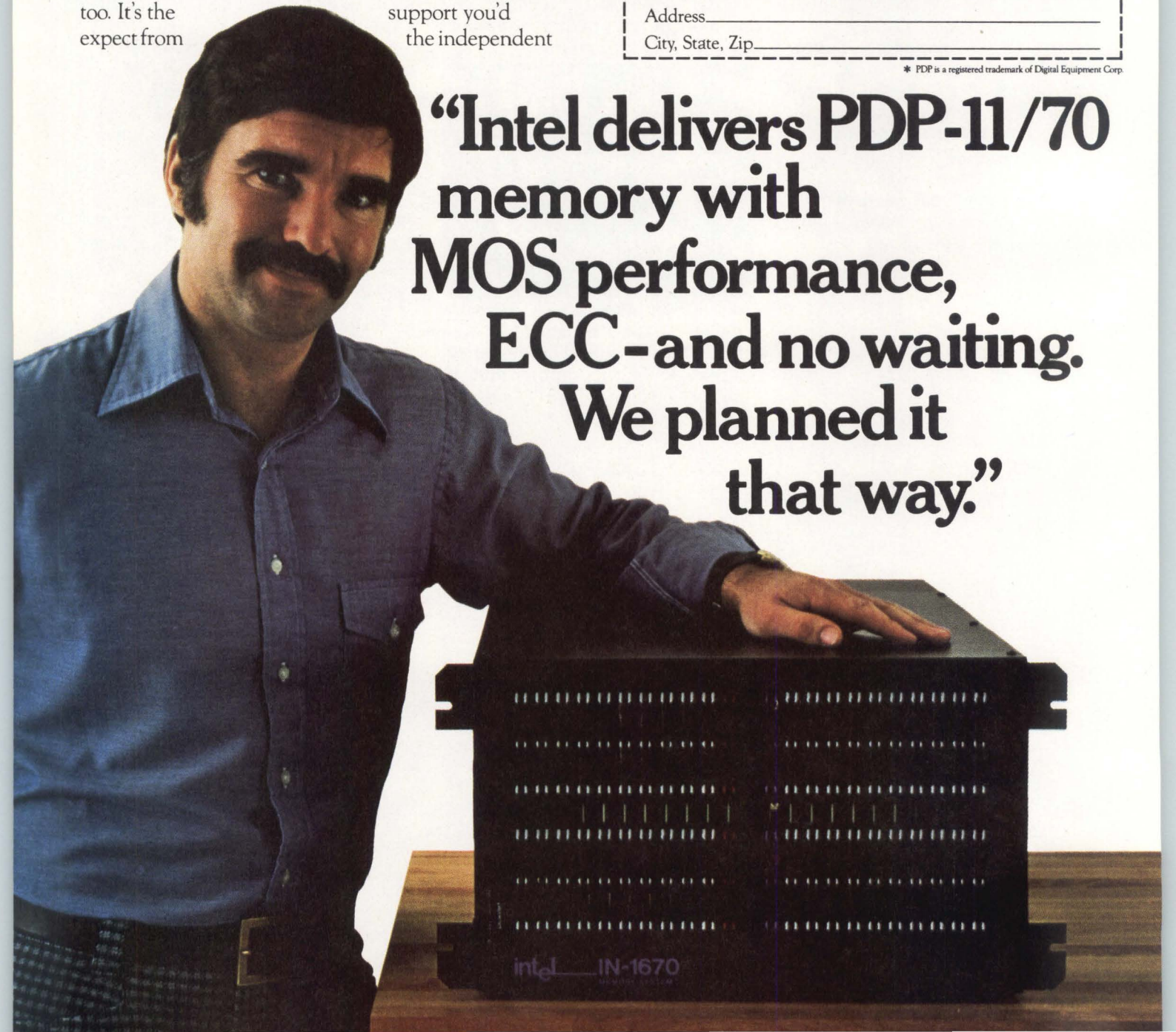

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tracks is first decoded to yield the basic input information with EDAC bits. Timing information obtained during playback is fed back to the disc drive to adjust rotational speed for optimum readout. EDAC circuitry checks the information out of the decoder and corrects the errors within the capability of the EDAC code. Finally the signals out of the EDAC circuitry are stripped of EDAC bits and fed to the multiplexer for recombination into the original input data format.

The system can be configured to record analog information with a signal bandwidth of up to 30 MHz, or a multiple track approach can be used to store digital information with a data rate of up to 200M bits/s. Storage of up to 5 x 10^{10} bits/disc side can be achieved with an access time of less than 1 s. Signal to noise ratio is 50 dB. Disc information can be updated and the system is considered to be compatible with automation.

Circle 145 on Inquiry Card

Small Computer System Adapts Readily to User's Needs

The 5110, a small computer system, exemplifies current trends in technology and cost which bring greater amounts of processing power within reach of virtually all businesses. Announced by International Business Machines Corp, General Systems Div, PO Box C-1645, Atlanta, GA 30301, the system offers a choice of four main storage capacities, two storage media, and two programming languages, allowing users to obtain a system that fits specific needs.

Featuring a desktop unit which houses CPU, typewriter-like keyboard with 10-key calculator pad, and a 1024-char display screen, the system offers the ease of use and compactness of the IBM 5100 computer (see *Computer Design*, Nov 1975, pp 130-131). Extended hardware capabilities, language enhancements, and improved internal performance are additional features.

The system provides full display screen management. Users can position data anywhere on the CRT, and have the option of an upper/lower case display. Data can be black on a white background, or the reverse.

Storage for 204k bytes of information is provided by magnetic tape cartridges. Two 5114 diskette units, each housing two diskette drives, can be attached to supply capacity for 4.8M bytes. Diskettes can be interchanged with other IBM systems. The computer can access data randomly on a diskette in approximately 200 ms, can read data at 48k bytes/s, and can write and verify data at a rate of 19k bytes/s. Model 1 uses tape and/or diskette; model 2 offers diskette only.

Data handling is facilitated by several programming features. Operators can group information on diskettes in records and access records directly, in sequence, or by indexed files. Up to 10 multiple open files are permitted on diskette. Users can build procedure files so that job streams can be executed without operator intervention. An optional hardware sort feature offers full record and address out sorting and is capable of sorting both secondary and primary fields in ascending or descending sequence.

Systems can communicate with some other IBM systems and devices. With asynchronous capability, the 5110 appears to a remote System/370 host as a 2741 communications terminal. With binary synchronous capability, it appears as an 2770 or 3741 to the host; this feature can be programmed in APL or BASIC. Appearing as a 3741 allows the 5110 to interact with a remote System/3, /32, or /34, or as another 3741 or 5110.

I/O devices available for attachment include the 5106 model II auxiliary tape unit and 5103 models 11 and 12 printers. Providing the advantages of upper/lower case output and capability to overlap printing with application processing, models 11 and 12 print bidirectionally at 80 and 120 char/s, respectively. Use of serial or parallel interfaces permits card and paper tape devices, printer/plotters, terminals, and instrumentation to be added to the system.

Ranging in price from $9,875 to $32,925, systems are supported by software which includes commercial and problem-solving programs. An upgrade to incorporate 5110 features into purchased 5100s will be available in June at a price from $3800 to $5800.

Circle 146 on Inquiry Card

Computer System Offers Twice the Power of Predecessor

V-8590 and V-8580 computer systems are the most powerful yet introduced by NCR Corp, Dayton, OH 45479. In addition to using the internal bus architecture, ECL circuitry, DMA, and diagnostics of earlier 8000 series models, the systems incorporate more efficient memory and processors with 56-ns cycle time.

With approximately twice the power of its predecessor, the V-8570, the -8590 capitalizes on internal transfer bus architecture, using two processing elements which share all system resources. Memory is expandable from 2M to 6M bytes in 1M-byte increments. Communications multiplexers can provide extensive communications capabilities for handling large numbers of terminals.

The -8590 implements an I/O method which incorporates an I/O link protocol that permits data transfer in a serial bit stream at 2M-bytes/s. Advantages of the method include increased speed, greater flexibility in configuring peripheral units, reduced channel contention, and lower overall cost. The discipline is implemented using an I/O link controller capable of accommodating four I/O links. Each controller attaches directly to the system's internal transfer bus. Each system can accommodate up to 24 I/O links.

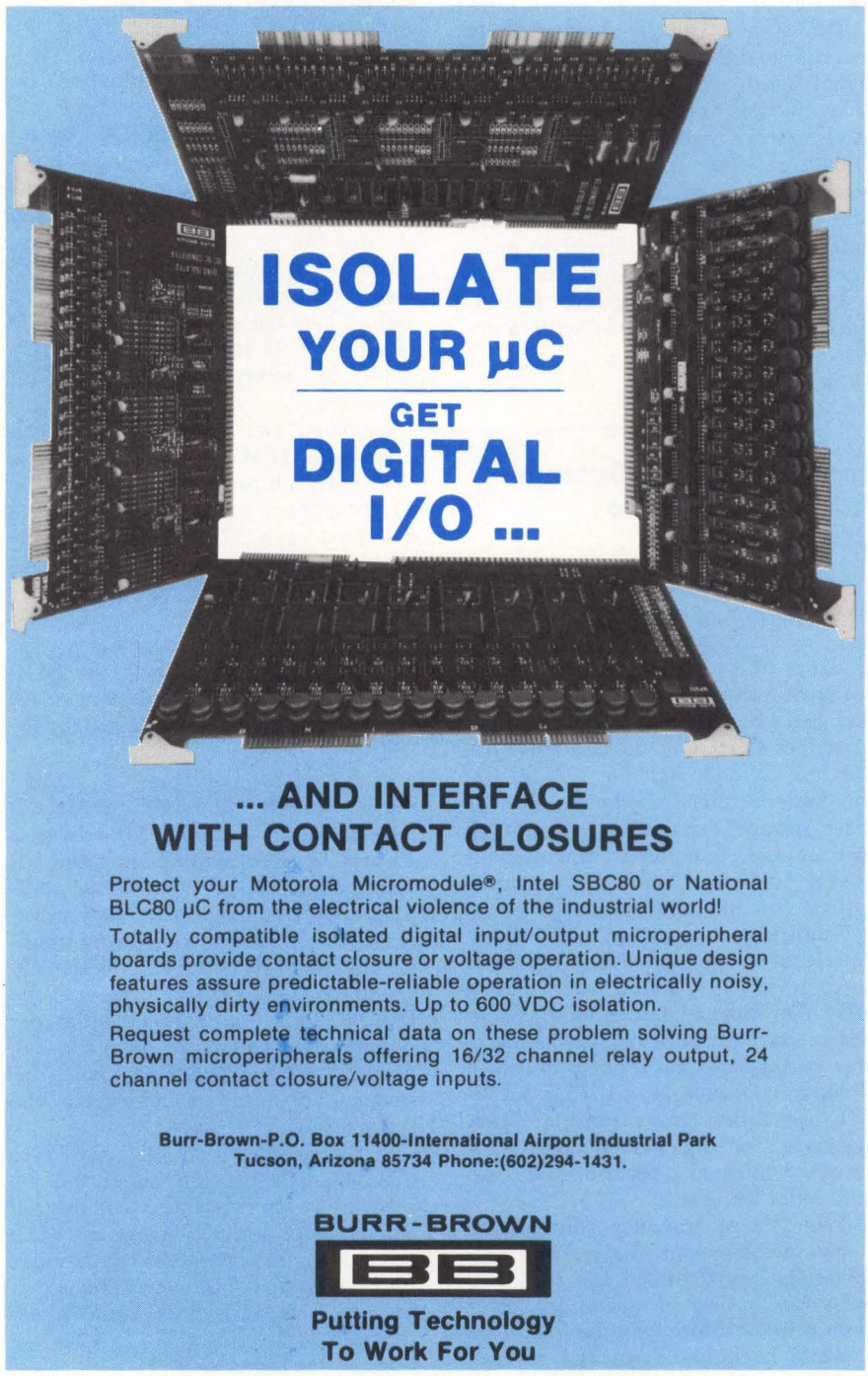
Peripherals using the I/O link protocol include the 6540 data storage subsystem and the 6370 group coded recording tape unit. 658 disc units and 647 printers also use the protocol.

A basic -8580 processor includes three I/O trunks. The system accommodates from 1M to 4M bytes of memory. Communications can be provided by both an integrated communications subsystem and by a free-standing communications multiplexer. Memory in both systems uses 16k-bit technology and features error detection and correction with 4-way interleaving, a memory design technique that allows several processing subsystems to access memory simultaneously. A hardware assist unit performs all operations necessary to set up a command for execution while a previous command executes.

Both systems operate under the virtual resource executive, and can operate in "N" (NCR Century) mode, in which a system is conditioned through firmware to operate as if it were a Century system. Languages available with the two systems include COBOL 74, NEAT VS, FORTRAN, and RPG. Century languages, COBOL 68, and NEAT/3 are also available.

Purchase price for a V-8580 in minimum configuration is $517,000. Deliveries are scheduled for third quarter of this year. V-8590 processors with minimum of 2M-byte memory are priced at $720,000. First units will be available in the last half of the year.

Circle 147 on Inquiry Card



At only $1088, you can't offer your customers a better buy.

Our quantity-50 OEM price for the *Silent 700** Model 743 KSR Terminal is now just $1088†. In larger quantities, the price goes below $1000.

And it keeps on costing less because the real payoff is in the cost of ownership. In the long run, it costs less than any other printer terminal with comparable performance.

The reason is easy. Superior design. The 743 KSR is built around a TI microprocessor. So, there are fewer components and circuit boards than in other printer terminals. That means less maintenance and more uptime performance. Plus standard EIA and current loop interfaces in a lighter, desk-top package.

The 743 features the speed, reliability and quietness that made the *Silent 700* terminal family so popular. Incoming data is buffered, so you get true 30 characters-per-second throughput.

TI's Model 743 KSR

Disturbing noises associated with impact printers are eliminated with the 743's non-impact electronic printing.

Use it as a console I/O for software development. Keyboard terminal for inquiry/response.

Data entry. Interactive remote computing. Or as a message terminal network. And it's now available with APL. The 743 is backed by TI's worldwide maintenance and support services.

Find out more about TI's 743 KSR printer terminal. Fill out and mail the coupon today. Or call your nearest TI sales office, or Terminal Marketing, (713) 491-5115, extension 2126.

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When you put a name like Classic on a new computer, you've either got a lot of nerve. Or a lot of computer.

Introducing the MODCOMP Classic.

A lot of computer.

Forget megabytes, bits and nanoseconds for a μ sec.

Because what you really need for a successful computer installation is cost/performance, ease of implementation and reliability/maintainability.

For years, MODCOMP has led the medium class computer market in all of these critical areas.

Now we've set a new standard for super minis.

The MODCOMP Classic.

Classic. A lot of computer. But not a lot of money.

The Classic costs less than any other super mini on the market. Yet, in benchmark tests, it's outperformed the best of them. The reasons?

- A new super-fast floating point processor.
- Lightning fast context switching provided by seven MAP files and 240 general purpose registers.
- MOS or core memory with effective cycle times as low as 150 nanoseconds.
- Up to 0.5 megabytes of memory is directly addressable.
- A unique multi-word (16-80 bit) architecture.
- An enhanced instruction set, with 55 special Fortran oriented instructions.
- I/O processors that can handle up to eight million bytes per second.
- And a CPU that can execute many instructions in 200 nanoseconds.

Built to save you the biggest expense of all - downtime.

The Classic will give you the performance you want. It's also designed to give you the reliability and maintainability you need.

Our exclusive wire-wrapped PC boards are more reliable and easier to service than soldered boards. Hardware diagnostics and convenient test connectors allow you to test all system components and locate faults quickly. And the PC boards plug in and out for easy, fast replacement.

When you buy a Classic, you also get our experience and product development tools to help you get your system up and running fast. And our service and support to keep your system running, successfully.

A complete family of computers. Plus field-proven software.

The Classic is not just one new computer. It's a complete family of computers, supported by a full complement of peripherals, process I/O interfaces and software operating systems for process control, data communications, terminal-based information processing, business data processing and distributed networks. And the Classic is upward compatible with all other MODCOMP computers.

Whether you're a computer user or an OEM, if you're thinking about buying or expanding a computer system, consider cost *and* performance. Short term *and* long term.

And consider Classic. Because when you get to the bottom line, there's only one choice, Classic.

For more information, send for our brochure.

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My application is _____

My need is ____ immediate ____ soon ____ future

Upgraded Interactive Application System Supports 32 Users

IAS version 2, an enhanced interactive application system for large PDP-11 systems, is designed to support up to 32 interactive users—12 more than its predecessor—as well as additional peripheral equipment and software options. In addition to greater user capacity and increased hardware options, the software extends communications flexibility and system utilities, and is compatible with more laboratory and industrial real-time interfaces.

Announced by Digital Equipment Corp, Maynard, MA 01754, the general-purpose, multifunction operating system extends support to the -11/60 CPU, RP05 and -06 disc storage subsystems, and the RX01 floppy disc subsystem. The multilanguage system supports RPG-11 and CORAL-66 in addition to BASIC, COBOL, FORTRAN IV, and FORTRAN IV-Plus. Data services include multikeyed ISAM capability of RMS, DBMS, SORT, and DATATRIEVE.

Circle 148 on Inquiry Card

Growth Offered for Out-of-Production Computers

Three families of computers—TCP-16, -24, and -32—emulate out-of-production computers from Lockheed, General Electric, and Xerox, allowing users of these mainframes to expand their computing capabilities without any change in software or operating procedures. Introduced by Telefile Computer Products, Inc, 17131 Daimler St, Irvine, CA 92714, the systems also represent a step-function improvement in performance and a reduction in cost.

Processing programs written for the Lockheed MAC-16 and LEC-16, TCP-16 computers reduce context switching from 6 to 1.6 μs. Furthermore, they offer additional multiplex data channels, more DMA channels, and a multiport memory system. TCP-24 computers emulate the GE-400, and -32 mainframes start where the Xerox Sigma 9 left off. Both of these units will provide a 4-to-1 improvement in performance as well as significant decreases in size and cost.

Circle 149 on Inquiry Card

MARK IV System Release Improves Efficiency and Flexibility

Major changes and improvements in terms of efficiency and flexibility to the MARK IV system are contained in Release 7.0. Highlights of the modified system from Informatics Inc, 21031 Ventura Blvd, Woodland Hills, CA 91364 are enhanced ease of use and extended capabilities for IMS and TOTAL data base management system users.

The system will provide query capability for CICS and INTERCOMM teleprocessing environments through Query Language/CICS and Query Language/INTERCOMM. These two products feature English-like syntax, text editor, data base support, and sequential or random data access.

Upward compatible from Release 6.0, Release 7.0 requires no modification to existing programs. It will be distributed at no cost to subscribers of the company's Annual Improvement Maintenance and Support service.

Circle 150 on Inquiry Card

Monitoring Systems Allow Detection of Disturbance Values

Oscillostore, Datastore, and Eventstore systems permit anomalies to be detected and analyzed when recording and monitoring chemical and physical processes. To provide the history of operation in an undisturbed state that is necessary to provide optimum disturbance sensing, Siemens AG, Postfach 103, D-8000, München 1, Federal Republic of Germany incorporated digital memories into the systems, which consist of function modules that may be combined to fit specific requirements.

The Oscillostore system consists of a measuring device with memory (static data carrier) and recorder for monitoring operating conditions. The system processes analog as well as binary measurement signals and can detect general disturbances as well as critical operating conditions. The Datastore system consists of a measuring device with memory and magnetic tape recorder (dynamic data carrier). It processes analog and binary input signals and can be used to detect general disturbances or critical operating conditions. Data recorded on the dynamic data carrier can be further processed on a computer. The Eventstore system is a measuring device with memory and printer (static and dynamic data carrier), with which operating conditions can be monitored and disturbances (events) logged immediately. The system has binary measurement signal inputs only.

In the Oscillostore, measurements to be checked are scanned using a multiplexer and are fed via A-D converters into a shift register, which allows for start-up of evaluating units such as recorder or printer, and thus gives a rough idea of the source of the disturbance. Digital values are then reconverted into analog quantities by means of system modules and are fed into recording equipment.

Datastore is based on the same design principles, but uses a different data carrier. Instead of a recorder (static data carrier), a magnetic tape cassette (dynamic data carrier) is employed so that recorded data can be teletransmitted directly to a computer.

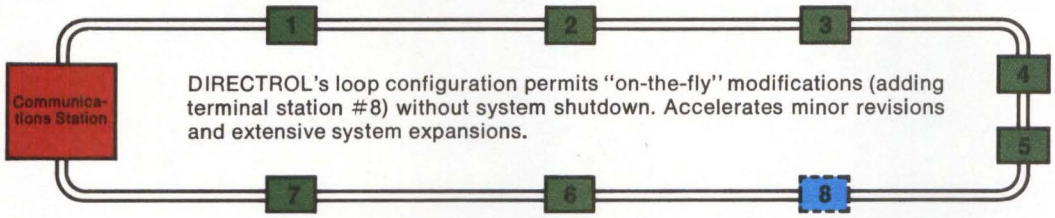
Using modules of the Eventstore (data logger modules), binary signals appearing in processes can be detected. The system has an input insulation level of 5 kV. Up to 2000 different measurement inputs can be scanned in 1 ms. Since results can be logged with printers, status changes with the corresponding numerical assignment can also be detected or additional alphanumeric information printed out.

When remote transmission of information from decentralized points is required, only mean values are transmitted since the number of transmission channels available is limited. The instantaneous values detected are, therefore, reduced to mean values before transmission. □

Circle 151 on Inquiry Card

New DIRECTROL™ Multiplexer. Signaling new directions for industrial control.

Cutler-Hammer's new DIRECTROL . . . finally, here's a multiplexer that's practical for industrial control application. DIRECTROL achieves startling advantages in project simplification, system productivity and plant versatility.



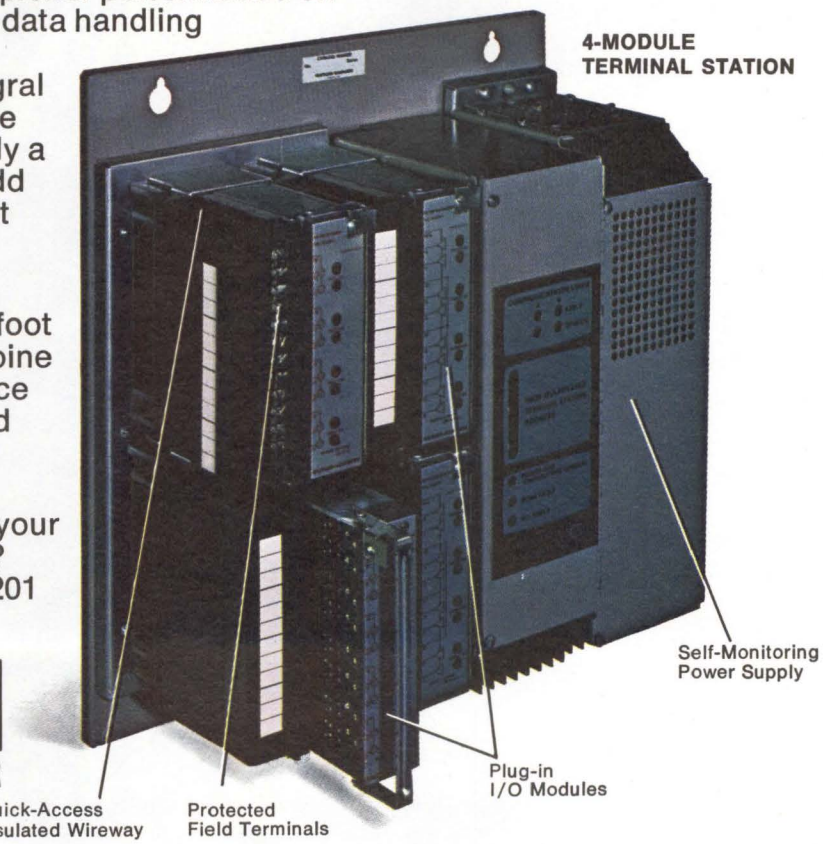
DIRECTROL's loop configuration permits "on-the-fly" modifications (adding terminal station #8) without system shutdown. Accelerates minor revisions and extensive system expansions.

Project simplification. DIRECTROL is designed and applied in a conventional control manner. But unlike the conventional, it substantially reduces wiring costs and project complexity—easily adapting to unanticipated requirements. For the first time, DIRECTROL offers control multiplexing in easy-to-apply, easy-to-order, easy-to-install modules.

System productivity. DIRECTROL's innovative approach provides high-yield features like monitoring of multiplexer performance on every signal scan, high security data handling routines, self-diagnostic/self-correcting characteristics, integral high noise immunity and multiple redundancy options to name only a few. Plus the unique ability to add new stations "on the fly" without affecting system operation.

Plant versatility. DIRECTROL's 4,096 signal capacity and 5,000 foot distance between stations combine with "stand-alone" independence or computer compatibility to add dramatic equipment selection flexibility for future needs.

Why not set a new course for your industrial control requirements? Write Milwaukee, Wisconsin 53201 for descriptive brochure.



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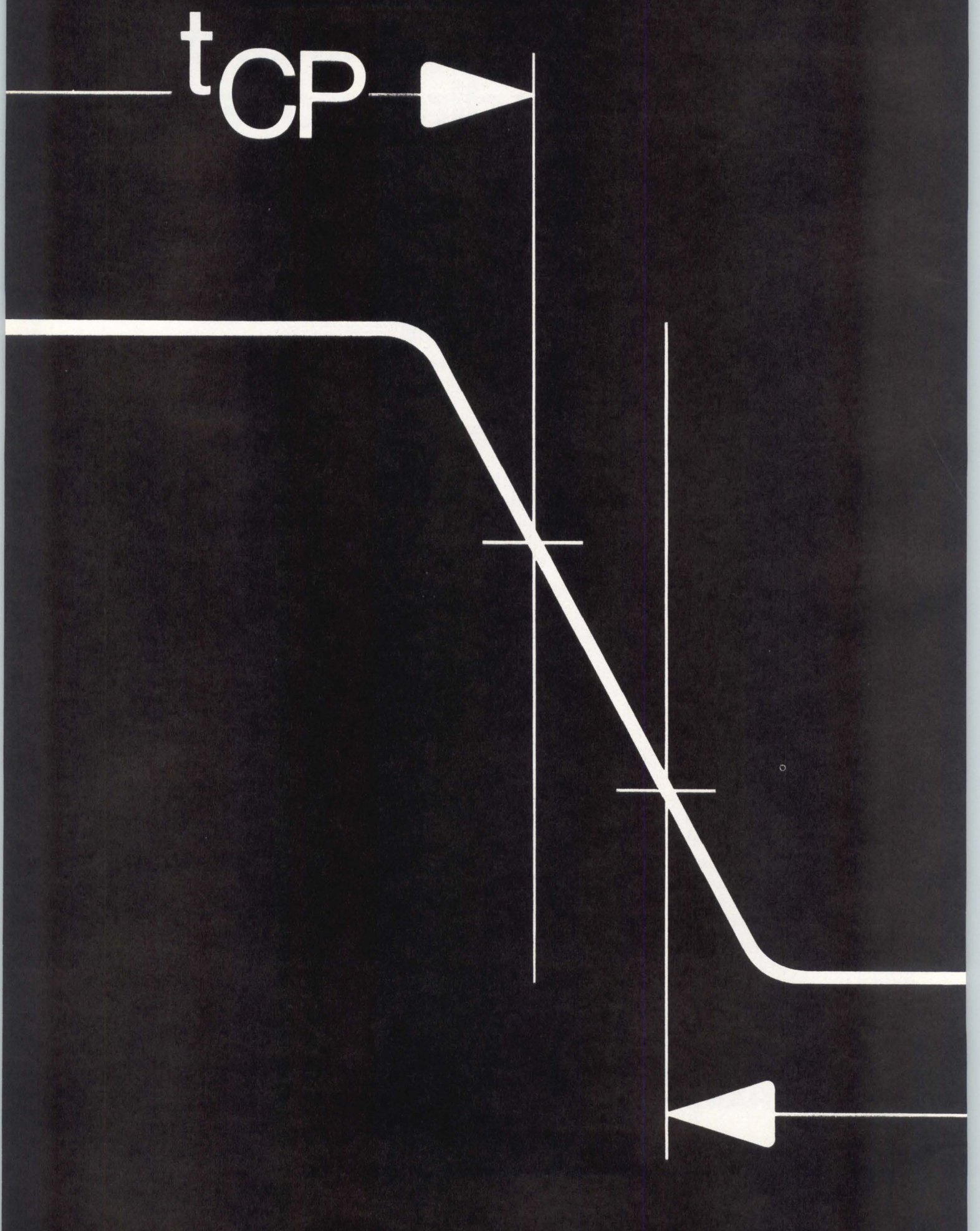

t_{CP}

TERADYNE'S MEMORY TEST SYSTEM GIVES YOU A DEFINITE EDGE.

Only Teradyne's J387 Memory Test System gives you Automatic Edge Control. A vitally important feature that eliminates the risk of inaccurate edges and the time and tedium of manual edge-setting.

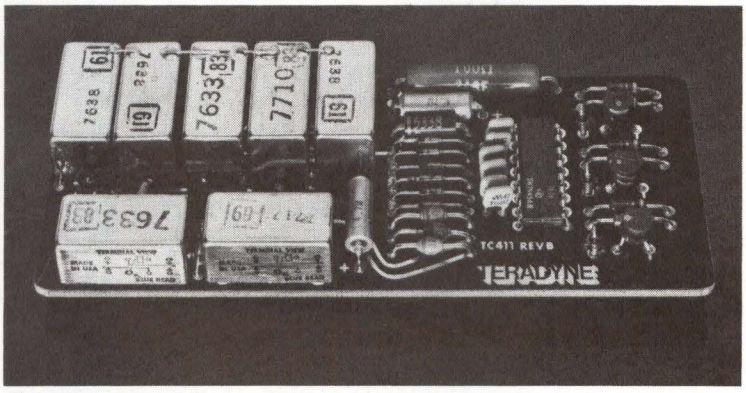
With Automatic Edge Control calibration becomes a function of the system itself. A function it performs automatically in a matter of a minute or two.

Now calibration can be performed often enough to keep edges repeatable. No more hours of downtime every week for recalibration. No more risk of human error.

The advantages are obvious. With 16k and page-mode parts in production, timing integrity is more vital than ever. Automatic Edge Control guarantees this integrity. And the fallout from that is strictly financial.

LEARN MORE.

Automatic Edge Control is one of the most important reasons why the J387 is the hands-down leader in memory testing. But it's far from the only reason. If you produce memories or use them in volume, send for our new booklet, "Memory Testing With a Difference." It will tell you why owners of the J387 have such a definite edge. Write Teradyne, 183 Essex Street, Boston, MA 02111.



This circuit module has revolutionized memory testing. With it Teradyne's J387 calibrates its edges automatically. At a rate of an edge per second!

TERADYNE

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DIGITAL CONTROL AND AUTOMATION SYSTEMS

Single-Board Microcomputers Monitor and Control Hydroelectric Plant With Remote Supervision

Operating an entire hydroelectric plant—including four generators—from the control room of another plant 90 miles (145 km) away allows the Army Corps of Engineers to save about five man-years annually. In addition, using microcomputers instead of hardwired logic or even minicomputers has saved thousands of dollars in system development, hardware, and installation costs.

Believed to be the first application of microcomputers for direct control of both water flow and power generation in a major hydroelectric power system, the system uses three microcomputers—two at the hydroelectric plant and one at the "base." The hydroelectric plant, known as the Jones Bluff project, is located on the Alabama River in the state of Alabama about 35 miles (56 km) northwest of Montgomery. It produces an average of 329 million kilowatt hours annually. The dam is 342 ft (104 m) long and 150 ft (46 m) wide with 11 spillway gates, each 50 x 35 ft (15 x 11 m). The "base" plant is located about 90 miles (145 km) farther southwest along the river at Millers Ferry.

Each of the three microcomputers in the system is an IMP-16C/200 from the Microcomputer Systems Group of National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. Of the two "remote" microcomputers, one performs data acquisition and monitors meteorological conditions, while the other handles plant control—both water flow and power generation. The base microcomputer serves as central supervisory unit for the two remotes. System organization was designed by Progress Electronics of Oregon, Portland, Ore.

System Functional Description

Essentially, the three microcomputers function as a distributed computer network (see diagram). They communicate in digital format over a single microwave link which contains a repeater station to regenerate 7- to 8-GHz multiplexed signals. Signals are converted and reconverted at each position by 300-baud modems.

Each microcomputer is a complete 16-bit system packaged on an 8.5 x 11″ (21.6 x 28 cm) printed circuit board. Space is included for necessary memory, arranged on the boards in RAM, ROM, p/ROM, and CROM as required.

The data acquisition microcomputer at the Jones Bluff hydroelectric plant contains 4k words of p/ROM and 1k words of RAM. It monitors approximately 20 parameters for each of four 17-MW generators, including output power load, voltage, reactive power, and demand in megawatt hours. In addition, it checks meteorological conditions such as wind characteristics, as well as river elevations and rainfall. This information is sent to the supervisory microcomputer at the Millers Falls plant over the communications link. All data readings are updated every two seconds.

Data from the data acquisition microcomputer are processed by the supervisory microcomputer which is interfaced directly to the control console. This supervisory microcomputer contains 10k words of p/ROM and 1k words of RAM. It computes values and converts raw data to engineering units. In addition, it serves as communications processor for transfer of data in both directions over the microwave link. Based on control steps built into firmware, this microcomputer codes and decodes multiplexed signals sent over the link, sets line protocol administration, assembles messages, checks syntax, and detects errors.

Operators at the Millers Falls plant can alter generator outputs by setting a switch or dial on the control console switchboard. This console contains a panel of 100 switches plus LEDs for alphanumeric display of data for operator readings. Operator changes in control parameters or setpoints are fed to the supervisory microcomputer for processing.

An Interdata 70 minicomputer at the Millers Falls plant interrogates the supervisory microcomputer every six minutes for data logging and record keeping. Every data point monitored at Jones Bluff is continuously updated. Summary tabulations of dam operations are based on data obtained by the minicomputer.

Control functions at the Jones Bluff plant are carried out by the control microcomputer under direction of the supervisory microcomputer. The control microcomputer contains 256 words of p/ROM and 1k words of RAM. It receives control signals from the supervisory microcomputer over the communications link, determines the necessary action to be taken, and carries out various operator actions through an array of relays. This includes placing all four generators on- or offline by throwing large circuit breakers, opening or closing concrete dam gates to regulate water flow, and actuating speed-adjustment motors to load or unload generators. A control algorithm is contained for each function.

(*Continued on p 66*)

FOR RENT... NOW...

the truly universal PROM Programmers from Data I/O that enable you to program any of the more than 200 PROMs now available.

A single Data I/O programmer—the Model V or Model IX—can be used to program every single commercially available PROM.

Data I/O programmers are universal. You can use them to program any PROM, and more than 200 PROMs are currently available. This means you don't have to get a separate programmer to accommodate different PROMs. With either the Model V or Model IX and the appropriate personality card, you can program any PROM or its second source equivalent. Moreover, one personality module can be used to program all PROMs within a generic family and keep your yield at the maximum.

ROM emulation and editing capabilities are built-in, making software development a breeze and virtually eliminating PROM waste.

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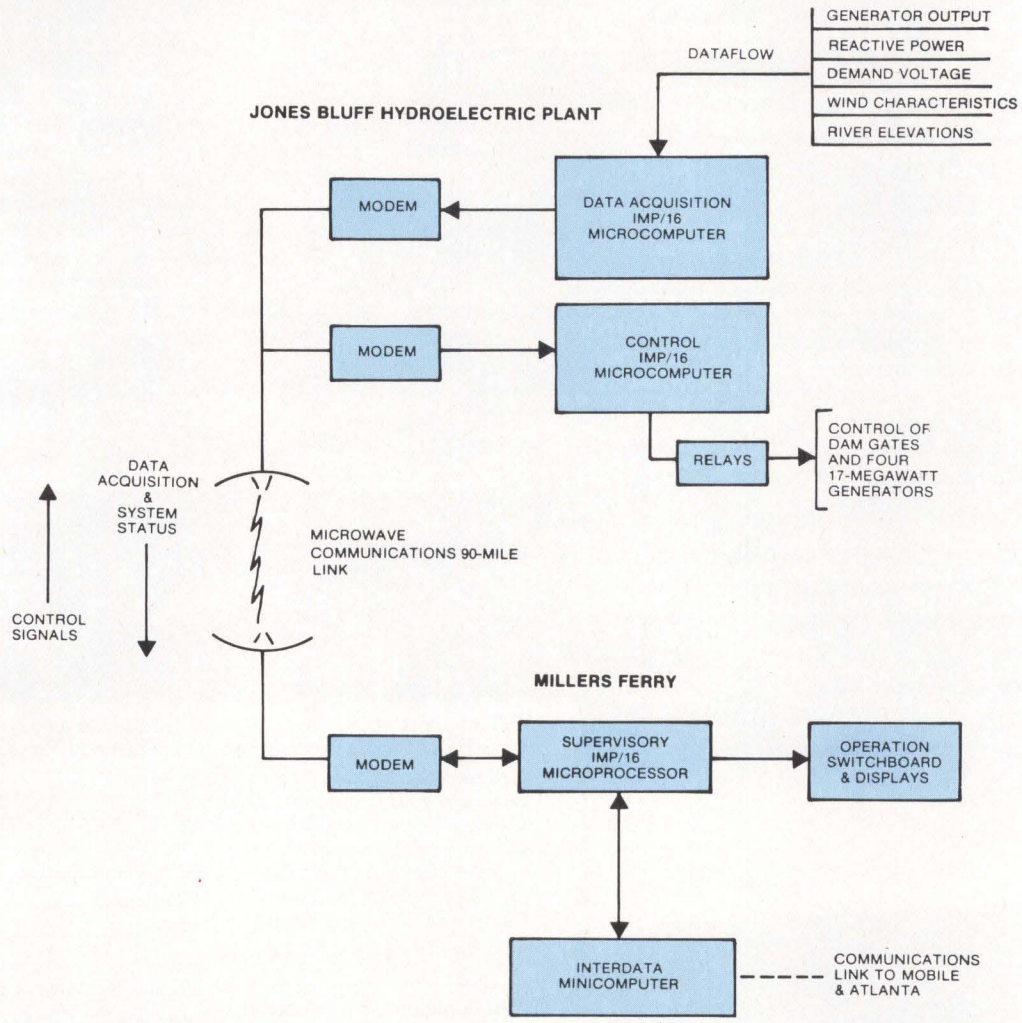


Three-microcomputer distributed processing network for remote control of hydroelectric plant. Data acquisition microcomputer monitors meteorological conditions and generator output at dam; supervisory microcomputer assesses that information and determines what, if any, adjustments must be made; and control microcomputer opens or closes dam gates or adjusts speeds of four generators. All this is accomplished over a 90-mile (145-km) span via a microwave communications link—which is also maintained by the supervisory microcomputer. Minicomputer interrogates supervisory microcomputer to obtain data to be logged for summary tabulations of dam operations

To assure correctness of control communications, the control microcomputer transmits commands received from the supervisory microcomputer back to the control console. There, the supervisory microcomputer compares the returned signal with the one originally sent and sends a verification signal if they match. This full process requires one second.

The verification procedure eliminates chance of transmission errors, inadvertent illegal commands, or orders to units taken offline for servicing. An alarm bell

Announcing another new 6250 bpi tape transport...

For minis!

Engineering breakthroughs enable Telex to bring big computer storage and reliability to OEMs at a fraction of the size and cost.

The long-awaited 6250 bit-per-inch (bpi) tape drive for minicomputers is here.

The Telex Model 6250.

It offers minicomputer users nearly four times the tape capacity of the previous 1600 bpi drives. Yet it takes up only one-fourth the space and costs only about half as much as the worldwide accepted, big box 6250 bpi units Telex has supplied to IBM users for years.

The four-to-one size reduction wasn't easy.

It took three years and a whole new standard of design to pack all that technology in a 19-inch frame. Parts innovations. Creative placement of needed elements. New materials. All have led to a remarkable achievement in simplicity and reliability.

The machine meets all the stringent requirements of true high density, 0.3-inch inter-record gap recording in both read and write operations.

In addition, the drive:

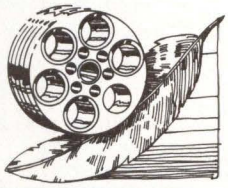
- Handles all three standard data formats—NRZI, PE and the new GCR.

- Runs reliably at speeds to 125 inches per second (models are also available at 45, 75 and 100 ips).
- Transfers data at the high speed of 781 kB per second (so off-loading can be done at nearly disk speeds).

- Rewinds a full 2400-foot tape reel in less than a minute. (That's 500 inches per second!)
- Reduces the complexity and cost of field maintenance (all work is done from the front).

Remarkable new capstan weighs only 1.9 grams.

To feel this Supr-Lite™ capstan is to believe its engineering achievement.



Not only does its lack of weight reduce inertia, it lets us use a smaller motor. Heat is reduced. Cooling blowers and hoses are eliminated.

Capstan walls are only 1/1000-inch thick, yet its patented manufacturing process assures strength, absolute roundness (and users a more consistent data rate).

Telex tape path gets you up to speed in a hurry.

Perhaps the most dramatic example of how Telex miniaturized the 6250 is its patented tape path. The path is very compact, yet it retains four vacuum columns (just like big brother).

It brings new efficiencies in tape dynamics and reduces the length of tape required between head and primary vacuum columns.

Combined with our new capstan, friction and mass are cut down so much that the unit runs tape full speed forward to full speed reverse in a mere 0.13 inches (a new record).

Special vacuum buffers and fixed air bearings gently handle tape at the high program rates possible with short inter-record gap operation. They eliminate long spans of unsupported tape, thus avoiding harmful tape oscillations that can restrict programming.

And we're so confident of tape servo reliability that we covered up the tape path with the operator's panel (further reducing space requirements).

New controller/formatter handles up to eight drives.

It includes the same proven logic design as our big controller, only miniaturized to fit a 10½-inch-high, rack-mounted box. And it's flexible enough to intermix all four tape speeds and all three densities—800, 1600 and 6250 bpi—in the same subsystem.

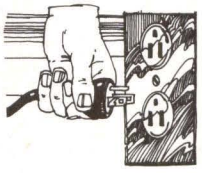
A built-in microprocessor handles extensive diagnostic routines.

When maintenance is required—on either controller or drive—the machine helps the technician quickly isolate faults down to board level for simple replacement. Given on-hand parts, a disabled machine should take less than an hour to fix. And all maintenance is done from the front.

Plug it in and go, it's that simple.

A common wall socket is all that's needed. And no special air conditioning. You can even operate it from a truck.

Design innovations with a goal of simplicity have enabled Telex to bring OEMs this remarkable new tape transport and controller. Large minicomputer users need this 6250 bpi mass storage capacity. Both dual density 800/1600 and 1600/6250 bpi models are available for 90 day delivery. Be the first to offer them.



Write or call Mr. Dan O'Neill, Telex Computer Products, Inc., 6422 E. 41st Street, Tulsa, Oklahoma 74315. Telephone: (918) 627-1111.

TELEX®

Miniaturization...in a big way.

automatically alerts an operator if there is any breakdown in communications.

Summary

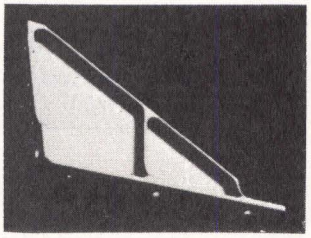
Closed-loop control routines for this overall system are stored in p/ROM, while RAM is used for temporary storage of data. Microprogramming is contained on one control read-only memory (CROM) with a 43-instruction set. Additional CROM can be added if arithmetic or peripheral handling capabilities are expanded at a later time.

A design approach based on microcomputers instead of hardwired logic enabled this system to be developed on a single set of control subroutines which can be applied to each of the four generators. Hardwired logic would have required the hardware to be duplicated for each generator.

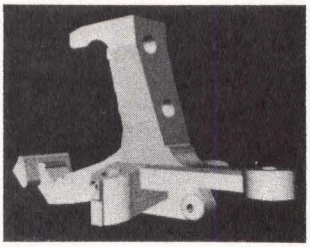
Programs Generate 3-D Presentations for CAD and CAM Applications

Creation of 3-dimensional views of complex, solid parts and systems has long been a desired capability for computer aided design systems. However, design engineers using Boeing Corp's Computer Services Co will now have access to a process—called SynthaVision—with this capability. Developed by Mathematical Applications Group, Inc, 3 Westchester Plaza, Elmsford, NY 10523, the process consists of a set of proprietary FORTRAN programs designed for use mainly with CAD and CAM systems. It typically will enable users to generate a 3-dimensional mathematical model, slice through it at any point from any angle, produce line drawings of any cross section needed, and analyze the object at any of these points.

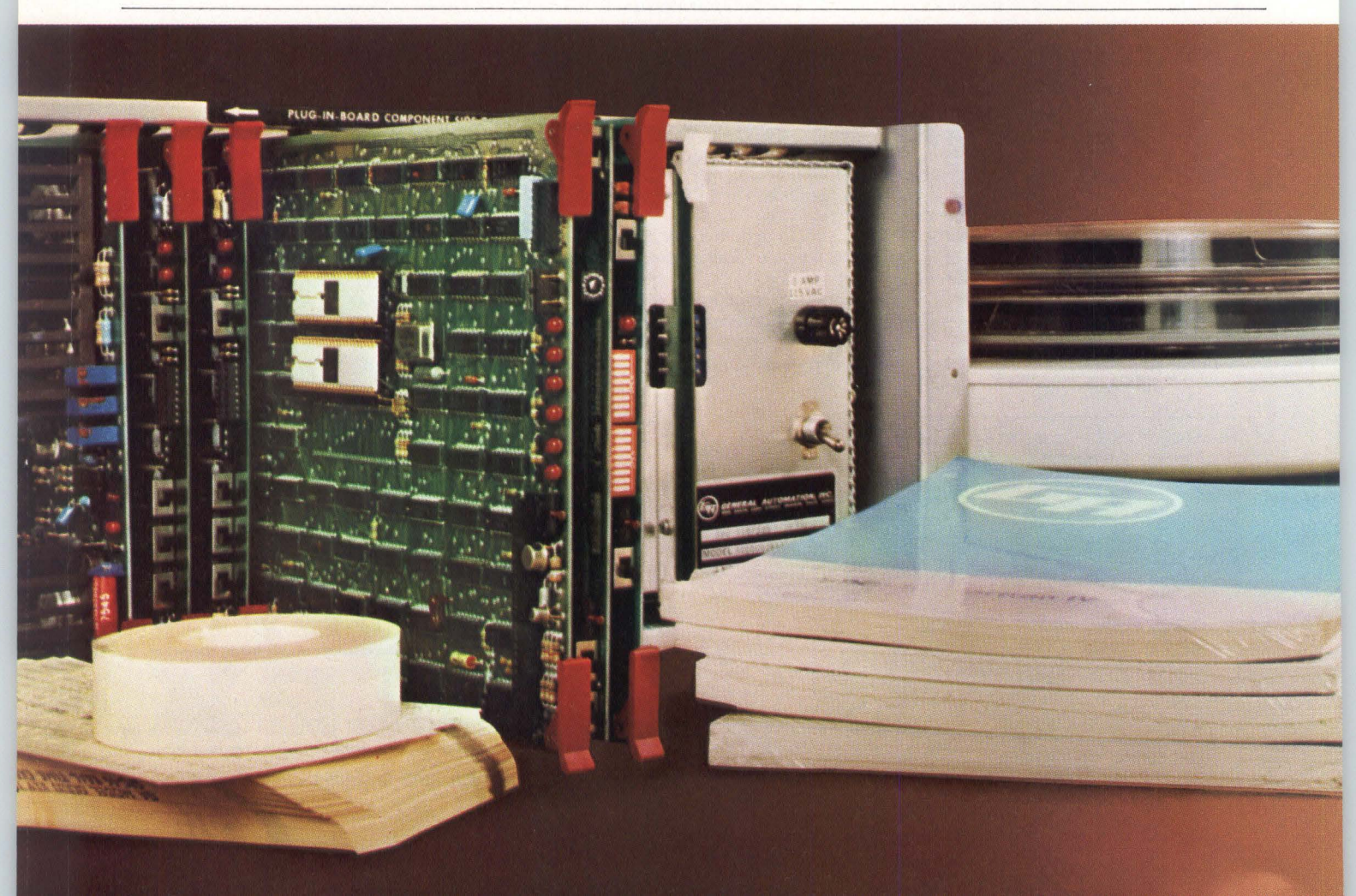
Initial step in using this process, regardless of application, is modeling the part to be depicted or

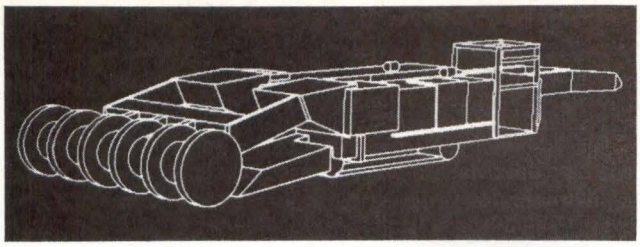


Three-dimensional model of wing strut assembled by SynthaVision computer-aided design process. Boeing's Computer Services Co will use process to model and analyze complex, solid aircraft components and systems



Three-dimensional model of an automotive wheel spindle. Mathematical input required for this computer construction can be used to calculate mass properties and perform stress analysis at fraction of time required by conventional methods





Line drawing of underground mining vehicle. U.S. Bureau of Mines will use process to simulate mining equipment and its lights and to verify that lighting meets required levels. It will also simulate machinery as if actually operating in a real mine

analyzed. The modeling technique is based on the theory that most solid structures, no matter how complex, can be broken down into simpler shapes. Using such geometric "primitives" as spheres, cones, and boxes, nearly any 3-dimensional object can be formed. There are now 11 primitives used in this process, but more are contemplated.

Boeing will use the process to model complex aircraft parts and systems. In addition to 3-dimensional shaded pictures, the process will produce line drawings as well as exploded and sectional views. It will also compute mass properties and interference calculations.

As a drafting tool it is expected to reduce the cost of many previously time consuming operations. For engineering analysis, the geometry of the mathematical model created can be used to determine volume, weight, center of gravity, and other mass properties, as well as provide data for stress analysis codes.

Three-dimensional input for interference calculations can be provided for operation of numerically-controlled machinery. Accuracy of a program can be checked before actual machining begins to be certain that parts to be machined will be handled properly. In addition, the realistic, shaded pictures produced by the process provide realistic views of nonexistent parts while they are still in the concept stage.

Another application for this process will be carried out by the U.S. Bureau of Mines in determining mine lighting levels. The system will create a 3-dimensional model of coal mining equipment and its lights and calculate the illumination levels of the simulated machinery as if it were actually operating in a real mine. The Mine Enforcement Safety Administration (MESA) will use the system to verify that mine lighting meets required levels.

In the past, manual methods have been used to create a life size model of the machinery, position the lights, and manually measure the illumination level over each point in a grid system superimposed on the mock-up of a mine face. MESA will be able to generate models of the mining machinery and its lighting, orient the lights on the equipment, simulate the mine face and the vehicle's position in the mine, and predict the lighting level. With the modeling system, a simulated machine and its lighting are expected to be analyzed in less than an hour, including a few minutes of computer time.

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DIGITAL CONTROL AND AUTOMATION SYSTEMS

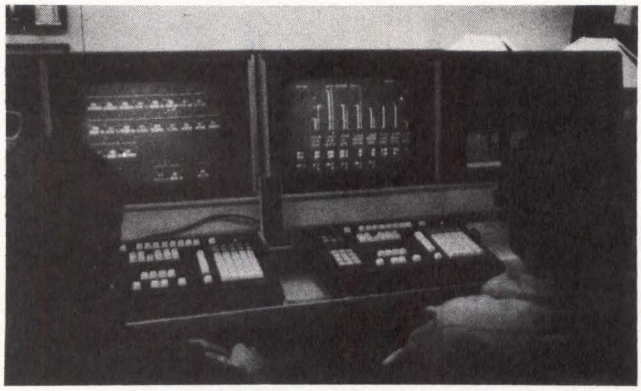
Microprocessor-Based Controllers in Alcohol Manufacturing Plant Maintain Process Flexibility

Process engineers constantly modify control schemes or change loop configurations to improve the control process. One of the practical methods has been to use direct digital control with a supervisory computer programmed to accept and carry out changes in tuning constants, setpoints, and alarm ranges.

Now, however, engineers at the Exxon Chemical Co U.S.A. Baton Rouge Chemical Plant can reconfigure controllers simply by use of pushbuttons at either a data entry panel or an operator station keyboard. Once loop functions are configured, they are locked into a protected core memory until the engineers want to modify them.

This capability results from installation of a TDC 2000 control system built by the Honeywell Process Control Div, 1100 Virginia Dr, Ft Washington, PA 19034. It is the first such equipment to go online at this complex, one of the largest alcohol manufacturing facilities in the U.S., and it is reported to have performed satisfactorily on 24-hr/day operations since startup. Incorporated are two operator-station CRT displays, 80 analog backup units, 39 trend recorders, and 10 remote-mounted control files, each with an associated data entry panel. CRT displays and associated keyboards form a single interface with the process, providing a centralized display of all variables in the alcohol manufacturing process.

Because microprocessor-based controllers in the system are completely self contained and not limited to being housed in the main control room, they are located in a separate compartment at the Baton Rouge facility. The system's "Data Hiway"—actually a single-conductor coaxial cable—links all control files to the CRT displays.



TDC 2000 control console in Baton Rouge facility of Exxon Chemical Co, U.S.A. Display at the left is overview showing status of approximately 80 process variables on recently expanded alcohol manufacturing unit. Display at right shows detailed information on particular group of eight variables. Operators can also call up single loops for closer monitoring and can adjust setpoints, ranges, and valve positions from keyboard

Although system controllers function normally under battery backup during a power outage, the CRTs lose their displays. In this event, program cassettes are reloaded and used to reprogram all displays for normal operator communication with the process after power is restored.

If the operator requires a view of the entire operation, he uses one of the station CRTs. The status of up to 288 process variables arranged in 36 groups of eight can be presented. If he wants a closer look—at a particular tower, for example—the operator can call up either a group display of eight variables, or look at a single loop by pushing a button on the keyboard. A display also can be called up which indicates the status of each controller on the Data Hiway.

The controller's internal self-exercising diagnostic program is performed every 0.33 s. This diagnostic check detects malfunctions and displays the nature and location of the fault on the CRT.

Circle 161 on Inquiry Card

DC&AS BRIEFS

Energy Management System Meets Federal Goal for Reducing Energy Consumption

GSA approval has been received for installation in the John W. McCormack Post Office and Federal Building in Boston, Mass of an energy management system that reportedly will meet President Carter's stated goal of reducing energy consumption in all Federal buildings by at least 20%. Predictions for this system—actually a full heating, ventilating, air conditioning (HVAC) control system—include a 20 to 30% cut in energy costs, but with no reduction in the comfort level. Improved air conditioning regulation during the summer months is expected to provide the greatest energy savings. In addition, the system will automatically shut off ventilating fans on specified floors in the event of a fire and will prevent elevators from stopping at "fire" floors.

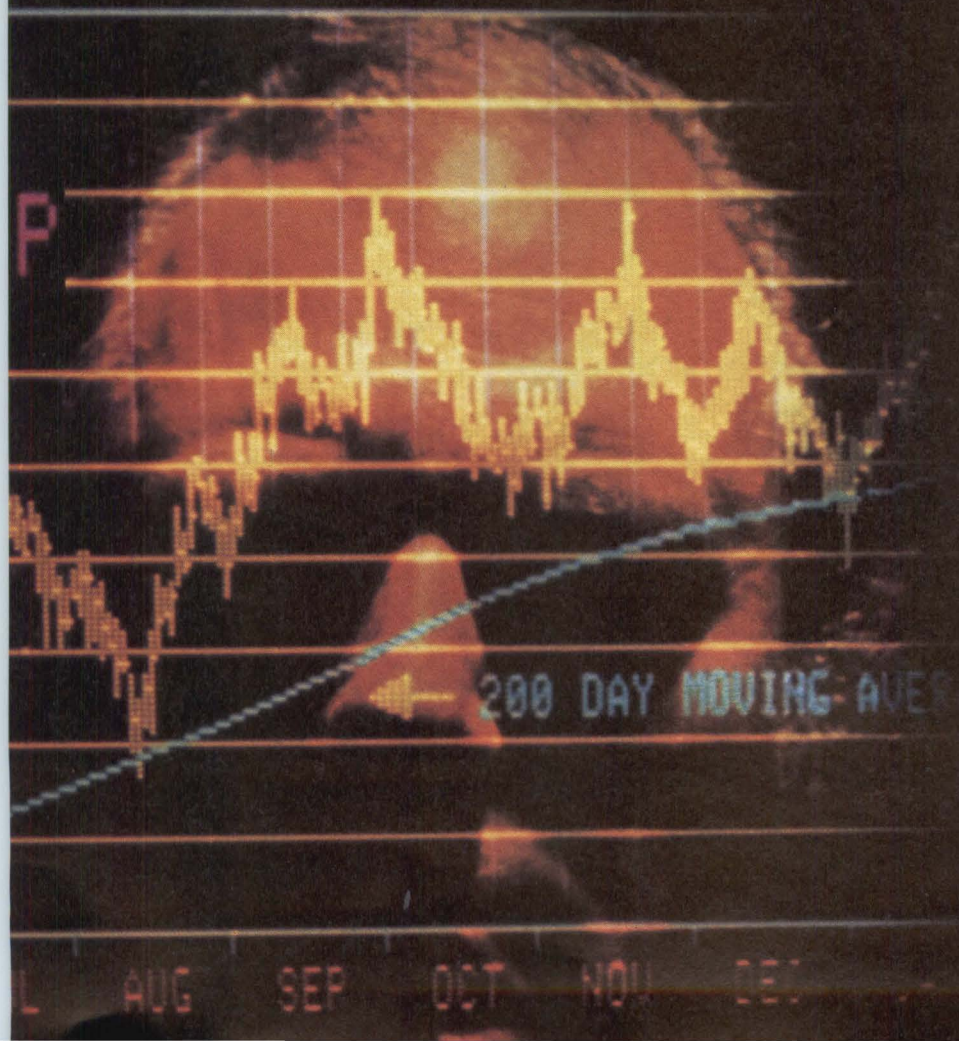
This configuration, the first to be installed in a Boston Federal building, will be made up of a master station and 18 remote terminals located throughout the vertically zoned, 22-story building. The master station will consist of a 16-bit Digital Equipment Corp PDP-11/04 microcomputer with 28k words of memory, dual floppy disc for mass storage, CRT, and printer. Data Signal Corp, 40-44 Hunt St, Watertown, MA 02172, designer of the system, has already installed the system and has scheduled startup for October of this year.

Whereas some HVAC control systems are effective only on new buildings since they must be installed during construction, this system was installed in Boston's longstanding main Post Office building. It ties together several existing, varied systems made by different companies and each with individual consoles. In the event of computer failure, the old mechanical systems can be returned to operation by throwing a switch.

Circle 162 on Inquiry Card

Ramtek's new MICROGRAPHIC™ terminal gives you color, intelligence, graphics, and alphanumerics at a price you can afford.

Color and smarts don't cost a lot anymore.



Here's great resolution and a bright, flicker-free display on a matrix of 512 elements by 256 lines in a terminal that's easy to program to your requirements.

No longer do you have to put up with poor resolution in economy-priced terminals. Ramtek gives you a combination of true graphics—such as vectors, conics, plots and bar charts—and high-speed alphanumerics with a high-resolution industrial-quality monitor. You can choose two sets of 8 colors for both graphics and alphanumerics. Dual and split screen capability too, with all the price/performance benefits of raster scan technology. And the independent alphanumeric refresh offers you single-character addressability within a visible matrix of 25 rows of 80 characters that are bright, crisp, sharp, and well defined. The refresh memory also allows selective erase, modification, and update.

The MICROGRAPHIC terminal is controlled by a powerful Z-80 microprocessor with up to 28K bytes of PROM and 16K bytes of RAM. Ramtek's control software gives you TTY compatibility and high-level graphic functions commanded by ASCII text strings. Choose from an extensive list of options such as additional serial I/O ports, alphanumeric overlays, programmable fonts, and packaged software.

Best of all, you'll find Ramtek gives you an affordable price, depending upon your individual requirements. Find out more by contacting us. We're Ramtek, 585 N. Mary Avenue, Sunnyvale CA 94086. In a hurry? Pick up the phone and call us. We'll tell you why you can afford color and smarts.

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CIRCLE 40 ON INQUIRY CARD

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SBC 80/10	X			X			$495
SBC 80/10A	X	or	X	X			$495
SBC 80/20-4	X	or	X			X	$825

Yesterday, we said that to break into a field somebody else had a lock on, we'd have to offer something extra.

Which we did, of course.

Our BLC 80/10.

Then it dawned on us that it was a mighty big jump from our 80/10 to the other guy's 80/20-4. That maybe you might not need to go that far.

So, now, in addition to our standard-setting 80/10, we're making and selling the BLC 80/11 and two new micro-computers that nobody else offers:

the BLC 80/12 and the BLC 80/14. All the advantages of which you can clearly see in the chart above.

Still more "oomph"

And, we're also introducing another little item. Another

or buy from the best.

SINGLE BOARD MICROCOMPUTER	EPROM/ROM CAPABILITY 2708/2308		2716/2316E	RAM CAPACITY 1K	2K	4K	1-9 UNIT PRICE
BLC 80/10	X			X			$445
BLC 80/11	X	or	X	X			$470
BLC 80/12	X	or	X		X		$495
BLC 80/14	X	or	X			X	$570

exclusive: a double-capacity BLC 8432 EPROM/ROM board. Mind you, that's 32K, at 10% less than the other guy's 16K board!

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☐ BLC 80/10
☐ BLC 80/11, 80/12, 80/14
☐ 16K BLC 416, 32K BLC 8432
☐ Hang the return mail. Have a salesman call me immediately.

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DC&AS BRIEFS

Weight/Volume Batch Controller Handles Up to 15 Ingredients

Quantobatch 4600 measures and controls flow of batch volumes of material under microprocessor control. Model /1 handles one to five ingredients; /2 handles up to 15. Both repeat batching cycles automatically. Materials such as feed, grain, and chemicals are processed on both weight and volume requirements.

Announced by the Streeteramet Div of Mangood Corp, 155 Wicks St, Grayslake, IL 60030, the controllers have three standard modes of operation: auto sequence for totally automatic formula dispensing in the order and quantities selected; auto single cycle for similar operation with sequence stops at the end of each ingredient dispersal; and manual mode for all manually controlled operations. Both full and reduced flow feeding rates are available, and incremental dumping of completed mixes for drum or bag filling or similar applications can be included.

Builtin test functions enable plant personnel to pinpoint trouble areas and minimize maintenance. A special alarm indicates system errors or power failures. Battery backup protects formula data in the case of power interruption. Printers, remote displays, and other options are available.

Circle 163 on Inquiry Card

Microprocessor-Based Controller Readily Programmable for Process Industries Applications

A standalone unit that the manufacturer states "is the industry's first microprocessor-based, multiloop programmable process controller with a high level language . . . designed specifically for the process engineer and the process industries" has been announced by Reliance Electric, Controls Div, 25001 Tungsten Rd, Cleveland, OH 44117. A basic UDAC (user digital analog controller) can control up to 64 analog loops and as many as 128 digital inputs and/or outputs. An expanded version can handle up to 192 analog and 384 digital I/Os.

A microprocessor card, memory card, and one to four analog or digital I/O cards fit into slots on the basic unit. Up to two additional 6-card expansion units can be added. The microprocessor has 16-bit word length, 2-MHz clock frequency, and 10-μs typical instruction time; on-card memory contains 1024 words of P/ROM and 512 words of static RAM. Communication rates to this card are 110 to 9600 baud.

SPEAK EASY, a high level English-based controller programming language, and user application programs are stored on 16-bit, 8k-word core or 16-bit, 8k or 16k MOS memory cards. Analog I/O cards handle 16 single-ended or eight differential multiplexed inputs with 12-bit resolution and 0.025% accuracy; outputs can be 4, 8, 12, or 16 with 8-bit resolution and 0.4% accuracy. Digital I/O cards have 32 inputs and 32 outputs.

Circle 164 on Inquiry Card

Energy Management System Available for Existing Small or Medium Sized Buildings

Sunkeeper Controller—a microprocessor-based, user-programmable energy management system for small to medium sized office buildings—controls central functions such as heating, lighting, ventilating, and air conditioning. It interfaces to existing electrical systems and handles 64 analog and digital inputs and 32 outputs. Digital inputs and outputs are 24 V, and analog inputs are 0 to 5 Vdc or from thermistor sensors. Andover Control Corp, PO Box 34, Andover, MA 01810 claims 15 to 30% reductions in energy costs will result from application of the system.

Circle 165 on Inquiry Card

Master and Satellite Microprocessors Interface in Chromatograph System

Petroleum, chemical, and petrochemical refinery applications are targets for a microprocessor-controlled process chromatograph system announced by Beckman Instruments, Inc, Process Instruments Div, PO Box 3100, Fullerton, CA 92634. Each model 6750 chromatograph system controls up to six chromatograph analyzers, each capable of independent operation with its own microprocessor.

Field-based analyzers store complete operating tables for each analysis. Peak values are digitized, integrated, and scaled by analyzer microprocessors for transmission to the system's processor which performs calculations, generates reports at the intervals and in the formats specified by the user, performs alarm analyses, and controls maintenance procedures.

An interactive data entry and display terminal allows English language operator communication. Programmed step-by-step instructions guide the operator through system startup, day-to-day operations, and maintenance procedures. A builtin digital voltmeter permits important analyzer voltages to be remotely displayed for diagnostic purposes.

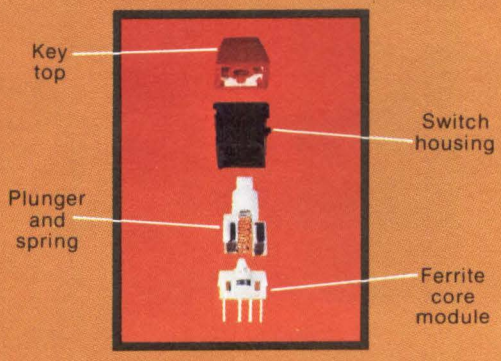
Analyzers may be remotely located up to 2000 ft (610 m) from the programmer. Information exchange takes place over a 5-wire data bus. Communication on the bus and throughout the system is in ASCII. The system provides 32 programmable analog outputs. RS-232-C ports allow communication with host computers and peripheral devices.

Circle 166 on Inquiry Card

Cost efficiency you can put your finger on . . . CORTRON® SOLID STATE KEYBOARDS

Get your hands on a CORTRON Solid State Keyboard, and you'll soon find out why you can't judge all keyboards on initial price alone.

It's after installation that cost efficiency becomes most important. In life expectancy, ability to endure extreme environments, high speed operation without "misses," accuracy, downtime caused by beverage spillages, reliability, serviceability and human engineered features. That's where a CORTRON Solid State Keyboard really pays off.



Unique contactless key switch makes the difference. Utilizing ferrite core switching technology, the CORTRON Key Switch is mechanically simple (only 4 basic parts!) and has an ultra reliable 100 million cycle life test rating. CORTRON Keyboard Professionals can translate what this can mean to you in cost efficiency terms of MTBF (mean time before failure). CORTRON has actual customer experience of MTBF in excess of 40,000 hours.

They'll also explain other advantages you'll gain over competitive technologies such as Hall effect, reed switch, and capacitive switching. All in all, you'll find the CORTRON Key Switch offers unusual built-in protection against costly service calls and the hardship of downtime.

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Nothing left to chance. CORTRON solid state keyboard materials, components, subassemblies, and final assembly are 100% inspected and tested to assure your specifications are met with plenty of room to spare.

These are just a few of the cost efficiency benefits CORTRON offers you and your customers.

Cost efficiency you can put your finger on. For a greater insight into the cost efficiencies attainable with a CORTRON Solid State Keyboard, write or call for details: CORTRON, A Division of Illinois Tool Works Inc., 6601 West Irving Park Road, Chicago, Illinois 60634. Phone (312) 282-4040. TWX 910-221-0275. Toll free line: 800-621-2605.

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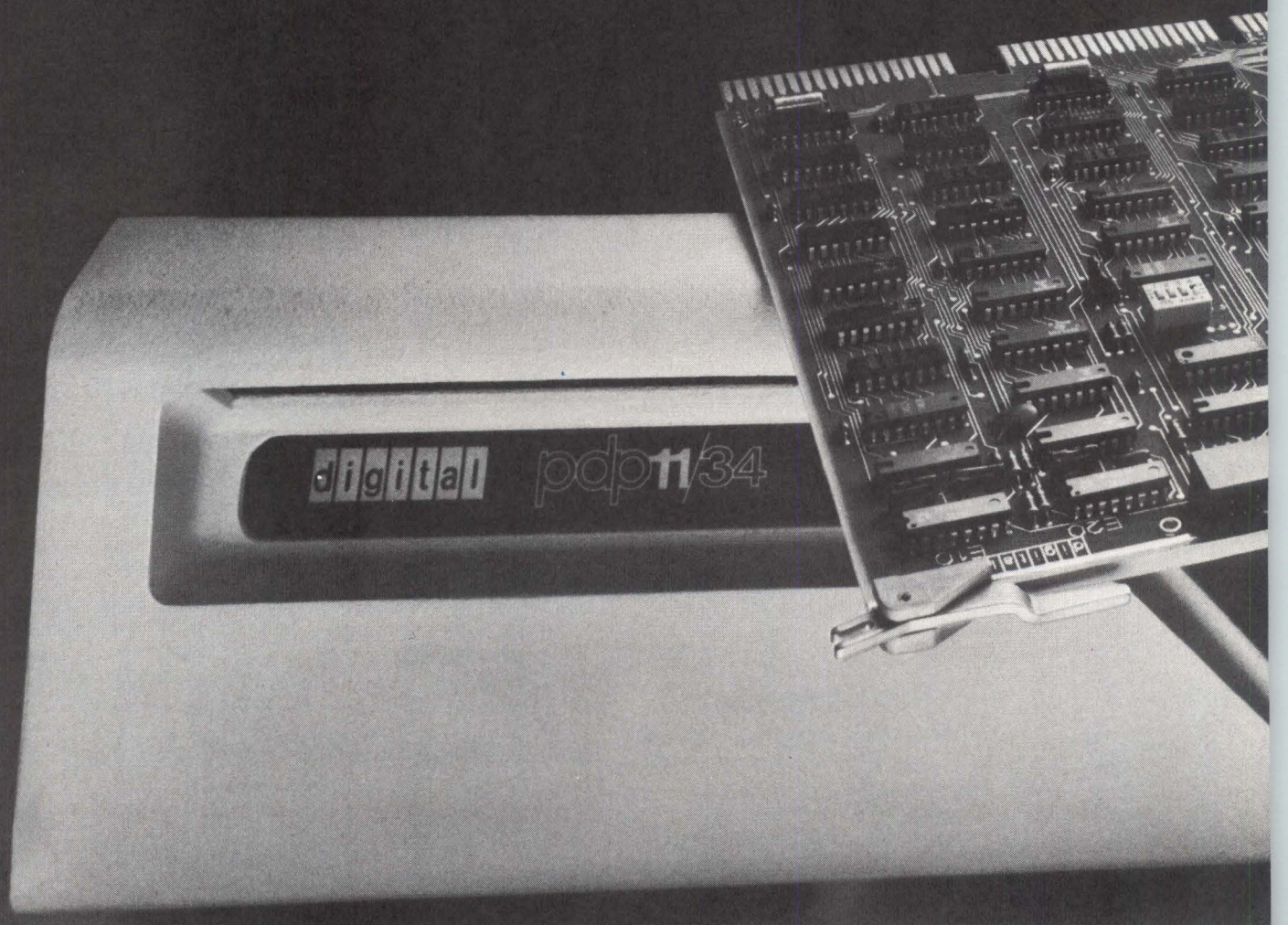

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CIRCLE 42 ON INQUIRY CARD

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The flat, smooth, front panel surface permits unlimited choice of graphics. Functions may be grouped by color, with 480 colors available. Thirty choices of type style and size. And whatever visual symbols meet your specific needs.

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- All switches and graphics on a .075″ thin panel.
- Flat, spill-proof surface wipes clean.
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CIRCLE 43 ON INQUIRY CARD

DESIGN MOTIVATIONS FOR MULTIPLE PROCESSOR MICROCOMPUTER SYSTEMS

Design decision factors involved in developing multiple processor microcomputer systems include means of minimizing contention for system bus utilization. System applications detail the appropriate hardware and software considerations as related to single-board computers in a multimaster bus structure

George Adams and Thomas Rolander* Intel Corporation, Santa Clara, California

Large-scale integrated circuit technology has reduced the cost of central processors to such a low level that the previously avoided concept of applying multiple processors to meet system performance requirements has now become an attractive and viable alternative. Several key benefits accrue from such an approach. In addition to enhanced system performance (throughput), improved system reliability, and improved system realtime response, modular system expansion capabilities may be realized. Although designing such systems "from scratch" with microprocessor component families can be a complex system design task with many subtle pitfalls which can inhibit efficient system operation, the advent of second generation single-board computers, such as the Intel® SBC 80/05 and 80/20, has allowed multiple processor microcomputer systems to become off-the-shelf products.

Motivation and Design Concepts

Discussion of the benefits of multiple processor structures in system applications will provide an understanding of the motivation for this implementation approach in system design. A primary objective addressed through multiple processor approaches is enhanced system performance and throughput. Enhanced performance is achieved through partitioning of overall system functions into tasks that each of several processors can handle individually.

In general, as the number of individual tasks any given processor must handle is reduced, that processor's response time to new requests for service will be reduced. A well planned multiple processor bus structure will allow new processors to be added to the system in modular fashion. When new system functions (ie, more peripherals) are added, more processing power can be applied to handle them without impacting existing processor (master) task partitioning.

As used here, a "master" is any element existing on the system bus that may take control of the bus (ie, assert address and control lines). Typical examples include processors and direct memory access (DMA) controllers that address memory and input/output (I/O) locations resident on the bus. "Slave" elements include passive functions on the bus, such as memory or non-DMA I/O interfaces. Note that although slaves may possess intelli-

*Mr. Rolander is now with Dharma Systems, San Jose, Calif.

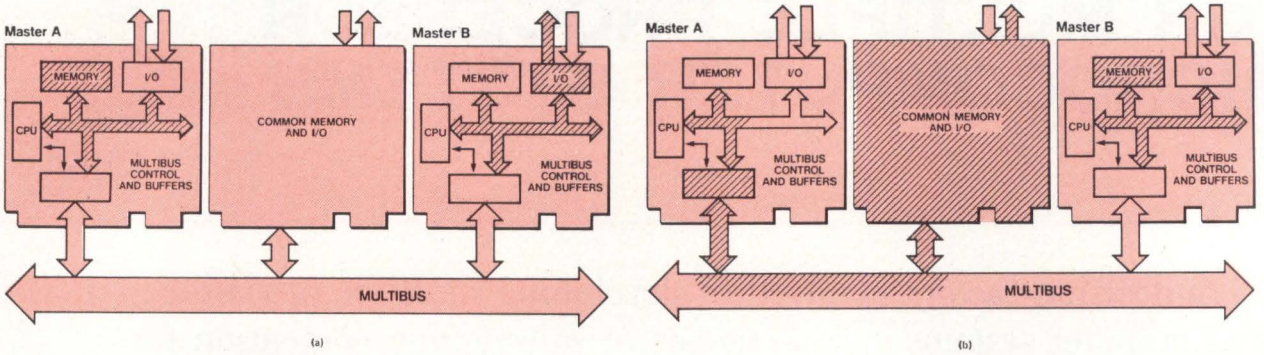

Fig 1 Multiple processor bus structure. Dual onboard/offboard structure of MULTIBUS allows each master to use its own memory and I/O without utilizing common system bus (a). Only when a master requires access to common memory or I/O does it use the bus (b). Note that other masters may continue onboard operations simultaneously

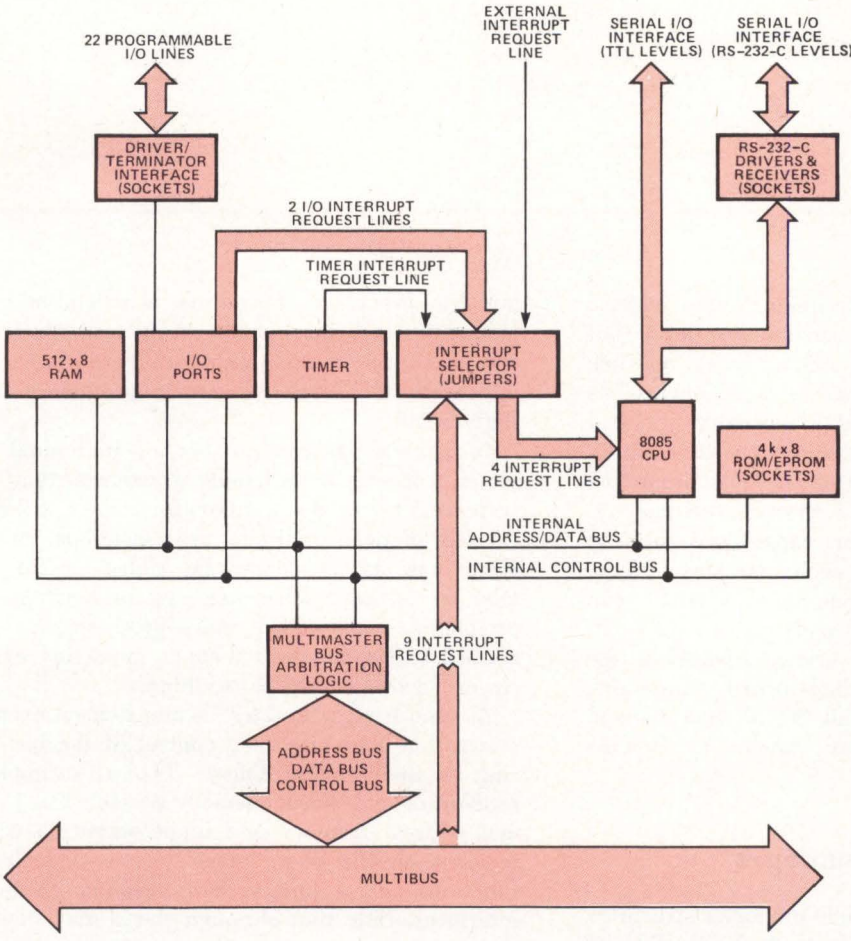

Fig 2 SBC 80/05 block diagram. SBC 80/05 is a full microcomputer on a single PC board. It provides 8085 CPU plus RAM for program or data storage, EPROM/ROM for program storage, interval timer, programmable parallel I/O (22 lines), serial I/O, and full MULTIBUS multimaster control logic

gence (eg, an onboard processor), they are not bus "masters" unless they can control the system bus.

Hardware Considerations

Hardware considerations must be thoroughly evaluated in any multiple processor bus structure. These factors are described in detail around a specific implementation of such a structure, the Intel® MULTIBUS™, which supports multiple processor systems with its multi-master bus structure.

Bus Architecture

One architectural option open to the system designer is that of a multiple master/single bus structure. Under this partitioning, every master utilizes the common bus data path to fetch instructions or data from memory, read data from input devices, or write data to output devices or memory. Therefore, the common system bus rapidly becomes the bottleneck for overall system throughput, and fast DMA transfers can easily approach the full bandwidth of the bus during block transfers so that all other masters must idle for extended periods. Such performance constraints can severely limit total system performance.

System bus utilization may be minimized through implementation of an alternate dual-bus structure as shown in Fig 1. Each processor-based master within the system retains its own local memory and I/O that it utilizes for most operations. Such local operations occur totally on the individual board and do not require the system bus. This greatly reduces the service request frequency by each master requiring use of the system bus. Such a dual-bus structure is implemented on the SBC 80/05 and 80/20 single-board computers, as shown in Figs 2 and 3, respectively, with the multi-master system bus (MULTIBUS).[1,2]

Access to the system bus is requested only when a global (resident on the bus and accessible by multiple masters) memory location or I/O device is referenced during an instruction execution cycle. Local/global (onboard/offboard) distinction is defined through the value of the physical address referenced. If it lies within the address range of onboard memory or I/O, no bus request is made. Only when the address references a global

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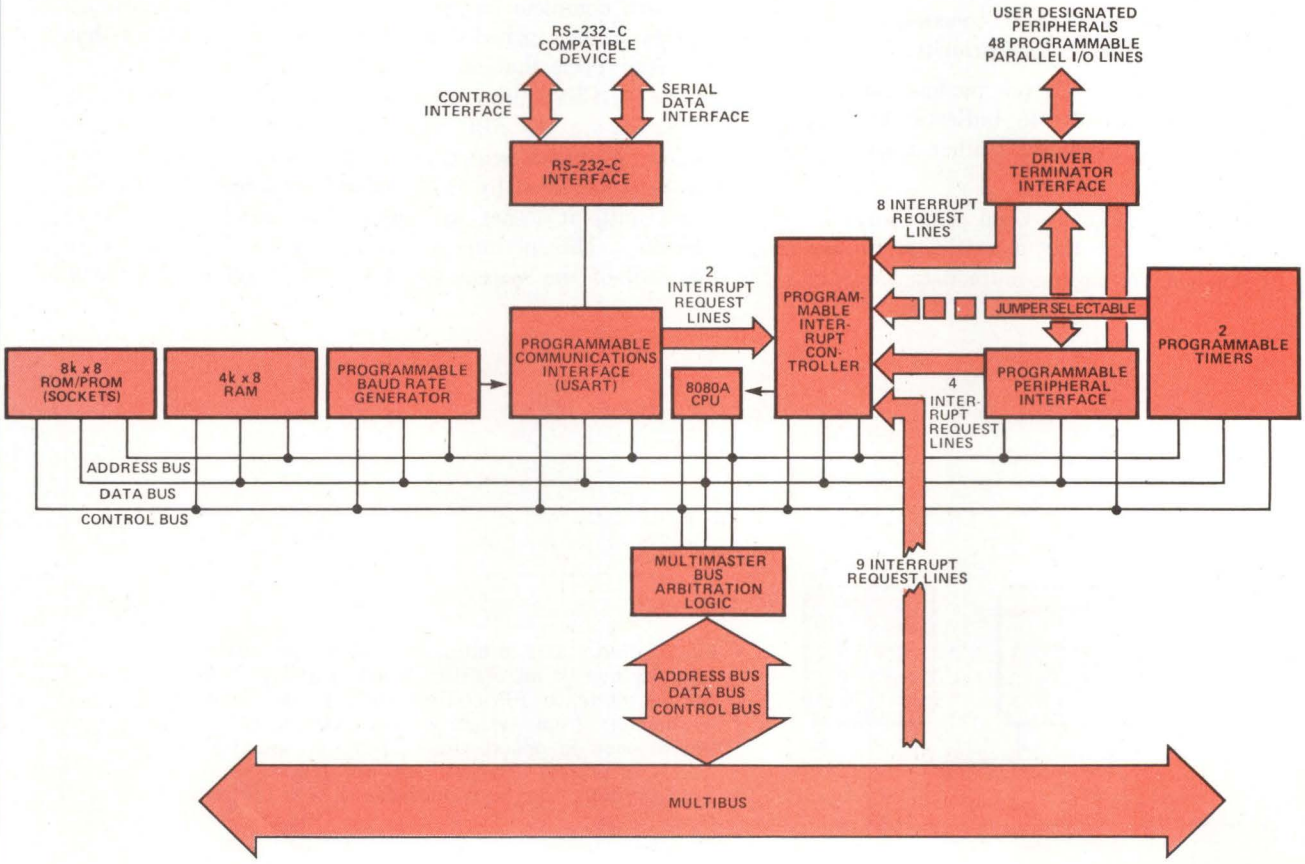

Fig 3 SBC 80/20-4 block diagram. SBC 80/20-4, also a full microcomputer on a single PC board, provides 8080A-2 CPU, 4k bytes of RAM, up to 8k bytes of EPROM/ROM, 48 programmable I/O lines, three interval timers, full RS-232-C serial port, 8-level priority interrupt logic, and MULTIBUS multimaster control logic

memory or I/O location, is a system bus request initiated. If no other master is currently utilizing the bus, this "new" master will be granted access immediately. However, this new master must wait if another master is currently utilizing the system bus. It continues to monitor the status of the system bus to determine when its current cycle may be completed. Thus, the MULTIBUS must provide a method for masters to determine whether or not another master is currently utilizing it.

Other masters may also simultaneously request the system bus. Arbitration must then be performed to resolve this multiple contention for the system bus. The MULTIBUS structure provides this arbitration in one of two techniques: serial (daisy chain) or parallel (encoded). The structure consists of four control lines that are synchronized by the common bus clock. These four control lines and the bus clock are active low. This is represented by the slash (/) character after each signal mnemonic. Control lines are as follows:

Bus Clock (BCLK/) —The negative edge of BCLK/ is used to synchronize bus arbitration. BCLK/ may be asynchronous to all CPU clocks, and it has a 100-ns minimum period. BCLK/ may be slowed, stopped, or single-stepped for debugging.

Bus Priority In Signal (BPRN/)—Indicates to a particular master that no higher priority master is requesting use of the system bus.

Bus Priority Out Signal (BPRO/)—Used with serial bus priority resolution scheme. BPRO/ is passed to BPRN/ input of master with next lower bus priority.

Bus Busy Signal (BUSY/)—Driven by bus master currently in control of MULTIBUS to indicate that bus is currently in use. BUSY/prevents all other masters from gaining control of bus.

Bus Request Signal (BREQ/)—Used with parallel bus priority network to indicate that a particular master requires use of the bus for one or more data transfers.

Serial (Daisy-Chain) Bus Arbitration

In a serially arbitrated MULTIBUS system (Fig 4) requests for system bus utilization are ordered by priority on the basis of bus location. Each master on the bus notifies the next lower priority master when it needs to use the bus for a data transfer, and it monitors the bus request status of the next higher priority master. Thus the masters pass bus requests along from one to the next in a daisy-chain fashion.

The highest priority master (Master 1) in the system will always receive access to the system bus when it requires it. There is no higher priority master to inhibit its bus requests, and its bus priority input line (BPRN/) is thus permanently enabled.

Masters operate asynchronously on the MULTIBUS. A master may thus be in the middle of a bus operation when a higher priority master requests the bus. Obviously, interruption of such an in-process cycle must not be allowed. The mechanism for avoiding such erroneous operation is the BUSY/ line. Upon being notified that access to the bus is possible, the master examines BUSY/. If this control line is inactive, the master will assert it, and complete its bus operation. If BUSY/ is already active, another master is currently using the bus. In this case, the master will examine BUSY/ upon every falling edge of BCLK/, typically once every 100 ns, until it becomes inactive. When BUSY/returns to its inactive state, the master will assert it, then complete its operation. The BUSY/line then inhibits higher priority masters from destroying a bus transfer cycle that may be already in progress.

The BUSY/ line is also controlled by a bus lock function on the SBC 80/05 and 80/20. This function allows a master, which currently has control of the bus, to retain control by independently asserting the BUSY/ line until it issues an unlock command that releases BUSY/. This permits a bus master to obtain exclusive control of the system bus for critical system functions,

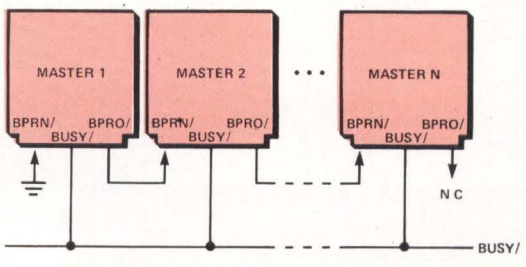

Fig 4 Serial bus arbitration. When any master requires use of MULTIBUS in serial (daisy-chain) priority mode, its BPRO/ line inhibits lower priority masters from system bus utilization. BUSY/ line is used to ensure that in-process operations of lower priority masters are not destroyed by asynchronous bus requests of higher priority masters

such as high speed memory or I/O data transfers and critical read-modify-write operations. With BUSY/ asserted in this way, all other masters will find the bus "in use" when they attempt to access it. Whereas system bus transfers normally take place on an interleaved basis (bus arbitration performed for each cycle), this bus lock function permits fast multiple-word transfers, when needed.

Two basic parameters determine the number of masters that can coexist on the system bus in serial bus arbitration mode. These are the BCLK/ cycle time and the BPRN/ to BPRO/ propagation delay of bus masters. Masters may be added to a system as long as the cumulative BPRN/ to BPRO/ propagation delay is such that the lowest priority master will always have its BPRN/ line driven inactive before the next BCLK/ falling edge after the highest priority master requests the bus. This worst-case timing condition is met as long as the following relationship is satisfied.

$$\sum_{i=1}^{N-1} (t_{BPRN-BPRO})_i < t_{BCLK} - t_{sh}$$

where

$(t_{BPRN-BPRO})_i$ = Propagation delay for master i
t_{BCLK} = Bus clock (BCLK) cycle time (period)
t_{sh} = Allowance for bus setup and hold times
N = Number of bus masters

Using serial bus arbitration and SBC 80 onboard clocks, up to three masters may coexist on the system bus. This number can easily be extended, if desired, by generating a BCLK with a longer cycle. The SBC 80/05 and 80/20 provide a jumper option which allows the onboard BCLK/ to be disabled. This allows the system designer to generate BCLK/ externally.

Parallel (Hardware-Encoded) Bus Arbitration

The parallel bus arbitration technique resolves system bus master priorities using external hardware. The parallel multimaster control line (BREQ/) comes into force in this case. Each master asserts BREQ/ when it requires access to the system bus. These lines are fed to a 2-chip parallel priority network. As with serial priority resolution, BPRN/ acts as the bus access enable input to each master. As Fig 5 illustrates, up to eight master priority levels are encoded by a 74148 priority encoder to a 3-bit code representing the highest priority master currently requesting the system bus. This code drives the 8205 3-to-8 decoder which asserts the proper BPRN/ line low to grant bus access to the highest priority master. The 74148/8205 propagation delay is less than 40 ns, easily fast enough to allow eight masters to coexist in this configuration utilizing a BCLK/ with a 100-ns period.

Systems requiring up to 16 masters may implement bus arbitration by utilizing two 74148 priority encoders and two 8205 decoders to provide a 16-level hardware priority network. The actual number of bus masters feasible on the system bus will also depend on bus drive/loading considerations. Even under this consideration, systems containing up to 16 masters are feasible.

Thus, single-board computer masters, in conjunction with the MULTIBUS control structure, provide off-the-shelf hardware solutions for the development of efficient multiple processor microcomputer systems. In addition to this hardware capability, the system designer needs to consider several software design issues.

Software Considerations

Several software operations, such as mutual exclusion, communication, and synchronization, are essential to proper multiple processor system operation. The MULTIBUS/SBC 80 functions that enable these software operations are examined.

Mutual Exclusion

In a multiple processor microcomputer system, there are

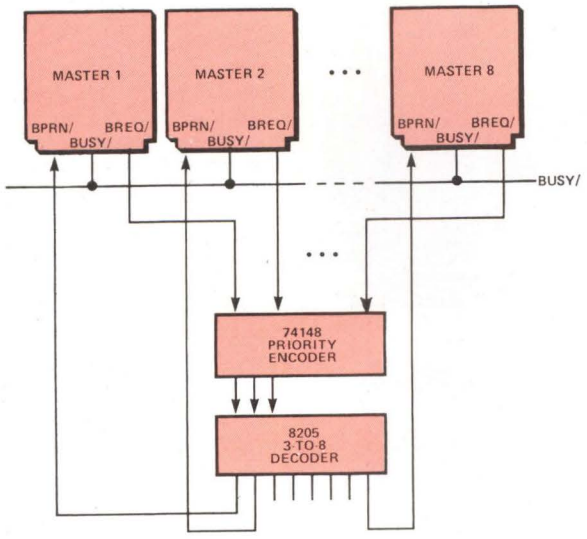

Fig 5 Parallel bus arbitration. Under parallel bus arbitration structure, multiple requests for access to the MULTIBUS are determined by 2-chip hardware priority network. When simultaneous multiple bus requests occur, only highest priority master has its bus grant (BPRN/) line asserted. BUSY/ line inhibits other masters from interfering with system bus cycles in progress

usually many resources that are shared by the processors. Such shared resources include common memory and peripherals. A properly functioning system must provide a mechanism to guarantee that asynchronous access to those resources is controlled in order to protect data from simultaneous change by two or more processors. Thus, some form of mutual exclusion must be provided to enable one processor to lock out access of a shared resource by other processors when it is in a critical section. A critical section is a code segment that once begun must complete execution before it, or another critical section that accesses the same shared resource, can be executed.

A Boolean variable can be used to indicate whether a processor is currently in a particular critical section (true) or not (false). Testing and setting this variable also presents a critical section. This function must be performed as a single indivisible operation; if it is not, two or more processors may test the variable simultaneously and then each set it, allowing them to enter the critical section at the same time. Such simultaneous entry would destroy the integrity of data and control parameters in global memory or cause erroneous double initialization of a global peripheral controller.

Mutual exclusion can be implemented as a software function alone, as described by Dijkstra[4], for n processors operating in parallel. The SBC 80/05 and 80/20 bus lock function mentioned earlier provides a means for using program control to simplify mutual exclusion. While the system bus is locked, the master can perform the indivisible test and set operation on the Boolean variable used to control access to a critical section without intervention from other masters.

Communication

Communication is an essential function that allows a program executing on one processor to send or receive data from a program executing on another processor. Typically, two processors communicate through buffer storage in common memory. One program, called a producer, adds data to buffer storage; another, called a consumer, removes information from buffer storage.

In a typical application, one master may produce buffers of data that are to be consumed by a program executing on another master that services an output device. Communication through buffer storage requires the operations of adding to and taking from buffers. These operations constitute critical sections that can be controlled by providing mutual exclusion around the buffer manipulation operations.

Synchronization

At times there is a need for one master to send a synchronization signal to another. In a sense, synchronization is a special case of communication during which no data is transferred. Rather, the act of signaling is used to "wake up" a program executing on another master. A program may "sleep," by waiting for a synchronizing signal, until it receives a wake-up signal that enables it to continue execution. Manipulation of synchronization signals requires mutual exclusion.

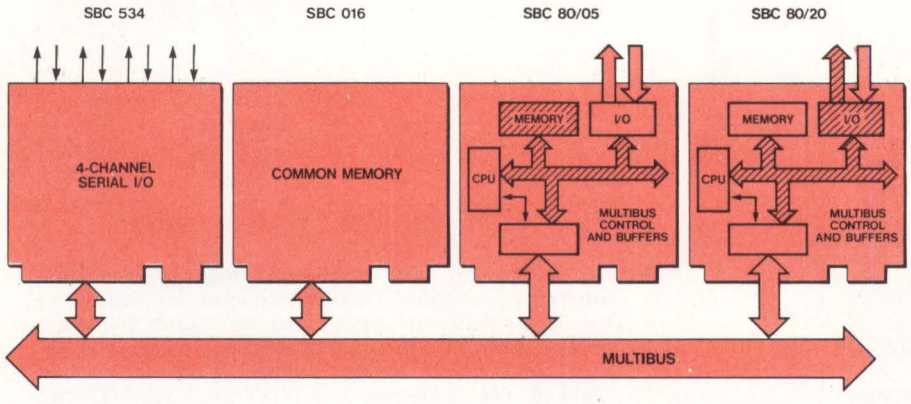

Fig 6 Multiple processor communication application. Multiple processors may be utilized to increase throughput in system requiring several high speed serial channels. SBC 80/05 single-board computer controls four RS-232-C or 20-mA serial channels interfaced to system through SBC 534 communication expansion board. Second single board computer (SBC 80/20) retrieves data records constructed by SBC 80/05 and performs further processing

System Initialization

In a microcomputer system that has multiple processors sharing a common system bus, a system initialization mechanism must be designed to set up the variables that control access to the shared resources. All single-board computers on the MULTIBUS begin execution simultaneously following a system reset. The bus lock function of the computers can be used by one specifically designated master to lock the bus immediately upon system reset and to perform system initialization for common resources before any other master attempts to access them. Since a locked bus has no effect on a single-board computer that is executing out of its local memory and using its local I/O, normal initialization by each processor can proceed while the shared resource initialization takes place.

Multiprocessor Applications

Two applications that are well suited to multiple processor microcomputer systems are examined. The first provides increased throughput, and the second allows shared resources.

Increased Throughput

Consider a system that is controlling multiple high speed serial communication channels in addition to other data processing activities. In this case, multiple processors may be utilized to increase system throughput. Such a system with four full-duplex serial channels operating at 4800 baud could produce interrupts every 250 μs. Interrupts at that frequency in a single master system would leave little time for other processing activities. In a multiple processor approach, one processor can be used to handle the interrupts from the serial channels, accumulate data into records, and then provide those records to another processor by placing them in common memory. The second processor is not burdened with the overhead of handling each character on an interrupt-driven basis, instead it is sent entire records of data available for further processing.

As shown in Fig 6, this application can be handled on the MULTIBUS with four boards. The SBC 80/05 single-board computer is used to service the communication board and prepare the data records. A 4-channel serial communication board (SBC 534) is used to provide the hardware interface for four serial communication channels. The SBC 80/20 single-board computer is used to process data records prepared by the SBC 80/05. Common memory is provided by the SBC 016 16k random-access memory (RAM).

Application of multiple processors to this problem requires communication through buffer storage. Two primitive operations, introduced by Dijkstra[4], can be used to simplify the communication and synchronization between the masters. These primitives, designated P and V, operate on non-negative integer variables called

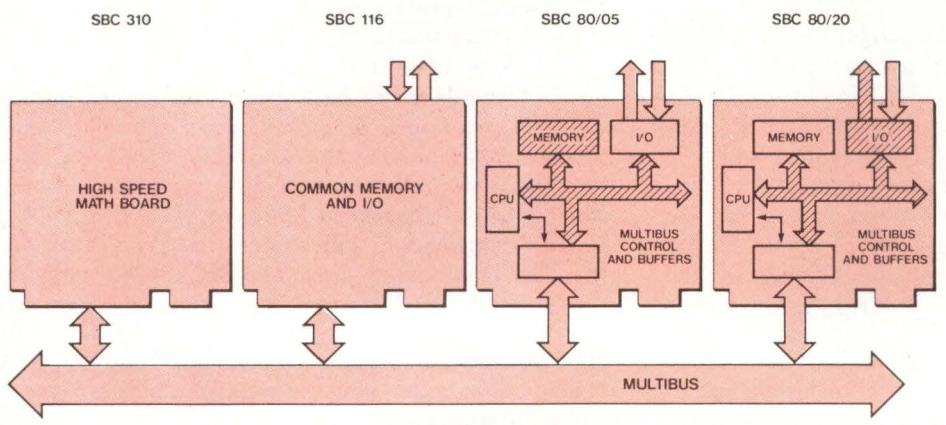

Fig 7 Multiple processor shared-resource application. MULTIBUS multiple processor structure allows two independent single-board computers to share common system resource, such as an SBC 310 high speed math board, to perform floating point operations

semaphores. The V procedure increments the semaphore (S) in a single indivisible operation. To make certain that fetch, increment, and store are not interrupted by another processor, the bus is locked during the operation.

Procedures for P and V primitive operations can be implemented in PL/M[6] as follows:

```
V:
  PROCEDURE (S$ADR);
  DECLARE S BASED S$ADR BYTE;
    OUTPUT(BUS$LOCK) = LOCK;          /* Lock MULTIBUS */
    S = S+1;                          /* Increment semaphore */
    OUTPUT(BUS$LOCK) = UNLOCK;        /* Unlock MULTIBUS */
END V;
```

The P procedure loops in a busy wait until S is greater than zero, at which time it decrements S. The act of fetching, testing, decrementing, and storing S is also an indivisible operation. Note that if several masters with different speeds are in a busy wait on the same semaphore, the solution presented may not be "fair" to the lower speed processor; that is, the lower speed processor would test the semaphore less frequently, resulting in an unfair advantage for higher speed processors.

Implementation of a procedure for the P primitive is shown in the following PL/M code.

```
P:
  PROCEDURE(S$ADR);
  DECLARE S BASED S$ADR BYTE;
    DO FOREVER;
      IF S > 0 THEN                   /* Test semaphore */
      DO;
        OUTPUT(BUS$LOCK) = LOCK;      /* Lock MULTIBUS */
        IF S > 0 THEN                 /* Retest semaphore */
       -DO;
          S = S-1;                    /* Decrement semaphore */
          OUTPUT(BUS$LOCK) = UNLOCK;  /* Unlock MULTIBUS */
          RETURN;                     /* Exit from P procedure */
        END;
        OUTPUT(BUS$LOCK) = UNLOCK;    /* Unlock MULTIBUS */
      END;                            /* and continue testing */
    END;
END P;
```

It is important to observe in the program listing that S is tested prior to issuing a bus lock. This initial test avoids continuous locking and unlocking of the system bus while looping in a busy wait. The second test is required because another processor could also have found S greater than zero and tried to enter the critical section at the same time.

With the P and V operations, semaphores can be used as resource counters in the buffer manipulation required for communication between the SBC 80/05 and 80/20. For example, a consumer program can use the P operation to decrement the number of full buffers and a V operation to increment the number of empty buffers. In a similar fashion, a producer program can use the P operation to decrement the number of empty buffers and a V operation to increment the number of full buffers. In addition to full and empty buffer counters, it is necessary to maintain linked lists pointing to actual full and empty buffers. A semaphore can be used to provide mutual exclusion around the manipulation of the linked lists. In the example that follows, three variables (FULL, EMPTY, and SEMA) are used to implement these functions. The two PL/M programs illustrate consumer and producer code segments, respectively. Note that the consumer performs initialization because it accesses the semaphores prior to the producer.

```
CONSUMER:
  DECLARE EMPTY BYTE EXTERNAL;        /* Number of empty buffers */
          FULL BYTE EXTERNAL;         /* Number of full buffers */
          SEMA BYTE EXTERNAL;         /* Binary semaphore */
    OUTPUT(BUS$LOCK) = LOCK;          /* Lock MULTIBUS */
    EMPTY = NUMB$BUFFERS;             /* Initialize semaphores */
    FULL = 0;
    SEMA = 1;
    OUTPUT(BUS$LOCK) = UNLOCK;        /* Unlock MULTIBUS */
    DO FOREVER;
      CALL P(FULL);                   /* Decrement full buffer */
      CALL P(SEMA);                   /*  semaphore */
                                      /* Decrement mutual exclusion */
                                      /*  semaphore */
      . . .
      . . .
      (Take data from buffer and
       place it in local memory,
       move buffer from full to
       empty linked list)
      . . .
      . . .
      CALL V(SEMA);                   /* Increment mutual exclusion */
      CALL V(EMPTY);                  /*  semaphore */
                                      /* Increment empty buffer */
      . . .                           /*  semaphore */
      . . .
      (Process the data)
      . . .
      . . .
    END;
END CONSUMER;

PRODUCER:
  DECLARE (EMPTY, FULL, SEMA) BYTE EXTERNAL;
  DO FOREVER;
    . . .
    . . .
    (Prepare data in local
     memory)
    . . .
    . . .
    CALL P(EMPTY);                    /* Decrement empty buffer semaphore */
    CALL P(SEMA);                     /* Decrement mutual exclusion */
                                      /*  semaphore */
    . . .
    . . .
    (Place data in a buffer,
     move buffer from empty
     to full linked list)
    . . .
    . . .
    CALL V(SEMA);                     /* Increment mutual exclusion */
    CALL V(FULL);                     /*  semaphore */
                                      /* Increment full buffer semaphore */
  END;
END PRODUCER;
```

Shared Resources

Another typical application for a multiple processor microcomputer system would be to allow sharing of a resource by two processors. For example, consider two independent processors that have a need for high speed mathematical functions. Although it may not be possible to justify a high speed math module for each system, such a module might be justified if it were to be shared by both processors. A multiple processor microcomputer system could provide the capability to allow both processors to share the math module and not interfere with their otherwise unrelated functions.

This application (illustrated in Fig 7) could be handled with four boards. The SBC 80/05 single-board computer is used to perform various data processing functions requiring high speed floating-point arithmetic. The SBC 80/20 single-board computer controls a process where high speed numeric computations are required. High speed floating-point mathematics functions for both single-board computers are performed by an SBC 310 high speed math unit. SBC 116 combination memory and I/O board provides 16k RAM, 8k electrically programmable read-only memory (EPROM), 48 parallel I/O lines, and an RS-232-C serial port.

The problem to be solved in this application is to ensure that only one processor has access to the shared math module resource at one time. Thus, mutual exclusion must be provided to control the access to the resource. The following PL/M function returns TRUE if access to a critical section, used to implement the mutual exclusion, has been granted.

```
ENTER$CRITICAL$SECTION:
    PROCEDURE (FLAG$ADR) BYTE;
    DECLARE FLAG BASED FLAG$ADR BYTE;
    DECLARE ACCESS BYTE;
      IF FLAG = BUSY THEN                    /* Test flag */
        RETURN FALSE;                        /* Return false if busy */
      ACCESS = FALSE;
      OUTPUT(BUS$LOCK) = LOCK;               /* Lock MULTIBUS */
      IF FLAG = NOT BUSY THEN                /* Retest flag */
      DO;
        FLAG = BUSY;                         /* Set flag busy */
        ACCESS = TRUE;                       /* and access TRUE */
      END;
      OUTPUT(BUS$LOCK) = UNLOCK;             /* Unlock MULTIBUS */
      RETURN ACCESS;                         /* Return either TRUE or */
                                             /* FALSE access */
END ENTER$CRITICAL$SECTION;
```

This PL/M function first tests the flag for the busy condition before issuing a busy lock. As in the P procedure described earlier, this initial test avoids continuous locking and unlocking of the MULTIBUS while a busy wait is being executed. The following procedure performs a busy wait operation on the flag used to control access to a critical section.

```
BUSY$WAIT:
  PROCEDURE (FLAG$ADR);
  DO WHILE NOT ENTER$CRITICAL$SECTION(FLAG$ADR);
  END;
END BUSY$WAIT;
```

Typical code segments illustrating the use of these procedures follow.

```
DECLARE MATH$BD$FLAG BOOLEAN EXTERNAL;   /* Flag must be */
                                         /*  initialized */
  MATH$BD$FLAG = NOT BUSY;
  . . .
  . . .
  CALL BUSY$WAIT(.MATH$BD$FLAG);         /* Here we wait until */
  . . .                                  /*  we have access */
  . . .
  (Process math functions)
  . . .
  . . .
  MATH$BD$FLAG = NOT BUSY;               /* Set flag not busy */
  . . .
  . . .
  /* We could also test and then do some other */
  /*   processing if the math module is busy */
  IF ENTER$CRITICAL$SECTION(.MATH$BD$FLAG)
  THEN DO;
          . . .
          . . .
          (Process math functions)
          . . .
          . . .
          MATH$BD$FLAG = NOT BUSY;       /* Set flag not busy */
       END;
  ELSE DO;
          . . .
          . . .
          (Something else)
          . . .
          . . .
       END;
```

Conclusions

The motivations for implementing multiple processor microcomputer systems include enhanced performance and throughput. When the appropriate hardware/software design considerations are made, modularity is easily achieved. Hardware solutions to many problems are provided by means of a MULTIBUS structure and SBC 80 single-board computers that have multimaster capability. Through control of MULTIBUS functions, the software designer can perform multiple processor communication, synchronization, and mutual exclusion.

Even with these significant steps toward the simplification of multiple processor microcomputer systems, the design of such systems remains a complex software/hardware design task. The future trend of multiple processor microcomputer systems will be to simplify the software tasks of implementing communications, synchronization, and mutual exclusion. These functions could be performed in varying degrees by additional hardware bus functions.

Potential rewards for a multiple processor architecture include enhanced system throughput, improved real-time response, modular system expansion, and improved system reliability. These benefits will pressure the technology of parallel processing to include microcomputers in an increasing number of computer applications.

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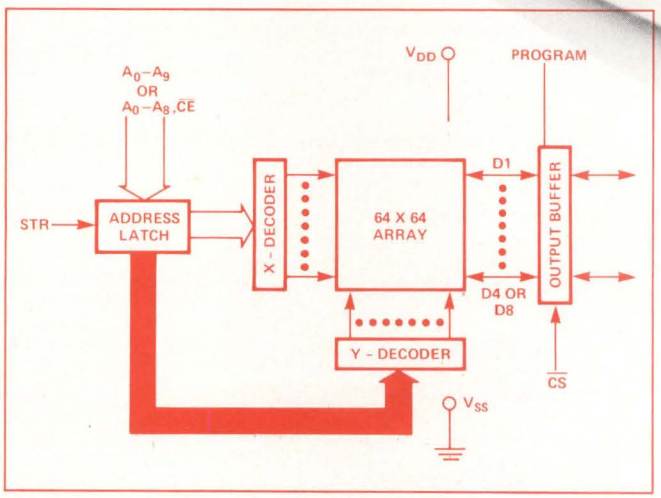

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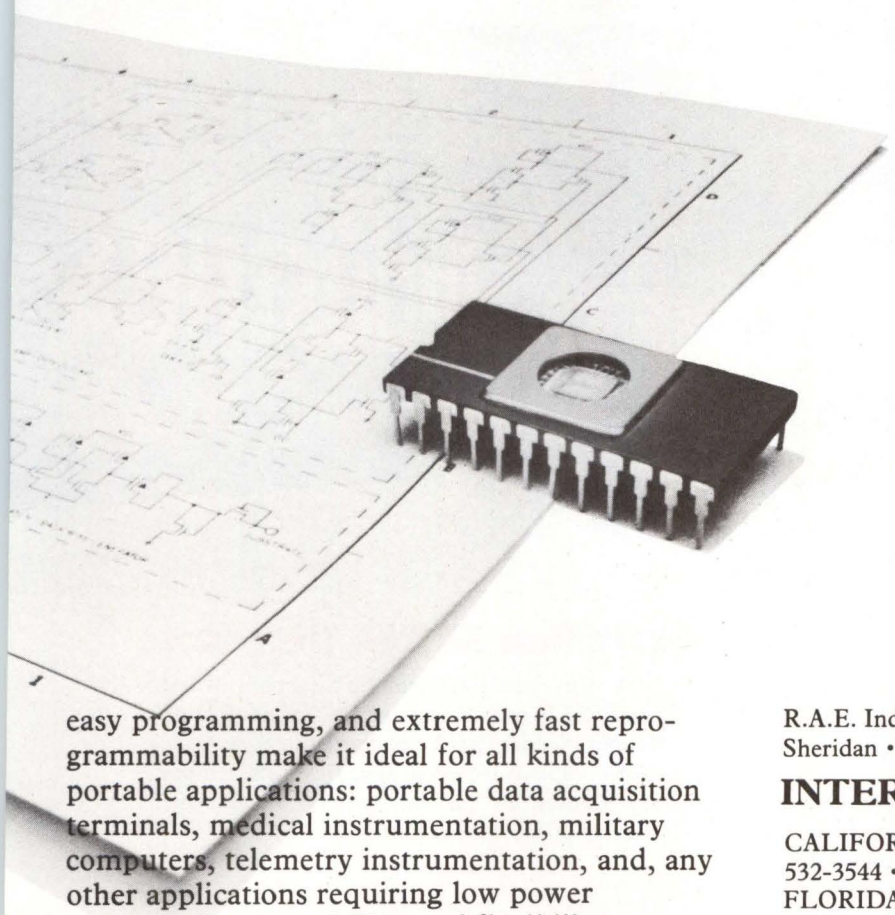

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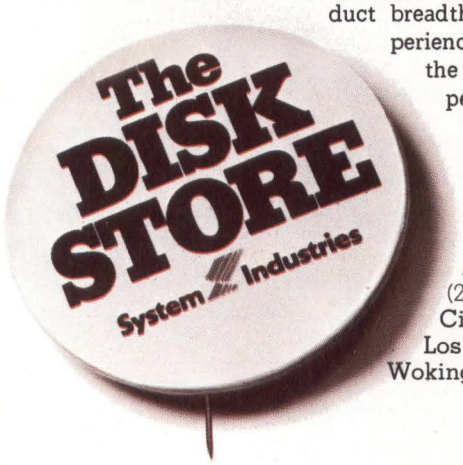

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ARRAY PROCESSOR PROVIDES HIGH THROUGHPUT RATES

A low cost, high speed array processor coupled to a minicomputer matches the processing throughput and accuracy of larger, more expensive systems for scientific computations

Woodrow R. Wittmayer Floating Point Systems, Incorporated, Beaverton, Oregon

Scientific computations impose special requirements on a computer system, such as a high rate of throughput for repetitive calculations, manipulation of large arrays of data, precision in cascaded calculations, accommodation of numbers over a large dynamic range, and reasonable ease of programming. To a large extent, algorithms for scientific calculations consist of long sequences of additions, multiplications, and multiplication-additions involving both real and complex numbers. Unless a high throughput rate is attained for such sequences, computation time becomes prohibitively long, especially when realtime calculations are needed for signal processing applications. A common measure of speed for scientific computations is the megaflop, defined as one million floating-point operations per second. Machines usually designated as scientific computers meet or exceed a 1-megaflop execution rate.

Scientific calculations on arrays of 1024 data points are routine, and more than 16,000 data points are often involved in fast Fourier transforms (FFTs), convolutions, or correlations. A scientific computer must manipulate these large data arrays quickly and accurately.

Although the accuracy of most scientific data does not exceed 0.1%, high precision is still mandatory in a scientific computer because various data points—or the same data point—are manipulated many times over in a multitude of combinations, increasing the chances for error propagation. Without a high degree of digital resolution, truncation errors and subtractions of similar sized numbers would cause large errors in the final results.

In many applications, general-purpose computers are used for performing scientific calculations; however, their performance is often unsatisfactory. Since they must serve a variety of application needs, general-purpose computers are not optimized to meet scientific computation speed requirements at an acceptable cost. General-purpose, large mainframe computers, while satisfying speed requirements, are too expensive ($1 million and up) to be dedicated to most single applications. In addition, their sheer size and power requirements present logistic support problems in mobile application environments such as shipboard or airborne installations. Less expensive minicomputer systems ($50k to $100k) are inherently too slow (less than 10^6 operations/s) for many scientific applications.

These drawbacks of general-purpose computers led to the design and development of high speed, hardwired machines to perform specific scientific calculations. Such machines offer user-acceptable cost/performance ratios. Typically, however, they perform only a few types of calculations and, hence, lack the flexibility to solve a broad range of problems in scientific computation. Also, much effort, time, and expense are expended in custom designing a hardwired machine for a particular application with only a limited market.

Certain machines designed for high speed scientific computation have been available, such as the ILLIAC IV.

These machines offer powerful solutions (based on architectures involving many parallel processors), which overcome the lack of flexibility inherent in hardwired machines. However, their cost is prohibitive for most scientific applications, and programming is complex for the uninitiated. On the other hand, small scale, low cost scientific computers are typically limited to integer arithmetic rather than floating-point for reasons of speed. This restricted word length (often 16 bits) imposes limits on scientific accuracy and the dynamic range of numbers which can be handled.

The pressing requirements for solving scientific computation problems have resulted in the evolution of a programmable array processor that can be combined with a host computer to optimize throughput, precision, and dynamic range, at a cost which makes widespread applications feasible. These processors also offer reasonable ease of programming for those who have no software expertise. In practice, the processor must either be programmable in a higher level language, such as FORTRAN, or be accessible through another computer programmed in FORTRAN. Although detailed software considerations are beyond the scope of this hardware-oriented article, the array processor described (AP-120B) is easily accessible through a host computer that controls routing of data to and from the processor, as well as initiating computations. The simplicity of the FORTRAN instructions needed to initiate computations is explained in an operational example.

Because of the large data arrays involved, scientific computing is often called vector processing or array processing. As used here, an array processor refers to a processor optimized for handling large arrays of data, not to the large array of separate processors used in a machine like the ILLIAC IV.

Optimum Data Format

Historically, scientific notation—or floating-point format—has been implemented as 32 bits (two words in a 16-bit machine). Typically, eight bits were used for the exponent and 24 bits for the mantissa. In decimal terms, this represents a dynamic range of about $10^{\pm 38}$, and a precision of approximately six significant digits. Since 6-digit precision had definite scientific accuracy limitations, development of a double-precision floating-point representation was forced—often a 64-bit format with the additional bits used in the mantissa.

For most scientific algorithms, a 64-bit double-precision format represents overkill. A 38-bit floating-point format using a 28-bit mantissa (between eight and nine significant decimal digits) and a 10-bit exponent (dynamic range of $10^{\pm 153}$) has proven to be an improved tradeoff in terms of precision, dynamic range, and hardware expense (both logic and memory). It would be difficult to implement such an optimum format in minicomputers where standard word length (16- or 32-bit) constraints exist. In a computational resource such as an array processor, a variety of input data sources must be accommodated, such as different host computers and peripheral devices. Since these have differing formats which must be converted in any case, it is just as easy to use the optimum 38-bit format as to be constrained to a non-optimum format.

Architecture Overview

Combining a special-purpose array-transform processor with a general-purpose host computer (Fig 1) allows each to perform individually in an optimum manner for a given application. AP-120B can be combined with a wide range of commercially available minicomputers or large mainframe computers ranging from the DEC PDP-11 series to the IBM 360/370 series. More than one array processor can be connected to the host to achieve a further increase in scientific computing power for applications where array processor calculation times are long enough to allow for sufficient host input/output (I/O) time.

The host computer provides overall system control; that is, it controls the flow of data and instructions between I/O devices and the array processor. Processing time inefficiencies would result if the high speed of the array processor were interfaced directly with peripherals, such as line printers, not required in the immediate fast computation scenario. On the other hand, today's minicomputers offer sophisticated operating systems capable of handling multiple peripherals (magnetic tape, disc file, line printer, and data communication ports) and large working memories.

Computational capability needed for fast, complex calculations involving large amounts of data (on the order of 64k words or more) is supplied by the array processor. It is more time efficient to leave single calculations, such as an occasional sum or product (or even short vector operations) to the host computer. For more involved computations, however, the array processor may well be 100 or more times faster than the host.

Functionally, the array processor can be separated into a floating-point adder and floating-point multiplier, multiple independent memories, and the multiple data paths necessary to connect various memories with the two arithmetic processing units. The interface between host and array processor can be structured into two sets of registers (see Fig 2). One set is devoted to control via programmed I/O, the other to data transfers via direct memory access (DMA). The programmed I/O section of the interface can be thought of as providing the array processor with a simulated front panel. Control of this front panel resides with the host computer which uses it for bootstrap operations (loading and starting programs in the array processor) and for debugging user software (inserting hardware breakpoints and modifying contents of array processor registers and memory). Programmed I/O registers include (1) a switches register used by the host to enter control or parameter data and addresses into the array processor; (2) a lights register which makes available to the host the contents of internal array processor registers; and (3) a function register into which the host can write typical front panel commands such as start, stop, reset, or continue.

Most minicomputer or larger hosts provide DMA capability. To maximize the speed of 2-way data transfer (and hence maximize throughput), the array processor includes a set of DMA interface registers to provide 2-way direct memory access. Stealing clock cycles for a 100-kHz data transfer rate degrades running speed of the array processor by only 3% or less. The DMA register set includes host memory address register, array processor

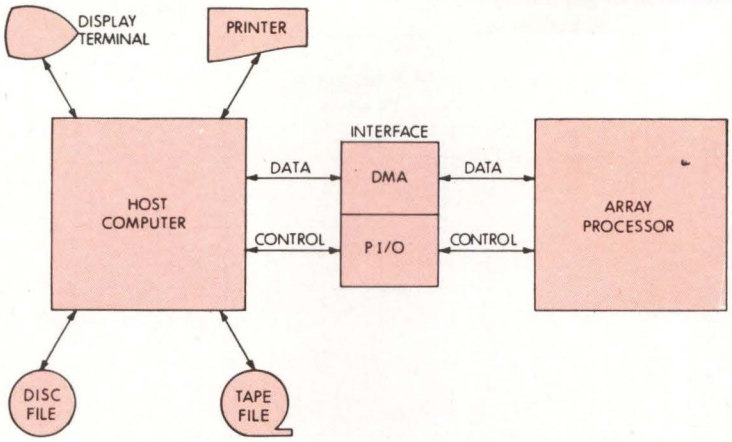


Fig 1 Array processor/host computer combination. Very high speed scientific computation at modest cost is achieved by combining general-purpose minicomputer for overall control and I/O with high speed, floating-point array processor for computation. Interface consists of programmed I/O for control of array processor by host and 2-way DMA for transferring data and programs between host and array processor

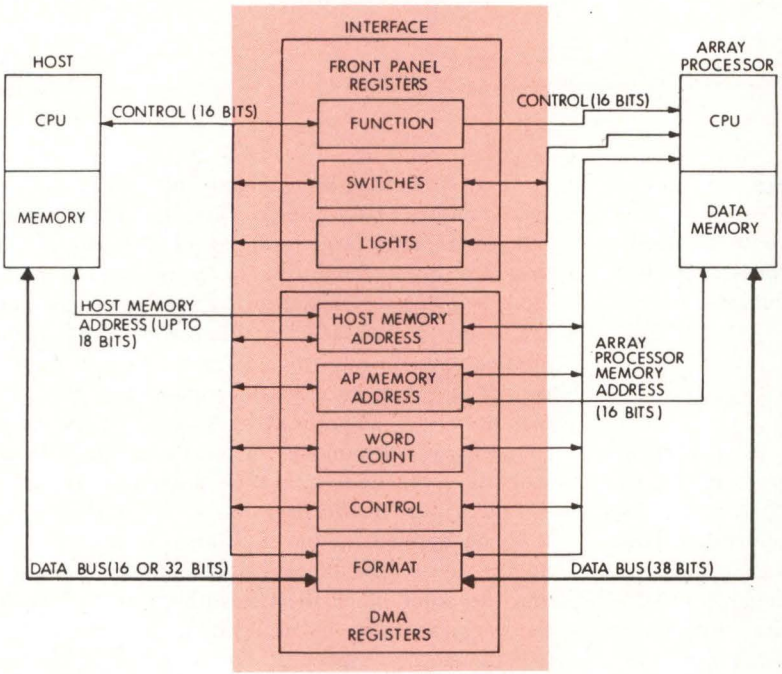


Fig 2 Interface between host and array processor. Interface consists primarily of two sets of registers. Through one set, host controls array processor by means of simulated front panel. Second set provides 2-way DMA for transfer of data and programs between host and array processor with floating-point format conversion on-the-fly

memory address register, word count register to keep track of the number of transferred words, and control register to govern direction of data transfer and mode of transfer. A fifth (format) register in the DMA set provides conversion between the floating-point format of the host and that of the array processor. Control of this double-buffered, 38-bit register is exercised by four bits in the control register. All transfers of floating-point numbers between host and array processor are by way of the format conversion register. This approach provides conversion "on-the-fly" between the various floating-point formats in existence among hosts and the 28-bit mantissa, 10-bit binary exponent format of the array processor. Interface logic permits data transfer to take place under control of either the host or the array processor.

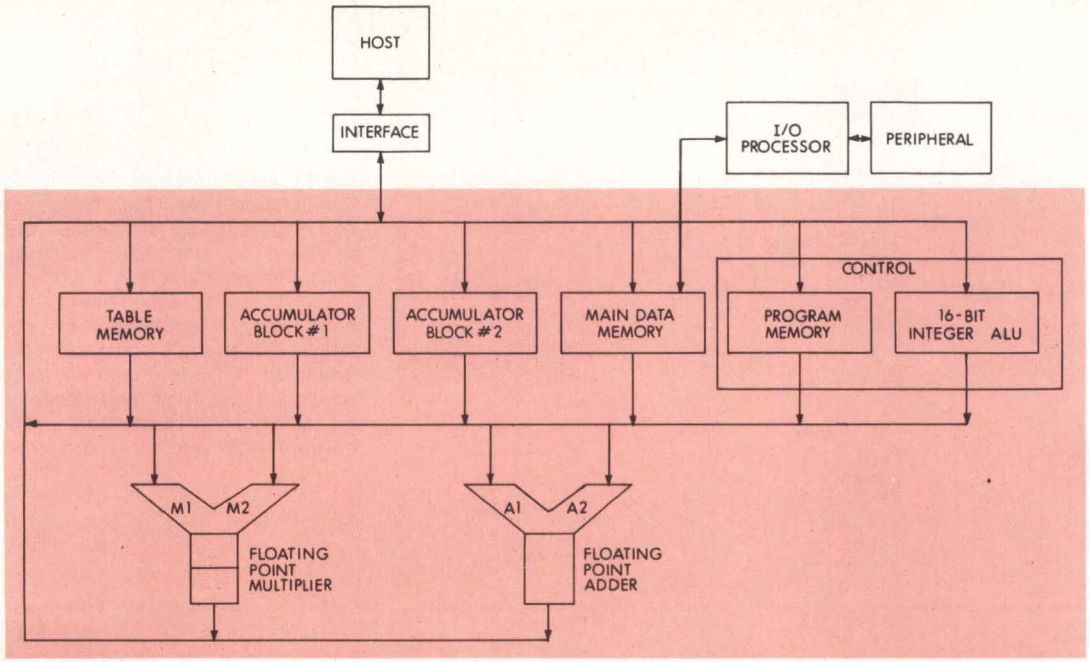


Fig 3 Parallel organization. To a large extent, array processor's high throughput stems from parallel arithmetic units and parallel memories. Floating-point adds, floating-point multiplies, control arithmetic operations, memory accesses, host array processor data exchanges, and peripheral I/O operations can all be overlapped in time

Achieving High Processing Speed

To achieve processing speeds consistent with scientific computation needs, the AP-120B array processor makes use of two primary architectural techniques—parallel organization and pipelining.

Parallel Organization

Parallel organization in this case refers to a parallel organization of dissimilar functional elements as shown in Fig 3. Separate program, data, and table memories are provided, and can be addressed independently. This organization speeds computation by eliminating memory access conflicts. Random-access read-write memory (RAM) is used for both program and data memories while read-only memory (ROM) is frequently used for the permanent constants in table memory. RAM can also be used for large blocks of constants in table memory which may change from time to time.

The arithmetic unit is composed of a floating-point adder and a floating-point multiplier. These two independent units increase throughput by allowing multiplication and addition portions of calculations to proceed simultaneously. The adder consists of A1 and A2 input registers plus a 2-stage pipeline which first adds the contents of the registers and then rounds the normalized result. The multiplier has two input registers, M1 and M2, plus a 3-stage pipeline for multiplying the two inputs. The product is a normalized and rounded 38-bit number.

There are two independent blocks of floating-point accumulators. Each block contains 32 registers of 38 bits each. This large number of accumulator registers provides great flexibility in storing temporary results from sequential calculations. Experience has shown that the majority of these accumulators are employed in many applications. In addition, dividing the accumulators into two blocks, or two scratchpads, adds flexibility. For instance, both adder and multiplier can be driven with four separate arguments on the same cycle, or two transformation matrices might be stored in the two blocks. An algorithm in the program could select which matrix is to be applied by the multiplier to a given vector. In another case, one block might contain a set of vectors and the other block the transformation matrix by which the vectors are to be multiplied.

Still another aspect of the parallelism for increasing throughput is an independent 16-bit integer arithmetic logic unit (ALU) for performing counting and address indexing. By incrementing and decrementing loop counts and generating memory addresses with this unit, the main arithmetic units are made available full time for the computations at hand.

Two vital elements complete the array processor's parallel structure. First, multiple 38-bit wide data paths connect the interface to multiple memories, and memories to floating-point arithmetic units. These multiple paths provide an independent connection between each memory and each arithmetic unit (see Fig 4) via a proprietary multiplexing scheme. Second, simultaneous control of the various parallel elements is provided by a

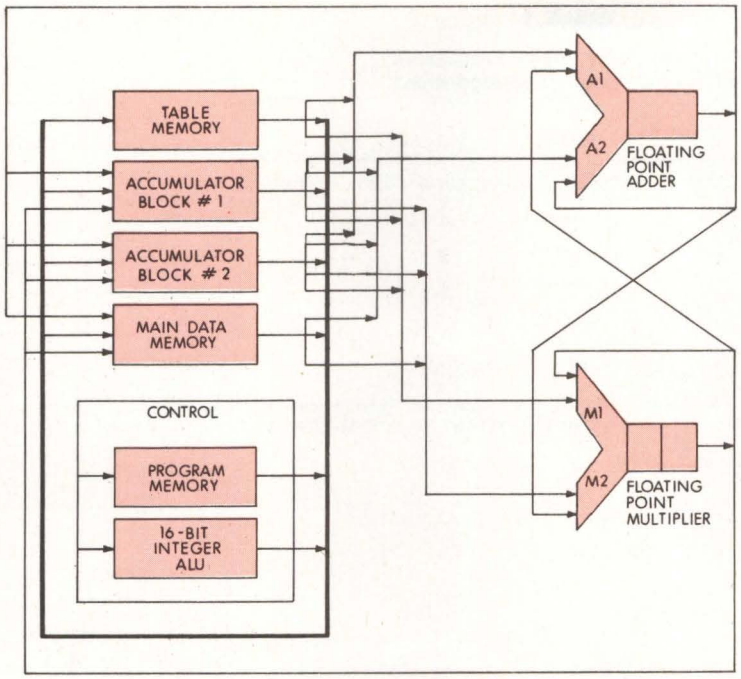


Fig 4 Multiple data paths. Array processor's adder and multiplier units are connected to multiple memories, to control arithmetic unit, and to each other by independent, multiple data paths. These multiple paths allow maximum use to be made of parallel functional elements for overlapping control, memory access, and computation times

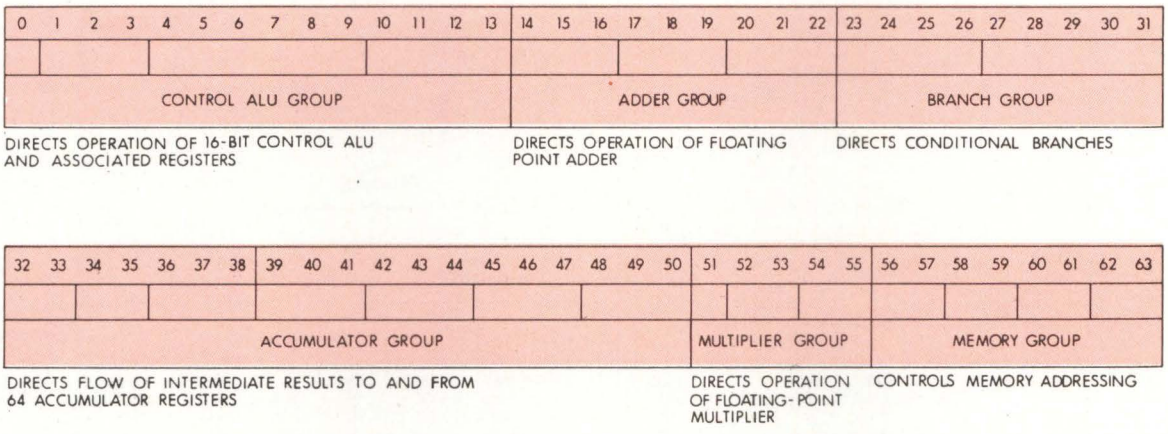


Fig 5 Instruction word command fields. A 64-bit instruction word makes possible up to 10 simultaneous operations (control functions, memory accesses, and computations). Coupled with 6-MHz clock, this results in up to 60M operations/s and assures high degree of utilization of 12-megaflop throughput capability of floating-point arithmetic units

64-bit wide instruction word subdivided into a number of command fields (as shown in Fig 5). Each command field controls a separate device. Thus, a single program instruction controls all operations. There is no need for separate programs for floating-point adder, floating-point multiplier, integer ALU, and memory controller; and no need for an elaborate master controller to synchronize such separate programs. As many as 10 op-

TABLE 1

Performance of Vector Processors In Phase Demodulation Algorithm*

Machine	CPU Cost (million $)	Performance (megaflops) Max	Actual	Cost/Performance Megaflops/$M	Performance Ratio**
CRAY-1	$4.5	80	20	4.44	10.57
STAR 100	$8.0	50	16.6	2.1	5.0
CDC 7600	$3.0	8	3.3	1.1	2.62
CDC 6600	$1.5	2	.63	.42	1.0
AP-120B	$0.1	12	7.9	79.0	188.0

*R. S. Brucy and K. D. Senne, "Nonlinear Filtering Algorithms for Parallel and Pipeline Machines," *Proceedings of Conference on Parallel Mathematics and Parallel Computing*, Apr 1977, North Holland Press, Amsterdam, 1977

**Compared to CDC 6600 as a base of 1

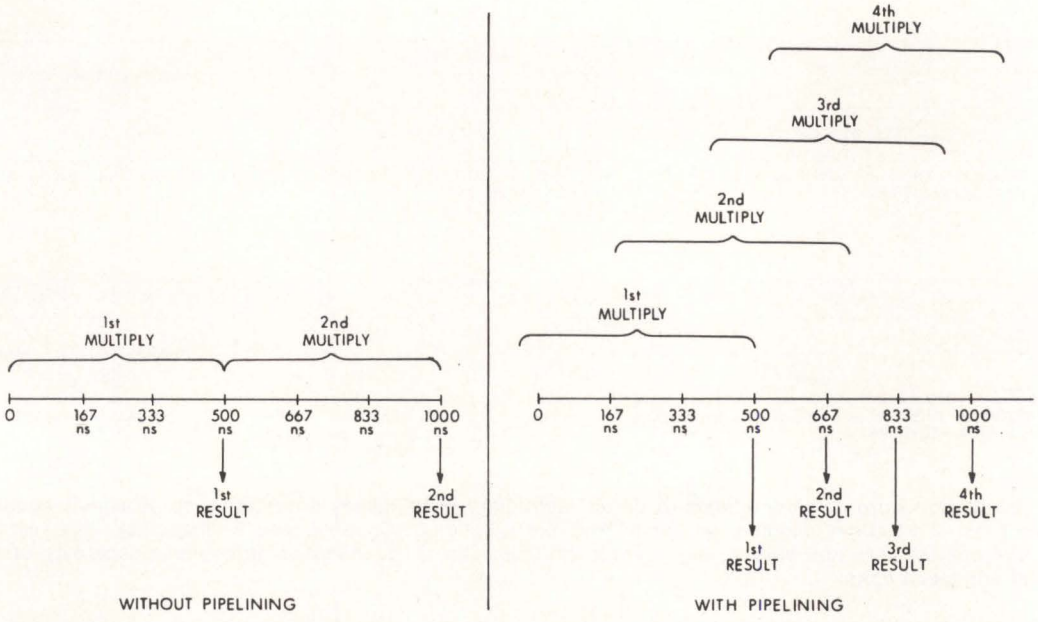


Fig 6 Pipelined design. By overlapping three steps of floating-point multiply in time, pipelining yields three times increase in throughput for sequential multiplications. Similarly, two times increase is achieved by pipelining two steps of floating-point addition

TABLE 2

Floating-Point Arithmetic Times

Operation	Travel Time	Pipeline Interval
Add/Subtract	333 ns	167 ns
Multiply	500 ns	167 ns
Multiply/Add	833 ns	167 ns
Complex Add/Subtract	500 ns	333 ns
Complex Multiply	1333 ns	667 ns
Complex Multiply/Add	1667 ns	667 ns

erations/cycle are possible with the 64-bit instruction.

The array processor's parallel memories, parallel adder and multiplier, and parallel data paths result in an almost complete overlap of computation time and memory access time, hence greater throughput. Note in Table 1 that the array processor (AP-120B) achieves a higher ratio of actual megaflops to maximum megaflops than several larger machines. This is largely because of the parallel structure and the multiple command fields in the instruction word.

Pipelining

In addition to providing parallel floating-point arithmetic units for simultaneous addition and multiplication, the array processor enhances throughput by pipelining each of these operations. A floating-point multiply, for example, involves three steps: (1) beginning product of fractions, (2) adding exponents and completing product of fractions, and (3) normalization and rounding of result. Each step requires one machine cycle (167 ns in the AP-120B); thus a complete multiply requires 500 ns.

Without pipelining, hardware associated with two of the three steps is idle while the third step is in process. This means that a result is available every 500 ns (Fig 6). With the array processor's pipelined design, the hardware for all three steps is in operation all of the time (Fig 6). When the first step of a multiplication is completed, that multiplication proceeds to step 2 hardware. While step 2 is in process, a second multiplication is started in the step 1 hardware. The process continues until the "pipe is filled." A long sequence of multiplications can be made to flow smoothly through the pipe. Results are available at 167-ns intervals once "the pipe is filled"—after 500 ns.

Results of Paralleling and Pipelining

The clock frequency of the array processor is 6 MHz (a 167-ns period). The floating-point adder and the floating-point multiplier operate simultaneously with each producing a result every 167 ns. This represents a maximum potential computation rate of 12M floating-point operations/s or 12 megaflops. Compare this rate with that of a general-purpose computer such as the PDP-11/70, which, even with floating-point hardware, has a 0.2-megaflop potential computation rate.

Presence of multiple memories in the array processor makes it easy to supply arguments to support the 12-megaflop computation rate. Moreover, data transfers to or from the host, and I/O communication with peripherals attached to the array processor can also take place during computation time. This leaves only the overhead (operations other than multiply-add) associated with a given scientific computation algorithm to cause less than maximum throughput. Actual travel time through the floating-point arithmetic units (total time to get from data source to data destination) and pipeline interval between successively available resultants are listed in Table 2 for various calculations.

Parallel structure and pipelining result in very high floating-point throughput. This architecture reduces the pressure to make use of the latest state-of-the-art high speed logic circuits. Standard Schottky transistor-transistor logic (TTL) circuitry has resulted in lower hardware cost and increased reliability compared with a design stressing the ultimate in high speed circuitry. Selection of a modest 6-MHz clock rate allows generous timing margins for worst-case design. The 12-megaflop array processor includes host interface and the data, table, and program memories needed for lengthy scientific computations such as FFTs involving 8k data points. It operates with a demonstrated mean time between failures (MTBF) of 3600 h.

The Array Processor in Operation

Proof of the array processor's successful performance in high speed computation results from extensive computational tests. Brief discussion of common scientific calculations serves as an indication of actual performance.

In digital signal processing, convolution is based almost exclusively on multiply-adds. Since results from multiply-adds are available at 167-ns intervals in the array processor, the maximum rate at which convolution could proceed is 167 ns/point. In actual operation, with all nonoverlapped memory access time and overhead operations accounted for, an average of 172 ns/point is achieved.

The array processor performs matrix arithmetic operations such as the transpose or inverse of a matrix extremely rapidly. The inverse of a 50 x 50 matrix, for example, can be performed in less than 0.15 s, compared

with the 12 s required on a Data General Eclipse computer.

Statistical analysis, as illustrated by standard deviation calculations, proceeds at a rate approaching 167 ns/point, which is about 100 times faster than on a PDP-11/70. The independence of the multiplier and adder units allows successive values to be brought in and squared and running totals of both the values and the values squared to be kept at the same time.

Processing speed in numerical simulation is portrayed by considering a phase demodulation algorithm which uses partial differential equations. Table 1 lists the results attained when this algorithm was run on several computers commonly used for scientific computation. As can be seen, the inexpensive AP-120B array processor compares favorably with more expensive machines in absolute performance, and surpasses them when cost/performance is the primary criterion.

Operational Example

To clarify the concept of how the host/array processor system operates, consider a simple FFT processing sequence. As initial conditions, assume that the FFT program is resident in the array processor's program memory and that the array to be transformed is resident in host memory. The operating sequence is

(1) The host sends an I/O instruction to the array processor to start operation.

(2) The array processor requests host cycles for DMA transfer of the data array from host memory to array processor data memory. Data pass through the interface's format conversion register where they are converted from host floating-point format to array processor floating-point format "on-the-fly".

(3) The FFT algorithm is run in its entirety inside the array processor. This means that full 38-bit precision is maintained throughout critical processing stages.

(4) The frequency domain array can then be transferred back to the host by requesting host cycles for DMA transfer. Again format conversion takes place "on-the-fly".

(5) The array processor proceeds to another process or stops executing instructions based on previous directions from the host. In the absence of further instructions, an interrupt command to the host can be issued.

The entire process is accomplished from the host computer with only four FORTRAN statements.

```
CALL APCLR                (clear array processor)
CALL APPUT (a1 ..... a4)  (transfer data to array processor)
CALL CFFT (a1 .....a4)    (perform FFT)
CALL APGET (a1 .....a4)   (transfer results to host)
```

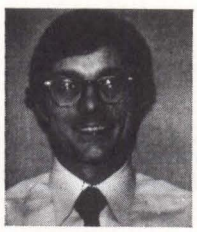
To minimize data transfer overhead, the four statements can be modified so that a longer unbroken sequence of calculations takes place. For example, both a digitized waveform and data representing an electrical network can be transferred from host to array processor. After FFTs have been performed on both data types, they could be array multiplied, an inverse FFT performed on the resultant, and the resulting time domain waveform transferred back to the host. Keeping the entire sequence in the array processor enhances precision in addition to reducing overhead.

Conclusions

Potential throughput of the AP-120B array processor is 12 megaflops. Viewed another way, the processor runs at 6M instructions/s and each 64-bit instruction word can control up to 10 simultaneous operations. These processing capabilities result in up to 60M operations/s including floating-point adds, floating-point multiplies, program memory accesses, data memory accesses, scratchpad accesses, integer arithmetic operations for control of the array processor, and I/O operations. Performing 60M operations/s (due to parallel arithmetic units, memories, and data paths, and to multiple command fields in the instruction word) assures a high degree of utilization of the unit's 12-megaflop potential.

With a mantissa of 28 bits, the array processor ensures the precision necessary in iterative scientific calculations. In decimal terms, the 28 bits correspond to between eight and nine significant digits. A 10-bit binary exponent provides the array processor with a greater dynamic number range than the commonly encountered 8-bit binary or 7-bit hexadecimal exponents without the precision problems of hexadecimal normalization.

The array processor satisfies the ever increasing demand for extremely high speed scientific computing at low cost. It handles the speed, precision, and dynamic range demands of scientific computations which previously were satisfied only by large, expensive mainframes. Coupled with a minicomputer, the cost of an array processor is on the order of 1% to 6% of a large mainframe's cost, and, in some cases, it may have greater throughput than the larger machine.



Woodrow Wittmayer holds BS degrees in psychology and computer science from Portland State University. Currently product manager for the AP-120B array processor at Floating Point Systems, his experience includes application engineering for array processors.

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UNIVERSAL SWITCHING REGULATOR DIVERSIFIES POWER SUBSYSTEM APPLICATIONS

Standard and advanced power control subsystems are based upon a single, universal IC chip, whose internal functional building blocks can be configured for differing voltage step-up, step-down, and inverter modes simply by connecting external components

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Fairchild Camera and Instrument Corporation, Mountain View, California

Unlike series-pass regulators, switching regulators are complex devices requiring external parts and demanding care in system application. In addition, switching regulators add noise, contribute output ripple, and respond slower to transients. However, these disadvantages are outweighed by two key advantages: switching regulators are very efficient, and they can produce output voltages that are greater than (step-up mode), less than (step-down mode), or of an opposite polarity to (inverter mode) the input voltage.

Efficiency is the outstanding feature. Switching regulator subsystems can achieve up to 90% efficiency; in high power systems this means small transformers, minimum cooling, low power consumption, and low operating cost. Series-pass regulator efficiency depends upon V_{OUT}/V_{IN}, and decreases as the input voltage increases for a fixed output voltage. Switching regulator efficiency is constant for variations in input voltage and is limited only by switching device losses due to small dc voltage drops and switching transients. This single integrated circuit (IC), made up of functional building blocks and operating over a wide spectrum of application conditions, enables a variety of complete switching and/or series-pass regulator systems to be developed by the system designer utilizing a minimum number of external components.

Switching Regulator Concepts

Switching regulators use output transistors (or switches) in a nonlinear mode and store energy in inductors and capacitors until needed by the load. The input/output differential voltage is applied across an inductor rather than across a pass transistor. [An inductor does not dissipate power while a pass transistor (in a series-pass regulator) does.] The switching device is turned on and off at a rate determined by the input and output voltages and load current to provide enough power from the input as demanded by the load. The output voltage is sensed by the control circuitry, which modifies the timing to keep the output voltage constant. An output capacitor is used to store energy during the off periods and to average the flow of current to the load.

Step-Down Voltage Regulator

A simple step-down voltage regulator is shown in Fig 1(a). When switch S1 closes, voltage V_A rises toward V_{IN} ($V_{IN} - V_S$), and voltage $V_A - V_{OUT}$ is applied across inductor L, causing current to increase from zero

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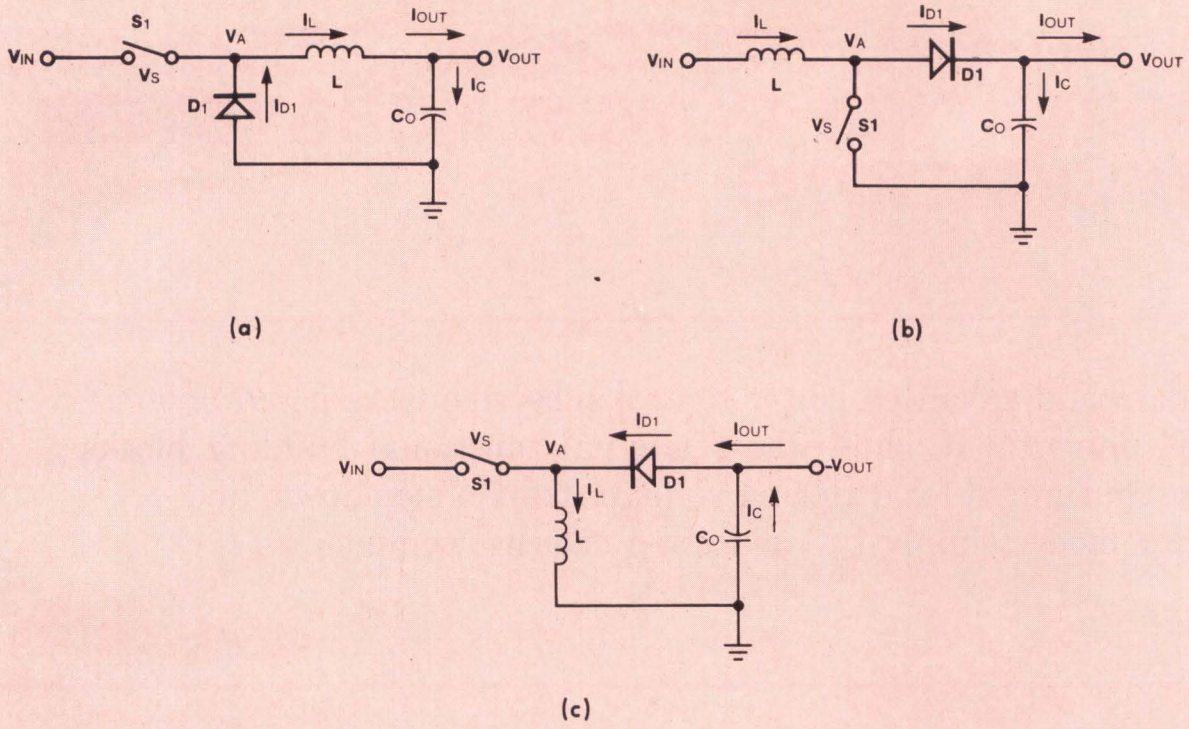

Fig 1 Basic operating modes. Simplified diagrams show essential components of flyback switching regulators, and their interconnection. Step-down (a), step-up (b), and voltage inverter (c) circuits use same four basic components: switch and diode to direct current flow, along with inductor and capacitor for energy storage

at a rate of $(V_A - V_{OUT})/L$. This current flows from the switch, through the inductor, and into load and output capacitor C_O. If the instantaneous inductor current (i_L) is less than the load current (I_{OUT}), the output capacitor provides additional current and V_{OUT} decreases slightly. When i_L exceeds the output current, the remaining current flows into the capacitor, increasing V_{OUT}; i_L will increase until switch S1 turns off (opens). At this time, since the inductor current cannot change instantly, V_A falls to $-V_D$; diode D1 provides and conducts the inductor current. The voltage across the inductor is now $-(V_{OUT} + V_D)$; thus, the inductor current will change at a rate of $-(V_{OUT} + V_D)/L$. Inductor current continues to fall toward zero until S1 turns on again, and the cycle is repeated.

On- and off-times of S1 are controlled so that the average inductor current equals the output current; thus, the average capacitor current will be zero and V_{OUT} will remain constant. The control circuit generally consists of an oscillator and a subcircuit. On- and off-times of the oscillator are set so that i_L will increase to a maximum current of Ip and then decrease to zero. The subcircuit senses the output voltage and increases the off-time (by adjusting the oscillator) if V_{OUT} increases too high. In this type of system, a maximum I_{OUT} of Ip/2 is possible, and for I_{OUT} less then Ip/2, the control circuit increases the off-time by an amount such that the average i_L equals I_{OUT}.

For a step-down regulator, peak current is determined by the input, output, and switch voltages, inductor size, and switch on-time; or conversely, the on-time (t_{on}) is set to give the desired peak current. In a similar manner, the off-time (t_{off}) required for i_L to drop to zero is related to Ip, V_{OUT}, V_D, and L. The ideal ratio of t_{on} to t_{off} is a function of V_{IN}, V_{OUT}, V_D, and V_S. The maximum output current for this timing is Ip/2, and the average input current is Ip/2 times the percentage of time the switch is on.

Efficiency of this regulator (excluding current for the control circuitry and switching losses) is $(V_{OUT} \times Ip/2)/V_{IN} \times I_{IN\ AVG}$, which is shown to be a function of V_{IN}, V_{OUT}, V_S, and V_D. If V_S and V_D go to zero, efficiency goes to 100%; therefore, if V_S and V_D are small compared to V_{IN} and V_{OUT}, very high efficiencies can be achieved. Output ripple is a function of Ip, t_{on}, t_{off}, and C_o, and can always be reduced by increasing C_O without affecting other portions of the circuit.

Timing control is very important in maximizing the efficiency of a switching regulator. Optimum on- and off-times are a function of circuit variables (eg, L, V_S, and V_D) and system variables (eg, V_{IN} and V_{OUT}), and must be able to respond to changes (eg, V_{IN}).

Consider the following cases of nonoptimum timing.

(1) If t_{on} is too short, the inductor reaches a peak current less then Ip. Therefore, $I_{OUT\ MAX}$ is less than Ip/2, but no efficiency is lost.

(2) If t_{on} is too long or t_{off} too short, after several continuous cycles, i_L will exceed Ip and will continue to increase. This situation can lead to excessive current flow and device destruction, and must be avoided.

(3) If t_{off} is too long, i_L falls to zero and stays at zero for some time before S1 turns on again. In this case, the average inductor current is less then Ip/2, and the available output current is less then Ip/2. No loss in efficiency occurs.

(4) For the t_{on} too-long case, the type of current limiting in S1 is unacceptable because when I_L is constant at Ip, the inductor voltage drops to zero, and the switch voltage increases to $V_{IN} - V_{OUT}$. This creates a large loss in efficiency and can even be destructive to the switch.

(5) For the t_{on} too-long case, another type of current limiting shortens t_{on} when Ip is sensed, without loss in either efficiency or peak output current.

(6) Current limiting adjusts t_{on}, but t_{off} is too short. In this case, there is no efficiency loss. However, since i_L does not fall to zero, the average inductor current exceeds Ip/2 and the maximum output current, therefore, is greater than Ip/2.

Step-Up Voltage Regulator

With the step-up voltage regulator shown in Fig 1(b), the output voltage is greater than the input voltage. When S1 closes, V_A falls to near zero ($V_A = V_S$), and voltage $V_{IN} - V_S$ is applied across the inductor, causing i_L to increase at a linear rate. Since V_A is less than V_{OUT}, the diode is reverse-biased and no current flows to the output. When S1 opens, i_L cannot change instantaneously and V_A goes to $V_{OUT} + V_D$. Now i_L can flow through D1 to the output load and capacitor, and will decrease at a linear rate determined by $V_{OUT} + V_D - V_{IN}$. As in the step-down regulator, timing is adjusted so that the average current to the output (i_{D1}) is equal to the load current. Since i_{D1} flows during the off-time, maximum output current is (Ip/2) x ($t_{off}/t_{on} + t_{off}$). When load current less than $I_{OUT\ MAX}$ is flowing, off-time is increased by a dead time during which i_{D1} is equal to zero. Input current flows during t_{on} and t_{off}; thus, the average input current is always greater than the maximum output current.

For a step-up regulator, the on-time is a function of V_{IN}, V_S, and L, while t_{off} is a function of V_{IN}, V_{OUT}, V_D, and L. The t_{on}-to-t_{off} ratio is a function of circuit voltages, as is the maximum output current. Efficiency is also a function of V_{IN}, V_{OUT}, V_S, and V_D, and approaches 100% as V_S and V_D become small compared with V_{IN} and V_{OUT}. Output ripple is a function of Ip, I_{OUT}, t_{off}, and C_O, and can again be reduced by increasing C_O without affecting circuit performance.

Voltage Inverter

The basic voltage inverter [Fig 1(c)] generates a negative output for a positive input. When S1 closes, V_A rises to $V_{IN} - V_S$, and this voltage is impressed on the inductor, causing current to increase at a linear rate. When S1 opens, the inductor current cannot change instantaneously, so V_A drops to ($-V_{OUT} - V_D$), forward biasing D1. Current i_L now decays at a linear rate. Cur-

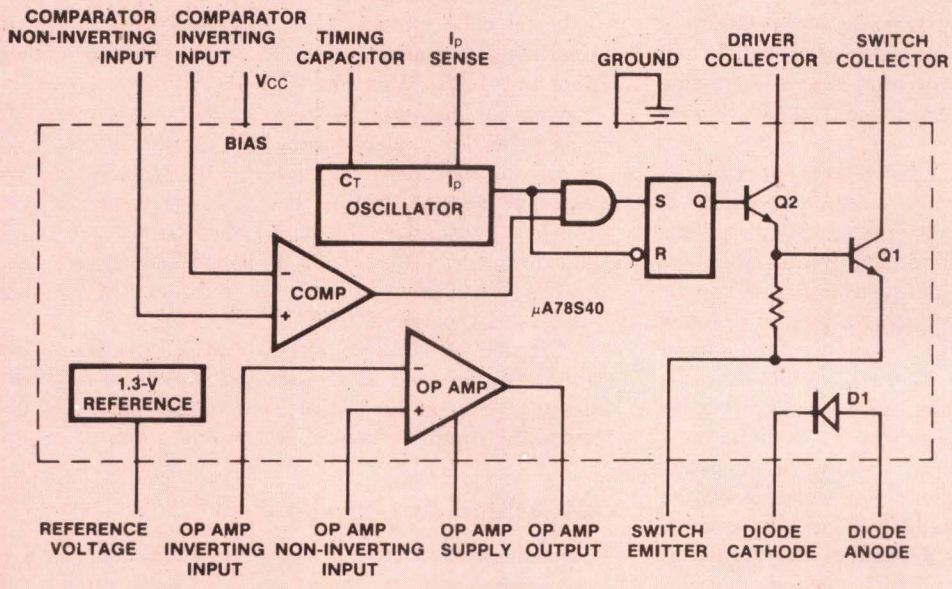

Fig 2 Universal regulator. Partitioning of circuit functions in μA78S40 allows maximum flexibility for interconnecting blocks while using minimum number of external parts. IC is available in 16-pin ceramic or 16-pin plastic with copper lead frame

rent i_{D1} flows to the output capacitor and load, and its average value must be equal to the load current. Input current flows only when S1 is closed and is therefore equal to $Ip/2 \times t_{on}/(t_{on} + t_{off})$.

For the voltage inverter mode, optimum t_{on} and t_{off} values are functions of V_{IN}, V_{OUT}, V_S, and L, while the ratio of t_{on}/t_{off} is dependent only on the voltages. $I_{OUT\ MAX}$ is always less than Ip/2, as is the average input current. Efficiency depends on input and output voltages and is basically independent of current level. Ripple can be minimized as usual by increasing the value of C_O.

IC Switching Regulator

A general-purpose IC switching regulator must include functional building blocks and versatile operation under as wide a range of operating conditions as possible. The μA78S40 universal regulator (Fig 2) accomplishes these goals while providing a wide input supply voltage range (2.5 to 40 V) and low quiescent current drain (2 mA), presently unmatched. Partitioning of the subsystem allows different types of regulators to be constructed using a minimum number of external components. These functional blocks are essentially independent. A current-controlled oscillator has drive circuitry for the transistorized power switch. Oscillator frequency (100 Hz to 100 kHz) is set by an external capacitor, and the duty cycle is internally fixed at 8:1.

The current-limiting circuit modifies the oscillator on-time to adjust the duty cycle to an optimum timing condition. This temperature-compensated circuit senses the switching transistor current across an external resistor and modifies the oscillator on-time to limit the peak current and protect the switching transistors. In addition, an independent, 1.3-V, temperature-compensated reference (0.1 mV/°C) is capable of providing up to 10 mA without external pass transistors. A high-gain differential error amplifier disables the power switch when the output voltage is too high.

The power-switching Darlington-transistor configuration can handle 1.5 A and withstand up to 40 V. Collectors of the switch and emitter driver are both externally available so that the output can be connected in an optimum manner. The power-switching diode is capable of handling 1.5-A forward current and 40-V reverse voltage.

A short-circuit protected, independent, operational amplifier (op amp) with an uncommitted output is capable of sourcing 150 mA or sinking 35 mA. This amplifier has a separate positive supply terminal. Its input common mode range includes ground, and can be connected in a variety of ways to produce series-pass regulation and feedback control for switching regulators.

This IC switching regulator operates under a wide range of power conditions from battery operation to high voltage, high current operation. Each functional block operates from low supply voltages and draws minimum current. The entire regulator functions from voltages of 2.5 to 40 Vdc, usually continues to operate down to 2.2 V, and draws only 2.0 mA at 5 V. This low voltage operation makes the μA78S40 useful in battery-operated or 5-V logic-operated systems. The low standby current drain greatly increases battery lifetime and significantly improves efficiency in low power applications. Most switching systems have a significant falloff in efficiency at low level operation. This regulator works with inputs up to 40 V and can provide up to 1.5-A switching current.

Using The Building Blocks

The universal regulator offers the designer maximum flexibility in deciding how to optimize power system performance. Oscillator timing is a critical operating parameter; the on/off-time ratio is internally set at 8:1. The designer must choose a peak current, oscillator capacitor, and inductor, along with input and output voltages to determine timing. On- and off-times determine the timing capacitor value. The designer should set the off-time and allow the current-limiting circuit to modify the on-time. The on/off ratio can therefore be adjusted from 8:1 to any lower number. Peak current is determined solely by the current-limiting circuit and is not dependent upon component variables. Off-time can be set to achieve either (1) discontinuous operation by setting t_{off} to be equal to the time it takes the inductor current to drop to zero, or (2) continuous operation by setting t_{off} to be less then the required time for the inductor current to drop to zero.

In the continuous mode, the average inductor current can exceed Ip/2, and more power is therefore available to the output; however, care must be taken with timing because if the on- and off-times are too short, switching transient losses may reduce efficiency significantly. With this regulator switching times should be greater than 10 μs for both t_{on} and t_{off}.

Line regulation of the switching regulator is a function of the power supply rejection of the 1.3-V reference and the error amplifier. Since they each have excellent supply rejection, line regulation of 80 dB or greater is possible. Timing is adjusted to account for variations in input voltage so that the regulator performs over a wide input voltage range.

The output switching Darlington configuration has the two transistor collectors and switch emitter available for external connections. When the collector output is used (emitter grounded), the designer has the choice of shorting both collectors (V_S is typically 1.1 V), and having no loss due to base current for the switch, or just using the switch output (V_S is typically 0.5 V) and providing base drive through the driver by connecting an external resistor to V_{IN}. Performance tradeoffs between the two approaches are determined by V_{IN}, V_{OUT}, I_{OUT}, and the expected variation of V_{IN}. When the emitter output is used, the two collector outputs can be shorted, and V_S is typically 1.6 V.

Capable of handling 40 V and 1.5 A, the switching diode can be used in step-up and step-down applications. In inverting applications, an external diode is needed since the diode voltage goes below the circuit common.

Standard Applications

Implementation of the universal regulator can be accomplished in a variety of standard applications; typical straightforward examples follow.

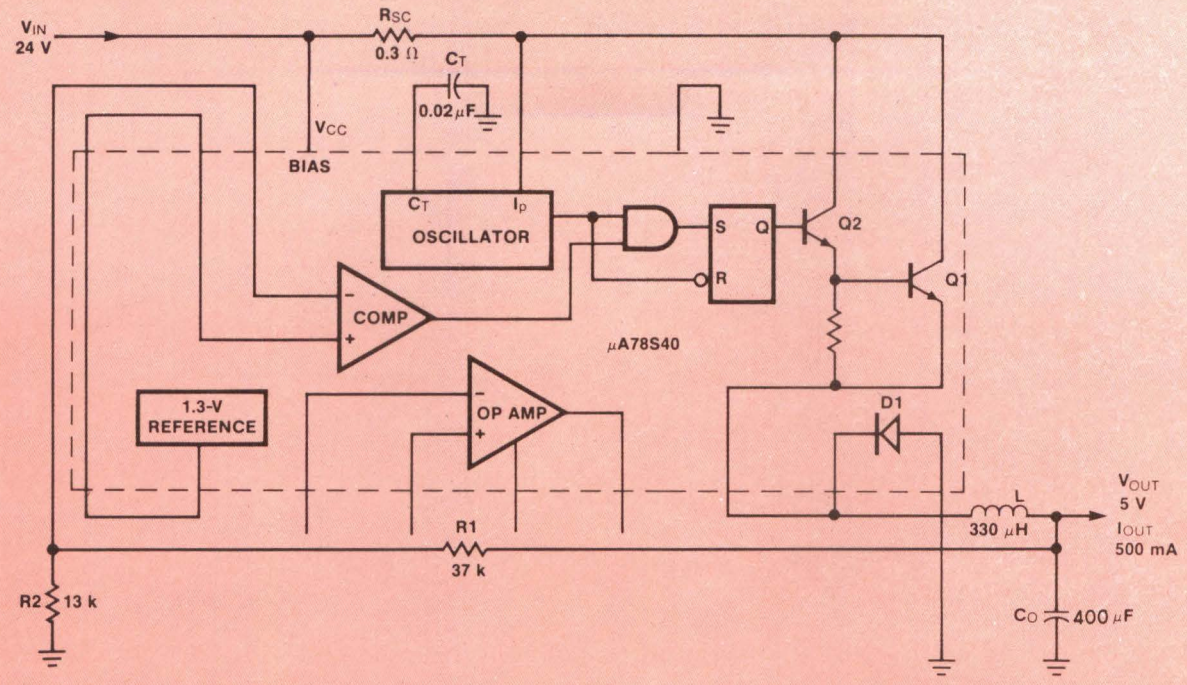

Fig 3 Step-down voltage regulator. In typical application, 24 V has been stepped-down to 5 V at efficiency of 83% for loads of 500 mA. Output voltage ripple of 25 mV and average input current of only 125 mA make this circuit useful for applications such as running TTL from 24-V battery

(1) Fig 3 shows the regulator connected as a series step-down voltage regulator. Regulator requirements are 5-V output at 500 mA from a 24-V input, and an output ripple of less than 25 mV. For this application, the regulator is connected with the power switch (Q1 and Q2) placed between the positive supply (24 V) and inductor (L); its voltage is determined by the emitter output limit of 1.6 V. For these values, the off-time will be approximately three times the on-time value

$$t_{off}/t_{on} = \frac{V_{IN} - V_S - V_{OUT}}{V_{OUT} + V_D} = \frac{24 - 1.6 - 5.0}{5.0 + 1.0} = 2.9$$

In order to keep the on-time greater than 10 μs, the off-time is made equal to 60 μs (with $C_T = 0.02\ \mu F$), and the inductor is selected to be 330 μH. Feedback resistors R1 and R2 set the output voltage. The required output capacitance is calculated to be

$$C_O = I_p \times \frac{t_{on} + t_{off}}{8 \times V_{peak\ ripple}} = 1 \times \frac{20 \times 10^{-6} + 60 \times 10^{-6}}{(8) \times 25 \times 10^{-3}} = 400\ \mu F$$

Efficiency of this circuit may be calculated from

$$\text{Efficiency} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{\frac{V_{OUT} + V_D}{V_{IN} - V_S + V_D} + \frac{I_Q}{\%\ \text{Full Load}}}\right)$$

where I_Q is the device quiescent current.

For full load, efficiency is

$$\left(\frac{5}{24}\right) \times \left(\frac{1}{\frac{5+1}{24-1+1} + \frac{2 \times 10^{-3}}{1}}\right) = 83\%$$

For 10% of full load, efficiency becomes

$$\left(\frac{5}{24}\right) \times \left(\frac{1}{\frac{5+1}{24-1+1} + \frac{2 \times 10^{-3}}{0.1}}\right) = 77\%$$

Notice that low standby power helps to maintain high efficiency even under light load conditions.

(2) The regulator is connected as a step-up voltage regulator in Fig 4. Design goals are $V_{IN} = 5$ V, $V_{OUT} = 15$ V, $I_{OUT\ MAX} = 150$ mA, and output ripple less than 25 mV. Using $V_S = 0.5$ V and $V_D = 1$ V, the on-to-off-time ratio is calculated as

$$t_{on}/t_{off} = \frac{15 + 1 - 5}{5 - 0.5} = \frac{11}{4.5} = 2.44$$

C_T is chosen to be 0.01 μF, setting the off-time to 30 μs; thus, on-time is approximately 73 μs. An 80-Ω resistor is used in the driver collector to provide 50-mA base drive to the switch. Peak input current is 1.1 A, so R_{SC} is set to 0.33 Ω. Average input current is 555 mA at full load for an efficiency of 80%. At 10% of full load, efficiency becomes 78%. The required output capacitor is calculated as

$$C_O = \frac{(I_p - I_{OUT})^2}{2I_p} \times \frac{t_{off}}{V_{peak\ ripple}}$$

$$C_O = \frac{(1.1 - 0.15)^2}{2\ (1.1)} \times \frac{30 \times 10^{-6}}{25 \times 10^{-3}} = 492\ \mu F$$

(3) With the voltage inverter in Fig 5, an external pnp transistor (Q3) and catch diode (D2) are required

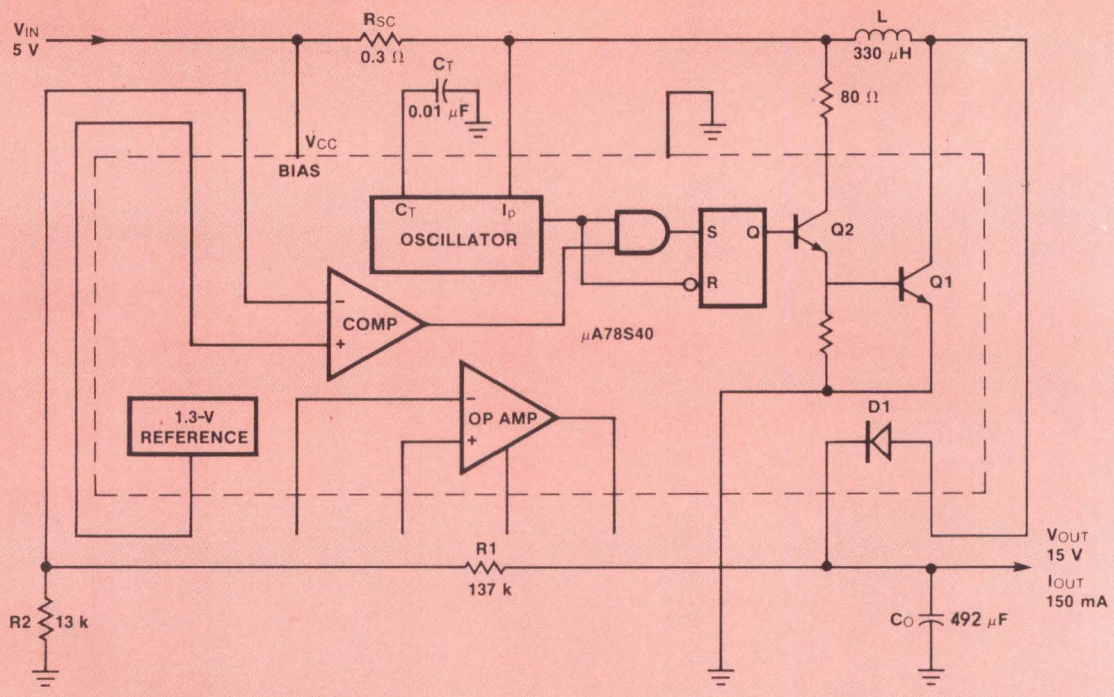

Fig 4 Step-up voltage regulator. Common configuration using only seven external parts transforms 5 V to 15 V at efficiency of 80% under full load (150 mA). Average input current is only 550 mA. Output voltage ripple of 25 mA could be reduced even more by increasing C_o

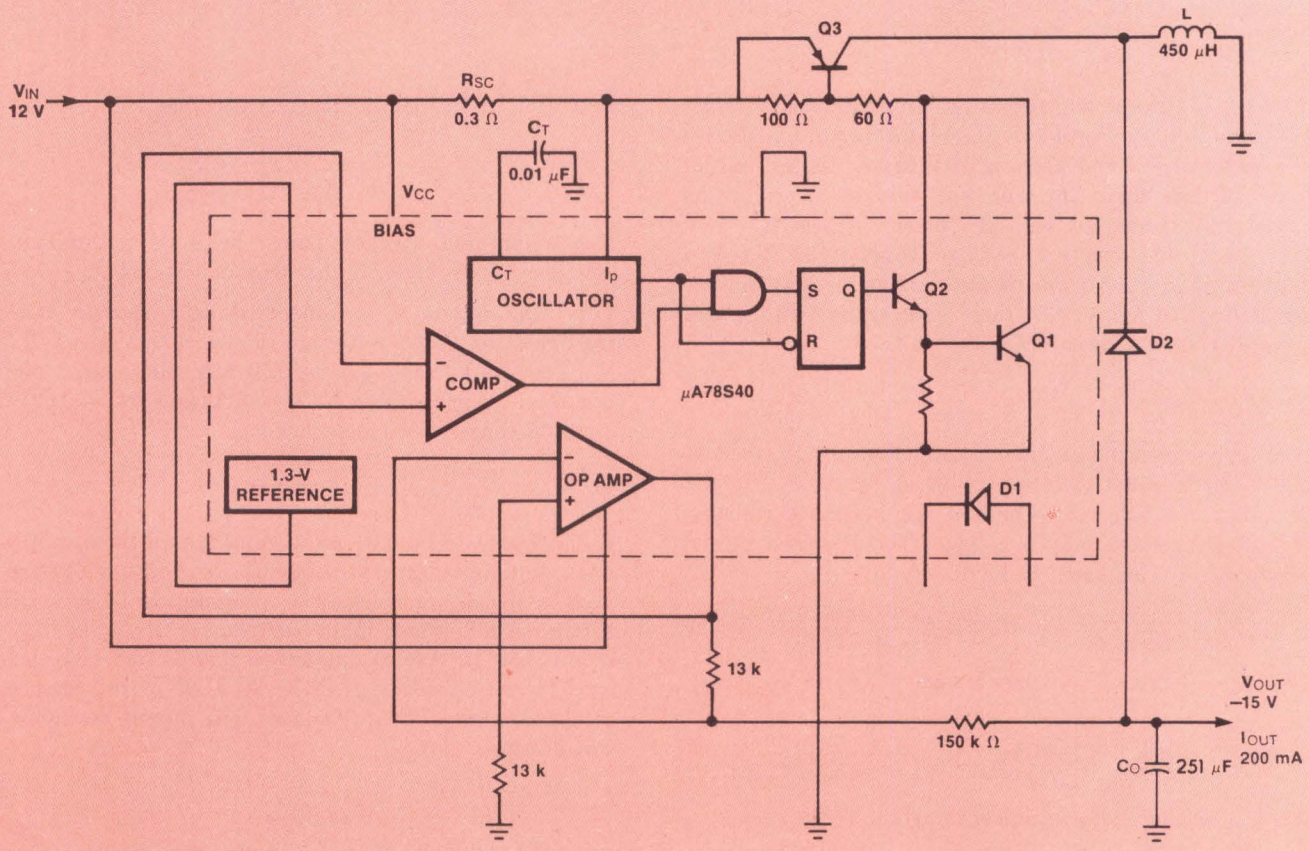

Fig 5 Inverting voltage regulator. Application requires additional pnp transistor and diode so that IC subsystem never sees voltage that is negative with respect to ground. Circuit provides output voltage of −15 V for input voltage of 12 V. Efficiency of power conversion is 84% with 200-mA load. Output voltage ripple of 50 mV can be reduced by increasing value of C_o

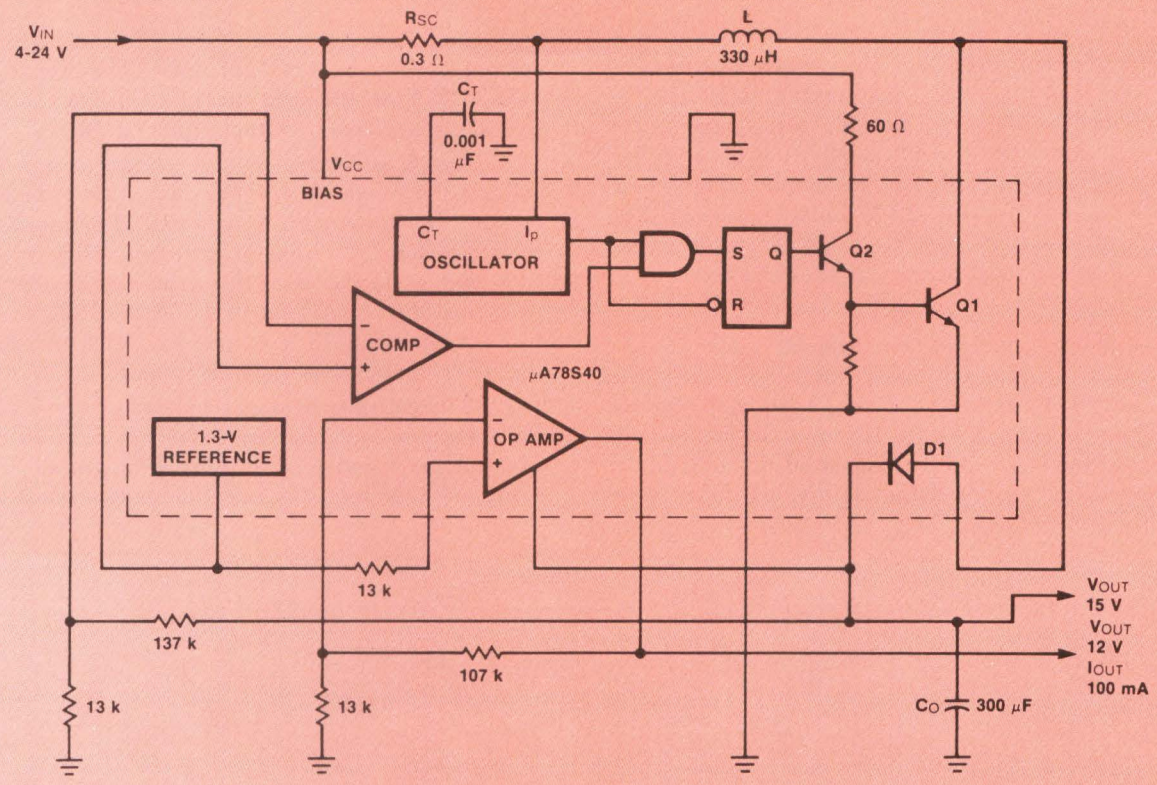

Fig 6 Constant output voltage regulator. Unusual requirement—regulator for 4- to 24-V input range—is implemented easily in step-up configuration with uncommitted op amp used as series-pass device

so that no pin of the IC sees a voltage more negative than the substrate (common). Input is 12 V, output is −15 V at 200 mA, and ripple must be less than 50 mV. The timing ratio is

$$\frac{t_{on}}{t_{off}} = \frac{(|V_{OUT}| + V_D)}{V_{IN} - V_S} = \frac{15 + 1.0}{12 - 0.5} = \frac{16}{11.5} = 1.39$$

Again, if using $C_T = 0.01\ \mu F$, then $t_{off} = 30\ \mu s$ and $t_{on} = 41.7\ \mu s$. The required peak current is

$$I_p = \frac{I_{OUT\ MAX}\ (V_{IN} + |V_{OUT}| + V_D - V_S)\ 2}{(V_{IN} - V_S)}$$

$$I_p = \frac{0.2\ (12 + 15 + 1 - 0.5)\ 2}{12 - 0.5} = 0.96\ A$$

Thus, $R_{SC} = 0.33\ \Omega$

and $L = \frac{V_{IN} - V_S}{I_p} \times t_{on} = 450\ \mu H.$

Average input current is 275 mA; efficiency is 84% at 100% load and 77% at 10% load. Output ripple is held to 50 mV by

$$C_o = \frac{(I_p - I_{OUT})^2}{2I_p} \times \frac{t_{off}}{V_{peak\ ripple}}$$

$$C_o = -\frac{(0.96 - 0.2)^2}{1.92} \times \frac{41.7 \times 10^{-6}}{50 \times 10^{-3}} = 251\ \mu F$$

Note that the uncommitted op amp is used in the latter application to invert the output voltage in order to compare it with the 1.3-V reference. This can be accomplished only because the common mode range of the op amp includes ground. No portion of the control circuit sees negative voltage; therefore, IC breakdown does not limit the output voltage.

Advanced Applications

Connection of the μA78S40 to additional external components can obtain output power up to 100 W and output voltages in excess of 100 V. Two regulated outputs are available when using a switching and a series-pass output. Some advanced application examples are included.

(1) A universal regulator, whose output voltage is constant for inputs both less than and greater than the output, is shown in Fig 6. The output voltage desired is 12 V at 100 mA for V_{IN} from 4 to 24 V. This is accomplished by generating a stepped-up output voltage of 15 V using a step-up regulator similar to that in Fig 4, and then reducing the 15 V using the uncommitted op

amp as a series-pass, 12-V regulator. When V_{IN} exceeds 16 V, the step-up regulator follows the input and is approximately V_{IN} — 1 V, but the series-pass output remains a constant 12 V. Additionally, the op amp has excellent noise rejection so that the output ripple is essentially eliminated at the 12-V output. Efficiency is about 50% for V_{IN} = 4 V or V_{IN} = 24 V, and increases for other voltages to a maximum of about 75%.

(2) A dual-tracking regulator can be built to give ±15 V out from a single 20-V input (Fig 7). The negative supply is generated using a voltage inverter circuit similar to that in Fig 5. However, in this circuit, the uncommitted op amp is connected in a gain of −1 configuration, and its output is divided down to be compared with the 1.3-V reference. The circuit can provide ±15 V at 100 mA, at 80% efficiency (75% positive, 85% negative). Output ripple is 30 mV.

(3) Fig 8 indicates a dual, high output regulator featuring a single 5-V input that gives 12- and 15-V outputs. In this circuit, an external npn transistor (Q3) is used to boost the step-up regulator, while another npn transistor (Q4) increases the series-pass regulator output in excess of 1 A. A total of 1.5 A is available from the two outputs. The 15-V output has 80% efficiency, and the 12-V output has 64% efficiency.

(4) A negative-switching regulator is more difficult to build because the reference voltage is referred to $-V_{IN}$, which is the negative input rather than ground. To obtain a ground reference, the uncommitted op amp shown in

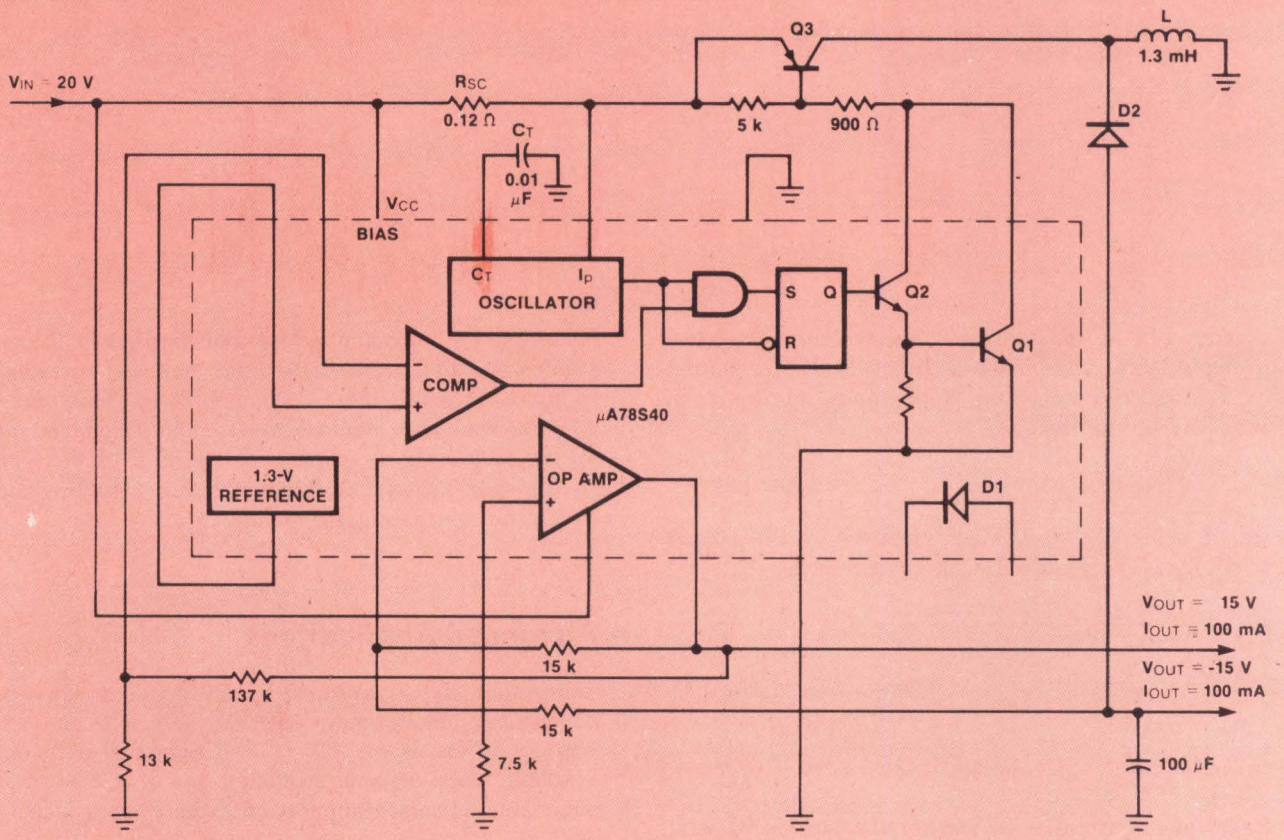

Fig 7 Dual-tracking supply. Device may be produced from single positive supply using voltage inverter mode and operating available op amp with gain of −1. For circuit shown, ±15 V is derived from single 20-V supply and can provide 100 mA at each of its outputs

Fig 9 is used to invert the reference with a differential amplifier configuration in order to generate a −2.6-V ground reference. A standard step-down regulator is then constructed. For −48 V in, −12 V out, and 300 mA load current, an efficiency of 86% can be achieved.

Summary

This IC subsystem is intended to be used as the control circuit for switching regulators in the low to medium power range. Its flexibility is shown by the wide variety of applications ranging from standard low power, minimum-parts-count type of operation for step-up (output greater than input), step-down (output less than input), and inversion (output of opposite polarity to input), to the more complex, high power applications for the same operating modes. These high power applications require more care in their design because of the large peak switching currents that are involved. Similarly, more careful selection of external components to be used in these applications is required. A circuit described has an input voltage range that includes values both greater than and less than the output voltage range, and requires the addition of only three external components (two resistors and a capacitor) to the minimum-part step-up application.

Versatility of this part is making switching regulator power supply subsystems easier and less expensive to design. Advantages are lower costs and less heat dissipa-

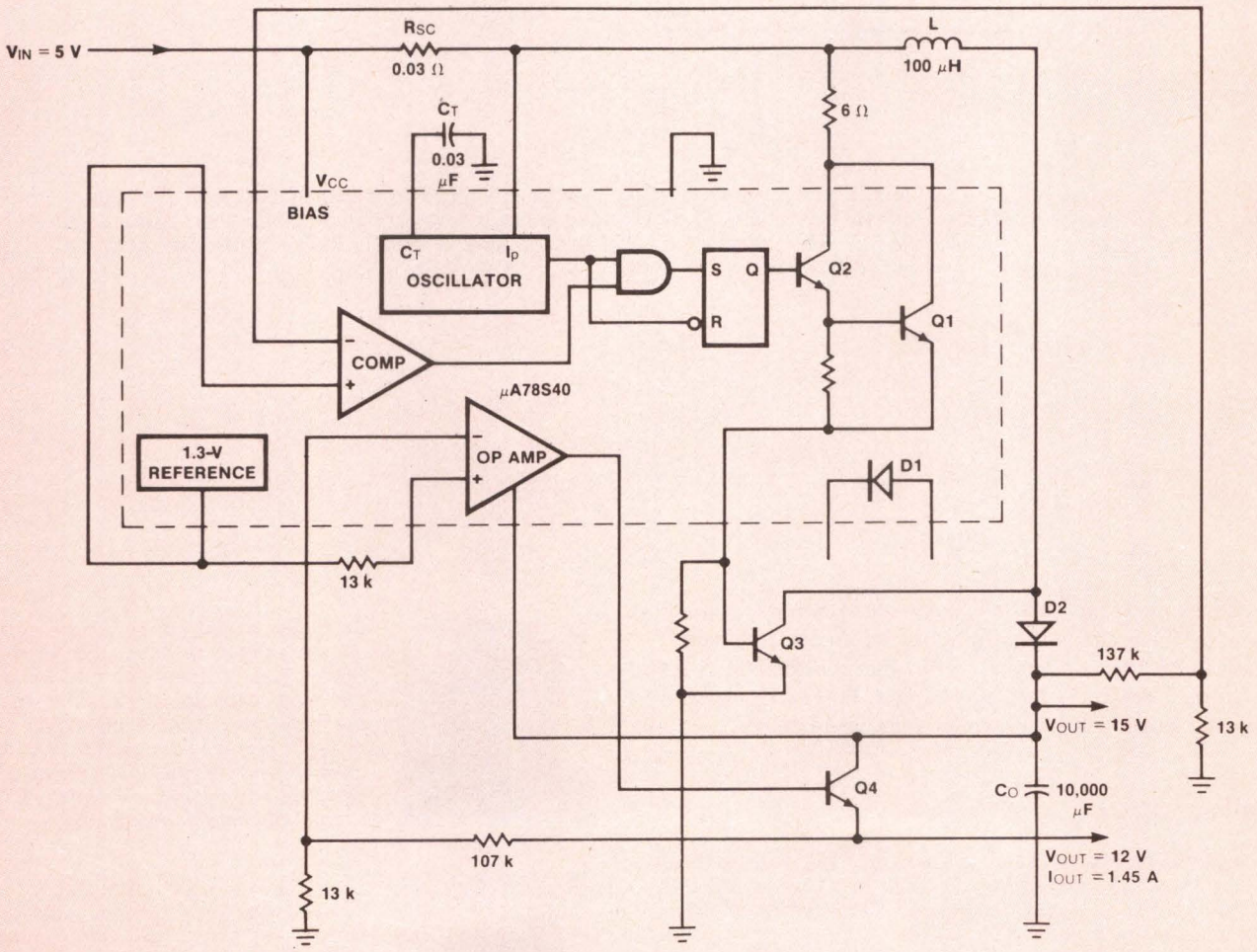

Fig 8 Step-up and series-pass regulator. Two positive output voltages of different magnitude, both of which are greater than input voltage, are accomplished because of available op amp. 5-V supply is first stepped-up to 15 V in usual manner, and op amp then is used to drive external series-pass device to produce 12-V output. Both outputs are capable of 1.45-A load current. Efficiency of transformation to 15 V is 80% while that to 12 V is 64%. Output voltage ripple on 15-V output is 300 mV

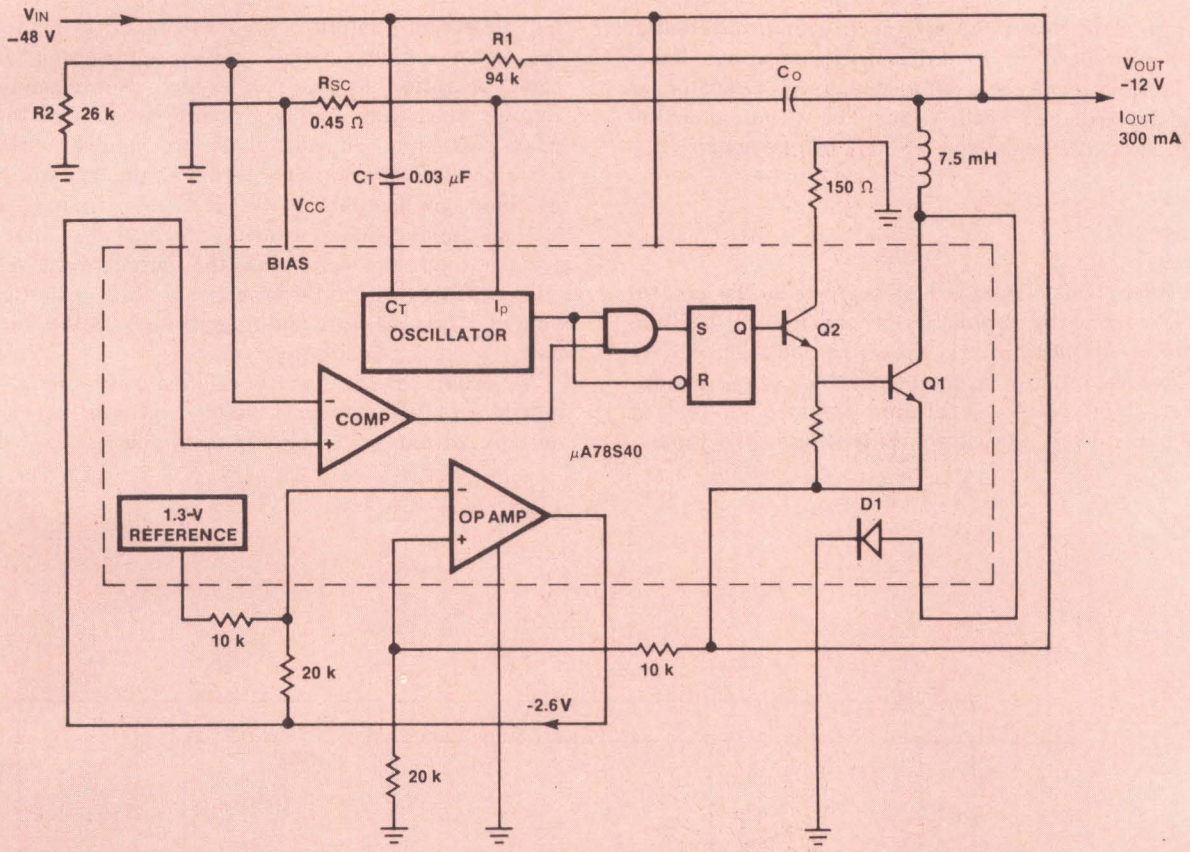

Fig 9 Negative I/O regulator. Negative output voltage may be produced from negative supply. For this circuit, −48 V is transformed to −12 V at efficiency of 86% and is capable of providing 300-mA load current. Output voltage ripple is 300 mV. In this configuration, available op amp is used to derive −2.6-V reference voltage from internal 1.3-V reference

tion resulting from high efficiency operation, and longer operating times for battery-operated equipment. However, the designer must contend with the disadvantages of slow transit response to load changes, output ripple, and increased noise over series-pass type regulators.

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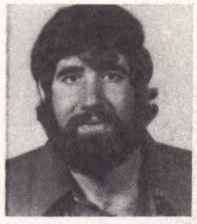
E. T. Moore and T. G. Wilson, "Basic Considerations for DC to DC Conversion Networks," *IEEE Transactions on Magnetics*, Sept 1966, pp 620-624



Currently employed as linear applications manager at Advanced Micro Devices, Russell Apfel formerly served in the same capacity at Fairchild. His experience has included managing of industrial product design for the linear division, with responsibility for op amps, comparators, voltage regulators, and special industrial products.

David Jones is a design engineer for Fairchild's Linear Division, Industrial Products group. His background includes work in the voltage regulator line as well as special industrial and consumer products. He received a BS degree in electrical engineering from California State University, San Jose.

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Questions should be addressed directly to the course instructors, David G. Larsen (703) 951-6478, Dr. Peter R. Rony (703) 951-6370 or Dr. Paul E. Field, (703) 951-5376.

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APPLICATION NOTE

Computer Simulation Program for a Second Generation Handheld Calculator

Running iterative computer simulations on a programmable handheld calculator is economical and convenient. Interactive capabilities of the computer model, with its prompting messages and labeled results, further simplify simulation and comparison of alternative computer designs

Ronald Zussman Securities Industry Automation Corporation, New York, New York

A complete computer simulation package, presented for the handheld calculator user, evaluates alternative computer system designs by comparing the quantitative performance measures of utilization, throughput, and response time. This generalized, fast, and interactive program can be applied to sizing new applications, projecting performance over a system's life cycle, and arriving at an optimum balance of system resources. Thus, simulations can be iterated to discover the degree to which system design parameters should be changed.

A program and background material for simulating a large class of computer systems on Texas Instruments' SR-52 pocket calculator were presented in a previous issue of *Computer Design*.[1] Since then, a second generation TI-59 calculator and companion PC-100A printer have been produced. This note, therefore, lists the code for running an enhanced computer simulation program on the TI-59, and at the same time demonstrates the current state-of-the-art in calculator capability via a real application. The convenience and portability afforded by the calculator, coupled with the printer's alphanumeric prompting and labeled results, make calculator simulations easier to run than a FORTRAN implementation written for a large time-sharing computer. Since calculator processing and connect times are essentially free, operating costs are also minimal.

Programming the Calculator

A total of 960 bytes of RAM in the TI-59 can be partitioned between instruction locations and data registers. Only one byte is required by each program step, while data registers take eight bytes apiece. The Computer Simulation Program (see Panel) allocates 480 bytes each for instructions and for data registers (ie, 480 program locations and 60 data registers).

To program the calculator, turn it on and enter the learn mode by pressing the LRN key; then, enter keystrokes shown under the program listing. The calculator provides for editing and correcting of mistakes.[2] Load data registers 12 through 59 with numbers listed at the bottom of the program. These are numeric representations for alphabetic messages that will be printed during subsequent executions. For example, in deciphering contents of register

Simulation Examples

(A)
```
*COMPUTER SIMULATION
*INPUT 8 PARAMETERS—
CPU ACTIVE TIME?
          1534.
NO. JOBS RUN?
         10228.
NO. IO'S?
        219164.
MEAN IO TIME?
          0.05
MULTIPROGRAM LEVEL?
             8.
NO. USERS?
           150.
USER THINK-TIME?
            10.
MULTIPROCESS LEVEL?
             1.
REG. 1-7
 .1499804458      C↑
 .0069993247      C
        0.05      I
           8.     M↑
         150.     N↑
          10.     Z↑
           1.     J
*COMPUTER SIMULATION
*CONSTANT MODEL
CPU UTIL. =
     98.2373      U(C)
THRUPUT =
      6.5500      T
RESPONSE TIME =
     12.9007      R
*EXPONENTIAL MODEL
CPU UTIL. =
     81.2927      U(E)
THRUPUT =
      5.4202      T
RESPONSE TIME =
     17.6742      R
```

(B)
```
*COMPUTER SIMULATION
*INPUT 8 PARAMETERS—
CPU ACTIVE TIME?
          1534.
NO. JOBS RUN?
         10228.
NO. IO'S?
        219164.
MEAN IO TIME?
          0.05
MULTIPROGRAM LEVEL?
             8.
NO. USERS?
           150.
USER THINK-TIME?
            10.
MULTIPROCESS LEVEL?
             2.
REG. 1-7
 .1499804458      C↑
 .0069993247      C
        0.05      I
           8.     M↑
         150.     N↑
          10.     Z↑
           2.     J
*COMPUTER SIMULATION
*CONSTANT MODEL
CPU UTIL. =
     49.1187      U(C)
THRUPUT =
      6.5500      T
RESPONSE TIME =
     12.9007      R
*EXPONENTIAL MODEL
CPU UTIL. =
     48.1347      U(E)
THRUPUT =
      6.4188      T
RESPONSE TIME =
     13.3689      R
```

(C)
```
*COMPUTER SIMULATION
*INPUT 8 PARAMETERS—
CPU ACTIVE TIME?
          1534.
NO. JOBS RUN?
         10228.
NO. IO'S?
        219164.
MEAN IO TIME?
          0.05
MULTIPROGRAM LEVEL?
            16.
NO. USERS?
           150.
USER THINK-TIME?
            10.
MULTIPROCESS LEVEL?
             2.
REG. 1-7
 .1499804458      C↑
 .0069993247      C
        0.05      I
          16.     M↑
         150.     N↑
          10.     Z↑
           2.     J
*COMPUTER SIMULATION
*CONSTANT MODEL
CPU UTIL. =
     98.2373      U(C)
THRUPUT =
     13.1000      T
RESPONSE TIME =
      1.4504      R
*EXPONENTIAL MODEL
CPU UTIL. =
     86.1048      U(E)
THRUPUT =
     11.4821      T
RESPONSE TIME =
      3.0638      R
```

12, code 51 represents an *, 15 represents a C, 32 represents an O, and so on. Data registers 0 through 11 are initially 0, and later contain variables used during computations.

Once the program listing and prestored data registers are entered and double-checked for accuracy, the contents of the entire RAM are written on two magnetic cards for subsequent use.[2] The first card will contain the program listing; the second card, data registers. To run a computer simulation, read these two cards into the calculator and proceed with the user instructions that follow. When the calculator is used without a printer, read only the first magnetic card.

User Instructions

The same user instructions listed for the SR-52 in the referenced article[1] may be followed. After storing

Simulation Examples, continued

(D)
```
*COMPUTER SIMULATION
*INPUT 8 PARAMETERS—
CPU ACTIVE TIME?
767.
NO. JOBS RUN?
10228.
NO. IO'S?
219164.
MEAN IO TIME?
0.05
MULTIPROGRAM LEVEL?
8.
NO. USERS?
150.
USER THINK-TIME?
10.
MULTIPROCESS LEVEL?
1.
REG. 1-7
.0749902229   C↑
.0034996624   C
0.05          I
8.            M↑
150.          N↑
10.           Z↑
1.            J
*COMPUTER SIMULATION
*CONSTANT MODEL
CPU UTIL. =
52.3317       U(C)
THRUPUT =
6.9785        T
RESPONSE TIME =
11.4947       R
*EXPONENTIAL MODEL
CPU UTIL. =
50.0959       U(E)
THRUPUT =
6.6803        T
RESPONSE TIME =
12.4540       R
```

(E)
```
*COMPUTER SIMULATION
*INPUT 8 PARAMETERS—
CPU ACTIVE TIME?
1534.
NO. JOBS RUN?
20456.
NO. IO'S?
438328.
MEAN IO TIME?
0.05
MULTIPROGRAM LEVEL?
8.
NO. USERS?
150.
USER THINK-TIME?
10.
MULTIPROCESS LEVEL?
1.
REG. 1-7
.0749902229   C↑
.0034996624   C
0.05          I
8.            M↑
150.          N↑
10.           Z↑
1.            J
*COMPUTER SIMULATION
*CONSTANT MODEL
CPU UTIL. =
52.3317       U(C)
THRUPUT =
6.9785        T
RESPONSE TIME =
11.4947       R
*EXPONENTIAL MODEL
CPU UTIL. =
50.0959       U(E)
THRUPUT =
6.6803        T
RESPONSE TIME =
12.4540       R
```

(F)
```
*COMPUTER SIMULATION
*INPUT 8 PARAMETERS—
CPU ACTIVE TIME?
1534.
NO. JOBS RUN?
20456.
NO. IO'S?
438328.
MEAN IO TIME?
0.05
MULTIPROGRAM LEVEL?
8.
NO. USERS?
150.
USER THINK-TIME?
10.
MULTIPROCESS LEVEL?
2.
REG. 1-7
.0749902229   C↑
.0034996624   C
0.05          I
8.            M↑
150.          N↑
10.           Z↑
2.            J
*COMPUTER SIMULATION
*CONSTANT MODEL
CPU UTIL. =
26.1659       U(C)
THRUPUT =
6.9785        T
RESPONSE TIME =
11.4947       R
*EXPONENTIAL MODEL
CPU UTIL. =
26.0878       U(E)
THRUPUT =
6.9577        T
RESPONSE TIME =
11.5590       R
```

seven fundamental parameters (C, c, i, M, N, Z, j) in data registers 1 through 7, the user can request CPU utilization by pressing either key A (Ue) for the exponential model, or key B (Uc) for the constant model. To display throughput (T) press key C, and for response time (R), press D. If the calculator is operating independently, these results are displayed only on its LEDs. However, when the printer is attached, results and identifying mnemonics are also automatically printed.

With an attached printer, the user has the added option of pressing key E for prompting; the calculator then directs questions in the form of printed messages. After each entry the user presses the R/S key to proceed. When all eight questions are answered, contents of data registers 1 through 7 are automatically computed, loaded, and printed. Pressing key D′ at any time prints out the contents of these data registers, along with the mnemonic code for each of the seven fundamental parameters stored there. Since only capital letters can be printed, normally upper case letters are followed by an upward arrow when necessary. Pressing key E′ initiates simulations and prints labeled results. Calculator and user interactions are further illustrated in the Simulation Examples.

Applying Simulation

Simulation predicts the effect of prospective design changes on computer system performance. This application

```
G) *COMPUTER SIMULATION
*INPUT 8 PARAMETERS—
CPU ACTIVE TIME?
        1534.
NO. JOBS RUN?
        10228.
NO. IO'S?
        219164.
MEAN IO TIME?
        0.019
MULTIPROGRAM LEVEL?
        8.
NO. USERS?
        150.
USER THINK-TIME?
        10.
MULTIPROCESS LEVEL?
        2.
REG. 1-7
   .1499804458      C↑
   .0069993247      C
         0.019      I
            8.     M↑
          150.     N↑
           10.     Z↑
            2.      J
*COMPUTER SIMULATION
*CONSTANT MODEL
CPU UTIL. =
        107.6847    U(C)
THRUPUT =
        13.3351      T
RESPONSE TIME =
         1.2485      R
*EXPONENTIAL MODEL
CPU UTIL. =
         88.1788    U(E)
THRUPUT =
         11.7587      T
RESPONSE TIME =
          2.7565      R
```

```
(H) *COMPUTER SIMULATION
*INPUT 8 PARAMETERS—
CPU ACTIVE TIME?
        1534.
NO. JOBS RUN?
        10228.
NO. IO'S?
        219164.
MEAN IO TIME?
        0.05
MULTIPROGRAM LEVEL?
        8.
NO. USERS?
        375.
USER THINK-TIME?
        10.
MULTIPROCESS LEVEL?
        1.
REG. 1-7
   .1499804458      C↑
   .0069993247      C
         0.05       I
            8.     M↑
          375.     N↑
           10.     Z↑
            1.      J
*COMPUTER SIMULATION
*CONSTANT MODEL
CPU UTIL. =
         98.2373    U(C)
THRUPUT =
          6.5500      T
RESPONSE TIME =
         47.2518      R
*EXPONENTIAL MODEL
CPU UTIL. =
         81.2927    U(E)
THRUPUT =
          5.4202      T
RESPONSE TIME =
         59.1854      R
```

```
(I) *COMPUTER SIMULATION
*INPUT 8 PARAMETERS—
CPU ACTIVE TIME?
        1534.
NO. JOBS RUN?
        10228.
NO. IO'S?
        219164.
MEAN IO TIME?
        0.05
MULTIPROGRAM LEVEL?
        8.
NO. USERS?
        150.
USER THINK-TIME?
        20.
MULTIPROCESS LEVEL?
        1.
REG. 1-7
   .1499804458      C↑
   .0069993247      C
         0.05       I
            8.     M↑
          150.     N↑
           20.     Z↑
            1.      J
*COMPUTER SIMULATION
*CONSTANT MODEL
CPU UTIL. =
         98.2373    U(C)
THRUPUT =
          6.5500      T
RESPONSE TIME =
          2.9007      R
*EXPONENTIAL MODEL
CPU UTIL. =
         81.2927    U(E)
THRUPUT =
          5.4202      T
RESPONSE TIME =
          7.6742      R
```

is illustrated with nine simulations. Example A is a validation benchmark while each of the remaining eight examples explores the effects of varying system parameters.

An existing uniprocessor system was monitored for a half-hour period (1800 s) and its performance measurement data were input to the simulation in Example A. CPU utilization during that time averaged 85.22%, which means that the CPU was active for 1534 s (1800 x 85.22%). A total of 10,228 messages were processed through the computer at a rate of 5.68 messages/s, and 219,164 disc I/Os were measured. According to the manufacturer's hardware specifications, an average disc access (mean I/O time) is 50 ms. With 150 inquiry terminals connected to the system, the computer was running a real-time application with eight copies of the program active in main memory. After receiving a response, operators spent an average of 10 s in contemplation before inputting their new inquiry.

To obtain the simulation printout for Example A merely press key E, answer the prompting questions, and then press key E′. Both constant and exponential models are automatically run and their results printed and labeled. These two models provide upper and lower bounds for CPU utilization, throughput, and response time, with real system performance lying between these constraints.

Example B indicates that adding another processor without simultaneously increasing main memory

Computer Simulation Program

Partition: 479.59

Program Listing:

```
000: Lbl A' STO 8 ( x=t 15 RCL 8 x Dsz 8 005 1 ) INV SBR
018: Lbl B' STO 9 Lbl C' Op 0 RCL Ind 9 Op 1 Op 29 RCL Ind 9
034: Op 2 Op 29 Iffig 2 Iffig RCL Ind 9 Op 3 Op 29 Iffig 3
049: Iffig RCL Ind 9 Op 4 Op 29 Lbl Iffig Op 5 CLR INV Stflg 2
064: INV Stflg 3 INV SBR INV Stflg 0 STO 0 ( ( RCL 2 ÷ RCL 3
080: ÷ RCL 7 ) y^x RCL 0 STO 11 x RCL 7 STO 10 INV SUM 11 y^x
098: RCL 11 x≥t 107 RCL 0 STO 10 RCL 10 Iffig 0 116 x RCL 11 ÷ (
118: RCL 4 − RCL 0 ) A' ÷ RCL 10 A' + Dsz 0 74 RCL 4 A' 1/x
138: Iffig 0 146 x RCL 7 +/− ) INV SBR Lbl A CP 2 0 4 1 5 5 1 7 5 6
161: Op 4 RCL 7 SBR 68 ÷ RCL 4 SBR 69 ÷ RCL 7 + 1 = STO 0
182: x 1 0 0 = Fix 4 Op 6 INV SBR Lbl C 3 7 Op 4 SBR Inx GTO 187
203: Lbl Inx RCL 0 − 1 = INV x≥t 215 0 + 1 = x RCL 7 ÷ RCL 1 =
225: INV SBR Lbl D 3 5 Op 4 SBR Inx 1/x x RCL 5 − RCL 6 GTO 186
244: Lbl B CP 2 0 4 1 5 5 1 5 5 6 Op 4 RCL 4 ÷ RCL 7 ÷ ( RCL 3
268: ÷ RCL 2 GTO 177 Lbl E INV Fix Adv 1 2 B' C' Adv C' R/S Prt
287: STO 1 STO 2 Stflg 3 C' R/S Prt INV Prd 1 Stflg 2 C' R/S
303: Prt INV Prd 2 Stflg 3 C' R/S Prt STO 3 C' R/S Prt STO 4
319: Stflg 2 C' R/S Prt STO 5 Stflg 4 C' R/S Prt STO 6 C' R/S
335: Prt STO 7 Lbl D' INV Fix Adv Op 00 3 5 1 7 2 2 4 0 0 0 Op 01
357: 0 2 2 0 1 0 0 0 0 0 Op 2 Op 05 1 5 6 0 Op 4 RCL 1 Op 06 1
382: 5 Op 4 RCL 2 Op 06 2 4 Op 4 RCL 3 Op 06 3 0 6 0 Op 4
403: RCL 4 Op 06 3 1 6 0 Op 4 RCL 5 Op 06 4 6 6 0 Op 4 RCL 6
424: Op 06 2 5 Op 4 RCL 7 Op 6 R/S Lbl E' Adv 1 2 B' Adv
443: Stflg 3 4 6 B' Stflg 2 C' B Stflg 2 C' C Stflg 3 C' D Adv 5 6
463: B' Stflg 2 4 9 B' A Stflg 2 C' C Stflg 3 C' D R/S
```

Prestored Data Registers:

```
12: 5115323033 4137173500 3624304127 1337243231 5124313341 3700110033
18: 1335133017 3717353620 1533410013 1537244217   37243017 7100000000
24: 3132400025 3214360035 4131710000 3132400024 3265367100 3017133100
30: 2432003724 3017710000 3041273724 3335322235 1330002717 4217277100
36: 3132400041 3617353671 4136173500 3723243126 2037243017 7100000000
42: 3041273724 3335321517 3636002717 4217277100 5115323136 3713313700
48: 3032161727 1533410041 3724274064 3723354133 4137640000 3517363332
54: 3136170037 2430176400 5117443332 3117313724 1327003032 1617270000
```

would be fruitless; although CPU utilization drops, neither throughput nor response time substantially changes. However, according to Example C, main memory capacity can be doubled to allow 16 copies of the program to reside simultaneously. Throughput then approximately doubles and response time decreases significantly. Both conditions improve system performance for users.

If the original uniprocessor were replaced with a machine that computes twice as fast, the result would be as illustrated in Examples D and E. In Example D a half-hour time period is considered, while in Example E a one-hour time period is selected. Naturally, both give the same results. Compared with Example A, both response time and throughput show improvement. Resorting to multiprocessing by adding a second fast machine is not cost-effective, according to Example F, because enhancements to throughput and response time performance are minimal.

The 50-ms disc used in Example B is replaced with a faster 19-ms model in Example G. Comparing results of Examples G with C establishes that greater improvement is obtained by using the faster disc than by doubling memory capacity. Note that CPU utilization for the constant model in Example G prints out as 107.6847%. Constant model CPU utilizations greater than 100% appear to indicate the degree of possible overload.

The number of terminals in Example H has been expanded from 150 to 375. Comparing these results with Example A shows only increased response time. Similarly, longer user think time in Example I results in shortened response time.

Conclusions

Practical applications of analytic models to computer design are difficult to locate.[3] Although they have proven popular with theoretical academicians in exercising high level "state space" mathematics, these models have rarely been translated to a practical form. Implementing the general-purpose interactive calculator simulation program for a Markov central-site analytic queuing model is easy and inexpensive. Nine illustrative examples demonstrate the program's viability as a practical tool for predicting computer performance, locating potential system bottlenecks, and fine-tuning the system.

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3. J. W. Boyse and D. R. Warn, "A Straightforward Model for Computer Performance Prediction," *ACM Computing Surveys*, June 1975, pp 73-79

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CIRCLE 52 ON INQUIRY CARD

DESIGN NOTE

Hardware/Software for Process Control I/O

Two address mapping modes for connecting real-time I/O peripherals in a microprocessor-based control application are examined to determine hardware and software criteria for efficient data processing

A. D. Marathe and A. K. Chandra Bhabha Atomic Research Centre, Bombay, India

Digital input and output hardware units, when implemented in microprocessor-based process control systems, may be used in isolated and memory-mapped input/output modes. The software programs of each memory-mapping mode require varying amounts of memory, hardware, and execution time, providing designers with suitable criteria for selecting the correct mapping mode for a specific hardware unit.

Digital Input Unit

An 8080 microprocessor has input/output (I/O) address space distinct from memory address space. Consequently, it is possible to connect a digital input unit (DIU) as either an isolated or a memory-mapped I/O device (Fig 1). For isolated I/O (Fig 1, Block A), the I/O channel provides an 8-bit address bus (lines A7 through A0). During an I/O instruction (ie, IN or OUT), the address of one of 256 ports is placed on these lines for decoding. Lines BD7 through BD0 constitute an 8-bit bidirectional data bus. During execution of an IN instruction, the microprocessor generates an I/O read ($\overline{\text{IOR}}$) control pulse, causing data content of the addressed port to be placed on the data bus.

To address 64 input ports, which is a sufficient requirement for most medium-sized process control applications, the DIU can be referenced when the port address specified in the IN instruction is 11 XXX XXX. The latter six bits specify any one of 64 input ports, implying a total capacity of 64 x 8 or 512 discrete input signals. In Fig 1, the DIU accepts 32 digital inputs organized as four groups of eight—D31 to D24, D23 to D16, D15 to D8, and D7 to D0. The most significant bits of each group (D31, D23, D15, and D7) are presented to the first four-to-one line data multiplexer, the next more significant bits (D30, D22, D14, and D6) to the second multiplexer, and so on. For isolated I/O, address lines A7 and A6 are ANDed to generate a digital input enable (DIEN) signal. Address lines A5 through A2 are decoded to obtain 16 signals, each being gated with DIEN to enable a group of four ports. Address lines A1 and A0 are fed directly to multiplexers and decoded internally. When either of the enclosed (dotted) blocks is enabled by address selection logic, specific data appearing at the output of selected multiplexers correspond to those indicated by A1 and A0 lines. Data corresponding to the selected port are strobed onto the microprocessor data bus by the $\overline{\text{IOR}}$ pulse.

If the microprocessor executes IN instruction 11 000 001, this port address indicates that data to be accessed are available at the second group of four ports in the first of 16 similar sets. Accordingly, data in-

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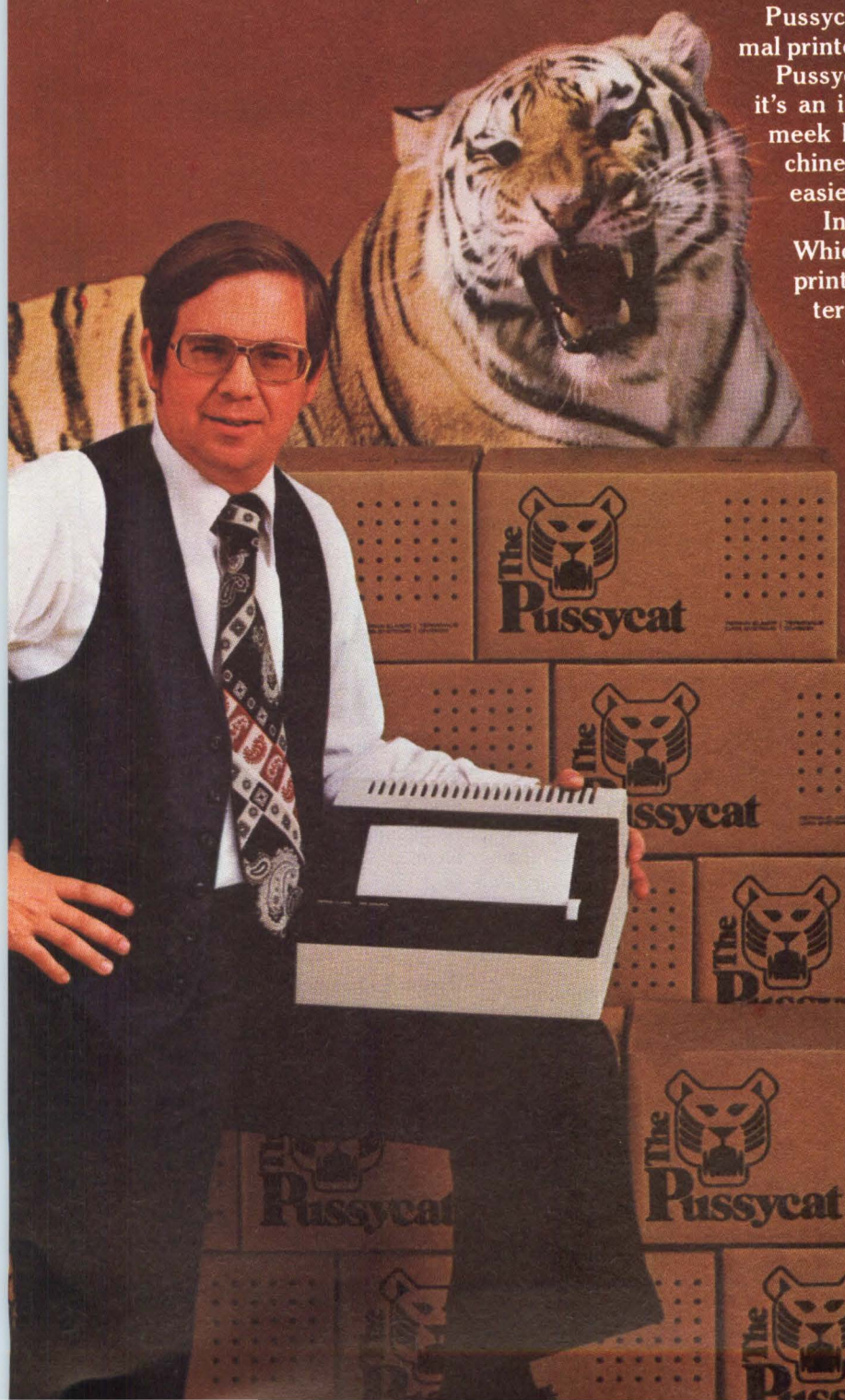

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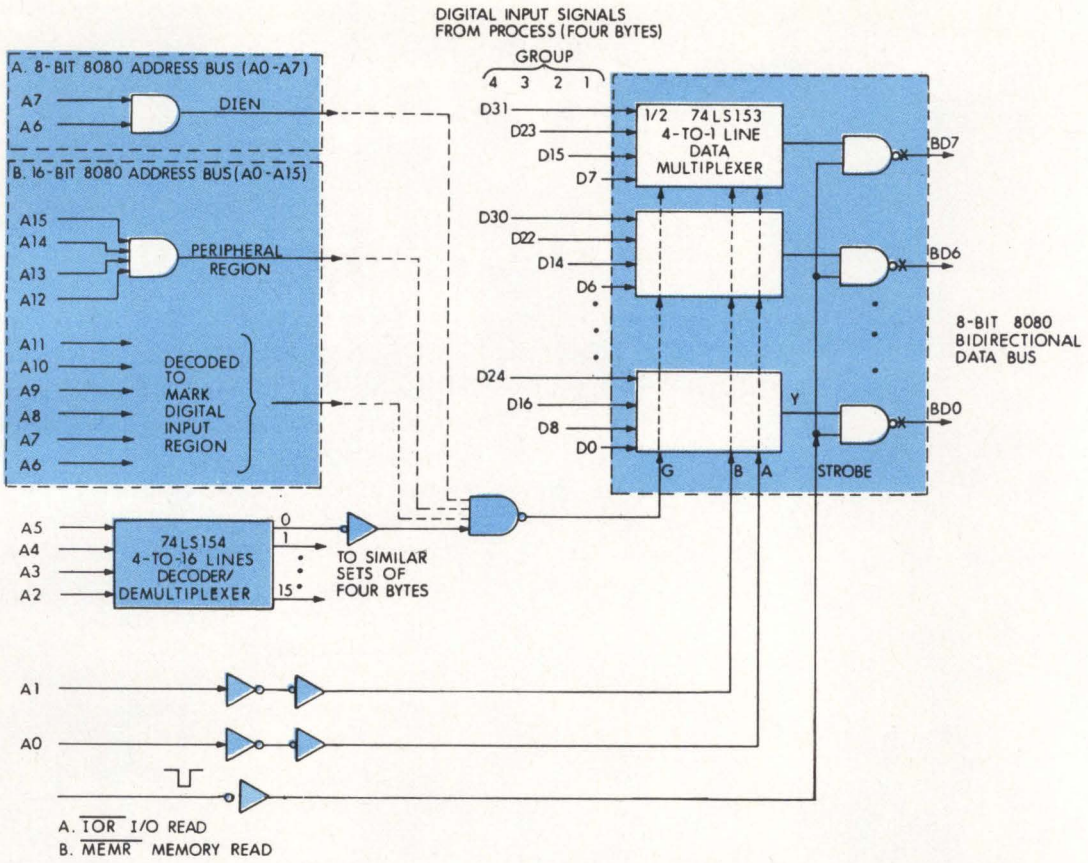

Fig 1 Digital Input Unit. Memory mapping is done in isolated I/O (Block A) or memory-mapped I/O (Block B) modes. The only structural differences are that with memory-mapped unit number of address lines to be decoded is more, and that strobing pulse is MEMR (Block B) instead of IOR (Block A). Hardware capacity can be expanded by adding enclosed (dotted) blocks

formation about states of signals D15 through D8 would be available at multiplexer outputs. The microprocessor issues the IOR pulse at an appropriate time to strobe states of multiplexer outputs onto the microcomputer data bus, then reads them into the accumulator.

The top 4k of memory address space (ie, hexadecimal addresses FXXX) may be reserved for peripheral devices using address lines A15 to A12 when DIU is connected for memory-mapped I/O (Fig 1, Block B). Since the microprocessor can address a 64k memory, the amount available for software programs is not greatly limited. Address lines A11 to A6 are decoded depending upon the specific digital input region allotted by the software program to the DIU in the top 4k. Operation of the DIU is the same for memory-mapped and isolated I/O; the difference from a hardware viewpoint is the increase in address lines (from eight to 16) to be decoded. In addition, the control pulse for reading data is memory read (MEMR) rather than IOR.

In both modes, input information is stored in the working area of memory. However, in process control, the operating system generally acts depending upon the input signals that have changed since the previous scan. The operating system generates a table in memory containing a list of changed inputs. Input states of the previous scan are XORed with those of the present scan, and any changes are stored in a change table.

As summarized in the Table for the DIU, programs based on memory-mapped mode require less memory space and initialization time, and have a faster read time per input port. Thus, inputting a block of 64 bytes can obtain a net saving of 480 μs in execution time.

Digital Output Unit

A digital output unit (DOU) can also be connected for isolated or memory-mapped I/O (Fig 2). When the DOU is connected for isolated I/O (Fig 2, Block A), the microprocessor places the address of the specified port on address lines for executing an OUT instruction. After a proper time delay, it generates an I/O write (IOW) control pulse to write data into the port. Data are available on bi-

Software Program for Digital I/O Units

Program Type	Memory Locations	Initialization Time (μs)	Time per Loop (μs)	Block Time (μs)	Time Saving (μs)
Isolated Output	19	18.5	23.5	1504	256
Memory Output	16	13.5	19.5	1248	
Isolated Input	19	18.5	23.5	1504	256
Memory Input (Without Generation of Change Table)	16	13.5	19.5	1248	
Isolated Input	26	22	37.5	2400	480
Memory Input (With Generation of Change Table)	20	15	30	1920	

Notes:

Memory Locations are number of locations occupied by relevant program
Initialization Time is time required for setting up data (like counter value, table pointer value, etc) in various registers
Time per Loop is time required for reading or writing one data item
Block Time equals Time per Loop x Block Length
Block Length is number of data items to be read or written; block length for digital I/O units is taken as 64 bytes

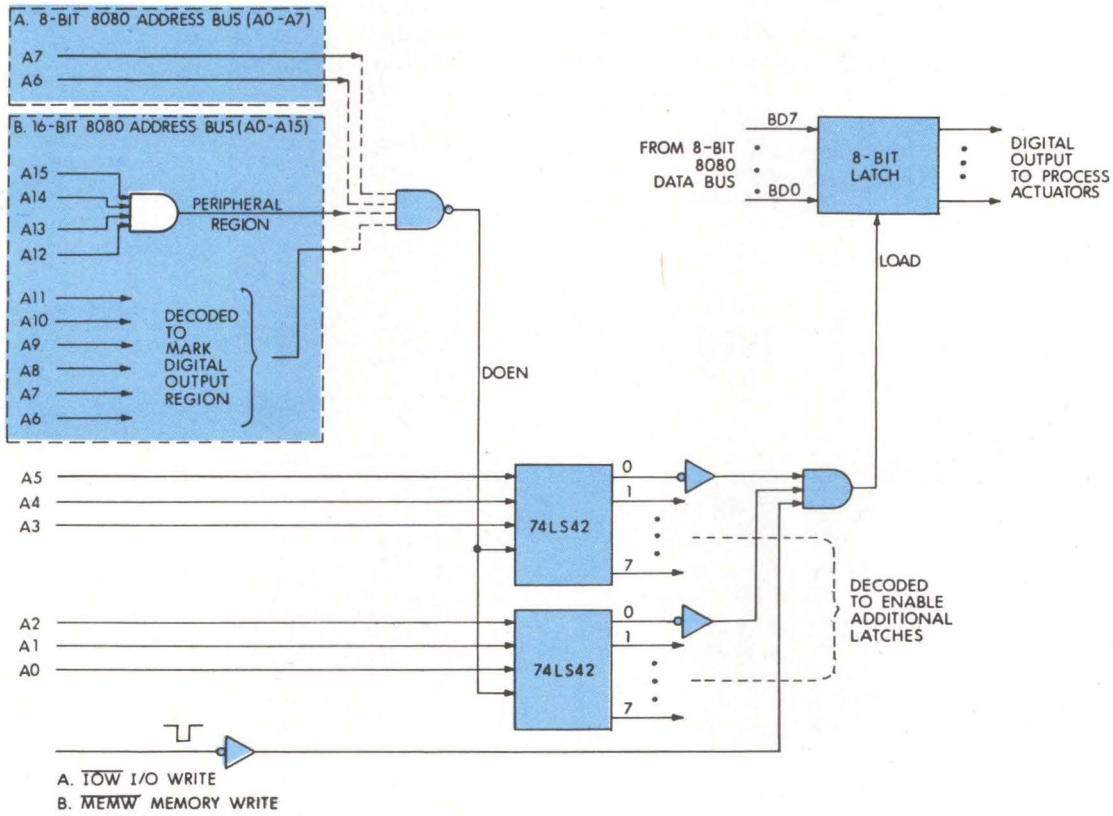

Fig 2 Digital Output Unit. Memory mapping is in either of two modes (see Fig 1). Hardware required is somewhat greater when unit is memory-mapped. Outputs can be used to energize lamps on operator's console or to actuate relays or solenoids in controlled process. Hardware capacity is expanded by adding more decoding logic and output latches

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directional data lines BD7 through BD0.

With 64 output ports, the DOU can be referenced when the port address specified in the OUT instruction is 11 XXX XXX. Fig 2 shows only one port, but the DOU can be expanded to full capacity by more complete address line decoding. For isolated I/O, address lines A7 and A6 are ANDed to generate a digital output enable (DOEN) signal. Address lines A5 through A3 and A2 through A0 are decoded into eight addresses each, and can be decoded further, in suitable combinations, to access each of the 64 output ports. The $\overline{\text{IOW}}$ pulse is used to write data from the data bus into the specified port.

When the DOU is connected for memory-mapped I/O (Fig 2, Block B), the top 4k of memory address space are reserved for digital inputs and peripheral devices, as described for the DIU. Main DOU hardware differences between modes are an increased number of address lines to be decoded (eight to 16), and use of the control pulse memory write ($\overline{\text{MEMW}}$) instead of $\overline{\text{IOW}}$. In process control, the operating system generates images of output commands to be delivered to the process. The system retains these images in memory store, and at a desired time dumps commands through the DOU. As listed in the Table, programs based on the DOU memory-mapped I/O mode require less memory space and execution time.

Summary

Real-time I/O peripherals can be connected to either I/O or memory address space in a microprocessor-based control system. Examination of these two address modes for a DIU and a DOU shows that, from a hardware point of view, there are no significant differences in either implementation. With software, however, the digital I/O unit programs for the memory-mapped I/O mode occupy less memory space and execute in a shorter time. With these results, designers have a means of deciding which I/O mode will suit a particular process control application.

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MCS-80 Users' Manual, Intel Corp, Santa Clara, Calif, 1976

J. F. Wakerly, "Microprocessor Input/Output Architecture," *Computer*, Feb 1977, pp 26-33

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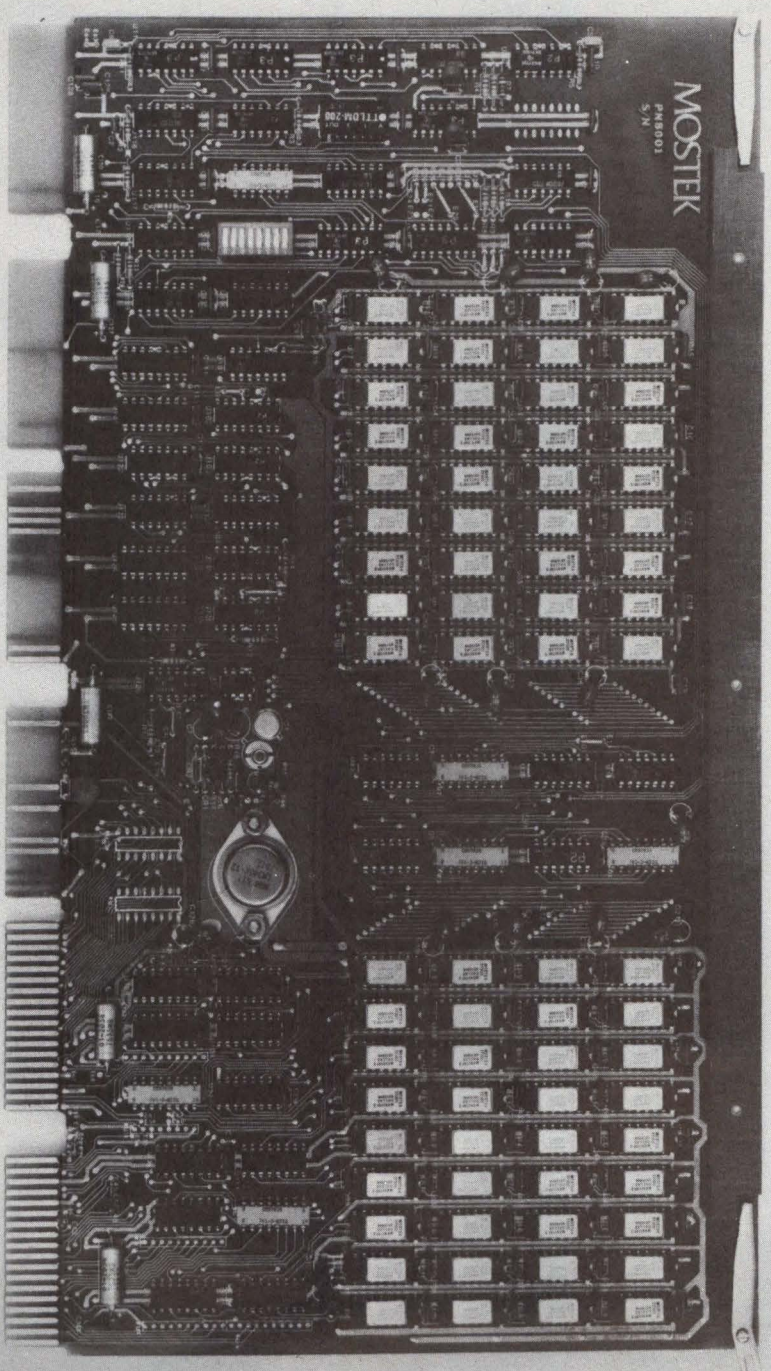

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CIRCLE 127 ON INQUIRY CARD

TECH BRIEF

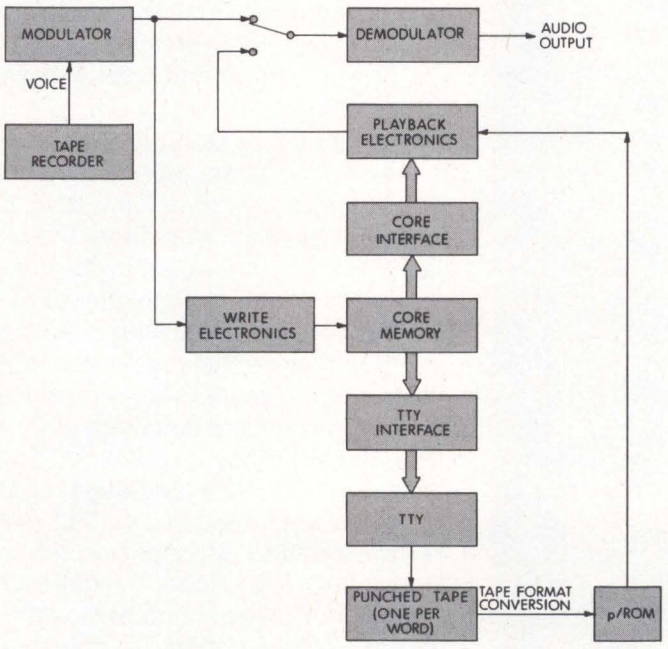
Oral Annunciator With Programmable Vocabulary

Basic vocabulary is four spoken words, expandable to 28

An oral annunciator system employing delta-squared modulation converts analog voice signals to an equivalent digital format and then stores the digital speech in a solid-state nonvolatile memory. Stored words are selectively reconstructed upon demand, using a delta-squared demodulator to reform the speech signals. The prototype annunciator has a basic vocabulary storage capacity of four spoken words, expandable to 28 if a read-only memory replaces the presently-used programmable read-only memory (p/ROM).

A block diagram of the annunciator is illustrated. The word generation process consists of encoding the word waveform, storing the word bit stream in the core memory (write electronics), playing back the stored-word bit stream from core via memory interface (playback electronics), and then dumping the digitized word through the teletypewriter (TTY) interface onto punched tape (either 4k or 6k bits long for the present vocabulary size). Programming the solid-state memories for each word, and inserting the p/ROMs into the playback electronics for word testing are last in the process.

The playback electronics implement the message selection by concatenating the bit streams representing each spoken word in the message and feeding the bits in a serial data stream to the demodulator. Control logic cycles the playback unit through 10 repetitions of any combination of 2-word messages by providing the timing signals that coordinate the logic functions. Logic functions include p/ROMs, address, and counting logic.



Voice (analog) signal is converted in oral annunciator to its digital equivalent and stored in solid-state memory. Upon command, memory becomes part of annunciator system which includes other digital logic, digital-to-analog converter, and audio amplifier

Note

This work was done by Don Paslay and Paul Wong of the Garrett Corp for Johnson Space Center. For further information, including a discussion of message synthesis techniques and breadboard development, write to: John T. Wheeler, Johnson Space Center, Code AT3, Houston, TX 77058. (MSC-14798).

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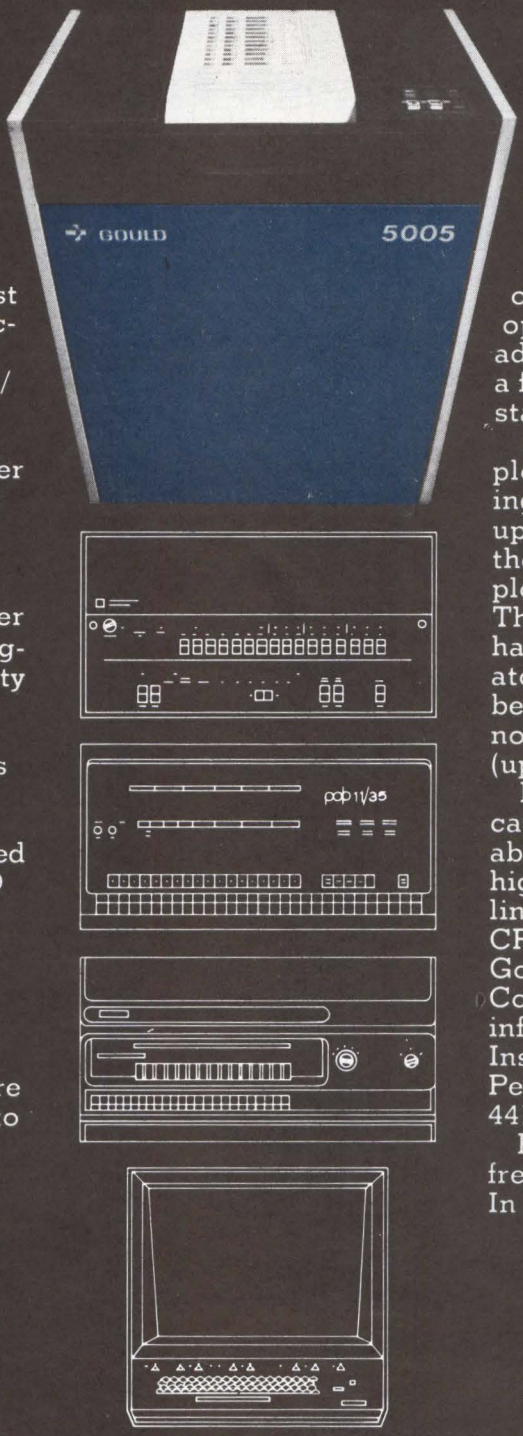

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TECH BRIEF

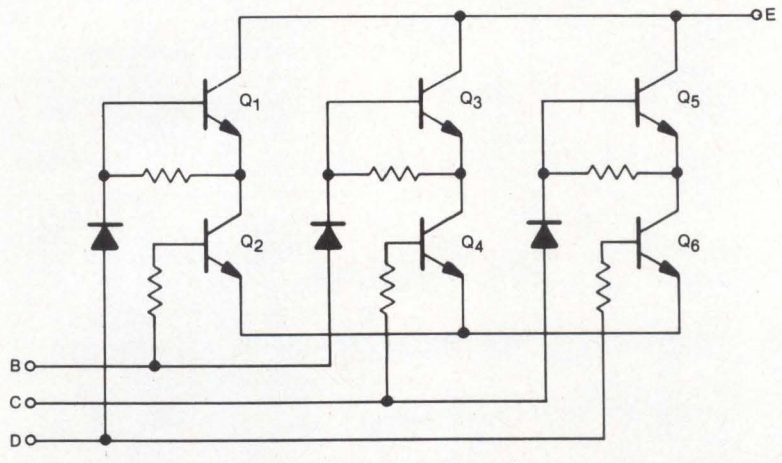
Majority-Voted Logic Fail-Sense Circuit

A self-monitored hybrid circuit reacts to both static and dynamic changes

The fail-sense circuit previously used in a portable, high reliability ac power inverter consisted of three single-channel detectors. These monitored overvoltage, undervoltage, and frequency shift. Over and undervoltage detectors were connected to the dc-regulated bus, the frequency shift detector was connected to the main ac bus, and detection was accomplished by using a tuned transformer. Its output was rectified to produce the required error signal. All three detector outputs were connected to an OR gate which drove a time-delayed relay driver and switched in the standby equipment. The relay would transfer normally if the signal were present for more than 1.5 s, but it could also transfer, or fail to operate, due to a single part failure anywhere within the fail-sense circuit.

A single part failure in an updated fail-sense circuit does not cause circuit malfunction. The redundant error-sensing amplifiers are majority voted; the circuit requires an input signal to at least two independent inputs for the fail-sense circuit to switch the power source from main to alternate supply.

In the new fail-sense circuit each detector requires three error amplifiers followed by the majority-voted logic stage. The error voltage is sensed at a point common to all three error amplifiers. Each amplifier compares the sensed error with its own reference to produce its error signal, which is weighed by the majority-voting circuit. If a signal is applied to any of the majority logic stage input points B, C, or D in the Figure, point E will remain high. Signals must be applied to at least two points to enable E to go to zero, thus causing the power supplies to shift from main to alternate source. If any part fails, open- or short-circuits, the circuit still functions normally.



Majority-voted logic component of fail-sense circuit receives three error-voltage signals that are sensed at a single point by three error amplifiers. Error-amplifier outputs (B, C, and D) are weighed by logic circuit. If a transistor shorts, only one signal is required to operate; if a transistor opens, two signals are required

Note

This work was done by Colonel W. T. McLyman of Caltech/JPL. For further information, write to: John C. Drane, NASA Resident Legal Office-JPL, 4800 Oak Grove Dr, Pasadena, CA 91103. (NPO-13107).

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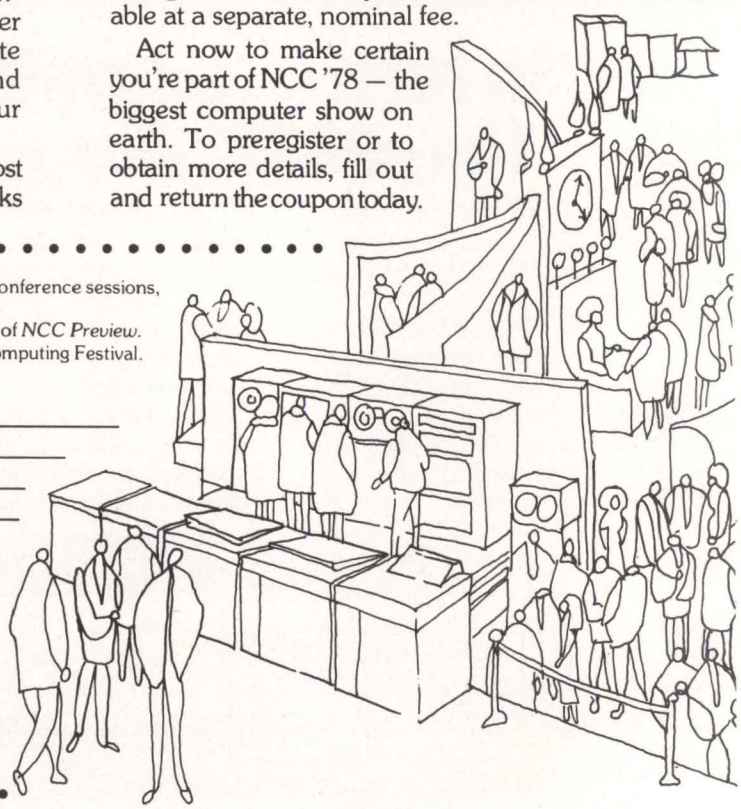

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CIRCLE 60 ON INQUIRY CARD

MICROCOMPUTER INTERFACING: A DEMONSTRATION PROGRAM FOR THE 8253 TIMER

David G. Larsen and Peter R. Rony
Virginia Polytechnic Institute and State University

Marvin L. DeJong
School of the Ozarks

Christopher Titus and Jonathan A. Titus
Tychon, Inc

Analysis of the 24-pin Intel 8253 programmable interval timer for counting and timing operations, which began in last month's column (p 136), continues with the presentation of two test programs—one demonstration program that illustrates the various modes of operation of the timer, and another that demonstrates the reading of counter data "on-the-fly." The counter, wired to an 8080A-based microcomputer, is detailed in Fig 1. Though the use of an oscilloscope is convenient for monitoring the output signal OUT0 from counter #0, it is just as useful to provide a single 7490 decade counter chip to detect negative-edge transitions at OUT0. The 25-kHz input clock frequency, which has a period, T, of 40 μs, is input at CLK0.

To use the 8253 chip, it is important to understand the nature of the output signal OUT0 as a function of the six different modes of operation—mode 0 through mode 5. Since the manufacturer's literature[1] seems to be somewhat confusing, we have simplified their diagrams by omitting all signals other than OUT0. This permits us to compare simultaneously all six modes (see Fig 2). Note that modes 0 and 1 provide a negative monostable clock pulse of duration NT; mode 2 presents a series of negative clock pulses of pulse width T and period NT; mode 3 gives essentially a square wave of period NT; and modes 4 and 5 provide a single strobe pulse of pulse width T at a time NT after a trigger pulse has been applied to counter #0. The quantity, N, is a 16-bit timing byte initially loaded

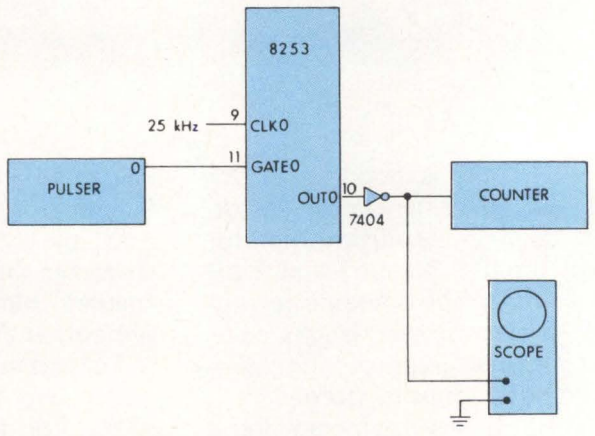

Fig 1 Circuit for counter #0 on 8253 timer to be used with demonstration program given in Listing. It is assumed that counter counts negative-edge transitions

Demonstration Program Listing

```
003 000   076   TIMER,  MVIA   /Move control word into accumulator
003 001   060          060     /Mode control word*
003 002   062          STA     /Store it within control register
003 003   003          003     /in 8253 interval timer chip
003 004   200          200
003 005   076          MVIA    /Move LO counter byte into accumulator
003 006   000          000     /LO counter byte
003 007   062          STA     /Store LO byte in counter #0
003 010   000          000
003 011   200          200
003 012   076          MVIA    /Move HI counter byte to accumulator
003 013   000          000     /HI counter byte
003 014   062          STA     /Store HI byte in counter #0
003 015   000          000
003 016   200          200
003 017   303          JMP     /Wait
003 020   017          017
003 021   003          003
```

To observe the counting process on a pair of output ports, replace last program instruction by the following sequence of instructions.

```
003 017   076          MVIA    /Move new control word into accumulator
003 020   000          000     /Mode control word to read counter #0
003 021   062          STA     /Store it within control register
003 022   003          003
003 023   200          200
003 024   072   RPT,   LDA     /Read LO counter byte into accumulator
003 025   000          000
003 026   200          200
003 027   323          OUT     /Output LO counter byte to port #2
003 030   002          002
003 031   072          LDA     /Read HI counter byte into accumulator
003 032   000          000
003 033   200          200
003 034   323          OUT     /Output HI counter byte to port #0
003 035   000          000
003 036   303          JMP     /Continue to output the counter bytes
003 037   024          RPT
003 040   003          0
```

*Control word is changed to demonstrate behavior of different modes of operation.

into counter #0. In our program, the timing byte is 000 000, corresponding to the decimal number 65,536.[1]

At this point, it is appropriate to comment on the two possible actions of the GATE0 input.

(1) GATE0 functions as a gating input; when at logic 0, pulses input at CLK0 do not reach counter #0 and no counting occurs. This type of behavior occurs with modes 0, 2, 3, and 4.

(2) GATE0 functions as a trigger/reset input; a positive-edge transition at GATE0 resets counter #0 and initiates counting. Each time that there is a positive edge at GATE0, counter #0 is reset. This type of behavior occurs with modes 1, 2, 3, and 5.

These different actions can best be observed with the aid of a counter and a value of NT in the range of 3 to 10 s. In this case, N is 65,536 and T is 40 μs, so NT = (65,536) $(40 \times 10^{-6}) = 2.62$ s.

The program used to test the 8253 chip is provided in the Demonstration Program Listing. Note that memory-mapped input/output (I/O) is used, in which the control register has an address of 200 003 and counter #0 has an address of 200 000. The program is quite simple. The user first outputs the control word, 060 (mode 0), into the control register. Next, the LO and HI counter bytes, both of which are 000, are successively loaded into counter #0. Finally, a wait loop is entered. By referring to Table 2 in last month's column (p 140), it is possible to determine that a control word of 060 (mode 0) indicates counter #0. The least significant byte is loaded first, then the most significant byte; mode 0 operation of the counter is then observed, and is counted down in binary.

During execution of this program, OUT0 goes immediately to logic 0 and remains at this logic state for NT seconds, after which it returns to logic 1. This behavior can be repeated only by executing the program a second time, starting at memory address 003 000.

If the control word at location 003 001 is changed to 062 (mode 1), the execution of the program is started,

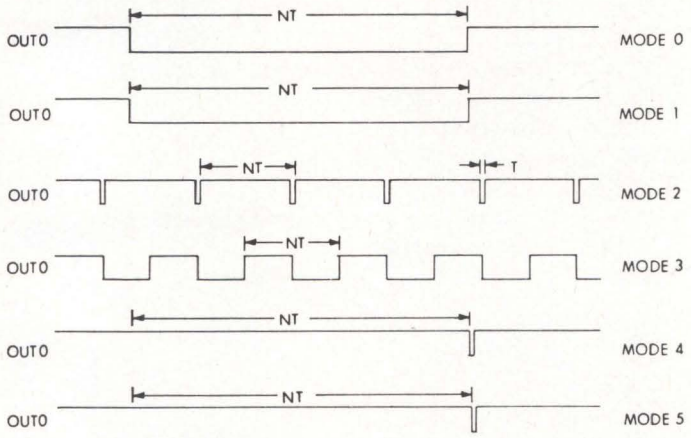

Fig 2 Timing diagrams for OUT0 output signal for each of six operating modes of 8253 timer

and the pulser shown in Fig 1 is pressed, a negative pulse of 2.62-s duration will also be observed. However, if the pulser is not pressed, and thus a positive edge is not applied at GATE0, no monostable pulse will be observed. On the other hand, repeated pressing and releasing of the GATE0 pulse at time intervals less than 2.62 s can prolong the monostable pulse indefinitely. In this way, a retriggerable monostable multivibrator output is produced.

A control word of 064 results in the behavior depicted for mode 2 in Fig 2. Repeated generation of positive edges at GATE0 at time intervals of less than 2.62 s causes counter #0 to be reset repeatedly, preventing the appearance of short negative clock pulses. The same result can be obtained by allowing GATE0 to remain at logic 0 after having applied a positive edge. The GATE0 input thus exhibits both gating and trigger/reset behavior.

Mode 3 behavior (control word of 066) is similar to that for mode 2, except that a nearly symmetrical square wave is produced. Deviations from symmetry occur when the counter byte is an odd number, and are most pronounced when the counter byte is very small.

In mode 4 (control word of 070) the positive edge of the $\overline{\text{WR}}$ pulse, which is applied at pin 23 of the timer when the STA instruction at 003 014 is executed, initiates counting that culminates in the production of a negative clock pulse of pulse width T. The time duration between the positive edge and the pulse is 2.62 s. GATE0 acts as a gating input, with a logic 0 inhibiting the counting process.

Finally, in mode 5 (control word of 072) a positive edge at GATE0 initiates counting. By repeatedly generating positive edges at GATE0 at time intervals of less than 2.62 s, the user repeatedly resets counter #0 and prevents the appearance of the single negative clock pulse.

It should be noted that in all modes counter action begins on the first negative clock transition after $\overline{\text{WR}}$ (pin 23) or GATE0 goes to logic 1, and that $\overline{\text{WR}}$ can initiate counting in all modes except 1 and 5.

Although the primary interest in many applications of the timer is to generate the proper signal at OUT0, as shown in Fig 2, it is also possible to read the contents of the 16-bit counter without affecting the counting operation. By inputting a control word of 000, 100, or 200, the 16-bit count of counter #0, #1, or #2, respectively, are latched. As shown in the memory mapped I/O example in the Listing, the two bytes can be read into the 8080A chip, the LO byte first and the HI byte second.

Owing to space limitations of this column, it is not possible to discuss applications in detail. A 16-bit frequency counter has been described recently by Lynne,[2] and a possible scheme has been proposed by DeJong* for measuring the half-life of a radioactive substance in a situation where the daughter is either stable or has a long half-life.

References

1. *Intel Data Catalog 1977*, Intel Corp, Santa Clara, Calif, 1977
2. P. Lynne, "Implementing an LSI Frequency Counter," *Byte*, Nov 1977, p 146

*Prof DeJong, the School of the Ozarks, Point Lookout, MO 65726 will implement a number of counting schemes in a physics laboratory, and would be interested in corresponding with others who have similar interests.

This article is based, with permission, on a column appearing in *American Laboratory* magazine.

Note: A series of 3-day microcomputer courses covering Microcomputer Interfacing, Introductory Assembly Language, and Intermediate Assembly Language will be offered between April 6 and 15. Featuring 8080 and 8085 processors, the programs will have over 15 operating microcomputers available for participant use during labs. Dr Christopher Titus and Jonathan Titus will conduct the sessions at Tychon, Inc, Blacksburg, Va. Information is available from Tychon, Inc, PO Box 242, Blacksburg, VA 24060, tel: (703) 951-9030.

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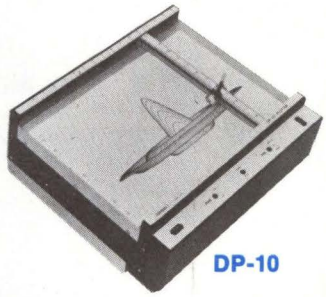

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As a 16-bit CPU, the device uses a single-word, 16-bit instruction and data word format, reducing requirements for memory access and program storage. The set of 45 instruction types breaks down into a general-purpose combination of 337 individual instructions. A key feature is the microprocessor's ability to operate on both 8- and 16-bit data words, thus extending its capabilities to 8-bit applications.

The chip contains status and control circuitry, conditioned branch sense circuitry, interrupt logic (6-level hardware-vectored priority interrupt structure), and a portion of the clock generation circuitry. Operating with a 2-MHz clock, the microprocessor has a clock microcycle time of 500 ns, and microinstruction cycle time for most internal operations of 2 μs.

Two functions required in external circuitry—a single-phase, true and complement clock input plus data buffering—can be provided by adding a MOS clock and bidirectional transceiver. Addition of a ROM and one to four RAMS, all with onchip address latches, produces a complete microprocessor system with no more than five to ten packages. The device can run at full speed with inexpensive standard memories.

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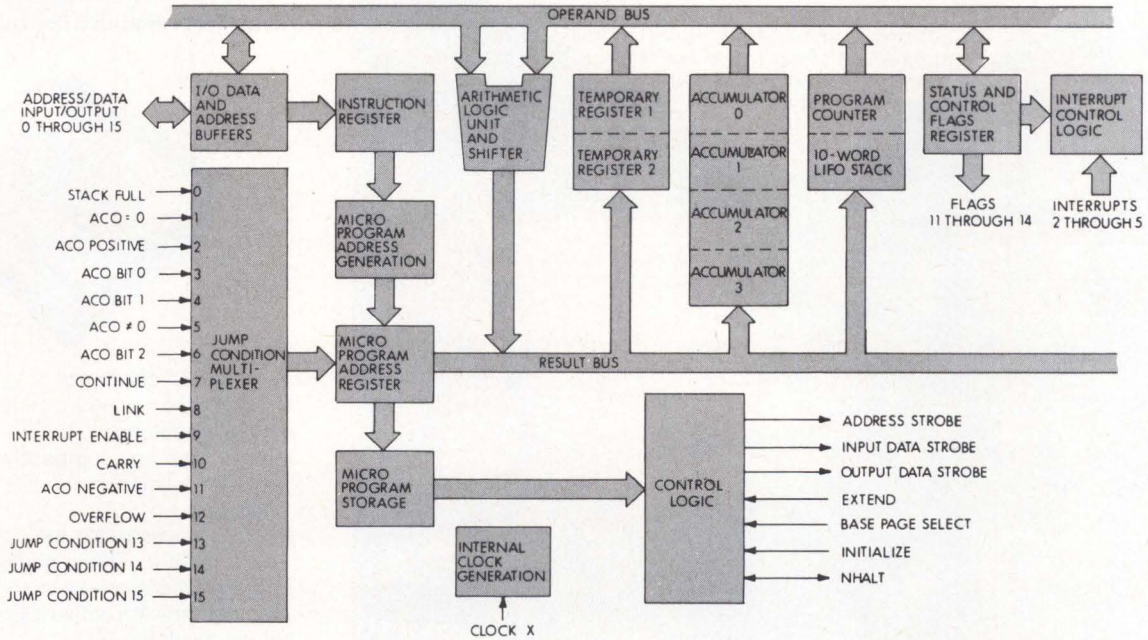
The ALU provides data manipulation with standard operations as well as addition of 4-digit/word BCD data and straight data. The microprocessor also uses a unified low power Schottky compatible bus architecture in which address and data transfers



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between CPU and external memories or peripherals occur over the same 16 data lines. An onchip I/O capability features flag output and jump commands which give flexibility in controlling peripherals and can be used together as a serial I/O port.

Software compatible with the PACE family, this microprocessor can also utilize the same development aids, allowing applications programs to be written, assembled, debugged, and executed prior to use with the 8900 application system. An 8900 low cost development system for developing, testing, and debugging its hardware and software will also be made available.

Version of Super BASIC Is Upgraded With Speed and Error Features

Version 3.0 of Super BASIC is an improved 12k BASIC interpreter, providing programmable error handling. It is relocatable and uses the monitor's operating system for I/O handling. Designed primarily to run on the company's Z80 microcomputer system, it is adaptable to other Z80 based systems.

The interpreter allows for serial input and output of ASCII and binary data from the Zapple Monitor defined reader and punch devices. Technical Design Labs, Research Pk, Bldg H, 1101 State Rd, Princeton, NJ 08540 has incorporated such features as a dynamic load/save specification and error processing functions.

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Microprocessor/ Software Performs With Minicomputer Capability

The 9440 Microflame™ 16-bit 10-MHz microprocessor that can execute a minicomputer instruction set with minicomputer performance, together with a software package, has been announced by Fairchild Camera and Instrument Corp's Semiconductor Products Group, 464 Ellis St, Mountain View, CA 94042. The complete single-chip CPU, packaged in a 40-pin DIP, executes Data General's NOVA™ 1200 instruction set. The microprocessor is based on Fairchild's I^3L™ technology, as are the TTL dynamic memories with which it is designed to operate.

Data and instructions are stored in external memory; a 16-bit wide, 3-state information bus carries data and addresses between the CPU and other computer circuits. Memory holds 32k 16-bit words, and I/O ports can serve up to 63 peripheral devices using programmed I/O, interrupt-driver I/O, or direct memory access.

An initial software package, FIRE I™ (Fairchild Integrated Real-time Executive) offers the appropriate tools to evaluate and develop 9440 systems. Its three main software systems are diagnostics, a bootstrap and binary loader, and an interactive entry and debugging program. Diagnostics include a toggle-in memory test, system exerciser, instruction timer, and memory diagnostics. Single quantity price is $250. Other FIRE software packages are a text editor ($110), symbolic debugger ($50) and BASIC business language program ($550).

An introductory kit consists of the microprocessor, 16 4k-bit memories, required SSI/MSI components and circuit schematics for memory control, software, and manuals for $750. Users can construct a board-level system in their own board format. Additional software and LSI support circuits will be announced.

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Add-On Disc System Upgrades 8080 Computer to a Z80 System

A disc system for Heathkit H8 computers includes dual diskette drives, power supply, case, intelligent controller, adapter, cables, and disc monitor in EPROM. The 8080 CPU board is replaced by the Z80/disc adapter board, which contains the Z80 microprocessor and support chips, 7k of EPROM, 1k of scratchpad RAM for the disc monitor, and logic for interfacing the disc system to the computer. With this addition, available from Info 2000 Corp, 20630 S Leapwood Ave, Carson, CA 90746, the H8 computer can operate in either of two switch-selectable modes.

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Hardware and Software Are Combined to Form Small Business Systems

The availability of the MicroExecutive line of turnkey small business computer systems has been announced jointly by Microcomputer Business Systems, Inc, 1776 Plaza, 1776 E Jefferson St, Rockville, MD 20852 and Industrial Micro Systems, Inc, Orange, CA 92669. The companies, respectively, will handle responsibility for marketing and hardware manufacturing.

Their first release is the MicroExecutive II, consisting of an 8080-based CPU, 65k bytes of static RAM, and two Shugart floppy disc drives (models 801 or 805 for 630k or 1.2M bytes of secondary storage). The system also comes with a Lear Siegler 80 x 24 CRT display terminal and 30-char/s printing terminal. Other terminals, printers, and hard disc drives are optional.

A small business accounting system has been designed by MBSI for the computer. An existing word processing system will also be made available. Other software packages for specialized businesses are being prepared.

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Compact Microcomputer System Combines With Dual Micro-Floppy System

A standalone, general-purpose computer system, the RD-11C is based on the DEC LSI-11 CPU. Teamed with a dual micro-floppy subsystem containing 205k bytes of storage, the entire system has up to 64k bytes of RAM, four serial interfaces, two quad expansion slots, and switching power supply. RDA, Inc, 5012 Herzel Pl, Beltsville, MD 20705 has housed the system in a 12.5 x 8.5 x 16.75" (31.8 x 21.6 x 42.5-cm) desktop enclosure.

Peripherals include mag and paper tape, punched card, and printers; std interfaces are IEEE-488, asynchronous and synchronous serial, general-purpose parallel, and DMA. A-D and D-A subsystems are available as plug-in modules. Compatible with DEC's RT-11 operating system, the computer supports various languages.

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We're ready with printers that fit your applications. The Spinwriter 5500 Series includes microprocessor-controlled receive-only and keyboard send/receive models, and basic mechanisms for those wishing to add their own power supply and housings. You may choose from RS 232-C, current loop and 8080 bus line interfaces, as well as Diablo- and Centronics-compatible interfaces. Custom interfaces are also available. Choose from six data rates from 110 to 1200 baud for half- or full-duplex communications. Spinwriter housings are die-cast aluminum for noise reduction, durability and appearance. They fit into any environment.

We're ready with service, through one of the largest, most competent organizations serving the computer industry. And we're delivering right now. Our experience tells us you can't afford to wait, and you don't have to. Spinwriters are available in OEM quantities in 60 days or less.

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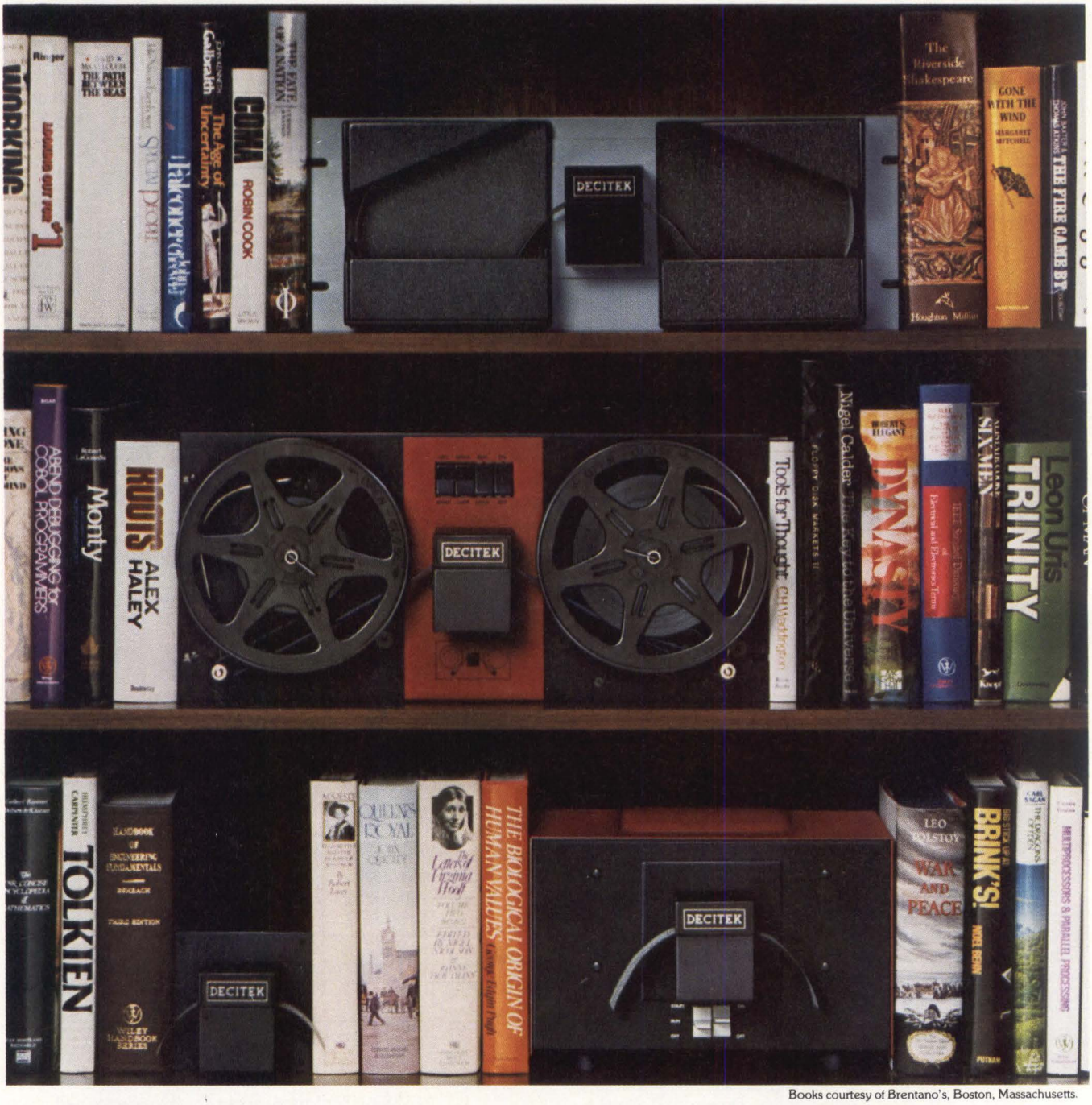
To find out more about the experience and the technology that make Spinwriters the best character printers in the industry, fill out the coupon, or call NEC Information Systems, Five Militia Drive, Lexington, Mass. 02173 (617) 862-3120.

NEC NEC INFORMATION SYSTEMS, INC.

5 Militia Drive, Lexington, Massachusetts 02173

CIRCLE 65 ON INQUIRY CARD

RECOMMENDED READING



Books courtesy of Brentano's, Boston, Massachusetts.

Decitek Punched Tape Readers come highly recommended by leading OEM's. The reason Decitek gets good reviews is simple. Simplicity of design in our complete line makes it easy to adapt our equipment to specific OEM requirements.

Also, state-of-the-art fiber optics that are far superior to LEDs are standard in all our readers. That means Decitek's 25,000 hour extended life lamps versus the competition's 2,000 hour lamps.

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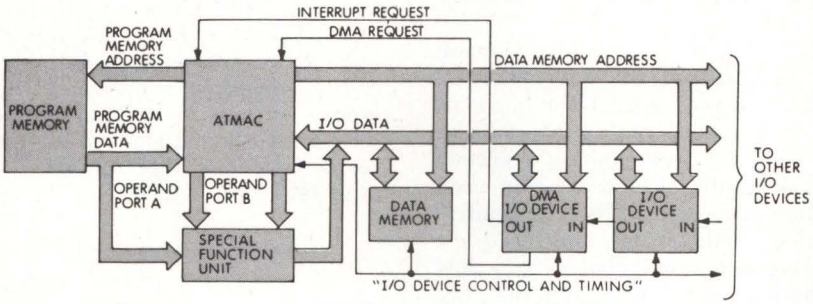
High Speed μProcessor Operates Under Aerospace Conditions

Experience in large systems integration and aerospace computer subsystems are the two areas that led to the development of the Advanced Technology Microelectronic Array Computer (ATMAC) at RCA's Advanced Technology Laboratories, Camden, NJ 08101. The 2-chip type, modular 8-bit slice, high performance CMOS/SOS LSI microprocessor is designed for real-time signal processing and high speed, low power military and commercial applications. A system can have an effective throughput rate as high as 10M operations/s, due to architectural features that enable communicating asynchronously with program memory, data memory, and I/O devices, together with specially designed hardware.

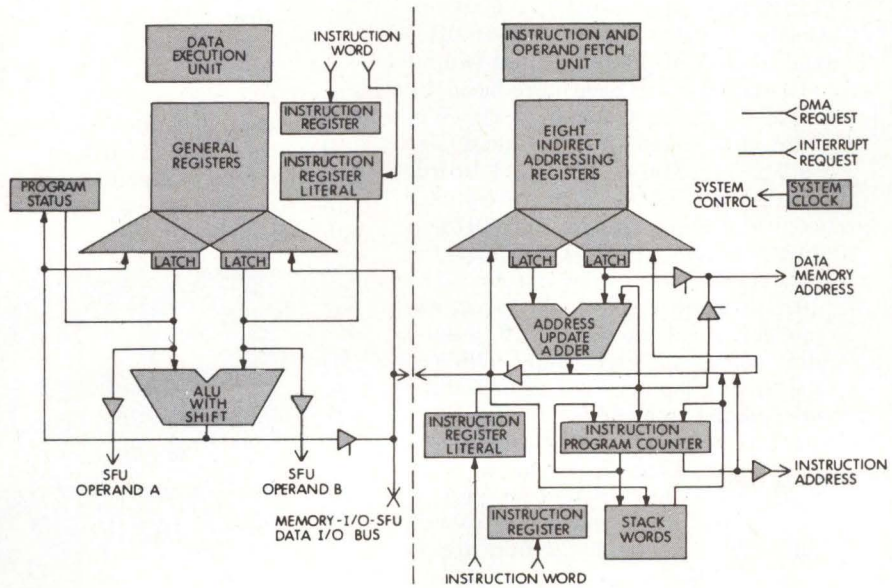
The device is a word-length expandable microprocessor. The data execution chip (DEU), containing eight registers, performs all arithmetic and logic functions, and supplies operands to application-dependent special function units (SFUs). The other chip—instruction and operand fetch unit (IOFU)—is independent of the DEU and provides addressing for operand storage in data memory, and instruction storage in program memory. It contains eight indirect address registers, program sequence counter, and 4-word program counter stack.

One or more of each of these two chip types are used. Number of DEUs depends on word length of data on which operations are to be performed; IOFUs depend on size of larger memory (data or program) to be used.

Other features include the SFU which performs special algorithms on one or two data operands at high speed, and a built-in DMA channel which uses one of the general registers for word counter and an indirect address register for address counter.



General block diagram of 16-bit ATMAC microcomputer system. Multiple bus architecture is applied to maximize functional parallelisms in arithmetic processing, fetching operands, and accessing instructions. Connections are provided to SFU, which enhances basic computational characteristics of chip in specific applications



RCA's ATMAC consists of two chip types (DEU and IOFU) operating in parallel, and partitioned along functional lines of arithmetic processing and control

Circle 405 on Inquiry Card

PDP-8 Cross Assemblers Serve Four Additional Microprocessor Types

Allowing the use of an additional DEC PDP-8 minicomputer and its peripherals for program development of more than one type of microprocessor, the X8 cross assembler series has been expanded by Sierra Digital Systems, 13905 Rancheros Dr, Reno, NV 89511 with the addition of four microprocessor cross assemblers. Containing the same features as the previous members of the series (see *Computer Design*, Dec 1976, p 126), the latest additions cover the Z80, 1802, SC/MP, and 8048 microprocessors, in addition to the prior 6502, 6800, 8080, F8, and 2650 versions. PDP-8 assembly language programs are converted into object code which is loaded into a microprocessor system or put into p/ROM.

Circle 406 on Inquiry Card

High Density Wirewrap Panel Interfaces to the SBC 80/10

The 2-8010 high density wirewrap panel, compatible with Intel's SBC 80/10, features 62 rows of 52 contacts, each on a 0.100 x 0.100" (2.54 x 2.54-mm) grid pattern with plated through-holes capable of mounting any combination of IC DIPS (from eight to 40 pins). Three 50-pin connector holes are available for I/O at the top of the board, in addition to the standard 80/10 edge connector interface at the bottom. The panel from Hybricon Corp, 410 Great Rd, Littleton, MA 01460 contains two ground planes and 10 independent power buses.

Circle 407 on Inquiry Card

Unit Interfaces 6800 μComputers to Cassettes and Data Terminals

Interfacing two cassette recorders and a data terminal to the MITS 680b computer, the CIS-30+ interfacing unit, previously used with the SWTP 6800, provides selectable cassette data rates of 30, 60, or 120 bytes/s, and data terminal rates of

300, 600, or 1200 baud. Percom Data Co, Inc, 4021 Windsor, Garland, TX 75042 has released technical memos describing this interfacing process.

Two cassette interfacing circuits are independent, enabling operations such as cross filing. Data encoding is KC-Standard/Biphase-M (double frequency); self-clocking ensures data integrity, even with inexpensive audio recorders. The computer's p/ROM monitor may be used for loading and running most programs. A local line switch isolates the computer for offline sending of recorded programs to the data terminal. Program control of recorders is optional.

Circle 408 on Inquiry Card

Family of Analog and Digital I/O Cards Are Compatible With LSI-11/2

Cards for A-D input (model 1012), analog input multiplexer expansion (1012-Ex), DMA (1620), digital optically isolated input (1616-0II), and digital optically isolated output (1616-0I0) have been introduced by Adac Corp, 15 Cummings Pk, Woburn, MA 01801 as half-quad size [8.5 x 5" (21.6 x 12.7-cm)] boards for the DEC LSI-11/2 microcomputer (see *Computer Design*, Feb 1978, p 146), LSI-11, PDP-11/03, and the company's 1000 series system. The 1012 is jumper selectable to accommodate 16 single-ended, 16 pseudo differential, or eight fully differential analog inputs. Four input ranges are jumper selectable; resolution is 12 bits with a 35-kHz throughput rate. The 1012-Ex expander card works with the A-D unit to provide 32 or 64 single-ended or pseudo differential, or 16 or 32 fully differential inputs.

DMA transfers to and from analog and digital peripherals for the LSI-11 bus are controlled by the 1620. Memory address register and word counter are 16 bits wide.

Model 1616-0II allows 16 lines of parallel data to be transferred from an external device to the bus of the microcomputer; the 1616-0I0 transfers data from the microcomputer bus to the external device. All lines are buffered through optical isolators for complete separation of device and computer grounds.

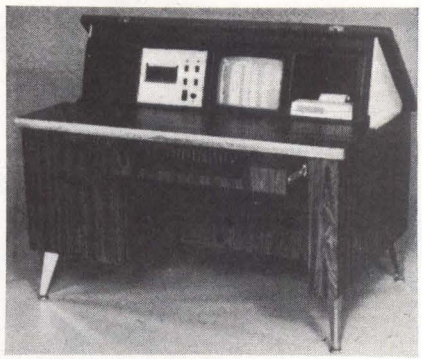
An isolated output control line, generated from one bit of the control and status register, is provided for both, as is an interrupt structure. For the input card, all lines pass through a debounce circuit after the isolator; an interrupt request is generated whenever a change of state occurs on any input line. Each of the lines of the output card is latched prior to driving the isolators.

Circle 409 on Inquiry Card

Self-Contained Computer System Enables Rapid Development Software

Software can be developed rapidly and efficiently with the 760 series computer system. The user can edit, assemble, and debug applications programs without externally saving or reloading source or object code.

The computer incorporates a Z80 microprocessor, 32k-byte user memory (RAM), three 8-bit parallel I/O ports, and an audio tone generator and speaker, plus 1k scratchpad and 1k video refresh memory. In addition, Noval, Inc, 8401 Aero Dr, San Diego, CA 92123 has included a programmable char generator, 3k of system utility routines in p/ROM, a 12" (30.5-cm) TV monitor, digital cassette tape recorder, 32-col matrix printer, and full keyboard.



Circle 410 on Inquiry Card

Anode lead wire for impressed current anodes for use in deep ground beds, sea water and other severe cathodic protection environments.

Jackets for use as cladding over glass fiber bundles in transportation applications utilizing fiber optics.

Electrical heat tracing systems maintain process temperatures in liquid-handling systems (pipes, valves and fittings). Also used to freeze-protect pipes under extreme climatic conditions.

Heat shrinkable tubing protects critical diodes and capacitors, carbon deposited resistors and provides support for butt-welded connections.

Solder Sleeves® provide electrical solder connections for wires, cables, cable shields and coaxial cables.

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Cable ties for nuclear and other tough environmental applications.

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KYNAR® Resin protects your wiring system end to end.

It's the unique balance of these properties that enables KYNAR to perform in many tough applications:

Kynar can be marked, printed, striped, or hot stamped for identification. It can also be pigmented for color coding.

Kynar has high dielectric strength and good insulation resistance.

Kynar has a temperature range from −80° to +300°F.

Kynar is nondripping, self-extinguishing (UL STD 94 V-0) and has an LOI (Limiting Oxygen Index) of 45.

Kynar has good chemical resistance, low permeability.

Kynar has a tensile strength of 7000 psi. It is mechanically strong and has good abrasion and cut-through resistance.

Kynar has low-moisture absorption (0.04%), excellent radiation and UV resistance.

For list of fabricators, more technical data, specifications (UL and military), write or call Joe Michaud. Plastics Department, Pennwalt Corporation, Three Parkway, Philadelphia, PA 19102. (215) 587-7520.

*KYNAR is Pennwalt's registered trademark for its polyvinylidene fluoride resin.
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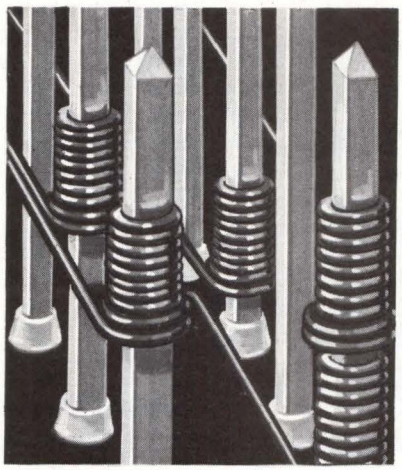

Kynar insulated wire is ideal for automatic wire wrapping operations for computer back panels.

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CIRCLE 67 ON INQUIRY CARD

Mag Tape System Provides Microcomputers With Mass Storage

Expansion of Intel's SBC 80 microcomputer into such applications as data acquisition, large file storage, and backup program storage is possible with the industry standard MT 80, a 0.5" (12.7-mm) magnetic tape system. Hardware and software compatible with the Intel SBC 80 and MDS development system, the device is made up of one to eight tape drives and a single SBC-80 Multibus™ interface card.

Formatters are an integral part of the tape drive and allow for NRZI, PE, or dual density operation on 7- or 9-track tape. Computer Marketing, Inc, 257 Crescent St, Waltham, MA 02154 has designed the interface card with dual memory mapped DMA buffer and up to 8k bytes of static RAM for tape buffering or system memory, to operate off a single 5-V supply. Software drivers for the RMX-80 and ISIS II operating systems are available.

Circle 411 on Inquiry Card

Floppy Disc Reliability Increases With Decrease in Size

The 5.25" (13.3-cm) DSD-110 floppy disc system is announced by Data Systems Design, Inc, 3130 Coronado Dr, Santa Clara, CA 95051 for use with DEC LSI-11 and LSI-11/2 microcomputer systems. Interface, controller, and bootstrap circuitry are on a single dual-wide card, thus saving one Q-bus slot by eliminating DEC's REV-11 bootstrap card. Featuring increased reliability, the system is organized into three models: interface/formatter/controller card; Shugart diskette drives, operating in IBM 3740 format; and power supply.

Circle 412 on Inquiry Card

Microcomputer System for Personal Computing Is Based on Z80 CPU

The REX microcomputer system, intended for personal computing use, comes assembled with a 4-MHz Z80 CPU, 24k RAM, video output, system keyboard, microfloppy disc drive with double-sided recording (up to 75k bytes/diskette surface), cabinet, and 15-A power supply. An S-100 motherboard holds the CPU, up to 64k of RAM, video display interface, bootstrap and Monitor p/ROM, and powerfail and vectored interrupt circuitry.

Space is available in the cabinet for a second microfloppy drive plus five slots for S-100 bus options. Realistic Controls Corp, 404 W 35th St, Davenport, IA 52806 is also offering peripheral and software options, such as Extended Disc BASIC and ANSI FORTRAN IV, for use with the system.

Circle 413 on Inquiry Card

Microprocessor Receives Approval As Military Standard Device

The 8080A microprocessor has been approved as a military standard device, meeting Military Spec MIL-M-38510D and Detail Spec MIL-M-38510/420. The approval, which consists of a listing of the microprocessor on the Qualified Products List (QPL) by the Defense Electronics Supply Center, will begin the use of microprocessors in military electronics systems and other high reliability applications. The listing allows Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 and qualified second-sources to supply the microprocessor to military contractors as a military standard part.

Circle 414 on Inquiry Card

Universal BASIC Compiler Operates With Four Microprocessors

The universal BASIC compiler is a high level language that can be compiled to run on 8080, 8085, 6800, and Z80 microprocessors, without rewriting programs. All standard BASIC statements are included; assembly language instructions may be intermixed in the BASIC program.

A debugger has been included by Futuredata Computer Corp, 11205 S La Cienega Blvd, Los Angeles, CA 90045. Outputting an assembly language source code of the compiled program to an editor file is optional. Suited for developing programs for real-time process control and test equipment, the compilers run in systems with at least 32k bytes of memory and are available for any of the company's disc-based Microsystems (see *Computer Design*, Feb 1978, p 156).

Circle 415 on Inquiry Card

Microprocessor System Functions in Control/Communication Situations

The Microline-76 microprocessor control system (ML-76) is a programmable microprocessor adaptable to many data and telecommunications control functions. The modular unit, available in desktop or rack mounting configurations, can be programmed for specific applications; it performs protocol, code, and speed conversions.

UTEC Corp, 871 Allwood Rd, Clifton, NJ 07012 has interconnected the CPU, memory units, I/O interface units, and 5- and ±12-Vdc power supply via a Unibus motherboard. A variety of standard and custom control panels and options can be accommodated.

The CPU implements the Fairchild F8 family, consisting of a microprocessor and several complementary chips tied together via an 8-bit, bidirectional data bus, timing, and control lines that interface to the memory and I/O units. Features include 8-bit organization, 2-μs instruction cycle time, and 64 general-purpose registers.

Static and dynamic memory interfaces and a floppy disc/controller comprise the memory units. Available plug-in communications interface hardware includes asynchronous 2-channel EIA or loop, full-duplex I/O interface ports; synchronous 1- or 2-channel I/O, full- or half-duplex I/O interface ports; F1/F2 analog interface; and remote mass memory I/O. Power requirements are 110 or 220 Vac, 50/60 Hz. A simplified diagnostic and plug-in maintenance program has been developed for the system.

Circle 416 on Inquiry Card

32-Channel A-D/D-A Interface/Peripheral Fits Inside µComputer

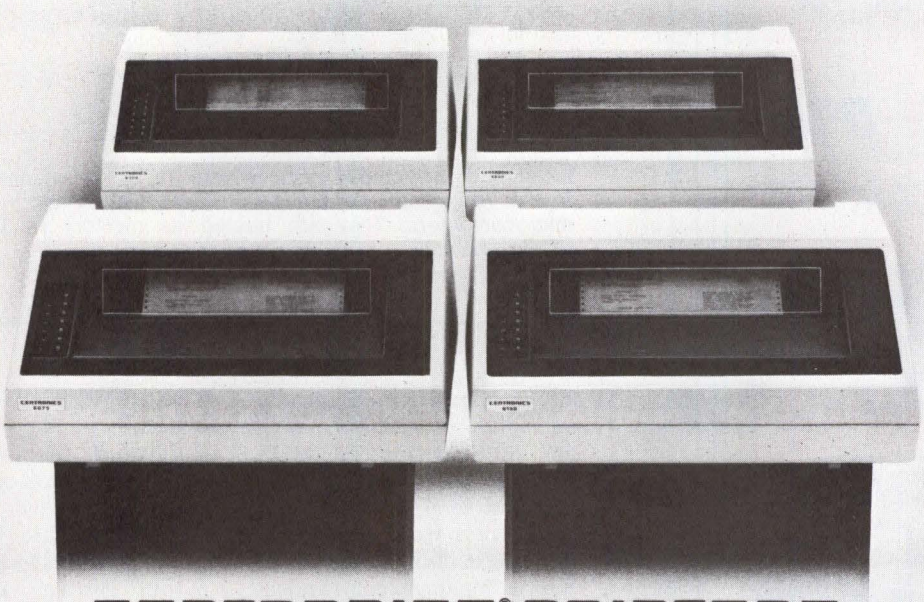
The ST-6800 series of data acquisition PC boards has been added by Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021 to its line of A-D/D-A peripherals. It is built to

Does 85% commonality make Centronics' line printer family the best?

NO. Centronics 6000 series band printers have much more to offer than just high parts commonality; technical features like an operator-changeable print band with a choice of EBCDIC character sets and microprocessor control, for example. Four models—providing superior print quality and a range of print speeds—75, 150, 300 and 600 lpm, plus design simplicity that provides exceptional reliability and makes the 6000 series a true family of low priced, fully formed character line printers.

And, as with Centronics' matrix printers and teleprinters, the 6000 series is backed by the largest worldwide service organization of any printer company, and Centronics' reputation for reliability.

Write or call for complete 6000 series information. Centronics Data Computer Corp., Hudson, NH 03051, Tel. (603) 883-0111.



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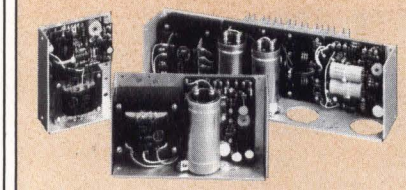
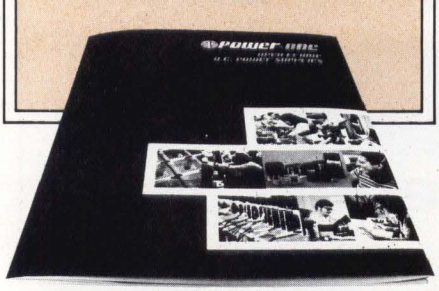


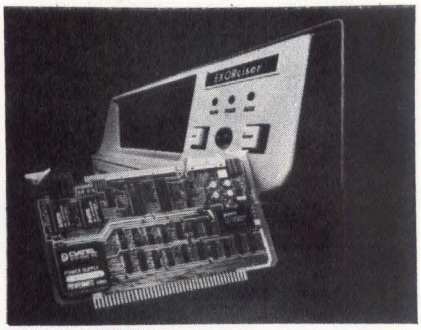


MICRO PROCESSOR COMPUTER DATA STACK

slide directly inside of and is bus compatible with Motorola's M6800/EXORciser microcomputers, saving the cost of an additional housing, power supply, and interface. It uses the 5-Vdc power from the computer bus and generates its own ±15 V for analog circuits using an onboard dc-dc converter.

Either 32 single-ended or 16 differential analog input channels are accepted and digitized to 12-bit binary data words. Speed of A-D conversion is 20 μs. Effective channel throughput rates of 30k samples/s may be achieved.

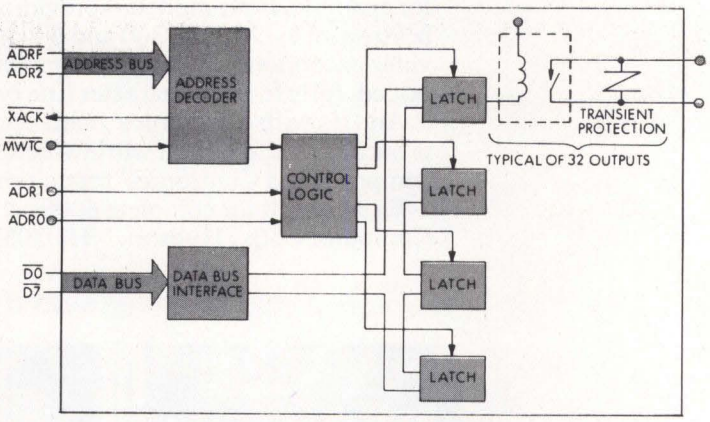
The master board also includes two D-A output channels with ±10 V and other voltage outputs. Additional expander boards with 48 A-D



or eight D-A channels/board provide capacities up to 128 channels. Memory-mapped I/O architecture is used. Single-quantity price for board with 16 A-D channels is $419, including program and manual.

Circle 417 on Inquiry Card

Isolated Digital Output Boards for Intel μComputers Handle 10 W



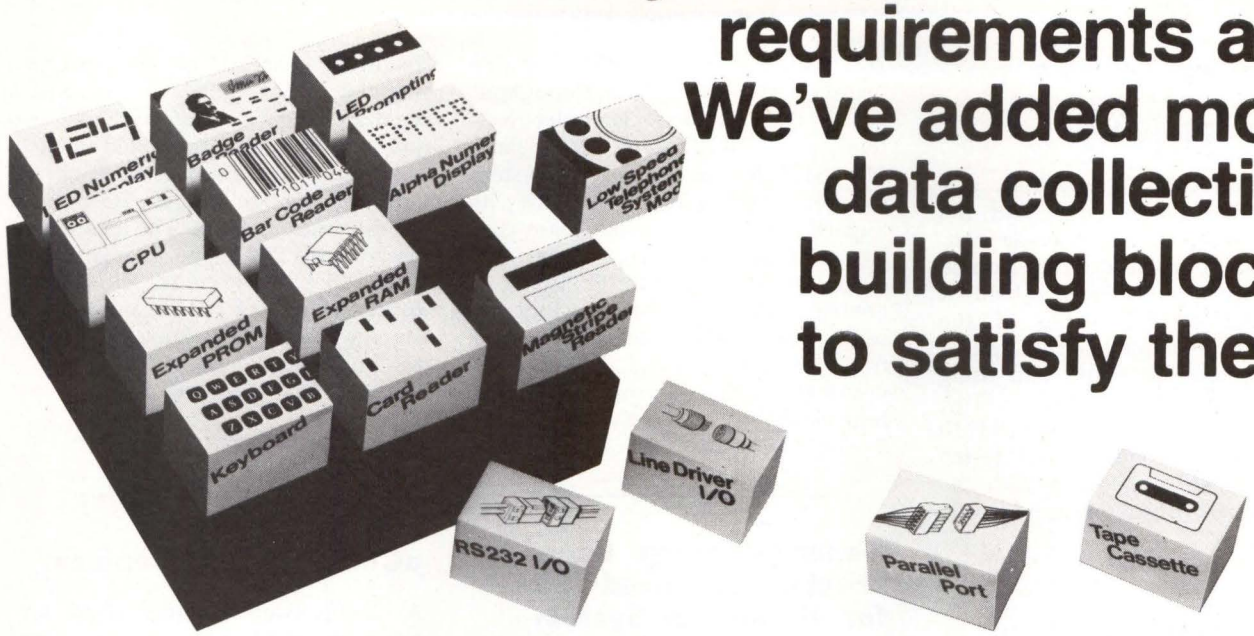
Isolated digital output systems with 16 or 32 channels operate from 5-Vdc supplies of compatible Intel SBC 80 and Intellec MDS microcomputers. They are treated as memory by CPU—eight output channels occupy one memory location

Digital output systems, mechanically and electrically compatible with Intel's SBC 80 and Intellec MDS microcomputers, offer isolation to eliminate ground loop problems and to protect the CPU from real world transients and malfunctions. Burr-Brown, International Airport Industrial Pk, PO Box 11400, Tucson, AZ 85734 has placed the memory mapped MP801 (16-channel) and MP802 (32-channel) systems on a single PCB. They provide all control and timing circuitry.

Channels are implemented by dry reed relays protected by metal-oxide varistors and can handle up to 10 W. With a life of 10^6 operations, relays provide low on-impedance, high output current, and isolate output channels from the computer bus (to 600 Vdc) and from channel-to-channel (300 Vdc).

Circle 418 on Inquiry Card

You tell us what your data collection requirements are. We've added more data collection building blocks to satisfy them.



EPIC DATA's Model 1647 data collection terminals and Model 1648 system control units (SCUs), let you configure exactly the data collection system you need. These "building blocks," based on microprocessor architecture and modularity, provide you with simple, practical and flexible terminals or systems for virtually any combination of requirements you may have.

simple. Building blocks can be combined to enable collection of information from a wide variety of pre-prepared and variable data with resulting improved efficiency and reduced errors. No computer knowledge is required for operation. Terminals can be programmed to: provide customized input, output and processing of data; prompt the user through entry steps and validating of data; and enable off-line or on-line operation.

EPIC DATA terminals are rugged, compact and lightweight. They can be wall-mounted or placed on a desk and are easily exchanged during maintenance.

practical. Environmental tests conducted in conformity with MIL-STD-810 plus in-depth, on-site testing assure reliable operation over a broad spectrum of hostile, industrial environments. Simple design and rigorous testing have resulted in an impressive MTBF.

flexible. EPIC DATA terminals can optically read punched badges and 80-column ANSI cards. User-defined keys are available for inputting variable data. Key entry data or time of day is displayed and LEDs are available for prompting.

Terminals can be configured to scan bar codes and magnetic stripes or accommodate other peripherals through RS232 ports. Display options include additional numeric displays, up to 15 LEDs for prompting and a 32-character alpha/numeric display. Serial asynchronous or synchronous communications ports with either RS232 or line driver I/O and a low speed modem may be added. Parallel communications ports are also available. Both PROM and RAM memories are expandable.

Newest Building Block: More to Come in Next Few Months

A self-contained cassette tape recorder providing up to 2.88 megabits of storage for transaction logging or store-and-forward applications is now available. The modular reel-drive tape recorder, like the rest of the building blocks, features high reliability and ease of maintenance. There is no pinch-roller or capstan to wear tape; only the head touches the tape.

SCUs. Model 1648 SCUs can be configured to poll up to 100 terminals, assemble transactions, format data, append time and date, and store or forward collected data to the host.

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Low Power Dynamic Memory Incorporates Refresh Circuitry

The SynchroFresh™ refreshing system for 8k memories uses half the power of static boards at lower cost. The system does not interrupt normal CPU operations or timing; instead, it utilizes the natural timing of the S-100 bus, monitoring the microprocessor's machine states and using T_4 states for refresh. Thinker Toy, 1201 10th St, Berkeley, CA 94710 is offering an assembled and tested dynamic memory equipped with the refresh design, Econoram III 8k x 8, for $149.

Circle 419 on Inquiry Card

System Throughput Is Increased With Addition of µComputer

The PCS 1880 microcomputer module incorporates both the 4-MHz Z80 and 4-MHz AMD9511 on one board to increase system throughput up to 60%. Process Computer Systems, Inc, 750 N Maple Rd, Saline, MI 48176 has developed the system to be fully compatible with its SuperPac 180 product line. Base configuration provides the Z80 CPU, 1k of RAM, sockets for 3k/6k bytes of EPROM, optically isolated tri-function serial port, switch selectable rates from 50 to 9600 baud, five internal vectored priority interrupts, and real-time clock.

Circle 420 on Inquiry Card

General-Purpose Board Provides Required I/Os for µComputer System

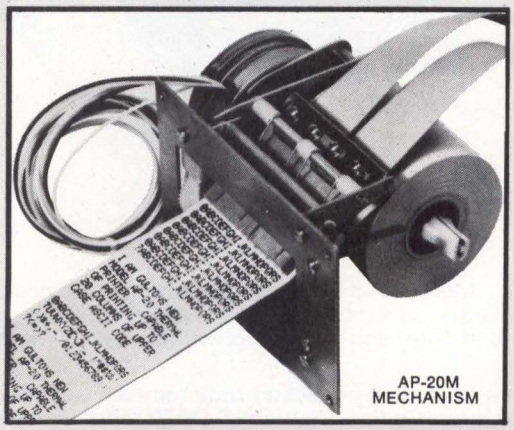
An S-100 compatible general-purpose I/O board containing most of the circuitry required for a complete microcomputer, has been announced by Infinite Inc, 1924 Waverly Pl, Melbourne, FL 32901. The MFIO-1 board, available in three versions, features memory or I/O mapped parallel input port for keyboard, memory or I/O mapped serial I/O port with crystal-controlled switch-selectable baud rates of 50 to 19.2k, and jumper selectable RS-232 or 20-mA current loop. The board also has two std 2708 type EPROM sockets and 128 bytes of RAM, allowing up to 2048 bytes of permanent program storage for system bootstrap, monitor, and utility routines.

Circle 421 on Inquiry Card

Prototyping, Extender Boards Speed Up µComputer Development

A double-sided plated-through prototyping board and extender board for the PCM-12 microcomputer system (see *Computer Design*, May 76, p 210) are both designed to speed development of custom modules. Produced by Pacific Cyber/Metrix, Inc, 3120 Crow Canyon Rd, San Ramon, CA 94583, the 12090 proto-

New Fixed Head Digital Thermal Printer Mechanisms

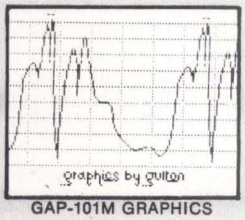


AP-20M MECHANISM

Gulton's fixed head approach to thermal printing takes advantage of the quietness and reliability of solid state switching. **COMPARE:** one moving part—the paper drive, independence from ink supplies and ribbon mechanisms, high character quality and/or full graphics capability versus **any** other printing technique such as moving head, print solenoids or wire matrix.

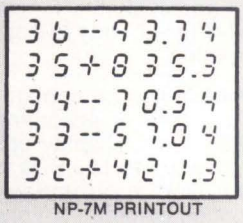
- ☐ Model GAP-101M. For simultaneous analog, alphanumeric (10 columns, 7x9) and grid pattern printing. Single row of 101 dual dot printing elements, 100 million pulses MTBF, up to 30 dot lines/sec.
- ☐ Model AP-20M alphanumeric dot matrix printer. 20 columns of 5x7 characters at up to 2.5 lines/sec.
- ☐ Model NP-7M has 7 columns of exceptional character quality in 7 segment numeric printout at up to 4 lines/sec. Model ANP-9M has two additional dot matrix I.D. columns. Up to 2.5 lines/sec.

Gulton also manufactures complete printers with interface and drive electronics, as well as custom thermal printheads.

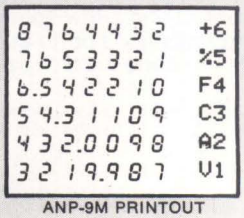


GAP-101M GRAPHICS

AP-20M PRINTOUT



NP-7M PRINTOUT



ANP-9M PRINTOUT

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Gulton Industries Inc., East Greenwich, Rhode Island 02818
401-884-6800 • TWX 710-387-1500

typing board, which plugs into the backplane bus, accommodates up to 40 14- or 16-pin DIPs, and up to four 40-pin DIPs. It handles wirewrap or solder-tail IC sockets. The 12190 extender board enables the user to physically extend the bus connections for a given module out beyond the cardcage area; thus, the module becomes easier to work on, with no degradation in system performance.
Circle 422 on Inquiry Card

Microprocessor Card Will Offer Hardware Assistance for Programs

Packaged on a single card to plug into an IBM Series/1 backplane as an I/O attachment, this microprogrammable card contains a microprocessor and loadable control storage. Under development by Advanced Software Products, Inc, PO Box 992, Arlington, VA 22216, the unit will be offered initially as a hardware assist for Series/1 COBOL programs. Performance will be transparent to the user.

Features include increased execution speed, self-diagnostic capability, and ability to detect and disable a failing unit without affecting other Series/1 functions. Microprogramming is possible from the host Series/1; user-developed microprograms can be loaded from the host without affecting concurrently executing units. Delivery of the card for IBM's CPS system is expected to begin during the fourth quarter of 1978, and for the RTPS system during the first quarter of 1979.
Circle 423 on Inquiry Card

Application Software Enables Coding and Graphing of Data

A histogram program requiring less than 4k bytes has been announced by Sunset Technologies, 210A E Ortega St, Santa Barbara, CA 93103. Developed on a Poly-88 microcomputer and video board with a 4.0 monitor, the 8080 machine language program on cassette tape may be adapted to other systems by utilizing the included source code. A bar or point graph is automatically drawn from data entered by keyboard. Features include scaling of the Y axis, alphanumerical characters, tape storage of data, and up to 109 data points on the X axis.
Circle 424 on Inquiry Card

Floppy Disc Controller For 80/10 Computer Has IBM Compatible Format

The 10043 controller is a microprocessor-based disc control card that accepts commands from an 80/10 CPU card (host computer) via the 80/10 backplane. Its IBM compatible format includes 3328 bytes of data/track with a total of 77 tracks. The card can control up to four disc drives and is equipped to perform internal CRC checks, self-tests, and status and error reporting. Manufactured by GSI Systems, 223 Crescent St, Waltham, MA 02154, the unit independently executes commands and reports their completion to the host computer. □
Circle 425 on Inquiry Card

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Functionally identical to the PDP-11V03, and using only 10-1/2" rack space, the MF-11 houses the Shugart dual floppy system, the backplane for the LSI-11 with associated peripherals, and all needed power . . . at considerable dollar savings.

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UNIT PRICE
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CRDS Charles River Data Systems, Inc., 235 Bear Hill Rd., Waltham, MA 02154,
Tel. (617) 890-1700

CIRCLE 72 ON INQUIRY CARD

MONOLITHIC DATA CONVERSION DEVICES PART 1: DIGITAL-TO-ANALOG CONVERTERS

Eric R. Garen, Daniel M. Forsyth, and Manolito E. Adan
Integrated Computer Systems, Incorporated, Santa Monica, California

Data conversion is one of the most rapidly advancing electronic technologies today, in terms of both price and performance. This development is spurred by an even more rapidly expanding market for a wide variety of digital products such as microprocessors, digital voltmeters, and digital process control systems. The key to reducing the cost of data conversion devices is the development of monolithic (single chip) circuits. This month's column will focus on digital-to-analog converters; next month, analog-to-digital devices will be reviewed.

First, some of the key parameters to consider when selecting a converter will be pointed out. Next, a reasonably complete status report of monolithic converters will be covered. Finally, some critical problems which remain to be solved in the quest for better performance will be reviewed, and some important recent developments will be highlighted.

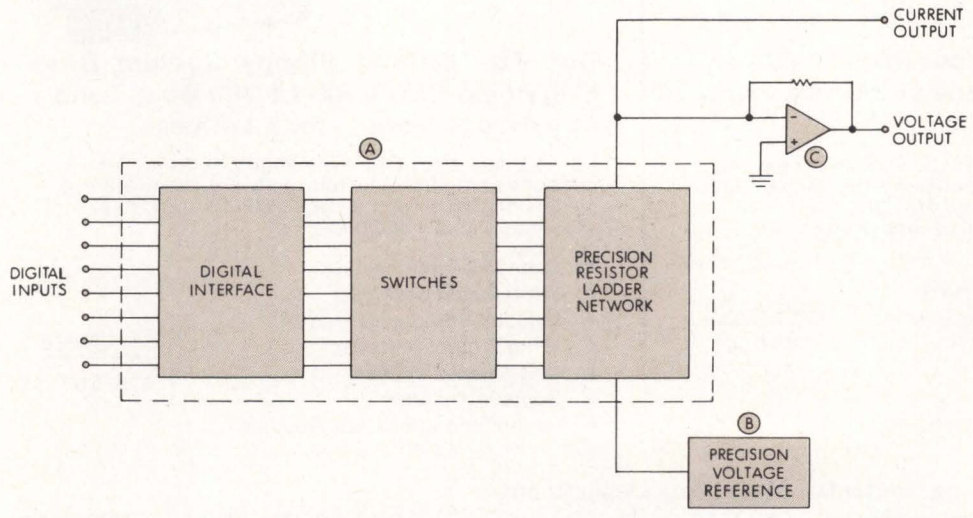

Fig 1 Basic D-A configuration. Primary elements of a D-A converter are (A) ladder and control network, (B) voltage reference, and (C) operational amplifier for current to voltage conversion. Many DACs contain only the first of these

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CIRCLE 73 ON INQUIRY CARD

Performance Parameters of Some Monolithic D-A Converters

Manufacturer	Model Family No.	Bits	Voltage Mode	Current Mode	Settling Time (typ ns)	Multiplying	Internal Reference	Linearity %	Monotonicity (Bits)	Accuracy (%)
Motorola	1406L	6	—	Y	150	Y	—	NS*	6	±0.78
Precision Monolithics	DAC-01	6	Y	—	1500	—	Y	±0.40	6	±0.78
Analog Devices	AD 559	8	—	Y	300	Y	—	±0.19	8	±0.19
Burr-Brown	DAC 90	8	—	Y	200	—	Y	±0.19	8	±0.19
Datel	DAC-IC8	8	—	Y	300	Y	—	±0.19	8	±0.19
Datel	DAC-08	8	—	Y	85	Y	—	±0.19	8	±0.19
Motorola	MC1408L8	8	—	Y	300	Y	—	±0.19	8	±0.19
Precision Monolithics	SSS1408	8	—	Y	250	Y	—	±0.19	8	±0.19
Precision Monolithics	DAC-08	8	—	Y	85	Y	—	±0.19	8	±0.19
Signetics	1408-8	8	—	Y	300	Y	—	±0.19	8	±0.19
Signetics	5005/8/9	8	—	Y	85	Y	—	±0.1, ±0.4**	8	±0.1, ±0.4**
Signetics	5018	8	Y	—	2000	—	Y	±0.19	8	±0.19
Analog Devices	AD 7530	10	—	Y	500	Y	—	±0.05, ±0.2**	8, 9, 10	±0.05, ±0.2
Analog Devices	AD 561	10	—	Y	250	Y	Y	±0.01	10	±0.01
Analog Devices	AD 7522	10	—	Y	500	Y	—	±0.05, ±0.2	8, 9, 10	±0.05, ±0.2
Datel	DAC-IC10	10	—	Y	250	Y	—	±0.1	10	±0.1
Motorola	MC3410	10	—	Y	250	Y	—	±0.05	10	±0.05
Precision Monolithics	DAC-03	10	Y	—	1500	—	Y	±0.1, ±0.04	8, 9, 10	±0.1, ±0.4
Precision Monolithics	DAC-04	10	Y	—	1500	—	Y	±0.1,±0.4	7, 8, 9, 10	±0.1, ±0.4
Precision Monolithics	DAC-02	11	Y	—	1500	—	Y	±0.1,±0.4**	7, 8, 9, 10	±0.1, ±0.4
Analog Devices	AD 7531	12	—	Y	500	Y	—	±0.05, ±0.2**	8, 9, 10	±0.05, ±0.2
Harris	MI 562	12	—	Y	200	Y	—	±0.005	12	±0.005
National Semiconductor	DA 1200	12	Y	Y	1500	—	Y	±0.01	12	±0.01
Precision Monolithics	SSS 562	12	—	Y	1500	Y	—	±0.005	12	±0.005
Analog Devices	AD 562	12	—	Y	3500	Y	Y	NS	12	±0.025
Precision Monolithics	DAC-76	8	—	Y	500	Y	Y	±1 Step	8	±0.009

*Not specified
**Values are minimum, maximum for several models

A block diagram (Fig 1) shows the basic configuration of a digital-to-analog (D-A) converter. A digital interface converts logic input levels to the control levels of a set of switches (many D-A converters can accept alternate input levels, including both TTL and CMOS.) The switches in turn control the flow of current in a resistor ladder network which provides a set of binary weighted currents. The ladder network itself is referenced to a stable precision voltage source. As the binary weighted currents flow through each of the ladder steps, they are summed to provide an output current which is proportional to the digital input value. For some applications, the output current is then supplied to an operational amplifier which converts the current level to an output voltage. A more detailed description of the D-A conversion process can be found in handbooks that are available from Analog Devices, Datel, and other data conversion equipment manufacturers.

Key elements of the D-A converter (DAC) can thus be broken into three components: (1) the digital interface/switch/ladder network, (2) the precision voltage reference, and (3) an optional operational amplifier to provide voltage output. Many of the monolithic DACs that are available today contain only the first of these elements. Others have both the ladder network and precision voltage reference. A few also include the operational amplifier, and provide a voltage output. In most high speed applications, a current output DAC is used, since the current-to-voltage conversion causes a significant loss of speed. It should be noted, however, that the drive capability in the current mode is extremely limited.

Hybrid and Discrete Converters

The alternative to monolithic DACs is to use a converter built with either hybrid or discrete technology. Hybrid converters typically fall in a range between the extremely high performance discrete and the lower performance monolithic converters, and cost between $40 and $200. They offer faster speeds and more input bits than are obtainable with present monolithic technology. Furthermore, most hybrids incorporate the voltage reference and operational amplifier within a hermetically sealed package, and many are packaged in IC DIPS. Discrete technology converters are typically 10 to 100

Gain Tempco (ppm/°C)	Unipolar Output Range	Bipolar Output Range	Output Voltage Compliance	Input Code(s)	Input Levels DTL	TTL	CMOS	ECL	p-MOS	Supply Voltages	Power Dissipation (typ at max V_{cc})
80	2 mA	±1 mA	±0.4	Binary	Y	Y				±5;−5 to −15	240
160	10 V	±5, ±10 V	—	Comp(Offset)Bin	Y	Y				±12 to ±18	250
20	2 mA	±1 mA	−1.5, 10.5	Binary	Y	Y				±5;−12 to −15	290
20	2 mA	±1 mA	−4, 4	2's Comp	Y	Y				±15	240
20	2 mA	±1 mA	−5, 0.5	Binary	Y	Y				5,−5 to −15	320 (max)
10	2 mA	±1 mA	−10, 18	Binary	Y	Y				±5 to ±18	200 (max)
20	2 mA	±1 mA	−5, 0.4	Binary		Y	Y			±5,−5 to −15	180
20	2 mA	±1 mA	−5, 0.5	Binary		Y	Y			5,−5 to −15	160
50	2 mA	±1 mA	−10, 18	Binary		Y	Y	Y	Y	±5 to ±18	135
20	2 mA	±1 mA	−5, 0.5	Binary		Y	Y			5;−5 to −15	190
10	2 mA	±1 mA	−10, 18	Binary		Y	Y	Y	Y	±5 to ±18	175
60	16 V	±5 V	±7 V	Binary		Y	Y	Y	Y	±18	270
10	2 mA	±1 mA	NS*	Binary	Y	Y	Y			5 to 15	20
30	2 mA	±1 mA	−2, 10	Binary	Y	Y	Y			5 to 15, −15	320
10	1 mA	±0.5 mA	100 mV	Binary	Y	Y	Y			15, 5 to 15	40
20	4 mA	±2 mA	−2.5, 0.2	Binary		Y	Y			5, −15	390 (max)
20	4 mA	±2 mA	−2.5, 0.2	Binary		Y	Y			5, −15	220
60	5, 10 V	—	—	Binary	Y	Y	Y			±12 to ±18	225
90	—	±5 V	—	2's Comp		Y	Y			±12 to ±18	225
60	—	±5; ±10 V	—	Sign-Mag	Y	Y	Y			±12 to ±18	300 (max)
10	2 mA	±1 mA	NS*	Binary	Y	Y	Y			5 to 15	20
2	5 mA	±2.5 mA	1 V	Binary		Y	Y			±5; −15	
	10 V; 2 mA	±10 V	±2.5 V	Bin; BCD		Y	Y			5; ±15	600
3	2 mA	±1 mA	−2.5, 10	Binary		Y	Y			−15;5 to 15	375
3	NS	NS	−1.5, 10	Bin; BCD		Y	Y			±15, 5	300
±0.1 Step	2 mA	±1 mA	−5, 18	Binary		Y	Y	Y	Y	5 to 15	
										−15 to −11	114

(Continued on p 156)

times more expensive than monolithic converters, and are thus restricted to high performance applications requiring many input bits (eg, 16) coupled with extremely high speed.

Monolithic Converters

Cost is the principal advantage of the monolithic converter. Monolithic converters in the $8 to $20 price range are common, even in single quantities. Furthermore, monolithic converters with as much as 12-bit resolution are currently available, and will increasingly cut into the hybrid market. As an example of today's technologies, consider that monolithic conversion time for eight bits is 85 ns, and for 10 bits the conversion requires 250 ns. Compare this with 8- and 10-bit hybrid conversion times of 25 ns. While this large difference in speed certainly may be critical in utilizing DACs to build very high speed systems, for typical microprocessor, digital voltmeter, or digital process control applications, the speed of currently available monolithic converters is already more than sufficient.

Most of the monolithic digital-to-analog converters currently available are summarized in the Table, together with the most important performance parameters describing each device. The table is organized in ascending order by the resolution (number of bits) of the converter; each resolution length is further divided into voltage and current modes (for most devices). The presence or absence of an internal precision voltage reference and/or voltage mode output operational amplifier is also indicated. The inexperienced reader, however, should be wary of the importance of seemingly innocuous parameters. For example, note that several of the 10- and 12-bit resolution devices actually have only 8- to 10-bit monotonicity. Since a DAC has a continuously increasing output for a continuously increasing input only if the monotonicity of the device is equal to or greater than the resolution, the devices are actually monotonic only to the resolution specified by the monotonicity.

Critical Parameters

The parameter "tempco" indicates the gain temperature coefficient of the converter. This parameter specifies the change in full scale voltage output per change in ambient temperature, and is usually specified in

Performance Parameters of Some Monolithic D-A Converters, continued

Manufacturer	Mil Temp Model Available	Number of Pins	Notes
Motorola	Y	14	
Precision Monolithics	Y	14	
Analog Devices	Y	16	≡ MC 1408
Burr-Brown	Y	16	
Datel	Y	16	
Datel	Y	16	High speed
Motorola	Y	16	Widely copied
Precision Monolithics	Y	16	≡ MC 1408
Precision Monolithics	Y	16	High speed
Signetics	Y	16	≡ MC 1408
Signetics	Y	16	High speed
Signetics	Y	22	Microprocessor compatible input buffer
Analog Devices	—	16	Single supply, low power (8-, 9-, 10-bit accuracy models)
Analog Devices	Y	16	High accuracy (¼ LSB), high speed
Analog Devices	—	28	Microprocessor compatible input buffer
Datel	—	16	Like MC 3410
Motorola	Y	16	Higher resolution
Precision Monolithics	—	18	8-, 9-, 10-bit accuracy models available; V output
Precision Monolithics	Y	18	7- to 10-bit accuracy models available; V output
Precision Monolithics	Y	18	7- to 10-bit sign accuracy
Analog Devices	—	18	Only 10-bit max linearity
Harris	—	24	¼ LSB accuracy; low tempco; fast
National Semiconductor	Y	24	½ LSB accuracy; both voltage and current out; internal reference
Precision Monolithics	Y	24	¼ LSB accuracy; low tempco
Analog Devices	Y	24	½ LSB accuracy
Precision Monolithics	Y	18	Companding Bell μ255 law, logarithmic, may be input level selected by V_{LC} (threshold control)

parts per million per degree centigrade (ppm/°C). Note from the table that this parameter varies from device to device from 10 to nearly 100 ppm. While 100 ppm sounds extremely small, this is equivalent to a change of 0.01%/°C or 0.1%/10°C. If the ambient temperature varied by 10 degrees, the full-scale voltage of a 10-bit converter would be erroneous by 1 LSB. Even worse, if the ambient voltage varied over the full commercial range of 0 to 70°C, a 100 ppm/°C tempco would cause a 0.7% full-scale voltage change. This is equivalent to an error of one bit out of seven, effectively reducing the full-scale accuracy of an otherwise 12-bit converter to seven bits.

Still another critical parameter for many designs is output compliance—the voltage range over which the current output of a current mode converter is accurate. This varies widely and can markedly affect the circuitry surrounding the converter. Finally, the input coding which the converter accepts as well as the input digital voltage thresholds with which it can interface are important, since the wrong code or wrong interface technology may require additional interfacing circuits between the original digital circuit and the converter. When all of these considerations are accounted for, it is not at all uncommon to spend a great deal more than the purchase price of a 10-bit converter for input interfacing, output amplification, external voltage references, and temperature compensation.

Specsmanship

Designers should also be keenly aware that the fine art of "specsmanship" is widely applied in the converter industry. For example, most manufacturers specify the "typical" settling time for a converter, rather than the maximum settling time. In general the maximum is twice the typical time. Furthermore, many manufacturers specify minimum and maximum parameter values only at $T_a = 25°C$, rather than giving minimum and maximum values over the full specified temperature range. Similarly, most specs are generated with the supply voltage close to the maximum allowable, rather than over the full range of supply voltages.

Glitches

Even more difficult is the problem of parameters which are seldom specified—in particular, the magnitude of glitches. Glitches in the converter's analog output are the result of different switching times for each of the switches in the resistor network. Fig 2 shows a typical problem; an intermediate glitch state occurs at the transition from 127/256 of full-scale voltage to one-half of full-scale voltage. For a short moment a full-scale output spike may be present. Fig 3 shows a very typical situation of voltage spikes occurring at various points during the conversion, primarily at the bit transitions where the most significant bits turn on and all

TIME	INPUT STATE	SWITCH OUTPUT STATE	DESIRED OUTPUT	ACTUAL OUTPUT
T_1	01111111	01111111	$\frac{127}{256}$ FS	$\frac{127}{256}$ FS
T_2	10000000	11111111	$\frac{1}{2}$ FS	FS GLITCH
$T_2 + T_G$		10000000	$\frac{1}{2}$ FS	$\frac{1}{2}$ FS

Fig 2 Full-scale glitch. At transition to ½ full-scale, glitch is caused by MSB current switch turning on before LSB switches turn off. (This problem is almost always present to some extent in D-A converters)

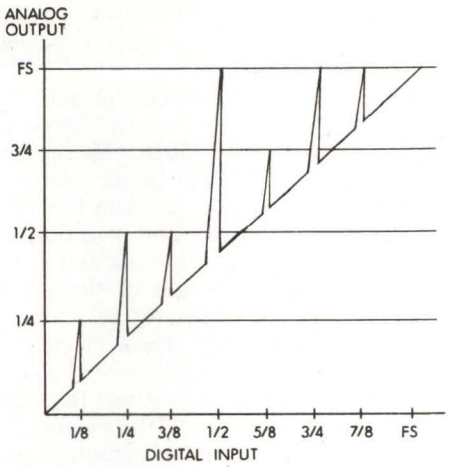

Fig 3 Voltage spikes. Typical glitches occur at transitions whenever one of the three MSBs turns on and all lower bits turn off

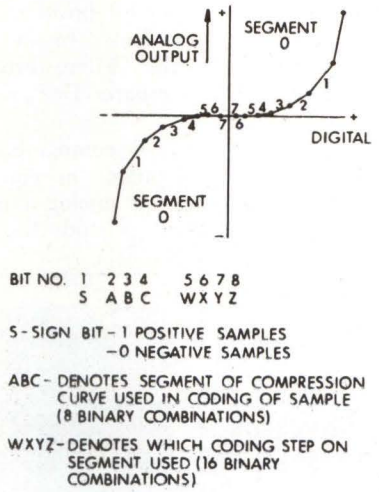

Fig 4 Companding technique. Companding converters provide an analog output that is exponentially related to the digital input according to the Bell μ255 standard for compression/expansion. Eight bits which enter are not straight binary code, instead they are interpreted with the MSB defining the sign of the output, the next three defining a linear voltage segment, and four LSBs a specific voltage point along the specified segment

lower bits turn off. The magnitude of these glitches varies widely from model to model, both in amplitude and duration, but the extent of the glitch is rarely specified in data sheets. These glitches are especially problematical when utilizing high speed DACs in a bipolar state. In this case, the maximum glitch occurs at the very smallest absolute voltages, when the transition from negative voltage to positive voltage is encountered.

The information above should help the reader interpret the specifications given in the Table. However, please note that the specifications were obtained from manufacturers' data sheets. Also note that the settling times stated are "typical" and that the power dissipation given is the "typical" power dissipation at the maximum supply voltage. Even so, the reader should not be dismayed by these specification problems, as they are by no means unique to monolithic DACs. Identical problems exist with both hybrid and discrete converters. Furthermore, for many of these performance parameters, monolithic converters surpass their hybrid or discrete technology counterparts. For example, temperature coefficients are extremely low for monolithic devices.

Recent Developments

One of the principal areas where converter manufacturers have concentrated research and development efforts, in their attempts to further reduce cost and improve performance, is the development of improved techniques for implementing precision resistors. At present, a number of techniques are utilized in implementing the resistor networks. Some manufacturers utilize untrimmed diffused resistors in their lower precision models. For higher precision, diffused resistors are utilized, but these are laser trimmed by cutting reverse-bias diode links between individual resistor segments. Another technology utilizes avalanche-induced migration (AIM) technology to "grow" links between diffused resistor segments. These techniques permit relatively quick trimming of the resistors in discrete steps. The number of steps, of course, limits the accuracy of the resistance. More accuracy can typically be obtained by utilizing nichrome resistors deposited on silicone. These resistors are then trimmed in size by a laser, permitting continuous variation of the resistance. All of these processes, however, are relatively time-consuming and capital intensive, and are, therefore, an impediment to continued cost/performance improvement at the present time.

A number of the devices listed in the table are worthy of special mention, as they represent important developments in D-A technology. The 12-bit Harris HI-562 converter has 200-ns settling time and ±¼ LSB accuracy, which represent a significant improvement in monolithic 12-bit converter performance. The National Semiconductor DA1200 is also an important development. This monolithic device incorporates not only resistor and switching networks but also a precision

voltage reference and operational amplifier, providing voltage mode as well as current mode output. Other manufacturers plan to introduce similar devices.

Another important development in monolithic converter technology is the introduction of microprocessor-compatible devices, such as Analog Devices' 10-bit AD-7522 and Signetics' 8-bit 5018. These devices incorporate a latch to hold the input data, allowing them to be attached directly to the data bus of a microprocessor. When the microprocessor performs an output instruction, data are placed on the bus and an I/O write control pulse is generated on one of the control lines. This pulse is used by the converter to strobe the data into the converter's input latch. These devices, attached directly to a microprocessor bus, need no intervening microcomputer output port to serve the data latch function. Such output ports would be required to interface most other DACs to a microcomputer system (although the cost of an LSI 8-bit I/O port, such as those provided on Intel's 8255, or Motorola's 6820, is only about $2.00). The 10-bit AD-7522 has the additional capability to interface to the microprocessor through a single 8-bit port. An 8-bit microprocessor would then output the 10-bit digital value to the converter in two successive output operations. The -7522 has the capacity to shift the data into the proper bit positions. A detailed description of interfacing this device to an 8-bit microcomputer was presented in the "Micro Processor/Computer Data Stack" column, *Computer Design*, June 1977, pp 203-205.

Precision Monolithics' DAC-76 companding converter is still another recent development in converter technology. This device provides an analog output that is (approximately) exponentially related to the digital input according to the Bell μ255 standard for compression/expansion. The eight bits which go into this converter are not a straight binary code. Instead they are interpreted, as shown in Fig 4. The most significant bit defines the sign of the output. The next three bits define one of eight linear voltage segments, and the four least significant bits define a specific voltage point along the specified segment. These eight segments approximate in a piecewise-linear fashion an exponential function. The purpose of this encoding is to obtain an output error which is approximately a constant percentage of the dynamic range of the input signal. Large input values have proportionately large changes from one analog output voltage to the next, while small digital inputs create very small analog changes from one output value to the next. This contrasts with a linear code where the change from one analog output value to the next is a fixed quantum amount regardless of whether the actual value is small or large. The effect of this technique is to provide 8-bit converter resolution over a 12-bit dynamic range. These companding digital-to-analog converters are extremely useful in digital speech communications.

Two chips which have not been discussed in this article are important because they are 5-V devices. They are the Ferranti ZN425E and the Datel ADC-MC8, and have not been included because they incorporate more than just a D-A circuit. They also include a counter and control logic that makes them ideal for use in inexpensive analog-to-digital (A-D) converters. These devices, more complete monolithic A-D converters, and a complete monolithic 16-channel data acquisition system, the National Semiconductor ADC-0816, will be covered in next month's column.

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CIRCLE 75 ON INQUIRY CARD

Single Chip Monolithic DAC Combines High Speed and 12-Bit Accuracy

Digital-to-analog converter performance previously available only in large and more expensive hybrid and modular devices is now available in monolithic form. Harris Corp's Semiconductor Products Div, PO Box 883, Melbourne, FL 32901 says that the HI-562 is the first 12-bit monolithic DAC to offer current output settling to ±½ LSB in 200 ns typ (400 ns max). In addition, worst-case absolute error over the full military temperature range is only ±1.5 LSB for unipolar mode operation (±2 LSB for bipolar), which the manufacturer claims makes this device one of the most accurate 12-bit DACs available in any form.

The fast settling speed has been achieved by using the company's high frequency bipolar dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized and drift is held to a low figure (±3 ppm of FSR/°C max) by including equally weighted current sources which are switched into an R-2R ladder network. The result is symmetrical on/off switching times and very uniform and constant thermal distribution within the chip. Thermal transients during switching are completely eliminated.

Large area, low ohms/square nichrome resistors permit precise laser trimming to an initial accuracy of ±⅛ LSB nonlinearity with a guaranteed maximum of ±½ LSB, as well as guaranteed monotonicity, over the full operating temperature range. Optional gain adjustment is accomplished by adding an external potentiometer between an external reference voltage and the reference input (pin 5 of pinout diagram) for unipolar operation. For bipolar operation an additional potentiometer for offset adjustment is connected between the reference and bipolar offset R input (pin 7).

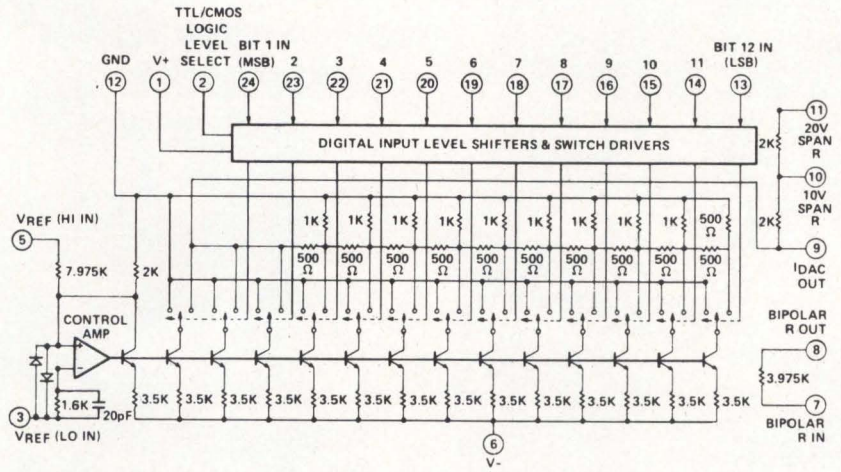
In addition to an external reference, the HI-562 requires a positive 4.75- to 12-V logic supply and a −15-V supply for operation. Digital inputs are TTL/DTL/CMOS compatible. For TTL, a 5- to 15-V supply is connected to V+ (pin 1). For higher voltage logic levels, pins 1 and 2 are tied together to the logic supply.

This DAC is pin-compatible with the Analog Devices model AD-562 hybrid except that it does not require external resistor-capacitor compensation components connected to the control amp summing junction (pin 4 of pinout diagram) for faster settling (3.5 to 1.5 μs); high frequency compensation is included internally for optimum high speed settling. Therefore pin 4 is not connected.

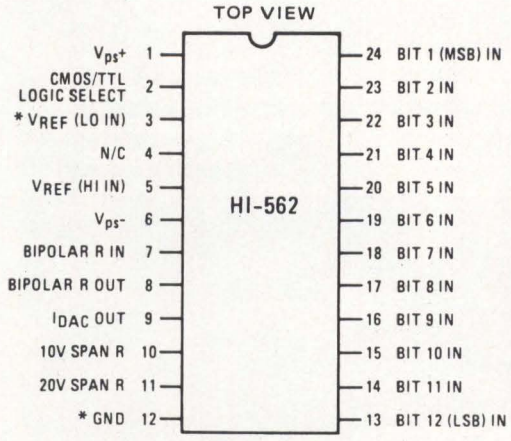
Three internal spanning resistors are provided for high accuracy current-to-voltage conversion with an external op amp for voltage output applications. By connecting these resistors in various combinations, output voltage range of ±10, ±5, ±2.5, 0 to 5, and 0 to 10 V can be selected when a 10-V reference is used. Output current capability of 5 mA assures that speed will not be degraded by the effects of stray capacitance loading.

Devices are specified for three operating temperature ranges: the -5 for 0 to 75°C, the -4 for −25 to 85°C, and the -2 and -8 for −55 to 125°C. All are packaged in hermetically sealed 24-pin DIPs. The -8 is processed to MIL-STD-883A Class B screening.

Circle 350 on Inquiry Card



Functional diagram of HI-562 DAC. High speed 12-bit monolithic device fits applications where hybrids and modular units have been used



Pinout diagram of Harris 12-bit DAC. Although pin compatible to AD-562 hybrid, pin 4 is not connected since external resistor-capacitor compensation components are not required at control amp summing junction

* Pins 3 and 12 connected to top and bottom case for high frequency shielding.

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Addressable Peripheral Drivers Simplify Circuitry In μProcessor Systems

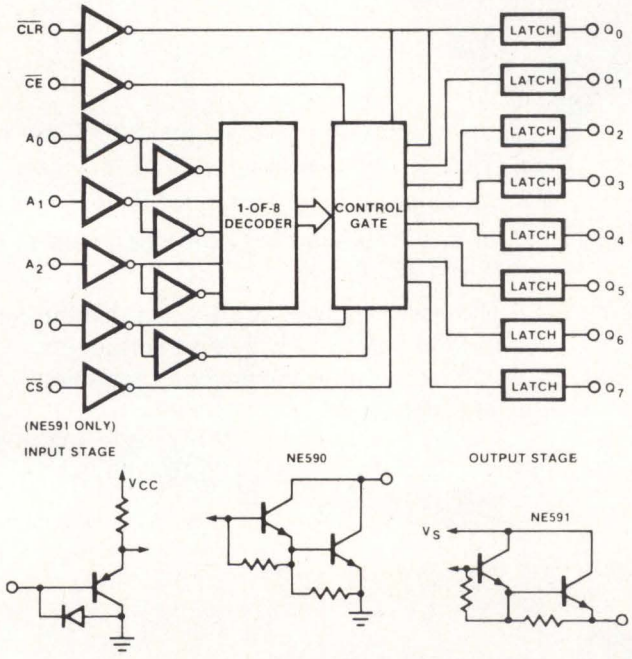
NE 590 and NE 591 are high current latched drivers with eight Darlington power outputs, each capable of 250-mA load current. Similar in function to the 9334 address decoder, the ICs provide a simple replacement for the complicated circuitry, discrete transistors, and Darlingtons required to trigger relays, lamps, LED displays, and stepper motors in microprocessor-based systems.

Developed by Signetics, 811 E Arques Ave, Sunnyvale, CA 94086, the NE 590 has eight open-collector Darlington outputs which sink current to ground. It operates in either addressable or demultiplex mode. Packed in a 16-pin molded or Cerdip package it is pin compatible with the 9334. Eight open-emitter Darlington outputs in the 591 source current to an external load from a common collector line, which may or may not be the same as the 5-V supply. It is packaged in an 18-pin molded or Cerdip package.

Both components feature low-loading, bus compatible inputs and allow random (addressed) data entry. A power-on clear feature ensures safe operation. Outputs are turned on or off by loading a logic high or low, respectively, into the device data input. Required output is defined by a 3-bit address. The device is enabled by a $\overline{CE}$ input line which also serves the function of further address decoding. A common clear input, $\overline{CLR}$ turns all outputs off when a logic low is applied.

Absolute maximum ratings include ambient temperature range of 0 to 70°C. At 25°C, power dissipation is 1 W and input voltage range is −0.5 to 15 V. Output current for each output is 250 mA and for all outputs is 1 A. Dc electrical characteristics include 2.0-V min input high voltage and 0.8-V max input low voltage. Max input currents range from −60 to 10 μA.

Circle 351 on Inquiry Card



Block diagram of NE 590/591 addressable peripheral drivers. High current latched drivers have eight Darlington power outputs, each capable of 250-mA load current, and can replace complex circuits presently necessary to turn on device with commands from microprocessors

3-Digit ADC Needs Only 10 Components to Form Complete DPM

A 3-digit IIL LSI circuit, the AD2020 requires only 10 components to form a complete digital panel meter. With an internal reference accurate to 50 ppm, the device serves as an alternative where low cost, simplicity, and reliability are more important than an extra ½ digit of resolution.

The chip includes input amplifier, comparator band-gap reference, counters, clock, control logic, multiplexer, and drivers needed to implement a dual-slope conversion DPM. Only a capacitor, three transistors, one decoder/driver, two potentiometers, and the three displays are needed.

Inputs from −99 to 999 mV are measured with an accuracy of 0.1% of reading ±1 digit. Balanced differential input rejects common mode voltages up to 200 mVdc, enough to eliminate most ground loop problems. Polarity detection is automatic, and plus and minus overload conditions are indicated through BCD coding. Zero shift is ±0.5 mV over the full operating temperature range, resulting in the same performance as a chip with auto-zero. Although the chip has an internal reference, it consumes only 50 mW of power and operates from a single 5-V supply.

Applications include use with LED or LCD displays where the chip performs all analog-to-digital conversion internally, feeding character serial data to the display driver. The hold input may be used as a pseudotrigger provided the trigger pulse is ≥5 ms; a conversion may be initiated only when all three digit lines are high and the hold line is low. As an A-D converter, digit select lines are used to strobe BCD data into latches. Hold, normal, and high speed conversion rates are controlled via voltage levels applied to the hold pin.

Packaged in a standard size 16-pin DIP, the chip is available in two ver-

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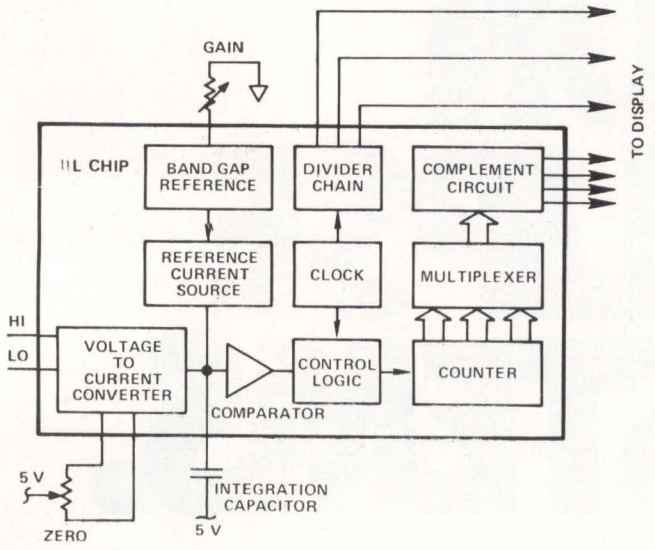


Analog Device's AD2020, a 3-digit IIL LSI chip, requires only 10 components to form a complete digital panel meter, thereby serving as an analog meter or digital indicator replacement where low cost and small size are more important than the extra ½-digit of resolution

sions with differing operating temperature ranges. Standard device is specified from 0 to 75°C; the double passivation and noble-metal interconnection scheme makes an extended temperature range version optionally available. The chip is offered by Analog Devices, Inc, Rt 1 Industrial Pk, PO Box 280, Norwood, MA 02062 at a per-unit price of $5.50 in 1000 quantities.

Circle 352 on Inquiry Card

CRT Controller Manages Display Memory, Handles Special Functions

Intended specifically for use in keyboard type terminals, the SF.F 96364 TV-CRT controller is an LSI chip that requires no setup of internal registers and no microprocessor support. Offered by Nucleonic Products Co, 6660 Variel Ave, Canoga Park, CA 91303, the chip allows fixed format display of 16 lines of 64 characters/line, is sensitive to data being entered into display memory, and offers capability to access more than one screen of data.

Manufactured in n-MOS silicon gate technology, the device automatically handles management of the display memory. Used with a 1024-word (6-bit min) static or dynamic memory and a 5 x 7 character generator, the device changes any TV set into a visual display, performing text refreshment, character writing, and cursor management. Line erase, line-end erase, and other functions make it compatible with any computing system.

Supplied in a 28-pin DIP, the device consumes 250-mW power typ from a single 5-V supply and is TTL compatible. Typical clock frequency is 1.6 MHz. Among its primary features are page linking capability, variable display size, character flicker capability, flickering cursor (2-Hz typ) mobile in four directions, read cursor address, and read memory capability for block transmission or hardcopy coupling.

Circle 353 on Inquiry Card

Dual Hammer Driver Combines High Current, High Voltage Capability

A dual 5-A hammer driver, the SH3011 can withstand 80 V between the collector and emitter of the output transistor. The drivers are independent of each other, and each is capable of sinking 5-A of current. Inputs are TTL compatible.

The device is well-suited for use in high voltage impact printers, stepper motor controls, solenoid drivers, large printers, and other applications that require a combination of high current and high voltage drive capability.

Fairchild Camera and Instrument Corp, Semiconductor Products Group, 464 Ellis St, Mountain View, CA 94062 supplies the device in a standard TO-3 metal can. Price is $5 in 100 quantities.

Circle 354 on Inquiry Card

3-Terminal Regulator Adjusts from —1.2 to —37 V

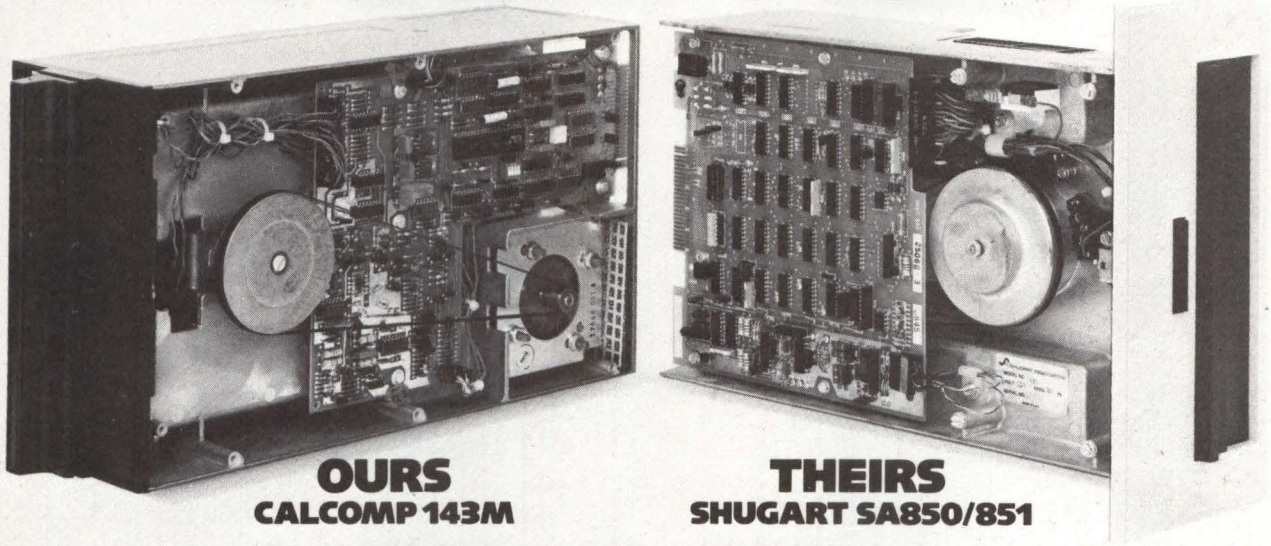
LM137 series monolithic ICs fill the need for negative adjustable regulators in standard 3-lead packages. Adjustable from −1.2 to −37-V with two external resistors, the series complements the LM117, also available from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, a 3-terminal positive adjustable regulator, to cover the full range of commonly used voltages.

A 1.5-A family that features internal current limiting, thermal shutdown, and safe area compensation, the devices are virtually blowout proof against overload. Line regulation is within 0.02%/V and load regulation is less than 0.5%. In addition, thermal regulation is specified to fully characterize the devices.

Thermal regulation is the effect that temperature gradients which occur when power is dissipated in an IC have on output voltage (in percentage output change per watt of power change). It is independent of electrical regulation or temperature coefficient and occurs within 5 to 50 ms after a change in power dissipation. It depends on IC layout as well as electrical design.

(Continued on p 166)

THERE ARE TWO SIDES TO EVERY STORY.



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- 50-pin compatible interface
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- hard *and* soft sectored
- *write current switching* in drive
- write precompensation *not required*
- one head fixed: *minimal* media wear

THEIRS
SHUGART SA850/851

- two-sided and double density
- industry standard format
- 50-pin compatible interface
- *etch-cuts* for variable functions
- hard *or* soft sectored
- *no write current switching* in drive
- write precompensation *required in controller*
- both heads move: *greater* media wear

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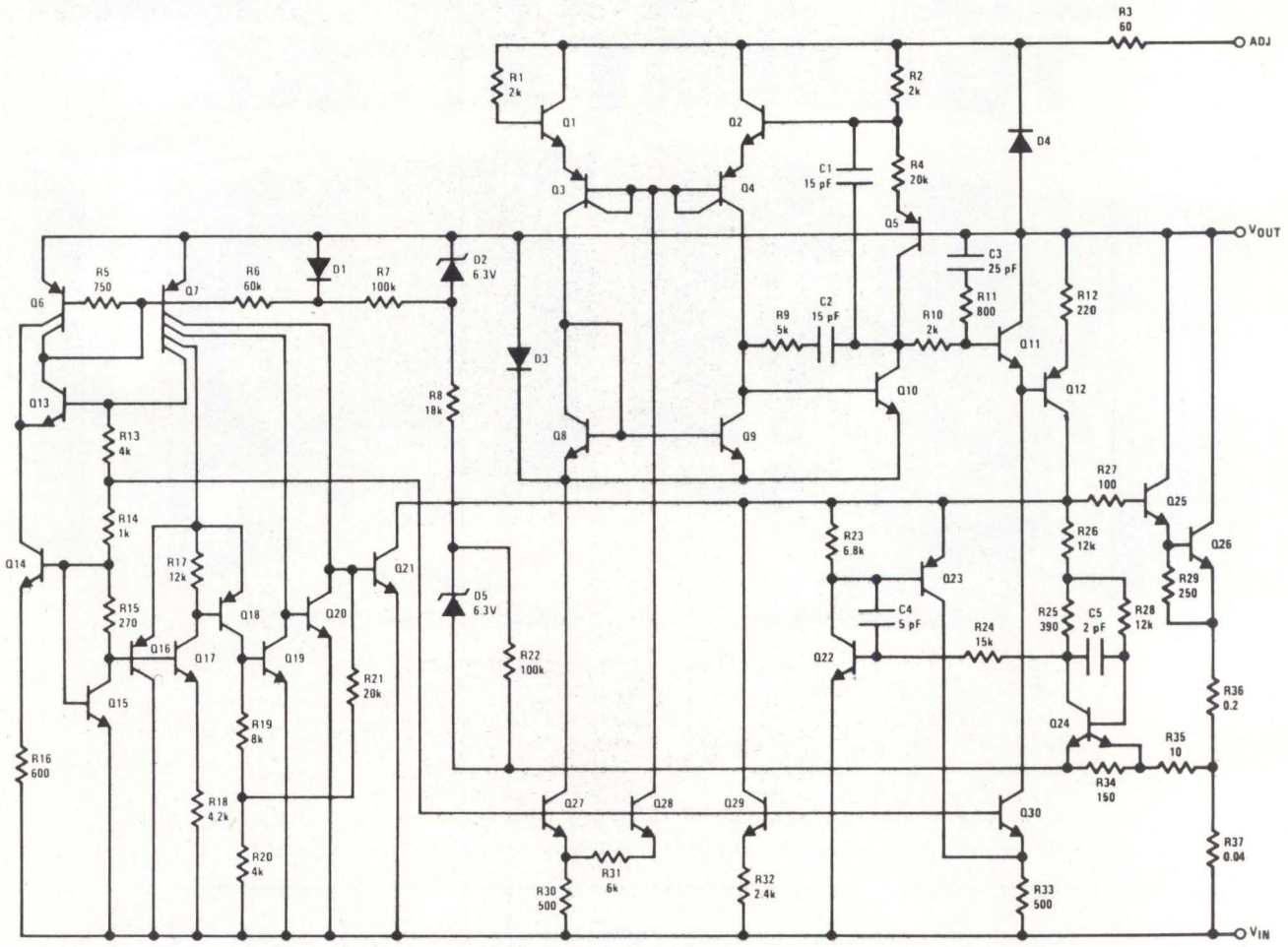

Claimed to be the first negative 3-terminal adjustable voltage regulators, National's LM137 series meets designers requirements for variable voltages and nonstandard voltage options. Thermal regulation, dependent on both IC layout and electrical design, is specified to be within 0.004%/W

Output voltage of the regulator is guaranteed to shift less than 0.2% when a 10-W pulse is applied for 10 ms. Other regulators are specified for only a few microseconds, before the junction warms up. If thermal regulation is not specified, users have no way of determining how well the device will perform. Its specification allows worst-case output change to be calculated easily.

The regulators are easy to use; two external resistors set the output voltage, and one output capacitor ensures dynamic stability and low output impedance. The −1.250-V reference voltage is stable to within 35 ppm/°C, preventing case temperature changes from degrading accuracy. Other features are high ripple rejection of 75 dB and an rms output noise of 0.003% of the output voltage up to 10 kHz.

Devices are available in TO-3 (steel), TO-5 (hermetic), and TO-220 and -202 (plastic) packages. Price for the LM137 guaranteed over the military temperature range from −55 to 150°C is $13.60 in TO-3; the LM337 over the commercial, 0 to 125°C range, is $3.60 in TO-3 and $2.80 in plastic TO-220 (quantities of 100-999).

Hybrid ADCs Operate From ±12-V Supplies

Hybrid IC analog-to-digital converter models ADC80AGZ-12 and -10 operate from ±11.4- to ±16.0-V supplies for compatibility with 12-V applications. The units, members of the ADC80 line from Burr-Brown, International Airport Industrial Pk, Tucson, AZ 85734, provide all performance characteristics of the line, including logic supply of from 4.75 to 16 Vdc.

The 10- and 12-bit successive approximation A-D converters are com-

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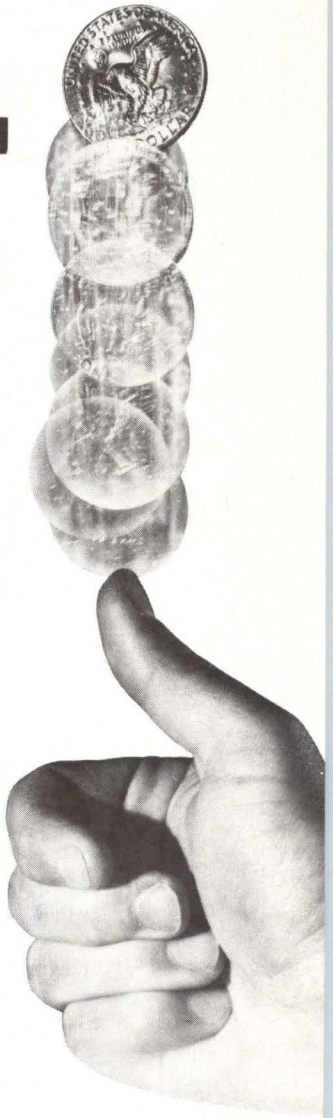

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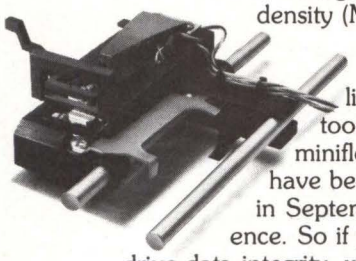

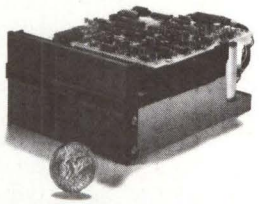

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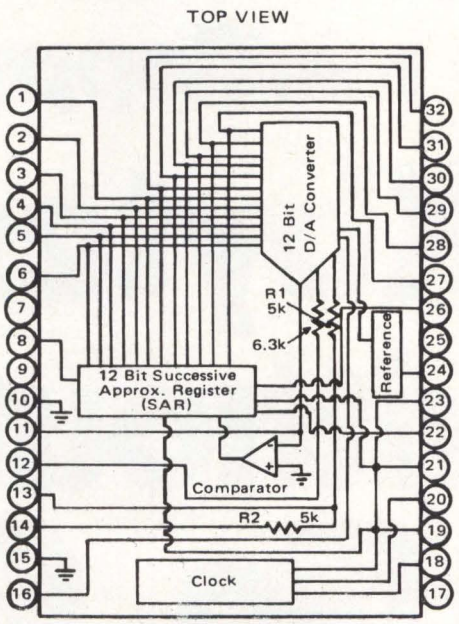

PIN CONNECTIONS

1. Bit 6	32. Bit 7
2. Bit 5	31. Bit 8
3. Bit 4	30. Bit 9
4. Bit 3	29. Bit 10 (LSB-10 Bits)
5. Bit 2	28. Bit 11
6. Bit 1 (MSB)	27. Bit 12 (LSB-12 Bits)
7. +5V Analog	26. Serial out
8. Bit 1 (MSB)	25. -15V
9. +5V Digital	24. Ref. out (+6.2V)
10. Digital Common	23. Clock out
11. Comparator IN	22. Status
12. Bipolar Offset	21. Short Cycle
13. R1 10V Range	20. Clock Inhibit
14. R2 20V Range	19. External Clock
15. Analog Common	18. Convert Command
16. Gain Adjust	17. +15V

Burr-Brown's ADC80AGZ analog-to-digital converters operate from ±11.4- to ±16.0-Vdc supplies to provide compatibility with ±12-V applications. Connection diagram indicates pinouts for standard 32-pin package

plete with internal reference, clock, and comparator. They use IC and laser-trimmed thin film components and are housed in compact 32-pin packages. Thin-film scaling resistors allow analog input signal ranges of ±2.5, ±5, ±10, 0 to 5, or 0 to 10 V to be selected. Gain and offset errors may be externally trimmed to zero, offering initial accuracy of better than ±0.0122% ±½ LSB.

Conversion speeds are 25 μs for 12-bit and 21 μs for 10-bit resolution. Speeds up to 23 μs for 12 bits, 12 μs for 10 bits, and 6 μs for 8 bits are possible with an external clock. Data are available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are DTL/TTL compatible.

Prices for the units in 32-pin ceramic packages are $49.50 for the 12-bit and $47 for the 10-bit converter in quantities of 100.

Circle 355 on Inquiry Card

DACs Offered for Low Linearity Applications

Designers requiring low linearity, low cost digital-to-analog converters for particular applications are now offered four such products by Micro Power Systems, 3100 Alfred St, Santa Clara, CA 95050. Two, the MP-7520G and -7521G, have 6-bit linearity while the -7520H and -7521H are rated at 7 bits. Resolution is 10 bits for the 16-pin -7520 DIPs and 12 bits for the 18-pin -7521 pair. All are available in either plastic or ceramic.

These DACs contain highly-stable, thin film R-2R ladders, plus CMOS current switches on monolithic chips (10 switches for -7520 converters, 12 for -7521 converters). For most applications, only the addition of an output operational amplifier plus a voltage or current reference are required.

Circle 356 on Inquiry Card

12-Bit CMOS DACs Are μP Compatible

Both series 7545 and series 7546 hybrid digital-to-analog converters have two input registers separate from the switch holding register, each of which can separately be enabled to accept a 12-bit input data word in 4-bit (MSBs) and 8-bit (LSBs) bytes from an 8-bit microprocessor bus. They can operate in a serial input mode or a parallel input mode and can alternately be switched from one mode to the other. Input translators on input registers can accept either TTL inputs using a 5-V supply or CMOS inputs using 5- to 15-V supply levels. Separate holding register and input register power supply lines allow this flexibility without compromising linearity. These devices, announced by Beckman Instruments, Inc, PO Box 3100, Fullerton, CA 92634, are said to be the first single-package, microprocessor compatible DACs to offer 12-bit accuracy and low power CMOS internal circuitry.

Series 7545 is a 4-quadrant multiplying model implemented by bipolar digital proportioning of an ac external reference; 2-quadrant multiplication can be implemented by either unipolar proportioning of an ac reference or bipolar proportioning of a unipolar dc reference. It can be used with a wide range of supplies to accommodate TTL or CMOS standard supply levels where digital and analog subsystems operate on different supplies. Typical power consumption is <10 mW.

Series 7546 includes series 7545 circuitry and incorporates additional output amplifiers for unipolar and bipolar operation and a precision 10-V reference. Each amplifier is laser-adjusted for zero offset and the precision thin film ladder network and feedback resistors are ratio-matched. The precision voltage reference allows the converter to be configured as a general-purpose DAC. Although the reference is preset and specified to 10 V ±10 mV, an adjustment pin permits setting the reference within the range of 10 ±0.5 V.

Commercial versions of both series use a polymer seal; military versions are hermetically sealed. Commercial series 7545C is priced at $22.50 in quantities of 100; commercial series 7546C is $40.50 in quantities of 100.

Circle 357 on Inquiry Card

When it comes to flexibility, the Infoton 400 Data Display terminal can hand you all you need.

Designed around the Z-80 microprocessor, it offers complete control of all Blocking and Editing functions through software settable modes. One thing that's especially easy to handle about the I-400 is its cost; at $1,095 in quantities of 100 or more, it's the most versatile terminal for the price you can get your hands on.

Infoton 400

More information on the I-400 is quickly within your grasp. Call Infoton toll-free at (800) 225-3337 or 225-3338. Ask for Barbara Worth. Or write Barbara Worth at Infoton, Second Avenue, Burlington, MA 01803.

Prepared by Chickering/Howell, Los Angeles.

CIRCLE 80 ON INQUIRY CARD

INTEGRATED COMPUTER SYSTEMS, INC.

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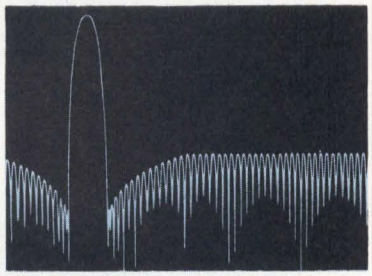
Digital Signal Processing



LOS ANGELES
May 2-5
WASHINGTON D.C.
May 9-12
TORONTO
June 6-9
BOSTON
June 20-23

Course 440 — Four days

Fiber Optic Communication Systems

LOS ANGELES
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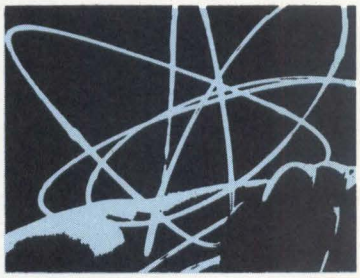
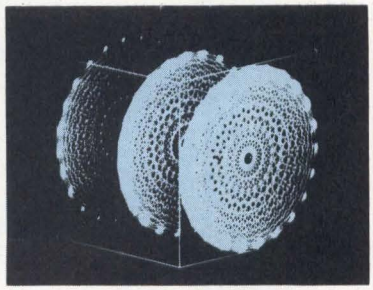
TORONTO
May 30-June 2
BOSTON
July 11-14
WASHINGTON D.C.
July 25-28



Course 365 — Four days

Computer Graphics



LOS ANGELES
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WASHINGTON D.C.
May 16-19
TORONTO
July 11-14
BOSTON
July 18-21
SAN FRANCISCO
July 25-28

Course 350 — Four days

Distributed Processing and Computer Networks

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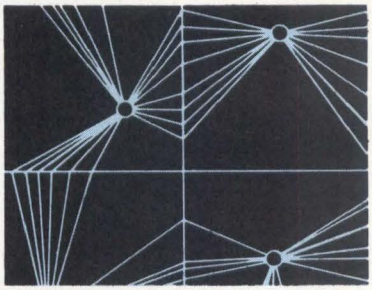
May 9-12
TORONTO
June 13-16
BOSTON
June 20-23
ASPEN
July 11-14



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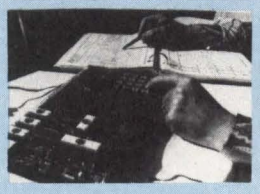

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TECHNICAL EDUCATION

SELF-STUDY MICROCOMPUTER TRAINING

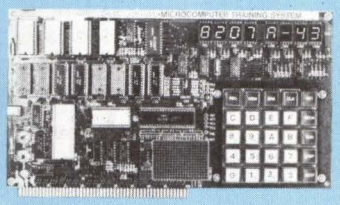
COURSE 525 SELF-STUDY MICROCOMPUTER SOFTWARE/HARDWARE TRAINING COURSE

WHAT THIS TRAINING COURSE IS! (and is not)

- **This is a truly tutorial course based on a 650-PAGE WORKBOOK/TEXT with specific learn-by-doing hardware/software exercises (it is NOT a set of skimpy documentation and operational manuals).**
- **This is a FULLY ASSEMBLED AND TESTED microcomputer system (it is NOT a kit—thus saving days of frustrated debugging).**
- **This is A COMPLETE SYSTEM with BUILT-IN KEYBOARD AND DISPLAY (it is NOT a useless "start-up" system requiring expensive peripherals such as a TTY or CRT).**
- **This course is based on the 8080A MICROPROCESSOR (it is NOT an unpopular microprocessor of little value for future work).**
- **This system is portable and ready to use in your office or home for "hands-on" experience at your own pace.**

Using the Training System, you will be taught both programming and hardware through clear explanations and scores of exercises on your own microcomputer. You will first learn each 8080 instruction through simple exercises which illustrate its effective use. These exercises then progress to more and more advanced techniques. Other exercises specifically teach how to debug your programs quickly and effectively. Furthermore, throughout the course, hardware design projects are coordinated with programming problems.

THE TRAINING COMPUTER INCLUDES:



- The 8080 Microprocessor • 0.5K CMOS RAM (with capability for battery back-up) • 1K MONITOR PROM • 3 parallel 8-bit I/O ports • Two serial ports • DMA channel • On-board 8-digit display and 25-Key Keyboard

Furthermore, the computer is easily expandable (see Course 536 below).

KEY TOPICS

• Introduction to the training system • Hardware fundamentals • Software fundamentals • The 8080 instructions – one by one • Using the keyboard/display to load and check programs • I/O programming – parallel/serial • Using a programmable I/O device • Interrupt handling (vectored/priority) • Organizing data in program (PROM) and data (RAM) memory • Subroutine structures • Advanced math routines (trig, logs, floating point, etc.) • Advanced I/O – block data and DMA use • Annotated work sheets for designing and implementing your own application

$545.00 TOTAL PRICE

Includes: 8080A training microcomputer, educational monitor, coordinated 650-PAGE WORKBOOK/TEXT with exercises, software, flowcharts, block diagrams and schematics. A separate power supply (+5V-2.0A, +12V-0.8A) is available for $95.00.

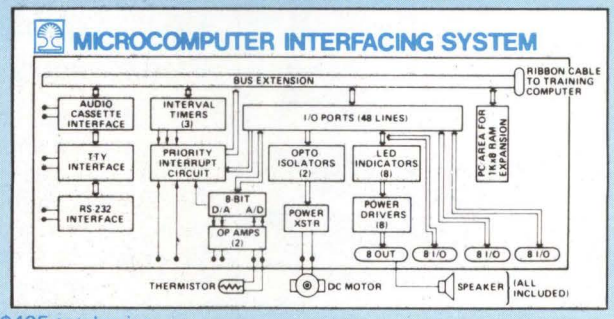
COURSE 536 SELF-STUDY MICROCOMPUTER INTERFACE TRAINING COURSE

This new Hands-On Interfacing Course includes a FULLY ASSEMBLED INTERFACING SYSTEM ready to connect with the training computer of Course 525, together with a 450-PAGE WORKBOOK/TEXT with dozens of exercises to teach you both the hardware and software to interface to the real-world.

In addition to analog and digital I/O, other features include: Cassette interface for easy program storage and retrieval on any audio cassette recorder, RAM expansion space for larger programs, and TTY/RS-232 interfaces. Also included is a cassette with dozens of advanced programs including mathematics, games (ping-pong of course) and a real-time executive.

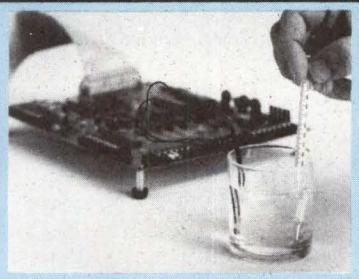
KEY TOPICS

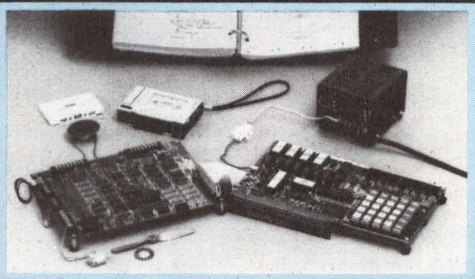
• Introduction to the interfacing hardware • INTEL 8255 I/O ports • INTEL 8253 Interval Timer • Real-time Clock • Cascaded Timers • Waveform Generators • Numerical Integration • Pulse Width Modulation • D/A Conversion • Music Generation • Motor Speed Control (open and closed loop) • A/D conversion • Digital Voltmeter • Digital Thermometer • Calibration • Linearization • Proportional Temperature Control • Real-time Interrupt-driven Executive • Advanced Interfacing Techniques



$495 total price

Includes: Interfacing System, cable to training computer, coordinated 450-PAGE WORKBOOK/TEXT with exercises, programs, flowcharts, block diagrams and schematics, and cassette with programs.





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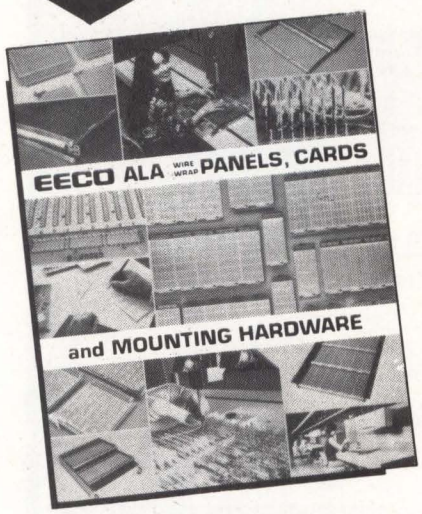

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AROUND THE IC LOOP

Quarter-Micron n-MOS FET Fabricated Successfully

Silicon gate, n-MOS field-effect transistors with gate geometries as small as 0.25 micron by 0.25 micron have been successfully fabricated in the Electronics Research Center laboratories of Rockwell International Corp, 3310 Miraloma Ave, Anaheim, CA 92803 using electron beam lithography and dry processing techniques. The 0.25-micron FET is believed to be the worlds' smallest n-MOS transistor, breaking the commonly-accepted 0.5-micron "lower limit." It may also be the fastest—during dynamic characterization of 61-stage ring oscillators constructed with this device, the 0.25-micron FET was shown to have an operating speed of 12 GHz.

Its development was discussed in a paper presented by Dr Michael T. Elliott at the International Electron Device Meeting (IEDM) in Washington, DC. Dr Elliott's paper summarized an investigation of the physical limitations on silicon MOS structures, which was partially funded under a contract from the Naval Ocean Systems Center.

Circle 358 on Inquiry Card

Agreement to Share 64k CCD Memory Concluded

An agreement between National Semiconductor and Intel will provide an alternate source for high density 64k-bit CCDs. According to the agreement, the two companies will share the design of Intel's 65,536-bit CCD serial memory. Intel will supply tapes and working plates for its 2464 device, while National will conduct its own wafer fabrication, assembly, and testing of the product. Predictions are that National's MM2464 will be available in volume later this year.

p-MOS Detector Fits Low Cost Alarm Systems

Intended as a component for micropower sensing alarm and detection systems which require a high input impedance comparator and alarm driving capability, the L911 monolithic, bipolar, p-MOS detector contains MOSFET input comparator, trip point comparator, internal trip point reference, output driver, and pulsing output oscillator. It requires the addition of only a few resistors to control set current of the IC and threshold setting of the input comparator. The output can be used for logic triggering or with higher current driver SCRs or transistors.

Key features of this device from Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054 include high input impedance comparator with $R_{in} > 10^9\ \Omega$; adjustable comparator input threshold, common-mode range from gnd to 4 V below supply voltage; less than 10-μA current consumption from a 9-V alkaline battery, allowing 1-year life in standby condition; adjustable output current sourcing from 0.5 to 30 mA; optional latched output; 6- to 16-V supply range; and reverse battery protection.

IR LEDs Offer Increased Output at Lower Cost

An infrared diode chip offered by Siemens AG, Postfach 103, D-8000 München 1, Federal Republic of Germany has a radiant intensity of 10 mW/sr. Although this is twice the intensity of its predecessor, LD 261 will sell at the same price as the earlier chip and manufacturing is expected to reduce that price in the near future. Increased lumen output permits operation with lower forward currents, which should result in longer service life at the same luminance. Applications include perforated tape or card readers, miniature photocell gates, and shaft position encoders.

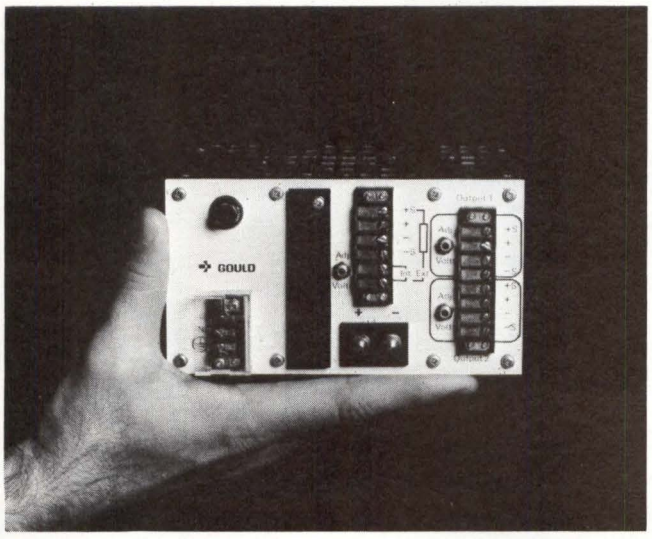
Circle 359 on Inquiry Card

Custom IC Program Licensed

An agreement between Stewart-Warner Corp and Dionics, Inc grants Dionics the exclusive license to produce and sell certain custom ICs developed by Stewart-Warner for itself and others under its SWAP (Standard Wafer Array Programming) program. [Under this concept, an array of cells is fabricated on a standard wafer (using IIL technology) and, depending upon the individual customer's logic requirement, a simple but distinct interconnection of those cells then creates the customized circuit.] Dionics was also licensed to produce for Stewart-Warner several of its custom CMOS ICs and to use such technology for other general industry requirements. □

The big switch

...is to smaller lighter switchers.



The 200 watt MGT 5-20A: 7" x 6.4" x 3.5", 7.5 lbs.

Switching power supplies average about ⅓ the size and ¼ the weight of linears. And in many applications that's reason enough to make the switch. But it's not the only reason. Compared to linears, switchers can cut energy consumption in half, generate far less heat, and offer better holdup protection. That's why more than 40,000 Gould switchers are already in use around the world.

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For more information or to arrange for an evaluation unit contact Gould Inc., Electronic Components Division, 4601 N. Arden Drive, El Monte, CA 91731. Telephone (213) 442-7755.

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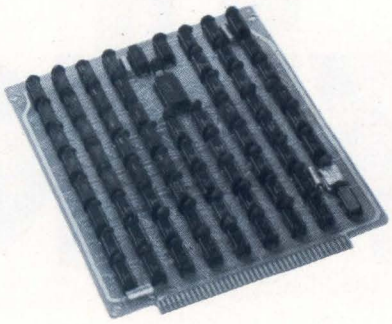
PRODUCT FEATURE

Single-Board Bipolar Computer Emulates Any Mini or Microcomputer

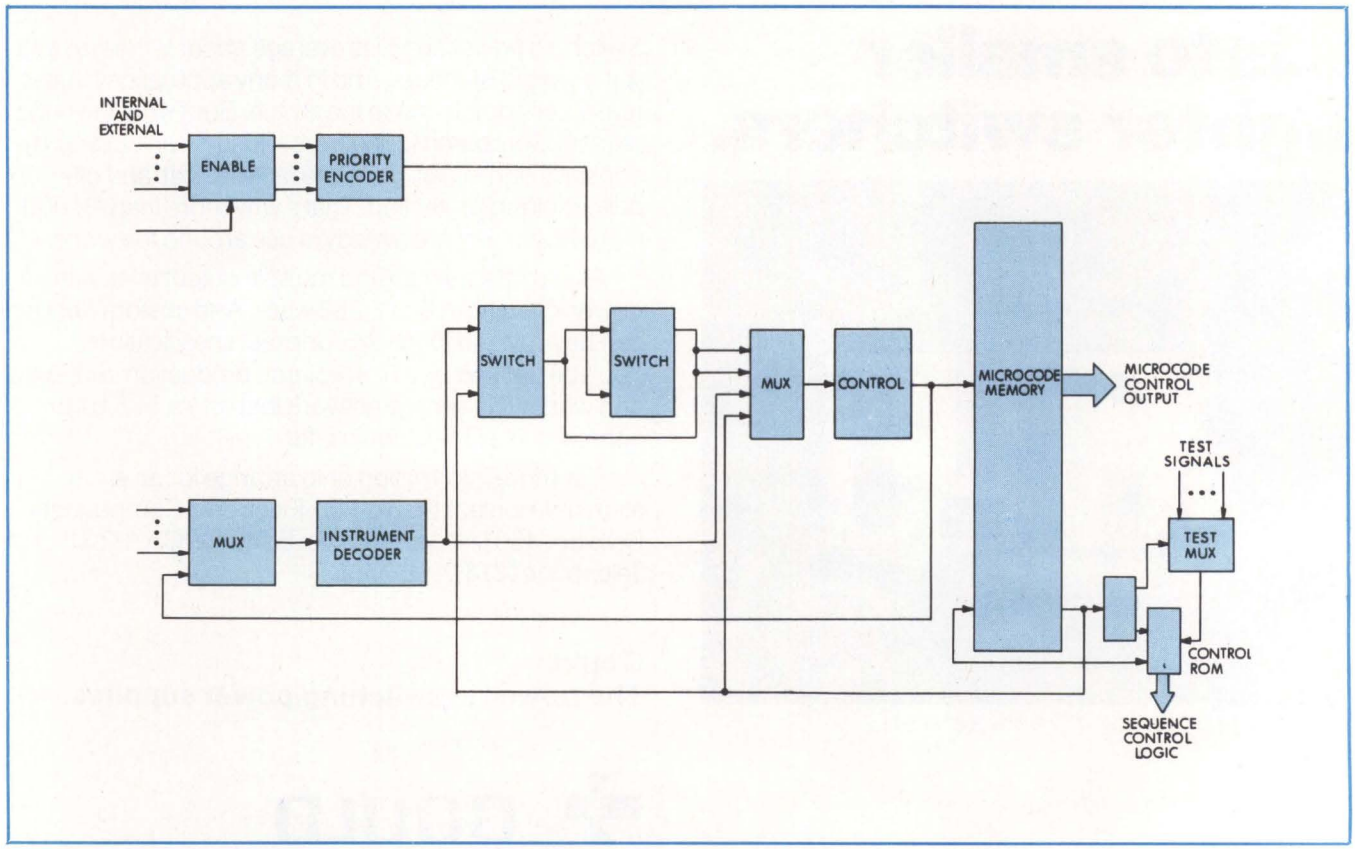
For those cases where an existing mini or microcomputer cannot meet expanded system requirements or is not adequate for new product development—too slow or not powerful enough—the T-1000 general-purpose binary processor can be substituted as an alternative for the original CPU. According to the manufacturer, this single-board bipolar, MSI minicomputer can be microprogrammed to run the instruction set of any known mini or microcomputer. It emulates the replaced CPU and operates on the existing software—but at higher performance levels; the cost and time required to prepare new software are eliminated.



Bit slice architecture enables this minicomputer to emulate computers with 8-, 12-, 16-, or 32-bit word lengths. Dynamic Sciences, Inc says that nominal performance of 300k operations/s is better than that of existing MOS microcomputers and many other bipolar minicomputers.

Operating Features

Emulation control is derived from a 1k x 32-bit microprogrammable memory. The CPU contains 16 full word (16-bit) hardware registers. Up to 65k words of memory can be directly



addressed; in some configurations 262k words of extended addressing are available. A direct memory access channel is provided.

Instruction control and execution speed are derived from interpretive microprogrammable memory and data option modules such as floating point and memory management. These options as well as additional memory, programmed I/O, and various interfaces are available on additional boards. Microinstruction execution rate is 10 MHz. Throughput will vary, depending on particular machine being emulated and data option modules selected.

The manufacturer builds the proper instruction set into ROM to enable the board to emulate the desired mini or microcomputer and to function with whatever language, hardwired items, memory, and peripherals are being used in the system. Connectors are added according to the customer's requirements. Because this minicomputer is tailored to the user, its board size as well as the board sizes of additional options can be customized to fit any space limitations. Minicomputer and options are available as either a card set or in a self-contained unit.

Modular partitioned architecture accommodates most mechanical installation requirements. This modularity also eases maintenance and modifications or upgrading. Component count is held to a minimum and reliability is increased by byte architecture and interpretive instruction control.

Both military specification and commercial versions are available. Reliability can meet MIL-STD-883, with boards ruggedized for difficult environments within the −55 to 125°C temperature range.

The minicomputer operates off a single 5-V supply. CPU power consumption is 8 to 16 W depending upon model and options.

Price and Delivery

Prices of the T-1000 minicomputer depend upon the computer being emulated and the options included. Basic 100-up quantities start at $1000. Delivery is 90 days ARO. Dynamic Sciences, Inc, 7660 Gloria Ave, Van Nuys, CA 91406. Tel: (213) 782-0820.

For additional information circle 199 on inquiry card.

1 In Conversion Efficiency: Fast-transition switching circuits and low-loss magnetics optimize efficiency for given size and weight. Thermal gradients closely controlled. No derating over full rated temperature range.

2 In Source/Load Isolation: Extremely high isolation permits complete separation of load circuits from input bus, even for high CMV.

3 In Freedom from Kickback: High-attenuation filters minimize inverter-switching spikes and reflected ripple current, protecting other loads across same DC bus. Many models include EMI/RFI shielding, permitting location of converter module near sensitive logic circuitry.

4 In Power per Unit Volume and Unit Area: Some conserve "real estate," others minimize total volume or height. Minimal case-temperature rise, with only free-air convection. No heat sinks or cooling fins required.

5 In Short-Circuit Protection: Positive protection is built in; type and limits are suited to the intended class of applications. Some include both automatic current-limiting and automatic restart; others "fold back."

6 In Static/Dynamic Regulation and Stability: High-frequency inverters and fast, high-performance regulators ensure excellent transient response. Superior thermal design ensures very low T.C. Static regulation, rated for "worst-case," is consistently superior to conventionally margined regulators.

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There's no such thing as a "routine" application for a DC-DC converter. Simple in concept, converters can create some very complex problems – reducing reliability margins, adding unforseen costs, driving you to circuit "fixes," even to circuit redesign. But Intronics' DC-DC converters, like our AC/DC supplies, anticipate and prevent those problems. Modestly priced, their *true value* lies in what they save you *after* installation.

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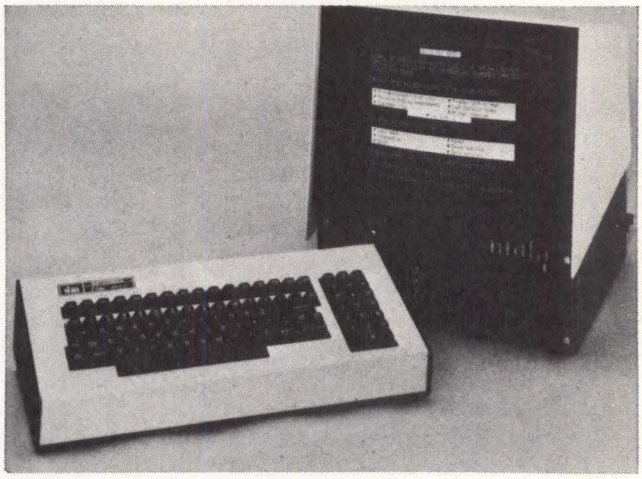
CIRCLE 84 ON INQUIRY CARD

PRODUCTS

Microprocessor-Based Video Terminal Provides Reliable Operation for Transaction Processing

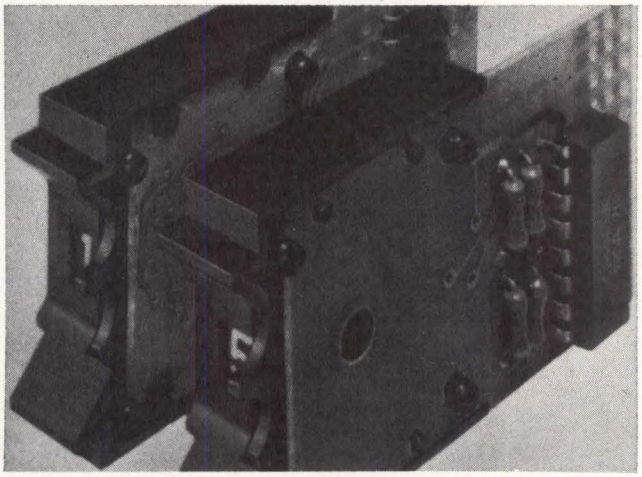
The Elite 3025A is a buffered Teletype® compatible CRT terminal with a single-page video memory that displays 1920 alphanumeric char in a 24-line/80-char format. It provides communications capabilities with a data processing system, minicomputer, or other peripherals supporting full- or half-duplex, 2- or 4-wire, internally or externally clocked, asynchronous communications. Features include local edit, remote, batch, batch modified, format, format modified, and transparent operating modes; host control of block transmit function in local or remote environment; asynchronous and optional isochronous communications interfaces; 103 and 202 modem compatibility (201 modem compatibility with the isochronous interface); and switch-selectable EIA and optional 20-mA current loop interfaces. Also included are 10 user function keys, detached keyboard, and 15 selectable baud rates up to 9600. **Datamedia Corp,** 7300 N Crescent Blvd, Pennsauken, NJ 08110.



Circle 200 on Inquiry Card

Thumbwheel Switches With Built-in Logic Functions Speed Design and Simplify Packaging

Line of "Smart Switches" includes 12 types of digital comparators and 4 types of counter/timer decades, which can be cascaded. Std configuration is the company's series S, front or rear mounted, "No-Hardware" system in which units snap together into various assemblies. In addition, switches mate with blank spacers, half-spacers, dividers, and end plates by snapping together. Digital comparators incorporate a BCD decade comparator. The switch converts the decimal number displayed by the switch into a BCD (1,2,4,8) format. For increased noise immunity, pullup resistors are provided at the switch. Units are available with either CMOS or TTL/DTL. Counter/timer decades incorporate an SN7490N (TTL) or MM74C90 (CMOS) chip. When the BCD of the counter is equal to the BCD equivalent of the decimal digit displayed by the switch, an equal signal is output at the common of the switch. **Unimax Switch Corp,** Ives Rd, Wallingford, CT 06492.



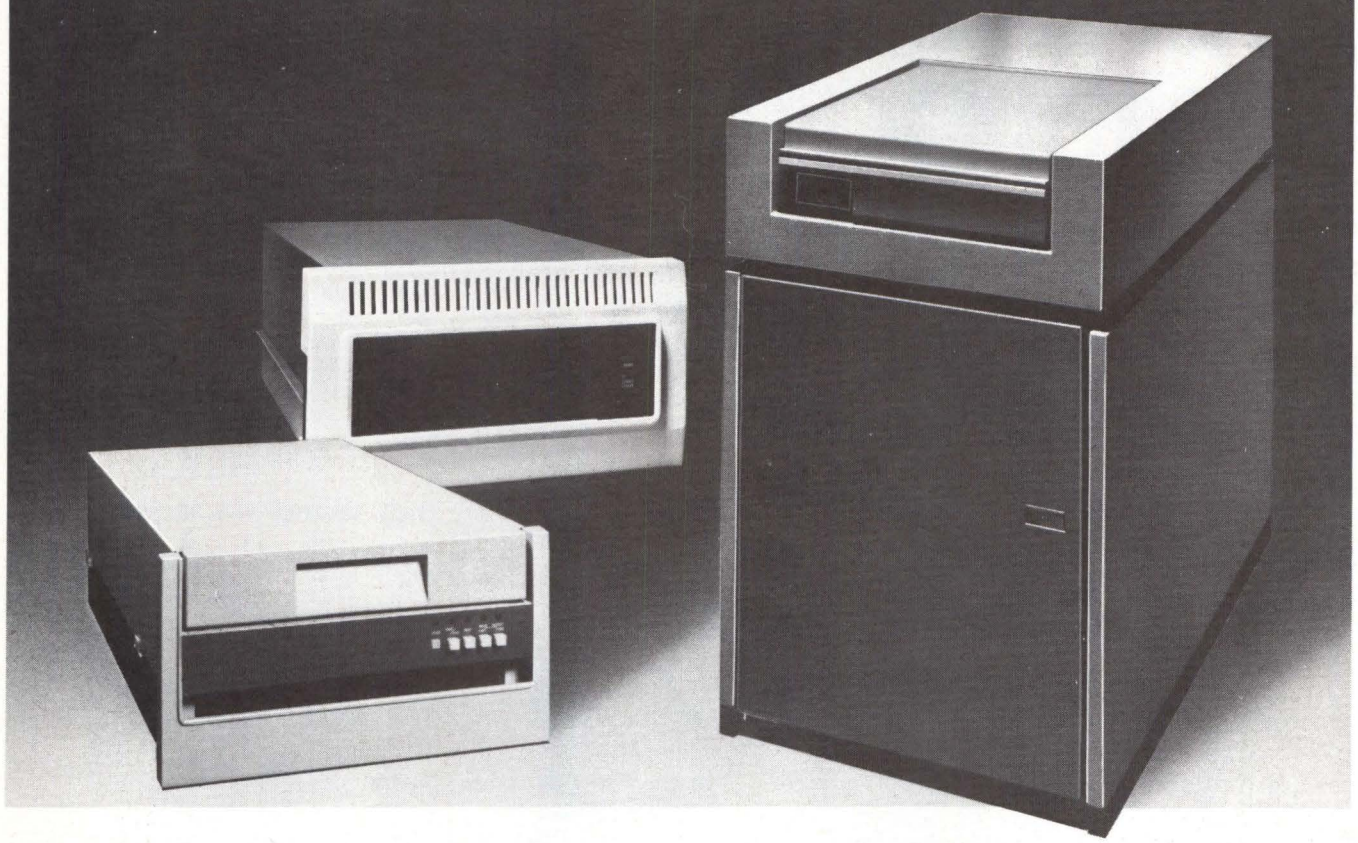
Circle 201 on Inquiry Card

Desktop Punched Tape Systems Serve Communications and Microprocessor Applications

Featuring pushbutton controls for tape duplication and automatic tape feeder preparation (with feed holes or all holes punched), the 8050 series is available in reader/perforator or perforator-only configurations; both styles are available with built-in RS-232-C serial interface for compatibility with data communications peripherals. Perforator motor, which is idle during nonpunching time for silent standby operation, functions at 50 char/s. Circuitry includes a 128-byte buffer for asynchronous operation in a parallel mode, or burst operation up to 1200 baud in serial mode. Reader mechanism can process std 5-, 7-, and 8-channel tape and 6/8-channel typesetter tape in both directions at a rate of 300 char/s, or up to 2400 baud with the serial interface. Selectable interface send and receive rates are 110 to 9600 baud and 110 or 1200 baud, respectively. **Ex-Cell-O Corp, Remex Div,** 1733 E Alton St, PO Box C19533, Irvine, CA 92713.

Circle 202 on Inquiry Card

There are many measures of quality in an OEM module drive from Control Data.



Here are three of them.

Greater System Flexibility

Our Storage Module Drive (SMD) has removable media. Our Mini-Module Drive (MMD) has fixed media. And Our Cartridge Module Drive (CMD) has both. Capacities start at 12 megabytes and range to 300 megabytes.

But all share compatible interface software and firmware. That means easy system integration, simple field upgrades. Without expensive modification of your design. It's the type of flexibility that saves money—for both you and your customer.

Exceptional MTBF Reliability

Control Data has a reputation for building module drives that last. We're backing it up with continued testing and feedback. And we design and manufacture all critical components in-house. We can build reliability into our drives because we built it into our heads, servos and media.

And Value That Matches Performance

We know we have the best and most reliable drive for your application. But we also have the competition beat on cost of ownership. Send us the coupon below. We will help you compare our lower cost-per-bit, our lower entry costs with others.

For more info on our SMD family, call us at 612/853-3399. Or, return coupon to:

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OEM General Manager, Product Sales
Control Data Corporation Dept. CD-38
P.O. Box 0, Minneapolis, MN 55440

Please send info on your ☐ SMD ☐ CMD ☐ MMD

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Company _____ Address _____

City _____ State _____ Zip _____

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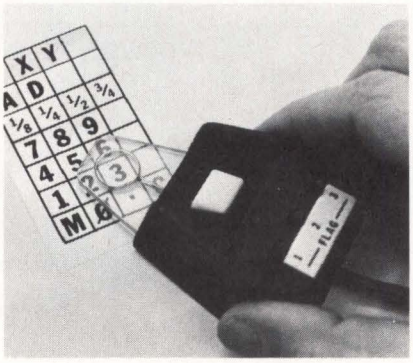
CONTROL DATA CORPORATION

More than a computer company

How to program a digitizer.

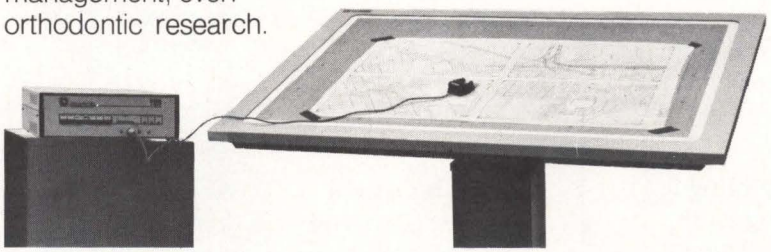
Just touch the free-moving cursor to the program menu pad. It automatically programs the Summagraphics ID (Intelligent Digitizer) for scaling, skew correction, area calculation, linear distance or other user defined functions.



That's because the Summagraphics ID has built-in microprocessor control. And we've done the programming. So when you touch the menu pad, you call up the program for the function you need.

The built-in microprocessor has other advantages. It means that you don't have to program your computer to do board-level operations, don't have to tie up system memory. It makes relocatable origin, binary/BCD conversion, metric output and incremental operation all standard, switch- selectable functions. And it makes the Summagraphics ID easier to interface, easier to operate and more efficient to use.

Application Notes: Call or write Summagraphics for application notes describing use of digitizers in circuit design, drafting, geophysics, land management, even orthodontic research.



Summagraphics® corporation

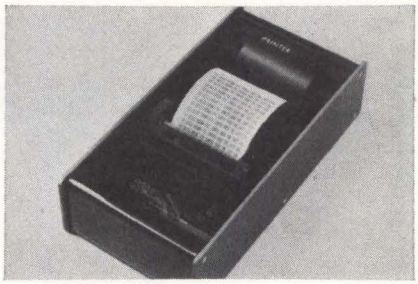
35 Brentwood Ave., Box 781, Fairfield, CT 06430
Phone 203/384-1344. TELEX 96-4348

PRODUCTS

NONVOLATILE HIGH SPEED SEMICONDUCTOR RAM

Model 4020, a single-card memory, maintains data for a min of 3 mo (6 mo typ) after the primary board power is removed. Size and word width are 2k x 8 or 9, or 1k x 16 or 18, jumper selectable. The 5 x 10" (12.7 x 25.4-cm) card features a 450-ns access time; bank select within 64k; 5-V, or 7- to 10-V power input at 260 mA; phase programmable operating controls, and separate data inputs and outputs that may be bused together. **ElectriCom Co,** 12567 Crenshaw Blvd, PO Box 1235, Hawthorne, CA 90250.
Circle 203 on Inquiry Card

DOT MATRIX MINIPRINTER



The 5 x 7 dot matrix printer for microcomputer systems uses electrosensitive paper to make permanent copies at speeds up to 88 char/s with 44 char/line. A 4.5 x 8.75" (11.43 x 22.23 cm) enclosure houses printer and paper supply mounted on an interface board with necessary components for connection to any microcomputer with TTL levels. Microcomputer controls the motor and print electrodes with an 8-bit parallel output word, and senses timing signals on 2 input lines. **Electronic Product Associates, Inc,** 1157 Vega St, San Diego, CA 92110.
Circle 204 on Inquiry Card

HIGH CONTACT DENSITY CIRCULAR CONNECTOR

Miniature connector features a "scoop-proof" design that eliminates the possibility of contact damage in blind mating applications. Rear release system allows contact retention. Connector meets performance requirements of MIL-C-38999 and operates at a −65 to 200°C temp range. 58 crimp, snap-in contact arrangements are available to accommodate from 3 to 128 contacts using AWG wire sizes 16 through 28. **International Telephone and Telegraph Corp, Cannon Electric Div,** 666 E Dyer Rd, Santa Ana, CA 92702.
Circle 205 on Inquiry Card

The Quad Squad

If you own a PDP-11 or an LSI-11, you made a great buy. Now we've got something that will make your buy look even better. It's the quad squad, the latest in the Able line of enhancers for the PDP-11 family. We're talking about the unusual cards that give you four asynchronous communication channels each while presenting only one load to the Unibus. There are four of them. The EIA-serial QuadrAsync/B™, a DL-11B replacement. The QuadrAsync/C™, a 20 mA current-loop alternative to the DL-11C. The EIA-serial QuadrAsync/E™, a DL-11E replacement. And the QuadrAsync/LSI™, a DLV-11 replacement which gives the LSI-11 user four asynchronous EIA and/or 20 mA serial channels.

All four condense onto a single quad board four times that which is on the DEC unit they are replacing. Yet there is relatively little requirement for bus repeaters and expansion boxes to increase the number of available channels. Operation is full duplex or half duplex with both the transmitter and receiver for each channel operating at the same baud rate. Each model is system software compatible with the unit it replaces.

These boards are available off the shelf. They are priced competitively. They install in minutes. They provide immediate results. And, in every instance, they outperform the competition. They should. We are the only *computer* people in the business and are clearly the most qualified to help. That's one reason why we outsell all our competition combined. Write for details. We'll include information on our Univerter™, Re-bus™ and cache memories. Able Computer Technology, Inc. 1751 Langley Avenue, Irvine, California 92714. (714) 979-7030. TWX 910-595-1729.

Able, the computer experts

PDP, DEC, UNIBUS, LSI, DL-11B, DL-11C, DLV-11 and DL-11E are registered trademarks of Digital Equipment Corporation.

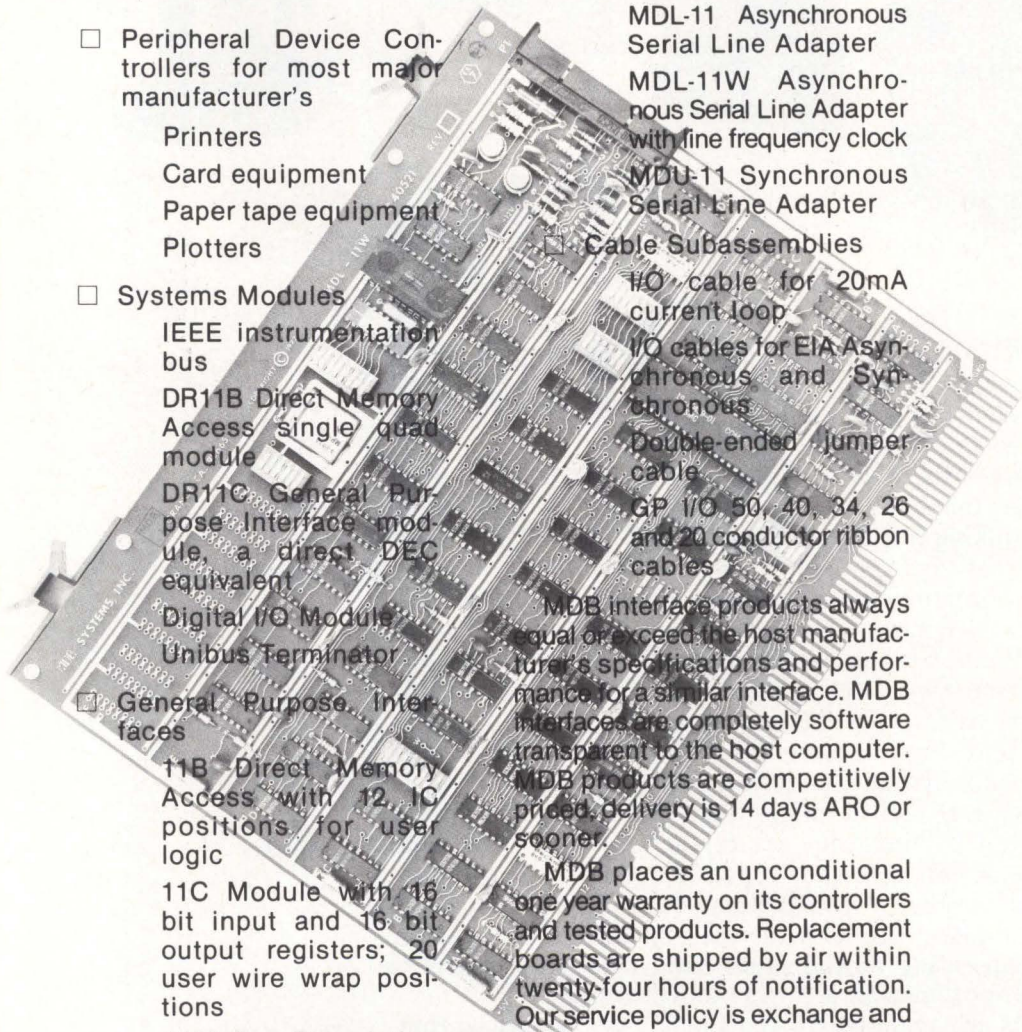
CIRCLE 132 ON INQUIRY CARD

PDP-11* interface . . . from MDB

Peripheral Device Controllers ▪ Systems Modules
General Purpose Interface Modules
Communications/Terminal Modules
I/O Cables ▪ Accessory Hardware

When it comes to PDP-11 interface, MDB has it:

- ☐ Peripheral Device Controllers for most major manufacturer's
  - Printers
  - Card equipment
  - Paper tape equipment
  - Plotters
- ☐ Systems Modules
  - IEEE instrumentation bus
  - DR11B Direct Memory Access single quad module
  - DR11C General Purpose Interface module, a direct DEC equivalent
  - Digital I/O Module
  - Unibus Terminator
- ☐ General Purpose Interfaces
  - 11B Direct Memory Access with 12 IC positions for user logic
  - 11C Module with 16 bit input and 16 bit output registers; 20 user wire wrap positions
  - 1710 Bus Foundation Module with pins for 40 user IC positions
  - Wire Wrappable Module with pins for 70 user IC positions
- ☐ Communications/ Terminal Modules
  - MDL-11 Asynchronous Serial Line Adapter
  - MDL-11W Asynchronous Serial Line Adapter with fine frequency clock
  - MDU-11 Synchronous Serial Line Adapter
- ☐ Cable Subassemblies
  - I/O cable for 20mA current loop
  - I/O cables for EIA Asynchronous and Synchronous
  - Double-ended jumper cable
  - GP I/O 50, 40, 34, 26 and 20 conductor ribbon cables



MDB interface products always equal or exceed the host manufacturer's specifications and performance for a similar interface. MDB interfaces are completely software transparent to the host computer. MDB products are competitively priced, delivery is 14 days ARO or sooner.

MDB places an unconditional one year warranty on its controllers and tested products. Replacement boards are shipped by air within twenty-four hours of notification. Our service policy is exchange and return.

MDB also supplies interface modules for LSI-11*, Data General and Interdata computers. Product literature kits are complete with pricing.

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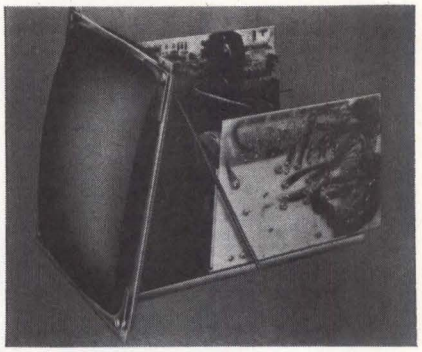
CIRCLE NO. 86 FOR LSI-11; 87 FOR PDP-11; 88 FOR NOVA; 89 FOR INTERDATA

PRODUCTS

WORD PROCESSING/ TEXT EDITING CRT MONITOR



Using a 15″ (38-cm) CRT to display up to 64 lines of text, 96 char/line, the noninterlaced HRD-15 system scans at 50k lines/s. Dot resolution is rated at 0.01″ (0.25 mm) with clear definition, since rise/fall time is <3 ns. Std phosphor is P-4 with others available upon request. Designed for text processing applications, the readable, high density screen is engineered for use 8 h/day without eyestrain. **CPT Corp,** 1001 Second St S, Hopkins, MN 55343.
Circle 206 on Inquiry Card

DC-TO-SYNCHRO CONVERTER MODULE

The unit develops a fully isolated 400-Hz, 11.8-V line-to-line, 3-wire ac output whose angle is linearly proportional to an input dc signal. Providing 0.5-VA full power output, it requires ±15 Vdc at 100 mA for full load with a 26-V ±10% 400-Hz reference voltage. Line-to-line sinusoidal ac output is insensitive to ±10% reference voltage variations. Specs include accuracy of 15 min of arc, full range dc inputs of ±10 V for a transfer function of ±18 deg/V, and tracking accuracy of 720 deg/s. **General Magnetics, Inc,** 211 Grove St, Bloomfield, NJ 07003.
Circle 207 on Inquiry Card

QUAD OUTPUT POWER SUPPLY

This PC board mountable power supply is part of the Micro-Supply family, which consists of an ac adapter plus regulated dc-dc converters. Typ quad output supply offers 5, 12, −12, and −5 V. Series has an overall height of <0.5″ (1.27 cm). Converter portion measures 2.25 x 3.25 x 0.45″ (5.72 x 8.23 x 1.14 cm) and is encapsulated in a rigid case. Wall plug-in unit measures approx 2 x 2 x 1.8″ (5.1 x 5.1 x 4.6 cm). **Scientific Programming Inc,** 1499 Bayshore Hwy, Suite 126, Burlingame, CA 94010.
Circle 208 on Inquiry Card

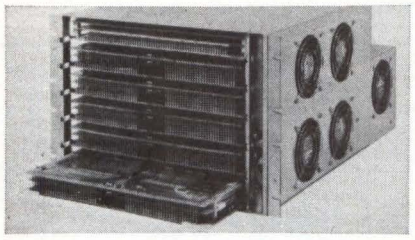
OPTICALLY COUPLED ISOLATORS

Three series of isolators feature 5630-Vdc isolation between their GaAs LED inputs and silicon phototransistor outputs. Packaged in 6-pin DIPs, SPX 7110, 7130, and 7150 are designed for microprocessor and solid-state relay applications, and provide 10 to 50, 30 to 80, and 50 to 125% CTR at 1-mA input current, respectively. 7530, 7550, and 7590 operate at 5-mA input current, while the 7270 to 7273 series offers controlled gain at 10 mA. Rise and fall times are 5 μs typ. **Spectronics, Inc, Commercial Components Div,** 830 E Arapaho Rd, Richardson, TX 75081.
Circle 209 on Inquiry Card

ECL IC DYNAMIC TEST SYSTEM

The S357 pulse parametric subsystem features a 10-ps resolution over a 0- to 20-ns range, and fully programmable pulse sources with voltage resolution of 1 mV from 200 mV to 2 V. Pulse parameters are automatically and independently calibrated at programmed values, and automatic deskew software corrects for system errors down to 50 ps. Flexible I/O pin configuration permits user to assign as many as 30 input or output pins and up to 24 I/O pins. **Teradyne, Inc,** 183 Essex St, Boston, MA 02111.
Circle 210 on Inquiry Card

BULK CORE MEMORY SYSTEM



Designed to augment storage capacities of medium to large scale computer systems, a single BCM 760 module has max capacity of 128k words x 20 bits, with 18- and 16-bit word configurations available. A std enclosure houses up to 6 modules or a total storage capacity of 65M bits. Max addressable memory in any given system is 32 modules. Composed of two independent core stacks and associated electronics, the module measures 15 x 17.5 x 1.8" (38 x 44.5 x 4.6 cm). Full cycle time is 1.5 μs; data access time is 500 ns. **Fabri-Tek Inc,** 5901 S County Rd 18, Minneapolis, MN 55436.
Circle 211 on Inquiry Card

200-W SWITCHING POWER SUPPLY

Series C offers 5 V regulated at 40 A with other models ranging up to 28 V regulated. RMK supply is fully enclosed with built-in emi filters, overvoltage protection, current limiting, soft start, remote on/off control, and high efficiency (75% typ) of a 25-kHz switcher. Providing easy accessibility, single PC card construction allows units to run cooler. Size C modules are 4.0625 x 5.125 x 8.75" (10.3188 x 13.018 x 22.23 cm); weigh 5.25 lb (2.36 kg); and produce >200 W of voltage stabilized power. **Kepco, Inc,** 131-38 Sanford Ave, Flushing, NY 11352.
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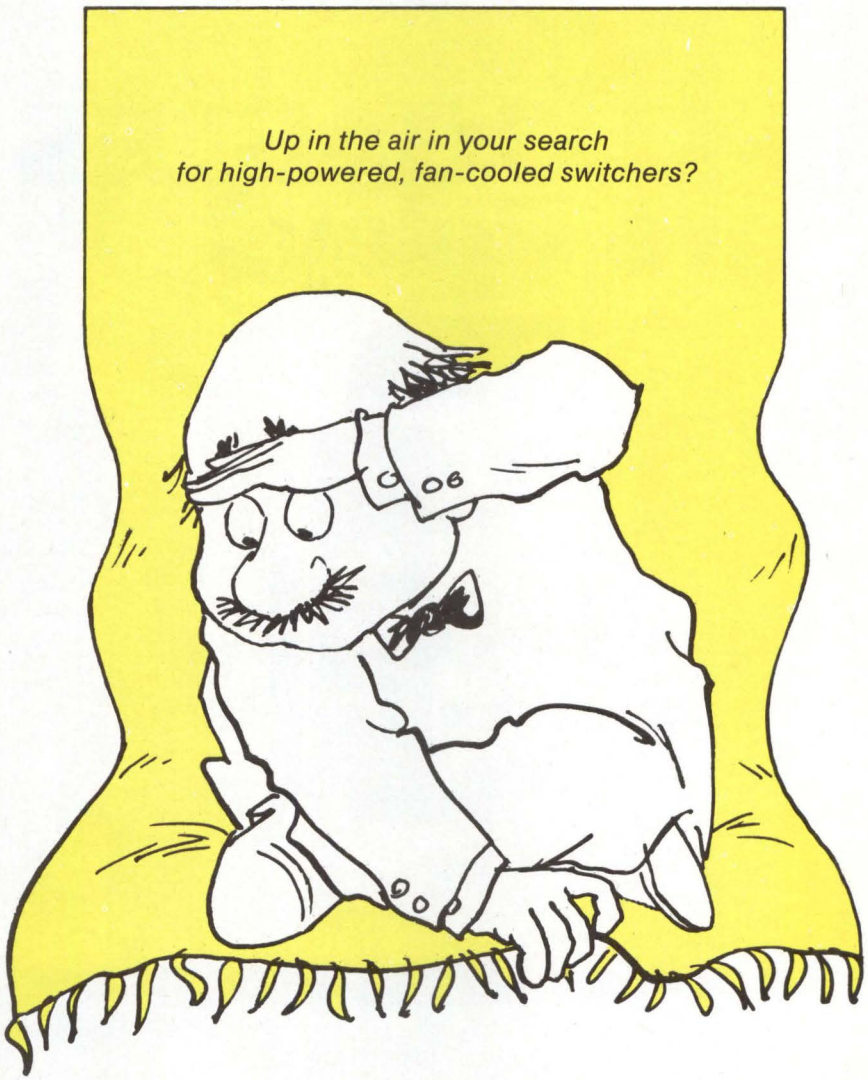
Up in the air in your search for high-powered, fan-cooled switchers?



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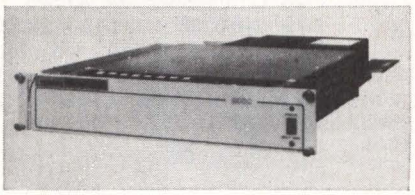
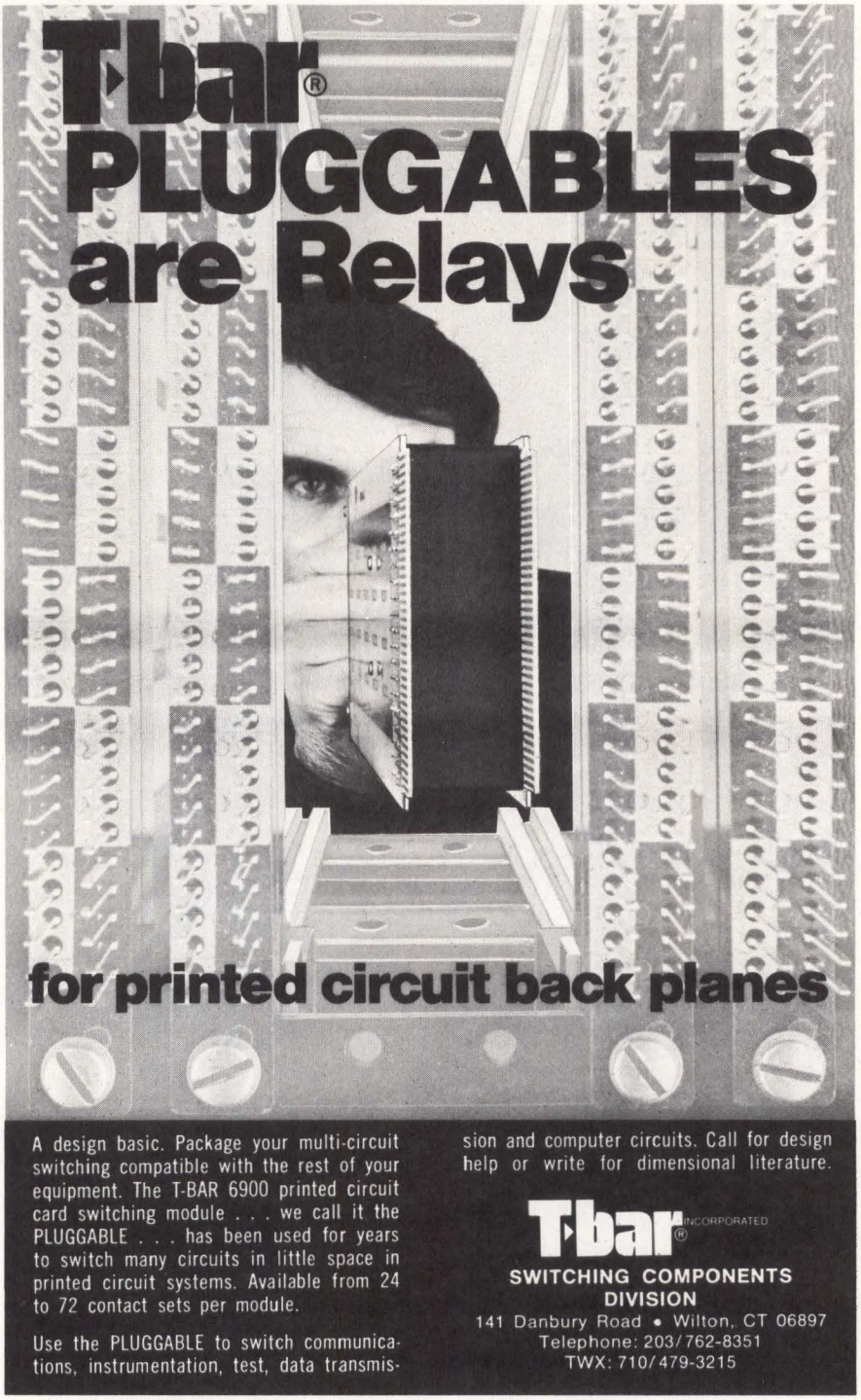
EMERSON®

RASTER SCAN IMAGING AND GRAPHICS SYSTEMS



The solid-state 9050 series of TV image generation systems are capable of displaying color, gray scale, and black and white. Resolution may be specified as 256 lines x 256 elements to 16 bits (RM-9150); 256 lines x 512 elements to 8 bits (-9250); 512 lines x 512 elements to 4 bits (-9350) or 16 bits (-9351). Composite video signals drive TV monitors, hardcopy printers and plotters, and large screen displays. Assorted computer interfaces are available, as are optional custom video boards, keyboards, and cursor controllers. **Ramtek Corp,** 585 N Mary Ave, Sunnyvale, CA 94086.
Circle 213 on Inquiry Card



A design basic. Package your multi-circuit switching compatible with the rest of your equipment. The T-BAR 6900 printed circuit card switching module . . . we call it the PLUGGABLE . . . has been used for years to switch many circuits in little space in printed circuit systems. Available from 24 to 72 contact sets per module.

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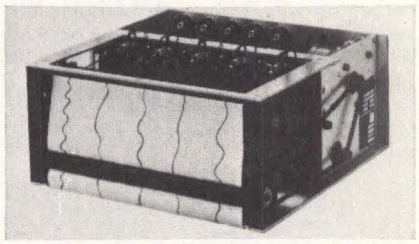
5-CHANNEL OSCILLOGRAPH RECORDER

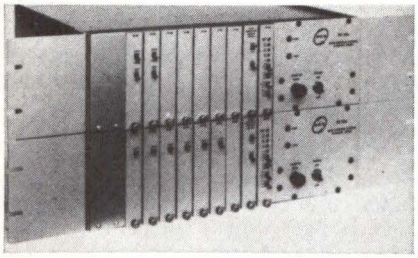


The TMD-540 offers a frequency response of dc to 100 Hz ±3 dB, sensitivity of 10 mV/div, and linearity of >1% at full scale. Each channel is 40 mm wide. Self-contained chart recorder unit includes a power supply/transformer and an integrated pen motor/amplifier. Std chart speeds are 25 and 50 mm/s. Recorder utilizes an indirect coaxial thermal stylus with sturdy ceramic tip for recording on rectilinear chart paper. Unit's dimensions are 5.5 x 13 x 11.875" (13.97 x 33 x 30.163 cm). **Gulton Industries, Inc, Measurement and Control Systems Div,** East Greenwich, RI 02818.
Circle 214 on Inquiry Card

MESSAGE LOGGING SYSTEM TALKING CLOCK

TCE-124 automatically logs time of day on the company's recording systems in English, German, or Arabic. Custom speech synthesis microcontroller produces vocabulary electronically. Instrument inserts a distinct verbal announcement immediately following a recorded message; each message is indexed with its own time reference. Features include 12- or 24-h format; visual LED display; monitor speaker; MSI/LSI circuitry; 1-W, 8-Ω audio output; and universal I/O control circuits. **Omnicron Electronics,** PO Box 623, Putnam, CT 06260.
Circle 215 on Inquiry Card

ALARM AND CONTROL TELEMETRY SYSTEM



Basic function of the ACT-200 system is to provide parallel-to-serial conversion of discrete data levels and convert them to a serial PCM bit stream for transmission over telephone lines to a remote location. Simplex, half-duplex, and full-duplex configurations are available. Expansion up to 225 channels of digital data in groups of 25 channels is possible. Designed to transmit and receive digital signals typical to process control and monitor systems, it can incorporate a modem module or use an external modem. **Data-Control Systems, Inc,** PO Box 584, Danbury, CT 06810.
Circle 216 on Inquiry Card

HIGH RESOLUTION CASSETTE HEAD

Model 71001 single channel and 71002 are dual gap mag tape heads designed for high reliability performance with a std cassette (with or without pressure pads). With low feedthrough of <2%, model 71002D has a max density of 6250 fcpi and meets ANSI, ECMA, and ISO proposed stds. Specs include write track width of 0.057 ±0.002" (14.5 ±0.05 mm), read track width of 0.036 ±0.002" (0.9 ±0.05 mm), tape speed of 10 in (25.4 cm)/s, and current rise time of 2 μs. **Creative Magnetics, Inc,** 49 E Industry Ct, Deer Park, NY 11729.
Circle 217 on Inquiry Card

TTY A,B SELECTOR SWITCH, PATCH, AND MONITOR MODULE

Model 8916 contains switching, patching, and serial monitoring functions for 2 independent data channels at the terminal-modem TTY current interface. Designed to operate with the model 8964 controller and power module, up to 8 monitor modules are housed in an 8903 cage assembly, which mounts in a std 19" (48-cm) cabinet. Remote control of the entire system is available. Bulk and individual channel switching is performed by means of A,B switches. **International Data Sciences, Inc,** 100 Nashua St, Providence, RI 02904.
Circle 218 on Inquiry Card

SEALED MICROMINIATURE POTENTIOMETER

Models 3391 and 3392 single turn potentiometers are designed for use in miniature circuit applications including handheld probes and hybrid circuits. Features include an optional switch with positive detent, linear or nonlinear tapers to match amp circuits, and an O-ring providing a dust and moisture resistant seal. Models are available in 9 std resistance values ranging from 1 to 500 kΩ. Std resistance tolerance is ±20% and contact resistance variation is 3% max. **Trimpot Products Div, Bourns, Inc,** 1200 Columbia Ave, Riverside, CA 92507.
Circle 219 on Inquiry Card

4" x 3" x 4"/Hi Performance/Lo Power
One Moving Part/Hard Mounted Motor

	DENSITY	
	800 bpi	1600 bpi
Tracks	1 or 2	1 or 2
Capacity (bytes) 1 Track	160,000	320,000
2 Tracks	320,000	640,000
Transfer Rate (bits/sec)	24,000	48,000
Speed Read/Write Rewind/Search	30 ips 90 ips	

AVAILABLE WITH:

- READ-AFTER-WRITE HEAD
- PIA INTERFACE
- READ/WRITE ELECTRONICS
- MOTION ELECTRONICS
- MOUNTING FRAME

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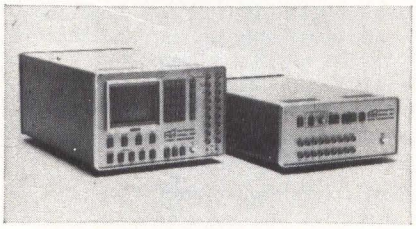
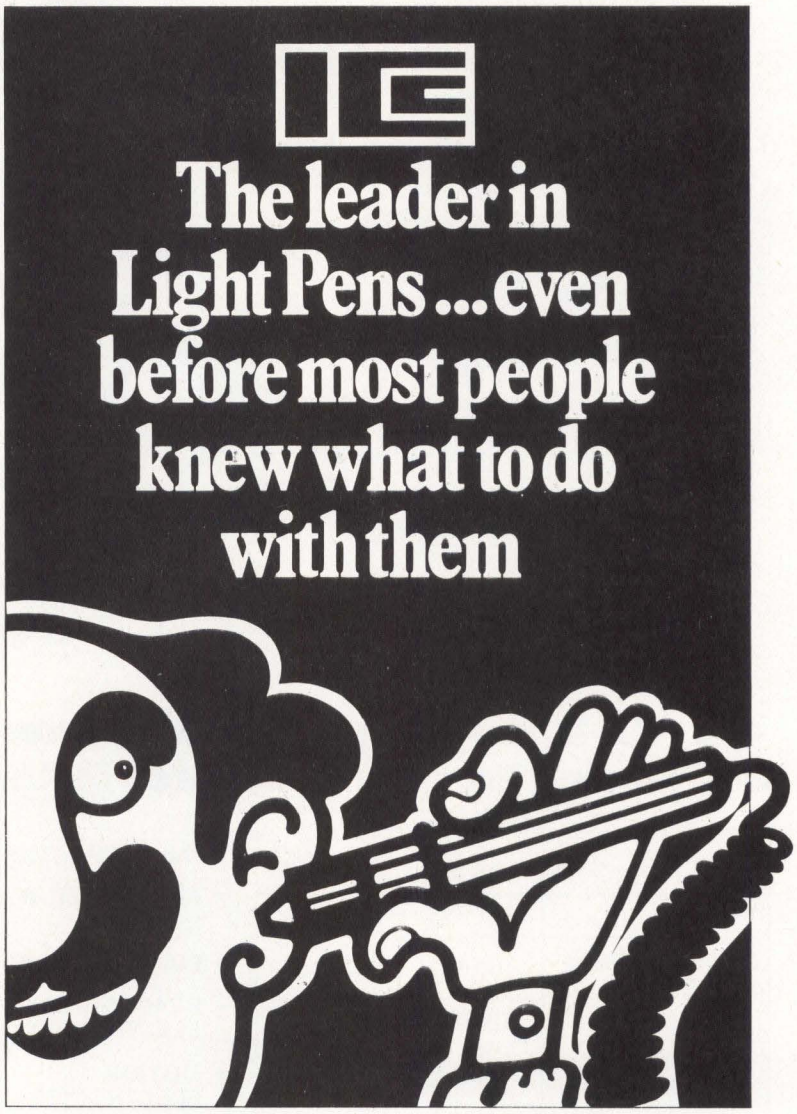
PRODUCTS

LOGIC ANALYZER AND DATA GENERATOR



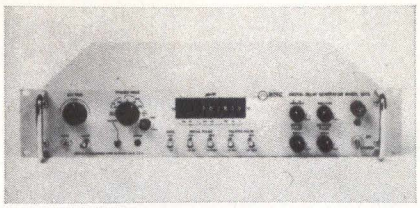
The microprocessor-controlled model 740 logic analyzer contains a compare memory that permits instant error analysis and display of input data in hex, octal, or binary digital formats or in a square wave timing format. When connected to an optional model 721 data generator, the analyzer's microprocessor, keyboard, and CRT are integrated with the generator to provide an NRZ data output and display with positive or negative logic sense. Features of the generator include crystal or variable data rates to 20 MHz. **Moxon Inc, Instrumentation Div,** 2222 Michelson Dr, Irvine, CA 92715.
Circle 220 on Inquiry Card



ICC. The leader in light pens since 1966. Now offering improved performance. Lower prices too. What are you waiting for? Write for full details or call, today.

INFORMATION CONTROL CORPORATION
9610 Bellanca Ave., Los Angeles, Ca. 90045 (213) 641-8520

DIGITAL DELAY GENERATOR

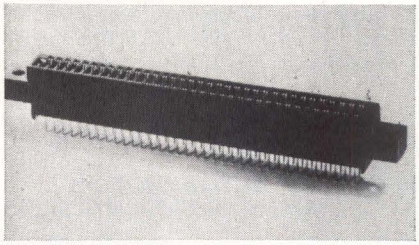


Model 7075 is a high precision unit offering variable delays and gates of up to 1 ms, selectable in 1-ns increments. An option extends max range to 1 s. Self-trigger generator has a 5-Hz to 5-MHz range. Internal clock pulse generator eliminates indeterminacy between random input trigger pulses and instrument's output pulses. Jitter is $<\pm 100$ ps. Error indicator lights when the triggering period is shorter than the delay time setting. Unit can approach ± 0.5-ns accuracy for long delays. **Berkeley Nucleonics Corp,** 1198 10th St, Berkeley, CA 94710.
Circle 221 on Inquiry Card

DATA OVER VOICE MODEMS

Solid-state integrated circuitry of modems for terrestrial microwave links and satellite FM systems guarantees reliability and low power consumption. Units interface directly with FM baseband input above the highest voice frequency. Data services can be provided from 1.2k to 10k bytes. Modem consists of an RF transmitter on which data stream is modulated using a quadraphase modulation technique. Interchangeable interface options allow use of RS-232, Bell 303, V35, or other interface arrangements. **American Modem Corp,** 160 Wilbur Pl, Bohemia, NY 11716.
Circle 222 on Inquiry Card

PC CONNECTORS FOR WAVE SOLDERING



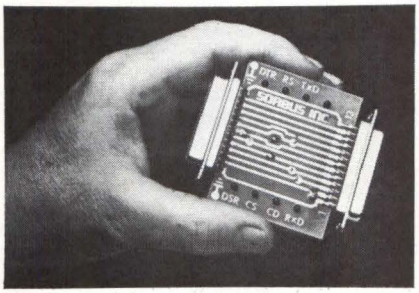
Connectors feature round tails that fit into smaller holes than square tails, and allow for more uniform solder joints. Since the 0.026″ (0.660 mm) dia round tails fit into smaller holes, more space is available between holes for printed circuitry. Contacts come on 0.100″ (2.54 mm), 0.125″ (3.175 mm), and 0.156″ (3.962 mm) centers. NK and NL series connectors are available in 2 tail lengths. **Viking Industries, Inc,** 9324 Topanga Canyon Blvd, Chatsworth, CA 91311.
Circle 223 on Inquiry Card

PORTABLE G-P SCOPE

A 15-MHz, 2-mV oscilloscope, PM3211 features comprehensive display as well as triggering facilities. It offers a full-sized 8 x 10-cm screen in a compact 300 x 135 x 445-mm package; weight is 7.5 kg. Power supply is double insulated; no grounding is needed and measurements can be made without ground loops, eliminating hum and spurious signals. Triggering can be in auto or level-set modes and multisourced, eliminating the need to change probes. 18-speed timebase has a vernier control. **Philips Test and Measuring Instruments, Inc,** 85 McKee Dr, Mahwah, NJ 07430.
Circle 224 on Inquiry Card

MODEM MONITOR

A compact, signal display device that can be placed inline between data sets and data communication terminals to provide a means of isolating failures, the pocket-sized Traffic Light uses LEDs to provide constant status display of 7 key signals on the EIA RS-232 25-pin business machine interface. Signals monitored include transmitted data, received data, request to send, clear to send, data set ready, carrier detect, and data terminal ready. A spare LED circuit can be used to show any other signal. **Sorbus Inc, an MAI co,** 150 Allendale Rd, King of Prussia, PA 19406.
Circle 225 on Inquiry Card



DIGITAL BATCH CONTROL COUNTER

Slimline preset counter totalizes input pulses and provides control signal when preset total is reached. Available with up to 6 full digits, counter operates from 120 or 240 Vac, and includes complete remote control capability. Display uses high efficiency red-orange LEDs and a nonglare faceplate. Ultrathin 0.625" (1.59-cm) case mounts flat on the front of any panel. Single circuit board construction improves resistance to shock and vibration. Operating at up to 20 kHz, unit counts up from 0 to a preset number or from a preset number down to 0. **Nationwide Electronic Systems, Inc,** 1536 Brandy Pkwy, Streamwood, IL 60103.
Circle 226 on Inquiry Card

MICROCOMPUTER CORE MEMORY BOARD

Designed to plug directly into the DEC LSI-11 microcomputer, the MM-1103/16 16k x 16 memory system provides nonvolatile storage with an access time of 400 ns. The memory, plug compatible with the DEC MMV-11A, may be installed in any location in the LSI-11 chassis. By using slot 4, the user is provided with 2 spare slots in addition to the microcomputer module slot in the same chassis. Features are byte control and onboard module selection in 4k increments up to 32k words. **Micro Memory, Inc,** 9438 Irondale Ave, Chatsworth, CA 91311.
Circle 227 on Inquiry Card

MINIATURE RELAY SOCKETS

A 10-pin flange-mounted relay socket, designated 9883-46-02, meets Signal Corps #SM-D-415156. An 8-pin flange-mounted socket, 9883-15-02 meets Signal Corps #SM-D-414117, and works with rack types, handwired systems, or first generation or breadboards. At the PC stage, the 8-pin 9883-14-11 meets Signal Corps #SM-C-374819. Contact tails are accurately controlled and can be tightly fitted to PC board holes without clamping. **EBY Co,** 4701 Germantown Ave, Philadelphia, PA 19144.
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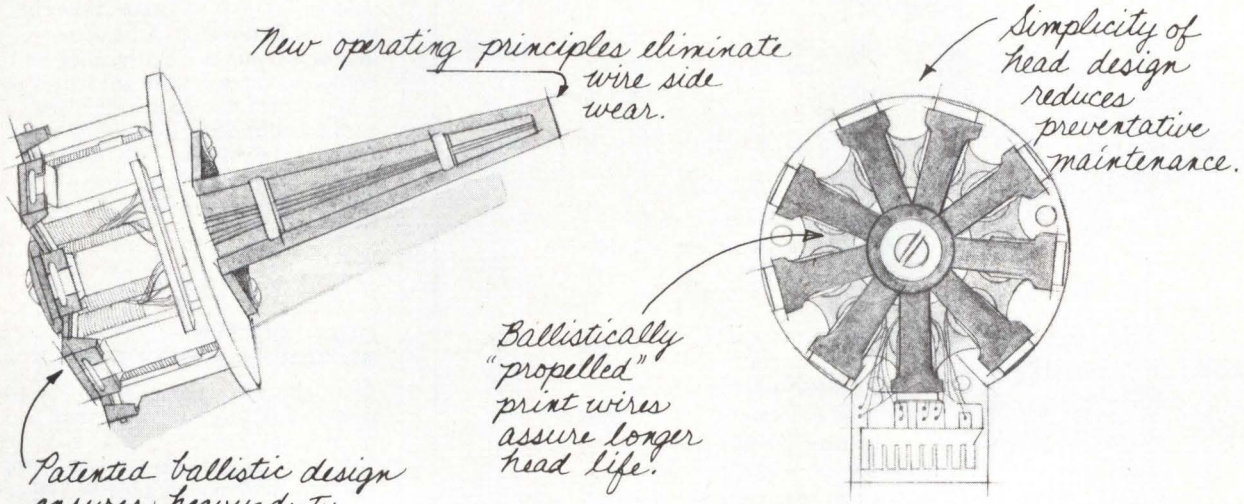
The Lear Siegler Ballistic Head™ for matrix printers.



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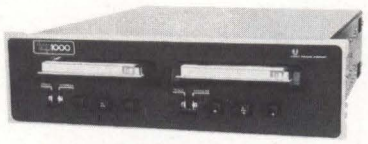

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PRODUCTS

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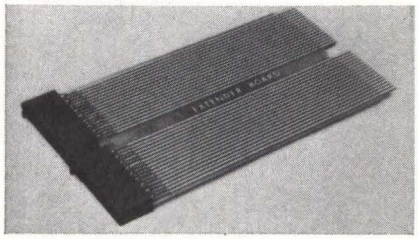


Available for use in DEC-type backplanes 1, 2, or 3 extender boards are required to fit dual, quad, and hex height backplanes, respectively. Board facilitates setup of a computer card by providing access to both of its outer sides, allowing availability of all test points as an aid to diagnostics and troubleshooting. Constructed of FR-4 epoxy fiberglass with solder mask traces and hard gold-plated card-edge contact fingers, board measures 5 x 8" (12.7 x 20.3 cm). **Southwest Systems,** Box 2808, Laguna Hills, CA 92653.
Circle 229 on Inquiry Card

DATA COMMUNICATIONS INTERFACE SWITCH

Model 1 (IS-1) eliminates the need for separate modems and ports in systems with dual terminals. Installed between modem and terminals conforming to EIA Std RS-232-C, asynchronous bit-serial data transfer, unit has 4 modes of operation activated by a 4-way switch. It allows incoming data to be sent to either or both terminals, or terminal to terminal. A computer can be interfaced with a video display unit and hardcopy printer. Unit measures 4.5 x 8 x 6.5" (11.4 x 20.3 x 16.5 cm). Self-contained power supply is optional. **Triformation Systems, Inc,** 3132 SE Jay St, Stuart, FL 33494.
Circle 230 on Inquiry Card

QUAD OUTPUT SWITCHING POWER SUPPLY

Unit offers 4 independent switching power supplies with isolated outputs of 5 V, 30 A; −5 V, 5 A; and ±15 V, 2 A. Overvoltage and current protection are provided on all outputs. MGQ-300 also withstands continuous short-circuit conditions. Temp range is −10 to 70°C with a 2.5%/°C derating from 50°C at full output. All outputs remain within voltage regulation at full load for 28 ms after removal of nom line voltage. **Gould Inc, Electronic Components Div,** 4601 N Arden Dr, El Monte, CA 91731.
Circle 231 on Inquiry Card

HYBRID 16-BIT D-A CONVERTERS

Series includes the DAC-HP16B with 16-bit binary resolution and ±0.003% linearity, and the 16D with 4-digit BCD resolution and ±0.005% linearity. Input coding is complementary binary and offset binary for the 16B and complementary BCD for the 16D. Binary version operates in both unipolar and bipolar modes with output voltages of 0 to 10 and ±5 V; BCD version operates in unipolar mode only with 0- to 10-V output. **Datel Systems, Inc,** 1020 Turnpike St, Canton, MA 02021.
Circle 232 on Inquiry Card

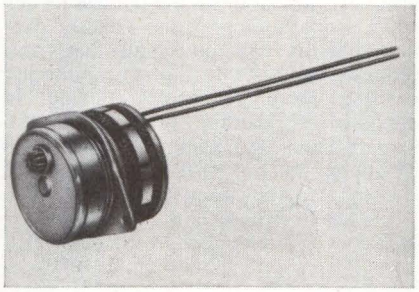
DISC REPLACEMENT MEMORY MODULE

Standalone mass memory module for OEM replacements of fixed head discs has complete timing, core array drives, and address and data registers. Max storage capacity is 131,072 words x 18 bits. Use of byte control allows operation as 262,144 words x 9 bits. Up to 16 modules can be directly paralleled without external control through an internal module address selection. Operating modes of ECOM-S are read/restore, clear/write, and read/modify/write. **Standard Memories/Trendata,** 3400 W Segerstrom Ave, Santa Ana, CA 92704.
Circle 233 on Inquiry Card

COMPACT SYNCHRONOUS MOTORS

GSI line of permanent magnet ac motors provides high torque outputs in a compact package. Operating voltages are either 115 or 230 Vac with power inputs ranging from 8 to 12 W. Rotor speeds are 250, 300, 500, or 600 r/min, and torque pullin values are 7.5, 8.0, or 9.5 oz-in (0.05, 0.056, or 0.067 N•m). Motors operate from 0 to 60°C with a temp rise of 55°C. Dielectric test is 1500 V rms. Models are reversible and gearhead compatible; they weigh 14 oz (397 g). **Portescap U.S.,** 730 5th Ave, New York, NY 10019.
Circle 234 on Inquiry Card

2-WIRE STEPPER MOTOR



Intended for control functions, the 31300 motor directly converts electrical impulses into discrete angular steps of the output shaft. Operating from simple on-off pulses, the rotor turns 180 deg when power is applied and an additional 180 deg when power is removed; no power is consumed between pulses. Rotation is unidirectional, CW or CCW, and std available step angles are 36, 30, 6, and 0.36 deg. Output torque at 0.36-deg step angle is 2.5 oz-in (0.018 N•m) at rates up to 40 pulses/s. **Haydon Switch and Instrument, Inc,** 1500 Meriden Rd, Waterbury, CT 06705.
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STATIC RAM BOARD

An 8k-byte memory for the S-100 bus, 8kRS is organized as 2 independently addressable 4k blocks with address selection by a jumper and plug system which can be changed while the board is plugged in. Onboard toggle switch provides write protection; logic also implements write protection of either or both 4k blocks via front panel controls. ICs are soldered, thus eliminating reliability problems associated with sockets. **Pacific Digital,** 2555 E Chapman Ave, Suite 604, Fullerton, CA 92631.
Circle 236 on Inquiry Card

HEAT SINK

MaxiFin heat sink, designed for 10 W and under power dissipation, provides a max degree of heat dissipation at a minimal cost. Two models, with TO-3 and TO-66 hole patterns and a 1″ (2.54-cm) fin height meet various heat reduction requirements. Sink accommodates plastic power packs and is easily mounted on PC boards. **Vemaline Products, div of Ostby and Barton,** 487 Jefferson Blvd, Warwick, RI 02886.
Circle 237 on Inquiry Card

ROYTRON™
plug-compatible reader/punch

Desktop combination reader/punch with serial asynchronous RS-232C compatible interface. Designed to operate with a terminal device on the same serial data lines or alone on a dedicated serial line. Reader will generate data at all standard baud rates up to 2400 baud.

Punch accepts data at all standard baud rates up to 600 baud continuous or 4800 baud batch, utilizing a 32 character buffer.

Two modes of operation are provided: *Auto Mode* — Simulates Model ASR 33 Teletype using ASCII defined data codes (DC 1, 2, 3 and 4) to activate/deactivate the reader or punch; *Manual Mode* — Code transparent mode. Panel switches control activation/deactivation of reader or punch and associated terminal device.

Tape duplication feature is provided by setting unit to LOCAL mode.

MODEL 1560-AS

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PRODUCTS

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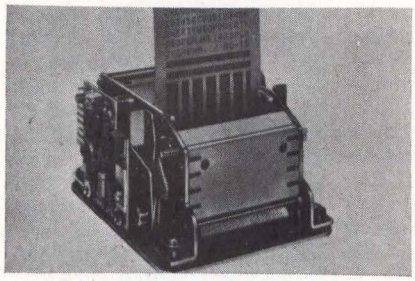

Electrosensitive printer EX-201 operates from 12 Vdc using a fixed stylus printhead. It is in light contact with a drive roller which moves paper under the head at up to 6 in (15.3 cm)/s. Alphanumeric printing speed is 800 char/s; char may be formatted horizontally or vertically on the paper to give line or message printing as desired. The printhead contains 120 tungsten styli embedded in a flexible urethane component with 0.5-mm separation and a built-in paper grounding element. Compact unit weighs 2.5 lb (1.1 kg). **Axiom Corp,** 5932 San Fernando Rd, Glendale, CA 91202.
Circle 238 on Inquiry Card

OPTICAL CHARACTER READER SYSTEM

Typereader™ system enables typewritten pages to be read and duplicated onto mag media of a word processing system for editing and printout, thereby allowing typewriters with OCR-B elements to function as input devices for word processing systems. Feature permits use of 12-pitch typewriters, and reduces the need to replace or modify existing office equipment. System is capable of reading 12-pitch, single-spaced lines, and eliminates format restrictions for the typist. **Hendrix,** 645 Harvey Rd, Manchester, NH 03103.
Circle 239 on Inquiry Card

SWITCHABLE ACOUSTIC COUPLER

The 103/202 is designed for dual 300- and 1200-baud operation for use with remote data entry and retrieval systems, enabling a terminal to be used with a single acoustic coupler at data rates of 110, 150, 300, 600, and 1200 baud. Protocol is readily accessible via an external switch. A Bell compatible 5-baud reverse channel is std; a 150-band FSK is optional. Std RS-232-C interface provides transparency with all data terminals. **Omnitech Data Corp,** 2405 S 20th St, Phoenix, AZ 85034.
Circle 240 on Inquiry Card

15-BIT A-D CONVERTER

Model ADC 1215L combines a conversion time of 5.5 μs and high accuracy of $\pm$0.004% with very high resolution—15-bit binary or 2's complement output—and linearity of $\pm$0.002%. Power consumption is 2.2 W. The self-contained unit digitizes high speed analog input signals. The company's SAH 1215 DP-5 with differential input and "ping-pong" operation functions with the ADC for 160-kHz system operation. No external reference voltage source or amps are necessary. **Phoenix Data, Inc,** 3384 W Osborn Rd, Phoenix, AZ 85017.
Circle 241 on Inquiry Card

ACOUSTIC COUPLER

Model 32 originate/answer coupler is Bell System 103/113 compatible, full or half duplex, with 300-bit/s data communication over marginal telephone connections. Linear phase active filters condition transmitted and received signals for optimum duplex operation by notching out interfering transmitter harmonics. Carrier detector circuit eliminates false carrier indication and permits reliable channel establishment over poor telephone circuits with received signal levels of $-$55 dBm or lower. EIA RS-232 and 20-mA interfaces are included. **Datec, Inc,** PO Box 839, Chapel Hill, NC 27514.
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The **Model 100A** has the major features of more costly logic state analyzers. Operates with virtually any scope and logic family; captures and displays sixteen 8-bit words before or after a pre-defined trigger word; formats data in HEX or OCTAL groupings; offers single or repeating truth tables; provides trigger output for waveform analysis.

For more advanced applications, add the mating **Model 10 Trigger Expander** to the Model 100A. This integrated package offers 24 bits, qualifiers, program paging and loop analysis capabilities. Model 10 prices: KIT-**$229.00**; ASSEMBLED-**$295.00**; Model 100A/10 mounting baseplate-**$9.95**.

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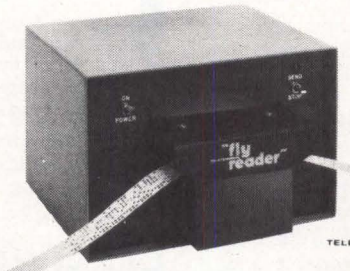

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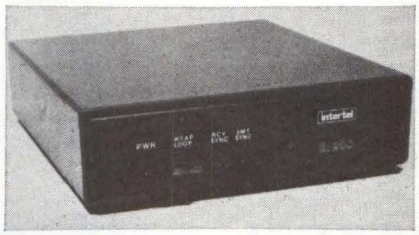
PRODUCTS

POLLABLE ASCII CHARACTER BUFFER

Model 721Z is designed for data or message buffering in centralized polling applications over switched public telephone networks. Unit consists of a microprocessor-based control section and up to 16 memory modules, all contained in a small card file. Buffer is equipped with an input port for attaching data/message source. An output port connects to a telephone line for polling by a distant location via dialup connection over the network. **Conrac Corp, Alston Div,** 1724 S Mountain Ave, Duarte, CA 91010.
Circle 243 on Inquiry Card

DIGITAL DATA SIGNAL ADAPTER



Capability of the NCS4000 network control system has been extended with the EI200 adapter to include IBM 3600 systems that contain remote loops of daisy-chained terminals. Discontinuous terminal subloops can be easily identified at the central site and, if necessary, bypassed. A direct replacement for the IBM RPQ adapter, the unit can be combined with a DA300 module to provide automatic dial backup. Compatible with the company's 1200- and 2400-bit/s modems, it performs the conversion between IBM and EIA signals. **Intertel,** 6 Vine Brook Pk, Burlington, MA 01830.
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SOLID-STATE SYNCHRO MODULES

Series of control transformer modules have std accuracies of ±6, ±15, or ±30 min of arc. Units simultaneously accept synchro or resolver inputs of 11.8 or 90 V, 400 Hz, or 90 V, 60 Hz, and 14-, 12-, or 10-bit binary digital data. Gradients are 0.4 or 1 V rms/deg; output angle range is ±7 or ±12.5 deg. Series of converters is insensitive to ±10% amplitude and frequency variations, ±5% power supply variations, and accuracy applies over the op temp range. **Computer Conversions Corp,** 6 Dunton Ct, East Northport, NY 11731.
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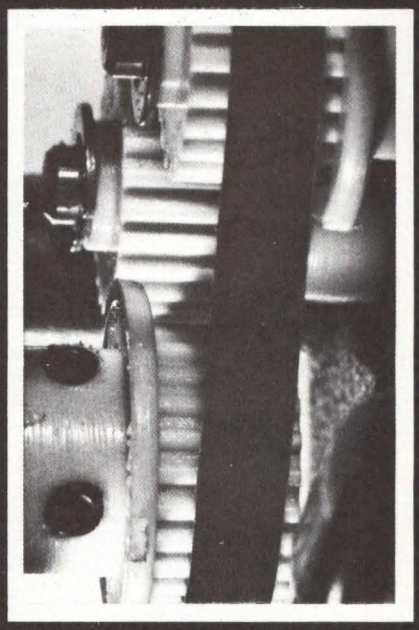

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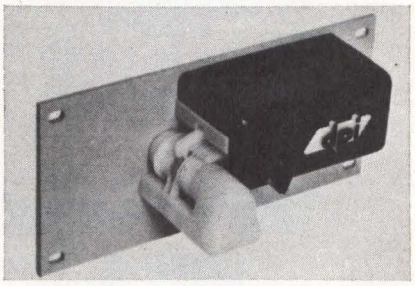
PRODUCTS

PAPER TAPE READER ASSEMBLY



Model 1200 is capable of supplying an accurate data timing translation every 15 deg of transport shaft rotation. This configuration enables inexpensive timing of data because it is built into the tape reader head and is operated by a 9th starwheel, reading an encoded transport shaft. Unit can be supplied with electromechanical unidirectional drive of 35 char/s; step motor drive (bidirectional) of 150 char/s; synchronous unidirectional motor drive of 60/72/105 char/s; or any other motor drive. **Data Peripheral, Inc,** 23 Vreeland St, Lodi, NJ 07644.
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DATA COMMUNICATIONS VIDEO MONITOR

Pacerscope, a video monitor under programmable control, provides a clear window to a data communication circuit from the RS-232 interface. The 1024-char window displays alphanumeric, hexadecimal, or binary data. The user can view data in real time up to 9600 FDX or selectively filter data to show only those portions of diagnostic interest. Offline it displays thousands of char to permit analysis of recorded data. Software control allows viewing of data between the occurrence of 2 events. **Digitech Data Industries, Inc,** 66 Grove St, Ridgefield, CT 06877.
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PRINTER/PLOTTER DATA EXPANSION BUFFER

Model P512 FIFO buffer is contained on a PC board, which plugs directly into the spare slot in the card cage of a Printronix™ unit. Interconnecting cabling is provided. Transparent to system interfaces and software, and requiring no modifications to the printer/plotter, the 512-char device has 2 clocks for data input and output. Users can increase system throughput up to 50% in plotting applications and 25% in printing. **USDATA Engineering, Inc,** 14241 Proton Rd, Dallas, TX 75240.
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MINICOMPUTER DISC CONTROLLER

Model SMC902 single-card controller for Data General minicomputers offers up to 600M bytes of online storage, occupies one CPU slot, and is compatible with cartridge module disc drives. Software support for controller includes RDOS, IRIS, and BLIS/COBOL compatible drivers, and a standalone diagnostic/formatter program. Std features include full sector buffering, DMA data transfer, automatic program loading, and overlapped seeks. **MiniComputer Technology,** 2470 Embarcadero Way, Palo Alto, CA 94303.
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AUTOMATED TEST SYSTEM

Digital testing, guided probe fault isolation, fault detection to the failed device, and optionally, the ability to perform digital logic simulation are supplied by the ATS-961. Features include a test rate of 200k tests/s, a capacity for 256 stimulus/response leads, external synchronization of a digital test pattern application, array software to allow data analysis, and ATLAS programming. A second test station can be accommodated for simultaneous testing of different board types. **Texas Instruments, Inc, Digital Systems Div,** PO Box 1444, Houston, TX 77001.
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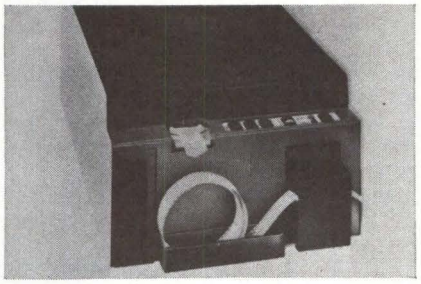
PRODUCTS

COMPACT CARD RECORDER

The HRC recorder offers input choices of analog, incremental, time, or any two combinations for X-Y or T-Y^R applications. Measuring 6.875 x 5.5 x 14″ (17.5 x 14 x 36 cm), the unit uses std computer punch cards allowing a record size of 2.5 x 5.5″ (6.4 x 14 cm). Recording area is visible through clear sliding cover. Preprinted cards can be used for subsequent data processing. Permanent pen trace can be continuous, intermittent, or dotted under control of the std electric pen lift. **Houston Instrument,** 1 Houston Sq, Austin, TX 78753.
Circle 251 on Inquiry Card

PAPER TAPE READER/PUNCH



Combination unit with parallel or serial (RS-232) interface features a punch that operates at speeds up to 75 char/s and a reader that transmits up to 300 char/s. Moduperf punch mechanism of SRP-3075 is guaranteed to perforate min of 1M ft (305 km) of paper tape. The 12″ (30-cm) unit interchangeably punches Mylar, Mylar laminates, oiled, unoiled, rolled, and folded tapes without readjustment or modification. Features are easy tape loading, chad removal, and access to controls. **Data Specialties, Inc,** 3455 Commercial, Northbrook, IL 60062.
Circle 252 on Inquiry Card

MEGABYTE MEMORY MODULE

Large capacity memory card configured as 1088k x 8 possesses an additional 64k capacity allowing for implementation of various error checking methods while maintaining a 1M-byte capacity for data. Memory is a complete random access 2-wire, 2½ D core memory, packaged on a pluggable PC card. System chassis accommodates up to 4M-byte modules, 2 I/O cards, and a power supply within 17.5″ (44.5 cm) of vertical rack space. **Electronic Memories & Magnetics/Commercial Memory Products,** 12621 Chadron Ave, Hawthorne, CA 90250.
Circle 253 on Inquiry Card

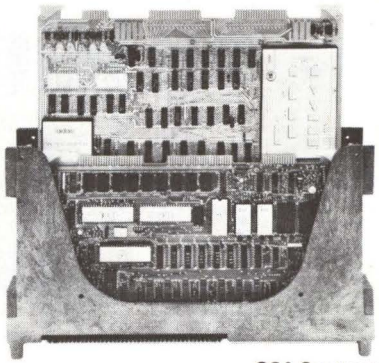
Intel compatible data acquisition system for only $495*

The low-cost ADAC Model 735 series of data acquisition systems is mounted on a single PC board that plugs into the same card cage as the Intel SBC-80/10, and SBC-80/20 single board computers and also the Intel MDS-800 microcomputer development system. The Model 735 bus interface includes a software choice of program control or program interrupt and a jumper choice of memory mapped I/O or isolated I/O.

The basic 735 OEM system which is contained on a single PC board (12″ x 6.72″ x 0.4″) consists of 16 single-ended or 8 differential analog input channels, either voltage or current inputs (4-20 mA or 5-50 mA), 12 bit high speed A/D converter, sample and hold and bus interface. The throughput rate of the Model 735 is 35 KHz. Optionally available is the capability of expanding on the same card to a total of 64 single ended or 32 differential voltage/current inputs. up to two 12 bit D/A converters, software programmable gain amplifier with auto zero circuit, scope control and third wire sensing.

ADAC Corporation, 15 Cummings Park, Woburn, MA 01801.
(617) 935-6668

***Price in quantities of 1 to 4.**



GSA Contract Group 66

adac corporation

PRODUCTS

LINE PRINTER

The LP 3036 provides high speed 300-line/min printout in 36-, 42-, or 60-col format or char-at-a-time operation. Simplified unit features 6 actuators that apply pressure to paper against scanner to print characters in a 9 x 7 matrix pattern; each actuator scans multiple columns and travels 0.002" (0.005 cm). Print mechanism is controlled by a microprocessor. Printer weighs 12 lb (5.4 kg), and measures 4.78 x 7 x 7" (12.14 x 17.8 x 17.8 cm). **Miltope Corp,** 9 Fairchild Ave, Plainview, NY 11803.
Circle 254 on Inquiry Card

DISPLAY TERMINAL CATHODE RAY TUBES

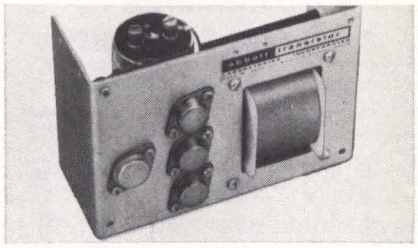
Two 12" (30.5-cm) CRTs, designed for alphanumeric and graphic data display applications in computer terminals, offer sharp corner focus and high resolution characteristics. T31-59P4 is a 100-deg deflection CRT with 1500-line resolution; T31-62P4 is a 90-deg deflection CRT with 1200-line resolution. Features are rectangular direct view display design and banded integral implosion protection with mounting lugs. Tubes are available in most std phosphors. **Panasonic Electronic Components Div,** 1 Panasonic Way, Secaucus, NJ 07094.
Circle 255 on Inquiry Card

SWITCHING POWER SUPPLY CAPACITORS

Type 139R thermal pack aluminum electrolytic capacitor features ESR values from 0.0030 Ω at 20 kHz at ±30% tolerance; capacitance tolerance at ±20%; up to 20-A ripple current at 85°C and 20 kHz; and op temp range from −55 to 85°C. Other output capacitors are the 100, 101, 300, and 500 series, and 557 and 057 premium-grade models, offering op temp ranges from 105 to 125°C. Input types are the DCM and 500 thermal pack models and computer-grade type 066 with op temp range to 85°C; and 2 premium-grade capacitors, types 057 and 557 with ranges to 105 and 125°C, respectively. **Sangamo Capacitors Div,** PO Box 128, Pickens, SC 29671.
Circle 256 on Inquiry Card

OPEN FRAME HI-REL POWER SUPPLY MODULES

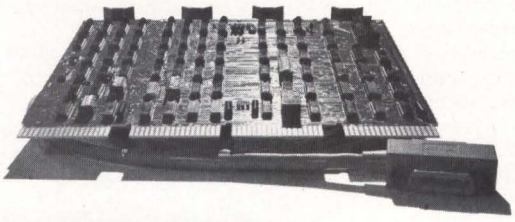
Delivering full power at amb temp of 0 to 50°C, derated to 40% at 71°C, the NL series offers typ efficiency of 45 to 60%. Std input is 105 to 125 V rms, with 210 to 250 V rms also available. Input frequency is 47 to 440 Hz. Single output versions feature 0.02% line and 0.1% load regulation; dual/triple output modules offer 0.1 and 0.2%, respectively. Typ pk-pk voltage is 1.5 mV. Also provided are remote error sensing and protection against over/reverse voltages and short circuits. **Abbott Transistor Labs, Inc,** 5200 W Jefferson Blvd, Los Angeles, CA 90016.



Circle 257 on Inquiry Card

PDP-11 interface

for IEEE 488-1975 standard devices



GPIB11-1

Now, PDP-11 users can configure complete computer control measurement systems, at low cost, and with commercially available instruments.

National Instruments offers a complete package that allows PDP-11 users the versatility of using the growing number of instruments that comply with the IEEE 488-1975 standard bus. The National Instruments package includes the GPIB11-1 plug-in board, complete software package in FORTRAN, BASIC or MACRO, cable and connectors. And the GPIB11-1 is so low priced that it makes conversion truly low cost, in addition to being easy.

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When Honeywell saw our MICRO-68 Microprocessors, they bought them.

So should you.

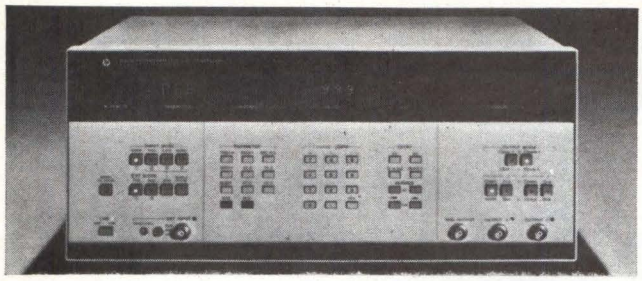
Honeywell is currently using the MICRO-68 as both a training device for employees, and at the same time, for extensive industrial prototyping. The reasons companies like Honeywell, as well as colleges and universities, are using the MICRO-68 microprocessor are as simple as the units themselves. The MICRO-68 comes complete and ready to run, has a self-contained power supply, hexidecimal keyboard, six-digit LED display, 512 word PROM resident monitor, and many other features and peripherals. And it is easily affordable.

Electronic Product Associates, Inc.
1157 Vega St., San Diego, CA 92110, (714) 276-8911
First In Microprocessor Systems

CIRCLE 107 ON INQUIRY CARD

CIRCLE 108 ON INQUIRY CARD

PROGRAMMABLE PULSE GENERATOR



Programmable timing accuracies of 2% of programmed value with a repeatability of 0.5% are available in model 8160A. All pulse parameters are programmable. Pulses are generated from 1 Hz to 50 MHz. Transition time of ±1% is specified for programmed repeatability. Basic pulse generator is single channel with a dual channel option, and can store and recall up to 9 complete instrument settings. Operating mode settings, pulse parameters, and output settings are recalled by simply pressing 2 buttons, or by addressing 1 of 9 storage registers via the interface bus. Pulse period is settable from 10.0 ns to 999 ms with 3-digit resolution. Internal and external trigger modes as well as external gate and counted burst are provided. **Hewlett-Packard Co,** 1501 Page Mill Rd, Palo Alto, CA 94304.

Circle 258 on Inquiry Card

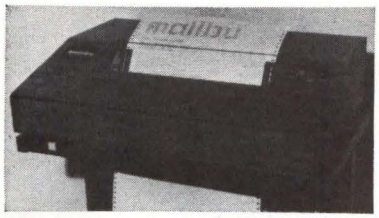
LSI-BASED INDUSTRIAL CONTROL SYSTEM

IP300, designed to supply programmable process I/O to localized applications, combines the 16-bit LSI-11 microcomputer with analog and digital I/O in a single box, and handles up to 78 I/O modules. Unit has 56k bytes of MOS memory, dual flexible disc unit, DECwriter II console terminal, RSX-11S real-time operating system, and space for up to eight I/O modules. Task scheduling is primarily event-driven, allowing the user to assign a software priority for each active task. Because RSX-11S is memory-based, program development and system generation are carried out on a separate processor running RSX-11M and transported using flexible disc. Programming is supported in macro assembly language, FORTRAN IV, FORTRAN IV-Plus, and ISA std process I/O subroutines. **Digital Equipment Corp,** Maynard, MA 01754.

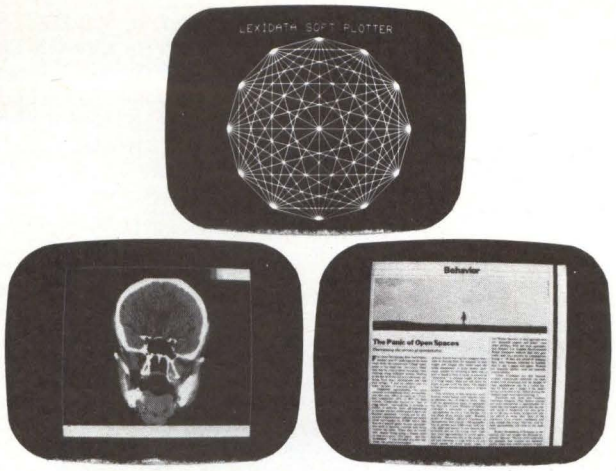
Circle 259 on Inquiry Card

DOT MATRIX LINE PRINTER

Model 160 is a commercial grade dot matrix machine which operates bidirectionally at 165-char/s and has graphics capabilities since each of the 9 printhead wires is under software control. Features include logic seeking capabilities for fast throughput, reinking rollers for ribbon life up to 50M char, jumper-selectable primary voltage (110-220 V, 50-60 Hz), Hydra Ballistic™ printhead for long life. Std software supports the 96-char ASCII set, but the user may change char easily. Tractor-operated paper feed allows dots to be placed immediately adjacent either horizontally or vertically, giving graphics capability at 3000 dot locations/in². Unit accepts paper from 4 to 15" (10 to 38 cm) wide and prints up to 132 char/line. **Malibu Design Group, Inc,** 2110G Nordhoff St, Chatsworth, CA 91311.



Circle 260 on Inquiry Card



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System-sophistication made practical for the OEM and end-user

- Full refresh, flicker-free, raster scan display
  - -up to 1280 x 1024 pixels in 16-levels of grayscale
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- High-speed, variable image processing
  - -pixel update as fast as 45 nsec per pixel
  - -random and sequential update
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- User can program the alphanumeric generator and define the cursor
- Nondestructive functions to highlight image displayed
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A versatile graphics-system to meet your widely diverse needs that you'll want to know more about. Just write Lexidata Corporation, 215 Middlesex Turnpike, Burlington, MA 01803 or faster yet, call us at 617 273-2700, and ask for Martin Duhms.

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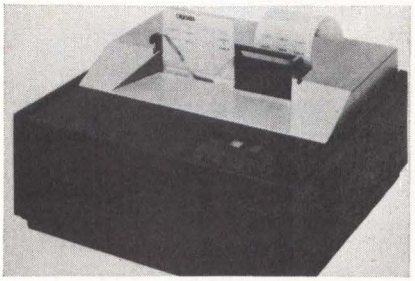
CIRCLE 109 ON INQUIRY CARD

PRODUCTS

DOCUMENT/PASSBOOK PRINTER



Designated CP210, model III, the printer accepts various documents, passbooks, and multipart forms from 2.5 to 8.5" (6.4 to 21.6 cm) wide and 2.5 to 30" (6.4 to 76 cm) long, without operator intervention or machine adjustment. It prints 60 lines/min. A microprocessor-controlled interface is incorporated to allow a document to be positioned up or down in increments of <1 line, assuring accurate positioning of the printed line. It can be configured for single or shared operation. **Okidata Corp,** 111 Gaither Dr, Mt Laurel, NJ 08054.
Circle 261 on Inquiry Card

MODEM ASSEMBLY

The 330-2R-0 houses 2 of the company's series 330 modems and provides display of 4 control and 2 data functions. Assembly may be used to house 2 300-baud modems, 1 300- and 1 1200-baud modem, 2 1200-baud modems, or 1 1200-baud modem with reverse channel. Compatible with the 330 rackmount series, the assembly can be used at the terminal end to permit max interchangeability of modems at both ends of the communications link. **ComData Corp,** 8115 N Monticello Ave, Skokie, IL 60076.
Circle 262 on Inquiry Card

PRINTING COUNTER

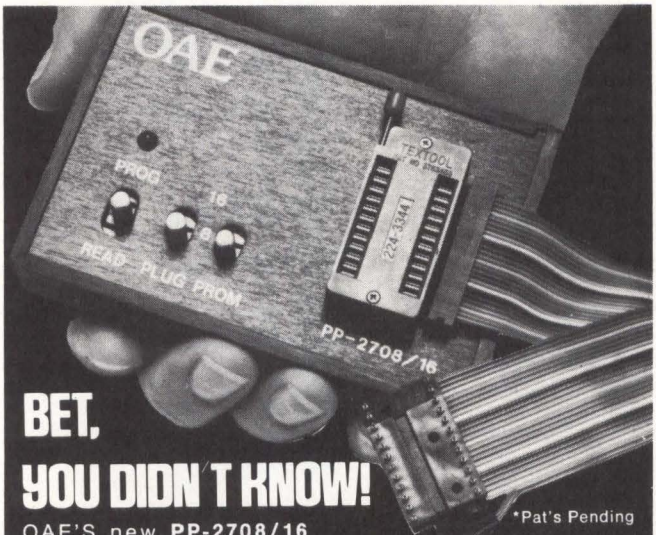
Capable of recording flow of natural gas or other liquids along with optional time and date data, unit consists of a 6-digit totalizing-counter that operates at speeds up to 600 impulses/min, and prints decades for alphanumeric capability. Life rating is 50M impulses, 1M printing cycles, and 0.5M reset operations. Electric reset permits full remote operations. Printer/counter prints on paper tape, cards, or both at speeds up to 1 line/s. Optional time and date register is available. **Sodeco Group, Landis & Gyr NA, Inc,** 4 Westchester Plaza, Elmsford, NY 10523.
Circle 263 on Inquiry Card

HYBRID D-A CONVERTERS

With settling times as low as 25 ns to 0.1%, the HDS-0820 and -1025 have resolutions of 8 and 10 bits, respectively, and are packaged in 24-pin DIPs. Active laser trimming has been used to produce high accuracy and adjustment-free performance. Microcircuit DACs have full 10-mA output current to drive transmission lines or other low impedance loads directly. Series is optionally available with MIL-STD-883 Level B processing for ultrahigh reliability. **Computer Labs, Inc,** 505 Edwardia Dr, Greensboro, NC 27409.
Circle 264 on Inquiry Card

HIGH DENSITY DIGITAL HEAD

A line of high performance digital heads for applications with 0.25" (6.35-mm) compatible ANSI/ECMA/ISO digital cartridges have max recording density of 3200 frpi. Available for read only, write only, read/write, and read-after-write applications are 1-, 2-, and 4-track models. Modified units can be designed to meet customer specs. All models feature choice of pin or lead connections. Head mount provides track location in azimuth and zenith, and ETL variable. **Brush Magnetic Heads, div of Forgflo Corp,** Third and Reagan Sts, Sunbury, PA 17801.
Circle 265 on Inquiry Card



BET, YOU DIDN'T KNOW!

*Pat's Pending

OAE'S new **PP-2708/16** PROM Programmer is the *only* programmer with all these features:

- Converts a PROM memory socket to a table top programmer: No complex interfacing to wire—just plug it into a 2708 memory socket*
- A short subroutine sends data over the address lines to program the PROM
- Programs 2 PROMS for less than the cost of a personality module. (2708s and TMS 2716s)
- Connect 2 or more in parallel — super for production programming
- Complete with DC to DC switching invertor and 10 turn cermet trimmers (for precision pulse width and amplitude alignment)
- All packaged in a handsome aluminum case

PP-2708/16 . . A & T $295.
KIT $245.
PP-2716 (Programs Intel's 2716) . . . . . A & T $295.
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CIRCLE 110 ON INQUIRY CARD

Hewlett-Packard 9825/31 Users...

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CIRCLE 111 ON INQUIRY CARD

PROCESSOR TERMINAL

MCS-PT112/32 is a self-contained computer system with display, disc storage, full keyboard, and 12-slot motherboard for use either as a standalone processor or as a processor terminal in a larger system. Features include a 15" (38-cm) high resolution monitor with full upper and lower case ASCII keyboard that has 8 user-designated special function keys, and 16-key numeric cluster pad. One Shugart SA-400 minifloppy disc drive is std. The 12-slot mainframe contains a CPU board with 8080 processor and a special circuit that implements a startup "jump to" routine to any user-selected byte address. 32k static RAM is provided; additional RAM is optional. A disc controller handles 3 minidrives. **TEI, Inc,** 5636 Etheridge St, Houston, TX 77017.

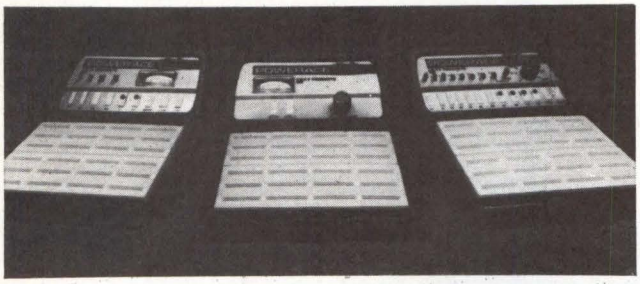
Circle 266 on Inquiry Card

16-SEGMENT ALPHANUMERIC LED DISPLAY

HA 4041 presents the entire alphabet, digits from 0 to 9, plus, minus, equal, and summation signs, and other symbols. The 16-segment LED display offers an alphanumeric set comprising 64 characters, each 4-mm high. Four such displays are combined on one module with associated electronics. Modules can be arranged in rows of practically unlimited length. Each contains a decoder for the 64-char ASCII set, multiplexer, memory, and LED driver stages. Externally, the circuits behave like a RAM; operating voltage of 5 V permits easy interfacing with standard logic levels. Display units put out 0.1 mcd/segment with a viewing angle of 20 deg from all sides. Up to 16 displays (four modules each 25 mm wide) can be lined up. **Siemens AG,** Postfach 103, D-8000 Munchen 1, Federal Republic of Germany.

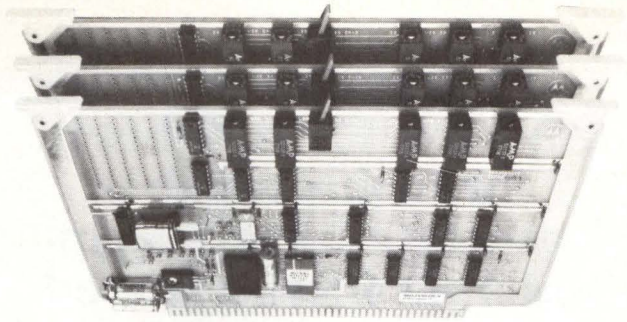
Circle 267 on Inquiry Card

POWER BREADBOARD CIRCUIT EVALUATORS

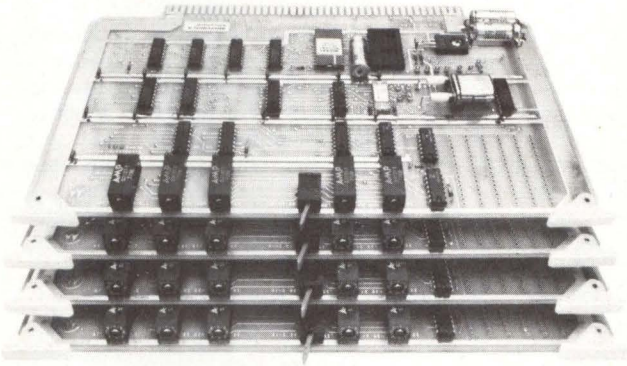


Powerace models 101, 102, and 103 feature industry accepted Super-Strip SS-2s and accept all DIP sizes, TO-5s, and discretes with leads to 0.032" (0.08 cm) dia. All offer 256 5-tiepoint terminals and 16 25-tiepoint buses, fused power supply, and ground plane. 101, 102, and 103 have power supplies and line and load regulations of 5 to 15 Vdc, 600 mA, and <3% at 120 Vac ±8%; 5 Vdc, 1 A, and <1%; and 5 Vdc, 750 mA, 15 Vdc, 250 mA, and −15 Vdc, 250 mA, and <1%, respectively. 101 features a 0- to 15-V meter, and a voltage adjust knob; the 102 has 4 slide switches with logic 0 or 1 output, and 2 momentary slide switches; and 103 provides a 15-0-15-Vdc meter, 2 LEDs, 2 slide switches, and 2 momentary slide switches. **A P Products,** 72 Corwin Dr, Box 110, Painesville, OH 44077.

Circle 268 on Inquiry Card



OEM Development Tools for Data Security



Info-guard™ modules, available now.

Flexible plug-in cards that make it easy to add encryption to your data processing and data communication systems. Boards compatible with the Motorola 6800 and Intel 8080 microprocessor systems are designed to give you multiple options in developing prototype systems. And they're available off-the-shelf. So you can quickly learn how easy it is to add encryption. And when you have determined the design that best suits your individual requirements **inexpensive custom hardware** can then be produced to meet those specific requirements.

Call your nearest Motorola Semiconductor Products Sales Office or an authorized distributor for standard hardware prices and delivery time. For custom hardware development, contact James Booth at 602/949-4735 or write to him at Motorola's Government Electronics Division, Dept. F-5, P.O. Box 2606, Scottsdale, AZ 85252.

MOTOROLA

OUR FIFTIETH YEAR

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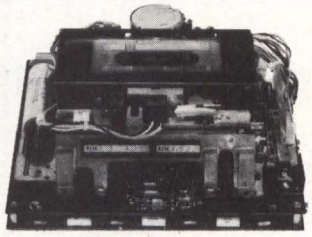
Choose an INSTANT-PERIPHERAL™ for highly reliable cassette recording in microprocessor-based systems.

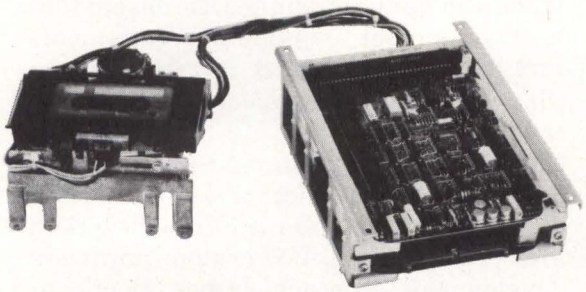
Now there's a ready-made solution for your low-cost digital storage needs. And EPI's Speed Tolerant Recording (STR®) technique provides error rates of less than 1 bit in 100 million for high data reliability.

The STR-150 and 300 interface easily with your microprocessor-based systems. Use them for automatic bootstrap, backup memory and field retrofit resident loaders—wherever you need fast, reliable program loading to restore lost programs, change programs or run diagnostic routines. The STR-300 is also ideal for data storage applications such as intelligent terminals, allowing you to store transaction data and remotely access for off-line data processing.

Look into an INSTANT-PERIPHERAL™ for your program loading and data storage needs. Contact Electronic Processors, Inc., 1265 W. Dartmouth Avenue, Englewood, Colorado 80110. Phone (303) 761-8540.



STR-150 provides full remote signal or character control of all transport functions. It includes read-write electronics, control and logic, and motor-control logic. Just supply a mounting location, power supply and interface with the controlling I/O device. $374 in 100's.



STR-300 is microprocessor based for added flexibility. Like the STR-150, it is fully remote controlled and easily interfaced, but includes a buffer memory for incremental or character-by-character recording and play-back. $685 in 100's.

ELECTRONIC PROCESSORS INCORPORATED

The INSTANT-PERIPHERAL™ Company

PRODUCTS

DATA COUPLER

Interfacing directly to the communications port of computer, CRT terminal, cassette, or other recording device, data coupler generates asynchronous bit-serial ASCII code characters for time/date information. The device is included within the series 70,000 digital clock housing. Bit-serial output can be provided at TTL voltage levels or as an EIA-RS-232-C voltage or 20-mA current interface. Numbers can be programmed manually into the output message from optional front panel thumbswitches. In addition, fixed (preprogrammed) characters, stored in an internal p/ROM, can be included as part of the message. Output message can include up to 31 ASCII-coded characters, 16 from variable sources, the remainder from p/ROM. **Chrono-Log Corp,** 2 West Park Rd, Havertown, PA 19083.

Circle 269 on Inquiry Card

TELEPRINTER SPEEDUP ADAPTER MODULE

Accelewriter™ adapts any LA36 DECwriter to 600-baud operation, converting the std 110/150/300-baud DECwriter to 110/300/600 baud. Adapter changes internal timing of the teleprinter and causes it to print at 60 char/s. Installation typically takes less than 1 h and requires the removal of 2 ICs which are replaced with low profile IC sockets. The module is installed in these sockets. Reconversion to the original electronic configuration requires only unplugging the adapter and installing ICs of the original types in the sockets. The adapter causes no permanent modifications to the teleprinter and does not interfere with installation of the std DEC™ option boards. **Larks Electronics and Data,** PO Box 22, Skokie, IL 60077.

Circle 270 on Inquiry Card

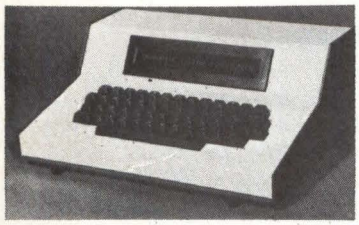
TELEPRINTER

TermiNet™ 1232, a 132-col teleprinter, is designed for use at rates to 1200 baud and includes a 1k buffer. Unit uses a rotating belt principle; fully formed characters and individually replaceable print fingers provide excellent legibility. Rotating print belt utilizes a 510-char/s hammerbank mechanism which has a hammer for each print position. All 128 ASCII characters may be generated from the std ANSI 4-row keyboard. An easily replaceable Mobius loop ribbon cartridge contains 65 yd (19.8 m) of 0.75" (1.9-cm) ribbon. Available in KSR, RO, ASR (paper tape), or magnetic send-receive (magnetic tape) configurations, unit allows front or rear paper handling; 6 pin-tractors handle 1- to 6-part forms. **General Electric Co, Data Communication Products Dept,** Waynesboro, VA 22980.

Circle 271 on Inquiry Card

ALPHANUMERIC DATA TERMINAL

Transactor III uses a microprocessor to provide features that include synchronous or asynchronous communications line support for dedicated or polled multidrop environments. Terminal has a single line 32-char gas discharge display and a 53-key TTY-style keyboard. It can be directly attached to any computer with an RS-232 or 20-mA current loop interface or to a communications line through a modem. Switches allow selection of operating mode, including 110- to 9600-baud transmission speeds, full- or half-duplex, even/odd/no parity, and station address. Std unit supports ASCII-coded data with EBCDIC as an option. An expanded 256-byte data buffer option allows up to 8 lines of data to be accessed offline. **Computerwise, Inc,** 4006 E 137th Terr, Grandview, MO 64030.



Circle 272 on Inquiry Card

PROGRAMMABLE TERMINAL CONTROLLER

A microprocessor-based controller, the 8B1 is capable of handling terminal speeds of 10, 30, or 120 char/s on private wire systems with an 8B1 protocol and offers an array of terminal diagnostics. A modified version of the Smarts controller, the unit uses only its communications processor with 4k of memory to control terminal polling and selection by a computer in both full- and half-duplex operations. The controller can be programmed to handle modified 8B1 as well as other protocols. Every terminal station includes a panel which provides controls for normal status and alarm indicator lamps, provides a hardware address for both selection and polling, and will respond to a roll call after receiving a message to indicate correct receipt. **Western Union Data Services,** 70 McKee Dr, Mahwah, NJ 07430.

Circle 273 on Inquiry Card

CRT TERMINAL/PRINTER PERIPHERAL PACKAGE

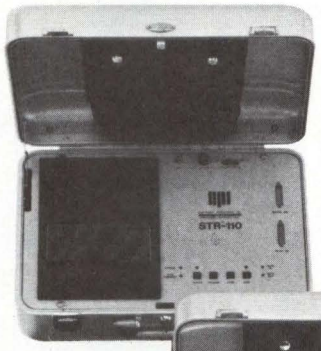
Combining the company's ADM-3A Dumb Terminal™, model 210 Ballistic™ printer, and interconnecting cable, Dumb Connection™ peripheral package provides flexibility to have both video display terminal and 180-char/s RO serial printer for about the same price as a comparable speed KSR printer. Terminal features 59 data entry keys, a 24-line, 12″ (30.4 cm) screen, and 1920-char display. 33 positive action switches allow user to activate a choice of 11 baud rates (75 to 19.2k bits/s), RS-232-C interface, or 20-mA current loop. Bidirectional printer outputs 132-char lines at 75/min. Its matrix printhead uses a lead screw drive system coupled to a dc servo motor for left and right movement. **Lear Siegler, Inc/EID, Data Products,** 714 N Brookhurst St, Anaheim, CA 92803.

Circle 274 on Inquiry Card

Plug into an INSTANT-PERIPHERAL™ for highly reliable cassette program loading and storage.

EPI's Speed Tolerant Recording (STR®) technique gives you error rates of less than 1 bit in 100 million. That's reliable! Good enough for recording, storing and loading critical programmable controller instructions or digital system diagnostic routines. Unlike many loaders using low-cost cassettes, these systems offer guaranteed unit-to-unit compatibility. That's backed by experience with more than 4000 units in the field.

Fast, reliable program loading... convenient program and data storage... easy interface to your system. Good reasons to rely on an INSTANT-PERIPHERAL™ for all your low-cost digital recording and programming tasks. Contact Electronic Processors, Inc., 1265 W. Dartmouth Ave., Englewood, Colorado 80110. Phone (303) 761-8540.



8-bit parallel STR-110 allows memory dumps or program loading up to 125 characters per second. $1210 in single quantity.

Microprocessor controlled STR-LINK II provides manual or remote control of Standard RS-232 functions via handshake lines or with control characters in serial data stream. Buffer option allows 9600 peak BAUD rate. Starts at $1650 in single quantity.

Custom designs, like this STR-110T for the Texas Instruments 5TI Programmable Control System, can handle special loader needs. We can provide automatic verification in both read and write modes, remote control and more. Just ask us.

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The INSTANT-PERIPHERAL™ Company

CIRCLE 114 ON INQUIRY CARD

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SYSTEMS INCORPORATED

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Phone: (408) 988-2550/TWX: 910-338-0130

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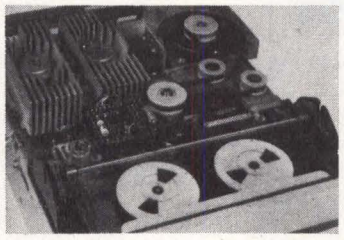
PRODUCTS

CARTRIDGE TAPE TRANSPORT

Model 650, a rugged, compact transport for use with 3M DC300A data cartridges, makes a memory module capable of storing up to 23M bits of unformatted digital data. It provides precise 30-in/s (76-cm/s) tape speed which, at ANSI compatible 1600-bit/in (630-bit/cm) PE recording density, yields a 48k-bit/s data transfer rate. Electromechanical module requires only 3.0125 x 7″ (7.9 x 17.8 cm) of front panel space. Cartridge is activated by plugging directly into transport via slot in the front panel bezel. Design uses patented belt drive to uncouple motor mass from capstan, thus preventing tape cartridge damage. An optical tachometer provides precise tape control. Unit accesses any location in 23M-bit memory within about 20 s. **North Atlantic Industries, Inc, Qantex Div,** 200 Terminal Dr, Plainview, NY 11803.



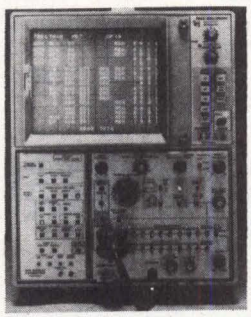
Circle 275 on Inquiry Card

S-BCD CONVERTER MODULES

Miniature, high performance, single module tracking converters accept 3-wire synchro or 4-wire resolver input data over a frequency range of 50 to 1200 Hz, and provide accurate, real-time conversion of angular displacement data to BCD format where direct, 3- or 4-digit display is required. The 4-decade output 168C650 provides angular displacement data from 0 to 359.9 or ±179 deg with an operating accuracy of ±6 min ±0.9 LSB, while the 3-decade 168C750 outputs 0 to 359 or ±179 deg accurate to ±30 min ±0.5 LSB. All accuracies are guaranteed over 5 Vdc ±5% at 500 mA and 11.5 to 17 Vdc at 60 mA power supply ranges, and 0 to 70°C std and −55 to 105°C optional op temp ranges. Units accept inputs at either 11.8 or 90 V rms. **Control Sciences, Inc,** 8399 Topanga Canyon Blvd, Canoga Park, CA 91304.

Circle 276 on Inquiry Card

LOGIC ANALYZER DISPLAY FORMATTER



Monitoring activity on the IEEE-488 bus in sequence, DF2 allows users of programmable instrumentation to link different types of instruments to a digital controller for display and analysis. Formatter displays bus control and device-dependent messages in IEEE-488 mnemonics. Information is acquired synchronously using the data valid line as a clock. Up to 256 instructions are stored in the 7D01 logic analyzer, then disassembled and displayed in mnemonic format 18 instructions at a time. States of ATN, EOI, SRQ, and REN management lines and 8 data lines are displayed in hex or decimal form. Four additional lines of data are user-definable and are displayed in binary. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.

Circle 277 on Inquiry Card

LITERATURE

Coaxial Cable Connectors

Dimensional diagrams, charts, and electrical, physical, and environmental performance characteristics of coaxial cable connectors are included in 16-page catalog. **TRW Cinch Connectors, an Electronic Components Div of TRW Inc,** Elk Grove Village, Ill.
Circle 300 on Inquiry Card

Miniature Precision Motors

Catalog provides torque curves, dimension and weight data, typ drive circuits, and temperature information on Big Inch® stepper, servo-, and integrating motors. **Haydon Switch & Instrument, Inc,** Waterbury, Conn.
Circle 301 on Inquiry Card

TTL Devices

Containing logic block diagrams and tables of basic specs and parameters for 80 TTL devices, catalog also provides cross-reference chart to major manufacturer numbers. **NEC America, Inc, Electron Devices Div,** Santa Clara, Calif.
Circle 302 on Inquiry Card

Monolithic Converters

"Analog Dialogue" includes application and design notes, descriptions, and diagrams and graphs for monolithic and A-D converters, digital thermometer, analog I/O board, and analog signal-handling. **Analog Devices, Inc,** Norwood, Mass.
Circle 303 on Inquiry Card

Optoelectronics

Illustrated manual covers application problems as well as photometry/radiometry, contrast enhancement in visible displays, and reliability of optoelectronic components. Cost is $19.25. **Hewlett Packard Co,** 1501 Page Mill Rd, Palo Alto, CA 94304.

Technical Reporting

Technical Report Standards, a handbook covering preparation, writing, and presentation of technical information, sets forth standards for accepted formats, correct data presentation, and use of graphs, tables, and illustrations. Price is $3.95 (softcover). **Banner Books International,** Banner Bldg, 7435 University Ave, La Mesa, CA 92041.

Magnetic Media

Containing compatibility charts for flexible discs, digital cassettes, magnetic cards, and disc products, pocket-size guide gives media users a product cross-reference. **Wabash Tape Corp,** Des Plaines, Ill.
Circle 304 on Inquiry Card

Planar/Modular Memories

Data sheets for DEC PDP-11 users depict design features, specs, and addressing and operating data for planar and modular memories. **Monolithic Systems Corp,** Englewood, Colo.
Circle 305 on Inquiry Card

Digital Tester

Folder includes data sheet providing specs, technique briefs explaining functions, and application notes describing the 851 tester's use in troubleshooting. **Tektronix, Inc,** Beaverton, Ore.
Circle 306 on Inquiry Card

DC Power Supply Designs

Instructions, graphs, charts, tables, and application notes are contained in booklet geared toward designers desiring to create custom systems from submodules and accessories. **Powertec, Inc,** Chatsworth, Calif.
Circle 307 on Inquiry Card

Converter Testing

Discussing A-D and D-A converter specs, application note defines and illustrates examples of testing techniques with the 2230 automatic test system. **GenRad, Inc,** Concord, Mass.
Circle 308 on Inquiry Card

Pocket Calculator

Slide-rule energy calculator computes dollar savings/yr and payback period in months, realized when using drip-proof and fan-cooled motors. **Gould Inc, Electric Motor Div,** St Louis, Mo.
Circle 309 on Inquiry Card

Modems

Comparison of features between two 4800-bit/s modems is offered in booklet illustrated with numerous photos and diagrams. **Racal-Milgo, Inc,** Miami, Fla.
Circle 310 on Inquiry Card

Software Packages

Bulletins detail features of std software packages for the company's microcomputer line, discussing micro and minicomputer resident assemblers, debug, and high level language packages. **Wyle Laboratories/ Computer Products,** Hampton, Va.
Circle 311 on Inquiry Card

Power Supply Applications

Power supply decoupling, preloading, and input transient suppression methods are treated tutorially in "Watts Up" journal, which also describes ac-dc and dc-dc supplies. **Semiconductor Circuits, Inc,** Haverhill, Mass.
Circle 312 on Inquiry Card

Sonic Digitizing

NT-101 Graf/Pen™ sonic digitizer, consisting of a stylus or cursor, electronics package, and sensor bar, is detailed in technical bulletin covering specs and dimensions. **Science Accessories Corp,** Southport, Conn.
Circle 313 on Inquiry Card

Text Editing System

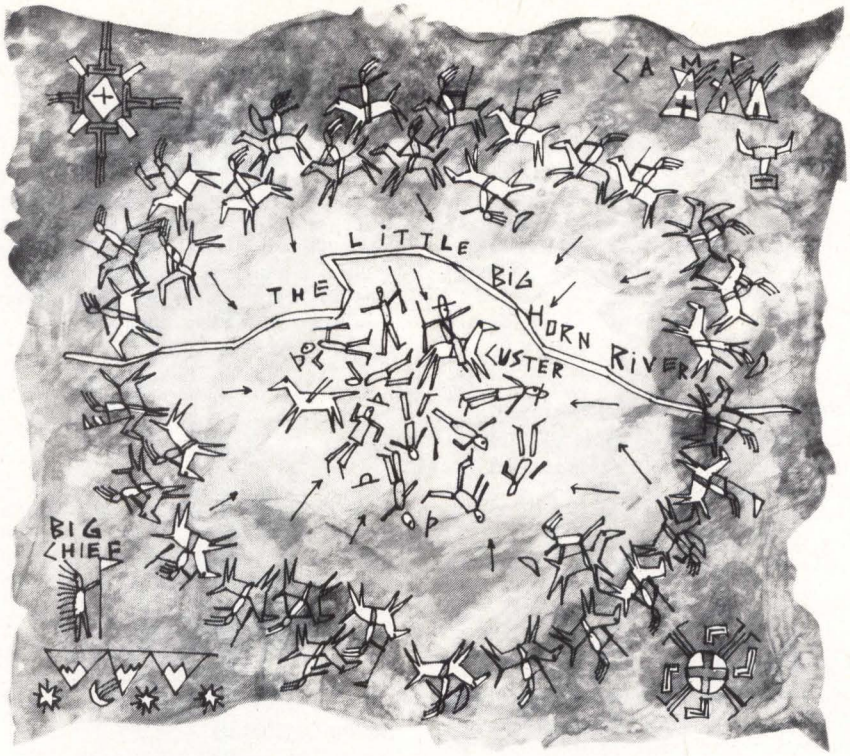
Booklet describes and gives examples of Aristotal™, an information management subsystem for word processing, which also performs arithmetic operations. **Proprietary Computer Systems, Inc,** Van Nuys, Calif.
Circle 314 on Inquiry Card

µProcessor Display Interfaces

Brochure provides summary of interfaces including video RAM, graphic, and alpha chip lines, with descriptions and tables specifying physical and electrical characteristics of each. **Matrox Electronic Systems,** Montreal, Quebec, Canada.
Circle 315 on Inquiry Card

Microcircuit Devices

Memory/LSI Data expands on reliability of LSI devices with data summaries of failure rates, screen and burn-in results, demonstration and environmental tests, field operation, and failure modes. Cost is $50 prepaid, $60 non-U.S. (#MDR-7). **Reliability Analysis Center,** Griffiss AFB, NY 13441.



On June 25, 1876, George Armstrong Custer ignored his scouts' warnings of many Indians gathered at Little Big Horn. So he rode out with 250 men to "surround" 6,000 Indians. This was a serious error.

Numbers can make all the difference.

It is always a serious error to ignore numbers or talk about them in vague terms. BPA (Business Publication Audit of Circulation, Inc.) guarantees the circulation figures of our member magazines — issue after issue. When you advertise in BPA-audited magazines, you get precise, nonpromotional numbers.

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LITERATURE

Interconnecting Devices

Catalog furnishes electrical and mechanical specs along with application and dimensional data for high voltage lead assemblies, harnesses, receptacles, and hermetically sealed connectors. **AMP Inc, Capitron Div,** Elizabethtown, Pa.
Circle 316 on Inquiry Card

Display Screens and Filters

Brochure on low reflectance LED display screens and filters features charts and selection guidelines to explain improvement of readability and resolution. **SGL Homalite, a div of SGL Industries, Inc,** Wilmington, Del.
Circle 317 on Inquiry Card

Subminiature Switches

Catalog outlines options and accessories of std subminiature toggle and pushbutton switches by including features, specs, and mechanical information. **American Switch Corp,** Wakefield, Mass.
Circle 318 on Inquiry Card

Power Supplies

Bulletin describes circuit characteristics, performance ratings, and specs of eight high performance, dual-output, ac-dc power supplies. **Intronics, Inc,** Newton, Mass.
Circle 319 on Inquiry Card

Microdevelopment System

Outlining the MicroCommand System™, brochure indicates user-oriented features and presents block diagram of system, along with available options. **Information Control Corp,** Los Angeles, Calif.
Circle 320 on Inquiry Card

40-Column Printers

Brochure contains general specs, descriptions, and outline drawing of DP-1000 series of self-contained, alphanumeric, ASCII compatible, mini and microcomputer printers. **Anadex, Inc,** Chatsworth, Calif.
Circle 321 on Inquiry Card

Backpanel System

Data sheet presents mechanical, electrical, environmental, and test specs for a multipin militarized interconnect backpanel designed for severe environment and high speed applications. **Fabri-Tek, Inc, National Connector Div,** Minneapolis, Minn.
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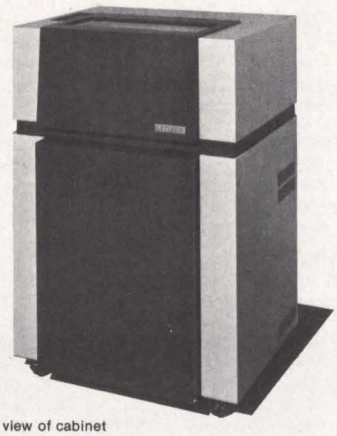
CITIZEN SERIES 8000 PRINTERS

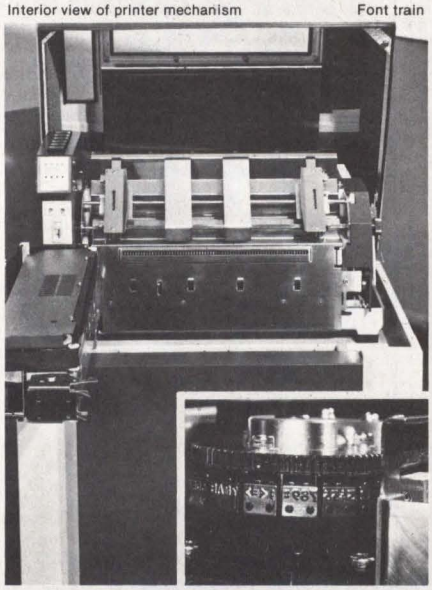
heavy-duty 132 Columns 250-720 LPM Chain Printer Excellent Quality and Price

Manufactured by
CITIZEN WATCH CO.
Tokyo, Japan



Exterior view of cabinet

Interior view of printer mechanism — Font train



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250 LPM — 64 characters	— 600 LPM
188 LPM — 96 characters	— 444 LPM

Full details on the competitive edge offered by the Citizen Series 8000 printers are yours for the asking. Call or write to:

Mike M. Fujiwara
Marketing Manager, Line Printers
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5301 Beethoven Street
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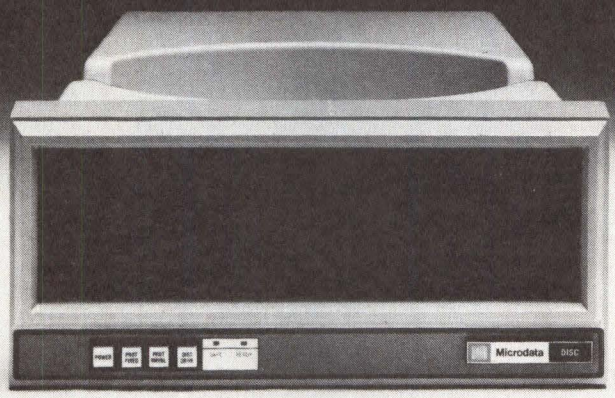
Marathon™ disc drive. The long distance runner. $2842*



The Marathon 5440 type disc drive gives you fast, dependable random access storage of 5 or 10 megabytes. Ten million bytes of on-line storage in 8.75 inches of rack space.

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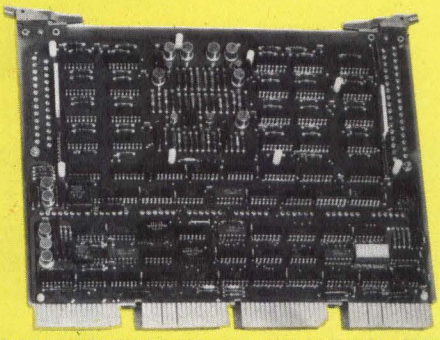

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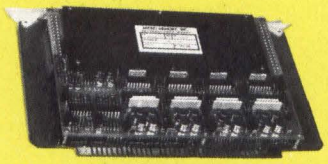

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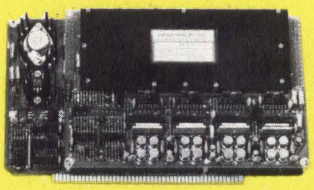

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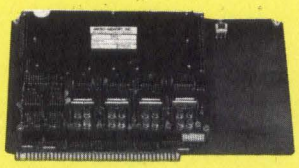

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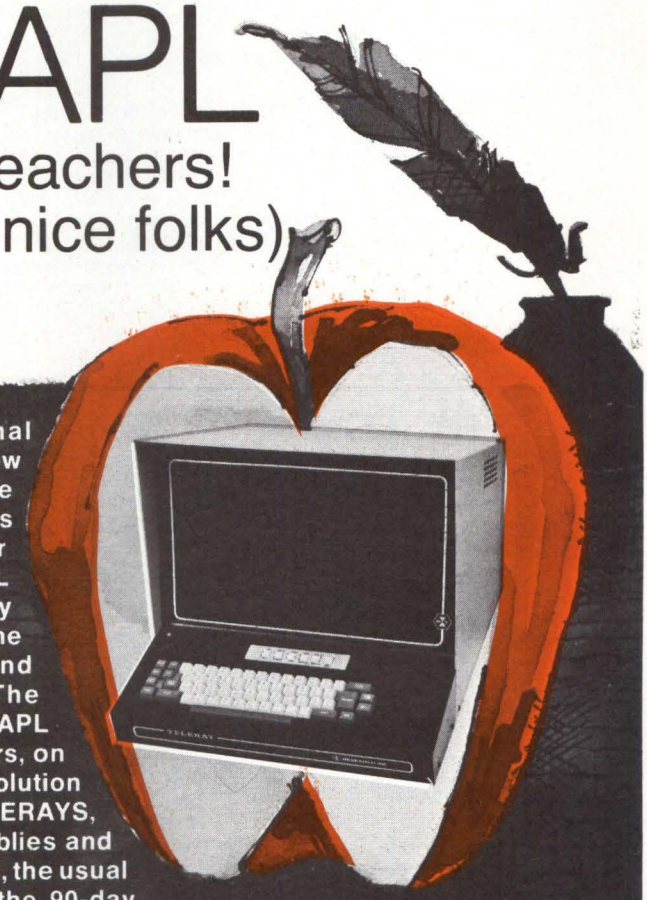

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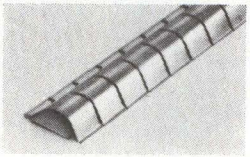

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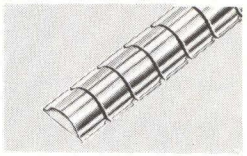

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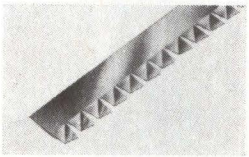

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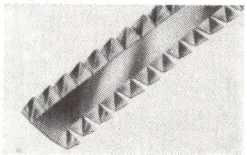

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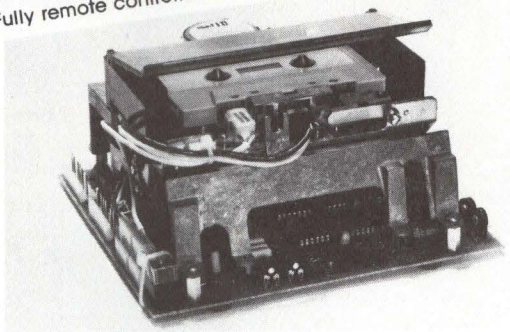

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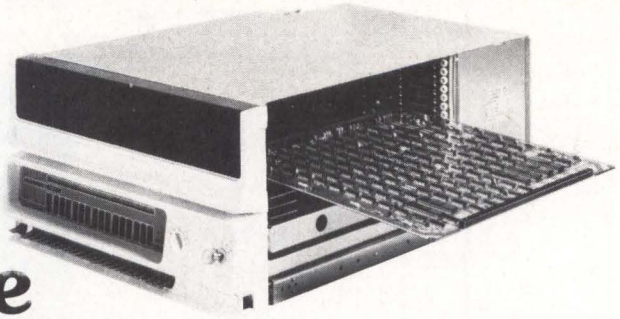

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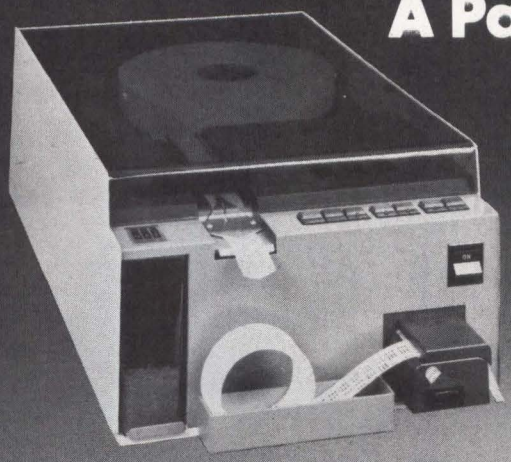

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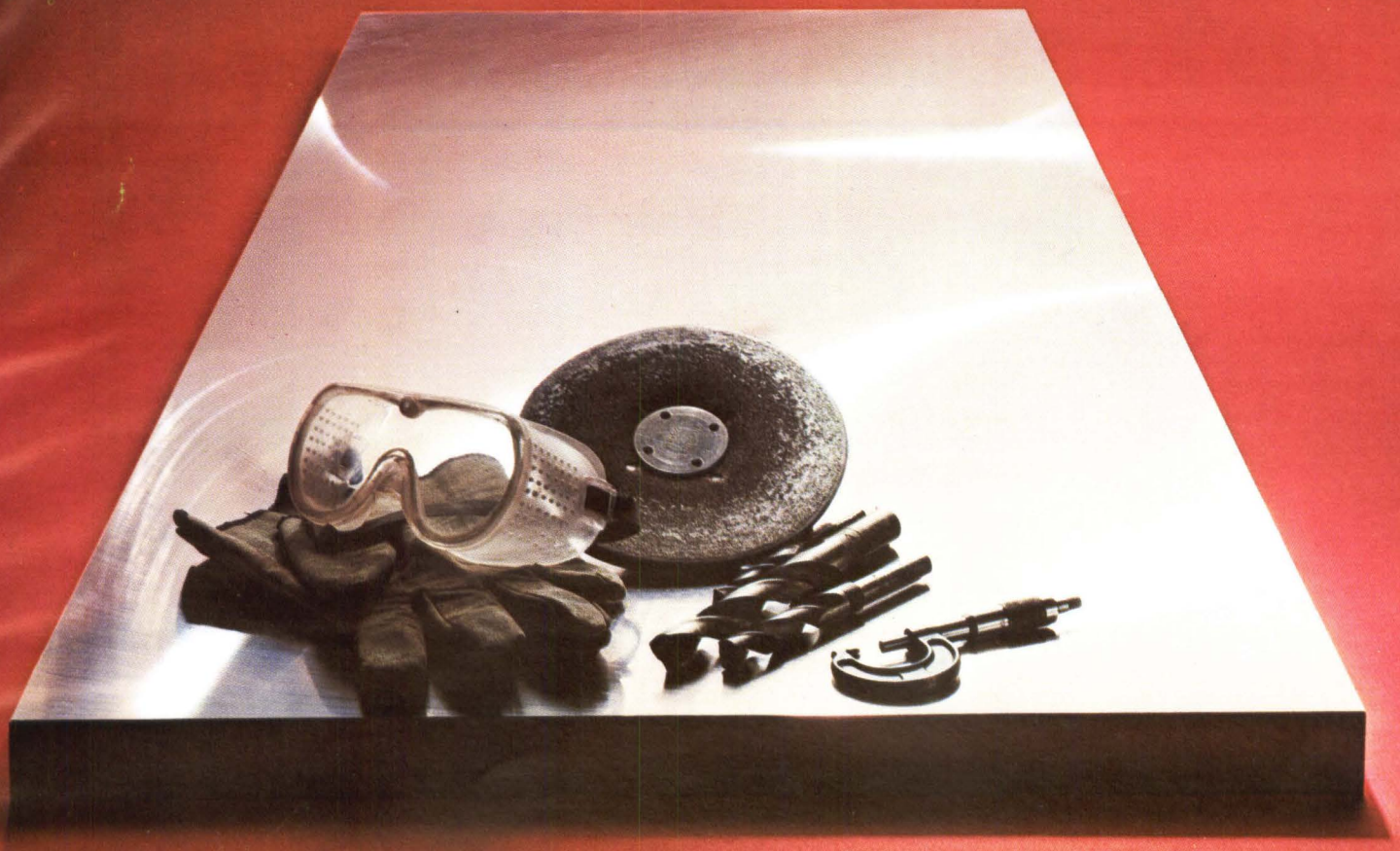

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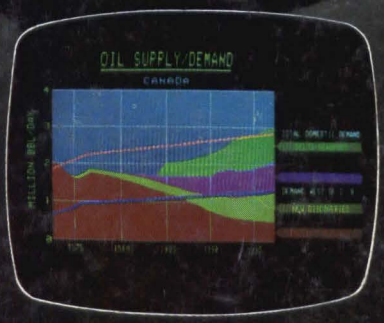

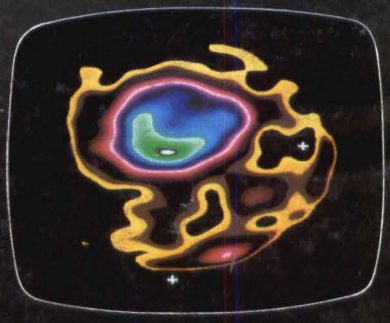

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