COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

JULY 1978

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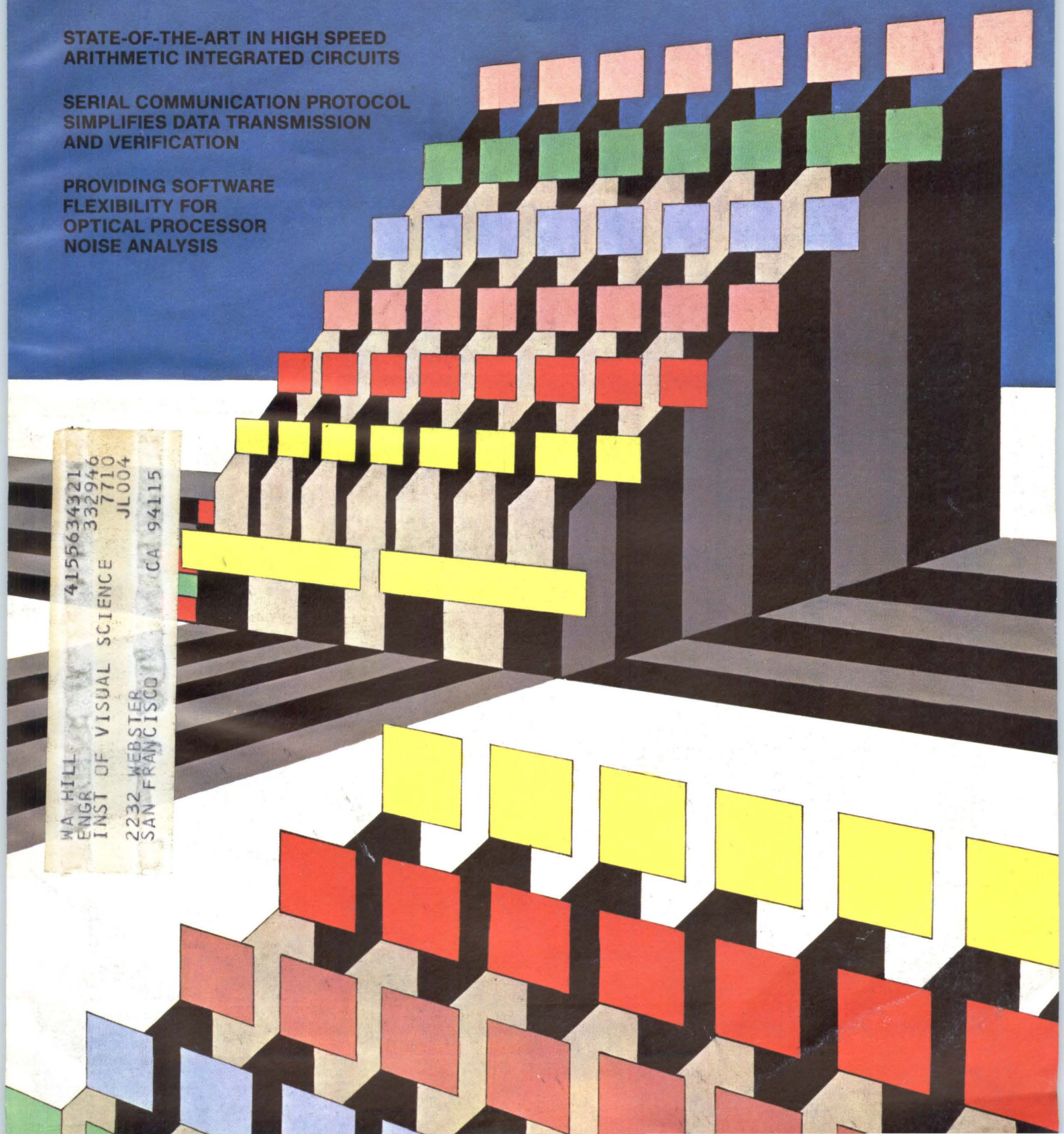

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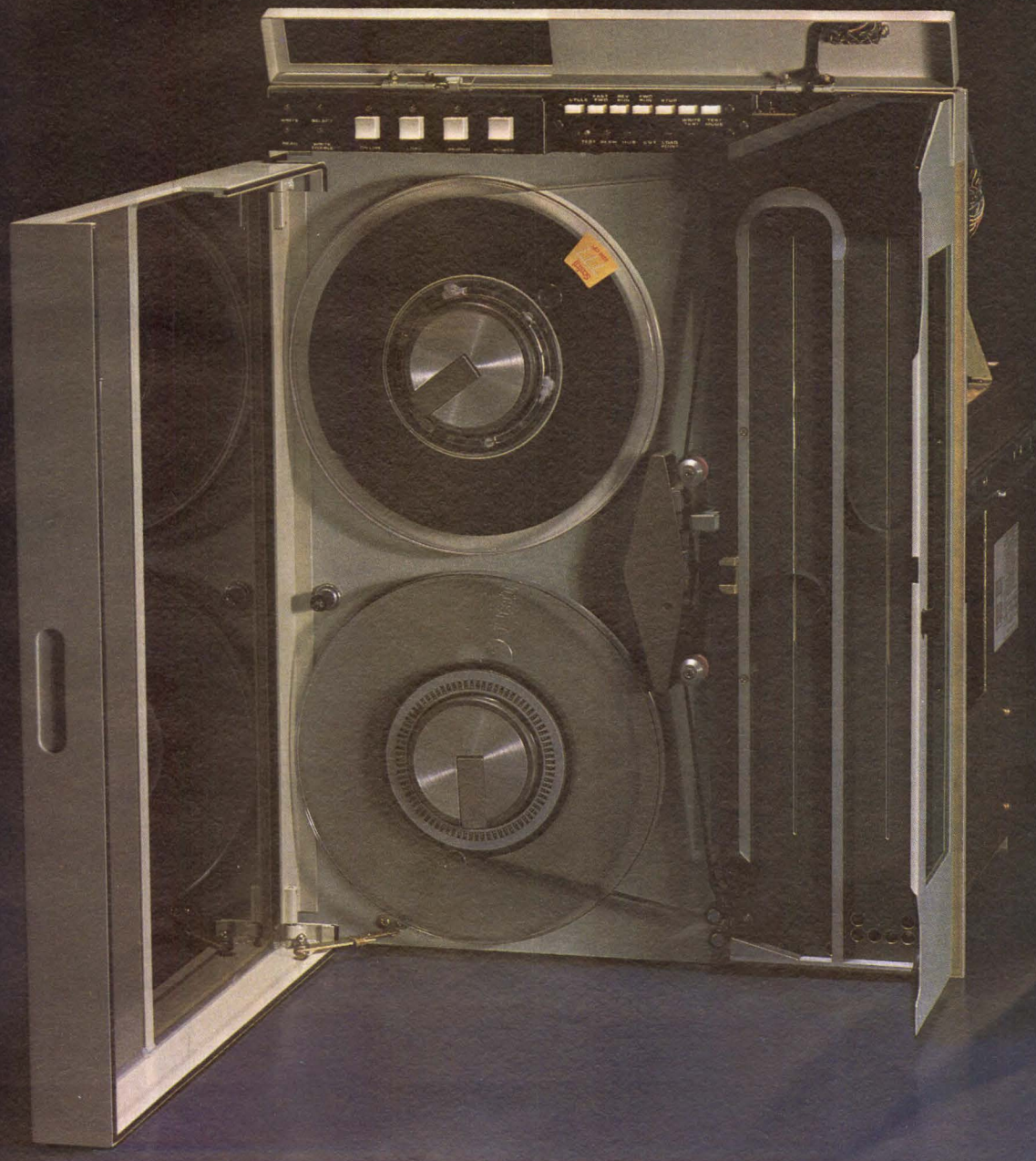

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COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

JULY 1978

VOLUME 17, NUMBER 7

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BPA

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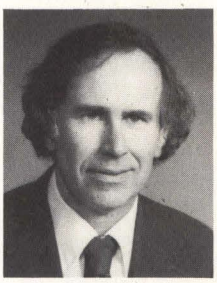
CIRCLE 5 ON INQUIRY CARD

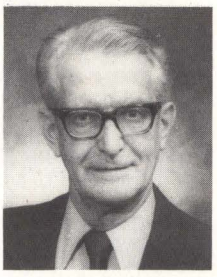
RECENT EDITORIAL APPOINTMENTS—

Computer Design has recently added two editors to its staff, one as a West Coast Editor based in Arcadia, Calif, and the other as an Associate Editor at the Littleton, Mass offices. Each has a varied and extensive background in magazine and/or book publishing.



Michael Chester
West Coast Editor

Mike Chester is the author of 25 published books, mostly on scientific topics, and has written many articles for publication in technical journals. He has a BA degree in physics from the University of California, Berkeley and has completed part of the requirements for an MA degree in biophysics at the University of California, Los Angeles. He has been a freelance author and independent consultant for a number of years.



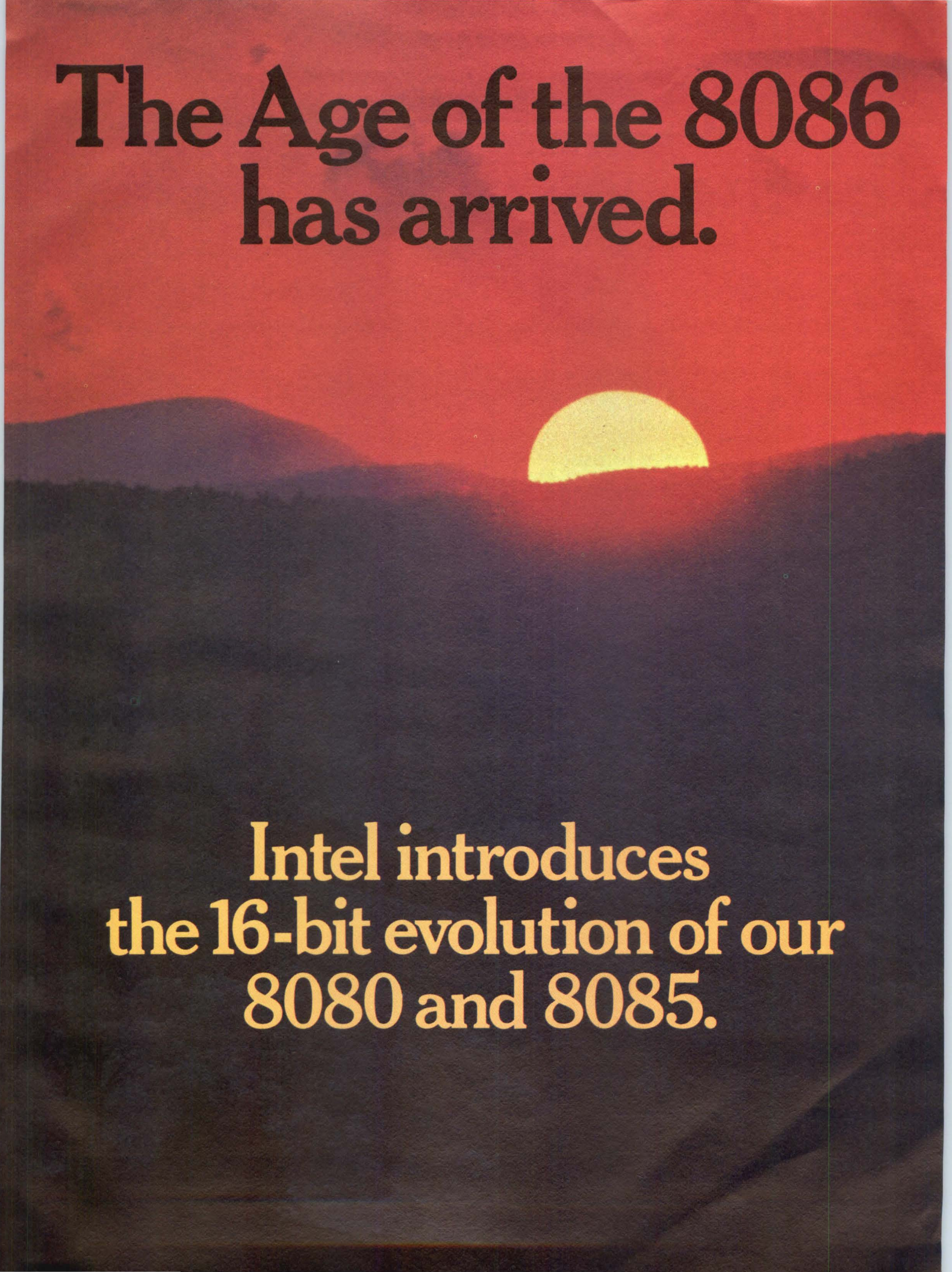
James W. Hughes
Associate Editor

Jim Hughes has been a staff member and developer of several technical magazines including *Microwave Journal* and *Solid State Design*. He founded the *Journal of the Association for the Advancement of Medical Instrumentation* and was Publisher and Editor of *Frequency Technology*, *Computer Component News*, and *Data Product News*. Most recently he was Managing Editor of *Telecommunications* magazine.

CORRECTION

The headline for the TRW LSI Products Div item on p 248 of the May issue should have read "70-ns Multiplier/Accumulator Can Be Communications Filter." Also, the company address should have been "PO Box 1125, Redondo Beach, CA 90278.

The Age of the 8086 has arrived.



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Circle No. 7 for more information

CALENDAR

CONFERENCES

AUG 20-25—Sym for Innovation in Measurement Science, Hobart/Smith College, Geneva, NY. INFORMATION: Peter Vestal, Instrument Society of America, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

AUG 21-31—17th USITA Data Communications Conf, Scheman Continuing Education Bldg, Iowa State U, Ames, Iowa. INFORMATION: Paul Bond, Conf Director, Engineering Ext, 110 Marston Hall, Iowa State U, Ames, IA 50011

AUG 22-25—Internat'l Conf on Parallel Processing, Shanty Creek Lodge, Bellaire, Mich. INFORMATION: Dr Charles S. Elliott, College of Engineering, Wayne State U, Detroit, MI 48202. Tel: (313) 577-3812

SEPT 4-8—Searcc 78, South East Asia Regional Computer Conf, Philippine Internat'l Conv Ctr, Manila, Philippines. INFORMATION: Searcc 78, Philippine Computer Society, MCC PO Box 950, Makati, Metro-Manila, Philippines

SEPT 5-8—COMPCON Fall '78, Capital Hilton, Washington, DC. INFORMATION: COMPCON Fall, PO Box 639, Silver Spring, MD 20961. Tel: (301) 439-7007

SEPT 6—Invitational Computer Conf, Newton, Mass. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: (714) 644-6037

SEPT 6-8—FOC '78, Fiber Optic and Communications Expo, Hyatt Regency-O'Hare, Chicago, Ill. INFORMATION: Information Gatekeepers, Inc, 167 Corey Rd, Suite 212, Brookline, MA 02146. Tel: (617) 739-2022

SEPT 6-8—Internat'l Optical Computing Conf, Imperial College, London, England. INFORMATION: S. Horvitz, Box 274, Waterford, CT 06385. Tel: (203) 442-0771

SEPT 12-14—Western Electronic Show and Convention (WESCON), Los Angeles Conv Ctr, Los Angeles, Calif. INFORMATION: W. C. Weber, Jr, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965

SEPT 15-17—Personal and Business Small Computer Show, New York Coliseum, New York, NY. INFORMATION: Personal Computing Expo Inc, 78 E 56th St, New York, NY 10022

SEPT 19-21—Computer Aided Design and Computer Aided Manufacturing Conf (CAD/CAM VI), Hyatt House, Los Angeles Internat'l Airport, Los Angeles, Calif. INFORMATION: Computer and Automated Systems Assoc of the Society of Manufacturing Engineers, 20501 Ford Rd, PO Box 930, Dearborn, MI 48128. Tel: (313) 271-1500, X403

SEPT 19-22—Conf on Microprocessors in Automation and Communications, U of Kent at Canterbury, England. INFORMATION: Conf Secretariat, Institution of Electronic and Radio Engineers, 99 Gower St, London WC1E 6AZ, England

SEPT 20-22—Telecomputer Application Group Conf, Washington, DC. INFORMATION: Hollis J. Sobers, Allied Chemical Corp, PO Box 1039R Morristown, NJ 07960. Tel: (201) 455-5123

SEPT 21-23—Interactive Techniques in Computer Aided Design, Palazzo dei Congressi, Bologna, Italy. INFORMATION: Dr Betram Herzog, Computer Ctr, U of Colorado, Boulder, CO 80303. Tel: (303) 492-6501

SEPT 26-28—Automatic Test Equipment Conf and Expo (ATEX), Hynes Auditorium, Boston, Mass. INFORMATION: Bill Hickey, Golden Gate Enterprises, 1307 S Mary Ave, Suite 210, Sunnyvale, CA 94086

SEPT 26-29—Internat'l Conf on Computer Communication (ICCC-78), Kyoto Internat'l Conf Hall, Kyoto, Japan. INFORMATION: ICCC-78 Executive Committee, c/o Internat'l Affairs Bureau NTT, 1-6, Uchisaiwai-cho, 1-chome, Chiyoda-Ku, Tokyo 100, Japan

SEPT 29-OCT 1—Internat'l Microcomputer Expo, Dallas Convention Ctr, Dallas, Tex. INFORMATION: Beverly Tanner, Expo Director, 413 Carillon Tower, 13601 Preston Rd, Dallas, TX 75240. Tel: (214) 271-9311

OCT 6-11—Japan Electronics Show, Tokyo Internat'l Trade Ctr, Tokyo, Japan. INFORMATION: Japan Electronics Show Assoc, No. 24 Mori Bldg, 11 F, 3-23-5, Nishi-Shinbashi, Minato-ku, Tokyo 105, Japan

OCT 10-12—Conf of the European Cooperation in Informatics (ECI), Venice, Italy. INFORMATION: Prof Dr Peter Lockemann, Institut für Informatik II, Universität Karlsruhe, Postfach 6380, D-7500 Karlsruhe 1, Germany

OCT 16-19—ISA/78, Instrument Society of America's Internat'l Instrumentation-Automation Conf and Exhibit, Philadelphia Civic Ctr, Philadelphia, Pa. INFORMATION: ISA/78, Philadelphia, Information Request, 400 Stanwix St, Pittsburgh, PA 15222

OCT 17-19—EUROMICRO 78, Sym on Microprocessing and Microprogramming, Munich, Germany. INFORMATION: Dr Helmut Berndt, Siemens AG, Div WS PZ1, Postfach 70 00 78, D-8000 München 70, West Germany

OCT 18-20—Canadian Conf on Communications and Power, Queen Elizabeth Hotel, Montreal, Canada. INFORMATION: Jean Jacques Archambault, Chm-Technical Program Committee, CP/PO 757, Succ C, Montreal, Quebec H2L 4L6, Canada

OCT 25-27—Sym on Computer Arithmetic, Miramar Hotel, Santa Monica, Calif. INFORMATION: Prof Milos D. Ercegovac, Computer Science Dept, U of Calif, Los Angeles, CA 90024. Tel: (213) 825-2660

NOV 7-9—Mini/Micro Conf and Expo, Astrohall, Houston, Tex. INFORMATION: Robert D. Rankin, Managing Director, Mini/Micro Conf and Expo, 5528 E La Palma Ave, Suite 1, Anaheim, CA 92807

NOV 20-22—BIAS Internat'l Conf: Automation and Microcomputer, Milan Fair Ground, Milan, Italy. INFORMATION: Federazione delle Associazioni Scientifiche e Techniche, Piazzale Roldolfo Morandi, 2, 20121 Milan, Italy

DEC 18-20—Internat'l Computer Sym (ICS), Academia Sinica; Nankang, Taipei, Republic of China. INFORMATION: K. S. Fu, School of Electrical Engineering, Purdue U, W Lafayette, IN 47907. Tel: (317) 494-8825

SEMINARS

AUG 21-23—Computer Networks, Continental Plaza, Chicago, Ill. INFORMATION: Technology Transfer Inc, PO Box 49765, Los Angeles, CA 90049. Tel: (213) 476-1331

SHORT COURSES

AUG 7-11—Electronic Counter Measures and Electronic Counter Counter Measures (ECM and ECCM) for Digital Communications, Howard Johnson's Motor Lodge, Redwood City, Calif. INFORMATION: Continuing Engineering Education Program, George Washington U, Washington, DC 20052. Tel. (202) 676-6106

AUG 7-18—Computer Graphics, Massachusetts Institute of Technology, Cambridge, Mass. INFORMATION: Director of the Summer Session, Rm E19-356, MIT, Cambridge, MA 02139. Tel: (617) 253-5960

AUG 22-24—Microcomputer Interfacing Course, Philadelphia Hilton Hotel, Philadelphia, Pa. INFORMATION: Dr C. Titus, Course Director, Tychon, Inc, PO Box 242, Blacksburg, VA 24060. Tel: (703) 951-9030

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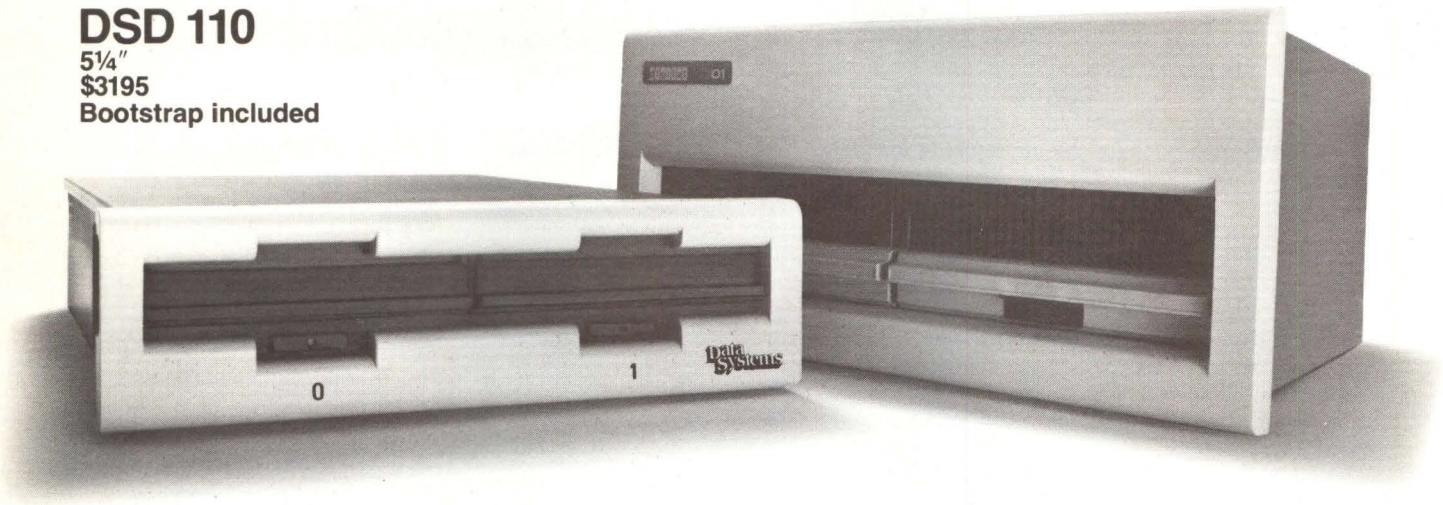

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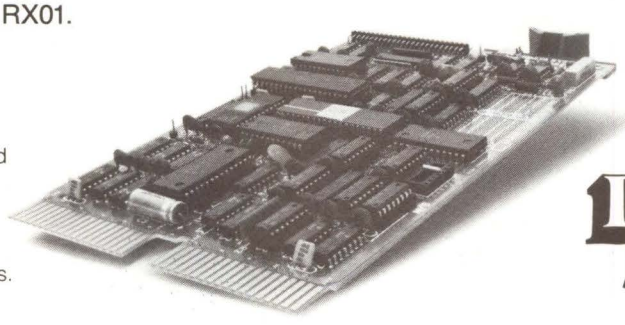


Data Systems has combined interface, formatter, controller, and hardware bootstrap on this single dual-wide card. Available separately in OEM quantities.

Data Systems

CIRCLE 8 ON INQUIRY CARD

CERTIFICATION UPDATE

John E. Buckley

Telecommunications Management Corporation
Cornwells Heights, Pennsylvania

On April 13, 1978 the FCC (Federal Communications Commission) issued the finalization of certification standards and procedures referred to in the December 1977 Communication Channel, "Certification 1977." With the release of its Third Report and Order in Docket 19528, the FCC attempts to complete implementation of the PBX (Private Branch Exchange) and Key Telephone Equipment System Registration Program. Encompassed also within the scope of this Order is the application of computerized telephone systems, which actually are digital computer systems with TDM (time division multiplex) switching rather than the traditional electromechanically switched systems. The Report and Order adopts regulations governing cabling associated with telephone system installations, means for the connection of these systems to the telephone network, and "grandfathering" standards for existing installed telephone systems. These equipment registration standards are intended to eliminate present requirements for utility telephone company-provided protective devices. However, the rules do not abolish protective devices entirely; rather, they specify the requirements that must be met as alternatives to connecting arrangements provided by the telephone company.

The Report and Order, effective June 1, 1978, does not fundamentally change the equipment registration standards previously adopted by the FCC. In general, the technical specifications have established boundaries for each separate technical condition such as hazardous voltage and signal power. When registered communications equipment and systems are installed in compliance with FCC standards with respect to both installation cabling and to the actual means of connection, connecting arrangements are, generally, not required. Compliance with the FCC standards is a matter of considerable complexity and, depending upon the type of installation involved, may itself require use of some form of protective device. The new rules address two areas: installation cabling (referred to as Premises wiring), and actual connection to the public telephone switched network.

Premises Wiring

Premises wiring is defined as wiring which connects the communications system components to one another. It also includes telephone network interface equipment located at the customer's site. The FCC has defined three separate classes of premises wiring: fully protected, protected and "other."

Fully protected wiring is cabling not greater than 25 ft (7.6 m) in length, registered as a component of and supplied to the user with the registered terminal equipment. Fully protected wiring must be preconnected to the equipment. It may be designed for connection by the installer or user if the registration application demonstrates that no harm will result from such connection. Premises wiring is also fully protected if it is electrically behind registered or grandfathered equipment. This assures that electrical contact between the cabling and commercial power wiring, including ground, will not result in either hazardous voltages or excessive longitudinal imbalance at the telephone network interface. Under the rules, fully protected wiring *must* be used to connect common equipment to the network interface equipment unless the telephone company is unable to locate the interface to within 25 ft (7.6 m) of the common equipment.

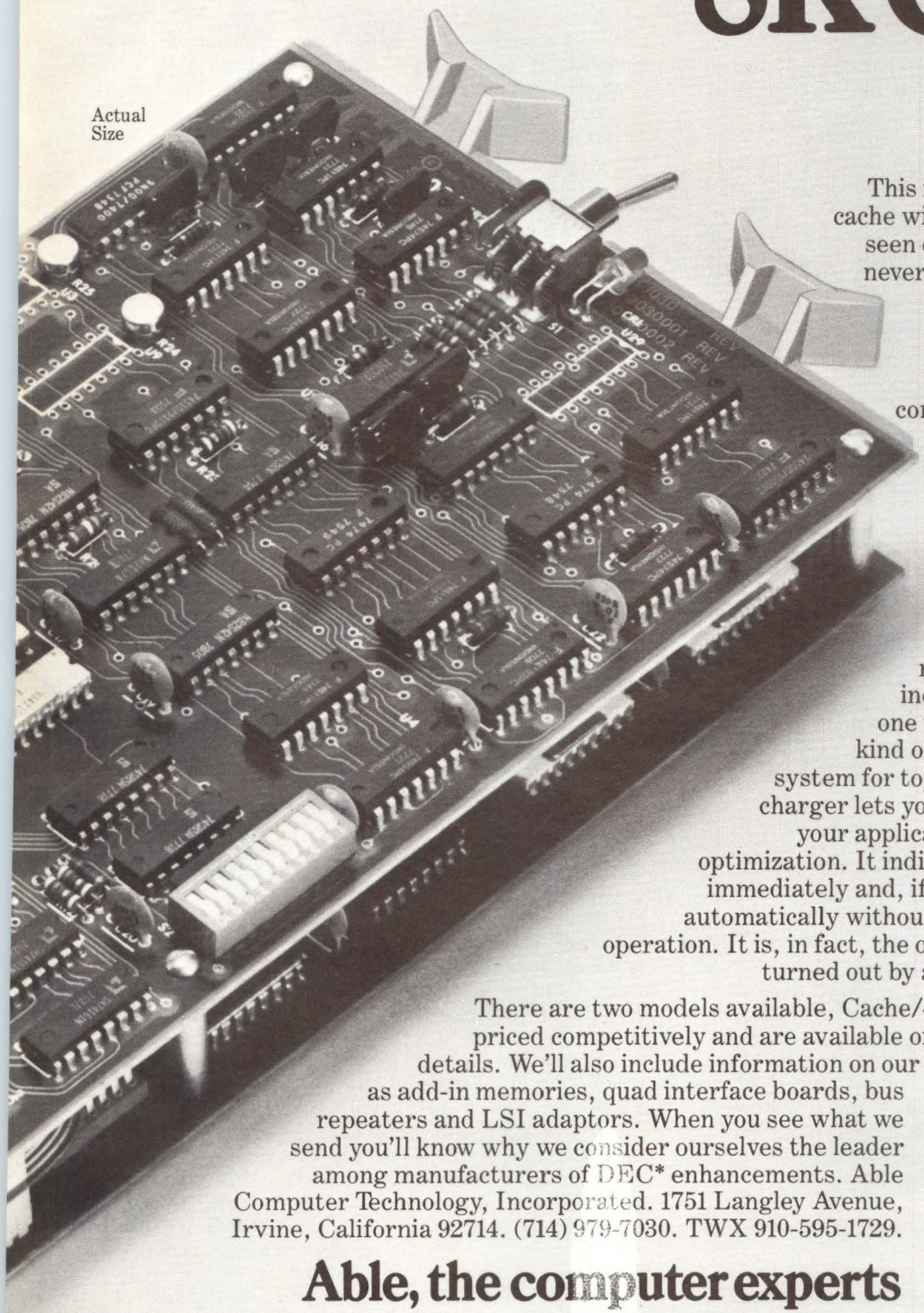
Protected premises wiring is that which is electrically behind registered or grandfathered equipment systems, components, or circuitry, which assures that electrical contact between the cabling and the commercial power wiring will not result in hazardous voltages at the telephone network interface. Principal difference between fully protected wiring and protected wiring is that with the former, the equipment provides design assurances against both hazardous voltage and longitudinal imbalance at the point of network connection, while the latter provides design assurances only against hazardous voltage. Use of the 25-ft (7.6-m) cabling to connect with the network does not render an installation fully protected where the premises wiring that connects system components is itself merely protected rather than fully protected.

Other premises wiring does not fall into either of the above categories. To maintain dc continuity, a transformer may not be interposed between unprotected wiring and the network interface. Obviously, transformer coupling used in the equipment design which has adequate balance and voltage breakdown ratings would render the wiring fully protected under the above definition. Other premises wiring and protected premises wiring may be used to connect separately housed equipments to each other but may not be used to connect to the network except where the utility telephone company is unable to locate the network interface within 25 ft (7.6 m) of the equipment.

Classification of premises wiring is the single most important determinant of what type of protective circuitry and/or testing and inspection requirements, if any, must be met prior to connection of the communications system to the telephone network. Assuming that requirements of the rules are otherwise met, where fully protected wiring is involved no further protective circuitry or testing procedures are necessary. The only requirement is a simple notice to the telephone company that a fully

The Incredible 8K Cache

Actual Size



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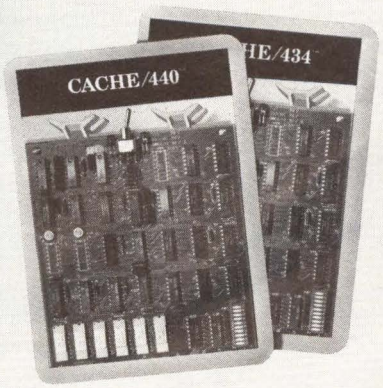
That's why there is always room in your computer for this incredible cache. You should put one there, especially if you are the kind of guy who likes to optimize his system for top performance. Our 8K super-charger lets you tailor performance to match your application and to establish hit-ratio optimization. It indicates hit rate and parity error immediately and, if errors are detected, shuts off automatically without ever interfering with system operation. It is, in fact, the only intelligent buffer memory turned out by an independent manufacturer.

There are two models available, Cache/434™ and Cache/440™. Both are priced competitively and are available off-the-shelf as usual. Write for details. We'll also include information on our other buffer memories as well as add-in memories, quad interface boards, bus repeaters and LSI adaptors. When you see what we send you'll know why we consider ourselves the leader among manufacturers of DEC* enhancements. Able Computer Technology, Incorporated. 1751 Langley Avenue, Irvine, California 92714. (714) 979-7030. TWX 910-595-1729.



Able, the computer experts

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CIRCLE 9 ON INQUIRY CARD

protected system is being installed. Changes and rearrangements may be made without the use of protective circuitry. As a practical matter, at the present time compliance with this standard will be possible only in the case of fully electronic PBX systems which use a 25-ft (7.6-m) cord for connection to the network.

In the case of protected premises wiring and unprotected premises wiring, the regulations establish a series of requirements in addition to the notice which must be met before the system can be lawfully connected to the network.

Network Connection

The means of connection of the communications system to the telephone network must also conform to the rules established by the FCC. The regulations apply to all key, CBX, and PBX installations, even when fully protected wiring is involved. For the vast majority of such installations, the FCC rules require the use of fully connectorized interfaces. Typically, the interface consists of a multiline plug with corresponding jack installed by the telephone company. Recognizing, however, that this fully connectorized approach can limit and increase the difficulty of rearrangements, the regulations permit cross-connect adapters to be used. Punch-down terminal strips and field-installable connectors are not ordinarily permitted under the FCC rules.

One limited circumstance in which field installable connectors (but not punch-down terminal strips) may be used is where the telephone company is unable to locate the interface within 25 ft (7.6 m) of the equipment. In this case the FCC states that field-installable connectors, other than the punch-down blocks, may be used.

Although these provisions concerning standard means of connection are stated to be mandatory, there is an important exception. Rules provide that the "telephone company and installation supervisor may mutually agree to use electrical connections alternative to those specified." The FCC has stated that it has no wish to limit flexibility at the time of installation, and this provision has been specifically added to permit such mutually agreeable flexibility in the means of connection, including punch-down strips.

Grandfathered Installations

Single most difficult aspect of the Third Report and Order relates to the grandfather standards that have been established for key, CBX, and PBX telephone systems. Purpose of the grandfathering provisions is to take into account existing installations which may not comply with the new rules, and to provide a transitional period during which manufacturers can reconfigure their designs in order to make equipment conform to the new technical standards.

All terminal equipment (other than CBX, PBX, and key) of a type directly connected to the telephone network as of October 17, 1977 may be connected and remain connected for life without registration unless subsequently modified. The FCC has established a list of the types of equipment which meet this test.

In the case of key, CBX, and PBX equipment, the grandfathering rules are more complicated. They do not, necessarily, permit direct connection of such systems even though systems of the identical type may previously have been directly connected to the telephone network. The different rules are based upon the FCC's belief that the bulk of these customer-provided telephone systems have been installed behind utility telephone company-provided connecting arrangements and therefore some method of continued protection is required.

The first category of grandfathered key, CBX, and PBX systems are those which have already been installed. Under the FCC rules, the entire system is grandfathered for life unless modifications are made. Note that grandfathering encompasses the entire system. Thus, if a system was directly connected to the network, it is grandfathered; but if the system was installed using a connecting arrangement, the combination of equipment and connecting arrangement is grandfathered and the connecting arrangement cannot be removed except as provided in the rules. In other words, even if the equipment is of a type which was directly connected to the network, the carrier-provided connecting arrangement cannot automatically be removed. It is possible, although unlikely, that some customers will be content to continue using the carrier-provided connecting device.

The second category of grandfathered equipment involves key, CBX, and PBX systems where the customer desires to remove the carrier-provided connecting device, or where modifications or additions are to be made to the system. Additions to grandfathered systems connected to the network on June 1, 1978 may be made up to July 1, 1979 without registration of the additional equipment. The new equipment added must be of a type directly connected to the telephone network as of October 17, 1977 and any wiring added must conform to the new rules governing premises wiring.

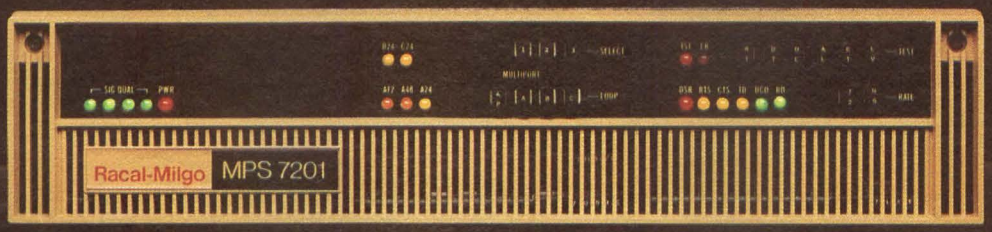
There are two methods by which utility telephone company-provided connecting arrangements on grandfathered systems may be removed. First, any existing system which is connected to the telephone network through a telephone company connecting arrangement may replace the arrangement with a device owned by the customer. However, the rules governing premises wiring must be satisfied. If the telephone company-provided device is replaced with a device which guards against both hazardous voltage and longitudinal imbalance, the rules governing fully protected wiring would apply; however, if the existing device is replaced with a device which guards only against hazardous voltage, the change would require compliance with the rules applicable to installation of protected wiring.

The second method by which a carrier-provided connecting device can be removed requires that an affidavit be obtained from the person who originally supervised the installation of the existing premises wiring; if that affidavit shows compliance with the documentation requirements of the new rules, the existing utility telephone company-provided hardware protection may be removed. If new wiring is required to restore compatibility of the system with the network, the rules governing installation of premises wiring must be satisfied. This would occur in cases where the existing connecting arrangements typically perform an interface function as well as a protective function.

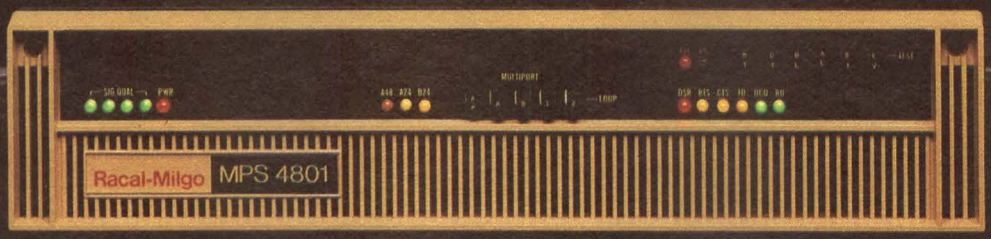
The final category of "grandfathered" equipment involves new installations during the period between June 1, 1978 and July 1, 1979. In this category, specific equipment types connected directly to the telephone network as of October 17, 1977 and therefore appearing on the FCC "grandfather list" may be installed even though they are not registered. However, premises wiring associated with the installation of such grandfathered equipment must comply with the new rules governing premises wiring. Thus, in terms of the installation of new systems prior to July 1, 1979, there is no practical difference between registered equipment and grandfathered equipment. In both cases the premises wiring standards must be met. After July 1, 1979, the equipment must be registered and the premises wiring and means of connection standards must be satisfied.

Racal-Milgo's new modems make sure you get every millisecond's worth from your data channels.

The MPS 9601 series includes 6 models of synchronous modems that deliver full 9600 bit-per-second data transmission in both point-to-point and multipoint networks. The modems offer unique cost saving advantages such as FASTRAN™ ultra-fast 30 millisecond response time and DYNAPORT™ automatic channel allocation as well as multiport operation and modem sharing. Models are available with CCITT/V.29 modulation.



The MPS 7201 modem series provides synchronous 7200 bps data communication over unconditioned lines in point-to-point or multipoint networks. Four models offer a selection of high efficiency features that include up to three independent ports, FASTRAN ultra-fast response time, diagnostics and DYNAPORT automatic channel allocation.



The MPS 4801 series offers optimum 4800 bps data communication over unconditioned lines in point-to-point or multipoint networks. Modems in this series are available with either a single 4800 bps data port, or with two 2400 bps ports. Cost-saving options, including DYNAPORT and FASTRAN, are available in this series.

The exceptional advantages offered in this new series of microprocessor-based modems are fully described in our 12-page brochure. We'll gladly rush you a copy.

Racal-Milgo™ – the new name for ICC

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Racal-Milgo Information Systems, Inc.
8600 N.W. 41st Street Miami, Florida 33166 Telephone (305) 592-8600 TWX: 810-848-6588

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CIRCLE 10 ON INQUIRY CARD

New Developments from SYSTEMS...

The SEL 32/30

Until now, you've either had to forego 16-bit pricing to get 32-bit performance, or you've had to give up 32-bit performance just to keep the budget in line.

No longer. Now you can invest in a full-blown 32-bit computer and pay no more than you would for a 16-bit computer. And not have to worry about insufficient power for future needs.

The SEL 32/30 is the smallest of the SYSTEMS hierarchy of 32-bit computers. But don't let its small size fool you. This MAXIBOX is big in performance and throughput, ideally suited for scientific or process control applications such as telemetry, simulation, industrial or laboratory automation. And it costs you no more than a 16-bit computer.

The SEL 32/30 is value-engineered for the OEM. It is a single chassis, fully integrated system that is upward compatible with the entire SEL family of 32-bit computers. So even if you start with a minimal investment, it will continue to pay off as your customers' applications expand.

If power and performance are what you need, and budget is a definite consideration, talk to us. We'll make sure that when you invest in a SEL 32/30 MAXIBOX, more dollars will flow to your bottom line.

Call us. We're easy to talk to.
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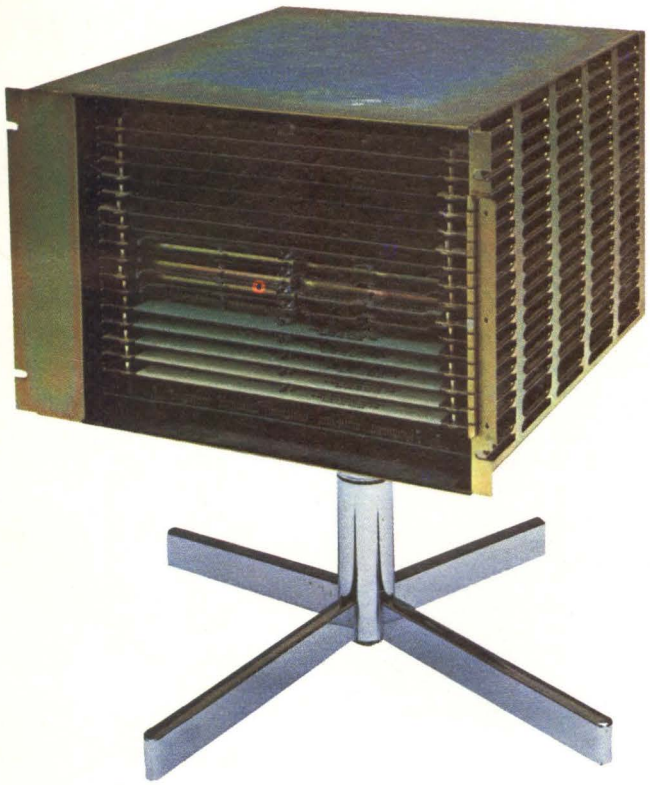
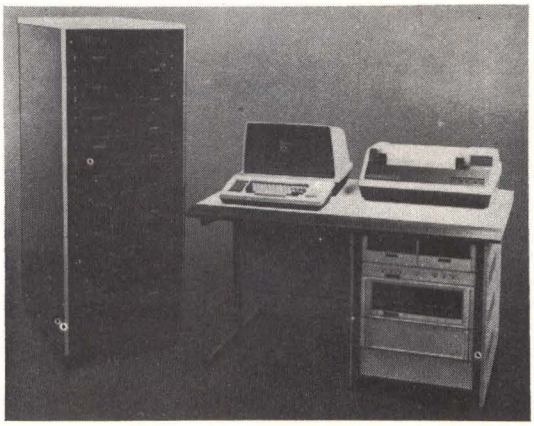
MOS MAXIBOX.™



SYSTEMS
ENGINEERING LABORATORIES

CIRCLE 11 ON INQUIRY CARD

Analysis System Automates Diagnosis of Circuit Faults in Data Communications Networks



Analysis CCB network management system control center. Operator can view complete status of any network drop, can determine levels of line noise, loss and/or phase jitter, measure modem voltage to within 0.01 V, measure line hit errors, and determine modem receive levels, phase jitter, and S/N ratio within 1.0 dB

"Analysis" network management system automatically tracks performance of data communications networks in real time and provides specific information on circuit problems in conversational English. System gathers and stores data on the condition of as many as 144 lines, modems, and terminals in point-to-point and multidrop networks, displays data in plain English, and provides control over modems throughout the network. It additionally gathers management reports on network, line, and modem availability.

Key to the system is the MP-48 4800-bit/s programmable modem, which uses dual microprocessors rather than hardwired logic or LSI circuits, according to Paradyne Corp, 8550 Ulmerton Rd, Largo, FL 33541. One of the microprocessors handles such functions as equalization, scrambling, encoding and filtering; the other provides dynamic information on transmission impairments, and controls the modem processor during diagnostics.

A 110-baud noninterfering diagnostic channel, monitored by a minicomputer based central site diagnostic processor, links MP-48 master and slave modems. Major system components are the central site control unit, one or more MP-48 master modems, and up to several hundred slave modems throughout the network.

The CPU is a 16-bit microprocessor with 667-ns memory, 16 general purpose registers with context switch capability, and workspace capability for fast interrupt handling. Hardware instruction set offers easy bit/byte manipulation, and includes floating point arithmetic with hardware multiply/divide. Main memory is expandable from 24k to 64k bytes in 8k-byte increments. Up to four diskette drives can be supported for direct access storage; a floating head disc capable of storing from 1M to 3M records will be available.

RS-232-C asynchronous interface is provided for 110-baud rates; basic Analysis system handles up to 17 lines expandable to 39. Transmission is in 8-bit ASCII. System software comprises ANSI standard FORTRAN IV supplemented by CALLS to assembly language subroutines. Available software includes an executive, and a series of independent modules, such as Autoscan, which in turn call out secondary modules.

Information on such performance parameters as noise, loss, phase jitter, amplitude, and phase delay distortion is gathered from every drop on the network, is assembled and analyzed for exception and alarm states, and is displayed in conversational English on CRT screen or LED readout.

System comes in two versions: CCA, priced from $3500, and CCB, with large CRT based control monitoring station, from $36,600. Availability is 90 days ARO.

Circle 400 on Inquiry Card

Message Communication Terminal Line Is Expanded

A number of enhancements to its model 43 family, and a 5-level model 42 terminal were recently announced by Teletype Corp, 5555 Touhy Ave, Skokie, IL 60076. Model 43 8-level message terminals, configured in Receive/Only (RO), Keyboard Send/Receive (KSR), and Automatic Send-Receive (ASR), are capable of interactive and batch communications. Buffered 43 terminals are now offered for point-to-point and multipoint communications, providing 20k chars of storage for sending, receiving, and editing.

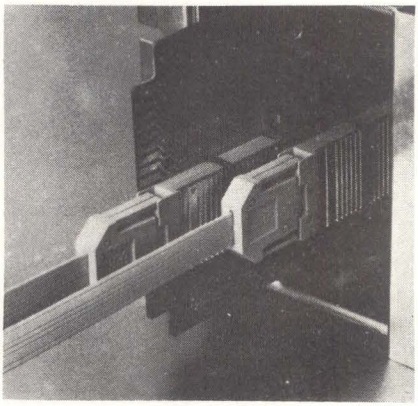
Terminals can automatically send and receive online via the buffer at 10 to 180 chars/s, while messages are being simultaneously edited and prepared for future transmission. Buffered ASR units include paper tape facilities. For editing, any text can be located by string searching, retrieved, and changed by character deletion and insertion.

Model 42 shares design elements of the 43 but has a 5-level code configuration for compatibility with the CCITT #2 standard.

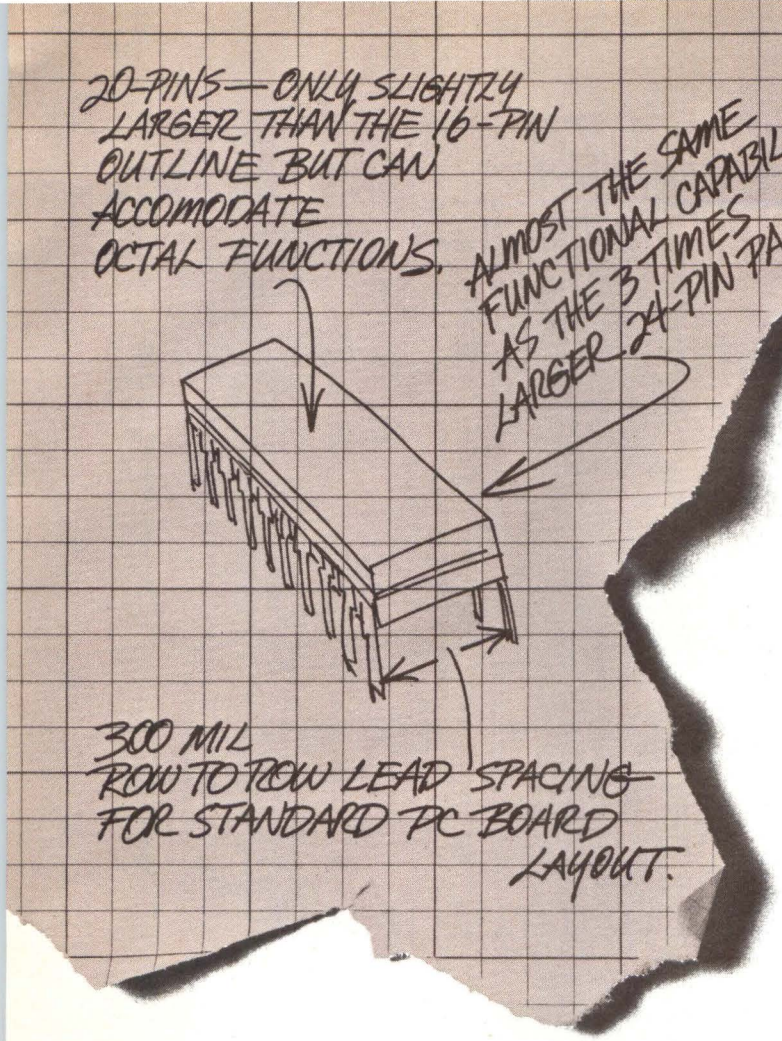
Circle 401 on Inquiry Card

Fiber Optic Link Provides TTL Compatible Duplex Data Transmission

Two transmitter/receiver modules and a preterminated duplex cable, 30 m in length, are combined in a fully assembled and tested fiber optic data link from 3M Co, Dept EP8-26, Box 33600, St Paul, MN 55133. The link uses duplex cable with two discrete low loss plastic clad silica fibers of



Link interconnection to PC board. Required signals are brought to a standard 3M PCB header. Transceiver module measures 0.375" x 1.25" x 2.5" (0.95 x 3.175 x 6.35 cm) and can be used in a card cage without modification. Preterminated, mechanically polarized duplex cable connector assembly incorporates internal strain relief for protection of the fiber optics



Eighteen months ago, we announced the start of a whole new family of 20-pin parts.

We told you that the 20-pin configuration not only made better packages—it made better ideas.

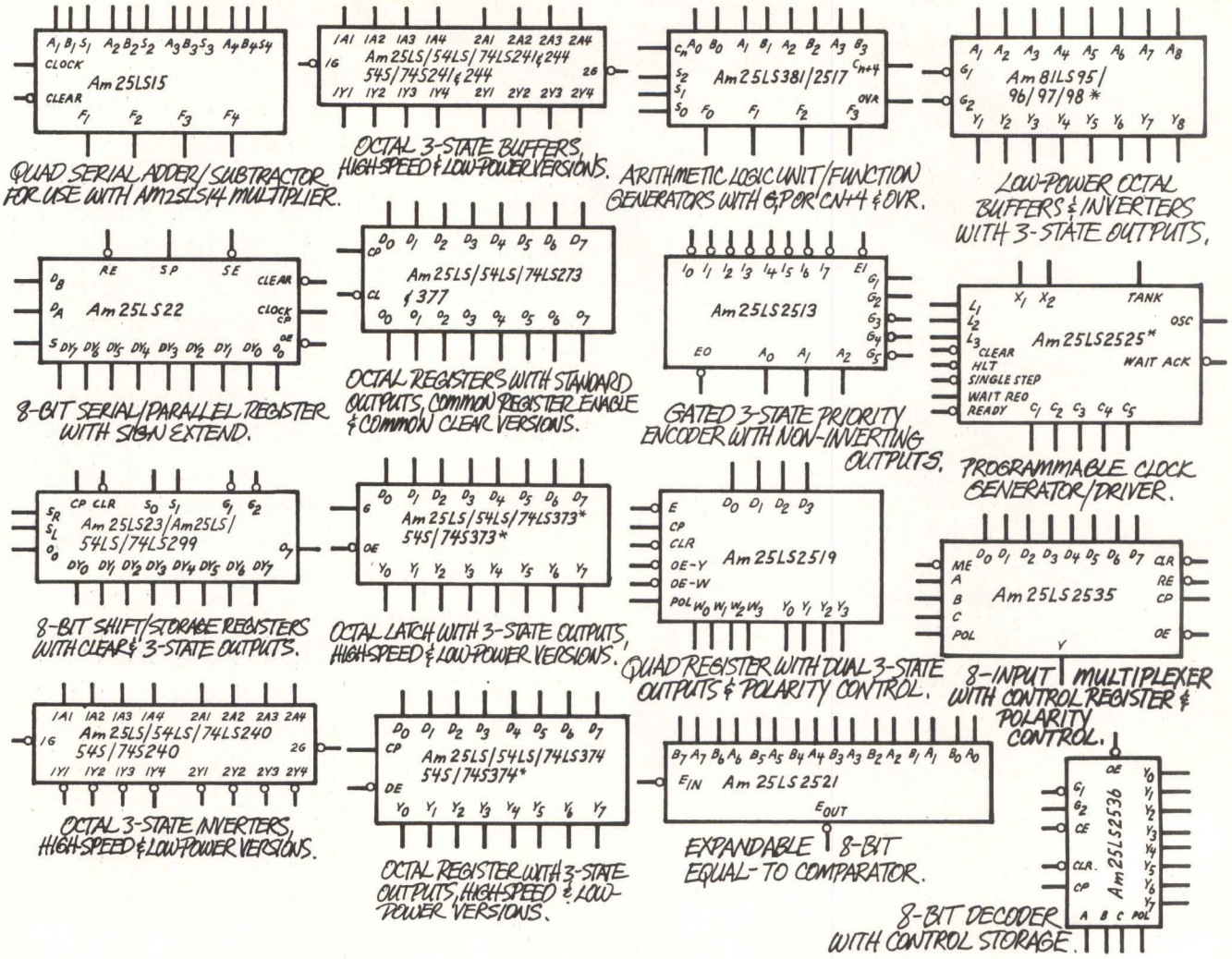
We told you all about 8-bit low-power Schottky buffers, registers and decoders.

Remember? "Perfect for use with 8-bit 8080-type microprocessors—as well as 2900, 4-bit bipolar slices. No more trying to manage too-much 24's and not-enough 16's."

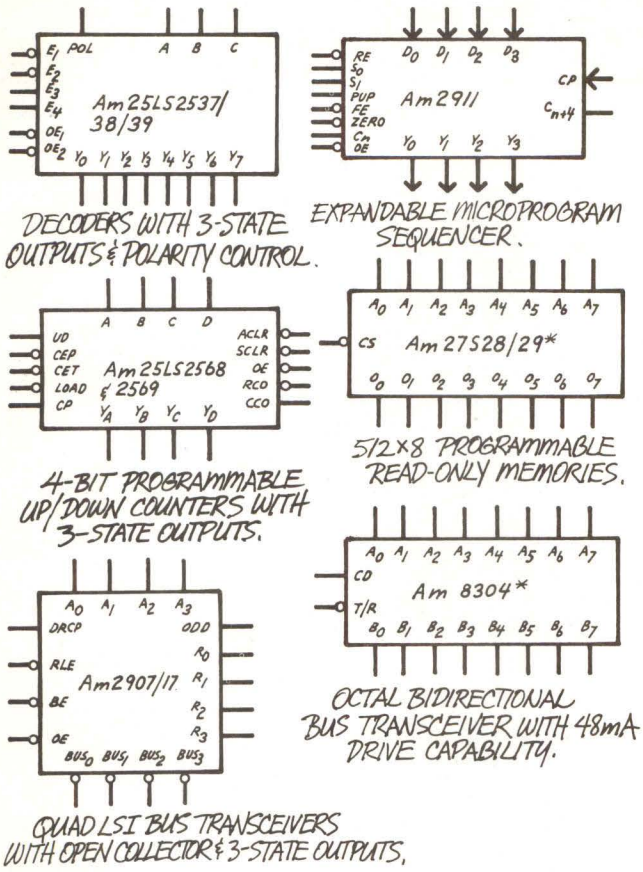
Well now we have new ALU's, counters, sequencers and more.

Fasten your seatbelt.

THE TWENTIES TAKE OFF.

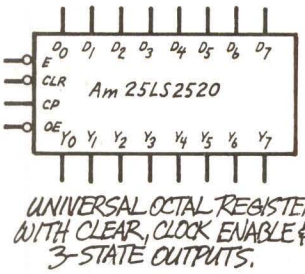


THIRTY-NINE TWENTIES.



* AVAILABLE SOON.

AND A TWENTY-TWO, TOO.



For more pictures, just open your Advanced Micro Devices' Schottky and Low-Power Schottky Data Book. Or ask and we'll send you a beautiful wall chart, suitable for framing.

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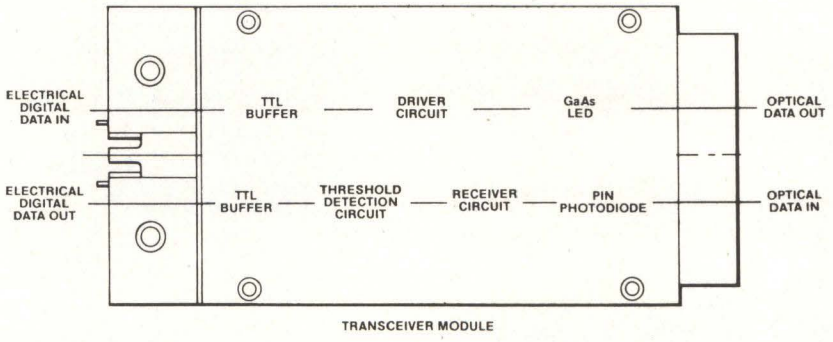
CIRCLE 92 ON INQUIRY CARD



Transceiver package. Modules have infrared emitting GaAs LED light source and PIN photodiode light detector. 10-contact socket on 0.100" (0.25 cm) centers mates with standard PCB header. Link requires microprocessor-type power source with ±7 to 15 V and 5 V

0.008" (0.30-mm) core diameter in a PVC-jacketed flat cable configuration for simultaneous transmission and reception of data.

Typical cable attenuation is 30 dB/km; connector attenuation is 1 dB/mated pair. The TTL compatible link has a data rate of 10M bits/s using biphase coded line format with synchronous or asynchronous transmission. Error rate is 10^{-10} at 10 MHz over a 90-m cable. An external resistor presets data quality threshold to customer requirements. Optical signals are continuously monitored; if signal quality falls below the chosen threshold, the receiver ceases to decode data.

Information security, electrical isolation, and a high degree of immunity to electromagnetic interference are provided. Special cable lengths to fit individual needs can be ordered. Price for complete data link is $695; delivery is 8 weeks ARO.

Circle 402 on Inquiry Card

Online Transaction Control Systems Offer Flexibility in Data Communications

A family of online modular transaction control systems, including data communications control processors, keyboards, displays, printers, and special purpose devices, has been introduced by Burroughs Corp, Burroughs Place, Detroit, MI 48232. Systems may be intermixed to fit a variety of requirements in financial institutions, government offices, school systems, hospitals, sales offices, plants, and warehouses.

TD 500 series system modules for input and display feature choice of 5 or 9" (12.7 or 22.8-cm) CRT screens; each can display 600 char in upper and lower case. Numeric or alphanumeric keyboard, personal identification number (PIN) keyboard, and mag card reader are modular options. PINS or security codes can be accepted without being shown on the screen. Dual buffers allow operator entry of new data while the screen is displaying information received from the central computer system. Particular items can be highlighted on the screen by reverse video feature. Microprocessor based design includes integral automatic confidence testing and fault diagnostics.

AP 100 series auxiliary printers, designed for various financial and commercial applications, operate at 90 char/s, can print single or dual forms, or can be equipped with pin feed for continuous forms printing. Split platen allows independent spacing of dual forms. Printer will accept journals, receipts, multiple-page passbooks, checks, and ledger cards. Two separate forms may be inserted and posted simultaneously and a continuous carbon copy journal record of all transactions may be posted at the same time. Passbook reading feature automatically aligns passbook before printing and ensures that correct passbook has been inserted.

AP 300 is a compact, multipurpose, microprocessor controlled printer station with 90-char/s, bidirectional matrix print mechanism. Printing is in any of four formats, from condensed to expanded, on a char-to-char or block basis. Emphasis is provided by double-width char, switching from one font to another, underscoring, and by reverse images (white on black background blocks).

In addition, data can be right or left justified. Up to 132 char used in repetitive printing, such as headings, prefixes, or suffixes, can be stored. Control code triggers printing, without need to retransmit data repeatedly from central computer. Dual receive buffers operate in flip-flop mode; as one is being loaded from the line, the other is unloading to the printer, ensuring continuous full-speed printer operation.

DC 128/129 systems and communications processors allow the devices to be used in conjunction with company's TV 1800 teller terminals, TT 100 and 600 transaction terminals, and TD 730 and 830 input and display terminals. The independent processors communicate with a central computer at line speeds up to 9600 bits/s. Both offer up to 64k bytes of user program memory. For secondary storage, the DC 128 has separate mag tape cassette stations, while the DC 129 has a 1M-byte capacity mini disc which can be used for data or program storage.

A financial terminal system program software product will be offered, designed to optimize performance in financial teller window operations. For other applications, new modules and processors can be incorporated into any online system operating with Burroughs standard data communications software.

Circle 403 on Inquiry Card

Datapac Service Supports 3270-Type Terminals

A Datapac service, designed to support IBM 3270 compatible CRT terminals, has been announced by Trans-Canada Telephone System's Computer Communications Group, 160 Elgin St, Ottawa, Ontario K1G 3J4, Canada. Datapac is an operational Canada-wide packet switched network pro-

TI 990 USERS: PLUG INTO THE REAL WORLD.

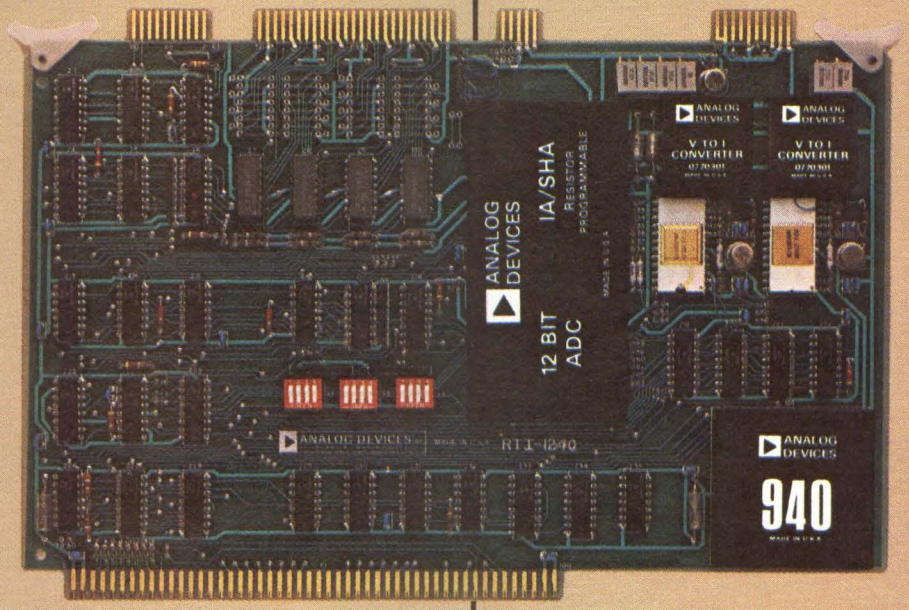
RTI-1240 SERIES SIX COMPLETE "PLUG-IN AND GO" ANALOG I/O SUBSYSTEMS.

Data acquisition made easy. Complete functional, mechanical and electrical compatibility with the Texas Instruments' TM990 family of powerful, 16-bit single board microcomputers. Functions are pre-wired to eliminate time-consuming set-up procedures. All you have to do is connect your analog signals and start collecting data.

Six different boards comprise the RTI-1240 Series—Combination Analog Input/Output boards (RTI-1241) with a choice of either resistor or software Programmable Gain Amplifier; Input only boards (RTI-1240) with either resistor or software PGA; and Output only boards (RTI-1242) with either four or eight Analog outputs plus eight digital logic drivers.

MEMORY MAPPED I/O SIMPLIFIES PROGRAMMING.

Memory-mapping makes a/d conversions as simple as reading data from a single memory location; the result—reduced system software, enhanced throughput, and faster setup.



COST EFFECTIVE SOLUTIONS FOR DATA AQUISITION PROBLEMS.

The Texas Instruments' TM990/100M 16-bit single board microcomputer coupled with the RTI-1240 Series Analog I/O Subsystems offer a complete, cost effective solution to demanding data acquisition requirements. Convenient setup, 12-bit accuracy, and simplified programming all add up to superior performance in the real world at a price you can live with. For example, an RTI-1240 -R analog input subsystem with 16 channels sells for $445, complete and ready to use.

Call or write Analog Devices, Inc. P.O. Box 280, Norwood, MA 02062. Telephone: (617) 329-4700.

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CIRCLE 14 ON INQUIRY CARD


MC6800-QPL
READY
FOR
ACTION!

Motorola MC6800 earns listing on QPL

It's the QPL-listed microprocessor with a fully-compatible hi-rel component family. The MC6800 recently earned JAN approval for listing in the QPL, Part II. Concurrently, DESC completed certification of Motorola's Austin, Texas factory for all its MOS integrated circuits. QPL listing for additional M6800 Family components is being pursued at this time.

Now the MC6800 can be used for defense systems with greater confidence than ever, and with less delay and red tape.

M6800 Family hi-rel series expanding to 38.

M6800 Family hi-rel series components numbered 28 at the end of the first quarter, '78, with additions through the third quarter raising the projected total to 38. A hi-rel version of the MC3870 single-chip microcomputer also is due for availability in the third quarter. All M6800 hi-rel series parts are processed to MIL-Standard-883.

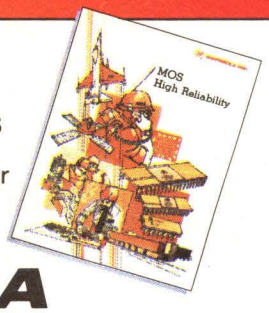
MIL-processed M6800 Family parts include the MC6802-6846 two-chip system, a variety of I/O functions, programmable timer, data link controller, MODEM, IEEE 488 bus interface, and plenty of memories: 1K and 4K Static RAMs, 4K and 16K Dynamic RAMs, EPROM, and 1K, 8K, 16K, and 32K ROMs.

Motorola Hi-Rel Microcomputer Components

Part Number	Function	Status
MC6800BQCS*	Microprocessor	Available
MC6800CQCS*	Microprocessor	Available
MC6802BQCS	Microprocessor with RAM and Clock	Available
MC6846BQCS	MC6802 Combo with ROM, I/O, Timer	Available
MC6802CQCS	Microprocessor with RAM and Clock	Available
MC6846CQCS	MC6802 Combo with ROM, I/O, Timer	Available
MCM6810BJCS	Byte-organized RAM	Available
MCM6810CJCS	Byte-organized RAM	Available
MC6821BQCS	Peripheral Interface Adapter	Available
MC6821CQCS	Peripheral Interface Adapter	Available
MCM6830BJCS	1K ROM	3rd Qtr '78
MCM6830CJCS	1K ROM	3rd Qtr '78
MC6840BTCS	Programmable Timer	Available
MC6840CTCS	Programmable Timer	Available
MC6850BJCS	Asynch Comm Interface Adapter	Available
MC6850CJCS	Asynch Comm Interface Adapter	Available
MC6852BJCS	Synchronous Serial Data Adapter	Available
MC6852CJCS	Synchronous Serial Data Adapter	Available
MC6854BTCS	Advanced Data Link Controller	Available
MC6854CTCS	Advanced Data Link Controller	Available
MC6860BJCS	0—600 bps MODEM	Available
MC6860CJCS	0—600 bps MODEM	Available
MCM2114BVCS	4K Static RAM	Available
MCM2114CVCS	4K Static RAM	Available
MCM4027BECS	4K Dynamic RAM	Available
MCM4027CECS	4K Dynamic RAM	Available
MCM4027BEBS	4K Dynamic RAM	2nd Qtr '78
MCM4027CEBS	4K Dynamic RAM	2nd Qtr '78
MCM4116BECS	16K RAM	3rd Qtr '78
MCM4116CECS	16K RAM	3rd Qtr '78
MCM68316EBJCS	16K ROM	Available
MCM68316ECJCS	16K ROM	Available
MCM68332BJCS	32K ROM	3rd Qtr '78
MCM68332CJCS	32K ROM	3rd Qtr '78
MC68488BQCS	General-Purpose Interface Adapter	3rd Qtr '78
MC68488CQCS	General-Purpose Interface Adapter	3rd Qtr '78
MCM68708BJCS	8K EPROM	Available
MCM68708CJCS	8K EPROM	Available
MC3870BQCS	Single-chip Microcomputer	3rd Qtr '78
MC3870CQCS	Single-chip Microcomputer	3rd Qtr '78

*The military equivalent part numbers for the MC6800 are JM38510/40001BQC and JM38510/40001CQC.

Our MOS high-reliability story is explained in a brochure covering wafer fabrication, assembly, testing, reliability, and how to order our hi-rel MOS products. For your copy, please circle the reader service number or write to Motorola Semiconductor Group, P.O. Box 20912, Phoenix, AZ 85036.



MOTOROLA

Semiconductor Group

CIRCLE 15 ON INQUIRY CARD

viding high speed data transmission. The service, called Datapac 3303, will enable IBM 3270 terminals and emulators such as CCG's VUCOM 2 terminals operating under binary synchronous line protocol to communicate with host computers over the network. IBM 3270 terminals and equivalents are widely used in financial and transportation industries, as well as in government, with approximately 10k units installed throughout Canada.

Datapac 3303 will be a NIM (Network Interface Machine) based service using Northern Telecom SL-10 line processors. These will poll the terminal controllers on an online basis over multipoint facilities using standard 3270 BSC line protocol. At the other end, host computers will access the network via Datapac 3000 (SNAP) service. In addition, a DMEP (Datapac Modified Emulation Program) software package will be available for host support.

Rates for the service will be announced later this summer. Commercial service is expected by the end of 1978.

TYMNET-Datapac Connection Tariff Is Approved

The Canadian Radio-Television and Telecommunications Commission (CRTC) has approved the tariff for interconnecting Canada's Datapac network with TYMNET, the U.S. public packet network. TYMNET has been operationally connected to Datapac for two months via the X.25 interface protocol.

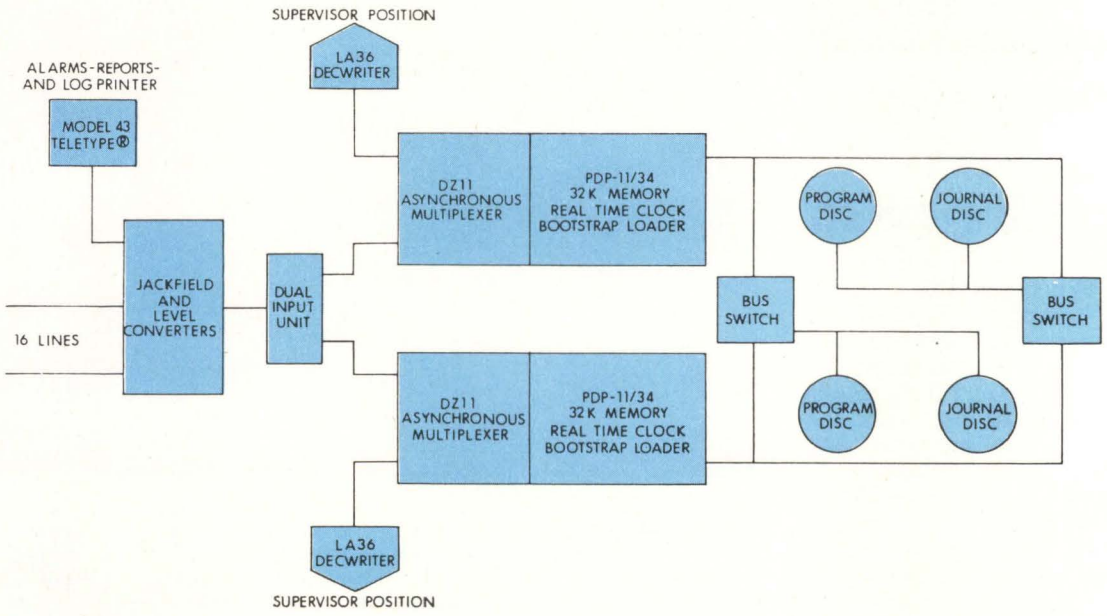
Datapac is providing dial access for 110- to 300-baud asynchronous half-duplex ASCII terminals, and additionally offers 1200-baud service using dedicated access ports.

Currently Tymnet, Inc, 10261 Bubb Rd, Cupertino, CA 95014 provides access to the 170 host computers on TYMNET from 57 Canadian cities. Conversely, access to host computers in Canada is available through TYMNET from 85 cities in the United States. TYMNET nodes allow dial-up access at speeds from 110 to 1200 baud. 2000- to 4800-baud synchronous speeds can also be used. Access charges from the 15 largest Canadian cities to TYMNET hosts range from $4 to $6/hour.

Fully Redundant Message Switching System Provides High Reliability

SCAMS-DX is a fully redundant, computerized, store and forward message switching system designed for use in communications networks where high reliability is a requirement. The system adds several features to the basic SCAMS switch introduced earlier this year by C & W Incotel, Ltd, One Penn Plaza, New York, NY 10001.

The system allows backup discs to operate with the primary system to provide duplicates of the transactions being carried out, as well as a dual record of the in-transit messages. Central processors in the configuration are Digital Equipment PDP-11/34s. Either fixed or moving head discs are available. Other options are mag tape, line printers, and a variety of line interfaces. All systems include hardware, software, installation, training, and documentation.



Equipment configuration for SCAMS-DX system. Program discs handle in-transit storage, program storage, and ledger; journal discs take care of journal and retrieval storage, overflow storage. System will accommodate up to 16 asynchronous circuits operating at different speeds or codes, and assigned in any combination of circuit types—full duplex, half duplex (83B polling system), simplex, and telex

Circle 404 on Inquiry Card □

WHO DOES THIS PRINTER THINK IT'S KIDDING?

THE M-200 MATRIX PRINTER

If the M-200 wants to go around acting like a line printer, we're not about to stop it.

And that's exactly how it does behave, cranking out an effortless 200 lines per minute, average throughput.

But the truth is, the M-200 is a serial printer. Which should certainly be obvious from the extremely reasonable purchase price of about $2000. (In OEM quantities.)

And so, if the M-200 delivers performance that can fool you, blame it on its design features.

Like our revolutionary 14-wire, dual-column print head, for instance. The design combines the flexibility of a single head with the speed and long life of multiple heads. (You can expect more than a year's use out of the head.)

Any operator can change the head easily.

And, like all products from The Printer Company, it's a dependable workhorse. Made even more so by its optional self-diagnostic system.

If something needs attention, the system tells you if you can tend to it yourself. Or if you can't, you know what to tell the serviceman. That can save him a trip, saving you down time and money.

And that's the inside story of the M-200. Acting like something it's not? Maybe. But since its delusions are all in your favor, why complain?

THE PRINTER COMPANY

Dataproducts

Call or write for your nearest Sales Office or Distributor. 6219 DeSoto Ave., Woodland Hills, Ca. 91365. Tel: (213) 887-8451 Telex: 67-4734 • Darmstaedter Landstrasse 199, Frankfurt, W. Germany. Tel: 681-034, Telex: 841-416344.

370 Compatible System Based on Bus-Central Multiprocessor Architecture

System/400 offers a low cost hardware solution to a chronic software problem—the lack of versatile software for the small computer user—by combining low cost minicomputer architecture with mainframe power and full compatibility with IBM System/370 software and I/O. Providing users with up to 16M bytes of memory, the microprocessor based system, developed by National Semiconductor Corp, Computer Products Group, 2900 Semiconductor Dr, Santa Clara, CA 95051, runs DOS/VS and VM/370 and uses advanced LSI components to ensure maximum performance and low cost.

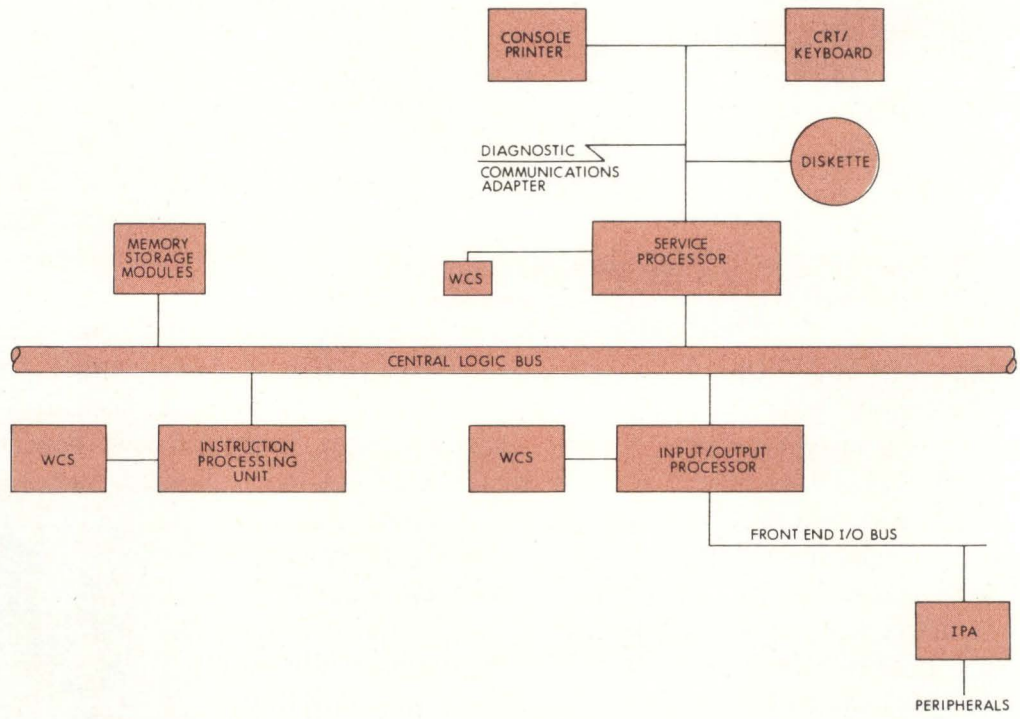
Bus-central functionally distributed multiprocessor architecture is used to provide flexibility, expandability, and economy. A time-sliced synchronous technique enables the system to achieve the necessary performance level and to maintain /370 compatibility. Functional units attach to the central logic bus capable of data rates to 20M bytes/s, and conduct all communications across it.

Attaching to the central logic bus are three types of processors and main memory. All processors are fully microprogrammed and feature large capacity writable control storage based on high speed static MOS RAMs. Main memory is composed of 256k-byte memory storage modules, each containing independent error checking and correction logic (ECC), and storage protection.

Emulation of the entire model-independent System/370 instruction set is performed by the instruction processing unit (IPU), a 32-bit microcomputer based on the IDM2901A. A microprogram that executes IBM instructions as on an IBM machine is loaded into its writable control storage.

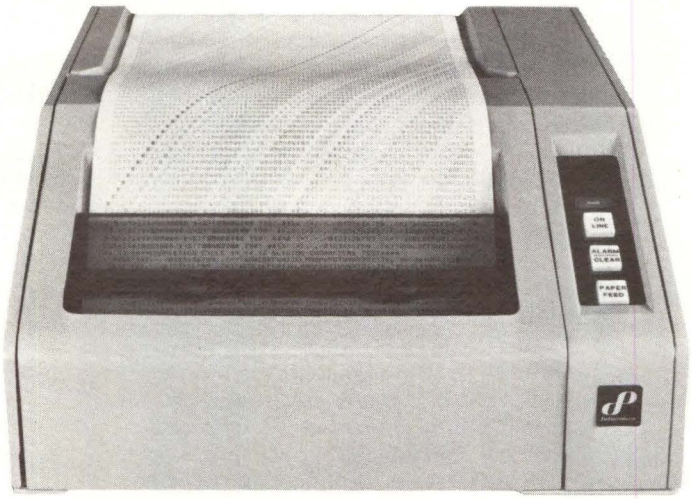
I/O functions are accomplished through use of input/output processors (IOPS) that attach to the central logic bus. Like the IPU, these are 32-bit wide microcomputers, completely controlled by microprogramming. Each IOP controls an 8-bit asynchronous frontend I/O bus with maximum data rate of 1.5M bytes/s to which a number of channel and device interfaces can be attached. Microprograms in IOP writable control storage emulate various channel command words that are used to control peripherals on System/370.

A service processor (SVP) provides system console, control, and diagnostic functions. This processor, based on



A bus-central multiprocessor system in which all functions communicate through the central logic bus, National Semiconductor's System/400 uses bit-slice microprocessor design to achieve low cost plus IBM System/370 compatibility

KEEPS QUIET. WORKS HARD. FOR VERY LITTLE.



THE T-80 THERMAL PRINTER

Our T-80 Receive Only printer is a quiet, unassuming sort. Doesn't take up much room on the desk. Doesn't make a racket while it's doing its work.

And it doesn't require a lot of money before it'll go to work. In fact, the T-80 runs less than $900 in OEM quantities. And it continues to save you money with its low cost of ownership.

On top of all this, the T-80 prints fast. 80 CPS fast. Which is nearly three times faster than most other thermal printers.

All these qualities — low price, impressive speed, high quality, and quiet operation — have combined to make the T-80 an absolute natural for applications that demand silence. Hospitals. Open office situations. Testing and instrumentation.

And the T-80 is the logical supplement to your CRT if you want occasional hard copy printouts.

Now, you don't have to buy a T-80 RO to get T-80 performance. The basic T-80 mechanism, with the same unique operator-replaceable print head and driver electronics, is available as a module: the T-80 M.

So, it's up to you. Buy the complete T-80 RO, ready-to-run. Or just take the T-80 M mechanism and design your own printer around it.

Either way, you save money, and the T-80 goes quickly and quietly about its business.

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the Series/80 microcomputer system, emulates /370 console functions, supporting a diskette drive that is used to store microprograms for all processors in the system, a console CRT and keyboard, a diagnostic communications adapter, and an optional console printer.

Memory storage modules (MSMs) are built using 16k dynamic MOS RAMs, and provide a full 256k bytes of memory on a single PC board. Each MSM contains internal single-bit error correction and double-bit error detection as well as /370 compatible storage protection capability. Improved system performance is achieved through the independent operation of each module, which permits separate operations to occur in each module attached to the central logic bus.

A typically configured machine will provide throughput similar to that of the System/370, model 145. Instruction execution is performed at approximately 1.5 times the speed of the 138; however, independent IOPs in the system do not degrade instruction execution rates as do 138 channels and I/O adapters. As a result, total system performance is not adversely affected in I/O intensive applications.

Modular architecture provides versatility in configuration—from a basic unit with 256k bytes of memory and a single IOP shared between all devices, the system can expand incrementally to 16M bytes of memory and 12 IOPs. These increases can be performed in the field.

Various frontend adapters attached to the IOPs offer alternative ways to attach peripheral devices; each IOP can interface to peripherals either through use of standard IBM channel protocol or through integrated peripheral adapters. With IBM standard channel-to-control unit interface adapter, the system emulates /370 I/O channels and can interface with standard IBM or PCM peripheral and control unit. For economy, attachment of minicomputer peripherals is accommodated through various integrated peripheral adapters. Implemented with device-specific frontend adapters and IOP microprograms, these attachments eliminate the need for channel interface and device controller. Microprograms in IOP writable control storage emulate both IBM channel and device controller for the equivalent IBM device.

Interactive Transaction Processing System Eases Program Development

TRAX™, a comprehensive minicomputer based system for interactive transaction processing, runs on PDP-11/34, -11/60, and -11/70 computers and uses VT62 video display application terminals. Designed by Digital Equipment Corp's Distributed Data Processing Group, Maynard, MA 01754, the software incorporates advanced development tools and data protection features. It provides a complete basis for customer implementation of a transaction processing application without system level programming, and is claimed to reduce development time for applications programs by more than 50%. Built-in communications options enable several systems to exchange data and process inquiries; systems can also communicate with mainframe systems.

VT62 display terminal possesses screen formatting and error detection capabilities to ease operation and allow early correction of most keying errors. Data are transmitted through point-to-point or multidrop lines in block mode to reduce processor overhead. Up to 16 terminals can be simultaneously active on a PDP-11/34 TRAX system; up to 64 terminals on an -11/70 TRAX system. An integral microprocessor performs instant error checks, relieving the system of responsibility for data validation. Users are guided through transactions with menu selection and function keys that avoid use of conventional computer commands. Reverse video, automatic cursor positioning, and left and right justification simplify data entry progression.

The software includes extensive file organization and record access services, restart/recovery, data protection, and forms handling capability. Applications programs are written in small structured modules using either COBOL or BASIC-Plus-2 languages; terminal screens are easily formatted using English-like ATL forms language. Programs are both created and tested interactively.

Small application program modules execute rapidly and require much less memory than large programs. Data management software can be resident and is shared by all users for fast execution while software caching of applications programs reduces disc accesses in addition to increasing throughput.

Automatic restart/recovery avoids system reloading or reentry of transactions after power failures or hardware or software malfunctions. Disc files are protected during media or equipment failure through the use of "journaling"—automatic duplication of data files up to the last completed transaction on a backup storage device such as another disc or magnetic tape.

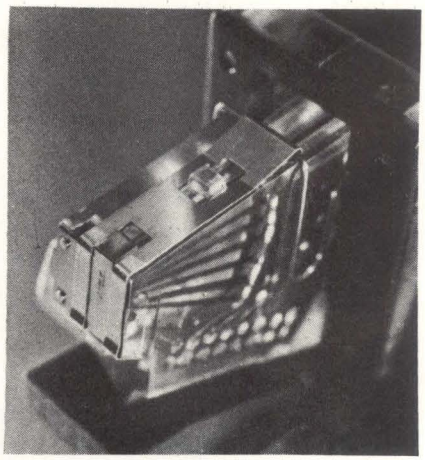
A staging feature delays update of records until transactions are complete, so that partial transactions aborted by either terminal user or system malfunction do not alter stored records. Record locking capability prevents simultaneous attempts to update records, but does not limit user access by locking large data blocks or the entire data file.

A typical PDP-11/34 TRAX system configured with eight terminals, up to 256k bytes of memory, 56M bytes of disc storage, and a 9-track tape drive, will sell for $131,840. A PDP-11/70 TRAX system with 20 terminals, 384k bytes of memory, 134M bytes of disc storage, and 9-track tape unit has a price of $211,420.

Circle 170 on Inquiry Card

Microprocessor-Controlled Ink Jet Printer Terminal Achieves 270-Char/s Speed

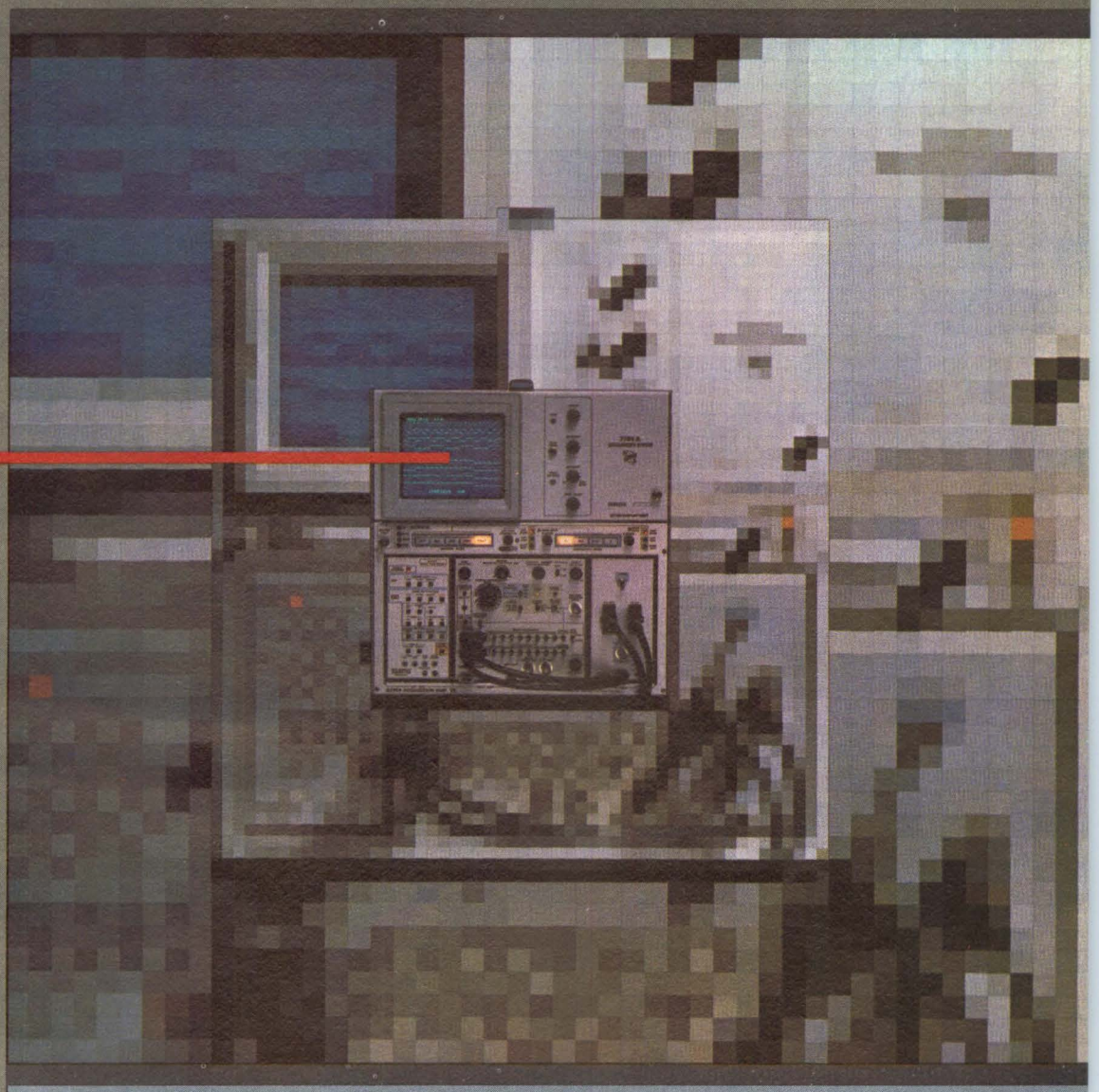
A high speed version of the silent ink-jet PT 80 printer terminal (see *Computer Design*, Aug 1977, pp 34, 36) is bidirectional in operation and microprocessor controlled. Developed by Siemens Corp, 186 Wood Ave S, Iselin, NJ 08830, the printer operates



Ink-jet printing head in Siemen's PT-80i printer terminal achieves speeds of 270-char/s under microprocessor control

TEKTRONIX thinks your logic analyzer should be as versatile as you are

So ours let you sample with *speed.* With *resolution.* With *confidence.*



Sample with confidence: up to 100 MHZ at 15 ns resolution

Versatility — it's the key to effective, efficient digital design. You've got to be versatile enough to make a variety of measurements every day. And so you need an equally versatile logic analyzer.

Speed is one important measure of logic analyzer versatility, because, especially in asynchronous measurements (say, chip to chip transactions), *faster is better.* Better because high speed means high resolution. And you've got to *see* information accurately in order to *measure* it accurately.

Use Tektronix Logic Analyzers for asynchronous measurements at 20, 50, even 100 MHz — with 15 ns resolution. You can also sample synchronously up to 50 MHz (not all logic analyzers provide synchronous *and* asynchronous operation).

Tektronix speed and resolution mean *confidence.* In the measurements you make...and in the job you do. **High speed data acquisition: it helps make our Logic Analyzers versatile. So you can do today's job and tomorrow's. So you can change applications without changing your logic analyzer.**

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TEKTRONIX LOGIC ANALYZERS THE VERSATILE ONES

Sperry Univac minis are doing

In Portland, Oregon, Sperry Univac minis help the Police Bureau come to the rescue hundreds of times a day.

Because Boeing Computer Services has computerized all of Portland's emergency services with Sperry Univac Series 77 minis.

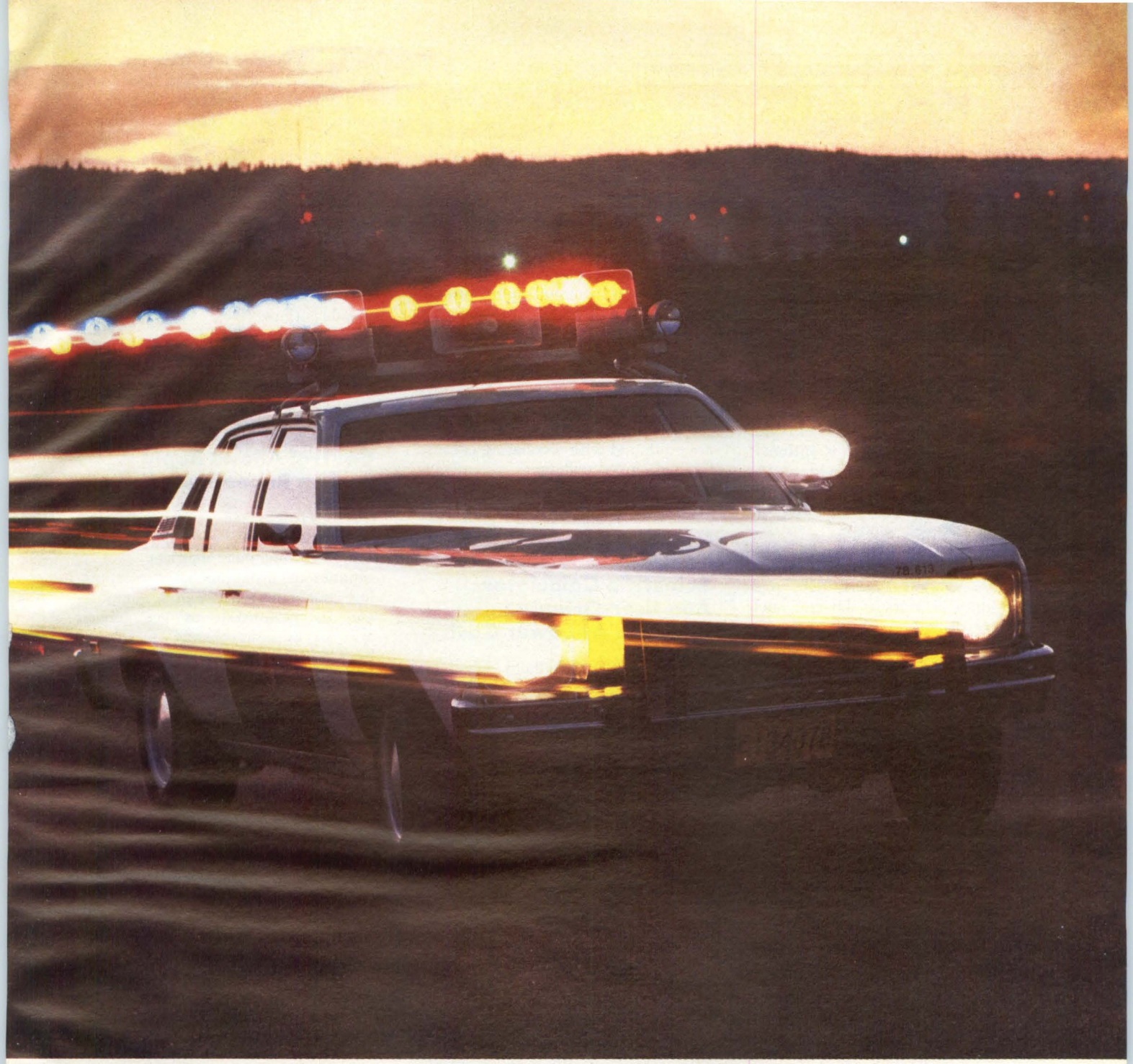
Now when a citizen reports a crime, our minis verify the address. Examine the surrounding area for similar calls, hazards, and temporary situations (such as streets under repair). And suggest which units should respond to the call.

This futuristic system coordinates dispatchers and officers and keeps them constantly updated. Much of the paperwork required of field officers is eliminated. And the data base it generates is used for uniform crime reporting and resource allocation.

Boeing Computer Services has found that our minis are cost effective and can handle the job efficiently and with real-time speed.

The Sperry Univac minis used in Portland are just part of our complete family of minis. One and all of them are supported by our powerful software.

If you have a system application, we undoubtedly have a mini that's just right for it. Whether it be business data process-



alarming things in Portland.

ing, scientific, instrument control, or data communications.

For more information, write to us at Sperry Univac Mini-Computer Operations, 2722 Michelson Drive, Irvine, California 92713. Or call (714) 833-2400.

In Europe, write Headquarters, Mini-Computer Operations, London NW10 8LS, England.

We'd like to hear from you. Even if your system application isn't as arresting as the one in Portland.

SPERRY UNIVAC

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CIRCLE 20 ON INQUIRY CARD

at 270 char/s using microprocessor control to take advantage of the ink-jet printhead's inherent capability.

In operation, the printing head moves bidirectionally and in relation to the text to be printed on the following line. The shortest path of movement for the printing head across a given line is the result. The printing head, which includes the 12 ink-jet elements, is capable of printing 127 characters in a 12 x 9 dot matrix from either one of two character generators and is free to choose character elements for printing logos or symbols. Italics (left or right) is optional; continuous underline is standard.

The 8085 microprocessor used for control provides, in addition to the standard parallel interface, an extended system information bus interface. This allows for external connection of network selectors, data sets, and additional storage devices, such as floppy discs.

Circle 171 on Inquiry Card

Microfilm Equipment Incorporates µProcessor For Online Operation

Computer output microfilm products introduced by DatagraphiX, Inc, PO Box 82449, San Diego, CA 92138 include a microfiche recorder, reader/printer, and a duplicator. Disc systems providing 10M bytes of storage for Mini Autocom Recorders were also announced.

Designed to provide intelligent on-line operation, the On-Line Autocom™ II uses a 32k-byte microcomputer system and interfaces directly with IBM System/360, /370, or 303X computers. The internal microcomputer enables the system to perform its own data reformatting, allowing data to be processed into fully titled and indexed microfiche at up to 12k lines/min. A fully integrated 3740 compatible diskette drive, remote and local power control, and choice of operating mode further extend its versatility.

Model 1500 DL microfiche printer/reader uses integral dual lenses to allow convenient switching between two different magnifications. The unit provides a three-quarter size image of COM-generated or source document microfiche data pages on an 8.6 x 12" (21.8 x 30.5-cm) screen, and is available with 24X, 42X, 48X, or 72X magnification. Its microfiche platen rotates 90 deg to accommodate comic or cine frame orientations. The roll-fed printer delivers copies on electrostatic paper in approximately 10 s.

Microprocessor controlled Datamaster duplicators produce up to 1500 fiche/h, communicating production routines directly to the operator through a message display panel and providing a power-guard memory system for storing job setup instructions. Model 100 copies from cut fiche masters; 200 works from both roll film and cut fiche masters. Models 150 and 250 are equipped with a collating carousel for high speed collation.

Circle 172 on Inquiry Card

Scientific Calculators Add User-Oriented Features At Lower Cost

Three scientific handheld calculators offer large LED displays with automatically inserted commas, temporary display of the 10-digit mantissa, and a diagnostic error code system. Introduced by the Corvallis Div of Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, the HP-31E, -32E, and -33E replace many of the company's present low end calculator line.

LED displays on the calculators are designed to allow easier and more accurate reading. For further ease of use, each calculator automatically inserts commas in displayed numbers as they are needed. A mantissa function on the keyboard allows the user to temporarily see the 10 significant digits of precision carried internally, then returns to the original display format. A "low" battery indicator light on the display warns the operator that the batteries are low in time to recharge. A diagnostic error code system informs the operator of mistakes through a code number.

Priced at $60, the HP-31E performs standard arithmetic, logarithmic, and trigonometric functions, and provides fixed and scientific display modes, and rectangular/polar, degree/radian, inch/millimeter, Farenheit/Centigrade, and pound-mass/kilogram conversion keys. It has the RPN logic system with 4-register stack and four addressable storage registers. The HP-32E, at $80, incorporates all features and functions of the -31E with an added engineering display mode, hyperbolic functions and their inverses, and collection of statistical functions, including linear regression, correlation coefficient, x and y estimates, normal and inverse normal distribution, and factorial. There are 15 addressable storage registers. HP-33E, a $100 calculator, has all features of the -32E, except hyperbolics, metrics, and certain statistical functions, and offers 49 lines of fully merged keystroke memory. Of particular interest is the calculator's capacity for three levels of subroutines.

Circle 173 on Inquiry Card

Intelligent Matrix Control Allows Rapid System Reconfiguration

IMC 317 is a microprocessor based intelligent matrix control for 3916 computer channel matrices that is capable of instantaneously rearranging connections between a computer and its peripherals as emergencies arise or as tasks change. Developed by T-Bar Inc, 141 Danbury Rd, Wilton, CT 06897 to overcome the increasingly difficult problem of timely response to the demands of operating a complex multiprocessor system, the control is the first of a series of facilitating equipment which should develop into an automatic data management system.

Basic purpose of the control, applied to the company's 3916 matrix switch, is to provide a simple method of changing or interchanging the computer-to-peripheral connections of two or more computerized application systems to restore critical service or to rearrange an application configuration to meet changes in tasks or load demands. A command to interchange the system, applied manually or automatically, causes the control to analyze the channel/peripheral connections to determine which matrix crosspoints are involved in the interchange. It then interchanges the appropriate connections and changes the system records to properly identify and display the system's new status. Average time required to complete the transfer of as many as 40 peripherals is estimated at under 3.5 s; operator response time without the control could be as much as 30 min.

Consisting of a microprocessor with dual diskettes for normal control and inquiry operations, the control includes a complete spare micro with dual diskettes and switchover equipment. Provision is made for a cus-

From a single CPU board

to a half million word super computer

That's the selection you get from ROLM's AN/UYK-19 family. It's the most complete line of Mil-Spec computers in the industry. And every piece is backed by extensive, updated, upward compatible software.

Delivery? 30 days or less because they're all standard products in continuous production. Plus they follow a modular concept for interchangeability, compatibility and upgrading.

Rolm completes the package with full nomenclature and an integrated line of both military and commercial peripherals.

In just seven years we've been able to put together a family plan that lowers your programing costs, reduces hardware costs, cuts out your risk and gives you quicker reaction time.

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CIRCLE 21 ON INQUIRY CARD

tomer-owned video terminal and 55-line/min printer to be connected. Abbreviated ASCII control commands may be initiated from the terminal's keyboard, a second computer, or via telephone lines from a remote control point. Master control commands allow the operator to change or interchange the connection of any or all peripheral devices from one computer system to another, manually or by program.

To supplement the switching commands, interrogation commands permit rapid identification of all peripherals attached to each CPU or attached to an application system. The matrix control responds to these commands with information that is displayed on the CRT as a matrix presentation of each matrix switch in the system. With this capability, the computer manager can request that a device classification be listed, and then assign available peripherals, as shown in the listing, without affecting performance of the remainder of the system.

The control matrix interfaces not only with 3915/6 peripheral matrix switches but with peripheral switches serving most mainframe and minicomputer hardware. As more functions are programmed onto simple memory devices, more routine control and instructions to overcome failure can be automatically controlled, until the equipment will have the ability to make decisions by interrogating its own stored data. Present equipment with future additions will make it possible to automatically manage not only the computer facility, but also the data communications system which transmits the data.

Circle 174 on Inquiry Card

Communications-Oriented Computer Systems Offer Supermini Performance

Five 3200 series, 32-bit virtual memory systems offer processing speed and power of the IBM System/370, 138 in a minicomputer package. The communications oriented machines, designed by National CSS, Inc, 542 Westport Ave, Norwalk, CT 06851, are field upgradeable, compatible with each other, and equipped with their own performance monitors.

Systems provide three simultaneous operating modes: online interactive, remote job entry, and batch. Up to 32 users can be concurrently online to a single-CPU system. Using multiple network facilities, the system can be concurrently in communication with an inhouse/370, the company's timesharing system, and another 3200. Connection may be made via the company's communication network, independent communications, or a customer's private network.

Basic structure of the system includes a CPU, main storage, and online I/O devices. The CPU operates on 32-bit words using dynamic address translation. It contains 16 general purpose registers, 16 control registers, and 4 floating point registers. Built using high speed Schottky TTL circuitry, it provides a 275-μs microcycle time.

Main storage is formed of up to 2M bytes of MOS memory elements. Error checking and correction and storage protection are provided. An 8k x 80-bit ROM serves as the control storage.

As many as 256 devices are supported simultaneously by the single byte-multiplexer channel in byte mode; in burst mode the channel accommodates 1 high speed device. Three selector channels provide 1.3M-byte/s throughput.

The /370 compatible computers run under the VPS operating system which manages CPU, storage, and I/O devices to make these resources available to many users at the same time. VPS consists of a virtual control program, which controls machine resources creating a virtual machine, and virtual user environment, which serves as the conversational interface that makes the machine suitable for direct problem solving. Operating system provides networking capabilities that include spooling, high and low speed terminal support, intermachine communications, and packet-switched software. The system supports COBOL, assembler, PL/1, BASIC, FORTRAN, and APL languages.

Circle 175 on Inquiry Card

Small Business Computer Family Expansion Provides Interactive COBOL

Additions to the Commercial Systems line announced by Data General Corp, Route 9, Westboro, MA 01581, the CS/20 and CS/60 provide standalone computing capability for small and large business firms. Both are compatible with program logic and file handling with other members of the CS/40 family.

CS/20, a single-station unit, can function either as a standalone business computer, or as an intelligent data entry system. Programming flexibility and efficiency are provided through interactive implementation of ANSI (American National Standards Institute) '74 COBOL with screen handling extensions.

Design features include micro-NOVA™ processor with 64k-byte main memory, mounted within the display housing; a 1920-char u/lc display unit, in a case which tilts or swivels for operator convenience; and an independently movable keyboard. The system is configured in a work table in which are located the power supplies, as well as up to four 315k-byte diskette drives. To round out the system there is a choice of 60- or 180-char/s, or a 240- or 300-line/min printer, and a standard communications interface.

CS/60 system series includes 3 models, based on an ECLIPSE® processor, ranging from C-3, a 64k-byte machine capable of supporting 4 active terminals and from 30M to 80M bytes of cartridge disc memory, to C-6, with up to 256k bytes main memory, 12 active displays, 760M bytes of disc pack or cartridge capacity, 2 simultaneous char or line printers, and HASP II workstation support in addition to RJE80 communication capability.

Circle 176 on Inquiry Card

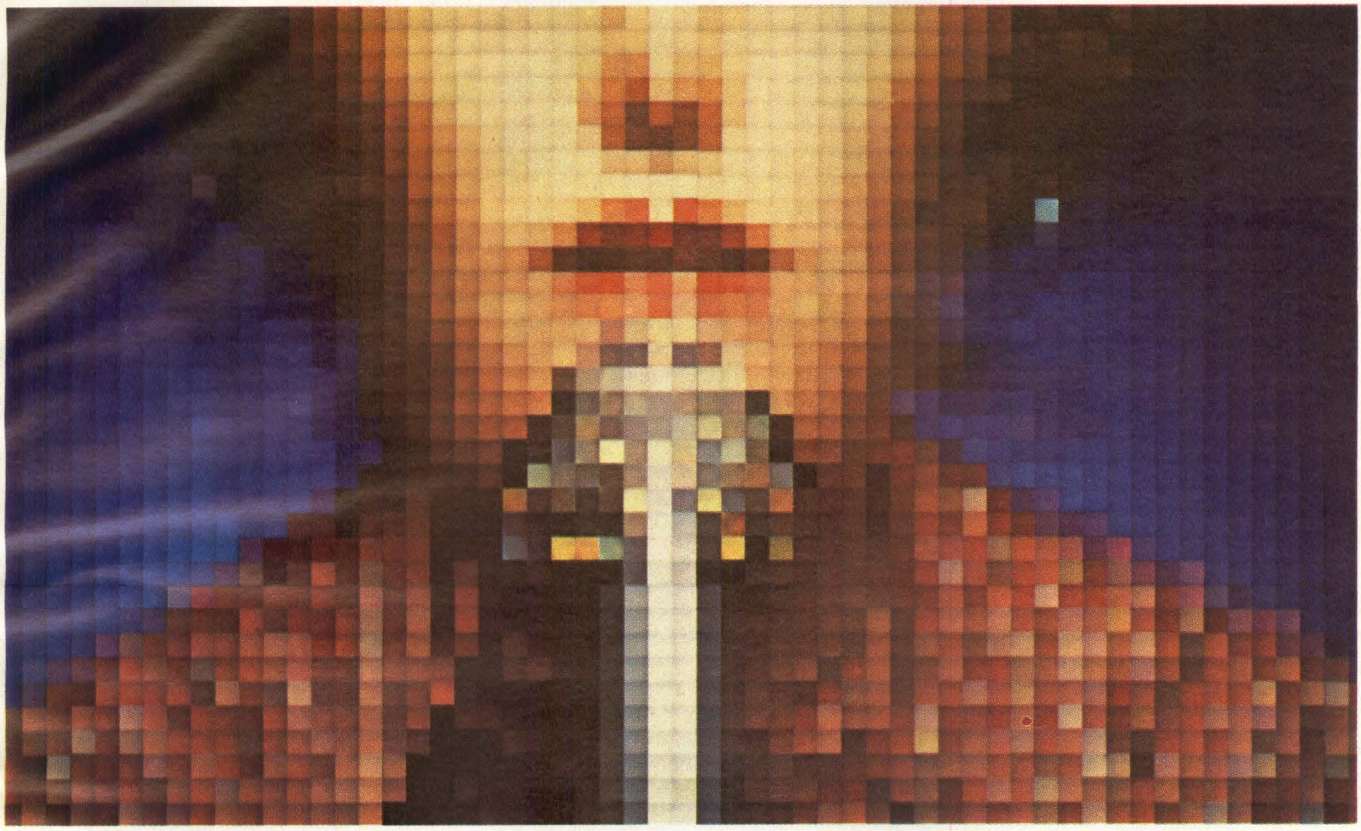
Portable µProcessor Based Terminals Allow Remote Data Entry

Handheld data entry terminals provide operator prompts, internal microprocessors for programmability, and communication with a central processor for timely portable data collection. Varying in features, the three units should find extensive applications in ordering and inventory control, as well as in material and process management.

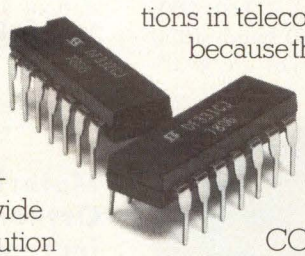
Programmable Data System

Totally programmable, the handheld 101 Portable Data System developed by Norand Corp, Cedar Rapids, IA 52406 can provide a 2-way link with central computers. Unlike other order-entry terminals that only collect and

Spread the word. Siliconix announces CODEC.



Siliconix introduces the ultimate man/machine interface: CODEC. Our DF331 coder is a high-speed serial output A/D converter — a complete subsystem-on-a-chip. Its counterpart, the DF332 decoder, converts high-speed digital bit streams into analog signals. Both devices operate logarithmically, giving our CODEC a wide dynamic range: 12-bit resolution (±1 bit) for low-level signals, and 8-bit accuracy for high-level signals.



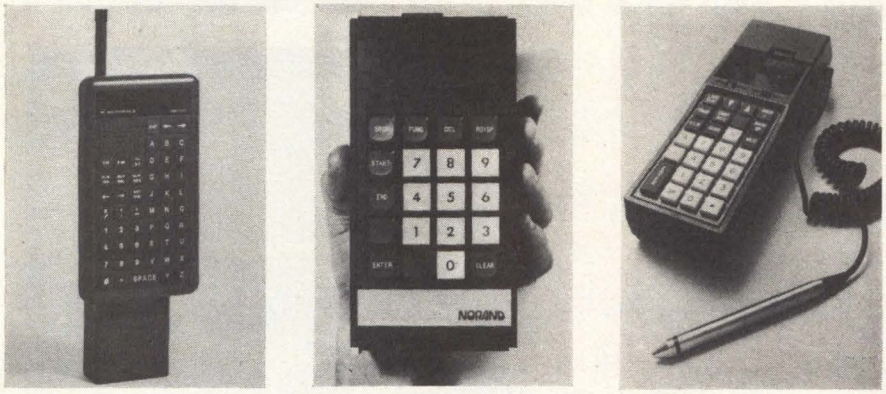
Designing with Siliconix' CODEC is a cost-effective solution to the problem of vocal interface with computers. Siliconix CODEC minimizes external component requirements and system costs: serial output and sample-and-hold circuitry are all on-board. And CODECs will have many applications in telecommunications because they meet all D3 specifications and are compatible with the μ255 law for companding. A key CODEC specification: signal to distortion is 28dB (Pin=−45dBmO) max.

Our CODEC set continues the Siliconix tradition of providing products that link the analog world to digital systems. We've been manufacturing monolithic analog-to-digital converters for five years. And we're currently supplying the instrumentation industry with the latest in technological advances, such as our LD120/LD121 series 4½ digit A/D converters, high-speed analog switches, and logic compatible VMOS transistors. Experience and expertise make Siliconix the logical source for CODECs. Spread the word. For details, call or write Siliconix, 2201 Laurelwood Road, Santa Clara, CA 95054; (408) 988-8000.

Siliconix

The Siliconix connection:
Innovative products linking the analog world to digital systems.

CIRCLE 22 ON INQUIRY CARD



Portable data terminals incorporate microprocessors to provide direct data entry to a central computer. With a 53-key alphanumeric keyboard and 16-char LED display Motorola's RDX 1000 (left) provides virtually all capabilities of fixed point CRT terminals; Norand's fully programmable device (center) has an easy-to-use 20-key keyboard and alphanumeric display. The MSI/88 (right) with segmented memory and programmable accumulator provides a 16-char LED display and optional bar code wand scanning capability

send information, the unit also receives it. Data are stored in solid-state memory that can range in capacity from 16k to 64k characters.

The microprocessor based unit provides 2k x 8 P/ROM program storage. Programs can be customized to match needs of the user, avoiding the need to alter business procedures to comply with system capabilities.

Data are entered via a 20-key keyboard and can be reviewed on the 12-char alphanumeric display. The display also provides operator prompts which guide the operator through the program sequences, making training requirements minimal. Operating from removable, rechargeable NiCad batteries, the unit links to a central computer via any telephone.

Circle 177 on Inquiry Card

Segmented Memory Terminal

In addition to a segmented memory that makes it the equivalent of several terminals in one, the /188 from MSI Data Corp, 340 Lischer Ave, Costa Mesa, CA 92626 has a programmable accumulator and memory capacity ranging from 24k to 48k characters. Other features are a 16-digit LED display, bar code wand scanning capability for universal product code and the company's code, and battery-powered operation.

The unit's memory can be divided into as many as nine separate parts of varying sizes. Each segment can be treated independently of the others, thus the terminal can handle different problems or departments without data loss or damage. Data transmission, editing, erasure, or searching can be accomplished on a segment basis by means of a selection or page key.

Incorporation of a programmable accumulator provides audit control of entered data. This accumulator is useful in such applications as accounts receivable, collection of inventory data, or in compiling departmental financial totals. Up to nine accumulators, one per memory page, with 10-digits plus sign each, are program selectable to accumulate only specific quantities entered.

Communication of 8-bit ASCII data code occurs at data rates of 110, 200, 300, 600, 1200, and 1350 baud; 1050 baud is optional. Interfaces are available for acoustic transmission over the voice-switched network, for MDAA transmission, or via modem.

Circle 178 on Inquiry Card

Wireless 2-way RDX 1000 terminals from Motorola are environmentally protected to allow use in industrial or outdoor environments. A 2-W transmitter and receiver permits 2-way communication with central computer

Wireless Data Terminal

A portable 2-way system that is compatible with the IBM 3270 Information Display System, the RDX 1000 Portable Data Terminal System consists of RDX 1000 terminals, duplex fm radio base station, and RDX 1100 control unit. Terminals require no phone lines, interconnect cabling, or external power source.

Developed by Motorola Inc, Communications Div, 1301 Algonquin Rd, Schaumberg, IL 60196, the terminal is a microprocessor based unit with built-in memory that has a 53-key alphanumeric keyboard, 480-char display buffer, and a 16-char LED display that provides operator prompts. Designed for rugged industrial use, the terminals are environmentally protected (to EIA 316 spec) and can be used indoors or out.

A 2-W fm transmitter and receiver allows 2-way wireless communication to the central computer system. This is achieved via two lines: an fm radio link that allows 1200-bit/s transmission between the portable terminals and a continuous duty, duplex fm radio base station operating in the UHF band; and a land line link between the RDX 1100 control unit and IBM system that operates at up to 9600 bits/s. Interfaced directly to the base station, a control unit supports up to 32 portable terminals.

Circle 179 on Inquiry Card

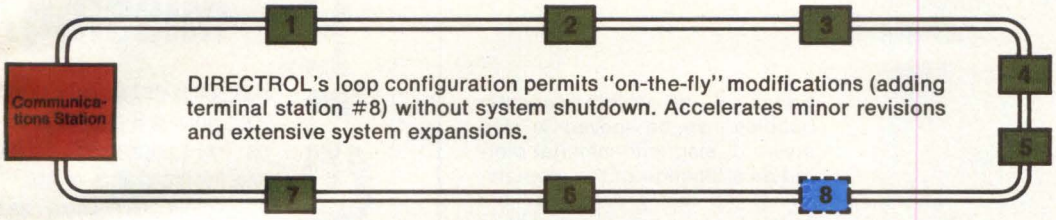
Materials With Orthorhombic Asymmetry Increase Bubble Speed

The speed at which magnetic bubbles can be moved is an important feature when these bubbles are to be used in memory elements for computers. Materials in which the bubble speed is 30 to 100 times faster than in previously known materials have been developed by researchers at Philips Research Laboratories in Eindhoven, The Netherlands.

Bubbles may be present in thin anisotropic layers of a magnetic material in which the preferred direction of magnetization is at right angles to the plane of the layer. If such a

New DIRECTROL™ Multiplexer. Signaling new directions for industrial control.

Cutler-Hammer's new DIRECTROL . . . finally, here's a multiplexer that's practical for industrial control application. DIRECTROL achieves startling advantages in project simplification, system productivity and plant versatility.



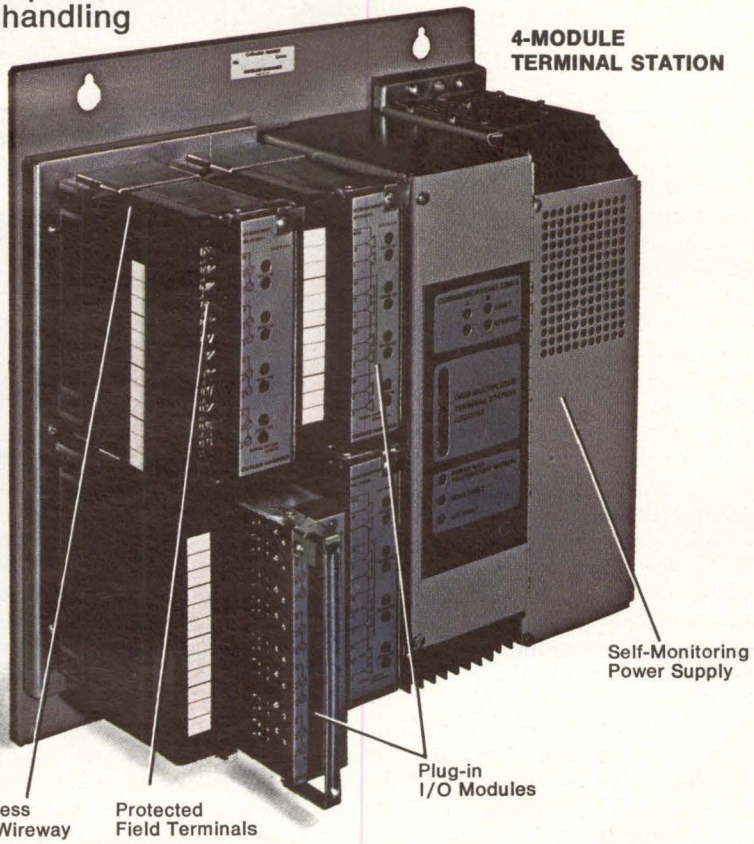
DIRECTROL's loop configuration permits "on-the-fly" modifications (adding terminal station #8) without system shutdown. Accelerates minor revisions and extensive system expansions.

Project simplification. DIRECTROL is designed and applied in a conventional control manner. But unlike the conventional, it substantially reduces wiring costs and project complexity—easily adapting to unanticipated requirements. For the first time, DIRECTROL offers control multiplexing in easy-to-apply, easy-to-order, easy-to-install modules.

System productivity. DIRECTROL's innovative approach provides high-yield features like monitoring of multiplexer performance on every signal scan, high security data handling routines, self-diagnostic/self-correcting characteristics, integral high noise immunity and multiple redundancy options to name only a few. Plus the unique ability to add new stations "on the fly" without affecting system operation.

Plant versatility. DIRECTROL's 4,096 signal capacity and 5,000 foot distance between stations combine with "stand-alone" independence or computer compatibility to add dramatic equipment selection flexibility for future needs.

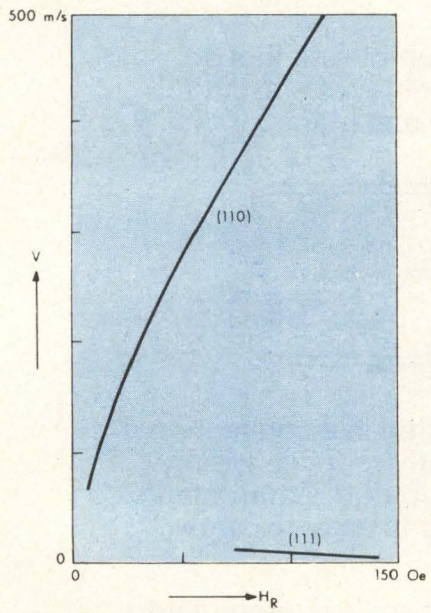
Why not set a new course for your industrial control requirements? Write Milwaukee, Wisconsin 53201 for descriptive brochure.



CUTLER-HAMMER

Best by Design

CIRCLE 23 ON INQUIRY CARD



Speed, v, at which magnetic bubbles can be moved in thin layers of magnetic material plotted as a function of the strength, H_r, of the rotary magnetic field applied to move the bubbles. Curve 111 has been measured for bubbles in conventional layers having uniaxial symmetry; curve 110 shows increase in speed obtained in materials with orthorhombic asymmetry

layer is in the preferred direction of magnetization in a magnetic field H_0, then with certain values of H_0, magnetic bubbles will occur in the layer in the form of cylindrical regions in which the direction of magnetization is opposite to that of H_0 and to the direction of magnetization in the remainder of the layer.

By applying a rotary magnetic field H_r in the plane of the layer it is possible to move the bubbles along a pattern of Permalloy strips arranged on the layer. The speed at which these bubbles can move is very important because it determines the maximum frequency of the rotary field and, therefore, the maximum clock frequency at which bubble memories can be operated.

An earlier investigation at the Philips Laboratories (see *Computer Design*, Feb 1975, p 50) revealed that the speed of the bubbles can be increased considerably by applying a field strength component parallel to the layer, in addition to the external perpendicular field H_0. With the usual bubble transport method it is impossible, when using the rotary field, for this extra field to be applied by external means (eg, coils). W. T. Stacy and D. J. Breed, research workers at the Philips Laboratories, have found, however, that it is possible to obtain this field component parallel to the layer by making use of a layer with "orthorhombic" anisotropy. In this case there is not only a strong magnetic preferred direction at right angles to the layer, but also some anisotropy in the plane of the layer; the magnetic properties are now clearly different in three directions at right angles to one another. Such anisotropy is obtained by a suitable orientation of the substrate and a composition of the layer such that there is a slight difference in lattice constant between layer and substrate ("misfit").

Investigations have shown that magnetic layers of manganese, europium, and lutecium containing iron garnet deposited on the (110) face of a single-crystal substrate of the nonmagnetic gadolinium-gallium-garnet

have the desired orthorhombic anisotropy. Bubble speeds of up to 500 m/s have been measured in these layers. Conventional layers, with uniaxial symmetry obtained using approximately the same material combination as (111) orientation (see graph), reveal bubble speeds of only 5 m/s. The graph shows the considerable gain in speed that can be obtained by appying orthorhombic anisotropy in the layer.

Circle 180 on Inquiry Card

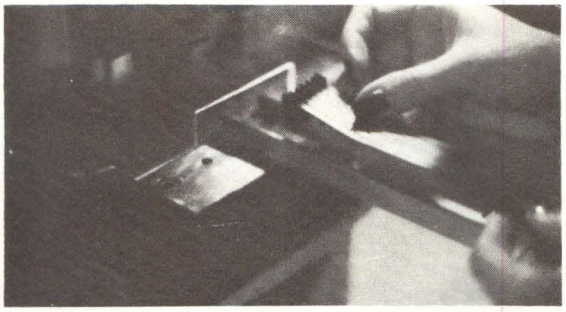
Flat Electronic Cable System Offers Improved Reliability

The Jet Flecs (Flat Electronic Cable System) is made up of several cable connector series, a variety of flat cable configurations, and an array of application tooling devices. Compatible with discrete wires as well as with flat cable, the system, developed by Molex Inc, 222 Wellington Ct, Lisle, IL 60532, claims to offer significant improvements in wiring interconnection reliability and cost savings.

System connector series JF KK .156 and .100 feature insulation displacement termination and are designed to satisfy connection requirements for high voltage, power distribution, and individual pairs of wires. Designed for use with either JF .156 flat cables or with 18-, 20-, 22-, or 24-gauge discrete wires, the JF KK .156 connector has a 3-point Trifurcon contact and is rated at 5 A. Connector sizes range from 2 through 16 circuits, in 94V-2 nylon with integrally molded strain relief tabs.

JF KK .100 system is designed for use with JF .100 flat cable or with 18-, 20-, 22-, and 24-gauge discrete wires. Contact is achieved through a 180-deg horizontally opposed 2-point configuration. Available in sizes 2 through 20, connectors are molded of 94V-2 nylon with integral wire strain reliefs, and are rated for 1 A.

Tooling for the system consists of a series of individual modules with the capability of completely preparing connector/cable assemblies. Either semiautomatic or manual, operator controlled modules have individual functions that include notching, shearing, and mass terminating flat cable to connector bodies, and testing the finished assembly for integrity of circuit continuation.



Bench-mounted, operator-controlled connector/cable assembly tooling supports Molex' Jet FLECS .100 and .156 systems, providing rapid assembly of prenotched cable to preassembled connectors

Circle 181 on Inquiry Card □

Microcomputer Interfacing and Analog Signal Conditioning Courses

August 21 through September 2, 1978

Donaldson Brown Center for Continuing Education, Virginia Polytechnic Institute & State University Blacksburg, Virginia

Presented by:
The Departments of Chemistry and Chemical Engineering and the Extension Division of Virginia Polytechnic Institute and State University

COURSE OBJECTIVES. The objective of these programs is to provide an intensive educational experience for the scientist, engineer, manager, or technician in the areas of microcomputer data acquisition, instrumentation, and measurement systems ranging from the analog sensor through the analog data channels to the microcomputer. The courses provide a combined lecture/laboratory experience. Continuing education units (CEUs) are provided for each course.

COURSES AND DATES. Basic Electronics for Measurements and Instrumentation. August 21, 22, and 23, 1978. This workshop will enable you to understand and use the basic AC and DC electronic laws as they apply to instruments and analytical measurement techniques. You will be introduced to signal conditioning using the versatile and popular operational amplifier in a variety of measurement and control configurations.

INSTRUMENTATION SIGNAL CONDITIONING TECHNIQUES. August 24, 25, and 26, 1978. This workshop will enable you to implement many signal conditioning and processing schemes found in analog instruments. Included is analog preprocessing of data for input into data acquisition and process control systems.

DIGITAL ELECTRONICS AND MICROCOMPUTER INTERFACE BASICS. August 28, 29, and 30, 1978. This workshop will enable you to use the digital circuits necessary for microcomputer interfacing and digital measurement techniques, and includes an introduction to microcomputer I/O.

MICROCOMPUTER, INSTRUMENT, AND ANALOG CONVERTER INTERFACING AND PROGRAMMING. August 31, September 1 and 2, 1978. This workshop will enable you to understand much of today's microcomputer jargon and implement analog converter and instrument interfacing schemes as well as develop the driver software routines for interface circuits and data handling.

INSTRUCTORS: Dr. Peter R. Rony, Mr. David G. Larsen, Mr. Howard M. Berlin, Dr. Paul E. Field, and Dr. Chris Skaar.

TEXTBOOKS: Texts will be selected from the popular Bugbook© series and Blacksburg Continuing Education Series© written by the course instructors and their colleagues.

COSTS: $195 for each three-day course, with textbooks, handouts, and lunches included.

FOR ADDITIONAL INFORMATION: Contact Dr. Linda Leffel at the above address or call at (703)951-5241.

Questions should be addressed directly to the course instructors, David G. Larsen (703) 951-6478, Dr. Peter R. Rony (703) 951-6370 or Dr. Paul E. Field, (703) 951-5376.

COURSE REGISTRATION

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"WITH THE MODCOMP CLASSIC, WE DON'T HAVE TO TRADE PERFORMANCE TO GET RELIABILITY."

Bill Greene, Staff Engineer
Process Computer Systems Group
Chemicals & Plastics Division Engineering
Union Carbide Corporation

Bill Greene is a staff engineer for the Process Computer Systems Group which is responsible for designing, building, testing and installing process control computer systems in the company's manufacturing plants.

Because of their experience, we gave them our new Classic 7860 super mini to test. Their experience with it was summed up in three words. "We love it."

"It's a reliable machine. And reliability is the name of the game."

"We'll trade performance for reliability anytime," said Bill. "But with the Classic, we don't have to.

"The Classic hardware is very solid. Especially for a new product. "The performance characteristics of the Classic are impressive, too. With its extremely fast floating point processor, the Classic can run through a program more than 3.7 times as fast as a MODCOMP II."

"A working computer with software that doesn't work is useless."

"We've been running the MAX III operating system for five years and the MAXNET III network extension for the past two years. They've performed well under very demanding conditions. In fact, over the past year, we've had more than 99.5% uptime on more than 30 installed MAX III systems.

"However, we're installing larger process computer networks now with more and more satellites. So we need increased host computer hardware and software capabilities.

"Our tests with MODCOMP's enhanced MAX IV operating system in the Classic have been very encouraging.

"MAX IV and the new MAXNET IV will help us relieve bottlenecks so that we can add more links and do more work with the computer. We also expect that File Manager, which can create a new file anywhere on a disc, will be a useful tool."

"We install 15-20 systems a year, so ease of implementation is important."

"Even though the Classic is a powerful and sophisticated machine, it should be an easy system for our project teams to implement. MODCOMP provides plenty of documentation and they've always been very helpful in working with us to get our systems up and running.

"In fact, we think so highly of MODCOMP and the Classic, we've already ordered two MODCOMP Classic 7860's to be used as host computers in large process control distributed networks."

It takes a tough computer to satisfy a tough customer.

At MODCOMP, we specialize in building real-time computers. They work in chemical plants. In petroleum refineries. In steel foundries. In jet propulsion labs. In electric power plants. In some of the harshest industrial environments you can imagine. Nevertheless, independent surveys have rated MODCOMP computers the most reliable systems on the market.

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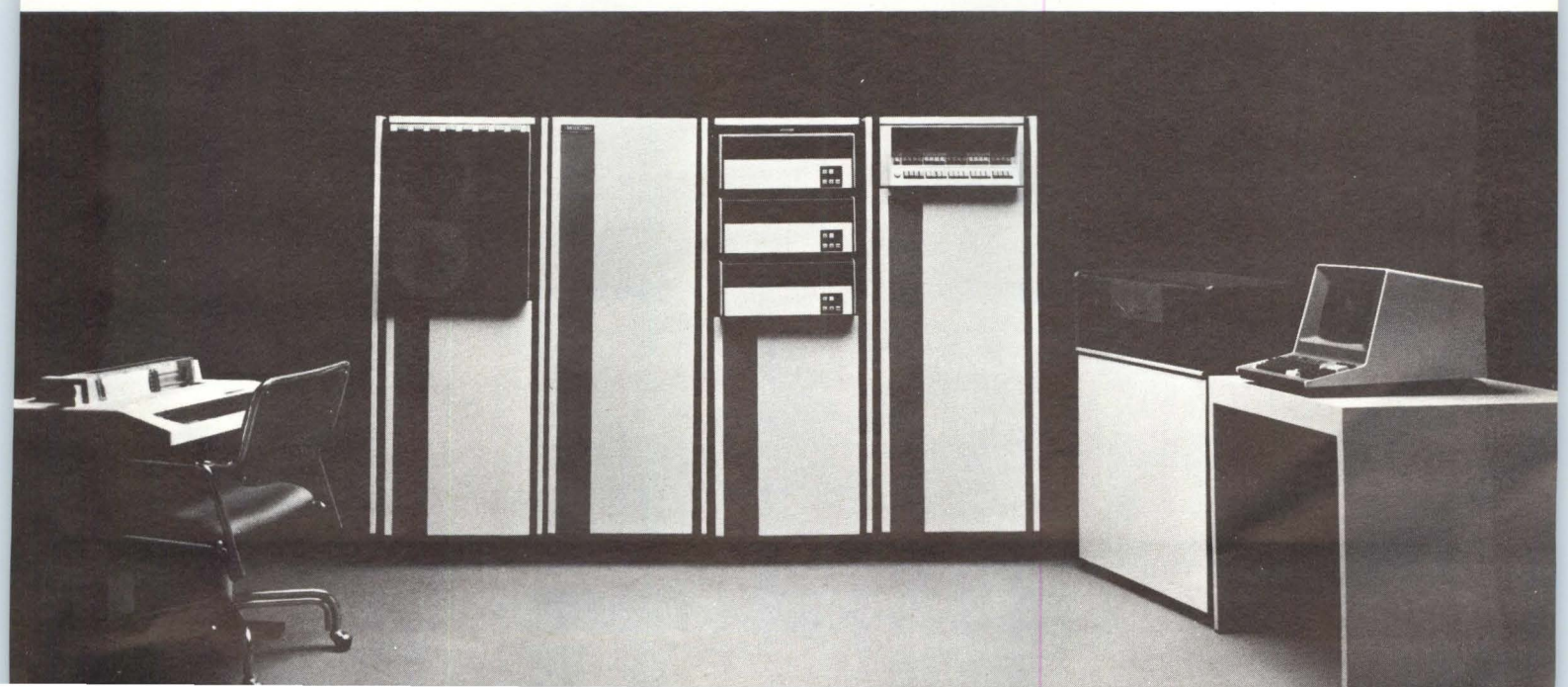
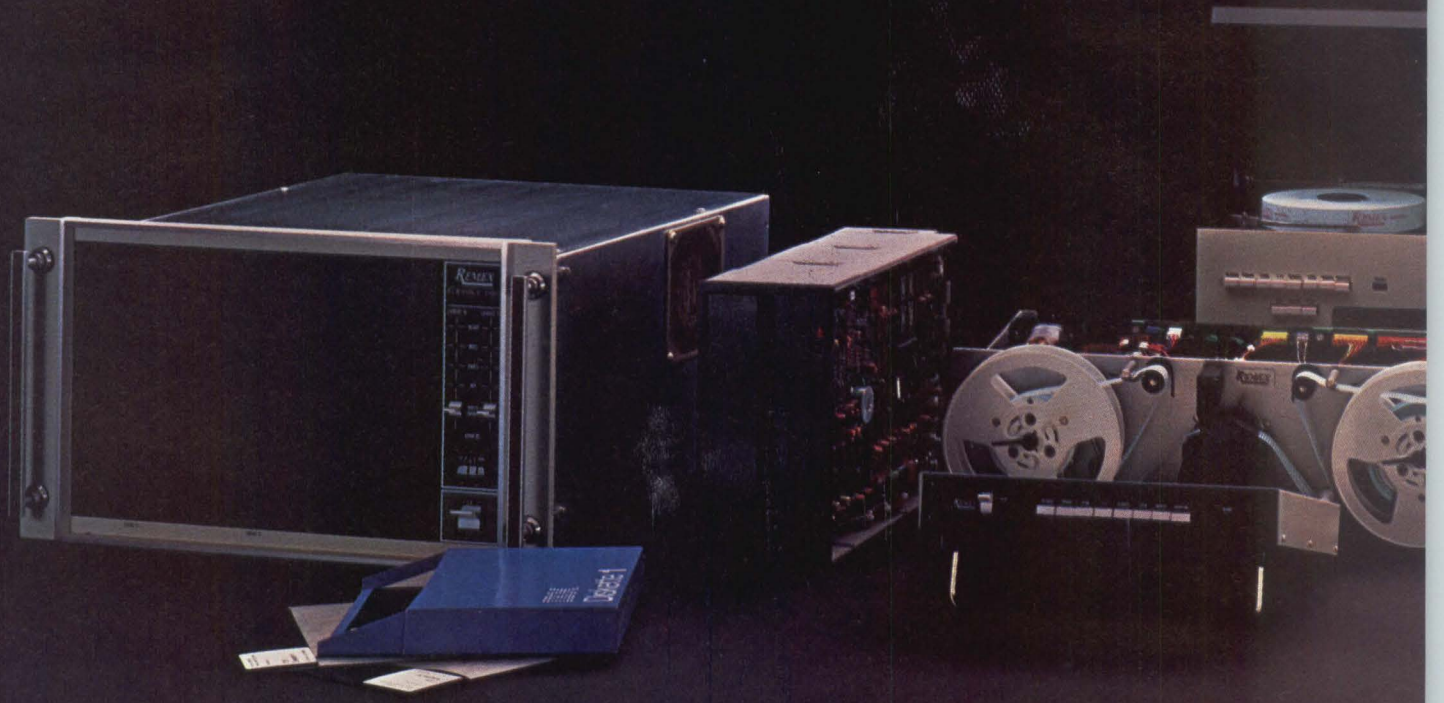




Paper isn't the only th

You think of Remex as the world leader in punched paper tape peripherals. Surveys show it. And our products and service prove it.

For nearly 20 years, we've offered the broadest selection of tape transports, readers, reader/spoolers, punches, perforators, combination units, computer interfaces, and communications gear—over 400 models in all.

Including a new family of handsome desk-top punched tape systems complete with a built-in RS232C serial interface.

Over 100,000 Remex punched tape peripherals are still operating in the field—some for over 15 years.

But paper isn't the only place where Remex looks good. We are, in fact, a leading manufacturer of quality *media handling* equipment, not just punched tape alone. Products like advanced flexible disk drives and systems you can benefit from today—not just on paper.

Our built-in formatter disk. It's like a $50,000 rebate for small OEMs.

Instead of spending the $50,000 or so needed to develop a good flexible disk controller/formatter, you can simply use ours—built right into the drive itself.

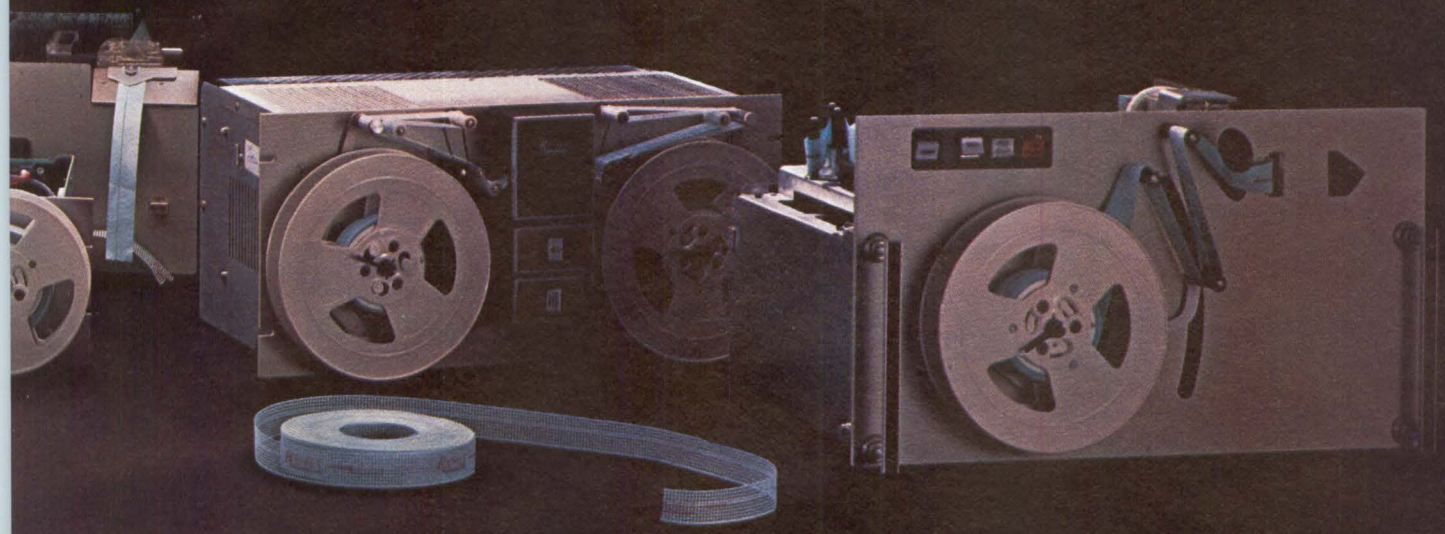
You save design dollars, time—and the space required by a separate formatter board. And you have the quality and good nationwide service support Remex is known for.

Remex' reputation cast in solid aluminum.

Think about it. Nearly twenty years of electro-mechanical sales and *service*. That's why the Remex drive mechanism is capable of 30,000 hours of normal use. Here's how we do it.

We use thick, solid castings instead of fabricated sheet metal. When you're talking about the densities on diskettes today, you're talking tolerances too close for bended metal.

We also use a V-groove lead screw with ball



ing we look good on.

bearing groove contact. The head is always perfectly centered on each track, because the wear is *downward* instead of side to side. No slop.

Something special for PDP-11® and LSI-11® users.

A completely optimized flexible disk system dedicated to improving throughput and capacity.

With our new Remex-11 flexible disk system you get a complete hardware/software package. And a choice of operation modes:

You can operate DEC's way within the constraints of RT-11®

Or you can enhance the performance of RT-11 by switching, literally, to a 16 sector-per-track format. You gain an instant 25 percent increase in capacity and a 19 percent increase in throughput.

Or, in special applications, you can take full advantage of Remex hardware such as transferring multiple sectors of up to 65K words with just two commands. Or formatting diskettes with just one.

We've even designed the Remex-11 so you can communicate with both DEC and IBM 3740 prepared diskettes — without losing RT-11 compatibility. The system supports up to four disk drives.

In short, Remex can provide you with future capability now at no extra charge.

Specifications and other information you need regarding drives, systems, and punched tape products are yours for the asking. Write or call: Ex-Cell-O Corporation, Remex Division, 1733 East Alton Street, P.O. Box C19533, Irvine, CA 92713.
Phone 714/557-6860. TWX: (910) 595-1715.

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REMEX DIVISION

CIRCLE 27 ON INQUIRY CARD

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Computers Overcome Tedium of Manual Monitoring in Data Acquisition and Control

Manual control of critical testing and monitoring procedures is gradually giving way to the digital computer. As more and more parameters are added to tests, the human element becomes inadequate. However, through utilization of the capabilities of present-day minicomputers, test engineers are not only able to meet all past requirements faster, cheaper, and better, they also can add much greater sophistication to testing procedures.

Two such test/monitor systems have been designed and implemented by engineers at Southwest Research Institute (SwRI), an independent research organization based in San Antonio, Texas. One of these systems, built for the U.S. Navy and installed at the Navy Shipyard in Long Beach, Calif, independently tests four rebuilt diesel engines at the same time. It not only saves costs in time and personnel, it also prevents engine failure during test. The second system automates tests of lubricating oils under exacting Army-specified test conditions. Components contained in both systems were manufactured by Hewlett-Packard, 1501 Page Mill Rd, Palo Alto, CA 94304.

Testing Operation of Navy Diesel Engines

Installation of the diesel engine analyzer (DEA) at the Long Beach Naval Shipyard permits twice as many engines to be tested with half as many people. In addition, it prevents catastrophic failure of engines while under test. (During a 2-year period before the computerized system was installed, 10 engines were seriously damaged during the manually supervised test periods. A few actually exploded.)

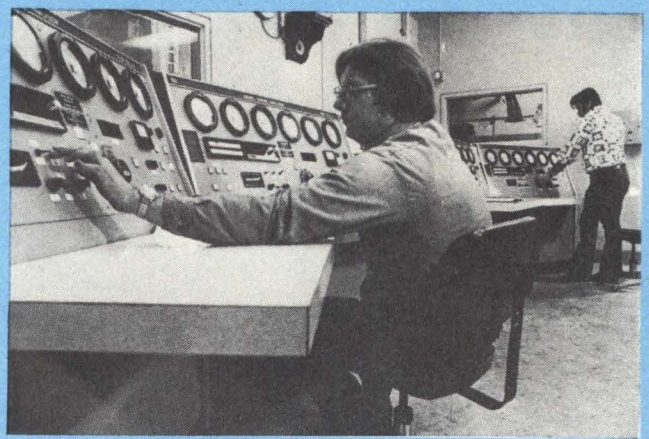

Fig 1 Control console at Long Beach Naval Shipyard diesel engine analyzer facility. Four diesel engines of different types can be tested and evaluated simultaneously. Windows in room allow viewing of cells adjacent to operator's panels

Automated testing and evaluation can be performed on 16 different types of engines. Four engines, all of different types, can be tested simultaneously in separate cells, each equipped with sensor sets for acquiring temperature, pressure, flow rate, wear, and performance data. Individual operator control panels are grouped at a central test console (Fig 1). Data from the sensors are recorded, stored, processed by an HP 9600E monitoring and control system. The DEA monitors up to 160 test points/s (40 for each engine under test), controls engine speed as well as dynamometer loading in programmed sequences, and triggers alarms and shuts down an engine if out-of-tolerance conditions are recognized. During testing, the computer performs realtime data analyses, calculates horsepower outputs under various operating conditions, and performs efficiency calculations.

Components of the monitoring and control system (Fig 2) include an HP 2100A minicomputer, HP 2313 analog-to-digital converter, HP 6940 multiprogrammer and HP 6941A extender subsystem for control of engines and dynamometers, two HP 2752A teletypewriters, HP 2640A CRT keyboard/display terminal, HP 2895A paper tape punch, HP 2748A paper tape reader, and HP 7901A cartridge disc subsystem. The 16-bit general purpose minicomputer has a 24k-word core memory and 980-ns cycle time. Its operating system, Hewlett-Packard's realtime executive, permits multiprogramming foreground-background operation and simultaneous-task use. The disc subsystem has an online capacity of 2.5M bytes (8-bit).

Software developed by SwRI consists primarily of four identical test/profile routines, one for each cell. These routines tie together and coordinate all program activities for a given test cell. All programs (Fig 3) are modular to simplify system checkout and future modifications.

Test points are scanned every second and readings from each point are updated. Data for every 5 min of a test, for the end of each test, and those read just before an emergency stop are stored on the system's disc memory. A "shutdown" file can be read back from disc after an emergency stop to where the out-of-tolerance

$1925

Unretouched photograph of screen.

There isn't a process control system in the industry that our Intecolor 8001G can't improve, because color communicates better.

Bailey Meter, Taylor Instruments, Dow Chemical, International Paper, ACCO Bristol, PPG Industries come from a long list of industry leaders who have integrated our Intecolor 8001 color data terminal into their systems—sophisticated systems that demand critical control. Now we can bring you the Intecolor 8001G, the same precision terminal with a special color graphics package as a standard feature, at considerable savings over the separate option cost. Look at some of the advanced Intecolor 8001G features: • Expanded hardware and software graphics • 48 lines by 80 characters with two different character heights • Eight foreground colors, plus eight background colors for additional definition • Character and line insert and delete • Page roll-up • 64 Standard Instrument Society of America characters • Plotting capability on a 160 by 192 matrix • Expanded keyboard with cursor and color controls • 19" display.

A 25" unit with the same standard features is available at slightly extra cost.

We guarantee delivery of your Intecolor 8001G evaluation unit for $1,925* (cash-with-order) within 30 days or your money back. The same $1,925 price goes for orders of 100 units or more. All Intecolor units are covered by a six month warranty. So get the jump on your competition, without outspending your competition. Call 800-241-9888 toll-free for a demonstration.

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1 Start your microprocessor-based product with HP's 2649A.

It's an 8080 MPU, CRT, display subsystem, power supply and 15-slot backplane, all in a good-looking case.

You choose the RAM, PROM, ROM, serial or parallel I/O, dual cartridge tape drives or keyboard you need for your product.

Then take advantage of our standard firmware, including utility subroutines for data display manipulation, keyboard switch translation, data transfer and communcations protocol. It's software you don't have to write and debug.

2 Study our documentation to understand the 2649A.

Our 2649A hardware and firmware documentation was written by engineers who know the 2649A inside and out. Because they designed it.

For easy reference, its 1,800 pages are organized in two volumes like an encyclopedia. So, for example, if you need the pin assignments for our keyboard interface module, it's easy to look up. And you'll find the details in the words of the engineer who designed it.

The more you know about our product, the less time you'll spend on yours.

3 Write, assemble and debug your software on the 13290B Development Terminal.

The 13290B has a source program editor so you can quickly write 8080 assembly language programs. A resident assembler to convert source programs into 8080 object code. 64K bytes of RAM as a test bed for your software. And a friendly, interactive debug program that lets you watch your program run step by step, in mnemonics, not ones and zeroes.

And because the 13290B *is* a 2649A, your program runs in your product's environment, which is a big help if timing or execution speeds are important.

It's probably the only development tool you'll need.

4 Get hands-on experience at our 2649A workshop.

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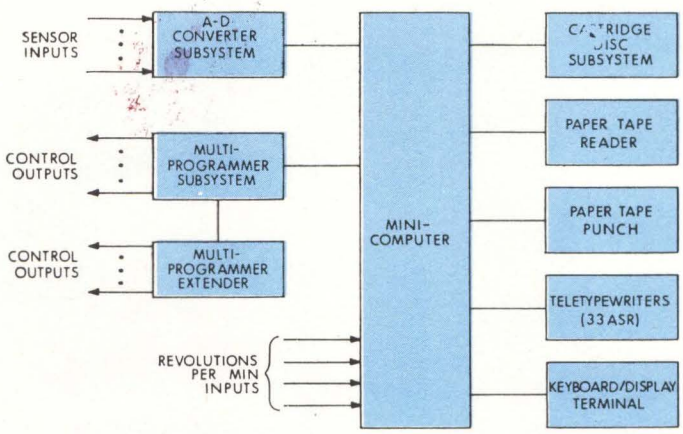

Fig 2 Diesel engine analyzer simplified block diagram. HP 2100A minicomputer is controller for other components of system. Sensors attached to engines under test are monitored via A-D converter subsystem and multiprogrammer subsystem. Test results are shown on readout devices either as displays or hard copy

condition occurred. If the condition detected is not an immediate emergency but indicates that an emergency condition could build up, the engine is automatically slowed to idle speed and run for 5 min to cool it gradually before it is shut down.

Prior to start of testing, each engine is usually completely overhauled (the engine is steam cleaned and disassembled; each part is chemically cleaned, inspected, and reground or replaced if noticeably worn; and the engine reassembled). Then the engine is placed in a test cell and connected to a dynamometer. This action is fully independent of the other three cells and does not interfere with or concern conditions in those cells.

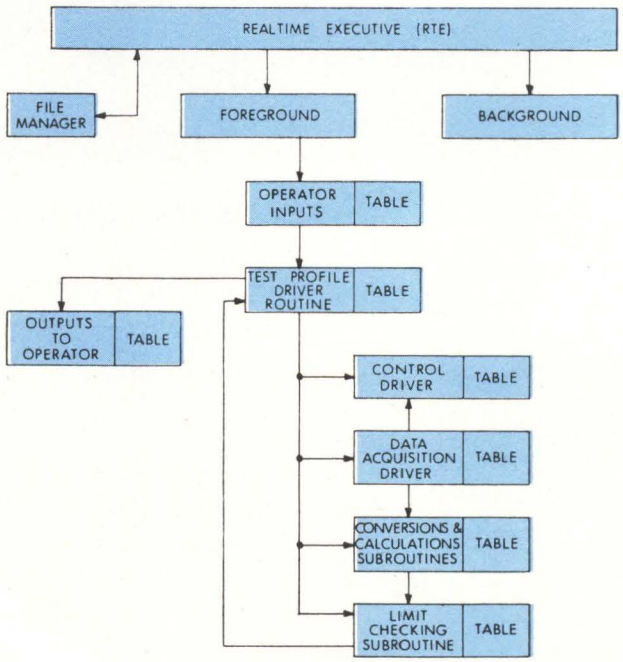

Fig 3 Interrelationships of major software programs for diesel engine analyzer system. Programs contain all list performance instructions. Operating system is Hewlett-Packard's realtime executive. Identical test/profile routines tie together and coordinate all program activities for each engine cell. All programs are modular and table driven

(*Continued on p 62*)

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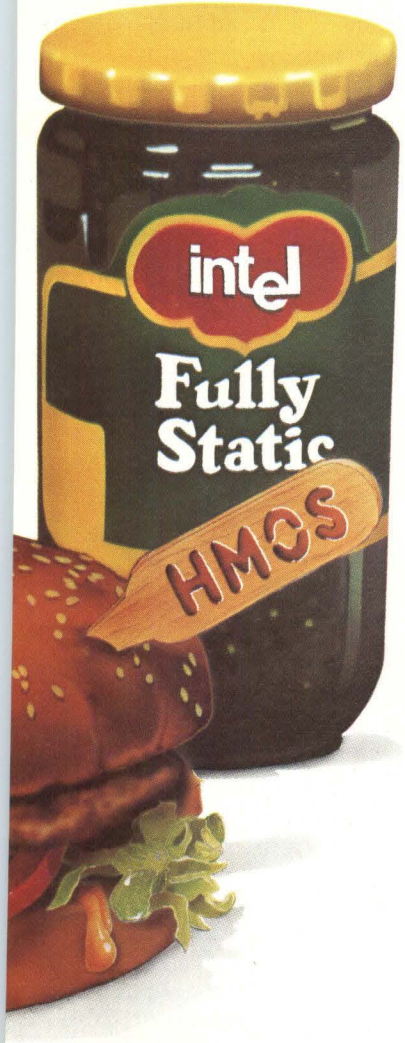
2141-3	150	70	20
2141-4	200	55	12
2141-5	250	55	12
2141L-3	150	40	5
2141L-4	200	40	5
2141L-5	250	40	5
2147	70	160	20
2147-3	55	180	30
2147L	70	140	10



For a copy of our HMOS reliability report and data sheets, write Intel, Literature Dept., 3065 Bowers Avenue, Santa Clara, CA 95051.

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CIRCLE 31 ON INQUIRY CARD

Each cell includes a transducer cabinet and patch panel. Transducers are attached to the engine under test according to the predetermined procedure for that particular engine. All arrangements simulate at-sea conditions as closely as possible.

Sensors are available to monitor engine speed; temperatures of cooling water in and out, lubricating oil, ambient air, fuel, exhaust, air manifold, dynamometer water, and dynamometer bearings; load torque; fuel use; smoke density; pressures of lubricating oil, water pump, turbocharger, exhaust manifold, crankcase, and dynamometer water; and oil line debris. When relevant transducers are attached, the system operator notifies the computer, via a teletypewriter, that the engine is ready for the test and enters engine type and identification data.

The appropriate program for the engine being tested is loaded into the minicomputer from disc memory. This program contains all test procedure instructions and tolerances set for each test point for each phase of the test. Adjustments to these parameters can also be made during the test. Then, before the computer system begins monitoring, it carries out a self-check to determine whether or not calibration is complete and all transducers are attached properly to the engine under test. (Calibration of transducers is performed every 200 hours of engine testing.)

Under control of the minicomputer, the engine is started and run through the break-in and performance-checking profiles for that engine type. A low idle speed is attained and progressively increased through several phases of levels of load and speed for run-in and system shakedown. Maximum power and torque are tested and governor dynamic performance and stability tests are performed. Engine load is governed by the computer system by controlling the dynamometer.

Next, the engine is returned to a low speed idle and shut down. If no parameter limits are approached or exceeded, the computer operator receives no outputs from the teletypewriter until the test is over—unless specific information is requested. Tests usually run 8 to 28 hours. Output from the tests can be obtained on the keyboard/display, on the teletypewriters, or on paper tape.

Key parameters and test data are displayed and updated every second on the keyboard/display terminal for all four test cells. The CRT screen is divided into four columns, with each column devoted to one of the test cells. Data displayed in tabular form include cell number, engine type, engine serial number, total test time, test time remaining, test status, and values of all key engine parameters being monitored and controlled.

In an emergency, such as a loss of lubricating oil pressure, the computer activates electrical solenoids to cut off fuel and thereby shut down the engine. When this occurs, an alarm is sounded and a red light appears in the engine test cell. A summary of the problem detected is printed out on the typewriter and the CRT test status display is updated. As a backup to the fuel cutoff system, provision is also made for the manual injection of carbon dioxide into the engine air inlet.

If diagnostics are required during the engine test, the engine is automatically brought to a no-load idle condition, and a message typed on the operator's teletypewriter requests that an engine specialist be called to assist in the diagnosis. The test status displayed on the CRT is updated accordingly and summarizes the problem, directing the specialist's activities according to preprogrammed diagnostics corresponding to the parameter or combination of parameters that are out of limits.

If the test is completed successfully, the engine is brought to an orderly stop and the operator is notified. A punched paper tape is marked and appropriately filed by the system operator.

In addition to the added protection for engines under test, including detection of contaminants in the engine, the computer-controlled engine analysis system reduces the number of trained personnel required at the test station and is far more dependable than manually-controlled monitoring and shakedown. Previously only the hearing and vision of operators could detect unusual conditions that might predict a catastrophic failure.

The overall result has been reduced cost and improved efficiency. Eventually, also, testing time may be reduced. More data can now be collected in less time than before and those data can be compared to engine performance prediction curves based on data collected from previous tests.

Testing of Automotive Lubricating Oils

At SwRI's San Antonio Laboratory test engineers monitor data from 800 sensors on 50 diesel engines to test lubricating oils and other automotive products (Fig 4). The system, which runs continuously for 20 days during a test, is controlled by an HP 2100A minicomputer with 24k words of core memory. It collects and logs vast amounts of data on temperatures, pressures, speeds, and other parameters and prints out both memory plots and tabulations in real time. In addition, it alerts oper-

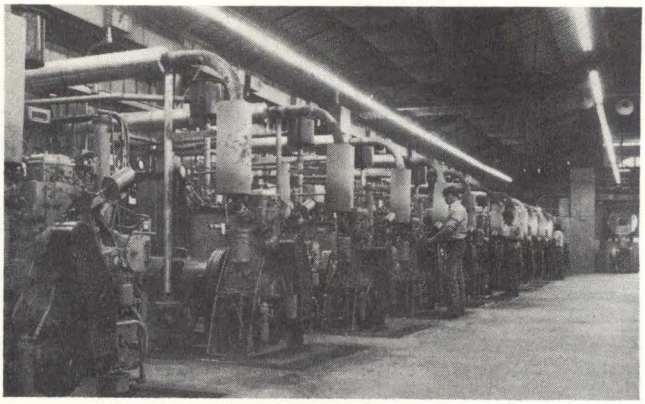

Fig 4 Part of SwRI test stand area. Up to 50 diesel engines, monitored and controlled by HP 2100A minicomputer, test lubricating oils and other automotive products to Army-specified conditions

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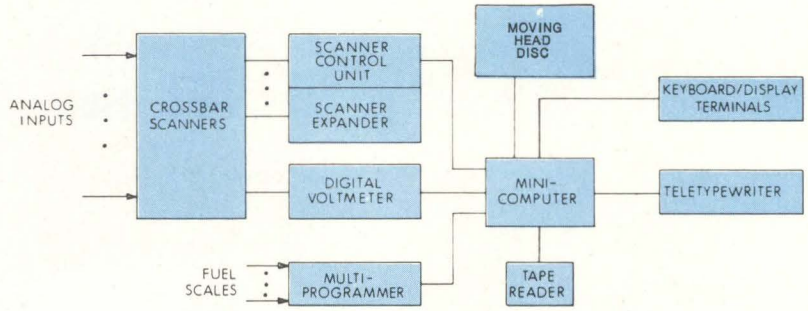

Fig 5 Simplified block diagram of system for testing lubricating oils. Crossbar scanners interface to engines to process up to 800 analog inputs on pressures, temperatures, engine speed, load, and fuel consumption rate

ators if any of the parameters exceeds specified range limits. An alarm message is printed on a teletypewriter and displayed throughout the laboratory via a closed circuit television system, alerting the operator where manual adjustments must be made. Alarm test specifications are set closer than the actual test specifications so that an alarm message will occur before the value actually goes out of limits.

The data acquisition system includes a 2.5M-word HP 7900A disc subsystem, HP 2748A tape reader, three HP 2640A keyboard/display terminals, and an HP 2754B teletypewriter. It makes full use of the realtime executive multiprogramming capabilities of the Hewlett-Packard software operating system. This allows simultaneous performance of tasks such as test administration, computation, plotting outputs, data retrieval, and debugging of other programs by multiple users. The system utilizes 10 core-resident programs, leaving foreground and background disc areas to perform less time-critical tasks. All data acquisition programs are written in assembly language.

The data acquisition system contains capacity for 800 separate analog channels, allowing 16 sequential channels to each engine. Channels are assigned to take readings of cooling water-out and water-in temperatures; oil, intake air, and exhaust temperatures; intake and exhaust pressures; oil and jet pressures; and humidity.

During the test, readings of each of these parameters are made at 6-min intervals. At any given time separate groups of engines can undergo varied or similar tests with different requirements. The computer calls from memory the appropriate program for each test.

Readings are added to a running hourly total accumulated in disc memory. At the end of each hour's run time, an average is taken and the data are logged on disc memory. High and low readings are also stored and all readings are constantly compared to specification tolerances in memory.

Sensors, such as thermocouple and pressure transducers, convey electrical signals in analog form from the engines under test to four HP 2911A electronic scanners (Fig 5). These signals are converted to digital form by an HP 2402A digital voltmeter. An HP 2911B scanner control unit performs control and input channel selection for the four scanners, and an HP 8159A scanner expander allows the single scanner control unit to handle all four crossbar scanners.

Fuel rates are determined by a gravimetric method. Each engine is assigned an input line on an event sense card in an HP 6940A multiprogrammer. Using the card's interrupt capability, the computer can detect a start time and a stop time and determine the time required for the engine to burn a set amount of fuel.

A second HP 2100A minicomputer, with 32k-word memory, provides backup data storage and added input/output lines to the engine laboratory system, and is used for software development. This system also contains two HP 7970B magnetic tape units, HP 7900A moving head disc with 2.5M-word capacity, HP 2716B card reader, HP 2895A tape punch, HP 2748A tape reader, HP 2752 teletypewriter, HP 2610 line printer, and Calcomp 565 high speed plotter.

The software development system is used to further process collected data and for development of new software application programs. Plots, tabulations, and other outputs are produced on this system's plotter and high speed printer. A disc memory unit stores data and programming for transfer to the data acquisition system when required.

According to SwRI, this laboratory can gather 10 times more data with greater accuracy than possible manually. Whereas the latter method required many slow, manual steps—which were subject to human error and interpretation—the computer-controlled method monitors, logs, calculates, and plots automatically. □

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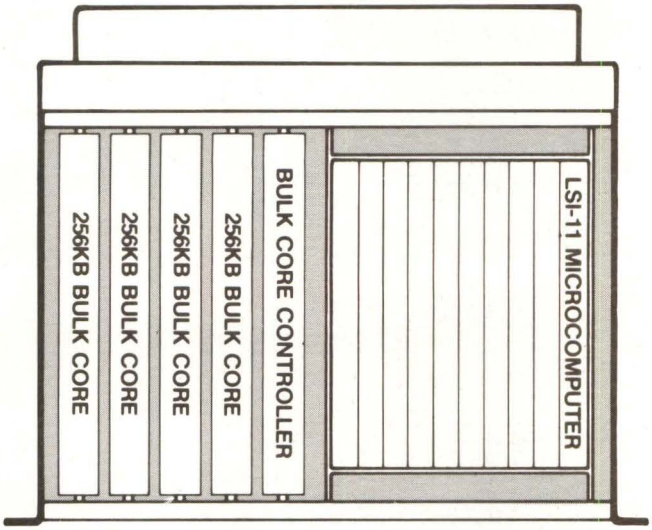

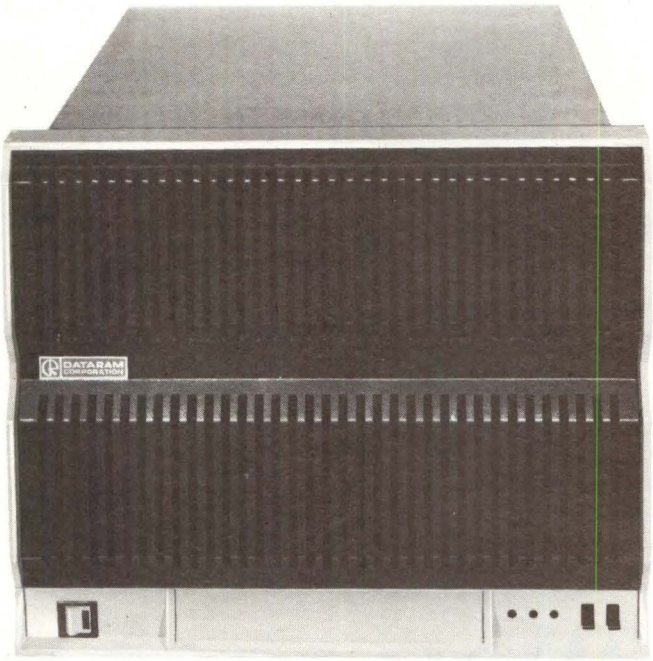

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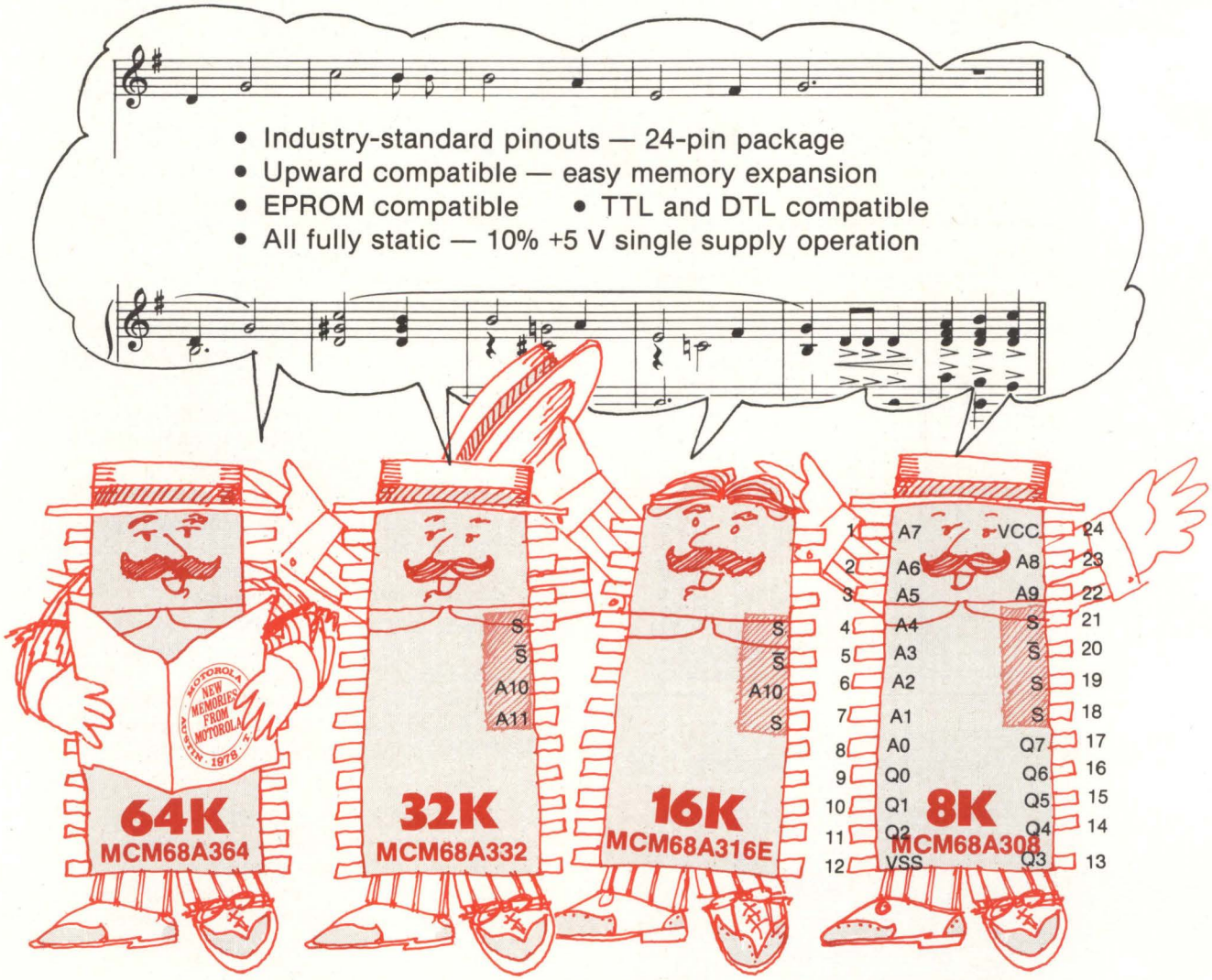

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STATE-OF-THE-ART IN HIGH SPEED ARITHMETIC INTEGRATED CIRCUITS

Use of bipolar technology to construct arithmetic ICs has resulted in devices with increased switching speed and gate density and low power dissipation. Future technological advances should have an even greater impact through larger chip diameters and sharper pattern fabrication

Shlomo Waser Monolithic Memories, Incorporated, Sunnyvale, California

Current integrated circuit technology provides a full spectrum of arithmetic devices, varying in speed and capabilities. These devices can be divided into three groups according to their speed. In the first, or slowest, group are calculator chips that operate at greater than 1 ms; in the second, or medium speed group (1 μs and slower), n-channel metal-oxide semiconductor microprocessors; and in the third, or fastest group (1 μs or better), bipolar data slices and bipolar discrete units (adders, multipliers, etc). The third group of high speed arithmetic integrated circuits, under discussion here, are significant building blocks in constructing "number crunching" systems for use in weather modeling, nuclear physics computations, and realtime digital signal processing tasks such as speech and image processing, computerized tomography, and air traffic monitors.

Technology Background

To understand the difficulties encountered in fabricating high speed arithmetic integrated circuits (ICs), it is necessary to review semiconductor technology in general, with particular attention to bipolar technology. In this respect, consider the three factors that limit how much parallel arithmetic can be put into one chip: maximum allowed power dissipation, pin count, and cost.

Maximum Allowed Power Dissipation

In high speed technologies (mostly bipolar), maximum number of gates is a direct function of the chip's maximum allowed power dissipation. This, in turn, depends on maximum allowed junction temperature of the silicon die, ambient temperature, and ability of the IC package to dissipate heat (thermal resistance). This relationship is defined as

$$\text{Max power dissipation} = \frac{T_{junction} - T_{ambient}}{\theta_{ja}}$$

For military specifications, $T_{ambient}$ = 125 °C, a typical package at still air has a thermal resistance (θ_{ja}) of 40 °C/W, and the maximum allowed junction temperature is 175 °C [for transistor-transistor logic (TTL)]. These values give 1.25-W maximum power dissipation, which is typical of most large-scale integrated (LSI) devices on the market today. However, effective thermal resistance between the IC package and the ambient environment can be reduced to 15 °C/W by attaching the package to a heat sink and cooling it by forced air.[1] If IC operation is limited to the commercial temperature range (maximum 70 °C), maximum power dissipation is about 7 W. While this latter dissipation value seems feasible, available ICs (with this characteristic) are undesirable, because they will usually be interfaced and surrounded by ICs that dissipate less than 1 W. Thus, a

local hot spot is generated that is difficult to cool efficiently and reliably.

The maximum number of gates that can be integrated into one chip is equal to the maximum allowed power dissipation divided by the power dissipation of each gate. For example, one of the most popular and successful technologies today is low power Schottky TTL (LS/TTL) which dissipates 2 mW/gate; this LSI chip type contains about 600 gates.

In a given technology, power dissipation of each gate is roughly proportional to its physical size, which in turn is determined by number of active elements and resolution of the lithography used to define the geometries of the transistors. For random-access memories (RAMs) the progress from 1k to 16k bits was mostly due to reducing the 3-transistor cell to a 1-transistor cell and cutting the line width of the fabrication pattern from 10 to 5 μm. Introduction of the 64k RAM will probably require an improvement over present photolithography techniques, with electron beam lithography the most likely process.

Pin Count

Number of available pins in the IC package is a severe limitation for high speed arithmetic on wide words. Multiplying 16-bit operands requires a package with at least 66 pins. The state-of-the-art is 64 pins, and no major breakthrough is in sight[2]. Even custom ICs do not exceed this limit by much, although the Amdhal computer uses a custom 84-pin flat-pack package. Pin count limitations have led to the data "slice" concept; ie, partitioning the desired system into identical parts that have common control and interconnection mechanisms (carry, etc). The pin limitation can also be circumvented by time-multiplexing the information via common pins; however this reduces the overall speed.

Cost

If power dissipation is not a limiting factor, as with metal-oxide semiconductor (MOS) and integrated-injection logic (IIL) technologies, cost will limit the die size. Noyce[3] points out that if yield is a function of random defects, cost increases exponentially with die size. For example, if a given chip size yields 10% good die, a chip twice as large will yield 1%. The cost for twice the function will be 20 times as great. Other major cost elements are testing and assembly, which are approximately fixed per chip. Consequently, as the number (N) of functions per chip increases, the assembly cost decreases proportionally to 1/N. Minimum cost per function will be at the crossover point between silicon chip cost and assembly and test cost. Progress in ICs can be viewed as a fixed cost (about $10) for increased complexity (three orders of magnitude in the last 15 years).[2]

Characterizing Technologies

To simplify comparisons among the various technologies, the "natural" gate implementation is analyzed. Natural gate is a realization of a Boolean operator that requires a minimum number of transistors while giving maximum speed. For TTL, this gate is a NAND; for ECL, it is a NOR. Unfortunately, no known technology has the exclusive-OR as its natural gate. Unless otherwise stated, the word gate will be used instead of natural gate.

Two main characteristics of a gate are power and speed. A common figure of merit is the speed-power product, where speed is in nanoseconds (ns), power is in milliwatts (mW), and product is in picojoules (pJ). A third characteristic is the gate's fan-in. In most bipolar technologies, fan-in is four. In the TTL family, NAND gates with one, two, three, or four inputs have the same speed and the same power, whereas larger fan-in NAND gates have larger speed-power products. Limited fan-in is a severe limitation in arithmetic operations on wide words requiring carry-lookahead (CLA).

Bipolar Technologies

All fast IC technologies are bipolar; the two most commonly used today for high speed arithmetic hardware are ECL and Schottky-TTL. Integrated-injection logic (IIL) is a relatively new technology that will become important for very large-scale integration (above 1000 gates/chip).

Emitter-Coupled Logic

ECL is the fastest, commercially available technology; gate delay is 1 to 2 ns, and speed-power product is 50 pJ. Although introduced about 10 years ago, the technology is still limited to applications that require very high speed, such as top of the line mainframe computers (IBM 370/168, Amdhal 470, DECsystem 10) and some signal processing equipment because of design difficulties. Interconnections become, in effect, transmission lines that require proper termination and matching. Also, reliable ECL designs need to use multilayer printed circuit (PC) boards, which are expensive. Since ECL devices normally are powered from a —5.2-V supply, they are incompatible with the popular TTL family. Another severe shortcoming of the ECL devices is their excessive power dissipation of 25 to 60 mW/gate, which requires forced air cooling. Nevertheless, if maximum speed is needed, ECL is the best choice. The internal circuit of ECL is a current-switching mechanism, which implies a constant current drain of the power supply. By contrast, the TTL logic family, using voltage threshold, causes large current spikes on the power supply during switching from one state to another.

ECL technology is implemented by various families. The fastest (1 ns) is MECL III from Motorola,[4] Fairchild, and Signetics. The 10,000 family has the largest selection of ECL LSI devices, and it is the only ECL family with arithmetic units. A typical gate operates at 2 ns and 25 mW.

Transistor-Transistor Logic

TTL technology was introduced in 1964 by Texas Instruments (TI).[5] It has been the most popular logic family for more than a decade. The original family had a 10-ns gate at 10-mW dissipation, and devices of this family are still the least expensive ICs. However, two subfamilies are making inroads. One is the Schottky-TTL (S/TTL) with a 3-ns gate at 20 mW, matching the speed-power product

TABLE 1

Comparison of Common Bipolar Technologies Used in Implementing High Speed Arithmetic Devices

		Gate Characteristics				2-Input Exclusive-OR			
Technology/ Year Introduced	Function	Delay	Power	Speed-Power Product	Density (gates/mm²)	Delay	Power	Speed-Power Product	Comments
ECL-III (1968)	NOR	1.1 ns	60 mW	66 pJ	30	1.3 ns	70 mW	91 pJ	Limited number of functions
ECL-1000 (1971)	NOR	2 ns	25 mW	50 pJ	30	2.5 ns	50 mW	125 pJ	Large selection of functions
S/TTL (1970)	NAND	3 ns	20 mW	60 pJ	30	7 ns	60 mW	420 pJ	Large selection of functions
LS/TTL (1972)	NAND	10 ns	2 mW	20 pJ	30	10 ns	8 mW	80 pJ	Large selection of functions
IIL (1975)	NAND	10 ns	0.1 mW	1 pJ	300				Not a mature technology
NMOS (1973)		100 ns	0.1 mW	10 pJ	130				For reference only
EEIC (1977)		0.25 ns	2 mW	0.5 pJ	100				Still in research and development

of ECL. The second subfamily, low power Schottky (LS/TTL), retains the speed of original TTL but decreases the power dissipation to 2 mW. Popularity of TTL technology has led to the largest selection of different ICs. Most small-scale integrated (SSI) and medium-scale integrated (MSI) devices are triplicated in three subfamilies (TTL, S/TTL, LS/TTL); however, most LSI devices are implemented only by LS/TTL. TTL ICs operate from a 5-V power supply. No critical problems have envolved in PC board layout as in ECL, and power dissipation typically does not require any special cooling. As noted previously, precautions need to be taken in decoupling the power supply lines, due to current spikes that are present while switching from one state to another.

Integrated-Injection Logic

IIL is a relatively new technology[6] (1975) that has not matured like ECL and TTL; thus, conflicting reports exist about its potential characteristics. Nevertheless, a gate with LS/TTL speed of 10 ns and power dissipation of 0.1 mW is reported.[7] It is likely that by 1980, most high density monolithic arithmetic processors will be implemented in IIL, replacing LS/TTL completely for such applications. In fact, the photochemical process used in fabricating LS/TTL can be modified to handle IIL, making it even more attractive than a completely new technology.

Most digital IIL devices are powered from a 5-V power supply to retain TTL compatibility. However, IIL technology needs only 1 V to operate, since it requires only current sourcing, and no voltage thresholds are used. Thus, for applications where TTL compatibility is not required, further power reduction is possible at no sacrifice in speed.

Table 1 summarizes the characteristics of the described technologies. A characterization of the implementation of an exclusive-OR gate is included for each technology because this Boolean operator is the major element in implementing digital arithmetic.

Arithmetic Elements

Arithmetic Logic Unit

Arithmetic logic units (ALUs)[4,8] are capable of add, subtract, shift, and logic operations (AND, OR, ex-OR). The most popular ALU device is the 74S181 implemented in S/TTL technology (or 74181), which is used in minicomputers such as the DEC PDP-11 and the Data General NOVA. This device performs addition using a carry-lookahead algorithm across four bits at a time. When operating on wider words, a companion device (74S182) provides a full carry-lookahead across any number of bits. Each carry-lookhead unit (74S182) receives the generate and propagate terms from a group of four 74S181s. In general, the number of levels of carry-lookahead is $\log_4 n$; eg, adding 64 bits with full carry-lookahead takes 15 ns in ECL and 28 ns in S/TTL.

The 74S181 (and the 10181) are combinatorial devices, and accumulation of results requires an additional register (accumulator). The 74S281 is an ALU with an accumulator on one chip, which still uses the 74S182 for carry-lookahead. Adding and storing 64-bit operands take 42 ns.

Texas Instruments has introduced two additional -81 devices. The 74S381 is similar to the 74S181—some functions of the 74S181 were removed to enable it to be packaged in a 20-pin, 0.3″ (7.6-mm) package instead of the 24-pin, 0.6″ (15.2-mm) package used to house the 74S181. The second device, the 74S481, will be discussed in the section dealing with processor elements.

Table 2 lists the speed and power of commonly used ALUs. As can be expected, power is approximately proportional to the gate count of the device. The first three devices listed in the table are basic ALU elements. 74S181 is implemented in S/TTL; the 10181 in ECL. 74S182 and 10179 serve as support chips for the ALU, and provide carry-lookahead when several ALUs are cascaded. The 74S281 contains an on-chip accumulator, but is slower than the combinatorial ALUs. Table 3 extends the chip comparison into the system level. When several ALUs are cascaded, the carry-lookahead units provide faster addition and subtraction, at the expense of increased power dissipation. S/TTL addition of 64 bits takes only 28 ns, but results in 11-W power dissipation. Addition of only 4 bits does not require carry-lookahead, addition of 16 bits requires only 1 carry-lookahead, but addition of 64 bits uses 5 carry-lookahead units.

Multipliers

In describing the ALU adder ICs it is clear that the most common addition algorithm is the carry-lookahead, and the most common configuration is four bits per IC. In contrast, multipliers use a variety of algorithms and configurations.

Parallel multiplication algorithms can be divided into two types: those that generate partial products and those that add the partial products. In generating partial products. The n bits of the ith partial product method is to use AND gates. If the multiplier (Y) and the multiplicand (X) each have n bits, there are n partial products. The n bits of the ith partial product are generated by ANDing Y_i with each of the n bits of the multiplicand X. However, in 2's complement representation, a correction is required since the most significant bit (MSB) has, effectively, a negative weight.

Booth's algorithm[9] is a method of recoding the multiplier so that the sign bit (MSB) is treated in the same way as the rest of the bits. A modified Booth's algorithm, suggested by MacSorley,[10] serves as a means of halving the number of partial products while keeping the elegance (sign bit treated as any bit) of the original algorithm for 2's complement numbers. The reduced number of partial products increases multiplication speed and decreases gate count. The motivation behind Booth's algorithm is to skip over a string of 1s and 0s, rather than form a partial product for each bit. Skipping a string of 0s is clear. Skipping over a string of 1s involves computing a string of 1s by subtracting the weight of the rightmost 1 from the modulus of the string. For example, the binary string 1111 is $2^4 - 2^0 = 15$, and the binary string 11100 is $2^5 - 2^2 = 28$.

In the actual hardware implementation, Booth's algorithm requires that the operand (multiplier) be divided into N/2 groups or substrings, each of which has

TABLE 2

Comparison of Arithmetic Logic Units

Part No.	Function	Gate Count	Speed	Power
74S181	4-bit ALU	75	11 ns	600 mW
10181	4-bit ALU	75	7 ns	600 mW
74S281	4-bit ALU/ accumulator	100	22 ns	700 mW
74S182	4 groups carry-lookahead	20	7 ns	350 mW
10179	4 groups carry-lookahead	20	4 ns	300 mW

TABLE 3

Comparison of Speed/Power at System Level

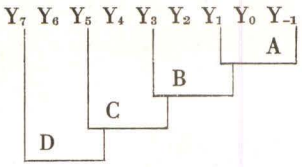
Part No.	Technology	Speed/Power 4 Bits	16 Bits	64 Bits
74S181/ 74S182	S/TTL	11 ns/600 mW	18 ns/2.7 W	28 ns/11 W
10181/ 10179	ECL	7 ns/600 mW	11 ns/2.7 W	17 ns/11 W

three bits. Assume that the multiplier has the binary pattern 0111. A 0 digit is added to the right, and the resultant number (01110) is divided into two 3-bit groups. All possible permutations of these substrings are computed from the chart to determine the partial products.

2^1 Y_{i+1}	2^0 Y_i	2^{-1} Y_{i-1}	
0	0	0	Add zero (no strings)
0	0	1	Add multiplicand (end of string)
0	1	0	Add multiplicand (a string)
0	1	1	Add twice the multiplicand (end of string)
1	0	0	Subtract twice the multiplicand (beginning of string)
1	0	1	Subtract the multiplicand ($-2X + X$)
1	1	0	Subtract the multiplicand (beginning of string)
1	1	1	Subtract zero (center of string)

The first group is 110, which requires subtracting the multiplicand; the second group (011) requires adding twice the multiplicand. Since the second group is shifted twice, its relative weight is four times that of the first group. Thus, "adding twice" for the second group means "adding eight times." Combining the two groups, the result is "add seven times the multiplicand." This method requires only six easy operations: ± 0, $\pm X$, $\pm 2X$.

Every two contiguous groups have one bit in common as follows.



This padded 8-bit multiplier is divided into four groups, each made up of three bits. Each of the groups is operated upon by encoding the previous definitions. However, each group has a different weight. Group A has a weight of 1, group B a weight of 4, and so on. Note that bit -1 is always 0.

Thus the modified Booth's algorithm is a multiplier encoding scheme that involves a constant shift of two bits at a time while examining three multiplier bits, resulting in N/2 partial products rather than the N partials involved without encoding. This algorithm can be extended by shifting three bits at a time while examining four bits at each subgroup. However, in encoding some permutations of a 4-bit string, such as 0110, the partial product is three times the multiplicand. Since generating a multiplication of three is not as trivial as the shifting used in generating a multiplication of two, none of the semiconductor multipliers use more than three bits for encoding.

The second type of multiplication algorithm deals with adding the partial products. All parallel algorithms use the carry-save adder; this adder is identical to a

TABLE 4

Comparison of Available Multiplier ICs

Vendor/ Device	Configuration	Pins	Speed	Power	Data Code	Amount of Parallelism	Algorithm
TRW/ MPY-8	8 x 8	40	130 ns	1.2 W	2's comp	Full	AND gates and carry-save adders
TRW/ MPY-12	12 x 12	64	150 ns	3.5 W	2's comp	Full	AND gates and carry-save adders
TRW/ MPY-16	16 x 16	64	180 ns	5 W	2's comp	Full	AND gates and carry-save adders
MMI/ 67558	8 x 8	40	100 ns	1 W	2's comp/ unsigned	Full	Modified Booth's; modified Wallace Tree
MMI/ 67516	16 x 16	24	800 ns	1 W	2's comp	Multiplicand/ 2 multiplier bits	Modified Booth's
MMI/ 67508	8 x 8	20	400 ns	0.75 W	2's comp	Multiplicand/ 2 multiplier bits	Modified Booth's
AMD/ 25S05	2 x 4	24	25 ns	0.6 W	2's comp	Full	Booth's
AMD/ 25LS14	8 x 1	16	50 ns	0.5 W	2's comp	Multiplicand/ 1 multiplier bit	Booth's
AMD/ 25LS2516	8 x 8	40	400 ns	1 W	2's comp	Multiplicand/ 2 multiplier bits	Modified Booth's
TI/ 74S274 (ROM)*	4 x 4	20	50 ns	0.5 W	Unsigned	Full	ROM lookup table*
Motorola/ 10183	2 x 4	24	20 ns	0.8 W	2's comp	Full	Booth's

*When used with companion device 74S275, partial products are added in a Wallace Tree configuration

TABLE 5

Performance Comparison Between 8 x 8 and 16 x 16 Multiplication

			8 x 8 Multiplication			16 x 16 Multiplication		
Vendor/ Number	Configuration	Pins	No. of Packages	Speed	Power	No. of Packages	Speed	Power
MMI/ 67558	8 x 8	40	1	100 ns	1 W	14*	140 ns	9 W
TRW/ MPY-8	8 x 8	40	1	130 ns	1.8 W	14*	170 ns	10 W
Motorola/ 10183	2 x 4	24	8	50 ns	6.4 W	32	100 ns	25.6 W
AMD/ 25S05	2 x 4	24	8	75 ns	5 W	32	150 ns	20 W
TI/ 74S274	4 x 4	20	12**	75 ns	5.4 W	45	120 ns	21 W
TRW/ MPY-16	16 x 16	64	—	—	—	1	180 ns	5 W
MMI/ 67516	16 x 16	24	—	—	—	1	800 ns	1 W
AMD/ 25LS2516	8 x 8	40	1	400 ns	1 W	2	800 ns	2 W

*4 packages are 8 x 8 multipliers, 10 are adders (74S181/10181)
**4 packages are 4 x 4 multipliers, 8 more are Wallace Tree bit-slices (74S275)

binary full adder. The only difference is in the interconnections of carries; instead of waiting for the carry to ripple, the carry is added at a later stage. Postponement of the addition of carries can be extended to all adder stages except the last. Carries from the last stage essentially form an n-bit operand to be added to the n-bit sum, and this operation can be done by carry-lookahead adders. Another side benefit of postponing addition of the carries to a later stage is the availability of a third input in each adder in the first stage; thus, the first three partial products can be added by the first stage, reducing the number of adder stages by one. This scheme is a minor modification of the Wallace Tree.[11]

Table 4 summarizes available IC multipliers and the algorithms that they use. For example, the TRW multipliers[12] use AND gates to generate partial products which are added by carry-save-adders, however (unlike the Wallace Tree), they let the carries ripple through the last adder stage.

The MMI 8 x 8 multiplier[13] (67558) generates partial products by using the modified Booth's algorithm. These partial products are then added in a Wallace Tree configuration. Texas Instruments extends the AND gate concept and provides a ROM (74S274) to generate a 4 x 4 segment of the partial products. They also provide a 7-bit Wallace Tree slice (74S275) for use in adding the partial products. This bit-slice can be used with other multipliers to provide an expanded multiplication. AMD 25S05[14] and the Motorola 10183 provide an onchip solution to the expansion problem by implementing X times Y plus K instead of just X times Y.

Some multipliers in Table 4 are semiparallel. The AMD 25IS14 generates and accumulates one partial product at each clock pulse; this product is made up of one multiplier bit and the full width of the multiplicand. Thus, for 8 x 8 multiplication, eight clock pulses are required. The MMI 67516 is similar except that it shifts two bits at a time and the multiplicand is 16-bits wide. Thus, 16 x 16 multiplication is performed in eight cycles.

Table 5 compares performance of the various chips in performing 8 x 8 and 16 x 16 multiplication, and can be used to make the engineering tradeoff in system design of multiplication. If maximum speed is needed, say for 8 x 8 multiplication, then using eight packages

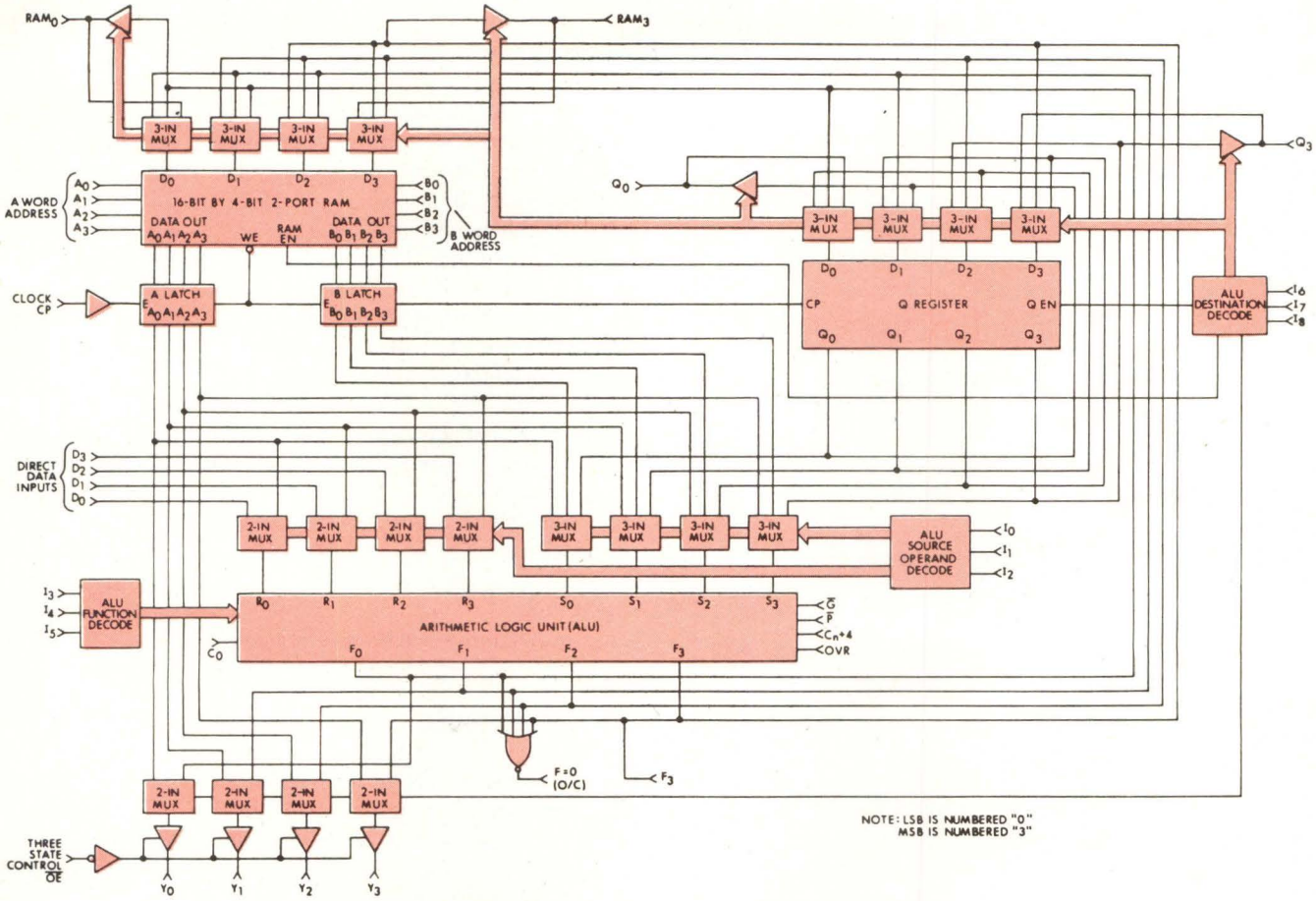


Fig 1 Detailed AM2901 microprocessor block diagram. Main element of 2901 is ALU, which performs eight operations according to three instruction lines. Source and destination of operands and results are determined by remaining six instruction lines. Register file, in upper left corner, is 16 x 4 dual-port RAM, which is used as 16 registers or accumulators for ALU. External input and output data buses are also used as source and destination, respectively

of the ECL 10183 is the best choice; however, if the associated power dissipation of 6.4 W is excessive, the single chip MMI 67558 is best. While it multiplies somewhat slower than the ECL device, its power dissipation is only 1 W.

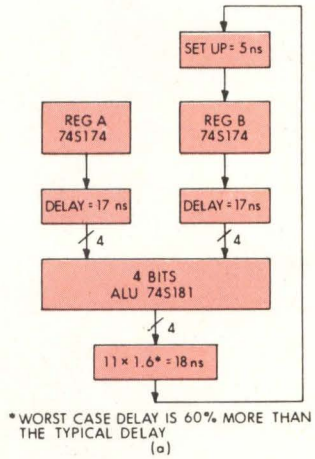
Bit-Slice Processor Elements

The first arithmetic IC was a binary adder, which was integrated later to the combinatorial ALU (74181). The next evolution of integration (after the ALU) received many different names, such as bit-slice microprocessor, RALU (ALU with registers), and data slice. The former is the most popular description. Architecture of the bit-slice is made typically from the classic ALU, but with multiple accumulators (registers) and control over ALU sources and destination. Fig 1 shows the architecture of the AMD-2901,[15] which is probably the most commonly used bit-slice processor element. Other such elements are Motorola MOT 10800, MMI 6701, Intel 3000, TI 74S481, and TI SBP 400. All have four bits per IC, except the Intel 3000 which is only two bits wide.

To determine the speed of these devices, the register to register operation ($R_A + R_B \rightarrow R_B$)* is examined. The 2901A, a faster version of the 2901, performs such an operation in 90 ns. To compare this speed with that of the 74181 type ALU, it is necessary to add registers to the 74181, as shown in Fig 2.

Expanding the bit slices to handle more than four bits is similar to expanding the 74181 ALUs. In fact, most bit-slice vendors recommend using the same carry-lookahead unit (74S182). To get a more realistic picture of the actual throughput of these devices, it is necessary to assume some overall system of architecture. Fig 3 shows the architecture for a 16-bit system. It is assumed to be microprogrammable with a pipelined microinstruction register; ie, maximum speed is achieved when no branch decisions are made. Fig 3 also contains a comparison of 16-bit throughput for various building blocks. In computing the addition time of the ALUs

*$R_A + R_B \rightarrow R_B$ means adding the contents of register A to the contents of register B and storing the sum into register B. All of this is accomplished in one cycle.



ECL	S/TTL	LS/TTL
10800	74S181	2901A
15 ns	40 ns	90 ns

(b)

Fig 2 MSI emulation of bit-slice processor element. (a) To compare simple ALU with bit-slice processor element, two registers are added to ALU. (b) Time to perform four bits ($R_A + R_B \rightarrow R_A$) is tabulated for various building blocks

(74S181 and 10181), the configuration assumed is similar to that of Fig 2, with the addition of a multiplexer (to select one of several sources) and a microinstruction register. From Fig 3(b) it can be seen that the speed of the arithmetic processor elements is about half that of the older ALUs. This ratio applies to both TTL and ECL technologies. Slower speed of these elements is probably the main reason that many recent minicomputers still use the older ALUs.

Monolithic Arithmetic Processors

The MMI 67516 (mentioned in the discussion on multipliers) continues the trend toward greater integration per chip. In addition to multiplication, the device performs division using a nonrestoring algorithm; thus, for 16-bit division, 20 clock pulses are needed. At 100 ns/clock, 2 μs are required to perform a division of a double-length dividend by a single-length divisor, resulting in a single-length quotient and remainder. The device contains four registers, two of which are used as accumulators, making it easy to perform (under microprogram control) a variety of operations, including sum of products, multiplication by constant, and division by constant.

Development of this device was originally motivated by speech processing requirements, where 16-bit multiplications performed in 1 μs are used to implement digital filter equations. Later, it was realized that most of the data paths and registers needed for division already existed; this allowed division capability to be incorporated into the chip with a small increase in hardware and expansion of the microprogram.

Future Trends

To provide perspective on currently available arithmetic ICs, the limitations imposed by bipolar technology were analyzed. Now to understand the future of arithmetic ICs, bipolar technologies must be examined in terms of potential density and speed.

Two major density improvements are in sight. The first is an increase of the wafer diameter from 3 to 4 in (7.6 to 10.1 cm). This increase, which has been implemented by some companies, doubles the chip size while maintaining the same cost (up to a limit, the cost of processing a wafer is almost independent of its diameter). The second, more revolutionary, improvement is a new method of drawing the patterns needed for the fabrication of integrated circuits. Resolution currently obtained with optical lithography is lines approximately 2 to 5 μm wide. Further resolution in optical techniques is limited by diffraction effects that occur between the mask and the wafer. The new method—electron-beam lithography—provides up to 20 times the resolution of optical lithography.[16]

With these improvements, Texas Instruments expects to achieve a chip size of 140,000 sq mils.[17] With IIL technology, this chip size will contain about 10,000 gates. At this high level of integration, many arithmetic ICs will probably give way to a single-chip high speed microprocessor that performs addition, multiplication, and division all at the same speed. Thus, one direction in the future will be further integration of multichip systems into a single chip while maintaining the same system speed.

A second possible future trend will be to retain the same level of integration but to employ higher speed technology. A new bipolar process—elevated electrode integrated circuit (EEIC)[18]—is reported to have 250-ps delay/gate at 2-mW power dissipation. With such a technology (still under research and development), it

(b)

ECL		S/TTL	LS/TTL	IIL
10181	10800	74S181	2901A	SBP400
32 ns	62 ns	68 ns	143 ns	300 ns

(a)

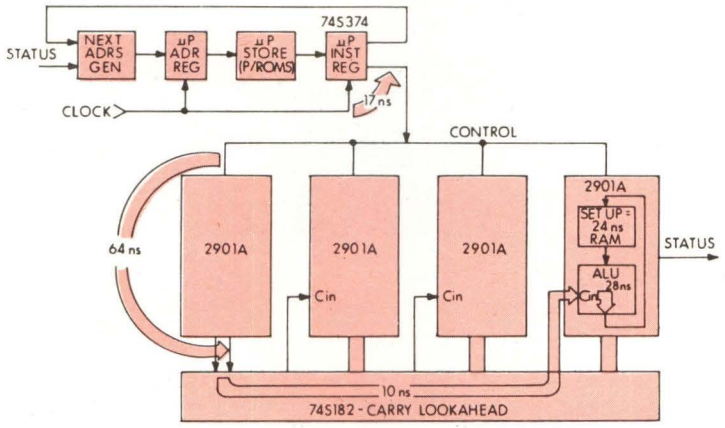


Fig 3 Architecture and performance of microprogrammable system. (a) Microprogrammable system (16 bits) made up of 2901s. For simplicity, data bus is not shown. (b) Comparison of minimum time to perform $R_A + R_B \rightarrow R_B$ for 16-bit systems made up of different building blocks

will be possible to construct an ALU that is functionally similar to the 74S181, but with an order of magnitude speed improvement, ie, 1 ns. A 16-bit computer made with this ALU and carry-lookahead units could perform register to register addition in 7 ns, if a sufficient variety of devices in the new family exist to build such a computer.

The future directions outlined are merely interpolations of the progress to date. As with the microprocessor revolution, it is possible that a completely new direction in computer arithmetic will emerge from the continuing advancements in IC technology.

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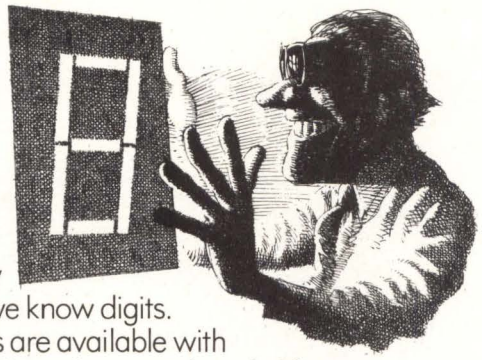

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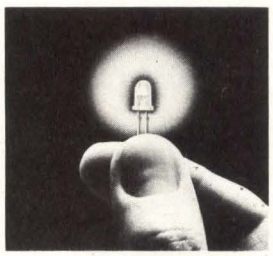

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A simple, easily-implemented protocol has been designed to detect and correct noise-induced errors in a bit-serial link, and to hold transmissions at a rate acceptable to the receiver

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When first developed in the mid-1960s, the Octopus computer network[1] comprised a few very large computers linked by custom-built high speed bit-parallel interfaces. As expansion occurred, numerous widely dispersed minicomputers were added. The economics of the growing system dictated the use of low cost bit-serial hardware devices on longer, relatively low bandwidth links. However, the simplicity of the serial link hardware was offset by the need for more complex software or firmware. As an example of the problems: control and status information were no longer neatly segregated from data into different parts of the interface; they were intermixed into a single stream of bits that had to be unambiguously sorted out by the receiver. Also, the hardware reported noise-induced transmission errors only to the receiver, which then had to request retransmission.

A serial communication link protocol was needed to sort out and handle these problems. However, after examining problems and solutions in the late 1960s, the suggested standard protocol at that time[2] was deemed excessively complex—and it did not permit movement of data, simultaneously in both directions, on a link. Therefore, to answer system requirements, a simple serial communication link, the Octopus protocol, was designed.

At present, nearly all computing resources at Lawrence Livermore Laboratory are tied together by the Octopus computer network. It provides a common shared data base, and permits maximum interaction with, and availability of, all resources at each interactive terminal.

Link Protocols

Flexibility and generality of data communication activity within a computer network are enhanced if a hierarchy of modular and somewhat independent communication protocols, rather than one that is all-encompassing, are used. Proceeding down the protocol hierarchy involves moving from higher-level rules and formats concerned with the meaning and disposition of messages, toward lower-level conventions concerned with the mechanics of transmission.

The Octopus protocol is designed for a full-duplex serial link, which connects two nodes so that two independent transmissions, one in each direction, can occur simultaneously, even though each transmission may consist only of a single serial stream of bytes. A link with different characteristics, such as one that can carry only one transmission at a time, or one with separate parallel paths for data, control, and status, would require a different link protocol.

Generally, a single message that moves from its originating node through several intermediates to its destination (Fig 1) may be subjected to a different link protocol on each link used. The same message is also subjected to a single, higher-level, end-to-end protocol that is inde-

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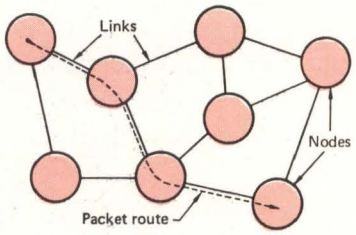

Fig 1 Serial communication network. Packet originating in upper left node, destined for lower right node, passes over three links and through two intermediate nodes to follow shortest route

pendent of the kinds of links used. Such a protocol typically operates by generating, interpreting, altering, and discarding headings that contain information regarding routing, sequencing, assurance of delivery, flow control, and logical blocking. Headings, included with each message in addition to the text, must be conveyed without change from the origin to the destination.

The end-to-end protocol interacts with the link protocols by using packets, each consisting of a heading and some text. Whether the text is a single complete message, part of a message, or several messages is determined by the higher-level protocols and does not concern the link protocols, which do not interpret the packet content. As determined by the end to end protocol, a packet generated by or arriving at a node is placed onto a queue of packets associated with the link over which it is to be output. Packets in this output queue are transmitted one by one over the link in accordance with the link protocol; a packet is retransmitted whenever a transmission error occurs. When a packet is correctly input by the node at the other end of the link, it is examined according to the end-to-end protocol to determine its disposition. In a typical node, the only aspects of a packet that are of interest to the link protocols are the locations and lengths of the chain of data buffers (or the single data buffer) where the packet is stored.

The Octopus link protocol consists of two nearly independent sub-protocols: block and byte. Block protocol is the higher level of the two and concerns matters that require action only at packet boundaries, namely, recovery from error and determination of readiness to input or output. This protocol would typically be implemented in software or perhaps in firmware. Simplicity is the outstanding advantage of this protocol. As compared to alternatives it requires less programming, working storage, and running time, which makes it ideal for use in small computers, or where programming effort must be minimized. However, simplicity leads to certain limitations, such as the fact that each packet must be acknowledged before the next is output, which may lower throughput to some extent.

The byte protocol provides synchronism maintenance, identification of packet boundaries, and error detection, all functions that require the examination of each 8-bit byte as it is sent or received. Byte rather than bit orientation represents a slight reduction in generality but results in considerable flexibility. The protocol can be used on asynchronous serial links using standard, simple, byte-oriented interfaces. Also, on synchronous serial links, the hardware only need search for synchronizing bytes at the start of each transmission; there is no need, as with some protocols,[3] for special hardware that inserts and deletes bits within a byte of data. Essentially the entire protocol can be implemented in software or firmware, although it can also be fully implemented in hardware to increase throughput or to reduce processor program load.

Block Protocol

To transmit a packet over a serial link without error when both ends are ready, control and status information about the packet must be sent in both directions over the link. A major effort in designing the block protocol, which manages control and status information, was devoted to minimizing the quantity of information in order to achieve the greatest simplicity. The effort succeeded because the information was compressed to a single 8-bit control byte per transmission. As explained later, this permits good meshing with the byte protocol, which provides a natural place for the byte in a transmission sequence. The control byte in each transmission is generated, interpreted, and discarded according to the block protocol. Specifically, the block protocol views each transmission over the link as being a data packet accompanied by a control byte, or only a control byte.

For each packet there is an outputter node at the end of the link that originally had the packet, and an inputter node at the other end that finally gets the packet. These terms must be distinguished from "sender" and "receiver", which are used in the conventional way to distinguish the two ends of a single transmission, for a control byte sent in one direction may contain information about a packet output in the other direction. Because the link is full duplex for output and input as well as for sending and receiving, two packets may be transmitted independently and simultaneously in opposite directions over the link. Therefore the algorithms used by the nodes at the two ends of the link can be identical; there is no need, as there is with some protocols,[2] for a slight asymmetry to resolve a conflict between ends that try to transmit over the link simultaneously.

The block protocol is centered around the content of the control byte (Fig 2). This byte always contains a current record of the status of the sender with regard to both input and output. The protocol is such that failure to receive a control byte may result in a need to retransmit a packet, but it cannot lead to permanent confusion. Three of the eight bits in the byte are input status (bits 6, 5, and 4), three are output status (bits 2, 1, and 0), and two provide redundancy (bits 7 and 3); bits are numbered starting with 0 on the right.

Bit 6, the input phase bit, and bit 2, the output phase bit, indicate node phases. At any given time, a node is

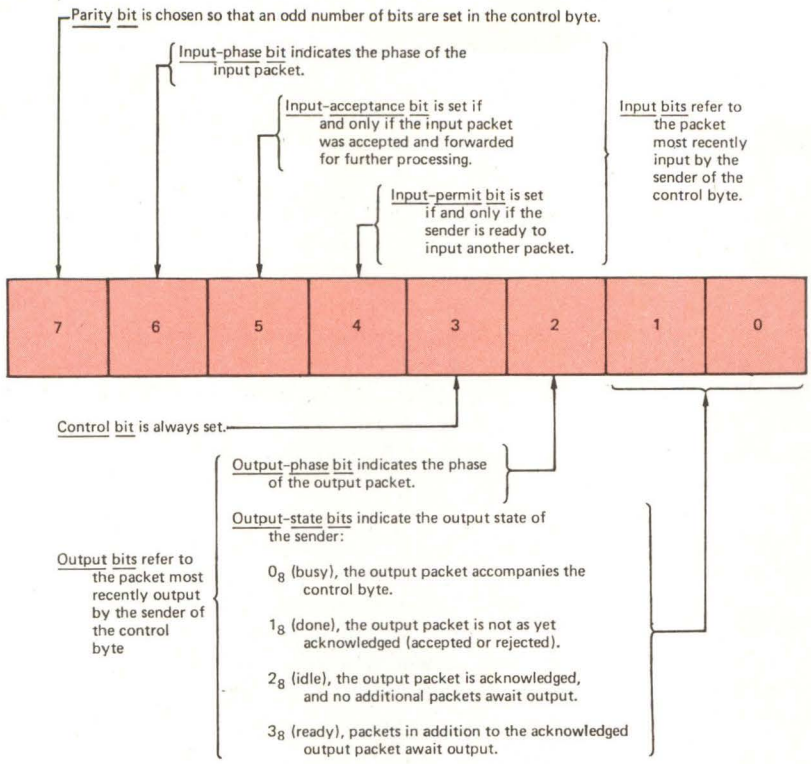

Fig 2 Control byte format. This byte is included in every transmission. Phase is modulo-2 counter (counting 0, 1, 0, 1, . . .) of transmitted packets

in one of two phases (0 or 1) associated with output and also in one of two phases (0 or 1) associated with input. In each case, the phases alternate as successive packets are transmitted. Change in a node's output phase occurs whenever it sends a packet, while the input phase is always made to conform to the output phase most recently received (without error) from the other node. A phase is essentially a modulo-2 packet counter (counting 0, 1, 0, 1, . . .) used to prevent confusion about which packet's status is being indicated.

The eight bits of a control byte are explained from high to low order.

Bit 7—parity bit—is selected so that the total number of bits set in the control byte is odd, providing redundancy for this highly critical byte in addition to the error-detection facilities of the byte protocol.

Bit 6—input-phase bit—indicates the input phase of the sender.

Bit 5—input-acceptance bit—is set if, and only if, the packet input by the sender during its current input phase was accepted, that is, was received without error and forwarded for further processing according to higher-level protocols. A packet is received with error if it is part of an erroneous transmission (defined in discussion of bit 3) or is accompanied by an improper output state (defined in discussion of bits 1 and 0).

Bit 4—input-permit bit—is set if, and only if, the sender is prepared to input a new packet (during its next input phase).

Bit 3—control bit—is always set to prevent a possible ambiguity in the byte protocol, and constitutes the only specific adaptation of block to byte protocol. A transmission is judged to be erroneous and its contents ignored if the byte protocol detects an error, the parity of the control byte is even, or the control bit is clear.

Bit 2—output-phase bit—indicates the output phase of the sender.

Bits 1 and 0—the output-state bits—indicate the state of the sender with regard to output.

If the output-state bits are equal to 0_8 (the two bits are represented as a single octal digit), indicating the busy state, the control byte accompanies a packet. The receiver should accept a packet only if it is in a non-erroneous transmission with a control byte that shows a change in the sender's output phase from its previous value, which has been remembered as the receiver's input phase, and shows an output state of 0_8. The acceptance or rejection of the packet is indicated by the input-acceptance bit (bit 5) in a control byte that shows the proper input phase, sent from inputter to outputter. Because the contents of an erroneous transmission are ignored and the output phase shown in its control byte is not examined, acceptance or rejection is decided upon receiving the first non-erroneous transmission that shows a new output phase, which is the transmission that causes a change of the receiver's input phase. An indicated output state of 0_8 causes acceptance; any other output state causes rejection. The decision of acceptance or rejection is then not altered until the phase changes again.

If the output-state bits are equal to 1_8, indicating the done state, the sender has not, during the current output phase, received an acknowledgement (indication of acceptance or rejection) of a packet; that is, he has not received (without error) a control byte showing an input phase equal to its own output phase. This state differs from the 0_8 state in that no packet is included in the transmission. During each output phase, an outputter normally sends a packet once, in a transmission showing the 0_8 state, and then shows the 1_8 state in subsequent transmissions (if any) sent before receiving an acknowledgment. However, the outputter could repeat the packet and show the 0_8 state in subsequent transmissions; any duplicate packets would be ignored by the inputter, since they would not be associated with a change of output phase. If a packet is rejected during one output phase, it can be output again during the next phase, and the process is repeated until the packet is accepted or a decision is made to give up because outputting has taken too much time.

If the output-state bits are equal to 2_8, indicating the idle state, the sender has received an acknowledgment of the packet output during its current output phase but has no further output waiting to be sent; that is, the output queue is empty.

If the output-state bits are equal to 3_8, indicating the ready state, the sender has a packet ready to be output during its next output phase and is waiting for input permission from the receiver. Permission is indicated by the input-permit bit (bit 4) in a control byte, which shows the proper phase, sent from the inputter to the outputter. Always permitting input, except in rare circumstances of failure or overload, is most efficient, because the transmission of a packet is followed by only one additional transmission (in the opposite direction), containing the acknowledgment, and the acknowledgment could be included with a packet going in that opposite direction. If input permission is given only after receiving an indication of output state 3_8, two more transmissions (one in each direction) precede the output of every packet. During each output phase, the output state should always change in sequence from 0_8 (busy) to 1_8 (done) to 2_8 (idle) to 3_8 (ready). However, the protocol permits some of these states to be skipped, but never all.

The records that must be kept by a node to carry out the block protocol are summarized in Fig 3. In addition to the six bits (bits 6, 5, 4, 2, 1, and 0) of its output and input status included in every control byte that it sends, a node must keep three more single bits of information on which to base its decisions: the send-permit, send-request, and output-permit bits. The send-permit bit, if set, indicates that the situation has changed since the last transmission and that the need for a new transmission should be examined. This bit is cleared whenever a transmission is sent, and is set whenever a transmission is received or when a new packet appears at the head of the output queue. The send-request bit, if set, indicates that the node at the other end of the link would like to receive a control byte. This bit is cleared and set along with the send-permit bit, except that the send-request bit is cleared whenever a nonerroneous transmission is received that indicates an output state of 2_8. Provided that sending is not already in progress, a node should send a transmission whenever the send-permit bit is set and at least one of the following is true: the send-request bit is set, or the node's own output state is not 2_8. The output-permit bit determines, in part, whether a transmission should include a packet. This bit, if set, indicates that the received input-permit was set during the current phase and, therefore, that the next packet in the output queue may be output.

A node should also operate an output and an input timer. The output timer is used to ensure that each packet in the output queue is transmitted and accepted within a reasonable time, the length of which is determined by considering the transmission rate of the link, the reaction time of the nodes, and the possibility of an error that would require a retransmission. The input timer is used to ensure that input buffers do not remain indefinitely allocated for a packet that may never arrive; the need for this timer depends on the details of the implementation. Records kept by a node also include the

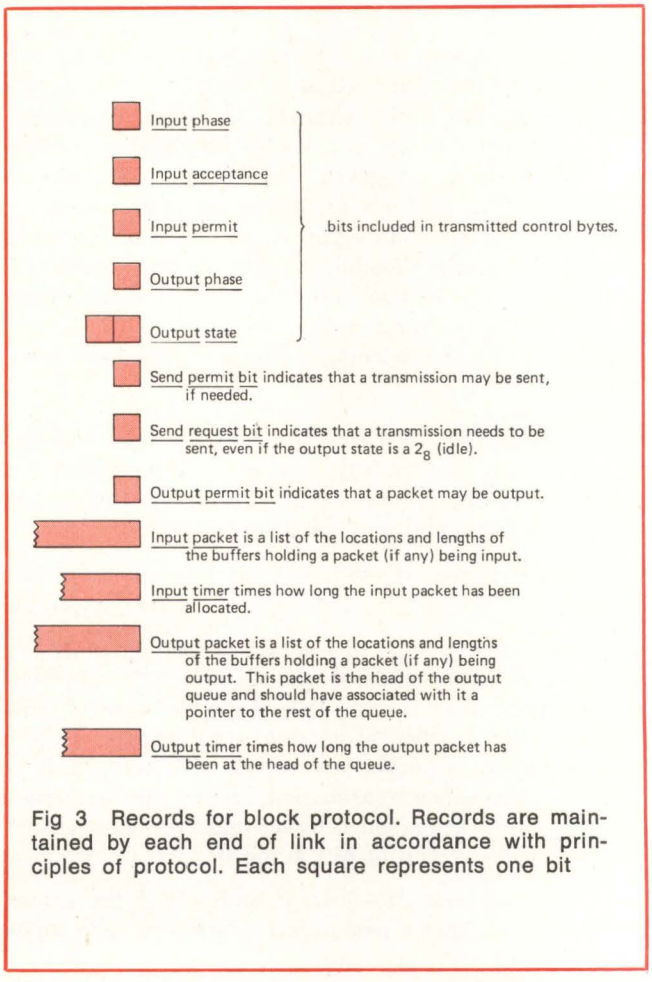

Fig 3 Records for block protocol. Records are maintained by each end of link in accordance with principles of protocol. Each square represents one bit

locations and lengths of the buffers that hold the input and output packets.

On the basis of the outlined data communication principles, a suitable algorithm for the block protocol has been constructed (Panel A).

Byte Protocol

The major decision in designing this byte protocol was how the end of a transmission should be indicated. There were two basic choices: either to precede each transmission with a byte count,[4] or to mark the end of the transmission with a flag byte.[3] The latter scheme was selected, primarily because transmission errors inevitably occur and some will affect the mechanism for detecting the end of transmission. If, in the unselected scheme, the receiver should misinterpret the byte count, even if it knows on the basis of redundancy checks that it misinterprets, it would have great difficulty in locating the beginning of the next transmission. The recovery mechanism must ultimately rely that there is a maximum length transmitted packet. While collecting and discarding the maximum number of implied bytes, the receiver may overlook many valid transmissions and cause unnecessary delay. In the scheme chosen, on the other hand, if a receiver does not recognize a flag byte and runs past the end of a transmission, it will be stopped by the flag byte at the end of the next transmission.

The byte protocol uses three special bytes: the SYN (synchronous idle, 026_8) byte that begins every transmission to provide byte-frame synchronization on a synchronous link; the SOH (start of heading, 001_8) data-flag byte that marks the start of a packet; and the DLE (data link escape, 020_8) control-flag byte that marks the end of a packet. The bit patterns of these bytes were chosen to be compatible with the ASCII character set,[5] but their important features are that each has odd-parity, and that bit 3 is clear, assuring compatibility with the block protocol.

A transmission is made up of the following sequence of bytes (Fig 4): a few synchronizing bytes (three or more SYNs on a synchronous channel, perhaps none on an asynchronous channel); the data flag (SOH); the bytes of a data packet (if any); the control flag (DLE); the control byte (any byte except DLE or SYN); and two check bytes that comprise a 16-bit redundancy check over all the bytes in the transmission starting with the SOH data flag. If there is no packet in the transmission, the SOH data flag and the DLE control flag are adjacent.

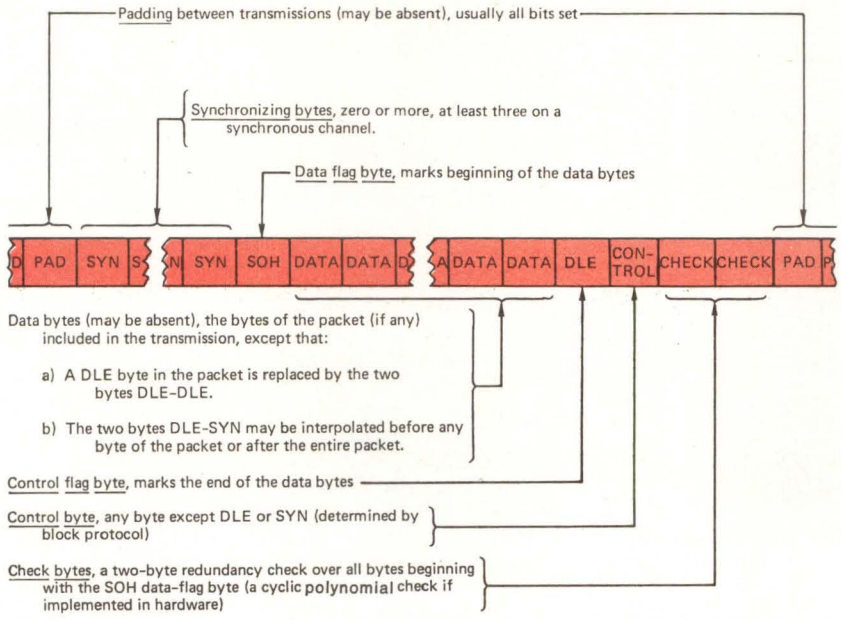

Fig 4 Byte protocol sequence. Each transmission consists of indicated (left to right) sequence of bytes. Data and control bytes are supplied by the block protocol, while others are generated by byte-protocol sender and discarded by receiver

PANEL A.

Block Protocol Algorithm

This algorithm is expressed in a colloquial dialect of ALGOL. Words that direct the flow of control through the algorithm are in boldface, and their scope is indicated solely by how they are indented. That is, alternative actions are indented further than the **then** and **else** that label them, and the **then** and **else** are equally indented beyond the **if** that chooses between them. Logical combinations of conditions following an **if** are made with **and, or,** and **not.** Comments begin with *comment* and are enclosed in brackets. Except for a terminal statement that goes to the beginning of the algorithm, the use of **go to** constructions has been avoided at some reduction in efficiency so that the algorithms will perhaps be easier to understand.

Comment: The block protocol algorithm is initiated at this point by an input or output timer or a Receiver or Sender byte protocol interrupt condition. An interrupt condition persists until its cause is removed or it is disabled.

if interrupt by input timer
  then
    abort Receiver [*comment:* This soon causes a Receiver byte protocol error since Receiver interrupt is always enabled.]
    stop input timer [*comment:* A stopped timer does not interrupt.]
if interrupt by Receiver byte protocol
  then
    if not chaining point
      then [*comment:* Normal end of transmission, byte protocol error, or no action.]
        send permit ← 1 [*comment:* Permit sending.]
        send request ← 1 [*comment:* Tentatively require sending.]
        if byte protocol error **or** no action
          then [*comment:* No-action interrupt is a spurious condition.]
            reinitialize Receiver [*comment:* Clear effects of error.]
          else [*comment:* Normal end of transmission.]
            if received control bit (control byte bit 3) = 1 **and** parity of received control byte = odd
              then [*comment:* Transmission is not erroneous.]
                if received input phase (control byte bit 6) = own output phase
                  then [*comment:* Treat received input bits, which refer to own output.]
                    output permit ← received input permit (control byte bit 4)
                    if own output state = 1_8 (done)
                      then [*comment:* Acknowledgement just received has been awaited.]
                        own output state ← 2_8 (idle)
                        if received input acceptance (control byte bit 5) = 1
                          then [*comment:* Output packet has been accepted.]
                            discard output packet [*comment:* Next packet (if any) moves up in output queue.]
                            initialize value of output timer.
                if received output phase (control byte bit 2) ≠ own input phase
                  then [*comment:* Treat received data packet.]
                    own input phase ← received output phase (control byte bit 2)
                    own input permit ← 1 [*comment:* This bit is always set because this algorithm assumes that buffers will be available when needed for further input. Alternatively, the bit could be cleared at this point if no more input buffers will be available and then set at a later time when they become available.]
                    if received output state (control byte bits 1, 0) = 0_8 (busy)
                      then [*comment:* Data packet is accepted.]
                        own input acceptance ← 1
                        make input packet available to higher level protocols for further processing [*comment:* Those protocols will ignore a packet that is too short (perhaps even of length zero) to contain a complete heading.]
                      else [*comment:* Data packet is rejected.]
                        own input acceptance ← 0
                if received output state (control byte bits 1, 0) = 2_8 (idle)
                  then send request ← 0 [*comment:* Sending not required.]
              discard input packet (if any)
              stop and initialize value of input timer [*comment:* Prepare for timing next input packet.]
              indicate to Receiver that it should interrupt for chaining at next data byte
              enable sender byte protocol interrupt [*comment:* If Sender is inactive, this causes a no-action interrupt; otherwise it has no effect.]
      else [*comment:* Chaining point.]
        start input timer [*comment:* This has no effect if timer is already running.]

```
            if buffer is available from free buffer pool
              then
                allocate additional buffer for input packet
                indicate buffer address and byte count to
                Receiver
                indicate to Receiver that data is to be
                    transferred [comment: Data transfer
                    is assumed to be disabled at time of
                    interrupt.]
                if maximum number of buffers have been
                    allocated for input packet
                  then indicate to Receiver that there is
                      no further chaining.
                      [comment: Chaining is assumed
                          to remain enabled at time of
                          chaining interrupt.]
              else indicate to Receiver that there is no
                  further chaining
                  [comment: Since data transfer is dis-
                      abled, Receiver will immediately
                      interrupt with a data-buffer over-
                      flow error.]
          indicate to Receiver that it should proceed
if interrupt by output timer
  then
    abort Sender
    enable Sender byte protocol interrupt
    stop output timer [comment: A stopped timer does
        not interrupt.]
if interrupt by Sender byte protocol
  then
    if not chaining point
      then [comment: Normal end of transmission,
          byte protocol error, or no action.]
        if byte protocol error or both no action and
            output timer timed out
          then [comment: Algorithm gives up on out-
              put.]
            dispose of entire output queue, including
                output packet, according to higher
                level protocols
            send permit ← 1
            send request ← 1 [comment: Force a
                new transmission.]
        if own output state = 0s (busy)
          then [comment: A packet has just been
              output.]
            own output state ← 1s (done)
        if own output state = 1s (done) and output
            queue = empty
          then [comment: This situation may result
              when output queue is discarded after
              error or time out.]
            own output state ← 2s (idle)
        if own output state = 2s (idle)
          then
            if output queue = empty
              then [comment: No output packet.]
                stop and initialize value of output
                    timer [comment: Prepare for
                    timing next packet added to out-
                    put queue.]
              else [comment: Packet waiting to be
                  output.]
                own output state ← 3s (ready)
                send permit ← 1
        if output queue ≠ empty
          then start output timer [comment: This has
              no effect if time is already running.]
        if send permit = 0 or both send request = 0
            and own output state = 2s (idle)
          then [comment: No transmission need be
              made.]
            disable Sender byte protocol interrupt
                [comment: When Sender proceeds
                at the end of the algorithm, no fur-
                ther byte protocol action will take
                place until the interrupt is reenabled,
                at which time a no-action interrupt
                occurs. Higher level routines should
                enable the Sender interrupt after a
                packet is added to the output
                queue.]
          else [comment: Transmission is to be
              made.]
            initialize Sender to transmit
            if own output state = 3s (ready) and out-
                put permit = 1
              then [comment: Packet is to be out-
                  put.]
                own output state ← 0s (busy)
                own output phase ← ~ own output
                    phase
                if output queue = empty
                  then [comment: This situation may
                      result when output queue is
                      discarded after error or time-
                      out.]
                    own output state = 1s (done)
                  else [comment: Packet exists.]
                    indicate that next output buffer
                        should be first buffer of out-
                        put packet
                    indicate to Sender that chaining
                        should take place
                      [comment: Prepare for the
                          possibility of a multiple-
                          buffer packet.]
                output permit ← 0
            send request ← 0
            send permit ← 0
            indicate to sender the contents of the
                control byte to be sent, composing
                it out of own output state, own out-
                put phase, 1 as a control bit, own
                input permit, own input acceptance,
                own input phase, and an odd parity
                bit
        if own output state = 0s (busy)
          then [comment: Output state is always busy
              while chaining.]
            indicate next output buffer address and byte
                count to Sender
            if buffer is not empty (byte count ≠ 0)
              then indicate to Sender that data is to be
                  transferred [comment: Data transfer is
                  assumed to be disabled at time of
                  interrupt.]
            if buffer is last buffer of packet
              then indicate to Sender that there is no
                  further chaining [comment: Chaining
                  is assumed to remain enabled at time
                  of chaining interrupt.]
          indicate to Sender that it should proceed
wait for interrupt
go to beginning of block protocol algorithm
```

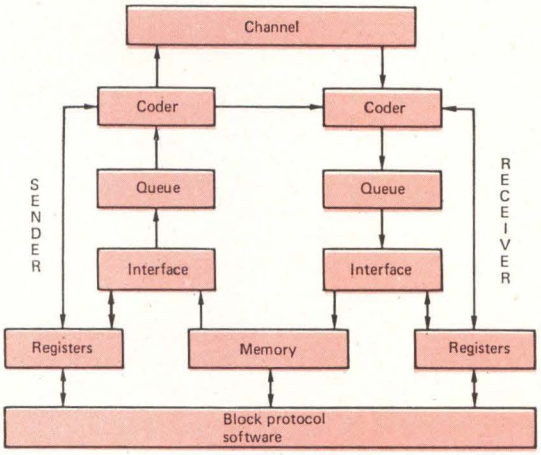

Fig 5 SCULL architecture. Block protocol software communicates with interfaces through sender and receiver registers. Coders interact with only few bits in registers and interact with each other only in maintenance mode. Sender data packets placed in memory by software, and control bytes from control-byte register are fetched by interface and passed through queue to coder, which inserts additional bytes required by byte protocol and sends information over channel. Coder for receiver receives information from channel and passes data packets and control bytes through queue to interface after discarding additional bytes used by byte protocol; interface places data packets into memory and control bytes into control-byte register, from which they are fetched by software

If a DLE occurs as a byte of the packet, it is transmitted as two successive DLE bytes (the data-repeat sequence), thus providing full transparency; that is, a packet can contain any sequence of bytes, including DLE bytes, without confusing the protocol. Also, within a packet, the 2-byte sequence DLE-SYN (the data-pause sequence) may be interpolated at any point by the sender to provide a delay; the receiver discards such sequences. The byte following the DLE control flag and preceding the two check bytes is used by the block protocol as the control byte. Because bit 3 of a control byte is always set, it can never be a DLE or a SYN; also, since a control byte, like DLE and SYN, has odd parity, a single bit failure in a control byte is always detected as an error. Therefore, there is no ambiguity in interpreting the byte following a DLE, even if there is a single-bit error that escapes the 16-bit redundancy check.

Note that two special bytes would have been sufficient for a viable protocol, although three are used to better conform to ASCII convention. The SYN byte could have been used in place of DLE, with DLE-DLE becoming SYN-SYN and DLE-SYN becoming SYN-SOH. The control byte would still have two forbidden forms, but these would be SOH and SYN, rather than DLE and SYN. It might appear that a more conventional and equally effective scheme for using only two kinds of special bytes would be to simply use DLE in place of SOH. This scheme is deficient in the case where an end of transmission is missed by the receiver, causing it to run on into the next transmission. The end of that next transmission would also be missed if it included no packet, because the two DLE bytes that would mark the start and end of a packet would be consecutive and, therefore, would be interpreted as a single DLE within a packet.

CONTROL BYTE REGISTER (read/write by software):

7	6	5	4	3	2	1	0

Contains control byte being sent or received; received control byte is placed in this register.

DATA ADDRESS REGISTER (read/write by software):

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Contains memory address of data byte next to be fetched from or stored into memory; incremented after byte is fetched or stored.

DATA BYTE COUNT REGISTER (read/write by software):

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Contains (twos-complement) negative of number of bytes remaining in current data buffer; incremented as byte is fetched or stored.

Fig 6 Three of four programmable registers used in hardware implementation of byte protocol. Each communication unit uses two sets of four registers, one for sender and one for receiver. Arrangement shown is used with DEC PDP-11 and is also applicable, with minor changes, to any 16-bit-word computer. Remarks under each register refer to interpretations and actions by hardware

Hardware Implementation

The block and byte protocols described have been used successfully in the Octopus computer network since the early 1970s. The block protocol has been implemented in software, while the byte protocol has been implemented both in software and hardware. Software implementation uses standard one-byte-at-a-time asynchronous teletypewriter interfaces; the check bytes are generated using an arithmetic checksum, which is efficient for conventional processors. Hardware implementation (Fig 5) is called the Serial Communication Unit for Long Links (SCULL)—a direct-memory-access device that executes the byte protocol. It interfaces to software that executes the block protocol through eight programmable registers—four for the sender and four for the receiver—as shown in Figs 6 and 7. Except for a maintenance mode, in which the receiver receives from its own sender, the sender and receiver are entirely independent, each consisting of two major parts: a coder and an interface. These parts communicate primarily by means of a first in first out (FIFO) queue, through which a sequence of packet data and control bytes pass. The queue is particularly important for a receiver because it can hold information that arrives on the channel while the software is taking action at a chaining point (the boundary between successive data buffers of a packet), or at the end of a transmission.

A coder is responsible for generating or interpreting the synchronization bytes (SYN), data-flag byte (SOH), data repeat (DLE-DLE) and data pause (DLE-SYN) sequences, control-flag byte (DLE), and two cyclic-poly-

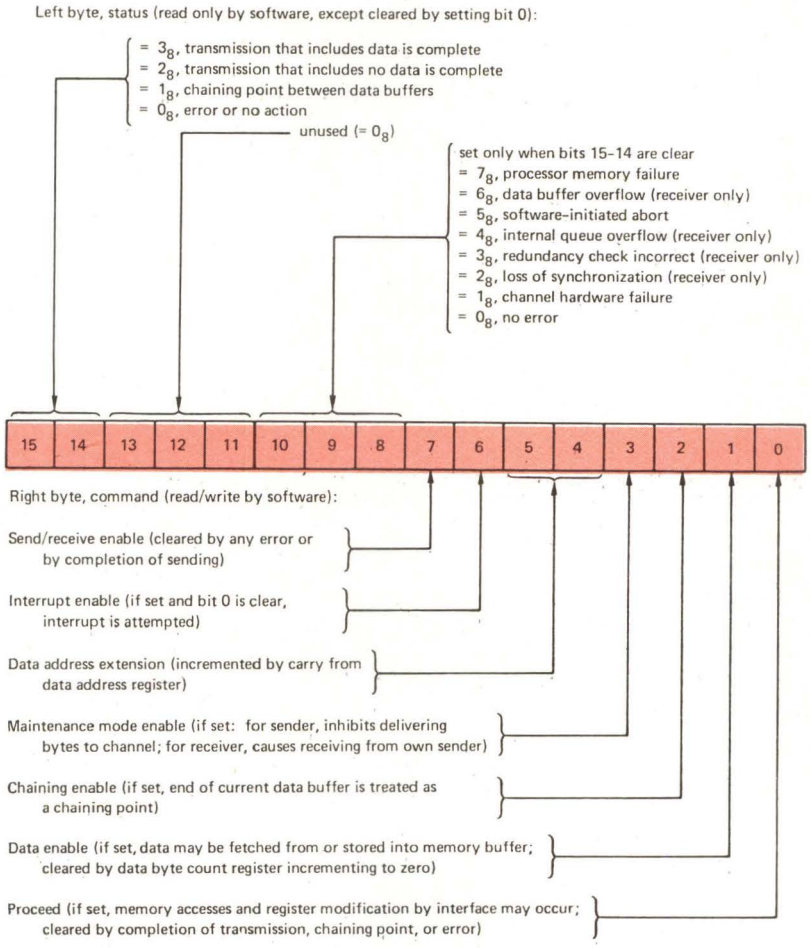

Fig 7 Command / Status Register format. This fourth programmable register is used in hardware implementation of byte protocol to convey various types of information between software and hardware. Remarks refer to interpretations and actions by hardware

nomial-check bytes. The sender coder properly intersperses these bytes among the sequence of data and control bytes obtained from the queue and sends the resulting sequence over the channel. The receiver coder discards such bytes from those received over the channel and places only the data and control bytes into the queue. An additional (ninth) bit, associated with each byte in the queue, is used to indicate whether the byte is data or control. The only software-accessible bits affecting coder action are the send/receive-enable bit (bit 7 of the command/status register shown in Fig 7), which must be set for the coder to operate, and the maintenance mode bit (bit 3 of the command/status register), which controls the connections among the two coders and the channel.

An interface is responsible for transferring data-packet bytes and control bytes between the queue and the memory or control byte register, incrementing the data address and data byte count registers as data are fetched from or stored into memory, managing most of the bits in the command/status register, and interrupting the processor whenever software intervention is required. The comments in Figs 6 and 7 provide a good overview of interface operation and of the programmer's view of the SCULL device.

SCULL is designed to be as independent as possible of the type of processor to which it is attached. Only the register layouts and the connections to the memory and I/O facilities of the processor need be changed when going from one processor to another; such changes will not affect the coders or the queues. The device is constructed with standard components, including universal receiver/transmitter and FIFO chips. High speed (hundreds of kilobits per second) is achieved because the implementation is entirely hardware. However, its logic is built around the concept of a finite state machine with transition rules that could be readily transcribed into a firmware (or software) algorithm.*

Conclusion

In the years since the Octopus link protocol was implemented, other more complex protocols have become commercially available.[3,4] These protocols usually offer greater generality, such as suitability for multipoint links. Most allow several packets to be sent before any are acknowledged, significantly increasing throughput on very long links, such as satellite links, that exhibit significant transmission delay. At least one of these protocols, associated with the international network interface standard X.25[6], will be implemented on some Octopus links.

However, the Octopus protocol remains unique in combining these features: simplicity of implementation; suitability for use with standard, inexpensive, byte-oriented, asynchronous I/O hardware; ready recovery when an error prevents properly recognizing the end of a transmission; and availability of a hardware implementation (SCULL) capable of throughput approaching 1M bits/s. Therefore, the protocol continues to be used within the Octopus network and on links between Octopus and remote micro- and minicomputers that do not provide the X.25 standard interface. Also, the Octopus block protocol is used to supplement the firmware protocols of a commercially-obtained, 50M-bits/s, multipoint trunk system that is being incorporated into Octopus. Finally, the protocol has been used as a vehicle for teaching the principles of serial-link communication.

*Interested readers may obtain a copy of Mr. Fletcher's algorithm for the byte protocol by requesting it in writing from the Editor, *Computer Design* Magazine.

Acknowledgement

The SCULL hardware was designed by Louis Harrold of the LLL staff.

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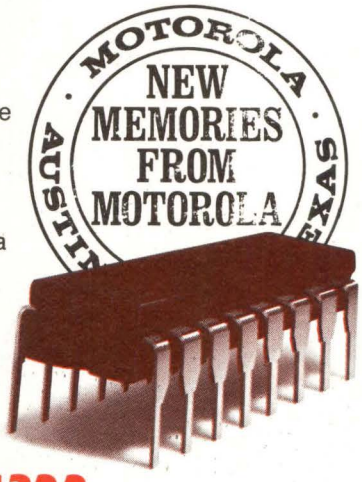

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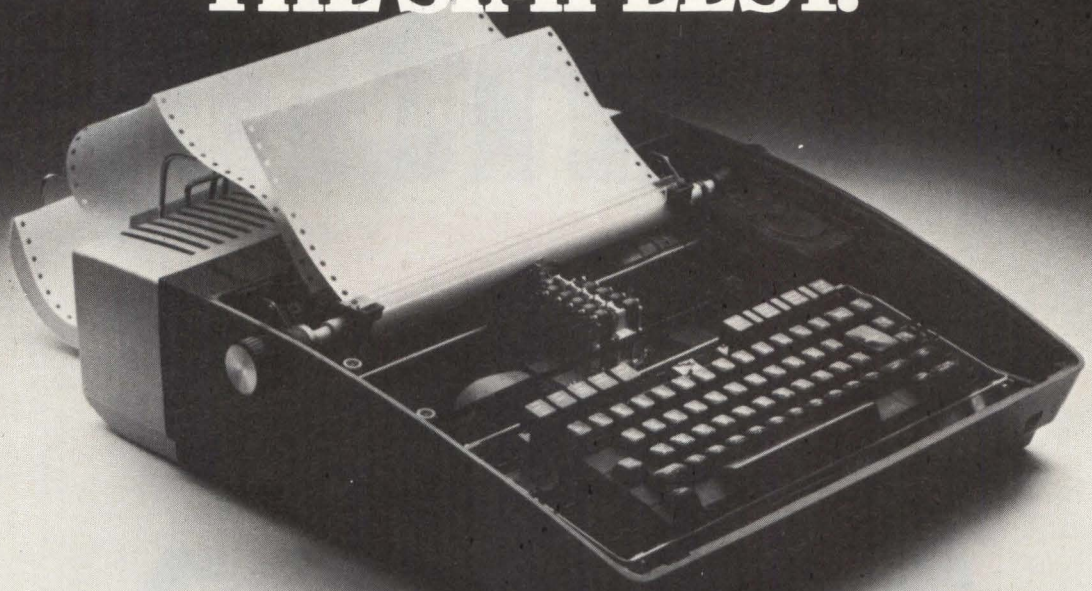

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PROVIDING SOFTWARE FLEXIBILITY FOR OPTICAL PROCESSOR NOISE ANALYSIS

Hardware/software design advantages and characteristics of an 8080A-based general-purpose laboratory signal processor offer flexibility, reliability, low cost, and simplified programming that are relevant to applications involving the extraction and analysis of analog signals contaminated by noise within optical processing systems

Richard G. Lyons Department of Defense, Washington, DC

Microprocessor-based signal processors have intrinsic properties that contribute to their utility in research, development, and commercial environments.[1,2,3] The 8080A under discussion is particularly well-suited for application in a laboratory environment by its wide implementation, hardware/software support, and well-known architecture.[4,5] Flexibility is the primary advantage from both the hardware and software standpoint. Hardware modifications are simplified because the common bus structure of microprocessors permits convenient addition or removal of peripheral input/output devices that provide both analog and digital data sources and sinks. Since the development of laboratory signal processing algorithms is a dynamic and heuristic process, the most valuable property of a microprocessor is the ease with which its application program can be changed. This software flexibility, along with the stability and accuracy provided by hardware digital processing, normally make microprocessor-based laboratory signal processors more feasible than nonprogrammable analog signal processors.

Because most laboratory signal processing algorithms are small (<300 lines of code) and can reside in programmable read-only memories (P/ROMs) once machine code is fixed, operating system software with associated mass storage devices or teleprinter terminal is not required by the laboratory signal processor, resulting in a simple, portable, reliable, and reprogrammable instrument.

Memory and input/output (I/O) devices tend to be the most expensive items in small digital processing systems. Since the laboratory general-purpose signal processor does not require large amounts of semiconductor read/write random-access memory (RAM) or sophisticated I/O devices, its cost is typically less than $1000, including analog to digital (A-D) and digital to analog (D-A) converters.

Hardware/Software Considerations

To understand the suitability of using microprocessors in laboratory signal processing instruments, some pertinent hardware/software characteristics must be considered. For example, hand assembly of long machine language programs is tedious and error prone. Since machine language code for some microprocessors requires absolute addressing for branching instructions, the resultant program is difficult to relocate manually when correcting errors or adding program features. A 16-bit microcomputer requires complex instruction sets and addressing modes so that cross-assemblers, cross-simulators, or complete resident development system programs are recommended, including a resident assembler,

editor, relocating assembler, linking loader, and realtime debugger.

The average metal-oxide semiconductor (MOS) single-chip microprocessor has single-instruction execution times that range from 2 to 10 μs, which is three to ten times slower than bit-slice machines or standard minicomputers. For 8-bit single-chip microprocessors, the result is longer algorithm execution times due to inherent semiconductor technology, limited word length, and limited addressing modes.

However, even without the use of a cross-assembler or a resident assembler, program development using mnemonic language can be simple and straightforward for short application programs when using an 8-bit microprocessor. Faster program development results as the designer/programmer becomes familiar with the microprocessor's instruction set for efficient hand coding techniques. A resident read-only memory (ROM) monitor is not needed with proper hardware design and use of software system diagnostics.

Several software techniques can be used to aid program development and debugging. One valuable technique is to insert no operation (NOP) instructions liberally throughout the original program to establish open memory locations. Thus, program errors can be corrected by adding diagnostic instructions without having to relocate addresses when conditional branching instructions are used. An extension of the NOP technique that can be helpful is the use of program patches. This involves leaving open a block of memory (patch area) that can be branched to, if a more extensive series of instructions is added, when fixing errors or adding program features. This technique eliminates the need to recalculate addresses that have been previously assembled. When the program in the patch area has been executed, a jump instruction can send the central processor unit (CPU) back to the proper location in the main program.

During the debugging process, a halt (HLT) instruction can be used to allow manual examination of memory. When the CPU executes an HLT instruction, it enters a wait state that allows the operator to manually examine RAM. Program execution can be continued by manually activating an interrupt pushswitch. If the contents of registers internal to the CPU are to be checked, a short routine that loads their contents into memory must be executed before the HLT instruction is executed. When the application program has been checked out, these software debugging aids can be skipped by the CPU or replaced with NOPs. If memory space is at a premium, the software diagnostic instructions can be removed and the debugged application program can be reassembled, recoded, and rechecked manually to conserve memory space.

Signal Processor Instrument

To accommodate the described hardware/software requirements, a complete general-purpose 8-bit signal processor instrument design has been evolved, based on the 8080A single-chip microprocessor (Fig 1). Initial program development for this processor is accomplished by manually keying octal instructions into RAM using the input keyboard. Static RAM is implemented for data storage because of the small program required, thus eliminating the refresh circuitry needed for dynamic RAM. After the final application program is completed, it can be loaded into nonvolatile erasable programmable read-only memory (EPROM), which will retain the program during power turn-off. After power turn-on, the operator manually loads a jump instruction into the first location of RAM, causing the program counter (PC) of the CPU to jump to the first memory location of the EPROM. Data and address bus states are displayed at all times on front panel numeric light-emitting diode (LED) indicators in octal format.

The direct memory access (DMA) controller permits convenient program loading, memory examination, single-step operation, and input of blocks of data via the A-D converter. With the CPU in HOLD mode and the address bus driven by a 16-bit address register, whose initial value is set by front panel thumbwheel switches, a program instruction is loaded by typing in the proper 3-digit octal number at the input keyboard. When the third digit is keyed in, the instruction code is automatically loaded into RAM and is displayed on separate

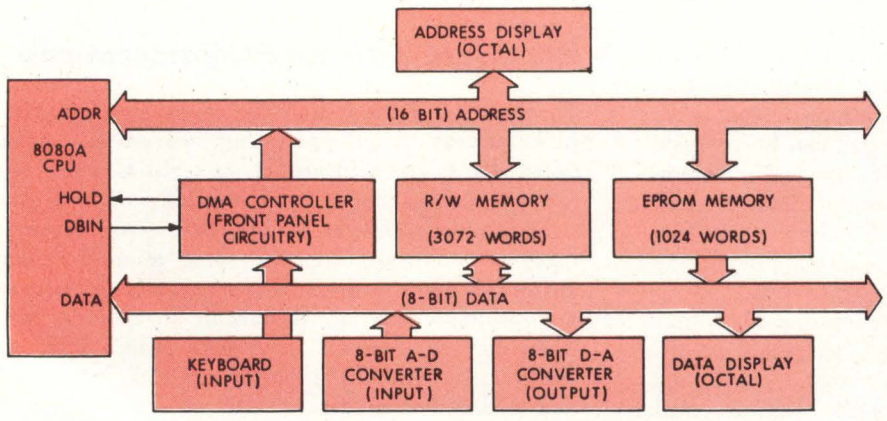

Fig 1 Simplified block diagram of general-purpose signal processor. Application programs are developed and debugged in RAM. Final program is then loaded into EPROM for easy access after power-up. A signal to HOLD input requests that the 8080A enter HOLD state. DBIN (data input strobe) output signal from CPU indicates that 8080A is ready for input data from 8-bit data bus

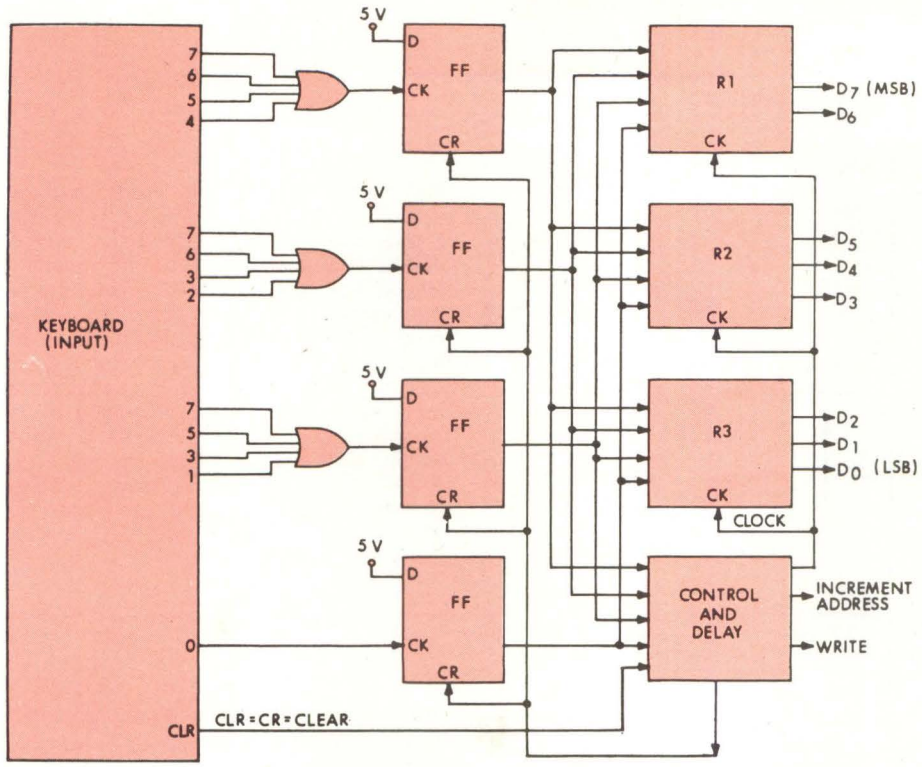

Fig 2 Simplified diagram of program load circuitry in DMA controller. Three octal digits of program instruction are loaded from keyboard consecutively into registers R1, R2, and R3. When third digit is loaded, address register (not shown) is incremented by 1, and data bits D_7 to D_0 are loaded automatically into RAM. 3 flip-flops are cleared after each digit is entered

numeric indicators, allowing the operator to double check the instruction machine code. The address register is incremented automatically so that the next program instruction can be keyed in.

A simplified diagram of the program load circuitry of the DMA controller is shown in Fig 2. If the programmer happens to load the wrong first or second octal digit, the keyboard clear (CLR) pushswitch can be activated to clear controller registers R1, R2, and R3. This allows the proper octal word to be loaded before the address register is incremented. Signals from the keyboard are used to clock the four controller flip-flops, which eliminate the need for contact-bounce elimination circuitry. While the CPU is in HOLD mode, the contents of the RAM location defined by the address register is displayed by the data display indicators. The address register can be incremented by a pushswitch on the front panel when consecutive memory locations are to be examined.

The DMA controller also contains circuitry that permits single-stepping through a program, mandatory for debugging purposes. Although the DMA controller can be designed to allow single machine cycle execution or single instruction execution during single-stepping, a single machine cycle is used because the CPU operation can be monitored in more detail during the execution of more complex instructions; eg, XCHG (exchange registers D,E with H,L), XTHL (exchange registers H,L with top of stack), and SPHL (transfer register H,L to stack pointer). The DMA controller also permits blocks of data to be loaded automatically from the A-D converter. Using DMA capabilities of the 8080A allows input data to be loaded at a speed that is limited only by that of RAM. This eliminates the need for using the 8080A INPUT instruction, which inputs one data word every 5 μs in this configuration. The DMA controller can be redesigned to handle data and addresses in a hexadecimal format rather than in octal, although this will not reduce the integrated circuit (IC) package count significantly. Typically the general-purpose laboratory signal processor in Fig 1 first loads a block of data into RAM via the A-D converter,[6] processes this data and outputs them through the D-A converter, then accepts a new block of data, and repeats the process.

Signal Processing Applications

A useful application for a microprocessor-based signal processor is processing digitized output signals from photodetectors in optical processing systems. In these systems, signals of interest normally are contained in the intensity of light or laser beams (Fig 3). A common device used to detect light intensity is a linear array of photodetectors. These photodetectors—usually silicon photodiodes—absorb photons for a specified period of time (integration period) and output an analog voltage that is proportional to the total number of photons absorbed. Thus, output of the entire photodetector array is a serial stream of analog pulses. Each analog pulse is the output of a particular detector during one scan of the array. The desired signals contained in the intensity of the light are now contained in the photodetector outputs. Normally, these output signals are contaminated with a fluctuating, as well as a fixed, pattern noise. In this particular optical application, the laboratory signal processor must digitize (A-D) and store the photodetector

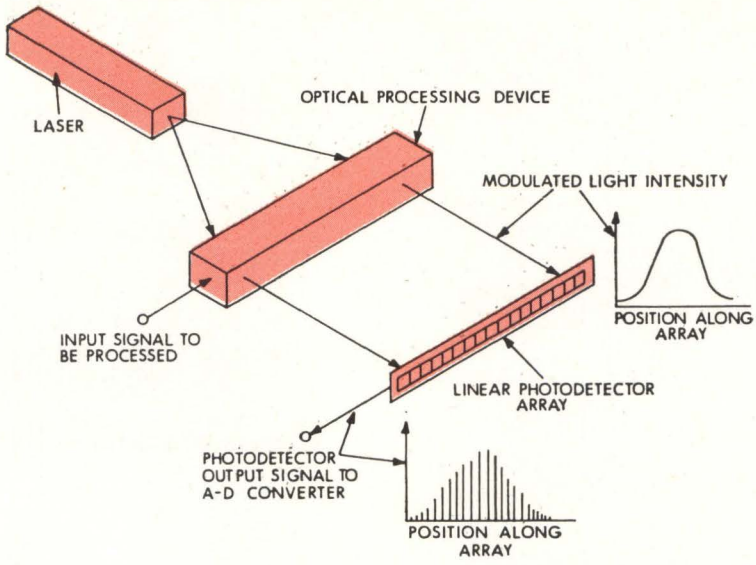

Fig 3 Simplified optical processing system. Optical processing device is typically a bulk wave acousto-optic defraction cell or a surface acoustic wave light modulator. Modulated light, whose intensity carries the desired signal, is detected by an array of discrete phototransistors, photodiodes, or a linear light imaging charge-coupled device. Output from the photodetector array is a serial stream of analog pulses whose amplitude is proportional to the intensity of the light imaged on the array. A 256-element photodetector array outputs 256 analog pulses during each scan

array output values in RAM, and extract the average value of each photodetector output from the noise. When the average value for each photodetector has been computed and stored in data memory, the entire block of average values are output via the D-A converter for display on an oscilloscope or an X-Y recorder.

Uncorrelated Noise Reduction Through Signal Averaging

The first type of fluctuating photodetector noise to be minimized is the inevitable thermal noise that arises in all semiconductor devices. This noise contributes to random fluctuations about the average value of each array photodetector output. Referred to as uncorrelated, the noise on one detector is unrelated with the fluctuating noise on any other detector. In some optical processing systems, it is necessary to detect changes in the average output signal that are smaller than the fluctuations about the average. A straightforward method to maintain the average while minimizing the fluctuations is through signal averaging. Statistical considerations of signal averaging are well known; from the Central Limit Theorem,[7] it can be shown that when n samples from the same distribution are averaged, then

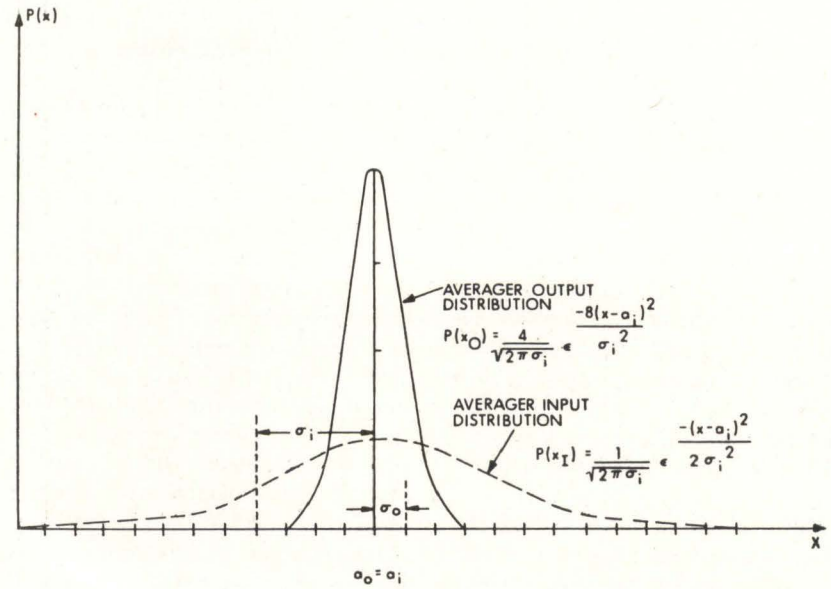

Fig 4 Input (dashed) and output (solid) probability distributions of signal averager that averages 16 input values. Eqs (1) and (2) show that average of the two distributions are equal to a_i while standard deviation of the output (σ_o) is equal to $\sigma_i/4$. If probability distribution function of input signals is normal, say $P(x_I)$, then distribution function of output signals from signal averager will be $P(x_O)$. Areas under both curves are equal to unity

$$\sigma_o = \sigma_i\sqrt{n} \quad (1)$$

and

$$a_o = a_i \quad (2)$$

where

σ_o = Standard deviation of signal averager output

σ_i = Standard deviation of input samples

a_o = Average value of signal averager output

a_i = Average value of input samples

Values σ_o and σ_i can also represent the rms noise levels of the output and input, respectively, of the signal averager. Note from Eqs 1 and 2 that the average of the output values from a signal averager is equal to the input average, while the variations about the output average (σ_o) is less than the variations about the input average (σ_i). The result of signal averaging is that the desired signal (a_o) is preserved, while the undesired signal (σ_o) decreases. Fig 4 shows the input and output distributions of a signal averager with n = 16.

Implementation of signal averaging is simplified with the general-purpose laboratory signal processor. An array of 16-bit (two 8-bit bytes) locations is established and initialized to 0 as data accumulators in memory. One data accumulator must be reserved for each detector in the photodetector array. An equal number of 8-bit locations (input block) is reserved in memory, which will contain the input values obtained via the A-D converter each time the photodetector array is scanned. After each array scan, the content of each location in the input block is added to the content of its corresponding data accumulator. A register must be established and initialized to count the number of sums taken in the averaging algorithm. This counter register can be one of the 8-bit registers internal to the CPU (B, C, D, E, H, or L) or a memory location, assuming that not more than 255 sums are taken. This counter register is initialized at the beginning of the program, decremented by 1, and checked for 0 each time the data accumulators are updated. When the register content reaches 0, the summing operation is completed. The CPU must then divide the content of each data accumulator by the number of sums taken to arrive at the final average.

In signal averaging, the CPU spends most of its execution time moving a 16-bit value from memory to its ALU, adding an 8-bit word, and storing the resultant 16-bit word back into its original memory location. Although the addressing modes of the 8080A appear limited, relative to minicomputers or 16-bit microprocessors, it has four sets of instructions that can be used to reference 16-bit values at memory locations defined by the content of register pairs internal to the CPU. They are as follows:

Memory Reference Instruction	Addressing Mode	CPU Register Pair Containing Memory Address
STAX and LDAX	Internal Register Pair Indirect	Register Pairs B, C and D, E
MOVrM and MOVMr	Internal Register Pair Indirect	Register Pair H, L
XTHL	Stack Pointer Indirect	Stack Pointer
PUSH and POP	Stack Pointer Indirect	Stack Pointer

The algorithm to perform the divide operation on the contents of the data accumulators is straightforward. If the number of sums taken is a power of two (2^n), then the contents of the data accumulators need only be shifted to the right n places to obtain the proper quotient. If the sum of 256 additions are contained in the data accumulators, then the average is contained in the most significant eight bits of each data accumulator location, and no shifting operation need be performed. Maximum error in this division technique is less than the least significant bit of the quotient. In 8080A Assembly Listing to Perform Signal Averaging on 64 Scans of a 128-Element Photodetector Array, all numbers are given in octal notation. First elements of input data block, data accumulator, and array of quotients are in memory locations 100, 300, and 1000, respectively. Input data block is loaded into memory during execution of halt (HLT) instruction.

Note that the signal averaging technique will minimize the effect of thermal noise from a photodetector only if the standard deviation of the detector noise is greater than the rms of the quantizing noise from the A-D converter. If the least significant bit of the A-D converter represents a voltage level of K volts, then rms of its quantizing noise is $K/\sqrt{12}$.[8] Therefore, signal averaging will minimize any random analog noise if the standard deviation of the noise signal is equal to or greater than K volts.

Correlated Detector Noise Cancellation

In optical processing systems, there is a noise type that is correlated among all photodetector outputs because it causes output signals of all photodetectors to either increase or decrease simultaneously. Sources of this noise are fluctuations in the intensity of the light or laser source and in the photodetector array power supply. A simple method used to minimize this noise is to establish a reference photodetector that monitors only the unmodulated laser intensity. The input signal to the optical processing device can be limited in bandwidth so that the first photodetector of the array receives only unmodulated laser light. This photodetector can be considered the reference detector because large changes in its output will be due only to laser light or array power supply fluctuations.

After each scan of the array, the value from the reference detector is compared to the reference value of the previous scan. With no correlated noise present between array scans, the present reference value will be equal to the previous reference value. If correlated noise is present between scans, the reference signals will not be equal, and the present values in the input block of data must be modified to eliminate the effect of the correlated noise. This modification is easily implemented in the signal processor either before or after any signal averaging by using the flowchart of Fig 5.

Differential Cancellation of Unwanted Signals

In some optical processing systems, it is not the actual outputs of the photodetector array that are of interest, but rather the change in outputs from one scan to the next. This situation exists when there is a fixed pattern on the photodetector outputs, given a uniform light or

8080A Assembly Listing to Perform Signal Averaging on 64 Scans of 128-Element Photodetector Array

```
        SUB     A       ; clear A
        MOV     D,A     ; clear D
        MVI     A,100   ; number of sums to be taken
        STA     6       ; sum counter in location 6
START:  HLT             ; wait for new input block
        MVI     A,200   ; number of detectors
        STA     7       ; detector counter in location 7
        LXI     SP,300  ; location of 1st data accumulator
        LXI     B,100   ; location of 1st word of input block
SUM:    POP     H       ; load data accumulator into CPU
        LDAX    B       ; load input data word into CPU
        MOV     E,A
        DAD     D       ; 16-bit add to data accumulator
        PUSH    H       ; store updated data accumulator
        INX     B       ; increment input data pointer
        INX     SP      ; increment data accumulator pointer
        INX     SP
        LDA     7       ; check detector counter
        DCR     A       ; decrement detector counter
        JNZ     SUM     ; if A ≠ 0, continue summing
        LDA     6       ; check sum counter
        DCR     A       ; decrement sum counter
        JNZ     START   ; if A ≠ 0, jump to START
        LDA     SP,300  ; location of 1st data accumulator
        DCR     H,1000  ; location of the 1st quotient
        JNZ     A,200   ; number of quotients
        LXI     7       ; quotient counter in location 7
DIV:    LXI     B,6     ; sets divisor equal to 2^6
        MVO     A       ; clear carry
        STA     D       ; load data accumulator into CPU
MO:     MOV     A,D
        RAR             ; rotate 8 MSBs right
        MOV     D,A
        MOV     A,E
        RAR             ; rotate 8 LSBs right
        JNC     AA      ; check state of carry bit
        CMC             ; clear carry bit
AA:     MOV     E,A
        DCR     B
        JNZ     MO      ; if B ≠ 0, continue divide routine
        MOV     M,A     ; store quotient
        INX     H       ; increment quotient location pointer
        LDA     7       ; check quotient counter
        DCR     A
        JNZ     DIV     ; if A ≠ 0, continue divide routine
        HLT             ; signal averaging routine completed
```

laser illumination, or when there are undesired continually present signals on the outputs. Deviations from this fixed pattern noise must be detected by the signal processor.

A process of differential cancellation can be performed by the signal processor by storing, in an array of memory locations, digitized values from a scan of unwanted fixed pattern signals. This reference array now contains a block of values to compare with subsequent scans. Desired signals are then the differences between an input scan and the reference scan. Memory reference instructions STAX, LDAX, and MOV of the 8080A CPU are sufficient to conveniently manipulate data arrays in performing the differential cancellation scheme.

Calculation of Statistical Variance Using Integer Arithmetic

In some optical processing systems, it is necessary to measure the fluctuating component of a single photo-

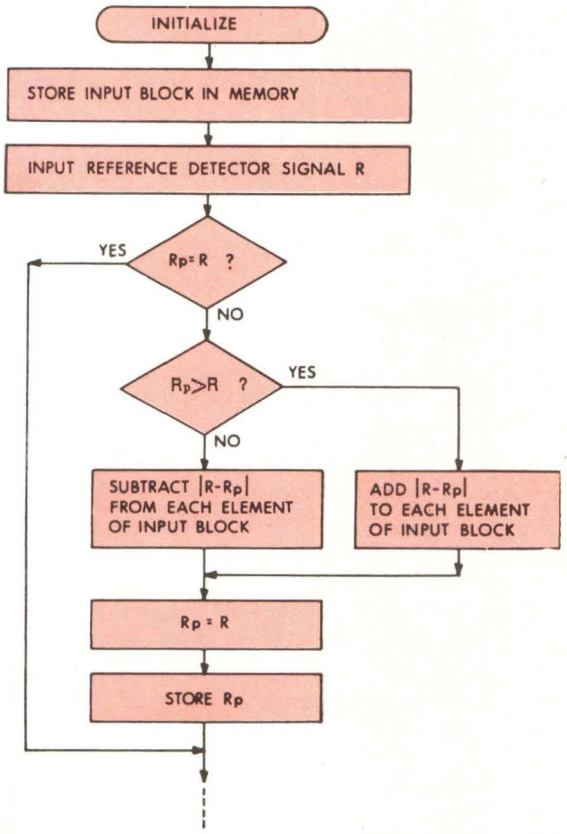

Fig 5 Functional flowchart for correlated detector noise cancellation algorithm. A single detector of a photodetector array can be used to obtain reference detector signal (R) during scan. R_p is reference detector signal from previous scan. Addition and subtraction operations are easily implemented because 8080A CPU uses 2's complement arithmetic

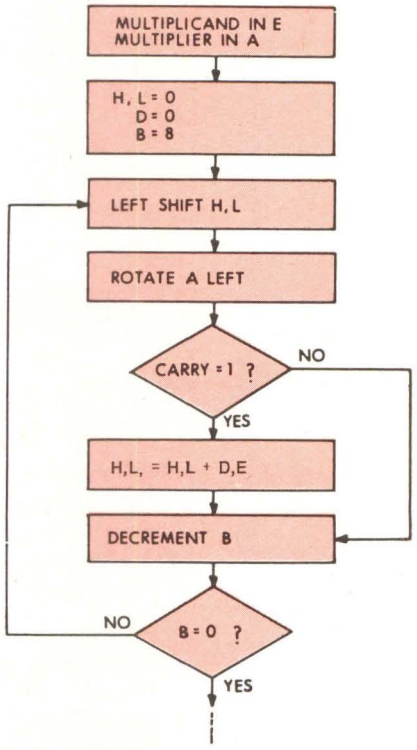

Fig 6 Functional flowchart of add-and-shift multiplication algorithm for 8080A CPU. 16-bit left shift is performed by adding H,L register pair to itself (DADH) instruction. Complete 16-bit product, contained in H,L register pair, can be obtained in less than 230 μs if 2.0-MHz clock is used with 8080A

detector output quantitatively. This requires the calculation of the statistical variance (s^2) of n output signals, where

$$s^2 = \frac{1}{n} \sum_{i=1}^{n} (x_i - \bar{x})^2 \qquad (3)$$

and

$$\bar{x} = \frac{1}{n} \sum_{i=1}^{n} (x_i) \qquad (4)$$

In Eq 3, x_i is the ith output sample and $\bar{x}$ is the average of n output samples. For an 8-bit microcomputer, it is convenient to let n = 256 in Eqs 3 and 4. This allows division by n = 256 in both equations to be realized by truncating the 16-bit sums to their most significant eight bits. After receiving 256 detector samples, the microcomputer can use the signal averaging technique to calculate $\bar{x}$ in Eq 4. Then, $\bar{x}$ is used in Eq 3. The standard multiplication technique of add-and-shift (Fig 6) can be used to perform the squaring operation in Eq 3.

Care must be taken during the calculation of s^2 in Eq 3 when truncation is used to effect division. With n = 256, Eq 3 can be rewritten in the form:

$$s^2 = \frac{(x_1 - \bar{x})^2 + (x_2 - x)^2 + \ldots + (x_{256} - \bar{x})^2}{256} \quad (5)$$

or

$$s^2 = \frac{(x_1 - \bar{x})^2}{256} + \frac{(x_2 - \bar{x})^2}{256} + \ldots + \frac{(x_{256} - \bar{x})^2}{256} \quad (6)$$

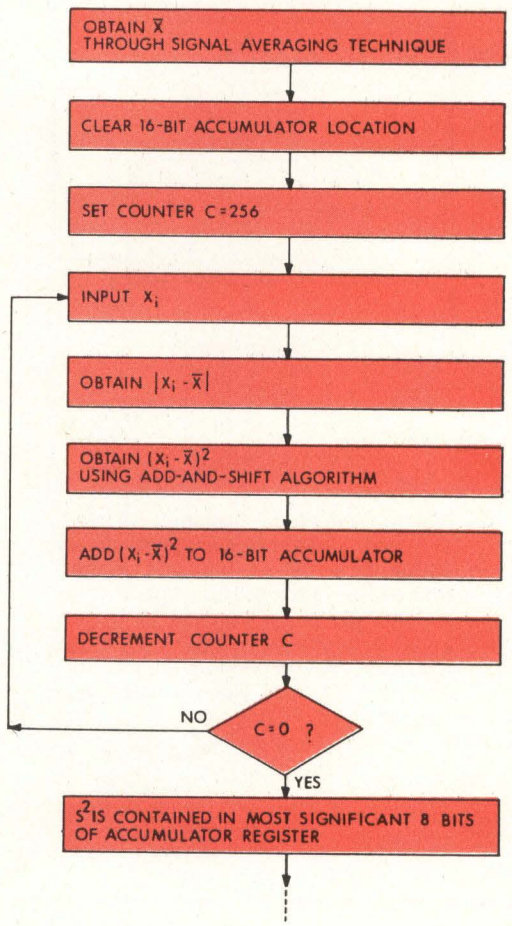

Fig 7 Functional flowchart for statistical variance (s^2) calculation using 256 samples from single photodetector element. Average output value of detector ($\bar{x}$) is obtained using described signal averaging algorithm. Use of 256 samples to calculate variance eliminates need to perform division in Eq 5 because variance is contained in most significant 8-bits of accumulator registers

Eqs 5 and 6 are mathematically equivalent, but Eq 6 cannot be used explicitly for small signals because the squared terms may be less than eight bits. If the squared terms are divided by 256 by truncating the least significant eight bits, the resultant variance will either be too low or 0. Therefore, Eq 5 must be used to calculate the variance, as shown in Fig 7.

Summary

Assuming that the optical signals to be processed can be digitized and stored in memory, a general-purpose microprocessor-based laboratory signal processor is capable of implementing several processing algorithms on input data. Using proper hardware design, a low cost, flexible, and reliable laboratory signal processor can be implemented with the 8080A microprocessor. Even without the use of a cross-assembler or a resident assembler, program development can be simple and straightforward for short application programs. The limited word length, speed, and addressing modes of 8-bit microprocessors do, however, limit their use in implementing complex algorithms. Although the applications presented in this article concern noise reduction and signal analysis techniques used on light sensing devices, the general-purpose laboratory signal processor is not limited to these uses.

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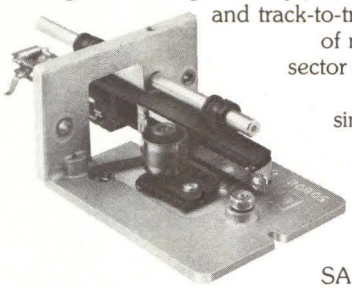

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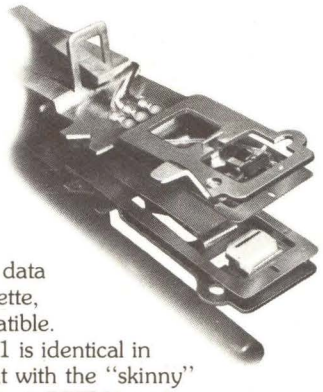

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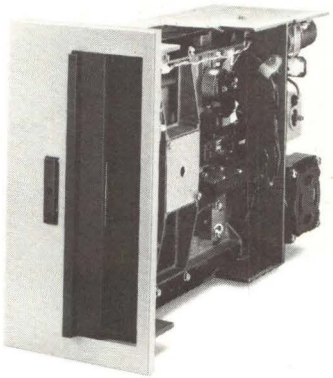

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TECH NOTE

Economics of Designing with Raster Scan Displays

Unfamiliarity with video display technology by digital designers can lead to expensive and unnecessary specification complications for CRT terminals. Examination of common problem areas for raster scan display sizes and uses can result in cost-effective design guidelines

Ronald L. Chisenhall Ball Electronics Display Division, St Paul, Minnesota

Raster scan was the favored method of alphanumeric display in the 1960s because of standard television parts and technology rather than such complex techniques as random point plot or character stroke tracing for the lowest cost/character displayed. However, television-type displays suffered shortcomings in picture quality, such as limitations in corner focus, geometric distortion, and video bandwidth, which were accepted as part of the price/performance tradeoff.

Since then, data displays using higher quality cathode-ray tubes (CRTs) and deflection yokes have improved performance levels of raster displays. Also, the development of improved electron guns enhanced brightness and resolution, and advanced deflection components and circuitry helped to optimize alphanumeric presentation.

Raster scan data displays are more expensive than television receivers because of higher requirements for resolution, focus, distortion, and reliability. Yet these displays are less expensive than any alternative high performance type because of design efficiencies in the resonant deflection and high voltage system, and CRT.

Presently, the rapid proliferation of applications for low cost data displays has revolved around the microprocessor for practical and affordable electronic data processing. This economical trend invokes renewed pressure for further cost reduction. By being aware of potential problems and pitfalls in designing raster scan displays, the designer can alleviate this pressure.

Design Problems

Basically, circuit design problems presented by raster scan displays resist low voltage or digital design solutions. The analog nature of the display signals, the high voltage and current levels involved, and the dependence on resonance for economical energy transformation preclude the flexibility that a digital design could provide. In the raster display, most performance parameters are interrelated via the resonant horizontal drive and high voltage supply networks.

Horizontal drive circuit, deflection coil, width coil, linearity circuit, and high voltage flyback transformer form a resonant circuit that produces a controlled curvilinear ramp for deflection, and utilizes the ramp

decay for generation of several critical supply voltages. The supply voltages, in turn, affect the CRT operating characteristics with which the ramp must interact. Almost any deviation from a nominal design will affect several interrelated parameters. For example, design modifications to the anode voltage (typically in the 10- to 14-kV range) would have major effects on picture size, spot focus, and brightness.

A simple design change could effect increased sensitivities to variances in component values, input signals, or environmental conditions. To prevent unwanted side effects, the designer must carefully follow through each proposed variation with adjustments to other circuit values. Circuit layout considerations, such as dissipation, cross-coupling, and stray reactances, also compound the design problem. Frequently after a special design implementation, an unexpected performance or reliability anomaly will surface in the field, resulting in significant service costs. Thus, the resonant curve and its rapidly changing slopes offer a special set of traps for raster scan display designers. Deviations from proven designs should be made only after all standard alternatives have proven infeasible.

Custom Display Costs

Design factors impacting the cost of CRT displays are unique and do not affect other elements in a data terminal system. High energy content in CRT production, expensive raw materials, and skilled calibration labor prevent radical cost reductions of the kind attained in other areas of electronics. Pending Department of Health, Education, and Welfare (DHEW) Radiation Performance Standards related to x-ray specifications, as well as Underwriter's Laboratory (UL 478) safety requirements, have increased the cost of data display monitors. Design improvements and changes must be in accordance with these regulations. Despite these restrictions, the overall cost increases for most raster scan displays have remained near the inflation baseline, while performance and reliability have been improved substantially over the past several years.

In some applications, nonstandard designs are necessary to satisfy special requirements. Conversely, many specialized design changes merely add costs with little increase in performance value. The designer must screen each proposed design change and carefully measure the expected performance value yield. For example, nonstandard active video area dimensions may be of no consequence if appropriate blanking intervals are specified. However, changes to standard size or blanking specifications, without a corresponding change in the other, can be costly. This situation could also adversely affect other performance parameters, such as linearity. A related problem would also result from special design requirements for video size adjustment range, especially in the horizontal axis.

When design parameters are specified tighter than the standard offering, costs will almost certainly increase, due to higher precision parts and increased calibration and inspection labor. In many applications other design tradeoffs need to be recognized. For example, further improvements in geometric distortion of the video field edges would require an expensive deflection yoke and lengthy calibration time, and could degrade corner focus. Improvements made on video area size, centering, and linearity tolerances are characteristically costly. Tight size and centering requirements frequently originate from improper coordination of the location and dimensions of the bezel opening with standard display tolerances.

Selecting the interfacing connector system continually presents design problems. Usually designers have evaluated and selected preferred connector types, and tend to reject different monitor connectors. Obviously, special connectors entail higher design, documentation, and part costs. For some applications, the designer may specify that a display monitor operate properly when powered from a system dc supply having fair regulation and/or no level adjustment. Assuming that the voltage swing is acceptable with regard to monitor dissipation and voltage ratings, the designer expects considerable performance variation. Display monitor operation is highly dependent on stable voltages, and careful factory calibration at nominal voltage will not be evident if the monitor is later installed with an off nominal power supply.

CRT Display Area and Information Capacity

CRT Size (diag)	Usable Display Area	Total Number of Characters (typ)
5 in (12.7 cm)	9.72 in^2 (63.2 cm^2) or 2.7 x 3.6 in (6.9 x 9.1 cm)	512
9 in (22.9 cm)	33.5 in^2 (217.8 cm^2) or 5 x 6.7 in (12.7 x 17 cm)	1280
12 in (30.5 cm)	60.3 in^2 (391.9 cm^2) or 6.7 x 9 in (17 x 22.9 cm)	1920
15 in (38.1 cm)	90.75 in^2 (589.9 cm^2) or 8.25 x 11 in (20.96 x 27.9 cm)	1920 to 6000

Display Sizes and Uses

An adequate understanding of the ramifications of CRT parameters is mandatory if the optimum display is to be designed for a given application. The Table, which includes display area and information capacity, itemizes pertinent CRT characteristics that are representative of industry values. For maximum economy, display designers should attempt to accommodate these values. CRT display applications have segregated into several categories. Small monitors, such as 5 and 9″ (12.7 and 22.9-cm) diagonal CRT sizes, are used for portable and mobile applications, instrumentation systems, desktop computers, and point-of-sale (POS) terminals. The 12″ (30.5-cm) diagonal CRT has been the most popular size for standard data terminal displays.

Currently, several factors are combining to increase the popularity of 15″ (38.1-cm) displays. Increased information densities, such as more complex character dot structures, or more characters per page, have dictated this larger screen size for proper readability. In many full-featured terminals, keyboard width remains the limiting factor in the overall size reduction taking place as logic, memory, and power supply modules shrink in size. More space has therefore become available inside the cabinet to utilize the 15″ (38.1-cm) display. Larger displays, such as 19, 23, and 25″ (48.3, 58.4, and 63.5-cm) sizes, are used in applications requiring increased viewing distances, such as process control, airport systems, and data terminal slave monitors.

Screen capacity for the compact 5″ (12.7-cm) display is normally 16 rows of 32 characters, and the 9″ (22.9-cm) size accommodates 20 rows of 64 characters. These capacities are primarily established by character size and readability at normal viewing distances. A 12″ (30.5-cm) display with 24 rows of 80 characters has been the de facto industry standard page format. For utility applications, a character of 5 x 7 dots in a 7 x 10 matrix dominates. When clearer character definition is required for more complex character sets and special symbols, a 7 x 9 character is used. This format requires a wider video bandwidth and higher horizontal line frequency. For these applications, the 15″ (38.1-cm) size applies. Applications for high performance 15″ (38.1-cm) displays require 5k to 6k characters displayed in an area of approximately 8.5 x 11″ (21.6 x 27.9 cm). Word processing and raster graphics applications will continue to place the highest demands on raster scan display technology.

For high volume low cost terminal applications, designers search for further cost reduction. For example, a recent implementation offers utility displays that are completed and aligned, but do not include a frame or chassis. Provision for mounting the interconnected display subassemblies are designed into the terminal structure. Certain design situations benefit in reduced overall costs by this approach, but subassembly location and orientation must still be coordinated.

Design Guidelines

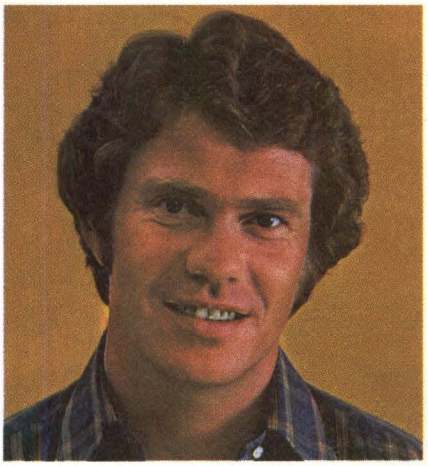
Many display parameters are specified in terms of operating ranges, and the achievable tolerance at a specific nominal is not always apparent. For instance, video size and centering can cause undue costs if small design tolerances are arbitrarily specified. In general, the design guideline for specifying the height and width of the active video area is to apply a tolerance of not less than $\pm 3\%$ of full scale, where full scale is the height or width, respectively, of the maximum usable display area. Centering tolerances should be not less than $\pm 2\%$ of full scale. Both size and centering are measured at the centerlines of the active video rectangle.

On-axis incremental linearity is properly specified by requiring character height and width to be within 10% of that for any adjacent character, and within 20% of that for any character on the screen. Distortion, which is a "catch-all" term for several off-axis positional errors, results in the video perimeter edges appearing nonrectangular, such as curved edges, trapezoidal effects, nonorthogonality, and CRT/yoke anomalies. The perimeter of a full field of characters should approach an ideal rectangle within $\pm 1.5\%$ of maximum usable height.

These examples illustrate design specifications that are directly dependent upon calibration labor and component cost. Display designers can design monitors that exceed these performance levels, but the incremental costs follow a sharply rising curve. Display package size, power dissipation, and reliability are also affected by tighter design specifications.

Summary

Operating characteristics of raster scan displays offer some degree of latitude in design choices of nominal parameter values. However, early evaluation by the display designer is advisable to determine the effects on standard hardware design. The best cost value is usually realized when standard display specifications are planned into the early terminal design. Skill and experience accumulated by industry designers have evolved standard displays that represent the best price/performance ratio. □



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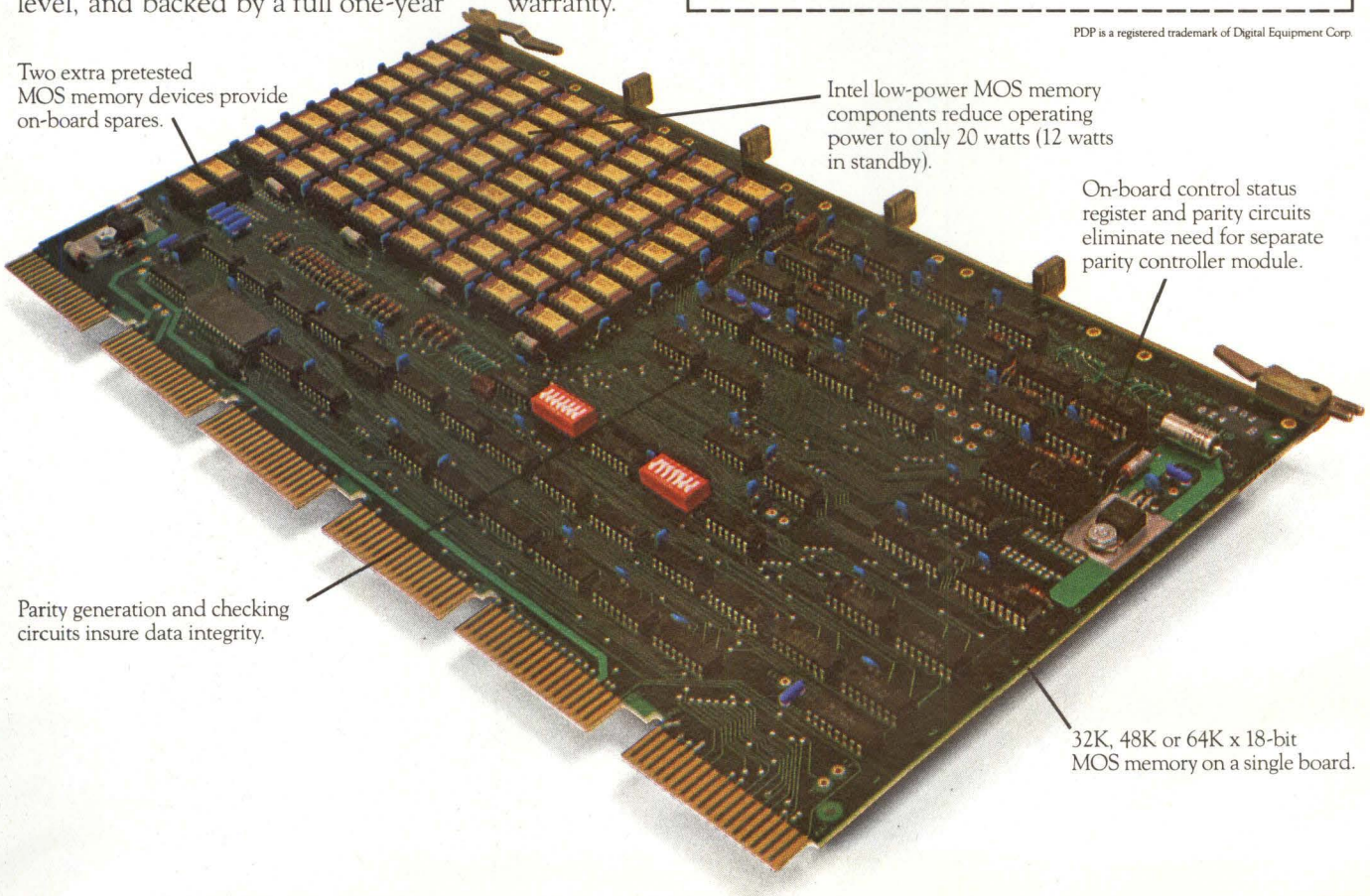

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TECH NOTE

Ink-Jet Printer Mechanism Uses Non-Static Vacuum Technique

A nonimpact serial printer terminal combines an ink-jet vacuum principle, an unusual ink chemistry, and a dense array of ejection nozzles to project an electrically controlled stream of uncharged droplets, without the need for field deflectors, onto plain paper, resulting in a fine dot matrix image with instant character recognition

Joachim Heinzl and Günter Rosenstock Siemens AG, Munich, West Germany

An ink-jet printer mechanism provides minimal noise, high speed, and sharp resolution by combining the high quality of type printing with the type variety of dot matrix printing to produce alphanumeric characters on ordinary fanfold paper that are instantly legible, smudgeproof, and nonerasable. Incorporating the vacuum ink-jet principle, the printer mechanism attains a printing speed of 300 char/s. The only noise sources are the carriage traveling with the printer mechanism across the paper, and the paper transport facility. Weighing 200 g, the printer mechanism holds sufficient ink for 5M characters, and operates from −15 to 55 °C. To overcome one usual limitation of ink-jet printing—the inability to produce immediate multiple copies—this modular mechanism is interchangeable with a duplicate-page producing standard needle printing mechanism. The Siemens PT80i serial printer terminal possesses unique ink composition properties.

Ink Characteristics

To satisfy severe jet-printing requirements, the ink possesses a defined surface tension and viscosity to ensure proper functioning of the printhead; produces a black, high contrast character on plain paper that is indelible and lightfast; does not dry in the jet-nozzle orifices, yet is instantly smearproof on the paper; and prevents dye deposits from accumulating in the printhead and blocking the nozzles, even if the printhead is not used for extended time periods. A wetting, hygroscopic antifreeze solvent enables the ink to be stored at low temperatures, while conservation additives prohibit fungus growth. Once deposited on untreated paper, the ink penetrates quickly into the fibers, becomes absorbed by capillary action, and establishes an unwashable imprint. For optical recognition, the ink provides a print contrast signal (PCS) of 0.39 according to optical character recognition (OCR) standards in infrared light, although it does not contain any pigments. In visible light, the contrast according to OCR standards is 0.6 to 0.7 PCS. An ink-jet nozzle can eject up to 2500 droplets/s. For each droplet, 10^{-5} watt-sec (Ws) are applied to the drive transducer; of which,

10^{-8} Ws are carried by the flying droplet in the form of kinetic and surface energy. An ink droplet measures 0.1 mm in diameter and produces a black spot that is 0.3 mm in diameter on the paper.

Comparable data for the substitute needle printhead are: one needle strikes the paper through an ink ribbon, up to 700 times/s; for each stroke, the drive solenoid consumes 2×10^{-2} Ws; and kinetic energy of the needle on impact is 10^{-3} Ws. In needle printing, the color in the ink ribbon has to be squeezed out before it is impregnated into the paper.

Ink-Jet Printing Techniques

The three common ink-jet printing techniques—high pressure, low pressure, and vacuum—differ according to the type of pressure used to supply ink to the jet nozzles.

In the high pressure technique, ink is ejected as a stream from a narrow nozzle, which breaks up into discrete droplets that are deflected by electrostatic or magnetic means. Ultrasonic excitation produces regular constrictions in the fluid jet and, thus, achieves uniform breakup into droplets. However, it is not possible to release the droplets individually. Printers operating on this principle are the Siemens SICOGRAPH terminal and the IBM 46/40 printer.

In the low pressure technique, the ink wets the tip of a narrow nozzle and forms a convex meniscus. Droplets are pulled off this meniscus by an electric field, and are deflected electrostatically to form characters. However, droplet formation cannot be kept stable over long periods of time. The Teletype® Inktronic printer and the Casio 300 printer are representative of this technique.

A vacuum is maintained in the nozzle, except at the instant that a droplet is ejected, in the vacuum technique. Ink that gets onto the face of the nozzle is pulled back by the vacuum; thus, the nozzle is selfcleaning. Upon demand, ink entering into the nozzle is formed into a concave meniscus at the orifice. A droplet is ejected by means of a shock wave that causes a momentary increase in pressure in the nozzle. This shock wave is generated by an electric field momentarily applied to a piezoelectric transducer. The ink forms itself into a droplet, breaks away from the nozzle trailing a long tail, and flies off as a tiny spherical entity.

Since the droplets can be released individually under electrical control and every droplet impacts the paper, there is no need to catch or deflect the droplets. Moreover, because the vacuum technique leaves the face of each nozzle unwetted, a large number of nozzles can be arranged in a dense array. The PT80i ink-jet printer mechanism is designed around the vacuum technique.

Printer Mechanics

The printhead (Fig 1) contains 12 nozzle orifices arranged in two offset columns of six each. Distance to the paper is about 1 mm. Twelve jet channels radiate outward in two planes from the orifices. The droplet flight direction is not dependent upon the angle of inclination of the jet channel; instead droplets fly on parallel paths from the nozzle array plate to the paper, in about 400 μs. The nozzle array plate is heated to a constant temperature by means of current through a small resistor. Consequently, ink droplets are always formed with constant viscosity and surface tension regardless of the ambient temperature. Jet channels are concentrically enclosed by piezoceramic transducer tubes. Silver films on the tubes' inner and outer surfaces serve as electrodes for applying the electric control field.

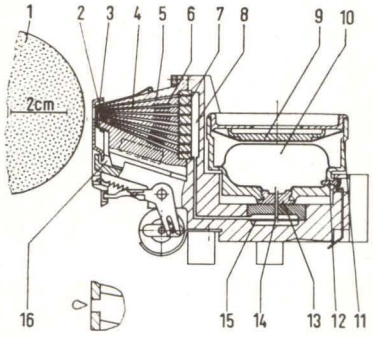

Fig 1 Structure of ink-jet printer mechanism. Ink is distributed from reservoir through manifold and constricted supply channels to 12 nozzles by vacuum system. Droplets are triggered by means of electrical pulses to piezotransducers. Transducers cause momentary decrease in nozzle pressure, resulting in shock waves that eject droplets in parallel paths onto untreated paper

The nozzle channels are supplied with ink from the manifold. Narrow channels provide a choke effect that protects the nozzles against pressure shocks from the ink reservoir.

The manifold is connected to the ink supply by means of a filter, which traps any dirt particles. The replaceable ink bottle holds the ink in a flexible plastic skin. Inserted in the base of the bottle is a molded rubber plug that establishes the link to the printing system. When the ink bottle is installed, the plug is pierced by a hollow needle. The ink bladder, located below the level of the nozzle orifices, creates a static vacuum in the nozzles. When the ink bottle is changed, the printhead remains filled since capillary forces in the nozzles prevent a reverse ink flow.

The ink supply is monitored by means of resistance measurements between electrodes in the base of the ink bottle. In the PT80i, for example, a flashing lamp indicates that the ink bottle is nearly empty and permits timely replacement. If this signal indication is overlooked, the printer terminal switches off automatically when the bottle is empty.

The protector plate is actuated by a small dc motor, and is guided between the printhead and paper platen whenever the printer terminal is switched off or the cover lid is raised. Any ink that emerges from the nozzles at this time is diverted into a slanted duct underneath the printhead, channeled back to the ink bottle, and absorbed by a swab.

Printer Electronics

In the PT80i, the analog section of the printer control electronics is mounted on a printed circuit (PC) board connected to the printer mechanism via a ribbon cable. For ink-jet printing, the printer electronics circuits include two character generators; power amplifiers for two stepping motors—one operates the line feed, the other the carriage; 12 final amplifiers for the piezoelectric transducers; monitoring circuit for the ink supply; heater circuit for the nozzle array plate; and motor control circuit for moving the protector plate.

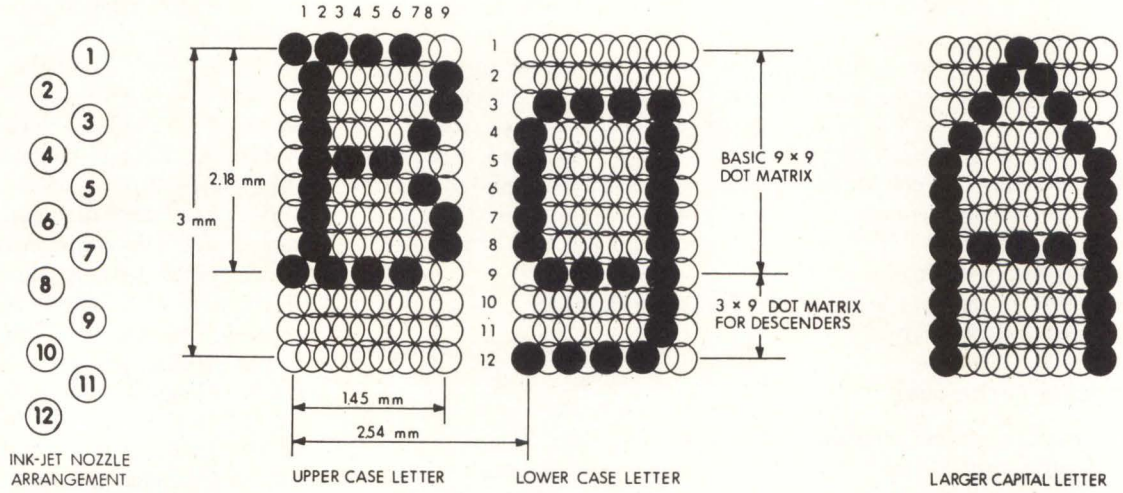

Fig 2 Serial matrix printout. Single printhead moves horizontally across paper, depositing inked upper-case, lower-case, and large capital letters, numbers, and symbols in 12 x 9 dot matrix array. Twelve ink-jet nozzles are arranged in two offset columns of six each to obtain highly legible characters

Alphanumeric characters are formed by a dot matrix array of 12 rows x 9 columns (Fig 2). In this array, the top 9 x 9 dot matrix is utilized for printing upper- and lower-case letters, numbers, and symbols, the bottom 3 x 9 matrix for descenders of lower-case letters. Larger capital letters are available by implementing the entire 12 x 9 format.

For printing, regular character fonts are stored in character generator 1, with a different font in character generator 2. Each generator is a 28-pin, 10k-byte, plug-in, read-only memory (ROM) or programmable read-only memory (p/ROM). ASCII-coded bit patterns are stored in each generator, 12 x 9 bits for each character. Matrix column 1 is addressed directly with a 12-bit pattern of the desired character; then, the printhead is moved horizontally by the carriage to the second column position. Triggering of each 12-bit pattern for the remaining eight matrix columns of the character is accomplished by column addressing signals.

The 12 ink-jet nozzles are arranged on the front guide of the printhead in two offset columns of six each, and the ink droplets that form a single vertical line on the paper are ejected on a trigger-delay basis, initially, the odd-numbered nozzles, followed by the even-numbered nozzles. Consequently, the offset ink droplets overlap and merge to form unbroken lines and crisp character printouts. Each droplet is ejected from a nozzle under control of an associated piezoelectric transducer. In turn, these transducers are activated by a series of electronic signals that are transistor-switched and transformer-coupled. The electrical signals cause the piezoelectric transducers to expand and contract, thereby creating the shock wave that forces the droplet to fly off the nozzle.

Summary

An ink-jet printer mechanism based on implementation of the vacuum technique comprises 12 nozzles, and prints characters composed from single dots like a needle printer but faster, quieter, and wear-free, since there are no moving parts in the printhead. Character imprint quality is attained with a simple, rugged, and reliable printer mechanism that can be refilled with ink easily, is self-cleaning, and ejects ink over a short distance, without deflection and without ink recycling, with every droplet striking the paper.

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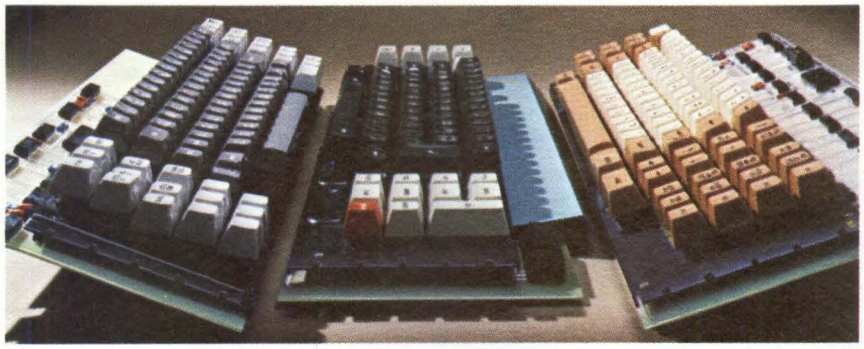

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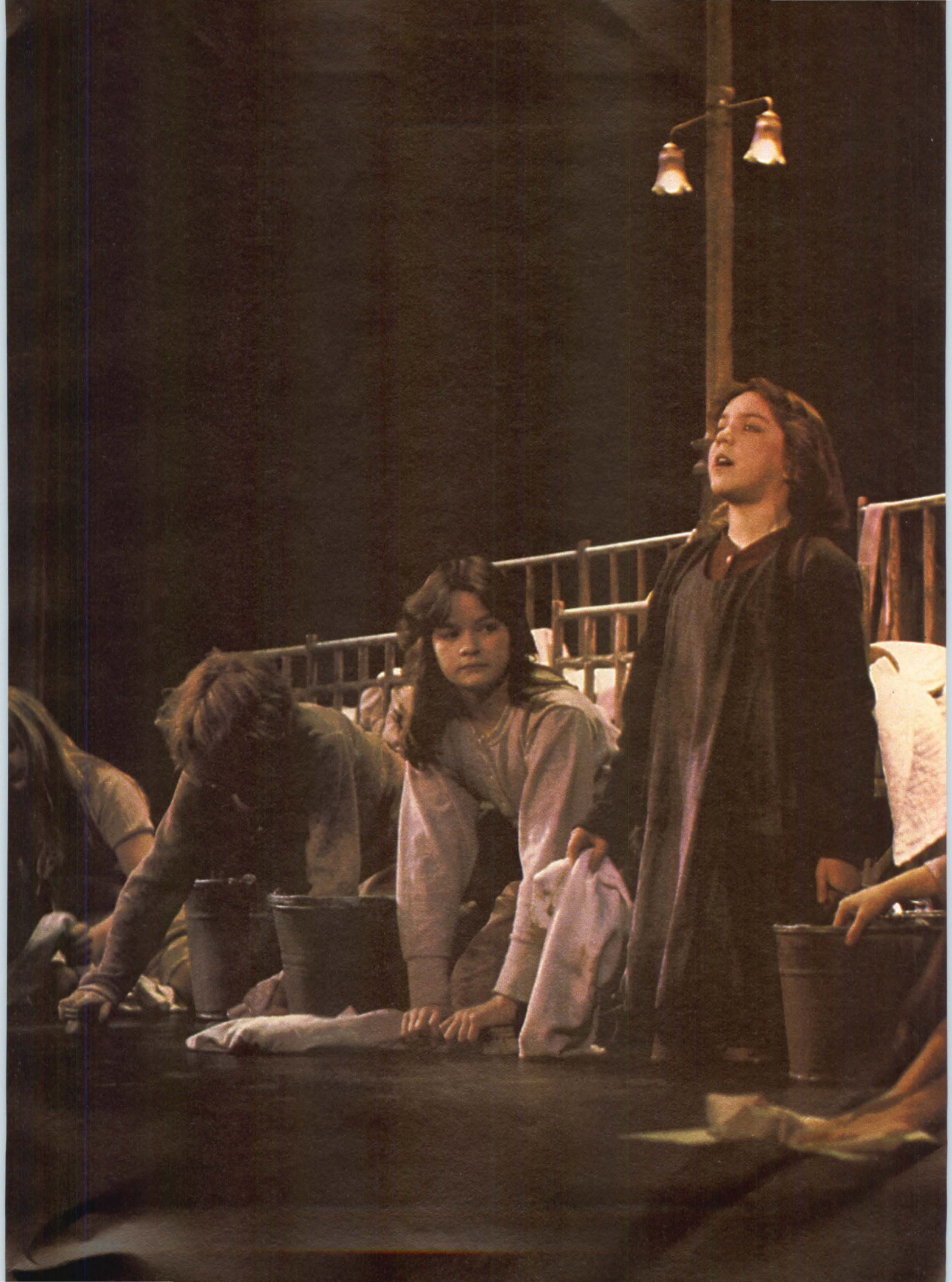
3. (Left bottom) Just as the human eye detects the variations in the visible light spectrum, the OMA-2 provides a real-time readout of wavelengths and intensities of this spectrum. Suitable detectors allow OMA-2 to "see" into the ultraviolet and infrared regions as well.



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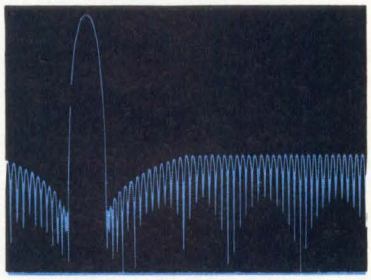

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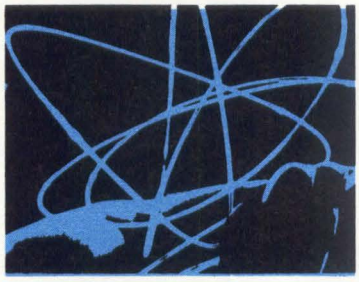

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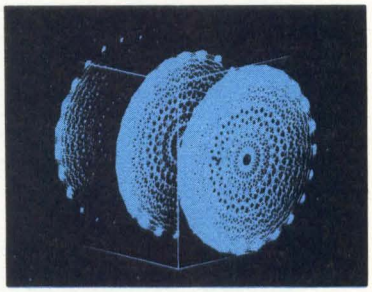

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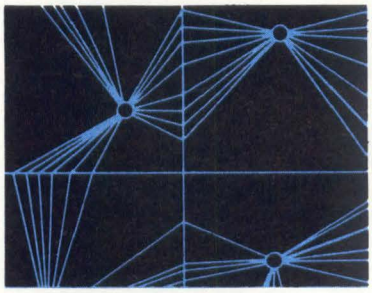

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TECH BRIEF

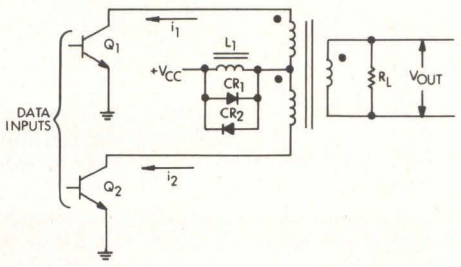
Voltage-Offset Reduction in Data Transmitters

An inductor and a pair of diodes improve the pulse-to-pulse efficiency of a transformer-coupled data transmitter

In transformer-coupled data transmitters, where complementary data pulses alternately drive a pair of identical output transistors, currents flowing through both legs of the primary winding must be of identical amplitude and duration. If the mirror-image primary currents are not equal, the resulting asymmetric output, V_{out}, will contain an offset voltage, V_{os}. This offset may falsely trigger on a receiver connected to the output, if the level detection threshold voltage of the receiver is comparable with the V_{os}. Such asymmetry may be caused by input pulse imbalance (amplitude of duration) or by differences in the conductance of the output transistors.

A current source which consists of an indicator and two silicon diodes may be used to reduce output voltage offset and to make the circuit less sensitive to conductance differences in the output transistors. As illustrated, the supply current i_1 and i_2 flows through inductor L_1. The reactance of L_1 at the data pulse repetition rate (1 MHz in the prototype) is higher than the reflected load impedance; the current flowing through L_1 changes very little from pulse to pulse. The inductor, therefore, acts as a low power-loss source that drives the output transistors with a current sufficient to saturate Q_1 and Q_2, thus retaining high power efficiency.

Diodes (CR_1 and CR_2) limit the voltage drop across the inductor to approximately ±1 V during current buildup at the start of transmission and during gaps between pulses. After the direct current builds up, the ac voltage drop across L_1 becomes small (±0.3 V), and remains low as the inductor regulates current during successive pulses.



Voltage-offset reduction inductor and diodes are common components with inductance of 250 μH and forward voltage drop of 0.6 V, respectively. At pulse repetition rate of 1 MHz, choke reactance is 1.5 KΩ; V_{out} is 15 V peak

Note

This work was done by C. Earle Theall of The Singer Co for Johnson Space Center. For further information, write to: John T. Wheeler, Johnson Space Center, Code AT3, Houston, TX 77058. (MSC-14933).

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INTERFACING FUNDAMENTALS: THE 8085 PROCESSOR

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Concentrating upon the 8080 central processing unit, past columns have contained interfacing and software examples developed for those computer systems. The 8085 processor is now available from Intel Corp with all of the capabilities of the 8080, plus a few additional worthwhile features.

One of the main aspects of the 8085 is that it is software compatible with 8080 machine codes. Thus, 303 is a jump (JMP) instruction in both systems. The 8085 has two additional instructions, however, that will be discussed later. Basic 8080 systems generally include a clock generator and status latch circuit for external control of the central processing unit (CPU). The 8085 chip now incorporates these functions. A simple resistance-capacitance network or crystal may be used directly with the 8085 to generate clock pulses needed by the system. The amount of external logic that is required is further reduced since many of the necessary external device control signals are generated in the 8085 chip.

There is a price to pay for this, though. The 8085 uses one set of eight lines to transmit both data and address information. In some systems, it may be necessary to latch the address bits (A7 to A0) so that they are readily available for use in the system. An Address Latch Enable signal (ALE) is output by the 8085 to control such a latch circuit. This type of bus multiplexing also was done in the 8008, an early general purpose 8-bit microprocessor chip.

A family of 8085 compatible devices makes small computer systems rather easy to design. These chips include the 8155 read/write memory and the 8355/8755 read-only memory devices. Since they require both the address and data information that is multiplexed on a single 8-line bus, they are set up to demultiplex the necessary data

TABLE 1

Internal 8085 Interrupts

Name	Restart Address	Characteristics
TRAP	000 044	Highest priority of all interrupts. Nonmaskable, always "on." Both edge and level sensitive
RST 5.5	000 054	Maskable, logic 1 sensitive
RST 6.5	000 064	Maskable, logic 1 sensitive
RST 7.5	000 074	Maskable, positive edge sensitive

TABLE 2

Instructions to Set and Read Interrupt Mask

SIM, Set Interrupt Mask 060

Accumulator Bits		Function
D0	RST 5.5 Mask	Mask bits for RST inputs on 8085 chip*
D1	RST 6.5 Mask	0 = Enable
D2	RST 7.5 Mask	1 = Disable
D3	Mask Enable	Must be a logic 1 to allow masks to be changed
D4	Reset RST 7.5	Logic 1 clears an RST 7.5 interrupt request*
D5	Not Used	
D6	SOD Enable	Logic 1 loads SOD data to SOD pin (pin 4)
D7	SOD Bit	

RIM, Read Interrupt Mask 040

Accumulator Bits		Function
D0	RST 5.5 Mask	Reads status of current masks
D1	RST 6.5 Mask	
D2	RST 7.5 Mask	
D3	Interrupt Enable	Enables RST 5.5, 6.5, and 7.5
D4	RST 5.5 Input	Reads any pending interrupt requests
D5	RST 6.5 Input	
D6	RST 7.5 Input	
D7	SID Bit	Reads data in from SID input

*All masks are disabled by an external reset

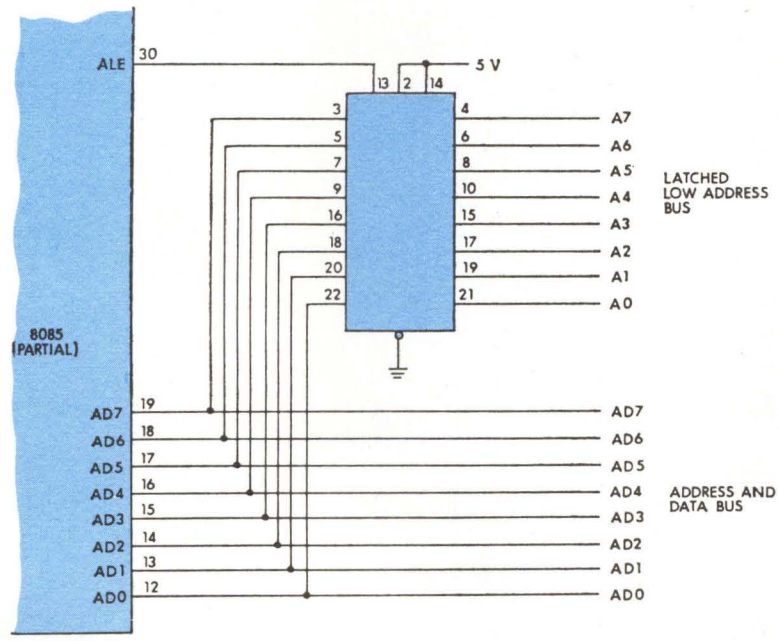

Fig 1 Use of latch to demultiplex 8085's low address bits

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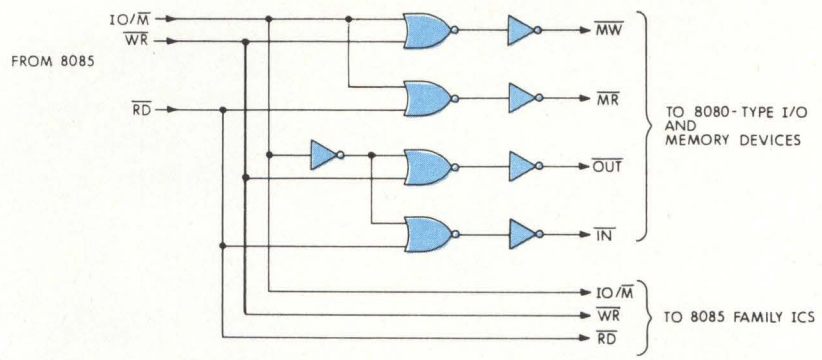

Fig 2 Gating required to generate 8080 compatible control signals in 8085 system

internally. The ALE signal is distributed to all of the 8085 compatible devices to control these internal functions. A latch circuit that will demultiplex the address and data is shown in Fig 1.

The 8085 provides the high address bits (A15 to A8) on eight output pins. Equivalent to the A15 to A8 lines in an 8080 based computer, these signals have no other purpose and are not multiplexed. Other 8085 inputs and outputs (I/Os) such as INTR (interrupt), $\overline{\text{INTA}}$ (interrupt acknowledge), RESET, HOLD, HLDA (hold acknowledge), and READY operate as they do in 8080 systems. Two added outputs from an 8085 are CLOCK OUT, a TTL compatible clock signal of one-half the system clock frequency, and RESET OUT, a signal that may be used to reset other system components. The latter is derived from the reset input to the 8085.

Three control signals—IO/$\overline{\text{M}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$—manage the flow of data to and from the CPU and memories or I/O devices. IO/$\overline{\text{M}}$ is used to indicate the type of device with which the CPU is attempting to communicate: logic 1 denotes I/O devices; logic 0, memories. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals coordinate the reading and writing of data, respectively. The 8085 compatible memory and I/O devices directly use these three signals. In other systems, these signals may have to be used to generate $\overline{\text{MR}}$, $\overline{\text{MW}}$, $\overline{\text{IN}}$, and $\overline{\text{OUT}}$ signals that have been discussed and used in previous columns (see *Computer Design*, May 1976, pp 196, 198, 199, and June 1976, pp 114, 116). Fig 2 illustrates the necessary gating.

While most 8080 based systems implement interrupts with an interrupt instruction port and restart instructions, the 8085 has four onchip interrupts (see Table 1). Overall priority from highest to lowest is TRAP, RST 7.5, RST 6.5, RST 5.5, and INT, which is the normal 8080-like interrupt input. These interrupts have their vector addresses placed within the address space 000 000 to 000 100, as is the case with the usual 8080 interrupts. Some of these addresses are placed between the 8080 vector addresses, leaving only four bytes of storage space between interrupt vector addresses. Most programmers use jump instructions to point to areas of memory that allow for longer interrupt service programs. These interrupts act in the same manner as normal 8080-like interrupts, so a stack is still a necessity. If these interrupt inputs are not to be used, they should be grounded.

A single input and a single output pin on the 8085 chip can be controlled directly by software. Of course, the 256 addressable I/O port capability is still maintained. The two single I/O connections may be used for a single sense input and a single control output, or for serial I/O to a terminal or teletypewriter, with the actual serialization being done in software.

Two new, 1-byte instructions are implemented in the 8085 for management of interrupts and two I/O lines—Serial Input Data (SID) and Serial Output Data (SOD). These two instructions are Set Interrupt Mask (SIM = 060) and Read Interrupt Mask (RIM = 040). The A register is used as the source or destination of the data bytes for each operation (Table 2).

These instructions are powerful, since they allow the user to select certain devices for interrupts, to check interrupts, and to control an input and an output line. These instructions do not affect other 8080-type operations, except that the A register or accumulator is used. Due to these functions, a small microcomputer based controller can be configured with a few integrated circuits. Future columns will describe how this can be done and how 8085 compatible chips can be used.

This article is based, with permission, on a column appearing in *American Laboratory* magazine.

Note: "Designing With Microcomputers," a 3-day course offered by Tychon, Inc in Blacksburg, Va from Sept 11 to 13, will cover the design of 8085 systems. Each participant will design and wire an 8085 based computer system that he may keep. Other interfacing and software courses also are being offered at this time. Contact Christopher Titus, Tychon, Inc, Blacksburg, VA 24060, tel: (703) 951-9030 for information.

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Editor's Note: With the ever increasing importance of microcomputer and microprocessor technology, *Computer Design* has found the Micro Processor/Computer Data Stack department, in existence since Aug 1975, to be too confining. Thus, beginning with this issue, it is being transformed into two departments—Micro Data Stack/ Processors and Elements, and Micro Data Stack/Computers and Systems—each to be prefaced by a featurette. The intent is to provide our readers with in-depth coverage of the massive amounts of developmental, technological, and product information in the most direct and convenient manner possible.

Comments, both critical and complimentary, and suggestions for improvement are invited. In this way will we be able to adapt the department to meet our readers' requisites.

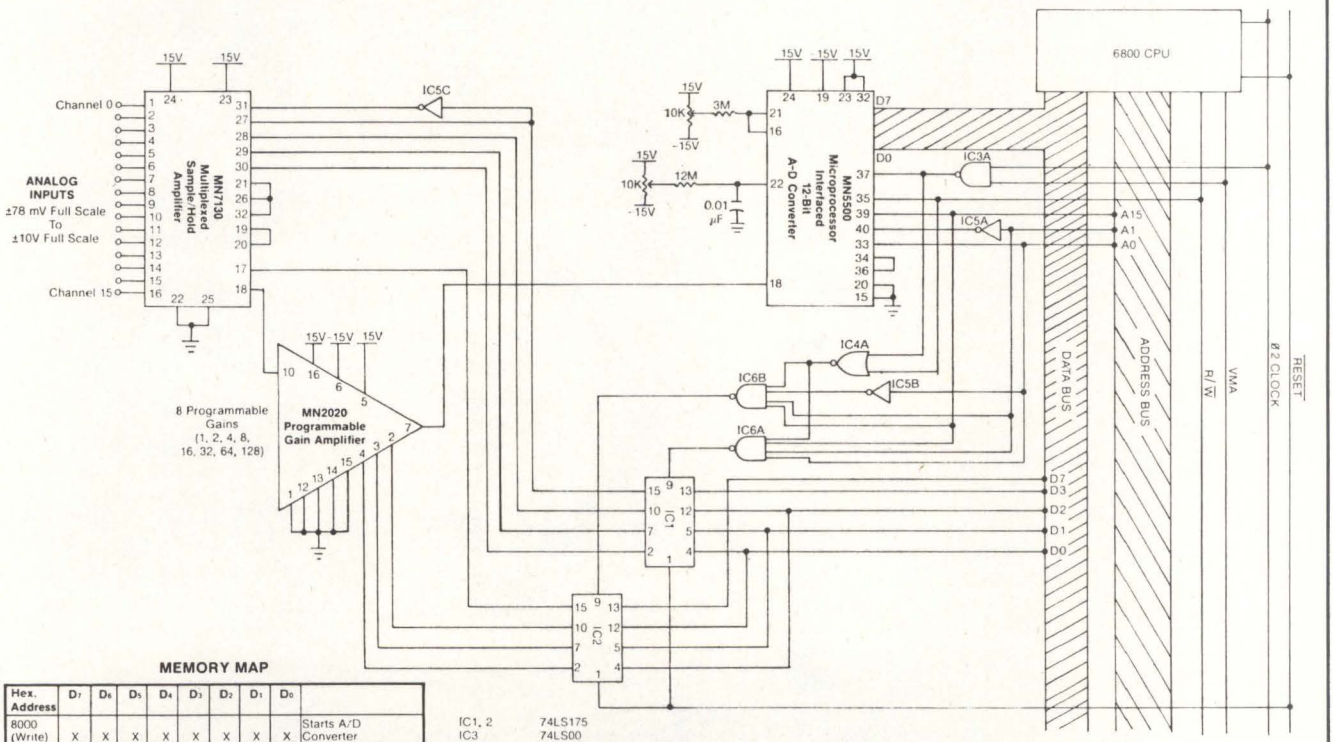
Each month, the Processors and Elements section will highlight individual devices such as microprocessors, memories, interface circuits, elements intended specifically for use with microprocessors, microprocessor development systems, logic analyzers, and software (at the development level).

12-Bit D-A and A-D Converters Add Analog Input and Output Capability to Microprocessor Based Systems

Savings in both board space and design/development time are obtained from two converters having 12-bit resolution. With the single hermetic DIPs, microprocessor users have a complete interfaced D-A or A-D function, so that it is no longer necessary to buy multichannel I/O boards or to design and build interface circuitry.

Both the MN3500 D-A and MN5500 A-D converters have been designed by Micro Networks Corp, 324 Clark St, Worcester, MA 01606 with universal microprocessor interfacing logic. Either easily interfaces to 8-bit microprocessors to add analog input or output capability. They provide internal circuitry for chip select, read/write, and address decoding, as well as "active low" acknowledge outputs. In addition, the DAC is double buffered to insure smooth transitions between analog output values and to eliminate unwanted intermediate states. The ADC also provides 3-state outputs.

In normal operation, the devices are connected to the microprocessor's address, control, and data buses and are each treated as two successive memory mapped or I/O locations. Writing to these two locations will



MEMORY MAP

Hex. Address	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
8000 (Write)	X	X	X	X	X	X	X	X	Starts A/D Converter
8001 (Read)	STATUS	"1"	"1"	"1"	MSB	Bit 2	Bit 3	Bit 4	Digitized Data MSB Byte
8000 (Read)	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	LSB	Digitized Data LSB Byte
8002 (Write)	S/H	X	X	X	X	A_2	A_1	A_0	PGA Gain S/H Command
8003 (Write)	X	X	X	X	A_4	A_3	A_1	A_0	Multiplexed S/H—Channel Address

IC1, 2	74LS175
IC3	74LS00
IC4	74LS02
IC5	74LS04
IC6	74LS20

Combining low cost, complete functions, and small DIL packaging, Micro Networks' MN5500 microprocessor interfaced, 12-bit A-D converter provides analog input capability for 16-channel data acquisition system. Either 8- or 16-channel systems can be configured using the MN7130 S/H amplifier. With the MN2020 programmable gain amplifier, full-scale analog input ranges from ±20 mV to ±10 V and autoranging capability under processor control are provided. Comparable MN3500 DAC supplies analog output capability for configuring multichannel data distribution systems

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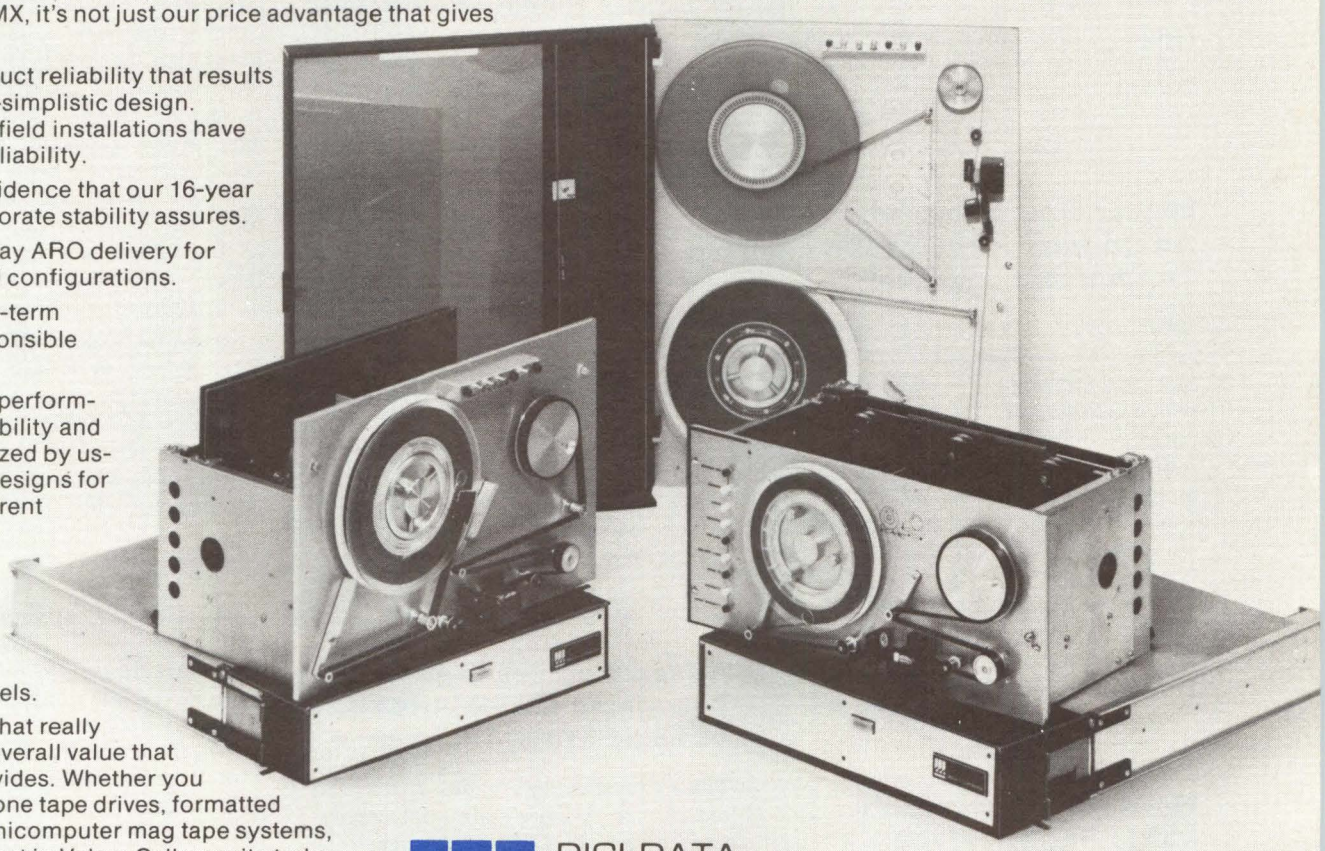

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load and latch the digital data into the internal DAC, and changes the analog output voltage.

With the ADC, writing to the first location initiates a conversion. The digitized data are available both directly and as two 8-bit bytes addressable by a microprocessor. When conversion is complete, the converter generates a status output that is available on the data bus for software interrupt or as a logic signal for hardware interrupt. The microprocessor then reads the two locations assigned to the ADC, retrieving the MSB and LSB data.

The converters offer ±½ LSB maximum linearity error over the full operating temperature range, as well as five user selectable input and output voltage ranges, two unipolar and three bipolar.

In addition, the 3500, priced at $90/100, has a 3-$\mu$s settling time and 1125-mW power consumption. The 5500, with a price of $129/100, guarantees no missing codes over the full operating temperature range; it features a 25-μs max conversion time and 1040-mW power consumption.

Circle 420 on Inquiry Card

Higher Operating Temps Adapt Microprocessors To Control Equipment

S6800 microprocessors have been adapted to meet the needs of manufacturers designing microprocessor controlled systems for operation over an extended temperature range. The industrial and military temperatures announced by American Microsystems Inc, 3800 Homestead Rd, Santa Clara, CA 95051 are between −40 to 85 °C and −55 to 125 °C, respectively. The ceramic packaged units sell for $35.30 (industrial) and $68.40 (military) in quantities of 100.

Circle 421 on Inquiry Card

Hardware Compatible LSI-11 Bus Interface Decodes GPIB Commands

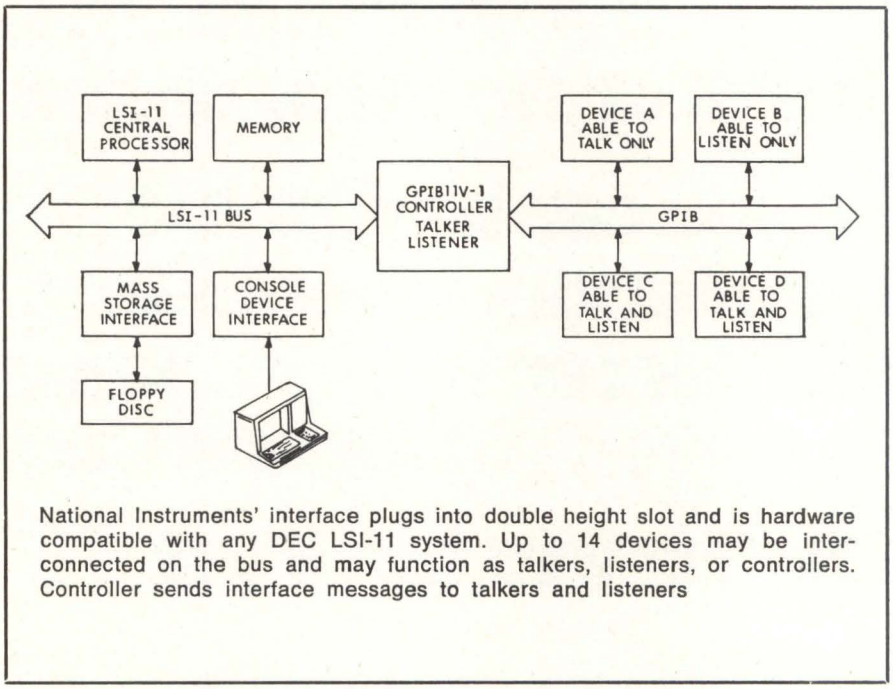
LSI-11 measurement and test systems are easily implemented with the hardware compatible GPIB11V-1 interface to the IEEE Std 488-1975 bus (also referred to as GPIB or HP-IB). It provides the necessary hardware for decoding GPIB commands in order to implement talker, listener, and controller functions, both in single and multiple controller environments.

The interface, produced by National Instruments, PO Box 9922, Austin, TX 78766, connects to the 16 signal lines of the bus. Standard bus cables with piggy-back connectors interconnect up to 14 instruments or devices to the LSI-11 bus of such systems as the LSI-11/2, PDP-11/03, and PDP-11V03.

Software support includes drivers, utilities, diagnostics, and an interactive control program. Utility and driver programs are available as MACRO source files that may be assembled as FORTRAN, BASIC, or MACRO callable subroutines. The driver program can be used in a standalone environment or as a device handler under the RT-11 operating system. The utility program performs most common sequences of bus functions, and includes a device table of specific information on each interfaced device so that they may be referenced by logical unit number rather than by GPIB addressing details.

GPIB functions are performed interactively and at a low level through the interactive control program, to facilitate debugging and instrument checkout. The $695 interface includes a 4-m cable with a GPIB connector on the outboard end.

Circle 422 on Inquiry Card



National Instruments' interface plugs into double height slot and is hardware compatible with any DEC LSI-11 system. Up to 14 devices may be interconnected on the bus and may function as talkers, listeners, or controllers. Controller sends interface messages to talkers and listeners

Added Modules Expand Debugging Capabilities of Logic State Analyzer

Three personality modules for the model 1611A logic state analyzer extend design and debugging capabilities to 1802A (option A18), 6502A (option A65), and 8085 (option A85) microprocessor based systems. The user configures the analyzer (see *Computer Design*, Sept 1976, p 120) for a specific system by selecting the desired module and installing it in about 15 min.

Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304 offers the modules in kit form with two PC boards, a replacement section of front panel, and a dedicated microprocessor probe for $1250 each. Kits are also available for the 6800, 8080, F8, and Z80 microprocessors.

Circle 423 on Inquiry Card

FOR RENT...NOW...

Hewlett-Packard's new, easy-to-use 1640A Serial Data Analyzer that simplifies analysis of your computer network by identifying and locating failures all the way down to the component level.

You don't have to be a programmer to use the new HP 1640A, nor learn instruction sets, nor write and debug programs. All you have to be is someone who wants to monitor a RS232C (V24) interface, measure time intervals, or simulate a network component.

The new Serial Data Analyzer is very easy-to-use, even for a semi-skilled operator. It comes with mylar overlays—pre-labeled for your application—which cut down on the time required to set-up and minimize the chance of errors. Your operator will enjoy the menu set-up concept with its keyboard parameter entry, pre-programmed measurement execution and transparent "wake-up" mode. The operator can quickly identify and isolate problems to the network component level, and flexible triggering allows the trapping of data errors, time-interval violations or invalid protocol sequences. Most problems may be located in a non-intrusive "monitor" mode, but the amazing new 1640A also simulates the CPU, terminal or modem to handle subtle problems or conduct loop-back tests. Plus, the new instrument can be operated with any combination of transmission modes—Simplex, Half Duplex or Full Duplex; 2-wire or 4-wire links; synchronous or asynchronous operation; and up to 9600 bps (19200 HDX) data rates.

Whether you're integrating a minicomputer with a few terminals or analyzing a complex, centralized CPU-based communication network, the low-cost 1640A will solve your problem while reducing system debugging time.

You can use the 1640A to locate problematical problems in your computer network before they cause a network failure. And you'll enjoy the real-time display of FDX data in ASCII, EBCDIC or Hex. Trigger specifications are continuously displayed, and measurement results are clearly displayed as well. Up to 480 characters may be displayed on the large screen. It's very easy to see exactly what's happening in your system. 1640A memory includes 2048 characters of monitor buffer and 1024 characters of transmit message buffer. Error checking is provided at odd, even or no parity. The lightweight (25 pound) 1640A Serial Data Analyzer from HP is on-the-shelf at Rental Electronics now. It's For Rent . . . for you.

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CIRCLE 48 ON INQUIRY CARD

Development Systems Operate With 6802 and 8085 Microprocessors

Plug-in modules for the 6802 and 8085 have been introduced as the fourth and fifth microprocessors supported by the development system line of Futuredata Computer Corp, 11205 S La Cienega Blvd, Los Angeles, CA 90045, which currently handles the 8080, 6800, and Z80 microprocessors, described in the Feb 1978 issue of *Computer Design*, p 156. Both disc and tape based Microsystems give hardware and software development capabilities. They include the CPU with up to a 64k memory, 960-char CRT, ASCII keyboard, and operating system software.

Containing the same features as well as optional accessories and software as the previous systems, Microsystem/31 has the Microdisk/3 dual 8" (20-cm) double-density floppy and 16k memory; /32 has Microdisk/4 double-sided floppy and 16k memory. The /15 has 32k RAM and the company's Quickrun™, a coresident assembly and interactive debugging system.

Circle 424 on Inquiry Card

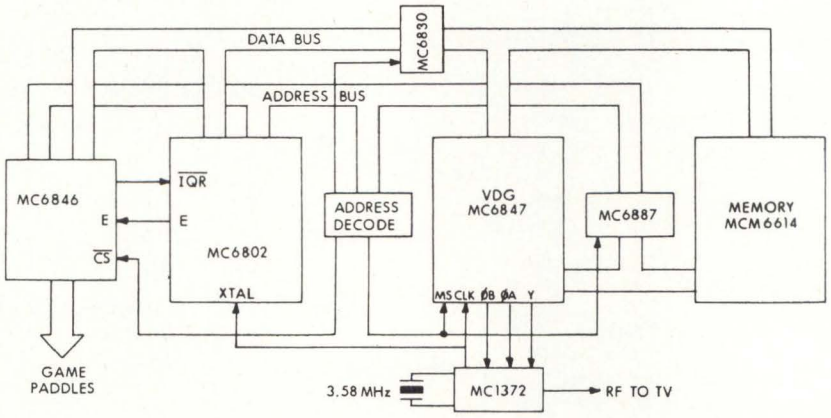
Video Display Generator Interfaces 6800 Family To Color or B/W TV

The MC6847 video display generator (VDG) produces four alphanumeric and eight graphic display modes as a means of interfacing the company's M6800 microprocessor family (or similar products) to either a color or black and white television receiver, for graphics uses in such areas as video games, displays, education, and communications. It reads data from memory and produces a full composite video signal that permits the displays to be generated.

Four analog outputs are used to transfer luminance and color information to an NTSC color TV receiver via the compatible MC1372 RF modulator or into Y, ϕA, ϕB, TV video inputs. The composite video may be modulated to channel 3 or 4. The up modulated signal may be applied to a color TV's antenna.

Eight TTL compatible inputs control the VDG's operating mode. All alphanumeric modes have a selected video inverse, and display 32 char/line x 16 lines. Two modes offer 8-color 64 x 32 or 4-color 64 x 48 density graphics. An internal ROM generates 64 ASCII display characters in a standard 5 x 7 box; a 512-word display memory is required. Two compatible semigraphic modes are offered.

Eight full graphic modes require 1k to 6k bytes of memory. Densities of 64 x 64, 128 x 64, 128 x 96, 128 x 192, or 256 x 192 are available. Either 2- or 4-color data structures are allowed. Depending on the color set select pin, these modes include an outside color border in one of two colors for the 2-color sets, or one of two sets of four colors in the 4-color mode.



Video display generator from Motorola Semiconductor may be used in typical TV game application. Interfacing with the M6800 family of microprocessors, unit reads memory and produces composite video signal to generate four alphanumeric and eight graphic display modes

Motorola Semiconductor Products, Inc, 3501 Ed Bluestein Blvd, Austin, TX 78721 has included an internal multiplexer in the VDG to allow the use of either the internal ROM or external character generator; this generator extends the internal character set for limited graphic shapes. A mask programmable internal character generator ROM may be special ordered.

The 13 TTL compatible address lines scan the display memory; 8 TTL compatible data lines input data from RAM to be processed by the VDG. Power input requirements are 5 V for V_{cc} and 0 V for V_{ss} (normally ground). The 40-pin plastic or ceramic DIPs are available in either an interlace or noninterlace mode, with an operating temperature range of 0 to 70 °C.

Circle 425 on Inquiry Card

Card Supports 6800 Design/Debug, and Expands Fault Diagnosis

A plug-in microprocessor personality card for the MicroSystem Analyzer (*Computer Design*, Dec 1977, p 124) has been announced by Millennium Systems, Inc, 19020 Pruneridge Ave, Cupertino, CA 95014; inexpensive hardware/software integration and fault diagnosis of products employing the Motorola 6800 microprocessor may be handled in both production test and field service applications. Swapping personality cards adapts the analyzer to different microprocessors.

The upgraded fault diagnostic feature provides pulse, interval, and frequency measurement as well as transition and pulse counting to analyze the clock, clock driver, and logic circuits. The EM-6800 personality card is priced at $895.

Circle 426 on Inquiry Card

INTRODUCING THE BENDIX PORTABLE MODULE TESTER

Now automatic, on-the-spot module testing is on the way.

Here's a new way to test anything from a printed circuit board to a complex logic system. And you can do it on the job.

Our new portable unit weighs just 30 pounds and has no moving parts. Yet it does everything that stationary digital cabinet-type units can. It eliminates downtime while modules are tested away from the job site. Does away with trial-and-error testing and unwarranted returns, too.

You can take it on board planes or ships, to hospitals, to labs, to computers or communications equipment, and to sophisticated quality-control operations in mass production plants.

Highly trained operators are not needed. Programming procedures are so easy to pick up. And an interactive display system makes operation easier still. Test systems are stored on solid-state cards, providing reusable data memory.

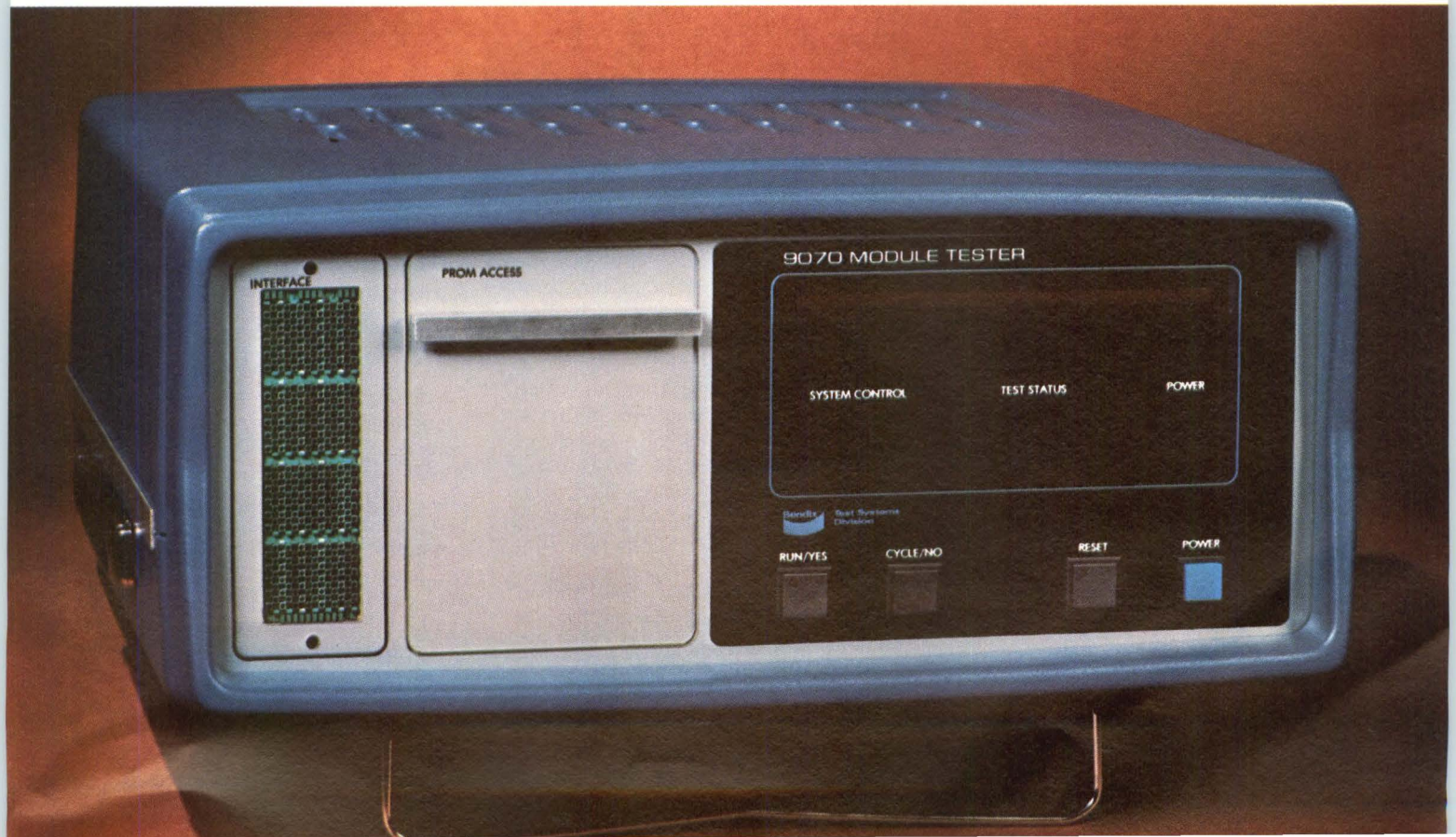
The Basic Bendix unit is capable of testing cards to 64 pins and has the capacity to expand to 256. Additional options are available including:

- Fault Isolation Testing
- Digital Voltmeter/Frequency Counter
- Teletype Interface and Advanced Software Aids.

For more information, contact: Bendix Corporation, Test Systems Division, Teterboro, N.J. 07608. Or call (201) 288-2000, extension 1789.

Bendix

CIRCLE 49 ON INQUIRY CARD



SOFTWARE

Software Program for PDP-8 Simulates 6800 Microprocessor Functions

Alternative binary paper tape versions of the Motorola M6800 microprocessor simulator have been developed for PDP-8 systems with either MIKBUG or MINIBUG debugging aids. The Mechanical Engineering Dept at The University of Manchester Institute of Science and Technology, PO Box 88, Manchester M60 1QD, England has produced the program for PDP-8 users who wish to develop microprocessor equipment, consider its possible applications, or demonstrate and teach its programming techniques without first investing in special purpose hardware.

The PDP-8 should have at least an 8k-word memory and paper tape input so that the microprocessor program under test can be generated on paper tape by cross assemblers. All computer memory above field 0 may be used to simulate RAM and ROM. Register and memory contents may be displayed or modified; programs execute continuously or in trace mode. Up to four breakpoints facilitate program testing and timing in conjunction with the cycle count feature.

Circle 427 on Inquiry Card

Utilities Package Rounds Out Capabilities Of ISIS Operating System

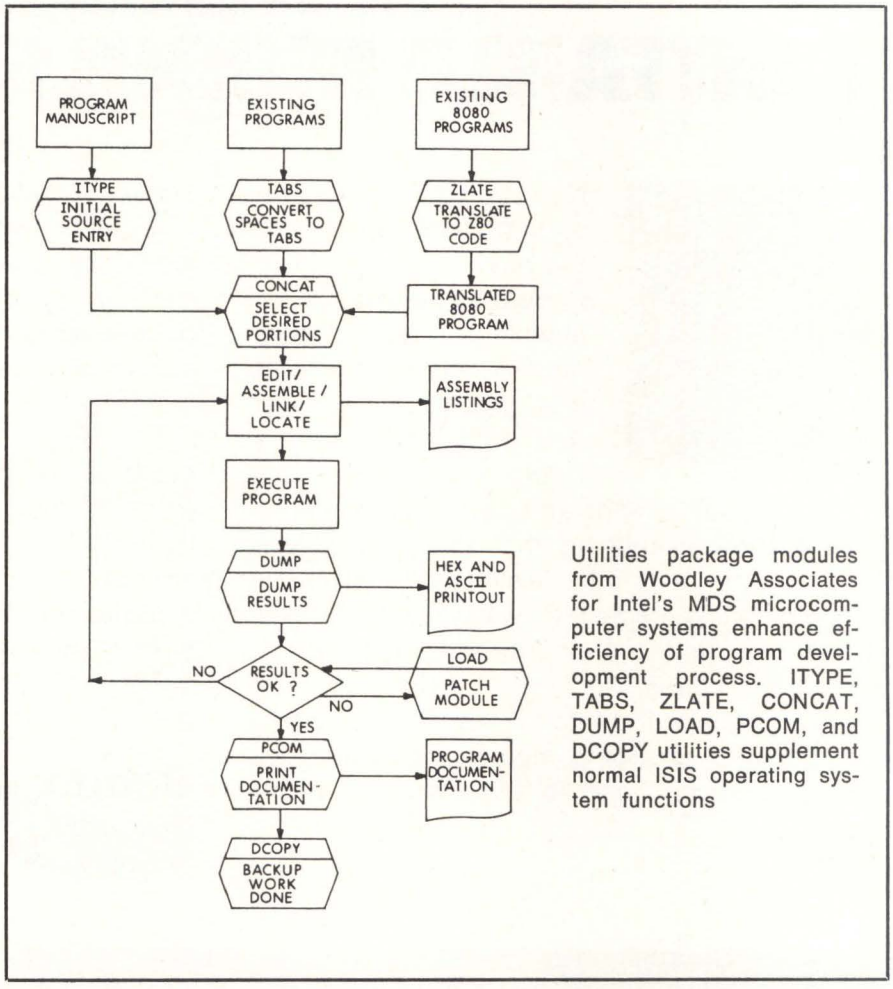
A software utility package for Intel microcomputer development systems improves the efficiency of the software development process while adding to the functions normally provided by ISIS I or II operating systems. Allowing pause/continue/stop control and performing extensive error checking, modules in the package fulfill many functions.

The ITYPE utility is a source data program that allows initial data entry by personnel unfamiliar with the computer. The file compaction/expansion program (TABS) converts spaces to tabs and vice versa in a controlled manner. ZLATE translates code written in Intel 8080 language to the Zilog Z80 language; CONCAT, a file concatenation program, allows new files to be built out of any portion of existing files; and the DUMP program permits examination of any disc file and detection of errors in any program generating or using such files.

Another utility allows disc files to be loaded, patched, and saved with various options; they also may be compared with contents of memory. PCOM automatically produces software documentation by printing selected portions of source files. Disc backup on a byte-for-byte basis is done quickly by DCOPY; the new disc may be renamed if desired.

Woodley Associates, 604 Indian Home Rd, Danville, CA 94526 has released the package with modules supplied on a dual- or single-density diskette. It is written in Intel 8080 macro language and requires a minimum of 32k bytes of memory and the ISIS I or II operating system.

Circle 428 on Inquiry Card



Utilities package modules from Woodley Associates for Intel's MDS microcomputer systems enhance efficiency of program development process. ITYPE, TABS, ZLATE, CONCAT, DUMP, LOAD, PCOM, and DCOPY utilities supplement normal ISIS operating system functions

Price Reduction Announced on 6500 Cross Assemblers

Two versions of cross assemblers for the 6500 microprocessor family have been repriced by Computer Applications Corp, 413 Kellogg, Ames, IA 50010 at $600, including test programs and 1-year support. FORTRAN based assemblers are available on magnetic tape for IBM, CDC, Xerox, and Honeywell computers. The MINMIC 1165, written in MACRO11, is available for any PDP-11 using the RT-11 operating system. Distributed on floppy or RK05 disc, assembler needs only 5k words of memory. □

Circle 429 on Inquiry Card

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CIRCLE 50 ON INQUIRY CARD

ALTAIR TIMESHARING BASIC

Susan Blumenthal and Stan Webb

Pertec Computer Corporation, MITS/Microsystems Division
Albuquerque, New Mexico

Primary design goals of the Altair Timesharing BASIC system were directed toward developing an operating system that would realize the maximum potential of the 8080 microprocessor's capabilities. In addition, it would provide efficient management of hardware resources, program development and debugging facilities, and responsive service to as many as eight users simultaneously and independently sharing a single Altair 8800 series microcomputer. Other design considerations (some unique to microcomputing) included providing security for each user's resources, systematic job rotation, program loading and storage, fixed memory locations, and interfaces to a variety of peripherals.

To isolate individual users so that each job and operating system is protected against alteration and destruction, the system's architecture is structured with memory partitions that confine each user to a fixed region of memory. Memory sizes (established during the initialization dialogue) vary according to each user's need. With diskette files, passwords are used to restrict access to specific files and individual diskettes, thus insuring security.

Job Rotation and Scheduling

Sharing of central processing unit (CPU) time by multiple users, to prevent a single user from dominating the CPU, was accomplished by implementing an interrupt driven, time-slice facility. Round-robin scheduling allows each process to run until it is input/output (I/O) bound or until it exhausts its time-slice.

Based on I/O and timer interrupts, this scheme utilizes an I/O interrupt handler to control the status of a process awaiting input or output. The vectored interrupt realtime clock generates an interrupt at a 60-Hz rate. Each time an interrupt occurs, the interrupt handler gains control, updates the time of day clock, and decrements the current user's time-slice counter. When that user's time-slice counter reaches zero, the allocated quantum of time has elapsed, and a new user is given access to the CPU.

Operating System Problem Analysis

Functions of the BASIC interpreter were defined to fit the multiuser system design goals. To coordinate process activity, an operating system that could be implemented in hierarchical levels was devised. The interpreter manages the hardware (ie, performs all I/O functions and controls the user's access) and interprets the BASIC programs, translating source program instructions into a series of subroutine calls that are executed immediately. In a single-user system, this hardware management is incidental to the actual interpretation process. In contrast, a system with shared resources requires a more sophisticated hardware management system to prevent simultaneous access to such shareable resources as the line printer and diskette. Thus, hardware functions were separated from the BASIC program interpretation. An operating system with a supervisor that controls the sequencing of programs being executed was designed to coordinate the hardware and I/O management.

In the Altair timesharing operating system, each user's terminal is a dedicated device so exclusive access to individual terminals presented no conflicts. However, terminal I/O routines of the BASIC interpreter were modified to issue a supervisor call (SVC) that transfers control to the operating system to drive the devices. In regular versions of Altair BASIC, these devices are driven directly by the interpreter.

Management of the line printer and diskette was more complex, because they can be accessed by all users in the system. To resolve this conflict, users requiring line printer access are placed in a WAIT queue if output from another user is already in progress.

The problem of multiple diskette access was solved by separating the physical (diskette oriented) and logical (file and record oriented) operations of the BASIC file manager. Physical I/O was made a function of the supervisor, accessible through a single diskette I/O SVC. The file manager was then modified to perform all I/O operations through this SVC.

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93471	TTL-3S	45 ns Max	650 mW Typ	Production
93L471	TTL-3S	45 ns Max	375 mW Typ	Samples
10470	ECL-10K	35 ns Max	800 mW Typ	Production
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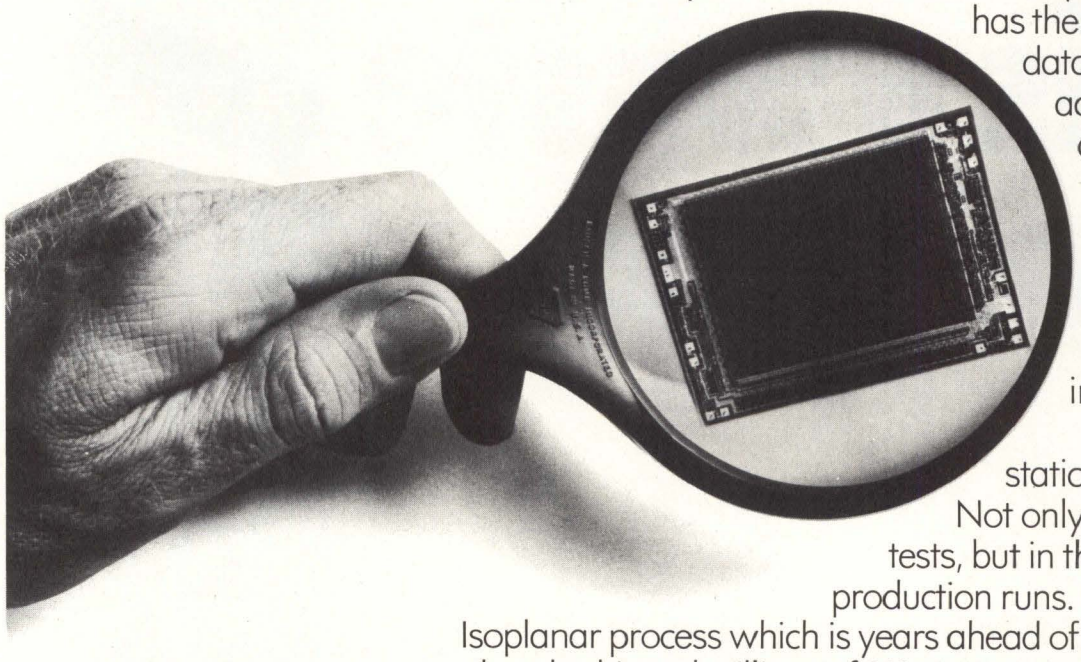

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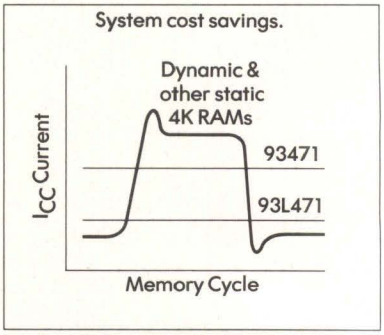

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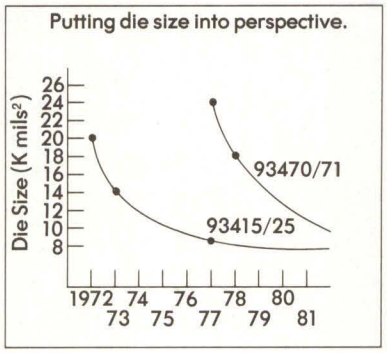

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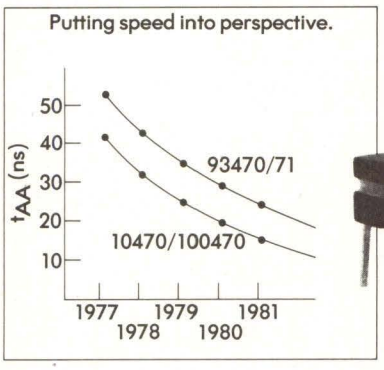

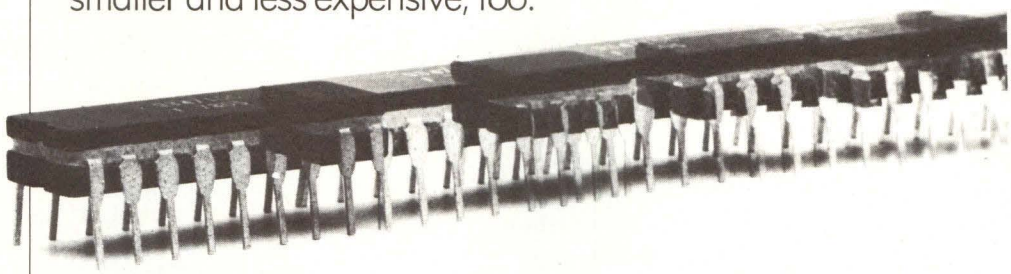

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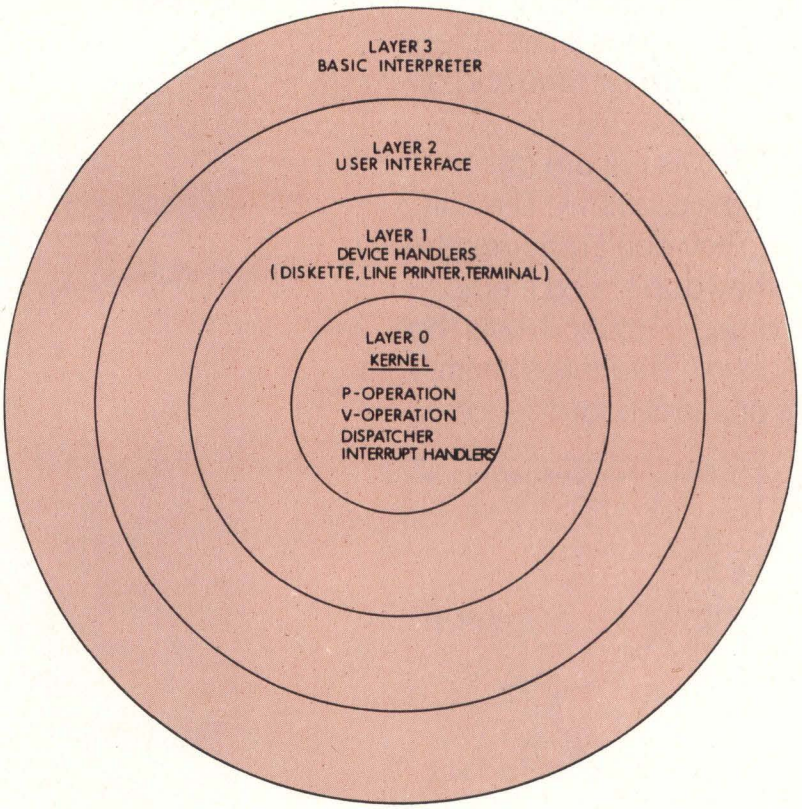

Operating system's internal structure separates Altair Timesharing BASIC interpreter from hardware. Layered architecture is comprised of kernel (multitasking support) on bottom level holding dispatcher, P-operation, V-operation, and interrupt handlers; more complex functions are built up from this. Next is the device handling layer of supervisor routines and I/O drivers, followed by user interface level containing supervisor and SVC handler

Establishment of Sequential Processes for Data Base Management

I/O conflicts arising in this multiuser system were resolved by the creation of two synchronization processes. They assign a device and synchronize user entry and exit from the device and its associated data base (in this instance, buffers, pointers, counters, and other data that track or coordinate program activity). The P-operation in effect "locks" a device or data base after it is accessed by one user to prevent simultaneous access by another user. The V-operation then "unlocks" the device upon completion of the activity to allow access by a new user. This concept of process synchronization was first introduced by Edsger Dijkstra.*

The P-operation and V-operation are performed on semaphores (signaling devices) associated with each data base. The initial value of the semaphore is an integer that corresponds to the number of users allowed to access that data base at one time. In this timesharing BASIC, the integer value is one.

Before a user accesses a data base, the process issues an SVC to perform a P-operation on the semaphore associated with that data base. The P-operation decrements the semaphore by one. If the resulting value is less than zero, the data base is, in effect, locked by a previous user. The requester is added to the queue of jobs awaiting access to that data base. Conversely, as a user exits a data base, an SVC is issued to perform a V-operation, which increments the semaphore by one, unlocking a data base. The two operations are indivisible and run with interrupts disabled.

These synchronizing processes can be illustrated in terms of line printer usage. The semaphore associated with the line printer has an initial value of one. User A performs a P-operation on the semaphore, decrementing it. The result is a nonnegative integer, allowing user A to access the line printer. While output is in progress, user B performs a P-operation. The semaphore value is now −1. The status of user B is changed to "blocked"; thus, it is unable to execute. When user A exits the device, line feeds are performed to position the new page and user A performs a V-operation. The line printer semaphore is now a nonnegative integer with a value of zero. User B, the first process waiting on the semaphore, is changed to a "ready" status and is allowed to access the line printer.

*E. Dijkstra, "Cooperating Sequential Processes," *Programming Languages*, Academic Press, New York, 1968, pp 43-110

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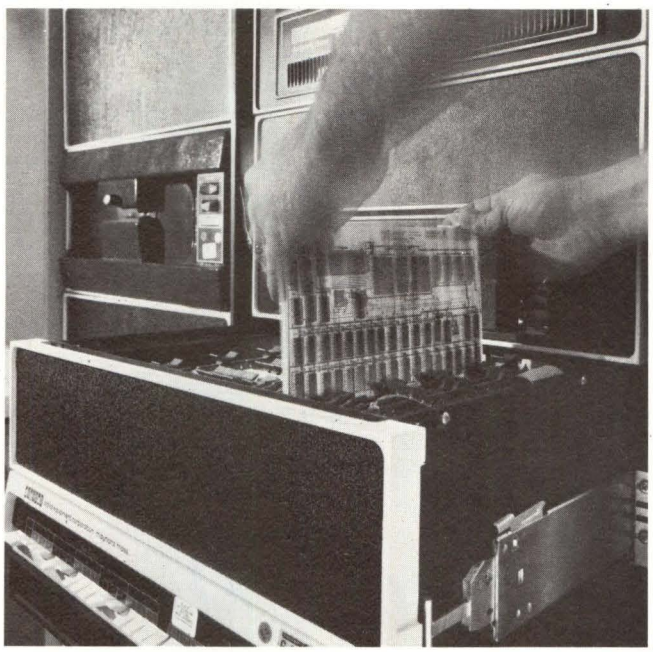

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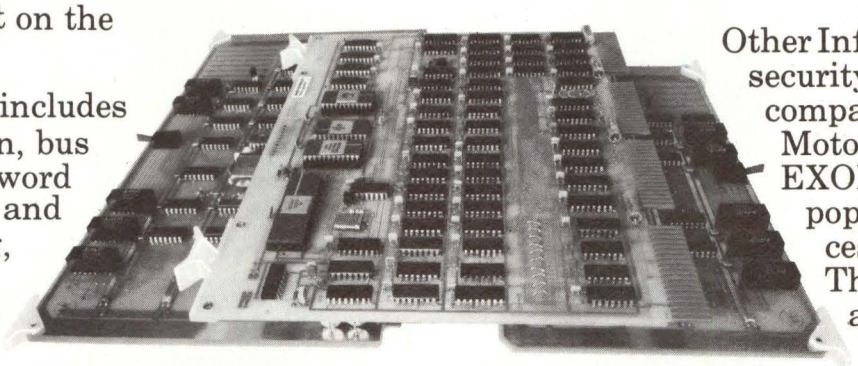

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Internal Structure of the Operating System

Sequential processes are nested within the internal structure of the operating system, which was designed with a layered architecture to separate the BASIC interpreter from the hardware (see Figure). The bottom level, or kernel, is the multitasking support layer. It consists of several basic facilities: the dispatcher, P-operation, V-operation, and interrupt handlers. Operating system functions of greater complexity are built from this lower level.

The dispatcher in the kernel level is composed of the selector and starter that together control process execution. The selector scans the entire list of tasks to find a previously blocked process to start; control is then transferred to the starter. If there are no tasks in a ready state, an idling task takes control. The idler task remains in control until a process is no longer blocked and is ready to run. At that time the idler task relinquishes control to the selector. The starter then reestablishes the process to its previous status by restoring the contents of all registers, the program counter, and stack.

The V-operation signals the availability of a device or data base to the next process awaiting access to that resource. This is done by incrementing the semaphore associated with a data base. If the resulting value is not greater than zero, the next process awaiting access is marked as ready to be selected by the dispatcher. The I/O interrupt handler, another component of the kernel, converts interrupts from the various devices into V-operations.

The second layer of the operating system—the device handling layer—contains the supervisor routines and I/O drivers. The supervisor in turn is composed of system subroutines including terminal control facilities such as enabling or disabling, echoing, switching console devices, and changing terminal line width.

Three types of I/O drivers are line printers, diskettes, and terminals. Synchronous devices (line printer and diskette) were established with linear buffers that are filled character by character from one end until full. The buffer's entire contents are then output to the appropriate device. In contrast, the asynchronous terminals required a more flexible buffering system to operate in full-duplex mode. This was achieved with circular buffers, which are filled from one end and emptied from the other, allowing the I/O handler to insert or remove single characters from the buffer.

Built upon the device handling layer is the user interface layer containing the supervisor and SVC handler. This routine provides the standard linkage to pass information between subroutines, and furnishes a common entry point that is the address of the subroutine and caller. When a user task requests a service provided by the supervisor, an SVC is issued. Each SVC contains an identification code designating the function to be performed. The SVC handler saves the state of the task at the time of the call, examines the SVC code, and selects the proper system routine to be called. When the system routine returns to the SVC handler, it restores the user to the precall state and adds the returned values.

Expansion of Altair BASIC and the 8080 processor based system for operation in a multiuser environment represents a major step forward in the implementation of microprocessors. Problems with hardware limitations, specifically the 8080 instruction set, were encountered in the design of a microprocessor controlled operating system; also, certain programming constructs for writing reentrant modules required numerous 8080 instructions. The result was a cost-effective multiuser timesharing system with a slower but very acceptable throughput, closely matching the efficiency of larger systems.

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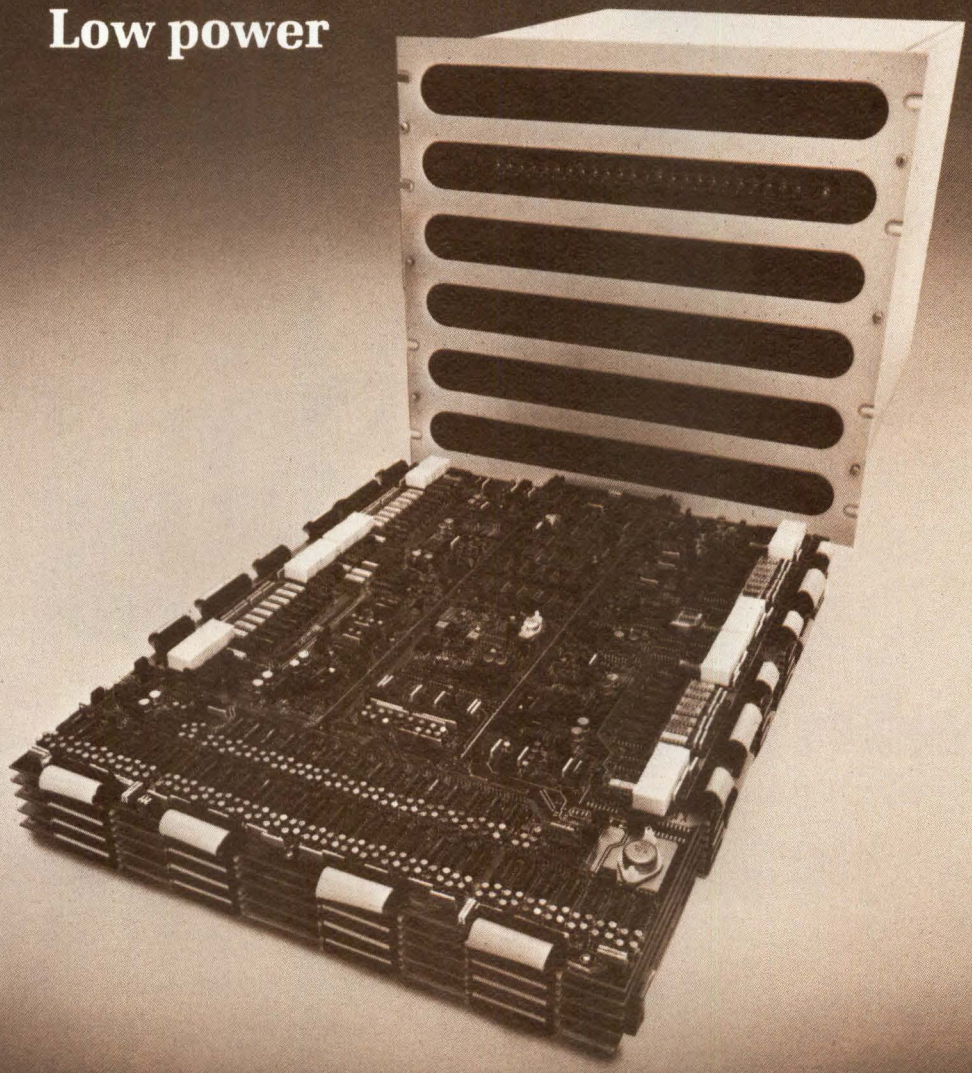

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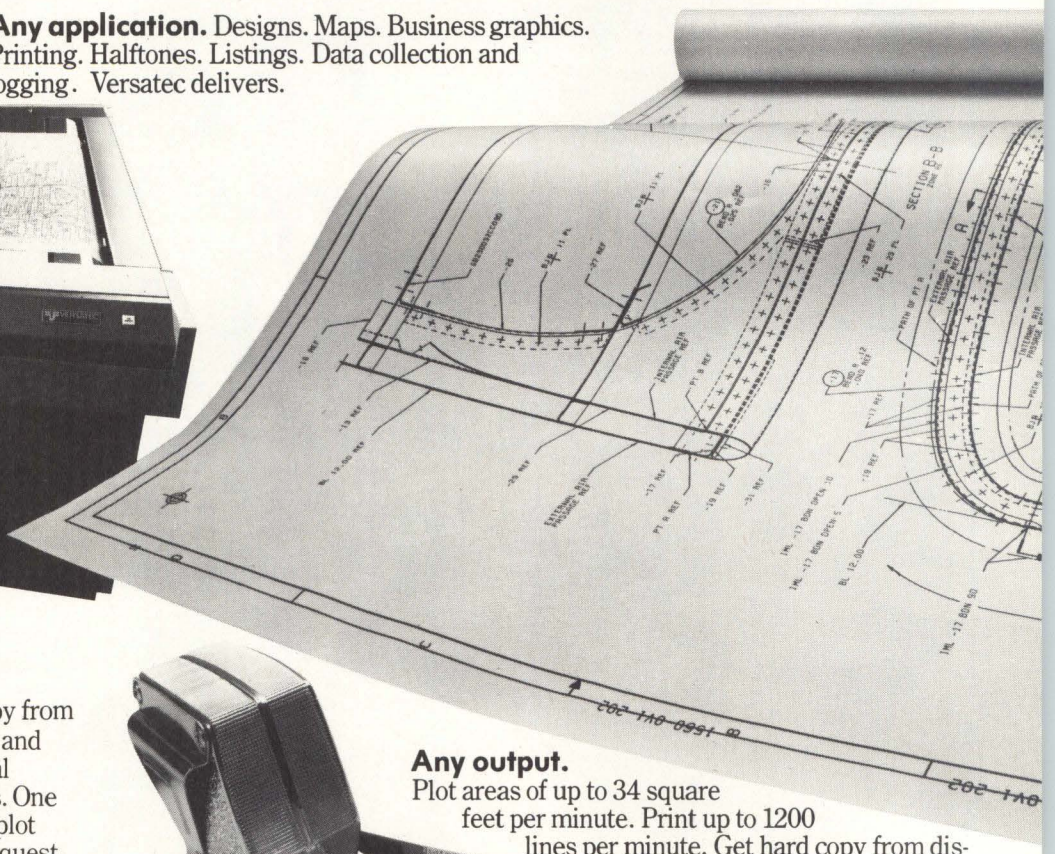

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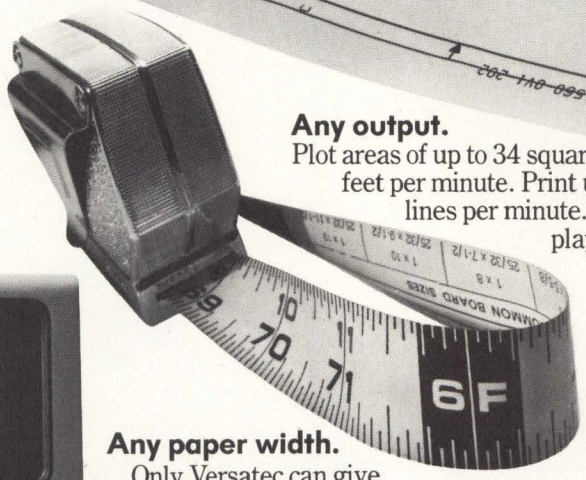

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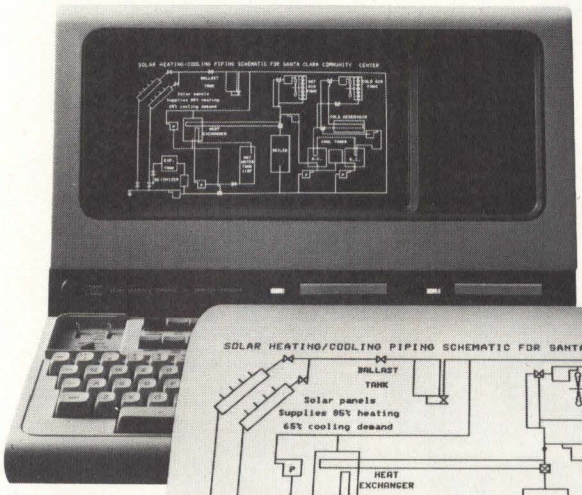

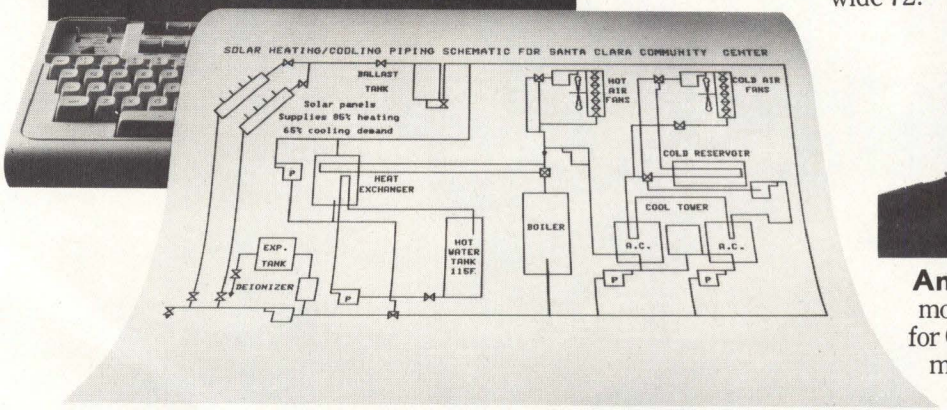

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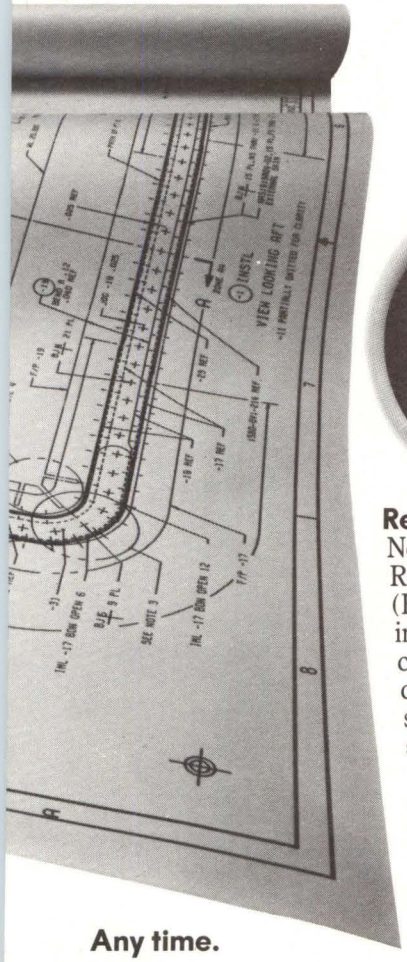

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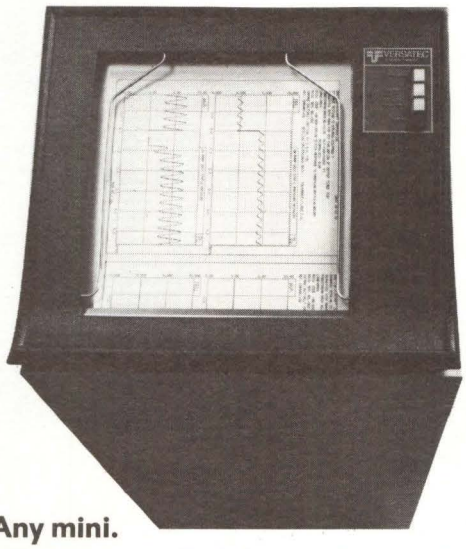

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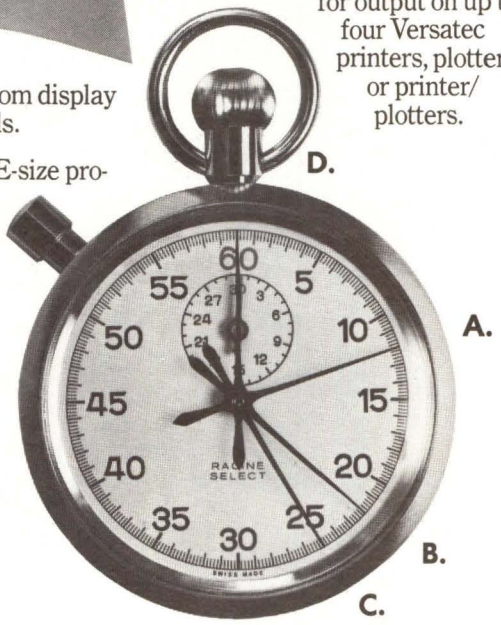

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CIRCLE 55 ON INQUIRY CARD

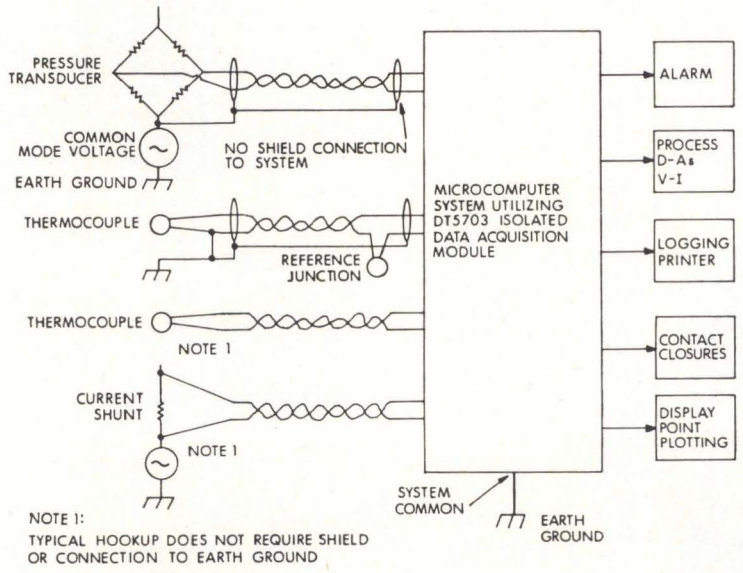
Editor's Note: This issue of *Computer Design* marks the advent of a new format for the Micro Data Stack department. To impart to our readers the significance of the technology and applications involved in the microcomputer/microprocessor field, the Data Stack has been subdivided into two sections: Processors and Elements, and Computers and Systems. This will allow greater flexibility in our coverage of the material to better serve the readers' needs.

We welcome feedback consisting of criticisms, suggestions on material to be covered in this department, and submissions of featurettes or contributions for consideration.

The Computers and Systems section will emphasize the design and applications of microcomputers—the processor, I/O, and memory—as well as peripheral equipment for the computer, complete systems, and application software. Also to be covered here is the area of "personal computing," which in our sense of the term implies use of microcomputer systems by individuals—computer professionals—whether in a business or home environment.

Isolated Data Acquisition Module Allows Microcomputer To Measure Low Level Signals Despite High Voltages

Users may now operate low cost microcomputer data acquisition systems in noisy industrial environments without having auxiliary equipment damage the measurement system. The significant feature of the isolated low level, wide range DT5703 data acquisition module is its high common mode input voltage capability, allowing it to acquire and digitize full-scale signal levels from 10 mV to 10 V while rejecting high common mode voltages up to 250 V. Safety of measurement integrity is obtained, despite hostile electrical environments.



DT5703 data acquisition module allows complete measurement isolation in presence of high voltages up to 250 V in various applications. Module allows industrial users to measure small low level process control signals from transducers and digitize these signals for use in microcomputer systems. Single twisted pairs can be utilized in most environments

Primarily aimed at industrial users who measure small process control signals from transducers such as thermocouples, pressure sensors, and strain gauges, the module allows these signals to be connected directly to the input. TTL logic and output TTL 3-state buffers are used for direct connection to a microcomputer bus. A low power version DT57C03 uses CMOS logic and CMOS 3-state buffers in order to connect to a CMOS microcomputer bus.

Compatability with the DATAX II data acquisition module series of Data Translation, Inc, 4 Strathmore Rd, Natick, MA 01760 provides the immediate availability of microcomputer interface boards incorporating the 5703 module. Analog I/O systems for Digital Equipment's LSI-11 and -11/2, Intel's SBC-80 series, Computer Automation's LSI series, and Zilog's Z80 MCB series comprise this interface group.

Some of the same functional elements contained in other models in the DATAX II series are a 4-channel input multiplexer, a high performance amplifier, a 12-bit integrating A-D converter, and all control and programming logic. The biggest alteration is the use of flying capacitor reed relays in a 4-channel differential multiplexer configuration. The reeds allow the multiplexer to withstand the ±250-V common mode voltage on any of the 4-input channels, and at the same time allow the amplifier to discern small signals of 1 to 2 μV for digitizing by the integrating ADC.

According to the company, the module can reject spurious noise spikes in industrial systems, as well as high voltage spikes that are often not anticipated. The module is claimed as the first one to be able to simply reject them and digitize the small signal level.

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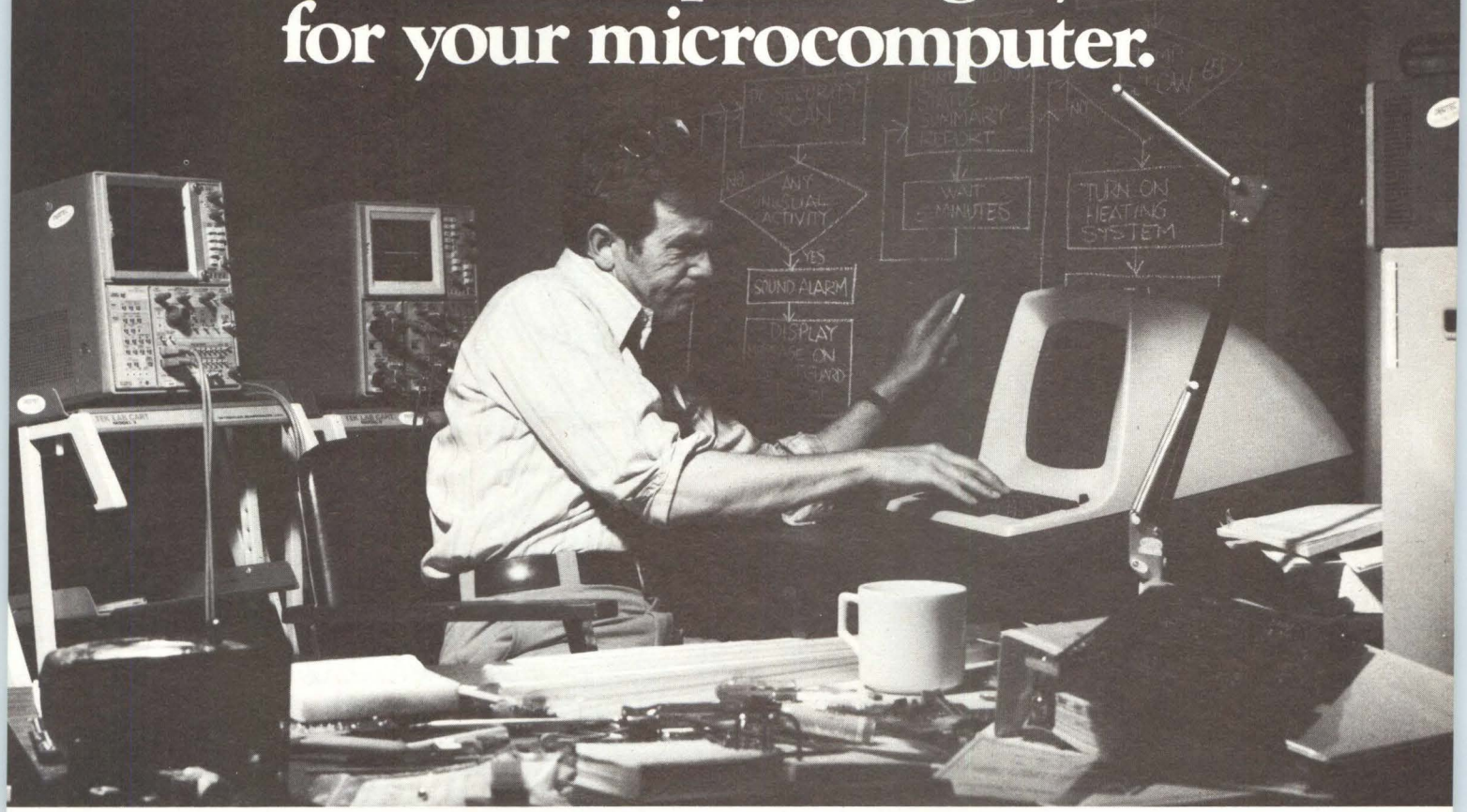

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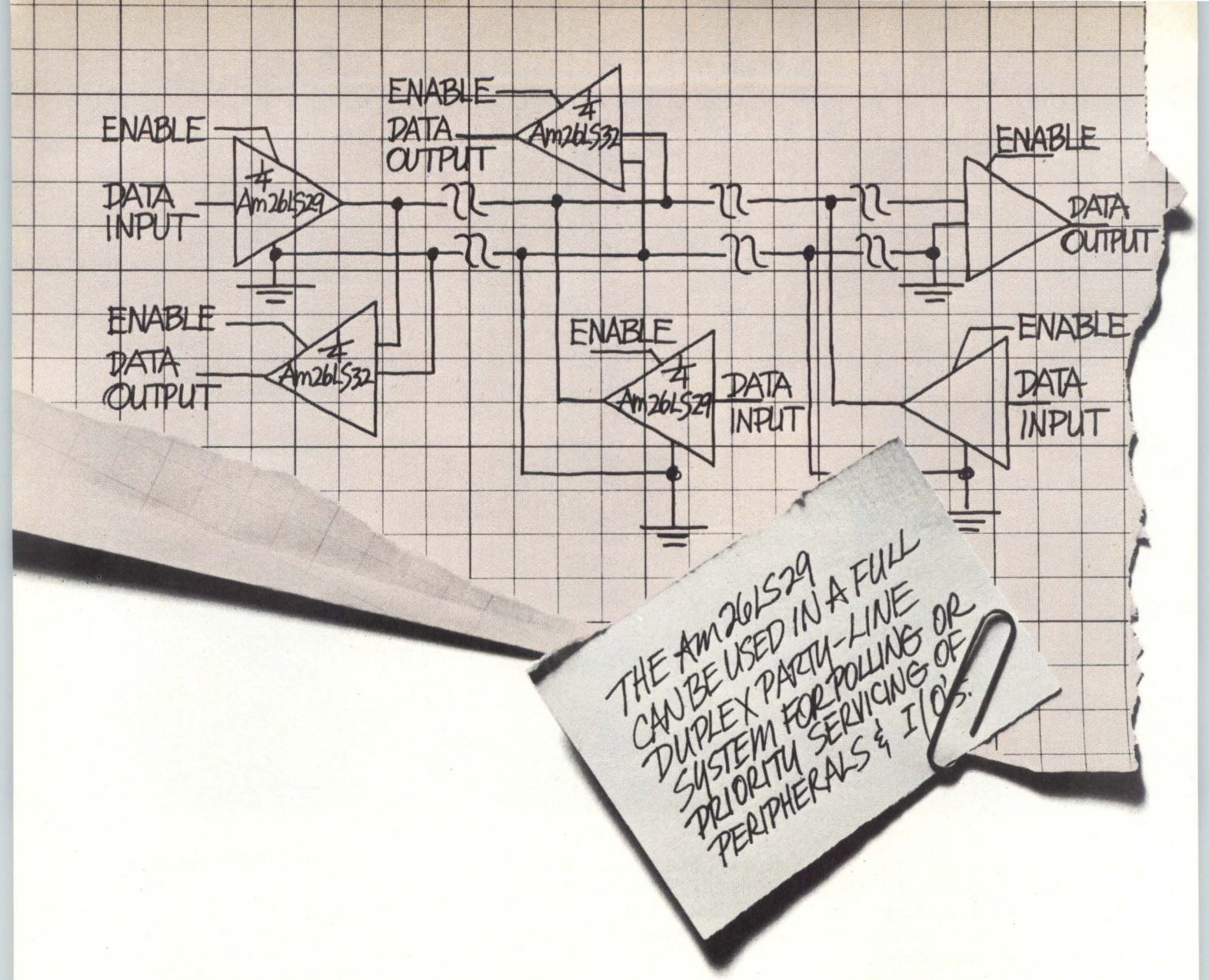

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It's a quad EIA-RS423 driver with three-state outputs, which makes it just right for bus-oriented systems.

Outputs don't clamp the line with power off or in high-impedance state—over the entire transmission-line voltage-range of EIA-RS423.

MEET AM26LS30.

It features a dual mode-control input which provides a choice of operation either as four independent single-ended RS-423 line drivers or two differential EIA standard RS-422 line drivers.

(Like the Am26LS29, outputs from the Am26LS30 won't clamp your style.)

Both devices can drive 50-ohm lines and have individual rise-time controls on each output for system flexibility. Both are MIL-STD-883 for free.

(If you'll write us, we'll rush you the complete EIA RS-422/423 Family pocket guide.)

Next time you're looking for line drivers and receivers, go right to the top. Call Advanced Micro Devices.

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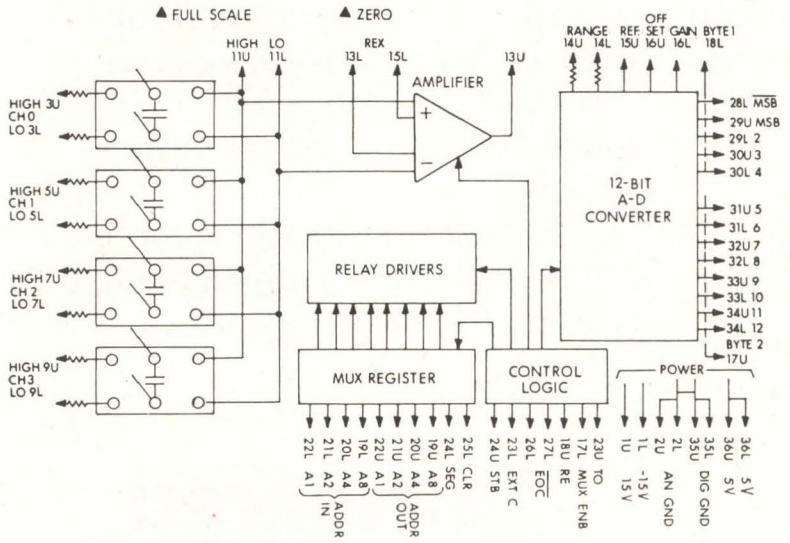
Multiple technologies. One product: excellence.
901 Thompson Place, Sunnyvale, California 94086
Telephone (408) 732-2400

CIRCLE 13 ON INQUIRY CARD



Flying capacitor reed relays are integral feature of Data Translation's data acquisition module, allowing multiplexer to withstand ±250-V common mode voltage while permitting amplifier to discern 1- to 2-μV signals. Relay outputs are brought out for expansion, so that large channel systems can be configured by using multiple expansion boards. With single resistor programmable gain amplifier, full scale can be set between 10 mV and 10 V. Direct connection to microcomputer buses is via digital outputs with 3-state control

mode, 40 conversions/s in sequential mode. The ADC within the module is operated at a multiple of the 60-Hz line frequency to further reject line noise pickup. For international applications, this A-D conversion can be obtained at a multiple of the 50-Hz line.

The unit is also able to anticipate system problems and shut down should these occur. If power goes off, the multiplexer goes to an open condition, preventing any load on signal transducers. Also if data are entered erroneously through power on and off cycles, the multiplexer again will go to an open condition.

Both versions use ±15 V at 45 mA; the DT57C03 uses only 150 mA of 5-V power, while the DT5703 uses 300 mA of 5-V power. Prices in unit quantity are $650 and $595, respectively.

Circle 430 on Inquiry Card

Microcomputer Systems Operate With Separate Memory and Interface

Two microcomputers have been introduced by Cromemco Inc, 280 Bernardo Ave, Mountain View, CA 94040, along with compatible boards and interfaces to allow professionals to perform general work in most fields. The System Two disc computer has the company's 4-MHz, Z80 CPU card; two 5″ (12.7-cm) floppy disc drives; a disc controller; 32k bytes of RAM (two 16k cards); a Z-2 chassis with 21-slot motherboard; and a 30-A power supply. Each drive has 92k bytes on each side of the diskette. The controller card can handle up to four disc drives, a disc bootstrap monitor in P/ROM, an RS-232 serial interface, and LSI disc controller circuitry.

System Three consists of the Z80 CPU card, a 32k-byte RAM (two 16k cards) expandable to 512k bytes, an RS-232 interface, a parallel printer interface, dual disc drive CRT terminal with line editing and block mode transfer capabilities, and line printer with 132 columns. Options include additional dual disc drive and memory. Disc protection is by software control to eject them, a key switch to disable disc eject buttons, and motor-driven disc loading and unloading.

Software support on IBM format soft-sectored diskettes for both systems includes a FORTRAN IV compiler, 16k Z80 BASIC, and Z80 Macro assembler and linking loader. System Two costs $3990; System Three mainframe is $5990.

Both the 32k BYTESAVER® card with onboard 2716 P/ROM programmer and the 8PI/O parallel interface card may be used with the S-100 bus and are compatible with the System Two and Three computers. With 32k-byte capacity of nonvolatile storage, the memory board holds up to 16 Intel 2716 P/ROMS or equivalents. Information can be stored by a one time write of the data into an erased P/ROM with the onboard programmer turned on. Switches protect and unprotect individual or group P/ROMS for programming, shadow ROM socket pairs, select card address, and control bank-select and DMA in/out features.

Located on any I/O boundary, the eight bidirectional 8-bit I/O ports can be used singly or coupled together for longer word lengths. I/O status flags for handshaking are grouped on one port. Strobed pulses can be issued after each 8-bit transfer or delayed until the proper word length has been formed. Additional features are eight sense switches, eight LEDS, two bits of optoisolated input, and two bits of relay-driven output. The two cost $195 in kit form, $295 assembled and tested.

Circle 431 on Inquiry Card

Multiplexer Board Offers High Density µComputer Channel Expansion

High channel capacity with no loss of sampling speed are common requirements of users of industrial processes, analytical data acquisition systems, and automatic test equipment. To fill these needs, Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021 has developed the ST-800 ADX 48S. This single-board 48-channel A-D multiplexer expander slides into the card guides of Intel's MDS-800 and SBC-80, and National Semiconductor's BLC-80 series. It is electrically compatible to the backplane pinouts and is

SUDDENLY THE FUNNEL LOADS 50% MORE. CUTS DISK-TO-CARTRIDGE STORAGE COSTS IN HALF.

With a new, increased capability to store up to 17.28 Megabytes on a single ¼" cartridge, The Funnel™ lowers your storage cost per kilobit to a single penny.

The Funnel is a 6400 BPI High Density Tape Drive featuring four-track, serial recording and boasts a transfer rate of 192 kilobits per second.

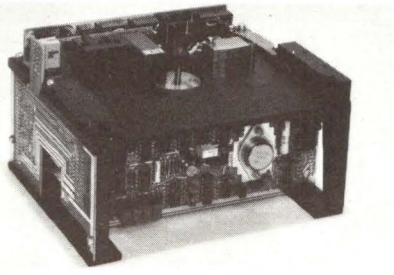
Funneling in more Megabytes.
By combining The Funnel with a 450 ft. cartridge you can load or unload an entire 12 M/Byte fixed disc. So The Funnel now out-stores and out-transfers a typical cartridge system 6 to 1. Or, you can still use smaller cartridges to store up to 11.5 M/Bytes.

Compare our performance.

	Typical Cassette	Double-Density Diskette	Typical ¼" Cartridge	The Funnel
Data Transfer Rate (K Bits/sec.)	24	500	48	192
Recording Density (Bits/inch)	800	6400	1600	6400
Unformatted Capacity (M Bytes)	0.7	0.8	2.87	17.28

For OEM price quotations and complete details, call (213) 351-8991. Or write: The Funnel, Data Electronics, Inc., 370 N. Halstead St., Pasadena, Ca. 91107, Telex 67-5327.

Add It To Your Mini System.



WE STORE BYTES IN M'S NOT IN K'S

CIRCLE 57 ON INQUIRY CARD

controlled by 8080 assembly language instructions.

The board acts as a slave to control from the company's master A-D converter board ST-800-32S. The master and slave board system digitizes analog inputs to 12-bit binary resolution with 0.025% accuracy. Together the two boards accept 80 single-ended A-D channels with input ranges of 5, 10, ±5, or ±10 V.

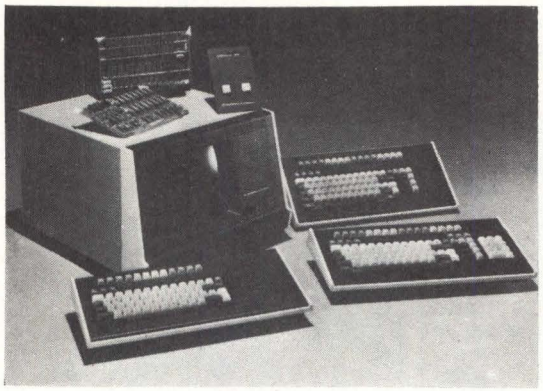
PC board pads are available for voltage-damping protection diodes and for users to install their own resistors for current loop inputs of 4 to 20, 1 to 5, or 10 to 50 mA. The CMOS LSI multiplexers with onboard channel addressing take only 1 μs to settle. A-D channel to channel throughput is 20 μs. Low channel to channel crosstalk (typ under 0.01% of 1 kHz) is insured by low input and coupling capacitance.

Performance options such as DMA operation offer a data transfer rate of 38k samples/s. Onboard addressing expands up to 256 A-D channels; D-A options are available. Ribbon cables carrying analog signals, channel addressing, and ±15-V power from the master board may be obtained from the company for the $449 board.
Circle 432 on Inquiry Card

Modular Intelligent Terminal Maximizes End-Use Flexibility

The level of componentry available to computer system manufacturers for the production of their products has been raised with the introduction of the EXOR 68. The multifunction programmable terminal system offers a choice of major building blocks with which to configure display oriented equipment. The matched macrocomponents are a basic display unit, a variety of keyboard options, and a group of microcomputer subassembly boards.

The philosophy of Motorola Microsystems, 3102 N 56th St, Phoenix, AZ 85018 is to allow the user to concentrate on software and firmware development, and then manufacture the final system with little or no hardware design using the modular units. This also allows the user to achieve performance and cost-effective upgrading of the end product.



EXOR 68 programmable terminal system from Motorola consists of basic display unit with CRT, keyboards with varying functions, and host of Micromodule computer boards to give the terminal intelligence; user can mix components to match specific end-use requirements

The basic unit is a CRT display that adds visual monitoring to a system. It consists of a video monitor capable of displaying up to 1920 characters in 24 lines on its 12" (30-cm) diagonal screen. Internal generators produce 128 characters, including 96 upper and lower case ASCII characters, 24 lower and 2 upper case Greek characters, and 6 special characters.

Built-in electronics permit operation with RS-232-C transmission and with 20/60-mA current loop equipment. Switches also permit the selection of word length, baud rate, communications mode, and modem control. Other features include blinking inverted cursor, audible alarm, and optional compatible motherboards for expansion with up to eight additional micromodules of EXORciser boards.

Operation is controlled by five executive firmware modules. The control board with MC6800 MPU permits such operations as multiple display modes, multiple data entry capability, and display of commands without execution. Built-in electronics are separate if keyboard entries are not required.

Six keyboard arrangements are offered as optional extras. TTY and control keys are standard on all, with various combinations of functional, editing, cursor control, page mode control, and auxiliary control keys, and numeric keypad. The keyboard can be connected to the display unit with optional-length cables to form a computer entry and display unit.

The addition of one or more micromodules adds any degree of intelligence the user may require. They range from partial computers (microprocessor, memory, and interface modules) to complete single-board microcomputers. The boards may be installed within the terminal card cage through an optional 8-card motherboard.
Circle 433 on Inquiry Card

Single-Chip μComputers Provide Faster Speed With 11-MHz Clock

Using the 8049 single-chip microcomputer to replace an 8048, designers can automatically double the program and data storage memory capacity without altering the design's hardware. Compatible with other MCS-48 family members, the 8049 and 8039 have an 11-MHz internal clock, which represents an 80% improvement in speed over the earlier 6-MHz 8049 version.

A performance advantage is obtained in control type applications, with over half the instructions executing in 1.4 μs and the others in 2.8 μs. Typical applications include high speed peripheral controllers and line adapters. The 8049 exceeds the onchip 1024-byte program memory and 64-byte read/write memory capacity of other family members. Designs requiring larger read/write memory with no onchip program memory are suited to the 8039.

The chips are fully programmable to perform I/O control and processing tasks at rates to 720k operations/s. Components are an 8-bit CPU with 96 instructions, 128-byte read/write memory, 3 programmable 8-bit I/O ports, 8 other control and timing lines, interval timer/event counter,

The PerSci generation of Diskette Mass Storage Systems Smarter, Faster, Smaller.

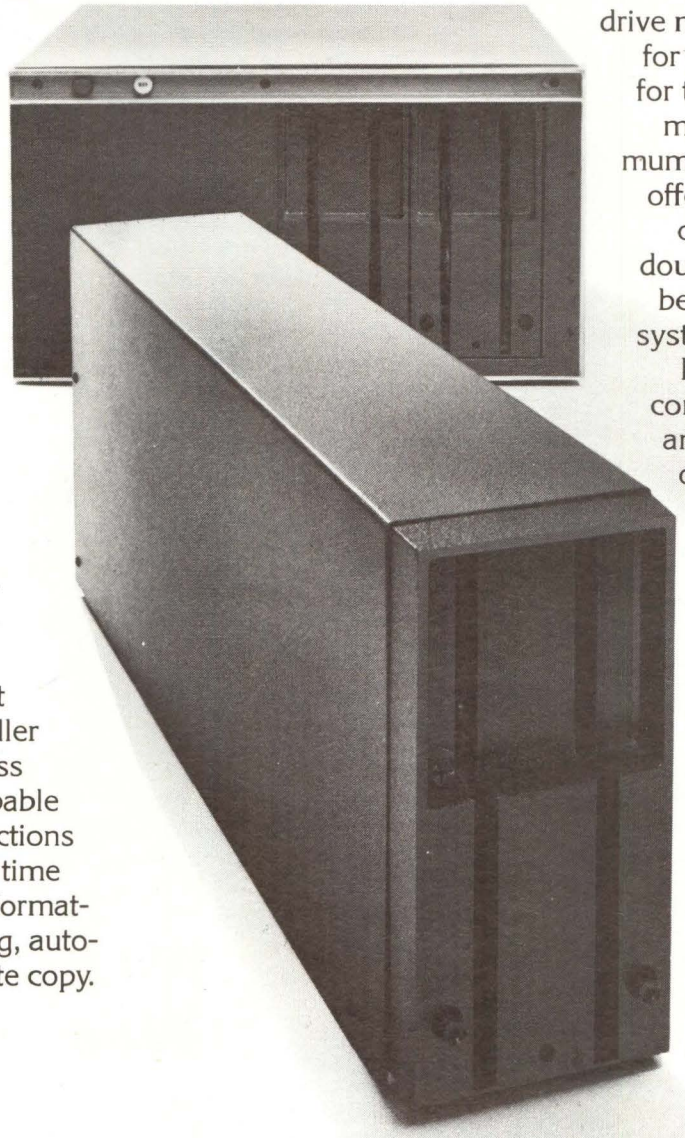
A new generation of advances in diskette drive technology comes together in PerSci Mass Storage Systems, the first diskette subsystems to provide large storage capacity, intelligence and high speed in as little as 4½" of space.

Two Times The Capacity...

New PerSci developments in large disk voice coil technology reduced to floppy disk applications make possible data densities as high as ½ Mbyte per diskette side—up to 2 Mbytes in a two drive system. When IBM data format compatibility is required, PerSci Systems will store ½ Mbyte per drive.

Microprocessor Intelligence...

PerSci's highly intelligent microprocessor based controllers, either single or double density versions, include the PerSci File Management Firmware. Under controller direction, the PerSci Mass Storage Systems are capable of performing many functions normally requiring CPU time and memory, including formatting, editing, reinitializing, automatic file and full diskette copy.



7 Times The Speed...

The unique voice coil positioning system of PerSci diskette drives allows PerSci systems to access data as much as 7 times faster than competitive systems. A random average seek is only 33 ms, as fast as many large disk systems.

In Half The Space.

PerSci Systems, one or two drive models, can be configured for mounting in a 19" rack or for table top operation. When maximum capacity in minimum space is called for, PerSci offers the "Slimline" system, only 4½" wide. A single or double density controller can be mounted in the standard system chassis or in the host. Interfaces to major microcomputers are available and an RS232 serial interface is optional.

Get all the most recent engineering advances in one smarter, faster, smaller system at competitive prices from PerSci, Inc., 12210 Nebraska Avenue, W. Los Angeles, Calif. 90025. (213) 820-3764.

PERSCI

Peripherals a Generation Ahead.

CIRCLE 58 ON INQUIRY CARD

priority interrupt controls, system clock generator, and a full set of system controls and utilities. The CPU can operate as a byte, 4-bit binary, or BCD arithmetic processor. Also, it can address onchip memory (expandable to 4k bytes), peripheral memory, or both.

To expand capability, the devices are software and pin compatible with a variety of I/O expander and MCS 80/85 system peripherals offered by Intel Corp's Microcomputer Components Div, 3065 Bowers Ave, Santa Clara, CA 95051. They are supported with enhancements of the Intellec® Microcomputer Development System. The chip operates off a single 5-V power supply. Samples of the 8049 are available; in large OEM quantity, it will sell for $10.
Circle 434 on Inquiry Card

Development Lab Emulator to Support Single-Chip µComputer

The Mostek 3870 1-chip microcomputer series is the first microcomputer to be supported by the 8002/8001 microprocessor development lab (*Computer Design*, Apr 1977, p 120). Tektronix, Inc, PO Box 500, Beaverton, OR 97077 has been working on engineering development on the basis of the microcomputer's technical merits and extensive logic replacement applications. The lab will also support the F8 microprocessor and the 3872 microcomputer, which has twice the 3870's onboard memory. The emulator will aid system designers, especially with program development, since no EPROM versions of the 3870 currently exist to support development efforts.
Circle 435 on Inquiry Card

Cartridge Disc Subsystem Adds 10M Bytes to microNOVA Family

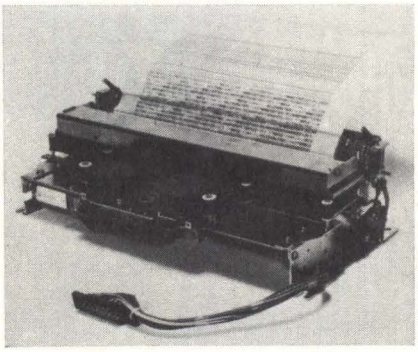
A 10M-byte cartridge disc subsystem for the microNOVA computer family model 6095 cartridge DG/Disc consists of an inhouse designed and manufactured cartridge subsystem that attaches to the microNOVA processor via its 16-line I/O bus. Each disc incorporates a 5M-byte fixed disc platter and a 5M-byte removable cartridge for integral system backup. A single spindle drives both discs and each disc surface has a corresponding read/write head. The data channel controller is physically part of the drive.

Systems using the disc have software support under the company's disc operating system (DOS), which provides a medium-scale program development or program environment on a small-scale system. It offers buffered and unbuffered I/O and device independent file transparency; comprehensive disc file management; high level language support; and extensive utilities. Most software developed for microNOVA diskette-based systems can readily be used on the disc systems. Similarly, disc formatting is compatible with NOVA® and ECLIPSE® computer systems for interchangeability, and those program development systems may also be used for the development of microNOVA software.

Data General, Rt 9, Westboro, MA 01581 has priced complete subsystems at $8900. Specs include 408 tracks/surface, 12 sectors/track, and 512 bytes/sector. Head positioning time is 38-ms average with a maximum of 8-ms track to track. Data are fully buffered by sectors and transfer at the rate of 312k bytes/s, I/O cabling is standard for the microNOVA, and the subsystem may be placed anywhere on the I/O bus, occupying only 10.5" (26.7 cm) of rack space.
Circle 436 on Inquiry Card

80-Col Dot Matrix Printer Mechanism Gives Increased Head Life

Featuring a 100M-char dot head, 80-column model 3110 dot matrix printer mechanism offers OEMs three times the present mechanism head life. Precise alignment and pin movement serve to lengthen the life of the ruby-jeweled supported head. Mechanism prints 80 columns at 150 char/s with a 5 x 7 dot matrix character and 1/10 column spacing.



The unit from Epson America, Inc, 23844 Hawthorne Blvd, Torrance, CA 90505, requires a 24-V/30- to 42-V/5-Vdc power supply provided by the OEM, plus case, control board, and interface electronics. Mechanism measures 95 mm high, 335 mm wide, and 185 mm deep; weight is 6.6 lbs (3 kg). Delivery of the device, which will sell for less than $250 in 500 quantities, is scheduled for September.
Circle 437 on Inquiry Card

Computer Can Be Equipped With Voice Data Input Unit

Complying with the Apple II computer smart peripheral conventions, the Speechlab model 20A allows speech input to be incorporated into users' present and future programs. It interfaces directly with user written BASIC programs and features a 32-word vocabulary, fast realtime response, and capability of multiple training samples for high accuracy. The program to run the unit is contained on an onboard P/ROM which is automatically enabled and executed by the computer's monitor program when speech input is desired.

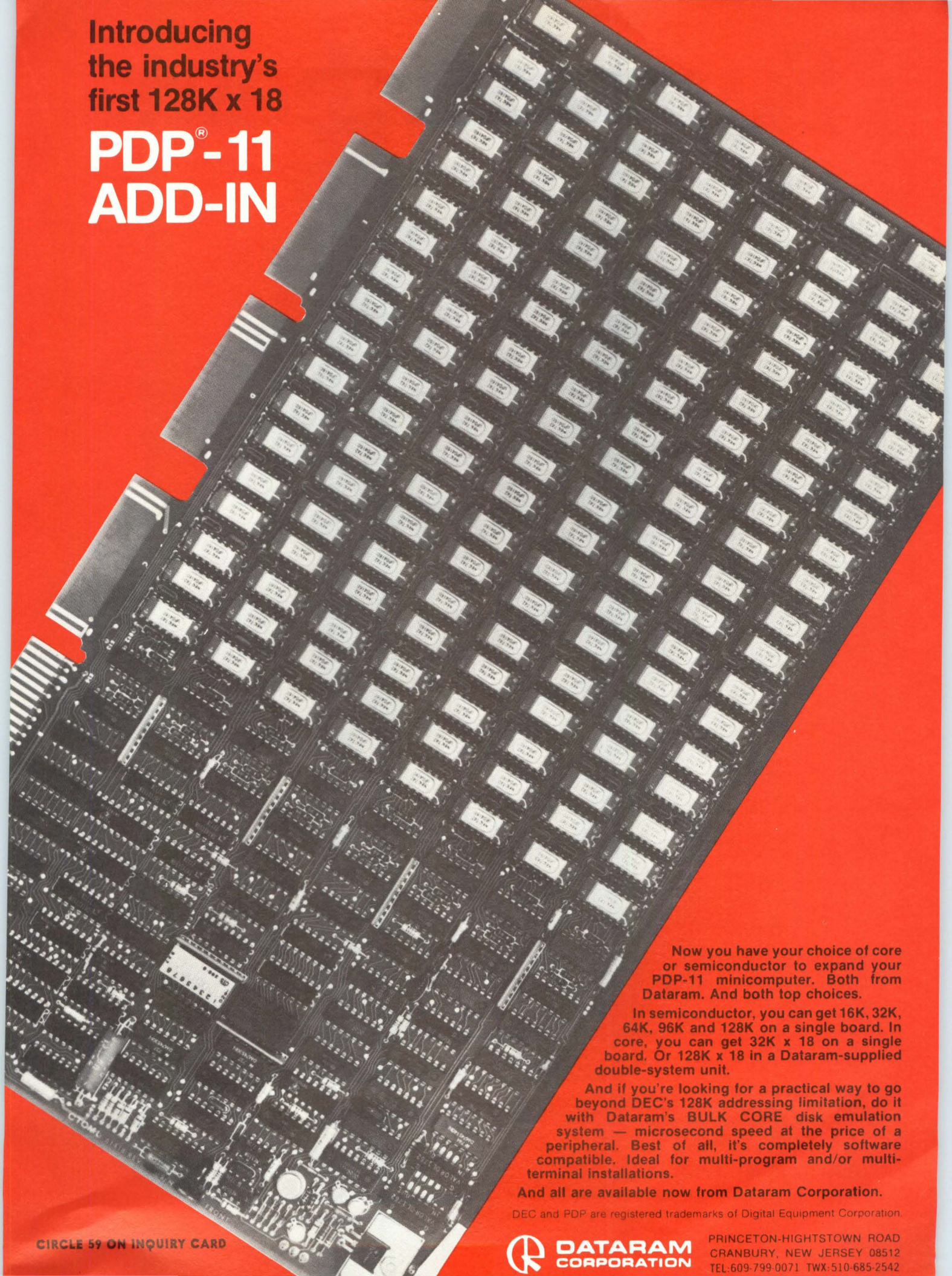
The voice data input system is available at computer stores or directly from the manufacturer, Heuristics, Inc, 900 N San Antonio Rd, Los Altos, CA 94022, for $189, assembled and tested. This includes a high fidelity microphone and user manual with six demonstration programs written in Apple BASIC illustrating the unit's use and capabilities.
Circle 438 on Inquiry Card

Multibus Compatible 32k P/ROM Board Holds 16 EPROMs

PROM-32, compatible with Intel's SBC 80/10 bus, accepts 16 2716 EPROMS or 2316 ROMS. All ICS are socketed. Manufactured by Electronic Solutions, Inc, 7969 Engineer Rd, San Diego, CA 92111, the board has a 475-ns max memory access time and uses 5 V. Jumper selectable base addresses fall on 16k boundaries. Any number of 2k memory address blocks may be deselected by jumper removal.
Circle 439 on Inquiry Card

Introducing the industry's first 128K x 18

PDP®-11 ADD-IN



Now you have your choice of core or semiconductor to expand your PDP-11 minicomputer. Both from Dataram. And both top choices.

In semiconductor, you can get 16K, 32K, 64K, 96K and 128K on a single board. In core, you can get 32K x 18 on a single board. Or 128K x 18 in a Dataram-supplied double-system unit.

And if you're looking for a practical way to go beyond DEC's 128K addressing limitation, do it with Dataram's BULK CORE disk emulation system — microsecond speed at the price of a peripheral. Best of all, it's completely software compatible. Ideal for multi-program and/or multi-terminal installations.

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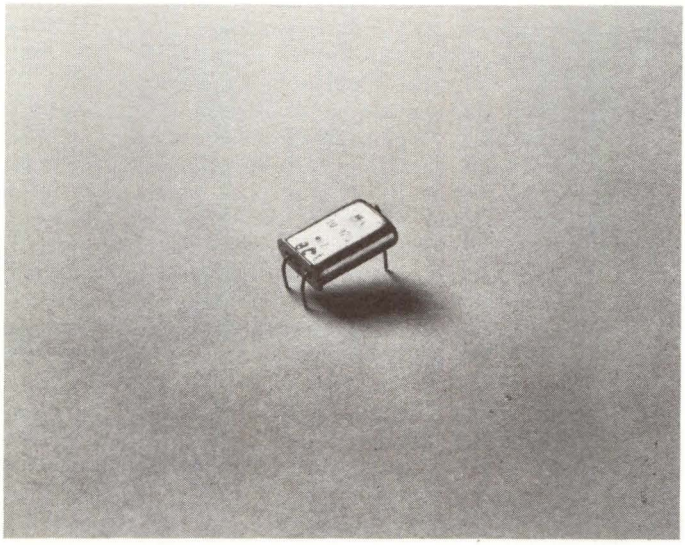
We've just introduced the least supported CRT controller ever—the National DP8350. Instead of the bagfull of support devices necessary with current MOS controllers, ours lets you off the hook with just one.

The reason is bipolar technology. It allows high frequency performance with high drive current outputs. So we can shift the functions of extraneous support chips onto the controller chip itself. Functions like dot counter/decode logic, crystal oscillator and high current Tri-State™ memory address bus drivers. The only support required is one crystal.

Since there are fewer components, you get benefits like lower systems cost. Less complexity. Greater reliability. And we made

Support, ours.



National's new DP 8350 CRT controller needs only one.

the DP 8350 mask programmable.

If you'd like to know more about the DP 8350, you're not alone. So we suggest you fill out the coupon today.

National's new DP 8350 CRT controller.

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Lower systems cost.

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National Semiconductor

MICRO DATA STACK
COMPUTERS AND SYSTEMS

Improved Performance Offered by Microcomputer Boards for OEMs

SD Series™ of microcomputer boards and peripherals utilize the Z80 microcomputer and industry-standard dynamic RAMs from Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006. Two versions of the Z80 based single-board microcomputer—the OEM-80/4 (4k RAM) and OEM-80/16 (16k RAM—feature four 8-bit I/O ports, serial ASCII interface (110 to 9600 baud), fully TTL buffered I/O lines, and four counter/timer channels. The series also includes two memory expansion boards: the RAM-80A which adds 16k bytes of RAM to the OEM-80; and the RAM-80B with 32 fully TTL buffered I/O lines and 16k bytes of onboard RAM, expandable to 32k, 48k, or 65k bytes of RAM using the XRAM-80 expansion kit.

The FLP-80 flexible diskette controller interfaces the OEM-80 to up to four single- or double-sided drives for large systems. With asynchronous or realtime operation, the controller accommodates database expansion to 2M bytes of storage. Card cages, extender and wirewrap cards, and a P/ROM programmer are available for prototyping and housing.

Circle 440 on Inquiry Card

System Is Marketed to OEMs As Large Equipment Computer or Controller

With applications including use as a general purpose computer or controller in medical diagnostic, scientific, analytical, and industrial control equipment, the C3-OEM microcomputer system runs software for the 6502, 6800, 8080, or Z80. Tabletop or rackmounted single-chassis construction includes dual 8" (20-cm) floppies for 500k bytes of online storage, 32k bytes of static RAM, one RS-232 port, and triple processor CPU board supporting the 6502A, 6800, and Z80.

The system, manufactured by Ohio Scientific, 1333 S Chillicothe Rd, Aurora, OH 44202, comes with 6502 disc based operating system, disc BASIC, and multiple processor switching software. Only four slots of an 8-slot motherboard are used in the base machine.

Additional memory, a 16-port serial I/O board, and 96-line parallel I/O board for process control applications are add-ons. Options include line printer interface and a 74M-byte Winchester disc drive.

Circle 441 on Inquiry Card

16-Bit μComputer Expands Amount of I/O Ports and Memory

Offering two serial I/O ports and increased memory expansion capability, the TM990/101M module provides an additional cost vs capability level between the TMS9900 component level and 990/4 microcomputer. The board contains up to 4k words x 16 bits of EPROM and 2k words x 16 bits of static RAM, along with two serial I/O ports. One port is intended for remote usage with a terminal or modem, the other for local usage with the company's 301 Microterminal, EIA terminal, or teletypewriter.

Three versions are manufactured by Texas Instruments Inc, PO Box 5012, Dallas, TX 75222. They differ in the type of local port I/O signals and in the amount of programming of the EPROM. Three programmable interval timers, up to 17 interrupts, and 16 lines of programmable parallel I/O are features of each version. The AMPL™ prototyping system supports the series. System modules ease design and cost of implementation, particularly with industrial or small business systems.

Circle 442 on Inquiry Card

Video Display Board Generates 1024 Char for S-100 Bus Computers

Requiring only 8 Vdc at 1.2 A, the FLASHWRITER™ generates a video display of 1024 characters (16 lines x 64 char) and uses a 7 x 9 dot matrix for a high resolution display image. It also has screen refresh memory, and an 8-bit parallel port with latched strobe that may be used as a keyboard port.

Alphanumeric displays, character by character, reversed video, reduced intensity, and block and line graphics may be generated. Vector Graphic Inc, 790 Hampshire Rd, Westlake Village, CA 91361 has manufactured the board to be compatible with most S-100 bus microcomputers operating with 4-MHz clock rates. Its video output conforms to RS-170 requirements and is available as composite video, or separate video and sync.

Circle 443 on Inquiry Card

C.P. CLARE'S LOW-COST SSR. 5 V IN GETS YOU 10-25 AMPS OUT.

Reed relay and triac.
C. P. Clare's hybrid relay snaps in at 4 VDC. Hook it directly to 5-volt DTL or TTL logic, no buffers needed. The triac switches 10 or 25 amps at either 120 or 240 VAC. It'll carry a 1.0 HP motor, 6.0 kW heater, or 2.5 kW lamp. No trouble. It'll take inrushes to 200 amps. So hang on power relays, contactors, solenoids, or whatever high-power equipment you're controlling —they'll quit before this relay. The 10 amp operates 20 million times; the 25 amp, 10 million times. C. P. Clare designed it that way.

Hockey Puck.
The package dimensions fit the industry standard "hockey puck" case: 2.25 x 1.75 x .87 inches. The rest is different. The square terminal bosses lock the wire clamp so the wire won't spin. (For those who want, quick-disconnect terminals can be had.) The slotted "U" self-seats on the mounting screw—two-hand installation is possible and easy. The plastic is something else—it resists fire, acids, and impacts. Inside, a closed-cell foam potting material reduces stress on the components and seals out the environment.

Black bottom line.
As far as we know, you can't get a heavy-duty, comparably-speced solid-state relay for less. For detailed pricing and application assistance, call a C. P. Clare representative or distributor. Let him lay all the facts on you. Hear how C. P. Clare's AC SSR can make your design better than the next guy's. That's our aim. Or call or write C. P. Clare & Company, 3101 W. Pratt Ave., Chicago, IL 60045. Phone: 312-262-7700.

We help you compete

C. P. CLARE & COMPANY
GENERAL INSTRUMENT CORPORATION

CIRCLE 61 ON INQUIRY CARD

Single-Unit Disc Based Computers Contain Full Operating Systems

A 9" (22.86-cm) video screen with 24 x 80 display, minifloppy disc drive with 143k bytes of storage, and an upper/lower case alphanumeric keyboard are built into the plastic enclosure of the VERSATILE 3B and the expanded VERSATILE 4. A numeric keypad is separate. Systems development and business applications are facilitated by the computers, which incorporate the 8085 CPU, 24k static RAM, and a serial I/O port with RS-232 connector. The 4 expands on this by providing 32k static RAM and 315k bytes of storage.

Computer Data Systems, 5460 Fairmont Dr, Wilmington, DE 19808 supplies the operating system with both units. Five diskettes comprise the software library; programs requested by purchasers are available on diskette for a copying charge only. The first diskette contains the disc operating system and 20k Extended BASIC; the second and third have games and a small business accounting package, respectively. The other two are blank so that users may enter their own programs.

Circle 444 on Inquiry Card

Z80 Software Operates on SuperPac Development System With Option

A Z80 option, added by Process Computer Systems, Inc, 750 N Maple Rd, Saline, MI 48176 to its SuperPac Development System, has produced the SPDS-Z, which supports both Z80 and 8080 based target systems. Software transparent to SPDS operators, the option allows target Z80 software to operate on the SPDS.

Similar to the SPDS Basic and SPDS, the only difference with the -Z is that the company's 1880 module replaces the 1806. It includes a Z80A CPU, 1k bytes of RAM, sockets for 3k/6k bytes of EPROM, five vectored priority interrupts, one nonmaskable interrupt, 3-function serial port, and system DMA capabilities. Its 300-W power supply permits up to 20 SuperPac 180 modules to be used.

The basic system, including interfaces, costs $7100. Also announced is a CPU independent software package with cross-reference generator, absolute and relocatable macro assembler, relocatable linking loader, source editor, floppy operating system, and up/down loader.

Circle 445 on Inquiry Card

System Computes Word Processing and Accounting Functions

Aimed at the first time computer user, the ABACUS 1 is a ready to use, standalone small business computing system that combines accounting functions with word processing at a price of $5995. Hardware consists of a Z80 microprocessor, dual Northstar disc system, video display, keyboard, and printer. Software programs are written in BASIC. Computer Products of America, division of the Computer Mart, 633 W Katella Ave, Orange, CA 92667 introduced the system.

Capabilities performed are general ledger accounting, accounts receivable and payable, inventory, payroll, mailing lists, data entry, sorting, and file management. A character oriented word processing system is optional. Software flexibility allows it to be tailored to specific needs of a business.

Circle 446 on Inquiry Card

Chassis, Power Supply, and Extender/Universal Cards for Multibus System

Four additions to the series 8000 designed for the 8001 Z80/Multibus single-board computer (see *Computer Design*, Jan 1978, p 144) feature Multibus compatibility for use with most other systems. The 8201 7-card slot chassis with Multibus PC backplane is std RETMA rackmountable or standalone. It features a popoff front cover for card access, switches and LEDs for NMI and reset, ±5- and ±12-Vdc connections, forced air cooling, and multichassis expansion capability.

The RETMA rackmountable 8202 power supply with front panel fuse and on/off switch provides ±5 and ±12 Vdc. It is regulated to ±1% of nominal output voltage, with short circuit, reverse voltage, and overvoltage protection. Five output voltages are supplied; power fail module is optional.

Full runs for the 86 Multibus pins as well as for the 60 auxiliary pins are provided by the 8203 extender card. The final addition by Monolithic Systems Corp, 14 Inverness Dr E, Englewood, co 80110 is the 8204 universal card, a Multibus compatible prototype design card for use with low cost wirewrap sockets. Interface buffers and bus master control logic are built in. The card contains all normal Multibus power and ground planes, and transfer acknowledge logic.

Circle 447 on Inquiry Card

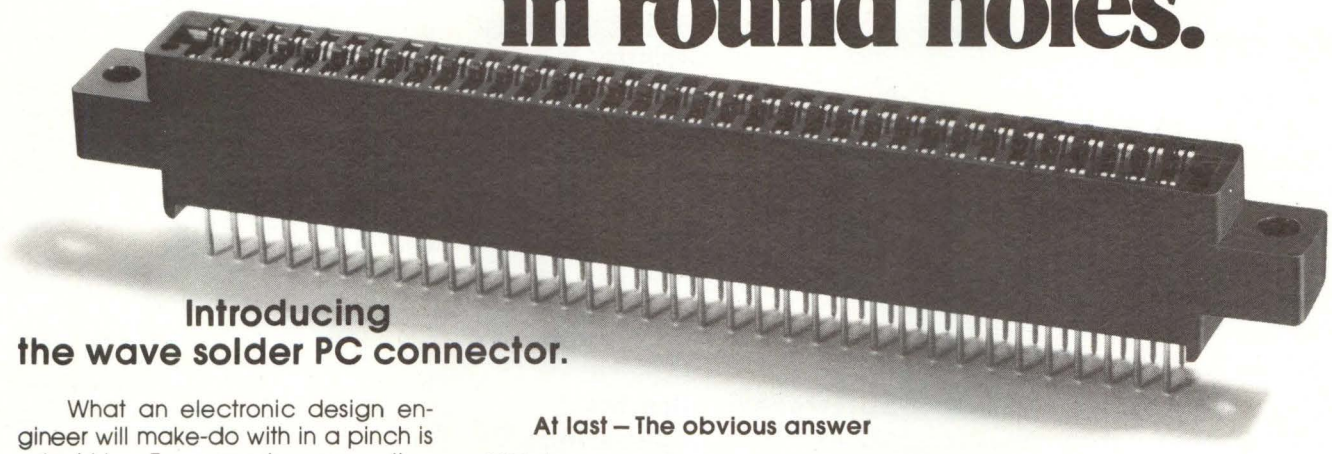
Single Cards Hold Complete µComputer and Development Systems

Minimum cost single-card systems can benefit from the real-world control system (RCS) modules, complete on single 100 x 160-mm eurocards. Built around the 8085 microprocessor, each module has analog and digital I/O interface circuits, 4k or 8k P/ROM and 256-byte RAM, optoisolated serial 20-mA I/O, and power regulation to run off a 24-V industrial supply. A programmable memory mapper allows interchangeable use of 2k or 4k P/ROMS on the same sockets. Other I/O configurations and scientific math functions are available.

Data Applications International SA, Drève des Renards 6, Bte 8, 1180 Brussels, Belgium has also introduced the 8085 based RCS-DM system contained on the same size card for microcomputer software development. It has a 1k, 2k, and 4k EPROM programmer; resident assembler, text editor, and utility programs; sockets for 8k or 16k P/ROM; 2.25k RAM; serial I/O with programmable baud rates; and power regulation for a 24-V supply. REAL-WORLD BASIC interpreter on P/ROM allows total system software to be written in BASIC, and executed directly from P/ROM.

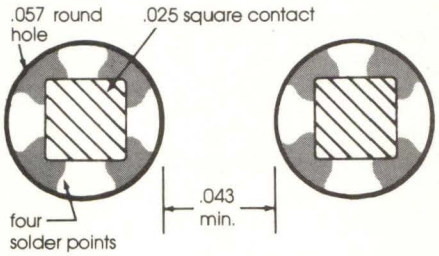
Circle 449 on Inquiry Card

No more square tails in round holes.



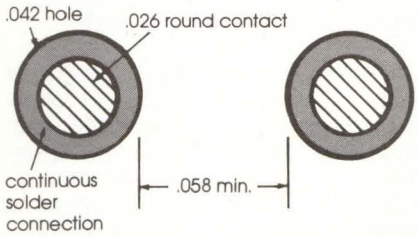
Introducing the wave solder PC connector.

What an electronic design engineer will make-do with in a pinch is astonishing. For example – converting wire wrap* PC connectors to wave solder.



How it's done: you saw off the square .025" tail and push it through a .057" round hole in the PC board. You get only 4 contact points for solder. And there's room for only one tracing between holes. But, so what...it works.

At last – The obvious answer



Our own design engineers, not afraid of doing the obvious and simple thing, have done just that. They've taken a series of our PC wire wrap connectors – and given them .026" round tails. Everything else stays the same: the insulator, semi-bellows contacts, pin and row spacing.

So what?

So – the .026" round pin slips into a .042" round hole in your PC board for an excellent solder connection. So – you can now get multiple tracings between rows.

We have two tail lengths: a .200" short one and a .250" longer one to take the AS400 Solderpak** System. These are available in connectors with contacts on .100", .125" and .156" centers, and in layouts from 6 to 50 positions.

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CIRCLE 62 ON INQUIRY CARD

SOFTWARE

Software for S-100 Interface to 488 Bus Is on Cassette Tape

The P+T−488 interface allows an S-100 computer to communicate with the IEEE 488-1975 Standard Digital Interface for Programmable Instrumentation, for talking, listening, or controlling. Hardware and software that is available for those computer systems can be used to configure custom instrumentation systems; in addition, the interface allows S-100 mainframes to use 488 bus compatible peripherals.

Software Package 1.0 is distributed by Pickles & Trout, PO Box 1206, Goleta, CA 93017 on a cassette tape that can be read with the built-in BITWIGGLER™ tape interface and a standard audio cassette player. The software, supplied as source code in Intel standard mnemonics, can be located in the region of memory most suitable to the particular system. It is operated as an interrupt driven or polled (serial and parallel) device, and implements 3-wire handshake.

Cable assemblies connect to the 488 bus and the cassette player. Unit is priced at $250 in kit form, $325 assembled and tested.

Circle 448 on Inquiry Card

Software Aids Language to Language Communication

Increased power for small computer software allows programs from one language to communicate with data from another. The disc operating system that makes this advance possible originated from Processor Technology Corp, 7100 Johnson Industrial Dr, Pleasanton, CA 94566. Extended BASIC, FORTRAN, FOCAL, and PILOT can communicate with each other using this standard data format.

PTDOS permits raw data created under its own text editor or assembler to be accessed by these high level languages, thus simplifying the programming of complex data manipulation applications. The disc operating system runs on the company's Sol Systems which include the Sol-20 terminal computer with built-in keyboard, and Helios II disc memory system.

Circle 450 on Inquiry Card

Software Facilitates μComputer Application Program Development

An assembly language development system, PDS runs on 8080/Z80 microcomputers using the Northstar minidisc or Micropolis MOD II disc drive. The package, which sells for $99, includes a unified assembler/editor, a macro assembler combining the features of a relocating linking loader, a string oriented text editor, and a trace debugger/disassembler. Each component is fully operational on computers with the 8080 CPU, yet the assembler and single-step trace debug/disassembler feature Z80 capability.

The assembler/editor and debug packages provide an interactive environment from which the system derives its power. Under trace execution, program modules can be modified, assembled, and checked in seconds. The assemblers favor the Intel instruction mnemonics treating the Z80 Superset as a logical and syntactical extension.

Source modules are also being offered by Allen Ashley, 395 Sierra Madre Ville, Pasadena, CA 91107 to facilitate application program development. These include floating point arithmetic and I/O, trigonometric functions, numerical and alphabetic sorting, matrix inversion, fast Fourier transform, and full function expression evaluator.

Circle 451 on Inquiry Card

Microcomputer Systems COBOL Meets ANSI Standards

Two packages—a complier for translating source code into relocatable object code, and a runtime system containing standard routines needed by the object code at execution time—comprise the COBOL-80 language for 8080/Z80/8085 systems. The whole system may be run in less than 32k bytes of memory under the CP/M and ISIS-II operating systems. Compilation rate is 250 lines/min.

Claimed by Microsoft, 300 San Mateo NE, Suite 819, Albuquerque, NM 87108 to be the first COBOL for those systems, the language conforms to the 1974 ANSI standard, giving users immediate access to existing COBOL programs. All Level 1 features as well as table handling, library, and interprogram communication facilities are included. The most useful Level 2 options for the nucleus and for sequential, relative, and indexed file handling facilities are incorporated, as are the verbs String, Unstring, Compute, Search, Perform, and Condition. A packed decimal data representation conserves memory on floppy discs.

Circle 452 on Inquiry Card

Word Processor Simplifies Document Preparation/Modification

Executing on the Micro-68b computer, TEXT word processor possesses 16k of RAM, one floppy disc unit, one CRT terminal, and a printer. It accepts lines of source text interspersed with lines of format control information. This is formatted into a printable, paginated document having a user designated style. Capabilities of the processor include left and right justification, automatic word hyphenation, page headings and footings, centering, footnotes, and bibliography references.

The text stream is free format: the typist, with the aid of the TEXT editor, types the document text in any convenient format, and the processor formats the output. Thus, document update is easily accomplished since the typed information remains on a magnetic diskette to be recalled or modified at any time. The processor, available from Electronic Product Associates, 1157 Vega St, San Diego, CA 92110, also allows the user to output only modified pages to reduce printing time. □

Circle 453 on Inquiry Card

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It took us a decade of growth to develop this new symbol. Its subtle intent is to symbolize the fact that Data Printer Corp has become a world leader in the computer line printer field. We not only manufacture the world's most popular make of OEM line printers – ChainTrain® – we've also built a brand new line of band-type printers, our Band Line 3000 Series. In fact, the demand on us has been so great, we've had to move to new, greatly-expanded headquarters in Malden, Massachusetts. It's just a cannonshot away from our previous production facilities. Now, we can serve you in meaningful OEM quantities.

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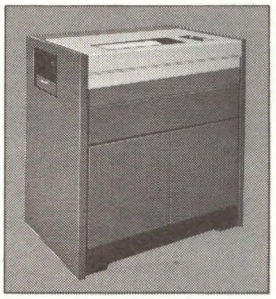

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CIRCLE 63 ON INQUIRY CARD

CUSTOM INTEGRATED CIRCUITS: A VIABLE ALTERNATIVE FOR LOW TO INTERMEDIATE VOLUME APPLICATIONS

Eric R. Garen

Integrated Computer Systems, Inc
Santa Monica, California

Despite numerous predictions that the use of custom integrated circuits would diminish as a result of the introduction of microprocessors and single-chip microcomputers, the demand for custom circuits is higher than ever before. Furthermore, interest in custom integrated circuits is not limited to extremely high volume (100,000 plus) production; it is also directed toward many applications where the required production quantity is as few as 1000.

While the most often cited reason for utilizing custom medium-scale integration (MSI) or large-scale integration (LSI) circuits is cost, other factors are involved. The custom development of an integrated circuit (IC) for special application purposes reduces circuit size and power requirements along with cost, as unneeded functions are jettisoned by the designer. In general, use of a custom IC provides a tradeoff among cost, size, and power requirements, and it is up to the planner to decide how much he wants to benefit in each of these areas. All of these factors are likely to be crucial, for instance, in a portable or handheld application with competitive cost constraints, such as in the development of watch or calculator chips.

Another related factor is that a custom IC can often deliver performance unattainable with standard circuits. A good example is the development of a custom IC for use in Winchester type disc drives. In this application, the read/write and select electronics are mounted at the tip of the data arm next to the read/write heads (Fig 1). This allows significantly improved performance in both moving head and fixed head disc drives; however, it would not be practical with standard discrete ICs. Instead, a custom IC was designed to provide the small size and performance that made the product possible.

Still another important reason to consider a custom IC is to prevent the theft of a circuit design. This can be important in highly competitive industries. For example, one manufacturer of arcade electronic games reported that (following the introduction of a new, highly successful game) his competitors were able to produce a replica, including an exact copy of the circuitry, and have it on the market less than two months after the introduction of the original game. The manufacturer has since turned

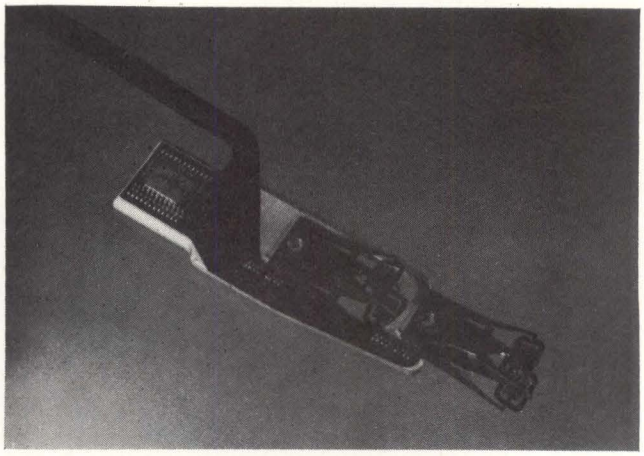

Fig 1 Winchester disc drive head assembly showing custom LSI circuit with read/write electronics mounted directly on tip of data arm together with read/write heads (Courtesy Silicon Systems Inc)

to custom LSI circuitry, which both cuts costs and protects design.

Despite these advantages, most engineers simply do not consider custom circuits because they believe the cost of development to be prohibitive for low volume applications. However, there are several approaches that enable the engineer to develop a custom IC for low and medium volume applications.

Solutions

One approach to the problem is to utilize a semicustom circuit. A semicustom chip contains a predefined array of linear and/or digital components (transistors or gates) and permits the designer to implement his circuit by specifying the metallization layer interconnecting these components (see *Computer Design*, Sept 1977, pp 148-154). This approach significantly reduces the design time that would be needed if a full custom circuit were to be developed. In fact, the layout of a semicustom chip is hardly more difficult than the layout of a printed circuit board. The disadvantage of this approach is that the chip will require more area than a full custom chip (and thus be more expensive) because unused components are present and because their arrangement has not been optimized.

A second approach to developing a custom IC is a "do-it-yourself" design. Often this involves considerable use of consultants and outside vendors. Starting with the basic circuit design, the engineer will usually subcontract the layout of the IC. A separate vendor will digitize this layout to produce a magnetic tape, which is given to a mask house for the production of the masks. Wafer fabrication is then performed by some semiconductor company, which will often do the prototype packaging as well. Testing also is typically done by an outside house. This whole approach is viable only if the engineer is extremely familiar with IC design. The fact that a circuit operates well utilizing discrete components does not assure that it will produce a good design when implemented on a single IC. Extensive knowledge of IC technology is crucial for the success of this method.

As a third approach, the designer can work in conjunction with a small semiconductor company with in-house processing capability. The obvious advantage of this approach is that a single vendor supplies all of the necessary steps. However, there are two drawbacks. The semiconductor company will certainly want to utilize one of its wafer fabrication processes for the part, even though the particular process may not be best in the particular application. Since small semiconductor houses often have only one or two processes available, this can be extremely limiting to the designer. In addition, small semiconductor companies will often want the right to sell the new chip as a standard product, thereby eliminating many of the advantages of the custom development.

A fourth approach for procuring a custom IC is to work with a "full-service" semiconductor house, such as Interdesign, Integrated Systems, or Silicon Systems. While some full-service houses have inhouse processing capability and are actually small semiconductor processors themselves, others function more as general contractors. They perform the design and layout of the IC and also test the completed devices, subcontracting the wafer fabrication and packaging to major semiconductor houses. This offers them a great range of flexibility in choosing the semiconductor process by which to implement the circuit.

These various custom IC vendors are perhaps best characterized by a production-cost to development-cost (or P/D) ratio. The large semiconductor companies such as Intel, Texas Instruments, and Motorola are primarily interested in doing custom work when the ratio of production dollars to development dollars is in the 75 to 150 realm. Thus, these larger companies will typically begin to show interest if a $30,000 design effort would result in $3,000,000 of production. It is true, then, that custom IC development with these companies would be interesting only in extremely high volume applications. In such cases, working with the large semiconductor companies is almost certain to be the most cost-effective approach.

Small and medium size semiconductor companies, such as Advanced Micro Devices, American Microsystems, Intersil, and Synertek, typically look for a P/D ratio of 20 to 50, and thus provide interesting alternatives for lower production volumes. Smaller, strictly custom houses typically operate on ratios of 5 or less, and it is largely for this reason that custom circuits are viable in small and medium production quantities. It should be noted, however, that these P/D ratios vary widely depending on the current load on a particular engineering department and the current production capacity. In "good times" the semiconductor companies look for jobs with ratios at the high end of the range, while in slow years they may settle for a lower ratio to attract additional business.

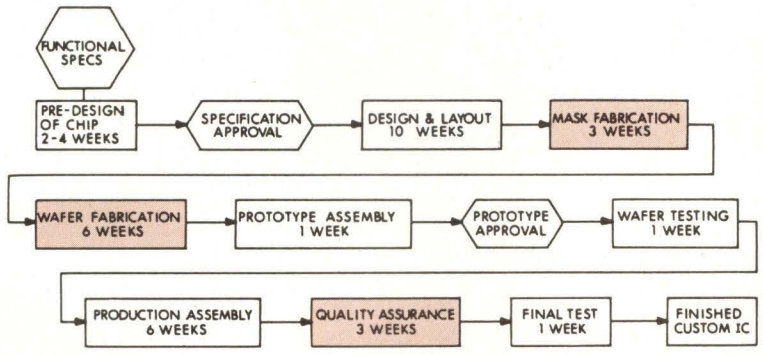

Fig 2 Typical development sequence for custom LSI circuits as performed by Silicon Systems, Inc. Shaded blocks represent subcontracted steps

Typical Example

The stages in developing a custom LSI circuit are perhaps best illustrated by a review of the typical procedure followed by a small custom IC full-service house, in this case Silicon Systems Inc. An engineer can approach one of these houses with a functional description of his chip, describing what that chip should accomplish. Along with this, he would provide a generalized system engineering analysis developing systems architecture, logic equations or algorithms, and the block diagrams necessary to describe the internal function of the chip. From these data either the engineer or the custom IC house can develop the detailed logic schematic and the appropriate device geometries. To assure the success of the IC, it is essential in this phase to perform an accurate circuit simulation that includes models of the actual semiconductor devices to be used. A simulation must be sophisticated enough to model such parameters as voltage dependent capacitances and second order dc effects. The result is an operative circuit design from which the layout starts.

In the layout phase, the chip designer must organize the devices in such a way as to minimize chip area. This phase makes heavy use of computer aided design techniques. Interactive graphics is often utilized and the designer can rely on the computer to assist him by establishing rule-checking criteria appropriate to the fabrication process and specific circuitry techniques to be used. Such rule-checking criteria include device spacing and minimum line widths.

The layout itself is then digitized. Specific locations of each line and component on the chip are read directly from the layout sheets into a computer. After a program checks the design rules, this information is stored on a magnetic tape for use by the mask-making equipment. The custom house then subcontracts the mask-making to specialized vendors. An important factor in maximizing yield and minimizing turnaround time is that the masks be identical in format to those ordinarily handled by the company doing the wafer fabrication.

Wafer fabrication is performed by one of several multisourced vendors, the choice of vendor depending on the process that has been selected. To be successful, a custom circuit must use processing identical to that used on a day-by-day basis for standard parts.

After wafer fabrication, several prototype parts are assembled and tested. Upon approval, all wafers are tested and production assembly can begin. The testing phases are of such paramount importance that Silicon Systems Inc insists on conducting its own tests. In fact, because many of its custom circuits have been combination linear/digital designs for which standard test fixtures are not available, the company has developed its own test bed.

As can be seen in Fig 2, the total development process for custom LSI circuits is typically less than 7 mo from the initial specification to part production. In some cases, working parts have been in the hands of customers in less than 22 weeks from the statement of functional specifications.

Summary

It is reasonable for an engineer to investigate utilizing a custom IC in volumes as low as 1000. Furthermore, it is certainly not necessary for the circuit to be LSI; many custom ICs are actually MSI circuits, replacing tens or hundreds of gates rather than thousands. An important point is that by selecting the technology to be used, whether CMOS, NMOS, or various bipolar circuit configurations, the designer can include both linear and digital circuits, can achieve extremely low power consumption, and can obtain high performance or other benefits that are unattainable with discrete standard components.

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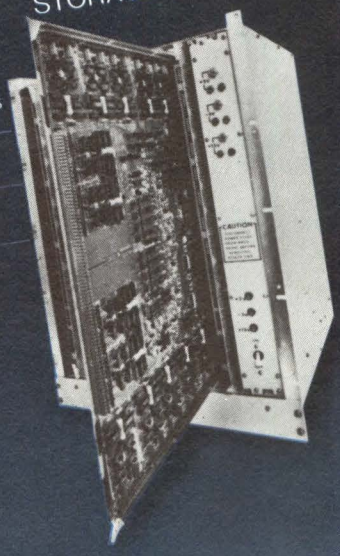

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CIRCLE 65 ON INQUIRY CARD

PDP-11 is a trademark of Digital Equipment Corporation.
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Programmable Constant Current Source IC Doubles As Current Mode Temperature Sensor

Designed to replace FET current sources as well as discrete circuitry, the LM134 will operate correctly on any voltage from 800 mV to 40 V. This device is programmable over a 10k to 1 range in operating current, from 1 μA to 10 mA, by means of a resistor between the trim terminal and the negative terminal. Current range can be extended by addition of a pnp transistor to the circuit. The drive capability of the external transistor is the only limit on the upper range of the combination. The manufacturer, National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, states that this is the industry's first programmable constant current source IC.

Current produced by the 3-terminal device is a linear function of absolute temperature. This linear dependence makes it usable as a current mode temperature transducer. In this usage, it is designed for remote temperature sensing applications now requiring as much as $10 to $25 worth of discrete and hybrid circuitry. Its particular value in remote sensing largely results because series resistance in long wire runs does not affect accuracy. Furthermore, only two wires are needed.

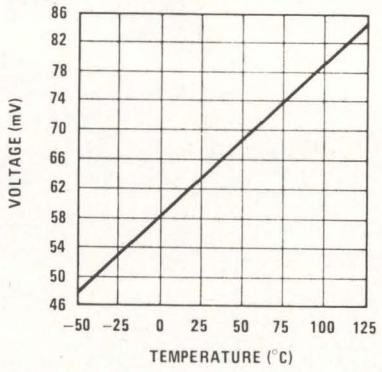
As a current source, diverse applications include oscillators, light metering, time delays, power supplies, impedance measuring, micropower biasing, and active filters. The device's programming feature is one of its chief advantages over discrete FET current sources. It is necessary to stock a wide range of FET current sources for the circuit designer to be assured that required current outputs will be available. With this single part, a user can now set any desired current output.

The device has the extremely high impedance necessary for a current source. For an operating current of 1 mA, the output impedance is 3 MΩ, while at 10 μA, output impedance is typically 1 GΩ. In addition, reverse applied voltages of up to 20 V will draw only a few microamperes of current, allowing the device to act as both a rectifier and a current source in ac applications.

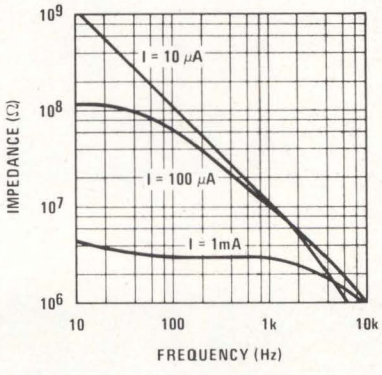
The series is divided into three principal members all having the properties discussed above. These are the LM134 itself, designed to military specifications and guaranteed over a temperature range of −55 to 125 °C; the LM-234, designed to intermediate specifications, and guaranteed from −25 to 100 °C; and the LM-334, designed to commercial specifications, and guaranteed from 0 to 70 °C. All models are true floating current sources with no separate power supply connections.

Key to the versatility and wide dynamic range of the series is the use of a mixed process technique in which two ultra low IDSS ion implanted junction FETs are fabricated on the same IC as bipolar transistors. The FETs, drawing only nanoamperes of current, are used to start chip operation at low voltages.

These devices are available in TO-46 hermetic packages with prices starting at $1.33 each in quantities of 100. In a TO-92 epoxy package, price ranges upward from 90 cents in quantities of 100.



Sense voltage used to establish operating current in National Semiconductor LM134 programmable constant current source. Voltage is linear function of absolute temperature. This property makes device usable, also, as current mode temperature transducer



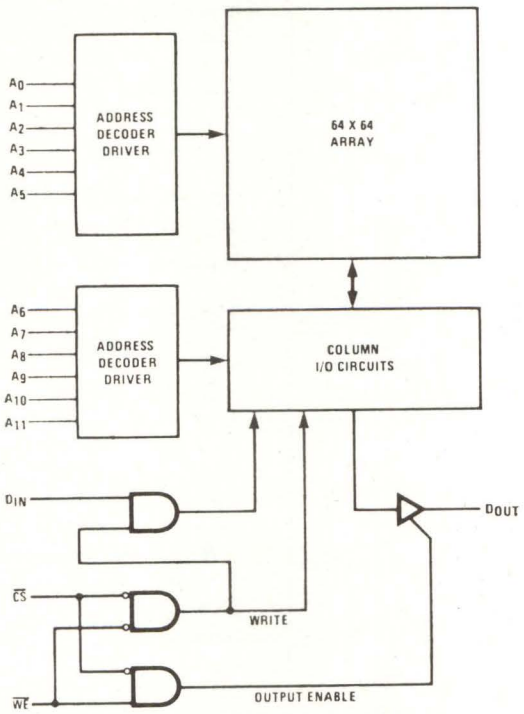
Output impedance of current source as function of frequency and current. Device is characterized by extremely high impedance over wide range of these parameters

VMOS Fabricated RAMs Are Designed for High Speed Applications

Fully static 4096-bit RAMs are TTL compatible on all I/Os. Fabricated by means of proprietary VMOS technology, these two devices feature low access times, single 5-V power supply, and 3-state outputs. Stored data are read out nondestructively and are of the same polarity as the original input data. These devices are produced by American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051.

The S2114 is intended for high speed microprocessor applications. It is a higher speed pin compatible replacement for the Intel 2114. The 1024 x 4-bit device is offered in versions with maximum access times ranging from 150 to 450 ns and supply currents as low as 50 mA, maximum. This 150-ns version is claimed to be the fastest 2114-type memory available.

Organized as 4096 x 1 bit, the S4017 is available in versions with access times of 55 and 70 ns. It has separate data I/O pins for maximum design flexibility. The fast chip select access time provides a high performance capability. As the chip se-



Block diagram of AMI S4017 high speed static VMOS RAM. Read occurs during overlap of low $\overline{CS}$ and high $\overline{WE}$, write during overlap of low $\overline{CS}$ and low $\overline{WE}$. $\overline{WE}$ must be high during all address transitions. If $\overline{CS}$ low transition occurs simultaneously with $\overline{WE}$ low transition, output buffers remain in high impedance state

lect is normally decoded from the address, the time required to decode the chip select will not impact the overall access time.

Absolute maximum ratings for the two devices include ambient temperature under bias from −10 to 80 °C, storage temperature from −65 to 150 °C, voltage on any pin with respect to ground from −0.5 to 7 V, and power dissipation of 1 W. Both RAMs are supplied in high density 18-pin plastic and ceramic packages, with operational temperatures in the 0 to 70 °C range.

Circle 350 on Inquiry Card

40-ns Bipolar P/ROMs Use Platinum-Silicide Fuse Technology

A series of bipolar P/ROMs provides maximum commercial range access times from 40 to 60 ns depending on the model selected. These devices feature a proprietary platinum-silicide fuse technology. All parts in the series are produced with a fusible link at each memory location storing a logic low and can be selectively programmed to a logic high through application of appropriate voltages to the circuit.

These devices all have low current pnp inputs and high current open-collector or 3-state outputs. Specific members of the series provide various properties: the Am27S18 and -19 are 256-bit memories with 40-ns (commercial) maximum access time; the corresponding figures for Am27S20/21 are 1024 bits and 45 ns, and for the Am27S12/13, 2048 bits and 50 ns. The Am27S15 is a 4096-bit device with onchip data latches and a 60-ns access time. The 4096-bit Am27S26/27 (addressed to clock setup time with 50-ns address setup and 20-ns clock to output times) feature onchip edge triggered registers, well suited to pipelined microprogrammed systems.

All members of the family use the same circuit design from the fuse to the output, so that all can be programmed with a single personality card set. Design techniques employ onchip voltage and temperature regulation to create extremely flat ac and dc performance over military requirements. In addition, selective feedback techniques have been incorporated in the design of the devices to minimize the propagation delay through critical paths in order to provide the fast access times. The devices are available in ceramic DIPs from Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086.

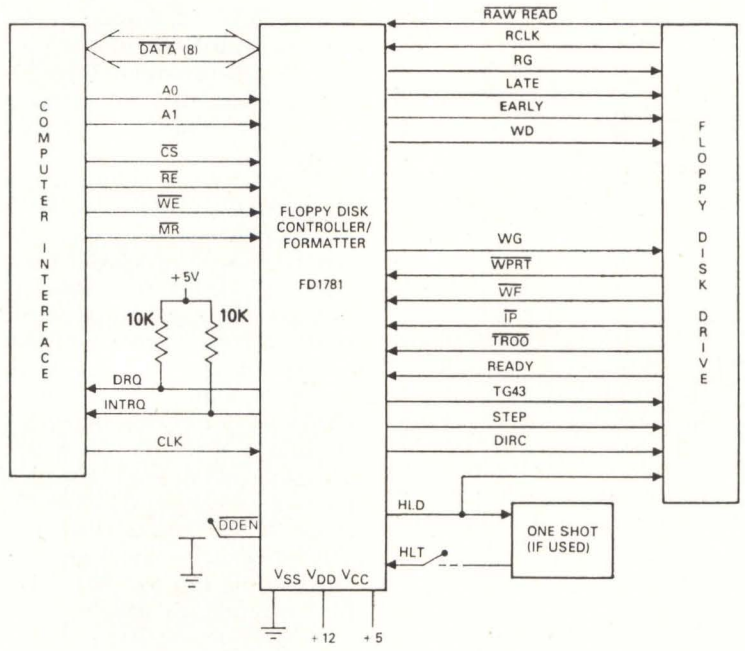
Circle 351 on Inquiry Card

Double-Density Diskette Formatter/Controller Is IBM Compatible

In a single-chip implementation, an MOS LSI device interfaces a processor to a flexible disc drive. This formatter/controller provides data accessing controls and bidirectional information transfer between the processor memory and the magnetically stored data on the diskette. Data are stored in a data entry format compatible with either a single- or double-density mode.

According to Western Digital Corp, 3128 Red Hill Ave, Box 2180, Newport Beach, CA 92663, the device is the first completely IBM compatible double-density floppy disc formatter/controller chip. It is the third in a family of related ICs by the same manufacturer. The first generation chip (FD 1771) was a single-density device; it was succeeded in Dec 1977 by the double-density FD 1781. The latest member of the series, FD 1791, provides for dual-density and dual-head applications with all IBM double-density logic contained within the chip and minimum external circuitry required. Fabricated in n-channel silicon gate MOS LSI technology, it is TTL compatible.

Family compatibility among the three devices is achieved by using the same computer interface, instruction



System block diagram of Western Digital formatter/controller. CLK input of 2 MHz is used for floppy disc interface with stepping rates of 3, 6, 10, and 20 μs. For mini-floppy interface, CLK input is 1 MHz and stepping times are doubled. DDEN = 1 selects single density, DDEN = 0 selects double density. Clock inputs are not altered upon transition between single and double density modes

set, I/O registers, and head load control, while changing only a few of the pin assignments for the 40-pin ceramic or plastic packages. Retaining the attributes of its other family members, the 1791 is able to read/write and format a double-density diskette using its added features of address mark detection, FM and MFM encode and decode logic, window extension, and write recompensation.

Circle 352 on Inquiry Card

Fast Data Acquisition System Components Provide Matched Pair

Used together, a hybrid video track/hold amplifier and an analog-to-digital converter can achieve word rates up to 450 kHz. These paired 12-bit devices, intended for data retrieval tasks in demanding military, aerospace, and industrial environments, are particularly suited for use with microprocessor control.

The ADH-050 video track and hold amplifier has a 120-ns acquisition time and aperture uncertainty of 500 ps. For maximum versatility the amplifier has a pin-programmable input buffer that can be bypassed, or connected in various ways, usable in a differential or single-ended mode or as a voltage follower. Linearity error of the 24-pin, double width, metal DIP is $\pm 0.0125\%$ and droop rate is 0.5 mV/μs.

Claimed to be the smallest 12-bit 2-μs ADC available, the ADH-8516 employs successive approximation to obtain $\pm 0.012\%$ linearity and a 1.8-μs conversion time. High speed conversion capability and 3-state outputs make this converter appropriate for both multiplexing and interfacing with a microprocessor. It is provided in a hermetically sealed 36-pin double width DIP.

Both modules are available from ILC Data Device Corp, Airport International Plaza, Bohemia, NY 11716. Each is processed to MIL-STD-883, Class C; screening to Class B is a standard option. The track/hold amplifier has an operating temperature range of -55 to 110 °C and the ADC is available with operating temperature ranges of either 0 to 70 or -25 to 85 °C.

Circle 353 on Inquiry Card

4k Schottky P/ROMs Have 35-ns Access Time, Dual Select Lines

Two 4096-bit P/ROMS are organized as 1024 words of 4 bits. The SN54S/74S476 commercial versions feature 35-ns typ access time, 30-ns max enable time, and 60-ns max access time. The SN54S/74S477 military versions have the same typical access time, 40-ns max enable time, and 75-ns max access time.

These devices, produced by Texas Instruments Inc, 13500 N Central Expressway, Dallas, TX 75222, also feature dual select lines to simplify memory expansion, a Ti-W fuse link of proven reliability, and fast, easy programming. Their memory organization and compact 18-pin packages make these Schottky P/ROMS particularly useful as fixed control store for relatively large, high density ROM applications such as computers (mini, midi, or mainframe), intelligent terminals, and high speed peripherals, as well as microprocessor based systems.

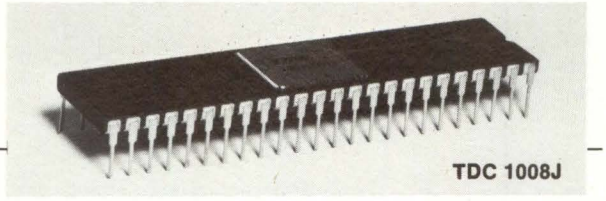
Circle 354 on Inquiry Card

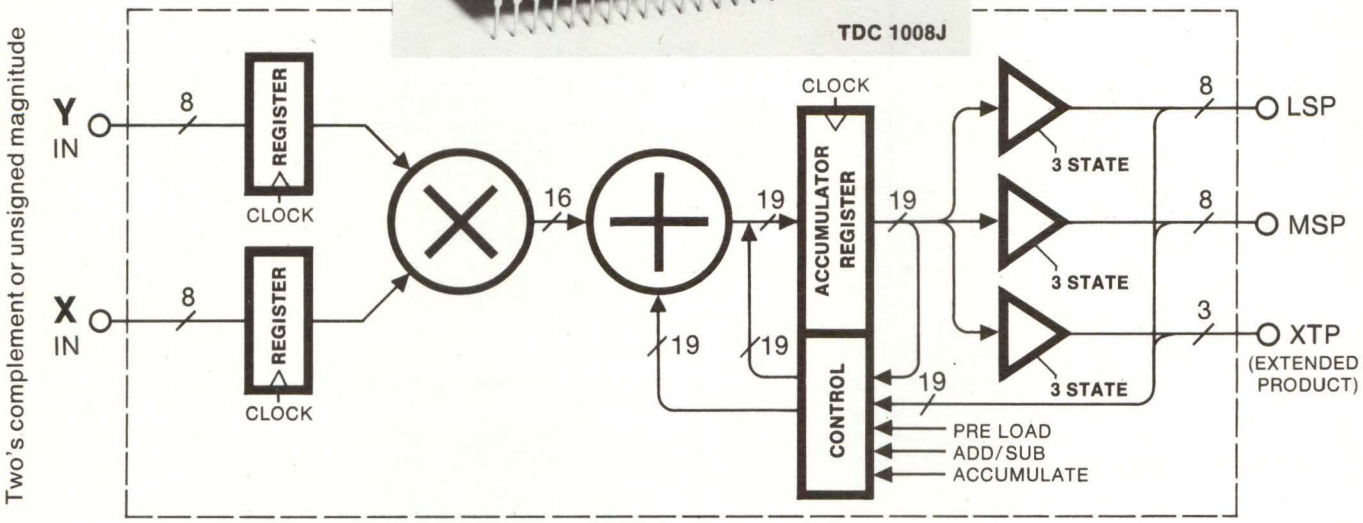
Programmable UART Interfaces with Wide Range of Devices

Independently programmable features of a recently introduced universal asynchronous receiver/transmitter IC include duplex mode, baud rate, data word length, parity mode, and number of stop bits. There may be 5, 6, 7, or 8 data bits; odd/even or no parity; and 1 or 2 stop bits (or 1.5 stop bits when a 5-bit code is used). These capabilities, obtainable through the use of external controls, enable the user to interface with a wide range of peripherals, modems, and remote data acquisition systems.

The COM6402 has high clock frequencies and low power requirements. Compatible with industry standard UARTS, it is a pin-for-pin replacement for the Harris HD-6402 and Intersil

Wow! Now you can multiply...or multiply and accumulate in 70 nsec





TDC 1008J

70 ns, 8 bits—$70 in 100's

- Controllable addition or subtraction in accumulator
- Round control
- Bipolar TTL monolithic technology
- Power dissipation of 1.2 watts
- Zero hold time
- Two's complement or unsigned magnitude
- Accumulator preloadable
- Cost effective as a 70 nsec multiplier
- Multiply-accumulate in 70 nsec
- Ideal for complex multiplying and filters (including FFTs)
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Let us show you how you can add functions, simplify the design...and reduce total circuit cost. Available from stock from Hamilton/Avnet or contact your local TRW Electronic Components field sales office or call us at (213) 535-1831, or send the coupon.

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COMPANY _____

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ADDRESS _____

CITY _____

STATE _____ ZIP _____

CD-7

TRW *LSI PRODUCTS*

...for Digital Signal Processing

CIRCLE 66 ON INQUIRY CARD

IM6402. CMOS LSI technology permits operator clock frequencies up to 3.2 MHz (200k baud) while requiring only 10 mW of power.

Requiring only a single ±5-V power supply, this TTL compatible device is available from Standard Microsystems Corp, 35 Marcus Blvd, Hauppauge, NY 11787. It is fully double buffered to eliminate dependence on external timing and provides start bit verification to decrease error rate. Three-state outputs are bus structure oriented. The hermetically sealed DIP assures easy board insertion. Baud rate clock can be generated by the company's COM8046.

Circle 355 on Inquiry Card

Multiplier/Divider In 14-Pin DIP Offers Low Cost 0.5% Accuracy

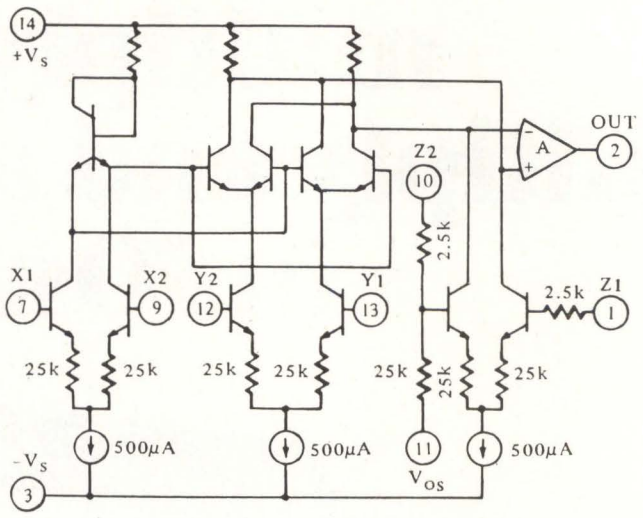
Multiplier/dividers designed for general purpose usage perform 4-quadrant multiplication, division, and square rooting of analog signals. The 4214 does not require use of additional amplifiers to perform these functions. It is laser-trimmed prior to final packaging and is guaranteed to its rated accuracy with no external components.

The device contains its own zener-regulated references and therefore is relatively unaffected by supply voltage variations. Output noise is only 120 μV rms in a 10-Hz to 10-kHz bandwidth.

The unit is available in two 14-pin DIP versions. A plastic ("P") package is offered for minimum cost over the −25 to 85 °C range. The hermetic metal package ("M" option) provides operation over the full −55 to 125 °C MIL temperature range.

Four versions are available to meet various requirements for accuracy, offset voltage, drift, and temperature range. The 4214AP provides better than 1% accuracy, less than 50-mV output offset, and less than 2-mV/°C drift. The RM provides the same performance but over the wider temperature range.

Higher performance models are the BP (in the narrower temperature range) and the RS (in the full range). These offer better than 0.5% accuracy, less than 25-mV output offset, and less than 0.7-mV/°C drift.



Simplified equivalent circuit for Burr-Brown multiplier/divider. Units have low output noise spec of 120 μV rms, 10 Hz to 10 kHz. Typical small signal bandwidth for ±3 dB flatness is 610 kHz; for ±1% flatness, it is 90 kHz. Small signal 1% vector error is 7.5 kHz

Burr-Brown, International Airport Industrial Pk, Tucson, AZ 85734, emphasizes the low cost of the devices. Prices in 100s are 4214AB, $14.00; BP, $22.50; RM, $18.75; and SM, $30.00. The manufacturer claims that the BP model has the lowest published price for a 0.5% accurate multiplier/divider in a 14-pin DIP.

Circle 356 on Inquiry Card

14-Bit CMOS DAC Is Low Cost, Precision Multiplying Type

A high performance series of digital-to-analog converters combine CMOS switches with laser-trimmed nichrome thin film resistors. These low power devices are designed for superior linearity and temperature drift characteristics. They also feature TTL compatibility and 500-ns output current settling time.

The recently announced 14-bit model, DAC-HA14B, is linear within ±1 LSB. Output is a ±1-mA current, designed to operate into virtual ground. This device, which can be operated as a 1-, 2-, or 4-quadrant multiplier, has a wide range of applications, including digitally controlled attenuators, D-A multipliers and dividers, automatic gain controls, signal correlators, and digitally controlled voltage sources. To produce true multiplying capability, the reference can vary from minus full scale through zero to plus full scale. The manufacturer points out that many DACs lack true multiplying capability, a result of having a reference that can be varied only over a limited range and that cannot reverse its polarity.

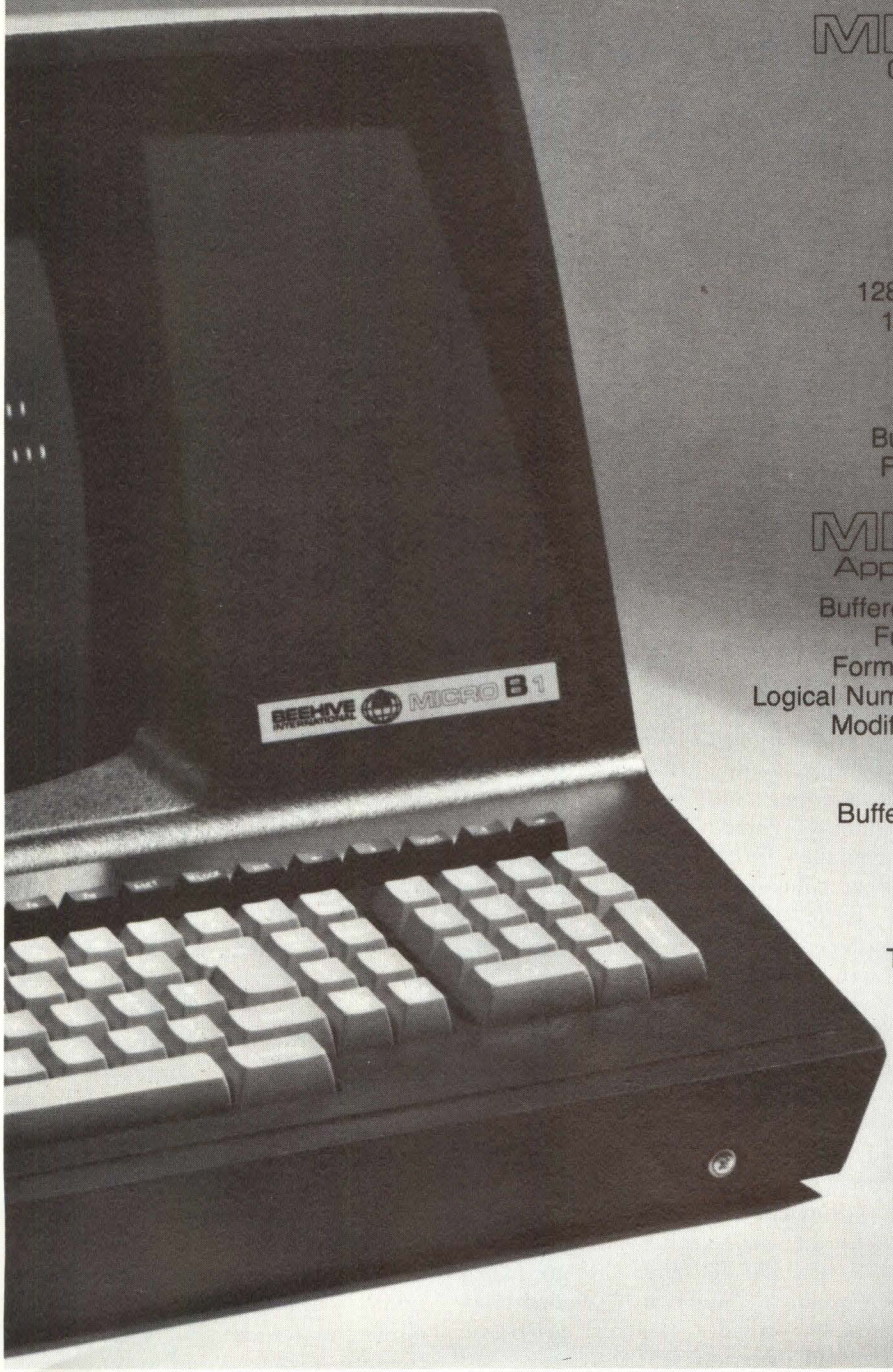
Produced by Datel Systems Inc, 1020 Turnpike St, Canton, MA 02021, the device comes in a hermetically sealed 24-pin ceramic DIP. There are three versions, with operating temperature ranges of 0 to 70, −25 to 85, and −55 to 125 °C. In addition, there are three models with identical performance except that the supply voltage requirement is 15 Vdc instead of 5 Vdc. Pricing in 1 to 24 quantity ranges from $69 to $139 as a function of operating temperature range. □

Circle 357 on Inquiry Card

WORTH WAITING FOR

Beehive International's new product line incorporates the latest state-of-the-art technology and provides the marketplace with heretofore unavailable functions and features

Take a look!



MICRO B 1
Conversational

Status Line
Self Diagnostics
Memory Lock
Read Status
Video Attributes
Line Drawing
128 ASCII Character Set
14 Key Numeric Pad
Split Screen
Time of Day Clock
OPTIONS
Buffered Auxiliary Port
Function Key Cluster

MICRO B 2
Applications Oriented

Buffered Transmission Modes
Full Editing Features
Formatting and Highlighting
Logical Numeric/Alphanumeric Attributes
Modified Data Transmission
Self Diagnostics
Memory Lock
Buffered Auxiliary I/O Port
Line Drawing
Status Line
Function Keys
Split Screen
Time of Day Clock

BEEHIVE INTERNATIONAL

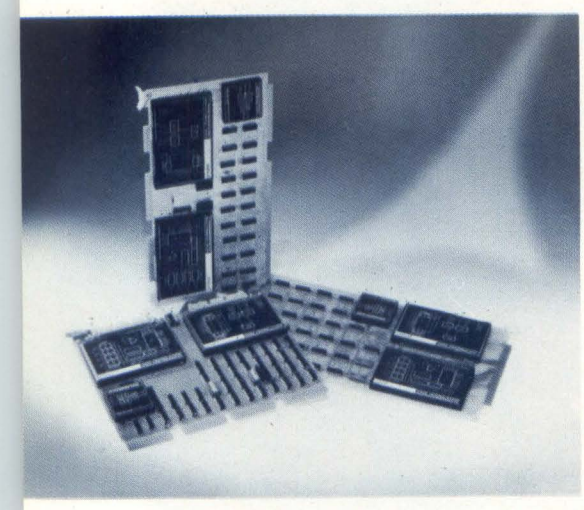
4910 Amelia Earhart Drive • Box 25668
Salt Lake City, Utah 84125
(801) 355-6000 • TWX 910-925-5271

EUROPE
Schipol Airport • Building 70 Schipol East
Amsterdam, The Netherlands
Phone 020-451522 • Telex 15284

CIRCLE 67 ON INQUIRY CARD

PRODUCT FEATURE

Microcomputer Compatible Analog Interface Systems Offer High Isolation



As many as 12 channels of analog signals can be measured and digitized for input to a microcomputer by a series of single-board systems. These microcomputer analog interface systems from Data Translation Inc process analog signals ranging from ±10 mV to ±10 V in the presence of common mode voltages up to ±250 V. They are directly hardware and software compatible with Digital Equipment Corp LSI-11 and -11/2, Intel SBC-80, National Semiconductor BLC-80, Zilog MCB (Z80), and Computer Automation LSI series microcomputers.

The systems (12 in all) are designed to withstand rugged industrial environments while performing multipoint, low level measurements under microcomputer control. Each is based upon a high isolation data acquisition module that uses a flying capacitor reed relay approach to alleviate problems usually associated with high common mode voltages, unknown ambiguities, and high voltage noise spikes that can damage semiconductor multiplexers.

Functional Description

Typical of these isolated wide range analog input systems is the LSI-11 compatible DT1768. Three LSI-11 versions are available: DT1768-4 with 4 differential input channels, DT-1768-12 with 12 differential input channels, and DT1769-4 with 4 differential input and 2 DAC output channels. Similar configurations are available for the other compatible microcomputer series.

Basic unit of each single board system is a 4-channel DT5703 isolated input module. (See Micro Data Stack/ Computers and Systems, pp 138, 142, this issue.) Expansion on the module to 12 channels is accomplished by adding an 8-channel DT03EX isolated expansion module. An expander card also can be added for further expansion to 64 channels. An optional programmable gain amplifier enables the user to select gains of 1, 10, 100, and 500 digitally. The interface, on a single quad LSI-11 compatible module, provides standard program I/O and interrupt functions.

Programming

All interfaces are designed to meet standard requirements and are structured around a control and status register for complete program control. Programming is straightforward and is accomplished by accessing that register.

There are a number of possible operating modes. Among these are program I/O, interrupt operation, random channel, sequential, and increment. Both device address and vector address are selectable via DIP switches.

In program I/O mode, standard microcomputer instructions can access and control the interface ADC. Start A-D conversion is accomplished by loading the multiplexer channel.

When it is preferable that the microcomputer not be dedicated to analog measurements, eg, in realtime applications, interrupt operation mode is used. In this situation, an interrupt is produced on the "A-D done" or "error" bits of the control and status register.

A conversion on a random channel can be started by loading a new multiplexer address. The "A-D start" bit will not start the converter in this mode.

In sequential mode, every start conversion will increment the multiplexer address automatically. The program can sample channels sequentially without the requirement of a software-maintained channel address counter. The multiplexer address is incremented before the conversion is initiated. Therefore, if the multiplexer address is read back upon completion of a conversion initiated under increment mode, the address bits will indicate the channel address from which the waiting data were obtained.

Increment mode can be used under all conversion triggering modes. Once the "inc mode" bit is set to allow sequential mode and an initial channel address is specified, every new "A-D start" command will increment the multiplexer channel address and perform a conversion on the new channel. When the multiplexer reaches the last channel installed on the board, the channel address is forced to zero and the cycle continues. This mode of operation eliminates the need for valuable CPU time to update a software channel

address counter and direct load a new address for every conversion.

One concern for the user application software is the need to know on what channel the given waiting A-D data were taken. To meet this need the control and status register always contains the address of the channel on which the current valid A-D data were taken. The multiplexer address is not incremented until the next trigger command is received, at which time the logic will automatically wait a preset time for the analog frontend to settle before triggering the conversion. The need for a software channel address counter is completely eliminated by this feature.

Specifications

Input specifications include common mode rejection ratio of 126 dB at 60 Hz with 1k unbalance; impedances of 10 MΩ power-on, 100 MΩ power-off; channel to channel zero offset of ±10 μV; throughput rates of 20 conversions/s in random mode, 40 conversions/s in sequential mode; and differential voltage of 15 Vdc max or 100 V for 10 ms max.

Amplifier specifications include offset voltage adjustable to zero; offset voltage tempco of ±3 μV/°C; gain tempco of ±10 ppm/°C; gain of 1 to 1000; bias currents of 50 pA at 25 °C, 1.2 nA at 70 °C; and input noise of 5 μV rms at 15 kHz.

A-D converter specifications include resolution of 12 bits; linearity of ±½ LSB, quantizing error of ±½ LSB; ranges of 0 to 10 V unipolar, ±10 V bipolar; and tempcos of ±20 μV/°C at zero, ±30 ppm/°C full scale.

Price and Delivery

Typical prices (in 1 to 9 quantities) for LSI-11 and -11/2 compatible analog interface systems are $795 for the 4-input channel device, $1055 for the 12-input device, and $1095 for the 4-input/2-output device. Comparable SBC-80, BLC-80, and MCB (Z80) devices are priced at $795, $1195, and $1095. LSI series devices are $1495, $2095, and $1695. OEM discounts are available. Delivery is quoted as 3 weeks ARO. Data Translation Inc, 4 Strathmore Rd. Natick, MA 01760. Tel: 617/655-5300.

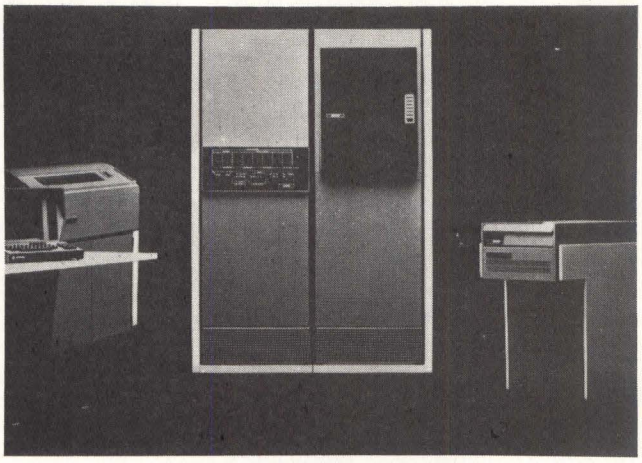
For additional information circle 199 on inquiry card.

PRODUCTS

Entry Level Computer System Offers Mainframe Power and Versatility

S123,' a completely functional entry level system, includes virtual memory CPU with 144k bytes of MOS memory and 768k bytes of virtual address space; operator's console; 40M-byte storage module disc drive; 9-track, 800-bit/in (314/cm) tape drive; 300-line/min printer; and a DMA communications processor with either 4 asynchronous or 1 synchronous port. System can accommodate up to 384k bytes of main memory plus a complementary I/O capability to support up to 8 interactive users. System features include concurrent timesharing, multibatch, remote job entry, and real-time processing. The VULCAN operating system supports 7 languages including FORTRAN IV, BASIC, ANSI COBOL, Macro Assembler, SNOBOL 4, FORGO, and FORTRAN. **Harris Corp, Computer Systems Div,** 1200 Gateway Dr, Ft Lauderdale, FL 33309.

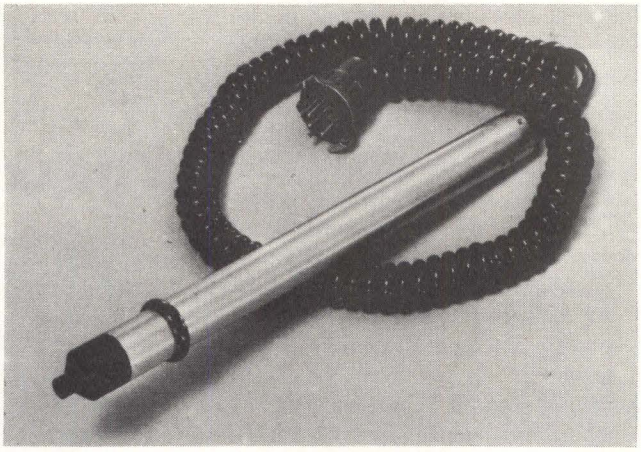
Circle 200 on Inquiry Card



Single Voltage Lightpens Incorporate All Electronics in Body

LP-220 series lightpens are each housed in a chrome finished metal body and include retractable cord and connector. The devices offer luminous sensitivity of 2 ft-L (avg brightness with P-31 phosphor, 20-mil spot, 60-Hz refresh rate); response time is <300 ns. Spectral response is 4200 to 11,000 A. Min vector speed is 20 cm/s. Power requirement is 5 Vdc ±5% at 60 mA max. Operating temp range is 0 to 55 °C. Model LP-220 features the patented Touch Sense™ (the operator touches the forward position of the pen with his index finger to form a high impedance bridge) actuation method. LP-221 has a pushtip switch and -222 has both Touch Sense and pushtip switches. **Information Control Corp,** 9610 Bellanca Ave, Los Angeles, CA 90045.

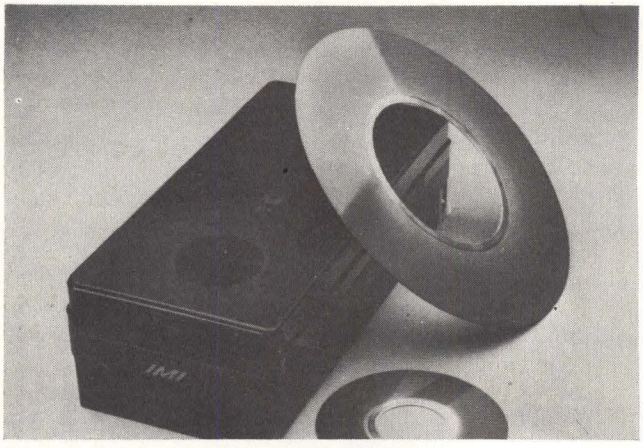
Circle 201 on Inquiry Card



200-mm Winchester Disc Drive Fits Into Floppy Drive Mounting Aperture

Packaged in a 5 x 8.5" (12.7 x 21.59-cm) unit offering twice the capacity at approximately one-half the cost of conventional disc drives, the -7710 mini-Winchester storage system is interchangeable with std sized floppy disc drive and offers 10k-hour MTBF. All components including subassemblies are mounted on a molded fiberglass-reinforced polyester base, characterized by light weight and high strength. Std Winchester-type read/write heads are positioned with a linear voice coil actuator using a closed loop, track following servo system. 200-mm oxide-coated discs provide the storage medium. 3 of the 4 surfaces store 11M bytes of data; the fourth is used for prerecorded servo information. Avg access time is 50 ms. **International Memories, Inc,** 10381 Bandley Dr, Cupertino, CA 95014.

Circle 202 on Inquiry Card

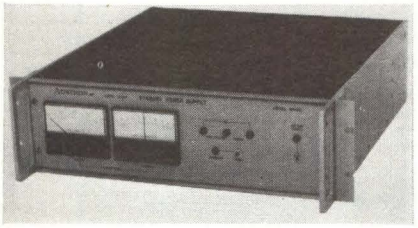


PRODUCTS

ADVANCED FEATURES FOR DIGITAL SWITCHING SYSTEMS

Detailed station message and accounting (DSMA) and least cost routing (LCR) are feature packages for D1201 and D1202 digital switching systems. DSMA provides incoming and outgoing call information for management control and departmental allocation of telephone costs. LCR allows for automatic selection of system's most inexpensive facility. Hardware for both consists of 4 plug-in units for mounting in PBX common equipment shelf and cabinet containing keyboard display unit, cartridge drive, formatter, and auxiliary power unit. **Digital Telephone Systems, Inc,** 1 Commerce Blvd, PO Box 1188, Novato, CA 94947.
Circle 203 on Inquiry Card

STANDBY POWER SUPPLY

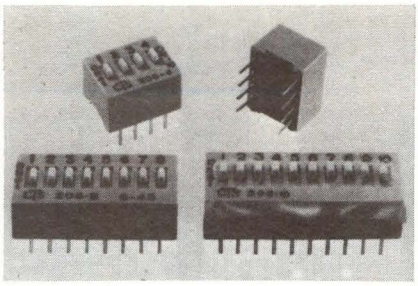


To maintain power during an extended ac power failure, the 1290A provides 24 Vdc at a max current of 3 A; total capacity is 19 Ah with fully charged, sealed cell type, internal batteries. An external 24- to 48-Vdc power source is also included. Electronic circuits provide automatic transient-free switchover from ac line to standby power, and back to ac. Additional features include ac interrupt, 10-A alarm relay contact, and front panel voltmeter and ammeter. **Austron, Inc,** 1915 Kramer Lane, Austin, TX 78758.
Circle 204 on Inquiry Card

RASTER SCAN DISPLAY SYSTEMS

Refresh memory organization and display technology (Opticolor™) are utilized in this image analysis/computer graphics system. Key component is the video digital interactive display processor (VDI) which features true operator/machine interaction, nondestructive image manipulation (such as display magnification and translation), and modular expandability. Available options include nondestructive cursor, RS-170 compatible video digitizer, pseudo 3-dimensional generation and display, overlay generation, and up to 1M-byte refresh memory. **Interpretation Systems Inc,** PO Box 1007, Lawrence, KS 66044.
Circle 205 on Inquiry Card

DIP SWITCHES



Series 206 slide actuated switch types have received qualification approval to military spec MIL-S-83504—spec sheet MIL-S-83504/4. The 9 spst switch types, 206-02 to -10, are now approved for all MIL use applications. The devices feature std 0.100 to 0.300" (0.254 to 0.762-cm) DIP centers. Options for the series include low profile actuators (actuators flush with the top of the switch housing), extended actuators, and sealed versions. **CTS Keene, Inc,** 3230 Riverside Ave, Paso Robles, CA 93446.
Circle 206 on Inquiry Card

LINE TO DC POWER SUPPLIES

With an input voltage of 105 to 125 Vac and frequency of 50 to 440 Hz, 4 models in the single 5-Vdc series offer 250-mA, 500-mA, 1-A, and 2-A outputs with 0.05% line and 0.1% load regulation, and 6.5-Vdc overvoltage protection. The dual 15-Vdc series offers 65-, 100-, 200-, and 300-mA outputs with 0.05% line and load regulation. Epoxy encapsulated models are short-circuit protected and rated at <1 mV rms ripple and noise. **Computer Power Source,** 370 Park Ave, Worcester, MA 01610.
Circle 207 on Inquiry Card

4-FLOPPY COMPUTER SYSTEM

An integrated small computer system with 4 full-size floppy discs online, Sol System IV includes the company's Sol-20 mainframe with 50, 176 8-bit words of RAM, Helios II mode 4 disc memory system, PTDOS disc operating system, Extended Disc BASIC, video monitor, and complete documentation. Total mass storage capability on 4 formatted discs is 1.5M bytes. PTDOS functions include complex editors, assembler, device independent files, and random indexed files. **Processor Technology Corp,** 7100 Johnson Industrial Dr, Pleasanton, CA 94568.
Circle 208 on Inquiry Card

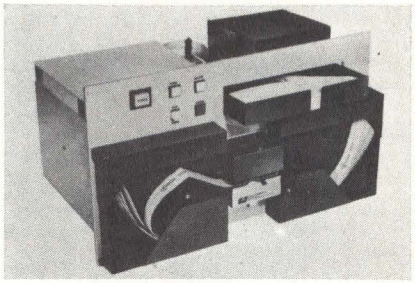
CIRCLE 70 ON INQUIRY CARD →

PRODUCTS

10.5" REEL MAGNETIC TAPE SYSTEMS

Available in 7-track 556/800-bit/in (219/315/cm), 9-track 800-bit/in (315/cm), and 9-track phase-encoded 1600-bit/in (630/cm) recording formats, mag tape systems can operate at up to 25 in (64 cm)/s and can store up to 5.7M char. Interrecord gap is 0.6" (1.5 cm) nom. The 0.5" (1.3-cm) recording tape is contained on reels of up to 10.5" (26.7 cm) in dia. Dual gap (read after write) mag head assemblies and VP, LRCC, and CRCC for error control are used. **Datapoint Corp,** 9725 Datapoint Dr, San Antonio, TX 78284.
Circle 209 on Inquiry Card

PAPER TAPE READER/PUNCH

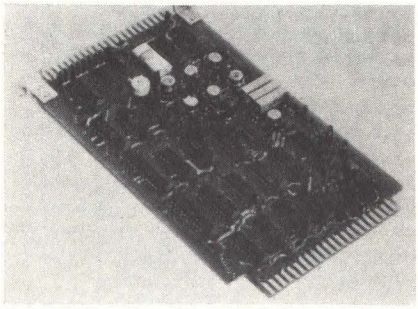


Sprocket-fed model RP 7100/D is a self-contained unit combining a 75-char/s paper tape punch with a 300-char/s photoelectric tape reader. All dc power supplies, and control and signal interface logic circuitry are included. Interface logic and signals are also fully compatible with other reader/punch combinations and most minicomputers. Cleaner perforations are made on 5- through 8-level data on 1, 0.875, or 0.6875" (2.5, 2.2, or 1.75-cm) wide paper or mylar tape. An option accommodates 6-level teletypesetting tape. **Digitronics Div, Comtec Information Systems, Inc,** 53 John St, Cumberland, RI 02864.
Circle 210 on Inquiry Card

10-kVA UNINTERRUPTIBLE POWER SYSTEM

The single-phase UPS model of the TAURUS™ series features an inverter operating at 90% efficiency under full load and at 87% efficiency at half load. A solid-state transfer switch, battery charger with automatic float/equalize modes, and an overload capability of 150% for motor starting or to provide peak power to high inrush loads are included. Frequency and phase synchronization are std, as are output current (limited at 150%) and short-circuit protection. **Nova Electric Manufacturing Co,** 263 Hillside Ave, Nutley, NJ 07110.
Circle 211 on Inquiry Card

DATA ACQUISITION SYSTEM DIAGNOSTIC CARD

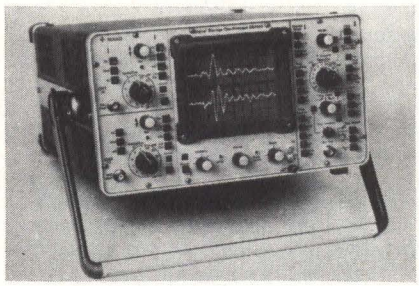


The AC3000 card allows diagnostics to be performed on the AN5400 data acquisition system either in real time on- or offline. Potential failures are detected before they alter accuracy of measurements being taken. Key elements of the system's analog section that can be mounted by the diagnostic card are power supply voltages, A-D and signal processor offset voltages, A-D range accuracy, signal processor programmable gain accuracy, A-D linearity, and ADC slew rate settling time. All digital R/W and DAC output functions can be monitored. **Analogic Corp,** Audubon Rd, Wakefield, MA 01880.
Circle 212 on Inquiry Card

LOW SPEED IMPACT LINE PRINTERS

Using a 48-char set, DOC 1000 and 1200 series, rated at 1000 and 1200 lines/min, have 2 integrated microprocessors to maintain and execute all printer functions from data transfer to forms movement. Model I is IBM 3211/3811 plug compatible, model II is IBM 1403/2821 plug compatible, and model III uses std OEM interfaces. Band printers have fully buffered print line of 132 char, and can handle up to 6-part forms. Slew rates are up to 50 in (127 cm)/s. **Documation Inc,** PO Box 1240, Melbourne, FL 32901.
Circle 213 on Inquiry Card

DIGITAL STORAGE OSCILLOSCOPE



The OS4100 portable, dual trace oscilloscope captures, stores, and displays signals over a range of frequencies without fade or flicker for viewing longterm events and low frequency transients. The instrument is powered from any 110/120- or 220/240-Vac ±10% source. In operation, 1 or 2 input signals pass through an ADC with a 1-MHz sampling rate and are stored in an 8-bit x 1024 RAM. An 8 x 10-cm CRT displays contents of memory. **Gould Inc, Instruments Div,** 3631 Perkins Ave, Cleveland, OH 44114.
Circle 214 on Inquiry Card

CURRENT LIMITED POWER SUPPLIES

Output voltage ranges from 0 to 6 up to 0 to 100 Vdc, with output current ratings to 16 A, are featured in this modular series of power supplies. All are voltage programmable with external resistance. Many provide for remote control of the current limit point and have a true constant voltage/constant current crossover characteristic. In constant voltage operation, line and load regulation are ±0.005% or 2 mV; in constant current operation, line is ±0.1% and load is ±0.2%. **Acopian Corp,** Easton, PA 18042.
Circle 215 on Inquiry Card

PLUG-IN TERMINATION MINI SOLID-STATE RELAY

The 4-A MINI CUBE relay is available with plug-in termination that is compatible with std relay sockets. This allows the user to select an electromechanical or solid-state relay to interface between the control circuitry and load. Relay measures 1 x 1.2 x 1" (2.5 x 3 x 2.5 cm) approx, and has load current switching capability of 0.1 to 4.0 A at 120 or 240 Vac. Logic compatible input circuit is available in operating ranges of 3 to 15 or 14 to 30 Vdc. **Grayhill, Inc,** 561 Hillgrove Ave, La Grange, IL 60525.
Circle 216 on Inquiry Card

THICK FILM CRYSTAL CLOCK OSCILLATOR

LOCO II provides master clock frequencies which can be divided to discrete UART frequencies for various baud rates or divided to provide multiple outputs to drive combinations of baud rate generators, microprocessors, and LSI circuits in a computer system. DIP form oscillator measures 0.820 x 0.520 x 0.250" (2.08 x 1.32 x 0.635 cm), operates from 5 Vdc, and drives 10 TTL gates; 6 discrete frequencies are available. Stability from 0 to 70 °C is ±0.05%. **Motorola Inc, Component Products,** 2553 N Edington, Franklin Park, IL 60131.
Circle 217 on Inquiry Card

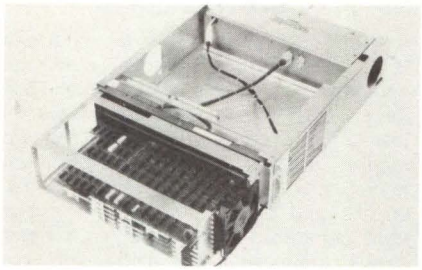
P/ROM PROGRAMMER WITH RS-232-C INTERFACE

Automatically setting baud rate of series 90 programmers to between 14 and 2400 baud, depending on incoming data rate, option 9105-6 allows M900 P/ROM programmer and M920 peripheral P/ROM programmer/duplicator to connect to computers and semi-intelligent terminal equipment. Options for 110-, 300-, and 1200-baud operation of the programmers in fixed baud rate applications are also available. **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 93940.
Circle 218 on Inquiry Card

SINGLE FIBER FIBER OPTIC CONNECTOR

A precision ferrule on the connector provides optical alignments that solve fiber positioning problems. Model FOS connector positions fiber ends to maximize coupling efficiency. Fiber to fiber coupling losses are typically 2 dB or less. Designed to meet military-type connector specs while in a mated condition, connector is available in components or complete cable assemblies. Fiber optic connector is environmentally sealed and has axial, angular, and gap alignment. **ITT Corp, Cannon Electric Div,** 666 E Dyer Rd, Santa Ana, CA 92702.
Circle 219 on Inquiry Card

EXPANSION CHASSIS FOR PDP-11

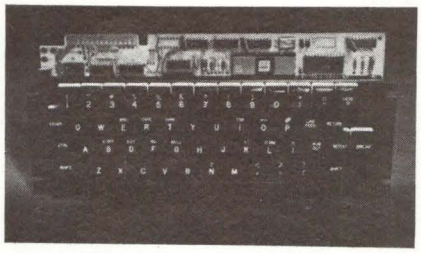


Look-alike model 919 expansion chassis for use with DEC PDP-11 minicomputers features snap-off front panel and extendable inner module; PC boards may be serviced without removing chassis from rack. LED indicators and toggle switch controls are available on the front panel. Two 4-slot or one 9-slot units hold memory, peripheral or memory controllers, or LSI-11 boards. Power supply provides 5 V at 15 A, ±15/12 V at 2 A fully regulated. **Western Peripherals, Inc, Wesperline Div,** 1100 Claudina Pl, Anaheim, CA 92805.
Circle 220 on Inquiry Card

PROGRAMMABLE FLOPPY DISC FORMATTER

Model 61F-600 features single-density (FM) and double-density (MFM or M²FM) modes with single- and double-sided operation. Under control of host computer, a single formatter handles up to 8 mixed density disc drives with multiple formats. IBM compatible and other industry-standard and nonstandard formats are used. Formatter employs an 8 x 300 bipolar microprocessor with 256 bytes of working storage. **Applied Data Communication,** 1509 E McFadden Ave, Santa Ana, CA 92705.
Circle 221 on Inquiry Card

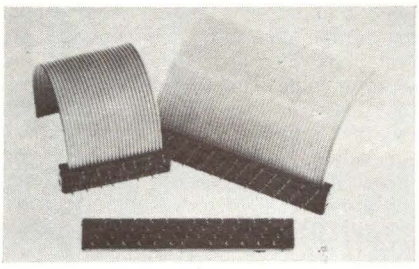
INTELLIGENT KEYBOARD WITH CAPACITIVE KEYSWITCHES



An 8-bit, single-chip microprocessor and patented low profile keyswitches with square capacitance plates comprise this keyboard. Software controllable key functions allow it to be programmed to the application. The microprocessor permits automatic repeats, multiple application programs in a single intelligent encoder, field program changes with firmware, serial or parallel I/O, and N-key rollover. Switches have a life expectancy of 100M operations. **C. P. Clare & Co, General Instrument Corp,** 3101 W Pratt Ave, Chicago, IL 60645.
Circle 222 on Inquiry Card

PADDLEBOARD CONNECTOR

6500 series connector is a permanent cable to board connector that connects flat cable to the plane of a PC board, using the same locking barb contact that is used in 6300, 6400, and 6700 series devices. Beryllium copper contacts are plated gold 0.000020" (0.000508 mm) thick and are available in 2 sizes to accommodate 0.062, 0.093, and 0.125" (1.57, 2.36, and 3.175 mm) thick PC boards. Black valox is used to make the insulator body. **Stanford Applied Engineering, Inc,** 340 Martin Ave, Santa Clara, CA 95050.

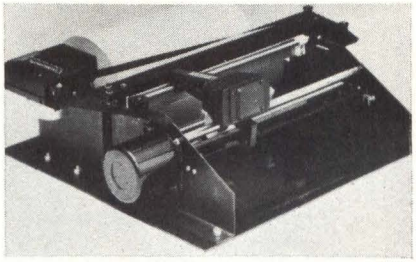


Circle 223 on Inquiry Card

CIRCLE 71 ON INQUIRY CARD →

PRODUCTS

PERIPHERAL PRINTER MECHANISM



The bidirectional, impact dot matrix print mechanism has a print rate of 120 char/s and a line capacity of 80 char at 10 char/in (4/cm). It uses 8.5" (21.6-cm) std roll paper, with up to 5-ply multiple copies. Paper slew rate is 400 lines/min. The device contains a pressure roller paper feed with motorized paper advance, and cartridge ribbon with independent power motor. Power requirements are 117 Vac, 60 cycle. Interface electronics are included. **MarComm Inc,** PO Box 535, Ramona, CA 92065.
Circle 224 on Inquiry Card

MULTIFONT CAPABILITY FOR MATRIX PRINTERS

Library card capability can be inserted into the model 2300's PC card cage, and can be programmed to add up to 4 different type and special symbol fonts to std font with each printer. Model 2300 offers optional plug-in ROM which contains 4 foreign language or special fonts. Each of 8 additional fonts recognizes full 128-char ASCII set and can print up to 96 char. For special purpose applications, OEM can use his own P/ROMS and the library card to design and print custom fonts. **Diablo Systems, Inc,** 24500 Industrial Blvd, Hayward, CA 94545.
Circle 225 on Inquiry Card

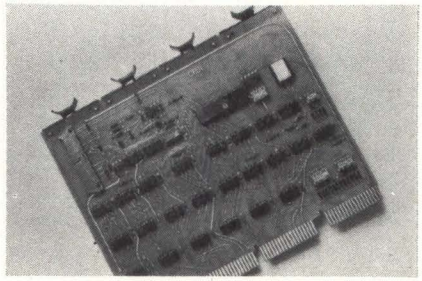
MULTIPLE-FUNCTION CONTROLLER BOARD

64k-bytes memory, 4 asynchronous communication channels, parallel line printer interface, realtime clock, and TTY port are provided on the 15 x 15" (38 x 38 cm) PC board which occupies 1 slot in a Data General Nova 3[R] computer chassis. Quintroller is complete with cable set for communications channels, TTY, and line printer. Communication channels are software compatible with DG 4060 asynchronous multiplexer, line printer with 4034/4193 printer controller, realtime clock and TTY with 4008 and 4010, respectively, and memory with DG8547. **Rianda Electronics, Ltd,** 2535 Via Palma, Anaheim, CA 92801.
Circle 226 on Inquiry Card

DATA CONCENTRATOR/ MULTIPLEXER

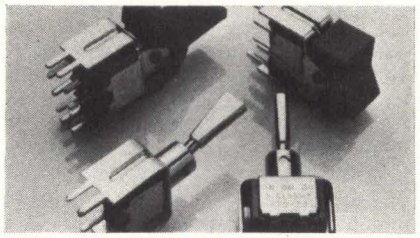
Suited to inquiry/response systems, model 811 allows up to 8 ASCII high speed data lines, operating separately at 75 to 19.2k baud, to access a single computer port. Buffer storage of several hundred char/line enables a small computer system to support many devices without losing data. Remote control of DSR/DTR, line speed, and reinitialization of individual line interfaces is possible. Polled line units are available with line editing and preprogrammed response protocols. **Kaufman Research,** 99 Sylvian Way, Los Altos, CA 94022.
Circle 227 on Inquiry Card

SERIAL LINE CONTROLLER FOR PDP-8



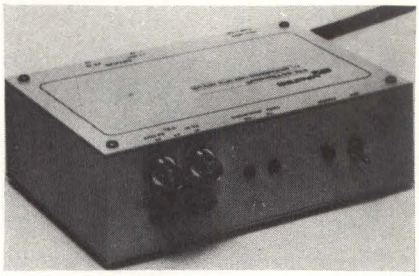
Providing an interface between the PDP-8 and an asynchronous EIA or 20-mA current loop interface, the SLC8 plugs directly into the DEC PDP-8 Omnibus™. The controller offers switch selectable baud rates (50 to 9600 in 13 increments); 5, 6, 7, and 8 data bits; 1, 1.5, and 2 stop bits; and parity selection. Device codes for transmit and receive are independently switch selectable. **Computer Extension Systems, Inc,** 17311 El Camino Real, Houston, TX 77058.
Circle 228 on Inquiry Card

PC BOARD SWITCHES



The 574 series miniature toggle and 577 series rocker and lever-operated switches have support brackets for vertical mounting on PC boards to prevent actuation stress from being applied to terminal-circuit connections. UL-listed switches are available in spdt and dpdt models with 9 switching function options; std, low level, or combination contact ratings; and PC terminals with or without epoxy seals. Actuator options include a variety of sizes and finishes. **Dialight, a North American Philips Co,** 203 Harrison Pl, Brooklyn, NY 11237.
Circle 229 on Inquiry Card

DIFFERENTIAL TTL FIBER OPTIC DATA LINK



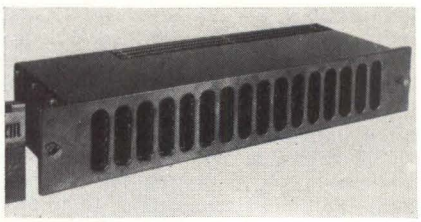
Differential TTL I/O in a 9-pin connector is a std feature of modules TTK and TTH fiber optic data links. Signals can be brought in and out of data link through coaxial cable terminated with BNC connectors or std cable terminated with 9-pin connector. TTK provides data rates to 10M bits/s over 3000 ft (915 m); TTH operates to 3M bits/s over 300 ft (91 m). Models operate in full duplex and have self-contained power supplies. Links can be converted to repeater operation by an external connection between BNC connectors. **Valtec Corp,** West Boylston, MA 01583.
Circle 230 on Inquiry Card

INTELLIGENT TAPE MAINTENANCE EQUIPMENT

Master Analyst family includes a vacuum column tape transport which cleans tape at 500 in (12.70 cm)/s; analysis cycle is 250 in (635 cm)/s. Field upgradeable electronics allows users to change equipment from 1600 to 6250 bits/s. Programmable analysis can allow analyzer to automatically reject tapes which will cause a malfunction. A microprocessor automatically controls all analysis functions. Buffered memory allows for accumulation of information. **Data Devices International,** 6301 DeSoto Ave, Woodland Hills, CA 91364.
Circle 231 on Inquiry Card

3.5" SLOT BLOWER

A 12.5" (31.8-cm) wide jet airstream is delivered vertically into an electronic enclosure by the blower, which produces 150 ft^3/min (0.07 m^3/s) with a low audible noise level. Slot Blower model 1E220C has a UL approved motor, 115 V, 50/60 Hz, single phase, 80 W, and 3150 r/min. The case is light semigloss gray finish with heavy gauge stainless steel grille. Air inlet filter is a permanent washable type. **McLean Engineering Laboratories,** 70 Washington Rd, Princeton Junction, NJ 08550.



Circle 232 on Inquiry Card

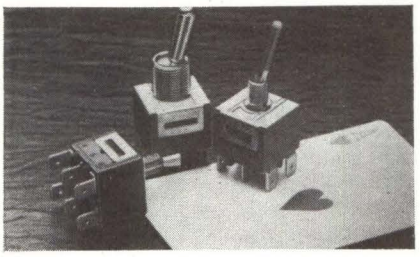
32k x 12 CORE ADD-IN FOR PDP-8/A

Single-board DR-118A can be used with DEC's KT8-A memory management option which expands the max addressing capability of the PDP-8/A minicomputer from 32k x 12 to 128k x 12. The 32k x 12 system is packaged on a DEC hex board. Access and cycle times are 330 and 1200 ns, respectively. It operates on 5, −5, and 20 V. A DIP switch is provided for address strapping. All systems have a min burn-in of 72 h. **Dataram Corp,** Princeton-Hightstown Rd, Cranbury, NJ 08512.
Circle 233 on Inquiry Card

SMALL AC-POWERED DIGITAL PANEL METER

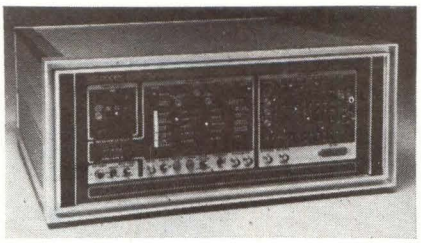
LCDs measuring 0.5" (12.7 mm) high are used in the mini DM-3100U2 3½ digit meter for display only applications. A tiny ac transformer accepts 115-Vac, 60-Hz power, and 9- to 15-Vdc external sources (at 3 mA) may also be used. Transformer dc isolation is 300 V rms. Features include CMOS LSI microcircuit ADC, requiring only 5 pA of bias current; autozeroing; autopolarity, ±1.999-Vdc input range; and internal ratiometric reference for scaling engineering units. **Datel Systems, Inc,** 1020 Turnpike St, Canton, MA 02021.
Circle 234 on Inquiry Card

MINI 10-A POWER SWITCH WITH TOGGLE ACTUATORS



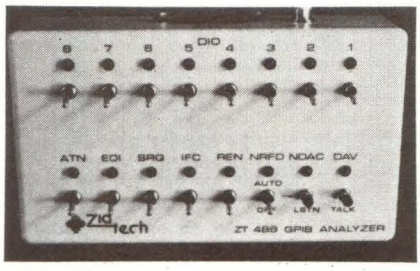
Dpdt model 9221 switch with bushing mount accepts 11 toggle handle actuators: S, L, L1, L2, L3, L4, P1, P3, P4, T, and T1. These include short, tall, thick, thin, round, flat, and shockproof plastic. With the exception of the plastic handle, all toggles are made of chrome-plated brass and are UL, CSA, and VDE listed. The power switch accepts 10 A with resistive load at 125 Vac, or 5 A with resistive load at 250 Vac. **C&K Components, Inc,** 103 Morse St, Watertown, MA 02172.
Circle 235 on Inquiry Card

AUTOMATIC CIRCUIT QUALITY MONITORING SYSTEM



An automatic model of the Circuit Quality Monitoring System provides the added capability of sequencing through each of the company's attached modems (up to 64), monitoring them for critical signals and degraded network performance. Detected degradations or circuit dropouts cause the system to generate an alarm report which can be printed or logged into the user's CPU for recordkeeping and line analysis. The ACQM also can be controlled from a CRT or KSR type of terminal. **Codex Corp,** 15 Riverdale Ave, Newton, MA 02195.
Circle 236 on Inquiry Card

LOGIC ANALYZER FOR IEEE-488 BUS SYSTEMS



Handheld ZT 488 enables designers to observe and/or control all transfers on the GPIB, HPIB, IEEE-488 standard bus. Analyzer displays bus including 8 data, 5 control, and 3 handshake lines. User may control all signals using the instrument's switch register. Data and control lines are set by user and handshake is performed by internal logic automatically or when single stepped by front panel buttons, allowing manual control of the bus or simulation of an instrument on the bus. **Ziatech Corp,** 10762 La Roda Dr, Cupertino, CA 95014.
Circle 237 on Inquiry Card

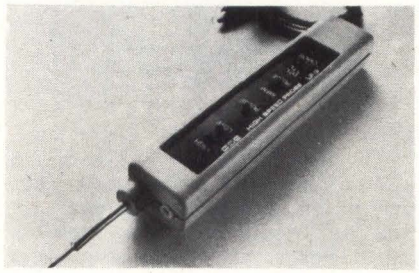
IBM SERIES/1 PRINTERS

Medium speed, high performance subsystems consist of a printer, ranging in speeds from 62.5 to 300 lines/min, and a self-contained control board that plugs into the Series/1 processor. The series features a char belt mechanism assuring char alignment and interchangeability, adaptive logic to adjust lines, 6-part printing on forms up to 17.5" (44.5 cm) wide, and universal power supplies. User defined char font sets, and 96-char ASCII or 48-char EBCDIC sets are optional. **Data 100 Corp,** 6110 Blue Circle Dr, Minneapolis, MN 55435.
Circle 238 on Inquiry Card

CIRCLE 72 ON INQUIRY CARD →

PRODUCTS

10-ns LOGIC PROBE



Capable of detecting, displaying, and optionally latching pulses as fast as 10 ns, the LP-3 responds to positive- or negative-going leading edge of a pulse, or to pulse trains up to 50 MHz. Pulse duty cycle can be accurately estimated by observing relative brightness of high and low logic state LEDs. Switches select DTL/TTL or HTL/CMOS family operation, and enable the latching Pulse Memory feature. A ground connection adjacent to the probe tip socket permits low input capacitance for high speed readings. **Continental Specialties Corp,** 70 Fulton Ter, New Haven, CT 06509.
Circle 239 on Inquiry Card

HIGH POWER TRANSIENT VOLTAGE SUPPRESSORS

TransZorb™ silicon suppressors are designed for industrial and computer power supply applications where high energy, fast rise time transients endanger sensitive solid-state circuitry. Capable of replacing crowbar circuits, the devices clamp excessive voltages and do not cause power interruptions. The 5KP ranges from 5.0 to 110 V and features a peak pulse power dissipation of 5 kW. The 15KP series ranges from 17 to 280 V with a peak pulse power dissipation of 15 kW. **General Semiconductor Industries, Inc,** 2001 W Tenth Pl, Tempe, AZ 85281.
Circle 240 on Inquiry Card

ANSI-STANDARD MUMPS LANGUAGE

Meeting ANSI-Std spec X11.1-1977, with extensions, the Digital Standard MUMPS (DSM-11) software package runs on appropriately configured PDP-11/34, -11/60, and -11/70 computer systems. The data base management package includes the MUMPS interpreter, an operating system, and a hierarchical file system. Min hardware requirements are 32k words of memory and one of the company's disc subsystems with a min 7.5M-byte capacity. Additional memory, data storage, and I/O devices are supported. **Digital Equipment Corp,** Maynard, MA 01754.
Circle 241 on Inquiry Card

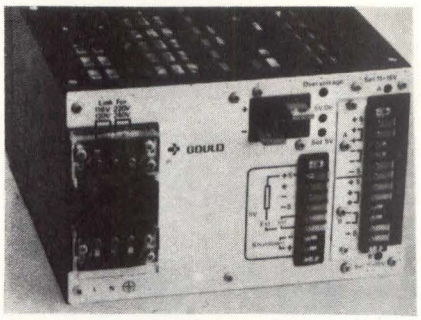
TERMINET 30 TWX COMPATIBLE INTERFACE

Intended for General Electric TermiNet 30 interface, the 4910 system offers 4 choices of transmission. It has dial-up capability for timesharing terminals through DDD at 10- or 30-char/s transmission speeds, access to the TWX network, direct hookup for local computer communications front end, and access to the TWX/DDD networks for multiple add-on terminals through a special RS-232 interface. Also featured are 80 or 132 print positions, single or dual mag tape cassettes, and 1200-baud tape transmission. **Omnitec Data,** 2405 S 20th St, Phoenix, AZ 85034.
Circle 242 on Inquiry Card

12- AND 16-CHANNEL MULTIPLEXERS

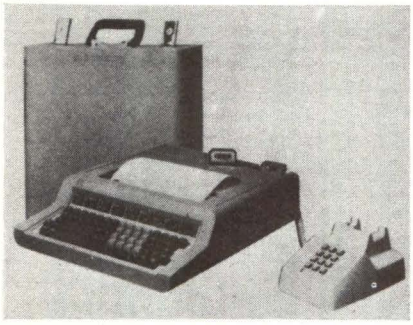
Micro800, a 4- and 8-channel statistical multiplexer, is now available in 12- and 16-channel configurations. Replacing time-division multiplexers, the unit is designed to permit several terminals, typically teletypewriter compatible terminals operating at 300, 1200, 2400, or 4800 bits/s, to share 1 telephone line with max efficiency, minimizing line and modem costs. Retransmission on error is performed automatically for all terminals using the multiplexer. **Micom Systems, Inc,** 9551 Irondale Ave, Chatsworth, CA 91311.
Circle 243 on Inquiry Card

3-OUTPUT SWITCHING POWER SUPPLIES



MGT-400 delivers 400 W from a 110- or 220-V line and operates from 47 to 440 Hz. Main output provides up to 5 V at 60 A; 2 auxiliary outputs can be set from 8.5 to 15 V with an 8-A current rating. MGT-250 delivers a 250-W output, operating from 24- or 48-V supplies. Main output provides 5 V at 25 A; others are set at 12 V with an 8-A current rating. Designed for communications uses, both supplies have overcurrent and overvoltage protection on all outputs. **Gould Inc, Electronic Components Div,** 4601 N Arden Dr, El Monte, CA 91731.
Circle 244 on Inquiry Card

ASR TERMINALS WITH 32k RAM



A 32k RAM option has been added to the Miniterm 1204 desktop and 1205 portable ASR terminals, which have an integral 32k RAM and built-in minicassette tape transport with 68k char of removable storage. The dual storage media of memory and tape work in tandem to provide simultaneous transmit/receive capability, tape to memory, memory to tape, and tape to memory to line transmission. The units also include a 3-mode keyboard, 35-char/s thermal printer, and switch selectable ASCII or binary code. **Computer Devices, Inc,** 25 North Ave, PO Box 421, Burlington, MA 01803.

Circle 245 on Inquiry Card

HIGH RESOLUTION 16-BIT DACs

DAC327C-16 and DAC327C-16-ER, packaged in miniature 24-pin metal DIPs, have been added to DAC327 series. Both include resistor ladder, switches, and gain trimmed output amp. With a −25 to 85 °C temp range, converters feature 0 to 10 V output range, ±0.003% FSR typ linearity, 30-μs settling time to ±0.005% FSR for 10 V change and 8 μs to ±0.005% FSR for 2 LSB change. TCRs are gain, ±20 ppm FSR/°C max; linearity, ±5 ppm FSR/°C typ; offset, ±2 ppm FSR/°C max. **Hybrid Systems Corp,** Crosby Dr, Bedford, MA 01730.

Circle 246 on Inquiry Card

VIDEO TERMINAL BOARD WITH SOFTWARE CONTROL

Display formats of the VR-106—80 x 24, 80 x 12, 40 x 24, or 40 x 12—are controlled by software. Display consists of 128 u/lc and Greek char, in 7 x 7 or 7 x 9 font. A bipolar P/ROM char generator simplifies font development; each char position can be used for reverse video, underline, half intensity, blinking, or graphics block. Compatible with Intel Multibus™ SBC series computers, the video board appears as memory. **Datacube/SMK-I,** 670 Main St, Reading, MA 01867.

Circle 247 on Inquiry Card

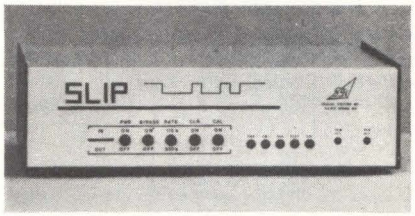
ROTARY PULSE GENERATOR

The Astrol bidirectional Rotopulser, which discriminates between directions of rotation, converts rotation of electrical pulses to actuate controller counters, printers, motors, and other equipment with pulse inputs. Pulses are supplied from 1 or 2 channels, depending on the direction of rotation. A count direction output is also supplied; it is high for clockwise rotation of the shaft. Models A328 and A432 are designed to withstand conditions of vibration and frequent shaft direction reversals. **Associated Controls Pty Ltd,** 55 Fairford Rd, Padstow, New South Wales, Australia 2211.

Circle 248 on Inquiry Card

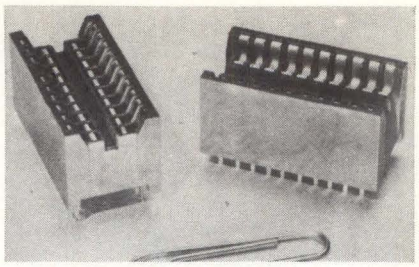
PRODUCTS

SERIAL LANGUAGE PLOTTER CONTROLLER



Installed between a terminal and modem or local computer, SLIP controller provides plotting and graphics capability through its connection to an X-Y recorder. Its microprocessor allows for internal vector and character generation. Functioning independently of formatting constraints imposed by programming language, the device does not interrupt user/computer communication, but rather intercepts plot data from computer and generates X-Y signals to plotter. The X and Y outputs accommodate input requirements of most X-Y recorders. **Special Systems, Inc,** 8045 Newell St, Silver Spring, MD 20910.
Circle 249 on Inquiry Card

20-LEAD DIP SOCKET

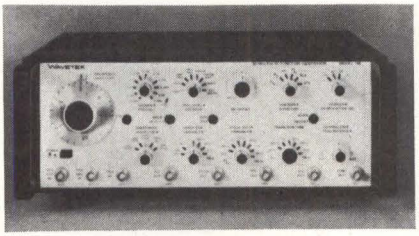


Elevated side walls of DIP sockets enhance durability and usability for burn-in, test, and IC applications requiring fast, damage-free insertion. A double-sided contact insures positive device connection and retention. Contact design provides long life with insertion forces as low as 10 g/pin. The 20-lead socket is tooled for 0.300" (0.762-cm) lead row centers. Contact and body materials permit use in temp ranges from −55 to 300 °C. **Wells Electronics, Inc,** 1701 S Main St, South Bend, IN 46623.
Circle 250 on Inquiry Card

MAINTENANCE AID FOR MAGNETIC TAPE DRIVES

Logic circuitry of a formatter and up to 4 7- or 9-track transports can be exercised with the DEMC-3, providing offline troubleshooting capability without interrupting other computer system functions. The card operates all of the company's NRZI, phase encoded, and dual mag tape drive systems without I/O interfacing. Selectable functions allow forward or reverse reading and writing in normal or "on the fly" mode, as well as read after write error checking. **Digi-Data Corp,** 8580 Dorsey Run Rd, Jessup, MD 20794.
Circle 251 on Inquiry Card

PULSE/FUNCTION GENERATOR

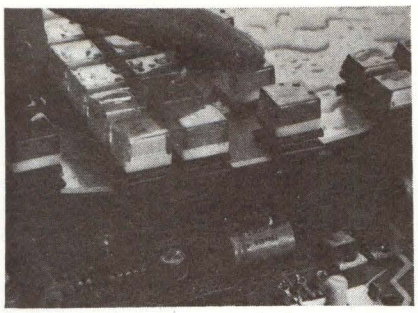


A 50-MHz combination pulse and function generator, the model 166 signal source operates over the frequency range of 0.0001 Hz to 50 MHz and delivers a full 30-V pk-pk output with sine, square, triangle, ramp, and pulse outputs. As a pulse generator, it offers independent repetition, width, and rise and full transition time control. Fixed TTL outputs are available simultaneously with the variable output. As a function generator, the device provides linear and logarithmic sweep capability; trigger, gate, and double trigger modes of operation; as well as external am and fm modulation capability. **Wavetek,** PO Box 651, San Diego, CA 92112.
Circle 252 on Inquiry Card

SIGNAL CONDITIONER

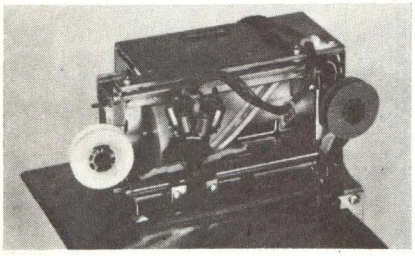
Carrier amps offer both switch selectable constant voltage and constant current transducer excitation for designers of transducer based measurement or control systems. Nom values of voltage and current are 2.5 V with a regulation of 0.25% into 40 Ω or more, and 10 mA into 10 to 240 Ω. The unit can be used with both linear variable differential and variable reluctance type transducers. Sensitivity is 5 mV for full-scale output of 10 V. **Natel Engineering Co, Inc,** 8954 Mason Ave, Canoga Park, CA 91306.
Circle 253 on Inquiry Card

LIGHTED KEYBOARD SWITCH FOR EXTREME ENVIRONMENT



T-5J lighted keyboard switches incorporate a neoprene boot that seals all internal switch parts both above and below the keyboard mounting panel from extreme conditions. They offer high switch to switch consistency and 20M-cycle life for most low voltage (24 V max) PC mountable applications. The mechanical switch has gold cross bar contacts. Also included are a precision nonbinding tracking surface between plunger and body, and T-1 bipin incandescent lamp. **Mechanical Enterprises, Inc,** 8000 Forbes Pl, Springfield, VA 22151.
Circle 256 on Inquiry Card

ALPHANUMERIC TICKET PRINTER SUBSYSTEM



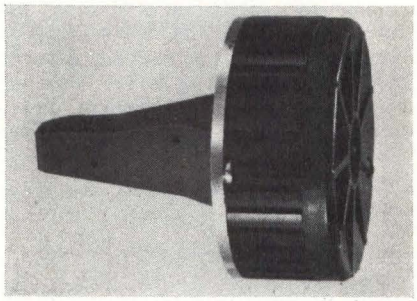
Mating microprocessor and LRC 7040T print mechanism, SP-308 subsystem is economically designed for OEM use. The 40-col, 5 x 7 dot matrix impact printer accepts multicopy forms up to 11 x 17″ (27.9 x 43.2 cm). Max of 22 lines may be printed at 50 char/s. Data are accepted in either RS-232-C or 20-mA current loop formats, with std data rates to 9600 baud. Unit provides 40-char buffering, double-width print capability, tab function, and pressure-roll release control. **Syntest Corp,** 169 Millham St, Marlboro, MA 01752.
Circle 254 on Inquiry Card

ACOUSTIC COUPLER

Model FM30 transmits and receives asynchronous, serial data at speeds up to 300 bits/s in half- or full-duplex mode over the switched telephone network, permitting data communications through a telephone handset. Features of the acoustic coupler include crystal controlled frequencies and rugged construction. It is compatible with all Bell 103 and 113 type modems and interfaces with devices utilizing the RS-232-B/C or 20-mA current loop stds. **Multi-Tech Systems, Inc,** 82 Second Ave SE, New Brighton, MN 55112.

Circle 255 on Inquiry Card

HIGH SPEED MATRIX PRINTER



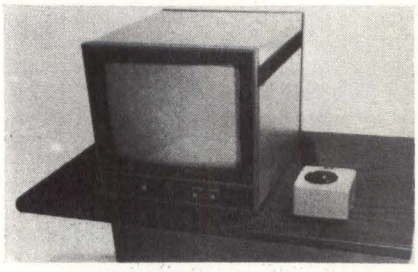
Mark IV OEM matrix printhead is designed for heavy duty use and can be easily integrated into any new or existing printer design. 9 0.014" (0.335-mm) dia print wires arranged in a single vertical column have a frequency of 1 kHz, enabling the unit to print through 6 carbon copies. Print wire tip to platen gap is 0.025" ±0.005" (0.635 ±0.127 mm). Approx 6.6 W of printhead power is required for avg text at 200 char/s in a 9 x 7 font. Typ operating voltages are 35 to 48 V. Peak operating current is 2.7 A typ. **Universal MicroPrinters, Inc,** 1155C Chess Dr, Suite F, Foster City, CA 94404.
Circle 257 on Inquiry Card

PORTABLE PC BOARD TESTER

A programmable minisystem for field service diagnosis of PC board faults, model 2225 contains a 16-bit microcomputer with 192 fully programmable driver/sensors, guided probe diagnostics, 6 user power supplies, magnetic tape program storage, paper strip printer, keyboard, alphanumeric display, and a built-in digital multimeter. An RS-232 interface allows down loading of testing programs translated from programs prepared for other PC board test systems. **GenRad, Inc,** 300 Baker Ave, Concord, MA 01742.

Circle 258 on Inquiry Card

IMAGE COMPUTER WITH COMPUTATIONAL FEATURES

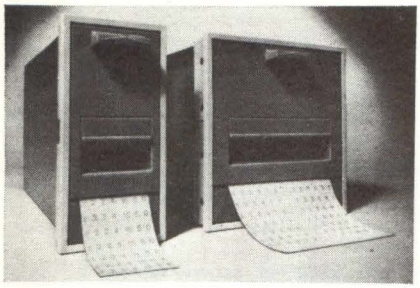


Model 70 is organized into input, output, memory, and control/arithmetic sections, and can perform arithmetic operations at a rate of 10M/s. Processing speeds of 100 ns/pixel are achieved between 512 x 512 arrays. Display terminal is compatible with NTSC formats in both input and output. Each of 3 parallel pipeline processing channels is selectively fed by any or all refresh memory channels and/or the digitized video input, performing arithmetic operation on data stored in refresh memory channels. **Stanford Technology Corp,** 650 N Mary Ave, Sunnyvale, CA 94086.
Circle 259 on Inquiry Card

OFFLINE CONVERTER POWER SUPPLIES

Encapsulated modular supplies operate over a 2:1 range of either ac or dc inputs and deliver 1, 3, and 4 outputs up to 25 W. Remote power shutdown of supply is achieved by application of a std TTL level logic command. USI and CSI models accept inputs of either 70 to 140 Vac at 47 to 440 Hz or 100 to 200 Vdc while US2 and CS2 models accept either 140 to 280 Vac at 47 to 440 Hz or 200 to 400 Vdc. A line- or dc-powered primary output switch mode regulator operates with near constant 75% efficiency. **Semiconductor Circuits, Inc,** 306 River St, Haverhill, MA 01830.
Circle 260 on Inquiry Card

PRINTING COUNTERS



PG series can count at up to 25 input pulses/s and print at 1.5 lines/s. Used for production monitoring, test instruments, traffic control, and recording weight, flow, time, and energy consumption, units have a life expectancy of 50M impulses or 2M printing cycles with 200k zero reset operations. Counting elements can be operated by 12, 24, or 48 Vdc while optional time/date elements require 110 Vac at 60 Hz, 220 Vac at either 50 or 60 Hz, or a train of external timing pulses. **Sodeco, Div of Landis & Gyr, Inc,** 4 Westchester Plaza, Elmsford, NY 10523.
Circle 261 on Inquiry Card

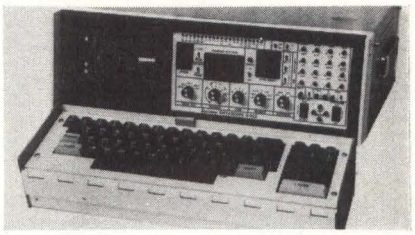
19k-BIT/s MODEM

Modem N10, for transmission over dc-coupled 2- or 4-wire lines, is suitable for speeds up to 19.2k bits/s. Operating in the voice frequency band, it may be used for speeds of 200 through 9600 bits/s. Featuring a balancing network for 2-wire duplex operation, unit is capable of multipoint operation for a large number of stations, and includes a test facility to check functioning of equipment. Binary dc keying is used for transmission. Unit is packaged in a flat case measuring 2.75 x 8.26 x 11.7" (6.99 x 20.98 x 29.7 cm). **Siemens Corp, Data Communications Dept,** 186 Wood Ave S, Iselin, NJ 08830.
Circle 262 on Inquiry Card

MINIATURE ELECTRONIC BUZZERS

Series CMB pin-type solid state buzzers, in 6- and 12-Vdc models, are intended for warning or monitoring systems in computer peripherals. Current drain is 8 to 25 mA for the 6-V model, and 6 to 15 mA for the 12-V; yet they generate an audible signal of 75 dB at 1 ft (0.3 m). Pins conform to std DIP sockets, or may be soldered directly to PC boards without additional wiring. Buzzers have withstood an endurance test of a minimum of 500k cycles of 1-s pulses followed by 168 h of continuous use. Op temp ranges are −40 to 159 °F (−40 to 70 °C). **Star Micronics, Inc,** Pan Am Bldg, 200 Park Ave, New York, NY 10017.
Circle 263 on Inquiry Card

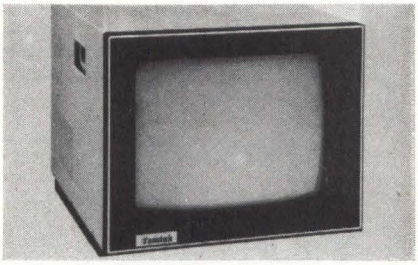
DATA COMMUNICATIONS TEST INSTRUMENTS



Additions to Datascope family of test instruments include the D-502B, which serves as a data monitor, data analyzer, and interactive data simulator and tester. D-301, a lightweight, portable instrument for diagnosing data communication problems, features large solid-state memory and contains a user-defined data trap. Unit operates at speeds up to 72k bits/s. D-201 data printer/monitor is a companion for units equipped with optional printer output feature. A digital tape unit and an ASCII/EBCDIC keyboard enhance the 300/500 series. **Spectron Corp,** 344 New Albany Rd, Moorestown, NJ 08057.
Circle 264 on Inquiry Card

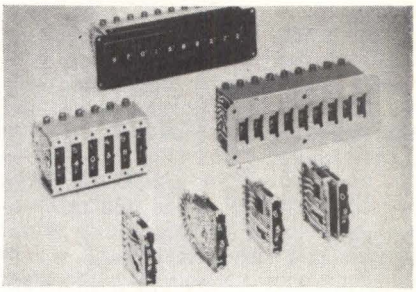
HIGH RESOLUTION COLOR MONITORS

1000 line 19" (48 cm) monitors for use with graphics and image display systems, feature 1280 x 1024-pixel addressability with a bright color display which allows users to present more data with finer detail and permits use of higher density memories and larger capacity microprocessors within display controller devices. Resolution is made possible by use of a black matrix tri-dot color tube with 0.31-mm pitch. Max misconvergence spec of a circle on the screen is 0.62 mm. Video bandwidth is 40 MHz. **Ramtek Corp,** 585 N Mary Ave, Sunnyvale, CA 94086.



Circle 265 on Inquiry Card

MULTIPLE STATION THUMBWHEEL SWITCHES

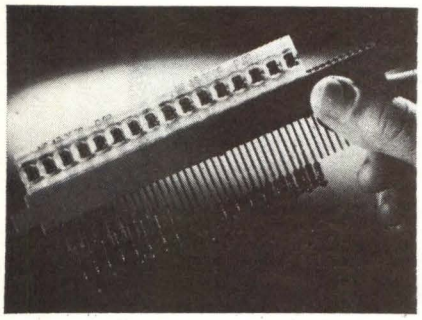


Metal-Mite 2 series offers flexible output code selection and up to 20 switching stations, and provides 2-pole switching modules. Switches are recommended for new applications and retrofitting machine controls and data processing and manufacturing process controls. Decimal, BCD, BCO, and hexadecimal codes are available. Modules with 8, 10, 12, and 16 positions, switch assemblies with or without bezels, and switches with escutcheons are all included in the series. **Switchcraft, Inc,** 5555 N Elston Ave, Chicago, IL 60630.
Circle 266 on Inquiry Card

PASCAL COMPILER

Available for use on Data General's minicomputers running under RDOS, PASCAL compiler compiles itself in a mapped Nova or Eclipse, or unmapped Nova with 32k of memory and a small operating system. PASCAL, which incorporates the best features of several languages, is conducive to easy program debugging and documentation. Since the use of this language is becoming increasingly important in the computer field, compiler meets current needs of computer users. Package includes all source and binary code, and ready to run demonstration programs. **Rhintek, Inc,** PO Box 220, Columbia, MD 21045.
Circle 267 on Inquiry Card

END STACKABLE 8-DIGIT LED ARRAYS



With a nom 0.140" (0.36-cm) char height, NSA1588A features excellent light transmission and wide angle visibility. PCB type terminals allow easy wire, pin soldering, or card edge connection. Modular design permits end to end stacking to form larger units. Each digit consists of 7 segments with a right-hand decimal point. 8 inputs select segments and decimal (anodes); 8 others select digit (cathode). GaAsP LED displays operate with TTL, DTL, or MOS interface circuits. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

LOW COST POWER SUPPLIES

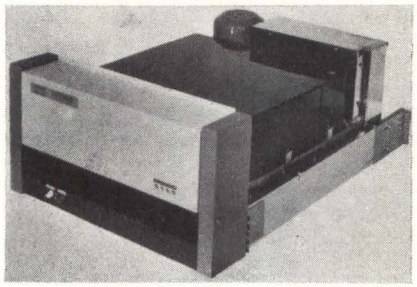
Designed to meet MIL STD-810C specs, the LN series contains 42 models in 5 package sizes with single output voltages of 5, 6, 12, 15, 20, 24, and 25 V, and dual outputs of 5 V ±5% adj, 9 to 12 V adj, and ±15 V to ±12 V adj. Features include 5-mV pk-pk max output noise and ripple. Current ratings range up to 22 A; overvoltage protection is std on 5 V models. Units can be used with or without covers, are convection cooled, and are fungus proof. **Lambda Electronics,** 515 Broad Hollow Rd, Melville, NY 11746.
Circle 268 on Inquiry Card

ALPHANUMERIC/GRAPHICS CRT CONTROLLER

MSBC-24/320, a TV CRT controller, provides an interface between any microprocessor and a TV monitor and integrates an alphanumeric and graphic display on the same PC board. Displays are aligned and scaled to occupy the same screen area, with the alphanumeric section outputting a full 24-line x 80-col text and the graphic portion generating a raster of 240 x 320 dots. Card input resembles a 4096 x 8 static RAM with an access time of 500 ns. Graphic data is addressed as 8-bit wide segments. **Matrox Electronic Systems,** PO Box 56, Ahuntsic Station, Montreal, Quebec H3L 3N5, Canada.
Circle 269 on Inquiry Card

PRODUCTS

DISC STORAGE DRIVE



Combination of head/track and moving arm in the M225X series provides the user with a powerful disc memory. Moving arm portion allows staging of files into and out of main memory, while head/track option provides fast access to high usage files. Winchester technology heads are employed. Each data access arm has 2 R/W heads. Disc media are nonremovable and sealed. Storage capacities are 12.7M, 25.4M, or 50.8M bytes of unformatted data. Access times are 10 ms track to track and 40 ms avg. **Fujitsu America Inc,** 2945 Oakmead Village Ct, Santa Clara, CA 95051.
Circle 270 on Inquiry Card

EMI/RFI AND UL STANDARD 478 AIR FILTERS

Series K aluminum air filter removes dust and lint from air being circulated for cooling purposes. Filter also has excellent emi/rfi attenuation characteristics in electric and plane wave fields, and meets some UL Standard 478 requirements. Staggered baffle design of filter sets up a controlled turbulence in the air passing through. Air is bounced from baffle to baffle to increase filtering surface area. When aluminum filters are dirty, performance is restored by washing and recoating. **Research Products Corp,** 1015 E Washington Ave, Madison, WI 53701.
Circle 271 on Inquiry Card

VIDEO INTERFACE BOARDS

Available in both 50 (CRT-1000A) and 60 Hz (CRT-1000B), the 16-line x 64-char video interface is based on the company's CRT processor chip (SFF-96364). Also included are a 1k x 6 RAM, a 64 x 7 x 5 row scan char generator, and supplementary logic. It accepts data at TTL levels in ANSI std ASCII, and provides a composite video output which can be directly connected to any std CRT monitor. **Nucleonic Products Co, a Div of DuMont Electronics Corp, a Thomson-CSF Co,** 6660 Variel Ave, Canoga Park, CA 91303.
Circle 272 on Inquiry Card

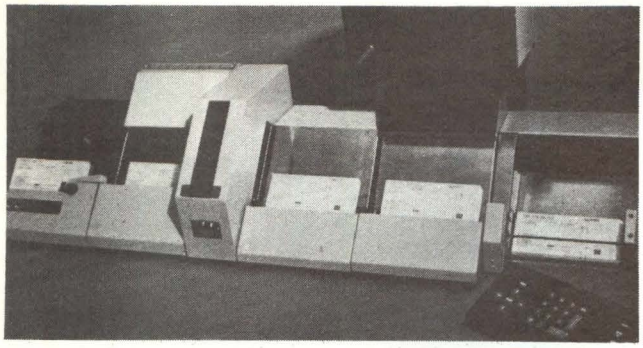
16-BIT, TRACKING S-D CONVERTER

Model 1661, a high accuracy, 1 min, S-D tracking converter, is an ultra stable device that incorporates transformer isolation and is pin programmable for either synchro or resolver inputs. Type 2 servo loop processing techniques assure error free data at tracking rates up to 720 °/s. An MTBF of >80,000 h minimum coupled with small size [3.125 x 3.465 x 0.82″ (7.938 x 8.8 x 2.08 cm)], and wide temp capability qualifies units for exacting conversion requirements. **Transmagnetics, Inc,** 210 Adams Blvd, Farmingdale, NY 11735.
Circle 273 on Inquiry Card

TIME CLOCK REPLACEMENT SYSTEM

By combining microprocessor based Time-2000 processing unit with a number of punched badge reading terminals, system allows 1 employee badge entry to eliminate up to 18 manual steps and associated human errors involved with conventional manual systems. System optically reads a punched employee badge number and records data onto a minidiskette in processing unit, which is equipped with CRT and alphanumeric keyboard. The system's processing unit offers std BASIC programming. **Panasonic,** One Panasonic Way, Secaucus, NJ 07094.
Circle 274 on Inquiry Card

OCR DOCUMENT READER



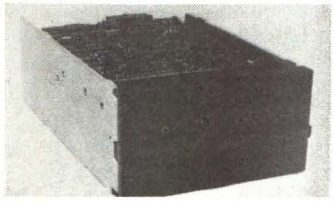
The Interactive Document Processor (IDP) consists of reader, feeder, 2 viewing stations, keyboard, and interface. Not limited to RS-232-C, the unit can interface with all common data processing systems with no hardware or software modifications in the host computer, eliminating conversion effort necessary to interface OCR document readers with existing equipment. In credit card slip processing, the unit reads and enters account numbers, halving the number of keystrokes and processing time. Where numerals are unrecognizable to the reader, an integral display unit mounted on the viewing station is triggered, automatically positioning the cursor under the questionable space on the display for manual entry from the keyboard. Rejection rate is <1 in 10k char. **Digitron,** 500 Fifth Ave, New York, NY 10036.
Circle 275 on Inquiry Card

INTELLIGENT FLOPPY DISC CONTROLLER

A controller with standalone, offline operational capability, IFC-8400 controls up to 8 Shugart SA400 or SA800 single-sided, single-density flexible disc drives. It interfaces to any computer or standalone terminal over an RS-232-C or 20-mA current loop serial channel or optional parallel 8-bit TTL I/O channels. An integral file-based operating system allows the controller to create, delete, or edit files, and fulfill other controller functions offline from the computer. The onboard diskette operating system (DOS) is operational when power is turned on. Its high level ASCII commands consist of printable ASCII character strings that allow operation with almost any device containing an ASCII keyboard and serial or parallel interfaces. **Cybernetic Micro Systems,** 2378A Walsh Ave, Santa Clara, CA 95050.
Circle 276 on Inquiry Card

DOUBLE-HEADED FLOPPY DISC DRIVE

FD650, a standard 8″ (20.3-cm) drive capable of recording and reading data on both sides of an IBM (or equivalent) Diskette 2 or 2D, also offers double-density recording using MFM encoding to provide an immediately addressable unformatted storage capacity of 1.6M bytes. Electronically compatible with the proposed ANSI standard, each drive is equipped with a door lock, and has die-cast construction. All electronics are on a single PC board. Track to track access time is 3 ms; head load time is 35 ms; and track settling time is 15 ms. Up to 8 drives can be daisy-chained. Head positioning is achieved by a steel band attached to the head carriage and to a drive pulley on the shaft of a 4-phase 1.8° permanent magnet stepper motor. Each step of the motor causes the head to move 1 track. **Pertec Computer Corp, Pertec Div,** 9600 Irondale Ave, Chatsworth, CA 91311.



Circle 277 on Inquiry Card

SYNCHRONOUS INTERFACE MODULE

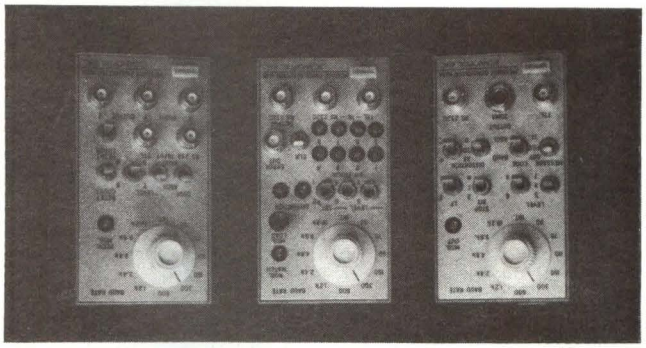
Intended for use in synchronous communications between S-100 computers and large-scale computers, modems, data encryption devices, or other S-100 computers, 88-SAI provides a synchronous or asynchronous port for any S-100 bus processor, and allows baud rate, word size, parity, and number of stop bits to be selected completely under software control. Also under software control are synchronous/asynchronous mode selection and functions associated with synchronous communications such as number of sync characters. Fully compatible with RS-232-C interfaces, unit includes provision for interface to nonstandard devices requiring inversion of various signal or handshake lines, and interfaces to MIL-STD-188 level devices. **International Data Systems, Inc,** 400 N Washington St, Suite 200, Falls Church, VA 22046.
Circle 278 on Inquiry Card

SHOP FLOOR INPUT TERMINAL

SDA-706MP is a rugged, benchmounted workstation designed for location in production work areas. Terminal has a combination optical card/badge reader which will read both std 3.250″ (8.255-cm) wide Hollerith cards and badges interchangeably. Any number of cards or badges may be read one at a time within a single transaction under software control. Variable data are entered through a 10-key numeric keyboard; fixed data either by numeric badge or Hollerith-punched tab cards. Unit provides a 16-digit alphanumeric display, 10 function keys, and system status indicators. Alphanumeric display assists operator in formatting and editing data entered at keyboard and displays responses to operator inquiries. **Sierra Research Corp, Data Systems Div,** PO Box 222, Buffalo, NY 14225.

Circle 279 on Inquiry Card

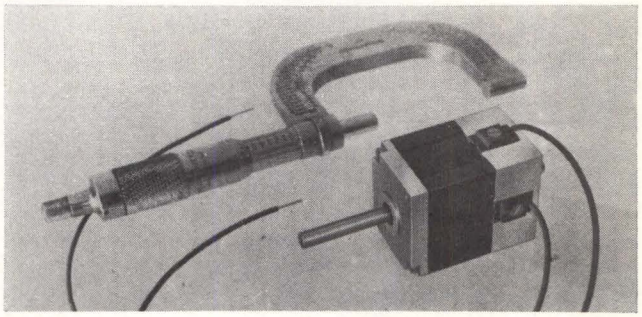
DATA COMMUNICATION TEST INSTRUMENTS



For use as a system, singularly or in combination, the 1024 Fox generator, 1026 error detector, and 1028 formatter are compatible with Tektronix TM-500 systems. Generator outputs a std "Quick Brown Fox" message as reference source for testing systems with serial asynchronous data input capability. Output may be switched to ASCII or Baudot, 5 through 8 levels. Output circuits are TTL, RS-232-C, or 20-mA loop. Error detector stores reference message read out from system under test, and continually compares it with further messages read out of the system, displaying differences or errors on front panel LEDs. Formatter inputs serial asynchronous data and displays it as alphanumeric chars on a std oscilloscope. All units have front panel baud rate adjustments at std values from 50 to 19.2k baud. **Scanoptik Inc,** PO Box 1745, Rockville, MD 20850.
Circle 280 on Inquiry Card

PRODUCTS

RARE EARTH FIELD DC MOTORS

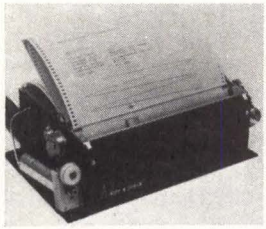


With theoretical accelerations of >75,000 radians/s², Series 7000 incorporates 4-pole samarium-cobalt fields with skewed 13-slot armatures. Designed to provide high output, small size, and low mass, as well as ability to drive low inertial loads in start-stop cycling as rapidly as 60 times/s, the motor combines the benefits of high coercivity and good magnetic induction at reasonable costs. With armature windings chosen to provide no load speeds of about 4000 r/min, the motors have peak torque (stall) values ranging from 12 to 20 oz-in (0.08 to 0.14 N•m) depending on length. All have a cross-section of 1.00 x 1.25" (2.54 x 3.175 cm) with lengths of 1.58, 1.69, and 1.80" (4.013, 4.293, and 4.572 cm). **The Paradyne Corp,** 8550 Ulmerton Rd, Largo, FL 33541.
Circle 281 on Inquiry Card

ENTRY LEVEL DATA COMMUNICATIONS SYSTEM

LCP allows IBM 360/370 users to implement a sophisticated yet affordable data communications system in low volume remote applications. System provides means of extending the multiplexer channel interface of mainframe to remote locations without mainframe-resident communications software such as BTAM, QTAM, or RJE. Consisting of control unit attached to byte multiplexer channel of the mainframe, either half- or full-duplex lines modules which allow CPU to CPU links, and remote control units, which can support card readers, reader/punches, and line printers at speeds to 1100 lines/min, system uses either digital network links or voice-grade lines and supports data rates from 4800 to 19.2k bits/s. **Paradyne Corp,** 8550 Ulmerton Rd, Largo, FL 33541.
Circle 282 on Inquiry Card

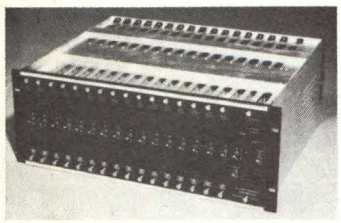
PRINTING RECORDER



BD-50 records both analog signals and alphanumeric data on the same chart by means of a flying thermal writing head that can be switched over from analog to digital mode by a switch or voltage on a control line. Thus, when attached to microprocessor equipped instrumentation, both analog signal and microprocessor derived results can be displayed. The flying head has a row of 10 dots; analog recording uses 1 dot, 7 dots are used for alphanumeric printing, giving characters in a 5 x 7 matrix. Interface connections are provided for CCITT V.24 (ANSI RS-232-C), 20-mA loops, IEEE-488 or IEC 66.22 inputs. Pen response is 0.1-s full-scale deflection; and printing speed is 15 char/s. **Kipp & Zonen,** 390 Central Ave, Bohemia, NY 11716.
Circle 283 on Inquiry Card

COMMUNICATIONS LINE SWITCHING SYSTEM

RCS-100 remote control switch performs fallback switching and line routing, and can be controlled manually or electronically from either local or remote locations. Unit operates through a self-contained microprocessor which can be controlled through panel switches or RP-1 remote control panel, from data terminal or CPU, or from std telephone equipped with Touch-Tone dialing. Software for the microprocessor can provide a variety of switching functions for any given control entry, plus alarm and status functions. System security can be maintained through use of access and security codes controlled only by the user. Interchangeable plug-in modules can accommodate 4-, 6-, 9-, or 25-wire (EIA RS-232) circuits. **Atlantic Research Corp,** 5390 Cherokee Ave, Alexandria, VA 22314.



Circle 284 on Inquiry Card

DUAL LED COAXIAL FIBER OPTIC SCANNER

The S27101 Micro-Skan is able to detect a 0.010″ (0.254-mm) target within an operational range of 0.005 to 0.200″ (0.127 to 5.00 mm) from scanner to target with repeatability of ±0.001″ (0.025 mm). Unit consists of two IR LEDs, silicon phototransistor, focusing lens, and glass fiber optic rod housed in a TO-18 type plated steel can. IR energy from the LEDs is transmitted through the formed plastic lens to the target; it is then reflected from the target's surface back through the fiber optic rod at the lens center to the phototransistor. Coaxial construction gives unit a small field of view which is not rotationally oriented. Device may be clamped or soldered to a circuit board or plugged into a mating receptacle with cable leads. **Skan-A-Matic Corp,** PO Box S, Rt 5 W, Elbridge, NY 13060.

Circle 285 on Inquiry Card

PROGRAMMABLE KEYBOARD FOR SMART TERMINALS

Microprocessor based keyboard has 106 keys standard with additional keys available for expanded features, and is interchangeable with keyboards previously used on D300 and D400 terminals. Several arrangements are available for the terminals, and special arrangements can be provided. Special key-cap engraving is also available. Keyboard offers operator comfort through its stepped arrangement and positive response click to the operator with each key depression. It enhances the editing data entry position of the terminals and allows users to design their keyboard to specific industry application. Options include adjustable brightness control for the video display and adjustable electronic click on depression of any key. **EECO, Computer Terminal Products Group,** 1441 E Chestnut Ave, Santa Ana, CA 92571.

Circle 286 on Inquiry Card

PRODUCTS

FLOPPY DISC SYSTEM FOR MILITARY SOFTWARE DEVELOPMENT

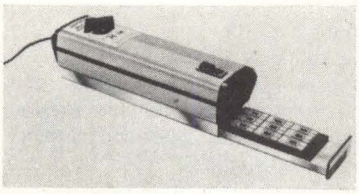
Model 3383 may be used with, or instead of, a moving head disc in the company's programming station packages, with diskettes providing the medium for software operating system, user data, and user application program. The 3300 combination I/O terminal interface replaces 5 individual modules providing for attachment of 4 external devices to the station and offering a built-in realtime clock feature. Realtime disc-based operating system (RDOS) provides system developer with the ability to begin development of algorithms immediately. System consists of a 3382 floppy disc interface module and an AED 6200P floppy disc subsystem that includes formatter and drive electronics for up to 4 model 3384 drives. A single diskette stores up to 12,500 lines of code, equal to 313,396 16-bit words of information. **ROLM Corp,** 4900 Old Ironsides Dr, Santa Clara, CA 95050.
Circle 287 on Inquiry Card

PRINTER/PLOTTER I/O MULTIPLEXERS

Offering I/O switching among multiple computers and the company's output units, crossbar switching, and optional long line extension, the 511 output multiplexer drives any 2 electrostatic printers, plotters, or printer/plotters from a single computer controller or parallel data source, such as a display controller. Multiple output units can share a common interface address, and can be driven independently or simultaneously. The 512 input multiplexer allows 2 computers or parallel data sources to share a single output unit. Used together as a crossbar switcher, units multiplex both inputs and outputs. Either multiplexer can include an optional long line repeater to extend the distance between data source and output device up to 1000' (305 m). **Versatec,** 2805 Bowers Ave, Santa Clara, CA 95051.
Circle 288 on Inquiry Card

EPROM-ERASING UV LAMPS

Spectroline PE-24T will erase up to 9 chips in as little as 12 min. Double-tube construction and specially-designed specular reflector provide broad, intense, uniform UV distribution. The lamp's 2 high intensity UV tubes are fully shielded within an anodized aluminum housing; a safety interlock prevents the unit from operating when the tray is not fully inserted. A conductive foam pad holds the chips in place during exposure and prevents electrostatic build-up, while protecting the chips from possible static charge. A 60-min timer is included for automatic shut-off of the unit. A small, low cost UV lamp, PE-14 is designed especially for the small systems user; -14T also has a 60-min timer. Both lamps erase up to 6 EPROMs in 14 min. **Spectronics Corp,** 956 Brush Hollow Rd, Westbury, NY 11590.



Circle 289 on Inquiry Card

LITERATURE

Power Supplies/Solid-State Loads

Performance characteristics, block diagrams, features, and common specs are outlined in catalog including open frame, ferroresonant, ac-dc and dc-dc encapsulated power supplies, and programmable solid-state loads. **Acme Electric Corp,** Cuba, NY.
Circle 300 on Inquiry Card

Remote Information Systems

Descriptions of components, software, and configurations of multifunction remote information systems, which perform batch communications, data entry, and standalone processing, based on the model 85 processor, appear in brochure. **Data 100 Corp,** Minneapolis, Minn.
Circle 301 on Inquiry Card

Stepping Motor Controls

Catalog provides charts, specs, speed vs torque curves, and connection diagrams on translator and preset indexer modules, power supply modules, open chassis and buffered translators, and open chassis preset indexers. **The Superior Electric Co,** Bristol, Conn.
Circle 302 on Inquiry Card

Connectors/Interconnection Devices

Catalog including features, photos, and electrical and mechanical specs covers flat cable connector systems, ribbon and subminiature connectors, and a range of std connector types. **TRW Cinch Connectors, an Electronic Components Div of TRW, Inc,** Elk Grove Village, Ill.
Circle 303 on Inquiry Card

Automatic Data Network Testing

EMS-one fully automated event management system operates in 4 modes for unattended monitoring and diagnostics of data communications networks, enabling 49 specific tests as described in brochure. **Intertel, Inc,** Burlington, Mass.
Circle 304 on Inquiry Card

Data Communications Test Sets

Listing typical applications, illustrated 8-p brochure discusses distortion measuring sets, test message generators, and data quality analyzers, all designed to exercise terminals, test modems, and transmission facilities. **Atlantic Research Corp, Teleproducts Div,** Alexandria, Va.
Circle 305 on Inquiry Card

Programmable Controller

Spec brochure includes programming examples, installation drawings, and detailed descriptions of all hardware of System 2 controller, which handles operation of up to 8 separate sequential processes with up to 99 timed steps for each program. **Versatyme Controls Corp,** Santa Clara, Calif.
Circle 306 on Inquiry Card

Subminiature Filters

Including information on regulatory agencies and emi prevention methods, ferrite filters, and considerations for digital circuits, handbook is directed at application of Quiet Line low pass subminiature filters. **AMP Inc, Capitron Div,** Elizabethtown, Pa.
Circle 307 on Inquiry Card

Power Supplies

Typ applications of switching power supplies in CRT, electromechanical, microprocessor based, and large multiple supply systems are presented in brochure on 25- to 400-W power supplies. **Boschert Inc,** Sunnyvale, Calif.
Circle 308 on Inquiry Card

Clutches/Brakes/Screws

Catalog and application/engineering selection guide provides details on power transmission and motion control products including clutches, brakes, power supplies, and ball bearing screws. **Warner Electric Brake & Clutch Co,** Beloit, Wis.
Circle 309 on Inquiry Card

Logic Analyzer Troubleshooting

Application note, using detailed diagrams and scope CRT photos, presents a problem-equipment solution approach to troubleshooting microprocessor based systems utilizing the 1650-D logic analyzer, 116 display control accessory, and 10-TC probe pods. **Gould Inc, Biomation Div,** Santa Clara, Calif.
Circle 310 on Inquiry Card

Applications Software Diskettes

Newsletter announcing 8 application software diskettes and over 50 application programs for HORIZON computer and MICRO DISC SYSTEM, along with 16-p product guide, is offered. **North Star Computers, Inc,** Berkeley, Calif.
Circle 311 on Inquiry Card

Data Modems

Brochure describes features, options, controls, and diagnostic functions of line of LSI point-to-point, multipoint, and international high speed data modems. **Codex Corp,** Newton, Mass.
Circle 312 on Inquiry Card

Line Conditioners and Transformers

Catalog discusses power line problems and provides applications data, block and installation diagrams, and detailed specs on high speed ac line conditioners, uninterruptible power systems, high isolation transformers, ac power sources, frequency converters, and inverters. **Elgar Corp,** San Diego, Calif.
Circle 313 on Inquiry Card

Logic and I/O Modules

Catalog lists accessories, module descriptions, specs, and typ logic elementary drawings for M series logic and I/O modules, with noise immunity for harsh environments. **Dynage, Inc,** Bloomfield, Conn.
Circle 314 on Inquiry Card

Synchro/Data Converters

Brochure includes descriptions of hybrid synchro converter modules, A-D converters, fixed reference and multiplying D-A converters, sample/hold amps, and many synchro products in discrete and hybrid form. **ILC Data Device Corp,** Bohemia, NY.
Circle 315 on Inquiry Card

Electronic Components

Covering full line of A-B attenuators, fixed resistors, potentiometers, resistor networks, and trimmers, 208-p softcover book supplements text with photos, dimensional drawings, tables, and specs. **Allen-Bradley Co,** Milwaukee, Wis.
Circle 316 on Inquiry Card

Technical Terms/Symbols

Publication No. 77-B, "JEDEC (Joint Electron Device Engineering Council) Recommendations for Letter Symbols, Abbreviations, Terms, and Definitions for Semiconductor Device Data Sheets and Specifications," covers technical terms and symbols for semiconductor devices as used in JEDEC registration data formats. Price is $13.50. **Standards Sales Office, Electronic Industries Assoc,** 2001 Eye St NW, Washington, DC 20006.

LITERATURE

Wire, Cable, and Conduit

Featuring illustrations, specs, and applications information, 4-p catalog covers INTER-8 WEAVE cable for reduced pickup and radiation of mag fields, CO-NETIC AA wire used in high permeability mag shielding braid over cables, and SPIRA-SHIELD conduit for magnetically shielding cables. **Perfection Mica Co, Magnetic Shield Div,** Bensenville, Ill.
Circle 317 on Inquiry Card

Signal Conditioning Instruments

Mounting diagrams, specs, and photos are given in booklet on 3000 series signal conditioners and digital indicators for electromechanical measurements. **Daytronic Corp,** Miamisburg, Ohio.
Circle 318 on Inquiry Card

Micro/Minicomputer Regulators

Illustrated brochure offers dimensional drawings and basic specs for line of portable, plug-in regulators with load ratings of 140 and 250 VA. **Sola Electric Co,** Elk Grove Village, Ill.
Circle 319 on Inquiry Card

Handheld Terminals

Connector data, specs, photos, and an ASCII code chart point out characteristics of five models of handheld terminals which have 128-char ASCII capability and RS-232-C or current loop interfaces. **Termiflex Corp,** Nashua, NH.
Circle 320 on Inquiry Card

Microcomputers

Components of the MMD-1 Mini-Micro Designer®, part of an integrated educational and development system, are discussed in 16-p catalog along with memory/interfacing information. **E&L Instruments, Inc,** Derby, Conn.
Circle 321 on Inquiry Card

Monitor/Alarm/Control System

Comprised of descriptions, photos, and specs, brochure profiles Autodata Nine system capable of 18-dB common mode rejection and remote scanning up to 5000 ft (1500 m). **Acurex Autodata, Inc,** Mountain View, Calif.
Circle 322 on Inquiry Card

PC Connectors

By giving characteristics, part number breakdowns, and contact termination diagrams, catalog discusses dip solder, wire-wrap, and round tail connectors with contact centers from 0.050 to 0.156" (0.13 to 0.396 cm). **Viking Industries, Inc,** Chatsworth, Calif.
Circle 323 on Inquiry Card

Control Motors

Servo, stepper, inertially damped, and hysteresis synchronous motors with integral tachometers and gearheads in frame sizes ranging from 0.5 to 2.25" (1.27 to 5.72-cm) dia are detailed in 48-p catalog through electrical and mechanical specs. **Vernitech Corp,** Deer Park, NY.
Circle 324 on Inquiry Card

Linear Actuators

Bulletin CM825 furnishes typ specs, charts showing linear force vs linear rate, switching circuits and unipolar drive tables, and outline and marking dimensions of a 12-Vdc, 1.5-oz (42-g), digitally controlled linear actuator. **North American Philips Controls Corp,** Cheshire, Conn.
Circle 325 on Inquiry Card

Data Acquisition PC Boards

Brochure supplies electrical and mechanical parameters and programming considerations on SineTrac 6800 series data acquisition PC boards as well as block diagrams, details on A-D/D-A base addressing, and channel expansion. **Datel Systems, Inc,** Canton, Mass.
Circle 326 on Inquiry Card

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

GUIDE TO PRODUCT INFORMATION

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ADVERTISERS' INDEX

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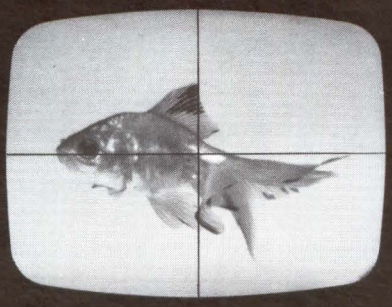

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