JULY 1980

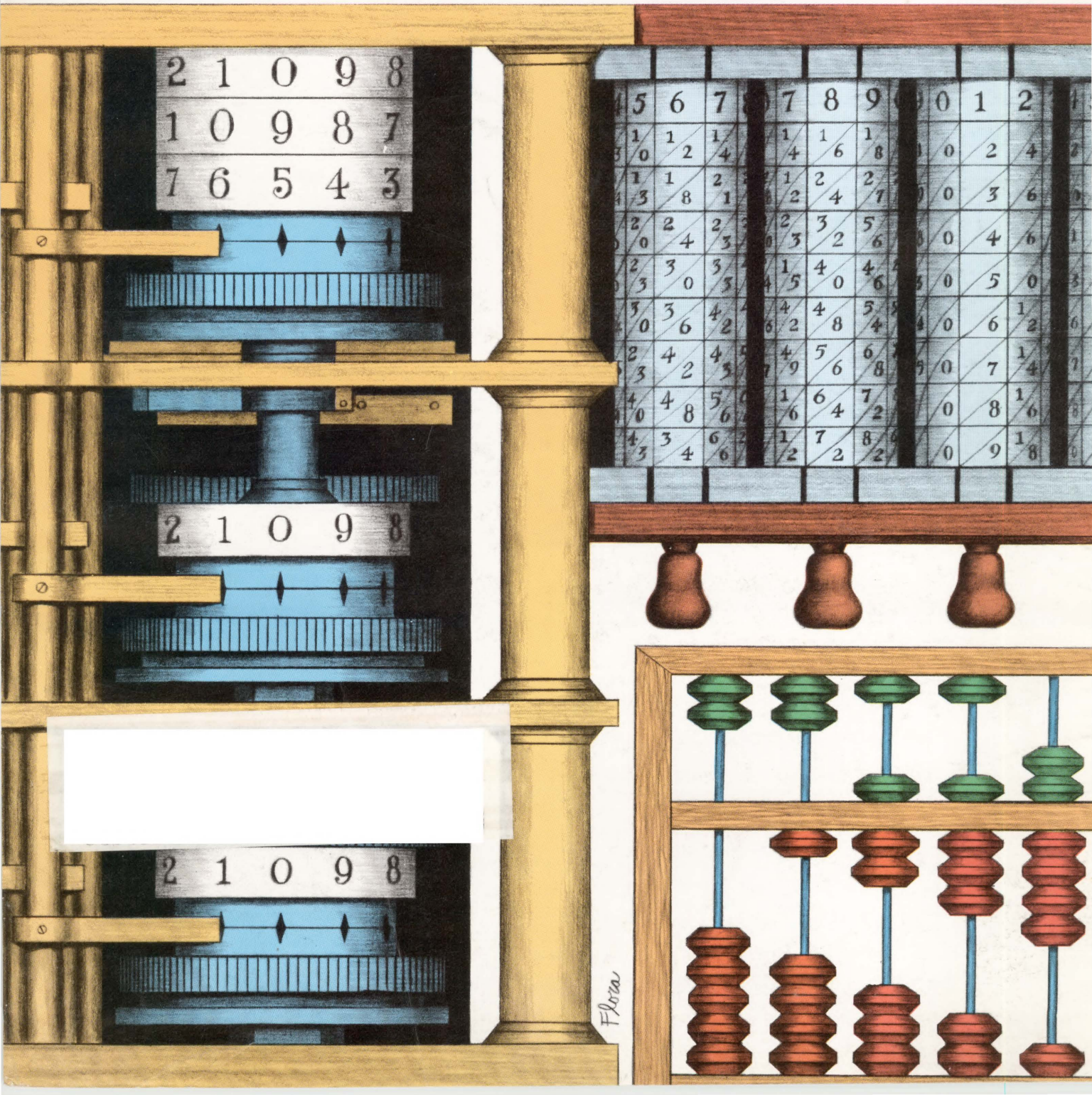
# COMPUTER DESIGN

**THE** MAGAZINE OF COMPUTER-BASED SYSTEMS

ARITHMETIC PROCESSOR CHIPS ENHANCE MICROPROCESSOR PERFORMANCE

DATA DRIVEN SYSTEM FOR HIGH SPEED PARALLEL COMPUTING — PART 2: HARDWARE DESIGN

BIT MAP ARCHITECTURE REALIZES RASTER DISPLAY POTENTIAL



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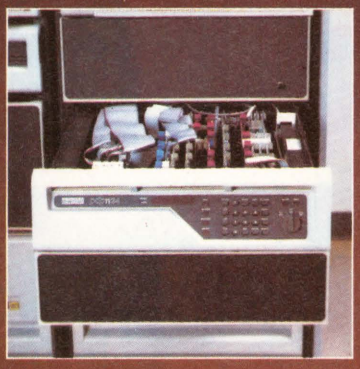

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**CIRCLE 2 ON INQUIRY CARD**

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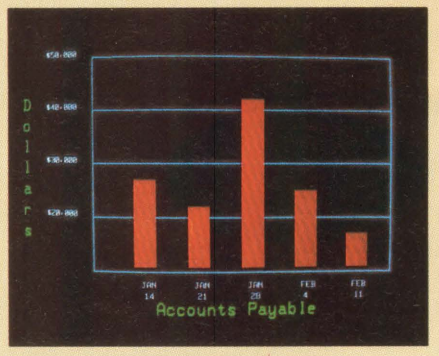
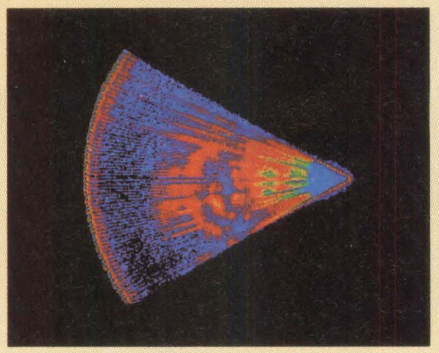



Management Information Display



Ultrasonic heart sector scan

High-resolution display with alphanumerics

# Get the professional color display that has BASIC/FORTRAN simplicity

## LOW-PRICED, TOO

Here's a color display that has everything: professional-level resolution, enormous color range, easy software, NTSC conformance, and low price.

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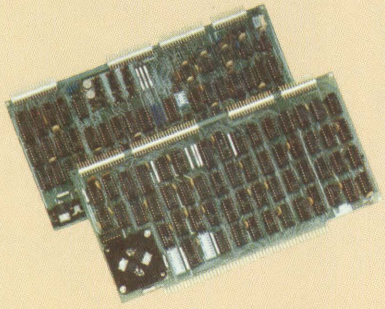
*U.S. Pat. No. 4121283



Model SDI High-Resolution Color Graphics Interface

## HIGH RESOLUTION

The SDI's high resolution gives a professional-quality display that strictly meets NTSC requirements. You get 756 pixels on every visible line of the NTSC standard display of 482 image lines. Vertical line spacing is 1 pixel.

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Model SDI plugs into Z-2H 11-megabyte hard disk computer or any Cromemco computer

## DISPLAY MEMORY

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## CONTACT YOUR REP NOW

The Model SDI has been used in scientific work, engineering, business, TV, color graphics, and other areas. It's a good example of how Cromemco keeps computers in the field up to date, since it turns any Cromemco computer into an up-to-date color display computer.

The SDI has still more features that you should be informed about. So contact your Cromemco representative now and see all that the SDI will do for you.

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CIRCLE 3 ON INQUIRY CARD

COMPUTER DESIGN THE MAGAZINE OF COMPUTER-BASED SYSTEMS

VOLUME 19, NUMBER 7 JULY 1980

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**by Stan Groves**

Careful attention to the relationship between access time and clock rate guarantees optimal throughput in a microprocessor system by tuning system parameters to make best use of the memories and supporting logic

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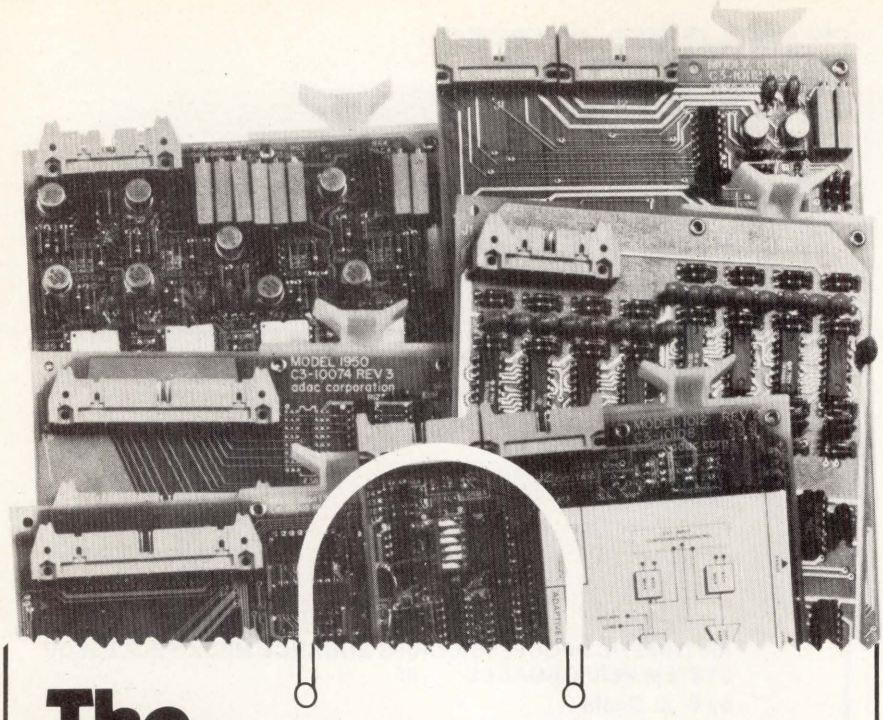


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| **1616/MIC** | 16 discrete inputs with priority encoder |
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| **1616/OII** | 16 parallel inputs, optically isolated, can cause interrupt |
| **1620TTL** | 16 latched inputs and outputs for DMA operation |
| **1616HCO** | 16 discrete outputs, high current drive |
| **1632HCO** | 32 discrete outputs, high current drive |
| **1632TTL** | 32 TTL I/O lines |
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**BUS INTERFACE**

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| **1620DMA** | Direct memory access controller |
| **1900** | Unibus to LSI-II translator |
| **1950** | Bus repeater |
| **1900CT** | Cable terminator card |

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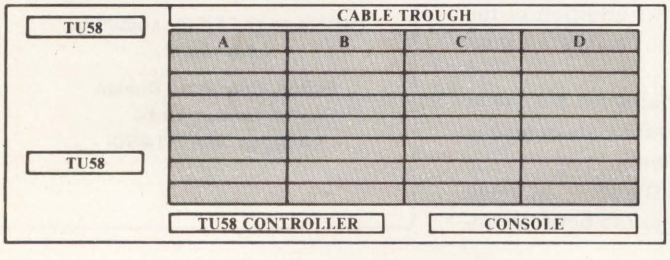


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CIRCLE 5 ON INQUIRY CARD

# LETTERS TO THE EDITOR

To the Editor:

I just received the April 1980 issue of *Computer Design* at work today and find the article entitled "Interfacing Fundamentals: Conditional I/O Using a Semaphore," pp 166-167, by Peter R. Rony, to be in need of several comments and corrections.

First, the statement in the last sentence of the second paragraph is inconsistent with the prior discussion and Fig 1 and is incorrect. Indeed, if the operation were as described by the sentence, the system would have two infinite loops! The sentence should interchange the "sensed high" and "sensed low" conditions: "For example, as long as the semaphore is sensed low [high] by the source, no new data can be provided to the buffer; while the semaphore is sensed high [low] by the acceptor, this acceptor cannot acquire new data from the buffer."

Second, the sequence of operations for an input device given in the third paragraph and Fig 2 is certain to cause problems. In step 2, the semaphore is set high, indicating that data are available; then in step 3, the data are transferred to the buffer. The data are thus indicated as being available *prior* to their *actual* availability. Steps 2 and 3 should be interchanged. In an attempt to circumvent the problems, step 5 includes a time delay, but leaves this delay unspecified. The changed sequence of operations could be implemented in hardware by clocking the data buffer from STB X rather than $\overline{\text{STB X}}$.

Third, the discussion of Fig 3 and the figure itself are only obfuscated by the unnecessary inclusion of the complementary output of the semaphore; the article could be improved by its omission. Also, the setting of the semaphore to indicate data availability should be delayed slightly, relative to the transfer of the data to the buffer, to allow for settling time of the buffer and deskew of the parallel word.

Last, the concept of setting and clearing a flipflop to control the transfer of data to a peripheral device is well known. For example, the basic concept of the subject of this article is discussed in Bartee, Lebow, and Reed, *Theory and Design of Digital Machines,* New York: McGraw-Hill, 1962, pp 220-222.

Robert H. French
District Heights, Md

*The Author Replies:*

Robert H. French is correct when he suggests exchanging "low" and "high" in the last sentence of the second paragraph in order to make the text consistent with Figs 1, 2, and 3. The sequence of events shown in Fig 2—and thus the sequence of events in paragraph 2 and the flowchart in Fig 1—were based upon the strobed input mode for the 8155/8156 and 8255 integrated circuits, as provided on pp 9-75 and 11-62, respectively, of the 1979 Intel Component Data Catalog. The strobed input timing could be implemented in the alternative manner suggested by French.

The sequence of events shown in Fig 3 was based upon the strobed output mode for the 8155/8156 and 8255 integrated circuits. For the DATA ACCEPTED state, the semaphore output from the 8155/8156 is a logic 1, whereas from the 8255 it is a logic 0. The two pin functions are listed as BF and OBF, respectively. Thus, the addition of the complementary output serves a useful purpose.

No claim of originality for the use of a flipflop to synchronize data transfers was made in the column. A systematic discussion of the differences between semaphores and flags, and between unconditional and conditional I/O, is appropriate in a column on interfacing fundamentals.

Peter R. Rony
Virginia Polytechnic Institute
Blacksburg, Va

---

To the Editor:

Your articles and ads on CRT terminals show that much more effort goes into the design of the electronic part of the keyboard than the keyboard itself. All of the designs that I have seen do not take the user into consideration. For instance, the carriage return is the second most used key after the space bar and should therefore be a large target; yet it is usually small and placed next to "disaster" keys. A suggested target would be two keys high and two keys wide. This would eliminate the error message (ie, TERMINAL ERROR, REENTER INPUT). Another problem is that "critical" keys are next to each other, causing the computer to "go bananas" whenever two keys are hit together. The solution is simple: put noncritical keys next to critical keys.

It seems to me that keyboard designers could do some "HUMAN" engineering to improve their product.

Urban Ludwig
Goddard Space Flight Center
Greenbelt, Md

**Letters to the Editor should be addressed:**

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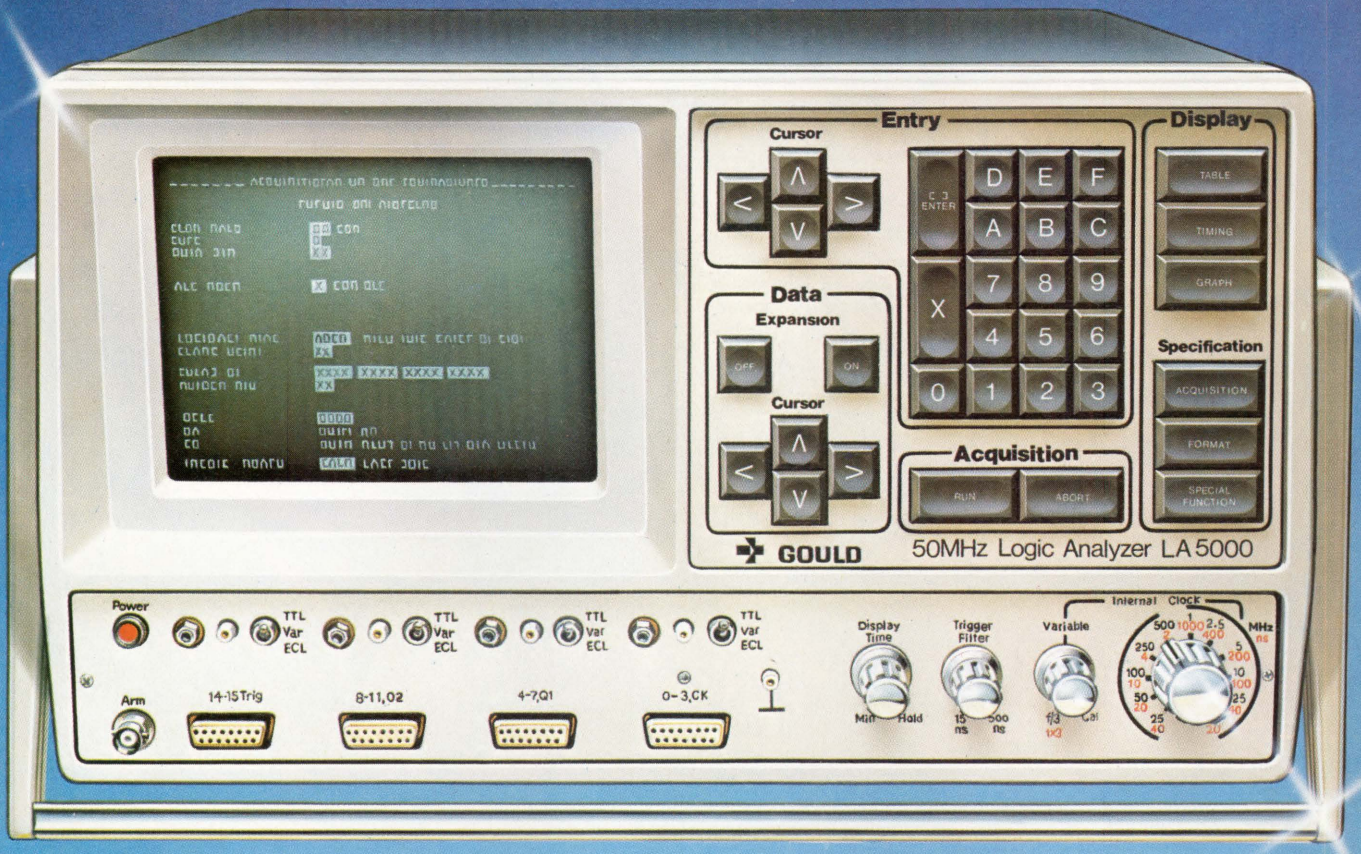
# MICROPROCESSOR GLITCHES: MEET YOUR FIXER.

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CIRCLE 6 ON INQUIRY CARD

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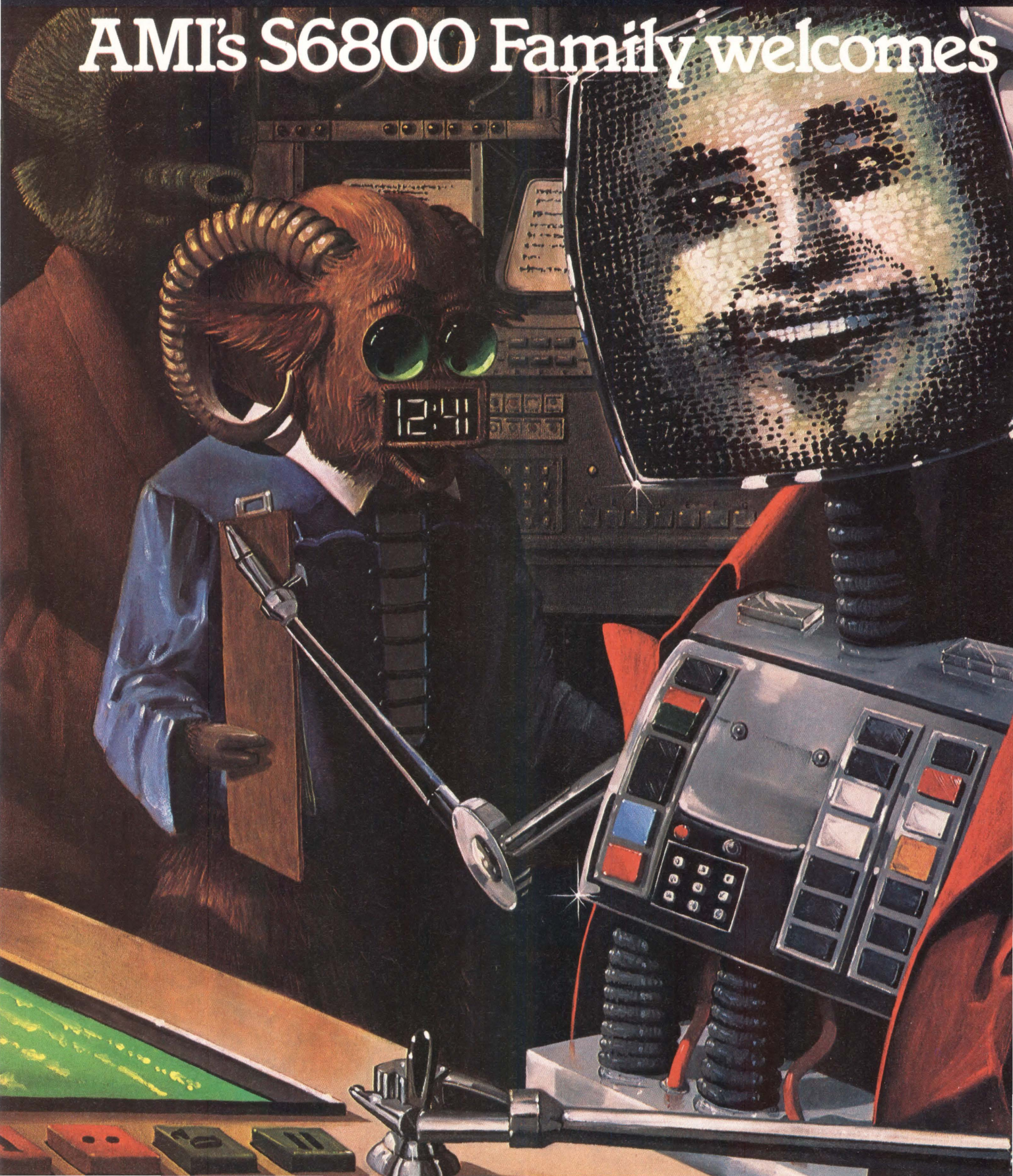
So give your MPU complete



mastery over its CRT with our lean, efficient controller. Check your nearest AMI distributor for details. Or get in touch with us at AMI S6800 Marketing, 3800 Homestead Road, Santa Clara CA 95051. Phone (408) 246-0330.

This is one new interface with real star quality.

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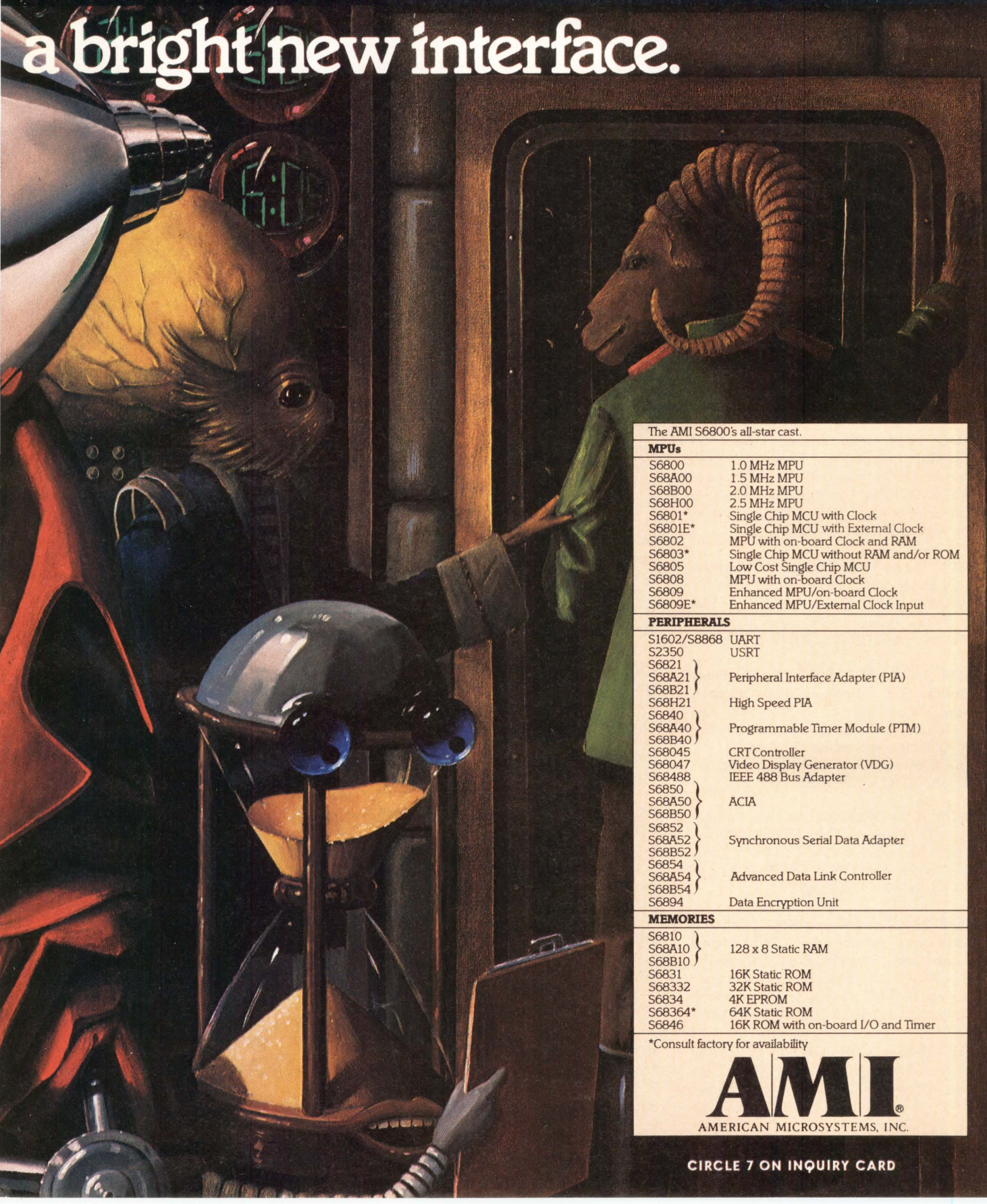

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## CONFERENCES

**AUG 12-15—1980 Joint Automatic Control Conf,** Sheraton-Palace Hotel, San Francisco, Calif. INFORMATION: David Hullender, Dept of Mechanical Engineering, U of Texas at Arlington, Arlington, TX 76019. Tel: 817/273-2561

**AUG 18-21—Nat'l Conf on Artificial Intelligence,** Stanford U, Stanford, Calif. INFORMATION: American Assoc for Artificial Intelligence, Stanford U, PO Box 3036, Stanford, CA 94305

**AUG 19—NECOM Show (New England Computer Show),** Marriott Hotel, Newton, Mass. INFORMATION: Norm De Nardi, Norm De Nardi Enterprises, 95 Main St, Los Altos, CA 94022. Tel: 415/941-8440

**AUG 26-29—1980 Internat'l Conf on Parallel Processing,** Boyne Highlands Convention Ctr, near Harbor Springs, Mich. INFORMATION: Kay Garringer, Dept of Computer Science, Wright State U, Dayton, OH 45435. Tel: 513/873-2491

**SEPT 3-12—1980 Internat'l Machine Tool Show,** McCormick Place, Chicago, Ill. INFORMATION: National Machine Tool Builders' Assoc, 7901 Westpark Dr, McLean, VA 22102. Tel: 703/893-2900

**SEPT 16-18—FOC '80 (Internat'l Fiber Optics and Communications Exposition),** Hyatt Regency Embarcadero, San Francisco, Calif. INFORMATION: Michael A. O'Bryant, Information Gatekeepers, Inc, 167 Corey Rd, Suite 111, Brookline, MA 02146. Tel: 617/739-2022

**SEPT 16-18—WESCON,** Anaheim Convention Ctr, Anaheim, Calif. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

**SEPT 22-25—Software INFO (National Software Package Conf and Exposition),** Hyatt Regency, Chicago, Ill. INFORMATION: Professional Exposition Management Co, Suite 545, 222 W Adams St, Chicago, IL 60606. Tel: 312/263-3131

**SEPT 23-25—COMPCON Fall '80,** Capital Hilton, Washington, DC. INFORMATION: Harry Hayman, COMPCON 80 Fall, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

**OCT 1-3—Fault Tolerant Computing Systems,** Kyoto, Japan. INFORMATION: Prof John Meyer, Dept Elec and Computer Engineering, U of Michigan, Ann Arbor, MI 48109. Tel: 313/763-0037

**OCT 1-3—Internat'l Conf on Circuits and Computers for Large Scale Systems,** The Rye Town Hilton Inn, Port Chester, NY. INFORMATION: Dr NB Guy Rabbat, 32 Tor Rd, Wappingers Falls, NY 12590. Tel: 914/897-8126

**OCT 6-9 AND OCT 14-17—8th World Computer Congress,** Tokyo, Japan, and Melbourne, Australia. INFORMATION: AFIPS, 1815 N Lynn St, Suite 800, Arlington, VA 22209. Tel: 703/243-4100

**OCT 8-9—Connector Symposium,** Benjamin Franklin Hotel, Philadelphia, Pa. INFORMATION: Jim Pletcher, Electronic Connector Study Group, Inc, PO Box 167, Fort Washington, PA 19034. Tel: 717/780-8857

**OCT 13-15—Symposium on the Foundations of Computer Science,** Sheraton Inn, Syracuse, NY. INFORMATION: Prof Ronald V. Book, Dept of Math and Comp Science, U of California, Santa Barbara, CA 93106. Tel: 805/961-2778, 2171

**OCT 14-16—Mini/Micro Computer Conf and Exposition,** Civic Auditorium, San Francisco, Calif. INFORMATION: Robert D. Rankin, Mini/Micro Conference and Exposition, 32302 Camino Capistrano, Suite 202, San Juan Capistrano, CA 92675. Tel: 714/661-3301

**OCT 27-30—ICCC '80 (Internat'l Conf on Computer Communication),** Peachtree Plaza Hotel, Atlanta, Ga. INFORMATION: ICCC '80 Executive Committee, PO Box 280, Basking Ridge, NJ 07920. Tel: 201/221-8800

**OCT 28-30—Interface West,** Los Angeles Convention Ctr, Los Angeles, Calif. INFORMATION: Peter B. Young, The Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502

**NOV 6-12—Electronica '80,** Munich Fairgrounds, Munich, West Germany. INFORMATION: Franc D. Manzolillo, Rm 6015, U.S. Dept of Commerce, Washington, DC 20230. Tel: 202/377-2991

## SEMINARS

**AUG 3-5—Realtime Software for Micro/Minicomputer Systems AND AUG 6-8—Microcomputer Architecture Interfaces, Testing, Reliability, and System Design,** Hyatt Regency O'Hare, Chicago, Ill. INFORMATION: National Engineering Consortium, Inc, 1211 W 22nd St, Oak Brook, IL 60521. Tel: 312/325-5700

**AUG 4-6 AND SEPT 16-18—Charge-Coupled Devices,** Copley Plaza Hotel, Boston, Mass, and Sheraton Palace Hotel, San Francisco, Calif. INFORMATION: Leonard H. Klein, Palisades Institute, 201 Varick St, 9th Floor, New York, NY 10014. Tel: 212/620-3377

**AUG 14, 19, and 21; SEPT 9, 11, and 16; AND OCT 14—Information Resource Management,** various U.S. cities. INFORMATION: Market Information Office, Intel Commercial Systems Div, 12675 Research Blvd, PO Box 9968, Austin, TX 78766. Tel: 512/258-5171

**SEPT 18-19—Distributed Processing and Multiprocessing: Components and Applications; SEPT 29-30—Data Communications; AND SEPT 29-30—Microprocessors: Hardware, Software, and Applications,** Worcester Polytechnic Institute, Worcester, Mass, Worcester Polytechnic Institute, Worcester, Mass, and Sheraton Tara, Framingham, Mass. INFORMATION: Ginny Bazarian, Office of Continuing Professional Education, Worcester Polytechnic Institute, Worcester, MA 01609. Tel: 617/753-1411, X517

## SHORT COURSES

**SEPT 3-5—Logic and Microprocessor System Design,** The University of Liverpool Computer Laboratory, Liverpool, England. INFORMATION: The Secretary, Computer Laboratory, PO Box 147, Liverpool U, Liverpool L69 3BX, England

### NOTICE

*The Electronic Business Communications Conference and Exhibition previously scheduled for Sept 3-5 has been postponed until 1981. For details, contact John Sodolski, Electronic Industries Association, 2001 Eye St, NW, Washington, DC 20006. Tel: 202/457-4934*

# THE DSD 440. TOTAL DEC® RX02 COMPATIBILITY,

# AND MORE.

The DSD 440 is the only alternative to the DEC RX02 that's 100% software, hardware and media compatible with LSI-11, PDP®-11 and PDP-8 computers, including those with extended memory. It can be configured as an RX02 for DEC double density or IBM 3740 single density recording, or as an RX01 for backward operating system compatibility.

## MORE

A 512-byte hardware bootstrap is built into all PDP-11 and LSI-11 interfaces. It loads system software automatically from either single or double density diskettes. Extensive self-testing is DIP-switch selectable with the "Hyperdiagnostics" that run without being connected to a computer. The low profile 5¼-inch DSD 440 features write protection and diskette formatting.

## FASTER

The optimized DSD 440 microcode increases system throughput when using the RT-11 foreground/background monitor. In particular, the DSD 440 with an LSI-11 runs fill and empty buffer operations 20% faster than an RX02.

## FOR LESS

The DSD 440 is the RX02 compatible flexible disk system that combines high performance and advanced features with fast delivery... at a lower price. For further information, call or write Data Systems Design today. A data sheet and price list will be forwarded to you immediately.

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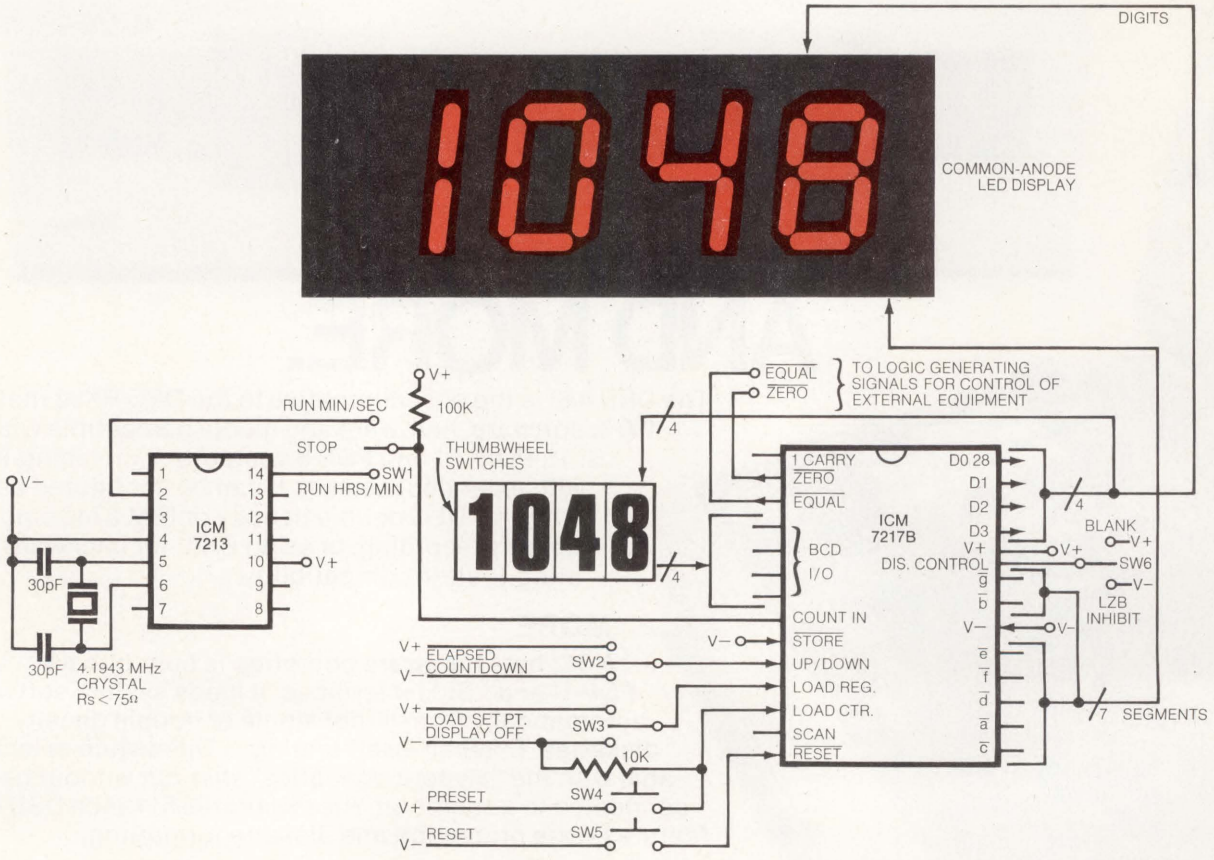
CIRCLE 8 ON INQUIRY CARD

# A MONOLITHIC 4-DIGIT THAT REPLACES UP

## THE ICM 7217/27

### Direct drive for up to 1" LED's




PRECISION ELAPSED TIMER OR COUNTDOWN TIMER

**ANOTHER FIRST FROM INTERSIL**

The ICM 7217/27 is the first family of 4-digit up/down counters that will directly drive large multiplexed LED displays. Common-anode or common-cathode. The common-anode devices typically drive 200 mA per digit, 40 mA per segment peak, for bright displays. Or for lower power and display cost, go common-cathode and use a calculator-type display. Either way, no external drivers or resistors are needed.

**FEATURES**

- On-chip direct drive to multiplexed 7-segment LED displays.
- Four-digit presettable up/down counter.
- Presettable register continuously compared to the counter.
- BCD input/output port, carry/borrow, zero, and equal outputs drive TTL directly.
- Leading Zero Blanking and Display Blank control provided.

# UP/DOWN COUNTER TO 20TTL PACKAGES

- Low power standby mode—300 $\mu$A typical with display off.
- Cascadable: 8, 12 or more digits in blocks of four.
- Counting speed: Guaranteed 0 to 2 MHz, typically 5 MHz.
- Single TTL—compatible 5V ±10% supply.

**TIME OR UNITS**
The ICM 7217/27 offers a decade count to 9999 or timing count of 5959. Time events. Count events or frequency. Set limits on the time or count. Cascade for more digits. Count can be continuously displayed, or display may be frozen while continuing to count. And, a Schmitt trigger on the count input allows accurate counting—even in noisy environments.

**$\mu$P BASED OR HARDWIRED**
The ICM 7217's are designed for hardwired, user-programmable applications, using thumbwheel switches for loading data and simple SPDT switches for chip control. The ICM 7227's are designed to interface to microprocessors where data input, output and chip control are directed by the processor.

**TRUE VERSATILITY**
We think the ICM 7217/27 will become the industry standard in applications such as: machine tool controllers, tachometers, hourmeters, limit set timers, speedometers, instrumentation, film projectors, $\mu$P controlled man/machine interfaces—in short, virtually anywhere versatile programmable up/down counting or timing must be displayed.

**LEADERSHIP IN CMOS**
The ICM 7217/27 is the latest in Intersil's series of MAXCMOS™ LSI devices incorporating direct drive for panel meter size LED displays. And, they offer levels of versatility and integration which can dramatically cut system costs. For example, the ICM 7217CIPI is only $6.10 in lots of 100.

**THE TIME IS NOW.**
For full information on the most versatile up/down counter/display drivers on the market, call your nearest Intersil Sales Office, Franchised Distributor, or return the coupon below.

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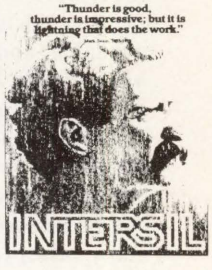


I'm counting on you.
____ Send me complete information on the ICM 7217/27 up/down counter/timer
____ Send me your Mark Twain poster

Name _____

Company _____

Address _____

City _____ State _____ Postal Code _____

# BROADBAND COAXIAL LOCAL AREA NETWORKS— PART 2: HARDWARE

**Mark A. Dineson**

Sytek, Inc, Northwest Engineering Laboratory

13333 NE Bellevue-Redmond Rd, Bellevue, WA 98005

Broadband media concepts are implemented primarily with off the shelf CATV hardware. Low cost signal splitters and taps achieve branching of cables, and commercial repeaters (line amplifiers) ensure adequate signal levels throughout the system. Mean time between failures for these devices has been established at 400k hours or better in large installations. Fully redundant repeaters are also available, and status monitoring equipment for these units has recently been introduced. All equipment is mass produced and highly reliable, thanks to the CATV industry.

Ease of maintenance is an attribute of the cable used in broadband coaxial networks. Should a cable be snapped, crushed, or otherwise seriously damaged, the entire service can be restored by the addition of one splice connector. In many cases, repair time is less than an hour, depending on the available technical control facilities.

In general, broadband network topology is not impacted heavily by the services provided in a single cable system. Conventional star, tree, and multiple hub topologies may be implemented, and the complexity of a broadband system topology can range from the very simple to the tremendously convoluted. However, the system can very often be implemented using only one cable. Unless specifically prohibited by analog gateway devices, all signals in a frequency division multiplex (FDM) system appear at each and every outlet. The simplest "gateway" device may be an analog filter, designed to channel portions of the spectrum to specific network areas.

Broadband designs encourage creativity and allow it to be realized to the greatest extent. Modems are available in many types and performance ranges for broadband systems. Basic units operate with RS-232 interfaces up to 9600 bits/s asynchronously, and may occupy from 100 to 400 kHz of spectrum. Synchronous modems are available in data rate ranges to 19.2k, 56k, and 512k bits/s.

Modems in the megabit range are available by special arrangement; their specifications depend on considerations of class of service, interface, and bandwidth. All units exhibit low error rates, ranging from $10^{-8}$ to $10^{-11}$, depending on the type and size of the network.

Packet communications units (PCUs) are currently nearing commercial availability. They are the intelligent modems required to support broadcast-type packet networks with backbone rates to 3M bits/s/channel. With reference to the

# Is your data scrambled?

# We can fix it sunny-side up!

At Dynatech we know how to prepare network management systems. Our management and control architecture unscrambles your hardware, software and operating procedures. The result is sunny-side up data — just as you like it.

## Our basic ingredients are:

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**7644 Dynatech Court**
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**CIRCLE 10 ON INQUIRY CARD**

**Commitment.**

It's one of those over-used words in danger of losing all meaning.

Not so for system houses and computer system manufacturers. To you, commitment is the difference between a supplier who leaves you in the lurch. And one who doesn't.

At Century Data, we understand that our success depends entirely on your success. And that broken shipment promises can mean a lot more to you than delayed drives.

Clearly we're in this together. You'll see that attitude reflected in everything we do.

Take our products. No one offers a broader selection of rotating disk drives. Our Trident has earned a reputation as the industry's most reliable removable-pack drive, in capacities from 25 to 600 MB.

Marksman is making a hit as the Winchester with built-in intelligence. It gets you to market quickly, without time wasted on controller development. It's available now—hard-tooled—in 10, 20 and 40 MB capacities, with or without built-in controller.

Hunter is gaining attention as the superior split-pack cartridge drive, combining 16 MB removable and up to 80 MB fixed. And the same reliability and maintainability proven in thousands of Tridents.

We've made the commitment to pump new life into Diablo cartridge drives. We couldn't be more delighted with Xerox's assignment to us of Diablo drive marketing. You can count on us as an eager, dependable source of supply.

The future looks even brighter as we listen to you. And the results are starting to show. The need for lower costs per megabyte led to development of this 600 MB Trident. Priorities have been made out of your need for more self-diagnostics and built-in intelligence. An intelligent Hunter is on the way. And more capacity for the Marksman.

Unlike few other disk drive manufacturers, we are able to draw on the resources of Xerox research to keep us—and you—on the leading edge of storage technologies as they develop.

Customers come to us for our products, then come back because we perform. With service. Support. Dependable delivery. And extra effort.

What it comes down to is this: Commitment may be just a word. We expect you to judge us on our actions. Then see if you can find a better word to describe our approach to this business.

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**CIRCLE 11 ON INQUIRY CARD**

# YOU CAN COUNT ON US FOR THE ENTIRE CENTURY.

service types listed in the Table "Broadband Data Devices," the characteristics of rf modems may be further analyzed.

### Fixed Frequency Modems

These are the oldest and most prevalent types currently available. They are normally crystal controlled, and are characterized by rate/bandwidth figure, data rate, interface, and operation. Generally, these modems have an almost linear cost/bandwidth curve based on efficiency. A synchronous modem capable of 19.2k bits/s and occupying 100 kHz of spectrum space may cost only $700. At this same data rate, one occupying 15 kHz of spectrum may be priced at $3000. Modulation method and filters account for the cost difference.

Fixed frequency modems are crystal controlled for several reasons. Phase modulation techniques usually used to encode data require low phase noise with high stability in the local oscillator in order to achieve low bit error rates. Because of the simplicity of crystal control, the cost of these modems is generally low, and the crystal approach is prevalent for this type of modem. Furthermore, the broadband medium requires the modem to maintain its relative frequency position. Any appreciable frequency drift in a modem would cause degradation in an adjoining channel.

Crystal controlled modems are characterized by several production difficulties. These include individual adjustment requirements, and the need to stock literally hundreds of different crystals. They also require readily available repair facilities in order to reduce the need for stocking spare modems of many different frequencies.

The modulation technique generally used in crystal controlled modems allows rather simple modulation at rates up to several megabits per second. Reception of the biphase or quadriphase modulated signals contributes most to the modem cost. Interfaces currently available for these modems include RS-232-C for asynchronous and synchronous units to 48k bits/s, CCITT V.35 for synchronous modems from 56k to 1.5M bits/s, and special interfaces for the higher rates.

Synchronous modems will operate in multipoint environments, allowing the system to support polled bisynchronous applications. They are also capable of switched carrier operation. In the case of high speed units, most provide either polled or contention operation, and easily accommodate packets and file shipping.

### Frequency Agile Modems

These are synthesized carrier types, and use modulation techniques compatible with synthesis. Their speed and application determine the number of carrier channels such modems provide. At low and medium speeds, up to 56k bits/s, these units may offer as many as 240 channels. Switches or computer control accomplish channel selection.

Agile modems offer two primary advantages over their fixed frequency counterparts. First, there is a minimal requirement for sparing; only a few units will achieve full sparing capacity. Second, allowing intelligent equipment to assign links by frequency opens up a whole new area of networking capability.

Interfaces available for agile modems include RS-232-C, V.35, and TTL (direct logic). Synchronous links are accommodated by internal clock only, and computer control of channels is parallel TTL-compatible. Since agile modems are a bit more expensive than fixed frequency types, their use demands a more critical analysis of system requirements, especially in the light of cost effectiveness.

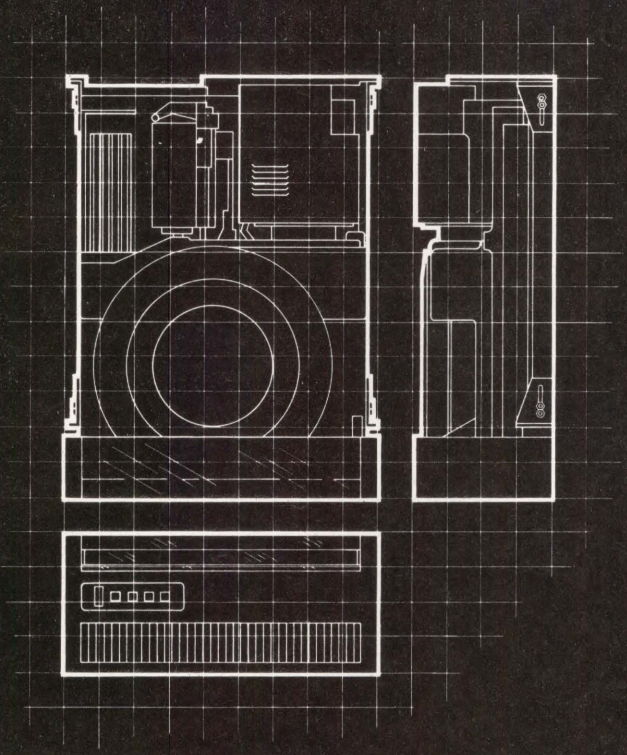
*(continued on page 22)*

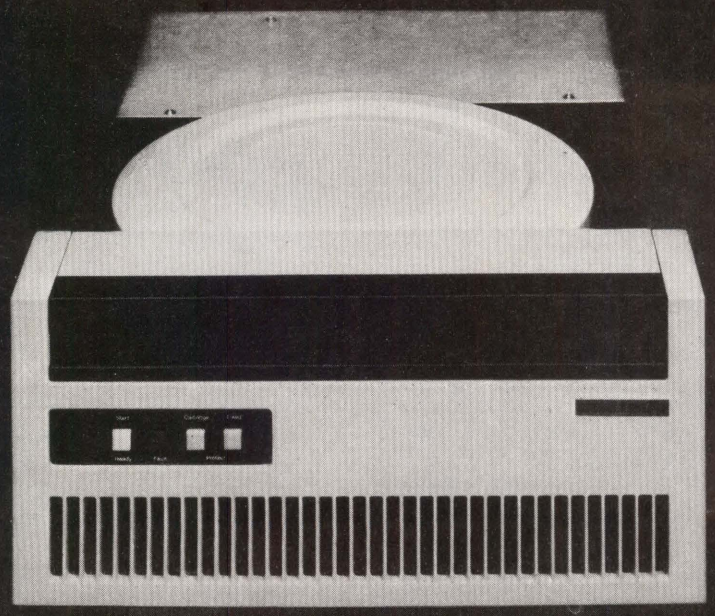
**Broadband Data Devices**

| Device | Primary Application | Mode | Frequency | Data Rate, Bits/s | Interface | Protocol |
|---|---|---|---|---|---|---|
| Modem, rf | Point to point | Asynchronous | Fixed | 110-19.2k | EIA, Bell | n/a |
| Modem, rf | Multipoint | Synchronous | Fixed | 300-19.2k | EIA, Bell | n/a |
| Modem, rf | Multipoint | Synchronous | Fixed | 56k-512k | TTL, EIA, Bell | n/a |
| Modem, rf | Point to point, Multipoint | Synchronous | Fixed | 512k-6M | TTL, EIA, Bell | n/a |
| Modem, rf | Point to point | Asynchronous | Agile | 100-9600 | EIA | n/a |
| Modem, rf | Multipoint | Synchronous | Agile | 300-56k | EIA, CCITT | n/a |
| PCU | Point to point, Virtual circuit | Synchronous, Burst, Contention | Fixed | 307k-1M 1200 at user interface | EIA, Parallel | HDLC variant CSMA/CD |
| PCU | Point to point | Synchronous, Burst, Contention | Agile | To 9.6k at user interface | EIA | Custom |

As can be seen, current modems and PCU devices allow terminal devices, minicomputers, microcomputers, and hosts to utilize the broadband medium to accommodate the data rates and services they require. Standard interfaces are offered in many units, as well as special bandwidth/data densities needed for increased cable capacity. There are devices available to suit most data requirements in broadband applications. New products will increase to an even greater extent the capabilities offered by this medium

# Perkin-Elmer presents a complete rethinking of the cartridge disk drive.





# Introducing VANGUARD I. Simple. Reliable. Economical.

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We wanted a totally new cartridge drive that would satisfy systems requirements for backup store and audit trails.

That would meet the needs for working and archival storage in small business systems.

That would offer the compactness needed for desk-mounted peripherals.

That would provide a high speed single storage system at a price that would give systems designers something to think about.

The result was the cartridge drive for the systems of the 80's—VANGUARD I.

We built VANGUARD I 24 inches deep for in-desk or rack mounting. We gave it a capacity of up to 20 megabytes and a standard cartridge disk interface for industry-wide compatibility.

To make VANGUARD I easy to maintain and service, we built it in simple modules. That makes maintenance a matter of minutes instead of hours. (VANGUARD I can be broken down into subassemblies in less than seven minutes, reassembled quickly with minimum tools.)

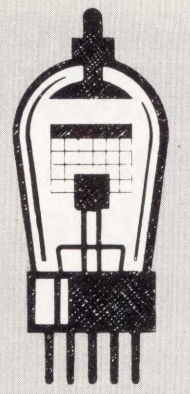
And to reduce the need for maintenance we gave it an air moving system designed for maximum cleanliness and minimum temperature rise in the media chamber.

VANGUARD I is everything we think a cartridge disk drive should be. Simple. Reliable. Fast. Universally compatible.

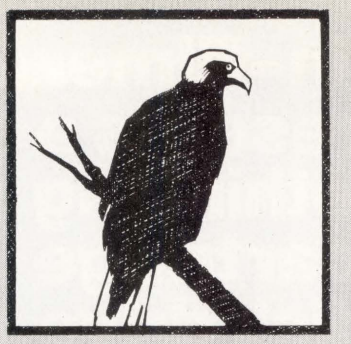
Call or write today for a preview look. And let us know what you think about our rethinking. Perkin-Elmer, Memory Products Division, 7301 Orangewood Avenue, Garden Grove, CA 92641. **Call toll free 800-631-2154. In California, call (714) 891-3711.**

**PERKIN-ELMER**

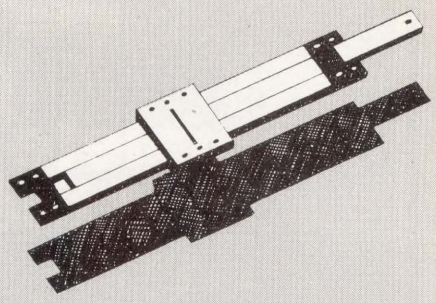
**CIRCLE 12 ON INQUIRY CARD**



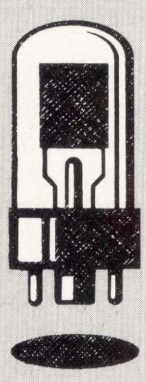
**Thyratron**—A hot cathode gas tube in which a control electrode initiates the anode current but won't limit it. Used as an electronic switch in early control circuits. Replaced by thyristors.



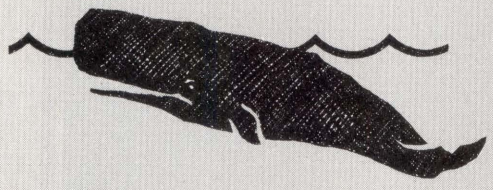
**American eagle**—The eagle narrowly defeated the turkey as America's national symbol. Although fabled to carry off children and lambs, eagles cannot lift more than seven or eight pounds. Comprehensive federal protection didn't begin until 1952, after the species was threatened by egg collectors, hunters and sterilization by DDT.



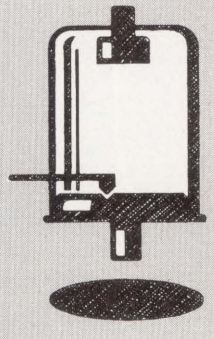
**Slide Rule**—An analog calculator based on the logarithm. Developed in 1630 and perfected by a French army officer in 1850. Used to multiply, divide, calculate squares, cubes, square roots, trig functions, etc. Virtually disappeared after the appearance of the inexpensive electronic calculator.



**Thermionic valve** — Early vacuum tube designed to control the emission of electrons and ions (called thermions) from heated substances. Principle discovered by Edison while working on the light bulb. Basis of many electron tubes. Outmoded by the semiconductor.

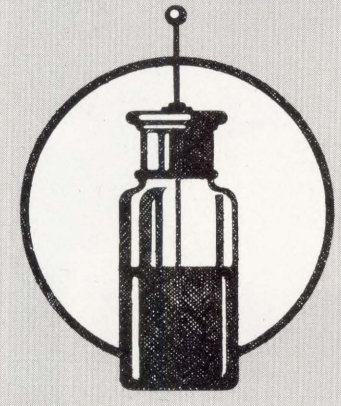


**Whale**—Huge mammals which reversed evolutionary trend by returning to the sea 60 million years ago. Once proliferating in all the oceans of the world, whales were reduced to 2,000 animals before controls were imposed. Valued for their oil, whales were first hunted in the 10th century by Basques standing on shore. Today they are caught and processed entirely at sea by huge floating factory ships.

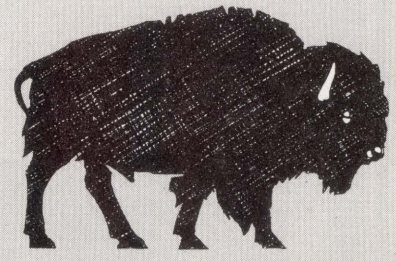


**Ignitron**—A type of mercury arc rectifier with only one anode. Developed in early 1950s. Arc is started at each cycle by an ignitor dipped into a pool of mercury (the cathode). Frequently broke down at higher voltages.

**Alligator**—A cousin of the crocodile, alligators eat fish and small animals, and only attack humans in self-defense. Once they averaged 18 ft. from snout to tail. Today 9 ft. is considered uncommonly large. Threatened by urbanization destroying their habitats, and by hunters seeking their skins for purses and shoes.

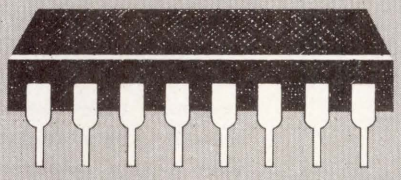


**Leyden jar**—A crude capacitor developed at the University of Leyden in 1742. Although important in the development of electronic theory, the Leyden Jar is considered cumbersome and inefficient by modern standards. Currently used only for laboratory demonstrations. Replaced by the modern capacitor in all its forms.



**American buffalo (bison)**—Related to the domestic cow. Males often top six feet at the shoulder and weigh 3,000 pounds. Once a primary source of food and hides for the American Indian, they were hunted into near extinction by the white man. There were 60 million buffalo in 1800, only 250 in 1900. Today 20,000 survive in parks.

# The low-density bipolar PROM will never become an endangered species.



**Low-density bipolar PROM**—First developed by MMI in 1971. Proliferated in a variety of commercial and military digital applications. Small species currently includes 256-bit, 1K and 2K sizes, closely related to the denser 4K and 8K-bit variety. 16K and even greater density types are now in evolution. The low-density bipolar PROM, rumored to be endangered in 1979, will continue to flourish at MMI.

## MMI is committed to producing bipolar PROMs from 256 bits up, in volume, as long as you need them.

You may have heard rumors you'll be forced to specify only 4K-or-denser bipolar PROMs, because low-density PROMs won't be available much longer.

Don't believe it.

MMI makes PROMs from 256 to 8K bits now, and we'll continue to make them in the future. That's a commitment that means something, coming from the company that ships more bipolar PROMs than anyone else in the world.

**Our PROM product line is alive and well.**

MMI's leadership in bipolar technology is clear. We introduced the 1K bipolar PROM in 1971, and the world's first 2K, 4K and 8K bipolar PROMs shortly thereafter. Now we have a 16K bipolar PROM in development. But even though we will continue to develop denser and faster versions, we'll never lose sight of the low-density PROM. In fact, watch for MMI's announcement of a new family of faster 1K and 2K PROMs to complement our current line. These new PROMs will have access times ranging from 45 ns to 60 ns and a power consumption range of 65 mA to 130 mA.

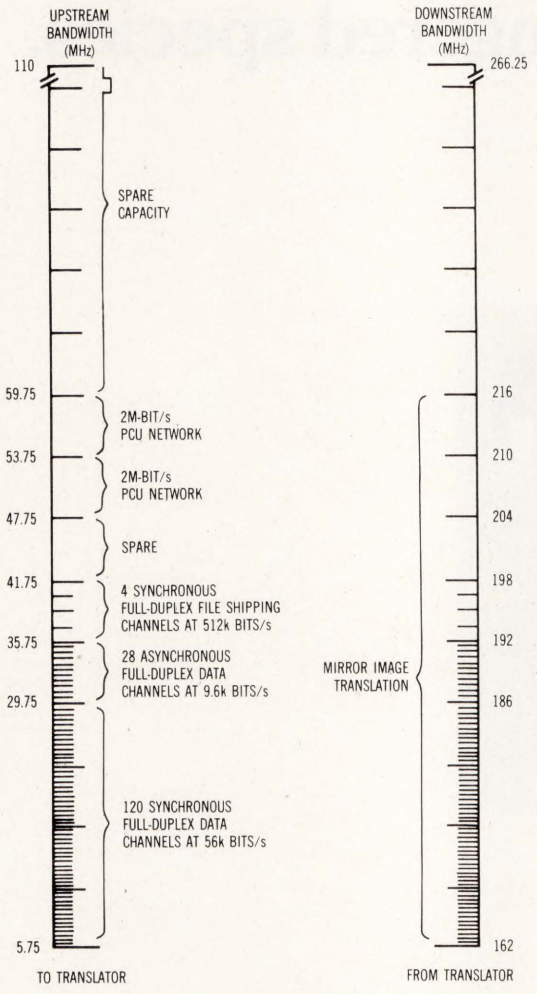
**Find out why our commitment to bipolar is important to you.**

Discover how the PROM and other bipolar products are flourishing at MMI. Ask your nearest MMI rep or distributor for our new, comprehensive LSI Data Book. You'll find the answers to your detailed questions about MMI's bipolar memory and logic.

Monolithic Memories, Inc.
1165 E. Arques Ave., Sunnyvale, California 94086.

**Monolithic Memories** MMI

CIRCLE 13 ON INQUIRY CARD




Basic channel allocation. Properly designed broadband system offers tremendous traffic capacity. Using selected products and technologies, large terminal distribution systems may be accommodated, as well as host and subsystem links. "Stacking" of channels by bandwidth occupancy resembles microwave and satellite practice, in that maximum use is made of available media bandwidth, where possible, by frequency division multiplexing

## Packet Communication Units

PCUs are actually intelligent interfaces to a packet backbone channel. They receive data from a user or host device in synchronous or asynchronous mode, format them into packets, and broadcast the data at a high rate onto the coaxial backbone. Distributed control of the shared backbone medium permits support of thousands of bursty terminal subscribers.

The PCU is a fixed frequency intelligent device. It accepts and buffers characters from a standard interface, and creates a packet of information. When the receiver side of the modem senses the backbone channel carrier "low," it broadcasts the buffered packet onto this line. The formatted packet contains addressing and error control information in addition to the packet data. When the appropriate destination address is detected at the receiving PCU, the packet is shifted into memory. The reverse process is then performed on the packet data and the information is supplied to the receiving party.

PCUs may be supplied with protocol translators that allow the high speed bus to service many different user terminal types on the same channel.

## Agile Packet Networking

Agile PCUs are useful where the basic network load is too high to be handled by a single packet channel. This may become a problem when bursty subscribers are replaced or augmented by smart terminals or minicomputers, or when response times become critical. These demands bring substantially more data traffic onto the backbone and may slow system response to the users. Agile PCUs provide dedicated channel allocation by activity. That is, when a subscriber wishes to request a file transfer, a screen of graphics, or something similar, he is switched to a secondary set of file transport channels, thereby offloading the shared packet network base.

Connectivity in this type of system is assigned by channel allocation, not by the medium. Unless the designer has taken specific steps to limit access, all of the signals submitted to a broadband network appear at all taps in the network. This allows subscribers to move locations and designers to add functions virtually at will.

## Summary

To generate the topology of a broadband system, showing only the basic tree or star hybrid of its form, is a straightforward project. A complex system, however, must be broken down into layers, each corresponding to a particular service, bandwidth, data rate, and control mechanism. To be realistic, connectivity for a broadband system may be just as complex as that of its conventional counterparts. The "Basic Channel Allocation" chart shows slots assigned in the channel space of a single broadband cable.

As may be seen, the capacity of one cable is immense. The capability to provide links for terminal, processor, computer to computer, and distributed processing applications on this transmission medium is virtually unmatched.

The combination of capacity and capability offered by broadband coaxial cable local area networks provides network architects and designers a medium of great power, flexibility, and growth potential. It represents the closest analogy to the "wired city" concept yet available, and should be considered as one of the top contenders for multimode local area networks.

Currently, the equipment necessary to configure broadband local area networks is available to the designer in basic form. FDM agile modems, PCUs, hierarchical network components, and network monitoring systems are on the verge of introduction as high volume commercial products. The designer or manager interested in implementing the growth of a network in a cost effective manner may be well served by fully investigating the benefits of broadband.

# Introducing the one-step AMP PACE connector.

# New AMP PACE connector. The proved pre-assembled compliant pin connector for solderless backplanes...with selective plating.

Step up your output with the new one-step AMP PACE connector. It not only reduces production time, but helps avoid rejects in the process.

Fully preassembled, it's simply pressed into the board.

The heart of the connector is the ACTION PIN contact. The first compliant pin to make successful solderless connections—without time-wasting and costly hole damage.

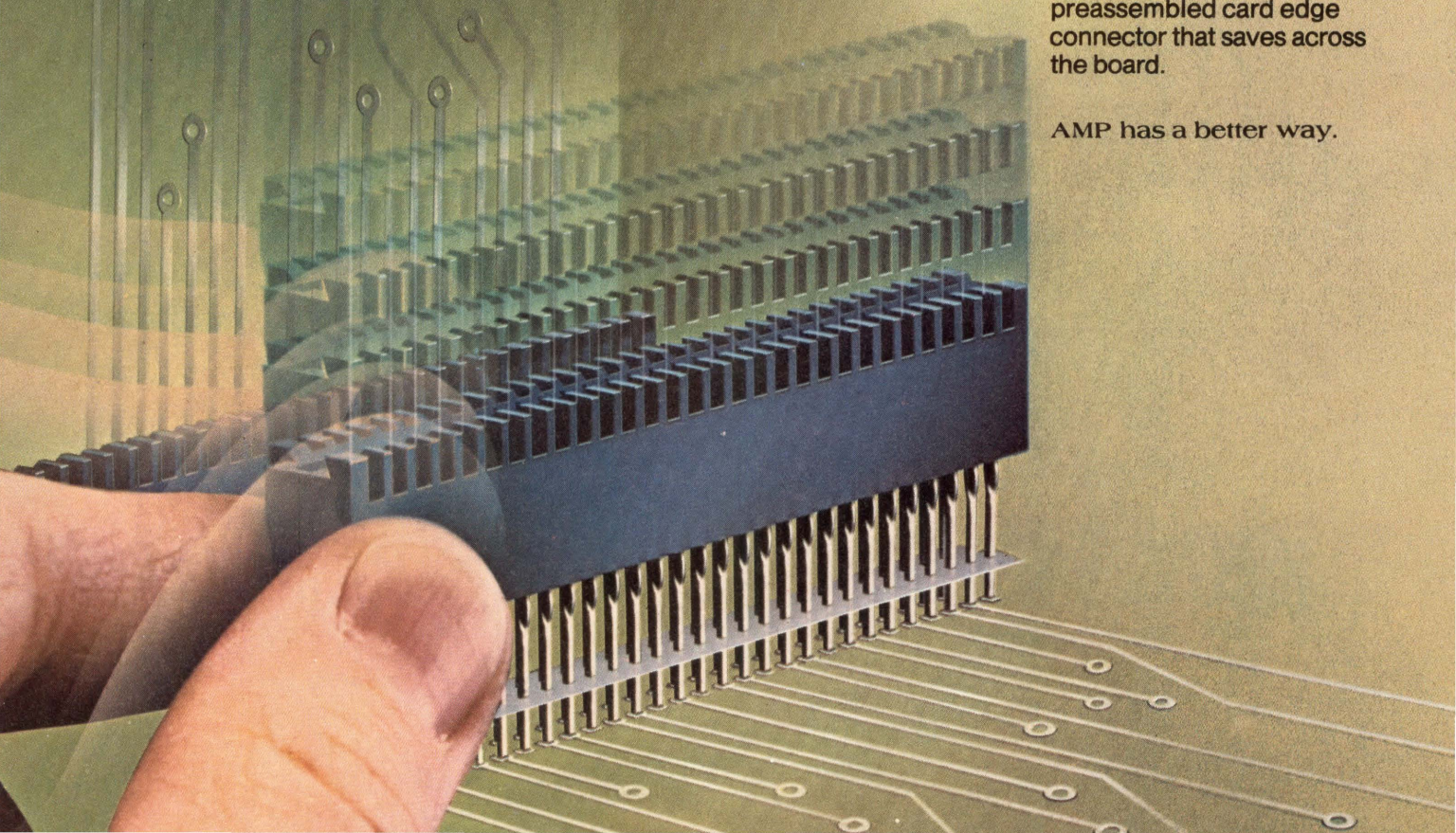
Complementing this concept, AMP engineers have applied our extensive plating technology by using selective gold striping in the connector's critical contact area—and tin-lead plating on the posts.

What's more, our unique beam design accommodates and compensates for any daughter board warp and stress. So you're assured of long-term performance.

You can have this preassembled card edge connector in .100" x .200" centerlines, and a range of positions.

See your AMP representative for the new preassembled card edge connector that saves across the board.

AMP has a better way.



**It has a firm grip**

The spring sections of the ACTION PIN contact compress in opposite directions for a gas-tight connection, every time.

The right touch

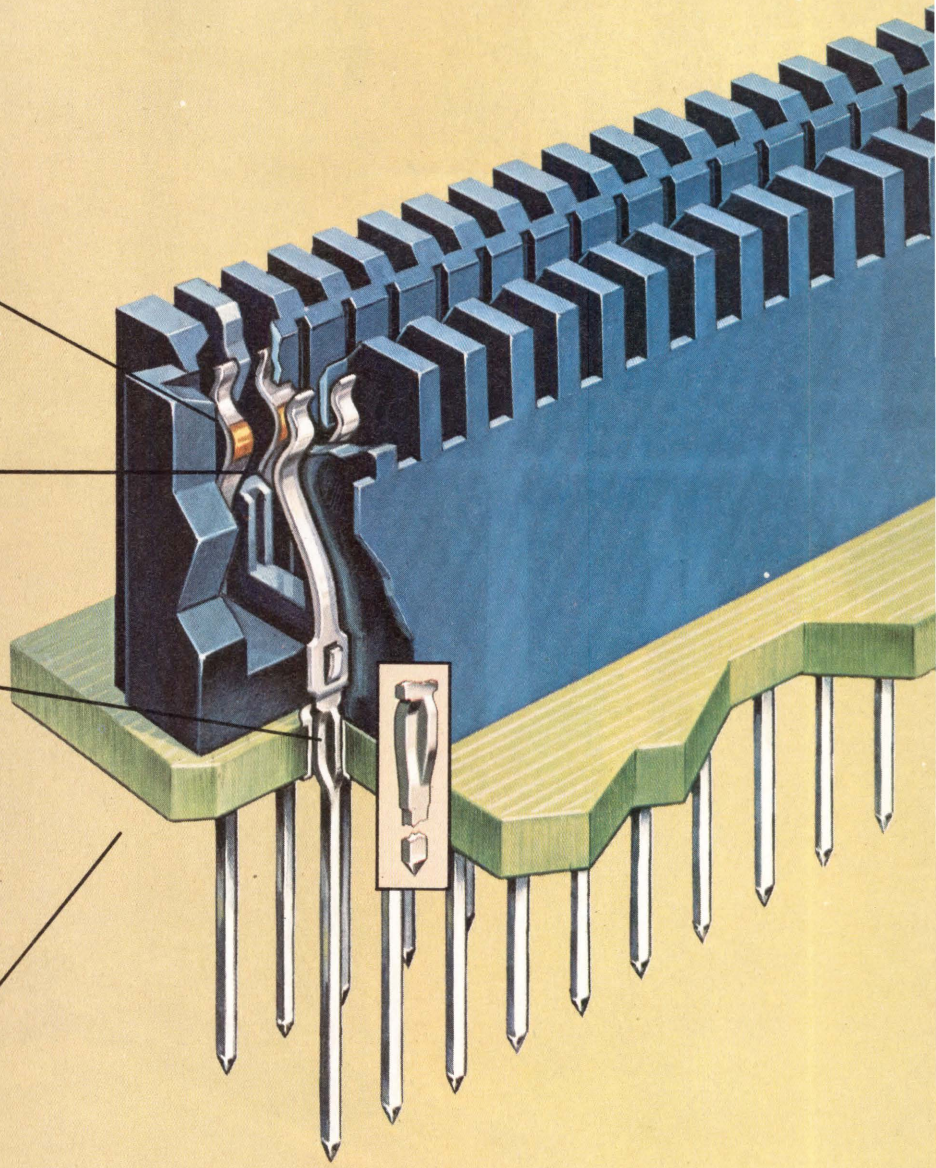
With selective gold plating engineered for the '80s, AMP PACE connectors ensure superior electrical contact at minimum cost.

**$aves money**

The solder-free contact fits into the board each time without rupturing the plated-through hole. Also, any pin can be replaced several times without affecting electrical or mechanical performance. Connectors come with pre-fitted spacer which keeps each contact in line.

**And you just PRESS it into service**

The AMP PACE connector's preassembly makes a one-step installation possible—with application equipment designed to provide even pressure across each contact.



**Some facts worth knowing about AMP PACE connectors:**

**Contact Rating:** 3 Amp.
**Contact Resistance:** Spring contact to test board—8 milliohms
Total circuit resistance—9 milliohms
**Operating Temperature:** −55°C to +85°C.
**Voltage Rating (Sea Level):** .100" centerline spacing—1000 VAC
**Insulation Resistance:** 5,000 Megohms.
**Durability:** 100 cycles.
**Salt Spray:** MIL-STD-1344, Method 1001.
**Thermal Shock:** MIL-STD-1344, Method 1003.
**Physical Shock:** MIL-STD-1344, Method 2004.
**Humidity:** MIL-STD-1344, Method 1002, Type II.
**Vibration:** MIL-STD-1344, Method 2005.
**Where to telephone:** Call AMP PACE
Connector Information Desk
at (717) 780-8400.
**Where to write:** AMP Incorporated
Harrisburg, PA 17105

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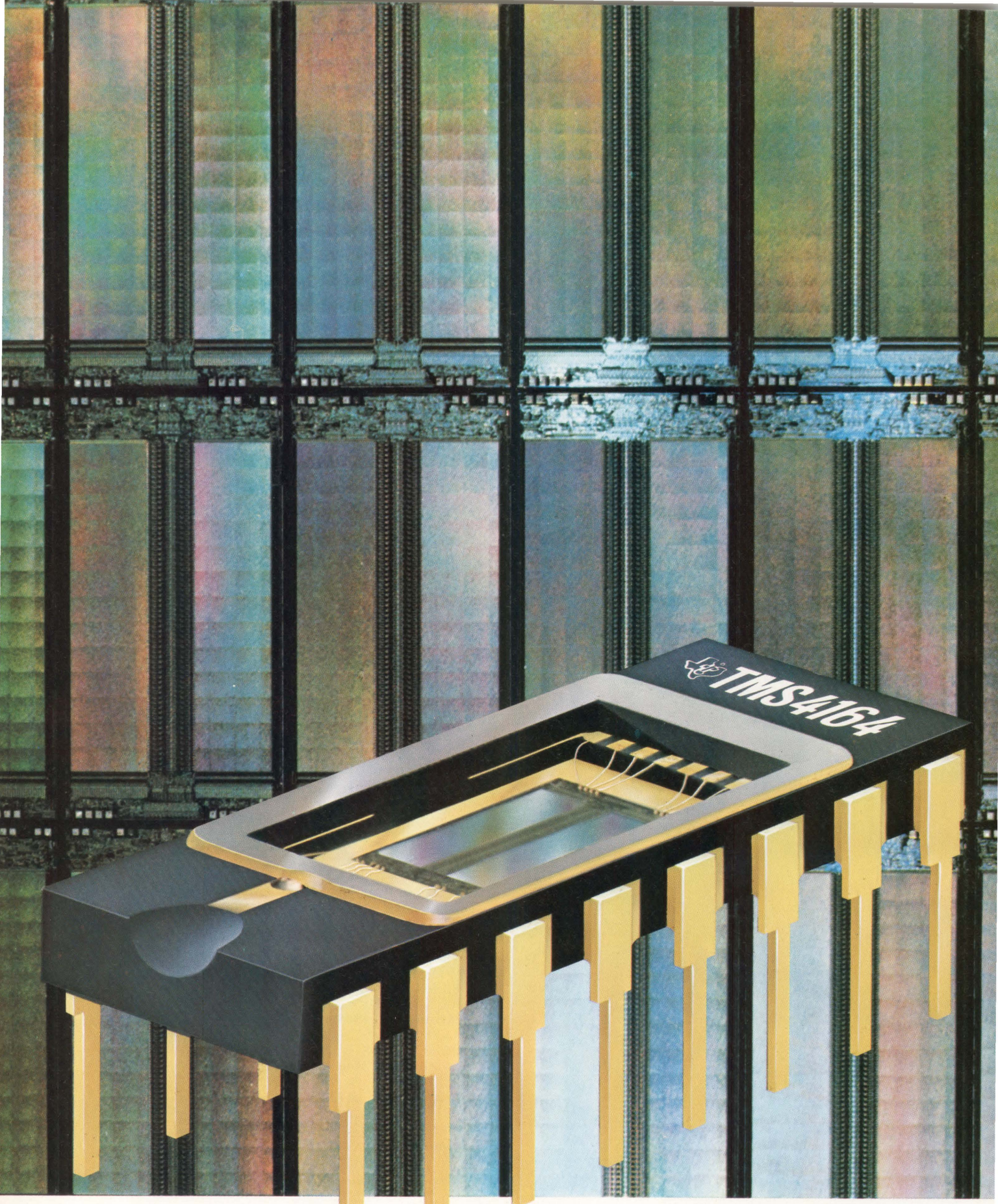
**AMP**

CIRCLE 14 ON INQUIRY CARD




*Another major milestone in MOS memory technology from Texas Instruments . . .*

# TI's 64K dynamic RAM is ready for delivery. Now.

TI has paced the industry through generation after generation of semiconductor innovation, pioneering a lion's share of the major milestones in technology and production capability.

The new TMS4164 from Texas Instruments represents the fourth generation of dynamic RAM computer memories, and continues to fulfill the bright promise of innovative MOS technology.

TMS4164. Advanced architecture. Superior performance. High speed. High reliability. Low power. *And ready for delivery.*

Ready with 4 times the capacity of 16K RAMs in the same size package.

Ready with 65,536 bits of random access memory — and that's more than many board-level computers.

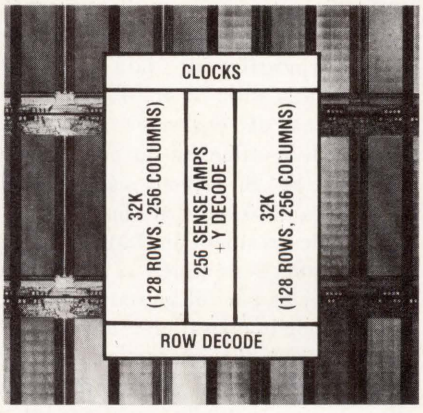
Ready with 256 cycle, 4 ms refresh architecture — the optimum organization evolving from all previous industry-standard dynamic RAMs.

Performance has been dramatically enhanced. Speed's up. Power's down. And design innovation makes this the *smallest 64K chip (35K mil²) available anywhere.* From anyone.

Improvements in density, reliability, system cost and ease of use are some of the features, functions and benefits system designers will appreciate. Here's more:

- 64K bits in a standard, 300-mil, 16-pin package saves valuable board space and reduces system size
- Single 5-volt operation lowers power supply cost and system cooling requirements and improves reliability

**TMS4164 256 CYCLE REFRESH ARCHITECTURE**




- JEDEC-approved pinout with N/C on pin one assures standardization and guaranteed availability
- High speed: 150-ns access and 280-ns cycle times (min.)
- TTL compatible I/O and clocks
- Lowest power dissipation available: 125 mW typical
- 256 cycle architecture means lower current peaks and reduced system noise
- State-of-the-art SMOS (Scaled MOS) processing

TI's new TMS4164 is perfectly suited for use in mainframe computers and large minicomputers. It also finds ideal application in microprocessor-based systems where smaller size, lower cost and improved performance are important considerations.

TMS4164. The deliverable, practical, usable 64K dynamic RAM. Compare our 256 cycle refresh architecture ... then compare our performance.

TMS4164. Truly another major milestone in MOS memory technology. Truly another example of the total commitment Texas Instruments is making to leadership MOS memory products.

**For more information about the deliverable 64K RAM,** call your nearest TI field sales office, or write to Texas Instruments Incorporated, P.O. Box 1443, M/S 6965, Houston, Texas 77001.

Fifty Years of Innovation

TEXAS INSTRUMENTS
INCORPORATED

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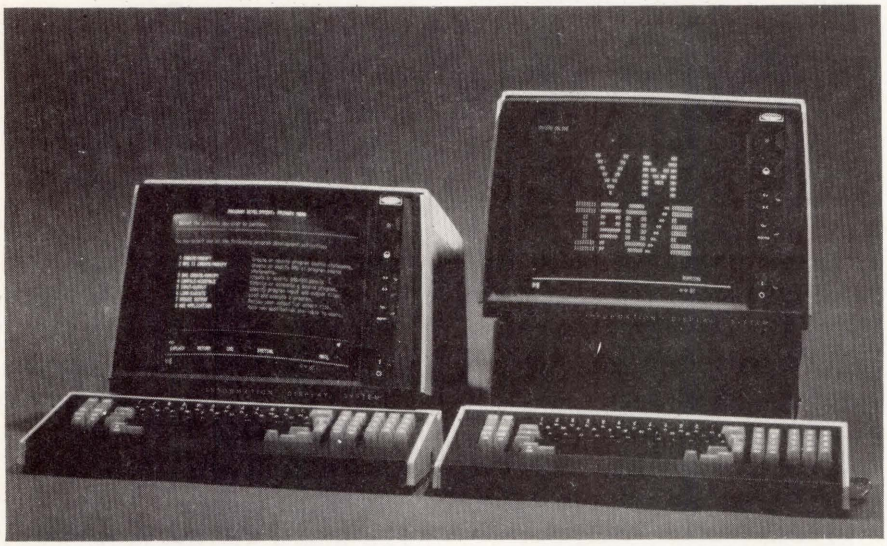
85007B

CIRCLE 15 ON INQUIRY CARD

## Intelligent Information Display System Emulates IBM Terminals




PTS-2000 display stations. Intelligent terminals are provided with typewriter or data entry keyboards with 75 or 87 keys, cursor select, separated function keys, and accessible display control knobs. Control unit can operate as standalone device, or as base for display terminal as shown above (right)

Said to be the foundation of the company's information processing product line for the 80s, the PTS-2000 information display system has been introduced by Raytheon Data Systems Co, 1415 Boston—Providence Tpk, Norwood, MA 02062. It is the first of a family of devices designed to operate under IBM systems network architecture (SNA). The PTS-2000 is a small cluster system that emulates IBM 3276 communications protocol. Display terminals, controller, and printer comprise a typical system.

The microprocessor based alphanumeric display terminal is a plug to plug compatible replacement for the IBM 3276 display system. Terminals can be located up to 5000′ (1500 m) from a control unit via RG-62/U coaxial cable. Display screen is 15″ (31.5 cm) diagonal, with selectable displays of 80-char by 12, 24, or 32 lines of 10 x 14 dot matrix characters. An extra displayable line of protected data carries system/terminal status and operator prompting messages. Display terminals and keyboards have built-in microprocessors to distribute the processing load internally. 16k bytes of RAM and 8k bytes of ROM are contained in each terminal, enabling the display unit to offload certain software functions formerly performed by the controller.

Keyboards can be furnished in either typewriter or data entry arrangements, with 75 or 87 keys in an assortment of character sets. The keyboard is attached to the display unit by an 8′ (2.4-m) cable. Each display and keyboard has self-test diagnostics resident in ROM, allowing all functions to be tested as standalone devices or as part of an entire system. A test mode of operation is also provided to display the interaction between control unit and host; in this mode the display unit actually functions as a communications test set.

The controller can accommodate any combination of eight display terminals and printers. It uses 3276 emulation software operating under BSC protocol, with up to 7200-bit/s data transmission to and from the host. The unit contains a 72k-byte mini-floppy diskette drive and up to two 32k-byte memory modules. Formatted data storage in the mini-floppy serves as the program load device and software distribution medium. One modem adapter with external clocking is supplied, with a second offered as an option. Extensive diagnostics are included.

The PTS-2000 series impact printer is a 120-char/s, bidirectional, 7 x 9 dot matrix output device.. It will accept 4 to 17.3″ (10.2 to 43.9-cm) wide continuous sprocketed paper and can accommodate up to 6-part carbon interleaved forms. Printing format is up to 132 cols, 10 char/in (3.9 char/cm), with 6 or 8 lines/in (2.4 or 3.1 lines/cm) vertical spacing, switch selectable. Character set is full 64-char EBCDIC.

A typical PTS-2000 configuration of four display terminals, one controller, and one printer is priced at $22,170, or $529/mo including maintenance on a 2-yr lease basis.

Later this year, according to company spokespersons, the system will add BSC and SNA emulation of large clusters (1- to 32-station), 3274 protocols, a 3440-char display screen, and an increase in data rate to 9600 bits/s.

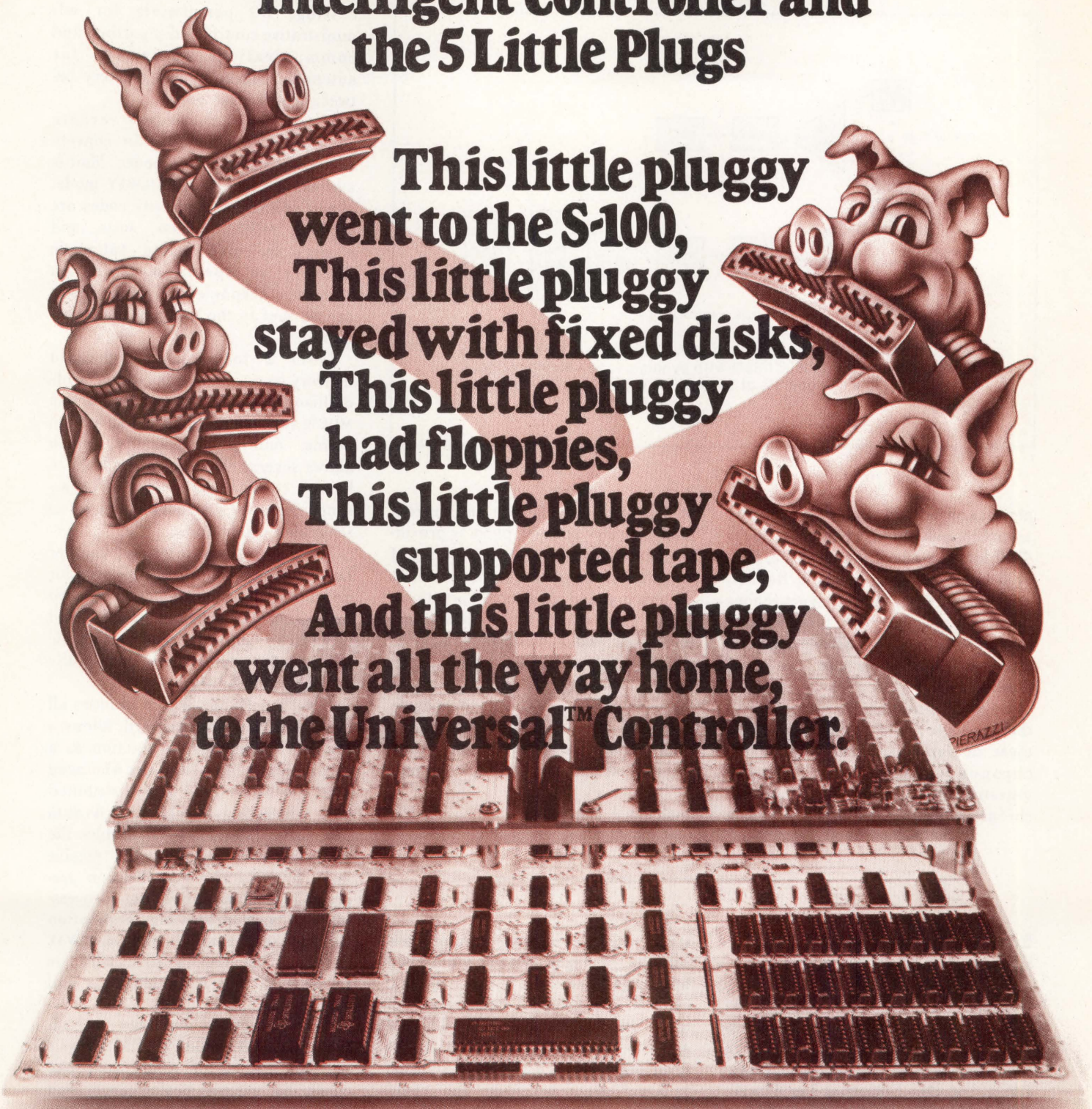
Circle 517 on Inquiry Card

## Network System Combines Processing and Control Functions

The portable 4200 network system can function as a statistical multiplexer, allocating transmission time on a dynamic demand basis to optimize line utilization. A single voiceband link operating up to 19.2k bits/s, or two separate 9600-bit/s links, can serve as many as 60 terminal circuits, for up to 90% savings in telephone line costs, according to Halcyon Data Systems, 2121 Zanker Rd, San Jose, CA 95131. X.25 Level 2 protocol, which includes ARQ error correction, is used. As a network control center, the system can remotely control network configuration, and also provide performance statistics and network diagnostics.

The unit handles a mix of synchronous and asynchronous lines, with a wide range of protocols and codes. No modifications are required to terminal software or line speeds, providing flexibility of application into

# The Universal™ Intelligent Controller and the 5 Little Plugs




Five plug sets is all it takes for simultaneous, multi-device storage control. DML's Universal™ Intelligent Controller makes it possible.

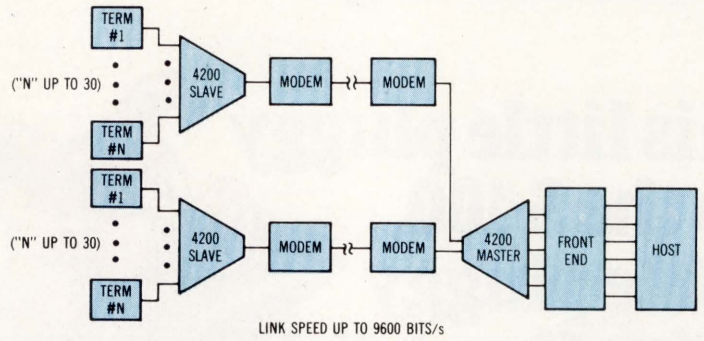
- S-100 Bus, with CP/M* support
- Plug adaptable device support
- Control of up to 8 storage devices: 4 fixed disks, 4 floppy or tape cartridge drives
- IEEE DMA or port transfer

Call or write for full information. Data Management Labs, 2148 Bering Drive, San Jose, CA 95131 (408) 946-9424.

*CP/M is a trademark of Digital Research

DATA MANAGEMENT LABS

CIRCLE 16 ON INQUIRY CARD




Multilink configuration. With links in simultaneous operation, each can transmit at up to 9600 bits/s with dynamic load sharing. Alternatively, either link can operate at 19.2k bits/s while other is on standby

almost any network. Full or half duplex asynchronous lines, operating up to 4800 bits/s, may carry codes of 5, 6, 7, or 8 bits/char, such as ASCII, Baudot, and BCD. Protocols for synchronous lines with speeds to 9600 bits/s include BSC, CDC 200UT, and UNIVAC; codes include EBCDIC, ASCII, and two user-defined codes.

Up to 60 lines can be connected to the processor, with as many as 16 of these operating synchronously. Asynchronous lines can operate unrestrictedly to 4800 bits/s, and synchronous lines to 9600 bits/s. A choice of EIA RS-232-C/CCITT V.24 and current loop interface adapter plugs is provided. The EIA plugs permit interfacing of asynchronous and synchronous lines in all terminal and modem combinations. 20, 40, or 60 mA current loop adapters for asynchronous lines handle all combinations of active and passive terminals and receivers. Additional features of the 4200 system include autobaud (from 110 to 1200 bits/s), data compression, echoplex, line priority assignment, and flow control.

Circle 518 on Inquiry Card

## Enhancements Added to Electronic Mail System

Software and hardware packages as entry and intermediate levels of its MAILWAY electronic mail system have been introduced by Wang Laboratories, Inc, One Industrial Ave, Lowell, MA 01851. The system, originally announced in 1979, is a software package allowing initiation of document distribution from a Wang system workstation to a number of recipients regardless of their location.

Level 1 software is aimed at the first time, small user. Level 1 allows communication from workstation to workstation on the company's word processing, OIS, or mixed systems via dial-up telephone lines at data rates to 4800 bits/s. Use of the mail system does not affect the conventional method of creating, editing, or printing of documents. Level 1 is also applicable to larger established users who intend a more deliberate move toward implementation of an electronic mail system.

Level 2 software incorporates the simultaneously introduced MAILWAY distribution controller (MDC50) hardware which provides central management of electronic mail functions for those not requiring data processing capabilities. MDC50 is not user programmable. It includes intermediate storage for store and forward mail processing, I/O peripherals for administrative control and reporting, and communications equipment for automatic collection and delivery between distribution points.

In Level 2, senders create documents to be mailed in conventional word processing modes. Mail is addressed using any MAILWAY mode. When security and priority codes are applied, MDC50 collects, sorts, and secures the mail before automatic delivery to specified sites. An automatic acknowledgment of receipt can be sent to the initial sender if required.

Level 2 includes an enhanced delivery services option which adds multizone ability, a zone being one MDC50 and its subordinate distribution points; multiport capability, which allows several communication lines to be run concurrently; and priority arrangements for immediate as well as scheduled distribution.

Word processing interface, another Level 2 option, eliminates the need for an additional system dedicated to word processing by providing both word processing software and electronic mail support to workstations locally connected to the MDC50.

Level 3 software, which includes all Level 2 features as standard, allows a Wang VS computer to function as a distribution center for users who need both electronic mail and distributed data processing capabilities. A data processing interface (DPI) enables the VS to interactively send and receive mail. DPI also allows application programs to send mail. Both data processing and word processing information can be sent through the MAILWAY system, as the application is transparent to transmitted data and text.

Other functions available in both Levels 2 and 3 include Traffic Analysis and Mail Log, for single keystroke check of system performance and system integrity, respectively. Mailbox function allows users to look into the system for their mail, revise documents to be returned to the sender, reroute documents, and to send documents for printing or for storage on large capacity discs.

Circle 519 on Inquiry Card

# To sell the best terminal, buy the best keyboard.

The keyboard is one of the most critical components in your computer system. Which is why the first thing to consider when you buy a keyboard is reliability.

That alone is probably good enough reason to specify a Hall effect solid state keyboard from MICRO SWITCH. It's the most reliable keyboard you can buy. From the beginning, it will help you and your customers save money on repairs.

As a result of design innovations, the Hall effect keyboard is competitively priced against lower-performance, less reliable keyboards. Innovations like the microcomputer that gave you the first "intelligent" keyboard, the three terminal keyswitch module and single-sided printed circuit boards.

In addition, there's our Value Engineering Program.

With specialists who work with you early in the design of your product, to give you the best, most effective keyboard for terminals used in high throughput applications like word processing, batch data entry, and photocomposition.

And only our keyboards are backed by a dedicated field engineering organization, and an experienced application engineering team. To make sure you have the most cost effective keyboard for the job.

That's really what buying a keyboard should be about.

And why it pays to buy a Hall effect keyboard from MICRO SWITCH, the most reliable keyboard you can buy.

For details, write MICRO SWITCH, Freeport, Illinois 61032. Or call 815-235-6600. In Germany, write Honeywell GMBH, Kaiserleistrasse 55, 6050 Offenbach/Main West Germany.

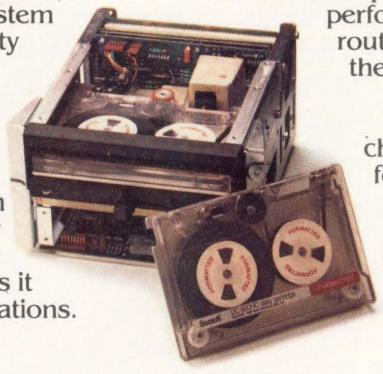
**MICRO SWITCH**
a Honeywell Division

# NEVER BEFORE HAS SOMETHING SO SMALL BEEN ABLE TO HOLD SO MUCH AT SUCH A LOW COST.

This is 3M's DC-600 HC Data Cartridge for disk back-up. It's just 4" x 6" x ½". Yet it holds a full 67 megabytes of formatted user information (144 megabytes unformatted). And most surprisingly, it only costs about thirty dollars.

The marvel that makes it work is our HCD-75 Data Cartridge Drive. At 4.6" x 7" x 8.6" (19" deep with controller/formatter module) it's the smallest full-capability back-up system available today. And its storage capacity makes it the most economical, too.

You see, the HCD-75 drive unit eliminates the need for costly multi-track heads. Instead, it uses a new tape head which features automatic positioning to any of the tape's sixteen tracks. The result is a storage capacity much larger than ever before possible with data cartridges. Which also makes it suitable for other mass storage applications.



Extensive use of microprocessors in the HCD-75 make it the world's first truly intelligent cartridge drive system. Other than initial commands, all tape drive functions are controlled locally. So the host computer system can remain free for other functions. What's more, the HCD-75 features sophisticated error detection and correction capabilities. And to insure system performance, self-test diagnostic routines run continuously. Even when the system is not in use.

Will wonders never cease?

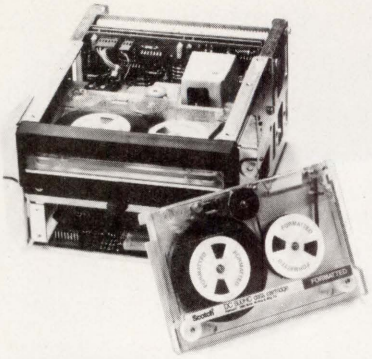
For more information, check the listing on the next page for the representative nearest you. Or write: Data Products Division/3M, Bldg. 223-5E/3M Center, St. Paul, MN 55144.

**THE DISK BACK-UP SYSTEM THAT'S SUDDENLY WAY OUT FRONT.**



**CIRCLE 18 ON INQUIRY CARD**

3M



**3M DATA PRODUCTS REPRESENTATIVES**

Data Products/3M
3M Center, 223-5E
St. Paul, MN 55144
612/733-8892

**WEST**

Hefte Industries, Inc.
Los Gatos, CA
408/264-8319

CTI Data Systems, Inc.
Long Beach, CA
213/426-7375

P.A.R. Associates
Denver, CO
303/355-2363

PSI Systems, Inc.
Albuquerque, NM
505/881-5000

**MIDWEST**

OASIS Sales Corporation
Elk Grove Village, IL
312/640-1850

Carter, McCormic & Pierce, Inc.
Farmington, MI
313/477-7700

The Cunningham Co.
Houston, TX
713/461-4197

**EAST**

J.J. Wild of New England, Inc.
Needham, MA
617/444-2366

Wild & Rutkowski, Inc.
Jericho, Long Island, NY
516/935-6600

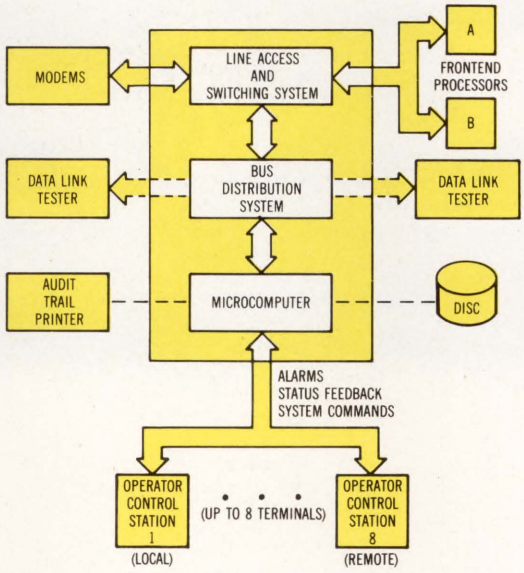
COL-INS-CO., Inc.
Orlando, FL
305/423-7615

3M

## System Supervises Online Data Network Operations

Microprocessor based multiple access switching system MASS+[R] detects and diagnoses network failures and equipment malfunctions and provides for restoration of online service from remote locations. It will access analog or digital communication lines in a data network for monitoring, testing, and reconfiguring network components. These functions can be performed from as many as eight widely separated operator controllable stations. The system was recently introduced by T-Bar Inc, Data Communications Switching Div, 141 Danbury Rd, Wilton, CT 06897. System architecture has the capacity to accommodate up to 512 digital and/or 512 analog lines, for a total of 1024-line capability of either type.

A standard ASCII CRT terminal at each operator station displays, in real time, all commands, line and patch status requests, and alarms for loss of carrier detect. MASS+ software provides for both action and information commands using abbreviated English, as well as prompting to minimize operator training. From a single operator position, the system allows either manual or software programmed centralized control for rapid access to monitor and test one or a group of lines on an individual or simultaneous basis. A single command restores failed service of one, a group, or all frontend ports by switching to a backup unit. Preventive maintenance and accommodation of changing tasks can be effected by preprogrammed switching of frontend ports. Remote patching and substitution of spare modems can be performed with no local degradation of signals.

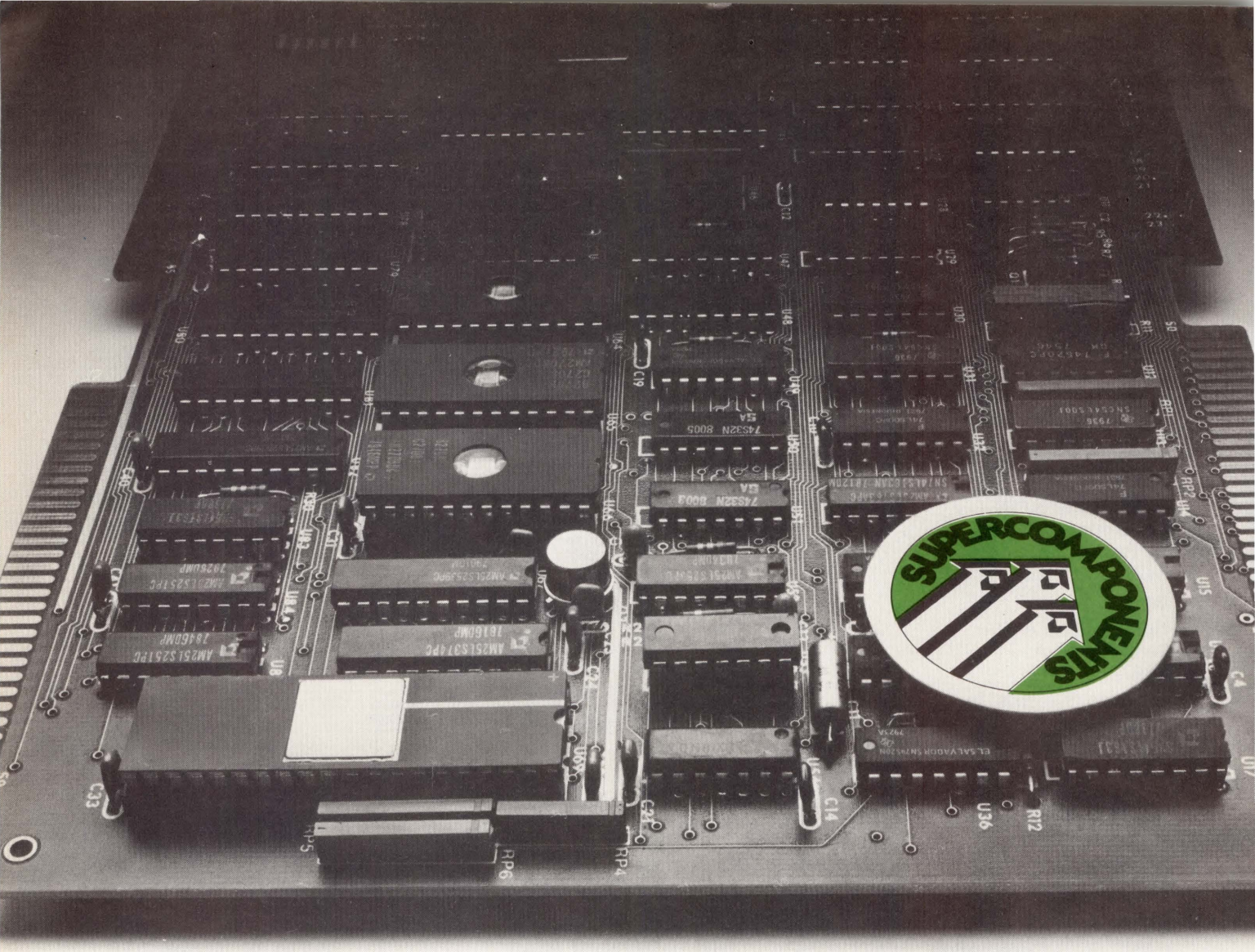



System configuration. All system functions are operational from up to eight independent control stations. Up to eight digital and eight analog system buses allow simultaneous monitoring/testing of multiple data circuits

Among the system options are provision for manual patching; a disc-stored data base for preprogrammed instructions for multiple frontend sparing or for random and/or sequence line transfer; a hard copy audit trail printer for recording all transactions; and interactive test capability using diagnostic test equipment such as the company's EXPLORER[R] family.

A 64-line MASS+ system is housed in a standard 19" (48.3 cm) computer grade cabinet 70" (178 cm) tall. Price ranges from $250 to $600/line, depending on selected options; delivery, 90 to 120 days. Circle 520 on Inquiry Card

*(continued on page 36)*




# You're only as smart as your next floppy disk controller.

Your new design is a work of genius. Why ruin it with a dumb floppy disk controller? Or one with half a brain? Get a Supercomponent.

## Announcing the Am95/6120. The world's smartest floppy disk controller.

The Am95/6120 has its very own 8085A. That's the most powerful CPU on any floppy disk controller board. It'll take a real load off your system's CPU.

And the Am95/6120 has more than brains. It has brawn too. It can handle up to four 8-in. or 5½-in. floppy disks. It can do double density, as well as single. One side or two.

No other floppy disk controller in the industry even comes close. Except one.

## Meet the Am95/6110.

It has the same brain as the Am95/6120. But a little less brawn.

It drives up to four 8-in. floppy disks. Single density only. Single or double sided.

Both Supercomponents offer you 20-bit address space, an Am9517 DMA, automatic check on startup, and automatic system boot. Both work like a charm with 8-bit and 16-bit systems.

## This is a job for Supercomponents!

The Am95/6120 and Am95/6110 are the newest members of our Supercomponent family.

Supercomponents are LSI-intensive boards built to save the serious designer a whole lot of time and money. They are changing the make-or-buy rules. Here's why:

Supercomponents are absolutely state of the art. They are designed in like components and they think like VLSI. All are plug-in ready. All are iSBC80 compatible and have a Multibus.* And, of course, we have a complete family of CPU boards, peripherals, enclosures, power supplies, card cages, and software.

If you're thinking about buying a floppy disk controller, call Advanced Micro Devices and get the floppy disk controller that thinks. Get a Supercomponent.

*iSBC and Multibus are trademarks of Intel Corp.

**Advanced Micro Devices**

901 Thompson Place, Sunnyvale, CA 94086, (408) 732-2400

## Joint Development Produces Fiber Optic Interface System

| SE 4352 With: | P-140 Distance* | PIR-140 Distance* | Data Rate* (Megabits/s) |
|---|---|---|---|
| SD 4323 | 5 m | 15 m | 1.0 |
| SD 4478 | 15 m | 30 m | 30.0 |
| SD 4324 | 10 m | 30 m | 0.1 |

*Distances and data rates shown are maximum values

Standardized components for a fiber optic system called the HDC interface together form an economical data link suited for short distance (to 30 m), medium speed (to 30M bits/s) applications. The components are the result of a joint development by three companies. Semiconductor light sources and detectors are from Honeywell Inc, Spectronics Div, 830 E Arapaho Rd, Richardson, TX 75080; Pifax plastic core cables used in the link are from Du Pont Co, Wilmington, DE 19896; and standard electrical connector hardware adapted for fiber optic cable termination is by ITT Cannon Electric Div, 666 E Dyer Rd, Santa Ana, CA 92702.

Components for the link—emitters, receivers, connectors, cables, and prefabricated harnesses—may be purchased separately from the respective companies for customer assembly. The assembled HDC interface data link will be available from ITT Cannon.

Low cost repackaged versions of the Sweet Spot™ LED emitters, and three photodetectors from Spectronics are compatible with the HDC interface. SE 4352 LED uses a glass bead lens on top of the chip to collimate emitted IR light into a 300-$\mu$m diameter spot of high radiance optical energy. This allows coupling of from 750 to 1000 $\mu$W optical power into the fiber.

Three optical receivers are available: SD 4323 for dc to 1M bits/s; high sensitivity SD 4478 PIN for speeds to 30M bits/s; and a Schmitt detector SD 4324 that includes onchip signal conditioning for TTL/CMOS compatibility from dc to 100k bits/s. The emitters and receivers were designed to interface with Du Pont Pifax P-140 Type B and PIR-140 Type B cables. Packages couple efficiently with ITT Cannon connectors.

Pifax P-140 and PIR-140 cables were designed to fit the 50-mil (1.27-mm) spacing of the Cannon standard microminiature connectors. The cables' high numerical aperture (NA) provides high coupling efficiency to the 300 $\mu$m light spot from the emitters. The chart shows distances achievable by the two cable types used in conjunction with the SE 4352 LED and the three detector types. Maximum attenuation of the P-140 cable at 650 nm is 385 dB/km; that of the PIR-140 is 320 dB/km at 690 nm. The flexible cables can withstand 25 kg tensile force in installation and use and can be subjected to the same tight bend environments as wire.

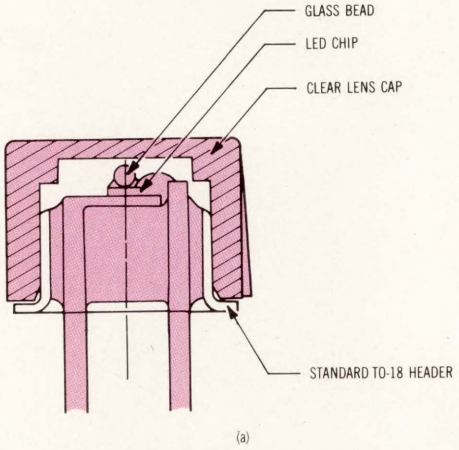
A fiber to diode connector by ITT Cannon links emitters/receivers to the fiber cable, and also can terminate the cable with the company's series MDM miniature connectors. The all-metal diode connector positions and maintains the terminated fiber end in alignment with the cap of the TO-18 diode package. The ability to also terminate the fiber into the MDM series environmental connectors provides both electrical and fiber optic compatibility within a single harness/connector combination for board to board or cabinet to cabinet OEM applications.

Spectronics: Circle 521 on Inquiry Card

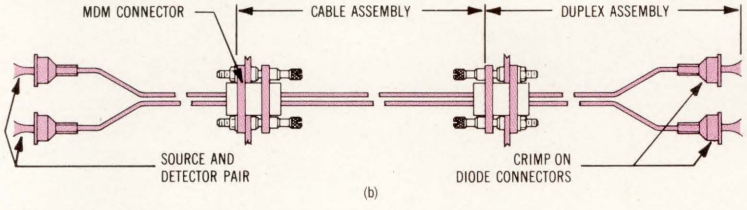
Du Pont: Circle 522 on Inquiry Card

ITT Cannon: Circle 523 on Inquiry Card

*(continued on page 40)*




Cross section of Sweet Spot LED. Fiber can be butted directly against device window. Standard LED requires pigtail connection, resulting in greater losses




Typical link configuration. Two-channel (duplex) link incorporates two emitters, two detectors, fiber cable, four diode connectors, and two miniature connectors

# Finally, a CPU that minds its own business.

# Announcing the HP 1000 Separate I/O processors let the

Our new HP 1000 L-Series is designed to give you outstanding processing performance—even in the most demanding applications.

The reason is our innovative distributed intelligence architecture. Each I/O interface has its own processor—made with our exclusive SOS LSI process—and its own direct memory channel. Which means each interface can control and monitor data transfers—without interrupting the central processor.

So the CPU can concentrate on its main job of computation.

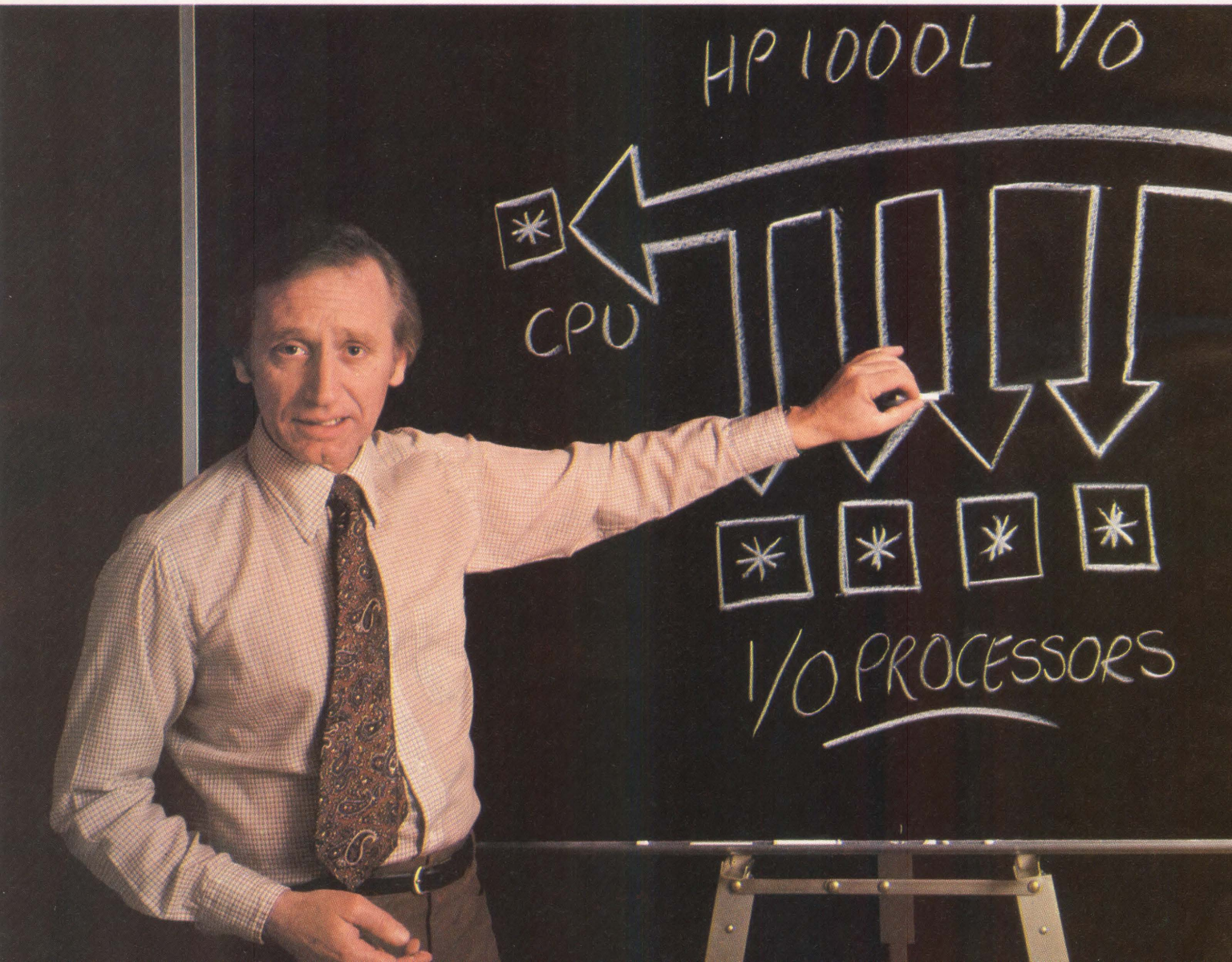
And you get faster response, higher throughput and superior system performance.

But what's really surprising about the L-Series is that you get all this performance at prices that start as low as $1968 for our starter set.† Or $15,510 for a complete disc-based system.††

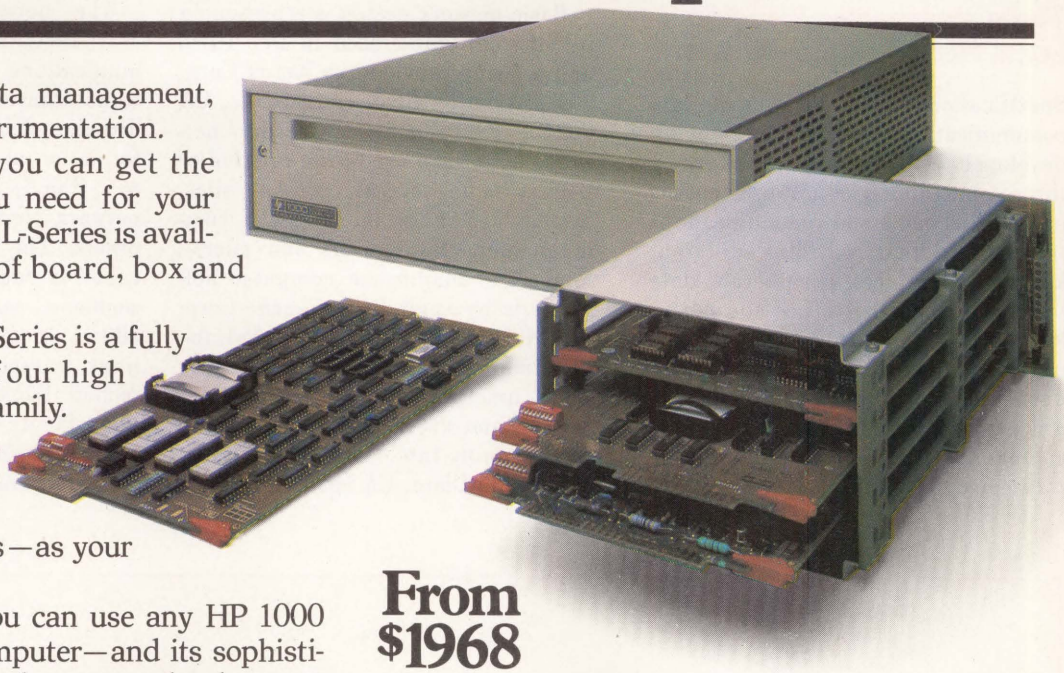
## Nobody makes processors like we do.

The key to the HP-1000 L-Series' impressive new architecture is our own Silicon-On-Sapphire technology. SOS lets us make CPU and I/O chips with extremely high circuit density, low power consumption, high processing speeds and high reliability—at a very low cost.

It's this combination of high performance and low cost that make the L-Series appropriate for the whole range of OEM and industrial appli-



# L-Series Computer. CPU concentrate on computation.



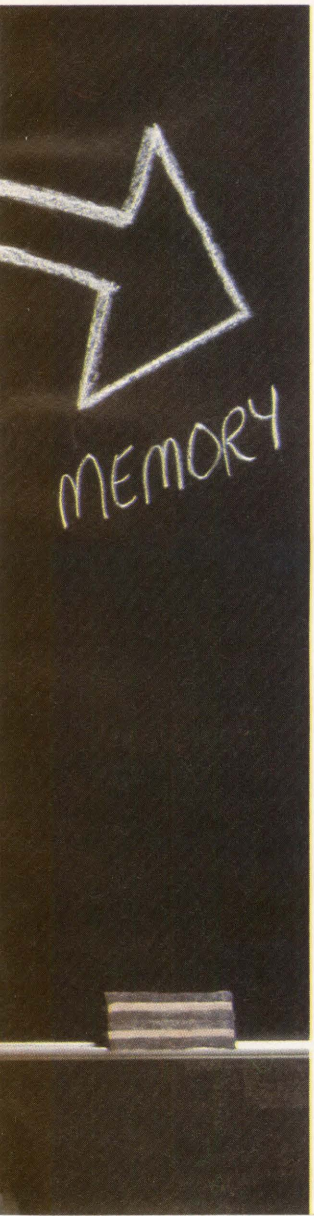
cations — including data management, process control and instrumentation.

And to insure you can get the exact configuration you need for your specific application, the L-Series is available in a wide choice of board, box and system packages.

The HP 1000 L-Series is a fully compatible member of our high performance HP 1000 family. Which means you can move up to a larger computer—all the way to our powerful F-Series—as your application grows.

It also means you can use any HP 1000 computer—and its sophisticated program development tools—to design programs for the L-Series.

**From $1968**




## The reliability is built in.

Like all HP computers, the HP 1000 L-Series is designed to give you outstanding reliability. Reliability that's significantly enhanced by our SOS technology — processor boards have fewer active parts, so fewer things can go wrong. In addition, the L-Series has its own self-test programs and diagnostics.

And, of course, the L-Series is backed by our full range of support and documentation services—including our worldwide service network.

For more information or a hands-on demonstration of our high performance, low cost L-Series, contact your nearest HP sales office listed in the White Pages or write to: Roger Ueltzen, Dept. 1273, 11000 Wolfe Road, Cupertino, CA 95014.

*†Starter Set: CPU, 64KB memory, one I/O board.*
*††Disc-Based System: HP's new 12MB Winchester disc drive and 2621 display console.*
*(U.S. OEM prices in quantities of 100)*

HEWLETT PACKARD

CIRCLE 20 ON INQUIRY CARD

22002HPDS30

## Three Companies Develop Local Network Specifications

Specifications for a local area data communications network are being developed in a major joint effort by three companies. The network consists of a coaxial cable and communications transceivers that will link different kinds of computers, peripherals, data terminals, and other office equipment located in a building, or in a complex of closely grouped buildings. Each device connected to the cable will have a control element that will allow it to communicate on the cable through its transceiver.

Basic network design is represented in Ethernet (announced in Dec 1979) and is being provided by Xerox Corp, 701 S Aviation Blvd, El Segundo, CA 90245. Experimental Ethernet networks have been used over a period of five years in several company sites. System design in the areas of communications transceivers and micro-, mini-, and mainframe computer networks is by Digital Equipment Corp, 146 Main St, Maynard, MA 01754; the partitioning of complex communications functions into microcomputer systems and VLSI components is being carried on by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051.

The network (*Computer Design*, Mar 1980, p 42) is a passive communications medium that simply accepts transmissions from computers, distributed peripherals, and other information processing devices attached to it (Fig 1). Failure of any one of the network elements does not affect the others. The 50-Ω terminated coaxial cable is made up of one or more segments, each of which can be up to 500 m in length, and a communications transceiver for each device attached. Each device has a control element for its own transceiver. Multiple cable segments may be interconnected in configurations (yet to be determined), provided that no two hosts are separated by more than 2500 m. Manchester channel encoding is to be used, and channel data rate is 10M bits/s.

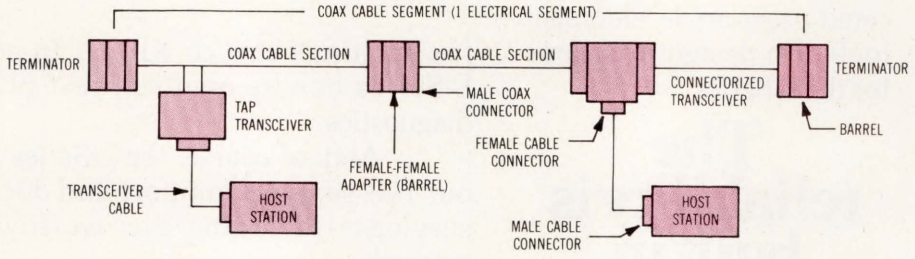



Fig 1 Transmission system components. Coax cable insulation and shielding must be appropriate to installation environment. Transceiver to coaxial cable connection is via cable "tap" (to be determined), with up to 128 transceivers per cable segment. Each transceiver monitors cable before transmission to be sure it is clear, and during transmission to detect interference. If interference is detected, packet is retransmitted when cable is clear

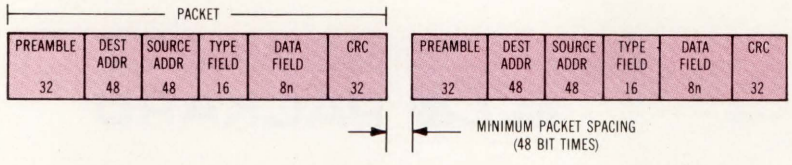
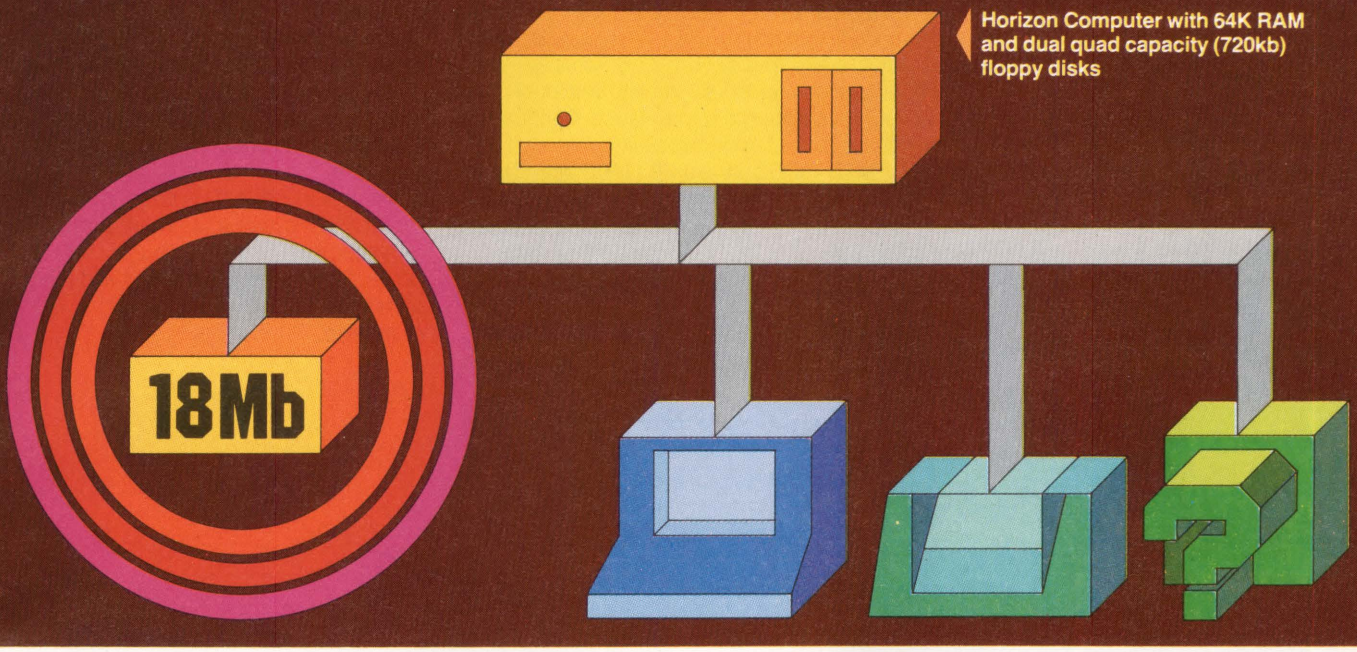



Fig 2 Packet format. 32-bit cyclic redundancy check (CRC) protects destination, source, type, and information fields. Minimum packet spacing provides time for receivers to reset

Information is transmitted in packets, which contain the data to be sent, the destination address, and the source address. Packet format is shown in Fig 2. The preamble enables bit synchronization and marks packet boundary. Destination address is a 48-bit field with $2^{47}$ physical addresses, one broadcast, and $2^{47}-1$ multicast group addresses. The source address is in the same format as the destination address. The 48-bit address field permits flexible assignment of addresses,

*(continued on page 44)*

# New on the North Star Horizon:
# 18Mb Hard Disk Drive!




Up to four 18Mb Winchester-type hard disk drives

Display terminal

Letter-quality or dot matrix printer

Horizon I/O flexibility allows expansion to meet your needs

**Unsurpassed Performance and Capacity!**

North Star now gives you hard disk capacity and processing performance never before possible at such a low price! Horizon is a proven, reliable, affordable computer system with unique hardware and software. Now the Horizon's capabilities are expanded to meet your growing system requirements. In addition to hard disk performance, the Horizon has I/O versatility and an optional hardware floating point board for high-performance number crunching. The North Star large disk is a Century Data Marksman, a Winchester-type drive that holds 18 million bytes of formatted data. The North Star controller interfaces the drive(s) to the Horizon and takes full advantage of the high-performance characteristics of the drive. Our hard disk operating system implements a powerful file system as well as backup and recovery on floppy diskette.

**Software Is The Key!**

The Horizon's success to date has been built on the quality of its system software (BASIC, DOS, PASCAL) and the very broad range and availability of application software. This reputation continues with our new hard disk system. Existing software is upward compatible for use with the hard disk system. And, with the dramatic increase in on-line storage and speed, there will be a continually expanding library of readily available application software. For further information, contact the OEM sales department at North Star Computers,Inc.

**North Star OEM Prices**

**HORIZON-HD-18**
Horizon computer with 64K RAM, 2 quad capacity mini drives and one HDS-18 hard disk drive **$5880***

**HDS-18**
Additional 18Mb hard disk drive for expansion of Horizon HD-18, or your present Horizon **$3150***

*in OEM quantities

NorthStar

North Star Computers, Inc.
1440 Fourth Street
Berkeley, CA 94710
(415) 527-6950 TWX/Telex 910-366-7001



CIRCLE 21 ON INQUIRY CARD

# Ideals tell you to design for performance. STC's product plan

Balancing your I/O performance objectives against your company's cost objectives can be a vexing challenge. STC is ready to help you resolve the dilemma with the most comprehensive offering of tape subsystem products and capabilities ever offered to the OEM.

**Improving Performance**

The 1900 Tape Family provides a choice of 9 basic subsystem configurations. So you can pick the precise combination of speeds, densities and features to complement your processor and your customers' applications. The chart on the right will help you start sizing up the appropriate model.

In demanding processing environments GCR (6250 bpi) is the obvious choice. For example, a GCR tape drive can handle a 100 Mbyte disk dump/restore with a single reel in as little as 4 minutes. (Compared to 4 reels and 20 minutes for PE.) On long sequential files, a 125 ips GCR drive will actually outperform most disk drives. Best of all, GCR performance comes with a significant bonus in read/write reliability.

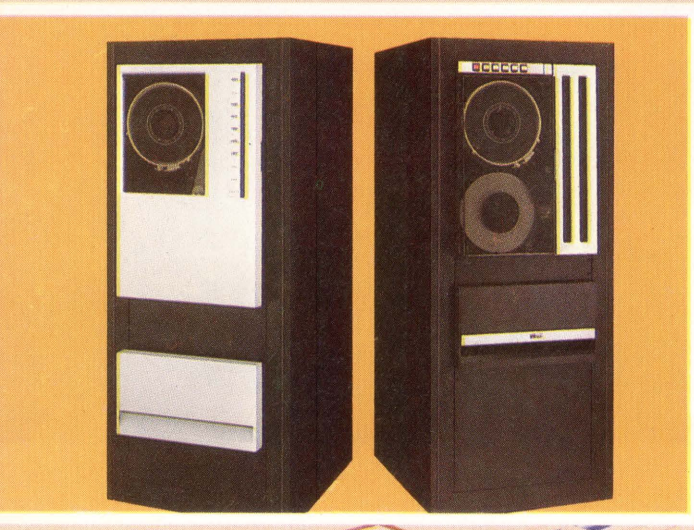
NRZI (800 bpi) and PE (1600 bpi) give your customers the ability to process archival data and to exchange information with systems lacking GCR capability. STC's 1953 lets you handle all three of these popular formats in a single drive/single formatter configuration.

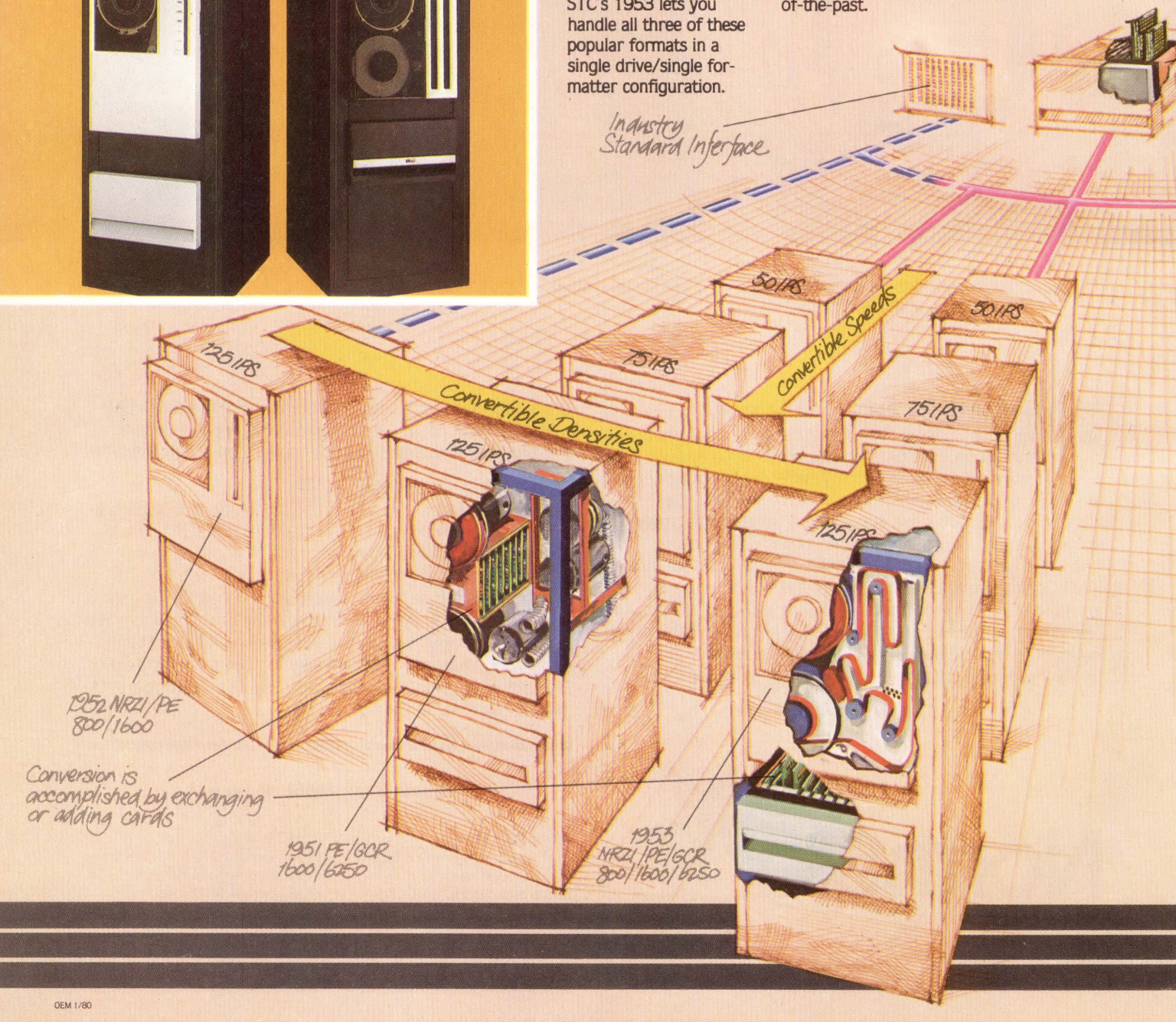
**Controlling Factory Costs**

If your company markets a line of systems to meet a variety of customer requirements, the STC 1900 can simplify your engineering and cut your costs.

The 1935 Formatter/Control Unit will handle up to four 1950 and 1920 Series Drives, intermixed in any combination of speeds and densities. That means a single hardware interface and a single set of operating system drivers and utilities can accommodate all the configurations in your marketing mix.

More good news. The seven 1950 Series Drives models have a 90% plus parts commonality. The same is true of 1920 Series Drives. So training is simplified and spare parts headaches are a thing-of-the-past.





# Practicality says design to cost. gives you both.

And for the ultimate in flexibility, 1900 subsystems provide a convenient growth path. With a few simple card changes, your field engineers can convert speeds and densities, on-site, in a matter of minutes.

**Containing Service Costs**

To assure fast, effective field service, STC provides you with the most comprehensive diagnostics in the industry. The 1900 Diagnostic Software features more than 180 routines including functional, reliability and artificial stress testing. Field experience has shown the package will deliver 95% fault detection and 70% isolation to one of three cards.

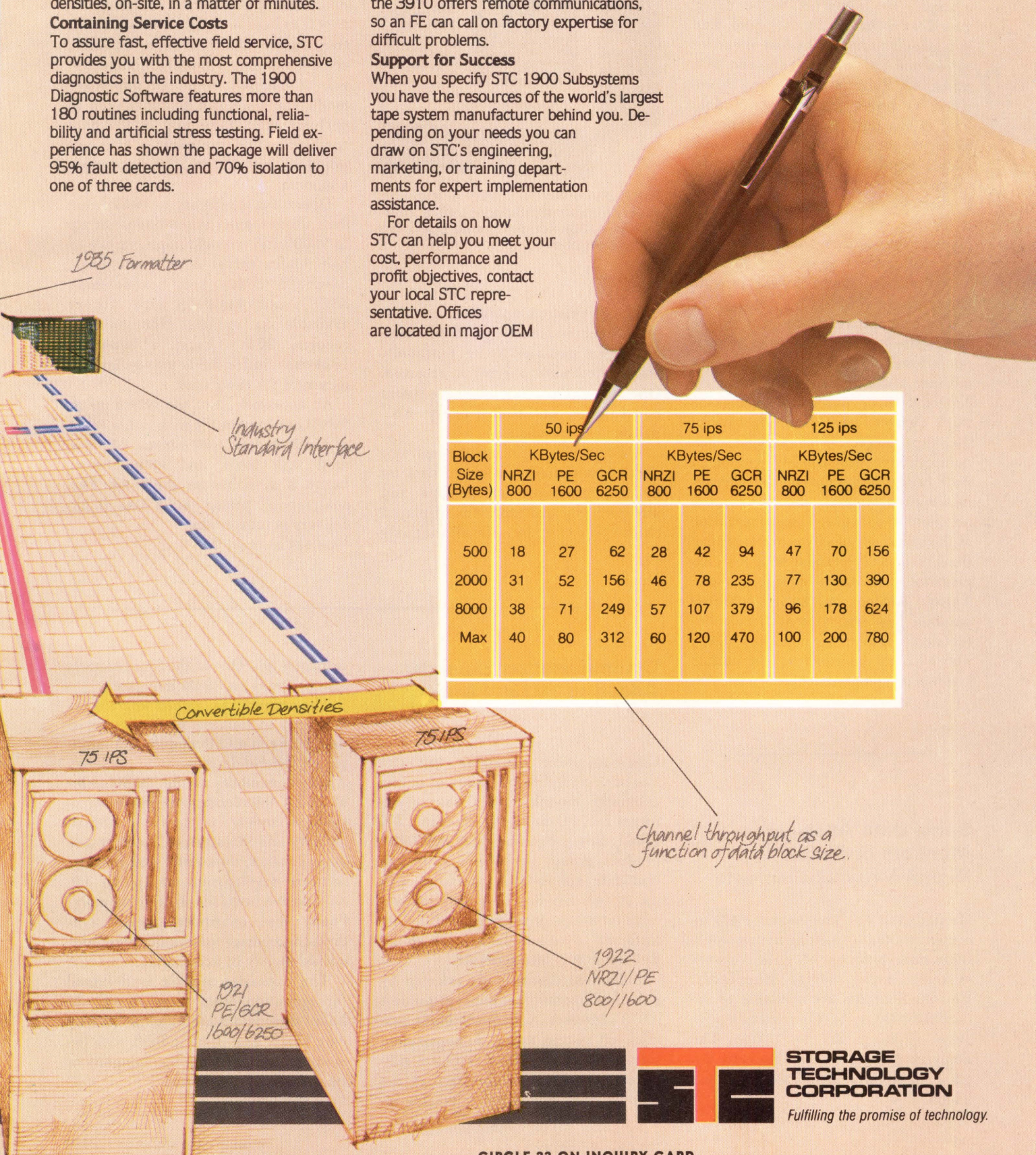
Your field engineers can run these routines on-line via the customer's processor or off-line via STC's 3910 Diagnostic processor. In addition to its powerful local capability, the 3910 offers remote communications, so an FE can call on factory expertise for difficult problems.

**Support for Success**

When you specify STC 1900 Subsystems you have the resources of the world's largest tape system manufacturer behind you. Depending on your needs you can draw on STC's engineering, marketing, or training departments for expert implementation assistance.

For details on how STC can help you meet your cost, performance and profit objectives, contact your local STC representative. Offices are located in major OEM centers around the world.

Or write Storage Technology Corp., P.O. Box 6, 2270 S. 88th Street, Louisville, CO 80027. Phone (303) 673-5151.




| Block Size (Bytes) | 50 ips KBytes/Sec NRZI 800 | PE 1600 | GCR 6250 | 75 ips KBytes/Sec NRZI 800 | PE 1600 | GCR 6250 | 125 ips KBytes/Sec NRZI 800 | PE 1600 | GCR 6250 |
|---|---|---|---|---|---|---|---|---|---|
| 500 | 18 | 27 | 62 | 28 | 42 | 94 | 47 | 70 | 156 |
| 2000 | 31 | 52 | 156 | 46 | 78 | 235 | 77 | 130 | 390 |
| 8000 | 38 | 71 | 249 | 57 | 107 | 379 | 96 | 178 | 624 |
| Max | 40 | 80 | 312 | 60 | 120 | 470 | 100 | 200 | 780 |

Channel throughput as a function of data block size.

STORAGE TECHNOLOGY CORPORATION

*Fulfilling the promise of technology.*

CIRCLE 22 ON INQUIRY CARD

operation of equipment of different manufacture on the same network, and prevents address duplication.

A 16-bit field designates types of protocol; its format is to be determined, as is that of the data field. End of packet is indicated by loss of carrier within one bit time after the last data transition. Runt packet filtering is provided to reject packets whose data field is less than a certain number of bytes, as yet to be determined. Total packet length must be greater than the round trip time through the network. Packets shorter than this are assumed to be the result of a collision. Link management is by contention arbitration with carrier sense and collision detection. The network will provide Datagram service.

The cooperative efforts of the three companies has resulted in the general operational objectives for the network outlined above. Full specifications are expected to be published during the third quarter, 1980. One objective of the joint project is to provide communications compatibility among a wide range of computers, peripherals, information systems, and office products, and to encourage implementation of the specifications by other organizations, especially standards groups expressing interest in adopting them. Xerox, holder of basic Ethernet patents, has said it will license interested companies, including those who wish to manufacture compatible systems or components.

## Serial Data Analyzer Monitors or Simulates Digital Network Elements

Menu-driven analyzer model 1640B incorporates features to further simplify functional analysis of data network systems using serial interfaces. Retrofit field kits are available to update HP 1640A units (*Computer Design*, June 1978, p 22) to 1640Bs. The analyzer is from Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304.

Patch panel matrix adapts analyzer to variety of system interfaces. HP-IB interface is option for automated operation under control of computer controller

The simulation operation now has two branching modes that allow a user-generated message to be repeatedly transmitted until a reply is received. One of two remaining messages is sent contingent on the "reply on" parameters specified.

A memory bit shift lets the operator check transmitted or received data bit by bit, or locate clock slips and unknown sync patterns. Any displayed character can be simultaneously decoded in binary, octal, hexadecimal, and the displayed code. Clock accuracy has been improved to ±0.01%.

In passive mode, the instrument is a nonintrusive monitor on the serial RS-232-C/V.24 lines in a digital network with five trigger modes: 8-char sequence, control line, error pattern, time interval, or external event. In the active mode, the 1640B can be configured to perform as a major unit of the data communication network: CPU, terminal, or, with the RS-232-C connection, a modem.

Operating speeds are to 19.2k bits/s (half duplex only) synchronous, or up to 9600 bits/s asynchronous, in full or half duplex across 2- or 4-wire links. Standard codes are hexadecimal, ASCII, and EBCDIC, with others available as options. The memory records 2048 chars; a separate 1024-char buffer holds user-generated messages for simulation.

All accessories but the 10291A menu P/ROM are compatible with either 1640A or 1640B models. 10291A menu P/ROM is used with 1640A, and menu P/ROM 10291B is available for the 1640B. The analyzer is priced at $5800 (U.S.); delivery is four weeks.

Circle 524 on Inquiry Card

## Communication Expander Added to TM990 Family

Communication expander TM990/307 has been added to its family of microcomputer modules by Texas Instruments Inc, PO Box 1443, Houston, TX 77001. Bus compatible with the TM990 product group, the device can communicate via RS-232-C interfaces with up to four synchronous or asynchronous terminals or modems. Parallel interfacing to an autodialer such as the Bell 801 ACU is also possible.

Individual channels are selected by means of communications register unit (CRU) addresses. A loopback mode permits self testing with a demonstration software package. Baud rates are software programmable, and each of the four channels has switch-selectable interrupt levels. One of the four channels also provides an RS-422 interface.

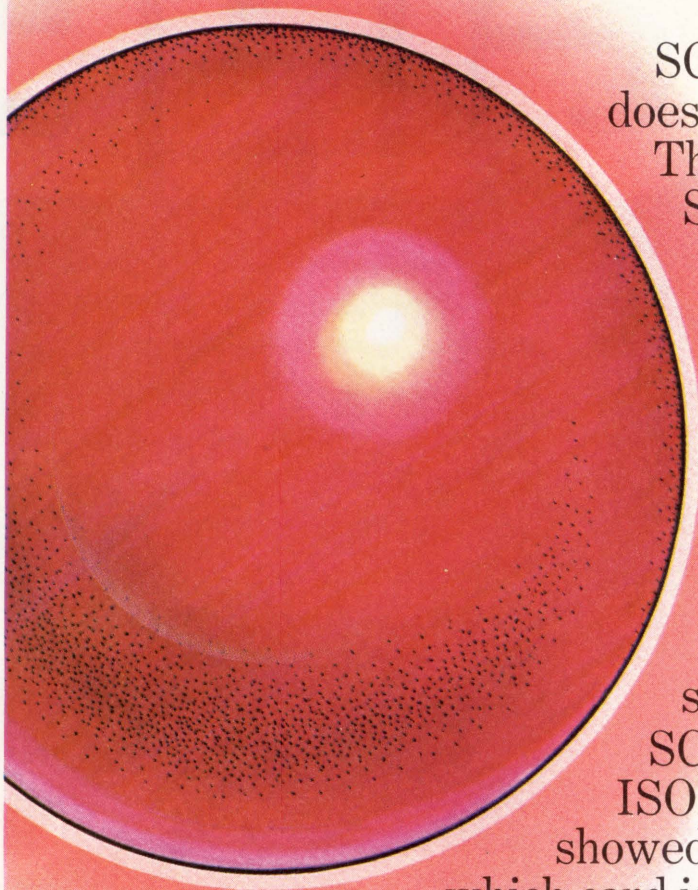
The expander is applied where there is a need to transmit or receive serial data between a CPU module and multiple peripheral devices.

Other members of the TM990 series of 16-bit microcomputer modules include complete CPUs with onboard memory and I/O interface, memory and I/O expansion, data entry and display, software development, ac and dc I/O, A-D and D-A interface, bubble memory, floppy disc controller, speech synthesis, industrial communications, and a wide variety of accessories.

The expander module is designed for operation from 0 to 70 °C. PC board dimensions are 11 x 7.5" (5.9 x 4 cm). Single unit price is $650, with immediate delivery from the company or its authorized distributed. □

Circle 525 on Inquiry Card

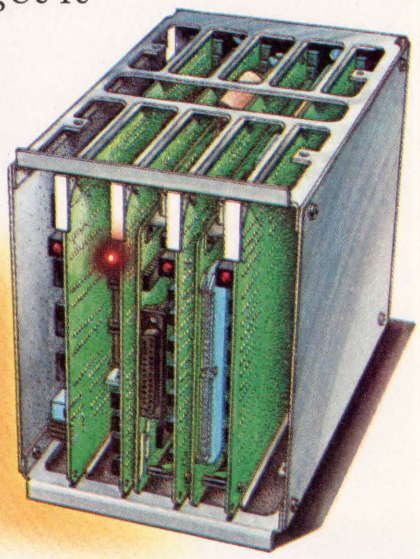
# See SCOUT save.



SCOUT™ has a red light. It does not mean what you think. The red light says one of SCOUT's boards does not feel well.

Will this make you sad because your minicomputer can't play anymore? Will the expensive repairman take a long time to get it fixed?

No no, silly. Since SCOUT's ISOLITE™ showed you which card is bad, all you do is pull it out and put in a spare 6.25″ x 8.3″ card.



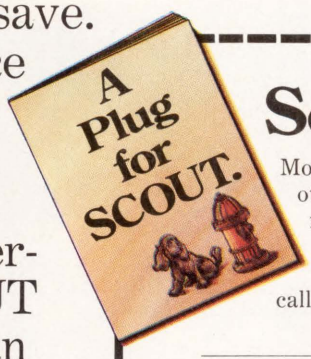
What fun! Now SCOUT can run and play again. And save you a lot of jack.

Save SCOUT, save.

Save on service costs. Save on system costs.

Save on 16-bit minicomputer performance. SCOUT starts at less than $1000 for a CPU, I/O, 32K Byte RAM and card cage.

Isn't saving fun? Save SCOUT, save.




## See SCOUT save.

Money.Time. And end user aggravation. Plus other ways to save in our how-to-save-on-maintenance primer, *A Plug for SCOUT.* Get your free copy with this coupon and a business card. Or, for immediate information call 714/833-8830, Ext. 455.

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CIRCLE 23 ON INQUIRY CARD

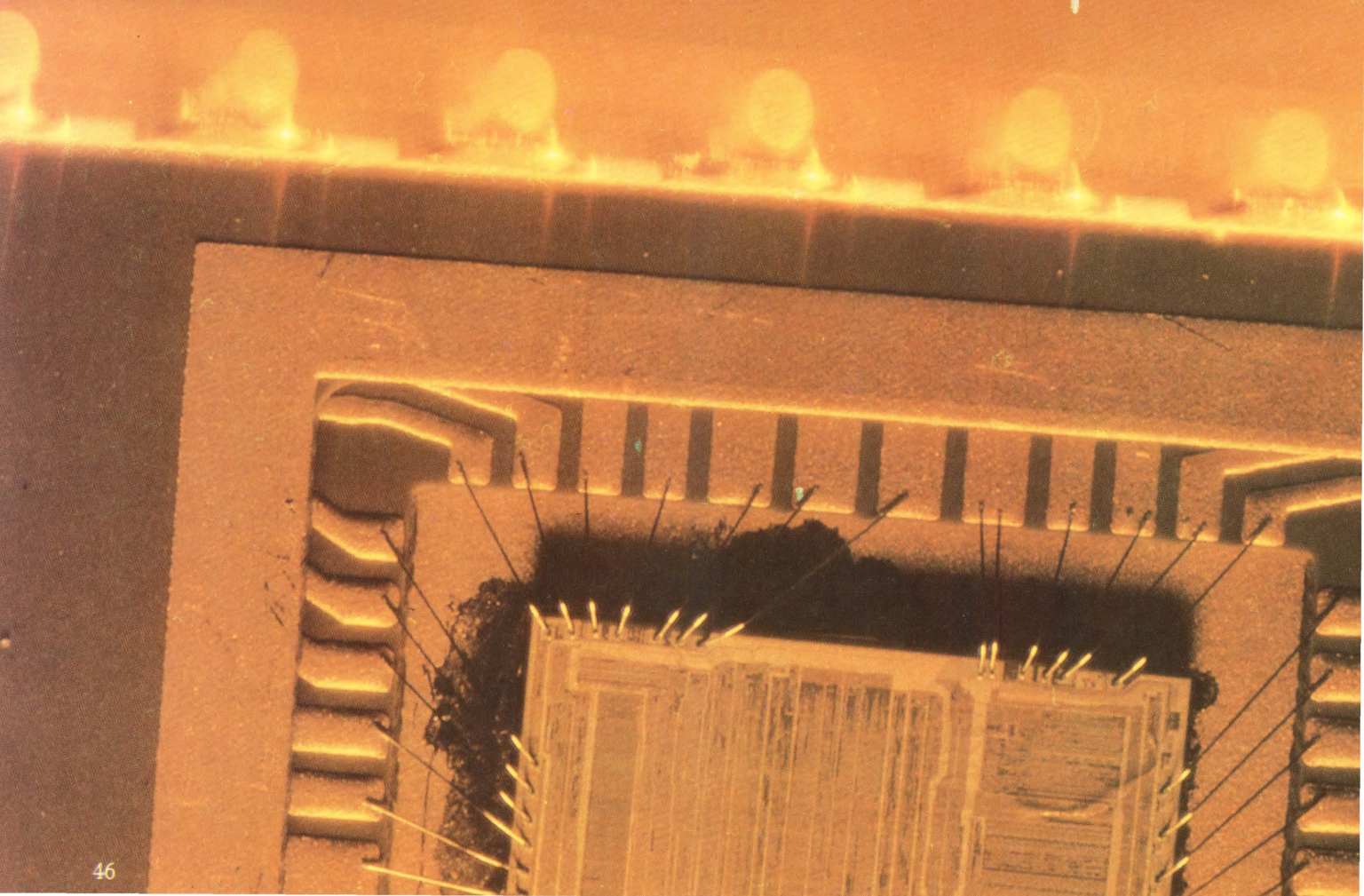
# IMAGINE

As your ideas race into the future, you need products to match your stride. Today Zilog offers you the most advanced family of microprocessor products made: components, support devices, software, development systems. All available in production quantities with worldwide support.

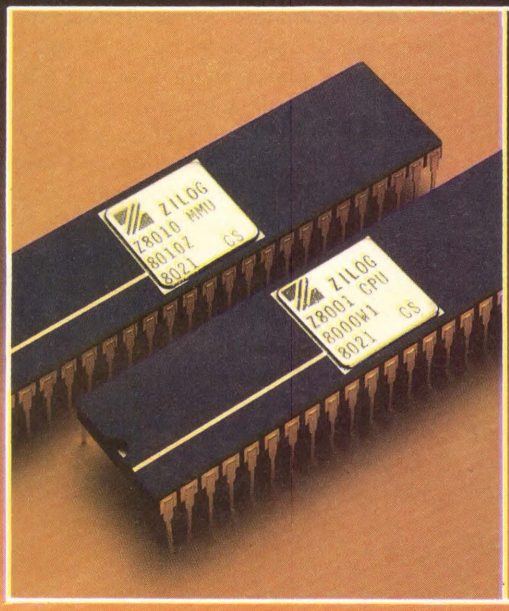
Elegant but soundly conservative scaled n-channel manufacturing processes combine with generation-ahead architecture to give Zilog products uncommon performance levels. The 8-bit Zilog Z80 revolutionized the microprocessor industry.

Today it's become the still more powerful Zilog Z80B. Its cousin, the Zilog Z8, packs an ingeniously flexible, complete 8-bit microcomputer onto a single chip. And, as you would expect, the incredible 16-bit Zilog Z8000 has set the microprocessor performance standards for the 1980's.

Give your imagination some of our hard, profitable facts to work with. Write: Zilog, Dept. E, 10460 Bubb Road, Cupertino, CA 95014. Or, call your nearby Zilog distributor.



# THE POWER TO DESIGN THE MOST ADVANCED MICROPROCESSOR-BASED SYSTEMS IN THE WORLD. AT YOUR COMMAND TODAY. FROM ZILOG.




JULY 1980:

## The Zilog Z8010 Memory Management Unit unfolds the next phase of the Z8000 concept.

With the advent of the Zilog Z8010 Memory Management Unit (MMU), each of the 128 memory segments of the 8M-byte Z8001 microprocessor can now be given its own broad range of programmed characteristics. Sophisticated data and program storage management is now possible, opening up new vistas for advanced systems design.

Zilog

An affiliate of EXXON ENTERPRISES INC.

CIRCLE 24 ON INQUIRY CARD

## 32-Bit Superminicomputer Runs Both 16- and 32-Bit Code

The 32-bit ECLIPSE[R] MV/8000 is a compact superminicomputer based on VLSI technology that bridges the gap between 16- and 32-bit word programs to offer orderly transition from 16- to 32-bit computer systems. Announced by Data General Corp, Rt 9, Westboro, MA 01581 in response to increased application demands from users requiring performance and data handling power, the system features virtual address space of 4.3G bytes and user address spaces of up to 512M bytes each, built-in diagnostic processor, and hardware supported 8-ring security and protection mechanism.

Programmed array logic and VLSI technology reduce components allowing the the CPU to be implemented on five boards. The system consists of four major subsystems: CPU, memory, system control processor, and I/O system. The three separate processors supporting these subsystems—central processor, system control processor, and I/O processor—allow management of intelligence as close to the source as possible. This increases performance and minimizes data movement and system overhead. A series of high speed buses maximize processor throughput. These with the system's combination of instruction and system caches provide a memory system throughput rate of 36.4M bytes/s with I/O to memory and CPU to memory transfer rates of 18.2M bytes/s.

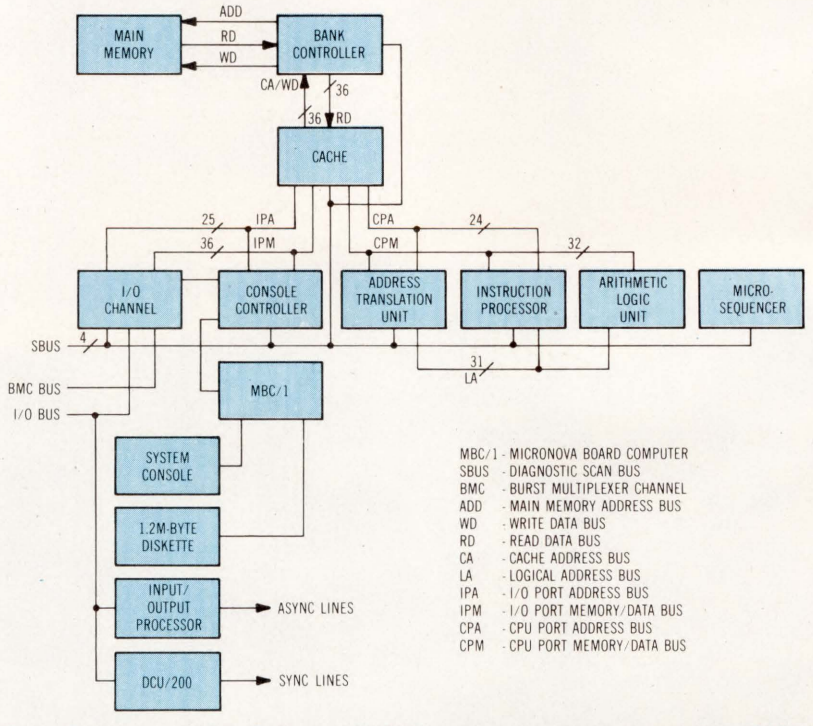
The CPU's 4-stage implementation allows instructions to be fetched, decoded, and executed simultaneously. A 1k-byte instruction cache in the CPU uses a lookahead lookback technique to increase speed. A RAM based microsequencer contains the memories that form the control store for microcode. Built around bit slices, the 32-bit ALU performs complex operations in a minimum of cycles. One section of the ALU operates on the exponents found in floating point numbers and the other works with floating point mantissas, fixed point quantities, and addresses.

Reliability and efficiency of the system's memory are enhanced by incorporation of an error detection and correction mechanism called "sniffing." This technique consists of the bank controller reading one double word from each RAM row as it is refreshed or recharged. (The bank controller is the interface between system cache and memory modules.) The double word goes through a complete error detection and correction check and is returned to the memory module. Because the operation is performed on a different double word during each refresh, the entire contents of memory are checked and corrected if necessary every 4 s.

Memory modules are available in increments of 256k bytes up to 2M bytes maximum, and are organized as 64k double words of 4 bytes each. Seven additional bits stored with each double word provide error checking and correction facilities; 4-way interleaving offers maximum performance. Data transfer between memory modules and system cache at a 36.4M-byte/s rate is possible because of overlapping of memory operations.

The 16k-byte system cache acts as a high speed buffer between memory modules and the rest of the system, reducing the time needed by both CPU and I/O system to access memory.

*(continued on page 48b)*




Data General's 32-bit Eclipse MV/8000 computer system supplies 512M characters of user program address space and main memory bandwidth of 36.4M characters/s. Machine uses a microprogrammed processing unit, block oriented memory system with 16k-byte cache, and independent I/O system, and provides integrated microcomputer based diagnostic capability for comprehensive system control and error diagnosis

# DEC PDP-11 TAPE USERS

## *NO WAITING . . .*

## For the first embedded single board Magnetic Tape System Controller

Datum's new PDP-11 software compatible single board design, Model 1520 Embedded NRZI Tape Controller offers you more for less. And we're delivering them right now.

More versatility; occupies a single HEX SPC slot or comes with its own chassis, 16 bit microprocess controlled, word and or byte memory transfers with odd or even starting addresses and byte counts. TM-11 or IBM data compatibility is available. The 1520 interfaces to the Datum D450 tape drive or any industry standard tape drive (up to four can be attached). Dual Density is achieved simply by adding a second board to accommodate the Phase Encoded function. Additionally, Datum offers you Phase Encoded ID data burst detection.

And we offer you less; less initial cost*, less preventative maintenance. And you use less space thanks to Datum's advanced embedded controller design.

If you're a PDP-11 tape user and need delivery now, you owe it to yourself to learn more about Datum's more for less tape program. **For early delivery contact your local Datum representative today.**

**datum inc**

CIRCLE 26 ON INQUIRY CARD

**CORPORATE HEADQUARTERS** 1363 S. State College Blvd., Anaheim, CA 92806, Tel: 714/533-6333, TWX: 910/592-1289, Telex 68-5579 • **EUROPEAN HEADQUARTERS, DATUM (ELECTRONICS) LTD.,** DATUM House, Harlington, Middlesex, England, Tel: 01-897-0456, Telex: 935-398 • **DATUM SALES OFFICES,** CANADA, Willowdale, Ontario, Tel: 416/491-6960, Telex: 06-966857 EOR TOR: MOUNTAIN STATES, Denver Colorado 80232, Tel: 303/693-3414; EAST COAST, Mountainside, New Jersey 07092, Tel: 201/654-5590; MIDWEST, Des Plaines, Illinois 60018, Tel: 312/296-1064; SAN JOSE, San Jose, CA 95117, Tel: 408/249-5370; NEW ENGLAND, Framingham, MA 01701, Tel: 617/872-6911.

*Single board NRZI design, $3,000 Qty-1

Systems (tape drive and controller) pricing begins at $6,900 Qty-1

PPD 103

Interface between system cache and main memory transfers data at a rate of 16 bytes in 550 ns for write and 16 bytes in 440 ns for read operations.

A hardware accelerator for the memory paging system, the address translation unit maintains a table of up to 256 address translations and access privileges for recently referenced pages. The unit also generates modified and referenced bits. Modified bits signal when a page in main memory must be written back to disc because it has been modified; referenced bits indicate that the page was referenced and are used by the operating system to perform page replacement algorithms.

Made up of a high speed burst multiplexer channel, data channel, and I/O processor, the I/O system is under the control of the I/O channel board. All data transferred within this system move to or from system cache; they need not pass through or interfere with the processor. Transferring blocks of data at up to 16.16M bytes/s the BMC is a direct communications path between main memory and high speed peripherals. The data channel handles transfers between CPU and medium speed devices operating at rates up to 2.27M bytes/s. An independent processor with ECLIPSE instruction set and 64k bytes of local memory, the IOP processes and buffers data from low speed units. Acting as a frontend processor for the system, it offloads the CPU and receives terminal output from the CPU.

Designed in conjunction with the computer, the concurrently announced Advanced Operation System/Virtual Storage (AOS/VS) takes advantage of hardware architecture to manage system resources for 128 users accessing up to 512M bytes of logical address space. The software also supports simultaneous execution of 16- and 32-bit programs and can run 16-bit programs developed under AOS without modifications and with increased speed. Support software for use under AOS/VS includes three 32-bit languages that conform to ANSI standards: FORTRAN 77, PL/I, and BASIC. In addition, the operating system offers a 32-bit SWAT™ Native Language Debugger.

The intelligent multiprogramming system controls concurrent timesharing, batch, and online operations for both 16- and 32-bit processes. Working dynamically with hardware, the system operates on a demand paging basis using pages of 2k bytes. It uses a cache based hardware address translation unit to accelerate the translation of logical addresses into virtual addresses.

Segmentation of virtual memory into eight processing regions provides the hardware for an 8-ring software security mechanism. The structure permits the operating system to reside in the user's address space while protecting it from user encroachment.

Compilers include a common code generator and optimizer to select the most efficient code sequence. Common language modules are used, further increasing system reliability and maintainability.

Representative prices for the systems range from $153,150 to $504,700. On the low end the system consists of CPU with 512k-bytes memory, battery backup, system console, 8-line asynchronous modem interface, 96M-byte disc, and 800/1600-bit/ in magnetic tape. The high end system has 2M-bytes memory, and adds three 16-line asynchronous terminal interfaces, 64 CRT displays, four 277M-byte discs, magnetic tape unit, and 900-line/min printer. Deliveries are scheduled for October.

Circle 420 on Inquiry Card

## Information Processing Systems Support Multiple Hosts, Multiple Protocols

Initially available in two models, the 9200 family of microprocessor based information processing systems allows for advanced networking capabilities and modular addition of functions. Both local and remote communications in either SNA/SDLC or BSC networks are supported by the units from Harris Corp, Data Communications Div, 16001 Dallas Pkwy, Dallas, TX 75240, to enable users to change protocols with minimum effort.

Ability of the system to support concurrent communications with multiple hosts will provide a major advantage that will enable users to combine operations under one interactive system for efficient utilization of communications lines and equipment. A user with host processors in two separate cities operating in BSC or SNA will be able to communicate with the 9200, which will handle communications with each host concurrently.

Local attachment to IBM host systems is achieved via byte, block, or selector channel in 3272 or SNA mode. Remote connection uses either BSC or SDLC protocol. Speeds up to 9600 bits/s are supported by 9200 processors.

When operating in BSC protocols the 9200 will communicate over duplex or half-duplex facilities in ASCII or EBCDIC. When in the SNA/SDLC environment, the unit will be capable of local channel attachment or remote communications in half-duplex, flipflop send/receive modes.

The basic 9210 will support up to 32 devices per system with local attachment at channel speed, and remote communications up to 9600 bits/s. When upgraded to the 9220 model, this system will also support more than one host concurrently.

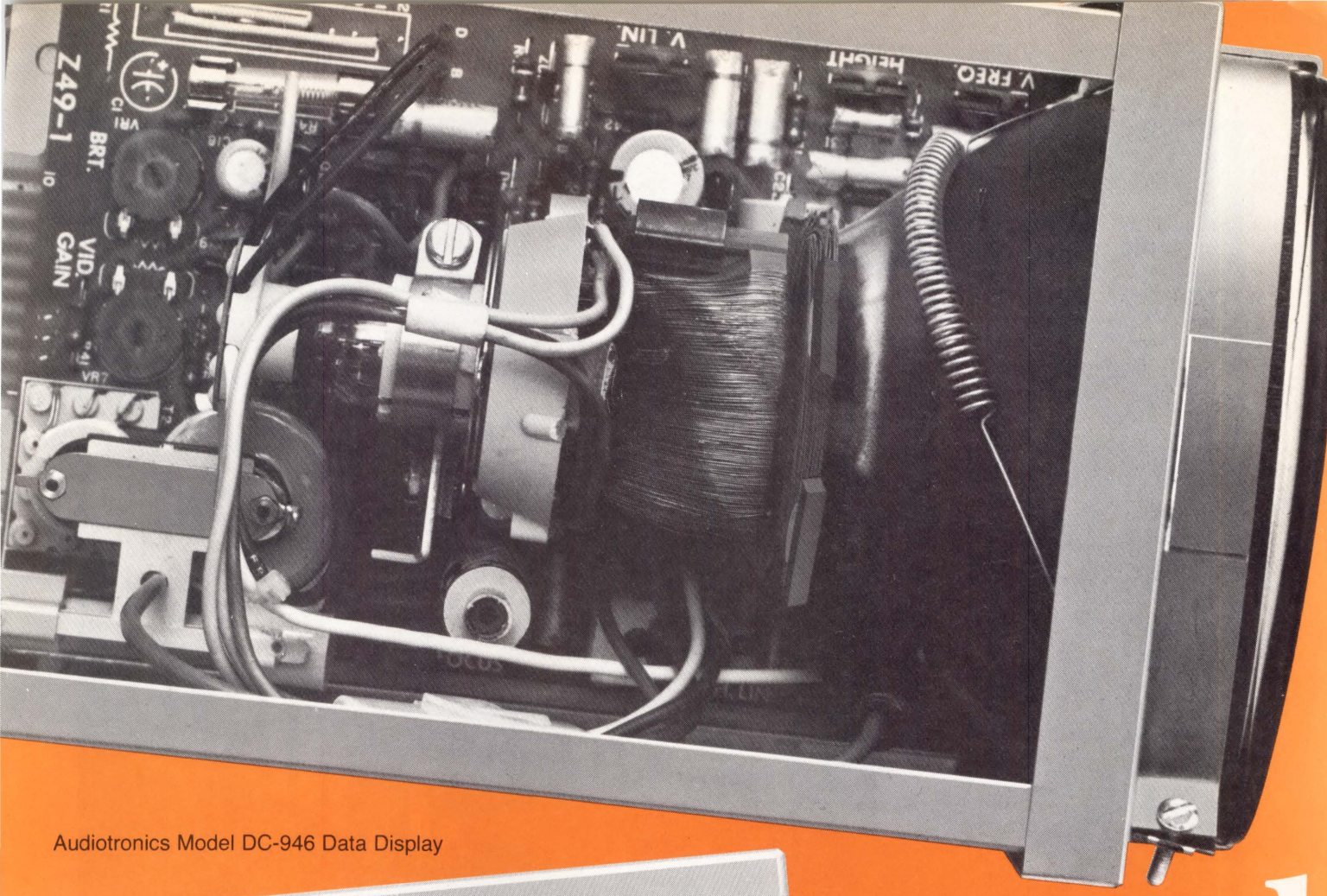
Systems are tailored to individual requirements by insertion of diskettes containing parameter definitions. This allows users to specify printer authorization, screen configuration, and number of devices, and to reconfigure the system by entering new system parameters.

Among the system peripherals are a 15″ (38-cm) nonglare CRT; keyboard configurations including 75- and 87-key data entry typewriter, and keypunch styles; and printers that include both dot matrix bidirectional and band printers. Other options include a photopen light sensor and magnetic slot reader.

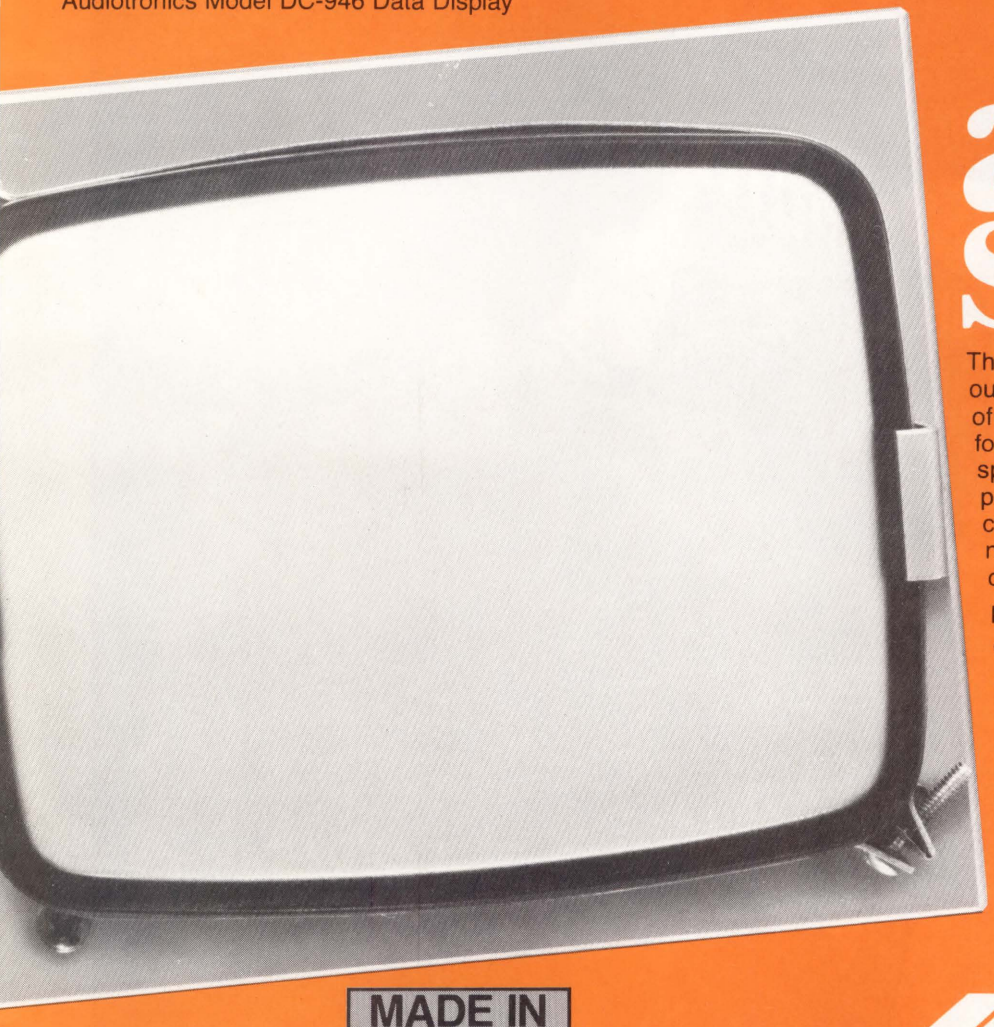
A basic 9200 system includes processor, six display stations, and one 130-char/s bidirectional printer. Purchase price is $23,306.

Circle 421 on Inquiry Card

*(continued on page 48f)*




Audiotronics Model DC-946 Data Display



# actual size

This popular Audiotronics data display is one of our 48 standard models. We have sold thousands of them to giants in the industry. Maybe it's perfect for your requirements. If not, talk to us about your specifications. We're dedicated to innovative product design, quality production standards and complete customer satisfaction. Whatever you need, we have the experience and talent to design it, or improve it. Contact us today.

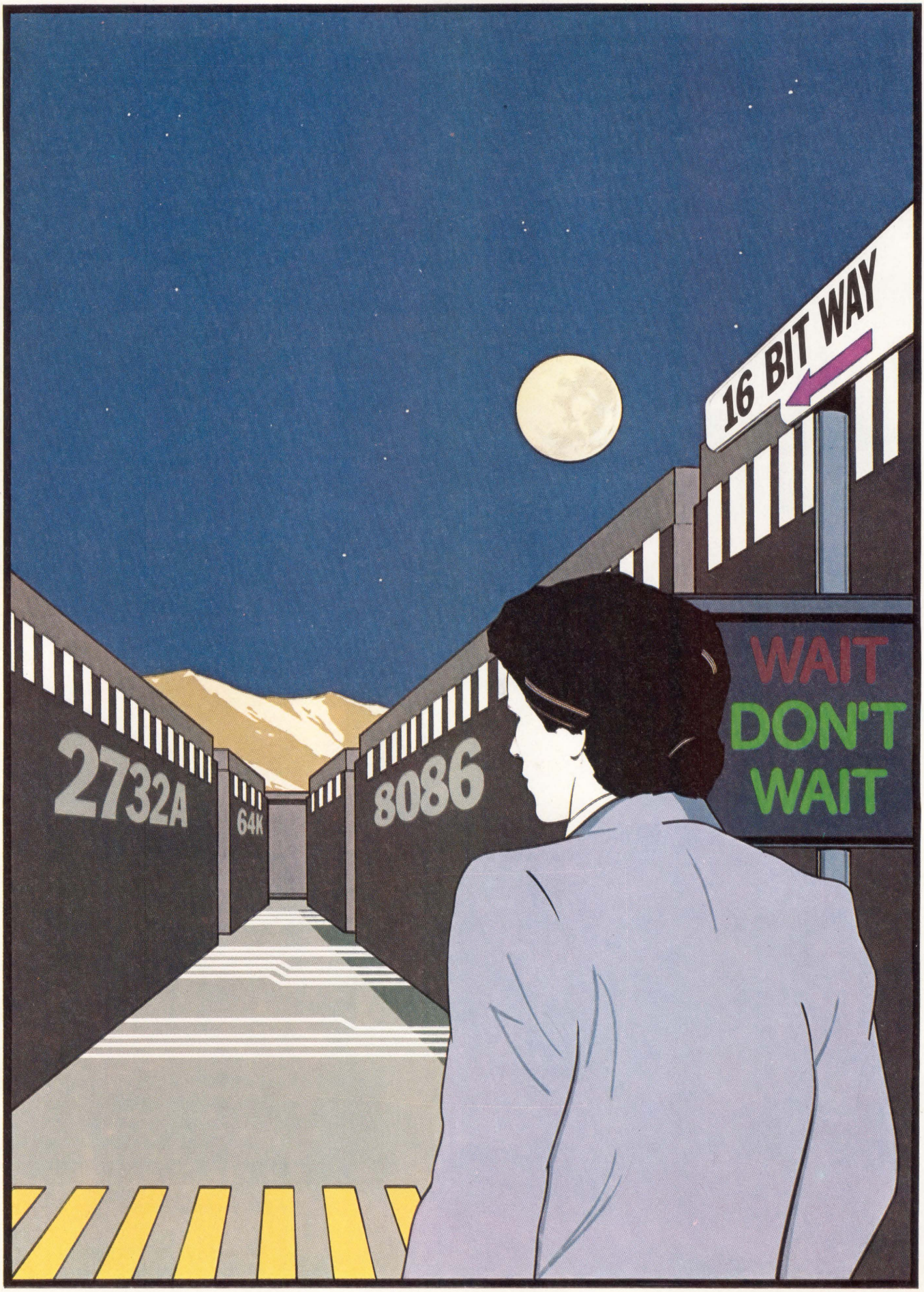
Model DC-946 features:

- modular construction
- 5″ cathode ray tube (12.7 cm)
- solid state
- DC operation—12V dc inputs
- choice of signal inputs:
  TTL (standard)
  Composite video (plug-in module)
- standard 15,750 KHz horizontal scan frequency
- 650 lines resolution

MADE IN ☆☆☆☆☆ AMERICA

CIRCLE 123 ON INQUIRY CARD

**AUDIOTRONICS**
**VIDEO DISPLAY DIVISION**
530 FIFTH AVENUE N.W. NEW BRIGHTON, MN. 55112 · (612) 633-3131


16 BIT WAY
WAIT
DON'T
WAIT
2732A
64K
8086

# No Waiting

## Introducing the Intel® 2732A EPROM. Now you can design 16-bit microcomputer systems without delays.

Now get all the performance you're paying for from your microprocessor designs with Intel's new 2732A EPROM. For 16-bit microprocessor systems, 2732A EPROMs deliver both the high speed (250ns) and high density (32K) solution. No other 32K EPROM on the market comes close.

### No speed limit

Other EPROMs require one, two, even three wait states to work with today's high speed microprocessors. Not Intel's 2732A EPROM. It's fast enough to keep up with any of them.

So now, at last, you can utilize the full potential of your microprocessor. In fact, when you use 2732As, you're designing a system that can run 25% faster.

And with a 32K bit density, you're not losing valuable board space to memory chips.

### The HMOS*-E generation

By designing with the 2732A today, you're actually designing with the standard of tomorrow. The 2732A is a product of Intel's proven, reliable fourth generation EPROM technology, HMOS-E, and the first to come in a family of dense, high speed EPROMs.

HMOS-E technology means that we'll be able to incorporate high performance features, like increased density, into future EPROMs, without affecting their speed or power characteristics. The 2732A is your first step towards a degree of flexibility in memory design never before available.

### JEDEC approved pinout

You can start designing for tomorrow now because the 2732A's pinout conforms to the approved JEDEC committee standard for byte-wide memories from 16K bits to 256K bits. So you can upgrade from a 2732A without changing your design or board layout. And you won't have to sacrifice features like 2-line control—a must in high-speed memories for avoiding bus contention problems.

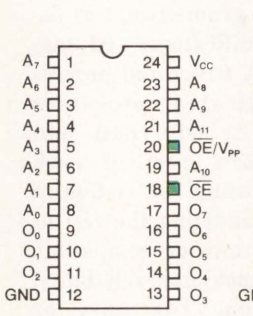
### Proven Intel reliability

Like all our EPROMs, your 2732As are put through rigid quality control tests to insure they'll retain their programs and programmability for years to come.

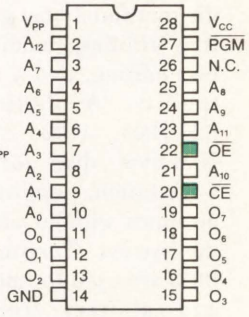
And like all Intel products, the 2732A is backed with our traditional field support and technical documentation. Which means, if needed, you always have a source for technical information and design help to speed development along.

So whether you're designing a system around one of the new 16-bit microprocessors, like our 8086, designing in a high performance 8-bit processor, or upgrading an existing design, *don't wait.* For a cost effective, reliable, and total EPROM solution, with a no-compromise growth path, your best choice is the 2732A.

2732A Pin Configuration




64K Pin Configuration




The 24-pin 2732A pinout conforms to the 28-pin JEDEC committee approved design for byte-wide memories. By using 28-pin sockets, there's no need for delays in upgrading to the 64K, 128K, or 256K EPROMS of the future.

Why add any unnecessary delays? To order now, or for more information—contact your local Intel distributor or sales office. Or, write Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051. Or call (408) 987-8080.

*HMOS is a patented Intel process.

**intel® delivers solutions.**

Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Alliance, Almac/Stroum, Arrow Electronics, Avnet Electronics, Component Specialties, Hamilton/Avnet, Hamilton/Electro Sales, Harvey, Industrial Components, Pioneer, L.A. Varah, Wyle Distribution Group, Zentronics.

## Turnkey System Offers Alternative to Automated Drafting System

Design Graphix is a turnkey interactive computer graphics and design processing alternative to automated drafting systems. Developed by Engineering Systems Consultants, Inc, PO Box 80318, Baton Rouge, LA 70898, the basic system consists of 64k-byte CPU, dual-drive, double-density floppy disc system, 11″ graphics CRT, and 3-dimensional drafting software system.

Operating on any Digital Equipment Corp PDP-11 series computer system under RT-11 or RSX-11M, the graphics system encompasses seven distinct functions; geometrics, text entry, utilities, modifications, editing, text editing, and a structured process facility. A dedicated processor (LSI-11/03, -11/23, or PDP-11/34) and 10M-byte disc form part of each workstation, permitting one station to go down without affecting the rest of the system. Tektronix or compatible CRTs are used for maximum reliability, and plotters from Tektronix or Calcomp can be shared by multiple stations. The unit provides a 4-channel serial line interface and onboard 1200-baud communications modem.

System software supplies a disc management subsystem to handle the disc data base, anticipate read requests and overlap I/O, and maintain directory and unused area table. The intelligent display processor bypasses nondisplayed data, improving display times an average of 10 to 1 over comparable units. Calculator function and full logic programming language are provided by the optional structured programming facility which features high speed and minimum memory requirements. Networked design of the software allows stations to communicate to transfer files to/from the host processor, or with large mainframes on a timesharing basis.

Features of the graphic system allow users to create line work and geometrics; insert text and figures; and rotate, scale, and translate. Multiple layers and pen selects and comprehensive display handling functions are supported, as are database search and geometric construction and local and remote plotting.

Capacity to perform both engineering and design computations is accomplished by design system software. This system accepts existing programs and can communicate with timesharing services. Among the available programs are coordinate geometry, earthwork, slope stability, contour mapping, and network synthesis and analysis. Other programs supply capability to perform project scheduling, resource distribution, population and traffic density and analysis, storm run-off analysis, and flood plain study and analysis. The system is able to make use of all graphics system capabilities.

Circle 430 on Inquiry Card

## Disc Controller Firmware Emulates RK611/RK06 Subsystems

SC01/C and SC11/C disc controllers permit LSI-11 and PDP-11 users to emulate DEC's RK611/RK06 disc subsystems. Intended to support the growing demand for cartridge module drives, the model C from Emulex Corp, 2001 E Deere Ave, Santa Ana, CA 92705 allows the combination of fixed and removable logical units to be selected for maximum capacity.

Controllers duplicate the architectural features of the equivalent DEC subsystem to provide complete transparency with software written for the RK06, including diagnostics and operating system software. Because the controller are implemented through a firmware adaptation of the basic SC01 and SC11 hardware, updates can be effected by simple changing a P/ROM set.

Separate disc drive registers, rotational position sensing, extensive error reporting with 32-bit error detection and 11-bit error burst correction, as well as dual-port drive operations are features of the units. An internal self-test on powerup with LED display of error conditions are provided; the controller can execute a subsystem diagnostic when it is initiated by the operator, with resulting errors displayed on the LEDs.

A 3-sector (1536-byte) disc I/O buffer eliminates data late errors even when operating at low bus priorities. Successive multiple adjacent sector transfers across tracks in the same cylinder are handled without a disc rotation or requiring a sector interlace scheme.

The units provide either 2- or 4-word transfer per bus grant to give adequate data throughput without adding excessive bus latency or locking out interrupt requests from other devices. Transfers consume less than 2.4 μs/pair of words transferred. A programmable bus DMA bandwidth control permits windowing of controller bus transfers to guarantee periodic access for low priority devices.

Circle 431 on Inquiry Card

## Automated PC Board Tester Speeds Production Testing

Model 4400, designed for high speed handling and testing of bare or loaded boards, moves PC boards from the feed conveyor through the test cycle on a rotary indexed multistation table. To meet individual test requirements, Electro-Mechanical Laboratories, Inc, 2 Oakwood Ave, Norwalk, CT 06850 offers a variety of system options and the choice of supplied computrized testing or an interface/adapter to the customer's computer/tester.

Among the design options are facilities to accomplish bare board, stuffed board, continuity, high voltage leakage, functional, and incoming pass/fail testing. Accommodation of board sizes up to 12 x 12″ is standard; other sizes require a special request. Production speeds can range up to 50 boards/min or 24k boards in an 8-h shift, depending on test time and other factors.

Circle 432 on Inquiry Card

*(continued on page 50)*

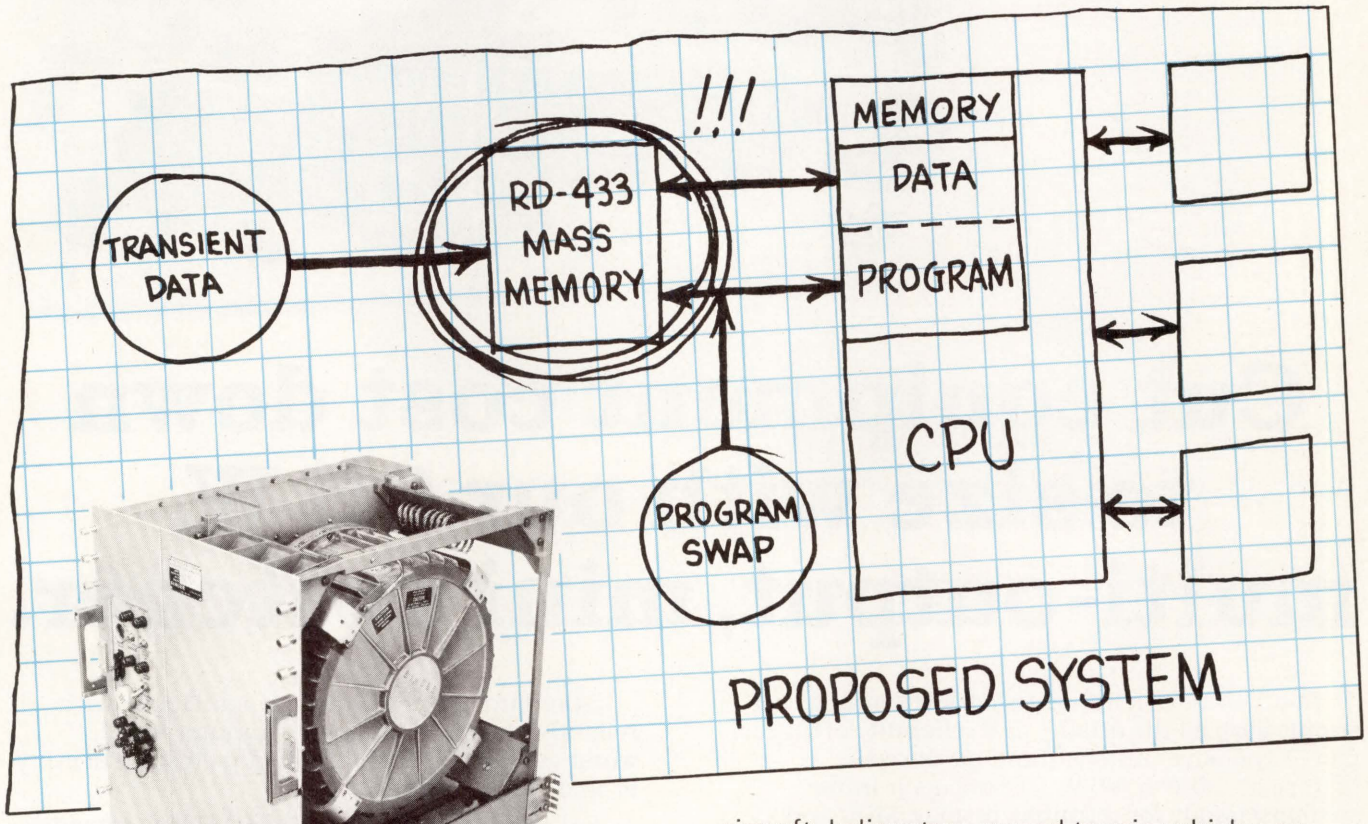
Dear System Manager:

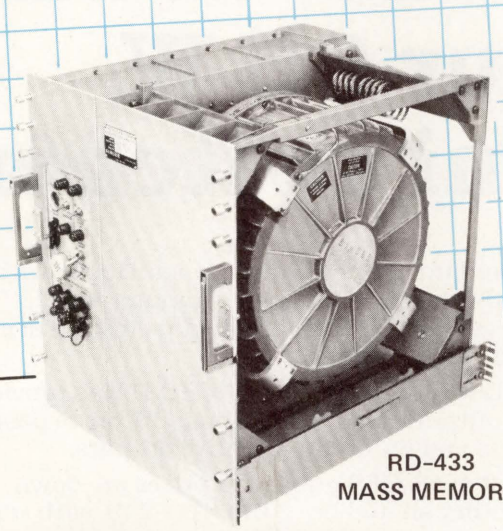
# Is your success just a matter of time?

## (Real Time, That Is)

It is not access time or record transfer time alone that is important. It is the complete read and write cycle time that is essential.

Design your system with Librascope's RD-433 MASS MEMORY like this:



RD-433
MASS MEMORY

The RD-433 is an off-the-shelf, self-contained, high speed head-per-track, fully militarized disc memory subsystem — qualified for the worst of environments, where non-volatility and reliability are paramount. Librascope Mass Memories are:

- ✓ Compatible with computers AN/UYK-7, AN/AYK-14, AN/UYK-15, AN/UYK-19, AN/UYK-20, AN/UYK-27, and Univac 1616.
- ✓ Currently employed in the U.S. Navy's TACINTEL, BQR-24, and TRIDENT IR$^2$ programs — and in the U.S. Coast Guard's new WMEC-270 Cutter Program.

**SO INCLUDE THE RD-433 IN YOUR SYSTEM BRAINSTORMING . . .** whether you are working with surface ships, submarines, fixed-wing aircraft, helicopters, rugged terrain vehicles, or transportable shelters.

The complete read or write cycle time for the RD-433 averages 20 milliseconds. This is twice as fast as the best of moving arm files, fixed head discs, and disc packs. Bubble memories don't even come close to these speeds and may never catch up. The RD-433 and Librascope's other head-per-track militarized Mass Memories are winners wherever high speed is crucial to limited CPU memory capacity.

For more information, write or call:

Librascope Division, The Singer Company
Department AA, 833 Sonora Ave.
Glendale, California 91201
Telephone: (213) 244-6541, X1891

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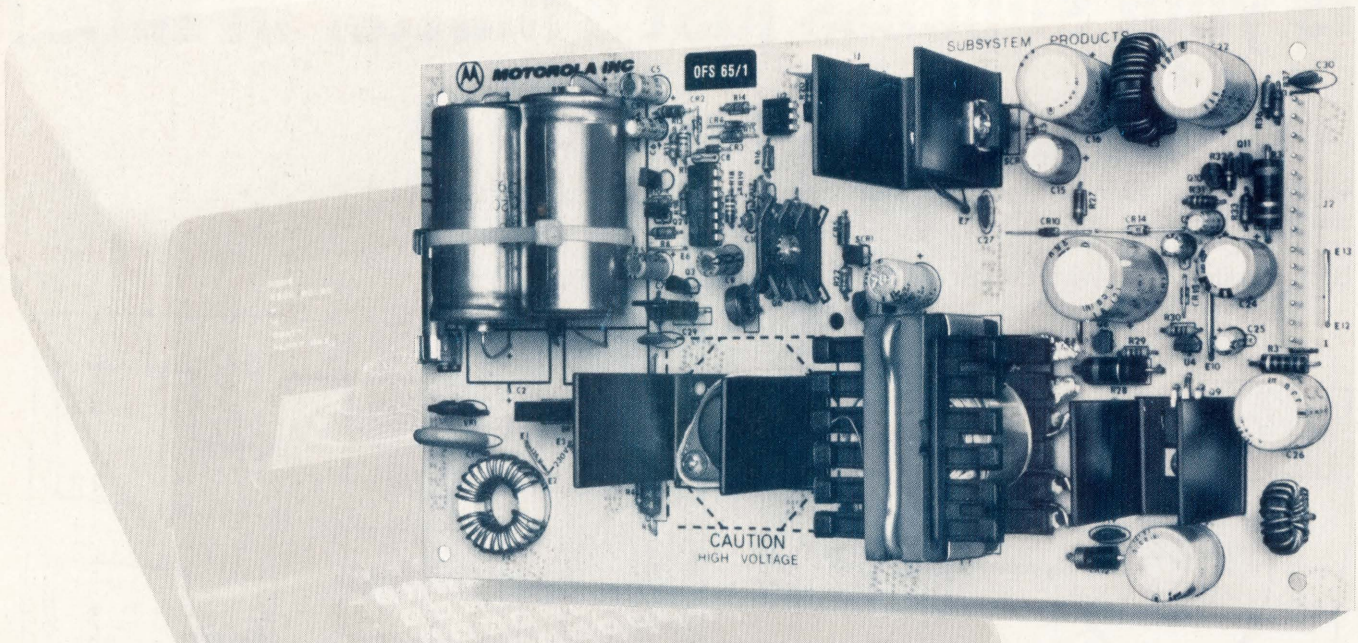
Technological leadership.




# Cut equipment cost down to size with our 65 W, multi-output, mini switcher.

Now you have a full-featured, switching power supply with all the quality and reliability of bigger, more expensive units without all the cost . . . Motorola's 50 W to 65 W, OFS65, open-frame switcher family for terminal, display, MPU and other low-power system applications.

## Less parts, more MTBF.

Cooler and more efficient than equivalent linears, parts count is about 20% less than similar switcher types—also a key cost-reducing element. No fans are required for cooling the design which boasts about 2 W output per cubic inch. Efficiency for the triple-output unit is approximately 65%.

## Full protection for self and system.

Small and lightweight (about 20 oz.), the OFS series is fully self-protected from abuse at output terminals. Shorts and opens can't damage it with high, low or in-between input voltages. Overload simply causes periodic recycling with normalcy restored when overload is gone.

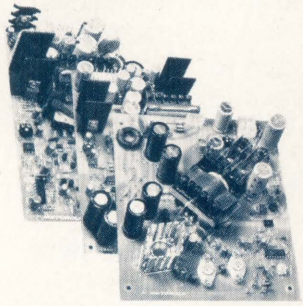
And if your system's going to crash due to power line failure, it sends a warning signal to the MPU to unload volatile memory with output voltage remaining within regulation for 32 ms after loss of nominal line voltage. That's about twice as long a spec as some others offer.

Of course, it provides EMI filter on input, soft start and reverse polarity protection.

Standard, 24-hour burn-in is included with reliability ensured through computer-aided, worst-case analysis and individual testing of every IC and discrete device.

Excellent line regulation of ±0.15% is provided on all outputs; load regulation is 1% on all positive outputs and 6% on the negative outputs.

Best of all, OFS published prices are down where they should be: $130, 100–249, with very competitive quantity pricing.



## Customs, too.

Other sizes and performance ratings are available for individual needs.

And you have Motorola's reputation for quality, integrity and conservative design in every one of these new

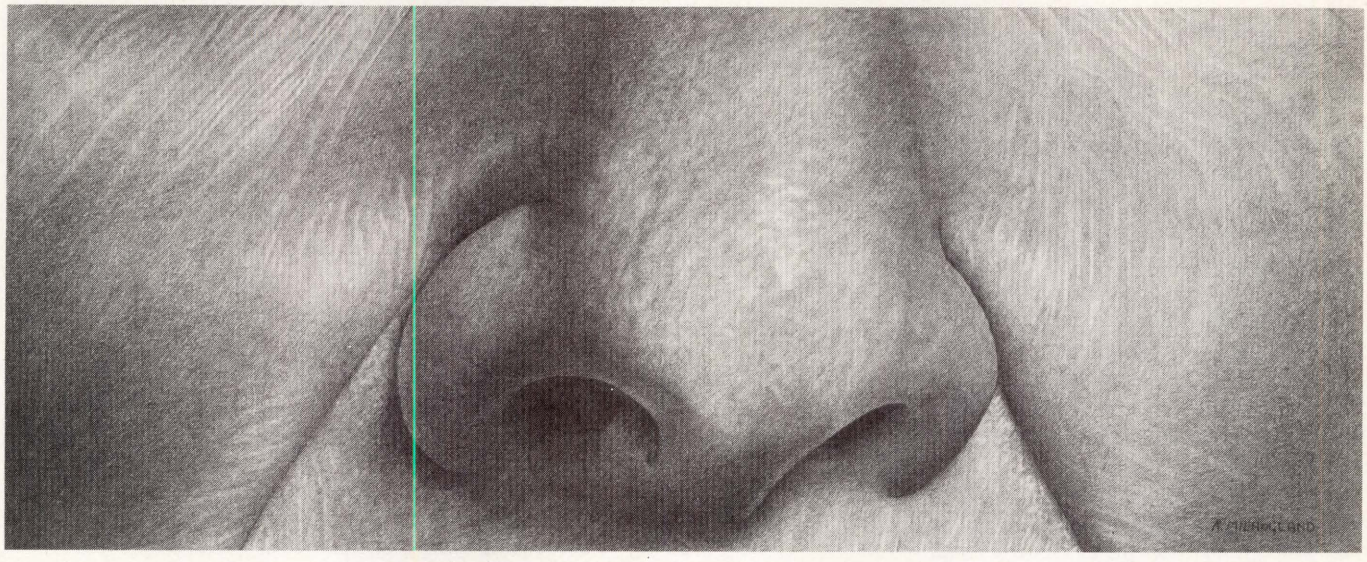
Innovative systems through silicon.

MOTOROLA INC.



CIRCLE 127 ON INQUIRY CARD

# Nosey, nosey, nosey.



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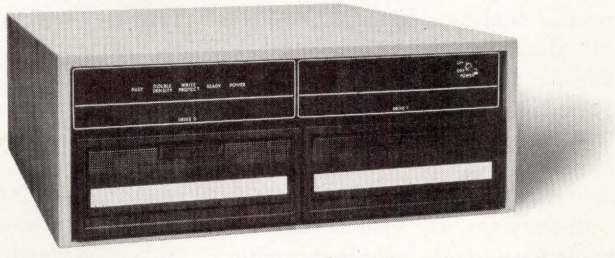

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## Multipurpose Computer System Designed For Versatility

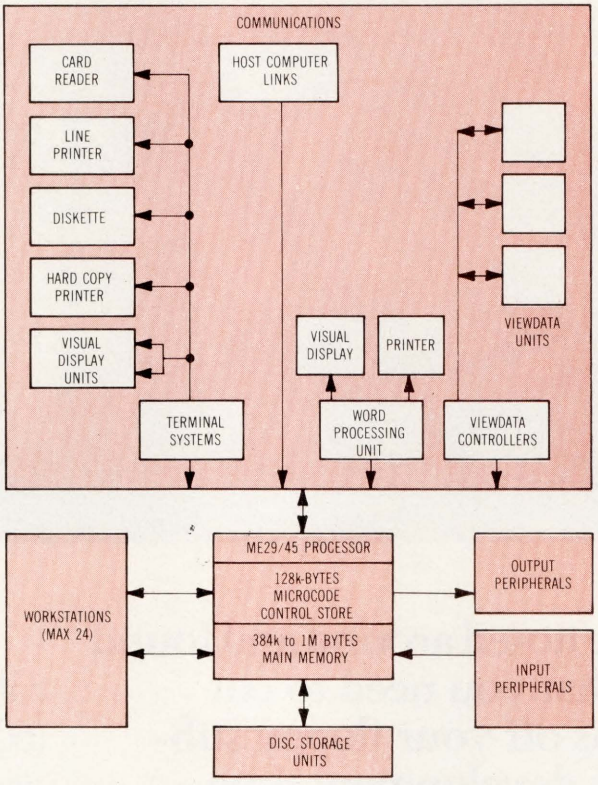
ME29 high performance, multipurpose medium powered computer systems use a microprogrammed processor operating at speeds greater than 3M instructions/s. Data throughput of the machine is claimed to be five times greater than that of its predecessor, the 2904/50. ICL Computers Canada Ltd, 1 Trippett Rd, Downsview, Toronto, Ontario M3H 2V1, Canada, states that the machine competes with IBM Systems/34, /38, and 4331 with prices 10 to 15% lower.

Heart of the system is a microprogrammed processor that operates at speeds above 3M instructions/s. The machines offer main memory capacities of 256k to 1M bytes. Disc storage builds from 35M bytes to a total of 16G bytes. Multipurpose workstations in the system serve as transaction processing terminal, interactive terminal, operator console, or direct data entry terminals.

Central processor in the ME29 has two separate memories—the main memory and a high performance microcoded control memory. Main memory uses 16k-bit chips to form 128k-byte modules having an access time of 4 bytes/750 ns. The model 35 permits main memory to expand from 256k to 1M bytes; the model 45 expands from 384k to 1M bytes.

Either 64k or 128k bytes of control store are available for system microcode. This store cycles at 155-ns nominal with a prefetch mechanism enabling most operations to occur in 93 ns. Additional hardware in the model 45 yields almost double the processing power of the model 35.

Five disc storage modules are available to meet storage requirements from 35M to 16G bytes. Modules include 35M-byte fixed disc drives, removable 60M-byte drives, 120M-byte fixed disc drives, combination 120M-byte fixed/60M-byte removable disc systems, and 500M-byte fixed disc system. One or two flexible disc drives within the CPU cabinet provide for convenient data and software input. Each has capacity for 1M bytes. Other attachable peripherals include magnetic tape transports, line printers, matrix printers, and paper tape and card equipment. Workstations comprise a 2000-char screen with comprehensive keyboard. Up to 24 workstations connect locally to the computer; up to 12 of these may be used for direct data entry. Any of the 24 may be used for transaction processing, operator console, program development work, or use of HELP or DIALOG systems.




ME29 model 45 from ICL Computers Canada offers versatile communications facilities through simple user interface. Processor instructions are implemented via microprogram residing in control store. Separate from main memory, this store operates at 155 ns nominal; main memory cycle time is 750 ns

Asynchronous and synchronous multiple line communications couplers (AMLCC and SMLCC) may coexist on the system. Each AMLCC provides connection for eight local devices which can be workstations or matrix printers. SMLCCs provide connectivity for up to eight local or remote communications lines.

More than 200 visual display units, hardcopy printers, and floppy discs linked to model 7500 terminal processors can be controlled by one computer. Connection between terminal processor and host is by telephone lines and SMLCC.

TME (Transaction Machine Environment) operating system for use on the system adds a leaf addressing mode to the executive and object modes of the EXEC 3S system used on 2903/4 and DME/2 systems. This mode incorporates many virtual memory functions by writing system program activities on a number of leaves and bringing the appropriate one into main memory when needed. Using this mode new system functions may be introduced without disturbing the operating system base.

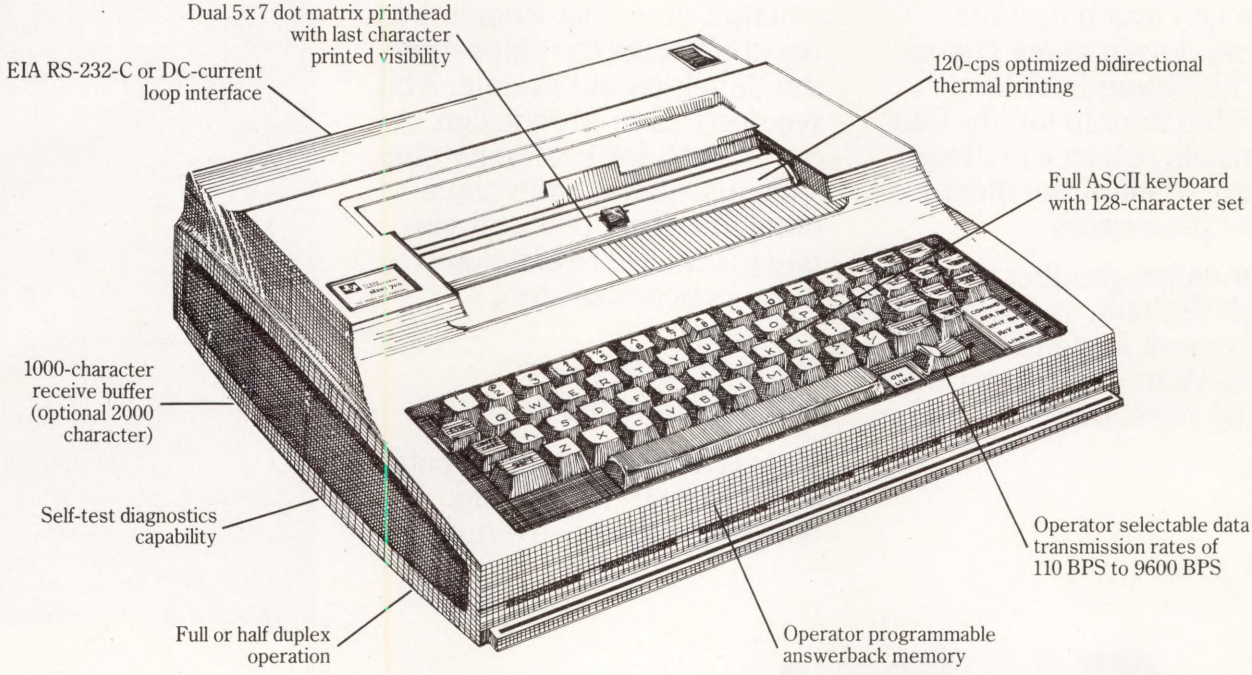
Both Data Management System and Data Dictionary Systems are implemented to administer data bases. Languages include COBOL, FORTRAN, RPG II, BASIC, and ALGOL.

Circle 429 on Inquiry Card

# The Task Master.

## 783 KSR

### Keyboard Send-Receive Data Terminal




Ideal for commercial applications, TI's *Silent 700** Model 783 KSR Data Terminal can master your workload with high-quality, efficient thermal printing. Offering a variety of user-oriented standard features and options, the virtually silent 783 KSR takes less work space while it maximizes printing throughput. That's why the versatile 783 KSR was designed to handle your most demanding printing tasks.

TI is dedicated to producing quality, innovative products like the 783 KSR Data Terminal. TI's hundreds of thousands of data terminals shipped worldwide are backed by the technology and reliability that come from 50 years of experience, and are supported by our worldwide organization of factory-trained sales and service representatives.

For more information on the 783 KSR, contact the TI sales office nearest you or write Texas Instruments Incorporated, P.O. Box 1444, M/S 7784, Houston, Texas 77001, or phone (713) 937-2016. In Europe, write Texas Instruments Incorporated, M/S 74, B.P. 5, Villeneuve-Loubet, 06270, France.

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When it comes to developing development systems that support more microprocessors, no one can touch us. Our universal development system doesn't box you in with a single chip or chip family. Our system sets you free to design with any or all of the most popular processors.

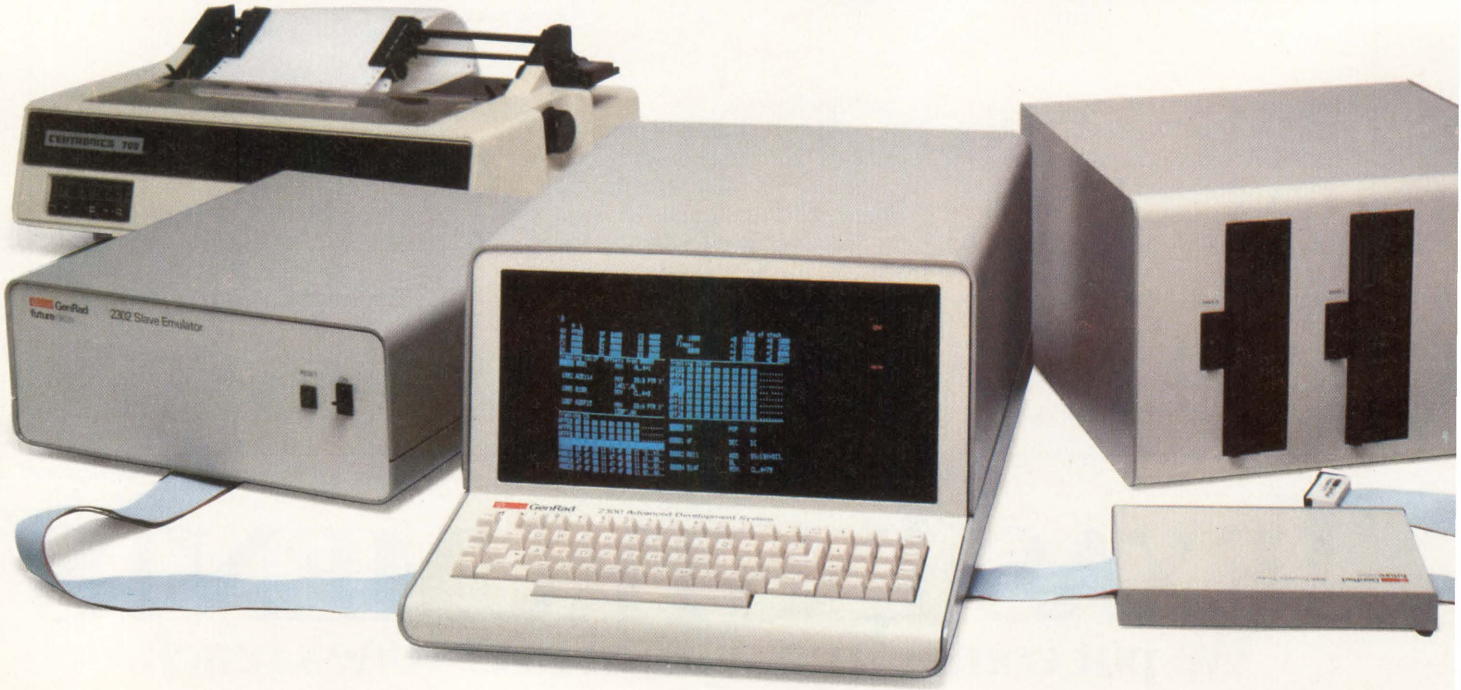
In your smart-product race through the '80's, switching development systems will be the pits. With our system that won't be necessary.

## WE ADD NEW CHIP SUPPORT FASTER

Thanks to our unique slave emulation system we can add new chips to your system in a matter of weeks. Remember, we don't make the chips – just the development system. And we don't have to redesign our system for each new chip – we just add another slave emulator. And, that's all you pay for. So, we're faster and more economical, too.

## WE SET THE PACE FOR EMULATION

Ours is the only system capable of delivering transparent, non-stop, full-speed emulation



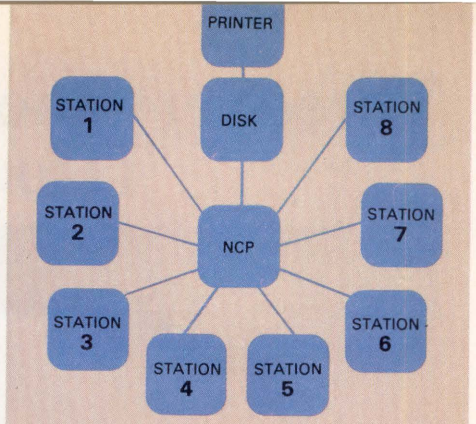
# 2300 series

advanced development systems

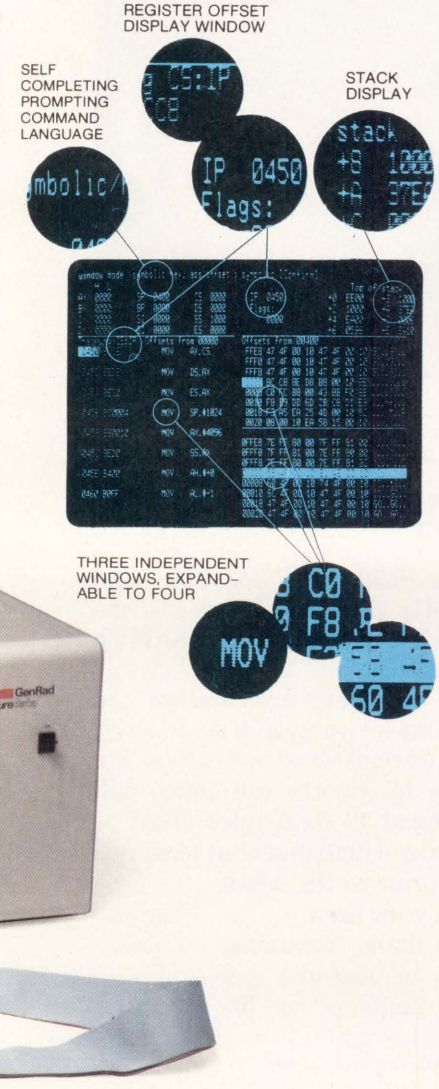
to 10 MHz. And it's the only system capable of emulating many different processors simultaneously.

Transparent, non-stop, full-speed emulation takes all the guesswork out of choosing the right microprocessor for your application. It allows you to evaluate each chip thoroughly, accurately and objectively.

The ability to emulate several different chips simultaneously paves the way to development of smart products using more than one processor.




2300 Series multi-station networks share disk and printer with up to eight stations. Each station is universal and may be ordered with the software and/or hardware capabilities required.




TYPICAL 8086 SNAPSHOT

The 2302 Slave Emulator allows you to view your program in single-step, snapshot or logic analyzer modes. This view can be formatted to match your requirements even for the most complex memory segmentation, interrupt-driven or multi-processor environments.

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Our system has been designed to make hardware and software development fast, efficient and productive. With our high-speed CRT, high-level language programming and powerful software, things happen fast – sometimes instantaneously. Now available with highly block structured PASCAL compilers, our system can cut your programming time by 50% or more.

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There is no finish in the smart-product race. To stay ahead you're going to need flexible, productive, expandable development systems and a supplier with staying power capable of giving you in-depth, after-sale service and support. Ask for a demonstration of the 2300 Series Advanced Development System. Sales and service offices in major cities.

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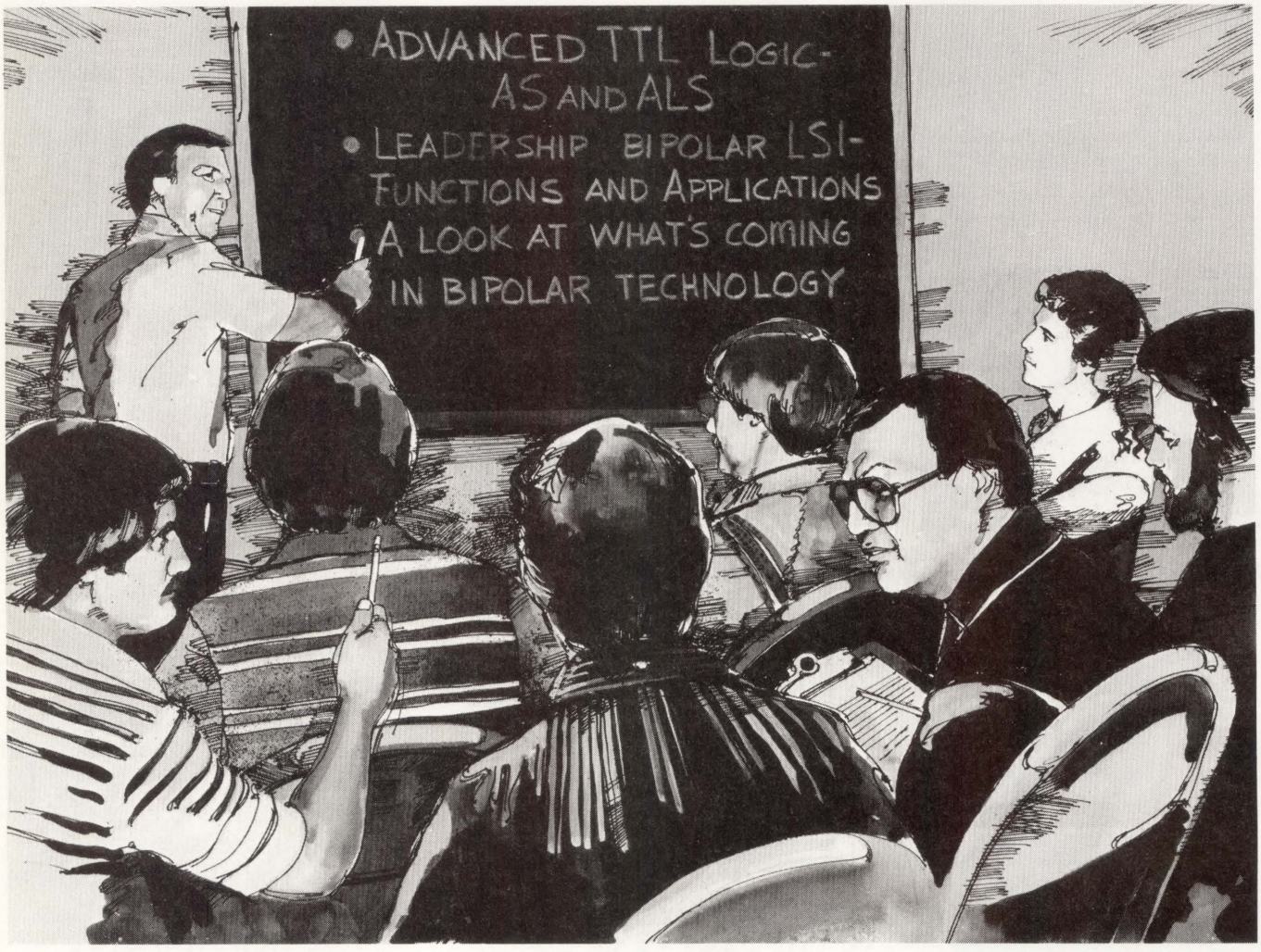
CIRCLE 27 ON INQUIRY CARD

# Three very good reasons why you should give TI four hours of your time.




## TI's new Advanced Bipolar Logic seminars start Monday, August 11.

On Monday, August 11, TI is kicking off a new series of seminars that will examine the role of bipolar logic design. A series of seminars that will provide an in-depth look at performance, power and reliability improvements with AS/ALS — for better systems solutions.

It's a different kind of seminar. Learning-intensive. For system designers who need to know what the future holds for Advanced Schottky, Advanced Low-Power Schottky and Low-Power Schottky.

The agenda will fill you in on the specific topics to be discussed, and we'll focus on information you can use right away. (Along with samples, data sheets and handouts that you can take away.)

Information that could give you the competitive edge today for leading state-of-the-art products tomorrow.

We know you'll be anxious to get started applying what you learn. But stay for lunch. It's free. And besides, that's when we'll be giving away a TI 59 — an extraordinary card programmable calculator with plug-in Solid State Software* and magnetic card storage — it's the pride of every engineering professional.

**For complete information** and to guarantee yourself a seat (sorry, only preregistered attendees are eligible to win the calculator) **call your local TI field sales office or authorized distributor at least one week prior to the seminar in your area.**

The dates, locations, names of contacts and phone numbers are listed on the right.

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84618

# Agenda

- TI's Schottky Families for the '80s . . . characteristics, applications and compatibility:
  - Low-Power Schottky
  - High-performance Schottky
  - Second Generation Families:
    - Advanced Schottky
    - Advanced Low-Power Schottky
- New product previews
- Quality/reliability improvements
- High-density packaging innovations:
  - Chip carrier packages
  - New 24-pin DIPs

# Dates, Locations, Contacts

| Date | Location | Contact | Phone |
|---|---|---|---|
| August 11 | Boston (Waltham) | Jack Edick | (617) 890-7400 |
| August 13 | New York (Melville) | Chuck Messmer | (516) 454-6616 |
| August 15 | New Jersey (Clark) | Terry Manton | (201) 574-9800 |
| August 18 | Philadelphia (Ft. Washington) | Ken O'Connor | (215) 643-6450 |
| August 20 | Washington (Arlington, VA) | Jim Myers | (703) 553-2200 |
| August 22 | Florida (Ft. Lauderdale) | Hank Keuhler | (305) 973-8502 |
| August 25 | Minneapolis (Edina) | Roger Scott | (612) 830-1600 |
| August 27 | Chicago (Arlington Heights) | Dave Nesbitt | (312) 640-3000 |
| August 29 | Dallas | Jim Roundtree | (214) 995-6531 |
| Sept. 8 | Denver | Ken Mudge | (303) 695-2800 |
| Sept. 10 | Seattle (Bellevue) | Dave Burkhart | (206) 881-3080 |
| Sept. 12 | San Francisco (Sunnyvale) | Tom Addie | (408) 732-1840 |
| Sept. 15 | Phoenix | Bill Tanner | (602) 249-1313 |
| Sept. 16 | Los Angeles (El Segundo) | Jim Davi | (213) 973-2571 |
| Sept. 17 | Orange County (Costa Mesa) | Joe Favela | (714) 540-7311 |
| Sept. 19 | San Diego | John Lucas | (714) 278-9600 |

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## Desktop Computer System Displays Graphics In 4913 Colors

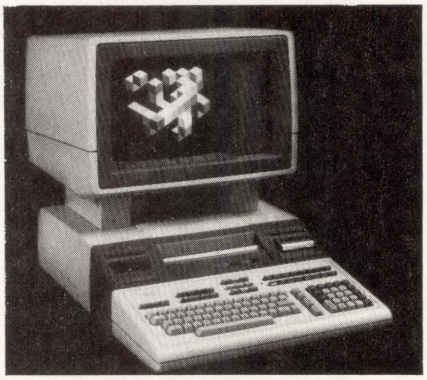
Integrating graphics computation and color display in a desktop unit, HP series 9800 system 45C offers the power to solve complicated computational, design, and data acquisition and control problems. Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, has packed built-in color graphics CRT display, light pen, operating system, read/write memory, enhanced BASIC language, keyboard, mass storage system, and thermal line printer in an interactive unit that is easy to use, and can handle problems that range from Fast Fourier Transforms to multiple linear regressions and project management.

Graphics computation power of the system stems from the combination of graphics language, high performance processor, and large user memory. Since the operating system as well as standard display, graphics, and control functions are contained in 152k bytes of ROM, 187k bytes of RAM are available to user programs and data. Memory expands up to 449k bytes.

The system provides 70 graphics statements which relieve the user of many programming tasks such as generation of geometric figures. Geometric figures such as circles, rectangles, regular polygons, and objects represented in matrices are drawn on the CRT through simple commands. An additional file parameter quickly adds color fill to any drawn figure.

System CRT uses a shadow mask tube incorporating a screen covered with triads of dots with red, green, and blue emissions. Each phosphor type is activated by an electron beam from a corresponding electron gun. A metal shadow mask guides beams so that, for example, only beams from the green gun hit green phosphors. This provides the eight basic colors. The remainder of the 4913 displayable colors are produced using a technique called dithering. In this process the 560 x 455 graphics raster CRT is divided into 4 x 4 arrays each containing 16 pixels (picture elements) which can be turned on or off. The various combinations of pixels being turned on or off in three different memory planes produces color shades on the CRT.

A built-in system ROM provides the programming tools necessary for powerful color graphics processing. The CRT offers high quality resolution, crisp color, and high speed vector writing. A light pen provides a fast easy way to pick, move, and construct objects directly on the screen. The pen permits selection of a single pixel; a second order, predictive algorithm located in firmware moves the cursor in the direction and speed of light pen motion.



Capable of displaying 4913 colors, Hewlett-Packard's System 45C constitutes a complete workstation. CRT display, light pen, operating system, read/write memory, BASIC language, mass storage system, and line printer integrated into unit furnish capability for solving complex graphics computational problems and displaying 3-dimensional representations of solutions

When hardcopy of the display is needed, a command input through the keyboard results in transfer of the image to the built-in thermal printer. This printer outputs at 480 lines/min, duplicating color images in shades of gray. Tape drives built into the mainframe provide storage for 217k bytes of data or programs.

In a standard configuration, the computer system includes color CRT and color graphics firmware, interactive light pen, 187k bytes of user read/write memory, two 217k-byte cartridge tape drives, and internal 80-col, 480-line/min thermal printer. The system uses enhanced BASIC language; an optional assembly language programming ROM is available for special control, I/O, and speed enhancement. An entry level configuration providing 56k bytes RAM and one tape drive is priced at $31,500. The standard system sells for $39,500.

Circle 422 on Inquiry Card

## Multipurpose Computer Provides Realtime Time-Critical Capabilities

The Cyber 170 model 740 computer, a multipurpose system from Control Data Corp, Box O, Minneapolis, MN 55440, provides realtime/time-critical network, scientific, commercial, and data management capabilities. The system is field upgradable to a Model 750 or 760. It is compatible with software and peripherals used with previous systems.

The CPU of the 740 consists of nine arithmetic functional units, each specialized for particular instruction types (Boolean, shift, normalize, integer add, floating add, multiply, divide, population count, and increment), which increases efficiency as compared to a unified CPU. The CPU uses subnanosecond ECL ICs for high reliability, compact physical packaging, and low power requirements. An address instruction stack provides fast retrieval of previously executed instructions. Computation can be floating or fixed point, single-, or double-precision.

Central memory of the system is built with 4k static MOS chips that provide 400-ns memory access time. Memory size ranges from 1.31M to 2.62M characters. Central memory is organized into eight logically independent, phased bands of 60-bit words that permit data to be either ten 6-bit characters or a floating point number with 48-bit coefficient and an 11-bit exponent. The phasing places successive addresses in different banks, permitting operation at much higher rates than the basic cycle time. Max data transfer rate is 10 char/50 ns.

The system can be configured to include one or two peripheral processor

# POWER-ONE
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Below are just a few popular examples of the over 90 "off the shelf" models now available from stock.

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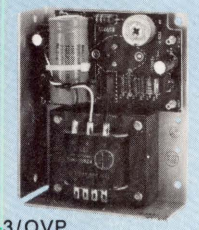
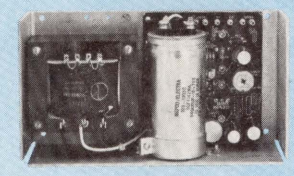
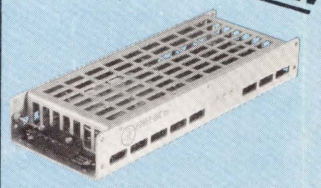
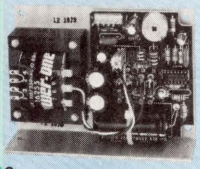
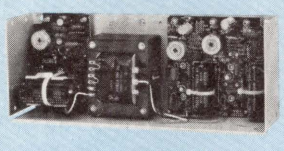
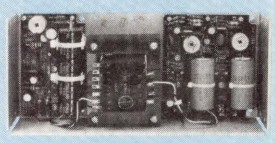
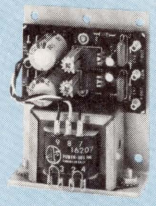
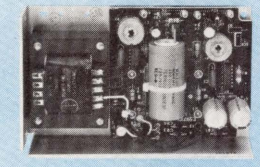
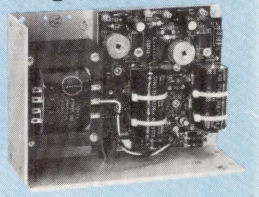
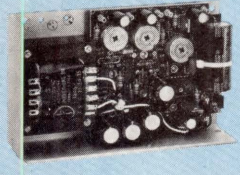
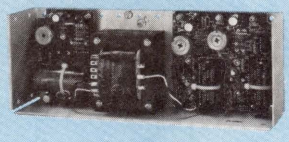
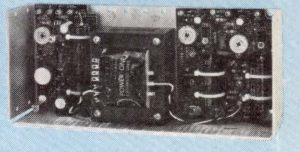
| **SINGLE OUTPUT & LOGIC POWER SUPPLIES**<br>• 56 "off the shelf" models<br>• 2V to 250V, 0.1A to 40A<br>• ± .05% regulation<br>• 115/230 VAC input | **5V @ 3A, w/OVP**<br>  <br>HB5-3/OVP<br>$24.95 single qty. | **5V @ 12A, w/OVP**<br>  <br>HD5-12/OVP<br>$79.95 single qty. | **5V @ 40A, w/OVP** NEW<br>  <br>SK5-40/OVP<br>Switching Model<br>$250.00 single qty. |
| **FLOPPY-DISK SERIES**<br>• 8 "off the shelf" models<br>• Powers most popular drives<br>• Single/dual drive applications<br>• 2-year warranty | **5V @ 0.7A, w/OVP**<br>**12V @ 1.1A/1.7A PK** NEW<br>  <br>CP340<br>For one 5.25" Media Drive<br>$44.95 single qty. | **5V @ 1A, w/OVP**<br>**−5V @ 0.5A, w/OVP**<br>**24V @ 1.5A/1.7A PK**<br>  <br>CP205<br>For one 8.0" Media Drive<br>$69.95 single qty. | **5V @ 2.5A, w/OVP**<br>**−5V @ 0.5A, w/OVP**<br>**24V @ 3A/3.4A PK**<br>  <br>CP206<br>For two 8.0" Media Drives<br>$91.95 single qty. |
| **DUAL OUTPUT MODELS**<br>• 15 "off the shelf" models<br>• ±5V to ±24V, 0.25A to 6A<br>• I.C. regulated<br>• Full rated to +50°C | **12V/15V @ 0.25A** NEW<br>  <br>HAD12-.25/HAD15-.25<br>$32.95 single qty. | **5V @ 2A, w/OVP**<br>**9 − 15V @ 0.5A**<br>  <br>HAA512<br>$44.95 single qty. | **±12V @ 1.7A or**<br>**±15V @ 1.5A**<br>  <br>HBB15-1.5<br>$49.95 single qty. |
| **TRIPLE OUTPUT MODELS**<br>• 10 "off the shelf" models<br>• 5V plus ± 9V to ± 15V outputs<br>• Models from 16W to 150W<br>• Industry standard size | **5V @ 2A, w/OVP**<br>**± 9V to ± 15V @ 0.4A**<br>  <br>HTAA-16W<br>$49.95 single qty. | **5V @ 3A, w/OVP**<br>**±12V @ 1A or**<br>**±15V @ 0.8A**<br>  <br>HBAA-40W<br>$69.95 single qty. | **5V @ 6A, w/OVP**<br>**±12V @ 1.7A or**<br>**±15V @ 1.5A**<br>  <br>HCBB-75W<br>$91.95 single qty. |

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CIRCLE 29 ON INQUIRY CARD

subsystems. The basic subsystem consists of 10 peripheral processors and 12 data channels. The optional second subsystem can be selected to expand to 14, 17, or 20 processors with an additional 12 data channels. Each peripheral processor is a functionally independent computer comprised of 8k 6-bit char of MOS memory and an arithmetic section that supports a full repertoire of arithmetic and I/O instructions.

The system is supported by NOS (network operating system), a multimode operating system. Languages include COMPASS assembler language, FORTRAN, COBOL, ALGOL, APL, SORT/MERGE, BASIC, GPSS, SIMSCRIPT, and APT.

The 170 is available for customer benchmarking. Prices range from $1,492,500 for 1.31M-char main memory, 10 peripheral processing units, and 12 I/O channels to $1,836,210 for 2.62M-char main memory, 20 peripheral processors, and 24 I/O channels.

Circle 423 on Inquiry Card

## CAD System Raises Design and Drafting Productivity

The Sigmagraphics II™ computer assisted design (CAD) system from Sigma Design West, Ltd, 13693 E Iliff Ave, Aurora, CO 80014, should raise design and drafting productivity by at least 200%. The drafting system is built around a Z80-A microprocessor with 176k-byte RAM. The basic system also includes 716k-byte minidiskette storage, a 36 x 48″ (91 x 122-cm) digitizing tablet with 4-button cursor, a graphic CRT, a 36″ (91-cm) drum plotter with 3 ink or ballpoint pens, and a 6-lines x 40-char plasma display for showing prompts, error messages, and other alphanumeric data.

SIGMAC is the operator command language. Its question and answer format guides users by requesting needed information, processing input, and clearly displaying progress every step along the way. The language contains all standard graphics functions plus calculator functions, provisions for user interaction, looping, and decision making capabilities.

With this drafting system, all plans can be computerized, common functions stored, and plans printed with increased speed and accuracy. Input is from a keyboard, from crosshairs on a CRT screen, or from the cursor on the digitizing table. Any combination of layers can be superimposed during design or output. The system can display and plot 3-dimensional output from 2-dimensional input.

Circle 424 on Inquiry Card

## 32-Bit Word Minicomputer Executes Multitasks Simultaneously

Designed for realtime, scientific, multitasking applications, the Systems 32/7780 can execute multitasks simultaneously, yet is totally transparent to the user. In a multitasking environment, the 32-bit word processor from Systems Engineering Laboratories, Inc, 6901 W Sunrise Blvd, Ft Lauderdale, FL 33313, can provide up to 80% more performance than the 32/77.

The minicomputer is available in one packaged and three nuclei configurations. The basic nucleus configuration includes the central processing unit (CPU), internal processing unit (IUP), 1M bytes of memory, and realtime option module. The second nucleus configuration adds two high speed floating point units, one each for the CPU and IPU. The third nucleus configuration also provides two scientific accelerators, one each for the CPU and IPU.

The packaged system is based on the third and largest nucleus. It includes a disc processor with 80M-byte disc, tape processor with 45 in (114 cm)/s, 1600/6250-bit/in (630/2460/cm) tape drive, teleprinter, line printer, card reader controller, CRT terminal, and MPX operating system. All components are packaged in two cabinets.

All configurations are available with either 1M or 2M bytes of memory. Prices range from $84,000 for the basic nucleus to $145,000 for the packaged system with 2M bytes of memory.

Circle 425 on Inquiry Card

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## Two Processors Fill Cost/Performance Gaps in Family

Completing the cost/performance range of the CLASSIC family, Models 7820 and 7840 are low and mid-range systems that use the MAX IV operating system. Introduced by Modular Computer Systems, Inc, 1650 W McNab Rd, Fort Lauderdale, FL 33310, the 7820 is suitable for standalone or satellite use in data acquisition and control or monitoring applications; the 7840 meets needs of realtime measurement and control, communication, and information processing applications.

Model 7820 includes 128k bytes of error correcting MOS memory; an upgraded version, the 7821 has capacity for 256k bytes. Both consist of 4-slot card file housing a single CPU/I/O processor module and the single-board 2-way interleaved MOS memory circuit card. Remaining slots within the file permit customizing or expansion of the basic system.

A context register file containing 16 general purpose register banks, each with 15 registers, enables context switching among several tasks without having to save and restore register content. This feature, in combination with four address mapping files, expanded instruction set, direct memory processing I/O channels, and fast interrupt response, reduces system overhead to a minimum.

A mid-range processor, with 256k bytes of programmable error correcting MOS memory, the 7840 is designed for realtime environments. Architecture of the unit processes formats that range from 1 to 64 bits in length.

An I/O connector panel used for peripheral interface accommodates remote file interface and extends the local I/O bus. The programmer's maintenance panel allows users to enter and display memory locations, and general or internal CPU registers. It can also be used to initiate console interrupts, master clear, file, run/halt, as well as additional maintenance functions.

The system uses the compatible MODCOMP II, MODCOMP IV, and CLASSIC instruction set, and can be used with

*(continued on page 62)*


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CIRCLE 31 ON INQUIRY CARD

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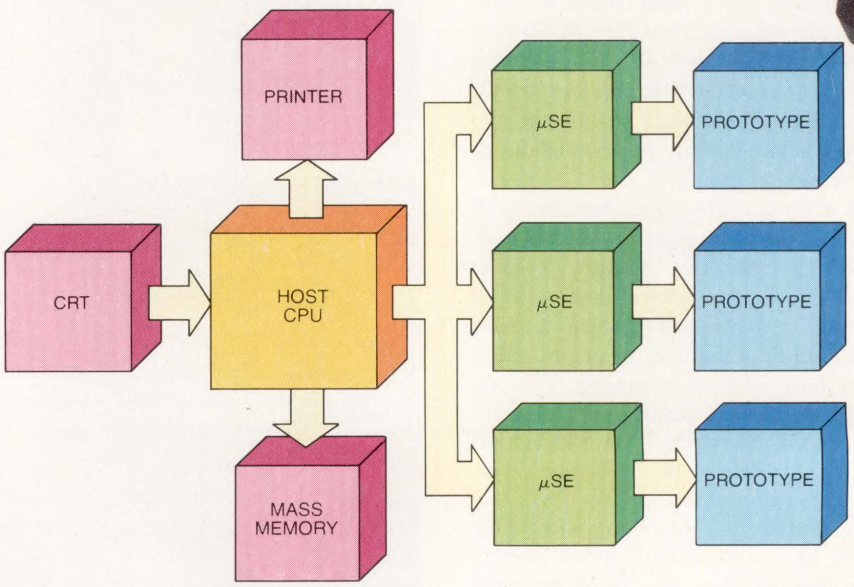
## What's Distributed ICE?

Distributed ICE solves some common microsystem design problems. It provides multi-user capabilities so that in-circuit emulation can be performed concurrently by a number of users while your development system is being used for software development. And it permits emulation of multiple microprocessors. With Distributed ICE, Millennium μSEs can turn your PDP-11, Nova or other minicomputer, or dedicated Intel, Motorola or Zilog software development system into a multi-user development network. Your engineers and development system become more productive.




## Here's how you do it.

You develop applications programs on your host system using cross-assemblers (which we also supply) and then download them into the μSE using standard hex over an RS232C serial link at rates up to 9600 baud. Our μSE becomes an intelligent terminal providing the distributed in-circuit emulation you need for rapid, efficient hardware/software integration. There is virtually no limit to the number of engineers one development system can support, because each low-cost μSE uses the host computer (or development system) only for downloading.

And you'll find that hardware/software integration of micro system designs is faster using our function-oriented keyboard with simple commands such as MEMORY, RUN/DISPLAY, PROM/MEM, I/O, BREAK, REGISTER, RUN and STEP to make complex jobs easier. (Time saved translates directly into dollars saved. That's our bottomline orientation at work.)

## Real-time trace: fast, accurate debugging.

Today's micros are fast, and you need an in-circuit emulator that

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meets the challenge. The μSE lets you do accurate debugging because you do it in real time. No artificial wait states. Emulates at the highest clock rates specified by the micro supplier. True real-time emulation.

Advanced emulation control tools are part of the package. You have dual breakpoints and dual triggers, both using 35-bit comparators. And the μSE's real-time trace records 128 cycles 35 bits wide for faster debugging. A wide range of trace qualifiers, pass counts and delay counts expands your debugging capabilities.

## In tune with today's realities.

We want to help you save money **and** get increased capability. By using our μSE's for Distributed ICE, you not only extend the capability and usefulness of your present development system or minicomputer, you will also be able to get your new design out the door ahead of the competition. And in budget. The μSE costs only $5000*, and emulation modules start at $1375.

## We help design and test micro systems, too. Economically.

Our MicroSystem Designer (μSD) is a low-cost (under $2000) desk-top design and evaluation tool that's helpful in breadboarding, debugging and training. Supports many of the important 8- and 16-bit micros.

And our MicroSystem Analyzer (μSA) is the first test system at any price (our price is only $5350) to combine in-circuit emulation, signature analysis and time-domain analysis in a single, portable package. We'll be glad to supply complete data on either system. Or both. Just ask.

## And that's the bottom line.

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To get yourself started on the right development track, call or write Millennium Systems today and ask about the μSE. Besides telling you all about Distributed ICE, we'll include—FREE—a reprint of Millennium's "Designer's Guide to Testing and Troubleshooting μP-based Products". Our address: 19050 Pruneridge Ave., Cupertino, CA 95014. Telephone: (408) 996-9109.

# We're Millennium

The bottom line in micro support

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*All prices quoted are single-unit, U.S. prices only.

Circle 32 for Literature
Circle 130 for Demonstration

MAX II, III, and IV realtime multiprogramming operating systems and MAXNET extensions for distributed network applications. Special hardware instructions are oriented toward fast FORTRAN execution for users writing realtime tasks in FORTRAN.

Two 128k-byte memory modules are combined on a single board to form a full 256k bytes of 2-way interleaved memory/card. Memory can be expanded to 1M bytes of local memory; the shared multiport option permits expansion to 2M bytes.

Two logical memory access paths allow concurrent CPU and I/O access capability, resulting in high I/O throughput without interrupting CPU process execution. Memory access overhead is reduced by allowing the I/O processor to execute a previously called instruction or conduct a DMI transfer while the CPU is accessing memory.

Virtual addressing in the system provides ability to address memories longer than 128k bytes, handle multiple dynamic tasks, address fragmented memory in a contiguous manner, and handle dynamic memory allocation.

Configured with 128k-bytes memory, control panel, and hardware floating point, the 7820 sells for $19,400. A 7840 with 256k-bytes memory, control panel, and 8-slot enclosure is $27,800. Shipments are scheduled for fourth quarter 1980.

Circle 426 on Inquiry Card

## Memory System Enhanced With Static and Dynamic 5-V RAM Modules

High speed dynamic and static memory modules added to the Series 90 Memory System family require only 5-V power supplies and can be directly upgraded with higher density modules such as 64k dynamic RAMs. Static memory modules operate at 250 ns. BXP™ bus architecture, designed into the systems by Intel Corp, Memory Systems Operation, 3065 Bowers Ave, Santa Clara, CA 95051, allows choice of word lengths from 18 to 88 bits, and permits static and dynamic modules to be mixed in a single system.

Replacing the original series which required three power supplies, CM-90 dynamic memory modules are built using 2118 16k-bit HMOS RAMs. Modules to be built using 64k HMOS RAMs will plug directly into CM-90 sockets allowing users to quadruple storage capacity with no system modifications. Also under development are 5-V replacements for 400- and 300-ns dynamic memory modules.

Operating at a 250-ns cycle time and storing up to 64k bytes, CM-92 static memory modules require 50% less power than previously available 100- and 140-ns modules. Built using 2141 4k-bit HMOS static RAMs, the modules operate on a single 5-V supply.

Circle 427 on Inquiry Card

## Small Business Computers Provide Users with Price/Performance Options

Enhancements to 2200 series computers present a range of options to entry level users. SVP and LVP small business computers, PCS-III, 2280 disc multiplexer, and IDEAS business application software were included in the announcement made by Wang Laboratories, Inc, One Industrial Ave, Lowell, MA 01851.

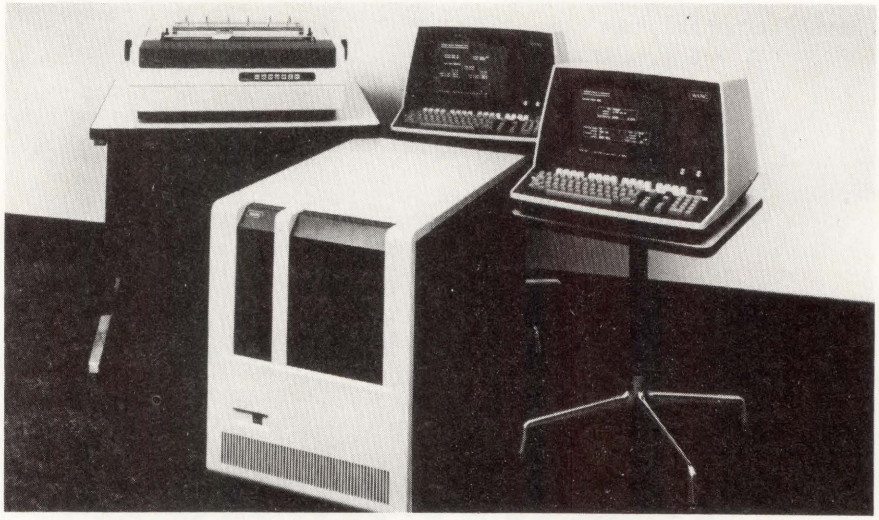
A single-user system, the SVP, programmable in BASIC-II, is offered with a 32k-byte processor, 2236 terminal, and double-density diskette. The system expands to 64k bytes and can support a 120-char/s printer, a second diskette, or 2M- or 4M-byte Winchester drives.

The high performance LVP supports up to four concurrent users. Features include a 2M-, 4M-, or 8M-byte fixed disc storage system. Fast backup is supplied by dual-sided double-density diskettes which are format compatible with IBM 3741 diskettes and store 1M-byte each. User memory is available in 32k-, 64k-, or 128k-byte modules. 60k of machine memory removes most overhead from user memory.

Forming the low end of the series the PCS-III small business computer replaces the PCS-II. Use of double-density diskettes provides 140k-bytes capacity/drive with considerably improved data access speeds. This unit supports BASIC language programming.

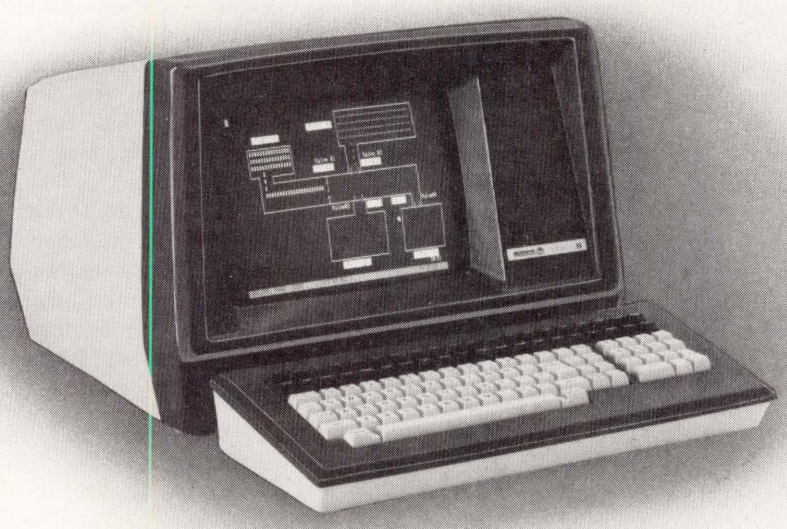
IDEAS (Inquiry Data Entry Access System) software consists of system utilities that enable development of packages for data entry, inquiry, file management, and report generation applications. The software is designed to run on the entire series and to require minimal programming skills.

Circle 428 on Inquiry Card



Advanced technology of the multiterminal 2200 LVP computer system from Wang Laboratories allows faster computing and larger storage capacity within compact, expandable system. System uses 1M-byte dual-sided, double-density diskette and 2M-, 4M-, or 8M-byte fixed disc. User memory expands from 32k to 128k bytes

# BEEHIVE'S terminal family is designed for OEM planning



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CIRCLE 122 ON INQUIRY CARD

## Business Computer Systems Expand to Use up To 32 Peripheral Devices

Control Center 2 is modular in design to permit incremental expansion from a basic system to one using more than 32 peripheral devices. Within the system, Infotecs, One Perimeter Rd, Manchester, NH 03103, has provided a decentralized system architecture for improved performance.

A basic system, consisting of CRT/keyboard terminal, 150-char/s impact printer, dual-drive floppy disc, two processor boards, and power supply housed in a control cabinet, runs a variety of software packages. Multiple dedicated CPUs (DPUs) are used to concurrently control operation of various system elements. As devices are attached to the system, additional DPUs are added to control them. This eliminates the CPU slowdown usually encountered as traffic load increases.

Five different option boards plug into the 32 slots available. Each board functions as a controller for a device and includes its own microprocessor with 32k bytes of memory. A CRT and printer controller, floppy disc controller, multiprinter controller, and general purpose controller for communications and other devices comprise the options.

The floppy disc drive uses two single-sided, double-density diskettes with capacity for storing 1M-char each. Provision is made in the control cabinet for a second drive which raises capacity to 4M char total. Further storage is available with cartridge disc units having 34M, 68M, or 102M char capacity. Up to eight of these units can be added to the system.

System CRT/keyboard terminal has a separate 97-key keyboard layout with standard typewriter features and numeric keypad. CRT has 12″ (30-cm) viewing area displaying 1920 char in 24 lines. In addition to the 150-char/s printer, a 340-char/s dot matrix model, a 300-line/min band printer, and a 55-char/s letter quality machine are available.

Systems can be configured with as much as 800M char of online storage. Up to 16 CRT terminals can be used. The number of printers can expand to 24 including 8 system printers plus 16 printers associated with CRT terminals. Communication occurs through an RS-232 interface.

Circle 433 on Inquiry Card



## Multiuser COBOL System Operates on DS990 Business Computers

COS990, a multiuser COBOL system for Texas Instruments DS990 model 1 and 2 business computer systems, features a flexible job description language and is source compatible with TI's DX10 COBOL. The package, developed by Ryan-McFarland Inc, 2111 N Mays, Round Rock, TX 78664, makes 30k bytes available to user programs in a 64k-byte computer. Directories, path names, and file types are logically equivalent with those of the DX10 operating system.

A flexible job description language makes provision for parameter passing, conditional execution, batch streams, and access control of over 64k levels. Compiler, cross-compiler, and conversion utilities operate on the DX10.

Circle 434 on Inquiry Card

## Packages Extend Word/Data Processing System Capabilities

Operating system packages, introduced by Alpha Professional Systems, 9465 Wilshire Blvd, Los Angeles, CA 90212, extend the capability of the company's Alpha System 7 word/data processing systems. The Pegasus operating system features data communication, word processing file merge, simultaneous printout of multiple queued documents, and financial computation.

Transfer of word/data processing files and correspondence at 300 to 2400 baud is facilitated by the communications package, allowing online conversation between workstations. Simultaneous printout permits documents up to 220k characters long to be queued to the printer. The system's file merge package allows a name and address file or other file to be merged with other word processing files. The financial program incorporates 23 separate functions including loan amortization, sinking funds, commercial paper, yields, depreciation, and future values. □

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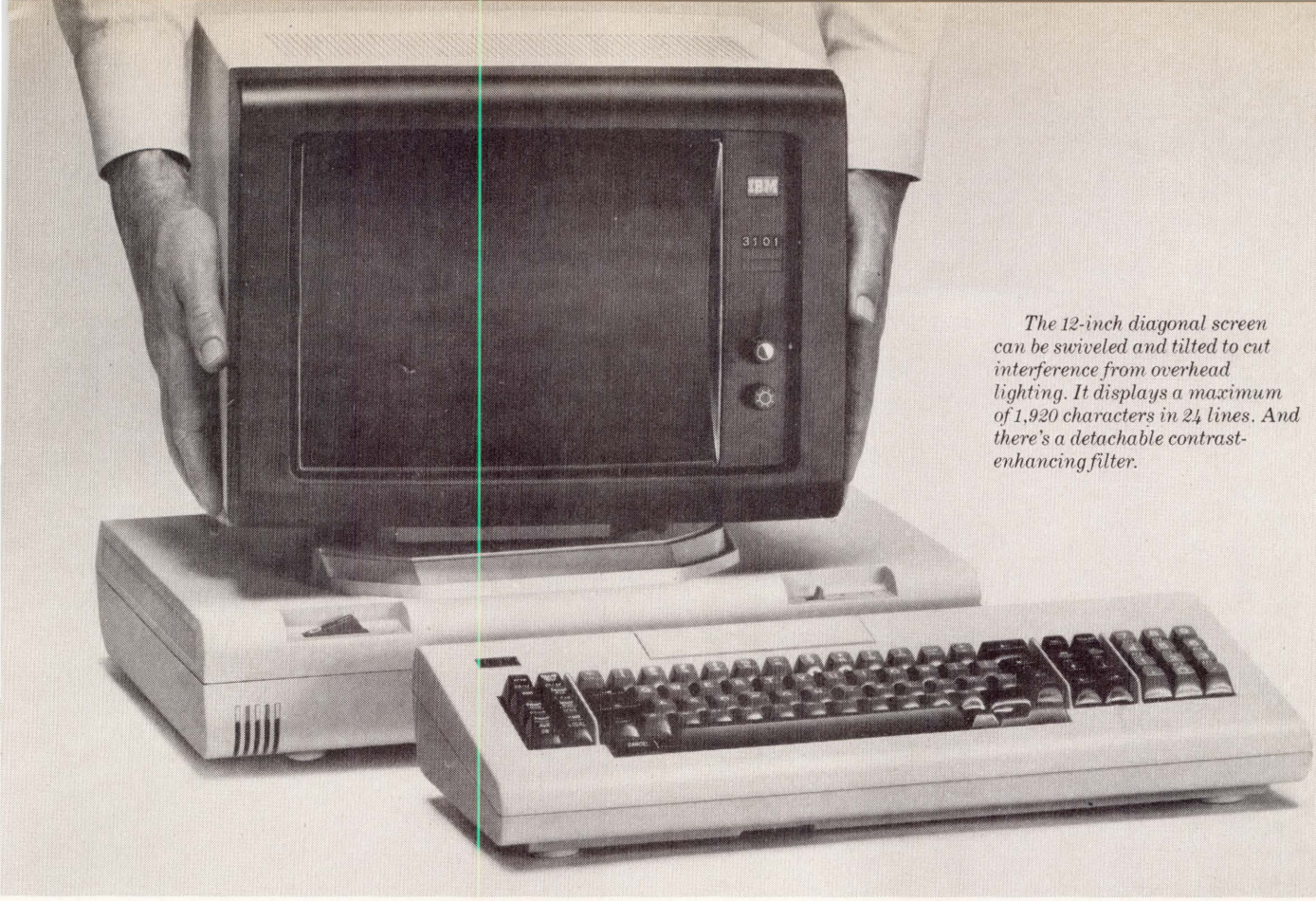


*The 12-inch diagonal screen can be swiveled and tilted to cut interference from overhead lighting. It displays a maximum of 1,920 characters in 24 lines. And there's a detachable contrast-enhancing filter.*

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# Energy Production Monitoring and Control Stressed at Annual Instrumentation Conference

As might be expected under present energy crisis conditions, a large number of papers presented at IECI '80 in Philadelphia were concerned with monitoring, controlling, and distributing energy. Several speakers at this 6th Annual Conference of the IEEE's Industrial Electronics and Control Instrumentation Society discussed solar power systems, while others covered hydroelectric generation, heating/ventilation/air conditioning equipment, and system simulation. For a review of other IECI '80 papers, see *Computer Design*, June 1980, pp 70-83.

## Hydroelectric Control

Results of a study conducted by the New England River Basin Commission have backed up a control system project involving hydroelectric power. That study pointed out that almost 10% of the total regional electric power requirements could be provided through use of existing but mostly abandoned dam sites. Generation capacities from these dams could be added to the overall power net for use in peak periods.

The feasibility of microprocessor control of small scale hydroelectric generation facilities was studied at the Massachusetts Institute of Technology and a system configured.[1] Bases for the system included automatic operation of the facilities and elimination of expensive mechanical regulators. Some basic requirements were that the system would be able to decide when to function (thus saving its generation potential for peak load periods); that once a start decision is made, the system would be able to effect a gradual increase from standstill to synchronous speed; and that once connected to the power distribution network, the reactive power would be kept positive and a target real-to-reactive power ratio would be maintained. In addition, the system would, of necessity, be able to monitor the facilities to enable shutdown if malfunctions occurred.

Fig 1 shows how signals corresponding to generator voltage, bus voltage, real power, reactive power, generator

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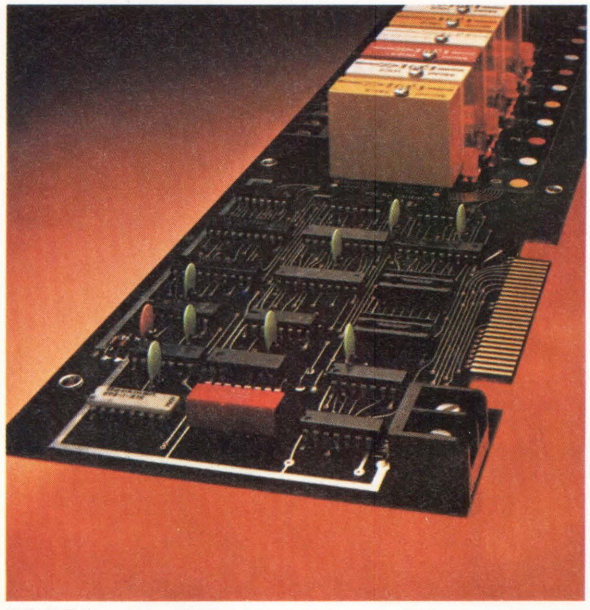

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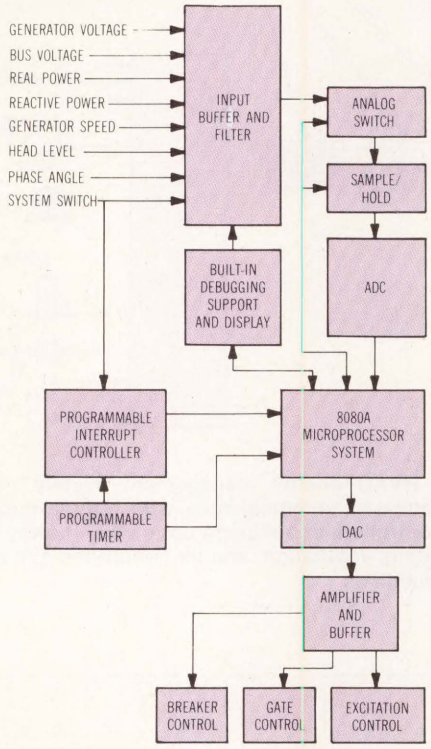


Fig 1 Hydroelectric generation facility control system.[1] Analog input signals from generator are multiplexed under control of microprocessor, then converted to digital format for processing. Microprocessor output signals, converted to analog, are used to control generator and dam site functions

speed, phase angle, and head level are normalized and passed through an analog multiplexer operating under control of the microprocessor. Selected signals are further sampled and digitized by the interface circuitry before being input to the microcomputer. Analog signals are output through DACs and appropriately scaled for control of the flood gates and the field excitation. A digital signal controls the distribution system connection breaker.

Special purpose timing hardware and the basic 8080A system handle a variety of timing and counting functions, thereby maintaining the system's flexibility while freeing

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the processor for performance of more time-critical activities. An interrupt controller monitors changes or failure conditions that require immediate attention. Priority level of the interrupt can be adjusted by the software to accommodate varying expectations as the system goes through different phases of operation.

Results of initial tests using a generator facility simulator indicate success in eliminating the need for a mechanical governor, providing the plant output remains very small in comparison with bus power. In addition, nearly all the problems encountered during the testing were remedied easily.

### HVAC Control

Energy management, in a 7-building facility, has been implemented to control separate heating, ventilation, and air conditioning for each building.[2] A central microcomputer, located in the boiler room of one of the seven buildings, acts as the master for remote microcomputers in the equipment room of each building (Fig 2). Equipment being controlled includes high powered fans, various dampers to control air flow through the building, and chilled-water valves to control cooling levels in the summer and reheat coils in the winter.

Central hardware (Fig 3) is based on an Intel SBC 80/20 single-board computer, comprised of an 8080A microprocessor, 4k bytes of RAM, sockets for 8k bytes of ROM, an 8-level interrupt controller, RS-232 channel for a printer, timers, and 48 parallel I/O lines. An expander board increases system program capacity by an additional 32k bytes, and SBC 534 4-channel communication boards provide

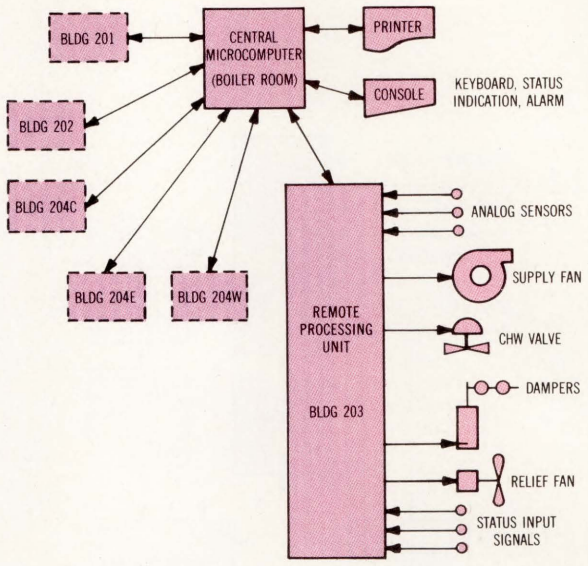


Fig 2 HVAC energy management system.[2] Central microcomputer communicates with remote microcomputer controllers in buildings up to 4000 ft away to control heating, ventilation, and air conditioning in each of seven buildings

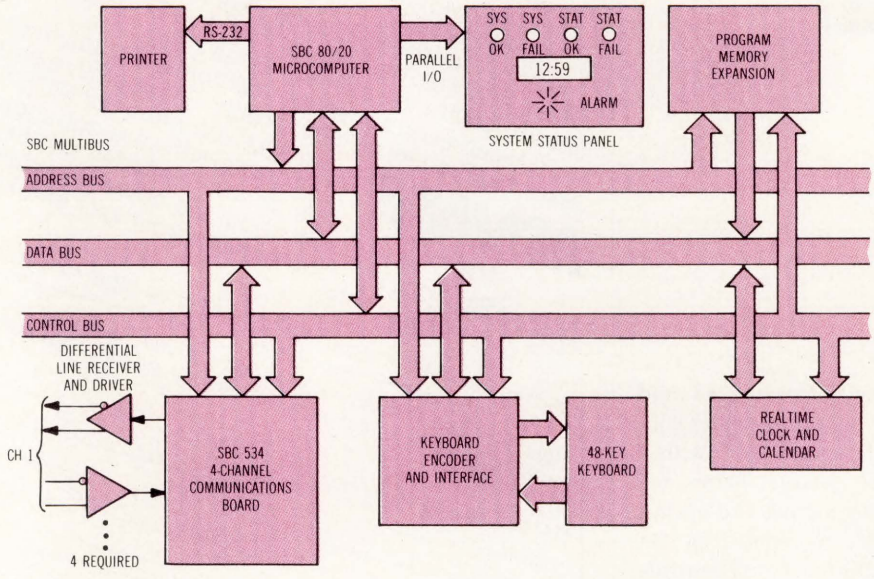


Fig 3 HVAC system central microcomputer hardware.[2] SBC 80/20 single-board computer interfaces with operator via printer and remote processors through dedicated serial communication link. It also executes energy control algorithms and system scheduling functions, and generates status logs and environmental reports

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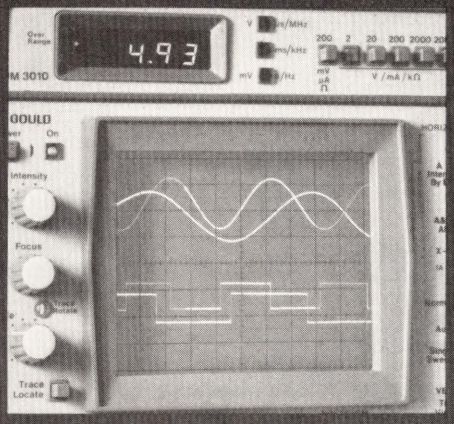


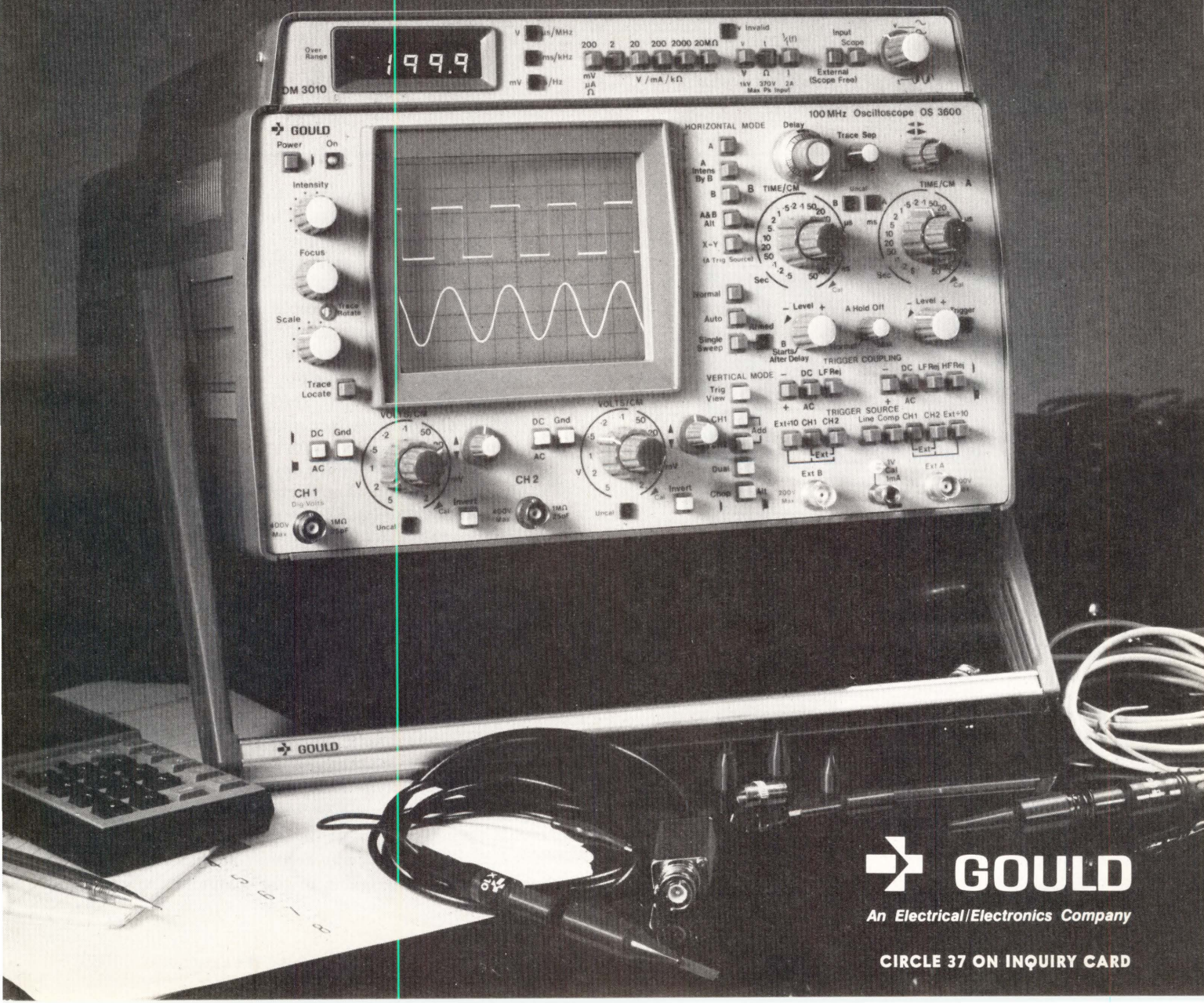


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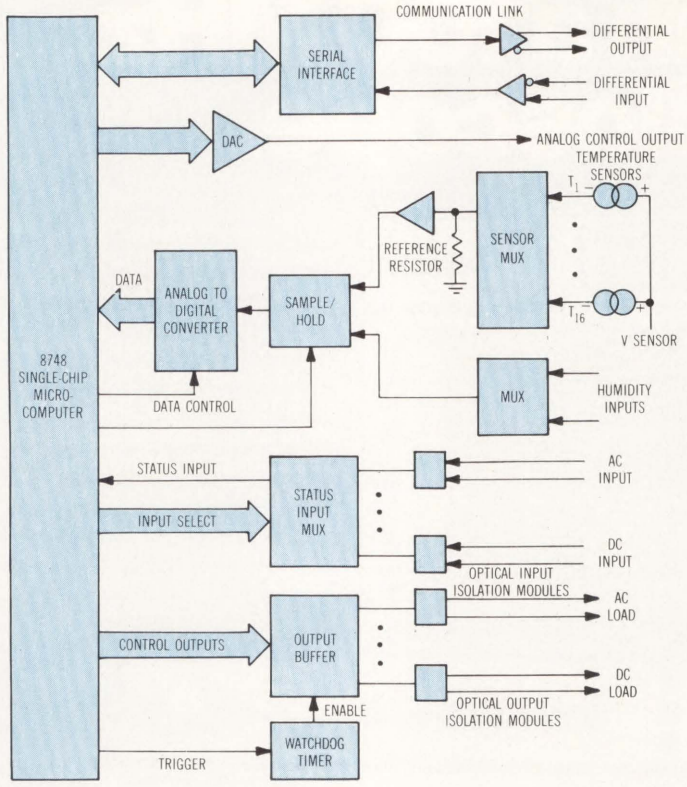


Fig 4 HVAC remote controller.[2] 8748 single-chip microcomputer in each building accepts commands from central microcomputer to regulate environmental conditions in that building

needed system channel capacity. Keyboard encoder, differential line drivers and receivers for the 4000-ft (1220-m) long link, communications realtime clock, power-fail detection circuits, and battery charger are on a separate interface board. During the design sequence, NMOS RAM on the computer board was replaced with CMOS devices.

Functions of the central microcomputer include communication through a dedicated multichannel serial communication link with the remote processor units that gather status information from their respective buildings, plus dissemination of appropriate control information to the remote processors. Interface with the operator is via a printer and a dedicated-function keyboard.

The remote processors (Fig 4) are Intel 8748 single-chip microcomputers containing 1k bytes of EPROM, 64 bytes of RAM, a timer/counter, and 27 I/O lines, all onchip. One type of command from the central microcomputer causes the remote processor to gather data, both analog and digital, and send them to the central unit. A second type of command consists of analog and digital control data for the appropriate outputs.

Each remote processor controls a 24-channel analog data acquisition subsystem, with 16 channels dedicated to inputs from temperature sensors that respond to temperature changes at a rate of 1 mA/°K. The remaining 8 channels are used for inputs from humidity transducers.

Although this prototype computerized energy management system is now in operation, and there is no doubt that substantial savings will result, insufficient operating time has been built up to provide an accurate assessment. In the meantime, work is progressing to add computer control to other buildings.

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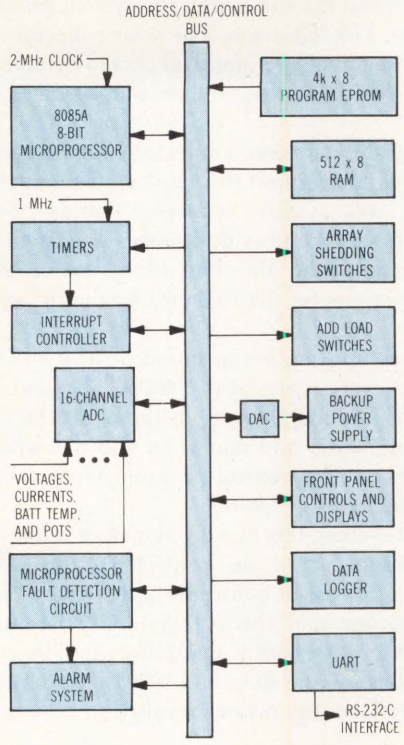


Fig 5 Photovoltaic power system controller.[3] As many as 33,600 photovoltaic cells are online except when overvoltage conditions require some cells to be temporarily shed

## Solar Power Generation Control

A microprocessor based controller for a photovoltaic power system designed by the Massachusetts Institute of Technology Lincoln Laboratory will provide more than 80% of the energy used annually by radio station WBNO in Bryan, Ohio.[3] The 15-kW peak power system, with predictable and constant dc load, went into operation on August 29, 1979.

Four major power components—array, battery, backup power supply, and load—are in the system. The array, which covers 0.33 acre (0.1 hectare), is configured as 100 4 x 8-ft (1.2 x 2.4-m) racks containing 33,600 photovoltaic cells. A 40-kWh lead-acid battery contains 60 cells connected in series to provide a nominal 120-V output. The ac to dc backup power supply has an output voltage range of 100 to 160 V at 40 A maximum. The am transmitter, plus studio equipment and production rooms, make up the load.

When the sun is shining and solar output is large, the array supplies all the current to the load. Excess current is used to charge the battery. If any rapid changes occur in bus voltage, as happens when the sun suddenly emerges from behind a cloud, array strings are shed to prevent overvoltage. When solar output drops to less than the load requires, the battery supplements load demand until solar power returns.

The system controller is an Intel 8085A microprocessor (Fig 5) with a 1-MHz internal clock frequency. Program memory storage is maintained in Intel 8755A and 2716 2k x 8 EPROMs. An 8156 256 x 8 RAM and two 5101 256 x 4 RAMs provide read/write storage. Analog voltages and currents are input through an Analog Devices RTI-1220 16-channel multiplexed 12-bit ADC that is interfaced to the bus as a memory mapped I/O device.

I/O ports in the 8755A and 8156, plus four 8255A programmable peripheral interfaces, provide all the digital I/O ports. A 6-bit binary output controls the array shedding switches. This output is decoded into n out of 50 "shed" signals at the switches. A group of six individual bits controls the six additional load switches. An 8-bit output applied to a DAC sends an analog control voltage to program the output voltage of the backup power supply.

Highest priority in the software interrupt routines is the control program (Fig 6). This routine measures analog voltages and currents of interest and compares them to alarm limits.

Except for three days during an inverter failure and three days for system modifications, this system has remained in operation. All design objectives have been met throughout a variety of weather conditions.

*(continued on page 74)*

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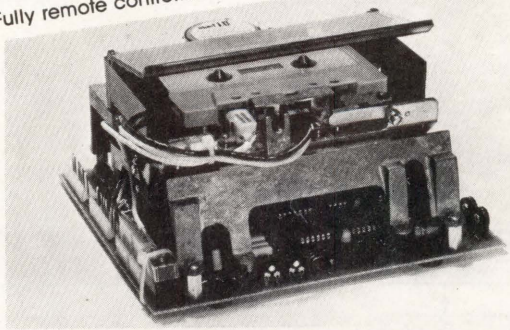
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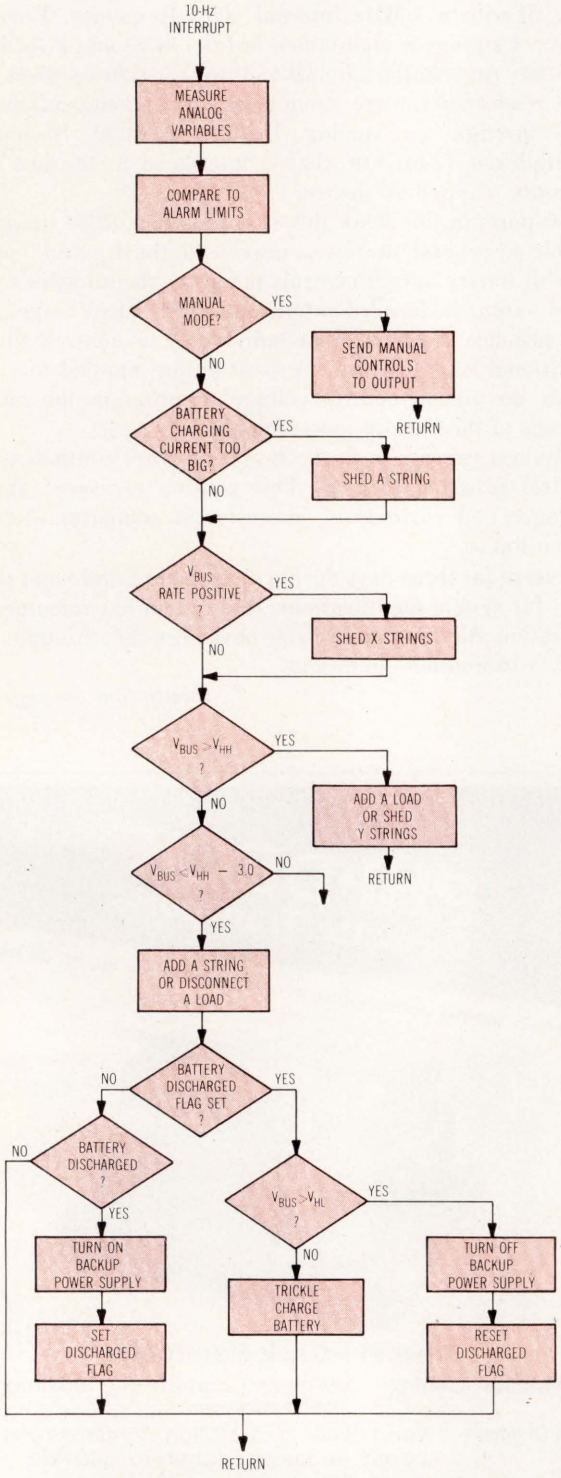


Fig 6 Photovoltaic power system control program.[3] Analog voltages and currents are compared to alarm parameters to determine condition of the system

A second solar energy system involves a 2-axis tracking controller for a concentrating collector.[4] In this system a controller based on a 6502 microprocessor commands a 70-kWh collector designed for high performance, low cost operation. When the sun is out, the system produces 250 to 650 °F (50 to 170 °C) steam. The solar collector is a Fresnel reflector made up of 108 identical curved columns that each hold eight 1-ft (0.3-m) square, second-surfaced, flat, glass mirrors.

Address and data buses connect the microprocessor to interface chips. Main input device is a 16-channel multiplexing 8-bit ADC. Light sensors, shadow bands, and temperature sensors provide analog signals that are connected directly to the ADC. Potentiometers on the collector provide A-D inputs for the collector's azimuth and elevation positions.

Temporary information is stored in RAM and the control program firmware is stored in EPROM. The control program uses 24 bytes of RAM, but larger blocks of RAM can be used for data acquisition and operation and maintenance information storage. The control program is modular and uses less than 750 bytes of EPROM.

In a third system, this one developed in Italy, Z80 and 6800 microprocessors serve as controllers for solar energy plants.[5] The Z80 based controller uses three 128-byte RAMs for data storage and three 1k-byte EPROMs for program storage. The 6800 based controller functions with two 128-byte RAMs for the data and two 1k-byte P/ROMs for the program. Both configurations resulted in economic systems.

## References

All of the following items are from the *IECI '80 Conference Proceedings.*

1. D. V. Le and S. I. Ross, "A Microprocessor Based Low Head Hydroelectric Generation Facility Control System," pp 193-197
2. A. Abramovich, "Microcomputer System Design for Remote Process Control," pp 247-251
3. C. H. Much and P. J. Rothenheber, "Microprocessor-Based Control of the Photovoltaic Solar Power System for an AM Radio Station," pp 210-216
4. D. N. Borton and W. E. Rogers, "A Microcomputer Based 2-Axis Tracking Controller for a Concentrating Solar Collector," pp 252-256
5. P. Cerami *et al*, "Experiences in Using Microprocessors for Solar Circuit Control," pp 257-263

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Copies of the *IECI '80 Proceedings, Applications of Mini and Microcomputers,* containing the text of most regular session papers presented, are available from the IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. (Catalog #80CH155-1.) The price is $25/copy.

IECI '81, again covering applications of mini and microcomputers, will be held in San Francisco from November 9 through 13. Tutorial and special evening panel sessions will be included.

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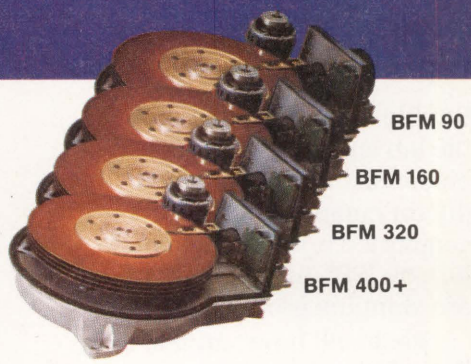


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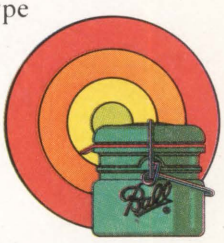

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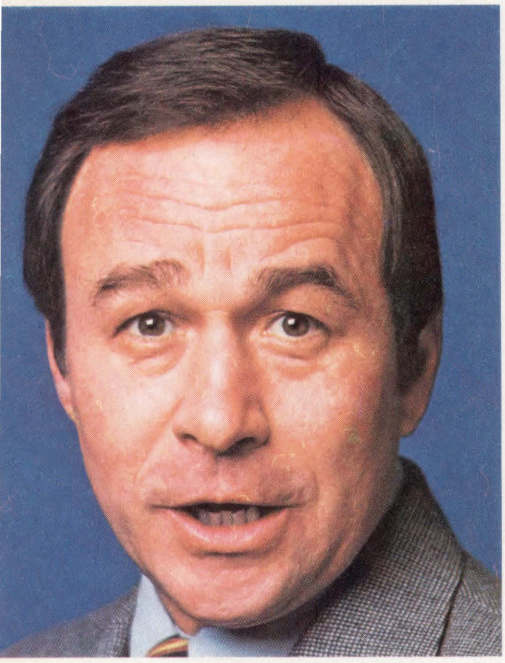
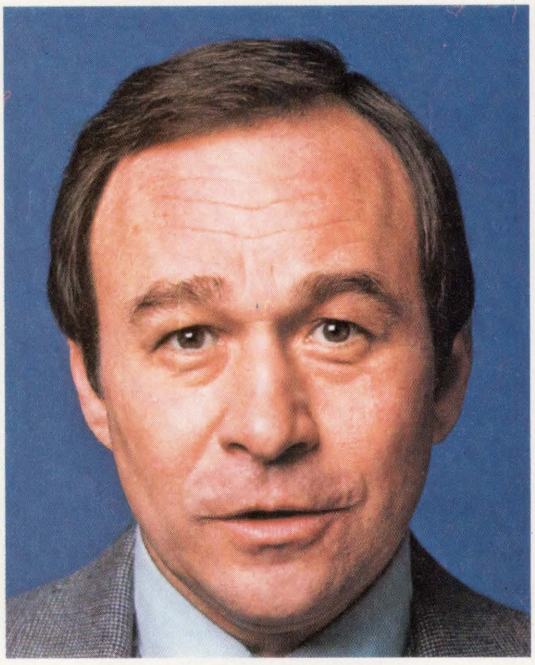
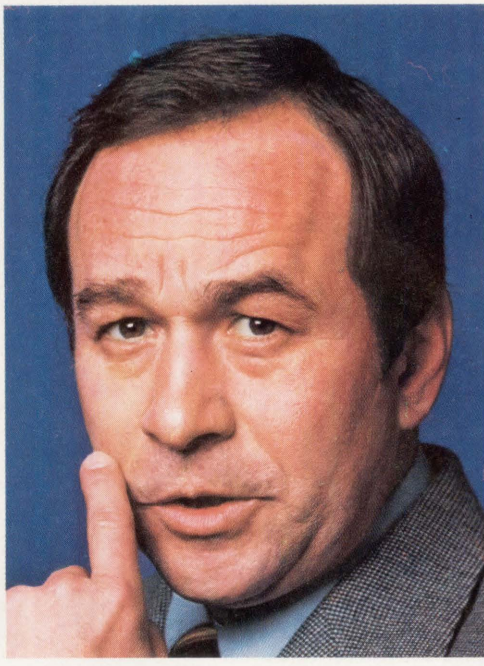
# 6 questions the V. may ask you about







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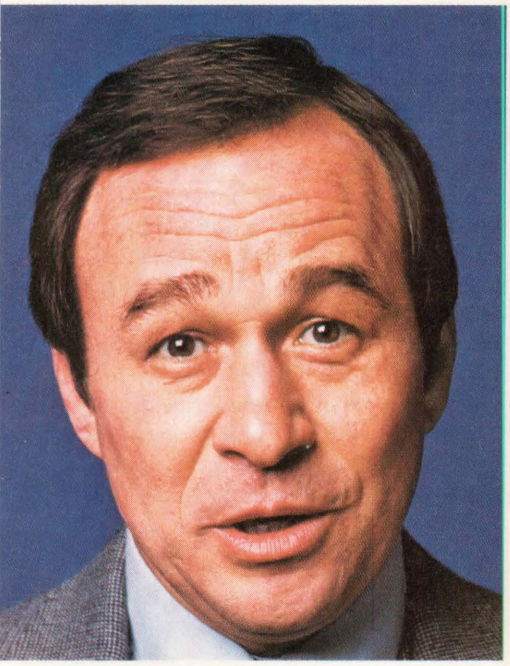
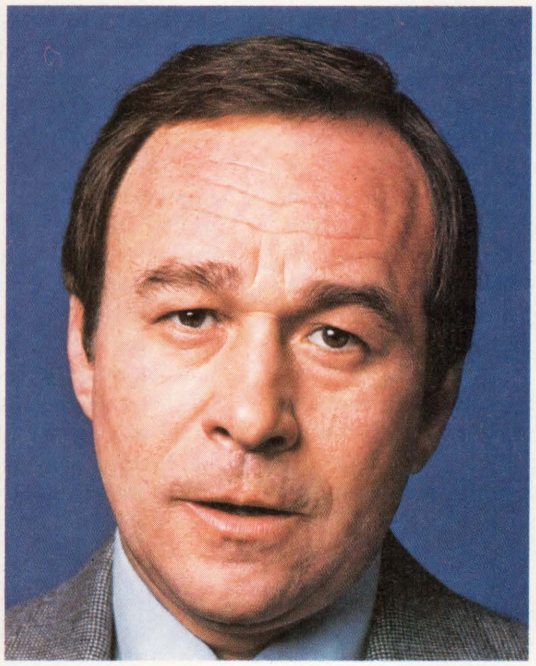
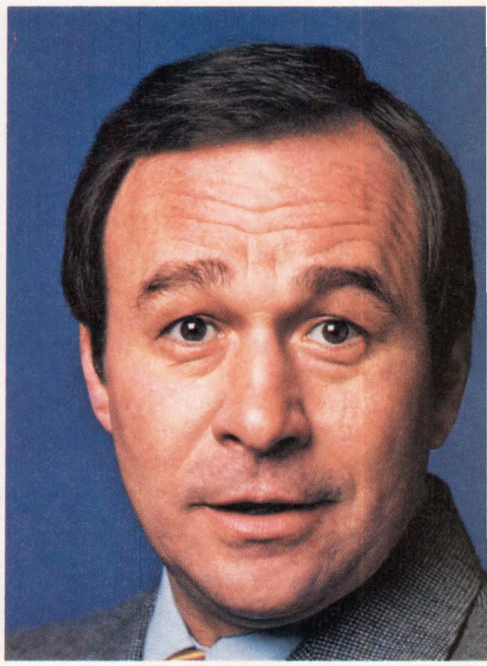
MicroPower

# P. of Engineering bubble memories.







## What bubble products are available now?

Another company has a 92K bit device in production, and Rockwell International is in production of a 256K bit device. Two other companies are now sampling their 256K bit devices. Three companies have announced megabit devices.

Rockwell devices are also available on memory board systems.

## What kinds of applications are best suited for bubbles?

Applications where modularity in 32K byte increments up to 8M bytes is required; where electronic equipment must withstand unclean conditions; where size or packaging flexibility is important; where memories must operate for long periods without maintenance; where non volatile, solid state data storage is mandatory.

## How about support circuits for bubble memories?

Most bubble memory manufacturers have committed to the production availability of LSI support circuits by the end of 1980. Rockwell International will have all support circuits and they will be alternate sourced. They will interface with the major microprocessor buses.

To learn more, ask Rockwell. Rockwell International, Bubble Memory Products, Electronic Devices Div., P.O. Box 3669, RC-55 Anaheim, CA 92803. (714) 632-3729.

CIRCLE 41 ON INQUIRY CARD

Rockwell International

...where science gets down to business

## Add-In Boards Increase Minicomputer Industrial Control Capabilities

Among the enhancements introduced by Computer Automation, Inc, 2181 Dupont Dr, Irvine, CA 92713, for its Naked Mini[R] 4 minicomputers are a pair of 64-bit TTL I/O interface modules and four single-board function boards specifically intended for the Scout[TM] 4/04 version. The latter provide mass storage capabilities, analog output, digital parallel I/O, and battery backup with watchdog timer.

Both of the interface modules allow a variety of I/O data formats to be monitored by the computer, including four 16-bit words or up to 64 discrete stimuli such as switch closures. Byte or word data formats are supported with each module. Onboard terminating resistors are provided to eliminate the need for a terminator board. The half-card modules can handle positive and negative true input or output. Latched or transparent inputs can be interfaced to the processor.

The input module features switch-selectable interrupt addresses. Eight external strobe lines work in conjunction with eight acknowledge signal lines to provide a handshake interface. Data then can be transferred in response to an external event using interrupts or through periodic status scanning.

Of the Scout boards, one, a 512k-byte flexible disc subsystem, consists of a dual-drive, single-sided floppy supported by a single-function controller board that operates under the realtime executive. It is format compatible with all NM4 family computers for transportability of application programs and data files.

A 32-bit bidirectional I/O board uses interrupt driven programmed I/O, which enables division of the 32 bits into 8-bit groups. Data can be transferred in and out in any combinations totaling four groups. The third board, a 4-channel DAC, offers output voltage ranges of ±2.5, ±5, 0 to 5, ±10, and 0 to 10 V, all switch selectable for each channel.

The battery backup board provides temporary power to memory ranging from 3 min for 128k bytes to 4.5 min for 32k bytes of dynamic RAM. A watchdog timer provides a signal to an external alarm when the CPU fails to activate the battery backup within a predetermined time frame ranging from 1 to 30 s.

Circle 442 on Inquiry Card

## Manual Data Input Unit Expands Machine Tool CNC Capabilities

Capability for an operator to program a milling machine for automatic 3-axis contouring is provided by a manual data input unit introduced by Bendix Corp, Industrial Controls Div, 12843 Greenfield Rd, Detroit, MI 48227. The computer numerical control features conversational programming between the operator and the control via a 9″ (23-cm) CRT display that shows both what to do and what occurs when the program is entered into the control through the keyboard. Once a program is set up and the part machined as verification, the program is stored for future use.

Part program storage is included for approximately 480 events, and programs can be loaded to or from teleprinter, magnetic tape cassette, or RS-232-C interface. Program data are similar to EIA format. Full editing is standard.

Operator aids include double-size position readout data, reverse video of active data, fault display, and messages. Optional polar coordinates can be substituted for standard cartesian coordinates.

Circle 443 on Inquiry Card

## Handheld Terminal Communicates With Central Computer

A system based on infrared light, mobile entry stations, and stationary data collectors allows personnel to input data via hand calculator size portable terminals for transmission to a central unit. Infrared light, which is not susceptible to electromagnetic interference and therefore performs well in a large assembly line atmosphere, carries data to and from terminal and collector.

The battery powered terminals, introduced by Siemens AG, Postfach 103, D-8000 Munich 1, Federal Republic of Germany, are not marketed in the U.S. but are available elsewhere. Data communications is carried out by transmitting and receiving diodes. In the data collectors, signal converters and line drivers move the data signals via a modem to the next interface. Transmission speed in both directions is between 2400 and 4800 baud.

# Vincent van Dumb.

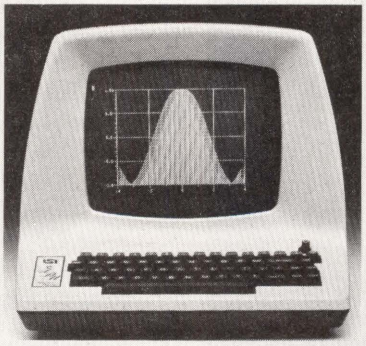
The Dumb Terminal® video display terminal has done it again.

For around $2000, you can have all the alphanumeric capabilities of the renowned ADM-3A Dumb Terminal, plus the full vector drawing and point plotting capabilities of a sophisticated graphics terminal. All in one neat package. That's less than half the cost of other comparably equipped graphics terminals.

The ADM-3A with Retro-Graphics™ gives you complete flexibility to develop bar charts, pie diagrams, histograms, even function plots. What's more, it's completely Tektronix® Plot 10™ software-compatible.

The package consists of an ADM-3A Dumb Terminal plus a single plug-in card engineered to fit neatly inside the ADM-3A without soldering, special tools, or a service call.

Retro-Graphics is a product of Digital Engineering, Inc., and is sold separately or installed in the ADM-3A by local Lear Siegler distributors. Contact the distributors listed below, any Lear Siegler sales office or Digital Engineering, Inc., 1775-C Tribute Road, Sacramento, CA 95815, 916/920-5600.



**DUMB TERMINAL. SMART BUY.**

LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

The Retro-Graphics-equipped Dumb Terminal. What does it mean to you?

Draw your own conclusions.

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DISTRIBUTORS: • Oakland, CA, Advanced Technology (415) 452-1401 • Oakland, CA, Consolidated Data Terminals (415) 638-1222 • San Diego, CA, Data Systems Marketing (714) 560-9222 • Orange County, CA, MQI (714) 751-2005 • Los Angeles, CA, David Jamison Carlyle Corp. (213) 277-4562 • Richardson, TX, Data Applications (214) 931-1100 • Hazelwood, MO, Dytec/South (314) 731-5400 • Chicago, IL, Information Systems (312) 256-5892 • Arlington Heights, IL, Dytec/Central (312) 394-3380 • St. Paul, MN, Dytec/North (612) 645-5816 • Orlando, FL, Gentry Associates (305) 859-7450 • Cleveland, OH, W.C. Koepf Associates (216) 247-5129 • Falls Church, VA, Marva Data Services (703) 893-1544 • Gaithersburg, MD, Leaseametric (301) 948-9700 • Cherry Hill, NJ, Data Store (609) 779-0200 • Stamford, CT, National Computer Communications (203) 325-3831 • Bedford, MA, Continental Resources (617) 275-0850.

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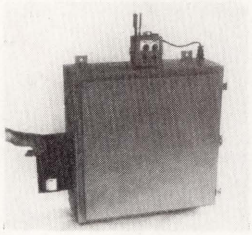
CIRCLE 42 ON INQUIRY CARD

## Floppy Disc Drive Retrofit Expands NC Machine Tool Memory



Whether acting as a standalone unit or as the final node of a computer system network, the FLOPPYMEM extends both editing and communications capabilities of machine tool systems. In addition to bypassing the tape readers and expanding the memory capacity to 156k char of parts program (equivalent to 0.25 mi or nearly 0.5 km of tape), the floppy unit eliminates reliability problems such as dirt and wear and speeds up operations.

Alden Computer Systems Corp, PO Box 985, Framingham, MA 01701, retrofits the floppy disc drive and microcomputer to any NC or CNC machine tool on a turnkey basis. The unit can be controlled from the control console as was the tape reader. Field applications indicate increases in cutting speed by three to five times.

Circle 444 on Inquiry Card

## Graphic Display Package Increases Programmable Controller Capabilities

Adding a GRPHPK display package and an intelligent color graphic CRT terminal provides the EPTAK$^R$ programmable controller with features normally found on larger computer based process control systems. Included in the features are direct digital control of master and slave loops and alarms, process and alarm displays, dynamic and historical trending, and process and alarm logging. Control loop trim parameters can now also be defined by the user.

With this package, introduced by Eagle Signal Industrial Systems, 736 Federal St, Davenport, IA 52803, a user can design the process display, define control requirements, and operate the process. The programmable controller communicates with the CRT through standard system interface modules; the operator interfaces to the system through the terminal's keyboard.

An autotracking feature provides bumpless transfer between manual and automatic control. Autotransfer to backup automatically forces a backup station to assume control of a loop if a failure occurs in the system.

Circle 445 on Inquiry Card

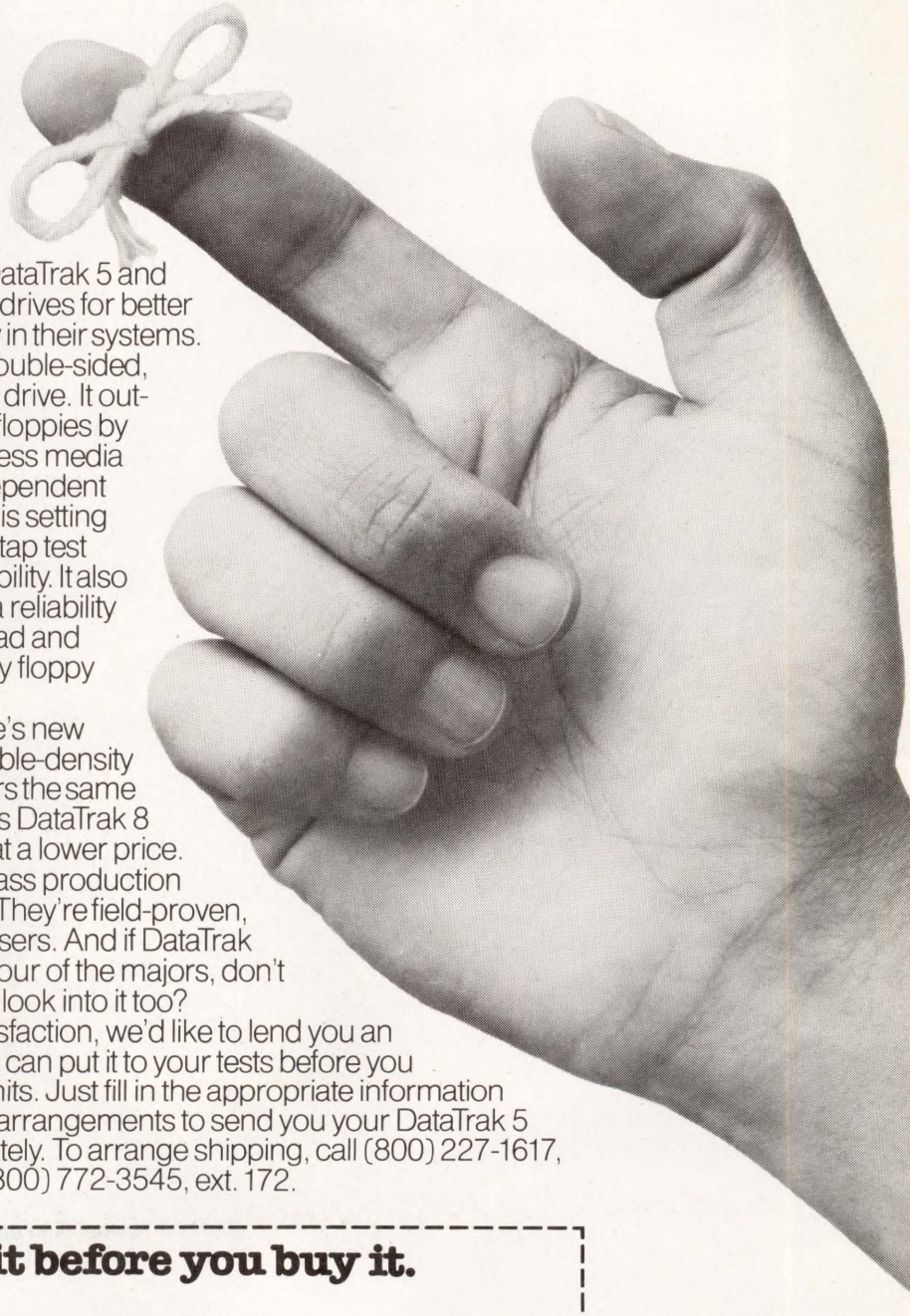
## Speech Synthesis Technology is Applied To Automotive Diagnostic System

A prototype automotive diagnostics warning system shown at the 1980 Society of Automotive Engineers Congress and Exposition converts inputs from a microcontroller into audible warning messages. This application of speech synthesis technology was demonstrated by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, and is based on that company's recently announced speech processor chip plus a memory device containing the words or phrases to be spoken. In this technique, a recorded word or phrase is digitized with A-D conversion, the code is compressed by a factor of 100 and stored in ROM, and that word or phrase is played back through the speech processor chip.

The information stored in memory is actually that of recorded speech, and therefore the vocabulary can incorporate virtually any word or phrase including male and female voices or a foreign language. However, because requirements differ, all speech synthesis applications using this device are dedicated, custom products.

Speech quality is said to be comparable to that of a high fidelity magnetic tape recording and is related to the number of bits of memory used to store the speech. By decreasing memory size the quality of the speech is reduced so it can be tailored to the specific application and the amount of memory desired. Approximately 1200 bits are needed to store an average length English word. A female voice or a foreign language requires approximately 40 to 50% more memory. □

# Why 3 out of 4 major OEMs can't keep our memories off their minds.



**DataTrak 5™ and DataTrak 8.™ Our unforgettable memories.**

More and more major OEMs are turning to DataTrak 5 and DataTrak 8 floppy disk drives for better efficiency and reliability in their systems.

DataTrak 8 is our double-sided, double-density 8" disk drive. It outperforms competitive floppies by offering considerably less media and head wear. In independent evaluation, DataTrak 8 is setting industry standards for tap test performance and reliability. It also delivers improved data reliability with the fewest data read and track seek errors of any floppy on the market.

DataTrak 5 is Qume's new 5¼" double-sided, double-density floppy disk drive. It offers the same outstanding features as DataTrak 8 in a smaller package, at a lower price.

Both units are in mass production and are available now. They're field-proven, too. By thousands of users. And if DataTrak works for three out of four of the majors, don't you think you ought to look into it too?

To ensure your satisfaction, we'd like to lend you an evaluation unit. So you can put it to your tests before you order any additional units. Just fill in the appropriate information below, and we'll make arrangements to send you your DataTrak 5 or DataTrak 8 immediately. To arrange shipping, call (800) 227-1617, ext. 172; in California (800) 772-3545, ext. 172.

## Try it before you buy it.

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CIRCLE 44 ON INQUIRY CARD

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Maybe it's because there's more to buy.

Digital Equipment Corporation has sold more 16-bit microcomputers than any other company in the business.

Over 100,000 of them.

And the reason is simple. We give you more to work with. More hardware, more software, and more true systems capability.

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So you'll never run out of ways to expand your business.

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You can choose from eight different configurations of our LSI-11/2 and -11/23 micros, in both boards and boxes. With high-performance features like general-purpose registers. Double-precision floating point processor. Up to 256Kb memory addressing. And the full instruction set of the PDP-11 family.

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## More options on the industry-standard bus.

Once you have the micro you want, your possibilities are wide open.

You can choose from dozens of micro products: 9 different memory boards, 11 I/O modules, 9 communications options, even kits for designing your own custom interfacing.

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Digital's micro software is literally years ahead of the competition.

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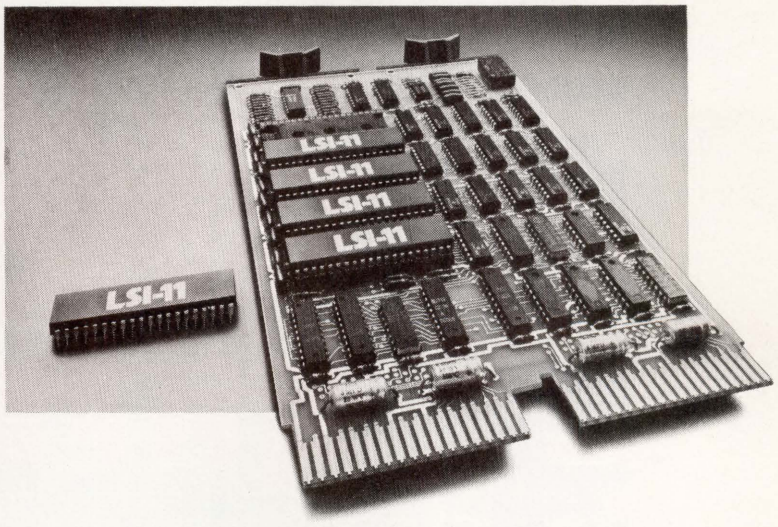


**It took the minicomputer company to make micros this easy.**

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CIRCLE 45 ON INQUIRY CARD

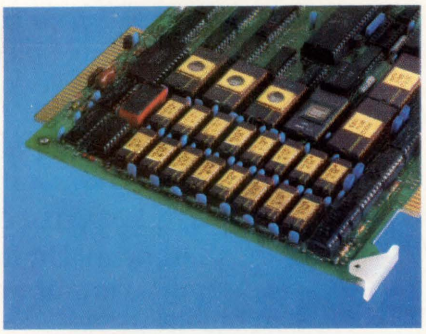
# Expand with the MSC 8009

**MULTIBUS™ compatible.** Designed around the Z80™ CPU, the fully MULTIBUS compatible MSC 8009 is a complete microcomputer, offering OEM designers a number of significant benefits:

**One board takes the place of four.** In many SBC 80 based systems, the MSC 8009 can reduce the number of boards from four or more to only one. This hardware reduction helps lower system costs while increasing capability, throughput, and reliability.

**Floppy disk interface.** An on-board, single chip 1793™ floppy disk controller provides a soft-sector format that can be made IBM compatible. With proper options, up to eight 4 or 8 inch single or double density drives can be controlled.

**CP/M™ compatibility.** Software support for the MSC 8009 includes the CP/M and CP/M-2 operating system which uses IBM-compatible flexible disks for backup storage. It provides users with program construction, storage, and editing, along with assembly and checkout facilities.



Monolithic Systems corp.

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**Extensive memory capacity.** The dual-ported memory can be configured with up to 32K bytes of dynamic RAM. The EPROM section is compatible with standard 1K, 2K, and 4K byte devices to a maximum of 16K bytes.

For additional information on the MSC 8009 and our other 41 Monolithic Systems Corp. products, please contact us at 14 Inverness Drive East, Englewood, Colorado 80112. (303) 770-7400. Telex: 45-4498.

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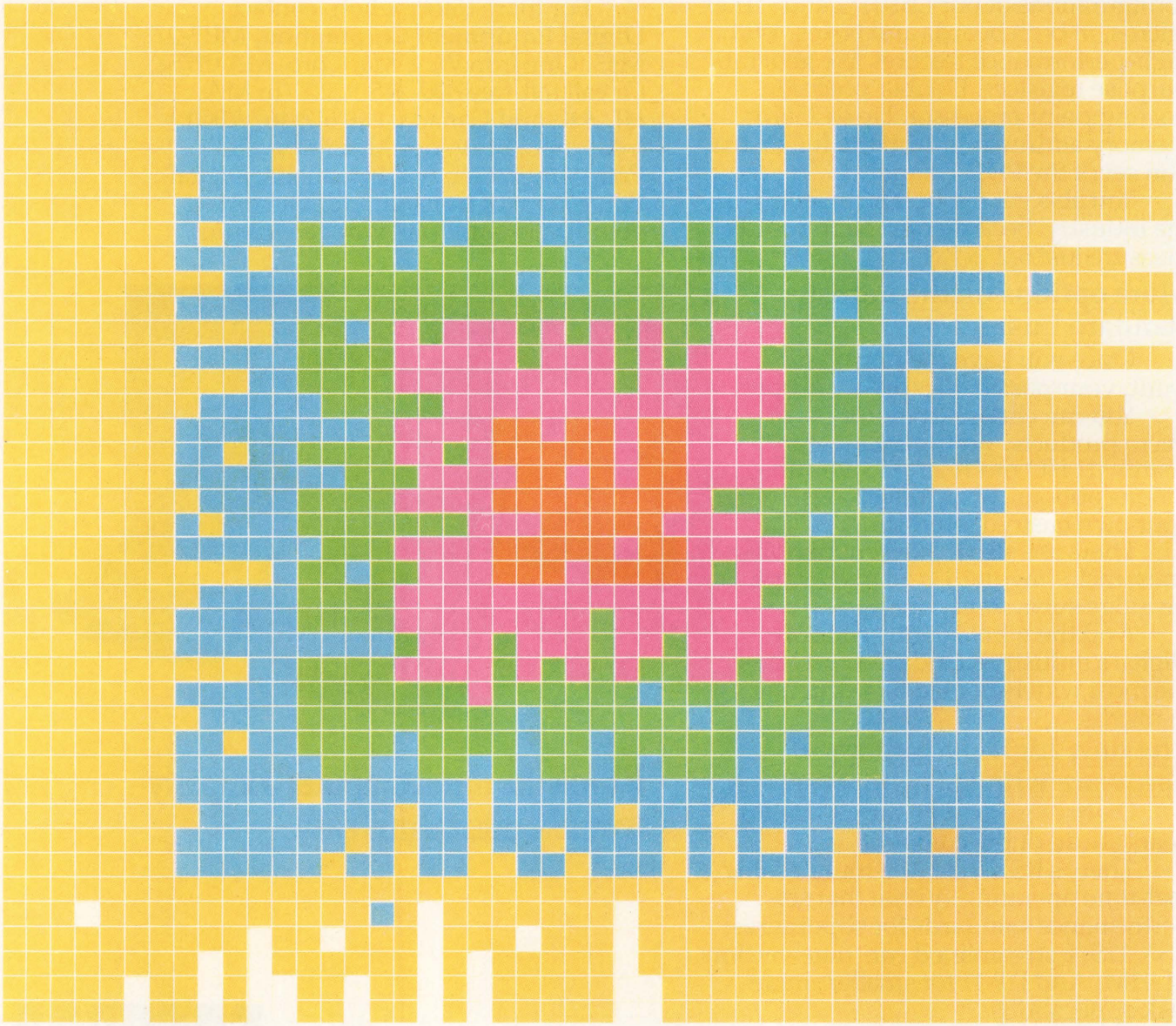
# With on-board floppy disk controller



MSC Regional Sales Offices: **Eastern Region** 1101-B9 State Road, Princeton, NJ 08540, (609) 921-2240; **Central Region** 14 Inverness Drive East, Englewood, CO 80112, (303) 770-7400; **Western Region** 49 South Baldwin, Suite D, Sierra Madre, CA 91024, (213) 351-8717.



**CIRCLE 46 ON INQUIRY CARD**

# ARITHMETIC PROCESSOR CHIPS ENHANCE MICROPROCESSOR SYSTEM PERFORMANCE

Specific interfacing details for two very different devices show how single-chip arithmetic processors can enhance system performance by relieving virtually any microcomputer of complex mathematical calculations, reducing software requirements, and affording the potential for parallel execution of concurrent tasks

**B. K. Gupta** Bhabha Atomic Research Centre, Computer Section
Trombay, Bombay 85, India

General purpose microcomputers require extensive supporting software to perform the complex arithmetic operations required by the many scientific and engineering applications involving process control, data reduction, laboratory instrumentation, and other highly computational tasks. It is worthwhile, then, to consider the use of specialized arithmetic processors as microcomputer extensions to relieve microcomputers of the burden of arithmetic computation. Commercially available calculator chips, the so-called number cruncher chips, and arithmetic processing unit chips lend themselves to such applications. In addition, a number of manufacturers offer hardware multiply/divide chips and general purpose microcomputer cards preprogrammed to perform arithmetic functions.

Selection of a particular arithmetic processor chip (APC) involves careful evaluation of cost, speed, precision, number representation, power consumption, ease of interfacing in the different microcomputer configurations required by the application, and the variety of different functions provided. Although the requirements are determined by the particular application, the basics usually include addition, subtraction, multiplication, division, exponentiation, and square root extraction, all in a choice of fixed point or floating point number representations. Trigonometric, exponential, and logarithmic functions offer a further convenience and often help to reduce program size.

Calculator chip input/output (I/O) systems, consisting of a keypad for entry of instructions or operands and a multiplexed display for visual output, are designed for operator convenience and do not allow for easy installation in a microcomputer based system. In addition to the circuitry for conversion between metal oxide semiconductor (MOS)

signal level and transistor-transistor logic (TTL) signal level, interfacing a calculator chip to a microcomputer involves simulation of keyboard functions for operand or instruction entry and tapping off the result of a computation at the display input terminals, with the number format conversion performed either by hardware or software. For these reasons, adapting a calculator chip to aid a microcomputer in performing arithmetic operations involves significantly more hardware and software development and much higher overhead than either alternative approach to be discussed.

## Interfacing Techniques

Methods for using an APC in a particular configuration are dependent on the application and are dictated by the level of performance required. In program development systems, where the sequence of instructions to be executed by the APC is not known in advance and execution speed is relatively unimportant, the APC can be configured to communicate with the microcomputer in I/O mode as shown within the broken lines in Fig 1. Using this configuration, the microcomputer will handle instruction and data transfers to and from the APC as shown by the typical flowchart of Fig 2. The microcomputer polls the APC ready status until the APC completes execution of an instruction and becomes ready to accept the next instruction; then it removes the result of the previous operation and supplies the next instruction with operands. Alternately, APC ready status can be connected to interrupt microcomputer execution, freeing the microcomputer to perform parallel tasks during APC operation. Either approach results in a simple, low cost hardware system that, however, incurs considerable overhead while routing instructions and data to and from the APC.

Known sequences of operations characterize dedicated systems that usually execute programs stored in read only memory (ROM). The I/O mode of APC connection, with its obvious advantages of simplicity and low cost, will suffice for dedicated systems if functions to be performed by the system as a whole are primarily sequential in nature. For example, in an automated x-ray diffraction application, peak search and processing involve crystal positioning using a high speed stepper motor, data acquisition, partial processing of data, and selective data retention. The system repeats this sequence of operations continuously until a peak has been fully identified, then it operates on the retained data in a more or less offline fashion. Because system functions are sequential for the most part, and little opportunity for parallel execution exists, the I/O mode of APC operation can be used with good results.

A more complex, alternative interfacing technique attaches the APC to the microcomputer in a multiprocessor or master-slave configuration shown outside the broken lines in Fig 1. This approach requires a separate sequencer/controller to transfer instructions and data between the microcomputer and the APC, along with bus arbitration logic in the microcomputer interface. It is best suited to those dedicated systems that do not perform wholly sequential operations, systems in which a definite potential for concurrent parallel execution exists. For example, in a laboratory instrument data acquisition and control system, overlapping computation of the next position setting with concurrent acquisition of data from the current position might improve system performance. Here, the APC computes the next position and processes the data read at the current position while the microcomputer drives the positioning mechanism and handles the actual data acquisition functions. Virtually any numeric control system can benefit from this division of labor into a position computation task and a parallel position control task, with data processing computation allocated among the parallel processors. Simplicity and low cost are sacrificed to achieve enhanced system performance.

In multiprocessor mode, the microcomputer must transfer data into APC subsystem local memory, initialize a program resident in APC local ROM (by writing the starting address to a prescribed location and activating the APC run mode), and then begin concurrent execution of the parallel task. As in I/O mode, APC program termination can be signaled by a microcomputer interrupt or by means of the APC ready status flag. Multiprocessor mode affords ample opportunity for the APC to participate in data acquisition and processing functions normally performed only by the microcomputer; however, this capability assumes that the APC has built-in features required by the application.

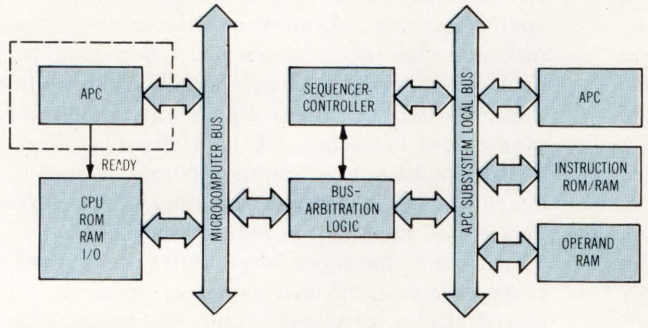



Fig 1 Basic APC interface block diagram. Microcomputer transfers instructions and data to APC in I/O mode (broken lines). External sequencer/controller performs function in multiprocessor mode, using bus arbitration logic to transfer microcomputer bus data to APC local bus. Simplicity of I/O mode interface constrasts with high performance offered by multiprocessor mode potential for concurrent, parallel execution in master-slave environment

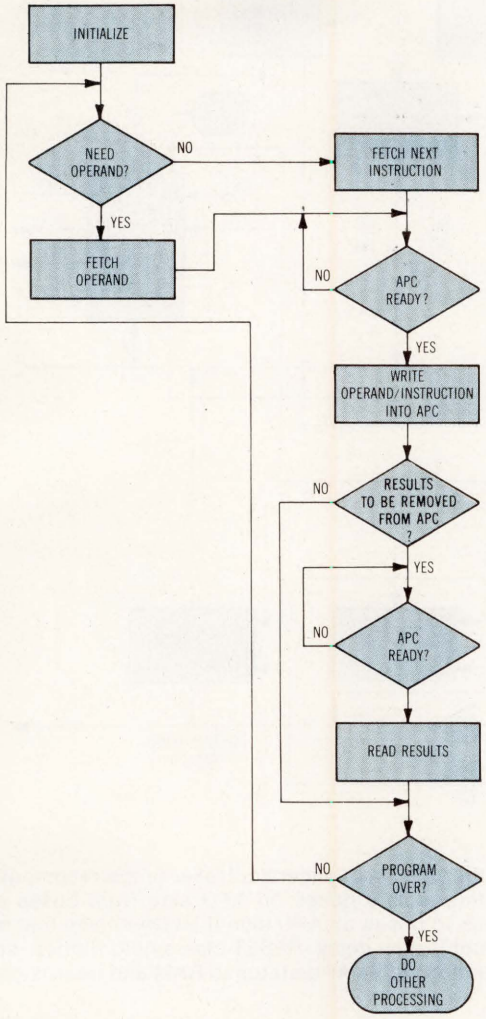



Fig 2 APC access in I/O mode. Microcomputer transfers instructions and data directly to arithmetic processor, in I/O mode, then retrieves results and status once operation has been performed. More complex multiprocessor mode of operation frees microprocessor from polling arithmetic processor status during two wait loops shown

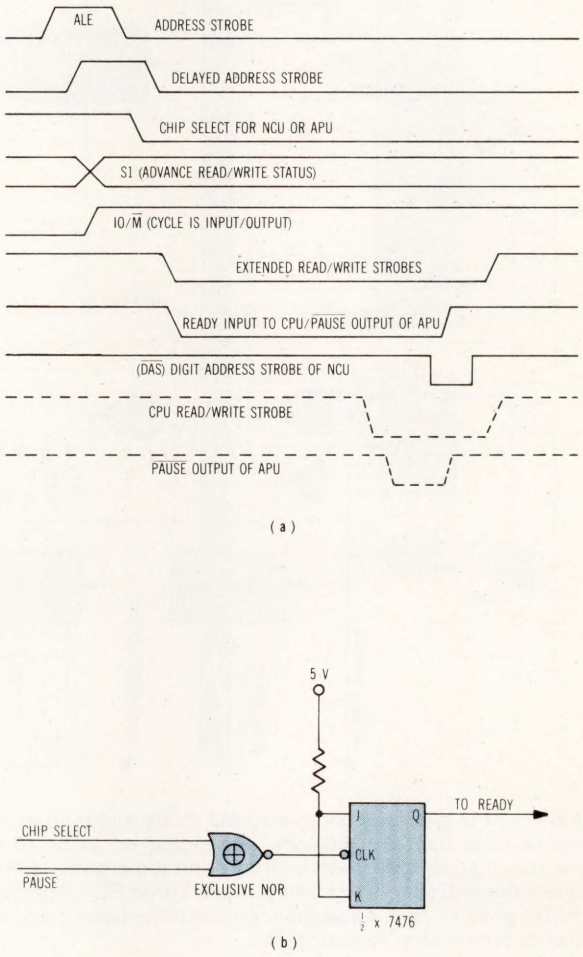



Fig 3 Timing diagram. In (a), both APU and NCU must generate ready input to microprocessor shortly after address strobe is issued. For NCU, digit address strobe (DAS) clears ready so processor can complete its cycle. If APU uses extended read/write strobes, PAUSE can serve as ready input; otherwise, in (b), Q output of J-K flipflop in toggling mode goes low at chip select falling edge and high on rising edge of PAUSE

## Architectural Differences

APCs under consideration have markedly different architectures. Accordingly, specific interface hardware varies with chip characteristics, and software must be designed with attention both to the differing data formats and to the selected mode of data transfer between the external hardware and the APC. One candidate, National Semiconductor's number crunching unit (NCU) chip, is a bit parallel, digit serial device that operates on signed, binary coded decimal (BCD) numbers in either fixed or floating point format. Its instruction set includes I/O and conditional branch operations and, because it is capable of sequencing through a series of stored program instructions, it can be used in standalone systems. On the other hand, the MM57109 pin

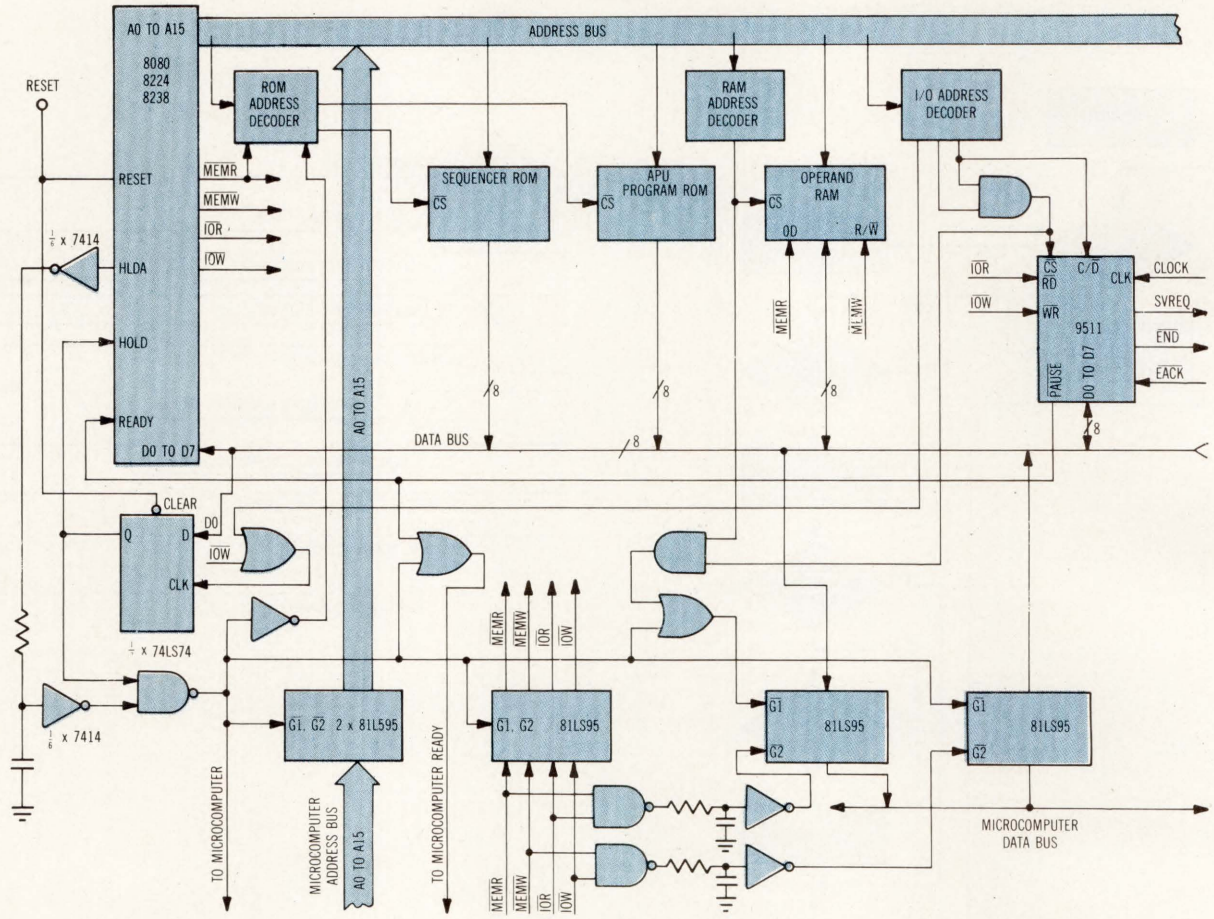



Fig 4 APU interface combining I/O mode and multiprocessor mode. Either APU sequencer/controller or microcomputer can access operand memory, depending on value of HLDA. Five buffers isolate buses on APU side from buses on microcomputer side. Simple arbitration logic gives microcomputer access to buses on APU side if HLDA shows that sequencer/controller is not using them. Three RC combinations add synchronization delay. RESET clears hold flipflop, and HLDA goes to zero, as sequencer/controller begins execution. Halt instruction writes APU status to RAM and returns control of buses to microprocessor

functions are not at all compatible with microcomputer bus signals, requiring extra hardware for the microcomputer interface, even apart from the circuitry for MOS-TTL and TTL-MOS signal level conversion.

Another related pair of contenders, Advanced Micro Devices's Am9511 and Am9512, are byte oriented devices with microcomputer bus compatible pin functions. Both operate on binary data: Am9512 allows 64-bit arithmetic operations for use in high precision applications but offers only the add, subtract, multiply, and divide functions; Am9511 arithmetic processing unit (APU, a particular type of APC) uses 16-bit fixed point numbers and 32-bit numbers in either fixed or floating point format, and performs 2's complement arithmetic operations. It connects directly to existing microcomputers, appearing to the microcomputer as two I/O ports. An 8-bit bidirectional bus handles data transfer to and from the APU, which can attach directly to the microcomputer data bus with the write pulse controlling operand and instruction input and the read pulse controlling output of both results and APU status. One bit determines whether I/O transfer of commands and data or transfer of results and status will occur.

For the APU, a low output at $\overline{\text{END}}$ signals completion of instruction execution, which can be acknowledged by an $\overline{\text{EACK}}$ input. A low at chip select ($\overline{\text{CS}}$) provides access to the APU. The APU returns multipurpose output $\overline{\text{PAUSE}}$ in response to an external demand for APU access; any attempt to read from or write into the APU while it is busy or while the APU conditions its internal circuits to an external request drives $\overline{\text{PAUSE}}$ low. As information transfer is not allowed while $\overline{\text{PAUSE}}$ is low, it must be deferred until the rising edge of $\overline{\text{PAUSE}}$. Instruction execution times range from 8 $\mu$s for a 16-bit fixed point and to about 6 ms for exponentiation using a 2-MHz clock.

## APU Interface Details

Most microcomputers have a ready status line used to synchronize slow memory and I/O devices. $\overline{\text{PAUSE}}$ can be connected to this input; however, a particular problem with connecting $\overline{\text{PAUSE}}$ to the microcomputer ready input arises because READY is generated only after the microcomputer read/write input goes low, whereas processors such as the 8080 or 8085 sample the ready input before issuing read/write strobes [Fig 3(a)]. One solution generates extended read/write strobes, as shown at address latch enable (ALE) time in Fig 3(a), from the status bits supplied by the processor at the beginning of the cycle, allowing the APU to generate $\overline{\text{PAUSE}}$ earlier for the microcomputer to sample earlier. Another approach generates the microcomputer ready input at $\overline{\text{CS}}$ time and clears READY on the rising edge of $\overline{\text{PAUSE}}$. As shown in Fig 3(b), this is achieved easily by using a ½ x 7476 flipflop in toggling mode and supplying as its clock input the "exclusive NOR" of PAUSE with $\overline{\text{CS}}$.

A 16-byte, last in, first out (LIFO) stack within the APU is available for storage of operands and results. The LIFO holds eight 16-bit values or four 32-bit values. An 8-bit, nonprogrammable status register can be accessed at any time, whether the APU is busy or idle; its most significant bit indicates whether or not the APU is busy. When the APU is idle, the remaining seven status bits flag a variety of error conditions. All of the 8-bit APU instructions use seven bits to

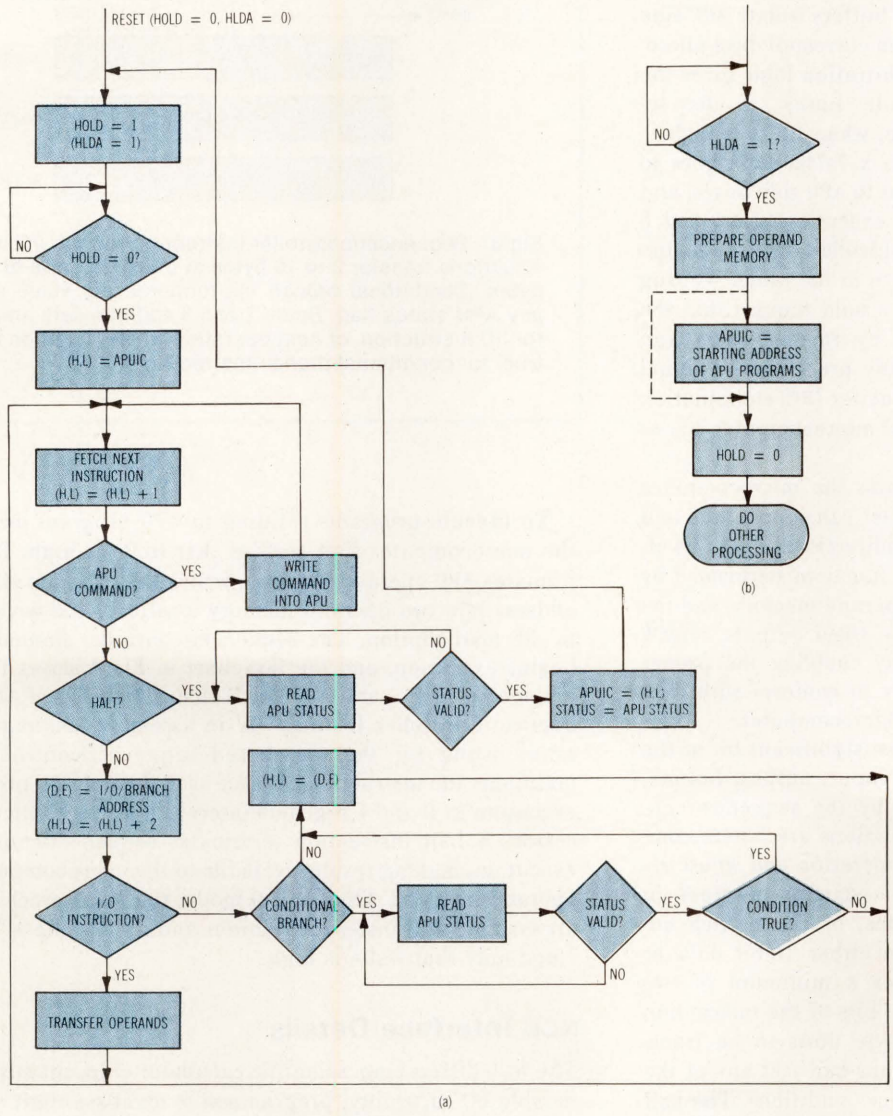



Fig 5 APU sequencer/controller operation. In (a), microprocessor based sequencer/controller determines whether it or APU must execute each instruction. It implements I/O and conditional branch capabilities not available in APU instruction set, and also maintains APU instruction counter in H and L registers internal to 8080 microprocessor. In (b), microcomputer prepares operand memory and program starting address, if required, before pulling HOLD low

determine the operation and data format, returning the eighth bit on the service request line (SVREQ) output upon completion of the operation. Use of SVREQ is optional; hence, the most significant bit of an APU instruction can be used to determine whether an instruction should be routed to the APU or executed directly by the sequencer/controller. This allows the sequencer/controller to implement I/O and branch instructions when using the APU in stored program execution mode.

An APU combined interface allowing both I/O mode operation and the master-slave mode of operation in a multiprocessor configuration, depending on the level of the hold acknowledge (HLDA) line, is shown in Fig 4. The sequencer/controller is based on the 8080 microprocessor with associated 8224 clock generator, 8238 system controller, and program ROM. The 8228 system controller cannot be used because it does not generate the extended write strobes required for $\overline{\text{PAUSE}}$ to serve as a READY input to the 8080. Although separate read and write strobes for memory and I/O devices appear, these may be shared if memory mapped I/O is used. Five 81LS95S 3-state octal buffers isolate APU side address, data, and control buses from corresponding microcomputer side buses. Simple bus arbitration logic gives the microcomputer access to APU side buses, if the sequencer/controller is not using them, when HLDA is high.

RESET clears the hold flipflop (½ x 7474); HLDA goes to zero, disabling microcomputer access to APU side buses; and the sequencer/controller enters its execution state. Fig 5 gives details of the sequencer/controller operation implemented by the 8080 program shown in the table. Writing a 1 into the hold flipflop generates a hold request that the sequencer/controller acknowledges by raising HLDA and floating its buses. Since HLDA slightly precedes the actual floating of 8080 buses, a resistor-capacitor (RC) combination at the HLDA output delays enabling of microcomputer access to the APU and operand memory.

HLDA high also enables $\overline{\text{PAUSE}}$ onto the microcomputer READY input so that the microcomputer can supply data and request instruction execution. The bidirectional data bus offers additional control for read/write functions performed by the microcomputer on the APU, the operand memory, and the hold flipflop. RC combinations at the ORed outputs, $\overline{\text{MEMW}}$ with $\overline{\text{IOW}}$ and $\overline{\text{MEMR}}$ with $\overline{\text{IOR}}$, delay enabling the proper direction of information flow slightly to conform with data hold times for the memory and the microcomputer.

SVREQ is not used, leaving the most significant bit of the command word available to define input, output, branch, and halt instructions implemented by the sequencer/controller (Fig 6). I/O and branch instructions are 3-byte commands whose first byte defines the operation and whose remaining bytes determine the data starting address in operand memory, for I/O instructions, or the branch address. Because the APU operates on either 16-bit data or 32-bit data, I/O instructions transfer a minimum of two bytes, and the least significant three bits of the instruction code determine the number of 2-byte units to be transferred. Conditional branch instructions can test any of the APU status bits and distinguish various conditions. The halt instruction transfers APU status into prescribed memory locations before returning control of the buses to the microcomputer. This allows the microcomputer to make decisions on the basis of APU status.

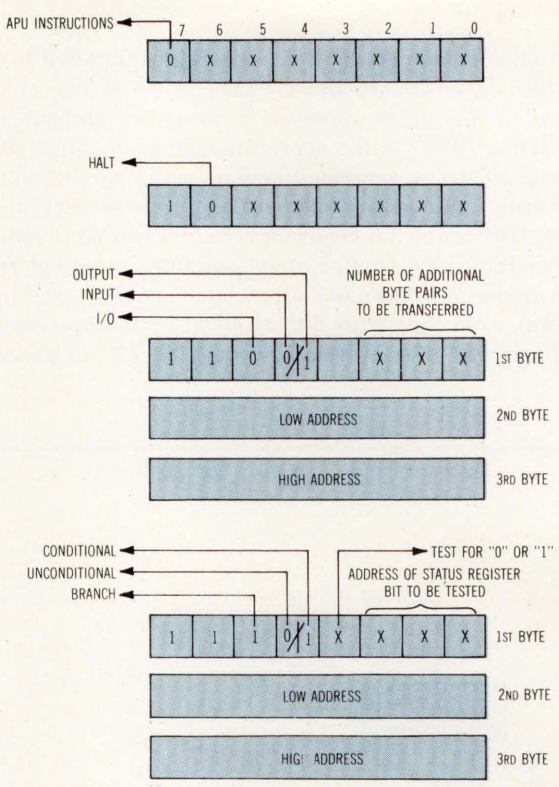



Fig 6 Sequencer/controller instruction format. I/O instructions transfer 2 to 16 bytes at a time in units of 2 bytes. Conditional branch instructions test value of any APU status flag. Bytes 2 and 3 address data area, for I/O instruction, or next operation when condition is true, for conditional branch instructions

To execute programs residing in APU program memory, the microcomputer first verifies that HLDA is high. It then prepares APU operand memory, writes the program starting address into two operand memory locations, and writes a 0 to the hold flipflop. The sequencer/controller immediately begins execution, and the flowchart in Fig 4 shows the remainder of the operation. The Table "8080 Based APU Sequencer/Controller Listing," is an assembly language program listing for the 8080 based sequencer/controller. It maintains the instruction counter used during APU program execution in H and L registers internal to the 8080 microprocessor. A halt instruction terminates sequencer/controller execution, making results available to the microcomputer in operand memory. Thus, in I/O mode, the microprocessor is always able to transfer instructions and data to the APU provided only that HLDA is high.

## NCU Interface Details

The NCU differs from scientific calculator chips mainly in its flexible I/O capability, programmable mantissa digit count, user programmable flags (F1 and F2) for driving external circuits, error flag, and simple handshaking arrangement implemented by RDY and HOLD signals for entry of operands or instructions and for instruction execution. Operands can

## 8080 Based APU sequencer/controller Listing

```
START:  MVI   01
        OUT   HOLD      HOLD = 1     HLDA = 1
        NOP             Wait for HOLD to go low
        LHLD  APUIC     Read APUIC into H and L registers, (L) = (IC), (H) = (IC + 1)
NEXINS: MOV   A,M       (A) = instruction
        MOV   B,A       (B) = instruction
        INX   H         Increment APUIC
        RLC   CY        CY (CARRY) = 7th bit of instruction
        JC    BRIOH     BRANCH, I/O, or HALT
APUINS: MOV   A,B       (A) = instructions
        OUT   INST      Instructions to APU
        JMP   NEXINS    Go to fetch next instruction
BRIOH:  RLC             CY = 6th bit of instruction
        JC    BRIO      BRANCH or I/O instruction?
HALT:   SHLD  IC        Store APUIC
GETST1: IN    INST      (A) = APU status register
        ANA   A
        JM    GETST1    APU status Valid?
        STA   STATUS    Store APU status at STATUS
        JMP   START
BRIO:   MOV   E,M       (E) = 2nd byte of instruction
        INX   H         Increment APUIC
        MOV   D,M       (D) = 3rd byte of instruction
        INX   H         Increment APUIC
        RLC             CY = 5th bit of instruction
        JC    BRANCH    Is it BRANCH?
IO:     MOV   C,A
        MOV   A,B
        ANI   07        (A) = Number of additional byte pairs to be transferred
        INR   A
        RLC
        MOV   B,A       (B) = Number of bytes to be transferred
        MOV   A,C
        RLC             CY = 4th bit of instruction
        JC    OUTPUT    OUTPUT
INPUT:  LDAX  D         (A) = Next byte of data
        OUT   DATA      Data to APU top of stack
        INX   D         Increment data address
        DCR   B
        JNZ   INPUT     Data transfer over?
        JMP   NEXINS    Go to fetch next instruction
OUTPUT: IN    DATA      (A) = APU top of stack
        STAX  D         Store Data
        INX   D         Increment data address
        DCR   B
        JNZ   OUTPUT    Data transfer over?
        JMP   NEXINS    Go to fetch next instruction
BRANCH: RLC             CY = 4th bit of instruction
        JC    CONDIT    Is it conditional?
EXCHAN: XCHG            (H,L) (D,E)
        JMP   NEXINS    Go to fetch next instruction
CONDIT: MOV   A,B       (A) = instruction 1st byte
        ANI   08
        JZ    TZERO     Test will be conducted for 0 or 1
        MVI   FF
TZERO:  MOV   C,A       (C) = Test status
        MOV   A,B       (A) = Instruction
        ANI   07        (A) = Address of status register bit
        MOV   B,A       (B) = Address of status register bit
        INR   B
        MVI   80        B register's bit corresponding to the status register bit to be tested
LSHIFT: RLC             = 1, rest all are zeros
        DCR   B
        JNZ   LSHIFT
        MOV   B,A
GETST:  IN    INST      (A) = APU status register
        ANA   A
        JM    GETST     APU status Valid?
        ANA   B         Separate the bit to be tested
        JZ    BZERO
        MVI   FF
BZERO:  XRA   C
        JZ    EXCHAN    Jump condition satisfied?
        JMP   NEXINS    If not, go to fetch next instruction
```

be entered by means of a sequence of instructions, as for a calculator chip, or by means of a sequence of BCD digits using the multidigit input instruction. A multiplexing signal, instruction select (ISEL), allows entry of either 6-bit instructions or 4-bit BCD data via pins I1 through I6 on the chip.

Four registers (X, Y, Z, and T) hold operands and temporary results; a memory register (M) can hold constants, or temporary results that might serve as loop counters directing program branches. Data always enter the X register, and the multidigit output instruction always supplies the X register content, digit by digit, at pins DO1 to DO4, accompanied by corresponding digit addresses at DA1 to DA4 and a write pulse. The 12-digit internal registers hold two digits of exponent, a digit containing mantissa and exponent sign bits, a digit giving the decimal point position, and up to eight digits of mantissa.

I/O instructions operate in either floating or fixed point format. Either mode sequentially transfers the sign digit, the decimal point position digit, and the requested number of mantissa digits. Fixed point transfers also supply the two exponent digits; the exponent sign is available in the sign digit. A reset establishes floating point operation with an 8-digit mantissa by default. A "toggle mode" instruction selects alternative modes of operation. I/O and branch instructions are 2-byte commands whose second byte is used externally as the eight high order bits of the data memory address, in the case of I/O instructions, or as the high order branch address for branch instructions.

The ready line (RDY) goes high to indicate that the NCU is ready to accept instructions, and low to read and execute an instruction if HOLD is low. Instruction time is lengthened, when necessary, to wait for HOLD to go low. I/O instructions

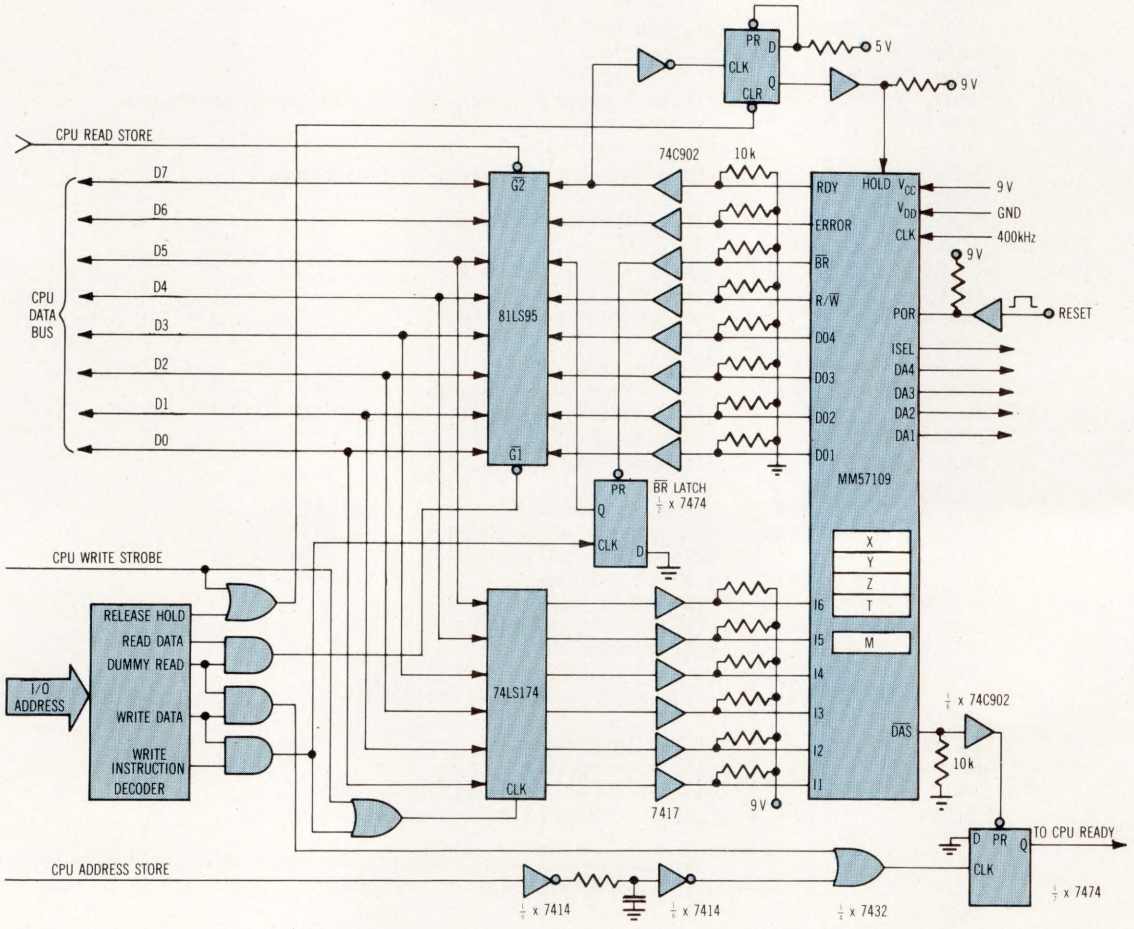



Fig 7 NCU interface in I/O mode. Two buffers achieve MOS-TTL compatibility. Instructions and data are latched, and 3-state octal buffers read output from DO1 to DO4. After latching an instruction, microcomputer releases HOLD to rise on the falling edge of RDY. Since data I/O occurs after $\overline{DAS}$ pulse, ready is generated at address strobe time and cleared by $\overline{DAS}$. Dummy read senses $\overline{DAS}$, and data are valid 15 $\mu$s later

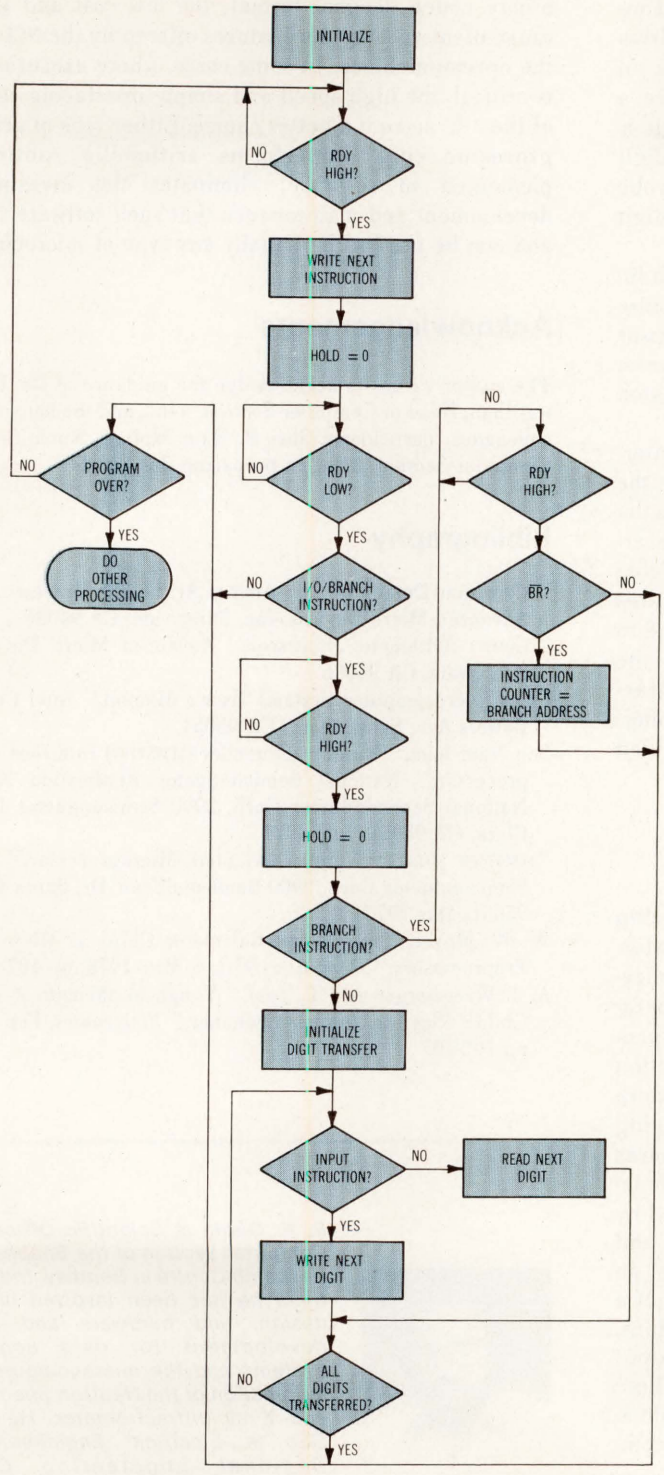



Fig 8 Data transfer between microprocessor and NCU. Multiprocessor mode interface for NCU requires modified sequencer/controller program that implements this series of operations, along with Fig 7 hardware in place of APU in Fig 4. I/O and branch instructions need not be implemented by NCU sequencer/controller, as was required for APU, because they appear in NCU instruction set

have the particular disadvantage that sequential transfer of digits occurs at a set, uncontrolled rate.

The NCU connected to a microcomputer in single instruction execution mode is shown in Fig 7. Data and instructions flow between the NCU and the microcomputer as shown in Fig 8. Since the NCU supply voltage differential is 7.9 to 9.5 V, a 9-V supply is used. The 7417 buffers convert TTL inputs to the 9-V level, and 74C902 buffers convert all MOS outputs from the NCU to TTL signal level. Outputs DO1 to DO4, ERROR, and RDY are connected to the microcomputer data bus by an 81LS95 octal, 3-state buffer. When RDY is high, the microcomputer writes an instruction into the 74LS174 6-bit latch by way of the data bus and pulls HOLD low to request NCU instruction execution.

For I/O instructions, the microprocessor prepares to accept serial digits in the current number format. Input instructions latch digit data into the 74LS174 at digit address strobe ($\overline{DAS}$) time. Output instructions leave digit data on pins DO1 to DO4 about 15 $\mu$s after $\overline{DAS}$ appears. In practice, a dummy read serves to sense $\overline{DAS}$, and the actual digit is available after a slight delay. As shown in Fig 3, the digit write or dummy read address ORed with CPU Address Strobe raises microprocessor HOLD, thereby lengthening the digit write or dummy read cycle until $\overline{DAS}$ appears.

When the condition specified in a conditional branch instruction exists and a branch must be made, the $\overline{BR}$ pulse issued by the NCU sets a branch latch. The microprocessor reads the branch latch when RDY goes high and performs a branch when this latch is found to be set. The branch latch is cleared at instruction latching time.

In multiprocessor or master-slave mode, the NCU interface can be implemented in much the same way as for the APU described earlier. Hardware shown in Fig 7 replaces the APU shown in Fig 4, in this instance, while the sequencer/controller assembly language program from the Table "8080 Based APU Sequencer/Controller Listing," requires suitable modification to implement the flowchart of Fig 8 to direct the flow of operands and instructions between the NCU and external hardware. I/O, branch, and halt instructions need not be implemented by the sequencer/controller, for a master-slave NCU interface, because they are provided in the NCU instruction set.

## Summary

Calculator chips, number crunching units, and single-chip arithmetic processing units enhance microcomputer performance in scientific and engineering applications by relieving the microcomputer of the burden of arithmetic operations. Both the calculator chips and the NCU are inexpensive, low power devices offering relatively slow instruction execution speed. However, apart from the need to achieve MOS and TTL signal level compatibility, interfacing calculator chips as microcomputer peripherals involves simulation of keyboard (input) and display (output) functions in hardware and software. The disadvantage posed by entering operands as a sequence of mixed instructions and data is reflected in further software overhead. The NCU, on the other hand, incorporates some of the best features of a general purpose microcomputer such as I/O instructions, conditional branch instructions, programmable output flags, and the ability to sense external conditions. These allow straightforward use of this component in standalone systems or in a multiprocessor configuration as a microcomputer extension.

An arithmetic processing unit chip is tailor-made for use as a microcomputer peripheral as it offers nearly 200 times the speed of the NCU. But, it does so at nearly twenty times the cost. The APU, on the other hand, performs only arithmetic functions and lacks I/O or decision making capabilities, thus requiring an external sequencer/controller for use in a multiprocessor configuration.

In view of the available alternatives, use of calculator chips as microcomputer extensions is of academic interest or, at best, should be confined to applications that require very sophisticated mathematical or statistical function capability. For most applications, particularly those that use binary coded decimal format, the low cost and the wide range of microcomputer features offered by the NCU make it the optimum choice. In some cases, where execution speed is critical, the high speed and simple interfacing capability of the APU make it a better choice. Either type of arithmetic processor chip outperforms arithmetic routines implemented in software, eliminates the investment in development and maintenance that such software requires, and can be used with virtually any type of microcomputer.

## Acknowledgements

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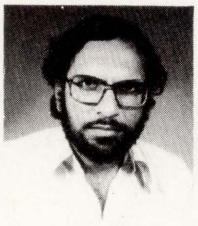

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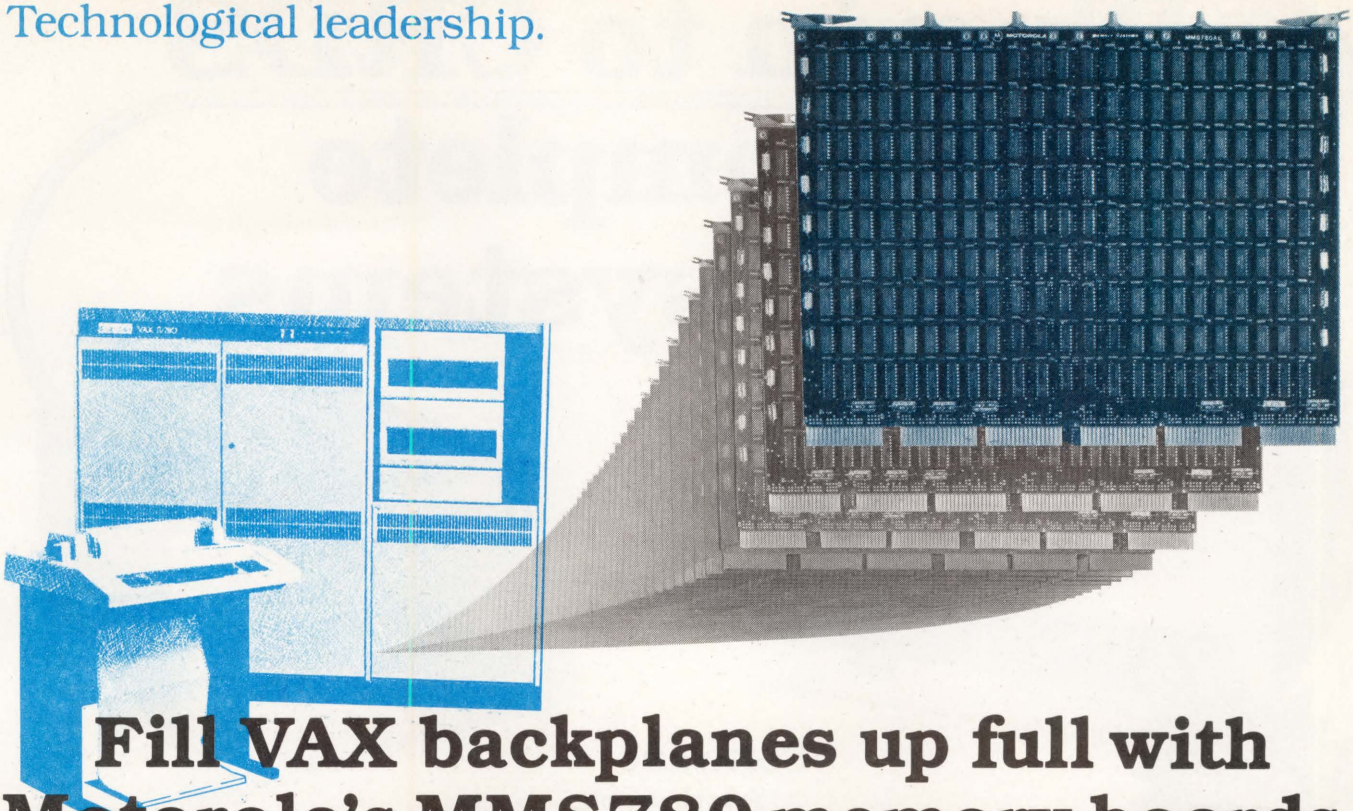

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# DATA DRIVEN SYSTEM FOR HIGH SPEED PARALLEL COMPUTING— PART 2: HARDWARE DESIGN

Prototype design for a data driven computer uses highly parallel hardware to speed up computation and implements a 2-dimensional flowgraph model of computing that departs markedly from traditional approaches to realize increased parallel activity in software

**John Gurd and Ian Watson**

University of Manchester
Manchester, England

A prototype data driven parallel computer being built at the University of Manchester, Manchester, England, implements a comprehensive model of computing based on data flowgraphs. Using the model created in Part 1, Part 2 determines the requirements for a system to execute the labeled flowgraph model. These lead to a circular pipelined architecture in which packages of information representing tokens, arcs, and nodes can circulate.

Investigation of parallelism in hardware as a means of speeding up computations discussed in Part 1 identified the pipeline and the parallel array as two basic hardware structures. A key factor in using such hardware is the ability to express parallel activity in software. Since conventional programming languages, based on the classical von Neumann concepts of sequential memory access using a program counter, are not suited to expressing parallel activity, a data driven model of computing was developed to clarify the dependency relations between data and to expose the potential for parallel activity in 2-dimensional flowgraphs. Computers based on this computational model have proven to be highly concurrent, but quite different in structure from traditional computers.

Studying one particular data driven computer* that implements the model previously developed, Part 2 details the design of individual pipeline stages and estimates system performance. Future developments in high level software and very high performance systems are also considered.

It is apparent from the rules for executing flowgraphs that a data driven computer must be capable of performing the following activities: transferring a token from the tail to the head of the arc on which it lies; grouping together tokens of the same color lying at the heads of arcs that point to a common node, and arranging for the node to fire when all of its inputs are available; and executing operations on input data, erasing the input tokens, and producing output tokens at the tails of the appropriate arcs. These actions must be performed continuously until no tokens remain in the graph. Furthermore, to present data as input and to receive results from the computation, there must be a means of inserting tokens into the system and extracting them from the system.

## Data Driven Architecture

The structure in Fig 1 reflects these needs. It comprises five units connected together in a ring. The major traffic around

*The system described is a small prototype machine based on an outline design proposed at Manchester, England, in 1978.[1] It is currently being constructed by the authors with funding from the Distributed Computing Systems Programme of the Science Research Council of Great Britain[2] and is expected to be operational in mid-1981.

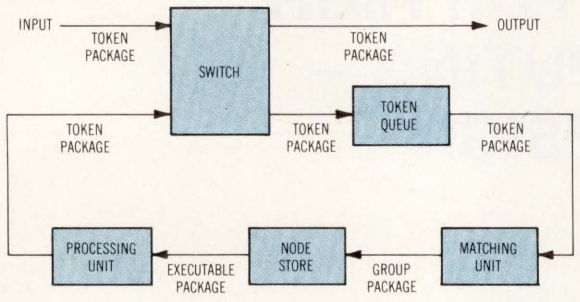



Fig 1 Data driven computer structure. Five major functional blocks communicate in clockwise direction around ring. Token package is main unit of information comprised of data value, label, and destination node pointer. Matching unit groups tokens. When sufficient tokens arrive to fire node, appropriate group package finds destination node description in node store. Executable package containing operator, all operands, label, and pointer(s) to further destination node(s) is sent to processing unit for execution. Switch handles external I/O. Token queue saves excess tokens

the ring is in token packages representing the machine equivalent of labeled tokens lying on flowgraph arcs. Token packages are either sent to the ring as external input or else formed during a computation at the output of the processing unit. They pass around the ring in a clockwise direction, first encountering the switch, which serves to merge the two sources of tokens and to direct output from the system, and then the token queue, which holds the large numbers of tokens that highly parallel programs can generate. The third unit, called the matching unit, groups together tokens with the same label traveling to the same node.

When sufficient matching tokens are present, the node can be fired and all tokens can be sent to the next unit in a group package. Otherwise, each incoming token must be placed in the matching store to await the arrival of further corresponding tokens. Fired groups of tokens find the operation to be performed on them in the node store. For convenience, they are also given the addresses of the nodes to which output should be sent when execution is completed. The node store thus constructs complete executable packages consisting of an operator, operands, common label, and one or more destinations for the resultant values. These packages are sent to the processing unit where the required operation is executed, eventually producing new tokens that start a repeat journey around the ring.

## Notational Influences

It is important to reiterate the influence of the labeled flowgraph notation in formulating this structure. Each token carries not only its value, but also a label and a destination, including the place of entry to the node (eg, the left- or right-hand side of an addition operator). This requires each word of token queue memory and matching memory to be much longer than a conventional memory word containing only a data value.

Moreover, the matching operation requires an associative memory for saving unmatchable input tokens. The common name used for association is the label and the destination (except for points of entry, which should of course differ). To conform to the required flowgraph behavior, the matching unit must perform two kinds of access to the associative memory after searching for items with the same name as the incoming token. If the search succeeds, and all matching tokens are present, matched token entries are extracted from the associative memory and sent to the node memory. If the search fails, or one or more required tokens are missing, the incoming token is inserted into the associative memory.

Finally, the processing unit instruction set must include data branch, token relabeling, and token delabeling operations, apart from the usual arithmetic functions. The instruction set naturally excludes conventional control branch or jump instructions and memory to memory instructions.

## Parallelism

The ring structure of Fig 1 is a natural candidate for pipeline construction as described in Part 1. Individual units interact only by sending token packages around the ring; hence, the individual switching, queuing, matching, node access, and processing operations implemented by the five functional units can be overlapped and even allowed to overtake one another. The only critical area of the system is the matching unit, where the associative memory must be searched serially. The speed at which tokens can be matched at the associative memory effectively determines the pipeline delay period. Elsewhere, functional units can be pipelined or paralleled as convenient to match this time period. In the prototype system under construction, it has proved necessary to place several processing elements in a parallel array within the processing unit. All other units are composed solely of pipeline stages operating serially at the required rate.

# Logical System Design

Two major features of a pipeline are its delay period and its synchronization type. Use of transistor-transistor logic technology determines the 200-ns delay period chosen for the prototype system. Both the modest technology and relatively slow speed are deliberate since the prototype serves only to test out ideas for data driven computing and is not intended as a very high speed production computer.

The choice between a synchronous or an asynchronous pipeline involves a compromise. Synchronous systems are attractive in situations where all operations take similar times to complete, and whenever arbitration between competing tasks is needed. However, the problems of distributing a common-phase clock in a physically large synchronous system mean that asynchronous communication is often preferred.

In the compromise design, local clocks are used within each major functional unit of Fig 1, with synchronous internal arbitration, either pipelining or paralleling, as appropriate. An asynchronous, unidirectional communication

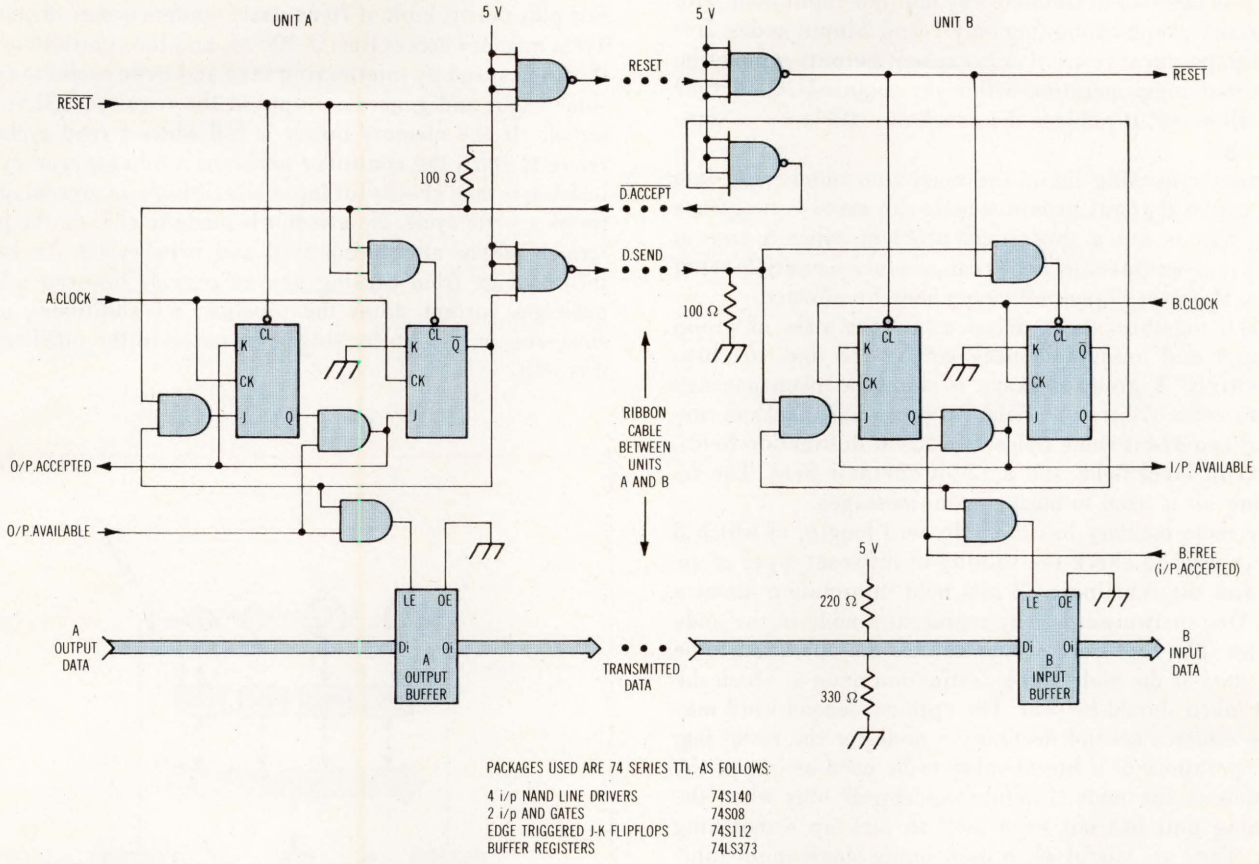



Fig 2 Interunit pipeline communication circuit. Each unit has its own local clock to synchronize internal events. Asynchronous transfer between units is synchronized to appropriate clock at each end by this circuit. Handshake between D.SEND and $\overline{\text{D.ACCEPT}}$ helps transmit data from output buffer of one unit to input buffer of next unit. Circuits are initialized by RESET, which is passed around pipeline from host system

link between each pair of functional units provides buffering and resynchronization at the input and output of each unit. Fig 2 shows logical circuits for controlling the input and output interfaces. An asynchronous handshake arrangement achieves data transfer by using the D.SEND and $\overline{\text{D.ACCEPT}}$ signals. A pair of edge-triggered J-K flipflops synchronizes the handshake to the appropriate clock at each end. While use of two flipflops slows the transfer slightly, it allows resolution of uncertainty when handshake signals change at the same instant as the synchronizing clock. This situation has long been recognized as a major trouble source in systems using asynchronous communication.[3]

Sender and receiver clock signals derive from unrelated 40-MHz sources, except in the matching and processing units, which use 25- and 10-MHz clocks, respectively. Delays through logic at either end of the circuit, together with the need for four delays through the linking cable, imply that communication over distances of up to 10 ft (3 m) is possible within the 200-ns pipeline delay period.

## Data Formats

For various reasons such as board size, connector density, expected costs (especially for memory), and anticipated system usage, token packages were designed to have a basic word length of 96 bits. Because all communication in the system takes place via the pipeline, one bit must be used to distinguish between system messages (eg, load a value into the node memory) and computational messages (eg, an actual token). In the case of token packages, the remaining 95 bits are allocated among a 37-bit value field, a 36-bit label field, and a 22-bit destination field. The method of labeling tokens and controlling data flow through program graphs brings about these unusual field sizes. The largest data value recognized is a 32-bit floating point value, and integers are 24 bits long. It can be seen from these figures that the storage requirements for data driven execution with labeling exceed conventional storage requirements by a factor of three or more.

Pragmatic arguments restrict the maximum number of tokens that can be associated or matched up in the matching unit to two. This is not a severe theoretical limitation, since it is possible to simulate any multiple-input node with a primitive graph containing only 1- and 2-input nodes. It is a useful, practical restriction because it permits completion of the matching operation within the required 200-ns time limit. However, it reduces the execution efficiency of some functions.

Similar reasoning limits the maximum number of data value copies that any primitive node can make to two. Once again, this is not a theoretical problem, since a tree of primitive, 2-output copy nodes can produce a multiple set of copies. However, again, efficiency may be affected.

Taken together, these decisions fix the sizes of group packages and executable packages at 133 and 167 bits, respectively. A group package is simply a token package with an extra 37-bit value field. An executable package consists of two 37-bit value fields, two 22-bit destination fields, one 36-bit label field, and a 12-bit operator field. The remaining bit is used to mark system messages.

The node memory has a 35-bit word length, of which 3 bits are used to check the validity of different types of access, and the remaining 32 bits hold information about a node. One or two words may represent a node in the node memory. The first word always defines the operation to be performed at the node and a destination node to which the result token should be sent. The optional second word may define either a second destination node for the result (eg, copy operation) or a literal value to be used as one of the operands at the node. Literals can appear only when the matching unit has not been used to pick up a matching token. They are useful when performing single-input functions that are of 2-input form but with one input constant (eg, increment value, which is equivalent to adding the value to a constant).

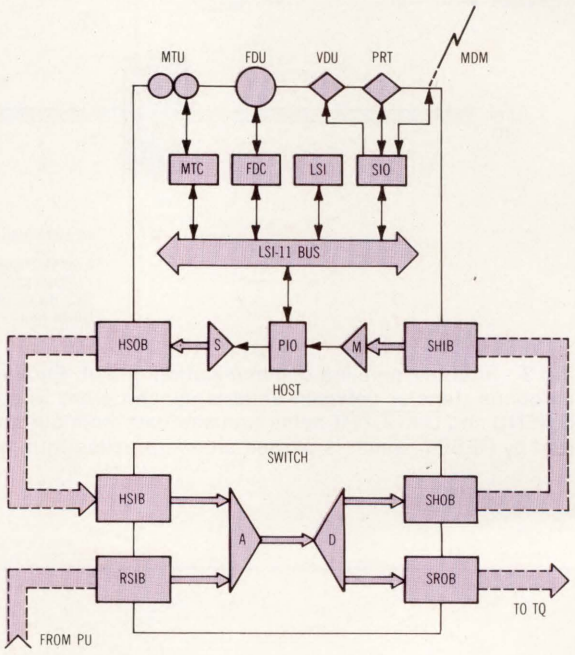
## Input/Output and Host System

The prototype system is capable only of data driven computation. Because it cannot control peripheral devices directly, a conventional host system handles file storage and input/output (I/O). Two asynchronous interface links attach the host to the data driven ring (Fig 3). The host machine is a DEC LSI-11 with a range of standard peripheral devices, including a telephone link to external mainframes. Although it is not the ideal system for its position because of its relatively small word length and slow speed, it is adequate as long as I/O traffic remains light. The LSI-11 drives the data driven ring through a 16-bit parallel interface and a 16- to 96-bit word expander. It receives output from the ring via the 96- to 16-bit word compressor and the same parallel interface.

An unusual pipeline unit, the switch must arbitrate between two separate sources of input: the host system and the processing unit. The synchronized nature of the two input buffers simplifies this task. Whenever two packages arrive simultaneously, the switch gives priority to the package coming from the processing unit. To avoid unreasonable delays in processing unit output, the switch operates within a 100-ns period. Output packages are recognized at the switch input and routed to the host exit output buffer. All other packages are sent to the ring output buffer.

## Token Queue

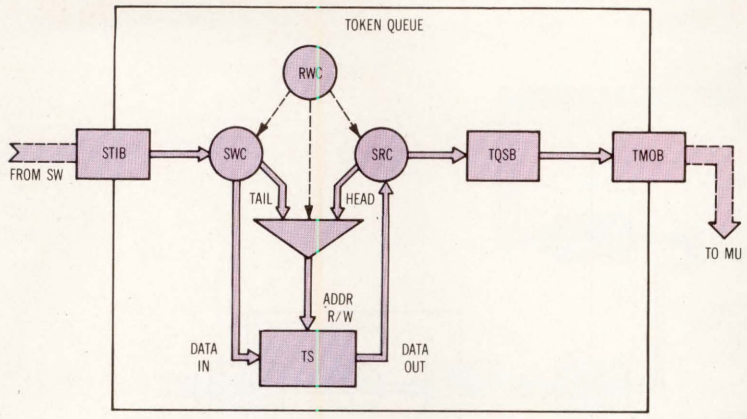
Implemented as a first in, first out circular buffer for token packages, token queue (Fig 4) memory is 16k words by 96 bits plus parity, built of 70-ns static random access memory. Total memory access time is 100 ns, and the controller uses this high speed by interleaving read and write cycles to consume input and generate output at the required 200-ns intervals. If the memory buffer is full when a read cycle is ready to start, the controller performs a dummy read cycle instead; it then checks for input and, if input is present, performs a write cycle. No attempt is made to change the pattern of 100-ns alternating read and write cycles. To keep this strategy from causing uneven periods between token packages further down the pipeline, an additional, synchronous, output buffer stage is inserted in the pipeline in this unit.




DOUBLE DOTTED LINES REPRESENT ASYNCHRONOUS COMMUNICATIONS LINKS

| | |
|---|---|
| MTU = MAGNETIC TAPE UNIT | S = 16-BIT TO 96-BIT DEMULTIPLEXER |
| MTC = MAGNETIC TAPE CONTROLLER | A = 2-WAY SYNCHRONOUS ARBITRATOR |
| FDU = FLOPPY DISC UNIT | D = 2-WAY DISTRIBUTOR |
| FDC = FLOPPY DISC CONTROLLER | SHIB = SWITCH TO HOST INPUT BUFFER |
| VDU = CONTROL TERMINAL | HSOB = HOST TO SWITCH OUTPUT BUFFER |
| PRT = 30-CHAR/s DECWRITER | HSIB = HOST TO SWITCH INPUT BUFFER |
| MDM = 300-BAUD MODEM | RSIB = RING TO SWITCH INPUT BUFFER |
| SIO = 4-CHANNEL SERIAL INTERFACE | SROB = SWITCH TO RING OUTPUT BUFFER |
| LSI = LSI-11/2 + 28-k WORD MEMORY | SRHB = SWITCH TO HOST OUTPUT BUFFER |
| PIO = 16-BIT PARALLEL INTERFACE | PU = PROCESSING UNIT |
| M = 96-BIT to 16-BIT MULTIPLEXER | TQ = TOKEN QUEUE |

Fig 3 Host system interface. LSI-11 frontend computer drives ring via switch module. Multiplexer and demultiplexer convert between 16-bit host word and 96-bit token package lengths. Host then mimics any other pipeline unit with asynchronous I/O communication links. Switch arbitrates between competing inputs internally and synchronously, avoiding the problem of asynchronous arbitration




DOUBLE DOTTED LINES REPRESENT ASYNCHRONOUS COMMUNICATIONS LINKS

SINGLE DOTTED LINES REPRESENT CONTROL SIGNALS

TS = 16k x 96-BIT WORD TOKEN STORE
A = ADDRESS ARBITRATOR
RWC = ALTERNATING READ-WRITE CONTROLLER
SWC = STORE WRITE CONTROLLER
SRC = STORE READ CONTROLLER
STIB = SWITCH TO TOKEN QUEUE SMOOTHING BUFFER
TQSB = TOKEN QUEUE SMOOTHING BUFFER
TMOB = TOKEN QUEUE TO MATCHING UNIT OUTPUT BUFFER
SW = SWITCH
MU = MATCHING UNIT

Fig 4 Token queue. Highly parallel programs may generate large numbers of tokens, many of which must be held temporarily. Basis of unit is 16k-word circular queue with 100-ns access time. Alternate attempts to read and write the store are made at head and tail of queue, respectively. Empty store, or absence of input, postpones read or write cycle for 200 ns. Extra synchronous buffer stage smooths irregular output

## Matching Unit

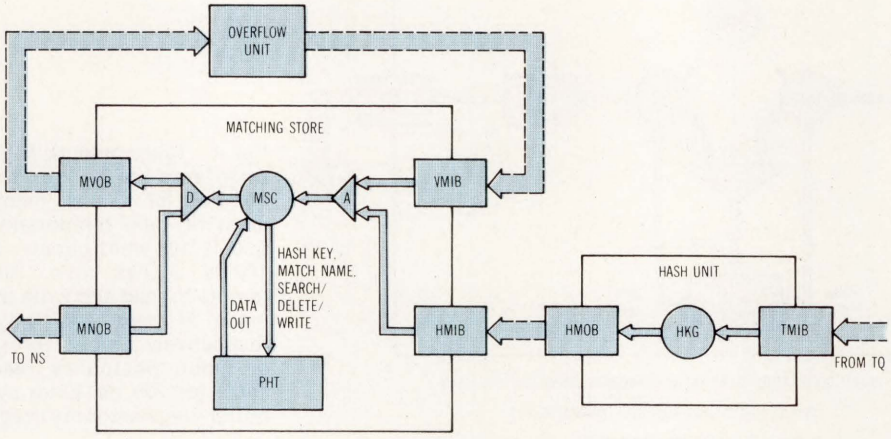
Token matching unit operation is the most critical part of the system. The matching store is relatively large (16k token packages plus parity) and must be accessed associatively on 54 bits of the label and destination fields. Present costs preclude using a true content-addressable memory of this size; therefore, a hardware hashing technique simulates the associative memory by implementing a parallel hashing scheme that searches several hash tables for a matching entry simultaneously, as shown in Fig 5.[4, 5, 6]

A separate pipeline stage precedes the main section of the matching unit. Here, an 11-bit hash key is generated from the label and destination fields of the incoming token package. The token package and the hash key are transferred to the matching memory's input buffer. At this point, examining a bit of the destination field determines whether matching is appropriate for this token package. Single tokens, for which matching is not appropriate, pass directly to the output buffer.

A hash table search locates the partner for other tokens. In this case, the hash key is used as an address to read the eight banks of the hash table in parallel. The label and destination fields of all eight accessed locations are compared with the corresponding sections of the input token package. Successful matches then cause the matching entry to be deleted from the hash table, and the matched token pair, together with its label and destination, is forwarded to the output buffer.

Unsuccessful matches normally cause the incoming token package to be placed at a free position within one of the parallel memory banks still addressed by the hash key. Occasionally, this will not be possible because all words addressed by the key already contain nonmatching token packages. In this last case, the system departs from conventional techniques. Instead of generating a new hash key and starting all over again, the controller routes the unmatched token package to an overflow unit where it can be processed at leisure.[4, 5] One advantage of the data driven notation is that subsequent token packages can be handled out of turn, providing that their hash keys are disjoint, without affecting computation results.

The overflow unit complicates the operation just described. For example, after an unsuccessful match, a token cannot be placed in a free location if an overflow has occurred for its hash key; instead, the nonmatching token package must be referred to the overflow unit. Also, there must be a return path from the overflow unit to the system. This is located at the input to the matching store itself, and provides potential competition for normal ring traffic.




DOUBLE DOTTED LINES REPRESENT ASYNCHRONOUS COMMUNICATIONS LINKS

HKG = HASH KEY GENERATOR
MSC = MATCHING STORE CONTROLLER
PHT = 8 x 2k x 96-BIT WORD PARALLEL HASH TABLE
A = 2-WAY SYNCHRONOUS ARBITRATOR
D = 2-WAY DISTRIBUTOR
TMIB = TOKEN QUEUE TO MATCHING UNIT INPUT BUFFER
HMOB = HASH UNIT TO MATCHING STORE OUTPUT BUFFER
HMIB = HASH UNIT TO MATCHING STORE INPUT BUFFER
VMIB = OVERFLOW TO MATCHING STORE INPUT BUFFER
MVOB = MATCHING STORE TO OVERFLOW OUTPUT BUFFER
MNOB = MATCHING STORE TO NODE STORE OUTPUT BUFFER
TQ = TOKEN QUEUE
NS = NODE STORE

Fig 5 Matching unit. Critical system area contains two pipeline stages and parallel overflow unit. Main matching store consists of parallel hash table. Preceding pipeline stage generates hash key. Access to store may be successful or unsuccessful; successfully matched tokens are extracted from store and sent to node store via output buffer. Unmatched tokens are usually written to spare table location. If hash line overflows, token is referred to separate overflow unit. Provided that hash keys differ, matching unit handles further tokens even before overflow outcome is known. Output occurs once every 300 ns on average

Simulation studies indicate that matching unit throughput remains largely unaffected until the hash table is about three-quarters full.[6] This compares favorably with other hashing schemes.

Viewed overall, the store and release mechanisms in the matching unit alter the nature of the pipeline between input and output. Output is less frequent than input but involves greater amounts of information. Simulation predicts that token packages arriving at 200-ns intervals will produce group packages every 300 ns on the average. This figure, however, depends critically on the form of programs. The basic hash table access time is 160 ns, and the three possible access types, neglecting overflow, take 40 ns for bypass, 240 ns for a successful match, and 320 ns for an unsuccessful match attempt. Given roughly even numbers of each access type, as would be expected, this yields the average figure cited. However, a long sequence of unsuccessful match operations results in inefficient use of later pipeline stages.

## Node Store

Two pipeline stages implement the node store (Fig 6). The first stage accesses a segment table containing 64 entries addressed by the six most significant bits of the incoming destination field. Each segment table entry points to the base of a segment of main node storage and holds an indication of the segment length. The second stage of the node store unit accesses the required node using 12 bits of the

destination field as an offset from the segment base. Accesses beyond the end of a segment flag an error. Node entries may be one or two words long; 2-word entries are accessed in sequence.

Depending on the kind of node entry discovered, the node store constructs an executable package for output to the processing unit. These packages are consumed at an average rate of one every 300 ns, the same rate at which input arrives at the node store. The 16-word main node store has an access time of less than 200 ns so that it can handle programs in which up to half of the nodes require 2-word entries.

## Processing Unit

Prototype computer system design dictates that all design decisions offer maximum flexibility. In particular, it is prudent to anticipate instruction set changes. This requires development of a microprogrammable processing unit. Because flexible microprogramming is relatively time consuming, it proved necessary to use a parallel array of processing elements within the processing unit to maintain the required throughput by processing one executable package every 300 ns. Fig 7 shows the basic structure of the processing unit.

The first pipeline stage executes certain high speed (200-ns) operations that cannot be performed within the parallel array. These operations control generation of activity names in the system and allow for gathering performance statistics. The main processing area comprises the parallel array of processing elements with appropriate input and output buffers. Each element is built around a 24-bit arithmetic unit constructed from 4-bit AMD2900 series bit slice microprocessors. A microprogram controller with a writable microcode store controls the main processing area to achieve the required, flexible instruction set.

Processing elements have a 200-ns microcycle time, and instruction execution periods that vary from 5 to upwards of 50 microcycles. The average expected execution time for a processing element is 4.5 $\mu$s per operation. Hence, the number of elements required to maintain the throughput at one executable token package every 300 ns is 4.5/0.3 = 15. More elements would leave a high percentage of elements idle because the pipeline could not provide input quickly enough to keep them busy; fewer would lead to a general slowing down of the system because the processing array could not cope with input as fast as the pipeline supplies it.

Token package execution results in the production of zero, one, or two result token packages. The expected combination of these different behaviors is such that the average consumption of executable packages once every 300 ns will lead to an average production of result token packages once every 200 ns.

The processing unit is synchronized with a relatively slow (10-MHz) clock to simplify the problems of distributing packages to and collecting packages from the processing elements. Each distribution or arbitration cycle is selected in advance and then executed in synchrony with the clock.

## System Performance

The most important feature of the pipeline just described is that all stages are independent from buffer to buffer. Each stage relies only on its input and its internal storage. This means that the system performance is determined by the overall amount of work provided, in the form of token packages, together with the average timing characteristics of the pipeline.

Average delay times associated with various pipeline stages yield a maximum processing rate of one executable package every 300 ns. Using the approximation that one

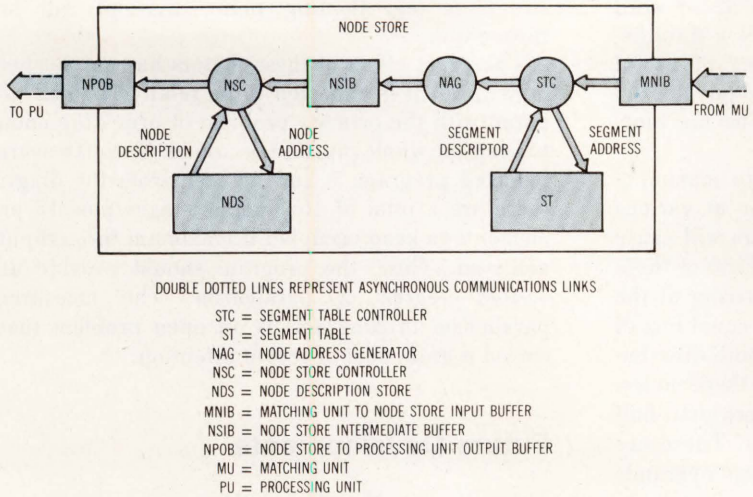
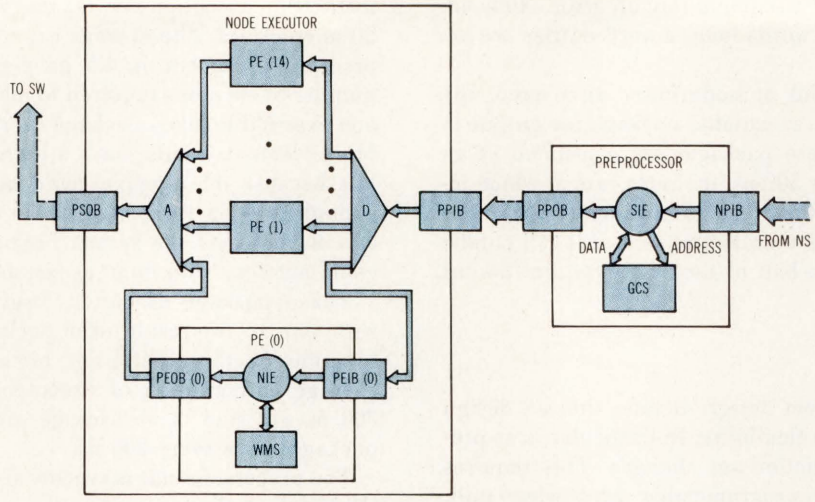



Fig 6 Node store. Two separate pipeline stages comprise node store. First stage accesses segment descriptor from 64-entry segment table and forms read address of required destination node. Second stage accesses node from one or two words in main node store. Resulting executable package is sent to processing unit via output buffer




DOUBLE DOTTED LINES REPRESENT ASYNCHRONOUS COMMUNICATIONS LINKS

SIE = SPECIAL INSTRUCTION EXECUTOR
GCS = GLOBAL CONTROL STORE
D = 15-WAY SYNCHRONOUS DISTRIBUTOR
A = 15-WAY SYNCHRONOUS ARBITRATOR
PE = PROCESSING ELEMENT
NIE = NORMAL INSTRUCTION EXECUTOR
WMS = WORKSPACE AND MICROPROGRAM STORE
NPIB = NODE STORE TO PROCESSING UNIT INPUT BUFFER
PPOB = PREPROCESSOR TO PROCESSOR OUTPUT BUFFER
PPIB = PREPROCESSOR TO PROCESSOR INPUT BUFFER
PEIB = PROCESSING ELEMENT INPUT BUFFER
PEOB = PROCESSING ELEMENT OUTPUT BUFFER
PSOB = PROCESSING UNIT TO SWITCH OUTPUT BUFFER
NS = NODE STORE
SW = SWITCH

Fig 7 Processing unit. Parallel array of 15 bit-sliced, microprogrammable processing elements achieves main processing capability. Distribution and arbitration are performed synchronously. On average, unit consumes executable package once every 300 ns and produces tokens at 200-ns intervals. Preprocessing stage performs system and monitoring tasks that cannot be distributed to individual processors because they are not strictly functional operations

executable package is equivalent to a conventional machine instruction in a comparable processor with a 32-bit word length and floating point operations, this gives a throughput of roughly 3.3M instructions/s. In terms of useful floating point operations, this has been found equivalent to about 1.1M floating point operations/s for one machine-coded example.

It must be stressed, however, that these are maximum rates that rely on uniform program behavior at various stages of the pipeline. Three secondary factors will cause performance degradation from the optimum. First of these is a long sequence of unmatchable tokens arriving at the matching unit. High performance relies on an equal mix of 1- and 2-input nodes in the program and a smooth distribution of matching store accesses resulting from these nodes. Secondly, the node store should receive no more than half of its total requests for double-length entries. These are typically used for instructions with literal constant operands and for copy operations; they occur quite frequently in practice. Finally, the processing unit requires an even mix of different kinds of executable packages to maintain the average execution period. A long sequence of lengthy instructions (eg, floating point division) will lower the throughput.

The exact effect of these factors has not yet been determined, but it is expected to be relatively small when compared with the primary problem of providing enough work to keep the whole pipeline occupied. Given an average, well-behaved program, it can be seen from the diagrams that there are a total of 16 pipeline stages plus 15 processing elements to keep occupied if maximum throughput is to be achieved. Thus, the program should provide at least a 31-fold degree of parallelism. The measurement of parallelism in programs is an open problem that has received a great deal of recent attention.[7, 8]

## Future Developments

Although the Manchester University research group is engrossed in practical details of machine implementation at the moment, there has been ample opportunity to anticipate

future challenges when the system is completed in 1981. Two interesting areas of study have emerged. One is the development of richly expressive, and yet efficiently translatable, high level languages for programming data driven systems. The second is realization of an extensible computer whose power may be increased without theoretical limit simply by adding more and more hardware modules.

## High Level Languages

It is no longer practical to design computer systems without regard for the programs they are intended to run, and most programs currently in use are written in a high level language. Consequently, many machines, including data driven machines, are designed around specific programming languages, and others, such as the one described here, are developed in close conjunction with a programming discipline.[9, 10, 11]

For general purpose systems, there is a broader requirement to run a variety of different languages, and it is interesting to see how versatile the data driven system can be in implementing these. Programming languages can be classified into three groups for this purpose.

The first group comprises those languages developed around data flowgraphs, usually for high speed parallel computing. These are expression oriented, or single-assignment languages with parallel semantics based on a data driven view of program execution. Of course, they are therefore a natural high level vehicle for data driven computers, as Part 1 of this article demonstrated in discussing the ease of translation into graphical machine code.

More of a challenge is presented by the second group of high level languages. It consists of the traditional, von Neumann languages with their semantics based on variables in fixed storage locations and sequential execution of program statements. Sequential flowgraphs for such programs can be generated by a straightforward, if somewhat tedious, translation.[12] However, the challenge is to unwind the sequential execution completely so that as much work as possible may be performed in parallel. This requires the use of sophisticated loop unraveling techniques together with software flow analysis.[13, 14]

Languages whose semantics are purely mathematical and not based on any particular view of program execution comprise the third group. These are founded mainly on the theory of mathematical functions (the lambda calculus) with the important exception of the language LUCID, which is based on an algebra of histories.[15] Because these languages are not machine oriented, they are difficult to implement efficiently on conventional computers. The principal problem is that of minimizing the amount of computation performed. Although the problem is also present for data driven implementations, there is some indication that the parallelism available to be exploited in data driven systems allows rapid execution of functional programs.

At present, high level software for data driven systems is at an early experimental stage. Pilot compilers for all three groups of high level languages have been written, but there is no clear indication of an optimal language among the candidates. On the other hand, most researchers agree that languages based on the von Neumann model are not appropriate for specification of highly parallel algorithms.

## Extensible Hardware

Data driven notation was developed as a means for expressing highly parallel computational activity. However, the architecture described here is limited in the amount of parallelism it can exploit by the need for sequential token matching within a serial pipeline. Since the prototype system has proven to have just over 30-fold hardware parallelism, problems with much greater amounts of parallelism will run relatively slowly. Two possible improvements to the prototype architecture may allow much higher rates of computation.

The first improvement would not alter the basic pipeline structure at all, but would instead increase throughput by making the primitive machine operations much more substantial than the simple arithmetic operators suggested in Part 1. Each executable token package could then represent a much larger fraction of the whole computation, and the fixed rate of package execution would increase the overall processing rate. While this might require a larger complement of more complex processing elements, the biggest difficulty lies in deciding which powerful primitive operations should be included in the instruction set.

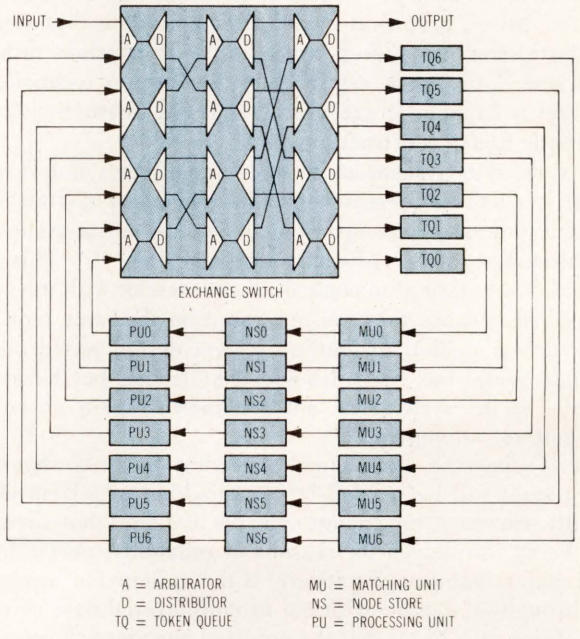



Fig 8 Parallel array of data driven rings. Very high processing rates might be achieved by connecting large numbers of pipelined rings in this kind of structure. Unidirectional, pipelined exchange switch is modularly extensible and of relatively simple form as compared to crossbar switch, for example. In very large systems, major problem is to distribute workload evenly among data driven rings

The second improvement involves changing the system structure so that several serial pipelines can operate simultaneously in a parallel array. The nature of the matching operation is such that tokens with similar colors and destinations could be isolated in separate pipelines as long as the output from any processing unit can reach the input to any matching unit. The unidirectional nature of the pipeline makes this feasible with relatively low cost in time and hardware complexity. The resulting system has a number of pipelined ring structures connected in layers to a greatly extended switch unit, as shown in Fig 8. The time delay through the switch increases logarithmically with the number of rings.

Consequences of this multilayered structure are far reaching. It seems capable of indefinite expansion, providing continually increasing computing power for problems with sufficient parallelism to keep the hardware busy. Of course, there are many practical difficulties that are largely concerned with the problems of distributing work evenly between layers of the system.

## Conclusions

Starting with the observation that the speed of computation for some problems needs to be much higher than is presently achievable, and that the best hope for achieving the required speed is through the use of parallel hardware, a novel parallel computer architecture with some interesting properties has been developed. The architecture is based on a data driven, graphical model of computation that views program structure and execution in two dimensions rather than one. A prototype system that uses low key technology and yet is capable of executing about 3M instructions/s is currently under construction.

Several other systems are at comparable stages of development. In particular, researchers at the University of Utah and Toulouse already have operational systems, and a group at MIT is about to start construction of a machine.[9, 16, 17] This article did not attempt to compare these systems with the one described because they are not based on the same type of data driven model. An outline system design based on a similar model has been developed at Irvine, but because details of the system are not yet known, again no comparison was attempted.[10]

It is expected that some alteration in programming techniques will be needed to use this kind of system efficiently. However, the changes may be of a kind that already are being introduced for reasons of reliability, portability, and maintainability of software. If the anticipated increase in throughput can be achieved in multilayered data driven structures, it is likely that the required changes will present a minor obstacle to development of such a system.

## Acknowledgments

We would like to acknowledge the assistance of all the members of the Data Flow Research Group at Manchester, whose many ideas have contributed continually to the development of the data driven computer. Chris Kirkham also was kind enough to read and comment upon the draft manuscript. In addition, the financial support of the Distributed Computing Systems Programme of the Science Research Council of Great Britain is gratefully acknowledged.

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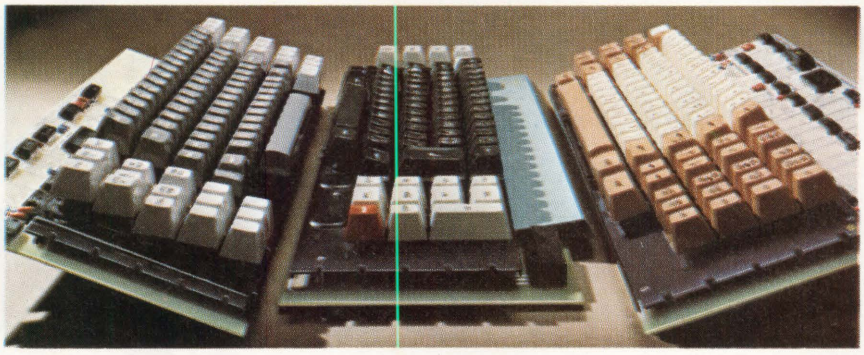

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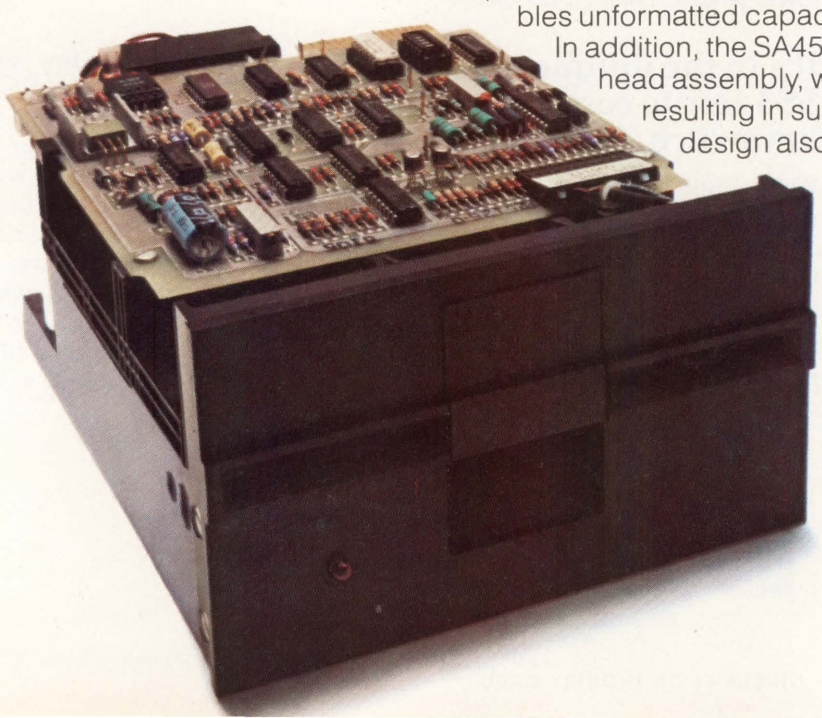

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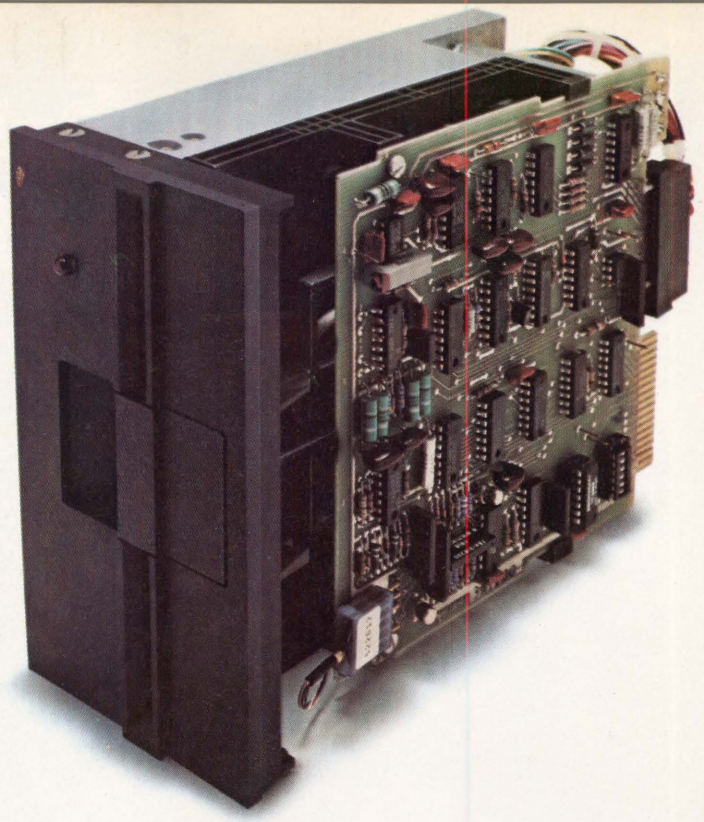

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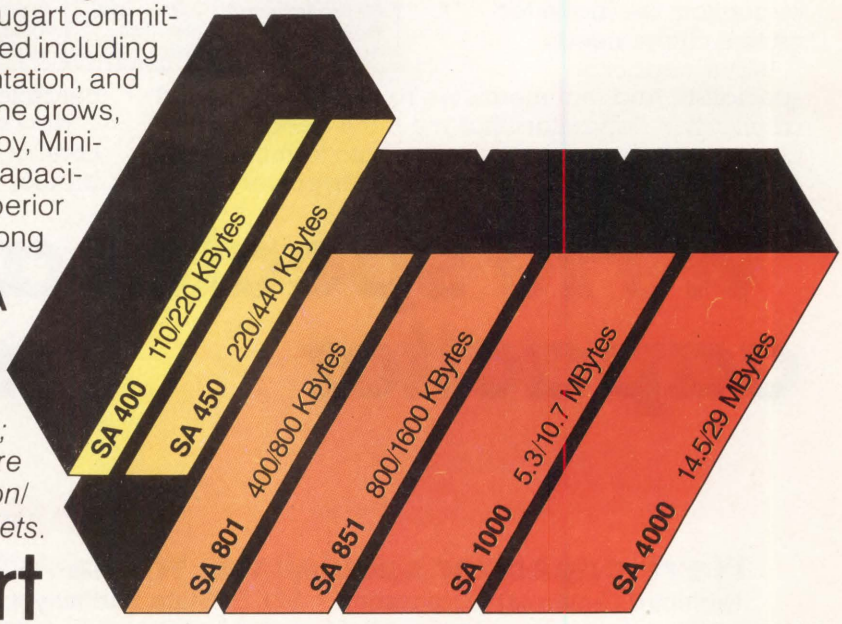


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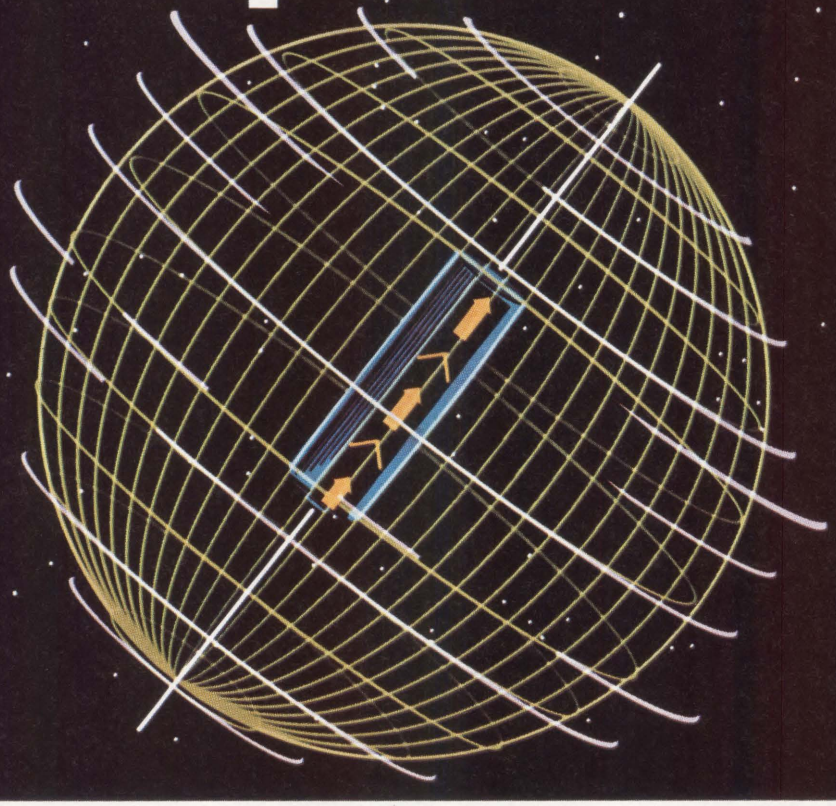

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# BIT MAP ARCHITECTURE REALIZES RASTER DISPLAY POTENTIAL

Low cost random access memories and microprocessor based control circuits accelerate the trend toward raster scan display systems that use bit map architectures to provide dynamic, interactive control over each picture element on the screen

**Robert J. Gray**

Genisco Computers
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Graphics and image processing systems constitute one of the fastest growing segments of the computer industry. Projections of current trends indicate that display system sales will double within the next three years to more than $600 million per year (Fig 1). Refreshed raster systems, most of which will be equipped with color monitors, could represent half of this total. These figures exclude the expanding personal computer market, which will most likely continue to use the familiar raster scan television receiver both as an alphanumeric display device and as a graphics monitor. The rapid growth in display systems of all types confirms the adage that a picture is worth 1k words, especially when large volumes of data must be presented in a form easily interpreted by the growing numbers of nontechnical operators.[1]

Refreshed raster displays offer a combination of potential advantages over their major competitors, the storage tube and the refreshed vector calligraphic or stroke writing system. Their photographic quality is equally adaptable to line graphics for computer aided design, solid tones for charting statistical data, and continuous tone imagery for applications ranging from medical instrumentation to satellite reconnaissance. Their cinematic capability provides the observer with a sense of continuous animation and, equally important, an almost instantaneous response to interactive commands. They offer a full spectrum of synthetic shades generated by the computer for such applications as process control and business graphics displays, and of real hues and saturations for manipulating images generated by a television camera or a spot scanner. In addition, mass production techniques developed for commercial television receivers make the inherent advantages of refreshed raster technology economically feasible in graphics and in image processing applications.

Historically, the photographic and cinematic potential of the raster scan led to its use in commercial television and to the subsequent development of a practical color raster monitor. Unlike calligraphic displays that stroke lines between randomly addressed points on the cathode ray tube (CRT) screen, a refreshed raster scan addresses, typically 30

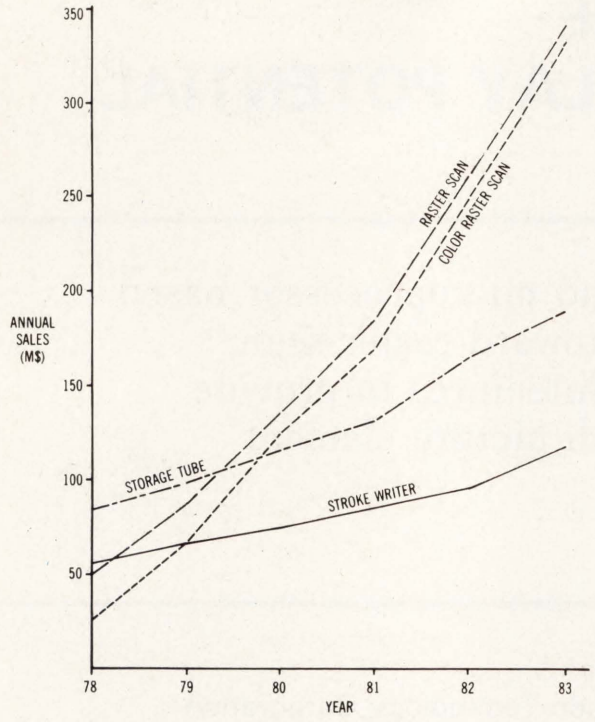



Fig 1 Projections of current trends. Display system sales could double within three years, reaching nearly $600 million. Refreshed raster systems could reflect half this total. Storage tube and stroke writer sales also will grow, but probably at a slower rate

or 60 times/s, every individual picture element (pixel) on the entire screen during each refresh cycle. Every pixel has the potential, therefore, of being defined and redefined in real time provided only that the system can deliver the required information to the monitor within the time limits imposed by the raster refresh cycle.

This refresh is most effectively achieved by storing the information in a display memory that will duplicate the data presented on the CRT screen. The techniques used to store and process the display data become, therefore, critical factors in determining the extent to which a system takes advantage of the potential of raster scan techniques.

The potential for higher photographic quality is enhanced by requiring that a maximum number of pixels be coded in memory and defined on the screen. The ability to produce colors, or multiple shades of gray, increases the amount of information required for each pixel. The possibilities for cinematic animation and fast response require processing an expanding volume of data at the highest possible rate. In a sense, then, each inherent advantage of raster technology presents graphics system designers with opportunities as well as challenges.

Bit map architectures represent the ultimate in design challenges because of the need for a separate binary code for each pixel on the screen. The use of these architectures is the most memory intensive of all the mapping alternatives to be described and requires the highest processing speed. At the same time, bit map architecture is the only design approach that delivers all potential benefits of the refreshed raster technique, and to the extent that bit map systems fulfill this promise, bit map advantages equate to those of raster technology.

## Resolution

Photographic quality depends on resolution, the number of addressable locations on the CRT screen. With each increase in resolution there is a corresponding increase in the fineness of detail, straightness of lines, and continuity of graduated color or intensity changes. A hypothetical grid of horizontal and vertical lines on the screen surface establishes resolution. The increased resolution of raster

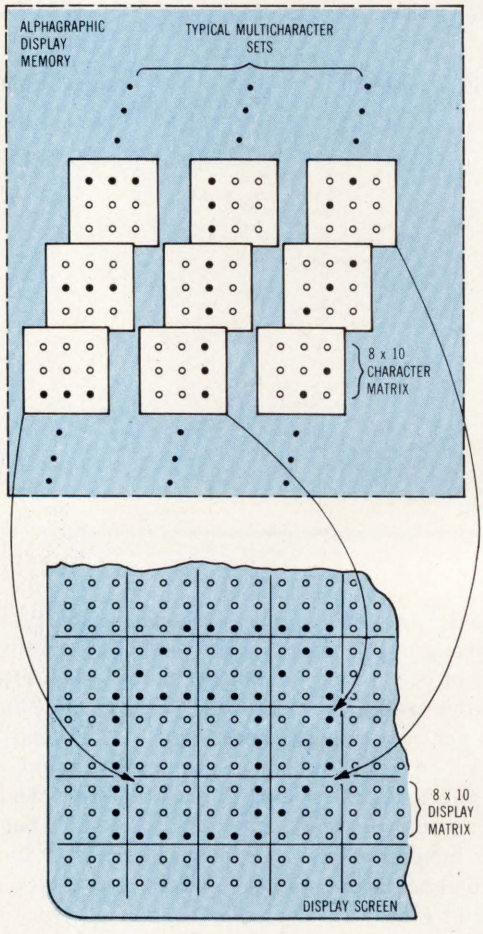



Fig 2 Alphagraphic mapping. Used to display lines and other simple graphic elements, character mapping scheme reduces display memory requirements about tenfold but also limits ability to control each individual pixel

displays was prompted, in large part, by the expansion of raster systems into new application areas and into established stroke writer domains, such as computer aided design and aircraft flight simulation. A typical, medium resolution raster display has a resolution of 512 by 512 lines. A higher performance system may increase the resolution to 1024 lines in one or both dimensions.

By contrast, stroke writers have hypothetical grids ranging up to 4096 lines or more; however, the stroke writer grid is truly hypothetical. Straight lines, for example, are defined in stroke writer system memory by their endpoint coordinates which correspond, in theory, to exact locations on the screen. By the addition of another bit to the coordinate data, the stroke writer resolution is doubled. The increase in resolution may be invisible to the eye, when viewed on a stroke writer screen and may become apparent only after the creation of a full resolution hard copy.

The raster grid, however, is only partly hypothetical. A raster scan produces physical horizontal lines on the CRT screen, and the distinguishable vertical alignment of pixels along each horizontal line determines the vertical grid. Doubling raster resolution requires the monitor to trace twice as many raster lines within the same refresh time. Video signal amplifiers must have four times their previous bandwidth, when raster resolution doubles, and convergence controls for color monitors must be not only faster, but far more precise to maintain color registration.

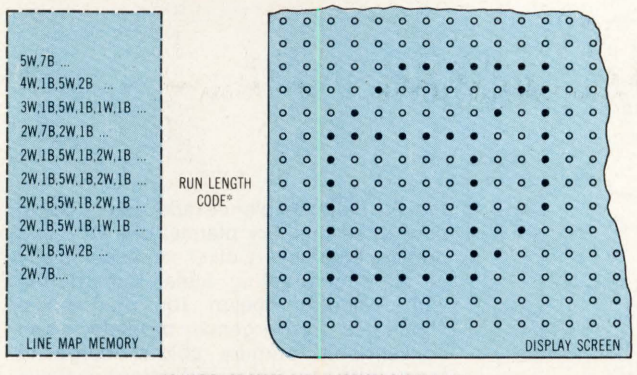
These high performance raster display monitors are presently available. Reduced spacing between shadow mask holes can now be used to help preserve the increased resolution of a color raster display system. For the system designer, however, the major task has been to meet the expanded memory and processing requirements that accompany each increase in resolution, without compromising the pixel by pixel, photographic potential of the raster technique. It has taken innovative microprocessor control concepts and inventive memory architectures based on new, lower cost, random access memory (RAM) to achieve this goal.

## Display Mapping Techniques

Raster display memory and transfer rate requirements expand geometrically with increased resolution. A 512 by 512 raster system must store definition data for a minimum of 262,144 pixels. A 1024 by 1024 raster display has 1,048,576 pixel locations. Up to 24 bits can be specified; yet with only 8 bits of information for each pixel, there is an increase from about 1M bits of stored data to more than 8M bits, all of which must be accessed within one refresh cycle.

In terms of transmitting data to the monitor, a higher resolution system with 8 bits/pixel would require a processing and transfer rate of about 500M bits/s. But equally important new information would have to be read into the memory at very high rates to maintain any sense of cinematic animation or realtime response. The temptation, of course, is to compress the memory with alternative mapping techniques. One method, for example, is character mapping, an extension of the use of alphagraphic characters to create lines and other simple designs on alphanumeric terminal displays (Fig 2). The IBM 3279 color graphics terminal typifies this approach, allowing definition of up to six sets of alphagraphic characters with 190 different pixel arrangements in each character set. However, the 1140 patterns represent only an insignificant fraction of the $2^{80}$ possible combinations of pixels within the 8 by 10 character matrix. There is a corresponding loss, therefore, in the ability to address and quickly modify an individual, randomly selected pixel from the hundreds of thousands on the monitor screen.[2]

Line mapping, another memory compression technique, achieves still greater versatility (Fig 3). Compared to the bit map approach, run length encoding can achieve a 30:1 reduction in memory requirements. However, this holds true only when the graphics are relatively simple. As the level of detail increases, the quantity of coded information escalates. Continuous tone images with changing values for successive pixels would consume far too much memory to display on a line-map raster system. This leaves bit map




*QUANTITY OF CODED DATA INCREASES RAPIDLY WITH LEVEL OF DETAIL, CONSUMING FAR TOO MUCH MEMORY FOR USE WITH CONTINUOUS TONE IMAGES

Fig 3 Line mapping. Run length encoding reduces display memory requirements up to thirtyfold—and also speeds display memory loading—but only for relatively simple graphics with few pixel transitions per line. Quantity of coded data increases rapidly with level of detail, consuming far too much memory for use with continuous tone images

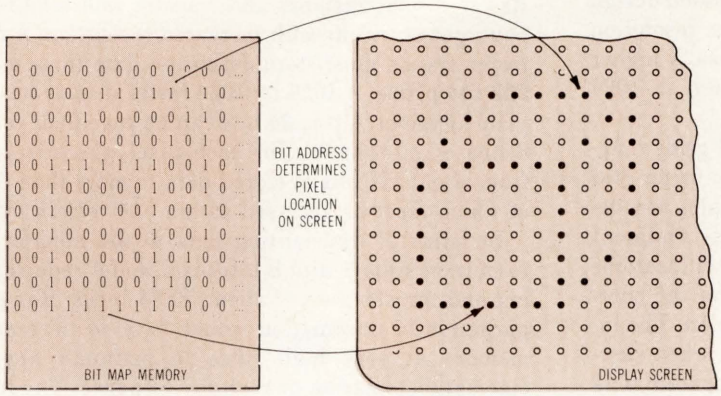



Fig 4 Bitmap display mapping. Simplest approach assigns one bit of display memory to each pixel on screen. In practice, bytes or words pass through shift register to supply serial data as video generator input. Display memory addresses correspond to pixel locations on screen

memories as the only storage method that gives the application program and the operator complete control over each pixel.

## Multiple Memory Planes

The simplest bit map display memory would assign a single bit to each pixel displayed on the screen. There would also be a one to one correspondence between the memory addresses and the display coordinates (Fig 4). In practice, memory bits are accessed in 8-bit bytes or 16-bit words, transferred to a shift register, and only then applied, as serial data, to the video signal generator. A binary 1 typically generates a full intensity spot of light at the corresponding pixel location on a monochrome monitor screen, while a binary 0 effectively turns off the CRT electron beam, producing a dark pixel on the screen.

With only a single bit per pixel, the memory would not begin to tap the color and gray scale potential of a bit map raster graphics system. It could emulate, of course, a lower performance stroke writer, at a considerable cost saving to the user. However, expansion to multiple-bit codes for each pixel location would offer advantages beyond those afforded by any other type of display system.

The technique used to create multiple-bit codes without reducing memory access speed simultaneously stores information on multiple memory planes, each representing a complete map of the display screen. Multiple planes add a Z dimension to the display memory, in addition to the X and Y dimensions implied by the pixel address. On the screen, the Z dimension appears as intensity or color.

How two or more monotone memory planes can be used to encode data for display on a monochrome monitor is illustrated in Fig 5. By applying parallel bits to a digital to analog converter (DAC) at the video input, black, white, and tones of gray are reproduced on the screen. For example, with eight memory planes each pixel can be coded for any of 256 different monochrome shades, far beyond the ability of the human eye to discern boundary lines between gray tone transitions.

Three- or Z-dimensional coding also makes it easy to add color to the graphics presentation using a 3-gun color televi-

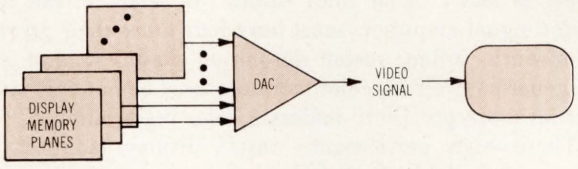
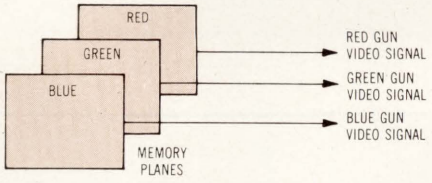



Fig 5 Multiple planes add third dimension. Applying parallel bits to DAC at video input produces black, white, and tones of gray on monochrome display screen. Pixel address implies X and Y coordinates. Z dimension appears as intensity or color. With eight memory planes, each pixel can assume any of 256 different shades




| RED GUN | GREEN GUN | BLUE GUN | PERCEIVED COLOR |
|---|---|---|---|
| OFF | OFF | OFF | BLACK |
| ON | OFF | OFF | RED |
| ON | ON | OFF | YELLOW |
| OFF | ON | OFF | GREEN |
| OFF | ON | ON | CYAN |
| OFF | OFF | ON | BLUE |
| ON | OFF | ON | MAGENTA |
| ON | ON | ON | WHITE |

Fig 6 Multiple planes add color. Using only three memory planes, one for each primary color, every pixel can assume any of eight contrasting hues. Substituting white electron beam for blue beam eliminates convergence problem when conventional primary colors merge to form white characters, still affording black and white with various combination and saturations of red and green

sion monitor. With only three memory planes, separate on-off bits can control the red, green, and blue electron beams to produce the eight colors, including black and white, listed in Fig 6. When displayed information includes a high proportion of white alphanumeric symbols, a 3-gun monitor with red, green, and white phosphors eliminates convergence problems encountered when the conventional primary colors merge to form white alphanumeric characters. In this case, the eight colors are white, black, and various combinations and saturations of red and green.

Yet the 8-color palette is only the starting point for bit map raster displays. DACs driven by multiple memory planes for the primary colors can produce dozens or hundreds of different hues and saturations. Alternately, a smaller number of memory planes might supply addresses in a look-up table that correspond, in turn, to multiple-bit color codes for the display monitor. Fig 7 illustrates how an 8-plane memory can address up to 256 different colors selected from a potential range of 4096 hues and saturations. The host computer program can alter the lookup table entries dynamically, and the table can be expanded with more bits per address and more bits per pixel, to generate a wider range of colors than the eye can distinguish.[3]

## Postprocessing

Multiple display memory planes combine with lookup tables and other programmable function generators to provide bit map raster systems with powerful postprocessing capabilities that add a cinematic quality to the display without changing the content of display memory. An earlier article described the use of 8 by 8 function memory tables to perform spatial filtering, edge enhancement, contrast control, and other image processing operations at a full, frame by frame rate. Selector switch control logic permits global variations, affecting the entire image, or local imaging functions in chosen locations on the monitor screen.

Similar postprocessing increases the usefulness of information generated by a computer aided tomography (CAT) scanning system. Here, body tissue densities are calculated to a very high precision (eg, 12-bit values) and stored in a multiple-plane bit map memory. Addressing the planes selectively in conjunction with a lookup table provides color coded or step contrast displays of one or more density levels. A physician can direct the system to display only those density values characteristics of bones, soft tissues, blood vessels, blood clots, or any combination of these structures.

Completely different images can be stored, if desired, on the bit map planes and displayed in any combination on the screen. A typical application of this technique would be found in the design of multilayer IC masks. With a pattern for each IC mask stored in a separate bit map plane, the designer can view individual masks, superimpose transparent or opaque layers, and toggle from one set of patterns to another for quick comparisons.

A variety of transformations can also be implemented in hardware as part of the postprocessing. Displays can be scaled up or down in size by duplicating or skipping pixel

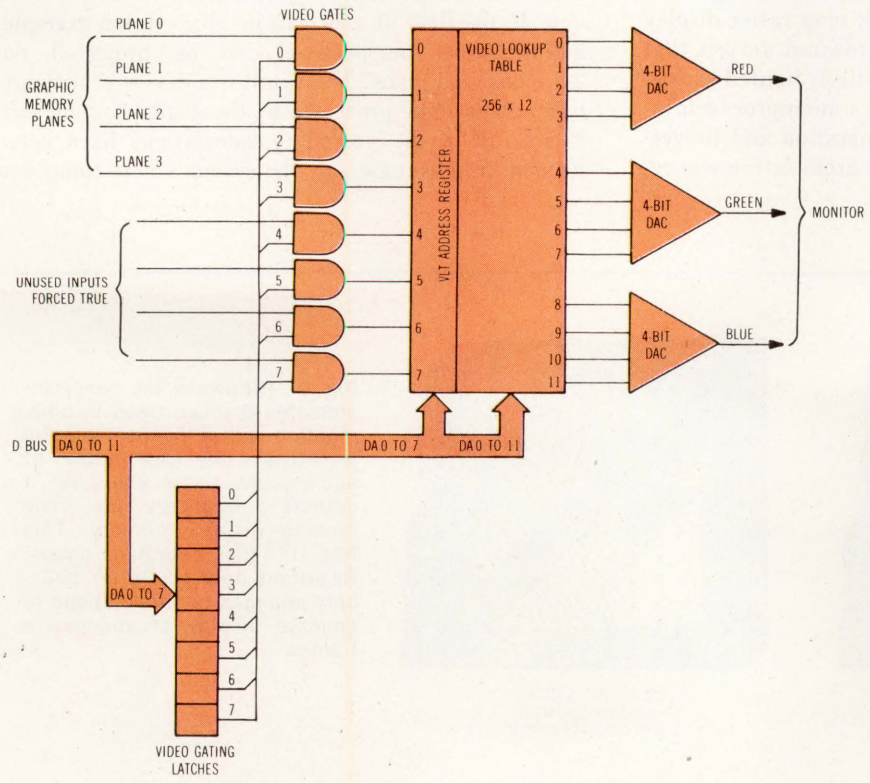



Fig 7 Lookup table extends spectrum. Fully programmable 12-bit lookup table selects any subset of up to 4096 possible color combinations. Using eight memory planes, system offers dynamic selection of 256 different colors. Table expansion adds more bits per entry or more bits per pixel to generate wider range of colors than eye can distinguish

values and raster lines, or a mirror image can be created, simply by changing the addressing sequence. In addition, scrolling can be achieved by starting the raster scan at different address locations within the bit map memory. When panning, new material can be scrolled into view by expanding the memory and using a virtual addressing scheme to select a movable display window. Information for several different displays can share space in memory to support split screen effects or brief animation sequences. The display can roam, in effect, to any point in the virtual display memory, or even to different areas on different planes.

A similar extension to the bit map memory can serve as a freeze frame buffer when the source of imaging data is a television camera or a spot scanner. Additionally, a double-size memory could act as a buffer between the display generation circuits and the monitor. One half of the memory would be used to drive the monitor while the other half is being loaded with new data. To the operator, the switch to a new display would appear to be instantaneous; no partially assembled images or graphic elements would be visible.

A variety of other hardware processing functions can be added to increase the versatility and throughput of a raster display system. Fig 8 illustrates the effects achieved by a hardware fill circuit that automatically changes the display color at boundary lines stored in the display memory. Individual boundary lines can be altered in a fraction of the time required to change all of the pixels within the bounded area, increasing the rate at which animated sequences can be generated and presented.

## Advanced Architectures

The hardware fill technique represents a continuing effort to increase the cinematic quality of bit map raster display systems. The earliest systems were hardwired devices that generated pixel code arrays from a relatively limited variety of display coordinate elements. Adding a microprocessor increased both the speed of display generation and its versatility. However, the straight through architecture was retained, and as the number of pixels in the display increased, the microprocessor cycle time became a limiting factor, especially when functions such as generation of circles and arcs were performed by software.[4]

More advanced systems now use a variety of hardware function generators and a multiple-bus architecture. There are, typically, a separate processor and memory buses linking the display memory planes, hardware generators, peripheral interfaces, and display controllers. The memory bus allows data transfer between memory modules and helps support such functions as splitting the screen, scrolling, and the combining of memory segments into a single display, all completely independent of the processor.[5]

A third type of architecture, particularly applicable to image processing, incorporates a feedback loop from the display output to the memory planes so that iterative calculations can be accomplished and displayed at realtime rates. Scale-ups or scale-downs can be zoomed and, with just a few iterations, small convolution kernels can become expanded kernels that other architectures could not practically process within the same time frame.

## Offloading The Host

A display system dedicated to image processing can be relatively self-contained. Generally the digitized output of a television camera or a spot scanner creates source data that can be loaded directly into the bit map memory planes for processing by the display system software. By contrast, computer generated graphics and images usually reflect the end product of a series of transformations. A variety of modeling operations process source data to define a set of display objects in a 2- or 3-dimensional world. The display elements are then subjected to viewing operations that equate to the functions of a theoretical camera (Fig 9). Portions of objects outside the field of view can be clipped, for example, and 3-dimensional perspectives can be projected onto a 2-dimensional plane. The result is a device coordinate data base, ready to be processed by the display system software. Nearly all of the preceding calculations have been performed, in most cases, by the system's host computer.[6]

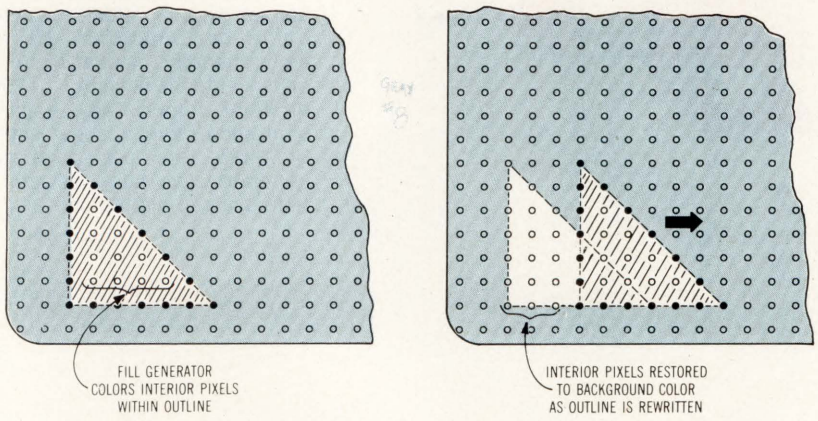



Fig 8 Hardware fill generator animates display. Used in combination with a lookup table, fill generator changes color of subsequent pixels whenever it detects a boundary line while reading display memory. This fills in the bounded shape. Rewriting only pixels on boundary changes bounded shape to animate display of successive frames

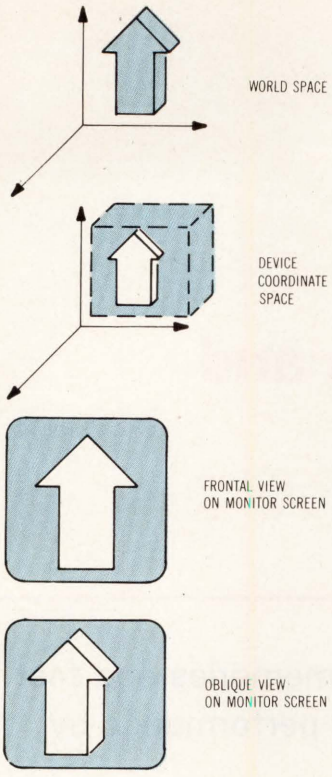



Fig 9 Viewing operations. Three-dimensional data can be viewed from any arbitrary vantage point to simulate function of a theoretical camera. Two-dimensional systems generally limit viewing operations to locating a window on the coordinate plane

This scenario is now shifting, particularly in the case of bit map raster systems. The trend is toward multiple processor systems with separate microprocessors to handle the host interface, memory management, and display generation functions. With processing power to spare, the graphics system software is taking over an increasing number of functions from the host computer, relieving it of the heavy computational burden imposed by a graphics application. Additionally, graphics system software modules have been expanded to include a variety of interactive and application directed transformations of device coordinate data, such as the scaling, translation, and rotation of individual display elements. The next step, already in progress, involves the transfer of 2- and 3-dimensional viewing operations. Also, a number of application oriented graphics software packages incorporate modeling aids, such as the generation of bar graphs for business reports and trend displays for process control applications.

A continuation of these evolutionary developments will lead to the day when bit map systems that take maximum advantage of the benefits offered by the raster scan display technique will be true standalone units, direct replacements for the host computers they now serve.

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*Co-founder and Vice President of Genisco Computers, since its inception in 1975, Robert J. Gray designed the initial version of the Genisco Graphics Display. For 22 years prior to 1975, he was an officer in the U.S. Navy, serving as a meteorologist and a computer specialist. As such he was highly instrumental in the automation of the Naval Weather Service System.*


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TECH NOTE

# Balancing RAM Access Time and Clock Rate Maximizes Microprocessor Throughput

Tuning timing relationships of high performance memories and fast buffer logic in microprocessor systems increases performance by eliminating unnecessary wait cycles

**Stan Groves**

Motorola Integrated Circuits Division
3501 Ed Bluestein Ave, Austin, TX 78721

Throughput and execution rate are of paramount importance in some systems. These systems require the most suitable microprocessor, running at the maximum usable clock rate, and the fastest available memories. More often, system cost also determines some, if not most, of the component parts used to build a system. Components are selected as the best compromise between performance and price. However, in quasi-synchronous systems, timing effects can interact so that it is not obvious just which of the various memory access times offers best performance, or whether the system will benefit from use of high performance memories.

Although the MC68000 has an asynchronous data and address bus, in the sense that it can wait interminably for a response showing availability of requested data, the microprocessor illustrates a quasi-synchronous machine in the classical sense: internal operations are asserted and external signals are sensed at specific clock times. Owing to the internal synchronous nature of this microprocessor, all bus access times are in increments of one full clock period. It senses all input data and control lines when the clock is in its high state and captures data or control line states when the clock goes low.

For example, as shown in the read cycle timing diagram of Fig 1, data acknowledge ($\overline{\text{DTACK}}$) is asserted low prior to the falling edge of the fourth clock state (S4). As long as $\overline{\text{DTACK}}$ is asserted a full setup time period prior to the falling edge of any clock signal, such as S4, $\overline{\text{DTACK}}$ will be sensed during that clock period. If $\overline{\text{DTACK}}$ is asserted low less than the required setup time prior to the falling edge of S4, a wait cycle of one full clock period, which equals two states, would be added. When $\overline{\text{DTACK}}$ is sensed low at the end

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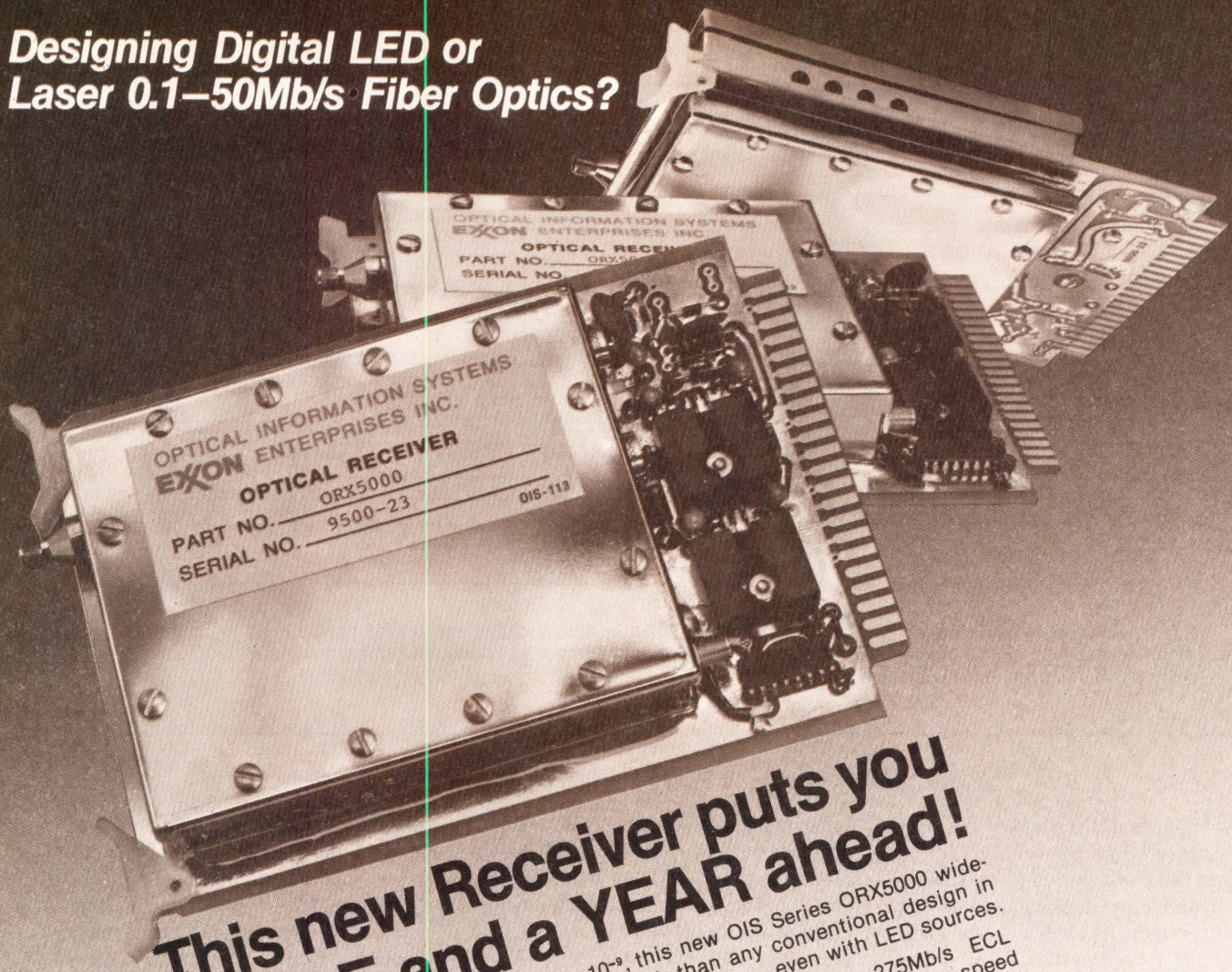


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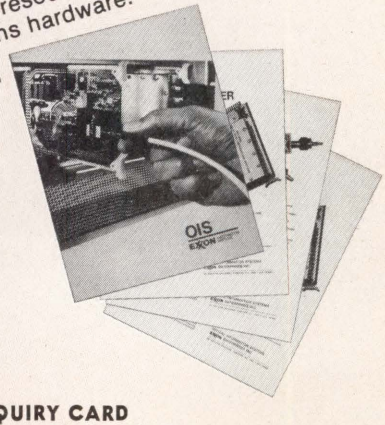


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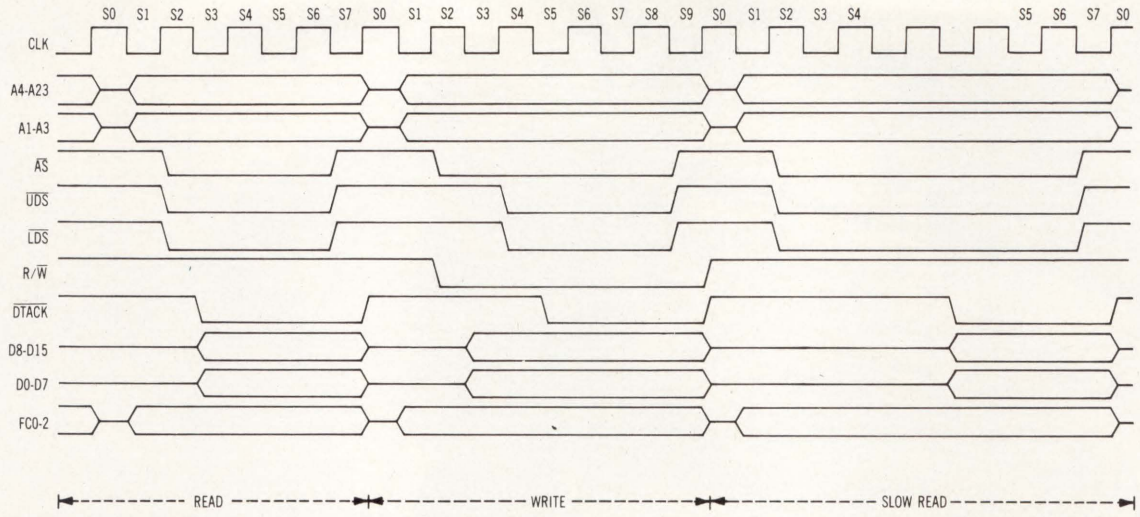


Fig 1 Read/write cycle timing diagram. As long as DTACK is asserted one setup time period prior to falling clock edge S4, it will be sensed during that clock period. Otherwise, as shown on right side of diagram, wait cycles will be added until DTACK is sensed

of a clock period, the state of the data bus is captured on the falling edge of the next full clock period (S6 in this instance) and only then applied to the microprocessor. As shown on the right side of Fig 1, wait cycles or wait states are added after S4 until DTACK has been low for the full setup time prior to the falling edge of the clock signal.

Any system that uses even a small portion of the MC68000 addressing capability needs signal buffers. The delay through these buffers, the delay through the logic to generate row address select (RAS) for the random access memories (RAMs), the output delay of the address lines and address strobe (AS) signals, and the data port input setup time must be considered overhead to the specified memory access time. Table 1 shows this additional overhead by listing RAM access times, typical values for the time delay through Schottky (S) and low power Schottky (LS) buffers, the critical path that generates RAS from AS, and MC68000 data setup delay with AS delay.

**TABLE 1**

**Access Time and Clock Rate Interrelationship**

Additional Overhead (ns)

| Specified RAM Access Times (ns) | Buffers 'S240 | Buffers 'LS240 | AS 'S32 | RAS 'LS32 | MC68000 Delay (Data Setup and AS Delay) 10 MHz* | 8 MHz | 6 MHz | 4 MHz | Bus Latency Period Required (ns) | Operating Frequencies (MHz) Max, no waits | Operating Frequencies (MHz) Nominal, no waits |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 50 | 4 x 7 | | 7 | | 10 + 50 | | | | 145 | 17 | 16 |
| 100 | 4 x 7 | | 7 | | 10 + 50 | | | | 195 | 12.8 | 12 |
| 150 | 4 x 7 | | 7 | | 10 + 50 | | | | 245 | 10.2 | 10 |
| 200 | 4 x 7 | | 7 | | | 15 + 55 | | | 305 | 8.19 | 8 |
| 200 | | 4 x 14 | | 22 | | 15 + 55 | | | 348 | 7.18 | 7 |
| 250 | 4 x 7 | | 7 | | | 15 + 55 | | | 355 | 7.04 | 7 |
| 250 | | 4 x 14 | | 22 | | | 25 + 65 | | 418 | 5.98 | 6 |
| 300 | | 4 x 14 | | 22 | | | 25 + 65 | | 468 | 5.34 | 5 |
| 350 | | 4 x 14 | | 22 | | | | 30 + 75 | 533 | 4.69 | 4 |
| 400 | | 4 x 14 | | 22 | | | | 30 + 75 | 583 | 4.2 | 4 |
| 450 | | 4 x 14 | | 22 | | | | 30 + 75 | 633 | 3.94 | 3.58 |

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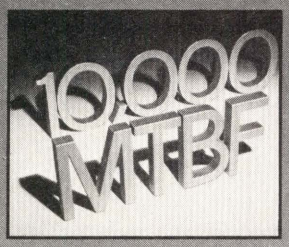


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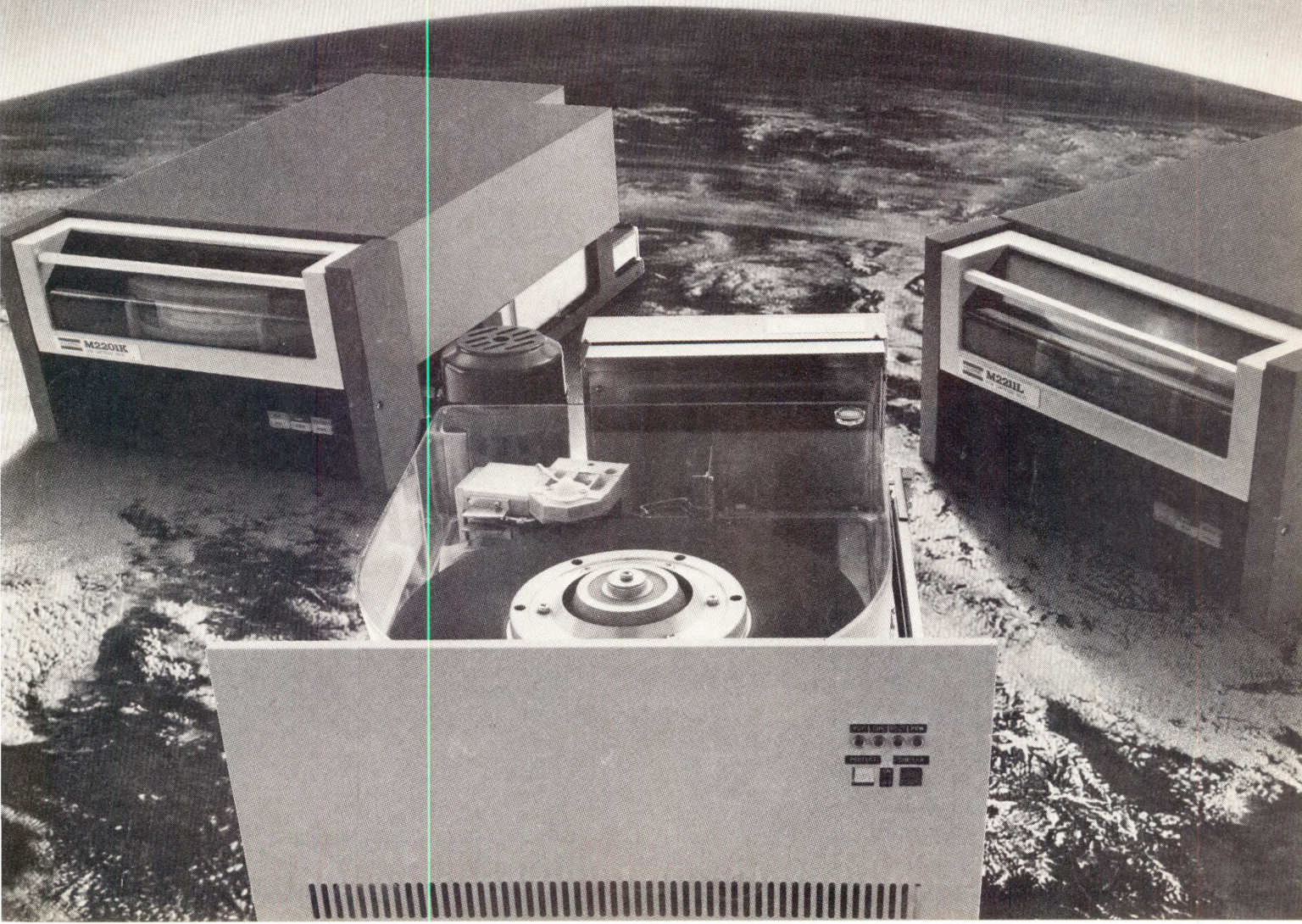

**TABLE 2**

**Operation with LS Buffers and 200 ns RAMs**

| Action | Clock Cycles | Time (ns) | Clock Frequency (MHz) | Performance |
|---|---|---|---|---|
| Instruction sequence (ideal) | 17 | 2125 | 8 | 100% |
| If wait on each read (actual) | 20 | 2500 | 8 | 85% |
| If reduced clock frequency | 17 | 2429 | 7 | 87% |
| If only ½ wait cycle on each read | 18.5 | 2313 | 8 | 92% |

MC68000 delay times are from the latest data sheet showing 4-, 6-, and 8-MHz parameters with projected 10-MHz parameters. When worst-case numbers are used, the resulting bus latency period permits operation at the nominal clock rate shown in the table, provided that no wait states of one full clock period each are to be incurred.

Instruction cycle times from the MC68000 data sheet assume a nominal read cycle time of 4 clock periods, with 2½ periods allocated for bus latency, and a nominal write cycle time of 5 clock periods, with 3½ periods allocated for bus latency. When writing, ample time is available to use the less expensive LS buffers and logic. However, again referring to Table 1, to avoid incurring wait cycles in a typical system with 200-ns RAM and LS buffers, a clock frequency must be selected for which the required 348-ns latency period represents 2½ clock periods (about 7.18 MHz), or else Schottky logic must be used.

In a simple 2-instruction sequence—read data followed by write data—there are four bus accesses of which only one is a write access. This reflects a nominal time period of 17 clock cycles, or 2125 ns at 8 MHz. Table 2 shows the effect of changing the clock period and incurring wait cycles for a particular case, assuming 200-ns RAM in an 8-MHz system, where cost or other considerations require use of LS buffers. If a system uses 200-ns RAM with LS buffers at 8 MHz, reducing the clock frequency to 7 MHz would improve performance. This occurs because, when using these components at 8 MHz, full clock periods are added as wait cycles. Consequently, in the Table 2 example, 250-ns RAM with Schottky buffers could be used instead of the 200-ns RAM to achieve the same 20-cycle instruction sequence period of about 2500 ns.

The last line of Table 2 describes operation if it were possible to add only one half of a cycle for each wait state. Using the previous example of a 2-instruction sequence requiring 17 cycles, the sequence now extends to only 18.5 cycles, instead of 20 cycles, when 200-ns RAM and LS buffers are used in an 8-MHz system.

Although the MC68000 extends bus cycles only in increments of one full clock period, the circuit shown in Fig 2 can be used to stretch S4 by unit periods of the oscillator input to flipflop A. This circuit will not stretch S2, because data strobes are not provided until S3 of a write cycle. Fig 3 clarifies the full impact of this approach by showing the combined interaction between memory access time with associated buffer logic type, microprocessor clock frequency, and the number of wait cycles incurred.

In Fig 3, average execution time per instruction (in microseconds) of the read data, write data sequence appears on the left vertical axis. Lines sloping down and to the left reflect nominal microprocessor clock frequencies. Curves sloping down and to the right are labeled along the right axis according to memory access time (in nanoseconds) and buffer logic type. These curves include both the bus buffer overhead and the microprocessor overhead from Table 1. For each combination of logic type, memory access time, clock frequency, and number of wait cycles, Fig 3 gives the corresponding average instruction execution time.

The numbers in Table 2 were derived from Fig 3 and illustrate its use. For the typical delay parameters in Table 1, the 8.0-MHz clock line crosses the zero wait cycle between its intersection with the contour for Schottky-buffered 200-ns RAM and its intersection with the contour for 200-ns LS-buffered RAM, showing that Schottky-buffered RAM would incur no wait cycles and execute the two instructions in 2.12-μs total time, or 1.06-μs average time on the graph. Using 200-ns RAM with LS buffers incurs a single wait cycle for each access. The two instructions would execute in 2.5-μs total time for an average execution time of 1.25 μs each. However, if the clock stretching circuit of Fig 2

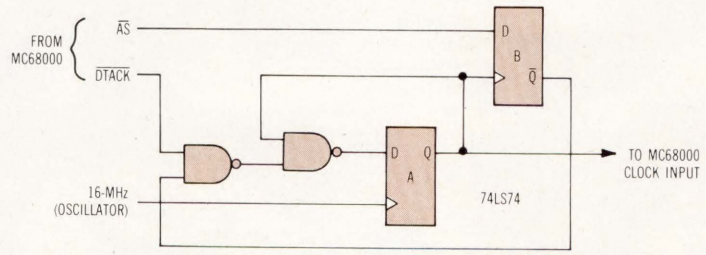


Fig 2 Clock stretching circuit. Although MC68000 adds only full cycles as wait states, this circuit extends S4 by unit periods of flipflop A oscillator input, allowing half cycle wait state and thereby gaining one half of a cycle

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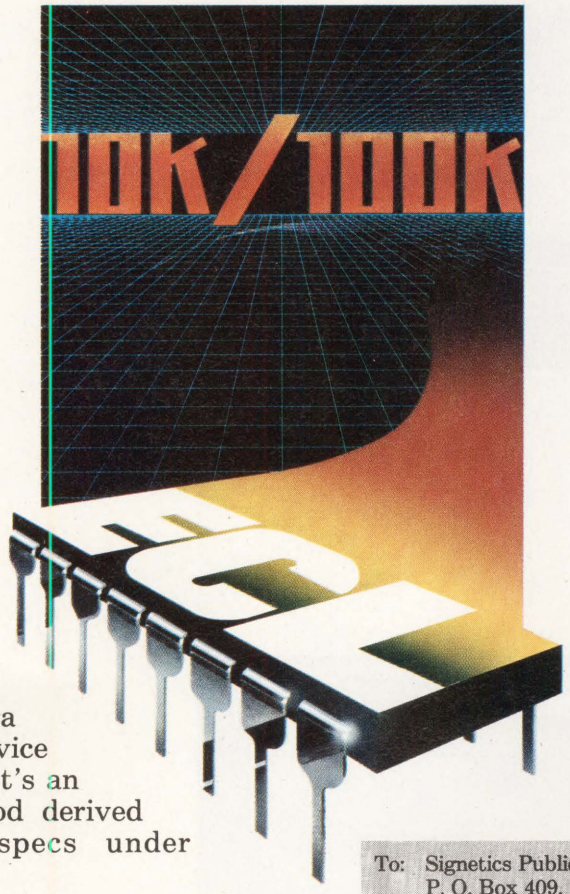


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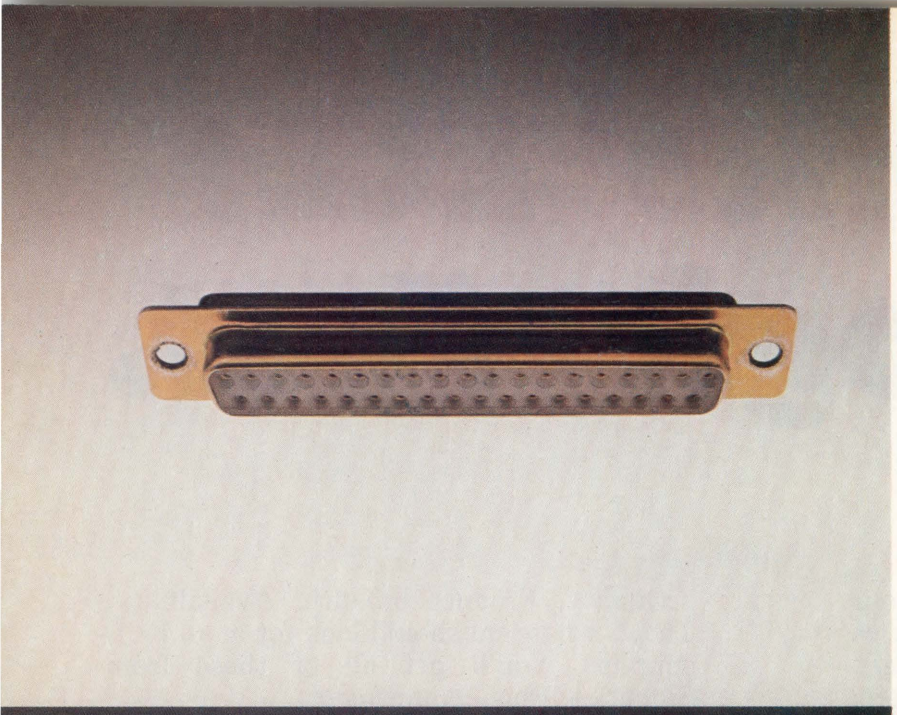

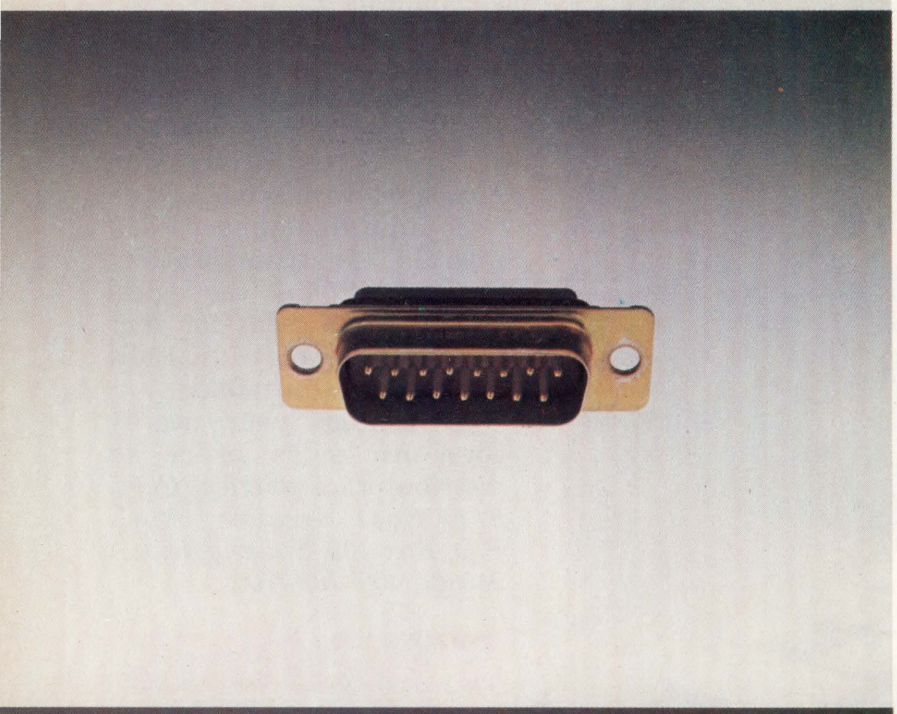

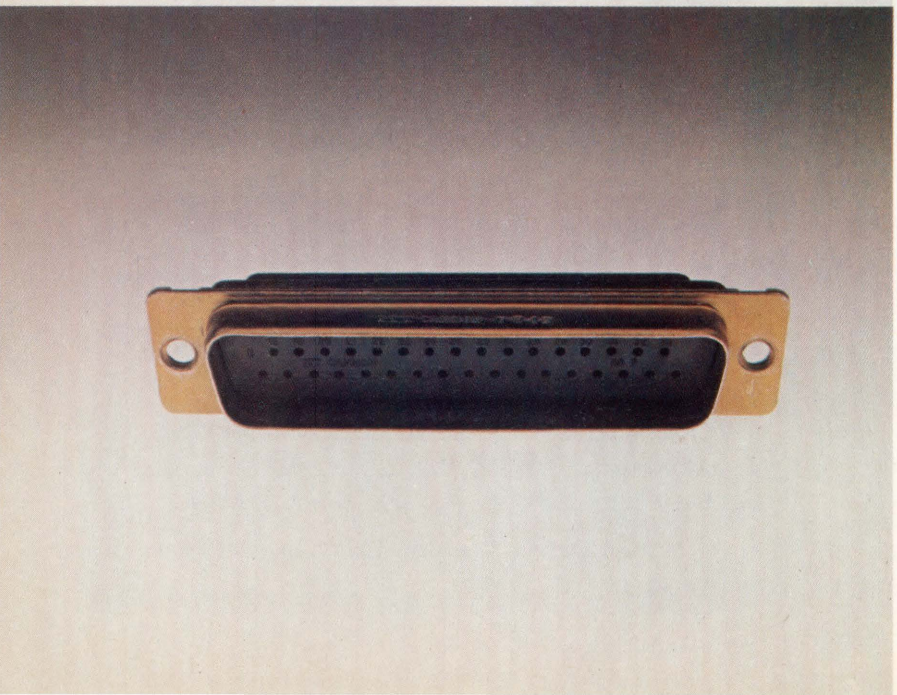

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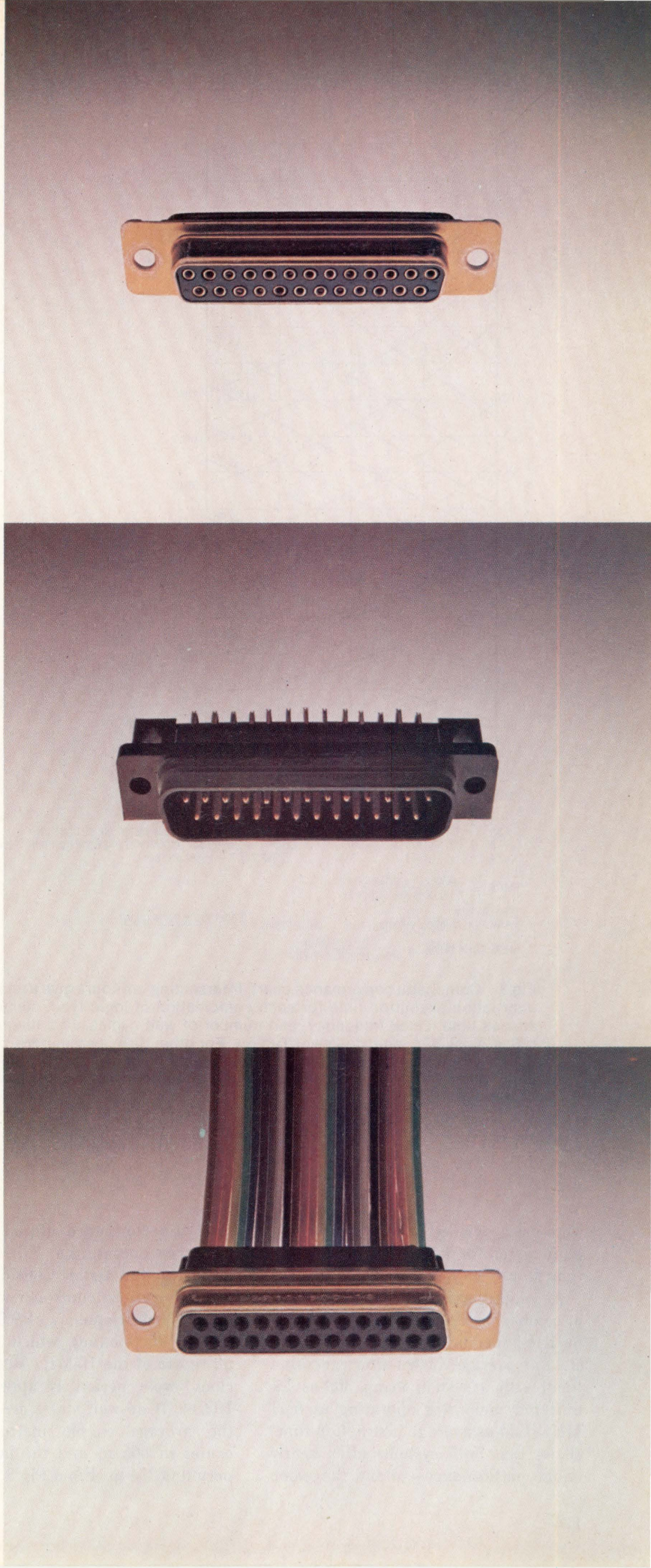

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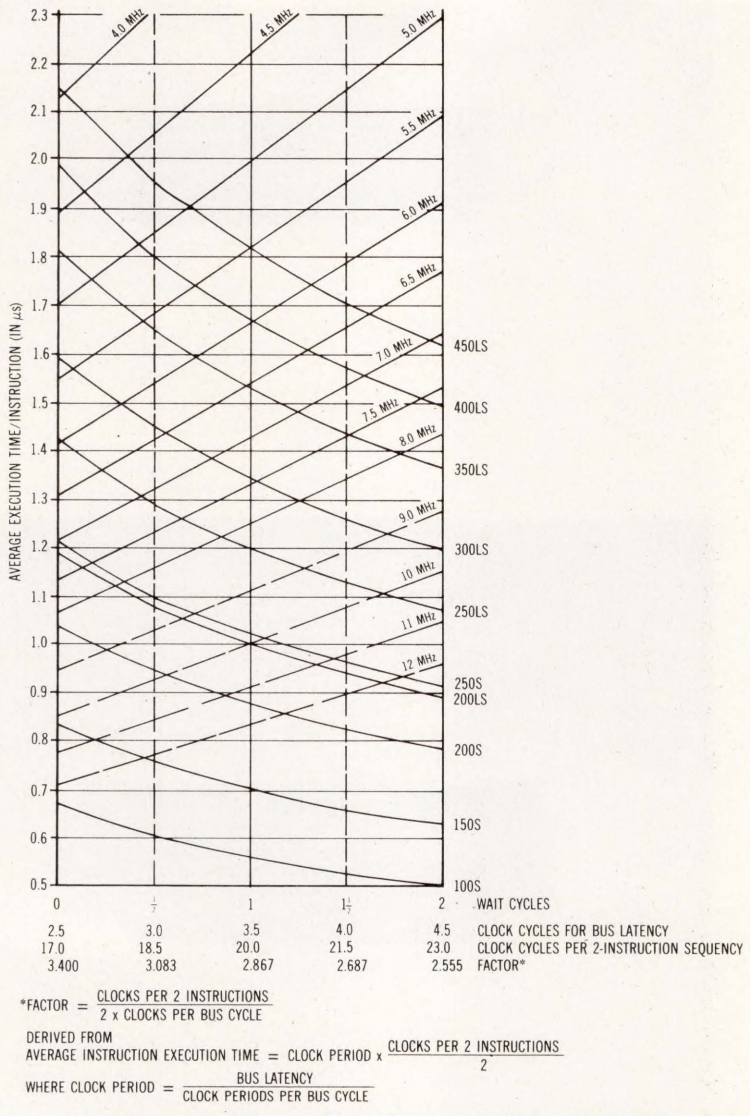


Fig 3 Composite performance chart. Intersecting contours give average instruction execution time for each combination of logic type, memory access time, clock frequency, and number of wait cycles. This diagram reflects specific logic delays of Table 1. For other delay parameters, product of factor on bottom line with total delay (memory access, buffer logic, and microprocessor) gives ordinate of contour sloping downward to the right

were used, only half a wait cycle would be incurred for 1.16-μs average execution time.

As another example of the use of Fig 3, comparing a system with 250-ns LS-buffered memory operating at 6 MHz (1.42-μs average instruction execution time) with a system using 300-ns LS-buffered memories operating at 6.41 MHz (1.44-μs average instruction time) shows that both systems offer nearly equal performance—about the same level of performance offered by 300-ns memories operating at 7.0 MHz (1.43-μs instruction time). Consider a data communications controller with a proposed clock frequency of 9.8304 MHz ($2^{10}$ × 9600 baud), which would require use of the 10-MHz MC68000. The clock cycle period is approximately 102 ns. If no wait states are incurred, the average simple instruction executes in 865 ns and the bus latency period is 254 ns. From Fig 3, Schottky-buffered 150-ns RAM is recommended here. Schottky-buffered 200-ns RAM may be used with the clock stretching circuit of Fig 2 with the resulting average execution time of 941 ns offering nearly 92% of the performance obtained from the faster RAM. Similarly, 250-ns LS-buffered RAM can be used, incurring full wait cycles and an average execution time of 1017 ns, to achieve 85% of the performance offered by the 150-ns RAM.

Different circuit configurations result in different delay times reflected by the Table 1 data used to plot those contours in Fig 3 that slope downward to the right. Factors listed at the bottom of Fig 3 can be used to plot a composite performance chart for any set of delay times. Suppose, for example, the MC68000 system includes a memory management unit. Adding the memory management unit delay to the Table 1 timing values increases the bus latency period. For each combination of access time and logic type, the corresponding new bus latency period multiplied by each of the factors listed in Fig 3 identifies a new crossing on each of the Fig 3 axes.

In any system whose addressable memory even begins to approach the full capacity of the MC68000, the cost of memory far exceeds the cost of the microprocesssor. Therefore, it is the microprocessor and its clock that should be tuned to the memories in use. The cost versus performance tradeoffs discussed here, with the composite performance chart of Fig 3 and the clock stretching circuit of Fig 2, determine which combination of logic type and memory access time offers best performance and allow adjustment of timing parameters to optimize performance of the components used.

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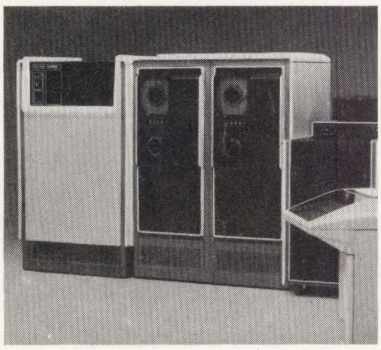

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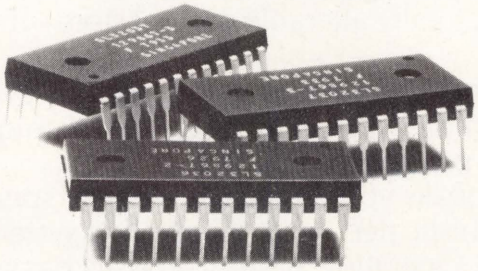

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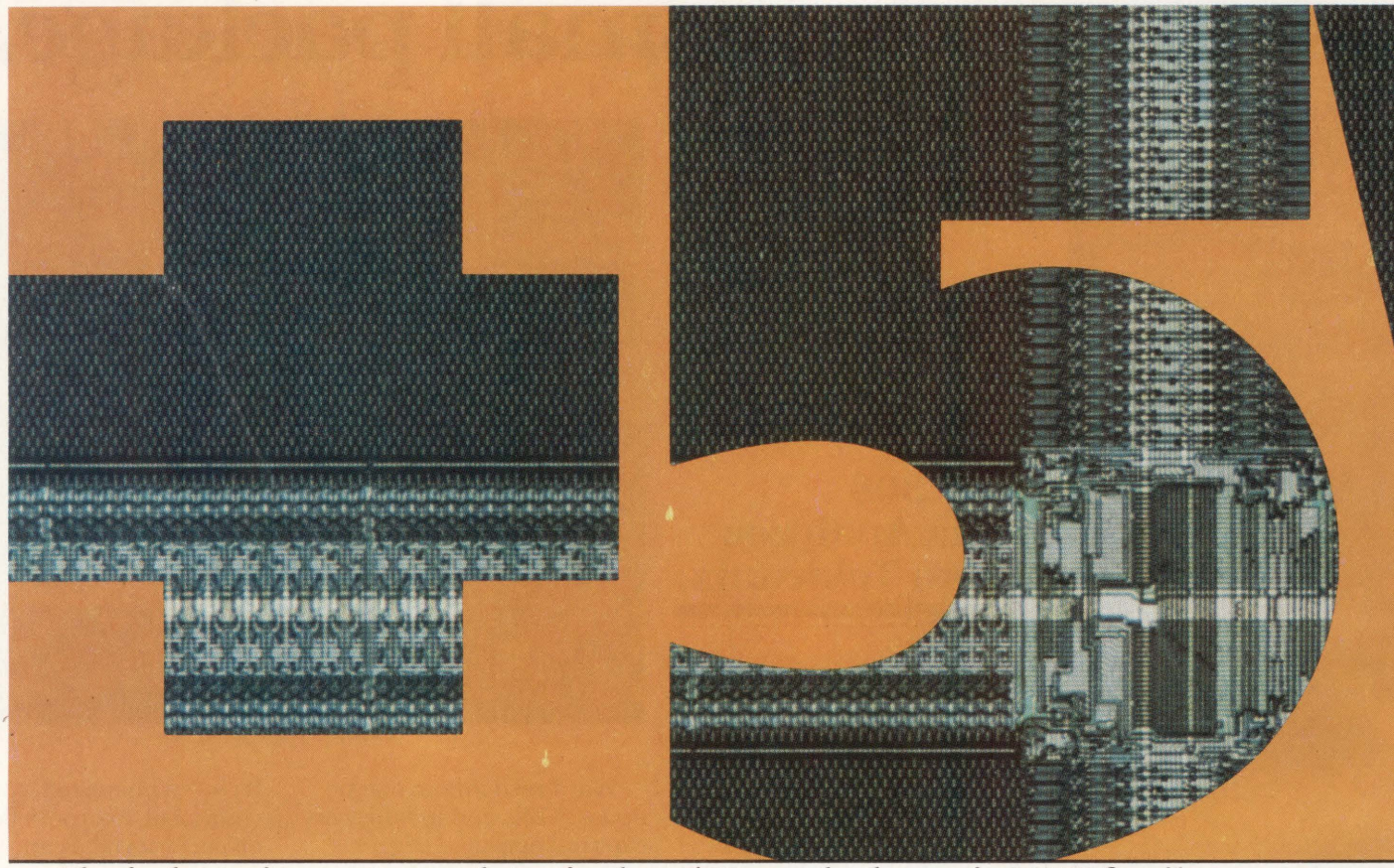


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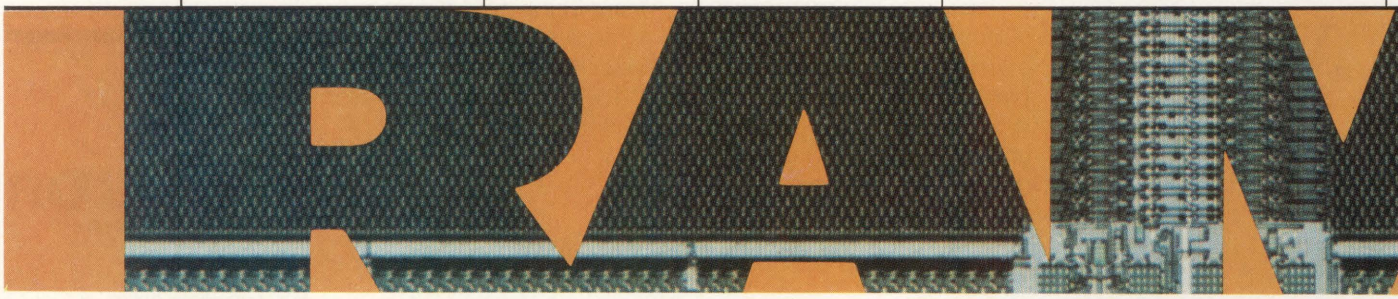
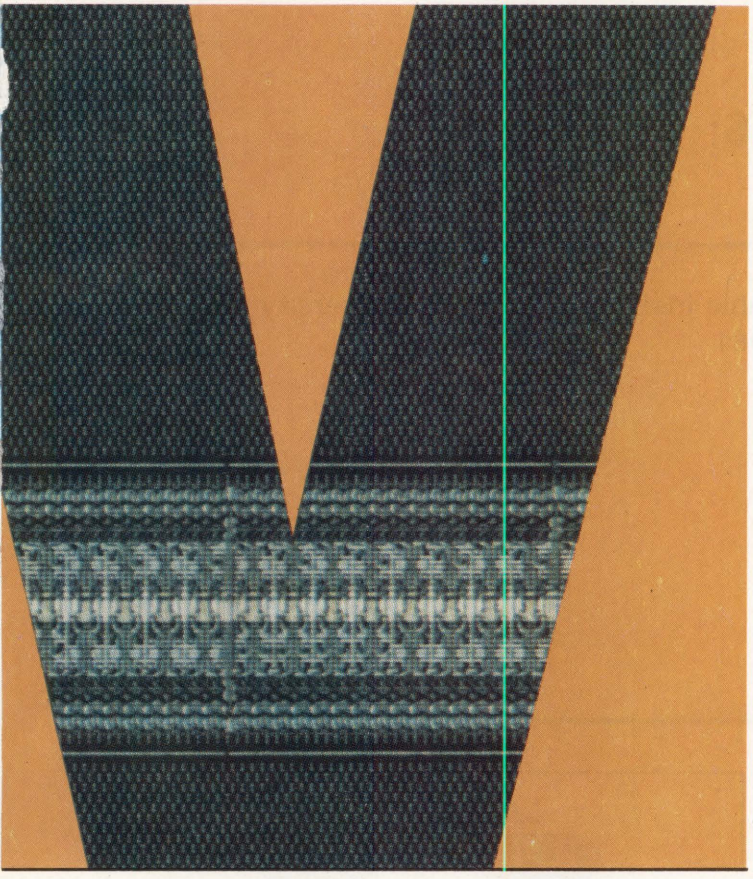
| 32K | MCM6632 | ✓ | +5 V, ±10% | 150, 200 |
| 32K | MCM6633 | – | | |
| 16K | MCM4516 | ✓ | +5 V, ±10% | 120, 150, 200 |
| 16K | MCM4517 | – | | |



# V dynamic RAM family today, from Motorola.



For the first time, a complete family of single-supply +5 V dynamic RAMs from 16K through 64K is available in production quantities. You can get them now, from Motorola.

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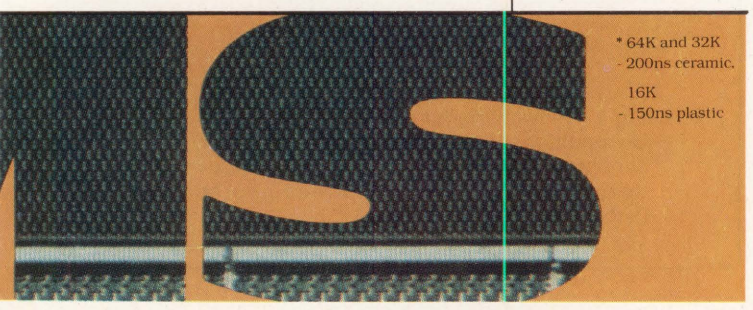

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CIRCLE 54 ON INQUIRY CARD

# INTERFACING FUNDAMENTALS: UNCONDITIONAL I/O

**Peter R. Rony**

Virginia Polytechnic Institute and State University
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In the three preceding columns, microcomputer input/output techniques have been discussed in which either a flag or a semaphore has synchronized data transfer between the microcomputer and the input/output device. Such techniques are referred to as conditional input/output, since the data are transferred only when the flag or semaphore reaches a certain condition, either a high or low state. To complete the comparison of input/output techniques, the simplest one, unconditional input/output, will be discussed. In this technique, data can be transferred at any time, without conditions.

Figs 1 and 2 provide flowcharts and timing diagrams, respectively, for unconditional input of data to a microcomputer. A comparison of the flowcharts with those given in Refs 1 and 2 indicates that no dotted lines are present in Fig 1; there is no communication or synchronization between the input device (source) and the microcomputer (acceptor). The input device is assumed always to be available. The microcomputer, through the use of a software loop or a realtime clock, determines how often the data transfer occurs. In Fig 2, the data to be input may need to be stable for a significant period of time, such as milliseconds or seconds. The rate at which it can change is determined by the nature

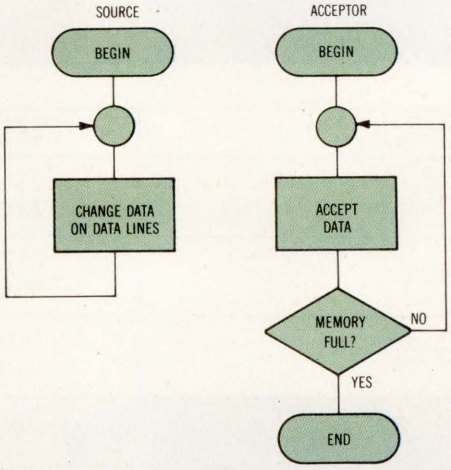
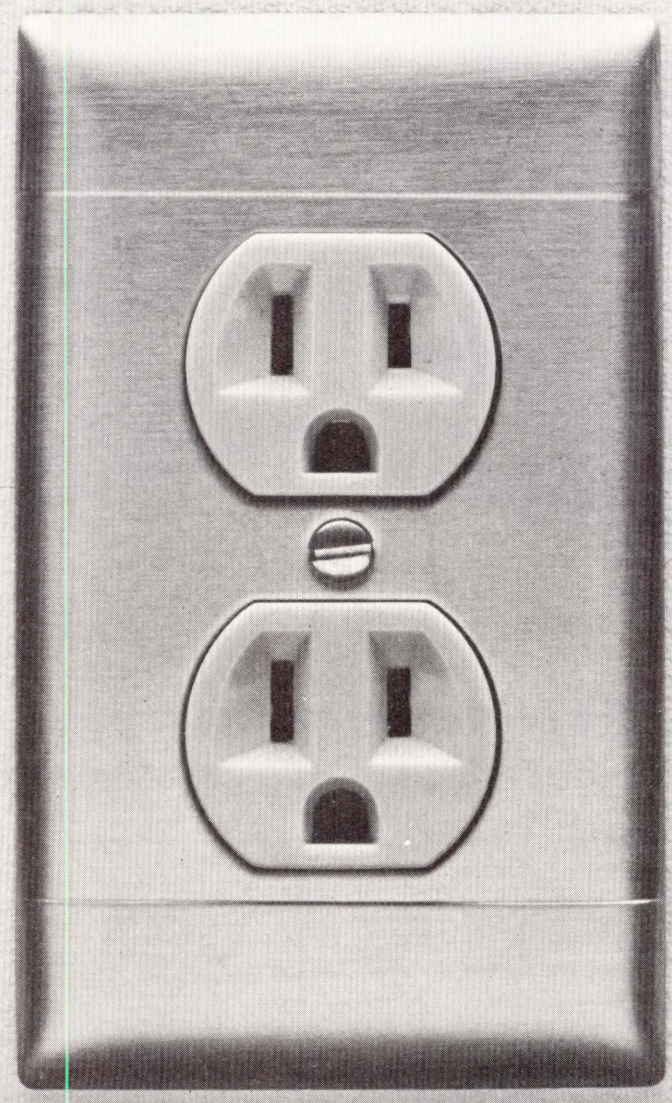



Fig 1 Flowcharts for source and acceptor. Unconditional input. No communication or synchronization occurs between input device (source) and microcomputer (acceptor)



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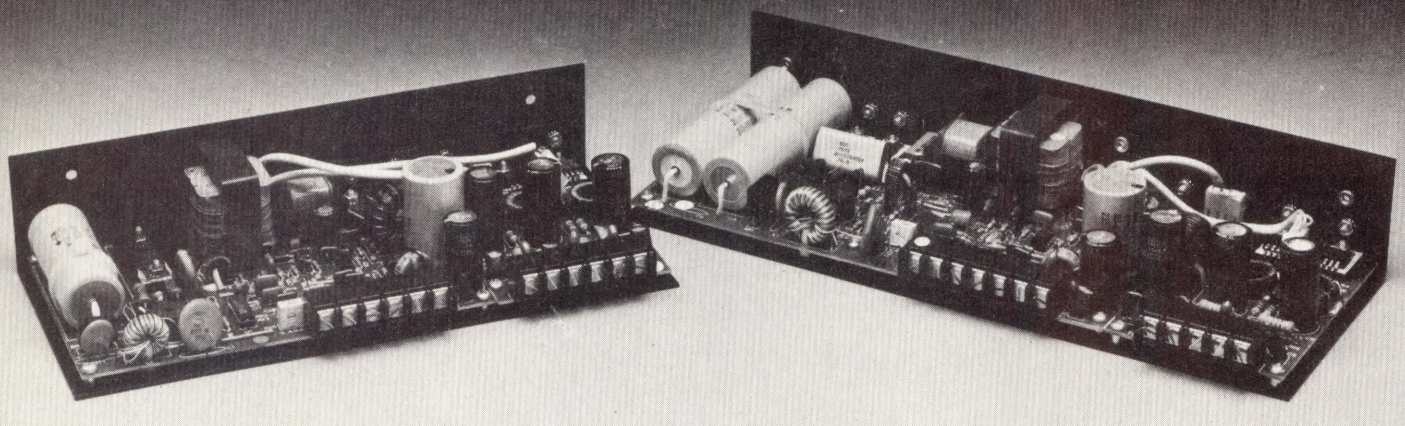

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The LMG line ranges from the single output 75 watt model to the 150 watt four output version. The chart on the right lists output combinations for the full LMG family.

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| | LMG 15-5 | 15-5 | | | |
| | LMGT 75/12 | 5-15 | 12-1 | 12-1 | |
| | LMGT 75/15 | 5-15 | 15-1 | 15-1 | |
| | LMGQ 75/12 | 5-15 | 12-1 | 12-1 | 5-1 |
| | LMGQ 75/15 | 5-15 | 15-1 | 15-1 | 5-1 |
| 150 watts | LMG 5-20 | 5-20 | | | |
| | LMGT 150/12 | 5-20 | 12-3 | 12-3 | |
| | LMGT 150/15 | 5-20 | 15-2.4 | 15-2.4 | |
| | LMGT 150/24 | 5-20 | 24-1.5 | 5-1 | |
| | LMGQ 150/12 | 5-20 | 12-3 | 12-3 | 5-1 |
| | LMGQ 150/15 | 5-20 | 15-2.4 | 15-2.4 | 5-1 |
| | LMGQ 150/24/12 | 5-20 | 12-1 | 12-1 | 24-1.7 |

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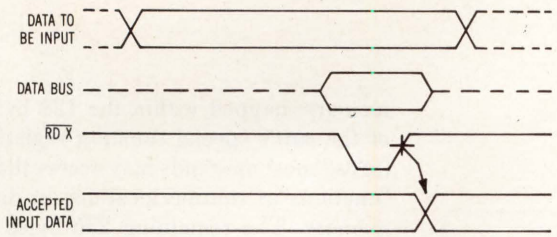



Fig 2 Timing diagrams for unconditional input. Because there is no synchronization between source and acceptor, data may be required to remain stable for a significant period of time

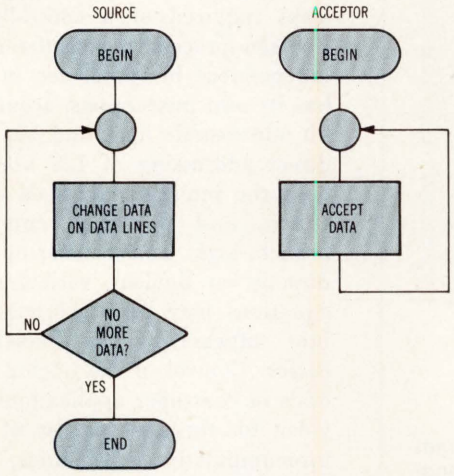



Fig 3 Flowcharts for source and acceptor. Unconditional output. Just as in unconditional input, data from the output device are assumed to be always available

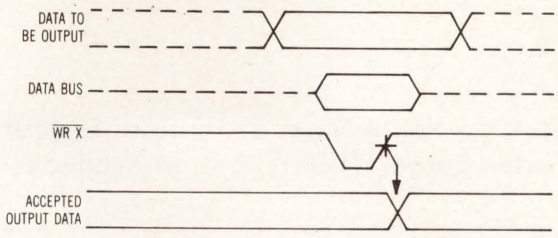



Fig 4 Timing diagrams for unconditional output. Microcomputer software loop or realtime clock determine when data transfer occurs between source and acceptor

**Summary of Flipflop Behavior**

| Type of I/O Technique | Sets Flipflop | Resets Flipflop | Tests Flipflop |
|---|---|---|---|
| Conditional (semaphore) | Source | Acceptor | Source and acceptor |
| Conditional (flag) input | Source | Acceptor | Only acceptor |
| Conditional (flag) output | Source | Acceptor | Only source |
| Unconditional | Neither | Neither | Neither |

of the input device, the repetition rate associated with the input and processing of new data, and whether every new data point needs to be input and processed.

Figs 3 and 4 are the analogous flowcharts and timing diagrams, respectively, for unconditional output of data from a microcomputer. Again, a comparison of these flowcharts with those given in Refs 1 and 3 indicates that no dotted lines are present in Fig 3; consequently, there is no communication or synchronization between the microcomputer (source) and the output device (acceptor). The output device is assumed always to be available, just as is the input device in Fig 1. The microcomputer determines how often the data transfer occurs.

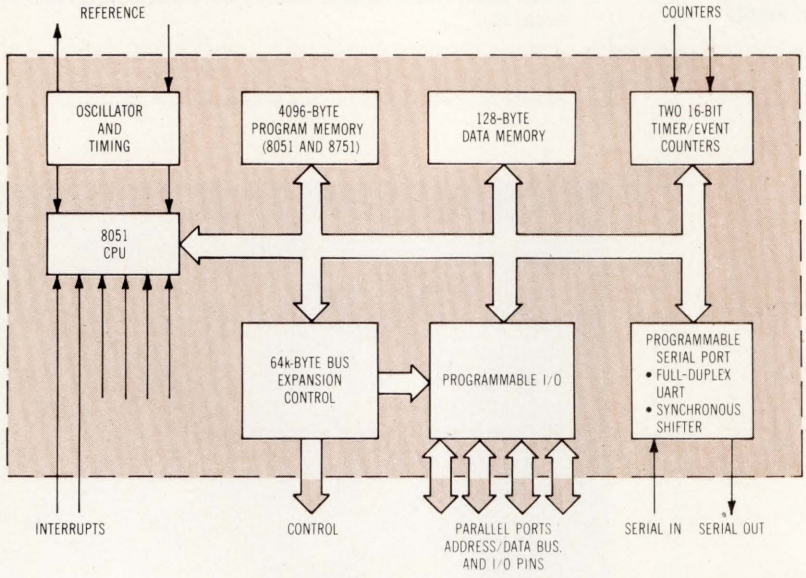
In unconditional input/output (I/O), the peripheral can be said to be dumb in that it does not influence the timing of the data transfer in any way. The microcomputer does not need or request confirmation that the I/O device is operating. When the I/O device operates continuously and relatively slowly, unconditional I/O techniques are acceptable. When the peripheral operates at sporadic time intervals, the use of a flag is more appropriate since it frees the microcomputer to direct its attention to other tasks.

The Table summarizes the behavior of the flipflop, whether flag or semaphore, for three different I/O techniques: conditional I/O with semaphore, conditional I/O with flag, and unconditional I/O. The distinction between the techniques is the presence or absence of the flipflop, and whether both source and acceptor test it.

## References

1. P. R. Rony, "Interfacing Fundamentals: Conditional I/O Using a Semaphore," *Computer Design,* Apr 1980, pp 166-167
2. P. R. Rony, "Interfacing Fundamentals: Conditional Input Using a Flag,"*Computer Design,* May 1980, p 208
3. P. R. Rony, "Interfacing Fundamentals: Conditional Output Using a Flag," *Computer Design,* June 1980, p 132

## Single-Chip HMOS Microcomputers Execute Programs 16 Times Larger Than Those of Predecessor




Intel's 8051 family single-chip 8-bit microcomputer architecture. Program memory capabilities differentiate between 8031, 8051, and 8751. 8051 is intended for use in realtime applications such as instrumentation, industrial control, and intelligent computer peripherals

Three high performance single-chip microcomputers, fabricated with n-channel HMOS technology, meet the power and cost effectiveness requirements of applications needing up to 64k bytes of program memory and/or up to 64k bytes of data storage. Each has more than 100k bytes of memory address space, a serial communications port, and several onchip peripherals.

Program memory is the only differentiating feature of the three devices introduced by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. The 8051 has 4k bytes of mask programmable ROM and the 8751 has 4k bytes of EPROM, while the 8031 has no onchip memory and is intended for applications where external program memory is provided.

The 8051, the key product in the family, executes programs up to 16 times larger than the largest possible with its 8048 predecessor. Although classified as an 8-bit processor, the 8051 can operate on 16-bit words, 4-bit nibbles, and 1-bit data.

Internal memory, arithmetic logic unit, and external data bus are designed to operate using 8-bit words; however, the word length flexibility permits a variety of data formats and independent control of individual output lines.

Since the arithmetic registers, pointers, I/O ports, interrupt system registers, timers, and serial port are memory mapped within the 128 bytes of the 8051's special function registers (SFRs), most operands may access these functions as routine locations in data memory. The remaining 256 bytes of internal data memory are data RAM, which contains four 8-register banks, 128 addressable bits, and a stack depth limited only by the amount of RAM available.

Because of its ability to function as a Boolean processor and a byte processor, the 8051 can perform better the tasks required of a controller. The Boolean processor, considered as an independent bit processor in that it has its own instructions, accumulator, bit addressable RAM, and I/O, permits direct addressing of 128 bits within both the internal data RAM and SFR space, and performs conditional branch, logic, and transfer operations directly on Boolean variables. Logic equations may be converted directly into software by the Boolean processor. Control of the onchip peripherals in controller applications is provided for through the use of special bit-manipulation instructions.

The 32 I/O lines available on the 8051 may be addressed as individual bits or as 4 parallel 8-bit ports. To expand program and/or data memory with external chips, low order addresses are sent out through one 8-bit port, and high order addresses are sent out through another port. The low order address port also acts as the interface between peripheral devices or external memory and the 8051. A serial communications port located on the 8051 permits 31,250-baud asynchronous data transmission and 1M-bit/s synchronous capability.

8051 interrupts occur through an assigned priority level interrupt scheme consisting of three internal and two external sources. Each interrupt source can be independently enabled and disabled.

Two 16-bit counters can be programmed independently to operate in 3 modes: an 8-bit timer with 8-bit prescaler or counter, a 16-bit time interval/event counter, or an 8-bit time-interval/event counter with automatic reload upon overflow. Frequency

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## Intel's new 8272 controller for double density floppy disks lets you command shorter design times.

Why have second thoughts about designing a double density floppy disk drive into your system, when Intel's 8272 is available now. With a powerful command set, microprocessor compatibility, Intel's HMOS* technology and the ability to reduce CPU overhead, our controller for IBM compatible single or double density floppy disks is the logical choice for system designers.

Now, you don't have to spend months building and programming an entire board of interface logic to control one, two, three or four double density floppy disk drives. Just incorporate Intel's new 8272 controller into your design to save time and space. Our double density floppy disk controller does more than reduce your parts count 50 to 1. It gives you enough flexibility to shorten your design cycle. And Intel's 8272 offers you the freedom of designing in the 5-volt world.

### Freedom for the CPU.

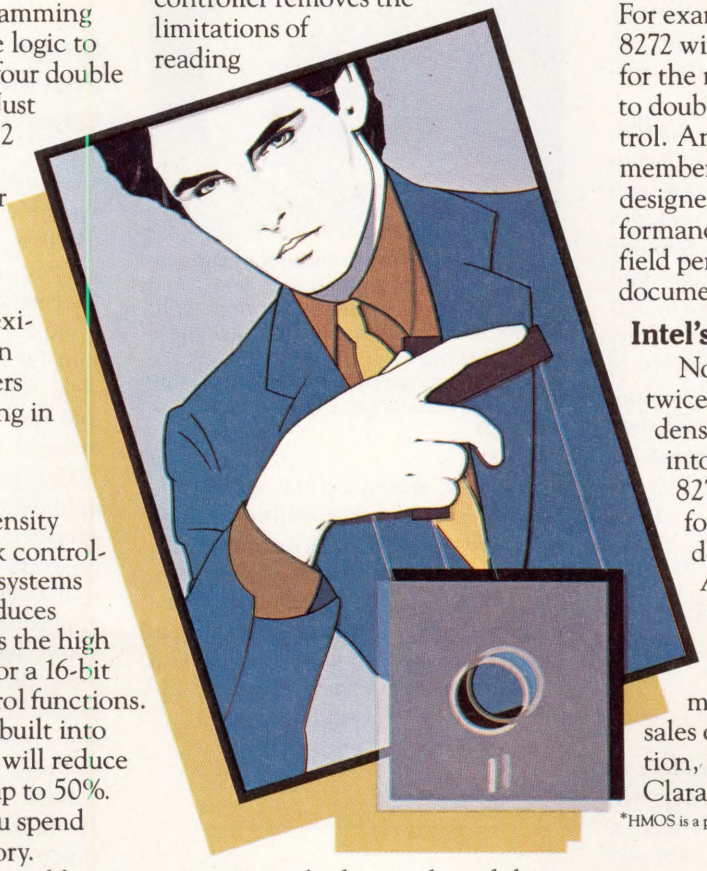
Our new 8272 double density floppy and mini-floppy disk controller is the right solution for systems designers. It saves time, reduces power dissipation and slices the high cost of burdening an 8-bit or a 16-bit CPU with floppy disk control functions. A powerful instruction set built into Intel's new 8272 controller will reduce your programming efforts up to 50%. Less code is required, so you spend less time and use less memory.

Intel's 8272 solution also tackles the problem of CPU overhead and software intervention. Our double density floppy disk controller has the capability of scanning a single sector or an entire track's worth of data fields. Data on the floppy disk gets compared byte-by-byte with data in your system memory. And, since a single command locates and compares the data, no additional software is necessary.

### Faster data access.

Our new 8272 controller does more than drive up to four floppy disks simultaneously. It handles parallel seek on up to four disks for faster data access.

With multi-sector and multi-track transfer capabilities, the CPU is freed from time-consuming I/O commands. Our new double density floppy disk controller removes the limitations of reading or writing only the number of characters a physical sector allows. The 8272 automatically transfers data across the disk's consecutive sectors... and, as a result, the CPU isn't forced to wait until the next sector is positioned. With Intel's new 8272, you not only free the CPU, you get the assurance of higher system performance.



### Easy microprocessor compatibility.

Intel delivers the new 8272 double density floppy disk controller into the 5-volt world. That makes our controller an easy, compatible interface with Intel's family of microprocessors like our 8086, 8088 and 8085.

As part of the Intel peripheral family, the new 8272 complements our other dedicated LSI performers. For example, you can team our 8272 with an 8237 DMA controller for the most bus-efficient solution to double density floppy disk control. And like our other family members, the 8272 offers systems designers highly reliable performance... plus the support of field personnel and complete documentation.

### Intel's new 8272, here today.

Now, you don't have to think twice about designing a double density floppy disk controller into your system. With Intel's 8272, you won't have to settle for fewer features or a long design cycle, either. Why wait. Already second sourced, our 8272 is on your distributor's shelves today.

For more detailed information, contact your local Intel sales office or write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051.

*HMOS is a patented Intel process.

intel® delivers solutions.

Europe: Intel International, Brussels, Belgium.
Japan: Intel Japan, Tokyo. United States and Canadian distributors: Alliance, Almac/Stroum, Arrow Electronics, Avnet Electronics, Component Specialties, Hamilton/Avnet, Hamilton/Electro Sales, Harvey, Industrial Components, Pioneer, L.A. Varah, Wyle Distribution Group, Zentronics.

CIRCLE 59 ON INQUIRY CARD

capabilities of the counters are 0 to 0.5 MHz from external inputs and 0.1 to 1.0 MHz when programmed for internal oscillator input.

An absolute assembler, the ASM-51, can be loaded into an Intellec™ development system to permit the user to write mnemonic assembly level programs and to have these automatically converted to machine level code. CONV-51, a conversion program, converts assembly level 8048 source code into an 8051 equivalent. A realtime simulation module, the ICE-51, operating at 12 MHz, is available to assist in development debugging of hardware and software for any of the 8051 family chips.

Multiply, divide, subtract with borrow, and compare instructions are new to the 8051 family. An unsigned 8-bit by 8-bit multiply or divide can be executed in 4 $\mu$s; most instructions execute in 1 $\mu$s.

Supporting the expanded capabilities of the 8051 family, 8048 single-chip microcomputers being produced with HMOS technology offer advantages over the previous NMOS technology versions. The 8-MHz 8048H and 11-MHz 8048-1 provide increases in performance of 33 and 80%, respectively. Power consumption is reduced from 675 mW to 400 mW, and all existing 8048 hardware and software are directly compatible with the HMOS chips.

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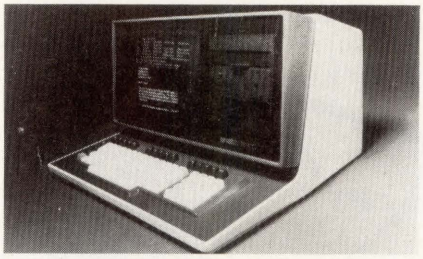
## Desktop Computer System Features Software Flexibility

The Z80 based System 10, a product of Gnat Computers, Inc, 7895 Convoy Ct, Bldg 6, San Diego, CA 92111, utilizes a screen editor, assembler, and CP/M version 2 disc operating system along with optional supporting software, including BASIC, FORTRAN, Pascal, and COBOL. Also included are 65k bytes of RAM, 700k bytes of dual-density, double-sided disc storage, a hard disc interface, DMA and interrupt controllers, and 3 serial I/O channels, 2 RS-232 and 1 IRS-449.

Directed toward small business data processing, word processing, office automation, and mainframe computer intelligent terminal applications, the system may be optionally configured with a 9511/9512 arithmetic processor and an IEEE-448 bus interface. Video display is provided by a 12″ (30-cm) CRT arranged in an 80 x 25 format with 8 x 12 dot matrix characters. A Selectric style keyboard includes an accounting keypad and 10 programmable function keys. All keys utilize capacitive action. The CRT is controlled by a separate microprocessor on the video board, which also handles keyboard data and graphics capabilities.

A power sense read/write protect circuit allows diskettes to remain in the drives during power application and removal and the high speed, hard disc interface provides for up to 80M bytes



System 10 desktop computer system includes monitor, diagnostics, and CP/M disc operating system. Optional software for word processing, accounts receivable/payable, payroll and cost accounting, and general ledger is available in BASIC, FORTRAN, COBOL, Pascal, C, and PL/1

of external storage. SDLC, HDLC, and BISYNC protocol capabilities, along with software-selectable baud rates for printer and modem interfacing provide for a variety of extended communication applications. The switching power supply is rfi filtered and enclosed in the system's 21 x 21 x 13″ (53 x 53 x 33-cm) cabinet.

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## Mass Storage System Uses Hard/Floppy Disc Combination

Up to 2900 separate files may be created using the GenRad/Futuredata (5730 Buckingham Pky, Culver City, CA 90230) 2303 mass storage system. Composed of a microprocessor controlled 35M-byte Winchester type hard disc and a 1M-byte single-sided, double-density floppy, the system provides 512 hard disc and 128 floppy disc byte sectors.

Designed for use with the 2300/2301 universal development systems and fully compatible with all existing systems, the mass storage system also has available a hard disc expansion unit which increases storage capacity to 70M bytes. Other floppy disc units may be driven by either of the controllers in the combination unit or expansion unit.

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## Single-Station System Provides Local Network Capability Option

Designed as 3 standalone entry-level systems, the 4-MHz, Z80A based, 64k-byte MCZ-2 series combines multitasking software and hardware advancements to provide expandability toward a local network capability option for multistation and multiprocessing functions. Packaging, memory, and system options denote differences between models.

Concurrent processing breaks down applications into modular tasks to be executed simultaneously. A special program allows users to supply their own operating system for specialized applications. Concurrent processing allows users to solve multiuser problems through Z-Net, an expandable networking system. Z-Net users can share peripherals and data base while utilizing dedicated CPUs.

Each system produced by Zilog, 10340 Bubb Rd, Cupertino, CA 95014, supports up to 5 asynchronous lines. Interface programs for devices with RS-232, 20-mA protocols may reside in the system. The MCZ-2 series incorporates multiterminal COBOL to facilitate MCZ-1 disc file and applications program transferral. Additional languages available for the single-terminal mode are BASIC and PLZ.

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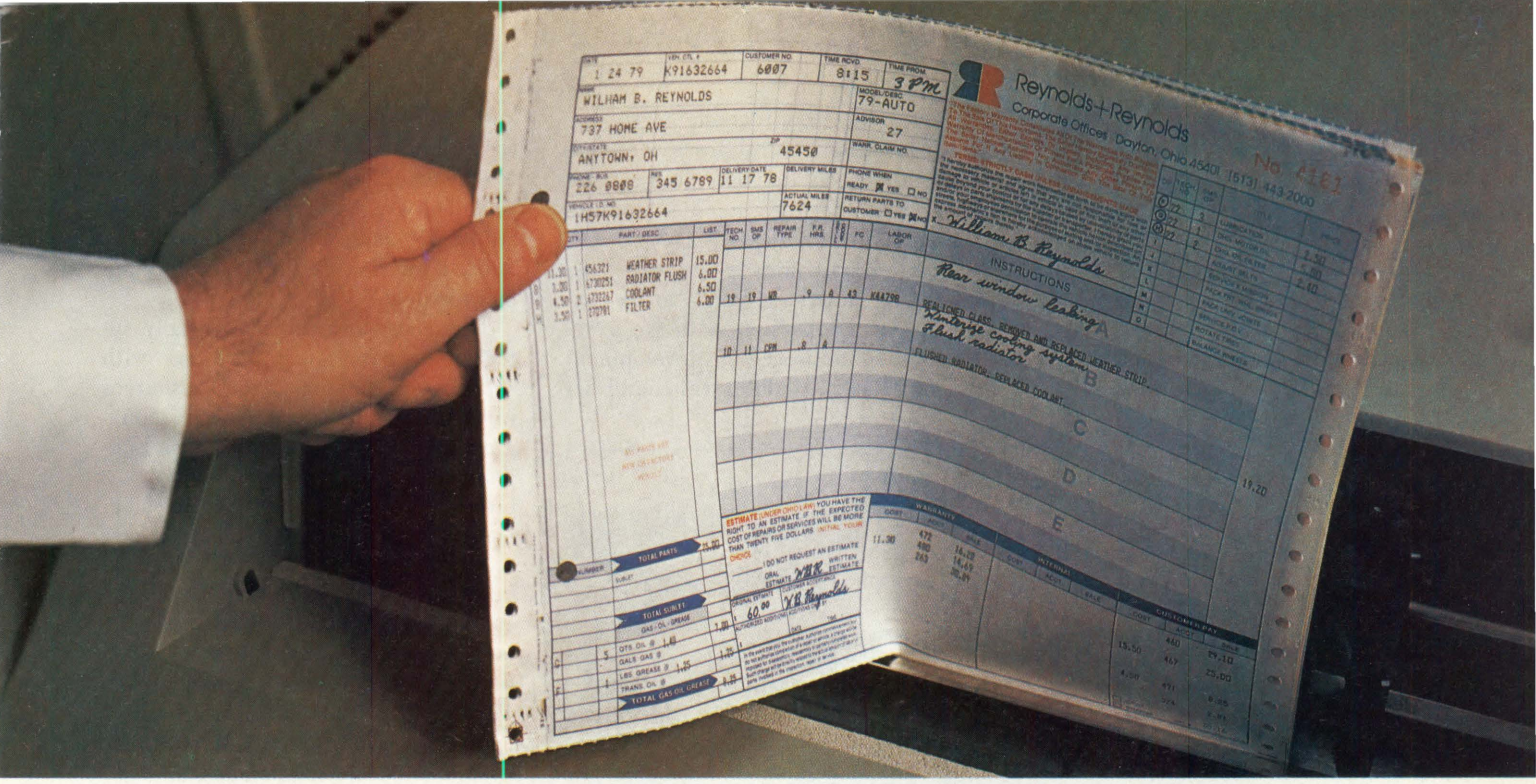


**Push-n-pull tractors, adjustable tear bar and 1-to-9 part forms handling: all in one printer.**

# Great rip-offs: Just one way TermiNet® 200 printers give you no-waste forms access

Finally, real-time forms access plus continuous forms output in one printer. Perfect for such applications as airline ticketing, invoicing, order preparation and more. And another example of the expanding TermiNet 200 printer family's application versatility.

## No-waste, flexible forms control

One reason: an adjustable tear bar that lets you use standard forms with different header lengths. For precise alignment, no paper waste and clean paper tear. Every time.

More reasons: servo-driven tractors that allow infinite manual adjustment in both forward and reverse. A non-volatile electronic VFU that makes forms set-up easy and permits storage of up to 8 vertical formats. A down-line loading option enabling you to load formats directly from your data source. Plus straight-through paper path and push-n-pull tractors that give you perfect first-to-last-copy registration. As well as smoother paper handling for all types of forms, including single-part paper.

## More features add up to more application versatility

With TermiNet 200 printers, you can also get a 9 x 9 printhead for exceptionally legible underlining and lowercase descenders. Two complete 96-character switchable print fonts for ASCII/APL use or your own special needs. A choice of Magnetic Tape or Edit Buffer Accessory. Plus a 100% duty cycle capability, excellent print quality at speeds up to 200 cps and low cost of ownership. All of which help make TermiNet 200 teleprinters and line printers the industry workhorses.

## Immediate delivery instead of piecemeal allocation

Why wait months for other printers when TermiNet 200 printers are available now? When you need them. Mail the coupon today and find out how the expanding TermiNet 200 printer family can meet your range of application needs and generate real cost savings.

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**MICRO DATA STACK**
COMPUTERS, ELEMENTS, AND SYSTEMS

## Emulator Subsystem Supports Hardware and Software Development

Operating in single or multiple in-circuit emulator environments, the RTE8/8800 in circuit emulator subsystem consists of control processor, communications, and debug boards, and also a realtime trace module. Modules for emulation of the 9080A/8080A, 8085, 8048, and Z80 families are added by the user. The subsystem can also be configured as a subsystem with the SYS29 bit-slice microprocessor development system. Basic emulator command set and CRT format are fixed, and only instruction set and internal CPU register for the emulated microprocessors vary. Included are 8k bytes of user mappable, 150-ns access time RAM and an RS-232-C interface to the SYS8/8 development system.

The emulator can sequentially integrate target system hardware with software by mapping SYS8/8 resources into the target system; system debugging can occur in small steps. Full-duplex, asynchronous, serial RS-232-C interface between the host development system and the emulator occurs at a user selectable rate of up to 9600 baud. The user can employ the emulator's 8k-byte RAM in place of the target system's RAM, P/ROM, or ROM. Because the emulation subsystem from Advanced Micro Computers, 3340 Scott Blvd, Santa Clara, CA 95051, has its own separate control microprocessor and ROM, it is capable of independent operation once emulation is initiated under the emulation control program. This operation continues until a specified event or condition occurs. Emulation commands include 23 instructions.

Emulators can be combined with several microprocessors to perform realtime, multiprecision emulation in which the emulators operate simultaneously and independently. External trigger output jacks and internal trace leads permit interaction between subsystems. Independent operation is provided for by a single host command which stores all pertinent data in a specified file and relinquishes control to the emulator system. The host system can then operate on other tasks.

While the emulator subsystem executes a user program in realtime, the trace module stores the last 128 steps of selected bus operations such as executed instructions, program counter, data and status lines, or external data bits. When a specified breakpoint condition occurs and emulation stops, the data collected in trace memory provides a detailed history of bus activity.

To define a value or trace an event, up to eight external TTL threshold probes may be used. A general purpose hardware counter (up to 64k) can measure elapsed time, specific events, or other system parameters before realtime tracing begins and/or stops.

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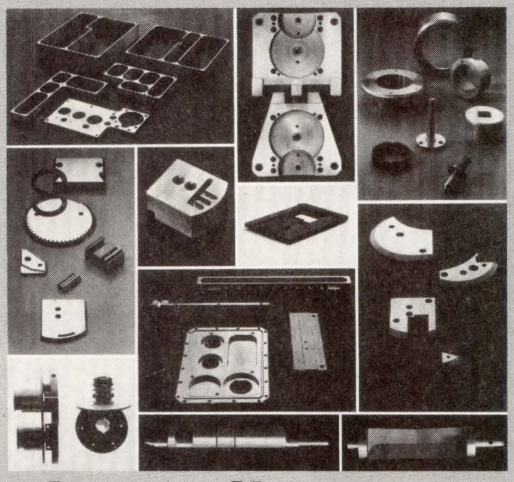

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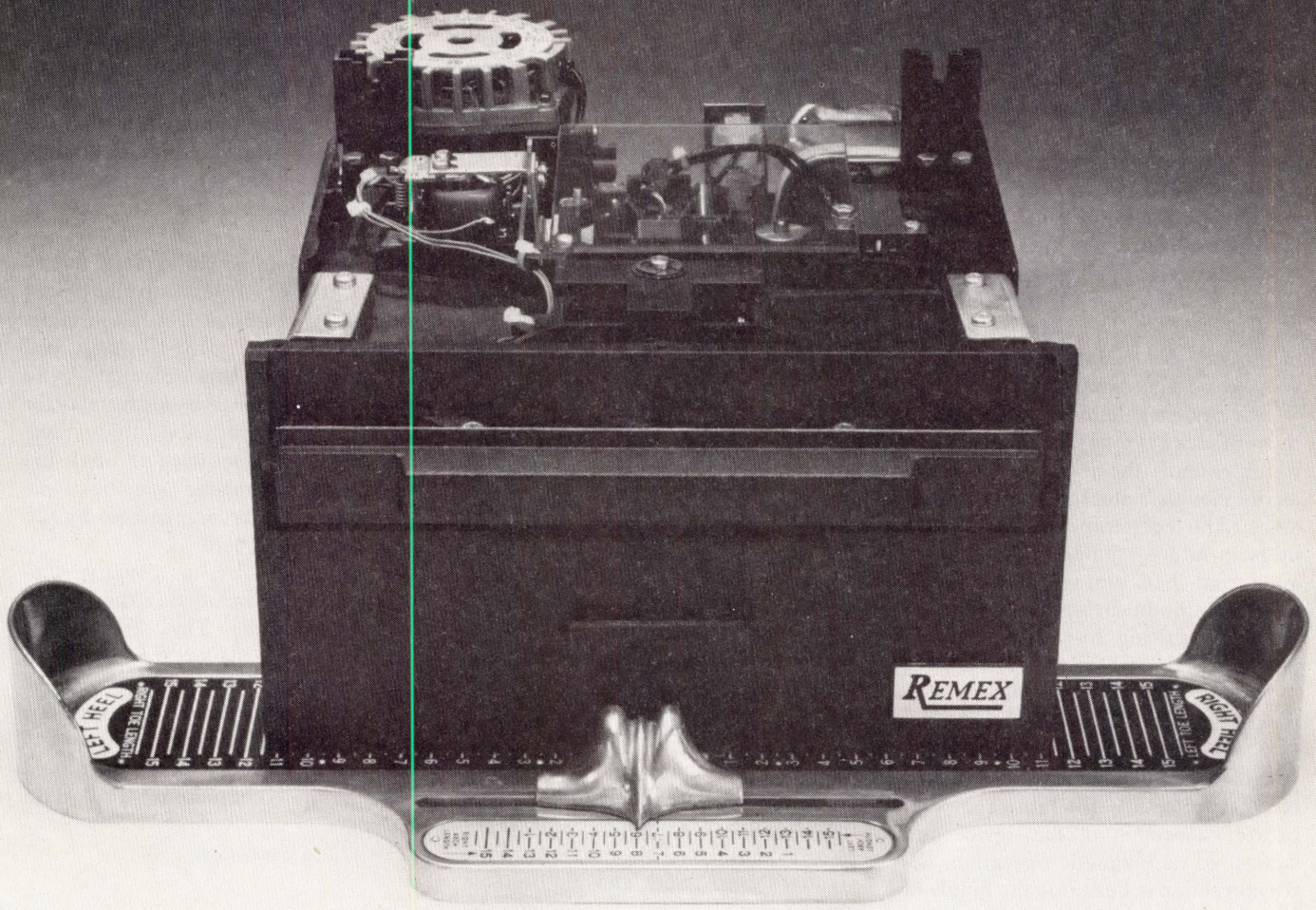


If you've taken a shine to Shugart, you're in luck.

Specifying Shugart means you're also specifying Remex. We're your alternate source for fast, volume delivery.

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What's more, Remex has solved the dual-head media wear problem for good with a new, improved head and carriage assembly.

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**REMEX DIVISION**

DATA WAREHOUSE

**CIRCLE 62 ON INQUIRY CARD**

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

## 70 °C Nonvolatile Storage Increases Applications Of Bubble Memory Device

Along with the extremely high storage density available through bubble memory technology, nonvolatility is the chief advantage of this technique. Available from Intel Magnetics, 3000 Oakmead Village Dr, Santa Clara, CA 95051, the 7110-1 1M-bit bubble memory device extends the upper nonvolatile storage capability from 50 to 70 °C. System reliability increases are due primarily to a design enhancement which extends the temperature range of the module's storage and bootstrap loops. The bootstrap loop is used as both an address index and a map of good and bad storage locations. A lower amplitude current pulse requirement for writing has also been implemented.

Support components, which include the 7220 bubble memory controller, the 7442 formatter and sense amplifier, the 7230 current pulse generator, and 7250 coil predriver are LSI fabricated and provide accessing of the device and control of its magnetic operation. Error correction is built into the family of bubble memory components which provide four 256k subsections per device.

Circle 470 on Inquiry Card

## Analog Input System Requires No Additional Interface Components

Contained in an 80-pin quad-inline package, the MP32BG/CG module includes a 12-bit CMOS A-D converter, instrumentation amplifier, input multiplexer for 16 single-ended or 8 differential signals, an address decoder, and control logic. The device interfaces directly with 8080A, 8048, Z80, and SC/MP microprocessors to provide a hybrid analog input (±10-V) system. A minimum of external logic is required for interface with other systems, and memory mapping allows simple programming for data acquisition.

Available from Burr-Brown, PO Box 11400, Tucson, AZ 85734, the module's instrumentation amplifier gain can be selected from 1 to 54 dB and is programmed with an external resistor, permitting ±10-mV input ranges. Control logic halts or interrupts the CPU while the conversion takes place and signals when data can be read. Nonlinearity of the device is ±0.0125%.

Use of a successive approximation device offers 40-μs max conversion time and 3-state outputs. A 15-μs max internal time delay between channel selection and start of conversion permits settling, and this delay is sufficient when operated at unity gain. Additional delay selection is external resistor selectable. 4096 memory locations, each with its own address, may be communicated with using 12 address lines.

Circle 471 on Inquiry Card

## 8-Bit D-A Converter Provides Direct Microprocessor Interface

Available in four grades and two package types, the monolithic AD558 features direct microprocessor interface capability. The device utilizes standard chip select and chip enable control signals. Input latches may be made transparent for direct access. Temperature stability over specified ranges holds without user trims.

Requiring 5 to 15 Vdc, the device has pin-selectable output ranges of 0 to 2.55 V in 10-mV steps and 0 to 10 V in 40-mV steps. Internal circuitry provides minimum settling time. A product of Analog Devices, Rt 1, Industrial Park, PO Box 280, Norwood, MA 02062, the device includes bandgap reference, microprocessor interface, output amplifier, and 8-bit D-A converter.

Grades J and K specifications include 0 to 70 °C operating range and 16-pin plastic or hermetically sealed packages. Grades S and T specify −55 to 125 °C operating range and hermetic packaging only, and can meet MIL-STD-883, class B, specifications. Accuracy over specified temperature is ±½ LSB max for J and S grades and ±¼ LSB max for grades K and T.

Circle 472 on Inquiry Card

## Diskette Controller Boards Support up to 4M Bytes of Online Storage

Up to 4M bytes of storage for SBC-80 MULTIBUS™ systems may be interfaced by the ZX-204 diskette controller board. Introduced by Zendex Corp, 6398 Dougherty Rd, Dublin, CA 94566, the board will interface up to four, double-sided, double-density, standard sized drives. Maximum transfer rate is 500k-bits/s.

Composed of an integrated floppy disc controller, DMA controller, data separators, Multibus arbitration logic, and standard, mini-floppy, and Multibus interface circuits, the diskette controller uses IBM formats for soft sectored operation. Additional sector sizes may be utilized through the use of programmable specifications. Write data are precompensated by 125 ns early, late, or zero.

High speed disc to memory comparison scan is included in the 15 controller commands. The 8219 bus arbitration chip places the ZX-204 in equal standing with other SBC-80 bus masters in competing for Multibus control. The DMA provides memory to memory block move capabilities, and I/O channel commands and data transfers.

Circle 473 on Inquiry Card

## Bubble Memory Board Provides 69k Bytes Of Nonvolatile Storage

Model 990-040 bubble memory board utilizes 6 TIB0203 bubble storage devices (92k bits each) to provide 69k bytes of storage capability. Compatible with the TI 990/4, 990/5, 990/10, and 990/12 CRU bus, the board features an access time of 7.5 ms to first byte and 20-W worst-case power consumption.

Available from Digital Interface Systems, Inc, PO Box 1446, Benton Harbor, MI 49022, the half-slot boards plug directly into the computer chassis and may be combined to multiply storage capabilities. The board contains provision for connection to an external load switch. Single-quantity price is $1950.

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# MAKE YOUR DUMB TERMINAL SMART.

*Teach it to talk back.* The SLC-1 Time Machine replies instantly to requests from your computer. It automatically tells it the date and time, enters log-in codes, gives any responses you specify. No changes are required in your operating system. Simply install it in the RS-232 or 20mA current loop serial link that connects your computer and terminal.

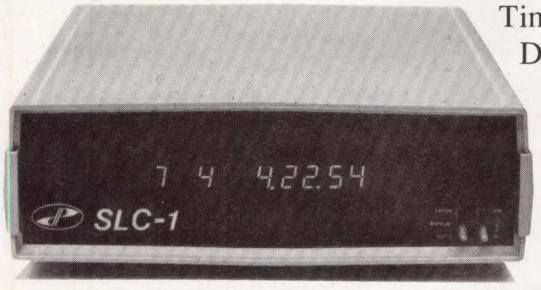
No more operator response errors. No more delays. Now you can automatically re-boot your system after power failure.

Whether you use your computer for business, research, or process control, the Time Machine will save you money. In fact, the first time it prevents a human error, it will more than pay for itself.

The Time Machine doesn't interfere with your computer's operation. It steps in and responds only when it sees the key phrases you have specified. And because it's battery-supported, it never misses a beat or a bit.

The Time Machine comes with a built-in bonus: it is also an independent microprocessor system. Its 1,000 bytes of RAM (expandable to 12K) lets you use it in the off-line mode to free your computer for other tasks. Applications support is available, including a growing 6502 machine language software library.

The single quantity price is only $640. Ten-digit display option, $190. For more information or literature on the SLC-1 Time Machine, contact Digital Pathways, Inc., 1260 L'Avenida, Mountain View, California 94043, or phone (415) 969-7600.




**GET INTO THE TIME MACHINE.**

# DIGITAL PATHWAYS

CIRCLE 63 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

## Enhanced Capabilities Expand Small Business Microcomputer Series

Consisting of a Z80A and LSI supporting circuitry contained on a single board, Ai Electronics Corp, 2-28-16 Shimomaruko, Ohta-Ku, Tokyo 146 Japan, has added capabilities to its model ABC-20 system, producing four additional models: ABC-21, -24, -25, and -26. Each is a general purpose, business-directed system capable of operating with a variety of software and conversion schemes to support single- to double-density conversions and file exchange programs.

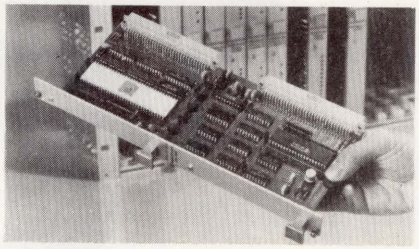
Distinguishing features between models are disc size, 5.25″ (13-cm) or 8″ (20-cm), CRT size, 9″ (23-cm) or 12″ (30-cm), and memory capacity, 640k bytes through 2.3M bytes. Disc systems are double-sided, double-density format and CRT display is 80 x 24. Optional are the 10M-byte Winchester disc and disc/cartridge units, memory extension unit, and 10M-, 20M-, and 40M-byte cartridge disc unit, a printer/lightpen adapter, and a paper tape reader adapter.

AI Electronics' ABC series of microcomputer systems feature 2-piece modular design, with disc and CRT size options. Keyboard includes function and screen control keys as well as numerics keypad

Arranged in a keyboard unit and a CRT/disc assembly, the system features separate RAM display refresh and two serial I/O ports.

Circle 475 on Inquiry Card

## TMS9900 Microprocessor Board Addresses up To 64k Bytes



Utilizing the 16-bit TMS9900 microprocessor, the CPU-200 module includes the microprocessor's bit-serial CRU feature for I/O capabilities. Programmable serial I/O port baud rate, variable character and stop-bit length, and an interval timer are included

Using a 56-line proprietary bus, the 16-bit CPU-200 board can address up to 64k bytes and provide I/O capabilities. Up to 4096 inputs and outputs may be addressed individually. The board includes 16 vectored interrupts, 8-line bit programmable port, and interval timer, and is software compatible with TI990 mini and microcomputers. TIBUG MONITOR and POWER BASIC are offered in P/ROM.

Included on the TMS9900 microprocessor based board from Erni and Co, 3316 Commercial Ave, Northbrook, IL 60062, is a serial port which can be configured as either an RS-232 or current loop. The port may be programmed for 75- to 38.4k-baud operation, 5-to 8-bit character length, and 1, 1½, or 2 stop bits.

The instruction set includes 16 arithmetic with multiply and divide, 20 program control, 14 data control, 6 logical, 4 shift, 5 bit serial I/O, and 6 external control instructions. Typical execution times with a 3-MHz clock rate are 2 μs for BRANCH and 31 μs for DIVIDE. The 4 x 9″ (10 x 23-cm) board requires 5 Vdc at 0.5 A, 15 Vdc at 90 mA, and −15 Vdc at 30 mA, and is priced at $560.

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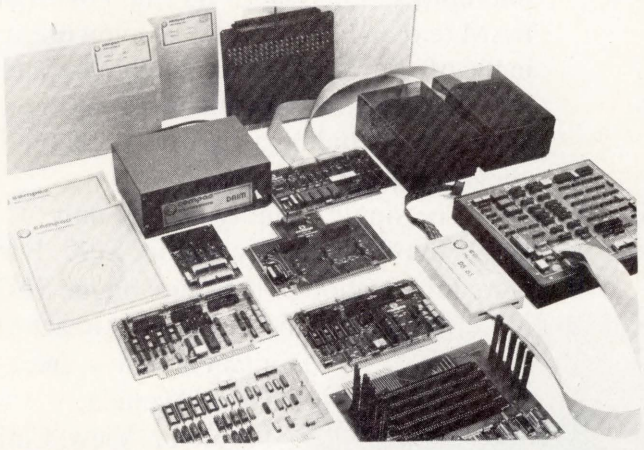
compas microsystems

6500 USERS



We offer the most complete line of 6500 support tools available — both hardware and software. Our CSB family of single board computers get your project running quickly. The DAIM floppy disk system turns your AIM 65 into a serious development system. The DB/65 provides the debug system you have been looking for. Cross assemblers are available for many popular computers plus CSL/65 — *the* high level language for the 6500 family.

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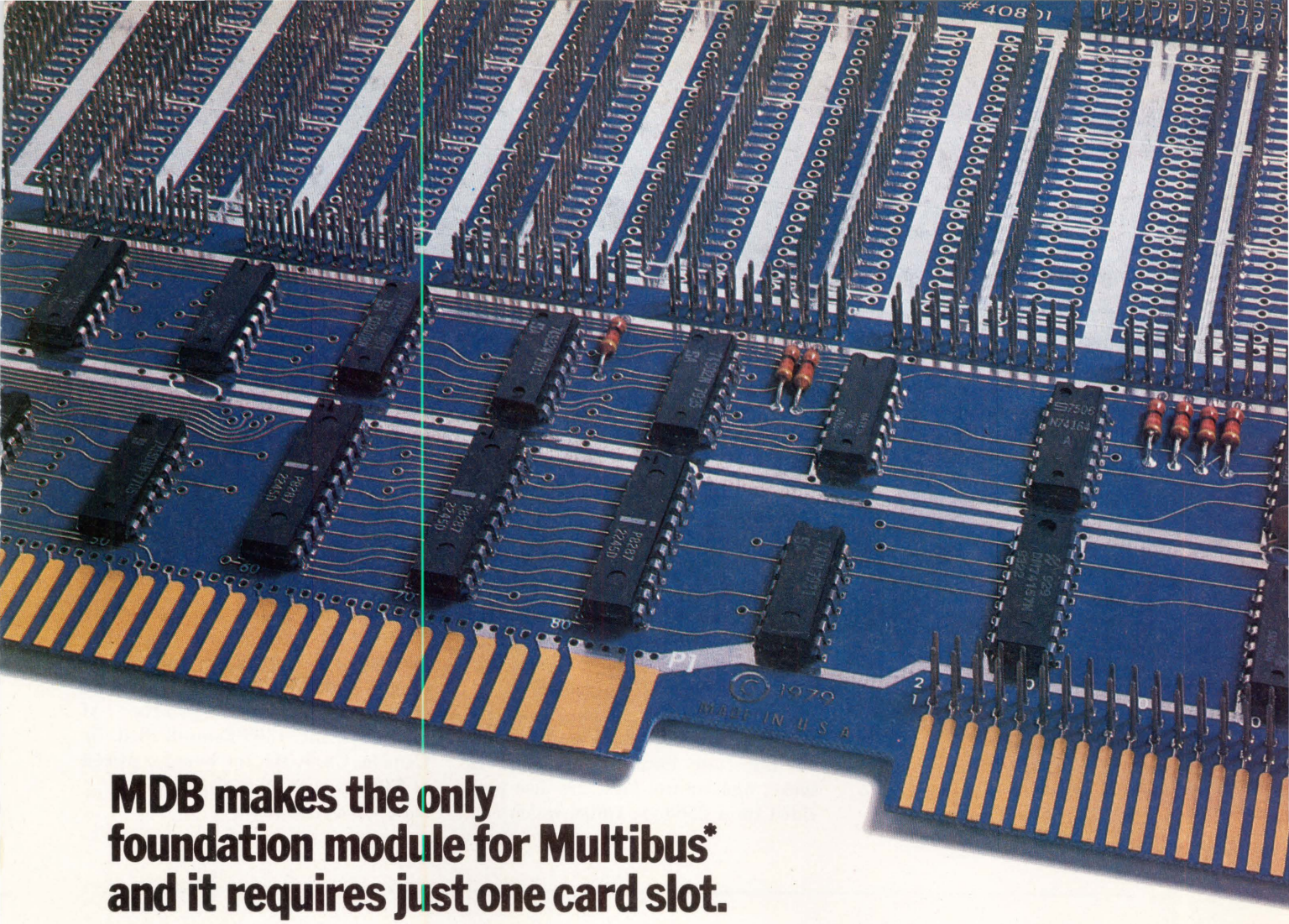


## MDB makes the only foundation module for Multibus* and it requires just one card slot.

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If you've never been excited about a foundation module before, now's the time. MDB offers the industry's first module for use with Intel 16 and 8 bit single board computers. It gives low cost Multibus-to-peripheral interface with complete address and interrupt logic, standard Intel board spacing and room for up to 38 sockets or IC devices of any size on the wire wrap portion of the board. Because all wire wrap pins and components are on the same side of the board, the module requires only one card slot. And it takes any configuration DIP package and provides three 50-pin edge connector positions. In addition, MDB makes a pure wire wrap general purpose module in a single slot configuration which has space for 60 IC positions. This is the kind of flexibility a logic designer dreams about.

If you're not an Intel user, you can still get MDB design flexibility—in single slot bus foundation and wire wrap modules for PDP**-11, LSI**-11, Data General and Perkin-Elmer computers and wire wrap boards for IBM Series/1. Even the dedicated portions of these modules are application adaptable in that they allow a change of functionality by the use of wire wrap pins.

What else can MDB do for you? Look at our line printer controllers. We offer more than 100 computer/printer combinations. If you need communications modules, interprocessor links, multiplexors and PROM boards, we've got them all with the built-in quality MDB is famous for.

MDB interface products are warranteed for a full year; most can be delivered in 30 days or less, and you can buy them under GSA contract #GS-00C-01960. What can we do for you?

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## Modular Construction Enhances Microcomputer System's Flexibility

Consisting of a Z80A based ZBC-80 single-board computer, 48k bytes of RAM and sockets for 8k bytes of ROM or EPROM, a 2k-byte monitor, dual 8" (20-cm) double-density floppy disc drives, and interfaces for video terminal, line printer, and additional peripherals, the MACS-10 System is MULTIBUS™ compatible. The system and software packages in Pascal, COBOL, BASIC, and FORTRAN are available from Matrox Electronic Systems, Ltd, 5800 Andover Ave, Montreal, Quebec H4T 1H4, Canada.

Modular hardware, which includes the ZBC-80, FFD-1 floppy disc controller/RAM card, CCB-7 7-slot card cage/backplane with power supply, and DF-28 floppy disc drive, is available separately, along with a 128k-byte RAM card and alphanumeric and graphic video display controllers. Up to 3 card cages can be stacked to provide 19 free card slots for system expansion. Single-quantity price is $5990.

Circle 477 on Inquiry Card

## Dual Serial Interface Board Facilitates RS-232/STD BUS Communication

Capable of full-duplex operation in synchronous and asynchronous modes at switch-selectable baud rates of 50 to 19.2k, the SB8420 interfaces two independent RS-232-C, 20-mA communication channels to STD BUS systems. Modem control signals for each channel are also provided.

The board is I/O mapped, and includes an interrupt mask register and an interrupt output connector. A socket and control logic are also provided for a 256-byte P/ROM which can be enabled at system reset to overlay system RAM. This allows RAM based systems to be initialized, and can be used to bootstrap programs from mass storage devices. A product of Micro/Sys, Inc, 1353 Foothill Blvd, La Canada, CA 91011, the board is priced at $325 in quantities of 1 to 9.

Circle 478 on Inquiry Card

## Compact General Purpose Computer Includes Dual Microfloppy Discs

Capable of acting as an intelligent terminal controller as well as a general purpose desktop unit, the RD-11C includes a dual double-headed, double-density microfloppy subsystem which provides 700k bytes of storage, up to 256k bytes of RAM, 4 serial interface ports, and switching power supply housed in a 12.5 x 8.5 x 16.75" (32 x 22 x 42-cm) enclosure. Standard interfaces included are IEEE-488, asynchronous and synchronous serial, general purpose parallel, and DMA.

Peripherals for the system from RDA, Inc, 5012 Herzel Place, Beltsville, MD 20705, include Winchester disc, magnetic and paper tape, punched card, and printers, as well as A-D and D-A plug-in modules.

Compatible with Digital's RT-11 Foreground/Background, the system is based on the LSI-11/2 or -11/23 central processors, and supports a macro assembler, FORTRAN IV, multiuser BASIC, APL, FOCAL, FORTH, and Pascal. Synchronous remote job entry software includes IBM 2780, Univac 1004, and User 200 emulators. Terminal software includes asynchronous TTY emulation for ASCII compatible interface. File transfers in ASCII or binary format are provided for.

Circle 479 on Inquiry Card

## Microcomputer System Uses Cartridge Backup For Data Security

Intended for business, research and development, and systems development, the Z80A based S/1000 microcomputer system, utilizing the S-100 bus structure, is composed of 64k bytes of RAM, 8" (20-cm) hard disc, tape cartridge data backup, optional peripherals, and expansion capability to 16-bit processors. Provided by Computer Service Systems Network (CSSN), 120 Boylston St, Fourth Floor, Boston, MA 02166, are operating systems in CP/M, 2.0, and CSSN PDOS, a literal superset of CP/M, 1.4. Software compatible with the operating systems includes BASIC, COBOL, FORTRAN, C, and Pascal.

Capable of handling four drives, the controller interfaces with the 24M-byte disc via SMD logic. Data stored on disc are protected by a front panel accessible cartridge drive. The backup system's file oriented software can store, file by file, up to 13.4M bytes per cartridge.

Circle 480 on Inquiry Card

# Inside this general purpose memory is the right mix for any match.

**The right mix.**
With the MK8600 add-on memory system, you can get up to 6 megabytes capacity in a compact 12¼ inch chassis. Configure it 768K × 72, 2304K × 16 or any other way you want to complement your existing system. It's that versatile.

**For any match.**
But the real beauty of the MK8600 is how easy it is to interface. The I/O is simple and direct because only minimal control signals are required for any data transfer. This lets you quickly integrate the MK8600 into your system.

Before you specify your next add-on memory system, make sure it has the capacity and interface flexibility to meet your requirements. To be sure, make it the MK8600 add-on memory from Mostek, 1215 West Crosby Road, Carrollton, Texas 75006; (214) 323-6000. In Europe, contact Mostek Brussels 660.69.24.

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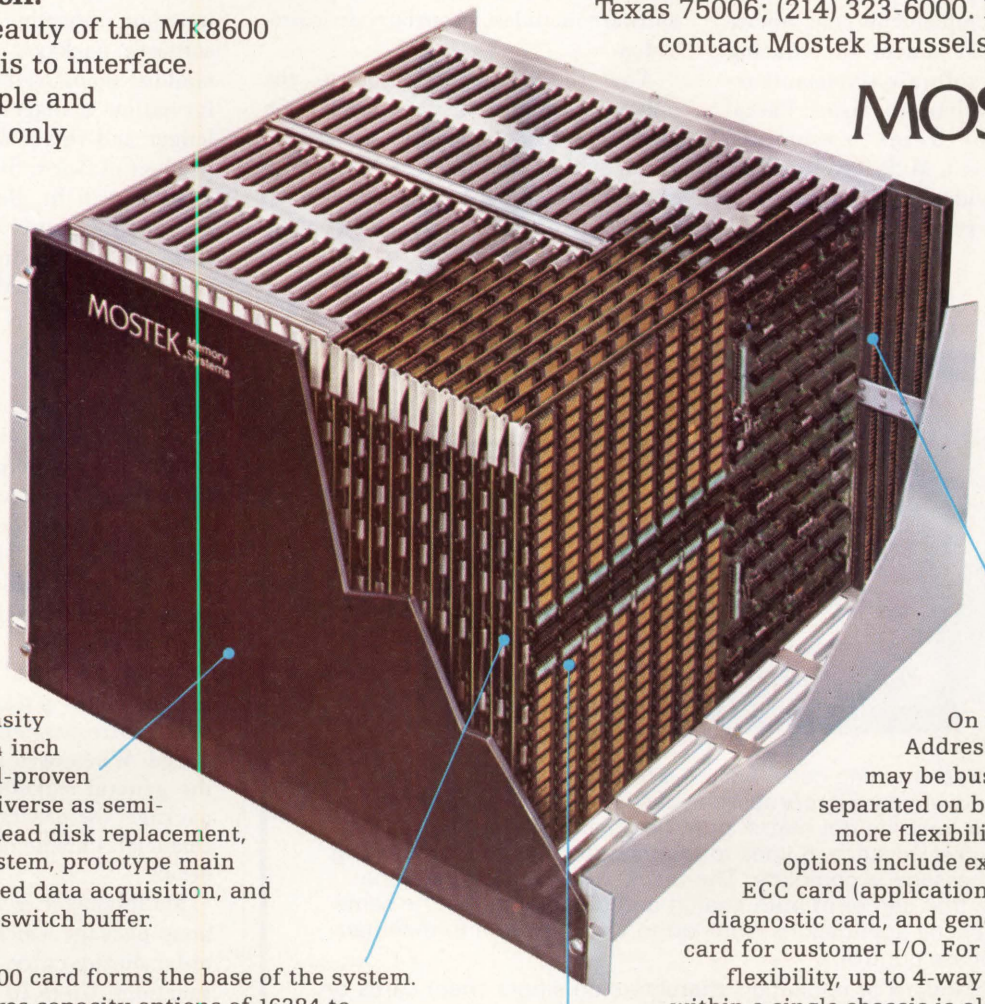


Six megabyte density in a compact 12¼ inch chassis with field-proven applications as diverse as semiconductor fixed head disk replacement, video memory system, prototype main memory, high speed data acquisition, and digital telephone switch buffer.

MK8000 card forms the base of the system. Features capacity options of 16384 to 131072 words up to 24 bits in length on a 15.4 × 11.75 inch P.C. card. Complete timing control and addressing logic self-contained on each board. Other features include customer-specified timing options, inverting or non-inverting data, and byte control.

On the MK8600, Address, DI and DO may be bussed, but are separated on backplane for more flexibility. Available options include extender card, ECC card (application dependent), diagnostic card, and general purpose card for customer I/O. For even greater flexibility, up to 4-way interleaving within a single chassis is also available.

All RAM memory is the industry standard Mostek MK4116 16K dynamic RAM with typical system speed at 250ns access and 450ns cycle time, with faster speeds available for applications requiring high throughput.

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## MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

## SOFTWARE

### Component Software Permits Modular Capabilities Increases

Software designers can incrementally add software for applications with the TMS9900 16-bit microprocessors and TM9900 microcomputer modules. This software bus is analogous to the hardware designer's bus system for expansion capabilities. The component software series complements the microprocessor Pascal system by reducing the number of software statements required; the microprocessor Pascal system, also by Texas Instruments, Inc, PO Box 1443, M/S6404, Houston, TX 77001, provides an optimal method for writing the remaining statements.

Available for use on the company's floppy or hard disc microprocessor development systems are realtime executive and file manager software. The realtime executive serves as the software keystone by providing the interface for all subsequent component software products and block-structured assembly language Pascal applications. System initialization, concurrent process synchronization, interprocess communication, interrupt linkage, memory management, and priority scheduling are contained in a 6k-byte nucleus of software routines which performs the necessary executive functions for a realtime multitasking application program. For the designer who wants to customize the component software modules, a source code is provided.

The file manager supports the TM990/303 floppy disc controller on several levels of capability and can interface the realtime executive on several levels depending on the I/O generality and the designer's application. Functions of the file manager can be increased to include install formatted volume, open/close/read/write files, provide sequential access to files, and rewind/forward and backspace to files. By linking 2k bytes of code to the realtime executive, the user can read and write a floppy disc.

Circle 481 on Inquiry Card

### Software Packages Operate Independently Or as Flexible System

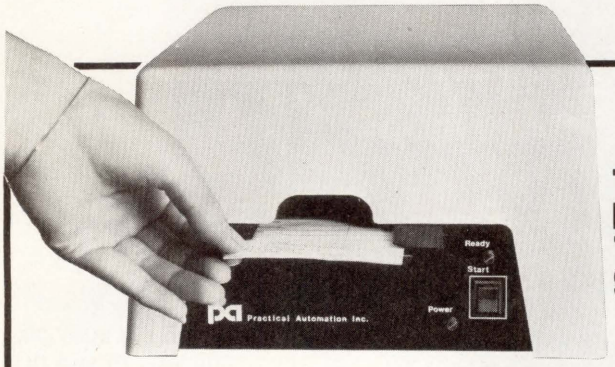
Intended for use either alone or in conjunction with others, four application software packages—word processing, mail-list management, list-oriented information management, and general ledger and financial reporting—are a product of North Star Computers, Inc, 1440 Fourth St, Berkeley, CA 94710. Designed for use on the company's HORIZON microcomputer, all packages require 64k of RAM, a minimum of 2 floppy disc drives, and are available for double-density and quad-capacity versions.

NorthWord, the word processor, incorporates onscreen text editing, simultaneous document printing, and formatting to specific criteria, including page numbering, titling, underlining, and spacing, and is the package upon which the others are built. An onscreen menu is available to the operator.

When combined with the mail-list management package, personalized bulk correspondence may be produced. When used in conjunction with the general ledger/financial reporting package, the production of customized financial statements and reports may occur.

MailManager is a mail-list management package which maintains correct order during entry, correct, and delete functions. Up to 10 data items for each name in the list may be used for sorting and selecting, including sorting by zip code. InfoManager accepts up to 50 categories of information for each record and has the ability to select and sort before printing. GeneralLedger maintains accounts based on input such as checks, deposits, and journal entries.

Circle 482 on Inquiry Card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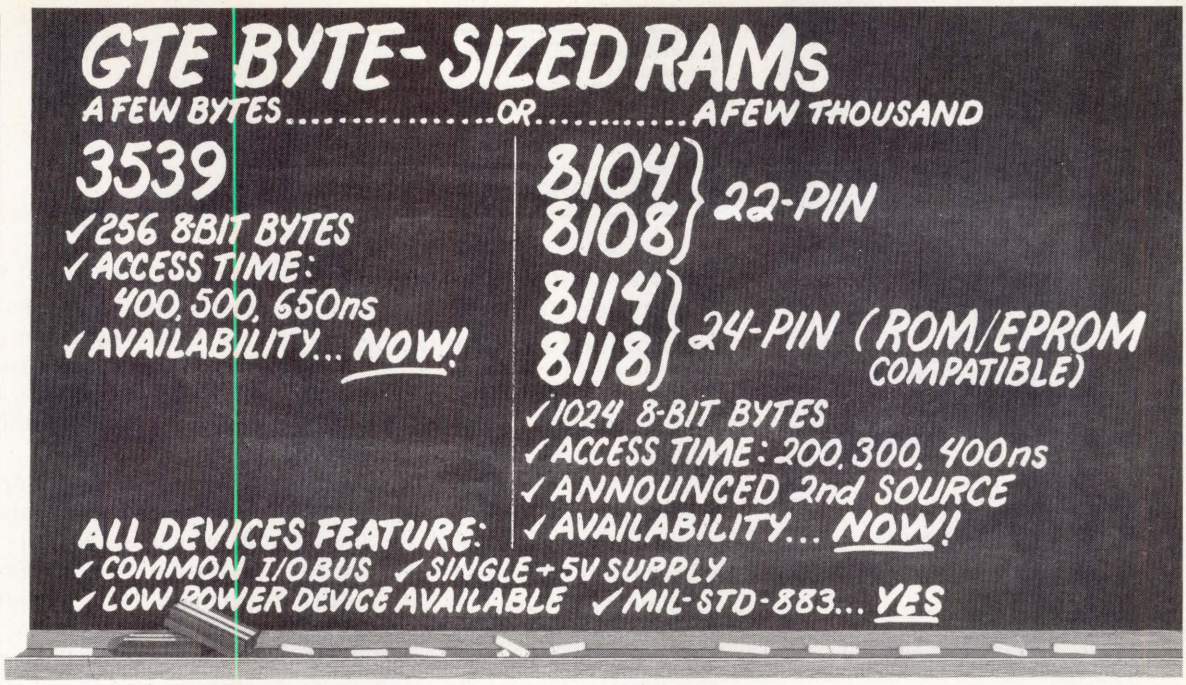
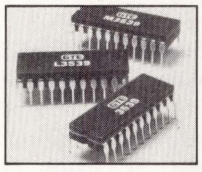
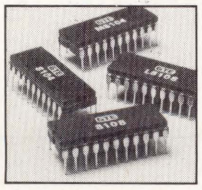



## GTE Has Byte-Sized Memory to Match Your Needs



### A Few Bytes...

If your system needs just a few bytes of memory, take a good hard look at our 3539. For small memory designs, it's ideal. It's organized as 256 8-bit bytes ...a 2048 bit Static RAM packaged in a standard 22-pin DIP. You have a choice of access times... and what's more, it's available in a low power configuration, or you can select a military version that meets MIL-STD-883 requirements. The time-proven, highly reliable 3539 is a natural upgrade for small memory applications using 2111's and 2112's... and you'll like the byte oriented I/O structure.



### or a Few Thousand

On the other hand, if you need a larger memory, consider our 8K family. GTE offers the most complete line of 8K Static RAMs in the industry. They all provide 1024 8-bit bytes, with a common I/O bus for ease of design. You have a choice of access times as low as 200 nanoseconds. For those special applications, our low power units may be the answer... or perhaps an 8K military device that meets MIL-STD-883 requirements... and, all are immediately available.

GTE 8K Static RAMs offer the design engineer many advantages... including higher performance, lower system cost, significant power savings... and the convenience of an 8-bit bus I/O structure. And furthermore, GTE's 8K's are the only Static RAMs with an announced second source.

So... if you need a few bytes, or a few thousand, GTE Microcircuits is the company with the *experience*, the *history*, and the *product variety* to match your memory needs.

## Call Toll Free 800-528-6050

# Byte-Sized Static RAMs

Call Toll Free for the name of your local distributor and a copy of our new Short Form catalog.

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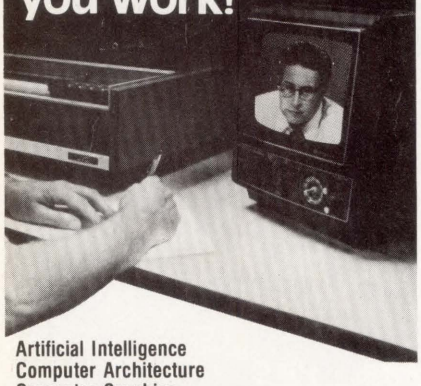

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## MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

## SOFTWARE

### Pascal Language Support Simplifies Z80 Equipment Programming

Known as the Pascal/8002 Z80 processor support package, a software product, designed for use with the Tektronix 8002 microprocessor development system, permits the developers of Z80 based equipment to realize the advantages of accommodation of structured programming techniques, standardization of features, and portability between machines derived through use of the Pascal language. In addition to programming process simplification, the development system provides powerful debugging capabilities.

Barriers to Pascal programming of microprocessors, such as programs being confined to specific ROM locations, variables being stored in known RAM locations, and specific I/O devices being required, are dealt with such that the users can configure Pascal programs to conform to their machine-dependent requirements. To support end-product execution, a multimode interpreter library is included.

Requiring less than half the storage space of equivalent assembly language code for the Z80, Pascal routines are stored in the form of P-codes, an optimized instruction set. Overall memory requirements are reduced since temporary variables are stored in RAM only while valid; thus, the same space may be utilized by different variables during execution.

The processor support package together with a universal program development package are used to assemble the necessary machine language routines required by the program. Integration into the final product occurs by linking the machine language and Pascal routines, locating these in the desired memory locations, and transferring to the Tektronix disc operating system.

Support modules available are real (floating point) numbers, transcendental functions, and operations on sets. Interpreter requirements vary from about 3k bytes to 7k bytes and together they support all features of the UCSD Pascal except external file handling operations. Available from Pascal Development Co, 10381 S De Anza Blvd, Suite 205, Cupertino, CA 95014, the user may select only those modules needed by his program application.

Circle 483 on Inquiry Card

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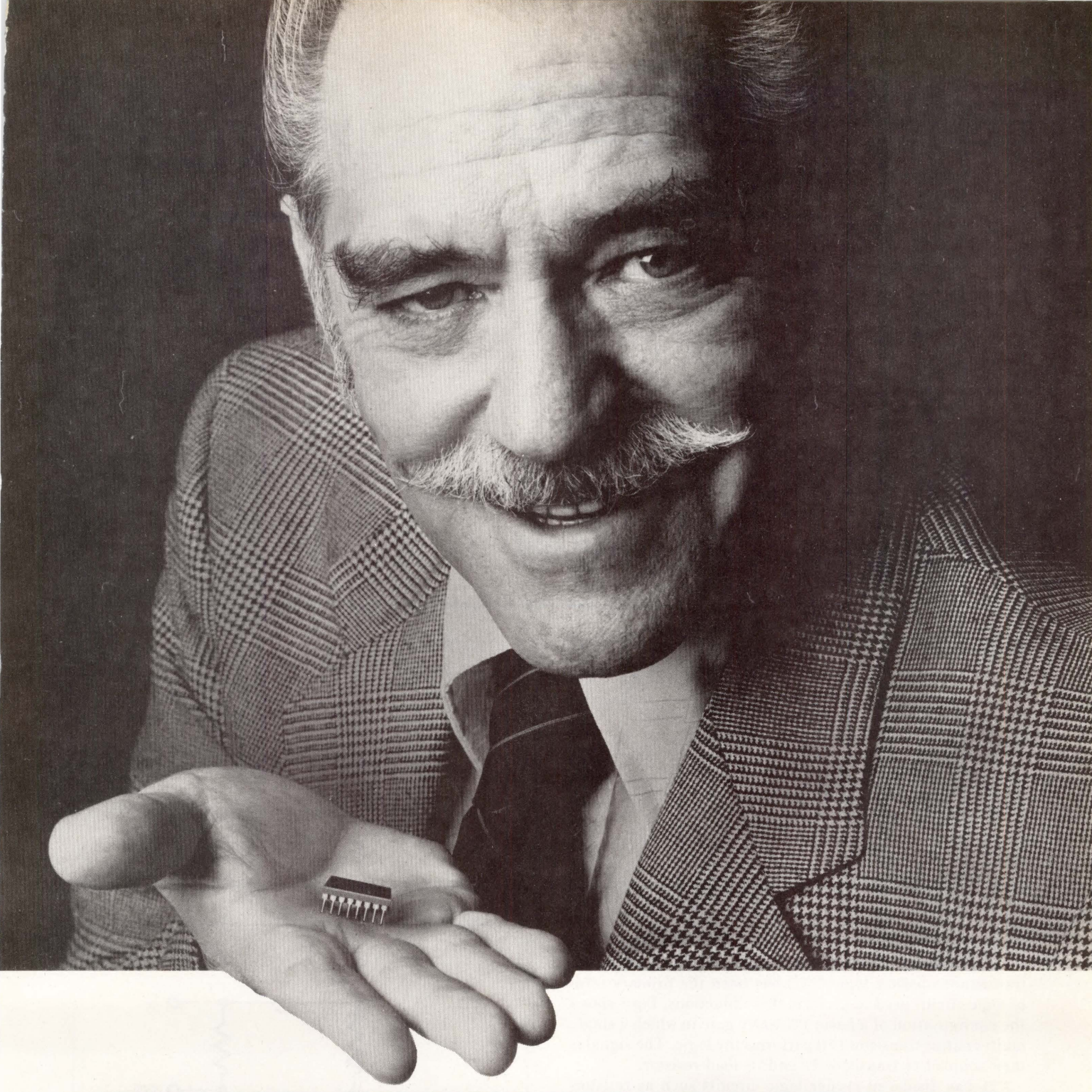
### Improved Pascal/M™ Compiler Extends System's Capabilities

Release two of Pascal/M includes user-initiated capabilities increases along with improved debugging tools. The system now supports long integers, full random I/O and Boolean output. Extensions for assembly language externals, ADA syntax random I/O, runtime recovery, and forty additional built-in procedures are included, as well as support for the full Pascal language.

Implemented using a pseudo-machine code called portable Pascal code (P-code), Pascal/M's instructions optimize instruction execution and code space of Pascal programs. P-code is executed through an interpreter which translates the generated code into target machine code.

Release two, available from Sorcim, 2273 Calle De Luna, Santa Clara, CA 95035, is designed to run on any standard 1.4 or 2.2 version of CP/M or on Cromemco CDOS based system using Z80 or 8080/8085. It requires one floppy disc and 56k bytes of memory. □

Circle 484 on Inquiry Card



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**CIRCLE 75 ON INQUIRY CARD**

# TWO SCHOTTKY TTL FAMILIES

**Robert A. Stehlin**

Texas Instruments Incorporated
PO Box 225012, Dallas, TX 75265

All computers, whatever their size, utilize basic logic functions such as OR, AND, NOT, NOR, and NAND. For many years, transistor-transistor logic (TTL) has been the primary form of logic circuit used to perform these functions. Fig 1 shows the configuration of a basic TTL NAND gate in which a single multi-emitter transistor (T1) performs the logic. The signal is then coupled to transistor T2 and its load resistor.

TTL has displaced earlier logic circuits such as resistor-transistor logic (RTL), in which logic was performed by input resistors, and diode-transistor logic (DTL), in which logic was performed by input diodes. This displacement is based on superior performance, the TTL provides faster speed, lower power, and higher fanout capability. It is adaptable to virtually all forms of IC logic and provides the lowest pico-joule-dollar product of any logic type.

Schottky TTL is a derivative of TTL, designed to increase TTL speed in order to approach the speed of emitter-coupled logic (ECL). This logic is fully compatible with other members of the TTL family and equally as easy to use.

The configuration for Schottky TTL is basically the same as standard TTL except that Schottky barrier-diode clamped transistors are included in the circuit. Fig 2 shows a transistor clamped with a Schottky barrier-diode (SBD). The

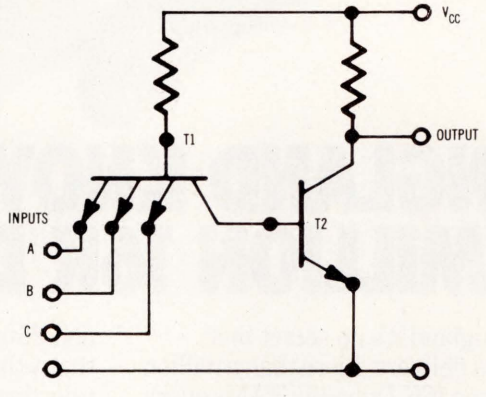


Fig 1 Basic transistor-transistor logic (TTL) circuit. T1 is multi-emitter TTL transistor

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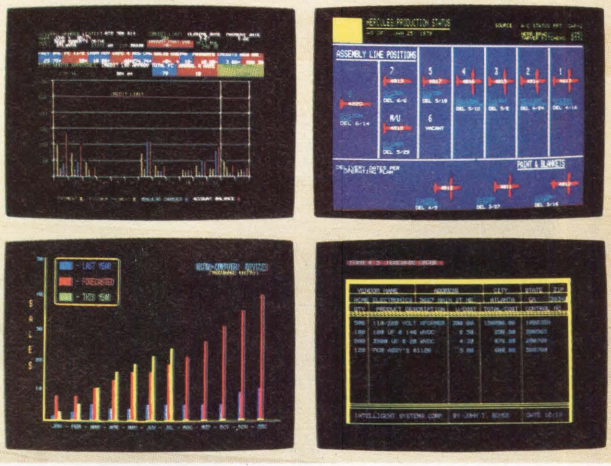
The 3621 is ideally suited for distributed processing. Standing alone or used on-line with another system, it can provide up-to-the-minute data on everything from inventory to personnel. In 8 dynamic colors that speed comprehension and increase user efficiency.

The system includes 32K RAM for user workspace, and a built-in micro-disk drive that uses specially formatted Sof-Disks™ with 51.2K bytes of storage per side. Optional separate disk drives can add up to 26M bytes of memory. Also available is an X-bus interface for any number of peripherals.

A BASIC interpreter and FORTRAN compiler, both standard, give a choice of two powerful languages. As an option, users may specify special graphic characters of their design.

Intecolor's 3621 is made for maximum flexibility – from its unique file handling capabilities to the deluxe built-in keyboard with color and numeric clusters.

See for yourself how it can address complex applications and improve your operation. Contact your ISC sales rep today, and put color to work for you. **Color Communicates Better**




Unretouched photo of screen. *U.S. domestic price.

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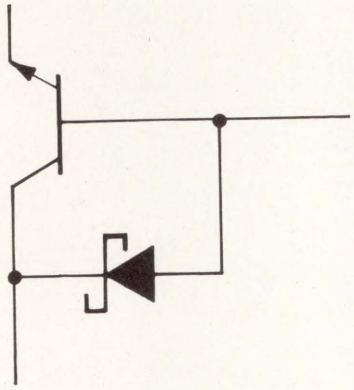

Fig 2 Schottky barrier diode-clamped transistor. Diode between base and collector has forward voltage lower than that for collector-base junction. This prevents saturation, increasing switching speed

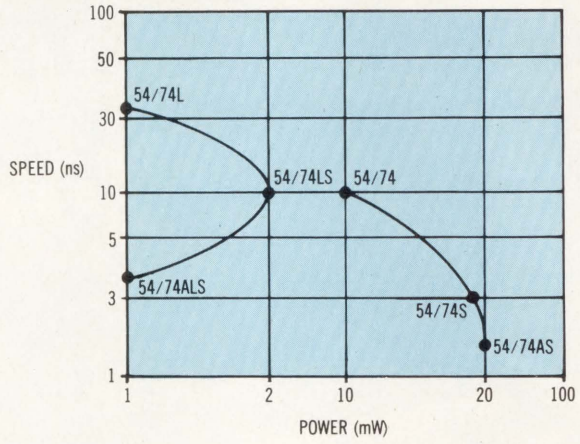


Fig 3 TTL logic families speed/power graph. Right hand curve traces higher speed families, including 54/74 (standard TTL), 54/74S (Schottky TTL), and 54/74AS (advanced Schottky TTL). Left hand curve shows comparable history of low power families, with most recent advanced low power Schottky (ALS) offering 4 – pJ speed/power product

diode is located between the transistor's base and collector to prevent the transistor from saturating. The diode's forward voltage, $V_F$, which is lower than the voltage required to forward bias the collector-base diode of a silicon transistor, prevents saturation. The SBD diverts current from the base of the transistor into the collector, reducing the base-collector voltage. Because the Schottky barrier diode is extremely fast and the transistor does not saturate, switching speed is increased and propagation delays are reduced.

## Advanced Schottky Families

Recently, Texas Instruments added two new Schottky TTL logic families to its line of bipolar 54/74 series TTL functions (Fig 3). The Advanced Schottky (AS) family is in the high speed portion of the spectrum. This series provides a complete family of functions two times faster than any Schottky TTL function previously available. Full gate delay for AS SSI functions is typically 1.5 ns and gate power dissipation, 20 mW. The speed/power product is, therefore, approximately 30 pJ. Internal gate delay for AS MSI functions is 1 ns (typ), and gate power dissipation is 12 mW (typ).

This new family is primarily for systems designs in which maximum possible speed is the primary factor. Available in 20- and 24-pin DIPs, the devices will encompass the MSI arithmetic operators and the supporting gate and flipflop functions required to implement high speed CPUs, controllers, and processors.

The second family, Advanced Low Power Schottky (ALS), is in the low power, high speed portion of the bipolar TTL performance spectrum. This series provides a complete family of TTL functions, which (when compared with the

earlier series from this manufacturer) presents a power dissipation 50% less than low power Schottky TTL (LS), and a speed two times faster than low power Schottky or the standard TTL series. Full gate delay is typically 4 ns and gate power dissipation is typically 1 mW for a speed/power product of 4 pJ.

This family is used for a broad range of applications in which low power is primary but speed is also critical. Because of the power demands, these devices will ease many design problems in microprocessor based systems and will significantly improve overall system performance. ALS functions can replace identical functions in the standard and low power TTL families, with improvements in both power and speed. It can also replace some LS and Schottky functions where speed/power tradeoffs can be made.

Fan-out capability, which eases system design and improves performance, is another advantage of the ALS family. Functions are capable of driving 10 loads (54ALS or 54LS) or 20 loads (74ALS or 74LS). Input voltage level $V_{IL}$ (max) is 0.8 V, providing good noise immunity.

This series will consist initially of 75 device types currently in the LS series, including gates, dual D and J-K flipflops, and MSI functions. Having the same drive as the LS series, these ICs will provide immediate plug-in to existing logic systems.

## Summary

The advanced Schottky TTL families described here are fully compatible with earlier TTL and Schottky TTL series, in both military and commercial temperature ranges. Improved speed/power performance, increased function complexity, and other advantages of these two advanced logic families are primarily the result of two technological factors. Oxide sidewall isolation significantly reduces parasitic capacitance and capacitance between active components. Ion implantion permits shallower junctions. With less capacitance and shallower junctions, speed is increased.

Many MSI functions will be offered in 300-mil wide, 24-pin ceramic and plastic DIPs, allowing a designer to approximately double the functional densities while reducing board space by 30%. This increased density, coupled with an increasing breadth of product selection, will provide significant improvements in efficiency and reliability.

Designers using TTL circuitry have always been faced with constraints in the correlated values of speed and power consumption. These two advanced Schottky families have been positioned at opposite ends of the bipolar speed/power spectrum to offer a choice of design options.


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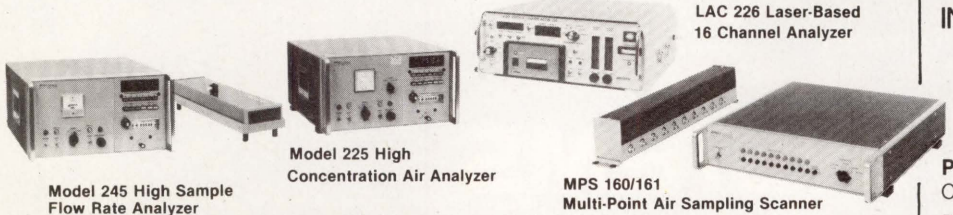

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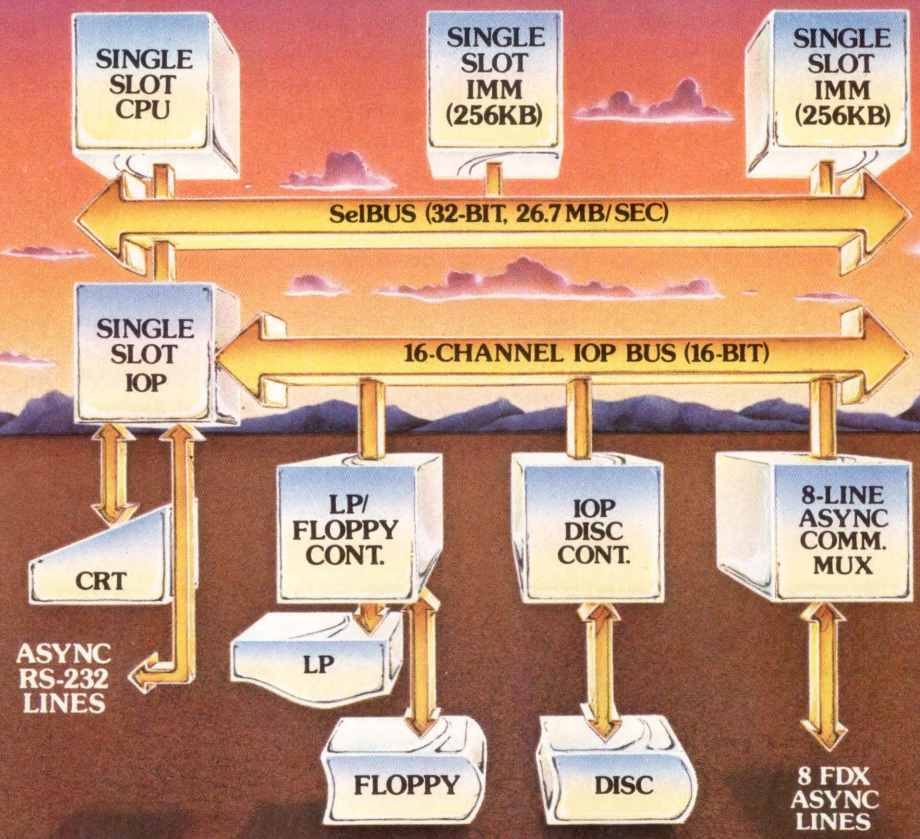


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**CIRCLE 80 ON INQUIRY CARD**

## Single LSI Chip Operates as Universal Analog Controller

Said to be the industry's first monolithic LSI universal analog controller, a chip from Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086, is aimed at industrial applications where closed loop control of machine speed and acceleration is required. These would include conveyer systems, web infeed for plastic film or paper, wire reel take-up, programmable acceleration, deceleration and speed control of single or multiple ac and dc motors, and similar process control installations. Electronic equipment applications would include such uses as magnetic tape transport control and rigid and floppy disc controllers.

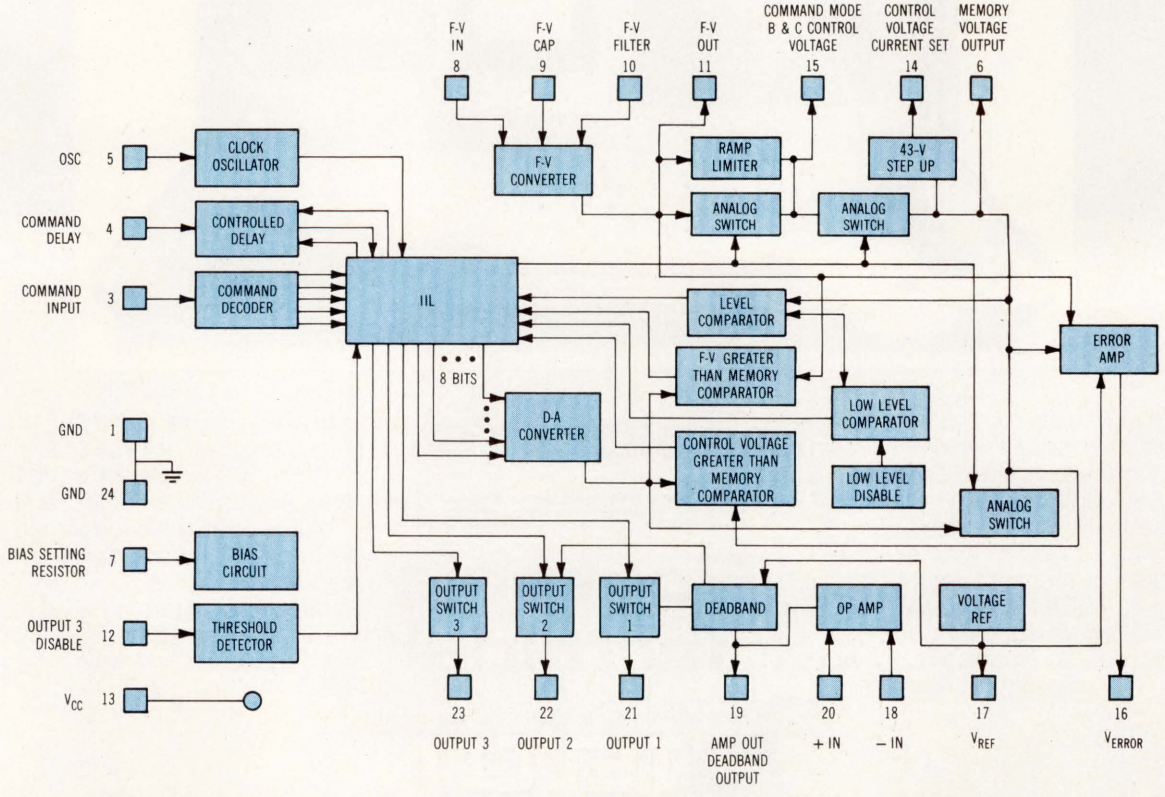
The NE5522N includes a frequency to voltage converter, an internal reference oscillator, a D-A converter, an IIL encoder-decoder, and 256-bit F-V dc level data storage.

This device offers programmable operation modes which can be selected by analog input command. Available modes include on, positive ramp and hold, compare to set memory, memory erase, set memory, and off. No external analog to digital converter is required.

In performance of the closed loop control function, an ac tachometer frequency representing a machine speed is fed into the controller. There, after being processed by the onchip F-V converter, it is compared with an internal reference voltage. An error signal is then generated which governs the corrective response of the output. The output function consists of three buffered open collector transistor ports which provide gating and on-off commands to peripheral circuitry. An analog error output is also available for interface with linear control systems.

The 256-bit memory makes it possible to modify the sequencing mode during normal operation, while retaining previously set information. Programmable command delay allows response time of command inputs to be adjusted in order to eliminate effects of switch bounce and unwanted noise.

System gain, frequency, sensitivity, and ramp rate are all adjustable, with the onchip memory and the DAC able




Universal analog controller, NE5522N, from Signetics is implemented in LSI. Chip is used for industrial applications involving closed loop control of machine speed and acceleration

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to operate at up to 100 kHz to accommodate rapid command input sequencing. Chip size is 130 x 170 mil, with packaging provided in a 24-pin DIP.

A typical operation sequence might be to bring a motor up to speed using the program accel mode. This would be accomplished by setting pin 3 (command input) to approx 0.55 $V_{CC}$. A ramp function determined by R20-C11 (pins 14, 15) then automatically programs the error system to drive up at a fixed rate. Once the desired speed is reached, a voltage of 0.75 $V_{CC}$ is momentarily impressed on the command input and the motor speed will then be controlled to stay at that level previously programmed in memory. Note that a voltage level of 1.1 $V_{CC}$ must be applied momentarily to the command input (pin 3) upon initial turn on in order to enable the device.

The nominal supply voltage is 8.2 V with a range of 7.4 to 9 V allowed. Current drain is nominally 20 mA for an 8.2-V supply. Temperature is limited to a range of 0 to 70 °C in operation and −65 to 150 °C in storage.

Circle 501 on Inquiry Card

## Bus Transceivers Implemented in CMOS

Designed for high speed asynchronous 2-way communication between data buses, a pair of octal bus transceivers from Mitel Semiconductor, PO Box 13089, Kanata, Ottawa, Ontario K2K 1X3, Canada, are implemented using a proprietary low power, high speed CMOS process. Each device contains two sets of octal buffers connected in parallel, and incorporates direction control logic. The MD74C245A is specified for operation over a temperature range from −40 to 85 °C, the MD54C245A from −55 to 125 °C. Packaged in 20-pin DIPs, the devices are pin-for-pin compatible with 74LS245 and 54LS245 transceivers.

While offering the fast propagation speeds and functional features of their low power Schottky, pin-for-pin counterparts, they possess noise immunity and negligible CMOS power dissipation. The devices are fully functional over an extended voltage supply range of 3 to 6.5 V. Three-state outputs permit driving of multiple TTL loads, while the inputs have the advantage of CMOS high impedance.

Typical parameters include a power consumption of 50 μW, port-to-port speed of 15 ns, enable-disable times of 24 ns, and output rise-fall times >15 ns. Absolute maximum ratings require that supply voltage, $V_{CC}$, stay between −0.5 and 7.0 V, and that input voltages stay between −0.3 V and $V_{CC}$ + 0.3 V.

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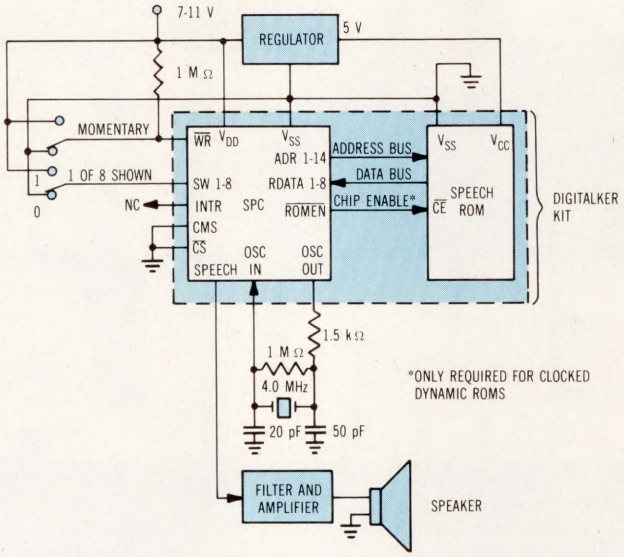
## Processor Chip Synthesizes Speech From ROM Data

A speech processor chip (SPC) from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, can access up to 128k bits of speech data, stored in read only memory. The storage of spoken sequences is offered on a custom basis by the manufacturer. As many as 256 separate addressable expressions are digitized and compressed from high quality reel to reel tapes provided by the customer. Stored with the speech data are the frequency and amplitude data required for speech output.

The final product delivered to the customer is a kit that includes the processor chip and one or more ROMs containing the digitized words or phrases. When these elements are combined with an external filter, amplifier, and speaker (as in the figure), the result is a speech synthesis system which generates high quality speech, including the natural inflection and emphasis of the original speech. The basic 128k-bits of accessible speech data can be expanded with minimum external logic. An interrupt is generated at the end of each speech sequence, so that several sets of words or phrases can be cascaded to form different speech expressions.

This is a completely independent system, not requiring a processor controller. It is designed to be easily interfaced to most popular microprocessors. Other characteristics include communication with either static or clocked dynamic ROMs, TTL compatability, MICROBUS™ compatability, onchip switch debounce for interfacing to manual switches, and the use of either a crystal-controlled or externally driven oscillator. The system provides the ability to store silence durations for timing sequences. Uses for the system are found in applications such as telecommunications, clocks, language translators, and annunciators. Since the system is not constrained by the kind of microprocessor used, it is generally adaptable to a wide variety of applications. The bus interface is simple enough to be handled by low cost microcontrollers, such as those in this manufacturer's COPs™ family.




Speech synthesis system from National Semiconductor uses speech processor chip (SPC) and ROM to generate up to 256 addressable expressions. External filter, amplifier, and speaker are added for complete system, Digitalker™, able to synthesize men's, women's, and children's voices

Absolute maximum ratings for the n-channel MOS speech processor chip limit $V_{DD} - V_{SS}$ and also voltage at any pin to 12 V or less. The allowable temperature range is 0 to 70 °C in operation and −65 to 150 °C in storage.

## Tone Encoder Chip Offers Oscillator Mute, Single Contact Keyboard

A CMOS chip from Intersil, Inc, 10710 N Tantau Ave, Cupertino, CA 95014, functions as a 2-of-8 sinewave tone encoder for use in telephone dialing systems. The ICM7206C Touchtone™ encoder combines the oscillator mute and single contact keyboard features of two earlier chips in this encoder family.

This circuit contains a high frequency oscillator, two separate programmable dividers, a D-A converter, and a high level bipolar output driver. The reference frequency is generated from a fully integrated oscillator requiring only a 3.58-MHz color TV crystal. This frequency is divided by 8 and is then gated into two divide-by-N counters (possible division ratios 1 through 128) which provide the correct division ratios for the upper and lower band of frequencies. The outputs from these counters are further divided by 8 to provide the time sequencing for a 4 voltage level synthesis of each sinewave. Both sinewaves are added and buffered to a high current output driver, with provisions made for up to two external capacitors for low pass filtering, if desired. Output distortion

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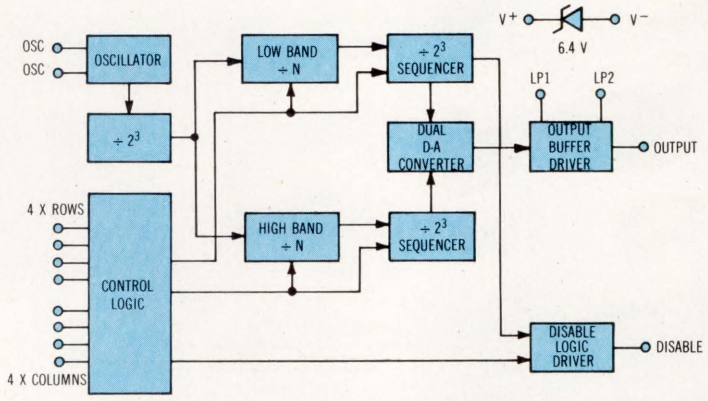



Intersil's ICM7206C touch tone encoder. Onchip elements include oscillator, programmable dividers, DAC, and output driver

is only 2 to 3% with simple filtering, decreasing in value with ascending harmonic frequencies.

The oscillator mute capability, a characteristic which this chip shares with the earlier ICM7206B, means that the oscillator will be on only during the time that a row is enabled (a key depressed). An n-channel open drain FET with its source tied to $V^-$ provides the disable output. The single contact keyboard feature is found in the earlier ICM7206, and, like that chip, this one can use a 3 x 4 or 4 x 4 keyboard.

Output drive level of the tone pairs will be approximately −3 dBV into a 900-Ω termination. Skew between the high and low groups is typically 2.5 dB without low pass filtering. The device will operate with supply voltages as low as 3 V, and dissipates less than 5.5 mW at 5.5 V.

This chip can generate either single or dual tones, suitable for use with telephones, for keyboard entry of numerical data, and similar applications. Oscillator startup time is only 5 ms, and a multiple key lockout is provided. The device is available from stock in either 16-pin plastic DIPs or in die form.

TMTouchtone is the registered trademark of AT&T.

Circle 503 on Inquiry Card

## Speech Chip Set Includes 128k ROM And Synthesizer Chip

Texas Instruments Inc, PO Box 1443, Houston TX 77001, has announced a series of speech-processing computer chips (TMS5000) and a series of compatible storage devices (TMS6000). Initial products being offered are the TMS5100 single-chip synthesizer and the TMS6100 PMOS 128k read only memory. A chip set, including synthesizer and ROM, provides 100 words (100 s) of synthetic speech.

Speech encoding on the speech synthesis IC is achieved through pitch excited Linear Predictive Coding (LPC), utilizing a linear equation to formulate a mathematical model of the human vocal tract and predicting a speech sample based on previous ones. LPC is a technique of analyzing and synthesizing human speech by determining from original speech a description of a time varying digital filter modeling the vocal tract. This filter is excited by either periodic or random inputs. An onchip 8-bit digital to analog converter transforms digital information processed through the filter into synthetic speech.

Periodic inputs to the filter are used to reproduce voiced sounds which have a definite pitch such as vowel sounds, or voiced fricatives such as Z, B, or D. A random input models unvoiced sounds such as S, F, T, and SH. The speech synthesis chip uses two separate models to generate the voiced and unvoiced excitation.

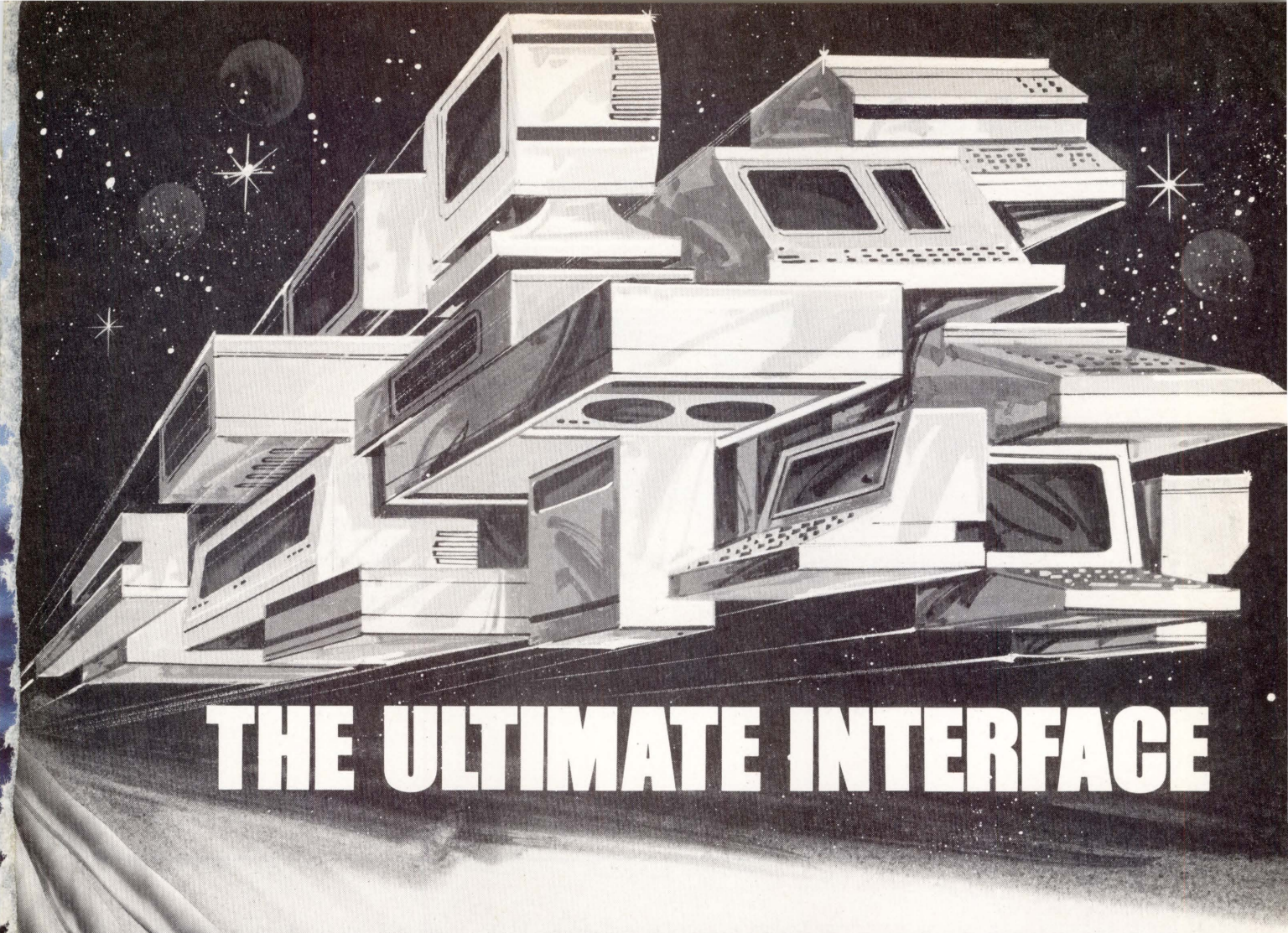
Codes for 12 synthesis parameters (10 filter coefficients, pitch and energy) serve as inputs to the synthesizer chip. These codes may be stored in ROM and, once decoded by onchip circuitry, represent the time varying description of the LPC synthesis model.

The onchip filter is an advanced design single-stage filter which implements a 10-stage lattice with an integrated array multiplier, an adder coupled to the multiplier output, and various delay circuits coupled to the adder output. With this computational sequencing capability and a fast continuous data transfer rate, the multiplier can accept 2 inputs every 5 μs. Twenty multiply and accumulate operations are needed to generate each speech sample, and the circuit can generate up to 10k speech samples per second.

Circle 504 on Inquiry Card

## Isolation Amps Feature Low Cost

Two isolation amplifiers announced by Analog Devices (Rte 1 Industrial Park, Norwood, MA 02062) provide ±1500-Vdc continuous isolation, 100-dB common mode rejection (min, at 60 Hz), single-supply operation from 8 to 15.5 V, and nonlinearity of ±0.1% typ. Priced from $49 in quantities of 1 to 9, and $30 in 100s, the devices also provide ±13-V power, isolated to ±1500 V, for floating front-end signal conditioning circuitry. No



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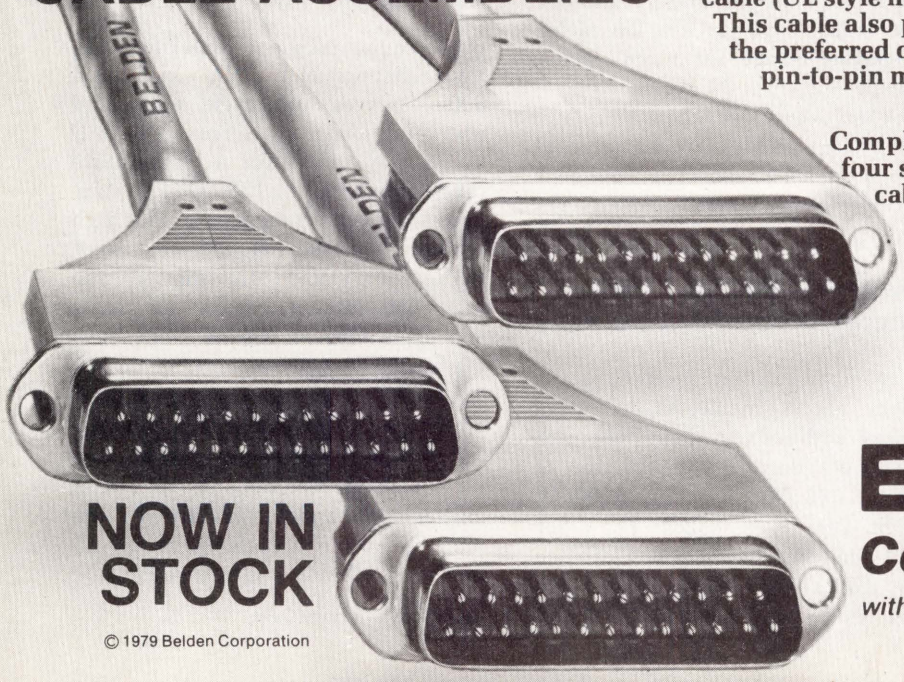
**Complete cable assemblies are now in stock in four standard lengths of up to 70′ (21m). Bulk cable is available in put-ups of up to 1000′. Custom designed assemblies are also available on special request. Belden Corporation, Electronic Division, P.O. Box 1980, Richmond, IN 47374; 319-983-5200. Out West contact our Regional Sales Office in Irvine, CA 714-833-7700.**

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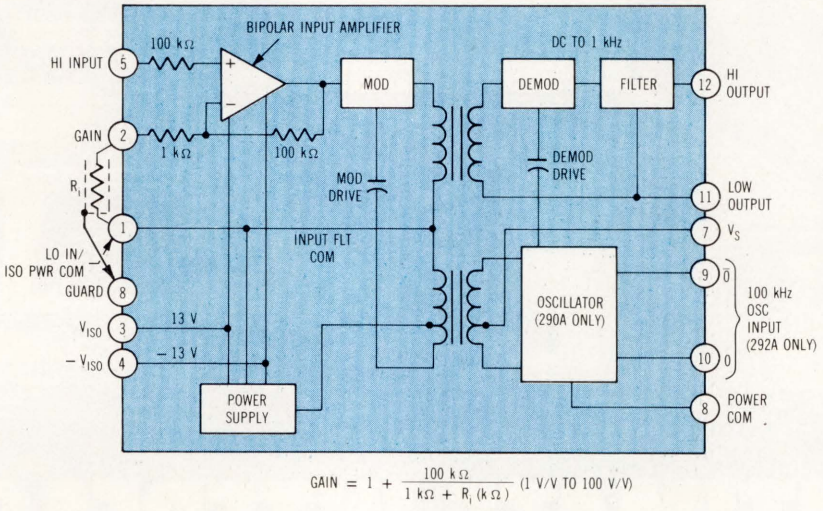
CIRCLE 85 ON INQUIRY CARD




$$\text{GAIN} = 1 + \frac{100\ \text{k}\Omega}{1\ \text{k}\Omega + R_1\ (\text{k}\Omega)}\ (1\ \text{V/V TO}\ 100\ \text{V/V})$$

Isolation amplifiers 290A and 292A from Analog Devices. Carrier isolation technique is used to transfer both signal and power between amplifier's guarded input stage and rest of circuitry

external dc-dc converter is required as in optically coupled designs. The devices are available from stock.

Model 290A has a self-contained oscillator and is intended for single-channel applications. The 292A is designed for multichannel applications. A single external synchronizing oscillator can drive up to 16 of the multichannel devices or a virtually limitless number of these can be configured using multiple oscillators. The user can supply the external oscillator circuit or specify model 281 oscillator module, which includes a voltage regulator for operation over a wide single supply voltage range of 8 to 28 V.

These devices offer complete galvanic isolation and protection against damage from transients and fault voltages in data acquisition systems, computer interface systems, and high CMV instrumentation. Other applications include process control, measurement and control systems, and (generally) the measurement of off-ground signals, especially in noisy environments.

Additional features include a gain range of 1 to 100 V/V which is set with a single external resistor, high reliability with a calculated MTBF exceeding 400k hours, low offset voltage drift of 10$\mu$V/°C, referred to input at a gain of 100 V/V, and small size of 1.5 x 1.5 x 0.62" (38 x 38 x 16 mm). Input noise is 1 $\mu$V pk-pk (10-Hz bandwidth, G = 100 V/V), nonlinearity is ±0.1% at 10-V pk-pk output, and I/O dynamic range is 20 V pk-pk. The operating temperature range for rated performance is −25 to +85 °C.

Circle 505 on Inquiry Card

## Industry-Standard RAMs Announced by Two Sources

Two companies that produce static random access memories have announced additions to their lines with industry standard 2114 RAMs. One of these is GTE Microcircuits, 2000 W 14th St, Tempe, AZ 85281. The other is OKI Semiconductor, 1333 Lawrence Expy, Suite 401, Santa Clara, CA 95051. In common with 2114 RAMs in general, all of the new memories are organized as 1k x 4, operate off single 5-V supplies, and provide fully static operation without clock or refresh. They provide directly TTL compatible I/O, a common I/O bus, 3-state outputs, and packaging in an 18-pin DIP.

### High Reliability RAMs

GTE's announcement describes the high reliability M2114-3MA, which has a 300-ns access and cycle time, and which (although not screened to MIL-STD-883) operates over a temperature range from −55 to 125 °C. The company has been producing another high reliability version of the 2114 since September 1978. Designated the M2114-UMA, that device has an access and cycle time of 450 ns. Both RAMs use a power supply current, $I_{CC}$, of 100 mA (max). These memories are intended for use in applications where operational integrity is essential. They are especially recommended for any space, military, or commercial aircraft application where replacement is difficult and reliability is imperative.

Circle 506 on Inquiry Card

# Computer Sciences Corporation

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**There appears to be no practical limit to CSC growth in advanced communication systems, or to the numbers of engineers we seek who understand digital circuit switching from a system viewpoint... who can generate requirements from customer inputs... who can conceptualize the systems... who can peg them to the realities of size, trade-offs, and, in many cases, to turnkey deliverables.**

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**Transmission & Communications Processing**
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Low power versions have also been announced in both the 300- and 450-ns configurations. Designated the N2114-3MA and N2114-UMA, these low power devices typically dissipate only 375 mW, with max $I_{CC}$ of 75 mA, and are screened to the requirements of MIL-STD-883.

### Fast Access Times

The three memories announced by OKI provide max power dissipation of 370 mW. They are the 2114L-2 (200-ns max access time), 2114L-3 (300-ns max access time), and 2114L (450-ns max access time). Directly interchangeable with all standard 2114L parts, these RAMs are available for immediate delivery beginning at $5.45 (for the 450-ns part) in 100 plus quantities.

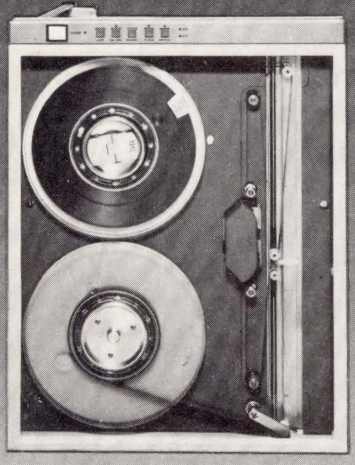
Circle 507 on Inquiry Card


$3550.

The new 75 ips TDX Series II Tape Drives – Priced from $3550 in OEM quantities.*

Fully IBM compatible. No program restrictions. Industry standard interface. Patented low inertia tape tensioning system.

*Includes complete 800 or 1600 bpi tape drives in 100 per year quantity. Dual Density 800/1600 bpi version — $3750. Contact Tad Richardson for additional details.



TDX PERIPHERALS

Division of GAW Control Corp.
150 New York Avenue, Halesite, NY 11743
(516) 423-3232

CIRCLE 87 ON INQUIRY CARD


## BiMOS Op Amps Combine MOS, Bipolar Advantages

A series of operational amplifiers from RCA Electro-Optics and Devices, Rte 202, Somerville, NJ 08876, features gate-protected MOS/FET (PMOS) input transistors for high input impedance ($10^{12}$ Ω typ) and a wide common-mode input voltage range, and bipolar and MOS output transistors for a wide output voltage swing and high output current capability. The CA080 is an externally phase compensated single amplifier; the CA081 is an internally compensated single amplifier; and the CA082 and CA083 are internally phase compensated dual amplifiers. All but the -082 have provisions for external offset nulling.

Combining the advantages of MOS and bipolar transistors on the same monolithic chip, these op amps are said to be improved equivalents of the industry standard TL080 BiFET series. Applications include inverters, high-Q notch filters, IC preamps, unity gain absolute value amplifiers, sample and hold amplifiers, and active filters.

Typical parameters include an input bias current of 15 pA, input offset current of 5 pA, slew rate of 13 V/μs, unity-gain bandwidth of 5 MHz, and equivalent input noise voltage of 40 $nV/\sqrt{Hz}$. Input offset voltage has a typ value between 2 and 5 mV, depending on model variations within each of the four principal types.

The devices are supplied in a variety of package options, including the 8-lead plastic DIP (Mini-DIP), the 14-lead DIP, the 8-lead TO-5 style, the 8-lead TO-5 style with dual-inline formed leads (DIL-CAN), and in chip form. Operating temperature range is either 0 to 70 °C or −55 to 125 °C, depending on model. Absolute maximum ratings limit dc supply voltage to ±18 V, differential input voltage to ±16 V, input voltage to ±15 V, and input current to 1 mA.

Circle 508 on Inquiry Card

# Little Impact.

## Meet the IMPs. A pair of stylish 3½ inch high impact printers that will look great on any desk.

Styled for desk top use, these sleek units stand just 3½ inches high, yet the unique fan-cooled printing system can knock out 80, 96 or 132 columns of crisp hardcopy with continuous throughput of one line per second.

**A winning pair.** IMP-1, with friction feed, can make multi-copies on plain 8½ inch wide paper, or on teletype rolls. In addition, IMP-2 has tractor feed and full forms control, with tractors adjustable from 1 inch to 9½ inches.

**Interfaces abound.** All IMPs have Centronics parallel and RS232C/20mA serial inputs as standard equipment. But if you need something different, then we make interfaces for just about any system — high speed serial, Apple, Pet, TRS-80, IEEE 488...

**Versatile, too.** 96 ASCII character set is standard. And you can select 6 character sizes, even graphics, under software control. Options include 2K buffering and special character sets.

**Service — a big difference.** No other printer manufacturer offers Axiom's combination of low cost and nation-wide service and distribution — in the USA and eighteen overseas countries.

**Pssst — the price!!!** It's low. $695 for IMP-1. $795 for IMP-2. And that's the single unit price.

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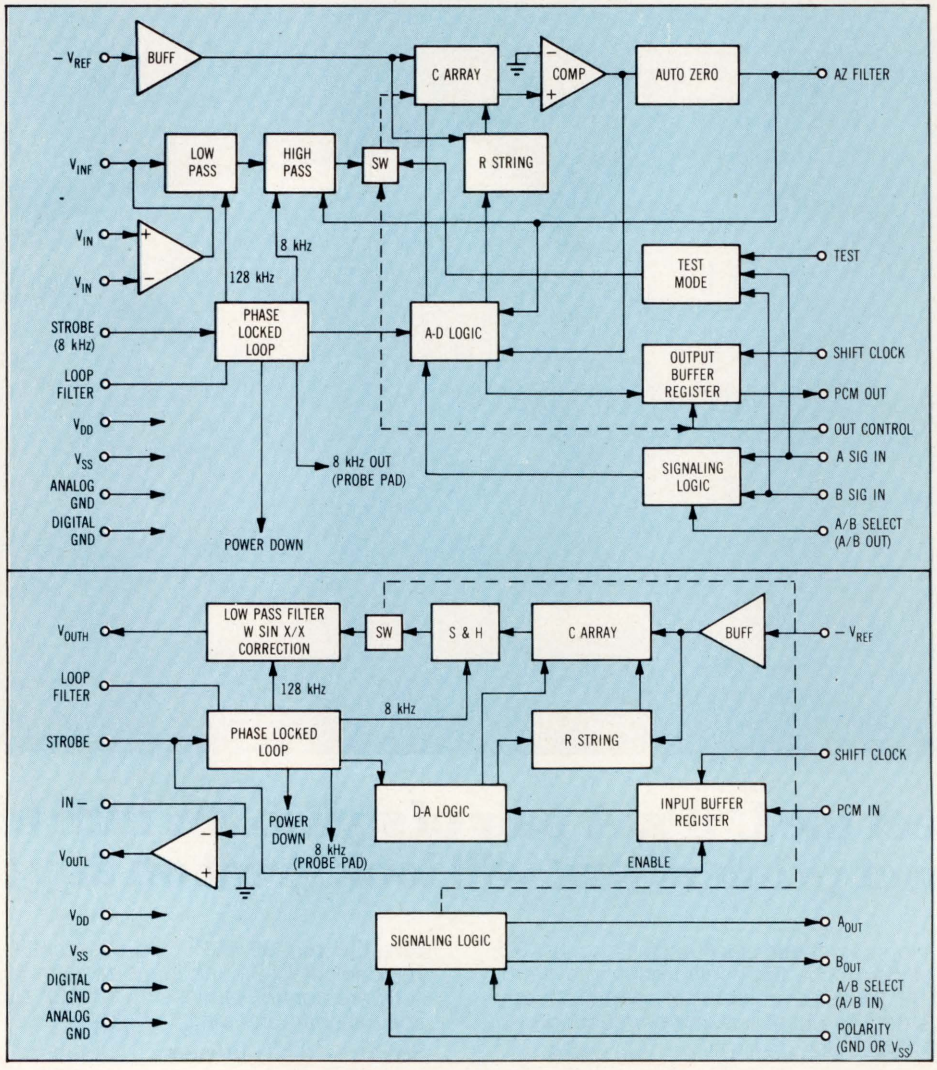
**CIRCLE 88 ON INQUIRY CARD**

## Two-Chip Codec Set Includes Filters




CMOS companding encoder (S3501, upper diagram) and decoder (S3502, lower diagram) from AMI constitute 2-chip codec set with onchip filters. Set meets or exceeds AT&T D3 and CCITT G.711 and G.733 specifications

A 2-chip CMOS codec set is partitioned into the S3501 encoder on one chip and the S3502 decoder on the other, each incorporating onchip filters. These circuits, from American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051, form a companding set designed to implement a per channel voice frequency coding conversion for PCM channel banks and PABX systems requiring a $\mu$-255 law transfer characteristic.

Each chip contains two sections, a band-limiting filter and an ADC or DAC that conforms to $\mu$-255 requirements.

Transmission and reception rates of 8-bit data words containing analog information can be arbitrary up to 32Mbits/s, with analog sampling at a nominal 8-kHz rate.

To reduce the pin count of their packages and facilitate machine insertion of the devices into PC boards, both chips generate all internal timing signals in a phase lock loop which uses the externally supplied 8-kHz strobe signal. This feature also simplifies an OEM's PC board design.

The 18-pin encoder chip includes a band-pass filter with D3 filter characteristics, an ADC that implements the $\mu$-255 law, control logic for CCIS and D3 signaling, an autozero loop which effectively nulls long term offsets in a system, and an uncommitted op amp for gain trimming and antialiasing. This device needs only one reference voltage and two noncritical power supplies ($\pm 5$ Vdc, typ).

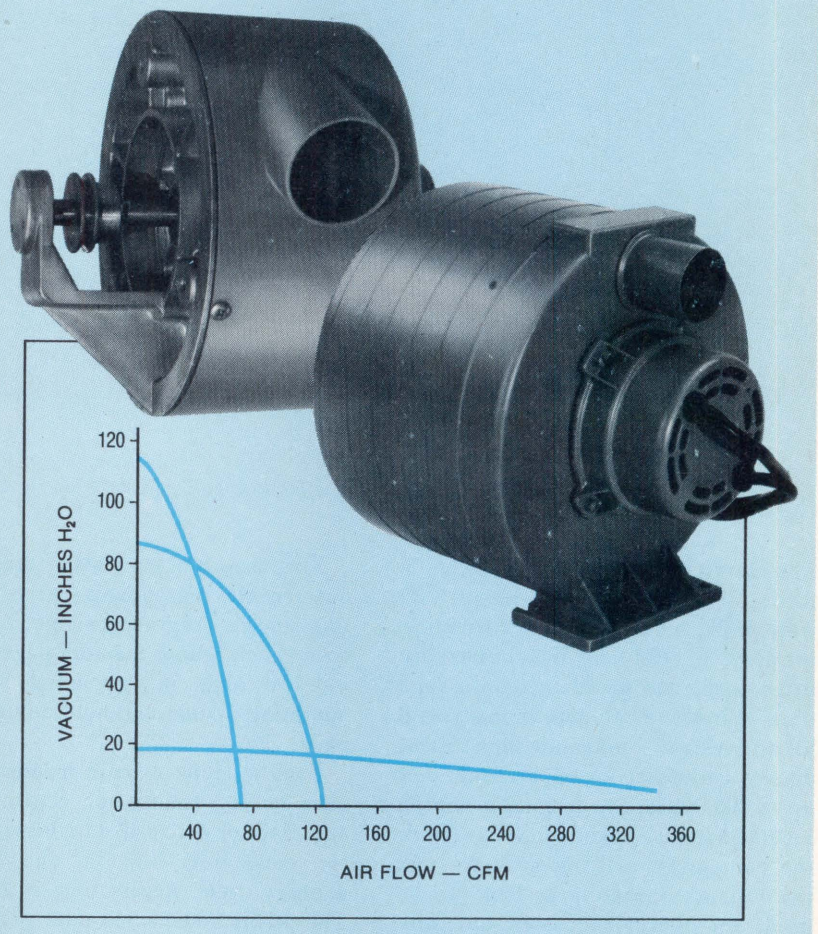
A sixth-order low pass elliptical filter followed by a third-order Chebyshev high pass filter constitute the band limiting filter. Loss below 65 Hz is at least 25 dB, which minimizes power and frequency induced noise. The ADC uses charge redistribution techniques to perform conversion, through a binary ratioed capacitor array and a linear resistor string.

Included in the 16-pin decoder chip are a DAC, a low pass filter with sin X/X correction, CCIS and D3 control logic, an uncommitted low impedance op amp for direct drive of a 600-Ω load and optional TTL or relay drive from the A/B signaling output. Its reference voltage and power supply requirements are identical with those of the encoder chip.

Both chips feature automatic power down in the absence of the 8-kHz strobe. If their phase lock loops sense an unlocked condition, the chips are forced into the power down mode automatically, to minimize power dissipation. Standby power dissipation is 15 mW per chip, vs typical operating power dissipation of 70 mW for the encoder and 55 mW for the decoder. □

Circle 509 on Inquiry Card


# Windjammer® blowers provide multi-function working air




**One air system for pressure, vacuum or both**

Windjammer high-performance blowers supply vacuum and/or pressure for a wide variety of jobs. Typical applications include tape transports, card sorting, vacuum hold down, air sampling and cooling.

These blowers are designed specifically for environments where high noise levels would be objectionable and feature carefully balanced components. They can be supplied for belt drive or complete with motor.

Lamb Electric engineers can work with you to develop a Windjammer system tailored to your requirements. And, we can schedule quantity deliveries to meet your production requirements. Contact AMETEK, Lamb Electric Division, 627 Lake Street, Kent, Ohio 44240. (216) 673-3451.

AMETEK
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CIRCLE 89 ON INQUIRY CARD

PRODUCTS

# High Performance Minicomputer

## Houses CPU and Magnetic Peripherals in Single Cabinet

The Harris 80 minicomputer system is made up of a 24-bit word length CPU with 192k bytes of error correcting memory, an 80M-byte Winchester disc drive, and a low profile magnetic tape unit—all in one cabinet. As many as 8 disc drives and 4 magnetic tape drives, on one controller for each group, and up to 32 interactive terminals can be included in an expanded system. Both the company's existing software and the VULCAN operating system can be used. An operator console CRT provides a communication link between operating system and operator.

### Operating Features

Bus transfer rate for the CPU is up to 19M bytes/s with 48 data lines plus 18 address lines. Address bits allow access to all of main memory by any subsystem using the bus.

Real memory expands from 192k to 768k bytes, and a hardware supported virtual memory system provides over 6M bytes of space, with both hardware and software memory protection. Each program page in memory is protected against access or inadvertent destruction by another concurrently executing program; and pages containing instructions and constants, as opposed to variable data, are hardware write protected, even within the same program.

Virtual memory in this system does not require reorganizing or compacting since a program does not have to occupy contiguous memory pages. Any physical page not occupied by the operating system can hold any logical page.

Each module of main memory contains its own timing and control logic and reads or writes 48 data bits plus error correcting bits in one 400-ns memory cycle. Access time is 290 ns. The 48-bit system bus data path provides high speed, direct memory access (DMA) input/output (I/O) between each memory module and universal block channels (UBCs).

Up to 24 logical I/O channels interface the central system bus to device controllers. The UBC is a block mode DMA channel for peripheral controllers. In scan mode, a UBC supports two concurrent I/O operations; in scan-lock mode, it operates as a single DMA channel. In addition, the UBC functions as a programmed I/O channel transferring data under CPU/program control between a CPU register and the channel. A 48-bit data buffer is contained for each logical channel.

An optional scientific arithmetic unit provides concurrent floating point arithmetic operations independent of the CPU. Double-precision (48-bit) floating point uses an 8-bit signed exponent and 39-bit signed mantissa, resulting in over 11 decimal digits of precision.

### Software

VULCAN, a priority structured, demand paged, multiprogramming operating system, concurrently supports multistream batch processing, interactive timesharing, data base management, remote job entry, and realtime operations. This operating system works with paging hardware to monitor and direct memory allocations.

Support is provided for nine languages, five programs, a programmable interactive command language, five remote job entry and two remote batch terminal packages, and a data base management system with an information retrieval system. The languages supported are an extended BASIC language processor, FORTRAN IV compiler, FORTRAN 77 compiler, extended 1974 ANSI COBOL compiler, APL interpreter, RPG II compiler, macro assembler, SNOBOL 4 interpreter, and FORGO (load-and-go FORTRAN). Support programs consist of a sort/merge package, VULCAN indexed sequential package, system accounting, cross reference, and VULCAN symbolic debugger. *(continued on page 176)*

*High-Speed Static RAMs . . .*

# 2147s with lower power consumption. Available in volume. Now. From Texas Instruments.

Now your reliable second-source for industry-standard 2147s is even better.

Because TI's 2147s consume less power than before. About 27% less.

And they're fast. We've got a 55-ns TMS2147-5. The TMS2147-7 and the even lower standby power TMS21L47-7 clock in at 70 ns.

High speed. Low power. Good availability. An unbeatable combination. For all your buffer/cache, process control, visual display and a wide range of other high-speed memory applications. For mainframes and minis and micros.

For optimum cost/performance effectiveness, TI's 2147s are manufactured using improved state-of-the-art SMOS (scaled MOS) N-channel technology.

Each device in the TMS2147 series is offered in a high-density, 300-mil, 18-pin DIP. Pinout is industry standard 4K x 1 static RAM.

| Device | Max Access (ns) | Max Power (mW) Active | Standby |
|---|---|---|---|
| TMS2147-5 | 55 | 715 | 165 |
| TMS2147-7 | 70 | 632 | 110 |
| TMS21L47-7 | 70 | 632 | 55 |

Improved 2147s from Texas Instruments. Available in production quantities. Now. Call your nearest TI field sales office or authorized distributor.

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85137

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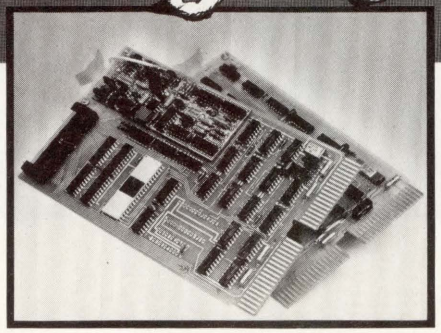

**Use Megalink™ for 1 Megabit/sec DMA transfer between as many as 255 DEC and Intel processors on local networks up to 32,000 feet long.**

- **Q bus, Unibus, and Multibus compatible units plug directly into DEC and Intel backplanes.***
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## Technical Specifications

Data transfer rate for the disc subsystem is 1.2M bits/s. Access times are 55 ms max, 30 ms avg, 7 ms min; latency times are 16.7 ms max, 8.3 ms avg. The automatic loading magnetic tape subsystem uses a 7 to 10.5″ (17.8 to 26.7-cm) reel, features a phase encoded (IBM and ANSI compatible) recording mode, and has a 9-track, 1600 char/in (630/cm) data density. Tape velocity is 25 in (63.5 cm)/s in read/write mode, 100 in (254 cm)/s rewind.

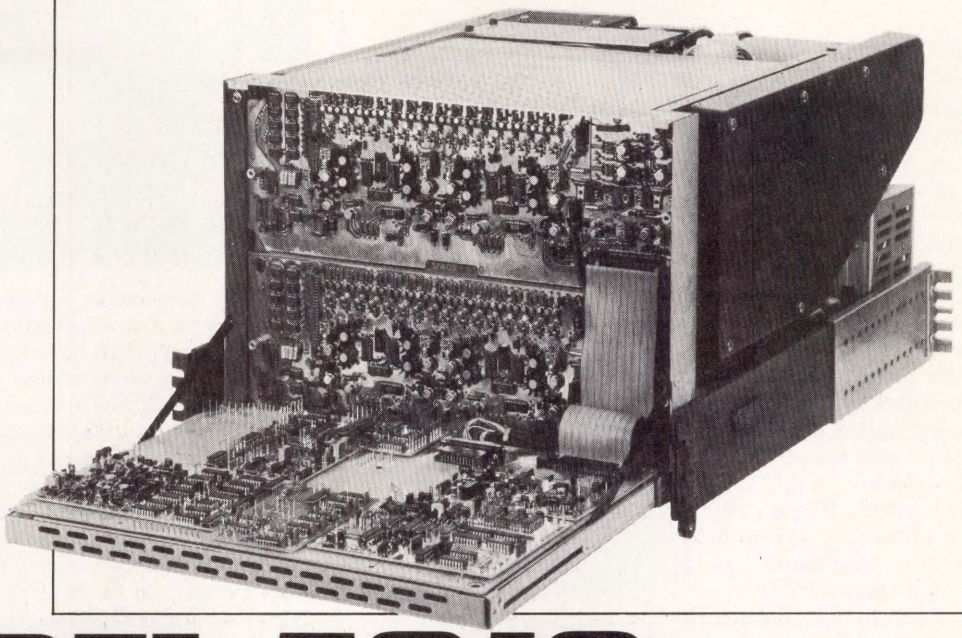
Electrical requirements for a single-cabinet configuration of CPU, memory, and channels are 230 or 208 Vac ± 10%, single-phase, 4-wire (std) or 220/240 Vac, single-phase, 3-wire (optional); 60 ±3 Hz (std) or 50 ±3 Hz (optional), and 12 A rms at 230 V (max). Temperature ranges for CPU, memory, and channels are 50 to 113 °F (10 to 45 °C) operating at 20 to 80% relative humidity non-condensing and 32 to 122 °F (0 to 50 °C) storage at 20 to 90% RH. Forced air cooling is provided by internal fans on each chassis. Altitude limitations are −1000 to 6000 ft (−300 to 1830 m) operating and −1000 to 15,000 ft (−300 to 4570 m) storage. However, limitations on currently used disc and magnetic tape subsystems cause effective temperature ranges to be 50 to 95 °F (10 to 35 °C) operating and 40 to 122 °F (4.4 to 50 °C) storage and the operating altitude range to be sea level to 6000 ft (1830 m).

## Price and Delivery

An entry level Harris 80 minicomputer consisting of CPU, 192k bytes of main memory, 80M-byte Winchester disc subsystem, single magnetic tape subsystem, and cabinet plus a separate terminal is priced at $74,950. OEM discounts are available on this and expanded configurations. Deliveries will begin in November of this year. Harris Corp, Computer Systems Div, 2101 W Cypress Creek Rd, Ft Lauderdale, FL 33309. Tel: 305/974-1700.

**For additional information circle 199 on inquiry card.**

# RELIABILITY: 28,000 hr. MTBF.
# ECONOMY: .035 cents per bit.



# VRC MODEL 4016 MEMORY

| | |
|---|---|
| CAPACITY . . . | 37.9 million bits |
| BIT RATE . . . . | 4.33 MHz |
| ACCESS TIME | 8.5 m/sec. |
| DIMENSIONS | Height – 12¼" (31.2 cm.) |
| | Width – 17½" (44.5 cm.) |
| | Depth – 22" (55.9 cm.) |
| MEAN TIME TO REPAIR . . | Less than 1 hr. |

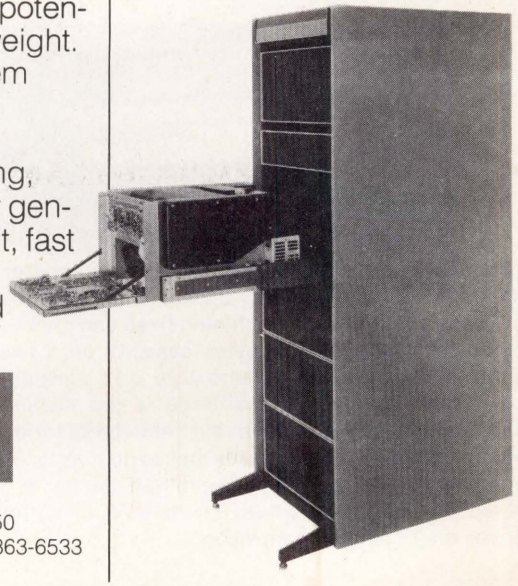
When it comes to speed, reliability and low cost, systems users in 25 countries in every continent of the world depend on the VRC 4016 head-per-track memory.

It features a fail-safe actuation system that eliminates the potential of media damage and data loss. It's compact and lightweight. All electronics, drive components and head retraction system are mounted outside the drum, making service simple and eliminating risk of contamination.

Applications are endless. Telecom and message switching, process control of all kinds, geophysical exploration, power generation, news editing, typesetting. Wherever low cost-per-bit, fast access and high data storage capacity are required.

For proven reliability, worldwide support, field service and predictable high quality, you can rely on VRC.

Write or call for complete details on the Model 4016 head-per-track memory...a simple, rugged, compact unit to improve the reliability of your system.



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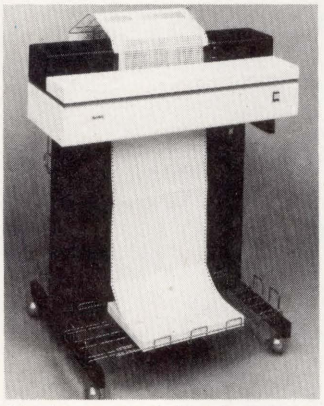
CIRCLE 92 ON INQUIRY CARD

# PRODUCTS

## Dot Matrix Printer/Plotter Produces 4 Colors in Single Pass

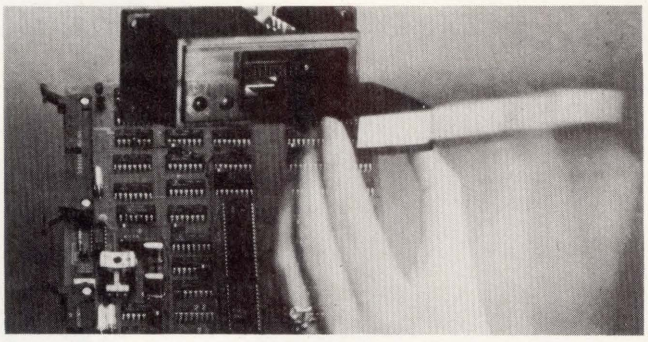
Microprocessor controlled model 4100 uses separate cartridge ribbons and printheads for each primary color plus black to produce full color or black and white hardcopy graphics on plain paper. The device switches quickly between graphics and alphanumeric modes, operating at three times the speed of comparable units. Separate magenta, cyan, yellow, and black ribbons and separate printheads allow readable black text to be obtained without changing ribbons and avoids ribbon contamination and resulting color muddiness.



Controlled by a Z80 microprocessor, the unit prints in a subtractive process, light colors first from a raster refresh graphics system. Maximum resolution is currently 60 dots/linear inch, horizontal or vertical. Plotting speed in full color graphics mode averages 3 pages/min for 11″ (28-cm) forms. Characters are printed in a 5 x 7 dot matrix at 60 lines/min. The unit operates in continuous motion to avoid the effect of rapid acceleration and deceleration. Self-diagnostic routines incorporated in the microprocessor facilitate maintenance. Use of microprocessor control, dc motors, and stepper drive paper advance reduce parts count and simplify maintenance. Life cycle of ribbons is extended because of reduced contamination. **Ramtek Corp,** 2211 Lawson Lane, Santa Clara, CA 95050.

Circle 200 on Inquiry Card

## Bubble Memory Cassette System Eliminates Paper Tapes and Cards



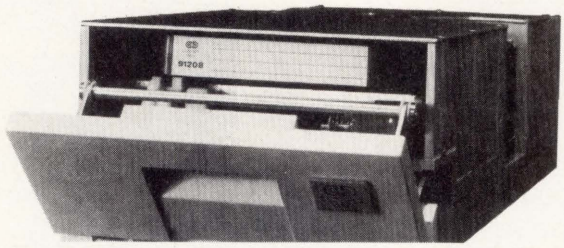
Portable, detachable bubble memories that operate in the same way as a tape cassette works with a tape recorder, the FBM31CA and 43CA have total capacities of 74,032 and 273,745 bits and provide access times of 740 ms max and 6 ms average, respectively. Cassettes connect to an 8-bit microcomputer through a cassette holder and a card incorporating a monitor program. Absence of moving parts eliminates need for preventive maintenance.

The system consists of a bubble memory cassette that allows the device to be loaded and unloaded quickly, a cassette holder unit, and a controller that interfaces to the host system. Up to eight cassette holder units can be controlled with one interface unit. The holder incorporates linear circuit, coil driver, function driver, sense amplifier, write inhibition devices, and busy check circuit. 8-bit parallel data can be processed (DMA possible) TTL compatible with the interface.

Cassettes have a transfer rate of 100k bits/s and operating power consumption of 500 and 700 mW for 31CA and 43CA, respectively. Packaged in a 24-pin housing, dimensions are 60 x 45 x 20 mm, and weight is 50 g. Power requirements for the U001 holder are 5 V, 0.4 A; 12 V, 0.25 A; 17 V, 0.1 A; and −5 V, 0.1 A. Control card 308C1A requires 5 V, 1.5 A; 12 V, 0.25 A; and −12 V, 0.1 A. **Fujitsu America, Inc,** 910 Sherwood Dr-23, Lake Bluff, IL 60044.

Circle 201 on Inquiry Card

## Rigid 8″ Disc Drive Combines Fixed and Removable Storage



The model 9455 Lark Module Drive offers an alternative solution to problems of memory backup confronting users of fixed 8″ (20-cm) disc drives. Combining fixed and removable storage modules, it provides 8M-bytes capacity on a fixed disc and another 8M bytes on a removable disc cartridge. The self-contained sealed 91208 cartridge is top loading for stable alignment of media to drive, but front loads for easy use. The unit's 9.67-MHz transfer rate makes it interface and format compatible with the 14″ (35.5-cm) SMD family. It can be combined with storage module, minimodule, or cartridge module drives on a common controller.

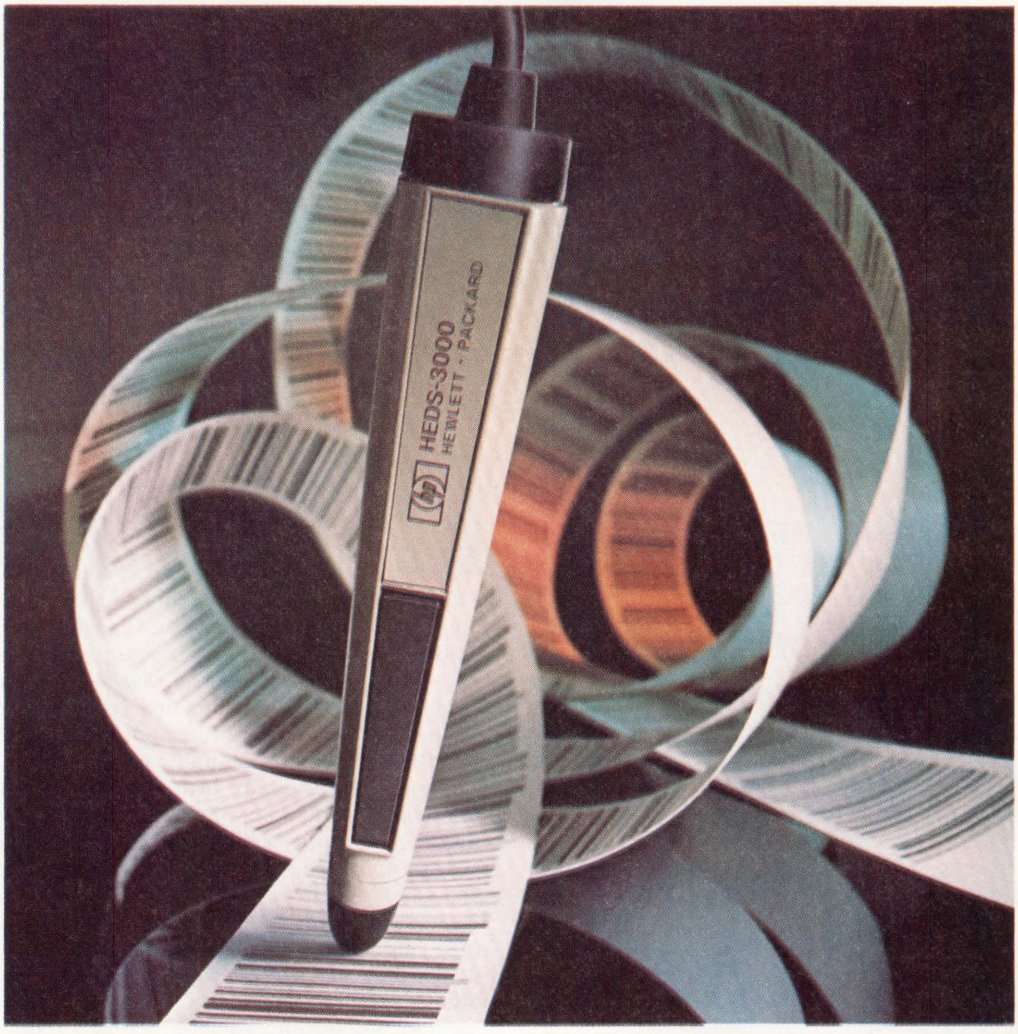
Micromodule drive and power and I/O modules are the unit's two major assemblies. Included in the drive are disc assembly, spindle motor, linear voice coil actuator, operator control panel, and basic electronics assembly. The PIO contains power supply system and interface electronics to the controller. The data recovery circuitry operates with fixed sector formats in 64- or 32-sector configurations.

The unit's low mass flying read/write heads attach to a precisely controlled linear head positioner. Servo information is factory written on each data surface for carriage positioning, index and sector pulse generation, and phase-locked oscillator reference clock.

An 8M-byte removable single-disc cartridge, the 91208 consists of an oxide coated disc clamped to a hub and encased in a plastic housing. Both surfaces are used for data and servo positioning and index/timing. The cartridge is enclosed in a plastic housing with head access door which is opened by the door actuator arm when the cartridge is inserted and closes automatically on removal. Track density is 237/in (93/cm) and there are 202 primary data tracks/surface. **Control Data Corp,** PO Box O, Minneapolis, MN 55440.

Circle 202 on Inquiry Card

# SURPRISE!




## HP Introduces the World's First Digital Bar Code Wand.

Anyone now using a keyboard or push buttons for data entry could benefit from using bar codes. Depending on the number of characters being entered, bar code scanning has been shown to be from two to four times faster than key entry.

HP's new HEDS-3000 Digital Bar Code Wand can scan black-and-white bar codes and convert the codes to microprocessor-recognizable digital output. Fully specified and guaranteed, the Wand contains a push-to-read switch which conserves power. It is well suited to portable systems as well as those with line power. The Wand is housed in a rugged, stylized, molded plastic case with attached cord and connector. Of even further interest to OEM's, the HEDS-3000 can be manufactured in custom colors with desired logos.

In quantities 1-99, the Wand is priced at $99.50* each.

For more information or immediate off-the-shelf delivery, contact your nearest HP Components franchised distributor. In the U.S. contact Hall-Mark, Hamilton/Avent, Pioneer Standard, Schweber, Wilshire or the Wyle Distribution Group (Liberty/Elmar). In Canada, call Hamilton/Avnet or Zentronics, Ltd.

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*U.S. Domestic Price Only

CIRCLE 93 ON INQUIRY CARD

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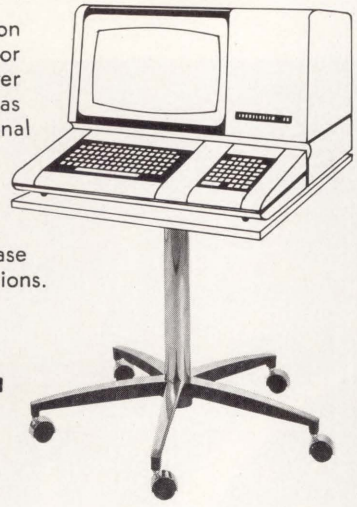
You can count on Est for stationary or movable computer stands that are as sturdy and functional as they are handsome. Your choice of style and anchor plate. Let us design a base to your specifications.



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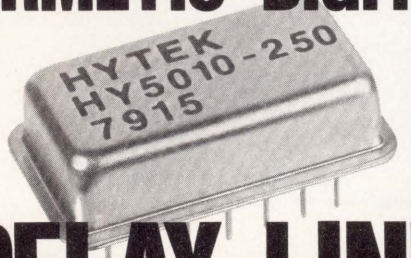
CIRCLE 94 ON INQUIRY CARD

# HERMETIC DIGITAL




# DELAY-LINE

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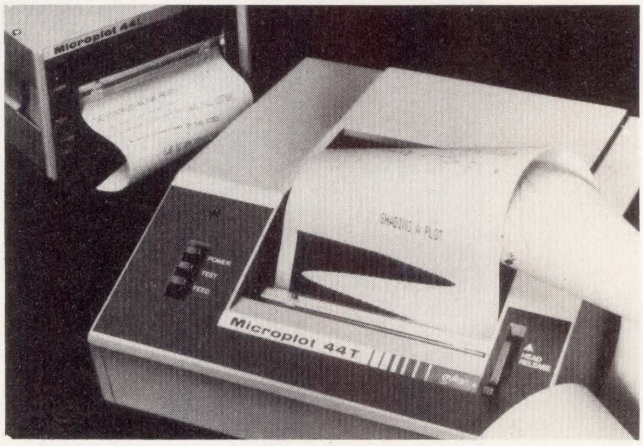
CIRCLE 95 ON INQUIRY CARD


# PRODUCTS

## Thermal Graphic Printer Uses Thick Film Linear Dot Array Technology




Equipped with a fully programmable graphics interface, Microplot 44 allows print and plot capabilities to be intermixed without burdening the microprocessor based system with unnecessary software overhead. Available in either desktop or panel mounted versions, the unit accepts analytical and computational data in digital form, prints both grid and scale, and plots data. The 44-col unit will also annotate data with alphanumerics and print text in either X or Y orientation. The printer/plotter incorporates a fixed head design using thick film linear dot array technology, which provides high print clarity with no moving parts and offers high abrasion resistance and quiet operation.

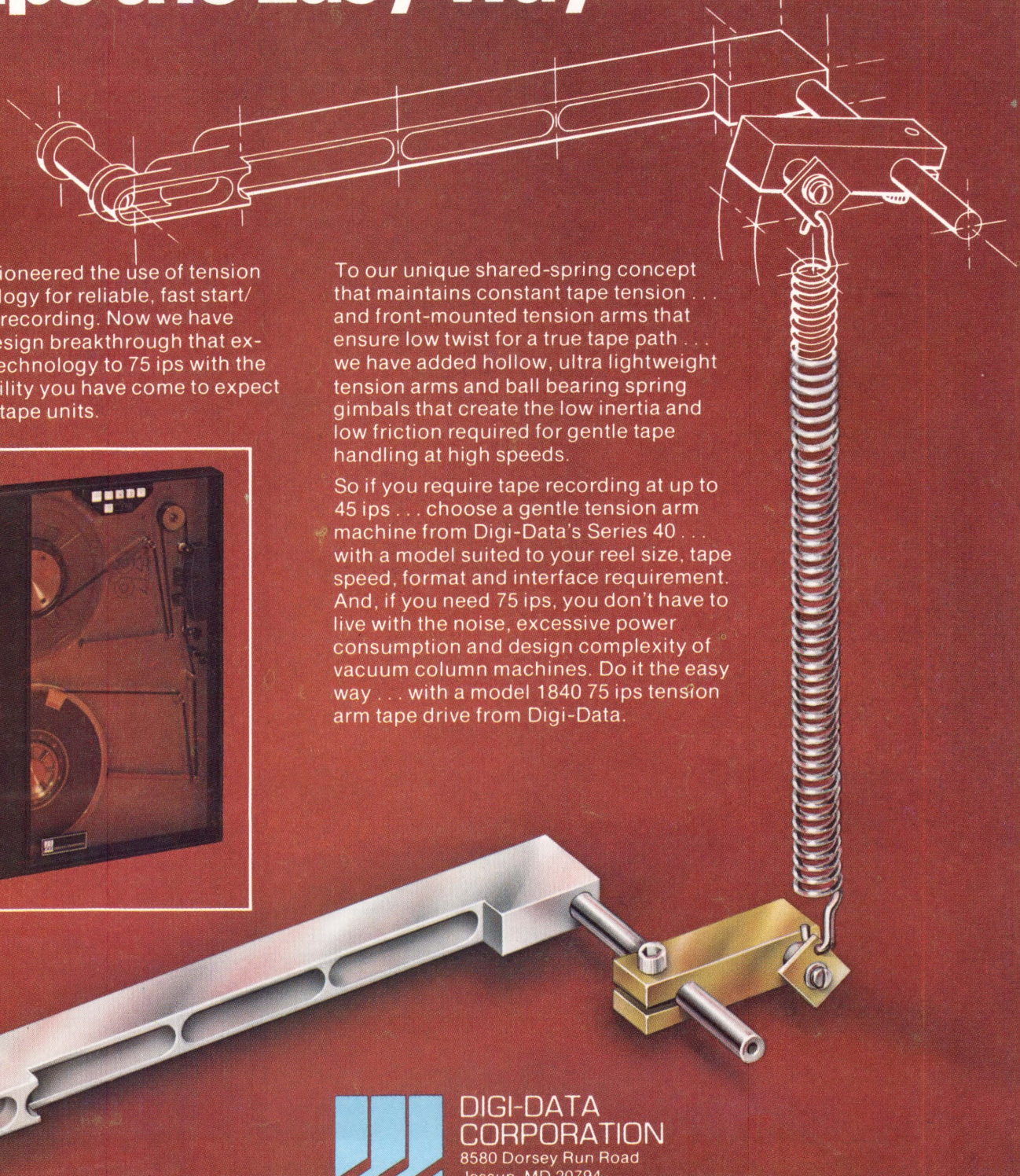
Microprocessor based electronics supply the unit with its fully programmable parallel graphics interface. The bit parallel/byte serial interface is organized for compatibility with other microprocessor based systems. Data are loaded into memory one dot or character line at a time. The 3-part data buffer—256-byte plot data, 44-byte X-axis, and 22-byte Y-axis—allows simultaneous X and Y printing, plotting, and annotating. Since each of the plot buffer's 256 bytes corresponds to a single dot location on the printhead array, each dot can be randomly accessed. This provides ability to slew to any dot position via a single data byte transfer, eliminating the need to sequentially load data as it increases in magnitude and to load blank data bytes for spacing.

The unit also operates in line segment plotting mode, whereby the operator specifies horizontal vectors by their endpoints and the unit plots data between points. Character printing modes include double height and double density, one-half height, and X- or Y-axis orientation. Backspace capability allows intermixing of character printing and plotting on same line. All mode selections can be manual or programmable.

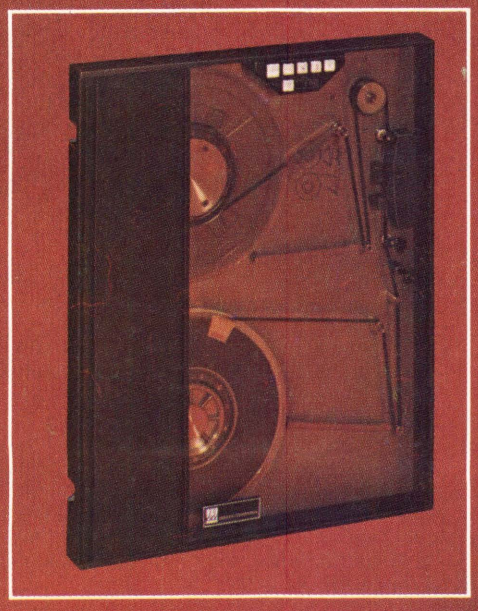
Providing a 256-dot linear array across a 109-mm plotting width, the unit uses 127-mm wide thermal printing paper. It operates on 115-Vac, 50/60 Hz and requires 25 W idle, 80 W max, or 25 to 50 W typ. Dimensions are 99 x 180 x 231 mm for the panel mount version: 109 x 251 x 292 mm for the desktop unit. **Gulton Industries, Inc, Measurement & Control Systems Div,** East Greenwich, RI 02818

Circle 203 on Inquiry Card

# Digi-Data's Tension Arm Design Breakthrough Brings You 75 ips the Easy Way



Digi-Data pioneered the use of tension arm technology for reliable, fast start/stop digital recording. Now we have achieved design breakthrough that extends that technology to 75 ips with the same reliability you have come to expect from 45 ips tape units.



To our unique shared-spring concept that maintains constant tape tension . . . and front-mounted tension arms that ensure low twist for a true tape path . . . we have added hollow, ultra lightweight tension arms and ball bearing spring gimbals that create the low inertia and low friction required for gentle tape handling at high speeds.

So if you require tape recording at up to 45 ips . . . choose a gentle tension arm machine from Digi-Data's Series 40 . . . with a model suited to your reel size, tape speed, format and interface requirement. And, if you need 75 ips, you don't have to live with the noise, excessive power consumption and design complexity of vacuum column machines. Do it the easy way . . . with a model 1840 75 ips tension arm tape drive from Digi-Data.

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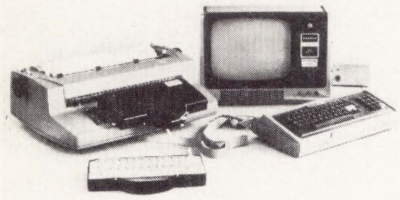
CIRCLE 96 ON INQUIRY CARD

# PRODUCTS

## COMPUTER-TYPEWRITER INTERFACE



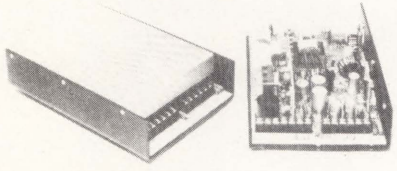
Designed to generate hard copy directly from a computer through any electric typewriter with powered carriage return, the I/O Pak consists of an array of coils positioned in the same pattern as the typewriter's keyboard. Unit fits directly over the keyboard, and coils are wired into electrical decoding matrix. Interfaces and software are available for TRS-80 level 1 and 2 and Apple level 2; a 6-bit parallel interface allows operation with other computers. **Rochester Data, Inc,** 3100 Monroe Ave, Rochester, NY 14618.
Circle 204 on Inquiry Card

## POWER SUPPLIES FOR DATA COMMUNICATIONS EQUIPMENT

Power supplies with outputs of 5 Vdc at 0.30 A and ± 12 Vdc at 0.13 A, or 5 Vdc at 0.60 A and ± 12 Vdc at 0.20 A, are available for either 117- or 220-Vac input. Intended for microprocessor based data communications applications, the external design eliminates heat buildup, interference, and space requirements experienced with integral devices. Line/load regulation is ± 5%, with <10-mV rms ripple. **Ault, Inc,** 1600H Freeway Blvd, Minneapolis, MN 55430.
Circle 205 on Inquiry Card

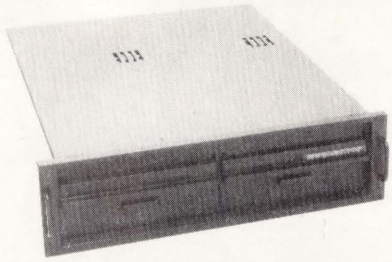
## 95-W SWITCHING POWER SUPPLY

Outputs from the 95-W EPS95 switcher are 5 Vdc at 12 A, – 5 Vdc at 0.5 A, and either ± 12 Vdc at 1.5 A or ± 15 Vdc at 1.2 A. The supply is available in either open or enclosed frame models. Included are 90 to 125/180 to 250-Vac dual input ranges, current limiting with automatic recovery after removal of short circuit, and power fail circuitry. Efficiency of the unit is greater than 70%. **Elpac Power Systems,** 3131 S Standard Ave, Santa Ana, CA 92705.



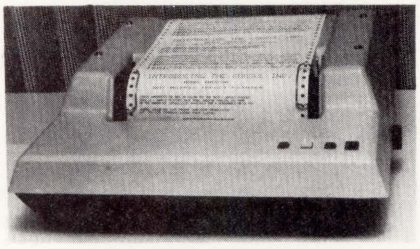
Circle 206 on Inquiry Card

## DUAL FLOPPY DISC SYSTEM



Consisting of MM-SBC-80F controller, cables, two 8″ (20-cm) disc drives, and power supplies, reconfigured Megabox can provide up to 2M bytes of storage. The Multibus compatible controller can handle up to 4 Shugart 800/850 type 8″ (20-cm) floppy drives in both single- and double-density modes. The system runs ISIS II, CP/M, MP/M, Pascal, or OASIS operating systems. **Micromation, Inc,** 1620 Montgomery St, San Francisco, CA 94111.
Circle 207 on Inquiry Card

## DOT MATRIX IMPACT PRINTERS



Available in kit or assembled form, the 88-col, tractor feed dot matrix printer is microprocessor controlled and programmable with 32 system level commands. Included are 96 ASCII characters (u/lc), 9 software selectable print sizes, 5 x 7 through 10 x 14 fonts, serial and parallel interfaces, selectable 110- to 9600-baud rate, and adjustable tractor width for paper size selection. **Coosol, Inc,** 1585-200 Adams Ave, Costa Mesa, CA 92626.
Circle 208 on Inquiry Card

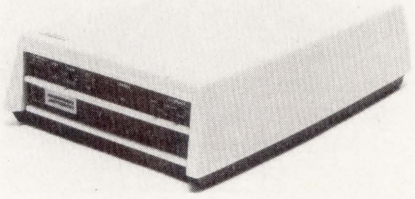
## MULTIPLE-WALL HEAT SHRINKABLE TUBING

Insultite$^{R}$ MW tubing combines heat shrinkable protection with encapsulation to keep out moisture, oils, and corrosive environments. The multiple-wall tubing is a combination of a radiation cross-linked polyolefin outer wall with an inner wall that melts at temperatures over 135 °C, shrinking the outer wall and compressing the inner wall, simultaneously insulating and encapsulating. It is manufactured in 8 std diameters from 0.125 to 1″ (3.175 to 25.4 mm). **Electronized Chemicals Co, Div of High Voltage Engineering Corp,** S Bedford St, Burlington, MA 01803.
Circle 209 on Inquiry Card

## ALTERNATIVE TIME BASE DISPLAY OSCILLOSCOPE

The 100-MHz/5 mV, dual-trace, PM3262 oscilloscope offers an improved CRT that produces a sharper display coupled with higher writing speeds. Alternate time base display facility shows main and delayed time base displays together over the entire screen width. A third channel allows for simultaneous viewing of trigger signals. The 21.1-lb (9.6-kg) scope measures 12.5 x 6.1 x 16.2″ (316 x 154 x 410 mm). Power consumption is 45 W. **Philips Test & Measuring Instruments, Inc,** 85 McKee Dr, Mahwah, NJ 07430.
**Circle 210 on Inquiry Card**

## SHORT-HAUL DATA SET



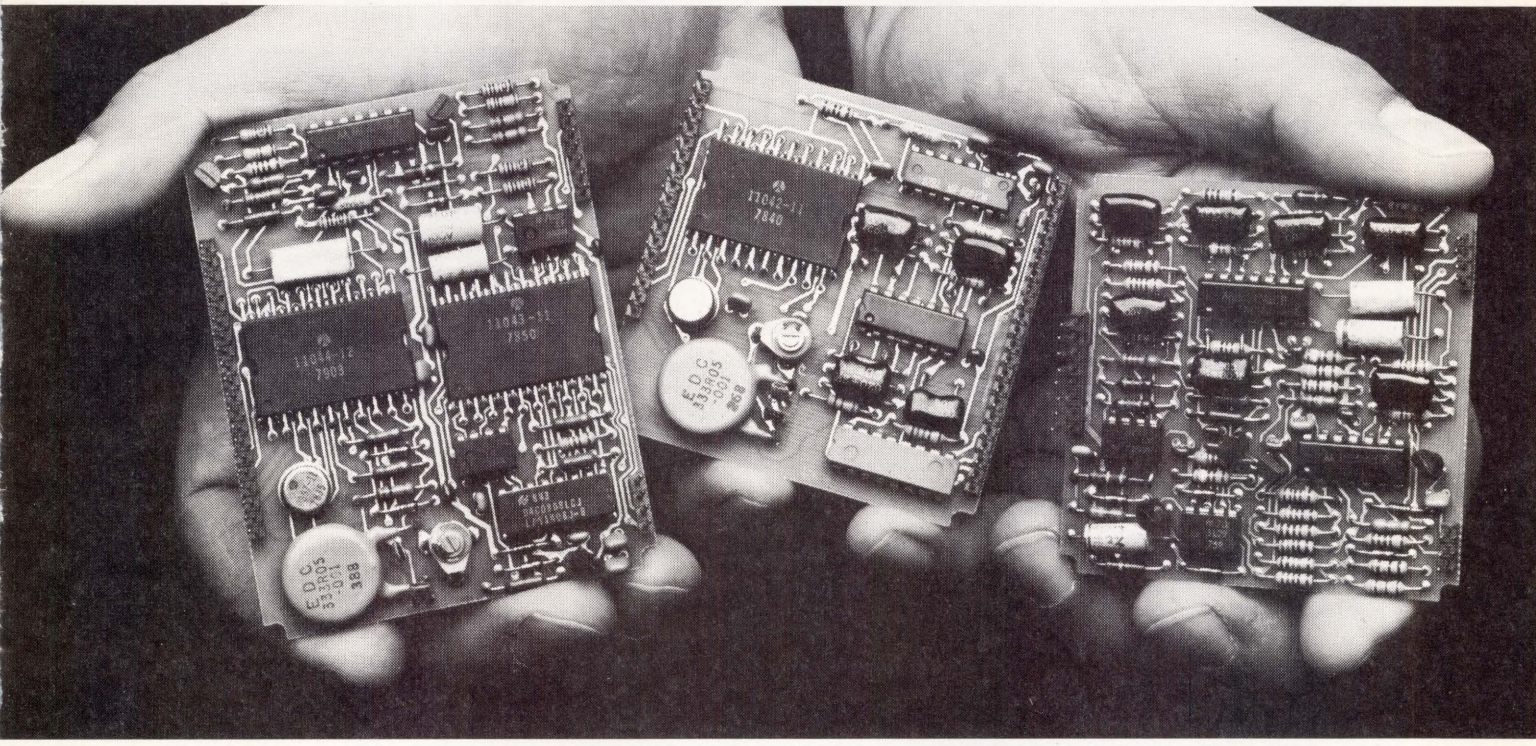
Designed for asynchronous data transmission at 0 to 9600 bits/s, model 1050 provides high speed data exchange in either half- or full-duplex systems. Transmission through twisted pair cable at distances of up to 28 mi (45 km) is possible, depending on data rate and wire gauge used. Available diagnostic capabilities allow local and remote tests of data sets as well as communications links. **Anderson Jacobson, Inc,** 521 Charcot Ave, San Jose, CA 95131.
Circle 211 on Inquiry Card

## PCM SYSTEM TEST GENERATOR

PCG-1 digital signal generator produces accurate and repeatable DSX-1 compatible PCM signals. Functions tested include insertion loss or gain, level tracking, and signal distortion and frequency response. A pseudorandom noise option simulates noise in a 350- to 550-Hz band. Std digital signal or encoded sinewave test tones (50 to 3600 Hz) are provided. **W & G Instruments, Inc,** 119 Naylon Ave, Livingston, NJ 07039.

Circle 212 on Inquiry Card

# R24. The first 2400 bps modular modem.



## Rockwell's compact MOS-LSI modem gives new physical design freedom.

Micro Power

Rockwell's R24 Modem is the most compact 2400 bps MOS-LSI modem available today. Its small size and modularity give designers a whole new form factor flexibility. Requiring only 25 square inches of system area, the R24 is ideal for terminals and communications equipment.

The R24 provides functional flexibility also. Of its 3 modules, one is the transmitter, two the receiver. Terminal designers can offer transmit-only or receive-only options. And, the R24 is Bell 201 B/C and CCITT V.26 and V.26 bis compatible.

With its major functions in LSI circuits, the R24 is solid-state reliable and economical. It can be configured for operation on either leased lines or the general switched network. And, each low-profile module can be plugged into standard connectors or wave soldered onto system PC boards.

A new generation of modems from the company that's delivered more high-speed modems than anyone in the world. That's Rockwell Micropower!

For more information, contact Modem Marketing, Electronic Devices Division, Rockwell International, P.O. Box 3669, RC 55, Anaheim, California 92803. (714) 632-5535.

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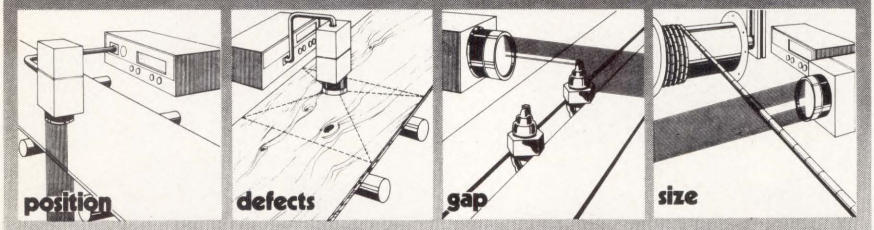
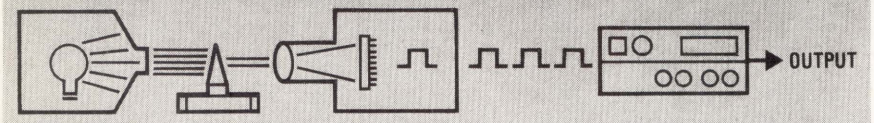
CIRCLE 97 ON INQUIRY CARD

# LOOK AT YOUR PRODUCTS WITH A NEW EYE!

## Image Sensing Systems from Reticon

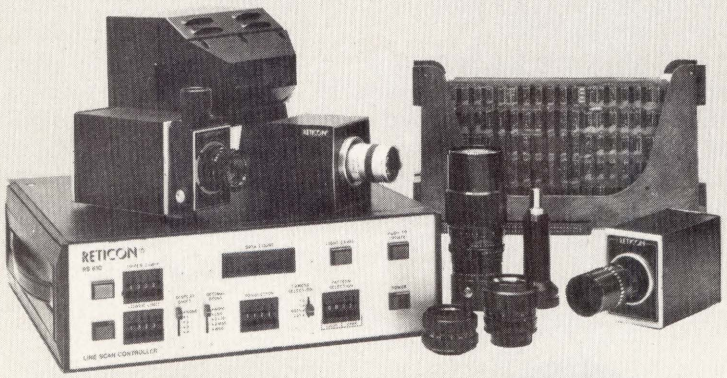



***Unlike film cameras, an image is focused on an array of photodiodes which are precisely aligned on a single chip located inside the camera. This photodiode array converts light energy into corresponding electronic signals. The intelligent controller uses these signals to collect production information, process data, make process decisions, and talk to computers and control equipment.***

Reticon Image Sensing Systems can be configured for practically any production application requiring non-contact inspection, measurement, detection, counting, sorting or monitoring. Choose the system components you need from a broad range of line scan or matrix cameras, lenses, illuminators, power supplies and intelligent controllers. There are even Interface Units that connect cameras to SBC–80 Computer Systems. And you can modify or expand your system to meet changing requirements.

Reticon's experience and technical services can help you define an imaging system that's right for your requirements. Write or phone for our applications brochure that describes our systems approach.




EG&G RETICON

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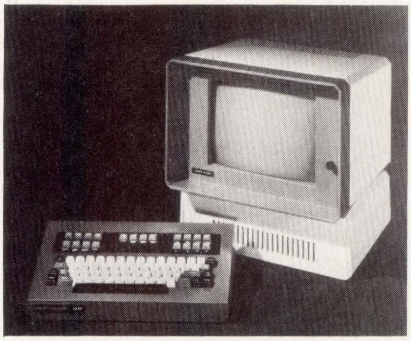
## PRODUCTS

### VIDEO DISPLAY EDITING TERMINAL



Model 1250 Super Owl offers a choice of 2 detachable keyboards, and/or a light pen. Both configuration details and 12 (shiftable to 24) function keys are programmable. Information is stored in a nonvolatile EAROM. 25th status line allows 2-way communications with the host without interfering with the current transaction. Std printer port is RS-232-C compatible at a baud rate independent of the main communication lines. **Perkin-Elmer Corp, Terminals Div,** 360 Rte 206 S, Flanders, NJ 07836.

Circle 213 on Inquiry Card

### COMPUTER CONTROLLED CARD EMBOSSING SYSTEM

The Cardwriter III is comprised of a Farrington CRT terminal and an embosser/controller. Format and message are variable with each card; outer perimeter of the embossing can be 0.25″ (0.318 cm) from card edges. Card throughput is 60/h based on 3 lines of ANSI format at 1.25 char/s. The unit will accept CR50, CR70, or CR80 size cards. Std 64-char drum includes 10 OCR 7B numerals, 26 alpha plus 11 repeated char, 10 numerics, and 7 punctuation marks. **Dymo Business Systems, Inc,** Randolph Industrial Pk, Randolph, MA 02368.

Circle 214 on Inquiry Card

### 9600-BIT/s OEM MODEM

Packaged on $<100$ in$^2$ (650 cm$^2$) PCB space, unit allows full duplex communication over 4-wire 3002 circuit and is CCITT V.29 compatible. Fallback to 7200 or 4800 bits/s is provided. Carrier freq is 1700 Hz ($\pm 0.01\%$), with line impedance of 600 Ω. Device is transformer coupled, with transient protection. Digital interface conforms to RS-232-C/CCITT V.24. LSI circuits handle digital operations involved in data communications. Modem control resides entirely in software. **Universal Data Systems,** 5000 Bradford Dr, Huntsville, AL 35805.

Circle 215 on Inquiry Card

# CENTRONICS COVERS THE COURT

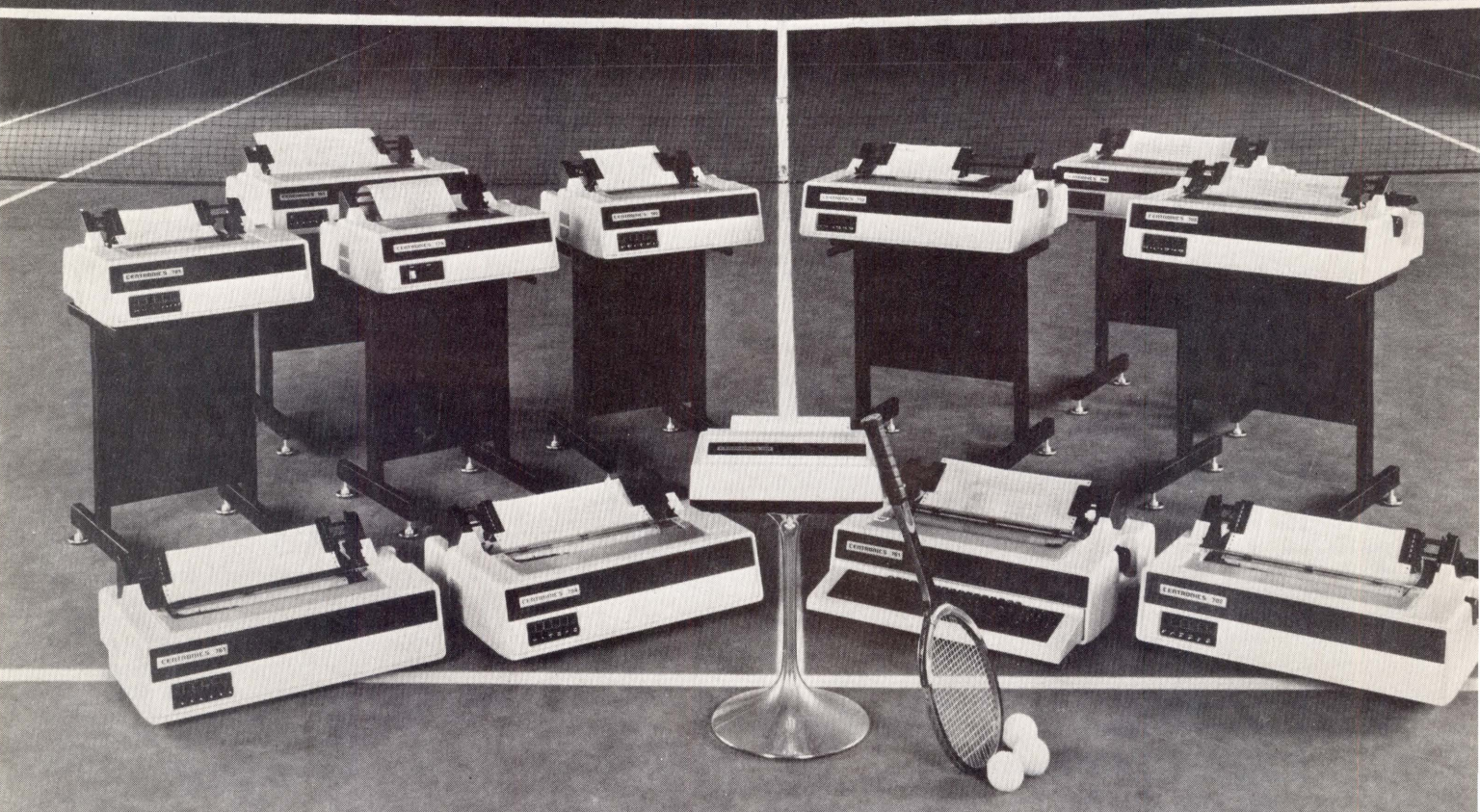
## ...with new, low-priced printers for small businesses

Now small businesses can have the advantage of Centronics performance. We have new models to meet the needs of small businesses—a selection that covers the court. And we've followed-through by pricing them **lower** than other printers that can't match Centronics' features and reliability.

**TOP-RANKED TEAM** We understand your small business needs—that's why Centronics has sold more printers to the small business market than anyone else. We have new, fully-featured models designed for small business applications. High throughput for inventory control. Full 132-column width for accounts receivable. Versatile forms handling capability for invoicing, payroll, and statements. Plus excellent print quality for labels and listings. The bottom line: with Centronics, small businesses can have mainframe performance at micro prices.

**READY FOR ANY TOUR** These printers are designed to deliver maximum in-service time, a key consideration for a small business. And we have the largest worldwide service organization of any independent printer company.

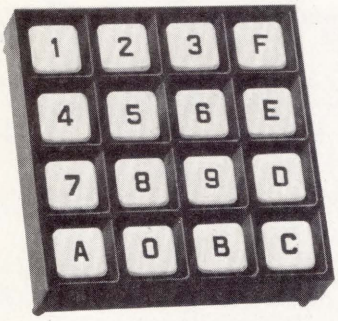
**DON'T WRITE**—phone Bob Cascarino today at (603) 883-0111, extension 4032, or contact any of our 15 U.S.A. or 9 international sales offices. Centronics Data Computer Corporation, Hudson, New Hampshire 03051.



**CENTRONICS® PRINTERS**
...the advantage

CIRCLE 99 ON INQUIRY CARD

# Grayhill 12 & 16 Button Keyboard Pads



## Choice of circuitry.

- XY Matrix
- single pole/common bus
- 2 out of 7 (or 8) coded output

Readily interfaced with logic circuitry.

## Outstanding performance characteristics.

Positive tactile and audible feedback, low profile, patented snap-action dome contact, and 3 million operation per button contact system life-rating.

## Standard product features.

½ inch or ¾ inch button centers. Total button travel of only .015 inch. Standard post or flange mounting; top or sub mounting. Molded of tough ABS plastic; buttons with black on white molded-in legends standard, other options available, including clear snap-on caps for user legending.

*Send for complete specifications, truth table, and information about our full line of Keyboard products.*

Grayhill INC

561 Hillgrove, LaGrange, IL 60525 (312) 354-1040


# PRODUCTS

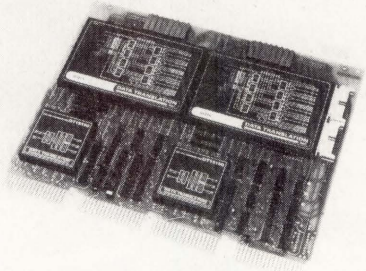
## VOICE RESPONSE VOLTMETER

The dual microprocessor based talking voltmeter automatically announces voltage readings via an internal 3″ (7.6-cm) speaker every 7 s or on command of the operator. A slave processor selects needed speech elements from ROM while the main processor handles system timing and signal processing. Powered by rechargeable NiCad battery pack, the 2.5-lb (1.1-kg) 2.5 x 10 x 9″ (6.4 x 25 x 23-cm) voltmeter has options including a liquid crystal display and foreign languages. **Franklin Institute Research Laboratory, Inc,** The Benjamin Franklin Pkwy, Philadelphia, PA 19103.

Circle 216 on Inquiry Card

## SINGLE-BOARD, 8-CHANNEL 12-BIT DAC

Mounted on a DEC std quad-height board, the DT1716 features 8 independent channels of 12-bit D-A conversion, each of which operates solely under PDP-11 program control and includes an individual, 16-bit data input register organized to appear as 8 consecutive read/write locations in the I/O address page. Resolution is 12-bit, with 0.02% nonlinearity and ± ½ LSB differential linearity. Converters are monotonic over the 0 to 70 °C operating range. **Data Translation Inc,** 4 Strathmore Rd, Natick, MA 01760.



Circle 217 on Inquiry Card

## 100-W SWITCHING POWER SUPPLIES

SF series power supplies consist of 5 models, each providing 100 W of regulated dc output power. Available voltage/current configurations are 5 Vdc at 20 A, 12 Vdc at 8.4 A, 15 Vdc at 6.7 A, 24 Vdc at 4.2 A, and 28 Vdc at 3.6 A. Totally enclosed packaging, 115/230-Vac input capability with 20% tolerance, ±0.05% line and load regulation, and holdup time ratings of 20 ms min, are std features. **Power-One, Inc,** Power One Dr, Camarillo, CA 93010.

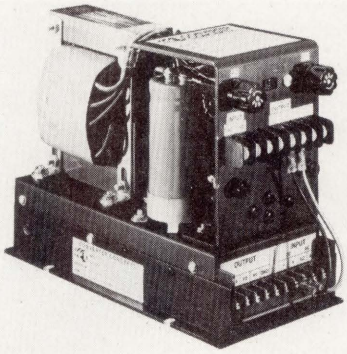
Circle 218 on Inquiry Card

## SONIC DIGITIZER

Model GP-6-50 enables users to perform axis rotation and slope calculations and to digitize in polar as well as cartesian coordinates, and allows extension into transcendental operation. Incorporating microprocessor capability, the unit also provides origin offset, incremental mode, area and line length calculation, and alphanumeric ASCII menu capability with variable scaling selection. Unit is housed in a chassis that adapts to rack mounting or tabletop installation. **Science Accessories Corp,** 970 Kings Hwy W, Southport, CT 06490.

Circle 219 on Inquiry Card

## AUTOMATIC SWITCHOVER POWER SYSTEM



Designed to operate in conjunction with the company's 1-, 2-, and 3-output dc-dc converters and a 24-V battery, LS1000 series UPS and battery charger system automatically switches from ac line to battery backup during power failures. Output regulation remains transient free during switching to battery or back to normal supply. Transition time from line to backup is 1 μs. Input is 115/230 Vac, 47-440 Hz. Unregulated output is 36 Vdc at 3 A. **Converter Concepts, Inc,** 435 S Main St, Pardeeville, WI 53954.

Circle 220 on Inquiry Card

## 80/300/675M-BYTE DISC STORAGE SYSTEMS

3100 series storage systems employ a microprocessor based single-board controller to emulate Data General's Zebra series 6057/6060/6061 disc systems. Up to 4 CDC storage module drives, 80/300/675M bytes each, may be daisy chained for a total capacity of up to 2700M bytes. Dual CPU capability option is provided for configuring redundant systems. The controller mounts within the minicomputer using one I/O slot. **System Industries,** 525 Oakmead Pkwy, Sunnyvale, CA 94086.

Circle 221 on Inquiry Card

# THE MOST FIELD PROVEN IS NOW THE MOST VERSATILE.

## *Telex introduces the new Tri-Density 6250 Tape Subsystem for OEM's.*

In 1978, Telex introduced and delivered the first high speed 6250 BPI tape transport for OEM mini-computers. It lets you compact more data. In less space. At faster speeds. Since then we've built up more field proven reliability than any other 6250 OEM tape drive manufacturer.

Now this rack-mounted 6200 Series tape family has been expanded to include the 6253 tri-density tape subsystem. The high performance drive and formatter combines three densities—6250 BPI (GCR), 1600 BPI (PE), and 800 BPI (NRZI)—into a single unit. And as with all 6200 models, tape speeds of 50, 75 or 125 IPS are available. Telex formatters attach up to four 6200 Series drives and up to eight with an expansion option.

One key to the reliable operation of the 6200 Series is our patented Supr-Lite™ Capstan. It weighs only 1.9 grams, and combined with our patented new tape path, lets us use a smaller, more efficient drive motor. Tape handling at high program rates is improved.

Most importantly, the 6200 Series now offers you extreme versatility in matching and field converting a wide range of features and system options. The 800/1600 BPI dual density model 6240 can be easily field upgraded to tri-density. And such options as a 360/370 channel adaptor, high altitude and seismic feature, and dual speed capability will enhance your system configurations and performance many times over.

For more information about the 6200 Series—including its price/performance competitiveness—call your nearest Telex OEM representative. Or phone our OEM Marketing Department in Tulsa at (918) 627-1111.

***The innovation continues...*** **TELEX®**

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CIRCLE 101 ON INQUIRY CARD

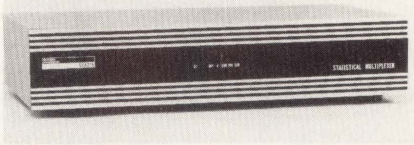
## DIGITAL DATA RECORDER FOR IEEE-488 STD BUS

GPIB-3000 digital cartridge subsystem provides data storage in compliance with ANSI/ECMA/ISO standards. Data are recorded serially at 1600 bits/in (629/cm) in a 4-track format. Up to 34.5M bits (4.3M bytes) of unformatted data storage may be contained on a DC 300 XL tape cartridge. The microprocessor based controller is designed to interface a TDC-3000 recorder to other IEEE-488 devices. **Innovative Data Technology,** 4060 Morena Blvd, San Diego, CA 92117.
Circle 222 on Inquiry Card

## TTL-IEEE STD BUS COUPLER

The 2488A interfaces instruments by translating their bit-parallel or serial codes, signals, or data into the bus serial, byte parallel format. In operation, the coupler provides all necessary functions to interconnect the instrument with a bus controller and/or other instruments. It can operate as a listener, a talker, or both. Passive cabling interconnects the instrument to the coupler. **Ballantine Laboratories, Inc,** PO Box 97, Boonton, NJ 07005.
Circle 223 on Inquiry Card

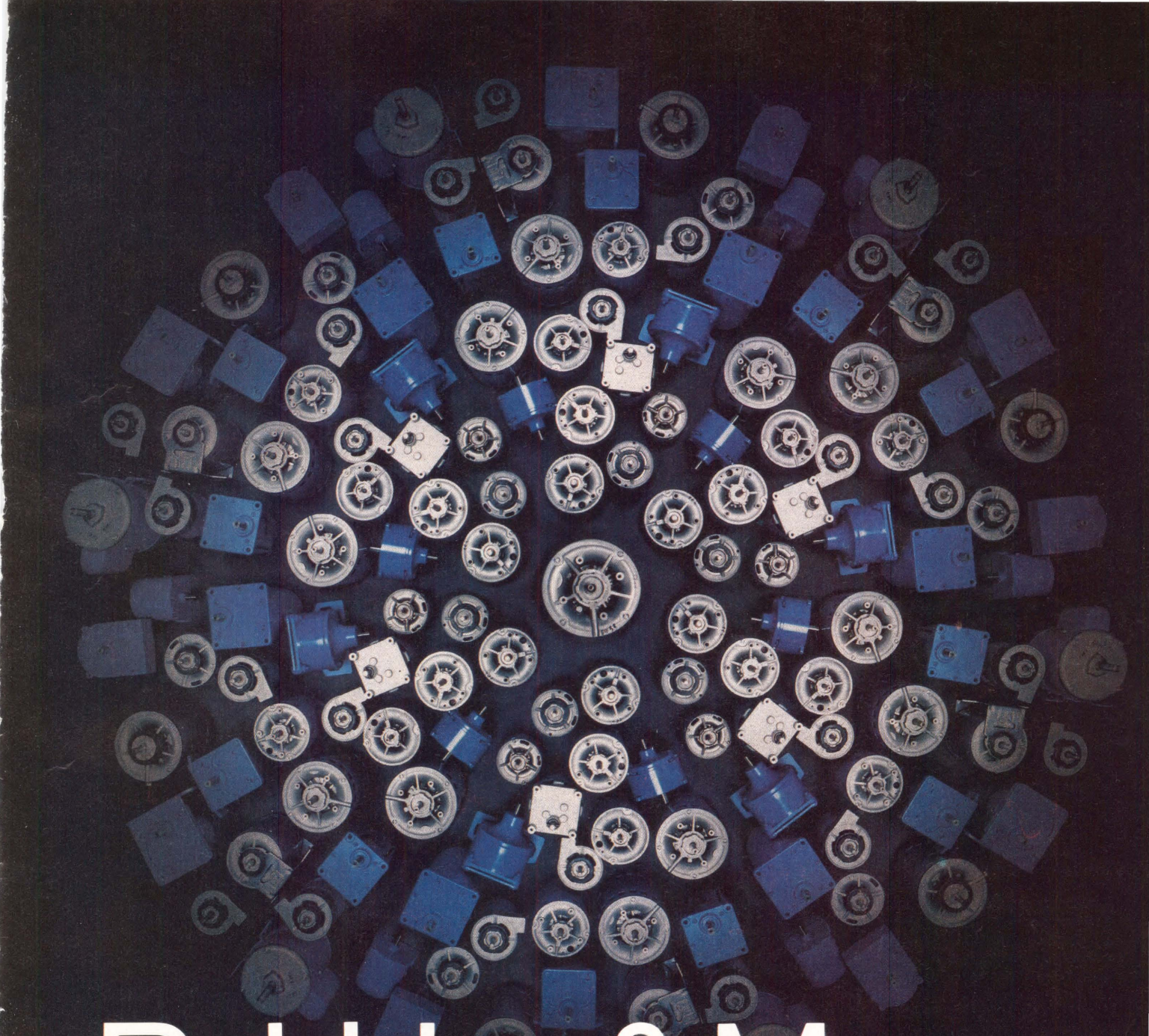
## STATISTICAL MULTIPLEXER



DCX815 family uses statistical multiplexing for compact, error free transmission of up to 8 asynchronous channels over a single composite link. The unit provides an unrestricted intermix of input speeds from 50 to 9.6k baud asynchronous for any 5-, 6-, 7-, or 8-bit Baudot, ASCII, or IBM code. Only active channels are assigned time slots. Error checking routing protects the link between multiplexers from transmission errors. **Rixon Inc,** 2120 Industrial Pkwy, Silver Spring, MD 20904.
Circle 224 on Inquiry Card

## 3-FORMAT TAPE CASSETTE DATALOGGER

Minilogger™ DL-42 records data in ASCII format, with elapsed time in days, hours, minutes, and seconds measured by the unit's crystal controlled, internal digital clock to a tested accuracy of better than 0.01%. Recorded data may be formatted as BCD, full alphanumeric, or binary. The tape drive is capable of recording up to 100k ASCII char. An RS-232 option outputs data to a terminal or printer. **A D Data Systems, Inc,** 200 Commerce Dr, Rochester, NY 14623.
Circle 225 on Inquiry Card



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Make your special motor out of standard pre-tooled parts. We specialize in subfractional HP motors and gearmotors for OEM applications. Our production motors will fit your product like the prototype, to let you design for maximum efficiency and reliability. You thus avoid excesses in power, structure, and cost. We have millions of permutations of standard designs and parts already proved in manufacturing. Let us match your application needs. Call us today. Or ask for Bulletin D-1120. Electric Motor Division, Robbins & Myers, Inc., 1949 Lagonda Ave., Springfield, OH 45501. Tel. 513-327-3329.

ROBBINS MYERS

*7 lamination sizes × 16 electrical types × 18 mounting types × 6 bearing systems × 4 frame sizes × 160 gear ratios = 7,741,440

CIRCLE 103 ON INQUIRY CARD

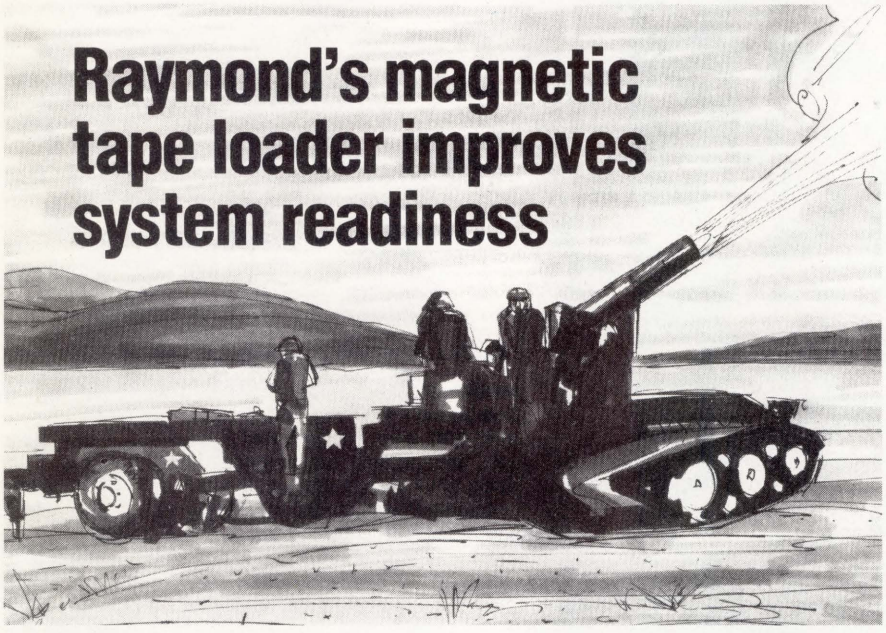
## PRODUCTS

### MONOCHROME CRT DISPLAYS

DT12-LF and DT12-ZF are 12″ (30.5-cm) monochrome displays for OEMs of industrial computer related equipment. These "Z power" displays provide low voltage dc required for the terminal logic circuits from the display horizontal deflection circuit. DT12-LZ has a flux-nulled 120/240-V line transformer to minimize CRT flux interaction. Scan derived terminal supply voltage is essentially constant from 98- to 134-Vac input. DT12-ZF has 120-Vac input, with its power supply driven by line operated regulator and horizontal circuits. **Zenith Radio Corp,** 1000 Milwaukee Ave, Glenview, IL 60025.

Circle 226 on Inquiry Card


# Raymond's magnetic tape loader improves system readiness



Model 6420 MTL

**. . . for digital program loading in severe military environments −54°C to +95°C**

Military system designers cannot gamble that program memory will always be available when needed. Whatever form that memory takes — core, bubble or semiconductor — designers insist on the most reliable military back-up memory available — magnetic tape. And for more than a decade, Raymond tape memories and program loaders have been the choice of these professionals, as demonstrated on over 60 military systems.

Raymond's Model 6420 MTL is specifically designed for data entry and program load applications, and features the smallest, lightest sealed cartridge available today. Proven military environment performance, outstanding reliability and cost effectiveness are just some of the reasons that Raymond continues as the leader in high quality magnetic tape memories. For more information on the 6420, or on how you can give your system the readiness edge, contact Raymond Engineering Inc., Military Recorder Division, 217 Smith St., Middletown, CT 06457 (203) 632-1000.

**RAYMOND ENGINEERING INC.**
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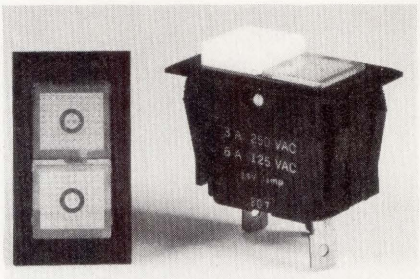
### PUSHBUTTON SWITCHES FOR ROCKER SWITCH MOUNTS



These pushbutton switches are interchangeable with rocker switches and fit standard mounting holes for the latter. Current ratings are up to 20 A either ac or ac/dc. Illuminated red, green, or amber models are available with 110-Vac neon, and 14- or 28-Vdc incandescent bulbs. Non-illuminated types are white, red, or black. Features of the 1- and 2-pole switches include interlocking pushbutton actuators, with solder lug, spade, and screw termination. **Eaton Corp, Commercial Controls Div,** 4201 N 27th St, Milwaukee, WI 53216.

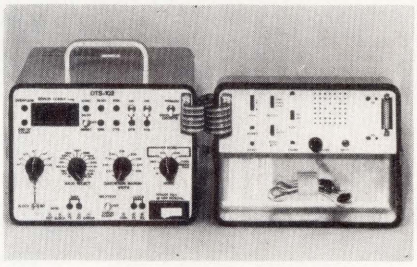
Circle 227 on Inquiry Card

### 300-BIT/s FULL-DUPLEX DIRECT CONNECT MODEM CARD

All circuitry for the VS300P is contained on a 5 x 6.35″ (12.7 x 16.12-cm) board and provides for switched-network, 300-bit/s full-duplex operation. Registered for direct-connect, the modem is fully compatible with Bell 103/113. Terminal interface is B-series CMOS input compatible, with output circuits capable of driving 2 TTL loads. The modem plugs directly into telephone company data and voice jacks. **Racal-Vadic, Inc,** 222 Caspian Dr, Sunnyvale, CA 94086.

Circle 228 on Inquiry Card

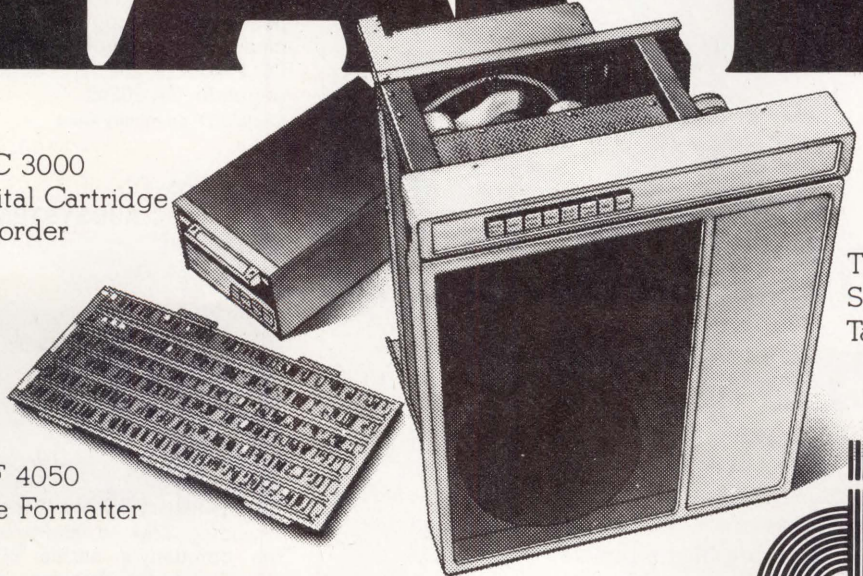
### DATA TRANSMISSION TEST SET



Portable DTS-102/TDM analyzes modem performance, measures turnaround time, and pinpoints cause of faulty RS-232/V.24 communication system operation. It provides 7 selectable output patterns and is programmable to generate start/stop characters containing pseudorandom, alternate, mark, or space data. Useful in synchronous, asynchronous, or start/stop character oriented systems such as TDMs, it measures bit or block error rate and displays turnaround time measured in milliseconds. **Navtel Ltd,** 8481 Keele St, Concord, Ontario L4K 1B1, Canada.

Circle 229 on Inquiry Card

# APE FOR TAPE?



TDC 3000
Digital Cartridge
Recorder

TDI 1050
Synchronous
Tape Transport

TDF 4050
Tape Formatter

A lot of people are, these days.

And our Synchronous Tape Transports, Digital Cartridge Recorders, and Formatters are three big reasons.

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It's a matter of record.

INNOVATIVE DATA TECHNOLOGY

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San Diego, CA 92117
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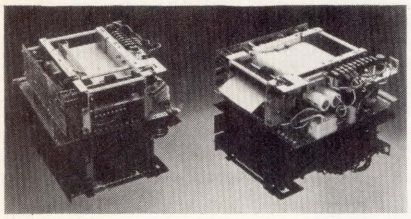
CIRCLE 105 ON INQUIRY CARD

## PRODUCTS

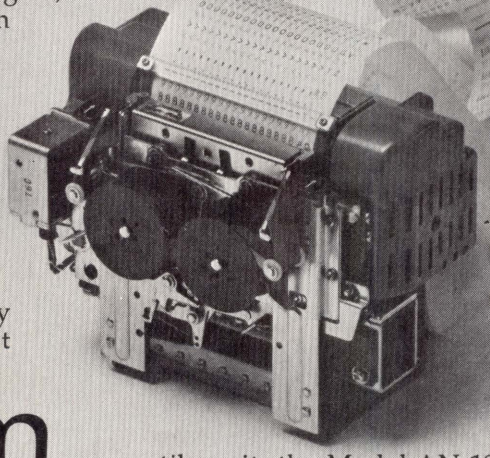
### TAPE/TICKET IMPACT PRINTERS



Tape printer models offer choice of 6- or 12-col formats with mechanical unit, and optional BCD interface electronics. Ticket printers offer 5- or 11-col formats with or without BCD interface electronics. Std open frame units are supplied with taps for 12-Vdc, 117-Vac, or 220-Vac power inputs; laboratory models are wired for 117 Vac. Std ticket provides 3 copies with 2 carbon overleafs: top copy is pressure sensitive paper, second copy is std bond, and third is a TAB card. **Smith & Wesson,** 2100 Roosevelt Ave, Springfield, MA 01101.
Circle 230 on Inquiry Card


# Workhorses.

Sometimes you need a dependable workhorse that will do the job efficiently, reliably, day after day. Like the compact drum printers from C. Itoh. Our Model 102 18-column digital, for example, weighs in at only 3.3 lbs., but it's more dependable than many units costing far more. Or our Model EP-101: it's at home in a lot of applications, but, like all our drum printers, it doesn't take much power—only 17 VDC. Or our most



# Drum printers from C. Itoh.

versatile unit, the Model AN-101F alphanumeric, the perfect OEM printer for anything from computer output to label printer to data logger. And more. Every one is solid, dependable, and right for any application where a minimum of downtime is a prime requirement; each features two-color printing, a compact design suitable for bench top or rack panel mounting, and one more dependable thing: the C. Itoh brand.

**C. Itoh Electronics, Inc.**

*C. Itoh means excellence in printers.*

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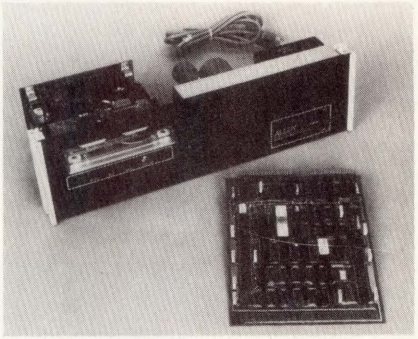
### CARTRIDGE TAPE BACKUP SUBSYSTEM

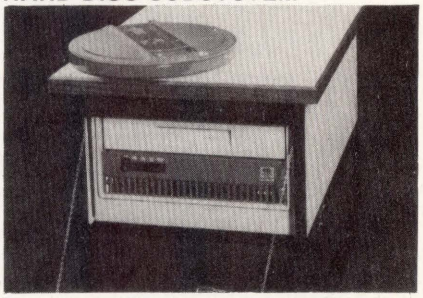


The DMN-1 cartridge tape subsystem features a 14M-bit storage capacity with a 0.9M-bit/min recording rate. Incorporating dual 6400-bit/in (2520/cm) 0.30 in (0.76 cm)/s data funnel tape drives, the 8085 based subsystem operates at a 20k-char/s DMA transfer rate. The unit requires only 5.25″ (13.34-cm) of vertical mounting space, using a single controller slot. **Alloy Engineering Co, Inc,** 85 Speen St, Framingham, MA 01701.
Circle 260 on Inquiry Card

### 6-BIT EVALUATION BOARD

The TDC1014PCB board contains all the necessary components to perform a 6-bit A-D conversion in 33 ns and accepts and digitizes a 1-V pk-pk signal from a 75-Ω source at rates from dc to 30M samples/s. Measuring 4.5 x 5.5″ (11.43 x 13.97-cm), the board includes its own 44-pin edge connector. A 2-bit input code permits output coding in true or inverted binary or 2's complement formats. **TRW LSI Products,** 2525 E El Segundo Blvd, El Segundo, CA 90245.
Circle 231 on Inquiry Card

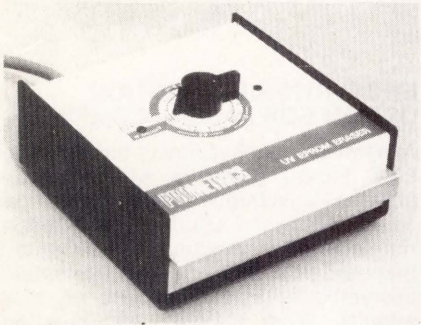
### 96M-BYTE HARD DISC SUBSYSTEM



Providing 32M- to 96M-byte storage for the company's series 8000 or 5000 microcomputer systems, the model 16 hard disc subsystem utilizes a fixed-removable disc drive. Included are a 16M-byte SMD technology cartridge for backup and a 16M-, 48M-, or 80M-byte fixed media employing Winchester 3340 technology. Also included is a model 490 hard disc controller that fully buffers one sector of data to and from the disc. **Industrial Micro Systems,** 628 Eckhoff St, Orange, CA 92668.
Circle 232 on Inquiry Card

## UV ERASER FOR EPROMs

Devices requiring 15 W-s/cm² erasure dosages such as 2708, 2716, 2732, 2758, 3728, and 8518 are erased in approx 20 min by the model 117A; devices erasable with lower dosage require correspondingly shorter times. An indicating scale shows time and dosage. Unit is in a leakproof housing, and an interlock turns off the UV source when the EPROM compartment is opened. Up to 5 EPROMs may be erased simultaneously. Power requirement is 110 to 125 Vac, 50/60 Hz, 30 W. **Prometrics, Inc,** 5345 N Kedzie Ave, Chicago, IL 60625.



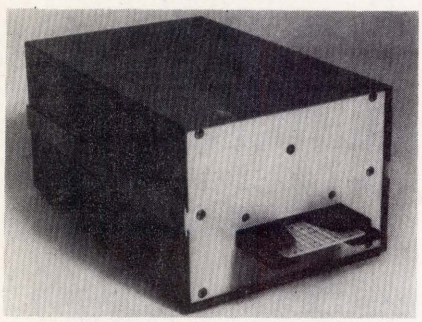
Circle 261 on Inquiry Card

## AC LINE PROTECTORS

DLP 5, 10, and 15 are a combination ac line conditioner and UPS. The -5, a 600-V-A inverter system coupled with an integral storage battery/charger system is capable of 120-V, 5-A, 60-Hz output for 6 min (60 min for the -5A). The units operate on 50/60-Hz input power at 120 Vac ±25% (230 Vac optional). Output power is 60 Hz ac (50 Hz optional) ±0.01%, at 120 Vac ±5%, with <5% total harmonic distortion. Ambient operating range is 0 to 45 °C. **Displex, Inc,** 21 Brewster St, Glen Cove, NY 11542. Circle 262 on Inquiry Card

## CARD/BADGE READER WITH RS-232-C TERMINAL

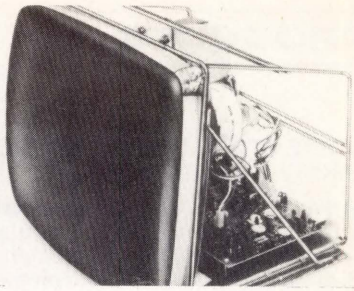
Self-contained series HT-100 terminal is designed for industrial applications in factory data collection systems, warehousing, and assembly floors. The terminals include power supplies and RS-232-C interface; flagging of operator errors make them virtually fool-proof. Data are asynchronously transmitted at rates of 150, 300, 600, 1200, 2400, 4800, or 9600 baud. **Taurus Corp,** Academy Hall, Lambertville, NJ 08530.



Circle 263 on Inquiry Card

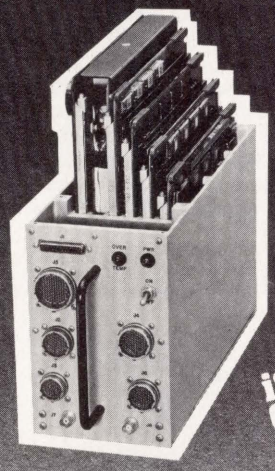
## WIREFRAME 15″ DISPLAY MONITOR

NDC-15 display monitor has 35-MHz video bandwidth, uniform focus characteristics, and horizontal frequency capabilities from 15,750 to 20 kHz. P4 phosphor is std, with P31 and P39 optional. The wireframe unit is electronically and mechanically compatible with Motorola and Ball Brothers monitors. Retrace times are >6 μs (horizontal) and >300 μs (vertical). **TSD Display Products, Inc,** 35 Orville Dr, Bohemia, NY 11716



Circle 264 on Inquiry Card


# Ruggedized Microcomputer



iSBC 80 Compatible

**It's Easy to Design Your Severe Environment System Using our Ruggedized Version of Intel's 80/10A Microcomputer and Versatile Support Modules.**

SECS 80 is a ruggedized version of Intel's iSBC* single-board computer. Even uses the same development system software.

Meets MIL-E-5400, 4158, 16400, making it perfect for military, avionics, and tough industrial environments.

SECS 80 comes with a multitude of support modules: RAM, ROM, EPROM, digital tape recorder and controller, 1553 interface, A-D converter, digital I/O, high-speed arithmetic unit, and more.

You can buy a complete system or configure your own with individual modules. Either way, this versatile microcomputer system will save you valuable time and development costs.

Phone or write for complete details today.

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**Telephone: (213) 998-9090 • Telex: 69-1404**

## PRODUCTS

### 32k-BYTE STATIC SEMICONDUCTOR MEMORY FOR PDP-8

PDP-8/A compatible, VM832 contains 32k 12-bit words on a single board and fits a hex-wide expander cabinet. When operated with the KT8A memory management option, onboard DIP switches allow each 4k memory field to be individually assigned to any field of 0 to 31. Access time is 280 ns and cycle time is 1.2 $\mu$s (KK8-E CPU) or 1.5 $\mu$s (KK8-A). Power requirements are 5 Vdc at 4.2 A. **Computer Extension Systems, Inc,** 17511 El Camino Real, Houston, TX 77058.

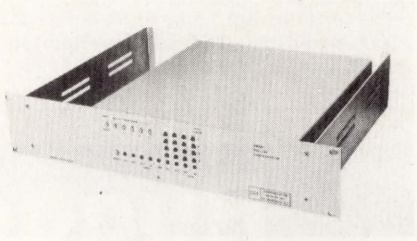
Circle 233 on Inquiry Card

### THERMAL CUTOFF DEVICE

Flat design of the M&TP thermal cutoff is particularly suited to 1-time protection of transformer or fractional-horsepower motor coils from catastrophic overheating. Inserted into or laid flat on or under coils during manufacture, the device opens the electrical circuit and shuts off the current when excessive temps develop. Both leads emanate from one end, lending it to wave soldering and automated assembly in PCBs. Current carrying capacity is 5 A max at 120 Vac. **3M, Industrial Electrical Products Div,** PO Box 33600, St Paul, MN 55133.

Circle 234 on Inquiry Card

### POLLING CONCENTRATOR



Five polling ports, each capable of handling up to 26 video terminals are a feature of the smart polling concentrator. Its learning capability allows it to seek out only those terminals responding to the poll chain and subsequently poll only terminals that have answered. Each port is firmware programmed for baud rates to 9.6k and bit structure. A 6k memory (expandable to 12k) is provided for each polling port. **Communication Devices Inc,** 290 Huyler St, South Hackensack, NJ 07606.

Circle 235 on Inquiry Card

### 3-W OPEN FRAME SWITCHER

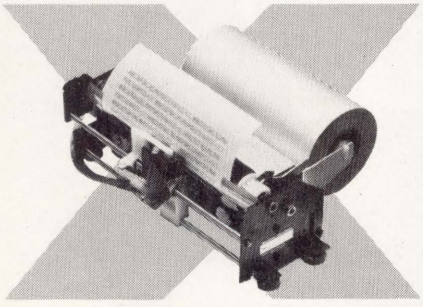
Efficiencies of the ES-D series open frame switching power supplies vary from 70 to 84% with 0.2% line and load regulation. Ripple and noise are <50 mV pk-pk. Regulation, modulation, and protective circuits are onchip, giving parts reduction of 20% and a MTBF of >50k hours. Power output is continuous rated to 70 °C, full rated at 50 °C. Outputs are 5 V at 6 A, 12 V at 3 A, 15 V at 2.4 A, 24 V at 1.5 A, 28 V at 1.3 A, and 36 V at 1.0 A, adjustable ± 10%. **Power/Mate Corp,** 514 South River St, Hackensack, NJ 07601.

Circle 236 on Inquiry Card

### ENCRYPTION/DECRYPTION OPTION FOR PASCAL COMPUTER

A hardware enhancement for the ACI-90™ Pascal computer system incorporates a WD2001 data encryption device. Using the algorithm specified in the Federal Information Data Encryption Standard (NBS #46), data are encrypted/decrypted at a transfer rate of 163k bytes/s. Work memory manipulation allows secure data transfer to ports or disc storage. **Associated Computer Industries,** 17751H Sky Park E, Irvine, CA 92714.

Circle 237 on Inquiry Card

**Fast, low cost printer.**

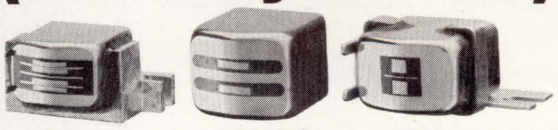
This DC-4004A discharge printer prints 48 columns at 144 cps. Printing alphanumerics in 5 x 7 matrix format on 4.72" paper, its MTBF is 144 million characters. Just 2.6" H x 6.7" W x 5.9" D, it's only $127 in 100 quantity. Other printers with interface electronics available.

Call or write HYCOM, 16841 Armstrong Ave., Irvine, CA 92714 — (714) 557-5252

HYCOM

CIRCLE 107 ON INQUIRY CARD

**We'll help you get a head (and stay ahead!)**



**3Q1-**
4-track/4-channel cassette head .. Precision Mount, (Azimuth ± 6')

**WP-1D2**
4-track/2-channel Extended low-frequency response head for .250" tape

**3D7-**
2-track/2-channel cassette head, Universal Industrial mount, Exceptionally versatile.

Three typical Vikron magnetic heads that come equipped with total service. That simply means we're not done helping you until you're done needing help.

**We deliver much more than quality magnetic heads!**

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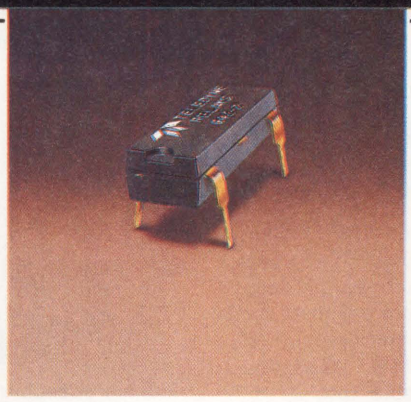
CIRCLE 119 ON INQUIRY CARD

# Ask us anything about SerenDIP® Solid State Relays.



An SSR in a DIP package? Certainly. All have logic compatible inputs. Some feature zero voltage switching for AC applications. Some are rated to switch 1.5 amps at 250 VRMS. Others are rated to 400 ma DC. Did you expect anything less from the people who introduced hybrid microcircuits to SSR design?

But you probably have other questions about this little relay and how to use it. So go ahead. There are no dumb questions.

- ☐ How can an SSR switch both AC and DC?
- ☐ How will SerenDIP® solve my low power AC switching needs?
- ☐ Are speed, long life, and bounce-free operation the only SerenDIP advantages?
- ☐ How can I get prototype quantities quickly?

Sorry. You missed my question. Here it is. _____

_____

_____

_____

Name _____ Title _____

Company _____ Phone _____

City _____ State _____ Zip _____

**TELEDYNE RELAYS**

**Ask us anything. There are no dumb questions.**

Mail to: TELEDYNE RELAYS 12525 Daphne Ave., Hawthorne, California 90250, (213)777-0077

**CIRCLE 108 ON INQUIRY CARD**

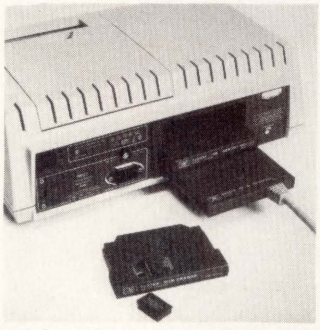
# PRODUCTS

## COLOR GRAPHICS SYSTEM

High performance graphics subsystems for all PDP-11 computers and the VAX-11/780, full color raster scan VSV11 and VS11 models use 2901 bit-slice architecture to produce dynamic color displays. VSV11/VS11 models are designed for LSI-11 bus microcomputers and PDP-11 Unibus computers, respectively, and are supported by RSX-11M, -11S, and VAX/VMS operating systems. Each is available with a 19″ (48-cm) full color display terminal, VRV02, or a monochrome VT100 terminal. A joystick provides cursor control. A DMA device composed of image processor, sync generator, and image memory, the subsystem interfaces directly with the LSI-11 bus and with the Unibus through a converter. Image memory is a video frame buffer with 512 x 512 x 2 bits of resolution and intensity in the basic configuration. **Digital Equipment Corp,** Maynard, MA 01754.

Circle 238 on Inquiry Card

## DATA ACQUISITION/CONTROL INTERFACE OPTIONS FOR DESKTOP COMPUTER



An HP-IB interface module and ROMs for I/O, plotter/printer control, and matrix math can be easily added to the HP-85 by plugging them into ports in the computer. The I/O ROM enriches the computer's BASIC language with straightforward I/O commands that configure, control, pass data to and from and check status of devices in the I/O system. The HP-IB module, when used with the I/O ROM, enables as many as 14 instruments to be controlled by each interface card and achieves data transfer rates up to 25k bytes/s. Plotter/printer ROM allows addition of HP2631B serial impact printer and HP7225A graphics plotter to the computer. Matrix math ROM provides statements for working with 1- and 2-dimensional arrays as large as 60 x 60. **Hewlett-Packard Co,** 1501 Page Mill Rd, Palo Alto, CA 94304.

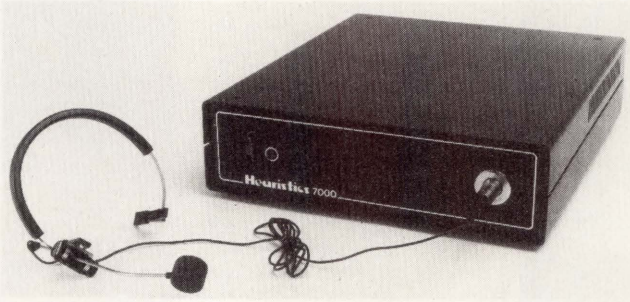
Circle 242 on Inquiry Card

## PRINTING SYSTEMS FOR HP-3000 MINICOMPUTERS

Add-on systems give users of HP-3000 series I, II, and III minicomputers the choice of 300- to 1800-line/min printers. The HPC30 controller is form, fit, and function compatible with HP's controller and is totally transparent to the operating system. It functions under programmed I/O or with DMA. Only one mainframe card position is required. Complete system consists of controller/interface card, 1 of 7 band or drum line printers, and all necessary cabling. Using std HP peripheral address numbers and interrupt priorities, it receives data and commands directly from the computer's I/O peripheral bus while print operations are controlled either from the CPU or multiplex channel bus. Transmission to printer is via a parallel bus with a max 1800-line/min rate. **BDS Computer Corp,** 1120 Crane St, Menlo Park, CA 94025.

Circle 240 on Inquiry Card

## INDUSTRY COMPATIBLE SPEECH RECOGNITION UNIT




Making speech input capability available with virtually every computer terminal, the model 7000 will interface with all RS-232-C terminals to provide advantages of hands-off operation. Key to the unit is a spectrum analyzer that uses digital filtering and pattern matching techniques to analyze audio input. Output is automatically transferred to the computer in standard ASCII format. The unit can be trained to recognize up to 64 words or phrases, each up to 3 s in length, and is compatible with all common programming languages, such as FORTRAN, COBOL, Pascal, and BASIC. It can be trained or retrained as often as necessary, and automatically rejects utterances significantly different from the vocabulary set. **Heuristics,** 1285 Hammerwood Ave, Sunnyvale, CA 94086.

Circle 241 on Inquiry Card

## 400-W SWITCHING POWER SUPPLIES

EPS1901F, 2F, and 3F series supplies feature a built-in electromagnetic interference (emi) filter designed to limit emi in accordance with the requirements of VDE 0871/6.78, curve A specs. The front panel of the cabinet has a front-mounted terminal block to allow addition of the emi filter without increasing case dimensions. EPS1901, 2, and 3 do not have the filter feature. Other features of the high efficiency (80%) units are soft-start circuitry to eliminate voltage overshoot and limit in-rush current, overcurrent protection, overvoltage protection, overvoltage protection with automatic reset, and remote turn-on and turn-off. All cabinets measure 8 x 5 x 11″ (20 x 12.7 x 27.9 cm). **Motorola Subsystem Products,** PO Box 20923, Phoenix, AZ 85036.

Circle 239 on Inquiry Card

See you at NCGA '80 and SIGGRAPH '80

# The AED 512... graphics, imaging, Superoam™ and integer zoom in one desktop terminal!

At the Siggraph '79 Show, it was acclaimed as 'The Incredible Graphics Machine!' Since then, the AED512 full-color graphics and imaging terminal has more than lived up to its reputation among sophisticated users. Its ability to display 256 simultaneous colors (from a total palette of 16.8 million) on a 512 x 483 pixel screen; zoom at integer increments to x16; pan continuously via joystick; perform full-screen DMA transfer in 0.5 second; emulate Tektronix 4014 software; allow overlaying TV images with computerized graphics; permit animation by using read/write masks and colorblink make its under $20,000 price tag seem small. Add to this its unique ability to Superoam an expanded image of 1024 x 1024 pixels and you'll see why the FIVE-TWELVE is features ahead of the competition. For more information contact Jerry Kennedy, Advanced Electronics Design, 440 Potrero Ave., Sunnyvale, California 94086, phone (408) 733-3555.

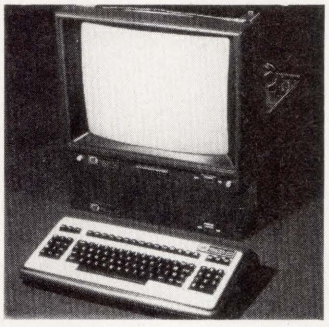
TM Trademark of Advanced Electronics Design

CIRCLE 109 ON INQUIRY CARD

# PRODUCTS

## COLOR GRAPHIC TERMINAL SYSTEM

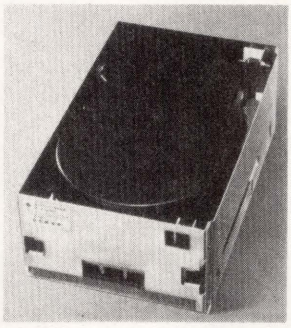
A color process information system with 512 x 512 individually addressable pixels at a 60-cycle (nonflicker) refresh rate, model 2000 offers a basic high performance terminal with field expandable building blocks that cover a selection of options. The multiprocessor architecture of the unit provides high speed macrographics, bar graph generation, complex polygon fills, programmable patterned vectors, and other options. Simple high level ASCII commands are used for programming. Special function keys and memory expandable to 64k add to this capability. The high resolution monitor incorporated in the terminal provides automatic degaussing and a high contrast filter. **Industrial Data Terminals Corp,** 1550 W Henderson Rd, Columbus, OH 43220.



Circle 243 on Inquiry Card

## 13.9M-BYTE 8″ HARD DISC DRIVES

Incorporating a Winchester type head which provides a recording density of 7300 bits/in (2874/cm) with MFM recording techniques on an 8″ disc, DK801-1 and -2 drives have unformatted capacities of 6.9M and 13.9M bytes, respectively. When functioning in a 44-sector format, capacities are 5.2M bytes for the -1 and 10.4M bytes for the -2. Both have track capacities of 1.3k bits with corresponding sector capacities of 256 bytes. Data transfer rates are 889k bytes/s with NRZ as the data transfer form. Avg access time is 70 ms with a max of 150 and a min of 30 ms. Avg latency is stated as 8.4 ms. Power requirements are listed as 24 V ±10% at 6 A start and 5 A rotating, 5 V ±5% at 3 A, and −5 A or −12 V ±5% at 0.9A. **Hitachi America, Ltd,** 100 California St, San Francisco, CA 94111.



Circle 244 on Inquiry Card

## 9-WIRE IMPACT MATRIX PRINTHEADS

Model 1000 has a max print wire frequency of 1250 Hz, typ life of 300M char, and a range of voltages and pulse widths. Model 5000 is electrically and mechanically compatible with Lear-Siegler impact matrix printers, and is interchangeable in the field as well as in production, while model 6000 is compatible with Diablo impact matrix printers as well as with Universal Microprinters printheads. Providing up to 250 char/s with a 9 x 7 font, the units accommodate 6-part forms. Char height is 0.130″ (3.302-mm) overall. Power consumption is 4 W/print wire at 1250 Hz continuous. Avg power requirements are 6.6 W for avg text at 250 char/s. **DH Associates,** 754 N Pastoria Ave, Sunnyvale, CA 94086.

Circle 245 on Inquiry Card

## HIGH SPEED PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER

Amplifier gain of 1, 2, 4, or 8 can be selected by applying logic signals to the two gain control inputs on the HY-6110, allowing digital control of gain in microprocessor based data acquisition systems. Gain accuracy is 0.05% and linearity is 0.005% at each gain setting (accuracy can be adjusted to 0.01% if required). In addition, this gain will settle to 0.01% of the final gain value in 5 μs when programming gain of the amp. Device has a slew rate of 10 V/μs and 10 μs settling time for an output voltage transistion from +10 V to −10 V. Common mode rejection is 85 dB min. Initial offset voltage is <1 mV and typ input offset voltage drift is 10 μV/°C. Differential input resistance is $10^{10}$ Ω and input bias current is 100 pA at 25 °C. **Hytek Microsystems, Inc,** 16780 Lark Ave, Los Gatos, CA 95030.

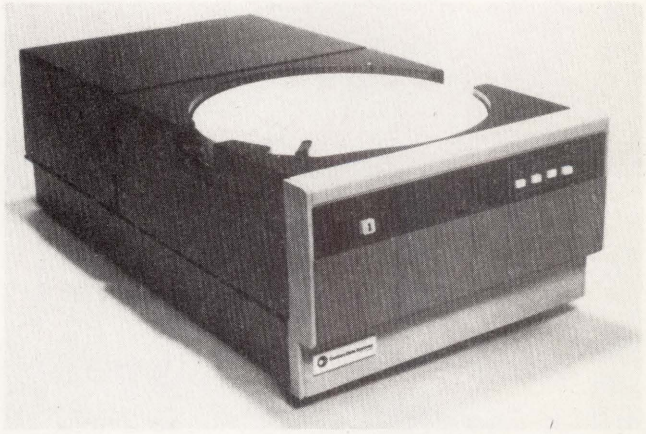
Circle 246 on Inquiry Card

## LSI-11 COMPATIBLE FLOPPY DISC CONTROLLER

F02CTR floppy disc controller card provides DEC RX02 emulation on a single dual-width PC board that plugs directly into an LSI-11 backplane. For use with either single- or double-sided drives, the card can identify a drive as either 1- or 2-headed and thereby establish the correct stepping rate and other control signals and can automatically recognize single- or double-density (RX01 or RX02) formats. Density is determined by means of a guessing algorithm rather than through an encoded sector byte. The card fully emulates RX02 with the LSI-11, -11/2, or -11/23 microcomputer and runs RX02 diagnostics as well as onboard self-test diagnostics. It also has a built-in bootstrap and uses DEC provided hardware. **Advanced Electronics Design, Inc,** 440 Potero Ave, Sunnyvale, CA 94086.

Circle 247 on Inquiry Card

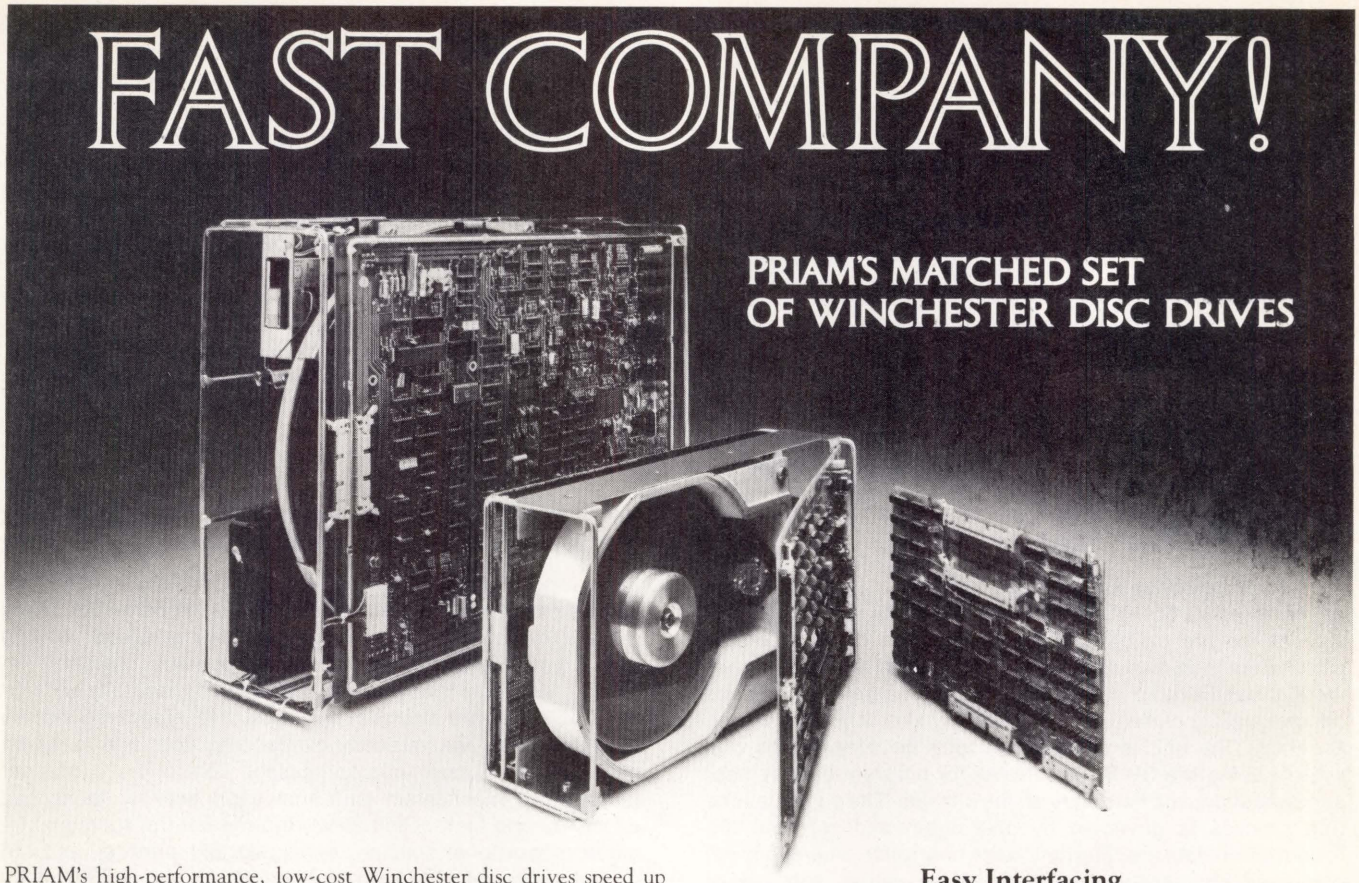
## 91.9M-BYTE INTELLIGENT DISC DRIVES



Plug compatible with the company's Intelligent Marksman, the Intelligent Hunter achieves system capacities up to 90M bytes in a fixed/removable media drive. General purpose I/O interface provides a simple TTL byte-parallel connection. The drive package operates on about 85% less power and occupies less space than is required by comparable disc drives operating with separate controllers. Models IH-32, -64, and -96 provide 30.5M, 61.2M, and 91.9M bytes of formatted data storage, respectively, in a 10.5″ (26.7-cm) high, rackmounted or tabletop device. Microdiagnostics allow detailed error-fault location. Single function command structure, automatic sector interleaving set by switch or command, DMA transfer, single sector transfer, and alternate track assignment are features. **Century Data Systems,** 1270 N Kraemer Blvd, Anaheim, CA 92806.

Circle 248 on Inquiry Card

# FAST COMPANY!




PRIAM's high-performance, low-cost Winchester disc drives speed up throughput and expand data storage from 20 megabytes to 154 megabytes. And a single controller can be used to operate 14-inch-disc drives with capacities of 33, 66, or 154 megabytes or floppy-disc-size drives holding 20 and 34 megabytes. So it's easy to move up in capacity, or reduce package size, without changing important system elements or performance.

## High Performance and Capacity at Low Cost

Fast, linear voice coil positioning gives you high system throughput, without traditional high cost. Track-to-track positioning time is less than 10 milliseconds for all models, and average positioning takes just 50 milliseconds. PRIAM's use of IBM 3350-level Winchester disc technology gives you high capacity at amazingly low cost.

Simple, efficient design makes both types of PRIAM drives reliable and economical. Brushless DC motors eliminate belts, pulleys and mechanical brakes. They also save you money and let any PRIAM drive operate anywhere in the world.

## Compact Sizes, Light Weight

Small size and light weight make PRIAM drives a cinch to fit into your systems. The space-saving DISKOS 3350, 6650, and 15450 weigh a mere 33 pounds. The DISKOS 2050 and 3450 have exactly floppy-disc-drive dimensions and weigh only 20 pounds. Compact, light steel rod frames permit easy flow of air in the system, improving system reliability. In the 14-inch drives, the optional power supply can be fully enclosed within the disc drive assembly.

## High Reliability

PRIAM's proprietary head-disc assembly air system assures long-term reliability by maintaining positive pressure at the spindle-bearing seals. Data reliability is guaranteed by fully servoed head positioning; dedicated servo tracks eliminate the positioning errors to which other low-cost drives are vulnerable. Microprocessor control reduces component count and cost and improves reliability and flexibility.

## Easy Interfacing

PRIAM's low-cost serial data interface is the same for both 8-inch and 14-inch drives, and all PRIAM drives include data separation. To make interfacing easier than ever, PRIAM's optional Parallel Data Interface provides functions that permit interfacing directly to the I/O bus at the byte level. It controls up to four drives, and provides serialization and deserialization of data, disc formatting, sector buffer, polled or interrupt operation, defect mapping, overlapped commands, implied seek, selectable sector sizes, and resident microdiagnostics. A simple interface to the CPU is all that's needed, eliminating tedious and expensive controller development.

## SMD Interface

If you have an SMD controller in your system, you can move quickly to Winchester technology performance, reliability and economy by using PRIAM's optional interface. It matches up conveniently with existing Storage Module interfaces and it is available with all of the following PRIAM models.

## THE PRIAM LINEUP

| Model/Disc Size | Capacity | Transfer Rate | Size |
|---|---|---|---|
| DISKOS 3350 (14") | 33 Mbytes | 1.03 Mbytes/Sec | 7" x 17" x 20" |
| DISKOS 6650 (14") | 66 Mbytes | 1.03 Mbytes/Sec | 7" x 17" x 20" |
| DISKOS 15450 (14") | 154 Mbytes | 1.03 Mbytes/Sec | 7" x 17" x 20" |
| DISKOS 2050 ( 8") | 20 Mbytes | 1.03 Mbytes/Sec | 4.62" x 8.55" x 14.25" |
| DISKOS 3450 ( 8") | 34 Mbytes | 1.03 Mbytes/Sec | 4.62" x 8.55" x 14.25" |

Take a closer look at future database requirements. Then get complete details about PRIAM Winchester disc drives by writing or calling:

PRIAM

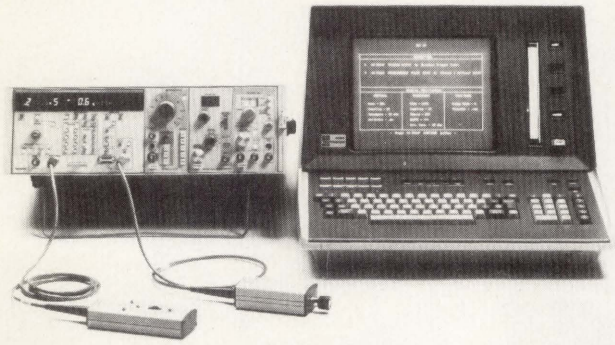
3096 Orchard Drive San Jose, CA 95134
Telephone (408) 946-4600 TWX 910-338-0293

Ask for "Who's Selling Rifles to the Indians?", PRIAM's FREE Winchester Technology Primer.

CIRCLE 110 ON INQUIRY CARD

## PRODUCTS

### PROGRAMMABLE OSCILLOSCOPE CALIBRATION GENERATOR



A microprocessor based calibration generator that is fully programmable, CG 551AP can be used as part of a computerized system for the calibration and verification of oscilloscope parameters including vertical gain, horizontal timing and gain, vertical bandwidth/pulse characteristics, probe accuracy and compensation, current probe accuracy, and calibrator output accuracy. The unit is designed to form an integral part of a system using the GPIB, a controller for program development and execution, and hardcopy or line printers. The entire calibration process is governed by preprogrammed software. Error/deviation data are returned to the controller, where they are compared to preprogrammed reference values and out of tolerance values are flagged. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.

Circle 249 on Inquiry Card

### SMART COMPUTER TERMINALS

Executive 80 terminals suit requirements of smaller modular computer systems as well as those of large host computers with highly distributed terminal networks. Model 20 is a buffered video display terminal with extensive video highlight and formatting features; model 30 is a high performance editing terminal with expanded function key capability, additional transmission modes, paging, and data validation. Std features include video highlighting, line drawing, status line, programmable function keys, and a horizontal split screen display. An enhanced video option selectively displays characters at normal font size, twice normal height and width, or in 132-col format on a 15″ (38-cm) monitor. **Hazeltine Corp, Computer Terminal Equipment,** Greenlawn, NY 11740.

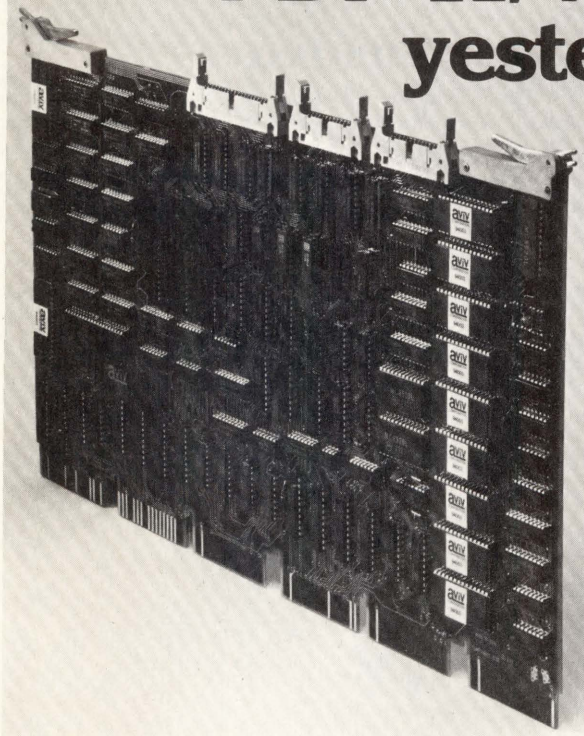
Circle 250 on Inquiry Card

### HIGH SPEED, HIGH QUALITY DOT MATRIX GRAPHICS PRINTER

Paper Tiger™ model 460 uses precision dot placement and advanced paper handling techniques to provide correspondence quality text and high resolution graphics at speeds of 160 char/s. To achieve this, the unit uses a dot matrix character formation technique that overlaps dots both horizontally and vertically. The 9-wire ballistic printhead has staggered needle rows to create the vertically overlapping dots and is driven bidirectionally under microprocessor control by a stepper motor drive mechanism with true logic seeking lookahead capability and high speed slew. Printing control functions include proportional spacing, enhanced text printing, and std print densities of 10-, 12-, or 16.7-char/in (3.9, 4.7, or 6.5/cm). **Integral Data Systems, Inc,** 14 Tech Circle, Natick, MA 01760.

Circle 251 on Inquiry Card


# All other Mag Tape Controllers for PDP-11/VAX-11 just became yesterday's technology.



Because Aviv is first again with another major step in minicomputer peripheral technology...the industry's first **dual-density** single-board mag tape controller for PDP-11* and VAX-11* users.

Aviv is the company that introduced the first mag tape controller for LSI-11's*... as well as the first GCR mag tape systems for PDP-11/VAX-11 and Nova/ECLIPSE.** Now, Aviv does it again with the new TFC-822... the industry's first **dual density,** mag tape controller on a single hex board for PDP-11/VAX-11 unibus computers.

We didn't take out features...we added them and still designed a smaller and more efficient controller. Features include: bit/slice technology; large FIFO data buffer; burst mode transfer; optional read/write of gapless tape and more.

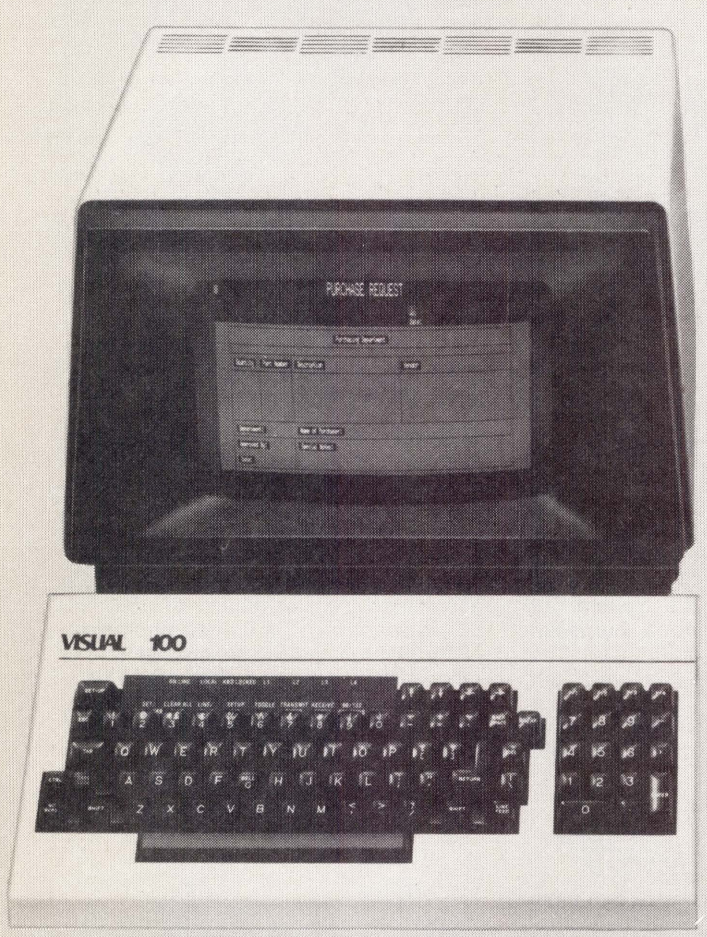
If you're a DEC user, Aviv's **dual density,** single board mag tape controller will enhance your total system. TFC-822 delivery is 30 days A.R.O. Write or call Aviv for further information.

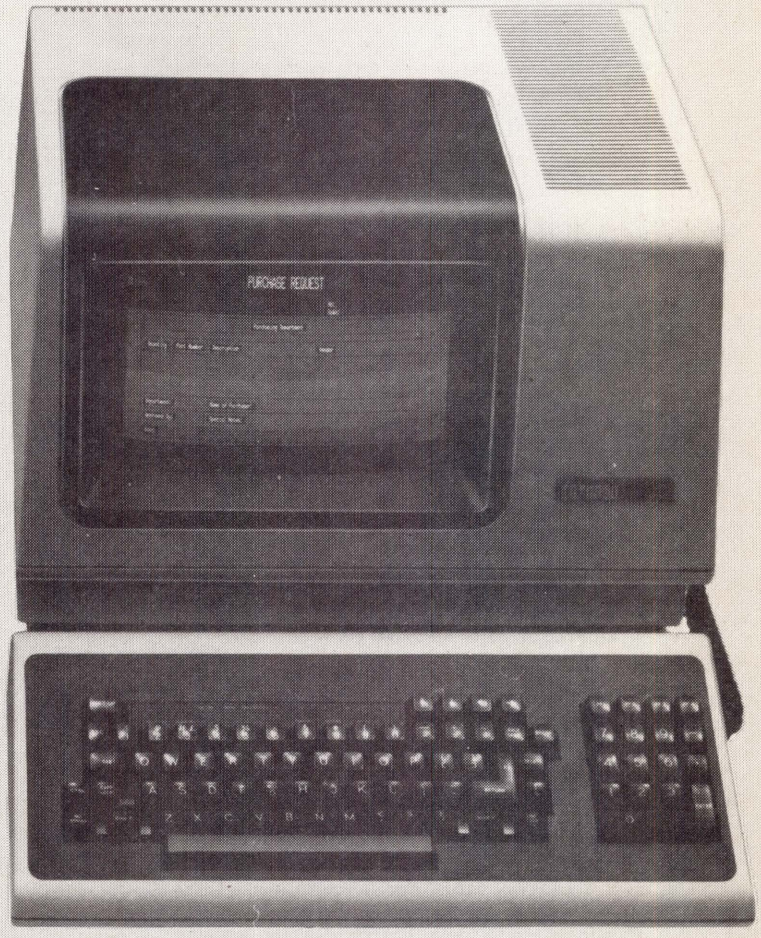
aviv CORPORATION

6 Cummings Park
Woburn, Massachusetts 01801
(617) 933-1165

* Digital Equipment Corporation
** Data General Corporation

# Freedom of choice.




## VISUAL 100 Digital VT 100®

These two terminals not only look alike—they act alike. But ours is a little better.

The new VISUAL 100 is 100% compatible with the DEC VT 100,® right down to the spacing of the keys and the roll of the keyboard. Neither your operator nor your software will know the difference. Except your operator will appreciate the superior human engineering features of the VISUAL 100 like the non-glare screen, adjustable viewing angle and low slung keyboard.

Further, the Advanced Video package and current loop interface that are optional with the DEC® terminal are standard with the VISUAL 100. And we've added an optional Buffered Printer Interface with independent baud rate, independent parity and printer busy via XON XOFF protocol or control line.

Although we think the VISUAL 100 is a little better than the VT 100®, we priced it a little lower. Plus it's from the Company that's delivered thousands of terminals emulating DEC, Hazeltine, Lear Siegler and ADDS. Call or write us today.

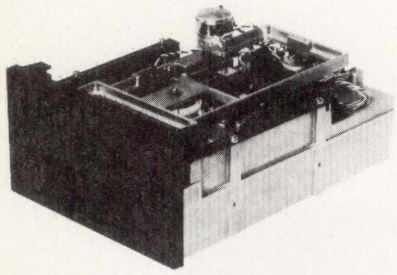
VISUAL See for yourself

**Visual Technology Incorporated**
Railroad Avenue, Dundee Park, Andover, MA 01810
Telephone (617) 475-8056

CIRCLE 112 ON INQUIRY CARD

# PRODUCTS

## 5.25 AND 8″ FLOPPY DISC DRIVES



For the Mini-Flexi 5.25″ (13.34-cm) drive, single-sided capacity is 875k bits, while double-density, double-sided capacity is 3.5M bits. Data transfer occurs at 125k and 250k bits/s, respectively. The 8″ (20-cm) drive provides 3.2M- and 12.8M-bit capacity, with data transfer rates of 250k and 500k bits/s. Access time to adjacent track is 3 ms. Hardware features improve disc handling and loading/unloading safety features. **C. Itoh Electronics, Inc,** 5301 Beethoven St, Los Angeles, CA 90066.

Circle 252 on Inquiry Card

## LOCAL DISPLAY CONTROLLER FOR DISTRIBUTED SYSTEMS

Model 320 local display controller, compatible with IBM 3274 models 1A, 1B, and 1D, supports the company's SOFTPRINT™ unit capabilities in a local environment by attaching to the IBM byte mux, selector, or block multiplexer channel. Intelligent hardware reduces inconvenience of device address shortage. The controller incorporates a 140-ns bipolar microprocessor for maximum channel transfer rates and imbedded diagnostics. **Lee Data Corp,** 5700 Green Circle Dr, Minnetonka, MN 55343.

Circle 256 on Inquiry Card

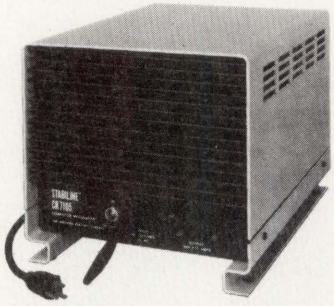
## INSULATION DISPLACEMENT CONNECTOR

PCB7 series PC board connectors use an insulation displacement technique for securing the wires in the connector without stripping, crimping, or tightening screws. Connectors are available in versions for 14, 16 to 18, and 20 to 22 AWG, and come in std lengths from 6 to 26 circuits with 0.200″ (0.508-cm) contact spacing. They will handle loads up to 10 A at 300 V. Contacts are phosphor bronze with tin plating; gold over nickel is optional. **Control Products Div, Amerace Corp,** 2330 Vauxhall Rd, Union, NJ 07083.

Circle 254 on Inquiry Card

## POWER LINE CONDITIONER

Stabiline® computer regulators offer complete power line conditioning in an easy to install package, providing a 120-Vrms ±3% output over an input voltage range of 95 to 130 V and correcting most changes in voltage within 1.5 cycles. 60-dB common mode noise rejection helps prevent noise related problems such as computer errors and loss of information. Wiring requires only simple plug-in connections to load and power source. **The Superior Electric Co,** Bristol, CT 06010.



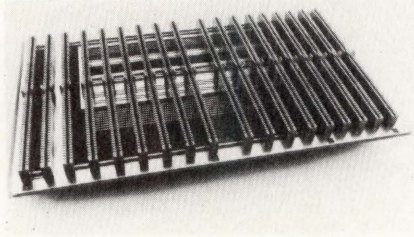
Circle 255 on Inquiry Card

## 0.5M-BYTE VAX-11/780 COMPATIBLE MEMORY CARD

512k bytes of storage can be contained on a single hex-wide NS780 card, which provides 225-ns access time and 425-ns cycle time. Included is an online/offline switch that allows the card to be electrically removed from the system. All RAMs are socketed and a burned-in spare RAM is included on the card. The card is fully compatible with all VAX-11/780 hardware, software, and peripherals. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

## BACKPLANE ASSEMBLIES WITH PRESS FITTED CONNECTORS

Contact-Sert™ backplane assemblies are made by press fitting contacts into 2-sided or multilayer PC boards with plated through holes. Std plating is a 0.1″ (2.54-mm) stripe of gold, 30-μin (0.76-μm) thick over 50-μin (1.27-μm) of nickel on the contact area and a gold flash of 5 μin (0.12 μm) (3 μin or 0.076 μm min) of gold over 50 μin (1.27 μm) of nickel on the rest of the contact body and tail. Military spec plating of 50 μin (1.27 μm) of gold over nickel is available. **Hybricon Corp,** 410 Great Rd, Littleton, MA 01460.



Circle 253 on Inquiry Card

## ULTRAVIOLET EPROM ERASER

QUV-T8 lamp erases most industry standard UV EPROMs such as 2708, 3716, 2532, and can erase up to 20 devices at a time. Erase time at 1″ (2.54-cm) distance from light source is approx 25 min. UV lamp has estimated life of 7700 h. Unit requires 105 to 130 Vac at 0.08 to 0.1 A. Package size is 25.4 x 7.62 x 11.43 cm. **Logical Devices, Inc,** 1525 NE 26th St, Ft Lauderdale, FL 33305.

Circle 257 on Inquiry Card

## INFRARED EMITTERS AND DETECTORS

TIL38 and 39 IR emitting diodes produce 12 mW of output power at 100 mA. Beam emission angles at half-intensity points are 60 and 20°, respectively. TIL40 diodes are intended for low cost applications. TIL100 and 413 photodiodes are spectrally matched with the TIL38 and 39 and have receiving angles of 150 and 60°, respectively. Darlington phototransistors TIL411 and 412 are spectrally and mechanically matched with the TIL40. **Texas Instruments, Inc,** PO Box 225012, M/S 308, Dallas, TX 75265.

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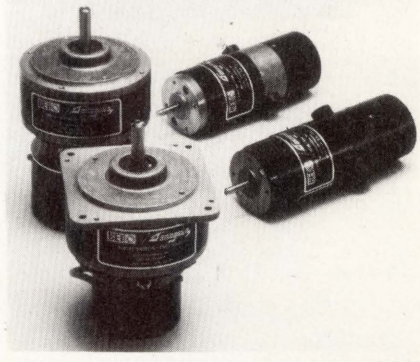
## SERVOMOTOR ENCODERS



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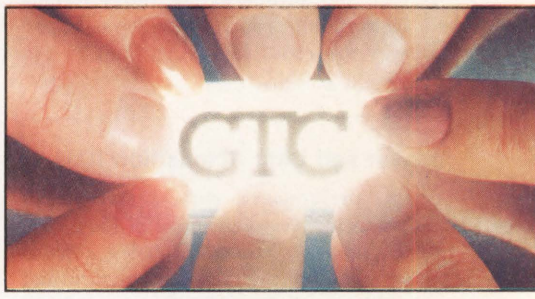


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# LITERATURE

### Magnetic Shields

Manual/catalog provides design and selection guidelines plus case histories and calculation assists, and discusses shielding effectiveness and Helmholtz coil testing. **Ad-Vance Magnetics, Inc,** Rochester, Ind.

Circle 300 on Inquiry Card

### Data Cables and Connectors

Included in catalog are cables and connectors for interconnection of CPUs of major manufacturers with peripherals, low capacitance and bulk cables, specs, and description of continuity tester. **Craig Data Cable Co,** Westport, Conn.

Circle 301 on Inquiry Card

### Solid State ac Power Conversion Devices

Catalog features specs and block diagrams for ac line conditioners and power sources, frequency converters, high isolation transformers, inverters, and uninterruptible power systems. **Elgar Corp,** San Diego, Calif.

Circle 302 on Inquiry Card

### Miniature Data Acquisition Modules

Pamphlet lists features and supplies descriptions, mechanical dimensions, specs, block and connection diagrams, and control pin functions of 8-, 16-, and 32-channel modules. **Datel-Intersil, Inc,** Mansfield, Mass.

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### Power Supplies

Catalog outlines specs on switch-mode, series pass, unregulated, and dc-dc converters, and introduces the "UGLY" family in its corporate capability section. **Elpac Power Systems,** Santa Ana, Calif.

Circle 304 on Inquiry Card

### Linear and Data Acquisition ICs

Specs, performance curves, and circuit diagrams for ICs are included in 464-p data book that has sections on analog applications, chip information, and quality and reliability programs. Available for $2.95 (prepaid) from **Harris Semiconductor,** PO Box 883, Melbourne, FL 32901.

### Bipolar LSI Devices

Data in generic form, cross references, selection guides, and data sheets are contained in guide to P/ROMs, ROMs, character generators, FIFO, PAL™, arithmetic elements, and interface. **Monolithic Memories,** Palo Alto, Calif.

Circle 305 on Inquiry Card

### IBM-Compatible Processors

Two brochures on the AS/3000, one on the AS/5000, and three on the AS/7000 family discuss performance and operating characteristics, depict alternate configurations, and provide specs. **National Advanced Systems,** Palo Alto, Calif.

Circle 306 on Inquiry Card

### Test and Measuring Instruments

Photos, specs, and selection chart are presented in catalog describing oscilloscopes, logic analyzers, high resolution reciprocal frequency counters, counter/timers, and pulse generators. **Philips Test & Measuring Instruments, Inc,** Mahwah, NJ.

Circle 307 on Inquiry Card

### RFI/EMI Suppression Filters

Handbook features technical data, mechanical dimensions, approvals for each type of filter, and FCC compliances for power line, medical equipment, fused, and reinforced insulation filters. **Power Dynamics,** South Orange, NJ.

Circle 308 on Inquiry Card

### Pascal Newsletter

Standards, programming techniques, "Programmer's Page" dealing with matters of style, and articles of general interest to Pascal users are included in publication. **Rational Data Systems,** New York, NY.

Circle 309 on Inquiry Card

### Network Communications Systems

Brochure discusses, with charts of capabilities, hardware, and software, the five network processing systems, and gives examples of user needs served by each. **Raytheon Data Systems,** Mansfield, Mass.

Circle 310 on Inquiry Card

### Fiber Optic Data Links

Besides detailing fiber optic advantages, brochure illustrates and describes Scotchflex® Fiber Optic Data Link Systems and provides specs and dimensions. **3M,** St Paul, Minn.

Circle 312 on Inquiry Card

### Linear ICs and LSI Circuits

Catalog lists DAC, ADC, precision voltage references, analog multiplexers and switches, op amps, and future products, specifying electrical characteristics and devices they replace. **Micro Power Systems, Inc,** Santa Clara, Calif.

Circle 313 on Inquiry Card

### DIP Sockets, Headers, Jumpers

Catalog supplies features, specs, photos, and dimensional drawings of strip and pin-line sockets and headers, elevator and edge card sockets, and programming devices. **Aries Electronics, Inc,** Frenchtown, NJ.

Circle 315 on Inquiry Card

### 6M-Byte Floppy Disc Drive

Brochure describes 3M-byte disc in dual drive with built-in advanced microprocessor controller, and lists applications, features, and advantages. **Burroughs OEM Marketing,** Detroit, Mich.

Circle 314 on Inquiry Card

### Data Modems

Overview of operating capabilities plus chart categorized by speed, model, compatibility, certification, data rate, modulation techniques, transmission mode, and interfaces are presented in catalog. **Codex Corp,** Mansfield, Mass.

Circle 317 on Inquiry Card

### Wire and Cable

Information on conductor material and coatings, insulation, circuit identification, braiding, shielding, cabling, jacketing and technical data section are found in guide that is available for $10 (prepaid) in U.S. and Canada, $15 elsewhere, from **Brand-Rex Co,** Wire & Cable Engineering Guide, WC-78, PO Box 498, Willimantic, CT 06226

# Now, OEMs can take the High Road or the Low Road with our Direct-Connect Modem Cards, small enough to mount inside Data Terminals.

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## The Low Road: 300 bps

The VS300P is a 300 bps full duplex, automatic originate/answer "Modem-on-a-Card." Like the VS1200P, it measures only 5" by 8.35," making it small enough to mount inside most terminals. The VS300P is Bell 103/113 compatible, and FCC Registered for direct connect via a Telco voice or data jack. Mounting holes on each corner make it a cinch to install. And the price would put a smile on the face of the thriftiest Scotsman. Just $200 in lots of 100.

## Both Roads: The TI Story

Two of Texas Instruments new Silent 700* data terminals include Triple Modems custom made by Racal-Vadic. Although small enough to fit into TI's portable 17 pound terminal, this remarkable modem combines a Racal-Vadic VA3400, a Bell 212A, and a Bell 103. Imagine, a full originate/answer direct-connect modem with both 1200 bps full duplex and 300 bps full duplex in such a tiny package. And it can even be acoustically coupled.

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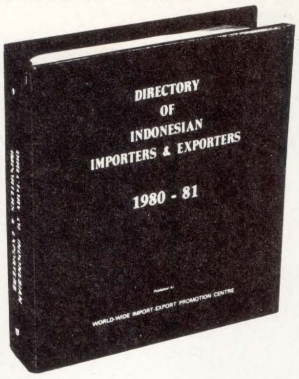


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## THE SOLID STATE MEMORY MARKET IN WEST EUROPE

The West European solid state memory market will undergo phenomenal growth over the next decade, as consumption moves from an estimated $210 million or 2.9 billion bits in 1978, to $494 million or 17.7 billion bits in 1982, and finally in 1990, to over $1.4 billion or 457 billion bits. The United States industry, and to a lesser extent the Japanese, have the greatest impact and influence on the W. European industry. Device prices are determined in the U.S. Ten of the top 12 solid state memory suppliers are American. Ten of the 13 major semiconductor process and product innovations over the last nine years have come from the United States. With rapid advances in semiconductor technology from discrete devices to integrated circuits, European manufacturers have been too slow to take advantage of exploiting the new technologies. While U.S. suppliers were enjoying the advantages of a healthy national economy, vertical integration and heavy spending on research and development, Europe's economic situation was questionable, companies were sadly lacking the vertical integration, and spending on research and development was too small to be of any significance. There is strong evidence now, however, that changes are coming, albeit slowly.

Frost & Sullivan has completed a 667-page, two-volume analysis and forecast of the W. European solid state memory market. The report, which covers 13 principal W. European countries, is believed to be the most comprehensive work of its kind on this market.

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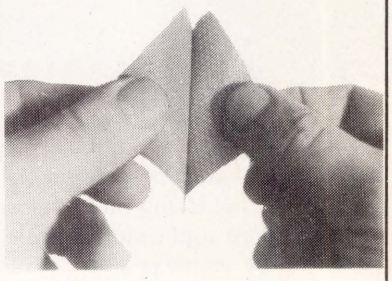

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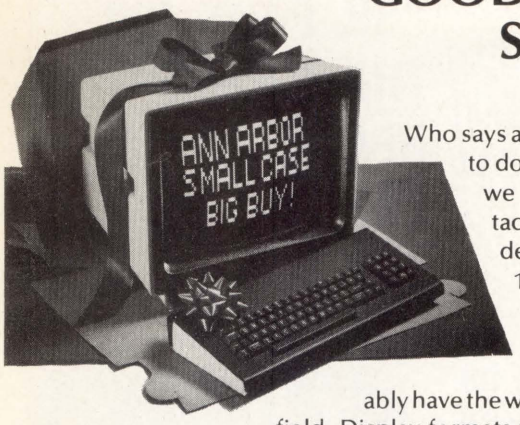


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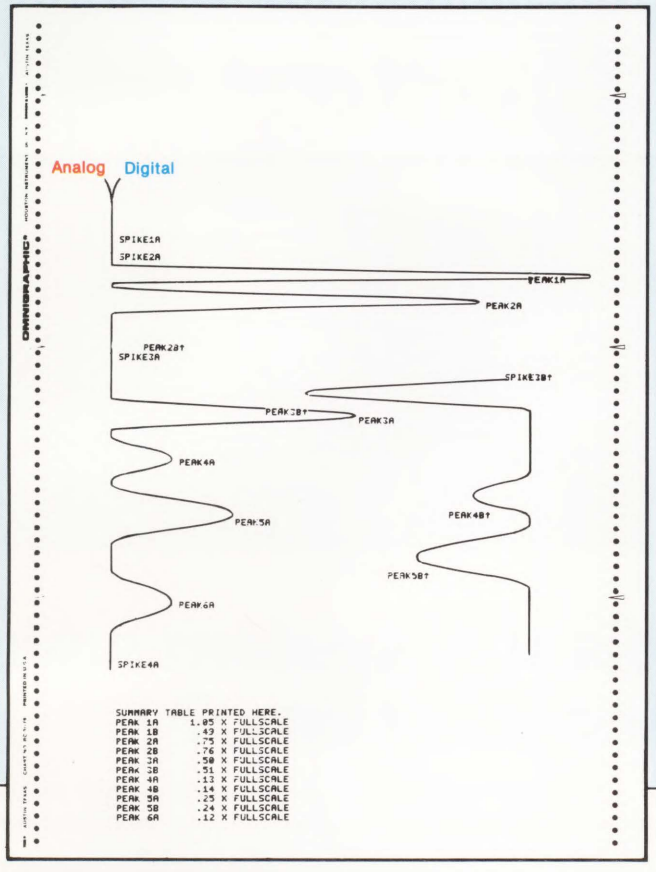


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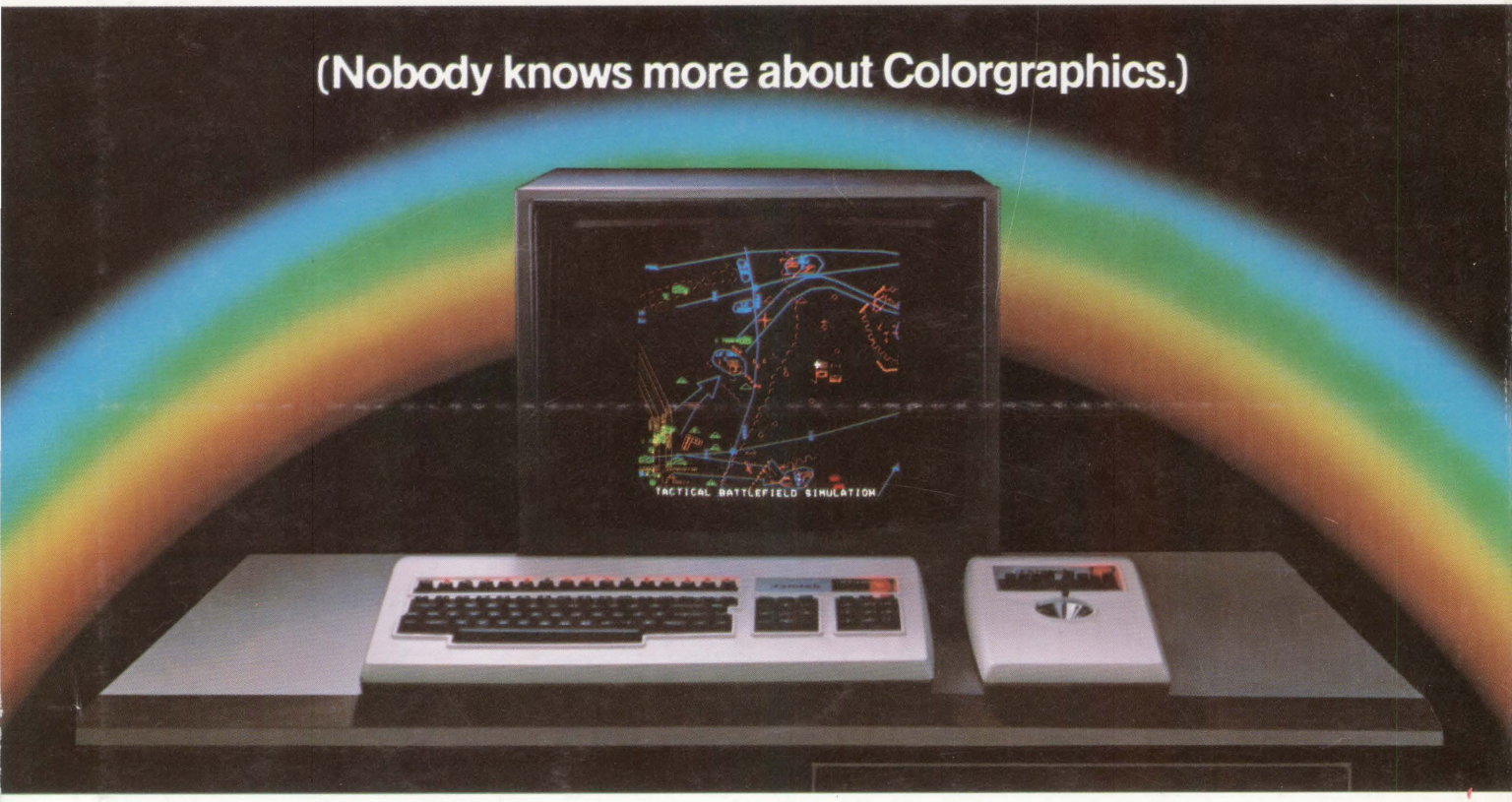


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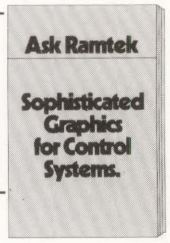


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