

A PennWell Publication

MAR 1983

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

**SPECIAL REPORT:
DATA COMMUNICATIONS
SYSTEMS DESIGN**

INFORMATION SCIENCE LIBRARY

640 x 480 full screen pixel resolution.

2D transformations for continuous scaling, translations, rotations and windowing.

4096 x 4096 virtual display space.

19" standard CRT display.

128K byte display list memory (256K optional).

ANSI compatible terminal with DEC VT-100 and VT-52 emulation.

Local blink, polygon fill and pick capability.

16 simultaneously displayable colors out of 4096.

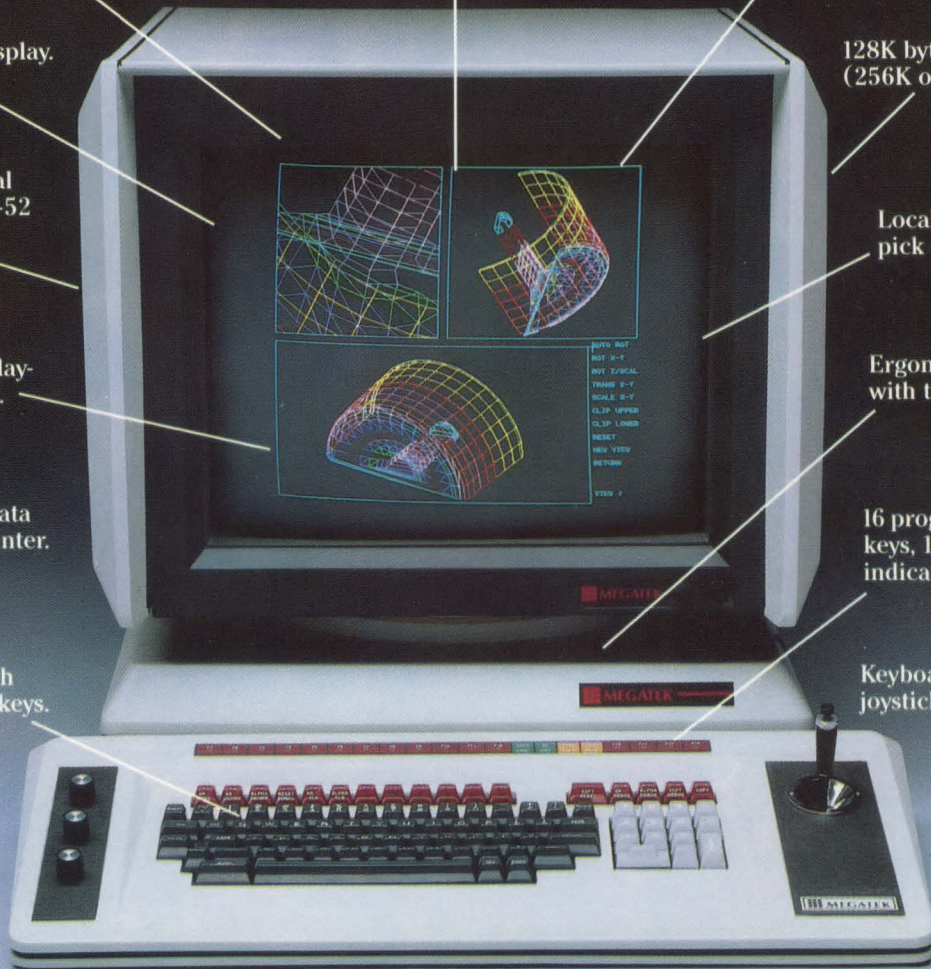
Ergonomic, anti-glare display with tilt and swivel CRT.

Other options include data tablet and hard copy printer.

16 programmable function keys, 16 programmable indicator lights.

Moveable keyboard with palmrest and sculpted keys.

Keyboard includes optional joystick and valuator dials.



Thaumaturgy.*

Graphics miracles right on your desk. Our latest Whizzard™ The 1650 desk top design terminal. Now, anyone can afford the power and performance of our more expensive Megatek Whizzards. Your own design station right at your fingertips. Another product of Megateknology™.

Finally. Everything an engineer or designer could want in desk top computer graphics. Convenience. High quality and powerful performance. VT-100 compatibility.

Functionality. Greatly increased productivity. Shouldn't every desk top design terminal offer this?

Tomorrow's graphics technology on your desk top today... thanks to Megateknology.

Making History out of State-of-the-Art.

*Thaumaturgy (thō'ma tûr jē), n., the performance of miracles.

 **MEGATEK CORPORATION**
UNITED TELECOM COMPUTER GROUP

3-30-83

Four reasons why you should look at our Winchester

1. **100% SMD format and interface compatible.**
Just plug it in and it is ready to accept data.
2. **The best price/performance ratio available.**
Kennedy can save you an average of \$2000.00 per unit over comparable disk equipment.
3. **Immediate availability.**
Most models are ready to ship 30 days ARO.
4. **Produced by an industry leader.**
Kennedy has been manufacturing Winchester since 1978 and its reputation for reliability is known world-wide.

KENNEDY

An Allegheny International Company

1600 Shamrock Ave., Monrovia, CA 91016
(213) 357-8831 TELEX 472-0116 KENNEDY
TWX 910-585-3249

KENNEDY INTERNATIONAL INC.

U.K. and Scandinavia
McGraw-Hill House
Shoppenhangers Road
Maidenhead
Berkshire SL6 2QL England
Tel: (0628) 73939
Telex: (851) 847871 KEN UKS G

KENNEDY INTERNATIONAL

Koningin Elisabethplein, 8
B-2700 Sint-Niklaas
Belgium
Tel: (03) 777 1962
Telex: 71870 KEN CO

165 Megabytes



82 Megabytes



KENNEDY • QUALITY • COUNT ON IT

PRINTER REPORT

New Line Printer Knows No Limits

Delivery of evaluation units is underway for Tally's new 600 line per minute multi-function line printer that drew rave responses at the '82 NCC. The Tally MT 660 offers features previously unavailable on line printers.

The technically advanced printer takes full advantage of the inherent flexibility of matrix printing to serve a wide spectrum of applications. Capable of multi-mode operation, the unit can produce letter quality text for high volume word processing printing, computer graphics with high resolution, label characters including bar code and OCR for material handling plus all types of special characters and symbols. A bonus feature is the resident host defined symbol generator that

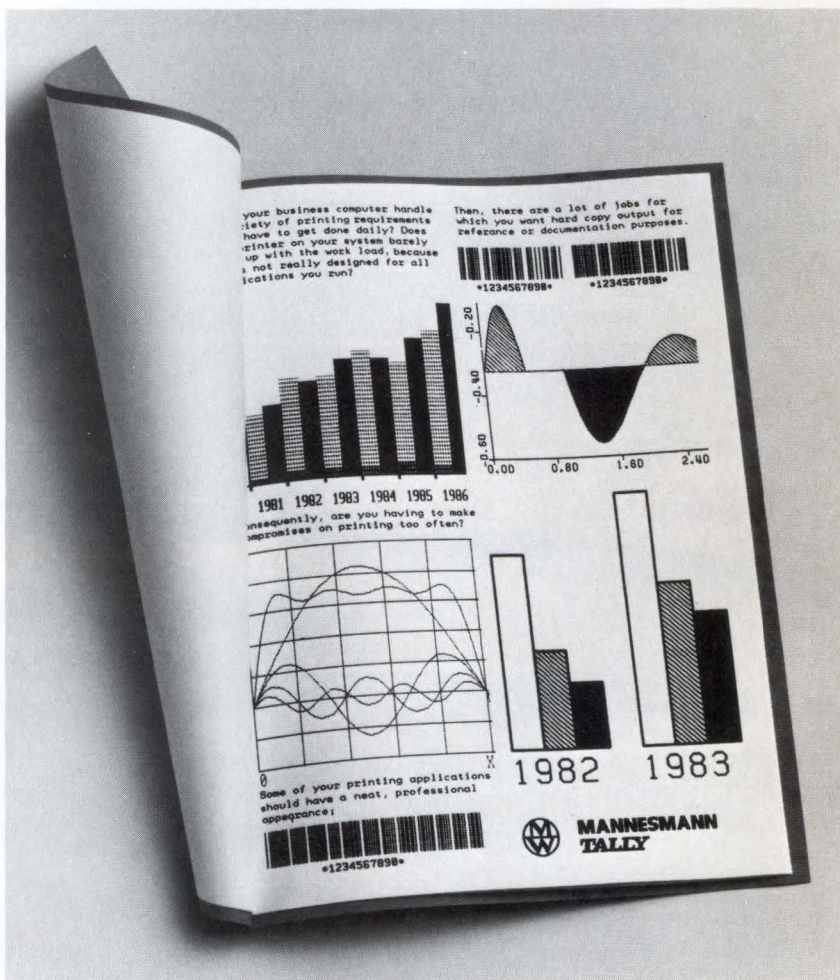
allows the user to call up on demand customized characters of his design.

Designed to provide numerous operator conveniences and features, the futuristic MT 660 offers whisper quiet office operation, an easy-change cartridge ribbon system, front panel forms set-up, self-diagnostics and status display feedback. Targeted towards professionals that demand high performance precision printing, the MT

660 delivers 100% duty cycle operation at 600 lines per minute without preventive maintenance. The printer emphasizes modular construction throughout its design for low cost of repair and parts replacement. With the unit's self-diagnostics, a service technician can quickly test each module in the machine to isolate the fault. The unit is priced under \$10,000. Production delivery is scheduled to begin in March.



Tally MT 660 line printer



MT 660 print samples

Clip and send for literature:

Name _____
Title _____
Company _____
Address _____
City _____ State _____ Zip _____
Telephone _____

MANNESMANN TALLY

8301 S. 180th St., Kent, WA 98032
(206) 251-5524

703 Petrolia Rd., Downsview, Ont., M3J2N6
(416) 661-9783

UP FRONT

Latest major entries impact personal computer market

Texas Instruments has entered the personal computer race with its "TI Professional Computer." An upgradable basic system consisting of monochrome display, keyboard, system unit with 64K bytes of RAM, and an integral 320k-byte floppy disk drive, the computer sells for \$2595. MS-DOS, CP/M, Concurrent CP/M-86, and UCSD p-System operating systems are supported. A number of software application packages and communications options are available on the 16-bit system.

Apple Computer's entry, Lisa, is a personal computer for the office. A 32/16-bit MC68000 microprocessor handles software, display keyboard, mouse, and peripherals, while three other microprocessors control I/O functions. The system includes 1M byte of main memory and 1.7M bytes (formatted) of mass storage on built-in 5 1/4 " floppy disk drives. Announced system price is "under \$10,000." Software application packages are geared to the office professional. Lisa runs high level BASIC, Pascal, and COBOL languages and will support other major operating systems.

NCR also entered the market with its Decision Mate V series, plus the Decision Net local area network. The Decision Net LAN links as many as 63 NCR and other manufacturers' personal computers. NCR computers are based on Z80A 8-bit and 8088 16-bit microprocessors and provide from 64K to 512K bytes of RAM. Both monochrome and color displays are available as are two integrated 5 1/4 " Winchester disk drives. Operating systems include CP/M-80 and -86, and MS-DOS.

And still more LANs

A joint venture of Cameo Electronics and The Fedder Software Group has produced Ultranet. This high speed transaction oriented local area network supports computers operating under CP/M, CP/M-86, and MS-DOS, as well as the IBM PC, Apple, and Radio Shack computers. Gateways will be provided for SNA, HDLC, X.25, Ethernet, Wangnet, and DECnet.

LANmark, a 512M-bps network from InteCom Inc, simultaneously handles both voice and data transmission and integrates local area networking into the company's IBX communication switch. Star architecture allows LAN functions to be performed internally. A single cable plant provides circuit and network packet switching. An Ethernet application is now available; a coax elimination for IBM 3270 workstations will follow.

Among the many cross-licensing agreements

Recent announcements for technology cross licenses and second source agreements include one between Nippon Electric Co and Standard Microsystems Corp. Still to be approved by the Japanese government, the tentative agreement involves exchanges of technology and cross licensing of semiconductor related patents.

Intel and Zymos have announced an agreement to provide Zymos's Zyp CAD system to Intel in return for Intel's CHMOS process. Both companies will maintain common CHMOS processing capabilities including a jointly developed standard cell library. Both will operate as second sources for customer designed VLSI.

A fully automated gate array IC design system, from schematic capture through finished masks, has been created by an agreement between Mentor Graphics Corp and California Automated Design, Inc. Under the agreement, Mentor will exclusively market CADI's placement, routing, and graphics software in conjunction with its own computer aided engineering design tools.

Pretriggers

- An Ethernet frontend processor on a single Multibus board** from Excelan allows OEMs and system integrators to incorporate LAN technology. The Exos/101 has an 8088 CPU, EPROM firmware, and up to 128K bytes of RAM. It implements Ethernet Version 1.0 and is compatible with Version 2.0.
- Software and hardware interconnection between a variety of host computers**, between hosts and workstations, and between stations is provided by Tri-Data's Netway family of interface processors. Extensive protocol conversion allows easy communication between diverse systems.
- A microprocessor with an 8-bit data bus and 32-bit internal architecture** provides simultaneous high performance and memory savings. National Semiconductor's NS16008 has a 24-bit address bus and is designed to ease high level language implementation.
- Mainframe performance in a desktop computer system** and at small-computer price is offered in the DN300 computational node from Apollo Computer. Performance is comparable to mid-range 32-bit superminicomputers. Included are a virtual memory CPU with 0.5M bytes of main memory and an interface to the Domain local area network.
- Choice of the 3¼" flexible disk package** in a soft vinyl jacket has been announced by Tabor Corp for its TC 500 Drivette. The single-sided drive has 500k-byte capacity.
- A microprogrammed bipolar bit-slice CPU and onboard cache memory** on Data General's 16-bit S/280 processor provide a performance level that overlaps the company's 32-bit MU/4000 and is twice that of its S/140 predecessor.
- DMA and link list processing on a text coprocessor chip** provide the capability to display publication quality text onscreen. Intel's 82730 chip can display proportional spacing with simultaneous superscripts and subscripts and can maintain linked lists of text blocks for rapid manipulation and formatting of text files.
- A compact drive featuring a 4" hard jacket removable diskette** has been announced by IBM for OEM applications. Features include a manganese-zinc recording head, LSI circuitry, FM encoding, and storage capacity of 358k characters of unformatted information on one side.
- Applying the CP/M operating system to a wide range of 16-bit microprocessors** is being eased through use of the C programming language. Digital Research's OS will also allow software authors to write programs that are compatible with both CP/M and UNIX.
- An electronic engineering workstation** from Kontron Electronics that allows an engineer to develop software also enables in-circuit emulation and logic analysis.

Computer Design (ISSN-0010-4566) is published monthly, with a thirteenth and fourteenth issue respectively in April and October by PennWell Publishing Company, Advanced Technology Group, 119 Russell Street, Littleton, MA 01460. P. C. Lauinger, Chairman; Philip C. Lauinger, Jr., President; Joseph A. Wolking, Senior Vice President; H. Mason Fackert, Group Vice President. Second-class postage paid at Tulsa, Oklahoma. COMPUTER DESIGN is distributed without charge to U.S. and W. Europe-based engineers and engineering managers responsible for computer-based equipment and systems design. Subscription rate for others is \$50 in U.S.A. and \$75 elsewhere. Single copy price is \$5.00 in U.S.A. and \$7.50 elsewhere. Microfilm copies of COMPUTER DESIGN are available and may be purchased from University Microfilms, a Xerox Company, 300 North Zeeb Road, Ann Arbor, Michigan 48106. POSTMASTER: CHANGE OF ADDRESS-FORM 3579 to be sent to COMPUTER DESIGN, Circulation Department, P.O. Box 593, Littleton, MA 01460 (USPS 127-340).



BULK SEMI

THE BIG IDEA IN MEMORY: UP TO 32 MB/CHASSIS

Now, from the memory leader, you can get 32 MB of high-performance memory in a compact 15 $\frac{3}{4}$ " system.

With chassis interface slots that allow you to use your own interface (our library of logic cards facilitates your designs!). Or choose a Dataram BULK SEMI interface that operates with DEC®, Data General, Perkin-Elmer, MODCOMP, or Honeywell minicomputers. SMD, MULTIBUS®, and AMPEX 4666-compatible interfaces are also available. And we have BULK SEMI for CSPI array processors too.

BULK SEMI. It offers single- or dual-port capability. Word lengths up to 72 bits/word. Optional battery backup. And the ultimate in price/performance.

BULK SEMI has been proven in seismic processing, process control, telecommunications, and array processing

applications — anywhere microsecond speed, megabyte main memory or peripheral memory is required. Our 16-page BULK MEMORY brochure will tell you more. And you can have it at no charge by completing the coupon below, or calling us at 609-799-0071.

DEC and MULTIBUS are registered trademarks of Digital Equipment Corporation and Intel Corporation, respectively.

**DATARAM
CORPORATION**

Princeton Road
Cranbury, New Jersey 08512
Tel: 609-799-0071 TWX: 510-685-2542

WHAT'S THE BIG IDEA?

- Send me your 16-page brochure detailing BULK SEMI.
- Please call me to discuss my application.

Name _____ Title _____

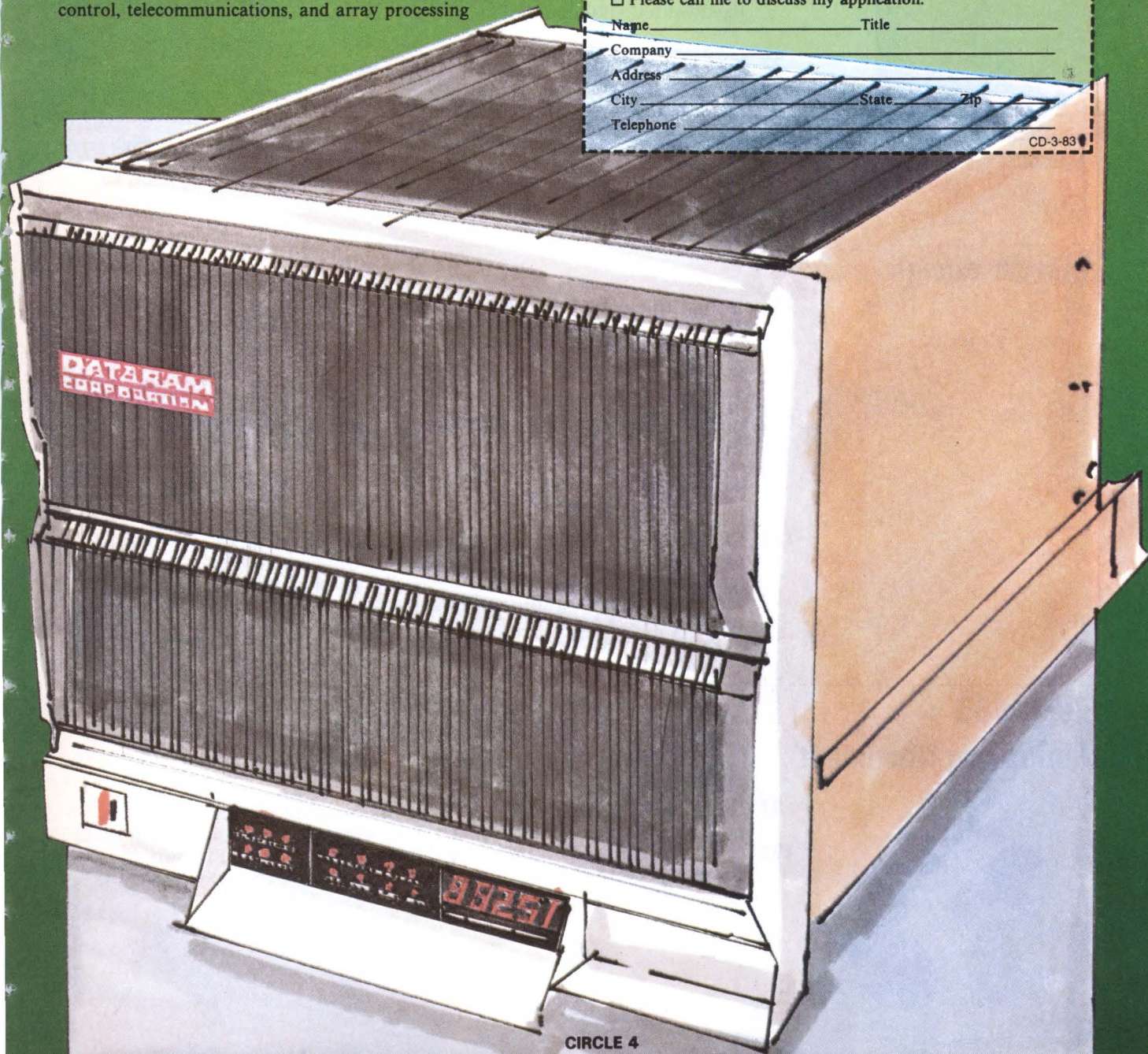
Company _____

Address _____

City _____ State _____ Zip _____

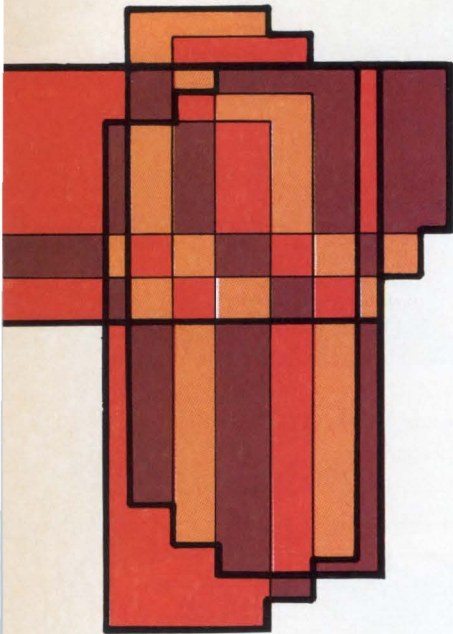
Telephone _____

CD-3-83



CIRCLE 4

System technology



Page 60

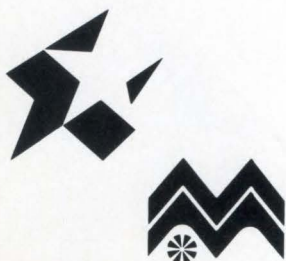
- 30 **Interface:** Committees push to standardize disk I/O
- 38 **Computers:** Multiple-processor system supports pipelined architecture with multiple cache memories
- 42 **Software:** Small computer schematic design aid automates board layout
- 52 **Memory systems:** Politics and technology—a volatile mix for ferroelectric memory
- 60 **Microprocessors/microcomputers:** Single-chip microcomputer system reduces microcontroller application development time
- 62 **Data communications:** Intelligent network component manages ultrawide bandwidth digital data links
- 72 **Test & measurement:** Protocol analyzer solves data communications network problems
- 74 **Development systems:** Gate array development system reduces circuit design time

System design

- 111 **Integrated circuits: The chip that refreshes itself**
by John J. Fallin, Joseph P. Altnether, and William H. Righter—
An 8k x 1 memory chip with onchip refresh and control circuitry offers designers the best aspects of both dynamic and static RAMs.
- 127 **Integrated circuits: Crunch BCD numbers with bit-slice chips**
*by Michael J. Miller—*Cascaded bit-slice processors improve computational accuracy when it is necessary to use the binary coded decimal number system.
- 143 **Microprocessors/microcomputers: Improving computational throughput**
*by Cedar Yoram and Meir Ben-Nun—*By tying several 8087 numerical data processing chips to a single 8086 CPU, parallel instruction execution can be accomplished with resulting increases in operational speed.

Electro/83

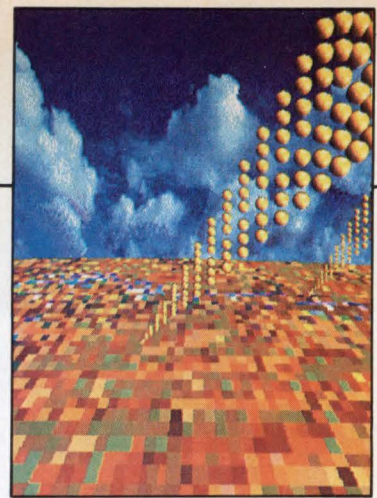
Mini/Micro-Northeast



- 87 Come April 19, Electro/83 and Mini/Micro-Northeast will witness the products and technology behind today's electronic components and small computers.
- 102 Organized separately though held conjointly, the two conferences give regional OEMs and system integrators a chance to size up the reaches of "Tomorrow's Technology Today."

Special report on data communications systems design

- 155 The proliferation of data communications products and subsystems has in some cases been detrimental to would-be designers of the overall systems. Because there are so many varied systems, designers are always deeply concerned about compatibility and incorporating the best available products in their systems. In particular, this is the case for local area networks (LANs). Almost every day another LAN is announced—sometimes new but often an already existing one new in name only. This month's "Design Frontier" report includes a review of current LAN technology and network suppliers, complemented by articles from actual designers and users.



This month's cover, entitled "The World of Data Communications," was created by Mark Lindquist and Joe Pasquale.

System components

- | | |
|-----|---|
| 218 | Controller interfaces Unibus, VERSAbus, and Ethernet products |
| 220 | Collision free LAN provides stability under all network loads |
| 222 | Peripheral controllers provide high throughput for Multibus systems |
| 226 | Vendor independent small computer networking system |
| | Linear predictive coding system synthesizes speech in real time |
| 228 | Time interval scope with picosecond accuracy and resolution |
| | Token passing local area network system hooks to 500 devices |
| 230 | Data communications |
| 233 | Computers |
| 234 | Integrated circuits |
| 244 | Interconnection & packaging |
| 246 | Interface |
| 248 | EMI protection |
| 248 | Data conversion |
| 250 | Software |
| 252 | Microprocessors/microcomputers |
| 254 | Test & measurement |
| 258 | Peripherals |
| 261 | Memory systems |
| 262 | System elements |

Departments

- | | | | |
|-----|-------------------------|-----|------------------------|
| 3 | Up front | 267 | Designer's bookcase |
| 11 | Publisher's perspective | 268 | System showcase |
| 11 | April preview | 270 | Advertisers' index |
| 17 | Editorial | 272 | Career opportunities |
| 22 | Letters to the editor | 275 | Reader inquiry card |
| 264 | Calendar | 275 | Change of address card |
| 266 | Literature | | |

Designers' preference survey*

- 241 Microprocessors,
ICs & modules

Editorial reviewers for parts of this issue:

Arthur H. Seidman
Ralph Preiss
Dennis Allison

*Appearing in Domestic issues only

A fully programmable digital storage plug-in: Tek 7000 Series Scopes pay off again!

For the price of a single plug-in, you can now convert your Tek 7000 Series scope to powerful digital storage. Or take advantage of this new productive digital dimension to invest in the high-performance 7000 Series scopes for the first time. The 7D20 is the latest and most rewarding dividend to the 7000 Series plug-in concept—a concept that keeps your scope current not only with each new application, but with new scope technology as well.

As you expect, Tektronix packed the 7D20 with capabilities well beyond anything comparable, beginning with the power to store, recall, magnify and reposition waveforms at will. A sampling rate of up to 40 MHz offers single-shot bandwidth performance to 10 MHz and 70 MHz for repetitive signals. Waveform storage and dual channel inputs let you record, display and compare up to three pairs of simultaneous events or six independent signals. You can



store up to 10 divisions (full-screen) of pre-trigger data, or delay up to 1500 divisions, always with sharp, jitter-free displays.

A convenient self-monitoring envelope mode captures and displays subtle variations among random events, so your time is spent more productively. Enveloping reveals otherwise difficult to detect amplitude and frequency deviations such as a missing pulse and jitter.

Also included are signal averaging for reducing uncorrelated

noise of a repetitive signal. On-screen cursor read-out. Non-volatile memory storage for up to six front panel settings. And extensive self-diagnostics. All designed to improve measurement accuracy and repeatability, save you time and eliminate guesswork.

IEEE-488 interface is built-in. You have the option to delegate repetitive measurements or other long-term monitoring tasks to a controller, facilitating complete and accessible documentation. Tek's Standard Codes and

Formats makes programming and bus control unusually easy.

Plug into the digital world now. Affordably. Powerfully. The 7D20 is an exceptional value. It is a dependable investment in more productive time. More creative opportunities. And in greater versatility than ever from the expanding 7000 Series. Talk to your Tektronix Sales Representative soon, or contact:

U. S. A., Asia, Australia, Central & South America, Japan

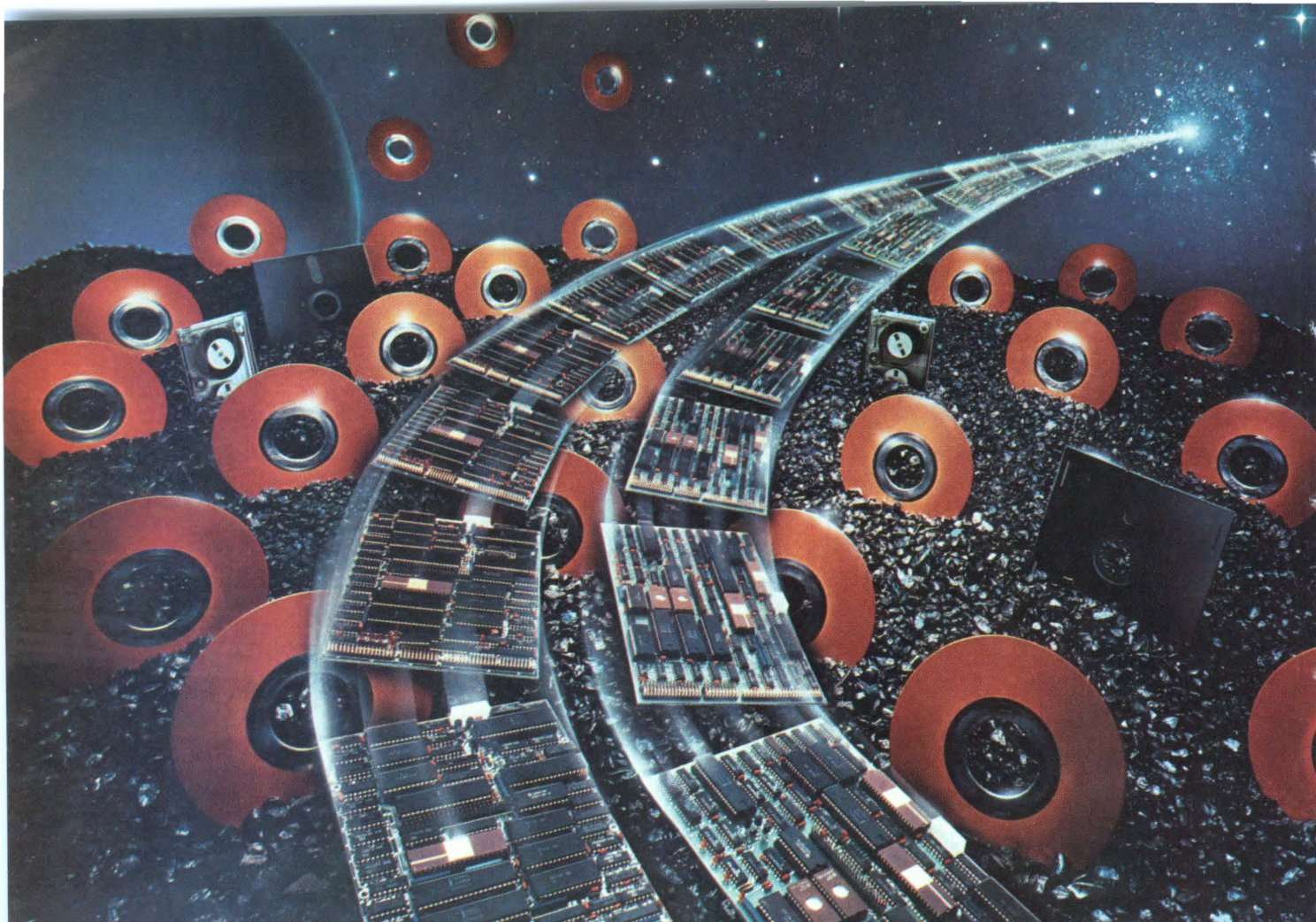
Tektronix, Inc.
P.O. Box 4828
Portland, OR 97208
Phone: 800/547-1512
Oregon only: 800/452-1877

Europe, Africa, Middle East
Tektronix Europe B.V.
Post Box 827
1180 AV Amstelveen
The Netherlands
Telex: 18312

Canada
Tektronix Canada Inc.
P.O. Box 6500
Barrie, Ontario L4M 4V3
Phone: 705/737-2700

The Answer By Any Measure

Tektronix
COMMITTED TO EXCELLENCE



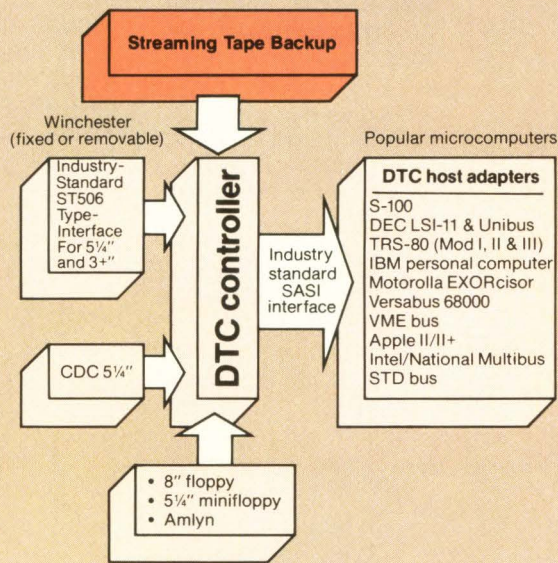
DTC Controllers for Little Winchesters with **Tape Backup.**

One controller does it all. Supports two Winchesters, fixed or removable, in 5.25" or 3 +," and streaming tape. Offers selective direct tape access or automatic save/restore. Programmable for different drive types. Complete with host adapters that link full-featured Winchester/tape backup control with your favorite micro. It's the new 540 from DTC.

Available from Arrow, Hamilton/Avnet, Kierulff, and more than 25 international distributors. Or order in OEM quantities direct from DTC. For information, circle our readers' service number. For faster response, call (408) 496-0434. In the East, call (617) 275-4044.

Easier system integration

DTC drive enclosures can simplify integration of drives, controller, power supply and cabling. Call us.



Data Technology Corporation
2775 Northwestern Parkway
Santa Clara, California 95051
Telephone (408) 496-0434 TWX 910-338-2044
East Coast (617) 275-4044

CIRCLE 7

Now distributed by Wyle

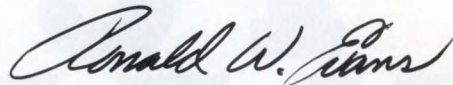
Bridging the communications gap

Swiftly growing and approaching maturity, data communications is one of the most influential sectors in system technology today. However, our editors will be the first to point out that, like any adolescent, it is not without its growing pains. Ironically, the most evident shortcoming in the data communications market is a lack of communication—among manufacturers, system integrators, and end users.

With a lack of universally accepted standards—along with a proliferation of communication media, network configurations, and protocols—we need to pause long enough to weigh the tradeoffs of various emerging standards. Instead, we continue to expand our universe before establishing a firm base on which to build.

To guide travelers in this data communications market, the editorial staff has stopped in its track and dug in its heels in an attempt to find some reliable paths through the communications maze. The result, in this month's Special Report, is a close look at recent innovations in local area networks, chip technology, and new architecture, just to mention a few key areas.

The influence of data communications on the computer industry is so pervasive, it has spread to specialized application niches including factory automation. Thus, in *Computer Design's* April Premier Edition on automation and control, the editors again pause in their exploration to look at the impact of local area networks along with other important technologies in factory automation. Be sure to catch that extra April issue for an in-depth view of yet another beneficiary of the emerging data communications industry.



Ronald W. Evans
Publisher

APRIL PREVIEWS—A DOUBLE HEADER

April 6: Special Report on Development and Testing

One of the design engineer's most commonly used development tools is now the logic analyzer. In an examination of this workhorse instrument, a staff editor will illustrate its impact on the design of powerful microprocessor based systems and will describe some presently available analyzers. Supporting articles include a manufacturer's viewpoint on logic analyzers, protocol simulation testing, and a designer's management information system for system development.

April 21: Premier Edition on Automation and Control

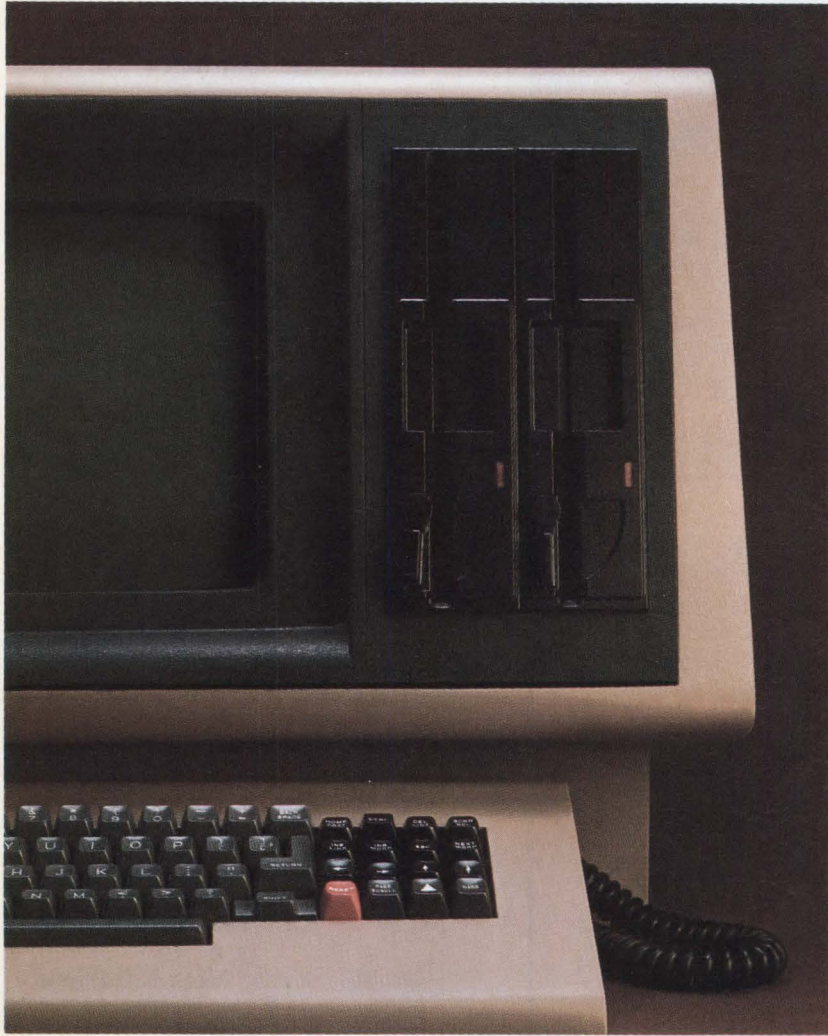
Many of the greatest advances in the design and application of computer based systems are surfacing for use in the automation and control of manufacturing processes. Thanks to the microprocessor, such systems are proliferating. Beginning with staff written reviews of single-board analog/digital I/O systems and microcomputers, this Premier Edition will contain articles from industry experts on artificial intelligence (expert systems), machine vision, I/O boards for personal computers, distributed control, and several phases of software.

**OUR NEW
8" DRIVES
PUT US
IN A TIGHT
SPOT.**

They're half the height of a conventional 8-inch floppy.

The exact depth of a standard 12-inch CRT terminal.

And actually capable of squeezing 8-inch drive performance into desktop systems that haven't room for full size 8-inch drives.



What's more, they're Shugart's newest family members—our SA810 single-sided and SA860 double-sided floppy disk drives.

These half-height 8-inch drives offer the OEM more design flexibility, while providing an attractive new alternative to today's minifloppies.

Unlike other reduced height drives, only Shugart's SA810/860 series eliminates the need for major redesigning of hardware. And software. And controllers.

Because they're compatible with our industry standard SA801/851 8-inch drives. Same mounting holes. Same internationally recognized DC power supply. Same controller interface. And all the jumper options you need to build in the features you need.

They're also compatible with the existing user base of over 200 million 8-inch diskettes.

And the SA810 and SA860 offer distinct advantages over 5¼-inch drives, including more capacity. In the case of the SA860 (1600 kilobytes), 60 percent more than a double-sided 96-TPI minifloppy. With faster access times (89 msec versus 158 msec average). And faster transfer rates (500 versus 250 kilobits per sec).

They also offer a bundle of features not found in conventional 8-inch drives.

The rapid start DC motor, for example, eliminates the need for belts, pulleys, and head-load solenoids. So reliability is substantially increased. Media wear is reduced. And overall operation is much quieter.

All of which makes our new SA810/860 drives the smart solution for a wide range of high performance desktop

applications—from word processing to distributed network systems.

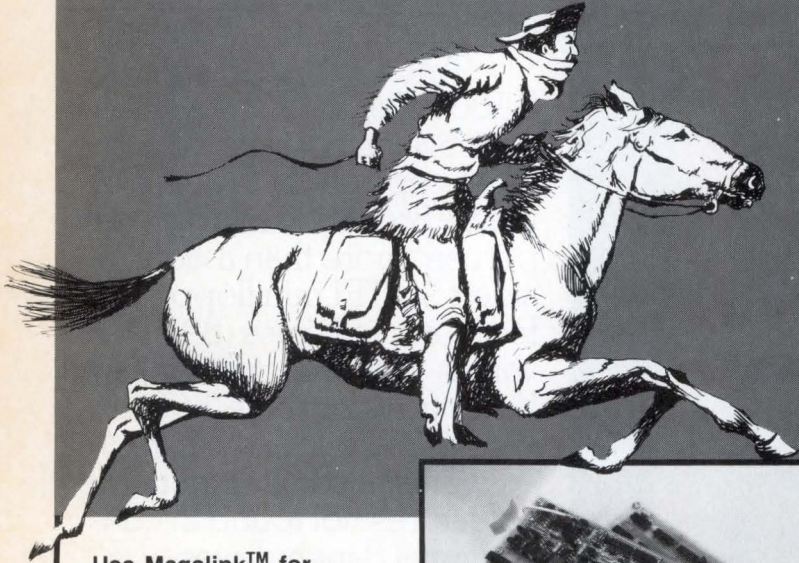
All backed by the industry's largest and most experienced engineering, sales and service organizations.

For more details, contact Shugart Associates, 475 Oakmead Parkway, Sunnyvale, CA 94086, (408) 733-0100 (Hamilton/Avnet, authorized distributor).

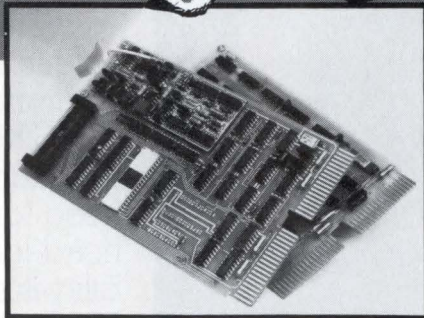
And see if you can squeeze us in.

Shugart
Right from the start.

Looking for a faster processor-to-processor communications link?



Use Megalink™ for
1 Megabit/sec DMA transfer
between multiple DEC and
Intel processors on local
networks up to 32,000 feet
long.



- Q bus, Unibus, and Multibus compatible units plug directly into DEC and Intel backplanes.*
- Multidrop operation of different processors on single coaxial cable for distributed networks.
- Integral 1 Megabit/sec FSK modem is immune to baseband noise, has better than 1 bit/10¹² error rate.
- Loadable RT-11, RSX-11M, and RSX-11S device drivers available on floppy disk.
- Virtual disk subsystem.
- HDLC protocol implemented in hardware.
- Polled, token pass, or CSMA contention networks possible.

Call Garry Stephens today at (203) 544-9371, or write now
for specifications of Megalink DMA Interface Units

COMPUTROL

Division of Kidde Automated Systems, Inc.

KIDDE

15 Ethan Allen Highway
Ridgefield, CT 06877-6297 USA
203-544-9371
Telex 643358

*DEC, Q bus, and Unibus are trademarks of the Digital Equipment Corporation.
Intel and Multibus are trademarks of the Intel Corporation.

COMPUTER DESIGN

Editor in Chief **Saul B. Dinman**
Executive Editor **Michael Elphick**
Managing Editor **Sydney F. Shapiro**
Technical Editor **Chris Brown**
Senior Editor **Peg Killmon**
Associate Editor **Deb Highberger**
Assistant Editor **Mary Therese Cipar**
Senior Copy Editor **Suki Adams**
Copy Editors **Colleen Feeny**
Linn Kurkjian
Editorial Assistant **Jocelyn J. Melanson**
Western Editorial Staff
Managing Editor **Tom Williams**
Field Editor **Sam Bassett**
540 Weddell Dr, Suite 8,
Sunnyvale, CA 94086, Tel: 408/745-0715
Field Editor **Joseph A. Aseo**
5199 E. Pacific Coast Highway, Suite 303A,
Long Beach, CA 90804, Tel: 213/597-6894
Production Manager **Linda M. Wright**
Asst Production Manager **Lou Ann Morin**
Production Assistant **Philip Korn**
Design Consultant **Ken Silvia**
Technical Art **Designline**

Publisher **Ronald W. Evans**

Director of Marketing **Gene Pritchard**
Marketings Services/PR Mgr **Linda G. Clark**
Promotion Manager **Tom Hodges**
Advertising Coordinators **Cherie LaFrance**
Sally H. Bowers

Circulation Director **Robert P. Dromgoole**

Controller **David C. Ciommo**

Computer System Manager **Ken Spiewak**
Data Services Manager **Wanda Holt**
Data Services Assistant **Sue Bowker**
Editorial & Executive Offices
119 Russell St, Littleton, MA 01460
Tel: 617/486-9501

PennWell
PUBLISHING COMPANY

Chairman of the Board **P.C. Lauinger**
President **Philip C. Lauinger, Jr.**
Senior Vice President **Joseph A. Wolking**
Group Vice President **H. Mason Fackert**
Group Vice President **Carl J. Lawrence**
Vice President/Finance **V. John Maney**
Vice President **L. John Ford**

Open the door to a new UNIX™ performance environment.



Exciting new doors are opening up for UNIX™ users. The Gould CONCEPT 32/87 is the key. Now there's a powerful alternative for the VAX-bound user. Running the authorized version of Bell Laboratories' UNIX operating system, the Gould CONCEPT 32/87 benchmarks at triple the performance of the VAX 11/780*. This new processing power can make you more productive. Whether you are dealing with VLSI design, molecular modeling, or simulation processing, the 32/87 has the versatility and performance you need for increased productivity.

Now Gould S.E.L. minicomputers offer a comprehensive ICSC-Ada** language translator to open new doors into the state-of-the-art DOD

language environment. The ICSC-Ada translator operates in conjunction with the C compiler under UNIX to enable users of Gould computers to learn Ada and to develop programs to satisfy emerging Ada requirements of military and scientific computer applications.

Let us open new doors to performance and productivity in your compute-bound UNIX environment. Just call or write.

Gould Inc., S.E.L. Computer Systems Division,
6901 West Sunrise Boulevard,
Fort Lauderdale, Florida 33313 1-800-327-9716.

*UNIX is a trademark of Bell Labs

**VAX 11/780 is a trademark of Digital Equipment Corporation

***ICSC-Ada is a proprietary software product of Irvine Computer Sciences Corporation. Ada is a trademark of the U.S. Department of Defense.

 **GOULD**

Electronics & Electrical Products

THE NEW CHROMATICS CT4200



WITH OUR 2 YEAR GUARANTEE
\$3995

NOBODY ELSE DELIVERS SO MUCH RELIABILITY FOR SO LITTLE MONEY.

- Best price/performance color terminal on the market.
- 512 x 512 x 4 Bitmap image, 512 x 384 viewable.
- No flicker 60 Hz refresh rate.
- 85 characters by 48 lines alphanumeric display.
- High resolution 13" precision in-line CRT.
- Optional 1024 x 1024 x 4 with 1024 x 768 viewable.
- 2 year limited warranty on all parts and factory service.
- Supported by many popular graphics packages.
- Quantity discounts available.

Chromatics

For full product information on the best price/performance color terminal in the business, contact:
Chromatics, Inc./2558 Mountain Industrial Blvd./Tucker, Ga. 30084/Telephone: 404/493-7000/TWX: 810/766-8099.
Offices Worldwide

CIRCLE 12

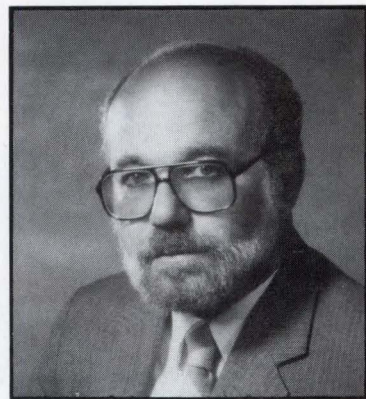
OUR MAGAZINE GROWS WITH THE INDUSTRY IT SERVES

Next month will mark another first in *Computer Design's* continuing efforts to keep pace with both the computer industry and your individual information needs. In April, you will be receiving two separate issues of *Computer Design*. One will be our regular monthly issue, while the second will be dedicated to the field of automation and control.

Over the past several years, the computer systems business has been evolving into a number of specialized, vertically oriented markets. Tracking this growth, we have organized each month's editorial coverage into a number of subcategories that address pertinent market areas. However, as the industry expands, information content in some fields snowballs until it becomes impossible to do it justice in a small subsection of a regular monthly issue.

Our solution to that problem, therefore, will be to devote extra issues of the magazine to rapidly growing vertical industry segments. Thus, in April we will publish a Premier Edition of *Computer Design* that is entirely dedicated to computer systems technology in automation and control—from machine vision to process control. Within that field, as always, we will strike a balance among the various subdisciplines: computers, peripherals, software, and system design.

We hope that you will share our excitement about this extra edition of *Computer Design*, which the staff is busily putting together at this moment. Beyond that, our editors are looking ahead to NCC and other important upcoming events in this dynamic industry.



Saul B. Dinman

Saul B. Dinman
Editor in Chief

Best Technical Article of the Month—August
“A Virtual Breakthrough for Micros”
John F. Stockton, Motorola Semiconductor Products Inc

This article will now compete with other monthly winning articles for the 1982 editorial excellence award.

THE CHIP HEARD



© 1983 The "WORLD-CHIP" is a trademark of Advanced Micro Devices, Inc.

AROUND THE WORLD.



Washington. Bonn. Tokyo. Paris. Now there's a complete single-chip modem that speaks all the different specs.

It's the only FSK modem you'll ever need.

It's the Am7910 from Advanced Micro Devices.

THE Am7910: THE WORLD-CHIP™ MODEM.

To send or receive, just select the spec. Any spec: Bell 103, Bell 202, CCITT V.21, or CCITT V.23. The Am7910 automatically takes over from there.

No drift. No tuning. No lie.

And you don't need any additional precision components. The WORLD-CHIP modem modulates, demodulates and filters. All digitally. It operates half duplex at 600 and 1200 bps, full duplex at 300 bps.

It has everything. RS-232 interface. Auto-answer and Loopback modes. Low-speed back channels. Terminal hand-shaking controls. And all operating modes can easily be selected by an MPU.

IT WILL LEAVE YOUR COMPETITION SPEECHLESS.

The WORLD-CHIP modem will put you as far ahead of the competition as we are. And it's just one of our high-performance VLSI circuits.

There are controllers, bipolar and MOS microprocessors, communications and signal processing circuits, and more.

And every part in every family meets or exceeds INT-STD-123, the International Standard of Quality.

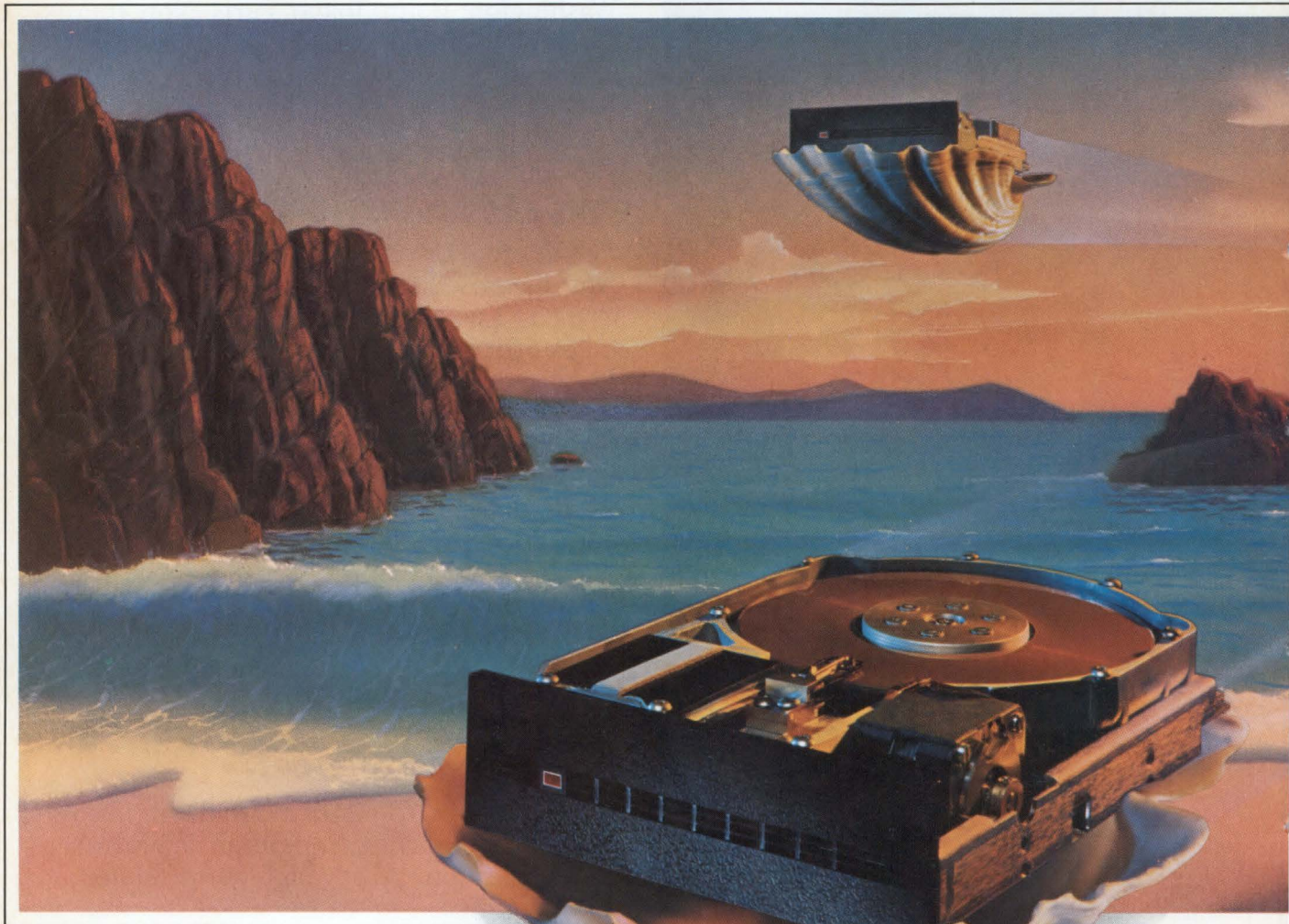
Pick up the phone, call AMD, and find out more about the WORLD-CHIP.

It's even better than it sounds.

Advanced Micro Devices

901 Thompson Place, Sunnyvale, CA 94086 • For direct factory response call (408) 749-3774.

5 Mb on the half-



Seagate Technology down-sizes the Winchester again. Now you can store five megabytes on-line in half the height of our standard 5¼" Winchesters.

Our new half-high ST206

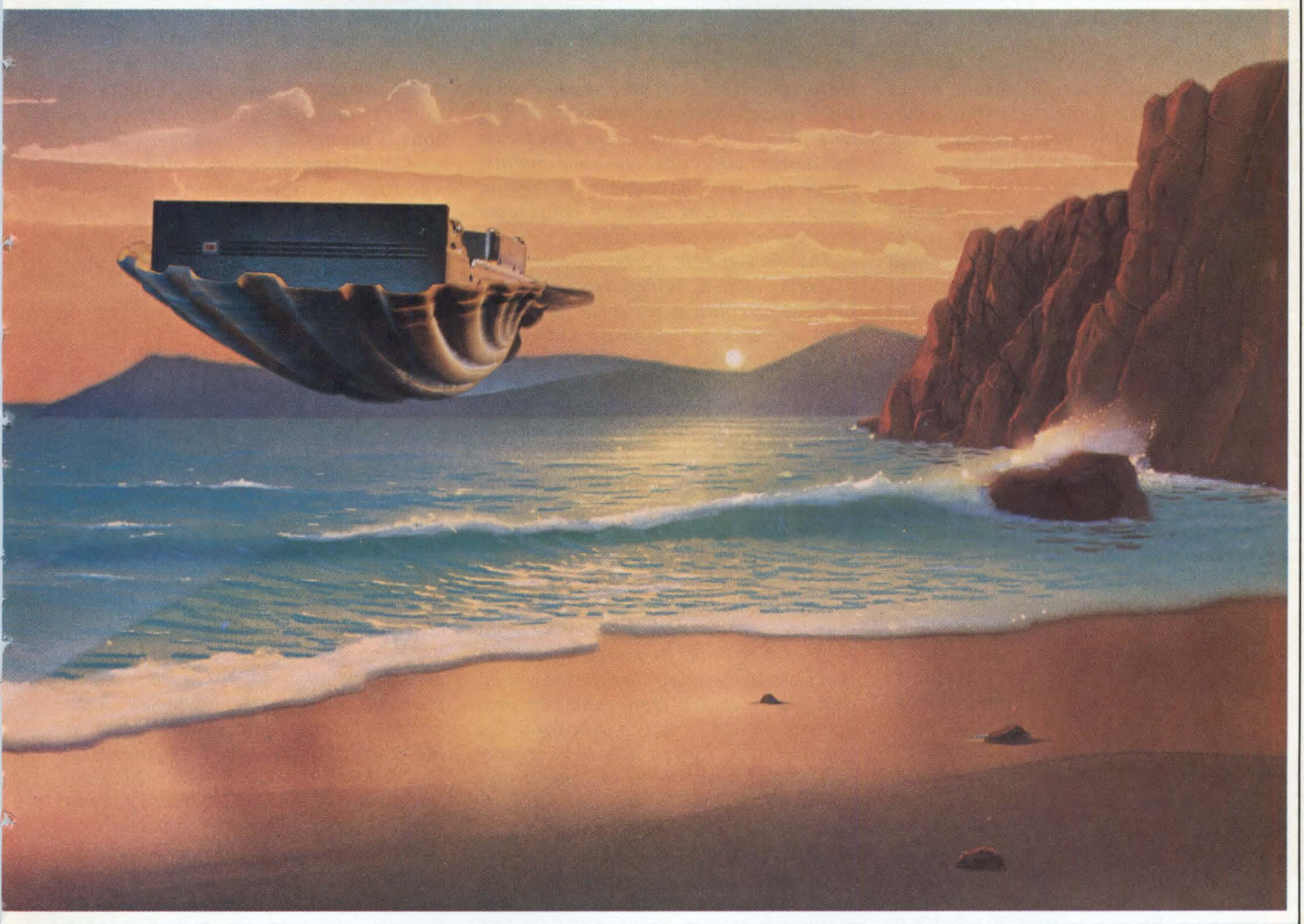
offers the same five megabytes (formatted) of storage capacity in a new, low-profile design. And we've included rugged plated media for even greater reliability.

The perfect half-high companion.

Now you can fit two half-high discs, our new ST206 and any half-high minifloppy in the same space as our standard Winchester. The ST206

Advanced Micro Devices

Shell, from Seagate.



the perfect size for your new, low-profile system designs. It's also rugged enough for portable applications.

Nothing has changed but the size.

The half-high ST206 has the very same capacity and

interface as the OEM's favorite Winchester—the Seagate ST406 and our ST706 removable cartridge Winchester. It's just smaller.

Shrinking the cost of Winchester.

We've reduced more than

size. The ST206 is an excellent value. Especially in volume.

Get small now.

Evaluation units are available now. So don't wait for promises. Call Seagate today and get five megabytes on the half shell.

Seagate Technology



360 El Pueblo Road, Scotts Valley, California 95066 (408) 438-6550, TELEX 172114 SCVL
Regional Sales Offices: Hopkinton, Massachusetts (617) 435-6961; Newport Beach, California (714) 851-9964; Richardson, Texas (214) 783-6711; Schaumburg, Illinois (312) 397-3727
European Sales Office: Kreillerstrasse 21, 8000 Munich 80, West Germany, 89-43-13-900, TELEX 5 213 379

Authorized U.S. Distributor: Arrow Electronics

"Turning the tide in disc technology"

© 1983 Seagate Technology

CIRCLE 14

Finding fault

Regarding John H. Wensley's article, "Fault tolerant systems can prevent timing problems" (Nov 1982, p 211), I am concerned that some important issues appear to have been overlooked, certainly in his article, and possibly in the design of the Series 300 computer.

The operating system is not detailed. Does it provide for self-restart on faults? Does it operate any memory protection schemes? Indeed, there is no real detail about software fault tolerance, except voting and synchronization. Does the software use stacks (not usually recommended in fault tolerant systems)? Are there hardware diagnostic routines included? Is data integrity checked internally (eg, by the use of checksums or access flags)?

Mr Wensley's description of the inter-processor communication for the purpose of voting particularly worries me. The implication is that communication is achieved by use of some shared memory resource or similar scheme. This approach has its own special problems. Any hardware that can be accessed by two or more processors can be vulnerable to what I shall call "resource locking." Resource locking is applicable to such resources as memory, buses, I/O ports, etc. A hardware or software failure in one processor, while it is accessing such a shared resource, can effectively lock other processors out of this resource unless there is some independent means of override such as a timeout in the bus arbitration scheme or the ability of the other processors to force disconnection of the faulty unit (this latter method includes its own added risks). If access to the locked resource is essential to the correct functioning of the remaining processors, then the system will fail.

Mr Wensley gives no account of precautions against resource locking, although it can disastrously affect the interprocessor communications—the mainstay of his redundancy scheme. Failure to take such precautions can lead to the complete nullification of the system redundancy; a single fault is able to wreck the whole system. If precautions were taken, they are important enough to be included in the article; if they were not, the design must be considered flawed!

D. Fosberry
TechScicon Ltd
3, Gladstone Villas
Albion Rd
Kent, England

Asking for tolerance

Mr Fosberry raises several issues that can properly be regarded as central to the design of a fault tolerant computer. Unfortunately, it is not possible in a single paper, and even more so in this letter, to cover all such issues. The Series 300 design addresses all these points, many of which have been covered in other articles and with its conceptual predecessor, the SIFT computer.

The first major points concern the operating system. It includes a full complement of routines for error detection, error correction, diagnosis, and reconfiguration. Voting assures data integrity between the three processing channels. In addition, where large blocks of data are manipulated (eg, in disk transfers or communication channels), then checksums and other coding techniques are used to ensure data integrity.

Questions were raised about inter-processor communication and resource sharing—a particular aspect of ensuring "fault isolation." In the Series 300, this is assured not by using a bus system, but by providing point to point communication links designed so that the maximum disturbance that a faulty unit can produce on another unit is a delay of a few microseconds. I agree with Mr Fosberry that shared bus systems in general present problems in providing adequate fault isolation.

Finally, resource locking is important. The design avoids this problem by not using any shared resources. Each processor has its own memory and its own input/output bus structure. The only connection between them is the communication link that, as mentioned above, can produce at most a delay of a few microseconds in one channel in the event of a fault.

I would like to thank Mr Fosberry for raising these issues.

John H. Wensley
August Systems, Inc
18277 SW Boones Ferry Rd
Tigard, OR 97223

Welcome to Sparta

I began reading the editorial "Technical Creativity and the Edifice Complex" (Nov 1982, p 11) with great expectations. I was eager to read about comparisons of management styles on R & D. Instead, it turns out the only real difference between the mind set of typical American Big Business and the High

Tech Exec is clothing. One prefers three-piece suits, the other, designer jeans and fashion tops (both cost about the same).

A most intriguing comment implied that Spartan environments, a "sea of cubicles made from movable partitions," do not affect creativity. Somehow the image of a huge office, lined with rows and rows of identical cubicles reeks of 1984 with all of its standardization, mass production, and numbers instead of names. I don't think creativity is enhanced in Orwellian environments.

Kirk Ireland
National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95050

Countdown...1984

I didn't say that I agreed with the observations, I was simply reporting them. I concur with your views on creativity and an Orwellian environment. In my opinion, we're already close to 1984, both temporally and philosophically. The problem with putting complex technology (eg, database management) in the hands of anyone (eg, a bureaucrat) is that it doesn't take a genius to translate the power of such a technology, once readily accessible, into personal or political power. We live in an era of roulette-like power politics based on the fear of total destruction—all this brought about by the reduction of a complex technology to a 38-cent red button.

—S. B. D.

Museum seeks support

I am very honored to be included in the Computer Design Pioneers (Dec 1982). And I am particularly pleased that *Computer Design* is taking this historic approach. Both Ken Olsen and I have a special hobby of preserving the history of this industry. Last year, we began to realize our dream with the opening of The Computer Museum as a public non-profit charitable foundation. But to really work, it must have the support of the entire industry.

Individuals are invited to join such pioneers as Gene Amdahl, Ed DeCastro, Jack Kilby, Ivan Sutherland, Gordon Moore, Bob Noyce, Ken Olsen, and Al
(continued on page 24)

LIGHTING THE FUTURE

With
Fiber Optics Technology

OIS

- OIS high-speed fiber optic transceivers for NASA Space Shuttle Data Acquisition Network
- Hundreds of OIS long-haul telecommunications systems installed in the U. S. in a one year period
- OIS fabricated custom wafers for semi-conductor laser devices used in a classified military communications program
- OIS pulsed lasers are used in nearly 50% of the commercial optical time domain reflectometers in the U. S.

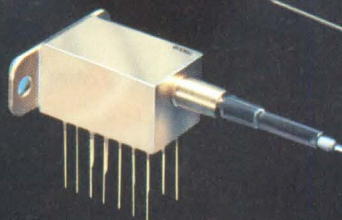
From components, systems, to custom applications... high technology that performs



FS-100 High Quality Video Transmission System

- S/N ratio at 12 Km typically 67 db
- Meets RS-170, NTSC-7, RS-250-B (short-haul) video transmission standards
- Space saving configuration — 1³/₄" high x 19" rack mount
- On-line status indicators for laser operation in transmitter unit
- Temperature controlled laser transmitter

CIRCLE 15



OL 8200 InGaAsP 1300 nm Laser

- Available in hermetically sealed DIP w/50 micron fibre pigtail
- Laser diode mounted on thermo-electric heat pump
- Each laser fully burned-in and tested to meet spec
- 15 mA threshold current
- Under 1 ns rise and fall time
- 3 mW power output

CIRCLE 16



OL-1010 AlGaAs Pulsed Laser

- Low Threshold current — 1 amp
- Hi-slope efficiency — 0.8 w/a
- Under 500 ps rise and fall time
- Very low pulse to pulse jitter
- Customized packages available with various windows, lens cap or fiber pigtail

CIRCLE 17

Optical Information Systems Inc. • 350 Executive Boulevard, Elmsford, N.Y. 10523
(914) 345-5850 • TELEX 64-6174

(continued from page 22)

Shugart, and become individual Founders of the Museum by sending in a personal, tax deductible check for \$250 or more.

In addition to individual support, we are also gathering support from across the industry for The Computer

Museum. Again, we have established a Founder's program for corporations for \$2500. You might be interested to know that Data General, ComputerWorld, The British Computer Society, Fujitsu, Intel, and a broad range of organizations have subscribed to this program.

One final suggestion is that you would also send a copy of the December *Computer Design* for the Museum's growing archives and library. Eventually, we hope to have videotaped talks from all the major historic figures in the industry and work to preserve all significant artifacts, photographs, and relevant documentation.

Gordon Bell
Board of Directors
The Computer Museum
1 Iron Way
Marlboro, MA 01752

... THE NEED
An easy, low cost way to input
visual information to your computer

... THE SOLUTION
DIGI-CAM



With the DIGI/CAM Self-Contained Digital Camera, your computer gains a new dimension in I/O flexibility.

Completely self-contained with its own internal microprocessor, DIGI/CAM will interface to any computer through an RS 232 serial port.

Since it is fully programmable using simple ASCII commands, using it is very simple. Besides being the "electronic eye" of your computer, you can program it to compare pictures, locate objects within a picture, detect motion, or to take timed, multiple exposures.

With a 128 x 256 pixel resolution and up to four gray levels, DIGI/CAM can be used in process control and automation, robotics, security graphics input and digitizing, quality control, or ... ?

BEST OF ALL ... we are extending our introductory offer of only \$395 for the complete system including lens.

A NEW DIMENSION IN VISUAL INPUT.

See for yourself. Or better yet ... now your computer can see by itself!

FOXVILLE
COMMUNICATIONS
CORPORATION

7741 E. Gray Road, Suite #17
Post Office Box 5419
Scottsdale, AZ 85261
(602) 948-9817
Telex 165 750

Kudos

Your special segment on *Computer Design Today* (Dec 1982) would make a valuable complement to textbook materials in our course on computer design. Would you be kind enough to donate 100 copies to the Electrical Engineering Dept at the University of Rhode Island? The copies would be distributed to 100 senior students in electrical engineering and computer science.

Louis Scharf
Electrical Engineering Dept
University of Rhode Island
Kingston, RI 02881

Your "Data Communications Technology" piece in the Dec 1982 issue (p 211) was definitely a "keeper." As a matter of fact, it is now required reading for all of our new salespeople.

Norman Brust
Contel Information Systems, Inc
130 Steamboat Rd
Great Neck, NY 11024

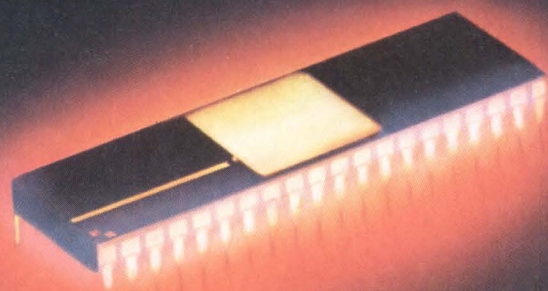
You asked for rated interest of the *Computer Design Today* article, "Input/Output Technology" (Dec 1982, p 157). Although I rate it as "high," I would like to add that it was highly interesting, very topical, all embracing, and most useful.

Congratulations to Mr Richard Parker, the author, who did a fine job.

J. Peter Cunliffe
Movement Control, Inc
Transportation Systems Engineering
Management and Operations
972 Town & Country Rd
PO Box 5367
Orange, CA 92667

**INTEL
INTRODUCES
TURBO-CHARGED
MICRO-
PROCESSING.**

**THE FASTEST,
EASIEST,
MOST EFFICIENT
WAY TO BOOST
SYSTEM
PERFORMANCE.**



Introducing a revolutionary advancement in microprocessor system design.

Intel Coprocessors.

They work much like a turbocharger in an automobile. Dramatically increasing the power of your CPU, by "kicking-in" whenever specific functions are required.

Intel Coprocessors are an architectural triumph. Processor extensions. Beyond peripherals. They're designed for complete compatibility with Intel microprocessors, boards and systems.

Everything that's needed to boost your power is on one chip. Not a bag of parts.

And no "kluge" of parts can equal the performance, the ease of use, or the cost effectiveness.

There's the 8087 and the 80287 Numeric Coprocessor. Made to work with the Intel iAPX 86 family of 8 and 16-bit processors. Both Coprocessors have the power to accelerate your floating point math calculations an incredible 50 to 100 times. Eliminating the need for a mini-computer in the process.

And there's the 8089 I/O Channel Coprocessor. Capable of tripling your performance in the I/O-intensive parts of your application. Such as in hard disk control and communications.

Intel is the only company with a family of Coprocessors. For the component, board and system level. All being delivered in production quantities, now. With new types of Coprocessors on the way.

Like the 82730 Text Coprocessor.

The first VLSI solution for fast manipulation and display of high-quality text.

And the 82586 LAN Coprocessor. Replacing 100 IC's for Ethernet,* or other Local Area Network designs.

The competition has yet to produce their first Coprocessor.

Typical Performance Improvements with Math Coprocessor
(All Clock Speeds 8 MHz.)

	8086	8086 + 8087
Double Precision (64 bit) Floating Point Multiply	1,313 μ S	1.7 μ S
Interest Rate Calculation	628 mS	.66 mS
3-D Graphics Image Generation	90.5 seconds	1.78 seconds
FORTRAN Whetstone Calculations	3K Whetstones per second	169K Whetstones per second
Real Matrix Multiply	134 seconds	4.08 seconds

Discover just how powerful and cost-effective Coprocessors can be.

For complete documentation, including application notes, call us toll-free. **(800) 538-1876**. In California, **(800) 672-1833**. Your information will be on its way in less than 24 hours.

Or write us. Dept. F3, 3065 Bowers Avenue, Santa Clara, CA 95051.

Or contact your Intel Sales Representative.

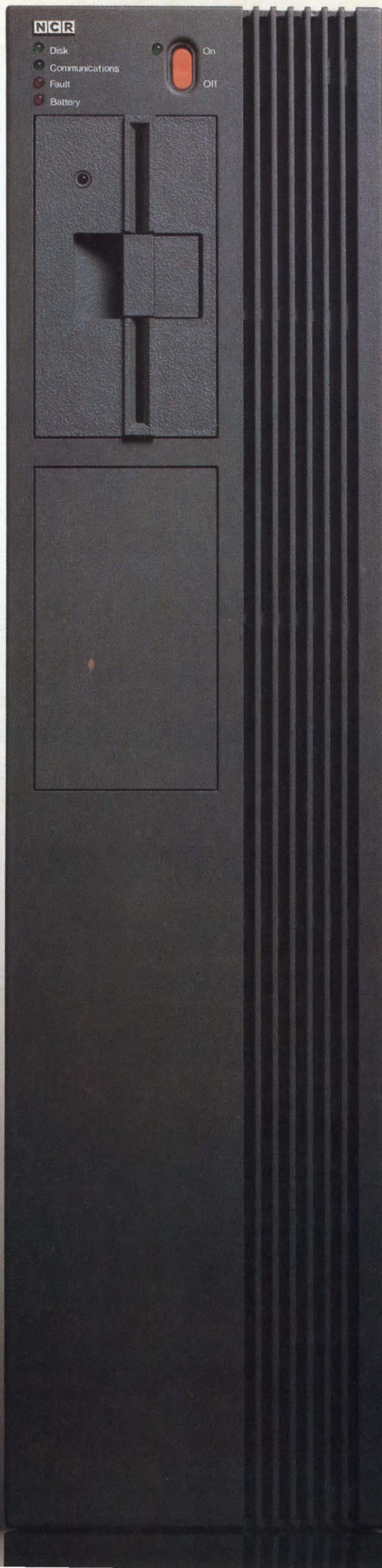
And don't be alarmed by our enthusiasm when you ask about Coprocessors.

We're just charged-up.

intel[®] delivers
solutions

United States and Canadian Distributors: Alliance, Almac Electronics Corporation, Arrow Electronics, Avnet Electronics, Hamilton/Avnet, Hamilton Electro Sales, Harvey, Kierulff Electronics, Inc., L.A. Varah, MTI Systems Sales, Mesa Technology Corporation, Pioneer, Wyle Distribution Group, Zentronics. In Europe and Japan, contact your local Intel Sales Office.

*Ethernet is a trademark of Xerox Corporation.



NCR

• Disk

• Communications

• Fault

• Battery

On

Off

TOWER 1632. IT TOWERS OVER THE MINICOMPUTER. AND FITS UNDER A DESK.

Tower™ 1632.

The power and performance of a minicomputer. At the size and price of a micro.

Only 29 inches tall. Yet it casts its shadow over everything before it. And, upon the system builder with the foresight to sell it, it will confer a truly towering advantage.

This single sleek package conceals as much as two megabytes of memory. Plus 60 megabytes of mass storage. And up to 5 additional add-on modules (each seven inches wide) can boost mass storage to one billion bytes.

Tower 1632's capacity to interface is equally vast. From networking to peripherals, it's as ready for the future as it is right for today.

We enhanced its full-scale UNIX* operating system for maximum software capability and flexibility.

And the NCR name guarantees maximum support, with more than 16,000 field engineers around the world.

But we've barely begun to explore the ground floor. Call us to learn more about this towering achievement.

The OEM price starts under \$10,000. The performance never stops.



BUILT FOR SYSTEMS BUILDERS.
TOWER 1632.

NCR
OEM Marketing Division

CIRCLE 20

NCR Corporation, World Headquarters, OEM Marketing Division, Dayton, OH 45479. Nationwide (800) 222-1235. In Ohio (513) 445-2380.

*UNIX is a trademark of Bell Laboratories.

Committees push to standardize disk I/O

Standardization efforts for disk drive I/O interfaces have been many and have generally fallen within the confines of larger efforts by the American National Standards Institute and the International Standards Organization, through various technical committees. Unfortunately, as with any evolutionary process, a misunderstanding has arisen as to what is in fact an adopted standard, and what is merely a proposed standard. Furthermore, differences, no matter how minor, are bound to surface between proposed standards and the original, temporary standards upon which the proposed standards are based. This occurs even though manufacturers of products already on the market may claim compatibility with both.

What is happening in disk drive I/O interface standards becomes clearer by examining more closely which American National Standards Institute (ANSI) technical committee is doing what work, and the status of that committee's work. Most of the I/O interface standards work is taking place in ANSI through the X3T9 I/O Interface Committee, which reports to the X3 American National Standards Committee. The X3 Committee's realm involves standards for computers and information processing.

Working in parallel with ANSI is the International Standards Organization (ISO) through its SC13 and parent TC-97 committees. Although ANSI is represented on ISO's TC-97 Committee, those ISO approved interface standards are not necessarily ANSI standards, and vice versa. Despite the lack of a formal mechanism for interorganizational consultation, ANSI or ISO will sometimes try to get its standard approved by the

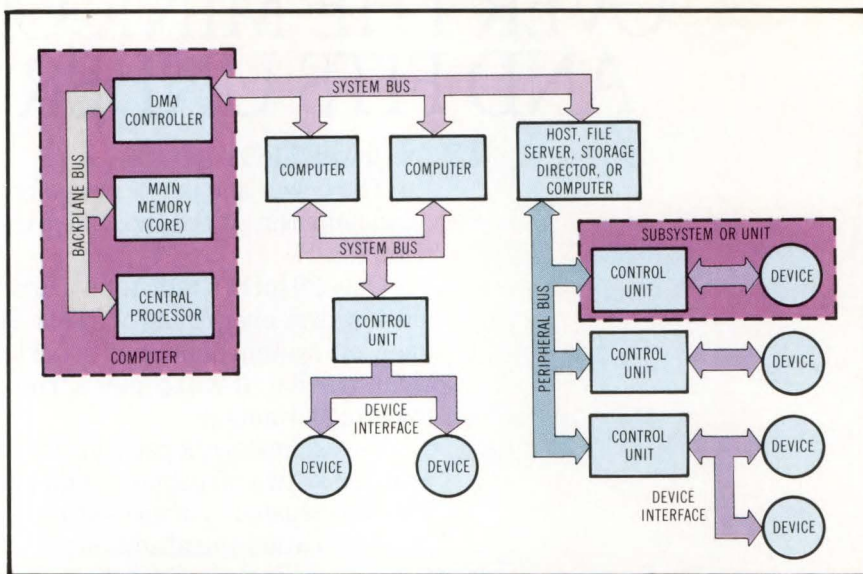


Fig 1 The ANSI X3T9 Committee is developing interface standards for backplane, system, device, and peripheral buses. All except the backplane concern disk drives as well as other peripheral products. The backplane bus relates to CPUs, DMA controllers, and main memory, but not peripherals.

other. However, approval is by no means certain.

Realistically, ANSI standards carry more weight in the marketplace, on a worldwide scale, than those of ISO. This results from commercial practicality. The majority of the world's computer and computer peripheral products are made and shipped by U.S. manufacturers, companies that sit on ANSI standards committees.

Much of the work for developing disk drive I/O interface standards is in the ANSI X3T9.2 Committee for lower level interfaces, the ANSI X3T9.3 Committee for device level interfaces, and the X3T9.5

Committee for future interfaces. Note that the "lower level" term for the X3T9.2 Committee is an old term that meant lower in performance than the IBM I/O channel. In its modern context, it means parallel buses for mini- and microcomputers.

Four main thrusts

The ANSI X3T9 Committee's work is aimed at developing I/O interface standards for four main areas: backplane, system, peripheral, and device level buses. The last three concern I/O interface standards for disk drive as well as other peripheral products. Backplane buses such as the S-100 and Unibus connect CPUs, single-board controllers, main memory, and DMA controllers, and are thus not directly involved with disk controller interfacing.

A system bus is defined as one that connects computers, peripheral subsystems, terminal concentrators, gateways, and file servers as peers. This bus can tie computers into a network of loosely coupled processors.

A peripheral bus is defined as one that connects a single host (computer, storage director, file server, and channel) to one or more peripherals, where the peripheral includes the device (eg, disk drive) and associated controller.

A device level bus is defined as one that connects a "naked" device such as a floppy or rigid disk drive or a printer. Fig 1 illustrates all four I/O interface concepts that encompass the work of the ANSI X3T9 Committees.

(continued on page 32)

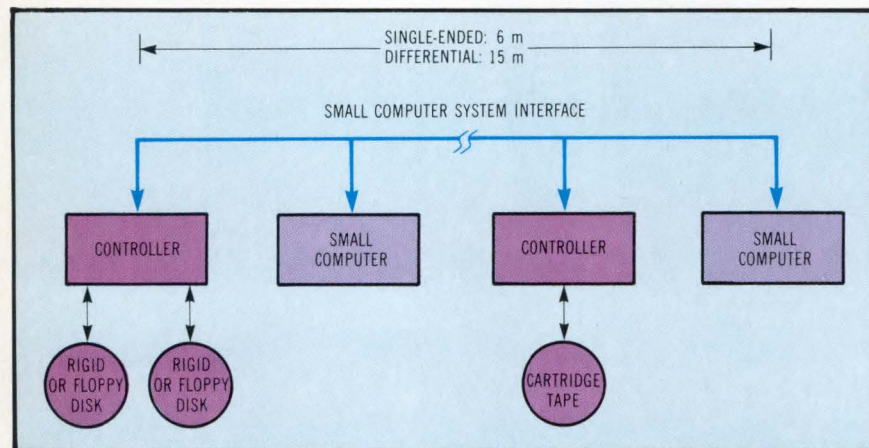


Fig 2 Proposed by ANSI X3T9.2 Committee for computers and computer peripherals, the Small Computer System Interface can operate at up to 6 m with single-ended flat ribbon or to 15 m twisted pair cable. Up to eight devices can be attached.

It's not Magic, it's NEC.



Spinwriters[™] and disk drives with supernatural reliability.

NEC peripherals are amazingly reliable. For example, our Spinwriter[™] printers often run two years without a failure. Typically, our Winchesters run more than five years without a failure. One of our diskette drives has a field-proven reliability of 24,000 hours—that's an incredible 12 years in normal operation between unit failures. When the rare failure

does occur, usually it can be fixed in less than 30 minutes.

So when you think peripherals, think NEC. For Spinwriter letter-quality printers, band printers and line printers. For Winchesters. For diskette drives. High performance peripherals that just keep running. It's not magic, it's NEC.

Spinwriter is a trademark of
Nippon Electric Co., Ltd.

NEC Information Systems, Inc.
5 Militia Drive, Lexington, MA 02173

- Have a representative call me.
- Send more information on NEC Peripherals.

Name _____
Title _____
Company _____
Address _____
City _____ State _____ Zip _____
Telephone _____ CD No. 3/83

NEC
NEC Information Systems, Inc.

Push for standards

(continued from page 30)

System bus efforts within the X3T9 Committee's jurisdiction include the Local Distributed Data Interface (LDDI) and the Small Computer System Interface (SCSI). Peripheral buses include the Intelligent Peripheral Interface (IPI) and the ISO's DP7069 standard proposed by the ISO's SC13 Committee. Device level buses include a floppy disk interface (approved as an ANSI standard X3.80-1981 and based on an industry *de facto* standard), the Storage Module Drive (SMD) Interface (approved as an ANSI standard X3.91-1982) for 14" disk drives, a rigid disk interface for high performance small Winchesters and some 14" disk drives (not yet approved as a standard), and a quarter-inch cartridge tape drive interface (in early stages of proposal).

Systems buses proposed

The ANSI X3T9.2 Committee has proposed the SCSI as a system bus for connecting computers and computer peripherals (Fig 2). The committee has submitted an early draft to the European Computer Manufacturers Association (ECMA) for further consideration. SCSI allows up to eight computers and peripheral controllers to communicate with one another (any one of the eight nodes can talk to any of the remaining nodes) over 6 m of a single-ended 50-conductor flat ribbon cable using 48-mA drivers (up to 15 m of 50-conductor flat ribbon or twisted pair cable for differential versions). Data can be transmitted at up to 5M bytes/s (synchronously) and at up to 2M bytes/s (asynchronously).

Designed for distributed bus arbitration, the proposed interface standard is suitable for floppy disks, all 5¼" and 8" Winchesters, and medium performance (eg, SMD) 14" rigid disk drives, as well as streaming tape drives. This interface has a relatively high level peripheral command set and includes commands for common peripherals.

SCSI is very similar to SASI (identical according to many experts), the interface proposed by Shugart Associates (Sunnyvale, Calif). In fact, SCSI evolved from the original SASI document. Opinions differ, however, among interface experts on the differences between SASI and SCSI, at least the original version of SASI. Some interface experts claim the SCSI proposal is SASI; however, other experts strongly dispute this.

Aside from the fact that the X3T9.2 Committee cannot endorse a standards proposal that is associated with a company name, such as SASI, the disputed differences between SASI and SCSI seem

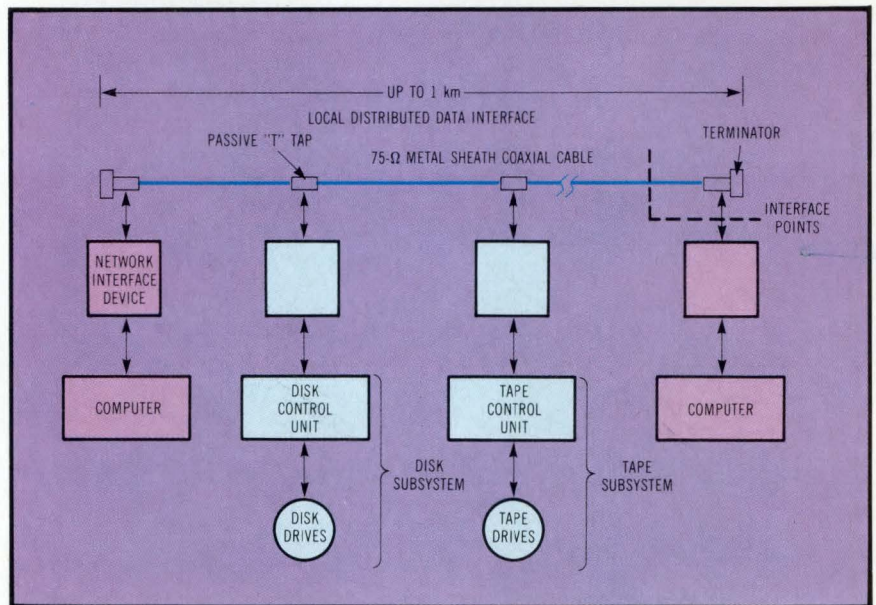


Fig 3 Essentially a local area network, the Local Distributed Data Interface is proposed by the ANSI X3T9.5 Committee for communication among eight computers or peripherals at up to 1 km. At shorter distances, more devices could be connected.

centered around the command sets. SCSI has a more precisely defined document, whereas SASI is more vague in some areas.

Here again, however, experts disagree. Some contend that it is difficult to define SASI. They also point out that SCSI allows system arbitration by any of the eight devices on the bus (any of the eight can act as the system controller), whereas SASI allows only one device to act as a controller. In addition, the lack of a seek command in SASI means that a CPU must waste valuable time while a peripheral is seeking its track. With SCSI, the CPU is not tied up by any one peripheral device until that peripheral is ready to read data.

In fairness to SASI, it has been undergoing many revisions and improvements by Shugart Associates since the first version was proposed about three years ago. Actually, the Shugart revisions and the X3T9.2 Committee's work on SCSI represent two attempts to arrive at the same thing and to narrow down whatever differences exist, without greatly impacting those products already in use and now being shipped with SASI compatibility.

Back in 1979, Shugart Associates asked Data Technology Corp (Santa Clara, Calif) to come up with the first TTL implementation of SASI—an implementation that is part of many products now in use. Many contend that the Data

Technology implementation is only a minimal SASI implementation and does not represent the full capability of SASI. From that perspective, perhaps it is easier to understand why some experts feel that SCSI and SASI are different. However, it should also be remembered that SCSI is a natural and evolutionary step following a proposed interface standard by an industry giant like Shugart Associates. Thus, some differences can be expected, no matter how small or insignificant.

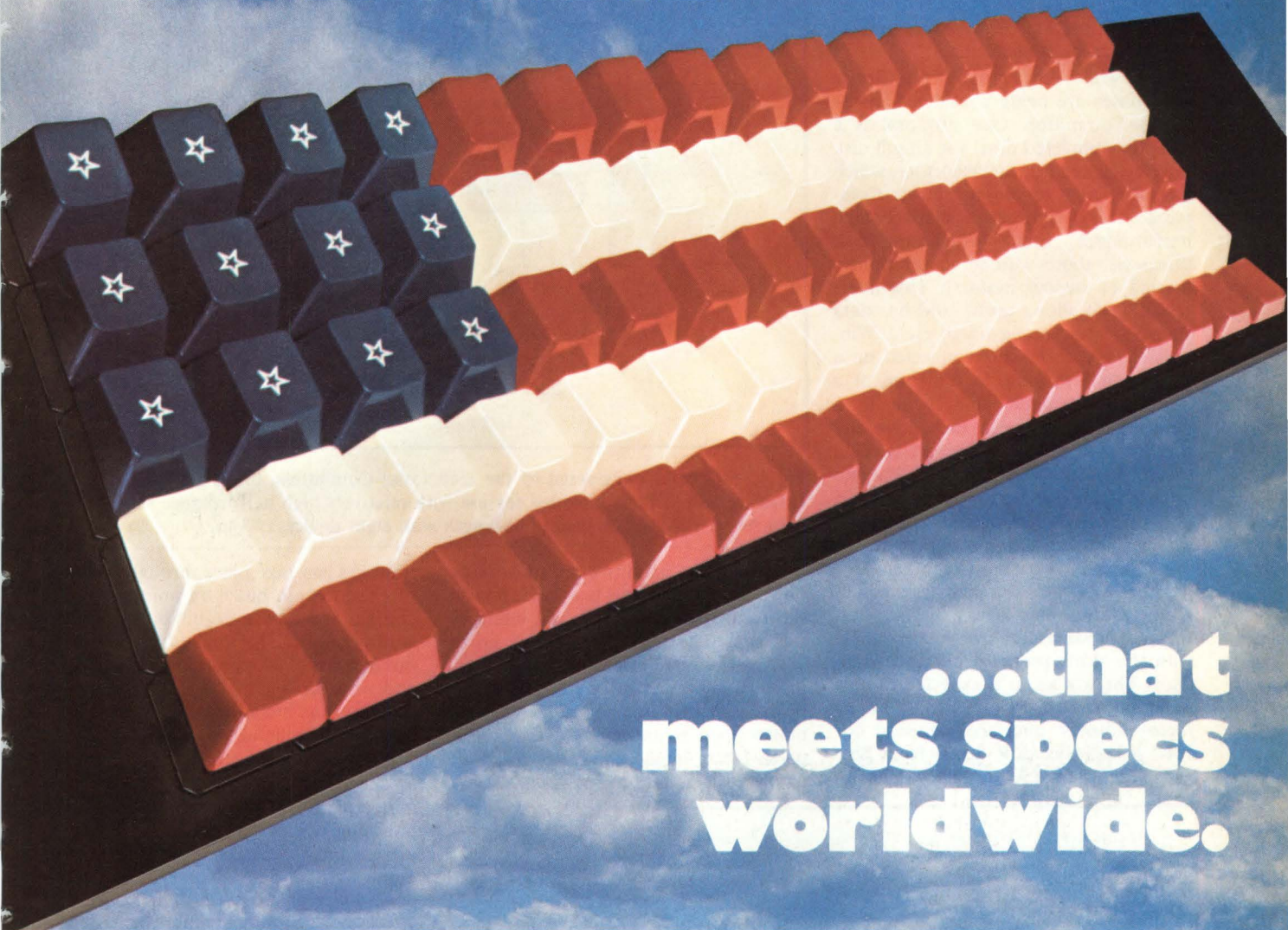
Meanwhile, many major disk drive and peripheral controller manufacturers are shipping products they claim are both SASI and SCSI compatible. This makes it credible that SASI and SCSI are very similar, if not the same. It also indicates that even if some differences exist between SASI and SCSI, they are so small that a user could take care of them with some software changes. After all, very few interfaces are perfect enough to guarantee no software changes.

A local network proposal

Still another system bus interface proposal is LDDI, now in the X3T9.5 Committee (Fig 3). LDDI is essentially a local area network that allows up to eight computers or peripheral devices to communicate with one another over a 1-km maximum distance through network access devices. The bus uses a prioritized

(continued on page 34)

THE ALL AMERICAN KEYBOARD



...that
meets specs
worldwide.

Cherry's new DIN-compatible foam pad capacitive keyboard:

- Low enough in profile to meet 1985 European ergonomic standards.
- Low enough in price to be your most cost-efficient spec.

Now, Cherry's proven foam pad capacitive technology is available in a low profile, linear feel, full travel key-module. A keymodule that's ideal for detached encoded keyboards. With a uniquely simple design requiring only five parts and a snap-in angled foam pad for hysteresis to prevent teasing. New ergonomic cylindrical button set with non-glare keycaps.

Another Cherry first is our new hex sense amplifier with six inputs that allow horizontal rows of keys to be attached with minimal printed circuit complexity... requires only six I/O lines from a microprocessor for operation. An inexpensive microprocessor that provides ASCII or other codes, N-key rollover, serial output and bi-directional serial interfaces.

Send today for complete technical and application data.



Just .704" (17.88mm) from PC board to keycap top of home row!

CHERRY 

KEYBOARDS

CHERRY ELECTRICAL PRODUCTS CORP. 3614 Sunset Avenue, Waukegan, IL 60087 • 312/578-3500

CIRCLE 22

Push for standards

(continued from page 32)

carrier sense multiple access accessing scheme and transmits data at 50M bps. Information is sent serially over a 75-Ω coaxial cable. For distances shorter than 1 km, more than eight computers or devices can be connected.

Meanwhile, other proposals for device level buses are being considered in the X3T9.3 Committee. One proposal is a recently completed draft for a rigid disk interface standard, the BSR X3.101, which has been sent to the parent X3 Committee. It is optimized for relatively high performance, small Winchester disk drives (ie, those with servo positioners instead of stepper motors). This interface (Fig 4) allows up to 10M-bps data transfer rates among up to eight Winchester disk drives interconnected on a bus up to 3 m long, in the form of a 50-conductor ribbon cable. It calls for a data separator between each drive and the interface line for bit-serial data transfers. This interface uses 24- and 40-mA single-ended control bus signals plus differential serial data and clock lines. The bus has parallel command bytes.

At the 1982 National Computer Conference, 12 Winchester disk drive manufacturers and 7 controller manufacturers showed products that were compatible with this draft proposal interface standard. The BSR X3.101 is expected to be a potential competitor to the ST-506 *de facto* industry interface standard for 5¼" Winchester disk drives from Seagate Technology (Scotts Valley, Calif).

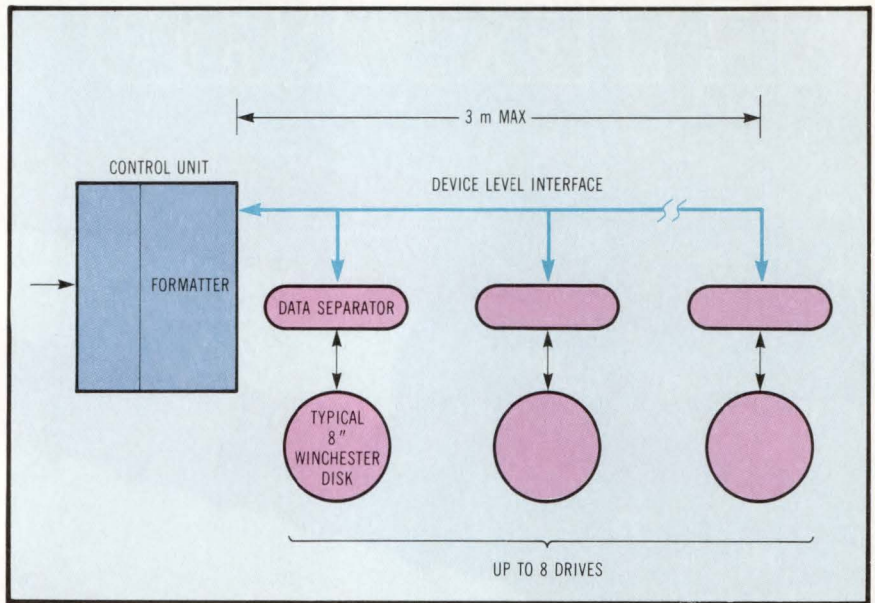


Fig 4 Still being considered by the ANSI X3T9.3 Committee, the Rigid Disk Interface BSR X3.101 is intended for use with relatively high performance small Winchester drives. Maximum bus length with eight devices is 3 m.

The X3T9.3 Committee is also working on another device level bus that is now in the form of a draft proposal interface standard. The IPI (Fig 5) allows up to eight peripheral devices (ie, disk drives, printers, tape drives, CRT terminals) to be daisy chained to a host controller in a master/slave arrangement, over a bus of up to 125 m long. It allows 8- or 16-bit data transfers at up to 5M bytes/s. Data

transfers can take place through the use of either a split bus 8-bit unidirectional configuration or a 16-bit bidirectional configuration. The single daisy chained bus consists of 24 signals, has centralized and prioritized arbitration of interrupt requests, and includes command sets for common peripheral devices.

Four electrical/cable configurations have been proposed by the X3T9.3 Committee for IPI: a 3-m maximum flat ribbon cable with 3-state and open collector drivers and TTL receivers, a 15-m maximum twisted pair ribbon cable with open collector drivers and high threshold receivers, 5-m maximum coaxial ribbon cable, and a 125-m maximum coaxial cable with open emitter drivers and receivers. The IPI's relatively long distance (up to 125 m) and high data transfer rate of 5M bytes/s make it useful for high performance 14" Winchester disk drives with large capacities of stored data.

Acknowledgment

The author would like to thank the following individuals for their valuable help in preparing this report: Tom Thawley, Engineering Director, Interphase Corp (Dallas, Tex); Larry Bucher, President of Adaptec Inc (Milpitas, Calif); William E. Burr of the National Bureau of Standards (Washington, DC) and chairman of the ANSI X3T9.2 Committee; and Gary S. Robinson of Digital Equipment Corp (Maynard, Mass), chairman of the ANSI X3T9.3 Committee.

—Richard Parker, Contributing Editor

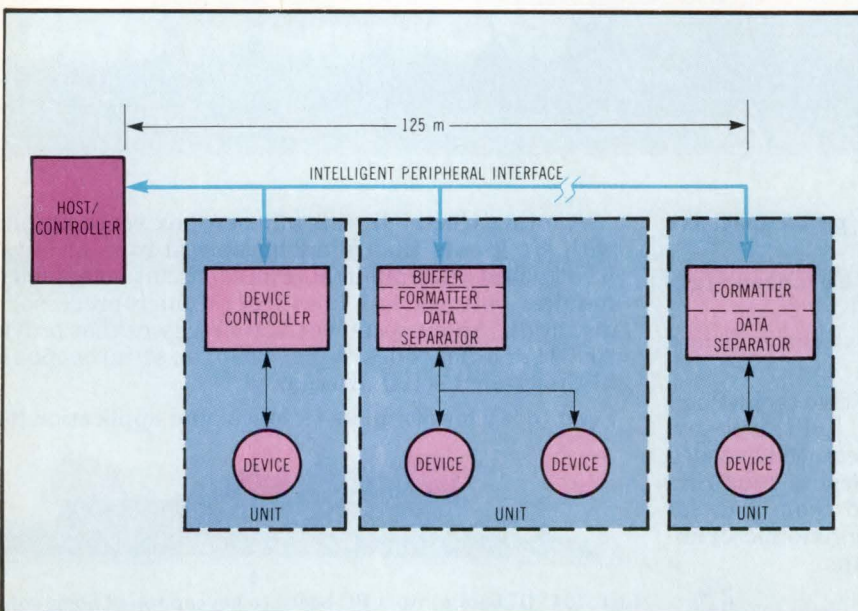


Fig 5 The ANSI X3T9.3 Committee has drafted a proposal for the Intelligent Peripheral Interface that will operate at up to 125 m. Data transfers occur on split bus 8-bit unidirectional or 16-bit bidirectional configurations.

EXPAND YOUR MULTIBUS SYSTEM'S OUTER LIMITS.



XYLOGICS HAS SOLD MORE HIGH PERFORMANCE MULTIBUS PERIPHERAL CONTROLLERS TO MORE MAJOR OEMs THAN ANYONE.

That's a fact. But it's sometimes obscured by the breadth and popularity of Xylogics' full range of peripheral controllers for mini and micro computers.

Yet for Multibus™ systems employing 68000, 8086 or Z8000 class microprocessors with large capacity disk and tape drives, no other Multibus controllers offer better performance or more advanced features.

NEW 450 AND 472 CONTROLLERS JOIN POPULAR XYLOGICS 440.

For the past three years, the Xylogics 440 peripheral controller—the industry's first Multibus SMD controller—has offered the highest peripheral control performance in Multibus benchmark tests and customer installations.

Now Xylogics has developed two new advances in Multibus periph-

eral control: the 450 and 472.

Together, they set the standard for price, performance and size for IEEE-796 Multibus applications.

The new Xylogics 450 peripheral controller provides even more performance for Multibus disk control applications. The 450 can address up to 16MB of memory and control up to four SMD disk drives at data rates of up to 1.8 MB/sec. non-interleaved.

The new Xylogics 472 is a high performance, single-board tape controller for streaming and start-stop tape drives. It can address up to 16MB of memory and control up to four tape drives—running at speeds from 12.5 ips to 125 ips and at densities of 800 bpi NRZI, 1600 bpi PE, 3200 bpi, or 6250 bpi GCR.

The 440, 450 and 472 feature advanced channel control tech-

niques and are designed to work together for system optimization. For Multibus users, this means low bus usage, non-interleaved disk operation and true high-speed streaming with no repositioning. All three work with any 16, 20 or 24 bit address Multibus system.

Xylogics. The leader in high performance Multibus peripheral control.

™ Multibus is a registered trademark of Intel Corp.



144 Middlesex Turnpike, Burlington, MA 01803

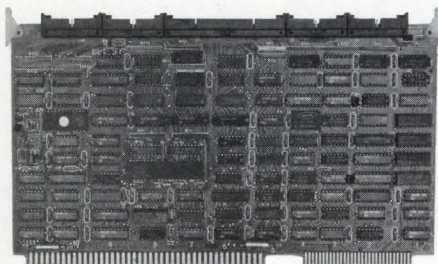
Tel: (617) 272-8140 TWX: 710-332-0262

Xylogics European Headquarters: (Slough, U.K.)

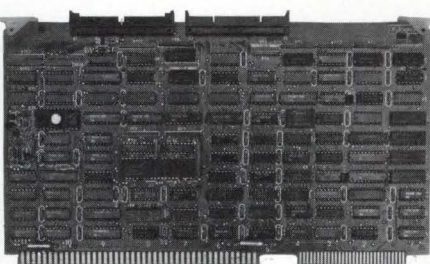
Tel: (0753) 78921 Telex: (851) 847978

Xylogics Germany (Eschborn)

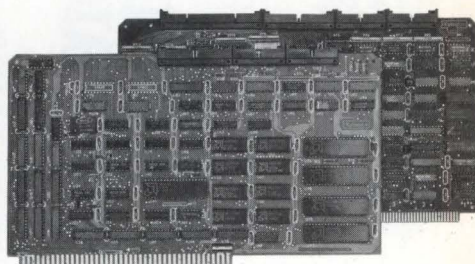
Tel: (49) 6196-47004



Xylogics 450 Multibus Disk Peripheral Controller.



Xylogics 472 Multibus Tape Peripheral Controller.



Xylogics 440 Multibus Disk Peripheral Controller.

Digital's new multi-user, multi-tasking Micro/PDP-11™ gives you all the microcomputer you need to solve your application problems. At a price almost anyone can afford—\$9,200.*

The Micro/PDP-11 is a powerful micro that's small enough to fit just about anywhere. It's available in rack mount, floor mount, and table top versions. And includes CPU, a 10 Mb 5¼" Winchester, 800 Kb floppy back-up, and auto-self diagnostics for I/O, CPU and mass storage.

But what puts the Micro/PDP-11 in front of all the others is what's behind it.

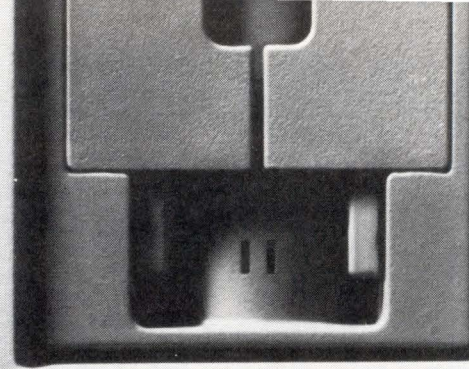
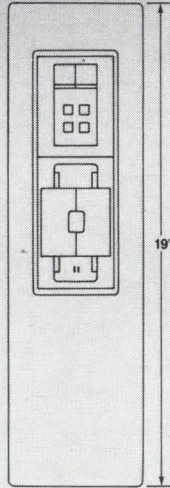
More software. Over 2,000 developed applications for laboratories, factories, offices, and other businesses. And thousands of PDP-11 trained programmers ready to write even more.

A wide choice of operating systems. Including RSX-11, RSTS/E, RT-11, DSM-11, MicroPower/Pascal, and UNIX.**

A variety of languages such as BASIC, FORTRAN-77, COBOL-81, C, DATATRIEVE, PASCAL and DIBOL.

Thousands of peripheral hardware interface products.

And the support of Digital's worldwide team of over 18,000 sales



and service professionals. Ready to answer any question. Or solve any problem.

The Micro/PDP-11. No other micro can stand up to it.

For more information, send in the coupon. Or call 800-225-9222 and ask for information package XX-000.

Send to: Digital Equipment Corporation,
HL2-1/E10
77 Reed Road, Hudson, MA 01749.

- Please send me more information on Digital's Micro/PDP-11.
- Please have a Digital Sales Representative contact me.

My application is _____

Name _____

Title _____

Company _____

Street _____

City _____

State _____

Zip _____

Phone _____

CA-3-83

**More than
a micro.**

*Quantity one, U.S. Prices only

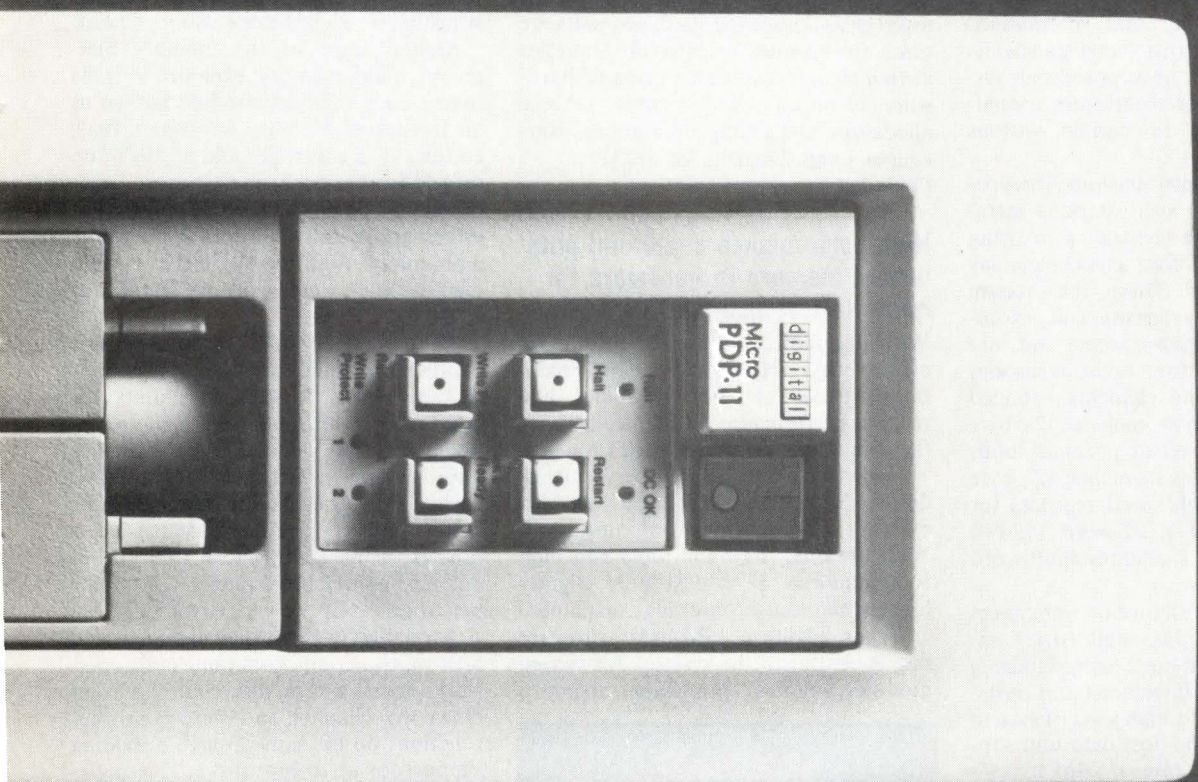
**UNIX is a trademark of Bell Laboratories.

©Digital Equipment Corporation 1983

digital

Actual size: 5¼" x 19"

No other micro
can stand up to the Micro/PDP-11.



Multiple-processor system supports pipelined architecture with multiple cache memories

Extending its reputation for offering unique system solutions to large scale computer users, Burroughs Corp announced its latest, the B7900. Members of the family include the single-processor B7900F with 12M-byte memory, the dual-processor H version with 24M-byte memory, and the 3-processor K model with basic memory capacity of 36M bytes.

The system's distributed architecture is based on multiple specialized functional processing units. These units—central processing module, host data unit, and auxiliary processor—each have a different capacity and orientation. Assigned in various configurations within the asynchronous processing system, each processor contributes specialized performance to handle various workloads.

Combining parallel and pipeline processing techniques with extended memory concepts, the central processing module consists of four asynchronously operating elements. These, the program control unit, data reference unit, execution unit, and memory access unit, are complemented by four cache memories that keep operating elements supplied with data. Memories include 12k-byte code cache for capturing program loops and working set code segments; 12k-byte data cache, 32 high speed registers for staging data; and a 32-word (52-bit) aging queue that facilitates multiword data stores.

Within the input/output subsystem module, the host data unit (HDU) has three host dependent ports each containing two message level interface (MLI) ports. These ports supply a high level of system I/O throughput. The host data unit supports an I/O burst rate of 24M bytes/s and addresses 96M bytes of memory.

The universal I/O subsystem is configured with I/O base modules each having up to eight microprocessor driven peripheral processors called data link processors (DLP). Each DLP contains at least one microprocessor, a peripheral interface, and buffer memory. Up to 32 DLPs can be used within the universal I/O subsystem.

When configuring multiple systems with shared peripheral subsystems, each I/O base module connects physically with up to four MLI ports. Each of its DLPs is assigned to one HDU at a time but may be transferred through console commands.

The auxiliary processor within the universal I/O subsystem module acts as an additional resource processor and is code compatible with the central processor module. It can address up to 96M

bytes of memory and can perform testing of system components.

Memory in a basic system has 12M-byte capacity. This can be extended in 6M-byte increments to a maximum of 96M bytes. Memory uses 8-way phasing and supports a memory/requestor bandwidth of 72M bytes/s. To provide single-bit error correction and multiple-bit error detection, the 60-bit words contain 48 data bits, 3 control bits, a parity bit, and 8 error correcting bits.

Master control program operating system software provides resource and task management for the systems. Designed together as an integral hardware/software unit, the system architecture supplies virtual memory, compiler oriented hardware, reentrant code, dynamic resource allocation, and multiprogramming. **Burroughs Corp**, Detroit, MI 48232. **Circle 241**

High performance supermini puts virtual memory in hardware for realtime response and flexibility

With unbundled features to offer cost-effectiveness, Harris's 700 series maintains virtual memory flexibility and realtime performance. Positioned between the company's 500 and 800 series systems, 700 series machines supply performance designed to cover the gap between existing 32-bit superminicomputers. With options, the basic units add high end functions at a cost only slightly higher than that of midrange machines.

A bus having a 19M-byte/s transfer rate is central to the system. All system modules, central processor, memory

subsystem, floating point processor, cache memory, and I/O channels, connect to this bus. The CPU operates with a 300-ns cycle time overlapping instruction fetch and execution.

Supporting 48M bytes of virtual address space, the virtual memory subsystem allows users to write programs that are larger than the real physical main memory. The demand paged system is supported by virtual memory management hardware and virtual operating system. By performing virtual memory address translations in hardware rather than software, context switching is reduced along with overhead.

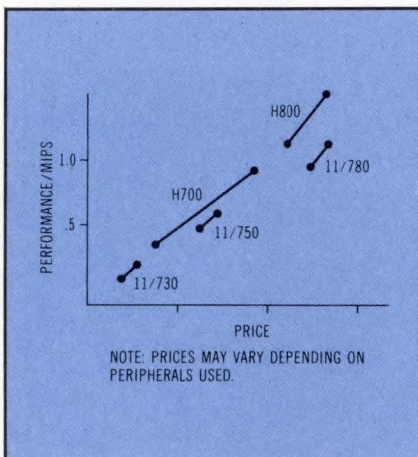
Second layer of the memory hierarchy, main memory expands to 12M bytes. Each memory module known as an Integrated Memory Subsystem (IMS) consists of a controller and arrays of up to 1.5M bytes on a single board. Error correcting logic handles all single-bit errors and detects all double-bit errors and many multiple-bit errors. Main memory cycle time is 335 ns; access time is 250 ns.

The system's optional 6k-byte cache is divided into equal stores for instructions and operands. Processor requests for data go to both main and cache memories, realizing significant performance improvements when data are found in cache. Typical cache hit rate is 90% or better. Cache cycle time is 150 ns; access time is 70 ns. With cache, the system operates with approximately 75% of the performance of the VAX-11/780.

Available for the system are integrated disk controller and communications network processor. The disk controller combines I/O channel and disk controller functions on the same board, providing support for up to four disks. The single-board communications processor simultaneously supports as many as 16 individually programmable communications lines for local or remote device connection via synchronous, asynchronous, isochronous, and X.25 protocols.

The machines derive usefulness in interactive, multistream batch, remote job entry host, and networking applications from the virtual operating system (VOS) and language processors—all designed for these environments. All H700 systems include communications network processor, operator's console, and VOS. Prices begin at \$49,900 for a machine with 384k-byte memory. Shipments will begin in the second quarter of this year. **Harris Corp, Computer Systems Div**, 2101 Cypress Creek Rd, Fort Lauderdale, FL 33309.

Circle 242



Harris's 700 series competes with superminicomputers over a wide performance range while allowing users to hold down costs through modular expansion.

Avoid being called for interference.



Oak's FTM™ keyboard. Fully shielded against RFI/EMI to meet the FCC Article 15, Class A&B deadline and VDE requirements. Right now. At the right price.

October 1, 1983 is coming fast. That's when the FCC Article 15 RFI/EMI requirements become effective. Lucky for you, the Oak FTM (Full Travel Membrane) is ready right now.

The FTM keyboard has an inherent design that offers an optional shielding system which can be easily designed right in. You don't have to re-design your equipment with cumbersome shielding. Or, wait for other types of keyboards that have added shielding with substantial added expense.

Find out how FTM keyboards block out interference. And they're available now for a surprisingly low cost.

You can't afford not to call Oak.
Phone 815/459-5000, TWX 910-634-3353,
Telex 72-2447

OAK Switch Systems Inc.

An Oak Technology Inc. Company
P.O. Box 517 • Crystal Lake, Illinois 60014

Circle 25 for Information
Circle 26 for Salesman to Call

Minicomputer eases system upgrades with multiple processors and flexible task scheduling

With easy field expansion and dynamic task scheduling, the Supramini multiprocessor system from PolyComputers Inc can handle system upgrades and various application requirements. Performance can be increased from 3 MIPS to 16 MIPS without software modification, by adding processor/memory modules. If computing and memory resources need to be reallocated to meet varying task requirements, the system operator can reassign processors and memory spaces without interrupting the affected tasks.

The system shares the Data General NOVA[®] bus structure and instruction set, with extensions to handle its multiprocessing functions. According to the company, peripherals such as rigid disk drives, terminals, and printers account for 90% to 95% of the total system cost. System integrators familiar with the Data General family can easily upgrade their multi-user/multitasking applications without extensive hardware and software investments.

Key to the system's performance and flexibility is the way the processor/memory modules and the virtual memory operating system (VMOS) are merged to provide a virtual computer with virtual memory for as many as 100 users. Each processor/memory module contains two 16-bit bipolar processors and 512k bytes of RAM, capable of supporting eight users with individual 64k-byte workspaces.

One such module is dedicated to servicing peripheral requests (eg, access to rigid disks and printer spooling) and handling interprocessor communications. From this module, the system operator can evoke VMOS commands that allocate processors to handle multiple batch streams, multiple timeshared terminals (up to four per processor), or single batch streams under end-user control. Main memory can be allocated as either working or cache.

Processors are assigned as one of three "ports": multiprogramming (MP), timesharing (TS), or batch (BT). MP ports

handle multiple batch streams under system operator control as parallel processes. The system operator can move from one MP port to another to monitor them and provide needed commands. He can create a single job stream by designating a disk file as the command source for a port. Multiple job streams can be created by assigning different files to different ports. Using dedicated MP ports to handle such tasks as payroll and report generation frees other processors to handle exclusively user-generated tasks.

TS ports differ from MP ports in that they accept command input from a remote terminal rather than the system console. Multiple tasks are also supported on TS ports so that an executing program can split itself into two or more asynchronously operating execution paths. When one of these tasks is blocked, another task can be run.

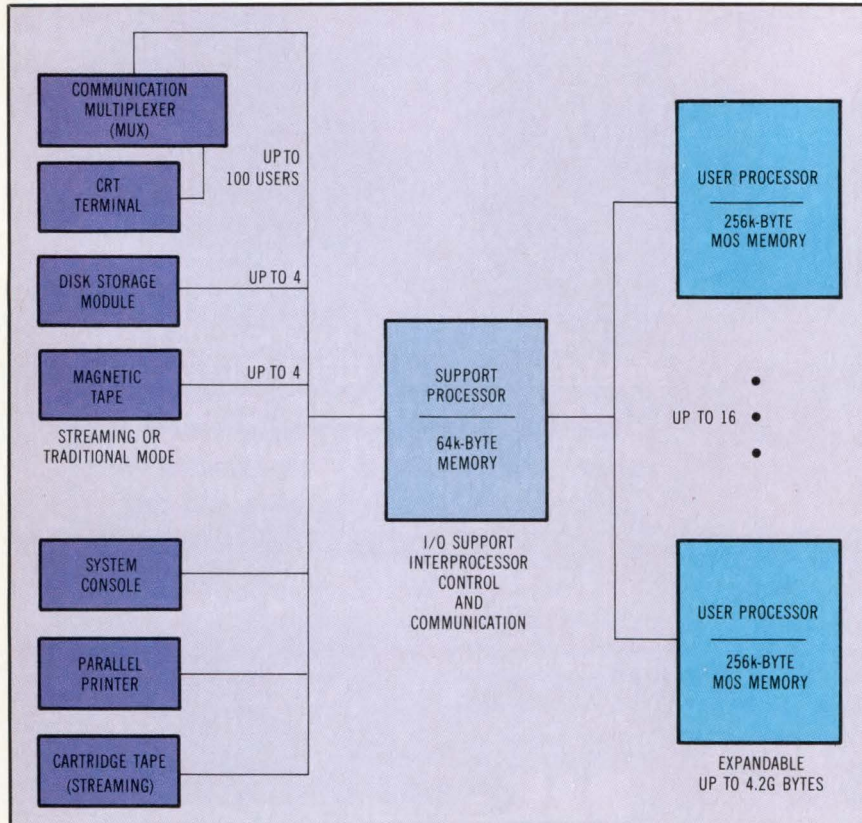
Single BT ports run under the control of TS ports in much the same manner as MP ports run under the system console. Thus, users can execute programs as scheduled tasks, while still working interactively with the system. Up to 20 asynchronous tasks can be scheduled by users in a realtime environment.

Virtual memory concepts are supported in VMOS as either working, fast storage (cache), or mass memory. All 512k-byte RAM segments on the processor boards are pooled together to provide either 64k-byte workspaces (where programs are executed and data are accessed without software intervention), or an area to store overlays if swapping is required. Any main memory not actively used as working memory is allocated as fast storage.

Code and data segments are initially stored in mass memory (Winchester and cartridge drives, as well as magnetic tape drives used for backup) when program execution begins. Segments are moved to working memory as needed. Further access to mass memory is dependent on the size of the user program and available fast storage.

When it overflows, a memory-tracking algorithm in VMOS moves code segments from fast storage to mass memory in the same manner as segments are moved from working memory to fast storage (the least used segments are at the bottom of the stack). For program execution, memory usage tends to reach an equilibrium. Frequently used code and data segments remain in working

(continued on page 42)



A dedicated processor/memory module handles only peripheral services and interprocessor communications. This frees other processor/memory modules in the Supramini system to handle program development and execution chores exclusively.

Lundy graphics terminals are setting standards because we set high standards for Lundy.

Standards: no other 3D graphics vector work-station delivers more speed or a higher IQ than the UltraGraf;™ only our color raster scan display products offer resolution as high as 1,536 × 1,024 pixels. But there's still another standard you should investigate—the one we set for our company.

Be careful. The fast-paced world of high tech breeds a lot of companies that don't survive; five years from now, many graphic terminal manufacturers won't be around anymore. Which means you could be left without service, support or enhancements.

Lundy: a company as good as its products.

That's why we think it's important you know as much about our company as our products. We're a high tech company that's been able to balance standard-setting technology with solid business sense—no small achievement.

Now, don't take our word for that, take *Forbes* magazine's instead. Lundy was on *Forbes*' Up&Coming List for 1982, a select roster of companies that look good for the long term because they've paid attention to basics: low debt load, consistently good profit picture, sound management, investment in service, support and R&D.



T5680 color raster, 3D UltraGraf™ and T5470.

Lundy maintains the largest service infrastructure—52 locations.

Our graphics terminals feature the best price/performance ratios available today.

We have developed a new software subroutine package with exceptional compatibility. Its 300 functions deliver a

new high in high powered productivity.

Lundy continues to invest in expanded R&D each and every year. Because R&D is the name of this highly competitive game—and we intend to keep setting standards.

We'll help you see more in graphics.

When you take a close look at our graphics terminals, service, support, software, systems capability, enhancements—and our company—you'll understand why Lundy can help you see more in graphics now and in the long term.

For more information, write: Lundy Electronics & Systems, Inc., Glen Head, New York 11545, or call: (516) 671-9000.



LUNDY

Mt. Everest, symbolic of aiming high, was generated on the Lundy T5680 raster. It offers 16 colors and 136 shades from a palette of 4,096 colors.



Easing upgrades

(continued from page 40)

memory or fast storage, while less frequently used segments migrate to the disk.

These virtual memory features support large application programs, with a maximum of 4M bytes of real memory backed up by 1.2G bytes of disk storage. Both multi-user timesharing and batch

processing job streams run on a common file structure (relative, indexed, and sequential). Using this structure allows concurrent file access from multiple users. Auto-index updates all files dynamically each time the data file is updated. All five supported languages

(BASIC, FORTRAN, COBOL, Wirth-standard Pascal, and ASGOL systems implementation language) also access the common file structure.

With three processors, 576k bytes of MOS RAM, a 34M-byte Winchester disk drive, quarter-inch streaming tape drive, high speed printer port, and eight RS-232 communications channels, the smallest configuration costs \$36,950 in end-user quantities of one. Also included are the VMOS operating system, one compiler, debugger, and utilities. Further software or system regeneration is not needed as processors and memory are added. A self-initialization utility in VMOS detects and uses added resources without affecting application programs or system level software.

A fully expanded system of 17 processors, 4M bytes of MOS RAM and 1.2G bytes of disk storage supports 100 users for less than \$100,000. **PolyComputers Inc.**, 18003-L Sky Park S, Irvine, CA 92714.

—Joseph Aseo, Field Editor

Circle 243

SOFTWARE

Small computer schematic design aid automates board layout

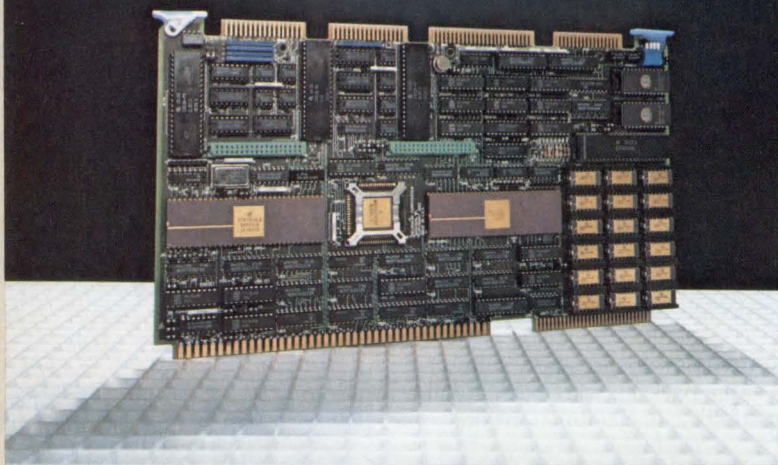
An electronic sketchpad replaces pencils, paper, and templates to design systems composed of integrated circuits and discrete components. FutureNet's DASH I (Design Aid Schematic Helpmate) adds a 640- x 360-pixel resolution graphics controller, memory expansion boards, printer/plotter, and a "mouse" for easy cursor manipulation to the IBM Personal Computer. Thus, in addition to creating, updating, and printing schematics quickly, a designer can also extract lists of materials (L/M), engineering change orders (ECOS), and Net List information.

Key to the DASH I is the schematic drawing editor. Its 16 simple keyboard commands allow entire drawings or just detailed portions to be created, modified, stored, and retrieved on the built-in floppy disk drive. Parts of the drawing can be moved and copied to eliminate tedious work, or they can be saved in a symbol parts library.

A starter library of standard discrete components (eg, transistors, diodes, zeners, capacitors, resistors, potentiometers, relays, LEDs, and inductors) is furnished with templates for popular TTL parts, microprocessors, and ROM and RAM chips. Users can also design

(continued on page 44)

(flek'sə-bil'ə-ti)



Defines The Heurikon HK68

For the systems integrator, power is flexibility . . . and flexibility is the Heurikon HK68!!!

Sporting an extremely well considered array of on-board features, the Heurikon HK68 presents itself as a single board one to eight user UNIX system!!!

Designed around the Motorola MC68000 microprocessor, the HK68 is compatible with the 24 bit Intel Multibus™ and includes quad channel

DMA controller, memory management unit, 128K or 256K bytes of dual access RAM with parity expandable to 1M byte on-card!!!, twin EPROM sockets providing a total capacity of 64K bytes, four RS-232-C ports with optional RS-422 on one port, winchester interface, streamer tape/printer interface, three 16 bit counter/timer channels, eight user definable LEDs and four dip switches, and two iSBX™ connectors for further expansion!!!

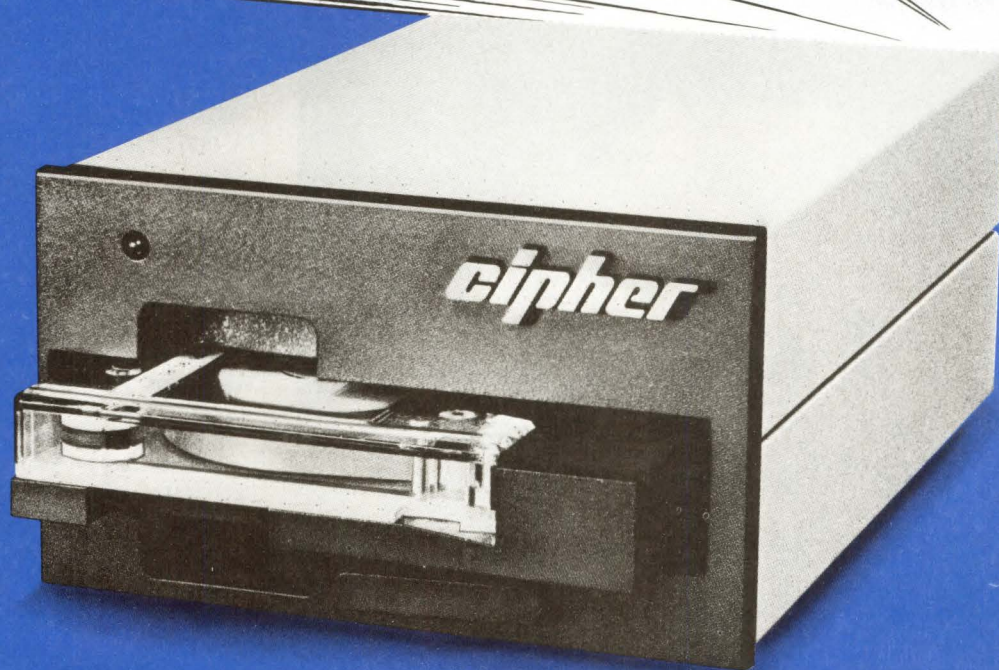

CeBIT Hall Booth 48

 heurikon corporation
3001 Latham Dr., Madison, WI 53713

Call Heurikon Direct 1 800 356-9602 In Wisconsin 1 608 271-8700

Multibus & iSBX are trademarks of Intel Corp.

CIPHER INTRODUCES THE 5 1/4" FORM FACTOR...



...a 1/4-inch
streaming cartridge
tape drive with
45 megabytes for
\$800.*

New, powerful, economical—and uniquely Cipher.
Choose Cipher for your 1/4-inch tape drives.
We've got a product that fits your needs.

- 45 MB capacity
- easy front loading
- O I C-02 interface standard
- 90 ips tape speed
- 5-1/4-inch form factor,
Model 540-CT
- 8-inch form factor,
Model 440-CT

cipher[®]
data products, inc.

10225 Willow Creek Road, San Diego, California 92131
P. O. Box 85170, San Diego, California 92138
Telephone: 619/578-9100, TWX: 910-335-1251

*O.E.M. Quantities

Automating layout (continued from page 42)

custom symbols to add to the library, as well as enter comments onto a drawing where required.

Components are displayed on screen within a 160- x 115-display unit work area, measuring approximately 5.5" x 8" (13.9 x 20 cm). These display units provide a device-independent definition of

graphic position where symbols, lines, and alphanumeric characters can occur. A digital mouse moves the cursor around the workspace to place symbols in the desired positions, as well as to draw the interconnects.

Instead of the designer learning a complex new language, he can use com-

mands like "\$138" to place a 74LS138 chip on the drawing. Status indicators, located to the right of the workspace, display such information as line types used in the drawing, as well as alphanumeric character size.

DASH I lets the user manipulate and view either the whole drawing compressed to the size of the screen, or a segment of the drawing at actual size. In the compressed mode, only the components and associated connections are displayed. Since the number of display elements remains constant between compressed and detailed modes, small details such as pin numbers and alphanumeric notations are omitted in the compressed mode. This information is viewed in the detailed mode within a rectangular area called a symbol cell. Printed copies of the schematic are available in five standard sizes: A (8½" x 11"), B (11" x 17"), C (17" x 22"), D (22" x 34"), and E (34" x 44").

By including detailed information (ie, part numbers and pinout configurations) with the interconnections and symbols, the central data base can be extracted and used as an input for a series of automated processes. A basic design checking program detects gross violations like missing interconnections, outputs without inputs, and improper pin loading. Separate packages allow the user to extract the L/M and automatically generate ECOS to eliminate errors encountered when these tasks are handled manually. Net List information provides the interconnection data for wirewrapping of breadboards, as well as input to automated PCB layout systems and logic simulators. Although the company does not provide a package to process the Net List information, it is confident that users can easily design interfaces for the available packages.

With an IBM Personal Computer, DASH I costs \$12,960. Also included are the Hawley model X063X Mouse (with three control buttons), a C.Itoh model 1550 printer (136- x 144-dot/in resolution), 256k bytes of RAM for system software, and 64k bytes of buffer storage (capable of holding two bit-mapped pages), monochromatic display, floppy disk controller, two 5¼" double-sided disk drives, mouse interface, and either MS-DOS or CPM/86 operating systems. Without the IBM PC and printer, DASH I costs \$5960. No hardware or software modification is required for existing PCs. **FutureNet, Inc.**, 21018 Osborne St, #5, Canoga Park, CA 91304.

Circle 244

From A Single Source



Magnetic Components To Your Specs.

When you need transformers, solenoids, coils, toroids or similar magnetic components, ECC has the experience, personnel and facilities to design, build and deliver your parts . . . on time.

Whatever techniques your magnetic components require:
HIGH SPEED WINDING • HAND WINDING • ASSEMBLY
MOLDING • POTTING • VACUUM IMPREGNATION

We are ready to put our facility to work for you.
For a complete capabilities brochure, call us at:



Endicott Coil Co., Inc.

24 Charlotte Street • P.O. Box 67 • Binghamton, NY 13905
607-797-1263

SEEQ'S 8001 ETHERNET CONTROLLER HAS EVERYONE TALKING.



Like their human counterparts, personal computers, copiers, and peripherals often need to exchange a few words among each other to get their work done. And now Seeq makes it practical and cost-effective for them to do just that. With the world's first Ethernet Data Link Controller (EDLC™), the Seeq 8001.

Practical because the 8001 doesn't dictate design criteria. You're free to choose the buffer management, memory management, and bus configurations that match your system's cost and performance.

Cost-effective because one 40-pin package contains all the logic to implement Ethernet's link layer. So you need very few support chips (21 for a PDP-11 and 18 for an

MC68000) to put popular mini- or micro-computers on speaking terms.

But there's more to the 8001 than just talk. Thanks to our structured VLSI design and CAD tools the 8001 is the first and only Ethernet controller available to meet your production needs now. And we'll use these design techniques to make die shrinks and cost reductions happen sooner, too.

So if your next product will be talking across an Ethernet network, contact Schweber Electronics or Seeq Technology, 1849 Fortune Drive, San Jose, California 95131. Telephone (408) 942-1990.

We'll make it easy for you to hold up your end of the conversation.

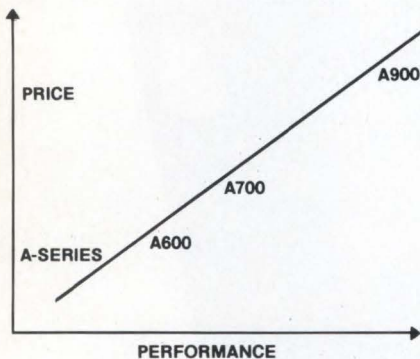
seeq

Ethernet is a trademark of Xerox Corporation. PDP-11 is a trademark of Digital Equipment Corporation. © 1982 Seeq Technology, Inc.

How do you make a 3 MIPS real-time computer for under \$15,000?

Simple. Hewlett-Packard's new HP 1000 A900 really makes things easy for OEMs with demanding industrial automation and process applications.

We made our computer exceptionally fast and rugged, as well as simple to use, expand and maintain. With state-of-the-art LSI technology, we were able to integrate the CPU and floating point hardware chips. We also included HP's Scientific Instruction Set and Vector Instruction Set firmware. Combined with a 4-kilobyte cache memory, two-level pipelined implementation and 3.7



If price/performance is important in your business, you can't do better than this.

megabytes per second I/O bandwidth, this made it comparatively simple to reach a CPU speed of 3 MIPS. As well as 560,000 floating point operations per second. All for an astonishingly low \$14,818.

Since we used only a quarter the number of components that are in our previous top-of-the-line computer, the A900 is even more reliable and simple to maintain. MTBF is a healthy 8000 hours; average repair time a scant 90 minutes.

You'll have an easy time expanding your system, too. You can start with our standard 3/4-megabyte board, and

move all the way up to 6 megabytes of 64K RAM error-correcting main memory. Without straining your budget. Because you can get this additional memory for just \$3340 per megabyte.

The Automators: a well-matched family.

In our HP 1000 A-Series family, you'll find two other members with the same level of price/performance as the new A900. For example, the A600 micro-computer gives you 1 MIPS minicomputer capabilities for only \$5K. The A700 minicomputer adds an easily customized microprogrammable processor. So, for just \$10K, you can tailor its power to handle data acquisition, process control and supervision of several dedicated processors.

All three computers come in a range of configurations, from \$2K micros to \$50K super-minicomputer systems. They all support identical peripherals, making it simple to expand or add power any time you want.

And we simplify planning your own system with a choice of nine graphics I/O devices, six CRT terminals, and a wide range of printers, disc drives and HP-IB compatible instruments.

A simple software story.

We made the software not just compatible but identical for the entire A-Series family. So you can interchange programs without any modifications at all. What could be simpler than that?

The family supports all major HP 1000 software packages, too. Including Graphics/1000 and IMAGE/1000 data base management. You can also use DS/1000-IV to network with the other HP 1000 or HP 3000 systems, as well

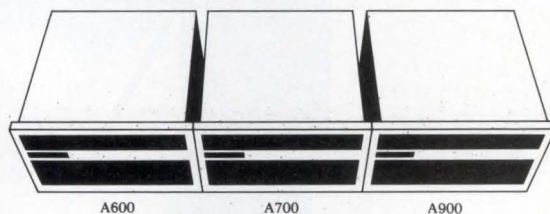
as X.25 packet-switching datacomm software.

All the Automators utilize the new RTE-A.1 real-time operating system. This supports programming in FORTRAN 77, Pascal, BASIC and Macro Assembly languages.

A new program for OEMs.

This is going to make things much simpler for you. It's a package of new discounts and credits that will help you sell more and keep more for yourself.

For instance, we'll give you a 10% credit for HP add-ons a customer orders for your system. And a 6% credit on the net price of a system for which you supply the software. To help your



The HP 1000 A-Series Automators provide a range of capabilities for real-time applications.

cash flow, we're offering 40% discounts on demonstration and development systems, too.

That's just for starters. Our new OEM program also involves competitive discounts, extended warranties, free training and much more.

So if you're looking for the best-performing real-time computers for the money—and a better-looking bottom line in the bargain—simply contact your nearest HP sales office. Ask a Technical Computer representative for complete details about the A-Series family and our new OEM plan. Or write to Joe Schoendorf, Hewlett-Packard, Dept. 11161, 11000 Wolfe Road, Cupertino, CA 95014.

Prices USA list, OEM quantities of 100



**HEWLETT
PACKARD**

LSI floating point
chips average 560K
floating point operations
per second.

Up to 6Mb
of memory,
with 64K RAMs
on 3/4 Mbyte
arrays.

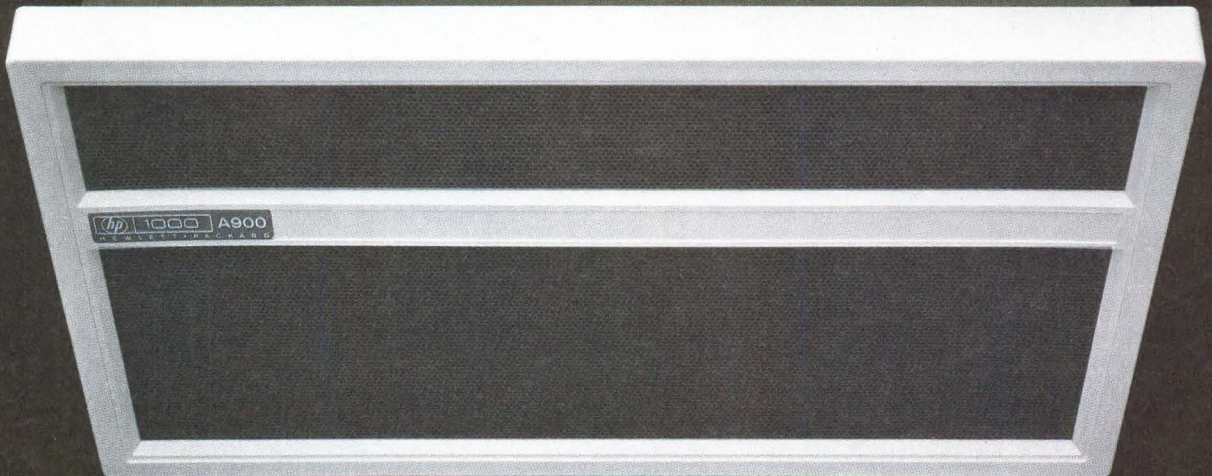
Pipeline
implementation
for 3 MIPS
performance.

Automatic
error-correcting
memory is
standard.

4 Kb cache
memory with 133 ns
response for fast
memory access.

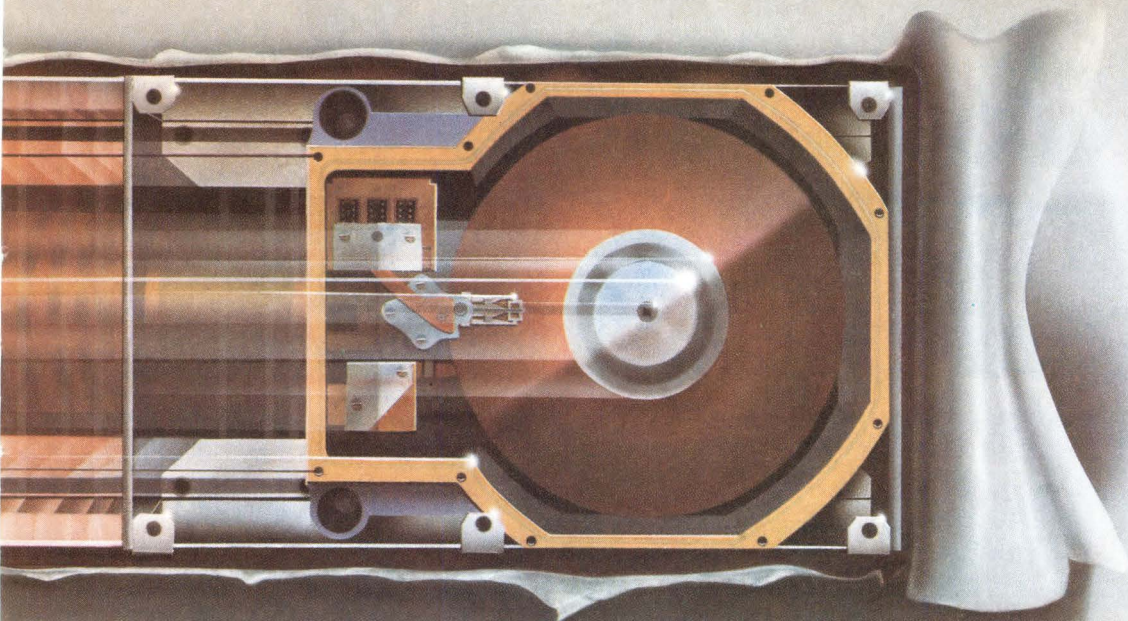
15 Kb of
extensive microcoded
self-test and program
accelerators.

Direct memory
access, supporting all I/O
channels with 3.7 Mb/sec
peak bandwidth.



PRIAM

**THE
DRIVING
FORCE IN
WINCHESTERS.**



In the world of Winchester's, only one company delivers the proven technology and breadth of line you need—PRIAM.

PRIAM Time. We've paid our dues by delivering thousands of Winchester disc drives. We've proven our technical superiority and high reliability in the field. We're the force to be reckoned with on the high-performance Winchester scene.

A growing family of winners. From the beginning in 1978, PRIAM has been the driving force in high-end Winchester technology. We've proven our technology in the 14-inch Winchester market with our 34, 68 and 158 Mbyte units. Our 8-inch drives have capacities of 35, 70 and 105 Mbytes in a floppy-sized package. And, we're adding a 50 Mbyte 5 1/4-inch drive to our growing family.

PRIAM Winchester Family.

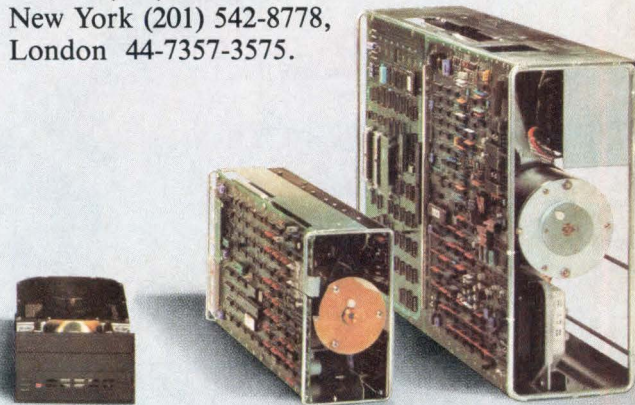
Size	Model	Capacity (MB)	Access Time
14"	3350	34	45 ms
	6650	68	45 ms
	15450	158	45 ms
8"	3450	35	42 ms
	7050	70	42 ms
	804	105	42 ms
5 1/4"	502	50	35 ms

SMART Interfaces. PRIAM gives you the finest in interfacing flexibility. Our intelligent interfaces can control up to four drives in any mix, plus tape or floppy backup. They're your fastest and easiest route to putting a Winchester database

in your system. Or, if you have an SMD or ANSI controller, our drives can be supplied with a matching interface.

We keep listening: We're driving upward to higher capacities, more compact packaging and enhanced performance with increased emphasis on quality and reliability. We believe our customers deserve high quality products. And we've committed the resources to meet that objective.

If you're thinking about Winchester's, think PRIAM. For more details, call (408) 946-4600 or the sales office nearest you. Los Angeles (714) 994-3593, Minneapolis (612) 854-3900, Boston (617) 444-5030, New York (201) 542-8778, London 44-7357-3575.



PRIAM

20 West Montague Expwy.
San Jose, CA 95134
(408) 946-4600
TWX 910-338-0293
FAX 408-946-5679

**NOBODY
PRICES DEC
MEMORIES
LIKE PLESSEY.**



But all you give up is cost.

Because while our DEC-compatible memories are typically 30% less expensive, they'll run up to 30% faster. Occupy less space. Are 100% burned-in and tested. Are run on the computers they were designed for before we ship them out the door. And come with an extensive 1-year warranty.

When you add in our OEM, GSA or educational discounts, you've got reliable high-density storage at a refreshingly low-density price. Check the chart for the memory you need, then check us out at (800) 992-8744.

We can also help your budgets and your systems with Plessey communications multiplexers. And with one of the broadest line of DEC-compatible disc controllers

in the world—for floppies, cartridges, disc packs, Winchester and magnetic tape, including a proven 1/4" streamer. (Complete subsystems with savings of up to 50%, too).

And we'll back you up with our own worldwide network of factory-trained specialists. They can service products from a variety of vendors and answer all your questions about configuration, operation or software. You get the responsiveness of an in-house technician at a fraction of the cost.

Nobody else even comes close.

For the rest of the story, contact:

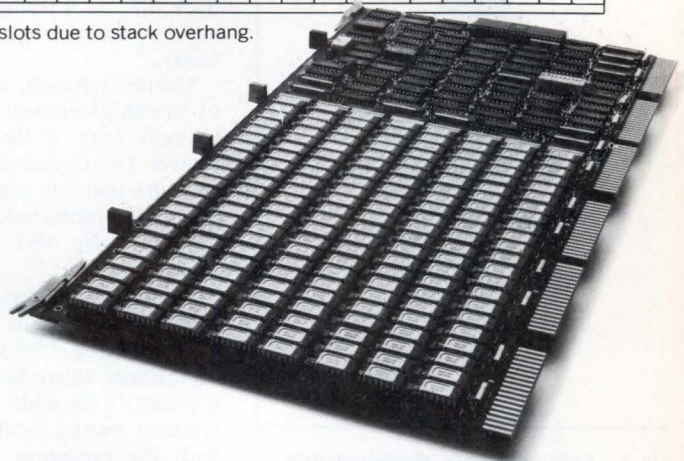
Plessey Peripheral Systems, Computer Products Division, 1674 McGaw Avenue, Irvine, CA 92714. Telephone (800) 992-8744 or (714) 540-9945.

PLESSEY'S DEC-COMPATIBLE MEMORIES

MODEL	TYPE	CPU										BUS		CAPACITY					PARITY		ECC	ADDRESSING		BOARD SIZE								
		LSI-11/2	LSI-11/23	LSI-11/23+	PDP-11/24	PDP-11/34	PDP-11/44	VAX-11/70	VAX-11/730	VAX-11/750	VAX-11/780	Q-BUS	UNIBUS	EXT. UNIBUS	MEM. BUS	32KB	64KB	128KB	256KB	512KB	768KB	1.0MB	On-Board Parity	Bits Only	Non-Parity	16-bit	18-bit	22-bit	Dual	Quad	Hex	
SV32AP	MOS	●	●											●	●							●	●									
SV128A	MOS	●	●											●	●	●	●					●	●			1						
SV512	MOS	●	●											●	●	●	●					●	●							1		
S11L/F	MOS			●	●	●								●	●	●	●					●	●								1	
S11E/4	MOS			●	●	●								●	●	●	●					●	●								1	
S750	MOS						●	●	●					●	●	●	●					●	●								1	
S780	MOS							●						●	●	●	●					●	●								1	
1132	CORE			●										●	●							●	●								1*	
1132A	CORE			●										●	●							●	●								1*	

*Memory is contained on a single board but requires space of two slots due to stack overhang.

✓ Check this one: about 1/3 the price of the DEC equivalent!



PLESSEY. ASK ANYBODY.

©Plessey Peripheral Systems 1983
DEC, LSI-11, PDP-11, VAX trademarks Digital Equipment Corp.

Politics and technology—a volatile mix for ferroelectric memory

Recent announcements regarding ferroelectric memory technology, a means of producing nonvolatile, high density, radiation-hard memory chips, are marred by controversy.

Principals in the ferroelectric drama include George Rohrer, developer and patent holder of fundamental ferroelectric techniques, and technical staff members of Sandia National Laboratories. It was Sandia that performed early evaluation tests on Rohrer's primitive ferroelectric devices in 1972. The fundamental question is, Why did this technology, which today holds the promise of being the computer memory panacea of the decade, failed to win acceptance when introduced in 1972?

As the political debate becomes more convoluted, the technology itself is becoming less puzzling. Curiously, the essence of it is not based in iron (ferro) compounds. Instead, the key to ferroelectric memory operation lies in the behavior of a chemical compound called 3-phase potassium nitrate (KNO_3). This substance exhibits a unique quality when under the influence of an electric field; a nitrate ion within a rhombohedral cell of potassium nitrate is physically displaced (Fig 1). The displaced NO_3 ion remains in one of two potential energy wells indefinitely after the electric field is removed

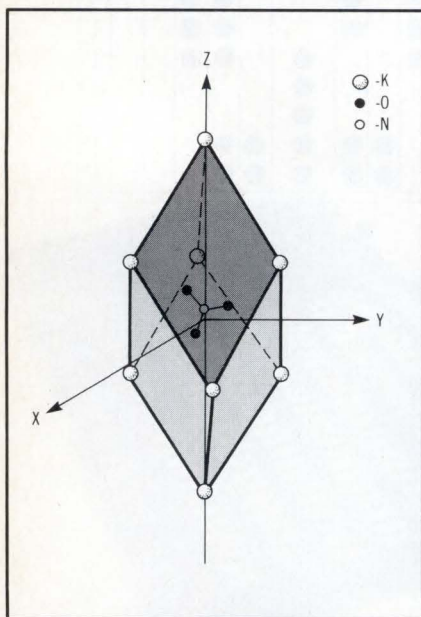


Fig 1 Polarized KNO_3 rhombohedral crystal is able to store digital information by altering its orientation. The physical position of nitrate ion within a lattice determines the logic state represented.

(Fig 2). By reversing the field, the nitrate ion's original position is restored. For computer memory applications, the net electric dipole moment induced in the field plates by this ionic shift represents two binary states. Since information storage occurs within a polarized crystal, the memory mechanism is robust and completely nonvolatile.

A memory cell can be constructed from KNO_3 by using a thin film of it as a dielectric layer between metal electrodes. A layer thickness of 0.01 to 0.10 microns is typical, with chip densities limited by the width of conductor electrodes rather than by KNO_3 related parameters. Existing production methods allow for conductor widths of one micron. At this scale, chip densities of 160M bit/in² are possible in 256k-bit packages.

By adjusting the thickness of the KNO_3 layer, switching voltages (cell output) can be controlled. Thus, memory cell compatibility with any logic level can be designed at the time of fabrication. Switching speeds on the order of 20 ns are typical and cycle times as speedy as 0.2 ns are theoretically possible.

George Rohrer explains his technology's initial setback in political terms: "After testing, they [Sandia Labs] wanted exclusive rights to my patent. I said no way...at least not without some money coming forward." Rohrer adds, "They then tried to put the strong arm of the government on me. At least that's my opinion of what was going on."

Rohrer claims that only the intervention of a phalanx of lawyers and congressmen on his behalf caused Sandia to back off. As a result, he concludes, "I am a *persona non grata* around Sandia today."

Charles Johnson, a long-time member of Sandia's technical staff, was involved in early tests of Rohrer's ferroelectric devices. He remembers things differently: "I think that you might say that Sandia was not impressed with George's devices...there were some definite reliability problems."

Johnson counters Rohrer's charge that Sandia tried to usurp ferroelectric patents saying, "I have never known of an instance where Sandia tried to usurp a patent." He adds, "Sandia is a government owned facility and all patents, with the exception of those that are classified, fall in the public domain. Anyone can use them." Rohrer, however, contends that this is not the case. "You must understand how Sandia is arranged," he insists. "It is not an arm of the government. It is owned by AT&T

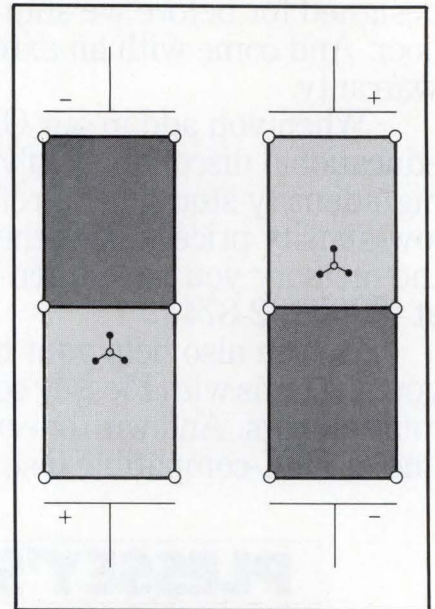


Fig 2 Nitrate ion occupies one of two energy wells within a KNO_3 lattice. When the ion is physically displaced by an externally applied electric field, a charge is induced on the memory cell field plates. The detected charge represents a binary state.

and funded by the government, on a reimbursable basis, to do research." The specter of AT&T involvement in Sandia is ominous for Rohrer.

In actuality, the structure of Sandia falls somewhere between these extremes; a distinction must be made between Sandia Corp and Sandia Labs. Sandia Labs was established in 1945 and operated by the University of California until 1949. The Bell system then assumed responsibility for operations, forming the Sandia Corp to oversee these details. Today, Sandia Corp is in fact a subsidiary of Western Electric and operates Sandia Labs on a no-profit, no-fee basis. According to a Sandia spokesperson, Western Electric influence is minimal.

Rohrer concedes that early ferroelectric efforts were hobbled by manufacturing problems. He maintains that today, this is not the case.

On paper, the ferroelectric memory fabrication process promises high yields at a paltry 0.001¢/bit cost. Additional benefits include high immunity to common mode and adjacent pulse noise (30 to 1). Also, the ferroelectric mechanism exhibits little sensitivity to particle radiation with a hardness of 10¹³ neutrons/cm² claimed. This quality

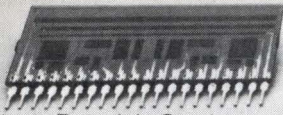
(continued on page 54)



Automotive
(Conformal Coated)



Porcelain Steel
(Pot Element)



Porcelain Steel
(Resistor Network)



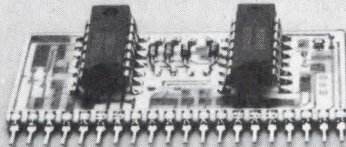
Thin Film SAW Devices (Filters)



Telecommunications Interface
(Using Small Outline
Components)



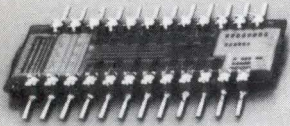
Commercial Circuit
(Using Surface Mount
Components)



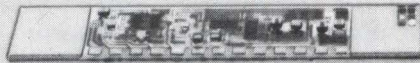
Telecommunications
(With PWB Components)



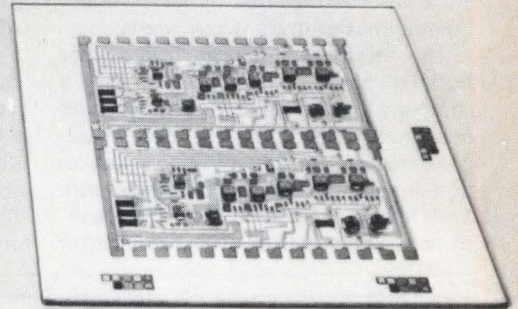
Precision Trimmable Resistor
(Ceramic DIP)



Porcelain Steel
(Multi-Layer)



High Speed Analog (Chip/Wire)



High Speed Digital
(Chip/Wire)

IF YOUR COMPUTER-BASED EQUIPMENT DEMANDS QUALITY, RELIABILITY, AND REDUCED SIZE, DEMAND THE ZENITH HYBRID ADVANTAGE.

The growing sophistication of computer-based equipment demands versatile, cost-efficient support technology vital to system performance and reliability.

And it demands consistent quality from prototype through high volume production requirements.

That means Zenith microelectronic capabilities.

Zenith hybrids offer countless advantages over printed wiring boards in space savings, and advantages over ICs in reduced development cost and rapid turnaround time.

Zenith microelectronic products can provide increased speed, lower access time, improved noise immunity and tight power regulation for applications such as ECL logic memories, printers, disc drives, modems and local area networks.

For more information on how Zenith can help

solve your OEM design problems just fill out and mail this coupon—or call direct at 312/391-7733.

Zenith CRT & Components Operations
1000 Milwaukee Avenue • Glenview, Illinois 60025

Please send me information about hybrids and other OEM components.

NAME _____

COMPANY _____

TITLE _____

ADDRESS _____

CITY _____ STATE _____ ZIP _____

TELEPHONE _____

CD-383



The quality goes in before the name goes on.®

Politics and technology
(continued from page 52)

alone makes ferroelectric devices attractive for military applications designed to function during nuclear Armageddon. Finally, high reliability and life expectancy (10^{10} read/write cycles) are claimed for modern ferroelectric devices.

The most attractive aspect of ferroelectric memories (aside from nonvolatility) is the potential ease with which they can be interfaced to existing logic families. In addition, symmetrical cell read/write times eliminate the need for special timing or control circuitry. Obviously, nonvolatility precludes the need for refresh circuits. Device power consumption at high output levels is not specified, but according to published literature is "on the order of microwatts." Standby power drain is zero watts.

The mechanism of the ferroelectric business plan is Technovation Inc, a company that George Rohrer presides over and formed 10 years ago. Headquartered in Necedah, Wisc, Technovation maintains a loose affiliation with Best Energy Systems, also of Necedah. Rohrer serves as Best's vice president of

engineering and Best's president, Terry Paul, acts as Technovation's business manager. Out of this amalgam, both men hope eventually to build a computer memory empire by licensing the technology that they have developed.

Technovation's business plan is ambitious, calling for the lease of a production facility in Colorado Springs by summer. Sample quantities of 1k-bit chips should be available by mid-1985. Larger 256k chips will be available by mid-1986, according to company spokespeople. In addition, a 10M-bit version of the memory, designed using cubic integration and 3-micron geometries, is planned for 1987. The \$10 million startup financing required is expected to be in place by April.

Given all these technological and entrepreneurial pluses, ferroelectric technology seems destined to succeed this time around. But, will it? George Rohrer is confident, yet philosophical, about his chances for success. "We were 10 years ahead of our time in 1972," he says. "We touted nonvolatility, density,

and radiation hardness before they were issues for most manufacturers." He sardonically adds, "With several companies we approached in those days, [Rockwell and Motorola] we also had to contend with the 'not invented here' syndrome." Now, in George Rohrer's view, his time has finally come. "This device is an absolute necessity today," says Rohrer, "because of the popularity explosion of small computers."

Terry Paul, Rohrer's business manager, is also optimistic. "We've been beseeged by inquiries from military contractors who want this device now," he claims. Paul adds, with a note of concern, that, despite its early setbacks, ferroelectric technology will soon be a reality—either here, or in Japan, where similar development is proceeding apace.

Whether or not the traditional cooperation—between government, industry, and the inventor—that drives Japan Inc will outrun citizen Rohrer in his quest for success remains to be seen. For the time being, George Rohrer is closer than he has ever been before. "You give me a company," he concludes, "and I'll give you a story." And, one assumes, a ferroelectric memory that works.

—Chris Brown, Technical Editor

Disk drive increases data transfers fourfold

Parallel read/write heads in the MegaVault MVP 132 rigid disk drive effectively boost the data transfer rate fourfold by creating four separate read/write channels that can be accessed simultaneously. Labeled a parallel random access memory (PRAM), the drive segments its eight read/write surfaces into upper and lower halves. This allows four read/write heads to be used at a time for a transfer rate of approximately 4.8M bytes/s. Typically, disk drives are limited to using one read/write head at a time, restricting data transfers to only 1.2M bytes/s.

The 8" PRAM drive is intended as a replacement for very large solid state memories in systems with high RAM requirements. For such applications as computer graphics, digital video, and image analysis, the drive offers 132M-byte unformatted storage, with a 40-ms average access time. A maximum of eight drives can be linked in a daisy chain to increase total capacity to over 1G byte.

(continued on page 59)

NEW Sealectro Mini Optical Reader

- Only 3.08" x 3.09" x 0.63" Actual Size
- No Moving Parts
- Self Cleaning
- Solid State Optics
- No Badge Counterfeits
- Available Now
- For Door Access Control, Time Clocks, Copier Control, Telephone Credit Calls... and much more



AS LOW AS
\$25
IN QUANTITIES



225 Hoyt St., Mamaroneck, N.Y. 10543
(914) 698-5600 TWX: 710-566-1110

INTELLIMAC

7000 M

NEW 32-BIT MULTI-USER COMPUTER SYSTEM WITH VAX* -like Speed + UNIX** + Ada***

The IN/7000M from INTELLIMAC is a state-of-the-art general purpose computer system. Based on the powerful MC68000 microprocessor, the 7000M supports multiple users and multi-tasking under UNIX Version 7 and/or the INTELLIMAC IN/MSX Multi-System Executive with TeleSoft Ada.

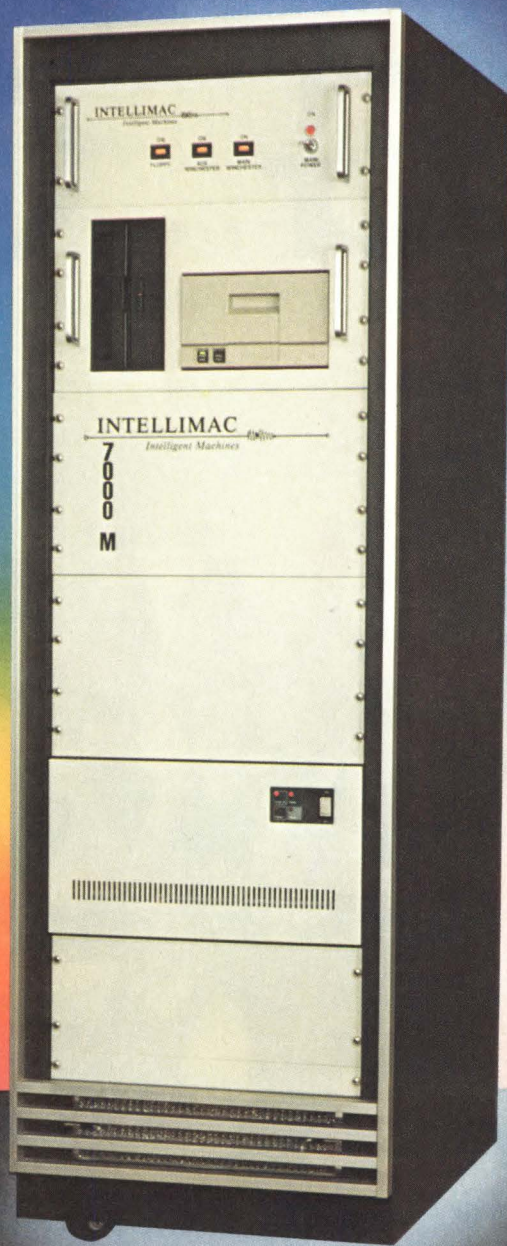
Standard Hardware Features:

- 8MHz single-board 68000 computer
- 21-slot Multibus**** chassis
- Multi-processor capable
- 256 KByte RAM (on CPU card)
- 1 MByte ECC RAM on Multibus (up to 8 MByte)
- Memory Management Unit (MMU)
- 8-line RS232C serial I/O
- 160 MByte Winchester Disk
- 8 MByte fixed plus 8 MByte removable cartridge disk
- 1.6 MByte 8" floppy
- 72" steel cabinet, rugged casters

Software Available:

- *Unix Version 7* ("C", FORTRAN 77, COBOL, Pascal, BASIC-Plus, Utilities)
- *IN/MSX Multi-User Ada* (TeleSoft-Ada and Pascal, 68000 Assembler, NASA Path Pascal, Ada Utilities, Applications)

Designed for high reliability, maintainability and availability (RMA), the 7000M's subsystems have very high MTBF's--many exceeding 15,000 hours. Program benchmarks indicate that the 7000M can perform at 50% to 150% of the speed of the DEC VAX 11/780, depending on operating system, language, and number of users.



INTELLIMAC

Intelligent Machines

FOR MORE INFORMATION, CALL OR WRITE:

INTELLIMAC, INC.—6001 Montrose Rd.

Rockville, Md. 20852 Ph: (301) 984-8000

• Twx: 710-828-9800 • Cable: INTELLIMAC

7000M Systems start at under **\$49,000.**

*Trademark of Digital Equipment Corp. **Trademark of Bell Laboratories ***Trademark of Department of Defense (A.J.P.O.) ****Trademark of INTEL Corp.



“G ODBYE

We joined the



PERTEC™

new leader in tape technology.

Hello PPC! The division that made Pertec Computer Corporation world famous for high tech peripherals is once again a separate, autonomous operating corporation—Pertec Peripherals Corporation.

It may seem like a small change, but it symbolizes the parent Triumph-Adler's commitment to PPC as an effective, independent organization free to pursue future generations in tape technology.

With worldwide sales and service capability and over 100,000 tape drives shipped, PPC is clearly the leader in tape technology and intends to stay that way. Its autonomy, and a doubling of product development dollars will provide its OEM customers with the best solutions and support possible for their future tape requirements.

PPC Introduces the VINDICATOR.™ PPC's engineers have designed this high performance 1/2-inch drawer mount streaming tape drive, providing 46 or 92 Mb capacity, to better meet OEM demands

for low cost, dependable tape transport. The VINDICATOR's high reliability design includes virtually all the features the OEM has been looking for:

auto-load, load-on-line, auto power restart, a diagnostic package with automatic self-test on powerup, a universal power module and a programmable front panel. And finally—extended gap start/stop performance and industry standard PPC formatter interface make the VINDICATOR the best choice for traditional and backup applications today, and for the requirements of the future.

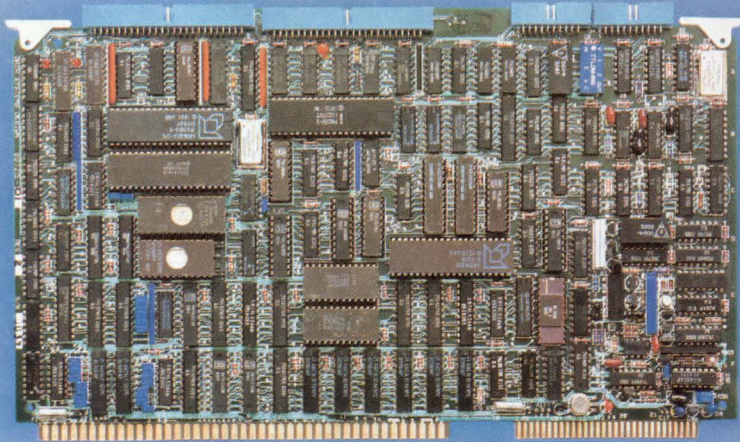
You too can join the new leader in tape technology. Call or write the "new" Pertec Peripherals Corporation, 9600 Irondale Avenue, P.O. Box 2198, Chatsworth, California 91311 or call (213) 882-0030, TWX: (910) 494-2093. In Europe and the United Kingdom, contact Pertec International, 10 Portman Road, Reading, Berkshire RG3 1DU Telephone (44) 734-591441.



SUBSIDIARY OF TRIUMPH-ADLER

Soaring to New Heights in Tape Technology

ONE SLOT SHOPPING.



INTRODUCING THE WINCHESTER/FLOPPY/TAPE THREE-IN-ONE MULTIBUS CONTROLLER.

Try this on for size.

DSD's new 7215 single-board Multibus® controller/interface handles two SA1000-type 40Mb Winchester, a 1/4" streamer, and two 8" floppies.

Plus on-board data separation, 32-bit ECC, and self-diagnostics. All on the same board.

There's also a version for 5 1/4" drives, the 5215, with similar capabilities.

And both are very, very quick.

Thanks to a pipelined architecture that moves data at non-interleaved speeds.

Top-of-the-line performance.

The 7215 and 5215 are the highest performance controllers on the market for 8" and 5 1/4" drives.

And that makes them ideal for multiuser and UNIX™ applications.

They also emulate Intel® iSBC® 215 and iSBX™ 218 controllers so you can run RMX 86 anytime.

And with 24-bit addressing support, you can take advantage of high performance microprocessors like the 68000 and the new inexpensive memory chips to address larger physical RAM memory.

To tune system performance, both boards offer four alternatives for bus arbitration. As well as having the capability to boost system performance by performing overlapped seeks and multisector operations.

Plus the convenience to match.

The best part about all this performance is that it comes on one board. So it only takes up one back-plane slot. And there are no extra boards to fool with.

As easy as that sounds, there are those of you who'd rather not do-it-yourself. For you, the 7215 controller is also available in our 770 storage systems.

And like all DSD products, our Multibus boards and systems are supported by our exclusive Rapid Module Exchange™ and regional service centers.

Shop around.

Compare our incomparable Multibus boards and systems to anything else you like. To make it easy, just send your business card to DSD Corporate Headquarters, Marketing Communications Department, for a free copy of "The Multibus Buyers Guide."

Corporate Headquarters: 2241 Lundy Avenue, San Jose, CA 95131. **Eastern Region Sales and Service:** Norwood, MA, (617) 769-7620. **Central Region Sales and Service:** Dallas, TX, (214) 980-4884. **Western Region Sales:** Santa Clara, CA, (408) 727-3163. **International Sales:** San Jose, CA, (408) 946-5800.

*Intel, Multibus, and iSBC are registered trademarks of Intel Corporation.™ iSBX is a trademark of Intel Corporation.

™UNIX is a trademark of Bell Laboratories.

™Rapid Module Exchange is a trademark of Data Systems Design, Inc.

DATA SYSTEMS DESIGN

Boosting data transfers

(continued from page 54)

Using multiple parallel heads differs from the common practice of placing multiple fixed heads on a single arm to read a single surface. Although the latter technique reduces track to track access and latency times, the company notes that channel to channel crosstalk and asynchronous noise degrade the data transfers when simultaneous accesses are attempted. Problems with increased channel to channel crosstalk preclude the simultaneous use of adjacent heads mounted on the same arm in the PRAM drive (see the Figure).

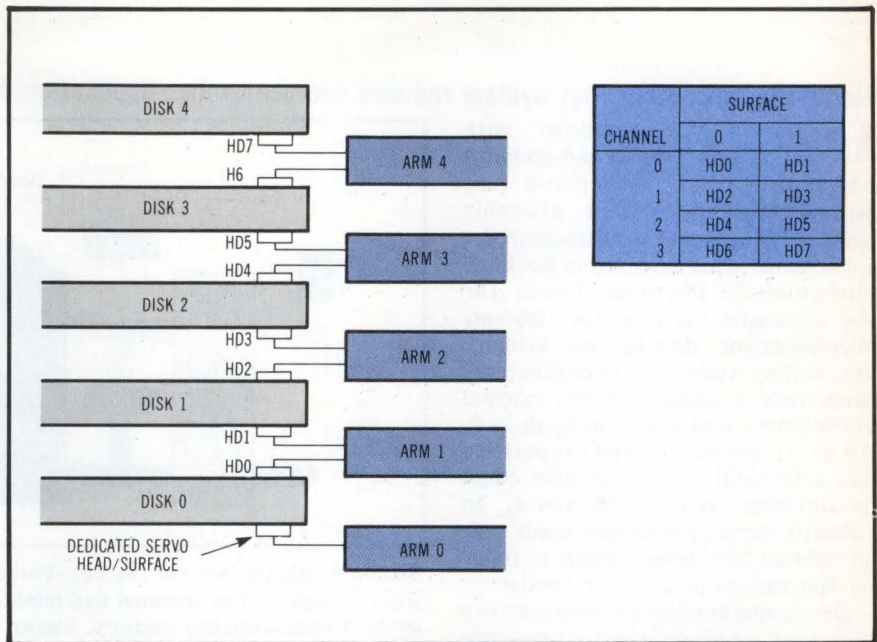
A single voice-coil positioner limits data transfers to the same track on all four surfaces. Simultaneous access to different tracks on each surface would either require multiple positioners or multiple heads per arm, according to the company. Typical access time between the drive's 823 tracks is 5 ms, with a full stroke move specified at 70 ms.

Although the company offers standard SMD and ANSI interfaces for the drive, the user needs to design a custom disk controller to take full advantage of the independent read/write channels. The company provides only the sealed head/disk assembly and an electronic module that consists of the power amplifier, servo tach, microprocessor control, and four sets of read/write assemblies. Each read/write head also has its own amplifier to reduce noise.

Necessary functions that the custom controller must handle include selection of the upper or lower surfaces to transfer data, breakdown of the data stream to pass to the individual channels, error detection and correction, and memory buffering to optimize throughput. If multiple drives are to be linked, the controller also has to synchronize the drives so that one drive can perform a read/write operation while another is seeking. This reduces latency times as well as increases throughput.

Controller design can be eased if the parallel read/write channels are treated as separate disk drives, according to the company. Apart from the selection of the upper or lower read/write surface, off the shelf controllers available for both the SMD and ANSI interfaces can serve as a basis for the custom controller. Off the shelf controllers already perform most of the needed functions.

The MVP 132 disk drive unit measures 7.1" x 17.5" x 14.75" (18.0 x 44.5 x 37.5 cm) and costs \$6500 in OEM quantities, with units shipped 60 days ARO. **MegaVault, an SLI Co, 6431 Independence Ave, Woodland Hills, CA 91367. Circle 245**



A user can transfer data to any four of eight surfaces on the MegaVault MVP 132 disk drive. This is accomplished by specifying either the upper or lower surface and the desired read/write channel.

WINCHESTER DISK CONTROL WITH MAG TAPE BACK-UP

On a Single Multibus* Board

- ALL ANSI/PRIAM 8 & 14 INCH WINCHESTER DISKS
- INDUSTRY STD. 1/2-INCH TAPE
- 1/4-INCH TAPE CARTRIDGES
- START-STOP OR STREAMING DRIVES

Our RIMFIRE controllers are full Bus Masters with a variety of options that make it easy to design them into any Multibus system. Their simple Parameter Block Interface offers numerous programming options such as Bus Lock, ECC and Retry Disable, Linked Commands and Mailbox Interrupts.

CALL OR WRITE FOR COMPLETE INFORMATION



2405 Annapolis Lane
Plymouth, MN 55441
Phone (612) 559-2034

*Multibus is a trademark of Intel Corporation

© 1982 Computer Products Corporation

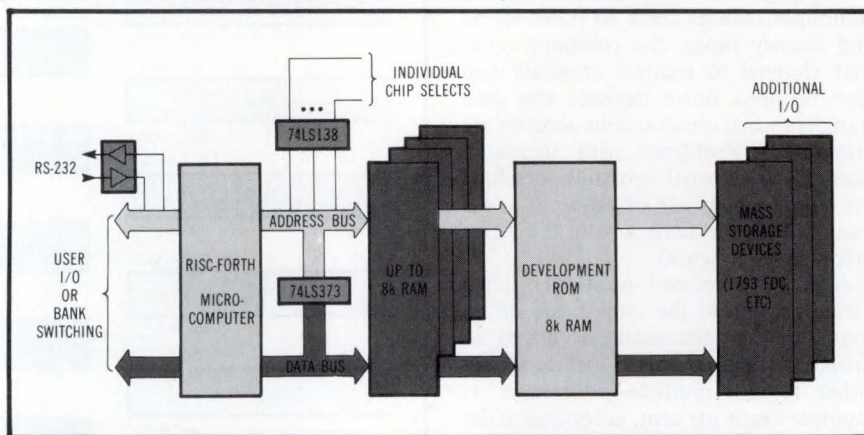
Single-chip microcomputer system reduces microcontroller application development time

A single-chip microcomputer with onboard Forth compiler and operating system reduces the development time associated with writing assembly language programs for microcontroller applications. This system from Rockwell International's Electronic Device Div also eliminates the need for elaborate microprocessor development systems. For writing code, the microcomputer needs only a single reusable, external development ROM and scratchpad RAM. An RS-232 compatible serial I/O port can link a terminal to the minimum count development system. Moreover, an onboard PROM programmer needs only an external 25-V power supply to transfer applications programs to EPROM.

Developing applications programs in a high level language lowers costs—code can be written and debugged in about one-third the time of an equivalent assembly language program (the most common language for writing controller programs). Forth was selected because it allows programmers to create machine-dependent I/O structures, as well as permits direct memory references.

Microcontrollers generally do not have access to such I/O devices as disk drives, video display terminals, and line printers that languages such as FORTRAN or BASIC typically require. Also, special purpose devices like timers and edge-sensitive lines, common in controller applications, are memory mapped devices. Languages developed primarily for multitask/multi-user systems usually prohibit any user from directly addressing system resources, such as memory. Forth supports memory references with commands like "fetch" @ and "store" ! that can read or write into any memory location.

Using Forth's interpretive quality, the user can test and run code without creating and assembling source code. The R65F11 and R65F12 host processors act as both development and target systems. Both processors contain the Forth interpreter and a runtime bootstrap routine in ROM code that develops applications programs in external RAM. Once perfected, the program can be preserved in ROM or EPROM as the code to be used in the same system for a dedicated control process. Similar configurations have also been implemented to support Forth on the RCA 1804 microcomputer and Tiny BASIC on the National INS8073 micro-computer.



System configurations for the RISC-Forth chip set allow a range of capabilities from a single-system terminal and minimal memory to floppy disk drives and 16k bytes of bank-switched memory. Shown here is a maximum configuration. EPROM programming is also available.

Both the R65F11 and R65F12 are based on the 6502 microprocessor and contain 3k bytes of mask programmed ROM and 192 bytes of RAM. Both have a 16k-byte external memory addressing capability. However, the number of available I/O lines differs—the R65F11 provides 16 lines; the R65F12 40 lines. The internal ROM is preprogrammed with all runtime words contained in Forth. About one-third are devoted to machine language primitives and the remainder are Forth words defined with these primitives.

Over 120 Forth functions are included in the kernel; the bootstrap program ("cold") initializes the part and looks for external applications programs to execute. One such program is the external development ROM. This contains all the dictionary definitions and compile-time only words a user needs to enter commands and create applications programs. The kernel in the microcomputer and the development ROM then combine to form a complete Forth operating system.

A serial port on the microcomputer (capable of fully buffered, duplex, asynchronous communications at baud rates up to 62k bps) is used to connect a system terminal to the 3-chip system. After program development is completed, the debugged code is then transferred from RAM to EPROM. Then the development ROM is removed so that the applications program can be set up similar to the development ROM.

Auto-start occurs when the system word "cold" is executed upon reset.

Cold initializes the microcomputer's internal registers, establishes the 16k-byte external memory map, and sets up the serial channel for 1200-bps asynchronous transmission. Essential Forth variables are then downloaded to zero-page RAM and the system RAM is set at memory location 300 Hex and up.

After initializing the part, cold searches the external memory map in 1k-byte segments. The first two bytes are read and compared to a 5A and A5 Hex pattern. When found, the following two bytes are used as a pointer to the high level Forth routine to be executed. An appropriate machine-coded interpreter will then be called, based on the address of the desired word's code field. If this pointer is directed at the fifth and sixth bytes, these, in turn, point to an assembly language program.

Thus, the system can execute any dedicated applications program written in either RISC-Forth (a version of Fig-Forth with extensions) or assembly language, as well as enter a preprogrammed ROM. Cold checks for an auto-start ROM, beginning at address 400 Hex. Applications programs are created starting with that same address. In this way, programs developed in RAM can be copied into EPROM and then replaced with a permanent copy. Higher starting addresses can also be accommodated at the user's discretion.

If neither an applications program nor a development ROM is found in the memory map, cold then turns over execution

(continued on page 62)

THE BUS STOCKS HERE:

PSM-512A: 512 kbyte Multibus™ memory with ECC, 275 nsec access time. Fixes single-bit errors, flags multi-bit errors.

CIRCLE 41

PSM-512P: 512 kbyte Multibus parity memory, 240 nsec access time. Very economical.

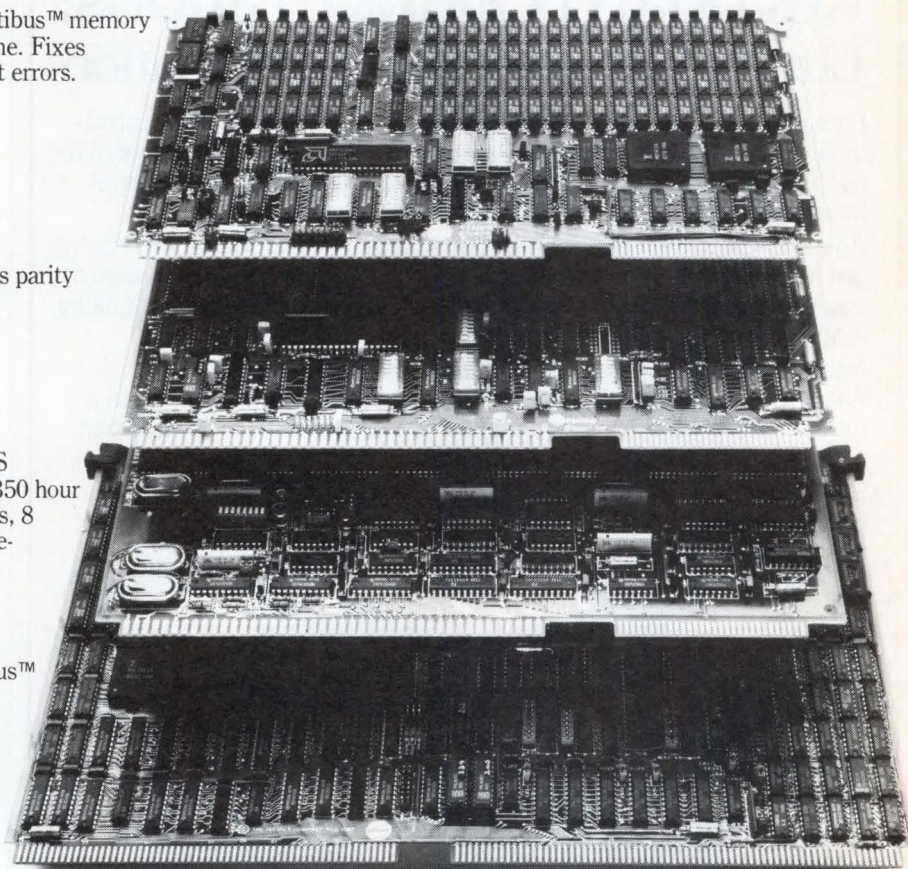
CIRCLE 42

PSM6463: 64 kbyte non-volatile CMOS Multibus memory, 200 nsec access time. 350 hour standby with on-board rechargeable NiCd's, 8 years with lithium. For process control, telecommunications, other critical applications.

CIRCLE 43

NEW PSM1VA: 1 megabyte VERSAbus™ memory with ECC, 300 nsec access time. Lots faster and much less expensive than Motorola and IBM equivalents. Full 32-bit VERSAbus compatibility.

CIRCLE 44



If you're on board the Multibus or VERSAbus, we've got the memories you need to get where you're going faster, for less. ECC, parity and non-volatile CMOS. All in stock now, all with one thing in common. Their first name is Plessey.

And since Plessey makes them all, they all have high reliability, a one year warranty and Plessey support worldwide.

For more information, just contact Plessey

Microsystems, 451 Hungerford Drive, Rockville, MD 20850. (301) 279-2892, TWX 710-828-9815. Irvine, CA: (714) 540-9931.

In Europe, contact: Towcester, UK: (0327)50312, Telex 31628. Paris: 776 41 06. Noordwijk: (01719) 19207. Munich: (089)2362226. Rome: (06) 350189.

Or get on board fast by calling (800) 368-2738 today. Your bus ought to be going our way.

 **PLESSEY**

Multibus is a trademark of Intel
VERSAbus is a trademark of Motorola

Reducing development time
(continued from page 60)

to an internal, high level Forth word that sends the message "no ROM" to the system terminal. It also attempts to boot a program from an RM65 floppy disk controller at memory location 100 Hex.

A target compiler can be used to produce standalone code, with only the needed portions of the kernel retained, if

a user needs to program many applications programs within the 3k-byte memory. After a program is written and tested with all the high level constructs available in Forth, "object code" modules are created with the compiler. These modules are suitable for submission as ROM codes for production runs without

fear of compiler translation errors. The RISC-System target compiler runs on an AIM 65/40 system with disk capabilities.

Prices for the RISC-Forth development system are \$17.85 for the R65F11, \$23.35 for the R65F12 in quantities up to 24, and \$45.70 for the single R65FR1 development ROM. Quantity discounts are available. Price for the target compiler is available upon request. **Rockwell International, Electronic Device Div, 4311 Jamboree Rd, Newport Beach, CA 92660.**

—Joseph Aseo, Field Editor

Circle 246

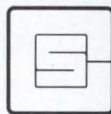
Keyboard Configurations: Limited Only by Your Imagination

Free yourself from the design limitation of standard keyboard products. Now Cal Switch can give you the keyboard of your dreams. We use Hi-Tek Dovetail Switch technology to create custom full-travel keyboards without custom tooling or extensive lead times.

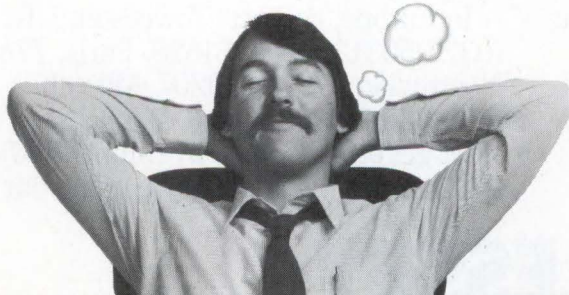
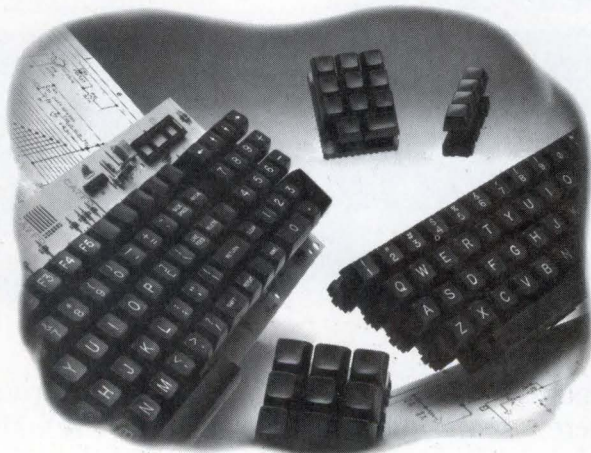
Add a single switch or a whole row. A separate control panel? You've got it! Off-the-shelf or off-the-wall . . . we can give you the keyboard you've always wanted. And with Hi-Tek switches you get high quality, long-life keyboards you can rely on.

Need more help? We can design and manufacture your PCB. Assemble to your specifications and test. From a single switch to a fully-encoded board — in quantities of 5 or 5,000 — Cal Switch can give you the keyboard of your dreams.

Experience design freedom!
Call or write Cal Switch today
for more information on
Hi-Tek Dovetail keyboards.



CAL SWITCH
13717 S. Normandie
Gardena, CA 90249
Toll free: 1-800-421-2471
(213) 770-2330 (714) 522-8600



DATA COMMUNICATIONS

Intelligent network component manages ultrawide bandwidth digital data links

Link/1 breaks T-1 facilities into as many as 200 standard speed channels under dynamic online centralized network control. It reduces the need for multiple networks by mixing data over digital links that operate at up to 2M bps.

As stated by Timeplex president Ed Botwinick, "the relatively low cost of the T-1 links now becoming available from the phone companies and other carriers will be one of the key factors that make office automation and the office of the future really possible." Until about two years ago, T-1 facilities were available only for internal use within the telephone system. Today, however, leased line T-1 service is available to subscribers. Digital transmission links running at 1.544M bps, T-1 facilities provide the equivalent of 24 voice grade lines.

The ability to mix information allows users currently operating separate data and voice networks as well as others for fax dial-up lines and video facilities to cut costs. In addition to reducing the need for multiple networks and thus saving in transmission costs, it extends the range of possible applications to include high speed computer to computer file transfers that were previously impossible over bandwidth channels.

To use T-1 facilities effectively, the Link/1 combines time division multiplexing, integral T-1 modems, programmable network configuration and port assignments, and dynamic bandwidth contention capabilities. With this, it provides the ability to mix synchronous,

(continued on page 65)

Penril's 4800 and 9600 Modems Are Out Front in Features, Not Price

Penril's new V.27 and V.29 compatible high speed modems use microprocessor control to give you a full set of no-compromise features at low cost.

FRONT PANEL CONTROLS

The 2127 (V.27) and 2129 (V.29) display their operating characteristics on the front panel. And five front panel switches let you change those operating characteristics or set up tests in seconds without internal strapping.

DIAL-LINE BACKUP AT 4800 BPS

The 4800 bps version provides the added security and convenience of two call direct connect dial backup. If data quality drops, the 2127 can make a backup connection on CCITT or Bell dial-up lines. An optional autodial feature eliminates the need for manual dialing and telephone sets.

DATA MONITORING

The 2127 and 2129 continuously monitor data quality with an audible alarm so you can respond instantly to signal degradation.

AUTOMATIC NETWORK TEST

The 2127 and 2129 implement V.54 (loops 2, 3 and 4) test loops. The 2127 and 2129 contain an integral V.52 test pattern generator and bit error rate detector. So you can perform a complete network Bit Error Rate Test without external equipment or a remote operator. Best of all, Penril's modems automatically test (ALB, remote LLB and remote DLB) point to point configurations and sequence through each modem in a multi-drop network with a pass or fail indication for each modem.

DIAGNOSTIC CONTROL

Optional side channel diagnostics provide network control functions without interrupting normal data flow. Alternately, a V.23 compatible side channel option is available.

COMPATIBILITY

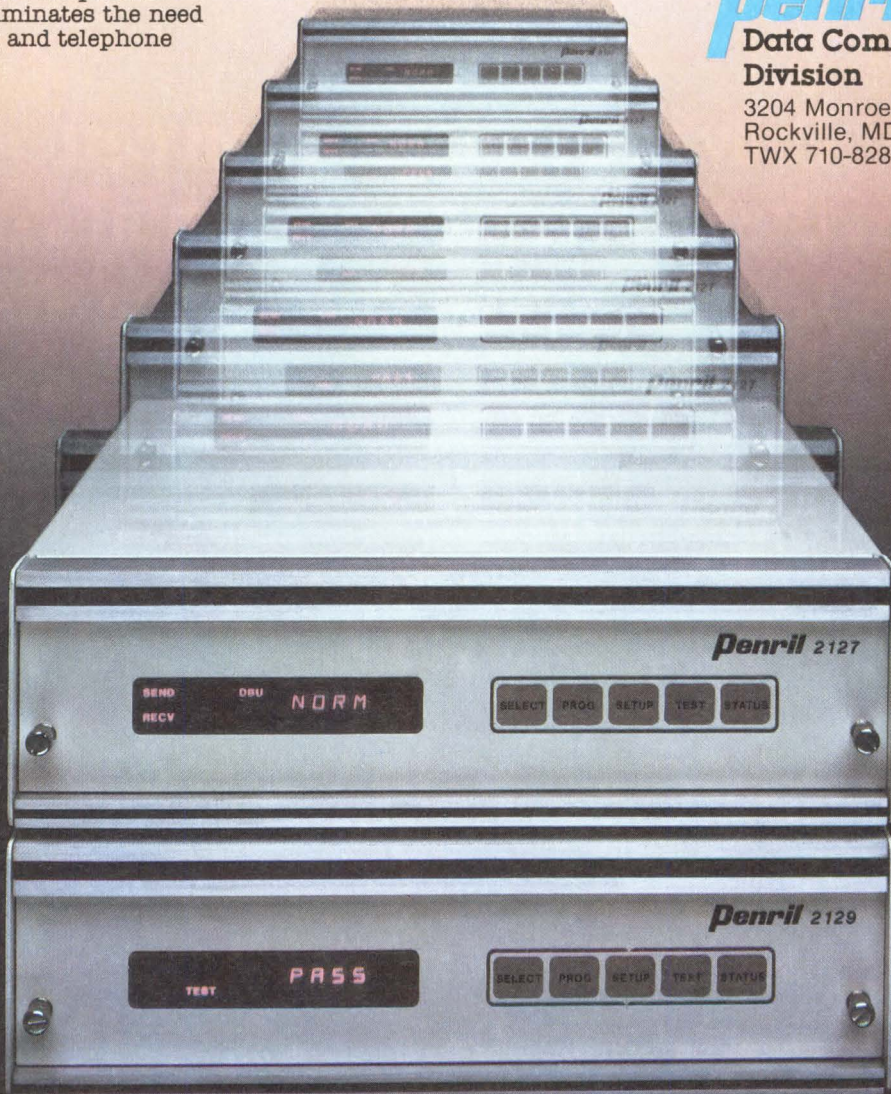
The 2127 and 2129 utilize automatic adaptive equalization to accommodate your Bell or CCITT networks. They are strappable for International power sources. And the user may choose an optional interface compatible with MIL STD 188C or RS-449.

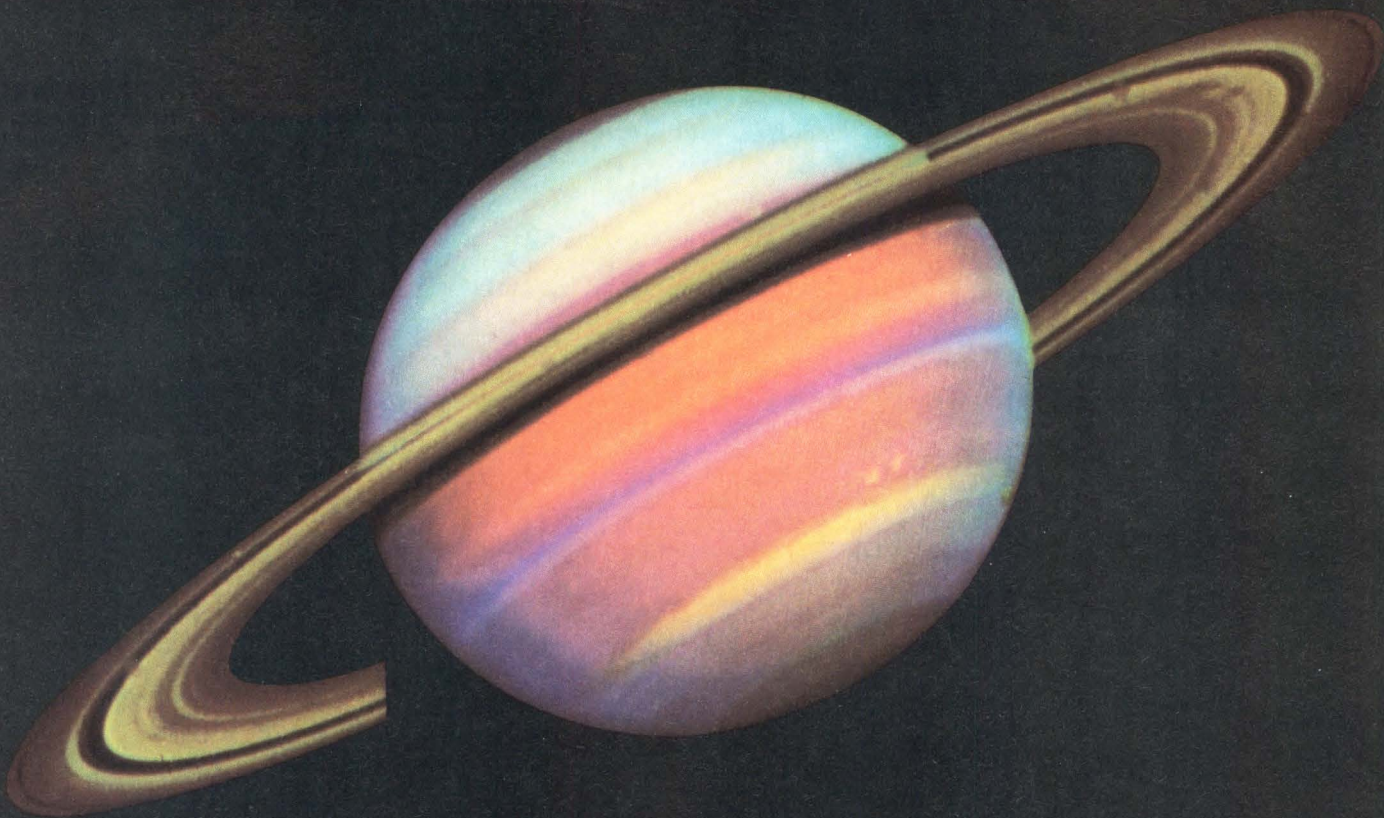
Check out the new pair of performers from Penril. Talk to one of our Applications Engineers today.

CALL TOLL FREE 800-638-8905.
IN MARYLAND DIAL 301-984-8225.

Penril
Data Communications
Division

3204 Monroe Street
Rockville, MD 20852-4297
TWX 710-828-0522





Only your imagination can limit the application of Comtal's new Vision Ten/24 Image Processing System.

Whether you're exploring the outer regions of space or exploring for oil in some remote area of the world, Comtal's new Vision Ten/24 is the only digital image processing system that processes and displays 1024 x 1024 high resolution images with a clarity never experienced before in image processing. It's a powerful tool for interpreting and analyzing images for such diverse applications as LANDSAT, meteorology, seismology, graphic arts, earth resource management, medical imagery, or something only you know about.

Four times the resolution at 30% lower cost.

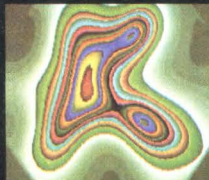
The Vision Ten/24 is the only image processing system capable of processing and displaying images at a 1024 x 1024 resolution in real time (1/30 second) with a 40 MHz video output rate. That's four times the resolution of the industry-standard 512 x 512 systems. With it, whole new worlds open up. Inter-



pretation and analysis become more precise. Best of all, the basic Vision Ten/24 system price is 30 percent less than our previous 1024 x 1024 system because of our design and manufacturing refinements. Giving you incomparable price/performance.

Building block flexibility.

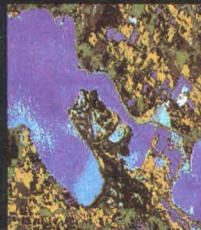
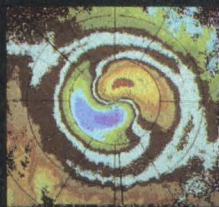
Our modular design approach with the architecture of the Vision Ten/24 gives you flexibility along with easier system upgrades. You can increase video paths, memory size or processing power by simply adding modules. Making the Vision Ten/24 able to keep pace with your image processing requirements. In addition, the system can operate as a standalone image processor or can be interfaced to a variety of host computers.



Comtal—a generation ahead in image processing.

Our new Vision Ten/24 is a generation ahead of any other digital image processing system. It's not surprising since our systems have consistently been the state-of-the-art in image processing. For example, our 512 x 512 systems offer more exclusive features and options, and give you more standard models to choose from, than anyone else. With a decade of experience in image processing and more than 600 systems installed worldwide, only Comtal gives you the leading edge of image processing technology.

Put your imagination to work and give Comtal a call today for a firsthand look at our new Vision Ten/24. Comtal, a subsidiary of 3M, 505 West Woodbury Road, Altadena, California 91001, (213) 797-1175



COMTAL

3M

CIRCLE 47

SYSTEM TECHNOLOGY/ DATA COMMUNICATIONS

Digital data links

(continued from page 62)

asynchronous, and isochronous digital information streams over a single data link.

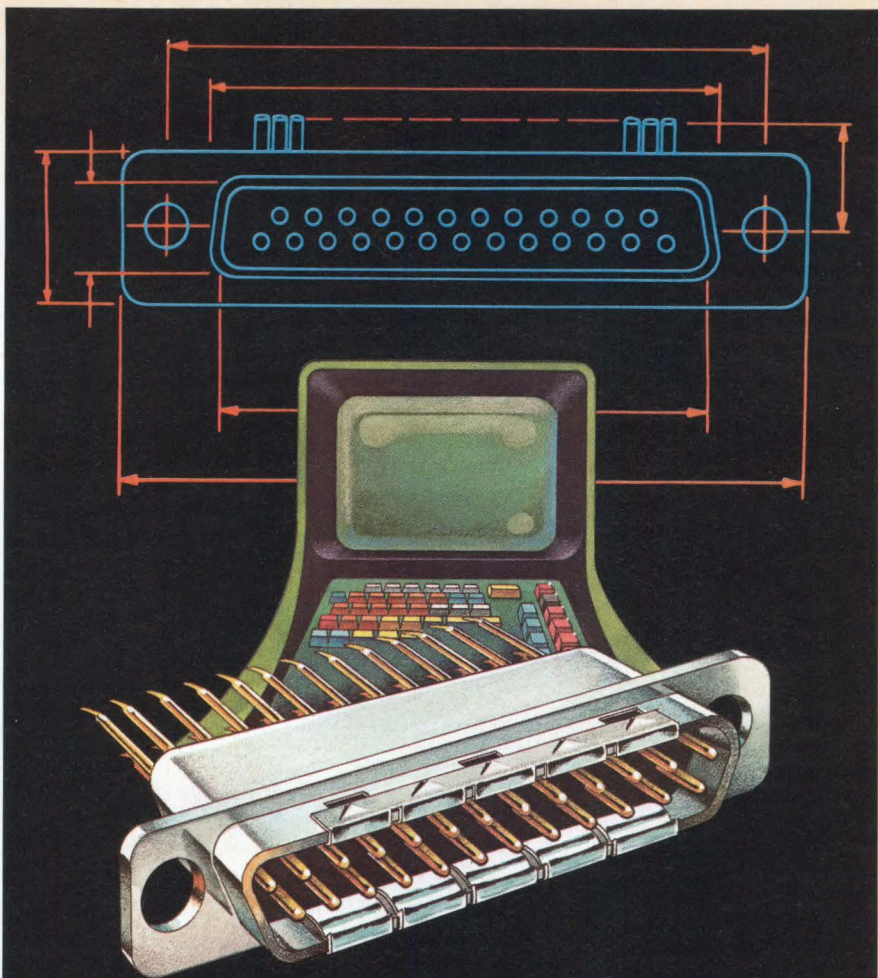
Voice connections are provided through a digital voice module. This module converts analog voice signals to a 32,000-bps data stream. This stream is multiplexed with other information on the T-1 link. The same module converts digital signals back to analog form. Achieved through the use of a sophisticated sampling technique and coding algorithm, the 32,000-bps rate is half the industry standard. The remaining bandwidth can be used for nonvoice applications.

To handle the facilities, a microprocessor has been dedicated to network management. This unit supplies three levels of processor controlled reconfiguration—dynamic, periodic, and manual. The microprocessor within the network manager can be user programmed to allocate available bandwidth on the data link to specific ports, types of applications, or particular end users on the basis of priority ratings. Allocation occurs dynamically, dropping lower priority channels in favor of higher priority ones.

An interactive supervisory port permits management and diagnostics to be done from a central site. All management and diagnostic functions are controlled from either an ASCII terminal on the port or by a computer connected to a special interface port. Diagnostic capabilities pinpoint problems using progressive isolation. This combats the increased finger pointing to be expected when using mixed vendor networks.

Since the unit assumes so much communications responsibility, fault tolerance has been designed in. Every major component that affects more than one I/O module can be backed up by a redundant unit. For example, dual independent power supplies share the load under normal conditions; either can assume the full load if the other fails. Similarly, common control logic, network manager, data link controller, and T-1 drives can have redundant online backups. Since port modules are designed to fail safe, only those ports routed through the module are interrupted; no other ports are affected.

Cost of the equipment ranges from about \$8000 for a minimum useful configuration to over \$70,000 for high end systems. Deliveries are scheduled for second quarter 1983. **Timeplex, Inc.**, One Communications Plaza, Rochelle Park, NJ 07662. **Circle 247**



When the FCC says control your interference

use Spectrum's shielded-filtered connector*.

Spectrum Control's low cost filtered and shielded D subminiature connectors are effective ways to make your computers comply with the FCC's Electromagnetic Interference (EMI) regulations.**

Spectrum Control's new filtered and shielded D Subminiature connectors provide maximum versatility and compatibility while eliminating any EMI problems. And they're far less expensive than you might think.

Spectrum connectors feature a complete range of performance options, and they're totally adaptable for easy retrofitting. The design is based on proprietary ceramic technology

of proven reliability and performance, and features programmable filter positions for unlimited versatility.

Spectrum Control itself, offers you a full range of electromagnetic compatibility services and products for both custom and standard applications. For more information call, or write for Engineering Bulletin 27-0027-53. Write Spectrum Control, Inc., 2185 W. Eighth Street, Erie, PA 16505. Or call 814/455-0966, TWX 510/699-6871. Spectrum's filtered connectors could be the low cost solution you're looking for.

*Patent Pending

**FCC Part 15 Sub Part J VDE and Mil STD 461 A/B



SPECTRUM CONTROL INC.

Making technology compatible with technology.

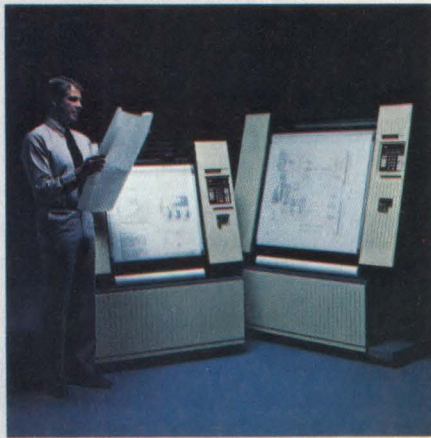


CalComp's \$16,000 vs. their \$16,000

Why settle for a plodding plotter when you can double your throughput with an all-new Model 945 or Model 965 beltbed plotter from CalComp for approximately the same price?

Productivity gains can range from 25% to more than 500%. It's like having up to two plotters for the price of one.

CalComp Model 945 beltbed plotter (left) for sheets up to ANSI size D (or ISO size A1), and Model 965 plotter for drawings up to sheet size E (or size A0).



What's the difference? The basic philosophy behind each plotter design. Their plotters trade off speed for one-time economies of smaller size, lighter weight, less powerful components. *You* pay the price in plotting time with each pen and paper movement (their 24-ips maximum vs. CalComp's 42-ips) and each excursion of the single-pen carriage to a side-mounted carousel.

CalComp's Model 945 and Model 965 plotters, by comparison, allow you to map up to 16 logical pens to four physical pens continuously poised over the plot surface—ready to be activated



6,000 plotter 00 plodder.



in a fraction of a second. If more than four pens are needed, the plotter performs an automatic stop and prompts the operator to change pens.

Plus the user-friendly control panel provides local control and plot manipulation with easily understood English language messages.

The same interactive firmware gives the operator complete control

over plot parameters. Training time is all but eliminated.

Your CalComp Model 945 or Model 965 plotter starts delivering high-speed plots the day it is installed, without changing a line of industry-standard software. Industry-standard because it was developed by CalComp—world leader in computer graphics and CAD/CAM.

So write or phone today for your illustrated copy of "The Plotter and the



Plodder." Compare the performance specifications. Then make your own move into the fast track of plotter technology—with CalComp. California

Computer Products, Inc., 2411 West La Palma Avenue, Anaheim, CA 92801.
714-821-2011 TWX: 910-951-1154

CALCOMP
A Sanders Graphics Company



SANDERS

DON'T A DRIV A STR

We're the world's leading manufacturer of micro peripheral disk drives. Which means that, whenever

TAKE E FROM ANGER.

You need a reliable 5¼" floppy, 5¼" Winchester or 8" ThinLine™ floppy, we're the supplier you can rely on.

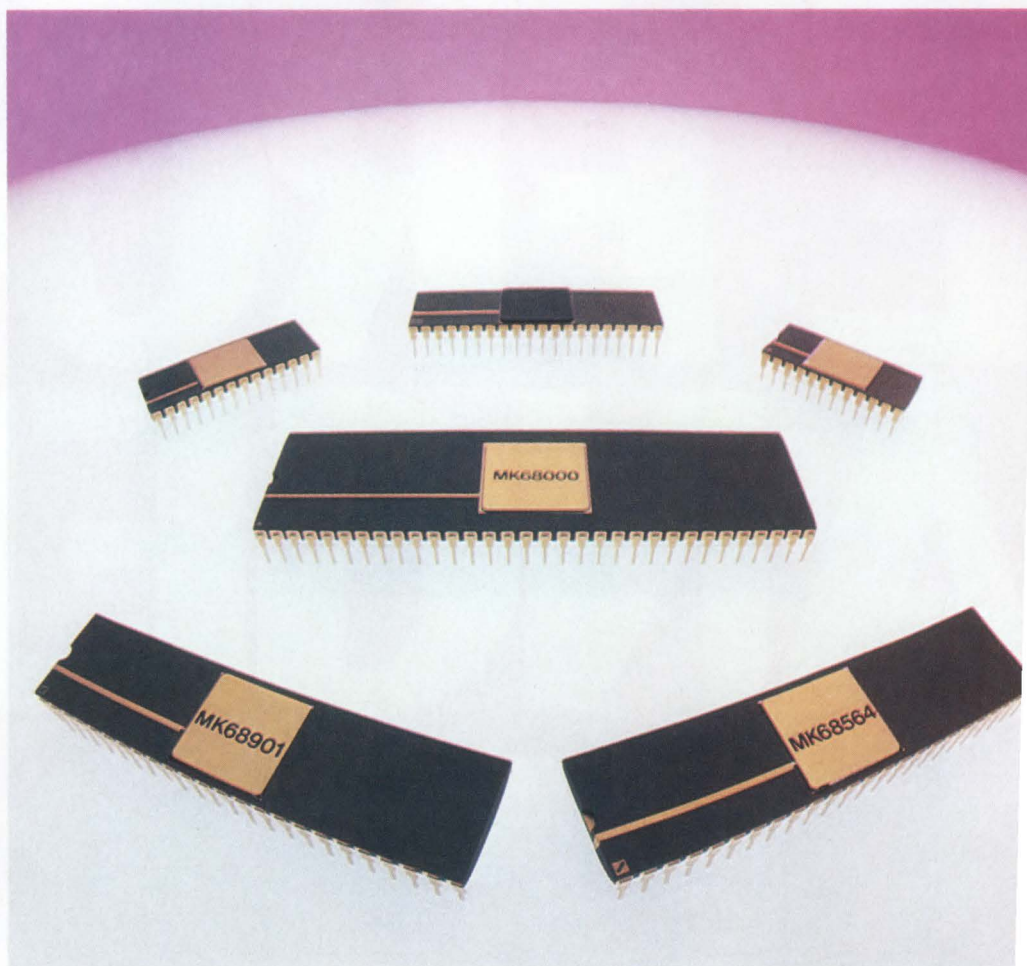
Tandon

THE MOST SUCCESSFUL DISK DRIVE COMPANIES YOU EVER HEARD OF.

Telex: 194794. Regional Sales Offices: Boston (617) 938-1916 • New York (201) 449-7720 • Atlanta (404) 934-0620 • Chicago (312) 530-7401
Frankfurt, West Germany 6107-2091, Telex 411547 • London, England (0734) 664-676 Telex: 848411. Distributors: Hall-Mark, Kierulff, Schweber.

CIRCLE 50

PERIPHER



AL VISION

Let's get clear about the overall picture. These new 68000 peripherals are not your garden-variety, 16-bit support chips. They're windows to the limits of your imagination.

Because with just these TTL-compatible devices (SIO, MFP and user-defined gate arrays) plus memory, such as our MK4564 64K RAM or MK38000 256K ROM, you can use our MK68000 to design any number of sophisticated I/O-intensive applications. And doing more with less not only saves space and weight, it also reduces manufacturing overhead and power consumption. Which in turn, also improves overall system reliability.

The MK68564 SIO features two independent, full duplex serial channels and can handle asynchronous as well as a variety of synchronous communications protocols. It has directly addressable registers and offers the choice of polling, interrupt (vectored and non-vectored) and DMA transfer modes.

The MK68901 Multi-Function Peripheral (MFP) has four timers, an interrupt controller for 16 sources, eight parallel I/O lines and a full duplex USART with programmable DMA signals, all in a 48-pin DIP.

With Mostek gate arrays, you can create custom logic peripherals for any system requirement simply, quickly and cost-efficiently. In fact, our ISHLANDSM Design System is probably the most user-friendly CAD tool available for developing semicustom logic.

Put it all together with the MK68000. It's the simplest way yet to create a vision of your own. To get the full picture, contact Mostek, 1215 Crosby Road, MS2205, Carrollton, Texas 75006. (214) 466-6000. Europe, Mostek International (32) 2.762.18.80. In the Far East, Mostek Japan KK (81) 3 404-7261.

©1983 Mostek Corporation



Protocol analyzer solves data communications network problems

Designed for electronic data processing centers, data communications equipment manufacturers, and common carriers, Hewlett-Packard's 4955A protocol analyzer can solve development, availability, and productivity problems of communications networks. The mainframe contains a 9" (23-cm) CRT, two 256k-byte cartridge tapes, a full ASCII keyboard, 8 menu soft keys, and 128k words of internal storage. For portable use, the keyboard folds up and doubles as a front panel cover. The 4955A provides analysis of communications lines with speeds ranging from 50 to 72k bps. Internal RAM storage can be used for realtime storage of data streams, physical lead status, and timing. Multiple events can be captured by 63 separate triggers.

Network connection is made via a user-selectable pod (RS-232-C, RS-449, V.35, or MIL-188C). While a full computer keyboard is provided, the eight function keys can control seven display formats on the CRT. The 4955A is particularly useful for troubleshooting. Moreover, no formal programming skill or language is required. A measurement sequence can be easily constructed using only the soft keys for selective monitoring or device simulation. Full terminal emulation and multiple trigger measurement can be done simultaneously.

For more complex operations and added features, BASIC is optional. Additional communications oriented commands and I/O control functions enhance the language. All datacom keywords from the menus can be assigned to BASIC to perform triggering or branching. The protocol analyzer can be used to emulate data-terminating equipment (DTE) or data-circuit terminating equipment (DCE) for troubleshooting a network with multiple-vendor equipment.

When realtime analysis is insufficient, tape storage allows offline examination of the various data streams. Instrument setups and measurement sequences can also be stored for field service applications. Efficient memory utilization makes maximum use of the internal 128k-word memory possible. Data bytes, lead transitions, and trigger controls are stored with time stamping (ie, long idle periods need not be stored). This eliminates the need for large disk based memory to handle large data streams.

A line diagram of any four interface control lines to pinpoint incorrect timing sequences is displayed on the CRT. Character by character examination of any transaction is possible. Eight menus are defined, each with a specific function, and the soft keys are related to correspond to the displayed fields. This

speeds user mastery of the instrument. In addition, the 4955A has resident firmware to act as an HP-IB (IEEE 488) bus controller for a printer. In the HP-IB controller mode, all keyboard functions can be accessed remotely.

The protocol analyzer costs \$20,950. Optional BASIC is \$2015; physical interface pods are \$1110 each. Delivery is 8 to 12 weeks ARO. Contact local **Hewlett-Packard** sales offices. **Circle 248**

Logic analyzer provides flexible operation through plug-in ROM packs

A multichannel mainframe with ROM, RAM, and COMM packs, the 1240 logic analyzer from Tektronix allows the user to select a wide array of capabilities and operational modes. The dual time base permits analysis of complex systems (eg, multiprocessor systems) in which separate portions of the design operate from independent clocks. Concurrent, synchronized data acquisition simplifies integration of such systems. Using information from both time bases, the 1240 permits the acquisition triggers to be defined, then displays the resulting data in a time-aligned manner.

Hardware triggers include counters, timers, duration filters, and glitch detection to 5 ns. Software analysis tools include flexible clocking and demultiplexing to handle multiplexed buses. There are 14 levels of trigger definition for isolating software execution loops. Pass counters, filters, looping, conditional branching, and data qualification are part of the 1240's software analysis capability.

A menu-driven user interface has four levels of user-selectable operation. Each level allows more powerful functions. Thus, the logic analyzer supports both novices and advanced users. The unit replaces the usual array of multifunction keys with a touch-sensitive display. Each menu uses onscreen selection fields to perform operations unique to that display, keeping dedicated keys to a minimum. With a turn knob on the front panel, scrolling in a smooth and continuous fashion can be either horizontal or vertical.

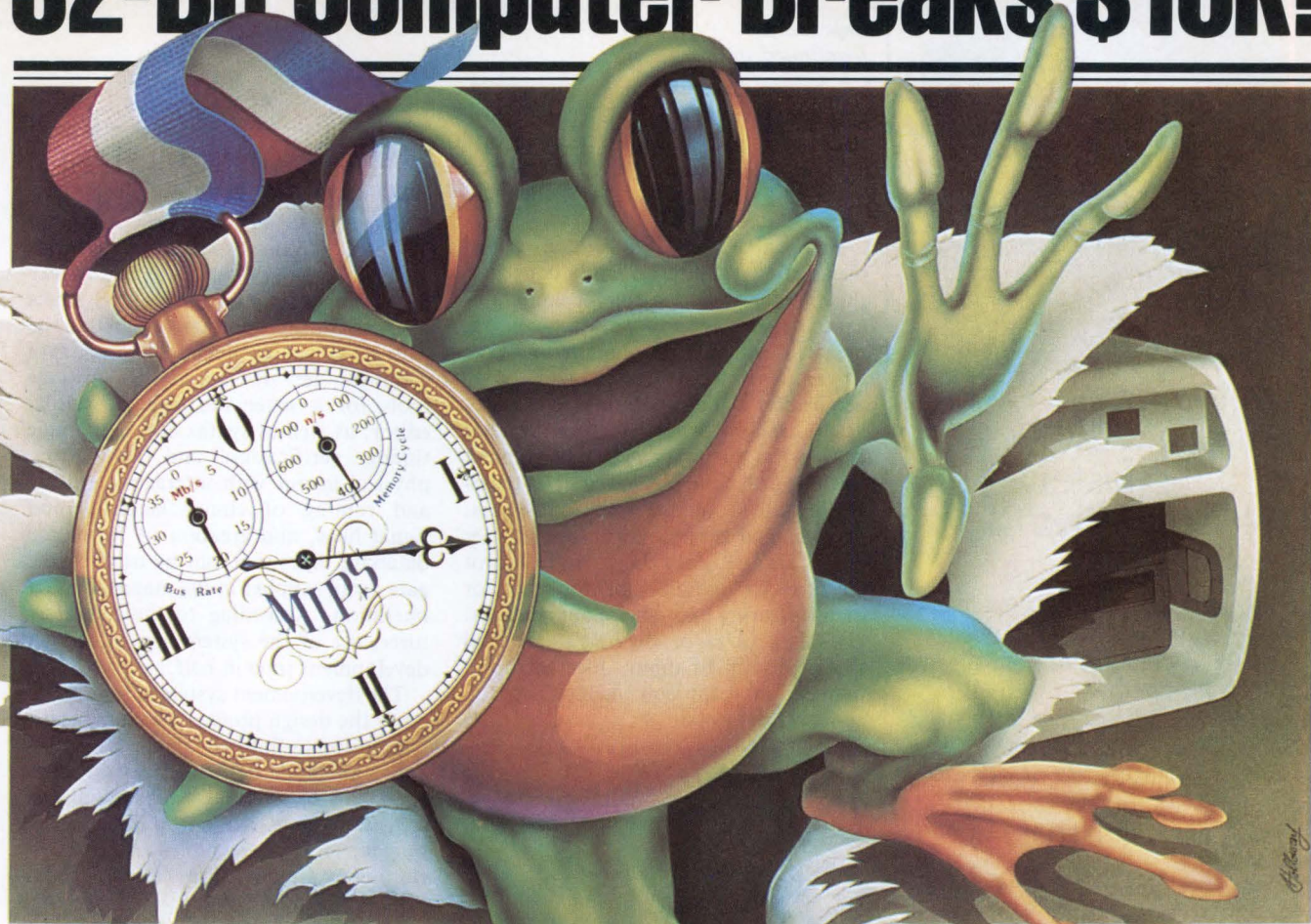
There are two types of data acquisition modules—the 9-channel 1240D1 at 100 MHz and the 18-channel 1240D2 at 50 MHz top speed. The mainframe accepts up to four of these modules in any combination. Each channel has 512 bits of data-capture memory, which can

(continued on page 74)



Soft key operation, BASIC programmability, and flexible protocol support are featured in the HP 4955A protocol analyzer. Internal 128k-word storage and dual 256k-byte tape drives provide mass storage for offline analysis of data streams and setup and measurement sequence storage.

32-Bit Computer Breaks \$10K!

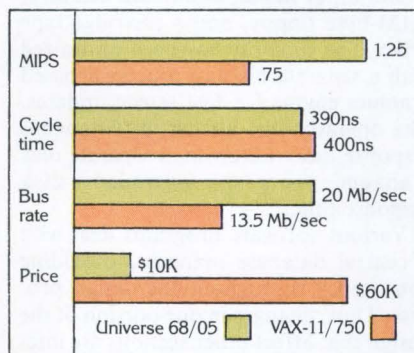


Universe 68/05 First to Smash Price Barrier

The new Universe 68/05 is the first true 32-bit computer priced under \$10,000 (OEM quantity one). "True" because, unlike other 68000-based systems, the Universe 68/05 handles 32 bits in parallel on its VERSAbus.

Outperforms VAX*

Its price is even more impressive when you look at Universe 68/05



performance versus that of 32-bit "superminis" several times more expensive, like the VAX-11/750.

High-Speed 68000, 4Kb Cache, 32-Bit Bus

The key to that performance is a 4Kb cache that eliminates processor wait-states and takes full advantage of a 12.5MHz 68000 processor. Also included are a separate 68000 I/O processor, four serial I/O ports (expandable to 64), 256Kb RAM (expandable to 3Mb), 20Mb/sec, 32-bit VERSAbus, 10Mb Winchester, 1.25Mb floppy disk, and 5-slot card cage. All in a 7-inch enclosure.

UNIX-Compatible Real-Time OS, Too

UNOS*, our UNIX* Rev7-compatible operating system with real-time features, runs Pascal, Fortran, C, BASIC, DBMS, and third party application programs.

For more information, just attach your business card to this ad and mail to Charles River Data Systems, 4 Tech Circle, Natick, MA 01760. Or call us at (617) 655-1800. We'll send you a copy of "The Insider's Guide to the Universe," a detailed discussion of the technical concepts behind this remarkable new computer.



CHARLES RIVER DATA SYSTEMS



Do-it-yourself with our WDI010 LSI Winchester Disk Controller.

Your component-level disk controller project will go much smoother and quicker with our WDI010 LSI Winchester controller. It's a 40-pin device with all the control circuitry needed to control ST500/SA1000 type drives and is compatible with most 8- and 16-bit microprocessor busses, handling data rates up to 5MHz.

Buy our board-level disk controllers. Have us build a custom board for you. Or do-it-yourself with our LSI. If you choose the latter, we'll provide schematics, microcode and generous engineering assistance.

We've got all the support components your design needs, too. To wit:

WDI011: Digital Data Separator

WDI012: Write Precompensation

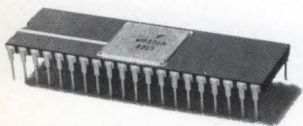
WDI014: ECC

WDI015: Buffer Manager

WDI510: LIFO/FIFO external sector buffer

WD279X: Single Chip Floppy Disk Controller.

Interested? Write on your letterhead for a free sample.



WESTERN DIGITAL
CORPORATION

Components Group,
2445 McCabe Way,
Irvine, CA 92714. 714/966-7827

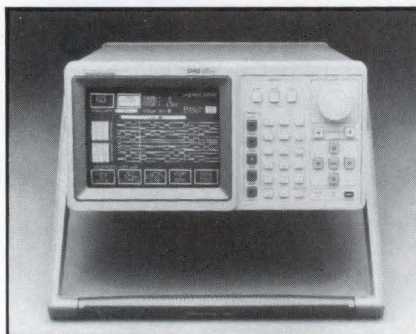
SYSTEM TECHNOLOGY/TEST & MEASUREMENT

Logic analyzer

(continued from page 72)

be chained to create wider or deeper data-capture tables. For example, a 36-channel configuration can be reconfigured to 18 channels with 1024 bits of information storage, or to 9 channels with 2048 bits.

Removable ROM, RAM, and COMM packs allow the user to easily configure the 1240 to support different communications interfaces and working environments. Tektronix is planning a large library of ROM packs for post-acquisition data processing (eg, histogram displays for software performance analysis). ROM packs will be convenient for user-definable mnemonics and disassembly for standard microprocessors. One planned ROM pack will support user definition of soft keys and permit custom configuration of the 1240 for manufacturing and service applications. COMM packs tailor the 1240's universal I/O capability to many different communications protocols such as RS-232-C and GPIB (IEEE 488).



The 1240 logic analyzer offers up to 72 channels at speeds up to 100 MHz. A dual time-base feature simplifies debug of multiclock-driven systems. Users can select four levels of functionality. A touch-sensitive display with menu-driven onscreen soft keys facilitates user proficiency.

An internal nonvolatile, battery-backed CMOS memory holds up to two complete instrument setups. Additional RAM packs can act as external nonvolatile storage for setups and reference memories. Reference memories contain correct response data and facilitate test transfer from engineering to manufacturing and field/factory service.

The 1240 logic analyzer ranges from \$7500 to \$19,500 depending on selected features. The portable instrument weighs 26 lbs (12 kg) and meets MIL-T-28800C environmental Class 3 specifications for rugged environments. Deliveries will begin in the spring of 1983. **Tektronix, Inc.**, PO Box 1700, Beaverton, OR 97075. **Circle 249**

DEVELOPMENT SYSTEMS

Gate array development system reduces circuit design time

Utilizing eight different processors and based on an expandable Multibus architecture, the Gatemaster gate array development system from Daisy Systems Corp addresses every function within the gate array design cycle. It provides a complete set of interactive software tools for a schematic oriented design editor, as well as syntax checking, logic timing verification and simulation, physical layout with interactive placing and routing of circuit elements and signal lines, and creation of formatted database tapes that can be used by the gate array supplier in the manufacturing operation. According to the manufacturer, use of the system can cut circuit development time in half.

The development system is the first to unify the design process from engineer's conception to finished layout. As a portable standalone design system priced at \$100,000, it represents a substantial cost reduction compared to traditional development methods (auto-placement and routing programs alone are priced at \$200,000 and require an external mainframe).

System hardware is based around the 10-MHz 8086 16-bit CPU and an 8087 arithmetic coprocessor. These are supported by 1.5M bytes of main memory, a 40M-byte Winchester disk, an 800- by 1024-pixel graphics display, a 19" (48-cm) monochrome or color monitor, and a programmable keyboard. A 19.2k-baud RS-232-C serial port and high speed RTE, DR11W, and Ethernet communications links are available. Options include a high resolution printer/plotter, a data input tablet, additional memory, a 1M-byte floppy, and a cartridge tape drive. The monitor has been optimized with a separate bit-slice processor based graphics engine for fast screen updates. The operator sees almost instantaneous response time. Likewise, a separate disk manager processor optimizes disk response time.

Various software programs deal with a central database manager, providing consistency throughout the design process. Thus, changes in one portion of the design that affect other sections are integrated into the final design.

The concept of correctness by construction permits the designer to define the electrical characteristics of the circuit elements when the schematic is created.

(continued on page 76)



MAKING THE LEADING EDGE WORK FOR YOU

Introducing a brainy new solution from the Wizards of Winchester Disk Controllers.

A new Winchester controller. Plus floppy controller. On one low cost board. Small enough to mount atop a 5¼" drive. And ST500/SA1000 compatible. "Smart" you say? What did you expect from the Wizards of Winchester Disk Controllers?

We promised you more for less. Our new WD1002 delivers. At \$195 (U.S. OEM quantities) it's \$50 less than its predecessor, the WD1001.

The big news, though, is that we've made the WD1002 the brainiest disk controller yet, with an abundance of new LSI innovations. Such as our WD1010 single-chip Winchester controller device. It replaces the microprocessor on our earlier boards. And about 25 other devices. Plus we've added the new WD1014 Error Correction device and the WD1015 Buffer Manager device.

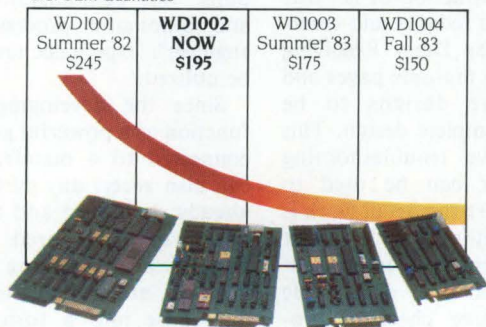
Because just about every system with a Winchester has a floppy nearby,

we included our new WD279X single chip floppy disk controller, too. So you get a complete, powerful solution on one reliable 5¼" x 8" board. And you're on the upgrade path to our upcoming WD1003 and WD1004 boards.

To make our disk controllers even more irresistible, we'll customize them to your bus and form factor. Or sell you our LSI, along with everything you need to build a controller yourself.

It doesn't take too much brains to see that it's safe, smart and simple to commit your disk-based systems to WD. Call our controller hotline, 714/966-7827 and we'll arrange to sit down with you and get into the details you need.

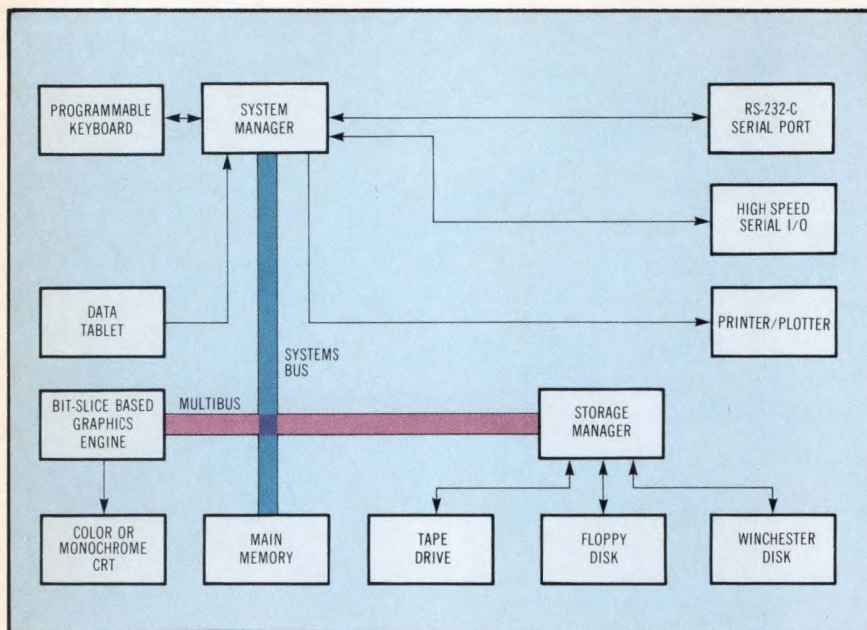
U.S. OEM Quantities



Components Group, 2445 McCabe Way, Irvine, CA 92714, (714) 557-3550

WESTERN DIGITAL
C O R P O R A T I O N

Gate array system (continued from page 74)



The Daisy Systems Gatemaster gate array development system with self-contained software for logic design, circuit simulation, timing verification with a physical layout editor, and auto-placement and routing programs. This software is supported by a multiprocessor Multibus architecture that includes a 10-MHz 8086/8087 processor pair and a bipolar bit-slice graphics processor. Up to 2M bytes of main memory are supported with a 40M-byte Winchester disk standard.

An electrical net list created by the schematic data base contains all component and signal names, as well as electrical parametric information. The list is compared in real time with all layout entries, and the system will not allow the creation of an electrical error. This alleviates the concern that a later interactive entry will upset the circuit's electrical characteristics. It also eliminates the need for external electrical and design rule verification programs.

In addition, the data base on the Daisy supported array families includes all layout rule and process information, thus avoiding physical design violations. The gate array family data base is fully documented and includes an entire set of component libraries for both the logical and physical design process. All entries, from the schematic through mask layout, are syntax checked and guaranteed correct by construction. The company supports all of the major gate array families from such manufacturers as Motorola, AMI, Texas Instruments, National Semiconductor, AMCC, and Mitel. Process independent, the system can support bipolar and MOS technologies.

Basic design is created by the engineer using the schematic editor. This editor uses the Gatemaster's hierarchical file system to permit a multilayered approach identical to the manual methods now

being used to create schematics. The designer can start with general block diagrams and logically progress through the design to the detail level drawing that shows components, transistors, and interconnections. A design data base maintains all entries by component and signal name and keeps track of all connections from page to page. Three programs check syntax and prepare the design data base for simulation.

The Daisy Network Connectivity Extractor (DANCE) syntax checks and flags any missed connections or parameter violations found on each page. It creates a net list from the graphics oriented schematic, thus eliminating a major source of error in conventional methods. Manual extraction of net lists from schematics is a tedious and error-prone operation. The Daisy Resolving Linker (DRINK) links multiple pages and permits incomplete designs to be operated on as a complete design. This facilitates interactive troubleshooting since the simulator can be used to analyze designs before the detail work is finished. The Simulator Input Generator (SING) creates a formatted component and network list and does design rule error checking. Three checking programs use assumed trace lengths to do circuit timing verification, logic simulation, and logic analysis to ensure that the logic design is error free.

A separate physical layout editor uses the graphic screen display, allowing the designer to interactively place components and route signal lines under the guidelines in the design database electrical parameters. Misconnection possibilities are eliminated by using the common data base. Thus, physical design is guaranteed to be identical to the previously checked logic design. Hardware pan and zoom permit the operator to physically inspect the detailed elements on each mask layer, as well as look at the layout globally.

Once the layout is complete, the design can be run through the timing and analysis programs with actual trace length values, and circuit operation can be confirmed. Further, test patterns can be created and, along with a correctly formatted tape, sent to the gate array manufacturer for input to his computer based layout process.

The development system incorporates both interactive and automatic layout and placement software. For example, an engineer can invoke a very fast placement routine to quickly evaluate how much silicon a particular function will require and then optimize the evaluation results. Then the interconnects are routed either automatically, or interactively if space is at a premium. The system is totally reentrant at any point in the placement and routing process.

Moreover, the user has the option of halting an automatic process, entering the interactive editor, using his intuition to make changes, and then letting the automatic process continue. Automatic placement programs will not move any component that the designer has specified. After placing the remaining elements, they will provide histogram data that indicate relative figures of merit for the proposed layout. The designer can use these to determine which ideas will be the most successful. While maintaining the advantages of automated functions, this combination of interactive and automatic processes permits an engineer's experience and knowledge to be utilized.

Since the development system can function as a powerful graphics terminal connected to a mainframe, customers can also access any custom design aids already developed and available on in-house or timeshared computers. A number of formatting programs, for example, are available to put the design data base into a form acceptable to various mainframe based simulation programs. **Daisy Systems Corp**, 139 Kifer Court, Sunnyvale, CA 94086.

Circle 250



MAKING THE LEADING EDGE WORK FOR YOU

Who says SMD Controller design is so r-r-rough? Introducing our new WD1050.

When you make the Wizards of Disk Controllers your design partners, there's no cause to approach any disk interface task with trepidation. Because now, in addition to our industry standard floppy disk controllers and ST500/SA1000 Winchester disk controllers, Western Digital delivers a single chip solution to SMD, CMD, MMD, LMD and FHT interfaces. Oh my!

It's the WD1050, a 64-pin VLSI controller/formatter. That's *one* chip, instead of up to 40MSI devices and a microprocessor. And instead of innumerable nights and weekends of software drudgery.

How powerful is the WD1050? Powerful enough to handle eight high level macro commands, auto format/verify with programmable interleaving, single/multiple record operation, hard sector formatting, CRC checking with external ECC compatibility and a 16-bit direct buffer access interface for disk drive-to-buffer data transfers.

Systems builders already following our Yellow Brick Road of disk controller solutions know that our ongoing LSI innovations soon turn into cost effective board level products for those who prefer "buy" to "build."

Starting today, though, adding the extra capacity and higher performance of SMD compatible drives to your system doesn't take courage. Just the brains to start with our new WD1050.

The next step is yours. Call our Controller Hot Line, (714) 966-7827 for more details. Or write on your letterhead.



It isn't just plug-compatible, it's software-compatible.

Introducing AMS 315, the first Winchester precisely designed to the storage specifications of 300-MB removable pack drives. So for the first time you get all the advantages of a 300-MB Winchester without rewriting your software. Or redesigning your interface.

We're truly SMD compatible.

Century's AMS 315 has the same 20,160 bytes per track.

Same 19 tracks per cylinder.

Same 823 cylinders per spindle.

Same 3,600 RPM rotation.

All in one-third the space.

Using less than half the power.

At about two-thirds the initial delivered cost.

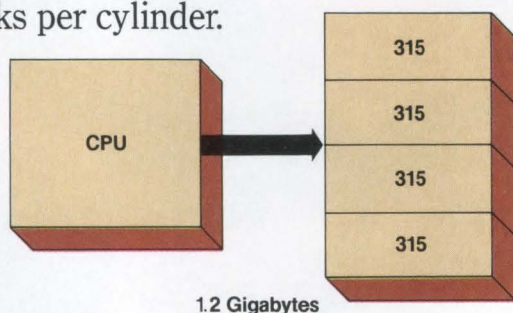
Plus you get more than twice the reliability and eliminate preventive maintenance so the on-going cost of ownership is less, too.

Expand your mass storage alternatives with Winchester technology. You'll see the difference right away. Your system never will.

Call to arrange a test drive.

Century Data Systems, Marketing Communications
C1-10, 1270 N. Kraemer Blvd., Anaheim, CA 92806,
(714) 999-2660.

AMD House, Goldsworth Road, Woking, Surrey,
England, GU 21 1JT, 44-4862-27272.



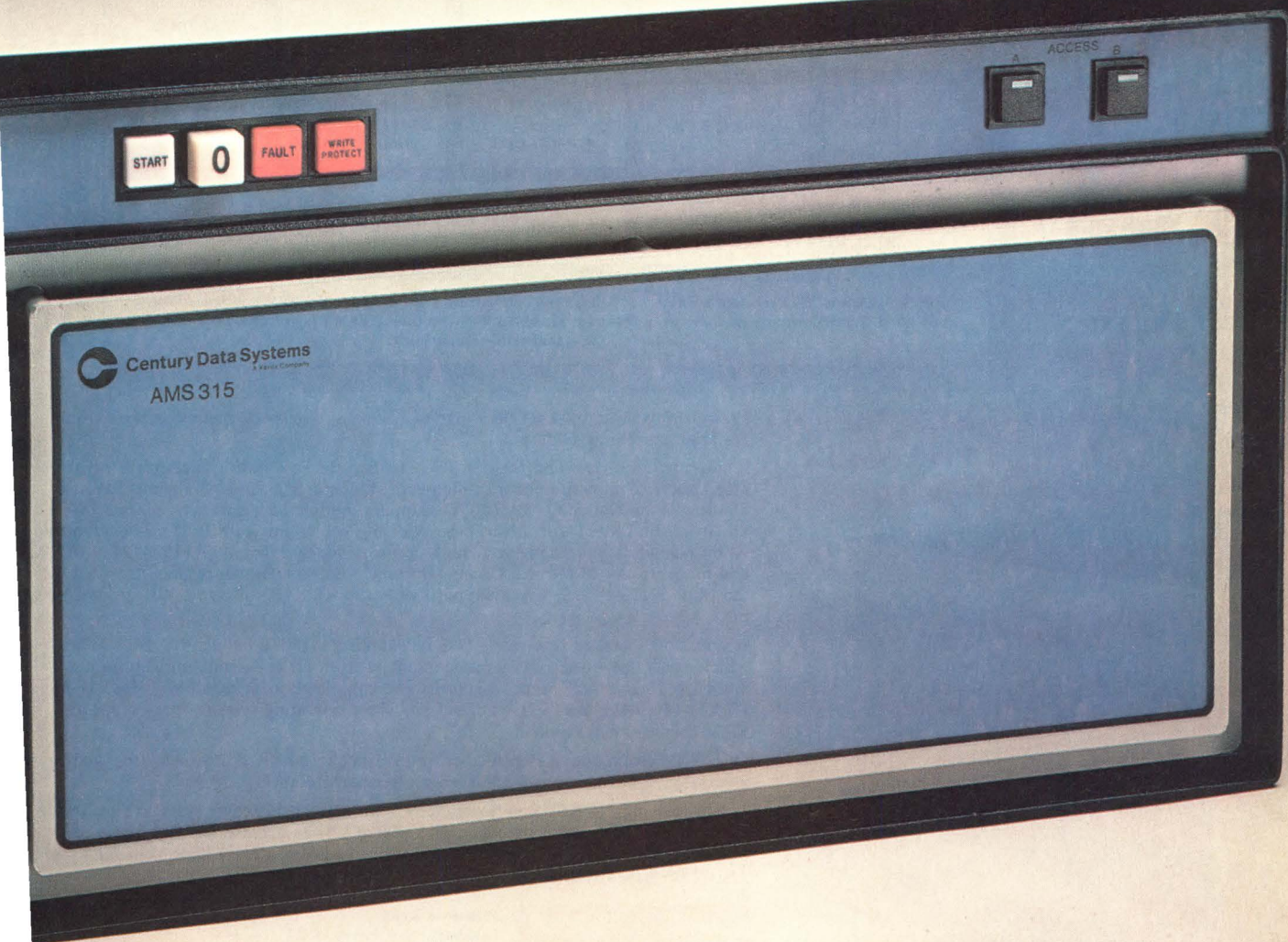
Stack four AMS 315s for 1.2 gigabytes of Winchester storage in about the same space as your 300-MB removable pack drive.



Century Data Systems

A Xerox Company

Finally, a Winchester that goes head-to-head, track-to-track, cylinder-to-cylinder, byte-to-byte with 300-MB removable pack drives.



Dataram goes to extremes to satisfy LSI-11 users.

	DATARAM B23 PLUS	PDP-11/23 PLUS	DATARAM M23	PDP-11/24	DATARAM W23
CHASSIS	5/4" Front loading	5/4" Front loading	5/4" Rear loading	5/4" Side loading or 10 1/2" Top loading	10 1/2" Top loading with 80 MB Winchester
BACKPLANE	8 x 4	9 x 4	9 x 6	9 x 6	9 x 6
I/O MAPPING	None	None	Q-MAP	KT24	Q-MAP
BUS	22-bit Q-BUS	22-bit Q-BUS	22-bit Q-BUS and 18-bit Q-BUS	22-bit extended UNIBUS (EUB) & 18-bit UNIBUS	22-bit Q-BUS and 18-bit Q-BUS
MEMORY & PERIPHERAL SUPPORT	Up to 4.0MB, but limited to 256KB when using peripherals other than RL01/RL02 or RX01		Up to 4.0MB. No basic limitation on peripherals.		
PRICING	B23, M23, and W23 are approximately 35% less than comparable DEC systems in 1.0MB configurations. Additional 1.0MB memory modules from Dataram are about 40% less than DEC's equivalent 1.0MB memory. Contact us for actual price comparisons.				

DEC, LSI-11, PDP, and UNIBUS are registered trademarks of Digital Equipment Corporation. Q-MAP is a trademark of Dataram Corporation.

From Q-BUS Pricing to UNIBUS Performance

From top to bottom, chart the range of LSI-11 system performance you get from Dataram...and only Dataram.

It starts with our low-end B23 PLUS Q-BUS system at lower (much lower!) than DEC prices. And continues with high-end M23 and W23 Q-BUS systems that use Dataram's innovative Q-MAP™ I/O mapping module to generate a separate 18-bit bus from the LSI-11/23's 22-bit bus. Allowing you to put 4.0MB of memory on the 22-bit bus while interfacing your high-performance peripherals (RM02, TM11, RX02 and more) to the 18-bit bus. Giving you much more performance than provided by the PDP-11/23 PLUS, which supports only the RL01/RL02 and RX01 on its 22-bit bus.

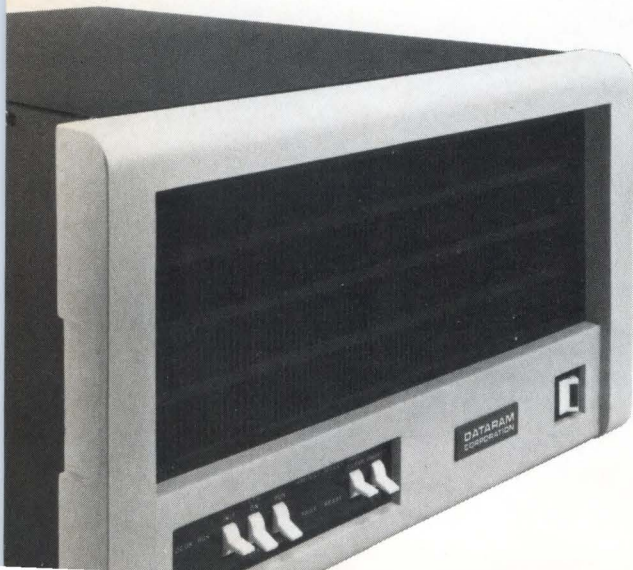
It's possible, because Dataram's Q-MAP duplicates the functions of DEC's KT24 — which exists only in UNIBUS minicomputers from DEC — enabling Dataram's 4.0MB M23 and W23 minicomputers to be completely compatible with RSX11-M, RSX11-M PLUS, RSTS, UNIX and any other operating system which supports KT24 memory management.

Our W23 system goes a step further, integrating an 80MB Winchester drive and associated controller to provide even greater performance.

Q-BUS pricing...UNIBUS performance...in an LSI-11 megabyte system. Plus a wide range of disk and tape controllers, and related LSI-11 accessories. Only from Dataram. Call us at (609) 799-0071. We'd like to tell you more about our family of LSI-11/23 based systems.

**DATARAM
CORPORATION**

Princeton Road
Cranbury, New Jersey 08512
(609) 799-0071 Telex: 510-685-2542



Electronic Show and Convention

**New York Coliseum and
Sheraton Centre Hotel
April 19 to 21, 1983**

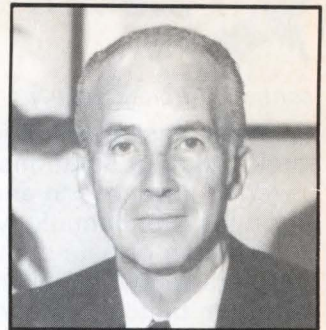
How far "Tomorrow's Technology Today," the theme of Electro/83, will take us depends on how well designers fit the barrage of rapidly developing elements into transitioning systems. From April 19 to 21 at the New York Coliseum, over 500 high technology manufacturers will shepherd this year's flock of new products before Northeastern professionals involved in the design, manufacture, and test of system level electronic components.

Of equal concern to *Computer Design* readers is Electro's Professional Program, held concurrently at the Sheraton Centre Hotel. Nearly one-quarter of the 1983 sessions will focus on updating approaches to chip technology, architecture, and applications. Discussions about improvements in nonvolatile memory technology and high speed, high performance CPU products—in addition to computer aided design and engineering—are also sure to draw crowds.

Session 1 will launch the Professional Program with a review of technical advances that are broadening the scope of 5-V only EEPROMs and nonvolatile RAMs. Guidelines for choosing between the two technologies will clarify basic issues that confront designers when contemplating how to match the memory to the application. Speakers will point to incipient developments that will govern the position of nonvolatile memory in future systems.

In many cases, high speed array processors are becoming flexible and cost-effective alternatives to bigger general purpose processors or special purpose hardware. Session 6 will recap the latest strides in the field, taking note of the array processor's growing slice of the design pie in industrial, scientific, and medical applications. Speakers will examine architectural aspects, pipelining, and parallelism, then look to future prospects that include a new generation of user friendly, system oriented array processors.

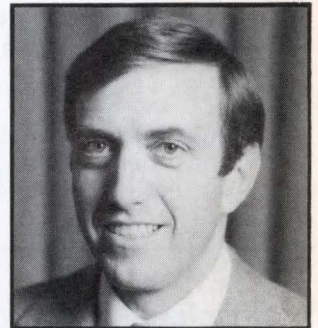
While manufacturers work out the bugs in design automation and production, logic arrays



Joseph Gavin
Keynote Speaker



Arthur Hansen
Conference Chair



Dan C. Krupka
Professional Program Chair

are gaining acceptance as workable semicustom alternatives. Bipolar and CMOS gate arrays are the favorites for both creating semicustom integrated circuits and converting discrete circuits to custom or semicustom arrays. In Session 19, industry trends will be reviewed alongside specific manufacturer advances in technology, architecture, and applications.

Growing ranks of hard disk drives in small computer systems are clamoring for VLSI controller designs that will achieve higher performance at reduced cost. Session 26 will analyze the features and design tradeoffs of several recently released VLSI controllers. Meanwhile, data communications engineers are beefing up a panoply of VLSI products to meet the burgeoning demand for higher performance in wider applications. At the top of Session 10's list is a survey of VLSI controllers for the leading local area network contenders.

Low technology circuit boards have gone back to school to cope with ECL's 7-ns switching speeds. Circuit boards are turning into sophisticated systems that often include controlled transmission lines. In addition, the surge toward chip carriers is revamping the face of integrated circuit packages. Chip carriers rely on improved techniques for dense interconnections because they employ nearly three times as many interconnections per square inch as 16-lead DIPs, for instance. Session 9 will explore techniques for dealing with higher densities, including multilayer printed circuits and discrete wiring.

(continued on page 88)

(continued from page 87)

Several sessions will follow emerging semiconductor solutions to analog problems. Covering advances in analog LSI, Session 4 will introduce the technology behind complex semiconductor data conversion systems. Speakers will weigh what the user stands to gain from building integrated circuits into a data conversion system—even though they may cost more than conventional elements. Multiplexed single-chip data acquisition systems and microprocessor compatible digital to analog converters will be prime topics.

For registration information, contact Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

Professional Program Excerpts*

Session 1: 5-V Only EEPROMs and Nonvolatile RAMs

Tues 9 to 11 am, Georgian B

Chair: W. P. Krysiak, NCR Microelectronics

- 1/1 "Silicon Nitride Oxide Silicon (SNOS) 5-V NVRAMS and EEPROMs"
T. J. Tyson, NCR Microelectronics
- 1/2 "Choosing between NVRAMS and E²PROMS: Guidelines to Match Applications to Memory Technology"
D. Pichulo, Intel Corp
- 1/3 "A New Family of User Friendly EEPROMs"
J. J. Spadaro, General Instrument, Microelectronics Div
- 1/4 "5-V Technology Makes Nonvolatile Memories Easy to Use"
G. Landers, Xicor
- 1/5 "Future Directions in Electrically Erasable ROM: Features, Applications, and Technology"
B. W. Smith, Seeq Technology, Inc

Session 3: Digital Signal Processing Hardware and Applications

Tues 9 to 11 am, Royal B

Chair: L. V. Kaplan, Texas Instruments, Inc

- 3/1 "The s28212 Signal Processor Development System"
G. Edwards, American Microsystems Inc
- 3/2 "Generalized Speech Peripheral Board Using TMS32010"
W. Gass, Texas Instruments, Inc
- 3/3 "Address Generation in Signal/Array Processing"
B. New, Advanced Micro Devices

- 3/4 "Application Areas for Digital Signal Processing Microcomputers"
S. Sweitzer, NEC Electronics USA, Inc
- 3/5 "DSP Chips Today and Tomorrow: A User's View"
J. Feldman, MIT Lincoln Labs

Session 4: Advances in Analog LSI

Tues 12:30 to 2:30 pm, Georgian B

Chair: S. Ohr, *Electronic Design* magazine

- 4/1 "CAD/CAM Building Blocks Aid Large Scale Integration in CMOS"
S. Sockolov, Intersil
- 4/2 "Acquisition, Processing, and Conversion with a Single Monolithic Device"
C. Hochstedler, Intel Corp
- 4/3 "Single-Chip Digital to Analog Converter Systems Reduce Board-Level Component Count"
E. Ritter, Signetics, Analog Div
- 4/4 "The Analog LSI Challenge—The CMOS Impact"
K-F. Lu, Texas Instruments, Inc
- 4/5 "Advances in Process Development Lead to New Architectures in Data Converters"
S. Miller, Analog Devices Semiconductor

Session 6: Array Processors—Advances in Technology and Applications

Tues 12:30 to 2:30 pm, Royal B

Chair: S. L. Cool, Analogic Corp

- 6/1 "A Survey of Systolic Arrays for Signal Processing"
J. M. Speiser and H. J. Whitehouse, Naval Ocean Systems Center
- 6/2 "Measuring the Performance of the FPS-164 Architecture"
A. Charlesworth, E. Hall, and J. Maticich, Floating Point Systems, Inc
- 6/3 "ST-100 Array Processor Architectural Highlights"
R. C. Hausman and P. A. Cannon, Star Technologies, Inc
- 6/4 "AP500—Architecture of a New Generation of User Friendly, System Oriented Array Processors"
J. B. Porter, S. L. Cool, B. A. Mattedi, and L. Mirkin, Analogic Corp
- 6/5 "MUSEC—A Powerful Data-Flow Network of Digital Signal Microprocessors"
M. J. Knudsen, Bell Labs

Session 7: Power MOSFETs—The Second Generation

Tues 3:30 to 5:30 pm, Georgian B

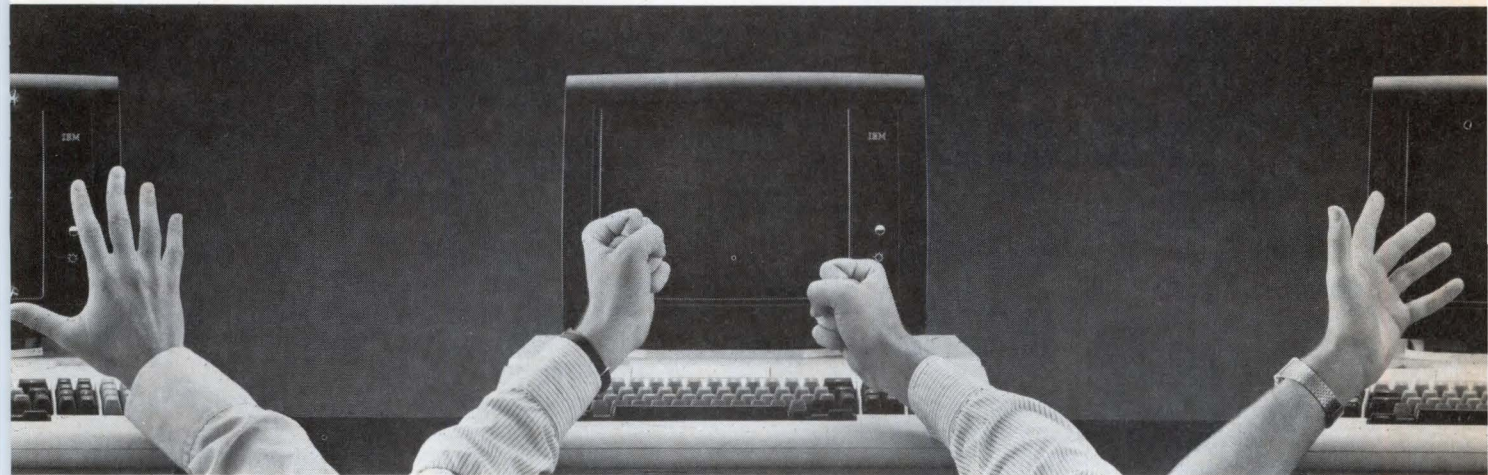
Chair: E. Oxner, Siliconix inc

- 7/1 "MOS Controlled Bipolar Devices"
B. J. Baliga, General Electric Corporate Research and Development

(continued on page 90)

*Program sessions are subject to last-minute changes.

How \$1.50 can save you \$150,000.



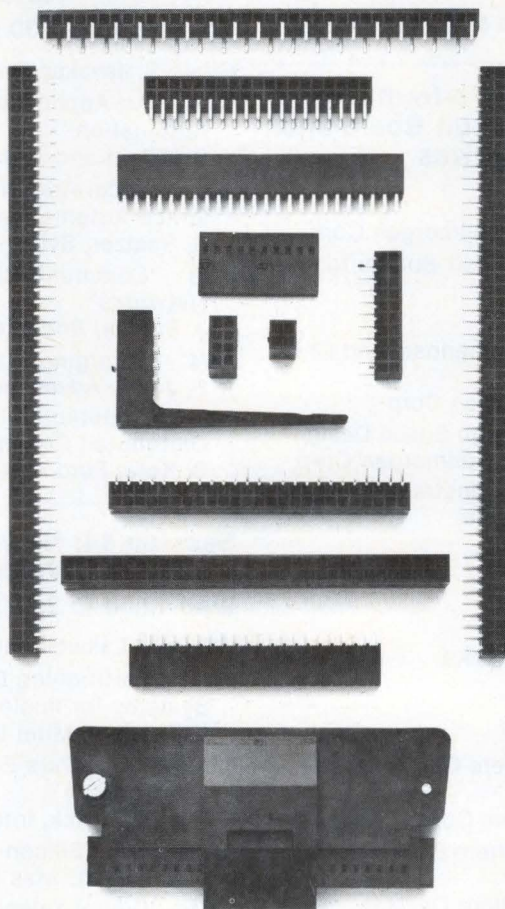
In the world of electronic data processing, choosing the wrong contact can result in lost information. And lost information means lost time and money. A simple error can cost you anywhere from \$50,000 to \$150,000—or more.

So, when you're connecting a PC board to a backplane or assembling I/O connections, check into the Cannon® ADAPTA-CON connector series. Check into the best way to not only save information, but to save time and money as well.

The ADAPTA-CON family of connectors is a versatile two-piece printed-circuit packaging system. It offers a variety of possible combinations, all emanating from a female box-type receptacle.

The heart of this system is a modified box contact that allows the designer to fabricate assemblies with over 100

ADAPTA-CON™ Connector Series



contacts that are easily mated and unmated.

Best of all, ADAPTA-CON series connectors are in stock right now, ready to be delivered wherever and whenever you need them.

For immediate information, refer to our pages in EEM. For literature, the name of your local ITT Cannon distributor or other information, contact: Commercial/Industrial Products Marketing Manager, ITT Cannon, a Division of International Telephone and Telegraph Corporation, 10550 Talbert Avenue, Fountain Valley, CA 92708. (714) 964-7400. In Europe, contact: ITT Cannon, 105A rue Colonel Bourg, B.3 1140 Brussels, Belgium. Phone: 02/735-6094.

CANNON ITT
The Global Connection

(continued from page 88)

- 7/2 "High Voltage, High Speed Cascode Bipolar/MOSFET Switch"
B. Pelly, International Rectifier Corp, Semiconductor Div
- 7/3 "MOSFET-Aided Thyristor Configurations"
L. Clark, Motorola Inc, Semiconductor Products
- 7/4 "MOSFETS in Arrays and Integrated Circuits"
R. Blanchard, Siliconix inc

Session 8: Developments in emc Design and Testing

Tues 3:30 to 5:30 pm, Royal A

Chair: W. S. Lambdin, Electro-Metrics Div, Penril Corp

- 8/1 "Designing for Commercial Electromagnetic Susceptibility (ems)"
D. M. Staggs, Xerox Corp, Office Products Div
- 8/2 "A Basic All-Weather Open Field emi Test Site"
D. N. Heirman, Bell Labs
- 8/3 "Open Site Verification of emc Antenna Factors"
E. L. Bronaugh, Electro-Metrics Div, Penril Corp
- 8/4 "State of the Art emi Testing"
F. A. Fisher and W. P. Kruse, NAP Consumer Electronics Corp
- 8/5 "Anechoic Facilities: A Controlled emi, All-Weather Test Environment"
E. D. Knowles and G. A. Roux, BE & C Engineers, Inc

Session 9: High Speed, High Performance CPU Products—Circuit Board and IC Package Alternatives

Tues 3:30 to 5:30 pm, Royal B

Chair: J. P. Plonski, Multiwire Div, Kollmorgen Corp

- 9/1 "High Performance Printed Circuit Boards for the IBM 3081 Processor"
F. Haining, IBM Corp
- 9/2 "Multiwire—Its Benefits in Subnanosecond Chip Carrier Applications"
T. J. Buck, Multiwire Div, Kollmorgen Corp
- 9/3 "The Effect of Substrates on High Speed Design"
G. Messner, PCK Technology Div, Kollmorgen Corp
- 9/4 "Packaging—The Significant Constraint Today in High Speed, Digital Based Products"
D. G. Grabbe, Amp, Inc

Session 10: VLSI Solutions for Local Area Networks

Wed 9 to 11 am, Georgian B

Chair: S. R. Naqvi, Intel Corp

- 10/1 "VLSI Circuit Provides Complete Controller for Token Pass Systems"
B. Cayton, Standard Microsystems Corp
- 10/2 "Protocols and Chips: Can There Be a Synergism?"
S. Joshi and V. Iyer, Advanced Micro Devices
- 10/3 "Programmable VLSI Controller for Local Area Network"
S. Naqvi, Intel Corp

- 10/4 "Local Networks: Token Passing Controller"
M. Stieglitz, Western Digital Corp, Communications Div
- 10/5 "General Purpose Ethernet Hardware Approach"
G. Ramachandran, Fujitsu Corp

Session 11: Probing the Limits of Optical Processing and Transmission

Wed 9 to 11 am, Royal A

Chair: W. B. Gardner, Bell Labs

- 11/1 "Physical Limits for Optical Switching and Logic"
P. W. Smith, Bell Labs
- 11/2 "Long Wavelength Ultralow Loss Fibers"
G. H. Sigel, Naval Research Lab
- 11/3 "Limits on the Propagation of Very Short Optical Pulses"
W. J. Tomlinson, Bell Labs
- 11/4 "Microfabrication Techniques for Integrated Optics"
J. T. Boyd, University of Cincinnati, Dept of Electrical Engineering

Session 13: Solving the Office Automation Puzzle

Wed 12:30 to 2:30 pm, Georgian B

Chair: S. Jayakar, Rolm Corp

- 13/1 "An Applications Oriented Approach to Office Automation"
S. Wilder and S. Jayakar, Rolm Corp
- 13/2 "Local Area Network Selection Criteria for the Office Automation Environment"
R. Shatzer, Sytek
- 13/3 "Communication Gateways between Dissimilar Networks"
J. Pathak, Bridge Communications Inc
- 13/4 "Emerging Standards in Data Communication"
S. Joshi, Advanced Micro Devices
- 13/5 "Architectural and System Design Issues for Distributed Communication Networks"
S. Kota, Ford Aero Space and Communications Corp

Session 14: New LSI Circuits Enhance Voice/Data Telecommunications

Wed 12:30 to 2:30 pm, Royal A

Chair: H. Laswell, Intel Corp

- 14/1 "Partitioning Digital Telecommunications Systems for Implementation in Silicon"
L. Thurlow, Mitel Inc
- 14/2 "Voice/Data Economies Arrive with New VLSI Components"
F. H. Cherrick, Intel Corp
- 14/3 "Total Silicon—Subscriber to Subscriber"
A. Ugge, SGS-ATES Inc
- 14/4 "Digital Telephone Integrated Circuits Handle Both Voice and Data"
A. Olesin, Motorola, Inc

(continued on page 95)

O.K., SGS.



Tell me two bright ideas for solenoid and motor driving

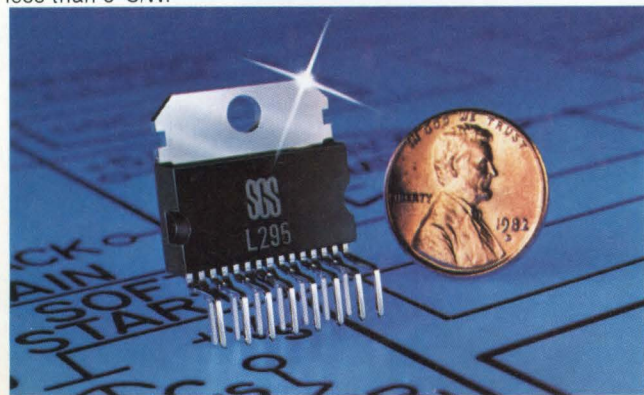
L295 High-Power, Dual Half Bridge Driver

The L295 is a dual half-bridge switchmode driver for either two solenoids or one phase of a stepper motor. Applications include hammer driving in matrix printers and stepper motor driving in either paper feed mechanisms or electromagnetic controllers.

The device incorporates two independent channels with separate inputs and outputs to provide all functions necessary for direct interfacing between digital circuitry and two inductive loads. The output current is completely controlled by switching techniques resulting in a very efficient operation. Dual supplies allow interfacing with peripherals running at voltages higher than logic.

The L295 drives loads up to 2.5A per channel from a 50V supply. Additional features include thermal protection and a minimum number of external components.

These devices assembled in the popular Multiwatt[®] package feature easy mounting and a low thermal resistance ($R_{th JC}$) of less than 3°C/W.



L294 High Power Solenoid Driver

The L294 functions as a transconductance amplifier to power solenoids in printer, hammer, and needle matrix applications. The device drives one solenoid from a supply of 50V with an output current of up to 4A.

The switchmode control of the output current allows high speed driving of electromechanical actuators with increased efficiency and reduced power dissipation.

Additional features of the L294 include thermal protection and diagnostic circuitry with latched output for recognizing conditions such as coil short circuit.



Technology and Service



- Please send me more information on your linear offerings.
- Have a sales representative contact me.

Name _____

Title _____ Company _____

Address _____

City _____ State _____ Zip _____

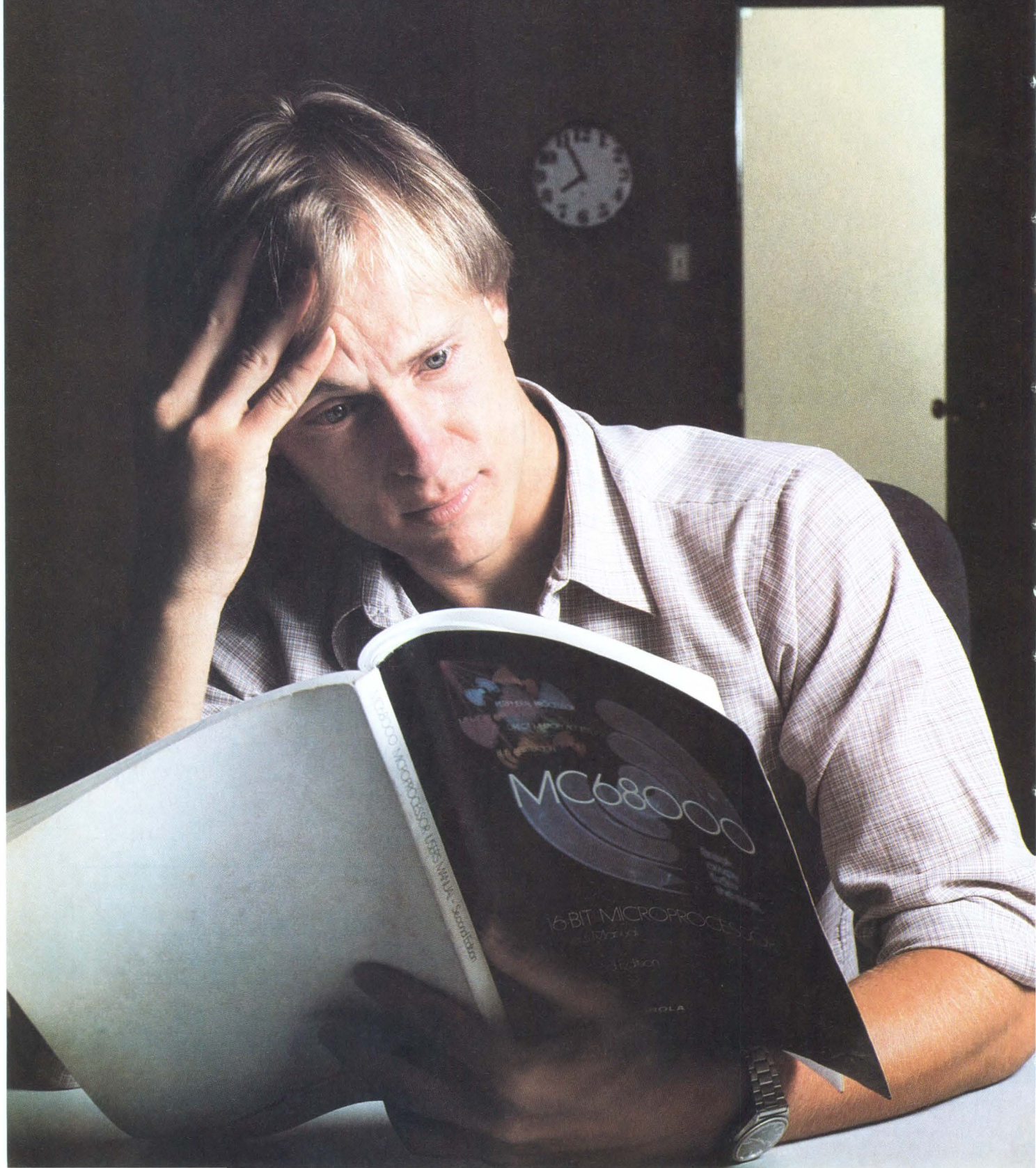
Telephone _____

CD 3/83

SGS-ATES Semiconductor Corporation
1000 E. Bell Road, Phoenix, AZ 85022 • (602) 867-6100

Sales Offices: Boston, MA (617) 890-6688; Chicago, IL (312) 490-1890; Indianapolis, IN (317) 241-1116; Dallas, TX (214) 733-1515; Austin, TX (512) 458-9182; Phoenix, AZ (602) 867-6100; San Francisco, CA (408) 727-3404; Los Angeles, CA (213) 716-6600; Sao Paulo, Brazil (11) 647 245

For the microcomputer designer
who has to turn promises into products



The power of the Color DAS comes to microcomputer software design.

To transform demanding specs into a fully functional digital design you need the best logic analyzer support you can get.

And that's what Tek's Color DAS Digital Analysis System now gives you: The best in logic analyzer performance coupled with the broadest microcomputer support on the market. Total software coverage for 10 major processors, plus support for your proprietary processors.

It's done through the new PMA 100 Personality Module Adapter and Tek's PM 100 Series of 12 microcomputer Personality Modules. You make only a single

probe connection to the system under test. The Color DAS does the rest.

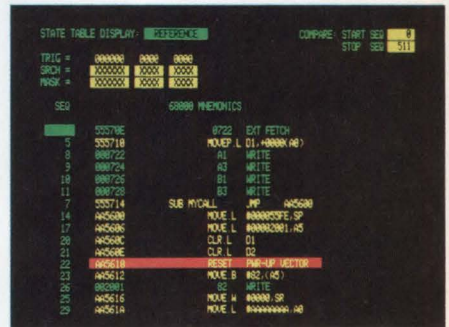
Only Tek gives you all three disassembly modes.

No matter how you want to see your real-time code execution, the Color DAS has you covered.

New Software Mnemonic Disassembly presents acquired data in a format identical to your original source code.

Hardware Mnemonic Disassembly gives you the mnemonics associated with every bus cycle.

Absolute Disassembly produces a straight hex version of data and addresses for each cycle.



User-programmed color highlights preselected data, calling immediate attention to critical code lines.

Custom mnemonics for custom chips.

You can even create your own mnemonic sets for proprietary or custom chips. And set up a special general purpose personality module to automatically handle the processor's data acquisition requirements.

Plus you get programmable color to highlight disassembled data when it appears on the display.

In every case, the Color DAS gives the best picture possible of real-time code execution. Quickly. Automatically.

Personality Modules and Mnemonics Tapes

Motorola	Intel	Zilog
6800	8085	Z80
6802	8086	Z8001
6809	8088	Z8002
68000	Multibus*	

*MULTIBUS is a registered trademark of Intel Corporation

Color software support into your microcomputer design.

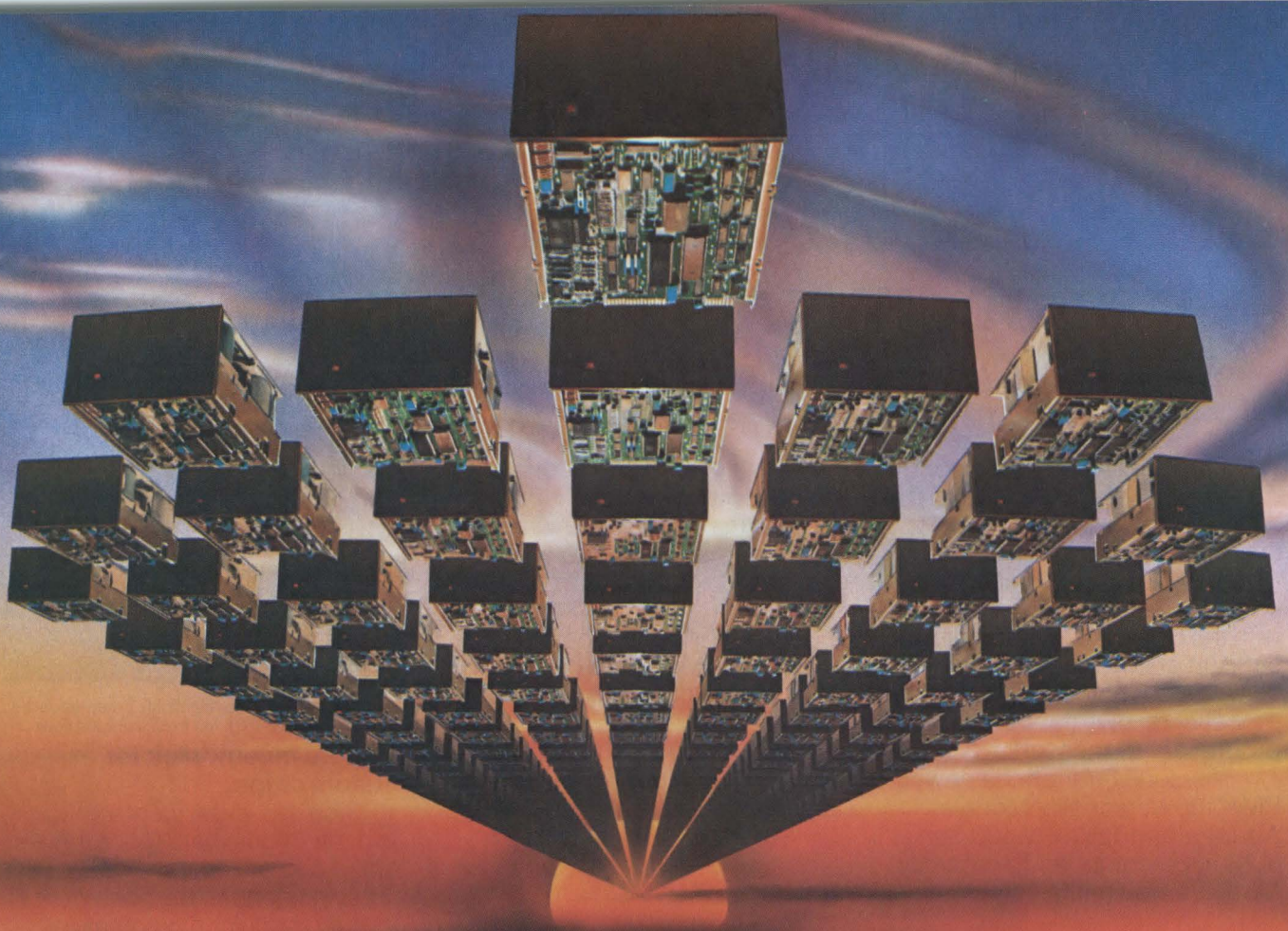
Contact your nearest Tek Sales Engineer or write us for more information.



U.S.A., Asia, Australia, Central & South America, Japan
Tektronix, Inc., P.O. Box 4828, Portland, OR 97208,
Phone: 800-547-1512, Oregon only 800 452-1877,
Telex: 910-467-8708, Cable: TEKTRONIX

Europe, Africa, Middle East Tektronix Europe B.V.
European Headquarters, Postbox 827, 1180 AV
Amstelveen, The Netherlands, Telex: 18312

Canada, Tektronix Canada Inc., P.O. Box 6500, Barrie,
Ontario L4M 4V3, Phone 705 737-2700



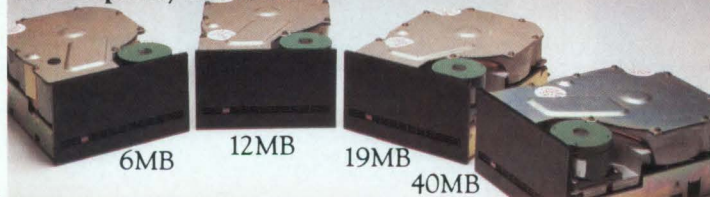
250 billion bytes delivered...

Reliable bytes, too. You've told us that. By the way you've ordered our high capacity 5 1/4" Winchester drives. Again and again. By now we've delivered more high capacity drives than any other supplier. And we've increased our production capacity to 2,000 drives a day. Just to accommodate the demand.

But don't worry. It hasn't gone to our head. We're still just as careful of quality as ever. That care has given us the industry's lowest rejection rate. And the highest performance rating.

Whichever capacity you choose — 6MB, 12MB 19MB or 40MB — you can always be confident that the last byte will be as good as the first. Call or write today for complete product and pricing information. 9216 Eton Avenue, Chatsworth, CA 91311
(213) 709-6445 TWX 910-494-4834

The Capacity Leader...



Computer Memories, Inc.

(continued from page 90)

Session 15: Engineering Research Online— Tomorrow's Technology Today

Wed 12:30 to 2:30 pm, Royal B

Chair: B. Gersh, Dialog Information Services, Inc

15/1 "Retrieval of Numerical Data at Bell Labs"
R. A. Matula, Bell Labs

15/2 "Online Engineering Information at IBM"
G. Hasslacher, IBM Corp

15/3 "Online Research Tools for Engineers: INSPEC
and EMIS"
G. Mears, IEE Station House

15/4 "A Survey of Online Bibliographic Information
Data Bases Useful to Engineers"
R. P. Caputo, Dialog Information Services, Inc

15/5 "Productivity through Information Retrieval"
J. Iervolino, Lockheed Electronics

Session 16: High Reliability Distributed Data Acquisition and Control Systems

Wed 3:30 to 5:30 pm, Georgian B

Chair: D. H. Chase, Analogic Corp

16/1 "Data Acquisition System Migration from the
Traditional Control Room Environment"
R. V. Farley, Gould Inc, S.E.L. Computer Systems Div

16/2 "Using Distributed Intelligence to Increase
System Reliability"
R. A. Havener, Analogic Corp

16/3 "Measurement and Control Systems:
A User's View"
C. Maher, Monsanto Plastics and Resins Co

16/4 "The Plant Information Center Based Upon
Control Systems"
J. A. Ward and E. L. Ellison, IBM Corp

Session 17: Display Technologies— Present and Future

Wed 3:30 to 5:30 pm, Royal A

Chair: J. A. van Raalte, RCA Labs

17/1 "Current Trends in Computer Graphic CRT"
C. Machover, Machover Associates Corp

17/2 "Liquid Crystal Displays"
A. R. Kmetz, Bell Labs

17/3 "Gas-Discharge Displays—Direct View and
Excited Phosphor"
A. Sobel, Lucitron, Inc

17/4 "Electroluminescent Displays"
L. E. Tannas, Jr, Aerojet Electro Systems

Session 18: Protecting and Exploiting Technical Developments: Basics for Engineers and Entrepreneurs

Wed 3:30 to 5:30 pm, Royal B

Chair: M. A. Lechter, Cushman, Darby & Cushman

18/1 "Basics of Property Rights in Technology"
M. A. Lechter, Cushman, Darby & Cushman

18/2 "Tax Aspects and Financing Alternatives for
R & D Activities"
H. Busbee, Coopers & Lybrand

18/3 "Employed Inventors' Rights"
B. Lehman, House Judiciary Committee

18/4 "R & D Contracts and the Issue of Rights in
Resulting Developments"
J. Wilson, R. P. Dobb, and W. T. Gerl, Georgia
Institute of Technology

18/5 "Protection of Software and Firmware"
F. R. Perillo, Digital Equipment Corp; and
M. A. Lechter, Cushman, Darby & Cushman

Session 19: Developments and Trends in Logic Arrays

Thurs 9 to 11 am, Georgian B

Chair: P. Madan, LSI Logic Corp

19/1 "Flex Array—A New Approach to Semicustom
Bipolar Circuits"
B. Loftis, Signetics Corp

19/2 "Design Automated Bipolar and CMOS
Logic Arrays—Design Considerations, Capabilities,
and Tradeoffs"
T. Chambers, Texas Instruments, Inc

19/3 "Advancements in Gate Array Technology"
C. Hardage, California Devices, Inc

19/4 "Developments in Products, Technology, and
Design Automation"
P. Madan, LSI Logic Corp

19/5 "Onchip Memory and Test Functions for
Gate Arrays"
D. Sabo, National Semiconductor

Session 20: Vision for Automatic Inspection and Robotics

Thurs 9 to 11 am, Royal A

Chair: R. M. Petitto, Electro-Optic Integrated
Controls Inc

20/1 "Vuebots: A Fast and Versatile Hardware
Approach to Vision"
L. A. Murray, Electro-Optic Integrated Controls Inc

20/2 "The Role of Vision in Industrial Robotic
Systems and Inspections"
P. Villers, Automatix

20/3 To be announced

20/4 "Intelligent Vision Systems—A Taste of the
Future . . . and Reality"
S. T. Jones, General Electric, Optoelectronic
Systems Operations

20/5 "Applications of the Pixie Machine Vision
System"
S. Wilson, Applied Intelligence Systems

20/6 "A New Approach to Machine Vision Simplifies
Application Development"
J. Trombly, Octek

(continued on page 96)

(continued from page 95)

Session 21: Primary and Secondary Batteries and Their Role as Components in Electronic Systems

Thurs 9 to 11 am, Royal B

Chair: J. Broadhead, Bell Labs

- 21/1 "Lead-Acid Batteries and Their Application to Electronics Systems"
D. P. Boden, C & D Batteries
- 21/2 "Long-Life Secondary Nickel Cadmium Batteries for Microelectronics Standby Applications"
J. A. Carcone, General Electric, Battery Business Dept
- 21/3 "High Energy Density Primary Batteries and Their Applications"
K. R. Brennen, Energy Technology
- 21/4 "High Energy Density Secondary Batteries and Their Applications"
E. J. Cairns, University of California, Lawrence Berkeley Lab

Session 22: Integrating CAD Software into the Customer Owned Tooling Approach

Thurs 12:30 to 2:30 pm, Georgian B

Chair: S. E. McMinn, American Microsystems, Inc

- 22/1 "Advancements in CAD Based ICS"
M. E. Cavanaugh, Atari, Inc
- 22/2 "CAD of IC Using Path Programmable Logic"
K. Smith, University of Utah, Computer Science Dept
- 22/3 "Integrating Foundry Processes into the Engineering Workstation"
H. Landman, Methus Corp
- 22/4 "The Development and Fabrication of a 3-micron CMOS Test Chip"
R. Cummins, Martin Marietta
- 22/5 "Potential Foundry Interface Problems when Developing CAD/Engineering Workstation Generated Designs"
M. E. Sharpless, American Microsystems, Inc

Session 23: Speech Recognition and Synthesis

Thurs 12:30 to 2:30 pm, Royal A

Chair: S. E. Dunn, Motorola, Inc

- 23/1 "Applications of Text to Speech Conversion"
D. Gilbom, Telesensory Speech Systems
- 23/2 "MCU Controlled Speech Synthesis"
T. Williams, Motorola, Inc
- 23/3 "MCU System Implementation of Speech Analysis, Synthesis, and Recognition"
L. Dusek, Texas Instruments, Inc
- 23/4 "Design of Connected Word Recognition System"
S. Viglione, Interstate Electronics

- 23/5 "Innovations in Speech Synthesis and Recognition"
J. Fattal, NEC Electronics USA, Inc

Session 24: Diagnostics and Testability Techniques in Digital System Design

Thurs 12:30 to 2:30 pm, Royal B

Chair: W. Miller, Advanced Micro Devices

- 24/1 "New PROM Architecture Simplifies Microprogramming"
J. Birkner, Monolithic Memories Inc
- 24/2 "Diagnostic Pipeline Register Enhances System Reliability and Testability"
B. Kitson, Advanced Micro Devices
- 24/3 To be announced
- 24/4 "Increasing the Diagnostic Capability of Large System Designs"
R. Rudis, Data General Corp
- 24/5 "Signature Verification Techniques in Digital Systems"
D. Hannaford, Data I/O

Session 25: Can an Engineer Really Design an IC Using an Engineering Workstation?

Thurs 3:30 to 5:30 pm, Georgian B

Chair: S. Sapiro, Computer Aided Engineering

- 25/1 "An EWS for IC Design"
S. Sapiro, Computer Aided Engineering
- 25/2 "CAD—Its Past, Present, and Future"
S. Daram, American Microsystems, Inc
- 25/3 "Optimizing the Engineering Workstation Environment for Gate Array Development"
L. Roffelsen, California Devices, Inc
- 25/4 "Using an EWS in a Systems Environment"
R. Harris, Magnetic Peripherals Inc
- 25/5 To be announced

Session 26: VLSI Implementation of a Hard Disk Controller

Thurs 3:30 to 5:30 pm, Royal B

Chair: H. Szejnwald, NEC Electronics USA, Inc

- 26/1 " μ PD7261D VLSI Hard Disk Controller"
P. Brooks, NEC Electronics USA, Inc
- 26/2 "ACS 5000 SCSI (SASI) Disk Controller Chip Set"
P. Devin, Adaptec
- 26/3 "High Integration Winchester Disk Controller"
L. Farrel, Intel Corp
- 26/4 "A Microcoded VLSI Controller for Hard and Floppy Disk Application"
S. Lau, Signetics Corp
- 26/5 "LSI Control for Winchester Drive"
J. Jaworski, Western Digital Corp

INTRODUCING THE TRANS TERM[®] 3 BATTERY POWERED TERMINAL

LIQUID CRYSTAL DISPLAY

Two lines with 40 characters each, 5x7 dot matrix font, 4.8 mm character height, upper and lower case ASCII character set, with an underscore cursor symbol.

KEYBOARD

68 keys, membrane with raise graphics and audible key-click for tactile feedback, On-line and Off-line modes with EDITing functions.

BATTERY POWERED

NiCd batteries inside the terminal supply power for up to eight hours of operation and for long-term retention of text and set-up parameters with automatic power shut-down (charger included).

OPTIONAL PRINTER

Forty column printer/plotter uses standard 2.25" wide adding machine rolled paper and a ball point pen stylus.



BUFFER MEMORY

1,920 character buffer memory organized in 24x80 or 48x40 format. Data retained by battery.

SETUP MODE FEATURE SELECTION

- Half/Full Duplex Operation
- Eight Baud Rates (110-9600)
- Parity Bit State (even, odd, mark, space)
- Buffer Format (40/80 Characters/line)
- Page/Line Mode selection
- X-on/X-off protocol
- Auto Line Wrap
- Auto Key Repeat
- Auto New Line
- Upper/Lower case
- Protected data fields

OPTIONAL MODEM

300 baud built-in modem with auto-answer and auto-dial features in either direct-connect or acoustic coupler versions.

COMMUNICATIONS INTERFACE

RS-232C compatible serial asynchronous ASCII. Eight baud rates and parity are user selectable. Current loop and RS422 I/O are available as options.

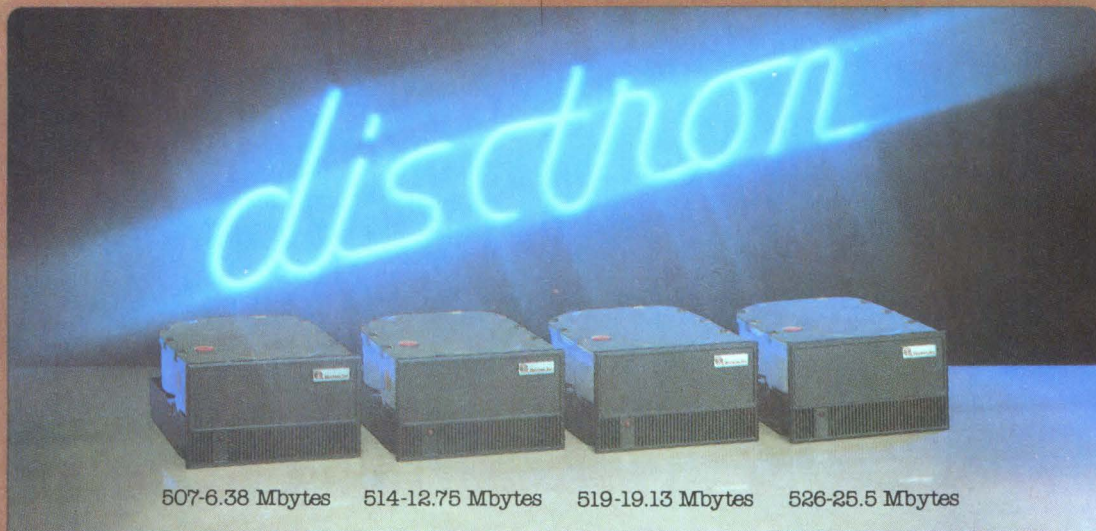
At last, the perfect answer to your portable communications requirement. It's the TransTerm 3—a compact, light weight, ASCII data terminal which will fit right into your briefcase for easy carry-around convenience. Domestic price under \$500.

COMPUTERWISE, INC.

4006 East 137th Terrace • Grandview, Missouri 64030 • 816/765-3330
TELEX 4991141 (ITT)

CIRCLE 63

To 40 megabytes. Disctron 5 1/4-inch Winchester.



Disctron Announces The 40 Megabyte Half-High 5 1/4" Winchester.



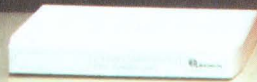
Disctron offers you more capacity, higher performance, and easier integration in 5 1/4-inch Winchester. With capacities to 40 megabytes. With average access times as low as 35 ms. And with special features—electronically damped actuator, buffered step mode, electrical spindle brake, integral microprocessor control and built-in AGC.

Easy integration. Slip these 5 1/4-inch drives into an existing minifloppy cavity. Use standard minifloppy voltages. Use standard ST506/ST412 interfacing. These drives are ready to go.

Plug in the Disctron difference in 5 1/4-inch Winchester.

To 160 megabytes. Disctron 8-inch Winchester.

disctron



(Lynx) 8"-Removable Disc Drive



8" Fixed Disc Drive

now 160
megabytes



160 Mbytes Fixed Disc Drive

Disctron has it all. Fixed and removable Winchester with capacities to 160 megabytes. Thin film media. Internal diagnostics. Self-contained shock mounting. Internal carriage lock. SMD and ANSI-standard interfacing. DC power. Plug in 10.6 megabytes on an ANSI-standard, transportable cartridge. Linear voice coil, embedded servo and microprocessor control provide precise head positioning and reliable data access.

Plug in the Disctron difference in 8-inch Winchester.

Only Disctron offers a complete family of 5¼-inch and 8-inch Winchester in fixed and removable, proprietary head technology and manufacturing, high volume manufacturing, and the solid financial foundations of CCT's more than \$75 million in assets.

More than megabytes. Discover the Disctron difference. For more information, circle our readers' service number. Or call us direct at (408) 946-6692.

the disctron
difference



CIRCLE 64

Disctron, Inc.
A Subsidiary of CCT

1701 McCarthy Boulevard Milpitas, California 95035
Telephone: (408) 946-6692 TWX: 9103382068 DISCTRON MPTS

European Representative: Micro Memory Systems Ltd., England 635-40405-Tel. 848277 Telex

If you really want protection against downtime, you can always tuck away an extra printer and use it strictly for emergencies.

But why buy two of their printers, when one Non-Stop Trilog TIP-300 will do? It's the only printer made that comes with a built-in back-up print head.

Two heads are better than one.

Most dot-matrix line printers use

only a single print head. That's fine – unless something goes wrong with the head. Then you're out of business until a service representative shows up.

On the other hand, the Trilog TIP-300 uses an exclusive two-headed system. Both 150 lpm print heads run simultaneously. Giving you a total output of 300 lpm.

Should one print head temporarily

fail, the user simply flips a switch and the remaining head continues printing at 150 lpm.

Now that's Non-Stop-Printing™!

Dual heads offer another advantage, too. Instead of being pushed to capacity like most single heads, each Trilog head runs at a 50% duty cycle. This makes them much more reliable than conventional print heads.

This is a printer with a spare for unexpected breakdowns.



Advanced innovation isn't just in our heads.

That's why we also gave Trilog printers dual tractors. They not only stabilize the paper and minimize friction, but allow the paper to move forward and backward. This gives you plotting capability and lets you generate forms. You can also print bar codes. Plus business and engineering graphics.

Five printers for the price of one.

Besides graphics, the TIP-300 gives you four other types of printing: standard data processing characters. Letter quality characters that approach the sharpness of fully formed characters. And two versions of compressed characters for paper savings and special formats.

For more information contact:

Trilog, Inc., 17391 Murphy Ave., Irvine, CA 92714. Or call (714) 549-4079. TWX (910) 595-2798.

You'll see that one of the most reliable printer combinations you can buy is a single Trilog Non-Stop Printer.

Non-Stop-Printing starts with



So's this.



For more information circle 65
For a sales contact circle 66



Mini/Micro Northeast

Computer Conference and Exhibition

**New York Coliseum and
Sheraton Centre Hotel
April 19 to 21, 1983**

Single-chip computers and processors are riding the crest of a development wave that is sweeping through general purpose and dedicated systems alike. As smart peripherals and onchip software come of age, basic architectures must be reshuffled to accommodate the metamorphoses of familiar system elements.

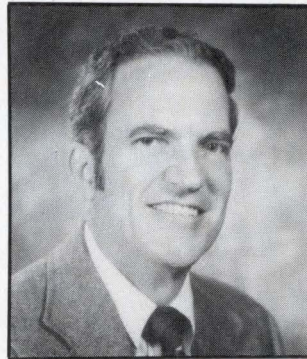
Mini/Micro-Northeast is one place for regional OEMs and system integrators who specify computers, data communications equipment, peripherals, and software to keep abreast of the legion alternatives at both chip and system levels. The technical symposium and exposition will take place on April 19 to 21 at the Sheraton Centre Hotel and New York Coliseum—in conjunction with Electro/83, but a separate event.

Advanced system concepts, development aids, and broadening applications for established technology are the backbone of the Professional Program. For instance, single-chip EPROM microcomputers are going beyond form factor emulation for their ROM based counterparts. Growing demand for modifiable program memory in medium and large scale applications is the impetus behind this development. Session 6 will review what these EPROM microcomputers can do, and discuss distinctive features such as self-programming.

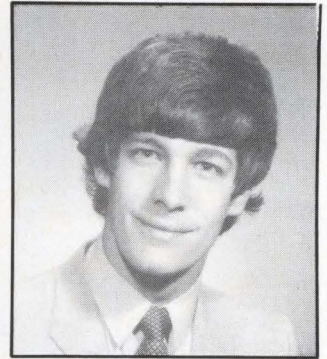
Dual processor systems are beating a path to smoother software migration and evolution. Session 1 will map out hardware and software decisions that confront designers building 2-processor systems. Floating point support for various 16- and 32-bit processors will be discussed in Session 7, with attendant architecture, hardware, and software.

Some computer designers are opting for 8-bit processors after finding that 16-bit gains do not always justify the extra hardware and software baggage. Session 8 will detail third-party operating systems that support a return to high performance 8-bit processors, while Session 3 reaffirms the value of low end microcontrollers in volume production.

For registration information, contact Jerry Fossler, Electronic Conventions, Inc., 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965



Charles Sutherland
Steering Committee Chair



Kerry Maletsky
Professional Program Chair

Professional Program*

Session 1: Dual Processor Systems Tues 9 to 11 am, Georgian A

Chair: R. Mateosian, Zilog, Inc

- 1/1 "Dual Processors Bridge the Gap"
B. Cohen, Digital Research
- 1/2 "Dual Processor Systems Using Zilog's z800 CPUS"
F. Lynch, Zilog, Inc
- 1/3 "Xedex's Baby Blue Coprocessor Technology for the IBM Personal Computer"
D. Murray, Xedex
- 1/4 "16-Bit Zoom Computer Attaches to Any Z80 CP/M System"
W. Fry, Exxon Office Systems
- 1/5 "The Design of the Cromemco DPU"
D. Mandelkern, Cromemco

Session 2: Advanced Microprocessor System Concepts

Tues 12:30 to 2:30 pm, Georgian A

Chair: S. E. Dunn, Motorola, Inc

- 2/1 "Using Microcode to Extend a CPU Architecture in a Manner Transparent to Software"
B. Rash, Intel Corp
- 2/2 "The z8000 Family Provides Advanced System Solutions"
T. Cramer, Zilog, Inc

(continued on page 106)

*Program sessions are subject to last-minute changes.

Choose between Winchester systems or controllers

Complete systems to minimize system costs . . .

SMS FWT series disk peripherals provide up to 80M bytes of 8" Winchester disk storage and 1M bytes of floppy disk storage for DEC's* PDP-11, LSI-11, and VT-103, INTEL Multibus** and other microcomputers! In only 5 1/4" of table top or rack space you also get the following benefits:

- Choose 8.9Mb, 17.8Mb, 35.Mb, or 71.2Mb of formatted Winchester disk storage.
- Up to 427K bytes/sec data transfer for Winchester and 63K bytes/sec for floppy.
- Supports IBM single and double density diskette formats plus DEC's RX01/RX02 formats or INTEL 202 format depending on host computer.
- Single board interfaces are compatible with PDP-11 Unibus, LSI-11 Q-Bus, INTEL Multibus or use your own adapter card for special microcomputer busses.
- Convenient Winchester backup requires only 40 seconds per 1.2M byte floppy diskette.
- Off-line and on-line system and drive tests verify correct disk and controller operation.
- Automatic error retry, ECC (Error Correction Code) and Winchester disk flaw management insure exceptional data integrity.

Or just controllers to optimize system packaging.

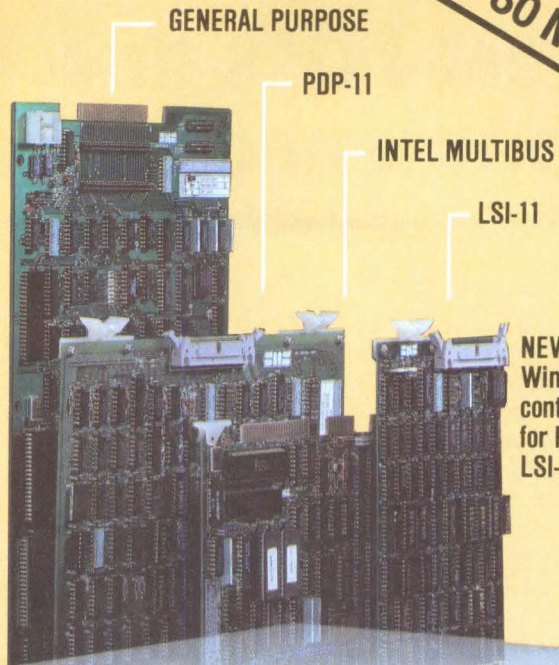
All controllers used in SMS disk peripheral systems are available separately. Each controller supports (2) Shugart/Quantum Winchester and (2) Shugart floppy disk drives, utilizes patented PLL circuitry to provide maximum margins for worst case bit shifted data recovery, incorporates ECC (Error Correction Code) and includes on-board self test! Additional features are:

DEC PDP-11/LSI-11

- Single LSI-11 dual height or PDP-11 quad height interface plus formatter board.
- On board bootstrap and 22 bit Q-bus support.
- Standard RT-11, RSX-11M, UNIX,*** and SMS utility software support selective file backup and load operation.
- High performance data transfer of up to 427 bytes/sec.
- Emulates DEC RX02 floppy disk controller.
- Automatic recognition of RX01, RX02 and IBM diskette formats.

INTEL MULTIBUS

- Single Multibus compatible PC board requires only 5A (max.) @ 5 volts.



NEW 5 1/4" Winchester/floppy controller available for PDP-11, LSI-11 and Multibus!



- Direct connection to (2) Shugart/Quantum and (2) Shugart floppy disk drives. Eliminates external data separator board.
- Interface and command compatible with INTEL iSBC 215A and iSBX 218 controller boards.
- Supports IBM and INTEL iSBC 202 diskette formats.

GENERAL PURPOSE

- Single board controller requires only 5A (max.) @ 5 volts.
- Interface, dimension and connector compatible with Shugart 1403D.
- Direct multi-sector disk transfer of up to 427K bytes/sec.
- Easy to use byte parallel general purpose interface.



Scientific Micro Systems, Inc.

777 E. Middlefield Road Mountain View, California 94043
(415) 964-5700

AUTHORIZED SMS DISTRIBUTOR
FOR DEC Q-BUS PRODUCTS:
FIRST COMPUTER CORPORATION—(312) 920-1050

SALES OFFICES: **Phoenix, Arizona** — (602) 978-6621 **Boston, MA** — (617) 246-2540
Atlanta, Georgia — (404) 296-2029 **Morton Grove, Illinois** — (312) 966-2711 **Yorba Linda, California** — (714) 993-3768

Meet HP's new 1630 Logic Analyzer a bottleneck...and ecstatic when we

From now on it makes no sense to buy an analyzer that offers timing and state measurements only. Not when you can have these capabilities plus interactive analysis and software performance measurements too. All for less than the cost of a good timing and state machine alone.

That's what you get with HP's new 1630A/D Logic Analyzer. It delivers advanced hardware and

software testing and debugging power. Plus the ability to quickly spot software bottlenecks and inefficiencies. And a way to resolve hardware/software fingerprinting conflicts. With one low-cost instrument.

HP's new 1630 extends the power of logic analysis to span most of the development cycle. And productivity gets a big boost. Because the 1630's simple interface, combined with low-cost peripheral compatibility, speeds setups and documentation. Best of all, it's affordable for even the smallest lab.

At \$8,600*, the 1630A gives you 35 channels of state (to 25 MHz), 8 channels of timing (to 100 MHz), or, in the interactive mode, 27 state and 8 timing.

For \$10,630*, the 1630D offers 43 channels of state or 16 timing. In the interactive mode, you have a choice of 35 state and 8 timing or 27 state and 16 timing. Both models include software performance analysis.

Here's what all that capability can do for you.



You'll be amazed when it shows you show you the price.

Software Performance Analysis

Ever had a software bottleneck? A routine that takes too much time? Those problems won't stand in your way with this powerful new analysis mode. Histograms of time-interval distribution eliminate guesswork by

showing you best case, worse case, and average time between any two events you define...nonintrusively... while your system is operating. Great for benchmarking. And spotting out-of-spec modules.

Histograms of memory space activity show where the action is. If you've got a bottleneck, this display leaves no doubt about its location.

Interactive Measurements

Now there's a logical way to resolve hardware/software fingerpointing feuds. The 1630 lets you monitor bus activity in the state mode, trigger on a given bus pattern, then view asyn-

chronous status and control line activity in the timing mode. This quickly unravels problems such as I/O port malfunctions. Similarly, you can establish trigger conditions

based on timing parameters, then view state activity. This correlates hardware malfunctions to software errors. For example, a false reset due to a glitch.

Timing and State Analysis

In traditional operating modes, the 1630 delivers new sequencing, triggering, and store qualification power. For timing analysis, this includes pattern triggering ANDed with a transition or glitch, edge or glitch triggering, and time qualification of pattern triggering. In the state mode, four user-defined terms can be used in any combination to define sequence, store qualification, trigger and restart conditions. With these resources, you get right to the problem. Without sorting through tons of data.

But that's not all. The 1630 makes it easier yet by talking your language. You can assign alphanumeric labels to input channels and status or control line patterns. Measurements are then displayed in your system's terminology. In addition, the 1630, with low-cost peripherals, performs inverse assembly. So you see listings in target microprocessor mnemonics. From now on, you needn't struggle with time-consuming conversions.

Get all the details on this advanced analyzer. See how it takes the drudgery out of logic testing, debugging and analysis, speeding your project to completion. Call your local HP sales office listed in the telephone directory white pages. Ask for an HP field engineer in the electronic instruments department.

* U.S.A. list prices only.



**HEWLETT
PACKARD**

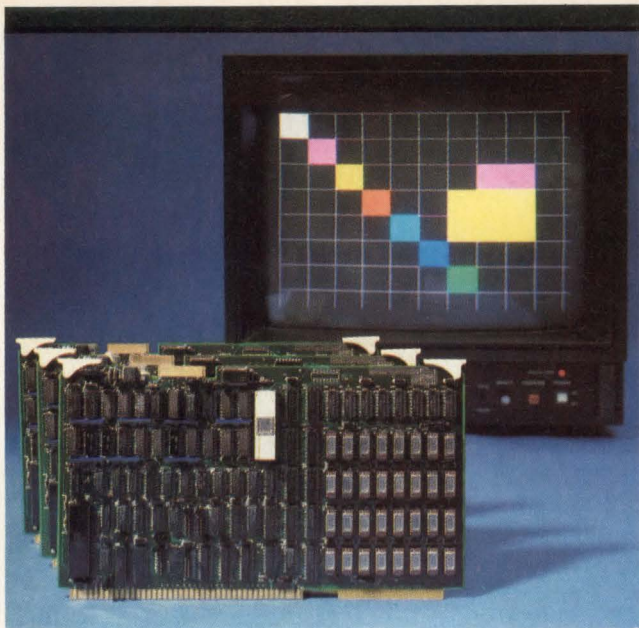
CIRCLE 68



DESIGNED FOR
HP-IB
SYSTEMS

HP-IB: Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a measurement system.

0801208



1024 x 1024 16 COLOR GRAPHICS CONTROLLER, \$4,100 in 100 QUANTITY.

It's a price breakthrough even at \$7,200 for a single unit. Our multibus display controller gives you performance too with 8, 16, or 256 colors; hardware, pan, scroll, and zoom; multiple plane BIT, BLT, and fast vector writing with the new NEC 7220.

Boards can be modularly configured to give you upgradeable options. You can start with a 2 board 8 color system; move to 3 boards with 16 colors, or grow to a 256 color set with overlay planes. Palettes of 2^{12} or 2^{24} can be selected for our look-up-table. The same boards can be configured for grey scale.

Hardware features don't become software pains either. Our Unix "C" driver and core package allows you to work above low level mental gymnastics.

Want more information? Circle the bingo or call us at (617) 275-4330 for an individual quote. Put some color in your systems life.

IKIER TECHNOLOGY, INC.

7 Oak Park Bedford, MA 01730



Mini/Micro Northeast

(continued from page 102)

- 2/3 "The 32-Bit Solution"
J. Browne, Motorola, Inc
- 2/4 "NS 16000 Family: A Top-Down Approach"
G. Kates, National Semiconductor
- 2/5 "Extending Computer Power with the TMS 320 Family"
L. Kaplan, Texas Instruments, Inc

Session 3: Microprocessor Development Aids Tues 3:30 to 5:30 pm, Georgian A

- Chair: M. J. Campo, Pro-Log Corp
- 3/1 "STD Bus Development Aid"
M. J. Campo, Pro-Log Corp
- 3/2 "Emulation Comes to CPM"
S. Thatcher, Applied Microsystems
- 3/3 "High Level Language Debugging Aids"
D. Johnson, Tektronix Inc
- 3/4 "Logic Analysis in Microprocessor Development"
R. Freund, Nicolet Paratronics Corp

Session 4: Single-Chip News Wed 9 to 11 am, Georgian A

- Chair: K. Kristie, Motorola, Inc
- 4/1 "Advanced Features of the New Members in the z8 Microcomputer Family"
S. Jasper, Zilog, Inc
- 4/2 "Performance Advances in Single-Chip Microcomputers"
J. Lanagan, Motorola, Inc
- 4/3 "The MK68200 Offers Design Flexibility for High-End Applications"
D. Folkes, United Technologies Mostek
- 4/4 "Continuing the Evolution of High Performance Single-Chip Microcontrollers"
M. Pawolski, Intel Corp
- 4/5 "High Level Languages Speed Application Development"
R. Dumse, Rockwell International

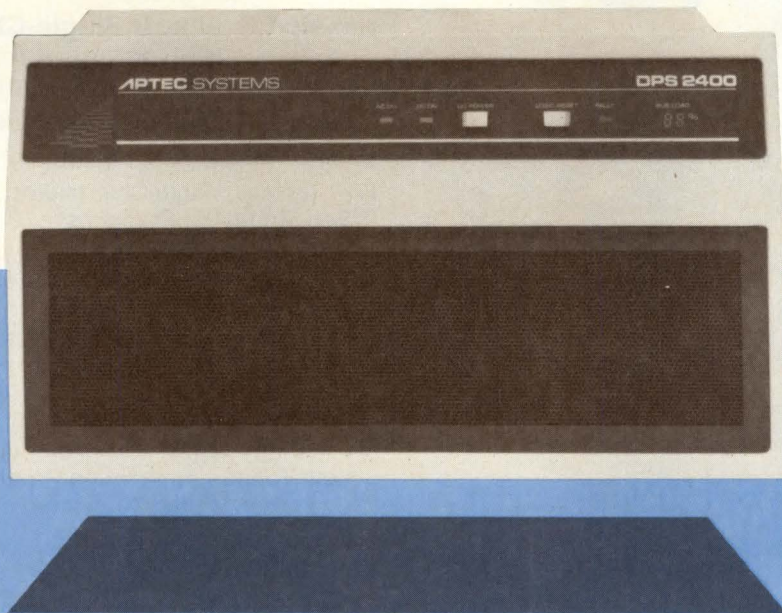
Session 5: Low End Microcontrollers Continue to Dominate Volume Productions

Wed 12:30 to 2:30 pm, Georgian A

- Chair: R. L. Murray, Motorola, Inc
- 5/1 "A Low Cost Single-Chip Microcomputer Solves a Wide Range of Applications"
R. Koster, Texas Instruments, Inc
- 5/2 "8-Bit Microcomputers Enter the Very Low End Applications Field"
B. Huston, Motorola, Inc
- 5/3 "Single-Chip Microcomputers for High Volume Applications"
J. Fattal, NEC Electronics USA, Inc
- 5/4 "Cops Microcontroller"
L. A. Distaso, National Semiconductor
- 5/5 "A New High Performance Microcontroller"
V. R. Ranganath and R. Palm, Synertek

(continued on page 108)

THE SIMPLE SOLUTION TO COMPLEX SCIENTIFIC COMPUTING.



Now You Can Create a 10 to 100 Megaflop "Supercomputer" for Your VAX* Using Multiple Array Processors.

Introducing the DPS-2400 Dimensional Processing System™ from Aptec. It's an evolutionary system concept that lets you configure powerful attached subsystems — using your choice of multiple array processors and other peripherals — free from the bottlenecks of current approaches.

Data acquisition and multiprocessing systems deliver far greater power when controlled by DPS-2400 than when controlled directly by your host.

The solution is simple when you start with DPS.

DPS-2400 attaches to the UNIBUS* of your VAX* or PDP-11* computer to form the central node of an attached subsystem using UNIBUS-compatible peripherals. DPS contains a 24MB/sec. Data Interchange Bus to handle multiple, concurrent data transfers without loading your UNIBUS. Up to 24MB of high speed mass memory provide efficient data staging for pipelined and parallel processing used in 2-D and 3-D applications. And, a set of fully programmable Data Interchange Adapters provide individual control of all DPS subsystem peripherals, including up to ten array processors.

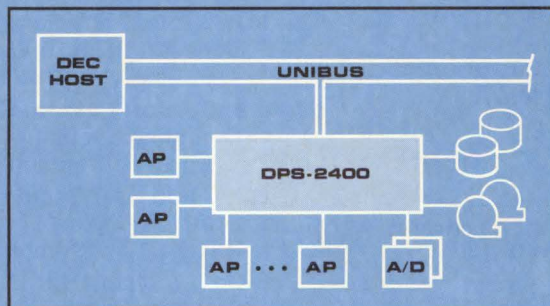
Because DPS is designed specifically for multiprocessing and dataflow operations, it can greatly increase the efficiency and throughput of a single array processor. DPS makes systems with multiple APs not only possible, but extremely economical. And, because it off-loads subsystem control, DPS frees your host for the higher level supervisory tasks for which it is best suited.

Aptec support speeds and simplifies application development.

Hardware integration is greatly simplified by DPS's full compatibility with your UNIBUS peripherals and a variety of standard, available array processors. Our STAPLE** application development software, and field application assistance, are provided to get you up and running in the shortest possible time.

The Dimensional Processing System from Aptec. There's no simpler, faster, or more economical route to a working solution for scientific computing.

For more information or to arrange a demonstration contact Aptec today.

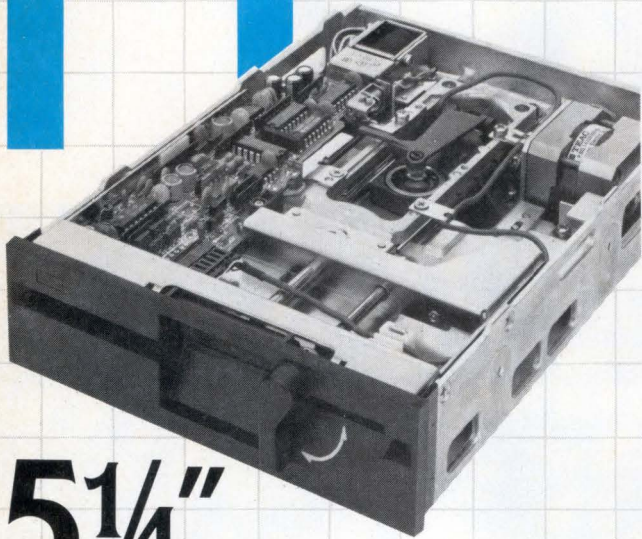


*UNIBUS, VAX and PDP-11 are trademarks of Digital Equipment Corp.
STAPLE® is Aptec's **STructured **AP**plication **L**anguage & **E**xecutive.

CIRCLE 70

APTEC COMPUTER SYSTEMS, INC.
10180 S.W. Nimbus Avenue
Portland, OR 57223 (503) 620-9840
Telex 467167

HALF HIGH



5 1/4" Floppy Disk Drives TEAC FD-55 Series

AT 1 5/8" HIGH, TEAC FD-55 SERIES 5 1/4" FLOPPY DISK drives use half the space and run cool at half the power of conventional drives. High-reliability, low-noise brushless DC motors provide an MTBF of over 10,000 hours, backed by a one-year parts and labor warranty.

FD-55A	FD-55B	FD-55E	FD-55F
• 48tpi	• 48tpi	• 96tpi	• 96tpi
• 40 track	• 40 track	• 80 track	• 80 track
• 250KB	• 500KB	• 500KB	• 1MB
• single side	• double side	• single side	• double side

Power Requirements:

DC +12V $\pm 5\%$ 0.3A typical, 0.7A max.
DC + 5V $\pm 5\%$ 0.5A typical, 0.7A max.

Phone, write or wire TEAC Corporation of America for complete technical data, price and delivery.



TEAC Corporation of America
Industrial Products Division
7733 Telegraph Road
Montebello, CA 90640
213/726-0303

© 1982 TEAC Corp.
MP82501M



Mini/Micro Northeast

(continued from page 106)

Session 6: EPROM Single-Chip Microcomputers—More Than Just a Prototyping Tool

Wed 3:30 to 5:30 pm, Georgian A

Chair: J. Millar, Texas Instruments, Inc

- 6/1 "EPROM Single-Chip Microcomputers for Self-Modifying Programs"
B. Huston, Motorola, Inc
- 6/2 "A Powerful EPROM Single-Chip Microcomputer Which Can Program Itself"
J. Wallace, Texas Instruments, Inc
- 6/3 "Will There Be ROM Based Microcontrollers in 1985?"
A. Toth, Intel Corp
- 6/4 "Piggyback EPROM Microcomputer Solves Low Volume Application Problems"
D. Folkes, United Technologies Mostek
- 6/5 "The z8 Protopak Offers a Low Cost Solution"
K. Marks, Zilog, Inc

Session 7: Floating Point Support for 16/32-Bit Microprocessors

Thurs 9 to 11 am, Georgian A

Chair: G. R. Kates, National Semiconductor

- 7/1 "Fast Floating Point for Speed-Hungry Applications"
G. Martin, National Semiconductor
- 7/2 "High Performance Floating Point Coprocessor for Protected Multi-User Systems"
J. Bhat, Intel Corp
- 7/3 "Floating Point Power for the MC68000 Family"
J. Boney and V. Shahan, Motorola, Inc
- 7/4 "Zilog z8070 Floating Point Processor"
R. Mateosian, Zilog, Inc
- 7/5 "99000 Family Incorporates Floating Point Onchip"
A. Orben, Texas Instruments, Inc

Session 8: Third-Party Software Enhances the Versatility of High Performance 8-Bit Microprocessors

Thurs 12:30 to 2:30 pm, Georgian A

Chair: J. F. Stockton, Motorola Semiconductor Inc

- 8/1 "Third-Party Software from a Semiconductor Vendor's Point of View"
J. F. Stockton, Motorola Semiconductor Inc
- 8/2 "An OEM's View of the OS-9 and Flex Operating Systems"
E. M. Pass, Computer Systems Consultants Inc
- 8/3 "End-User Requirements Determine an Operating Systems Choice"
R. Tripp, The Computerist Inc
- 8/4 "Problems with Supporting Applications Programs in a Multiple OS Environment"
R. Dennington, Introl Corp
- 8/5 "8-Bit vs 16-Bit: A Performance Comparison of Multi-User Operating Systems"
J. Heckman, Universal Data Research Inc

Retro-Graphics™ and DEC.



Now GEN.II™ delivers Tek 4010/4014/4027 compatible graphics on your VT100, VT101, VT102, VT103, VT131, or VT132.

Generating cost-efficient yet sophisticated images on your DEC™ terminal first begins with your choice of VT100™-Series displays. Then add Digital Engineering's GEN.II Retro-Graphics terminal enhancement. Our plug-in upgrade transforms an otherwise "dumb" terminal into a multi-featured bit-map graphics workstation, capable of plotting complex business and technical renderings. In a raster-scan resolution of 800 by 480 and in concert with your Tektronix®-based program.

But best of all a Retro-Graphics enhancement costs only a fraction of what you'd pay for an equivalent graphics terminal: about \$1200 - 1800, depending on the GEN.II model you order.

Introducing GEN.II Retro-Graphics for DEC. More graphics power and Tek™ simulation.

An easily installed PC card assembly, our second-generation enhancement provides emulation of the Tektronix 4010 graphics terminal *plus* one-color simulation of the Tek 4027 color graphics terminal.

And for extra power — and compatibility with your existing or future Tek 4014 applications programs — *GEN.II for DEC also features one-color 4014 simulation.* With little or no software modification.

In addition, GEN.II's 32 Kb's of "local" intelligence ensures that images come up quickly — and costly terminal-host data transmissions are held to a minimum. And because GEN.II is based on industry-standard Tektronix protocol, graphics programming and operation are considerably eased. Case in point: by entering from the keyboard or computer the following command string

!PIE 100, 0, 360, 45

an eight-sided *polygon* with a radius of 100 will be plotted and its interior will be *filled* with a shading pattern (GEN.II maps 4027 colors to dithered shades).

With similar high-level command strings, GEN.II will also perform *arc* and *vector drawing*. *Define* and *shape text characters*. *Store* and *recall* graphs. And, while in 4014 mode, *perform additional graphics annotation using all four 4014 character sets.* And you get all this with no loss of existing terminal features.

Software compatibility ensures your long-term investment.

Since our GEN.II products for DEC provide 4010/4014/4027 compatibility, their use with utility and applications programs, whether now or in the future, is guaranteed. Currently, more than 20,000 Retro-Graphics products are performing successfully on graphics programs such as *DISSPLA®* and *TELLAGRAF®*, *PLOT 10™*, *Template™*, *DI-3000™*, and *ILS®*.

Graphics I/O and solid backup throughout.

Digital Engineering has built a solid foundation of "user-chosen" interactive tools for GEN.II. For instance, a crosshair cursor and light-pen port (for our optional light pen) are standard features, while optional interfaces allow you to simultaneously interact with a digitizer while outputting to an impact or non-impact serial printer and video device.

Comprehensive documentation assists at every level of operation. A worldwide distribution network assures prompt delivery and backup. And whether you tap our service network or opt for on-site service — from one of the largest field service organizations in the world — your needs will be quickly met.

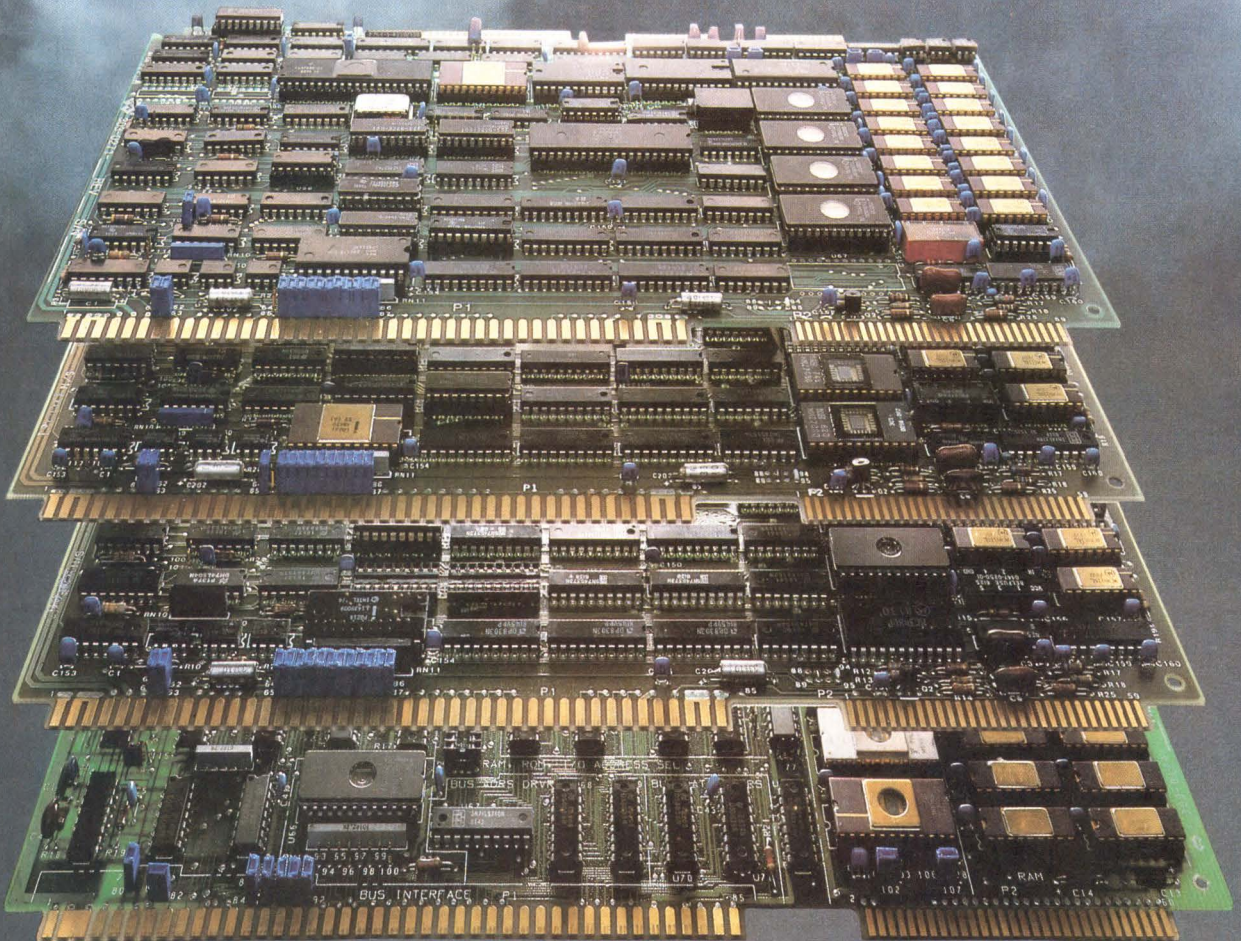
DEC's VT100, VT101™, VT102™, VT103™, VT131™, or VT132™ and Digital Engineering's GEN.II Retro-Graphics — for high-grade imaging in a low-cost graphics system.

Call us today for full details, demonstration, and the name of your local Retro-Graphics distributor — your "one-stop" source for graphics.

 **DIGITAL
ENGINEERING**

630 Bercut Drive, Sacramento, CA 95814
(916) 447-7600 Telex: 910-367-2009

MULTIBUS* PLUS PERFORMANCE DEPENDABILITY SELECTION



Single Board Computers by Monolithic Systems Corp.

Finding a single source for IEEE-796 products is often as challenging as the project you are working on. Monolithic Systems Corp. meets that challenge by providing a variety of products that satisfy your performance, quality and budgetary requirements.

Our board-level computer products offer many features: 4 MHz Z80A CPU, dual map addressing capability, 64K RAM and 32K RAM capacity, on-board floppy disk controller, serial and parallel I/O ports, APU options and a full, one-year warranty. Circle the reader service card for a free catalog detailing over 50 **Multibus PLUS** products.

MONOLITHIC SYSTEMS CORP.
84 INVERNESS CIRCLE EAST
ENGLEWOOD, COLORADO 80112
1-800-525-7661
TELEX: 45-4498

IN EUROPE:
JUSTINIANSTRASSE 22
aM MAIN 1
FRANKFURT, WEST GERMANY



...We are the source.

*Multibus is a registered trademark of Intel Corp.

THE CHIP THAT REFRESHES ITSELF

An 8k x 1 memory chip with onchip refresh and control circuitry offers designers the best aspects of both dynamic and static RAMS.

by John J. Fallin,
Joseph P. Altnether, and
William H. Righter

The ideal microprocessor memory has three major characteristics: ease of use, flexibility, and low cost. Unfortunately, all of these characteristics are seldom available in a single device. Thus, memory system design involves compromises. Matching memory component characteristics to desired design parameters rarely results in a perfect fit.

To optimize memory design, the designer must set priorities in choosing between static random access memory (SRAM) and dynamic random access memory (DRAM). Neither choice completely supplies all the beneficial characteristics. SRAMs are easy to use, but high cost, limited density, and high power consumption limit their application to under 64k bytes. DRAMs are suitable for large memory arrays (above 64k bytes) where density and low power are important. In addition, the refresh

John J. Fallin is currently an applications engineer at Intel Memory Products, 2111 NE 25th, Hillsboro, OR 97123. He is responsible for iRAM applications. Mr Fallin has a BSEE from Oregon State University.

Joseph P. Altnether is the technical marketing manager at Intel Memory Products and is involved in the technical marketing of Intel iRAMs. Mr Altnether has a BSEE from St Louis University.

William H. Righter is also an applications engineer at Intel Memory Products. He is responsible for the graphics applications of dynamic RAMS. Mr Righter is currently working on a BSEE from the University of Portland.

overhead of large memory systems is spread over a large amount of memory. Between the two extremes represented by static and dynamic RAMs, however, is a performance zone where all three ideal characteristics (low cost, flexibility, and ease of use) are required.

Low cost can be achieved with a DRAM cell. A major factor determining the cost of a memory device is the physical area occupied by the memory cell. Small cell size allows small die size, which results in more die per wafer. The net result is lower cost. DRAMs achieve lower unit costs because they use a single transistor for the memory cell. Each SRAM cell, on the other hand, requires six transistors. In addition, the DRAM cell provides the benefits of low power and high density. The remaining ideal characteristics (flexibility and ease of use) demand more innovative approaches than are presently available.

A microprocessor memory system using DRAMs consists of three major elements: microprocessor, memory, and controller. To gain ease of use, the controller must be incorporated into either the microprocessor or the memory. By including the memory control in the microprocessor, a simple memory device can be built in which the cost of the control logic is distributed over the entire memory system. Sadly, this approach has inherent faults. Because refresh is derived from microprocessor timing, any operation that suspends or stretches the timing must be carefully analyzed to ensure that it does not violate system refresh timing. Examples of such time stretching operations are extended wait states, hold operations in direct memory access, or the single-step operations important in system debugging. Moreover, placing the burden of refresh on the microprocessor can reduce processor performance by suspending operation to service memory refresh.

Another technique for refresh control is to incorporate most of the refresh mechanism on the RAM chip, leaving the most difficult portion—the arbiter—to the system designer. This type of RAM is known as a

pseudo- or quasistatic RAM. Statistical techniques or special features of a particular central processing unit (CPU) may be used to accomplish refresh, though it is not always guaranteed. The system must be thoroughly analyzed to ensure proper refresh timing.

The third memory refresh method incorporates all of the memory control logic, including arbitration logic, into the RAM chip. Thus, all DRAM cell control is contained on the same piece of silicon, creating a complete integrated memory system on a chip. This concept is called an integrated RAM (iRAM.) Combining the best features of dynamic and static RAM, the iRAM satisfies the ideal microprocessor memory requirements—a DRAM storage cell for low cost, a Joint Electron Device Engineering Council 28-pin package configuration conforming to universal flexibility standards, and ease of use because of onchip control. (See the Panel.)

Intel's 8k x 8 iRAM contains all the elements needed for complete memory control. Recognizing the need for both synchronous and asynchronous refresh, Intel offers the 2187 iRAM with synchronous refresh for special applications and the 2186 with asynchronous refresh for general purpose designs. With onchip refresh, the 2186 needs no external stimulus or control. As a result, memory is autonomous; like an SRAM it can be left alone with power applied and still retain data. Any operation that suspends or stretches the system timing has no effect on refresh operation. However, because refresh is asynchronous with the microprocessor, a memory request can occur during a refresh cycle. In this case, the iRAM signals the system microprocessor that a delay will occur in the cycle.

Device operation

The 2186/2187 performs four types of cycles: read, write, false memory, and refresh. It is important to note that chip enable (\overline{CE}) is an edge-triggered, not a level-triggered, input. On the 2186/2187, an access cycle is requested for every high to low transition of \overline{CE} . Care must be taken to ensure that a new access cycle is not requested before the previous cycle is completed. This would violate memory cycle time (TELEL) and would jeopardize data integrity. A minimum precharge (\overline{CE} high time—TEHEL) must also be guaranteed. The violation of \overline{CE} high time would most likely occur in systems where noise spikes can occur on chip enable.

Functioning like a clocked static RAM, iRAM addresses are latched off the external address bus on the falling edge of \overline{CE} . This feature is useful in many designs because it saves the designer one or two transistor-transistor logic packages. In contrast to the trailing edge write of the SRAM, the iRAM requires a leading edge write. Further, the iRAM permits three different types of access cycles. Depending on the active time of \overline{CE} and its relation to output enable (\overline{OE}) or write enable (\overline{WE}), a long mode cycle, a pulsed mode cycle, or a false memory cycle (FMC) can be performed.

A long mode cycle is similar to a fully static RAM cycle in that \overline{CE} remains valid throughout the entire cycle. In the pulsed mode cycle, the iRAM operates as a clocked static RAM and \overline{CE} is active only at the beginning of the cycle. When \overline{CE} becomes active, without an \overline{OE} or \overline{WE} , the iRAM performs an FMC and terminates on the rising

edge of \overline{CE} . This is useful during byte write operations of 16-bit microprocessors. In this case, a 16-bit word is selected (two iRAMS), and only one receives a write pulse to perform byte write. The other selected iRAM performs an FMC.

Assuming a refresh is not in progress when the cycle begins, an access cycle is initiated on the high to low transition of \overline{CE} . After activating \overline{CE} , addresses are latched from the external bus and data are presented to the bus. Data will remain at the bus as long as \overline{OE} remains active, independent of the state of \overline{CE} .

Any operation that suspends or stretches the system timing has no effect on refresh operation.

If a refresh cycle is in progress at the time \overline{CE} goes low, a deferred cycle occurs. In this case, ready (RDY) will respond by going low within a given time (TELRL) of \overline{CE} going low. After the refresh cycle and part of the access cycle complete, RDY will return to a high state. At a specified time after this (TRHQV), valid data will become available at the data input/output (I/O) outputs.

It should be noted that \overline{OE} can remain active for an unlimited period of time, and data will remain on the bus even though internal refresh cycles continue to be performed. This allows operation in systems using single-stepping hardware debug, since wait states can be inserted at will. RDY does not respond under these conditions.

For the sake of clarity, assume that a refresh cycle is not in progress at the time of \overline{CE} 's falling edge. A write cycle begins in the same way as a read cycle, with addresses latched on the falling edge of \overline{CE} . For a pulsed mode, \overline{WE} must go low within a specified time of the falling edge of \overline{CE} (TELWL). If this specification time is not met, an FMC occurs and thus, no write. For a long mode, TWLEH must be met to ensure a write given setup time before (TDVWL) and a given hold time (TWLDX) after the leading edge of \overline{WE} .

If a refresh cycle is already in progress at the onset of a write cycle, the RDY will respond at a given time (TELRL) after \overline{CE} 's falling edge. Data will still be latched into the device on the falling edge of \overline{WE} , but the actual write to the array will not occur until after the refresh cycle is completed. RDY responds during write cycles to prevent cycle timer (TELEL) violations. As in a read cycle, \overline{CE} and \overline{WE} can remain active for an indefinite period to accommodate single-step type operation. An FMC occurs when \overline{CE} becomes active but neither \overline{OE} nor \overline{WE} becomes active. An FMC is a valid mode of operation and also acts like a row address strobe (RAS) only refresh, in which the row selected by the seven external row addresses is refreshed.

Internal vs external refresh

The 2186 internal refresh is completely automatic, requiring no external stimulus; an internal timer provides refresh requests. If an access cycle is requested during a refresh cycle, the 2186 will respond by outputting a RDY low. For applications requiring maximum performance,

the 2187 allows external generation of refresh signals. A high to low transition on the refresh enable ($\overline{\text{REFEN}}$) input of the 2187 will initiate a refresh cycle. After starting a refresh cycle, one cycle time (TELEL) must be allowed before attempting another access or refresh

cycle. Deferred access cycles are not allowed on the 2187, as it has no arbitration circuitry. If $\overline{\text{REFEN}}$ is held low for at least one timer period, the internal timer will begin to time out, and the 2187 will maintain refresh with no outside intervention.

Inside the iRAM

Included in the 5-V iRAM device are a dynamic array, an arbiter, a refresh address counter, and a refresh timer along with complete control and precharge circuitry. The 2187 differs from the 2186 only in the refresh timer and arbiter control circuitry. The diagram illustrates the interrelation of these iRAM elements.

Arbiter

The arbiter that determines the priority sequence of two or more asynchronous inputs is the most significant element of the 2186 internal refresh circuitry. In the 2186, the two inputs to the arbiter are an external access cycle request and an internal refresh cycle request. When either of these requests is made, the arbiter decides whether the cycle will proceed immediately or be delayed. For example, if an access cycle is in progress at the time of an internal refresh request, the refresh cycle will be delayed until after the access cycle is completed. Conversely, if an access cycle is requested while the 2186 is performing a refresh cycle, the access cycle will be delayed. Here the 2186 will respond with a RDY low output, instructing the device that more time must be allowed. In the limit, both cycle requests can occur simultaneously. Therefore, arbitration becomes necessary along with the simple state gating as outlined.

Array

The memory array, designed with direct random access memory (DRAM) storage cells, is fabricated using an N-channel double-layer polysilicon gate process. The array features polysilicon word lines and folded metal bit lines that provide high common mode rejection.

Refresh timer

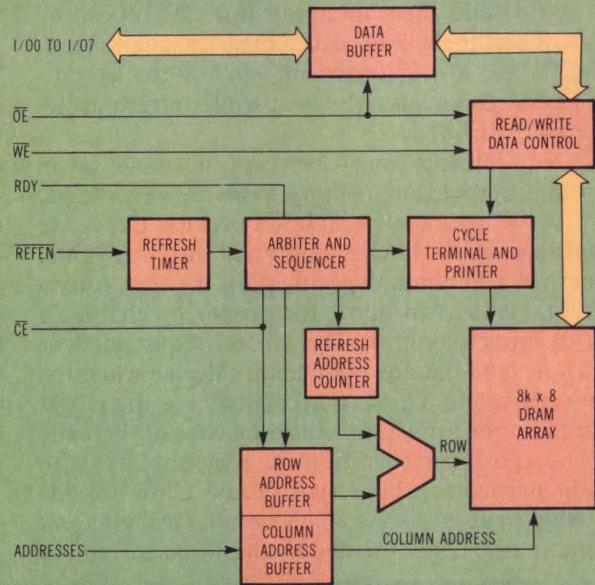
Refresh peripheral circuitry is included on the device to preserve the integrity of the data in the DRAM array. A refresh timer provides refresh cycle requests at appropriate intervals. The timer is designed to track with both process variations and temperature so as to guarantee proper refresh over all specified ranges.

Row address counter

When the internal refresh cycle is granted, refresh addresses are provided by a refresh address counter. This counter contains the 7-bit address of the next row to be refreshed and is incremented after each refresh cycle. Control logic within the peripheral circuitry handles the multiplexing of external memory addresses and refresh addresses during appropriate cycles.

Device pinout

The 2186/2187 comes in Joint Electron Device Engineering Council compatible 28-pin socket. Pin 1 (labeled "CNTRL") becomes the RDY output on the 2186, or the $\overline{\text{REFEN}}$ input on the 2187. Pin functions are described in the Table.



iRAM Pin and Signal Definitions

Pin	Description/Function
A_0 to A_{12}	Address inputs. These inputs provide the addresses needed to select one of 8192 bytes. Addresses appearing on these inputs are latched into the device on the high to low transition of $\overline{\text{CE}}$.
I/O_0 to I/O_7	Data input/output. These bidirectional pins receive data to be written to the device and output data during a read cycle.
$\overline{\text{CE}}$	Chip enable input. A high to low transition on this pin latches addresses and initiates an access cycle.
$\overline{\text{OE}}$	Output enable input. During a read cycle this input turns on the data output buffers.
$\overline{\text{WE}}$	Write enable input. Data are latched into the device on the leading (falling) edge of this signal.
$\downarrow \text{RDY}$ (2186 only)	This output becomes active to signify a delay in the cycle. It is open drain, allowing the wire ORing of several 2186 RDY outputs.
$\downarrow \overline{\text{REFEN}}$ (2187 only)	This input allows for external refresh control. A high to low transition of $\overline{\text{REFEN}}$ causes a refresh cycle to be initiated. Holding $\overline{\text{REFEN}}$ low causes asynchronous timer operation.
V_{CC}	This input supplies operating voltage to the device. V_{CC} is specified at $5 \text{ V} \pm 10\%$.
GND	Ground input for the device.

After $\overline{\text{REFEN}}$ returns high from this state, a minimum amount of time (TRFHEL) must be allowed before the next falling edge of $\overline{\text{CE}}$ or $\overline{\text{REFEN}}$ in order to complete any refresh cycles initiated by the timer. This mode of operation is called power-down refresh. The 2187 also supports a single-step mode of operation, which is accomplished by strobing $\overline{\text{REFEN}}$ low after an access cycle is started and then holding it low. $\overline{\text{REFEN}}$ can be kept low indefinitely and data integrity guaranteed. With $\overline{\text{REFEN}}$ held low, data remain valid on the I/O pins as long as $\overline{\text{OE}}$ remains active, even while refresh cycles are being performed.

Three requirements must be kept in mind when building microprocessor memory systems with iRAMs. The first is the need for a stable $\overline{\text{CE}}$ because the active low transition of $\overline{\text{CE}}$ latches addresses into the iRAM. Also, there is a minimum specification between transitions of $\overline{\text{CE}}$ (TEHEL) to allow for proper precharge of internal dynamic circuitry. The second requirement is the need for valid data at the memory device when the $\overline{\text{WE}}$ line is activated. This is a necessity since the iRAMs write data into the array on the leading edge of the write pulse. The third consideration is compatibility with SRAMs. In particular, the design should allow for the trailing edge write of SRAMs. This permits using SRAMs as second source chips, or allows the iRAM to replace

read only memory (ROM) or erasable programmable read only memory (EPROM) during system debug stages.

Following are applications that exemplify the techniques for interfacing the asynchronous 2186 and the synchronous 2187 iRAMs to various microprocessors. Although the designs can be simpler, additional circuitry is included to provide memory site compatibility with SRAMs and EPROMs.

5-MHz 8088 processor application

The first example involves a 5-MHz 8088 microprocessor configured to a bank of 2186 iRAMs. It runs in the maximum mode without wait states for normal memory access cycles, except when RDY is activated due to internal refresh. The schematic diagram is shown in Fig 1. The iRAM chip enable circuit is a simple cross-coupled latch that provides an active low enable signal ($\overline{\text{E}}$) synchronized with address latch enable (ALE). This enable signal, along with latched status bit S2, is used to enable the 74S138 address decoder to provide stable chip enable signals ($\overline{\text{CE}}_0$ to $\overline{\text{CE}}_7$) to the 2186 iRAMs. The memory write control ($\overline{\text{MWT}}_0$) output from the 8288 bus controller provides the memory write control ($\overline{\text{MWT}}_0$) output from the 8288 bus controller provides for both leading and trailing edge write conditions.

The basic operation of the $\overline{\text{CE}}$ circuit is as follows: early in the CPU cycle, ALE goes high, then low, clearing the cross-coupled latch and driving $\overline{\text{E}}$ high. $\overline{\text{E}}$ remains

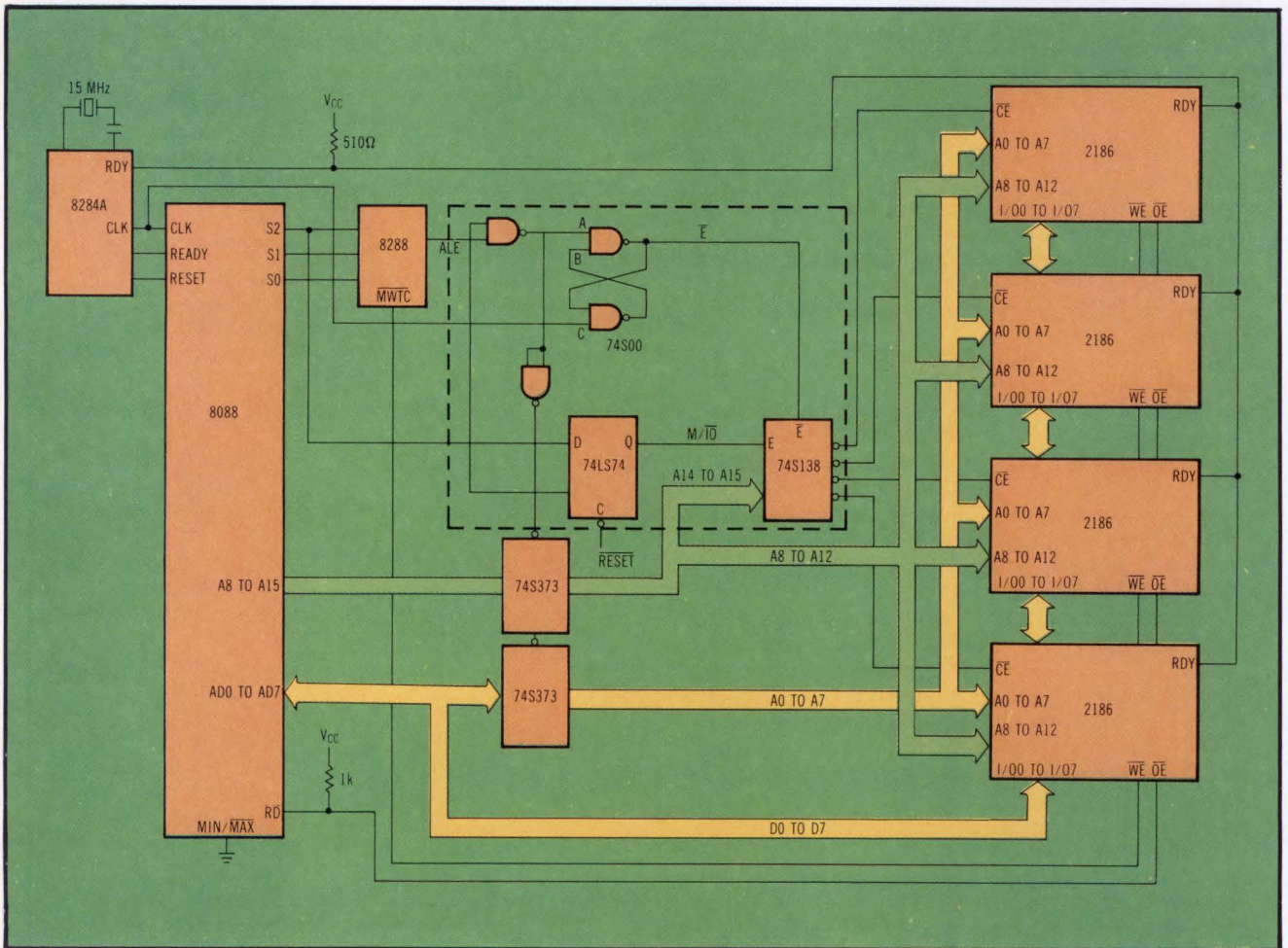
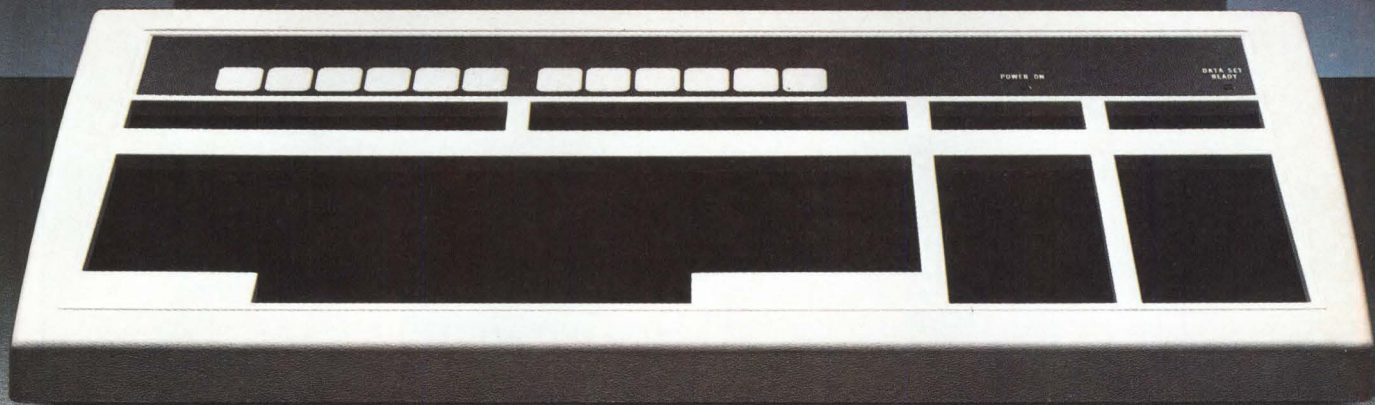


Fig 1 Schematic for iRAM use with 8088 microprocessing unit running in maximum mode. To ensure proper startup, all iRAM control inputs must be inactive for 100 μs after V_{CC} reaches spec.



Five good reasons to put a Hall effect keyboard here.

When it comes to considering a keyboard for your next terminal, there are many reasons a Hall effect keyboard may be your best choice. Here are just five.

Have it your way.

You can get Hall effect keyboards any way you like, from completely customized to standard designs available off the shelf. Or, you can buy separate keyswitch modules to build your own keyboard or modify a standard design. And you can choose from a virtually endless combination of legends, shapes and colors in sloped, stepped or sculptured versions.

Proven performance.

Consider our track record of quality and reliability. The keyswitch modules are rated at over six million hours MTBF, with a life rating of 100 million operations. Our Quality Assurance program allows us to offer a two-year warranty and 1% AQL. Right from the start our Hall effect keyboards will help you and your customers save money on repairs.

Expertise inside and out.

Ever since we introduced them in 1968, Hall effect keyboards have offered exceptional human factors and electronics. We design our keyboards to become a smooth and efficient interface between operator and machine. With true n-key rollover. And the solid state output is ideal for direct microcomputer interface. In fact, it's still the easiest and fastest to scan in the industry. No keyboard looks better, feels friendlier or is easier to work with.

Cost-effectiveness.

Due to their high performance and dependability, Hall effect keyboards will save you and your customer time and money throughout the life of your product. And you may be surprised at how competitively they're priced.

The Keyboard Consultants, of course.

We've been designing, applying and producing keyboard products for 25 years. In that time, our production facilities have grown to become the largest and most sophisticated in the industry. So we can deliver your keyboards on time, in any volume. Our direct salespeople and application engineers are eager to get involved early in your design process to come up with a cost-effective keyboard for your application.

For more information about our Hall effect keyboards or any of the other keyboards we offer, and for the location of our sales offices and authorized distributors around the world, call 815-235-6600. Or write MICRO SWITCH, The Keyboard Consultants, Freeport, IL 61032.

MICRO SWITCH
a Honeywell Division

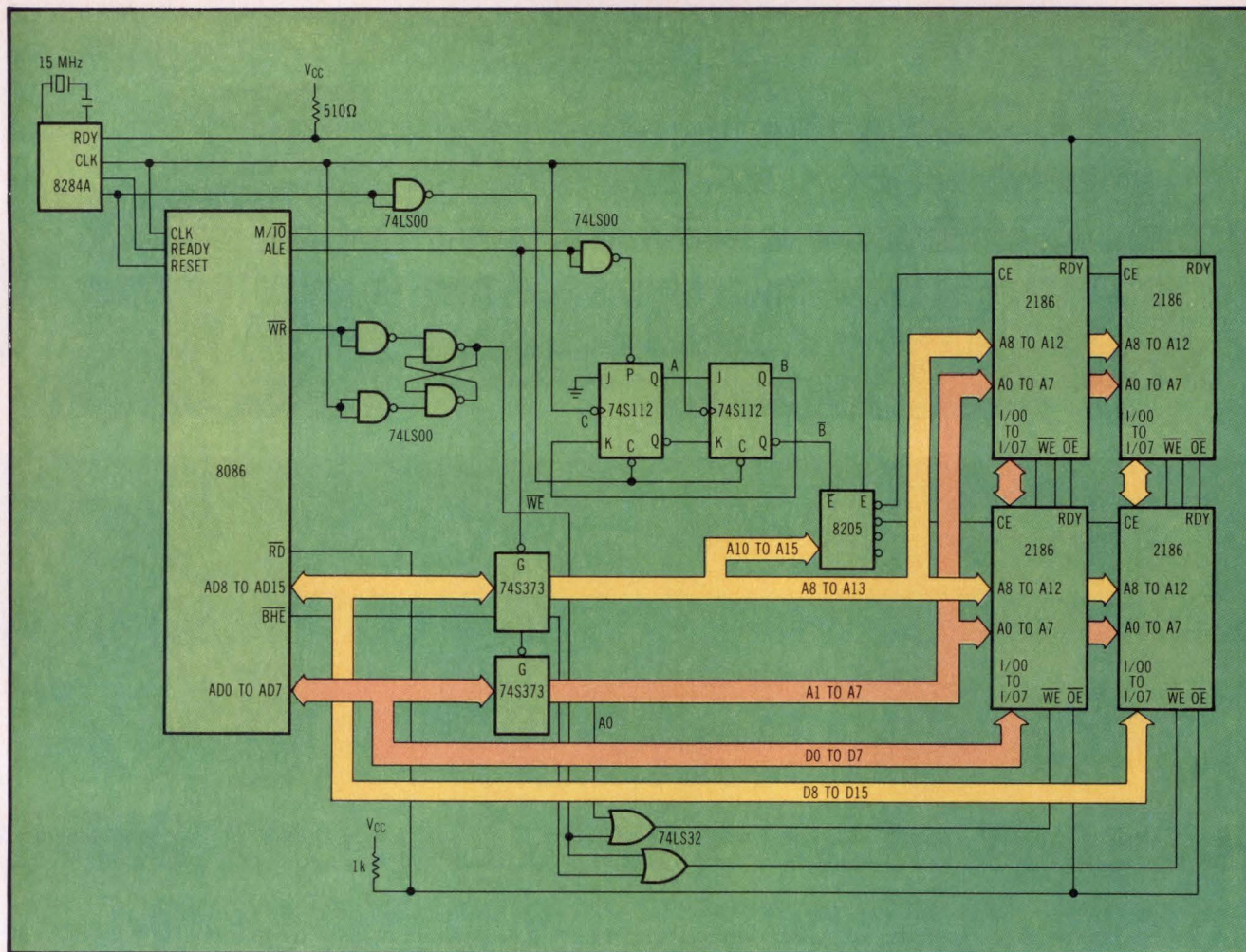


Fig 2 Schematic for iRAM use with 8086 microprocessing unit operation in minimum mode. NAND latch in processor's \overline{WR} line ensures adequate delay of data to iRAM as well as supplying trailing edge WR signal required by conventional SRAMs.

high at least as long as ALE holds the clear condition of the latch. Due to the skew of the falling edge of ALE with the system clock, two possible decoder enable timing sequences exist. The first occurs when ALE returns to a low state before the falling edge of the system clock. In this case, the latch remains cleared and \overline{E} remains high. On the falling edge of the system clock, the latch is set, driving \overline{E} low and enabling the decoder (depending on the state of S2). The other timing sequence occurs when ALE goes low after the falling edge of the system clock. In this case, when ALE goes low, the \overline{E} signal is immediately driven low as a result of the system clock (low) input on the "set" side of the latch. The memory cycle completes and early into the next cycle when ALE goes high, \overline{E} returns to a high state. This clearing action occurs independently of the state of the clock.

The net result is the enabling of the 74S138 decoder after its address inputs have stabilized. Thus, a transient-free chip enable is supplied to the iRAMs. The balance of the memory system is wired in a straightforward manner. The \overline{OE} signal for the memory array is connected directly to the read control (\overline{RD}) signal of the 8088 processor. Bidirectional data lines of the memories are connected to the processor's AD0 to AD7 lines. CPU addresses are latched by the 74S373s two gate delays after the falling edge of ALE. Although the iRAMs do not require the address latches, they are included for completeness. A

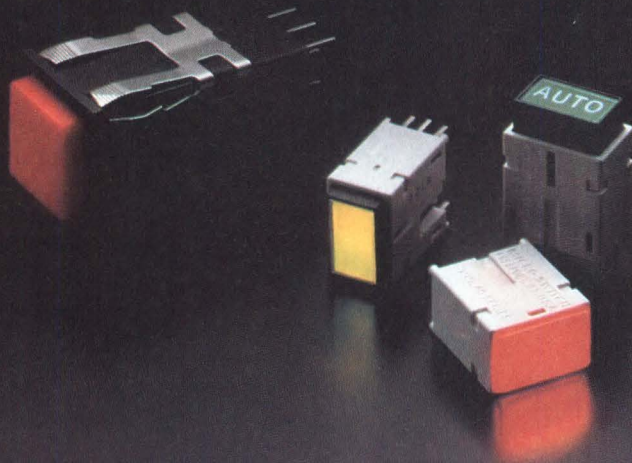
typical system needs to latch the addresses from the multiplexed bus for interfacing to SRAMs, EPROMs, and so on. The address lines feed the memory array via the 74S373 flow-through latches. All of the RDY lines of the memory array connect to a RDY input of the 8284A clock generator in an OR configuration. A 510- Ω pullup resistor is used for stability.

Note that S2 is latched into a 74LS74 flipflop on the rising edge of ALE. This is important because, during certain CPU operations such as the execution of the halt instruction, the status bits are not guaranteed to remain valid until the falling edge of ALE. To guarantee proper power-up of the 2186, all control inputs must remain inactive for 100 μ s after V_{CC} reaches specification. This is accomplished by tying RESET to the clear input of the M/IO flipflop. A pullup resistor on the \overline{OE} is also required because the RD line on the 8088 goes into a high impedance state during RESET.

iRAMs in an 8086 based system

The interface requirements for an 8086/2186 system (Fig 2) are similar to those for an 8088. The \overline{CE} generation circuitry consists of two JK flipflops, arranged as a 4-state sequencer. This sequencer makes its first transition on the rising edge of ALE, when sequencer output A is set. On the next falling edge of the system clock, sequencer output B is set, enabling the 8205 decoder if the cycle is a

Finally, a pushbutton for those who like everything about our AML. Except its size.



The Advanced Manual Line—AML—was introduced in 1975. It continues to set standards for panel design flexibility and harmonious appearance. Now, the same standards have been applied to our new Miniature Manual Line—MML. With all the features you've liked in AML, including high quality and ergonomic excellence.

Our new miniature pushbuttons and indicators measure a mere 10 x 15 mm on the panel, with a housing only 17 mm deep. So they take up less space, on both sides of the panel. Their ergonomic design includes full-face LED illumination. A feature no other miniature pushbutton has. And they feel good when you use them. Smooth operation. Solid feel. And tactile feedback for better operator/machine interface.

Because there are many electrical and circuitry options, you can satisfy a wide range of functional needs, yet maintain a consistent appearance on the panel. Choose from 1 or 2 pole circuitry, momentary or alternate action, gold or silver contacts, and electrical ratings from 1 to 6 amps. (Our 6 amp power-duty pushbutton is the smallest of its kind.) And our MML is designed to meet UL, CSA and other international standards.

MML offers some special features that help lower your installation costs. Like a unique housing design that accommodates cleaning before and after wave soldering and single-level printed wiring board termination in standard configurations.

MML joins the broadest selection of manual controls anywhere. And, it will continue to grow as we expand our Miniature Manual Line. Like our trusted AML, our new miniature pushbuttons and indicators will provide you with a variety of high quality controls you can depend on.

For more information on our new MML, and the location of our sales offices around the world, call 815-235-6600. Or write MICRO SWITCH, Freeport, IL 61032.

MICRO SWITCH
a Honeywell Division

memory access (\overline{M}/IO also gates the decoder). After one more clock cycle, output A is reset, causing output B to be reset on the fourth clock cycle. When output B is reset, the \overline{CE} decoder is disabled, causing the \overline{CE} to the 2186 to return to a high state. With this arrangement, \overline{CE} is low for only two processor T states, allowing a \overline{CE} high time of at least two T states. This relatively long deselect time is important in 16-bit systems where a 2186 could receive a \overline{CE} but no \overline{OE} or \overline{WE} . This preceding condition would cause a false memory cycle to occur, in which case an extended \overline{CE} high time is required because TE_{HELP} is greater than TE_{HEL} .

For an 8086 operating in minimum mode, data output during a write cycle is not guaranteed to be valid at the falling edge of \overline{WR} . To satisfy the leading edge write requirement of the 2186, the leading edge of \overline{WR} needs to be delayed until data out is valid. This can easily be accomplished through the use of a cross-coupled NAND latch, which also provides the trailing edge write needed for SRAMs. This delayed \overline{WE} is then steered to either one or both devices in the 16-bit word by ORing \overline{WE} with either A0 or bus high enable (\overline{BHE}). This allows for either word or byte writes. If wait states are needed, the RDY outputs of the 2186 can be routed back to the RDY input of the 8284A clock chip. Because the RDY outputs are open drain, a 510- Ω pullup resistor is required.

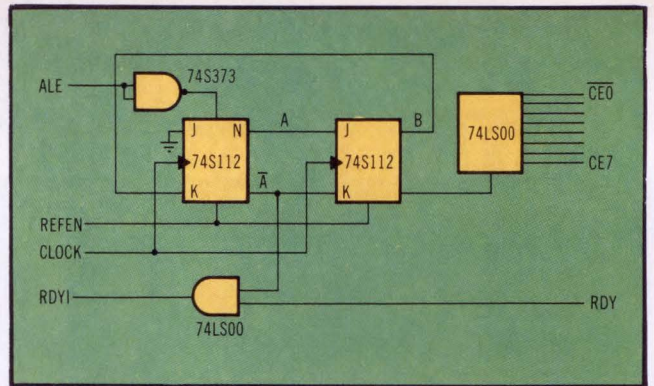


Fig 3 Additional circuitry required for 10-MHz 8086 microprocessing unit/iRAM operation with one wait state.

By adding a single AND gate to the 8086 interface (Fig 3) 2186 can be run in one wait state 10-MHz 8086 system. Upon going high, ALE causes the flipflop driving A to be set, forcing \overline{A} low. After a 1-gate delay, RDY1 is asserted. On the next falling edge of clock after ALE goes high, the flipflop driving A can now be reset on the next falling edge of clock, which occurs at the end of T2.

This arrangement ensures that RDY1 will remain low for the time frame required to insert at least one wait state. If the 2186 responds to this access with a RDY low

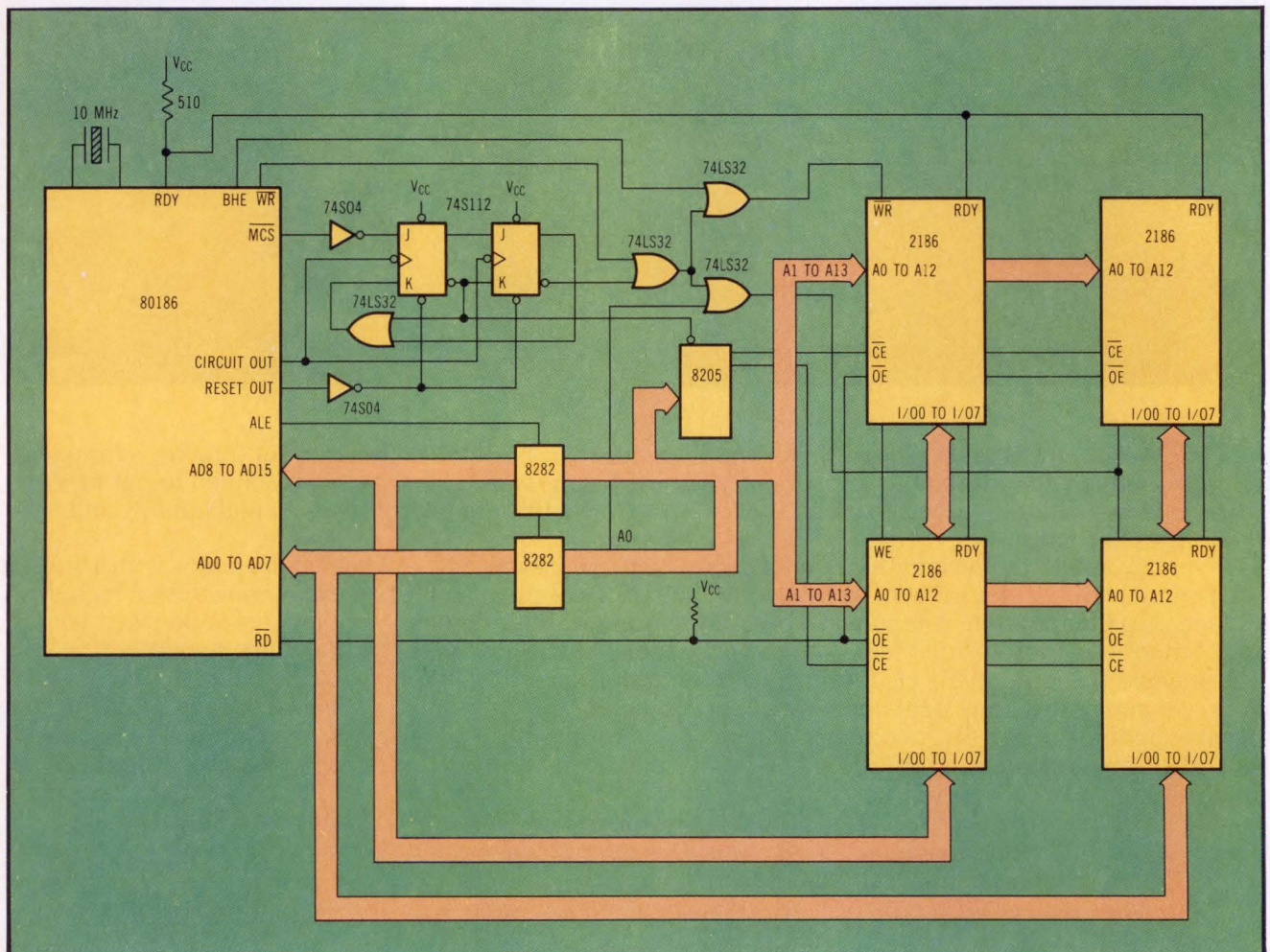
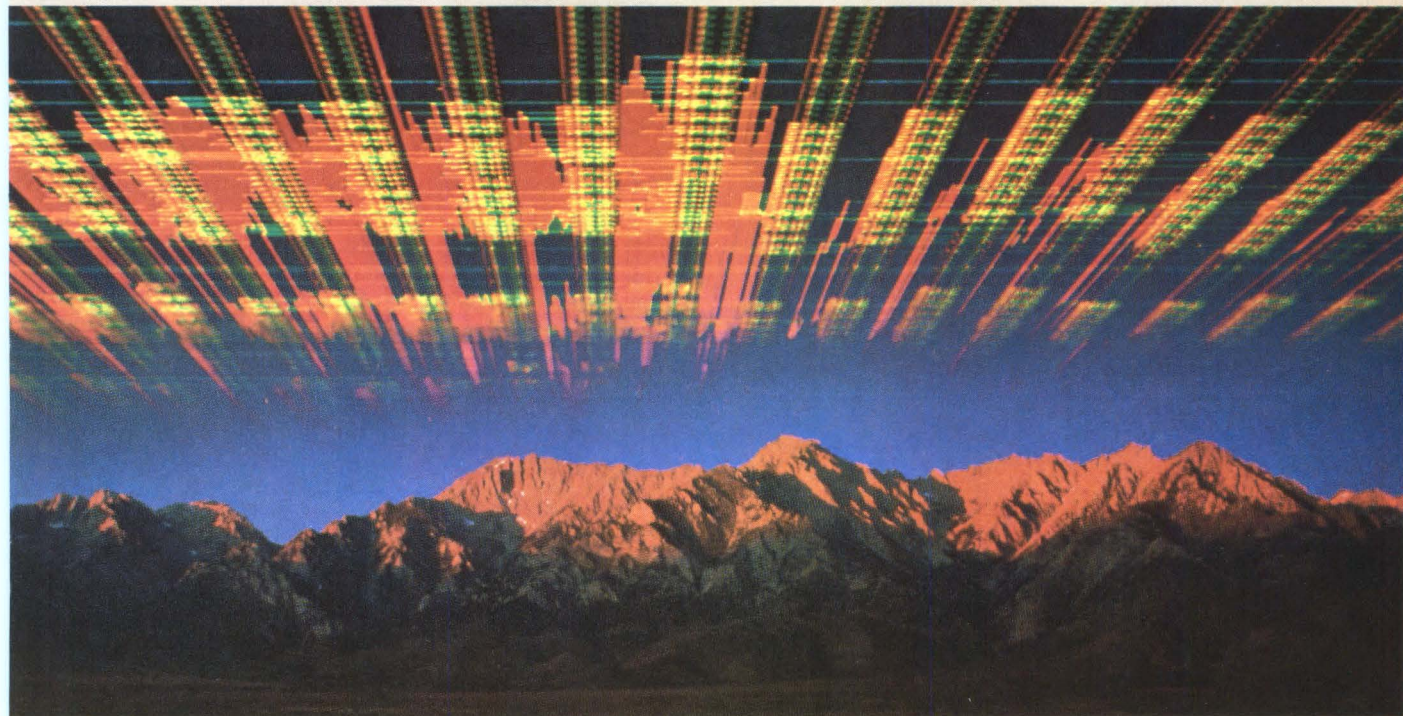


Fig 4 Interface circuitry required for iRAM operation with 5-MHz 80186 microprocessing unit. This system, based on popular iAPX 86 family of components, provides users with programmable memory chip selects for blocked memory applications.

**8,000-gate,
si-gate CMOS at 2.5 ns.
2,000-gate STTL at sub-1 ns.
400-gate ECL at 400 ps.**



At Fujitsu Microelectronics, nowhere else.

We've designed and produced gate array devices since 1974 — most of them so far ahead of their time in performance, the rest of the industry still hasn't caught up. Our current devices are no exception.

One reason for our strong lead is our exclusive CMOS double-level metallization technique. It solves the biggest problem in achieving good gate array performance — interconnection.

Interconnecting the thousands of logic cells in a gate array with one level of metal — as other manufacturers do — requires connections which are either very roundabout, or which pass through the silicon itself. Both these approaches create problems.

Roundabout interconnection paths slow the device because of their excessive length. Density suffers as well, because so many paths must run around the active area of the chip.

Silicon interconnections also slow the device, because silicon doesn't conduct as well as metal (or as predictably). In addition, the required metal-to-silicon contacts have well-known yield and reliability problems.

These problems don't exist for our gate arrays. Rather than having to go *around* one another, our interconnect paths can go *over* one another, so the paths are much shorter. This means greater speed, higher density, and improved reliability for you.

Advances like double-level metallization put our gate arrays years ahead in performance. When you add it all up, what better edge can you give to your product? Find out more. Contact your Fujitsu Microelectronics sales office listed below.

FUJITSU MICROELECTRONICS

FUJITSU MICROELECTRONICS SALES OFFICES:
Boston 617/964-7080; Chicago 312/934-6400;
Dallas 214/669-1616; New York 516/273-6660;
Northern California 408/866-5600;
Southern California 714/547-9525.
Design Centers in Boston; Dallas;
and Santa Clara, California.

**Creating New Horizons...
in Large Scale Logic.**

condition, the trailing edge of RDYI will be pushed out to insert more wait states as needed. The number of wait states that can be inserted will never exceed six—assuming a maximum RDY low time of 575 ns.

Fig 4 shows the circuitry required to interface the 2186 with Intel's 80186 high integration 16-bit processor. The 80186 is an integration of 10 common iAPX 86 components, including an enhanced 8086-2 CPU, a clock generator, a local bus controller, and an interrupt controller. The clock speed of this configuration is 5 MHz. The 80186's bus structure is much like that of the 8086, but there are some useful additions, including programmable memory chip select (MCS) outputs. These outputs can be programmed to become active for a user-selected block of memory. In Fig 4, one of four available mid-range MCSs would be programmed to become active in the memory space allocated to the iRAM. This MCS signal is then used to initiate a count sequence with the two JK flipflops. The two flipflops' outputs provide both the \overline{CE} and the properly positioned \overline{WE} (for leading edge writes) to the iRAMs.

FMCs, in which the iRAM receives a \overline{CE} but no \overline{OE} or \overline{WE} , will occur any time a single byte write occurs. If this is the case, the \overline{CE} high time requirement becomes somewhat longer than that required for a read or write cycle. The \overline{CE} circuitry used was selected with this consideration in mind because of the long \overline{CE} high time it guarantees.

Synchronous iRAMs in an 8088 system

One way to create a synchronous design using the 8088, operating in maximum mode with the 2187 iRAM, is to use a status decoder to generate a refresh signal during an opcode fetch cycle. The following example assumes that the 2187 iRAM is used for data store only, so that the iRAM can be sent a refresh strobe during the time the 8088 is executing an instruction fetch from some other portion of memory (ie, EPROM, ROM). It also assumes that opcode fetches occur often enough to meet the 128 refreshes/2-ms refresh specification.

In the circuit shown in Fig 5, it is evident that the 2187 and the 8088 are interconnected with a minimal amount

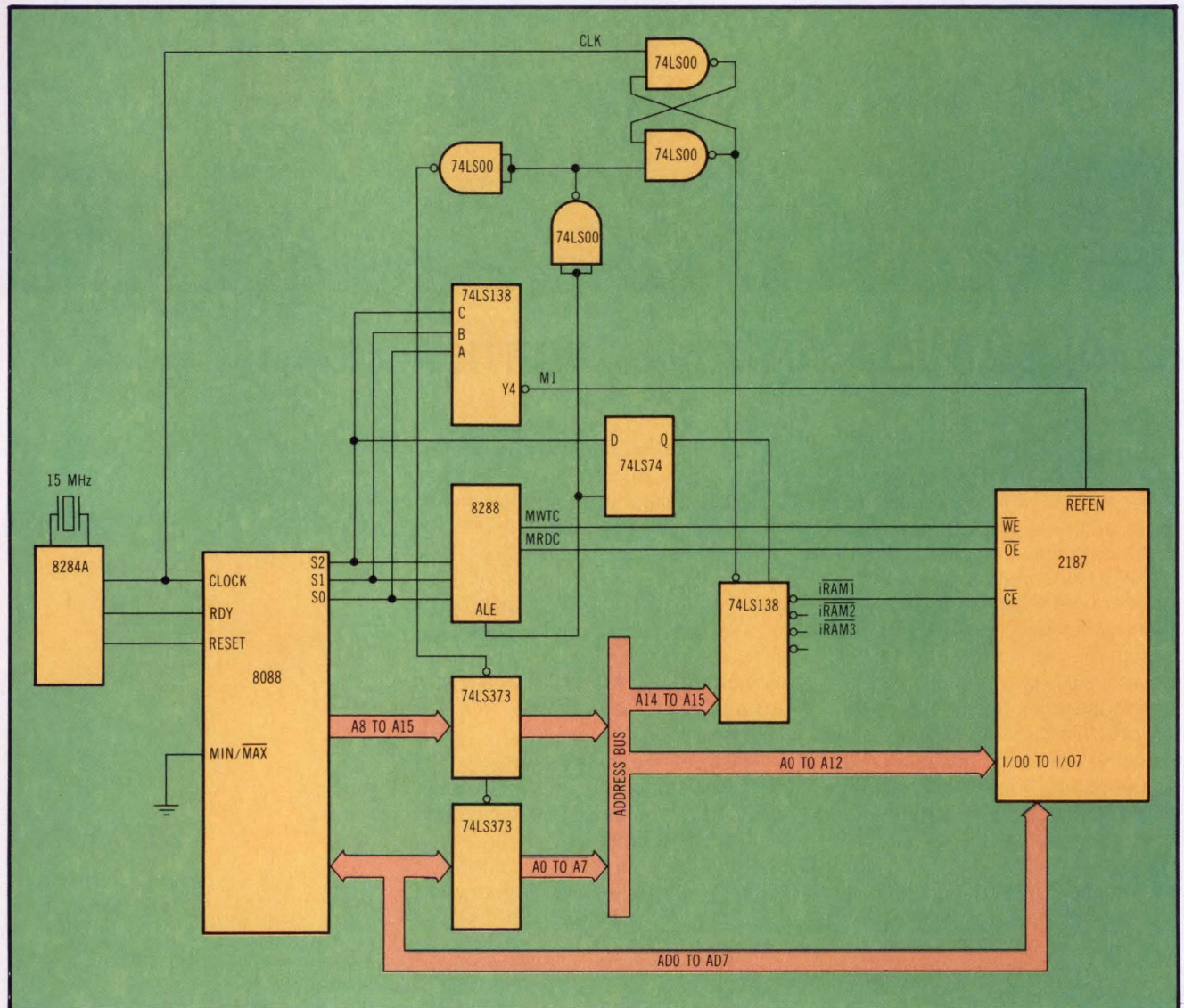


Fig 5 System diagram of 2187/8088 synchronous system. iRAM refresh occurs during 8088 instruction fetch cycle and is generated by external status decoder. Minimal transistor-transistor logic interface circuitry is required.

μ MAC-4000 is the complete, low-cost measurement and control system that's optimized for harsh industrial environments.

A fully integrated, pre-calibrated, intelligent system, μ MAC is designed to interface real world signals to any computer. Its unique single board design makes it the most cost-effective solution for small channel clusters, yet with its family of economical analog and digital I/O boards, it's versatile enough to expand for any growing needs.

μ MAC is optimized for the highest performance in harsh environments, bringing crucial measurement and control to exactly where it's needed—locally or miles from your host computer.

Standard RS-232C/20mA communication makes interfacing to any computer fast and simple. And with on-board intelligence, μ MAC not only unburdens the host CPU, but through a powerful command set and available

software packages (including DEC's RSX-11, HP-85, APPLE II and IBM), it makes implementation easy and user software development minimal.

μ MAC gives you features unequaled in low-cost measurement and control. All the signal conditioning is done for you, and with mix and match capabilities you are provided with direct connection to a wide variety of sensor inputs including thermocouples, RTDs, strain gages and 4-20mA. High noise rejection and $\pm 1000V$ isolation assure signal integrity, and with vital bumpless transfer and increment/decrement you maintain precise control in computer or manual modes.

▶ ANALOG DEVICES

For the complete details on what makes μ MAC-4000 your complete measurement and control solution, simply fill out and mail this coupon to Analog Devices, Box 280, Norwood, MA 02062, or call John Mills at (617) 329-4700.

Name

Title

Company Name

Phone

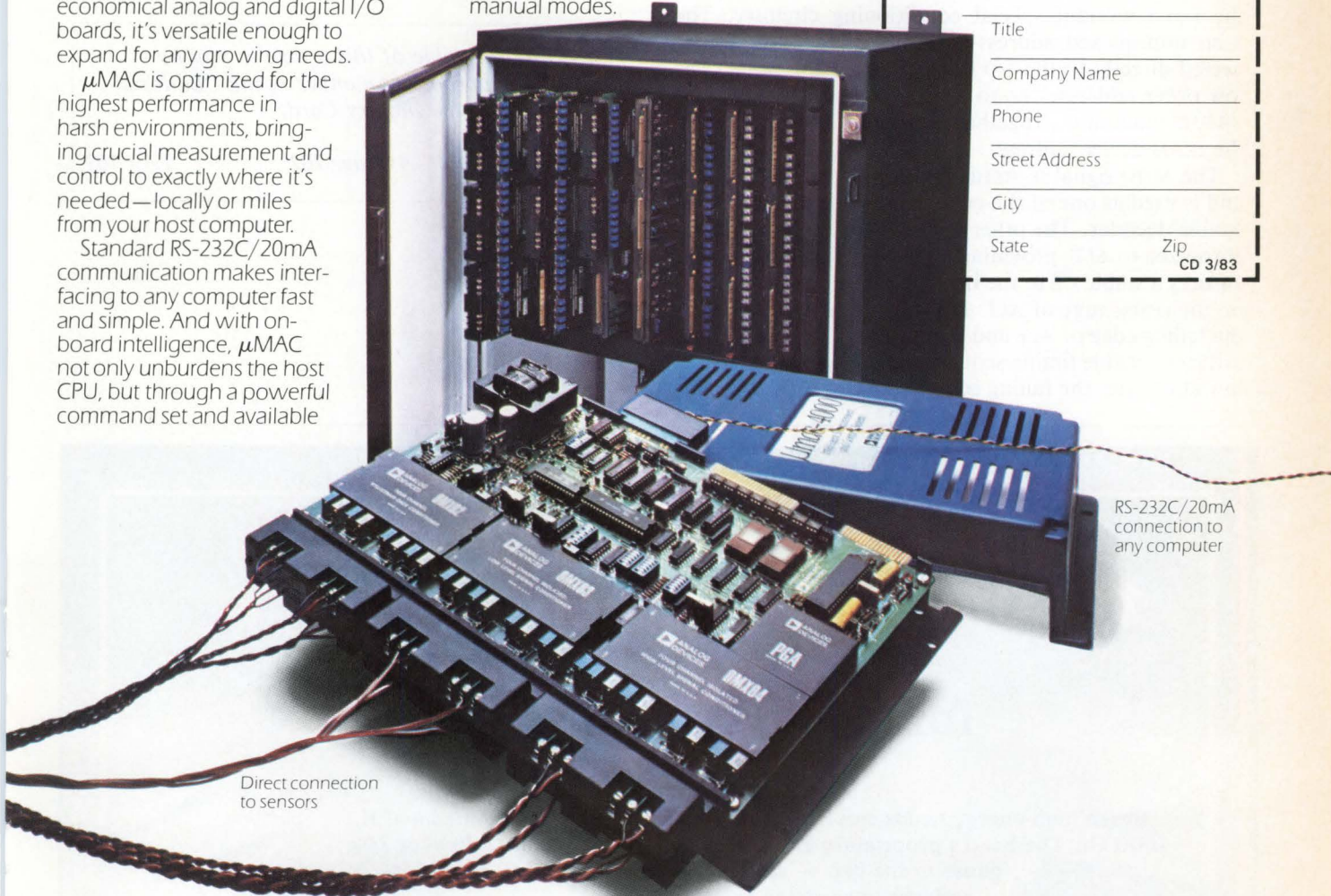
Street Address

City

State

Zip

CD 3/83



Direct connection to sensors

RS-232C/20mA connection to any computer

For any computer, this industrial sensor I/O is better across the board.

Analog Devices, Inc., One Technology Way, Norwood, MA 02062, Headquarters: (617) 329-4700. California: (714) 842-1717, (408) 947-0633. Illinois: (312) 653-5000. Michigan: (313) 644-1866. New Jersey: (201) 967-1126. Ohio: (614) 764-8870. (216) 531-9455. Pennsylvania: (215) 643-7790. Texas: (214) 231-5094, (713) 664-5866. Washington: (206) 251-9550. Belgium: 031/37 48 03. Denmark: 02/84 58 00. France: 01/687 34 11. Holland: 016/20 51080. Israel: 052/28995. Italy: 02/68 98 045. Japan: 03/263 6826. Sweden: 08/282740. Switzerland: 022/31 57 60. United Kingdom: 01/941 0466. West Germany: 089/514010.

Combining memory and control together on a single piece of silicon... satisfies all the requirements for microprocessor memory.

of transistor-transistor logic interface circuitry. The decoded 8088 signal M1 is connected to the $\overline{\text{REFEN}}$ input of the iRAM. This connection generates a refresh strobe to the 2187 every time the 8088 performs an opcode fetch. The 8288 bus controller generates memory read commands and memory write commands that are properly timed for all memory requirements. Thus, these signals may connect directly to the $\overline{\text{WE}}$ and $\overline{\text{OE}}$ control lines of the iRAM without special conditioning circuitry. The 8-bit multiplexed address-data bus of the 8088 is connected directly to the I/O 0 to 7 lines of the iRAM. The low order addresses A0 to A7 are latched by ALE at the 74LS373 latch and, together with lines A8 to A12, form the iRAM device address.

The M/IO signal is status bit S2. It is latched by ALE and is used as one of the enable inputs to the iRAM chip enable decoder. The other decoder enable input is synchronized to ALE, providing a properly timed signal that ensures a stable $\overline{\text{CE}}$ to the iRAM. The decoder is disabled on the rising edge of ALE. However, due to the skew of the falling edge of ALE and the system clock, two slightly different enable timing sequences can occur. If ALE goes low at or after the falling edge of the clock, the $\overline{\text{E}}$ enable

line is immediately activated and enables the decoder. Note that when RESET is low, REFEN will be forced low. This guarantees proper 2187 power-up. This circuit runs at 5 MHz without wait states.

Combining memory and control together on a single piece of silicon, the iRAM satisfies all the requirements for microprocessor memory. Its ease of use, flexibility, and low cost make it an attractive memory alternative. By using it in some of the applications demonstrated, engineers will find that the iRAM can help them meet the majority of both present and future memory system design needs.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 701

Average 702

Low 703

high-energy recording heads

for high H_c mag-stripes

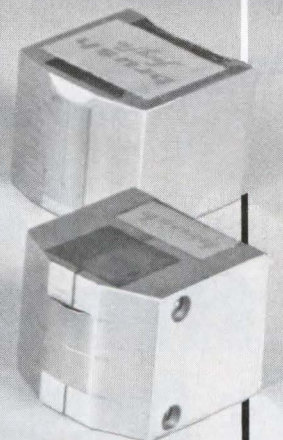
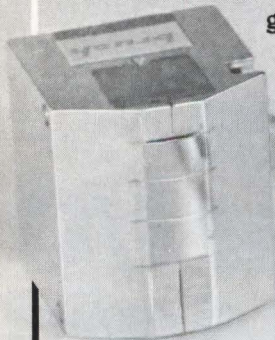
Brush high-energy heads can fully saturate magnetic recording media of H_c 4000 Oe. The head's proprietary HSI core material will sustain a field of 20k gauss in the gap — suitable for erase-resistant, alteration-resistant mag-stripe encoding.

HSI heads are available in any track configuration, including ABA, IATA, and THRIFT. Track widths to .375".

Brush high-energy heads are in production now. Immediate delivery on standard models, prototypes within 30 days.

Brush also has other high technology core materials for extended life applications on conventional stripes.

Call or write for more details.



brush[®] magnetic heads

3rd & Reagan Sts., P.O. Box 638, Sunbury, PA 17801

Phone 717/286-5611 • TWX 510-655-0222

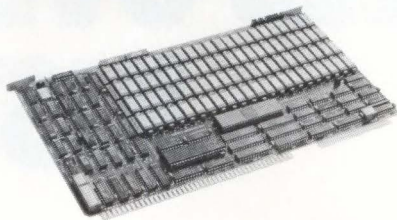
MULTIBUS* MEMORIES

DYNAMIC RAM (IEEE P796-COMPATIBLE)

NEW

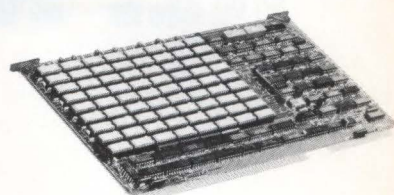
MM-8086E

- 512K, 256K bytes
- Error detection and correction
- 1000_H boundaries/16 Mbyte address
- Access/Cycle: 300/500 nsec
- CSR/ESR for EDC control and LED error correction indication
- Battery backup option



MM-8086D

- 512K, 256K, 128K, 64K bytes
- For 8 and 16-bit processors
- 1000_H boundaries/16 Mbyte address
- Even parity with output selectable to any of bus interrupts
- ACCESS/Cycle: 250/400 nsec

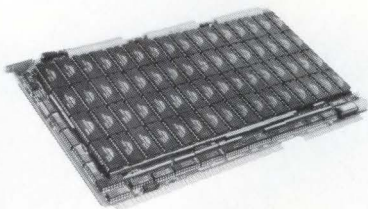


NON-VOLATILE CMOS RAM (IEEE P796-COMPATIBLE)

NEW

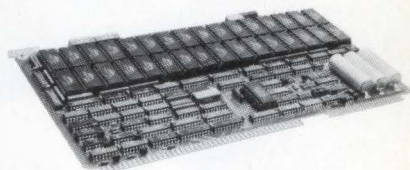
MM-8000C

- 128K, 64K bytes
- Data retention (on-board batt.):
2 weeks rechargeable batteries
- 4000_H boundaries/16 Mbyte address
- Access/Cycle: 220/220 nsec
- Battery status line allows monitored battery condition
- Redundant batteries provide improved reliability
- Accommodates 2716 EROM



MM-8086C

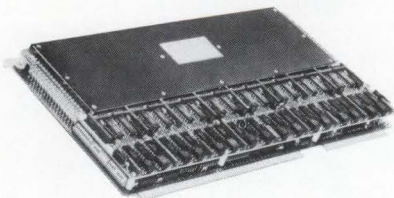
- 64K, 32K, 16K bytes
- Data retention (on-board batt.):
3 weeks rechargeable batteries
2 yrs. non-rechargeable batteries
- 1000_H boundaries/16 Mbyte address
- On-board calendar/clock
- Access/Cycle: 250/250 nsec
- Redundant batteries provide improved reliability
- Accommodates 2716 EROM



NON-VOLATILE CORE MEMORY

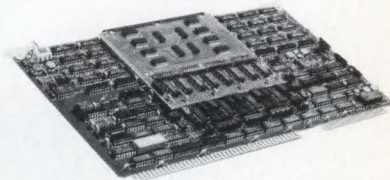
MM-8086

- 32K bytes
- For 8 and 16-bit processors
- 1000_H boundaries/1 Mbyte address
- Access/Cycle: 375/1200 nsec
- Power monitoring for data protection



MM-8086/16

- 16K bytes
- For 8 and 16-bit processors
- 4000_H boundaries/1 Mbyte address
- Access/Cycle: 280/800 nsec
- Power monitoring for data protection



ONE YEAR WARRANTY ON PARTS AND LABOR

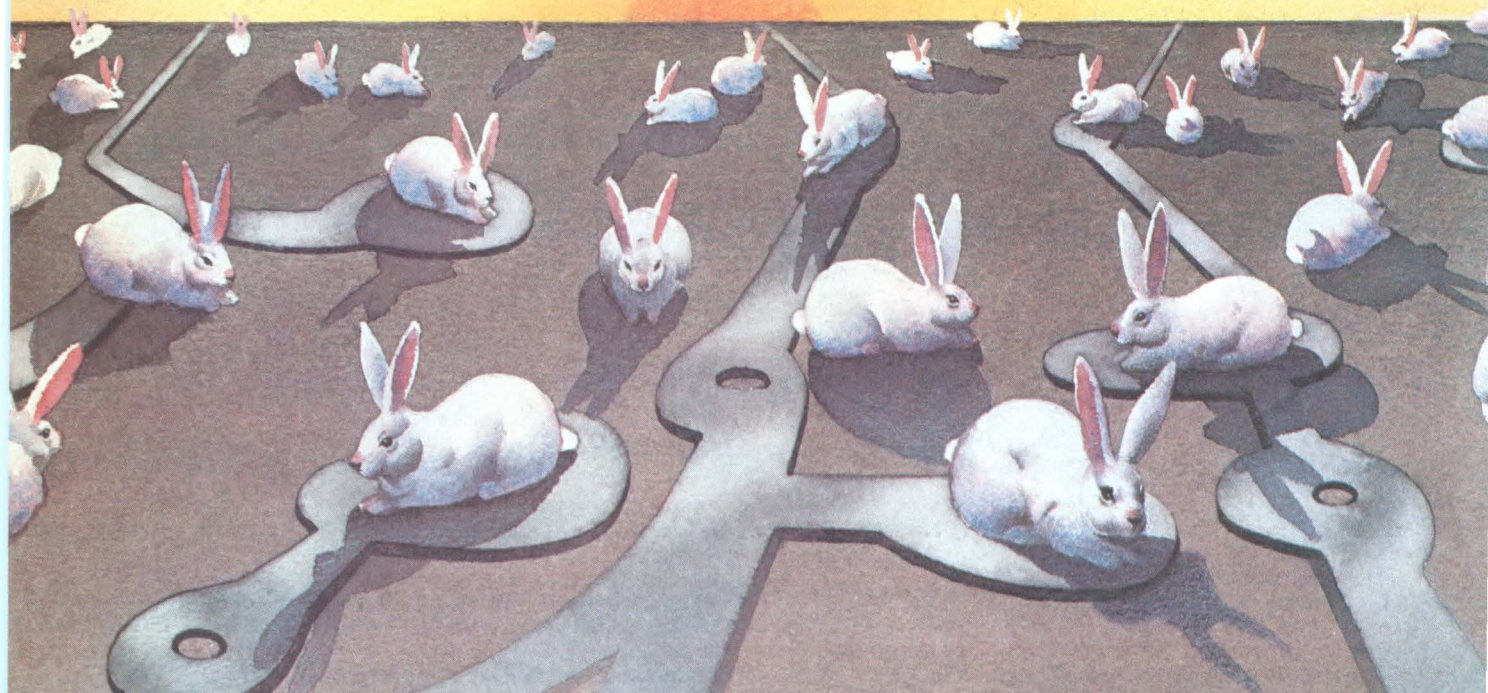
ALL BOARDS TEMPERATURE-CYCLED AND BURNED-IN DURING MEMORY DIAGNOSTICS

**micro
memory
inc**

9436 Irondale Ave.
Chatsworth, CA 91311
Phone: (213) 998-0070

*Trademark of Intel Corp.

TOSHIBA'S SILICON REPRODUCES OVER 2,000,000 JUST FOR



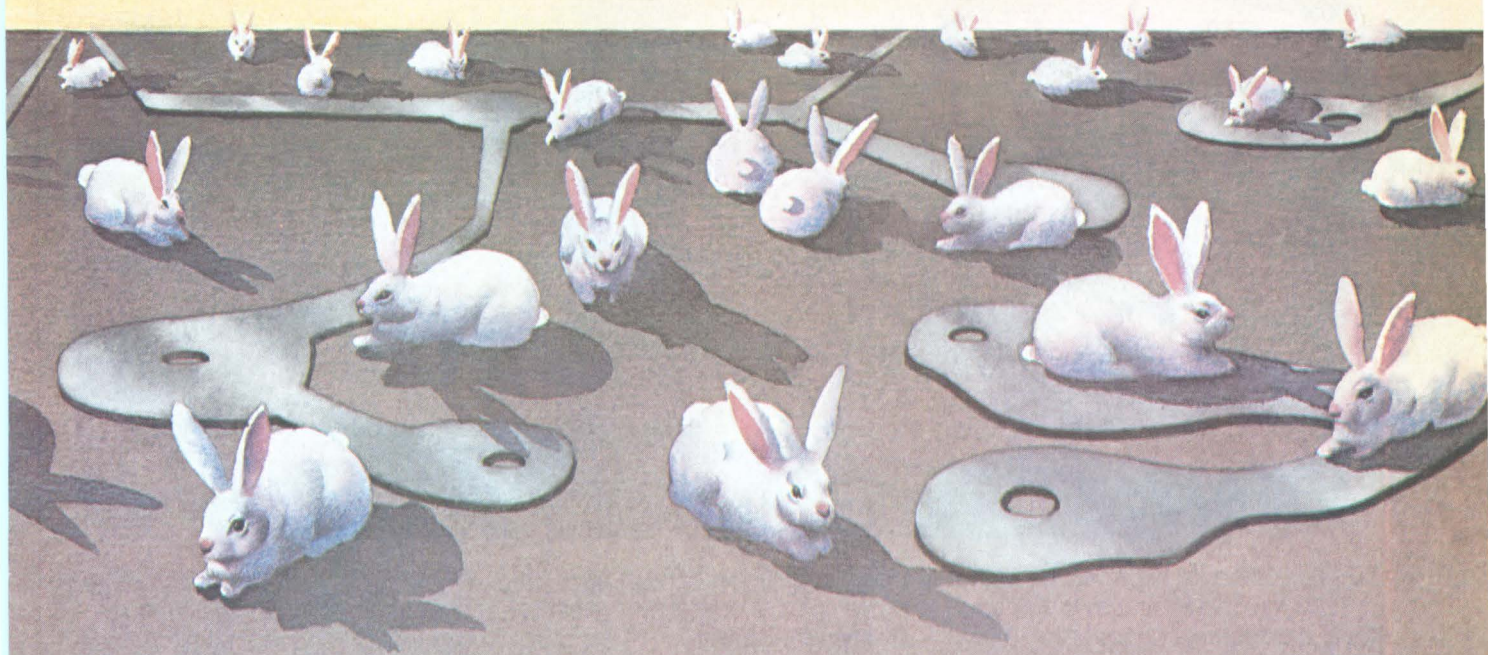
Toshiba's Sunnyvale, California plant which opened over two years ago is fine-tuned and fully operational. For starters, the 2,000,000 plus ROMs per month being produced, include 16K, 32K, and 64K. Also, at another of our facilities, we're producing the 256K ROM.

16K The 16K is organized as a 2K x 8 and is pin compatible with the 2716 EPROM.

32K The 32Ks are 4K x 8. They are pin compatible with either 2732 or 4732 type EPROMs.

64K Our 64Ks are 8K x 8s. They're available in either a 24 pin package or a 28 pin compatible with 2764 type EPROMs. Optional features include

VALLEY PLANT 100,000 ROMs A MONTH. A START.



output enable control, up to three program-
mable chip select inputs and access time to
200 ns. Operating current is 40 mA maximum
with 15 mA standby maximum.

256K Our 256K is a
32K x 8 and
is available

in the standard 28 pin package. It has fast
access time of 150 ns. Standby mode cuts
current down to 10 mA maximum.

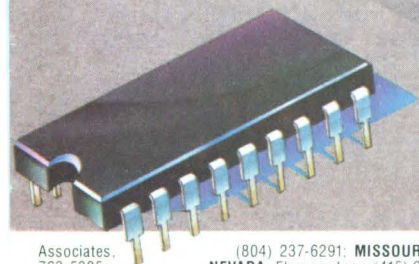
What's also cut down to common sense
levels is our lead times, so, delivery's a snap.
And the code logistics are quickly and easily
handled.

If you would like a copy of our MOS
Memory Products Data Book, lead times, or
data sheets, write Toshiba America, Inc.,
2441 Michelle Drive, Tustin, California
92680, (714) 730-5000 or call your local sales
representative.

And we'll get you started.

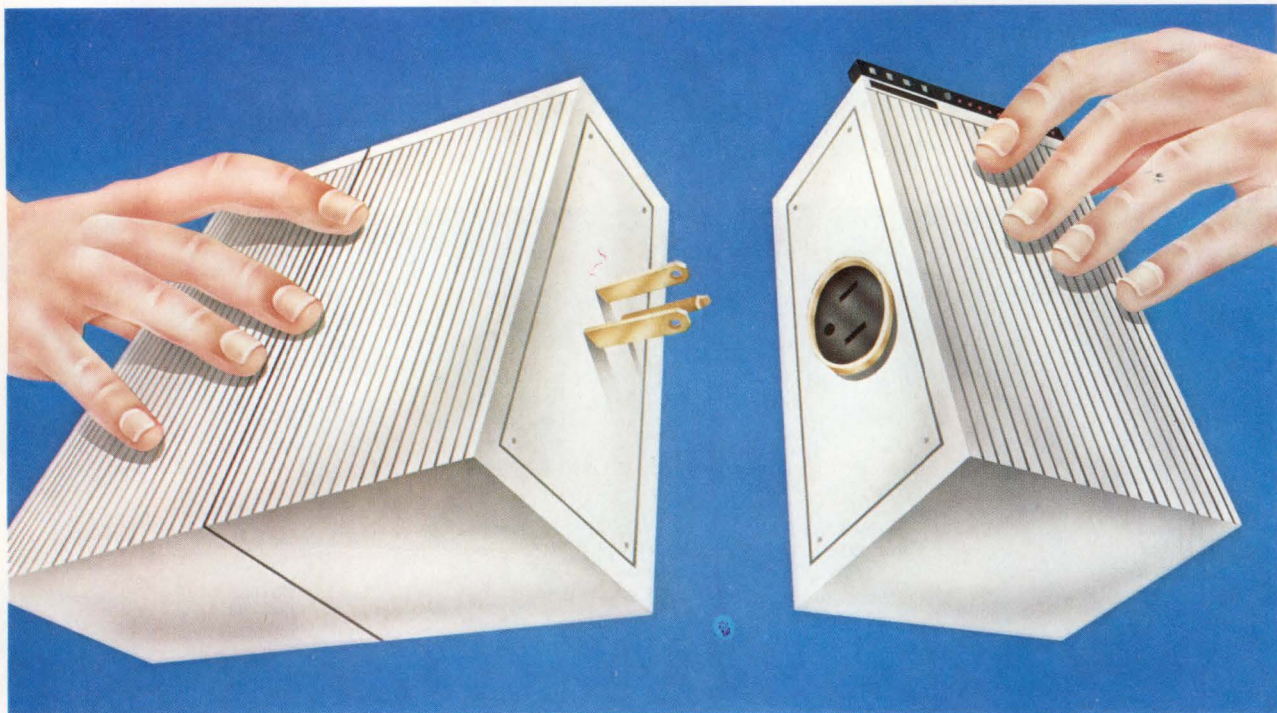
TOSHIBA AMERICA, INC.

A WORLD STANDARD IN MOS.



Associates. (804) 237-6291; **MISSOURI**, R.R. Burton & Associates, (816) 763-5385; **MONTANA**, Components West, (206) 271-5252; **NEBRASKA**, R.R. Burton & Associates, (816) 763-5385; **NEVADA**, Elrepro, Inc., (415) 962-0660; **NEW JERSEY**, Necco 1, (201) 461-2789, Vantage Sales, (609) 663-6660; **NEW MEXICO**, Semper Fi Sales Company, (602) 991-4601; **NEW YORK**, Necco 1, (201) 461-2789, Pi-tronics, (315) 455-7346; **NORTH/SOUTH CAROLINA**, Glen White Associates, (919) 787-7016, (919) 787-7023; **NORTH/SOUTH DAKOTA**, Quantum Sales, Inc., (612) 884-4700; **OHIO**, Makin & Associates, Inc., (513) 871-2424; **OKLAHOMA**, Engineering Sales Company, (918) 493-1927, Technology Sales Company, (214) 380-0200; **OREGON**, Components West, (503) 643-5588; **PENNSYLVANIA**, Vantage Sales, (609) 663-6660; **TENNESSEE**, Glen White Associates, (615) 477-8850; **TEXAS**, Technology Sales Company, (214) 380-0200, (512) 476-9874; **UTAH**, Duffy Associates, (303) 595-4244; **VIRGINIA/WEST VIRGINIA**, Glen White Associates, (804) 237-6291, (804) 295-0435, (804) 224-7764, (804) 224-0404; **WASHINGTON**, Components West, (206) 271-5252; **WISCONSIN**, L-TEC, (414) 774-1000; **WYOMING**, Duffy Associates, (303) 595-4244; **CANADA**, Source Electronics, Ltd., (416) 675-6235.

At last, plug-in parallel processing in a 32-bit supermini system.



Perkin-Elmer announces the Model 3200 Multiple Processing System, an exciting new concept for demanding real-time applications.

Room to grow

The Model 3200MPS gives you extraordinary system expandability. You can start with a host CPU and one auxiliary processing unit (APU). Then as your needs grow you can plug in more performance by adding as many as eight additional APUs.

Should you need even more horsepower, plug-in parallel processing lets you add exactly what you need as you need it—from a single APU to a whole fleet of multiple processing systems.

And no matter what the size of your configuration, a central point of control and management is pro-

vided by a single copy of our field-proven OS/32 operating system.

Design flexibility

With parallel-processing APUs you can take advantage of application segmentation and structured programming techniques to speed system development. You can segment your application into multiple task modules, with each APU performing a set of related functions. To further optimize system performance, you can easily re-allocate tasks among the APUs.

Your Model 3200MPS provides maximum flexibility for software development, reliability, and system maintenance. To incorporate new design changes or correct problem modules, simply work on the problem module while your system continues to operate. And the

Model 3200MPS can be structured to permit continued system operation though one or multiple APUs may fail. When so structured, the APUs can receive immediate maintenance attention while the system continues to run or they can wait for routine scheduled maintenance.

And our state-of-the-art universally optimizing FORTRAN VIIZ enables you to use modular programming techniques without sacrificing real-time efficiencies.

To find out more about how you can plug into all the advantages of plug-in parallel processing minis, mail the coupon or call today: The Perkin-Elmer Corporation, Two Crescent Place, Oceanport, NJ 07757.

Tel: 800-631-2154. In NJ, 201-870-4712.

PERKIN-ELMER

CRUNCH BCD NUMBERS WITH BIT-SLICE CHIPS

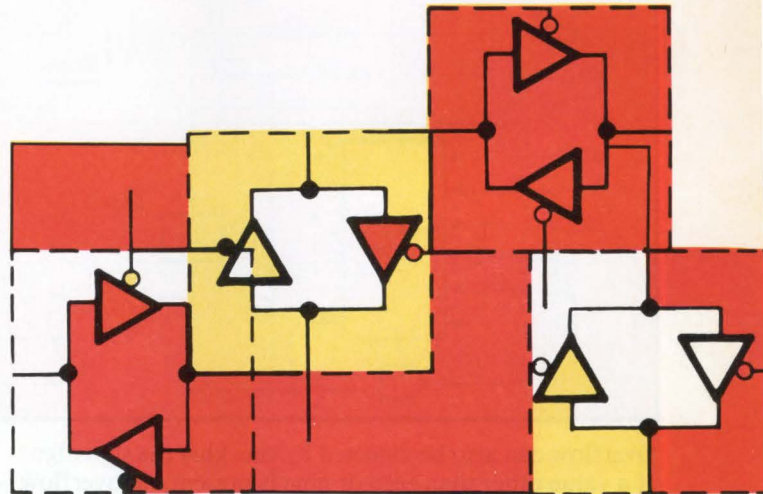
Cascaded bit-slice processors improve computational accuracy when it is necessary to use the binary coded decimal number system.

by Michael J. Miller

The binary coded decimal notation system answers the twofold problem experienced by computers in business settings. Two things occur where base 10 number crunching is paramount. Inaccuracies are introduced by normal floating point number operations based in octal or hexadecimal number systems during round-off and conversion, and the computing overhead necessitated by frequent conversion between bases slows program execution. These problems are minimized if the machine is allowed to work in the same number base as the user. The binary coded decimal system allows binary hardware to operate comfortably in the decimal number system and enables fast and powerful numerical computing because of its bit-slice building block design. In a minicomputer class machine, a bipolar arithmetic logic unit such as the Am29203 can be used to supply binary coded decimal operations that are second to none.

For binary coded decimal (BCD) multiply and divide operations, the arithmetic building blocks are addition and subtraction. When a 4-bit word length is appropriate, the 29203 chip provides these BCD functions as single microcycle instructions. In order to gain speed, the chip employs a carry lookahead scheme compatible with the binary scheme. Consequently, the same signals (CARRY-IN, CARRY-OUT, GENERATE, and PROPAGATE) can be used during BCD and binary arithmetic.

Michael J. Miller was employed by Advanced Micro Devices, where he developed the Am29203 and Am2901C 4-bit slices, when this article was prepared. Currently, he is a software manager at Step Engineering, 757 Pastoria Ave, Sunnyvale, CA 94086.



In order to preserve a valid BCD digit in each slice during addition, the 29203 asserts a carry if the sum is greater than nine. Upon receipt of a CARRY-IN, the next slice must add a 1 to its sum. As in binary, the GENERATE signal indicates that there will be a carry from the slice because the result is greater than nine. If the result is equal to nine, the PROPAGATE signal is asserted, indicating that a carry into the slice will be propagated. Because GENERATE and PROPAGATE are defined as they are, an Am2902 can be used in a carry lookahead scheme just as in binary.

BCD subtraction is also analogous to the binary operation. As in binary, the inverted carry output sense can be interpreted as borrow. It is necessary to borrow from the next digit whenever a larger value digit is subtracted from a smaller value digit. If both digits are of the same value, borrowing is necessary only if the next lower digit is borrowed. GENERATE and PROPAGATE operate as in a binary subtract operation in that a 2902 can be used.

Overflow occurs when there is an unexpected carry into the sign digit, causing an invalid result. This condition can be detected by exclusive ORing of the CARRY-IN to the sign digit with the CARRY-OUT of the sign digit.

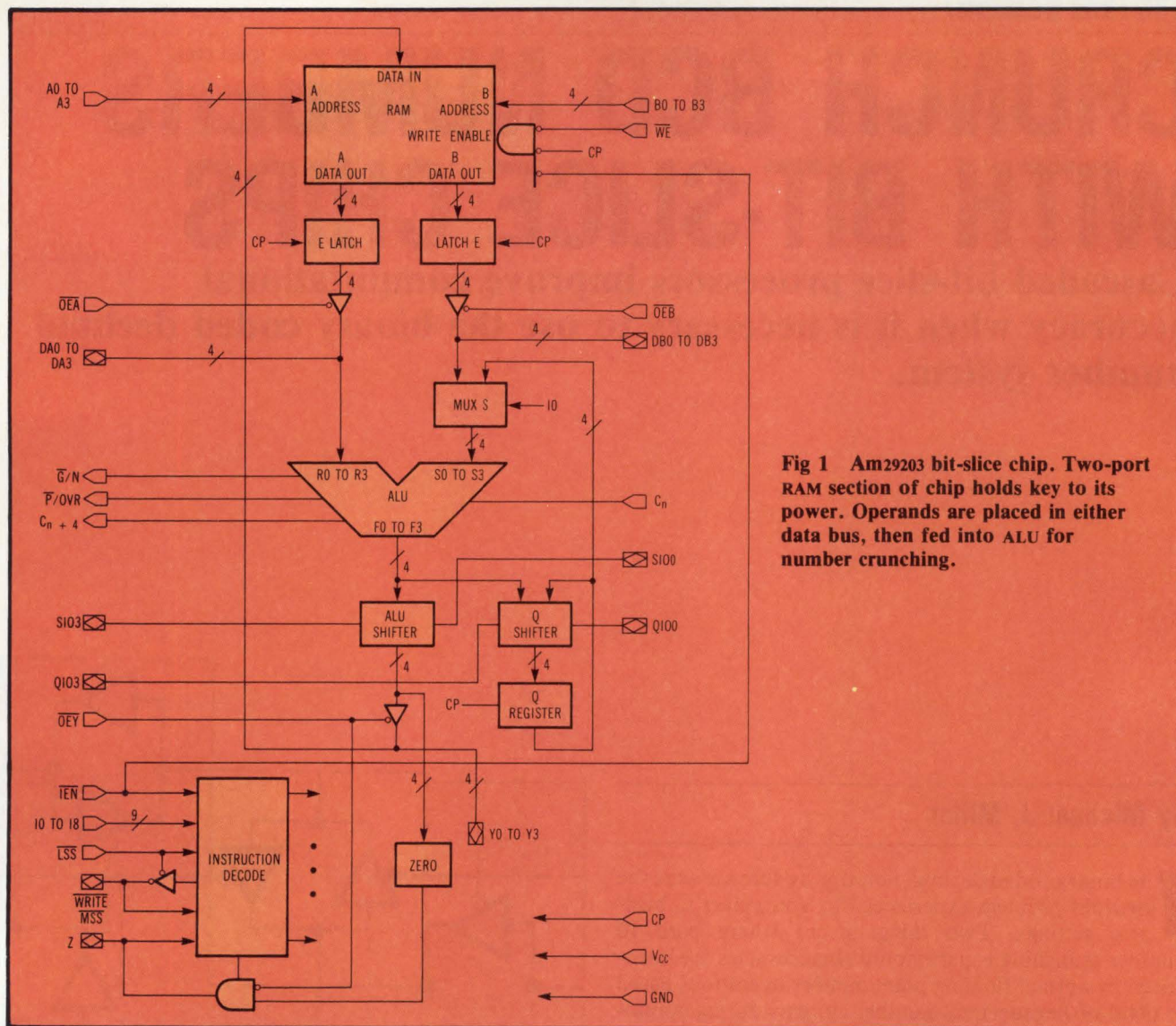


Fig 1 Am29203 bit-slice chip. Two-port RAM section of chip holds key to its power. Operands are placed in either data bus, then fed into ALU for number crunching.

Overflow can also be detected by checking the sign digit. If a value other than zero or nine is present, an overflow has occurred.

ADD and SUBTRACT instructions in the 29203 are also used to simulate multiply and divide operations via iterative algorithms. Because the algorithms are iterative, care must be taken to minimize the microcode loop. When minimizing the microcode, trade-offs can be made between hardware and firmware. The system designer should be aware of these trade-offs since they have an impact on how well the machine fits into the target application.

A 2-port random access memory (RAM) is the 29203's key feature (Fig 1). Two operands, selected by the A and B address buses, can be placed on either of two data buses. They can then be fed into the multifunction arithmetic logic unit (ALU) for number crunching. The ALU's output passes through a shifter and is then returned to the chip's RAM. By cascading 4-bit wide chips like the 29203 together, words of any width can be accommodated.

The 29203 is normally used in a microprogrammable architecture similar to that shown in Fig 2. In such architectures, a processor is composed of two main parts: a microprogram sequencer and an ALU. Lightly shaded

boxes represent the microprogram control. In normal execution, the instruction is fetched into the instruction register. The operation code of the instruction is converted to a microprogram subroutine address by the mapping programmable read only memory (PROM). The sequencer executes the subroutine to generate control and timing signals that direct the rest of the machine in executing the instruction in the instruction register. The sequencer executes an instruction every system clock cycle. As a result, microprogrammable architecture resembles a sophisticated state machine where the pipeline register serves as a current state register.

The darker shaded area of Fig 2 shows the ALU and condition code (CC) circuitry. The ALU takes instructions from the sequencer. The CC register saves the resulting condition code generated by the ALU from one microprogram cycle to the next. The sequencer can examine any one of the condition codes via the CC multiplexer and, when necessary, take a conditional program branch.

Multiplication and division trade-offs and implementation
In most general purpose applications, multiplication constitutes a portion of the instructions at least one order of magnitude smaller than addition. Division usually

occurs two orders of magnitude less than addition. Because addition and subtraction themselves usually represent less than 10% of the total instructions, it is more cost effective to implement multiply and divide operations in firmware rather than combinatorial logic. Firmware algorithms for BCD multiplication and division

are analogous to some of the more classical binary methods. These algorithms are composed of simple operations such as SHIFT, ADD, and SUBTRACT.

Multiplication can be viewed as a series of addition operations. This simple view of multiplication implies a multiple sum of the multiplicand as numbered by the multiplier. This multiple sum can be easily implemented as a firmware loop. Unfortunately for large multipliers, this iterative type of operation is central processing unit (CPU) cycle intensive. However, if the multiplier is viewed as a group of individual digits, each digit can be multiplied with the multiplicand and the result added to an accumulator. After each multiplication and addition, the multiplicand is multiplied by 10 (a 4-bit left shift). The accumulator then becomes the summation of all the multiplications. This algorithm's mathematics can be stated

if multiplicand: $(a_{n+1} a_n \dots a_1 a_0)$
 multiplier: $(b_{m-1} b_{m-2} \dots b_1 b_0)$
 then $A \times B = S \cdot 10^{m-1} \cdot (a_{n-1} a_n \dots a_1 a_0) +$

$$\sum_{i=0}^{m-2} b_i + (a_{n-1} a_n \dots a_1 a_0) + 10^i$$

where $S = \begin{cases} 0 & \text{if } b_{m-1} = 0 \\ -1 & \text{if } b_{m-1} = 9 \end{cases}$

As the equation shows, the sign digit must be accounted for. This is done by subtracting rather than adding when multiplying with the multiplier digit. This algorithm gives a performance improvement over the previously stated method of approximately $(10^m - 1)/9m$, where m is the number of digits in the multiplier. This improvement is realized with only a few additional lines of microcode.

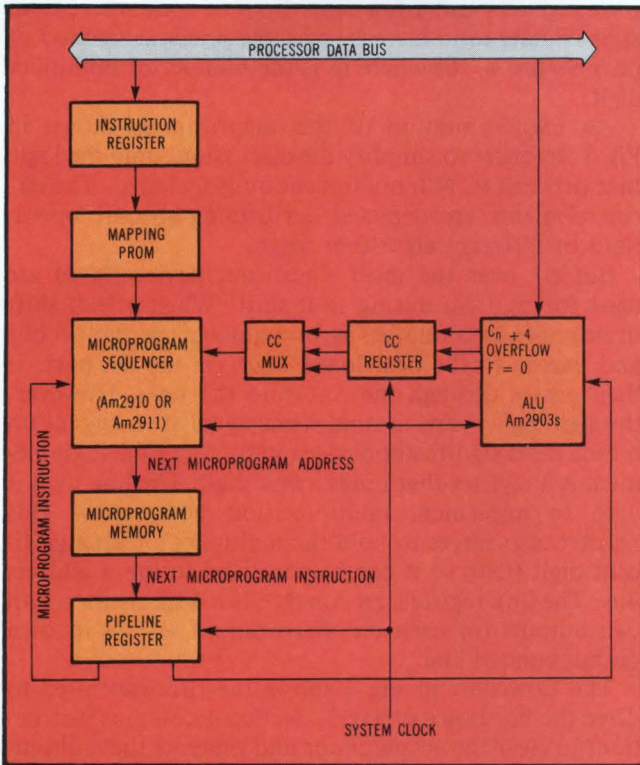


Fig 2 Typical architecture incorporating bit-slice ALU chips. In such schemes overall control resides with microsequencer. Condition codes are generated by ALU.

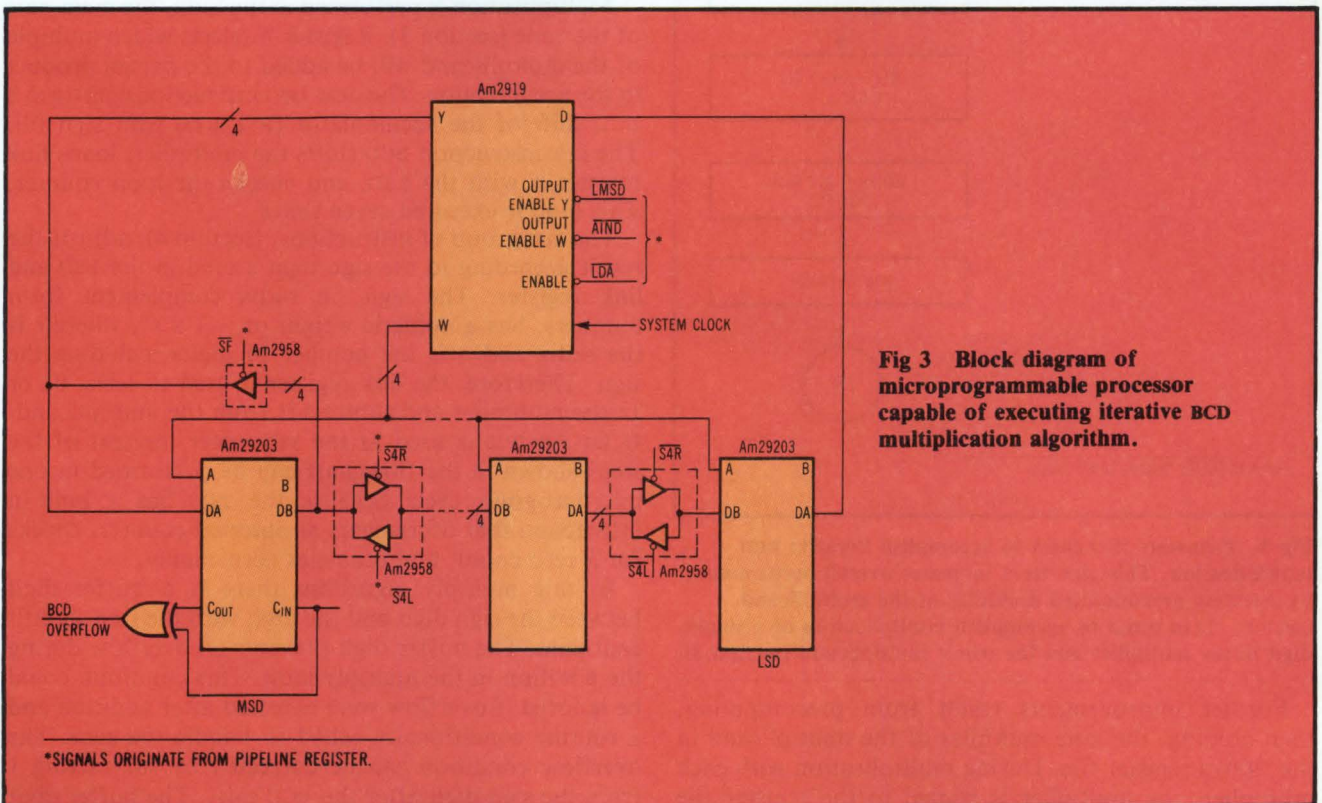


Fig 3 Block diagram of microprogrammable processor capable of executing iterative BCD multiplication algorithm.

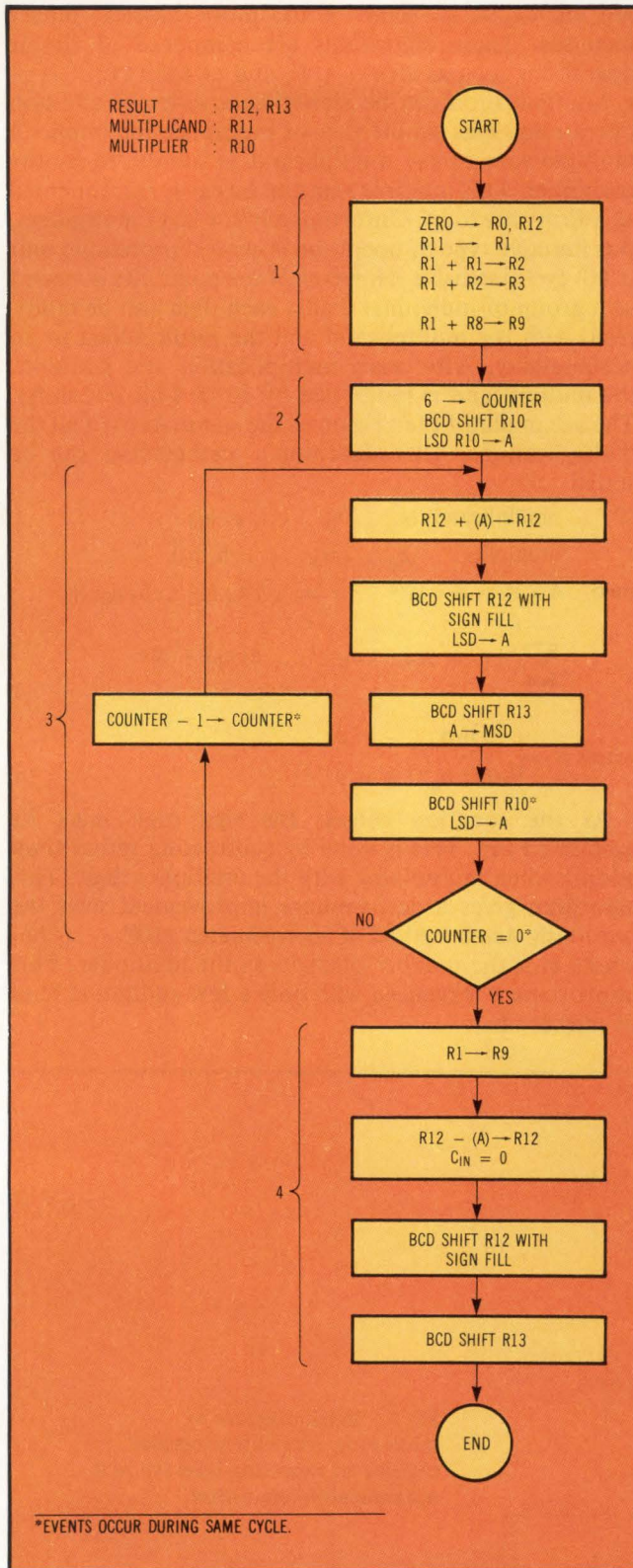


Fig 4 Firmware flowchart to accomplish iterative BCD multiplication. This algorithm increases overall performance by selecting precomputed multiples of the multiplicand (section 1) in order to accomplish multiplication of a single digit in the multiplier and the whole multiplicand (section 3).

Further improvements result from precomputing, then holding, the nine multiples of the multiplicand in the 29203's register file. During multiplication with each multiplier, the multiplier is routed to the register file

address bus to select the multiple, thereby producing a single multiply in one cycle. Because there are nine multiples of the multiplicand, it is not economical to multiply each by 10 every cycle. The same result can be achieved arithmetically by a 4-bit right shift of the accumulator's contents. By using several additional hardware registers and a few more lines of code, there is an approximate ratio increase over the previous method of $(m \times 9)/(m + 10)$ where m is the number of multiplier digits.

An implementation of this algorithm is shown in Fig 3. In order to simplify the discussion, only the logic that pertains to BCD multiplication is included. The circuit elements are depicted performing specific operations of different algorithm parts.

Buffers over the most significant device (MSD) are used for sign fill during BCD shift. When a BCD shift occurs, the BCD number is brought out on the DB bus and passed to the next lower digit via the DA port. It then passes through the ALU into the RAM. However, the sign digit wraps around from signal DB to signal DA on the most significant device (MSD). The final logic element is a register that holds a link digit. The link digit is used to implement multiprecision BCD shifts. This register also serves to hold the multiplier's least significant digit (LSD) so it can be presented to the A address bus. The link register, an Am2919, is a 4-bit register with two outputs for each bit. Each output set has its own output control line.

The flowchart in Fig 4 shows the firmware used to drive the hardware of Fig 3. Section 1 contains instructions to clear the accumulator and generate the multiplier's multiples. This operation takes 11 cycles to execute. Section 2 initializes the counter in the sequencer to one less than the number of times desired to loop. It also loads the multiplier's LSD into register A.

Multiplication is performed in the loop, the main part of the code (section 3). Register A selects which multiple of the multiplicand will be added to the partial product in the accumulator. The next two instructions perform a BCD shift of the accumulator (R12, R13) with sign fill. The last instruction BCD shifts the multiplier, loads link register A with the LSD, and checks the loop counter. This loop is executed seven times.

The last group of instructions, (section 4), adjusts the result according to the sign digit stored in the LSD and link register. The sign, in radix complement form numbers, has a numeric weight of $-1 \times r^n$, where r is the radix and n is the number of digits including the sign. Therefore, the link register is used to select 0x or 1x the multiplier and subtract it from the multiplicand. If an Am2910 is used as the sequencer, several of the steps shown in the flowchart can be performed in one microprogram cycle because the 2910 has a built-in instruction that decrements an internal counter, checks for a zero count, and branches accordingly.

In this multiply algorithm there is a buffer digit between the sign digit and the digit with the first significant data. The buffer digit prevents an overflow during the addition in the multiply loop. This condition could be ignored if overflow were detected after addition and a routine conditionally called to handle the case. The overflow condition can be corrected by subtracting 1 from the sign digit after the BCD shift. The buffer digit



OUR SURPRISING COLOR, RESOLUTION AND PRICE.

The ECM 1301 price is as surprising as the resolution and color choice.

Electrohome ECM 1301 enhances the capability of professional desk-top computers.

Resolution is extremely high. Color choice is virtually infinite—although one computer enthusiast has worked it out to a choice of 16 million colors.

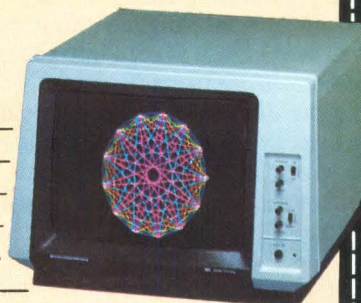
There is also a choice of interface modules for compatibility with leading computer makes.

The performance would be surprising at any price.

But, it's even more remarkable that the 13" Electrohome ECM 1301 is priced far lower than you'd expect for conventional, high resolution color monitors.

ELECTROHOME (U.S.A.) LIMITED,
250 WALES AVENUE,
TONAWANDA, NEW YORK 14150
 PLEASE SEND MORE INFORMATION.
 PLEASE HAVE A REPRESENTATIVE CALL.

Name _____
Company _____
Street _____
City _____
State/Prov. _____
Zip/Postal Code _____
Phone _____



ECM/CD/3

Mail the coupon now for more information on the ECM 1301—another result of Electrohome's seventy-five years of quality and innovation.

ELECTROHOME

ELECTRONICS

can also be eliminated by converting the numbers to a positive sign magnitude, multiplying them, and adjusting the result according to the product of original signs of multiplier and multiplicand.

Division: a series of subtractions

In the same way that multiplication is viewed as a series of additions, division can be thought of as a series of subtractions. The simplest way to divide is to count the number of times the divisor can be subtracted from the dividend before it is negative. Though this method is costly in microprogram cycles, it illustrates how division is the inverse of multiplication. The algorithm developed for division is a form of nonrestoring division.

For convenience' sake, it is assumed that both the dividend and the divisor are fractions, that the dividend and divisor are normalized (which implies keeping track of exponents implicitly or explicitly), and that both are positive. Since division is the inverse of multiplication, it is reasonable to assume that a method of division can be devised that entails subtracting a multiple of the divisor from a running partial sum and then shifting the partial sum. This is, in fact, the basis for most division algorithms. Generally speaking, division is not as fast as multiplication because it is difficult to determine which multiple of the divisor to subtract from the partial dividend. Consequently, most division algorithms employ trial and error to determine how much to subtract.

One such algorithm, the restoring division algorithm, subtracts the divisor from the dividend until a negative partial dividend is created. The divisor is then added to the partial dividend to restore it to a positive partial dividend. A count—the MSD of the quotient—is kept of how many divisors went into the dividend before there was a negative dividend. The partial dividend is then shifted up one digit by multiplying by radix 10. The procedure of subtracting the divisor and counting is repeated for each digit in the quotient. This method is similar to the long division taught in grade school where trailing divisors are tested and finally subtracted from the dividend. After each division the trailing divisor is moved over one column.

An average of five subtractions and one addition for each digit in the quotient is performed by the restoring algorithm. The addition is eliminated by performing a nonrestoring algorithm. The nonrestoring division algorithm functions like the restoring algorithm until it encounters the negative partial dividend. At this point, the dividend is shifted up one BCD digit without being restored. The count that was kept is placed into the quotient's MSD. The counter is then set to nine and is decremented each time the divisor is added to the dividend. The adding and decrementing continues until the partial dividend is positive. The counter's contents are then placed in the quotient's second MSD, and the partial dividend is shifted up one BCD digit. At this point, the algorithm starts over.

The nonrestoring algorithm is the more efficient of the two firmware algorithms. A further improvement can be made in the nonrestoring firmware algorithm if, instead of repeatedly subtracting the divisor from the dividend, binary weighted multiples are subtracted in a successive approximation. To accomplish this, an algorithm starts by subtracting 8x the divisor from the

dividend, then 4x the divisor, then 2x the divisor, and finally the divisor itself. Each time a multiple is subtracted, the result's sign is inspected. If the sign does not change, a 1 is placed in the corresponding bit of the quotient digit. For example, if 8x the division worked, then a 1 would be placed in the most significant bit of the quotient digit (2^3). If the sign changes, then a 0 is placed in the corresponding bit position. When the sign changes during operations with the next lower binary weighted multiples, the algorithm continues in the same way, but addition is performed rather than subtraction.

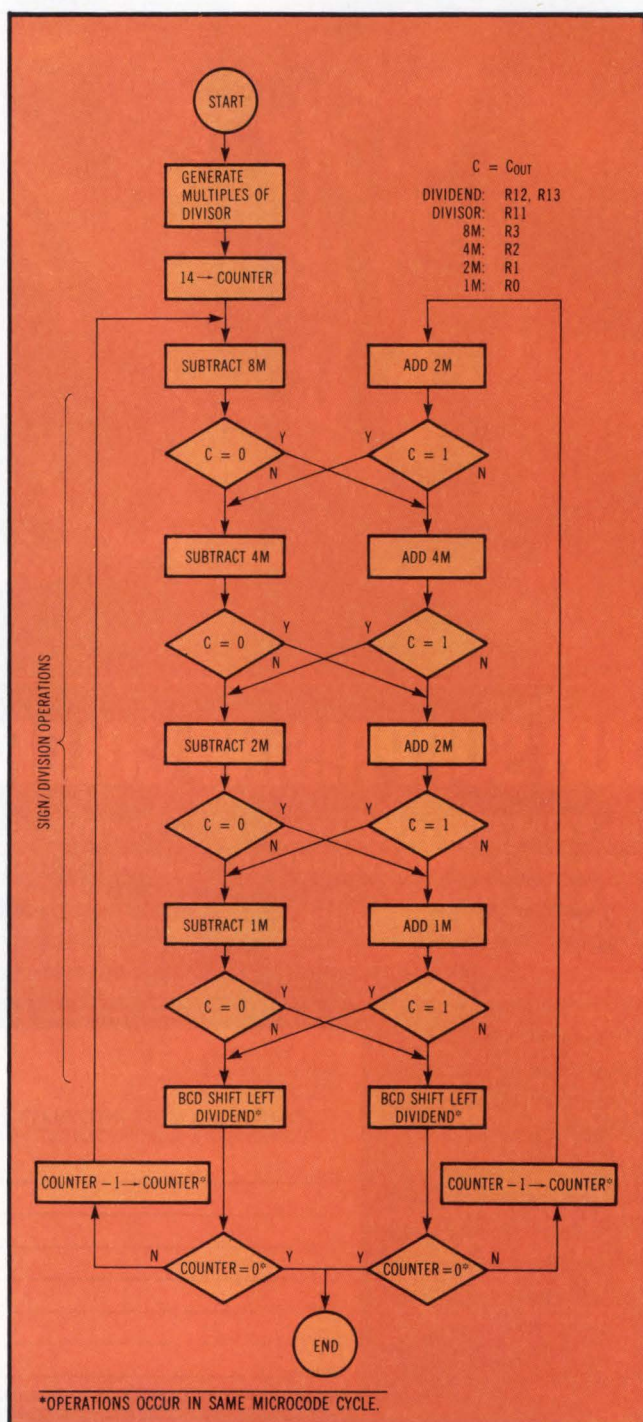


Fig 5 Firmware flowchart to accomplish iterative BCD division. This algorithm employs the concepts of both nonrestoring division and successive binary approximation.

Available now!
And SMS is
not afraid
to show it

A Micro Winchester System
in a Micro Package

Compact 9.5"W x 11.2"H x 17"D table top package

256Kb main memory (4Mb addressability)

Expansion space for 4 dual LSI-11 boards

PDP-11* architecture compatible with DEC*
RT-11, RSX-11M and Unix** software

LSI-11/23 processor

4 serial ports

8" RX02 and 1.2Mb IBM floppy backup

Auto self-test for CPU, memory, disk drives

Easy access to LED display of system faults

10.6Mb or 15.9Mb 5¼" Winchester package

Advanced disk controller with ECC, flaw management, bootstrap,
error retry, and direct non-interleave data transfer

AVAILABLE WITHOUT CPU and memory for volume requirements

* Trademark of Digital Equipment Corporation. ** Trademark of Western Electric.

SMS

**Scientific Micro
Systems, Inc.**

777 E. Middlefield Road
Mountain View, California 94043
(415) 964-5700

AUTHORIZED SMS DISTRIBUTOR FOR DEC
Q-BUS PRODUCTS: FIRST COMPUTER
CORPORATION (312) 920-1050

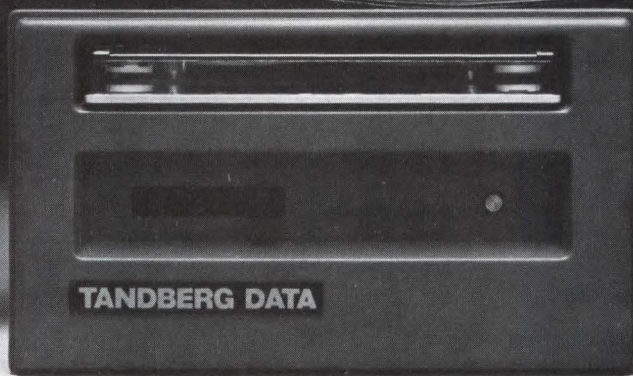
SMS SALES OFFICES:

Phoenix, Arizona (602) 978-6621;

Boston, MA (617) 246-2540; **Atlanta, Georgia**

(404) 296-2029; **Morton Grove, Illinois** (312)

966-2711; **Yorba Linda, California** (714) 993-3768.



A STRONG STATEMENT ABOUT OUR STREAMER'S ACCURACY AND RELIABILITY.

We're standing on our streamer to show you just how well Tandberg's 3200 family of 20 MB and 45 MB $\frac{1}{4}$ " cartridge drives are engineered. Of course, we didn't design them to be stepstools.

DESIGNED FOR DATA INTEGRITY.

Unlike most other drives, the 3200's body is fully cast to keep drive mechanisms stable and accurate. What's more, Tandberg's exclusive 3-point positioning and cartridge locking system ensures that cartridges are always correctly loaded and can't be jarred off track.

And while others still use less accurate mechanical referencing to locate the edge of the tape, Tandberg's exclusive Floating Head System finds this reference point dynamically using a signal seeking method. A precision, microprocessor-controlled stepping motor then locates the desired track—with better than 16 track accuracy. (Since our

20 MB and 45 MB units have 4 and 9 tracks respectively, the system is at least twice as accurate as it needs to be.)

Tandberg's system completely eliminates interchangeability problems caused by cartridge wear, drive wear, and mechanical tolerance build-up. It's the main reason why our streamer gets more reliable performance from $\frac{1}{4}$ " cartridge tapes than anyone else in the industry.

A HEAD ABOVE THE COMPETITION.

Our 20 MB drive has the same cast body, the same cartridge lock, the same head positioning system as our 45 MB unit. Even the standard features are the same: QIC compatible interface, expandable circular FIFO buffer (up to

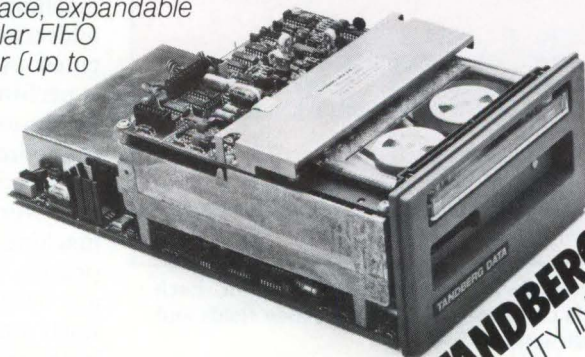
16 KB) for increased throughput, and full saturation recording. So what's the difference between our 20 and 45?

The head.

One screwdriver and one 9 track head are all you need to upgrade our 20 to 45 MB—with no mechanical adjustments whatsoever.

So if you're looking for a streamer that's accurate, reliable, and extremely flexible, step up to the only one you can stand on. Tandberg.

For more information contact, Tandberg Data Inc., DATA STORAGE DIVISION, 571 North Poplar, Suite H, Orange, CA 92668/(714) 978-6771.



TANDBERG DATA
QUALITY IN EVERY BIT.

Microcode for Bit-slice BCD Operation*

Field names Subfield names	Microcode address	Program label	Constant field PL	Am2910					3-address/ 2-address operation 3 address
				I	CCP	CC	CLEN	\overline{RLD}	
Bit position in microword			0 to 11	12 to 15	16	17 to 19	20	21	22
No of bits in each field			12	4	1	3	1	1	1
	100	BCDM:	x	E	x	x	x	1	0
	101		x	E	x	x	x	1	0
	102		x	E	x	x	x	1	0
	103		x	E	x	x	x	1	1
	104		x	E	x	x	x	1	1
	.		.	.	x	x	x		.
	.		.	.	x	x	x		.
	.		.	.	x	x	x		.
	10A		x	E	x	x	x	1	1
	10B		OOD	4	x	x	x	0	1
	10C	LOOP1:	x	E	x	x	x	1	1
	10D		x	E				1	1
	10E		x	E				1	1
	10F		x	8				1	1

*Four-bit fields are in hexadecimal; others are in octal. Symbol x indicates "don't care." Microword bit positions not depicted for Am29203 have the following signal levels: C_n , WE, OEY logic zero.

executes in five cycles for each BCD digit. Since it takes just as many cycles as the nonpipelined system, the net gain is equal to the performance difference between the pipelined and the nonpipelined systems.

Working in microcode

After the hardware is designed and algorithms are chosen, the programmer has to generate flowcharts and translate them into working microcode. In order to

provide some understanding of this esoteric task, some of the assembled code for the BCD multiply routine is provided in Fig 7.

Because each microprogrammed machine has a different architecture, the syntax and mnemonics of the microprogram can vary. And, because architecture dictates the signals that need to be controlled, the microprogram word's structure and content for each machine also varies. When writing microcode for a new machine, the programmer has two choices: write a new assembler or use a meta assembler. The disadvantage of writing a new and unique assembler is that it takes time. Also, it is often more difficult to accommodate changes in the microword as hardware development proceeds. In addition, the meta assembler approach allows more flexibility.

The following is an example of how BCD multiplication can be implemented in microcode. Each line of microcode is a complete instruction to the microengine and is composed of several operation code fields. These fields control the different portions of the entire machine. In this example a single field generates the address of the next microprogram instruction to be executed. Another field specifies which operation the 29203 is performing. The Table, "Microcode for Bit-slice BCD Operation," shows the different opcode fields in the microprogram word.

Since there are multiple opcode fields in the instruction word, the syntax must be different from that of machine assembly language—which, in general, has one opcode field. Like standard assembly language, there are opcodes and operands represented as mnemonics. Each mnemonic is associated with a particular bit field in the microinstruction word. The "&" symbol is used

```

100 BCDM:  LOW R0 & CONT
101        LOW R12 & CONT
102        PAR R11,R1 & CONT
103        BCDA R1,R1,R2 & CONT
104        BCDA R1,R2,R3 & CONT
105        BCDA R1,R3,R4 & CONT
106        BCDA R1,R4,R5 & CONT
107        BCDA R1,R5,R6 & CONT
108        BCDA R1,R6,R7 & CONT
109        BCDA R1,R7,R8 & CONT
10A       BCDA R1,R8,R9 & CONT
10B       BCDSR R10 & LDA & COUNT OOD & CONT

10C LOOP1: BCDA R12,,R12 & AIND & CONT
10D       BCDSR R12 & SIGNFILL & LDA & CONT
10E       BCDSR R13 & LMSD & CONT
10F       BCDSR R10 & LDA & CNTR & GOTO LOOP1

110       PAR R1,R9 & CONT
111       BCDS R12,,R12 & AIND & CONT
112       BCDSR R12 & SIGNFILL & LDA & CONT
113       BCDSR R13 & LMSD
    
```

Fig 7 Source microcode for BCD multiply operation. Each line of microcode is composed of several opcode fields and one complete instruction.

Am29203								Miscellaneous BCD Control Signals					
Source A	Source B	Destination B	$\overline{OE}A$	I_0	$\overline{OE}B$	Destination $I_{5 \text{ to } 8}$	Function $I_{1 \text{ to } 4}$	\overline{SF}	\overline{LMSD}	\overline{AIND}	\overline{LDA}	$\overline{S4R}$	$\overline{S4L}$
24 to 27	28 to 31	32 to 35	36	37	38	41 to 43	44 to 47	48	49	50	51	52	53
4	4	4	1	1	1	4	4	1	1	1	1	1	1
x	x	0	0	0	0	8	8	1	1	1	1	1	1
x	x	C	0	0	0	8	8	1	1	1	1	1	1
B	x	1	0	0	0	F	6	1	1	1	1	1	1
1	1	2	0	0	0	B	0
1	2	3	0	0	0	B	0
1	8	9	0	0	0	B	0	1	1	1	1	1	1
x	A	A	1	0	0	8	8	1	1	1	0	0	1
x	C	C	0	0	0	B	0	0	1	1	0	0	1
x	C	C	1	0	0	8	8	1	0	1	1	0	1
x	D	D	1	0	0	8	8	1	1	1	0	0	1
x	A	A	1	0	0	8	8
							

as an operator to concatenate the different operations to be performed in a given microprogram word. For example, two operations are specified in word 100 of Fig 7. LOW RO directs the 29203 to clear register 0, and CONT directs the 2910 to continue to the next instruction at 101.

If the microprogram word 100 in Fig 7 is carefully compared with the assembled code in the Table, it is apparent that some bits were not logically specified by LOW RO or CONT. These bits were left to default. Line 10D is an example of when one of the bits ("sign fill") is finally specified rather than allowed to default. Default values must be supplied by the microcode assembler. Sometimes, the default can actually be a "don't care."

The Table shows the final assembled code as it will be programmed in the microprogram control store. The bits that are shown as "don't cares" are allowed to be in the unprogrammed state of the control store.

There are several inherent advantages in taking a bit-slice approach to BCD multiplication and division operations—improvements in system performance, speed, and accuracy are just a few. The Am29203's architecture is particularly suited to applications where both binary and BCD arithmetic is a necessity. By incorporating iterative algorithms into microcode, many of the disadvantages of time-consuming BCD operations are eliminated.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 704 Average 705 Low 706

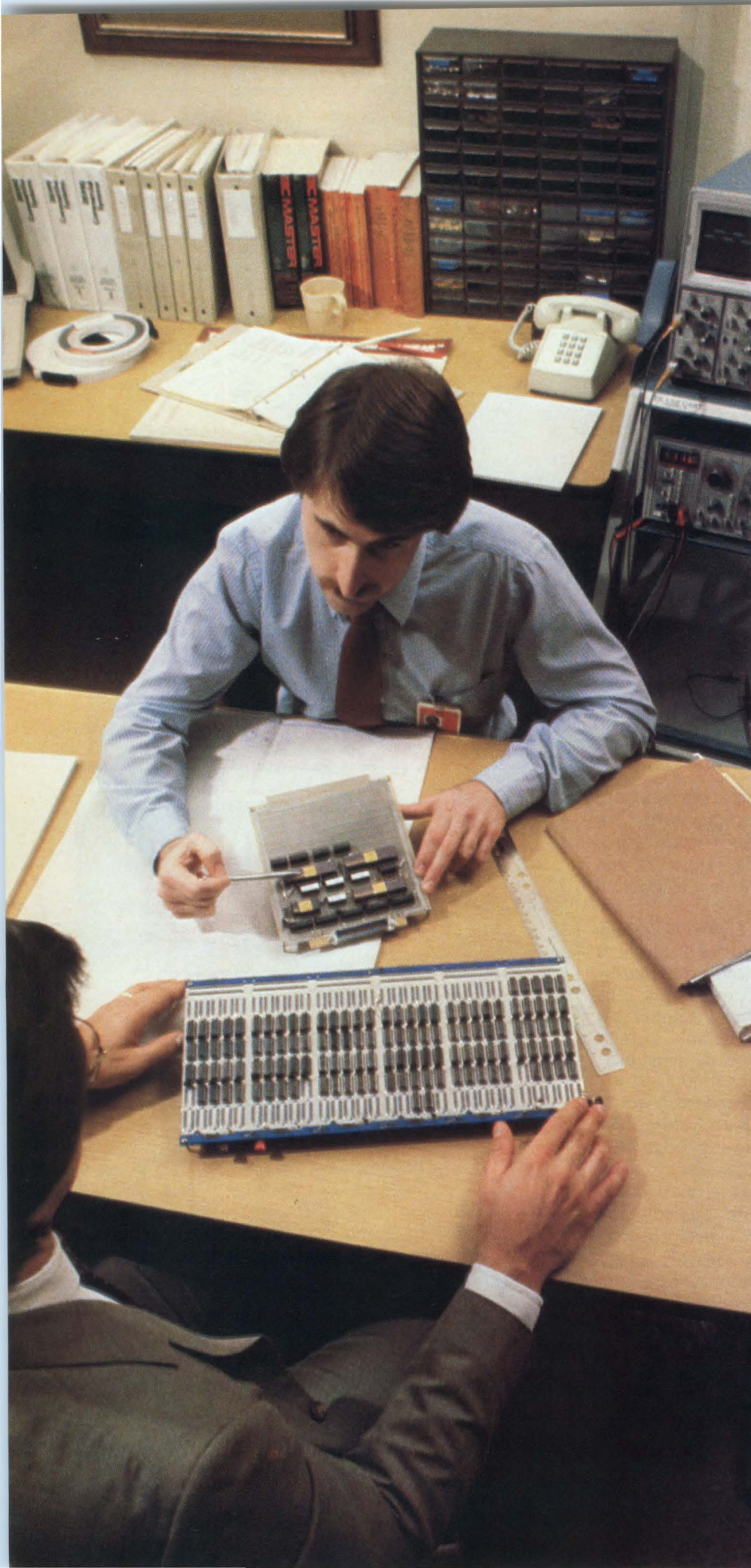
The "free piston" air pump quietly gives you more CFM per W & per lb.

MÉDO Sole Distributor **FREE PISTON**

"Free piston" design makes the Médo linear-motor-driven vacuum pump/air compressor totally different from all others. With only one moving part, it not only uses less power than anything else that pumps the same amount of air, it's also quieter (sound levels 40-50 dBA/m), smaller, lighter, longer lived, and more reliable. It does not need oil, cannot spark, and an overload cannot cause coil burning. Applications include robotics products, vacuum pickups, vacuum sensors, air bearings for magnetic tapes, health and medical aids, aspirators, cosmetic and beauty aids, septic tank blowers, and spray guns.

Ten standard models usable as pumps or compressors range from 0.28 to 1.94 CFM, 20 to 95 W (AC) input power, 1.8 to 10.8 lbs., and approx. 4.8" x 3.56" x 3.25" to 8.8" x 5.4" x 6.1". Two vacuum-pump-only models can produce vacuums of -7.8"hg. and -24.4"hg., use 40 and 70 W, weigh approx. 6.4 and 11 lbs., and measure approx. 8.2" x 4.1" x 5.9" and 8.28" x 5.38" x 6.1". Customization available on large orders.

Call or write the sole distributor, Médo USA, Inc., 808-C N. Central Ave., Wood Dale, IL 60191. Tel: 312/860-0500. West Coast: 213/534-0337. Mfd. by Nitto Kohki, Co., Ltd., Tokyo, Japan.



No. 3 in a series:

Is there a my "glue

Certainly. And, TI's new, easy-to-use TAL002 and TAL004 low-power Schottky logic arrays help you substantially cut component count and power consumption. The Answermen at TI's Regional Technology Centers (RTCs) can help you decide whether these arrays or more complex arrays from TI's broad family (see table opposite page) will be the most appropriate for your applications.

RTC Answermen Hot Line Numbers

ATLANTA	(404) 452-4686
BOSTON	(617) 890-4271
CHICAGO	(312) 228-6008
DALLAS	(214) 680-5096
NORTHERN CALIFORNIA	(408)-980-0305
SOUTHERN CALIFORNIA	(714) 660-8164
BEDFORD, ENGLAND	0234 223000
FREISING, WEST GERMANY	08161 800
HANNOVER, WEST GERMANY	0511/648021
TOKYO, JAPAN	03-498-2111

The TAL002 offers 280 gates while the TAL004 offers 400 gates—LSI complexity that allows each array to eliminate 10 to 25 devices in systems implemented with traditional SSI/MSI logic.

Utilizing TI's time-proven low-power Schottky technology, these new arrays operate at 1.25 mW typical power dissipation per gate. At the standard 5 volts.

All of which means not only smaller boards and lower power but also fewer parts to order, inspect, and inventory. Faster board assembly. And improved system reliability.

TI produces and stocks the master low-power Schottky logic arrays, each of

◀ **Reduced board size** is only one benefit of using TI's new low-power Schottky logic arrays. RTC Answermen at TI's Regional Technology Centers can explain in person or over the phone how you can also reduce power consumption, improve reliability, and achieve overall system savings. The RTCs are equipped and staffed to provide an efficient, accessible means of determining the most cost-effective semiconductor solutions to your design problems.

Ask the RTC Answermen at Texas Instruments

place for logic arrays in logic" applications?

which is a collection of uncommitted gates. During the last stage of manufacture, these master arrays are completed with the specific interconnect pattern provided to TI by you. As a result, you get a customized array at a cost near that of volume production.

Can I realize the benefits of low-power Schottky arrays in my present system?

Yes, that's one of the major advantages of these new arrays. They are a highly efficient, economical means for upgrading existing systems—and for implementing new designs—that require moderate-size logic blocks.

The TAL002 and TAL004 arrays interface directly with TTL-compatible devices, including popular microprocessor and memory components.

How much design help will you give me?

As much or as little as you feel you need.

Since TI first patented the logic array, TI has developed and put in place what has been called "probably the most advanced in-house design automation capability" of any of the leading array suppliers surveyed.* These resources, equally available to all of TI's logic array customers, are especially applicable for higher density arrays.

Actually you'll find the design of TI low-power Schottky arrays relatively easy.

A comprehensive design manual sets out the logic and layout rules. The manual also explains a simple shorthand method of describing the circuits so that a detailed check of layout and test patterns can be carried out at TI.

You furnish your interconnection pattern, drawn on a translucent grid supplied by TI, and the software data base describing device behavior. If you wish, TI will contract with you to do the layout and other design work.

To further simplify the design effort, a variety of standard macro overlays is available for commonly used circuits, and

*A multi-client study of the STRATEGIC IMPLICATIONS OF LOGIC ARRAYS," Mackintosh Consultants Co., Ltd., Mackintosh House, Napier Road, Luton, England LU1 1RG.

Fast, Efficient TI Logic Array Family

Array	Gates**	Technology†	Gate Delay	Gate Power	I/O Signals	Commercial/Military
TAL002	280	LPS	5.0 ns	1.25 mW	29	C
TAL004	400	LPS	5.0 ns	1.25 mW	42	C
TAT004	400	STL	2.5 ns	600 μ W	76	C/M
TAT008	800	STL	2.5 ns	600 μ W	104	C/M
TAT010	1000	ASTL	1.0 ns	300 μ W	88	C
TAT020	2000	ASTL	1.0 ns	300 μ W	120	C/M
STL700	560	STL	3.0 ns	300 μ W	61	M
SBP96700	1120	I ² L	11/15 ns	100 μ W	96	M
SBP96600	2120	I ² L	11/15 ns	100 μ W	140	M

**Usable gates

†LPS—Low-power Schottky

†STL—Schottky Transistor Logic

†ASTL—Advanced Schottky Transistor Logic

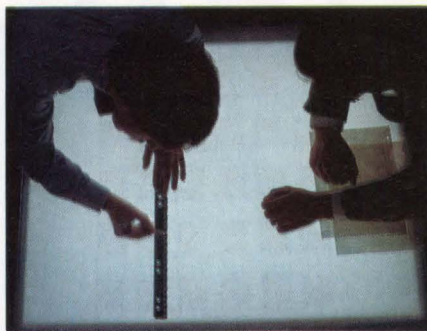
†I²L—Integrated Injection Logic

a wide choice of standard buffers is provided for inputs and outputs.

Can I check out my design before production?

Yes, that's the point of TI's logic array design process—to minimize design errors and aim for first-pass success.

TI will computer-verify your design prior to mask fabrication. This computer-aided check makes certain that the final interconnect layout is identical to your original schematic and that all fabrication layout rules have been followed.



Preparing the interconnection pattern for your low-power Schottky logic arrays is but one task that can be done for you on a contract basis by TI's Regional Technology Centers. The RTCs can also provide engineering services for complete array design.

What's my first step?

Talk with the Answerman at your nearest Texas Instruments RTC about low-power Schottky logic arrays. His Hot Line telephone number is listed on the opposite page. He is immediately available to give you more detailed information and to answer more of your questions.

He can help you determine how and where these new arrays can best benefit your system. And should logic arrays of greater complexity seem more suitable, he can explore with you all of the options available in TI's broad logic array family.

You can also visit the Answerman at your RTC and learn first-hand what low-power Schottky logic arrays can do for your system. Or contact your local TI sales engineer.

For our logic array brochure, write
Texas Instruments
Semiconductor Group RL,
Dept. 3010S, P.O. Box 401560,
Dallas, Texas 75240

Creating useful products
and services for you.



TEXAS INSTRUMENTS

**16000 WAYS
TO OVERCOME
THE LIMITATION
OF YESTERDAY
MICROPROCESS**

E
NS
S
ORS.

THE NS16000 MICROPROCESSOR FAMILY INCREASES SOFTWARE PRODUCTIVITY AND MAKES OTHER MICROS LOOK ARCHAIC.

Software productivity has become a major issue in computer-related product development. In microprocessor-based systems, software productivity centers around the capability of the microprocessor to maximize software utility relative to shorter development cycles, improved software reliability, and extended software lifecycles.

The degree to which the microprocessor can maximize software utility directly affects the cost of a product, its reliability, and time to market. It also eliminates future software modification for product enhancement or because of rapid advances in hardware technology.

The NS16000's architecture effectively addresses these software issues.

EFFICIENT MEMORY MANAGEMENT.

This microprocessor family combines 32-bit performance with demand paged virtual memory for efficient management of large address space. It facilitates high level language program development and efficient program execution. Floating point is also integrated into the architecture.

This combination gives the user large system computing power at a lower cost. Two orders of magnitude lower, in fact.

WE WEREN'T SATISFIED WITH THE "BOTTOM UP" APPROACH.

When we began designing the NS16000 microprocessor family, we decided on a radical departure from existing architectures—designs that date back more than a decade.

While others extended 8-bit component technology upward to the system level, we weren't satisfied with that "bottom up" approach. Instead, we anticipated the computing needs of the '80s and '90s and took the time to extend sophisticated mainframe and minicomputer technology downward to the chip level.

The result is an advanced and efficient family of microprocessor hardware, software and development support products. Our entire NS16000 family offers everything you'd expect from powerful 32-bit machines and is easier to program and use than 16-bit "bottom up" micros.

Everyone who has evaluated the NS16000 recognizes its advanced architecture. We appreciate that response. Because it proves that the NS16000 family is exactly what we designed it to be—a solid foundation from which we can build solutions for your future designs while satisfying your needs for today.

NS16000. THE PROGRAMMERS' MICROPROCESSOR.



National Semiconductor

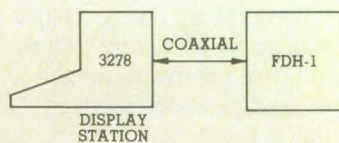
MICROCOMPUTER SYSTEMS DIVISION

Protect your sensitive IBM data with our new Fiber Optic Link

- Plug compatible with IBM series 3250, 3270A, and 3270B equipment.
- Replaces coaxial cable with fiber optic cable.
- Up to 1 Km operating range — virtually immune to electromagnetic interference.

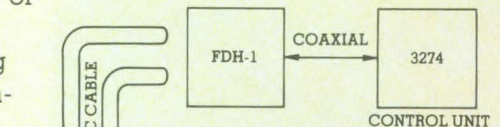
Versitron's FDH-1 (fiber optic digital hybrid) was designed to replace the coaxial transmission path in systems equipped with the IBM 3250 or 3270 series equipment. The simple installation of a fiber optic link provides two very important benefits to the user. First of all, the security level of the transmission link is greatly improved since fiber optic cables are inherently im-

mune to conventional wire-tapping techniques. Secondly, the system operating capability will be enhanced since fiber optic cables are impervious to virtually all types of electromagnetic interference. This includes, of course, interference from heavy duty manufacturing equipment and noisy adjacent cables.

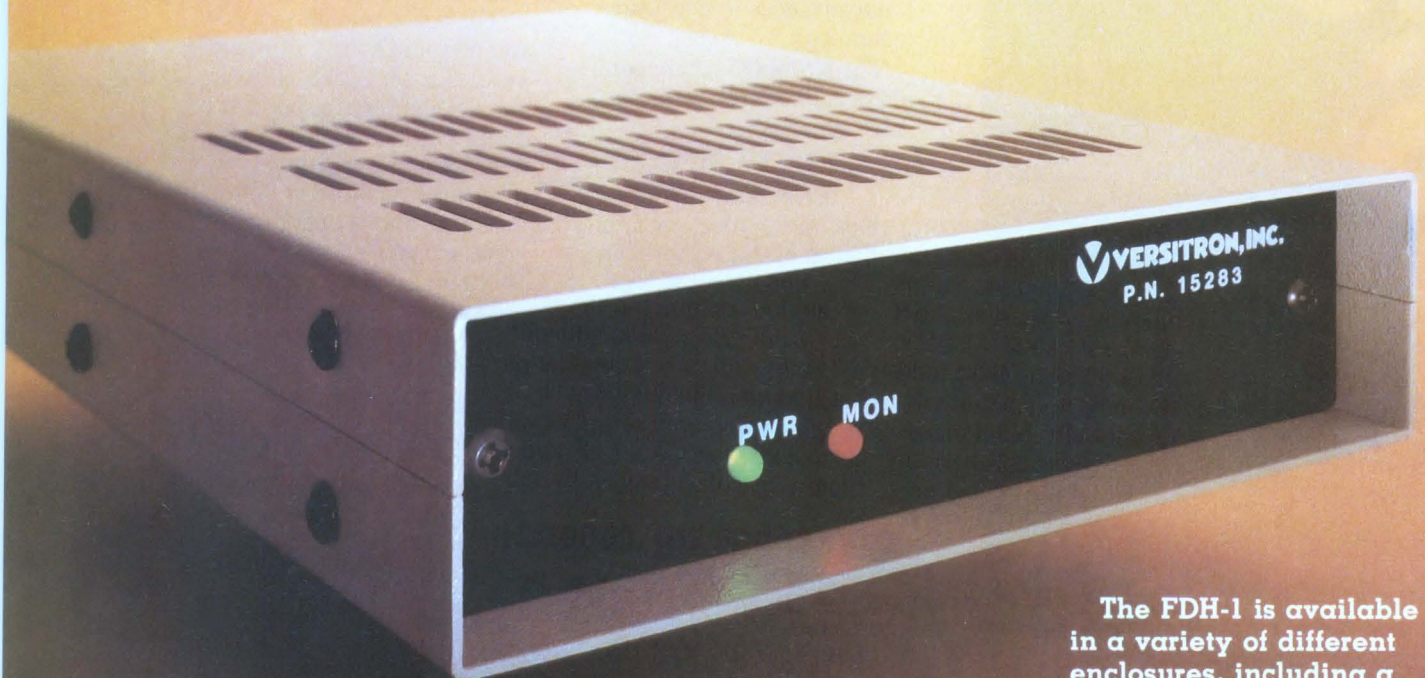


Versitron's FDH-1 combines the high speed capabilities of a coaxial cable with the inherent advantages of a fiber optic cable. By in-

terfacing directly to the coaxial cable, the FDH-1 appears totally transparent to the rest of the system; thus eliminating any operating restrictions.



If you're currently transmitting high speed data over a coaxial cable and you're concerned about data security, give us a call at (202) 882-8464 and get all of the details on how our FDH-1 will not only protect your data; but may also actually increase the operating efficiency of your entire system.



See us at Interface Booth 526

The FDH-1 is available in a variety of different enclosures, including a sealed unit specifically designed for EMI/RFI suppressed applications.

 **VERSITRON, INC.**

6310 Chillum Place, N.W., Washington, D.C. 20011, TEL: (202) 882-8464
CIRCLE 88 TWX: 710-822-1179

IMPROVING COMPUTATIONAL THROUGHPUT

By tying several 8087 numerical data processing chips to a single 8086 CPU, parallel instruction execution can be accomplished with resulting increases in operational speed.

by Cedar Yoram and
Meir Ben-Nun

Using microcomputers to perform arithmetic computations is a technique that has seen striking growth. Recent progress in this method has been aided considerably by the introduction of the 8087 numerical data processor. This chip, together with the 8086 central processing unit, forms the iAPX 86/20 microcomputer. The numerical data processor allows fast and simple numerical computations of floating point arithmetic and transcendental functions. Performance is hindered, however, because the manufacturer imposes a severe restriction on the system—only one numerical data processor can be connected to a central processing unit. Therefore, other solutions must be considered for applications that require a greater computational throughput than that available from the iAPX 86/20.

One recommendation is a design based on a number of microcomputers connected through a standard Multibus.¹ Unfortunately, such a solution leads to a partitioning of the algorithms, which results in intensive and complex data communications problems. Using a custom designed bus, tailored specifically for a given

Cedar Yoram is manager of the electrical engineering design group at Israel's Ministry of Defence, Haifa, where he is responsible for the design of multiprocessing computers. Mr Yoram has a BSEE from the Technion, Haifa, Israel. He is presently working on his MSEE at the Technion.

Meir Ben-Nun is a senior electronic design engineer at Israel's Ministry of Defence, where he is working on the design of multiprocessing computers. Mr Ben-Nun has a BSC in electrical engineering and a BSC in electronic teaching from the Technion.

problem, could simplify the communication protocol. Designing such a bus, however, would be a complicated task. Another solution is a special purpose high speed arithmetic unit designed to suit the specific computational demands of the problem. This method usually requires a large number of components and a long design period. A third solution, the multiple numerical data processor system (MNDPS), presents a simple method for combining a number of numerical data processors (NDPs) with one 8086 central processing unit (CPU), thus overcoming the throughput bottleneck imposed by normal design constraints.

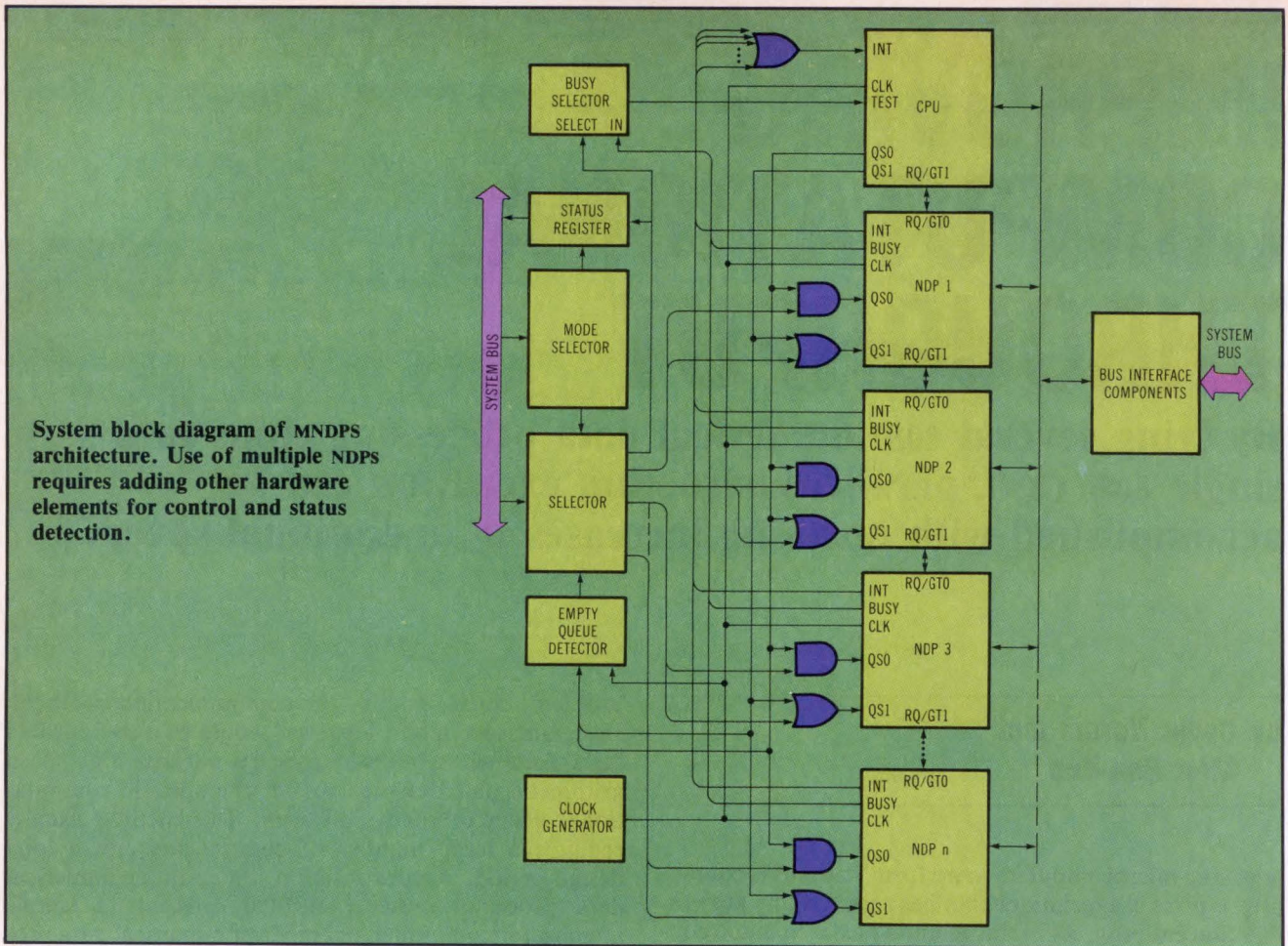
System features and architecture

The MNDPS has several main features. First, there are four modes of NDP operations.

- *Mode 0* is the conventional iAPX 86/20 operation mode with any one of the 8087s specified to be active, while others remain idle
- *Mode 1* is when all NDPs perform in parallel on the same operation using different data
- *Mode 2* is when NDPs work in an automatic cyclic mode
- *Mode 3* is when NDPs work in a prescribed order, which can be arbitrarily modified by the program

In addition, different instructions can be executed concurrently. Bus arbitration between the CPU and the NDPs is automatically performed without additional hardware. The instruction set required for programming MNDPS remains essentially the same as that of the iAPX 86/20. Only two additional instructions exist, neither of which is required when the system operates in modes 1 and 0. One is used in mode 2, both in mode 3. Finally, all the advantageous characteristics of the iAPX 86/20 system with respect to high level languages and development systems remain unchanged, while performance increases.

Although the proposed architecture connects a number of 8087 NDPs to a single 8086 CPU simply, there are two fundamental difficulties in implementing this concept. First, the instruction queue operates in first in,



System block diagram of MNDPS architecture. Use of multiple NDPs requires adding other hardware elements for control and status detection.

first out mode, and whenever an escape instruction (which initiates the 8087 operation) appears somewhere in the queue, neither the exact time of the execution nor the NDP chosen to perform the operation is known. Second, the escape instruction code does not have a special field for addressing the different NDPs of the set. A straightforward solution to these problems would introduce an early detection and direction unit. The architecture shown in the Figure has overcome these implementation difficulties.

In addition to the basic iAPX 86/20 hardware, the proposed system contains an 8087 selector, an 8087 mode selector, an 8087 busy selector, an 8086 empty queue state detector, and a status register. The 8087 selector is controlled by the CPU and has the ability to change the queue status at the inputs to the NDPs. Forcing an empty queue combination in all NDPs except for the one that has to perform the instruction is the key principle. The empty queue combination erases the contents of the queues, thus preventing both execution of the specified instruction and reception of subsequent instructions by the unselected NDPs.

A CPU move instruction that loads data into the NDP selector performs the desired NDP selection. The NDP's queues, normally synchronized with the CPU queue, lose their synchronization due to the execution of the move instruction. Therefore, resynchronization of the queues is required immediately after the execution of the NDP instruction. Resynchronization is accomplished by forcing an empty queue state in the CPU through a jump instruction. The 8086 empty queue state detector identi-

fies this state on the 8086 queue status outputs and then signals the 8087 selector to remove the empty queue combination, thus resynchronizing all the NDPs. Using the move and jump instructions enables an arbitrary selection of the NDPs, economizing execution time.

Additional improvement in computational speed can be achieved in mode 2 by arranging for cyclic NDP selection. This is done by omitting the move instruction and using only the jump instructions. In addition to the synchronization process, executing the jump instruction with the system in mode 2 results in the cyclic selection of successive NDPs. The best results in computational speed and software economy are achieved in mode 1 (whenever this mode is applicable), with all NDPs executing the same instruction in parallel. Such operation requires no additional instructions beyond those used in the conventional mode 0.

All NDPs are connected to a common local bus. Bus arbitration logic, a built-in feature of the NDP, prevents contention on the local bus. Connecting the NDP request/grant pins provides an automatic mechanism for mastering the bus. The highest priority in accessing the bus is given to the last request in the requesting chain.

The busy outputs of the NDPs are routed to the test pin of the CPU by the NDP busy selector, prior to the execution of the NDP instruction. In the parallel mode, all busy lines are Ored and routed to the test pin.

The NDP interrupts are handled with the standard Intel approach. A special status register is included in the system to restore the state of the NDP selector and

NDP mode selector prior to an interrupt. This is necessary since an interrupt acknowledged after the selection of an NDP causes the same effect as a jump instruction—it cancels the NDP selection.

Now that the architectural fundamentals have been described, several applications of the hardware can be discussed. To show the benefits of this hardware configuration operating in several modes, consider a common problem encountered in typical defense applications—the generation of a vector using scalar multiplication.

Scaling a vector

Three types of operation are examined in this example. In case 1, the system is working in the conventional mode (0) with NDP 1 chosen to work as the coprocessor with the CPU host. In cases 2 and 3, the system contains

three NDPs, according to the dimension of the vector to be multiplied. In case 2, the system is working in a combination of modes 3 and 1. Finally, in case 3 a combination of modes 2 and 1 is applied.

Here, advantages and drawbacks to using each of the modes are discussed. Also, the relative gains in time for cases 2 and 3, as compared with case 1, are provided. The following notations are used

$$\bar{a} = (a_1, a_2, a_3) \text{—Vector } \bar{a}$$

b—scalar

$$\bar{c} = b \cdot \bar{a} = (b \cdot a_1, b \cdot a_2, b \cdot a_3)$$

Note that the “wait” instruction is implicitly assumed to precede each NDP instruction. Also, every NDP instruction is characterized by an F prefix.

iAPX 86/20 basic system concepts

The iAPX 86/20^{2,3} is a microcomputer based on two major components—the 8086 CPU functions as the host processor; the 8087 NDP serves as a coprocessor. The coprocessor interface allows specialized hardware to appear as an integral part of the host's architecture, controlled by the host's special instructions. When the host encounters these special instructions, both the host and the coprocessor recognize them and work together to perform the desired function. Connection between the coprocessor and the host is via the local bus lines (ie, address, data, status, clock, ready, reset, test, and RQ/GT).

Once the coprocessor begins operation, the host can continue program execution in parallel. The coprocessor's parallel operation does not normally affect the host unless the coprocessor has to refer to memory. When the host releases the local bus to the coprocessor, it may continue to execute instructions from its internal queue. However, the host must stop when it needs the local bus currently in use by the coprocessor. This parallel operation of host and coprocessor is called concurrent execution. Concurrent execution of instructions requires programs to provide synchronization between the host and the coprocessor.

Synchronization results in either the host or the coprocessor waiting for the other to finish an operation in progress. The host/coprocessor synchronization instruction, called “wait,” uses the host's test pin. The coprocessor can signal to the host via this pin that it is still busy. When the host executes a wait instruction, it stops program execution, while it

checks the test pin for activity. When the test pin becomes inactive, the host resumes program execution with the next instruction following the wait.

Special instructions called “escape” initiate coprocessor operation. The host/coprocessor interface requires the coprocessor to recognize when the host has encountered an escape instruction. Whenever the host begins executing a new instruction the coprocessor must look to see if it is an escape instruction. Since only the host fetches instructions and executes them (except for the execution of the escape, performed by both of them) the coprocessor must monitor the instruction currently being executed by the host. The host can fetch an instruction at a variable length of time before it executes the instruction. In this way the instruction queue of the CPU is formed. An instruction queue allows instructions to be prefetched when the local bus would otherwise be idle. The host does not indicate which instruction it is currently executing. Instead, the host indicates when an instruction is fetched and, later, when it is executed.

To identify the actual instruction that the host fetched from the queue, the coprocessor must also maintain an instruction stream identical to the host's. When the host has filled its queue, it stops prefetching instructions. Instructions are removed from the queue one byte at a time for decoding and execution. When a jump occurs, the queue is emptied. The coprocessor follows the host's actions by monitoring the host's bus status, queue status, and data bus signals (see Tables 1 and 2).

TABLE 1

Queue Status Signals and Their Encoding

QS0	QS1	Host Function	Coprocessor Activity
0	0	No operation	No queue activity
0	1	First byte out of queue	Decode opcode byte
1	0	Empty queue	Empty queue
1	1	Subsequent byte out of queue	Flush byte; if second byte of escape, decode it

TABLE 2

Bus Status Signals and Their Encoding

$\bar{S}2$	$\bar{S}1$	$\bar{S}0$	Function
0	0	0	Interrupt acknowledge
0	0	1	Read input/output port
0	1	0	Write input/output port
0	1	1	Halt
1	0	0	Code fetch
1	0	1	Read data memory
1	1	0	Write data memory
1	1	1	Idle

In case 1 (mode 0), the assembly language program to accomplish vector generation looks as follows

```

MOV MODE-0, AL ; Select mode 0 (NDP1)
FLD DWORD, a1 ; Load a1 into NDP1 stack
FLD DWORD, a2 ; Load a2 into NDP1 stack
FLD DWORD, a3 ; Load a3 into NDP1 stack
FLD ST(0) ; Get a3 from stack
FMUL DWORD b ; Multiply a3 by b, replace on stack
FLD ST(1) ; Get a2 from stack
FMUL DWORD b ; Multiply a2 by b, replace on stack
FLD ST(2) ; Get a1 from stack
FMUL DWORD b ; Multiply a1 by b, replace on stack

```

The fact that every NDP instruction is preceded by a wait implies a serial execution of NDP instructions. Thus, the CPU spends most of its time executing the wait instruction while waiting for the NDP to finish its instruction.

In case 2, the following assembly program is required for operation in modes 3 and 1

```

MOV MODE-3, AL ; Select mode 3
MOV NDP1, AL ; Select NDP1
FLD DWORD a1 ; Load a1 into NDP1 stack
JMP N1 ; Resynchronize
N1: MOV NDP2, AL ; Select NDP2
FLD DWORD a2 ; Load a2 into NDP2 stack
JMP N2 ; Resynchronize
N2: MOV NDP3, AL ; Select NDP3
FLD DWORD a3 ; Load a3 into NDP3 stack
JMP N3 ; Resynchronize
N3: MOV MODE-1, AL ; Select mode 1
FLD ST(0) ; Get a2s from stacks in NDPs
FMUL DWORD b ; A parallel multiplication
; by scalar b in all NDPs

```

Loading vector \bar{a} is done using mode 3, allowing different vector elements to be loaded into different NDPs. The CPU's ability to initiate a new NDP instruction before the previous one is terminated causes the operation to be partially parallel. Multiplication is done in mode 1 (fully in parallel), reducing the execution time of this phase of the algorithm to one-third the time required in case 1. Overall execution time in case 2 is roughly one-half of that required for case 1.

In case 3, mode 2 is selected to load vector data cyclically into different NDPs. Multiplication is done concurrently, as before in mode 1. With each jump instruction, resynchronization and selection of successive NDPs are executed by the hardware in a cyclic mode without addressing the particular NDP. The assembly program for case 3 operation is as follows

```

MOV MODE-2, AL ; Select mode 2
MOV NDP1, AL ; Determine the first NDP
; in the cyclic mode
FLD DWORD a1 ; Load a1 into NDP1 stack
JMP N1 ; Resynchronize and select NDP2
N1: FLD DWORD a2 ; Load a2 into NDP2 stack
JMP N2 ; Resynchronize and select NDP3

```

```

N2: FLD DWORD a3 ; Load a3 into NDP3 stack
MOV MODE-1, AL ; Select mode 1
JMP N3 ; Resynchronize all NDPs
FLD ST(0) ; Get a2s from stacks in all NDPs
N3: FMUL DWORD b ; A parallel multiplication
; by scalar b in all NDPs

```

Overall execution time in this case is slightly less than one-half the time required for case 1 and 15% faster than case 2. This improvement over case 2 results mainly from the economy in software realized by using the jump instruction to synchronize all NDPs.

System performance appraisal

Evaluating MNDPS performance in comparison with the iAPX 86/20 in executing a given algorithm Q can be defined by the following gain ratio

$$\gamma(Q) = \frac{\text{Execution time of Q on iAPX 86/20}}{\text{Minimum execution time of Q on MNDPS}}$$

Minimum execution time in the denominator has to be understood under the conditions of the most convenient partitioning of the algorithm Q into a number of parts, and selection of the optimum mode for each part of Q.

The performance gain $\gamma(Q)$ depends on a number of parameters, such as data loading time from memory to NDP(s) stack; data storing time from NDP(s) to memory; execution time of various arithmetic and stack manipulation operations; minimum time between the execution of consecutive NDP(s) instructions, depending on the mode of operation of MNDPS; and non-overlapping memory access time of NDP(s) working parallel (mode 1).

This proposed system, a simple technique for combining a number of NDPs with one CPU, can operate in several modes. Throughput improvements for a given algorithm depend, to a great extent, on the selection of the proper modes for different parts of the algorithm. In the example of partitioning algorithms in two parts, one with a pronounced serial and the other with a parallel character, the result was clear at the outset. But such partitioning may present quite a complicated task for other, more complex algorithms. In addition, it is conceivable to design the system so that some of the NDPs operate in one mode, while others operate in a different mode. Working out the indicated problems, however, is an ongoing challenge.

References

1. Barthmaier, "Intel Multibus Interfacing," AP-28A, Intel.
2. "The 8086 Family User's Manual," Intel, numerics supplement, July 1980.
3. "Getting Started with the Numeric Data Processor," AP-113, Intel.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 707

Average 708

Low 709

Check The Chart Before You Choose Your New 16-Bit Computer System.

**Columbia Data Products'
New Multi-Personal® Computer,
Featuring IBM-PC® Compatibility,
Excels In Professional, Business
And Industrial Applications.
Check it out.**



Columbia Data Products' MULTI-PERSONAL® COMPUTER can use software and hardware originally intended for the IBM® Personal Computer . . . while enjoying the flexibility and expandability of all Columbia Data's computer systems.

Available operating system software includes single-user MS-DOS® or CP/M 86® or multi-user, multi-tasking MP/M 86® or OASIS-16®, with XENIX® available soon, providing users with a host of compatible software packages for personal and professional business and industrial applications. A large selection of higher level languages are also available, including BASIC, FORTRAN, COBOL, PASCAL and MACRO Assembler.

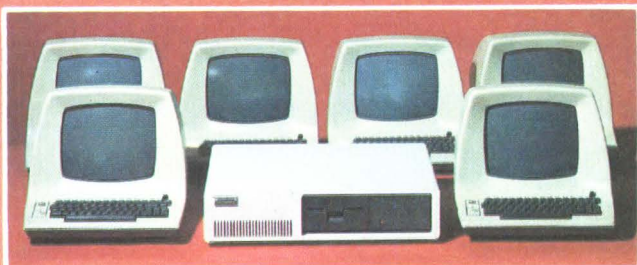
Our standard 16-Bit 8088 hardware configuration provides 128K RAM with parity, two RS-232 serial ports, Centronics parallel printer port, interrupt and DMA controllers, dual floppy disks with 640K storage, Winchester disk and keyboard interfaces, and eight IBM-PC compatible expansion slots . . . and lists for only \$2995. Winchester hard disk configurations, featuring cache buffer controllers for enhanced disk access performance are also available, starting at \$4995.

So, when you need to grow, why gamble and hassle with independent third party hardware and operating system vendors which may or may not be compatible . . . not to mention the hidden expense and frustration of implementing peripheral drivers in the different operating systems and upgrades? Who needs the finger-pointing when things don't work out?

After you review our chart, you will agree . . . for overall 16-Bit microprocessor superiority, expandability, flexibility, compatibility and real economy, Columbia Data is your *total source*.

Our Multi-Personal Computer . . . the 16-Bit system born to grow!

Get yours now.



MAIN FEATURES	CDP-MPC	IBM-PC*	OTHERS
Microprocessor	16-Bit 8088 8-Bit Z-80 (Opt)	16-Bit 8088	?
USER Memory	128K-1 Mbytes	16K-256 Kbytes	?
IBM-PC Compatible Expansions Slots Beyond Professional Configuration ¹	8 Slots	0	?
Resident Floppy Disk Storage	Dual 320K (std)	Dual 160K (Opt) Dual 320K (Opt)	?
Resident Cache Buffer			
Hard Disk Storage	5M/10M	—	?
OPTIONAL OPERATING SYSTEMS (Supported by Company)²			
MS-DOS (PC-DOS)	Yes	Yes	?
CP/M 86	Yes	Yes	?
MP/M 86	Yes	—	?
OASIS-16	Yes	—	?
XENIX	Soon	—	?
OPTIONAL HARDWARE EXPANSION BOARD (Supported by Company)			
RS-232 Communications	Yes	Yes	?
B/W and Color Display Controller	Yes	Yes	?
Expansion Memory	Yes	Yes	?
Z-80 CP/M-80 Board	Yes	—	?
Cache Buffer Hard Disk	Yes	—	?
Time/Calendar Board	Yes	—	?
IEEE Bus Controller	Yes	—	?
8" Floppy Disk System	Yes	—	?
8" Hard Disk System	Up to 40 Mbytes	—	?
Tape Cartridge System	Yes	—	?

¹For comparison purposes, typical professional configurations consist of 16-Bit 8088 Processor, 128K RAM with Parity, Dual 320K 5-inch Floppies, DMA and Interrupt Controller, Dual RS-232 Serial Ports, Centronics Parallel Port and Dumb Computer Terminal or Equivalent.

²Columbia Data Products also supports CP/M 80® with an optionally available Z-80 CP/M Expansion Board.

*As advertised in BYTE Magazine, August 1982.

COLUMBIA
DATA PRODUCTS, INC.

Home Office:
8990 Route 108
Columbia, MD 21045
Telephone 301-992-3400
TWX 710-862-1891

West Coast:
3901 MacArthur Blvd.
Suite 211
Newport Beach, CA 92663
Telephone 714-752-5245
Telex 277778

Europe:
P.O. Box 1118
450 Moenchengladbach 1
West Germany
Telephone 02161-33159
Telex 852452



TELEVIDEO SYSTEMS INC PRESENTS THE 970

ANSI 3.64

256 DOWNLOADABLE FONT

14" SCREEN

VT-100 COMPATIBLE

92 NON-VOL. FUNCT. KEYS

ACCOUNTING KEYPAD

24 X 132 COLUMN

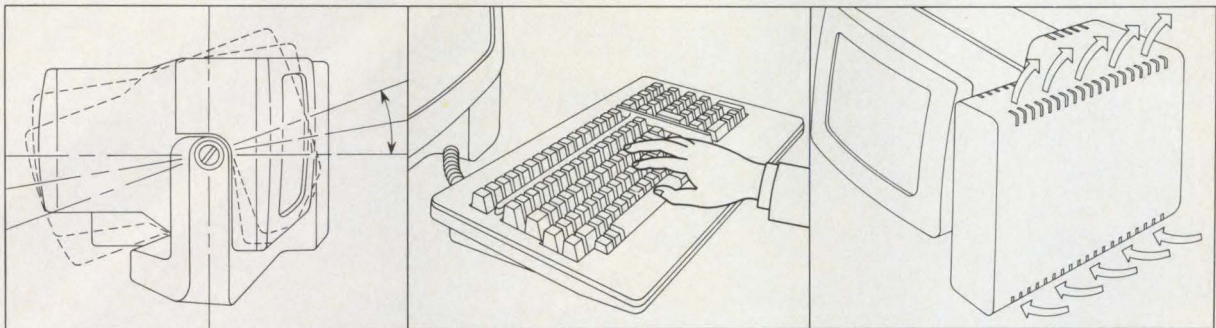
NO SPACE ATTRIBUTES-16

LOGICAL ATTRBS.

TELEVIDEO 970

TeleVideo
MODEL 970

The new 970 from TeleVideo. Nothing else looks like it. Nothing else performs like it.



Productive office work depends on people and their equipment working efficiently together.

That's why we have engineered the exciting, new TeleVideo 970 to perform better than any other terminal.

For instance, only our "natural balance" tilting mechanism lets you easily adjust the screen at a touch, so you avoid neck-craning, straining and glare.

Our unique keyboard is designed to avoid user fatigue. We've created a natural palmrest, sculpted keys and the best ten-key accounting pad in the industry. Our non-volatile function keys save time and energy.

Like every feature of the new 970, the screen is designed for ease of use. Our non-glare 14-inch green screen is restful on the eyes, and its 132 column display can format more information. All in highly legible double-high, double-wide characters.

Our communications protocol is the industry standard ANSI 3.64.

As you probably know, most terminal downtime is caused by overheating that results from extended use. There's no such problem with our unique vertical convection cooling tower.

And because we wanted to extend the life of your CRT, we've installed a screen saving

feature that automatically turns it off after fifteen minutes of idle time.

Naturally, like all TeleVideo terminals, service is available nationwide from General Electric's Instrumentation and Communication Equipment Centers.

The new 970 from TeleVideo. Nothing else looks like it and nothing else can perform like it.

For more information about TeleVideo's new 970, call 800-538-8725; in California 408-745-7760.

TeleVideo Systems, Inc.
Dept. #219D
1170 Morse Avenue
Sunnyvale, CA 94086

Yes, I'd like to know more about the unique 970 from TeleVideo:

NAME _____

ADDRESS _____

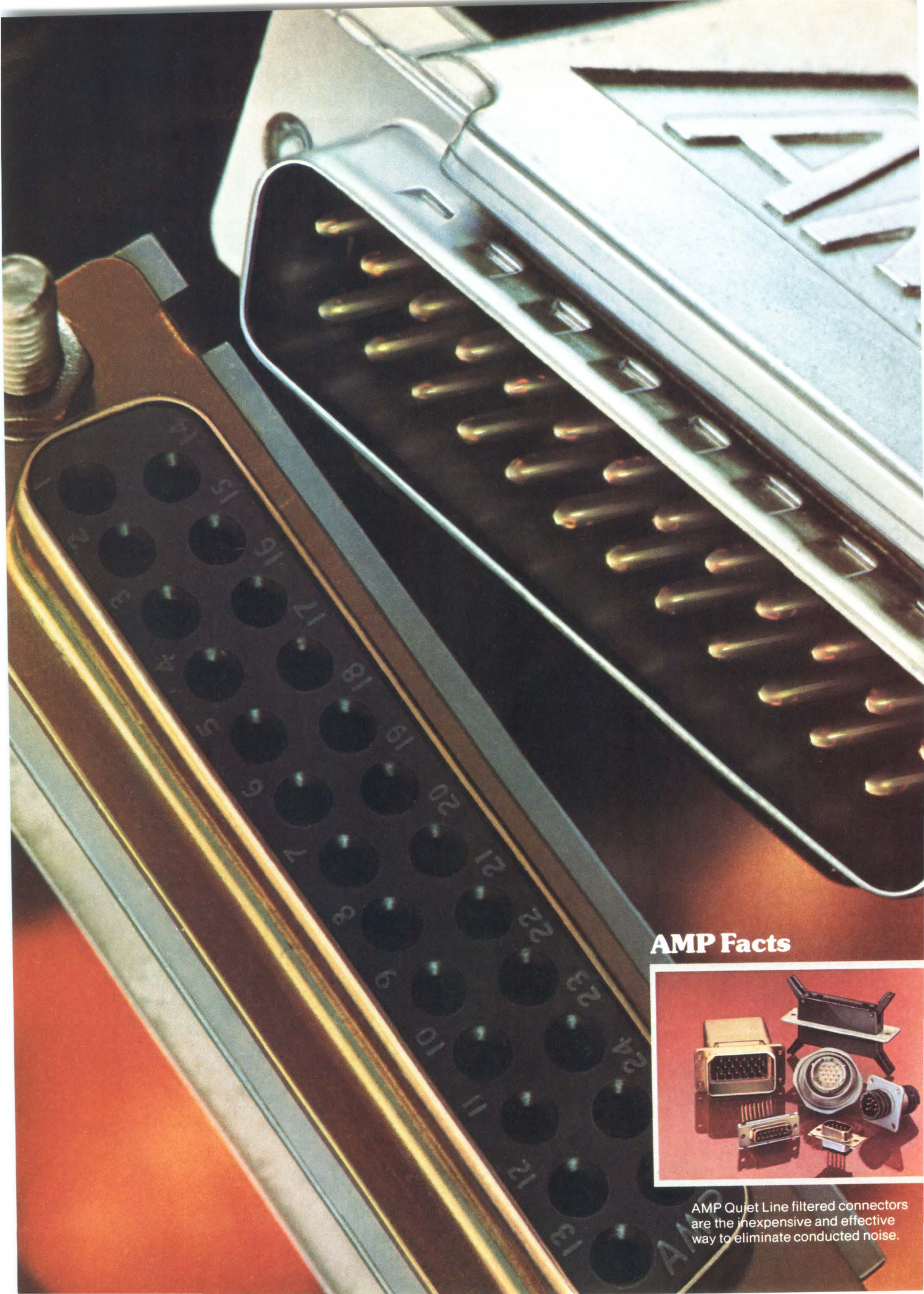
CITY _____

STATE _____ ZIP _____

TELEPHONE (_____) _____

California/Santa Ana 714-557-6095; Sunnyvale 408-745-7760, Georgia/Atlanta 404-255-9338; Texas/Dallas 214-980-9978; Illinois/Chicago Area 312-351-9350; Boston/Massachusetts 617-668-6891; New York/New Jersey 201-267-8805; United Kingdom/Woking, Surrey 44-9905-6464.

 **TeleVideo Systems, Inc.**



AMP Facts



AMP Quiet Line filtered connectors are the inexpensive and effective way to eliminate conducted noise.

COST-EFFECTIVE QUIET.

AMP filtered and shielded connectors stop EMI coming and going.

Electromagnetic crackles, blips and zaps can scramble a computer's memory, garble communications and destroy IC's. And for years, AMP has been applying uncommon talents to solving this common problem.

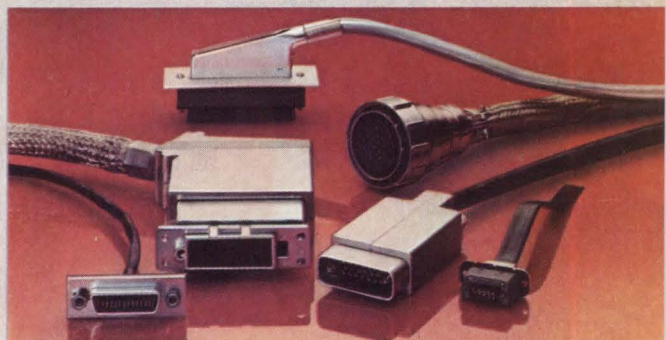
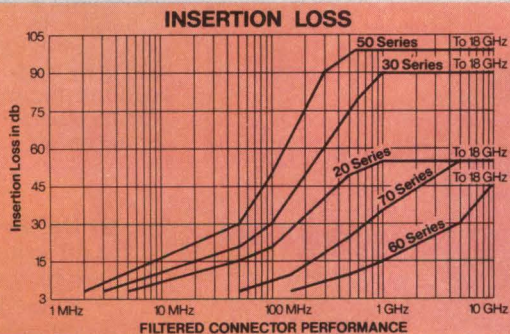
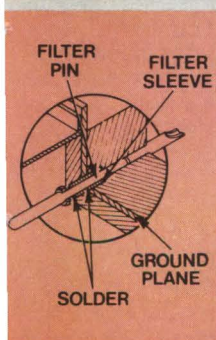
To help ensure your own system doesn't radiate noise that FCC regulations forbid, we can now supply shielded versions of connectors that are the standards of the industry. In every size and style you might need, including high density, subminiature and circular types. And they're all designed to deliver the plus performance you expect from AMP.

The AMP attack on EMI goes beyond shielding to stop conducted interference as well. Unique one-piece filter contacts built into AMP connectors absorb and dissipate noise, letting only pure signals through, often eliminating the need for special cables and auxiliary filter circuits.

You get this premium performance with termination economies that AMP has pioneered for half a century.

For complete shielded and filtered facts, call the AMP Information Desk at (717) 780-4400. AMP Incorporated, Harrisburg, PA 17105.

AMP means productivity.



You can choose the insertion-loss vs. frequency characteristics you need.

CIRCLE NUMBER
10

A complete range of shielded styles, including post/receptacle configurations.

“Amphenol gives me a low-cost standard circular connector. And lets me choose crimp or solder.”

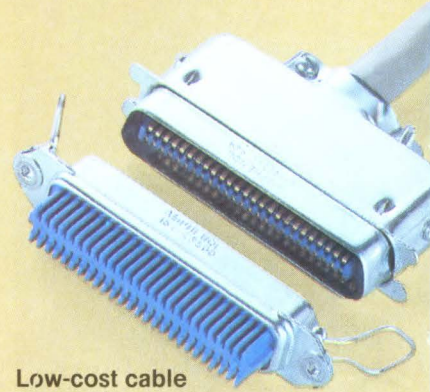
The new crimp-type 97 Series connector gives you faster termination. It is designed to the same MIL-C-5015 A and B performance specifications as the popular solder-type 97 Series. Both are commercially priced.

Use either solder or crimp in computers, business equipment, instrumentation, communication

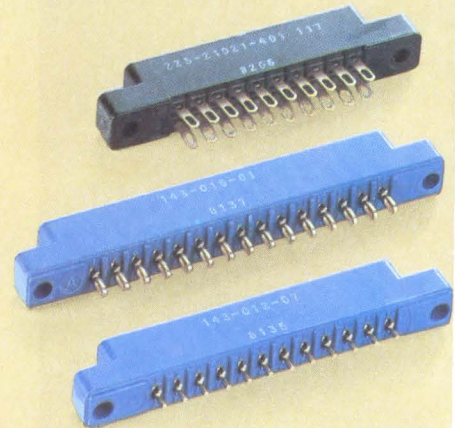
equipment, machine tools, industrial controls, transportation, servos, robotics, welding equipment—the list goes on and on.

Both types are intermateable and intermountable with each other and with all other connectors with MIL-C-5015 shells and insert configurations.

More connector ideas from Amphenol



Low-cost cable to panel connectors—intermateable, intermountable
Solder-type 57 Series and solderless 157 Series connectors. Ideally suited for modems, multiplexers, computers, peripheral, medical equipment, PBX devices, instrumentation, vending machines and conventional telephone equipment.
Circle Reader Service Number 91



Broad range of printed circuit connectors—commercial, industrial, military
Wide variety of plating, mounting, contact and tail configurations. Useful in computers, data terminals, data printers, CRT displays, modems, industrial controls, instrumentation, signal equipment, security systems, telecommunications and medical equipment.
Circle Reader Service Number 92

97 Series
Left, crimp-type;
right, solder-type.
Circle Reader Service
Number 171



MIL-C-38999 Type circular filter connector

The 418F Series connector provides protection against RFI, EMI and EMP in stringent environments: shock, vibration, temperature extremes, moisture, corrosion. Used in military and commercial aerospace systems, industrial process control, data processing, communications and navigation systems.

Circle Reader Service Number **93**

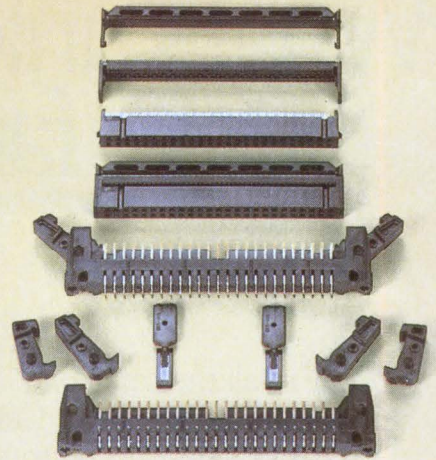


Circular fibre optic connectors for multi-channel applications

Four- or eight-channel 801 Series connectors for small diameters ranging from 125 microns for single fibres to 1100 microns for multifibre bundle diameters.

Useful in computers, aerospace, instrumentation, commercial, laboratory and industrial equipment.

Circle Reader Service Number **95**



Spectra-Strip® IDC sockets and headers—meet MIL-C-83503 requirements

812/816 Series are just part of the Amphenol® broad line of mass-termination connectors for computers, peripherals, instrumentation and communications equipment. Types available to meet requirements ranging from low-cost commercial applications to high-performance military applications.

Circle Reader Service Number **96**

Low-cost environmental connectors

Inexpensive quick-connect-and-disconnect 44 Series connectors. Valuable for automotive, truck and off-highway vehicles. Also for traffic control systems, marine and mining electrical/electronic systems.

Circle Reader Service Number **94**

These are only a few examples of Amphenol® and Spectra-Strip® products available worldwide. For more information, contact your nearest sales office or distributor.

Amphenol

An **ALLIED** Company

Amphenol World Headquarters: 2122 York Road, Oak Brook, Illinois 60521

Sales Offices: Atlanta (404) 394-6298 • Boston (617) 475-7055, (617) 938-8580 • Boulder (303) 443-4780 • Chicago (312) 986-2330 • Dallas (214) 343-8420 • Dayton (513) 294-0461 • Denver (303) 934-2355 • Detroit (313) 722-1420 • Greensboro (919) 292-9273 • Houston (713) 444-4096 • Indianapolis (317) 842-3245 • Kansas City, Mo. (816) 737-3937 • Knoxville (615) 690-6765 • Los Angeles (213) 532-3180 • Miami (305) 981-2100 • Milwaukee (414) 542-9566 • Minneapolis (612) 835-4595 • New York (516) 364-2270 • Orlando (305) 678-5504 • Philadelphia (215) 732-1427 • Phoenix (602) 265-3227 • St. Louis (314) 569-2277 • Salt Lake City (801) 364-6481 • San Diego (714) 272-5451 • San Francisco (408) 732-8990 • Seattle (206) 455-2525 • Syracuse (315) 455-5786 • Washington, D.C. (703) 524-8700
Canada: Montreal (514) 482-5520 • Toronto (416) 291-4401 • Vancouver (604) 278-7636
International: Oak Brook, Illinois TELEX 206-054

DISTRIBUTORS (A = Amphenol, S = Spectra-Strip)

ALABAMA
Hall-Mark, Huntsville—(205) 837-8700—A

ARIZONA
Bell, Tempe—(602) 966-7800—S
Cetec, Phoenix—(272) 7951—A/S
Kierulff, Phoenix—(602) 243-4101—A

CALIFORNIA
Bell, Gardena—(213) 515-1800—S
Bell, Sunnyvale—(408) 734-8570—A/S
Cetec, South Gate—(213) 773-6521
San Diego—(714) 278-5020
San Jose—(408) 263-7373—A/S
Ei-Com, Cerritos—(213) 926-7887
San Diego—(714) 578-0906—S
Kierulff, Los Angeles—(213) 725-0325
San Diego—(714) 278-2112—A
Schweber, Irvine—(714) 556-3880—A
Western Electromotive, Santa Clara—(408) 727-7411—A
Wyle, El Segundo—(213) 322-8100
San Diego—(714) 565-9171
Santa Clara—(408) 727-2500—A

COLORADO
Bell, Wheat Ridge—(303) 424-1985—S
Kierulff, Denver—(303) 371-6500—A
Newark, Denver—(303) 757-3351—A
Storm Products, Broomfield—(303) 466-1991—S
Wyle, Thornton—(303) 457-9953—A

CONNECTICUT
Connector Company, Hamden—(203) 288-0044
Harvey, Norwalk—(203) 853-1515—A
Marshall, Wallingford—(203) 265-3822—A

FLORIDA
Arrow, Palm Bay—(305) 725-1480—A
Kierulff, St. Petersburg—(813) 576-1966—A
KSM Electronics, Ft. Lauderdale—(305) 739-5880—S
Schweber, Hollywood—(305) 921-0301—A

GEORGIA
Arrow, Norcross—(404) 449-8252—A
Hall-Mark, Norcross—(404) 447-8000—A

ILLINOIS
Electronic Connector, Chicago—(312) 767-2200—A

GBL/Goold Electronics, Elk Grove Village—(312) 593-3220—S
Kierulff, Elk Grove—(312) 640-0200—A
Klaus Radio, Peoria—(309) 691-4840—A
Newark, Chicago—(312) 638-4411—A/S
Ohm, Palatine—(312) 359-5500—A/S

INDIANA
Genesis, Indianapolis—(317) 637-5571—S
South Bend—(219) 287-2911—A
Graham, Indianapolis—(317) 634-8202—A

KANSAS
Wichita Aircraft, Wichita—(316) 838-1421—A

MARYLAND
Arrow, Baltimore—(301) 247-5200—A
Hall-Mark, Baltimore—(301) 796-9300—A
Pioneer, Gaithersburg—(301) 948-0710—A
Vertex Electronics Mid-Atlantic, Inc., Beltsville—(301) 937-0180—S

MASSACHUSETTS
Gerber, Norwood—(617) 769-6000—A/S
Industrial Components, N. Wilbraham—(413) 596-3854—A
Kierulff, Billerica—(617) 935-5134—A
Marshall, Burlington—(617) 272-8200—A
Pacer Electronics, Woburn—(617) 935-8330—S
OPL Electronics Distributors, Burlington—(617) 229-2424—S
Schweber, Bedford—(617) 275-5100—A

MICHIGAN
Ambur Electronics, Walled Lake—(313) 669-3710—S
Madison, Roseville—(313) 778-7640—A
RS Electronics, Livonia—(313) 525-1155—A
Wedemeyer, Ann Arbor—(313) 665-8611—A

MINNESOTA
Arrow, Edina—(612) 830-1800—A
Custom Connections, Burnsville—(612) 894-4090—S
Kierulff, Edina—(612) 941-7500—A
Newark, Minneapolis—(612) 331-6350—A

MISSOURI
L-Comp, Kansas City—(816) 221-2400
Maryland Heights—(314) 291-6200—S
Olive Industrial Electronics, St. Louis—(314) 426-4500—A/S
Walters Radio Supply, Kansas City—(816) 531-7015—A

NEW HAMPSHIRE
Yankeo Electronic Supply, Manchester—(603) 625-9746—S

NEW JERSEY
Harvey Electronics, Pinebrook—(201) 227-1262—A
Marshall Electronics, Fairfield—(201) 882-0320—A
Radio Electric Services, Pennsauken—(215) 925-6900—A
Schweber, Fairfield—(201) 227-7880—A

NEW MEXICO
Bell, Albuquerque—(505) 292-2700—A
Connecting Components, Albuquerque—(505) 345-8921—S

NEW YORK
Arrow Electronics, Farmingdale—(516) 231-1030—A/S
ASI Electronics, Endwell—(607) 754-3823—A
Genesee Radio Parts, Buffalo—(716) 873-9661—A
Harvey Electronics, Binghamton—(607) 748-8211, Woodbury—(516) 921-8920—A
Help Electronics, Binghamton—(607) 729-3528—S
Progress Electronics, Plainview—(516) 433-1700—A
Schweber, Westbury—(516) 334-7474—A/S
Simcona Electronics, Rochester—(716) 328-3230—A
Summit Distributors, Buffalo—(716) 887-2800—A/S
Vertex Electronics, Farmingdale—(516) 233-9880—S

NORTH CAROLINA
Arrow, Winston-Salem—(919) 725-8711—A
Hammond Electronics, Greensboro—(919) 275-6391—S

OHIO
Pioneer, Cleveland—(216) 587-3600
Dayton—(513) 236-9900—A
Schuster Electric, Cincinnati—(513) 489-1400—A/S
Twinsburg—(216) 426-8134—S
Schweber, Beachwood—(216) 464-2970—A
Stotts Friedman, Dayton—(513) 298-5555—A/S

OKLAHOMA
Electro Enterprises, Oklahoma City—(405) 478-1752—A

OREGON
Bell Industries, Lake Oswego—(503) 241-4115—A

PENNSYLVANIA
Almo Electronics, Philadelphia—(215) 698-4000—A
CAM/RPC, Pittsburgh—(412) 782-3770—A/S
Omega Wire & Cable, Harleysville—(215) 247-7820—S
Pytronic, Montgomeryville—(215) 643-2850—A/S

TEXAS
Allied Electronics, Ft. Worth—(817) 336-5401—A/S
Altair, Richardson—(214) 231-5166
Houston—(713) 462-3029—S
Hall-Mark, Dallas—(214) 343-5000—A
Harrison Equipment, Dallas—(214) 239-2750
Stafford—(713) 879-2600—S
Kierulff, Dallas—(214) 343-2400—A
Solid State Electronic Company, Irving—(214) 438-5700, Houston—(713) 772-8483—S
Southwest Electronics, Stafford—(713) 491-4900—A
Sterling, Dallas—(214) 245-1600
Houston—(713) 627-9800—A

UTAH
Diplomat, Salt Lake City—(801) 486-4134—A/S
Standard Supply, Salt Lake City—(801) 486-3371—S

WASHINGTON
Bell Industries, Bellevue—(206) 747-1515—A
Carlyle Technical Sales, Seattle—(206) 575-6750—S
Wyle, Bellevue—(206) 453-8300—A

WISCONSIN
Electronic Expeditors, Milwaukee—(414) 228-8100—A
Taylor Electronic Company, Mequon—(414) 241-4321—S

CANADA
Distributors in major cities

What's unique about the GE 3000 printer family is its commonality.

"They're all the same only different." That's the simple advantage of General Electric's new GE 3000 series of printers...single design simplicity without the application limitations of a single model product line.

Our basic concept is application driven price/performance matching. Choose speeds from 40 to over 400 cps. Single or dual mode printing. Type quality from EDP to NLQ. Multi-color printing. Graphics. 80 and 136 column models. Selectable type fonts. Accessible, easily programmable set-up by either the operator or the system. Multi-model flexibility...all with high parts commonality.

Now, you can stock just one line of printers, yet meet a diversity of needs. Enjoy every advantage of single source supply. With each printer backed by General Electric's worldwide service.

Take a close look at any of the GE 3000 printers. You'll find they're easy to use, lightweight, functionally styled, reliable tabletop matrix printers. And when you take the entire GE 3000 series altogether, they stack up beautifully compared to everything else on the market today.

General Electric. We introduced the first fully electronic printer with LSI circuitry in 1969. And our complete line today makes us the industry leader you should look to first.



First In Electronic Printing.

For the solution to your printing needs, call
TOLL FREE 1-800-368-3182

General Electric Company, Data Communication Products Department B321, Waynesboro, VA 22980. In Virginia, call 1-703-949-1170.

GENERAL  ELECTRIC

SPECIAL REPORT ON

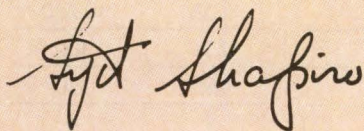
DATA COMMUNICATIONS SYSTEMS DESIGN

Baseband, broadband, star, tree, ring, CSMA/CD, CSMA/CA, token passing: all these and more are the current buzzwords related to local area networks (LANs). A host of manufacturers have chosen varying topologies as the bases for their LANs, while designers differ in their preferences for protocols. And, where some systems are designed to use coaxial cable, others use twisted pair wires or even fiber optics as their media. Furthermore, although many systems are mutually compatible, many more are not. Therefore, the potential user must somehow make a choice—and stick with it. But, how is the user to decide which is best? Even more relevant, which manufacturers will still be in business 10 or 15 years from now? Will future systems be compatible?

Does all this benefit the user? It is doubtful. Are all the varied topologies and protocols truly significant? Probably, yes. Yet, the user still suffers from the lack of firm standards. To aid the designers of still “in concept” data communication systems, a review article in this issue explains the debates between network suppliers and illustrates how at least a part of the scene is slowly coming into focus.

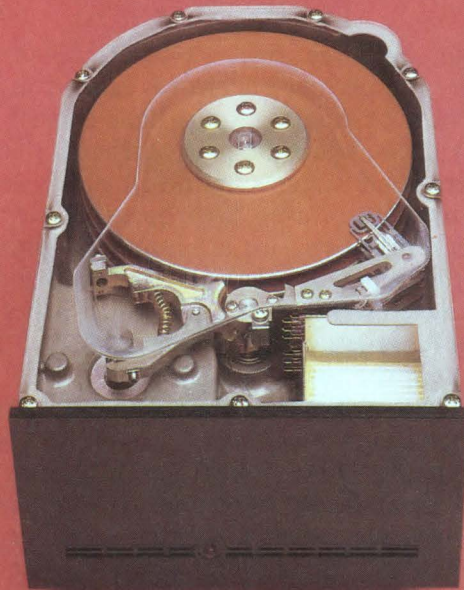
Complementing that staff written report are several other data communication articles from actual system designers, manufacturers, and users. Understandably, these articles argue for particular concepts. Yet, each in itself presents an important alternative.

Again, it is the designer's choice. Only that person can weigh all of the values, both positive and negative, involved in such decisions. We have presented much of the basic information—but the designer needs even more. Further details are available to the data communication system designer in National Bureau of Standards reports, in detailed studies by research organizations, and in the proceedings of relevant conferences. It's all there to find.



Sydney F. Shapiro
Managing Editor

It's like every
other 5¼-inch
disk drive.
Except
it's a Fujitsu.



Our competitively priced 5¼-inch Winchester has features as advanced as any disk drive available. LSI circuitry. Seek optimization. A choice of two interfaces. And three capacities. But beyond these features you will find the experience, the support, and the trust that are identified exclusively with the name Fujitsu. So the first time, you might specify our 5¼-inch disk drive for its features. The second time, it will be for the name. 

MODEL	M2231	M2233	M2234
CAPACITY (MB)	6.7	13.3	20.0
AVG. POSITIONING TIME (ms)	95	95	95
TRANSFER RATE (KB/s)	625	625	625
INTERFACE	ST506/SA4000		
AVERAGE LATENCY (ms)	8.3	8.3	8.3
RECORDING DENSITY (BPI)	8,020	10,200	10,200
TRACK DENSITY (TPI)	254	300	300
NUMBER OF CYLINDERS	160	320	320
NUMBER OF DATA HEADS	4	4	6
POSITIONING METHOD	Buffered Stepper		
DIMENSIONS (HxWxD in.)	3.3x5.7x8.0		

Fujitsu America Sales Offices:
Northwest 408/988-8100 Southwest 714/558-8757
East Coast 617/229-6310 Europe 44-1/493-1138



QUALITY LIVES



Special report on data communications systems design

- 159 Untangling local area networks**
by Richard Parker and Sydney F. Shapiro—Competing local area networking schemes offer diverse characteristics that may or may not fit your specific application. But the issues are becoming clearer and standards are emerging.
- 175 Single-chip modem slashes space requirements**
by Kerry A. Hanson—Among advancements in LSI modem chips is a single-chip frequency shift keying modem that provides full communication functions at 300 bps.
- 183 In praise of ring architecture for local area networks**
by Howard C. Salwen—Incorporating the concept of wire centers and the wonders of fiber optics into a ring configured LAN eliminates the traditional bugaboos associated with circular network schemes.
- 195 Bit oriented data link controls**
by Alan J. Weissberger—A bit oriented approach to network control is finding increased acceptance among many national and international standards organizations. The simplicity of the single-frame format is just one reason.
- 209 Broadband network design: issues and answers**
by Edward B. Cooper—Building a broadband local area network involves more than determining cable runs and calculating gain levels. The crucial work lies in the preliminary planning.

ACCES™

“We’ve got what makes the difference in Local Area Networking...”



The ACC Exchange System (ACCES) is a product umbrella that incorporates a comprehensive approach for truly distributed networks.

ACC Knows Networking. For over a decade, ACC personnel have set the pace in network product development. Beginning with the ARPANET, ACC has designed and developed a broad range of high performance network access equipment for packet switched and local area networks.

It is this experience that makes the difference in our approach.

Everyone agrees that Local Area Networking is good. But no one seems to agree on much else. Coax versus twisted

pair. Baseband versus broadband. Token ring versus random access. The list goes on and on. Our experience, however, has taught us that low level features are only a small part of a functioning network.

The ACCES Approach. Most Local Area Network products today are hardware solutions at the lowest networking levels. Before LANs can become truly useful, network users need to have higher level functions at their fingertips. The ACCES approach provides network services through the upper layers of the OSI model. By following the layered model, the ACCES product line does not rely on specific low level implementation (baseband, broadband, etc).

The ACCES Product Line. Some of the products under the ACCES umbrella:

- Intelligent Ethernet front ends (UNIBUS and VERSAbus)
- X.25/Ethernet Bridge
- IBM Channel/Ethernet interface
- Baseband/Broadband Converter
- Xerox Network Systems (NS) communications protocol package
- LAN industry news, over your terminal and modem, dial up On-Line Information at (408) 475-7940. And it's free.

If you'd like more information on the ACCES approach and product line, call us. Today. (408) 425-0937.

ACC LOCAL AREA NETWORK CENTER

Associated Computer Consultants
Local Area Network Center
2901 Park Avenue
Soquel, CA 95073
TWX 910 334-4907
(408) 425-0937

ACCES is a trademark of Associated Computer Consultants.
UNIBUS is a registered trademark of Digital Equipment Corporation.

© ACC 1982



UNTANGLING LOCAL AREA NETWORKS

Competing local area networking schemes offer diverse characteristics that may or may not fit your specific application. But the issues are becoming clearer and standards are emerging.

by **Richard Parker, Contributing Editor and Sydney F. Shapiro, Managing Editor**

Despite the seemingly endless debates between baseband and broadband local area network suppliers, the local area network scene is coming into sharper focus. Both sides, each claiming superiority, use two totally different techniques. Broadband uses a carrier technique to support many different services, while baseband uses a single signal (information channel) to transmit information. Nearly completed local area network standards, international agreement on several networking issues, and a proliferation of integrated circuit and integrated circuit based interface products are hastening the application of local area networks.

Potential local area network (LAN) users are discovering that, contrary to manufacturer exhortations, both baseband and broadband LANs are required to address vastly different needs, even though some performance overlap exists between the types of networks. Furthermore, baseband and broadband networks are not the only games in town. Existing and newer installations of private area branch exchanges (PABXs) are proving perfectly viable for networking applications and are starting to contend for many LAN applications. The result—the user has an ample choice of network hardware and software offerings.

Much of the activity in LANs is centered on cutting the cost of network interfacing through very large scale integration (VLSI) implementation, a development that necessitates some measure of standardization to be viable. Fortunately, such standards are forthcoming. Concurrently, LAN manufacturers are improving the performance of their products by offering more versatile workstations, terminals, and software packages, all designed specifically for local networking applications, and largely consistent with emerging LAN standards. Those standards are coming out of the IEEE 802 Committee (see the Panel).



The PLAN 4000 community microcomputing system simultaneously links up to 255 users of personal computers into a sophisticated and powerful business system.

More support for standards

In December of last year, 13 electronics companies: Bridge Communications Inc (Cupertino, Calif); Data General Corp (Westboro, Mass); Fujitsu America Inc (Santa Clara, Calif); Hewlett-Packard Co (Palo Alto, Calif); Interlan Inc (Chelmsford, Mass); Intel Corp (Santa Clara, Calif); National Semiconductor Corp (Santa Clara, Calif); Siemens AG (Munich, W Germany); 3Com Corp (Mountain View, Calif); Ungermann-Bass Inc (Santa Clara, Calif); Xerox Corp (Palo Alto, Calif); Tektronix Inc (Beaverton, Ore); and Digital Equipment Corp (Maynard, Mass); endorsed P802.3, an emerging IEEE 802 standards proposal, as a single worldwide standard. Eventually, this development

The IEEE 802 Committee

The IEEE Standards Project 802 was established by the IEEE Computer Society in February 1980, under the chairmanship of Maris Graube of Tektronix Inc. Its purpose is to standardize as much of the means of connecting digital computer equipment and peripherals within a local environment as possible. This standardization process is unfolding within the constraints of present and projected LAN hardware and software technologies. The term local area covers local settings such as office buildings, several closely spaced buildings, and campuses, usually denoting a geographic distance of not much more than a few miles.

The driving force for the committee's work is the belief that a single LAN standard (in the ideal case) will benefit equipment manufacturers, by allowing them to mass produce their wares (and thus theoretically offer them at lower prices). A single standard will also aid equipment users who would benefit from the resulting simplicity and low cost of the equipment they can apply. In addition, system designers will benefit by being allowed to specify standard products.

In reality, though, conflicting manufacturer, designer, and user requirements have not made it possible for the IEEE 802 Committee to come up with a single standard that suits all. Remember that the hundreds of IEEE 802 Committee members represent a wide range of interests. For example, those from real-time process control industries are much more concerned with determining the time it takes a message to go from one node on a network to another than those from office automation circles. Thus, the former group would want a network accessing scheme highly deterministic in nature—much like that of token passing—instead of the simpler and less expensive CSMA/CD accessing scheme favored by the latter group.

The committee has had to contend with varying requirements and has taken the route of standardizing on more than one LAN approach. It is attempting, however, to structure these standards in

such a manner that the drawbacks inherent in more than one standard (ie, limited manufacturer production runs, high equipment costs, more complex equipment to apply) are minimized.

The committee is working on standards that govern the interrelationship of computers and peripherals within a network, as well as from one network to another. It is also examining standards for networks that support such applications as file transfers, digital voice and data transmissions, graphics applications, word processing, electronic mail, video, process control, and accessing of remote data bases, all under a set of accessing protocols. As can be seen from these many different applications, data exchange over the network is different for each application, from short data bursts of large messages, to frequent data transfers of small messages, to massive amounts of data being transferred continuously, as in the case of mainframe computer to mainframe computer applications.

The IEEE 802 Committee has attempted to standardize on three media accessing schemes: CSMA/CD, and token passing for both bus and ring topology networks. It has also included within its standards proposals such media as twisted pair wiring, both baseband and broadband coaxial cable, and fiber optic cable.

Draft A, the first draft of the 802 Standard, was completed in May 1981, when it was presented to the IEEE 802's parent committees: the Technical Committee on Computer Communications of the IEEE Computer Society, and the Computer Standards Committee of the IEEE Computer Society. As with any draft proposal, the committee reviewed and modified it as needed. Thus, by October 1981, Draft B was completed and by May of 1982, Draft C was done. At its October 1982 meeting, the committee reviewed Draft C and proceeded to produce a final version of the 802 proposed standard in a December 1982 meeting. The 802 parent committees are now in possession of that document which should, possibly this year, become a full-fledged official LAN standard.

will permit intercommunication between computers and office equipment, regardless of brand. This proposal, a carrier sense multiple access/collision detection (CSMA/CD) network accessing standard, represents a convergence of the IEEE 802 Committee's working drafts, Xerox Corp's Ethernet LAN specifications, and European Computer Manufacturers Association documents, with no substantial differences.

The IEEE 802 Committee has just finished wrapping up proposals for LAN standards under three major categories: P802.3 for CSMA/CD accessing on a bus topology, P802.4 for token passing accessing on a bus topology, and P802.5 for token passing accessing on a ring topology. CSMA/CD and token passing accessing, as well as bus and ring topology networks, represent the major LAN implementations within the IEEE 802 Committee's efforts. The Committee has also standardized the use of twisted pair wiring, as well as baseband and broadband coaxial cable.

Under the P802.3 proposals for coaxial cable media, both baseband (single-channel) and broadband (multi-channel) operations are considered. In the former case, four data speeds of 1M, 5M, 10M, and 20M bps are considered, while under the latter case, 10M-bps speeds are considered, at 6-MHz wide channels. Note that the 10M-bps speed for baseband LANs is the same as Xerox's Ethernet *de facto* industry standard baseband LAN.

Under the P802.4 proposals for token passing bus networks, broadband operation for coaxial cable media is spelled out at the T1 (telephone standard) rate of 1.544M bps, within both 4-MHz wide and 6-MHz wide channels. Also spelled out are data rates of 5M bps within 6-MHz wide channels, 10M bps within 6-MHz wide channels, and 10M and 20M bps within 12-MHz wide channels. For token passing bus networks operating at baseband frequencies over coaxial cable media, data rates of 5M and 10M bps are specified.

Introducing the Series 100 statistical multiplexors from DCA. So versatile, you may never have to replace them. And so reliable, you'll never want to.

Each Series 100 unit is engineered to expand with your network. The System 110 with 2-to-8-port capacity can be upgraded to a System 120 with 32-port capacity. The System 120 can be upgraded to a System 125 multidrop master.

Both Systems 110 and 120 can serve as slaves to the System 125 and can be multidropped along a single telephone line wherever terminals are clustered.

Further, since all DCA products are compatible, your Series 100 statistical multiplexor can grow to become a Series 300



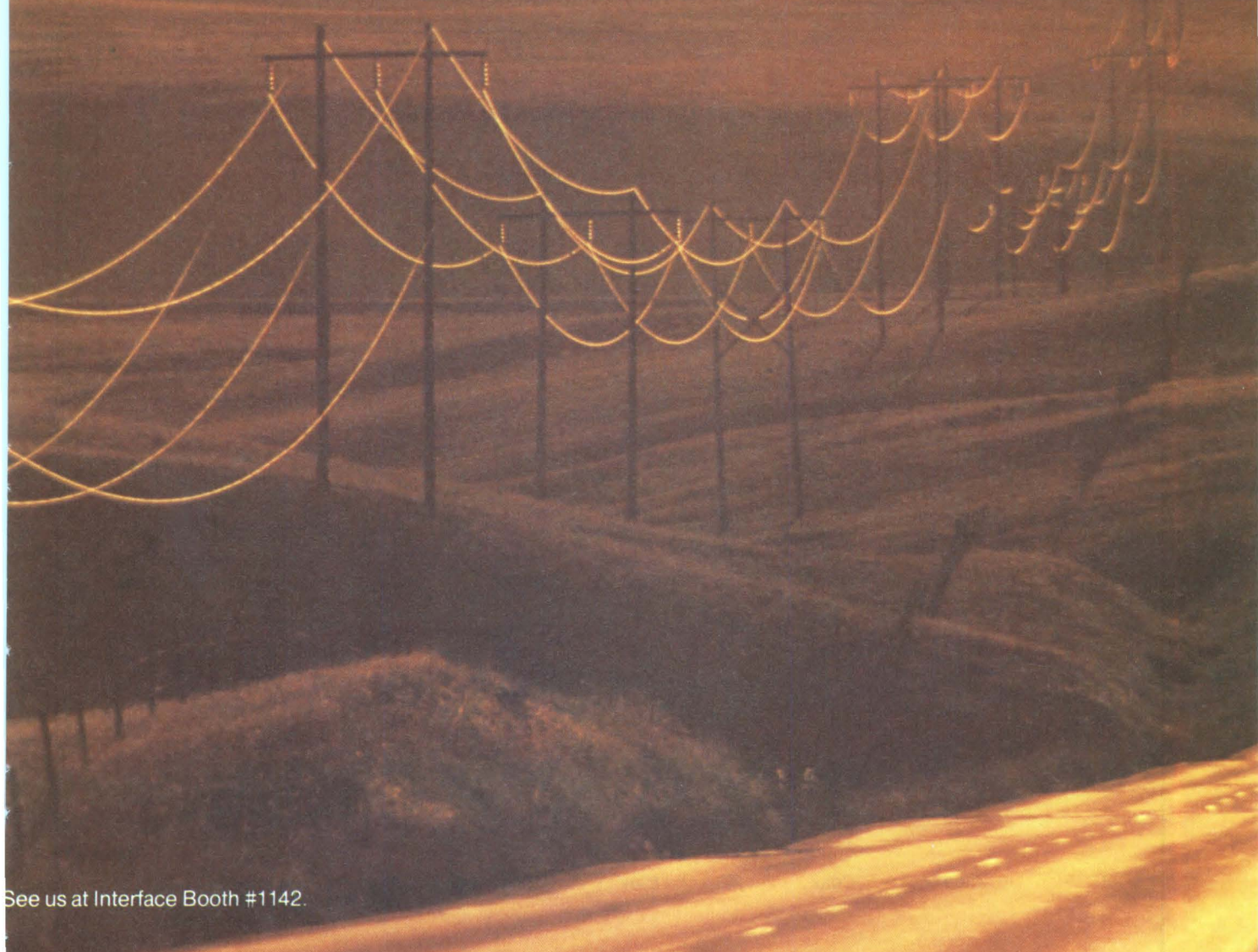
network processor with features such as unlimited port capacity, host selection and port contention. All by adding—instead of replacing—DCA components. So your investment is protected all the way down the line.

For more information about our newest statistical multiplexors, call toll-free: 1-800-241-5793. Or write: Digital Communications Associates, Inc., 303 Research Drive, Norcross, Georgia 30092. Somewhere down the line, you'll be glad you did.

dca

Digital Communications Associates, Inc.
DCA products are available worldwide.

SOMEWHERE DOWN THE LINE, YOU'LL BE GLAD YOU CHOSE A SERIES 100 STATISTICAL MULTIPLEXOR.



See us at Interface Booth #1142.

CIRCLE 100

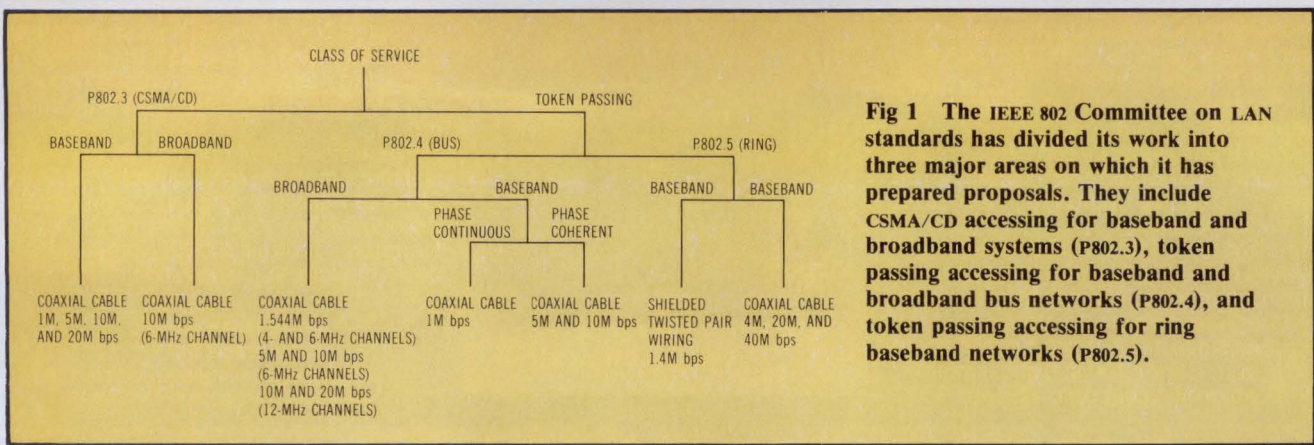


Fig 1 The IEEE 802 Committee on LAN standards has divided its work into three major areas on which it has prepared proposals. They include CSMA/CD accessing for baseband and broadband systems (P802.3), token passing accessing for baseband and broadband bus networks (P802.4), and token passing accessing for ring baseband networks (P802.5).

Under the P802.5 proposals for token passing ring networks, only baseband operation is considered for both shielded twisted pair wiring (at 1.4M bps) and baseband coaxial cable (at 4M, 20M, and 40M bps). (See Fig 1 for an outline of the IEEE 802 Committee's standards proposals.)

Toward an open systems architecture

Though the IEEE 802 proposed standard is compatible with only the first two layers (physical and data link) of the 7-layer International Standards Organization (ISO)

Open System Interconnection (OSI) reference model (Fig 2), work is proceeding to eventually have LANs compatible with all seven layers. Remember that the ISO OSI reference model represents an ideal case, something few computer and peripheral equipment manufacturers can be expected to support completely. The first two layers, adopted by all LAN equipment suppliers and international standards organizations, are generally implemented in hardware. Layers 3 through 7 are software intensive, thus more difficult to implement readily at low cost.

**TABLE 1
Representative CSMA/CD and CSMA/CA Baseband LANs**

Network	Company	Media	Max nodes	Max rate (bps)	Max distance (no repeaters) (m)	Topology	Comments
Cluster/One Model A	Nestar Systems	Ribbon, Twisted pair	65	250k	305	Varied	Office automation Personal, engineering, small business computers
Ethernet	Xerox	Coax	1024	10M	500	Bus	<i>De facto</i> industry standard Office automation Personal, small business computers
1553 Net	VLSI Systems	Coax	256	3M	305	Bus	Personal computer Two independent channels for command and data signals
HYPERbus	Network Systems	Coax	128	10M	732	Bus	Laboratory, factory, office automation Satellite compatible
HYPERchannel		Coax	16	50M	1524	Bus	Large mainframe and scientific computers Satellite compatible
Net/One	Ungermann-Bass	Coax	100	10M	500	Bus	Laboratory, office, factory automation Ethernet compatible
Omninet	Corvus Systems	Twisted pair	64	1M	1219	Bus	Personal, small business computers
PACXNET	Gandalf Data	Twisted pair Coax Fiber optic	8	5.3M	—	Varied	Office automation Word processing Resource sharing
Z-net	Zilog	Coax	255	800k	2000	Bus	Office automation Small business computer

Last year, nearly two dozen major manufacturers of computer systems, information retrieval systems, and network equipment from Japan, Europe, and the United States agreed to back layer 4—the transport layer—of the ISO OSI reference model. Standards for both layers 3 and 4 have been developed by the Defense Applied Research Projects Agency and adopted by the U.S. Department of Defense. Furthermore, Xerox has publicly defined layers 3 and 4 for its Ethernet LAN protocol.

Software compatibility for the ISO OSI reference model layers 3 through 5 is now available for up to 32 RS-232 compatible non-Ethernet devices, thanks to the CS/1 communications processor that Bridge Communications Inc made available last year. The CS/1 employs the higher level protocols of the Xerox Network Systems (XNS). XNS provides internetworking commands for dissimilar Ethernet devices.

Standardization of the first two layers of the ISO OSI reference model has also meant X.25 protocol compatibility, assuring network to network transfers of data packets over the switched public network. Several products are available on the market that allow X.25 LAN interfacing. One such product, the GS/1 XNS gateway from Bridge Communications, allows host to host, host to terminal, and terminal to terminal connectivity.

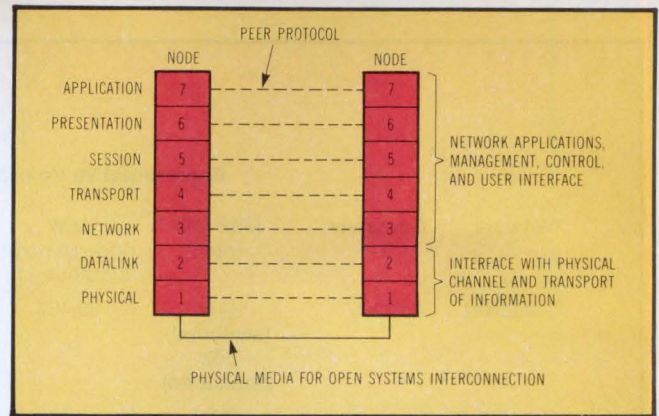


Fig 2 An ideal case for communications between computers and peripherals is governed by a 7-layer architecture protocol formulated by the ISO. Known as the OSI reference model, it represents a set of rules by which effective communications can be achieved.

In the meantime, LAN manufacturers have been busy cranking out record numbers of baseband and broadband LANs, spanning a range of topologies, access schemes and transmission media (see Tables 1, 2, and 3 for a representative sampling).

Although there are accessing schemes besides CSMA/CD and token passing—schemes such as time

TABLE 2
Representative Token Passing Baseband LANs

Network	Company	Media	Max nodes	Max rate (bps)	Max distance (no repeaters) (m)	Topology	Comments
Attached Resource Computer	Datapoint	Coax	255	2.5M	610	Bus	Office automation, data processing Each processor node can participate in up to 6 ARCs
		Infrared optical links			1609		
DOMAIN	Apollo Computer	Coax	—	12M	914	Ring	Engineering, CAD/CAM, factory automation
LINC	Vector Graphic	Twisted pair	16	750k	3218	Ring	Interconnects Vector 4 microcomputer family into a multi-user environment
Modway	Gould Modicon	Coax	250	1.544M	4572	Bus	Process control, data processing, office automation Satellite compatible
Omnalink	Northern Telecom	Coax	20	40k	1524	Ring	Office automation, data processing
PLAN 4000	Nestar Systems	Coax	255	2.5M	6437	Varied	Personal computer ARC and Ethernet compatible
PLANET	Racal-Milgo	Coax	250	19.2k	198	Ring	Protocol, application transparent
Primenet	Prime Computer	Coax	247	10M	3048	Ring	CAD/CAM, office automation, data processing
proNET	Proteon Associates	Coax Twisted pair Fiber optics	255	10M	2414	Ring	Process control Relays bypass faulty nodes
Xodiac	Data General	Coax	32	2M	1609	Bus	Office automation, word processing, electronic mail, data processing

TABLE 3
Representative Coaxial Cable Broadband LANs

Network	Company	Max rate (bps)	Max node to node distance (m)	Accessing scheme	Topology	Comments
CableNet	Amdax	14M (switched) 56k (dedicated)	80,467	TDMA (switched) FDM (dedicated)	Bus	Office and factory automation, data processing, security
ContelNet	Control Information Systems	10M/channel	305	CSMA/CD	Bus tree	Office automation, data processing
GEnet	General Electric	1M or 5M	4828	CSMA/CD	Bus	Factory and office automation
Local/net 20	Sytek	128k	50,000	CSMA/CD	Bus	Distributed processing Design, factory, office automation
Local/net 40		1.7M	4000	CSMA/CD	Bus	
Net/One	Ungermann-Bass	5M	16,093	CSMA	Bus	Office automation, small business, data processing Functionally similar to baseband version
Token/Net	Concord Data	5M	16,093	Token passing	Bus	Large data communications systems, factory automation, realtime applications
Video-data	Interactive Systems/3M	5M	32,186	FDM/TDM	Tree	Data processing, office automation, small business computers, security
Wangnet	Wang Labs	64k	Several kilometers	CSMA/CD	Tree	Office automation, image and data processing, security

division, frequency division, and space division multiple accessing—these two are the most common in commercially available LANs.

The CSMA/CD baseband approach is a random one conceived by Xerox Corp in 1973 for its Ethernet LAN. It is now used by Zilog Corp (Cupertino, Calif) for its Z-net network, and Ungermann-Bass Inc for its Net/One network. Many others offering baseband LANs do not use collision detection. Instead, carrier sense multiple access/collision avoidance (CSMA/CA) is employed. Token passing, which unlike CSMA/CD is a deterministic accessing method, can be found in applications for real-time process control applications. Proponents of this approach, led by IBM, include Datapoint Corp (San Antonio, Tex) for its ARC network, Gould's Modicon Div (Andover, Mass) for its Modway LAN, and a host of others. Table 4 compares three major criteria of LANs: transmission medium, accessing method, and network topology.

As can be seen from Table 4, a wide choice of network tradeoffs is possible. For example, although CSMA/CD accessing is nondeterministic, it makes economic sense (since it is less expensive than a broadband network when all other factors including maintenance are considered) to use it for an office automation application. In such an application, whether a message gets

from one office location to another in a fraction of a second or a few seconds is of little significance. On the other hand, a token passing accessing scheme must be used to ensure that a valve in a process control loop is turned off at the critical moment, lest the entire process be ruined.

For many office automation applications in which video teleconferencing plays a large role, a broadband network, with its many more channels and wider bandwidth than a baseband one, can be the proper choice. Even here, there is room for disagreement, since some baseband systems, as well as PABXs, can transmit video information, though not simultaneously with data. For many applications in which some data but mostly voice information is transmitted, PABXs can prove to be useful choices, particularly when they are already installed in a building to service telephone communications, and only a minor addition is required to handle data.

Comparing CSMA/CD and token passing

CSMA/CD is a random accessing scheme in which a network node transmits a message after listening to the network to make sure it is not busy. Should the network be busy, the node must wait until it is clear, before it can begin transmitting. Once it transmits a message, the

node continues to listen to the network to detect any collision with message packets being sent simultaneously by one or more other nodes on the network. In the event of a detected collision, all transmitting nodes abort their operations and back off a random amount of time before attempting to retransmit their packets. The waiting time is a random one and is influenced by such factors as network traffic volume, message length, and network physical length.

Besides being nondeterministic, a CSMA/CD message packet must be twice as long as the message's propa-

gation time to the most distant network station. This guarantees collision detection before transmission is completed.

A variation of CSMA/CD is CSMA/CA in which no collision detection is used. In fact, many experts contend that most of the cost of CSMA/CD interface hardware is in the collision detection circuitry, and that eliminating it would reduce that cost substantially. One example of this approach is the Omninet from Corvus Systems Inc (San Jose, Calif). Employing RS-232 twisted pair wiring, the baseband system can transmit messages on a

TABLE 4
Relative Comparisons of LANs
By transmission medium

Media	Bandwidth	Ability to handle many nodes	Distance	Topological versatility	Installation ease	Noise immunity	Cost*
Twisted pair	Low	Low	Low	High	Moderate	Low to moderate**	Low
Baseband coax	Low to moderate	Moderate	Moderate	High	High	Moderate to high	Moderate
Broadband coax	High	High	High	High	High	High	Moderate to high
Fiber optic	Very high	Low	Very high	Moderate to low	Moderate	Very high	Very high

By accessing scheme

Accessing method	Control	Bandwidth	Ability to handle many nodes	Transmission distances	Contention degree	Deterministic?	Flexibility	End to end message delay
Random (CSMA/CD)	Distributed	High	Moderate	Moderate to high	High	No	High	Unknown
Polling (token passing)	Distributed	Moderate to high	High	Low	Low	Yes	Moderate	Low to moderate
Dedicated (TDMA, FDMA, SDMA)	Central	Low	High	Moderate	Low	Yes	Low	Low

By network topology

Topology	Interface complexity	Flexibility	Expandability	Reliability	Cost
Bus	Low to moderate	High	High	High	Low
Ring	Low	Moderate	Moderate	High	Moderate
Star	Low	Low	Low	Moderate to high	High
Tree	Moderate	High	High	High	Low
Varied	High	Very high	Very high	Moderate	High

*Excluding installation cost

**Higher for shielded versions

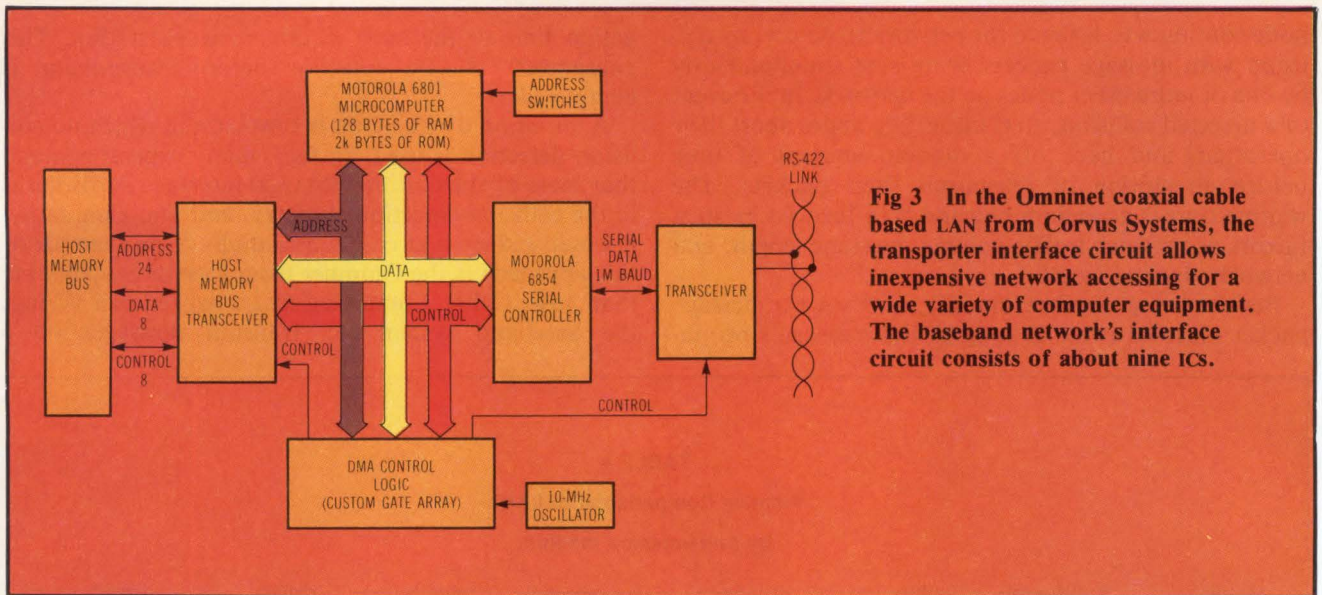


Fig 3 In the Omninet coaxial cable based LAN from Corvus Systems, the transporter interface circuit allows inexpensive network accessing for a wide variety of computer equipment. The baseband network's interface circuit consists of about nine ICs.

network up to 4 km long. Omninet allows interfacing through a proprietary transporter circuit that conforms to the first four layers of the ISO OSI reference model (Fig 3). The transporter is based on a 6801 microcomputer and consists of just nine integrated circuits (ICs), only two of which perform the transceiver function. Its direct memory access hardware adapts to nearly any processor with a minimum number of extra parts. For example, interfacing the Apple II personal computer to Omninet through the transporter requires just five ICs plus the basic transporter.

A disadvantage of the CSMA/CA approach is that, should one or more packets on the network collide, the transmitting nodes will continue to send their messages, unaware of any collisions, and thus waste valuable data and time.

Token passing solves the CSMA/CD and CSMA/CA non-deterministic and message length problems. In token passing, a message in the form of a token is sent from one network node to another, in one direction, where each node examines it. Each node has a specific time during which it can remove the token and strip or add a message to it. At this time, all other network nodes can only listen to the network. This process continues until the original sending node receives the token from the last network node and acknowledges that the intended recipient node got the message.

Token passing thus guarantees access to each network node within a prescribed period of time, hence its highly deterministic nature, a critical quality for certain applications such as process control and other realtime tasks.

Some experts contend that token passing is more complex to implement in hardware and is thus potentially more costly, a point on which the jury is still out. Certainly Western Digital Corp (Newport Beach, Calif) has shown that building interface chips with token passing in mind is no more expensive to do than making CSMA/CD interface devices.

Furthermore, in a ring topology network, the token is passed along from one node to another, in one direction, and any break in the ring causes the node to lose accessing privileges. Being a synchronous scheme (CSMA/CD is an asynchronous scheme since it is a random one) makes token passing more vulnerable to

errors. For example, an access control message could be destroyed or even mistaken, requiring a node to make up another message or delete the wrong one, a difficult task to accomplish in a decentralized environment.

IBM (Research Triangle Park, NC) has developed a token passing ring network (Fig 4) in which the token may be recovered in the event of a node or ring failure. In IBM's design, the ring network includes two or more concentrators from which lobes of one or more stations radiate. The concentrators contain active subsystems that can locate a failure in a node by trial and error. Once a failure is located, the subsystems set up a bypass around the failed node or use a reverse channel parallel to the network's main ring to bypass the failed node. Proteon Associates (Waltham, Mass) uses relays to

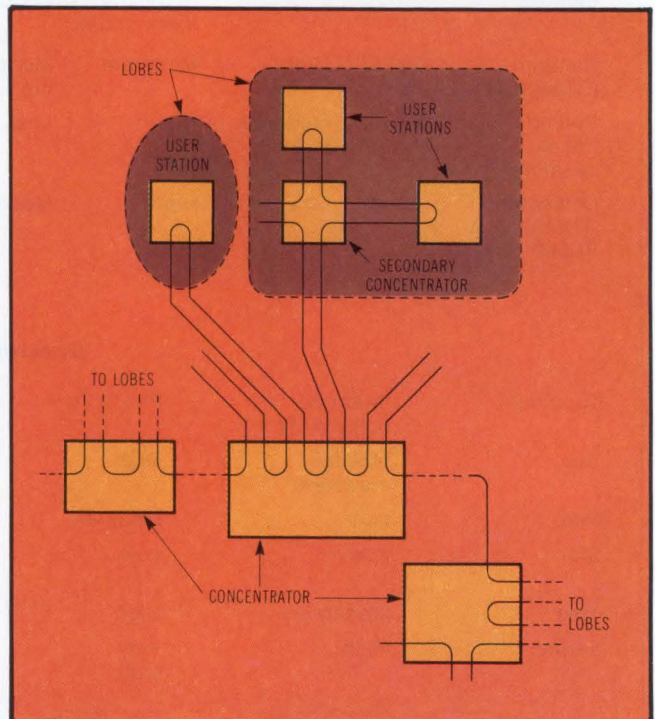
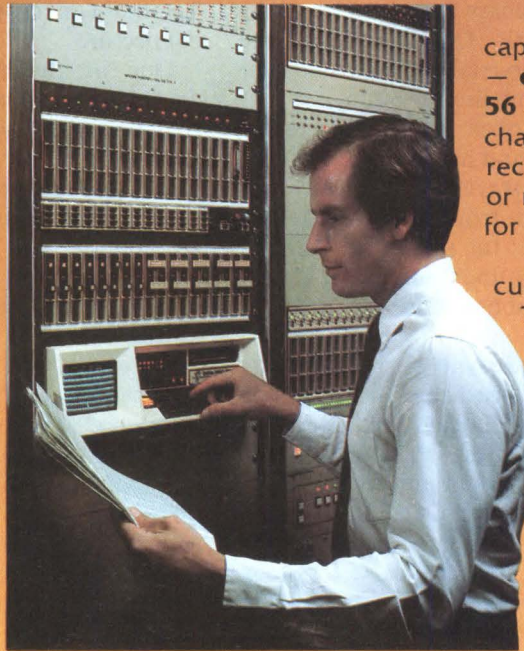


Fig 4 This ring topology implementation from IBM for a token passing LAN uses concentrators to simplify node interfacing. It is particularly effective for networks in which groups of nodes are geographically close to one another.

Dyna-Test[®] Protocol Analyzers: The Friendly Family That Pinpoints Datacomm Problems — Fast.

The Dyna-Test Family of Protocol Monitor/Simulators includes four closely related but distinct models. Dyna-Tests are all easy to operate and engineered to get you back on line — fast. Whether you're locating a defective communication link . . . chasing a timing glitch . . . or isolating software faults — Dyna-Test will quickly solve your network problems.

That's because Dynatech Designs Each Protocol Analyzer To Get the Job Done Right. Our unique combination of versatility, operating ease and high performance enables you to isolate faults quickly. Just a glance at the interface display panel may identify the problem. If not, run standard tests by simply depressing a few select buttons — our protocol key stores all operating parameters for seven different communication lines. Or, write your own test program with our simplified menu/macro format. All programs are entered in a non-volatile memory and can be transferred to tape for use with other units.



Dyna-Test Easily Handles the Most Complex Network Problems. Our split-screen display format decodes frame and packet headers and simultaneously displays both on the screen: **All on a real time basis!** — you can actually see the link initialization occur.

The Dyna-Test integral tape captures data and control signals — even at data rates as high as **56 kbps**. Specific events or character sequences can be recorded and either played back or routed to an external printer for off-line analysis.

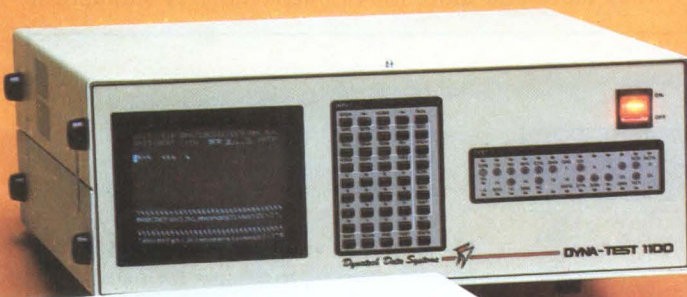
Dyna-Test protocol analyzers currently enjoy world-wide use. They support most standard interfaces, protocols (SDLC, HDLC, X.25, 3600) and data codes. Most models are available from stock; special orders for unique interfaces take 30 days.

Let us introduce you to Dyna-Test, our friendly family. Dynatech Network Specialists are eager to demonstrate — on site — the Dyna-Test protocol analyzer best suited to your needs. For an appointment call or write:

Dynatech
Data Systems

7644 Dynatech Court
Springfield, Virginia 22153
800-368-2210
In Virginia, (703) 569-9000

CIRCLE 101



Although CSMA/CD and token passing are similar, each is more suitable for certain applications.

sense loss of signal and to bypass failed nodes in its PRONET token passing network. One feature of the PRONET system is that it uses coaxial cable twisted pair and optical fibers as the transmission medium.

Both the CSMA/CD and token passing accessing schemes can be used on baseband as well as on broadband LANs. For example, CSMA/CD is used on such broadband networks as GENet from General Electric Co's subsidiary Intersil Systems Inc (Sunnyvale, Calif), Local/nets 20 and 40 from Sytek Inc (Sunnyvale, Calif), and Wangnet from Wang Laboratories Inc (Lowell, Mass).

A host of baseband local area networks are using token passing accessing as well (see Table 2). Two of the most recent are the Personal Local Area Network (PLAN) 4000 from Nestar Systems Inc (Palo Alto, Calif) and Local Interactive Network Communications (LINC) from Vector Graphic Inc (Thousand Oaks, Calif).

The PLAN 4000 system from Nestar is an interesting one. Employing a freeform and arbitrary topology (such as a bus, tree, star), PLAN integrates elements of three different LAN technologies: the ARC from Data-point Corp, the Ethernet from Xerox Corp (Dallas, Tex), and Nestar's own Cluster/One Model A. The first provides the PLAN 4000's token passing network, the second adds the internetworking software, and the last one supplies software for the PLAN 4000's design for personal computer interfacing. The PLAN 4000 has plug-in interface cards that allow the networking of IBM's personal computers, as well as Apple III personal computers, into a multi-user environment. The PLAN 4000 network is designed to support about 10 times as much data traffic as most low cost personal computer networks.

Twisted pair wiring is all that is needed for the LINC network from Vector Graphic. The low cost network connects up to 16 Vector 4 single-user microcomputers

into a flexible and expandable multi-user system. A LAN makes use of the integrated disk drives in each of the Vector 4 microcomputers to eliminate the need for expensive file servers and multiplexers. Interfacing any of the Vector 4 microcomputers is accomplished by inserting a SABER-Net controller board into the microcomputer's modified S-100 slots, and then attaching the Vector 4 microcomputer to LINC via a modular connector.

One of the first (the first deliverable network, according to its manufacturer) broadband LANs using token passing accessing is Token/Net from Concord Data Systems (Waltham, Mass). The bus topology system is said to be totally compatible with upcoming IEEE 802 LAN standards and is designed for realtime factory automation and similar applications. The network transmits data at 5M bps and can interconnect 2 more nodes up to a maximum distance of approximately 10 miles.

A closer look

Though CSMA/CD and token passing accessing are similar in that they both are distributed control techniques, there are some important differences between the two, differences that render one or the other less suitable for certain applications. For example, to ensure that every CSMA/CD packet is detected when it collides with another, the packet is restricted to some minimum size, increasing its propagation time through the network and causing some delays. These delays become more noticeable in very lengthy LANs. Token passing, on the other hand, is insensitive to network medium length and data transmission rate.

The two packets for CSMA/CD and token passing are similar at the physical and data link layers (the first two layers of the 7-layer ISO OSI reference model). However, an access control field in the token passing packet is matched by a filler field in the CSMA/CD packet (Fig 5). The filler field is needed to ensure a CSMA/CD packet long enough to cause collision detection.

Low cost interface hardware and software products for tapping onto the Ethernet LAN are making the network more and more the *de facto* industry standard it

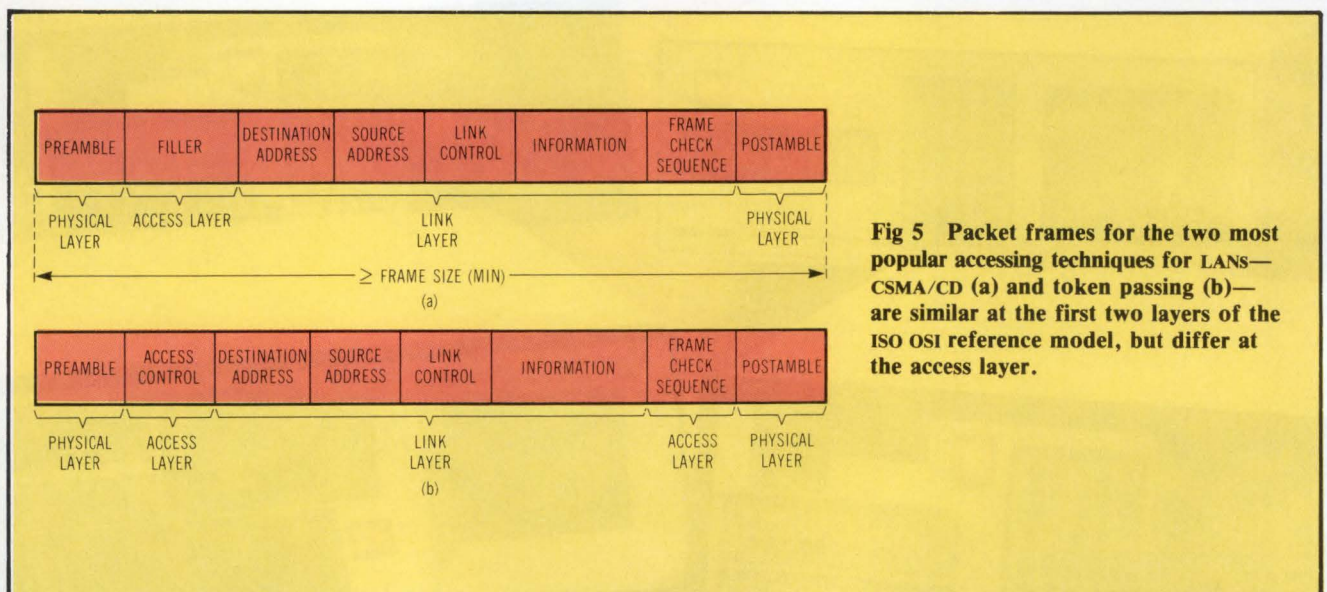
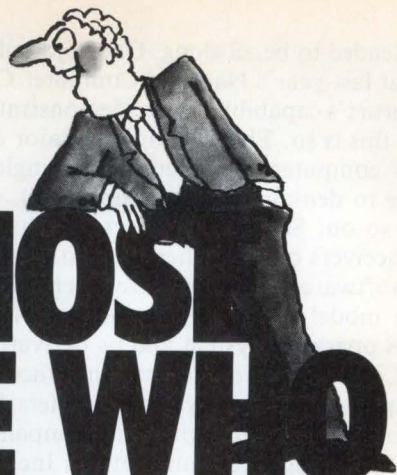


Fig 5 Packet frames for the two most popular accessing techniques for LANs—CSMA/CD (a) and token passing (b)—are similar at the first two layers of the ISO OSI reference model, but differ at the access layer.

"I JUST LOVE
EMULEX FEATURES
AND QUALITY..."



"BUT CAN YOU
BELIEVE THEIR
NEW LOW PRICES?"



FOR ALL THOSE LSI-11 PEOPLE WHO NEVER CONSIDERED EMULEX ON PRICE.

Consider the products and prices below:

You'll soon see that Emulex is as unbeatable on price as we are in quality and performance. Included are two new Winchester disk controllers with remarkably high performance and reliability (MTBF over 70,000 hours).

All Emulex Q-bus tape and disk controllers have the same microprocessor architecture and all the key features of our PDP-11 and VAX-11 products, including error correction, micro-diagnostics, and software transparency. Price our performance. Write or call: Emulex Corporation, 3545 Harbor Blvd., P.O. Box 6725, Costa Mesa, CA 92626; (714) 662-5600; Outside Calif.: (800) 854-7112.

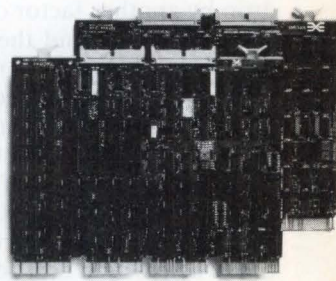
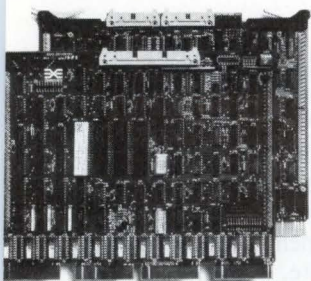
In Europe: Emulex Corp., 10th floor, Cory House, The Ring, Bracknell, Berkshire, England. Telephone: 0344-84234; Telex 851-849781.

SC01 (RM02/05, RP06) \$2530*

SC02 (RL01/02, RP02/03, RK06/07)
Now \$1410*

SC04 (RL01/02, RP01/02, RK06/07)
Now \$1410*

TC01 (NRZ) Now \$1150*
TC01 (PE) Now \$1470*



**NEW
REDUCED
PRICES!**

Put big SMD drives on your SI-11.

Links Q-bus with 1-2 SMD-type drives. Software transparent; media compatible with DEC RM02, RM05, RP06. Features 3-sector data buffer, 32-bit ECC, up to half a billion bytes capacity. Over 1500 units in service!

Low cost for smaller-sized disks.

Single quad-board interfaces LSI-11s to 8" & 14" SMD hard disk drives. Same great SC01-level performance in most applications. Software transparent. Full 32-bit ECC, self-test, 512-word bootstrap, real-time clock control, and bus terminators. Mix and match drives on one controller. 72,000 hours MTBF!

New! ANSI interfacing for 8" Winchesters.

Supports up to 8 drives per single quad-board controller. Fits into any single LSI-11 back plane quad slot. Same design, performance, and high reliability as the SC02.

Q-bus embedded dual-density tape controller.

Handles all open-reel half-inch tapes — 800/1600 bpi, operating at 12.5-75 ips. Compatible with DEC's TU10/TM11. Daisy-chain up to 4 drives. Firmware includes a self-test and extended diagnostics. Fully embedded.

*Price each in 100 quantities. All Emulex disk, tape, and communications products can be combined to reach quantity price breaks.

Coming soon: Emulex's SC03, 11-performance /23 disk controller. \$1790



The genuine alternative

has tended to be all along. One need only have been present at last year's National Computer Conference where Ethernet's capabilities were demonstrated to understand why this is so. There, about 10 major companies linked their computers together over a single 1500' Ethernet cable to demonstrate electronic mail, word processing, and so on. Several manufacturers had controllers and transceivers on the Ethernet, and 3Com Corp provided the software for the top five layers of the ISO OSI reference model. The Unet network software runs on the UNIX operating system and its derivatives.

3Com is one of several interface communications component and subsystem suppliers for Ethernet and other LANs. Other prominent companies include Interlan Inc, Bridge Communications Inc, Associated Computer Consultants (Soquel, Calif), and Perex Inc (San Jose, Calif).

Interlan recently introduced the NT10 transceiver, a \$290 product that allows immediate tapping onto Ethernet without interrupting the network's operations. The product is physically attached to the Ethernet cable by a tap mechanism that allows nonintrusive connections. The mechanism has two sets of probes that extend through the coaxial cable's insulation. One probe makes contact with the cable's center conductor and the other with its shield. A drill fixture and bit, provided by Interlan, allow two precisely located holes to be made into the cable. Triple protection watchdog circuitry in the NT10 isolates the product from Ethernet in the event of an NT10 malfunction.

The chips are coming

One of the most important trends in LANs is the integration of interface functions into silicon, allowing truly low cost networking. Ethernet's connection cost, for example, has dropped from about \$5000 per connection to about \$2000 for small-quantity orders, and under \$1000 for larger orders. And that is not the end of it. Experts claim that the price per Ethernet connection will drop by another factor of 2 this year, dropping down to about \$500, a trend they expect to continue as greater VLSI implementations are achieved.

This dropping connection cost trend is important in view of the fact that many LANs, including Ethernet, are designed to interconnect personal computers. In an era when the average price for desktop 16-bit personal computers ranges from \$3000 to \$6000 (for useful configurations), it would be prohibitively costly if the average direct connection cost for networking were to constitute a third or more of the price of the personal computer it is to serve.

Over one-half dozen semiconductor IC manufacturers have either already delivered or are readying samples of large scale integration chips that will reduce interconnection costs for all types of LANs. The basic system chip that makers are trying to integrate into silicon includes the medium tap (also referred to as the transceiver), the interface between the tap and computer or peripheral (driver), and the computer's controller—a task that is complex enough to warrant the use of two or more silicon chips. In the meantime, some companies are pursuing board level solutions as an interim measure.

Seeq Technology Inc (Milpitas, Calif) is delivering samples of a single-chip interface device for Ethernet in its model 8001. Seeq and 3Com Corp codeveloped the 8001 with help from Silicon Compilers Inc (San Francisco, Calif). The N-channel metal oxide semiconductor (NMOS) IC is totally compatible with the second layer of the 7-layer ISO OSI reference model. It contains the basic Ethernet interface control functions, including collision handling (retransmission), address generation, cyclic redundancy code generation and checking, and data serialization and deserialization. This is supplied on a chip 225 x 225 mils, through the use of 3-micron design rules. The 40-pin plastic dual inline package operates from a single 5-V supply and dissipates 1 W. It is being priced at \$135 in 100-unit quantities.

This year, designers at Seeq Technology are readying an even smaller chip at 160 x 160 mils using 2-micron design rules. Incidentally, the Seeq 8001 chip differs from other interface IC designs in that it will totally interface to anyone's microprocessor (other designs are dedicated to specific microprocessors).

An important influence on LANs is the integration of interface functions into silicon.

Yet another joint Ethernet interface development is the teaming up of Ungermann-Bass Inc and Fujitsu's U.S. subsidiary to develop a 2-chip set from gate arrays, to be made available early 1983. One is the bipolar LAN-1 and the other complementary MOS LAN-2. The LAN-1 meets all specifications for layer 1, and the LAN-2 all specifications for layer 2, of the 7-layer ISO OSI reference model. The LAN-1 is designed to operate from 5 V and dissipate 750 mW, while the LAN-2 will operate from 5 V and dissipate 100 mW. The latter version will be placed in a 64-pin grid array package. The LAN-2 is intended to mate with nearly any microprocessor bus structure.

Intel Corp, a member of the Ethernet triumvirate that also includes Xerox and Digital Equipment Corp, has been busy developing a 2-chip Ethernet interface set that it will also prepare for early 1983 sampling. The 2-chip set will offer all the basic Ethernet interface functions, including data encoding/decoding, line control, serialization, line driving, as well as system diagnostics.

In the meantime, Digital Equipment Corp, the second member of the Ethernet triumvirate, is also busy with a joint 3-chip set for Ethernet interfacing that Digital Equipment has designed. The firm has teamed up with Advanced Micro Devices Inc (Sunnyvale, Calif) and Mostek Corp (Carrollton, Tex), in an effort that is expected to yield chips by late this year or early next year. Mostek will produce a single-chip NMOS local area network controller for Ethernet (LANCE) device (MK7990) that will act as the Ethernet controller, while AMD will produce two bipolar chips, one (Am87991) a serial interface adapter, and the other (Am7990) the Ethernet transceiver. The LANCE chip set has an onboard direct memory access channel and flexible buffer management.

Xerox itself has in design a single-chip NMOS Ethernet controller that it discussed at this year's International



MODEMS SHOULD BE HEARD

AND NOT SEEN.

As you can't see, the terminal on the left has a low-cost Rockwell R24DC modem built in. It's connected directly to the U.S. dial-up network with nothing more than a standard telephone jack. No acoustic coupler. No phone. No tangled wires.

It's easy to connect the R24DC modem inside your terminal. It's LSI-based, with the entire 2400 bps modem and data access arrangement on a single 5" x 7.85" plug-in card. With power requirements of $\pm 12V$ and $+5V$, it consumes only 3 watts.

Rockwell's R24DC integral modems are FCC-registered and both Bell- and CCITT-compatible. And they're widely used in point-of-sale terminals, and for cleaning up PBXs, data concentrators and data communications devices.

To get the inside story on Rockwell modems, call the Electronic Devices Division, Rockwell International at (800) 854-8099. In California, call (800) 422-4230. Or write us at P.O. Box C, MS 501-300, Newport Beach, California 92660.



Rockwell International

...where science gets down to business

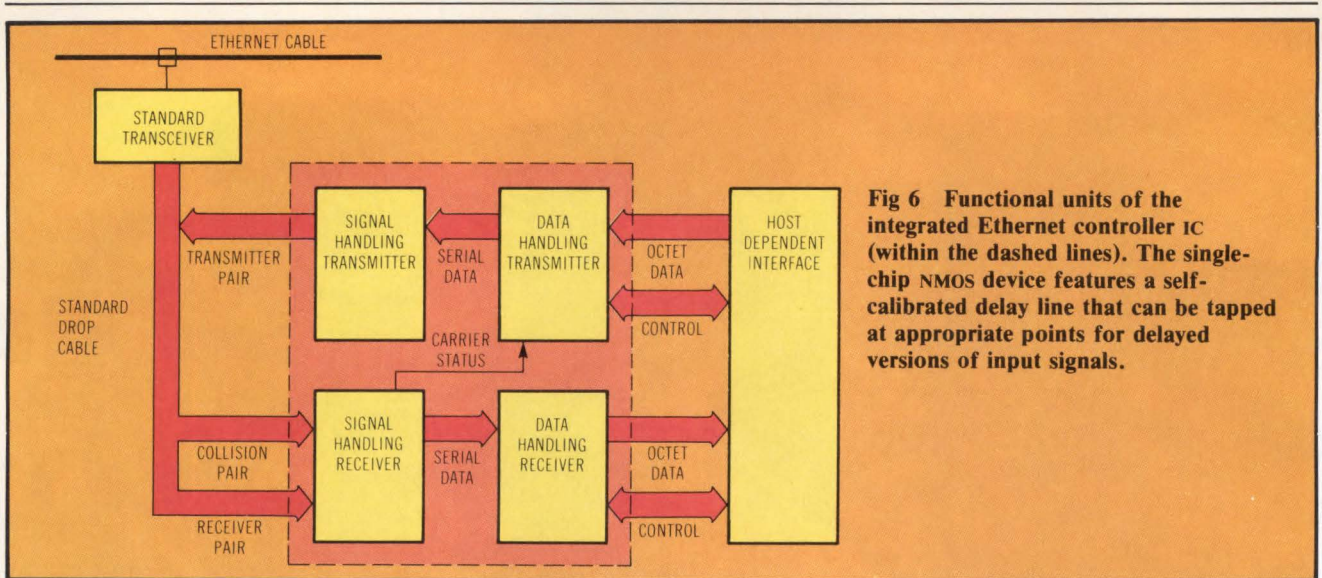


Fig 6 Functional units of the integrated Ethernet controller IC (within the dashed lines). The single-chip NMOS device features a self-calibrated delay line that can be tapped at appropriate points for delayed versions of input signals.

Solid State Circuits Conference (Fig 6). The device implements the first two layers of the 7-layer ISO OSI reference model. A fully functional prototype of this chip has been demonstrated in Xerox's 8010 processor. An important aspect of the 6.6- x 4-mm chip is a self-calibrated delay line that can be tapped at appropriate points to obtain delayed versions of input signals.

Rockwell Corp's Microelectronics Div (Newport Beach, Calif) is also actively developing an Ethernet interface chip. Early this year, the firm will have its R68802 ready. This chip has similar control functions to those used in the LANCE chip set. National Semicon-

ductor Corp also plans to make a single-chip Ethernet device available this year. Furthermore, National is planning to make available a token passing chip set.

Already, IBM's Communication Products Div and Texas Instruments Inc (Dallas, Tex) have announced their joint VLSI chip development for token passing LANs. The effort involves TI designing and building MOS chips on printed circuit cards to IBM's specifications, for the latter's token passing LANs.

Standard Microsystems Corp (Hauppauge, NY) is now making available the COM9026, a single-chip token passing device that the firm built under an agreement with the Datapoint Corp for the latter's ARC LAN. The chip uses ARC's modified token passing protocol and transfers data at 2.5M bps. The IC supports up to 255 nodes per network segment and reconfigures itself as nodes are added or deleted from the network.

Although it is slower—a top speed of 1.1M bps—Western Digital Corp's WD2840 for token passing networks performs a variety of functions. The controller connects 2 to 254 nodes and performs data framing, error checking, destination filtering, fair and adjustable transmission scheduling, network initialization, as well as fault recovery. The chip has two other speeds of 100k bps and 500k bps. Speeds higher than the highest 1.1M-bps speed are also available on special order.

Besides all this activity among semiconductor manufacturers to produce interface CSMA/CD and token passing chips and chip sets, a multitude of other semiconductor manufacturers have already announced that they will produce many of the aforementioned chips as alternate sources. These developments, coupled with the nearly completed IEEE 802 proposed standards (which include CSMA/CD and token passing accessing as the two key accessing schemes), mean that the day when computer and peripheral equipment users can tie into local networks inexpensively is not too far off.

Single Board Computer

6 MHz Z80

DSB-4/6 is Fast, Powerful and Compact

- 4 MHz Z80-A* or 6 MHz Z80-B* Processor and I/O
- Full DMA for Both 5 1/4-inch and 8-inch Disk Drives
- High Speed Bi-directional Parallel Port
- 4 RS-232 Serial Ports (110-38,400 baud)
- Centronics Type Parallel Printer Port
- 64K of RAM and 2K of ROM

Davidge Corporation
 1951 Colony Street, Suite X
 Mountain View, CA 94043
 (415) 964-9497

* Z80 is a registered trademark of Zilog

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 710

Average 711

Low 712

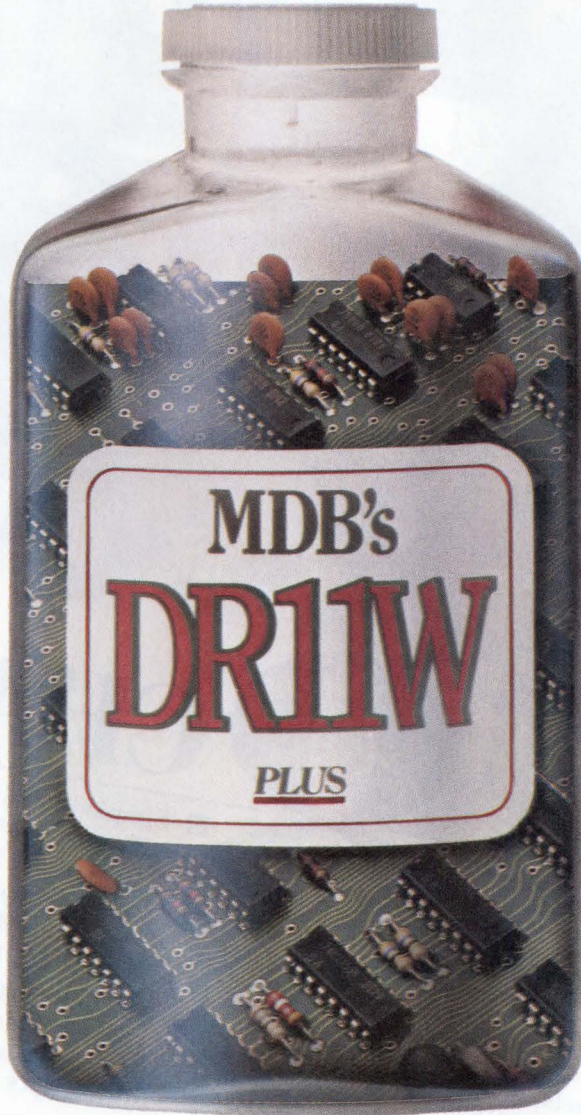
How do Unibus* users spell peak I/O rate relief?

High speed data acquisition can be a real headache. Especially during peak I/O rates when transfer can exceed the CPU's capacity and key bits of information go off in thin air.

So we developed a DR11-W module. First for the Unibus. Now for the Q-Bus. Both feature our exclusive DMA Throttle that efficiently regulates data flow down to average rates to maximize overall CPU performance. But that's not all.

Additional design features make it a cure for many other troublesome Unibus or Q-Bus system ills. For example, it offers:

- Edge mounted LED's to illuminate performance status
- Micro-sequencer driven, self-test diagnostics
- Long lines capability
- Switch selectable 22-bit addressing (Q-Bus)



- Bus Address Extension for memory transfer throughout the 4 megabyte range (Q-Bus)
- Switch selectable, 4-level or single level interrupt arbitration (Q-Bus)
- Compatibility with 16, 18 and 22-bit backplanes (Q-Bus)

This high speed, digital input/output device is prescribed for such typical applications as:

- High speed graphics
- Digital data acquisition
- Parallel information processing
- Interprocessor linking between a Unibus and Q-Bus

There's more. And we're anxious to spell out all that the DR11-W and our complete line of computer interfaces can do for you. Call or write today and ask about full year warranty. Available under GSA contract #GS-00C-03330.

Now for Q-Bus* users too.

*TM Digital Equipment Corp.

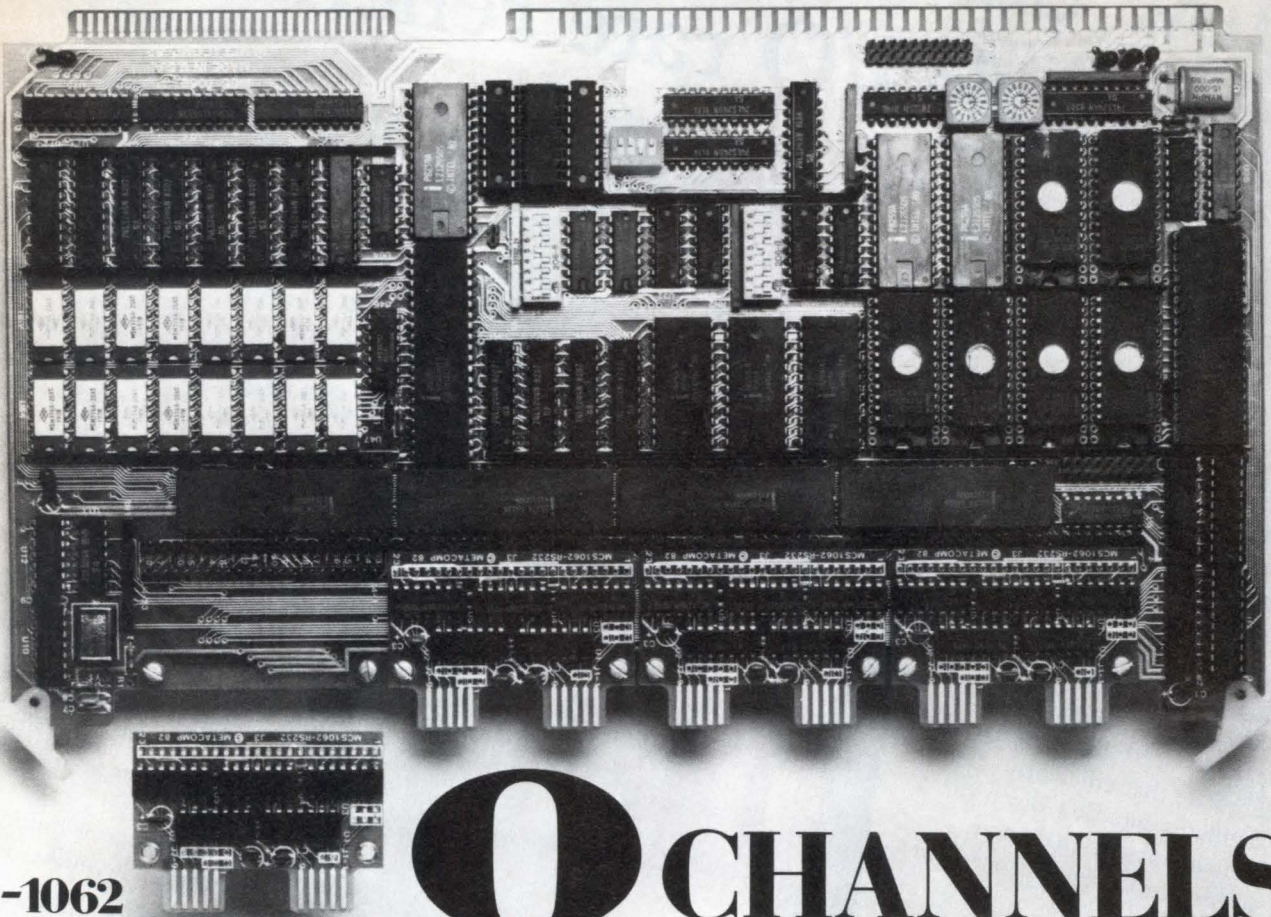
MDB
SYSTEMS INC.

1995 N. Batavia Street, Orange, CA 92665
714-998-6900 TWX: 910-593-1339

Circle 105 For LSI-11 106 for PDP-11

See us at SOUTHEASTCON/ELECTRO '83, COMDEX SPRING and INTERFACE '83

THIS INTELLIGENT MULTIBUS* SERIAL CONTROLLER SUPPORTS



MCS-1062

8 CHANNELS

The next generation in high performance, high capacity, intelligent serial controllers. NOW for the first time, features AND flexibility are available to the MULTIBUS user.

Product Highlights:

- Eight individual channels, programmable for ASYNC, SYNC or BITSYNC.
- Programmable data rates to 38.4K Baud.
- Choose from a wide range of modular interface adapters, each field interchangeable.
 - RS-232
 - RS-422/RS-423
 - Optical Current Loop
 - MIL 188-114
- On-board INTEL 8088 CPU
 - 96K bytes EPROM (using 27128's)
 - 128K bytes RAM

- Simple "handshake" architecture for user software interface
- Dual Port RAM
 - Supports 8 or 16 bit system accesses
 - 24 bit MULTIBUS addressing
- Standard MULTIBUS architecture
 - One unit load
 - One card slot height
 - Vectored or Non-Vectored Bus Interrupts

The MCS-1062. The capacity has doubled, but the price remains the same. \$1,570. ea.**



METACOMP, INC.
7290 Engineer Rd., Suite F
San Diego, CA 92111
619-571-1168
TWX: 910-335-1736 METACOMP SDG

*MULTIBUS is a trademark of INTEL Corporation.
**Quantity 50 price, including RS-232 interface module
Price may vary, depending on interface module optio



SINGLE-CHIP MODEM SLASHES SPACE REQUIREMENTS

Among advancements in LSI modem chips is a single-chip frequency shift keying modem that provides full communication functions at 300 bps.

by Kerry A. Hanson

Data communications via the telephone is becoming more than a convenient option for many small computer users. In this era of distributed computing and processing power, data communications is essential. With the recent availability of large scale integration modems, designers can now incorporate data communications components into the smallest and most inexpensive computer hardware.

Today, incorporating one large scale integration (LSI) chip into a small computer system yields all the necessary modulation, demodulation, and filtering for implementing 0 to 300 bps, full-duplex data communications. Further, by using frequency shift keying (FSK) modulation, compatibility with the Bell 103 series data sets is possible.

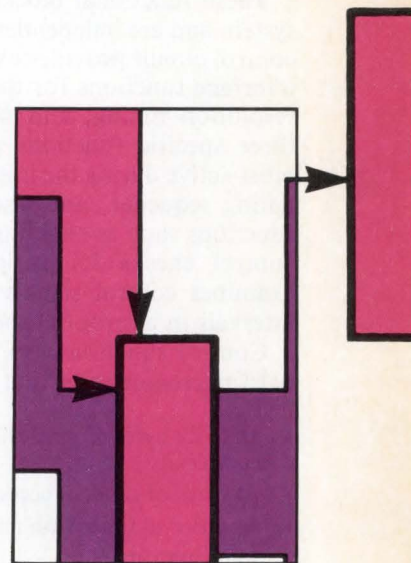
A typical modem chip's functions exemplify the interface requirements between digital computers and analog telephones. For example, the block diagram of Texas Instruments' TMS99532 FSK modem chip (Fig 1) reveals

Kerry A. Hanson is a telecommunications design manager at Texas Instruments, Inc, Data Systems Group, PO Box 1444, Houston, TX 77001, where he is responsible for integrated modem design. Mr Hanson has a BSEE from Montana State University and an MSEE from the University of Minnesota.

clock generation circuits, modulation circuits, demodulation circuits, and filter circuits. The clock generation circuits include a crystal oscillator that runs at 4.032 MHz, a pseudo-random shift register, and frequency dividers that generate the sampling frequencies used by the analog sections of the chip. There are three principal sampling frequencies: the antialias filters use 103 kHz; the rest of the analog circuits use 25.8 kHz; and an 800-Hz clock is used for update in the automatic gain control (AGC) circuit. These frequencies were specifically chosen to minimize the intermodulation products between the FSK signals and the sample clocks. An oscillator output at the master clock frequency is also available, providing a clock for other chips.

Using the modem intelligently

To best understand how a system designer implements an intelligent modem into general purpose data terminal equipment (DTE), one must look at the functional elements of such an integrated, modem based system. Integrated modem functions can be divided into several areas. These encompass digital functions, analog functions, and line interface operations. Digital functions include synchronous/asynchronous conversion, encoding, and overall modem control. Analog functions



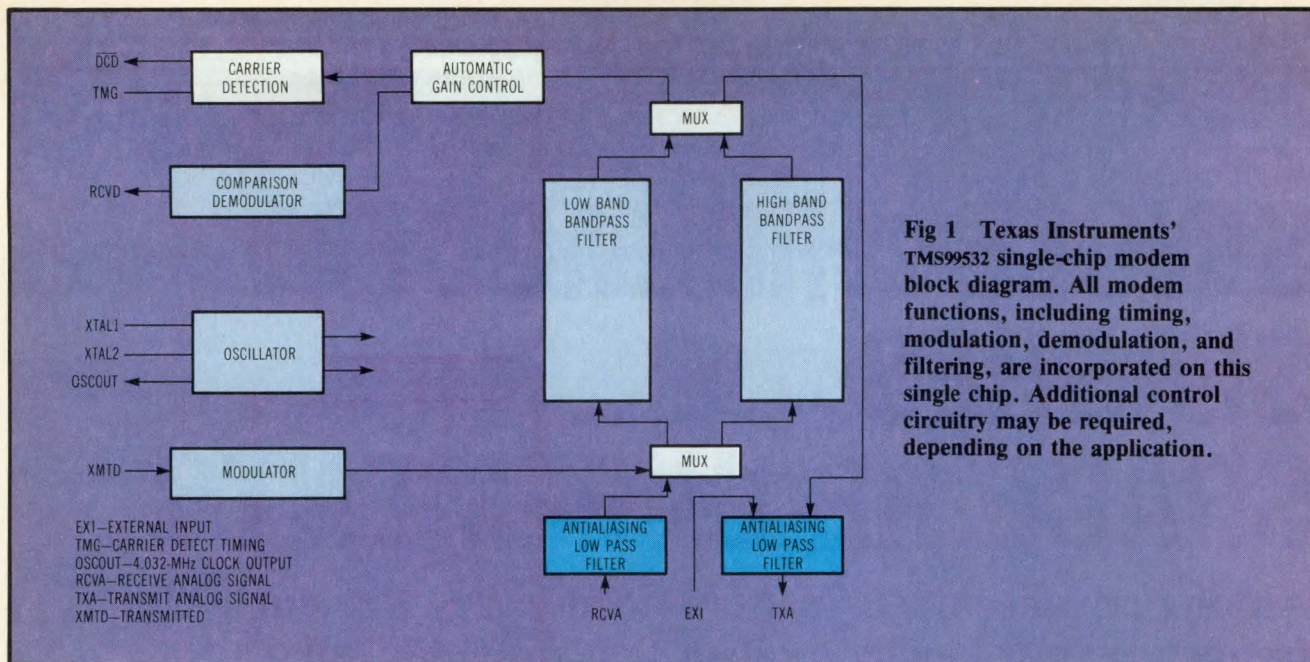


Fig 1 Texas Instruments' TMS99532 single-chip modem block diagram. All modem functions, including timing, modulation, demodulation, and filtering, are incorporated on this single chip. Additional control circuitry may be required, depending on the application.

cover transmit modulation, receive demodulation, filtering, and carrier detection. Line interface circuits include the hybrid transformer, the data access arrangement (DAA), and the acoustic coupler.

These functional blocks represent the entire modem system and are independent of the integration level. The control circuit provides overall modem control and DTE interface functions for the modem. Mode control, low resolution timing, and DTE interface support are the three specific functions performed. The controller is most active during the initiation sequence and the terminating sequence, and also during intermediate special functions such as enabling remote loopback. The mode control checks for various inband carriers, sets or examines control signals to the DTE, and sets proper intervals in appropriate sequence.

Control functions can be implemented with a standard microcomputer that meets the following criteria

- 1k to 2k bytes of read only memory, depending on modem complexity
- 64 bytes of random access memory
- An interval timer with millisecond resolution
- Interrupt capability
- 5 to 15 bit-addressable output lines, depending on modem complexity
- 2 to 5 bit-addressable input lines
- Enough additional interface lines to provide the desired DTE interface

The clock circuits supply the master timing and frequency information for the modem. These circuits include an oscillator, sample clocks, and an FSK carrier clock. In the TMS99532 modem chip, the high frequency sample clocks are signals that drive all sampled data switching elements. Frequencies are dependent upon the operational mode. An FSK carrier frequency clock furnishes the four carrier frequencies needed by a Bell 103J FSK modem. This circuit also provides the answer tone needed for the International Consultative Committee for Telephone and Telegraph (CCITT) V.25 specification.

Texas Instruments' FSK modem chip incorporates a clock oscillator using an external crystal to provide system timing information. This chip can also drive the DAA in all configurations. It has a separate analog signal input, EXI, which is summed with the output of the FSK transmitter. The result is filtered through a voice-band low pass filter before being sent out to the DAA. This allows convenient switching between the external tone mode and the FSK mode and results in simpler mode control.

Designing the chip

For the FSK circuit to transmit Bell 103J compatible FSK data over the phone line, it must perform carrier generation, modulation, and output filtering. Frequency shift keying is a method of modulating a carrier frequency when two states of binary data are assigned to two different frequencies. In the Bell 103J modem, there are two pairs of each assignment. A logic 1 (mark) is assigned 1270 Hz and a logic 0 (space) is assigned 1070 Hz in the originate mode. Frequencies in the answer mode are almost twice these values—a mark is 2225 Hz; a space is 2025 Hz. These frequencies can be used for any data rate from 0 to 300 bps.

To be totally asynchronous, data must be phase and amplitude continuous. In the energy spectrum of the transmitted signal, there must be essentially no energy outside the voice band or in the received data band. This requires band shaping in the modulator as well as a voice-band transmit, low pass filter. The FSK transmitter also generates the answer tone, 2100 Hz, which is required in V.25 applications during the call initiation procedure. In addition, this tone is used to disable the echo suppressors.

On the receiver end, the FSK circuit accepts an FSK modulated carrier from the telephone line, demodulates it, and sends the data to the DTE. The circuit consists of an input filter, a demodulator, and a carrier detect circuit.

A voice-band low pass filter, the input filter acts as an antialiasing filter and prevents high frequency signals

Single-chip modem call establishment sequence

The following steps represent the procedure necessary to initiate communications in the TMS99532 modem:

1. Call is placed to the remote modem
2. Ringing occurs at the answering end
3. Answering modem is enabled to answer the call by asserting DTR
4. Answering modem goes off hook at completion of ringing
5. Answering modem waits 2 s for the billing delay (tBD), specified in part 68 of the FCC's regulations
6. Answering modem turns on transmitter to send an answering mode mark (2225 Hz)
7. Mark (2225 Hz) answer tone is received by the originating modem, and the originating modem is placed in the data mode
8. Originating modem activates its carrier detect (DCD) signal (by a logic 0) after its carrier detect delay (tDCD)
9. Originating modem unquelsches its transmitter, sends an origination mode mark (1270 Hz), and starts a 200- to 350-ms clear to send delay (tCTS)
10. Answering modem receives originate mode mark signal (1270 Hz)
11. Answering modem activates its carrier detect (DCD) signal (by logic 0) after its carrier detect delay (tDCD)
12. Answering modem activates its clear to send signal (by logic 1). Answering modem can now start data communications
13. Clear to send delay of the originating modem expires. Originating modem can now start data communications

from entering the demodulator. The signal is then band-pass filtered. Once the demodulator accepts this frequency, it reduces the signal to the original mark/space data that were transmitted. The carrier detect circuit looks for inband energy. When it finds a valid carrier for a predetermined period of time, it indicates this by setting the digital carrier detect (DCD) signal high. The FSK carrier signal will not turn on unless it receives a mark carrier signal.

A circuit that connects between the data communications equipment (DCE) and the telephone network, the DAA's two principal purposes are network control and electrical isolation. A 600- Ω transformer is normally used for this function. This DAA must be approved under part 68 of the FCC regulations. Part of the approval requirement is to limit the modem's transmitted signal power. If the DAA is FCC approved apart from the modem, it must have either a transmit clamp to shut off the transmitted signal in the event it becomes too strong, or an AGC function in the transmit signal path. DAA signaling functions include indicating an off-hook condition, providing pulse dialing, and showing the presence of a ring signal.

An extra function that must be provided by the DAA circuit is a 2-W/4-W hybrid transformer. This transformer separates the transmitted and received signals on

tip and ring lines and provides a return path for each of them. The hybrid allows the modem full-duplex capability in a 2-wire configuration.

Electrically, the simplest way to connect to the communications network is with an acoustic coupler. Since there is no electrical path, signals are transmitted acoustically to a telephone handset. In this situation, the modem provides the transmit and receive signal lines separately—the termination points are a speaker and microphone. The hybrid transformer inside the telephone yields 4-wire to 2-wire conversion.

Getting connected for communication

Before any data can be transmitted or received, a connection between two modems must be established. A call can be originated either manually or automatically (by an automatic calling unit). When the originating modem detects an answer, the modem is placed in the data mode. Similarly, a call can be answered either manually or automatically and the modem placed in the data mode at the appropriate time. The TMS99532 modem's call establishment sequence is described in the Panel, "Single-chip modem call establishment sequence."

During the call establishment sequence, logic must control the TMS99532 modem's squelch transmission (SQT) and the answer/originate (A/O) pins to ensure that the correct mode is selected and the billing delay requirement satisfied. Depending on a particular application's requirements, there are several call termination procedures. Modem manufacturers offer the user these options by means of jumper wires or switch settings.

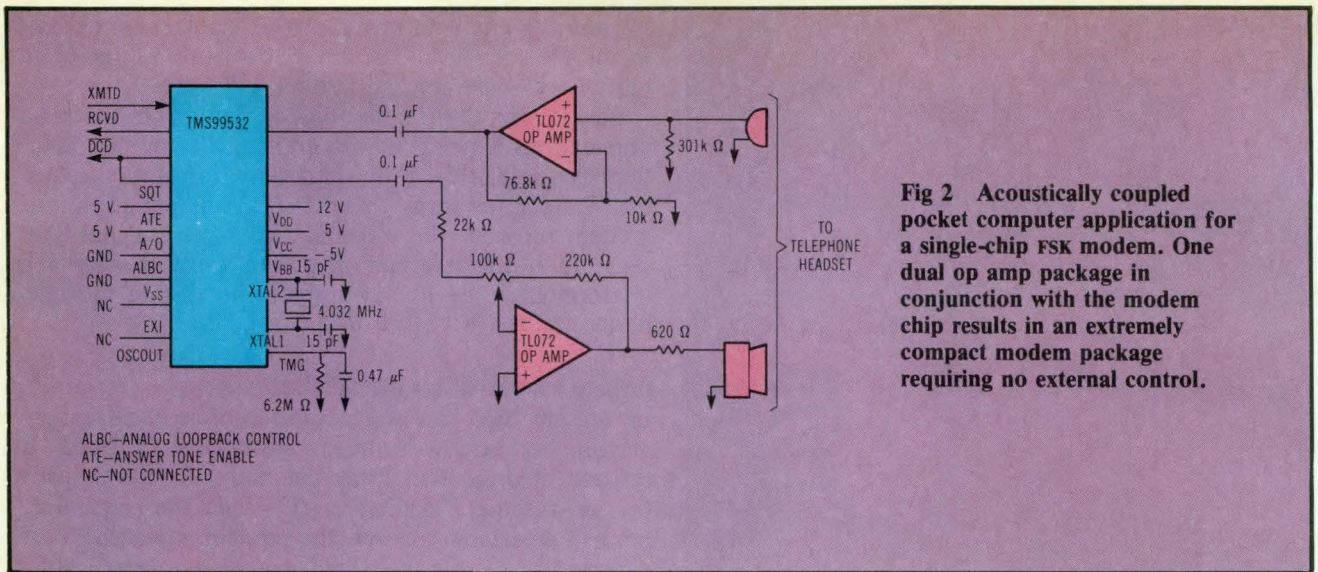
The TMS99532 modem will terminate a connection (go on hook) when a received carrier energy loss is detected. This sequence begins when the received signal level goes below the carrier detect turn-off level. If the carrier is off longer than the turn-off time delay, the modem immediately clamps the received (RCVD) signal to a mark and deactivates the DCD pin (by a logic 1) to show the carrier loss. When this happens, the SQT pin should be activated (by a logic 1) to turn off the transmit carrier. The modem is then disconnected from the network.

For the modem to remain connected to the telephone line, the data terminal ready (DTR) signal must be activated. By placing the modem on hook, DTR will not be activated and the telephone connection will be terminated. This disconnection procedure is the only way the DTE can terminate a call.

Receive, transmit, and abort are the three long-space disconnect options. In the receive disconnect sequence, the received data must be monitored for the presence of a spacing condition (logic 0) that lasts at least 1.7 s. After 1.7 s of continuous spacing, the modem goes off hook. The TMS99532 modem requires external logic to monitor RCVD for 1.7 s of space before disconnection.

The transmit disconnect sequence is similar to the data terminal not ready sequence. When DTR is not activated, the modem transmits a spacing condition (logic 0) for 2 to 4 s before going to the on-hook condition. Transmitted data going to the TMS99532's XMTD pin must be controlled by logic to implement this termination procedure.

Usually not an option, the abort disconnect sequence is used when the data set ready (DSR) signal is activated.



If a valid carrier is not received in 10 to 18 s, the modem goes to the on-hook condition. This sequence should be implemented on automatic answer modems in case the modem is called by mistake (ie, the modem will not stay connected to the telephone line in anticipation of a received carrier).

Cost-effectiveness across the gamut

The TMS99532 modem chip was designed to be cost-effective over the complete range of low speed modem designs—from the very simple to the very complex. To show how the chip can be used, consider three applications: a simple acoustically coupled application for a pocket calculator or computer; a direct connect application for instrumentation diagnostics; and a complete automatic originate and answer modem to meet general purpose data communications requirements.

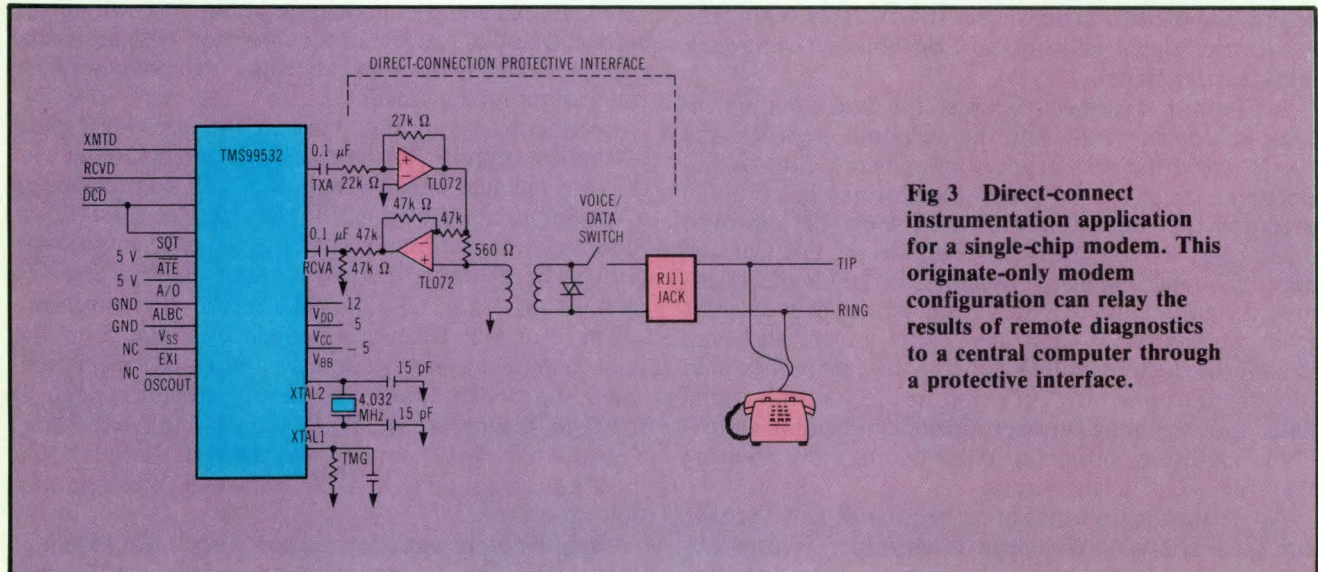
Pocket calculators and computers are becoming more intelligent, especially with the recent availability of high level languages for calculators. With such a modem based machine, a user can call up a central data base of stored software packages and downline load a particular program. The calculator or computer is then customized to a particular requirement. A user can also use the modem for general data access.

In this type of application, a modem must meet several conflicting requirements to be cost-effective. It must be small enough to carry in a briefcase with the calculator or computer; it must use little power to maintain long battery life; and, obviously, it must be very inexpensive. Finally, as acoustic coupling to a telephone is often a chancy enterprise due to distortion and ambient noise, the modem must perform well.

To meet these requirements, the TMS99532 modem (Fig 2) uses only two ICs (the TMS99532 and a dual op amp package). The modem's passive elements include one crystal, seven resistors, five capacitors, and one potentiometer (to set the transmit level). In this case, the modem is inside the DTE (the pocket calculator or computer); no external control signals are necessary.

The second application for an LSI modem package allows the modem to be electrically connected to the telephone network. As the cost of electronic instrumentation increases, downtime becomes an issue. One way to reduce field service downtime is to include a low cost modem in remote equipment, strictly for diagnostic and update purposes.

A circuit that can accomplish this places a manual, originate-only modem directly in the telephone network through a protective interface (Fig 3). If the user



Cut cost without cutting corners; Buy 4800 bps modems from UDS

Economical, cost-effective datacomm systems require economical, cost-effective modems. That's why 208s from UDS are the optimum buy.

UDS produces a basic 208A/B which may be adapted for private or public network use. In the private line ("A") configuration, the UDS 208 provides full duplex operation; when configured for the two-wire circuits ("B" version) it is a half duplex device and is FCC certified for direct connection to the dial-up network.

Three simple strapping changes determine whether the unit is in the "A" or "B" configuration. Anti-streaming protection, extensive self-

test and loop-back test capabilities are built in.

UDS 208s are available as free-standing units, OEM cards or basic components of the RM-8 multi-channel package. This version supports up to eight communications channels or a mix of modem, auto-dialer and other support cards. For the ultimate in quality, reliability and economy in 4800 bps data communications, select UDS 208s or RM-8s. Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Phone 205/837-8100; TWX 810-726-2100.

Single unit prices UDS 208 A/B, \$1750

 Universal Data Systems

 **MOTOROLA INC.**
Information Systems Group

DISTRICT OFFICES:

Old Bridge, NJ, 201/251-9090 • Blue Bell, PA, 215/643-2336 • Atlanta, 404/998-2715 • Chicago, 312/441-7450
Columbus, OH, 614/895-3025 • Boston, 617/875-8868 • Richardson, TX, 214/680-0002 • Englewood, CO, 303/694-6043
Houston, 713/988-5506 • Tustin, CA 714/669-8001 • Sunnyvale, 408/738-0433



CIRCLE 108

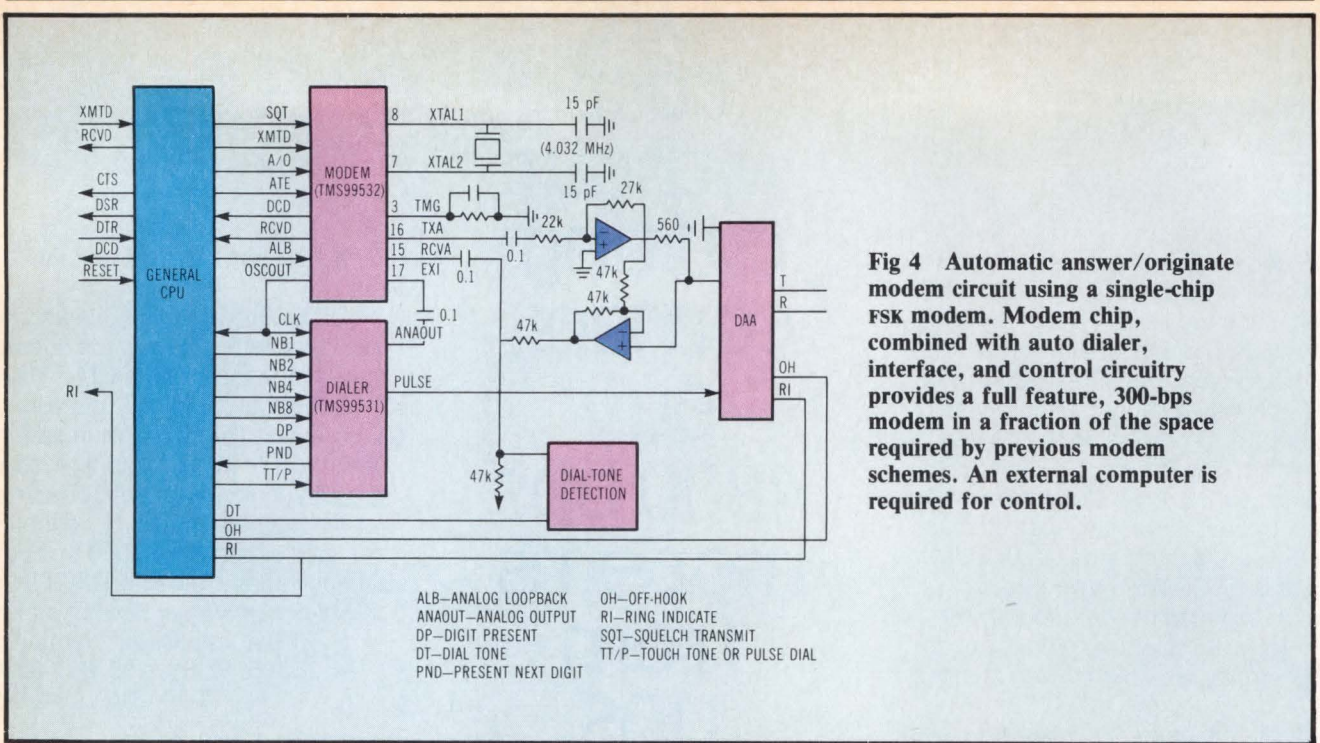


Fig 4 Automatic answer/originate modem circuit using a single-chip FSK modem. Modem chip, combined with auto dialer, interface, and control circuitry provides a full feature, 300-bps modem in a fraction of the space required by previous modem schemes. An external computer is required for control.

suspects equipment malfunction, he simply plugs the RJ11 jack into the telephone network connection. After dialing a service number and getting an answer tone, the user switches the instrument to data mode. Now the instrument can communicate directly with a central computer and run the appropriate remote diagnostics. When these are completed, the user switches back to the

voice mode and disconnects the instrument. This application requires only three signals: transmit data, receive data, and carrier detect.

An example of a general purpose data communications application is an automatic answer/originate modem that includes local intelligence (Fig 4). In this application, the TMS99532 modem is used with a TMS99531 dialer chip, a hybrid circuit, a dial-tone detect; or a direct-connect protective interface (also called a DAA) and a general purpose microcomputer for control functions. The modem interface can be RS-232-C compatible, a data bus, or a general purpose interface bus.

The protective circuit includes a ring indicator signal for automatic answering and an off-hook control signal to connect to the switched network. The dial-tone detection circuit is simply a band-limited energy detector. With a slight addition, the user can also have busy tone detection. Because the microprocessor is in control, this entire function can be made user-transparent.

As the foregoing application examples have shown, the era of the cost-effective modem is at hand. Emphasis on portability and compactness in today's small computers also abets the single-chip modem. As lightweight, compact, powerful, and more aesthetically styled micros are cloned, the inclusion of modems will be commonplace. A single-chip LSI modem operating in an FSK mode can be very advantageous for tomorrow's portable computer users. From virtually anywhere, they will be able to reach out and connect with someone.

SNA X.25

Systems Strategies/Communications Division
Specialists in Data Communications Software

225 West 34th Street
New York, New York 10001
(212) 279-8400

- Custom software to allow your product to interface networks and emulate other vendors equipment
- SNA, X.25, BSC software to communications compatible product developers for a more timely and cost effective entry into the marketplace
- Software that is utilized by computer and terminal manufacturers. Target processors have included Zilog Z-80, Z-8000, Intel 8086
- Close contact with your engineers to adapt our software to your hardware
- Software in 'C', Pascal and Assembler
- Microcomputer systems development

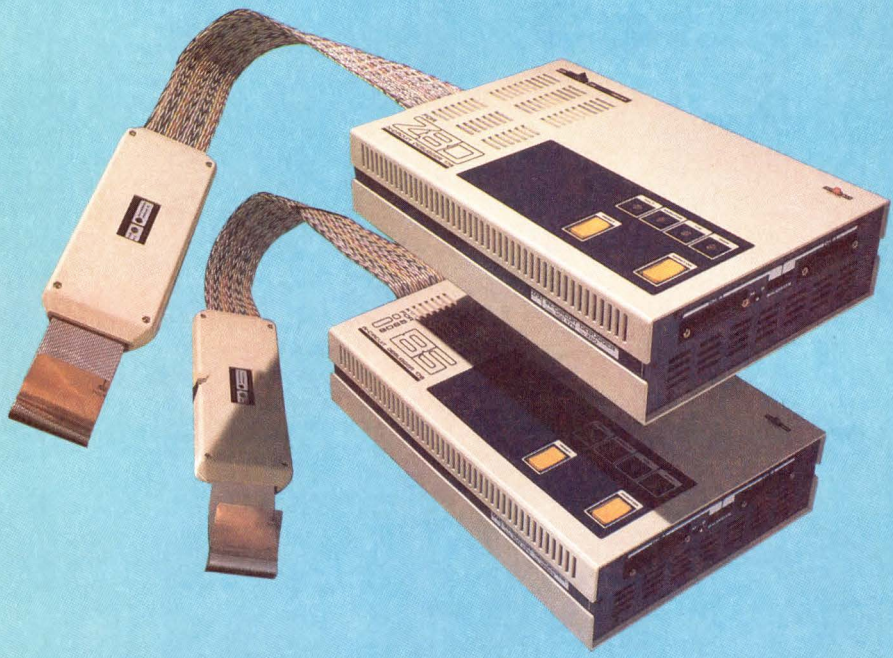
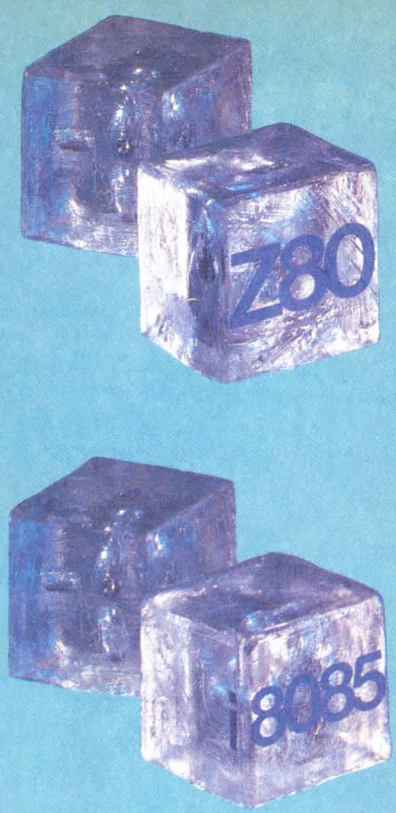
Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 713

Average 714

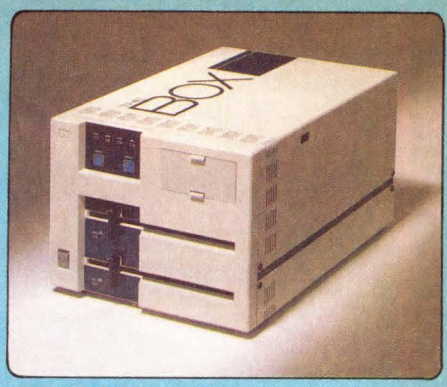
Low 715

THE ICD IN CIRCUIT DEBUGGER



ICD-178 IN-CIRCUIT EMULATORS

Z80 and 8085 In-Circuit Emulators the way they should be. A full 64K of memory for mapping. A Real-Time trace buffer 2K deep by 32 bits wide. Displays in either Hex/ASCII or Disassembled code. Code patching in either processor mnemonics or Hex. Full upload/download with host computers with no special software required. Eleven breakpoints. Three software trace functions including single step. 2 RS232 ports. All this and much more (a total of 22 different debugger commands) for only \$3995.00.



THE BOX COMPUTER

The BOX is an 8-Bit CPM Micro-Computer that connects to the ICD's to give you a μ P Development System for under \$10,000.00.



QUICK-E UV ERASER

The Quick-E UV EPROM Eraser uses the latest in flash strobe technology to erase EPROM's in just 2 to 10 seconds.



MICROCOMMUNICATOR 177III

The MicroCommunicator is compact, light weight portable terminal that gives you the added features of a printer and EPROM programmer.

Zax
Zax Corporation 8311 Westminster Ave.,
 Westminster, California 92683
 Toll Free 1-800-421-0982
 CA, HA, AK 714-898-2373

The new data comm tester that obsoletes all others.

ARC's INTERVIEW® 4500 Interactive Test System.

Now a total solution to problems encountered in data communications networks. ARC's new INTERVIEW 4500 Interactive Test System. Featuring a new concept in portable test equipment design that simplifies diagnostics of data comm problems and reduces the most complex testing to a few simple operations. **Three units in one.** The 4500 is an emulator, programmable monitor

and high speed bulk recorder. Fully emulates CPU, terminal and node. And simplifies network performance measurements.

Special capabilities to emulate packet protocols and SNA. Seven codes are standard.

The first graphic display that guides the operator in entering timing relationships between data and interface leads.

Self documented tapes allow user to build library of diagnostic tests. Unit records data and all test parameters, providing a record of system problems with the test that found the problem.

Selective recording of specific terminal, controller and logical channel eliminates time spent reviewing unrelated data. Reliable 72 Kbps recording is provided by a one megabit high speed bulk memory (optional).

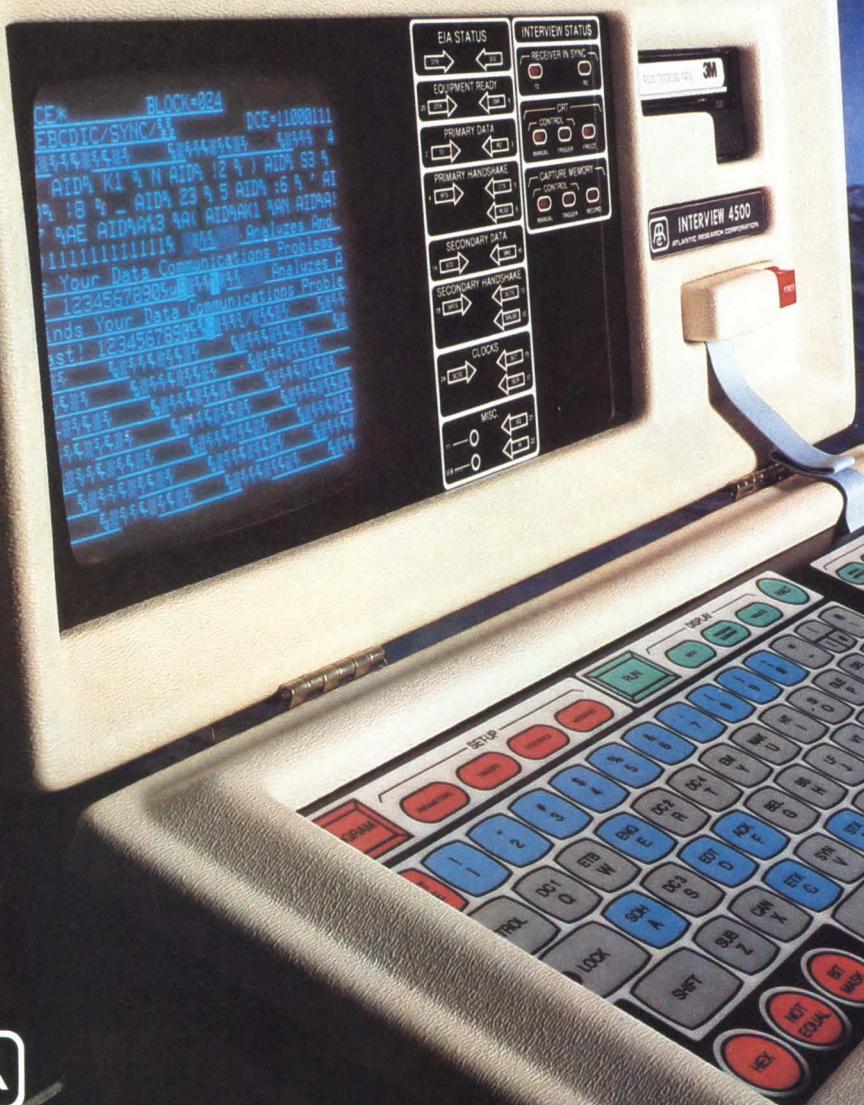
Easy to understand code converted keyboard and self-teaching menus dramatically reduce training time.

Easiest to use interactive tester. Unique triggers automatically locate problems by simultaneously looking for up to 16 test conditions.

Significantly reducing time required locating problems in the network. Developing a test is no more complicated than responding to a few simple prompts.

If you need interactive capability, your best choice is the 4500. Or you can have monitor capability now with the 3500, and convert it later to a fully interactive unit.

Call us or our representative today



Now available with the most extensive DDCMP diagnostics ever offered.

```
*MON/TAPE*          BLOCK=088
BOTH/ASCII/7/ODD/DDCMP/FRAME
```

	ADR	TYPE	OS	RES	NUM	CTL	BC1	CNT	BC2
DTE:	001	REP	10		016	%			
DCE:	001	ACK	10		016	%			
DCE:	001	REP	10		234	%			
DTE:	001	ACK	10		234	%			
DTE:	001	DAT	10		234	017		00029	
DCE:	001	ACK	10		017	%			
DCE:	001	DAT	10		235	017		00005	
DTE:	001	ACK	10		235	%			
DCE:	001	DAT	10		235	018		00098	
DCE:	001	ACK	10		018	%			
DCE:	001	DAT	10		236	018		00011	
DTE:	001	ACK	10		236	%			
DCE:	001	DAT	10		237	018		00005	

DDCMP protocol trace display includes control information and both message block check indications. Specific addresses or message types can be highlighted or suppressed from the display and it's just as easy to use an even more powerful in emulation for both sync and async DDCMP.



Atlantic Research Corporation
Teleproducts Division

5390 Cherokee Avenue, Alexandria, VA 22314
Telephone: (703) 642-4000 Telex: 248893
TWX: 710-832-9828

Representatives worldwide

See us at Interface '83, Booth #904

CIRCLE 11



IN PRAISE OF RING ARCHITECTURE FOR LOCAL AREA NETWORKS

Incorporating the concept of wire centers and the wonders of fiber optics into a ring configured LAN eliminates the traditional bugaboos associated with circular network schemes.

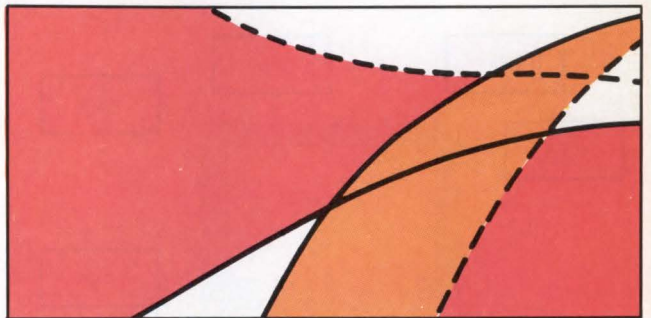
by Howard C. Salwen

Ring networks boast several advantages over bus architected networks. They are less complex and more flexible, and provide higher throughputs with guaranteed maximum access times.

It was once assumed that the carrier sense multiple access/collision detection (CSMA/CD) bus approach could provide higher reliability and would thus be adopted by the IEEE 802 committee. But the committee's initial ballots indicated that no single approach could be supported. The committee is now laboring to produce a standard document including separate sections for three techniques: token rings, token buses, and CSMA/CD buses. In the opinion of many designers, however, token rings are top achievers where reliability, maintainability, and availability are concerned.

Fig 1 illustrates three network topologies. Where many terminals desire access to a dominant central node, the star configuration (a) is applicable. A timesharing system is a good example of a star network. Obviously, such a system totally fails when the central

Howard C. Salwen is president and cofounder of Proteon Associates, Inc, 24 Crescent St, Waltham, MA 02154, where he is responsible for the design of communication and tracking systems. Mr Salwen is former chairman of the IEEE Communications Society, Boston Section, and holds BSEE and MSEE degrees from MIT.



node fails. The ring (b) and bus (c) network configurations are examples of decentralized networks that avoid the hazards of central node failures. However, they require more complex control and access strategies.¹

Trapping elusive reliability

For reliability's sake, each node in a ring network must be robust, since it must actively repeat each message. Bus topology does not require the message to be regenerated by each node. A node can fail without disrupting the bus if the failure presents high impedance to the bus. Of course, short circuits anywhere on the bus, or in the transceiver attached to the bus, cause the entire bus network to fail.

This reliability problem is often considered the major fault of ring topology. The argument against the basic ring design is that an open circuit anywhere in the ring, or failure of any repeater in the ring, disrupts service. While this is true of the basic ring design shown in Fig 1(b), most of the ring schemes in vogue are not basic

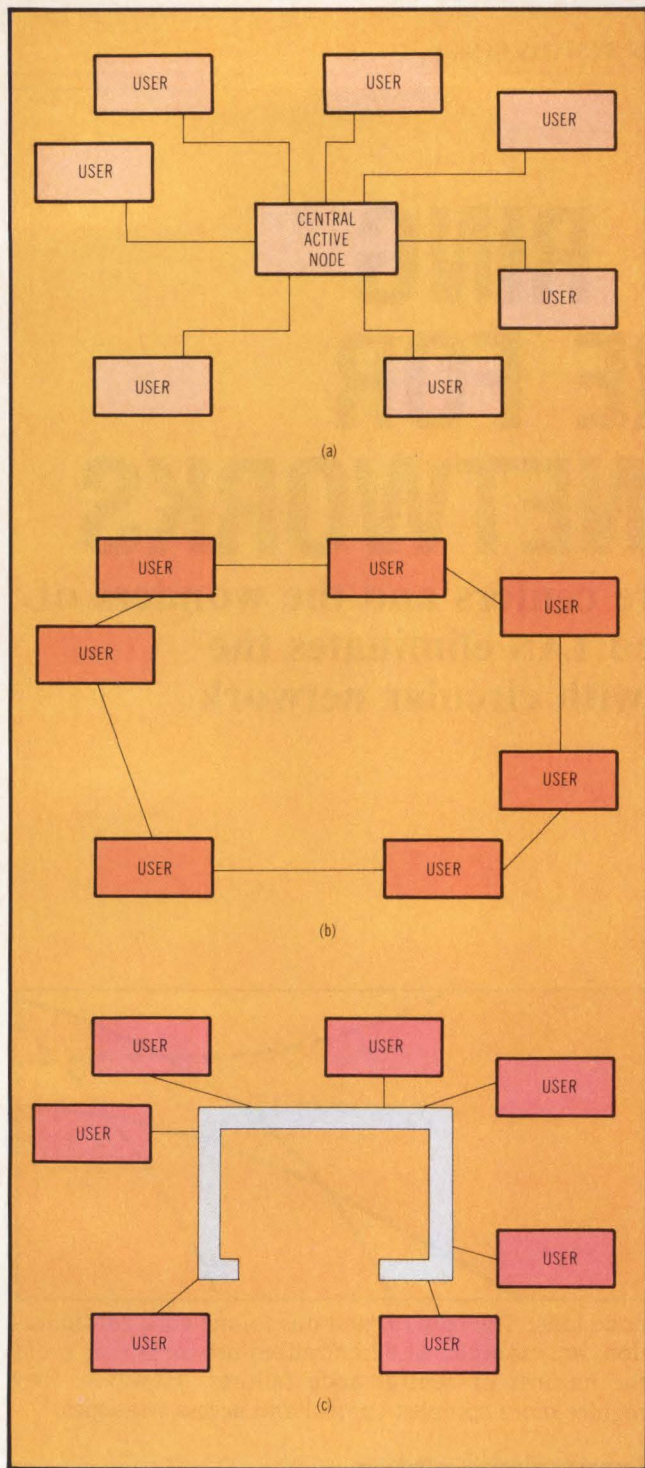


Fig 1 Three popular LAN configurations. Star scheme (a) is totally dependent upon the integrity of its central node. Ring (b) and bus (c) schemes do not suffer from this weakness in reliability.

rings. Modern ring configurations use either redundant paths or fail-safe bypassing, thus avoiding first-level failure problems.

In a discussion of ring reliability, J. R. Pierce suggests that "simple circuits" can be used to bypass failed nodes.² The wire center approach is one such circuit.³

A basic star shaped ring shown in Fig 2 is actually implemented in a wire center at the hub of a star configured network. The wire center is passive and provides a way for users to break into the ring. Attachment to the

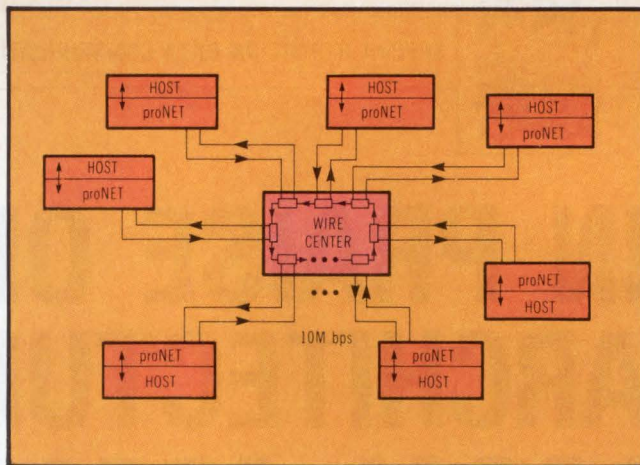


Fig 2 Star shaped ring LAN featuring a wire center. This configuration forgives failures in network nodes and its relay connections facilitate fault isolation. Many such rings can be connected by optical fiber data links.

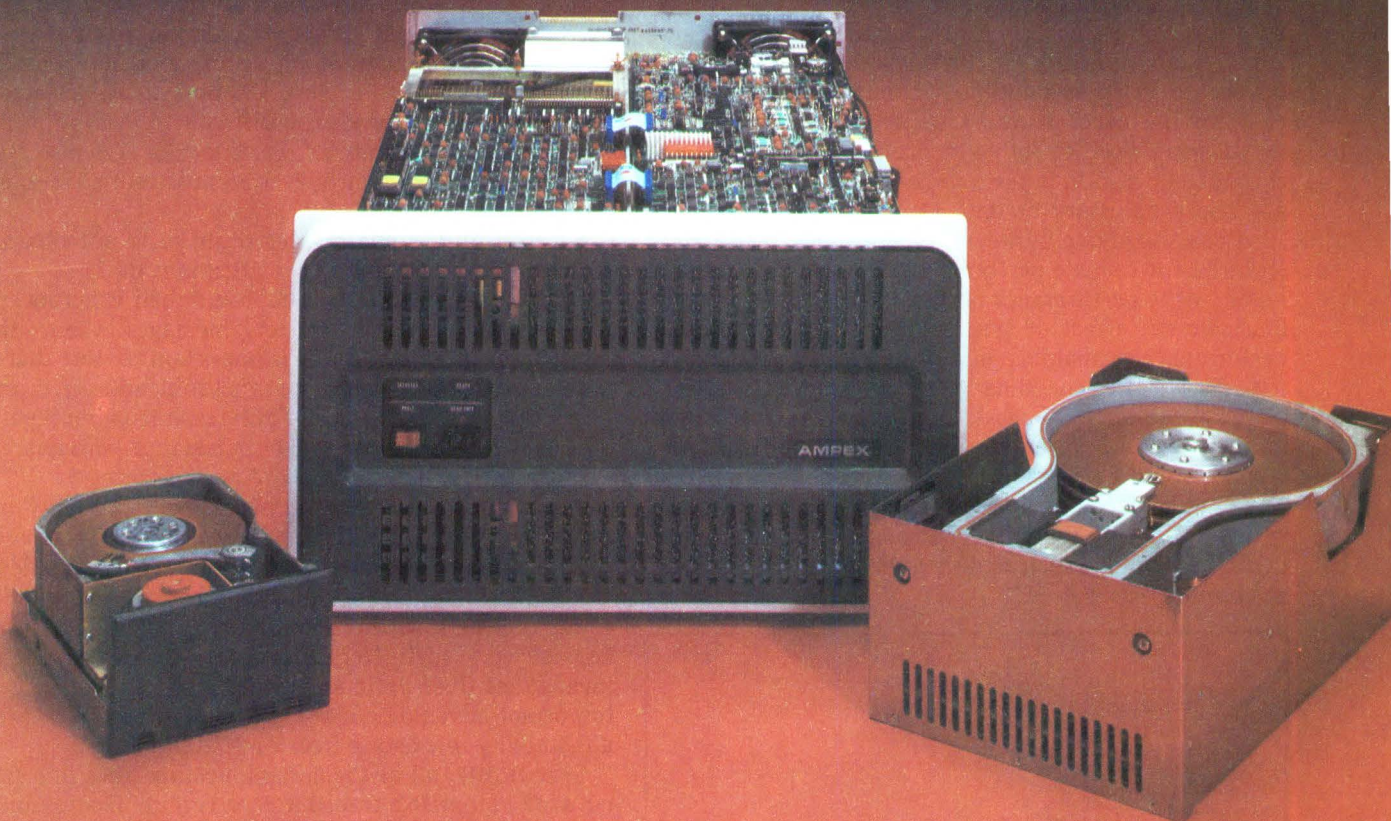
ring is usually accomplished through a relay. Energization of the relay is accomplished by the user hardware through cable from the user to the wire center. The wire center itself does not have any intrinsic power requirement. When the user host is operating properly and desires to join the ring, it energizes its associated relay at the wire center. If the cable between the host and the wire center is broken, or if the host encounters software problems or power supply failure, the relay returns to its normal de-energized state, bypassing the user. In this way, most of the first-order failure mechanisms cause the automatic bypass of a misbehaving node.

Note that both baseband and broadband bus systems are vulnerable to a variety of single-point failures. For example, a short circuit anywhere in a bus system will disrupt the bus. Similarly, a transceiver that fails to stop transmitting jams the bus. Experience with both types of systems has shown that a duality exists between ring and bus systems. For instance, open circuits are detrimental to rings, while short circuits disrupt buses. Further, repeaters that fail to transmit disrupt rings, while transceivers that fail to stop transmitting disrupt buses.

The wire center concept applied to the ring topology results in a system with a graceful failure mode. That is, defective nodes are automatically bypassed without destroying the entire system. Current baseband and broadband bus topology systems are not designed with such devices. Consider, for example, the effect of a large mismatch (short or open circuit) on a bus system employing the CSMA/CD approach. In such systems, the user listens before transmitting. If the line is not busy, the user transmits a packet of data. The user continues to listen on the chance that someone else has started a transmission at the same time. Each of the users detects the collision of their packets in the ether and backs off for a short time.

Unfortunately, a user's signal that is reflected off mismatches can make the user think that a collision has occurred although it has not. The result is an aborted transmission. Digital Equipment Corp's Ethernet system includes the equivalent of a built-in time domain reflectometer at each node. This device facilitates the detection and location of short and open circuits on the

WE'VE GOT IT ALL



FROM 7MB TO 330MB IN 5 1/4", 8" AND 14" WINCHESTER FAMILIES.

Ampex's Winchester families deliver the performance you need in today's competitive marketplace. There's 5 1/4" Pyxis with up to 27MB; 8" Scorpio with up to 83MB; and 14" Capricorn with up to 330MB. All offer the features you want, like automatic disk and head locking; industry-standard interfaces and packaging; power-up self-test and diagnostics; and capacity expansion. None requires any preventive maintenance.

Our Winchester disk drives are backed by a continuing Ampex commitment to leading-edge technology research, automated processes, and vertical

integration beginning with heads and media; by a highly professional worldwide service and support organization; and by manufacturing capacity in excess of a half-million square feet located in four countries.

That's why you can count on Ampex to deliver whatever you need in Winchester disk drives, today and tomorrow.

Ampex Corporation, Memory Products Division, 200 North Nash Street, El Segundo, CA 90245. 213-640-0150. TWX: 910-343-6243.

AMPEX

Ampex Corporation • One of The Signal Companies

CIRCLE 112

bus network. None of the available bus systems addresses this problem. On the other hand, the star shaped ring facilitates graceful failure and built-in maintainability by means of very simple circuitry.

Synchronous operation and fiber optics

Effective communication is another measure of the system's reliability. Most of the bus systems discussed so far operate in the asynchronous burst mode. Ring topology, on the other hand, with its circulating control signal, lends itself to fully synchronous operation. Synchronous operation in the local network environment is not really necessary at data rates below 1M bps. At 10M bps and above, however, synchronous operation is required for reliable performance. This point is clearly made by the performance curves of Fig 3. These curves illustrate the effect of synchronization error on error performance probability in a Manchester encoded system. Manchester encoding uses 2 transmitted bits/data bit transmitted; ie, a mark could be represented by a mark-space pattern on the communication channel and a space could be represented by a space-mark pattern. Manchester encoding is used in many communication systems such as Ethernet and Proteon's proNET and in other applications such as disk recording systems where ac coupling is required.

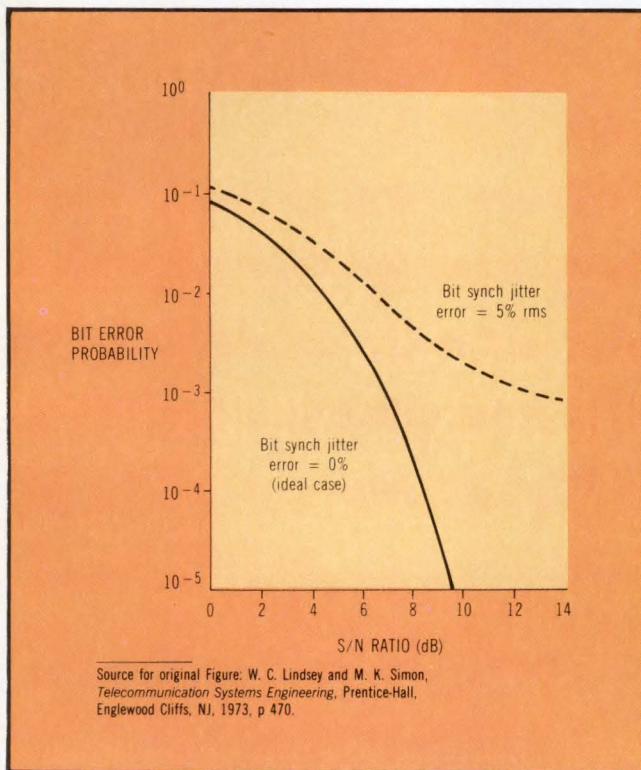


Fig 3 Effect of bit synchronization error on network performance. With jitter error of 5% (dashed line), unacceptable error rates are achieved even when S/N ratios are high.

In Fig 3, the probability of bit error as a function of signal to noise (S/N) ratio is plotted for two cases: the lower solid curve represents the ideal, and the upper dashed curve shows the effect of bit synchronization error. Note, for example, that a 5% root mean square (rms) bit synch jitter error (dashed curve) results in an

error probability of 10^{-3} when the S/N ratio is 12 dB. In the absence of such synchronization error, 12 dB would provide extremely high performance.

If the results shown in Fig 3 are extended to higher S/N density ratios, marginally acceptable error rate performance can be achieved at 5% bit jitter when S/N ratios exceed 50 or 60 dB. When the system is running at 10M bps, the estimate of bit synchronization must be less than 5 ns rms to achieve 5% bit synch jitter error. Such performance levels are difficult to achieve in the burst mode. Synchronous, phase locked systems easily achieve this performance level because more averaging time is used.

Severity of the phase jitter problem is not obvious from the Ethernet Phase I specification. DEC has a synchronization quality circuit built into their Ethernet system that automatically rejects messages when jitter levels threaten reliability. It is important to note that in a burst mode bus system, the synchronization error can be caused by noise, but it can also result from multipath-type reflections caused by impedance mismatches throughout the network.

Very soon, large local networks will probably use broadband techniques that employ fiber optic transmission technology. Current fiber optic technology allows the implementation of long transmission links with fewer repeaters when compared to similar links using coaxial very high frequency (vhf) technology. This means that fiber optic links will be more reliable. One important advantage of the ring design approach is its adaptability to existing fiber optic technology.

Specifically, all of the communication links in a ring network comprise a transmitter, a communication link, and a single receiver. This configuration is easily implemented with available fiber optic components. (See *Computer Design*, Jan 1983, p 75, "Effectively Link Microcomputers with Fiber Optics.") The bus approach requires an n-way coupler, which limits the number of users to around 10 per system if reasonable separations are to be achieved. The star shaped ring requires more fiber optic transmitter and receiver modules. But again, each link is an elementary simplex link.

Maintaining reliability a must

Any reliable system must be decentralized. That is, operation of the system should not depend upon the performance or availability of unique system elements such as master clocks or token management hardware. Token ring systems with fully decentralized clock distribution plus token management and error recovery can, and are, being designed. The techniques employed are substantially simpler than those required by a token bus system.

As mentioned, the wire center concept allows the system to fail gracefully. This ability reduces the maintenance burden, since not all failures require an immediate reaction. The wire center scheme discussed provides an even more useful function in this respect—it enables rapid fault isolation. The wire centers play the same role in the communication network as a circuit breaker panel plays in a power distribution network. If a defective node tries to attach itself to the ring, the wire center causes that node to be bypassed without disrupting the whole ring. Wire centers also provide

More Multibus.™ And less.

VMC 186 VIDEO MONITOR CONTROLLER 80 Character X 24 line alphanumeric and limited graphic display. Upper and lower case, Reverse, half-intensity, flashing, and underline attributes.

FDC 1680 FLOPPY DISK CONTROLLER WITH 16K RAM 4 single density drives. Automatic DMA into the dual-ported on-Board 16K RAM.

SMD 2181 STORAGE MODULE CONTROLLER Same as SMD 2180 except *damned* fast DMA 24 bit addressing, 11 bit Error Correction, software selectable sector size and interleave. *Can transfer a full track in one disk revolution.*

WDC 2880 WINCHESTER DISK CONTROLLER Up to 8 drives with ANSI X3T9.3 interface. Very high speed DMA, 20 bit address. Software selectable sector size and interleave factor, 11 bit Error Correction.

We're constantly at work creating new capabilities for Multibus.

LAN 5180 LOCAL AREA NETWORK CONTROLLER Up to 255 devices are supported on a coaxial cable. Data rates up to 2 Mb/Sec. SDLC/HDLC protocol, 20 bit DMA, automatic transaction completion, mailboxes. First in a family of LAN products.

HDC 1880 HARD DISK CONTROLLER Up to 4 cartridge (5440 type) disk drives. High speed 20 bit DMA. Automatic Retry, ECC, switch selectable sector size and interleave.

SMD 2180 STORAGE MODULE CONTROLLER Up to 4 SMD compatible drives (including CDC LARK), 8-300 Mbytes, bit rates to 20 Mb/S. High Speed 20 bit DMA, ECC, switch selectable sector size and interleave.

Now, the most talented Multibus specialists in the country bring you more Multibus options than ever before. And less.

More technology with less risk. More function

with less cost. And more support with less hassle.

When you're ready to expand your Multibus capabilities, talk to us. We're the specialists who give you more. And less.

Entire rigid disk controller family is software interchangeable. Automatic completion of simple multisector commands, automatic recovery from errors, bad track mapping, full sector buffering, extensive diagnostic reporting. Variable burst DMA in 8 or 16 bit systems. Software drivers and disk subsystems also available.



We stay ahead of our competition so you can stay ahead of yours.
13667 Floyd Circle/Dallas, Texas 75243/(214)238-0971

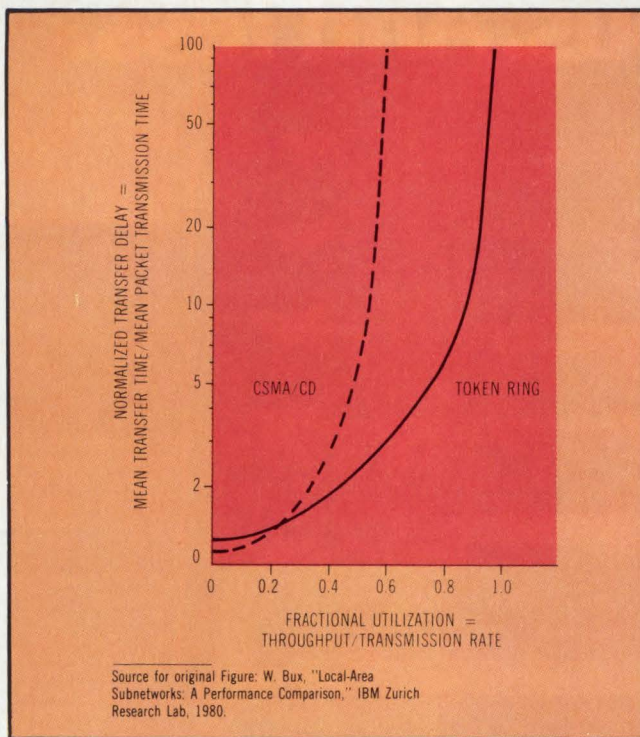


Fig 4 Performance comparison of CSMA/CD system versus token ring system. Given similar network parameters, token ring system offers higher performance and faster access.

centralized locations where signals can be monitored, and a manual means for dropping or adding nodes to the ring. Thus, the wire centers substantially reduce the mean time to repair the network.

Rapid fault isolation and short mean time to repair improve the network's availability. The token approach further enhances availability by establishing a guaranteed maximum waiting time before access is granted. Fig 4 shows the normalized mean time to transmit as a

system loading function for CSMA/CD systems versus token passing ring networks. The CSMA/CD system depicted is assumed to be 2 km in length; the token ring is assumed to be 2 km in circumference. Both systems have 50 active nodes and an assumed 1000-bit average message length. Under these conditions, the maximum achievable throughput on the CSMA/CD system is about 6M bps, achieved with infinite waiting times. Throughput on the token ring system asymptotically approaches a value just below 10M bps. Typical token ring protocols impose a maximum packet size. Given a 50-node network and a 1000-byte maximum packet size, the maximum time before access to the system is approximately 40 ms.

The proNET local area network (LAN) illustrates the various design concepts of ring network schemes. ProNET is a token arbitrated, ring local network operating at 10M bps. Up to 255 users can be supported by each ring. The proNET configuration in Fig 5 is an extension of the star shaped ring concept. In fact, it is a string of stars or a "constellation." Short runs from a wire center to various computers in a computer room can be interconnected with twisted pairs. Long runs from one wire center to another can be implemented with dual fiber optic links. Note that the wire center attachment point for fiber optic links includes a bypassing relay. If the fiber optic link connecting the two wire centers were to fail, the system would automatically partition itself into two star shaped rings. In this case, no interconnecting fiber optic link exists between them.

At each node or host there are two hardware modules: a control board (CTL) and a host specific interface board (HSB). The CTL hardware module performs bit-level network functions and signal modulation/demodulation required for data transmission through the transmission medium. The HSB module contains a full-duplex direct memory access (DMA) interface to the host. In addition, this board contains two separate

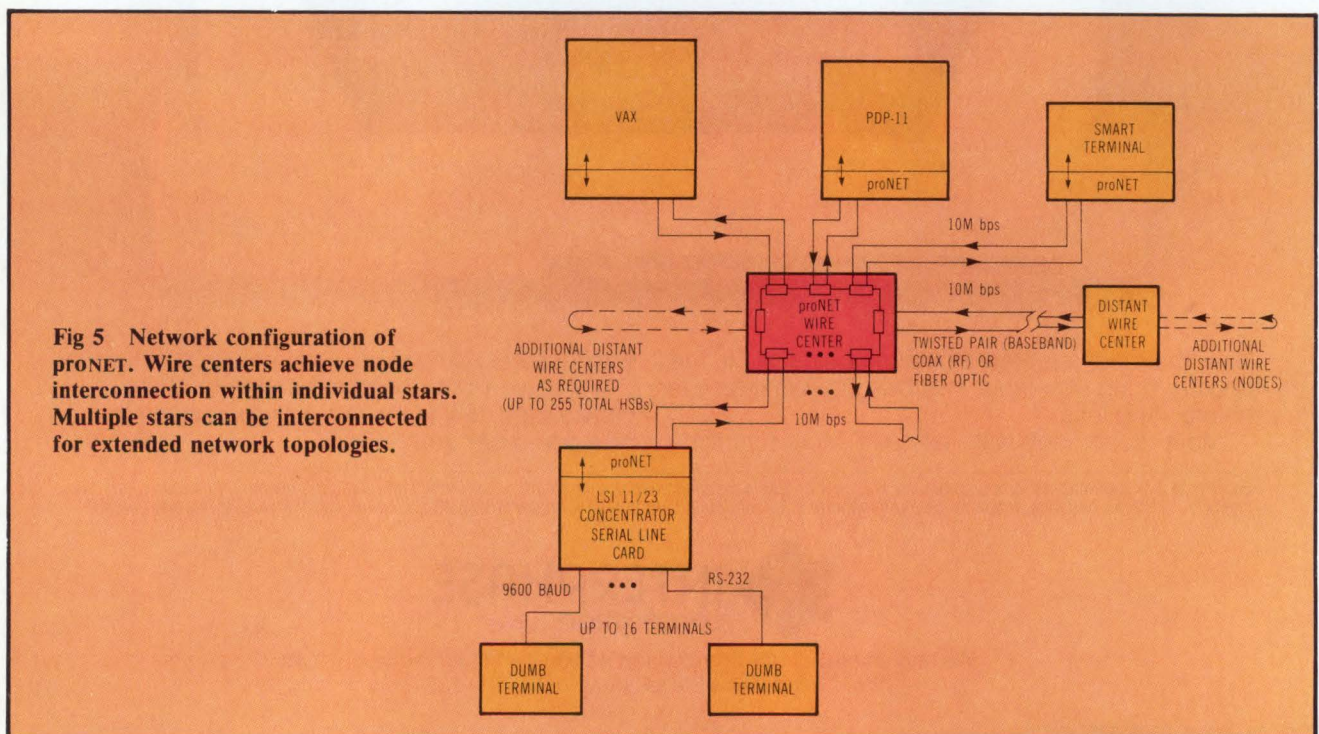


Fig 5 Network configuration of proNET. Wire centers achieve node interconnection within individual stars. Multiple stars can be interconnected for extended network topologies.

"Racal-Vadic's Invisible Modem Gives Grid's Ultra-Portable Computer Access to a Whole World of Data!"

Dave Hanna — V.P. Marketing and Sales, Grid Systems, Inc., Palo Alto, California

One of the hottest personal computers on the market is the new Grid Compass. It weighs about 10 pounds and takes up less than half of a standard briefcase.

Business Week calls Compass "a Porsche for top executives."

A custom Racal-Vadic modem is behind the smashing success of Compass. This VS212A/103 modem — complete with auto dial and auto answer — is built on a 6" by 6" PC board.

"Without this built-in modem we couldn't have made the product," says Glenn Edens, V.P. of Development for Grid Systems, Inc., Palo Alto, California.

Racal-Vadic's incredibly small modem is vital because it gives Compass a unique communication capability, setting it apart from other portable computers. For example, Compass can "talk" to another Compass... or to Compass Central, a user-owned, 240 Mbyte desk-top computer, which is designed to support a number of Compass computers in the field. It can also access Grid Central, a Grid-owned mainframe which distributes new software and provides data storage for its users. And there's more! The ultra-portable Compass can access corporate mainframes and public data bases.

Imagine... a Fortune 500 executive in a hotel room with the whole wide world of data at his or her fingertips — using the dial-up telephone.

Why Racal-Vadic? Because we invented 1200 bps full-duplex technology. Because we ship more modems than anyone. Because we utilize the most advanced automated production equipment and superb quality control. And because our custom modem department is dedicated to creating integral modems for OEMs.

WE DID IT FOR GRID. WE CAN DO IT FOR YOU!



Racal-Vadic

Member IDCMA

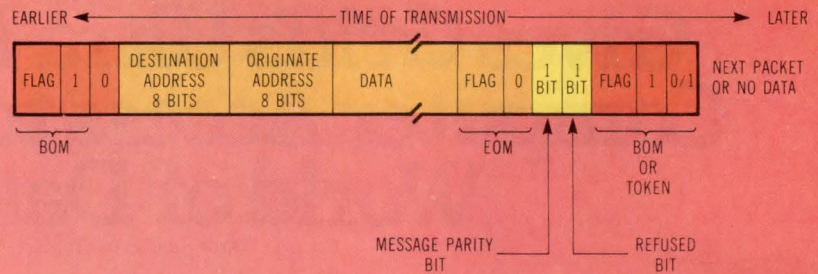
222 Caspian Drive, Sunnyvale, CA 94086
Tel: (408) 744-0810 • TWX: 910-339-9297

RACAL

"See us at Interface Booth 633"

CIRCLE 114

Fig 6 Packet format in PRONET.
 Maximum data field of 2044 bytes can be accommodated with 255 destination and source addresses.



2046-byte (1023-word) packet buffers, plus control and status registers. In short, all of the firmware needed for an automatic communications operation is supplied. This minimizes the host's software burden imposed by the communication network.

The wire centers shown in Fig 5 are passive. Control signals for the node relays are passed through the transmission medium to the wire center by each respective node. Maintenance switches included in each wire center override node relay control. This improves network fault isolation and reliability. Loopback testing is also implemented by the wire center. In this way, a host can check out the entire circuit right up to the attachment point before joining the ring.

Fig 6 illustrates the network's data link format and control characters. An important feature of the data encapsulation format is the absence of a word count field. Each packet can have a variable number of data bytes, since the end of message (EOM) control character serves as a data field boundary. Size of the packet buffer memory is the only restricting factor on the number of data bytes placed on the network. PRONET's HSB allows a maximum data field of 2044 8-bit bytes, plus 1 byte each of destination and source address data.

Every node within the ring network is identified by means of its node address. An 8-bit switch on the CTL allows 255-node address selection, with address 255 reserved as the network-wide broadcast address. An 8-bit source address follows the destination address in the data encapsulation format. The source address is equal to the node address as set by the 8-bit switch on the CTL card. Hardware automatically inserts this source address into the second byte of the message data received from the HSB.

Bit stuffing of the network data stream is implemented by inserting a 0 bit after detection of six consecutive 1s in the outgoing data. Destuffing and control character decoding is accomplished on the CTL by detecting a 0 followed by six 1s and then examining the 7th bit. A 0 here indicates the data stream contains a stuffed bit; a 1 indicates a control character (flag). If the sequence is a flag, the two bits following the flag are examined to determine whether the character is a beginning of message (BOM), EOM, or token. Since control characters consist of specific 8- or 9-bit patterns, they are rarely generated by accident.

Messages can be placed on the ring only if a valid token has been detected by the node wishing to transmit. At idle, the ring network circulates a token control character around the ring. If a node has a request to send

pending, the CTL will convert the next received token into a BOM character by changing its last bit, marking a BOM. Converting the token into a BOM ensures orderly queuing among nodes wishing to place messages on the ring. A token sent at the end of the message will allow nodes that are downstream of the originating node to place messages on the ring.

This data communication technique allows for simple 1-way communication between nodes. Low error rates are obtained on runs of several thousand feet between nodes at baseband parameters. The biphasic modulation technique allows the nodes to be ac coupled. Frequency components below 1 MHz are rejected by filtering at each node so that the network is relatively immune to ambient noise. The communication medium for runs of under 300' (91 m) can be inexpensive twisted pair cable. Longer runs can be made with dual-axial cable. In addition, the network can be adapted to other transmission media, such as modulated radio frequency (rf) on coaxial cable or fiber optic links. In fact, 4-km links using fiber optics are available. Such links can be employed between wire centers so that networks many kilometers in length are feasible. In addition, token architecture does not limit maximum propagation delay across the network as CSMA/CD does.

Operational modes provide flexibility

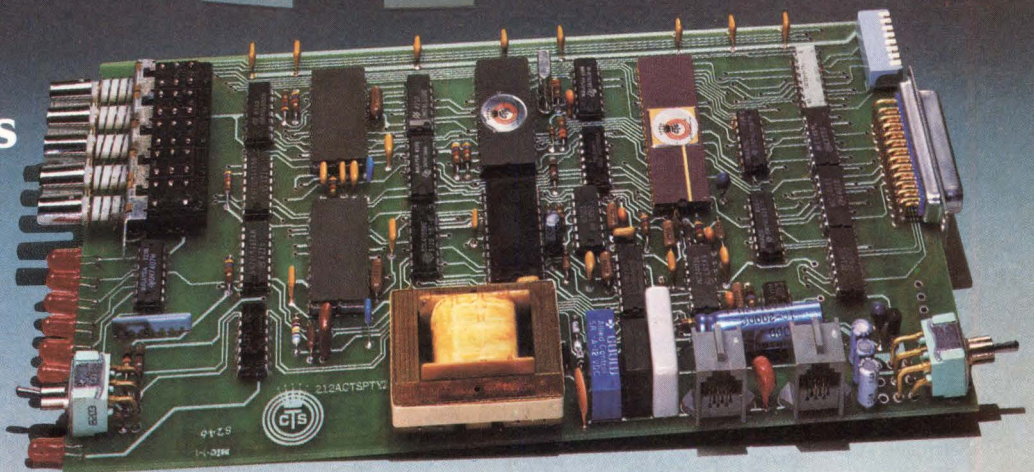
In the network configuration described, four operating modes are available: repeat, copy, originate, and initialize. In addition, there are two possible test configurations: digital loopback and analog loopback. The CTL is usually found in the repeat mode, where the CTL repeats data on the ring. The data received from the adjacent node upstream are passed to the next node downstream.

The CTL automatically switches from the repeat mode to the copy mode if it determines that the message passing through it is intended for its associated host processor. Specifically, the message will be copied if the destination address in the message corresponds to the CTL's address. It will also be copied if the message has the broadcast address. Alternatively, the CTL can be strapped in the match-all configuration, allowing any message to be copied.

When copying or originating, the host's operations are similar in complexity to those required when writing to or reading from a disk. For example, when the host desires to transmit a message to another node, it carries out an originate operation. It begins when the packet to be sent is transferred from the host memory to an output packet buffer on the HSB. Then, upon recognition

Phone lines garbling your data?

**CTS 212A
COMPATIBLE
CUSTOM MODEMS**
deliver superb
error-free data
communication
—even over poor
phone lines



Bit error rate performance is what everyone demands in a 212A Modem. This new, advanced CTS integral Modem delivers far better signal-to-noise rejection consistently because CTS uses digital signal processing. And it does it with excellent front end dynamic range of 72dB which is considerably higher than usual. You get consistent error-free signal transmission and reception—free from garbled data or lost bits due to less than adequate phone lines. Synchronous detection, in the low speed mode, allows increased performance to 600bps FSK.

Tightly controlled, rigidly maintained manufacturing processes assure consistent performance—from the first modem to the 50,000th unit. And with years of experience in supplying high-reliability electronics, CTS was a natural choice to be the sole supplier of modems to a leading personal computer firm.

Write for complete data on these CTS 212A Modems, customized to your needs, without a price premium. Contact CTS Corporation, 1201 Cumberland Ave., West Lafayette, IN 47906. Phone: (317) 463-2565.

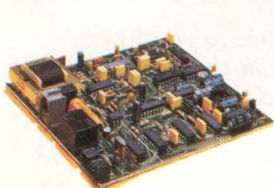
CIRCLE 115



CTS builds Custom Modems your way—Bell compatible, offering superior performance—without a price premium. ■ 0-600 or 1200bps operation. ■ Both synchronous and asynchronous. ■ Custom connectors: flat cable, card edge or any variety you specify. ■ Both DTMF and pulse dialing capability. ■ Interface by software command or RS232. ■ Full telephone line status information. ■ Excellent bit-error rate performance. ■ Built in diagnostics and full loopback features. ■ Smallest 212A customized Modem we've seen to date. Less than 40 square inches! ■ FCC Part 68 approval and UL certified. ■ CCITT V.22 capability. ■ Minimum yearly quantity—1000 units

CTS means Reliability

CTS CORPORATION • ELKHART, INDIANA



Microcomputer
Integral Modem



Point-of-Sale Modem



Remote Monitoring
Equipment Modem



Data Acquisition
Equipment Modem

of the token, the CTL changes it to a BOM, transmits the message, and ends it with a token. Once the message circumnavigates the ring, the CTL removes it, leaving the following message or token intact. If the ring network does not have a valid token control character circulating it, the CTL module can create one by initializing the ring in response to an initialize request from the host processor.

The initialize mode is essentially the same as the originate mode, with one important exception: The CTL does not wait until an access control token passes into it before sending the message. In this way, the CTL module forces a message onto the ring. It removes the returning message, leaving only the valid token circulating on the ring.

Since every CTL module can initialize the ring in this fully decentralized network, it is important to avoid simultaneous attempts at initialization by two or more CTLs. Initialization of PRONET is assumed to be random due to the random arrival of users. Typically, an originate request to the CTL is accompanied by an initialize request. However, if the CTL monitoring circuitry indicates that a valid token is circulating and flags are being seen at the required rate, the initialize request is blocked. If, at the instant of initialize request, the CTL indicates that the ring is not available, the origination is carried out immediately. Of course, it is still possible for two originators to arrive simultaneously at the network, causing each to think the ring is not available. As a result, each will attempt to initialize the ring, causing

each CTL to drain the other's message. Each will then report a "message lost" to its associated host through the HSB, and the ring will remain without a token. The next originator who arrives at the ring will initialize it, while the first two are executing software-randomized timeouts.

In the normal mode of operation, the CTL receives data from its adjacent node upstream, and transmits data to the next node downstream. Two test configurations, digital and analog loopback, are also implemented under host control.

Digital loopback can be used to test all portions of the CTL/HSB, except for the modem and cable interconnection. All four modes of operation can be analyzed in digital loopback and all hardware associated with the operation can be tested without actually disturbing the existing network. Analog loopback is a special operation implemented with a wire center. It allows the user to test all CTL circuitry and cables leading to a wire center, without disturbing the existing network.

Fully decentralized, token arbitrated ring networks provide superior reliability, maintainability, and communication availability. For these reasons, they are becoming widely accepted by network users.

References

1. D. D. Clark, K. T. Pograd, and D. T. Reed, "An Introduction to Local Area Networks," *Proceedings of IEEE 66*, vol 11, 1978, pp 1497-1517.
2. J. R. Pierce, "How Far Can Loops Go?" *IEEE Transaction on Communications*, vol COM-20, 1972, pp 527-530.
3. J. H. Saltzer and K. T. Pograd, "A Star-Shaped Ring Network with High Maintainability," *Proceedings of the Local Area Communications Network Symposium*, MITRE Corp, 1979.

Bibliography

- P. Abramson and F. E. Noel, "Local Area Network Media Selection for Ring Topologies," IBM, July 27, 1982.
- H. Meyr, H. Bouten, H. R. Muller, and U. Bapst, "Manchester Coding with Predistortion: An Efficient and Simple Transmission Technique in Local Digital Ring Networks," IBM research report RZ 1042, Nov 17, 1980.
- P. V. Mockapetris, M. R. Lyle, and D. J. Farber, "On the Design of Local Network Interfaces," *Information Processing 77*, B. Gilchrist, ed, IPIF North-Holland Publishing Co, 1977.
- J. F. Shoch and J. A. Hupp, "Performance of an Ethernet Local Network—A Preliminary Report," *Proceedings of the Local Area Communications Network Symposium*, MITRE Corp, 1979.
- M. V. Wilkes and D. J. Wheeler, "The Cambridge Digital Communications Ring," *Proceedings of the Local Area Communications Network Symposium*, MITRE Corp, 1979.

SENIOR FIRMWARE ENGINEERS

Data Communications

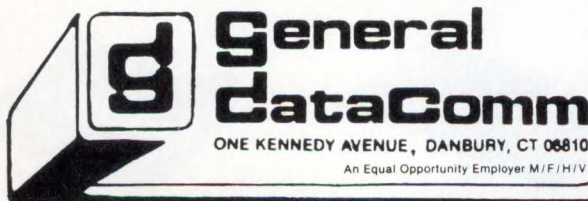
At General DataComm, we're recognized worldwide for our technological leadership in the design and development of data communications products including network management systems, multiplexers and voice band modems. On-going, dynamic growth has created the need for innovative, seasoned professionals to join us as Group Leaders to take charge in the development of high level micro systems.

To have the responsibility of systems design, software development and integration of advanced communication networks, you must have hands-on experience in the development of real-time, interrupt driven micro systems plus a knowledge of mainframe communication protocols.

We're located in southern New England where you can take advantage of major cosmopolitan cities and year round recreational facilities. We offer excellent salaries free from state income taxes, and generous benefits.

To explore career opportunities in the field of data communications, please call, send your resume or drop a line in confidence to:

Michael Blazak
(203) 797-0711 ext. 950



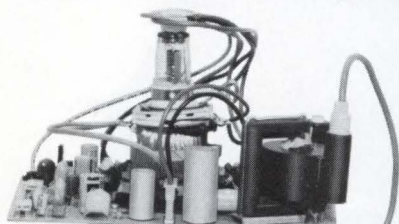
Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 716

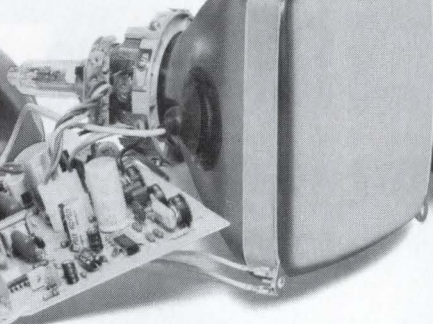
Average 717

Low 718

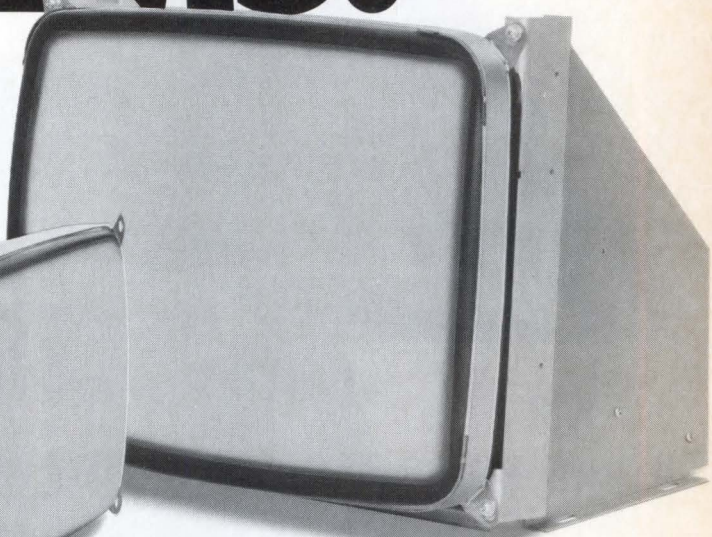
WE SOLVE PROBLEMS!



Integrated PCB



Kit form



Chassis version

Meet some of our new problem solvers.

High performance, innovative design data displays in 9", 12" and 15" screen sizes, for system designers like you. And they're all available in integrated, chassis or kit versions.

Using these basic displays, our engineers become your engineers! They custom design a display for your specific application, meeting your particular system design requirements.

Scanning frequencies to 32 KHz and more. Up to 1200 line resolution. TTL or composite

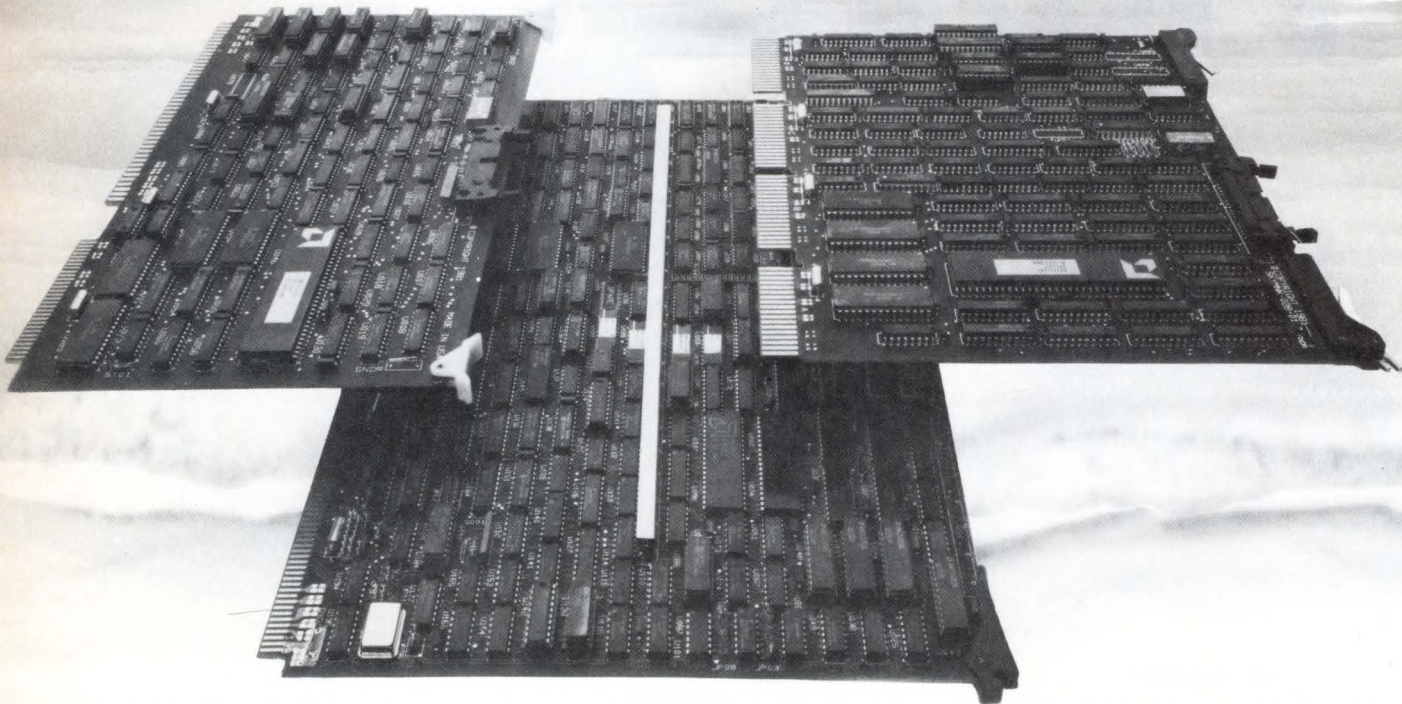
video. 120 or 240V AC, or 12 or 24V DC. Give us your specifications and we'll solve all your display problems. And we'll deliver on time, when you want them.

Audiotronics has been solving problems for over 25 years, designing hundreds of custom data displays for important customers, large and small. Call today. Turn our engineers loose with your display system problems.



North Hollywood
California 91605
(213) 765-2645

We Crunch Numbers Not Budgets



Crunching numbers used to mean also crunching your budget. Big problems required big machines. Megaflops meant Megabucks. **No more!** At SKY Computers, we believe you'd really rather use a micro. If only it were fast enough. Well, now it can be. Our high-speed, low cost array processors are designed to plug right into your Q-bus, VERSAbus, or Multibus system and give your microcomputer VAX 11/780 performance at a micro price.

You'll find SKY'S Micro Number Crunchers (SKYMNK's) in the best of

places. In real time laboratory signal processing systems, in field exploration systems doing seismic analysis, in graphics workstations doing 3-D coordinate transformations, and in imaging systems doing 2-D FFT's. Anywhere fast interaction with lots of data is important.

And now, if you thought hardware floating-point support for the MC68000 was a year or more away, **you're in for a pleasant surprise!** Our new SKYFFP Floating-Point Processor provides both 32-bit and 64-bit precision IEEE Format

arithmetic on a single plug-in card, for the Multibus and VME bus.

Our SKYMNK and SKYFFP are unsurpassed in ease of use and reliability. Our users say so! They'll also tell you that SKY Computers offers the best customer support in the industry.

Challenge us with your requirements. Call us for our free benchmark analysis.

Circle the bingo and we will promptly send you descriptive data on our products. For immediate response, call SKY at 617-454-6200.

Remember. We do lots of things to crunch numbers. None of them will crunch your budget.

CIRCLE 118

SKY COMPUTERS, INC. Foot of John Street Lowell, MA 01852 (617) 454-6200 TELEX 4991331 SKYMNK
London: Data Translation LTD, Munich: Stemmer Elektronik, Paris: Metrologik, Tokyo: ASR International, Toronto: Transduction LTD



BIT ORIENTED DATA LINK CONTROLS

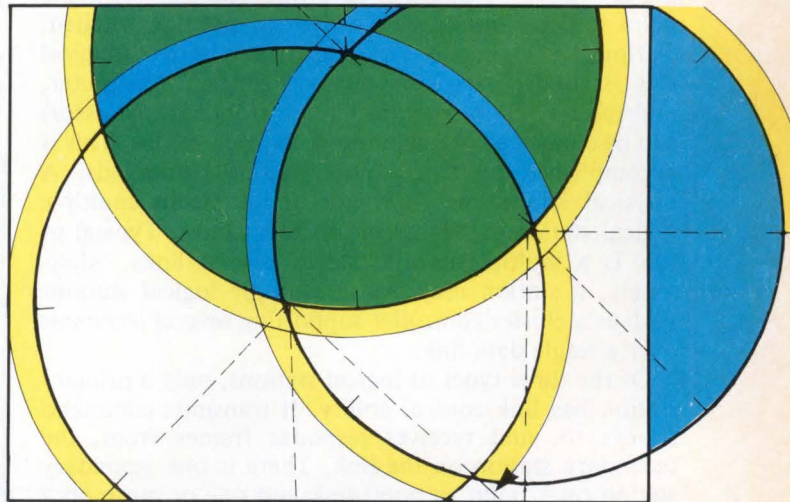
A bit oriented approach to network control is finding increased acceptance among many national and international standards organizations. The simplicity of the single-frame format is just one reason.

by Alan J. Weissberger

The International Standards Organization's Open Systems Interconnection/Reference Model lays the foundation for data communications architecture. As a result, in an open systems environment, end-user hardware such as terminals, workstations, cluster controllers, and computers communicate via a 7-layer peer to peer protocol. The data link layer is the second layer in the model. It provides one of the lowest levels of interconnect, provides services to the network layer above, and uses the services of the physical layer below.

As defined by the International Standards Organization (ISO), a data link control (DLC) is simply a set of rules for orderly information interchange between physically connected stations. Further, there can be one or more data link stations per data terminal equipment. Frontend processors, multiplexers, and remote data concentrators often handle several data links and thus contain many data link stations. Among the most popular DLCs are high level data link control (HDLC), advanced data communications control procedure (ADCCP), X.25 and X.75 link levels, IBM synchronous data link control (SDLC), DEC digital data communications message protocol (DDCMP), and IBM binary synchronous (bisync) communications.

Alan J. Weissberger is technical director of advanced technology at Memorex Corp, 18922 Forge Dr, Cupertino, CA 95014. Mr Weissberger is responsible for planning, systems architecture, and systems integration of data communications products. He is a participating member of ANSI X353.7 and a senior member of the IEEE.



The three categories of DLCs appear in Table 1; Table 2 compares their features. Standards organizations and the U.S. Government have adopted bit oriented procedures as the preferred method of data link control. Similarly, computer manufacturers have adopted bit oriented DLCs for the link layer of their proprietary network architectures. Bit oriented procedures are distinguished from character oriented procedures by the absence of American National Standard Code for Information Interchange (ASCII), extended binary coded decimal interchange (EBCDIC), or other information coded characters for link control. Unlike character oriented DLCs, the attributes of bit oriented DLCs—single-frame format, unrestricted information field length, use of any character code, and only three reserved bit sequences—simplify software design and maintenance.

TABLE 1
Three Categories of DLCs

Character Control		Character Count	Bit Oriented	
ANSI	X3.28	DEC DDCMP	ANSI	X.3.66 (ADCCP)
ISO	1745, 2111, 2628 2629 (Basic mode)	Statistical Multiplexers	ISO	3309, 4335, 6159, 6256 (HDLC)
ECMA	16, 24, 26, 27, 28, 29, 37	Satellite Communications	CCITT	X.25 LAP, LAPB X.75 link level
IATA	SLC		ECMA	40, 49, 60, 61, 72 (HDLC)
IBM	BISYNC		Federal Government	Fed Std 1003A FIPS 71
			IBM	SDLC
			Burroughs	BDLC
			Univac	UDLC

Operating across the spectrum

HDLC covers many applications including 2-way alternate and 2-way simultaneous data communications. Communications can occur between computers, cluster controllers, concentrators, and buffered terminals, and a wide range of physical data link schemes including point to point, multipoint, switched, and nonswitched. Various HDLC functions are specified in terms of logical DLC stations. A given physical station (computer, multiplexer, cluster controller, or frontend processor) can be composed of one or more logical stations. This is accomplished by HDLC mode setting commands. A physical station may provide simultaneous multiple logical station capability on different links. Typical of this is a multiplexer that serves several links. Alternately, a station may house multiple logical stations such as a cluster controller supporting several terminals over a single data link.

Of the three types of logical stations, only a primary station has link control ability. It transmits command frames to, and receives response frames from, the secondary station on the link. There is one secondary station on a point to point link and one or more on a multipoint link. A primary station maintains separate information transmitting/receiving ability with the primary station. It can be employed on a point to point or multipoint line. A combined station has a balanced link control capable of transmitting both command and response frames to and from another combined station and is therefore restricted to a point to point line. The three types of logical data link control stations, used in different logical link configurations, are shown in Fig 1.

In HDLC there are two basic logical data link configurations: unbalanced and balanced. An unbalanced configuration features one primary station and one or more secondary stations connected to a link (ie, point to point or multipoint, 2-way alternate or 2-way simultaneous, switched or nonswitched). The configuration is unbalanced because the primary station is in control of each secondary station and initiates link level error recovery functions. A balanced configuration consists

of two combined stations connected point to point, 2-way alternate or 2-way simultaneous, switched or nonswitched. Both combined stations have equal data transfer and link control ability. The balanced configuration is used in X.25 linked access procedure balanced (LAPB) and X.75 link level.

Two independent point to point unbalanced logical station configurations can be connected in a symmetric manner and multiplexed on a single physical data link. This configuration may be 2-way alternate or 2-way

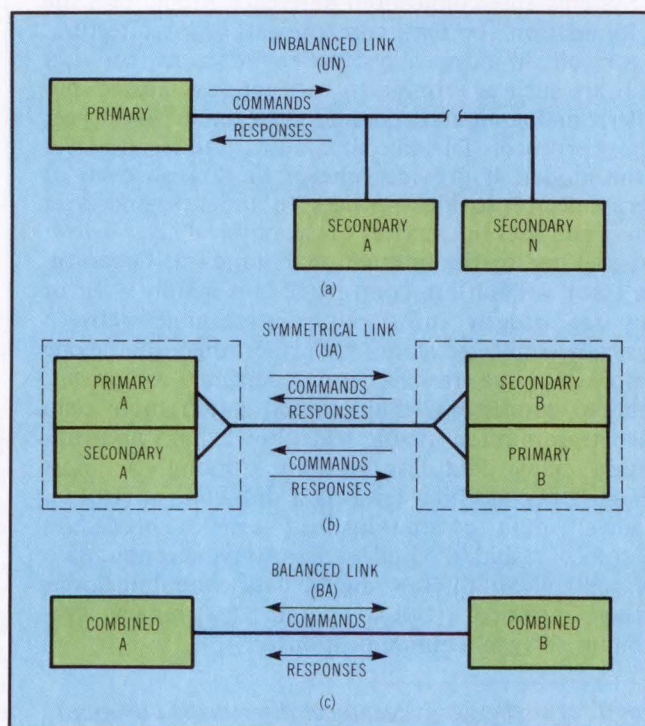


Fig 1 HDLC logic link configurations. Unbalanced system (a) has primary station and one or more secondary stations. Symmetrical configuration (b) features two unbalanced multiplexed links. Balanced system (c) uses two combined stations.

The 15-Minute Data/Voice Network

New Line Miser™ Converts Your Ordinary Phone System Into a Local Area Network

Now you can turn your phone system into a versatile local area network (LAN) for data and voice. It's as easy as plugging in a new telephone. And it takes about that long, too.

Gandalf's new Line Misers enable you to use your existing phone wiring for **simultaneous** voice and data communications. They function as limited distance modems that pass voice transpar-

ently. Simple bandwidth allocation is used to separate the data from the voice. Should your PBX fail, the data will not be affected.

Line Misers provide a fast, cost-effective means of expanding your data terminal network — up to 18,000 feet. Everywhere you have a telephone, you can quickly and easily add a terminal. It's a plug-in job — all you need is a power outlet and a phone jack. No

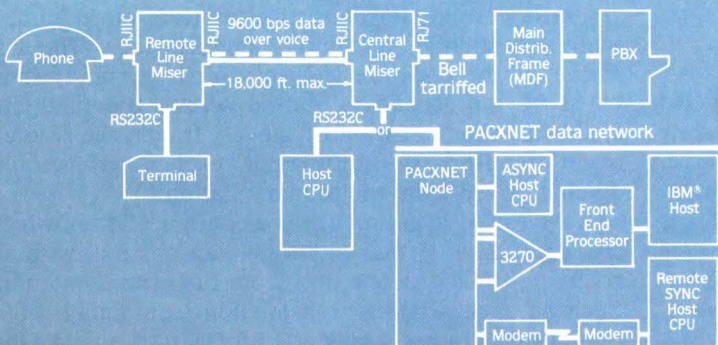
more 4-wire dedicated data lines! Asynchronous full-duplex data rates up to 9600 bps can be handled. An option is available for synchronous operation.

What's more, all Line Misers are FCC registered. Gandalf Line Misers let you create your data-over-voice LAN in record time and at a price you can afford. Call your local Gandalf sales representative for details today.

gandalf™

Fully supported technology
from concept to customer

Rackmount
units available



USA: Gandalf Data, Inc. (312)541-6060
 Canada: Gandalf Data, Ltd. (613)225-0565
 Europe: Gandalf Services, S.A. 22-98-96-35
 U.K. Gandalf Data PADGATE (0925)
 Communications Ltd. 818484

Subsidiaries of Gandalf Technologies Inc.

TABLE 2
Feature Comparison of DLCs

<u>Feature</u>	<u>Character Controlled (Bisync)</u>	<u>Character Count (DDCMP)</u>	<u>Bit Oriented (ADCCP/HDLC)</u>
Transmission format	Sync	Async/sync	Sync
Transmission mode	Half duplex	Half/full duplex	Half/full duplex
Framing: Start end	2 SYNs Terminating characters	2 SYNs Character count	Flag Flag
Frame formats	Numerous	1 (3 types)	1 (3 types)
Link control information	Optional header	Required header	1 or 2 octet control field
Station addressing	Contention (point to point) of polling sequence (multipoint)	Address in header	Single or extended address field
Error checking	Text messages only	Header and info field separately	All frames between flags
Error detection/ generation	VRC/LRC-8 VRC/CRC-16 CRC-16 CRC-12	CRC-16	CRC-CCITT V.41 CRC-32
Requests for retransmission	Stop and wait	Go back n frames	Go back n or Selected Reject
Maximum outstanding frames	1	255	7 or 127
Flow control	Control characters: write acknowledge, no acknowledge	None: data discarded	RNR frame, window mechanism
Character codes	ASCII, EBCDIC, SBT	ASCII for SOH, DLE, ENQ only	Any
Information field length	n x 6 (SBT) n x 8 (ASCII/EBCDIC)	n x 8	Unrestricted
Transparency	Transparent mode escape mechanism	Character count	Zero insertion/deletion
Control characters/ bit patterns	Numerous 1- and 2-character sequences	SYN, SOH DLE, ENQ	Lag, abort, idle

simultaneous, switched or nonswitched. In this configuration there are two primary to secondary station logical channels with primary stations having responsibility for mode setting. Each of the four stations has an information transmitting line, one information receiving line, or both. This configuration is used in X.25 link access procedure (LAP).

Logical states and modes

Communication between any two stations is conducted in one of three logical states: information transfer state (ITS), initialization state, or logically disconnected state. While in the ITS, the secondary/combined station transmits and receives information frames. This state is entered after the logical link is set up in one of three possible modes: normal response mode (NRM), asynchronous response mode (ARM), or asynchronous balanced mode (ABM).

NRM is used in an unbalanced configuration in which the secondary station initiates transmission of frames only as the result of receiving explicit permission to do so from the primary station. Permission is obtained when a frame with the poll bit set is received. After the secondary station receives permission, it initiates a response transmission consisting of one or more frames, while maintaining an active channel state. The last frame of the response transmission is explicitly indicated by the secondary station setting the final bit. Following the indication of the last frame, the secondary station stops transmitting until explicit permission is again received from the primary station.

ARM is used in an unbalanced configuration in which the secondary station initiates transmission without receiving explicit permission from the primary station. Such an asynchronous transmission, containing single or multiple frames, transfers information or indicates



MULTI-VENDOR LOCAL AREA NETWORK COMMUNICATIONS MARCHES TOWARD REALITY.

INTRODUCING ETHERNODE 1000 SERIES. COMPLETE ETHERNET DATA COMMUNICATIONS SYSTEMS LINKING DEC VAX's, PDP-11's AND UNIX BASED COMPUTERS.

High speed, reliable communications between computers with dissimilar system architectures is no longer just fantasy.

It's reality. And it's called ETHER-NODE 1000. From Interlan.

The ETHERNODE 1000 Series consists of all hardware and software required for high-performance, embedded Ethernet communications among DEC VAX, PDP-11 and UNIX based systems. Each offers a complete Ethernet transport service to user-written application programs.

An integral part of each ETHER-NODE is the NS4200 software, consisting of the Internet Transport Protocols (ITP). Because these protocols were modeled after the Xerox Network Systems ITP Specifications, communications can be

achieved between VAX, PDP-11 or UNIX based machines and ITP compatible systems manufactured by Xerox and other vendors.

ETHERNODE 1000 Series features:

- Supports high bandwidth communications.
- Minimizes CPU loading.
- Supports internet communications.
- Provides virtual circuit communication services.
- Provides network management (NETMAN™).

NETMAN, an integral part of ETHERNODE, is a screen-oriented, menu-driven utility that displays a wide variety of performance, configuration and utilization parameters.

Other elements of the ETHER-NODE 1000 Series include Interlan's intelligent UNIBUS, QBUS, or MULTIBUS

Ethernet communications controller, a non-intrusive tapping transceiver unit, and transceiver cabling.

If you are presently using or evaluating Ethernet, and require reliable, program-to-program communications, call or write for details on how Interlan can provide the total data communications solution:

The ETHERNODE 1000 Series.

INTERLAN
WE MAKE NETWORKS WORK.
 3 Liberty Way, Westford, MA 01886
 (617) 692-3900 TELEX 95-1909

See us at Interface '83, Booth No. 1739

EASTERN REGIONAL SALES OFFICE: 10 Kearney Rd., Suite 24, Needham, MA 02194. WESTERN REGIONAL SALES OFFICE: 2091 Business Center Drive, Suite 100, Irvine, CA 92715
 INTERNATIONAL DISTRIBUTORS: ADCOMP Equipment Ltd., Switzerland 741-4111, ASR Arizona, Disc, Japan 781-2422-723, Data Translation Ltd., England 044-86-3412, Prosoftware, S.A., Spain 3-321-32-55, Stemmer Elektronik, West Germany 089-8060-61, Transduction Ltd., Canada 416-625-1907, Yrel, France 956-81-42

status changes in the secondary station (eg, the number of the next expected frame, transition from a ready to a busy condition or vice versa, or occurrence of an exception condition). ABM is used in a balanced configuration in which a combined station initiates transmission without receiving permission from the other combined station. Otherwise, it is identical to ARM.

While in the initialization state, communications are under control of a system defined procedure outside the scope of HDLC. The system defined procedure causes the secondary/combined station to be initialized by receiving parameters from the remote primary/combined station. The logically disconnected state (LDS) prevents the secondary/combined station from receiving or transmitting information. Communications observe the constraints of one of two disconnected modes: normal disconnected mode (NDM) or asynchronous disconnected mode (ADM).

NDM is used in an unbalanced configuration in which the secondary station is logically disconnected from the link and not permitted to initiate or receive information. The secondary station can initiate transmission only as the result of receiving explicit permission to do so from the primary station. After receiving permission, the secondary station initiates a single-frame transmission indicating its status. ADM is used in an unbalanced or balanced configuration in which the secondary/combined station is logically disconnected from the link and not permitted to initiate or receive information. A station in ADM initiates transmission without receiving explicit permission from the primary/combined station and transmits a single frame indicating the station status.

Classes of procedures

There are three classes of HDLC procedures: unbalanced asynchronous response mode (UA), unbalanced normal response mode (UN), and balanced asynchronous response mode (BA). Each class has a basic repertoire of commands and responses, plus functional extensions that can be selected as options. Classes UA and UN can be used on either unbalanced or symmetric configurations, although only UN can be used with a multipoint data link. Class BA is used on a balanced point to point configuration and generally operates with equal or better link efficiency than the UA class (ie, CCITT X.75 link level and X.25 LAPB).

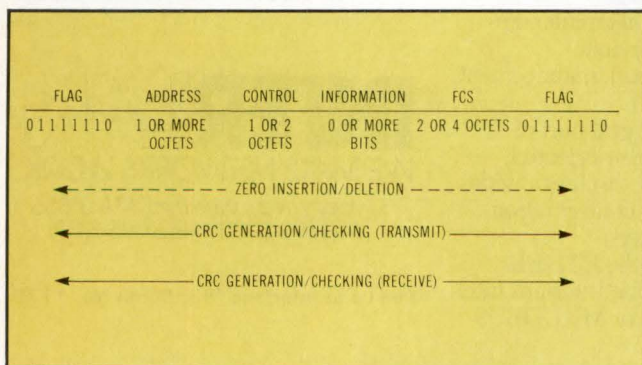


Fig 2 HDLC frame formats. Each frame consists of opening flag octets and sequence of additional address and information octets. All frames must be enclosed by flag octets.

All stations use the same frame format...independent of mode, class of procedure, and link configuration.

Because of the equal link control nature of combined stations, BA makes for more uniform equipment design. A station conforms to a given class of procedures if the receiving station can decode and respond to the control field in the received command/response: a primary station receives all responses in the class of procedures, a secondary station receives all commands, and a combined station receives both.

In HDLC operations all stations use the same basic frame format (see Fig 2). This format is independent of their mode, class of procedure, and link configuration. Each frame contains an opening flag, address field, control field, frame check sequence (FCS) field, a closing flag, and depending upon the frame type, an information field. Information frames and some unnumbered frames contain an information field; supervisory frames do not.

The flag is a fixed 8-bit pattern, also known as an octet. One flag can be shared between contiguous frames such that the ending flag and opening flag are the same. Address fields can be one or more octets and can be recursively extended, by prior agreement, to accommodate addressing of any number of stations. A 1 in the least significant bit (LSB) of an extended address octet terminates the address field; a 0 extends it. The control field consists of one or two octets depending on whether basic or extended mode is specified. Depending on the frame type, the information consists of either user data or specially formatted data. An FCS field is the result of a 16-bit CRC that is generated by the transmitting station and checked at the receiving station, using the CCITT V.41 polynomial: $X^{16} + X^{12} + X^5 + 1$. A 32-bit CRC is being included in the next version of ISO 3309 and is already included in FED-STD-1003A and FIPS 71-1. Address and control fields transmit and receive with the LSB first. FCS transmits and receives with the highest order polynomial coefficient first. The order of bit transmission for the information field is application dependent.

Besides the flag there are two reserved bit patterns: abort = 01111111 and idle = 11111111111111. An abort terminates a frame prematurely. It is sent when the transmitting station has a problem, such as an underrun, or is required to take recovery action based on a frame received during transmission. Flags following an abort keep the link active so transmission can continue. The idle pattern identifies an inactive or idle link state. When a half-duplex station detects the idle pattern, it can reverse the direction of transmission (turn the line around) and then transmit. The idle may be an indication of physical level failure if flags are expected in the quiescent state when the transmitter has nothing to send.

A link is in an active link state when a primary station, secondary station, or combined station is actively transmitting a frame, an abort sequence, or interframe time fill. When the link is in the active state, the transmitting station may continue transmission at its discretion. Interframe time fill is accomplished by

How to dress up your IBM.

Fred Molinari, President

Low cost data acquisition and control for the IBM Personal Computer.™

Data Translation is fashioning a new look in the personal computer market.

Our new single board plug-in brings complete analog and digital I/O capability to your IBM Personal Computer.

The complete DT2801 I/O system fits on just one board. It includes A/D, D/A, digital I/O, and a programmable clock and has direct memory access capabilities.

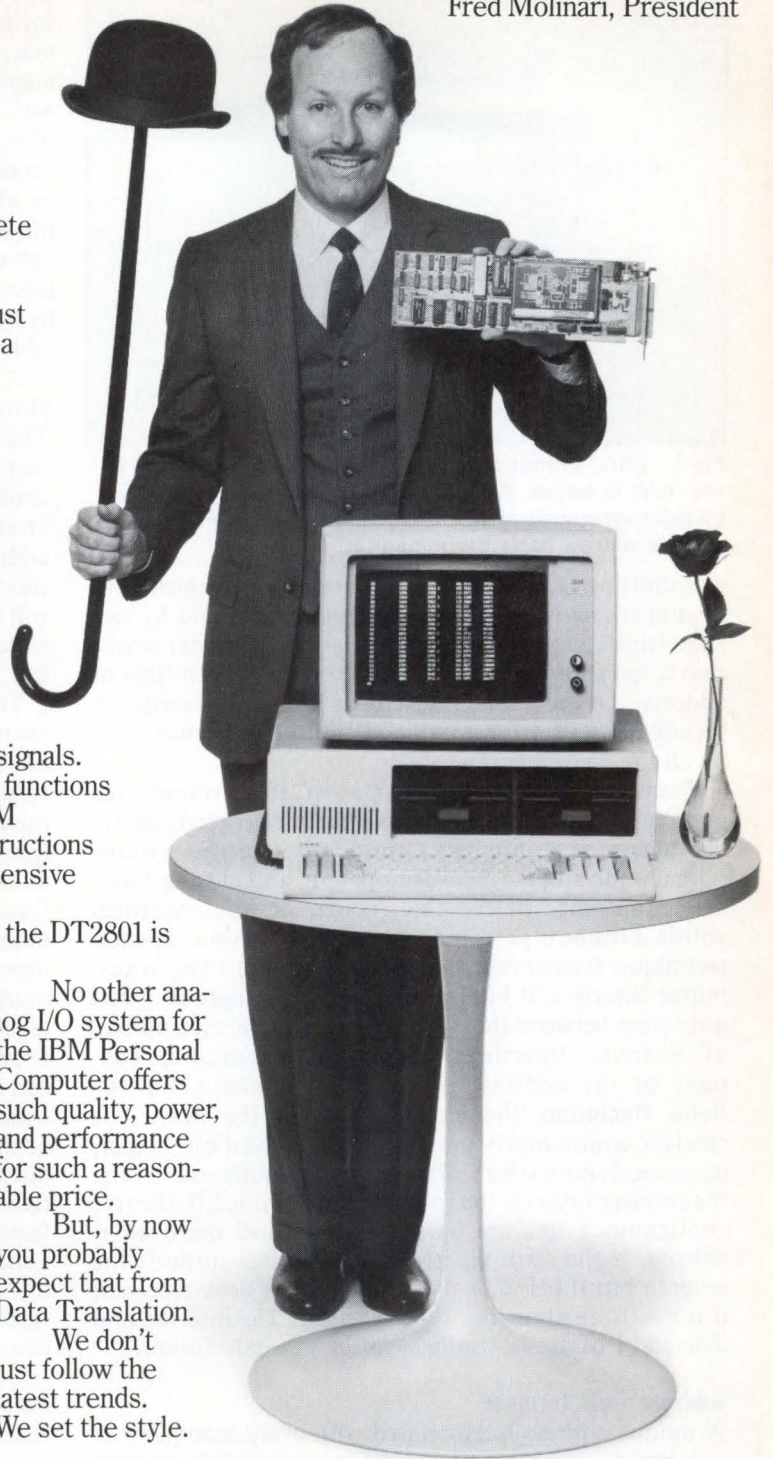
With power and performance to match that of the IBM PC, the DT2801 provides 12-bits of resolution with over 14kHz throughput rates.

And whether your application is in laboratory data acquisition or in industrial process control, you will find the DT2801 highly reliable at a very low cost... under \$1,200.

The DT2801 is easy to use. Just plug it in to one of the IBM Personal Computer's expansion slots. No need for separate housing or cables. An optional terminal panel is available for connecting analog and digital input signals.

And it's easy to program. More than 30 I/O functions are accessed with just 3 commands from the IBM Personal Computer's BASIC. Programming instructions and sample routines are detailed in the comprehensive User Manual.

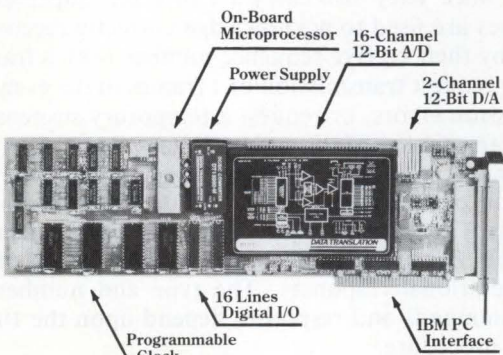
Plus, as with all Data Translation products, the DT2801 is fully backed by our service and support team.



No other analog I/O system for the IBM Personal Computer offers such quality, power, and performance for such a reasonable price.

But, by now you probably expect that from Data Translation.

We don't just follow the latest trends. We set the style.



The DT 2801 from Data Translation is a complete single board data acquisition system for the IBM Personal Computer.

DATA TRANSLATION

World Headquarters: Data Translation, Inc., 100 Locke Dr., Marlboro, MA 01752 (617) 481-3700 Tlx 951-646.

European Headquarters: Data Translation, Ltd., 430 Bath Rd., Slough, Berkshire SL1 6BB England (06286) 3412 Tlx 849-862.

IBM Personal Computer is a registered trademark of IBM.

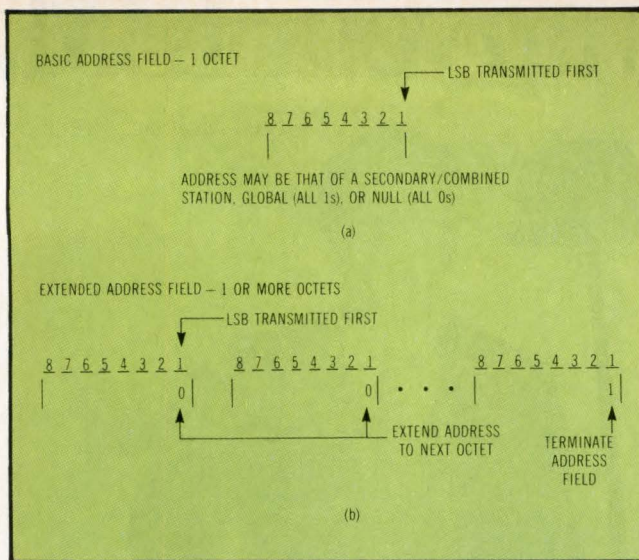


Fig 3 HDLC address field format. Basic address field (a) is one octet in length. Extended address field (b) is established by prior agreement of DLC stations. Zero in LSB position extends address field; 1 terminates it.

transmitting continuous flags between frames. An invalid frame is one that is not properly bound by two flags (thus, an aborted frame is an invalid frame) or one that is too short (ie, shorter than 32 bits between flags or address, control, and FCS fields not completed). A secondary station or combined station will ignore any invalid frame.

Transparency enables a DLC to treat all transmitted and received data, including normally restricted control characters, as a pure data stream. HDLC provides transparency for all data between opening and closing flags. The occurrence of the flag, abort, or idle sequences within a frame is prevented via a 0-bit insertion/deletion technique (sometimes called bit stuffing). The transmitter inserts a 0 bit following five contiguous 1 bits anywhere between the opening flag and the closing flag of the frame. Inserting the 0 bit thus applies to the contents of the address, control, information, and FCS fields (including the last five bits of the FCS). The receiver continuously monitors the received bit stream; upon receiving a 0 bit followed by five contiguous 1 bits, the receiver inspects the following bit. If it is a 0, the five contiguous 1 bits are passed as data and the 0 bit is deleted; if the sixth bit is a 1, the receiver inspects the seventh bit; if it is 0, a flag sequence has been received; if it is a 1, an abort has been received. The inserted and deleted zeros are not subject to the FCS calculation.

Address field formats

A unique address is associated with every secondary or combined station on a link. When a secondary or combined station responds, it will always utilize its own unique address. Additionally, a secondary or combined station may be capable of accepting frames that use a group or global address. An example of this might be a broadcast message to all secondary stations on a multi-point line. The address field in a command frame transmitted by a primary or combined station contains the address of the (remote) secondary or combined station. The address field in a response frame transmitted by a secondary or combined station contains the address of that station.

Two address encoding formats are defined for the address field: basic and extended (see Fig 3). These formats are mutually exclusive for any given secondary station or combined station on a link, and the addressing format must be explicitly specified. In basic address format, the address field contains one address octet, which may be a single secondary/combined station address. In extended address format, the address field is a sequence of octets that make up one address. This field may be a single secondary/combined station address, or a group or global secondary/combined station address. When the first (least significant) bit of an address octet is 0, the subsequent octet is an extension of the address field (except for null address). The address field is terminated by an octet having a 1 in the first bit position. Thus, the address field is recursively extendable.

A single octet address of eight 1 bits is reserved as the global address in both basic and extended addressing. The global address is used if a specific secondary/combined station address is not known (eg, switched connection) or is not relevant to the situation (eg, broadcast transmission). When the first octet of the address field appears as eight 0 bits, the address is considered to be a null (no station) address and the frame will be ignored. The null address frame might be used as an initialization or diagnostic procedure to verify that a DLC station is online.

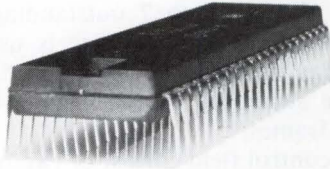
Three types of HDLC frames are information, supervisory, and unnumbered. The frame type is specified by the first two (least significant) bits of the control field. Information (I) frames may contain an arbitrary number of bits of user data in the information field. (Some bit oriented DLCs such as SDLC and X.25 require an integral number of octets in the information field.) I frames are sequentially numbered with a send sequence number $N(S)$ and allow piggybacking of acknowledgments of received frames through a receive sequence number $N(R)$. They also carry a P or F bit. Supervisory (S) frames are used to acknowledge correctly received I frames by their receive sequence number $N(R)$. S frames can also request transmission of I frames in the event of transmission errors, or request a temporary suspension of the transmission of I frames. S frames also carry a P/F bit. Unnumbered (U) frames are used during link initialization or disconnection for additional link control functions. There are no sequence numbers; consequently, 5 modifier bits are available that allow definition of up to 32 additional responses. The type and number of these commands and responses depend upon the HDLC class of procedure.

Parameters associated with frames

Each I frame is sequentially numbered and may have the value 0 through modulus -1, where modulus is the modulo of the sequence numbers. Modulus equals 8 for the basic control field format and 128 for the extended control field format. The sequence numbers cycle through the entire range and recirculate starting from zero. The maximum number of sequentially numbered I frames that a station may have outstanding (ie, unacknowledged) at any given time is called the window size. This number can never exceed one less than the modulus of the sequence numbers. The window size is determined by either the sending or receiving station storage capability; eg, the number of the I frames that

OK OEMS

we're playing your game.



Hazeltine's new Executive 10™ is factory programmed to meet your system application. So, you get a highly customized terminal instead of just an "off the shelf" product. And you get a long list of features:

- precision balanced ball-joint tilt and swivel
- detached keyboard
- split screen
- video attributes
- programmable function keys,

a unique combination of features for terminals in its price class.

Your system deserves a special display. We call it the Executive 10. But we designed it so that you can call it your own.

Hazeltine Corporation
Computer Terminal Equipment
Commack, NY 11725
(516) 462-5598
or call toll free: 800-645-4508

Hazeltine

The new terminal technology.



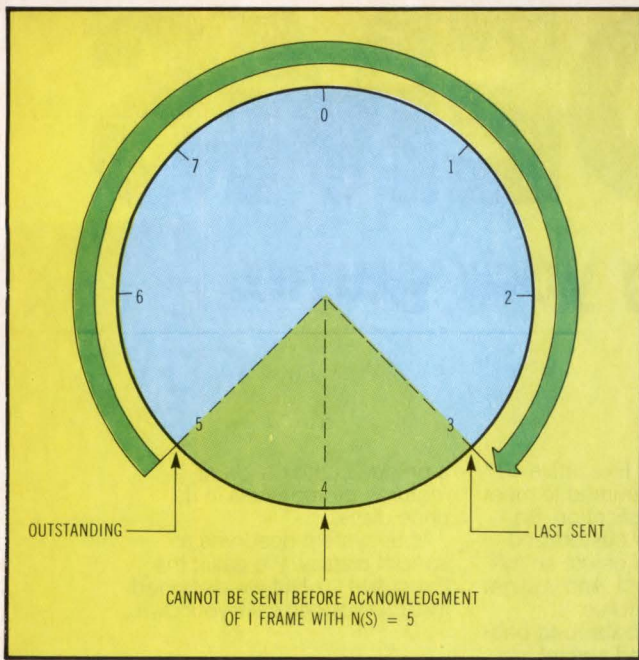


Fig 4 Window operation. Assume basic control field, window size of 7, and I frames with $N(S) = 5, 6, 7, 0, 1, 2, 3$ have been sent without receiving an acknowledgment. At this point the window has closed; one or more I frames must be acknowledged by received $N(R)_6$ before the next I frame can be transmitted.

can be stored for transmission or retransmission (in the event of a transmission error). When I frames are acknowledged, the window is rotated and additional I frames can be sent. Fig 4 illustrates window operation.

Every station in the information transfer state maintains a send variable on the I frames it transmits, and a receive variable on the I frames it correctly receives. Each station capable of transmitting I frames has a send variable S that indicates the sequence number of the next I frame to be transmitted. S takes on the value 0 through modulus 1. S is incremented by 1 with each completed I frame transmission. For example, after the I frame with $N(S) = 6$ is transmitted, $S = 7$. S will not be incremented when an I frame transmission is aborted. Only I frames contain $N(S)$, the sequence number of the transmitted frame. Prior to transmission of an I frame, $N(S)$ is set equal to S . In the previous example, the next I frame to be transmitted would have $N(S) = S = 7$.

Each station capable of receiving I frames will have a receive variable R equal to the expected $N(S)$ contained in the next I frame received. R is incremented by 1 upon receipt of an error-free I frame whose $N(S) = R$. For example, if the modulus is 8 and the I frame with $N(S) = 7$ is correctly received, then $R = 0$. All I frames and S frames contain an $N(R)$, the expected sequence number of the next received I frame. Immediately before transmitting or retransmitting an I or S frame, $N(R)$ is set equal to R . $N(R)$ thus indicates that the station transmitting the $N(R)$ has correctly received all I frames numbered up to and including $N(R) - 1$. In the previous example, $N(R) = R = 0$.

Poll (P) and final (F) bits are used for various operations. They indicate when a secondary station can begin and has finished a response transmission under NRM. The poll/final (P/F) bit can also aid in determining if error recovery is required or in obtaining a response

from the secondary/combined station. The P bit is set to 1 by the primary/combined station in command frames to solicit (poll) a response or sequence of response frames from a secondary station(s) or a combined station.

The F bit is set to 1 by a secondary station to indicate that the response frame was sent in reply to the receipt of a poll command. Additionally, the F bit indicates in NRM that the final frame has been transmitted as the result of a previous poll command. The F bit is set to 1 by a combined station to indicate, in ABM, the response frame sent in reply to the receipt of a poll command.

Control field formats

The basic control fields consist of the single octet shown in Fig 5. For I frames, the $N(S)$ and $N(R)$ modulus is 8, which allows up to 7 outstanding (unacknowledged) frames. The window size is usually fixed at seven, but may be less in low cost HDLC terminals that do not have sufficient buffer storage to hold seven outstanding frames.

Extended control field consist of two octets. On long propagation delay links (eg, satellite or multiple microwave hop transmission) it is desirable for reasons of efficiency to have more than seven outstanding I frames. Extended control field extends the modulus of the sequence numbers for $N(S)$ and $N(R)$ to 128. The window size may be less than 127 in order to conserve buffer space. For example, if I frame length is 1k bytes, a window size of 127 would require a 128k transmit buffer (current frame plus 127 outstanding frames) and a 127k receive buffer. An HDLC terminal probably would not have that much storage and would therefore select a much smaller window size.

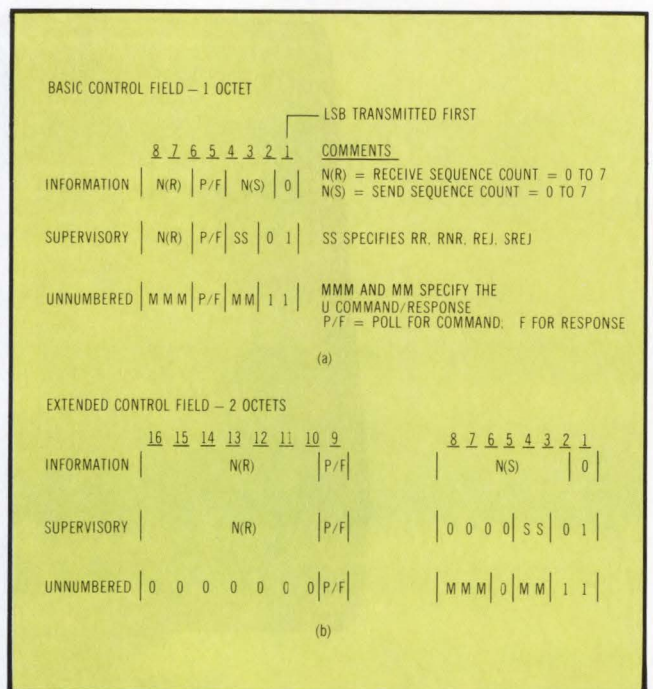
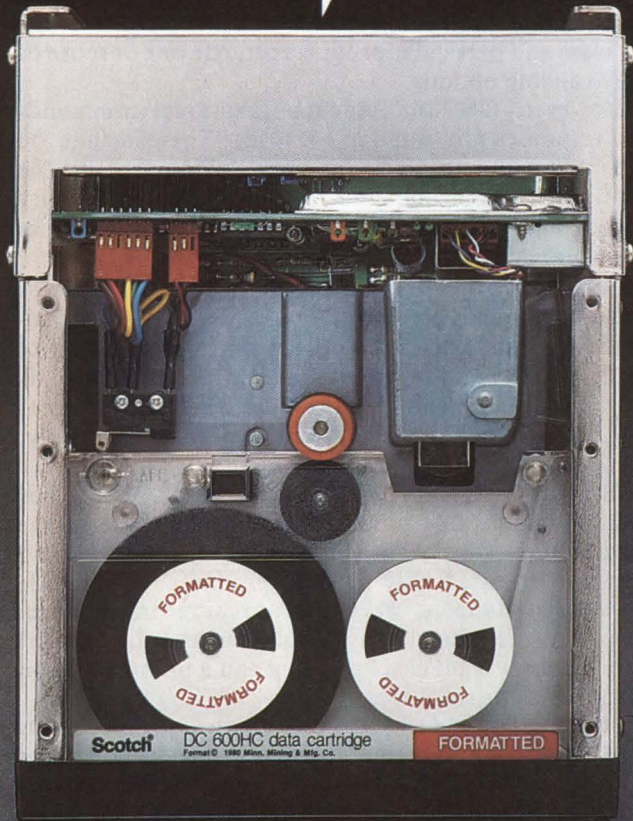
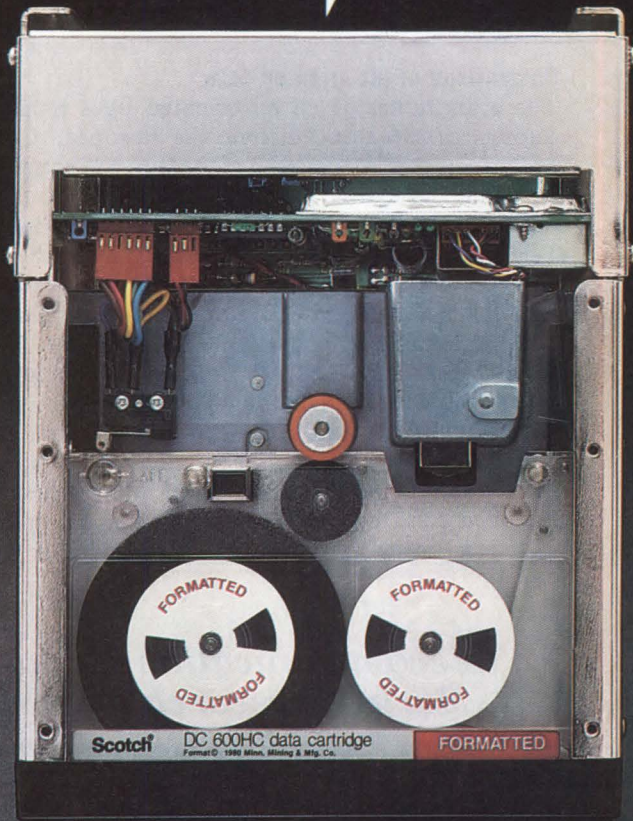


Fig 5 HDLC control field formats. First 2 bits of first octet specify frame type: information, supervisory, or unnumbered. In basic control field (a), up to 7 I frames can be outstanding. In extended control field (b), up to 127 frames can be outstanding. Maximum number of outstanding I frames is determined by user-specified window size.

"I'M A
STREAMER."



"I'M BLOCK
ADDRESSABLE."



The HCD-75. It's both.

Meet the high capacity 1/4" cartridge back-up system with the split personality. The 3M HCD-75 does everything streamers do, and more! Now you don't have to choose between streaming and block addressability for data storage. The HCD-75 lets you design a reliable system that does both. Best of all, it's available right now — thousands of them are already in use — with the following high performance features:

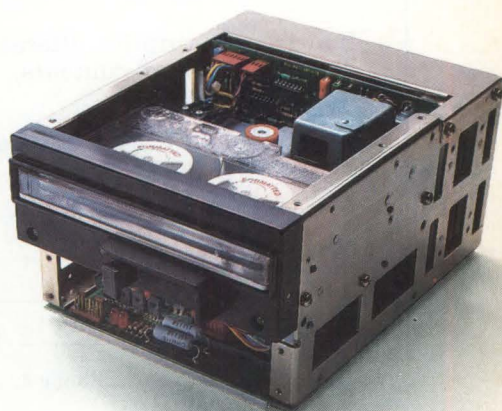
HIGH CAPACITY — a full 67 megabytes of formatted back-up storage — more than any other 1/4" system and most 1/2" systems.

DATA/CARTRIDGE INTERCHANGE — unlike some other systems, every HCD-75 drive

will read every 3M formatted data cartridge, no matter where it originated. A unique combination of stepper head and edge seek features allows unlimited cartridge interchange between drive systems.

COST EFFECTIVE — you get more for less. Total cost per megabyte with the HCD-75 is significantly lower than any other tape system.

Put it all together and you have one of the best friends a computer designer ever had: the 3M HCD-75 back-up system. For more information call (612) 736-9003 or write: Data Recording Products Division/3M, 3M Center 223/5N, St. Paul, MN 55144.



3M hears you...

Circle 123 for sales contact

Circle 124 for Literature

3M

Increased popularity of bit oriented protocols and HDLC interconnect formats is resulting in a proliferation of bit oriented data link controls.

In extended control field format, an HDLC transmitter sets the P/F bit in bit position 9 (ADCCP sets the P/F bits in positions 5 and 9) for unnumbered format commands and responses. A receiver in extended control field format interprets the P/F bit in bit position 9. A receiver in basic control field format cannot receive an extended control field format frame.

Comparison of bit oriented DLCs

The grandfather of all bit oriented DLCs is ISO HDLC. Subsets of ISO HDLC include the European Computer Manufacturers Association (ECMA) HDLC, the American National Standards Institute (ANSI) ADCCP, the International Consultative Committee for Telephone and Telegraph (CCITT) X.25 and X.75 link levels, the Federal Government's 1003A and FIPS PUB 71 and 78 standards, and IBM's SDLC. Federal standards, ISO ADCCP, and ECMA are basically equivalent. As an option proposed for ISO HDLC (3309) and ADCCP, federal standards allow for a 32-bit cyclic redundancy check (CRC). Note that ISO HDLC differs from ADCCP in that HDLC requires the poll/final (P/F) bit to be set in only the second control octet (8-bit group), rather than both octets of an extended control field. The standard also disallows use

of the four nonreserved unnumbered command/response frames in ADCCP, and adds, rather than deletes, a RSET command. ECMA HDLC encompasses ISO HDLC plus the TEST command and response frames. CCITT X.25 LAPB and X.75 link levels are point to point subsets of ISO HDLC. The IEEE 802 logical link control is a bit oriented procedure for local area networks. It has a slightly different frame structure, a 32-bit CRC, and provisions for a mandatory connectionless type of service as well as an optional connection oriented service.

IBM SDLC is roughly equivalent to the ISO HDLC UN class of procedure as specified in DIS 6159 and the NDM as specified in DIS 4335/DAD 1. All IBM SDLC products provide the minimum command/response repertoire of the UN class and particular products provide one or more of the available options.

However, IBM SDLC contains additional commands and responses not found in ISO HDLC. These include the TEST command/response for link testing purposes, the configure (CFGR) command, CFGR response, and binary coded number (BCN) response for SDLC loop mode. ISO HDLC does not include loop operation, which is a major feature of SDLC. In addition, IBM SDLC address and control fields are one octet each (ie, there is no provision for an extended address or extended control field). The SDLC information field is restricted, its length is a multiple of 8 bits, while the HDLC information field length is a system specified parameter. Finally, there is no option for a 32-bit CRC in SDLC.

IBM products implement a subset of SDLC. For example, some IBM products do not allow use of the read (RD) response while the reject (REJ) command and response are used only in SDLC products that provide 2-way simultaneous (TWS) information interchange. Two-way alternate (TWA) products such as the IBM 3274 and 3276 use P/F bit checkpointing and a primary station timer for error recovery.

Increased popularity of bit oriented protocols and HDLC interconnect formats is resulting in a proliferation of bit oriented data link controls. For today's network designer, familiarity with this approach to protocols is becoming increasingly essential. This article is offered to make the minutiae of bit oriented HDLCs slightly less imposing. In Part II, an expanded discussion of the power and flexibility of bit oriented approaches to data communication control will be presented.

Telecommunications Industry Market Research Reports

Frost & Sullivan has recently published analyses and forecasts of the following Telecommunications industry segments:

- 1142 Advanced Business Communications (U.S.)** Price \$1,300
- 1091 Videotex & Teletext (U.S.)** Price \$1,250

For free descriptive literature, including a detailed table of contents, check the above reports of interest.

- Please call me I have questions about these reports***

Name & Title: _____

Company: _____

Address: _____

City: _____ State: _____

Zip: _____ Phone #: _____



Frost & Sullivan 106 Fulton Street
New York, New York 10038 (212) 233-1080

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 719

Average 720

Low 721

NOW TWO FIXED/REMOVABLE 8" DRIVES DOUBLE YOUR STORAGE OPTIONS.

50-MBYTE VERSION ADDED. New LARK Model 9457, with 25 Mbytes of fixed storage plus 25 Mbytes of removable storage per cartridge, joins the 16-Mbyte Model 9455 (8 Mbytes fixed, 8 Mbytes removable).

COMPACT SIZE—STANDARD PACKAGE. Both LARK models are identical in size, shape and mounting; both are the width of an 8" FDD—just right for more space-efficient system.

INTERFACE FLEXIBILITY. Both 16-Mbyte and 50-Mbyte LARKs come with SMD interface or LARK Device Interface (LDI). Plus new optional 9050 Control Module brings you ISI—the Intelligent Standard Interface.

EXCEPTIONAL RELIABILITY. LARKs are totally sealed during operation. No external air is forced across fixed module or cartridge disk surfaces.

QUIET. Low noise level designed for the office—easy on power, too.

ELIMINATES ADJUSTMENT TWO WAYS. Embedded servo information and microprocessor logic mean no need for head alignment; no electric adjustments, even when changing CBs; highly reliable cartridge interchange.

HIGH PERFORMANCE 4 WAYS. (1) low-mass, lightly-loaded flying read/write heads. (2) 9.67 Mhz transfer rate. (3) 42 ms average access time—9455; 35 ms average time—9457. (4) linear voice coil actuators and precision closed-loop servo system.

T H E L A R K™ F A M I L Y

Now LARK doubles your options for built-in back-up with unlimited shelf storage: we've added the 50-Mbyte Model 9457 to the 16-Mbyte Model 9455. Both come with high quality and reliability built in. For more information, call your local Control Data OEM Sales representative or write: OEM Product Sales, HQNO8H, Control Data Corporation, P.O. Box 0, Minneapolis, MN 55440.

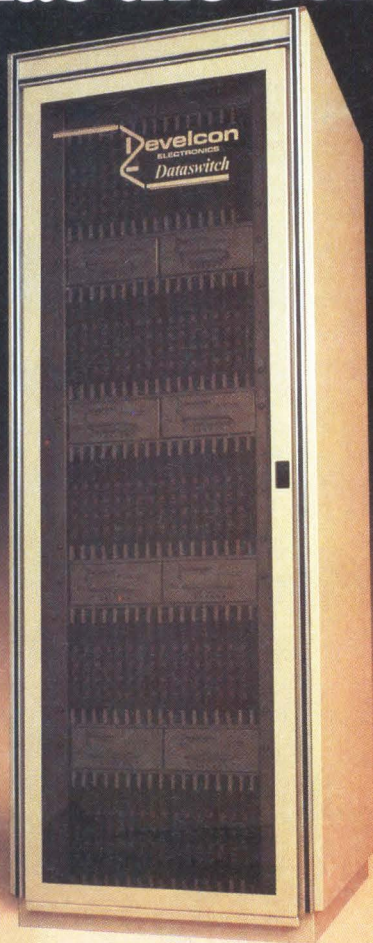


GD CONTROL DATA

*Addressing society's major unmet needs
as profitable business opportunities*

CIRCLE 125

When you have information, Develcon has the connections.



Develcon's unique Dataswitch is an intelligent data switching system which supports any combination of over 2000 devices (or any multiple when run in tandem with other Dataswitches).

Because Dataswitch is a software-based system, continued enhancements and upgrading to meet new market applications is easier, since system software is written in a high level language.

Develcon's Dataswitch provides *universal* access, including port to port, terminal to port and terminal to terminal, and it supports 19.2K baud asynchronous and synchronous operation.

Develcon's Dataswitch. When you have important business to do, isn't it nice to know you have all the right connections?

General Benefits:

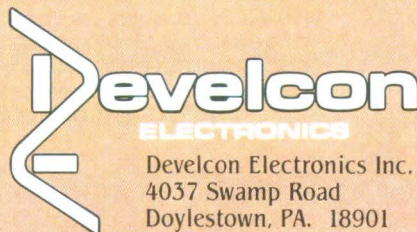
- Support any combination of over 2000 devices.
- Provide universal access allowing port to port, port to terminal, etc.
- Support 19.2K baud asynchronous and synchronous operation.
- Utilization of single autobaud/code recognition sequence.
- Support of ASCII, EBCDIC, BCDIC, selectric correspondence character sets.

- Message forwarding to destination device at connection.
- Port autobaud, log-on message.
- Intelligent port-terminal speed-code matching.
- Prioritized queueing.
- Programmable interval queue position message.
- 8 character password protection.
- Accounting feature.
- Line by line access.
- 510 character banner message.
- Programmable system prompts.
- Programmable status messages.
- Unlimited number of available class restrictions.
- Over 20 statistics generated.
- Party line connection.

Hardware:

- Choice of 3 types of hardware — DB25, barrier strip, amphenol.
- Multiple processors handling unlimited number of requests for service.

- Economical single shelf modularity.
- Economical integral power supply.
- Decentralized, reliable on-board power supply regulation.
- System performance maintained in large networks.
- Automatic dual logic switchover capability.
- Capability to interrogate processors through operator console.
- RS422 level L.D.D.S.
- Multiple line monitoring ability.
- ACU support.
- Interface card test center available.
- Universal synchronous clocking.
- Selectable time-out intervals.
- Triple break disconnect feature.
- Inexpensive tandeming of switches.
- Available T1 carrier format switch link.



Develcon Electronics Inc.
4037 Swamp Road
Doylestown, PA. 18901
Telephone: (215) 348-1900
Telex: 84-6389

Sales offices in most metropolitan areas



BROADBAND NETWORK DESIGN: ISSUES AND ANSWERS

Building a broadband local area network involves more than determining cable runs and calculating gain levels. The crucial work lies in the preliminary planning.

by Edward B. Cooper

It happened only recently: data- and telecommunications managers finally decided on broadband as the preferred medium for their local area networks. Although this decision largely resolves this major issue, many new questions are being broached. Design engineers are eager to define their local area network parameters. Before they do so, however, they first must understand the key local area network design technologies available that offer cost and performance advantages.

Understanding the communications medium known as a local area network (LAN) is vital to its overall success. Without this understanding, network managers often must search for information from many sources that may or may not be design compatible. Curiously, many broadband systems designed over the last 13 years are still in operation, and most have been converted to LANs without redesign or level readjustment. The reason is simple: broadband design parameters developed years ago are still valid because broadband communications design techniques have not changed radically. They have simply been refined and updated to reflect technological advancements.

Edward B. Cooper is manager of the Cable Design and Consulting Group at Sytek, Inc, 1225 Charleston Rd, Mountain View, CA 94043. He is currently working in the area of worldwide cable and LAN engineering. Mr Cooper holds a BSEE from San Jose State University.

For controversy's sake, one might ask about new network schemes such as LocalNet, CableNet, VideoData, or WangNet. In most cases these names merely reflect one particular application of an overall broadband scheme. If properly designed, all such applications, except WangNet, can be supported on the same broadband system. Thus, broadband systems are flexible utilities that can be planned, designed, and installed around the applications they are meant to support.

Broadband design

In developing any advanced communications medium, one must remember the three Rs—redundancy, reliability, and repairability. Reliability and repairability eliminate the need for redundancy, since redundancy alone does not pay for itself unless the system is either poorly installed or poorly designed. Though redundancy and status monitoring can be incorporated into any network, properly designed and certified systems usually have few problems that can be solved by redundant hardware. For example, broadband systems commonly operate for several years without a single radio frequency (rf) component failure. In such cases, redundancy is a needless expense.

The case for redundancy is further weakened, since there are few inexpensive methods of providing diverse cable routes for backup trunk cables. To guarantee that redundant trunks are not damaged by negligence or catastrophe, a backup cable must be run far away from a primary cable. Further, since cable breaks can be repaired easily, and at a much lower cost than designing and constructing redundant trunk systems, cable redundancy is also a waste of money.

TABLE 1
Common Cable Frequency Splits

Split	Frequency Assignment	Bandwidth
Mid-split	Return path 5 to 116 MHz. Forward path 168 to 300/400 MHz.	
Sub-split	Return path 5 to 32 MHz. Forward path 54 to 300/400 MHz.	
High-split	Return path 5 to 174 MHz. Forward path 234 to 300/400 MHz.	
Dual cable	Inbound and outbound paths from 54 to 300/400 MHz.	

As an alternative to cable redundancy, status monitoring can be incorporated into the system along with redundant amplifiers. Any status monitoring system, however, must allow the owner to monitor the entire length of each major cable trunk or branch. Status monitoring systems under development use remodulators assigned with unique addresses. With these systems, polling communication links that poll up to 512 units in 15 s can be incorporated. Through continual polling and responses, fault isolation of any cable branch or amplifier can be accomplished cheaply and quickly.

Another factor that demands attention in network design is topology. When addressing system topology, one must first choose between single- and dual-cable schemes. If single cable is chosen, mid-split, sub-split, or high-split frequencies should be implemented.

In this regard, four major frequency splits, or bandpass spectrums, are available to LAN designers (see Table 1). Three serve single-cable systems, and one is appropriate for dual-cable systems. Some community antenna TV system (CATV) equipment manufacturers display slight variances in the frequency splits since most mid-split filters are designed and installed in existing modules. For this reason, it is wise to consult each broadband vendor to determine the exact frequency split used. This ensures that filter skirts will pass the signals and desired data types.

Dual-cable systems are far more restrictive from design, and cost versus benefit, standpoints. In addition to twice the hardware and labor cost, dual-cable schemes require twice the maintenance. Further, it is not

easy to control dual-cable bandwidth or manage the large numbers of rf carriers present on wide spectrum, dual-cable networks.

Though single-cable networks are also notorious for distortion and have their own data carrier management problems, they do have decades of successful service to their credit. Moreover, the IEEE 802 and TR 40.1 standards committees favor the single-cable scheme for LANs. Although standards for mid-split and high-split schemes are being developed, the TR 40.1 committee has not yet completed its final report to the IEEE. Standards for dual-cable systems are even farther from finalization.

After choosing the network topology, the next step in LAN design is to determine the highest operational frequency. Today, most systems are designed for 300 MHz, although 400-MHz systems are growing in popularity. To determine the optimum LAN design frequency for various services, most engineers use a frequency allocation chart similar to that in Fig 1. This chart graphically depicts the operating frequencies at which system services should function. Using this allocation procedure ensures that no conflicts occur between applications supported by more than one vendor. Designers should also provide for the reasonable expansion of each vendor's bandpass to facilitate growth without having to relocate any existing data or video traffic.

Tap placement is another traditional concern for system planners. Most LANs enjoy growth patterns beyond their planners' highest estimates. Once a LAN system is in operation, users fight for the chance to connect. Consequently, network designers activate portions of the system that were not originally scheduled for operation during the first phase of installation. Thus, it is often best to design for full tap coverage immediately. Such coverage should not only support a drop to each office but a 25% service expansion as well. This expansion factor can be accommodated simply by terminating one of the four rf ports available on each tap. In the case of eight port taps, two ports can be terminated.

How are expansions handled when multiple tap branches are required? First, unlike the restrictive expansion aspects of baseband systems, broadband system expansion does not require disturbing existing users. Second, LAN topology varies from one installation to another based on physical realities such as conduit runs, outlet locations, and the number of offices

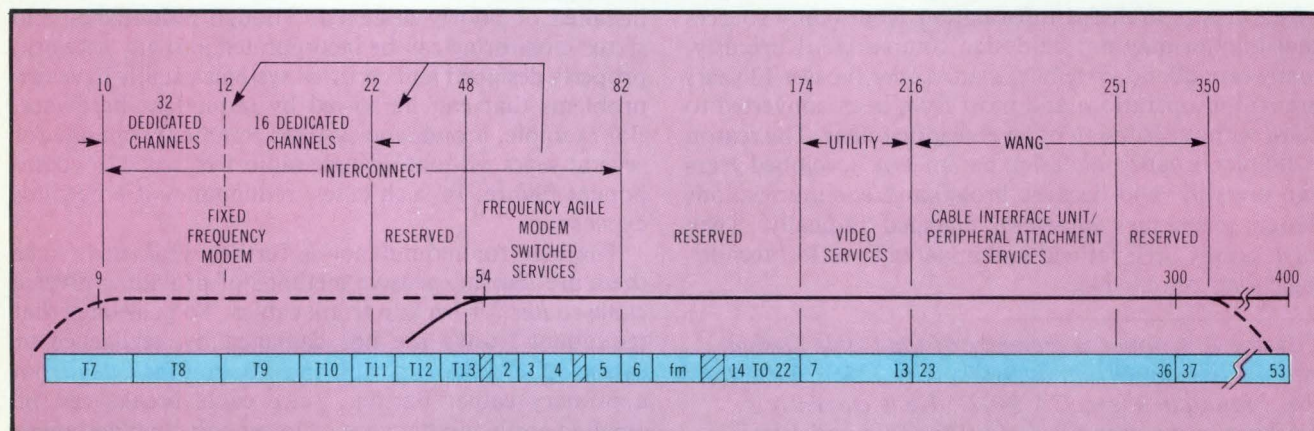
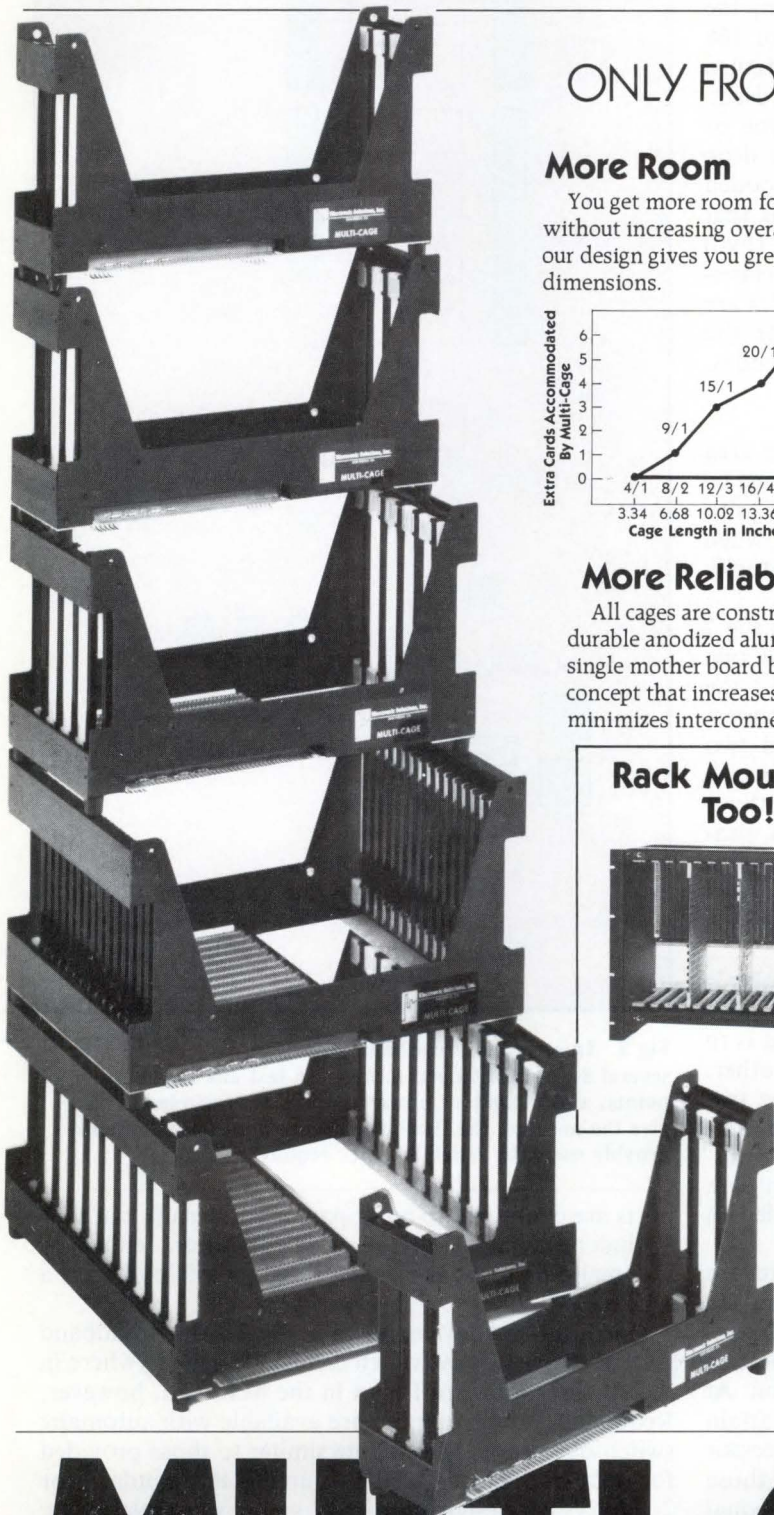


Fig 1 In this typical frequency allocation chart used for broadband LAN planning, WangNet allocations are shown. All frequency values are in megahertz.

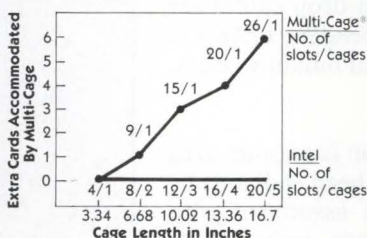
More Room... More Multibus® Cages.



ONLY FROM ELECTRONIC SOLUTIONS!

More Room

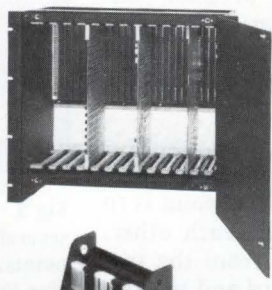
You get more room for extra cards without increasing overall size, because our design gives you greater inside dimensions.



More Reliability

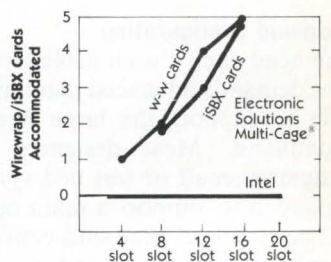
All cages are constructed of sturdy, durable anodized aluminum with a single mother board backplane... a concept that increases reliability and minimizes interconnections.

Rack Mounting Too!



More Models

We have more models than all our competitors combined. Choose a cage with 3, 4, 5, 6, 7, 8, 9, 12, 14, 15, 16, 20, 24 or 26 slots for the right solution to your problem. We have models with either 0.6" or 0.75" card centers and can even accommodate wirewrap cards.



Multi-Cage Wirewrap/ISBX Capacities

All models are electrically and dimensionally interchangeable with Intel's iSBC-80® Cages.

More Warranty

A three year warranty is your assurance of quality.

More Information?

Call our toll free number
(800) 854-7086



Electronic Solutions

5780 Chesapeake Ct., San Diego, CA 92123
(619) 292-0242
Telex II (TWX): 910-335-1169

Note: Multi-Cage is a registered trademark of Electronic Solutions. Multibus, Intel and iSBC-80 are trademarks of Intel.

MULTI-CAGE®

and buildings supported. The best expansion strategy is to place a splitting device with one of its ports terminated at each major branching point. This unused terminated port eliminates the need to disrupt services while new trunk lines or tap branches are added.

The next step in broadband LAN design is to select the cable. Loss and attenuation characteristics play major roles in this decision. In most cases, two frequencies for each path are desirable. For mid-split operation, the losses associated with forward path frequencies of 168 and 300/400 MHz should be calculated. For the return path, 5 and 116 MHz frequency losses should be used.

Loss figures are directly influenced by the type of coaxial cable chosen—whether trunk, feeder, or drop cable. Whatever the choice, a basic rule is to use flooded aluminum cables within conduit or vault systems that interconnect buildings, and polyvinyl chloride (PVC) jacketed cable for internal cable runs. In the drop classification, PVC and teflon multishielded drop cables are advisable. Cable selection is also dependent upon the internal building environment and local building codes.

Head-end configuration

The head end of each cable termination is another area that demands advanced planning. The head end must be able to support the large bandwidth associated with broadband. Most designers miss this point when designing small or test bed systems that are eventually expanded to support a main network.

The standard head-end configuration shown in Fig 2 illustrates its design and support features. The two 8-way combiners connect the mixed services in the system. This sample system has the ability to connect four 8-way combiners in the forward path and two 8-way combiners in the return path. Such an approach allows many services to be introduced later without reconfiguring or readjusting the video or data processing levels. Fig 2 also shows the forward and return paths combined in a system filter. Naturally, the type of filter used will be indicative of the system frequency split chosen.

As with any communications network, a test point is required to connect automated test equipment or spectrum analyzers. One way to provide this test point is to connect two directional couplers opposite each other. The need for this configuration results from the two major types of data/video traffic: forward and reverse. Since nontranslated systems have no frequency translator, they must look to the cable system's return path for status information. Hence, a coupler installed in reverse mode is provided.

Another directional coupler in Fig 2 is terminated on one leg. This coupler provides an expansion point for additional head-end devices or a point for trunk expansion to take place. The amplifier shown provides needed return signal gain and return frequency equalization. At least 75% of all systems require this amplifier to attain proper signal levels at the translator and TV processor inputs. This additional amplifier also ensures that those signals arrive at the data translators' input at equal amplitudes.

Finally, there are system trunks, each able to measure its own return signal independent of other branches. This is accomplished by installing taps in reverse whose

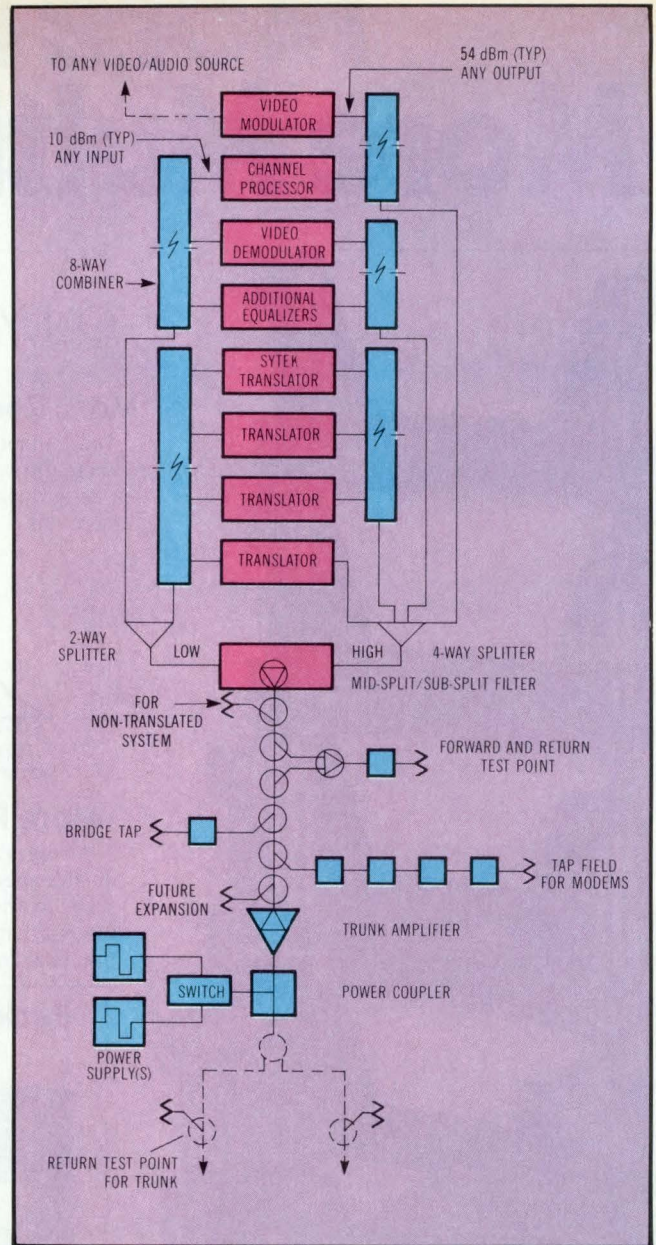
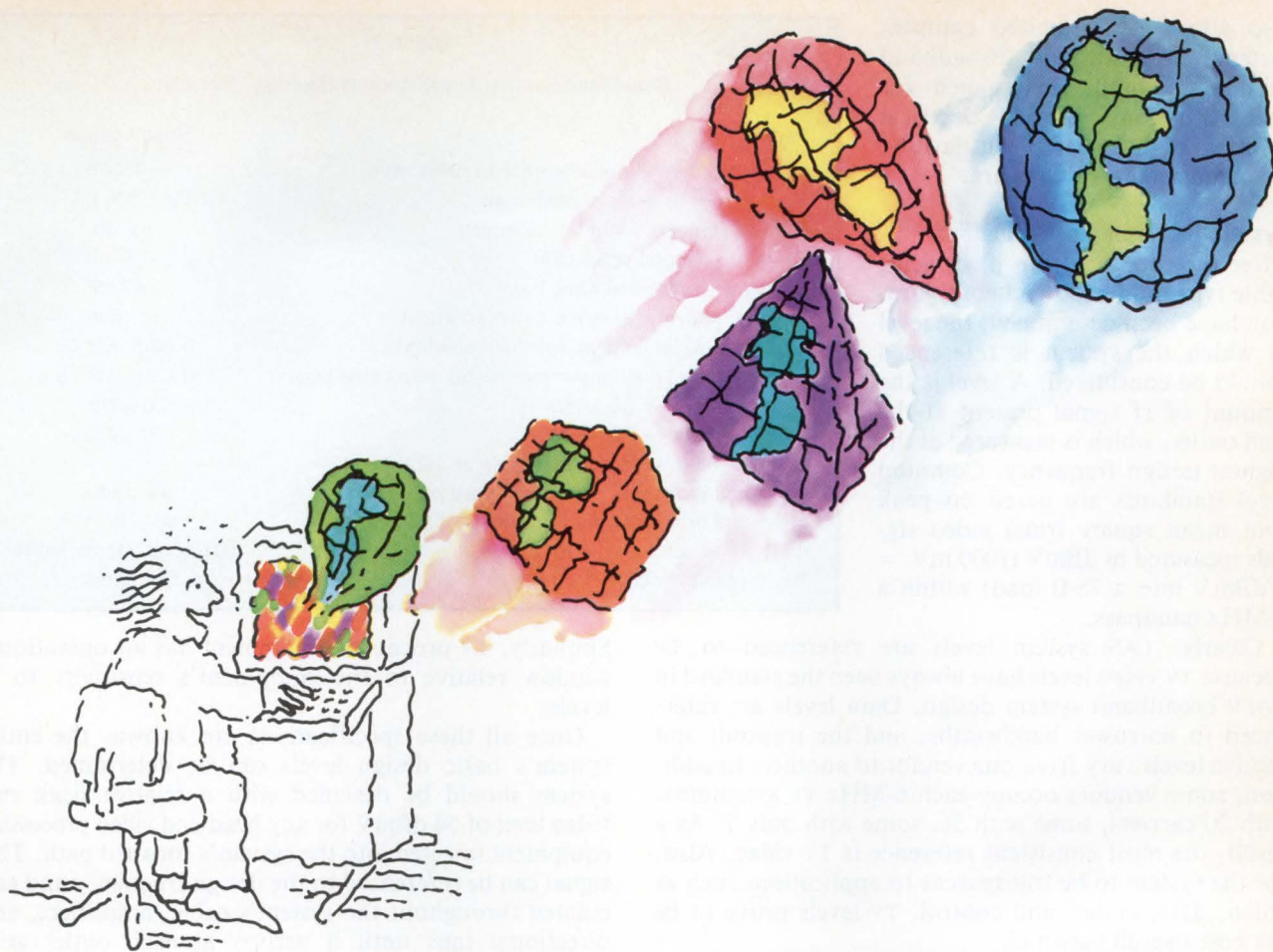


Fig 2 In a typical broadband LAN head-end configuration, several 8-way combiners, terminated test and expansion points, and redundant power supplies are included. These give the network the flexibility needed for expansion and provide users the reliability they require.

ports are connected to a test panel. Each trunk can thus be independently analyzed. Fault isolation, either by automatic or manual means, is also possible in such a scheme.

One head-end device shown in Fig 2 is the broadband system power supply, which can be located anywhere in the system. Most are found in the head end, however. Redundant power supplies are available with automatic switch-over units that operate similar to those provided for data translators. A 60-V source is the standard for 2-way system design since 30-V systems are restrictive. The CATV community has, in fact, converted most of its systems to the 60-V standard.

While head-end configuration appears simple, the broadband LAN's flexibility and splitting characteristics



CHANGE THE WORLD.

Or anything else you can display. Easier and faster than you imagine. Because D-SCAN's new GR-2412 terminal is changing the cost/performance standards for raster scan graphics.

Its world address space, for example, is a full 32K by 32K. Large enough to handle the most ambitious project. Yet easily manageable with dynamic zoom, pan, window, and viewport commands.

Its zoom operation faithfully preserves resolution and detail, instead of simulating it with pixel replication.

And those aren't all the improvements we've made.

Our dual microprocessor architecture draws 25,000 short vectors per second while transferring data at 19.2 kilobaud. And our exclusive anti-aliasing



GR-2412 with standard 20-in. x 20-in. digitizing tablet. GR-2212 (monochrome) also available.

hardware removes jaggies without affecting drawing speed.

About the only thing we didn't change is our long list of standard features. Like our high resolution 1024x780 display. Local transformations. Up to 768K bytes of local segment memory. 4014 emulation mode. And the 10 years of Daini Seikosha (Seiko) craftsmanship in every D-SCAN product.

If you're ready to make some changes, contact us at Seiko Instruments U.S.A., Inc., 2620 Augustine Drive, Santa Clara, California 95051. Telephone (408) 727-0768.

We'll give you a terminal that can take on the world.

D-SCAN

Seiko Instruments U.S.A., Inc.

also allow for unlimited complex system configurations. Broadband networks should be designed for each situation, just as electrical utilities and heating/ventilation/air conditioning systems are.

System levels and specifications

After the topology, tap placement, cable type, and head-end configuration have been determined, the level at which the system is referenced should be considered. A level is the amount of rf signal present at the wall outlet, which is measured at the highest design frequency. Common level standards are based on peak root mean square (rms) video signals measured in dBmV (1000 mV = 0 dBmV into a 75-Ω load) within a 6-MHz bandpass.

Clearly, LAN system levels are referenced to TV because TV video levels have always been the standard in CATV broadband system design. Data levels are referenced to narrower bandwidths, and the transmit and receive levels vary from one vendor to another. In addition, some vendors occupy each 6-MHz TV assignment with 20 carriers, some with 56, some with only 7. As a result, the most consistent reference is TV video. Also, for the system to be transparent to applications such as video, data, audio, and control, TV levels prove to be the best overall yardstick.

Broadband systems can provide color or monochrome TV signals to any outlet. In addition, remote TV signals can originate from any system outlet. Using a variety of transmission techniques and access schemes, non-TV signals are also compatible with the broadband system. Signals such as data, control, and audio must conform to TV distribution standards, however. As a result, data carrier levels are based on the standard deration formula of $10 \log n$, where n is equal to the number of carriers within a 6-MHz assignment.

To determine the correct signal amplitude of each data carrier level, the resulting number is subtracted from the peak rms video levels. For example, Sytek Inc's LocalNet 20 has twenty 300-KHz wide carriers within a 6-MHz TV assignment. If the formula $10 \log 20$ is applied, the result is 13.01 dBmV. These carriers are 13 dB below the equivalent system peak rms video levels. This relationship is also apparent when the deration formula is applied to specifications given in the product literature. The published rf output specification indicates a nominal output level of 42 dBmV and a nominal receive level of -6 dBmV. By adding the 13-dB deration figure ($10 \log 20 = 13$) to both parameters, the equivalent nominal peak rms video level of the system can be determined. Adding 13 dB to 42 dBmV yields a 54-dBmV output level. The receive level is calculated in the same manner. A -6-dBmV level plus 13 dB yields a 7-dBmV equivalent video level.

Based on these known derations, the desired signal levels for transparent operations can be found. Every vendor's data modem has a nominal operation window relative to receiver sensitivity and transmitter output.

TABLE 2
Broadband System Specifications (Mid-split Sample)

Parameter	Specification
Carrier to thermal noise (carrier to noise ratio)	≥ 43 dB
Peak carrier to peak to peak hum	≤ 1.5% dB
Gain vs frequency (6-MHz Channel)	± 1 dB
Carrier to second-order beat	> 60 dB
Carrier to composite triple beat	≥ 52 dB
Maximum level difference between outlets	± 1.5dB
Minimum outlet level at specified bandpass	6 dBm ± 3 dB
Minimum tap level (assuming a 2-dB drop cable loss)	8 dBm ± 3 dB
Radiation (below 50 MHz)	20 μV/m
(above 50 MHz)	50 μV/m
(as measured with a tuned dipole at 10')	
Head-end processor output (forward path)	54 dBmV
Head-end processor input (return path)	10 dBmV
Data translator input/output	Based on vendor limits
Return path injection output level	54 dBmV

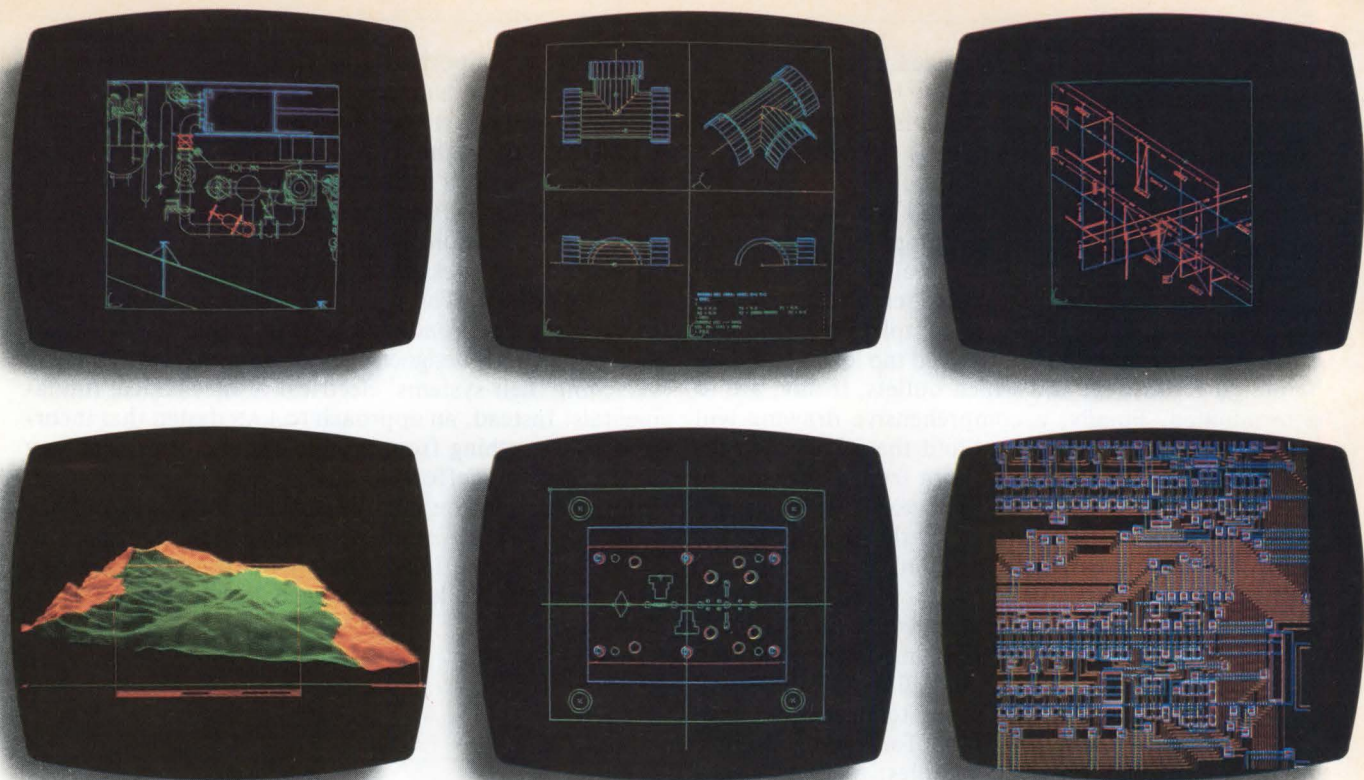
Similarly, TV processing equipment has an operational window relative to the equipment's sensitivity to rf levels.

Once all these specifications are known, the entire system's basic design levels can be determined. The system should be designed with a relative peak rms video level of 54 dBmV for any head-end video processing equipment injected into the system's forward path. This signal can be referenced to the design frequency and calculated throughout the system's cable, amplifiers, and directional taps until it arrives at each outlet at a 7-dBmV level.

When that level has been established, data levels are easy to determine because the deration formula can be applied to calculate the actual data carrier level for each vendor. For instance, if LocalNet levels are used, then the relative nominal receive signal level will be -6 dBmV. If Amdax Corp's point to point modems are used, on the other hand, then fifty-six 96-kHz wide carriers within a 6-MHz assignment are found. Using the deration formula ($10 \log 56 = 18$), data levels are 18 dB below the system video level. In our example LAN, -11 dBmV falls into the center of their receiver operational window. When designs are based on video requirements and the deration formula, any system can be configured to support any vendor's LAN equipment as long as their frequency assignments do not conflict.

A summary of the standards used to design a mid-split transparent LAN system appears in Table 2. Though existing systems prove that these specifications work, each manufacturer should be consulted to ensure that the levels are consistent with proper modem operation. Based on the parameters of Table 2, the tap values, the number and value of all passive splitters and directional couplers, and the number and type of connectors required for any LAN can be determined.

Once a broadband system's design parameters are known, this information must be translated into a set of drawings. This design phase is crucial since the system's drawings are the most important tools used to develop the LAN. Without comprehensive and accurate drawings, troubleshooting would be extremely difficult as would be network expansion.



IT'S TIME TO TAKE YOUR PLOT 10 IDEAS OUT OF STORAGE.

Give your imagination the benefit of the latest graphics technology, with a D-SCAN dual-microprocessor GR-2412 raster terminal.

For example, the GR-2412's remarkably fast, remarkably accurate 4014 emulation makes it a snap to add color and selective erase to existing PLOT 10 routines.

And its high resolution 1024 x 780 raster display, with exclusive anti-aliasing hardware, means image quality that rivals a storage tube.

If your ideas grow too big for PLOT 10 to handle, you can always take advantage of the GR-2412's unsurpassed collection of standard graphics features. Like local transformations. Closed figure drawing. Up to 768K bytes of local segment memory. And a software utility package that

can replace lines of PLOT 10 code with a single FORTRAN statement.

Something else to consider while you're thinking about the future.

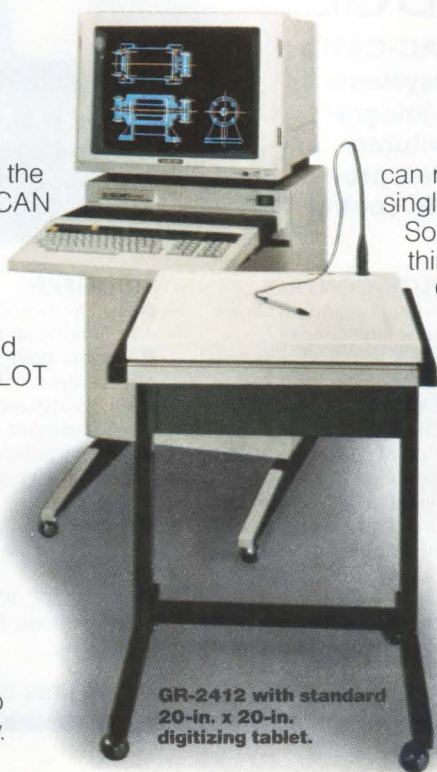
Our past.

D-SCAN products have been field proven for over a decade. And every one is crafted by Daini Seikosha Co., Ltd. (Seiko), known worldwide for its precision watches, robots, and computer peripherals.

For immediate information on the GR-2412, contact Seiko Instruments U.S.A., Inc., 2620 Augustine Drive, Santa Clara, California 95051.

Telephone (408) 727-0768.

Because ideas in storage don't get any better. Just older.



GR-2412 with standard 20-in. x 20-in. digitizing tablet.

D-SCAN
Seiko Instruments U.S.A., Inc.

Drawing standards, symbols, and head ends

Several items should appear on every broadband system drawing. One is a list of symbols used and their associated part numbers. Another is the system design frequency (both forward and return), as well as the type of cables selected and their associated loss. It is also wise to include trunk and distribution amplifier levels, both forward and return, as well as the alignment method. (The Flat Output method is considered standard for broadband LAN alignments.) A complete drawing will also indicate the minimum outlet and tap levels based on the design frequency, and which outlets, if any, are to be terminated. Finally, a comprehensive drawing will provide detail of the head end and the calculated outputs of the TV processors and data translators, noting any vendor limitations in power levels. It is also good practice to note any items that block the ac power at the head end or at any amplifier location.

Aside from the network's obvious electrical aspects, several of its physical aspects must also be documented. Drawings should note extra cables pulled in conduits for redundancy or spares and should illustrate the trunk routings and their locations in the system. Also, the suggested pad values and equalizers for each amplifier should be noted, as should manholes, raceways, conduits, and trays. Documenting each cable's length and associated loss for the forward and return directions is especially important. On the cover drawing, the designer's name, telephone number, and address should be included, and a bill of material should be provided as part of the documentation.

Finally, an important and often overlooked issue in designing a LAN concerns the symbols used in system drawings to represent components. The need for written consistency throughout the entire process of designing and documenting a network cannot be overemphasized. Documentation is fundamental to the long-term success of a communications network.

Another factor essential to the broadband LAN's success is planning. The design, construction, and implementation of a broadband LAN is a multifaceted task. As a result, LAN designers cannot be content with merely sketching their systems' electrical or mechanical fundamentals. Instead, an approach to LAN design that incorporates everything from a judicious choice of topology to an exacting effort at documentation is required. Remember that the goal of any network is to provide users with reliable, uninterrupted service. A little extra time spent in the initial design phases can ultimately save time, for both the user and the designer, farther down the line.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

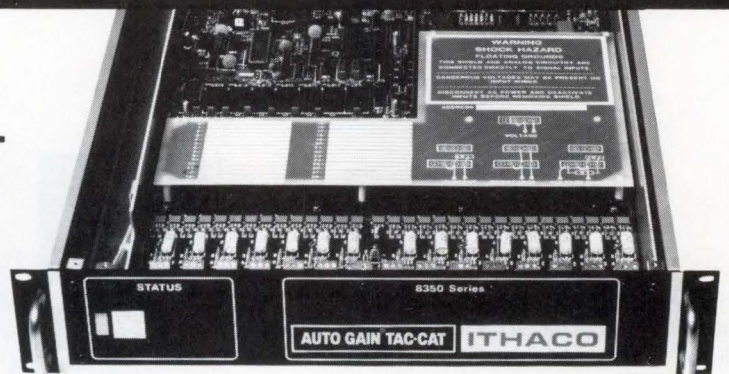
High 722

Average 723

Low 724

ON THE PROWL FOR KNOWLEDGE.

Ithaco presents AUTO GAIN® TAC-CAT; a family of flexible, intelligent, subsystems specifically designed for system integrators, original equipment manufacturers and engineers building distributed process systems to acquire, compute/control and transfer data.



ACQUIRE

- Intermix 30 inputs: TC, MA, μ VDC, HVAC, Resistance
- Expand to 210 analog & 64 digital I/O (optional)
- Auto-zero & slope, line synchronous integrating ADC
- Built-in filters and cold junction compensation
- AUTO-GAIN® and user programmable gain per channel
- >180dB CMRR, >80dB NMRR, and 250V isolation
- Definable scan sequence and group assignments

COMPUTE/CONTROL

- Continuous scanning allows real-time limit checking
- 3 to 6 full digit programmable resolution and integration
- Full Z80 single board computer with bus extension
- Multi-point piecewise-linear scaling functions
- Non-volatile RAM for set-up, acquired and calibration data
- Digital outputs for external DACs and on/off control (optional)
- Linearization tables, mx+b and post scaling transformations

TRANSFER

- Host and local operator RS232 communications ports
- Remote-computer, full-duplex, message oriented protocol
- Highly stylized serial link management, easy interfacing
- Asynchronous event reporting, error checking and hand-shaking
- Names identify transducers/sensors, scale functions and groups
- High speed differential current-loop, 6000 ft. daisy chaining

- Additional GPIB interface per IEEE 488 (optional)
- Catch a CAT of your own. Call, write or telex Ithaco today for complete information. ITHACO, Inc., 735 West Clinton Street, P.O. Box 6437, Ithaca, New York 14850-6437, (607) 272-7640 Telex 510-255-9307

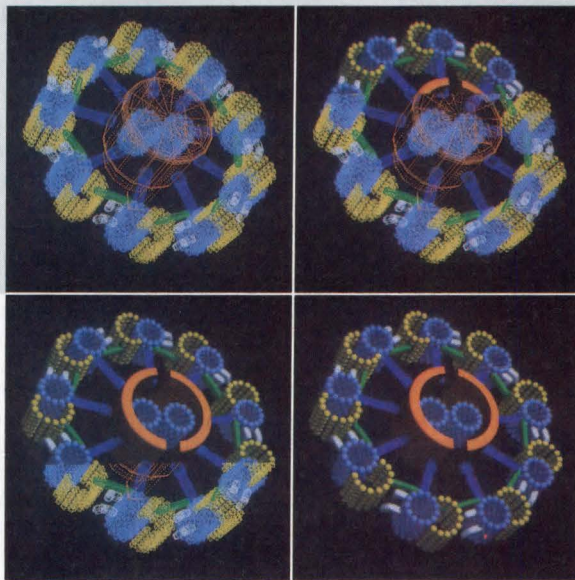
ITHACO

139C-CD-383

A MEASURABLE DIFFERENCE.

Image manipulations in seconds, not hours.

With Mini-MAP... The Array Processor For The Graphics OEM



For tough image processing problems like pixel rotation, picture regeneration, or hidden line removal from wire frame models, Mini-MAP gets results in seconds, not hours. Attach a Mini-MAP, model MM-111, to a PDP-11 UNIBUS and you have an interactive number cruncher that is ideal for image processing, CAD/CAM, solid modeling, simulation, and animation.

Shared memory simplifies programming and provides the unprecedented throughput necessary for truly interactive image processing of complex algorithms. 32-bit floating point arithmetic, along with 7 MFLOPS of number crunching power, adapts to any input data format with ease.



A scientific sub-routine library of FORTRAN callable routines including an expanding selection of image processing algorithms

Courtesy of Al Barr, Raster Technologies, Inc.

is available for Mini-MAP. For optimum performance, high-level FORTRAN control languages are provided for both the host and Mini-MAP.

Memory is expandable up to 16 MBytes. Configurations include a four-board set with DEC-type backplane or fully packaged systems.

System integrators are finding Mini-MAP is the most cost-effective number crunching solution for image manipulation. Write for information or call on our applications engineers for assistance.

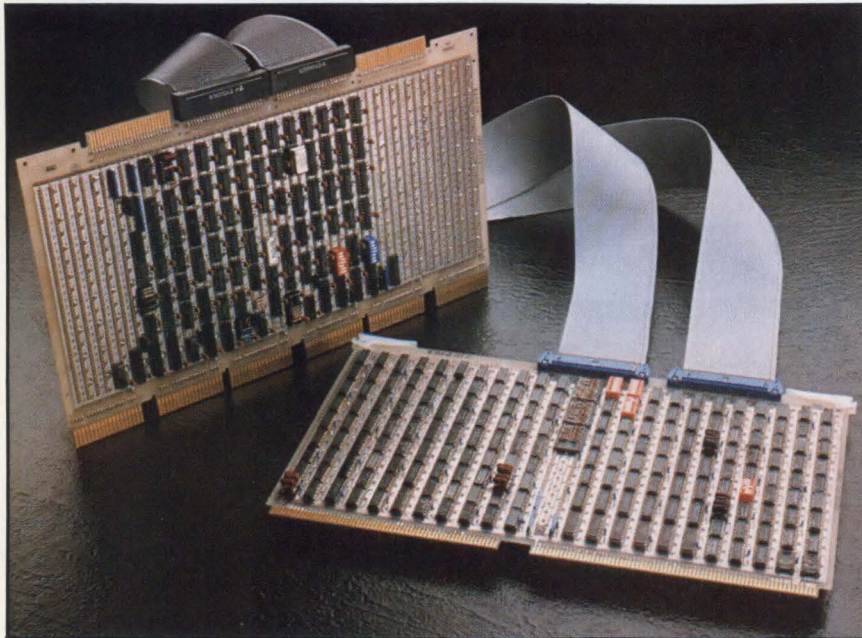
- 32-bit floating point precision
- Shared memory UNIBUS interface
- 150 FORTRAN callable arithmetic routines
- Up to 16 MBytes of memory
- 1024 x 1024 2-D real FFT in 8.8 seconds
- 1280 x 1024 4-color image rotation (Raster Scan Storage Format) in 27.5 seconds.

DEC, PDP-11, and UNIBUS are trademarks of Digital Equipment Corp. Mini-MAP and MM-111 are trademarks of CSPI

CSPI
THE ARRAY PROCESSORS

40 Linnell Circle, Billerica, Massachusetts 01821 • 617/272-6020 • TWX: 710-347-0176

Controller interfaces Unibus, VERSAbus, and Ethernet products



By acting as a bridge between Digital Equipment Corp's Unibus products and Motorola's new generation VERSAbus, the UNI/VERS gateway from Associated Computer Consultants allows high performance VERSAbus products to front end the slower VAX and PDP processors. The bridge is also a vehicle for subsequent high speed interfaces that will link Unibus processors to Ethernet, ARPANET, X.25 packet-switched networks, IBM mainframes, and various other data communication systems.

To be previewed at "Interface '83" this month, UNI/VERS essentially acts as a high speed, transparent DMA controller between a Unibus processor and processors on the VERSAbus. VERSAbus architecture enhances overall system capabilities since it is 10 times faster than the Unibus, connects with multiple processors, and has a 16M-byte address space (expandable by 8 more address bits) compared to the 256k bytes allotted on the Unibus.

UNI/VERS furnishes cost-effective intelligent front ends for VAX and PDP. To prevent DEC processors from being saturated, users can offload such specific functions as protocol processing to the 68000 based VERSAbus CPUs, which have higher speed and faster throughput. In addition, while both Unibus and VERSAbus data paths are 16 bits wide,

VERSAbus data can be extended to 32 bits for increased addressing capability.

Conversely, VERSAbus applications development is no longer restricted by limited hardware, operating systems, and applications programs when UNI/VERS is used. Any VERSAbus system under development can be connected to the entire pool of DEC compatible products and software. The UNI/VERS bridge also operates as a fast DMA controller in all four inter- and intrabus permutations—VERSAbus to Unibus, Unibus to VERSAbus, VERSAbus to VERSAbus, and Unibus to Unibus.

Memory mapped DMA

All 256k Unibus memory locations can be memory mapped onto the VERSAbus in a transparent mode via UNI/VERS, without any system CPU setting up physical address pointers. The VERSAbus processor views the Unibus memory as part of its own, an advantage when examining control structures on either side of the gate. In transparent mode, the UNI/VERS detects a Unibus address, requests a Unibus cycle, obtains the required data, and presents it on the VERSAbus.

Although Unibus is a single-processor environment, with only one CPU fielding interrupts and having only one bus arbitrator, this is not the case with the

VERSAbus. Its enhanced architecture allows one or more 68000 CPU to gain access to the bus. By using UNI/VERS, a normal mode DMA data transfer can be set up between any two nodes within the four inter- or intrabus permutations. The board on the VERSAbus side (with more intelligence than the board on the Unibus side) features a DMA controller with source and destination registers, transfer count register, data register, and control and status register. When transferring data blocks, the address and count registers are initialized by the active CPU, which then sets a GO bit and begins the DMA transfer process.

As the block transfer progresses, address sequences are monitored and decoded. If the current address lies within the Unibus address range, a request for a Unibus cycle passes to the board on the Unibus side. There, the Unibus protocol is monitored as soon as the Unibus grant has been issued. Upon completion of data transfers, the DMA controller interrupts the requesting 68000 to determine the gateway's status.

If potential transfer error conditions are detected, the data transfer is terminated and indicated by status bits. Each end of transfer interrupt will vector control back to the CPU that initiated the DMA transfer. An interrupt handler for that CPU assumes control and determines which subsequent activity to schedule.

Intrabus DMA

On the VERSAbus side of the gateway, multiprocessor, multitasking applications are facilitated as well. The gateway's design is based on fast, discrete logic implementations of registers, counters, and asynchronous control elements, thereby allowing it to direct very high speed memory to memory transfers along either bus (see Diagram). These transfers take place at speeds much faster than a programmed operation.

If numerous VERSAbus processors are simultaneously and independently working on different tasks, and common operating resources such as buffers, tables, and I/O controllers need to be reallocated, the UNI/VERS' DMA controller can shift 16 bits from one memory port to another at speeds up to

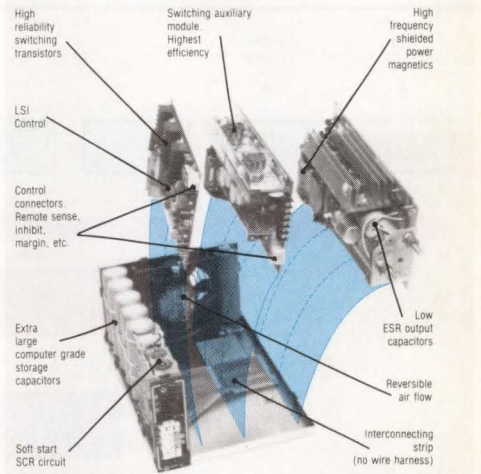
(continued on page 220)

750 to 1500 Watt Switchers

More than just a Power Supply ... a power system.

This is the only multiple output power supply that has the reliability and low cost of modular construction and the versatility of 12 standard options. We call it a "Power System" because it saves system design time and hardware costs. Options such as AC power fail detection, out-of-tolerance monitoring and margin checking etc. are available. Twelve submodules and twelve standard options provide over 7000 specific models.

RE Series



Feature	Function	Benefit
Industry standard 5" x 8" profile	Provide standardized packaging and good power density	Can replace most competitive models
750W/800W/1000W multi output models	Serves the entire computer/systems market	Upgrades possible as systems expand
High efficiency auxiliary regulators	Reduce dissipation for cooler operation	Greater reliability, lower power consumption
40 mSec holdover storage	Provides maximum time for orderly system shutdown during power failure	Provides excellent performance during normal operation; increases power fail warning time
Industry's widest selection of standard catalog options	Too numerous to mention; call or write for details	Maximum user flexibility; lower overall cost; easy system integration
Totally unique, high efficiency 360W auxiliary module	Provides highest regulated output currents available in 5" x 8" package	Increased flexibility, high density, excellent price/performance ratios

Additional Features and Benefits • Modular construction that eliminates wire harnessing • User selectable input voltage range (115/208/230VAC) • Extremely wide input range (90-132VAC/180-264VAC) • Designed to meet UL/CSA/VDE0804 • Shielded, vacuum impregnated magnetics • Common mode noise filtering • Electronic soft start • Bidirectional forced air cooling • Extended operating temperature range • Protected against over-temperature • Remote sense, all channels • Inhibit, all channels • Parallel operation, all channels • Series operation on auxiliary channels • All semiconductors tested per MIL883B • Computerized in process and final testing including test data • Comprehensive manual • 48 hour, 50°C dynamic burn-in • And much more . . .

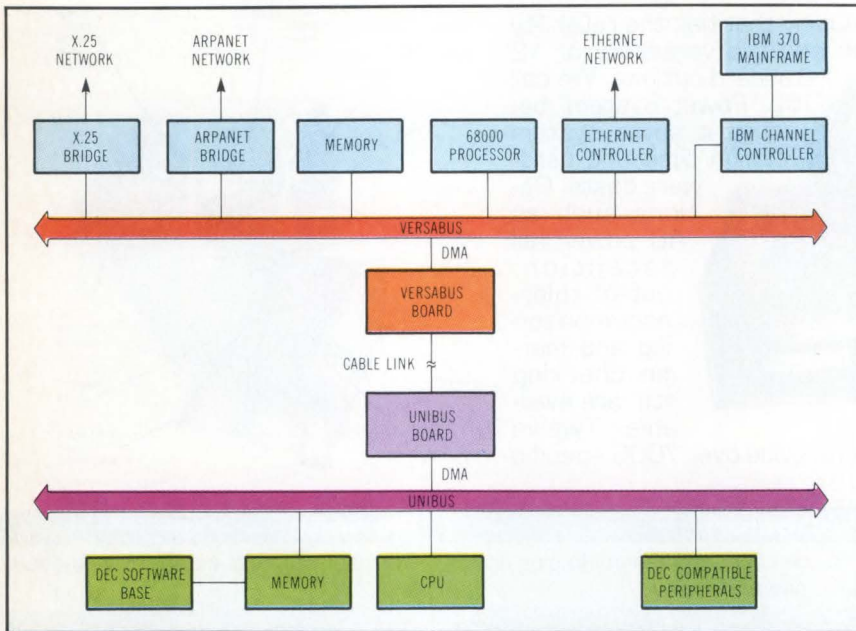
OUT-PUT VOLT	SINGLE OUTPUT				OUT-PUT VOLT	DUAL OUTPUT				750W/1000W TRIPLE & QUAD				800W TRIPLE & QUAD				
	MODEL/OUTPUT CURRENT					MODEL/OUTPUT CURRENT				MODEL/OUTPUT CURRENT				MODEL/OUTPUT CURRENT				
	RE 751	RE 801	RE 101	RE 151		RE 752	RE 802	RE 102	OUT-PUT VOLT	RE 753	RE 103	CH 2	CH 3	CH 4	OUT-PUT VOLT	RE 803	RE 804	
5V	120A	—	100A	—	150A	—	5V	120A	150A	240W MAX.			5V	100A	360W MAX.			
2V	200A	200A	300A	400A	2V	20A	30A	20A	2V		10A	10A	5A	2V	15A	15A	5A	
5V	150A	160A	200A	300A	5V	20A	30A	20A	5V		10A	10A	5A	5V	15A	15A	5A	
12V	70A	70A	83A	125A	12V	20A	30A	20A	12V		10A	10A	2.5A	12V	15A	15A	2.5A	
15V	55A	55A	67A	100A	15V	16A	24A	16A	15V		8A	8A	2A	15V	12A	12A	2A	
24V	35A	35A	42A	63A	24V	10A	15A	10A	24V		5A	5A	1.5A	24V	7.5A	7.5A	1.25A	
28V	28A	30A	36A	54A	28V	8A	13A	8A	28V		4A	4A	1A	28V	6.5A	6.5A	1A	
MAX PWR.	750W	800W	1000W	1500W	MAX PWR.	750W	800W	1000W	MAX PWR.	750W	1000W			MAX PWR.	800W			
PRICE	\$809	\$875	\$1068	\$1285	PRICE	\$863	\$929	\$1133	PRICE	750W TRIPLE 750W QUAD	\$891	\$923	1000W TRIPLE 1000W QUAD	\$1143	\$1185	PRICE	TRIPLE	QUAD
																	\$957	\$989

acdc

electronics

401 Jones Road, Oceanside, CA 92054 • (714) 757-1880 • TWX 910-322-1470

(continued from page 218)



Although fewer devices are available for the high performance VERSABUS than the Unibus, UNI/VERS gateways link the vast DEC compatible product lines to the VERSABUS, while a wide range of high speed datacom bridges are made available to DEC users.

1M words/s. Otherwise, programmed control elements limit the transfer speed. The gateway's control speed is limited only by Schottky TTL logic, making it much faster than semiconductor RAMs.

UNI/VERS' dual boards are joined by a standard 12' (4-m) cable. On the Unibus side, the cable assembly connects with a circuit board occupying one slot of a DEC backplane. On the VERSABUS side, the cable assembly connects to a 9" x 14" (23- x 36-cm) board occupying one full slot in the VERSABUS backplane. Prior to insertion, the user defines base address assignments and range boundaries.

The bridge is immediately ready for transparent mode transfers. For DMA mode, host operating systems must initialize four registers on the VERSABUS side. Interbus protocol is supported by 16 dual-port registers and 16 user-defined registers.

UNI/VERS gateways are priced at \$5000 per set in unit quantity; OEM discounts are available. **Associated Computer Consultants**, 720 Santa Barbara St, Santa Barbara, CA 93101.

Circle 260

Collision free LAN provides stability under all network loads



Token/Net local area network system capitalizes on a token passing controlled access scheme via broadband CATV cable. The modularly designed, field upgradable LAN from Concord Data Systems operates at 5M bps over virtually unlimited distances. Token/Net is claimed to be the first LAN to fully comply with IEEE 802 and ECMA standards for local networks and token passing schemes. Most datacom equipment

manufacturers endorse these guidelines. As equipment becomes standardized, network connection costs may sharply decrease.

Interface modules that support both synchronous and asynchronous devices connect data terminal equipment (DTE) into the LAN. The modules operate at all popular data rates, adding to vendor flexibility. Each Token/Net interface module (TIM) holds a modem, access unit, control unit, and optional function boards.

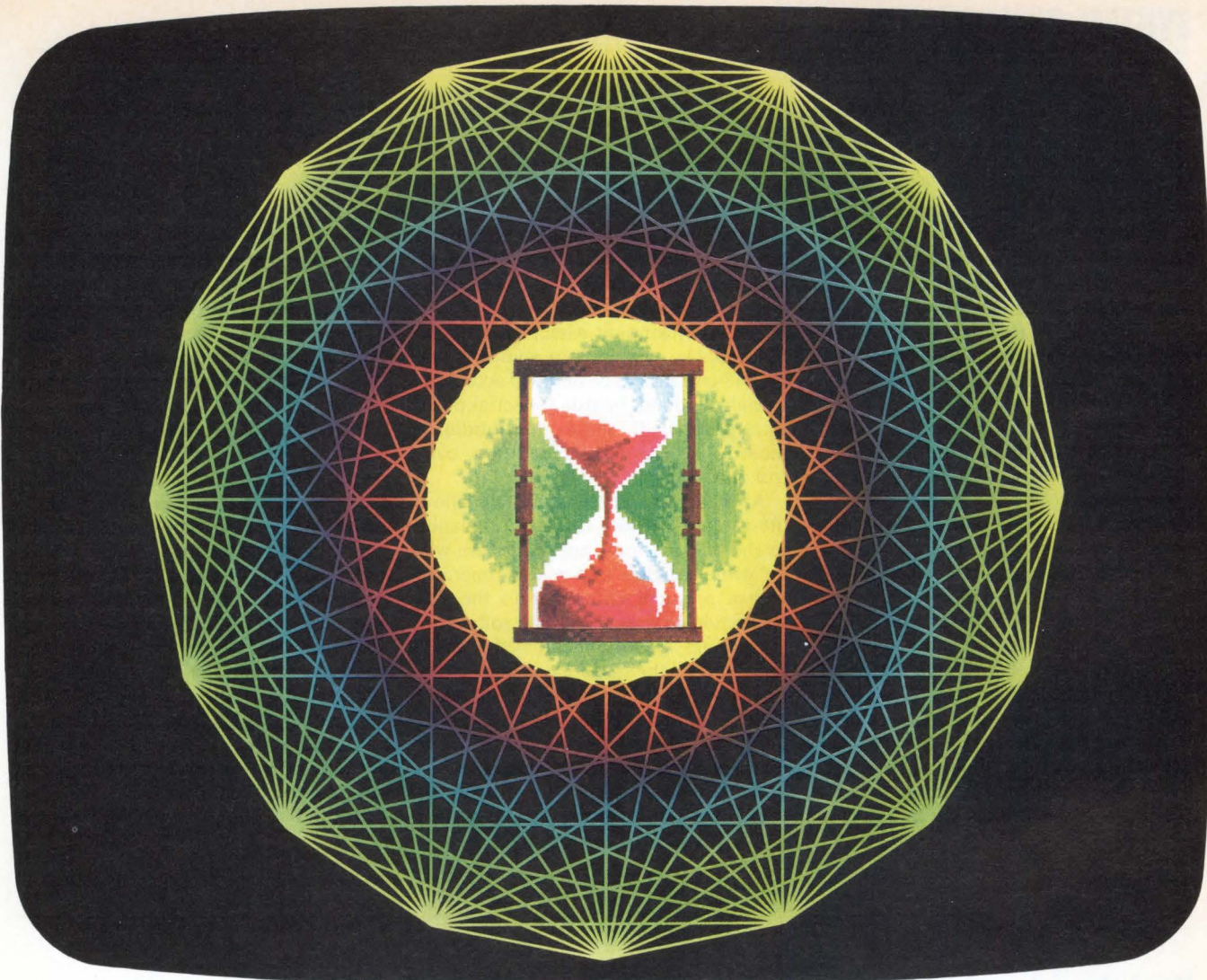
A form of distributed polling, the token passing controlled access method defines a set of rules for sharing high speed network bandwidth. This method is more stable under all network loads than the alternate carrier sense multiple access (CSMA) method. Out of band transmissions are strictly controlled to

allow adjacent channel operation. Since token passing does not foster signal collisions, intermodulation effects caused by such collisions, and which affect other CATV services on the cable, are eliminated.

Token passing prioritizes data awaiting media access. Four priority levels can be assigned to each data port. The highest priority frames are transmitted whenever a receiving node gains the token. Other priority classes have individual target times which, unlike CSMA systems, can be independently determined.

Each standalone, portable TIM connects to a common high speed cable serving as the broadcast medium to all other TIMs. High speed data packet messages are transmitted (invisible to the network user) over the shared communications medium, in a manner similar to time division multiple access. Data packets can also be optionally encrypted

(continued on page 222)



Our Past Is Your Future

Ikegami Technology

For systems applications requiring high quality, dependable CRT display monitors, Ikegami brings you the technology of the future, today. An innovator in video technology for over 36 years and the world's leading producer of high quality broadcast camera systems and monitors, Ikegami has applied its unparalleled experience to the design and production of display monitors for the computer industry. Put Ikegami's Emmy award-winning digital techniques for automatic setup to work for you.



©NATAS/ATAS

HDM Series

Ultra high resolution for your most demanding graphics systems. Ikegami's HDM Series color and monochrome display monitors utilize a delta-gun, raster-scan CRT and superb quality wide band, high speed scan, video amplifiers to provide the precision you need (up to 1280 × 1024 pixels interlace mode), plus the long life and easy maintenance you demand from a top quality graphics display. Available in 19V and 25V CRT sizes.

The CD Series (CDA/CDB)

Quickly becoming our most popular line of high resolution in-line gun

For more information on high-performance CRT display units designed to meet your needs, today and tomorrow, write or call Ikegami today.

color CRT display monitors. If your requirements are for high resolution (up to 1024 × 1024 pixels interlace mode), stable operation and very low maintenance, the CD Series may be your solution.

Available in 13V and 19V analog or digital models, the compact-size CD Series is perfect for simulation, medical, CAD/CAM and other high resolution applications.

The UD Series

Medium resolution, digital drive, color display monitors for business graphics systems. The Ikegami UD Series provides high performance (615 × 240 or more pixels interlace mode) at a very economical price.

The BDM Series

High performance, flicker-free monochrome CRT display units that bring Ikegami quality to word processing or on-line data entry systems. Available in green or white display and standard CRT sizes (5", 9", 12", 14" and 15").

Easy Interface. Easy Maintenance.

Ikegami display monitors are designed to interface with your equipment, quickly and easily. There's no complex rework ... no hassle. Ikegami's sophisticated design virtually eliminates maintenance problems, so you know your Ikegami displays will continue to bring out the best in your systems, year after year.

Ikegami®

We are the future.

CIRCLE 133

East — 37 Brook Avenue
Maywood, NJ 07607
(201) 368-9171

West — 3445 Kashiwa Street
Torrance, CA 90505
(213) 534-0050

(continued from page 220)

before transmission for added security. The TIMs simultaneously monitor the medium for incoming messages. On arrival, messages are error checked and passed to other receiver functions within the interface module. Permanent virtual circuits are provided for dedicated point to point or multipoint configurations. Switched virtual circuits are also available for flexible phone-like dial-up of connections.

Three interface module configurations are available. The TIM-200 desktop unit interfaces to two DTE devices. Measuring 15" x 12" x 3.5" (38 x 30 x 8.9 cm), it houses the radio frequency (rf) modem, as well as access and control units. It provides two 25-pin DB serial interface connectors and an F-type connector for attachment to the CATV cable.

TIM-220 adds two card positions to this basic design for optional boards and a larger power supply. The 15" x 12" x 5" (38- x 30- x 13-cm) unit lowers the cost

per connection by sharing the same rf modem, and access and control units among 10 user interfaces.

TIM-800 rackmount assembly, soon to be available, will fit in a standard EIA 19" (48-cm) rack. The unit will accept up to eight optional boards (34 serial ports total) that will share the module's modem, access unit, and 2-port control unit.

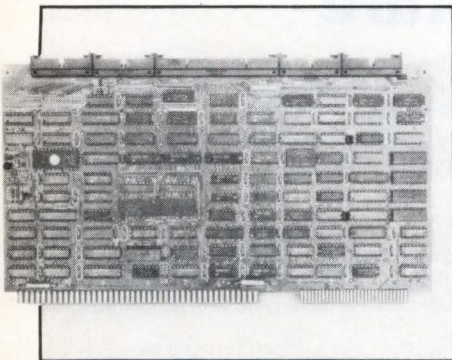
An accessory TIM-Keypad will allow the user to generate routing commands to the TIM. Its most applicable use will be with a digital device that operates with a protocol unfamiliar to the TIM connection services application software.

Optional boards include the quad serial port, the network management processor, and the soon to be marketed high speed serial port. The quad serial port provides interfaces for up to four data terminals and can be added to any base TIM unit except the TIM-200. It presents RS-232/V.24 interfaces to a data

terminal operating from 75 to 19.2k bps in synchronous or asynchronous modes. Network management processor boards provide network functions such as software reload and/or privacy key management. Multiple management processors can be installed to distribute and share functional responsibilities and to ensure that these functions can survive any single interface module failure. The high speed serial port will provide a single RS-449/V.35 serial/synchronous interface that will operate from 56k to 230.4k bps.

Among the network maintenance functions are local/remote diagnostics, integral signal level measurements, statistic utilities, monitoring facilities, and access control. The Token/Net LAN guarantees a stable network under all designated loads. Token/Net interface modules are priced from \$500 to \$2000 per connection, depending on configuration. **Concord Data Systems**, 303 Bear Hill Rd, Waltham, MA 02154. **Circle 261**

Peripheral controllers provide high throughput for Multibus systems



Xylogics' 450 disk peripheral and 472 tape peripheral controllers join with the 440 disk peripheral Multibus SMD controller to provide efficient operating performance and low bus use overhead for MC68000, 8086, or Z8000 microprocessor based systems. Since many Multibus systems use large capacity tape and disk controllers to extend the host computer's onboard processing power, mass storage use becomes optimally efficient when main memory can be quickly accessed and peripheral devices and data transfer are controlled at high speeds.

The 450 peripheral disk controller is a single-height Multibus PCB implementa-

tion of the dual-board 440 controller. It addresses up to 16M bytes of memory and controls up to four SMD drives per board at data transfer speeds up to 1.8M bytes/s. When attached to four disks, the 450 can access 2.4G bytes of disk storage. With appropriate memory, a full cylinder of data can be transferred to memory without losing a disk revolution.

Implementing channel control techniques improves bus operating efficiency and performance. Command chaining allows concurrent processor and peripheral operation without operating system intervention between commands. Each of several tasks can prepare its own command I/O parameter blocks (IOPBs) in system memory. The 450 controller then reads the command IOPB from system memory through DMA and performs the required function. When processing is complete, the IOPB is returned to memory via DMA with appropriate status data. Multiple IOPBs can be linked for optimal peripheral processor throughput. Scatter-read and gather-write functions can be implemented.

Support is given for 8- and 16-bit processors. The disk controller also features 32-bit ECC, overlapped seeks, a 2k-byte

FIFO buffer, and onboard diagnostics. The 450 peripheral disk controller sells for under \$1500.

Peripheral tape controller 472, for streaming and start/stop tape drives, resides on a single-height Multibus PCB. It addresses up to 16M bytes of memory and controls up to four tape drives per board, running at speeds from 12.5 to 100 ips at densities of 800-bpi NRZI, 1600-bpi PE, or 6250-bpi GCR. This peripheral controller also uses channel control techniques for an optimal match to the multiprocessing environment of the IEEE 796 bus and the newer 16/32-bit microprocessors.

Xylogics' Multibus 472 is program compatible with the 440 and 450 peripheral controllers. Drivers for these disk controllers need only slight modifications to drive the 472 tape controller. Like the 450, the 472 features 16-, 20-, or 24-bit addressing, onboard diagnostics, programmable throttle, and support for 8- and 16-bit processors. A 1k-byte FIFO buffer is provided. DMA circuitry transfers data at 2M bytes/s. The 472 tape controller sells for under \$1400. **Xylogics, Inc**, 144 Middlesex Tpke, Burlington, MA 01803. **Circle 262**

Professional Books That Help You Get Ahead—And Stay Ahead!

HANDBOOK OF ELECTRONICS PACKAGING DESIGN AND ENGINEERING
by B. S. Matisoff
582515-5 Pub. Pr., \$32.50 Club Pr., \$25.95

RADIO HANDBOOK, 22/e
by W.I. Orr
582442-6 Pub. Pr., \$39.95 Club Pr., \$33.95

MICROPROCESSOR DATA BOOK
by S. A. Money
427/062 Pub. Pr., \$35.00 Club Pr., \$27.00

STANDARD HANDBOOK FOR ELECTRICAL ENGINEERS, 11/e
by D. G. Fink & H. W. Beaty
209/74X Pub. Pr., \$65.95 Club Pr., \$48.95

INTUITIVE IC ELECTRONICS
by T. M. Frederickson
219/230 Pub. Pr., \$19.95 Club Pr., \$15.50

ELECTRONICS ENGINEERING FOR PROFESSIONAL ENGINEERS' EXAMS
by C. R. Hafer
254/303 Pub. Pr., \$27.50 Club Pr., \$21.50

OPTICAL FIBER SYSTEMS: Technology, Design & Applications
by C. K. Kao
332/770 Pub. Pr., \$26.00 Club Pr., \$20.00

INTRODUCTION TO RADAR SYSTEMS, 2/e
by M. I. Skolnik
579/091 Pub. Pr., \$39.95 Club Pr., \$31.00

MODERN ELECTRONIC CIRCUITS REFERENCE MANUAL
by J. Markus
404/461 Pub. Pr., \$67.95 Club Pr., \$52.95

BIT-SLICE MICROPROCESSOR DESIGN
by J. Mick & J. Brick
417/814 Pub. Pr., \$29.50 Club Pr., \$22.50

DIGITAL HARDWARE DESIGN
by J. B. Peatman
491/321 Pub. Pr., \$35.50 Club Pr., \$27.50

ELECTRONIC COMMUNICATION, 4/e
by R. L. Shrader
571/503 Pub. Pr., \$26.95 Club Pr., \$20.95

ANTENNA THEORY: Analysis and Design
by C. A. Balanis
582493-0 Pub. Pr., \$39.50 Club Pr., \$29.95

HANDBOOK OF OPERATIONAL AMPLIFIER CIRCUIT DESIGN
by D. E. Stout & M. Kaufman
617/97X Pub. Pr., \$38.00 Club Pr., \$29.00

MICROPROCESSOR APPLICATIONS HANDBOOK
by D. F. Stout
617/988 Pub. Pr., \$35.00 Club Pr., \$26.50

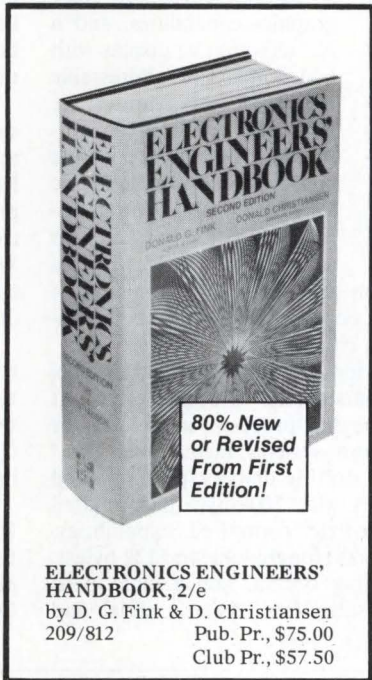
DIGITAL CIRCUITS AND MICROPROCESSORS
by H. Taub
629/455 Pub. Pr., \$32.95 Club Pr., \$25.50

ENGINEERING MATHEMATICS HANDBOOK, 2/e
by J. J. Tuma
654/298 Pub. Pr., \$31.25 Club Pr., \$24.95

ELECTRONIC FILTER DESIGN HANDBOOK
by A. B. Williams
704/309 Pub. Pr., \$41.50 Club Pr., \$31.50

HANDBOOK OF SEMICONDUCTOR AND BUBBLE MEMORIES
by W. A. Triebel & A. E. Chu
582376-4 Pub. Pr., \$24.95 Club Pr., \$18.50

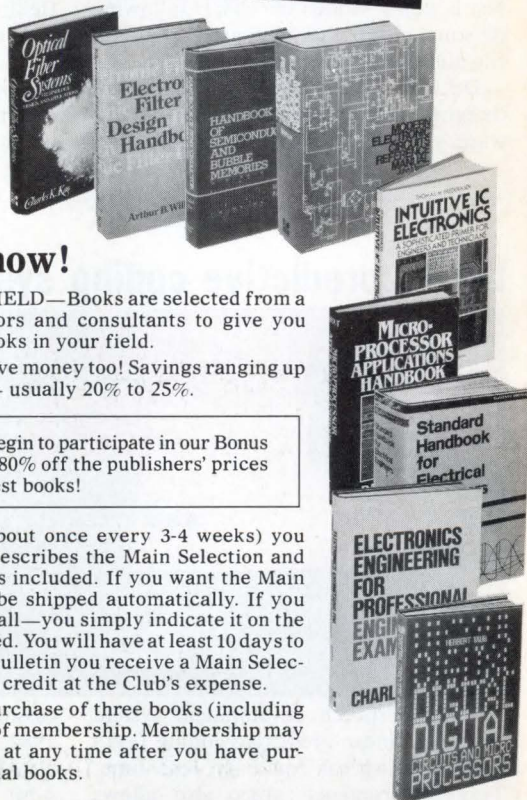
Join the **ELECTRONICS AND CONTROL ENGINEERS' BOOK CLUB** and...



ELECTRONICS ENGINEERS' HANDBOOK, 2/e
by D. G. Fink & D. Christiansen
209/812 Pub. Pr., \$75.00
Club Pr., \$57.50

- Keep up with current technology
- Sharpen your professional skills
- Be ready for new career opportunities
- Boost your earning power

New members!
Any one of these great professional books for only...
\$2.89 as a premium with your 1st selection!
Values up to \$75.00



Why YOU should join now!

- **BEST AND NEWEST BOOKS IN YOUR FIELD**—Books are selected from a wide range of publishers by expert editors and consultants to give you continuing access to the best and latest books in your field.
- **BIG SAVINGS**—Build your library and save money too! Savings ranging up to 30% or more off publishers' list prices— usually 20% to 25%.

BONUS BOOKS—You will immediately begin to participate in our Bonus Book Plan that allows you savings up to 80% off the publishers' prices of many professional and general interest books!

- **CONVENIENCE**—12-14 times a year (about once every 3-4 weeks) you receive the Club Bulletin FREE. It fully describes the Main Selection and alternate selections. A dated Reply Card is included. If you want the Main Selection, you simply do nothing—it will be shipped automatically. If you want an alternate selection—or no book at all—you simply indicate it on the Reply Card and return it by the date specified. You will have at least 10 days to decide. If, because of late delivery of the Bulletin you receive a Main Selection you do not want, you may return it for credit at the Club's expense.

As a Club member you agree only to the purchase of three books (including your first selection) during your first year of membership. Membership may be discontinued by either you or the Club at any time after you have purchased the first selection plus two additional books.

MAIL THIS COUPON TODAY

McGraw-Hill Book Clubs
Electronics and Control Engineers' Book Club
P.O. Box 582, Hightstown, N. J. 08520

Write Code No. of the \$2.89 selection here

Write Code No. of First Selection here

Please enroll me as a member and send me the two books indicated, billing me for the \$2.89 premium and my first selection at the discounted member's price, plus local tax, shipping and handling charges. I agree to purchase a minimum of two additional books during my first year of membership as outlined under the Club plan described in this ad. A shipping and handling charge is added to all shipments.

Signature _____

Name _____

Address/Apt. _____

City/State/Zip _____

This order subject to acceptance by McGraw-Hill. All prices subject to change without notice. Offer good only to new members. Orders from outside the U.S. cannot be accepted.

E33624



Vendor independent small computer networking system



With the Decision Mate V series of microcomputers, and the Decision Net local area network system for linking small computers from various manufacturers into a resource sharing network, NCR Corp enters the lucrative OEM personal computer arena. Key to Decision Net is NCR's Modus file sharer, allowing personal computers to share a common file and peripheral pool.

Decision Mate V computers are designed around industry standard hardware/software subsystems. Single- and

dual-processor models are available with 512k-byte memory, flexible or Winchester disk drives, high speed monochrome or color graphics capabilities, and a 12" (30-cm) CRT display with 640 x 400 dot addressable resolution. All features are integrated into a small footprint, low profile cabinet and detached alphanumeric keyboard with 20 programmable function keys. System sophistication ranges from a single 8-bit Z80A processor running at 4 MHz to a coprocessing Z80/8088 combination using either CP/M or MS-DOS.

Prices for an 8-bit processor model with monochrome graphics start at \$2800. The dual-processor model sells for \$3340. Both systems include two 5 1/4" flexible, double-density/double-sided disk drives with 500k-byte unformatted and 320k-byte formatted capabilities, 64k-byte RAM (upgradable to 512k bytes), an operating system, and a high speed graphics subsystem. RS-232-C serial and

Centronics parallel interfaces provided. The computers can also be configured with one flexible disk and one 5 1/4" Winchester with 12.76M-byte unformatted and 10M-byte formatted capacities. Single-processor model deliveries begin immediately; the dual-processor model will be available in June.

With Decision Net, concurrently shared data among personal computers is accomplished via Omninet LAN and the Modus file sharer. Modus employs an I/O processor with onboard RAM and controlware, a 5 1/4" formatted flexible disk, a Winchester with 10M- to 96M-byte capacity, and an optional streaming tape drive.

Up to 64 computers can be linked into the carrier sense multiple access (CSMA) LAN. Data are transmitted at 1M bps over twisted pair cable links up to 4000' (1.2 km) in length. The network is user installable and field upgradable.

Decision Net deliveries are scheduled for June. Prices are \$9995 for the Modus file sharer and \$500 per personal computer networking. **NCR Corp**, Dayton, OH 45479. **Circle 263**

Linear predictive coding system synthesizes speech in real time



The SDS50 speech development system processes linear predictive coding (LPC) synthesized-speech data in real time. Texas Instruments' SDS50 also allows users to edit LPC speech data via any RS-232-C compatible terminal. This system can record, store, and edit data for both prerecorded words and allophone strings. Pitch, energy, and vocal effects can be modified by the user, then immediately produced through the system's loudspeaker. Commands can also be issued to store results in EPROM via an optional built-in EPROM programmer.

Words and phrases require fewer than 1.8k bps of memory space, representing

a 50:1 reduction in space requirements over directly digitized speech waveforms. Up to 12 s of speech can be accommodated in the system's 16k bytes of available RAM. This data can be uploaded to, or downloaded from, a host computer.

Four microcomputer boards make up the system—a custom processor board, a CPU, a memory board, and either the TMS5110A or TMS5220 voice synthesis processor (VSP) (*Computer Design*, Feb 1982, p 33 and July 1982, p 85). The 5110A VSP can be combined with standard 4-bit microcomputers, a TMS6100 or TMS6125 voice synthesis memory (VSM) chip, and a speaker to form a complete speech synthesis system. Processing LPC speech data that have been prerecorded and stored in VSMS or EPROMs, the 5110A outputs male, female, or children's voices, along with tones, chimes, and sound effects.

For applications based on 8- and 16-bit microprocessors, the 5220 VSP features TTL compatibility, an 8-bit bus, and a FIFO buffer. The 5220, in effect, handles all I/O and processing operations

needed to produce speech. It synthesizes the same sound effects as the 5110A, and accepts speech data from VSMS, EPROMs, and the host processor. The 5220 processes LPC prerecorded speech data and can also process LPC allophone speech, providing the potential to develop an unlimited vocabulary.

Custom or semicustom vocabularies can be developed through the 6100 or 6125 voice synthesis ROM chips, which hold the prerecorded custom vocabularies. The 6100 128k-bit ROM stores approximately 2 min of synthesized speech, while the 6125 32k-bit chip stores approximately 30 s of speech. Both devices feature onchip address decode logic that allows any VSP to work with up to sixteen 6100 or four 6125 VSMS without additional address decoding circuitry. The 6100 or 6125 can also be supplied as a series of low cost prepackaged vocabulary ROMs that currently include industrial, numeric and time, avionic, weather and time, and military vocabulary sets.

The SDS50 LPC speech synthesis system is available for \$16,000, with a four to six week delivery time. Options are available. **Texas Instruments Inc, Semiconductor Group**, PO Box 401560, Dallas, TX 75240.

Circle 264

PERIPHERAL TESTING: MORE THAN A QUESTION OF PASS/FAIL

Testing any rotating memory device involves more than the simple question of pass/fail. It is a complex set of questions encompassing the how's, when's and why's of testing. Applied Circuit Technology designs and manufactures final production and incoming inspection test equipment that answers the complex requirements of testing. Designed for volume throughput, ACT's equipment has solved the testing dilemma for many manufacturers. We've helped insure the reliable performance of rotating memory devices and assisted the manufacturers in achieving a low 2% return rate of shipped product.

ACT's equipment has tested more 5¼" Winchester disk drives than any other system in the world. Our expertise, however, does not stop at Winchester drives. Today,

Applied Circuit Technology is involved in floppy systems test, tape systems test, fixed/removable Winchester disk systems test as well as Servo Writers and Spiral Testers.

Whether you are shipping or receiving 10 or 10,000 units a month, Applied Circuit Technology provides the answer to high volume, in-depth, final production testing.

If you realize that testing is more than a question of pass/fail, contact Applied Circuit Technology.



Applied
Circuit
Technology

2931 La Jolla Street
Anaheim, CA 92806
(714) 632-9230



Available in first quarter 1983: ACT's new MTS (Modular Test System)

Time interval scope with picosecond accuracy and resolution



Offering 50-ps accuracy and 10-ps resolution, Hewlett-Packard's HP 1726A time interval oscilloscope makes fast, reliable timing measurements on complex, repetitive signals. Counter and oscilloscope technologies are combined to yield the viewing and measuring effectiveness of a 275-MHz scope and the ease of use of a time interval counter.

Designed for precise timing measurements, the instrument is configured with a crystal referenced time base in conjunc-

tion with a CRT and stable triggering circuits. This combination enables the scope to display the signal being tested, as well as to measure the designated interval with its 50-ps accuracy. Drawing timing measurements from a crystal referenced time base permits precise time interval measurements relative to the trigger event that synchronizes the waveform display.

First-pulse measurements can thereby be made with a ± 30 -ps characteristic repeatability. The crystal referenced time base uses a horizontal sweep vernier out of calibration to extend the measurement range by a factor of three. For example, the scope can measure time intervals as long as $1.2 \mu\text{s}$ with ± 10 -ps resolution and 50-ps accuracy. A dual-marker system supplies precise measurements from specific points on any waveform displayed. In addition, the unit's matched wideband preamplifiers allow a waveform's signal fidelity to be examined.

Overlap and triggered modes incorporate time interval averaging, which supports precise measurements on virtually any repetitive signal displayable on an oscilloscope. Overlap mode takes measurements from specific points on the displayed waveform. Time intervals are measured through two intensified markers that simultaneously appear on the scope's CRT and are displayed on successive sweeps. Measurements are calculated by the interval from the main trigger event to the start event, the time from the main trigger event to the stop event, and the time interval difference between the start/stop events.

For rapid, multiple timing measurements, triggered mode is controlled by set levels that the start/stop events should trigger. The difference between the trigger level of the start intensified marker to the trigger point of the stop intensified marker is then calculated. Results are repeatable to within ± 30 ps. The oscilloscope also features fast mode operation that reduces the number of averages required for a measurement by a factor of 10. HP 1726A is \$7675. A standard HP-IB interface is included on the unit. Contact local **Hewlett-Packard** sales offices. **Circle 265**

Token passing local area network system hooks to 500 devices



Planet series of local area network products extends Racal-Milgo's long-haul communications products into resource sharing and networking of independent devices that operate in a totally protocol transparent environment. Although the series was introduced on the European market a year ago, the Planet Token Ring series is the first to be domestically available. It uses baseband coaxial cable in a twin ring configuration as the local area communications link. The system can operate in either full- or half-duplex modes.

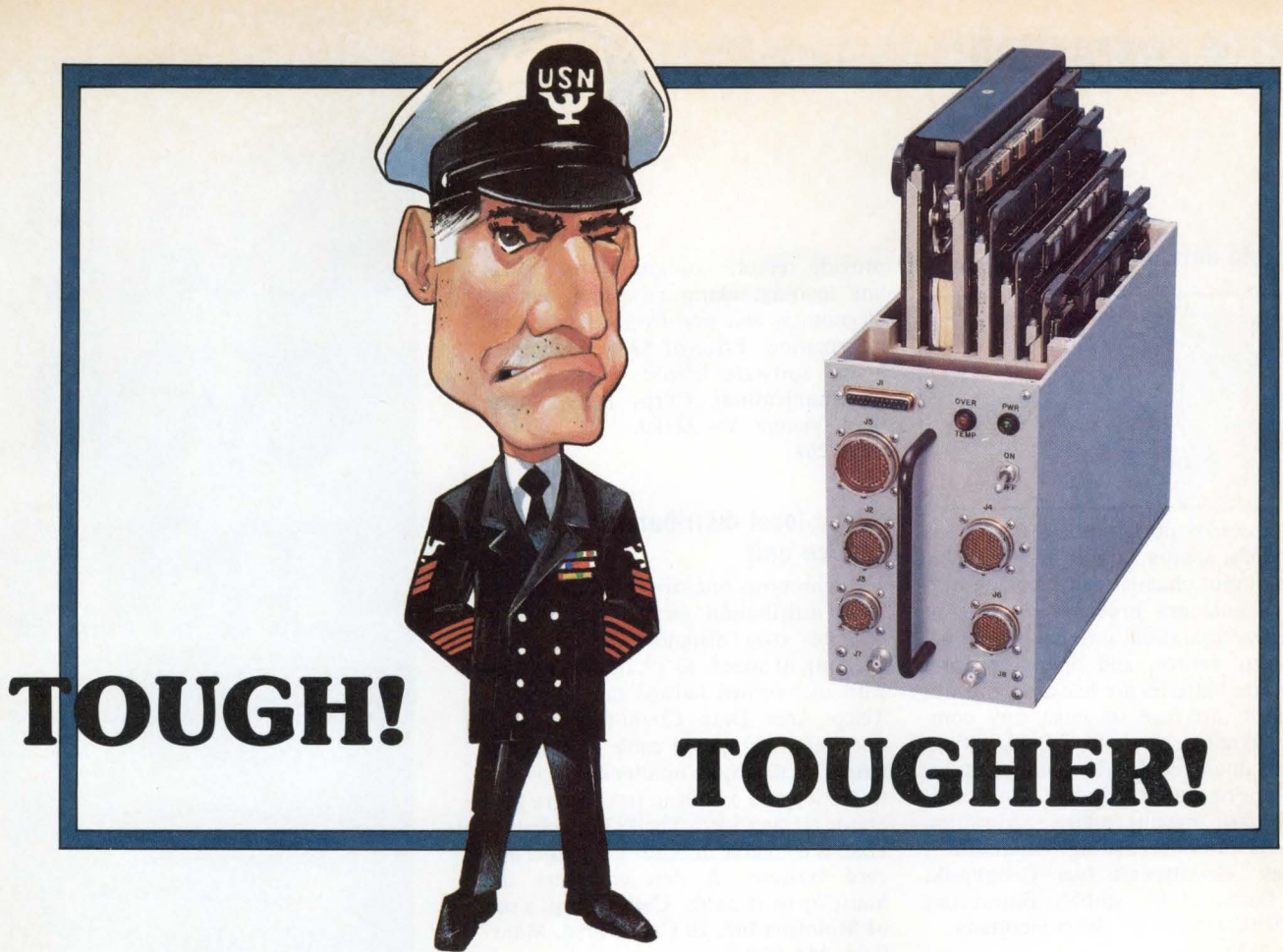
Each Token Ring configuration accepts up to 500 communications peripherals. The Planet Director PL3000, an intelligent desktop network processor, controls the communications link. The Director manages all connection paths, disconnections, system failures, queuing entries, port profile summaries, and transfers. The Director stores the LAN's data base, including the 500 possible user and port parameters per ring and the 250 simultaneous connections in nonvolatile RAM. Port selection and contention enable device contention for, and sharing of, a limited number of typically expensive computer ports by a greater number of low-cost terminals.

System interface is through the PL2000 Terminal Access Points (TAPs). Each of up to 250 TAPs has two RS-232-C ports that can operate synchronously, asynchronously, or in mixed mode at speeds up to 19.2k bps per port, independent of user protocol. Once access to the net-

work is obtained from a TAP, the TAP acts as a packet assembler/disassembler, passing data into and from the network. The network can be easily expanded by adding more TAPs.

PL1000 Cable Access Points (CAPs) interface the TAPs to the digital Planet ring. This coaxial cable interface consists of four standard connections, with each TAP connected through a 15-pin D-type connector. Additional CAPs can be installed anywhere along the cable, without interrupting data flow.

The Planet series supports any combination of point-to-point, multidrop, or broadcast circuit plans, in permanent or switched modes that work simultaneously. Each virtual circuit appears to the user to be a dedicated line connection. Using any authorized terminal on the ring, this connection can be easily reconfigured without recabling, external switching, or special software. A failsafe mechanism allows the system to reconfigure itself, bypass a given problem, and automatically reestablish the communications link. **Racal-Milgo, Ltd**, 8600 NW 41st St, PO Box 520399, Miami, FL 33152. **Circle 266**



EMM's SECS 80 Ruggedized Microcomputers Work Where Others Won't - We've Proved it Over 1000 Times!

Tried and Tested Through the Years

When the going gets tough, you want rugged quality you can depend on — whether it's in today's military spirit or your microcomputer system.

Already, there are over 1000 SECS 80 units in use, serving in airborne, shipboard, and ground systems as well as tough industrial applications.

In short, EMM's Severe Environment Computer Systems have an extensive history of dependable performance — under the most hostile conditions.

Complete Systems, Built to MIL Specs

The SECS 80 family is comprised of a variety of total microcomputer systems, each software compatible with Intel's® standard systems. Numerous support modules are available, including 8080, 8085, 8088 and 8086 CPU's, memory, and I/O expansion modules (PIO, SIO, A/D, D/A and 1553).

As for **tough**, each component of these 8- and 16-bit computers is built to Military Specs, meeting or exceeding the stringent requirements of MIL-E-4158, 5400, 16400...and more.

Eases the Design Burden

Available software and field-proven components simplify the task of designing a ruggedized computer system. For example, compatible software includes the RMX-88® real-time multitasking Executive as well as Fortran, Pascal, PL/M and a MIL-STD 1589B Jovial (J-73) Cross Compiler.

Thus you develop software for your military computer system using off-the-shelf Intel commercial systems. Then you need only transfer the software to a ruggedized SECS 80 system.

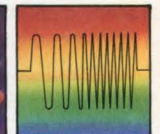
Call or Write for Details — Today!

The full SECS 80 story is available in a new brochure. Just contact us today for your free copy.

RMX 88 and Intel are trademarks of Intel Corporation.



Severe Environment Systems Company
A Subsidiary of Electronic Memories & Magnetics Corporation
P.O. Box 2668 • Chatsworth, CA 91311
Telephone: (213) 998-9090 • TELEX: 69-1404



COMPUTER PRODUCTS FOR SEVERE ENVIRONMENTS

France, Italy, Spain & Belgium
Tel. France (6) 085 1255
Telex 600 233

Germany, Switzerland, Austria & Holland
Tel. Germany (06171) 2931
Telex 0410734

U.K., Scandinavia & European Head Office
Tel. U.K. (0628) 72134
Telex 849298

Portable data/memory logger



MDL/600 CMOS portable data logger has 2k to 65k analog sample activity. One analog input channel and 1 analog output channel are provided. Twelve-bit digitizing resolution, internal or external triggering source, and operation from 8-AA size batteries are featured. Std v.24 provides interface to most any computer, terminal, or modem. Data/settings remain unaltered for 10 years or more, even during battery change. Unit combines data logging/online acquisition and memory recording capabilities. **Geotek, Gesellschaft fuer Geophysik, und Datentechnik gmbH, Bluecherstr 32, D-1000 Berlin 61, West Germany.** Circle 267

X.25 compatible concentrator pad

Micro800/X.25 concentrator pad packets data from up to 16 asynchronous terminals/ports for transmission over a single phone line to a public or private X.25 packet data network. Certified for use on Telenet, Tymnet, and Uninet networks in the U.S. (international certification pending), the concentrator requires no changes to existing hardware or software. Unit stores user selectable, preprogrammed parameter channel profiles. Channel configuration data can also be downline loaded from a central site and stored in nonvolatile memory. Several add-on functions are available at no cost. **Micom Systems, Inc, 20151 Nordhoff St, Chatsworth, CA 91311.** Circle 268

Low cost X.25 concentrator accesses packet switched networks

A small scale X.25 network interface processor for access to public or dedicated packet switched networks, the TP3005 concentrator supports CCITT X.3, X.28, and X.29 async terminals, as well as Telenet enhanced parameters. An X.25 port provides a high speed access link to the network and conforms to CCITT X.25 1980 or 1976 recommendations. The company's network control facilities

provide remote configurations, down-line loading, alarm reporting, remote diagnostics, and port-by-port accounting information. Price of \$2350 includes a 3-year software license. **GTE Telenet Communications Corp, 8229 Boone Blvd, Vienna, VA 22180.** Circle 269

Async local distribution service unit

Asynchronous line driver model 8150, a local distribution service unit (LDSU), operates over distances up to 23 mi (37 km), at speeds to 19.2k bps. For use with user-owned twisted pair cables or Telco Area Data Channels, the 8150 operates over loaded cable at 4800 bps max. Local/remote unattended diagnostic testing and a built-in test pattern generator are provided. The \$335 single-unit LDSU is available in both standalone and card versions. A nest enclosure can house up to 16 cards. **Codex Corp, a sub of Motorola Inc, 20 Cabot Blvd, Mansfield, MA 02048.**



Circle 270

Networking system supports 800 or more ports

Two switching statistical multiplexers added to the Microplexer® family provide 96 or 144 local ports and are geared to networks requiring 800 or more total ports. User friendly features add reliability even in complex larger networks. The networking systems also provide dedicated or switched port assignment, camp-on facilities, password protection, and traffic balancing. The included Configurator subsystem, based on a 16-bit microcomputer, runs menu-driven utility programs that simplify setup, reconfiguration, and network interrogation. Delivery is scheduled for the second quarter of 1983. **Timeplex, Inc, 1 Communications Plaza, Rochelle Park, NJ 07662.** Circle 271

Save even more.

Effective immediately, System 2000 terminals are priced lower than ever before.

In quantities of 50, you can buy System 2000 black and white terminals for \$7,425.

Color terminals, in quantities of 50, for \$10,200.

To place your orders call (617) 663-8550.

LEXIDATA
The clear choice in raster graphics.

A new, improved way to give your competition headaches.

(System 2000 terminals, \$8,250*.)

The Lexidata System 2000. In terms of price, it's the most affordable step forward in raster technology since the development of raster technology.

In terms of performance, System 2000 will outdo any terminal near it in price and many that cost considerably more.

The combination of which will give you an edge if you're an OEM. In fact, quite a considerable edge.

And what will it give your competition? Something to keep them awake nights.

More OEM flexibility

There are five processor option slots in a System 2000 terminal. They'll allow you to add more serial ports, and more program memory (up to 1.28 megabytes).

A detachable keyboard with integral joystick is standard with pre-programmed peripheral interfaces.

User code may be downloaded to augment the system's capabilities, off-load the host CPU, and increase system response time.

Low price. High performance. And a whole new bend in flexibility.

A new ergonomic policy

On the screen, there are four hardware assisted work spaces. Each with a set of functions that

you can call up with simple English commands.

These individual workspaces reduce the overall system cost by eliminating the need for a separate alphanumeric display and a menu space on the digitizer work surface.

This feature, plus the fact that the System 2000 has a multitasking operating system, contribute to two very important aspects of customer concern: Ease of learning and ease of use.

Improves Tektronix™ PLOT-10™ four ways

You can put the System 2000 in a PLOT-10 environment very simply. And very quickly, you can improve that environment.

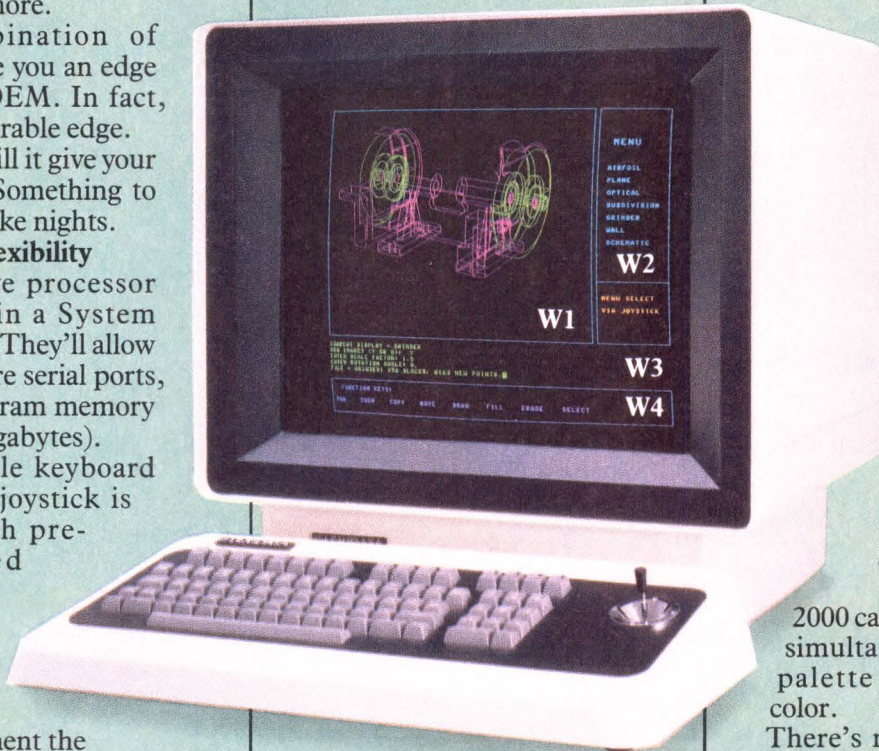
The System 2000 will give you a 62.5% higher resolution on a 1280 by 1024 line screen.

In black and white, the System 2000 will give you steady, flicker-free graphics. At a refresh rate of 60 Hz.

In color, the System 2000 can provide you with 16 simultaneous colors from a palette of 4096 shades of color.

There's more, too. Standard features like zoom, pan, text scroll and independently controlled cursors. And options like an 11" x 11" data tablet and a hard copy interface.

If you're interested in a demonstration of all this call (617) 663-8550 or write to us at 755 Middlesex Turnpike, Billerica, MA 01865. TWX 710-347-1574.



What the 4 workspaces do:

W1 Supports pan and zoom. Ideal for interactive graphics.

W2 Accommodates system-select menus.

W3 Is perfect for processing text.

W4 Is used for logging messages or annotating keyboard function keys.

Note: Each workspace has graphics and text cursors and is adjustable in size.

LEXIDATA

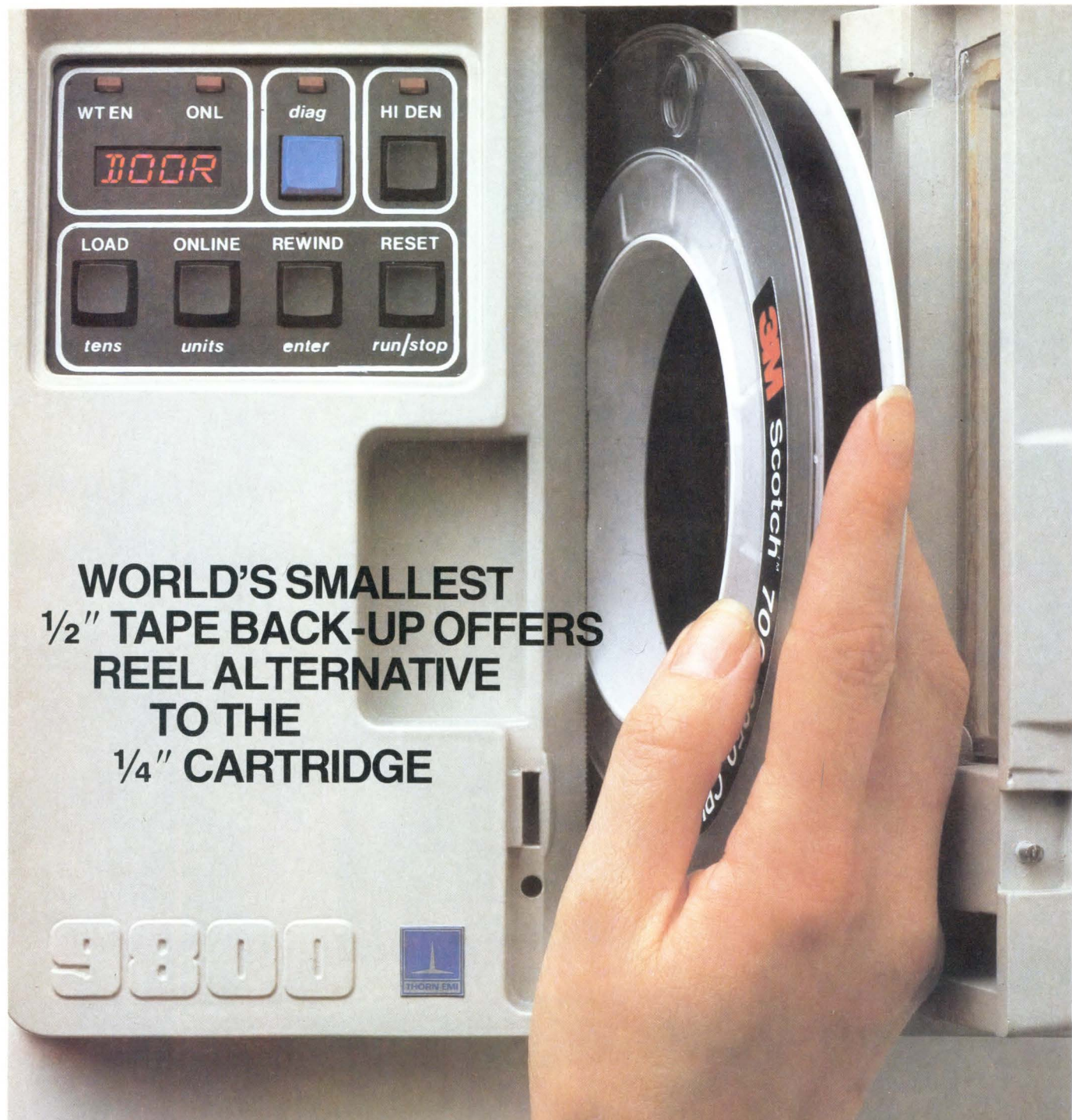
The clear choice in raster graphics.

*PLOT-10 is a registered trademark of TEKTRONIX

* System 2000, black and white model, \$8250 in quantities of 50.

System 2000, color model, \$11,621 in quantities of 50.

© 1982 Lexidata Corporation



**WORLD'S SMALLEST
1/2" TAPE BACK-UP OFFERS
REEL ALTERNATIVE
TO THE
1/4" CARTRIDGE**

Providing low cost back-up for Winchester drives the miniature 2-speed EMISTREAMER 9800 is as easy to use as a cartridge, offers proven reliability and universal interchange.

The 9800 fits within a twin 8" floppy enclosure and automatically loads the standard, multisourced 7" reel of 1/2" wide computer tape. The unformatted capacity is 15 Mbytes at 1600 bpi, PE, optional 30 Mbytes at 3200 bpi. With full IBM/ANSI format compatibility the world's smallest standard 1/2" tape drive with Industry standard interface is the REEL alternative you have been looking for.

Also in the EMISTREAMER range are the autoloading 9900 with total capacity of over 60 Mbytes (120 Mbytes optional) and the high performance 8900. These low cost streamers provide reliable data interchange between the smallest micro and the largest mainframe. Contact us now for full details.

9800 is designed for high reliability—practical features include:

- Short tape path
- Autoload
- PCB access from the top
- Three levels of diagnostics
- Alphanumeric display



**THORN EMI
Datatech**

THORN EMI Technology Inc 8601 Dunwoody Place Suite 301
Atlanta GA 30338 tel: (404) 587 0017 telex 810766 2267

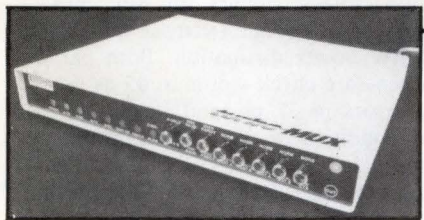
In Europe contact:

THORN EMI Datatech Ltd Data Products Division Spur Road
Feltham Middlesex TW14 0TD England tel 01-890 1477 telex 23995

THORN EMI companies

EMISTREAMERS FOR BACK-UP PLUS UNIVERSAL DATA INTERCHANGE

2400-baud, 212A compatible stat mux



TurbOMUX microcomputer based multiplexer doubles the throughput of a 1200-baud modem to 2400-baud full-duplex operation. The 2-channel stat mux attaches via std RS-232-C interfaces to the 212A modem on one end, and to DTE on the other end. A proprietary data compaction algorithm guarantees 100% data reproduction fidelity. During data transmission, each unit receives and dynamically compacts messages. Error-free detection and retransmission facilities are provided. Prices range from \$995 to \$1275. **Chung Telecommunications Inc**, 4046 Ben Lomond Dr, Palo Alto, CA 94306. Circle 272

Low cost 212A type modem



VA212LC is a Bell compatible switched network originate/answer, 1200-bps and 0- to 300-bps full-duplex modem. It features a combined microprocessor and LSI technology design configured on a single PC card. Modem is 1.5" (3.8 cm) high. Voice mode disables the auto-answer function. Five LEDs display modem's operational status. Modem (\$550) uses an automatic detection algorithm to handle both 9- and 10-bit char codes and an auto self-test routine. **Racal-Vadic**, 222 Caspian Dr, Sunnyvale, CA 94086. Circle 273

Tell us what you like

Did you remember to rate the articles in this issue of Computer Design? Turn to the Editorial Score Box on the Reader Inquiry Card.

COMPUTERS

Low cost UNIX system

A combined System III version of UNIX OS and a series of packaged NAKED MINI[®] computer systems provides multi-user, timesharing, 16-bit superminicomputer capability for \$7990, quantity 200. The system contains a Series 5 processor with memory management, 256k-byte ECC

RAM (expandable to 1M byte), 1M-byte floppy disk subsystem, 10M-byte Winchester, and 4 serial I/O ports. License price for the company's 16-user UNIX is \$789; a 32-user version is \$1198. UNIX is configured on several NAKED MINI Series 5 systems with prices of \$7990 to \$94,875. **Computer Automation Inc**, 18651 Von Karman, Irvine, CA 92713. Circle 322

FRANKLIN . . . THE ONLY UPS WITH A WRITTEN GUARANTEE AND A PENALTY CLAUSE



Franklin guarantees Uninterruptible Power System efficiency ratings down to 25% of full load . . . in writing.

And backs it up . . . with cash.

Figuring efficiency at full-rated load doesn't square with the real world. Most UPS operate in the 30-65% range of full-rated load.

Franklin UPS will hold their efficiency ratings at 75%, 50% and as low as 25% of full-rated load. We guarantee it.

It takes superb design and outstanding quality to maintain high-efficiencies at these crucial levels.

We've always produced the highest efficiency UPS available. And we'll continue to do so.

That's why we'll give you a cash reimbursement for five years of power if your Franklin UPS doesn't achieve written guaranteed efficiency ratings.

Call or write us today for complete information.

CALL TOLL-FREE

800-538-1770

IN CALIFORNIA (408) 245-8900



Franklin Electric
Programmed Power Division

995 Benicia Avenue • Sunnyvale, CA 94086 • Telex: 357-405

Control circuits for switched mode power supplies

TDA 4700/4718 switched mode power supply regulator ICs provide voltage control of single-ended and pushpull applications. Integrated control components minimize total components count and provide the switcher controlled systems with feed forward control, double

impulse suppression, under/overvoltage protection, soft start, PLL operation for external synchronization, and symmetry inputs. TDA 4700 has an op amp for use in a control loop. TDA 4718 has no op amp. Versions are available in cerDIPs or plastic packages. **Siemens Components, Inc.**, PO Box 1000, Iselin, NJ 08830. **Circle 274**

Low power Schottky 8-bit EDAC

Two parallel error detection and correction (EDAC) circuits for 8-bit processors, SN74LS636 and SN74LS637 have typ 500-mW power dissipation. Both parts can generate check words in 45 ns typ, flag errors in 27 ns, and flag a gross error condition of all high outputs from memory as a dual-bit error. Modified Hamming code generates a 5-bit check word from an 8-bit data word. SN74LS636 3-state output and SN74LS637 open collector output configurations are provided in 20-pin 300-mil plastic and ceramic DIPs. Prices range from \$16.43 to \$24.65. **Texas Instruments Inc.**, PO Box 401560, Dallas, TX 75240. **Circle 275**

SYSTEM-READY MULTIBUS™ COMMUNICATIONS FROM ETI MICRO

SAVES TIME ... SAVES MONEY

We include sophisticated, user-proven, communication processing firmware as a standard feature on our multibus-compatible communication controllers, to cut your time to market and save precious dollars.

Our 8103 and 8140 controllers feature:

- two Bell modem ports and two RS232C ports
- controls up to 255 ETI Micro remotes
- communicates over twisted pair, leased phone lines or radio
- performs real-time multiple communication tasks
- interrupt-driven, communication processing firmware
- supports packet-switching protocol

- source codes listed for implementing custom protocols

Combine our 8183 (FCC approved) Direct Access Arrangement with the 8140 and get rotary auto-dial and auto-answer.

		Quantity: 1
8103	Controller with two Bell 202 modems. Two RS232C ports	\$1,020
8140	Controller with two modems. (Bell 103/202, CCITT V.21, V.23) Two RS232C ports	\$1,240
8183	DAA Interface (FCC Part 68 Registered)	\$ 190
8182	Lightning Protector, Transformer Coupled	\$ 111

We've done it for you...two levels of processing firmware! For a system-ready communications controller, call us today.

ETI
MICRO

6918 SIERRA COURT, DUBLIN, CA 94568

(415) 829-6600

MULTIBUS is a trademark of Intel Corporation

Schmitt trigger optocouplers

Infrared optocouplers with Schmitt trigger output for coupling digital logic circuits eliminate need for comparators or other offchip wave shape circuitry. The series of 5 gallium arsenide couplers guarantees switching time suitable for high speed logic interface. Couplers provide high common noise immunity, restore the distorted bit stream to its original form, and pass the bit stream data from microprocessor to TTL with negligible distortion and delay. Packaged in a std 6-pin plastic DIP, price range is \$1.55 to \$3.30. **Motorola Semiconductor Products Inc.**, PO Box 20912, Phoenix, AZ 85036.

Circle 276

12-bit DAC guarantees 900-ns settling time

AD7420 12-bit CMOS DAC has 900-ns voltage settling time max to $\pm 0.01\%$. The DAC eliminates need for trim potentiometers with guaranteed total unadjusted error of $\frac{1}{2}$ and -1 LSB max. Power dissipation is 30 mW max. The DAC's current steering mode operates with an ac reference to give multiplying DAC performance. Output capacitance/resistance are code independent. Chip operates with a fixed positive reference voltage and requires a single op amp to develop bipolar output voltages from its $10k-\Omega$ output impedance. Three 18-pin DIPs in 3 temp ranges with guaranteed monotonicity are available. Prices range from \$9.90 to \$44.80. **Analog Devices, Inc.**, Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062.

Circle 277

YOU WON'T BELIEVE YOUR EYES!



Introducing the Kratos KM1400 high-resolution color video display:

1024 lines, non-interlaced.

60 Hz refresh (64 kHz horizontal scan rate).

100 MHz video bandwidth.

For more information on the color video display with the highest resolution available today, call or write: KRATOS Display Systems • 101 Cooper Court • Los Gatos, CA 95030 • (408) 395-3700
TELEX 171946

KRATOS

Display
Systems

© 1982 KRATOS Display Systems

CIRCLE 141



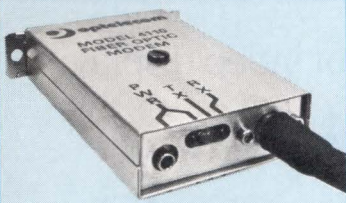
Direct Plug-in Full Duplex Fiber Optic Modem

- DC to 100Kbaud Asynchronous
- RS-232-C or MIL-STD-188-C
- DTE and DCE Versions
- Field Installable
- Up to 1Km Range
- AC or DC Power Options
- Tx Data, Rx Data, PWR ON LED Indicators

One pair of OPTELECOM's Model 4110 modems permit 100Kbaud full duplex communication between distributed terminals, peripherals, or telephone modems, and CPUs or communication controllers over spans to 1Km. They require NO field termination kits, NO interconnecting EIA cables, and NO rack or desk top space.

These modems use standard fiber optic cables which can be pre-installed in existing cable trays, ducts, or air plenums. Since these cables are immune to electro-magnetic interference, they can penetrate screen rooms, pass through manufacturing areas, or run between locations of varying ground potential; ALL without line conditioning, shielding, or filtering.

Save time, money, and your data processing system with the OPTELECOM Model 4110 and associated cables.



optelecom
The Optical Communications Company

15940 Luanne Dr. Gaithersburg, MD 20877
(301) 948-4232

CIRCLE 142

Bus arbitration module

A bipolar asynchronous bus controller, the MC68452 multiplexes local microprocessor buses onto a common global bus, allowing the local buses to share memory, I/O devices, and communications. A single module provides arbitration for up to 8 bus masters and can be expanded indefinitely to support more masters. The central arbitration function utilizes a separate request-grant pair for each user. Each module circuit has 8 data bus request and data bus grant pairs. Samples are available now for \$25 in quantities of 100. **Motorola Inc, MOS Microprocessor Div**, 3501 Ed Bluestein Blvd, Austin, TX 78721.

Circle 278

CMOS macrocell arrays

LL3000 series of Sigate CMOS arrays includes 10 devices with complexities ranging from 272 to 2550 gates, and pin counts ranging from 36 to 104. The 3.5-micron arrays use single-level metal interconnection. Nominal delays are 6 to 8 ns through a 2-input NAND gate. The series is fully supported by the company's logic development system (LDS) and an extensive library of macrocells and macrofunctions. All array pads are completely bidirectional and can be configured as input, output, or bidirectional lines. Lines can be TTL or CMOS compatible, and are protected from static discharge. **LSI Logic Corp**, 1601 McCarthy Blvd, Milpitas, CA 95035.

Circle 279

64k static RAM

HM6264 8k x 8 static RAM has 100-, 120-, and 150-ns access times and a JEDEC 28-pin package that is pinout compatible with std 64k EPROMs. HI-CMOS technology provides high speed, high density, and low power consumption. The VLSI device includes a single 5-V power supply, 10- μ W standby and 200-mW operating power, 3-state output, and full TTL compatibility. **Hitachi America, Ltd**, 1800 Bering Dr, San Jose, CA 95112.

Circle 280

Talk to the editor

Have you written to the editor lately? We're waiting to hear from you.

Fast access 8k PROMs

93Z451 junction fuse TTL compatible 8192-bit bipolar PROM, organized as 1024 x 8, provides max commercial access time of 40 ns and mil access time of 55 ns. The 93Z451A grade features 35-ns commercial and 45-ns mil access times. With max supply current of 135 mA, the chip claims the lowest power dissipation for any high speed PROM. The vertical NPN transistor is programmed via a self-adjusting current ramp. Programming yields are typ 98%.

Fairchild Camera and Instrument Corp, 441 Whisman Rd, Mountain View, CA 94039.

Circle 281

CMOS ADC with onchip sample and hold

Featuring a built-in sample and hold function, MSM5204RS CMOS 8-bit ADC enables direct input of analog signals. The device has a latched 3-state output register that facilitates use in bus oriented systems. Typ conversion time is 66 μ s at a 500-kHz clock rate; faster operation can be achieved at higher clock rates. Device provides $\pm 1/2$ LSB accuracy and employs a successive capacitor ladder conversion system. Typ power consumption is 4.5 mW. In an 18-pin plastic DIP, price is \$4.10 each. **OKI Semiconductor**, 1333 Lawrence Expy, Santa Clara, CA 95051.

Circle 282

RAM integrates refresh and arbitration functions

Family of integrated RAMs (iRAMs) initially includes the 2186 8k x 8-bit device that integrates refresh and arbitration. The low cost (\$19.95) static RAM is suited for microprocessor memory applications. Produced in a std 28-pin package, 2186 based designs are functionally compatible with Intel's EPROMs. All normal dynamic memory refresh functions are performed internally, and onchip async refresh arbitration is provided. Max access time is 300 ns; cycle time is 500 ns. Max active current requirement is 70 mA, and standby current requirement is 20 mA. **Intel Corp**, 3065 Bowers Ave, Santa Clara, CA 95051.

Circle 283

LOW COST MULTIPLEXING AND NETWORK MANAGEMENT

WITH M/A-COM DCC'S ADVANCED STAT AND SWITCHING MUXES

M/A-COM DCC's ACM9100 Advanced Statistical Mux and ASM9200 Advanced Switching Mux extend the capabilities of your data network while reducing your communications costs.

NEW NETWORK CONTROL PORT

Now you can manage your network more effectively:

- Performance statistics for network evaluation and optimization
- Status of multiplexers and port configurations
- Diagnostic loopbacks, interface status, and link performance
- Any async port can be a password-protected Network Control Port

MORE STANDARD FEATURES

New "no cost" standard features include:

- User selectable bisync and async inputs up to 9.6 Kbps
- Extensive 32-Kbyte data buffer
- Enhanced flow control

FOR YOUR SWITCHING REQUIREMENTS

Maximize your data network flexibility with ASM9200 port selection, port contention, and data PBX features, plus:

- Switchable bisync and async connections
- Individual user connection to any async port
- Central supervisory control of total network configurations
- Status of switched port connections

PLUS INTEGRAL MODEMS

ACM9100 and ASM9200 models are also available with CCITT high-performance 9.6 Kbps and 4.8 Kbps integral modems featuring automatic speed fallback and return.

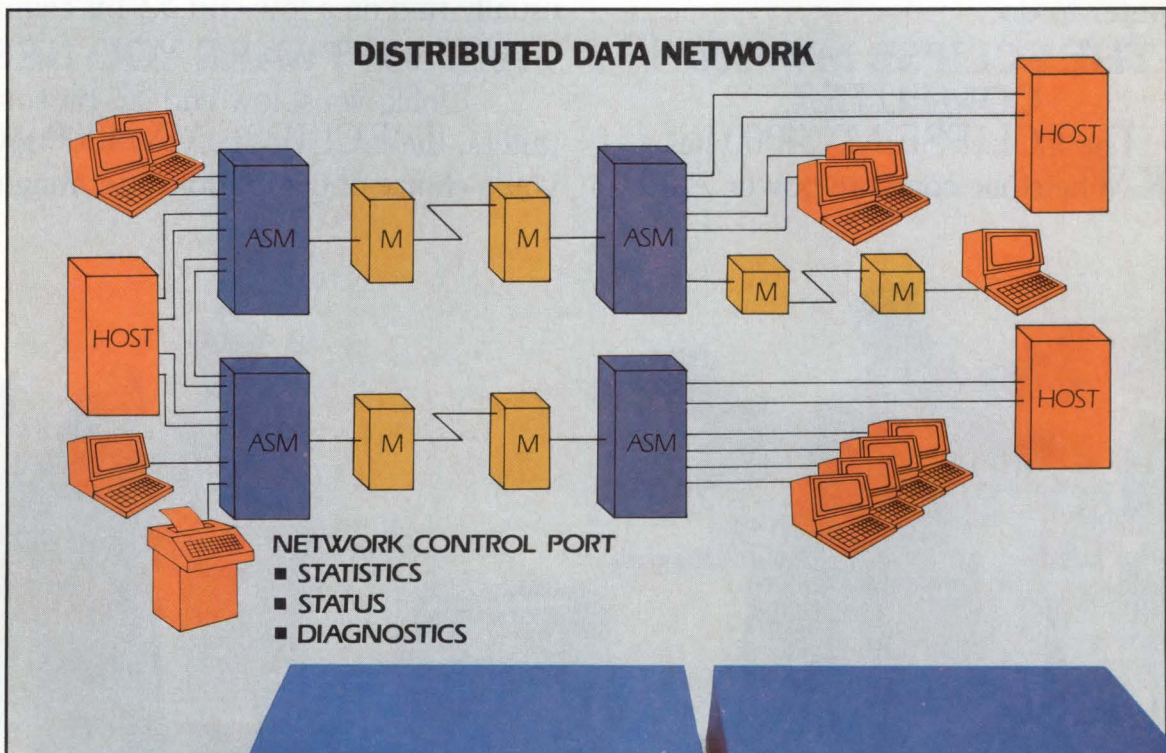
CONTACT US NOW

Call or write the Data Communications Group. M/A-COM DCC, Inc., 11717 Exploration Lane, Germantown, MD 20874-2799, (301) 428-5600, TWX 710-828-0541.

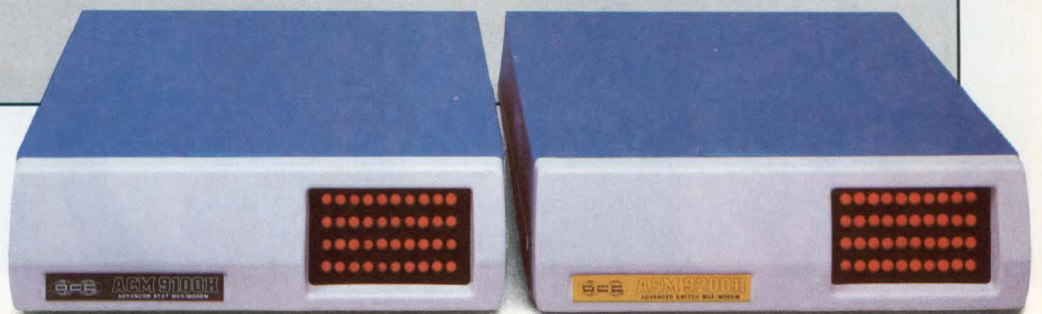


M/A-COM DCC, INC.

Leading the Way in Data Communications Technology



**NEW
FROM
M/A-COM DCC**



THE ONLY LITTLE 32-BIT COMPUTER EVEN WORTH DISCUSSING.

The problem with most low end 32-bit computers is that their usefulness is right down there with their price.

So we've come out with a low end 32-bit computer that has up to twice the performance and twice the memory of comparable machines.

Which means it can actually do the kinds of things you want a 32-bit computer to do.

THE ECLIPSE MV/4000™ COMPUTER.

The ECLIPSE MV/4000 has 600K-Whetstone compute power. And an

I/O bandwidth of 5 megabytes per second.

And to make that performance easy to perform with, the ECLIPSE MV/4000 has virtual addressability, 16 KB of user microcode space, nine I/O slots, and a rack-mountable OEM chassis version. As well as the ability to handle up to 8MB of memory, 4.7 Gigabytes of on-line storage and 64 terminals. All of which you don't usually find on a low end 32-bit computer.

THE SOFTWARE YOU NEED.

Unlike most low end 32-bit computers, the ECLIPSE MV/4000 gives you a choice of compatible operating sys-



tems: AOS/VS (our interactive advanced operating system with virtual storage). Or AOS/RT 32 (our lean, deterministic, real-time operating system). Plus a wide variety of industry and international standard communication protocols. As well as our XODIAC™ network management system, SNA, CEO™ (office automation) and data base management software. And an array of commercial and technical languages, productivity tools, and third party software packages.

THE COMPATIBILITY YOU EXPECT.

Should you one day need even more of a computer, you can take all your code (and all your peripherals) onto the bigger members of the ECLIPSE family. Because the ECLIPSE MV/4000 is fully compatible with the entire Data General ECLIPSE MV product line.

600K-Whetstone	✓
8MB Maximum memory	✓
5MB/sec I/O	✓
Virtual addressability	✓
Real-time operating system	✓
4.7 Gigabytes of On-Line Storage	✓
Multiple I/O slots	✓
User microcode space	✓
Low Price	✓

Should you find yourself staying with the ECLIPSE MV/4000 system, you'll find it stays with you. Partly because of our worldwide network of field service engineers. And partly because of some inherently reliable design considerations. Like extensive self diagnostics on power up. The simple, two board implementation. And the 55°C burn-in test it goes through. In fact, we're offering an uptime guarantee of 96 to 99%. And a remote diagnostic program.

The way we see it, making a little 32-bit computer is no excuse for making any less of a computer.

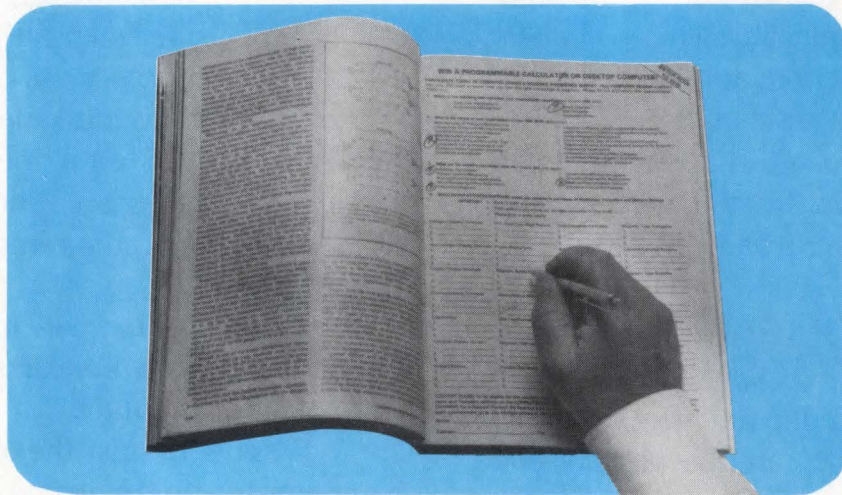
Want to discuss the only little 32-bit computer worth discussing? Call your local Data General office. Or write us TPD, F134, 4400 Computer Drive, Westboro, MA 01580.

Data General



Take a Few Minutes to HELP OUR EDITORS HELP YOU

YOU MAY WIN A VALUABLE PRIZE IN THE PROCESS

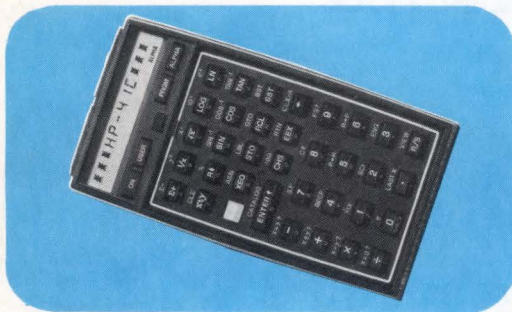


In every issue of *Computer Design* you'll find a bound-in survey questionnaire entitled "Designer Preference Survey." Your participation in these surveys is important. Your answers are significant. They tell our editors what's going on in the marketplace, what kinds of systems you are designing, how your product choices are shaping up, what products, subsystems, equipment and components you are using or would like to use.

The answers you supply can guide our editors in selecting the topics, features, and technical data that will be on target with the kinds of projects you are working on.

The questionnaires also alert manufacturers to your needs. The inputs you give us help them to develop products with the speeds, ranges, capacities, etc. that you require.

As an added incentive, each questionnaire returned gives you a chance to win a valuable prize. Drawings are made each month, with a grand prize drawing at year end.



MONTHLY DRAWING
HP 41C
PROGRAMMABLE CALCULATOR

The HP 41C offers advanced problem-solving power yet is easy to use. Communicates in words as well as numbers. Can be programmed to meet your specific needs. Fifty-eight popular functions, 130 total operations in function library. You can add peripherals and extension modules to expand capabilities.



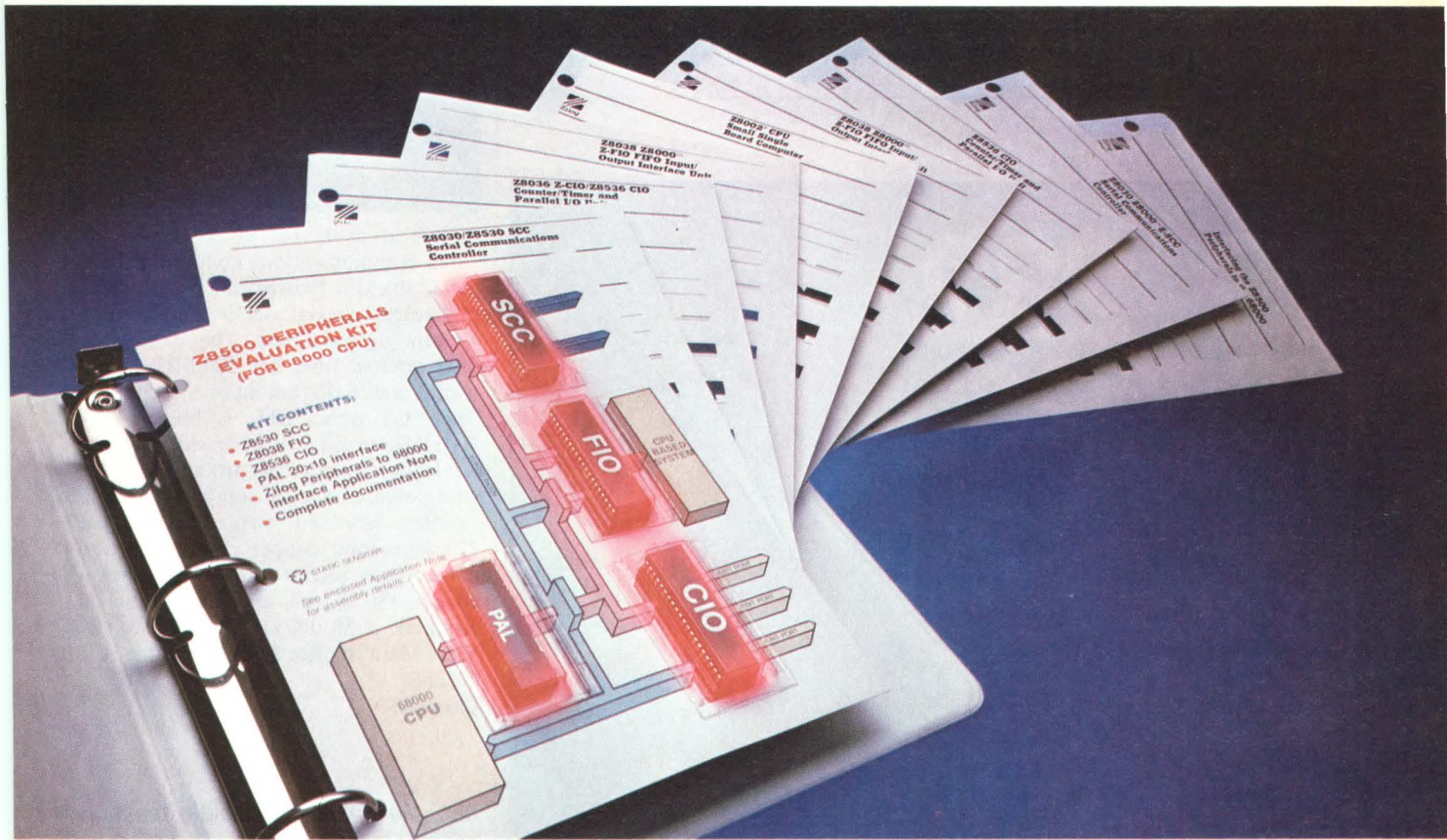
ANNUAL DRAWING
HP 85
DESK TOP COMPUTER

This portable (20#) unit includes an alphanumeric keyboard, tape drive, thermal printer, built-in 56 K byte memory, CRT screen, and 150 built-in HP BASIC language commands. You can add peripherals and software packages to expand system capability. A \$2800 value!

COMPUTER DESIGN

The only computer magazine that concentrates on design.
The only design magazine that concentrates on computers.

Invest \$129.95 in Zilog's Peripherals Kit and get what you paid for out of the 68000.



So, you picked the 68000 for your new design only to discover the manufacturer doesn't offer all the peripherals you need to back it up. What now? Order Zilog's handy new Z8500 Peripherals Evaluation Kit today to help bring your designs to reality. Only Zilog has the peripherals and foresight to develop this unique kit. And only Zilog can make you this special offer.

You get the most advanced peripheral chips available to enhance the performance of your 68000 CPU in addition to interface applications notes and complete documentation—all for \$129.95!

Zilog peripherals feature

68000-compatible interrupts and software programmable operating modes to increase system performance and flexibility. All you supply is the 68000. You get faster answers, too. Follow the kit's easy instructions, and you can have results in a matter of hours, not weeks.

The Z8500 Peripherals Evaluation Kit. The peripherals you need for the 68000 that you can't get from the manufacturer. Kits are in stock at all Zilog distributors. For the phone number of the distributor nearest you, or for additional free information on the Z8500 peripherals call Zilog TOLL FREE (800) 272-6560.

Z8530 SCC

- One Megabit/second data transfer rate
- Two full-duplex channels
- Asynchronous and synchronous data communications modes

Z8038 FIO

- 128-byte asynch bidirectional FIFO buffer
- Mailbox registers
- Pattern recognition logic

Z8536 CIO

- Three I/O ports
- Four handshake modes
- Three independent 16-bit counter/timers

Zilog

Pioneering the Microworld.

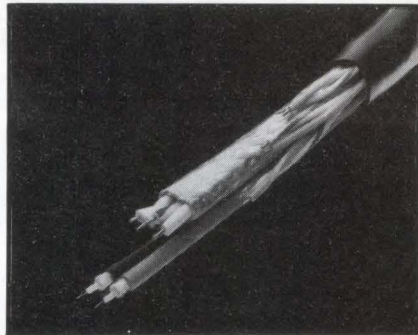
An affiliate of **EXXON** Corporation

Mini flex cable connector

The 7583-CN 0.1" (0.3-cm) center flat flex cable connector has an envelope size of 0.15" x 0.26" (0.38 x 0.66 cm). It terminates membrane switch tails and other high impedance circuitry to PCBs. With the connector's dual-beam terminal design, contact can be made on either

side of the mylar tails. Housing is 94V-0 polyester with standoff base. Terminals are tinplated copper alloy. Circuit sizes are 5 to 21, in straight and right angle versions. Low insertion/withdrawal force allows 10 mating cycles. Current rating is 1 A. **Molex Inc.**, 2222 Wellington Ct, Lisle, IL 60532. **Circle 284**

Hybrid cable



A hybrid cable for voice, data, and video communications contains twisted pairs, shielded twisted pairs or shielded miniature coaxial cable, and dual-window optical fibers. The 100-micron dual-window fiber has 300-MHz bandwidth and 6-dB/km max attenuation. The fiber optic cable is buffered by Hytrel for crush resistance, shielded with Kevlar for tensile strength, and jacketed with polyurethane for nonplenum applications. Shielded twisted pairs use 22-gauge solid copper conductors and handle data rates to 16M bps. Impedance is 150 Ω /pair, and attenuation on crosstalk is 58 dB/km. **Brand-Rex Co.**, West Main St, Rte 32, Willimantic, CT 06226.

Circle 285

RS-232 USERS

The cost effective 75 ips TDX provides a simple solution to your tape system requirements! Just plug it in any RS-232 compatible device—

- Transmit data via modems and telephone lines, even tape to tape
- Communicate at standard baud rates up to 46K baud
- Use synchronous / asynchronous / isosynchronous protocols
- Ping-pong 2K buffers or up to 4K records standard
- Automatic error detection and correction standard
- Remote programmable control standard
- Serial data interface for input/output and control standard
- IBM bi-synchronous protocol supported up to 56K baud

Call us now for complete details!

TDX PERIPHERALS

Division of **GAW**
Control Corp.
148 New York Avenue
Halesite, NY 11743
(516) 423-3232



DEC, MULTIBUS compatible mass storage and backplane modules

StacPac individually packaged mass storage modules have their own power supply and can stand alone as an add-on memory system. The modules can also be stacked together as a system by adding CPU, I/O, and memory boards to the StacPac backplane module. Available in either DEC or MULTIBUS compatible versions, the modules have an interlocking design that prevents tipping. Individually packaged units include slimline floppy module, tape module, 8" Winchester module, and processor module. **Data Systems Design, Inc.**, 2241 Lundy Ave, San Jose, CA 95131.

Circle 286

Get your own

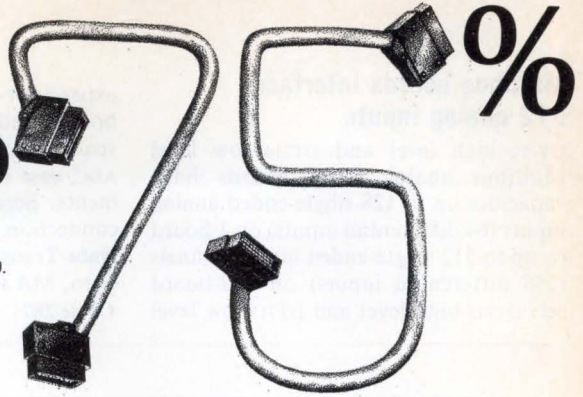
If you're reading someone else's copy of Computer Design, why not get your own? To receive a subscription application form, circle 504 on the Reader Inquiry Card.

Cut your cable costs up to 75%

Connect yourself with Digital right now and save up to 75% in our mid-winter sale. On just about every cable we offer. All brand new. And fully warranted.

To order, simply call toll-free 800-258-1710. In New Hampshire, Alaska and Hawaii, call 603-884-6660. But call now, supplies are limited. Offer ends April 3.

All orders must be placed through Digital's Accessories and Supplies Group. Standard A&S/G terms and conditions apply. Prices are net. You must agree to immediate delivery. Minimum order \$35, unless charged to MasterCard or VISA. Digital reserves the right to limit order quantities. Maximum order by phone \$5,000. Larger orders must be accompanied by purchase order and mailed to: Digital Equipment Corporation, P.O. Box CS2008, Nashua, NH, 03061.



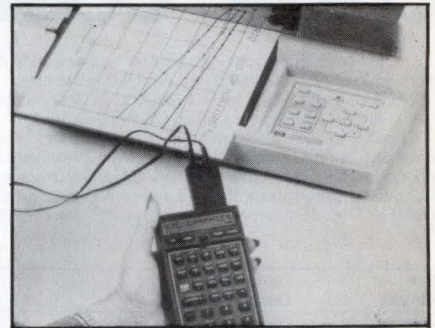
Part Number	Description	Regular Price	Sale Price**	% Off	Part Number	Description	Regular Price	Sale Price**	% Off
BC01V-25/BF	Cable Assy DP8-EA 25 FT	\$126.	\$82.	34	4A-L0T-CB-AA/BF	Lot of 5, BC01V-25 (25' Cable)	540.	375.	30
BC02M-25/BF	WO21-WO22 Ribbon, 25FT	150.	39.	74	4A-L0T-CB-AB/BF	Lot of 10, BC01V-25 (25' Cable)	899.	695.	22
BC02S-05/BF	Cable, WO23-WO23 TU55 5FT	180.	45.	75	4A-L0T-CB-AG/BF	Lot of 5, BC03M-A0 (100' Cable)	1,116.	425.	31
BC03L-05/BF	EIA Cable, H856 TO RS232C MAL	250.	110.	56	4A-L0T-CB-AH/BF	Lot of 10, BC03M-A0 (100' Cable)	1,116.	750.	33
BC03M-A0/BF	10' Null Modem Ext Cable	140.	95.	34	4A-L0T-CB-AT/BF	Lot of 25, BC03M-A0 (100' Cable)	2,748.	1,895.	38
BC03N-A0/BF	Coax Cable 100 Foot	140.	80.	42	4A-L0T-CB-AK/BF	Lot of 50, BC03M-A0 (100' Cable)	4,997.	3,195.	36
BC03N-A5/BF	Special Built Cable 150FT	200.	100.	50	4A-L0T-CB-AL/BF	Lot of 5, BC05C-25 (25' Cable)	543.	425.	21
BC03P-A0/BF	Null Modem, 2 Fem Ends, 100FT	150.	90.	40	4A-L0T-CB-AM/BF	Lot of 10, BC05C-25 (25' Cable)	1,015.	795.	21
BC04R-10/BF	Special Built Cable 10FT	32.	22.	31	4A-L0T-CB-AN/BF	Lot of 25, BC05C-25 (25' Cable)	2,363.	1,895.	19
BC04R-12/BF	Mate-N-Lok to 4 Rings, 12FT	140.	34.	24	4A-L0T-CB-AP/BF	Lot of 25, BC05C-25 (25' Cable)	4,375.	3,595.	17
BC04R-A0/BF	Special Cable 100FT	100.	70.	30	4A-L0T-CB-BQ/BF	Lot of 5, BC05D-25 (25' Cable)	648.	475.	26
BC04R-B0/BF	Mate-N-Lok to 4 Rings, 200'	200.	130.	35	4A-L0T-CB-BD/BF	Lot of 10, BC05D-25 (25' Cable)	1,197.	895.	25
BC04Z-01/BF	H856, 40 Conductor Flat (1')	48.	26.	45	4A-L0T-CB-BE/BF	Lot of 25, BC05D-25 (25' Cable)	2,742.	2,175.	20
BC04Z-00/BF	H856, 40 Conductor Flat (6')	50.	30.	40	4A-L0T-CB-BF/BF	Lot of 50, BC05D-25 (25' Cable)	5,152.	3,950.	23
BC04Z-10/BF	H856, 40 Conductor Flat (10')	52.	35.	32	4A-L0T-CB-BG/BF	Lot of 5, BC05D-50 (50' Cable)	895.	525.	24
BC04Z-15/BF	H856, 40 Conductor Flat (15')	80.	40.	50	4A-L0T-CB-BH/BF	Lot of 10, BC05D-50 (50' Cable)	1,318.	995.	24
BC04Z-25/BF	H856, 40 Conductor Flat (25')	90.	45.	50	4A-L0T-CB-BJ/BF	Lot of 25, BC05D-50 (50' Cable)	3,115.	2,375.	23
BC05C-09/BF	Cable Modem 9FT	112.	80.	28	4A-L0T-CB-BK/BF	Lot of 50, BC05D-50 (50' Cable)	5,750.	4,495.	21
BC05C-25/BF	BC05C-25 Cable Modem	120.	90.	25	4A-L0T-CB-CL/BF	Lot of 5, BC11A-02 (2' Cable)	626.	435.	30
BC05D-15/BF	RS232 Male-Fem, 25 Cond, 15FT	125.	90.	28	4A-L0T-CB-CM/BF	Lot of 10, BC11A-02 (2' Cable)	1,186.	950.	20
BC05D-20/BF	RS232 Male-Fem, 25 Cond, 20FT	130.	95.	26	4A-L0T-CB-CN/BF	Lot of 25, BC11A-02 (2' Cable)	2,800.	1,995.	28
BC05D-25/BF	RS232 Male-Fem, RS232 Fem 25'	140.	100.	28	4A-L0T-CB-CP/BF	Lot of 50, BC11A-02 (2' Cable)	5,272.	3,895.	26
BC05D-50/BF	RS232 Male to Female, 50FT	150.	110.	26	4A-L0T-CB-CQ/BF	Lot of 5, BC11A-10 (10' Cable)	846.	625.	26
BC05D-75/BF	RS232 Male-Fem, 25 Cond, 75FT	225.	160.	28	4A-L0T-CB-CR/BF	Lot of 10, BC11A-10 (10' Cable)	1,603.	1,200.	25
BC05F-A0/BF	Cable Interface LA305	150.	75.	50	4A-L0T-CB-CS/BF	Lot of 50, BC11A-10 (10' Cable)	2,928.	2,785.	22
BC05J-06/BF	Line Cord Set 240 V 6 FT	100.	65.	35	4A-L0T-CB-CT/BF	Lot of 50, BC11A-10 (10' Cable)	7,125.	5,595.	21
BC05L-15/BF	H856 TO H856 Flat Reverse 15	80.	40.	50	4A-L0T-CB-CU/BF	Lot of 5, BC11A-15 (15' Cable)	996.	775.	22
BC05M-04/BF	Cable H856 to Mat-N-Lok 4'	42.	20.	52	4A-L0T-CB-CV/BF	Lot of 10, BC11A-15 (15' Cable)	1,886.	1,495.	20
BC05M-20/BF	Special Cable 20FT	62.	40.	35	4A-L0T-CB-CW/BF	Lot of 25, BC11A-15 (15' Cable)	4,454.	3,650.	18
BC05M-25/BF	Cable H856 to Mat-N-Lock 25'	150.	75.	50	4A-L0T-CB-CX/BF	Lot of 5, BC11A-15 (15' Cable)	8,384.	6,995.	16
BC05M-50/BF	Cable H856 to M-N-Lock 50'	90.	60.	33	4A-L0T-CB-CY/BF	Lot of 5, BC22A-10 (10' Cable)	228.	140.	38
BC05W-10/BF	50 Conductor Signal Cable 10'	85.	45.	47	4A-L0T-CB-DZ/BF	Lot of 10, BC22A-10 (10' Cable)	436.	260.	40
BC05W-25/BF	50 Conductor Signal Cable 25'	160.	85.	46	4A-L0T-CB-DA/BF	Lot of 25, BC22A-10 (10' Cable)	1,038.	600.	42
BC06F-25/BF	M908 TO Compstar 191, 25 FT	425.	225.	47	4A-L0T-CB-DB/BF	Lot of 50, BC22A-10 (10' Cable)	5,925.	4,095.	31
BC06K-10/BF	H885-H885, Mirror Conn, 10 FT	50.	50.	0	4A-L0T-CB-DC/BF	Lot of 5, BC22A-25 (25' Cable)	1,186.	190.	27
BC06S-25/BF	Round Massbus Cable, 25 FT	1,040.	425.	59	4A-L0T-CB-DD/BF	Lot of 10, BC22A-25 (25' Cable)	498.	360.	27
BC07A-10/BF	Cable H856 1-End 20 TW PR 10'	130.	70.	46	4A-L0T-CB-DE/BF	Lot of 25, BC22A-25 (25' Cable)	1,181.	850.	28
BC07A-25/BF	Cable H856 1-End 20 TW PR 25'	154.	120.	22	4A-L0T-CB-DF/BF	Lot of 50, BC22A-25 (25' Cable)	2,235.	1,495.	33
BC07B-25/BF	Cable H856 1-End 11 TW PR 25'	90.	50.	44	4A-L0T-CB-DG/BF	Lot of 10, BC22B-25 (25' Cable)	2,237.	145.	27
BC07D-15/BF	H856 2-2 COND Ribbons 15'	140.	85.	39	4A-L0T-CB-DH/BF	Lot of 10, BC22B-25 (25' Cable)	487.	270.	44
BC07D-25/BF	H856 2-2 COND Ribbons 25'	160.	100.	37	4A-L0T-CB-DI/BF	Lot of 25, BC22B-10 (10' Cable)	1,151.	650.	43
BC08A-02/BF	M903 to M903 Dual Mylar 2'	150.	40.	73	4A-L0T-CB-DJ/BF	Lot of 50, BC22B-10 (10' Cable)	2,166.	1,150.	46
BC08A-05/BF	M903 to M903 Dual Mylar 5'	200.	50.	75	4A-L0T-CB-DK/BF	Lot of 5, BC22B-25 (25' Cable)	307.	195.	36
BC08A-07/BF	M903 to M903 Dual Mylar 7'	220.	55.	75	4A-L0T-CB-DL/BF	Lot of 10, BC22B-25 (25' Cable)	580.	367.	37
BC08A-09/BF	M903 to M903 1.25 Mylar (9')	235.	65.	72	4A-L0T-CB-DM/BF	Lot of 10, BC22B-25 (25' Cable)	1,067.	900.	34
BC08A-10/BF	M903 to M903 Dual Mylar 10'	250.	65.	74	4A-L0T-CB-DN/BF	Lot of 50, BC22B-25 (25' Cable)	2,568.	1,650.	35
BC08A-15/BF	Cable, BC08A	300.	75.	75	4A-L0T-CB-DO/BF	Lot of 5, BC04R-12 (12' Cable)	161.	110.	31
BC08A-25/BF	M903 to M903 Dual Mylar 25'	350.	90.	74	4A-L0T-CB-DP/BF	Lot of 10, BC04R-12 (12' Cable)	307.	199.	35
BC08F-08/BF	Cable Module	300.	100.	66	4A-L0T-CB-DQ/BF	Lot of 5, BC04Z-10 (10' Cable)	155.	245.	32
BC08F-06/BF	H856 to M953 40 CND 3M 6'	300.	130.	57	4A-L0T-CB-DR/BF	Lot of 6, BC04Z-10 (10' Cable)	662.	299.	33
BC08J-10/BF	H856 to M953 40 CND 3M 10'	180.	90.	50	4A-L0T-CB-DS/BF	Lot of 5, BC04Z-25 (25' Cable)	419.	215.	48
BC08J-15/BF	H856 to M953 40 CND 3M 15'	210.	100.	53	4A-L0T-CB-DT/BF	Lot of 10, BC04Z-25 (25' Cable)	777.	410.	47
BC08J-25/BF	H856 to M953 40 CND 3M 25'	250.	110.	56	4A-L0T-CB-DU/BF	Lot of 5, BC05F-A0 (Cable In)	915.	350.	61
BC08J-50/BF	Cable IO PDP8E	300.	135.	55	4A-L0T-CB-DV/BF	Lot of 10, BC05F-A0 (Cable In)	1,708.	650.	61
BC08K-00/BF	H856 to M955 40 CND 3M 6'	100.	60.	40	4A-L0T-CB-DW/BF	Lot of 5, BC05M-04 (4' Cable)	200.	95.	52
BC08K-15/BF	H856 to M955 40 CND 3M 15'	300.	125.	58	4A-L0T-CB-EA/BF	Lot of 10, BC05M-04 (4' Cable)	378.	175.	53
BC08M-0M/BF	H807 to H807 Mylar 11"	250.	120.	52	4A-L0T-CB-EB/BF	Lot of 5, BC06S-25 (25' Cable)	4,875.	1,995.	59
BC08R-08/BF	H856-H856 3M REV 8'	68.	35.	48	4A-L0T-CB-EC/BF	Lot of 10, BC06S-25 (25' Cable)	9,176.	3,750.	59
BC08R-20/BF	H856-H856 3M Cable (20')	80.	55.	50	4A-L0T-CB-ED/BF	Lot of 5, BC07A-25 (25' Cable)	571.	575.	0
BC08S-05/BF	H856-H856 3M Strap, 5 FT	60.	30.	50	4A-L0T-CB-EE/BF	Lot of 10, BC07A-25 (25' Cable)	1,128.	1,095.	2
BC08S-06/BF	H856-H856 40 Cond, Cable 6 FT	62.	32.	48	4A-L0T-CB-EF/BF	Lot of 5, BC07D-15 (15' Cable)	649.	395.	39
BC09B-07/BF	Cable M912 12FT	1,936.	800.	58	4A-L0T-CB-EG/BF	Lot of 10, BC07D-15 (15' Cable)	1,198.	775.	35
BC09B-10/BF	I/O Bus M912 Cable 10 FT	1,963.	825.	57	4A-L0T-CB-EH/BF	Lot of 5, BC07D-25 (25' Cable)	758.	495.	34
BC10S-12/BF	Bus 2 M912 to M912, XXFT	871.	200.	77	4A-L0T-CB-EI/BF	Lot of 10, BC07D-25 (25' Cable)	1,397.	950.	31
BC10K-05/BF	Cable 5 FT, Quick Latch	2,373.	1,400.	41	4A-L0T-CB-EJ/BF	Lot of 5, BC08S-06 (6' Cable)	298.	140.	53
BC10K-10/BF	10 MEM BUS Cable 10 FT	2,551.	1,500.	41	4A-L0T-CB-EK/BF	Lot of 10, BC08S-06 (6' Cable)	566.	275.	51
BC10K-15/BF	10 MEM BUS Cable, 15 FT	2,725.	1,650.	39	4A-L0T-CB-EL/BF	Lot of 5, BC11S-25 (25' Cable)	647.	425.	34
BC10K-25/BF	PDP 10 MEM BUS Cable	3,073.	1,875.	38	4A-L0T-CB-EM/BF	Lot of 10, BC11S-25 (25' Cable)	1,204.	795.	33
BC10K-35/BF	PDP 10 MEM BUS Cable	3,443.	2,100.	39	4A-L0T-CB-EN/BF	Lot of 5, BC11S-50 (50' Cable)	811.	595.	26
BC10L-35/BF	AMP Quick Latch to (5) W021 Cable	2,750.	800.	70	4A-L0T-CB-EO/BF	Lot of 10, BC11S-50 (50' Cable)	1,510.	1,095.	27
BC11A-02/BF	External Unibus 2'	135.	90.	33	4A-L0T-CB-EP/BF	Lot of 5, BC11S-A0 (100' Cable)	1,297.	925.	28
BC11A-05/BF	External Unibus 5'	155.	100.	29	4A-L0T-CB-EQ/BF	Lot of 10, BC11S-A0 (100' Cable)	2,415.	1,795.	25
BC11A-08/BF	External Unibus 8'	160.	115.	29	4A-L0T-CB-ER/BF	Lot of 5, 70-11212-25 (Cable)	900.	475.	47
BC11A-09/BF	External Unibus 9'	170.	125.	26	4A-L0T-CB-ES/BF	Lot of 10, 70-11212-25 (Cable)	1,626.	895.	44
BC11A-10/BF	External Unibus 10'	182.	130.	28	4A-L0T-CB-ET/BF	Lot of 5, 70-11212-50 (Cable)	1,134.	625.	44
BC11A-15/BF	External Unibus 15'	210.	160.	23	4A-L0T-CB-EU/BF	Lot of 10, 70-11212-50 (Cable)	2,130.	1,195.	43
BC11A-17/BF	Special Cable 17FT	215.	170.	20	4A-L0T-CB-EV/BF	Lot of 5, BC10K-05 (5' Cable)	11,076.	6,750.	39
BC11A-20/BF	External Unibus 20'	220.	175.	20	4A-L0T-CB-EW/BF	Lot of 10, BC10K-05 (5' Cable)	20,570.	12,750.	38
BC11A-25/BF	External Unibus 25'	230.	180.	21	4A-L0T-CB-EY/BF	Lot of 25, BC10K-05 (5' Cable)	46,150.	28,875.	35
BC11A-35/BF	External Unibus 35'	400.	300.	25	4A-L0T-CB-EZ/BF	Lot of 5, BC10K-10 (10' Cable)	11,905.	7,250.	39
BC11A-50/BF	External Unibus 50'	450.	350.	22	4A-L0T-CB-FA/BF	Lot of 10, BC10K-10 (10' Cable)	22,109.	13,995.	36
BC11K-25/BF	H856 1 End 20 Pair 25'	180.	90.	50	4A-L0T-CB-FB/BF	Lot of 25, BC10K-10 (10' Cable)	49,604.	33,125.	33
BC11S-25/BF	H856 TO H856 18 TW PR 25'	138.	90.	34	4A-L0T-CB-FC/BF	Lot of 5, BC10K-25 (25' Cable)	14,365.	9,125.	36
BC11S-50/BF	H856 TO H856 18 TW PR 50'	173.	125.	27	4A-L0T-CB-FD/BF	Lot of 10, BC10K-25 (25' Cable)	26,679.	17,900.	32
BC11S-A0/BF	H856 TO H856 18 TW PR 100'	277.	190.	31	4A-L0T-CB-FE/BF	Lot of 25, BC10K-25 (25' Cable)	59,856.	39,750.	33
BC20Y-25/BF	TU58 Cable, 25 FT	120.	45.	62	4A-L0T-CB-FG/BF	Lot of 5, BC10K-35 (35' Cable)	16,066.	9,995.	37
BC20Z-25/BF	TU58 Cable, 25 FT	120.	45.	62	4A-L0T-CB-FH/BF	Lot of 10, BC10K-35 (35' Cable)	29,837.	18,950.	36
BC21S-25/BF	VK170 10 Pin Conn Cable	48.	30.	37	4A-L0T-CB-FI/BF	Cable Module PC04	100.	100.	0
BC22A-10/BF	Null Modem RS 232 C 10'	48.	30.	37	70-09562-00/BF				

Multibus boards interface 512 analog inputs

DT712 high level and DT714 low level Multibus analog input boards have capacities up to 128 single-ended analog inputs (64 differential inputs) on 1 board or up to 512 single-ended input channels (256 differential inputs) on a 2-board set. DT713 high level and DT715 low level

expander boards are also available. The boards reduce power and backplane space requirements, and with a single ADC, ease software programming requirements. Screw terminal panels facilitate connection of several user input signals. **Data Translation**, 100 Locke Dr, Marlboro, MA 01752. Circle 287

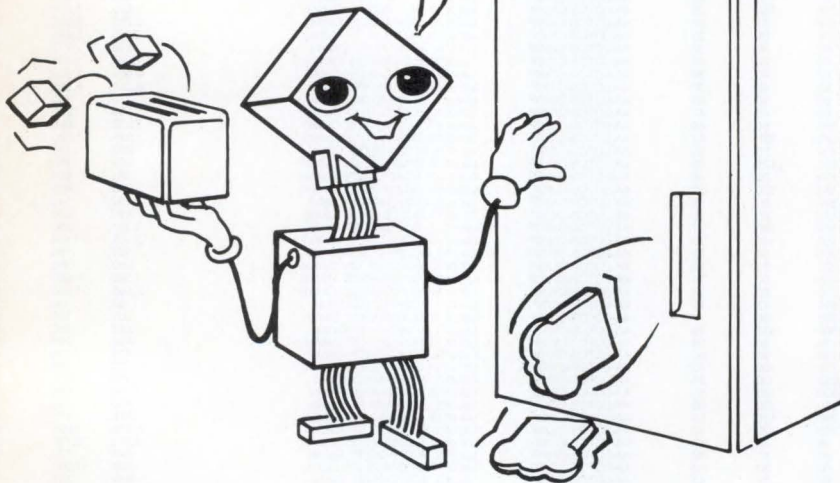
Plotter module adds graphics to HP-41 computers



HP-41 handheld computers can be linked to the HP 7470 color graphics plotter for chart, graph, and bar code plotting capabilities. The plotter module (\$75 list price) and computer connect to the graphics plotter via the HP interface loop (HP-IL). An HP-IL compatible plotter version (HP 7470 option 003) is currently available with the plotter module. Remote and benchtop data acquisition applications are accommodated. The 15-ips plotter lists at \$1575. Plotter module allows users to create HP-41 bar code on the HP 82162 thermal printer. Contact local **Hewlett-Packard** sales offices. Circle 288

Boxey Says: "We can't interface a toaster to a refrigerator...Yet."

One of our customers heard we could (*they said*) but we can't...yet.



The **BLACK BOX®** Catalog has adapters and converters to interface almost any dissimilar types of computer equipment, but we haven't solved the toaster-refrigerator problem...yet.

However, whatever you need for system installation or expansion, from data cables to protocol converters, chances are it's one of the 282* products in the **BLACK BOX®** Catalog of Data Communication Devices. It's free.

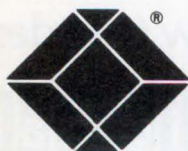
Send for your copy today!

*56 models of Data Switches, 23 types of Data Cables, Cable Parts, 14 Test Sets, 7 Modem Eliminators, 6 Line Drivers, 5 Protocol Converters, 9 Communication Adapters, 8 Printer Interfaces, 8 Terminal/Line/Modem sharing devices, Tools, etc., etc.

Phone or write:

BLACK BOX® Catalog

A MICOM COMPANY



Dept. SP • P.O. Box 12800 • Pittsburgh, PA 15241
(412) 746-2910 • TWX 510-697-3125

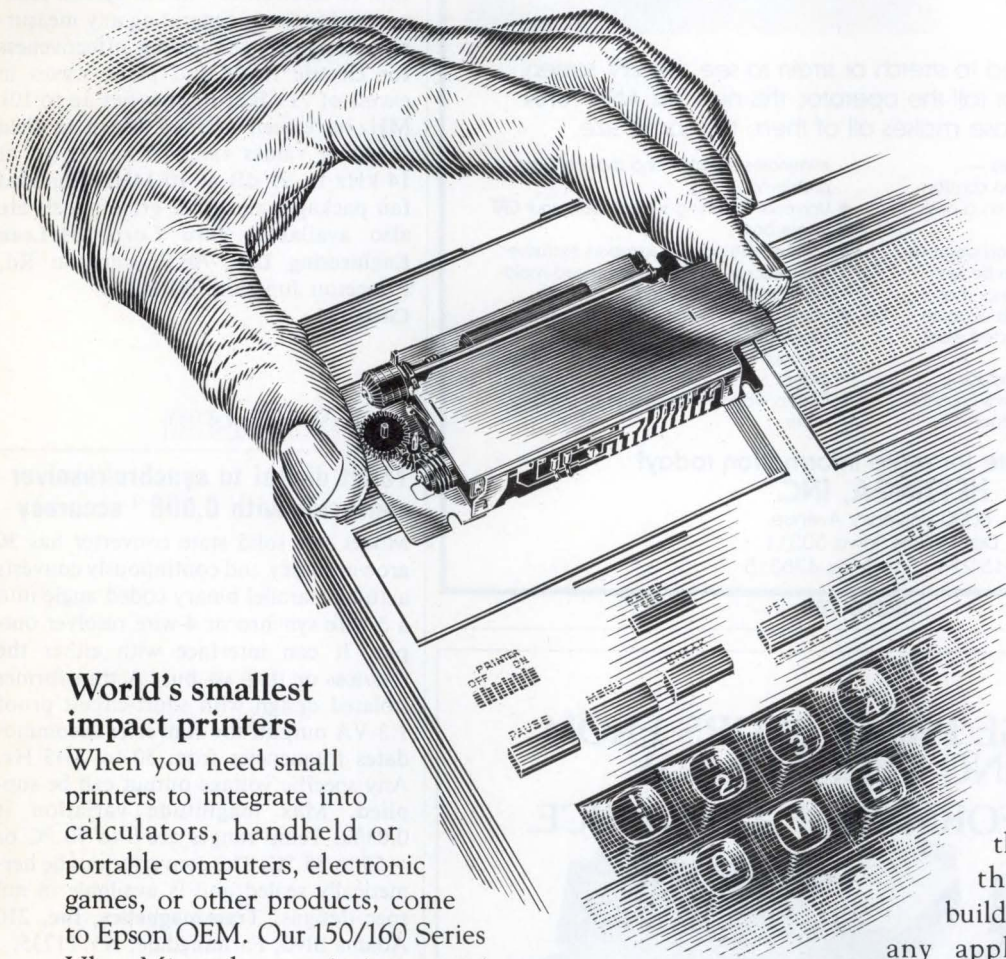
Controller for 1/2" drive compatibility with QIC hardware

C160-90A-B single-board intelligent controller makes the D160 1/2" streaming tape drive hardware/software compatible with any 1/4" tape cartridge drive using the proposed Quarter Inch Cartridge (QIC) interface standard. The controller provides an 8-bit parallel connection to the host processor and handles data separation, tape formatting, and error correction and control. It supports nonstop streaming file backup and restores at 90 ips. Any 1/4" tape cartridge with QIC interface can be configured with a 160M-byte D160 1/2" streaming device. Evaluation versions will cost approx \$600. **Rosscomp Corp**, 16643 Valley View Ave, Cerritos, CA 90701. Circle 289

Like to write?

The editors invite you to write technical articles for Computer Design. For a free copy of our Author's Guide, circle 503 on the Reader Inquiry Card.

Custom fit.



World's smallest impact printers

When you need small printers to integrate into calculators, handheld or portable computers, electronic games, or other products, come to Epson OEM. Our 150/160 Series Ultra Micro dot matrix impact print mechanisms are the world's smallest and lightest, yet each is manufactured to standards of precision that yield astonishing reliability.

More importantly, Epson OEM can supply the 150/160 Series 16 and 24-column print mechanisms in the quantities you need. They feature dot addressable graphics as well as alphanumeric printing, and can even be battery operated when necessary.

Custom made

But small printers are only part of the story. We build custom printers — with custom packaging and

**YOU'VE GOT A FRIEND
IN THE PRINTER BUSINESS.**

custom firmware — in sizes up to 136 columns. And since we build more print mechanisms than anyone else in the world, we can build printers for almost any application, custom-designed for about the same price as many off-the-shelf units. And we can build a thousand or a hundred-thousand, and deliver them... on time.

Call Epson OEM

Let us show you how we can take your specifications and give you the printers you need for any application. With a custom fit.

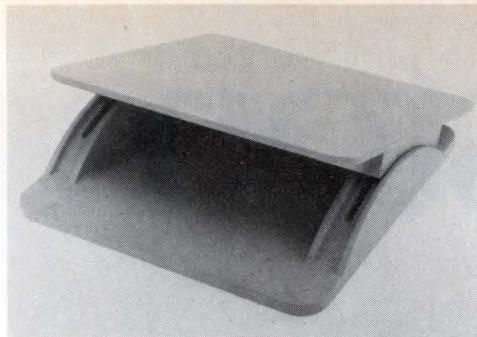


EPSON
EPSON AMERICA, INC.
OEM PRODUCTS

3415 Kashiwa Street
Torrance, California 90505
(213) 534-0360

NEW!
**The TILT AND
 TURN
 CRT base
 from HETTINGA!**

**Designed for operator
 comfort, accuracy
 and efficiency.**



There's no more need to stretch or strain to see the CRT screen. No matter how short or tall the operator, this new TILT AND TURN electronics enclosure base makes all of them the same size.

- Tilt the base up to 45 degrees — operators can view the screen comfortably whether the terminal is on a desk or countertop.
- Your cabinet will turn a full 360 degrees horizontally so the screen can be seen from anywhere in your office or shop.
- Measuring 3" x 12" x 12", this versatile base fits even the most restricted work area.
- Adaptable to all CRT units, including heavier models. This base turns on a full nine-inch weight-bearing surface that eliminates balance and maintenance problems.
- Universal fastening system locks your CRT to our base.
- Built by Hettinga Equipment's exclusive TCM process, the most advanced molding system in the world.
- You save by buying directly from the manufacturer.
- 24-hour turnaround upon receipt of your order.
- Orders welcome from one to 5000 or more.

Call or write for more information today!

HETTINGA, INC.
 8000 University Avenue
 Des Moines, Iowa 50311
 515/224-1114 Telex 478315

CIRCLE 168

**OEM IMAGE PROCESSORS FROM
 IMAGING TECHNOLOGY.
 HIGH PERFORMANCE, LOW PRICE.**



Introducing the IP-512. The first family of OEM image processing modules with high performance features available only on systems costing much, much more.

The IP-512 is a real-time image processor that's plug compatible with the INTEL MULTI-BUS and DEC Q-BUS.

It interfaces with any standard video source, stores images in single or multiple 512x512 frame buffers with up to 24 Bits/pixel and includes a pipeline ALU for real-time image averaging, summation, subtraction and convolutions.

The modules include programmable I/O Transformation Tables and provide for B&W and RGB output.

Specialized applications include image analysis, factory inspection, medical imaging, industrial radiography, robotic vision and teleconferencing, among others.

For details call, (617) 938-8444. Or write to: Imaging Technology Incorporated, 400 West Cummings Park, Suite 4350, Woburn, MA 01801.

IMAGING
 Imaging Technology, Inc.

*MULTI-BUS is a trademark of INTEL CORP
 †Q-BUS is a trademark of Digital Equipment Corp.

© 1983 IMAGING TECHNOLOGY INCORPORATED

**SYSTEM COMPONENTS/
 EMI PROTECTION**

Shielded packaged blowers

Line of 13 mil spec and 13 commercial packaged blowers counteract effects of emi while cooling electronic enclosures. Clean, filtered air is delivered up to 1k CFM to electronics without system leakage and without generating any measurable emi noise. Shielding effectiveness for electric fields and plane waves in excess of 71 dB at frequencies up to 10k MHz have been attained. Magnetic field shielding values range from 30 dB at 14 kHz to 99 dB at 10 MHz. Shielded fan packages and filter grille panels are also available. **Zero Corp, McLean Engineering Div, 70 Washington Rd, Princeton Junction, NJ 08550.**

Circle 290

DATA CONVERSION

**16-bit digital to synchro/resolver
 converter with 0.008° accuracy**

Model 1667 solid state converter has 30 arc s accuracy and continuously converts a 16-bit parallel binary coded angle into a 3-wire synchro or 4-wire resolver output. It can interface with either the 8085/8086 or IEEE 488 bus. A transformer isolated design with short-circuit proof 1.3-VA output, the converter accommodates frequencies from 50 to 2045 Hz. Any specific voltage output can be supplied. Max magnitude variation is 0.03%. Temp ranges are 0 to 70 °C or -55 to 85 °C. The converter can be hermetically sealed and is available in mil spec designs. **Transmagnetics, Inc, 210 Adams Blvd, Farmingdale, NY 11735.**

Circle 291

**Data acquisition system with
 ±40-V protection for LSI-11 bus**

Model 1023AD/EX 12-bit 35/100-kHz analog input system, upgraded to ±40-V common mode protection, is a half-quad size dual-board system. It is fully compatible with LSI-11, -11/2, -11/21, and -11/23 microcomputers. Model 1023AD provides 16 single-ended, 16 pseudo-differential, or 8 fully differential inputs. Companion model 1023EX expander module handles up to 64 single-ended, 64 pseudo-differential, or 32 fully differential inputs plus 2 optional DAC outputs. Featuring programmable gain selection, system operates under program control/interrupt with multilevel interrupt interface. **ADAC Corp, 70 Tower Office Park, Woburn, MA 01801.**

Circle 292

The challenge: conformance to VDE and international standards

The solution: Airpax IPG and SNAPAK[®] magnetic circuit breakers.

For the export market, your product must conform to international and VDE specifications. Airpax engineers designed the IPG and SNAPAK to comply with the spacing requirements of VDE 0730, IEC 380, and IEC 435 standards.

You now have the benefits of precision magnetic "stand alone" protection – with choices of handle actuation, colors, illumination, terminals, and hardware. Also, the IPG will mount in any equipment that currently uses the UPG and UPL style breakers.

HOTLINE delivery is assured for prototype requirements. Find out how we can help you meet the challenge of international standards with positive, reliable circuit switching and protection.

Specifications are in our new catalog. Write or call Airpax Corporation, a North American Philips Company, Cambridge Division, Woods Road, P.O. Box 520, Cambridge, MD 21613, telephone (301) 228-4600.

Protection for Intelligent Electronics



AIRPAX[®]

CAMBRIDGE DIVISION

Ada compiler for iAPX 86 microprocessors

Ada 86 family of computer language translators compiles the Ada language for Intel's iAPX 86 series of 16-bit microprocessors. The compiler will meet U.S. DoD standards and will be hosted on VAX minicomputers as well as on other

Intel based products. Similar introductions include Ada 432 Version 1—an Ada compiler for the iAPX 432 micromainframe computer, and iMAX—an iAPX 432 operating system written entirely in Ada. **Intel Corp.**, 3065 Bowers Ave, Santa Clara, CA 95051. **Circle 293**

Ladder diagram translator for programmable controllers

A ladder diagram translator for GE's Series Six programmable controllers automates production of the controller's program documentation. The software allows the translator system to program the GE data processor unit, a function normally provided by the GE program development terminal. The package is also available for programmable controllers from Allen-Bradley, Gould Modicon, and Texas Instruments. **XYCOM, Inc.**, 750 N Maple Rd, Saline, MI 48176. **Circle 294**



Now! Low cost digitizing with five built-in programs.

The GrafBar* sonic digitizer from Science Accessories.

You've waited for a low cost, feature-packed sonic digitizer free from the restrictions of a solid data tablet. Now your patience has been rewarded: The Science Accessories' GrafBar digitizer is here with built-in ORIGIN, LINE, METRIC, STREAM, and CANCEL programs!

A compact 19" x 6" x 1 3/4" assembly, the SAC® GrafBar digitizer incorporates two point microphones to unencumber the work area, to accommodate left or right hand digitizing, and to allow the utilization of any work surface rather than a prescribed digitizing tablet. And the 18" x 24" active area is the largest of any low cost digitizing system currently available; most other digitizers only offer 11" x 11" active areas.

Mobility and the large active area of the GrafBar microphone assembly mean interaction with a variety of images, including CRT or plasma displays, projections from x-rays or films, maps, or drawings on drafting tables.

The GrafBar sonic digitizer features built-in microprocessor conversion of slant ranges into absolute cartesian (X-Y) coordinates. Available outputs include RS-232 serial ASCII, parallel ASCII packed binary, or BCD, allowing virtually universal interfacing.

The output is selected with a jumper on the output connector. The RS-232 baud rate is selectable at 150-19,200 in eight steps.

Both stylus and cursor compatible, the GrafBar digitizer provides a built-in 115 VAC power supply, 0.01 inch/centimeter output resolution, and 100 point per second slant range digitizing rate. And the new SAC low cost digitizer offers a built-in, five-function menu which is operational in a 2" margin between the GrafBar assembly and the active area.

The SAC GrafBar sonic digitizer. At under \$ 900.00 list, it's the most compact, portable, user-oriented digitizer yet, perfect for microcomputer systems, interactive graphics, and data entry.

The whole GrafBar story is now yours for the asking. Ask. We're Science Accessories Corporation, 970 Kings Highway West, Southport, Connecticut 06490, (203) 255-1526.

*Trademark of SAC

SAC SCIENCE ACCESSORIES CORPORATION

UNIX based DBMS for 16-bit micros

Unify UNIX based relational database management system for 16-bit microcomputers incorporates pointers, hashing, and B-tree access methods to increase hardware performance. The software system requires 1.5M-byte disk storage and 100k-byte main memory. Applications can be developed without programming via integrated fully relational, nonprocedural development tools. These include interactive menu handler, command line functionality, online help features, and full-screen data entry that interfaces through an online data dictionary. Package is \$2995. **North American Technology, Inc.**, 9570 SW Barbur Blvd, Portland, OR 97219. **Circle 295**

Ethernet software

Fusion software package supports file transfer, remote program execution, and electronic mail between VAX, PDP-11, 68000, 8086, and other CPUs across a 10M-bit Ethernet LAN. Process to process data transfer rates in excess of 100k bytes/s are achieved. Versions also accommodate file transfers between UNIX, DEC VMS, IBM PC-DOS, and several other operating systems. Multiple communications protocols are also handled. Binary licenses are priced from \$500. **Network Research Corp.**, 1964 Westwood Blvd, Los Angeles, CA 90025. **Circle 296**

Let's hear from you

We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

CRYSTAL UNIFORMITY
ADVANCED BINDER
REFINED LUBRICANT
IMPROVED JACKET
INTENSIFIED CALENDERING

THE GOLD STANDARD

**You can wait for industry standards
to mandate improved performance.
Or you can have it now on Maxell.
The Gold Standard.**

What distinguishes a Maxell floppy disk? Improvements great and small, achieved in a decade of innovation. We developed unique, uniform crystals to assure dense oxide packing. Intensified the calendaring process to minimize the need for abrasive burnishing. Created an improved binder and lubricant. And a new jacket design that leaves industry standards in our wake.

It would require photomicrographs to make some of these improvements observable. On the job, the advantages become obvious. Resolution enhanced by 20% creates a cleaner

signal output. And guarantees the read/write accuracy in double-density applications. New jacket construction, heat-resistant to 140°F, extends disk use without risk of mistracking. In effect, durability is redefined. And in accelerated tests against the most respected names in the industry, Maxell sustained the highest and most consistent output over time.

We applaud industry standards that aspire to dropout-free, reliable disk performance. The Gold Standard expresses a higher aim: perfection.



maxell
IT'S WORTH IT.

Computer Products Division, Maxell Corporation of America, 60 Oxford Drive, Moonachie, N.J. 07074 201-440-8020

JOIN THE PROFESSIONALS

RTCS Products give your PC/MDOS computer, professional program development capabilities, just like Intel's Series III or System 86/330.

RTCS offers a family of Operating System Development Tools.

- **RTCS UDI**

The UDI allows your PC to execute Intel's Compilers, Assemblers and Utilities.

\$995.00

Features

Memory Management
File Management
PC/MSDOS File Structures
8087 Support

- **RTCS PC/RMX**

The RTCS PC/RMX lets your PC run under Intel's Real-Time Operating System, iRMX.

\$2250.00

Features

Up to 65536 tasks
Hierachial Directories
Multi-User Capability
Supports IBM Peripherals
Hard Disk Support
Ethernet Support

- **RTCS UDEBUG**

The RTCS UDEBUG is a powerful system debugger. 8087 support. Symbolic debugging.

\$750.00

- **RTCS PC/SBC Execution Vehicle**

The PC/SBC allows your PC to control the execution of any of Intel's SBC Computers. Both download and upload capability.

\$750.00

MDOS IS A TRADEMARK OF MICROSOFT CORP.
SBC & iRMX ARE TRADEMARKS OF INTEL CORP.

RTCS

**REAL-TIME COMPUTER
SCIENCE CORPORATION**

P.O. Box 3000-886 (805) 482-0333

Camarillo, CA 93011

TELEX #467897

CIRCLE 154

SYSTEM COMPONENTS/ MICROPROCESSORS/MICROCOMPUTERS

8-bit EPROM microcomputer unit

MC1468705G2 and MC1468705F2 CMOS EPROM microcomputers feature static operation, single 3- to 5-Vdc power supply requirement, internal 8-bit timer with software programmable 7-bit prescaler, external timer input, external timer and interrupts, and onchip oscillator. The 1468705G2 has 40 pins and contains 112 bytes of RAM, 2106 bytes of UVEPROM, and 32 bidirectional I/O lines. The 1468705F2 will have 28 pins, 64 bytes of RAM, 16 bidirectional I/O lines, 1080 bytes of UVEPROM, and be an EPROM version of the mask ROM 146805F2. The \$250 1468705G2 is being sampled now; 1468705F2 will be available during mid-1983. **Motorola Inc, MOS Microprocessor Div**, 3501 Ed Bluestein Blvd, Austin, TX 78721.

Circle 297

CPU board accesses 16M-byte nonsegmented memory

Able to directly access a full 16M bytes of nonsegmented memory on the IEEE 696/S-100 bus, the 10-MHz, 68000 based CPU board handles 8- and 16-bit memory and allows simultaneous mixing of both types. The CPU 68K board (\$850) includes the 68000 processor, a socket for the 68451 MMU, and sockets for up to 16k bytes of EPROM. Onboard sockets accept 2716, 2732, or 2764 type EPROMs, and provision is made for power-on jump using EPROMs. Onboard wait state generator and interrupt structure are included. Up to 5 waits can be added to any cycle. Software support includes the CP/M-68K and a Forth OS. **CompuPro Systems**, Oakland Airport, Oakland, CA 94614.

Circle 298

16-bit supermicro with Winchester, multi-user capabilities

Sage IV 16-bit supermicrocomputer, accommodating up to 6 simultaneous users, is based on the 8-MHz 68000 processor. System performs 2M operations/s. It comes std with 128k main memory expandable to 1M byte. A 5M- to 30M-byte fixed or removable Winchester disk is built-in next to a 5 1/4" floppy backup. Since there are no wait states, a 20k program loads from the floppy in 1 s, and from the hard disk on 0.1 s. **Sage Computer Technology**, 35 N Edison Way, Reno, NV 89502.

Circle 299

Desktop micro



DTC desktop microcomputer includes keyboard/CPU, screen, and disk drive. It comes standard with 64k-byte RAM, 32k-byte ROM, and dual 320k-byte floppy disk drive. Facit DOS, CP/M 2.2, and a 15" (38-cm) 80-col nonglare screen with amber phosphor chars are also included. Two RS-232-C serial communications ports and a BASIC interpreter are provided. Several software packages are available, in addition to a wide selection of CP/M applications. **Facit, Inc**, 235 Main Dunstable Rd, Nashua, NH 03061.

Circle 300

16-bit CPU board for STD bus

RSD-8088 single-board STD bus computer (\$390) features the 8088 4.77-MHz microprocessor with internal 16-bit wide registers, 16-bit ALU, and a set of 16-bit instructions. Twenty programmable parallel I/O lines are usable with/without handshaking, and onboard interrupts for serial and parallel I/O are included. Five 28-pin byte-wide memory sockets are jumper configurable for 24- or 28-pin EPROM or RAM, and 256-byte additional RAM reside onboard. Wait state generator, programmable memory and I/O map decoder, 1M-byte address range and 64k I/O range, and CPU status bits available on STD bus interface are featured. **Robotrol Corp**, 1250 Oakmead Pkwy, Sunnyvale, CA 94086.

Circle 301

Micro delivers low cost minicomputer/UNIX performance

A 68000/UNIX based multi-user MULTIBUS configured microcomputer, the CODATA 3300 comes std as an 8-user system with integral 5 1/4" 33M-byte Winchester drive for \$9600. A 2-user version with 12M-byte Winchester is priced at \$7800. An 8" 84M-byte Winchester configuration is \$13,500. System has 320k bytes of parity protected RAM, expandable to 1.5M bytes with memory management. Backup is via quad-density floppy disk, cartridge tape, or 9-track tape drives. **Codata Systems Corp**, 285 N Wolfe Rd, Sunnyvale, CA 94086.

Circle 302

Digi-Data Cartridge Systems Don't Care Which Bus You're On.

Select just about any popular microcomputer. Digi-Data has a Series 70 Cartridge tape drive that's ready to go, adding up to 30 Mbytes of unformatted storage capacity to your system. Delivering data reliability through proven conservative electro-mechanical design. Performing now . . . without additional hardware or software design.

Cartridge tape drive systems are available in standard or serpentine configurations to record on ANSI standard 1/4" data cartridges and are supplied as a small, attractive desk top unit.

Model 70R systems house their controller within the desk top unit, and interface with any RS-232C port having asynchronous protocol emulation.

Models 70S, 70M and 70Q include single board imbedded controllers for S-100, Multibus* and Q-bus** processors respectively. Compatible interface software is included for S-100 and Multibus

configurations operating under CP/M*** or MP/M.***

Model 70Q emulates DEC** TM11/TU10 magnetic tape subsystems, and is supported by RT-11V4, RSX-11MV4.0 and RSTS/EV7.0 operating systems without modification. The Q-bus controller occupies one quad-slot.

So take the easy road to microcomputer bus-compatible storage. Select a Series 70 system from Digi-Data.

If you need conventional 1/2" tape systems, investigate our Series 40 start/stop line and our Series 2000 streamer, the best value in large volume Winchester drive back-up.

Registered Trademark of *Intel Corp.,
Digital Equipment Corp., *Digital Research, Inc.



**DIGI-DATA
CORPORATION**

8580 Dorsey Run Road
Jessup, MD 20794
(301) 498-0200
TWX 710-867-9254

In Europe contact:
Digi-Data Ltd.
Kings House, 18 King Street
Maidenhead, Berkshire
England SL6 1EF
Tel. No. 0628 29555-6
Telex: 847720
CIRCLE 155



MULTIBUS

Q-BUS

RS-232

S-100

WESTREX DOT MATRIX PRINTERS

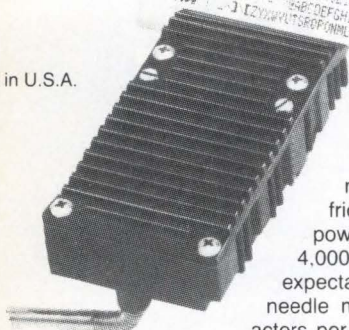
800 SERIES

MODEL 801
Low Profile, Low
Weight, Low Cost,
Impact Needle Matrix
Print Head

Presently Used In POS/
ECR Printers. Adaptable
To Scales Systems,
Ticketing Systems And Other
Special Printing Applications

Westrex Model 801 features a 7
needle vertical array with minimum
friction straight needle paths, low
power consumption; a duty cycle of
4,000 characters per minute with a life
expectancy of 75×10^6 characters; impact
needle matrix printing at up to 150 char-
acters per second with a character height of
3.45 mm (0.136"). Made with quality tested
components for maximum cost effectiveness.

Made in U.S.A.



For full details, write or call us

WESTREX OEM PRODUCTS

Litton

51 Penn Street, Fall River, MA 02724, (617) 676-1011 TELEX: 1651490, WFRW
IN FRANCE — WESTREX OEM PRODUCTS, 103-105 Rue de Tocqueville,
750 Paris, France 01-766-32-70 TELEX: 610148
IN SWEDEN — WESTREX OEM PRODUCTS, Box 3503, S-17203 Sundbyberg,
Sweden 46/8 + 981100 TELEX: 12139

CIRCLE 169

DIAL-A-PROM Today... Plug It In Tomorrow.

- Call DIAL-A-PROM™ at 408/746-0333
- Transmit your PROM data via modem to our computer. Available formats: Binary, Tek Hex, Intel MDS, ASCII Hex, Motorola Mic Bug, BNPF/BHLF and PALASM text files.
- We'll have your PROMs on the way to you **today** ...!

EPC... Everything for the PROM User.
DIAL-A-PROM... A Service of

ePC electronic
programming
corporation

3681 Enochs St.
Santa Clara, CA 95050
408/746-0333 TWX: 910-338-2311

DIAL-A-PROM is a trademark
of Electronic Programming Corporation

SYSTEM COMPONENTS/ TEST & MEASUREMENT

Network tester emulates DEC protocol



Dyna-Test 2000B troubleshoots networks using the DEC DDCMP protocol, displaying the header, block check chars, and text in a DDCMP message. Transmit signal is shown in reverse video and the receive signal in normal video. Noninterrupt mode monitors all interface signals and displays transmit/receive signals. With the interface open, unit can simulate a terminal, modem, or frontend processor port to the DDCMP network. Full keyboard, 200k-char tape, and external video and printer outputs are provided. All programs are stored in nonvolatile 1k-byte memory and can be transferred to tape. **Dynatech Data Systems**, 7644 Dynatech Ct, Springfield, VA 22153. **Circle 303**

Logic analyzer adds performance measurements to timing/state analysis

Models HP1630A (35 input channels) and HP1630D (43 input channels) logic analyzers work as 8- or 16-channel timing analyzers, 35- or 43-channel state analyzers, interactive state/timing analyzers, and software performance analyzers. Performance measurements provide realtime distribution of execution times and software events. All modes have 1024-word sample memory. State measurements up to 25 MHz and timing measurements up to 100 MHz are made in real time and nonintrusively. Units are compatible with the HP-IL, HP-IB, HP's minicassette drive, and most 8- and 16-bit processors. Contact local **Hewlett-Packard** sales offices.



Circle 304

TOP OF THE LINES.

The C. Itoh dot matrix line printers deliver a new level of price/performance for a wide range of business and scientific applications—including a complete selection of graphics.

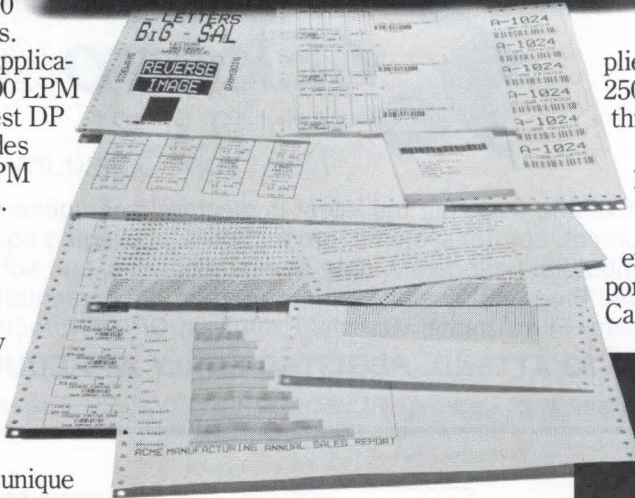
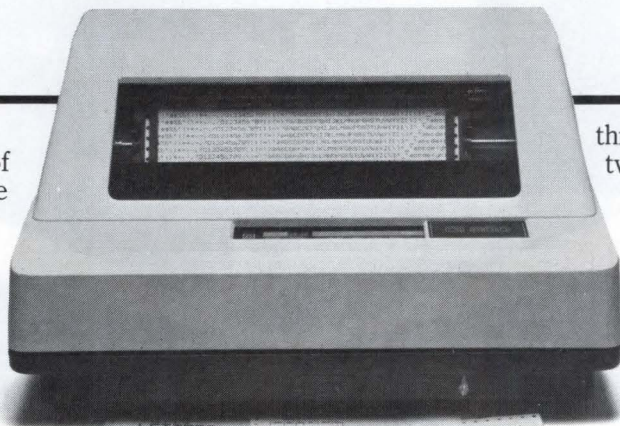
There's the CI-300, a variable speed line printer that offers 300 LPM print speeds for data processing, 80 LPM for letter quality use and up to 2400 DLPM for graphics applications.

For your highest volume applications, there's our CI-600. Its 600 LPM print speed cuts even the biggest DP jobs down to size. It also provides letter quality printing at 170 LPM and up to 4800 DLPM graphics.

Both models bring bit-addressable graphics and high resolution to Bar Codes, OCR, Form Generation, Labels, and Word Processing. An incredibly small .013" print head diameter in the matrix produces the highest quality output you can find. Resolution is enhanced still further with our unique variable shuttle speed capability.

You get tremendous flexibility too. Thanks to easy user selection of print speed and density, character and line spacing, line feed speed, print control and many functions, including 3 paper loading entry points. In addition, a vast array of download features enable the printers to match many specific computer requirements.

At C. Itoh, we don't think a printer has to look ugly to perform beautifully. That's why both of our line



three convenient built-in interfaces: two parallel and one serial.

For exceptional reliability, both printers feature a minimum of moving parts. Each is designed for highest duty-cycle use, making them ideal for all demanding environments, even warehouse and industrial locations. And don't forget, they're supplied by C. Itoh, one of the most experienced printer suppliers in the world with more than 250,000 units delivered in the last three years.

C. Itoh's CI-300 and CI-600 line printers. Top of the line performance—at a very low price.

For full details, contact our exclusive representative, Acro Corporation, 2515 McCabe Way, Irvine, California 92713 (714) 557-5118.

printers are designed to fit right into every office environment. They offer a small footprint, a low profile, and a true office environment noise level.

To satisfy your exact requirements, hundreds of unique character fonts are standard—plus you can design your own characters through the RAM which can be downloaded for special sets. An option board permits you to use macro selection for graphics production. Both printers come with

Either on desk top or with stand



C. ITOH ELECTRONICS

5301 Beethoven St, Los Angeles, CA 90066 (213) 306-6700

Northeast's Largest Hi-Tech Electronics Event.




Electro/83

April 19, 20, 21
New York Coliseum

- 1000+ Product Exhibits featuring the latest in electronic components, instruments, test equipment, control systems, production & packaging equipment, minicomputers, peripherals, data communications, and software.
- 26 Professional Program Sessions with more than 130 presentations • Special Seminars • Film Theater • Special Exhibit on *Office Automation*

PLAN NOW TO ATTEND. REGISTER EARLY AT REDUCED FEE.

For a Preview Program, write: Electro/83, P.O. Box 92275 Worldway P.C., Los Angeles, CA 90009



00000

\$5 EARLY
REGISTRATION

REGULAR
ADMISSION
FEE: \$20
IEEE or ERA: \$10

Please PRINT as you want shown on badge

Name _____
FIRST OR INITIALS LAST

Position • Telephone _____ • _____
AREA CODE NUMBER (OPTIONAL)

Company/Organization _____

Address: Bus. or Home _____
DEPT. or M/S

City, State, Zip Code _____
STATE ZIP CODE

Important Note: To receive your badge in advance, complete this form and mail along with check to: Electro, P.O. Box 92275, Los Angeles, CA 90009; to arrive no later than March 31, 1983. Persons under 18 years of age not admitted.

CIRCLE APPLICABLE BLOCKS

A	Electrical/Electronic Engineering
B	Mechanical Product Engineering
C	Test Engineering
D	Production/Mfg. Engineering
E	Engineering Services
F	Purchasing
G	Sales/Marketing
H	Manufacturers Rep.
I	Management
J	Student/Educator
K	Other

JOB FUNCTIONS(S)

AREAS OF MAIN PRODUCT INTEREST

L	Active Components
M	Passive Components
N	Electro-Mechanical Components
O	Tools and Production Equipment
P	Computers and Peripherals
Q	Instrumentation/Test Equipment
R	Control Systems
S	Mechanical/Electronic Packaging
T	Data Communications
U	Power Sources
V	Other

DOUBLE YOUR SIGNAL-TO-SPACE RATIO WITH AUGAT SELECTIVE GROUNDING.

Now there's an IDC mass termination receptacle and header system that lets you double I/O density on standard-sized printed circuit boards. It's called the Selective Grounding, SG Series from Augat. Here's how it works:

INTERNAL GROUND BUS. A unique bussing feature built into the SG Series receptacle allows you to mass terminate common ground wires. Designate any one I/O contact (or more) per row as ground. Use all the rest for signals. This allows one receptacle to accommodate two planar cables, and in effect, doubles your signal-to-space ratio.

TWO FLAT CABLES. Connector accepts two twist and flat, standard grey PVC or color-coded planar cables simultaneously.

SEVERAL PLATING OPTIONS reduce sensitivity to the price of gold and ensure high reliability. They include: receptacle contact points with 50 micro-inch selective gold plating; header contacts with 10 to 50 micro-inch all over or selective gold plating.

FULLY SHROUDED HEADER connects receptacle to printed circuit board. Unique electromechanical lock/eject function automatically decouples optional shield drain wire. Eliminates soldering of drain wire to board.

Augat SG Series receptacles come in 24 to 64 positions. Headers 10 to 64 positions. Inquire about our DIN compatible and EMI/RFI shielding options. Complete applications tooling for in-house production available. Contact Augat Inc., Interconnection Components Division, 33 Perry Avenue, Attleboro, MA 02703. Tel: (617) 222-2202. TWX 710.391.0644. See our catalog in GOLD BOOK, Volume II-1, 9th Edition.

See us at ELECTRO SHOW—Booth # 2224

AUGAT[®]

Quality and
Innovation

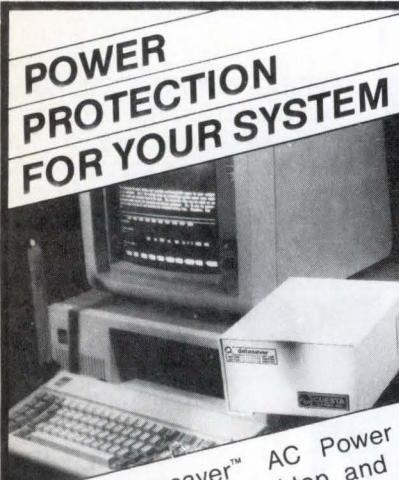
Pressure sensing digitizing pen



Digitizing pen senses up to 32 pressure levels applied to the pen tip. These levels are translated into varying line widths and textures, gray scale, color, or depth in a computer generated image. Control station visually indicates status through red, green, and yellow LEDs. Zero and max pressure adjustment controls are included. Compatible with the company's Digi Pad digitizers, the pen can be used with the 4-D pen tilt output option for natural pen control. Price is \$720. **GTCO Corp**, 1055 First St, Rockville, MD 20850.

Circle 305


POWER PROTECTION FOR YOUR SYSTEM



The Datasaver™ AC Power Backup fits most desktop and portable microcomputer systems. Call **Cuesta Systems, Inc.** at (805) 541-4160 for product information and application literature. VISA/Mastercard orders call (800) 851-6055.

CUESTA SYSTEMS, INC.

3440 Roberto Court
San Luis Obispo
California 93401
(805) 541-4160

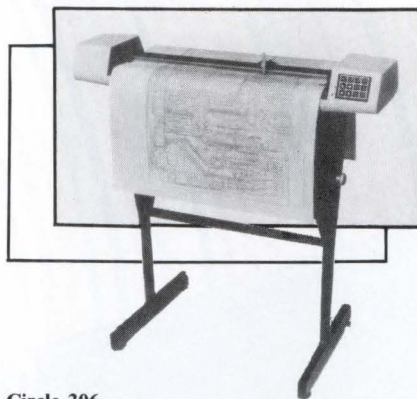


INSTANT POWER

CIRCLE 159

D-size plotter

DMP-41 drafting quality graphics plotter (\$2995) for micro- and minicomputer CAD applications accepts D-size (55.88- x 86.36-cm) formatted media and plots a 50.8- x 81.28-cm area. Drive mechanism accepts fiber, ball-point, and ink pens on bond, vellum, or mylar media. Intelligent plotter can scale drawings up or down, vary aspect ratios, clip, and viewport/window portions of a drawing. Firmware automatically generates circles, ellipses, arcs, and portions of curves. **Bausch & Lomb, Houston Instrument Div**, 8500 Cameron Rd, Austin, TX 78753.



Circle 306

Touch-sensitive display terminals

Model TT-150 touch-sensitive display terminal with tilt and swivel base has all switches, adjustments, and cable connections accessible through a key operated panel to prevent tampering. With program selectable 2-page display memory, the microprocessor based terminal also has a high resolution 15" (38-cm) CRT and 10 x 14 dot matrix display. Full upper- and lowercase ASCII char set with normal/reverse attributes are standard. Graphics char set, additional video attributes, and keyboard are optional. Terminal is \$2000. **Interaction Systems, Inc**, 24 Munroe St, Newtonville, MA 02160.



Circle 307

VT-132 emulating terminal



TS-132 terminal emulates DEC's VT-132 unit and includes a video display, keyboard with 80- and 132-col formats, block mode for local editing, local RS-232-C printer port, 14 programmable function keys, and 128-char set. Programs written for the DEC machine can be directly transported without modification. Local storage is increased by memory management that converts unused horizontal area into additional vertical storage. Lines with repeated chars are stored in packet format for increased buffer storage. Price is \$1650. **Falco Data Products, Inc**, 1286 Lawrence Station Rd, Sunnyvale, CA 94086.

Circle 308

Upgraded color graphics terminals

Added versions to the Colorgraphic terminal series include rackmount R6211, 40-Hz interlaced LP phosphor 6211-03, and the 6221 Colorgraphic terminal with complete VT100 compatibility. R6211 rasterscan terminal (\$3995 without monitor) communicates with any host computer via RS-232-C interface. Its 640- x 480/512-pixel resolution allows simultaneous display of up to 16 colors from a 64-color palette. The 6211-03 terminal (\$4995) is for applications that do not need video peripheral support provided by the 6211-01 and 6211-02 terminals. **Ramtek Corp**, 2211 Lawson Lane, Santa Clara, CA 95050.

Circle 309

Like to write?

The editors invite you to write technical articles for Computer Design. For a free copy of our Author's Guide, circle 503 on the Reader Inquiry Card.

New Amdek 3" micro-floppydisk drive system!

AMDISK-III . . . the engineer's choice:

- New 3" hard plastic encased diskette.
- Up to 1 megabyte storage. (unformatted)
- Plug-in compatible with 5¼" drives.
- Compatible with - IBM-PC.



Economically priced for business or personal computers!

Specifications

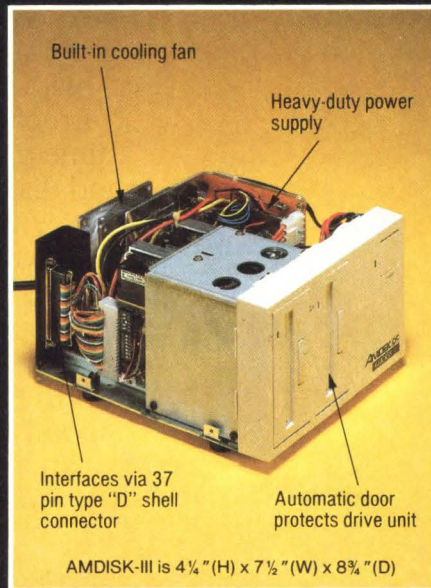
	Unit	Double Density
Capacity		
Unformatted Per Surface	Bytes	250K
Media		
Record Surfaces	2	
Tracks	80	
Recording		
Max Recording Density	Bpi	8946
Track Density	Tpi	100
Transfer Rate	bits/sec	250K
Access Time		
Average Access Time	msec	55
Track to Track	msec	3
Setting Time	msec	15
Average Latency Time	msec	100
Motor Start Time	sec	1
Disk Speed	rpm	300
Reliability		
Error Rates		
Soft Error		10 ⁻⁹
Hard Error		10 ⁻¹²
Seek Error		10 ⁻⁶
Media	3-inch Cartridge	
Drive Interface	Plug Compatible with 5.25 inch FDD	

External Interface

Connector: 37-pin "D" shell connector

Pin No.	Signal	Pin No.	Signal
1-5	Unused	13	Write data
6	Index	14	Write enable
7	Motor enable C	15	Track 00
8	Drive select D	16	Write protect
9	Drive select C	17	Read data
10	Motor enable D	18*	Select head 1
11	Direction	19	GND
12	Step pulse	20-37	GND

*drives are single head



Built-in cooling fan

Heavy-duty power supply

Interfaces via 37 pin type "D" shell connector

Automatic door protects drive unit

AMDISK-III is 4¼" (H) x 7½" (W) x 8¾" (D)



Evaluation samples \$480

Includes two-drive Amdisk unit with built-in power supply, 4 diskettes and application literature . . . Call (312) 364-1180.

The AMDISK-III Micro-floppydisk System is an engineering breakthrough in disk size, storage capacity, media protection and user convenience. Designed for microcomputers for many applications, the Amdek system is ruggedly constructed to provide years of trouble-free operation. Warranty is 90 days (parts & labor).

Put the new AMDISK-III to test . . . its recording format, data transfer rate and disk rotation speed are compatible with 5¼" floppydisk drives. Call, or write for evaluation samples at only \$480.00 . . . or circle the reader service number for full technical details.

2201 Lively Blvd. • Elk Grove Village, IL 60007
(312) 364-1180 TLX: 25-4786

AMDEK CORP.

Amdek . . . your guide to innovative computing!

On the perception of elegance.

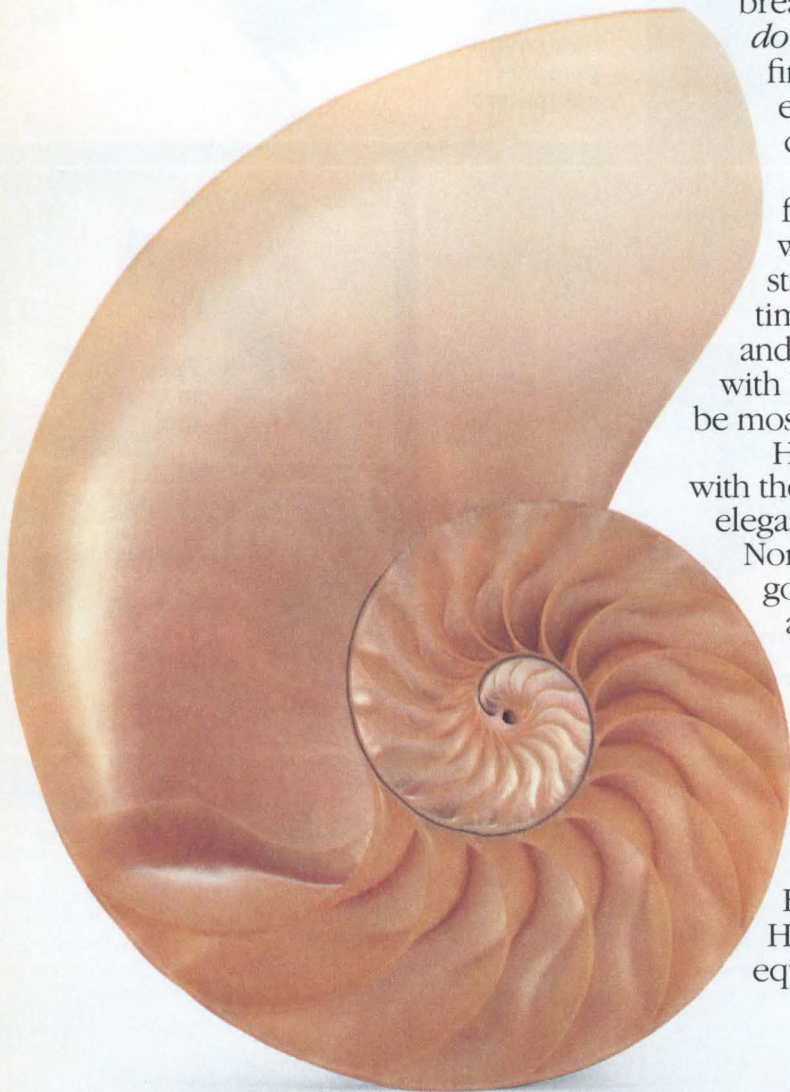
Artist, engineer and scientist alike can't help but share a passionate appreciation for the forms of nature. Regard the exquisite symmetry of the nautilus shell. It is only one of nature's expressions of grace in shape and line. And it was achieved through a development program aimed entirely at function.

Around Honeywell, Underseas Systems Division scientists occasionally speak warmly of the elegance of algorithms encountered along the way to significant breakthroughs in software design. We *do* enjoy working with people who find pleasure in technical solutions embodying that special simplicity called elegance.

Right now we're searching for a few such software specialists with a BS/MS and background in structure design, field testing, or real time/time-control applications for test and diagnostic hardware. Experience with UYK-20, AYK-14, or CMS-2 would be most welcome.

Here's vigorous challenge, coupled with the opportunity to discover certain elegances of style among the Vikings, the North Stars, and other elements of good living unique to the Twin Cities area of Minnesota—the vigorous quality-of-life capital of the U.S.

For prompt, confidential consideration call George Bills collect at 612/931-6713. Or send resume to: George Bills, Engineering Manager, MN 11-102 0D, Underseas Systems Division, Honeywell, 600 Second Street N.E., Hopkins, MN 55343. Honeywell is an equal opportunity employer.



Honeywell

Making a world of difference.

SYSTEM COMPONENTS/ MEMORY SYSTEMS

Quarter-inch cartridge tape drives with 5¼" footprint



Microtape® family of ¼" digital start/stop cartridge tape drives fit into std 5¼" Winchester or floppy disk package dimensions and are available with either end-loading or side-loading cartridges. Initial family member is a 17.3M-byte, 4-track drive that is media and interface compatible with "The Funnel" digital cartridge tape used for Winchester backup. An equivalent, Funnel compatible, serpentine version requires no rewind time between tracks. Streaming 30- or 60-ips members have capacities to 10M bytes. Prices range from under \$400 to approx \$870. **Data Electronics, Inc.**, 10150 Sorrento Valley Rd, San Diego, CA 92121. **Circle 310**

Self-contained 512k x 24 memory array

Single memory array card MK8064 features 64k dynamic RAM technology, capacities up to 512k at 16 to 24 bits/word, and includes all logic circuitry to perform read, write, split cycle, and refresh operations. Inverting or noninverting data option and byte control are featured. Customer controlled timing options are available. Price is \$6415 for the 512k x 24 version in single-unit quantities. **Mostek Corp, a sub of United Technologies Corp**, 1215 W Crosby Rd, Carrollton, TX 75006. **Circle 311**

Half-height 5¼" floppy

Pico RFD 485 500k-byte, 48-tpi and Slimline® RFD 965 1M-byte, 96-tpi double-sided drives measure 1.61" (4.09 cm) behind the bezel. Self-centering clutch and spindle design improves media to spindle registration. Advanced LSI circuitry reduces logic board size. Bezel is interchangeable with 3 sizes. R/W heads are loaded onto and unloaded from the media surface; head load solenoid is eliminated. The ANSI compatible RFD 965 (\$260) drive has 3-ms track to track access and RFD 485 (\$210) is rated at 5-ms access. **Ex-Cell-O Corp, Remex Div**, 1733 Alton St, Irvine, CA 92713. **Circle 312**

COMPUTER GRAPHICS

COMPUTER PROFESSIONALS MANAGERS/ENGINEERS DESIGNERS CONSULTANTS IN-HOUSE AND SERVICE BUREAUS

Fed up with all the confusion about which computer graphics systems are best for you?

Get the facts you need most to benefit fully from all the latest advances and innovations.

From the drawing board to the boardroom ... COMPUTER GRAPHICS WORLD is the bridge between technology and applications.

In fact-filled issues we'll cover the entire scope of **worldwide developments** and **bottomline applications**, including ...

CAD/CAM ... CIM ... exploration ... cartography ... engineering ... education ... businesssystems ... transportation ... medicine ... architecture ... art ... energy ... training ... communications ... marketing ... printing ... video ... microprocessors ... data analysis ... management ... construction ... PLUS the latest news on software and hardware advances, meetings, and conferences. Whether you're currently using computer graphics or just considering the possibility, COMPUTER GRAPHICS WORLD is your vital, one-stop information resource. **Subscribe today!**

Act now and save 20%

To order, either:

Fill in the coupon below and return to COMPUTER GRAPHICS WORLD, P.O. Box 122, Tulsa, OK 74101.

or

Circle the reader service number below.

or

Call toll free 1-800-331-5959 (in Oklahoma call 918-835-3161), and tell us you want to save 20%

Fast!

Faster!

Fastest!

Yes, I want to save 20%. Enter my one-year subscription

L012

U.S.A. \$24.00 Canada/Mexico \$28.00 International \$32.00

Payment enclosed Please invoice Visa MC Card

Account Number _____ Expiration Date _____

Cardholder's Signature _____

Name _____ Title _____

Company _____

Type of Business _____

Address _____ Home Business

City _____ State _____ Zip _____

**Computer Graphics
World**

A PennWell Publication

16k pseudo PROM board

DCM 16 16k CMOS memory module has a 4k block increment write protect feature, accepts up to eight 2k 6116 CMOS RAMs, and can be addressed in 8k blocks. During software development, a program can be written/executed in RAM and later protected like ROM. Optional onboard NiCad rechargeable battery supplies module with over 1k h of backup. Eurocard sized with DIN connector, board is RM 65 and AIM 65/40 bus compatible. Module operates from 5-V and draws less than 50 μ A, fully populated. Prices range from \$295 to \$379. **Dynatem Inc**, 22600-D Lambert St, El Toro, CA 92630.

Circle 313

EDC enhances 512k-byte Multibus memory

Compatible with Multibus systems using 8086, 68000, and Z8000 microprocessors, MM-8086E (\$1695) chip provides up to 512k bytes plus error detection and correction. Circuit uses a modified Hamming code with 6 check bits for correction of single-bit errors (transparent to the processor) and detection of double-bit errors. Double-bit errors can be sent to the host computer for further processing via a jumper selectable interrupt line. Onboard control and error status registers are accessible under software control. Access time is 300 ns and cycle time is 500 ns. Battery backup is provided. **Micro Memory Inc**, 9436 Irondale Ave, Chatsworth, CA 91311.

Circle 314

Quarter-inch streamers give 45M-byte Winchester backup

Series 5000 $\frac{1}{4}$ " streaming cartridge tape drive measures 1.62" x 5.75" x 8" (4.11 x 14.61 x 20 cm) and has 90-ips tape speed. To ensure interchangeability, it employs a single-action loading mechanism to positively register a std 3M-DC3000XL $\frac{1}{4}$ " tape cartridge on ANSI defined data. Series is fully compatible with the QIC II intelligent interface and the QIC IIC recording formats. Series 8000 streamers are compatible with form factors of 8" floppy or Winchester disks and with QIC recording formats. The series stores 20M or 45M bytes and provides 30- or 90-ips speed. OEM price for either tape is \$800.

Wangeo, Inc, 5835 Uplander Way, Culver City, CA 90230. Circle 315

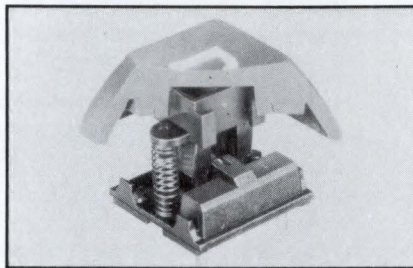
SYSTEM ELEMENTS

Thermal line printer mechanism

Thermal line printer mechanisms in 8", 4", and 2" (20-, 10-, 5-cm) models include model KSC252-N 2" mechanism that features 56-mm printhead, head driver, and stepping motor. In addition, 2.5 dots/mm, graphic print speed of 60-dot lines/s, paper feed speed of 78 mm/s, and paper set by moveable magazine at platen are included. Model measures 104.6 x 134 x 75 mm. **KSC Electronics, Inc**, 543 West Algonquin Rd, Arlington Heights, IL 60005.

Circle 316

Sealed contact keyswitch



Keyboard contact switch has two 1-mm balls held in line between concave conical faces of right angle switch terminals by a flexible silicone tube. Lateral pressure by the actuating plunger on the external tube wall displaces the balls to a "make" position with the terminal faces. Tube provides an atmospheric seal for the silver plated contacts and a restoring force to return contacts to an open condition. Low bounce closure with contact resistance of 15 m Ω and a life rating of 15M cycles results. Contamination protected switches can be water washed after wave soldering. Contact element is a removable subassembly of the company's DN series keyboard switch line. **Mechanical Enterprises, Inc**, 461 Carlisle Dr, Herndon, VA 22070.

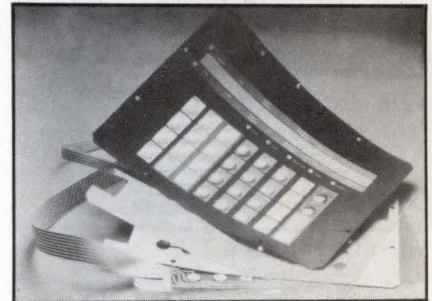
Circle 317

Low current LED lamps for battery powered applications

CMOS/MOS and TTL compatible red and yellow lamps, available in T1-3/4, T-1, and subminiature packages, operate at 2-mA current. Suitable for portable, battery powered applications, the lamps allow a longer battery life while providing a typ luminous intensity of 2 mcd. Both lamps have low forward voltage. Two red lamps can be driven in series from a 5-V supply. Contact local **Hewlett-Packard** sales offices.

Circle 318

Dome membrane keyboard



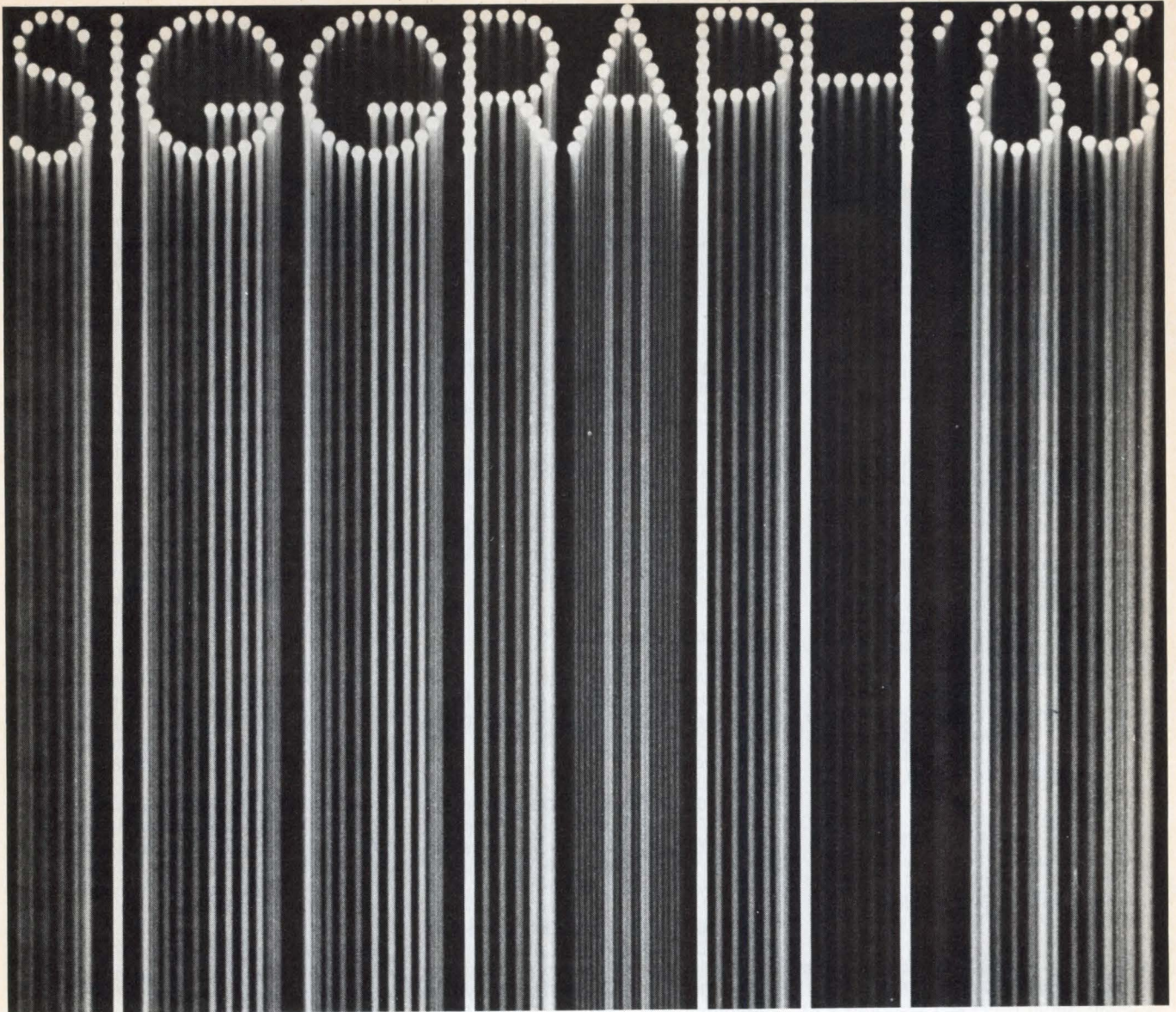
Polydome, a dome membrane keyboard, provides consistent tactile feel of keys and is a low cost sealed assembly alternative to mechanical switches. Switch travel is 0.03" to 0.038" (0.08 to 0.097 cm) with a 10M-operation life expectancy. The custom designable keyboard is assembled with an optional dome or flat overlay over a domed upper circuit, with a middle insulating spacer layer and a lower circuit. **Dorman Bogdonoff Corp**, Shetland Industrial Park, Andover, MA 01810. Circle 319

DIP switches with coded outputs

Line of DIP switches that provide BCD and hex coded outputs are available in 10 and 16 station lengths. The switches can be provided as a 1 of 10 circuit switch, a 1 of 16 circuit switch, a 10-position Tap switch, or a 16-position Tap switch. Common bus versions can be mounted side by side as an alternative to matrix switching. Prices range from \$2 to \$2.35 in 1k-piece lots, depending on circuitry and number of stations. **Grayhill, Inc**, 561 Hillgrove Ave, La Grange, IL 60525. Circle 320

Miniature infinite resolution potentiometers

Model 5010 10-turn potentiometer is 1.5" long and 0.5" in diameter (3.8 cm long and 1.3 cm in diameter) and has a resistance range of 5k to 100k Ω . Linearity is 0.1%. The wiper travels 3" (8 cm) along a helical resistance element. Model 55 single-turn rotary potentiometer measures 0.5" x 0.5" (1.3 x 1.3 cm) and has a resistance range of 500 to 50k Ω . Linearity is 2% to 0.5%. Model 125 linear motion potentiometer is 1.5" x 0.28" x 0.3125" (3.8 x 0.71 x 0.7938 cm) with an electrical stroke of 0.5" (1.3 cm). Resistance range is 1k to 10k Ω and linearity is 2%. All three devices employ proprietary conductive film resistance element and precious metal alloy wipers. **Vernitron Corp, Vernitech Div**, 300 Marcus Blvd, Deer Park, NY 11729. Circle 321



**The Premier
Computer Graphics Conference**

**July 25-29, 1983
Detroit, Michigan**

**The Tenth Annual Conference
on Computer Graphics
and Interactive Techniques**

Prepare for the technologically challenging years ahead. Plan now to attend the educational courses, technical program and exhibition at SIGGRAPH '83.

SIGGRAPH '83 . . . today's most comprehensive computer graphics conference.

Return the coupon for a SIGGRAPH '83 preliminary program containing complete information and registration forms. (Members of ACM/SIGGRAPH, Engineering Society of Detroit, IEEE Technical Committee on Computer Graphics and Eurographics automatically will receive the preliminary program in late April.)



Please send me the SIGGRAPH '83 preliminary program! K

Name: _____

Address: _____

City, State, Zip: _____

Return form to: SIGGRAPH '83
Conference Office, 111 East Wacker Drive, Chicago, Illinois 60601

CONFERENCES

APR 4-8—Tutorial Week East (including sessions on interactive computer graphics; robotics; data communication; and software design, development, management, and testing), Orlando, Fla. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

APR 5-8—Communications Tokyo, Tokyo Ryutsu Ctr, Tokyo, Japan. INFORMATION: Clapp & Poliak Internat'l, PO Box 70007, Washington, DC 20088. Tel: 301/657-3090

APR 5-7—Internat'l Reliability Physics Sym, Hyatt Regency Hotel, Phoenix, Ariz. INFORMATION: Richard Moss, Hewlett-Packard, 3000 Hanover St, Bldg 20DQ, Palo Alto, CA 94304. Tel: 415/857-4278

APR 6-8—Internat'l Optical Computing Conf, Cambridge, Mass. INFORMATION: S. Horvitz, PO Box 276, Waterford, CT 06385. Tel: 203/447-4270

APR 13-20—Hannover Fair, Hannover, West Germany. INFORMATION: Hannover Fairs Information Ctr, PO Box 338, Whitehouse, NJ 08888. Tel: 201/534-9044; 800/526-5978 (outside NJ)

APR 18-21—Internat'l Sym on Industrial Robots/Robots 7 Conf and Expo, Conrad Hilton Hotel and McCormick Pl, Chicago, Ill. INFORMATION: Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1500

APR 19-21—Electro, New York Coliseum and Sheraton Ctr, New York, NY. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965; 800/421-6816 (outside Calif)

APR 19-21—Mini/Micro-Northeast, New York Coliseum and Sheraton Centre Hotel, New York, NY. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965; 800/421-6816 (outside Calif)

APR 27-29—Satellite and Computer Communications Internat'l Sym, Versailles, France. INFORMATION: T. Bricheteau, Secretariat du Symposium, Domaine de Voluceau, Rocquencourt, BP 105, 78153 Le Chesnay Cedex, France. Tel: 3/954.9020; Poste 600

MAY 2-5—Test and Measurement World Expo, San Jose Conv Ctr, San Jose, Calif. INFORMATION: Meg Bowen, 215 Brighton Ave, Boston, MA 02134. Tel: 617/254-1445

MAY 9-13—SID (Society for Information Display) Internat'l Sym, Marriott Hotel, Philadelphia, Pa. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables FL 33134. Tel: 305/446-8193

MAY 10-12—Mini/Micro-Northwest, Portland Coliseum, Portland, Ore. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965; 800/421-6816 (outside Calif)

MAY 10-12—Northcon, Portland Coliseum, Portland, Ore. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965; 800/421-6816 (outside Calif)

MAY 16-18—Electronic Components Conf, Contemporary Hotel, Orlando, Fla. INFORMATION: Don L. Willyard, Bendix Corp, Dept 867 MF39, PO Box 1159, Kansas City, MO 64141

MAY 16-19—NCC (National Computer Conf), Disneyland Hotel and Anaheim Conv Ctr, Anaheim, Calif. INFORMATION: AFIPS, 1815 N Lynn St, Arlington, VA 22209. Tel: 703/558-3624

MAY 18-20—MIPRO (Microprocessors/Microcomputers Course/Conf), Congress Ctr, Hotel Adriatic, Opatija, Yugoslavia. INFORMATION: P. Dragojlović, MIPRO Secretariat, Trg P. Togliatti 4, 51000 Rijeka, Yugoslavia. Tel: +38 51 31 211 X424 (am); +38 51 741 494 (pm)

MAY 25—Automating Intelligent Behavior: Applications and Frontiers, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: Marvin Denicoff, Trends and Applications 83, PO Box 639, Silver Spring, MD 20901. Tel: 202/696-4302

JUNE 13-16—Internat'l Conf on Computer Architecture, Stockholm, Sweden. INFORMATION: H. W. Lawson, Jr, Linkoping Univ, S-581 83, Linkoping, Sweden

JUNE 14-16—Ohmcon, Cobo Hall, Detroit, Mich. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965; 800/421-6816 (outside Calif)

JUNE 19-23—Computer Vision and Pattern Recognition (formerly Pattern Recognition and Image Processing) Conf, Crystal City Hyatt, Arlington, Va. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JUNE 19-22—Internat'l Conf on Communications, Sheraton-Boston Hotel, Boston, Mass. INFORMATION: C. William Anderson, New England Telephone & Telegraph, 350 Cochituate Rd, Framingham, MA 01701. Tel: 617/879-9000

JUNE 26-30—NCGA, McCormick Pl, Chicago, Ill. INFORMATION: Nancy LeFebvre, Nat'l Computer Graphics Assoc, 8401 Arlington Blvd, Fairfax, VA 22031. Tel: 703/698-9600

JUNE 27-29—Design Automation Conf, Fontainebleau Hilton, Miami Beach, Fla. INFORMATION: Charles E. Radke, IBM Corp (ZIP-47A), Rte 52, Hopewell Junction, NY 12533. Tel: 914/897-4682

JULY 25-29—SIGGRAPH (Assoc for Computing Machinery Special Interest Group on Computer Graphics), Detroit, Mich. INFORMATION: SIGGRAPH Conf Office, 111 E Wacker Dr, Chicago, IL 60601. Tel: 312/644-6610

SEPT 19-23—IFIP (Internat'l Federation for Information Processing) World Computer Congress, Paris, France. INFORMATION: Philip H. Dorn, Dorn Computer Consultants, Inc, 25 E 86th St, New York, NY 10028. Tel: 212/427-7460

SEMINAR

APR-MAY—EMI Problems and Design Solutions, various cities and dates. INFORMATION: R & B Enterprises, 1050 Colwell Ln, Conshohocken, PA 19428. Tel: 215/828-6236

WORKSHOPS

APR 25-27—Software Engineering Technology Transfer, Miami Beach, Fla. INFORMATION: Richard Morton, General Systems Group Inc, 6849 Old Dominion Dr, McLean, VA 22101. Tel: 703/734-4915

APR 27-28—Strategic Planning for Office Automation, Watergate Mall, Washington, DC. INFORMATION: Nancy Anderson, Micronet/KSI, 2551 Virginia Ave NW, Washington, DC 20037. Tel: 202/333-4800

Solve your puzzle at INTERFACE '83

INTERFACE '83 offers practical solutions, because it is that very special annual gathering of major users and vendors located precisely at the convergence of computer and communications technologies. If you're a decision-maker involved with today's increasingly complex information systems, already planning or working with various pieces of the puzzle like...

- Local area nets
- Front ends, modems and MUXs
- Policy and regulatory issues
- Network services
- Desktop computers
- Office systems integration
- DDP
- And more...

Then join your peers at the 11th annual INTERFACE '83, March 21-24 at Miami Beach Convention Center, where you will discover how to put all the pieces together for solutions to your particular puzzle.

Once again, the INTERFACE Conference will point the way,

with more than 200 experts offering presentations on all aspects of the DataComm/Info Processing puzzle. These experts tell it like it is, so that you can convert their insights into productive operational decisions.

With these new insights provided by our experts, you'll really be in position to profit from the state-of-the-art displays on the INTERFACE '83 exhibit floor. More than 250 leading supplier companies will be on the floor of the Miami Beach Convention Center with their newest hardware, software, services ... ready to discuss with you the solutions they offer.

To round it off, you'll want to attend the second annual Industry Awards Banquet (black tie optional), and you'll also want to spend many informal hours exchanging views with the industry's leading consultants and most distinguished executives.

For complete details, *call us today* - 617-879-4502. Or complete and return the coupon below.

INTERFACE® '83 HAS YOUR SOLUTION

YES, I'd like to know how INTERFACE '83 can solve my Data Communications/Information Processing puzzle. I'd like more information.

Name _____

Title _____

Company _____

Address _____

City _____ State _____ Zip _____

Phone () _____

Send to: The Interface Group, Inc. Registration Department 160 Speen Street P.O. Box 927 Framingham, MA 01701



INTERFACE '83

March 21-24, 1983 • Miami Beach Convention Center, Miami Beach, FL

Co-Sponsored by **BusinessWeek** and **Data Communications** Magazines

THE INTERFACE GROUP
160 Speen Street, P.O. Box 927, Framingham, MA 01701 • (617) 879-4502

Producers of:
INTERFACE, FEDERAL DP EXPO, COMDEX/SRING, COMDEX/FALL, COMDEX/EUROPE, THE COMPUTER SHOWCASE EXPOs (Nationwide)

Glass fiber optic component

Bulletin specifies PVC jacketed Luxicon[®], which comes in continuous or terminated lengths with 0.043", 0.063", 0.079", or 0.09" diameter. **Dolan-Jenner Industries, Inc.**, Woburn, Mass.
Circle 410

Local area network

Short-form catalog examines PACX data switching systems, modems, multiplexers, and other LAN products. **Gandalf Data Inc, sub of Gandalf Technologies Inc.**, Wheeling, Ill.
Circle 411

Winchester backup

Brochure contains specs for quarter-inch, 20M-byte Intelligent Sidewinder and 45M-byte Super Sidewinder and compares factors involved in floppy disk and streaming cartridge tape backup systems. **Archive Corp.**, Costa Mesa, Calif.
Circle 412

Eight-bit selector guide

Product reference details features and functions of M6800 microprocessors, microcomputers, and peripherals; also covered are CMOS M146805 processors, preprogrammed ROM based microcomputers, and development systems for the 8-bit line. **Motorola Inc, MOS Microprocessor Div.**, Austin, Tex.
Circle 413

Reaction injection molding

Booklet describes plastics production technique using Bayflex and Baydur high performance polyurethane, and comments on product design applications. **Mobay Chemical Corp, Polyurethane Div.**, Pittsburgh, Pa.
Circle 414

International emi/rfi filter specs

Wall chart selection guide classifies filters that suppress rfi generated from equipment and rfi generated from power lines, and illustrates an electrical network for each filter. **SFE Technologies, San Fernando Electric Div.**, San Fernando, Calif.
Circle 415

Microprocessor peripheral chips

Booklet gives technical overview including communications and I/O support circuits, as well as peripheral and DMA controllers that operate with commonly used CPUs; functional descriptions, architectural diagrams, and pinouts for Z8000, Z8500, and Z80 peripherals are rendered. **Zilog, Inc, affiliate of Exxon Corp.**, Campbell, Calif.
Circle 416

Thin film disk drive

Technical data sheet describes STC 8380 drive, which has 2.5G-byte storage, 16-ms average access time, and 3M-byte/s data transfer rate; read/write technology allows a per-actuator capacity of 630M bytes. **Storage Technology Corp.**, Louisville, Colo.
Circle 417

Trimming potentiometers

Product reference contains complete electrical/mechanical specs for low cost and sealed single- and multiturn models; open type potentiometers with carbon, conductive plastic, and cermet resistive elements are also covered. **Murata Erie North America, Inc.**, Marietta, Ga.
Circle 418

S/R to digital converters

Data sheets outline series 5209 (14-bit) and 5210 (12-bit) models, which take continuous demodulation rather than peak sampling approach. **Transmagnetics, Inc.**, Farmingdale, NY.
Circle 419

Data conversion

Catalog gives general technical and detailed product information for data converters, hybrid modules, synchro instruments, and data bus products. **ILC Data Device Corp.**, Bohemia, NY.
Circle 420

Digital telecommunications test

Brochure presents test instruments for fiber optics, satellite communications systems, and digital modems; bit error rate test instruments for DS1, DS1C, DS2, and DS3 testing and interface noise test set are also described. **Scientific-Atlanta, Inc.**, Atlanta, Ga.
Circle 421

Data communications switching

Booklet introduces line of hard contact and solid state electronic equipment from low cost switching and patching modules to prepackaged and more sophisticated configurations that mount in computer-grade cabinets. **T-bar Inc.**, Wilton, Conn.
Circle 422

Uncommitted logic arrays

Product guide describes over 50 bipolar gate arrays with chip complexities from 100 to 10k gates and performance from CMOS power levels to ECL speeds; also covered are Digilin ULAS, which combine linear and digital functions, and ULAS developed to accommodate custom linear LSIS. **Ferranti Semiconductors, ULA Design Center.**, Commack, NY.
Circle 423

Fiber optic cables and connectors

Brochure details crush-resistant simplex and duplex cables, a patented connector that eliminates grinding and polishing of fiber ends, and versatile PCB/bulkhead receptacles. **Mohawk Cable Co, Optical Group.**, Leominster, Mass.
Circle 424

Portable network analyzer

Booklet introduces Encore 200 data communications diagnostic system, which acts as intelligent monitor, interactive simulator, storage device, remote controller, and network performance analyzer. **Digitech Industries, Inc.**, Ridgefield, Conn.
Circle 425

Motion control systems

Folder presents control motors/drives and preset indexers that fit a wide range of instrumentation, industrial control, automation/robotics, and laser/fiber optics applications. **Compumotor Corp.**, Petaluma, Calif.
Circle 426

Linear ICs for measurement and control

Catalog gives overview of product line, including basic specs and performance data as well as multiple-source cross reference. **Precision Monolithics Inc.**, Santa Clara, Calif.
Circle 427

Data communications events

"Sherry Says" wall calendar for 1983 lists significant moments in communications history and major industry conferences/exhibitions. **Racal-Milgo.**, Miami, Fla.
Circle 428

Realtime digital image processors

Short-form catalog illustrates standard line of image processing equipment, including table that compares features and specs of different models. **Quantex Corp.**, Sunnyvale, Calif.
Circle 429

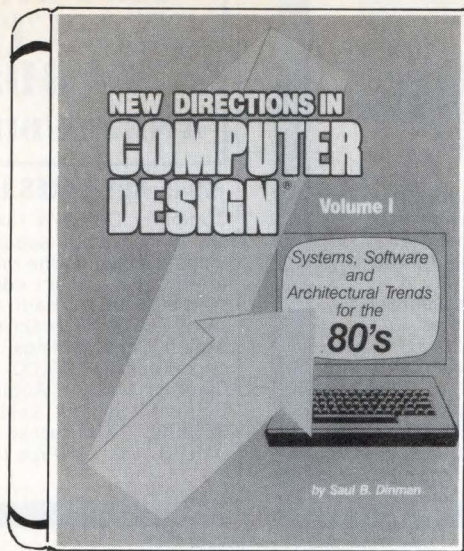
Custom integrated circuits

Brochure gives an overview of facilities, equipment, and custom ICs, along with CMOS and bipolar charts outlining process parameters for wafer fabrication plant. **Silicon Systems inc.**, Tustin, Calif.
Circle 430

Switching power supplies

Data sheet examines KRL series low cost, single-output power supplies, including I/O specs, dimensional drawings, and product photos. **KEC Electronics, Inc.**, Torrance, Calif.
Circle 431

Designer's Bookcase



New Directions in Computer Design: Systems, Software and Architectural Trends for the 80's Volume 1, by Saul Dinman

Some 20 years of technological innovation have created dramatic developments and changes in the computer systems industry. The book presents systems, software, and architectural trends for the 80's through a collection of articles covering Minicomputers, Microcomputers, Memory Systems, Software, and Data Communications.

PennWell Books, 1982, 135 pages, ISBN 0-87814-209-6, \$19.95. **Circle 455**

HOW TO ORDER:

15-DAY FREE EXAMINATION (U.S. AND CANADA ONLY)

Simply circle the appropriate number(s) on the Reader Inquiry Card at the back of this magazine.

Your book will be sent to you for your **15-day free trial**. If you are satisfied, keep the book and an invoice will follow. Otherwise return the book by the end of the 15-day period, and owe nothing.

Microcomputer Systems by Ivan Flores and Christopher Terry

Until now, microcomputer books simply told how to buy a microcomputer and then summarized what was available, discussed specific computer language and operating systems, or described families of integrated circuits. But this one-of-a-kind guide on microcomputer systems clearly explains both how each part of the system works and how they all fit together. 208 pp, 6 x 9, \$22.50, April **Circle 456**

Musical Applications of Microprocessors by Hal Chamberlain

Immediately acclaimed as a classic! Covers all current electronic and computer music performance techniques as they apply to microprocessors. Signal-processing techniques are presented in nonmathematical language and applied to newer, more powerful 16-bit microprocessors.

#5753-9; 688 pages; Hayden Book Co, Inc.; \$26.95 **Circle 457**

The S-100 Bus Handbook by David Bursky

Exclusively discusses S-100 bus computer systems and how they are organized. Covers computer fundamentals, basic electronics and the parts of the computer. Explains all operating details of commonly available S-100 systems. Each major system board detailed as to its operation and how it connects to the rest of the system.

0897-X, 272 pages; Hayden Book Co., Inc. \$15.75 **Circle 458**

Operating Systems A Pragmatic Approach by Harry Katzan

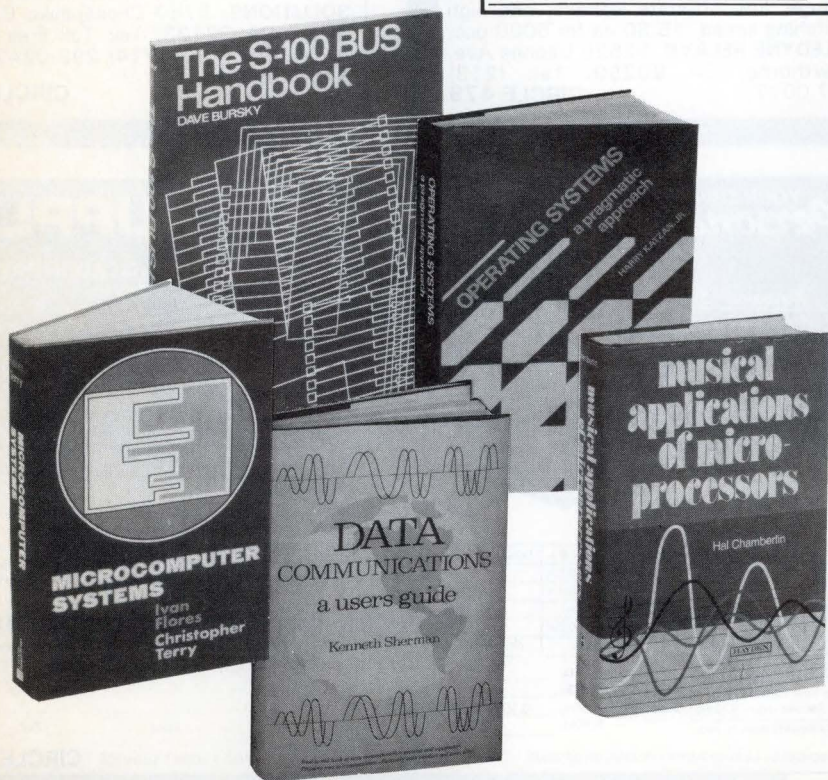
Computer pro Harry Katzan provides here authoritative coverage of the construction, functions, and terminology of operating systems. He fully explains such areas as dynamic loading and address translation, use of public and private storage, and virtual memory, data sets, and access methods. "A valuable addition to any computing library."

374 pp, 6 x 9, \$10.95, February **Circle 459**

DATA COMMUNICATIONS a user's guide by Kenneth Sherman.

A BRAND NEW quick and effective source for pinpointing and eliminating system malfunctions, discovering new, more efficient data movement, learning effective troubleshooting, ensuring strong, clear signal transmission and achieving maximum performance and value. Put these *all new* ideas and many others to work for you!

348 pages; 95 illustrations; Reston Publishing Company Inc; \$21.95. 1981. **Circle 460**



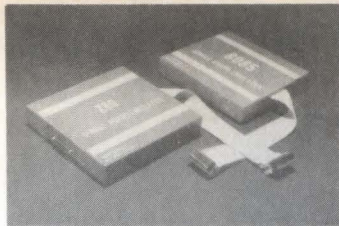
Presenting:
System Showcase

Your product could be represented here next month...

CALL

MAUREEN SEBASTIAN
(617) 486-8944
TOLL FREE
(800) 225-0556

CIRCLE 475



Z80 AND 8085 IN-CIRCUIT EMULATORS

- Real-time emulation to 6 MHz with hardware breakpoint or single-step
 - 16K bytes of mappable memory
 - RS232C interface for operation with a terminal or a host computer
 - In-line assembler and disassembler
 - Download or upload hex files
 - Complete debugging facilities
 - CP/M symbolic debug linking software via RS232 optional
 - 8085 unit \$1895; Z80 unit \$1895
- HUNTSVILLE MICROSYSTEMS, P.O. Box 12415, Huntsville, AL 35802. Tel: (205) 881-6005.**

CIRCLE 476

**COMPUTER DESIGN'S
HOTLINE
ACTION
CARDS**

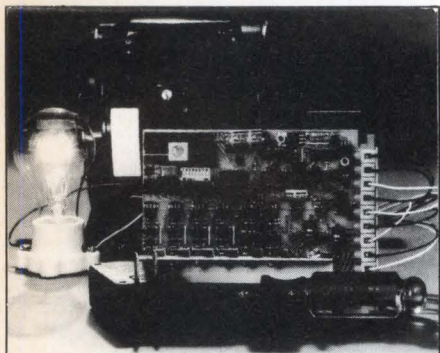
FAST
EFFECTIVE



MORE HOT SALES LEADS...

Computer Design's Hotline Action Cards are mailed to a special list of 65,000 readers including the most recent inquirers to our new product editorial items. Rates start at \$895 per card. If you run 2 or more cards in Computer Design's regular Direct Action Card Mailings your Hotline Card costs only \$795.00—A \$100 saving! Closings: May 21, August 21, October 21. Contact Shirley Lessard, **COMPUTER DESIGN**, 119 Russell St, Littleton, MA 01460. Tel: Toll Free (800)225-0556.

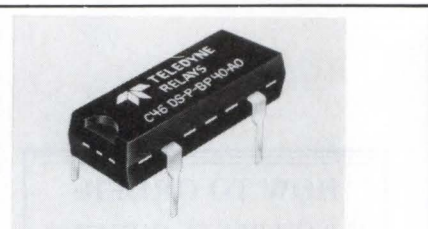
CIRCLE 477



6801 MICRO CONTROL SYSTEM

Analog and Power Control I/O...in a Single Board Computer, 6801 or 68701 MPU with 2K ROM or EROM, 128 RAM, timer. 8 12-bit analog inputs, 8-bit analog output, 8 AC or DC inputs or outputs, serial I/O, digital I/O, watchdog timer, power supply. **WINTEK CORPORATION**, 1801 South St, Lafayette, IN 47904. Tel: (317) 742-8428.

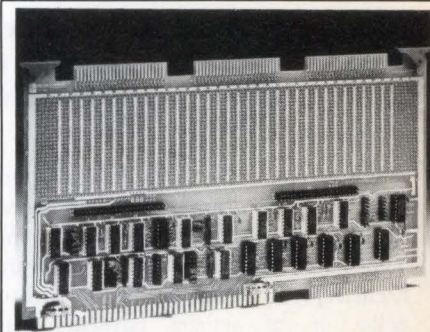
CIRCLE 478



SOLID STATE POWER FET AC/DC RELAY

Teledyne's C46/C47 series are pin compatible replacements for DIP reed relays where low EMI switching, high reliability and long life are required. Switches AC or DC up to 400V. On-resistance as low as 7 ohms. Control voltage range is 3.8 to 32VDC. Optical coupling provides 1500VDC isolation. Features no offset voltage, low off-state leakage, and high switching speed. \$5.80 ea for 5000 pcs. **TELEDYNE RELAYS**, 12525 Daphne Ave, Hawthorne, CA 90250. Tel: (213) 777-0077.

CIRCLE 479



MULTIBUS™ INTERFACE & PROTOTYPE

Prototype QUICKLY and EASILY. 100% of Multibus interfacing circuitry included. 20-bit Address, 8/16-bit Data. Delivery from stock. Multibus™ Intel corp, Model# PR 80A, Price: \$355 each. **ELECTRONIC SOLUTIONS**, 5780 Chesapeake Ct, San Diego, CA 92123. Tel: Toll Free (800) 854-7086, in CA (714) 292-0242, TLX 910-335-1169.

CIRCLE 480



A COMPLETE LINE OF PANASONIC CARD READERS offers quality, versatility and excellent reliability. Optical Badge Readers in both vertical and horizontal versions. A durable Automatic Magnetic Card Reader. And a choice of compact, low-cost Manual Magnetic reader/writers. **PANASONIC INDUSTRIAL COMPANY**, Office Automation Dept., One Panasonic Way, Secaucus, NJ 07094. Tel: (201)348-5337.

OPTICAL & MAGNETIC CARD READERS

CIRCLE 481

YOUR OWN Personal Switcher POWER SUPPLY

For Lab or Original Equipment



FEATURES: Efficient 30 kHz switching frequency • Four Models satisfy most applications • Years of trouble-free service • Each side AC line fuse protected • Tele-Tale LED "Pwr-On" Panel Indicator • Three separate voltage outputs • Metal enclosure provides physical and EMI protection • For experimental use or permanent power source • Soft start feature protects critical circuits • Parallel operation acceptable for a variety of uses and applications • Push-in terminals, accept wire or test lead • Light-weight, easy to use • AC line cord permanently attached • Most reliable power source for a variety of uses and applications • 48 hour burn-in assures MTBF of 3½ years, reasonably priced at \$1.90/watt • Full one year guarantee • 2-tone anodized case • Custom volt/current outputs on special order • Input surge protection • Automatic short circuit protection and restoration • UL recognized components • Handy Service Aid

SPECIFICATIONS: Input: 90-132VAC, 47-440Hz • Dual AC Input Fuses • Line Regulation: ±0.1% Max. for 10% input change • Load Regulation: ±0.2% Max. on #1 Output • Ripple Noise: Typ. 1% PP Max. • Over Voltage Protection • Reverse Polarity Protection • Compact, only 7½" x 4" x 2½" • Fast load transient response • 5 volt adj. ±10% DC Output: 42 Watts continuous • 70% Efficiency

ecom inc 1545 Osgood St. Unit 11L, No. Andover, MA 01845

Charge to: MasterCard Visa American Express Check/Money Order

Card # Exp. Date.....

Name

Address

City State Zip

Signature

SCHOOLS—LABS: QUANTITY PRICING ON REQUEST PHONE ORDERS: CALL (617)682-6936 FOR PROMPT SERVICE

CIRCLE 482

Qty.	Model	Output #1	Output #2	Output #3	Total
	PS-1	5V-6A	+12V-0.5A	-12V-0.5A	
	PS-2	5V-6A	+15V-0.4A	-15V-0.4A	
	PS-3	5V-6A	+12V-0.5A	-5V-1A	
	PS-4	5V-3A	+24V-0.6A	-24V-0.6A	
	Information on other switcher models				NC

ORDER INFORMATION		Sub-Total
Order First Unit—\$99.50		
Second Unit—\$79.60	Shipping & Handling	3.50
OFFER EXPIRES March 31, 1983		TOTAL

SCHOOLS—LABS: QUANTITY PRICING ON REQUEST

PHONE ORDERS: CALL (617)682-6936 FOR PROMPT SERVICE

DISCOVER CHEYENNE !

- NO—Corporate Income Tax**
- NO—Personal Income Tax**
- NO—Inventory Tax**
- NO—Tax on In-transit Goods**
- NO—Tax on Intangibles**
- NO—Problems!**

- 2 Industrial Parks • 2 Major Railroads
- 9 Truck Lines • "Right-to-Work" State

**Locate your corporate HQ,
master distribution warehouse,
or manufacturing plant in
CHEYENNE, WYOMING**

HAROLD M. MILLER, Ex. Director
Industrial Development Assn. of Cheyenne
Municipal Building, 2101 O'Neil Ave
Cheyenne, WY 82001 - 307-637-6385

CIRCLE 483

FREE

Industrial Devices, Inc.
The source
for
Indicator Lights
Let. Ritephoto. Non-obsolete



52 PAGE INDICATOR DESIGN GUIDE

New 52 page indicator light design guide/technical manual. Covers off-the-shelf and custom products—virtually every indicator design need—relampable, non-relampable, and LED's: bare LED's, LED assemblies and LED packages. Contains full size photos, specs, ratings and mounting drawings. **INDUSTRIAL DEVICES, Inc.**, Edgewater, NJ 07020.

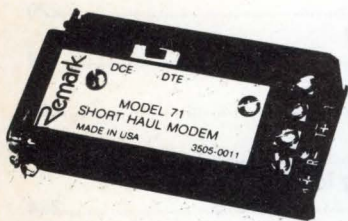


CIRCLE 484

NEW — MULTIBUS READ/WRITE PROM BOARD

The EEPROM-32 is a Multibus compatible EEPROM/EPROM board that utilizes the latest in program-store technology. With E2PROMs, reprogramming now takes only milliseconds instead of hours of expensive manpower. The EEPROM-32 accepts 2815, 2816 type E2PROMS or 2716 UV-erasable EPROMS, with an 8 or 16 bit data path and a 20 bit address space. Delivery from stock...Price: \$695 unpopulated. **ELECTRONIC SOLUTIONS**, 5780 Chesapeake Ct, San Diego, CA 92123. Tel: (714)292-0242, outside CA (800) 854-7086, TLX (910)335-1167.

CIRCLE 485



SHORT HAUL MODEM \$87

- 0 to 9600 BAUD
- 0 TO 10 MILES AT 1200 BAUD
- 2 MILES AT 9600 BAUD
- FULL DUPLEX
- OPTICALLY ISOLATED
- HOST POWERED MODEL 71 \$87
- SELF POWERED MODEL 72 \$125
- AVAILABLE NOW!

Remark DATACOM INC.
4 Sycamore Drive Woodbury, NY 11797 (516) 367-3806

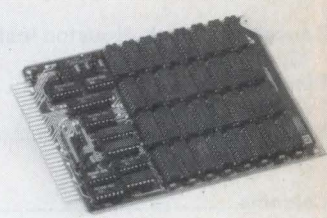
CIRCLE 486



LIKE NEW PRODUCTS

For free catalog,
phone toll-free (800)225-1008
In Massachusetts (617)938-0900
GENSTAR REI SALES COMPANY
6307 DeSoto Ave, Suite J,
Woodland Hills, CA 91367.

CIRCLE 487



TRUE STD NON-VOLATILE RAM. NO BATTERIES...AND VERY FAST!

The PM2212A is a TRUE Non-Volatile Memory card with 4K RAM & 4K Shadow EEPROM. Easy to program. One command STORES THE COMPLETE RAM ARRAY IN ONLY 10 MSEC. Long waits between byte writes are eliminated. Second command recalls array from EEPROM. Retains data indefinitely w/o power. Superior to battery backup. 1K, 2K & 4K populations. **PENN MICROSYSTEMS INC.**, 2318 West Eighth St, Erie, PA 16505. Tel: (814)452-4005.

CIRCLE 488



MAGNETIC SHIELDS & MATERIALS

Magnetic shields for storage, photomultiplier and cathode ray tubes, ESCA, auger spectrometers, special applications. Design, engineering, production services. Materials available in sheets or coils for forming your own shields. Also preserver cases for magnetic tape. Catalog, Designer's Reference **MUSHIELD CORP.**, 121 Madison St, Malden, MA 02148. Tel: (617)321-4410.

CIRCLE 489

LOW COST ADVERTISING

You can market your products to over 90,000 systems builders

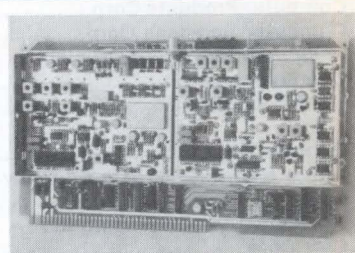
- * Hardware
- * Software
- * Services
- * Consulting

For only \$595.00 your ad will be typeset, laid out, and appear in this space. Sales leads will automatically be sent to you as we receive them.

Start today! Call Maureen Sebastian for details on how to start a low cost advertising program. Your sales results will tell you that it is the best decision you have ever made.

(800)225-0556 (Outside Mass)
(617)486-9501

CIRCLE 490



MULTIBUS BROADBAND MODEM

Featuring Sub, Mid, and 802 split compatibility, this modem transfers RS-422 data from DC to 4 MBaud. Synthesized transmit and receive frequencies provide 2 channel operation while FSK modulation, fast carrier control and low BER allow implementation of almost any network access protocol. Multibus provides frequency, status and test selection. **COHERENT SYSTEMS, INC.**, 3301 Airport Frwy #110 Bedford, TX 76021. Tel: (817) 267-4167.

CIRCLE 491

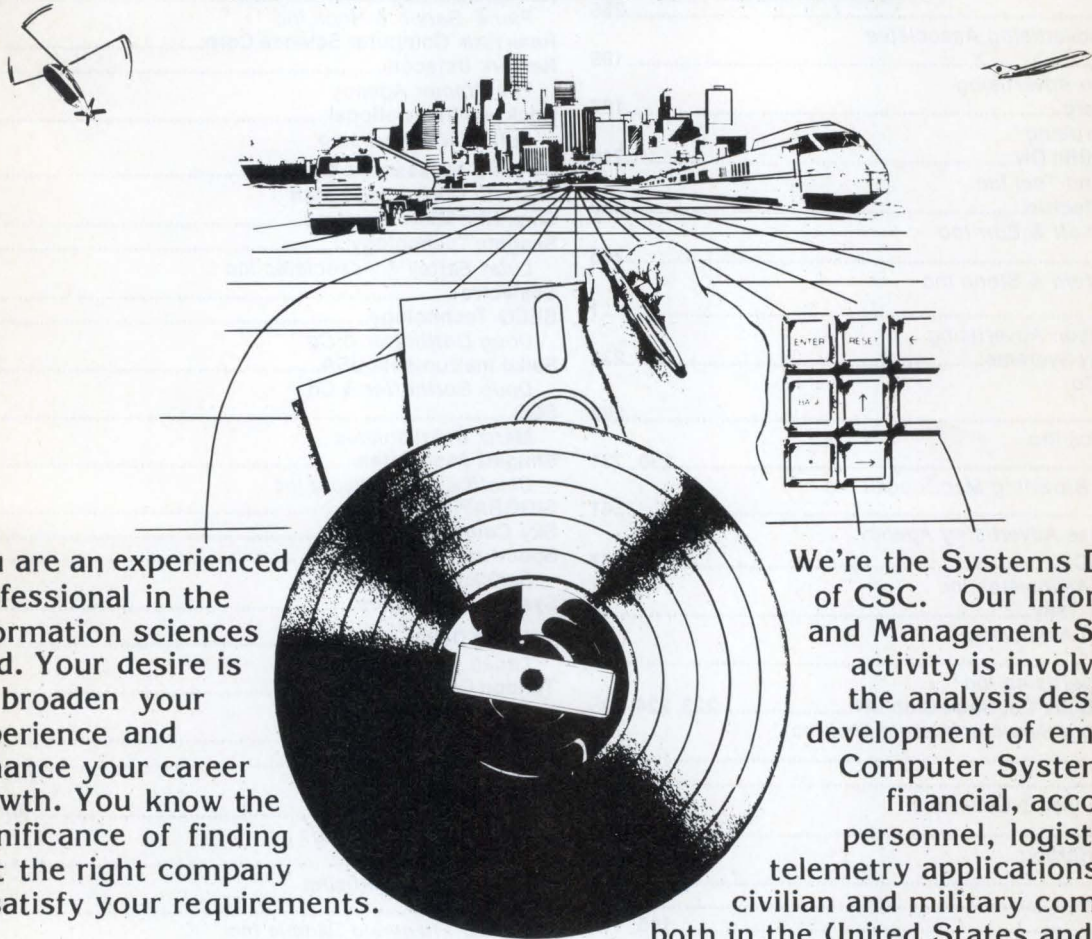
AD INDEX

ACDC.....	219	Davidge Corp.....	172
ACDC Advertising		Cencom	
Advanced Micro Devices.....	18, 19	Develcom Electronics Inc.....	207
Keyel/Donnal/Pearlstein		Robert H Fuller Advertising	
Airpax, Cambridge Div.....	249	Digi-Data Corp.....	253
The Aitkin-Kynett Co Inc		Business Marketing Inc	
Amdek Corp.....	259	Digital Communication Associates.....	161
George M Drake & Associates Inc		Cole Henderson Drake Inc	
AMP.....	150, 151	Digital Engineering.....	109
The Aitkin-Kynett Co Inc		Digital Equipment Corp.....	36, 37, 245
Ampex, Memory Products Div.....	185	Schneider Parker Jakuc	
Amphenol, an Allied Co.....	152, 153	Disctron.....	98, 99
Marsteller Inc		Peter Chope & Associates	
Analog Devices.....	121	Dynatech Data Systems.....	167
Giardini/Russell Inc		Pallace Inc	
Applied Circuit Technology.....	227	Electro '83.....	256
Cube 4		Electronic Conventions Inc	
Aptec Computer Systems.....	107	Electrohome Ltd.....	131
Jack Ramsey Agency		R T Kelly Advertising	
Associated Computer Consultants.....	158	Electronic Programming.....	254
Atlantic Research Corp.....	182	Stephen E Grossman Inc	
Audiotronics.....	193	Electronic Solutions.....	211, 268, 269
Augat.....	257	Bowen & Associates Inc	
Creamer Inc		EMM.....	229
Bausch and Lomb, Houston Instrument Div.....	Cover III	Courtney/Wilson Advertising	
Cooley & Shillinglaw		Emulex Corp.....	169
Black Box Catalog.....	246	Jansen Associates Inc	
Erdner Advertising		Endicott Coil Co.....	44
Brush Magnetic Heads.....	122	R V Swinamer Associates	
Greystone Advertising		Epson America.....	247
Calcomp.....	66, 67	Ripley-Woodbury Advertising Inc	
Cal Switch.....	62	ETI Micro.....	234
Galusha & Associates		Marken Communications	
Century Data Systems.....	78, 79	Evotek.....	81-86
Jansen Associates Inc		Doug Gotthoffer & Co	
Charles River Data Systems.....	73	Foxville Communications Corp.....	24
Cherry Electrical Products.....	33	Franklin Electric.....	233
Kolb & Bauman Advertising Inc		Marken Communications	
Chromatics.....	16	Frost & Sullivan.....	206
Nucifora & Associates		Fujitsu America.....	156
Cipher Data Products.....	43	The Lone Co	
Richter & Carr Communications		Fujitsu Microelectronics.....	119
Coherent Systems.....	269	The Lone Co	
Columbia Data Products.....	147	Gandalf Data.....	197
Computrol Div of kidde Automated Systems.....	14	Wizard Associates	
Technell Inc		General DataComm.....	192
Computer Memories.....	94	Bernard Schrank Associates Inc	
Jansen Associates Inc		General Electric.....	154
Computer Graphics World.....	261	Cabell Eanes Advertising	
Computer Products Corp.....	59	Genstar REI Sales Co.....	269
Computer Sciences Corp.....	272	Warr Foote & Rose	
Bernard Hodes Advertising		Gould, SEL Computer Div.....	15
Computerwise.....	97	Group 3hree Advertising Corp	
Comtal Corp.....	64	Hazeltine.....	203
TCI		TCI Advertising Inc	
Control Data Corp.....	207	Hettinga.....	248
E H Brown Advertising Agency Inc		Heurikon Corp.....	42
CSPI.....	217	Gutzman McLaughlin McFee & May	
Amsterdam Advertising Inc		Hewlett Packard/TCG.....	46, 47
CTS Corp.....	191	Wilton Coombs & Colnett Inc Advertising	
Kennedy Advertising Inc		Hewlett Packard/Colorado Springs Logic.....	104, 105
Cuesta Systems.....	258	Tallant/Yates Advertising Inc	
Johnson Design Associates		Honeywell USD.....	260
Data General.....	238, 239	The Burns Group Inc	
Schneider Parker Jakuc		Hospital Corp of America.....	274
Dataram Corp.....	5, 80	Thompson Recruitment Advertising	
Louis Zimmer Communications Inc		Hughes.....	273
Data Systems Design.....	58	Bernard Hodes Advertising	
Tyser • Fultz • Bellack		Huntsville Microsystems.....	268
Data Technology Corp.....	10	Ikegami Electronics USA.....	221
Peter Chope & Associates		Bon Advertising Agency Inc	
Data Translation.....	201	Iklar Technology/ITECCOM.....	106
Quinn & Johnson Inc			

Imaging Technology	248	Plessey Microsystems	61
<i>Cooper/GK</i>		<i>Pawluk Advertising Inc</i>	
Industrial Development Association of Cheyenne	269	Plessey Peripherals	50, 51
<i>Ray Lansing Advertising</i>		<i>Pawluk Advertising Inc</i>	
Industrial Devices	269	Priam	48, 49
<i>Jarman Spitzer & Felix Inc</i>		<i>Cortini • Brown • Rigoli</i>	
Intel	25, 26, 27	Racal Vadic	189
<i>Chiat/Day Inc Advertising</i>		<i>Courtney/Wilson Advertising</i>	
Intellimac	55	Ramtek	Cover IV
Interface '83	265	<i>Pinnē Garvin & Hock Inc</i>	
<i>Interface Advertising Associates</i>		Real-Time Computer Science Corp	252
Interlan	199	Remark Datacom	269
<i>G Anderson Advertising</i>		<i>The Kramer Agency</i>	
Interphase Corp	187	Rockwell International	171
<i>Cope Advertising</i>		<i>Ketchum Advertising</i>	
Ithaco, Scientific Div	216	Science Accessories Corp	250
<i>Northrup and Teel Inc</i>		<i>Smith Dorian & Burman</i>	
ITT Cannon Electric	89	Scientific Micro Systems	103, 133
<i>Abert Newhoff & Burr Inc</i>		Seagate Technology	20, 21
C Itoh	255	<i>Lutat Battey & Associates Inc</i>	
<i>Lenac Warford & Stone Inc</i>		Sealectro	54
Kennedy Co	1	SEEQ Technology	45
<i>R L Thompson Advertising</i>		<i>Doug Gotthoffer & Co</i>	
Kratos Display Systems	235	Seiko Instruments USA	213, 215
<i>The Lone Co</i>		<i>Doug Gotthoffer & Co</i>	
L-COM	268	SGS	91
<i>Marketronics Inc</i>		<i>Martz & Associates</i>	
Lexidata	230, 231	Shugart Associates	12, 13
<i>Humphrey Browning MacDougall Inc</i>		<i>Chiat/Day Advertising Inc</i>	
Lundy	41	SIGGRAPH '83	263
<i>Lundy House Advertising Agency</i>		Sky Computers	194
M/A-COM DDC	237	Spectrum Control	65
<i>E G White Associates Inc</i>		<i>Barickman Advertising</i>	
Mannesmann Tally	2	Systems Strategies	180
<i>Richard Hill Associates</i>		Tanberg Data	135
Maxell	251	<i>Lenac Warford Stone Inc</i>	
<i>AC & R Advertising Inc</i>		Tandon Corp	68, 69
McGraw-Hill Book Co, Book Club Div	223, 224, 225	<i>Reiser Williams DeYong</i>	
<i>Media Buying Services International Inc</i>		TDX Peripherals	244
MDB	173	TEAC	108
Medo USA	137	<i>TVC Ads</i>	
<i>Zam & Kirshner & Geller Inc</i>		Tektronix	8, 9, 92, 93
Megatek Corp	Cover II	<i>Tektronix Advertising</i>	
<i>LeAnce & Herbert</i>		Teledyne Relays	268
Metacomp	174	<i>Michelson Advertising</i>	
Micro Memory	123	TeleVideo	148, 149
Micro Switch	115, 117	<i>Dancer Fitzgerald Sample Inc</i>	
<i>N W Ayer Inc</i>		Texas Instruments	138, 139
Monolithic Systems	110	<i>McCann-Erickson</i>	
<i>Dan Meinerz Graphics</i>		Thorn EMI	232
Mostek	70, 71	<i>Marsteller Ltd</i>	
<i>Crume & Associates Inc</i>		3M Co	205
MuShield Corp	269	<i>BBDO Inc</i>	
<i>Bell & Wilson Inc</i>		Toshiba America	124, 125
National Semiconductor Corp	140, 141	<i>Michelson Advertising</i>	
<i>Reiser Williams DeYong</i>		Trilog	100, 101
NCR Corp	28, 29	<i>Jansen Associates Inc</i>	
<i>Reiser Williams DeYong</i>		Universal Data Systems	179
NEC Information Systems	31	<i>Dayner/Hall Advertising Inc</i>	
<i>The Strayton Corp</i>		Versitron	142
Oak Switch Systems	39	<i>Pallace Inc</i>	
<i>Marsteller Inc</i>		Western Digital	74, 75, 77
Optelecom	236	<i>Leading Edge Communications</i>	
Optical Information Systems	23	Westrex OEM	254
<i>Cooper-Cameron Inc</i>		<i>GHB Advertising Inc</i>	
Panasonic	268	Wintek Corp	268
<i>Sommer Inc</i>		Xylogics	35
Penn Microsystems	269	<i>G Anderson Advertising</i>	
<i>D E Wendelboe Associates Inc</i>		ZAX	181
Penril, Data Communications	63	<i>Sales Management International Inc</i>	
<i>Business Marketing Inc</i>		Zenith Radio Corp	53
Perkin-Elmer	126	<i>Foote, Cone & Belding</i>	
<i>Marquardt & Roche Inc</i>		Zilog	243
Pertec Peripherals Corp	56, 57	<i>Pinnē Garvin & Hock Inc</i>	
<i>B J Johnson & Associates Inc</i>			

COMPUTER SCIENCES CORPORATION...

Providing information and answers for virtually every facet of the world's needs.



You are an experienced professional in the information sciences field. Your desire is to broaden your experience and enhance your career growth. You know the significance of finding just the right company to satisfy your requirements.

We're the Systems Division of CSC. Our Information and Management Systems activity is involved with the analysis design and development of embedded Computer Systems with financial, accounting, personnel, logistics and telemetry applications to the civilian and military community both in the United States and abroad.

The available services range from analytical studies to full implementation of an operating system. Our continued growth in these areas have created on-going openings in EQUIPMENT EVALUATION, SYSTEMS DESIGN AND ENGINEERING, CONFIGURATION MANAGEMENT, MODELLING AND SIMULATION, SOFTWARE DEVELOPMENT AND TECHNICAL DOCUMENTATION. These openings are in the areas of office automation, command and control, intelligence and flight test data processing.

If you are interested in a company that offers multiple career paths and many avenues for upward mobility; a company whose people are always encouraged to learn new skills and seek out the project and work location that best suit their interest and career goals, find out more about your future with Computer Sciences Corporation.

Computer Sciences Corporation
Systems Division (MC 218 CD-3)
6565 Arlington Boulevard
Falls Church, VA 22046

Equal Opportunity Employer

CSC

COMPUTER SCIENCES CORPORATION

The Hughes story continues...

Thermal Image Story.

Our story begins with you. Your talent. Your skills. Your career and Hughes Electro-Optical and Data Systems Group.

The quest to see beyond the adversities of nature no longer eludes our vision.

Hughes is producing Thermal Imaging Systems (TIS) that can see through darkness, haze and smoke. This heat sensing device projects a clear picture of a target invisible to the naked eye.

Today's TIS technology application at Hughes is the key to a number of projects: M-1 Abrams tank, Bradley fighting vehicle, TRAM DRS and the Airborne TOW system.

With over 1500 projects company-wide, Hughes offers challenge and technological growth.

If you'd like to be part of a story that's still unfolding, write yourself in.

Current openings:

Image Processing Engineers
Component Application Engineers
Circuit Design Engineers
Test Engineers
Material/Process Application Engineers
Thermal Systems Engineers
Electro-Optical Systems Engineers
Failure Analysis Engineers
Systems Analysts
Project Engineers
Servo Control Engineers
LSI Design/Test Engineers

Send your resume to:

Hughes Electro-Optical & Data Systems
P.O. Box 913, E9/W101, Dept. DC-3
El Segundo, CA 90245

Proof of U.S. Citizenship Required/Equal Opportunity Employer

**Electro-Optical
and Data Systems**

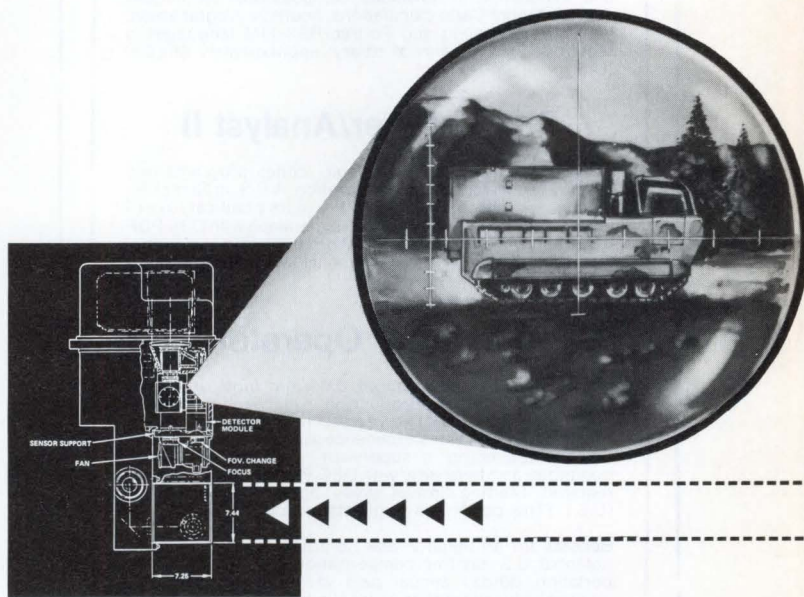
Creating a new world with electronics

HUGHES

HUGHES AIRCRAFT COMPANY

Write yourself in.

CIRCLE 165



Opportunities In Computer Programming/ Operations Saudi Arabia

The King Faisal Specialist Hospital and Research Centre is a modern multi-disciplinary specialty and referral health-care facility located in Riyadh, Saudi Arabia. We are currently seeking highly qualified professionals to operate the new CANCER THERAPY INSTITUTE, the most comprehensive and advanced institution in the Middle East incorporating extensive facilities for investigations in cancer treatment and research.

Current openings include:

Data Analyst

Applies hardware and software resources of the CTI to solve complex scientific problems generated by the scientists and staff, and maintains/directs repairs of the hardware/software systems. An M.S. in Science or Engineering with 5 (+) years experience in the application of computer systems and languages for scientific problems and experience in advanced computational techniques such as Monte Carlo calculations, heuristic programming, linear programming and Fortran/RIS-11M languages is required. Starting annual salary: approximately \$61,000 (U.S.).

Programmer/Analyst II

Designs and tests program logic, codes programs and prepares them for computer operation. A B.S. in Computer Science or related field with 5 (+) years practical experience in EDP programming work, experience with DEC PDP 11/70 and with Fortran/RIS-11M programming/job control languages is required. Starting annual salary: approximately \$41,000 (U.S.).

Computer Operator I

Will operate computer, input data and monitor system performance during production runs. A high school education with at least two years technical data processing training with 3 (+) years experience as a Computer Operator (1 of which being in supervisory capacity over other operators) and familiarity with DEC PDP 11/70 hardware is required. Starting annual salary: approximately \$28,000 (U.S.). (This position is single status contract only.)

Benefits for an initial 2 year contract in addition to the potential U.S. tax-free compensation include: free transportation; 30-day annual paid vacation; free furnished housing; educational tuition for eligible dependents; bonus pay and leave; and more.

If you wish to be considered for a position with the support operations of this Treatment and Research team, we would like to hear from you! Please call toll free 800-251-2561 or indicate the position in which you are interested by sending your resume and salary history to: **Steven H. Ludlam, Personnel Consultant, HCA - International Division, P.O. Box 550, Nashville, TN 37202.** An Equal Opportunity Employer.

HCA International Division

Home Office
Director of Marketing
Gene Pritchard

Direct Marketing
Shirley Lessard

List Rental
Robert P. Dromgoole

Classified Advertising
Maureen Sebastian
Account Representative
119 Russell St.
Littleton, MA 01460
(617) 486-9501

**New England and
Upstate New York**
Regional Manager
Barbara Arnold

Account Representative
Maureen Sebastian
119 Russell St.
Littleton, MA 01460
(617) 486-9501

**Middle Atlantic States,
Long Island and
Southeastern States**

Dick Busch, Inc.
Richard V. Busch
6 Douglass Dr., R.D. #4
Princeton, N.J. 08540
(201) 329-2424
Eleanor Angone
74 Brookline Ave.
E. Atlantic Beach, NY 11561
(516) 432-1955

**Midwestern States
and Colorado**

Berry Conner Associates
Berry Conner, Jr.
88 West Schiller St.
Suite 2208
Chicago, IL 60610
(312) 266-0008

**Western States
And Texas**

Buckley/Boris Assoc., Inc.

Tom Boris
John Sabo
Terry Buckley
2082 SE Bristol
Suite 216
Santa Ana, CA 92707
(714) 957-2552
(408) 866-8735
Terry Buckley
M. Patricia Shay
P.O. Box 278
Campbell, CA 95009
(408) 866-8735
(714) 957-2552

*(TM)

With the COMPLØT® Series 7000 Digitizers

You get user configuration controls not ordinarily found in competitive digitizers



Prices start at \$2,950*

the Houston way

Only the Series 7000 digitizers give you 40 user selectable or host computer controlled features for the ultimate in tailoring these microprocessor-based digitizers for specific applications.

- Variable digitizing rates up to 160 coordinate pairs per second in 8 selections.
- Resolutions of .001", .005" or .01".
- Incremental mode with 64 step sizes from 0.005" to 0.315".
- Manual or host computer control.
- Single point data averaging.
- Fixed or relocatable origin.
- English or metric dimensioned positions.
- Built-in annunciator on/off.
- Parity on/off.
- 8 Bit Parallel/BCD or Binary.
- Dual port RS-232-C.

These are a representative few of the multitude of combinations available. But the Series 7000 story isn't over yet. Consider four sizes from which to choose with active areas of 12"x12", 17"x24", 36"x48" and 42"x60" PLUS a complete border for user definable menus — no need for a separate extra-cost menu pad.

All COMPLØT Series 7000 digitizers are translucent for backlighting. And while the 12-button cursor is standard, single-button cursor, inking/non-inking stylus or magnifying cursors are available. You also get the Houston Instrument commitment to accuracy, $\pm 0.005"$ right to the edge of the active area. And no demagnetizing (biasing) is ever necessary.

Wouldn't you like to finish the COMPLØT story? Get complete information on the COMPLØT Series 7000's scores of user configuration controls.

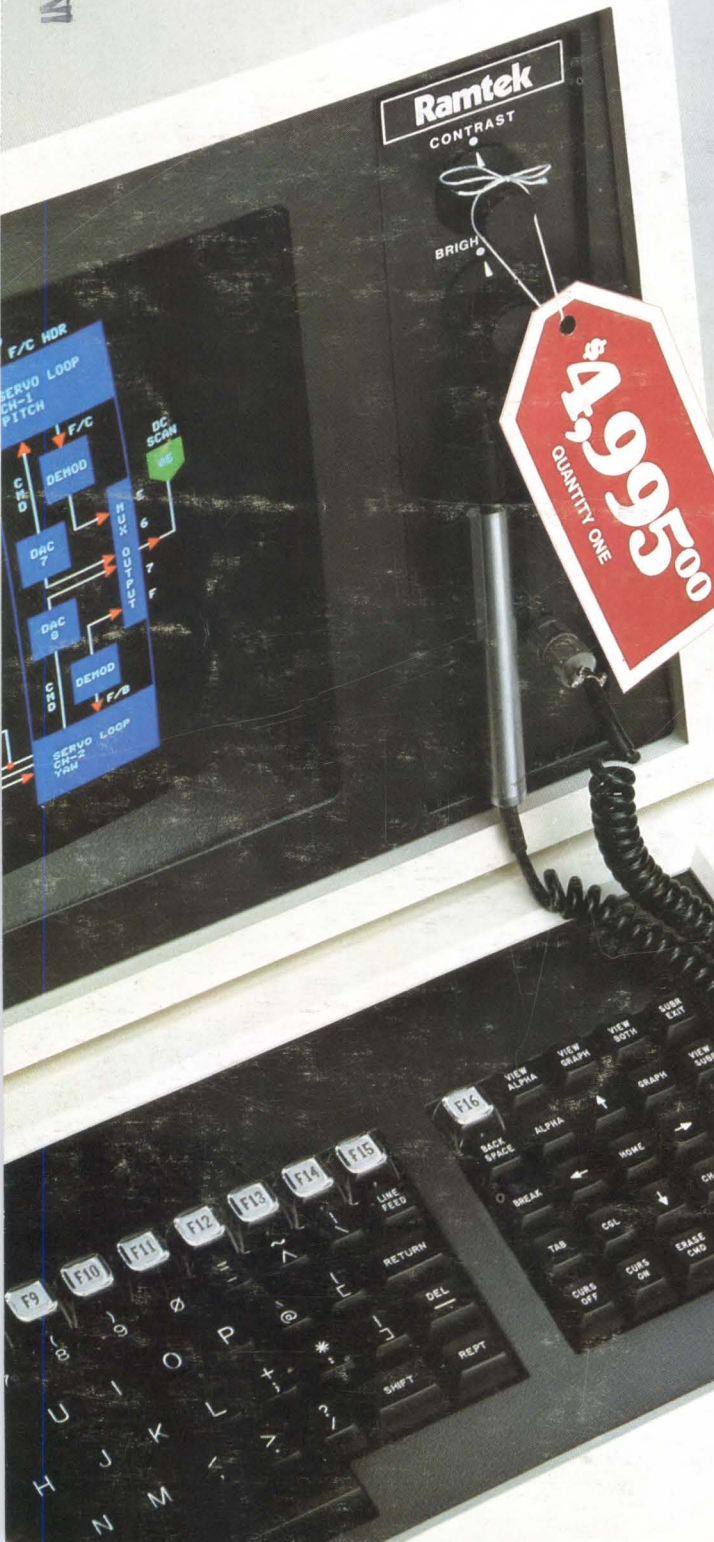
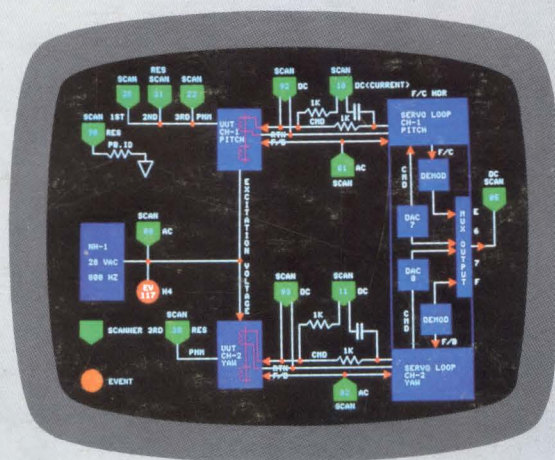
For the name, address and phone number of your nearest representative, write Houston Instrument, 8500 Cameron Road, Austin, Texas 78753. Phone 512-835-0900, or 1-800-531-5205 if outside Texas. In Europe contact Bausch & Lomb Belgium NV., Rochesterlaan 6, 8240 Gistel, Belgium. Tel 059-27-74-45. Tlx 846-81399.

BAUSCH & LOMB 
houston instrument division

* Registered Trademark of Houston Instrument.
* U.S. Domestic Price only.
FCC class B tested.

4N009A

THE BEST HAS JUST
BECOME THE BEST DEAL.



\$4,995.00
QUANTITY ONE

Ramtek's popular 6211 Colorgraphic Terminal is now just \$4995*. This versatile desk-top unit is ideally suited for the majority of color graphic applications in CAD, science, business, and control systems. Rack mounted (without monitor), it's even more of a value at just \$3995.

Need data terminal functions, too? The companion 6221 with full VT 100™ compatibility is priced at just \$5995. Plus there's a 12% discount available through March 31, 1983 on systems with both color printer and 35mm slide camera.

The price of quality has never been lower. Volume discounts are also available. For details, call our office nearest you. Or, contact us at 2211 Lawson Lane, Santa Clara, CA 95050. (408) 988-1044.



OUR EXPERIENCE SHOWS.

- World Headquarters**—Santa Clara, CA (408) 988-2211
- European Offices**—Amsterdam (31) 2968-5056; London (8956) 76211; Cologne (2234) 78021
- U.S. Offices**—Dallas, TX (214) 422-2200; Los Angeles, CA (714) 979-5351; Seattle, WA (206) 575-1600; Chicago, IL (312) 397-2279; Houston, TX (713) 774-2233; McLean, VA (703) 893-2020; Denver, CO (303) 694-0758; Cleveland, OH (216) 524-1882; Upper New York/Canada (716) 425-1742; New Jersey (201) 238-2090; Florida (305) 645-0780; Boston, MA (617) 273-4590; Atlanta, GA (404) 252-5066.

*Light pen sold separately.

VT 100 is a registered trademark of Digital Equipment Corporation.