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SEPTEMBER 1983

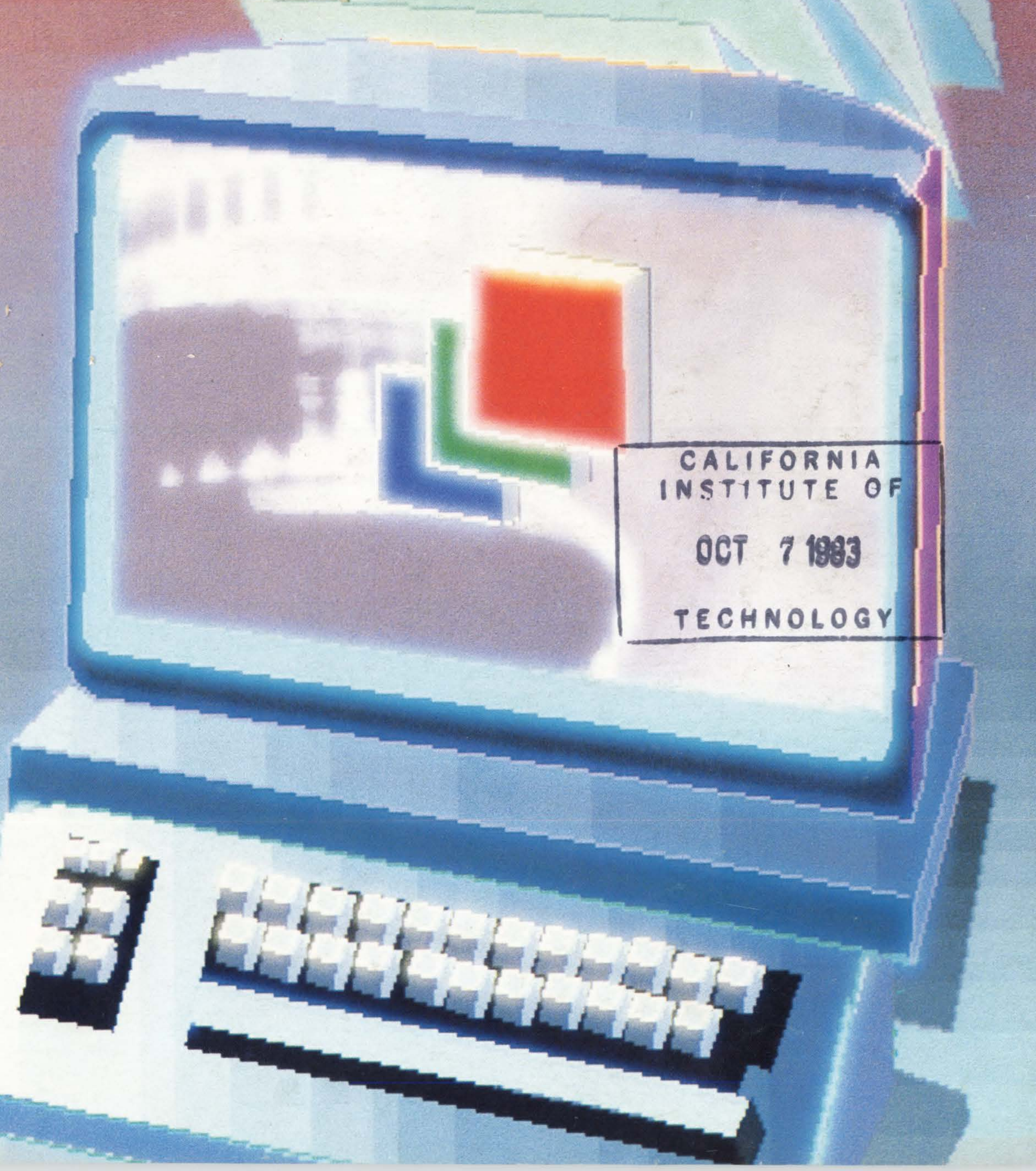
COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

TERMINAL AND PRINTER TECHNOLOGY

SPEECH RECOGNITION IS A REALITY

UNIX IN REAL TIME



Whizzard® 1600s. The newest addition to Megatek's family of graphics products. High resolution, interactive graphics and alphanumeric desktop terminals that give designers and engineers everything they need – right at their fingertips.

Whizzard 1650 color and 1645 monochrome terminals are ergonomically-designed with a 19″ tilt and swivel monitor and detachable keyboard. Both models provide powerful local graphics functionality including translation, scale, rotate, clip, complex polygon fill, pick and peripheral event queuing.

In addition, the 1600s feature VT-100/52 compatibility so you can perform a complete range of alpha terminal functions. Software development and debugging and document generation to name just a few. Two terminals in one.

Whizzard 1600s let you easily handle difficult electronic or mechanical CAD applications through a wide variety of available third party software. And, thanks to our WAND™ software, 1600s are compatible with every other Whizzard, right up to the top of our line. If that's not enough, you can even use our device independent and intelligent TEMPLATE® software as well. Total flexibility.

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CIRCLE 1

Model 6455 Cartridge Tape System

Loaded with Features — Loaded with Benefits.

Kennedy products have always provided innovative new features. And these features have always provided added benefits and convenience for the user. For instance, our Model 6455 offers these features and benefits:

Feature: Start/Stop Operation

Benefit: Drive can emulate a ½" tape drive by providing the ability to perform selective file back-ups, file-restructuring, journaling and software updates.

The drive is effectively a ½" Tape Drive in a smaller package.

Feature: Hard Read Error Spec. of 1 in 10^{11} bits.

Benefit: Best data reliability of any tape cartridge drive. Gives the user confidence in the integrity of the back-up medium.

Feature: On-board Diagnostics

Benefit: Drive can be tested off-line with no test equipment required. Use of S.A. also lowers the MTTR.

Feature: Cartridge Jam Protection

Benefit: Protects the cartridge from damage if cartridge jams. This is accomplished by sensing a current surge and then disabling the motor, thus insuring that the cartridge will not be damaged.

Feature: High Density Recording

Benefit: Storage capacity of 23 MB on a single cartridge.

Feature: Optional industry standard ½" tape interface.

Benefit: Operates with existing tape couplers and software. The drive operates as though it were a ½" tape drive without having to modify existing hardware or software.

By now you can see what we're driving at. Model 6455 is full of unique features and benefits for you. For the complete story, write or call us today.

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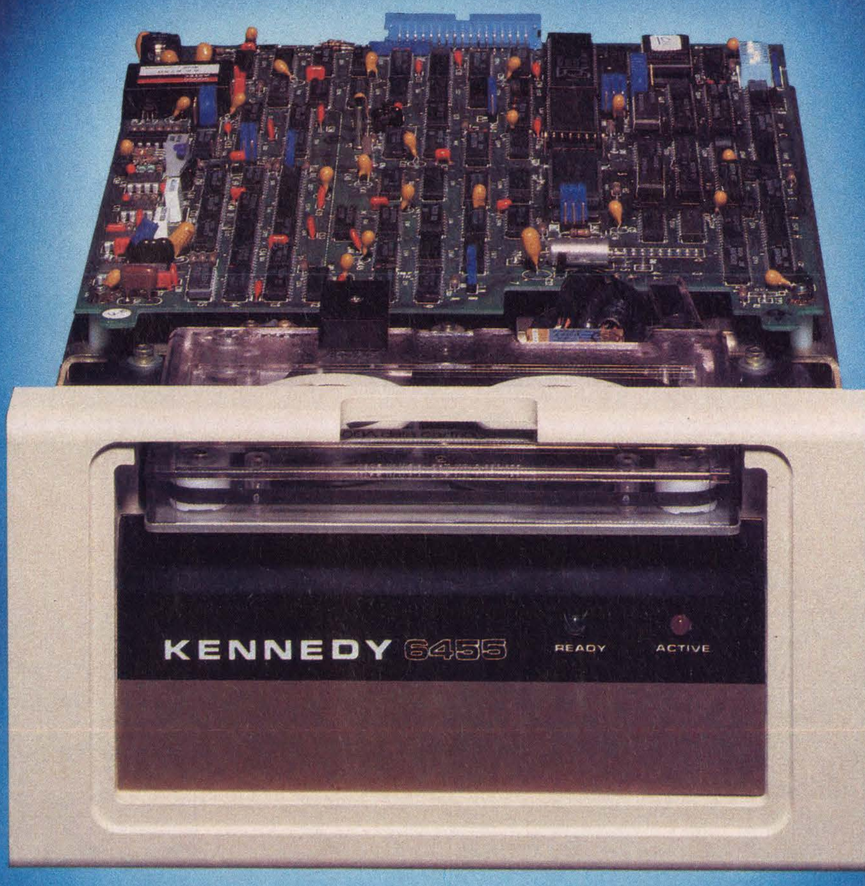

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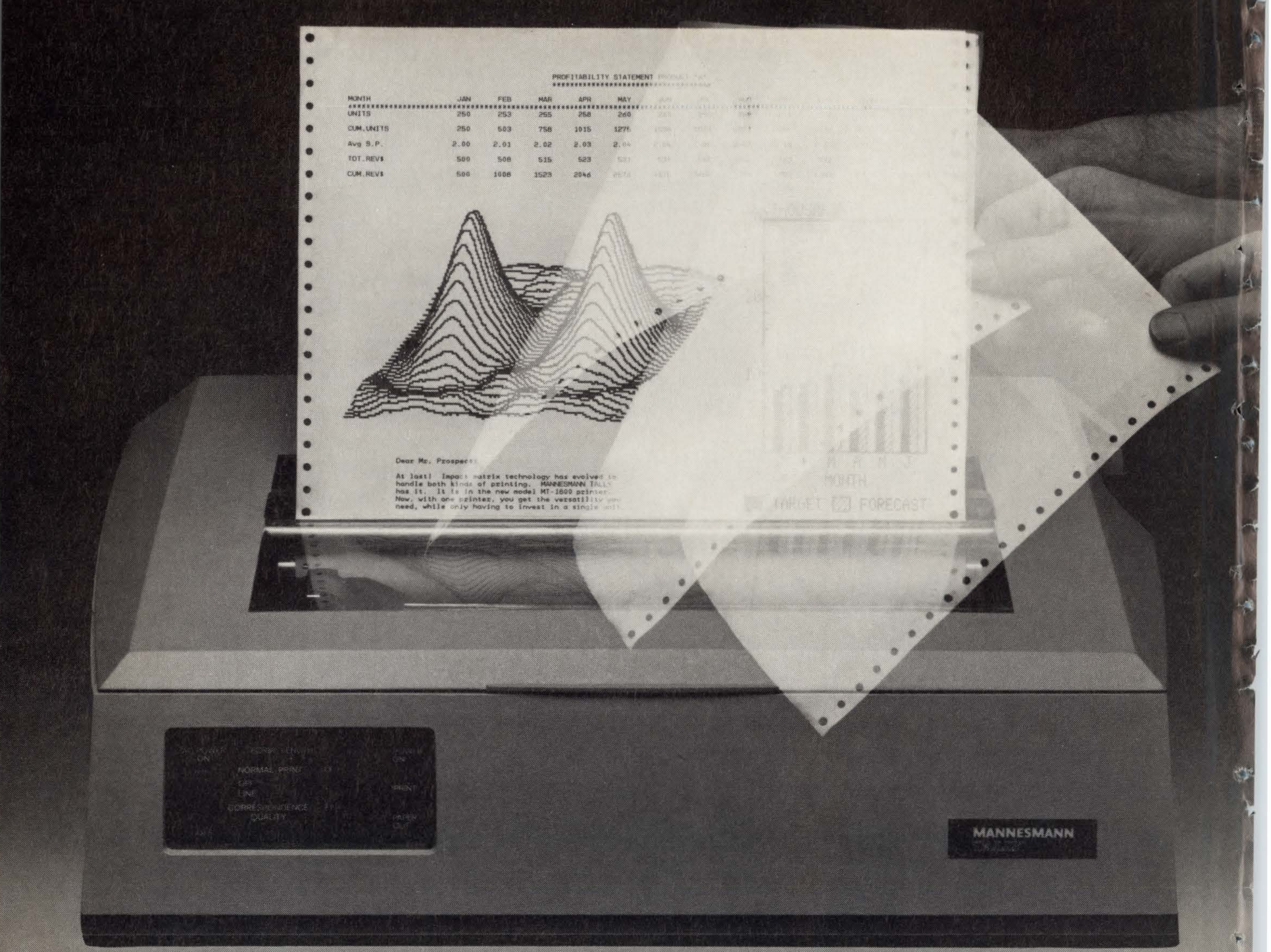
MANNESMANN

UP FRONT

International technology exchange to parent 100M-byte tape drive

One of the first products to emerge from a cross-licensing and technology exchange agreement in principle between Data Electronics and Tandberg Data is expected to be a half-inch tape cartridge drive with a capacity of over 100M bytes. Probably available by the first quarter of 1984, the drive is based on Data Electronics prototypes but uses patented Tandberg Data moving-head technology. As part of the agreement, 3M Co, which licenses Data Electronics to manufacture tape cartridges, will receive royalty-free use of the cartridge design. Although both Data Electronics and Tandberg Data are founding members of the QIC standards committee, neither company will comment on the possibility of formulating new standards.

Intelligent controller will gain momentum from system interface

A technology exchange agreement calling for joint development of "the first controller that cost-effectively implements" the small computer system interface (SCSI) on a 5¼" streaming cartridge tape drive has been completed by NCR and Archive Corp. SCSI, an intelligent bus used in Winchester disk drives and other peripherals, is being reviewed by the American National Standards Institute as a possible official standard. The controller will permit a system integrator to expand a system or link peripherals to the system with only minor software modifications. A single host adapter will support various peripherals. The controller will only be available with the Archive Scorpion 5¼" tape drive, which will be supplied to NCR for its business computer system.

Lee Data acquires Wordtronix

Terminal system designer and manufacturer Lee Data Corp has reached an agreement in principle with Wordtronix, whereby Lee Data will acquire the advanced word processing system manufacturer. A version of the Wordtronix word processor is expected to be integrated into the existing Lee Data terminal system product line as part of the company's expansion into areas of the data processing industry. Recently, Wordtronix formulated an agreement with Remington Rand to acquire its trademark for office products. Wordtronix will market future products under that trademark.

Stolen memory devices appear

Certain memory devices stolen from raw stock at one of Motorola's Semiconductor Product Sector assembly plants are showing up in the marketplace, according to the company. These memory devices include a quantity of 64K dynamic random access memories (DRAMs) and a smaller number of 16K DRAMs. The parts are packaged in plastic, only partially tested, and not marked with the company's name. Motorola believes its logo, and possibly those of competitors, are being used on the stolen parts. Although the company is making every effort to recover the parts, and some of the people implicated in the theft have been apprehended, the company is alerting its worldwide customers to buy only from authorized distributors or the company's salespeople. Because the stolen devices are not fully tested and some may even be rejects, the company cannot verify that they will meet performance and reliability standards.

UP FRONT

Pretriggers

Software has been traded for hardware in Megatest's MegaOne VLSI test system. A complete set of testing electronics is dedicated to every pin of the device under test. Reportedly, this tester-per-pin architecture alleviates many of the problems inherent in shared-resource testers.

A commercial program that performs mathematical manipulation in symbolic form was exhibited by Inference Corp at the National Conference for Artificial Intelligence. According to the company, it is the first marketable product that is a direct application of artificial intelligence to a real-world problem.

Network hardware and software can connect unlike systems via Ethernet with Interlan's NTS10 terminal server. This allows information sharing among personal computers and the mainframe data base, and also resolves long-standing distributed environment problems.

A graphics processor for low cost, high performance CAD/CAM systems was introduced by Telesis Systems at NCGA '83. A dual-ported memory architecture enables picture storage with a 2000- x 1000-pixel resolution claimed to be 4 to 16 times greater than for current low end systems.

A high performance, virtual disk multi-user microprocessor development system, the Emunet-2 provides the full power of a VAX 32-bit minicomputer to each project team member. Emulogic's system can support up to 60 hardware/software workstations at up to 5000′ from the host, and at 1M-baud data transfers.

Op amp architecture that provides oscillation-free operation over the full range of gain settings is promised for Comlinear's CLC200 series. A dc-100-MHz, −3 dB bandwidth remains virtually unchanged over inverting and noninverting gain settings of 1 to 50.

The latest in a series of EXORset systems, Motorola Semiconductor Products' model 110 is an 8-bit development system and OEM desktop controller based on the MC6809. It can be used as either a complete system integration and development tool or configured for OEM applications.

Piggybacking operating systems—letting one run as a subtask of another—is said to solve the common microcomputer problem of file incompatibility. Datalex has piggybacked the UCSD p-System on IBM's PC-DOS.

A Unix-based 32-bit superminicomputer, the Pyramid 90x has a system architecture with elements derived from the Reduced Instruction Set Computer (RISC) machines produced at the University of California, Berkeley. A 125-ns CPU, 32-bit internal bus, and intelligent peripheral handlers provide an efficient environment for high level languages.

Plug-in communication adapters on a network controller simplify the support of different networking schemes. With Able Computer's system, the electrical interface to support Ethernet can be easily changed for token passing, X.25 packet switching, or IBM SNA-type communications.

Faster application program execution results from swapping speed-critical portions directly into the control store of Lisp Machine's Lambda computer. A microcompiler simplifies microprogramming routines.

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NEW... from DATARAM

MOTOROLA VERSAbus 1.0 MB ADD-IN

Not just more capacity; more capability

Motorola's 68000 is a winner, and using this popular microprocessor in a VERSAbus/VERSAboard configuration is a smart move. Dataram's new single-board 1.0 MB DR-680 can make it even smarter. Increased single-board memory capacity means lower power, less space, higher reliability, and lower cost...and the DR-680 provides a lot more!

More speed: Ability to perform match cycles reduces access/cycle times by allowing immediate reading of data registers when adjacent words/bytes are accessed.

Advanced error handling: The DR-680 provides an on-board control and status register (CSR) which allows program control of ECC functions and contains the diagnostic information required for error analysis. The CSR can be read or written via the VERSAbus. Additionally, the DR-680 greatly increases reliability by performing error "sniffing" and error "scrubbing" during refresh operations.

Availability: Best of all, the 1.0 MB DR-680 is available now. And it comes with Dataram's standard one-year warranty.

For more information, send in the adjacent coupon or, for faster response, call Dataram today at (609) 799-0071.

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COMPUTER DESIGN®

System technology

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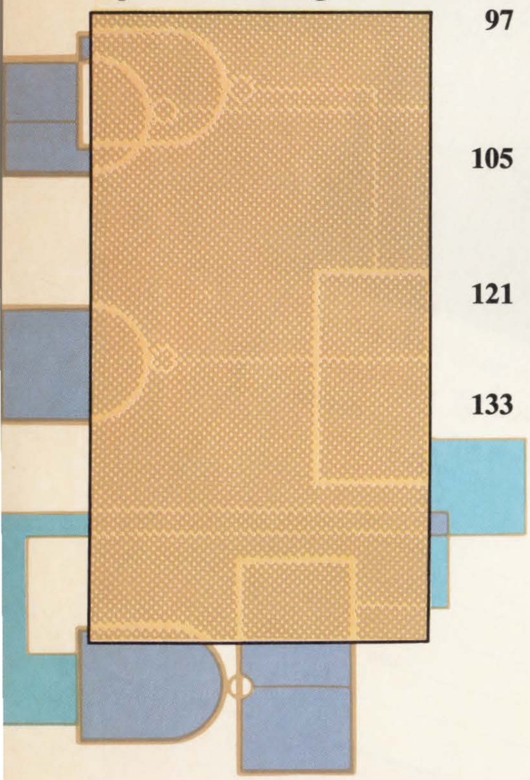
System design



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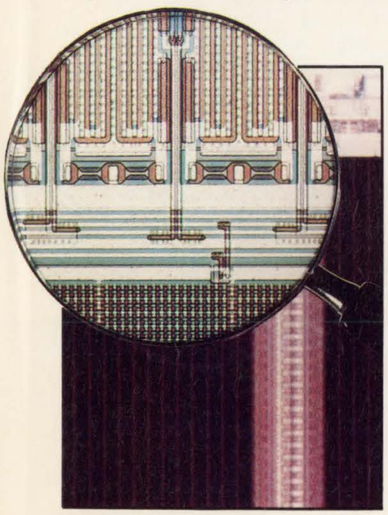
ISA/83

Vol 22, No 10
Sept 1983

This month's cover, depicting terminal and printer technology, was created by Mark Lindquist on the Digital Effects Video Palette III and D-48 high resolution camera system. The artist's conception was based on material supplied by Advanced Micro Devices.

Special report on terminal and printer technology

System components



Page 220

Departments

Designers' preference survey*

*Appearing in Domestic issues only

Editorial reviewer for part of this issue:

E. Vargas-Ortega

INTRODUCING Ω500 DISPLAY CONTROLLER

Last year we brought you the Ω400 Display Controller, with 1024 x 768 resolution, 8-bit planes and one million pixels/second vector drawing speed. This innovation introduced state-of-the-art color graphics performance from a single circuit board, providing OEMs with the ultimate in reliability, flexibility and price.

Today, Metheus has moved even further ahead of the competition with the introduction of the Ω500, the first of a new generation of color graphic display controllers.

New standards in resolution, refresh and ergonomics. Still on a single board.

The Ω500 Display Controller sets a new standard in graphics display ergonomics, bringing you brighter, crisper images and truly flicker-free displays. It has the highest resolution available, 1280 x 1024 at 60Hz non-interlaced refresh, the rate needed to drive the latest 100 MHz monitors.

Ω500's bit-slice processor supports drawing speeds ranging from 1.5 million to 120 million pixels per second.

And, once again, Metheus' advanced graphics technology is neatly packaged on a single board for exceptional reliability and efficiency. On-board signature analysis circuitry and extensive self-testing capability ensure consistent, dependable operation and fast diagnosis of any malfunction.

A Writeable Control Store (WCS) feature allows OEMs to customize the controller's instruction set for a wide range of specialized customer applications.

And Ω500 is compatible with Ω400 software.

Let Metheus put you a generation ahead.

The Ω500 is available as a controller alone or as an integrated graphics subsystem incorporating a high resolution monitor. And it is available for immediate delivery in quantity.

If color graphics are a part of your product, you owe it to yourself and your customers to talk to Metheus today.

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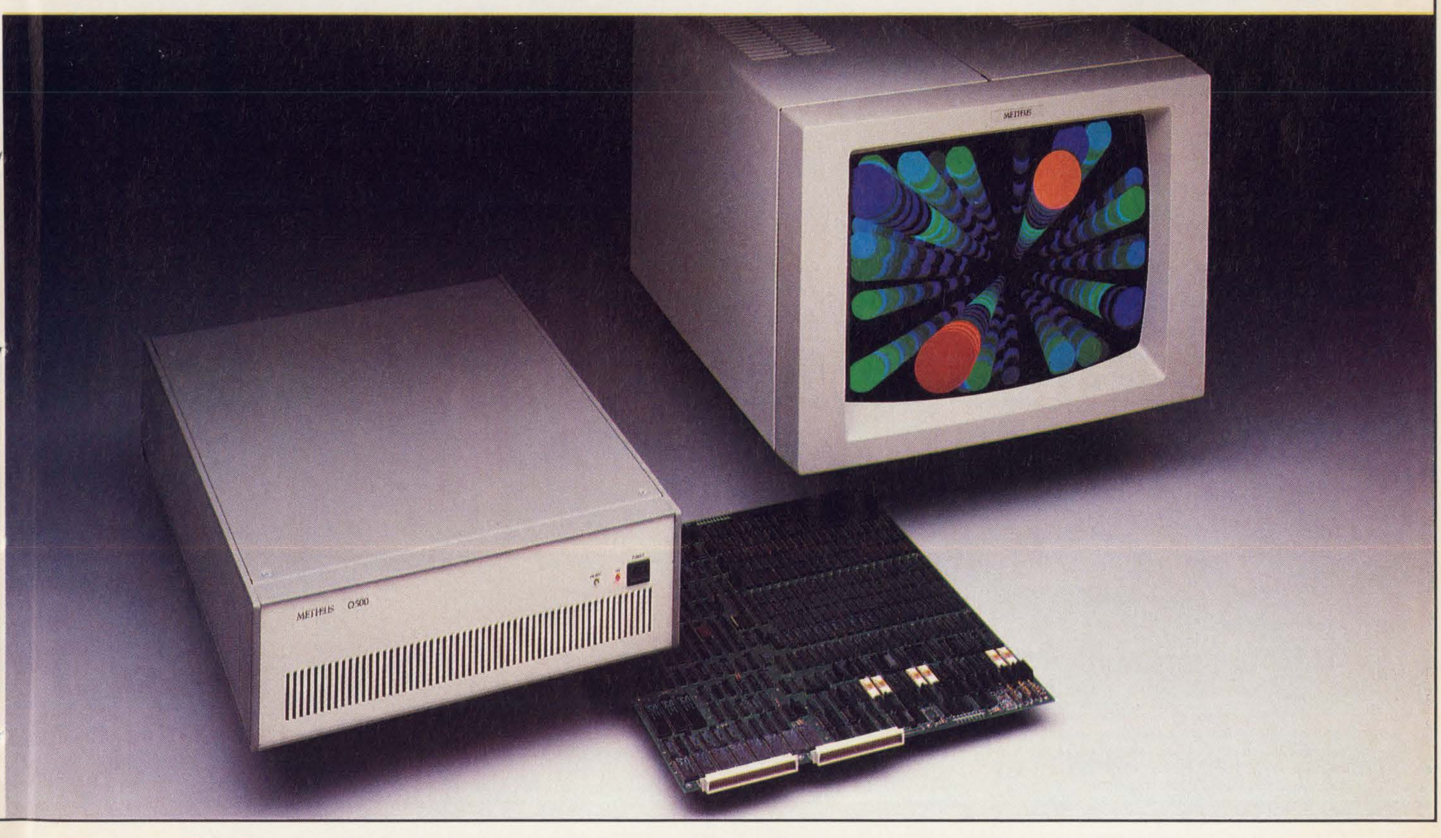


CIRCLE 5

ACADEMIA AND THE SHARK

Almost every summer, Hollywood releases a gory shark movie presumably to scare vacationers off the beaches and into the movie theaters. It turns out, however, that sharks aren't nearly as dangerous as Hollywood portrays them. Apparently, only about 10 people throughout the world are killed by sharks each year. In our view, the really scary aspect of shark movies and newspaper stories is that marine biologists admit they often exaggerate the shark threat to secure lucrative research funding and movie jobs for themselves.

In the computer field, universities and other special interest groups pursue a similar strategy: scare people half to death and then offer to save their lives for a fat fee. The latest example of a great white shark in our industry is the Japanese national programs in information technology. One program is aimed at developing a computer a thousand times faster than current supercomputers, and the other (the Fifth-Generation Computer Project) is aimed at developing computers that embody artificial intelligence functions. All of a sudden, nearly every major university and independent research laboratory is offering to help counter the threat from this impending economic Pearl Harbor—provided, of course, the American taxpayer picks up the tab.

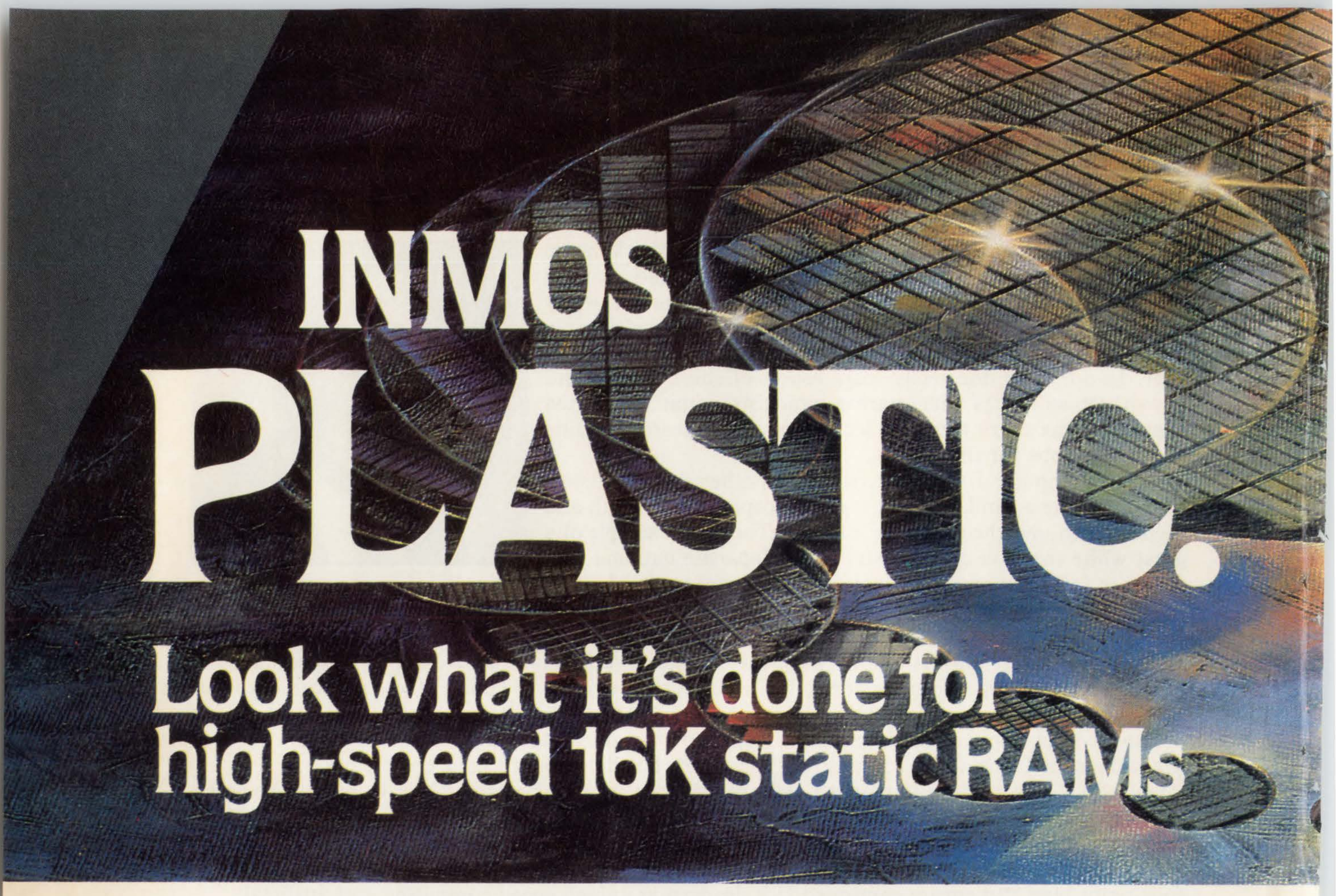
The latest example of academic scare tactics to cross our desk is a news release from Massachusetts Institute of Technology. Though its headline doesn't have the brevity of "Jaws-3D," it is obviously intended to be equally frightening. It reads: "MIT Computer Expert Predicts Havoc for U.S. Information Industry if Japan Realizes Even Fraction of its Goals."

After setting the stage by reminding us of Japan's impact on the U.S. automotive industry, Professor Michael L. Dertouzos of the MIT Laboratory for Computer Science proposes a four-point plan "to ensure continued U.S. leadership in high speed computing and artificial intelligence." Two components of the Dertouzos plan—asking for government handouts and for a relaxation of the antitrust laws—are already being implemented. A government funded effort led by the Defense Advanced Research Projects Agency is currently awaiting congressional approval. In addition, the newly established Microelectronic and Computer Technology Research Corporation involves 16 different corporations and therefore requires a benevolent antitrust posture by government. In making these proposals, Dertouzos shows political acumen. Proposing something already being done lends it credibility and reassures politicians that they are probably on the right track.

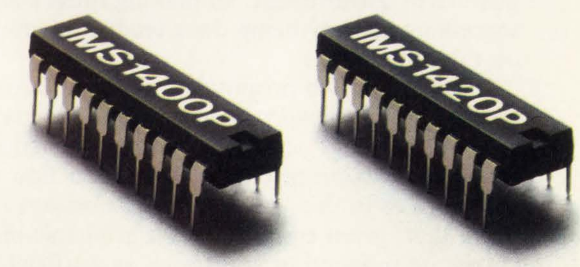
In his other two proposals, however, Dertouzos may have overplayed his hand. Essentially, he proposes a handicap race in which academia and industry compete by different rules. He suggests an "open policy" toward university exchanges with foreign researchers, but he also proposes curtailment of proprietary information flow out of industry to foreign competitors. By trying to rig the rules in this way, Dertouzos betrays a lack of confidence in university research. We would think that, given equal funding, academic research holds two important advantages over corporate research in areas such as artificial intelligence. First, universities can take a more basic and long term approach because they are free from the pressure of showing a quick return on investment. Second, universities can more easily pull together the multidisciplinary expertise required for good research in such areas as speech recognition. After reading the MIT proposals, however, we're not so sure.

As we've said in earlier editorials, the Japanese research threat may not be as great as people like Dertouzos would have us believe. Though the Japanese now dominate the world in mass production, quality control, and, increasingly, in product development, they haven't yet cornered the market in Nobel Prizes. And, as Dertouzos himself claims, "Japanese plans for a high speed computer were based on ideas copied from MIT." Though there is a real risk of the United States' eventually losing computer industry leadership to Japan, we think that institutions like MIT demand too high a price to counter this exaggerated threat. Or perhaps we just like to live dangerously, because we don't intend to consult a shark expert the next time we swim in the ocean, either.

Michael Elphick
Editor in Chief



High Speed...



Here's good news for designers who need fast 16K static RAMs...at an affordable price. INMOS has combined plastic packaging with its proven track record in fast 16K static RAMs, resulting in a new low-cost plastic family.

This new plastic family includes the fast static RAMS you've grown accustomed to in our ceramic package. Featuring access times of 45 and 55ns, the IMS1400P-45 and IMS1400P-55 16Kx1 static RAMs are lower in price than their ceramic counterparts, without sacrificing INMOS' high level of quality and reliability. Also available are the 45ns IMS1420P-45 and the 55ns IMS1420P-55 4Kx4, for applications requiring a by-4 organization.

When you need the combination of low power and low cost, choose one of our new "L" products. The IMS1400P-70L (16Kx1) dissipates only 495mW active and 83mW standby, while offering a 70ns chip-enable access time. You can also get identical performance for the IMS1420P-70L, with a 4Kx4 organization. Also available are 100ns versions of these low-power products, priced to provide

HIGH-SPEED 16K STATIC RAMS

Part Number	Organization	Speed (ns)	Power (mW)	
			Active	Standby
IMS1400P-45	16Kx1	45	660	110
IMS1400P-55	16Kx1	55	660	110
IMS1420P-45	4Kx4	45	605	165
IMS1420P-55	4Kx4	55	605	165

COMPUTER DESIGN

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A Forth analysis

As a Forth user, I was pleased to see the article, "Call Forth for Realtime Control Programming," by Al Whitney and Marvin C. Conrad (Apr 21, 1983, p 81). Unfortunately, there were several misstatements in the examples.

This probably stems from Forth's use of spaces as word delimiters, and some words being mistaken for punctuation. I think it is worthwhile to print corrections for the examples as well as expand on the language's temporal aspects.

First of all, I disagree with the authors' statement about Forth's readability. True, it is probably easier to write unreadable code in languages like Forth or C. However, Forth's use of structures makes bad Forth easier to figure out than bad BASIC. Forth can actually be written in a more readable style than any other language I have seen. Good Forth style demands factoring tasks into simple steps whose names will lead to easily read code. I can illustrate this with the author's example from p 83. The definition of QUADRATIC could have read

```
: QUADRATIC DUP 52 * 15 - * 10 - ;
```

Let's assume this calculation performs some kind of transducer correction. As this is a correction, let's call the word DO-CORRECTION instead of QUADRATIC. Furthermore, let's assume there is a constant called A-D that puts the address of an A-D converter (the transducer's output) on top of the stack. Moreover, let's use the word CCPRINT (for cursor-controlled printing), which takes an argument describing a CRT window in which a number is to be printed. A word might be defined to get the current reading from the transducer:

```
: GET-DATA ( --- n) This is stack notation.
( before --- after ) A-D @ ;
```

By entering the following directly from the keyboard, the system designer could make a word continuously show the corrected transducer value during troubleshooting or calibration:

```
: PRINT-IN-WINDOW1 ( n --- )
WINDOW1 CCPRINT ;
: DISPLAY-DATA ( --- )
BEGIN
GET-DATA DO-CORRECTION
PRINT-IN-WINDOW1
?TERMINAL UNTIL ;
```

The word ?TERMINAL is part of the standard word set and returns a Boolean true if any key is depressed. This allows termination by pressing any key on the terminal when the calibrations are finished. This definition certainly has reasonable readability. Of course, as with any language that uses procedures or subroutines, one has to look at previous definitions to get the real details of the action.

On p 84, the < BUILDS -- DOES > construct was misprinted (< BUILDS -- DOES > in Fig-Forth and Poly-Forth, CREATE -- DOES > in 79 standard). I think the definition should have read

```
: TABLE (n --- < name > compile time)
<BUILDS 0 DO , LOOP
DOES > SWAP 2* + @ ; (n< name >---n2
runtime)
```

This is a defining word whose temporal aspects give beginners a lot of trouble. The words between < BUILDS and DOES > execute at compile time and the words between DOES > and ";" execute at runtime. < BUILDS creates a new name in the dictionary and the compile time code executes, in this case to set up and initialize a data structure. DOES > links the runtime code to each new word created with TABLE.

This is a poor example in several ways. First, the table's size is restricted to the stack's size at compile time, a value that varies depending on nesting of control structures during compilation. Second, it is rather poor style to create a data structure and initialize it all in one fell swoop. It's fun to see that it can be done, but woe to the poor person who takes over when you move on from Cogsly Cogs to Spacely Sprockets.

I would also like to mention that the authors' statement that it is syntactically impossible to mix assembly and high level code could be misleading. The statement is true at runtime. (Well, almost true. It is possible to cause assembly code to select and execute a Forth word.) But, at assembly time, the entire Forth vocabulary is available for address calculation and conditional assembly. After all, the assembler is written in Forth. Also, high level definitions can be created in the assembler vocabulary, resulting in very flexible macros. The addresses of Forth variables and the values of constants are all directly available during assembly. This, combined with single pass structured assembly, makes assembly language use a breeze.

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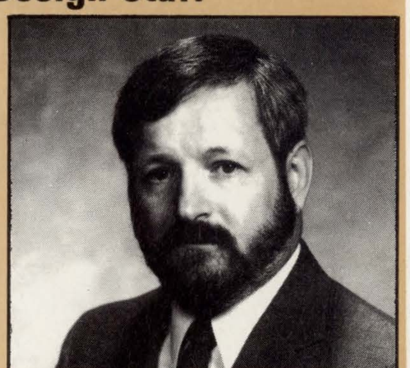
Bond joins Computer Design staff

John Bond has joined *Computer Design* as a Senior Editor. He brings with him an extensive high technology background from *Electronic Design*, where he was New England editor. Previously, John was computer editor for *EDN*, and an associate editor with *Mini/Micro Systems*. He has also been a marketing communications manager at Digital Equipment Corp, an engineer at General Dynamics, and a semiconductor sales engineer at Texas Instruments.

John graduated from the U.S. Naval Academy with a BS in engineering. He served with the U.S. Air Force as an electronics engineer and attained the rank of Captain.

John is working out of *Computer Design's* Littleton, Mass offices,



where he specializes in microprocessors/microcomputers, development systems, interface, and test & measurement. He is responsible for coordinating the magazine's System Design section.

Forth has flaws

As a Forth user, I feel that I must comment on the rosey tone cast in the Whitney and Conrad "Call Forth" article. It is obvious to everyone involved in computing today that what may be a feature to one user will be a flaw to another. This is true not only for two users working on different applications, but for two people working on the same instrument. Forth is perhaps the best example of this.

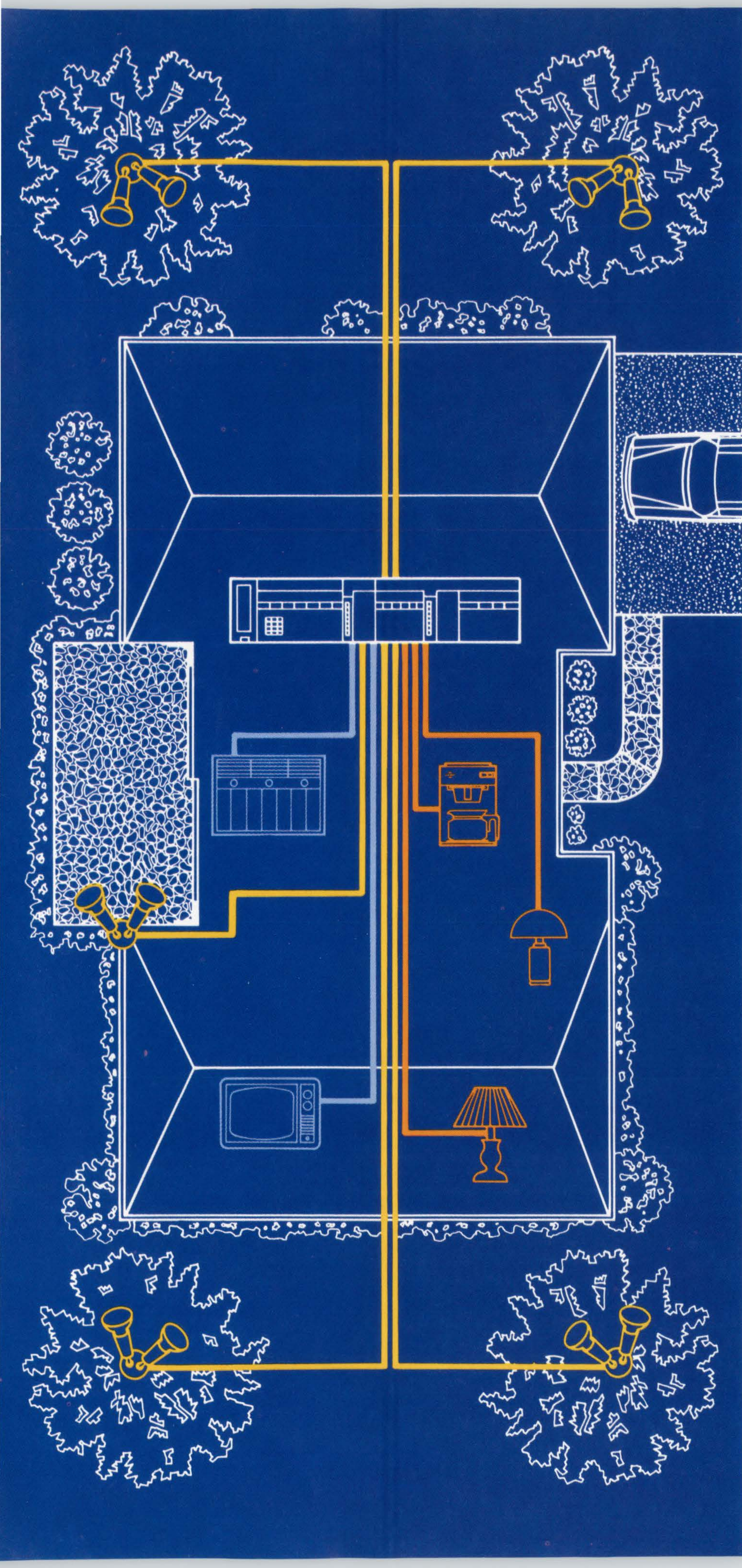
It is true that Forth may be faster than a FORTRAN program, but that is a mark against the FORTRAN compiler rather than a point for Forth. Forth cannot be faster than properly written assembly code, since Forth must not only execute the base level words (or nucleus) in machine code, but must also interpretively determine which code to execute. A user written assembly routine is

(continued on page 21)

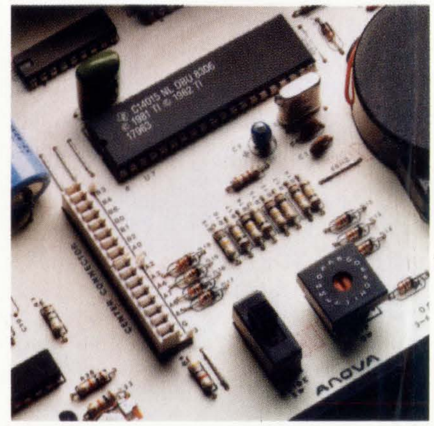
Texas Instruments and Anova team up for peace of mind when you're away... and extra convenience when at home.

- **High functionality, low cost** of TI's TMS7040 8-bit microcomputer contributes to Anova's pioneering intelligent electronic control for modern homes *(Page 2)*.
- **Two new additions** to TMS7000 single-chip microcomputer family combine outstanding NMOS performance with CMOS low-power dissipation *(Page 3)*.
- **Dependable, economical assistance** that helped Anova achieve cost-effective design is available from any of the TI Regional Technology Centers *(Page 4)*.

▶



Only TI's demands



It was a tall order. A microcomputer with large, on-board memory. On-chip timer. Sufficient I/O ports. With performance capability that would minimize hardware to hold costs down. And meet overall system size constraints. TI's TMS7040 8-bit, single-chip microcomputer fit the bill.

Result: Anova Electronics' sleek, new remote Control Center brings a greater degree of security to American homes and small businesses. Total convenience in the operation of lights and appliances. And significant energy savings. Whether anyone is on the premises or not.

Outstanding cost/performance ratio

The Anova Control Center handles up to 16 individual lights and/or appliances. Instantly. Or automatically by program which can vary from day to day. With immediate display of what's going on, including the status of each light or appliance.

The TMS7040 has 128 bytes of on-board RAM that readily accommodate all necessary programming. Plus 4K of on-board ROM which, with the TI TMS1000 4-bit microcomputers in the outlet modules, provide the intelligence for the "status" feedback.

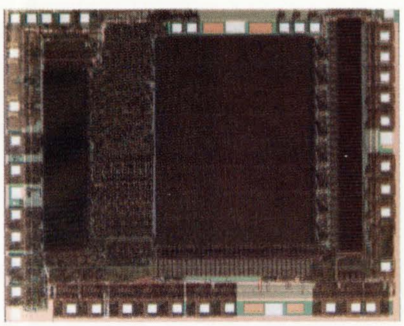
◀ **Electronic control of home or business** is now possible with new Master System designed by Anova Electronics. The Control Center utilizes TI's TMS7040 8-bit microcomputer to handle infinitely variable control of up to 16 lights or appliances. When Control Center is linked with Protection and Telephone centers, the highly functional TI microcomputer provides all necessary unification.

7000 8-bit μC passes stiff design of new Anova home control center.

TMS7000 Strip Chip Architecture yields smaller, microprogrammable chips.

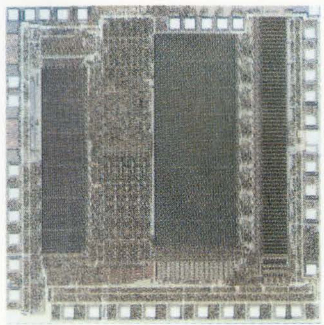
TI's unique Strip Chip Architecture Topology (SCAT) gives the TMS7000 family today's smallest 8-bit microcomputer chip. One that is low cost, microprogrammable, and that can be customized.

SCAT eliminates as much random logic as possible in favor of defined individual sections — such as control, ALU, and registers — for easy interconnection. For example, registers for the timer, I/O control, interrupt handling, ALU, etc., are arranged in a strip. Any additional 8-bit registers can be added to the strip with the eight interconnect lines already being available. There is no need for randomly locating additional registers and then routing interconnect lines all over the bar.



TMS7040 Microcomputer Strip Chip derived from TMS7020 Chip

SCAT allows TI to develop new family members easily from the basic TMS7000 chip. The TMS7040 microcomputer chosen by Anova was economically created from TI's TMS7020 by separating the memory border and inserting an extra 2K of memory.



TMS7020 Microcomputer Strip Chip

Another development using SCAT technology is TI's new TMS70120 microcomputer. The memory area has been expanded to 12K bytes of ROM and brings TMS7000 family advantages to a broad range of larger, more complex applications. Check your TI sales office for availability.

Because a control ROM replaces random logic for defining the instruction execution sequence, the original TMS7000 instruction set can be replaced by new, user-defined instructions. In some applications, such microprogramming can substantially enhance performance and improve the efficiency of on-chip program memory.

Contributing to TMS7040 functionality are 32 configurable I/O ports that permit the display and keyboard multiplexing. And, an internal, on-chip timer that provides for different delays within the software. As well as three fully utilized interrupts.

So much functionality packed into a device enabled Anova to hold parts count down, simplify its design, maximize reliability, and achieve cost goals.

Effective design help from Regional Technology Center

In designing the trim, compact Control Center, Anova relied on TI's convenient Regional Technology Center.

Anova engineers determined what functions the Control Center was to perform — defined the specifications — and left the development of the software code up to the specialists at the TI center. For both the TMS7040 and TMS1000 microcomputers.

By contracting to have the center perform the programming, Anova was able to utilize its engineering staff more effectively. And eliminated the need to invest in a development system.

For more details on TI's growing TMS7000 8-bit and popular TMS1000 4-bit microcomputer families, check numbers 1 and 2 on the coupon.

New TMS7000 members combine CMOS/NMOS advantages.

Well suited to telecommunications, portable instrumentation, and high-performance consumer products are two unique additions to the TMS7000 series. Both combine the performance capabilities of TMS7000 NMOS microcomputers with a CMOS typical power dissipation of only 50 mW at 5 volts. Reducing power even further are a "wakeup mode," dissipating 4 mW (typical), and a "halt mode" that typically requires only 2 mW.

The new TMS70C20 is a CMOS version of the TMS7020, with 128 bytes of RAM, 2K bytes on-chip ROM, 3- to 6-V operation, and 3 MHz nominal operating frequency.

The new TMS70C00 is a ROM-less 8-bit microcomputer intended for software development.

Engineering samples of both the TMS70C20 and TMS70C00 are available now in 40-pin, 600-mil, dual-in-line plastic packages.

Coming soon: New TMS7000 UART capability.

A serial port in TI's new TMS7041 microcomputer enhances I/O and communications capability. Otherwise identical to the TMS7040, the TMS7041 operates in several modes. One permits interface with Universal Asynchronous Receiver/Transmitter (UART) peripherals as well as multiple microcomputers. Serial links are implemented by standard asynchronous protocols. In the unique "isosynchronous mode," transmission rates are 16 times those of the asynchronous mode. A serial I/O mode can be used to expand I/O lines using external shift registers and to communicate with peripherals requiring a non-UART serial input. Check with your TI sales office for details on availability.

(continued from page 16)

always faster than the same procedure written in Forth. The IF. . .ELSE. . .THEN construct does help give structured code, but many real assemblers are available with the same features.

Forth also lacks features that help realtime control instruments. The Forth users here have found it impossible to perform the simplest of Forth words under interrupt control; all interrupt handlers must be written in assembly code. The closest approximation to realtime execution of Forth words depends on Forth's multitasking ability, but there still may be unacceptable delays before the interrupt handling task is executed. Because the multitasking feature depends on other tasks voluntarily releasing the processor, it is possible that the interrupt handler may never execute.

It is true that Forth code is unreadable. Saying that Forth code needs to be read less than other code is not true. Forth code needs just as much maintenance as any other language. And, having two people who cannot read each other's code working on the same project can be futile. It is often easier for Forth programmers to write their own routines to perform a function another person has already coded, than it is to try to understand the other person's code.

The only "feature" that I cannot imagine as a benefit to anyone is the disk file structure, or more accurately, the lack of structure. The disk is treated as a collection of screens, 1024 characters in length. It is possible to have anything on any screen, and it is possible to have code anywhere on a disk. The most common complaint I hear about Forth is that it is impossible to keep track of code once it is written.

The data acquisition systems used here keep data in Forth disk format only as long as it takes to copy these data onto a normal file structured disk on the minicomputer used to perform data reduction and archival storage. File structured Forth routines are being sold to reduce this problem, but are only a paste-up fix of an inherent defect.

This is not a condemnation of the Forth language. It is meant to show readers, who may decide to choose Forth as their language, the other side of the coin. Forth is not the panacea of instrument control. It has faults, but can be a useful tool after its limitations are understood.

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Missing statements

We enjoyed the premier issue on automation and control (Apr 21, 1983) and found some useful nuggets of information. We would, however, like to make some observations on the article "Control Software for Factory Automation" by John Sylvan (p 119).

First, the equations on p 124 are missing a proportional factor, K, which would factor the proportional contribution to output to an appropriate amount. In the examples given on p 124, K is assumed to be 1. The correct form of the third program should include line 35 K=1 and the output equation should be line 100 AOT(2,0)=K * (E + I + R) + C. Without this tuning constant, the controller gain could be too large, resulting in sustained or unstable oscillations.

Second, the third program listing on p 124, which includes the derivative term, may "bump" the process when the program is first begun. This occurs because the derivative term uses the error factor from the previous iteration to calculate the rate of change. Line 60, which equates the previous error with the current set point during the initialization phase, is as dangerous an assumption as equating it with zero. What is needed is an equalization cycle prior to beginning control that allows the derivative term to settle down. Line 60 should be F=S − AIN(1,0) and line 65 should be WAIT 1. Thus, the final form should be as follows:

```
10 S=5
20 C=5
30 I=0
35 K=1
40 P=1
50 D=1
60 F=S−AIN(1,0)
65 WAIT 1
70 E=S − AIN(1,0)
80 I=I + P * E
90 R=(F − E) * D
100 AOT(2,0)=K * (E+ I + R) + C
110 F=E
120 WAIT 1
130 GOTO 70
```

Kevin R. Grantham
Walter R. Rager
Sun Refining and Marketing Co
PO Box 920
Toledo, OH 43693

Changing equations

*As Mr Grantham and Mr Rager pointed out, the PID control program on p 124 is missing two statements. The first is a proportional factor and the second is an equalization cycle. To include a proportional factor, line 100 could read 100 AOT(2,0)=K * (E + I + R) + C.*

In the simple case where proportional contribution is factored directly to the output, or K=1, the K factor disappears and the line would indeed be 100 AOT(2,0)=E + I + R + C.

An actual program, however, would need the proportional factor K to correctly scale the proportional contribution into the output. In effect, the K factor acts as a programmable gain that the user can alter to achieve the proper control.

The equalization cycle avoids "bumping" the process when the program is first begun. Bumpless transfer eliminates the sudden jump in the control output. With equalization, the program would change from 60 F=S to

60 F=S − AIN(1,0)
65 WAIT 1

As it stands, the PID control program on p 124 is the minimal program requirement for a PID control loop. Once the standard equation is available, it becomes simple for the control engineer to try out various control options with the addition of only a program line or two.

John Sylvan
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Norwood, MA 02062

In search of computer humor

Gary Auguston, director of computer and information systems here at Penn State, has assured me that "there is no humor in the field of computer science. It is a most serious business, bereft of any humor." So far, I have little evidence to the contrary, but I am searching.

For an anthology [that I am preparing] I would welcome contributions of humor in the sciences, historic and contemporary, especially in computer-related sciences. The ordinary man's disquiet about computers has sometimes been expressed in contrived jokes that bring the resented superiority of the expert down to earth. How are jokes changing with the spread of personal minicomputers?

I would welcome anecdotes, biographical notes, witty accounts, cartoons, parodies, verse, self-deception, and hoaxes. Especially sought are items that, while humorous, also have value in the history of a science, providing insight into changing attitudes or illuminating personalities. Please fully identify all contribution sources.

Robert L. Weber
104 Davey Laboratory
University Park, PA 16802

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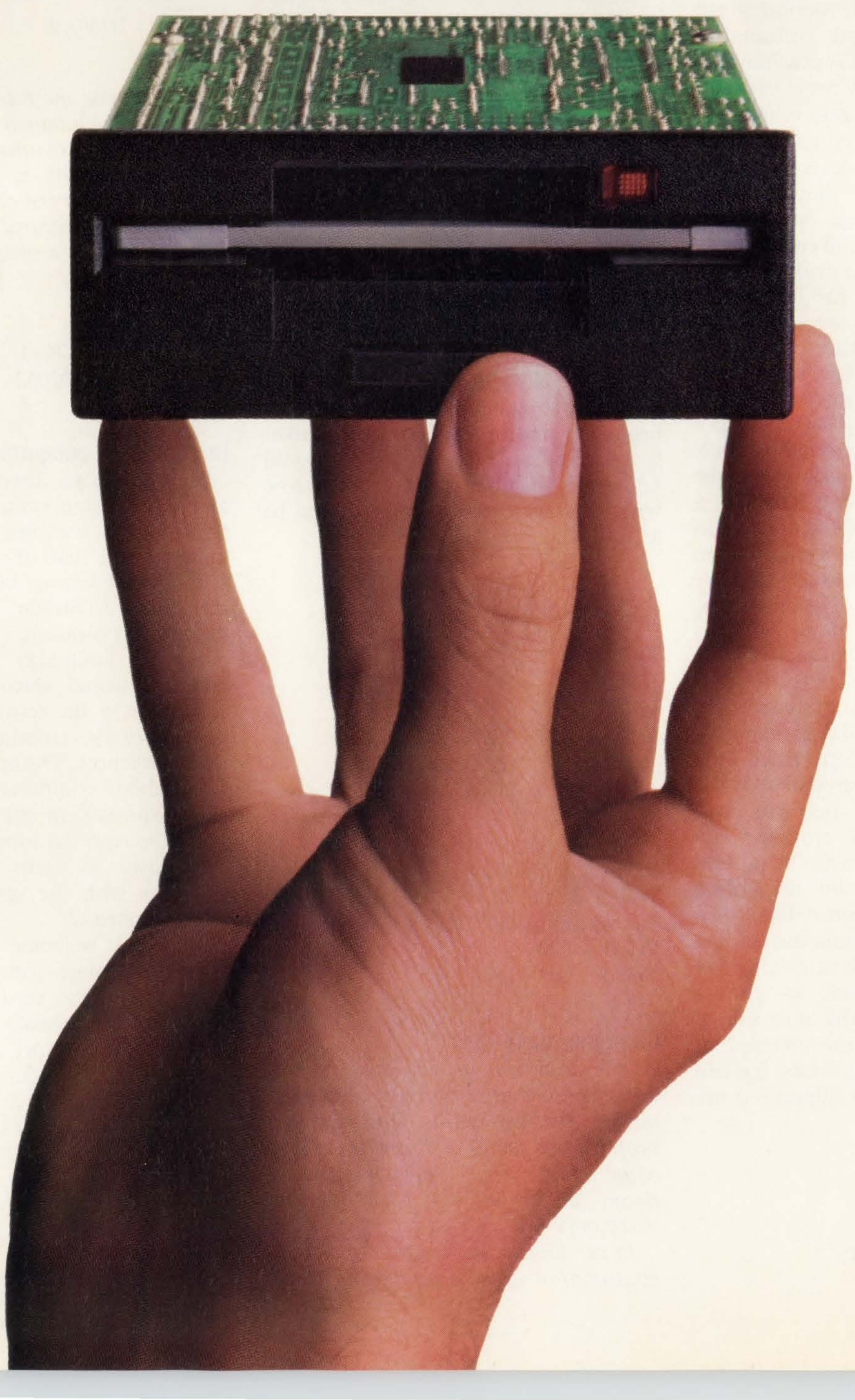
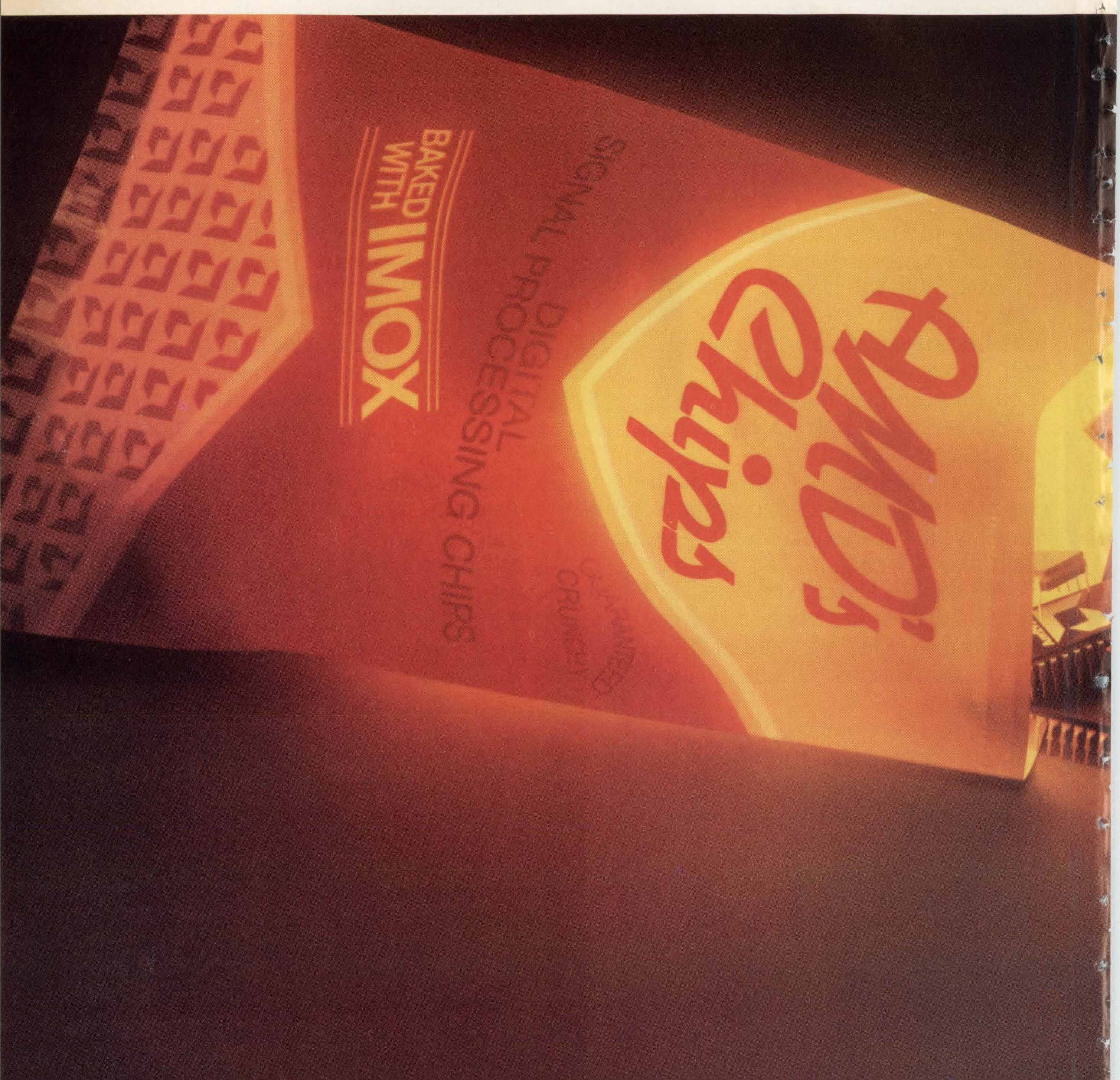


THE WORLD'S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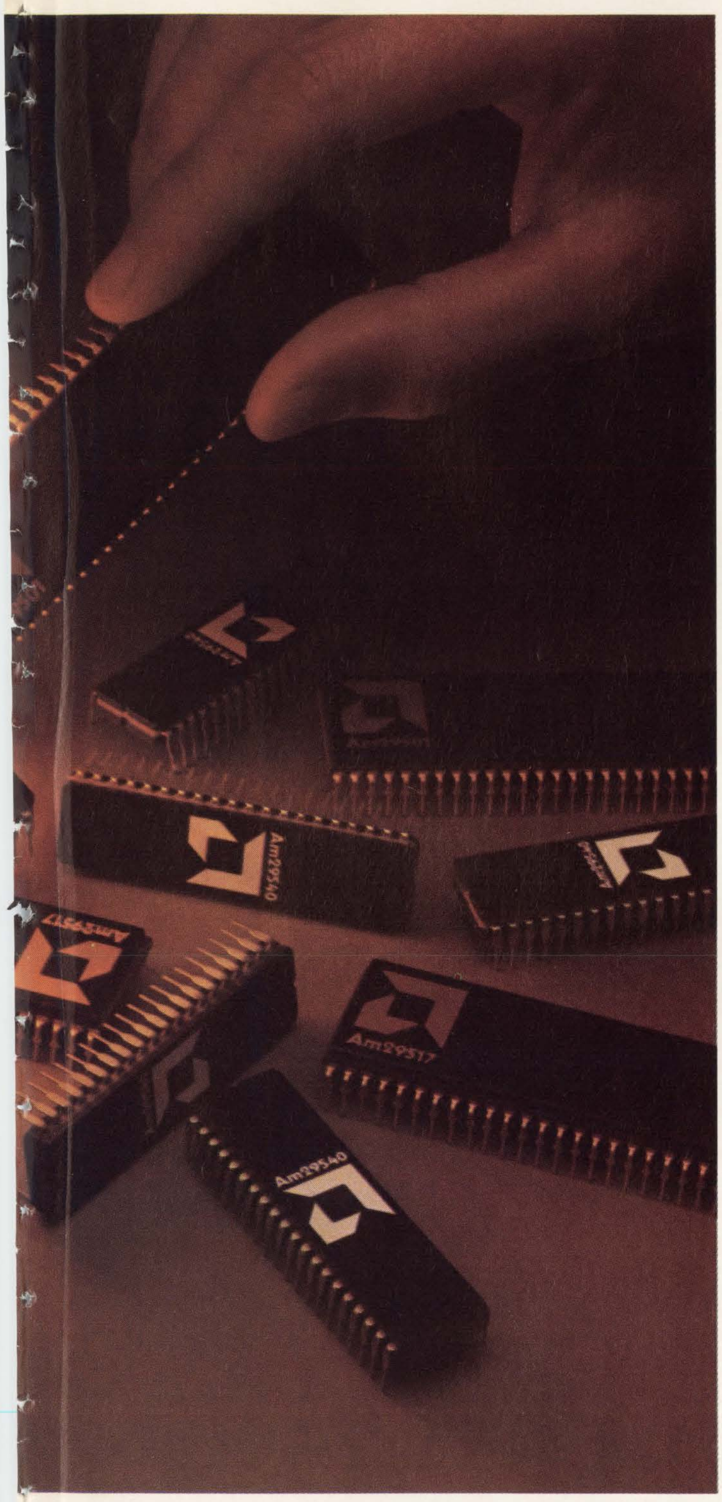

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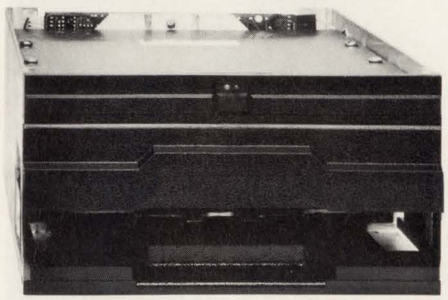
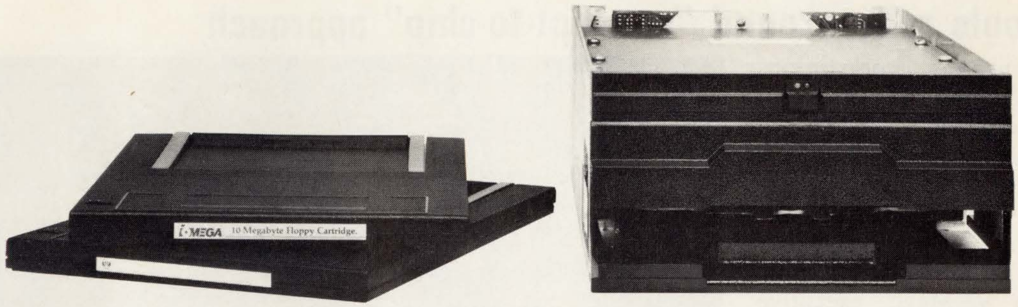
CIRCLE 13

FRONT.



BACK.



Any Way You Look At It, Superior Storage Solutions.

What you see here are two different views of one very different drive.

Sure, the camera angle on each view is the same. But "front" and "back" refer, in this case, not to a photographic perspective, but rather to an *applications* perspective. They refer to the fact that this revolutionary cartridge drive is the most versatile and economical storage device you can buy for a full range of applications—from back-up and archival storage to up-front primary storage.

Front View: High Reliability Primary Mass Storage.

There are several powerful reasons to seriously consider the Alpha 10 as a primary mass storage device. First of all, each cartridge stores 10 Mbytes of data—easily matching capacity with today's Winchesters.

But just as important, the Alpha 10 matches the Winchesters in reliability, thanks to several IOMEGA innovations in flexible disk and removable cartridge technology. As for versatility, the unique cartridge format of the Alpha 10 speaks for itself—a straightforward approach to library management and data interchange.

Back View: High Versatility Back-Up And Archival Storage.

The Alpha 10's advantages for back-up and archival storage are just as impressive. For instance, a 10 Mbyte Winchester file can be dumped onto a single Alpha 10 cartridge in literally minutes, not the usual hours. You can look forward to a new standard of reliability that is integral to our design. And, because our cartridges are the most inexpensive on the market today, archival storage doesn't cost you an arm and a leg.

Overview: The Careful Evolution, And Immediate Availability, Of A Drive Design Revolution.

Any way you look at it, the Alpha 10 is a breakthrough in data storage device design. Actually, it's a series of breakthroughs, including non-contact head-to-disk interface, high linear bit densities, a run-length limited code that compresses the data stream from the host, and closed servo control of the head positioning, all to achieve the economy and versatility of flexible disks with the capacity and reliability of hard disks.

But the best part of the technology is that it's here, now, packaged and available in OEM quantities. Get the whole story, today, on the Alpha 10 from IOMEGA.

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CIRCLE 14

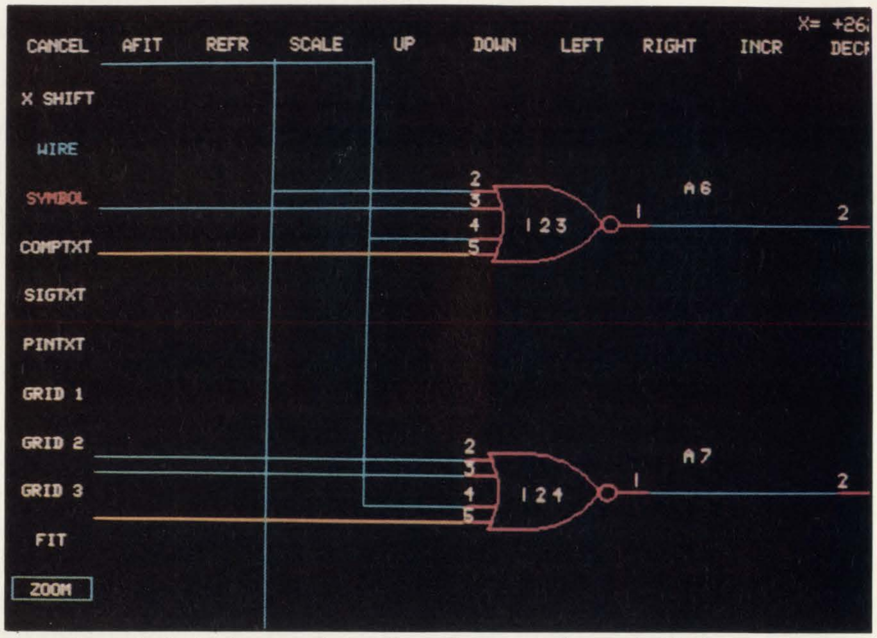
Design tools rally around "concept-to-chip" approach

Today's engineering workstations are seriously lacking in basic design automation tools that would let a designer create conceptual designs quickly. Currently, the tools are mainly being used to improve existing designs. That sharp criticism was voiced recently by keynote speaker John S. Mayo, executive vice president of Bell Laboratories (Murray Hill, NJ), at the Design Automation Conference.

The technical meeting and exhibit was held June 27-29 in Miami Beach, Fla. It is the prime technical meeting for engineers in computer aided design who are working in a broad spectrum of application fields ranging from electronic to mechanical systems. Mayo emphasized that design automation tools are absolutely essential to the future of electronics, citing the 32-bit Bellmac-32 as one very large scale integration (VLSI) microprocessor whose design and debugging would have been virtually impossible without design automation tools.

"Despite good progress in design automation," said Mayo, "experience has taught us that some tough problems still remain. We need to have more powerful aids to enable designers to crystallize their ideas into initial designs." According to Mayo, "Even well-worked areas such as layout and testing could be further improved. Architecture design and functional design need strengthening." He added, "We also need more powerful tools to manage change, especially to deal with multiple design changes that occur at different stages of the design process."

As if to answer his call, many companies at this year's conference exhibited what they touted as more powerful systems that make a better effort to integrate the basic design tools. One such system is the series 8000 from Cadtec Corp (San Jose, Calif). Claiming that current standalone workstations only address the needs of the individual engineer and



A portion of a logic diagram designed on the VIA series 100 is displayed with a portion of one signal net highlighted. When TRACE is activated, signals tied in a net are displayed in a special color.

fail to address the larger issues of project design teams, Cadtec engineers developed an integrated design and management system that they believe meets both these needs.

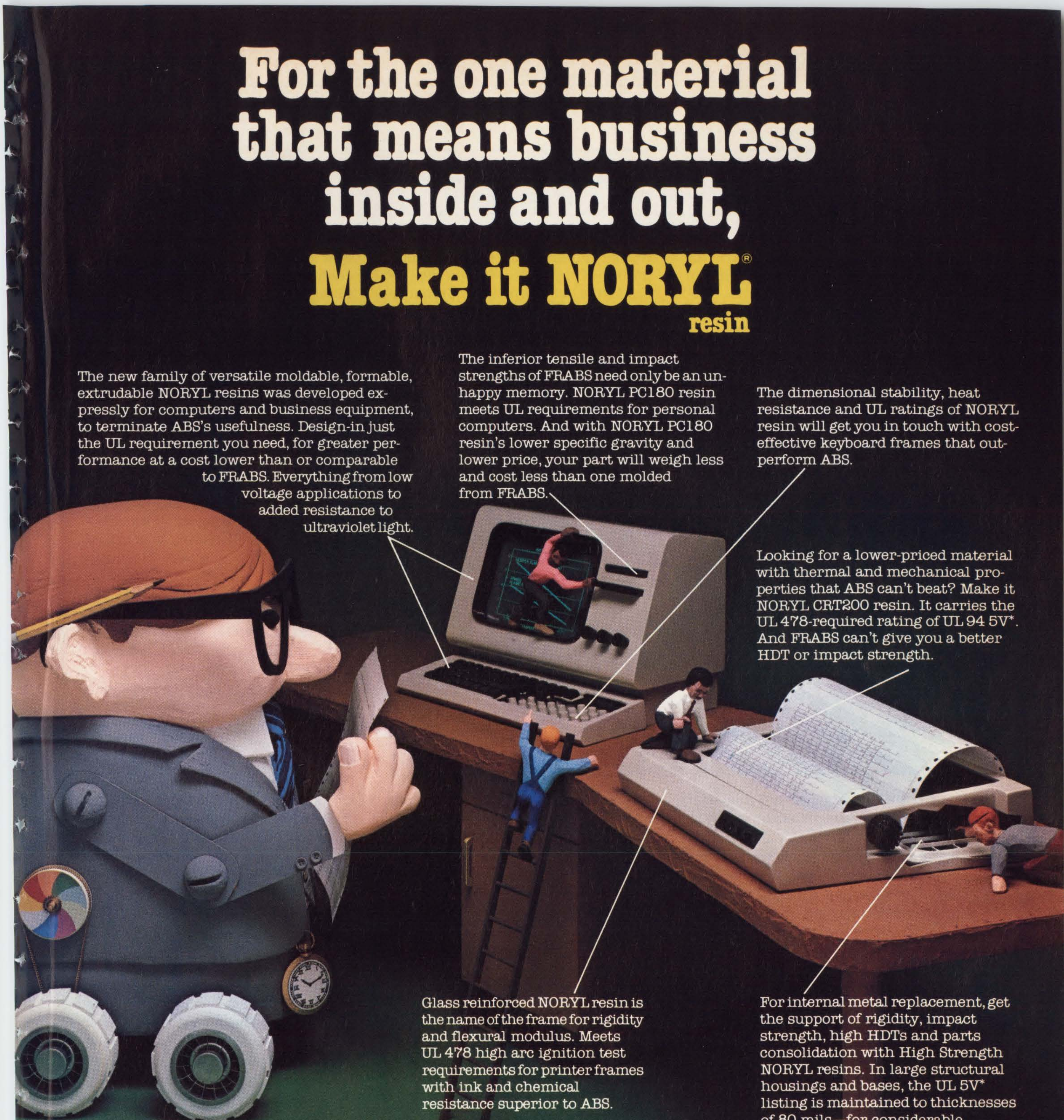
Addressing large logic design

The series 8000 is said to be the first systems approach to large logic design that integrates workstations to a central projects host computer through extensive system software and a project database system. The system integrates the company's model 8200 interactive graphic workstations, model 8500 graphic office stations, and extensive system software and application tools with a Digital Equipment Corp VAX-11 host computer.

Cadtec's founders are former IBM and Intel engineers who were responsible for large project design. To them, large team-oriented projects have a different set of requirements than those of individual engineers. For example, some of the problems confronting the project leader of a large team effort might include partitioning the design and assigning it to individuals, reintegrating the separately developed design partitions when complete, controlling the access and distribution of project data, checking the operation of one partition with the others, monitoring the progress of the overall design, communicating and enforcing particular design standards and design methodologies, coordinating releases to manufacturing and testing, coordinating the work of the project team members, and communicating with the various team members. The individual workstation does not address these project-oriented issues.

The model 8200 is a 68000-based workstation that runs on a Unix operating system with a project-oriented database management system. This system interfaces to the VAX-11 series host computer. The workstation includes 1M byte of memory, an 8" Winchester disk, a color or monochrome 19", 1024 x 1024 CRT display, the 68000 dedicated applications processor, and three 2900 bit-slice processors

(continued on page 30)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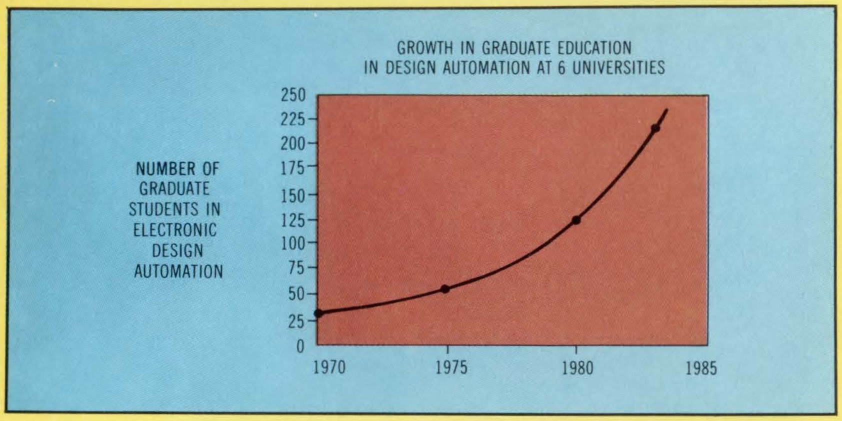
"Concept-to-chip" design
(continued from page 28)

Academia increases interest in CAD/CAM

John S. Mayo's call for a unified design automation approach for developing VLSI chips is being answered on several fronts. Besides industry's contribution of more powerful design automation tools, academia is playing an increasingly participatory role to keep design automation in step with electronic circuitry as chips increase in complexity and speed.

In his keynote address at the conference, Mayo pointed to the role that universities are playing: "Progress in design automation is emerging from both a growing design automation industry and from increased activity in the universities. The design tool industry is helping meet the needs of various innovative companies, especially small- to medium-sized companies that cannot afford the high costs of developing their own design automation." According to Mayo, some companies that cannot afford to make the investment alone are participating in joint ventures to develop design automation instead of buying standard products from the design automation industry. In addition, Mayo said that more and more universities are aggressively pursuing design automation.

Mayo cited the results of an informal sample of six university programs—from the University of California at Berkeley, Carnegie-Mellon, MIT, Stanford, Cal Tech, and Illinois State University—where the number of graduate students working in design automation has grown sharply since 1970 (see Figure). "There has been similar growth in numbers of courses and research projects, as well as in their range and magnitude," said Mayo. "A growing list of companies are supporting a growing list of universities with special programs." Mayo added, "Design automation has become a major and exciting frontier in the field of electronics and the universities know that message."



Evidence of that can be seen from IBM's recent announcement to grant $40 million worth of CAD/CAM equipment to 20 engineering graduate schools. The grants are part of a $50-million corporate program designed to encourage education in manufacturing systems at American engineering schools.

The universities, with student populations ranging from under 1200 to more than 54,000, were selected from 115 universities that submitted proposals in response to IBM's announcement last fall. At that time, the company offered a cash and equipment grant program to help universities update manufacturing engineering curricula. The equipment includes IBM 4341 processors with 16M bytes of memory, direct access storage devices with 660M bytes of memory, and interactive CAD/CAM workstations.

These systems will be used to help teach mechanical engineering, computer science, business, and architecture students up-to-date design and manufacturing techniques. IBM software packages from various divisions and packages donated by CADAM, Inc, (Burbank, Calif), Dassault Systemes (Paris, France), Bell Northern Research, Ltd (Ottawa, Canada), and Structural Dynamics Research Corp (Cincinnati, Ohio) complement the IBM equipment.

The 20 universities selected are Arizona State University, Boston University, Brigham Young University, University of California, California Polytechnic State University, University of Florida, George Washington University, Georgia Institute of Technology, University of Illinois at Urbana-Champaign, Lehigh University, University of Massachusetts, Michigan Technological University, University of Missouri-Rolla, Ohio State University, Polytechnic Institute of New York, Rensselaer Polytechnic Institute, San Jose State University, University of Texas at Austin, Utah State University, and Virginia Polytechnic Institute and State University.

Several schools offer their freshman class an added attraction. Polytechnic Institute of New York, for instance, will distribute a free personal computer to the next term's freshmen class for use as remote terminals for the IBM 4341 mainframe. The students can keep the computer when they graduate.

---

that control disk I/O, host I/O, and manage bit-mapped graphics.

The workstation architecture allows parallel processing of graphics and application data, using separate buses that share a common display list memory. According to Cadtec, adding more workstations maintains a uniform system performance because the system's processing power expands commensurately.

To get both engineers and engineering managers involved in the project, the company developed the companion model 8500 office station. The office station has a resolution of 640 x 408 pixels on a 13" color CRT with four color planes. It communicates with the host over standard RS-232 lines. Since application programs can run in the host or the workstation, the office station gives each engineer, as well as the
(continued on page 32)

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CIRCLE 16

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"Concept-to-chip" design

(continued from page 30)

project manager, direct access to all project data. This is done by using the project database with the same tools, user interface, and design environment that are part of the workstation.

The system includes application programs for schematic entry, logic validation, documentation, and project management. Two high level interfaces—the Cord data system and the View user interface system—isolate the applications from the hardware and from the I/O details for both graphics and data storage.

Cord is a relational database, object-oriented interface system that allows storage of both a project database for a large design, and local databases for individual workstations. Once complete, the design partition can be integrated back into the project database to reflect approved design changes. The View menu-driven interface allows separate applications to be performed simultaneously in multiple windows.

Cadtec's initial application software offering focuses on logic design. Future extensions are planned for all design levels, from architectural design through integrated circuit layout, and printed circuit (PC) board place and route operations. Currently, a typical installation of the series 8000 system that supports 10 engineers costs an average of $50,000/user.

Manufacturers of standalone workstations are also answering the call for more sophisticated design automation tools. At least four companies introduced enhancements to their systems at the conference: VIA Systems, Inc (N Billerica, Mass), HHB Softron, (Upper Saddle River, NJ), VLSI Technology, Inc (San Jose, Calif) and Valid Logic Systems (Sunnyvale, Calif).

A package for all layouts

VIA Systems introduced a multifunction integrated design engineering and layout package, called Diagram, that provides IC design engineers with logic and schematic capture, and design verification for gate arrays and standard cell layouts. The package has been integrated into the company's series 100 computer aided design/computer aided manufacturing (CAD/CAM) systems for custom VLSI layout and mask preparation.

According to Richard M. Jennings, vice president of marketing, the series 100 systems can now offer design engineers a full range of "concept-to-chip" support tools, beginning with logic diagramming and continuing through mask preparation and tooling in both bipolar and MOS process technologies. The user can create logic and schematic diagrams to trace the connectivity of networks through these logic diagrams. Net lists can be extracted for each diagram and the design engineer can map the logic diagram onto the physical circuit layout of gate arrays or standard cells.

The system's data structure has been expanded to include wire connections directly in the data base. The designer traces signals in a schematic or layout using the TRACE function, which highlights all pins and wires connected to a particular net in a special color (see Photo).

Generating a net list

The net list is generated from the completed logic or schematic diagram after a postprocessor performs basic checking operations to flag any violations. At this point, the net list can be formatted for interfacing to logic simulation and analysis tools as well as placement and routing programs. After design verification, the user maps the logic diagram onto a gate array or standard cell layout. When the designer is satisfied with the output, the VIA series 100 writes either an optical or an electron-beam control program on magnetic tape.

The first release of Diagram formats the net list for automatic input to HHB Softron's Computer Aided Design and Test (CADAT) simulation and test program development system. This digital logic simulator package handles IC and PC board design verification and test generation on VLSI chips. The CADAT software is written in the C language and runs on the DEC VAX computer under the VMS operating system as well as on engineering workstations or minicomputers under the Unix operating system.

CADAT combines design and fault simulation for a chip from its initial design through test generation. Once the design is complete, the design simulation data can be recycled for test generation. CADAT generates 12 simulation states for both bipolar and MOS chips. The bidirectional signal flow inherent in MOS circuits is modeled using transmission gate models and a "wired-bus" method. Circuits are simulated with a 10-ps timing resolution with independent rise and fall delay times permitted for each device output.

A 60-fold speed increase

According to the company, a concurrent fault simulation algorithm in a CADAT system analyzes potential test vectors for fault coverage up to 59 times faster than traditional fault simulation techniques. This is because CADAT bases the number of faulty circuits simulated per pass on CPU memory availability rather than CPU word size, thereby simulating up to several thousand faults at once.

The menu-driven interface and the input stimuli are specified in an English-like language that is capable of macro and vector manipulation. Thus, the user can analyze the simulation data at the terminal without generating a hardcopy output.

Other features of the CADAT package include a charge decay model of MOS circuits, a fault trace capability, a batch processing mode, and a random fault sampling feature that permits a worst-case projected fault coverage to be calculated at the end of each fault simulation pass. In addition, PC design and PC test functions can be done using existing IC library models or new models developed by the user. The CADAT package costs approximately $100,000.

At the conference, VLSI Technology, Inc announced a composition editor that automates the

(continued on page 34)

Don't limit your computer's input with a mouse. A mouse can move a cursor on a screen. Period. With GTCO's new Micro Digi-Pad™ you can position a screen cursor...or draw, trace, select menu functions on the tablet, even use the stylus like a joystick. Micro Digi-Pad is priced like a mouse...and you can use it like a mouse. Or use it with a stylus for input as natural as a pencil on paper.

GTCO's patented digital electromagnetic scanning--with no mechanical parts--lends itself to operation in office and industrial environments that cripple an optical or mechanical mouse.

The Micro Digi-Pad is GTCO's answer to the need for low cost,versatile graphic input.

MICRO DIGI-PAD CHALLENGES THE MOUSE

COMPARE

FEATURE	MICRO DIGI-PAD	vs.	MOUSE
Low cost	Yes		Yes
Small Package	Yes		Yes
Ergonomic	Yes		Yes
Low Power	Yes		Yes
Single Voltage	Yes		No (RS-232C Model)
Absolute Coordinates	Yes		No
Off Screen Menu	Yes		No
Trace Graphics	Yes		No
Stylus Option	Yes		No
4D (Stylus tilt output)*	Yes		No
4 buttons	Yes		No
Digitizer Compatible	Yes		No
Dual RS-232C	Yes		No
Hostile Environment	Yes		No
Proven Supplier	Yes		?

*Patent Pending

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CIRCLE 17

"Concept-to-chip" design

(continued from page 32)

layout and interconnection of cells that make up VLSI circuits. These cells are obtained from the company's cell compiler library. The composition editor is a hierarchical system that enables the user to operate on symbolic building blocks such as ROMs, RAMs, counters, and arithmetic logic units, and to wire them. The structured composition editor then takes care of the specifics in creating the layout and all physical interconnection, in addition to creating the pad-ring wiring.

The designer edits a design by specifying particular cell characteristics before a cell is compiled to a physical layout. The compiler library can therefore generate thousands of cell variations rather than the usual few hundred. "This approach," says Doug Fairbairn, vice president of VLSI Technology's User-Defined Technology, "allows the designer to achieve the higher performance and lower cost ICs usually associated with full-custom circuits."

According to VLSI Technology, in contrast to other graphics systems, the block and wire placement operations are done in a relative fashion so the user does not have to be concerned with absolute block placement. After the wiring is complete, the editor automatically optimizes the block spacing, minimizing the area between them to make better use of silicon. When the chip core is complete, a pad-ring generator automatically places the desired number and type of bonding pads around the chip, wires them together, and lets the user specify the final pad-to-core wiring.

All of the system cells, along with the text that describes them and any other user-specified data, are organized in a tree-structured data base with a graphic interface. The user points the cursor at the appropriate category of items to display the elements in that category and the structures included on the next level down in the hierarchy. The cells are constructed using either the company's cell compiler library or using the symbolic STICKS editor, its geometric layout editor, or even cells from another design editor.

A few companies are hedging both sides of the single workstation versus clustered computer aided engineering (CAE) systems issue. For instance, Valid Logic Systems introduced the SCALDSystem II which, according to the company, functions both as a standalone 32-bit CAE design station and also as part of a mainframe computer network. When operating in a standalone mode, the system is configured with a dedicated 32-bit processor for validating designs and a 16-bit processor for capturing schematics.

Optimizing mainframe resources

Company founder and president, Jared Anderson, makes the point that today's large system designs or VLSI chip designs simply cannot be completed on a standalone workstation in acceptable times. Thus, SCALDSystem II was developed for users to take advantage of mainframe resources to run Valid Logic's verification programs in a user-transparent mode. Valid offers its own completely supported programs on such mainframes as the DEC VAX and the IBM 3081.

Designed and manufactured by Valid Logic, the entire system consists of individual graphics design stations based on the 8086 16-bit microprocessor and a cluster controller based on the 68000 microprocessor that runs on Unix. The cluster controller includes Winchester disk storage, magnetic tape for backup, and an electrostatic plotter, all shared by design station users. High speed ports communicate with a host computer.

SCALDSystem software validation tools include a graphics editor, the SCALD compiler, a timing verifier, a logic simulator, and a post-processor. The graphics editor runs on the design stations and creates schematics online. The compiler then produces a design data base from the schematics incorporating device models obtained from component libraries. Finally, the design's timing errors and logic behavior are verified. The post-processor generates a net list and other design data for the physical design. The SCALDSystem II is available for about $60,000.

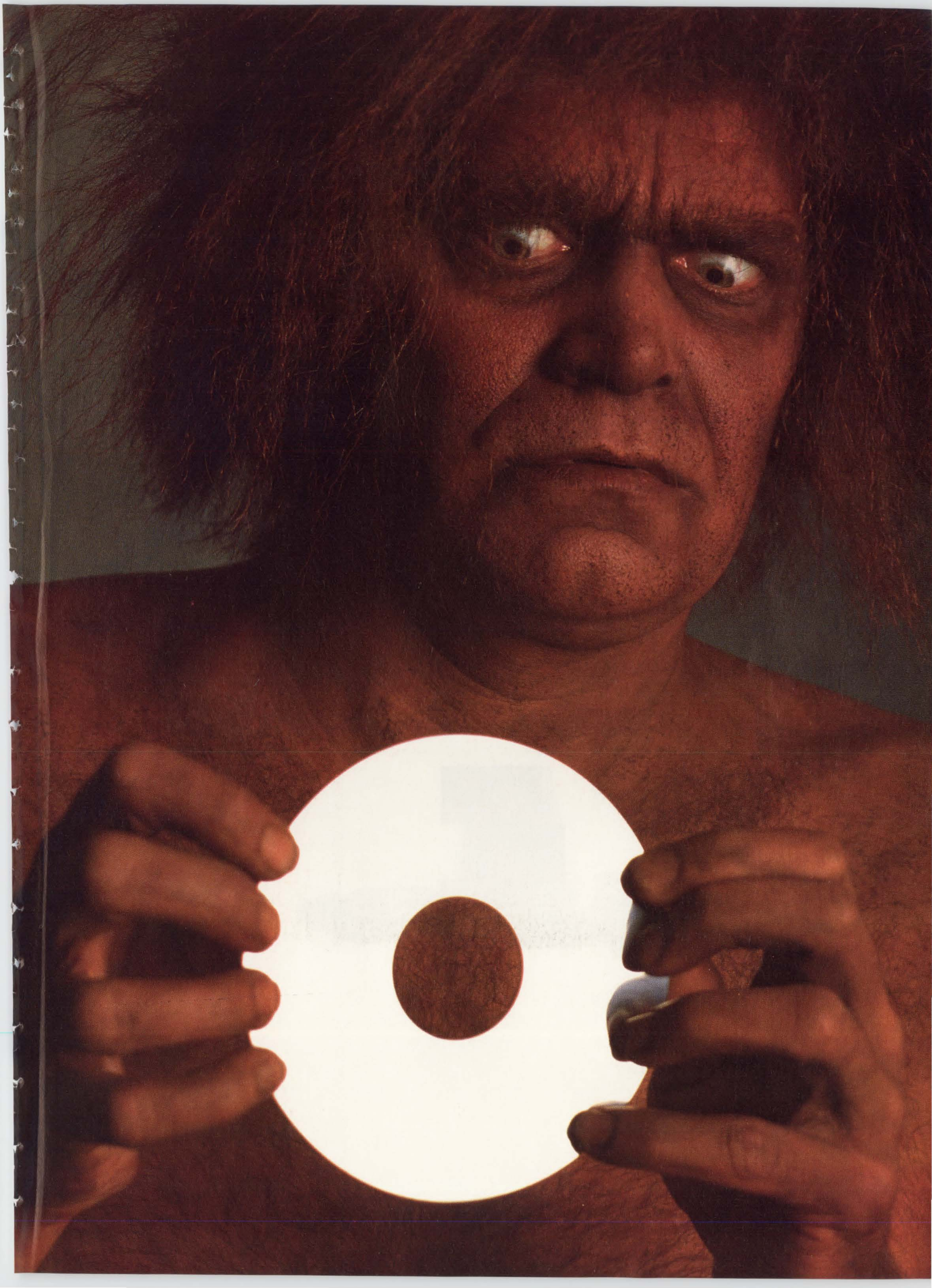
Not to be outdone, Avera Corp (Scotts Valley, Calif) dropped the price of its product line while enhancing its system with a 768 x 1024 pixel, 19" color monitor. An advanced software package allows drawing of true circles, arcs, and adds array capabilities. The workstations, which previously cost from $50,000 to $70,000, are now in the $35,000- to $57,000-range that is more in line with competitor's product in a similar performance range.

In general, other CAE workstation manufacturers are constantly improving their products. While the overall worldwide CAD/CAM market is currently estimated in the $350 million revenue range, the CAE market alone should reach that figure by 1986. As was evident at the conference, most CAE contenders realize that circuit designers need more than an electronic draft table to create new designs. More people have to be brought into the design cycle, and the design cycle must encompass more interactive tools from concept to finished product. Thus, opportunities exist for clever people to create sophisticated system-based design automation tools. These systems must also be able to operate each other's application programs.

Currently, no two systems can run programs other than the ones designed specifically for them. As far as the potential for standardizing compatible software to make a designer's life easier, that remains the subject of a future article.

—Nicolas Mokhoff, Senior Editor

SYSTEM TECHNOLOGY
(continued on page 40)



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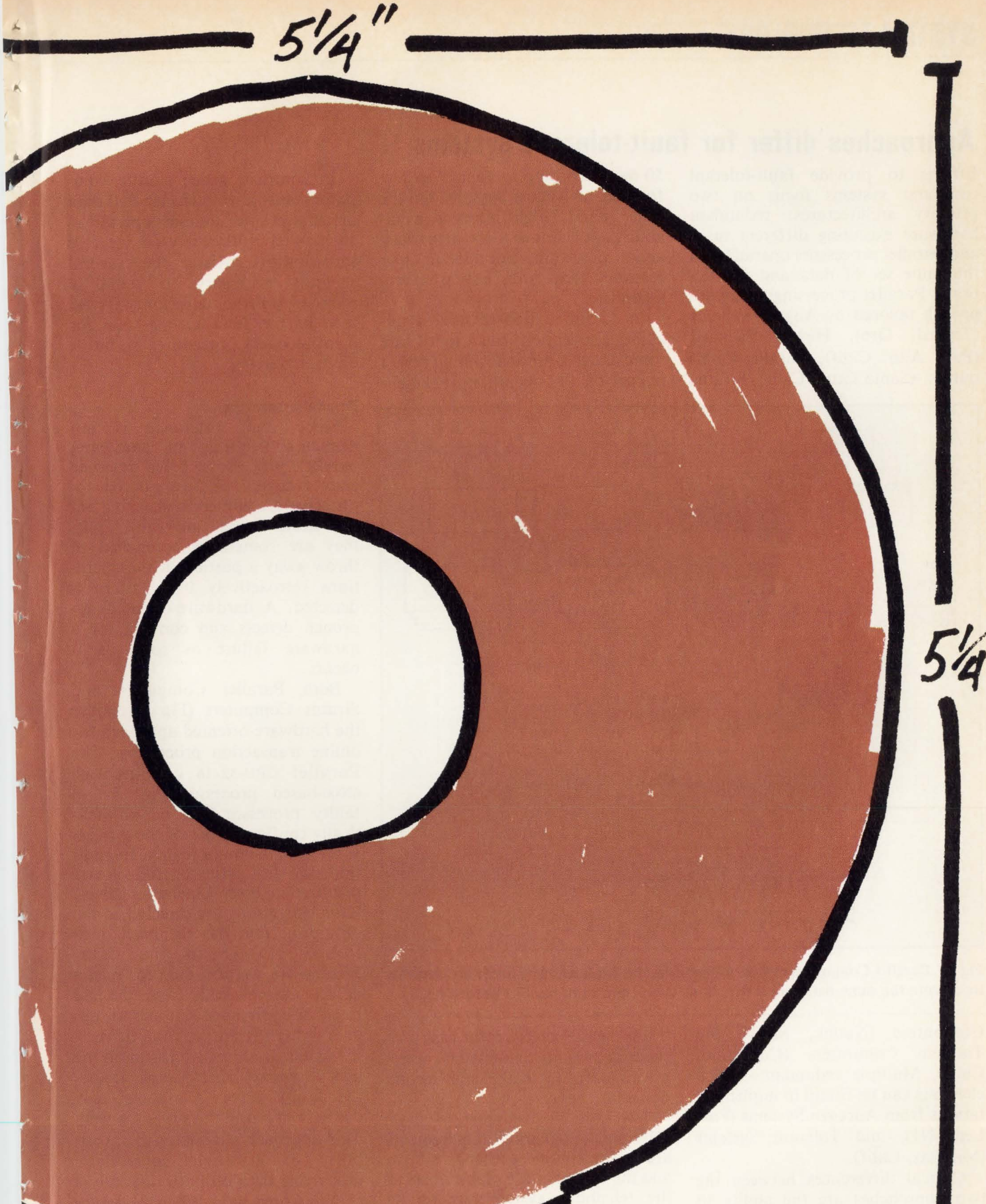
CIRCLE 20


5¼"
5¼"

Approaches differ for fault-tolerant systems

Efforts to provide fault-tolerant computer systems focus on two primary architectures: redundant hardware executing different tasks and parallel processors operating on the same set of data and instructions. Parallel processing is the approach favored by August Systems (Tigard, Ore), Hewlett-Packard (Palo Alto, Calif), Parallel Computers (Santa Cruz, Calif), Stratus Computers (Natick, Mass) and Tandem Computers (Cupertino, Calif). Multiple redundant system elements can be found in implementations from Auragen Systems (Fort Lee, NJ), and Tolerant Systems (Milpitas, Calif).

Critical differences between the two approaches are the ability to recover from errors in real time as well as the degree of fault tolerance implemented in hardware and software. High data integrity applications, such as process control or aircraft instrumentation, deal in realtime error recovery in less than 50 ms, according to John Wensley, founder of August Systems. On the other hand, high resource availability applications like online transaction processing can tolerate error recovery procedures lasting several seconds.

In addition, high resource availability applications can also tolerate some data corruption without severe impact on the operation of the entire system. Such is not the case with realtime systems that rely on correct information to make split-second decisions, however.

Two notable examples of these different application requirements are the telephone exchange system and the space shuttle. Subscribers to the telephone system rely on its ability to provide continuous service even if one or more of its operating elements (eg, central offices) are in disarray. Subscribers are relatively indifferent to occasional corruption of data (eg, misdialed calls) and the recovery time for errors.

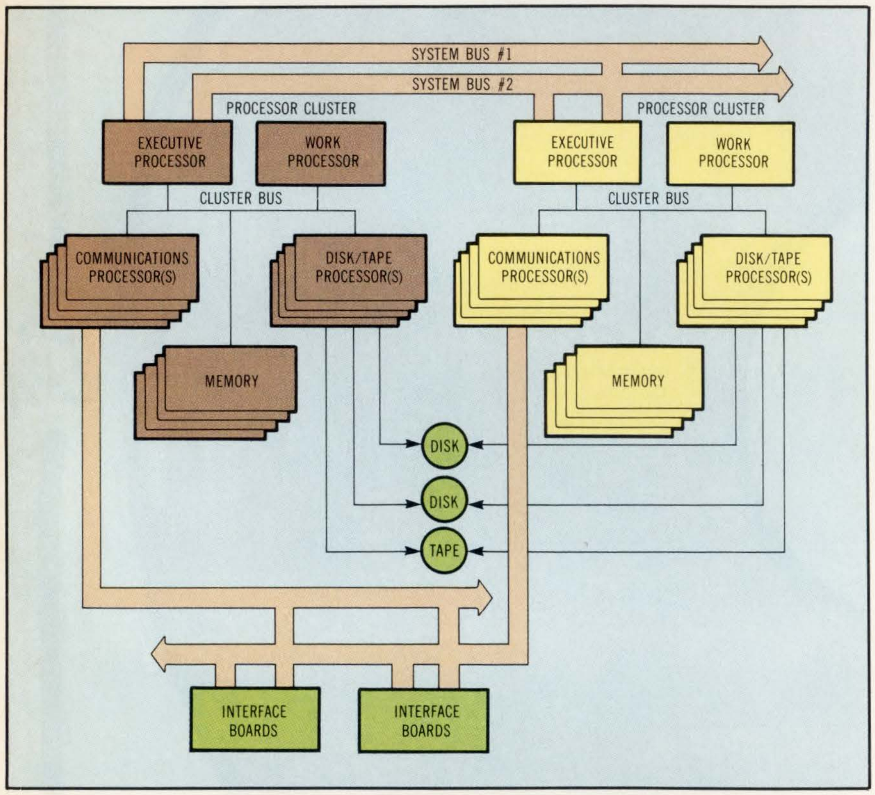


Fig 1 Parallel Computers CPU-32/16 illustrates the duplication of hardware elements to execute the same data and instructions characterized in parallel processing.

In contrast, space shuttle computers must always ensure that data are correct since complex operations such as navigation rely on accurate information. Also, the several seconds necessary to redial a number on the telephone system may be too long a time span for error-recovery procedures in shuttle control systems.

Parallel processing

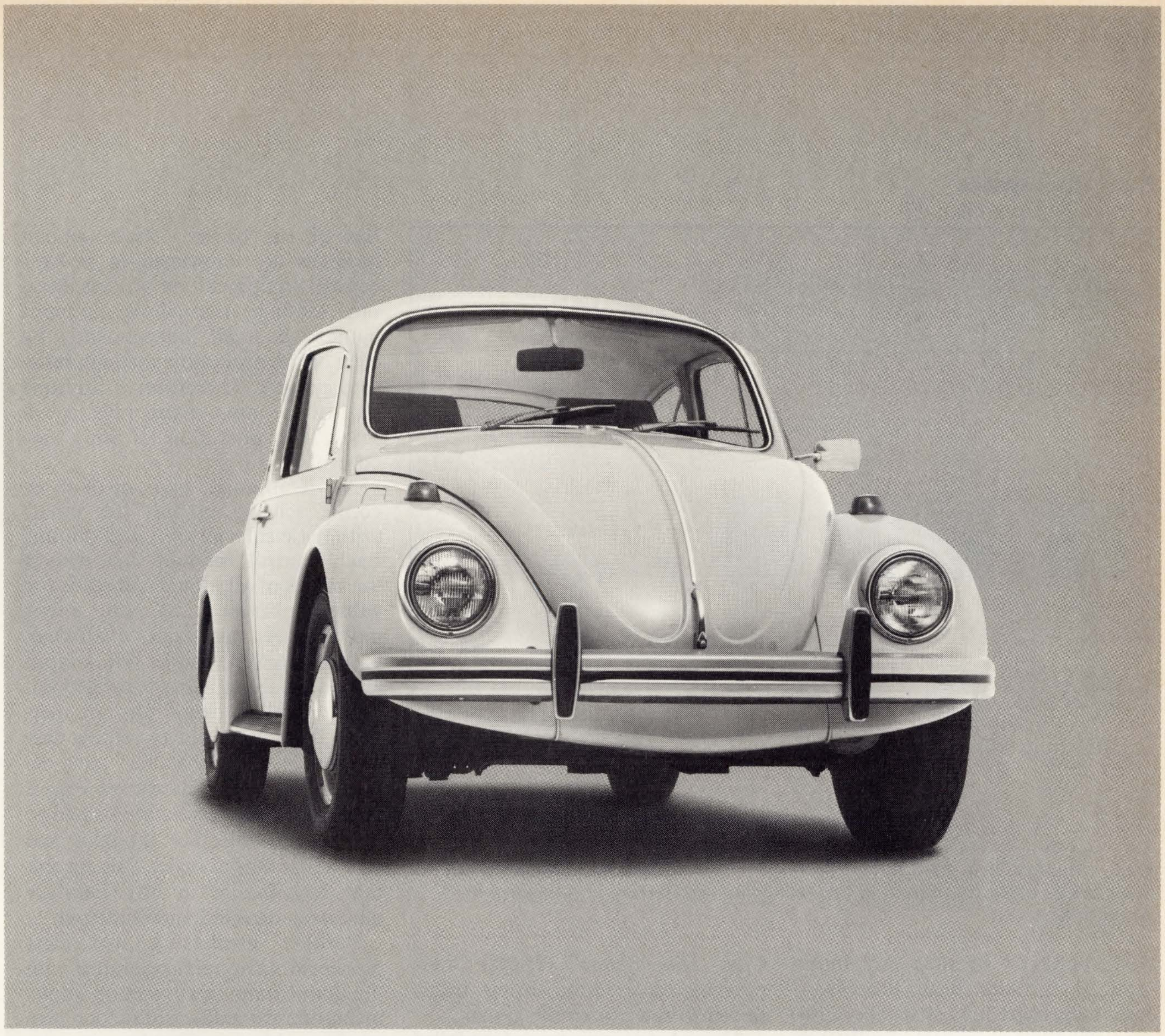
Since fault tolerance is implemented entirely in hardware, parallel processors offer realtime error recovery. Software-based approaches are limited to checking out operations at set intervals. Thus, they are sometimes compelled to throw away a portion of the operations retroactively if a failure is detected. A hardware-oriented approach detects and corrects for a hardware failure as soon as it occurs.

Both Parallel Computers and Stratus Computers (Fig 1) choose the hardware-oriented approach for online transaction processing. The Parallel CPU-32/16 couples two 68000-based processors so that a faulty processor can be automatically configured out of the system. If the results do not match. In addition, all disk write operations are mirrored on both Winchester drives. Read operations are directed to the disk drive that has the head positioned closest to the data. Read/write errors due to media defects automatically cause the bad track to be mapped out and an update written from the good drive.

If a hardware malfunction on the disk drives or backup tape occurs, the faulty drive is automatically configured out of the system as well. This approach eliminates the possibility of a single controller's destroying data on both disk drives of a mirrored pair. When the faulty drive is brought back into service, it is automatically updated to the current state of the other mirrored drive.

Each serial device (eg, printers and terminals) is connected to two

(continued on page 42)



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Fault-tolerant systems
(continued from page 40)

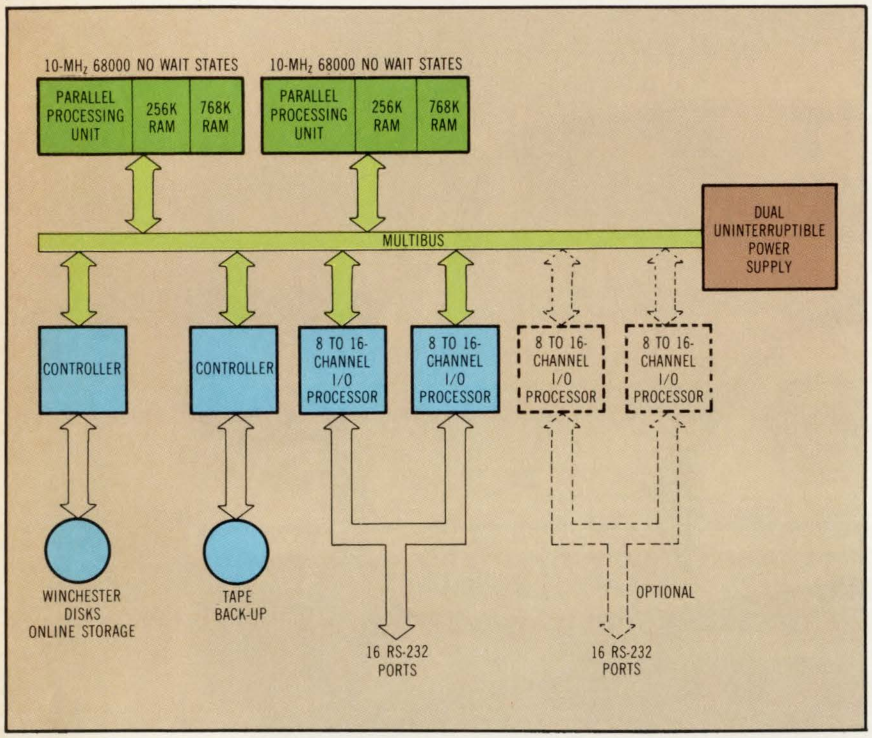

Fig 2 Multiple high speed links separate processor clusters so that interrupted tasks can be easily transferred in this redundant architecture implemented by Auragen Systems.

I/O processors so that any input received through both processors can be checked for consistency. Inconsistencies caused the faulty I/O processor to be automatically configured out of the system. On the other hand, output is directed to only one processor. If the I/O processor malfunctions, it is removed from the system and the output request is sent to the other processor.

The Stratus/32's approach to fault tolerance is similar to the Parallel CPU-32/16's, but adds another level of parallelism by including two sets of logic on each processor, disk controller, and communications controller board. The company claims that this approach is one of the simplest ways to combine onboard failure detection with realtime repair. A set of comparators checks the outputs of the two logic sets every clock cycle (approximately 8 million times/s). When a hardware comparator discovers a board component failure, that board removes itself from the system. Trigger logic prevents data from being transferred to the rest of the system.

The redundant partner of the failed board continues to operate without knowing that its counterpart on the bus has failed. In addition, the rest of the system is unaware that a board failure has occurred so that any executing program need not back up and restart at an earlier checkpoint.

August Systems does not go to such lengths in redundancy to support realtime control systems. (See Fault Tolerant Systems Can Prevent Timing Problems, by John H. Wensley, *Computer Design,* Nov 1982, pp 211-220.) Rather, to verify operations, its series 300 system uses three independent control modules that are able to read data from the memories of the other two through read only links. No provision is made for writing to another processor's memory to eliminate the possibility of a faulty processor's overwriting good data in the memories of the others. These control modules are connected to process control equipment via process interface modules that allow all input data to be read independently by each of the processors through separate circuits. Therefore, if any one part of the input circuit fails, it will affect the operation of only one control module.

An elaborate two-out-of-three voting scheme verifies the input, arithmetic calculations, and output. Each control module first detects the values of all inputs and reads the values obtained by the other modules. At this point, a software vote is taken to remove faulty input effects. A second vote is carried out after identical operations are performed on the input to remove any arithmetic errors that may have occurred. Finally, a hardware vote is taken after the results are passed to the process interface modules and sent to the output logic. This ensures that any failure in any interface module is detected and corrected.

Parallel processing was first pioneered using minicomputers with Tandem Computers NonStop implementation for online transaction processing. More recently, it was implemented for process control with Hewlett-Packard's Datasafe 1000 (*Computer Design,* Jan 1983, p 22). First announced in 1977, the NonStop system relies on multiple computers connected by two independent interprocessor buses for block data transfers among different processes residing on different CPUs.

System-wide access to I/O devices (supervised by a dual-ported I/O controller) consists of two cooperating processes on different processors that control a particular I/O device. One of the processes is considered the "primary." This process handles any requests for operations and sends the same information to the backup process via messages along the high speed bus. These "checkpoints" ensure that the backup process will have all the
(continued on page 44)

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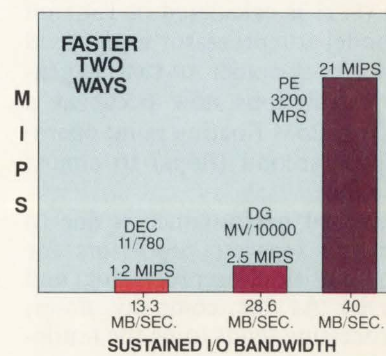

PERKIN-ELMER

CIRCLE 22

Fault-tolerant systems

(continued from page 42)

information needed to take control of the I/O device in case of an I/O channel error or failure of the primary process's CPU.

Data bases can be duplicated on separate disk drives under software control for further reliability. Similar techniques using a dual-ported I/O controller and disk drive mirroring allow dual Hewlett-Packard HP1000-F computers to detect and recover from errors in as little as 200 ms.

Redundant processors

If realtime error detection and recovery is not required (as in many online transaction environments), the cost of duplicated hardware that performs the same task may not be economically feasible. Redundant processor systems dedicated to multiple tasks would probably be more suitable. Both the Auragen System 4000 and the Tolerant System Flexible Architecture system (Fig 2) combine hardware and software redundancy. Auragen chooses to cluster multiple 68000 microprocessors, with one processor dedicated to executing most of the operating system and fault-tolerant functions, while another processor is assigned to execute application programs only.

Independent communications and disk/tape controllers complement these processors in the cluster. Several clusters (up to 32) are then loosely coupled by two 16M-byte/s system buses so that if any component in a cluster fails, another cluster can resume execution without operator intervention.

Redundancy is also provided for data bases since dual-ported disk drives allow access by two separate clusters. Similarly, the dual-ported communications bus provides fault-tolerant access to interface modules controlling attached peripherals.

A similar clustering concept is used for Tolerant's System Building Block (SBB). It consists of a central processor, auxiliary processor, up to two I/O processors, and system interconnect buses. A 64-bit wide memory bus provides all resources common access to data. The central processor executes processes out of a memory queue, while the auxiliary processor handles interrupt servicing and monitoring of the rest of the system with background diagnostics.

If a fault is detected, the auxiliary processor logically separates the SBB from the rest of the system. Different parts of the operating system have saved relevant state information of the interrupted transaction. In this way, new processes are initialized to the last encountered beginning of the transaction.

Unlike other redundant schemes that implement data recovery and integrity mechanisms in the file system, Tolerant Systems provides these mechanisms below the file level. Performance is enhanced because any disk-based data can be protected from failure using the before-image and rollback/restart facilities. The Tolerant implementation also provides mirroring of files for protection from media failure and for load balancing.

—Joseph Aseo, Field Editor

Array processors split work for increased speed

A distributed processor architecture allows the FPS-5000 family of array processors from Floating Point Systems to accelerate computations three times faster than its previous generation products. For example, a 2-dimensional fast Fourier transform (FFT) is calculated in 1.4 s on the model 5110 processor as opposed to 3.4 s for the older AP-120B. In general, calculations now occur at a rate from 26M floating point operations per second (flops) to almost 62M flops.

Increased performance is due to dedicating separate processors for data acquisition, preprocessing, and analysis. As the company notes, preprocessing tends to be the bottleneck in any array processing application (50% to 75% of total processing time). These calculations tend to be standard operations (eg, digital filtering, FFTs) that require relatively low precision. On the other hand, calculations for data analysis tend to be application-dependent (requiring custom software) and high precision.

Meanwhile, data acquisition must obtain information from a variety of sources (eg, disk drives, group code recording (GCR) tape drives, bulk memory, or directly from A-D converters). The FPS-5000 family consists of different combinations of a control processor (responsible for host communications, system control, and data analysis), general purpose I/O coprocessors, arithmetic coprocessors (primarily dedicated to data preprocessing), and system common memory.

Hardware architecture

The control processor is upward compatible with the company's older 38-bit processors (AP-120B, FPS-100, AP-180V, and AP-190L). As the central system controller, the central processor supervises the distributed system elements by assigning processing tasks and synchronizing the flow of data through the system. It also provides a compatible environment to run 38-bit application programs as well as the FORTRAN compiler and over 400 library subroutines. A pipelined hardware architecture allows parallel processing through its floating point multiplier and adder unit, an integer processing unit, scratchpad registers, and multiple data memories.

Separate executive, arithmetic, and control units mark the pipelined architecture of the arithmetic coprocessor. The arithmetic section is controlled by a microsequencer (Am2910) tied to a 16-bit bipolar microprocessor (Am29116). Dual floating point adders are tied to a single floating point multiplier for 32-bit computations. Multiported

(continued on page 46)

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CIRCLE 23

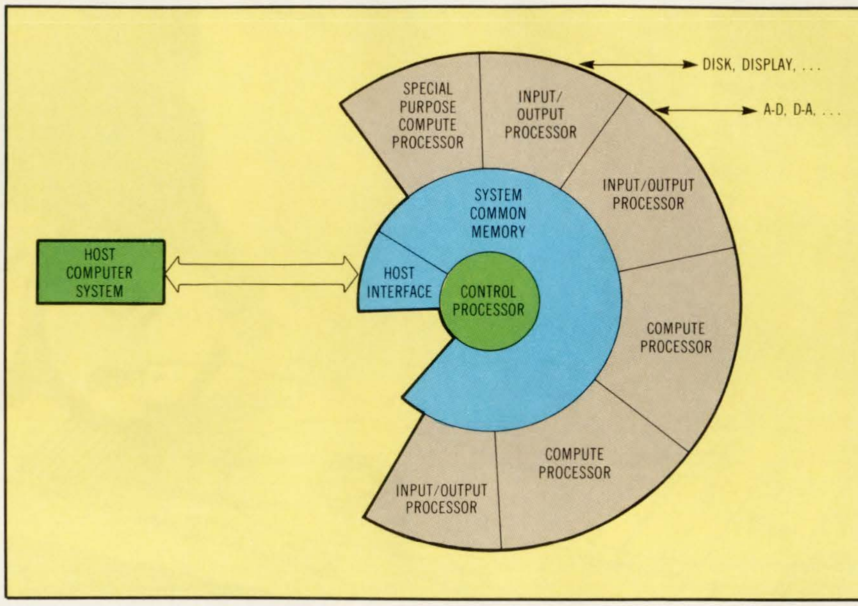
Array processors

(continued from page 44)

data memory (up to 16K 32-bit words) allows the channel executive to load programs and data from system common memory concurrent with computations occurring in the vector-oriented arithmetic section. In addition, the data transfer path between the system common memory and the local data memory contains logic to handle format conversions (38-bit to 32-bit) as selected by a user's application program.

Also included with the arithmetic coprocessor are 4K words (32-bit) of control memory that can be loaded by the control processor, as well as a table memory loaded with cosine values of FFT computations and other constants required by library subroutines.

The general purpose I/O coprocessor handles data acquisition via a 16- or 32-bit interface adapted to A-D and D-A converters, GCR tape drives, disk drives, and bulk memory. It also supervises display systems and realtime control equipment. In addition, its hardware architecture consists of a 20-bit wide bit-slice processor used for address calculations and device protocol, and a format processor for fix/float and pack/unpack operations.



The system architecture of the Floating Point Systems FPS-5000 distributed array processor has the inner ring elements (host interface, control processor, and system common memory) operating synchronously for simple application debugging. The outer ring elements operate asynchronously for maximum throughput.

Software architecture

A systems language based on FORTRAN-77 constructs, Multiple Array Processor Execution Language (MAXL) provides the necessary extensions to coordinate the tasks being executed in each distributed processor. User code developed in MAXL executes in both the control processor and the executive units of the arithmetic coprocessors.

The control processor uses MAXL routines to set up channel programs for both I/O and arithmetic coprocessors in system common memory, and provides the appropriate processor interface with the address of the program. From then on, the control processor and its coprocessors operate concurrently, using common memory locations or device registers to synchronize the execution sequence.

Instead of treating each system element as a channel processor, the control processor can also directly control the coprocessors via I/O instructions to a set of device registers. This method is typically used when it becomes necessary to quickly coordinate coprocessor operations to halt coprocessor execution, perform interface diagnostics, or start coprocessor operations. This master/slave relationship can be extended so that the control processor controls both processing and data flow.

Such a master/slave mode allows the control processor to take command of the system when individual tasks are completed. While individual coprocessors perform their tasks, the control processor supervises acquisition of the next data block and sends the results of the last data block out of the array processor.

Complications set in when a single processor is allocated to more than one task. It may be necessary to write channel programs in MAXL in order to reflect the master/slave relationship. The distributed control mode may be appropriate because it allows individual coprocessors to synchronize data flow among themselves. Throughput can be optimized because data flow requirements often control the timing of operations.

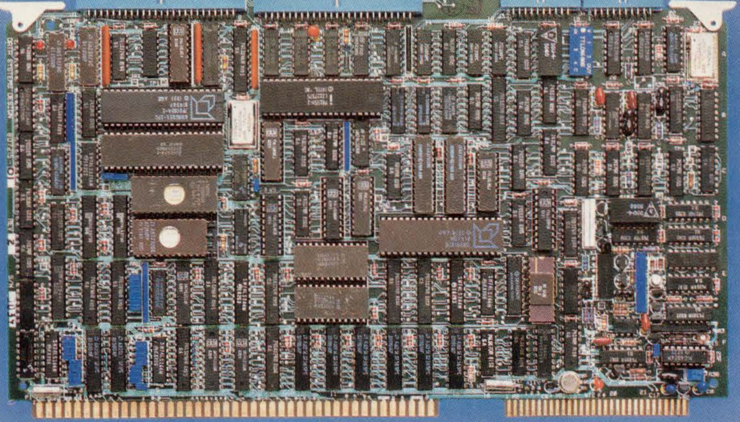
All members of the FPS-5000 family can function under the direct control of the host computer, or as an autonomous processor, or a combination of the two schemes. The base configuration includes 256K words of data memory (32 bits), 12.5K words of table memory, a general purpose control processor, and a single-compute coprocessor. Depending on the model, program memory is expandable to either 512K words or 1M words (38 bit). The 5300 models provide up to two coprocessors, while 5400 models allow three processors. System price for a typical 26M-flops unit starts at $60,000. The 62M-flops model is priced at less than $100,000. **Floating Point Systems,** PO Box 23489, Portland, OR 97223.

—*Joseph Aseo, Field Editor*

Circle 210

SYSTEM TECHNOLOGY
(continued on page 48)

ONE SLOT SHOPPING.



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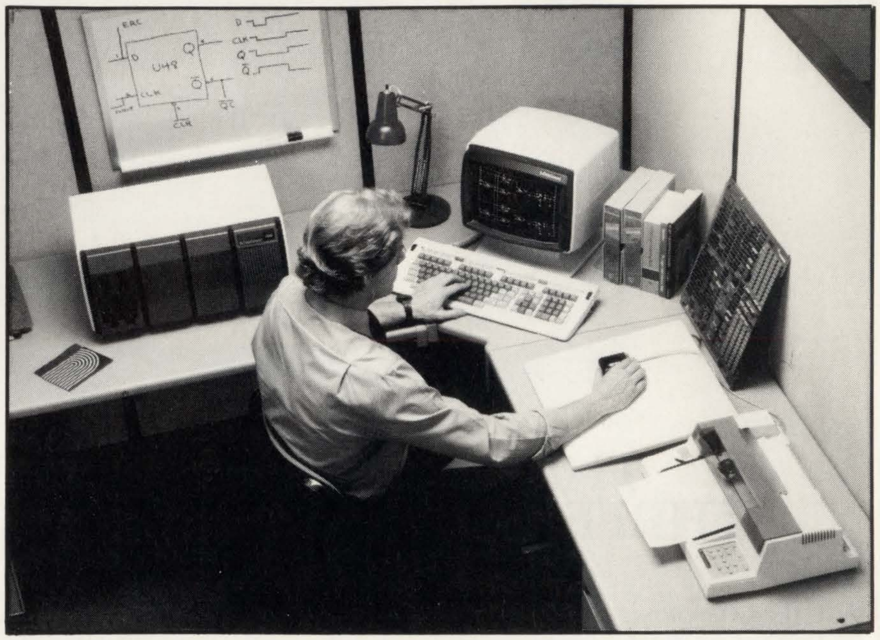
CIRCLE 24

Data General makes stand in professional computer field



Not merely another breed of standalone microcomputer siblings with only subtle differences from their parents, the Desktop Generation™ series introduced by Data General is designed to dovetail with the company's expansive line of minicomputers. Four models—the 10, 10/SP, 20, and 30—exhibit novel design features and offer wide potential, particularly with the increased memory, operating system options, and floating point performance available on the advanced systems.

These additions to the already broad microcomputer field mark a move by Data General to capture a sizable piece of the personal/small business market. Unlike an earlier offering, the Desktop Generation are professional computers that maintain compatibility with both industry standard software and the company's superminicomputer software. They are intended particularly as corporate-level personal computers for both office automation and technical applications.

Coprocessors offer dual operation systems

The most interesting aspect of the tightly coupled coprocessor approach Data General has chosen is true operating system concurrency. By allowing two operating systems to run concurrently on the same microcomputer, up to four users can simultaneously execute proprietary software and either CP/M-86 or MS-DOS-based applications.

This dual operating system capability is achieved through the use of a microEclipse processor and an Intel 8086 processor. The microEclipse processor runs Data General's AOS, RDOS, or MP/AOS operating systems, while the 8086 operates under CP/M-86 or MS-DOS.

The company's 16-bit proprietary processor incorporates internal memory protection and allocation logic. Its internal CP/M and MS-DOS interface allows it to function in conjunction with either operating system by controlling memory usage and allocation for the 8086 processor. In addition to serving as an I/O processor for the Intel CPU, the microEclipse processor establishes a memory map for the entire system. This memory map provides discrete RAM space for both operating systems and their applications. Thus, two diverse software environments reside in system RAM simultaneously. No page swapping is required when moving from one to the other.

All 8086 I/O requests are controlled by the Data General processor. If needed, a high priority interrupt demanding immediate attention can be assigned to the 8086 operating system at system generation time. Internal bus contention issues are resolved by tri-stating one processor's data and address lines when the other needs the buses.

Modular architecture is built around two 7" x 9" boards. In addition to the processors and their associated control circuitry, memory management and protection, control ROM (CROM), disk and display controllers, and 256K bytes of RAM are located on the two main boards. A floating point instruction set in ROM is also included for use on the microElipse processor.

Modularity and compatibility provided

The system's modular design philosophy assumes that users will require increased functionality with time. Hardware modules of 4.5" x 12" x 9" snap together (no cabling required) and provide users with incremental performance steps. The power supply, floppy disk, Winchester disk, and CPU modules can be located off-desk (see Photo), and also simplify maintenance operations.

Compatibility with the company's full line of 16- and 32-bit Eclipse computers is promised, and a host of communications options are available. In addition to proprietary communication packages, the micros also support IEEE 802, X.25, HASP, SNA, SDLC, and 3270 protocols. Interfaces are also available for IEEE 488, and USAM-4, which is a 4-line universal synchronous/asynchronous multiplexer.

Mass storage is provided in the form of 5¼", double-density floppy or flippy drives using the IBM PC's 8-sector/track format. A 15M-byte Winchester is also available, as is a

(continued on page 50)

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CIRCLE 25

Data General

(continued from page 48)

15M-byte cartridge tape for backup. Memory options abound and, depending upon the family member, run from 128K to 2M bytes of RAM. A minimum of 512K bytes is recommended for dual operating systems.

In recognition of the role graphics play in office and business computing, Data General is providing a variety of graphic options. Medium resolution, bit-mapped monochrome (12″) and color (13″) displays are available. A 4096-color palette is also supplied, and display resolution is 640 x 240 pixels. Graphics and alphanumeric characters can be displayed simultaneously and a DMA channel between the display and hard disk allows high speed transfer of graphic data. The system also supports a graphic tablet and mouse, and the GKS software standard.

An entry level model 10 is priced at $3200, and the line tops out at slightly over $17,000 for a fully configured model 30. **Data General Corp**, 4400 Computer Dr, Westboro, MA 01581.

Circle 211

INTEGRATED CIRCUITS

Silicon Glen aims at European market

"Purveyors of fine technology since 1765" is the punch line of an ad used by the Scottish Development Agency (SDA) to call attention to the scientific capabilities of Scotland. To stress that point, the SDA recently invited a group of editors from seven U.S. based trade magazines and newspapers to visit selected plants and universities in the middle-Scotland stretch, including Strathclyde, East Kilbride, Livingston, and Glenrothes, as well as the two major cities of Glasgow and Edinburgh.

There is much competition within the British Isles, particularly among Scotland, Wales, and Ireland, to attract companies. Incentives are many: available facilities with as much as three years free rent, willingness to custom-build new plants, tax breaks, plenty of talented labor, and an excellent interface with high technology groups at several universities. Moreover, although salaries and employee benefits are relatively low, there is only a 2.6% turnover of salaried staffs; and labor disputes, at least in Scotland, seem to be rare. (An estimated 65% of the workers are nonunion.)

Much of the industry in the middle-Scotland area is related to semiconductor technology. As was done by computers and peripheral manufacturers in the various sections of Britain, semiconductor manufacturers have located plants in Scotland in order to meet trade competition. Motorola, National, General Instrument, Hughes, and Burr-Brown from the United States and NEC from Japan manufacture a variety of semiconductor devices: memories and microprocessors from Motorola, National, and NEC; nonvolatile memories and gate arrays from General Instrument; and custom devices from Hughes and Burr-Brown. Most of these firms develop, manufacture, and market devices that specifically meet European standards; however, at least one firm merely breaks apart and packages devices from wafers that are fully processed at the home plant. Based primarily on the manufacturing output of those companies, Scotland has become the "center of European (Common Market) semiconductor manufacturing," producing 21% of Europe's requirements and 79% of the United Kingdom's needs.

Technologies involved include NMOS, CMOS, HMOS, bipolar, SOS, and hybrid. Most companies use, or plan to use, 4″ or 5″ wafers and 2-, 2.5-, or 3-micron geometries. Numbers of employees currently range from 35 to 1300, facility sizes

(continued on page 52)

Silicon Glen

(continued from page 50)

from 35,000 to 150,000 ft^2 (3000 to 14,000 m^2). Projections for current and future expansions call for from 700 to 2100 employees and 75,000 to 300,000 ft^2 (7000 to 28,000 m^2) of space.

Apparently, there is no lack of either engineering talent or skilled or trainable personnel. Several colleges and universities provide a fine pool of well-educated electronic engineers. Generally, electrical engineering departments stress microfabrication, computer technology, or microelectronics with particular emphasis on the needs of the semiconductor fabrication companies.

Non-engineering personnel are also readily available and, according to company representatives, there is little problem in training them to meet the requirements for fabrication or technician positions. At least one company hires mostly inexperienced personnel (as young as 16 years old) and molds them to set specifications.

Of course, the concentration of semiconductor fabricators is backed by a proliferation of material suppliers. For example, Barr & Stroud provides germanium and lithium niobate wafers; Heraeus Silica, fused silica and quartz glass; and Compugraphics, semiconductor masks. The proximity of these suppliers guarantees the necessary working materials without the relatively long delays required to receive shipments from the Continent or the United States.

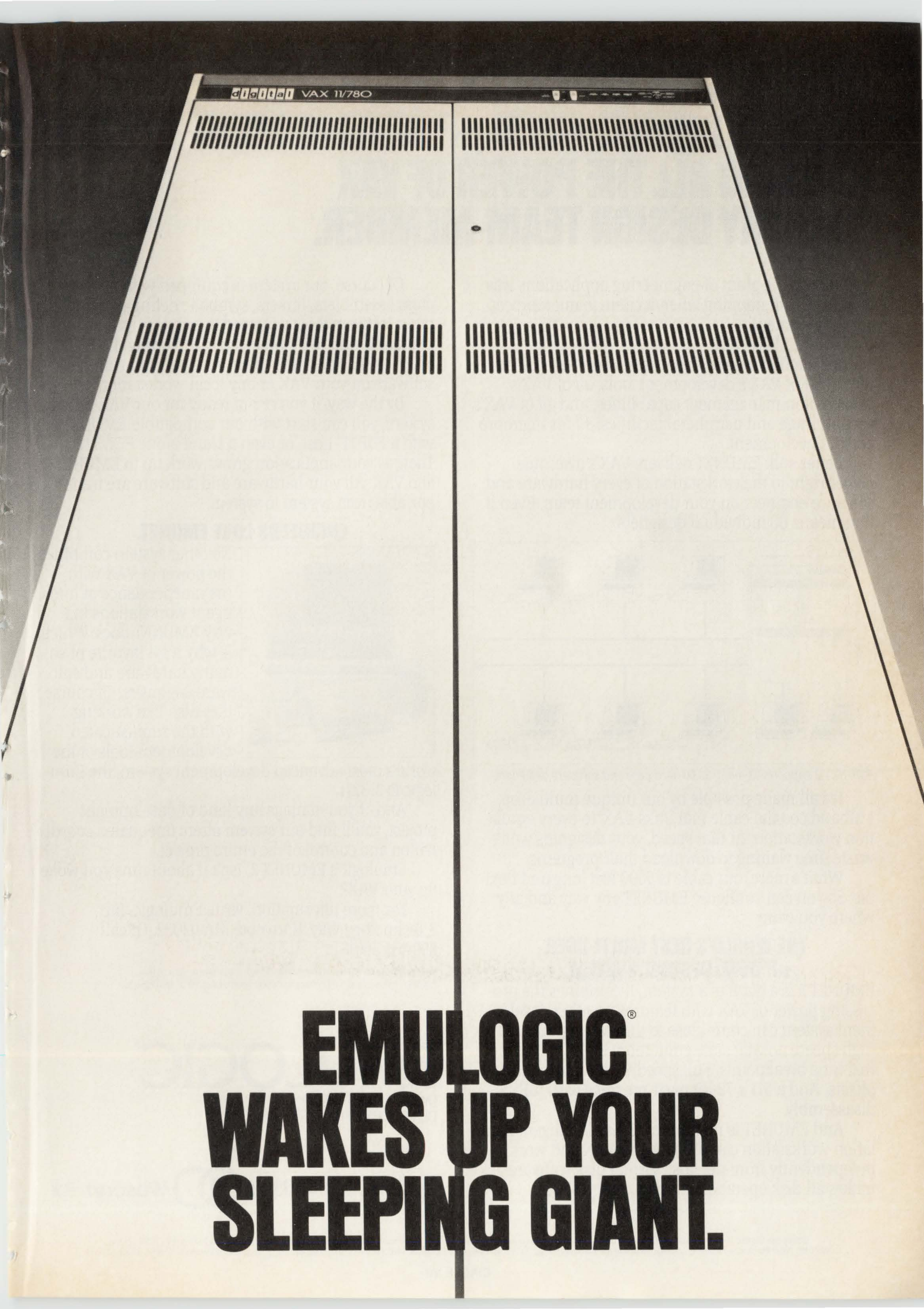
University/college backup

Three scholastic institutions, the major sources of engineers for the area, are influenced by the requirements of semiconductor and related firms. Each has its particular areas of specialization, which are noted in the research grants funded by the U.K. government's Science and Engineering Research Council (SERC), the U.K. Ministry of Defence, and private firms.

Glasgow University's Electronic and Electrical Engineering Department fits its research projects into two broad classes. In the first class—electronics and materials engineering—studies include very high resolution electron beam and X-ray lithography as well as molecular beam epitaxy of semiconductor compounds. Concentration in the latter area covers gallium arsenide, indium phosphide, aluminium gallium indium arsenide, and the lithium niobate group of materials. Systems engineering—the second research class—includes control and simulation and pattern recognition.

(continued on page 56)

 CIRCLE 27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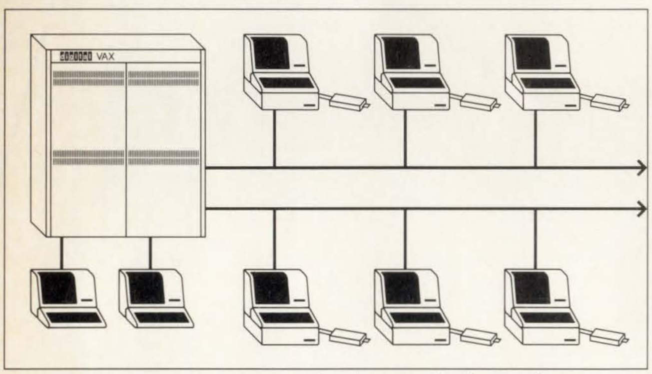

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CIRCLE 29

VAX 11/780
REGISTERS HS MAPPING TRACE SYSTEM
D0 00000006 A0 00000100 MFC FROM TO ASSG TYP ON OFF BREAK POINTS
D1 12345678 A1 00050000 - 000000-000000 0 OFF B7 > B0 000230 ON
D2 00005555 A2 00050003 S 000000-007FFF 1 RAM B1 UNDEF OFF
D3 00056789 A3 00042354 S 008000-00FFFF 2 RAM B2 UNDEF OFF
D4 FFFF0000 A4 00F0FF0E B3 UNDEF OFF
D5 00770077 A5 00000000 SFC 6 B4 UNDEF OFF
D6 00000FFF A6 00F0FEFE DFC 6 B5 UNDEF OFF
D7 00BBBBBB US 000014FE VBR 00000100 T S I X N Z V C EFC B6 UNDEF OFF
PC 000200 SS 000003F0 SR 2705 0 1 7 0 0 1 0 1 6 B7 LOGICAL ON
LOC ADDRESS INSTRUCTION DATA
499 00022C TRAP #0 4E40 00000000 6 1111 7 11 0 00 11 1 1
500 00022E NOP 4E71 00000000 6 1111 7 11 1 00 11 1 1
501 0003F4 DATA 022E 00000000 5 1111 7 11 0 00 11 0
502 0003F0 DATA 2700 00000000 5 1111 7 11 0 00 11 0
503 0003F2 DATA 0000 00000000 5 1111 7 11 1 00 11 0
504 0003F6 DATA 0080 00000000 5 1111 7 11 0 00 11 0
505 000180 DATA 0000 00000000 5 1111 7 11 1 00 11 1
506 000182 DATA 0230 00000000 5 1111 7 11 0 00 11 1
TYPE: 68010
FREQ: 8000 KH
SCNT:
MODE: COMMAND
EMULOGIC

Silicon Glen
(continued from page 52)

Most of the research in these areas is application oriented, but work is also being carried out on the development of general techniques.

Current research at Paisley College of Technology involves electro-optical effects in liquid crystal films, gas discharge physics, reliability of monolithic integrated circuits, mathematical modeling of electromechanical devices, image processing, and robotics. The College also provides consultant services to industrial organizations and arranges short courses within companies.

One of Britain's largest and most modern universities, Edinburgh University, obtains £8M of its £60M income from research grants and contracts. All of its research and development activities fit under an umbrella that the University calls "information technology" (IT). Unlike the scope of work at most other educational institutions, IT includes the development of products that can then be sold for profit. Wolfson Microelectronics Institute, a fully commercial subsidiary company handles that phase of operations.

Artificial intelligence

As in many academic and industrial organizations throughout the world, artificial intelligence (AI) is recognized at Edinburgh University as an important discipline. Its AI Department collaborates with other departments within the University as well as with the Masachusetts Institute of Technology (robotics), Stanford University (natural language), and Carnegie-Mellon University (the PERQ machine) in the United States, and Grenoble University (robotics) in France.

Under a SERC grant, the AI Department has been investigating the use of robots for assembly tasks. Research Fellow Mrs Patricia Ambler and Research Associate Mr Chris Malcolm said that members of their project are experimenting with a Puma robot to assemble a simple wooden model. They are developing a robot command language called RAPT for robot APT. (APT is the better known acronym for automatically programmed tools, a numerical control language.)

RAPT, which can be used with other robots as well, is intended for use by non-computer experts to program assembly robots. Assembly tasks are programmed in terms of the job to be done and how objects are to be fitted together instead of how the manipulator should be moved.

Other areas of study in the AI Department include languages and systems, mathematical reasoning, vision and remote sensing, natural language, planning systems, and computers in education. The last area uses LOGO, which is equivalent to a substantial subset of LISP. And, of course, the Department is involved in intelligent knowledge based systems—more commonly known as expert systems. (For a recent review of an application for the latter, see "Prospects for Expert Systems in CAD," by Mark J. Stefik and Johan de Kleer, *Computer Design,* Apr 21, 1983, pp 65-76.)

—Syd Shapiro, Managing Editor

SYSTEM TECHNOLOGY
(continued on page 63)

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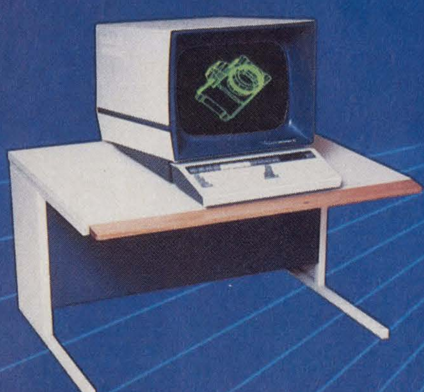
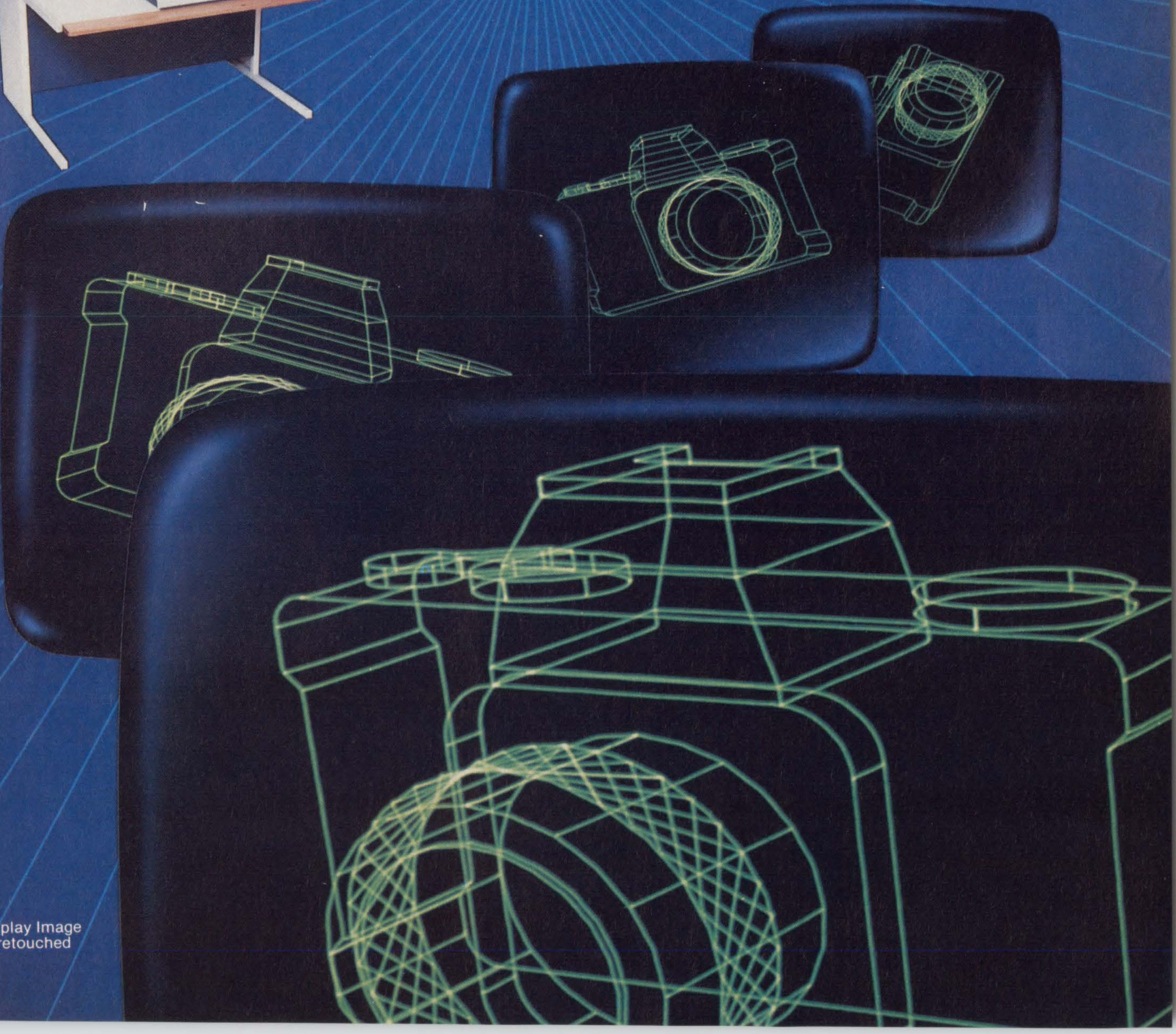
CIRCLE 31





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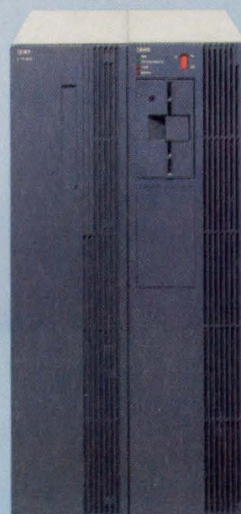

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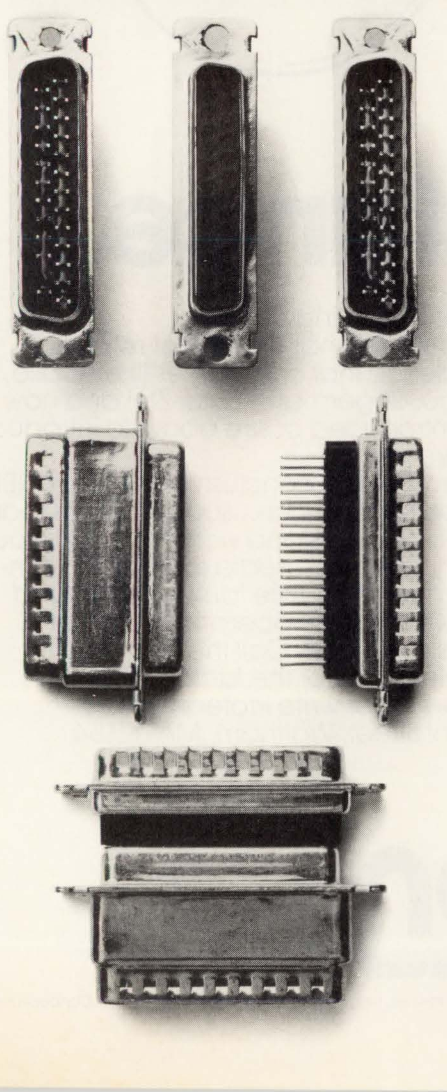
*UNIX is a trademark of Bell Laboratories.

CIRCLE 32

Capitol Punishment.

D Subminature Transverse Monolith Filter Connectors



to help meet Docket 20780 requirements.

The addition of the transverse monolith filter expands the technical versatility of the D Subminiature without adding to the overall dimensions of the connector. And these Cannon connectors are available in contact arrangements of 9, 15, 25 and 37, with a wide range of capacitances and cutoff frequencies offered.

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For more information on Transverse Monolith Filter Connectors, contact Phoenix Division, ITT Cannon, 2801 Air Lane, Phoenix, AZ 85034. Telephone: (602) 275-4792.

Contact Commercial/Industrial Products for more information on the D Subminiature Shielded D Series. ITT Cannon, a Division of International Telephone and Telegraph Corporation, 10550 Talbert Avenue, Fountain Valley, CA 92708. Telephone: (714) 964-7400.

CANNON ITT

The Global Connection

CIRCLE 33

Controller mixes different disk drives

Support of up to two different types of Digital Equipment Corp disk drive configurations on its four parts is Emulex Corp's claim for its Model SC31-BX emulating controller. In addition to emulating over 60 different RP and RM drive configurations, the SC31-BX can also map multiple logical disk drives on a high capacity physical drive for lower per-byte storage costs.

Any SMD-compatible disk drive (80M bytes or larger) can operate on the Unibus of PDP-11 and VAX-11/730 computers using the controller. Both conventional data rates (1.2M bytes/s) as well as the faster throughput of high density disk drives (1.8M bytes/s) are supported. In this way, users can take advantage of newer storage technologies while still retaining older disk drives for archive and image backup.

Unlike other disk controllers that use separate firmware sets for each drive family, the SC31-BX contains in its firmware the necessary drive parameters for all popular disk subsystems supported on the PDP-11 and VAX-11/730 computers. In PDP-11 Unibus applications, the controller emulates the RH-11 interface operating with RM-02/RM-03/RM-05/RM-80 or dual RP-06 disk subsystems with capacities ranging from 67.4M to 348.8M bytes. For the VAX-11/730, the RH-11 interface is also used to emulate RM-02/RM-03/RM-05/RM-80 or expanded RM-80 disk subsystems with capacities up to 405.2M bytes. Furthermore, no firmware changes are necessary to use the controller in any of the predefined configurations since all changes are switch selectable.

Its flexibility also extends to the ability to mix two drive types on any of the four ports. The user is required to specify only the physical address of the desired disk drive and the port address on the controller. This capability is similar to that of smart printer controllers that can address different types of parallel and serial printers through software intervention.

On the SMD interface side, the SC31-BX can operate drives with differing numbers of heads and cylinders. A configuration PROM set at the factory defines the necessary drive parameters according to user specifications, and the firmware converts these to the desired DEC-compatible configurations.

In a similar manner, multiple DEC disk drives can be emulated on a single high capacity physical drive. Such an approach typically requires changes in the drive parameters stored in firmware and modifications to the software drivers, however. An advantage to such an implementation is the extended storage capacity possible, (especially in the newly introduced 500M-byte drives), with relatively minor modifications.

Similar efforts are made to support SMD drives with the faster data transfer rate (1.8M bytes/s). Existing software drivers already provide the capacity for high transfer rates, but were deliberately limited to take into account bus restrictions present when Unibus was first conceived. The SC31-BX provides an 8K buffer to accommodate as many as 14 sectors during high speed transfers.

Furthermore, a DMA throttle monitors the waiting time for other pending requests, and can suspend the controller's activity to allow for other DMA transfers. A programmable deadband time can also be implemented so that CPU functions (including interrupt servicing) are not locked out for excessive amounts of time by disk transfers. Thus, bus contention can be "fine tuned" for optimum system throughput on heavily populated Unibus configurations.

All DEC operating systems and diagnostics can be used with the controller, with onboard internal self-test also provided via LED displays. The SC31-BX also generates a 32-bit error correction code to correct single error bursts up to 11 bits and to detect longer length bursts.

(continued on page 64)

Controller mixes
(continued from page 63)

Both PDP-11 and VAX-11/730 versions of the controller reside on a single hex printed circuit board that takes up only one small peripheral control slot. The VAX-11/730 version also comes with the VAX/UM software package that consists of the formatter, driver, boot routines, and diagnostic modules. Either version can generate DEC-compatible media when the disk pack is identical to that of the equivalent DEC drive.

Single-unit pricing for the SC31-BX starts at $4900. Delivery is quoted at 30 days ARO. **Emulex Corp,** 3545 Harbor Blvd, Costa Mesa, CA 92626. **Circle 212**

Buffering tape controller speeds data transfers

Using a 64K-byte buffer, the Tape Dimension III controller from Western Peripherals (Irvine, Calif) accommodates data transfers to half-inch tape drives at speeds approaching 125 ips. A separate Unibus frontend processor handles the necessary handshaking needed for TS-11 emulation on Digital Equipment Corp's VAX-11 and PDP-11 computers, while the main processor can manipulate data in any of three recording formats, ie, nonreturn to zero inverted (NRZI), phase encoded (PE), and group code recording (GCR).

The large onboard buffer makes the emulating tape controller ideal for demanding applications such as data acquisition and high speed backup of Winchester disk drives. Such applications typically record data at 6250 bpi (GCR format). Other controllers with small buffers often generate data late conditions because of the need for multiple DMA transfers. In realtime situations like satellite telemetry and seismology, data late conditions often cause information to be lost. Other applications see an overall degradation in system performance as these controllers interrupt the bus many times to transfer information.

In contrast, the Tape Dimension III requires only a single DMA transfer to obtain data. Thus, it acts as an intelligent data staging area that minimizes the number of start/stop operations occurring on the tape drive. In fact, the controller is capable of on-the-fly transfers if the host processor can pass data at the maximum 800K-byte/s capacity of GCR tape drives operating at 125 ips. This is usually not the case because of the amount of system traffic that occurs along the bus, especially the slower programmed I/O transfers involving peripherals like card readers and line printers.

Critical to its high throughput is the controller's asynchronous Unibus frontend control logic that handles bus arbitration without supervision of the main bit-slice processor. Other controllers require that asynchronous control signals be synchronized with the clock of the onboard processor (eg, 200 ns for 2901-based controllers) in order to test signals and take necessary action. Delays imposed by synchronization often lead to reduced efficiency since the controller must either hog the bus or relinquish control many times.

Meanwhile, the control logic on the Tape Dimension III acts as a Unibus sequencer for the onboard processor. It takes asynchronous commands issued along Unibus and directly executes necessary actions needed for bus arbitration. The onboard bit slice processor merely issues commands that call for read/write operations between the host processor and associated tape drives.

This controller will handle up to four dual-density drives or four
(continued on page 66)

Tape controller

(continued from page 64)

tri-density drives. Tape transports can be configured to run at speeds up to 125 ips, as well as intermix recording densities in 9-track NRZI, 9-track 1600-bpi PE format, or 6250-bpi GCR formats. The controller itself takes up a single printed circuit board that resides in a standard small peripheral control slot. Thus, no special backplane or cabinet is required. Interface cable connectors link the controller to the user-selected formatter.

The controller is completely software transparent to the VAX-11 and PDP-11 Unibus environment including VMS diagnostics. Single-unit price for the Tape Dimension III is quoted at $1983, with OEM quantity discounts available. Delivery is specified at 60 days ARO. **Western Peripherals,** 14321 New Myford Rd, Tustin, CA 92680.
Circle 213

SOFTWARE

Ada compilers—validated and available at last

After several years of debate, followed by a couple of years of frantic coding, compilers for the U.S. Department of Defense (DoD) standard computer language, Ada, are finally available. On April 11 of this year, the DoD's Ada Validation Office approved New York University's Ada/Ed compiler—a large, slow version targeted for educational applications. It has extensive error-handling abilities and provisions for checking input program semantics.

In mid-June, Data General (Westboro, Mass) and ROLM Corp (San Jose, Calif) also received a validation certificate for a compiler they developed jointly. Software developed for Data General machines runs on ROLM's mil-spec computers, and ROLM offers an Ada development workstation centered on its MSE/800 32-bit minicomputer. The workstation provides several ports for up to eight users, and produces code for several different processors by cross-compilation.

At present, these are the only products that can be advertised and sold as Ada without further qualification. Other products on the market featuring the name prominently in their advertising are either subsets of the standard language, or Ada-like languages with nonstandard extensions.

Dealing with delays

Intermetrics (Cambridge, Mass), one of the earliest contenders in the Ada compiler development race, faces delays in bringing its own validated Ada compiler to market. As a result, a company spokesperson describes the relationship between Intermetrics and its client, the Air Force, as "at a sensitive point over renegotiation of schedules." A 4-month schedule slip has already resulted from the Air Force's insistence upon additional quality-assurance testing. Lately, reliability problems encountered by the government with other Ada projects and contractors have heightened quality-assurance awareness.

The company stresses, however, that it intends to have a production quality, high performance, optimizing compiler available by Nov 1984. Target performance is 1000 lines of code/min, in contrast to the lethargic 200- to 600-line/min performance the present ROLM/Data General Ada compiler supports.

Down the road at SofTech Inc (Waltham, Mass), Ada project development is also encountering delays. A company spokesperson indicates that this is due to the Army's modification of original project contract specifications. Since the Army has specified additional software tools, SofTech's delivery dates have slipped six months. Delivery is slated for July 1984.

SofTech emphasizes, however, that its package is an entire Ada environment, not merely a compiler. Its Ada Language System incorporates tools, utilities, and full documentation, all of which will be available simultaneously.

When asked if the Army's respecification of its Ada project smacked of changing the rules while the game is in progress, SofTech's spokesperson (who preferred to remain anonymous) said that this sort of thing was par for the course with military contract work. This spokesperson added that as the deadline for Ada project completion drew near, the Army became more realistic and less grandiose in its expectations.

Only Ada will be acceptable

As a programming language, Ada will be tremendously important because of the sheer number of software contracts that the DoD issues every year. In the future, all of these contracts will require that the programming be done in Ada. No more FORTRAN, no more COBOL, and no more Jovial.

However, the fact that a given implementation of Ada is only a subset is not necessarily a reason to be wary. TeleSoft, (San Diego, Calif) has a fairly complete subset that has been accepted by the Joint Program Manager for the World-Wide Military Command and Control System (WWMCCS) as a basis for software development tools on pathfinder projects. The company is proceeding with development of a compiler for the full language but has not achieved it yet, nor has it received a validation certificate.

Gould Inc's SEL Computer Systems Division (Fort Lauderdale, Fla) has announced an Ada

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Ada compilers
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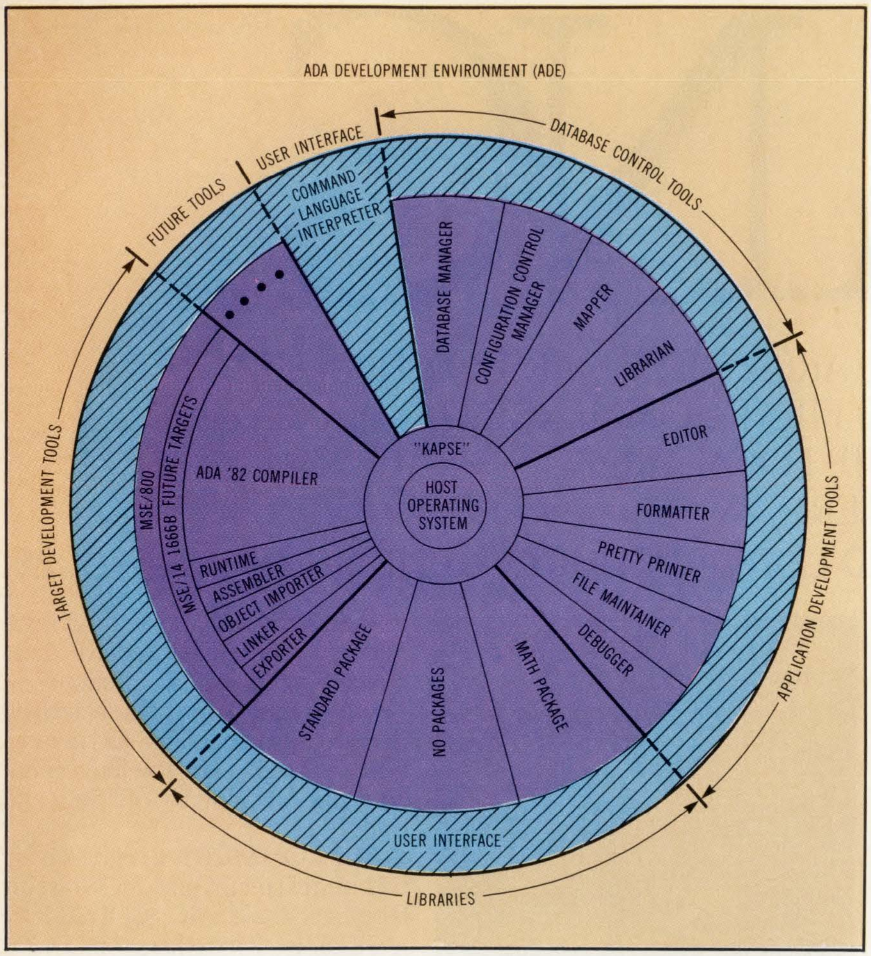

Ada includes a programming system environment as well as a programming language. The Kernel Ada Programming System Environment (KAPSE) interfaces with the host system to provide facilities and I/O functions for Ada programs.

Learning Environment (ALE) package, running on its Concept/32 computers. While not validated as full Ada yet, it is described as a complete hardware and software package designed to teach programmers how to use Ada.

The ALE package adopts a novel approach to generating object code—Ada text the programmer inputs is processed through a translator program to produce C language source code, which is then compiled to machine code. The C intermediate step allows applications to be relatively machine independent, while avoiding the costs involved in writing separate Ada compilers for each separate machine on which they might run. In addition, C compilers exist for almost every computer type.

Other subset compilers range from good to questionable. Some very small subsets are a long way from certification and may never achieve it. A large, experienced programming staff is needed to generate a compiler for such a large, complicated language; this may be beyond the ability of a small organization.

Nonstandard compilers will almost certainly never be validated, nor do the developers seriously intend to seek validation. While they may be excellent languages in and of themselves, and good ways to learn standard Ada programming, they will not be acceptable to the DoD, which is very firm about language requirements.

Some drawbacks

Ada has been described as being "out of PL/I by Pascal," since it combines structure and type checking with large size and complexity. Putting aside the questions raised by C.A.R. Hoare in his 1980 Turing Award Lecture (about whether it is possible to make all of the parts of the language work), Ada's sheer size and complexity mitigate against ease of use and efficiency.

Only the largest and fastest 16-bit microcomputers will have the power to handle the language and its development environment. Unless the developer applies special care and a certain amount of genius, both the compiler and the object code it produces are likely to be slow and clumsy. Diagnostic messages and development tools may or may not be helpful, or even available.

Thus, careful analysis of individual compilers and packages is in order, before making major capital expenditures on either the software or equipment. Most major hardware and software vendors are working on Ada implementations or machines, and can provide technical information.

The Ada Joint Program Office has subcontracted with the IIT Research Institute to maintain an Ada Information Clearinghouse (AdaIC), to disseminate information about the current status of the language and available products. A letter to them at PO Box 849, Rome, NY 13440, produces a large packet of information, including instructions on how to access an online information data base maintained at the University of Southern California.

The Association for Computing Machinery (ACM) has an Ada Technical Committee (AdaTEC) as part of its Special Interest Group on Programming Languages (SIGPLAN). Information on publications and charges is available from the ACM, 11 W 42nd St, New York, NY 10036.

An Ada Language Reference Manual (MIL-STD-1815A) is available from the U.S. Government Printing Office, Superintendent of Documents, Washington, DC, 20402. The price is $8, and the stock number is 008-000-00394-7.

Copies of Ada/Ed are available on magnetic tape (Order No AD A110 710, Ada/Ed NYU) for a $300 nominal reproduction charge. In

(continued on page 73)


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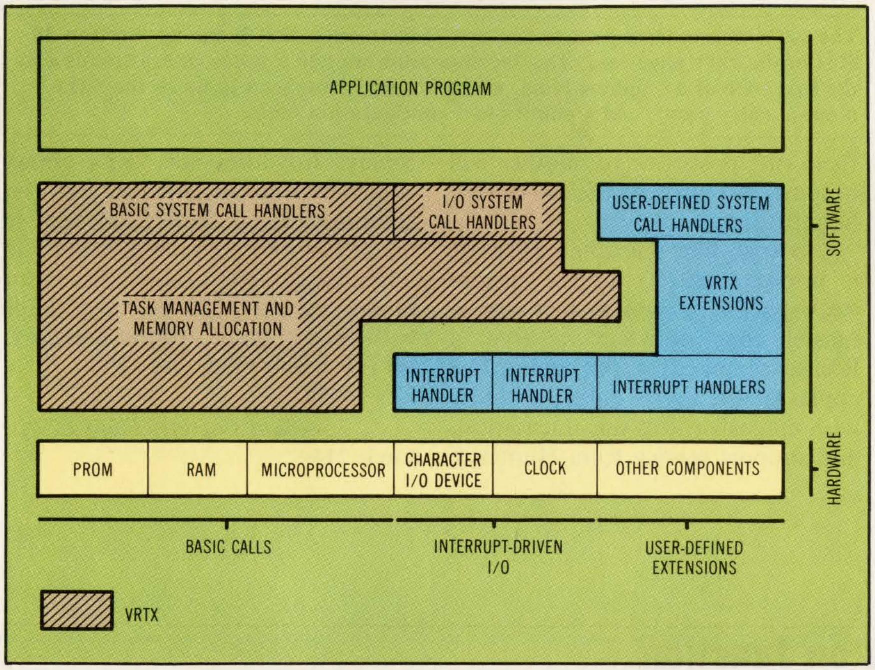
Ada compilers
(continued from page 68)

addition, an Ada compiler Validation Implementor's Guide is available in paper or microfiche (Order No AD ADA 091-760) for $23. Both can be obtained from the National Technical Information Service (NTIS), 5285 Port Royal Rd, Springville, VA, 22161.

ROLM's Ada Work Centers cost from $158,965 to $409,665 and are quoted as available within 90 days ARO. Gould's ALE workstations range in price from $129,000 to $366,000, although the software is available at a lower price for users who already have Concept computers.

—Sam Bassett, Field Editor

Kernel for 8-bit systems gives 16-bit functionality



The basic VRTX system provides an interface between the application programs and the hardware on which they run. Software hooks provide the ability to build custom interrupt handlers and system call functions into the applications.

A ROM-resident realtime operating system kernel has been developed for Z80-based machines used in embedded applications. Produced by Hunter & Ready, Inc and endorsed by Zilog, Inc (Campbell, Calif), the kernel does not require the time-consuming and difficult development process typical of one created from scratch. This kernel allows software written in high level languages on 16-bit machines to run on Z80s without significant alterations.

Hunter & Ready has been producing the Versatile Real-Time Executive (VRTX) multitasking kernels in ROM for the Motorola 68000, Zilog Z8002, Intel 8086/88 and 186/188 for several years. With the introduction of the VRTX/80 8-bit version, which is also compatible with the new Zilog Z800 CPU, realtime multitasking is available in 8-bit applications as well.

Designing and coding multitasking executives for embedded microprocessor systems can be a long and painful process. Working out the details of timing, message passing, and interrupts requires many man-months of expensive programmer effort.

Since the majority of all microprocessors (up to 80%) go into embedded applications, where the end user of the product does not necessarily know what provides its intelligence, any savings in programming time translates directly into lower product price. Just as standard hardware components and peripherals save design time, standard software components that interface easily with applications code can save programming time.

VRTX functions

The VRTX kernel is about 4K bytes long, and can reside anywhere in the processor's address space. Gaining access to kernel functions is done via an unconditional jump to a fixed address in the VRTX ROM module, while parameters are passed in the processor's registers. Thirty-two available calls provide task management, memory allocation, communication and synchronization functions, realtime clock support, character I/O for a serial terminal device, and interrupt servicing. Software hooks are also provided for user-defined system calls and interrupt handlers.

Hunter & Ready provides interface library packages for a variety of C, Pascal, and PL/M compilers. The user can thus include the appropriate library, and a single source-code program can then be compiled and run on any of the supported processors. Of course, details of particular I/O requirements vary from system to system, and processor to processor, but these are normally contained in separate library packages anyway, and not hard coded into the application program itself.

Having produced VRTX versions for most major microprocessors in use today, the company indicates that the next step is to put other parts of a normal operating system into ROM—possibly beginning with file systems. This would be significant because file systems, like CP/M or Unix, are the most time-consuming part of an operating system to build,
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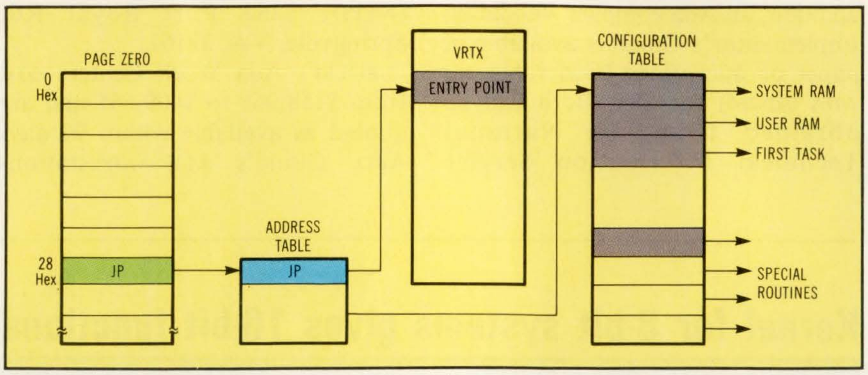
Kernel for 8-bit systems

(continued from page 73)

next to task management. The prospect of standard operating systems, complete with identical file structure, I/O, and realtime operation (which would run on virtually any microprocessor) would alleviate the virtual Tower of Babel that incompatible disk formats, idiosyncratic I/O handling, and the re-invention of the wheel have inflicted on today's microcomputer world.



The VRTX/80 is entered by a restart (RST 5) instruction that jumps to location 28 Hex in the Z80's page zero. This location must contain a jump (JP) instruction to the first byte of an address table, which in turn, contains a jump to the VRTX internal entry point, and a pointer to a configuration table.

Marketing agreement made

At the same time Hunter & Ready announced the availability of VRTX/80, Zilog announced a cooperative marketing agreement with the company. Under this agreement, each company recommends the other's products and participates in joint marketing efforts for the Z8002, Z80, and VRTX versions each supports. Zilog thus joins Hewlett-Packard and Mostek in endorsing VRTX, an indication that applications will have a broad base of support from several manufacturers, and that code migration from one processor to another will become increasingly easier—a very hopeful sign.

VRTX/80, like the other versions, is priced at $2750 for the custom R&D package, which includes a master copy of VRTX in ROM, a license to make five R&D copies, five copies of the user's guide, a binder with extensive R&D documentation, and support service from Hunter & Ready. Royalties for VRTX binary copies that are installed in end-user equipment range from $300/copy in quantities of 1 to 9, to $75/copy in quantities of 100 to 499. Prices for quantities over 500 are negotiable with the company. **Hunter & Ready, Inc**, 445 Sherman Ave, Palo Alto, CA 94036.

—Sam Bassett, Field Editor

Circle 214

PERIPHERALS

Graphics systems—focus on function

Making it obvious that microcomputers have become a force to be reckoned with in graphics systems, Stephen A. Mucchetti, director of the 1984 National Computer Graphics Association Conference, announced that Computer Graphics '84 will "systematically and purposefully incorporate sessions and exhibits acknowledging their active role." The role that microcomputers play in the graphics industry was further emphasized during the session "Hardware Directions of the Future," chaired by Carl Machover at this year's NCGA conference in Chicago. During this session, Michael Coffman summarized the past and gave clues to the future in his paper on low cost workstations, stating "the microprocessor made the low cost workstation possible, and it is the more powerful microprocessors that will drive the workstation into application areas currently reserved for more powerful computers."

How much has already been accomplished using the humble microprocessor becomes obvious from looking at some products introduced at the 1983 NGCA conference held in Chicago. Benefiting from the performance gained from 16-bit microprocessors, graphics workstations continue to drop in cost while providing increased function integration.

While programming new applications has been the traditional means of expanding into markets, this has left many user needs unfilled. The demand for increased productivity can be filled only by allowing automatic movement through the steps involved in taking a product from concept to design and into manufacturing. An ideal package would thus take low cost microcomputer technology and package it with software that automates the overall design process. Taking one step in this direction, a graphics processing unit aimed at schematic entry and PC board design runs automatic placement and routing programs that can cut week long design cycles down to a few hours.

Micro offloads realtime routines

Based on three microprocessors and a dual-ported memory, Telesis Systems Corp's (Chelmsford, Mass) graphics engine architecturally supports sophisticated CAD applications. Retrofittable to the existing LSI-11/23-based workstation, the enhanced graphics processor plugs into the Q-bus to make 512K bytes of dual-ported memory accessible to both the -11/23 and a 68000 microprocessor. The 68000, operating realtime with the -11/23, controls the graphics processing unit with its

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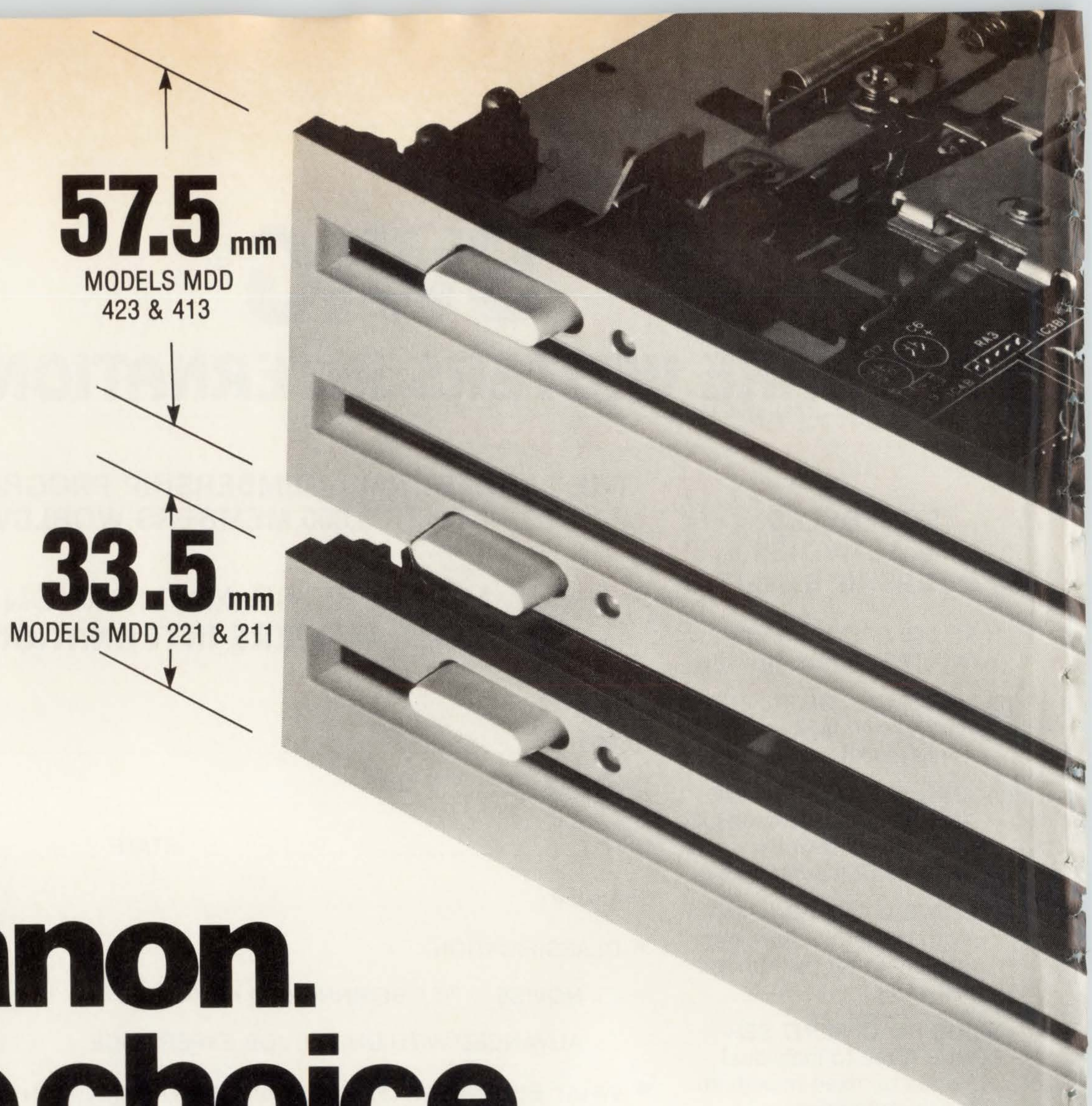

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Canon gives you lots of choices with their 5-1/4″ floppy drives and lots of reasons why they should be your choice.

The choices:
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- 96 TPI — or 48 TPI.
- Single drive — or double drive.
- Double drive with two stepper motors.

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Our single drive is only 33.5 mm high — 20% less than a standard half-height drive; our double drive is only about two-thirds the height of a full size drive.

The single drives weigh 1.2 Kg, the double drives 1.9.

The single drives use 0.8A (12V and 5V); the double drives 0.9A (5V) and 1.3A (12V). As you can see, our double drives use 25% less power than two separate single drives — even ours!

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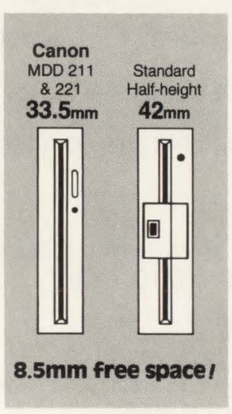

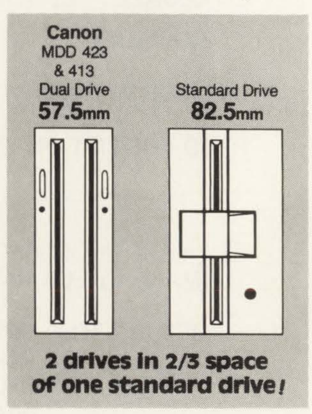

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Canon

CIRCLE 40

Graphics systems

(continued from page 74)

Intel 8085 and NEC 7220 chips. Thus, time critical realtime routines are offloaded from the -11/23 and executed five times faster by the 68000.

Ancillary features resulting from this power include the ability to change magnification of a displayed picture instantaneously through hardware supported zoom. World/Window allows operators to toggle back and forth at the flick of a lightpen between display of the world (entire drawing) and display window. The world view permits the operator to adjust roam space and thus the resolution of the image being displayed. Two roaming schemes smoothly move the window over the entire 2k x lk bit map.

Proprietary automatic placement and routing programs operate visually—operators watch progress in realtime on the workstation screen. There are no limitations on grid size, number of components, or number of connections. The placement algorithm simultaneously considers clusters of components and places them based on connectivity relationships. Synergy between the placement routine and the router increases the resulting number of successful routes. Completion rates with the router vary between 92% and 95%.

Micro controls bit-slice processor

As terminal or communicating workstation, the Jupiter 12 supplies 1280 x 1024 displayable resolution that is enhanced by antialiasing of vectors and solids as well as alphanumerics, using a proprietary edge filtering system resident in the terminal.

Based on a dual-processor architecture using an MC68000 and a bit-slice processor, Jupiter System's (Berkeley, Calif) terminal supports a 60-Hz noninterlaced refresh rate at maximum resolution. The standard 19" display supplies 37-Hz interlaced refresh at 1280 x 1024 resolution. Vectors can be written at 300 ns/pixel.

Performing hardware vector generation, the 16-bit bipolar bit-slice processor is loaded and controlled by the 68000 microprocessor. All microcode is resident in writable control store and may be modified or extended by the user. Programmed in C, the microprocessor also handles communication control, display list maintenance, and high level graphics functions. It directly addresses the entire pixel array.

The basic 256K bytes of memory expand to 4M bytes, making up 4 to 32 planes of display memory each 1280 x 1024. A 20 x 1 ECL pixel cache for each plane allows local pixels to be accessed while display memory cycles occur.

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Graphics systems
(continued from page 77)

Graphics capabilities of this machine include 3-D transformations and independent pan and zoom of each memory board. In color lookup table mode, the unit simultaneously displays up to 65,000 of the 16.7 million colors available. As an RGB machine, it can provide 12-bit RGB of either 4 or 8 bits/color with 4 or 8 bit planes for overlays.

High resolution raster displays

Offering a choice between Z80- or MC68000-based controllers as well as among standard features, Ramtek Corp's (Santa Clara, Calif) RM-9465 offers 1280 x 1024 x 4 pixel resolution and up to 24-bit refresh memory planes. Vectors can be written at up to 16,000/s. The system can simultaneously display 1.3 million colors from the 16 million available.

Configured with the Z80, the system has 12K bytes of RAM, expandable to 256K bytes; the MC68000 version offers 240K bytes of RAM. Either unit can have color or monochrome display with local pan and zoom, image enhancement, coordinate transformation, and split-screen clipping.

Priced as low as $11,250, the terminal is basic to the model 9465/CCB CAD/CAM system. The terminal accommodates requirements ranging from 2-D drawings, layouts, and schematics to 3-D wireframe models, as well as high speed generation of shaded pictures for solid modeling. The RM-9465 also supports command and control, image processing, and process control.

Viewable resolutions of 1536 x 1024 are supplied by Aydin Controls' (Fort Washington, Pa) Aycon 2000. The display computer provides 64k x 64k world picture storage and can display 65,000 simultaneous colors out of 16 million hues. Combining an 8-MHz 8086 frontend processor and 8087 coprocessor with 1M byte of system RAM and memory control processor provides fast graphics. The memory control processor yields 63-μs/char write time as well as fast circles, vectors, and transformations. Data/module display resolution storage can run to 6M bytes. This module supplies screen-to-screen DMA, and direct I/O from video digitizer at frame rate speeds.

The system can be equipped with standard interactive devices. In a 6-card chassis containing processor, two memory modules, video output, and parallel DMA I/O boards with power supply, the price is $17,500.

Lexidata Corp's (Billerica, Mass) 1280 x 1024 60-Hz noninterlaced raster-scan color graphics display brings the cost of high resolution down to under $10,000. To generate vectors at up to 42 million pixels/s, the 3700 display processor contains hardware that allows blocks of 80 pixels to be written simultaneously. This block writing feature allows area fills to occur almost instantaneously. Rapid line drawing is enabled by the unit's 750-ns/pixel vector write time.

A desktop graphics terminal offering 1280 x 1024 resolution and displaying 1024 colors, GR-2414 sells for $18,950. Its 60-Hz noninterlaced 19″ display can be written at 25,000 vectors/s. In this terminal, Seiko Instruments Graphic Devices & Systems Division (Milpitas, Calif) provides for high level needs through local interactive processing that supports basic 2-D transformations for scale, rotation, and translation. This unit's graphics processor generates an array of graphics primitives, including circles, arcs, grids, polygons, hatchings, and paintings. Local functions operate on data from the 128K-byte display list segment memory. A clipping feature is built into the system hardware to prevent system speed degeneration.

Claiming 1280 x 480 resolution on a 14″ raster-scan monitor, ID Systems Corp's (Hilliard, Ohio) ID-200 family comes in at $4000—competitive with low resolution units. The terminal's dual video generator presents both alphanumerics and graphics on a single monitor; in addition, it allows the images to be split and displayed on separate monitors. Each monitor can be independently manipulated.

Instantaneous hardware pan and 16 levels of zoom are possible. Eight windows can be displayed simultaneously. Independent color plane control permits multilayer designs. Multimemory architecture allows picture replay without retransmission from the host computer.

Drawing primitives give users a choice of drawing vectors by absolute, relative, or concatenated coordinates. The terminal's fill-until and fill-while algorithms perform both polygon fill and seed fill.

Low cost function

Using a 16-bit Z8002 processor to handle graphics computations that provide area fill and polygon drawing, Intecolor Corp's (Norcross, Ga) 2427D also has an 8-bit 8085 that supports the ANSI X3.64 control system and handles alphanumeric terminal functions. In bit-mapped graphics mode, the terminal offers three 560 x 288 dot-addressable video display planes. It supports standard Tektronix hue, intensity, and saturation, and either relative or absolute color lookup table mapping.

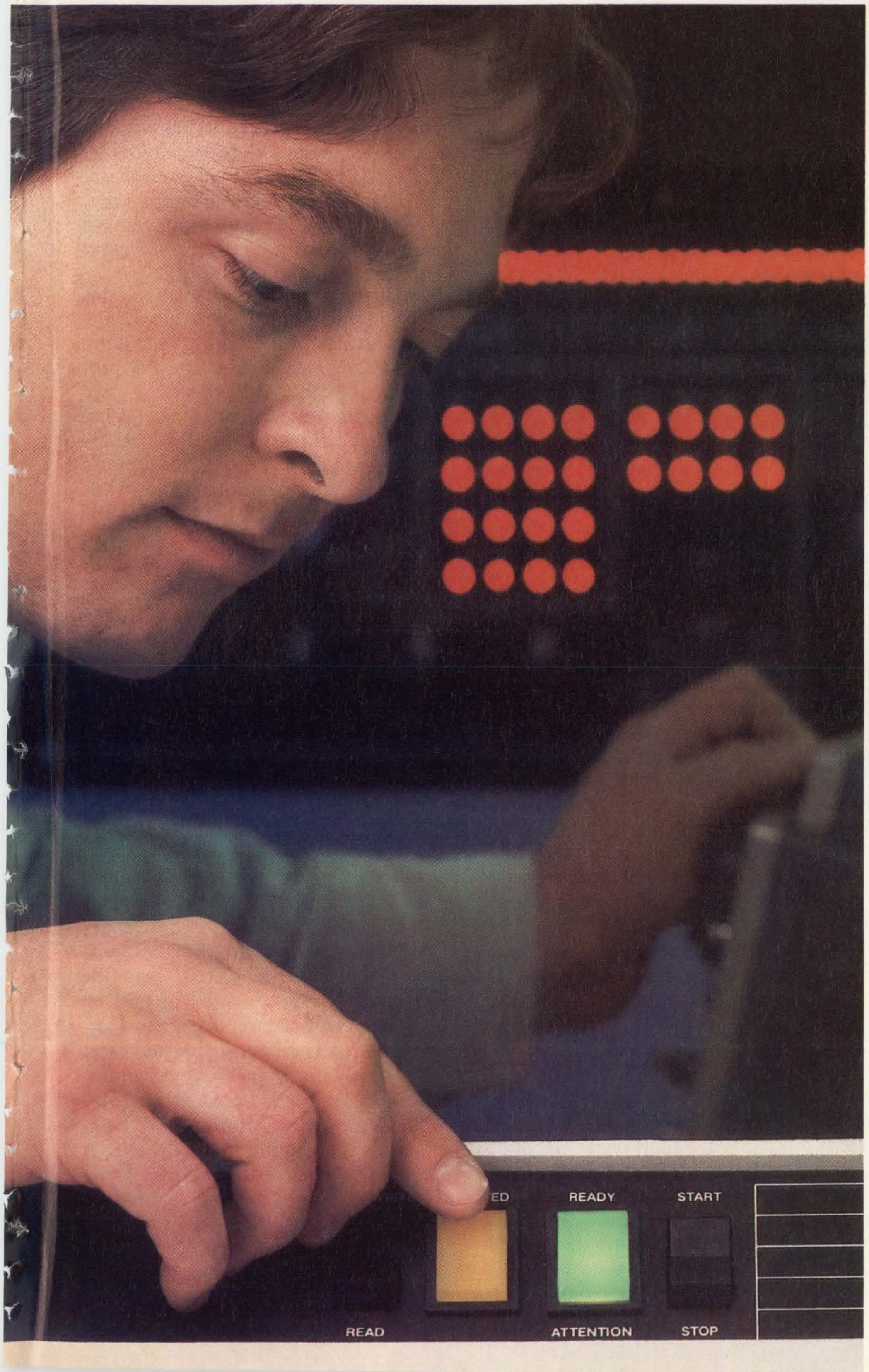
With single commands, the terminal emulates Tektronix' 4010/4014. Programs written according to 4010/4014 protocol run correctly with all features available for color raster technology including plotting, interactive mode, status reporting, and printing. It also emulates most of the 4027's commands and features including arcs and regular polygons, area fill, and interface to color dot-matrix printers. Price is $1995.

Integrating advanced graphics functions with high resolution displays, low cost packages such as these indicate that the future will bring still greater enhancements. Along with the workstation-on-every-desk concept that now seems feasible, perhaps the power of these workstations will allow integration of functions to achieve further productivity improvements.

—Peg Killmon, Senior Editor

SYSTEM TECHNOLOGY
(continued on page 80)

A Memorex team spent over 100,000 man-hours doubling the capacity of this disk storage subsystem. It deserved Dialight switches.



When they committed all those man-hours to bringing off such a feat, Dialight illuminated switches were the natural choice for its front panel.

Dialight has a complete line of computer-grade illuminated switches at reasonable cost. Our rocker and toggle line contains countless combinations of standard colors, sizes, mountings and contact ratings—including front-panel and sub-panel types, plus many styles for snap-in and printed circuit board applications.

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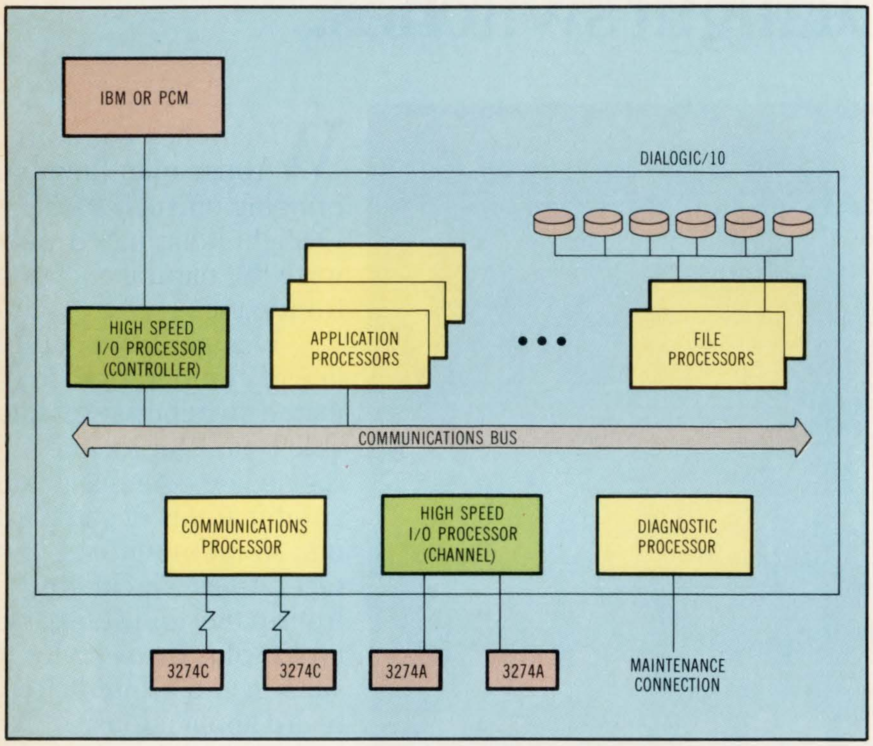
CIRCLE 42

Mainframe satellite supplies subsecond user response



Dialogic/One system's highly redundant architecture contains a diagnostic processor that allows dynamic redistribution of tasks if a component fails. Application processors supply local memory and processing for user operations; system processors handle system functions.

A one, two, three punch cuts through the cumbersome morass of interactive processing in an IBM mainframe environment. The layered interactive processing concept—embodied in the Dialogic/One—distributes batch and interactive computing across different machines while maintaining the user's view of a single system.

Three major components—satellite computer, host-based software, and satellite-resident software—make up the system. Operating in conjunction with an IBM MVS operating system environment, the satellite provides a separate physical layer of processing power. Response conscious tasks can then operate within the satellite processor, while batch jobs are handled within the mainframe.

Since mainframe computers are designed to crunch numbers, interaction with such machines requires sophisticated software. Software techniques can provide a degree of interactivity; however, this is complicated by resulting contention for computer resources between the users and the batch tasks, and the interactive support software itself. The layered concept addresses these problems to provide subsecond response time at low per user cost while preserving a single system image.

To accomplish this, the Dialogic/10 computer sits between the MVS host and terminal user, transparently processing the interactive workload. It connects to the mainframe through a block multiplexer channel and to 3270 terminals through a standard SNA terminal controller. Terminal users retain their traditional view of the MVS system through an ISPF-like editor; MVS perceives the terminal as a normal SNA 3270 device.

The satellite computer's architecture distributes user and system tasks across an interconnected complex of processors. This allows both system and user operations to be done concurrently. The two types of processors within the computer—application and system—communicate with each other across a high speed communication bus made up of 16 serial lines.

Application processors supply local memory and processing power to user operations. System processors are customized for the functions that they perform (file control, host channel communication, terminal communication, and diagnostics).

Host-based software maintains communication between the satellite processor and the host MVS system. Operating as a Virtual Teleprocessing Access Method (VTAM) application, this software establishes all connections to MVS through external interfaces. Other portions of the software reside within the satellite computer. That part of the operating system that is not host resident is distributed over all of the up to 32 68010 microprocessors except those used as application processors. Timesharing option (TSO) replacement software resides within the up to six application processors. This user software, a superset of TSO, includes a set of application packages tailored to application developers and system programmers as well as a high level command language for developing customer written applications.

These application packages include an editor interface similar to IBM's Interactive System Productivity Facility (ISPF) editor, but with extended functions. These suit the system to both new application development and to program maintenance. Better response time increases productivity in these applications. Knowledge-based editors that automatically select appropriate commands and utilities for the user support the added functions.

Price ranges from $198,000 to $385,000 depending on configuration. **Dialogic Systems Corp,** 1335 Bordeaux Dr, Sunnyvale, CA 94089. **Circle 215**

Floating Point Systems array processor to break

The FPS-5000 Series from Floating Point Systems

Now, a new family of products from Floating Point Systems brings increased computing power and unmatched price/performance to the signal/image processing world.

With 3 to 6 times the speed and 4 times the memory capacity of previous FPS products, the FPS-5000 Series provides computing for applications that exceed their present system's capability.

The FPS-5000 Series offers fast, accurate, flexible computing for the most demanding real-time, user-interactive, and production-oriented applications.

Four basic product groups make up the new FPS-5000 Series: the 5100, 5200, 5300 and 5400. Peak performances range from 26 million floating-point operations per second (MFLOP), to 62 MFLOP. Data memory of 0.5M to 1M words is available along with program memory to 32K words.

By combining a distributed architecture concept with the latest VLSI technology, the FPS-5000 Series sets a new standard for cost-effective computing, breaking the $2,000 per MFLOP* barrier—the first time this has been achieved in any floating-point computing system.

*Based on U.S. Domestic Prices

Distributed processing architecture

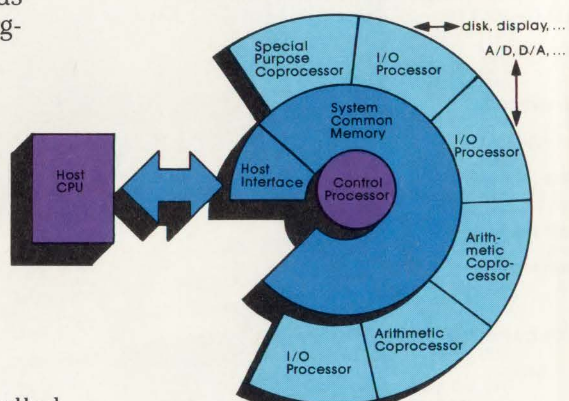
The FPS-5000 Series is a distributed processing system that maximizes throughput by allocating the computational load to a set of high-performance, independent, floating-point processing elements called Arithmetic Coprocessors. Data flow is simultaneously managed

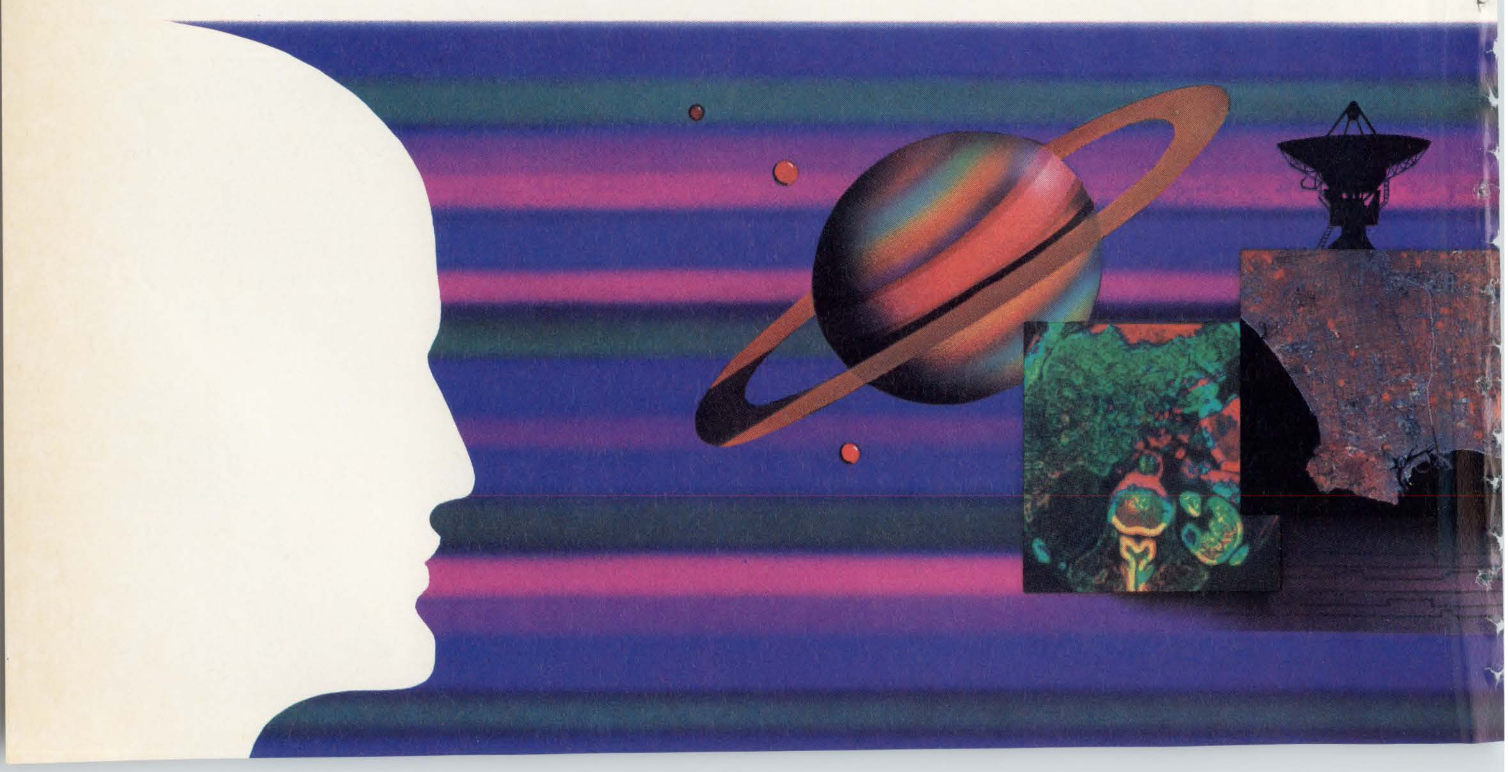
Typical performance examples of geophysical, medical imaging and signal/image processing applications.

Application Example	AP-120B	FPS-5410	5420	5430
1. Demodulation/Signal Analysis	13.8 msec.	6.5 msec.	N/A	N/A
2. Tomography Preprocessing	60 sec.	25 sec.	16 sec.	12 sec.
3. Multispectral Image Classification (512 x 512 pixels 8 Bands, 4 classes)	49 sec.	25 sec.	13.3 sec.	10.5 sec.
4. 2D FFT (512 x 512 complex)	3.4 sec.	1.4 sec.	.7 sec.	.5 sec.
5. Matrix Multiply (100 x 100)	439 msec.	177 msec.	96 msec.	71 msec.

Based upon specifications subject to change.

FPS-5000 Series Architecture





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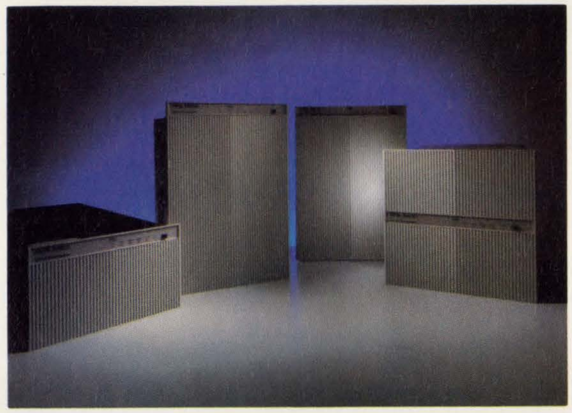

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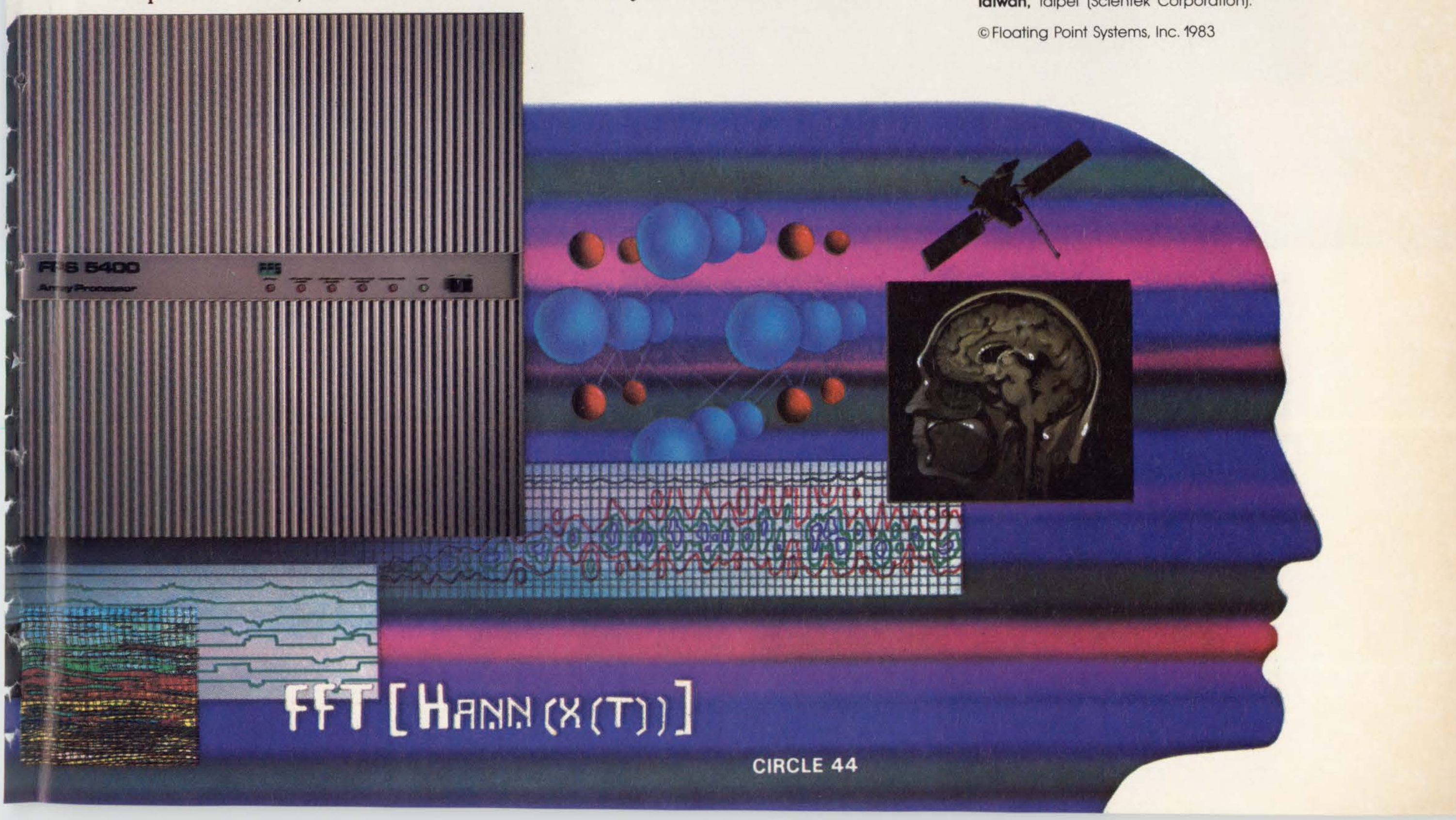

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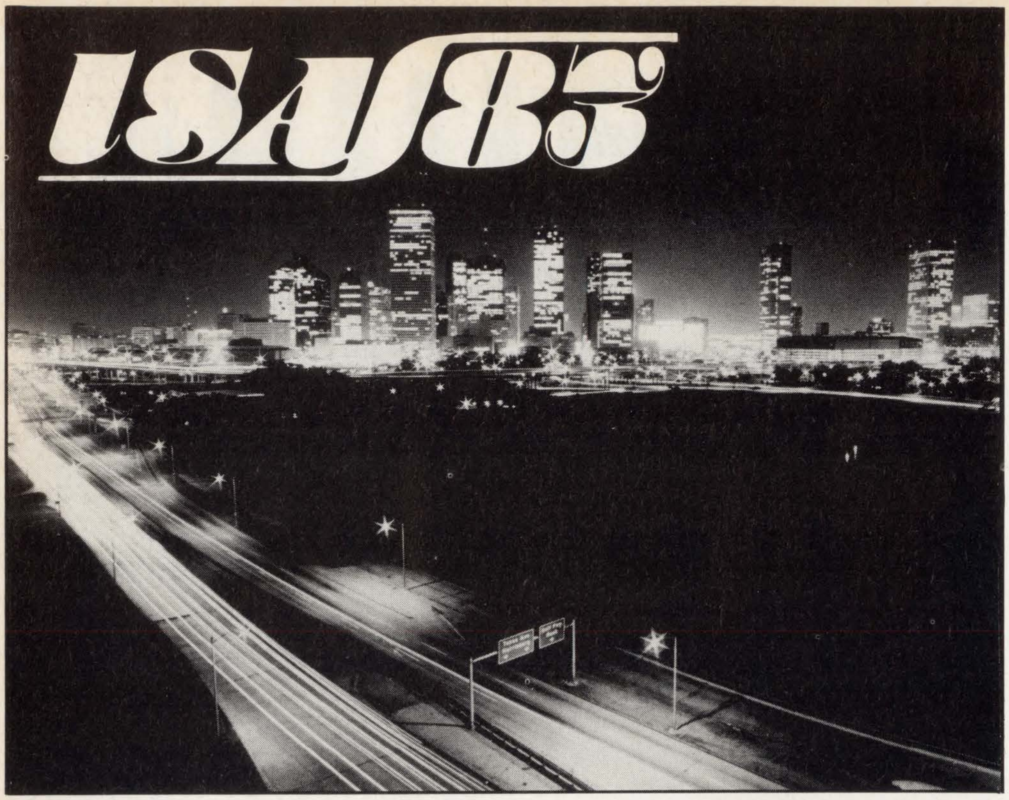

International Conference and Exhibit

Astrohall
Houston, Texas
October 10 to 13, 1983

Every industry must respond to change, and that task, perhaps, most challenges the instrumentation field. Tools for testing and measuring technology must keep apace with rapid and sometimes exponential developments. When the Instrument Society of America's International Conference and Exhibit convenes Oct 10 to 13 at the Astrohall, it will offer a product exhibition and Professional Program, covering updates on special subjects as well as reviews of the basics. Technical courses are organized into 20 topical program tracks, featuring presentations led by top professionals in the instrumentation field. A new Electro Optics group, focusing this year on fiber optics, will join previously established program tracks such as Process Measurement and Control.

The Automatic Control Systems group includes Sessions 3, 19, 31, and 44 and also features robotics clinics. Sessions 4 and 65 will project future batch factory automation and applications, while Session 58 will cover system packages for robotics control.

Another clinic, part of the Computer Technology track, deals with controllers. This is divided into two parts, one for basic programming, and the other for advanced applications. Computer Technology sessions also include Sessions 5, 6, 21, 32, 45, 59, and 67, which examine a wide range of subjects from data communication standards to human/machine interfaces.

Numbers preceding program information identify papers that are offered as ISA preprints.

For registration information, contact Charles Glazer, Instrument Society of America, 67 Alexander Dr, Research Park, NC 27709. Tel: 919/549-8411

Professional Program Excerpts*

Session 3: Simulation for Training and Process Control

Mon 10:15 am to 12:15 pm, Rm 114

Session Developer: M. Clemens, The Lummus Co

816 "A Training Program for Control Engineers Using Simulation"
M. Clemens, The Lummus Co

817 "Operator Training Simulator—User's Viewpoint"
A. Chou, Mobil Oil

(continued on page 90)

*Program sessions are subject to last-minute changes.

(continued from page 88)

Session 4: Tutorial Clinic: Future Batch Factory Automation

Mon 10:15 am to 12:15 pm, Rm 118

Session Leader: S. Bansal, Polaroid Corp

Session 5: Personal Computers for Process Control

Mon 10:15 am to 12:15 pm, Rm 300

Session Developer: C. Andreason, Fisher Controls

846 "Evaluating Personal Computers for Use in Process Control"
J. B. Grierson and D. R. James, Systems Application Engineering Inc

847 "Use Your Personal Computer to Simulate, Test, and Fine Tune Process Control Loops"
P. Y. Keskar, Merck & Co, Inc

848 "The Development of the Personal Control Computer (PCC)"
J. J. Pinto, Action Instruments Co, Inc

849 "Personal Computers Automate Instrument Maintenance Activities"
L. R. McArthur, Alyeska Pipeline Service

Session 6: Panel: Data Communications Standards

Mon 10:15 am to 12:15 pm, Rm 307

Session Leader: R. Caro, Autech, Inc

Panelists: R. S. Crowder, E. I. DuPont De Nemours; R. H. Douglas, Concord Data Systems; T. Kozlik, Honeywell, Inc; and A. Hammond, Texas Instruments Inc

Session 7: Fiber Optics Sensors

Mon 10:15 am to 12:15 pm, Rm 311

Session Developer: R. Belz, Sverdrup Tech, Inc

876 "Fiber Optic Sensors in Industrial Applications—An Update"
D. A. Krohn, EOtech Corp

877 "Fiber Optic Motion Sensors"
T. Boiarski, Battelle Columbus Labs

878 "Optical Fluid Distribution Measurement Systems"
D. E. Larsen and V. S. Scown, EG&G Idaho

879 "Industrial Optical Pyrometers Survive by Design"
J. V. Meleski, Ircon, Inc

880 "Fluoroptic TM Thermometry—A Self-Referenced Fiber Optic Thermometry Employing a Phosphor Sensor"
R. Alves, J. Christol, M. Sun, and K. Wickersheim, Luxtron

Session 19: Control Systems Reliability

Tues 8:30 to 10:30 am, Rm 307

Session Developer: J. P. Rooney, Foxboro Co

819 "Reliability Considerations of System Architecture"
J. F. Olivieri, Foxboro Co

Session 21: Programmable Controller Applications

Tues 8:30 to 10:30 am, Rm 311

Session Developer: R. E. Bergerson, Industrial Systems Design

850 "Robot, Vision, Programmable Controller, and Computer Team to Provide 1-Step Test of Finished Assemblies"
J. A. Almond, Texas Instruments Inc

851 "Coordinated Bleach Plant Operation—Advanced Regulatory and PC Functions"
M. Greaves and S. E. Kallos, Foxboro Co

852 "Automation of Pharmaceutical Operations Using Programmable Controllers"
L. K. Hill, D. J. Fraade, and F. Riggs, Burroughs Wellcome

Session 22: Electro Optics

Tues 8:30 to 10:30 am, Rm 201

Session Developer: N. Hartman, Battelle Memorial Institute

881 "Optical Data Processing and Object Recognition"
J. Upatnieks and I. Cindrich, Environmental Research Institute of Michigan

882 "Holographic Camera, a New Instrument"
M. Chang and D. Rosenthal, Newport Corp

883 "Applications of Integrated Optics in Industrial Process Control"
C. M. Verber, Battelle Columbus Labs

884 "Optical Detection of Surface Flaws"
R. Simonson and R. J. Reid, Target Systems Inc

885 "Today's Lasers in Manufacturing"
J. Johnson, Control Laser Corp

Session 31: Process Control Packages

Tues 10:45 am to 12:45 pm, Rm 307

Session Developer: R. Lankering, IBM Corp

821 "Installation of the New ACS Process Control System at Imperial Oil"
G. C. Bodie, Imperial Oil Ltd

(continued on page 92)

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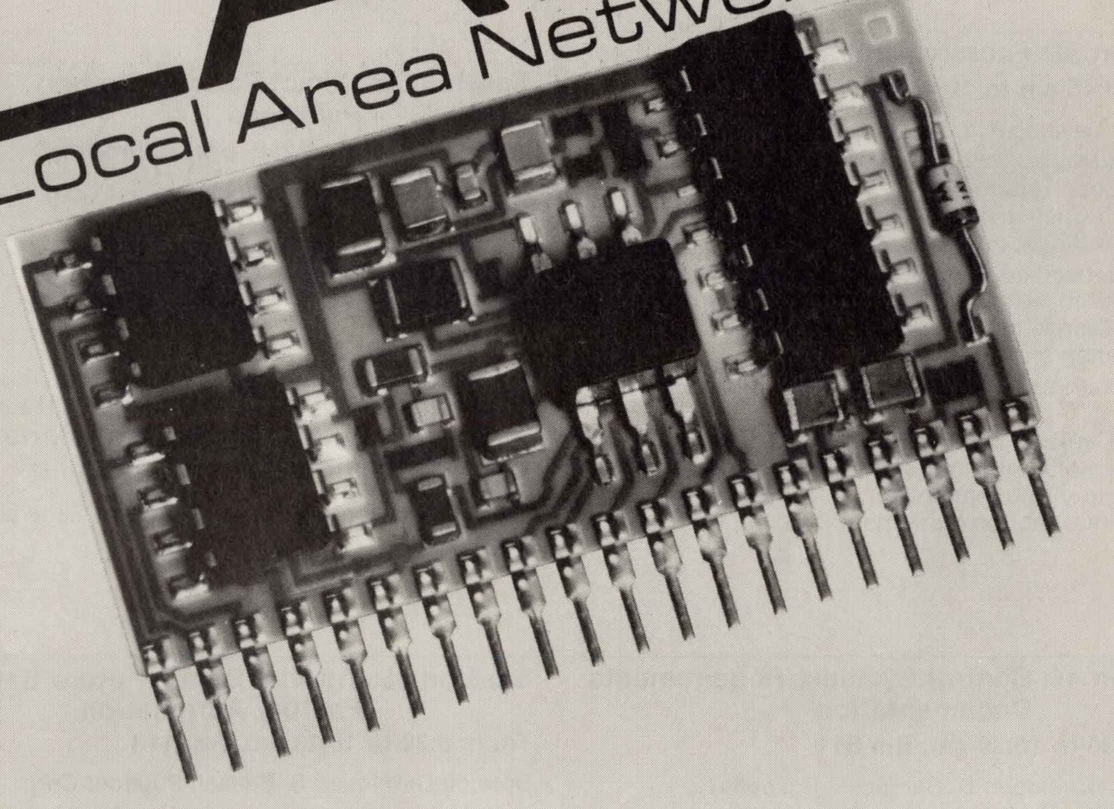

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CIRCLE 48

(continued from page 90)

822 "A Process Control Language for Distributed or Centralized Architectures"
J. I. Llansa, Setpoint, Inc

823 "An Interactive Fill in the Blanks Software System for Process Control"
H. R. Foster, Quadrex Computer Systems

824 "A Language for Specifying Sequential Control Processes"
E. Ellisor, IBM National Accounts

Session 32: Factory Automation

Tues 10:45 am to 12:45 pm, Rm 311

Session Developer: J. Rovnak, Stone & Webster

853 "A Microcomputer-based CAD/CAM System for Low Cost Automation"
J. Y. F. Chen and V. C. Venkatesh, National Univ of Singapore

854 "Networked Programmable Controller Applied to Realtime Batch Process Control"
W. F. Raines and T. D. Metzgar, Texas Instruments Inc

855 "Distributed Faultproof TM Industrial Control System"
R. H. Caro, Autech Data System

856 "Robotic Intelligence Techniques Applied to Factory Automation"
J. J. Pinto, Action Instruments Co, Inc

Session 44: Control Systems Requirements Documentation

Wed 8:30 to 10:30 am, Rm 311

Session Developer: D. Campbell, Foxboro Co

825 "On the Development of System Hardware and Software"
M. G. Rekoff, Jr, Univ of Tennessee

827 "Requirements Definition for Process Control Systems"
P. Ward, Yourdon Co; and D. Campbell, Foxboro Co

828 "Models of Complex Process Control Systems"
I. Morrow, Arthur Young, Inc; and B. Robinson, Foxboro Co

Session 45: Panel: ISA and Computer Networks

Wed 8:30 to 10:30 am, Rm 201

Session Leader: H. P. Zinschlag, Monsanto Co;

Panelists: H. P. Zinschlag, Monsanto Co; C. D. McAlister, ISA; R. E. Blue, IBM; W. C. Rutledge, Mead Corp; L. K. Christensen, Fisher Controls; R. Wang, Exxon Co; and R. Mulley, Fluor

Session 48: Distributed Control

Wed 8:30 to 10:30 am, Ballroom A

Session Developer: J. Hefler, Bechtel Power Corp

917 "System Models as Configuration Tools"
R. Bibbero and J. J. McCarthy, Honeywell PMSD

918 "Power Plant and Industrial Automation through Distributed Control"
L. K. Klein, Eaton Corp

920 "Effectively Using Distributed Control Concepts"
D. Scharringhousen, M. W. Kellogg Co

Session 58: Clinic: Robotic System Packages

Wed 10:45 am to 12:45 pm, Ballroom C

Session Developer: R. Lankering, IBM Corp
Speaker: W. Short, IBM Corp

832 "Robotic Control Language"
T. M. Larson, Unimation, Inc

Session 59: Clinic: Communications and Intelligent Human Interfacing

Wed 10:45 am to 12:45 pm, Ballroom D

Session Developer: R. A. Whitehouse, General Electric Co

Session 65: Tutorial Clinic: Future Batch Factory Automation

Thurs 8:30 to 10:30 am, Rm 118

Session Developer: S. Bansal, Polaroid Corp

Session 66: Clinic: Programmable Controllers

Thurs 8:30 to 10:30 am, Ballroom C

Session Developer: J. Benedetto, Modicon

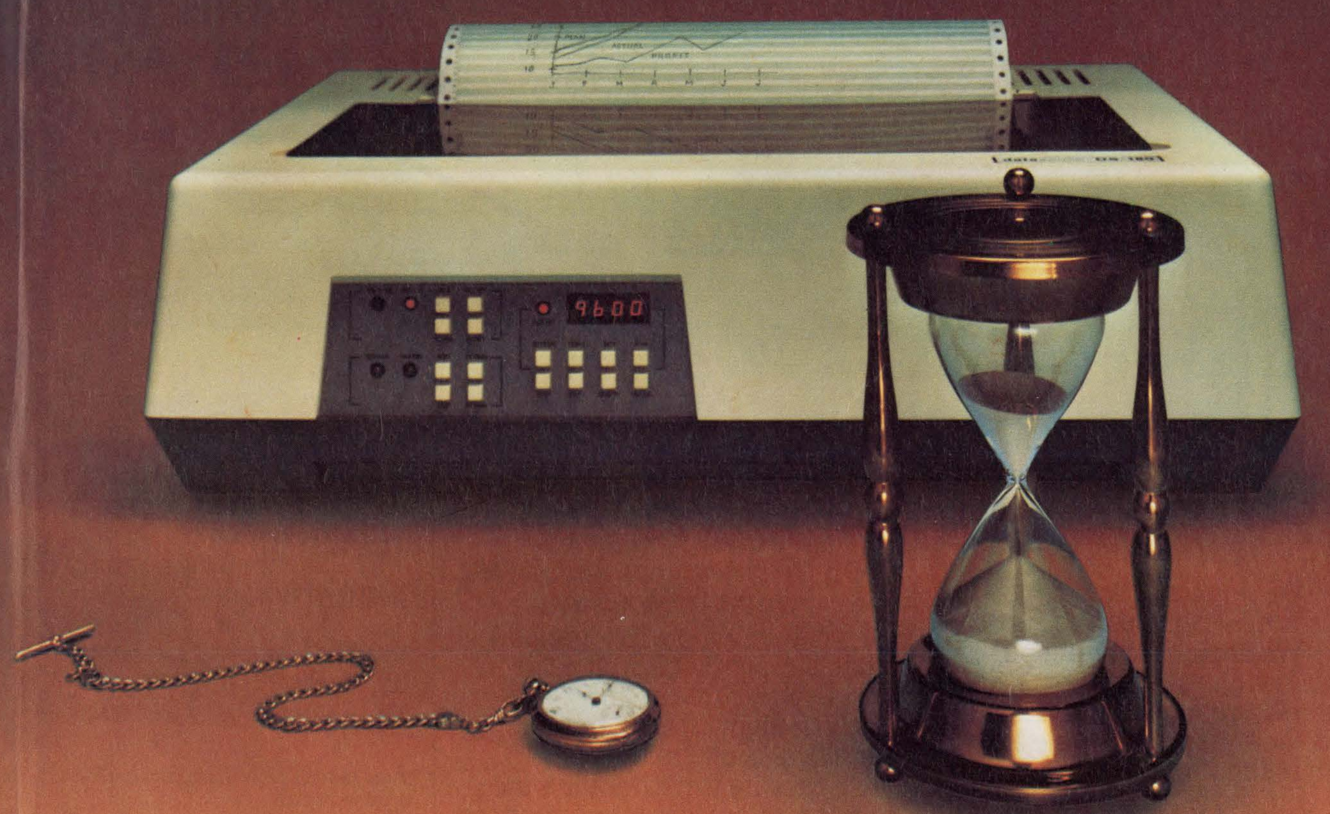
Session 67: Man/Machine Interface

Thurs 8:30 to 10:30 am, Rm 201

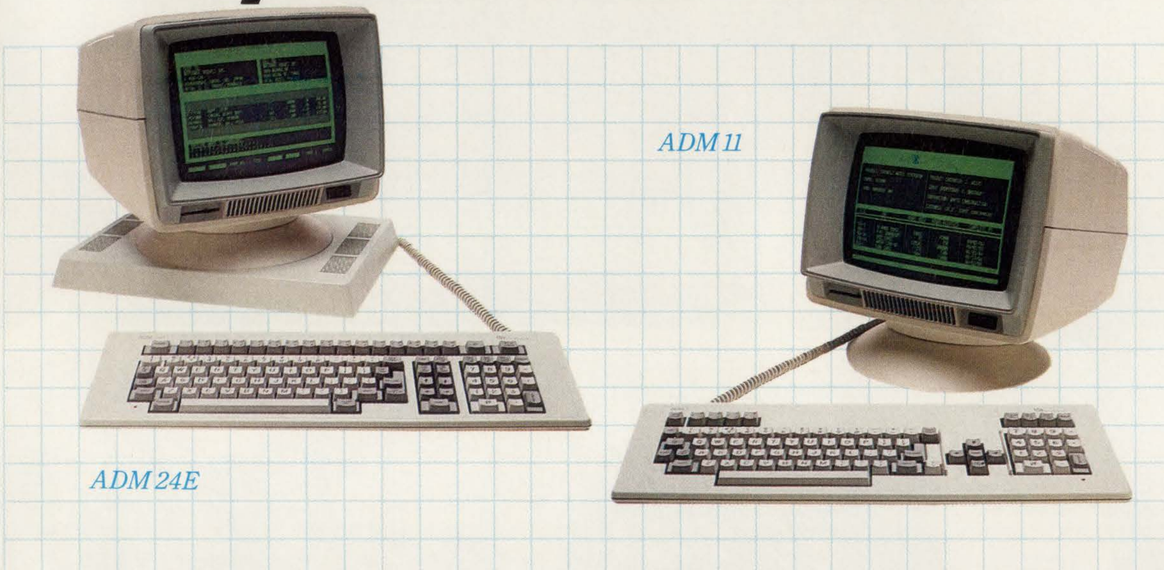
Session Developer: K. Hopkins, DECI Corp

857 "Ease of Use"
R. S. Shirley, Foxboro Co

858 "Realtime Information Access and Control through Programmable Controller-based Automation"
A. R. Miller, Process Control Industries, Inc □



Introducing the High Touch™ Terminals. Because there's more to ergonomics than simply separating keyboard from monitor.

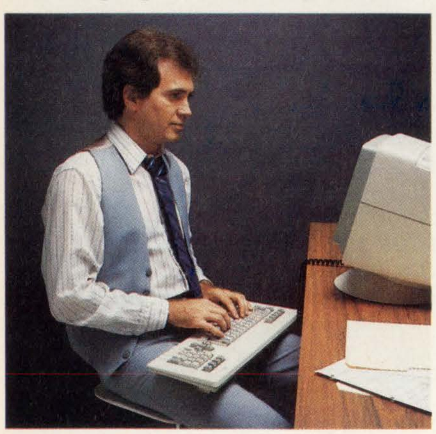


Have you ever noticed that the more high technology we put into the workplace, the more human touches the workers put in?

We noticed. Plants, pictures, macrame. Funny coffee cups.

We decided that people were trying to tell us something. There's a real need to soften the interface between people and high technology.

So we designed our new High Touch™ terminals from the desktop up to work together



6′ coiled cable lets you put the keyboard anywhere.

with biology, not just with technology.

Because if our product doesn't feel good, you DP managers and OEMs don't look good.

There's more to ergonomics than simply tacking on a few faddish features as an afterthought. We put our thinking in up front. We spent a long time studying the way humans relate to computers. And we came up with a whole new way for computers to relate to humans.

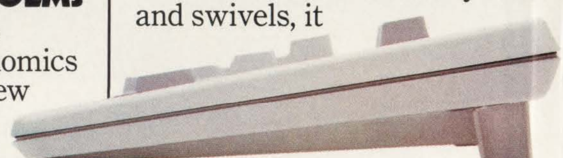
No aspect of terminal design escaped our deepest consideration. Or reconsideration.

And the result is a terminal that's downright considerate.

Because whether you're a DP manager or an OEM, the fact remains that the terminal represents your system. So High Touch terminals are made to feel as good as they look to the people who use them.

Dozens of little touches add up to the convenience and comfort of High Touch. For example, we put the power "on/off" switch and contrast control knob in front where they're easy to reach.

The monitor not only tilts and swivels, it



Low profile DIN-standard keyboard with adjustable tilt.

stops positively in almost any position. With other tilt-and-swivel terminals, the cables always seem to reposition the monitor for you the moment you have it adjusted perfectly.

The clean, crisp display features a large character matrix on an easy-to-read non-glare screen—made even easier to read by the hooded bezel.

The low profile, DIN-standard keyboard is not only tapered, its angle of tilt is easily adjusted for maximum operator comfort.

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entry almost as natural as talking.

Because the only thing that should be difficult is making an error.

On the ADM 11, for example, you'll find the separate cursor control keys logically arranged in a cross for ease of use without looking.

Monitor tilts and swivels to almost any position. Both models available with 12 or 14 inch screens.

We placed the *control* and *escape* keys close to the alphanumeric keys, where people just naturally expect to find them.

And there are no keys at all next to the space bar, so no one can accidentally hit them.

Our uncluttered keyboard, with its logical and physical separations between key groupings, improves your efficiency.

On the whole, we've taken the approach that if something isn't needed, it shouldn't be there. That's why the ADM 11 has just four function keys shiftable to eight.

And speaking of staying out of the way, our High Touch terminals' small footprint will fit as easily on a secretary's return as on an executive's credenza.

Because styling and comfort are just the first steps toward increased productivity.

No terminal has ever been so easy to live with. But don't get the idea that High Touch is the opposite of High Tech. It isn't.

The ADM 11, for example, is a High Touch conversational terminal that accepts data continuously at 19.2 kilobauds. Block mode terminals simply can't match this high throughput.

In addition there are four programmable function keys (shiftable to eight) with two levels of setup mode to reduce errors while still giving the operator maximum flexibility.

On the other hand, for a High Touch terminal that's more intelligent and has more functions and features, choose the ADM 24E. It features a moveable 24-line window you can use to look at 48 (or optionally, 96) lines of memory.

There are eight non-embedded attributes with embedded mode for existing applications, and 16 programmable non-volatile function keys (shiftable to 32) with legends on the status line (25th line). It runs in either conversational or block mode.

The ADM 24E also offers plenty of additional space for OEMs, with up to 56K ROM and 22K RAM.

When it comes to terminal technology, we're the historic leader with the largest installed base. We've been continuously implementing state-of-the-art technology in an ever-expanding line longer than any other major manufacturer.

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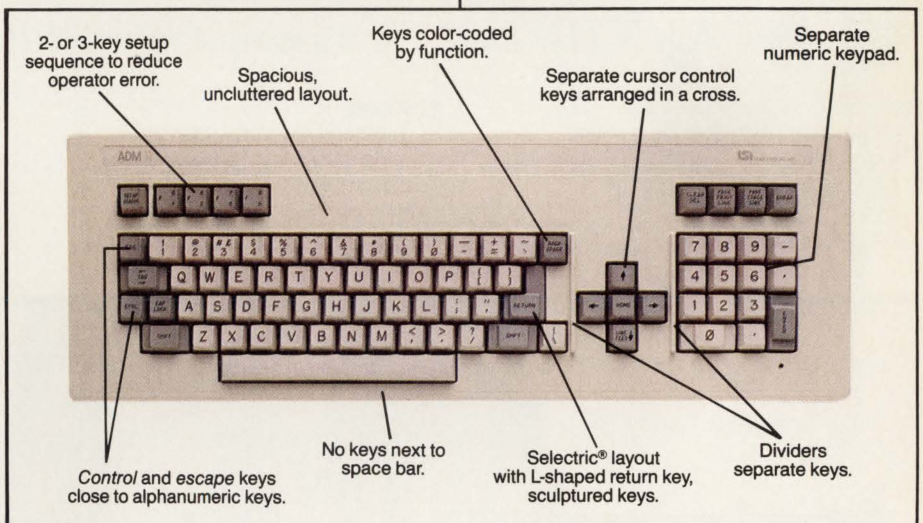
Lear Siegler High Touch terminals are made in America—designed, engineered, manufactured and shipped from Anaheim, California to provide you with the best local support. That's one reason they're called the American Dream Machines.

Our new High Touch terminals. Because it's high time.



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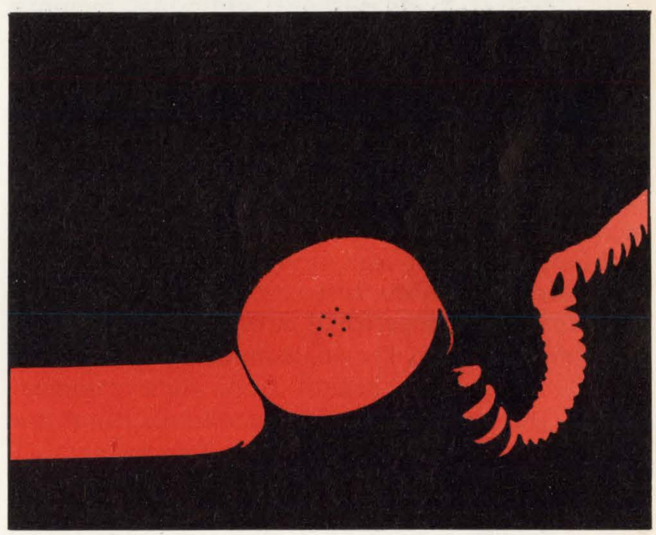
CIRCLE 50

TERMINALS, LISTEN UP, SPEECH RECOGNITION IS A REALITY

"Speaker-independent" speech recognition technology can simplify data terminal operation for many users.

by Thomas B. Schalk and
Elizabeth L. Van Meir



Terminals will soon carry a low-cost speech recognition option that will greatly enhance their functionality. Sparked by a succession of technological developments, speech recognition systems are ready for application in intelligent data terminals. In addition to breakthroughs in basic voice recognition techniques, a number of digital signal processing microcomputers are becoming available. These microcomputers cut cost and hardware complexity in terminal systems.

The goal of a low-cost speech recognizer should be to recognize every speaker's voice. So far, all of the well-known techniques have been used to design speaker-dependent systems. Now, an innovative speech recognizer, using a "feature analysis" technique that is based on analysis of a voice's phonetic features, has been developed. The key aspect of this system—speaker independence—is essential to applications in which many users share the terminal.

A timesharing computer system typifies this concept. Users of such a system log on simply by uttering their passwords into the system. (Passwords are usually a string of four digits). To activate a speaker-dependent terminal, a user would first go through a "training session" during which he enrolls his voice patterns into the system. The enrolling of voice patterns is a time-consuming process that may have to be repeated several times to be successful.

After logging on, a speaker-dependent recognition system can be more beneficial than a speaker-independent one. This is because speaker-dependent systems have larger and more flexible vocabularies.

Thomas B. Schalk is senior vice president of consulting at Voice Control Systems, Inc, 16610 Dallas Parkway, Dallas, TX 75248, where he is manager of the speech recognition consulting staff. Mr Schalk holds a BSEE from George Washington University and a PhD from Johns Hopkins School of Medicine.

Elizabeth L. Van Meir is marketing manager in charge of marketing and public relations at Voice Control Systems. She has studied journalism at the University of Maryland.

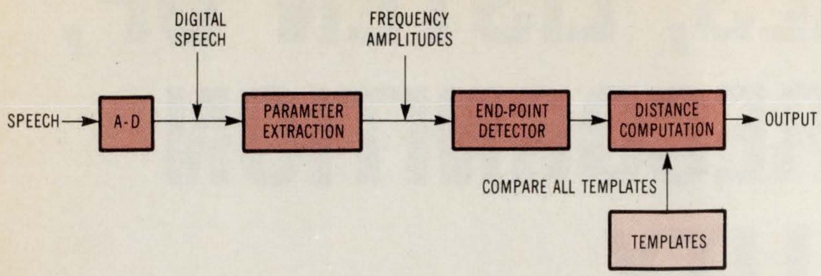


Fig 1 Template-matching speaker-dependent word recognizers are best suited for single-user data terminals. Users must "train" the system to recognize their voices by making templates of their voice patterns. Such templates are used by the system to make comparisons with spoken voice patterns.

For example, a typical speaker-independent system is limited to recognizing the digits zero through nine, and simple control words such as yes, no, stop, begin, and erase.

A number of terminal manufacturers now offer speaker-dependent voice-input features made possible by the development of dedicated digital signal processing (DSP) microcomputer chips. Among the most popular DSP devices are the Texas Instruments' TMS 320, Nippon Electric's NEC-7720 and Intel's 2920. Second-generation versions of these devices should provide additional memory and greater versatility, spurring more advanced speech recognition applications.

Board-level speech recognition products are also making their presence felt in terminals. Interstate Electronics makes a recognition board that fits inside standard cathode ray tube (CRT) terminals such as the DEC VT-100, and Keytronics has keyboards with self-contained, standalone recognition hardware. Texas Instruments offers optional voice input on its personal computer. Even home computers, such as the voice-input option offered by Milton Bradley, benefit from voice enhancements. Other speech recognition manufacturers are gearing up to provide systems for data terminals.[1]

Although rapid strides are being taken to incorporate recognition systems into data terminals, designers must remember that voice-input technology is still evolving and has limitations. And compared to input devices such as keyboards, speech technology is still very expensive. However, current improvements, coupled with new programmable integrated circuits may open the way for integrating speech recognition technology with data terminals.

The status of recognition technology

Voice recognition is called an interface technology in which human voice patterns are analyzed by a machine to determine the words spoken. Recognized commands are sent to a computer system that converts them into physical functions. For example, voice input can be used to move and control a cursor in a terminal's CRT. In this sense, voice recognition is a value-added feature of a keyboard, much like a 10-key numeric pad.

Although some observers believe that voice recognition could replace the keyboard, current technology is not yet sufficiently developed to achieve that end. Advances in capabilities and performance must occur in three major areas: connected speech versus single-word recognition; vocabulary size; and speaker independence.

Most current voice recognizers operate only on discrete or isolated speech. Isolated word recognizers impose speaking rate restrictions on users. That means users must pause between words so that each word's end points can be determined. Even the few commercially available connected-word recognizers perform better on isolated speech than on connected speech.[2] The reason is that the acoustic variation is greater for connected speech than for discretely spoken words.

Speaker-independent systems represent a practical alternative for speech recognition in data terminals.

On the issue of vocabulary size, users tend to be more impressed with the number of words the system can recognize than in their own application needs. No current system comes close to having recognition capabilities comparable to those of a person. But a vocabulary as simple as "yes" and "no" can have practical applications. For example, a pay-by-phone service could use a series of yes-no questions to allow customers to pay bills.

Even expensive recognizers have difficulty with vocabularies of over 200 words. For this reason, designers should minimize the number of words in the vocabulary for a specific application; the selection of words is more important than the absolute number. Thus, the vocabulary application requirements are more critical than recognizer restrictions.

Almost all available recognition systems are speaker dependent. Such systems impose training requirements on users who must enroll their unique voice patterns into the system. Typically, users utter each word in the vocabulary five times. The voice patterns, called templates, are stored in a random access memory (RAM) as reference patterns, and are accessed for comparison purposes whenever users access the system. Because of the comparison scheme, users may have to re-enroll certain words into the system to achieve the proper recognition performance. Most speaker-dependent, isolated-word recognizers are based on the template-matching technique.

The block diagram of Fig 1 illustrates the data flow in a typical template-matching system. A microphone converts acoustic waves into electrical signals that are then digitized. Parameters—usually frequency amplitudes—are extracted from the digital representations, typically every 20 ms. When a word's end points are determined, the input parameters are formatted and compared to each template. If a proper match occurs, the word is hypothesized or selected. After a specific word has been recognized, "machine acceptable" data such as binary codes, signals, or impulses can be sent to a host computer.

Template-matching systems are beset by inherent weaknesses. If the size of the vocabulary doubles, the template memory size also doubles. This increases system response time since twice as many template data must be compared to the input data word. In addition, the template comparison does not begin until the end of the spoken word. This so-called energy-based end-point detection scheme also slows system response time. Another criticism of template-matching systems is that they do not mimic the human auditory process. They are sometimes called signal matchers as opposed to speech recognizers. Nevertheless, such systems represent the majority of existing recognizers.

Fig 2 shows the flow diagram of Voice Control System's speaker-independent recognizer. As a feature-analysis system, it overcomes many of the problems of speaker-dependent recognizers. No training or speaker enrollment is necessary. The feature-analysis technique requires examining

The most important voice-input applications are those where speech offers a clear advantage over manual input.

word features only to the extent of recognizing a word's unique components. Characteristics such as coloration, pitch, accent, and inflection are disregarded. When the beginning of a spoken word is detected, feature identification begins.

A word can be selected when a sequence of features is identified along with the end of the word. Some investigators believe that this concept applies to human speech perception. Speaker-independent feature-analysis systems use no templates. Instead, reference data are stored in a read only memory (ROM) to help identify such features as a leading "s." Since the English language has a limited number of distinct features, the memory size required to accommodate vocabularies is small, even for very large vocabularies. Moreover, processing time and response speed are quite insensitive to vocabulary size. Speaker-independent systems are beginning to manifest themselves as solutions to the speech recognition problem. With their potential for optimizing a manufacturer's price/performance needs, they represent a practical alternative for speech recognition in data terminals.[3]

Designing-in recognition hardware

In modern computer systems, speech recognition hardware is usually found in one of four locations: within the CRT, within the host mainframe, within the keyboard, or as standalone peripheral units. Most speech recognizers fall into the last category—they are standalone peripherals having RS-232 compatibility.

There is also a growing trend toward single-board units designed to fit within a terminal system. Fig 3 shows such a board for an Apple computer. These types of recognizers typically cost between $1000 and $3000 and are speaker dependent.

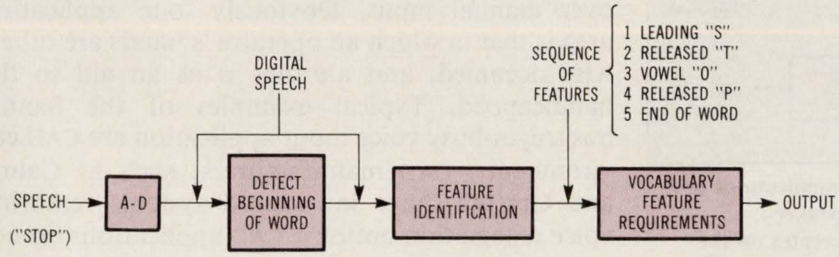


Fig 2 Speaker-independent word recognizers are phonetically based, that use no templates, and require no user training. Operating on the principle of feature identification, speaker-independent systems need less memory than speaker-dependent types, making them more cost-effective for data terminals.

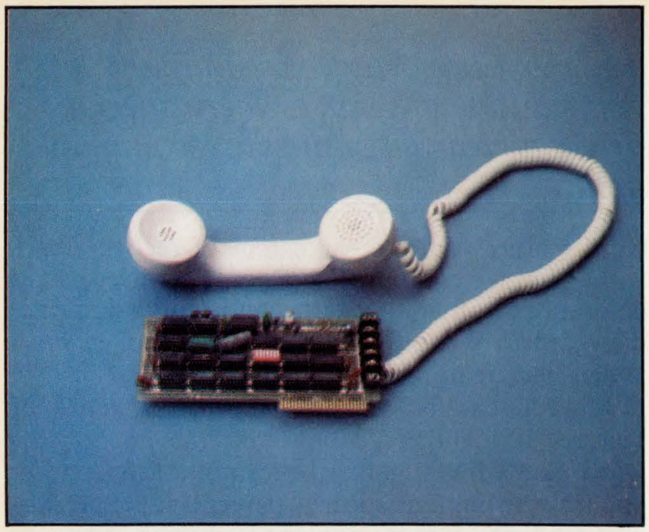


Fig 3 Speech recognition hardware is decreasing in size as illustrated by this single-board system for an Apple computer. Although this prototype is not standalone, RS-232 compatible peripherals are well suited to data terminal applications.

The amount of RAM required for template storage varies significantly among systems; on a per-word basis, storage differences can be anywhere from 10 to 1000 bytes/word. Storage size varies due to basic differences in recognition algorithms, and more importantly, due to the type of distance measure used to compare templates with the input data.[4]

Optional speech recognition circuitry usually dictates simple hardware interfaces such as bit-serial transistor-transistor logic (TTL) or RS-232 to minimize the number of connector pins and cables between the speech recognizer and terminal. This technique is used in Voice Control System's recognizer as shown in the Fig 4 hardware block diagram. With the proper protocol, it is possible to place the speech recognizer in the serial path between the terminal and central processing unit (CPU). In this case, the recognizer acts as an intelligent bidirectional buffer and need not be in the same housing as the CRT or keyboard.

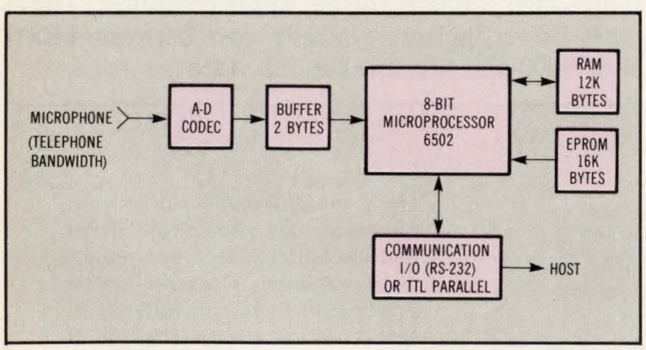


Fig 4 An 8-bit microprocessor and a communications port form the core of Voice Control Systems' speaker-independent word recognizer. Because it operates on the principle of feature identification, this recognizer uses far less memory than speaker-dependent word-recognizer systems.

The arrival of high speed, cost-effective complementary metal oxide semiconductor (CMOS) microprocessors and peripheral circuits make it possible to design speech processors having low power dissipation. This simplifies heat removal and power supply design since the speech system can be sealed and powered from the CRT or host computer. The growing use of CMOS gate arrays permits smaller speech system packaging configurations.

Because speech recognition technology is in a dynamic state, it is very important that any speech recognizer system be software based. This gives a designer the necessary flexibility to incorporate algorithm enhancements. On the other hand, hardware-based systems will probably become obsolete in about three years.

Microphone selection is an important consideration when integrating voice input with terminals. The microphone should be chosen with two factors in mind: the background noise of the environment, and the system application. In general, microphones with low signal to noise (S/N) ratios increase the probability of speech recognition errors. For high performance, S/N should be greater than 25 dB. A popular microphone with good noise-cancelling ability is the Shure SM-10. A headband microphone, the SM-10 is most suitable for "hands-busy/eyes-busy" environments such as computer aided design (CAD) applications. However, this type of microphone is inappropriate for executive workstations. An excellent choice for the executive is the common telephone handset. Many of the new executive terminals already incorporate such handsets, so users are familiar and comfortable with this type of input device.

For quiet environments, the lapel microphone, which clips onto clothing, is a good choice. Even better is a directional microphone mounted inside a CRT terminal. From a human factors viewpoint, this may be the ideal choice. Users easily accept the familiar handheld microphone, but it is unsuitable for applications requiring hands-free terminal operation.

Voice-input in the terminal

Today's most important voice-input applications are those in which speech offers a clear advantage over manual input. Obviously, one application area is that in which an operator's hands are otherwise occupied, and another is as an aid to the handicapped. Typical examples of the hands-busy/eyes-busy voice input application are CAD environments. CAD manufacturers, such as Calma and Graftek, have introduced systems featuring voice recognition options. CAD applications do not necessarily require large vocabularies—Calma estimates that 50 words could handle 80% of the typical workload of its terminals. In many cases,

Fig 5 This portable speaker-independent word recognizer designed by Voice Control Systems is a demonstration unit for showing speech recognition capabilities. A liquid crystal display depicts the spoken word, and the telephone handset serves as the microphone.

voice recognition enhances productivity in CAD environments. Intel reports gains from 40% to 200% in their voice-input CAD environment. IBM's personal computer uses CAD software called the DASH-1. This software uses 18 commands to call picture templates from a parts library and position them on a CRT screen. Limited vocabulary applications of this type are another productive use of voice-input technology.

Speech recognition hardware can also help improve productivity in industrial control. For example, in quality control, a person can inspect a part and report its defects verbally into a computer. Inspectors do not have to put the part down to log its defects, nor do they require any kind of typing skills.

Besides its contribution to office and factory productivity, speech recognition offers "perceived benefits." These are associated with the state-of-the-art image conveyed by speech recognition technology. Executive CRT terminals, for example, serve primarily for data review and retrieval—voice messages, documents from data bases, electronic mail, and electronic calendars. Speech recognition technology in the terminal enhances such applications and interfaces well with these features. Fig 5 illustrates an "image" word recognizer built by Voice Control Systems to demonstrate the benefits of speech recognition.

Home and personal computers also fall into the perceived-benefits category. Possible uses range from household accounting to voice-controlled joysticks. Texas Instruments has recently developed a "transparent keyboard" concept for its personal computer. This allows a programmer to convert conventional software into voice-input software. The use of voice commands actually simulates keystrokes.

Good speech recognition performance and small vocabularies go hand in hand, especially for speaker-independent recognizers. Large vocabularies are best handled by incorporating syntax into the application software. That is, certain words can be activated based on the last word recognized. This concept works well for speaker-dependent, isolated word recognizers and is ideal for the menu-based systems often used in terminals.

A few of the common menu-based applications include text editors, voice store and forward, videotext, and data query systems. If speaker-independence is required, a small (10-word) vocabulary can remain active at all times, while the functions (meanings) of individual words can change based on the menu or question. Given a maximum of 10 choices in a menu-based system, numbers one through ten can be used as words with which to make menu selections. This concept is equally applicable to speaker-dependent recognizers. Another technique for menu-based systems involves cursor movement to identify menu selections. A small, fixed-word vocabulary can easily accomplish this, making speaker independence appealing.

Speaker independence and the telephone have a number of common applications. Technically, a telephone is a terminal since data can be input by voice and responses can be provided to users via synthetic speech. Future uses are numerous, including pay-by-phone, videotext, home banking, and voice store and forward. In fact, it is reasonable to expect special-function keys on keyboards to be voice activated through speaker-independent technology. Future applications will exhibit tremendous improvements in voice technology, and possibly within a decade, the telephone will become the universal terminal.

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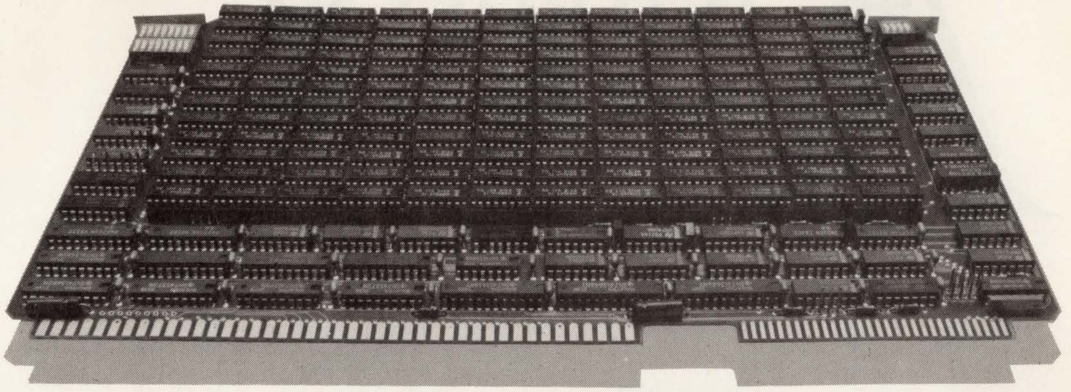

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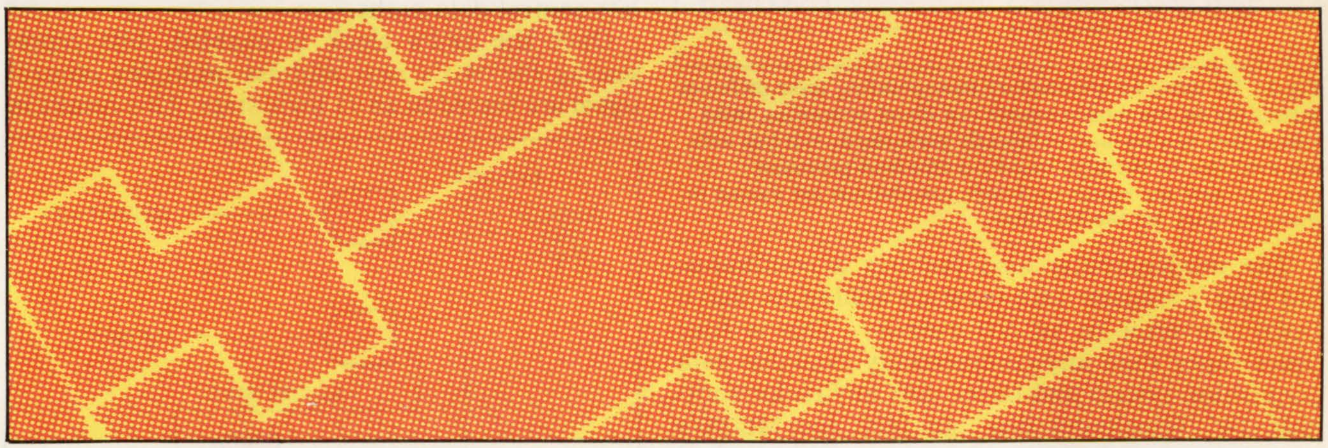

by Aaron Boxer

In a minicomputer system designed to help scientists and other technical users monitor and control realtime processes, data acquisition performance must be reliable. Usually, process data are gathered from any number of specialized user input/output devices, including sensors, stripchart recorders, and other instruments that monitor each event in progress. In addition, data must be gathered quickly so that the system can compute and display information as well as make realtime decisions.

Masscomp's MC-500 is a 32-bit Unix-based minicomputer system built for demanding realtime scientific and technical applications. The system architecture distributes the processing load among three dedicated subsystems that perform high speed computation, graphics display, and data acquisition (Fig 1). These subsystems are linked by three high speed buses: a proprietary bus links the main central processing unit (CPU) with physical memory storage; Intel's Multibus connects system peripherals to the graphics display processors; and twin STD buses channel data between the system and user input/output (I/O) devices.

The key subsystem enabling the MC-500 to swiftly collect and process critical realtime data is a data acquisition and control processor (DA/CP). This frontend, user-programmable, data acquisition controller can input or output analog or digital data at rates up to 2M bytes/s. Featuring 8 million instructions per second (MIPS), the DA/CP's 2901 bit-slice processor can manipulate two parallel STD buses that are connected to external user I/O devices. This lets the processor gather data, perform some preprocessing, and pass information along the Multibus to the system's main memory and graphics displays for further computation. When coupled with an analog input interface, the DA/CP enables the minicomputer to acquire analog data at a 1M, 12-bit sample/s rate.

Aaron Boxer is senior systems engineer at Masscomp Inc, 543 Great Rd, Littleton, MA 01460. He is responsible for data acquisition and control processor design. Mr Boxer holds a BS and an ME in biomedical electronics from Rensselaer Polytechnic Institute.

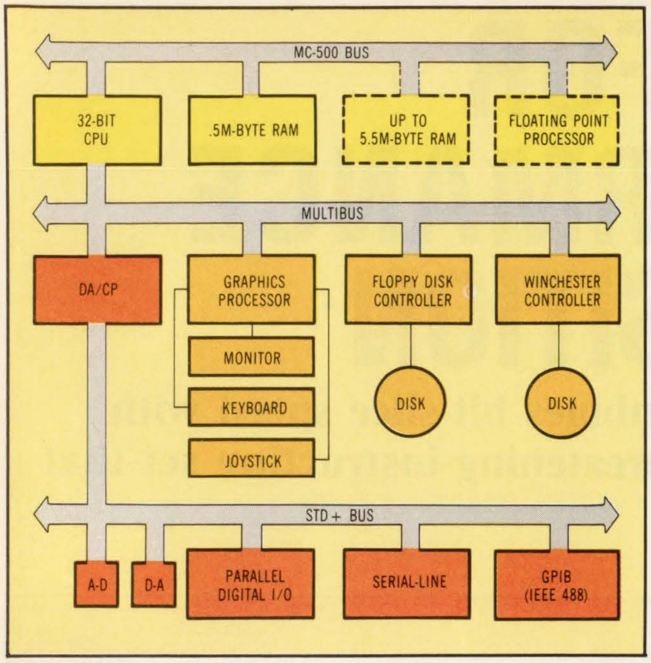

Fig 1 By using an architecture incorporating three different buses, the MC-500 minicomputer can direct processing tasks where they can be most efficiently performed. STD bus data are available to the high speed I/O frontend processor (DA/CP), and the results of 8-MIPS calculations are passed to main memory via the Multibus.

The minicomputer also features a continuous 2M-byte/s transfer rate from an analog to digital (A-D) converter to MC-500 memory. This is four times faster than any commercially available data acquisition system and faster than any rackmountable 14″ Winchester disk. In fact, the MC-500's stored data acquisition performance will be limited by disk speeds for at least two more years.

Because the DA/CP is specifically a data acquisition controller, its software provides data types and functions that prove useful for transferring and monitoring data from peripherals such as A-Ds and digital to analogs (D-As). To make user programming as easy as possible, the instruction set is designed to look like that of a micro or minicomputer. An assembler with opcodes and syntax familiar to assembly language programmers, and a powerful debugger, are all part of the DA/CP programming package.

Clock control reduces decoding hardware

The DA/CP uses 2901 bit-slice chips for its data path, and 2911 chips for its program sequencer. Usually, bit-slice based processors have wide instructions to simultaneously control the sequencer and the data path. Instructions ranging from 64 to over 100 bits are common. However, the DA/CP has a narrow instruction width of only 40 bits, and includes instructions for controlling the data path and the sequencer. This approach results in a compact instruction set. MOVE class instructions control the data path and cause the sequencer to increment the program counter. BRANCH class instructions control the sequencer in program jumps based on previous MOVE instructions.

While the narrow instruction width saves program-store random access memory (RAM) space, this savings could easily be lost in decoding MOVE and BRANCH instructions from the same bits. An unusual clocking scheme simplifies decoding and saves hardware. This clocking scheme also reduces the gate delays in decoding instructions and achieves 125-ns execution times for all DA/CP instructions.

The DA/CP's clock control circuitry is shown in Fig 2(a), while Fig 2(b) illustrates the specifics of clock timing. The arithmetic logic unit (ALU) clock enable signal is represented by 1 bit of the MOVE/BR instruction. When set, this bit enables the 2901's internal clock. The rest of the MOVE/BR instruction bits control data paths.

Once the 2901's clock is enabled, bits representing the 2911's next address multiplex control signal are forced to an 11 logic state. This results in

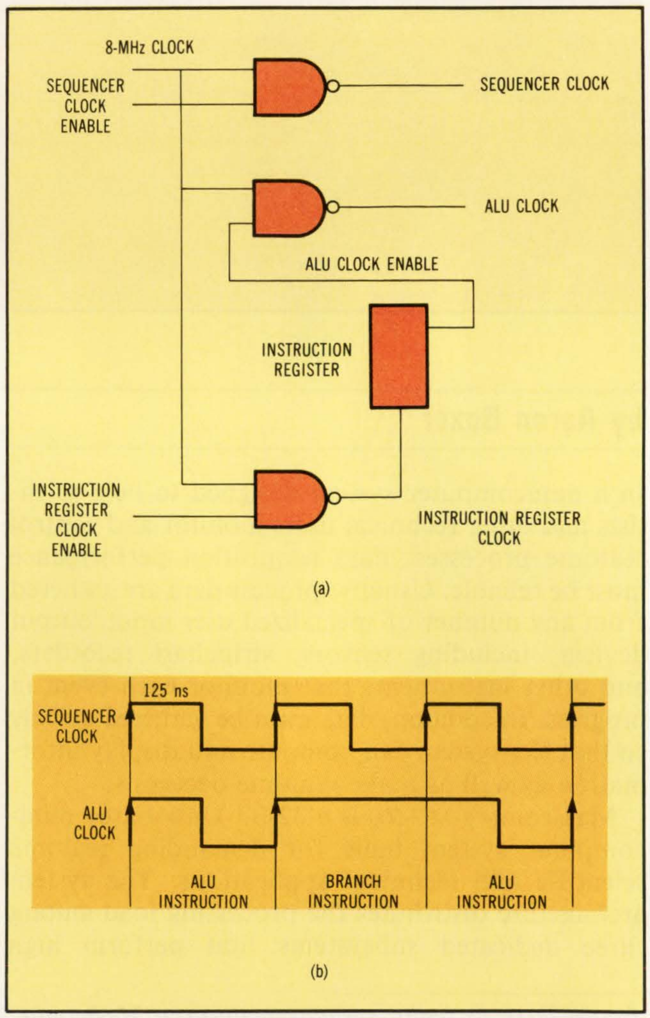

Fig 2 Clock-control circuitry of the bit-slice I/O processor (a) speeds instruction decoding and boosts performance. Clock waveforms (b) reveal the difference between MOVE and BRANCH instructions.

the selection of an internal program counter value as the next address. Other MOVE/BR instruction bits that could possibly affect program flow are now ignored. This instruction regime is known as a MOVE class instruction.

If the ALU clock enable bit is zero, the instruction is a BRANCH class instruction. Here, the test condition programmable logic arrays (PLAs) determine the 2911's multiplexer controls, with the ALU clock to the 2901s disabled. Though instruction bits still affect the data path's combinational logic, the disabled clock inhibits writes to 2901 registers or the data store. Thus, the data path is effectively blocked during a BRANCH class instruction. Control fields for the sequencer and the data path can be overlaid in the same instruction bits without a lot of decode logic or associated gate delays.

The data path of the DA/CP MOVE class instructions is 24 bits wide. Each data-store location is divided into 3 bytes: high byte, mid byte, and low byte (Fig 3). The MOVE class instructions allow operations on three data types. Byte data occupy the low byte of a data-store location. Words are in the mid and low bytes, and gulps (24 bits) use all 3 bytes of a data-store location. The DA/CP also has test conditions in the BRANCH class instructions for each of these data types.

All MOVE class instructions allow merge operations on the input bus to the ALU. The 2-byte wide input registers can put data on low byte, mid byte, or both, while a data-store location provides the other input bus bytes. The merge operation is useful for assembling bytes from an STD bus module into words in the data store before sending them to system memory. For example, all 12-bit A-Ds on the STD bus (except Masscomp's) transfer data 1 byte at a time. An STD bus read operation can put 1 byte in the data store, and the next read can merge that byte with the rest of the data from the STD bus input register on the input bus.

All MOVE instructions can write selected bytes of a data-store location while writing the output registers on the output bus. This feature improves the performance of some common DA/CP operations. For example, a Multibus direct memory access (DMA) address kept in the data store can be updated and returned to the data store in the same instruction that writes it to an output register for use in a DMA. The DA/CP also has shift and rotate operations on byte, word, and gulp data types.

Although all MOVE class instructions produce a 24-bit result in the ALU, test conditions in the BRANCH instructions exist for the byte data, word data, and the full 24-bit gulp. Arithmetic tests fall into two groups: unsigned integer tests, and tests on 2's-complement signed data. Full 24-bit arithmetic is only done on Multibus addresses for DMA. Since these are not signed numbers, the tests provided are for unsigned integers. Word data can be unsigned integers, like those from a 16-bit digital I/O device, or 2's-complement data from a bipolar A-D converter. Therefore, a full set of signed and unsigned data tests are provided for word data. All the unsigned integer tests and several of the signed data tests are provided for byte data. BRANCH-IF-TRUE and BRANCH-IF-FALSE instructions exist for all the tests. There are 32 arithmetic test conditions in all.

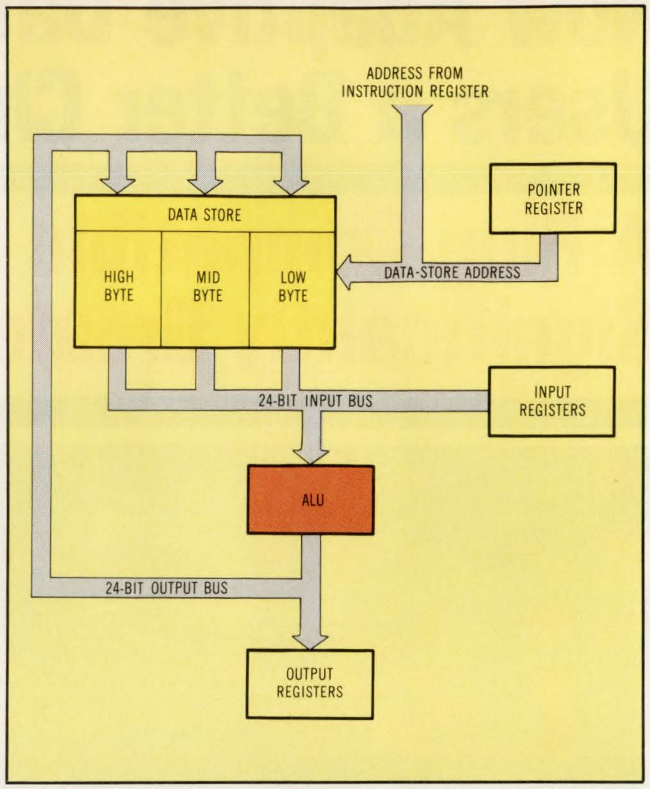

Fig 3 A MOVE instruction uses 3 bytes (24 bits) of data. Low, mid, and high bytes can be combined and written to the data store or output registers simultaneously. Individual STD bus data bytes can be combined into words for further processing.

Direct, indirect, and interrupt addressing

The DA/CP has a 1K-instruction program store and a separate, 256-location data store. Direct addressing allows a BRANCH class instruction to jump to any location in the program store and a MOVE instruction to access any location in the data store.

Moreover, the DA/CP has an indirect addressing mode that uses the contents of a data-store location as a BRANCH address. Changing the contents of this data-store location alters the program flow. This feature is useful for eliminating code from a program loop after it is no longer needed. For example, a routine can include code to test input data for a threshold crossing. Once the threshold is detected, changing the value in the data-store location that was used to jump to that location eliminates the threshold-detect code from the routine. This yields faster code than using a

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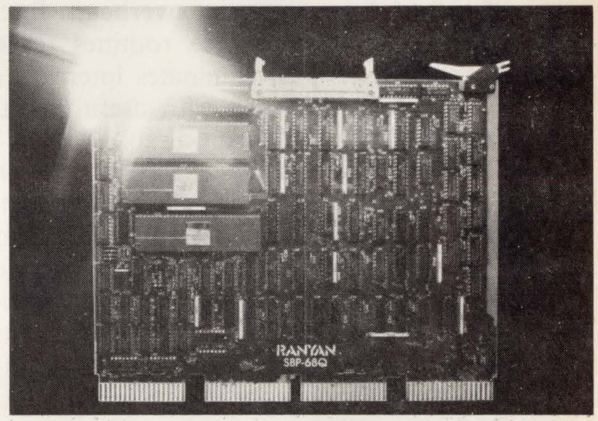

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SEE US AT DEXPO WEST '83, LAS VEGAS, OCTOBER 23-26. CIRCLE 56 threshold-detect flag bit that is tested every pass through the routine to determine if the threshold-detect code should be invoked.

In addition, DA/CP features indirect data addressing in the data store. A pointer register on the output bus can be loaded with a value and its contents can be used as the data store's address source in subsequent MOVE instructions. This feature is useful for implementing ring buffers in the data store. A block of data-store space is allocated for the buffer, and a load address and an unload address are also kept in the data store. When data are put into the ring buffer, the load pointer is moved into the pointer register and used to address the data store for the load. The address is incremented and saved for the next load. The same process is done for unloading the ring buffer. For high speed data output devices, it is necessary to compensate for normal Multibus latency by prefetching some data into a ring buffer.

Another beneficial aspect of DA/CP performance is its freedom from interrupt overhead. Interrupts that invoke interrupt service routines drive data acquisition. The DA/CP eliminates interrupt service overhead by overlapping it with useful instructions and maintaining an interrupt-disable default condition. The interrupts are only enabled for one instruction at a time, usually during the last instruction of an interrupt service routine. Hardware translates the STD bus interrupt lines directly into program-store addresses. After interrupts are enabled, the next instruction comes from the hardwired program-store address of the highest priority STD bus interrupt (Fig 4). The idle loop is the lowest priority interrupt and is always active.

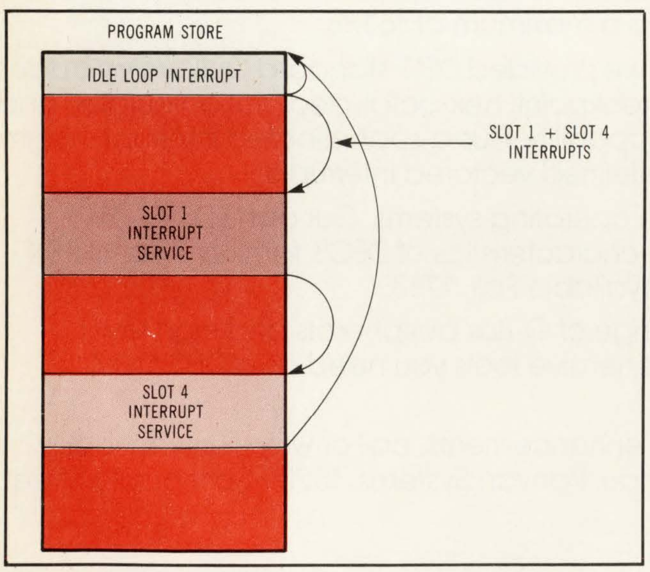


Fig 4 Interrupt overhead is kept minimal by using low priority idle loop default. When higher priority interrupts occur (slot 1) they are serviced immediately. The last service routine instruction enables all interrupts and initiates processing of the next interrupt (slot 4).

When no other interrupt is active, the DA/CP sits in this one instruction loop with interrupts enabled. But, when an interrupt from an STD bus slot occurs, the DA/CP immediately jumps to its service routine, which performs the required service and clears the interrupt in the process. In the very last instruction it enables interrupts and, if none are active, the DA/CP returns to the idle loop. As shown in Fig 4, interrupts from slot 1 and slot 4 occur simultaneously. Since slot 1 has a higher priority, it is serviced first. On its last instruction, interrupts are enabled and slot 4 is then serviced immediately. The DA/CP returns to the idle loop only after both STD bus interrupts are serviced.

An architecture that provides a dual-ported data store enhances multitasking performance.

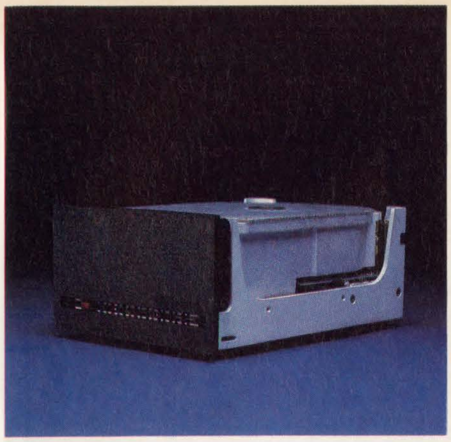
This style of interrupt service has two major implications for realtime applications. First, there is no overhead penalty for multitasking data acquisition. The DA/CP wastes no instructions determining which device is interrupted and can handle interrupts from several devices. This is not the case for some realtime controllers. Because these controllers must examine interrupt flags to see which device is interrupting, they have bigger polling loops for applications with more interrupts.

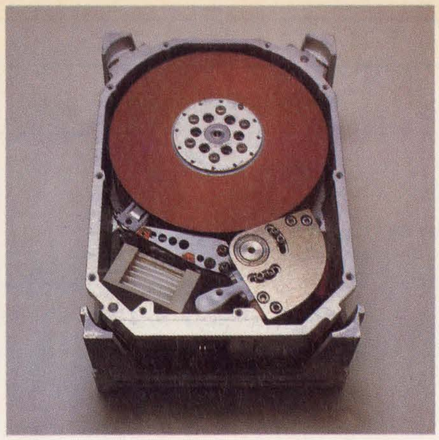
Second, leaving interrupts disabled until a service routine specifically enables them makes performance calculations as easy as counting instructions. Each DA/CP instruction takes 125 ns, so a 16-instruction interrupt service routine can be invoked every 2 μs (a 500-kHz interrupt rate). If two data acquisition tasks are running simultaneously and each has a 16-instruction service routine, then their interrupt rates may total 500 kHz. This assumes that each can tolerate a 2-μs latency while the other is serviced.

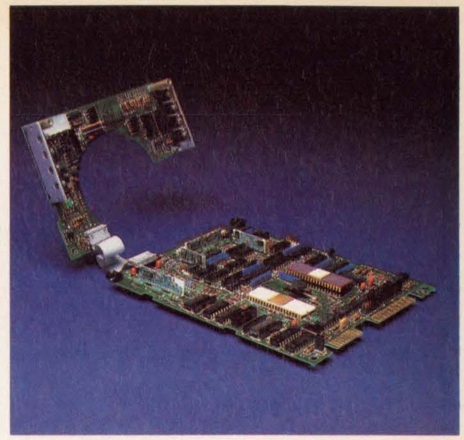
Software precedes hardware

The sample of code shown in the Table was written before the DA/CP hardware was designed and is an interrupt service routine. Several of the DA/CP features resulted from writing this code to achieve the 2M-byte/s transfer rate to memory.

For example, indirect branch addressing is used in the second instruction. As the code segment shows, the code is entered when an interrupt signals that data are ready. Only half the code is executed for each interrupt. The indirect branch determines which half. The last operation of each half of the code is used to change the address in "ffad vector" so that the other half of the code services the next interrupt. The first half, called "fst data," gets the data from the A-D on the STD bus and updates the address of a host memory buffer,







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CIRCLE 57

Interrupt Code Segment

```
        ; interrupt servi ce

        MOV #dat rd, SA                    ; start word read
        JMP ffad vector                    ; 1 jump to data service


fst data:
        ADD3 adreg, lit 4, adreg, FA       ; 2 update address, down fifo & save
        MOV datal, FO                      ; 3 first data word down fifo
        MOV data2, FO                      ; 4 second data word down fifo
        BFOOV fo err                       ; 5 check for fifo error
        MOV SD, datal LM                   ; 6 get the data
INT     MOV jmp2rg, ffad vector, SD        ; 7 set for snd data service & qui t
```

sending it and two previously collected samples down the DMA first in, first outs (FIFOs) to host memory. The second half, called "snd data" (not shown), also gets data from the A-D and updates the buffer count, checking if the end of the buffer has been reached.

Each line of code corresponds to one DA/CP instruction and is similar to minicomputer or microprocessor assembly language. In addition, the DA/CP assembler has many of the features common to minicomputer and microprocessor assemblers. The "#" before a name defines it as a constant. The assembler can evaluate an expression and equate it to this constant. If a number follows "#," a constant of that value will be created. Addresses in BRANCH instructions are labels that the assembler resolves into absolute addresses. The assembler also recognizes if the name in a BRANCH instruction is a data store. If so, it creates an indirect branch.

A debugger is also included in the DA/CP programming package. It can examine and deposit locations in the data store and the program store. It can single step through DA/CP code or force instruction execution to any location in the program store.

Any number of breakpoints may be set in the code to halt the DA/CP. The breakpointed instruction address and the next instruction address to execute are displayed. An action list the user writes can be linked to each breakpoint. When the breakpoint is reached, the action list (which can include any debugger command) is executed.

An architecture that provides a dual-ported data store enhances multitasking performance. This gives users access to the data store from the Multibus at all times. The CPU can read and write data while the controller is running. The controller is not slowed down as the CPU is reading or writing. The dual porting of the data store facilitates double buffering of data during acquisition from the DA/CP to host memory. While the controller is filling a data buffer in memory, the host CPU can fetch and load the next buffer address into an appropriate data-store location. When the current buffer is filled, the DA/CP can fetch the next buffer address from the data store and start filling that buffer.

The MC-500 with a DA/CP is a computer system that acts as a high performance data acquisition engine capable of handling multiple data acquisition tests simultaneously. The system incorporates a loadable program store, a simple instruction set, and a development environment to address the specialized and unique problems facing scientific and engineering users with data acquisition needs. For those researchers involved in unique experiments demanding very high performance requirements, the DA/CP is the only alternative to custom-designed hardware. For manufacturers with expertise in specific data acquisition fields, the DA/CP represents an opportunity to add hardware and software value to a well-integrated computer system.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 704 *Average 705* *Low 706*

Protect your sensitive IBM data with our new Fiber Optic Link

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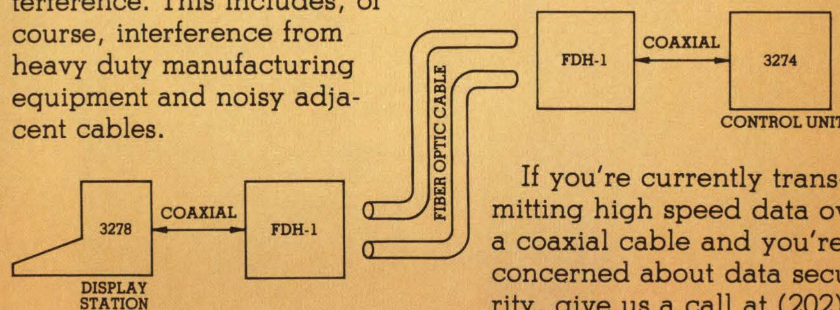

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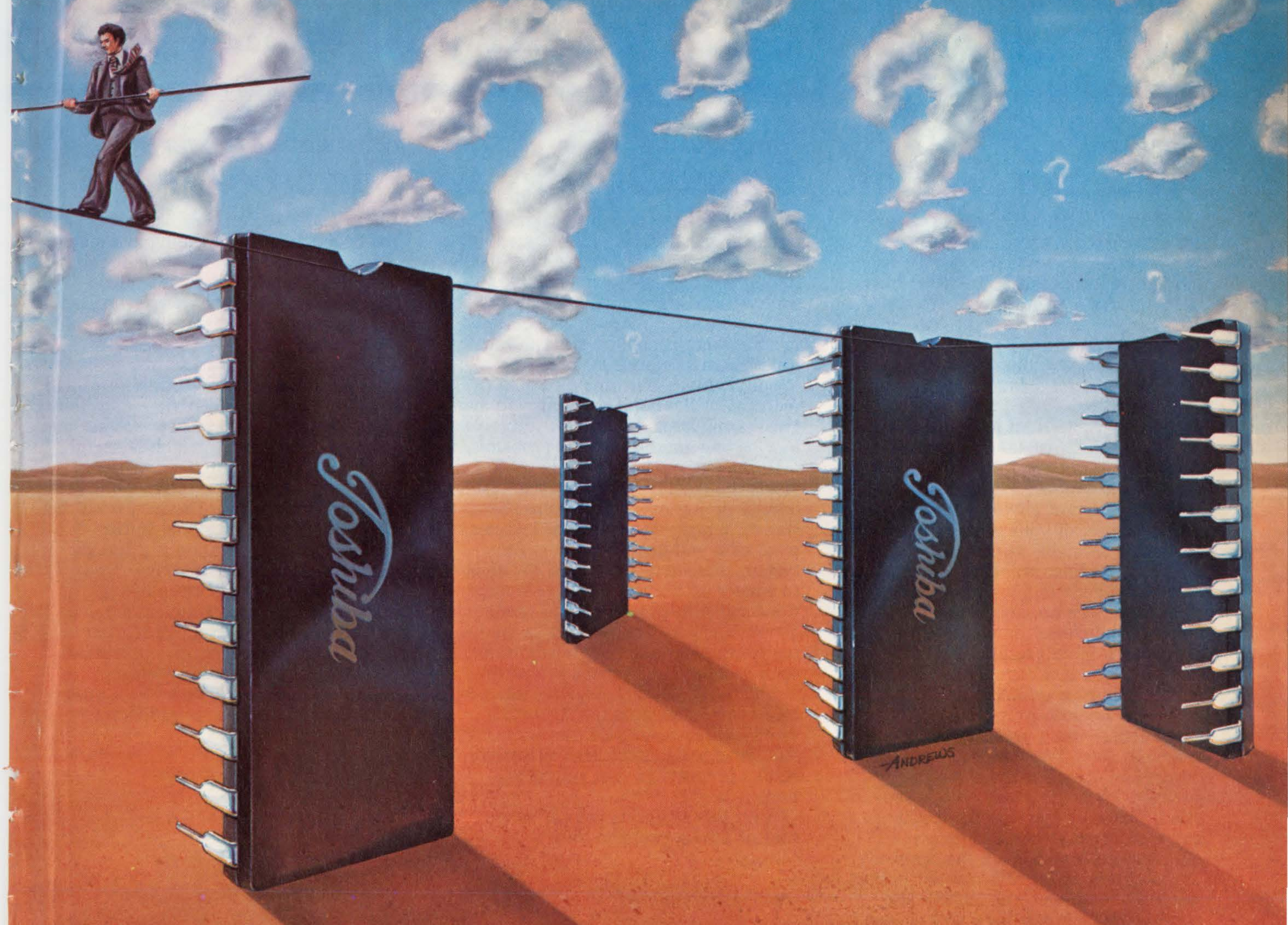
CIRCLE 58

THE ANSWERS.



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Max. Clock Freq. (typ) J/K F•F (C_L = 15pF)	60MHz	45MHz	20MHz	2MHz
Quiescent Power Diss. (typ) (GATE)	0.01μW	8mW	0.01μW	0.01μW
Noise Margin V_{IH} (min)/V_{IL} (max)	3.5V/1.5V	2.0V/0.8V	4.0V/1.0V	3.5V/1.5V
Output Current $\vert I_{OH}\vert$ (min)/I_{OL} (min)	4mA/4mA	0.4mA/4mA	0.36mA/ 0.8mA	0.12mA/ 0.36mA
Op. Volt. Range	2-6V	4.75-5.25V	2-8V	3-18V
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CIRCLE 59

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CIRCLE 60

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CIRCLE 62

A SUPERMINI FOR SUPERMAXI TASKS

Single-package machine executes 16M-byte tasks using a dual-band 32K-byte cache memory and a writable control store.

by Robert L. Hawk

Designing for an optimum cost/performance ratio sometimes runs counter to computer design engineers' natural inclination. Those people, after all, want to use the fastest and most functionally packed chip to produce a computer whose performance is one up on the competition. To keep within the cost/performance goals set at the beginning of a project design, engineers must constantly make design tradeoffs between extrapolating from knowledge gained from the company's past products and developing new architecture that will ensure a product with state-of-the-art technology.

Keeping a close eye on the cost/performance goal, engineers constantly adhered to three key principles in designing the Concept 32/67. These principles were a top-down hierarchy, and the use of specialized circuits and redundant components where applicable.

In a top-down hierarchy, all design parts have the most powerful and advanced technology at the highest level of interaction, with less costly broader-based technology at lower levels. For instance, the hierarchy of the 32/67 memory includes a 32K-byte dual-bank, 2-way set associative cache memory in the central processing unit (CPU)—a unique feature among competitive machines. Below that level in the memory hierarchy is a 16M-byte metal oxide semiconductor (MOS) memory with a 300-ns access time. At the bottom of the hierarchical memory structure is virtually unlimited rotating or mass memory.

Using specialized circuits, rather than a general purpose chip could better integrate functions to accomplish a particular end. In the Concept 32/6780 configuration—CPU plus internal processing unit (IPU)—the IPU performs only computational tasks and is relieved of any input/output (I/O) functions. At the same time, the CPU hands off the great majority of I/O functions to the input/output processor (IOP), thus freeing the CPU to also concentrate on computational tasks.

The third principle, duplication or redundancy of components, ensures that certain performance improvements can be achieved at a small incremental cost. For instance, in a CPU/IPU configuration, either processor can be used as the CPU. Moreover, the machine will function properly even if one of the units is entirely out of the task stream. Similarly, since output to peripheral devices is the slowest function of any computer, the 32/67 machine, using multiple IOPs and intelligent controllers, can simultaneously drive a number of peripherals.

Using these principles, company engineers were able to pack a number of innovative features into this middle performance-range machine (1M to 3M Whetstone instructions/s) which is self-contained in a single cabinet occupying less than 5 sq ft of

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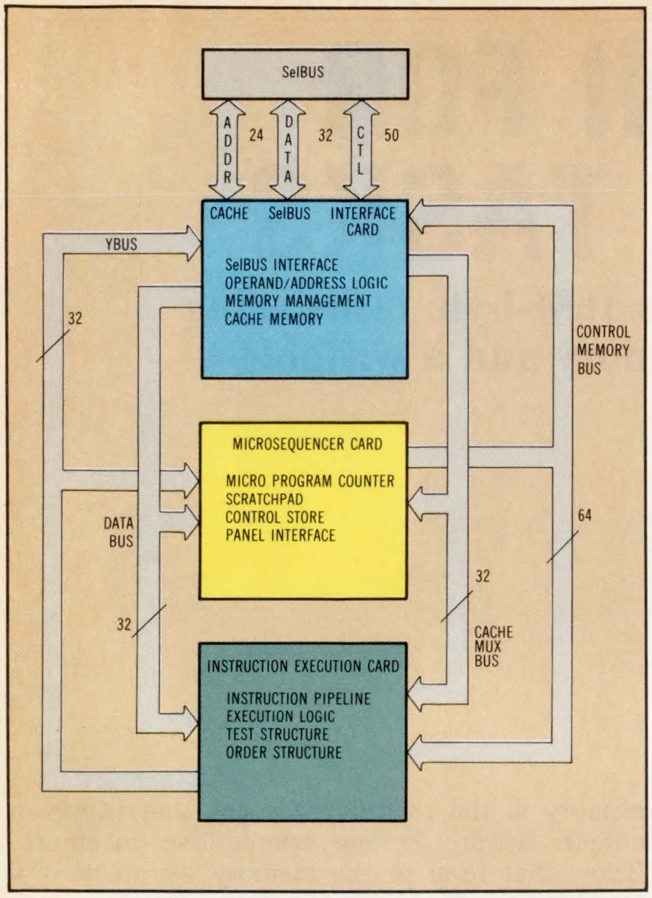

Fig 1 The CPU is made up of three multilayer printed circuit boards that connect to the SelBUS via data, address, and control buses. The cache SelBUS interface card performs the memory management functions, the microsequencer card contains the control store function, and the instruction/execution card houses the pipeline logic and diagnostic circuits.

floor space. Among the machine's innovations are a 32K-byte dual-cache memory, split into two 16K-byte sets of associative instruction and data banks; a writable control store that allows addition of unique instructions that execute in firmware at hardware speeds; and an alterable control store that permits field modification of the machine's basic instruction set.

Other features include the ability to run completely resident 16M-byte tasks and a 4-stage instruction pipelining scheme with effective 150-ns execution times. Also, a hardware and software architecture common to the entire Concept/32 family line allows running the Unix and proprietary MPX-32 operating systems. Thus, current users of Concept/32 superminicomputers can move to the Concept 32/67 with minimal effort.

System architecture

The CPU is made up of three printed circuit boards, with bipolar Schottky transistor-transistor logic (TTL) and bit-slice technologies (Fig 1). The microstore board contains the microsequencer of the machine: programmable read only memories (PROMs), random access memories (RAMs), and some of the microprogram counter control logic. The instruction/execution board contains the microprocessor bit slices, while the cache/SelBUS board houses the physical cache chips, cache control, memory map, and SelBUS interface.

Physically, the three boards are tied on the foreplane, with three rows of 96-pin connectors mounted on a different printed circuit board that has a common ground plane. Overall, close to 1200 integrated circuits occupy the three boards.

Perhaps the single most important feature of the 32/67 is its cache memory. In general, a cache memory is a high speed buffer memory physically located in the CPU and functionally located between the CPU and main memory. Its purpose is to hold portions of the contents of main memory, which are currently used by the CPU, or which can be expected to be used within the next few cycles of CPU time. The cache memory can provide dramatic increases in the total system's absolute execution speed. This was proven by special tests that were run to measure the 32/67's performance.

These tests measured the execution speed of single-precision Whetstone instructions using only one CPU. The computer's speed without cache memory was used as the baseline measurement. Through some unique software instructions, various parts of the cache memory were added to the CPU. Impressive increases in execution speed over the baseline measurement were obtained. (See the Table "Whetstone Performance.")

Toward a 100% hit rate

The cache memory consists of TTL 45-ns static RAMs, which are an order of magnitude faster than dynamic RAMs. The memory is split into two independent 16K-byte banks—the cache instruction bank and the cache operand or data cache—whose contents are acted upon by the cache instructions. Because the instructions are almost always present in the instruction bank, there is an almost perfect "hit" rate that allows the CPU to process near its maximum speed without being slowed down by waiting for either data or instructions to be brought in from the main MOS memory.

Since the cache contains only portions of main memory, its effectiveness depends on the percentage

Whetstone Performance

32/67 enhancement levels	Performance
CPU with no cache	100%
Addition of operand, cache bank only	120%
Addition of instruction, cache bank only	170%
Addition of operand and instruction cache bank	230%

of time that the required data can be fetched from the high speed cache rather than from the slower main memory. A cache "hit" occurs if the data are found in cache, and a "miss" occurs if the data are not located in cache and must be fetched from the main memory.

Each 16K-byte data bank can be considered independent, consisting of 2048, 32-bit wide locations. Both banks are associated with a set of index arrays, each containing the most significant 11 bits of the associated memory address and a valid (hit) bit (Fig 2).

As many as 2048 possible memory words can be contained in any given cache location, with one 2K-word operand or instruction cache, and up to 4M words (16M bytes) of main memory. With 32/67 containing two 2K-word operand caches and two 2K-word instruction caches in the worst possible case of a 4M-word program that just consists of instructions, only 2 of the 2048 possible alternatives can be simultaneously cache resident.

The cache index array tracks the content resident in cache at any given time. In combination with the valid flag, it provides a set of comparison data to determine if the required operand/instruction is cache resident.

Both cache banks (operand and instruction) are accessed in parallel; valid data can exist at the same locations in both banks concurrently. Valid data are moved from cache and replaced with newly requested data based on a decision as to which cache bank was last used. A RAM in the least recently used (LRU) circuitry is addressed in parallel with the cache banks, index arrays, and valid RAMs to determine for the specific address required which cache bank was used least recently. The data are then written into the selected cache bank.

An example of manipulating a large array demonstrates the dual cache's power. This type of program would be small and its routines would fit nicely in the 16K-byte instruction cache. The array data would be moved in and out of the other side of the cache, yet the program would be functioning at a 100% hit rate in the instruction bank. In most other cache systems, instructions and data are mixed together as new data are brought into those cache memories. Thus, the instructions are purged unnecessarily.

The overall hit rate for the Concept/32 is in the high 90% range and can be 100% in the cache instruction bank. If there is a miss, the cache's intelligent control initiates an access to main memory, bringing the referenced item into the data cache bank for use. At the same time, it brings more data than necessary into the cache—data that are located near the requested data—on the "look-ahead" theory that the processor will also need that data very soon. Such block moves of memory are built into the entire product line.

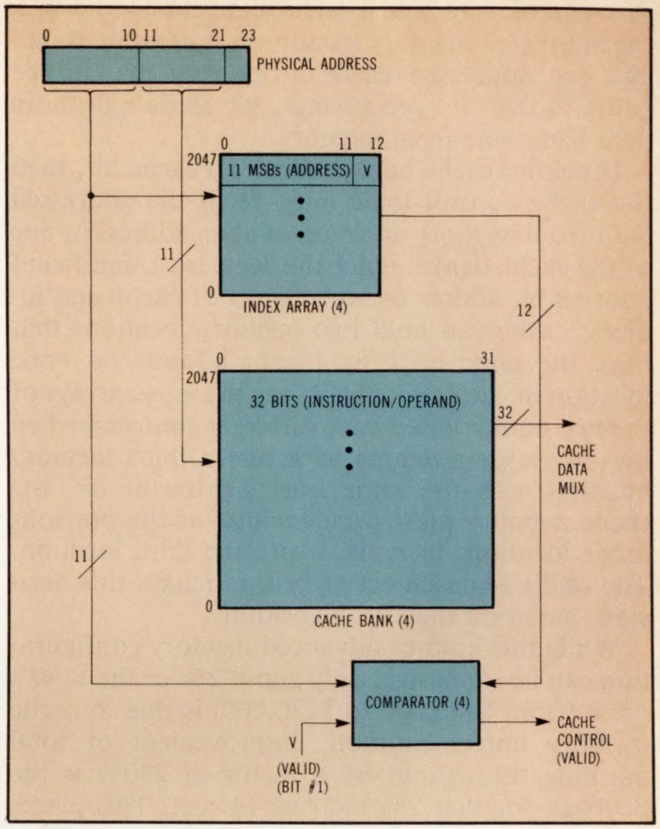

Fig 2 The cache memory is divided into two 16K-byte banks. One bank shown consists of 2048 locations, each being 32 bits wide. The 11 most significant bits (MSBs) of a physical address are compared with 11 most significant bits from the index array to determine if a given operand or instruction is cache resident.

When additional data are brought into the cache memory, usually some existing data must be overwritten. Some competitive systems use a first-in, first-out concept that often leads to "thrashing" if the overwritten data are soon accessed again. Other competitive systems use a random replacement algorithm. The algorithm used in the 32/67 replaces the LRU data resident in cache on the principle that if the processor has not recently called on a location, it probably has no further need for the data stored there. Just in case it is needed, a backup copy of the data in cache is in main memory.

The 32/67's 2-way set associative technique organizes small high speed memory cache so that it contains a variable subset of a much larger, but slower, memory. As the main memory loads the address into the cache, the most significant address bit is stored in one of the two indexed arrays at the same location as the address of the least significant bit. The index array also carries a valid bit for each index location, which is set when the upper address bits are loaded into the index RAM. This bit validates the index location.

During read operations, the memory address's low order bit addresses cache index array RAMs. Upper order bits of the memory address are compared with the index array contents. If they agree, the valid bit is set and a cache hit occurs, indicating the addressed memory location is present in cache, and the addressed cache array contents can be gated to the CPU processing logic as though those data had come from memory.

If neither cache bank indicates a cache hit, then the cache control logic must fetch the addressed data from memory and store it at an address in one of the cache banks. Since the same least significant address bit addresses both banks of cache and indices, cache can hold two memory locations that have the same least significant address bit—one location in each cache bank. As the index arrays of the two banks would have different contents, when the processor attempts to access a third memory location with the same least significant bit, the cache memory must decide which of the previous cache locations to replace with the third location. The cache replacement algorithm makes this decision, based on the LRU algorithm.

While this kind of advanced memory configuration can be expensive, only about 2% of the 32/67's price (from $120,000 to $170,000) is due to cache memory implementation. Improvement of total machine throughput by a factor of 230% is the payback for that 2% increase in cost. This places the 32/67 in a favorable price/performance position vis-à-vis its competitors.

Writable control store

Usually a relatively expensive option in other superminicomputers, the writable control store (WCS) is a basic feature of the 32/67. With WCS, a user can create custom instructions, developed in microcode, and place them in firmware for CPU use as if they were parts of its own instruction set in PROM. Thus, routines that were previously only executable as software loaded in main memory can become a part of the machine's instruction set, executing at hardware speeds. Graphics applications, where frequently used subroutines could be written into WCS and executed at hardware speeds, would be a typical WCS use. Theoretically, the improvement in speed, through execution of instructions in WCS, is about four to one over a fully optimized software routine.

The total address range of the microengine's control store is 12K of 64-bit words. PROMs populate the first 4K; WCS makes up the next 8K, in 4K x 64-bit control store memory. The micro assembler and MPX-32 control store loader support this 8K of WCS. WCS routines can be interrupted, then resumed at the breakpoint. This is a vital consideration in realtime situations, such as simulations where some outside call to the CPU gets absolute priority. Writing into the WCS can be done through macro-level instructions, such as those used by a software programmer or through the optional diagnostic processor.

A similar feature that allows the actual CPU instruction set to be modified is the alterable control store (ACS). Besides being resident in PROM in the first 4K x 64-bit word of the microengine's control store, the instruction set is also mirrored in a 4K ACS with duplicate addressing. The duplicate instruction set in the ACS, rather than the instruction set in the PROM, drives the machine. By changing the instruction set in the ACS, the machine's basic "personality"—the instruction set in PROM—has been effectively altered without changing the PROM. Aside from the obvious ability to change personality without changing PROMs, this arrangement has a second advantage: if updates to the PROM become necessary, they can be sent to the field on magnetic media and installed without changing the hardware.

Available operating system and diagnostic software packages allow the ACS to be loaded from either patches (minor corrections) or from a complete set of microcode. This capability reduces the risk of microcode errors, thereby minimizing downtime. The ACS is both readable and writable through both of its access paths, thereby providing a means to verify its content and to exercise it and verify its functionality.

A flexible addressing scheme allows a 16M-byte task program and data tasks to be run. It also comes in handy for applications such as very large structural design programs, image processing, seismic efforts, and large database manipulation. To achieve a fully resident 16M-byte task, the machine uses 2048 map registers, 8 base registers, and 8 general purpose registers. Further, a variety of separate addressing techniques can be used to support the most efficient programming routines: direct, indirect, indirect indexed, indirect pre- and post-indexing, and direct/base register and base/indexed addressing.

The diagnostic processor greatly enhances the user's ability to program the WCS.

This flexible addressing scheme's core is a 4-stage pipeline in the CPU that separates the four main parts of instruction execution—fetch, decode, execute, and store. This pipeline is functionally the same as the one used in the 32/87. (See *Computer Design*, "Besting the Benchmarks—Supermini Style," Aug 1982, p 131.) The pipeline can run simultaneously in a CPU and an IPU.

The instruction pipeline is the direct information channel through which machine instructions pass from macro level to micro level. The pipeline consists of four stages: backing store, decode, vector, and execute.

All instructions pass through each stage of the pipeline during their execution. In general terms,

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Event Trigger	1	1	1
Software Breakpoints	8	8	8
Exernal Probe	1	1	1
Debugger Commands	31	29	29
Real Time Trace Size	4K x 40	2K x 32	2K x 32
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Emulation Modes	3	3	3
Mapping Incruments	1K Blocks	1K Blocks	1K Blocks
Mapping Range	1M Byte	64K	64K

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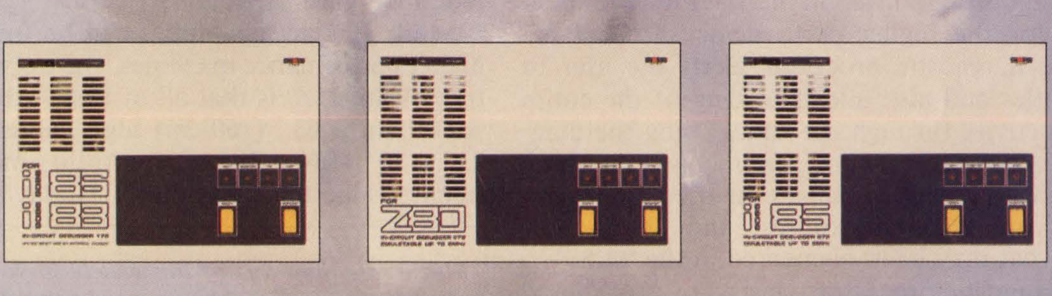

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CIRCLE 63

the functions of the four stages can be categorized as follows:

- The backing store stage loads the instruction from cache memory.
- The decode stage decodes the instruction and computes the effective address.
- The vector stage finds access to the decoded address in the control store unit, translates it into a physical address, and fetches the operand.
- The execute stage executes the instruction, stores the result, and fetches the next instruction.

For example, as instruction 4 is being fetched at the top level of the pipeline, instruction 3 is being decoded at the next level, instruction 2 is being executed, and the results of instruction 1 are being stored.

An individual move through the 4-tiered pipeline takes 600 ns/instruction. However, once the pipe is primed by the fourth fetch, the process is effectively operating at an instruction completion rate of once every 150 ns, the typical processor speed for most single instructions. When a branch condition exists in the program that breaks the pipeline, the worst case is 600 ns. If the next instruction is in cache, the pipeline will be filled in less than 600 ns.

For maximum performance, an IPU can be added to increase the throughput to more than 3M Whetstone instructions/s. The optional IPU is a three printed circuit board processor set, physically identical to the primary CPU. Through selection from a front panel switch, either of the two processing units can serve as the CPU. The other acts as the IPU. If there is a malfunction in one processing unit, the other can be switched in as the CPU. In effect, this provides a redundant backup CPU. Addition of the IPU is totally transparent to programs, thus eliminating any software alteration to achieve the 80% throughput improvement.

Made up of two printed circuit boards, a floating point processor, which handles floating point calculations in hardware in a fraction of the time required by software, can also be added to both the CPU and the IPU.

Onboard diagnostics

Self-diagnostic routines in the 32/67 were first developed for the higher performance 32/87. Basically, the diagnostic processor alerts the user to irregularities and also allows tracing of the entire flow of activity through the CPU. Using the diagnostic processor to monitor precisely what is going on in the CPU greatly enhances the user's ability to program the WCS and to test and debug subroutines that may be implemented in the WCS.

The diagnostic processor consists of a Z80-based processing unit that contains the controlling intelligence for the diagnostic system. It interfaces to the IOP, system console, modem, and to the multipurpose bus. This bus gives it access to a floppy disk controller and line printer. Another interface board connects directly to the 32/67's CPU. It sets up the different kinds of control the user wants to exercise over the CPU and directs implementation of that control at the CPU level.

In addition, the diagnostic processor executes at two levels of machine instructions. At the macro level, the processor executes instructions similar to those generated by programmers writing in assembly language or to those generated by compilers for the many high level languages available to the machine. Such macro-level instructions are refined in the CPU to several, and in some cases, many microcode instructions.

At the second or microcode level, the user has true insight into the workings of the computer. In general, microcode instructions are unavailable to the programmer in the field. However, by using the 32/67's ACS and its diagnostic processor, microcode instructions can be loaded directly into the machine. With a 150-ns known instruction execution time, tracing individual bits through the machine's various buses becomes easy.

By looking at the microprocessor program counter or the contents of the registers, the diagnostic processor can take snapshots of the result of execution of any microcode instruction. Conditions can be set in the diagnostic processor that will, when met, halt execution in the microprocessor for evaluation. Previous snapshots, either on the cathode ray tube or on a printout, can tell exactly what brought about the particular condition. A related use for the same type of diagnostic procedure is in taking a snapshot history of the machine's microcode execution when it is functioning properly. When it is malfunctioning, this serves as a standard for reference against a duplicate set of snapshots. Overall, this ability to perform diagnostics at the microcode level allows failures to be isolated to much narrower segments of the machine than simple tracing of the macro-level instructions.

Another feature of the diagnostic processor is diagnosis from a remote location via a modem port and telephone line. The total diagnostic set at both macro and micro levels can be loaded using this remote linkage capability.

While similar capabilities can be found in most higher performance machines, the outstanding feature of the 32/67 is that all of these advantages are packed in a 63" (160-cm) high cabinet, within a 23" x 30" (58- x 76-cm) footprint, making it the smallest superminicomputer on today's market.

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HP's 5180A...the Waveform Recorder for bench and ATE.

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In either environment, the 5180A can do the job of several instruments, saving you cost and complexity.

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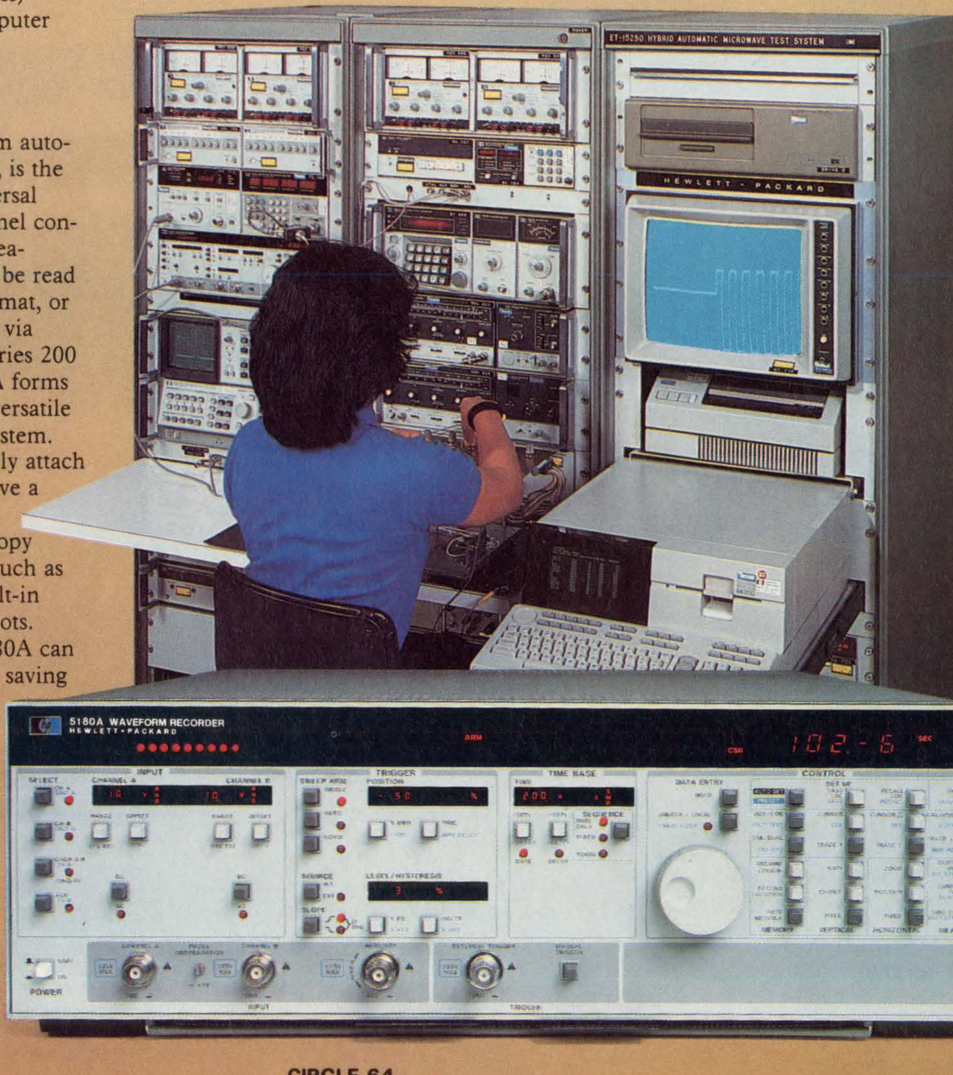

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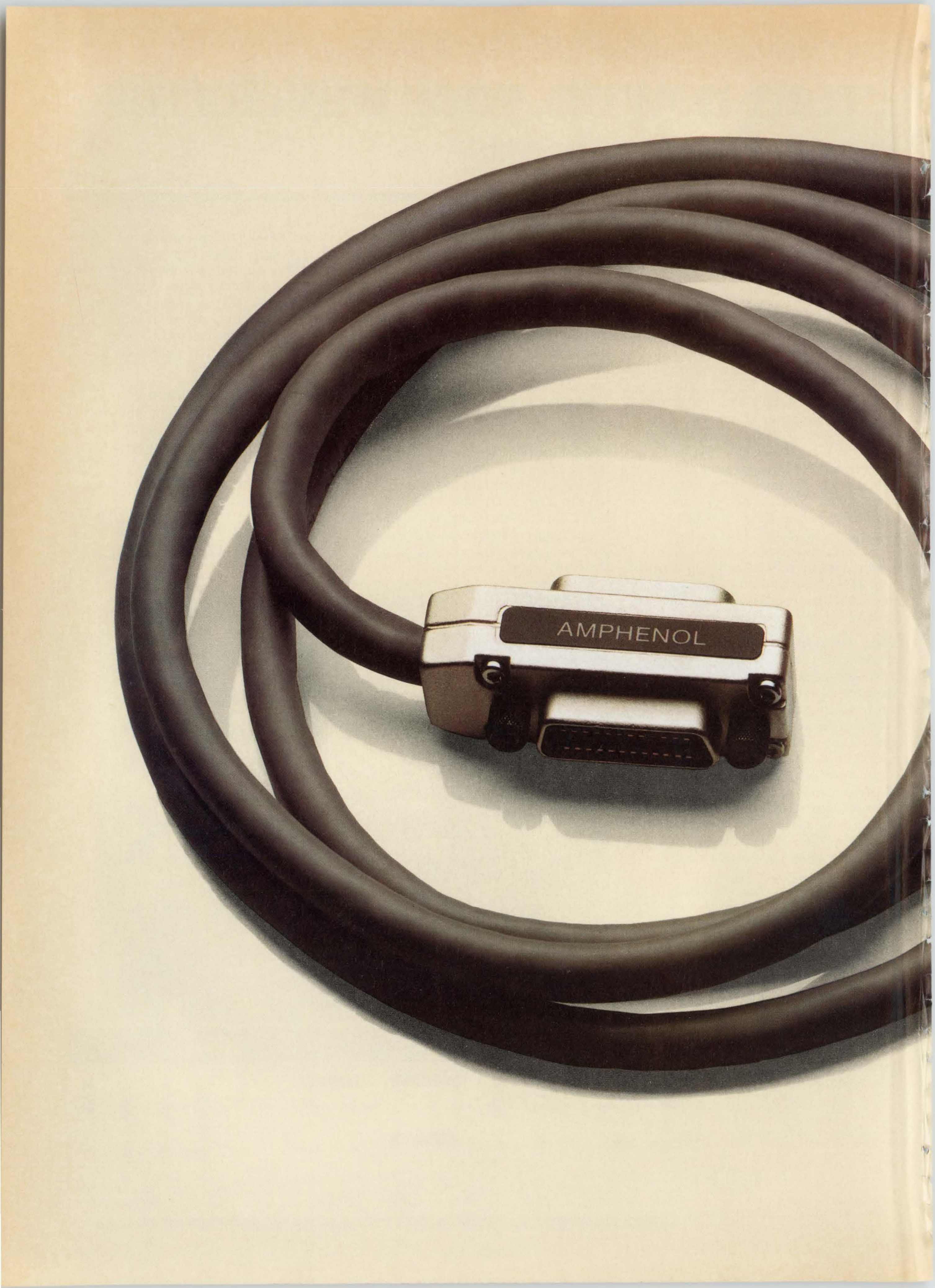
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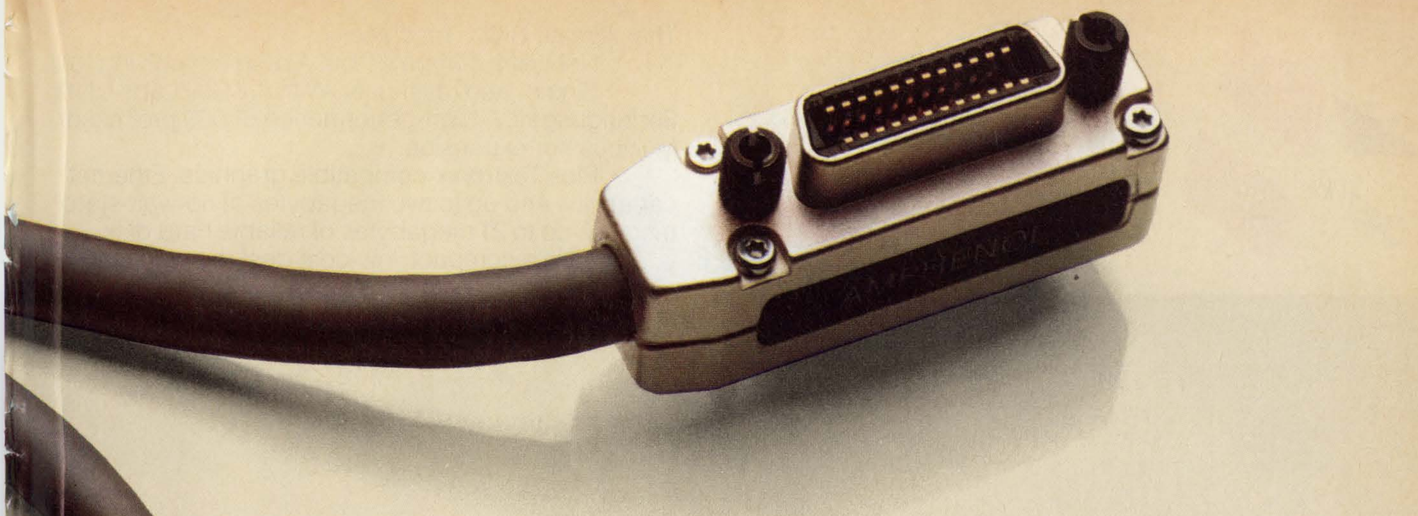

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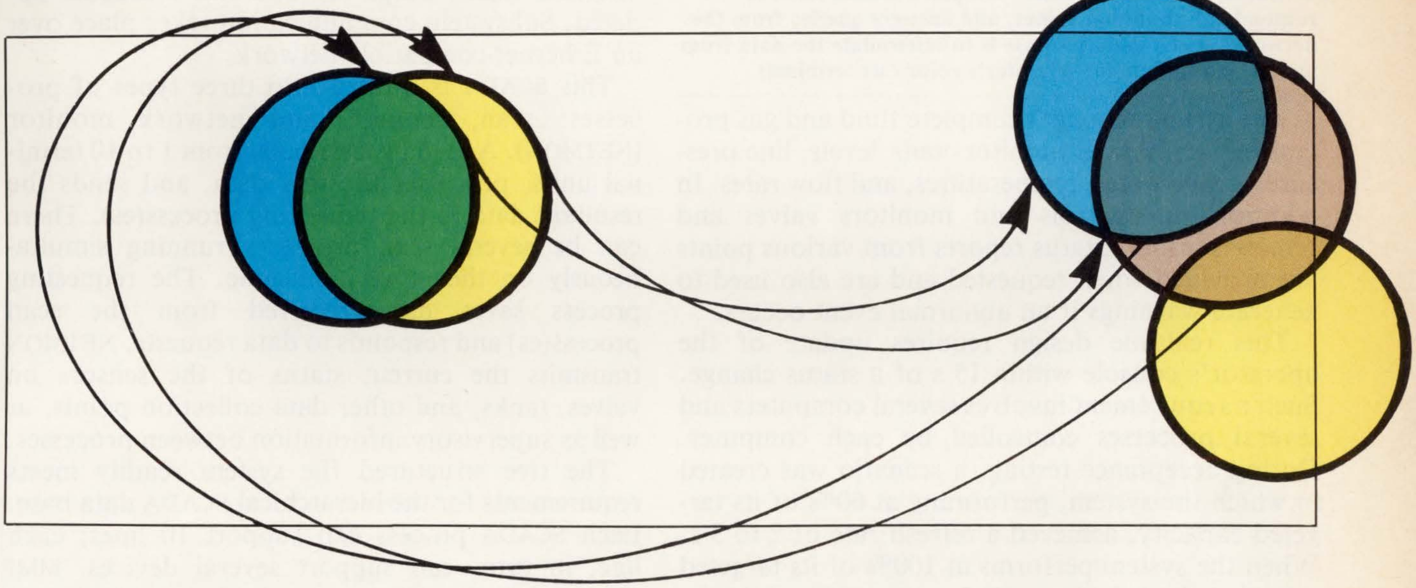
ADA

THERE IS REAL TIMELINESS IN UNIX

Contrary to conventional beliefs, Unix performs quite well in realtime process control settings.



by Dan E. Ladermann and David J. Preston

In the world of small computer systems, Unix and realtime applications are thought to be mutually exclusive. The reasons for this are varied, but, in general, have to do with the way the Unix operating system handles files, processes communications requests, and delegates responsibility within both its command shell and kernel. As experience frequently shows, conventional wisdom is often wrong. Such is the case where Unix and realtime applications are concerned.

While it is true that generic versions of Unix in no way support realtime functions, modified versions of Unix abound that do. By altering file structures, priority scheduling, and interrupt handling routines within the Unix system, an effective, realtime operating system for process control can be sculpted out of the Unix massif. This, in fact, is exactly what has been done in crafting the Unix operating system to meet the demands of an oil transmission facility in the Middle East. In the process of melding Unix to a process control system called Pilot network (PNET), designers extracted the best of the Unix operating system. This particular system uses networking, distributed realtime processing, and color graphics to control and monitor the flow of petroleum products across Saudi Arabia.

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David J. Preston is director marketing for The Wollongong Group. Previously, he was manager of product marketing for Perkin-Elmer Corp. Mr Preston holds a BSEE from the Newark College of Engineering.

Constructing the system

PNET is built around a 10M-bit Ethernet system and connects several different processors that run Unix. Included are two Digital Equipment Corp PDP-11/23s, a Perkin-Elmer 3230, and an Onyx Z8000 based system. Operator workstations consist of Ramtek color terminals, while supervisory and programming work is performed on a variety of cathode ray tube (CRT) terminals. Subsystems managed by the application include a tank farm, an associated pipeline, and refinery facilities.

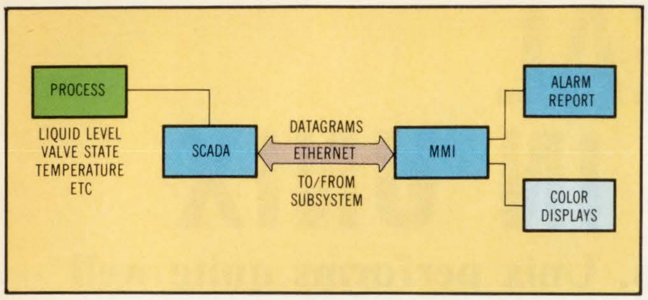


Fig 1 The SCADA and MMI subsystems communicate via datagrams, which are sent by the 10M-bps Ethernet bus. SCADA monitors the sensors, computes measurements, responds to abnormal values, and answers queries from the network. MMI's main purpose is to interpolate the data from SCADA and update the operator's color CRT terminals.

The system manages complete fluid and gas processing facilities. It monitors tank levels, line pressures, valve states, temperatures, and flow rates. In addition, it controls and monitors valves and remote sensors. Status reports from various points are provided when requested and are also used to generate warnings if an abnormal event occurs.

This realtime design requires update of the operator's console within 15 s of a status change. Such a requirement involves several computers and several processes controlled by each computer. During acceptance testing, a scenario was created in which the system, performing at 60% of its targeted capacity, achieved a refresh rate of 2 to 3 s. When the system performs at 100% of its targeted capacity, the refresh rate is 5 s—one-fifth of the required maximum. Thus, the system comfortably meets its realtime response requirements.

PNET is implemented as two major subsystems (Fig 1), each operating on a separate computer. This hierarchy is further divided into multiple cooperative processes. With hierarchical levels of directories and subdirectories, the Unix file system is exploited in both the development and online design to speed system delivery. Interprocess communication is accomplished using pipes. (See the Panel, "Unix Pipes.")

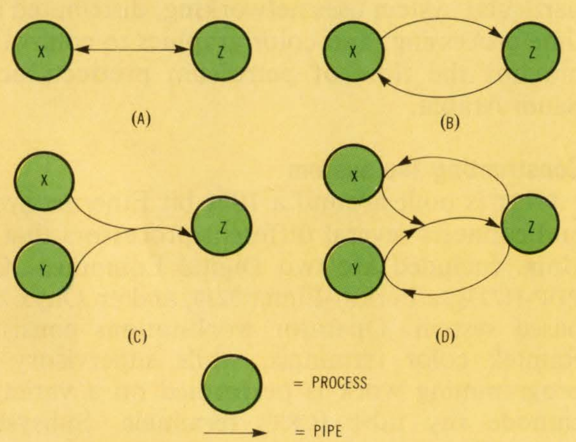
The first subsystem, a classic supervisory control and data acquisition (SCADA) control system, maintains a realtime data base of the monitored points (Fig 2). The second subsystem, the man-machine interface (MMI) keeps the operator's console updated. Subsystem communication takes place over an Ethernet-compatible network.

This SCADA is broken into three types of processes: scan, request, and network monitor (NETMON). A scan process polls from 1 to 10 terminal units, processes the raw data, and sends the resultant data to the requesting process(es). There can be several scan processes running simultaneously on the SCADA machine. The requesting process saves data received from the scan process(es) and responds to data requests. NETMON transmits the current status of the sensors on valves, tanks, and other data collection points, as well as supervisory information between processes.

The tree structured file system readily meets requirements for the hierarchical SCADA data base. Each SCADA process can support 10 lines; each line, in turn, can support several devices. MMI (Fig 3) consists of two processes: update and NETMON. An update process issues requests that, through the NETMON processes and network hardware, are automatically routed to the proper process within the SCADA system. It then receives the

Unix pipes

Under Unix, interprocess communication occurs via a pipe. It is used when one process must send data to another while they are both active (as opposed to the first process creating a file and completing, then the next process reading that file). A pipe is a conduit with two ends, each of which is attached to a different process. One end appears as a write-only file, the other as a read-only file. The Figure shows four typical pipe uses.



The first example (A) illustrates how one process uses a pipe to send data to another process (1-way communication). Example (B) depicts how the same two processes accomplish 2-way communication. A useful feature of pipes is that the write-end can be connected to many processes simultaneously. Unix thus guarantees that any message written by any one of those processes arrives at the read-end intact.

In the next example (C), processes X and Y can both send a message to process Z at the same time, and each message will arrive ungarbled. The last example (D) shows how pipes can be used for 2-way communication between more than two processes. Process Z can be used to route messages, or can even be a database manager, while the other processes request transactions. Also, due to the way pipes deliver messages, concurrency control (lockout) is implied.

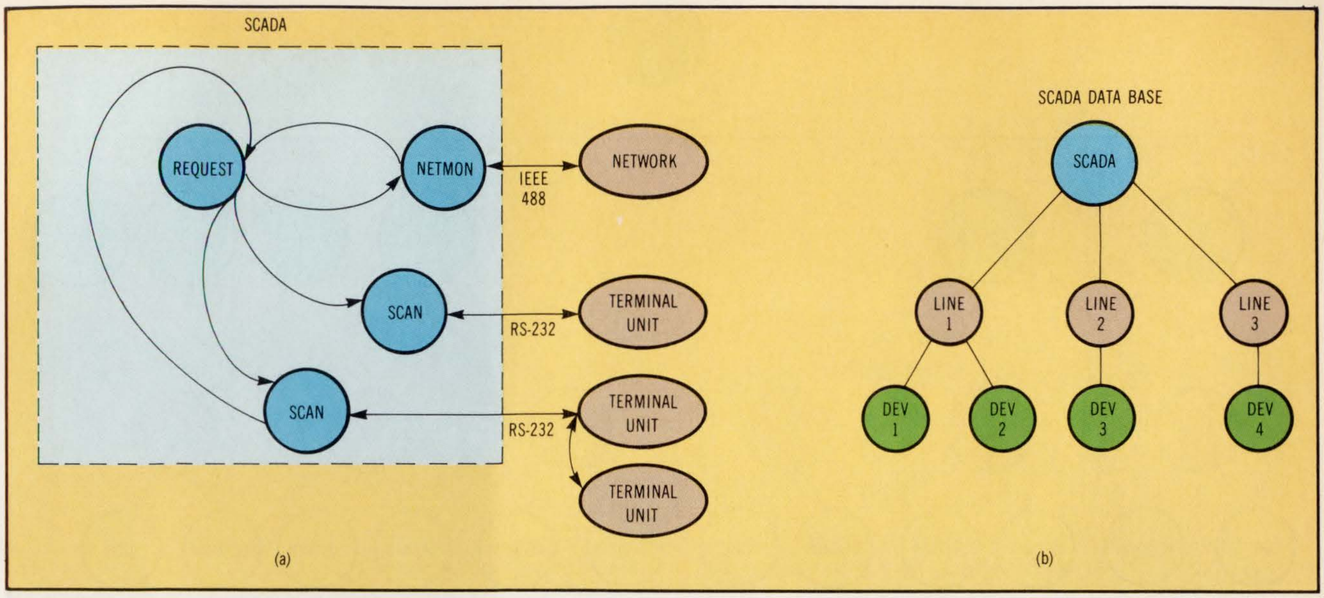


Fig 2 The SCADA subsystem (a) manages interface devices and responds to status requests via the network. The various processes communicate through Unix pipes. SCADA, which serves as the main directory, has a subdirectory for each hardware communication line in the system (b). Each line, in turn, has subdirectories for each of the devices connected to it. These lowest level directories contain information about specific device parameters.

SCADA response and updates the operator's console with the most current information for that data collection point.

Because protocols are defined outside the process, the NETMON process interfaces the subsystems using any communication protocol desired. Note that with this modularity, point to point or network datagram communications can be used by simply invoking the correct process. None of the other processes in either subsystem have to be modified, recompiled, or reloaded. Thus, the subsystem approach adopted via Unix mirrors the hardware world where differing computer architectures can be connected by using standard interfaces (eg, RS-232 and IEEE 488).

Streamlining with Unix

Software development is the first commercial and most widely accepted use of Unix. The combination of easy to use yet comprehensive utilities, plus the basic structure of the Unix file system, simplifies automating software development cycles. Unix provides a homogeneous system for the development and control of documentation. Source code development and management of software projects are other important benefits.

Unix offers full screen editors, a powerful text processing system that provides access to letter-quality printers, and photo-typesetter output that can be diverted to laser printers for high quality bulk documentation. All of these tools provide a natural, trackable flow of information from the initial design proposal, through system specification, to final application documentation and system delivery. With Unix, the developers can put the information online once. And tools provided can eliminate redundant work and increase software development efficiency.

The PNET system is decomposed into subsystems (Fig 4), then into specific processes (eg, SCAN, REQUEST, and NETMON). Unix directories and header files are designated for design, coding, and documentation efforts. These directories parallel the natural structure of the project and are added to as the project progresses. During the entire span of the project, the names and locations of all files remain consistent. This structure helps facilitate top-down development methodology, as well as maintaining an ordered approach.

Unix maintains access permission information for every file and directory of the system. This allows their creators to control access to the data within the file. Permissions for access are based on file or directory ownership, and the relationship of the owner with other users on the system. This

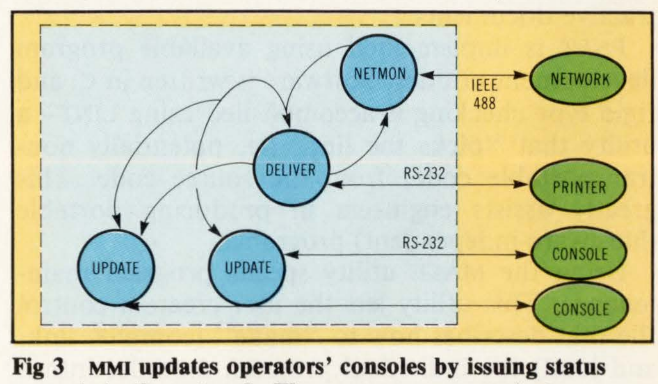


Fig 3 MMI updates operators' consoles by issuing status requests to the network. The processes communicate through Unix pipes. Many update processes may be running, with each operator using a different display.

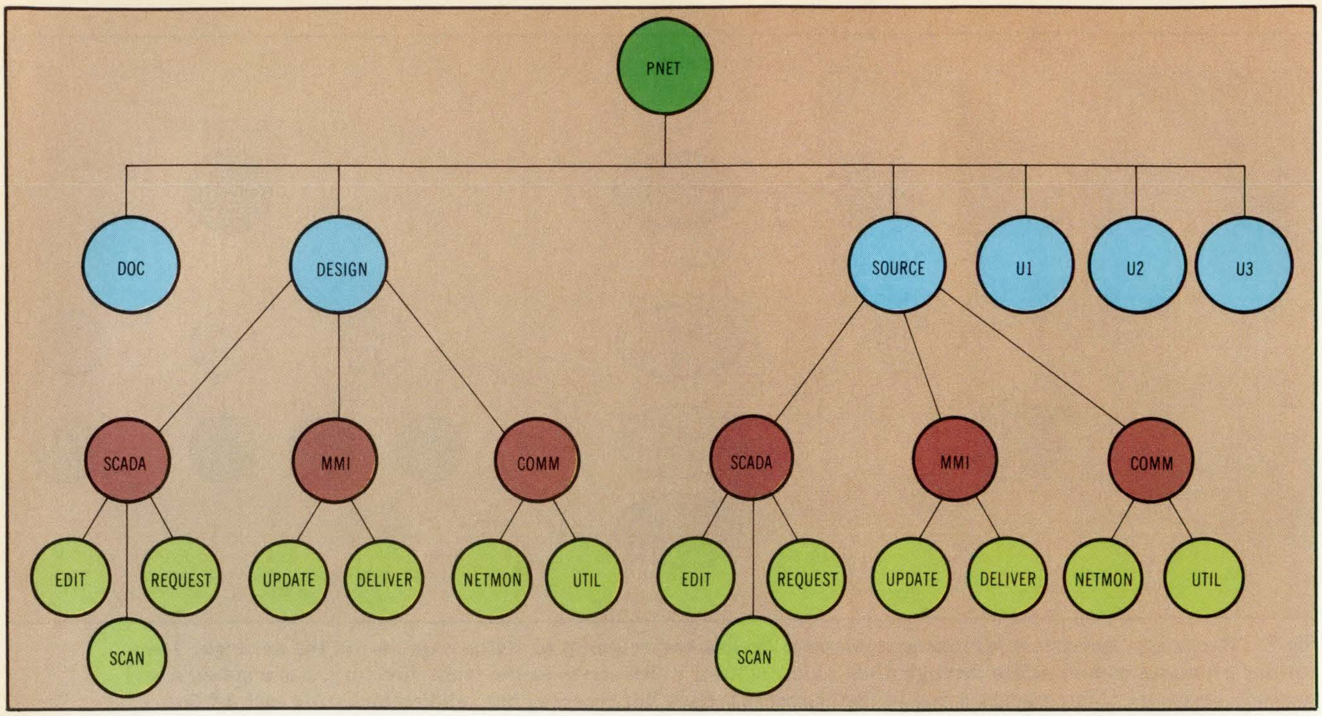


Fig 4 In the PNET project, organized in the Unix file system, each team member has a directory (illustrated as U1, U2, and U3). Miscellaneous documents are developed in the document directory.

relationship is further defined by allowing the creation of group (cooperative team) and nongroup (system-wide) file accesses.

To round out the protection scheme, Unix allows the creator of a file to define what type of access is permitted to each class of user. File owners define read, write, and execute permissions for their individual use, local group use, or for any other users on the system. A PNET group allows full access by any member of the project team, but no access to other system users.

Design documents consist of manuscripts defining the requirements, specifications, and pseudocode outlines. Manuscript documents are prepared using the standard Unix formatter and document preparation packages. Split-screen and insertion features of the editor speed pseudocode preparation. These tools provide an easy method to define the pseudocode, modify the supporting text, and generate attractive documents.

PNET is implemented using available program development utilities. Software is written in C, and rigid type checking is accomplished using LINT—a utility that "picks the lint" (ie, potentially nontransportable code) from the source code. This greatly assists engineers in producing portable (hardware-independent) programs.

Using the MAKE utility speeds program maintenance. This utility lets the user create a control file that describes how to "make" (compile, link, and load) the individual program modules into a single executable program. MAKE also provides a "best case" compilation and link loading procedure, so that unmodified source need not be recompiled. It also ensures that modified files are not excluded from the recompilation and linking process. Experienced Unix users could assist novices by preparing command scripts and MAKE description files, resulting in higher productivity at the steepest point of the Unix learning curve.

The source code control system (SCCS) provides efficient modification controls and tracking for all documentation and code. It also provides complete version tracking and previous version regeneration capabilities. Moreover, it imposes an effective method for total configuration control, since it only records the changes made to a file. Thus, disk space is conserved, while full reproduction of previous versions of the software or documentation is ensured. This utility contributes to the reduction of development time, since changes can be removed or added at will.

Fig 5 typifies an SCCS scenario. In this example, phase 1 of the development of a module has been completed and version 1.4 is ready for integration

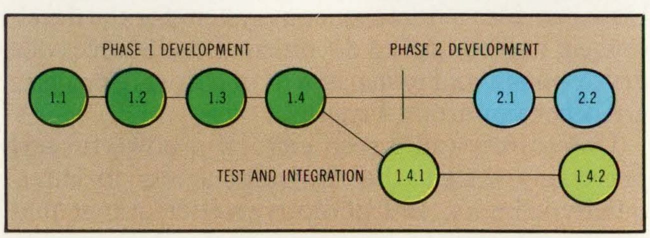


Fig 5 Use of SCCS during development permits the original version (1.1) and the changes to be kept, rather than keeping copies of each version—a net disk space savings results. Only one user can access and change a file at any given time; all others must wait. SCCS also provides file management reports.

and testing. Integration and testing of version 1.4 can proceed while development of phase 2 continues. As an example, the SCADA subsystem can be integrated and debugged while the MMI system is still being coded.

Once testing and integration are complete, the two versions can be merged and development can continue. There is only one copy of the SCCS data base. SCCS also provides access controls and restrictions, thus preventing several users from updating the same version of a document or program at the same time. Unauthorized personnel cannot update the files under SCCS control at this stage.

Device drivers key to performance

Many realtime applications require special device drivers to handle high speed device requirements, such as analog to digital converters and high speed networking interfaces. Custom device drivers support many special purpose realtime systems. Unix device drivers, including interrupt handlers, are written in the C language. This makes them easy to create and modify. This can be contrasted with most operating systems, where device drivers are written in assembly language: a most laborious process. Most Unix device drivers consist of less than 8 pages of code, including comments.

There are, of course, some realtime applications that are better suited for special purpose operating systems designed for realtime operation, such as Perkin-Elmer's OS/32 or Gould/SEL's MPX-32 operating system. The problems involved in a distributed, realtime event driven processing environment are addressed, however, with capacity to spare, on a Unix based system.

Multiprocessing, pipes, consistent file interface, and the hierarchical file system ease implementation. There is no need to redevelop or modify any of the standard device drivers. In fact, a special device driver supporting IEEE 488 is available. Consequently, all the facilities needed to implement this system exist within Unix.

PNET proves that a standard Unix system, without modification, can be used to support a large percentage of realtime application projects. Researchers and developers should keep in mind that there are still areas for improvement. Despite this, no existing operating system compares with Unix's field proven reliability and wealth of development and support utilities.

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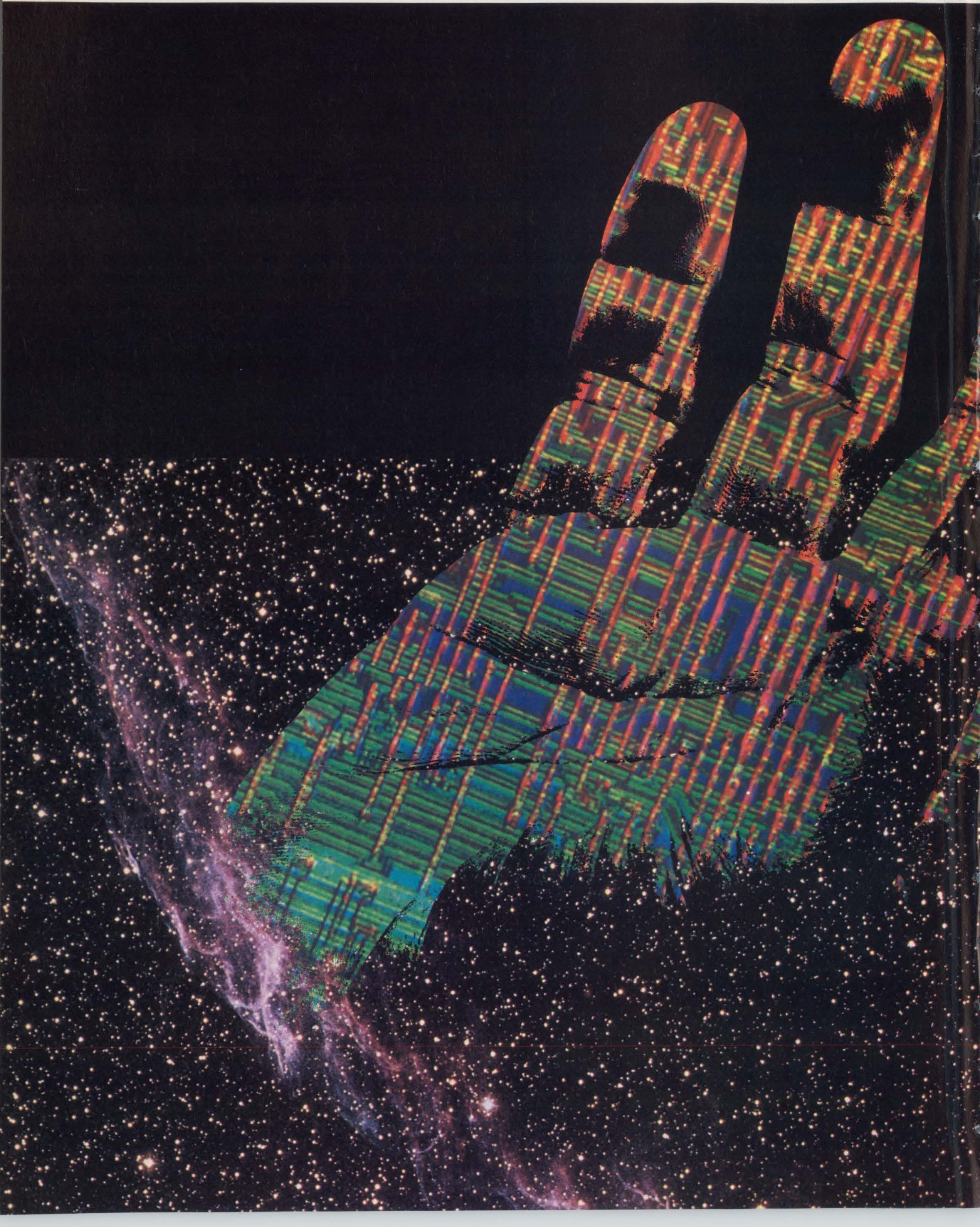
Where in the Microworld



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CIRCLE 71

SPECIAL REPORT ON

TERMINAL AND PRINTER TECHNOLOGY

With more and cheaper computing power available, computer system designers can devote more of the system's data to controlling and driving two ubiquitous computer peripherals—the terminal and the printer. For their part, terminal and printer manufacturers are busily incorporating features that make their products more versatile, packing them with capabilities that complement every conceivable system application from word processing to color graphics.

The quest for a reliable printer that can generate a letter-quality hard copy with color graphics at a reasonable speed and can also do so repeatedly is stretching both impact and nonimpact technologies to their limits. As a result, more automated functions and software-generated commands are being incorporated into the dot-matrix printer workhorse while researchers are working to develop reliable nonimpact ink-jet and thermal transfer printers. The market share for these printers is growing at a faster rate than that of the dominant impact printers. The staff report on printer technology highlights the advances that allow for this fast growth rate, which is especially true in Japan and Europe. Printer noise—a point of contention between vendors and users—is discussed in a separate article. Its author discusses current standards and offers one solution to a printer noise standard that could satisfy all concerned parties.

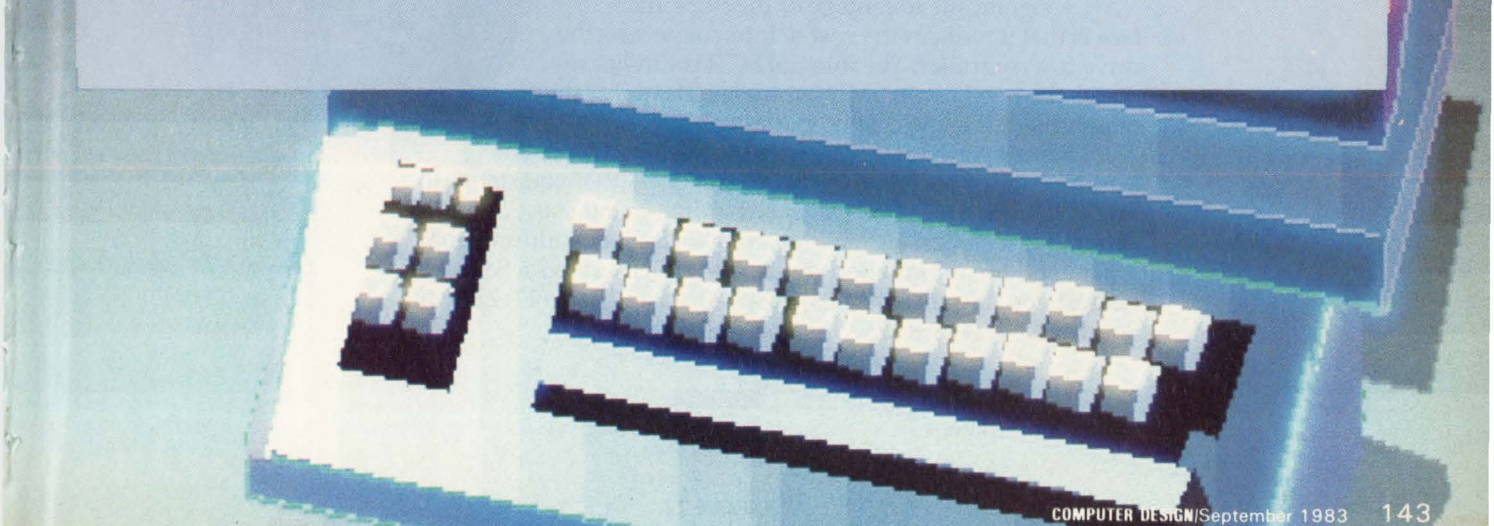
The technological progress in graphics for terminals, though, seems unabated. Two separate articles highlight how LSI chips make it easier to control video processing and all graphic and alphanumeric manipulations on the screen. Much formatting can be done up front before the characters ever reach the printout stage. This alleviates the normal overhead functions in the printer. Thus, terminals and printers are vying to become smarter with each taking on more tasks and thereby alleviating the other's chores.

Features such as flat-panel displays and, for limited applications, low cost speech recognition systems are also beginning to enhance terminals. In the fourth special report article, display technologies such as ac plasma and electroluminescence are being actively promoted as direct replacements for the ageless CRT in portable small-screen size applications. Attempts to remedy the age-old problem of developing a low cost speaker-independent speech recognizer may prove irrelevant when a device that uses a feature analysis algorithm appears on the market in an actual terminal.

Overall, the two most common peripherals to most all computer systems are not being ignored and may even one day develop into full-fledged, standalone computers.

Nicolas Mokhoff

Nicolas Mokhoff
Senior Editor



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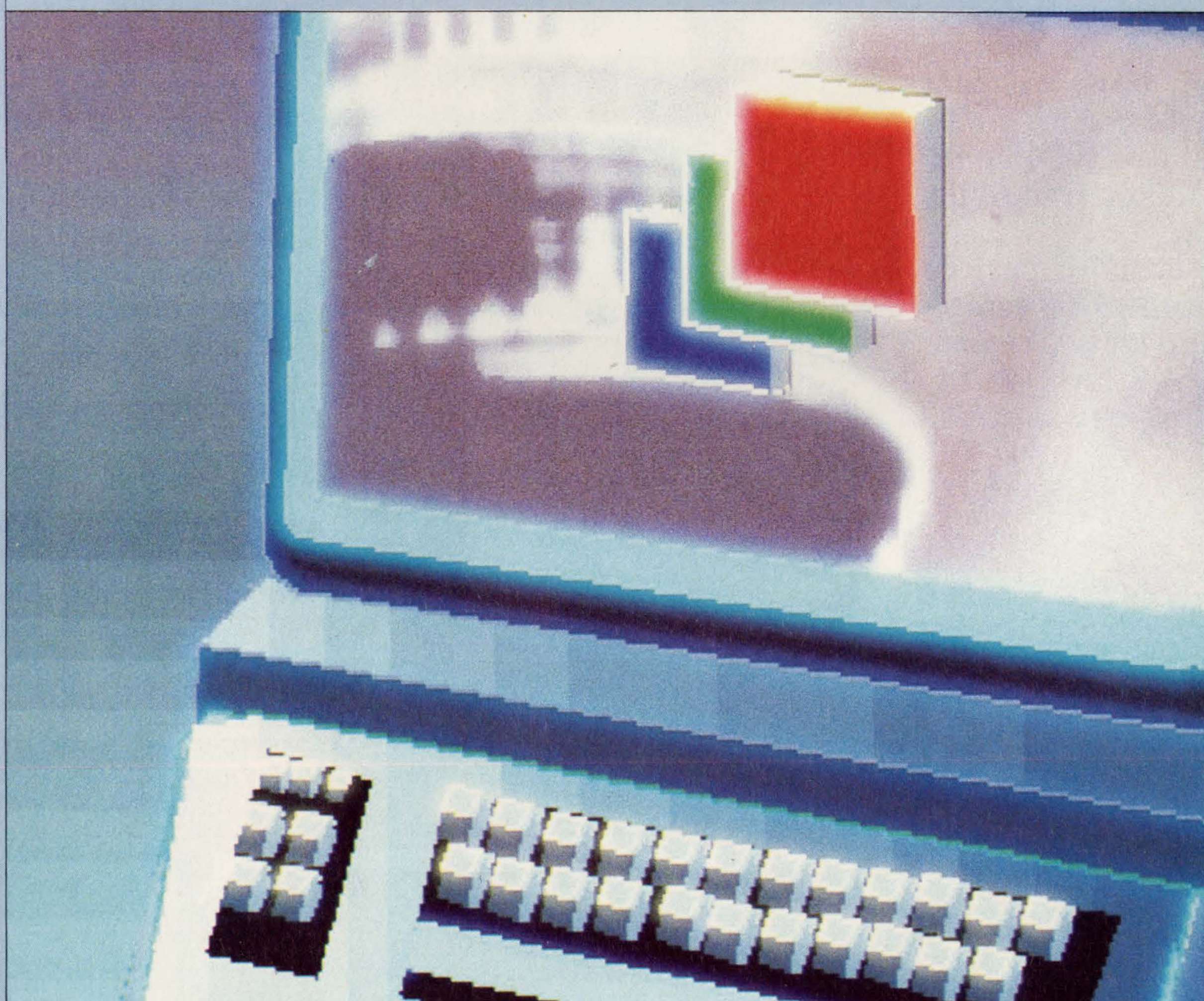

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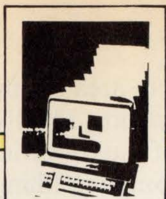
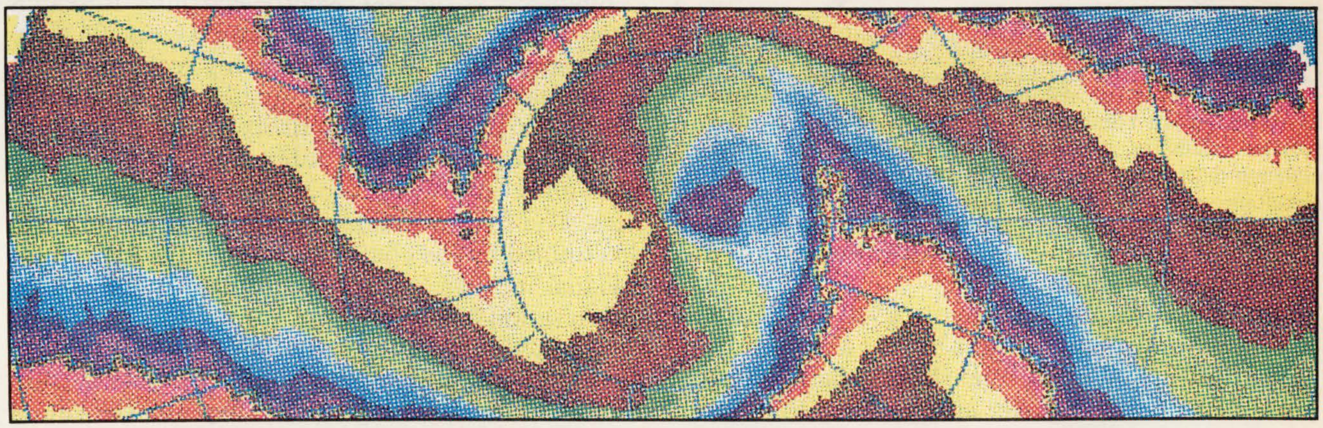


PRINTER TECHNOLOGY QUIETLY ADVANCES

Nonimpact printing methods vie for attention now that key characteristics like print quality, speed, and sound level rival those of impact printers.



by Nicolas Mokhoff, Senior Editor

The most common type of computer output is a hard copy. For the most part, printers of the last 20 years have been very obvious about generating a hardcopy output—they usually made a lot of noise doing so. While input devices and central processing units have made a smooth transition to the world of quiet electronics, printers have mostly remained in the electromechanical realm. The next couple of years should change that picture.

The age of the practical nonimpact, and thus "quiet," printer has finally arrived. Whether shooting a stream or drops of ink from a jet, bombarding electrons from a laser, applying heat from a platen, or depositing ions on a magnetic drum—all these printing methods resort to a nonimpact way of placing ink on paper. Nonimpact methods are currently at the threshold of complementing every conceivable computer system application, from the simple word processor character printer to the sophisticated data processing line and page printers.

Two technologies stand out as able to encompass the vast span of applications at a reasonable cost. Both ink-jet and thermal transfer have been talked about for years, but not until the last year have an onslaught of commercial products hit the market. And, according to some market analysts, they are about to give the long-standing bastion of printer technology—the dot matrix printer—a run for the money.

Interest in ink-jet printing technology has recently become feverish. From January 1975 through January 1983, over 500 U.S. patents relating to ink-jet technology were issued; of these over 100 were issued in 1982. Currently about 50 firms are active in ink-jet research and development. Clearly, considerable progress has been made since the first demonstration of an ink-jet oscillograph at Stanford University in the early '60s.

Both synchronous (continuous stream of ink) and asynchronous (drop-on-demand) ink-jet systems are finding applications. In synchronous

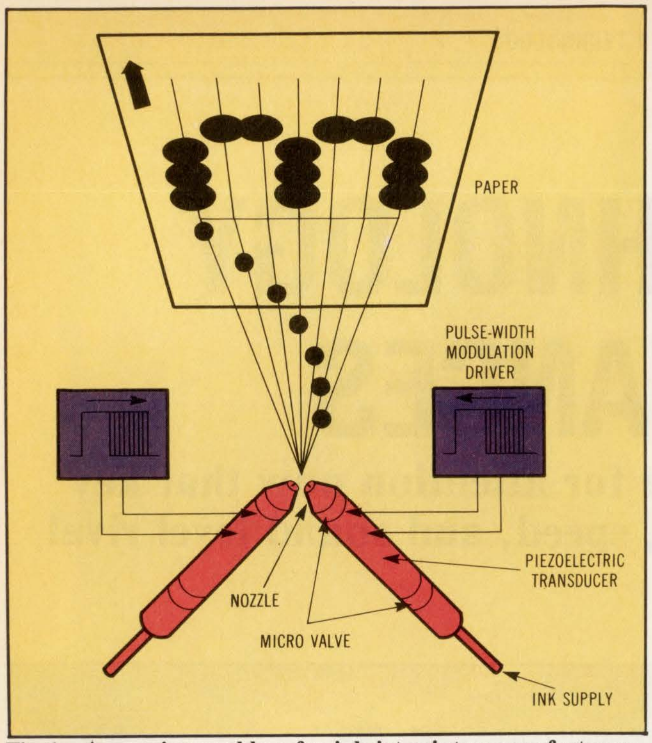


Fig 1 A growing problem for ink-jet printer manufacturers has been the low reliability of the ink jets themselves. To increase reliability, jet number must be reduced. NEC's drop collision deflection technique uses only two jets to emit two simultaneous drops which, upon colliding, combine at a point adjacent to the nozzle orifices. Micro valves apply a constant pressure on the ink; pulse-width modulation drivers control the direction of the ink drops.

design, the exiting ink droplet is given an electrical charge proportional to plates having a fixed potential difference. When no mark is to be made, the ink is deflected to a gutter and returned to a reservoir. A line of characters can be printed by moving the printhead along the width of the page. Another approach with a continuous stream of ink is the use of a multiple nozzle printhead, where charged droplets are deflected to the gutter and uncharged droplets ink the paper at fixed positions on a character matrix.

In drop-on-demand designs, both single and multiple heads can be used. The usual configuration of a drop-on-demand printhead is an ink reservoir, a deformable chamber, and a nozzle. The system designer must choose stable, nontoxic inks that will not encrust the nozzle (due to drying, mold formation, etc) and maintain appropriate wetting, drying, and spreading properties. Equally important is the choice of a paper matched to the inks and to the application.

Although ink-jet printers constitute only 10% of the dollar volume of nonimpact printers, there is reason for optimism about the growth of this technology. Market analysts have predicted that of the various nonimpact printing technologies, small electrophotographic and ink-jet printers will experience the most rapid growth through 1986. Another source pointed out that ink-jet printing is likely to be the major marketing growth area for the next 20 years in certain special applications. Finally, in considering the best combination of the following characteristics—line and edge definition, area filling, color accuracy, and copy speed—a Massachusetts Institute of Technology study found ink-jet technology to be the best choice for color graphics.

Japanese ink jets

Japanese efforts in placing reliable and low cost ink-jet printers on the market are especially intensive. They are exploring color printing technology beyond character reproduction to full facsimile of color photographs. Companies such as Nippon Electric Co (NEC), Hitachi, Sanyo, Canon, and Fujitsu have major ongoing programs to reduce the nozzles down to a minimum number for high quality and improved printer reliability. Multiple nozzles are usually used to maintain continuous pressure on the ink emanating onto the paper.

Engineers at the NEC Microelectronics Research Laboratories in Kawasaki, Japan developed a drop collision deflection ink-jet printing technique (Fig 1) that uses just one pair of single nozzle pressure-pulsed ink-jet heads. Two drops emitted from the two independent nozzles collide and combine with each other at a point adjacent to the nozzle orifices. The flying direction of the combined drop is determined by the combined momentum of the individual incidence drops, according to the law of conservation of momentum.

Pressure-pulsed ink-jet heads, having two 1-way micromechanical valves, are used in the drop collision deflection printing head. They are well suited for drop momentum control because of their high operational frequency and wide-drop volume variation characteristics.

The printing head is composed of a pair of pressure-pulsed ink-jet heads mounted at a fixed angle, one on either side of an ink chamber, where a piezoelectric transducer is used. The forward direction of both valves tends toward the nozzle orifice. Pumping effect due to joint operation among the piezoelectric transducer and the two valves not only causes steady drop ejection, but also a forced ink supply.

A pair of taper nozzles are used to set the drop collision point adjacent to the nozzle orifices. At the taper nozzle end, wall thickness is less than 10 μm. This effectively permits constant and stable drop ejection.

In general, a deflection type head provides better control over dot size when generating dot matrix characters. Drop collision deflection is characterized, in addition to the above, by a large deflection angle with small deflection error. This makes it possible to shorten the gap between the deflection head and the paper. Also, a lower voltage may be used than that in the electrostatic deflection system.

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CIRCLE 74

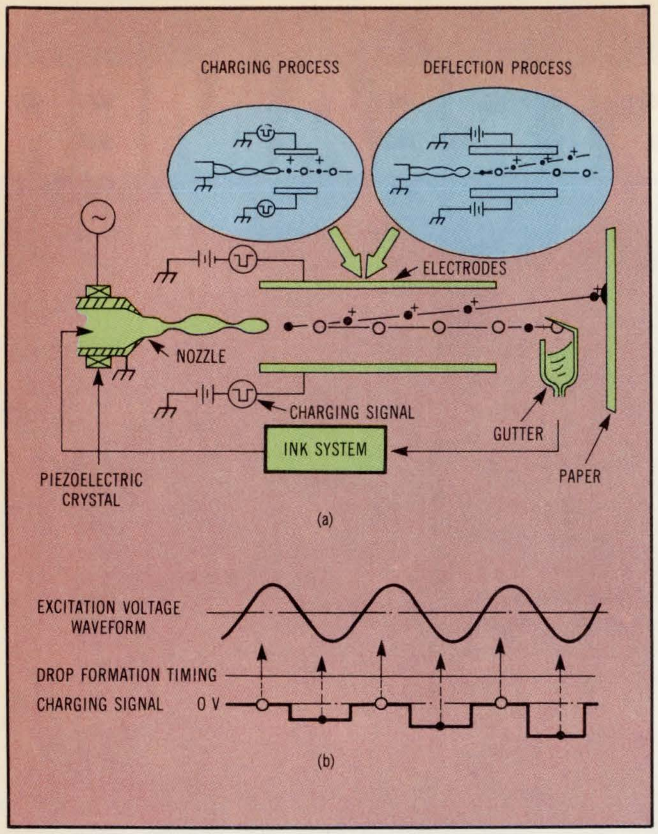

Fig 2 Hitachi's microdot printing technique controls the dot's size and shape by having the ejected ink stream pass from the nozzle between two electrodes used as deflection plates (a). Dot size is controlled by applying a variable excitation voltage that stabilizes the formation of an optimal dot pattern (b). Microdots alternate with large drops, and charged microdots are deflected to the paper while uncharged drops fall into the gutter.

NEC expects to generate over 100-char/s printing speed for 9- x 7-dot matrix high quality characters. This performance is suitable for such a small-sized, low priced printer as a peripheral device for personal or small business computers. Engineers at Hitachi's Research Laboratory of Ibaraki, Japan, meanwhile, have developed two high resolution color printers using a microdot ink-jet printing system. One printer prints 30 pages of color pictures per hour with a dot density of 400 dots/in and the other prints 10 pages per hour with 1000 dots/in.

What's a microdot?

In the microdot ink-jet printing method, only microdots, which are small droplets between large drops, are used for printing (Fig 2). Pressurized ink is pushed through a narrow nozzle and forms a continuous ink-jet stream. When a synchronization signal is applied through piezoelectric crystals, the ink jet breaks into a well-defined stream of drops. Change in ink pressure and amplitude of the applied voltage gives rise to small droplets, called microdots or satellites, between large drops. Only these microdots are used for printing. A charge is applied to the microdots electrostatically by small electrodes, which are also used as deflection plates. Charged microdots are steered upwards as soon as they are charged, and they hit the paper to form pictures or characters. Uncharged drops move straight into a gutter to be recirculated to the nozzle.

The diameter of microdots ejected from the 65-μm diameter nozzle with an oscillator frequency of 124 kHz is approximately 40 μm, while the diameter of large drops is approximately 120 μm. Dot density of printed pictures is 400 dots/in. When the 30-μm diameter nozzle is used with a 245-kHz frequency, the dot density is 1000 dots/in.

Stable generation and charging of microdots is controlled by voltage amplitude applied to the nozzle. A microcomputer-based automatic microdot generation control system has a drop sensor, a control circuit that controls a test signal generator, and a variable voltage circuit for excitation. Since only appropriately charged microdots pass through the drop sensor, it is possible to find proper conditions for microdot generation by changing the excitation voltage value while charging microdots with a predetermined test signal. This process is repeated until an optimal microdot generation range is obtained, where microdots and large drops are formed alternately with roughly the same distance between them.

The microdot ink-jet printers can be used not only for copying color pictures, but also for

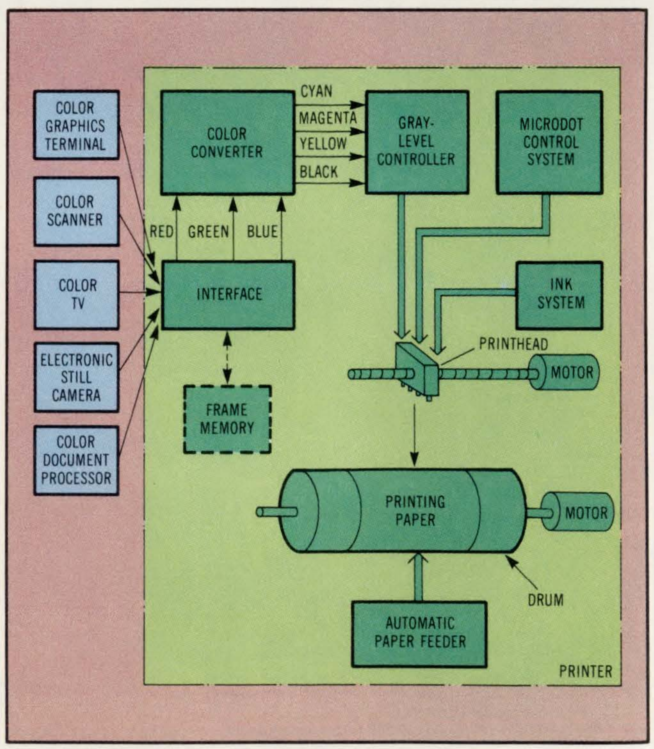

Fig 3 Hitachi's full-color printing unit can accept color information from many different sources. A frame memory is used to retain data from a video source for reproduction. Four ink jets (cyan, magenta, yellow, and black) move horizontally across the paper as it rotates on the drum.

obtaining hard copies of images on color TVs, color scanners, color cathode ray tubes (CRTs), etc. These full-color printers are best suited as hard-copy output equipment for reproduction of images from high resolution color scanners. The quality of the print from the 1000-dot/in printer comes close to that of a 35-mm photograph.

Information in terms of three primary colors (red, green, and blue) is input from various color input devices and fed into the full-color printer through an interface (Fig 3). Necessary data for reproduction are stored in a frame memory. Through a color converter, signals in the additive primary colors are converted into corresponding signals in three primary colors of ink (cyan, magenta, and yellow) and black. Halftone is controlled by a gray-level controller to give 16, 32, and 64 gray levels. In order to charge microdots generated from respective nozzles, signals for four colors from the gray-level controller are transmitted to the respective electrodes mounted on the printhead. An automatic paper feeder places the printing paper on a drum. Moving the printhead horizontally while rotating the drum produces a high resolution, full-color print (Fig 4).

A similar minute-dot, high resolution printing mechanism has been developed by Sanyo Electric Co Ltd of Osaka, Japan. This drop-on-demand printer uses a metal diaphragm-type ink head and a novel nozzle guard system that overcomes the three main obstacles to an effective drop-on-demand ink-jet printer: clogging of the nozzle due to dryness; accumulation of dirt around the nozzle; and defective pressurization because of bubbles.

It's all in the nozzle

In Sanyo's nozzle guard system, the small cell is filled outside the nozzle with ink and immerses the nozzle in ink when printing stops (Fig 5). Consequently, the nozzle cannot be clogged by dry ink, when printing stops. At the same time, as the ink is fed into the small ink cell through the nozzle, the dirt around the nozzle is melted and bubbles in the head are discharged.

This nozzle guard system with an outer ink cell allows high resolution printing of 12 dots/mm by using minute dots. To achieve the highest scanning accuracy, a drum-type scanning mechanism is applied to the printer. Because each minute dot cannot be seen in high resolution color printing, smooth graduation is obtained by controlling the dot density by a systematic dither method. Also, image data processing techniques such as the independent dither matrix, density conversion, and black signal processing improve the printing quality.

Ongoing research for improving print quality has recently focused on the way the ink drop in ink-jet printers is formed and subsequently ejected onto the paper. Researchers at the Fujitsu Laboratories Ltd of Kawasaki, Japan worked on developing optimum conditions for a stable droplet ejection.

Fig 4 A 1000-dot/in resolution is possible with Hitachi's ink-jet printer using a nozzle with a 30-μm diameter. Printed dot size is 35 μm on this unit, which allows print quality to approach that of a 35-mm photograph.

They investigated the characteristics of droplet ejection using a typical ejection unit with a cylindrical nozzle installed on a multilayer head. The droplet ejection process consists of the following phases: droplet formation; meniscus retraction; refill, in which the meniscus moves from the maximum retracted position to the outer end of the nozzle; and settling, in which meniscus vibration approaches equilibrium enough for the next droplet to be ejected with an acceptable droplet velocity change. Fujitsu engineers observed the following optimum conditions for stable droplet ejection: First, in terms of the droplet formation, an ideal droplet would be one without a satellite droplet and with a thread-like ink mist, and one that could absorb air bubbles. Second, the meniscus retraction should be kept within the nozzle. Also, in terms of optimal head dimensions and ink viscosity, Fujitsu engineers found that droplet ejection at higher frequencies can be achieved by shortening the nozzle while keeping meniscus retraction within the nozzle and maintaining a high viscosity level.

Ink-paper relations

An increasing number of available color display terminals are driving the demand for color hard-copy devices. The reasoning is that if one can see a color display on a CRT, one should also be able to obtain a good quality color hard copy of the display's contents. Ink-jet technology shows great promise for rapidly producing high quality, low cost, color hard copies. To this end, Tektronix (Beaverton, Ore) researchers are investigating the ink and media interaction to learn as much as possible about the requirements for ink-jet color

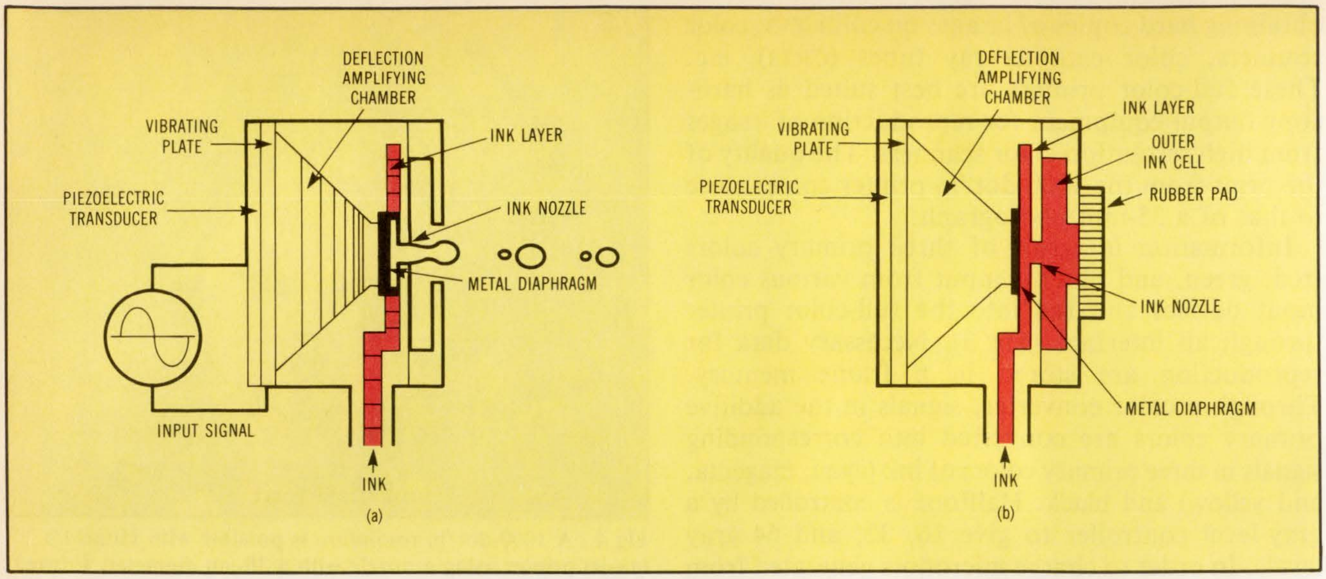

Fig 5 A drop-on-demand printing system developed by Sanyo Electric uses a metal diaphragm to shield the outer ink cell, which is constantly filled with ink (a). This keeps the nozzle immersed in ink in the standby condition, thereby keeping the nozzle from clogging (b). When an input signal is applied, minute drops are generated that print a copy at 12 dots/mm.

quality printing. They chose to use the air-assisted, ink-on-demand ink-jet for their research.

Tektronix researchers took a very scientific approach to their work. Their experimental hardware dictated the rheology requirements for the ink used in the system. Narrowly defined ink properties were viscosity, surface tension, and specific gravity. In order for the ink to have those specifications and be nontoxic and nonflammable too, water became the natural choice as the main solvent. The small ink-jet orifice restricted the choice of colorants to those water-soluble dyes classed by the Colour Index as acid, base, direct and, in some cases, reactive.

Because of the way in which color is generated in a subtractive 3-color system, the subtractive primaries—cyan, magenta, and yellow—must be used to obtain the largest color gamut possible. A separate fourth jet printed black, instead of generating black by combining all three primary inks.

Color science likewise dictates requirements of the receptor (ie, the printing paper). Adding a colorant into a light-diffusing medium, such as a sheet of paper, reduces the effective absorbing strength of the colorant. In a transparent film, light passes through the complete color layer. However, in a light-absorbing and light-scattering material such as paper, the scattering property causes part of the entering light to be re-emitted before it has passed through the full depth of the absorber—hence, the reduced coloring strength. The ideal situation would be to put all the colorant in a vanishingly thin layer right at the paper surface. That is close to what is achieved in normal printing processes and is the reason why those processes are able to produce deeply saturated colors. In ink-jet printing, the ink must be very fluid for the jet to work.

Thus, if smearing and running of the ink is to be prevented, the receptor must rapidly absorb all of the ejected ink, which most likely means penetration of the ink well into the bulk of the substrate. From that point of view, the perfect ink-jet receptor would be a blotter with a coating that retains the colorant right at the surface, yet allows the solvent to be absorbed into the substrate as fast as the ink is applied. The ideal coating would be transparent, so that no scattering of incident light occurs in the colorant layer.

Using different coatings

Tektronix engineers identified certain coated papers as working best with the quantities and type of inks put down by their color printer. Coatings appear to behave much the same as a chromatography column. Dyes used in their inks can contain either anionic sulfonic acid groups or cationic sites. Upon contacting the ionic materials of the coating layer, they are rapidly locked onto the surface by ionic interactions, while the remaining ink solvent is rapidly eluted down into the substrate.

Company researchers concluded that good quality hard copy by ink-jet printing requires rapid absorption of the ink solvent into the paper. But, the colorant must be retained on or near the paper surface. In all cases, some degree of lateral migration of the ink drop in the receptor will occur. The extent of that migration must be matched with the resolution of the ink-jet printer to produce uniform solid fill. Uniformity of that migration is related to surface smoothness and ink absorptivity of the media.

Also, researchers found that the lightfastness of an image is not solely determined by the colorant. Continued work is needed to identify dye and paper combinations that are even more lightfast, without compromising the largest color gamut obtainable—with particular emphasis in the area of a magenta primary. Tektronix engineers call for some industry-wide standards on lightfastness that would be very helpful in guiding such research.

As the demand for color hard copy approaches that obtained from photographic equipment, and as high resolution computer graphics become more commonplace, ink-jet technology will be the cost-effective solution capable of such quality. At the same time as the required number of dots per unit area for photographic quality will increase considerably, the corresponding amount of ink applied to the paper surface will most likely remain about the same. This will mean that the volume of ink per drop will have to be considerably reduced. The real goal then will be to produce a practical and reliable ink-jet that is capable of rapidly ejecting uniformly small drops.

The pulse that shoots ink

Meanwhile, in the laboratories of IBM (San Jose, Calif) researchers are studying the electrical signal's effect on the drop quantity needed for an effective print. As previous examples in drop-on-demand ink-jet printing have shown, a voltage pulse is applied to a piezoelectric transducer for each drop ejected at the nozzle exit. Past research maintained that this voltage signal should be a pulse with a short rise time, followed by a slow decay to zero to allow refill of the nozzle prior to the ejection of the next drop. More recently, a more complex voltage signal was investigated that was characterized by a sharp initial rise, a subsequent slow decay, and a secondary rise to an intermediate level prior to reaching zero.

IBM researchers studied the dependence of the drop formation process on the characteristics of the voltage pulse, such as pulse width, amplitude, and shape. The voltage pulse applied to the transducer causes a pressure pulse in the fluid chamber, and this pressure pulse, in turn, causes the drop to form at the meniscus. Thus, the shape of the voltage pulse should significantly influence the drop formation process. Using a Motorola 68000- based signal generator, IBM engineers observed that pulse width and amplitude of the voltage pulse significantly influence the drop volume and frequency response, almost independent of pulse shape.

Their experimental setup consisted of a signal generator to drive the drop-on-demand drop generator, a long working distance microscope, and a low light level TV-camera with monitor. A strobe light or a light emitting diode furnished the light and monitored the drops. The results of the experiments confirmed that the pressure pulse that ejects the drop at the nozzle is the integrated effect of the distributed local pressure waves in both space and time and that this integrated pressure pulse is similar in all cases.

For more than 10 years, IBM was one of the pioneers in ink-jet technology. The company, however, has made headway in other printing technologies as well. For instance, its West German subsidiary has recently developed a very high quality black and white printer that uses an electro-erosion printing technology. The printer creates composed text and graphics on a special aluminized paper with a 600 x 600 picture elements-per-inch resolution. The 4250 is aimed at end users and is well suited for office environments because of its inherent quietness.

In the electro-erosion process, text and line graphics are created by passing an electric current into aluminized paper, thus eroding the metal part of the paper where printing is done. The extremely crisp image can be used as a camera-ready master page or inserted into a copier or direct-plate maker. The 4250 can reproduce up to 22 typeface families in various styles and sizes ranging from 6 to 72 points. Control electronics can remotely address all 600 points in both directions, enabling an electronic layout of pages using both text and line graphics. The specialized paper cost is about $0.12/ft, according to IBM. The printer sells for $21,000.

While IBM is not ready to introduce a commercial ink-jet printer, many other companies have done so in the last year. Besides Tektronix, there is Xerox's Diablo Systems Series C, Exxon's 965, Siemens' Printacolor TC1040, Konika's JM241, Canon's A1210, and a host of others that are in their development stage. The quality of printouts varies between machines, depending upon many factors: the number of jets used for resolution, the print speed, and the number of fonts available. Comparing these printer characteristics is not very useful since no two printers have the same elements. Thus, true comparison becomes an exercise in specsmanship.

Examples of companies placing their best foot forward are the print speed specifications for the Xerox (Hayward, Calif) Diablo Series C color printer and that for the Printacolor (Norcross, Ga) TC1040. Diablo specifies 20 chars/s (10 pitch) at either unidirectional or bidirectional printing. Printacolor TC1040 specifies the printing speed as being able to generate a 512 x 512 image in less than 1 min. Now it's your turn to translate.

Similar considerations must be kept in mind for printers using thermal transfer technology—the other main nonimpact contender. Probably to no one's surprise, most recent thermal transfer research has been carried on in Japan. Many products have appeared on the market there during the last year or two and more recently have been introduced in the United States. A major reason for the strong effort in Japan is that the Japanese language lends itself better to a facsimile-type mechanism of printing. Much of the thermal transfer work was first used in facsimile equipment. The companies involved include Nippon Telephone and Telegraph Corp (NTT) of Yokosuka, Japan; Oki Electric Industry Co, Ltd of Tokyo; and Toshiba Corp of Kawasaki. The research of these companies has resulted in patents, and, in some cases, products. Olivetti & Co of Ivrea, Italy and IBM have also been granted thermal transfer patents.

Thermal transfer is here to stay

In the late 1970s, Japanese researchers at NTT recounted the advantages of silence, simplicity, and high reliability of thermal paper printing, but also noted that thermal paper results are subject to fading and color change. They studied ink-transfer imaging to obtain plain paper prints without losing the advantages of thermal paper printing. Two processes were found to be satisfactory.

With both processes, imaging is accomplished by using a thermal head to heat and melt an ink-coated base. When the ink is melted, it is transferred to plain paper, forming an image. The difference between the two processes is in the type of base with which the ink is coated. The ink-film method uses a thin film as the base, while the ink-thermal paper method uses thermal paper as the base. With this method, thermal paper printing is achieved on the top layer and thermal ink-transfer copying on the plain paper beneath.

In operation, a film or a sheet of thermal paper that is coated with ink on the underside is heated by the thermal printhead. The heat is transferred through the film or thermal paper to the ink, which melts—lowering its viscosity and thereby letting it flow into the paper. Usually a thermal printhead is of a dot matrix type and the characters are formed out of dot configurations.

NTT engineers have researched the importance of the melting point and viscosity of an ink in ink-transfer efficiency and in print quality. A typical ink in this type of printer has a melting point of 60 °C and a viscosity of 50 centipoise (cp) at 100 °C. The ink is heated to above its melting point so that it will penetrate the paper, which is pressed against the ink layer.

Last year, engineers from Oki Electric Industry Co, Ltd developed a new printing unit that, according to Oki, improves upon the thermal ink-transfer method developed by NTT. According to Oki, the NTT method has a disadvantage. Solid ink on the film is used up by a single printing, and the ink film tends to become wrinkled by ink-film treatment in the facsimile and printer.

With Oki's printing unit, the return roller's built-in heater melts the solid ink (Fig 6). A thermo-detector senses the surface of the ink roller while a microcomputer adjusts the airflow from the fan and the heating power of the roller. In this manner, the printer uniformly and continuously forms a thin layer on the platen roller surface. It then solidifies the ink layer at an optimal temperature before the transfer. As the thermal head is pressed against the roller, the heat is selectively applied to the dotted-line-type elements from the rear paper surface. Ink is then resupplied to the part of the ink layer where ink has been depleted through transfer.

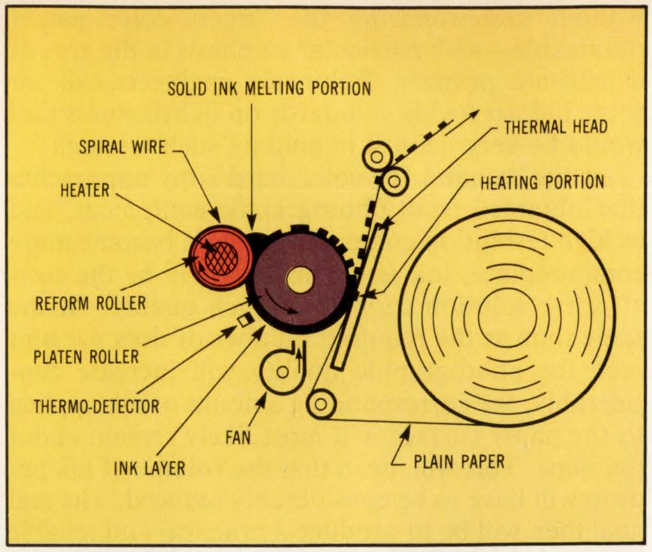

Fig 6 A breakthrough in thermal transfer printers by Oki Electric in 1981 was to use a second roller with an internal heater to melt the ink, thereby applying a uniformly thin layer on the surface of the platen roller. A heat detector senses proper ink temperature, while a microcomputer adjusts for proper heat and airflow from the fan. The printer, however, requires specially treated paper.

Thermal transfer is accomplished by thermo-melting solid ink that has been coated on thin film onto a plain paper. This printing cost, however, is expensive because the ink-film can be used only once. More research by Oki engineers yielded better results this year. They developed a thermal ink-transfer printer that uses an ink-film repetitiously by reforming the ink layer on the film (Fig 7).

To reform is to repeat

The reformation unit consists of a reform roller and an ink bath. This reform roller has a built-in heater and a delicate spiral groove on the surface. The ink bath is a double structure that prevents heat loss.

The ink in the bath is melted by the heat of the reform roller. According to reform roller rotation, the melted ink is carried to the contact portion between the film and the reform roller. At this contact portion, the ink that remained on the film is melted again and mixed with the ink from the bath. A constant amount of melted ink is supplied onto the film through the grooves of the reform roller

surface. The supplied ink spreads out because of its wettability and forms a flat ink layer.

Oki experimentally confirmed that the ink-layer thickness is reduced to approximately one-half of the calculated value, because the reform roller must be pressed sufficiently hard against the film to supply a constant amount of the ink.

In the reforming process, the supplied ink is kept in a molten state in order to form the flat ink layer when the ink is spreading out on the film. Ink transfer occurs when the ink surface, in contact with the plain paper, has been melted. By using the thermal head, the ink is heated from behind the film. Therefore, the thinner film and the thinner ink layer decrease heat loss and increase print quality. Furthermore, the film requires heat resistivity due to its direct contact with the thermal head. In practice, 25-mm thick polyamide film is used.

Thus, Oki's printer has all the wanted characteristics of a thermal transfer-printer: plain paper print, no print fading, low cost, and high resolution. Applications of this printer may be found for word processor printers and office computer printers, according to Oki officials.

Commercial thermal transfer printers from Oki will directly compete with the impact printers produced by its American subsidiary, Okidata (Mt Laurel, NJ). This company is one of the leading suppliers of impact dot matrix printers. Its entire Microline product line is geared toward personal computer users.

Microline printers can be considered typical of those using the dot matrix impact technology—still the workhorse of all printer technologies. Lately, these printers have taken on an elegant and compact look, and have had design features incorporated that are specific to interfaces with Apples and IBM personal computers, and others (Fig 8). A typical specification sheet will read that 80 chars/s is the unidirectional printing speed, that it utilizes a full 96-character ASCII set with 80 columns for standard characters and 132 columns for condensed characters.

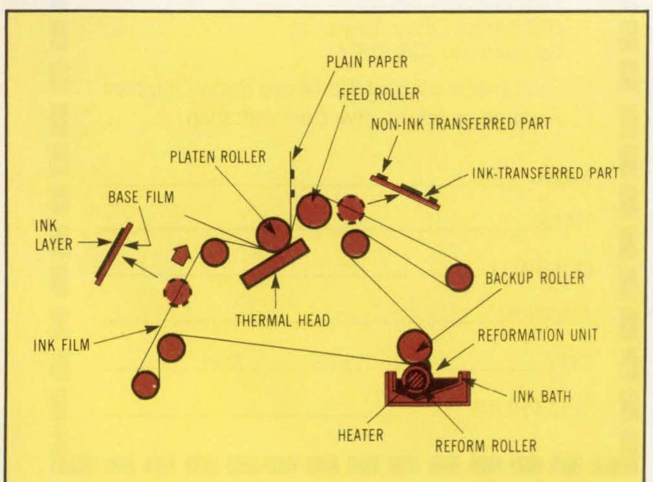

Fig 7 Oki's plain-paper thermal transfer printer uses an ink film in an endless loop, while the ink is selectively melted by heat elements of the thermal head and transferred to the paper. Ink remaining on the film is remelted in the ink bath by the reform roller, which again supplies a uniformly thin 5-μm ink layer on the film for the next cycle.

Fig 8 Most dot matrix and full-character impact printers have been packed with useful new features that make them more attractive to the office worker. Besides variable form lengths, speeds, and formats, the units are smaller and lighter due to increased electronics within. Okidata's microline, for example, allows downloading of full-custom character sets from the computer. This makes for faster and more versatile printing.

Good old impact printers

Okidata's ML-80 product line also features 64 block shapes for generating graphics, and can type various densities of lines/min depending on the number of characters/line. Oki's latest version (μ92) prints at 160 chars/s and has a density resolution of 13 x 17 dots. Users can also download formatted characters from a diskette to the printer. All these features are making the printers more accessible to the nonengineer.

For the most part, the state of this type of impact printing technology has not progressed much beyond the original designs. For letter-quality printing, users can now choose a daisy wheel printer, still considered less reliable than dot matrix. Their full-character impact mechanism, however, comes close to typewriter format quality and is again attractive to personal computer users for that reason.

The leader in this type of impact printer is Daisywriter, a division of Computers International of Los Angeles, Calif, whose model 2000 purports to print up to 500 pages in an average 8-h day. The printer is a Z80-based system that uses the computer-optimized printer interface and emulation system (COPIES) algorithm that provides protocol emulation for Diablo 630, Qume Sprint 9/11,

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CIRCLE 76

NEC 3500, 5500 and 7700 series, Centronics 737, and IBM PC printers. A built-in buffer memory of 16K bytes (48K bytes optional) allows computers to load up the buffer memory in less than a second and to print for up to an hour with an optional low cost sheet feeder or a tractor.

As in most modern printers, while printing, the host computer can be used for other operations. Clear buffer and reprint buffer commands can be controlled by the front panel or software. The buffer can be automatically reprinted up to 255 times by software control. Also, the full-screen display of a CRT can be instantly dumped directly to the printer with no handshaking required. Four interfaces are included in the Daisywriter 2000: Centronics 8-bit parallel; IEEE 488; RS-232-C; and 20-mA current loop.

Another typical feature in current full-character and high quality, dot matrix impact printers is the use of stepper motors for driving the printing mechanism, the paper feeder, and any other mechanical part. These motors are easier to control electronically and are made exact in responding to the printing cycle. In the Daisywriter printer, for instance, a linear stepping motor magnetically drives the carrier along a rugged stainless steel track. There are no cables, belts, wheels, or pulleys to fail, stretch, adjust, or malfunction. In addition, three control microprocessors reduce the complexity and number of mechanical parts.

Daisywriter 2000's modular construction consists of five units: platen, carrier, controller, power supply, and an interface-emulator-buffer memory board. Maintenance is made easy by just loosening two captive screws to remove the cover for quick onsite replacement of these modules. All cables between modules are terminated through connectors for quick disconnect. Fourteen print styles and 16 languages are available on printwheel cassettes pioneered by Daisywriter. The printer is manufactured by Computers International, which sells its units to original equipment manufacturers (OEMs). Daisywriter's printing mechanism has been in production nearly two years in Japan's Brother Industries' model EM-2 electronic typewriter.

On the dot matrix side, Epson America Inc of Torrance, Calif, the leading producer of that technology, sells its full product line to OEMs who have incorporated the printing mechanism in their equipment under many different labels.

Specification nightmares

Comparing impact printer features can be an even more frustrating exercise than comparing nonimpact printer features. For instance, Daisywriter engineers contend that specifications for printer speed in chars/s do not have a basis for standardization. Some printer's char/s specifications are based on unrealistic printing situations such as repetitive printing of the same character or ignoring of "white space" between characters. They usually do not account for computing or handshaking delays.

Thus, Daisywriter engineers express their printers' speed in chars/s, in what they deem accurate terms. Their rationale is that, because different applications will dictate the speed at which the printer will operate, it is important to qualify the white space between characters for each application (Fig 9).

As a consequence, the effective throughput speed in chars/s is defined as a function of the definitions for white space and the effective printing time. White space is defined as the space between the left and right actual printing margins from the beginning of the first line to the end of the last printed line, less the printed characters that the carrier moves through. This assumes that the carrier moves through the shortest possible path in both directions. Effective printing time is the time from the first computer-issued print command to the last character printed.

Clearly, objectively comparing printer manufacturers is hard to do, especially since the last count indicated 500 serial printers that print characters in terms of a dot matrix array. This does not include line printers, page printers, and printers incorporated as part of other equipment with special features.

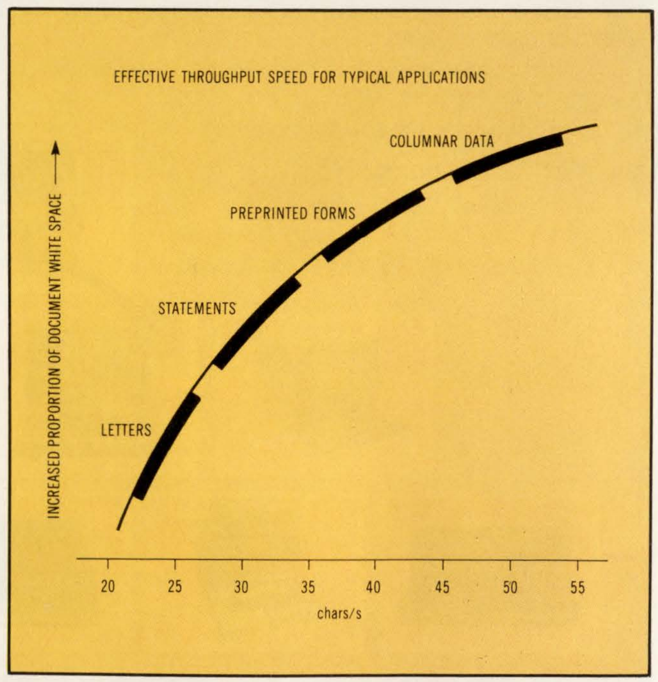

Fig 9 Users find themselves at a loss when interpreting printer specifications. Daisywriter, a leading manufacturer of full-character printers, makes what may be a subtle point about the different printout qualities according to individual applications. To them, a printer's speed should be chosen proportionate to the amount of white space that a user can tolerate on a document. Thus, comparable printer speed specifications should be viewed in terms of what kind of hard copy is generated, and how the user wants the printout to appear.

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CIRCLE 77

Comparing Printing Technologies							
Performance criteria	Impact	Ink jet	Electro-photographic	Dielectric	Electric discharge	Thermal (direct)	Thermal transfer
Speed	3	3	4	3 to 4	3 to 4	2	2
Hardware cost	4	3	1	2	3	3 to 4	3 to 4
Print quality (dot size, resolution, image density)	4 (FC) 2 to 3 (DM)	3	4	3	1	2	3
Acoustic noise level	1	4	3	3	3	4	3
Expendables cost	4	3	3	2	2	2	2 to 3
Paper requirement or tolerance	4	3	3	2	1	1	4
Reliability	3	2	2 to 3	3 to 4	3 to 4	3 to 4	?
Color potential	3	3 to 4	2	3	1	1 to 2	4

Key: 1—serious restriction or problem
2—often negative in some technological applications
3—normally seen as advantage in technological applications
4—considered major technological advantage

A reasonable objective comparison can be made, in very general terms, of competitive technologies. Datek Information Services, Inc of Newtonville, Mass, specializing in following the hardcopy market, has made a comparison in their most recent report on thermal transfer printing. (See the Table, "Comparing Printing Technologies.")

The Table was composed to assess the thermal transfer potential as a significant alternative technology that could "impact" current products or technologies. A 4-point rating system is admittedly arbitrarily used to cover the very wide range of products in any given technology grouping. Ratings are unweighted in that, in any given application, one or two characteristics may be critical, and others only helpful. In most any user survey, reliability is named as a top requirement. Because of a lack of data due to the novelty of thermal transfer printers, manufacturers have not yet included mean time between failures (MTBF) or mean time to repair (MTTR) specifications in their literature. Simplicity and high reliability are claimed, but only field experience can be used as a basis for hard reliability generalities.

Certain qualifications regarding the Table are in order. In general, thermal printing is inherently a slower printing technology than any of the others. It requires not only mechanical motion, but must also overcome the thermal inertia of both the resistive element in the head, and the ink-transfer substrate and ink. Although the range of product speeds in every technology varies widely, the fastest thermal and thermal transfer printers are much slower than the fastest printer products in each of the other technologies.

Progress has been rapid in all types of thermal printing, with speeds of the line printers approaching 6 pages/min. Faster thermal transfer printers are on the way. For instance, Oki Electric is placing the ink layer on a platen roller, and thus provides for continuous re-inking, which results in greater printing speed. A print rate of 400 lines/min, based on 85 chars/line, can be achieved using this method.

Thermals excel in color

In the area of color hardcopy printing, thermal transfer is in the lead. Thermal transfer computer printers might still be desirable even at slower speeds for applications in which other thermal transfer features, such as quietness, prove important.

For printers in a similar speed bracket, thermal transfer products can be relatively inexpensive. In color, although the resolution is the lowest at 100 dots/in, the Japanese Shinko CHC-33 has one of the fastest page speeds of any low cost color printer, yet is priced well below many others. In black and white serial, the print mechanisms of the Brother Industries' typewriter and Sony (Tokyo, Japan) Typecorder Printer contribute to the low price tags of these products. Costing well under $1000 (when made available) the Toshiba TH1000H looks like one of the more cost-effective, high resolution, plain paper printers. The Diablo EPM1 promises to be one of the more cost-effective printers in its speed range, especially considering the high density resolution (8 dots/mm or 1680 pixels/line). The OEM price is $2500.

Thermal transfer print quality ranks fairly high, although it cannot match the quality of the daisy wheel printer or the highest quality electrophotographic printers. However, a smaller dot size is possible than with even the best high resolution impact matrix printers. While conventional thermal print quality has improved over the past few years, a thermal transfer printer can offer inherently better print quality because it creates an actual inked image.

However, a thermal transfer printer has to handle more material than a conventional thermal and, thus, is noisier. The few noise specifications that exist for thermal transfer printers fall in the 50-dBa

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	ANALOG INPUT/OUTPUT
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MP8418-PGA-AO	15-channel Differential/31-channel single-ended input. Programmable Gain, 12-bit. 2-channel output, ± 10VDC
	ANALOG OUTPUT
MP8316-I	16-channel 0-20mA, 12-bit (common DAC).
MP8316-V	16-channel ± 10VDC, 12-bit (common DAC).
	SPECIAL PURPOSE INPUT
MP8430	16-channel RTD 3-wire (100 ohm or 1000 ohm).
	DISCRETE OPTICALLY ISOLATED INPUT
MP810	24-channel Dry-Contact Closure, 1.5mA Wetting Current at 24VDC.
	DISCRETE REED RELAY OUTPUT
MP802	32-channel Relay, 0.5A at 28VDC
	DISCRETE INPUT/OUTPUT
MP830-72	72-channel TTL levels. User configured in 8-channel increments of inputs or outputs.
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	ANALOG INPUT
MP7217	16-channel, single-ended, Fixed Gain, 12-bit.
	ANALOG INPUT/OUTPUT
MP7432-AO	32-channel Differential/64-channel single-ended inputs, Fixed Gain, 8-bit. 2-channel output, ± 10VDC, 8-bit (individual DACs).
	DISCRETE OPTICALLY ISOLATED INPUT
MP710	24-channel Dry Contact Closures, 1.5mA Wetting Current at 24VDC.
	DISCRETE REED RELAY OUTPUT
MP702	32-channel relay, 0.5A at 28VDC.
DEC LSI-11 COMPATIBLE	
LSI-11, -11/2, -11/23 PDP 11/03, 11/23	
	ANALOG INPUT
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ZILOG Z80 COMPATIBLE Z90, MCS	
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range for such devices as the Toshiba TN 5000 and TN 5300, and 55 dBa for the Diablo. These are in line with the noise levels specified for ink-jet printers and, thus, make thermal transfer a strong potential contender for printing in the office environment. In fact, quiet operation is one of the main reasons thermal transfer has been developed for use in a number of word processing printers in Japan. The relative quietness may be this technology's key attribute.

Expandable costs of thermals

Thermal printers require special papers and ribbons, which raise the expendables cost per page above that of other technologies. Seiko (Tokyo, Japan) claims a cost of about $0.25 for a 3-color page, which is mostly ribbon cost. This compares favorably with the Polaroid-based hard copiers, which can run several dollars/page, but may be a bit more than the ink-jet and impact color printers, which are the main competitors.

Ribbon costs for thermal printers are currently high. Because thermal transfer technology is very new and rapidly developing, ribbons are currently single-source supply items available only from the hardware manufacturer. The high price explains, in part, the great interest in thermal transfer within the ribbon industry.

In some black and white applications, thermal transfer printers can be used without a ribbon when coupled with conventional thermal paper. Such is the case with the Diablo EPM1. At current ribbon prices, thermal paper is significantly less expensive and offers an option when print quality and archivability are less important.

Multi-impression transfer ribbons are also being developed with ribbons that feature 5 to 10 times the number of impressions. This significantly lowers per-copy cost.

In general, impact printing is rated highest for the tolerance of the type of paper used, since almost any material that can be physically handled by the printer can be printed. In conventional applications, thermal transfer printing, like ink-jet printing, uses paper that the OEM usually supplies or recommends to achieve maximum print quality. Such paper increases the expendable per-copy costs and restricts applications. Paper need not be chemically treated or coated, which makes thermal transfer less restrictive than conventional thermal, dielectric, or electric discharge. But, judging from print samples, the paper required for optimum print quality is significantly more restrictive than for impact printing. It is also less akin to plain paper than what is normally required for ink-jet printers.

On the other hand, in some special applications, thermal transfer offers greater printing surface versatility than many other technologies. Color copiers can print directly onto transparency material for overhead projection. Advanced Color Technology of Chelmsford, Mass, however, has demonstrated similar capacity for its ink-jet printer, but it is not normally considered an application possible for ink-jet or most other printing technologies. One of the early applications of thermal transfer is imaging of cotton fabric tee shirts from an intermediary material imaged with thermal inks or toners containing sublimable dyes. Thermal transfers remain uniquely suited for this application.

Advanced Color Technology recently introduced their second-generation ink-jet printer, the ACT-II (Fig 10). Featuring the same capability that ACT-I has of printing directly on acetone for overhead projector transparencies, the new printer has 35% fewer parts and an impressive MTBF claim of 6000 hours.

It owes its claim to new enhancements in the ink-jet system that include automatic purging and waste ink disposal, simplifying operation; quick disconnect ink system components for ease of maintenance; and the introduction of peristaltic pumps that provide constant ink pressure and prevent ink supply contamination.

The ACT-II features a newly designed DuraPulse™ jet head with three integral secondary reservoirs that maintain constant pressure levels for reliable operation. The nozzle array of 12 piezoelectric crystal jets is arranged as four jets for each of the three primary ink colors. The automatic jet cleaning mechanism and the nonwater-based inks overcome the clogging problems of earlier ink jets,

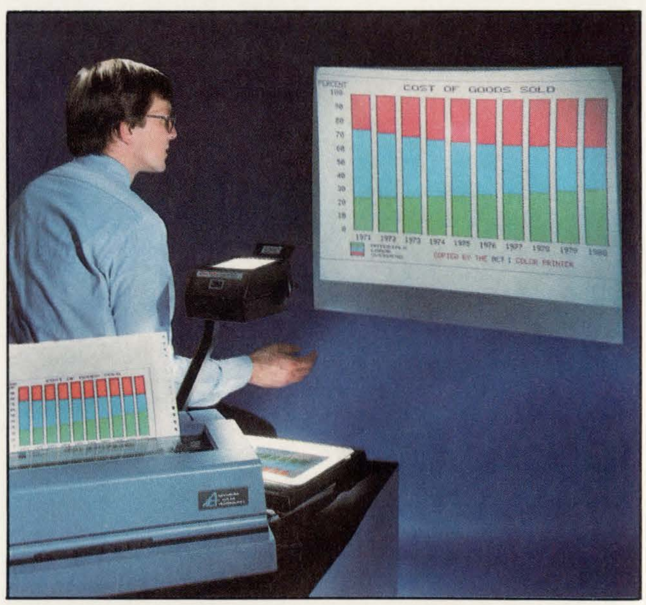

Fig 10 Traditional manual creation of color transparencies can take hours or days depending on complexity, and can cost $20 and up. With the increased use of color CRT displays, newer photographic techniques have allowed creation of color transparencies in 10 min at a cost of about $10. ACT claims its ink-jet printer can directly generate computer color graphics in transparency form in 90 s for only $1.75 each.

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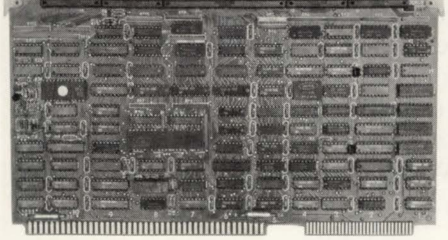

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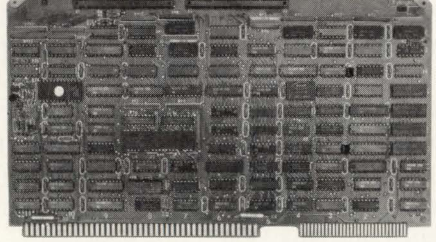
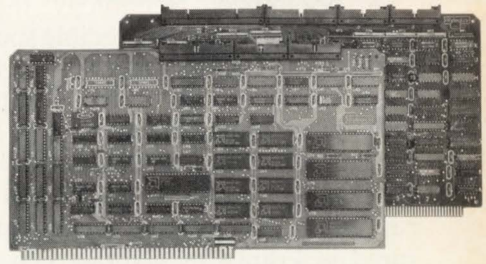


Xylogics 472 Multibus Tape Peripheral Controller.



Xylogics 440 Multibus Disk Peripheral Controller.

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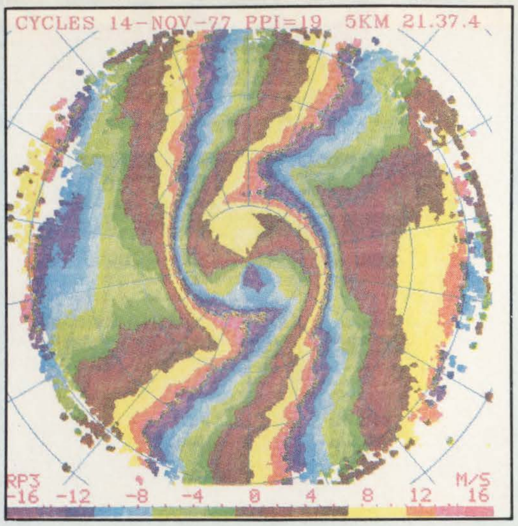

Fig 11 Dot matrix printers incorporate graphics and print at fairly high speeds. Trilog, for instance, has a Colorplot Model C-144 that was designed specifically for producing color hard copy from CRT displays with non-square aspect ratios and for applications requiring high resolution. (Plot: courtesy of the National Center for Atmospheric Research.)

says Advanced Technology. Its claims are backed with a limited 2-year warranty for both reliability and maintainability (MTTR of 15 min) for the DuraPulse ink-jet head. The ACT-II is priced at $6400 in single quantity. Ramtek Corp of Santa Clara, Calif has also introduced a printer for generating color overhead transparencies. Its 4111 Colorgraphics is a thermal printer, however, that uses a substractive color transfer process and sells for $6500. Printacolor's TC1040 also has a transparency printing capability.

Datek researchers believe that the potential of thermal transfer in the area of color is especially significant. Compared with impact color printers, transfer of wax-based inks from thermal film offers more vivid image quality than today's inked fabric ribbons offer. Such inks also tend to be more fade resistant than ink-jets inks. Spot size possible with thermal transfer seems to be smaller and more closely controlled than that of either ink-jet or impact printers.

Finally, the Sony Mavigraph thermal transfer printer, which can print directly from a video source, is specified to be able to vary the intensity of any given pixel, giving it "color greyscale" capability. This sets it apart from any of the other low cost printers, regardless of technology.

A nonimpact technology that produces high quality output at an incredible speed has been incorporated in the MP6090 from Cynthia Peripheral Corp of Sunnyvale, Calif. The printer operates at 6000 lines/min (88 pages/min) and uses perpendicular recording technology adopted from magnetic media concepts to print at a 240- x 240-dot resolution. The MP6090 was designed and manufactured in France by Cynthia's parent company, Cii Honeywell Bull, and will carry an OEM-quantity price tag of about $25,000. Three primary proprietary technologies are used in the printer: a magnetic drum, in conjunction with perpendicular recording heads, and a single-component magnetic toner.

Magnetically speaking

Magnetic recording heads record desired information on the magnetic drum, which rotates through the single-component toner. The toner is attracted to the magnetized regions on the drum; thus, the desired information is transferred to continuous fanfold paper.

According to Cynthia, the magnetic printing process offers a reduced parts count and higher reliability than other high speed printer technologies such as laser/electrophotography. For example, the MP6090's single-component toner eliminates the need for a closed loop process monitoring usually required by dual-component systems. In addition, the drum life is estimated at 10,000,000 pages versus 500,000 to 1,000,000 pages for most high speed laser/electrophotographic machines. Also, the required scheduled head cleaning and other preventive maintenance necessitate only 2 service calls/year versus 12 to 20 for competitive high performance, nonimpact printers.

Modular electronics in the MP6090 provide maximum flexibility for OEMs and system integrators via video interface electronics for such applications as graphics and image processing. A line printer emulation capability permits standard line printer formats, using multiple fonts in both landscape (horizontal) and portrait (vertical) directions. Interface electronics on the MP6090 support standard Dataproducts (Woodland Hills, Calif) protocols. Evaluation units will be available toward the end of this year.

Meanwhile, Dataproducts, a leader in high speed serial impact matrix printers, has assembled a

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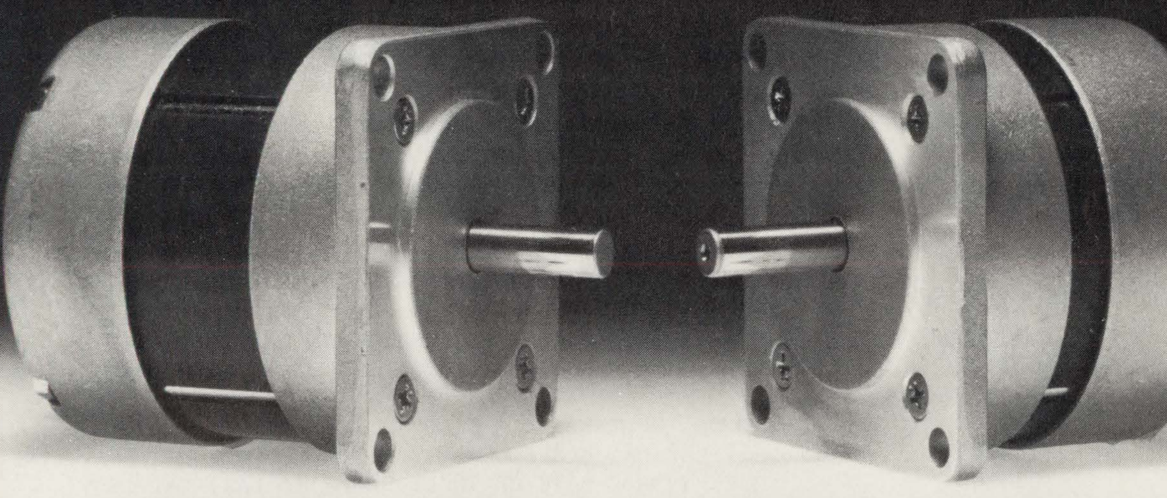

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CIRCLE 80

```
030600 PROCEDURE DIVISION.
030700
030800 A00-MAIN-LOGIC.
030900
031000     OPEN INPUT CALENDAR-PARMS.
031100     MOVE ZERO TO SPEC-POINTER.
031200
031300 A10-READ-BEG-END-PARMS.
031400
031500     READ CALENDAR-PARMS AT END
031600                         CLOSE CALENDAR-PARMS
031700                         GO TO A20-CHECK-CALENDAR-PARMS.
031800     DISPLAY "INPUT-PARMS ARE " INPUT-PARMS.
031900
032000     IF NOT (BEG-END OF INPUT-PARMS = "BEG" OR "END" OR "TOP")
032100         DISPLAY "RECORD MUST BEGIN WITH 'BEG', 'END' OR 'TOP'"
032200         GO TO A10-READ-BEG-END-PARMS.
032300
032400     IF BEG-END = "TOP"
032500         GO TO A15-CALENDAR-HEADINGS.
032600
032700     MOVE YYMMDD-DATE OF INPUT-PARMS TO FORMATED-DATE.
032800     PERFORM U00-DATE-VALIDATE THRU U30-EXIT.
032900     IF FORMATED-DATE = "ERROR"
033000         GO TO A10-READ-BEG-END-PARMS.
033100
033200     IF BEG-END OF INPUT-PARMS = "BEG"
033300         IF FIRST-CAL-DAY = SPACES
033400             MOVE YYMMDD-DATE OF INPUT-PARMS TO FIRST-CAL-DAY
033500             MOVE WEEK-DAY OF INPUT-PARMS TO BEGIN-WK-DAY
033600           ELSE
033700             DISPLAY "ONLY ONE BEGIN DATE CAN BE SPECIFIED"
033800             GO TO A10-READ-BEG-END-PARMS.
033900
034000     IF BEG-END OF INPUT-PARMS = "END"
034100         IF LAST-CAL-DAY = SPACES
034200             MOVE YYMMDD-DATE OF INPUT-PARMS TO LAST-CAL-DAY
034300           ELSE
034400             DISPLAY "ONLY ONE END DATE CAN BE SPECIFIED"
034500             GO TO A10-READ-BEG-END-PARMS.
034600
034700     GO TO A10-READ-BEG-END-PARMS.
034800
034900 A15-CALENDAR-HEADINGS.
035000
035100     MOVE INPUT-PARMS TO FIELD-HEADINGS.
035200     MOVE CHARSET-NUMBER OF FIELD-HEADINGS TO NUMBER-TEST.
035300     IF NOT (NUMBER-TEST > -1 AND NUMBER-TEST < 32)
035400         DISPLAY "CHARACTER SET FOR FIELD DATA INVALID"
035500
035600
035700
035800
035900
036000
036100
```

This page was produced with the 4800 Page Printer in the portrait printing format. When combined with prepunched 8½ x 11 fanfold paper, reports can be stored in standard 3-ring binder for easy access.

Fig 12 For high quality batch printing, laser units still excel. While these printers are still far too expensive for normal office use, some Japanese companies are researching low cost units that will use semiconductor technology. The printout shown here is from Datagraphix's 4800 laser printer which, in addition to this type of form, can print out in other condensed and expanded formats at 45 pages/min. IBM, Siemens, KEL Inc, and Xerox are leaders in laser printing.

special configuration of its 140-chars/s M100 model. The M100L can generate labels, bar codes, block letters, graphics, line drawings, and text in any combination from software commands. The company, like its competitor, Epson, designs and manufactures all of its line printer hammerbanks, matrix printheads, and daisy wheel hammers. Dataproducts also provides these components and full assemblies for OEM customers who then incorporate the units in their printers for special applications. Trilog, meanwhile, has distinguished itself as a provider of a dot matrix color printer/plotter that serves the CAD/CAM community and less specialized applications such as mapping and scientific/medical research (Fig 11).

A challenger to Cynthia Peripheral's magnetic printer is another 240- x 240-dot resolution nonimpact technology that has been incorporated in an ion-deposition printer from Southern Systems, Inc of Fort Lauderdale, Fla (see *Computer Design*, Dec 1982, p 62).

The technology was developed by Delphax Systems of Mississanga, Ontario, who sells it to OEMs for custom applications. A large selling point for the Southern System's Mercurion 1 is that it is plug compatible with all major mini and mainframe computers, and thus can replace an existing impact line printer for $60,000. That price, while steep for a 60-page, 5280-line/min printer, is close to half of that for laser xerographic systems—the luxury class of all printers.

Lasering to print

The bottom line of any printout is the quality of the print at high speed. Thus far, laser xerography comes closest to fulfilling this characteristic. Perhaps a printout from the latest laser printer from Datagraphix, Inc, a subsidiary of General Dynamics, San Diego, Calif, can illustrate the point (Fig 12). The 45-page/min printer provides the kind of quality output in the form of reports, correspondence, and documents. Preprinted forms can be replaced with electronic forms and memos, and electronic mail can be printed at lower cost and higher speed than conventional letter-quality printers on office copiers, claims Datagraphix.

Siemens ND3 laser printer has a multimode feature that allows printing at 5250 lines/min if the density one wishes is 6 lines/in, or 1000 lines/min at 8 lines/in, 10,500 lines/min at 12 lines/in, and 21,000 lines/min at 24 lines/in. The ND3 is huge and bulky, as are most laser printers, and is clearly intended only in large volume data processing applications. KEL, Inc (Woburn, Mass) also offers a laser printer. Its 8211 printer incorporates hardware and software interfaces to IBM mainframes or IBM-compatible computers. The printer also takes high quality plotting inputs from CalComp plot software at a 5.5-in/s speed.

As nonimpact printers start to make headway, dot matrix serial printer manufacturers have found new ways to trim their products to keep attracting a loyal customer following. Anadex, of Chatsworth, Calif, for instance, has attained new printing speeds by using an 18-needle printhead that consists of two vertical columns of nine needles each. Since the two columns of print needles are adjacent to each other, two identical columns of dots can be printed at one time. This doubles the printing speed of the conventional single column, 9-needle printhead.

Thus, the new DP-6500 data processing printer achieves speeds of 500 chars/s at 10 chars/in, putting it at the low end of the line printer speed range. For 132-column printing, the DP-6500's speed is over 200 lines/min. It sells for $2995.

Also, because dot matrix printers are notoriously noisy, it is surprising to note that Anadex's Silent/Scribe family of dot matrix printers sports the same noise level (55 dBa) that nonimpact printers specify. Anadex owes its low acoustic noise level, however, not to a quieter mechanism, but to a case design that contains special sound-dampening foam and a sound deflector at the paper exit.

Another feature with which impact printers are now endowed is the multimode capability. This allows producers of these printers to tout their products as suitable to both low volume, medium speed word processing and high volume, fast speed data processing applications. Thus, Anadex's DP9725A printer is advertised to produce multiple colors in four print quality modes that include near letter, correspondence, condensed, and data processing. This is achieved by operating in both single- and double-pass printing modes, which permit full color capabilities and multiquality characters.

All these extra features may entice impact printer followers. However, the bottom line for many users is a printer that can reliably yield a letter-quality copy at a minimum 1000-char/s speed, using a "noiseless" mechanism. Such a printer may sooner be developed using a nonimpact technology than an impact one.

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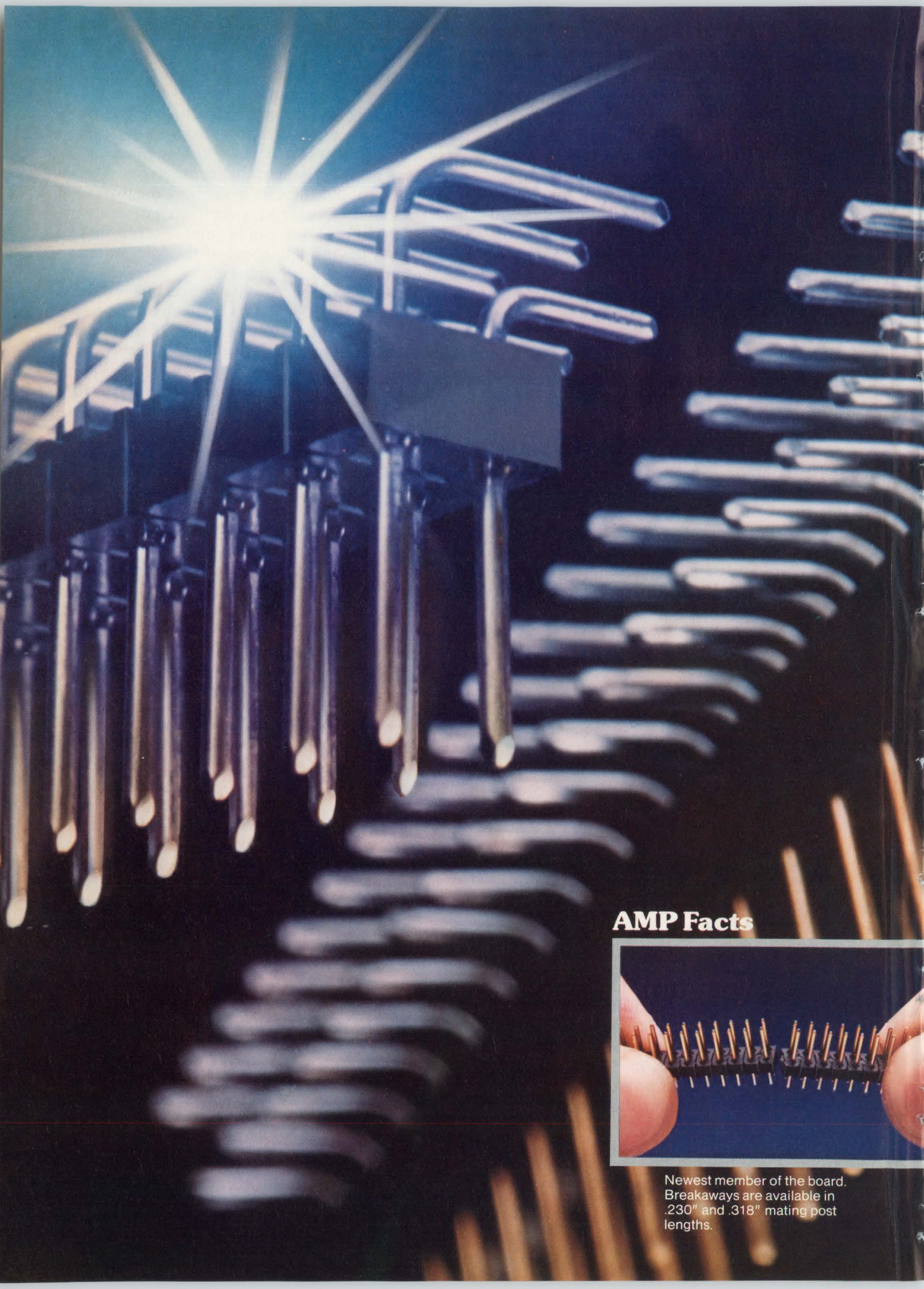

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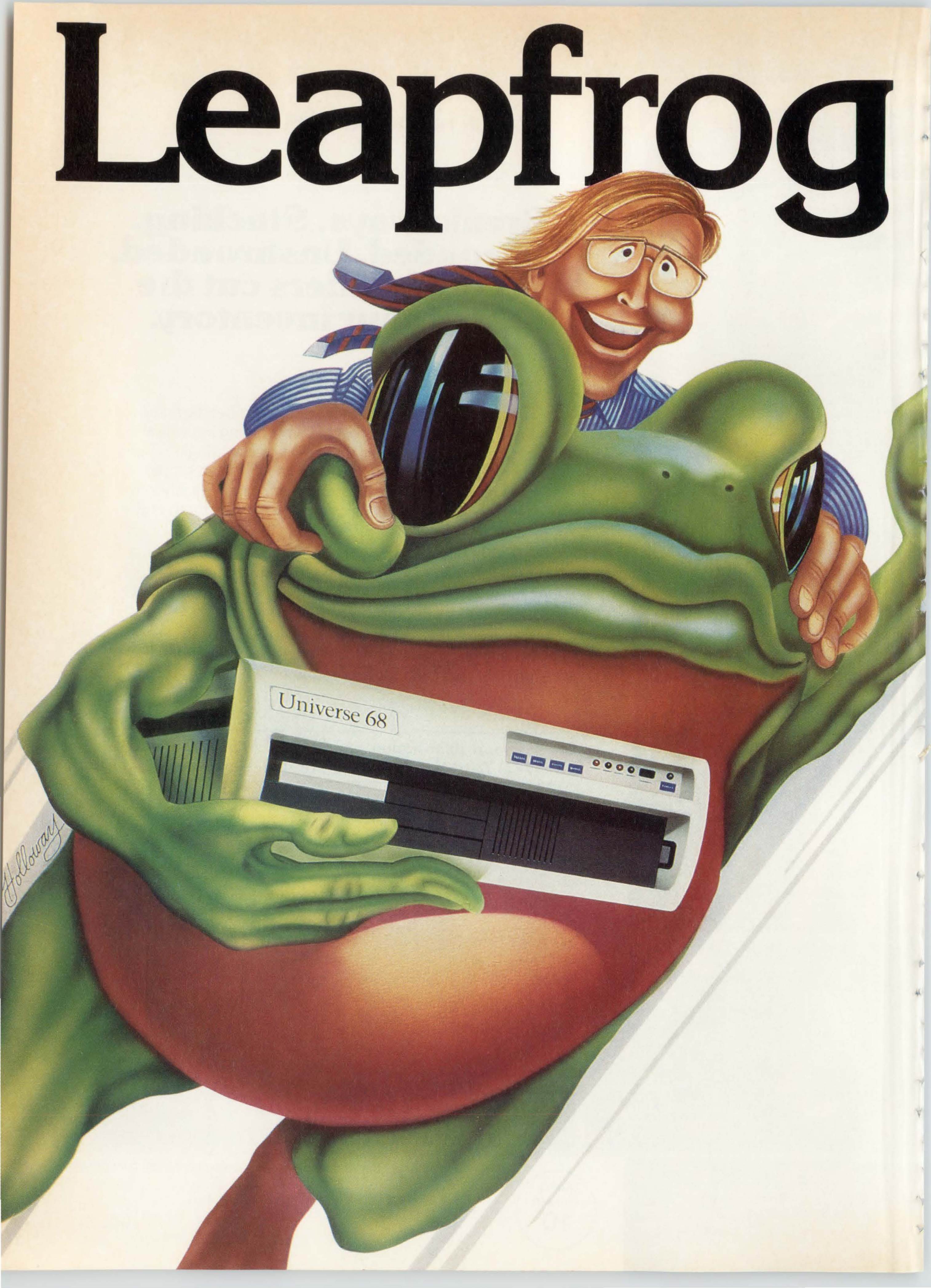
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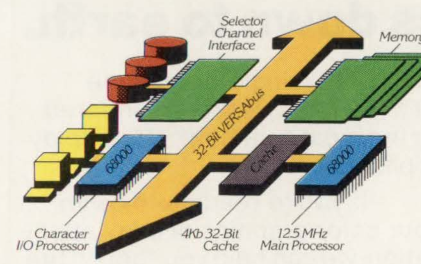

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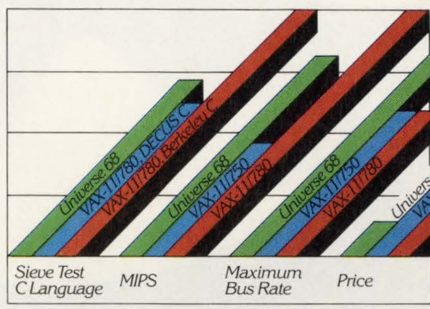

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CHIP SET GIVES A SMOOTH SCROLL IN CRT DISPLAYS

Two large scale integration chips and a read only memory font generator interface 16-bit processors with CRTs directly to control scrolling in multiple windows and to space characters proportionally.

by Steven Dines and Mohammad Maniar

Marrying state-of-the-art display technology and computational capability in today's terminal requires a large data handling capability. Features such as a noninterlace flicker-free frame refresh and a full-page graphics representation dictate high dot update rates in the 100-MHz range. This speed can only be handled by emitter coupled logic chips with all of their attendant problems. Similarly, embedded local editing intelligence places severe constraints on a terminal's microprocessor subsystem, which must efficiently handle such interactive tasks as insertions and deletions.

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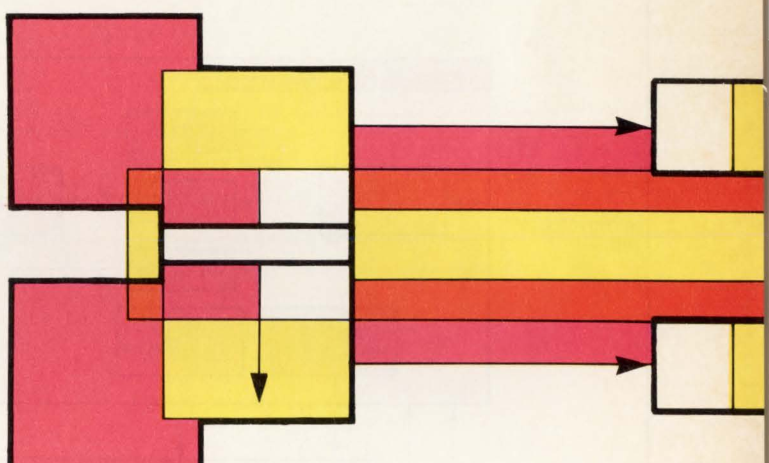
Mohammad Maniar is supervisor of MOS microprocessor design engineering at Advanced Micro Devices. He holds a BS in electrical engineering from NED Engineering College, Pakistan, and an MSEE from the University of California, Berkeley.



These and many other obstacles have been solved by a 2-chip cathode ray tube (CRT) controller set that combines the advantages of N-channel metal oxide semiconductor and bipolar technologies. The two chips, together with an offchip font generation circuit, form a complete CRT interface between the microprocessor bus and the monitor (Fig 1). In this application, the Am8052 CRT controller is used as a direct memory access (DMA) controller. This has two advantages: first, it eliminates a separate DMA controller, thereby keeping costs down and saving space in the CRT terminal. Second and more significant, the DMA channel on the CRT controller can be customized to facilitate the controller's editing functions. Thus, a font-control read only memory allows a full video subsystem to be built that matches display data formats with printed information.

The DMA channel is configured as a linked-list processor, which sets up the display data with minimal editing overhead. This channel fetches data into onboard buffers that store three rows of character information. Incorporating triple row buffers onchip solves a major impediment to a pleasant-looking display: it allows the user to scroll smoothly in a split-screen application, which has always been a major problem in screen formatting.

Parallel pixel data emerge from the font generator and are serialized by the CRT controller set's second chip, the Am8153. All clocks for the system are also generated here. These consist of a 100-MHz pixel or dot clock, and two subclocks, the Am8052 CLK1 bus clock and CLK2 character clock. Emitter coupled logic (ECL) outputs in the Am8153 obviate the need for peripheral ECL output devices. Thus, both analog and ECL video are output from the Am8153.

Smooth scrolling

Scroll has always been one of the main requirements of any display terminal. Usually data are moved on the screen on a character row by character row basis, which makes for poor viewing. In addition, using "hard" scroll to rapidly scan a document is prohibitive to use because the eye has a hard time following the staccato movement of the text.

Smooth scrolling allows the text to be scrolled gradually, scan line by scan line. Not only is this much more pleasing to the eye, but it also allows documents to be visually scanned very rapidly, in a manner similar to the way one scans a phone book for a particular entry. Implementing this scan line by scan line offset is fairly easy. The difficulty lies in holding part of the screen stationary while scrolling the remainder. The Am8052 supports both split screens (horizontal and vertical) and smooth scroll of a subscreen—a combination that has previously been impossible to implement economically. Window screens also create data structure problems since each scroll involves juggling large amounts of data. While this may be a difficult task for a local central processing unit (CPU), the Am8052 CRT controller integrated circuit (IC) fetches all its refresh data by means of a linked-list data structure.

In this structure, a top-of-page register contains the 24-bit memory address of the first component in the list, called the main definition block (MDB). The MDB, in turn, points to a sequence of row

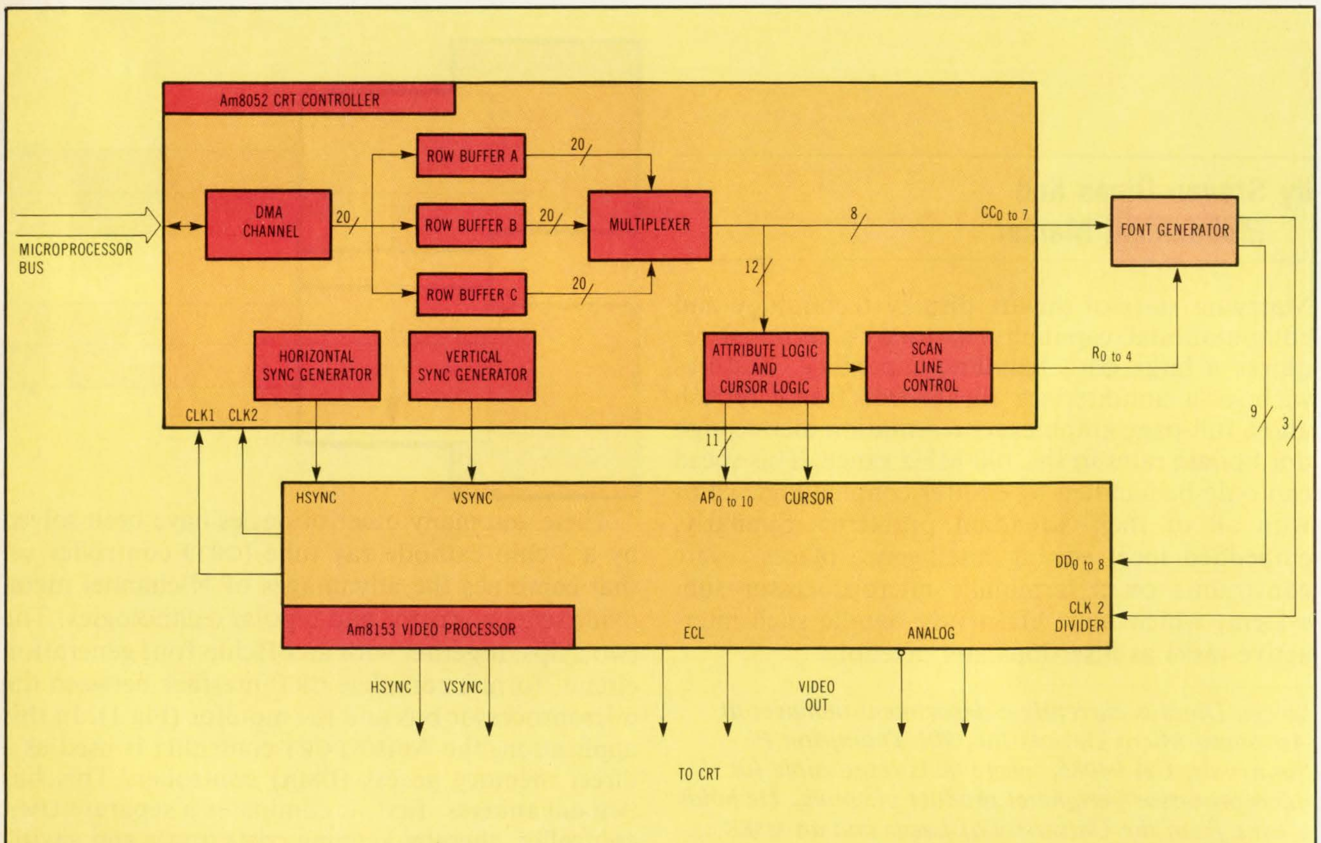


Fig 1 Two large scale integration chips and a font-generation read only memory form the interface between a 16-bit microprocessor bus and the CRT. Using three row buffers instead of the usual two ensures smooth scrolling in a split-screen application. The DMA channel fetches rows of characters into the three row buffers and outputs multiplexed data for attribute and cursor generation. The video processor chip serializes data for a video output and synchronizes the display with all the appropriate timing signals. The font generator can format the characters for proportional spacing to match the typical proportionally spaced characters of a printer output.

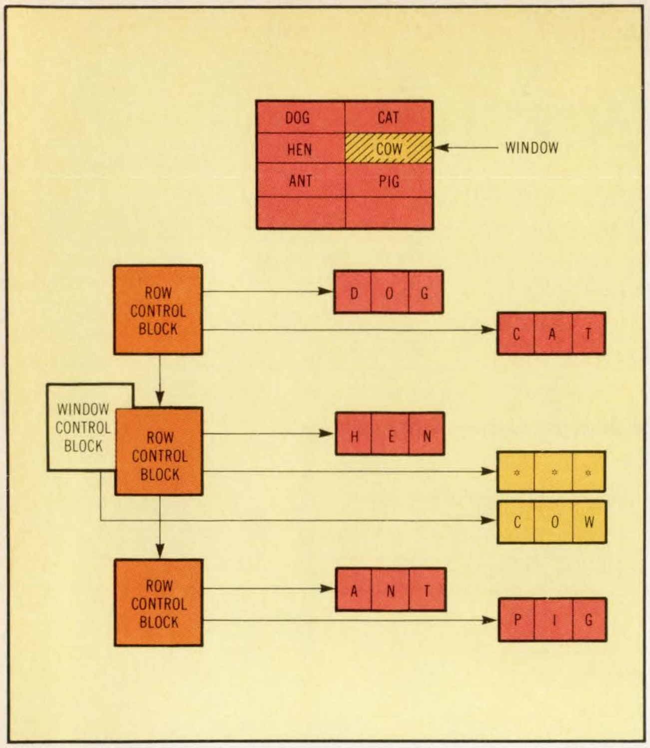


Fig 2 Windowing requires manipulation of a large amount of data. By using a linked-list data structure, the CRT controller chip can perform the windowing task at the CRT refresh rate. The chip maintains parallel control over the characters for both the full screen and the window. In this example, the three row control blocks keep track of their row entries in the background of the screen, while at the same time the window control block is used to insert the word "COW" in the appropriate window.

control blocks (RCBs). These blocks hold pointers to character and attribute lists for the appropriate row. The controller IC scans this complete list once per frame. Furthermore, the Am8052 keeps an eye on a second parallel list—the window data structure. This window linked list is used to overlay windows onto the screen. As the controller fetches screen data, it jumps from the screen to the window and vice versa to format the display (Fig 2).

After setting the display and one or more windows, the user can now issue a "scroll window" command to set the scroll in motion. When scrolling the screen, the user must ensure that the data structure is updated to reflect the new screen by modifying a pointer. Likewise, when scrolling one of multiple windows, the user must then update the window list in a similar fashion. In both cases, no complex data movements need occur. The Am8052 can scroll as slowly as one scan line every eight frames, and as fast as eight scan lines per frame—a significant spread in scroll rates. A system of interlocks protects the data from corruption during this scrolling.

A split-screen smooth scroll mandates three row buffers; a 2-row buffer configuration [Fig 3(a)] is acceptable for a single screen. Each of the rows is swapped or toggled with the other. Thus, while one row is being loaded, the other can be displayed. As long as each row buffer (ie, character row) is displayed for multiple scan lines, enough time is available to reload. However, for a split-screen smooth scroll, a character row can only be present in the frame for one scan line. This does not permit the alternate row buffer to be loaded and causes the screen to flicker. With three row buffers, however [Fig 3(b)], the problems of single scan line rows are averaged out, eliminating annoying screen flicker.

Character display generation

The Am8052 gives a flexible character capability to a video display terminal. Once the size (in scan lines) of a given character row is determined, the characters can then be placed in any position on the row. Further, row size can be varied on a row-by-row basis, and characters can be displayed as normal, superscripted, or subscripted, to allow flexible text.

Each character can be modified by an attribute word [Fig 4(a)] that is stored along with the character in the row buffers. Attribute words are fetched from memory, at the time the display is on, in a fashion similar to characters. The number of attributes fetched, however, can be programmed to be much smaller than the number of characters, thus reducing bus overhead. As in Fig 4(b), the string "CHANGED" is to be displayed in reverse video. By fetching a reverse attribute on the first "C" and a nonreverse attribute on the first "N" of "NORMAL," only two attributes are required to reverse the 7-character string.

The Am8052 attribute word on APO-AP10 can be used by the Am8153 to produce gray-level video from the font generator. For example, normal characters are displayed gray on white. If the highlight bit is set, however, the character will be

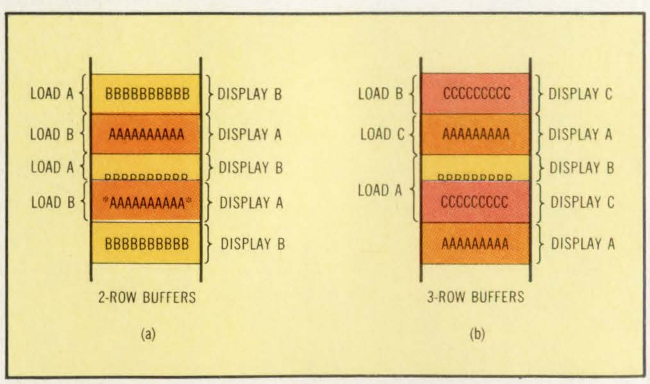


Fig 3 For split-screen scrolling applications, a character row could be displayed for only a single scan line. With two row buffers (a), this does not leave enough time for the reloading of the alternate row buffer, which results in a flashing screen. With three row buffers operating in a rotating fill-display mode (b), any single row buffer can be displayed for one scan line without any danger of screen flashing.

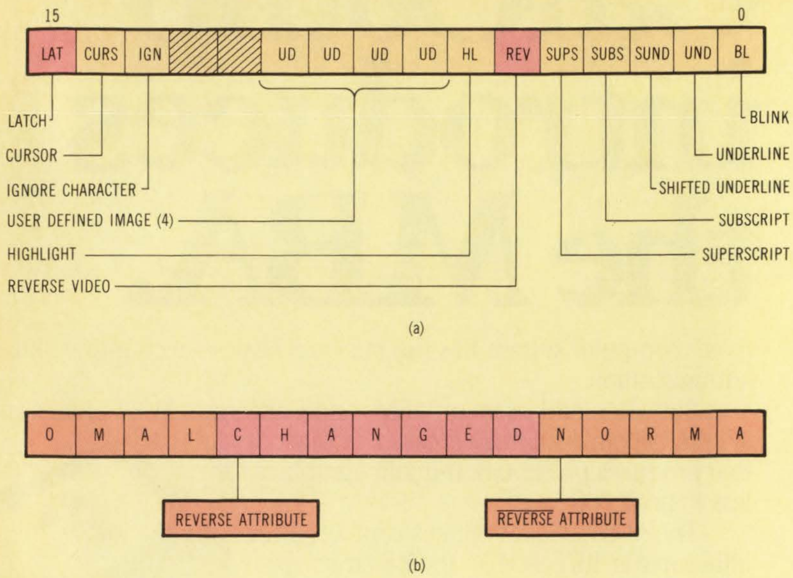


Fig 4 A 16-bit character attribute affects each individual character as it is output from the CRT controller (a). In memory, however, each new character need not invoke a new attribute. In example (b), the latch attribute, in conjunction with the reverse attribute, allows a string of characters to be displayed in reverse video without each character having to be individually reversed.

displayed white on black. Proportional spacing is achieved by altering the CLK2 input to the Am8052. The CLK2 spacing can be made to be as narrow as 2 pixels, or as wide as 17, assigning each character a width value that can be used to program the CLK2 output of the Am8153. Proportionally spaced video characters allow the screen to be formatted similar to the output of a proportionally spaced printer. Thus, proportionally spaced text can be composed accurately on the screen, prior to printing.

The CLK2 output of the Am8153 can be further modified by trailing blanks. Any number of blank pixels, between 0 and 3, can be inserted after the visible character. This allows the user to implement a smooth right justification of text, without inserting blank characters between consecutive words.

In addition to handling characters, the controller chip applies innovative techniques to the raster scan. It provides programmable horizontal synchronous (HSYNC), vertical synchronous (VSYNC), and BLANK signals, and accepts an external synchronization input. This input allows the frame to be synchronized to some external source such as line frequency, which prevents annoying interference display patterns known as "swimming."

Beyond supporting the more common noninterlaced and interlaced modes of operation, the chip also has a repeat field interlace feature that has each character row effectively repeated and offset by the scan line. This has the effect of making a vertical stroke on the screen look more solid, to match the horizontal strokes.

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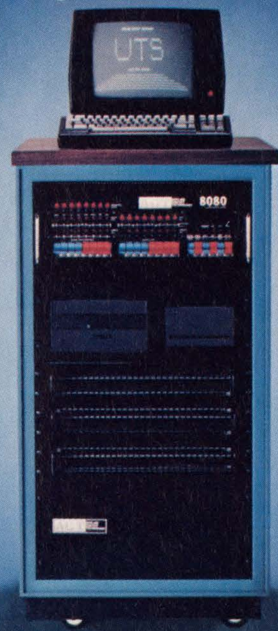

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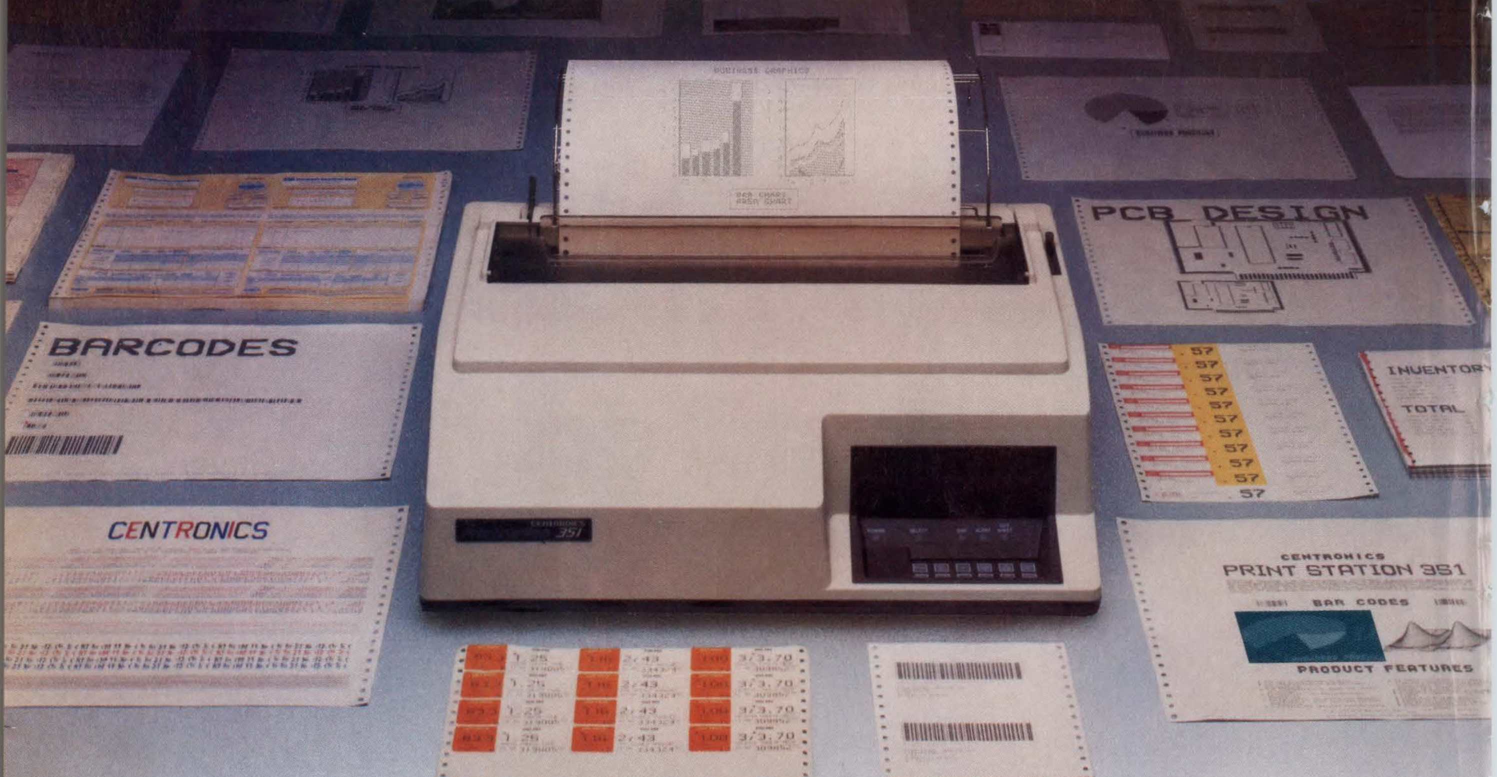

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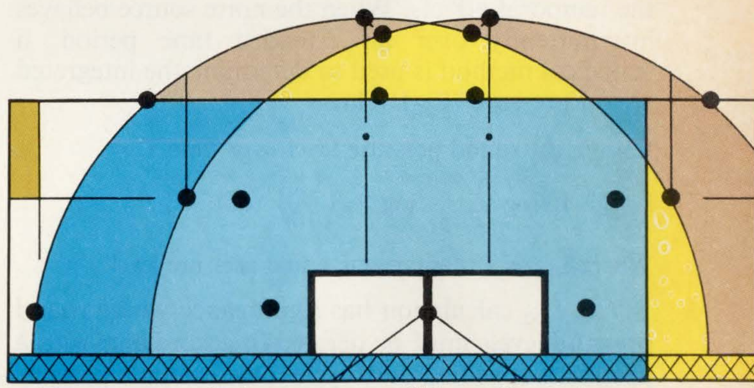
CIRCLE 89

MEASURING PRINTER ACOUSTIC NOISE

A standard measurement technique for printer noise can make reading dBa as easy as ABC.



by Stephen C. Armfield

Interpreting a printer's rated sound output in dBa should be simple. However, due to the lack of standards for measuring and specifying printer acoustic noise, this is not the case. Lack of such standards affects both end users, who must make objective comparisons of competitive products, and manufacturers, who must design quieter printers and publish noise specifications as part of product documentation.

Acoustic noise in printers has always been an annoying problem. In recent years, however, this problem has become acute. This is largely due to the migration of computer systems, and their associated printers, from the isolated computer room into the office.

The growing demand for quiet has been accompanied by general confusion. How quiet is "quiet"? How does one quantify the sound output level? How can a user compare two printers' dB noise levels without a common reference? Clearly, adopting a measurement standard is essential to answer these questions.

Stephen C. Armfield is manager of product planning at Centronics Data Computer Corp, Matrix Printer Div, One Wall St, Hudson, NH 03051, where he is responsible for future product plans. Mr Armfield holds a BS in engineering science and mechanics from the University of Florida and an MSEE from the University of Waterloo.

Numerous techniques are candidates for industry adoption. These techniques use well-known principles of acoustic theory, which specifies measurements to be made in terms of either sound pressure, sound power, or a noise rating method.

Sound pressure

While acoustic output of a noise source can be directly measured as an absolute pressure in units of Pascals (N/m^2), more often measurements are given relative to a reference pressure ($p_{ref} = 20\mu$ Pa) according to the equation

$$\text{Sound pressure level in dB} = L_p = 20 \log \left(\frac{p}{p_{ref}}\right)$$

The sound pressure measurement is usually made with a single microphone, which suggests why this measurement alone is not sufficient for fully characterizing the noise source. Microphone position becomes extremely critical, both in its distance from the source and in its relative position, in what is frequently a nonuniform dispersion pattern.

Adding numerous microphone positions around the noise source and calculating a logarithmic average from their individual measurements can alleviate the problem of a nonuniform sound field. This is the average surface sound pressure level, which for a reverberation field, is calculated by the equation

Surface sound pressure level =

$$L_{pf} = 10 \log \left[\frac{1}{N} \sum_{i=1}^{N} \log^{-1} \left(\frac{L_{pi}}{10}\right)\right] - K$$

Where L_{pi} = Sound pressure level of the ith measurement

N = Total number of measurements

K = Environmental correction over the measurement surface

Note, however, that the microphone's distance from the noise source still greatly affects surface sound pressure.

Frequency spectrum of the noise source, as well as its temporal characteristics (impulsive versus continuous), also affects sound pressure measurements. Weighted filters can be used to address the first problem, while the dynamic response of the sound pressure level meter can be adjusted to accommodate the temporal effects. When the noise source behaves intermittently over an extended time period, a statistical method is used to determine the integrated sound pressure (L_{eq}). Thus,

Equivalent sound pressure level over time T =

$$L_{eq} = 10 \log \frac{1}{T} \int_0^t \log^{-1} \left(\frac{L_{pt}}{10}\right) dt$$

Where L_{pt} = Instantaneous sound pressure level

The L_{eq} calculation has significance where sound pressure levels must be derated in accordance with a product's specified duty cycle. One example pertains to the use of the West German VDI 2058 standard. This standard limits the acoustic noise according to the average sound pressure level over an 8-hour period, and as a function of the type of work being performed (eg, 55 dBa for demanding, intellectual work). Since most printers operate at less than 100% duty cycle, the average noise level over an 8-hour period must be derated from the normally specified operating level. Derated noise level is calculated with the equation

$$L_{eq} = 10 \log \frac{1}{T} \left[t_1 \log^{-1} \left(\frac{L_{p1}}{10}\right) + t_2 \log^{-1} \left(\frac{L_{p2}}{10}\right)\right]$$

Where T = Total measurement time ($t_1 + t_2$)

L_{p1} = Sound pressure level during time t_1

L_{p2} = Sound pressure level during time t_2

If the nonoperating noise level is zero (ie, no fan, or printer turned off), then the rated duty cycle (d) can be directly converted to a derating correction level with the formula

$$L_{pd} = 10 \log d$$

For example, if the operating sound pressure level is 62 dBa and the rated duty cycle is 25%, then the average sound pressure over eight hours would be determined by derating 62 dBa by log (0.25) = −6.02 dB. This results in a 56-dBa average level.

Sound power

The total acoustic output of a noise source can be expressed as either an absolute value in units of watts, or as a relative value in units of dB

$$\text{Sound power} = L_W = 10 \log \left(\frac{W}{W_{ref}}\right)$$

Where $W_{ref} = 1_{pW}$

In practice, sound power in a free field is calculated using the surface sound pressure previously described.

$$\text{Sound power} = L_W = \overline{L_{pf}} + 10 \log \left(\frac{S}{S_0}\right)$$

Where $\overline{L_{pf}}$ = Surface sound pressure level

S = Area of measurement surface

S_0 = Area of reference surface

(ISO 7779 specifies $1m^2$ for S_0)

Note that sound power measurements compensate for the microphone's distance from the noise source. These measurements also accommodate noise sources with irregular field patterns. Sound power offers a degree of definitiveness not provided by single-point measurements of sound pressure. Thus, sound power is often recommended for equipment labeling and comparison purposes.

Noise rating

While sound pressure and sound power measurements are essentially broadband measurements, the noise rating technique is based on a noise source octave-band analysis. A set of spectrum curves, which allows each noise source to be assigned a noise rating (NR) number, has been derived. This number (NR65 or NR55) is derived by measuring the sound pressure level in each octave band at the worst-case position one meter from the source. Plotting these values yields the noise rating (corresponding to the predefined curve just exceeding the plotted spectrum). Although the noise rating method is used in certain narrow markets, it does not have wide support as a global standard.

For an industry standard sound measurement method, three groups have viable existing or proposed standards. These include several related ISO standards, certain German standards (DIN and VDI), and a group from ANSI. (See the Panel, "Printer noise measurement standards.")

ISO standards largely stress sound power as the parameter of interest. One exception is proposed draft ISO 6081, which specifies an operator position sound pressure measurement. Note that even with the sound power measurement standards, an "operator position" sound pressure value can be extracted from the normal measurement results. In ISO 3745, for example, microphone position 6 in the 10-position microphone array approximates an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Printer noise measurement standards

Standards for specifying noise measurements have been developed by the International Standards Organization (ISO), the Deutsches Institut fur Normung (DIN), the Verein Deutscher Eigenieur (VDI), and the American National Standards Institute (ANSI).

Currently, the ISO has nine standards:

- ISO 3740, "Acoustics—Determination of sound power levels of noise sources—Guidelines for the use of basic standards and for the preparation of noise test codes." This standard explains how and when to apply the following six related standards.
- ISO 3741, "Acoustics—Determination of sound power levels of noise sources—Precision methods for broadband sources in reverberation rooms."
- ISO 3742, "Acoustics—Determination of sound power levels of noise sources—Precision methods for discrete frequency and narrow-band sources in reverberation rooms."
- ISO 3743, "Acoustics—Determination of sound power levels of noise sources—Engineering methods for special reverberation test rooms."
- ISO 3744, "Acoustics—Determination of sound power levels of noise sources—Engineering methods for free-field conditions over a reflecting plane."
- ISO 3745, "Acoustics—Determination of sound power levels of noise sources—Precision methods for anechoic and semi-anechoic rooms." This standard has enjoyed popularity in a wide range of applications to determine sound power. Unfortunately, it does not specify the printer operating conditions to be used during the test, nor does it explicitly address an operator position sound pressure measurement.
- ISO 3746, "Acoustics—Determination of sound power levels of noise sources—Survey method."
- ISO 6081, "Acoustics—Noise emitted by machinery and equipment—Guidelines for the preparation of test codes of engineering grade requiring noise measurements at the operator's position." This standard is still a draft. However, it offers a well-defined procedure for determining the operator position sound pressure level.
- ISO 7779, "Acoustics—Measurement of airborne noise emitted by computer and business equipment." This is the most complete standard and is currently being considered for approval. It specifies a sound power measurement (based on ISO 374X), a sound pressure measurement at an operator or bystander position (based on ISO 6081), and specific operating conditions for certain classes of equipment such as typewriters, disk drives and printers.

DIN and VDI have three local standards that essentially apply to equipment to be used in West Germany. The acoustic noise issue is more critical in the German marketplace than anywhere else. In Germany, there is a trend toward equipment labeling requirements, and laws are already in place that prohibit the use of excessively noisy products. The standards are

- DIN 45635 Teil 19, "Measurement of airborne noise emitted by office machines." This standard defines a sound power measurement equivalent to the ISO 374X series of standards. Exporters of printers to West Germany may be required by law to provide equipment noise data that have been measured in accordance with this standard.
- VDI 3729, "Noise emission characteristics of technical sound sources." Versions of this standard are available for particular categories of equipment (eg, typewriters, copiers, and cash registers).
- VDI 2058, "Judgment on noise in the workplace with regard to hearing damage." Referenced by German Ergonomics standard ZH1/535, this standard is also associated with a German workplace law that limits the amount of acoustic noise to which a worker can be exposed over an 8-hour period.

Both ANSI standards are essentially equivalent to some of the standards already mentioned. ANSI S1.30-35 specify sound power measurements that relate to the ISO 374X series of standards; ANSI S1.29 is related to the ISO 7779 draft proposal.

For further information, contact

International Standards Organization
c/o ANSI
1430 Broadway
New York, NY 10018

Deutsches Institut fur Normung
Burggrafenstrasse 4-10
Postfach 1107
D-1000 Berlin 30, West Germany

Verein Deutscher Eigenieure
VDI—Kommission Larmminderung
Graf-recke Strasse 84
4 Dusseldorf 1, West Germany

American National Standards Institute, Inc
1430 Broadway
New York, NY 10018

operator position. However, the distance of microphone 6 from the noise source can vary, yet still be in compliance with the measurement standard.

A measurement technique has to accommodate both technical and marketing requirements. The right technical solution is frequently incompatible with historical or user behavior in the marketplace. The needs in both areas can be widely different.

Engineering needs for an acoustic measurement method are accuracy, repeatability, and conformance to a standard. In terms of accuracy, the method must be able to characterize the sound output within a small range of error and uncertainty. The tests must also be done such that they can be repeated by others. Environmental and operating conditions must be specified and controlled so that tests performed at a different time or place can be readily compared with previous tests. Making such comparisons is the only way that a program for noise control can succeed.

To maintain the credibility of published noise levels, and to provide a method of making comparisons with competitive products, a standard from one of the major standards organizations should be used. Many technical groups have favored the ISO 3745 sound power measurement. But, marketing

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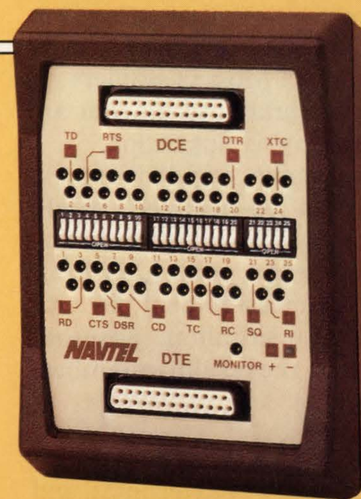

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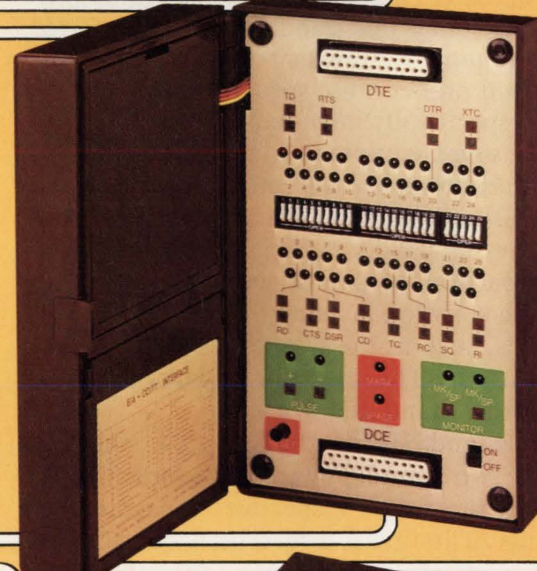

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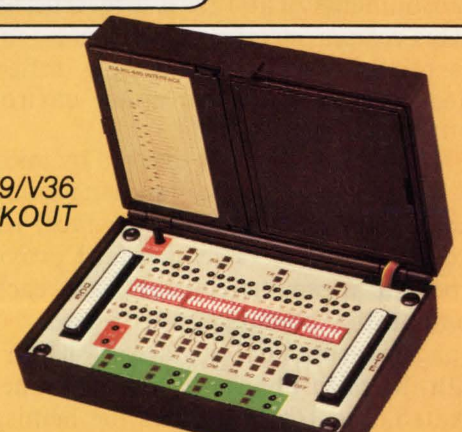

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and sales groups resist using sound power numbers just because they are inherently greater than numbers obtained by a single sound pressure measurement.

In general, marketing groups will only endorse a standard method that yields a low number. Through reasonable means, the quoted noise number should be no greater than that of a given competitor. The method should also prove easily understandable to a customer. Most customers do not want to discuss noise criteria in terms that are unfamiliar and require lengthy explanations.

Currently, the most popular way to express acoustic noise levels is in A-weighted sound pressure levels (dBa). However, there is rarely any qualification as to measurement standard, environment, operating conditions, measurement distance from the source, or relative microphone position. Without these qualifications, the resulting numbers are meaningless.

Standardizing sound measurement

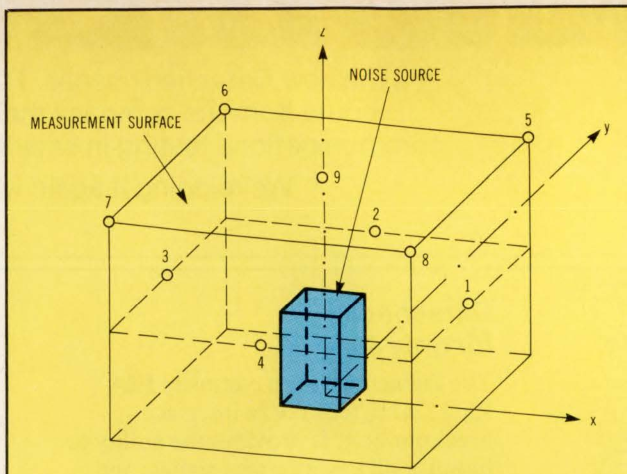
One approach that could satisfy both technical and marketing needs is embodied in the ISO draft proposal 7779. Adopting this standard as the preferred method of sound measurement could unravel the mystery behind printer noise specifications.

ISO 7779 is specifically intended for use with computer and business equipment. It provides for two types of sound power measurements, plus a sound pressure measurement at an operator or bystander position. The standard's explicit objectives are to enable comparison of similar equipment and to provide noise emission labeling data. Several other ISO standards, such as the 374X series and 6081, are referenced in 7779. This maintains a level of continuity with other standards work.

Sections II and III of the ISO 7779 standard describe the two sound power procedures. These differ only in their respective measurement environments. The first is a reverberant room that meets certain specific requirements; the other is an essentially free field over a reflecting plane. Measurements made in either environment yield similar results.

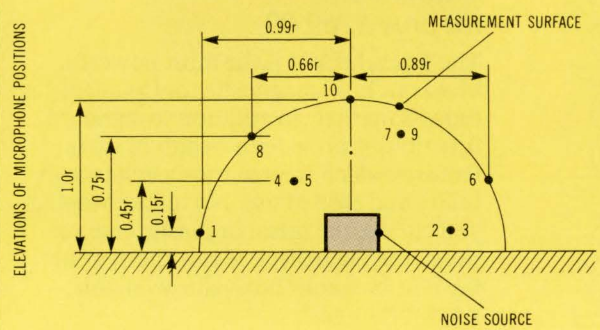
Sound power level is derived by taking a number of sound pressure readings using microphones, arranged on a measurement surface, that surround the noise source. The standard provides for two types of measurement surfaces, each producing comparable sound power figures. The parallel piped measurement surface is shown in Fig 1(a), with the positions for a 9-microphone array as indicated. Fig 1(b) illustrates the hemispherical surface with a 10-microphone array.

Section IV of the standard also describes a free field sound pressure measurement. A single measurement is made over a reflecting plane. This is done by using a microphone to correspond to either a "bystander" or an "operator" position,



(a)

Position	$\frac{x}{r}$	$\frac{y}{r}$	$\frac{z}{r}$
1	−0.99	0	0.15
2	0.50	−0.86	0.15
3	0.50	0.86	0.15
4	−0.45	0.77	0.45
5	−0.45	−0.77	0.45
6	0.89	0	0.45
7	0.33	0.57	0.75
8	−0.66	0	0.75
9	0.33	−0.57	0.75
10	0	0	1.0



(b)

Fig 1 Standard ISO 7779 could feasibly be adopted as an industry standard for measuring acoustic noise in printers. It provides for a sound power measurement, a sound pressure measurement in a bystander position, and clearly defines the test operating conditions. Sound power level can be derived by taking sound pressure readings from either a 9-microphone array in a parallel piped arrangement (a) or from a hemispherical surface with a 10-microphone array (b).

depending on the equipment type being tested. The criterion for determining which position is appropriate is whether or not the equipment requires operator attention while in operating mode. According to this test, most printers would be measured from the bystander position. Although the operator or bystander sound pressure measurement is included in the standard for comparison purposes, the standard recommends that these levels not be used as primary labeling information.

Accurate comparisons of two sound outputs can only be made if the installation conditions and equipment operation modes are identical. Annex C

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Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4
Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4
     Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4
          Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4
               Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4
                    Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4
                         Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4
                              Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4
                                   Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4
X6d-4                                   Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk
     X6d-4                                   Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk
Pgltk     X6d-4                                   Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe
     Pgltk     X6d-4                                   Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe
5ftoe     Pgltk     X6d-4                                   Jlyy7     2da90     8s8=2     6ai8q     B3laj
     5ftoe     Pgltk     X6d-4                                   Jlyy7     2da90     8s8=2     6ai8q     B3laj
B3laj     5ftoe     Pgltk     X6d-4                                   Jlyy7     2da90     8s8=2     6ai8q
     B3laj     5ftoe     Pgltk     X6d-4                                   Jlyy7     2da90     8s8=2     6ai8q
6ai8q     B3laj     5ftoe     Pgltk     X6d-4                                   Jlyy7     2da90     8s8=2
     6ai8q     B3laj     5ftoe     Pgltk     X6d-4                                   Jlyy7     2da90     8s8=2
8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4                                   Jlyy7     2da90
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2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4                                   Jlyy7
     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4                                   Jlyy7
Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4
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          Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4
               Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4
                    Jlyy7     2da90     8s8=2     6ai8q     B3laj     5ftoe     Pgltk     X6d-4
```

Fig 2 The ISO 7779 standard specifies the operating conditions to be used during testing, including the type of font, paper size and type, line spacing, and print speed. Furthermore, a print pattern specific to the printer's line length is defined. This pattern is for printers that have upper- and lowercase capability and can generate copy with more than 110 print columns.

of the standard specifies typical operating conditions for many equipment categories. Some printer parameters discussed include type of font, paper type and size, multicopy control, line spacing, margins, and print speed. For example, the print pattern to be used during measurement is defined for printers of various line-length restrictions. Fig 2 gives a sample page for use on printers with greater than 110 print columns and upper- and lowercase capability.

Although ISO 7779 is only a draft proposal, many industry officials agree that it would be unreasonable to await full approval before the printer industry adopts it as the preferred method of measuring acoustic noise. If adopted, future product documentation would use the following wording to specify sound output

Acoustic output (per ISO 7779)

Sound power	__dBa (__dBa idle)
Bystander sound pressure	__dBa (__dBa idle)

Eventually, sophisticated users will probably use just sound power measurement. However, the bystander position measurement is well defined by ISO 7779, and would be desirable to include in any equipment testing.

Published figures for sound output could be in either sound pressure or sound power, or in both. However, the published figures would have to be based on actual measurements. They would therefore be derived from a population size that offers a reasonable degree of statistical confidence. Thus, ISO 7779 could help manufacturers and end users make the proper choice when comparing similar products.

Acknowledgments

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Use the 1630 in software development and integration phases and you have sequencing, triggering, store qualification, and sequence restart power to isolate targeted areas of code and view just the measurement information you desire.

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The 1630 also gives you interactive measurement capability for greatly enhanced analysis power. The ability to cross arm and trigger between state and timing analyzers helps you get to the problem source quickly when the difficulty could be either a hardware or software malfunction.

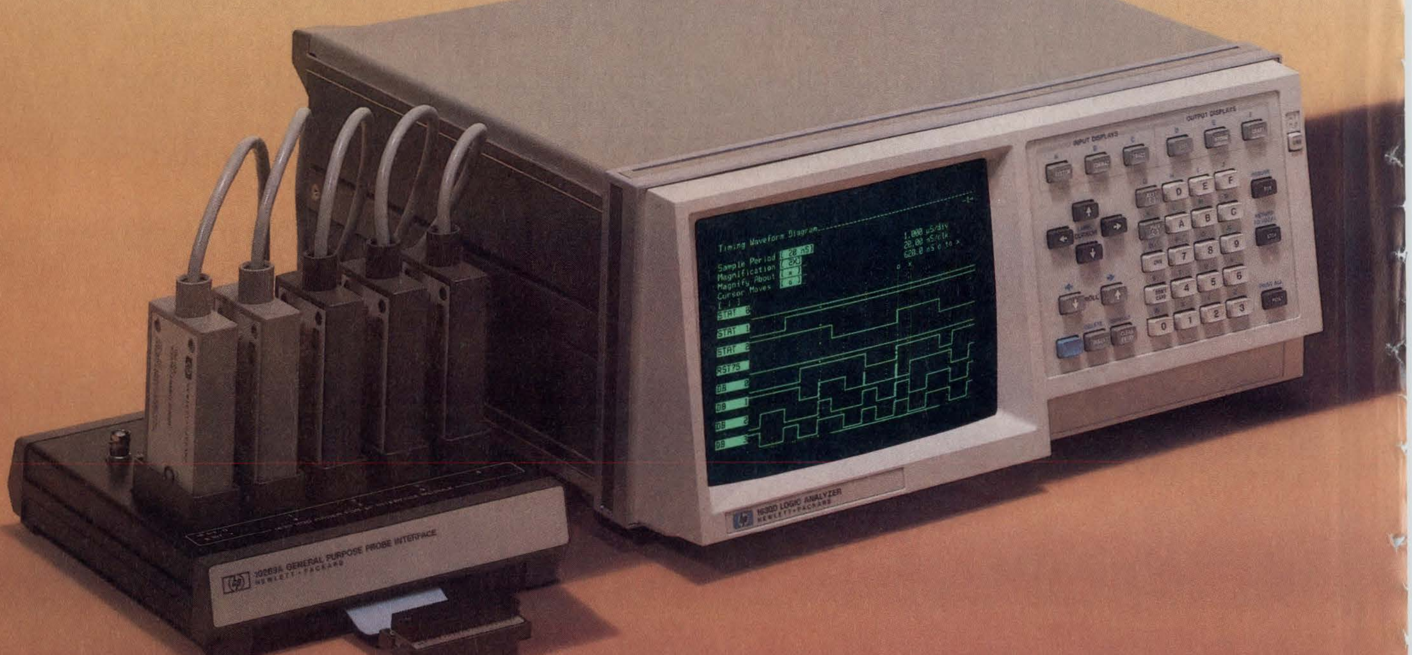
Throughout the development cycle, you'll find the 1630 easy to use. That's because menus simplify operation. Label assignments let you view results in your system's terminology. And inverse assembly, via low-cost peripherals, displays listings in familiar target microprocessor mnemonics.

The 64110A...a configurable analyzer that can handle those complex problems found in multiprocessor environments.

This logic analyzer is, in reality, a number of different analyzers, depending on how you configure it. For example, it can be a standalone timing analyzer with 8 or 16 channels.

It can also be a standalone state analyzer with up to 120 channels. You can combine timing and state with performance overview. Or, combine multiple state or timing analyzers in the same station.

Price for the 64110A,



nalyzer you need here... logic analyzer.

including a 60 channel state analyzer subsystem with performance overview is $21,870*.

Put the 64110A to work in the hardware test and debug phase and you can allocate high speed timing resources. For example, you might choose sampling speeds to 400 MHz. The resulting 2.5 ns resolution lets you make high-resolution measurements to resolve timing margin problems.

In addition, the timing analyzer provides new triggering capability. The dual threshold mode lets you trigger on marginal signal levels, which helps you spot excessive fan-out, bus loading problems, and slow transition times. Other trigger modes include time qualification of pattern triggering, sequential triggering, pattern triggering ANDed with a transition or glitch, glitch triggering, plus other modes that simplify the analysis of handshake problems.

In software test and debug, the 64110A gives you unequalled tracing, triggering, and store qualification power. With its master enable function, 16-level sequencer plus 8 user-definable terms for trigger, store qualification and count functions, you'll have little trouble locating the specific portion of code you want and displaying only the information of interest...even in the most complex multiprocessor software.

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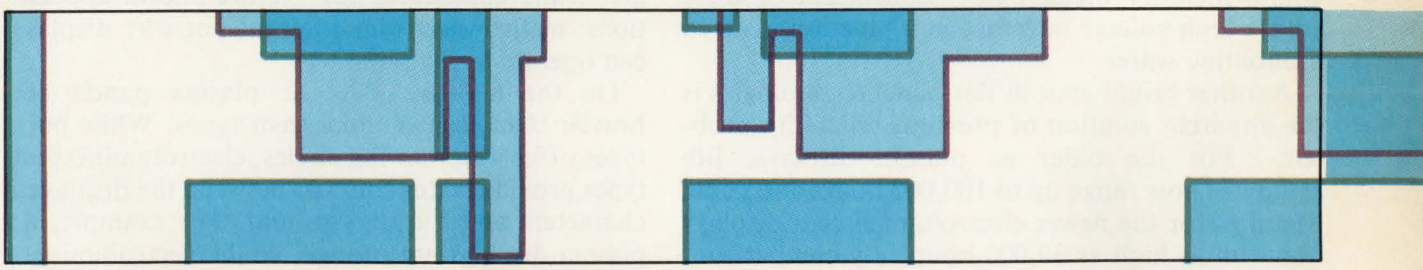
FLAT DISPLAYS—AN ALTERNATIVE TO CRTs?

Low cost driver chips are helping two flat-panel display technologies to displace CRTS in a variety of portable applications.



by Tom Engibous and Greg Draper

As the demand grows for portable and rugged terminals, personal computers, and workstations, the long-necked cathode ray tube must give way to space-saving flat-panel display technologies in a variety of applications. Despite the fact that cathode ray tubes still edge out the emerging technologies on a pure cost basis, from a technical point of view, flat-panel displays offer significant advantages. In addition to being smaller and more lightweight than cathode ray tubes, flat-panel displays are void of flicker, jitter, drift, and distortion. Moreover, flat panels provide better power efficiency and higher display resolution.

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Greg Draper is applications engineering manager of the display circuits branch at Texas Instruments Inc. He holds a BSEE from Southern Methodist University, Dallas.

Of course, the flat-panel display's major advantage is that it can be easily packaged in portable and rugged equipment. In contrast, the fragility, size, and weight of a cathode ray tube (CRT) system, as well as its bulky power supply, prevent true portability. Thus, flat-panel displays are well-suited for applications that include video telephones, wall-hung displays, electronic typewriters, and some word processors. Key parameter tradeoffs of three display types (CRT, ac plasma, and electroluminescence) are summarized in the Table.

Until recently, reliability, manufacturing, and driver-cost problems plagued flat-panel displays such as ac plasma and electroluminescent types. Now, through the application of bipolar double-diffused field effect transistor (BIDFET) semiconductor technology to display-driver integrated circuits, the driver-cost problems are greatly reduced. A rugged, low cost, patented process developed by Texas Instruments, BIDFET merges

Display Types			
Characteristic	CRT	AC Plasma	Thin-film Electroluminescence
Largest physical size at a given resolution	25" diagonal at 60 lpi	39" x 39" at 60 lpi	3.57" x 4.76" at 70 lpi
Largest number of elements	2048 x 2048	1200 x 1600	76,800
Display thickness	>2'	1/2"	1/4"
Weight	Heaviest	Light	Lightest
Luminous efficiencies	5	.1 to .3	1
Element memory	None	Inherent	Demonstrated but not used with large matrix panels
Gray scale	Yes	Not easily	Feasible
Contrast	50:1	30:1	50:1
Life	10,000 hours	>40,000 hours	30,000 hours
Basic color	Any color	Orange	Yellow
Multicolor potential	Full color	Any color phosphor, but difficult to construct	Yellow/red/blue (future development)

precision bipolar control circuitry and self-isolated complementary metal oxide semiconductor logic with a high voltage interface in a junction-isolated monolithic wafer.

Another bright spot in flat-panel technologies is the apparent solution of previous reliability problems. For the older ac plasma displays, life estimates now range up to 100,000 hours and panel lifetimes for the newer electroluminescent displays now run as high as 30,000 hours. By comparison, most CRTs have only a 10,000-hour operating rate.

Rating the displays

In order to choose the appropriate display for use in portable computer equipment, the best approach is to examine the strengths and weaknesses of ac plasma and electroluminescence. AC plasma (which has been on the market for over eight years) has two strong points: longevity, and a proven track record in ruggedized applications. For instance, ac plasma panels are being actively evaluated by the Department of Defense for use in military systems.

Due to an inherent memory feature (data-retention property), the electronics need not update an ac plasma display as often as those using other technologies, and ac plasma displays require no refresh. Thus, ac plasma panels require less bandwidth in supplying the display with new data—an important factor when display information is transmitted over a communication line. And, since ac plasma systems need not be refreshed to sustain an image, updating can be performed at a much lower rate than in electroluminescent or CRT displays. In fact, electroluminescent and CRT displays must be constantly refreshed to maintain data on the screen. As a result, ac plasma panels are prime candidates for picture-phone applications; neither electroluminescent nor CRT displays can operate in the same way.

On the negative side, ac plasma panels are heavier than electroluminescent types. While both types offer wide viewing angles, electroluminescent types provide better contrast between the displayed characters and the background. For example, ac plasma displays are orange, while electroluminescent types have yellow characters against a black background. Both are considerably easier to see than dc plasma displays, which have poor resolution and especially poor off-angle visibility. However, dc plasma types can be driven with less support circuitry than either ac plasma or electroluminescent types can.

To effectively compete with CRT displays on a cost basis, flat-panel driver components must be in the range of \$0.15/bit. Currently, driver-electronic costs for flat panels represent approximately 20% to 40% of the total system cost. This is due to the matrix-addressing nature of a flat panel. For example, replacing a standard 12" CRT requires drive components for 1024 individual electrodes or bit positions. Between ac plasma and electroluminescent displays, the drive components for ac plasma cost more. This is because they must provide signals with faster transition times than those required for electroluminescent panels. Thus, electroluminescent panels use a simpler type of drive than ac plasma, and electroluminescent panel drivers cost less on a cost/bit basis.

Cost is just one consideration when choosing a display. As far as structure, the ac plasma panel consists of two thin-glass plates separated by a

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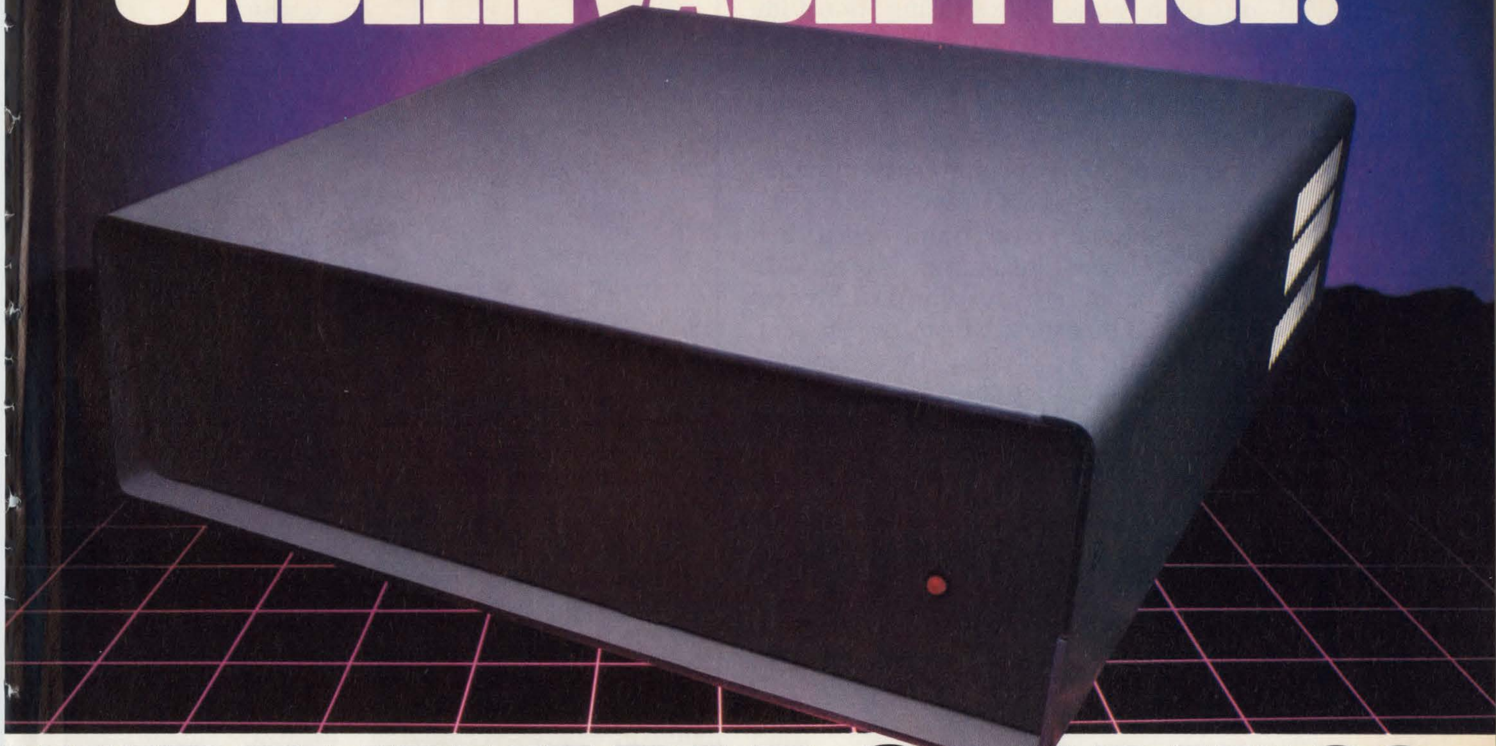

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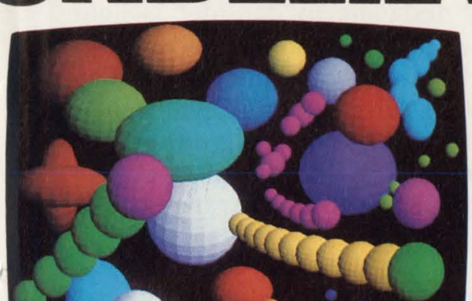
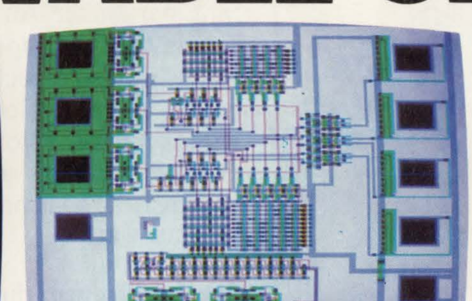
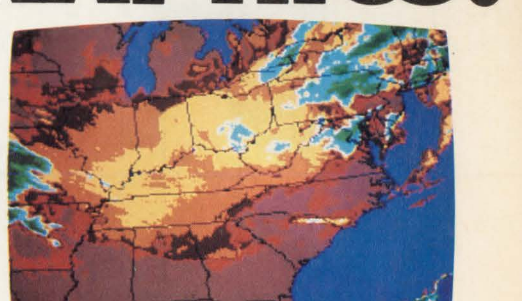


"*In The Beginning*" By Richard Katz, Vectrix Corporation



"*Integrated Circuit Design*" Courtesy of Floyd J. James, University of North Carolina at Chapel Hill



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gas-filled gap (Fig 1). A conductor pattern covers the inner surface of each plate. The conductors are deposited on both glass plates using thin-film techniques, and are covered by a dielectric layer. A gap between the two pieces of glass is filled with a neon-argon gas mixture, and a sealing material around the active area provides a gastight seal.

On the other hand, the electroluminescent panel consists of multiple layers, with an electroluminescence material layer sandwiched between upper and lower insulating layers. All electroluminescent-panel parts, except possibly the back electrodes, are constructed from transparent films (Fig 2). Like the ac plasma, the electroluminescent panel is configured as an X-Y matrix display by having horizontal electrodes and vertical transparent electrodes deposited at right angles to each other to form the matrix. Picture elements light up when ac voltage pulses are applied across electrode groups, and a high electric field is sent to specific electrode intersections.

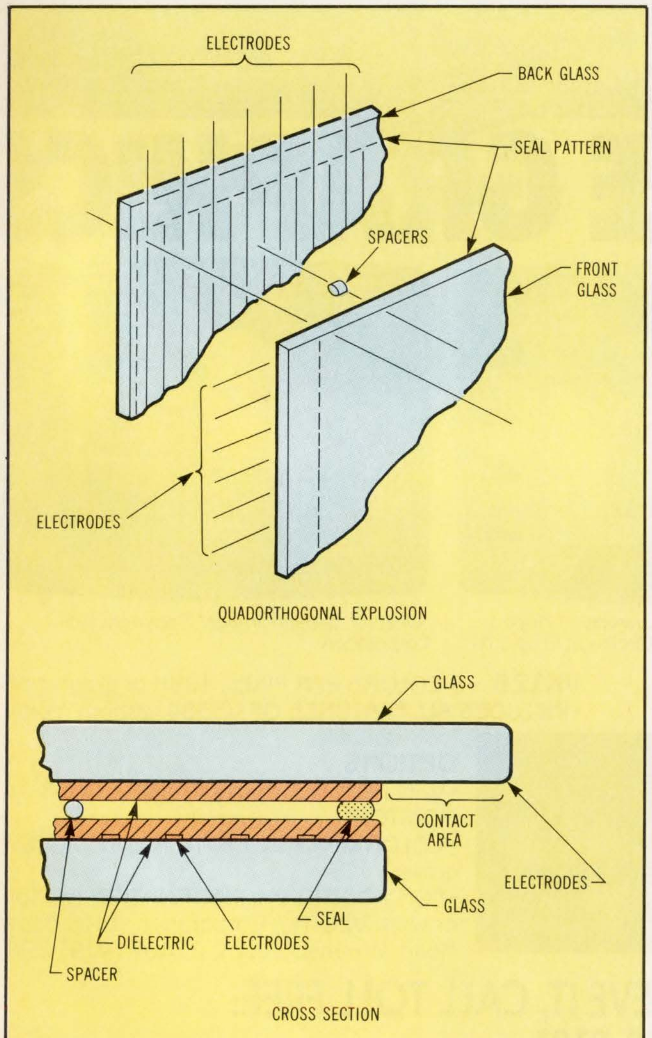


Fig 1 Two pieces of glass, separated by dielectric spacers, are the essential elements of an ac plasma panel. Electrodes for exciting the neon-argon gas mixture are plated on the glass, but separated from the gas by dielectric coatings.

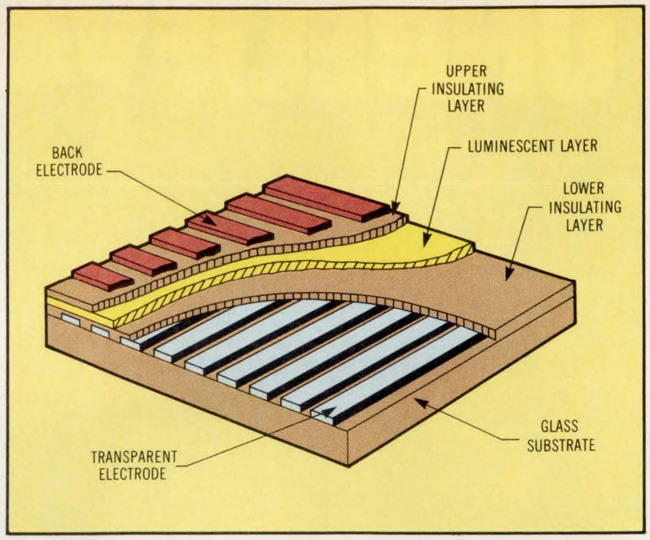


Fig 2 Electroluminescent panels use doped zinc sulphide that emits light when the voltages, which the embedded electrodes impose across it, exceed a threshold value.

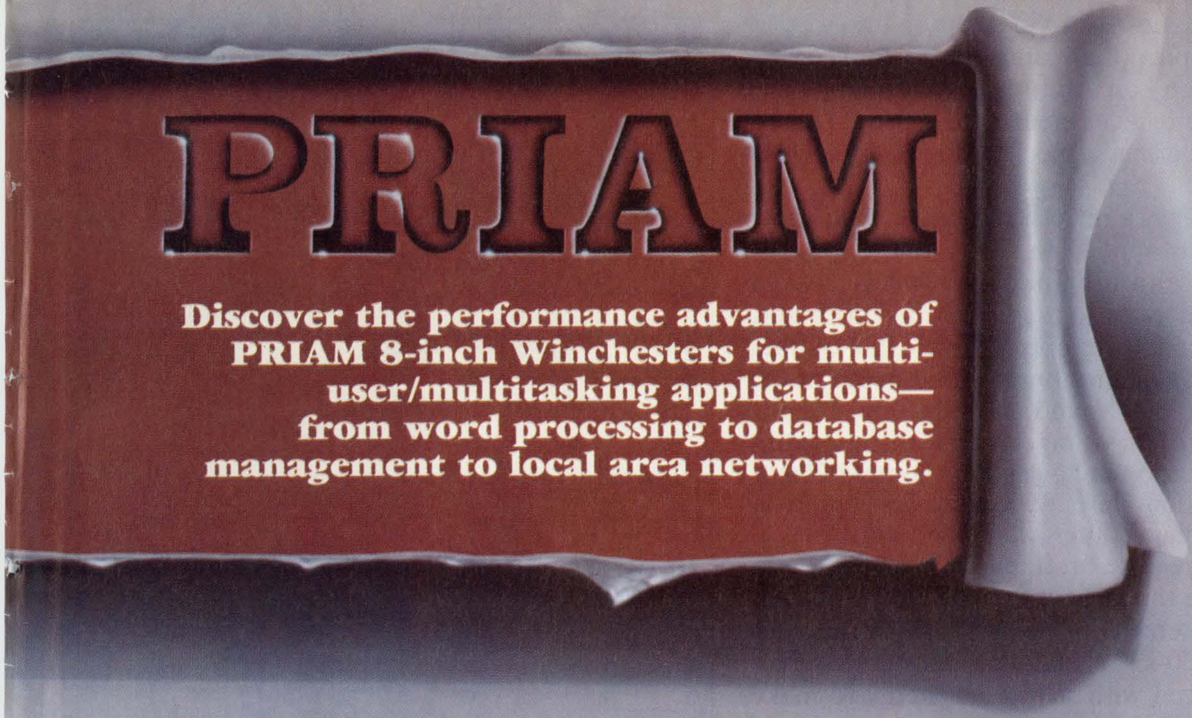
In both electroluminescent and ac plasma displays, light output is a drive voltage and frequency function. An electroluminescent-panel's light intensity depends on the frequency at which the display is refreshed, while an ac plasma panel's light intensity is related to the sustaining waveform's frequency.

Because light output is a variable that can be controlled over a fairly wide range, a more important parameter for designers to consider is light output/watt of input power, measured in lumens/watt. In this respect the electroluminescent display proves highly efficient. Electroluminescent panels with a yellow color on a black background have efficiency ratings as high as 0.5 lumens/watt. In contrast, ac plasma panels run in the range of 0.3 lumens/watt.

One intelligence, three displays

Whether CRT, ac plasma, or electroluminescence, the intelligent portion of any display is basically the same for each design: a universal asynchronous receiver/transmitter (UART) receives serial information from a host system and converts it to 8-bit parallel data for input to the intelligent controller's central processing unit (CPU); and an 8-bit bus links the UART, CPU, keyboard, read only memory (ROM), and random access memory (RAM). The UART is a bidirectional device; parallel data sent from the CPU are converted back to a serial stream and returned to the host system. The host system can be any type of computer, from a small personal computer to a large mainframe.

All three display types usually have commands and data for the controller CPU stored in ROM. RAMs are used to store pointers for tracking the line and cursor positions on the display. Data from the CPU are sent to the display map RAM that stores every location or position the data can occupy on



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the screen. Thus, an ASCII "A" written into a position in the display map appears at the corresponding location on the display screen. The character generator ROM creates the dot or pixel information that defines a specific character, such as the ASCII "A."

In a CRT display, a refresh controller then coordinates all signals applied to the screen [Fig 3(a)]. There, one line of information at a time is clocked from the line generator to the beam-control circuit. The line generator stores one complete line of data and clocks it out synchronously to the sweep of the electron beam. The X and Y deflection circuits generate a sawtooth voltage waveform. In addition, the X-deflection voltage sweep is either 256 or 512 times faster than the Y deflection, depending on whether the display is interlaced or noninterlaced.

CRT systems require an intensity or Z-axis control to modulate the intensity of the electron beam that strikes the screen. A high voltage source produces up to a 30-kV signal that accelerates electrons to the screen with sufficient energy to make the screen phosphors glow.

Typical electroluminescent and ac plasma systems use the same intelligent controller as the CRT display [Fig 3(b)]. However, except for the character generator, the drive circuitry is considerably different for both electroluminescence and ac plasma. In the electroluminescent system, control logic operates in a similar manner to the CRT's refresh generator, and the parallel-in-serial-out (PISO) register is an analog of the CRT system's line generator.

The PISO stores character data from the character generator and clocks this information out to the serial column drivers. A full line of information is stored in the SN75553 and 75554 column drivers. The required number of drivers depends on the electroluminescent panel's width. All drivers are serially daisy chained and clocked with a common clock signal. As a line of data is transferred and latched to the electroluminescent column drivers, a new line of data is loaded from the PISO.

Row drivers SN75551 and 75552 function similar to a CRT system's Y-deflection driver; that is, they select the line to be driven by using a raster-scan method that is a popular driving technique for electroluminescent displays. A data pulse is clocked to the first row driver, thus enabling data in the column drivers to be written on the display's first line. A second clock input to the row drivers activates the driver for the second row, and new data stored in the column drivers are written to the second row. The process continues until the entire screen is written. Data are refreshed at rates from 60 to 500 times/s, depending on the type of electroluminescent display used.

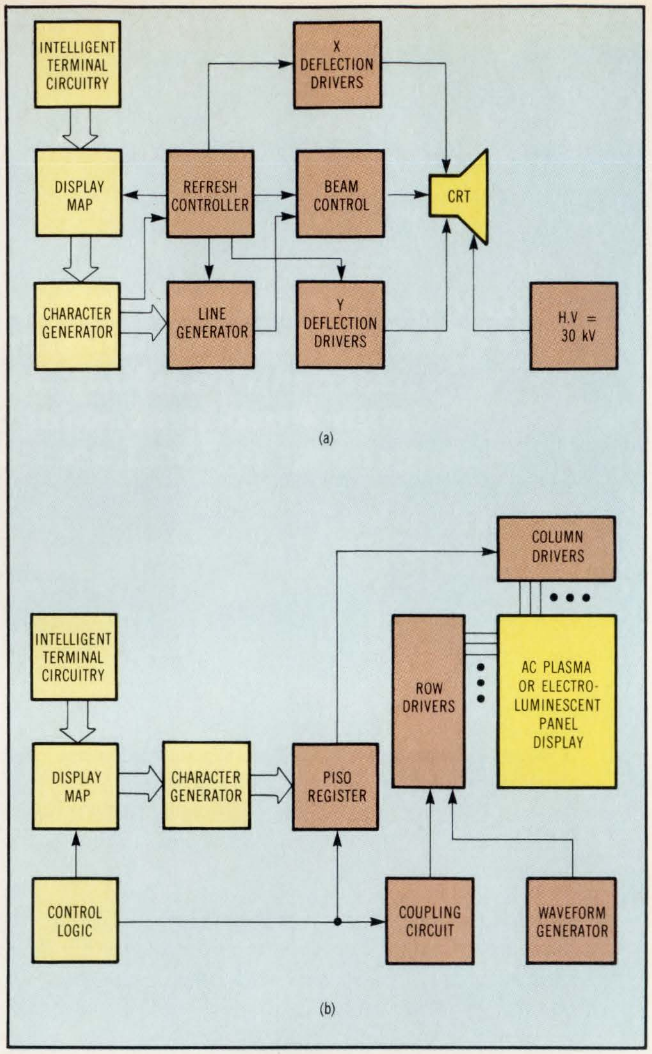

Fig 3 Circuitry for CRT displays (a) differs significantly from that of ac plasma or electroluminescent displays. The required high voltage power supplies also add weight and bulk. The ac plasma and electroluminescent circuits (b) differ mainly in the types of row and column drivers used (SN75500 and SN75501 for the plasma display; SN75551, 2 and SN75553, 4 for electroluminescence), and in waveform generator voltages (100 V for plasma, and ±200 V for electroluminescence).

Electroluminescent display column drivers use a ground-based logic that has the drivers' ground terminal connected to system ground. On the row drivers, however, the substrate common terminal connects to the composite waveform generator [Fig 3(b)]. Thus, the row-driver signals are referenced to the composite waveform (Fig 4). In an electroluminescent system, the magnitude of both positive and negative voltage is about 190 V.

The first pulse on the composite waveform is a refresh pulse with two functions: to maintain an average dc value of 0 V across the total display, and to provide a voltage of opposite polarity to each display pixel. This is necessary to ensure the appropriate operating potential for an ac-coupled electroluminescent display. In fact, the opposite polarity voltage increases a pixel's light intensity.

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Feature Comparison Chart *

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Overall Quality	2	**5**	3	4	3
Keyboard	3	**5**	2	4	2
Rollover/false keying	5	**5**	3	4	4
Video Quality	1	**5**	4	4	3
No. of attributes	5	**5**	5	2	5
Attribute method	2	**5**	2	4	2
Suitability for micros	2	**5**	3	5	3
	24	**39**	26	30	27
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*MICROSYSTEMS—March 1983
**THE ERGONOMICS NEWSLETTER—August 1982

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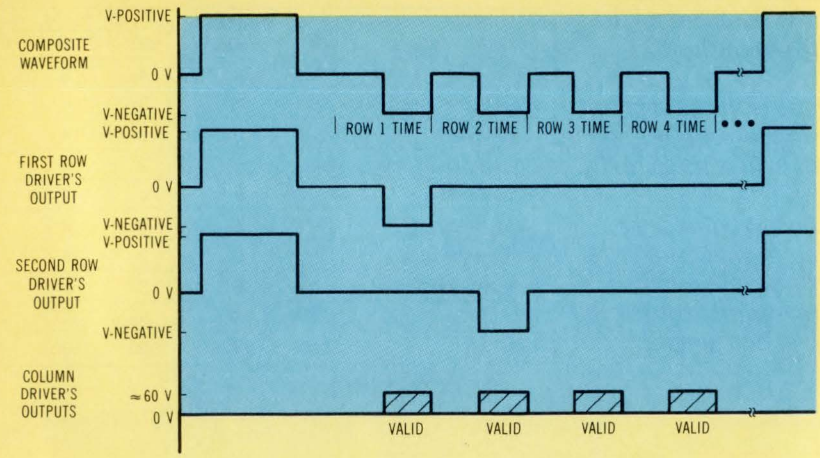

Fig 4 The composite waveform across an electroluminescent display reflects the information on each row driver, with a refresh pulse that maintains an average dc value of 0 V across the display.

The output voltage waveform of the first-row driver is a negative pulse that represents the data pulse stored in the register. When the driver is strobed, only the first row of the display is activated. As the clock pulse shifts the data out, the second-row driver creates a similar waveform to the first-row driver. A light output results at each display location (pixel) that has a logic 1 level stored in its column driver.

Feeding the row drivers is a coupling circuit consisting of a number of optical isolators that couple ground-based signals from the control block to the row drivers. Information coupled to the row drivers consists of a clock signal, data, and enable and strobe pulses. The typical ac plasma system uses a control circuit resembling that of the electroluminescent system. As in the electroluminescent system, the vertical or column drivers are ground based, while the horizontal or row drivers are referenced to a base waveform and must receive control information through an optical coupling circuit.

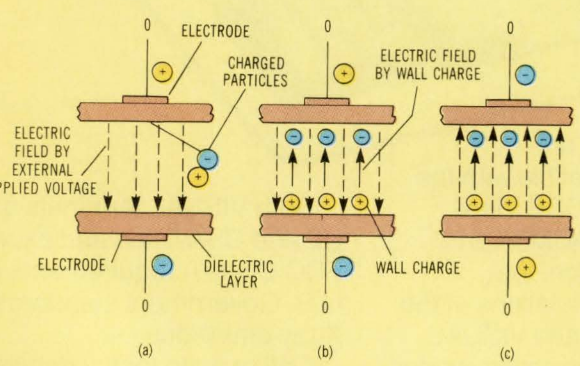

Fig 5 To initially ionize the cell, a relatively higher voltage is required (a). Once ionized, however, ions in the panel adhere to the walls (b), creating a wall charge that makes it possible to sustain light emission at a lower voltage. Thus, the next discharge starts at a lower external voltage than the initial starting voltage (c).

Driving the ac plasma

A major difference between ac plasma and electroluminescence is the data retention or memory property of plasma. While the light from any electroluminescent pixel fades quickly after about 1 ms, in the ac plasma display, the light must be erased. In addition, to write data into an ac plasma display, a wall charge must be created. A wall charge is an accumulated electrical charge across the dielectrics. These dielectric regions separate the electrodes from the ionized gas (Fig 5). When data are to be erased, some of the wall charge must be removed or subtracted.

The three possible phases of an ac plasma display are a write waveform that creates sufficient wall charge for writing data; a line erase waveform that subtracts wall charge when data are removed; and a sustain waveform that holds data on the screen until an erase waveform is applied to eliminate it (Fig 6). The base waveform, generated in the base waveform generator block, is a symmetrical square wave of about 100-V amplitude, but the actual voltage depends on the type of plasma display used.

Row drivers function in the same manner as those in an electroluminescent system. A row driver activates a specific line of the display, and the column drivers supply the actual data written on that line. Row drivers have 32 outputs, but since an SN75500 driver chip has just a single 8-bit register, the outputs are split up into four groups of 8 bits each. A system decode selects the correct 8-bit group to drive the display. The ac waveforms

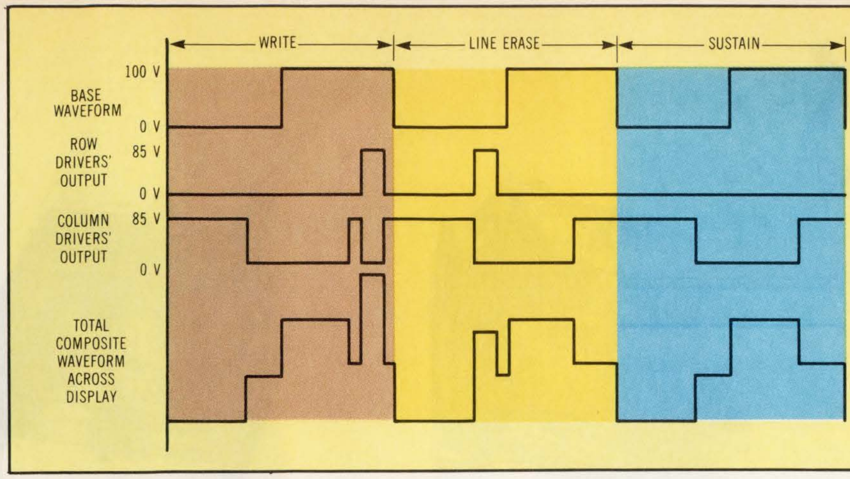

Fig 6 The base waveform establishes the basic timing and voltage levels for writing and erasing ac plasma displays. Signals applied to the row and column drivers determine whether data will be written, erased, or sustained.

applied to the display range from 30 to 60 kHz, depending on the type of display. But, the information a user views only needs updating about 10 times/s to create an adequate display terminal.

The total composite waveform is formed by adding the base waveform to the row drivers' switching waveform, and then subtracting the column drivers' switching waveform from the result (Fig 6). This composite waveform represents the voltage variations across each pixel. The composite waveform begins light emission when data are written. It sustains that emission if data remain unchanged and stops emission when data are changed.

Examining various flat-panel display characteristics confirms that such technologies hold many advantages in a number of applications. By focusing on the tradeoffs among display size, resolution, weight, and thickness, the designer can more easily determine the most appropriate display for a particular portable application.

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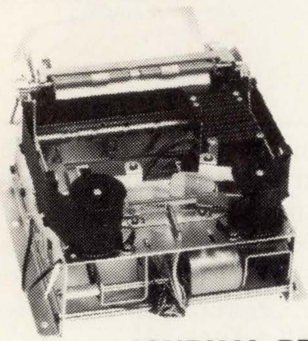

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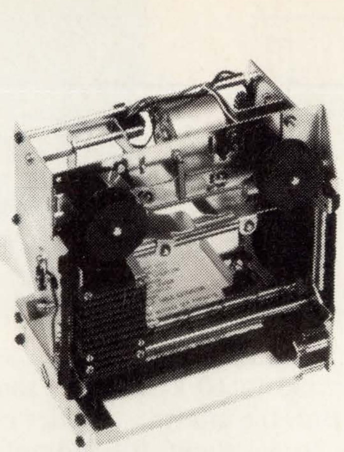

SLIP/DOCUMENT PRINTER
Model 840
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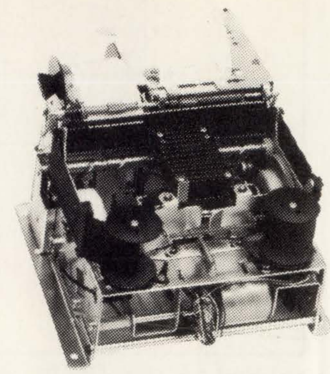
- Flat Bed Form Table
- Easy Side Or Front Form Insertion
- Top And Bottom-Of-Form Sensors
- Adjustable Slip/Document Stop
- Optional Forward/Reverse Paper Feed (Model 841)

CIRCLE 103



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Model 820
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CIRCLE 104

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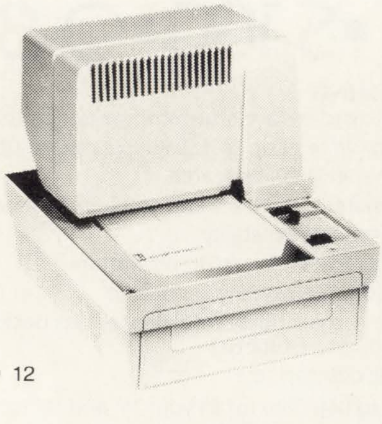

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Model 8400/8410

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CIRCLE 105

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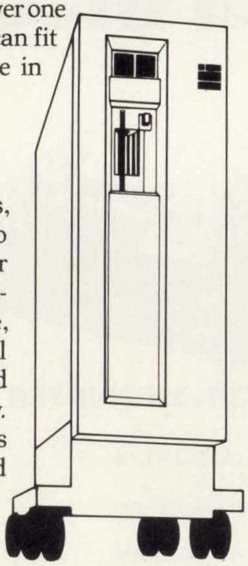

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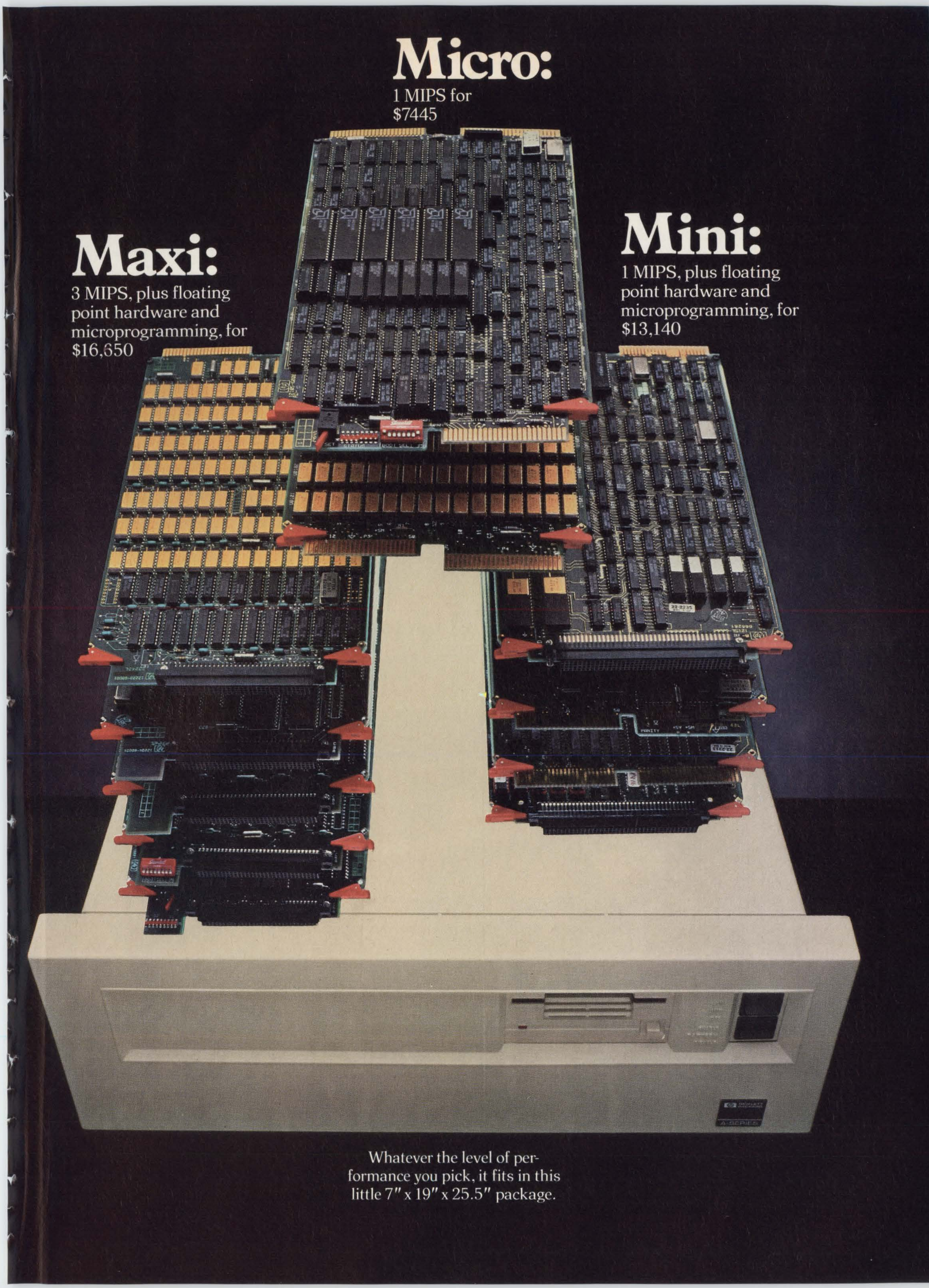
CIRCLE 111

TC-02309



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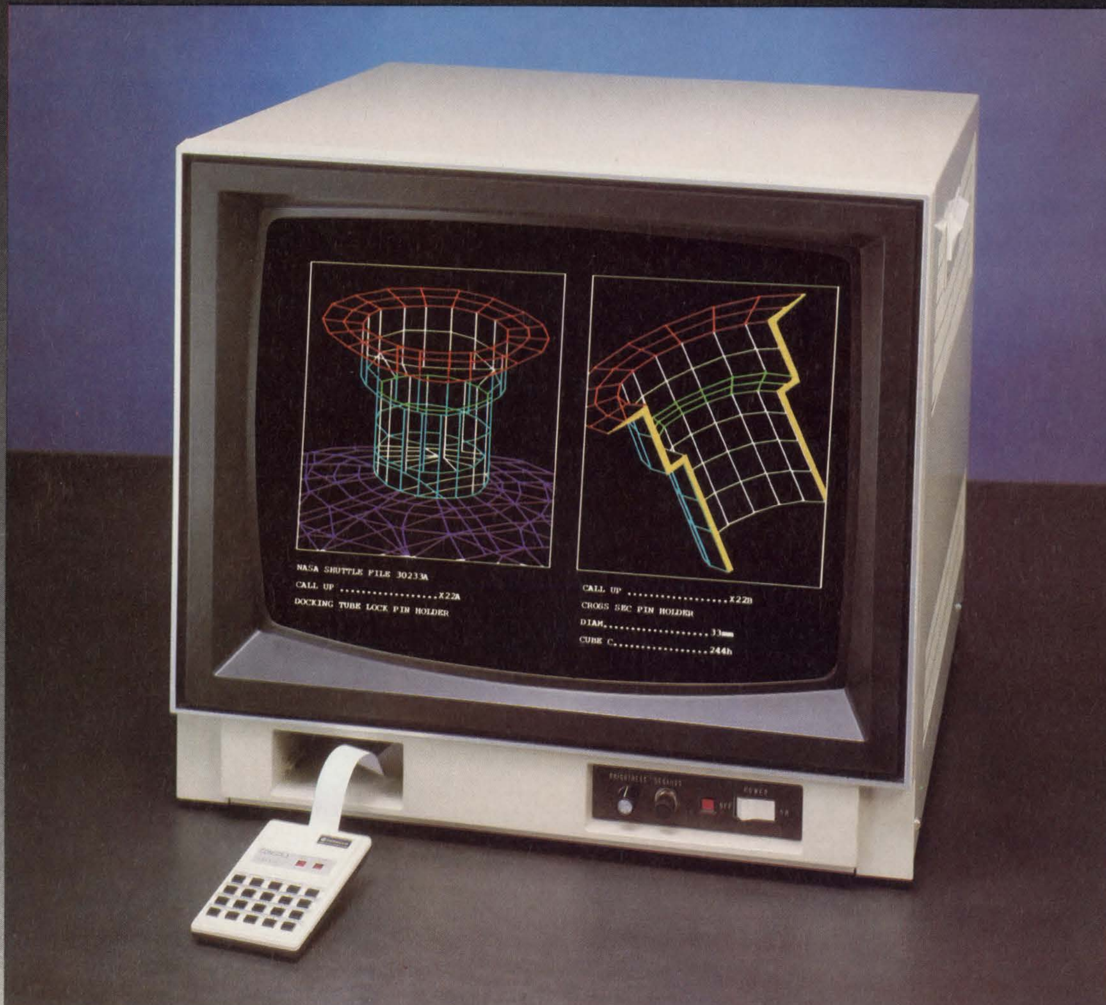

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CIRCLE 112

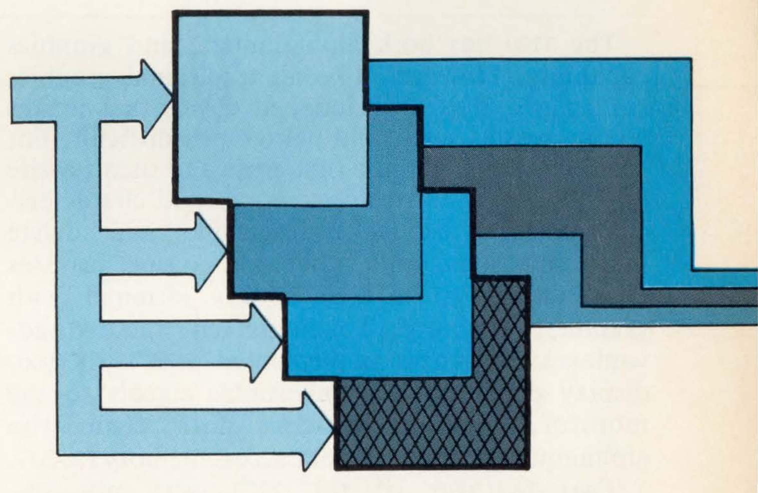
VLSI CHIPS SHINE IN COLOR TERMINALS

A graphics controller chip enhanced by support circuits allows designers to combine color graphics with alphanumerics in a compact and versatile CRT terminal.

by A. Mason Killebrew, Jr, and Susan B. Vogtlin

Design performance requirements of a particular computer system can seldom be precisely satisfied by using standard off-the-shelf integrated circuits. Usually, the more complex the chip, the greater the probability of compromised design and performance objectives. Occasionally, however, clever use of support chips can capitalize on the strengths of a very large scale integration chip while overcoming its deficiencies. Thus, many design and performance concessions can be eliminated or circumvented.

Peacock alphanumeric/graphics terminal is designed using a very large scale integration integrated circuit in conjunction with smartly used support



chips, thus realizing product objectives without major design compromises. The design objective was to combine color graphics capability with a high performance alphanumeric terminal. Zentec opted for the NEC 7220 graphics display controller (GDC) chip in designing its dedicated graphics controller. Thus, a significant learning curve for bit-slice designs was avoided. This resulted in fewer components, smaller circuit boards, and less development time than needed with bit-slice technology.

A. Mason Killebrew, Jr is currently product line manager in charge of terminals at Zentec Corp, 2400 Walsh Ave, Santa Clara, CA 95050. He holds a BA in economics from Florida Presbyterian College.

Susan B. Vogtlin is manager of advanced workstations at Zentec Corp. She holds a BA in German from Stanford University.

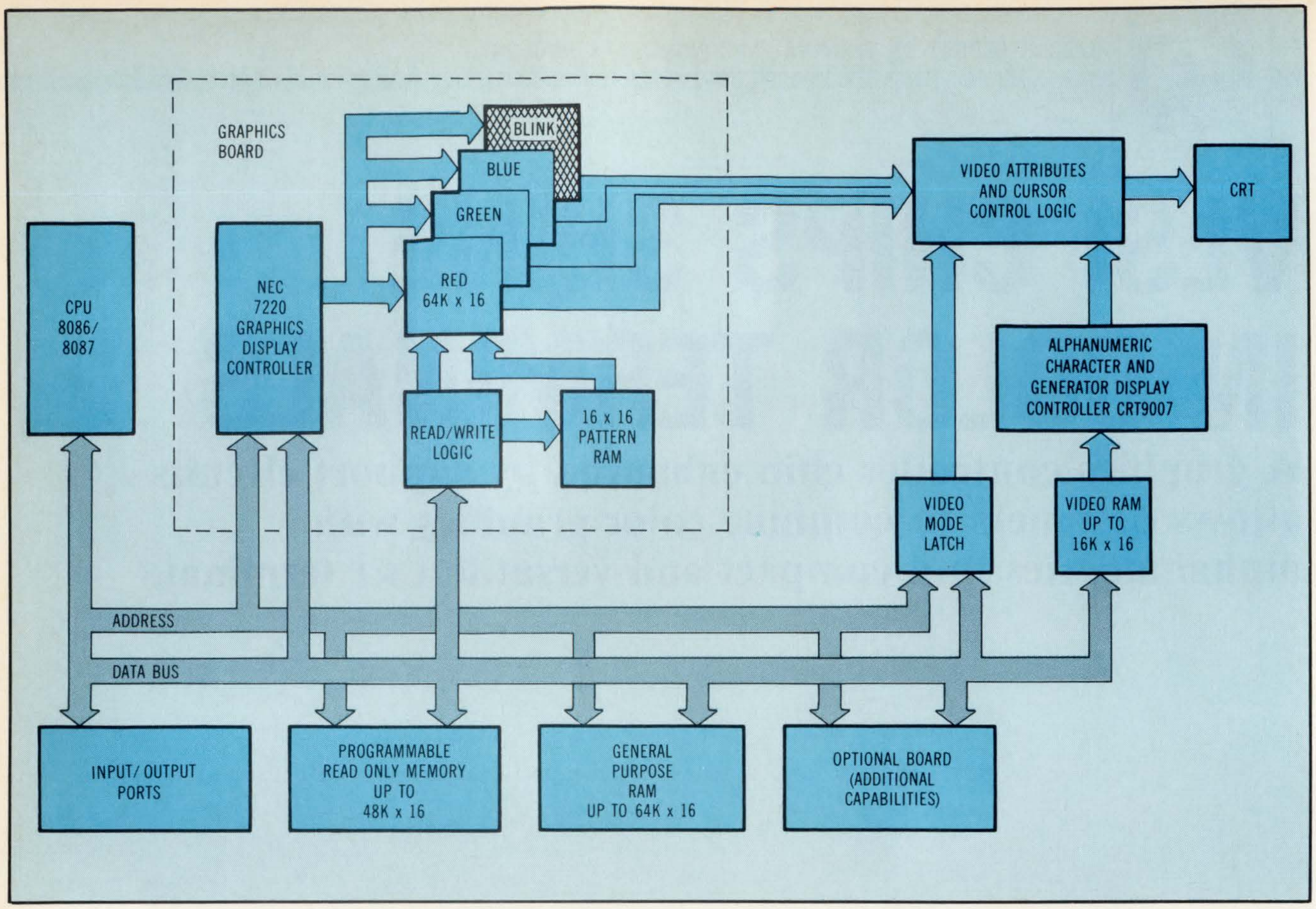


Fig 1 Here, the CPU (an Intel 8086 with optional 8087 numeric processor) handles computation, input/output to the keyboard and other devices, and controls the video signal to the CRT. An NEC 7220 on the graphics board handles all graphical manipulations in the image planes.

The 7220 has both alphanumeric and graphics capability. However, like all traditional graphics controllers, it is a bit-mapped device that makes editing words, lines, and paragraphs difficult. For example, the user must first erase and then rewrite on the display to avoid superimposed characters. The controller also lacks "insert line" and "delete line" functions, and other text-editing features characteristic of a high quality terminal with graphics capability. To circumvent these disadvantages, designers implemented SMC's CRT9007 display controller to synchronize signals to the monitor, and to process data from the alphanumeric video random access memory (RAM).

Two features of the 7220 were not implemented—one being a light pen. Though the light pen proves useful for certain applications, overcoming the light's parallax error is costly. Parallax error limits the light pen's utility for screen drawing. In addition, direct memory access capability for high speed data transfer is not used. This is done in order to limit hardware cost and conserve board space.

In the Peacock's graphics mode, the 7220 manages three banks of dynamic RAMs that are organized into "planes" and dedicated to bit-map graphics (Fig 1). Each plane stores pixel data for a primary color—red, green, or blue. An optional fourth "blink" plane is also managed by the 7220. The four 64K x 16 RAM planes store all the information from the drawing functions. The GDC chip manipulates these data, as well as performs zoom, pan, and horizontal split-screen functions.

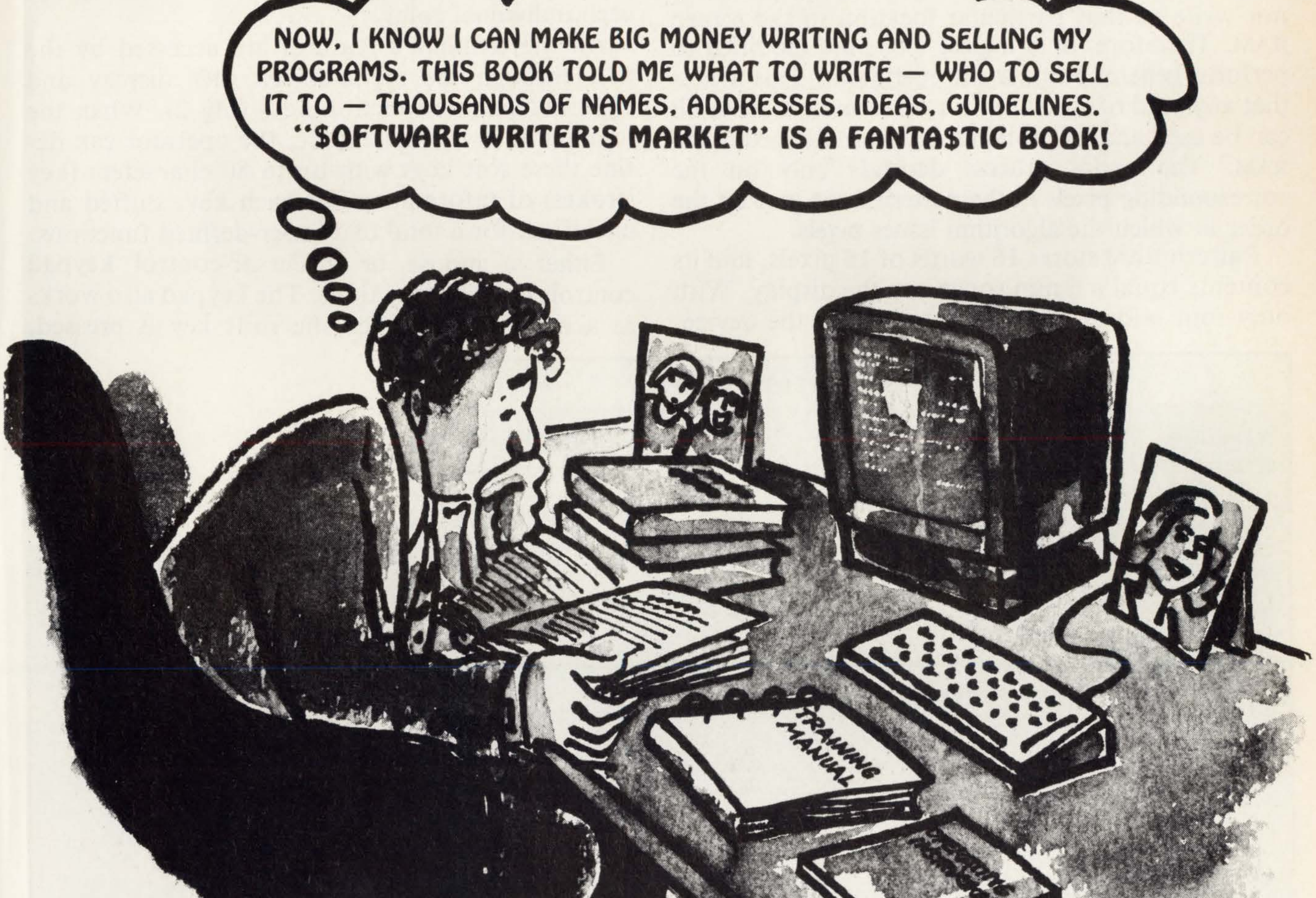
Responding to commands from the central processing unit, the GDC chip has to read a word in a 16-bit latch. The controller chip then modifies one pixel and sends the data out on a graphics data bus. Usually, the latched word read comprises all logical 1s. Consequently, one pixel of a modified word results in a logical 0. This bit indicates the bit to be written to the dynamic RAMs.

Exclusive-OR write logic controls the 16 write lines to each RAM plane. Data are input to a programmable logic array (PLA) from the graphics data bus. The PLA examines the data, recognizes the modification made by the GDC, and determines which pixel should be modified. This architecture can selectively force each bit to a 1, 0, or its complement.

If no bit is to be modified in any one plane, the draw-plane select latch disables the CAS of that plane during the write portion of the read/modify/write cycle. Thus, one drawing operation

programmer s

READ THIS...



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CIRCLE 113

can write to and independently complement selected bits, forcing them to 1s and 0s, or leaving them unchanged.

Terminals based on the 7220, but without clever support logic, can only specify bit-write times, a limiting parameter to say the least. On the other hand, Peacock specifies a 1.3-ms pixel/write time with up to 4 bits per pixel, 1 bit for each RAM plane. In addition, pattern RAM provides another benefit for interfacing the terminal to a host system. If the GDC reads data from the RAM while in its reset mode, it modifies only the logical 1 bits. Logical 0 bits remain unchanged, so the PLA does not write to that particular location in the screen RAM. Therefore, only logical 1 bits are modified to perform general-purpose fill operations. This means that any kind of algorithm for performing an area fill can be used and still obtain the pattern defined in the RAM. The entire process depends only on the corresponding pixels in the pattern RAM, not on the order in which the algorithm issues pixels.

Pattern RAM stores 16 words of 16 pixels, and its contents equal a 6-mm square on the display. With only four address lines used to decode the device, the image contained in pattern RAM is replicated across the screen horizontally and vertically.

Support circuitry allows the 7220 to fill circles, rectangles, and other figures oriented for any angle. Six system default patterns are stored in the RAM for area fills, and eight patterns for line drawings. Two additional patterns for area fill and line drawings can be defined by the user, either via the keyboard, or downloaded from the host system. In addition to speeding up the response time of the drawing process, the logic circuitry also minimizes the firmware required to set up the terminal, since drawing parameters do not have to be set up for each individual color.

All the terminal's features are accessed by the user through the menu-driven CRT display and eight redefinable function keys (Fig 2). When the terminal is in the user mode, the operator can define these soft keys with up to 80 characters (key strokes) of information for each key, shifted and unshifted, for a total of 16 user-defined functions.

Either a mouse or a cursor-control keypad controls drawing functions. The keypad also works as a numeric pad when the shift key is pressed.

```
                         TERMINAL WINDOWING MENU

Window         Workspace       Start:   Row          Stop:   Row
A/N #1         ---------                ---                  ---
A/N #2         ---------                ---                  ---
A/N #3         ---------                ---                  ---
A/N #4         ---------                ---                  ---
Viewport
G #1           ---------                0                    ---
G #2           ---------                                     ---

Workspace      Right Margin       Maximum Line Count        Cursor?
A/N #1            ---                    ----               Yes  No
A/N #2            ---                    ----               Yes  No
A/N #3            ---                    ----               Yes  No
A/N #4            ---                    ----               Yes  No

                  X                       Y
G #1             ----                    ----
G #2             ----                    ----

System Windows:      Message:     Enable      Disable
                     Status:      Enable      Disable
                     Prompt:      Enable      Disable

(Reserved for Messages)
Window Mode: Use cursor to position to fields.  The SELCT key
   highlights the selected field.  Press "save" to save menu.
   F1                  F3

  save                 recall
```

Fig 2 User interaction with the system occurs in two ways: via displayed menus and soft function keys. Similar menu displays prompt the operator through drawing functions and graphics text configuration.

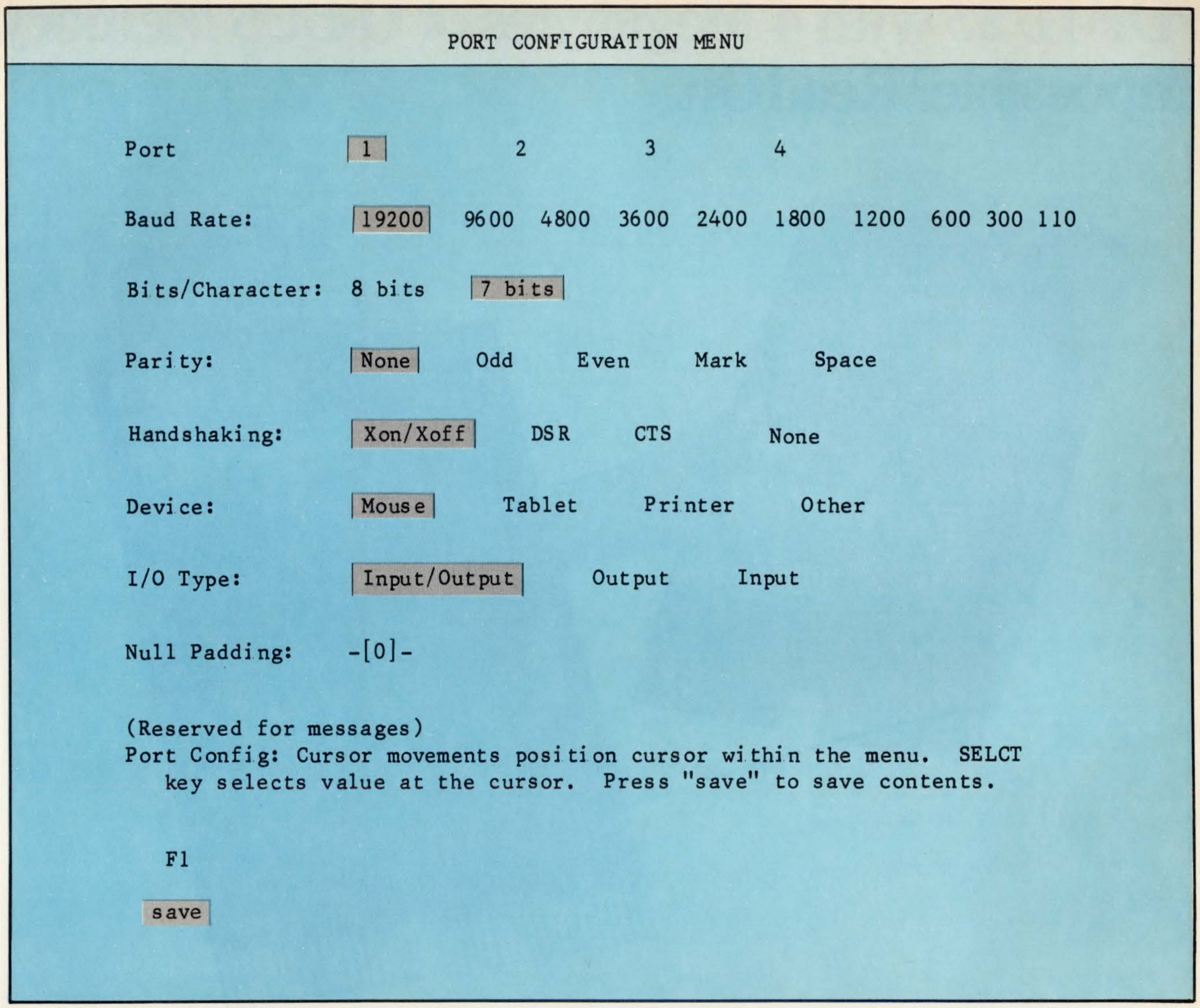

Fig 3 In this terminal configuration menu, nonvolatile RAM stores terminal set-up parameters, which traditionally have been set by dual-inline package switches.

Nonvolatile RAM stores terminal set-up parameters such as baud rate, number of bits per character, and input/output port configuration, along with the cross-hair cursor size (Fig 3). The keyboard has been simplified to the minimum 42 function keys plus standard alphanumerics.

In the future, terminals will probably be designed using either discrete components or a custom chip that can combine the dedicated CRT control functions with the support/logic functions. New circuits, such as area filling, could also provide some operations that firmware now provides. This will save on memory cycles and thus increase speed and throughput even more.

High performance clipping is achieved in hardware. The controller performs clipping using some of the high-order bits of the address lines to terminate an image at the end of an address range. If a drawn vector extends beyond that boundary, it continues into virtual space instead of entering the display from the opposite side.

Clipping would be more efficient if the system would stop drawing a vector when it reached a boundary, and could proceed to another drawing task. Implementing this in the existing architecture, however, would have been prohibitive in terms of chip count and cost.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

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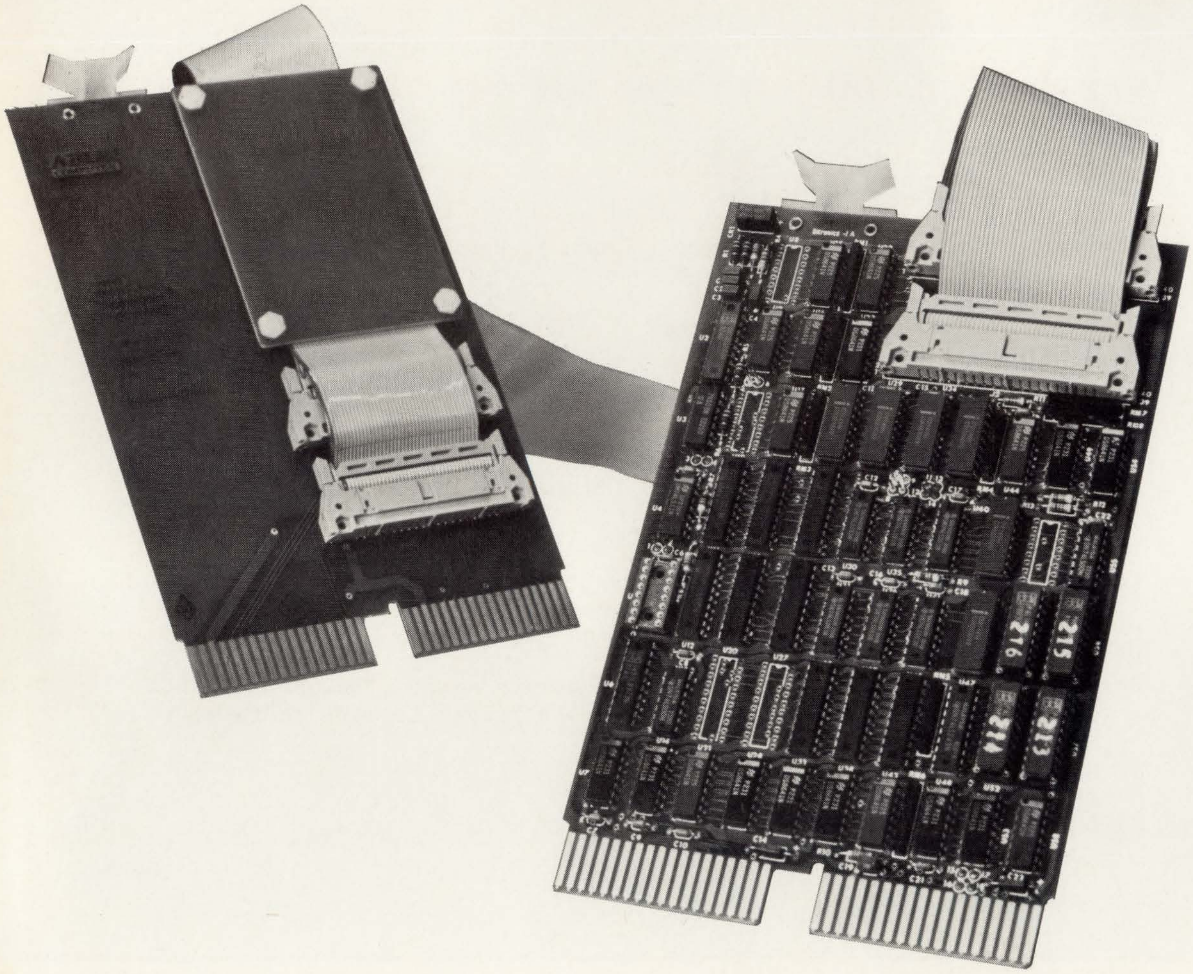

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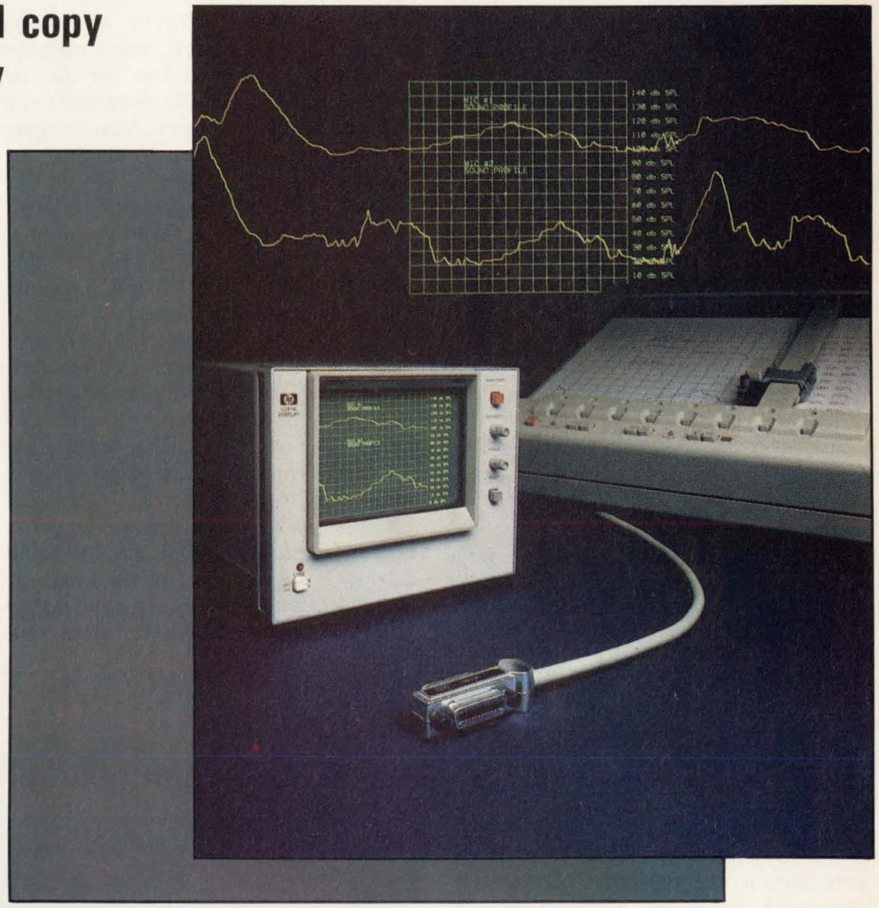
ABLE COMPUTER

CIRCLE 114

Data scrolling joins hard copy in programmable display



The 1347A HP-IB display combines full programmability with high speed vector graphics. Packaged as a self-contained unit, the Hewlett-Packard display has a 6″ (15-cm) directed beam display suitable for rackmounting or bench use. The electrostatic deflection CRT produces realtime graphics with high resolution (2048 x 1513). By using random vector plotting, straight lines and smooth curves can be generated without the discontinuities produced by raster displays.

The ability to scroll through data horizontally and bidirectionally is a key feature of the display. This allows the display of up to 32 waveforms, and the scrolling of graticules as well as text. The extensive memory enables stored data to be scrolled for monitoring and analyzing data. Data displayed onscreen can be duplicated using a plotter; this gives the user a "snapshot" of the scrolled data.

A variety of programmable features provide flexibility. The display accepts both 8- and 16-bit binary commands and ASCII commands from a mainframe or desktop computer. Its ability to decode and display all bus commands allows the display to function as a bus analyzer.

In addition, four programmable writing speeds combined with three programmable intensities provide 12 intensity levels. Four programmable line types are also included. These programming features are used to differentiate parts of complex pictures and data.

A modified full ASCII character set with foreign language extensions and special symbols are stored in ROM. These character data enable characters to be drawn in four programmable sizes and orientations. Since all character data are stored in ROM, just one word needs to be stored in RAM to describe a screen character. This leaves more memory for storing vector information.

The interface language, Hewlett-Packard's Graphics Language, sends graphical information to plotters through a front panel push button or a program command. Hard copy is therefore available for important data, and the need to plot unnecessary data is eliminated.

An 8K x 16 refresh memory enables the display to store over 8000 characters or 4000 vectors. The segmented refresh memory allows up to 64 pictures to be stored. These pictures can be displayed in rapid succession for animation and simulation applications. Comparisons between reference and test data are possible with the segmentation feature.

Reliability and serviceability are provided by 19,000 hours of life testing and periodic environmental testing. Three built-in features that lower service time and cost consist of self-test, continuous diagnostics, and signature analysis. Self-test can be started at any time and tests all internal memory. Continuous diagnostics run recurrently, listing component designators of defective memory ICs onscreen. Signature analysis aids in troubleshooting.

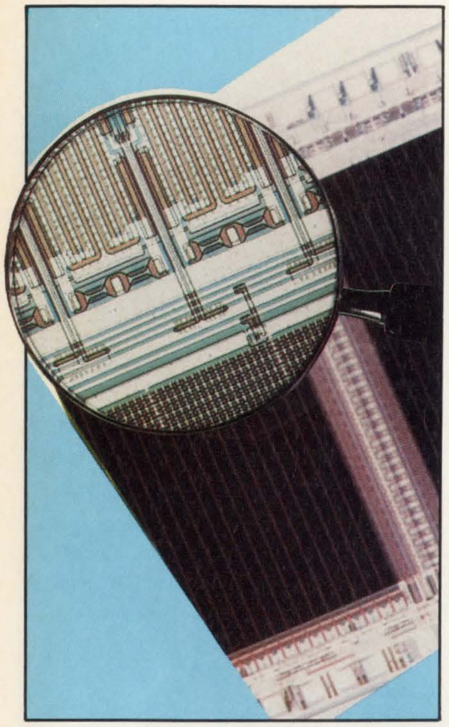
Key applications for the display include ATE systems, process control and monitoring, and measurement and analysis. In ATE systems, the IEEE 488 compatibility allows the display to be easily integrated into a test system. It also consolidates several instrument readings in one location.

Fast update speed and graphics and scrolling capabilities allow the display to be used in process control applications where large amounts of data are stored, displayed, and updated. In measurement and analysis, the high addressable resolution feature allows the display of data, such as voltages, in full range without obscuring slight variations in the voltage plot.

Priced at $5100, the display is delivered within four weeks from date of order. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 260

High density distinguishes speedy EPROM



Speed is often an important factor in a memory device. In a view of this, the Am27256 is a 256K-bit UV EPROM with access times down to 170 ns. Also, the memory chip features redundancy, a fast programming time, and an auto-select mode.

Redundancy is achieved with poly-silicon fuse technology. Spare memory cells are incorporated into the die. At wafer probe, if a bit is found defective, a fuse in the chip is blown. Next, a spare row replaces the row containing the defective bit.

The interactive programming algorithm performs EPROM programming. This algorithm reduces programming time by using short (1-ms) program pulses and giving each address only as many pulses as needed to reliably program the data. The data are then verified. If they do not verify, an additional pulse is applied for a maximum of 25 pulses. The address is then given another 3X-ms overprogram pulse where X is the number of 1-ms pulses required. After the final address is complete, the entire memory is verified. With this algorithm, a typical programming time is 5 min.

In addition, bit locations can be programmed singly, in blocks, or at random. The auto-select mode allows reading the binary code from an EPROM. This code identifies the EPROM's manufacturer and type. The auto-select mode automatically matches the device to be programmed with its corresponding programming algorithm.

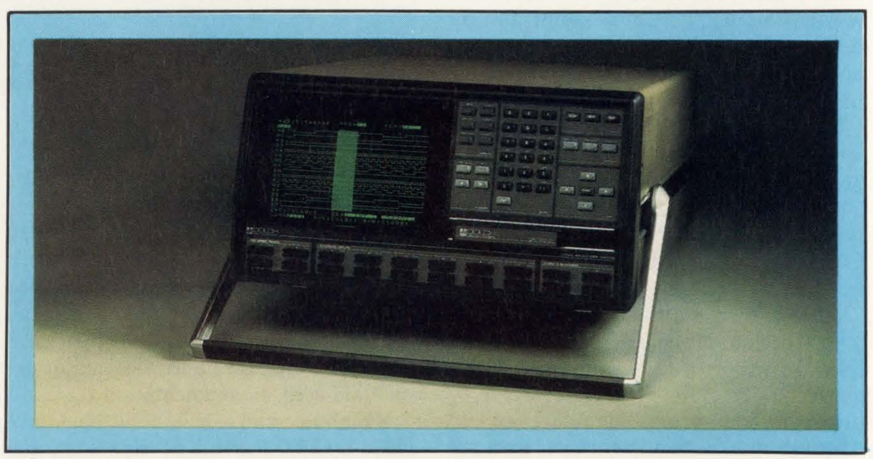
To accommodate multiple memory connections, a 2-line control function is provided. This function serves two purposes: it allows for low power dissipation, and it ensures that output bus contention will not occur. The chip enable control is decoded and used as the primary device-selecting function, and the output enable is a common connection. This means the output pins are only active when data are needed from a particular memory device.

Other features of the EPROM include a 12.5-V programming voltage, fully static operation (and therefore no clocks), and a 10-MHz system operation to increase throughput. By dissipating 525-mW active and 130-mW standby, the chip reduces system power requirements.

Pricing for the EPROM in 100-piece quantities is $197.80 for the 250-ns version and $334.20 for the 170-ns version. **Advanced Micro Devices Inc**, 901 Thompson Pl, Sunnyvale, CA 94086.
Circle 261

Logic analysis system features 64 channels for micro development

Software performance analysis, user friendliness, and a modular system all contribute to the flexibility of the 64300 logic analysis system. Microprocessor/microcomputer development, measurement, and debugging applications can benefit from the logic analyzer's broad range of features.



There are 64 channels in the maximum system configuration (available in 16-channel increments). This includes sixteen 300-MHz (3.3-ns resolution) async channels for timing analysis, and 48 (25/50-MHz) sync/async channels for timing/state analysis. Clocking is performed from a dual time base with three external clocks. The time base captures and correlates independently clocked signals.

A time-saving feature of the system is DataPak, an integrated, transportable mass memory. It automatically stores and loads machine setup parameters and data. This feature allows testing to begin immediately, thus saving setup time. Also, the system offers micro-specific interfaces that feature 2-D triggering. This triggering helps to isolate problems and unravel machine code. Another time-saving feature is the monitor, which follows instructions and execution and tells the user what went wrong and how to correct it.

Standard performance features include multilevel triggering, search and compare, an Up Trace module with full disassembly, and RS-232-C and IEEE 488 interfacing. Software performance features are time stamp, area trace, and histogram.

The prices for the systems range from $7930 for the 16-channel implementation to $14,930 for the 64-channel implementation. **Dolch Logic Instruments, Inc**, 3052 Orchard Dr, San Jose, CA 95134.
Circle 262

Microprocessor system supports up to four users

The microSystem 6/20 is a multi-user microprocessor system designed for small business, departmental, or branch office environments. Compatibility with the entire DPS 6 line is provided, and the computer supports up to four users who can both install and maintain it.

A typical system configuration consists of a Micro 6 processor, 1M byte of main memory, a 5¼" 650K-byte diskette, and a 40M-byte Winchester disk (20M-byte fixed, 20M-byte removable). In addition, the system's five RS-422 ports are adaptable to RS-232 devices. Options include a dual-line async/sync communication controller and a second 40M-byte disk.

The Micro 6 is a 16-bit processor based on LSI technology. This processor enables the system to run a wide range of software used by the company's minis and the single-user 6/10. The software includes office automation packages with document and records processing, thereby allowing users to create office level data bases.

Data Entry Facility II provides communication capabilities to both Honeywell and IBM hosts. The operating system is the menu-driven GCOS 6 MOD 400. It supports transaction processing, data entry, program development, terminal emulation, and communication software.

Communication features enable the system to function as an endpoint serving several workstations in a larger information processing network. It provides DSA and SNA protocols as well as BSC and pre-DSA communications, electronic mail, and teletype emulation.

Three dot-matrix and two letter-quality printers are optional with the 6/20. The dot-matrix printers are available in 80 cols, 100 chars/s; 132 cols, 100 chars/s; or 132 cols, 400 chars/s. The letter quality printers are offered at speeds of 35 and 55 chars/s.

The basic system price is $17,000. Workstation configurations start at $795, and printers begin at $1195. **Honeywell Inc, U.S. Marketing and Service Group**, 200 Smith St, Waltham, MA 02154. **Circle 263**

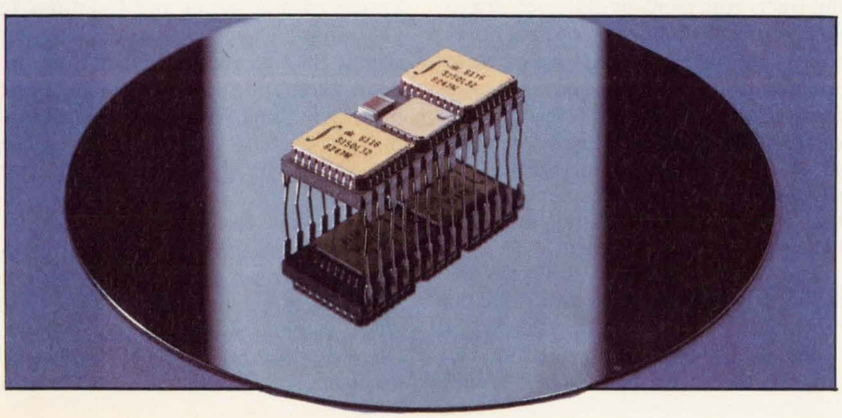
RAM modules combine high speed with low power

A family of 64K-byte CMOS static RAM modules is available in three organizations (8K x 8, 16K x 4, and 64K x 1). The family is based on Integrated Device Technology's line of 16K-byte static RAMs that are fabricated using the proprietary CEMOS I process.

Each 64K-byte module is constructed on a ceramic substrate using four 16K-byte RAMs in leadless chip carriers. Using an onboard decoder circuit to interpret higher order addresses achieves functional equivalence to a monolithic 64K-static RAM. The 8K x 8 modules are available in two pinouts: IDT7M864, a 64K-byte RAM, or IDT8M864, a 64K-byte EPROM.

In 28-pin DIPs, the modules feature 120-, 150-, and 200-ns military speeds and 85-, 120-, 150-, and 200-ns commercial speeds. The IDT7M464 in the 16K x 4 configuration features 65-, 85-, and 100-ns military speeds and 55-, 65-, 85-, and 100-ns commercial times. The IDT7M164 (64K x 1 configuration) provides 100-ns military access and 70-ns commercial access. The latter two devices are available in 22-pin, 300-mil pin center DIPs.

Performance and reliability are achieved through the CEMOS I dual-well fabrication process. Traditionally, CMOS solves the high junction temperature and heat dissipation limitations of other technologies, but does not provide sufficient speed. The CEMOS I process uses readily producible die sizes with 2.5-μm geometries.



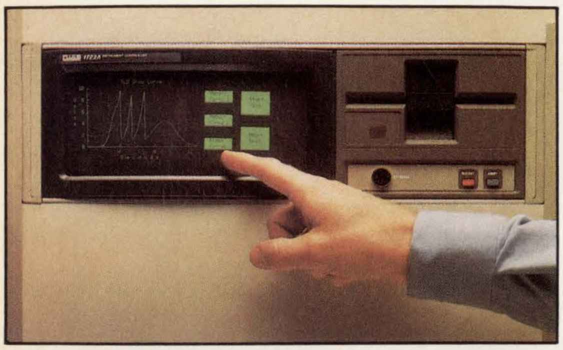
In addition, the use of double polysilicon layers allows stacked polyload resistors on top of memory cell transistors. This creates a cell size of 1.1 square mils. The process architecture dual-well structure solves the soft error problems associated with fast static RAMs.

Moreover, the CEMOS I process offers several distinct characteristics. An inverter that drains current only during switching accomplishes a lower power performance than NMOS. This low power consumption allows denser VLSI products. Design flexibility contributes to a high noise margin.

All I/Os are TTL compatible and operate from a single 5-V supply. Full operating power is less than 0.5 W; full standby consumption is 5 mW and 2-V battery backup data retention power consumption is below 4 μm. The async circuitry requires no clocks or refreshing.

The 8K x 8 version is priced at $200 in 100-piece quantities. The 16K x 4 version starts at $275; the 64K x 1 version starts at $260. **Integrated Device Technology**, 3236 Scott Blvd, Santa Clara, CA 95051. **Circle 264**

Specialized microcomputer system is at instrument controller core



The 1722A instrument controller was designed with industrial applications in mind. This 16-bit microcomputer-based system is optimized for automating factory test and process control systems. It is particularly well suited for applications in which unskilled personnel operate complex systems.

Once the controller is programmed, the user can remove the keyboard and operate the system from the display. The 80-char x 16-line CRT is touch sensitive and divided into 60 fingertip-sized areas. Combining display enhancements (highlighting, blinking, and reverse video) with 640 x 224 dot-addressable graphics allows large amounts of information to be communicated quickly. These capabilities also permit intricate displays that guide operators through complex test routines.

To allow software compatibility with other controllers in the series, the controller is based on the TMS99000. In addition, the chip has Macrostore and a high processing speed. Macrostore allows extensions to the processor instruction set, and its 8K bytes of RAM contain single- and double-precision arithmetic functions.

The 136K-byte system memory is expandable to 2.6M bytes using RAM expansion modules. Allocating part of the memory to an electronic disk allows faster program execution. Data arrays and program overlays stored in this manner are accessed faster than in either disk or bubble memory. Also available is a 400K-byte double-sided, double-density, floppy disk drive.

Standard interfaces include an IEEE 488 and an RS-232-C. The system has room for three additional interface cards. One has both IEEE 488 and RS-232-C; one has a dual RS-232-C card with high speed buffering capability; and the other has a dual 16-bit parallel interface for older or custom instrumentation interfacing.

An enhanced BASIC interpreter with over 25 extensions is the standard language for the instrument controller. The extensions initialize different bus functions using 1-word commands. Other language options include a BASIC compiler, FORTRAN, and assembly language. With the compiler, subroutines from FORTRAN and assembly can be linked into one BASIC program.

Starting at $7450, the controller includes the BASIC interpreter and full documentation. A limited 1-year parts and labor warranty is also provided. **John Fluke Mfg Co, Inc**, PO Box C9090, Everett, WA 98206. **Circle 265**

High performance Pascal compiler operates under Unix-based 68000s

A Pascal compiler that is fully integrated into the Unix operating system on the MC68000 produces code that is smaller and faster than C, FORTRAN 77, or other Pascals on Unix. Using Pascal-2 has two main advantages. First, vendors of Unix-based systems now have access to Pascal-trained programmers. Second, existing Pascal applications can be transported to Unix from other operating systems. Ultimately, this should result in a larger software base for Unix.

The software consists of a compiler, a debugger, a profiler, and utility programs. Operating in five phases, the compiler uses a virtual memory system to compile large programs. There are nine types of optimizations: global register allocation, range tracking, constant folding, dead-code elimination, short-circuit evaluation, expression targeting, array index simplification, branch-tail merging, and common subexpression elimination.

Conforming to the proposed Pascal standard, the compiler offers standard Pascal capabilities at level 0 and conformant array parameters at level 1. The Pascal-2 language includes several extensions. An external procedure compiles separate Pascal procedures; a non-Pascal external call uses the standard C calling sequence; and an include directive combines multiple source files. I/O extensions include random access files and additional parameters to specify external file names.

All error checking is done in the first two phases of compilation. Type compatibility checks ensure that data types conform, while other checks detect uninitialized variables and other errors normally found during execution. Runtime checking detects array index errors, subrange assignment errors, nil pointer references, nonexistent case labels, and I/O and arithmetic errors.

Running as a separate process, the debugger allows the programmer to solve logic errors interactively at the source level. Control capabilities include full trace, statement-by-statement execution, and any number of control breakpoints that the block name and statement number identify. Runtime errors transfer control to the debugger for problem identification. Debugger data commands permit display and/or modification of all existing variables. The debugger can also write a complex array or record structure with one statement.

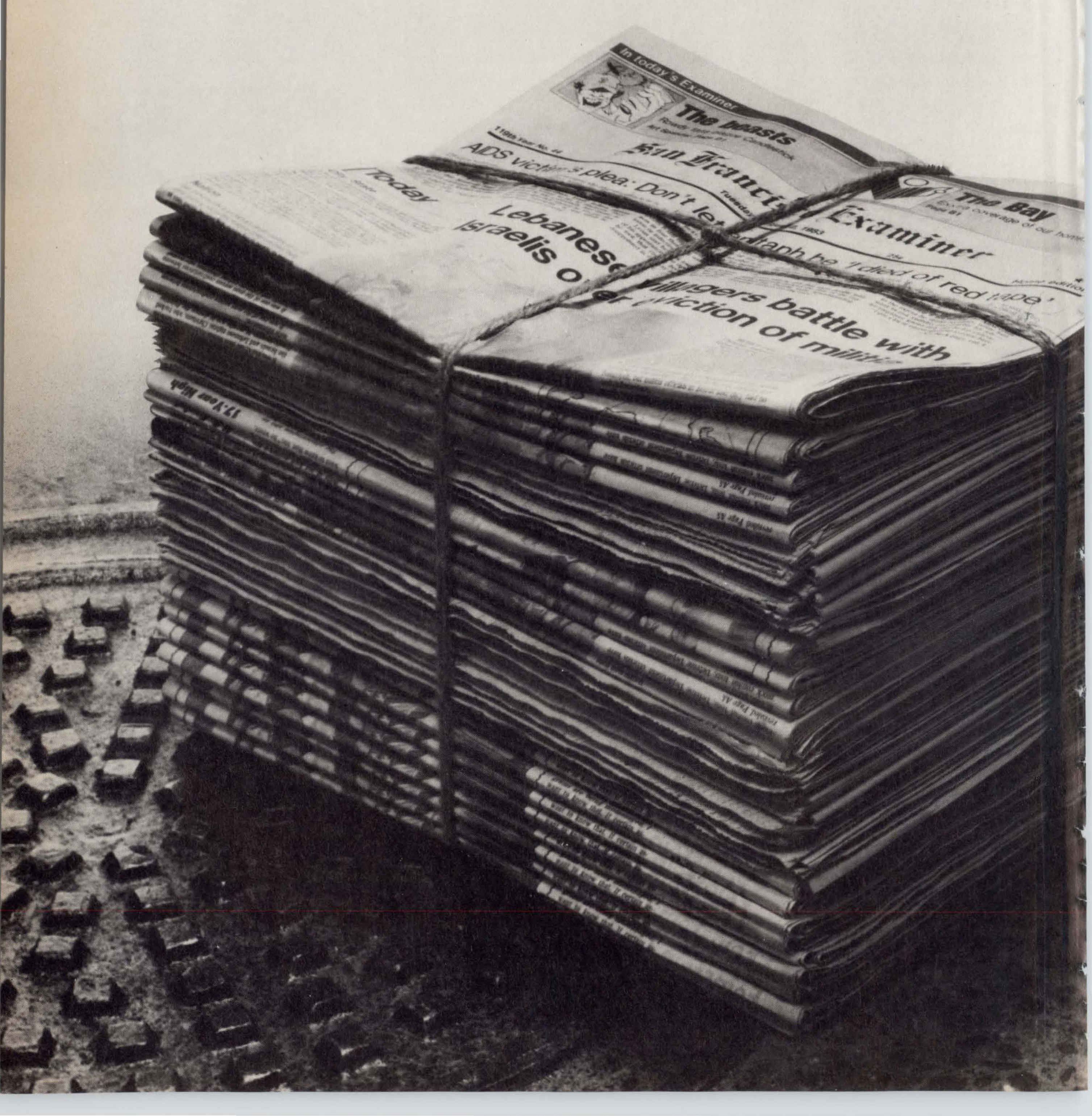
The profiler is a measurement tool that points to program sections that can be reorganized for greater efficiency. It counts each statement executed in every program block and then displays a modified listing with the actual execution count attached to each source line. Each procedure and function is summarized, and the percentage of the execution count is indicated.

Utility programs help the application programmer with development, maintenance, and documentation. The PASMAT and PB source formatters automatically create a consistent and readable program structure. Cross-reference generators include XREF, which displays an index showing each identifier and its uses; and PROREF, which displays an index of nesting structures and identifies the procedure calls for each program block.

The dynamic STRING library is a collection of procedures and functions for programming with dynamic character strings. PROSE, the test formatting program, contains directives that specify page layout and paragraph conventions. It can automatically number pages, place titles, justify margins, and create an index.

Licensing fee for the complete Pascal-2 Unix system, including the debugger, other tools, and a year of software support, is $1650. The compiler, purchased separately, is $600. **Oregon Software**, 2340 SW Canyon Rd, Portland, OR 97201. **Circle 266**

Our UNIX Super UPI Cover



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And that our 83/20 includes full UNIX* System III with Berkeley enhancements like C-shell and Visual Editor.

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CIRCLE 116

Membrane keyboard

A full-travel membrane keyboard, the KS-500E is rated at 10M cycles. Keys have a 0.140" (3.556-mm) nominal stroke. Typ bounce is less than 1 ms, with a 5-ms max bounce over the switch's life. The custom keyboard meets DIN standards and has an overall home row height of 18.3 mm. The monolithic housing, molded as one piece, eliminates key-switch alignment problems. The keyboard offers protection against spills and other contaminants since the screened circuit traces and contacts are laminated between two pieces of polyester. In quantity, price is under $0.30 per station. **Stackpole Components Co,** Box M, Farmville, VA 23901. **Circle 267**

Current loop optocouplers

Optocouplers designed for use in 20-mA current loop systems are available as a transmitter (HCPL-4100) or a receiver (HCPL-4200). Features contributing to performance include precise thresholds with hysteresis for consistent, noise-free performance, isolated loop electronics powered by loop current, and a 19.2k-baud rate plus speed capability. An internal shield in both products provides rejection to common mode interference of typ 10k V/μs at 25 °C. The current loop transmitters are $6.65 each in 1000-piece quantities; the receivers are $6.15 each in the same quantity. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303. **Circle 268**

Illuminated indicators

The Compu-Lite series 200 are illuminated push buttons and indicators. Rated at 5 A at 250 Vac, the switch line is designed for snap-in panel or PCB mounting. Fingertip-removable switch caps and built-in lamp extractors allow easy replacement of lamps from the front panel. Other features include LED and incandescent illumination, full or split legend caps, various colors, and gold contacts for low-level switching. **Eaton Corp, Aerospace/Commercial Controls Div,** 4201 N 27th St, Milwaukee, WI 53216.
Circle 269

Compound curve rocker switch

The Curvette rocker switch has a soft, glare-free matte finish and a compound curve bezel that blend into the panel. It features an integral pin design in which the spring creates contact pressure and dissipates heat. The device has been tested for up to a 75-A inrush and can withstand 50k actuations minimum, at full load. A mounting ear design lets the switch fit in any opening from 0.48" x 1.072" (1.22 x 2.723 cm) to 0.55" x 1.125" (1.40 x 2.858 cm). **Carlingswitch, Inc,** 505 New Park Ave, W Hartford, CT 06110.
Circle 270

Programmable keyboard encoders

The KB3600 series are low cost microprocessor-based keyboard encoders. Std features include n-key rollover, 9 output data bits, and pulsed data ready signal with 5.4-ms debounce. Two versions are available: a std ASCII-coded typewriter keyboard version and a PRO version that provides binary output code when any key is depressed. The devices are compatible with TTL/DTL or MOS logic. Units can be custom programmed from customer supplied key codes to meet specific needs. The encoders are priced at $2.30 in 25k quantities. **General Instrument Corp, Microelectronics Div,** 600 W John St, Hicksville, NY 11802.
Circle 271

IC relay

ChipSwitch is a solid state relay that uses high voltage monolithic circuits. The device is composed of three elements: two identical output power ICs and an LED. Based on solid state switch with zero cross technology, the relay offers improved performance characteristics. These include a dv/dt spec of 600 V/μs, off-state leakage of 10 μA max; min load current is 0.5 mA, and 1 cycle surge is 30 A. The device operates from 5 to 280 Vac with pickup at 5 mA, 10 mA, or 3.5 Vdc, depending on model. Prices range from $7.45 to $10.45 in 100-piece quantities. **Crydom, a div of International Rectifier,** 1521 Grand Ave, El Segundo, CA 90245. **Circle 272**

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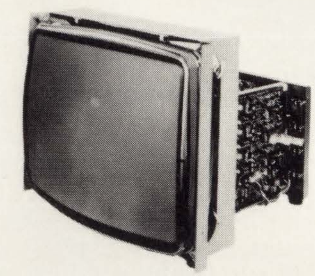
CIRCLE 118

LED indicators

The HLMP-5000 series of indicators are right-angle LED lamps. They are designed to be used as back-panel diagnostic indicators and PCB logic status indicators. Incorporating the existing range of T-1 ¾ LEDs, the lamps provide the design engineer with a color choice of high efficiency red, std red, yellow, and high performance green. All are available with or without a current-limiting resistor. The black-plastic design allows flush seating on the PCB. The LEDs can be end stacked on 6.35-mm centers. In 1000-piece quantities, prices range from $0.29 to $0.50. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303. **Circle 273**

Graphics monitors



The CD series consists of high resolution color display monitors for computer graphics and data. The monitors are raster scan, RGB units with inline gun CRTs. They have a displayable pixel range from 720 x 256 to 1024 x 1024. Obtainable in both 13- and 19-V models, applications for the devices include simulation, CAD/CAM, and process control. The CDA models feature wide frequency range analog video amps, while the CDB models feature digital video amps. Other specs include a 0.31-mm dot-trio pitch and horizontal-deflection frequencies from 28 to 36 kHz. **Ikegami Electronics (USA), Inc,** 37 Brook Ave, Maywood, NJ 07607. **Circle 274**

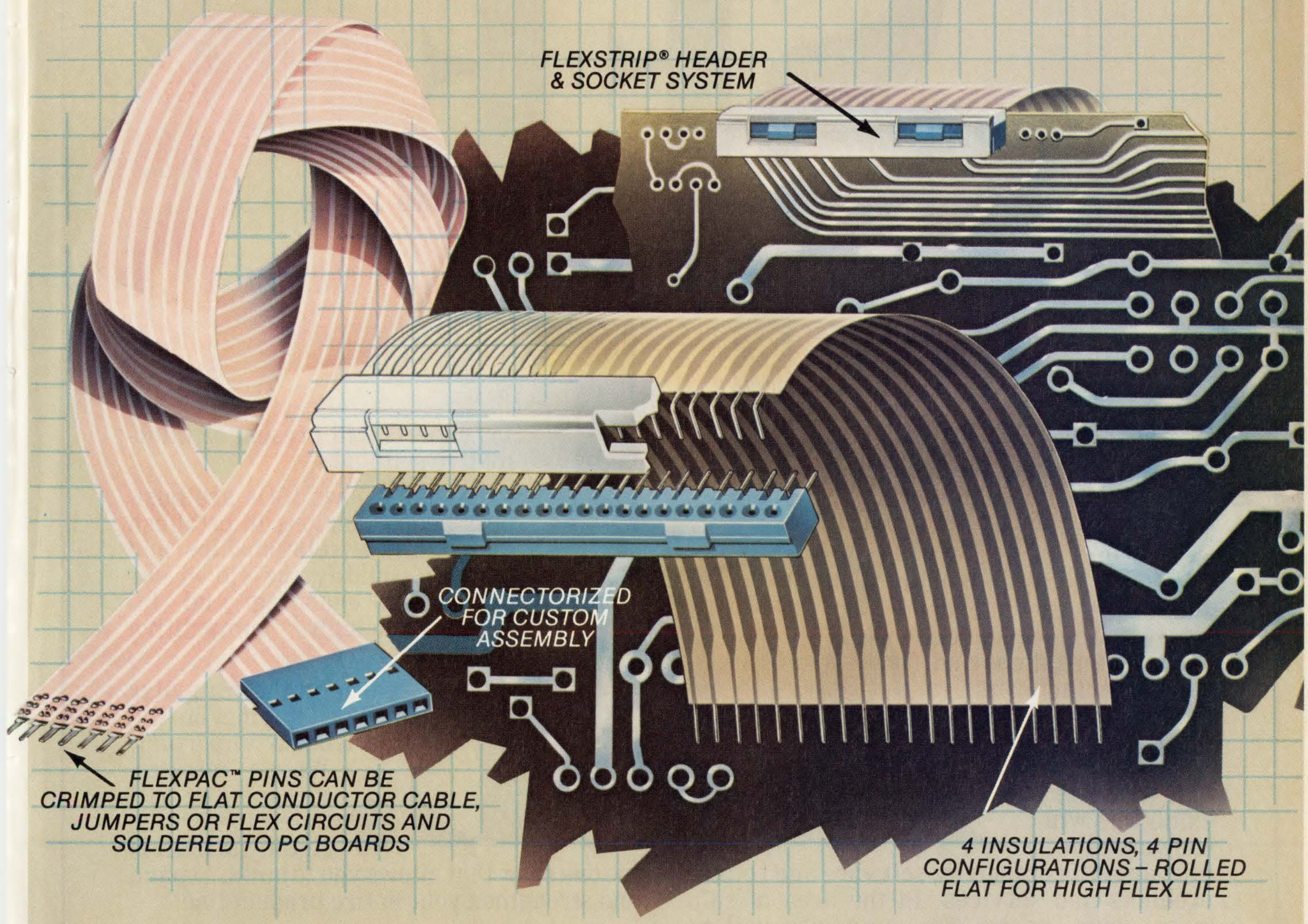
Single-key switches

Miniature TACT switches are available in 2 basic types: series KH (mechanical contacts) and series KE (conductive rubber contacts). Both types offer std single-pole, double-pole, transfer circuit, double-action and built-in LED. Specs include operating life ratings of 3M cycles, max bounce of 5 or 10 ms, and contact rating of 50 mA at 12 Vdc and 1 mA at 36 Vdc. The switches have an operating force of 75 g and a stroke travel distance of 0.25 to 1.0 mm. Outline sizes are 6 x 6 mm, 8 x 8 mm, 10 x 10 mm, and 12 x 12 mm. **Alps Electric (USA), Inc,** 100 N Centre Ave, Rockville Centre, NY 11570. **Circle 275**

4-LED board array

LED arrays (series PCL1254) are available in any combination of 1 to 4 colors: red, amber, yellow, and green. The arrays, with LEDs spaced on 0.17″ centers, are constructed of black, glass-filled nylon for temp stability. They include 3 standoffs for clearance from the PCB. With diffused lenses and 20 mA of drive current, typ light outputs for red LEDs are high efficiency 18 mcd, super bright 8 mcd, and medium bright 5 mcd. The PCL1254 series prices range from $1.28 to $2.12. **Data Display Products,** 303 N Oak St, Inglewood, CA 90302. **Circle 276**

Advanced packaging flexibility from Ansley Electronics.



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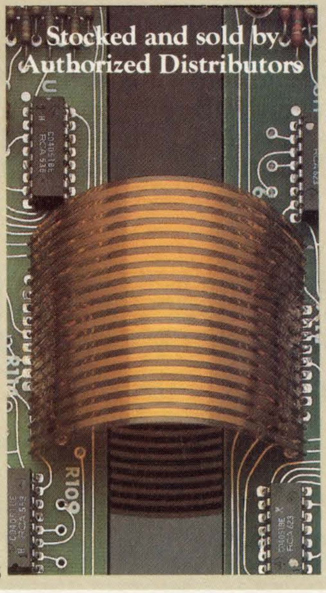

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CIRCLE 120

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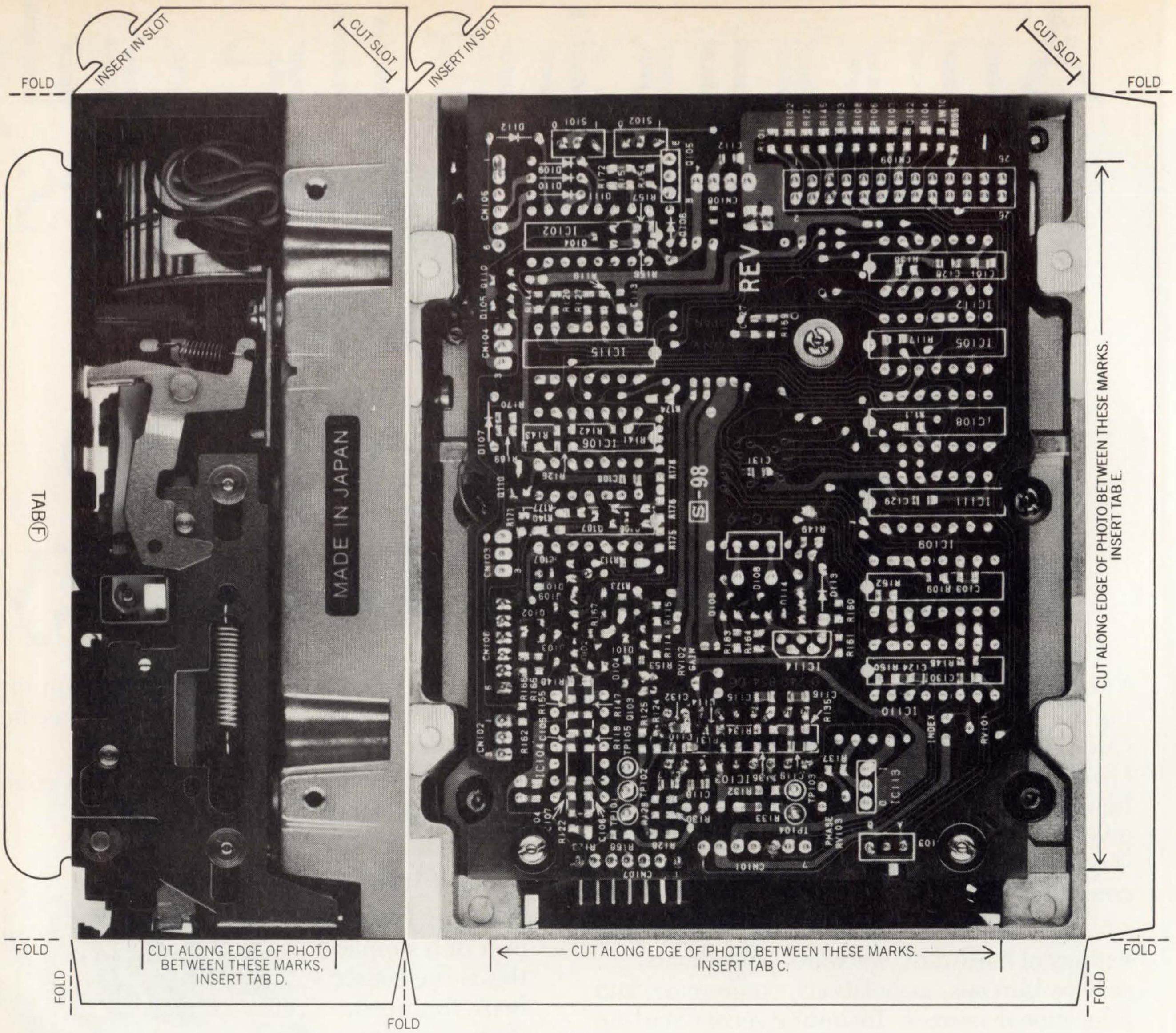
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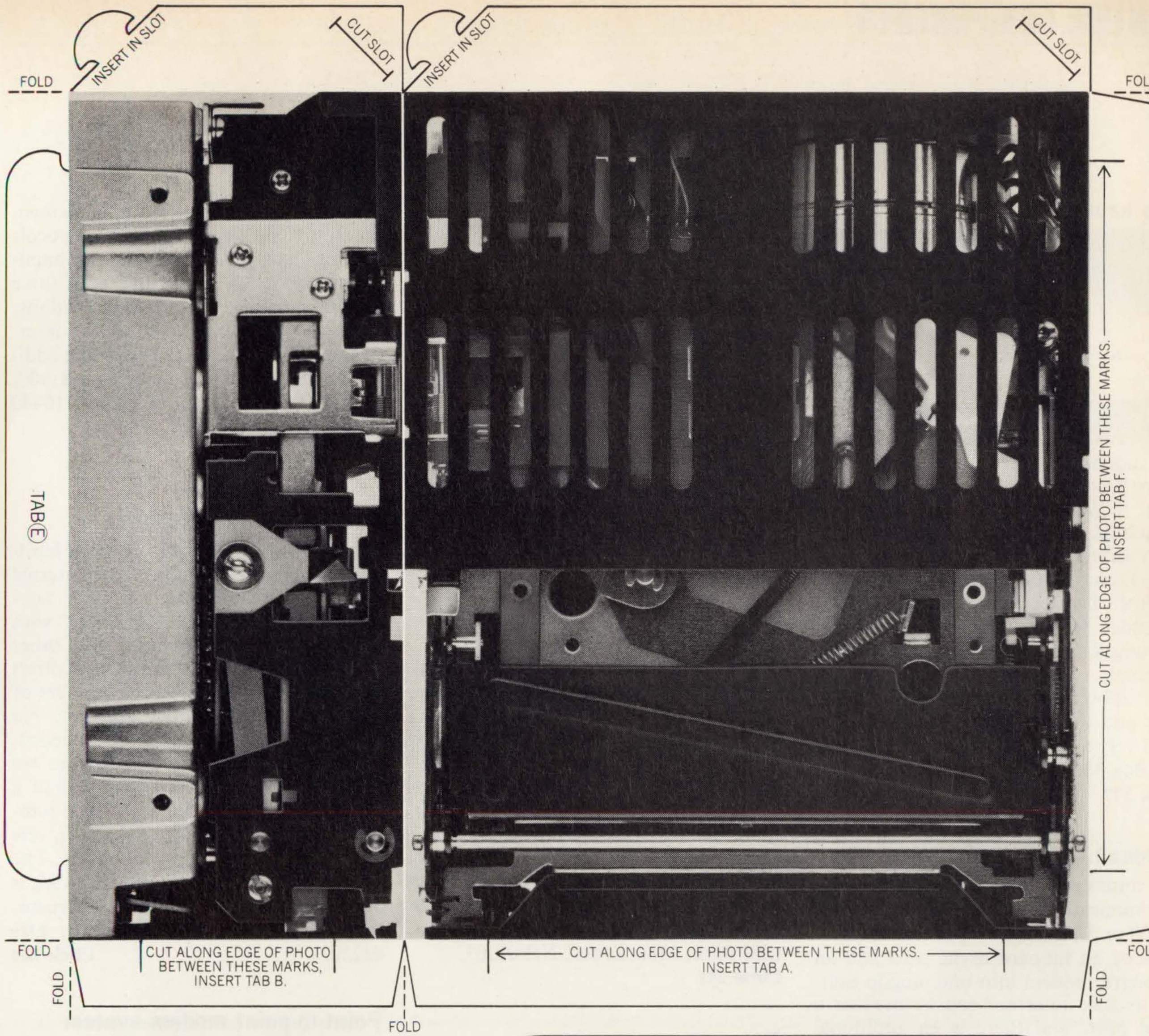
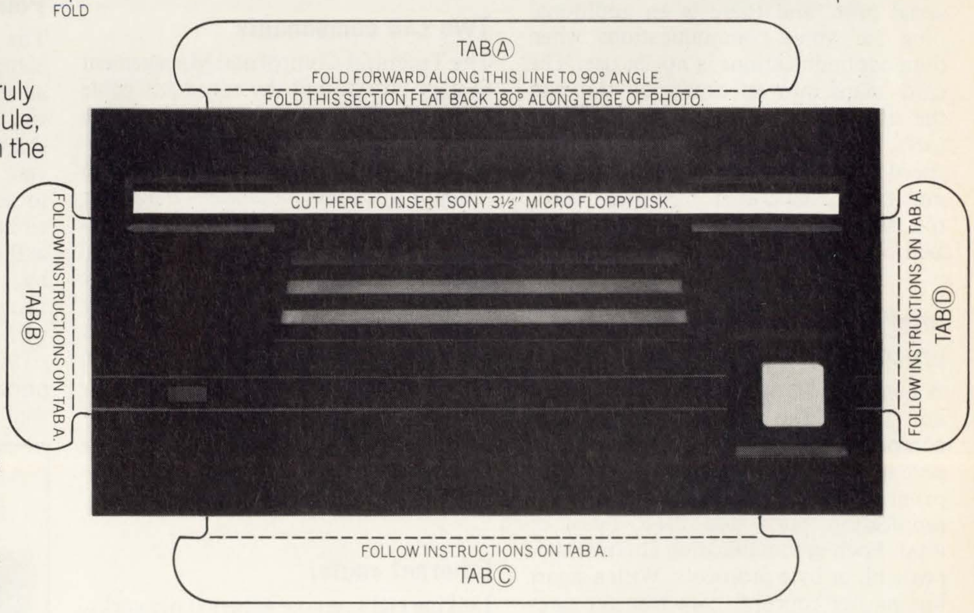
ACTUAL SIZE
SONY
Micro Floppydisk
Double Sided





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CIRCLE 124

Line expander

The model 6641 series line expander is an active baseband repeater. It allows a network to operate in star, extended star, multidrop, or combination star and multidrop arrangements. In a star configuration, a coax cable connects the expander to a MUX. Longer coax cables link the expander to four remote MUXes that demultiplex the data for distribution to terminals. An extended star arrangement allows more distance between the MUX and the repeater; total distance is 3000′. The device is priced at $250. **3M**, PO Box 33600, St Paul, MN 55133.
Circle 277

Communication card for IBM PC

Ideacomm 1200 is a plug-in card offering communications with the IBM PC. It runs at 300 or 1.2k baud and combines functions of an inboard async card and an outboard modem into one plug-in unit. An RS-232-C interface can be used as a serial port, and there is an additional plug for voice communications when data communications is not in use. The card snaps into an expansion slot and the user plugs in a modular telephone jack. There are no switches to set, and speed is software selectable or automatically selectable by the card. **IDEAssociates, Inc**, 7 Oak Park Dr, Bedford, MA 01730. **Circle 278**

Intelligent communication processor

A communication processor for PDP-11s and VAXes, the ICP 1600 features code compatibility with the host instruction set. A single hex-height card has eight programmable sync/async serial communication ports and 256K bytes of RAM. Each communication channel supports bit or byte protocols. With a smart bus master concept, DMA transfer rates are achieved between processor and host memory with minimal bus contention problems. An optional device implements the data encryption std. **Simpact Associates, Inc**, 5520 Ruffine Rd, San Diego, CA 92123. **Circle 279**

Stat MUX/modem combination

Functioning as a 2-channel stat MUX and a modem, the 2X212 Modemplexer is 212A compatible. The full-duplex, 1.2k-baud device is designed for timesharing operations since it enables two remote terminals to transmit on one line. It features auto dial/answer, auto redial, and auto selection of correct dialing mode. The device also provides speed dialing, stored number directory (up to 10 numbers), continuous memory, and dynamic buffering of up to 3000 chars/port. The modem is priced at $995. **Omnitec Data, Inc**, 2405 S 20th St, Phoenix, AZ 85034.
Circle 280

Mini couplers for fiber optics

The MC series of mini optical directional couplers is designed for taps or feeds in digital and analog fiber optic systems. The couplers' dimensions are 50 x 11 x 8 mm and they weigh less than 1 oz. They are available in the step or graded index fiber with 0.5-m fiber leads for splicing into fiber optic cable systems. Characteristics of the devices include low insertion loss, high directivity, and various splitting ratios. **Phalo/Optical Systems Div**, 900 Holt Ave, East Industrial Park, Manchester, NH 03103.
Circle 281

Two LAN components

The Technical Control and Management System (TCMS) and the CMUX-3270 cable MUX are two LAN components. The TCMS is a menu-driven system that provides network managers with tools to monitor operating parameters and detect failure and service degradation. Consisting of a monitor and a database management system, the TCMS provides status reports that it combines with data management information. The cable MUX is an interface device linking IBM 3270 peripherals with an IBM 3274 control unit. The TCMS is priced at $7500 and the MUX is priced at $3375. **Wang Laboratories, Inc**, 1 Industrial Ave, Lowell, MA 01851.
Circle 282

Ethernet router

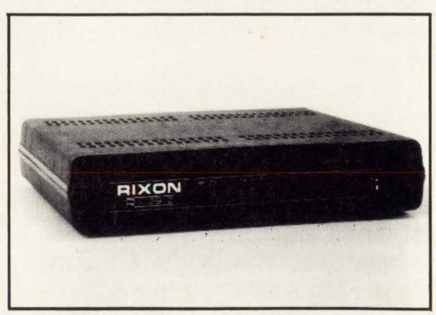
Linking eight remote Ethernet networks, the GS/3 Internetwork Router uses a common point-to-point connection media. The communication processing system supports from two to eight communication lines with a max aggregate data rate of 304k bps in the fully configured system. It has the full implementation of the XNS transport protocols and uses RS-232/423 or 422 sync communication ports. The unit consists of three logical modules for communications, Ethernet interfacing, and serial interfacing. The GS/3 is priced at $9900; additional communication lines cost $1900. **Bridge Communications, Inc**, 10440 Bubb Rd, Cupertino, CA 95014.
Circle 283

Internal IBM PC modem

The PM-300 is a 300-baud modem hardware package designed for internal mounting in the IBM PC. This FCC-certified modem is compatible with Bell-103, COMPAC software, and other IBM PC communication software. It offers auto answer with a selectable number of rings before pickup and dial out. No RS-232 cards or connectors are needed. The modem and COMPAC software are sold as a system. COMPAC consists of a videotex program to support async communications. It has auto log on, file download, and upload capabilities. The system sells for $249.95; the software is available separately for $69.95. **Avcom, Inc**, PO Box 29153, Columbus, OH 43229. **Circle 284**

Point-to-point modem system

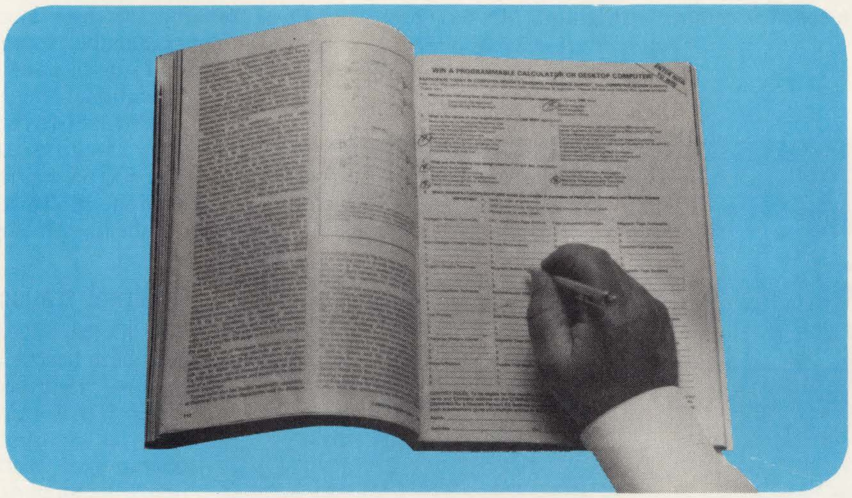
The RV.29/2 is a full-duplex V.29-compatible sync modem system. It has an integral line contender that allows a single DTE or two collocated DTEs to share one 3002 unconditioned 4-wire private line. The first DTE to raise "request to send" gains control of the transmit circuitry. The system normally operates at 9.6k bps, but it will operate at the fallback rate of 4.8k bps if necessary. The LSD-6C line-saving device can be used with the system when more than two DTEs are used. The modem system is priced at $2495. **Rixon Inc**, 2120 Industrial Parkway, Silver Spring, MD 20904.



Circle 285

Take a Few Minutes to HELP OUR EDITORS HELP YOU

YOU MAY WIN A VALUABLE PRIZE IN THE PROCESS

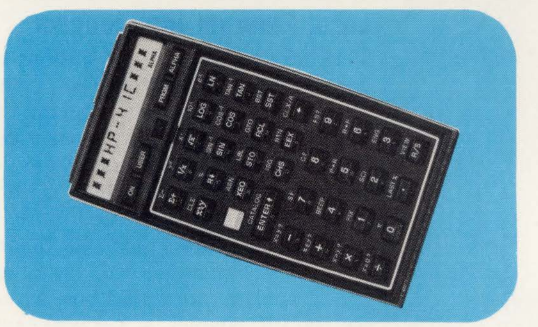


In every issue of *Computer Design* you'll find a bound-in survey questionnaire entitled "Designer Preference Survey." Your participation in these surveys is important. Your answers are significant. They tell our editors what's going on in the marketplace, what kinds of systems you are designing, how your product choices are shaping up, what products, subsystems, equipment and components you are using or would like to use.

The answers you supply can guide our editors in selecting the topics, features, and technical data that will be on target with the kinds of projects you are working on.

The questionnaires also alert manufacturers to your needs. The inputs you give us help them to develop products with the speeds, ranges, capacities, etc. that you require.

As an added incentive, each questionnaire returned gives you a chance to win a valuable prize. Drawings are made each month, with a grand prize drawing at year end.



MONTHLY DRAWING
HP 41C
PROGRAMMABLE CALCULATOR

The HP 41C offers advanced problem-solving power yet is easy to use. Communicates in words as well as numbers. Can be programmed to meet your specific needs. Fifty-eight popular functions, 130 total operations in function library. You can add peripherals and extension modules to expand capabilities.

ANNUAL DRAWING
HP 85
DESK TOP COMPUTER

This portable (20#) unit includes an alphanumeric keyboard, tape drive, thermal printer, built-in 56 K byte memory, CRT screen, and 150 built-in HP BASIC language commands. You can add peripherals and software packages to expand system capability. A $2800 value!

COMPUTER DESIGN

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Statistical MUX series

The Multi-MUX series of stat MUXes are available in 1-, 2-, 4-, and 8-channel versions. Both point-to-point and multipoint networks are supported. Channels accept async data at any speed up to 9.6k bps for transmission over a single sync full-duplex link. Total peak input rate is 19.2k bps. Auto speed selection, dynamic buffer allocation, and CRC error detection/correction are provided. Complete diagnostic capabilities with local, remote, and self-test are available as well as seven system status indicators. The 4-channel version is $1295 and the 8-channel version is $2095. **Multi-Tech Systems, Inc,** 82 Second Ave SE, New Brighton, MN 55112. **Circle 286**

Interfacing MUX

The SCD-DZV11 is a microprocessor-based, 8-line MUX for the EIA/CCITT V.24 interface. The dual-wide, async MUX supports RS-232-C terminals or remote lines and plugs directly into LSI-11 Q-bus-based systems. It has jumper-selectable address and vector assignments. In addition, it uses modem control and programmable speed for character length and stop bits and is compatible with DEC operational and diagnostic software. Included are two cables with 40-pin berg to four 25-pin RS-232-C female connectors. The 100-piece price is $715. **Sigma Information Systems,** 6505 Serrano Ave, Anaheim, CA 92805. **Circle 287**

Ethernet transceiver

The model 2010EB transceiver operates with both heartbeat and watchdog timer features. Heartbeat circuitry allows the transceiver to inform the connected station that collision detection circuitry is operational. Watchdog timer circuitry limits the amount of data sent out in a particular packet by cutting off the signal after 60 ms. The transceiver operates at a 10M-baud data rate. It features a self-adjusting spring-action stinger that maintains contact with the center cable conductor. The model is priced at $232.80. **TCL Inc,** 2066B Walsh Ave, Santa Clara, CA 95050. **Circle 288**

Local Ethernet interconnect

This device permits eight stations to be connected to an Ethernet LAN, or it can be used as a standalone system. Called the DELNI, it accepts transceiver cables from Ethernet communication controllers and can be attached to the network through a dedicated port. The interconnect follows the CSMA/CD protocol and is compatible with the Ethernet spec. The data rate is 10M bps. An external switch enables a network system manager to partition grouped stations into standalone stations for running applications that require either security or performance testing. The unit is priced at $995. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754. **Circle 289**

October Preview—
A Special Report on microprocessors and microcomputers.

IF ENOUGH GOOD ENGINEERS AREN'T MADE IN AMERICA, WHAT WILL BE?

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FRANCE

And that requires money—money to help American colleges fight skyrocketing costs.

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Solutions In Silicon

Single-user operating system

The CP/M 8-16 operating system is a proprietary implementation of CP/M-86 Version 1.1. It is designed to operate with 8085/8088 based System 816 computers. The single-user system allows both 8-and 16-bit applications programs to run on the same microcomputer. Dual-processor architecture runs directly on the processor, not in emulation mode. System throughput is increased with the interrupt-driven DMA floppy and hard disk controllers and by the proprietary M-Drive/H solid state disk memory device. The operating system costs $450 with software upgrade available for $150. **CompuPro,** Oakland Airport, CA 94614. **Circle 290**

Operating system for Eclipse®

Sphinx is a Unix-based operating system for the Eclipse® computer family. The system is compatible with the system III version in form, content, interface, and documentation. Software features include enhanced software development through the source code control system and high-level AOS/VS programming. It offers the Unix capability of pipes and filtering, where pipe is a command string acting as an interface for data filtered between programs. The software price is based on the number of users and ranges from $9845 for 16 users to $27,845 for more than 64 users. **Data General Corp, Information Systems Div,** 4400 Computer Dr, Westboro, MA 01581.
Circle 291

Pascal version

Micro Concurrent Pascal (MCP) is a high level language for programming realtime embedded systems. The MCP provides process, monitor, and class constructs for Concurrent Pascal. It introduces the device-monitor constructs permitting hardware interaction directly from the software. Programs compile into pseudo-code (P-code) that can be either interpreted or native assembly language code. Designed for microprocessors, the p-code is reentrant, relocatable, and completely PROMable. Features include interrupt handling capabilities and separate compilation and assembly language routine calls. **Enertec, Inc,** 19 Jenkins Ave, Lansdale, PA, 19446.
Circle 292

VME/68000 operating system

VMEFORTH/32 is a realtime operating system that uses the capabilities of the 68000 and 68010 processors in a VMEbus configuration. The 32-bit language system allows users to perform 16-, 32-, and 64-bit mathematical operations. Features include direct address to 16M bytes of memory with no paging, control from the resident system with no overlays, 2000G bytes of directly accessible disk storage capability, 230K bytes of user program space in a 256K partition, and unlimited size of user partitions. Full 32-bit operating system capability includes 32-bit stacks, 32-bit wide I/Os, 32-bit addressing without degradation, and 32-bit precision for math primitives. **Astraea Computer Corp,** 846 Del Rey Ave, Sunnyvale, CA 94086.
Circle 293

SYSTEM COMPONENTS/ SOFTWARE

Streaming software for TI 990

A streaming software utility package, the Stream DX10 is designed for the TI 990 minicomputer line. The standalone software allows continuous transfer of data from disk to tape. It streams DX10 compatible disks to formatted drives as fast as 100 ips, 1.6k bpi via a multifunction tape controller. Software uses a sector map for a continuous rather than a broken reading process. Error handling is a std feature in which the utility will check data 25 times for verification. The software is available on TI/ANSI compatible 800- or 1.6k-bpi mag tape for a 1-time $500 charge. **Spectra Logic Corp,** 1227 Innsbruck Dr, Sunnyvale, CA 94086. **Circle 294**

IBM PC/Unix software link

The FUSION version 2.0 network software links MS-DOS-based IBM PCs to 8086, 68000, 16032, PDP-11, and VAX processors. The software applies to systems running Unix and Unix-like operating systems on an Ethernet LAN. It incorporates a complete implementation of Xerox's XNS internet transport protocols and provides file transfer, virtual terminal, and network utility programs. The file transfer program allows the user to move groups of files or directory hierarchies between PC and Unix systems with a single command; the virtual terminal function allows remote log in. **Network Research Corp,** 1964 Westwood Blvd, Los Angeles, CA 90025.
Circle 295

I/O software for IBM PC

PCLAB and PCTHERM are realtime software for analog and digital I/O interfaces. They complement the line of plug-in data acquisition hardware products for the IBM PC. Both are libraries of routines to be called from BASIC under PC-DOS. The packages consist of two parts: a save module, which contains machine language routines to be called from IBM BASIC, and a set of standalone data acquisition and control utilities. Single-unit price for PCLAB is $495; for PCTHERM, $695. Both are on single-sided, single-density (160K-byte) floppy diskette. **Data Translation,** 100 Locke Dr, Marlboro, MA 01752. **Circle 296**

Onchip operating system

Micro-51/OS is an onchip, realtime, multitasking operating system. Designed for realtime control applications in consumer and industrial products, it operates on the 8051 family of single-chip microcomputers. The operating system allows up to 16 application tasks to execute in a single-chip or expanded hardware environment. Available on diskette or EPROM, the $750 package includes a complete user's guide and examples of application tasks. **Micro Computer Control,** PO Box 275, Hopewell, NJ 08525.
Circle 297

IBM-compatible workstation

A color raster workstaiton, the DC/4250 is driven by a controller that executes both the IBM 3250 graphics command set and a color raster set of extensions. The workstation is packaged in an ergonomic console and features a 19" display monitor with 1024 x 1024 resolution. A 4096-color palette is available from which 16 colors can be chosen for simultaneous display. Image refresh is generated with a 20-MHz (50-ns) pixel writing rate. A 1280 x 1024 resolution is available optionally, as is refresh buffer memory expansion to 128K bytes. In a typ configuration, the workstation sells for less than $43,000. **Adage, Inc**, 1 Fortune Dr, Billerica, MA 01821
Circle 298

Unix floating point option

The FPP-8/01 is a 2-board floating point processor option for the System 8000 family of supermicros. Implemented in hardware with bit-slice architecture, the boards meet the IEEE std for binary floating point arithmetic. It offers performance of 0.12M flops and performs all internal operations in double-extended precision with a 19-decimal digit accuracy. It operates on floating point numbers ranging from 10^{-4932} to 10^{4932}. The boards consist of five functional units: the ZBI interface unit, microcode sequencer and control store, sign engine, exponent engine, and fraction engine. The set is priced at $5450. **Zilog Corp**, 1315 Dell Ave, Campbell, CA 95008. **Circle 299**

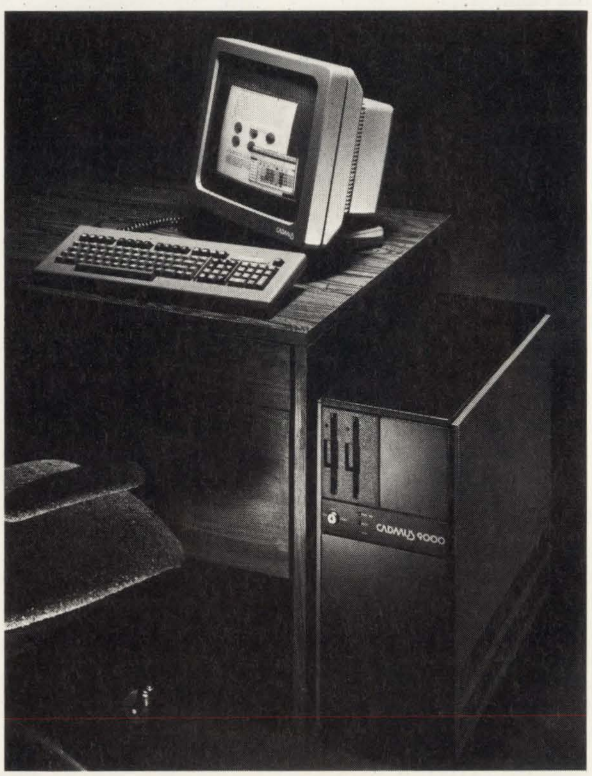
Hardware floating point unit

Designed for the Universe 68 line of 32-bit computers, this hardware floating point unit provides single- (32-bit) and double-precision (64-bit) arithmetic. A system configured for scientific applications includes floating point hardware, 32M-byte Winchester, and 1M byte of high speed main memory. The floating point unit is mounted on a single VERSAbus PC card. The price for the unit is $2750. **Charles River Data Systems, Inc**, 4 Tech Circle, Natick, MA 01760.
Circle 300

APL array processor

The APL machine delivers mainframe APL performance using array architecture. A typ configuration consists of a 4M-byte array processor, an IBM PC workstation, a 124M-byte hard disk, and a dual mode tape drive. An APL interpreter runs in the 12.5-MHz 16/32-bit super micro control processor, handling all syntax and conformance checking. The array processor can execute up to 10M full floating point operations. A memory manager allows the user to nest applications and to share code among concurrent processors. Prices for the APL machine, with a 0.5M-byte memory, start at $44,000; a typ system costs $85,000. **Analogic Corp**, Audubon Rd, Wakefield, MA 01880
Circle 301

RAW



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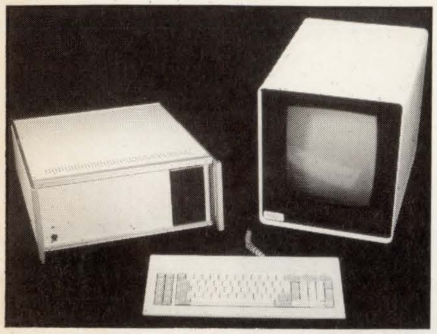
CIRCLE 137

High speed processor



Based on a 32-bit bit-slice ALU, the RNA processor adds hardware to support high speed shifting of 64-bit operands, stack and scratch RAMs, and parallel array multipliers. The peak instruction rate is 5 MIPS, avg rate is 1 MIPS, multiply time is 1.2 μs, and floating point is 2 to 3 μs. The operating system is similar to the UCSD p-system. Microcode supports dynamic linking of code segments. The R-code instruction set supports strings, sets, and packed fields as well as bit, byte, and half-word instructions. Memory addressing range is 32M bytes. Prices start at $9950. A fully configured system costs $32,500. **RNA, Inc,** 4377 First St, Pleasanton, CA 94566.
Circle 302

Memory packaging revision

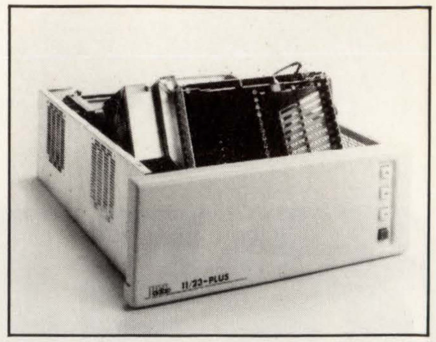
Series/1 processors have a 30M-byte integrated disk and optional 1.2M-byte diskette with the model 30D packaging. The package decreases purchase prices, maintenance costs, and size. The units can be rackmounted in a modular series/1 frame or used in a tabletop enclosure. An optional cache memory, which is microprocessor controlled, minimizes physical disk accesses by storing most frequently used data. Depending on the application, cache memory can double disk throughput. Model 30D prices range from $17,675 to $23,360. **IBM Corp, Information Systems Group,** 900 King St, Rye Brook, NY 10573.
Circle 303

Unix for 68000 microprocessor

The QU/32 is a 12-MHz 68000/68010-based Unix system. Rated at 1.3 MIPS, the system supports 4M bytes of 100-ns physical memory without address space limitations inherent in other systems. Dual-bus architecture and ported memory together with memory management and arbitration techniques allow memory access without wait states. The operating system is the Berkeley enhanced system III Unix with networking. Pascal, C, FORTRAN, BASIC, Ada, and relational DBMS are available. System pricing starts at $9900. **Integrated Solutions, Inc,** 1350 Dell Ave, Campbell, CA 95008.
Circle 304

Enhancement for 11/23-PLUS

System 11/23-PLUS enhances the KDF11-BA CPU with greater board capacity and overtemp protection. It uses the extended LSI-11 22-bit addressing (up to 4M bytes), two serial I/O lines, memory management, user friendly boot/diagnostics, and a line frequency clock.



Design allows expansion of an additional 9 full-quad boards, or 19 half-quad boards, or any combination. The basic system is offered with a choice of 256K or 512K bytes of RAM. In one to nine quantity, prices range from $4465 to $5265. **ADAC Corp,** 70 Tower Office Park, Woburn, MA 01801.
Circle 305

Compact display system

The RM-9465 is a compact graphics and imaging display system that consists of a Z80-based display processor and 64K bytes of RAM to store pictures in raster-scan format. It offers a resolution of 1280 x 1024 x 4 pixels and up to 24-bit refresh memory planes. Vector writing speeds are up to 16k vectors/s. The system can display a max of 1.3M colors simultaneously from a 16M-color palette. Features include context switching for independent graphics on multiple workstations, local pan and zoom, coordinate transforms, and split-screen clipping. Prices start at $11,250. **Ramtek Corp,** 221 Lawson Lane, Santa Clara, CA 95050.
Circle 306

INTEGRATED CIRCUITS

Low power RAM

The CDP1826C is a 64 x 8 CMOS static RAM. The chip has 8 common data input and data output lines, all with 3-state capability. A chip select input, CS/A5, permits the chip to be selected directly from the address bus without latching or decoding. Typ access time after a valid input address is 500 ns. Chip operates in 1 of 3 modes: read, write, or deselect. The deselect mode allows 6 input-address buffers to gate with the chip select function for reduced standby current. The chip operates from a single supply voltage in the 4.5- to 6.5-V range. In quantities of 100, the device is priced at $2.45 (plastic DIP) or $9.33 (cerDIP). **RCA Solid State Div,** Rte 202, Somerville, NJ 08876. **Circle 307**

Independent read/write RAMs

As a 16 x 4 open collector RAM, the 85S06 has a 35-ns access time; the 85S07 is the Tri-state version with the same access time. The 85S07A offers a 25-ns time. The fully decoded RAMs, which feature a chip-enable input, can be read or written into without one process interfering with another. This allows both data inputs and outputs to be connected to the data lines of a bus-organized system without complex interface circuits. In either plastic or ceramic packaging, prices range from $2.15 to $3.25 in quantities of 100 to 999. **National Semiconductor Corp, Microcomputer Systems Div,** 2900 Semiconductor Dr, Santa Clara, CA 95051.
Circle 308

Multifunction peripheral chip

Combining popular peripheral functions on one chip, the MK68901 multifunction peripheral (MFP) is compatible with the MK68000 microprocessor family. The chip's functions include four timers with individually programmable prescaling, an interrupt controller for 16 sources, 8 parallel I/O lines, and a single-channel USART. The full-duplex USART is both async to 62.5k bps and byte-sync to 1M bps, and has a baud-rate generator. A daisy chaining capability allows cascading of multiple MFPs without external logic. The chip sells for $56.25 each in 100-piece quantities. **United Technologies Mostek,** 1215 W Crosby Rd, Carrollton, TX 75006.
Circle 309

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CIRCLE 138

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SYSTEM COMPONENTS/INTEGRATED CIRCUITS

In-system write/erase EEPROM

A 16K-byte EEPROM, R5213, is organized as 2K x 8 and has an access time of less than 350 ns. The 24-pin DIP requires a single 5-V supply and TTL-level signals for operation. Six operating modes are available: write/erase inhibit, chip erase, byte erase, byte write, standby, and read. There is no limit to the number of times data may be read, and the device is guaranteed for a minimum of 10k write and erase cycles/byte. The device is pin compatible with the 2816 EEPROM. In volume quantities, it is priced at $10. **Rockwell International, Electronic Devices Div,** 4311 Jamboree Rd, PO Box C, Newport Beach, CA 92660.
Circle 310

Video display chip

The TMS9118/28/29 family of video display processors minimize system chip count in video graphic applications by reducing chip count from nine to three. Designed to interface directly with the TMS4416 16K x 4 RAM, the chip generates video, control, and sync signals. The processor controls storage, retrieval, and refresh of screen memory, which contains video display data. The chips provide 16 colors and sprite and pattern features for easy-to-program color animation capability. Offered in std 40-pin plastic packages, the prices in 10k quantities range from $9.96 to $12.10. **Texas Instruments, Inc, Semiconductor Group,** PO Box 401560, Dallas, TX 75240.
Circle 311

A-D array

Model TMG6001 is a CMOS A-D semicustom array. Specs are in the precision analog range: 2- to 5-mV op amp offset, 10-μV noise, and 5-MHz bandwidth. Matching specs include capacitance 0.1%, current source 1%, and resistor 0.5%. The chip has applications in A-D, D-A converters, PLL, capacitor filters, and MUXes. Consisting of 16 op amps, bipolar transistors, 4 zener diodes, 80 capacitors, 32 flip-flops, 530 logic gates, and a band gap reference, the device is TTL compatible and has 42 I/O pads. Developmental costs start at $20,000. Production costs are based on circuit complexity and quantities. **Telmos, Inc,** 740 Kifer Rd, Sunnyvale, CA 94086.
Circle 312

Half-power PLAs

Providing a 50% reduction in power dissipation, the L-series of PLAs can replace std PLAs in current production systems. The 35-ns max propagation delay and the 24-mA output drive capability are identical to the std. Typ ac performance parameters are 25 ns for propagation delay and setup time, and 10 ns for clock to output. Programming characteristics are the same as std PLAs, and the devices require no new adapters or other hardware. The half-power PLAs are available in 20-pin plastic, cerDIP, and leadless chip-carrier packages. Prices range from $6.80 to $7.50 in 100-piece quantities. **Advanced Micro Devices, Inc,** 901 Thompson Pl, Sunnyvale, CA 94086.
Circle 313

Page alterable EEPROM

A 32K-bit EEPROM (4K words x 8 bits), the NCR 52832 uses a single 5-V power supply. Typ read access time is 200 ns; max access time for commercial and military use are 300 and 450 ns, respectively. Erasing is accomplished in either block or page fashion. Writing or storing data is done as a single byte at a time or a page of up to 16 bytes. A memory margining feature is used for measuring the remaining data retention and number of store/erase cycles. The device is available in a 28-pin DIP or 32-pin cerDIP at $39.60 each in quantities of 100. **NCR Microelectronics Div**, 8181 Byers Rd, Miamisburg, OH 45342. **Circle 314**

Fast 16K PROMS

The 63S1681A and 63S1681 16K-byte PROMs offer a typ speed of 27 ns. The A device offers a 35-ns max access speed, while the second device has a 50-ns max access time. The devices feature low current PNP inputs, full Schottky clamping and 3-state outputs. Organized as 2048 x 8, the PROMs are available in three different packages: a 24-pin skinnyDIP, a std 24-pin cerDIP, and a 28-pin LCC. They are programmable on most commercially available programmers. Prices range from $18.50 to $23.38 each in quantities of 100. **Monolithic Memories, Inc**, 1165 E Arques Ave, Sunnyvale, CA 94086. **Circle 315**

Write protect EEPROM

A 150-ns, 16K-bit EEPROM, the 2816A requires a single 5-V supply and includes onchip circuitry that prevents accidental data erasure. Organized as 2048 x 8, the chip provides 2K bytes of memory. Data can be written at 9 ms and read access times are 250, 350, and 450 ns. The flexible firmware feature has applications in data processing, to implement soft function keys or changeable lookup tables, and in LANs, where each workstation can receive software updates. Prices range from $17.50 to $20.90 in 1000-piece quantities. **Intel Corp**, 3065 Bowers Ave, Santa Clara, CA 95051.
Circle 316

Array provides 90% cell use

A CMOS gate array, the C3900VH has 3900 gate elements and offers a 90% usage of the available basic cells. Typ delay times are 2.5 ns per gate. The chip has a max of 127 I/O pins to accommodate many I/O signals. It is available in a std 40-, 42-, or 48-pin DIP package, as well as in a 48- or 64-pad leadless chip carrier. In addition, std pin grid array packages with either 64, 88, or 135 pins are available. Non-recurring engineering charges are typically $27,000, and unit pricing at 10k pieces per year is $48.70 in a 40-pin cerDIP. **Fujitsu Microelectronics, Inc**, 3320 Scott Blvd, Santa Clara, CA 95051.
Circle 317

October Preview—
Watch for a major staff-written review on microprocessors and microcomputers.

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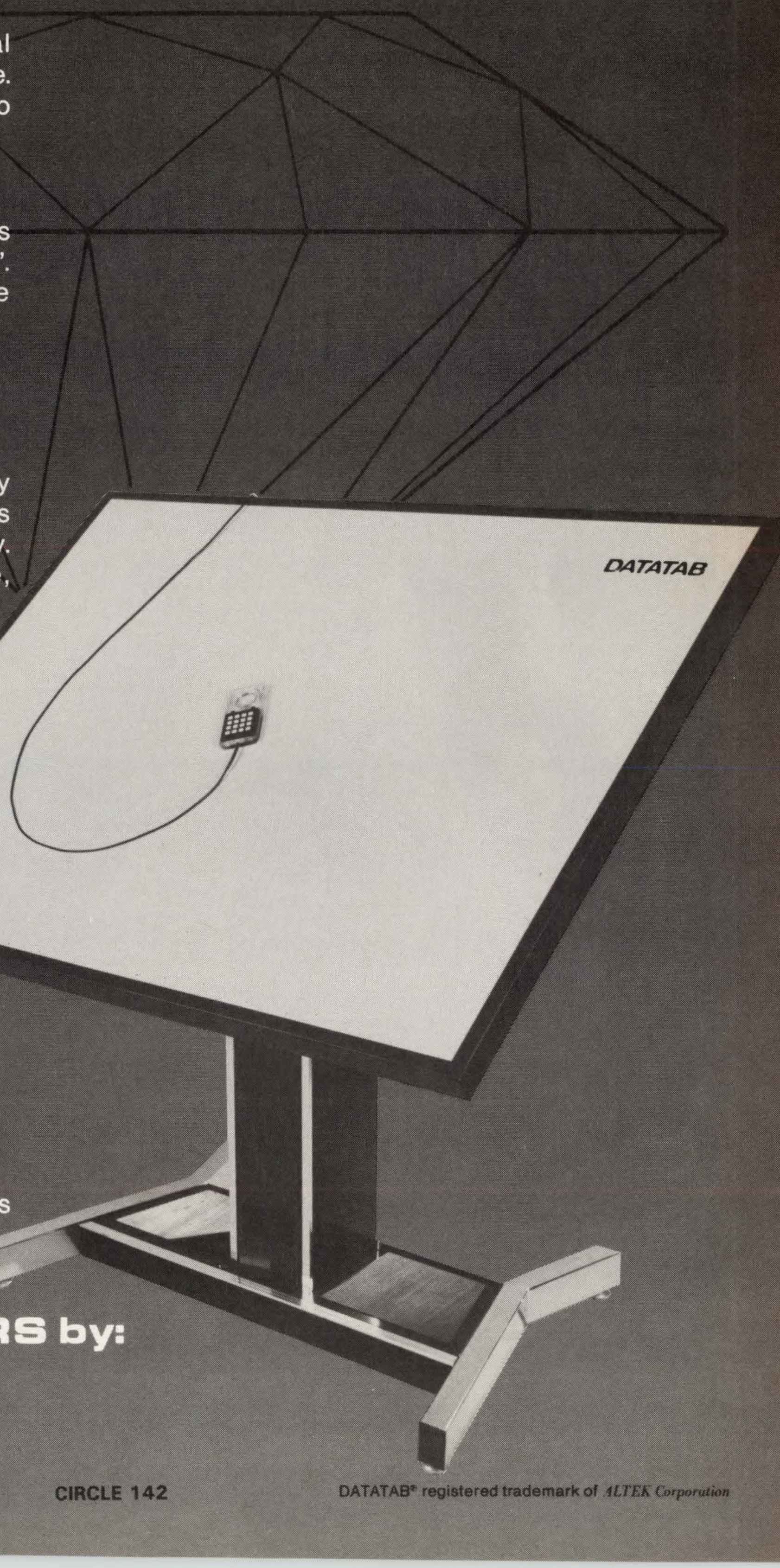

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CIRCLE 142

Low power static RAM

A static CMOS RAM, organized as 8K x 8, is designed for computer and instrumentation applications. The EDH8808CL suits low power requirements (standby current 40 μA) and large memory capacity in a small space. Unit is pin compatible with JEDEC byte-wide memory pinout and is EBM-pack compatible, conforming to industry std 28-pin DIP mechanical outline. Address access times are 150 or 200 ns, and max active power dissipation is 400 mW. The 150-ns version is priced at $62 and the 200-ns version costs $59, all in lots of 100. **Electronic Designs, Inc,** 35 South St, Hopkinton, MA 01748.
Circle 318

Multiplying 14/16-bit DACs

The MP7614 (14-bit) and MP7616 (16-bit) are proprietary, decoded, CMOS, current output, multiplying DACs. Using the MSB segmentation technique, the DACs feature 14-bit (0.003%) differential and 13-bit (0.006%) integral linearity. Chips have a low output capacitance (50 pF) fast settling time (500 ns), and a low feedthrough. The MP7616 can display linearity drifts of less than 1 ppm/°C, and will hold well over time. Packaging is in 20- or 22-pin plastic or cerDIPs with prices ranging from $26 to $83.25 in 100-piece quantities. **Micro Power Systems, Inc,** 3100 Alfred St, Santa Clara, CA 95050. **Circle 319**

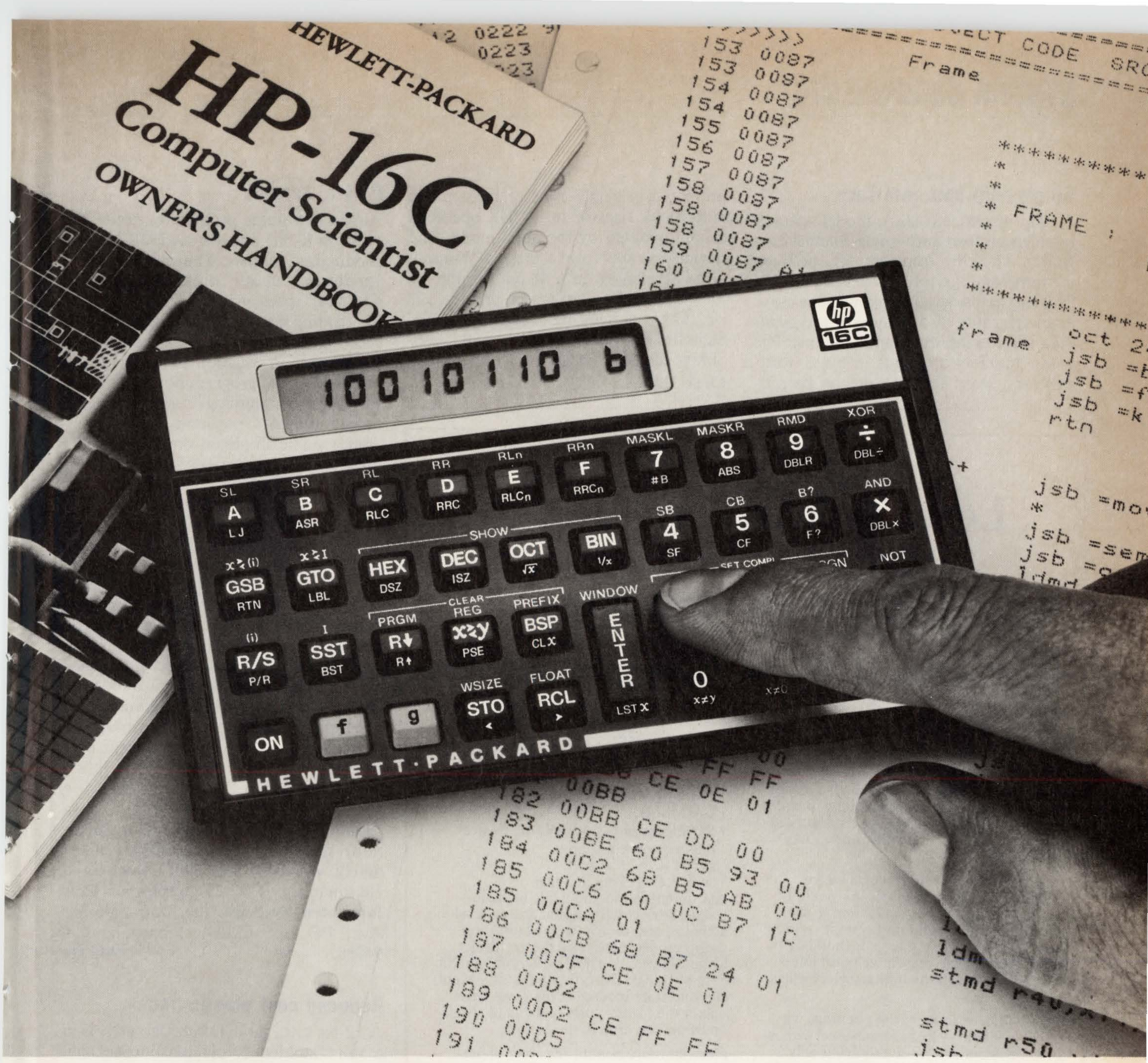
Low power logic circuits

The family of programmable array logic (PAL®) circuits has been expanded to include the A-2 (½ power) and A-4 (¼ power). A-2 has power consumption of 90 mA and a propagation delay of 35 ns (worst case). A-4 consumes 45 mA and has a propagation delay of 50 ns (worst case). Each circuit has 2 extra fuses to make copying difficult. Typ applications include personal computers, minicomputers, and industrial control. Circuits are housed in 20-pin skinnyDIP packages. Prices are $6.13 in 100-up quantities. **Monolithic Memories, Inc,** 1165 E Arques Ave, Sunnyvale, CA 94086. **Circle 320**

EPROMs with 250- and 300-ns speeds

The HN4827128G, a 16K x 8 EPROM, is pin compatible with the industry std (a JEDEC approved, B-type, 28-pin DIP). The device is offered with two different operating speeds: 250 ns (-25) and 300 ns (-30). Active current is 60 mA typ, with 100 mA max and 35 mA standby. Other features include a 5-V power supply and a 21-V single programming voltage. The EPROM is compatible with microprocessor-based products and other equipment using byte-organized architecture. The device is uv erasable. In 100-unit lots, the chip is priced at $28.90. **Hitachi America, Ltd,** 1800 Bering Dr, San Jose, CA 95112.
Circle 321

Premier Edition Preview—
Tying micro/personal computers into office automation networks— in late October.



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CIRCLE 144

PG02315 225C

Single-chip DMA interface

A DMA interface (DMAI), model SCB68430 is a high performance single-channel controller. The chip transfers data between memory and peripheral devices in 16/32-bit systems designed around the 68000. Transfer rates of 5M bytes/s are available for I/O intensive applications. The DMAI transfers operands in byte, word, and long word formats. It can be programmed in single cycle or burst mode with block sizes of up to 64K operands accommodated by the burst mode. The device operates from a single 5-V supply and is packaged in a 48-pin ceramic or plastic DIP. The 1000-piece price is $31 or $34, depending on packaging. **Signetics Corp**, 811 E Arques Ave, Sunnyvale, CA 94086.

Circle 322

Plastic EPROMs

Aimed at volume production needs, the P2764 (64K-bit) and P2732A (32K-bit) are production EPROMs. They are housed in windowless plastic DIPs. The EPROMS' electrical specs are the same as those of ceramic parts. Access times can be specified as 200 or 250 ns, depending on the model. Production EPROMs feature the intelligent programming algorithm for fast programming times. The rapid programming turnaround allows immediate volume shipment of systems using the chips. In quantities of 10k, the chips range from $5.50 to $6.60. **Intel Corp**, 3065 Bowers Ave, Santa Clara, CA 95051. **Circle 323**

Disk write amplifier

As a single IC interface between write data signals and tunnel erase magnetic heads, the XR-2247 disk write amp is suitable for floppy disk drives and single/double head systems. Write and erase currents are externally programmable by selecting the appropriate resistors. The device supplies two sets of current outputs for dual-drive heads. Write information is applied to the chip via a TTL-compatible, serial binary data stream. When write mode is in operation, negative input transitions alternately write to each half. Price in a 10k-quantity is $2.29 in plastic. **Exar Integrated Systems, Inc**, 750 Palomar Ave, PO Box 62229, Sunnyvale, CA 94088. **Circle 324**

Reduced cost plastic DAC

A 12-bit DAC, model DAC800P-CBI-V, is in a solid molded 24-pin plastic package. Specs include a 12-bit resolution, ½ LSB nonlinearity max, 3-μs settling time; max offset drift is ± 15 ppm/°C full scale range (bipolar). Max gain drift is ± 30 ppm/°C. Digital inputs are TTL, LSTTL, and 54/74HC CMOS compatible. An onchip proprietary open-loop baseline reference circuit eliminates the need for the designer to provide an external precision reference. An internal op amp converts output current to voltage internally. Price in 100s is $16.95. **Burr-Brown**, Box 11400, Tucson, AZ 85734.

Circle 325

Let's hear from you

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 CIRCLE 145

The Convergence Factor.

Convergence: the single most critical factor in color CRT performance.

Until now, Delta-gun tubes were the best way to achieve near perfect convergence, but only with costly adjustment electronics. Meanwhile, many in-line tubes are plagued by perceptible misconvergence. Which can lead to poor picture quality. A poor quality image for your product. And poor, bleary-eyed operators.

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The achievement of Panasonic high resolution in-line color CRTs.

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CIRCLE 146

Mini circular connectors

A range of Binder multipin connectors meets several DIN specs including 41524, 45322, 43321, and some VDE requirements. They are available for panel mounting or cable end terminations with 1 to 14 contacts/connector. Connector bodies are constructed in all metal or plastic configurations. Mated connectors are locked in place using a push-pull or screw locking mechanism. Cable end connectors have a straight or right angle strain relief. **Alpha Products, Inc,** PO Box 4306, Thousand Oaks, CA 91359.
Circle 326

Logic board

The Methode series 2300 wrappable logic board, specifically designed for 68000 VERSAbus systems, features universal layout. Its spacing is 0.300", 0.400", 0.600", and 0.900". For JEDEC type A devices, the board has two 68-pin leadless chip carrier sockets, including wrappable pinout with alternate pairs of grounded terminals for twisted pair termination. With an IC field of 55 cols of 53 pins, the board capacity is 120 16-pin ICs, plus 5 cols of 0.600" spaced devices. **Methode Electronics, Inc, Logic Board Div,** 7444 W Wilson Ave, Chicago, IL 60656. **Circle 327**

Interface breadboard

The parallel breadboard module is designed for the implementation of customized interfaces. Assembled on an industry-std 4.5" x 6.5" (11.4- x 16.5-cm) circuit board, the breadboard includes a 6821 parallel interface adapter, address decoding logic, and decoupling capacitors. Holes on the board are placed on 0.1" centers for use with 0.3", 0.4", or 0.6" DIPs. A special area accepts any connector using 0.1" spacing, up to a 50-pin ribbon cable header. The module is priced at $49 and the manual is $5. **Wintek Corp,** 1801 South St, Lafayette, IN 47904. **Circle 328**

DIN spec connectors

A PCB connector family includes post and box contact versions of the std 96-position DIN connectors, reverse DIN configurations, and DIN modules containing 21 contacts. Grid spacing is 0.100" x 0.100" (2.450 x 2.450 mm). Post and box grid spacing is 0.200" x 0.200" (5.080 x 5.080 mm). Connector features include 50% higher PCB density, matched impedance, lower crosstalk, and shorter electrical paths. The DIN family is covered by MIL-C-55302, IEC 130-14, DIN 41612, and VG 95324 spec. Costs are $0.08 per mated line for a std set of 96-pin connectors in 1000-piece quantities. **Malco, a div of Microdot Connector Group,** 12 Progress Dr, Montgomeryville, PA 18936. **Circle 329**

IBM PC expansion chassis

This bus expansion chassis doubles the IBM PC's option adapter board capacity. The PC-XTRA increases to 10 the total number of option slots. Features include six expansion slots and a power supply. The chassis is double the capacity of the PC bus, and no hardware or software modifications are required. It allows the addition of all special options without filling the plug-in and back panel space; these include lightpen, game control adapter, main memory expansions, and communication ports. The device sells for $680. **PC Horizons, Inc,** 200 N Tustin Ave, Santa Ana, CA 92705.
Circle 330

CIRCLE 147

MUX connects terminal to copier

This 4-port MUX allows four GR-1104 desktop graphics terminals to connect to the CH-5201B color hard copier. Priced at $1950, the MUX is a standalone unit. The terminal, priced at $4950, offers a resolution of 1024 x 780 and features an onscreen display of 8 colors from a palette of 512. The 14" terminal is designed with a noninterlaced display. The $8950 copier is based on technology that blends color printing concepts with thermal image transfer technology. The copier can produce transparency copies. **Seiko Instruments U.S.A. Inc, Graphic Devices and Systems,** 1623 Buckeye Dr, Milpitas, CA 95035. **Circle 331**

Push-button Apple interface

The Print-It! card enables an Apple screen to be dumped to a printer. By pushing a single button, the card will pause a program, print whatever is on the screen, and then continue processing the interrupted program. It automatically selects the text/graphics mode and will print in either 40- or 80-col text. For control, the microprocessor is removed and placed in the control board. This board is placed in the micro slot. The entire kit consists of a plug-in card, push button, printer cable, and a plug-in controller board. It is priced at $299. **Texprint, Inc,** 8 Blanchard Rd, Burlington, MA 01803. **Circle 332**

Switching modules

A series of computer I/O switching modules, the C76 DIP I/Os are available in either output or input models. Output modules allow either TTL or CMOS-level signals to control power switching to high voltage loads. Input modules convert the presence or absence of load-level voltages from pressure, flow, and limit switches to clean low-level logic signals for computer input. The modules are intended for use in robotics, process control, and automatic test equipment. The family is available at $7.75 to $8.95, depending on function. **Teledyne Relays,** 12525 Daphne Ave, Hawthorne, CA 90250. **Circle 333**

IEEE 488/Ethernet connector

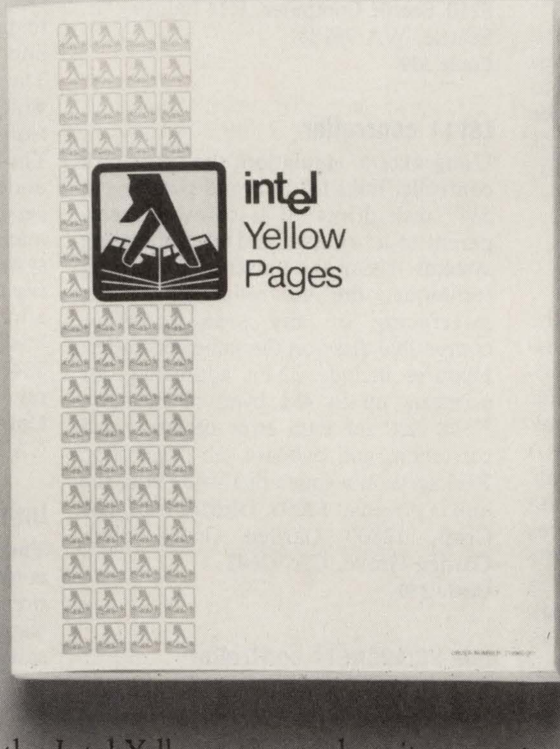
The IEEE 488 to Ethernet interface board allows connections from an IEEE 488 (GPIB) port to an Ethernet LAN. The board offers 2K-byte transmit buffer, 2K byte receive buffers, and an auto-discard for undesirable receive packets (performed in hardware for increased throughput). Software configurations include partial multicast address filtering, reloadable station address, and 4 address reception modes. A statistics mode runs in parallel with regular receive transmit functions. The board also provides internal self-test and diagnostics. **Xebec,** 432 Lakeside Dr, Sunnyvale, CA 94086. **Circle 334**

Graphics display controller

The MSBX-800 is a color graphics iSBX multimodule that provides a 512- x 512-pixel resolution. It can display 16 colors from a palette of 4096. User may choose from either interlaced (30-Hz) or noninterlaced (60-Hz) operation. The 7220 GDC VLSI video controller provides a high level software interface. Other features include split screen, smooth scroll and pan, hardware vector and circle generation, high speed characters and patterned area fills, and hardware blink. **Matrox Electronic Systems Ltd,** 5800 Andover Ave, TMR, Quebec, H4T 1H4, Canada. **Circle 335**

CIRCLE 149

INTRODUCING THE EASIEST WAY TO CALL UP YOUR SOFTWARE.



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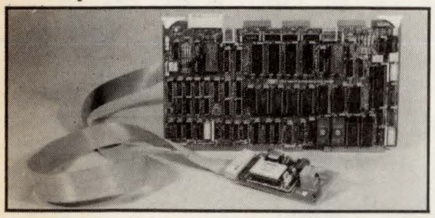


As a Multibus-compatible board, the 8140 smart communication controller can operate in a multiple board system or as a standalone controller. It contains two RS-232-C ports, two Bell 202/103 modems, and onboard 8085A micro, dual-port RAM, and two levels of preprocessing firmware. The firmware supports packet-switching protocols, and when used together with the 8183 direct access arrangement, it provides pulsed auto dial/answer communications. Unit price for the 8140 is $1240 and for the 8183 is $190. **ETI Micro,** 6918 Sierra Ct, Dublin, CA 94568.
Circle 336

Unibus interface

DMA general purpose interfaces, the DRE11 and DRU11 maintain continuous-flow data transfers to and from a computer's main memory. They transfer streams of 16-bit parallel data at peak rates to 600k (DRE11) and 500k (DRU11) words/s and connect to the systems' Unibuses. Under software control, data can be transferred through the interfaces in words, single blocks, and multiple blocks. Buffer areas are defined within the computer's main memory (up to 64k words) and switch automatically between areas during data transfer. Each is priced at $2495. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754.
Circle 337

Low cost network controller

A LAN controller board, the 1553-NET is a carrier sense multiple access controller complete with collision avoidance and detection features. It allows OEMs to provide small-computer users with network capability. The controller provides transfer rates of 3M bps and operates over low cost coaxial cable (50, 75, or 120 Ω). Each computer is linked to the cable using BNC connectors at each workstation point. Features include dual-channel communication, five levels of error protection, variable block sizes, and switch-selectable transmission rates. Price is $349. **VLSI Networks, Inc,** 6314 W Manchester Blvd, Los Angeles, CA 90045.
Circle 338

IBM PC/XT multifunction card

The RAM+3 is a slot-saving multifunction card designed for the IBM PC and XT. It gives users a time of day clock/calendar with battery backup, a parallel printer port, an RS-232 serial port, options for 256K bytes of additional RAM, and Flash Disk software. The card eliminates the need to manually input the date and time when the system is powered on. The software allows clock operation to be integrated into DOS 1.1 or 2.0. Flash Disk software permits the user to designate a portion of the memory to be used as if it were a disk drive. The basic version is priced at $210. **Seattle Computer,** 1114 Industry Dr, Seattle, WA 98188.
Circle 339

LSI-11 controller

Using RK06/07 emulation, the DQ615 disk controller links LSI-11/23 and 11/23Plus to 5¼" disk drives. It is software transparent to RT-11, RSX, and RSTS operating systems. Using the universal formatting technique, the controller allows the interfacing of any ST506 interface compatible disks on the same controller. Features include 22-bit addressing for accessing up to 4M bytes of memory, 32-bit ECC for data error detection and correction, and onboard self-diagnostics. Packaged on a single dual-wide PCB, the unit is priced at $2095. **Distributed Logic Corp,** 12800 Garden Grove Blvd, Garden Grove, CA 92643.
Circle 340

IBM PC/ARCNET® controller

The ARC-PC LAN controller module provides the user with an interface between the IBM PC and an Arcnet® modified token-passing LAN. The module, which includes a 2K-byte onboard data buffer to provide four pages of packet storage, can be configured for double buffering. The interval timer allows user programmable timeouts. The interface will support up to 255 nodes/network segment while running at a 2.5M-bit data rate. The price in unit quantity is $495. **Standard Microsystems Corp,** 35 Marcus Blvd, Hauppauge, NY 11788.
Circle 341

Analog input for Q-bus

Models 120, 121, and 122 are high speed analog input boards compatible with Q-bus microcomputers. Model 120 offers 50-kHz throughput, 121 offers 150 kHz, and 122 offers 200 kHz. The units are supplied on a std DEC style PCB measuring 8.9" x 5.2" (22.6 x 13.2 cm) and reside in a single card slot. Features include 12-bit resolution, input voltage ranges of 0 to 10, ±5, ±10 VFS, DMA, and programmed I/O. Sixteen input channels can be configured in the field for 16SE, 16PD, or 8DI channels; optionally available are 32SE, 32PD, or 16DI. Prices in quantities of 1 to 9, range from $1295 to $1795. **Grant Technology Systems Corp,** 11 Summer St, Chelmsford, MA 01824.
Circle 342

Mainframe/personal computer interface

Designed to link mainframe data bases to personal computers, the Data Pipeline is a hardware/software package. The system is based on the iDIS 86/735, which serves as a data gateway by controlling access to database information. The iDIS 86/735 uses the 8086 chip and runs under Xenix. The Data Pipeline uses a version of the System 2000® database management system. Extensions to the system provide a relational database capability, graphics, and fourth-generation software architecture. The database information system sells for $34,995, with system 2000 extensions ranging from $40,000 to $165,000. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051. **Circle 343**

Interface for IBM PC-XT

The GPIB-PC is an IEEE 488 interface that converts the IBM PC into an instrumentation workstation complete with software. Features include small size (half a slot in PC-XT), high speed (300k bytes/s), and documentation. Software consists of a handler under PC-DOS 2.0 and subroutines called from applications programs written in BASIC, C, 8088 assembly, Pascal, and FORTRAN. Additional software includes an interactive control program for troubleshooting and software development. The card is priced at $385 with OEM discounts available. **National Instruments,** 12109 Technology Blvd, Austin, TX 78759. **Circle 344**

Tell us what you like

Did you remember to rate the articles in this issue of Computer Design? A special editorial score box is provided on the Reader Inquiry Card.

Independent-channel interface

The STD SIO-2 board provides two independent RS-232 serial data channels to interface with terminals, printers, modems, and other serial devices. Features include 150- to 19.2k-baud rates, polled or interrupt operation, and switch-selectable address. The board has transmit and receive buffering, auto parity checking, and auto break detection. Size spec is 4.5" x 6.5" x 0.5" (11.4 x 16.5 x 1.3 cm) with an operating temp of 0 to 70 °C, and power requirements of 5 V ±5% at 375 mA typ. Price for the interface board ranges from $195 in single quantities to $175 in quantities of 10 or more. **Forethought Products,** 87070 Dukhobar Rd, Eugene, OR 97402.
Circle 345

LSI-11 controller

The Spectra 25 is a single-board, multifunction disk and tape controller. Designed for use with the LSI-11, users can attach a removable pack of Winchester SMD disk drives and start/stop or streaming half-inch tape drives. The controller offers software transparency to std DEC operating system and diagnostic software. It attaches up to 2 SMD disk drives and up to 8 formatted tape drives without operating system modification. Options can be selected without removing the controller from the system by using extended commands to program the onboard EEPROM. **Spectra Logic Corp,** 1227 Innsbruck Dr, Sunnyvale, CA 94086. **Circle 346**

Processor/controller board

An 8-color video display board is VME bus compatible. Model DSSE512CHROMA8-1 is built around a graphic display processor and an intelligent peripheral controller. Capabilities include vector and plot pointing, ASCII alphanumeric character display, figure generation, and image memory readback. The 192K bytes of image memory are divided into two screen pages of three planes each. The board can be located anywhere in the memory map and uses 256 consecutive odd address locations. The board is delivered with an EPROM for std firmware and a 2K-byte RAM for monitor/user. Unit price is $2850. **Data Sud Systems/U.S. Inc,** 2219 S 48th St, Tempe, AZ 85282.
Circle 347

DEVELOPMENT SYSTEMS

Software development system

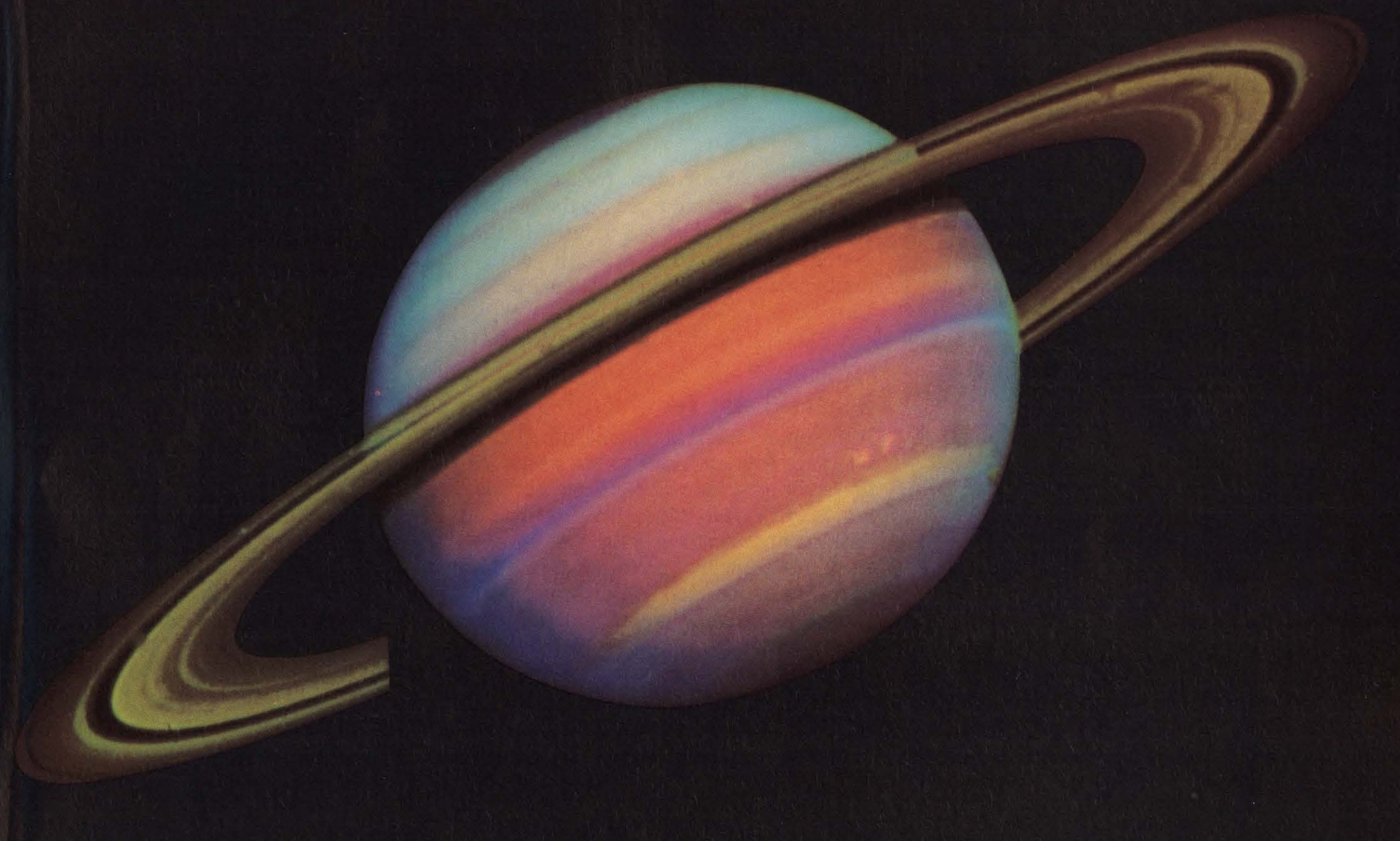
Model 95/86 RMX workstation is a microcomputer system designed for RMX-86 software developers. The system consists of a 10M-byte Winchester and a 500K-byte floppy drive, 512K bytes of RAM, and an 8086/8087 dual-processor set. Software tools for developing utility and device drive application software include ED, ASM86, LINK86, LOC86, and LIB86. In addition, PL/M, FORTRAN, Pascal, and C are available. For flexibility, the workstation has six Multibus expansion slots and one std 8" disk drive slot. The system is priced at $14,425. **Zendex Corp,** 6644 Sierra Lane, Dublin, CA 94568.
Circle 348

VMEbus development system

VMEbus Baseline system allows the evaluation and development of VMEbus-compatible systems. Std is a 10-slot VMEbus-compatible backplane equipped with three VMEbus boards: the VME-SBC, VME-SIO, and VME-DRAM. These boards provide an MK68000 microprocessor, five RS-232 serial I/O channels, 256K bytes of DRAM with byte parity, 12K bytes of static RAM, interrupt control, and two timer/counters. Monitor and debugger firmware perform initialization, DRAM diagnostics, display/modify memory, and program disassembler. Price is $6995. **United Technologies Mostek,** 1215 W Crosby Rd, Carrollton, TX 75006.
Circle 349

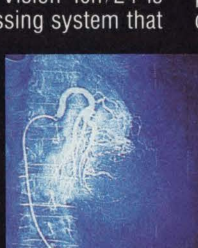
Graphics development system

The EROS/186 development system provides a complete 80186 based microcomputer system. It includes high resolution color graphics with full-function realtime multitasking operating system and high level runtime language support for program development. The unit operating system is the iRMX 86, which contains the UDI/URI interfaces. Hardware features include an 8" flexible disk controller, programmable interrupt controller, 64K bytes of RAM, and 512K bytes of system memory. Prices range from $10,000 to $60,000 (Canadian). **Datem Ltd,** 7 Slack Rd, Suite 206, Nepean, Ontario K2G OB7, Canada.
Circle 350



Only your imagination can limit the application of Comtal's new Vision Ten/24 Image Processing System.

Whether you're exploring the outer regions of space or exploring for oil in some remote area of the world, Comtal's new Vision Ten/24 is the only digital image processing system that processes and displays 1024 x 1024 high resolution images with a clarity never experienced before in image processing. It's a powerful tool for interpreting and analyzing images for such diverse applications as LANDSAT, meteorology, seismology, graphic arts, earth resource management, medical imagery, or something only you know about.



Four times the resolution at 30% lower cost.
The Vision Ten/24 is the only image processing system capable of processing and displaying images at a 1024 x 1024 resolution in real time (1/30 second) with a 40 MHz video output rate. That's four times the resolution of the industry-standard 512 x 512 systems. With it, whole new worlds open up. Interpretation and analysis become more precise. Best of all, the basic Vision Ten/24 system price is 30 percent less than our previous 1024 x 1024 system because of our design and manufacturing refinements. Giving you incomparable price/performance.

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Comtal—a generation ahead in image processing.
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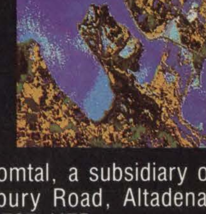

Put your imagination to work and give Comtal a call today for a firsthand look at our new Vision Ten/24. Comtal, a subsidiary of 3M, 505 West Woodbury Road, Altadena, California 91001, (213) 797-1175

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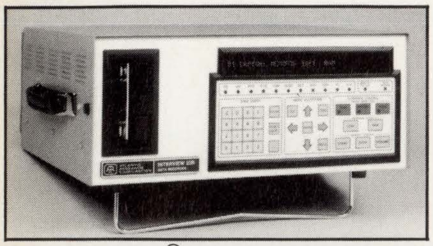
CIRCLE 152

Portable data recorder



The Interview® 20R data recorder is designed for use with any protocol analyzer. Its data tape format is compatible with the Interview 3500/4600 data analyzer series. An integral realtime clock permits unattended data collection by starting and/or stopping at a specific day and time. The unit records a bit image of the communication line. This allows protocol-independent data recording to 19.2k bps using the 600K-byte drive or to 72k bps with an optional 4M-bit capture RAM. **Atlantic Research Corp,** 5390 Cherokee Ave, Alexandria, VA 22314. **Circle 351**

Frequency counters

Covering the frequency range from 10 Hz to 1 GHz, models 5384A and 5385A frequency counters offer high accuracy in a low priced system. The 5384A frequency range is 10 Hz to 225 MHz; the 5385A is 10 Hz to 1 GHz. Both units feature a measurement resolution of 9 digits/s minimum 4- to 11-digit display resolution (front panel selectable), and an input sensitivity of 10 mV rms (typ). Additional specs include input-signal conditioning, and 3-gate time selections—0.1, 1.0, and 10 s. The 5384A costs $1400 and the 5385A runs $1700. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.

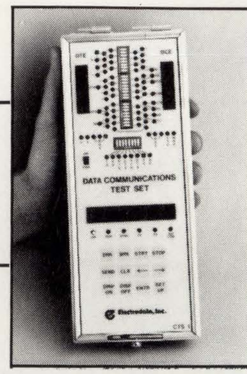
Circle 352

PCB tester

The Autoprobe automatically moves an electronic probe to a location on a PCB and takes signals from various positions to find faulty components. It is based on an open bed positioning mechanism and is controlled by two 6809 microprocessors with 8K bytes of memory. The probe can test PCBs of all sizes up to 18″ x 32″ (46 x 81 cm). The probing mechanism has a pneumatic dampener for constant operator adjustable force on the probe. A variety of probes can be used in the system since they are all easily removable. Price is $6095. **Alpha Merics Corp,** 20931 Nordhoff St, Chatsworth, CA 91311. **Circle 353**

Handheld test set

A handheld data communications test set, the CTS 1 conforms to EIA std RS-232 or CCITT V.24. It will perform bit and block error rate tests, bias distortion tests, count and trap pulse transitions, and make delay measurements. All operating parameters are menu selected and retained while power is off. Error rate tests can be run on both full- and half-duplex sync and async systems using 1 of 8 patterns. The test set can count and display bit and block errors, blocks received, and sync faults. The CTS 1 is $1495. **Electrodata, Inc,** 23020 Miles Rd, Bedford Heights, OH 44128.
Circle 354



MICROPROCESSORS/MICROCOMPUTERS

Z80-based micro bus board

The 1864+ microcomputer bus board is compatible with other boards in the 180+ family. It comes equipped with 128K bytes of dynamic RAM and sockets for up to 112K bytes of nonvolatile memory—in the form of EEPROM, EPROM, and battery-backed CMOS RAM. A memory mapper allows any of 16 4K-byte blocks of memory to be mapped into the CPU's 64K-byte address space. The device features two serial communication channels, a 4-channel counter/timer circuit, and a realtime clock. As an option, an arithmetic or floating point processing unit is available. **Xycom, Inc,** 750 N Maple Rd, Saline, MI 48176. **Circle 355**

Microcomputer on one board

The SBC6511 is a single-board computer that uses the recently announced R6511Q microprocessor from Rockwell. This chip uses an enhanced version of the std 6502 instruction set. It has an onchip clock, async serial port, event counter, timer, and 192K bytes of RAM. The basic configuration includes the CPU, power supply, address decoders, 1.8432-MHz crystal, and serial port ops to 19.2k baud. Options include an IEEE 488 (GPIB) interface, an RS-232 interface, development board with monitor, and assembler. Expansion ports allow 2K bytes of RAM and 8K bytes of ROM. Single-unit price is $189. **Connecticut microComputer,** 36 Del Mar Dr, Brookfield, CT 06804. **Circle 356**

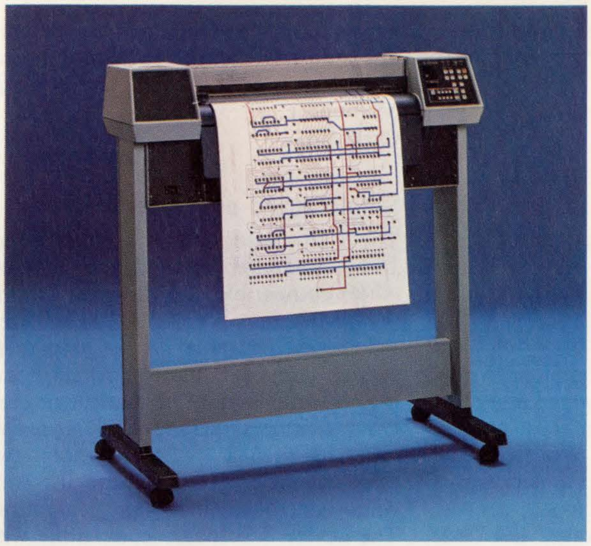
CP/M coprocessor for DEC minis

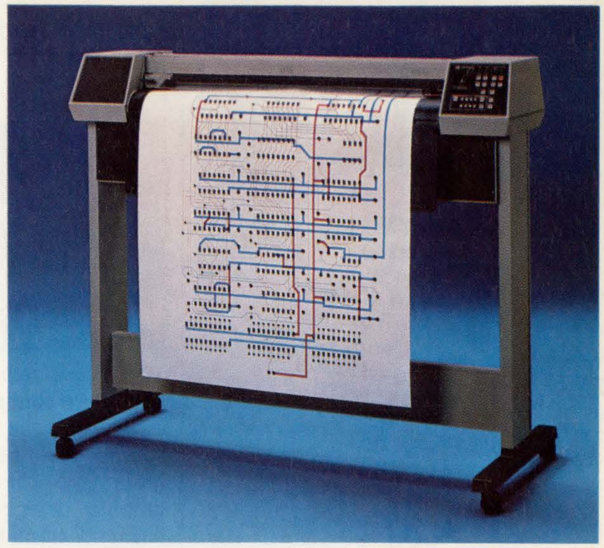
The zplus board is a CP/M coprocessor for the DEC Unibus. It works with the CP/M Bridge system to enable DEC minicomputer users to use other minicomputer CP/M software. The board is designed to support control of external devices, communication protocols, RAM disk-based processing, and CP/M 3.0. It offers two micro coprocessors, 512K bytes of RAM, and four serial ports. The board cell is accessible as a normal device to host processes via dual-ported memory and Z80 control and status registers. The Bridge and board are available for PDP-11s and VAXes. **Virtual Microsystems,** 2150 Shattuck Ave, Berkeley, CA 94704.
Circle 357

S-100 board computer

An S-100 computer system on a single S-100 board, the Super-Quad consists of 64K bytes of bank-select RAM, a Z80A CPU, a 2K-byte monitor EPROM and a Z80A CTC for realtime interrupts. It also has a 5¼″ and 8″ floppy disk controller and two serial and two parallel interface ports. Full DMA operation is supported, and the board operates under both CP/M and MP/M software. As a single-user system, it allows the addition of user-defined options. Its ability to be a bus master makes it suitable for multi-user environments. The price is $875. **Advanced Digital Corp,** 12700 B Knott Ave, Garden Grove, CA 92641.
Circle 358

Now you have a choice!





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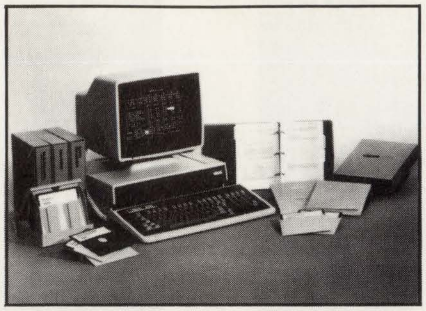
CIRCLE 153

SYSTEM COMPONENTS/MICROPROCESSORS/MICROCOMPUTERS

Low cost professional computer



The Visual 1050 small computer system provides a complete software library. Included with the system are the Multiplan spreadsheet package, Wordstar 3.3, Mailmerge 3.3, a graphics package, a graphics device driver, CBASIC, a VT-100 terminal emulation package, and CP/M Plus®. Hardware includes two 400K-byte disk drives, 96K-byte RAM expandable to 160K bytes, and a 640 x 300 bit-mapped monochrome display. Additional std equipment includes a printer and modem port, Winchester port, and a 93-key keyboard. Price, including software, is $2695. **Visual Techology Inc**, 540 Main St, Tewksbury, MA 01876.
Circle 359

CMOS microprocessor

The 80C86 16-bit microprocessor uses CMOS technology. This chip offers the same computational performance as the 8086 with up to a 90% reduction in power consumption. Other benefits include reduced heat generation, longer equipment life, and decreased sensitivity to electromagnetic noise. It operates over a wide temp range, from −55 to 125 °C. Applications for the micro are in personal and portable computers, office automation, communication systems, and industrial control. Price in 100-piece quantities is $31.25 each. **Harris Corp**, Melbourne, FL 32919.
Circle 360

Single-board computer

The Multimaster 186 SBC is a high speed, 16-bit computer system. It is IEEE 696 (S-100) compatible and designed around the 8-MHz iAPX 186 micro. The system is switch configurable as a permanent master, temporary master, or temporary master with dummy permanent master. Other features include 128K bytes of RAM, up to 64K bytes of EPROM, two DMA channels, and hardware for software controlled interrupt generation. The device is software compatible with the 8086/8088. **Communications Research Corp**, 1720 130th Ave, NE Bellevue, WA 98005.
Circle 361

Z80 compatible microcomputer

A self-contained board level 16-bit microcomputer, the DSTD-188 is available with an optional math coprocessor (8087). The board supports memory refresh compatible to Z80 transparent refresh, allowing 0.25M-byte memory cards to be used. A push-button reset input can be configured as a sync pulse to preserve RAM contents. The 8-MHz version will support all Z80A peripheral chips on the STD bus. It provides for the configuration of either the Z80 or 8088 STD bus architecture, ensuring future compatibility. **dy-4 Systems Inc**, 888 Lady Ellen Pl, Ottawa, Ontario K1Z 5M1, Canada.
Circle 362

POWER SOURCES & PROTECTION

RS-232 protection

The Surge Sponge protects RS-232 interfaces from high voltage transients produced by inductive coupling of interface cables with high power cables. Model 21 has MOV devices to protect pins 2, 3, 4, 5, and 7 of the interface. On any of these pins, all voltages that exceed approx 27 V are clamped to ground. All interface pins are wired through the device so it appears transparent and does not affect std interface levels. In single quantity, the Surge Sponge sells for $39.95; in 100-piece quantities, it sells for $32 each. **Remark Datacom Inc**, 4 Sycamore Dr, Woodbury, NY 11797. **Circle 363**

Triple output switcher

Model 3040-1 is a switcher with up to three output voltages in a single PCB. It provides outputs of 5 Vdc at 3 A, 12 Vdc at 2 A, and −12 Vdc at 0.1 A. Other specs include 70% efficiency, 16-ms hold-up time, and 1500-Vac input-to-output isolation; convection cooling is std. The power supply input offers pin strappable voltage ranges of either 90 to 130 Vac, or for European applications, 180 to 260 Vac at 47 to 440 Hz. The supply is on a 3″ x 5″ x 2″ (8- x 13- x 5-cm) card and is priced at $79. **Power General**, 152 Will Dr, PO Box 189, Canton, MA 02021. **Circle 364**

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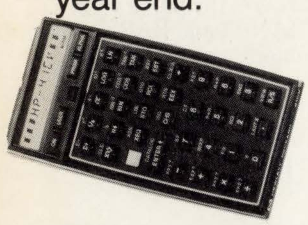
CIRCLE 155

YOUR ANSWERS TO THESE QUESTIONS HELP US SERVE YOU BETTER

YOUR ANSWERS ARE IMPORTANT. The results of these surveys help our editors select topics, features and technical data that will be on target with your design activities. Your inputs also alert manufacturers to your needs and can result in the development of product speeds, ranges, capacities, and other specs that you require.

YOUR ANSWERS CAN ALSO WIN YOU A VALUABLE PRIZE!

Each questionnaire returned gives you a chance to win a special prize. Drawings are made after each issue, with a grand prize drawing at year end.



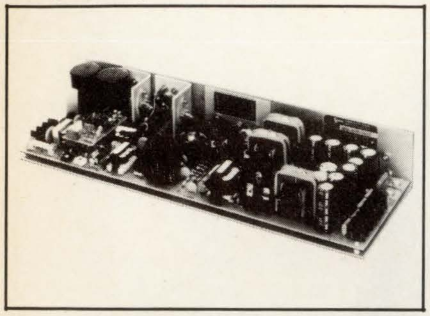
MONTHLY DRAWING **— HP 41CV PROGRAMMABLE CALCULATOR**

The HP 41CV offers advanced problem-solving power yet is easy to use. Communicates in words as well as numbers. Can be programmed to meet your specific needs. Fifty-eight popular functions, 130 total functions in program library. Memory expandable to almost 6,500 bytes.

ANNUAL DRAWING **— HP 85 DESK TOP COMPUTER**

This portable (20 lb.) unit includes an alphanumeric keyboard, tape drive, thermal printer, built-in 56K byte memory, CRT screen, and 150 built-in BASIC language commands. You can add peripheral and software packages to expand system capability. A $2800 value!

Peripheral power supplies



A series of multiple-output, open frame, switching power supplies deliver 5-V, 50-A output. The MOX-400 series is designed to power logic, memory, interfaces, disk drives, and printers. A choice of ±12 V, 10 A or ±15 V, 10 A is offered for outputs. One model in the series has user specified second, third, and fifth outputs. The main control loop regulates line and load of the 5-V output to ±1%. A second loop regulates the ±12- or ±15-V outputs to 2%. Ripple and noise are rated at 0.2% rms. Supplies are priced at $407 in 100-piece quantities. **Todd Products Corp,** 50 Emjay Blvd, Brentwood, NY 11717.
Circle 365

Voltage regulators correct in one cycle

A portable voltage regulator is designed for protecting electronic equipment against problem-causing voltage fluctuations. It is rated for operation at 1 kVA and uses multitap autotransformer technology. This enables the regulator to correct voltage fluctuations in less than one line frequency cycle. Features include a choice of output voltage envelopes (±7%, ±5%, or ±3.3% of nominal line voltage) and 98% power efficiency for energy conservation. All models operate over a frequency range of 47 to 63 Hz and add less than 0.1% total harmonic distortion. Prices start at approx $800. **Powermark, a div of Topaz, Inc,** 3855 Ruffin Rd, San Diego, CA 92123. **Circle 366**

Logic-controlled regulator

A logic-controlled, dual 5-V output regulator, the LT1005 contains two independent regulator circuits. The main regulator's output can be controlled by a TTL- or CMOS-compatible enable signal. Its 5-V output can be switched to near zero by a logic low signal. The auxiliary output is unaffected by the logic control signal and fault conditions. The dual-output structure permits the main 5-V supply to be shut down for power savings. Outputs are regulated to 5 V at 1 A and 5 V at 35 mA. The regulators have a 2% output voltage tolerance, 66-dB ripple rejection, and 0.5% load regulation. The 5-lead package is priced at $2.15 in quantities of 100. **Linear Technology Corp,** 1630 McCarthy Blvd, Milpitas, CA 95035.
Circle 367

DC-DC converters

A line of 24-V input encapsulated dc-dc converters offers output voltages of 5, 12, 15, ±12, ±15, and ±18 Vdc. Output voltage accuracies are ±1%, output ripple is 5 mV rms; back ripple current is 1% of linear max. Max breakdown voltage is 300 Vdc, transient recover time is 50 μs, and all units have output current limiting protection. Each 5-W model comes encased in a 2.0" x 2.0" x 0.75" (5.1- x 5.1- x 1.90-cm) case and the 10-W models are in a 3.5" x 2.5" x 0.875" (8.9- x 6.4- x 2.222-cm) package. In quantities of one to nine, prices range from $75 to $103. **Datel-Intersil,** 11 Cabot Blvd, Mansfield, MA 02048.
Circle 368

Enclosed/shielded switchers

A line of enclosed and shielded multi-output power supplies, the EMR series provides power in the 20- to 80-W class. Three or four outputs are rated for CRTs, logic, disk drives, CPUs, and memory. Designed with a computer, the supplies employ a proprietary hybrid micro-circuit to reduce part population. An onboard conducted emi filter meets the requirements for FCC Class B computing devices. The 80-W model has sufficient 24-V power to run an 8" floppy disk drive. **Kepco Inc,** 131-38 Sanford Ave, Flushing, NY 11352.
Circle 369

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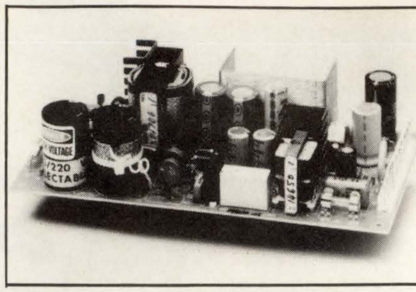
Open-frame switcher



The XL60 is a 70-W 4-output, open-frame switching supply powering CRTs, micros, minifloppies, cassettes, and small printers. A proprietary current controlled feedback network achieves tight regulation and fast transient response. Std features include input voltage 110/220 Vac user selectable, input surge protection, rfi filter designed to meet FCC and VDE level B, power limit and short circuit protection, and over-voltage protection on the 5-V output. In 100-unit quantities, the supplies are $100. **Boschert Inc,** 384 Santa Trinita Ave, Sunnyvale, CA 94086.
Circle 370

Factory automation power supply

The ES281AM 280-W switcher joins the Hi-temp series of power supplies. This unit provides full output power at 60 °C and requires no fans or forced air cooling. It has a 50-kHz forward converter that regulates its three outputs to a max of 0.1%. Outputs are 5 Vdc at 45 A, 12 Vdc at 3 A, and −12 Vdc at 2A. A wide input voltage range (92 to 132 Vac) and a 20-ms holdup time prevent brownouts and missing half-cycles from power flow interruption. The unit is priced at $459 in 100 pieces. **Lorain Products,** 1122 F St, Lorain, OH 44052.
Circle 371

Uninterruptible power supplies

The GPS-5K120 series of online uninterruptible power systems are rated at 5000 VA. They are designed for use with minicomputer-based systems that perform in erratic power environments. The power supplies operate from a 120-Vac, 60-Hz, utility power line with a sealed battery backup. Available options include an RS-232 interface, batteries, custom or std enclosures, and various voltages and frequencies. The supplies include a no-break static transfer switch, two ac voltmeters, and an output ac ammeter to measure load current. **General Power Systems,** 1400 N Baxter St, Anaheim, CA 92806.
Circle 372

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Selanar Native Mode Command Structure, Area Fill, Circle, Arc and Box Commands.
Also variable scale factor for changing image size, relocatable origin, special write modes, switchable video.

SINGLE BOARD DESIGN
The SG480 is a small single board design (4.5 by 5 inches) and simply plugs into the VT100 STP port. Only one small cable is required. The SG480 comes with a replacement CRT tube and attached yoke —simple installation without critical adjustments.

DEC TERMINALS SUPPORTED
VT100, VT132. In addition Selanar has comparable products for the VT101 and VT102 plus other products for the VT100, VT103, VT105, and VT180.

HARDCOPY
Hardcopy is standard for the DEC LA34 format. Options currently available are for C.Itoh, Epson, Data South, Texas Instruments, and Selanar's SG120 PLUS with DEC's LA120.

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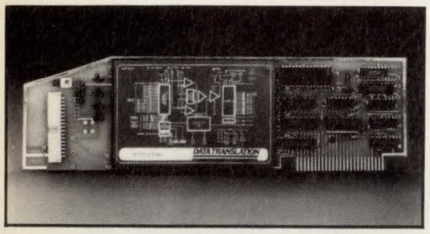
CIRCLE 157

Corporate Headquarters: 437-A Aldo Avenue, Santa Clara, CA 95050
European Headquarters: Selanar GmbH, Ahastrasse 5, 6100 Darmstadt, West Germany

Apple-compatible input boards



The DT2832 is a board-level data acquisition board for the Apple II. The plug-in analog input boards are available with 12-, 14-, or 16-bit A-D resolution. Model DT2832 includes a 12-bit ADC system, jumper selectable for 16 single-ended or 8 differential inputs. Software selectable gains are 1, 2, 4, or 8. The DT2834 includes these features but with software gains of 1, 10, 100, or 500. It accommodates a 20-mV to 10-V full-scale range. Both boards can be programmed in any language resident in the Apple computer system. Single-unit prices range from $550 to $975. **Data Translation**, 100 Locke Dr, Marlboro, MA 01752. **Circle 373**

A-D converter

The Am6108 A-D converter offers a 1-μs conversion time with 0.1% nonlinearity. It includes a precision reference, D-A converter, successive approximation registers, and control logic. The chip is housed in a 28-pin DIP that handles voltage ranges of 0 to 10 V, 0 to 5 V, and $\pm$ 5 V without external components. The converter has 3-state outputs for bus compatibility, and two status outputs—one is a std TTL signal and the other is available as a status output on the data bus. The chip is priced at $14.95 in 100s. **Advanced Micro Devices, Inc**, 901 Thompson Pl, Sunnyvale, CA 94086. **Circle 374**

Op amp and comparator

The AD630 contains a precision op amp with 2 independent differential input stages and a comparator for selection of the active channel. It has a typ small signal bandwidth (-3 dB) of 2 MHz, a 45-V/μs slew rate, and channel to channel crosstalk of -120 dB at 1kHz. The comparator provides onchip thin film resistors for pin-programmable closed-loop gains of ± 1 and ± 2 (max gain error of $\pm 0.05\%$). Min common mode rejection is guaranteed at 90 dB, with 3-μs settling time and 200-ns response time. Pricing in 100s is $9.95, $14.95, and $18.95 for AD, BD, and SD grades, respectively. **Analog Devices,** Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062. **Circle 375**

Sync converters

Series SD109 synchro to dc converters, convert 3-phase synchro or 2-phase resolver inputs to dc sin and cos outputs. The units operate at 400 conversions/s and offer a peak angular error of $\pm 3'$. Converters accept the output of a std 11.8- or 90-V 3-wire synchro or 4-wire resolver, and they provide 2 dc voltages. One voltage is the sin and one is the cos of the rotor shaft angle. The input is transformer isolated and balanced line to line. The unit is short circuit proof and meets MIL-E-5272C, E54006, and T21200. Prices start at $350 each. **Computer Conversions Corp,** 6 Dunton Ct, East Northport, NY 11731.
Circle 376

Proprietary DAC

The MP8526 is a 13-bit bipolar DAC with ± 5 and ± 10 V full scale. It uses the MSB segmentation technique, which digitally decodes the 4 MSBs into 15 equal current sources. Specs include gain error 0.1% (max), bipolar offset 0.05% max, CMOS/TTL compatible, and fast settling time (5μs typ). The chip has linearity over temp ½ LSB (13-bit) and differential linearity over temp ¼ LSB (14 bit). The 25- to 99-piece price is $130; packaging is in a 52-pin leadless chip carrier. **Micro Power Systems, Inc,** 3100 Alfred St, Santa Clara, CA 95050.
Circle 377

Talk to the editor

Have you written to the editor lately? We're waiting to hear from you.

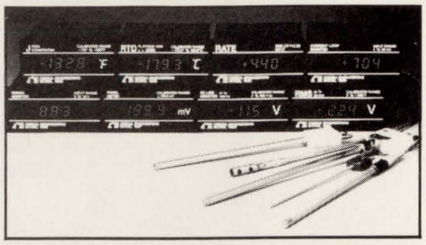
CIRCLE 158

Motion controller

The MP-500 microcomputer controller provides integration of single- or multi-axis motion and/or process control. The motion controller features a 500k-count/s input rate with an 8- or 12-bit count register for position, and 8 bits for zero position. Microprocessor based, the system can operate as a standalone controller or be integrated into a full-line management system. It provides 2K bytes of EEPROM, up to 72 I/Os, and 2 servo reference output channels. The package includes a 12″ display, membrane touch control panel, integrated cabinet, and hardware. **Possis Corp**, 825 Rhode Island Ave S, Minneapolis, MN 55426.
Circle 378

Digital indicators in monitors

The 199 letter series are process monitors with a modular design. They can be adapted to any input frequency via easily accessible DIP switches or plug-in modules. Features of the monitors include universal power sources, parallel BCD output, analog output, and an



operating range of −10 to 50 °C. The monitors are capable of monitoring any process measurement thermocouple, RTD, rate, current loop, voltage, or rms display. Prices start at $104. **Omega Engineering, Inc**, One Omega Dr, PO Box 4047, Stamford, CT 06907.
Circle 379

Computer development system

A modular control computer, the Stack 65 has multiple, programmable serial and parallel ports. The computer is AIM-65 software compatible and can serve as its own development system when used with a dumb terminal or personal computer. Microprocessor, I/O, memory expansion, and program development functions are on individual cards. Each card has two 20-pin bus connectors which also space the boards 0.5″ apart. Memory expansion boards can hold 2K or 4K RAMS or ROM/PROMS with 64K-byte address space. **duTec, Inc**, 4801 James McDivitt Rd, PO Box 964, Jackson, MI 49204.
Circle 380

Module with 16 voltage inputs

An analog input module, the RM65-5302E can be used in any RM65/RME-based system application that samples analog signals. The module provides for either 16 single-ended or 8 differential analog input channels. A-D conversion provides 12-bit resolution and can be calibrated for 12-bit accuracy over five selected voltage ranges. These include unipolar 0 to 5 V and 0 to 10 V, and bipolar ±2.5, ±5, and ±10 V. The module is Eurocard sized (100 x 160 mm) with a std DIN-41612 connector. It is priced at $375. **Rockwell International**, 4311 Jamboree Rd, PO Box C, Newport Beach, CA 92660. **Circle 381**

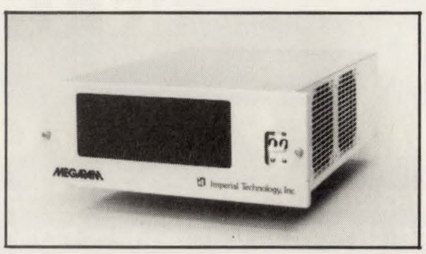
MEMORY SYSTEMS

Intelligent minifloppy

The FDS-100 minifile is an intelligent minifloppy disk system with a 5¼″ floppy disk drive, power supply, micro controller, and an RS-232-C interface. Storage capacity is 89K bytes, single sided and 179K bytes, double sided. The front panel keyboard allows control of all file management functions, which are resident in firmware. Switch-selectable options include baud rate, number of stop bits, hardware synchronization, and features for custom applications. **Atek NC Corp**, 887 Main St, PO Box E, Monroe, CT 06468.

Circle 382

Disk emulator



A nonrotating disk emulator system, the MegaRam 7000 is all solid state semiconductor storage with no moving parts. The system features 10M bytes of memory with expandability to 16M bytes, battery backup option, and full error detection and correction. The error checking and correction (ECC) capability (on a per word basis) results in improvement in MTBF. The battery backup consists of a power supply assembly to replace std assembly, and it supports a 4M-byte system for approx 2 h. **Imperial Technology, Inc**, 831 S Douglas St, El Segundo, CA 90245.
Circle 383

VAX-11/750 upgrade kit

A packaged main memory upgrade kit for the VAX-11/750 allows the CPU to be expanded up to 8M bytes. Formerly constrained by the 2M-byte system limit, the kit's expandability gives users added capabilities. When field conversion is finished, user is left with 0.25M-byte cards that the company will buy back. The avg price of the min 2M-byte upgrade kit designated model VX-2MB-750CA is $11,500 without trade-in. Additional 1M-byte memory cards are $2450. **EMC Corp**, 385 Elliot St, Newton, MA 02164.
Circle 384

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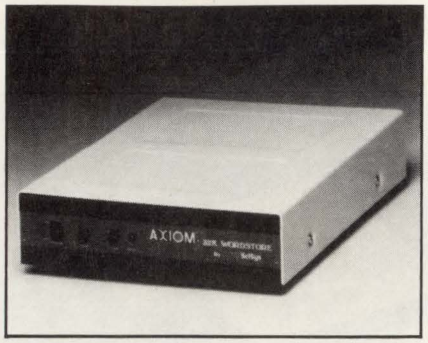
Cartridge drive subsystem

The model 70S cartridge drive is compatible with any 8080/8085/Z80-based system that contains an S-100 bus. A single S-100 controller card supports eight tape drives. The subsystem operates as a nonintelligent I/O memory to the host and stores up to 17.3M bytes of unformatted data at a 20k-byte/s transfer rate. Record length can be selected from 256 to 32K bytes with a max formatted storage of 16.6M bytes. Max effective storage rate is 1.1M bytes/min. **Digi-Data Corp,** 8580 Dorsey Run Rd, Jessup, MD 20794.

Circle 385

Small computer printer buffer

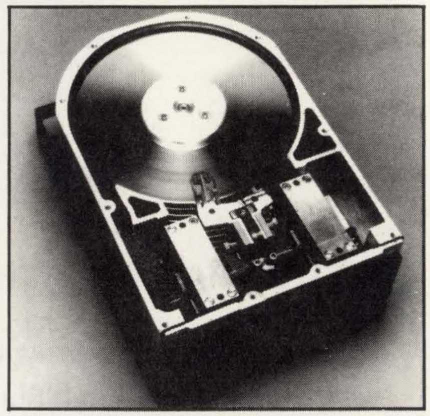


Wordstore is a 32K-byte printer buffer that takes over the task of communicating with the printer, leaving the computer free to handle other chores. Data compacting, a feature of the buffer, permits repeated characters to be compressed to save memory space. Copy mode allows a user to print multiple letters or documents using only the memory required for a single message. Available with 32K bytes of memory, the buffer can be upgraded to 64K bytes. Wordstore, with 32K bytes, is priced at $199. **Axiom Corp,** 1014 Griswold Ave, San Fernando, CA 91340.

Circle 386

Winchester family

The 500 series of 5¼" Winchester disk drives feature 32-ms access time and storage capacities ranging from 55M to 111M bytes. Model 502 has 4 disks storing 55M bytes while model 504 has 6 disks storing 86M bytes. Models 503 and 505 have 71M and 111M bytes of unformatted storage capacity, on 4 and 6 disks, respectively. The 502 and 504 specify a 0.625M byte/s transfer rate and 9212 bpi recording density. Specs for the 503 and 505 are 0.806M bytes/s and 11,886 bpi. In quantities of 500, prices range from $1550 to $2500. **Priam Corp,** 20 W Montague Expy, San Jose, CA 95134.



Circle 387

High MTBF Winchesters

The D5200 family consists of four 5¼" Winchester disk drives. These drives offer unformatted capacities of 6.4M, 12.9M, 19.3M, and 25.8M bytes. They also offer a direct-drive dc spindle motor and micro controls for an MTBF of 12,000 power on hours. The drives have an 85-ms avg access time, a 5M-bps data transfer rate, and a 3600-rpm rotational speed. The drives are intended for use by small business and personal computer OEMs and systems integrators. The 100-piece pricing ranges from $915 to $1410. **NEC Information Systems, Inc,** 5 Militia Dr, Lexington, MA 02173.

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CIRCLE 161

CIRCLE 162

Cartridge Winchester

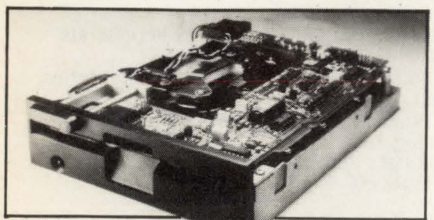
Designed to use with the Intellec microprocessor development system that runs the ISIS-II operating system, the DataSafe -8/8R is a fixed/removable Winchester subsystem. It provides 8M bytes of fixed and 8M bytes of removable storage. Each 5¼" cartridge holds 42k, 128-byte blocks. A std copy program is used so no software changes are required. In addition, a special track-to-track copy program copies an entire cartridge to or from the fixed Winchester in 3 min. With a full 1-year warranty, the Winchester is priced at $8995. **Winchester Systems, Inc**, 14 Laurel Hill, PO Box 545, Winchester, MA 01890. **Circle 389**

Cache board increases speed

The OR-88C disk cache memory board works in conjunction with the floppy disk controller in the MDS series of development stations. It increases the computer speed by three times, on the average, and provides 480K bytes of storage capacity. One board supports four double- or two single-density floppy drives and is fully compatible with ISIS® and CP/M. The cache board uses an 8088 to control the memory and data transfer allocations. Memory allocation is based on the LRU algorithm in which sectors that have been dormant the longest are replaced first. In single quantities, the board is priced at $2850. **Origin, Inc**, 9136 Gibson St, Los Angeles, CA 90034. **Circle 390**

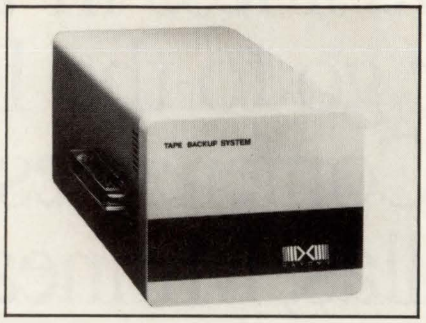
Half-height drives

Five different models of 5¼" half-height floppy drives are equipped with a unique ball bearing carriage. Storage capacity for 96-tpi drives range from 500K bytes to 1.6M bytes (unformatted) with a 3-ms access time. Storage capacity for the 48-tpi drives ranges from 250K to 500K bytes (unformatted) with a 6-ms access time. Features include a read/chain design for data integrity improvement, self-centering clutch, band positioner for fast access time, and an auto disk eject. **Hi-Tech Peripherals Corp**, 15192 Triton Ln, Huntington Beach, CA 92641.



Circle 391

IBM PC/XT streaming tape drive



This standalone streaming tape drive backs up any Winchester disk or floppy drive used with the IBM PC or XT. Key specs include a cartridge capacity of 20M bytes (unformatted), 18M bytes (formatted), a 90-ips linear speed, and an 8k-bpi density. The system uses NRZI bit serial, 4-track serpentine recording and a 450'-tape. Transfer rate is 90k bps (burst) and 28.9k bps (avg). Backup is accomplished by volume or individual file. Four error checking methods ensure data integrity. The drive is priced at $2195. **Davong System Inc**, 217 Humboldt Ct, Sunnyvale, CA 94089. **Circle 392**

Fixed/removable Winchesters

The series 8 Winchester disk system features an 8" removable hard disk that holds 10.6M bytes of storage. The system provides minicomputer designers with fixed and removable media add-on subsystems. Advantages of the system include easy handling for backup files as well as rapid editing of file dates and programs. Series 810 has a single cartridge drive; the 853 drive is fixed and is equivalent to 4 DEC RL02 drives. Single-unit price for the 810 is $4550 and for the 853 is $7800. **Xacom Technology Inc**, 560 Forbes Blvd, South San Francisco, CA 94080. **Circle 393**

Funnel std cartridge drive

The Serpentine funnel is a ¼" digital cartridge tape drive set to the industry-std start/stop drive. A bidirectional R/W head allows 4 tracks to be read forward and backward so the tape is never rewound. Memory capacity is 21.3M bytes and the transfer rate is 24k bytes/s. The 30-ips R/W speed and the 90-ips search are the same as on the std funnel. Applications for the drive include Winchester disk backup, as a full function tape peripheral, or in data acquisition. In 1000-piece quantities, the drives are priced at $900. **Data Electronics, Inc**, 10150 Sorrento Valley Rd, San Diego, CA 92121. **Circle 394**

Mag tape subsystem

The Sperry 5055/Uniservo 28 magnetic tape subsystem offers high speed group coded recording (GCR) tape capability. The subsystem is a dual-density GCR/phase encoded (PE) unit with tape speed of 125 ips. It provides a transfer rate of 750k bps GCR and 200k bps PE. A second unit, the Uniservo 26, has a tape speed of 75 ips and transfer rates of 480k bps GCR and 120k bps PE. The tape subsystem can be configured from 1 to 8 tape units and 1 or 2 control units. It provides a dual channel option allowing the control unit to attach to 2 block MUX channels. Purchase price is $22,000 for the Uniservo 26 and $24,750 for the Uniservo 28. **Sperry Corp, Computer Systems**, PO Box 500, Blue Bell, PA 19424. **Circle 395**

High capacity disk subsystem

The Magnum disk subsystem is designed for industrial applications that need large online data storage with rapid access times and a more highly available system. It has one or two 140M-byte data modules, or it can be configured as a master/slave subsystem that can store up to 560M bytes on 1 I/O channel. Transfer rates through cache memory have a peak throughput of 1.2M bytes/s with an avg seek time as low as 25 ms. MTBF with 2 data modules is 2500 h, with 1 module, 4000 h. Built-In-Test isolates faults in 1 of 6 field replaceable modules. Subsystem provides support for shared data storage through the use of dual data ports. The quantity-1 price (military spec) is $94,000. **ROLM Corp**, 1 River Oaks Pl, San Jose, CA 95134. **Circle 396**

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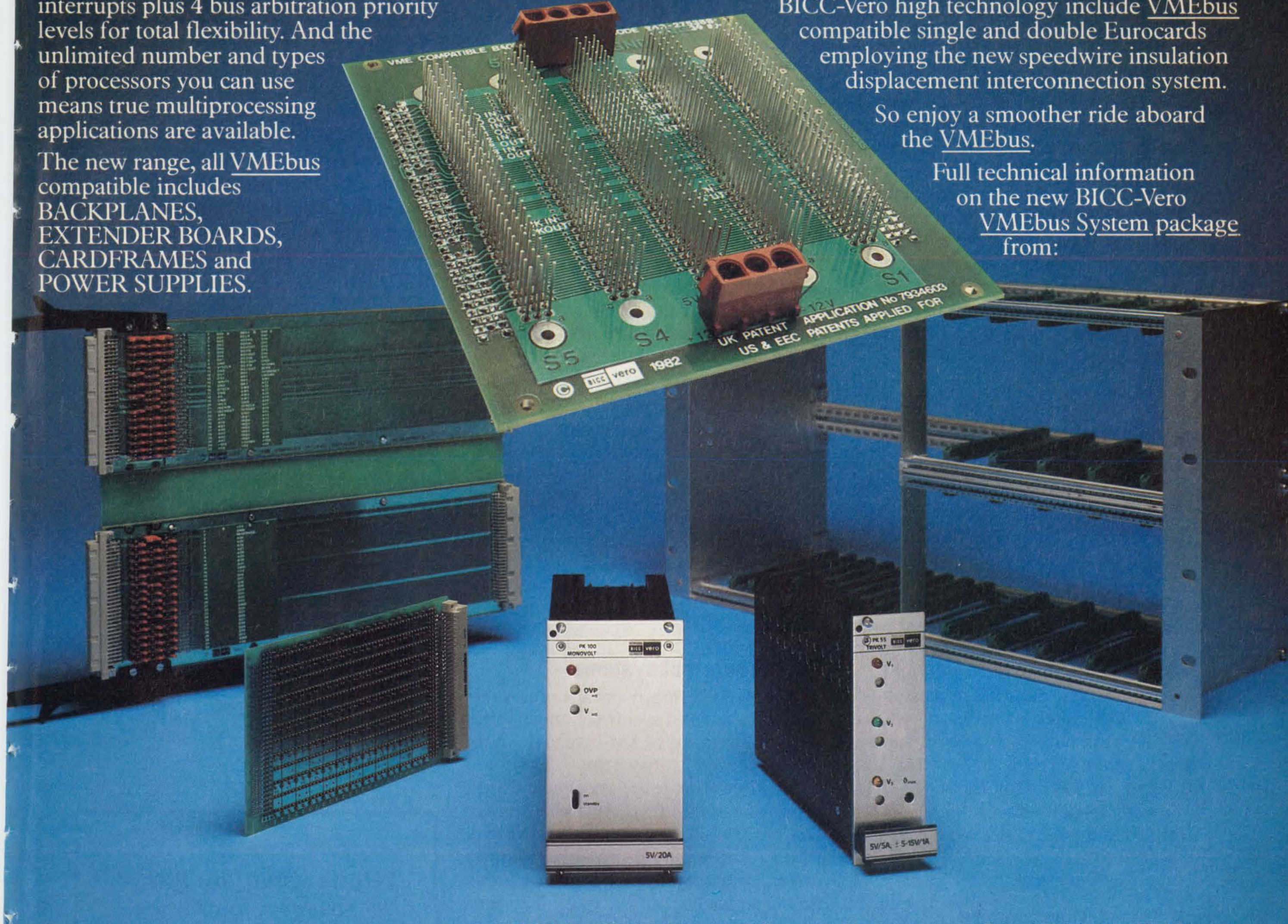

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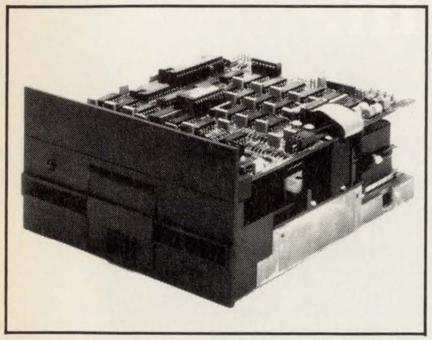
CIRCLE 163

3.2M-byte 5¼″ floppy drive



The RFD 3200 5¼″ flexible disk drive features 3.2M bytes of memory capacity. It offers 170 tpi in a double-sided version with a 500k-bit transfer rate. The electrical interface and data formats are industry and ANSI compatible for std 8″ diskette drives and controllers. The drive provides a 3-ms track to track access time; the direct drive dc motor's MTBF is 30,000 h. A reference track is built into the unit to control the positioning system. The step motor micro steps to the accurate location on the desired track. **Ex-Cell-O Corp, Remex Div,** 1733 E Alton Ave, Irvine, CA 92714.
Circle 397

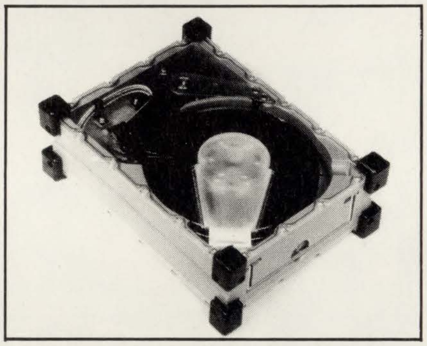
Multibus RAM

The VLS system provides 4.5M bytes of high speed Multibus memory. The memory has a 440-ns cycle time with faster response times available. Designed to alleviate program partitioning, resource sharing, and memory fragmentation, the system allows memory mapping, paging, and segmentation through the 16M-byte range. It supports systems with 16-, 20-, and 24-bit address buses and allows an 8-bit processor access to 16M bytes of memory with a 16-bit address bus. OEM pricing for the system ranges from $1295 for the 512K-byte to $9995 for the 4.5M-byte. **Advanced Digital Technology,** 14125 Capri Dr, Suite 4, Los Gatos, CA 95030.
Circle 398

Half-height Winchesters

The TM250 family of Winchester drives, which includes models TM251 and TM252, features plated media and 6.4M- and 12.8M-byte capacities. The half-height drives have a 345-tpi track density; recording density is 9074 bpi; and they use 306 cylinders. The TM251 has 5M bytes of formatted capacity with recording performed on both sides of a disk. The TM252 has 10M bytes of formatted capacity. An onboard micro calculates position for an avg access time of 85 ms, head settling time of 15 ms, and an avg latency of 8.33 ms. The TM251 is priced at $425 and the TM252 at $500. **Tandon Corp,** 20320 Prairie St, Chatsworth, CA 91311. **Circle 399**

MIL spec Winchester



A cartridge-loaded Winchester disk drive, RD-5/15 is designed for high speed mass data storage in military computers. The drives transfer data at a 5M-bps rate with a 40-ms avg access time. Storage capacity is 15M bytes on a 5¼″ plated disk media. The intelligent interface allows easy interfacing to most computers. Features include formatting, error detecting/correcting, addressing, and device controlling. The drives comply with MIL-E-16400/MIL-E-5400/MIL-E-4158 standards. **Miltope Corp,** 1770 Walt Whitman Rd, Melville, NY 11747.
Circle 400

20.8M-byte subsystems

Available with floppy or tape removable media for I/O and archival storage, series 6000 additions are 20.8M-byte, 5¼″ Winchester-based subsystems. They are compatible with LSI-11 systems and with series 6000 computers. Available storage can be combined with a single 1M-byte floppy drive, dual 1M-byte floppy drives, or a 20M-byte ¼″ tape cartridge drive for backup and storage. The subsystems use formatting capabilities to allow multi-user configurations. Two 20.8M-byte subsystems can be configured to provide 41.6M bytes of Winchester mass storage. Prices range from $4550 to $11,250, with OEM discounts available. **Plessey Peripheral Systems,** 17466 Daimler, Irvine, CA 92714.
Circle 401

Fixed media disk drive

The 9794 Winchester disk drive emulates DEC's RMOS and has a 315M-byte capacity. The 256M-byte formatted capacity combines a 25-ms avg head positioning time with an 8.3-ms avg rotational latency to yield a 34-ms avg access time. CPUs connect to the storage devices via MASSNET, a high speed network that supplies up to 64 nodes within a 1-mile radius. The storage device can access any part of the 55G bytes of stored data within tens of seconds. **System Industries, Inc,** 1855 Barber Lane, PO Box 789, Milpitas, CA 95035.
Circle 402

11/23 compatible memory boards

For use with the 11/23, the CI-1123 plus is a dynamic memory system. It has 1M byte on a single dual-width board. It features check parity with onboard control status register, and 64K- and 256K-byte RAM with 240-ns access time and 400-ns cycle time. Power requirement is 1.2 A max from a 5-V supply. The board is easily configured for battery backup supply for 1M byte of memory in the down state. The CI-1123 plus is available in 256K-, 512K-, and 1M-byte configurations with prices ranging from $595 to $3995, **Chrislin Industries, Inc, Computer Products Div,** 31352 Via Colinas, Suite 102, Westlake Village, CA 91361.
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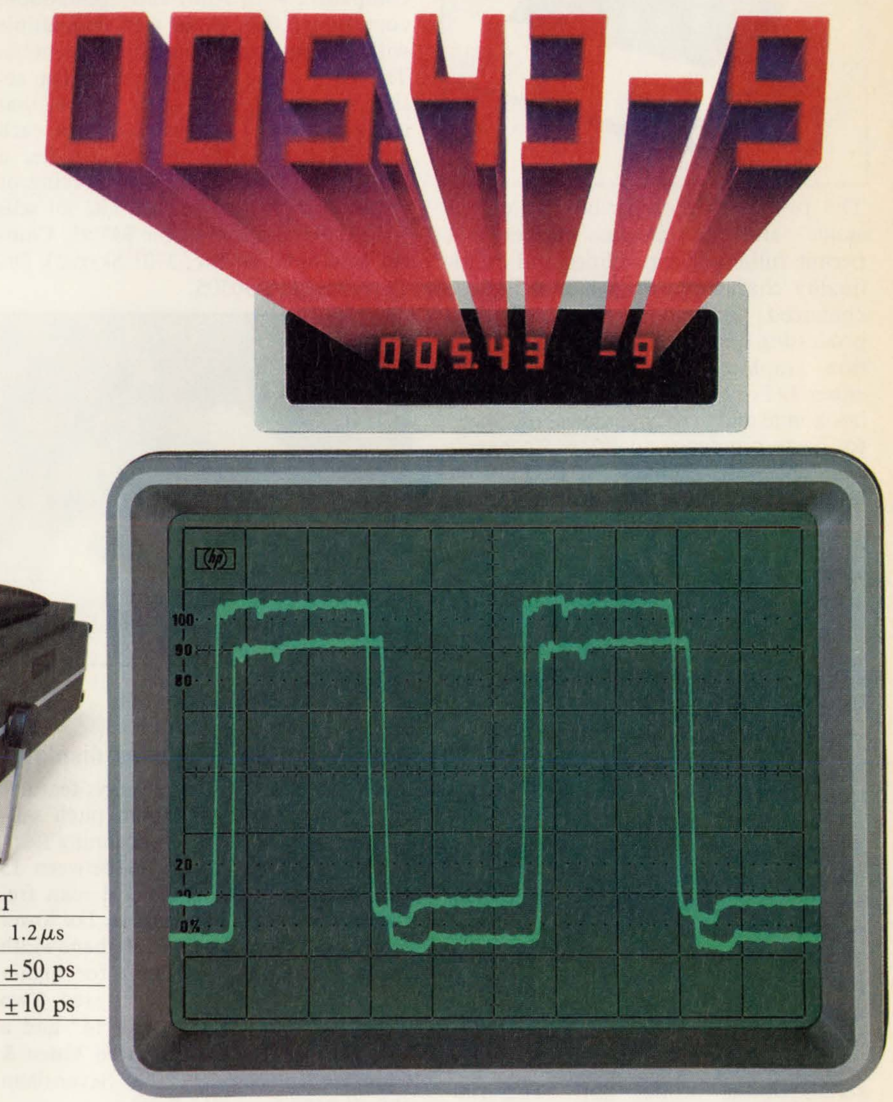

If the accuracy of your timing measurements must keep pace with the latest technology, the HP 1726A Time Interval Oscilloscope is your best solution. It can handle tough timing problems. Although most general-purpose, laboratory oscilloscopes solve a variety of problems, their timing accuracy is typically design limited to ±500 picoseconds. This simply is not adequate for designing and producing many of today's products.

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HP's 1726A time-interval oscilloscope solves this timing limitation with a revolutionary approach. Its new method of making timing measurements is based on combining HP counter technology with HP's advanced oscilloscope triggering circuits. The results? New levels of accuracy (±50 ps), resolution (±10 ps), and repeatability (±30 ps). All this in a portable package

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TIME INTERVAL	500 ps	5 ns	1.2 μs
1726A Accuracy	±50 ps	±50 ps	±50 ps
1726A Resolution	±10 ps	±10 ps	±10 ps

that won't clutter your bench or test station. Typically, the 1726A's accuracy is a factor of ten improvement over most laboratory scopes, including the one you're probably using or planning to purchase.

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Check the time interval table.

With the 1726A, your time-interval answers are consistently accurate...and oscilloscope timing calibration is preserved even with its Time/Div vernier out of detent. In fact, intervals as long as 1.2 μs can be measured with ±50 ps accuracy.

For unprecedented convenience and ±30 ps repeatability, dial in start/stop trigger levels with 1 mV resolution, position the on-screen markers, and read the answer on the 1726A's LED display. You get fast, convenient, results you can trust...time after time.

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CIRCLE 164

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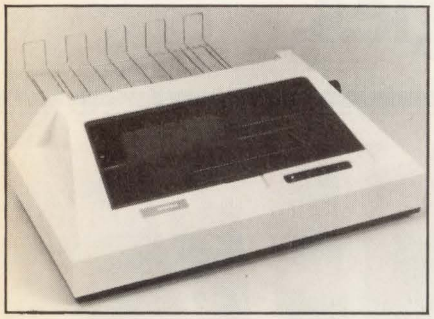
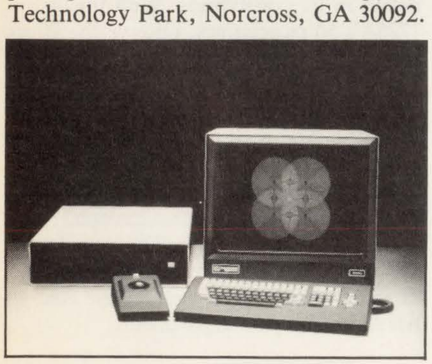
Multimode printer



The DP-9725A Color/Scribe printer has single- and multiple-pass modes that permit full-color capabilities and multiquality characters. Four modes include enhanced, correspondence, and data processing quality as well as high resolution graphics. Graphics resolution is either 144 dots/in or 72 dots/in, in both horizontal and vertical dimensions. Speed for correspondence quality is 50 chars/s at 10 chars/in, 60 chars/s at 12 chars/in; in enhanced mode, 164 chars/s for 10, 12, 15, and 16.4 chars/in. Single-quantity price is $2350. **Anadex Inc,** 9825 De Soto Ave, Chatsworth, CA 91311. **Circle 404**

Color graphics terminal is Tek 4014 compatible

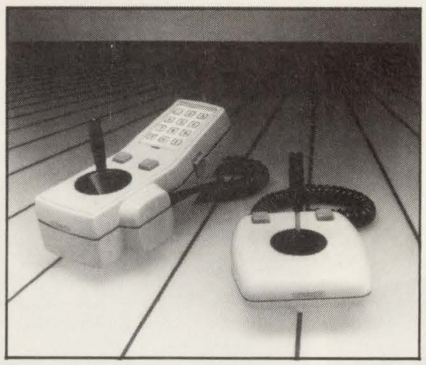
The VHR19 is a 1024 x 1024 color graphics terminal, designed for applications where color, speed, and Tektronix 4014 compatibility are needed. A total of 4096 colors are available with eight of them concurrently displayable in a 19″, bit-mapped display. The terminal supports full graphics commands; four sizes of character sets are included plus two graphics character sets, one of which is user definable. Features include an RS-232-C serial port with 50 to 19.2k baud, DMA channel, auxiliary I/O port, and serial/parallel printer port. The 100-piece price is $3995. **Intecolor Corp,** 225 Technology Park, Norcross, GA 30092.



Circle 405

Analog joystick

Two contoured joysticks provide precision control, quick response, and ease of operation. The joysticks are available in two models. The CR-301 and CR-401 are compatible with Atari and Commodore computers; the 401 is also compatible with Apple and Franklin computers. The 401 is a true analog joystick with action supported by a single gimbal that actuates dual 100k pots, one in each axis. With a self-centering handle, a player can select either free floating or centered stick movements. The 301 sells for $19.95 and the 401 for $44.95. **Comrex International Inc,** 3701 Skypark Dr, Torrance, CA 90505.



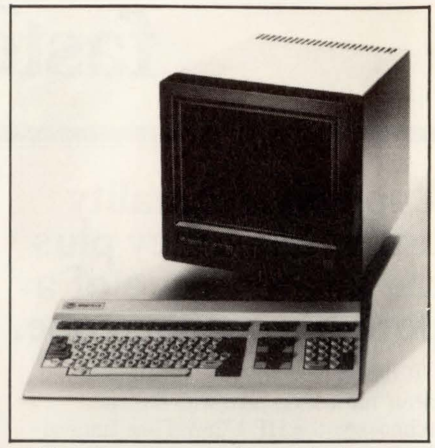
Circle 406

High resolution graphics displays

The CDCT 5000 series of displays features a high resolution, 0.31-mm pitch self-convergent CRT. It offers scanning flexibility with live frequencies between 15 and 37.5 kHz and a vertical scan frequency between 38 and 80 Hz. For lower frequency ranges, a 25-MHz bandwidth analog video amp is used; for higher scanning, a 50-MHz device is used. Two screen sizes are available: a 14″ and a 20″, both black matrix. **Barco Video & Communications** nv, Th Sevenslaan 106, B-8500 Kortrijk, Belgium.
Circle 407

European display terminal

A video display terminal for the European market, the Eurobee FT-10 has a 14″ (35.5-cm) screen. The terminal uses an 8085 with 6K bytes of RAM (expandable to 40K bytes). The screen has 80 cols, 24 rows of data with a 25th for status. The keyboard has 107 key stations including a 14-key numeric pad and 8 function keys. All European character sets are in the terminal, as are 161 graphics symbols and 16 bar codes. Features include



editing, memory and line lock, ASCII comm code, RS-232 interface, and transmission rates from 50 to 19.2k baud. The terminal is priced at $1085. **Beehive International (UK) Ltd,** Index House, Ascot, Berkshire, SL5 7EU, England.
Circle 408

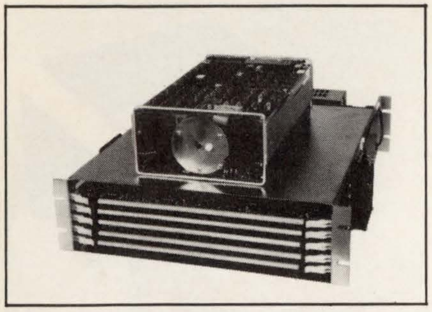
RGB color displays

Model DT-D1300D is a 13″ RGB/composite computer display. It is compatible with the IBM PC, Apple III, and Panasonic JR-200. The CRT is a direct etched non-glare type. The unit accepts a composite video input; the alternate RGB input features a multipin input connector. Interface allows generation of 16 colors when connected to the IBM PC or Apple. In RGB mode, 2k chars in 80 x 25 format are displayed. In composite mode, 1k chars in 40 x 25 format are displayed. The unit has a built-in audio system. **Panasonic Industrial Co,** Information Systems Group, 1 Panasonic Way, Secaucus, NJ 07094.
Circle 409

High resolution display processor

Model 3700 color display processor offers flicker-free, 1280 x 1024, 60-Hz high resolution, noninterlaced color graphics. Special hardware allows it to write in 80-pixel blocks, resulting in fast writing speeds of up to 42M pixels/s. Vector write time is 750 ns/pixel (continuous speed) and up to 4096 colors can be displayed simultaneously from a palette of 16.7M colors. Options include hardware cursor, hardware pan and zoom, and graphic input devices such as data tablet, keyboard, joystick, and trackball. Prices range from $9995 to $18,700. **Lexidata Corp,** 755 Middlesex Tpke, Billerica, MA 01865.
Circle 461

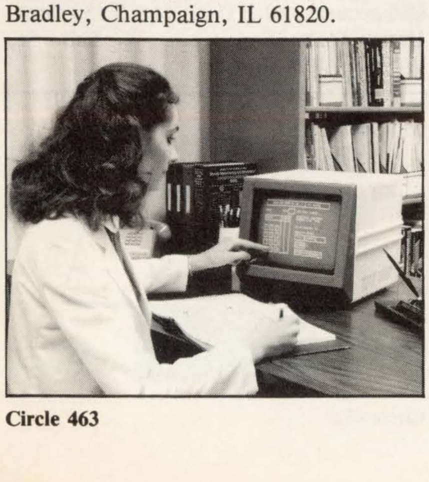
Voice processing subsystem



The VoiceStor model 30 is a voice storage subsystem for high level voice response and storage retrieval. The device records and plays back words, phrases, or sentences exactly as spoken. Its vocabulary is very flexible with no fixed limit on any element. Recording capacities vary from 100 s to 60 h, depending on the applications. It supports up to 32 simultaneous voice channels, allowing access to several sources on an async basis. The system interface is a std RS-232-C control channel operating at a range of data transmission rates. **Voicetek Corp,** 10 Dedham St, Newton, MA 02161.
Circle 462

Touch-active system

The Touch Information Display touch terminal uses opto-technology with no overlay. This technology gives a clear view of the screen and is difficult to damage. The display allows the user to define a variety of touch-active areas for more flexible programming in a wider range of applications. The interface is an RS-232-C and an ASCII port is std. The display is 24 lines x 80 chars on a 12″ screen, and the character set is 96 ASCII plus 32 special graphic symbols. The display sells for $1400. **Electro Mechanical Systems, Inc,** 801 W Bradley, Champaign, IL 61820.



Circle 463

Fast display generator

The 2020 color graphics display generator offers 675k short vectors/s. It is designed with pipelined, parallel coprocessors and a 32-bit VMEbus structure. It features a writable control store implemented in RAM and a 3½″ microfloppy for added software capability. The peripheral uses multiple MC68000s, and bit-slice processors handle complex bit manipulations. Vectors are drawn at a 37- to 74-ns/pixel rate. Each memory board in the display contains two bit planes of 1280 x 1024 bits each. The display is priced at $32,700 in the basic configuration. **Ramtek Corp,** 2211 Lawson Lane, Santa Clara, CA 95050.
Circle 464

Emulating graphics terminal

The 2427 color graphics terminal offers dual-processing power. With single commands, it emulates the Tektronix 4010/4014. Programs written in the Tektronix protocol can run with plotting, interactive mode, status reporting, and printing. Also compatible with the 4027 color graphics terminal, the 2427 emulates commands and features that include arcs and regular polygons, area fill, and printer interface to dot-matrix printers. The design includes a 16-bit Z8002 CPU with alphanumeric functions handled by a dedicated 8085 processor. Graphics resolution is 560 x 288. The unit is priced at $1995, quantity 100. **Intecolor Corp,** 225 Technology Park, Norcross, GA 30092.
Circle 465

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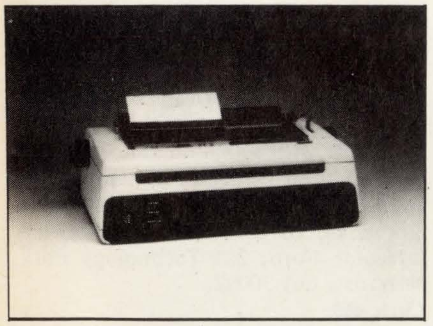
Printer has drop-in printwheel



The 4560 Generation II daisy wheel printer features an easy drop-in printwheel with up to 112 chars. The model offers boldface, shadow printing, and auto underlining. It comes equipped with a 2K-byte input buffer and an RS-232 interface. Paper handling is friction feed with an optional tractor. A cartridge ribbon is available in a single- or multistrike film. Baud rate and DIP switches are accessible from the outside to easily change the functional parameters. The printer features a noise level of less than 60 dBa. It is priced at $1095. **Facit, Inc**, 235 Main Dunstable Rd, Nashua, NH 03061.

Circle 466

Low cost dot-matrix printers

Dot-matrix printer mechanisms, models 81 and 82 are suitable for use in ECR/POS systems, mobile printer applications, and data logging. Data are printed in any desired dot-matirx pattern based on a 7-needle vertical dot array (5 x 7, 7 x 7, 9 x 7). Both printer units are alphanumeric and bidirectional. They consist of two separate assemblies: the main printer and a paper handling device. Model 81 prints 38 cols at 13 chars/in and model 82 prints 18 cols at 13 chars/in. The printhead life expectancy is 75 x 10^6 at 14 dots/char. Both models are priced below $100. **Westrex OEM Products,** 51 Penn St, Fall River, MA 02724.

Circle 467

High speed printer

The 4111 colorgraphic printer produces color paper hard copy or overhead transparencies in less than 60 s. The thermal printer duplicates an image on a CRT screen. Each dot on the hard copy corresponds to the CRT screen's 640 x 480 pixel resolution. The screen image is reproduced at a 160- x 120-mm size. A subtractive color transfer process uses yellow, magenta, and cyan to produce hard copy in eight colors. The printer provides multiple paging in several alphanumeric formats, ranging from 80 chars x 24 lines to 132 chars x 48 lines. Price is $6500. **Ramtek Corp,** 2211 Lawson Lane, Santa Clara, CA 95050.

Circle 468

Two bit-map terminals

Model 480 and 489 are graphics terminals with 640 x 480 graphics resolution and 60-Hz noninterlaced displays. Display features include 8 screens of character memory, 48 line operations, and a vertically split screen that allows display of 96 half lines. Graphics features are geometric functions, drawing modes for draw behind/draw over, and scaling and clipping. Cross-hair cursor is used for graphic input; with pan and zoom it provides location and magnification of points of interest. Three planes of bit-map memory provide 1024 x 512 pixels with each pixel definable in 1 of 8 colors. The 480 costs $5000; the 489 is priced at $5500, with volume discounts available. **Colorgraphic Communications Corp,** 2379 John Glenn Dr, PO Box 80448, Atlanta, GA 30366.

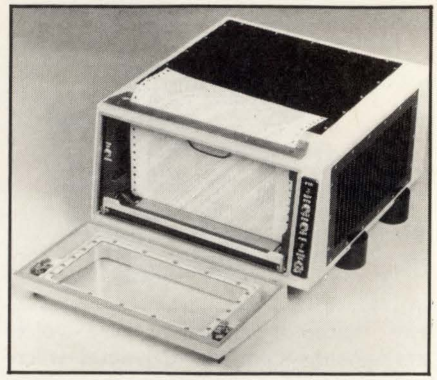
Circle 469

High speed remote printer

A remote line printer connects to the parallel printer port of many computer systems, thereby eliminating software modifications. It includes data compression, print buffering for high throughput, and built-in diagnostics. Other features/options include an aux stat MUX channel, allowing a CRT to be connected to the system for remote job entry; an auto dialer that stores and recalls up to 50 remote site numbers; and satellite circuit compatibility. The printer can be used in a direct connect configuration at speeds up to 56k baud. **Digital Associates Corp,** 1039 E Main St, Stamford, CT 06902.

Circle 470

Printer/plotter upgrade

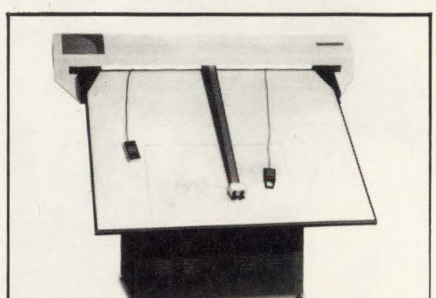


The TP3000 graphics printer/plotter has been upgraded to print up to 750 lines/min. The military tactical device meets the following specs: MIL-T-21200, MIL-E-16400, MIL-E-5400, emi per MIL-STD-461A and Tempest per Nacsem 5100. The thermal printhead spans an 8″ paper width and provides high resolution graphics at 100, 153, or 200 dots/in, both horizontally and vertically. It prints a 64 ASCII char subset in 80-col (10-char/in) and/or 132-col (17-char/in) formats. **Miltope Corp,** 1770 Walt Whitman Rd, Melville, NY 11747.

Circle 471

Digitizer and plotter

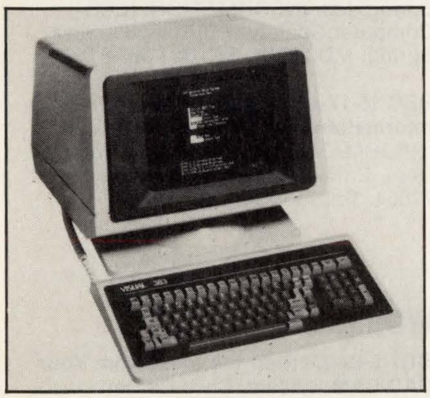
A combined digitizer/plotter, designated the DP4060, allows operators to digitize graphical information and plot back on the same surface. This technique lets the user verify the entered data, edit the information, and produce the final engineering drawing. The digitizing area is 42″ x 60″ (1066 x 1524 mm), which allows ample space for a menu. Resolution is 0.001″ (0.025 mm) and accuracy is 0.010″ (0.254 mm). The plot area is the same as the digitizing area with a resolution of 0.0025″ (0.0635 mm) and accuracy of ±0.006″ (±0.153 mm). **Data Technology, Inc,** 4 Gill St, Woburn, MA 01801.



Circle 472

Emulating terminal

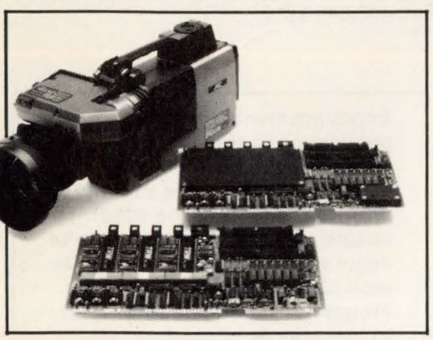
A video display terminal, the Visual 383 emulates the Burroughs TD830 terminal. A tilt and swivel display, 14" nonglare screen, and N-key rollover keyboard are terminal features. Power-on diagnostics, line-monitor mode, printer support, user definable keyboard (which includes 8 programmable keys—16 with shift), and std Burroughs poll/select protocol allow easy integration into present systems. Other features include six display pages, selectable interface, dual logic stations, and local forms storage. The terminal is priced at $1695. **Visual Technology Inc,** 540 Main St, Tewksbury, MA 01876.



Circle 497

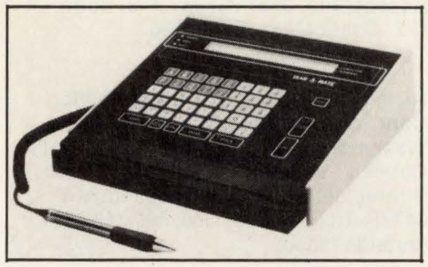
Realtime digitizer

A color RGB video digitizer, RGB-512 is plug compatible with either the Multibus or the Q-bus. It captures 3 channels of decoded RGB video images in 1/30 of a second. Sequential signals are digitized in 3 x 1/30 of a second. Three flash ADCs digitize each signal at 5 or 10 MHz to 6 to 8 bits of accuracy. Each channel provides 4 bits of graphics overlays. Other features include 50/60-Hz compatibility PLL circuit, and switchable int/ext sync source. Digitizer is $7495. **Imaging Technology, Inc,** 400 W Cummings Park, Woburn, MA 01801.



Circle 498

Data terminal reads bar codes



The D5 series reader/terminal combines a bar code reader with a data terminal in one package. Features include an alphanumeric keyboard, a 2-line/80-char LCD, and 2-way communications via RS-232, RS-442, or 20-mA current loop interfaces. Without changing switch settings or software, the unit decodes interleaved 2 of 5, code 3 of 9, Codabar, UPC-A, UPC-E, EAN-8, and EAN-13. Bar code data can be entered by a code pen, an external fixed beam or moving beam scanners, or an integral card slot scanner. **Skan-a-matic Corp,** PO Box S, Elbridge, NY 13060.

Circle 499

Thermal printer

Model 822 is a microcomputer-controlled ASCII character printer for use with computers, data terminals, and instrument systems. This alphanumeric thermal printer interfaces to the IEEE 488 instrumentation bus and acts as a listener in either the addressed or listen-only modes. In the addressed mode, primary addresses from 0 to 31 are front panel switch selectable. In the listen-only mode, all messages on the bus are printed regardless of address. Prices start at $745 in single quantities. **Newport Electronics, Inc,** 630 E Young St, Santa Ana, CA 92705.

Circle 500

Premier Edition Preview—
Artificial intelligence for office automation systems —in late October.

CONFERENCES

OCT 2-5—Robotech (Internat'l Conf and Exposition for the Application of Automated Manufacturing Technology), Curtis Hixon Convention Hall, Tampa, Fla. INFORMATION: Tom Will, Latcom Inc, 4135 Laguna, Coral Gables, FL 33146. Tel: 305/667-5150

OCT 3-6—Data Communications Symposium, Sea Crest Lodge, Falmouth, Mass. INFORMATION: Kenneth J. Thurber, Architecture Technology Corp, PO Box 24344, Minneapolis, MN 55424. Tel: 612/935-2035

OCT 5-6—Compusource, Red Lion Inn and Convention Ctr, San Jose, Calif. INFORMATION: Norm De Nardi Enterprises, 289 S San Antonio Rd, Suite 204, Los Altos, CA 94022. Tel: 415/941-8440

OCT 8-10—PC (Internat'l Exposition and Conf Featuring IBM Personal Computers and Compatibles), Bayside Exposition Ctr, Boston, Mass. INFORMATION: Northeast Expositions, Inc, 822 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000; 800/841-7000 (outside Mass)

OCT 10-13—ISA (Instrument Society of America) Internat'l Conf and Exhibit, Astrohall, Houston, Tex. INFORMATION: Philip Meade, ISA, 67 Alexander Dr, PO Box 12277, Research Triangle Park, NC 27709. Tel: 919/549-8411

OCT 10-14—Fiber Optics and Communications LANs, Bally's Park Place Hotel, Atlantic City, NJ. INFORMATION: Barbara Coffin, 138 Brighton Ave, Boston, MA 02134. Tel: 617/787-1776

OCT 14-15—Forth Interest Group Conv, Hyatt Palo Alto, Palo Alto, Calif. INFORMATION: Linda Kahn, PO Box 1105, San Carlos, CA 94070. Tel: 213/478-7398

OCT 18-20—Internat'l Test Conf, Franklin Plaza Hotel, Philadelphia, Pa. INFORMATION: Doris Thomas, PO Box 371, Cedar Knolls, NJ 07927. Tel: 201/267-7120

OCT 24-26—IEEE Internat'l Symposium on Electromagnetic Compatibility, Shoreham Dunfey Hotel, Washington, DC. INFORMATION: IEEE EMC '83, PO Box 2228, Rockville, MD 20852. Tel: 301/984-8400; 800/638-0111 (outside Md)

OCT 31-NOV 3—Internat'l Conf on Computer Design: VLSI in Computers, Rye Town Hilton, Port Chester, NY. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

OCT-NOV—Invitational Computer Confs, King of Prussia, Pa; Vienna, Va; Houston, Tex; and Dallas, Tex; various dates. INFORMATION: B. J. Johnson & Assocs, Inc, 3151 Airway Ave, Suite C-2, Costa Mesa, CA 92626. Tel: 714/957-0171

NOV 1-3—Federal Office Automation Conf, Washington Convention Ctr, Washington, DC. INFORMATION: Nat'l Council for Education on Information Strategies, PO Box N, Wayland, MA 01778. Tel: 617/358-5356; 800/343-6944 (outside Mass)

NOV 5-6—San Diego Computer Fair, Scottish Rite Ctr, San Diego, Calif. INFORMATION: Barbara E. Sack, San Diego Computer Society, PO Box 81537, San Diego, CA 92138. Tel: 619/565-8720

NOV 7-11—IECON (IEEE Conf on Industrial Applications of Mini and Microcomputers), Hyatt Regency, San Francisco, Calif. INFORMATION: Patrick P. Fasang, Siemens Corp, 105 College Rd E, Princeton, NJ 08540. Tel: 609/452-7070

NOV 8-11—Mini/Micro-West, Brooks Hall, San Francisco, Calif. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

NOV 8-11—Magnetism and Magnetic Materials Conf, Hilton Hotel, Pittsburgh, Pa. INFORMATION: R. W. Cochrane, Dept of Physics, Univ of Montreal, Montreal, Quebec, Canada. Tel: 514/343-7423

NOV 8-11—Wescon, Moscone Ctr and Civic Auditorium, San Francisco, Calif. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

NOV 14-16—Connectors and Interconnections Technology Symposium, Franklin Plaza Hotel, Philadelphia, Pa. INFORMATION: Electronic Connector Study Group, Inc, PO Box 167, Fort Washington, PA 19034. Tel: 215/279-7084

NOV 14-17—Autofact 5 Conf and Expo, Cobo Hall, Detroit, Mich. INFORMATION: CASA/SME Public Relations, PO Box 930, Dearborn, MI 48128. Tel: 313/271-0777

NOV 17-19—Northeast Computer Show and Software Exposition, Hynes Auditorium, Boston, Mass. INFORMATION: Northeast Expositions, Inc, 822 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000; 800/841-7000 (outside Mass)

NOV 28-DEC 2—Comdex/Fall, Las Vegas Convention Center, Las Vegas, Nev. INFORMATION: The Interface Group, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600

DEC 5-6—Internat'l Electron Devices Meeting, Washington, DC. INFORMATION: Melissa Widerkehr, Courtesy Assocs, 1629 K St NW, Washington, DC, 20006. Tel: 202/296-8100

DEC 7-9—Realtime Systems Symposium, Crystal City Marriott, Arlington, Va. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

DEC 12-14—Computer Networking Symposium, Sheraton Hotel, Silver Spring, Md. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

DEC 15-17—Internat'l Conf on Information Systems, Houston, Tex. INFORMATION: Maryam Alavi, Mgmt Dept, Univ of Houston, Houston, TX 77004. Tel: 713/749-3727

WORKSHOPS

OCT 5-6—Getting the Most from Your CAD/CAM System, Civic Center Campus, Milwaukee, Wis. INFORMATION: John M. Leaman, Dept of Engineering and Applied Science, Univ of Wisconsin-Extension, 929 N Sixth St, Milwaukee, WI 53203. Tel: 414/224-4819

OCT 24-25 AND NOV 28-29—CAE, CAD, CAM, and Computer Graphics for Better Design, San Francisco, Calif, and Boston, Mass (respectively). INFORMATION: American Management Associations, PO Box 319, Saranac Lake, NY 12983. Tel: 212/586-8100

DEC 6-8—Software Maintenance Workshop, Naval Postgraduate School, Monterey, Calif. INFORMATION: Janice Thill, Code 54Ss Naval Postgraduate School, Monterey, CA 93940. Tel: 408/646-3212

Announcements intended for publication in this department of *Computer Design* must be received at least three months prior to the date of the event. To ensure proper timely coverage of major events, material should be received six months in advance. Programs and dates are subject to last minute changes.

This space contributed as a public service.

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Interconnection components
Product guide covers pin and socket connectors, solderless terminals, PCB interconnection systems, 0.050" center ribbon cable connectors, insulation displacement products, planar cable, and application tooling. **Molex, Inc,** Lisle, Ill.
Circle 410

Self-contained power supplies
Data sheet details applications and specs of the Series 30/31 Flatpak models, and explains their modular packaging technology. **Tempo Instrument, Inc,** Commack, NY.
Circle 411

Test equipment
Short form catalog uses photographs and specs to highlight major general purpose devices: digital and analog multimeters, oscilloscopes, frequency counters, audio and rf generators, power line monitors, isolation transformers, and dc power supplies. **VIZ Manufacturing Co,** Philadelphia, Pa.
Circle 412

Power MOSFET applications
Book gives design information for 200 p- and N-channel HEXFETS®, covering control, switching recommendations, amplifier circuits, and power usage. **International Rectifier Corp,** El Segundo, Calif.
Circle 413

Disk drive elements
Foldout reviews applications for proprietary components that lower cost and improve performance of disk drive units. **Rogers Corp,** Rogers, Conn.
Circle 414

Flat-panel display terminal
Data sheet lists functional, environmental, and physical specs of the 2500 Alphagraphic Plasmascope, and discusses significant capabilities and military program applications. **SAI Technology Co,** San Diego, Calif.
Circle 415

Membrane switch
Catalog summarizes construction and design features of the Electropanel, with some focus on tactile location and graphic capability. **Hallmark Electropanel Co,** Farmingdale, NY.
Circle 416

Data communications news
Covering data communications and related computer applications, *The Communicator* also introduces new products and reference books. **Black Box Catalog,** Pittsburgh, Pa.
Circle 417

Floppy drives
Brochure outlines recent advances in floppy technology, including form factor and electrical interface compatibility, high density recording, and closed and open loop servos. **Amlyn Corp,** San Jose, Calif.
Circle 418

User configurable card
Data sheet describes DMS531 Multibus compatible data acquisition and control interface cards, and includes encapsulated descriptions of the DMS200 series modules. **DI-AN Micro Systems,** Stockport, Cheshire SK4 3EA, England.
Circle 419

Circuit reliability
Report discusses reliability programs for linear circuits, covering device and package reliability monitor programs, data analysis, temperature accelerated life testing programs, and failure mechanism with failure rate calculations. **Precision Monolithics, Inc,** Santa Clara, Calif.
Circle 420

Sonic digitizer
Bulletin describes GP-6-3D-P 3-D digitizer and offers capsule specs for the complete system, its control unit, and an optional multiplexer. **Science Accessories Corp,** Southport, Conn.
Circle 421

General purpose switches
Catalog with spec charts, dimensional drawings, and photographs illustrates toggle, foot, heavy duty, contact, push button, illuminated, miniature, and keylock switches, as well as fuse holders. **MG Electronics,** Hauppauge, NY.
Circle 422

Cable guide
Booklet offers conversion factors, general design equations, cable designs, material technical data, decimal equivalents, and a wire and cable glossary. **k-x Cable, Inc,** Pine Brook, NJ.
Circle 423

Hardware and technology for emc
Catalog gives electrical and mechanical characteristics for shielding kits, hardware, and PCB mounted filters, along with shielded and filtered connectors; lists of shielded HD-20 and military D-type plugs/receptacles accompany specs for full-metal and metallized plastic hardware. **AMP, Inc,** Harrisburg, Pa.
Circle 424

Software facility courses
Digest of educational services supplies information, schedules, and tables covering personal computer, office automation, word processor, hardware, maintenance, VAX/VMS, RSX-11M, RSTS/E, RT-11, TOPS 10/20, IAS, COS-310, OSM-11, PDP-8, network, and audiovisual training programs. **Digital Equipment Corp,** Bedford, Mass. **Circle 425**

Signal measurement and test
Reference folder features scalar analyzer 6500 and modulation meter 2305, along with synthesized generator models 2017, 2018, and 2019. **Marconi Instruments,** Northvale, NJ. **Circle 426**

Packaged switches
Catalog offers photos, pin pattern drawings, and features table, in addition to spec and application diagrams for each switch. **Ledex, Inc,** Vandalia, Ohio.
Circle 427

Intelligent modem
Data sheet explores the series 14,400, presenting full component specs and diagram-supported applications. **Timeplex, Inc,** Woodcliff Lake, NJ.
Circle 428

Federal regulation 15J
Question-and-answer brochure examines the ramifications of FCC regulations that will go into effect on Oct 1, 1983, discussing interference specs and rf standards. **The Keenan Corp,** Vienna, Va.
Circle 429

High performance microcomputers
Brochure details expanded line of 4 fast-loading models, and contains UCSD p-System and operating system information. **Sage Computer Technology Co,** Reno, Nev. **Circle 430**

Communications processors
Brochure summarizes characteristics and properties of the 3600 line. **NCR Comten, Inc,** St Paul, Minn. **Circle 431**

Stat MUX
Data sheet specifies the DP-1000 and describes how it multiplexes 8 asynchronous terminals to 1 phone line. **Dynapac,** Alexandria, Va.
Circle 432

Time division LSI MUX
Brochure provides illustrations and applications of the TDM 1223. **General DataComm Industries, Inc,** Danbury, Conn. **Circle 433**

Data acquisition
Data book presents the system 620 line, related software, and computer interfaces, including analog multiplexers, signal conditioners, and I/O systems. **Neff Instrument Corp,** Monrovia, Calif.
Circle 434

Electromagnetic brakes
Folder of parts drawings and mechanical/electrical specs for fail-safe and disk brakes includes a glossary of terms and general selection information. **Regdon Corp,** Brookfield, Ill.
Circle 435

Single-board computer
Release specifies 6502 microprocessor performance, detailing STD-bus applications. **Designatronics, Inc,** New Hyde Park, NY. **Circle 436**

Subminiature indicators
Catalog details features of incandescent and neon indicator lights, providing photos, line drawings, and dimensional information; mil-type designation index is included. **Dialight,** Brooklyn, NY.
Circle 437

Video display terminals
Data sheets describe ergonomically engineered ADM 11 and ADM 24E terminals. **Lear Siegler, Inc, Data Products Div,** Anaheim, Calif.
Circle 438

Controllers for DEC systems
Product specs of communication multiplexers and disk/tape controllers are accompanied by general and technical service information. **Emulex Corp,** Costa Mesa, Calif.
Circle 439

Heat sinks and accessories
Catalog contains graphs, diagrams, photos, and specs, covering a range of snug-fit, plug-in, end-grease, slide-on, and wave-soldered equipment. **Aavid Engineering, Inc,** Laconia, NH.
Circle 440

Image analyzer
Brochure supplies Quantimet 900 system I/O logic diagrams, hardware/software specs, and display monitor photos. **Cambridge Instruments, Inc,** Monsey, NY.
Circle 441

Power conversion
Photos accompany tabulated specs with case, pin, and socket configurations for modular switching supplies, plug-in power adapters, and encapsulated mounts for single-, dual-, and triple-output modules. **Datel-Intersil,** Mansfield, Mass.
Circle 442

Automation system
Folder explains the ICC 3200 off-the-shelf solution to automation control projects that require motion control and sequential logic for both dc and ac brushless servo systems. **International Cybernetics Corp,** Pittsburgh, Pa.
Circle 443

A 32-bit board set
Product handbook describes Quadrabyte computer components, and supplements product groupings with configuration charts. **Gould Inc, Computer Systems Div,** Plantation, Fla.
Circle 444

Keyboards, arrays, and keyswitches
Footprint and mounting details of the KS-200E ergonomic keyboard, ancillary arrays, and discrete keyswitches are profiled in bulletin that includes specs for both low and ultralow keycaps. **Stackpole Components Co,** Raleigh, NC.
Circle 445

Rotary switches
Brochure lists electrical ratings and illustrates materials and finishes of standard and PC mountable 0.5″ diameter switches. **Grayhill, Inc,** La Grange, Ill.
Circle 446

Connector systems
Catalog covers line of 0.050″ insulation displacement connector sockets, mating headers, DIP and DIN 41612 connectors, plugs, and accessories, and introduces Nanoflex 0.025″ connector systems. **Nanocon, Inc,** Chatsworth, Calif.
Circle 447

Digital bipolar IC
Brochure introduces the H3000 LSTTL/CML gate array, a semicustom VLSI circuit. **Honeywell Inc,** Minneapolis, Minn.
Circle 448

Optoelectronics
Guide summarizes features, packaging, and dimensions of fiber optic emitters and detectors, infrared emitting diodes, silicon photodetectors, slotted couplers, and optocoupler/isolators. **Motorola Semiconductor Products, Inc,** Phoenix, Ariz. **Circle 449**

Relays
Digest offers specs, applications, and contact selections of miniature, general purpose, mercury-wetted, power, solid state, latching, and time-delay relays. **Midland-Ross Corp,** North Mankato, Minn. **Circle 450**

Linear motion products
Guide to standard ball bearing and roller ball bearing systems describes functions and applications. **Thomson Industries, Inc,** Manhasset, NY.
Circle 451

Contrast enhancement
Technical bulletin illustrates, tabulates, and specifies features and applications of Chromafilter® sheet materials for energy emitting displays. **Panelgraphic Corp,** West Caldwell, NJ.
Circle 452

Sensor and control technology
Booklet describes unique applications, including nuclear reactor inspection and high power switching. **Westinghouse Electric Corp,** Pittsburgh, Pa.
Circle 453

Data concentrator families
Text and diagrams overview the effectiveness of Data Xchange, Data Express, Economux, and Bi-Link with information systems in which terminals are remotely located. **Compre Comm, Inc,** Champaign, Ill. **Circle 454**

Data communication products
Catalog features specs for the "Tri-State Box" modem and terminal interface pocket analyzer, and covers switches, printers, computer ports, modems, multiplexers, concentrators, and front-end processors. **Electro Standards Laboratory, Inc,** Providence, RI.
Circle 455

Precision resistors
Data book furnishes outline drawings, schematics, and performance characteristic tables for the Micronox® and Tetrinox® resistance film technologies, as well as for precision instrumentation resistor networks. **Caddock Electronics,** Riverside, Calif. **Circle 456**

Designer's Bookcase

PRACTICAL COMPUTER COST ACCOUNTING
By *Kenneth M. Sullivan*

Keep computer costs as low as possible! Ken Sullivan explains how to maximize the return on your hardware investment by measuring and costing all services performed on your computer system. He shows you how to set up cost accounting systems for centralized, decentralized, and distributed processing systems and how to use accounting data for managing computer costs.
$24.95 **Circle 473**

USING THE RADIO SHACK TRS-80 IN YOUR HOME
By *Kenniston W. Lord, Jr.*

Get the most out of your versatile TRS-80 and turn it into the ultimate home management and entertainment machine. Ken Lord provides step-by-step instruction for using the computer as a tutor, personal finance manager, and time- and work-saver. He describes every aspect of programming the computer and includes numerous sample programs.
$23.50 **Circle 474**

IMS PROGRAMMING TECHNIQUES
A Guide to Using DL/1
By *Dan Kapp and Joseph F. Leben*

Find out how to write effective programs for the IMS family of data base management systems supplied by IBM. This comprehensive guide explains IMS and how application programs interface with it. You discover how to achieve system objectives, load a data base, use command codes, and retrieve, send, and store data.
$17.95 **Circle 457**

CDP REVIEW MANUAL
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By *Kenniston W. Lord, Jr., and James B. Steiner*

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SYSTEMS DEVELOPMENT DOCUMENTATION: Forms method
By *Technical Communications Associates, Inc.*

This 430 page publication presents a series of simple procedures for preparing documentation that evolve around the use of pre-structured forms that record the results of the task performed during the system development cycle. The forms cover a wide range of system development functions and are formatted to present all types of documentation. Also suggested in this publication are standards for documentation preparation.
$69.50 **Circle 459**

A GUIDE TO PROGRAMMING IN BASIC PLUS, Fourth Edition
By *Bruce Presley*

Extensively revised and updated, this fourth edition shows how to write easy-to-read programs for Digital Equipment Corporation computers that run BASIC PLUS. It demonstrates the latest techniques in computer game programming, mathematics, files, recursion, searching, and sorting. An easy-access format helps you locate single definitions and commands rapidly, and each new topic is accompanied by review exercises.
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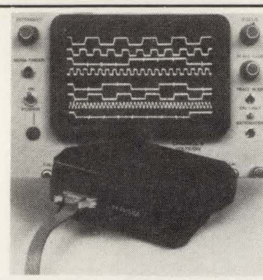

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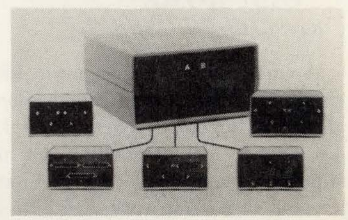

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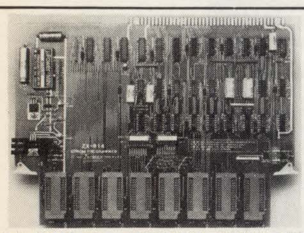

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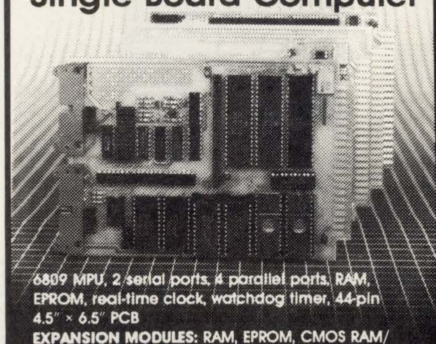
6809
Single Board Computer



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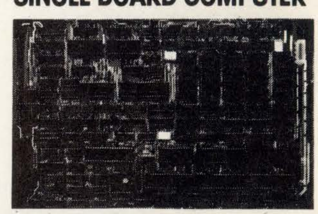

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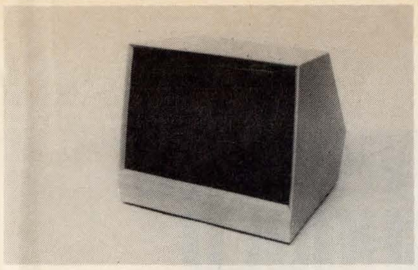

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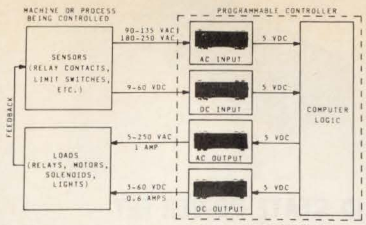

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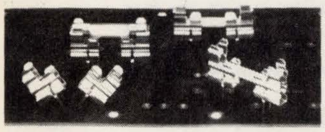

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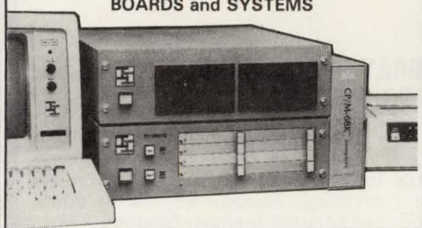

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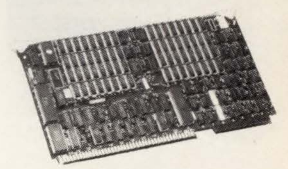

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