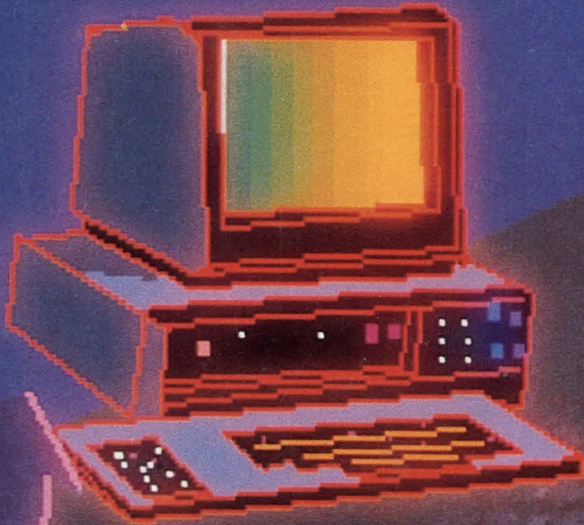


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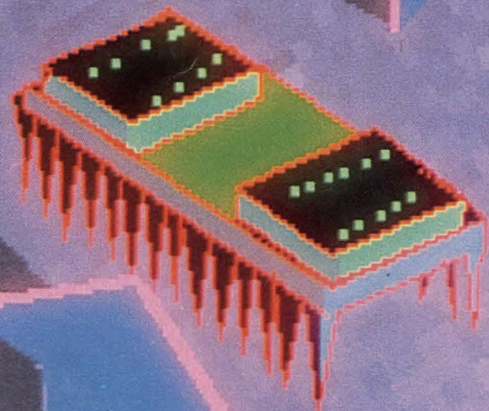
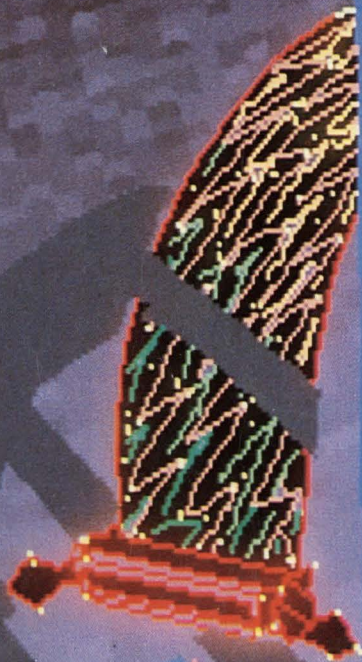
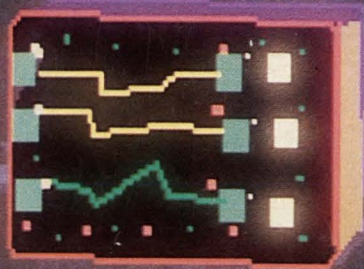
DECEMBER 1983

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS



**SPECIAL REPORT:
SYSTEM COMPONENTS '83**



from out of the West...

TAPE DIMENSION III

DEC COMPATIBLE CONTROLLERS

Tape Dimension III is the only buffered tri-density (GCR/PE/NRZI) TS-II™-emulating controller on the market. The combination of its unique asynchronous handshake design and 64K byte buffer enables it to take full advantage of bus speeds without the risk of causing data late conditions in other bus transfer operations. It makes Tape Dimension III particularly adaptable to systems with high speed disk drives.

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CIRCLE 1

2X the speed, 3X the density, 4X the capacity, 1/3 the cost.

The first low cost GCR Tri-Density Tape System offering large system performance.

Kennedy is, and has always been, the leader in peripheral tape technology. With Model 9400, Kennedy has done it again. For instance:

2X the speed. Model 9400 is a dual speed transport, operating at 45 ips in the GCR mode and 75 ips in the PE/NRZI modes with a maximum rewind speed of 500 ips.

3X the density. The drive utilizes Group Coded Recording at 6250 BPI along with previous industry standard densities of 1600 BPI/PE recording and 800 BPI/NRZI recording.

4X the capacity. In GCR mode, the Model 9400 can store up to 180M BYTES of data (four times more capacity than the traditional 1600 BPI drive).

More? The Model 9400 features multiple processors to separate data handling and control functions. An 8088

processor provides overall system control and accommodates a variety of industry standard interfaces.

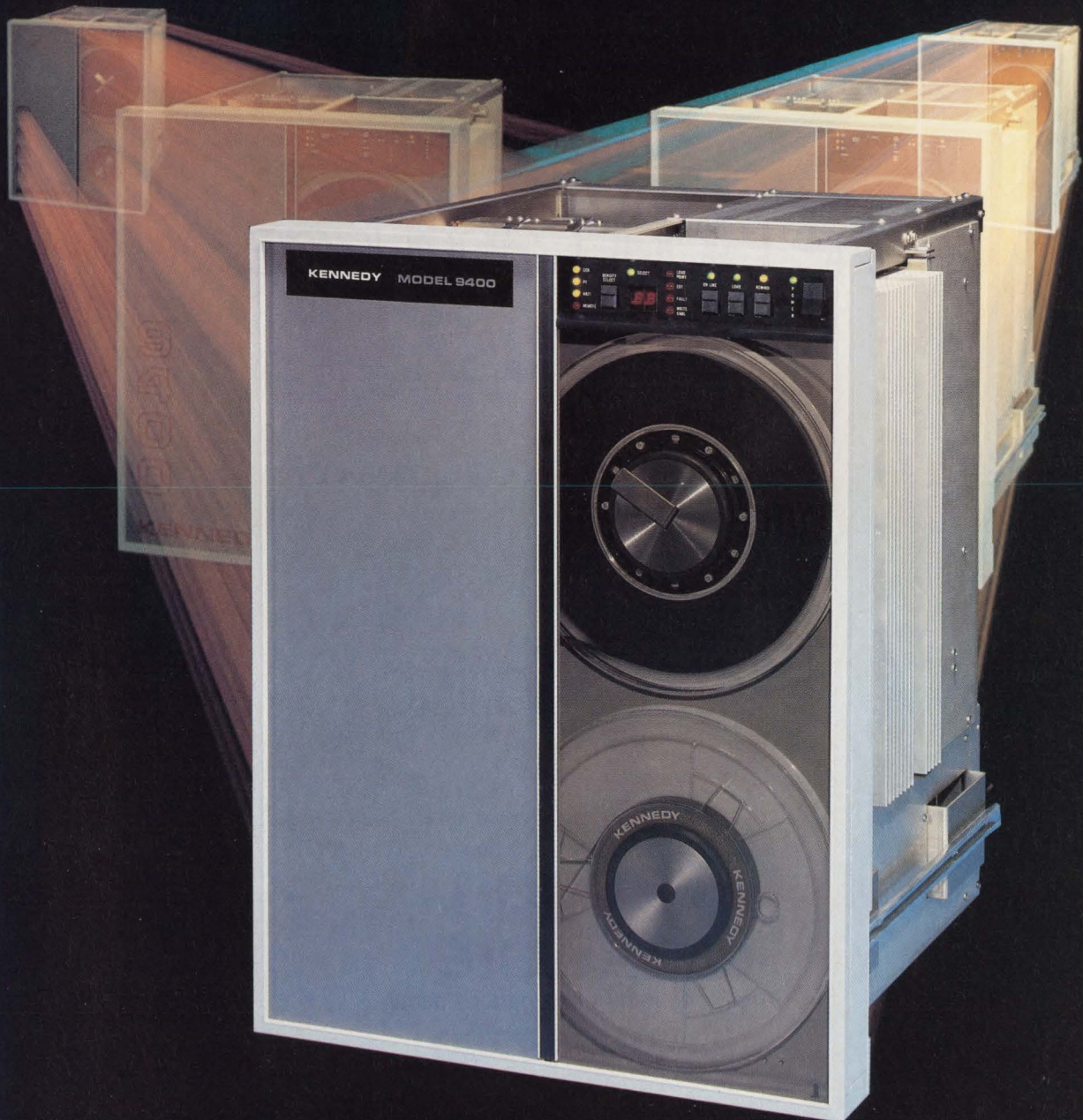
Among the many features of the 9400 is its RS-232 communication port and complete internal software which permits off-line diagnostic operations via a terminal, the host computer or by a remote test facility with a phone modem.

1/3 the cost. Best of all, the Model 9400 is priced at about 1/3 the cost of a conventional GCR tape system. Kennedy Company . . . designers of the finest peripheral tape products for 20 years.

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UP FRONT

A 32-bit supermini is first to use 256-Kbit DRAMs

Small size and high performance are combined in Data General's new Eclipse MV/8000 C superminicomputer. A 4-Mbyte version uses 256-Kbit DRAMs, claimed to be a first for 32-bit superminis; a 1-Mbyte model uses 64-Kbit devices. For both, a 16-Mbyte system cache uses custom arrays with more than 2000 gates. This supermini fits into a 10.5-in. high chassis and can be mounted in a 19-in. wide rack; yet it can execute 1.2 MIPS and can support 5.6 Gbytes of mass storage.

Designed in a cooperative effort between engineering teams in Westboro, Mass and Nippon Data General in Japan, the MV/8000 C was announced at Autofact 5 in Detroit—because of its match to many industrial automation operations, one of three Data General targets for the future. (The other two are office automation and personal automation.) Its high computational speed fits the requirements for CAD workstations, continuous process monitor and control systems, high speed data acquisition, and distributed system networks. At the same time, Data General announced the Array Plus 2000 array processor for imaging, modeling, simulation, and other applications that require very rapid computation of large data blocks.

Ten-MIPS transputers support Occam

Designed for multiprocessing applications, a family of 16- and 32-bit microprocessors has been introduced by Inmos Corp (Bristol U.K. and Colorado Springs, Colo). Both the IMST424 (32 bits) and T222 (16 bits), dubbed transputers, contain a 10-MIPS processor, 4 Kbytes of 50-ns RAM, an 8-bit peripheral interface, and four 1.5-Mbyte/s full-duplex links. In addition, the T424 has a 32-bit, 26-Mbyte/s memory interface while the 16-bit chip offers 17 Mbytes/s. The 32-bit transputer is made with a 2-micron CMOS process to pack in 250,000 devices. A multiplexed memory interface on the 32-bit chip ties the processor to offchip mixed memory that is directly addressable to 4 Gbytes. A simple RISC-like instruction set speeds code execution. The architecture was specifically designed to support Occam, a concurrent programming language, although sequential programming languages such as Pascal and Fortran also run efficiently.

Digital ac servomotor-controlled robot improves velocity control

Called the "affordable electric robot," the IRI M50-E digital ac servo robot is controlled by digital signals generated by a proprietary monoboard containing eight microprocessors. According to International Robotation/Intelligence (Carlsbad, Calif), digital ac servo power provides improvements over dc servomotors in robot motion velocity for more accurate path control. In addition, the electric robot will provide more graceful realtime control than the company's air servo-powered robot.

Workstation expands CAE capabilities

The prototype of an "ergonomic workstation" with high performance graphics that will be added to its ICEM (integrated computer aided engineering and manufacturing) line was shown by Control Data in its Autofact 5 booth. Expected to start at about \$30,000 at the lowest capability level, the workstation will have a 1024- x 1280-, 60-Hz, noninterlaced color display; separate alphanumeric display; 200,000-vector transform rate; three-dimensional display file; and 512 Kbytes to 2 Mbytes of RAM.

Logic simulator offers simultaneous modeling and testing

A fully interactive, multiple-level, mixed mode logic simulator introduced by Prime Computer (Natick, Mass) enables engineers to model, verify, and analyze the logical operation of digital electronics systems before they become actual physical design. Themis is also said to be the first system of its kind to offer simultaneous modeling and testing at the switch, gate, functional, or language level. Users can interrupt and restart a simulation as necessary to spot errors and make changes without rerunning the entire simulation.

Development tool provides graphic device independence

Incorporating the international Graphical Kernel System, NOVA*GKS, a graphics application development tool, provides for device independence and portability over hardware. In the package, Nova Graphics International Corp (Austin, Tex) has used a multilayer architecture consisting of a GKS interface, workstation manager (with picture storage independent of the graphics device) and workstation supervisors that each handle a specific graphics device.

Fortran-77 compiler promises software portability

A language development technology that promises to protect software investments cuts the time necessary to port languages and applications from one microprocessor to another. Digital Research Inc (Pacific Grove, Calif) has based the design of a Fortran-77 compiler on this technology. The design uses standard language processors coupled to common code generators and runtimes. First in a family of five, the compiler produces 8086 native machine code and runs on Concurrent CP/M and CP/M-86 operating systems. The language meets full ANSI specifications. It also supports overlays, handles arrays as large as 65,536 elements, and runs programs as large as 1 Mbyte.

Gate array eliminates channels

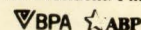
By using dual layer metal and a "sea of gates" geometry, California Devices (San Jose, Calif) eliminated internal wiring channels from its high speed CMOS gate array. The resulting family of 220 to 10,000 gate arrays will rival custom and standard cell designs in size, performance, and cost. The first product will be a 990-gate array built with 3-micron technology. Typical gate speeds will be 2.5 ns. The new technique eliminates wide avenues of silicon interconnecting cells. This provides a larger ratio of active area to interconnect area for reduced die size. Outputs will drive a 150-pF bus in 15 ns at 35 MHz.

Workstations compete with superminis

Supermini class systems in computational intensive applications may receive a run for their money from the DN460 and DN660 workstations introduced by Apollo Computer (Chelmsford, Mass). Rivaling VAX performance at a lower cost, the computational nodes handle IEEE format single and double precision numbers using an integrated hardware floating point processor.

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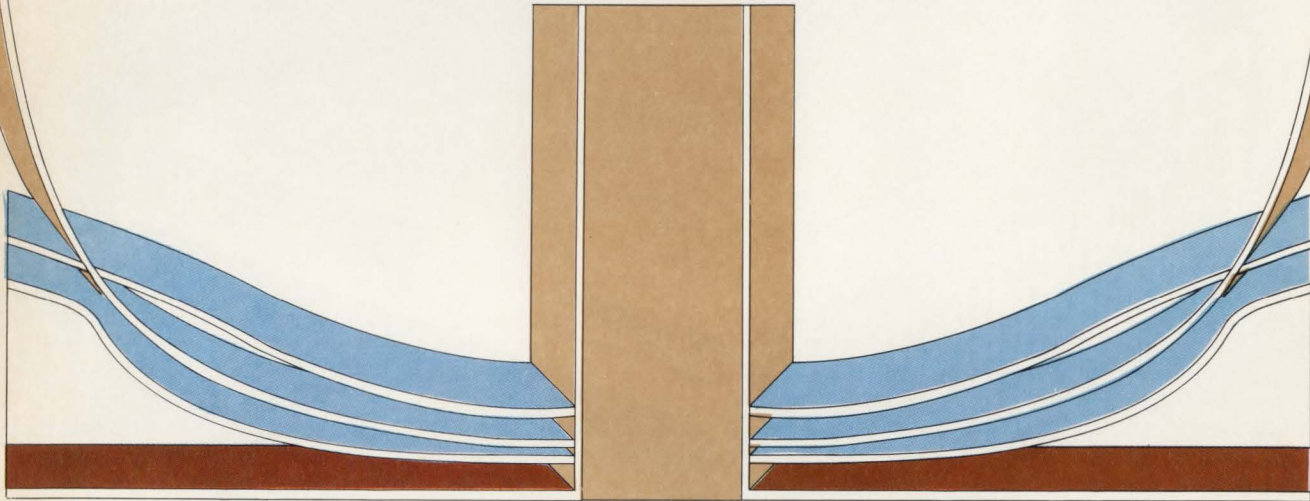
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CIRCLE 4

COMPUTER DESIGN[®]

System technology

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System design

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by David W. Gulley—Differing architectures of 64-Kbit dynamic RAMs permit designers to optimize the design of memory systems.
- 89 **Software: Graphics software standards promote device independence**
by Paul Caron, John Gray, and Harold Schofield—Proposed standards permit software development independent of specific graphics hardware as in this example of printer control.
- 109 **Software: Language-based architecture eases system design-II**
by Pete Wilson—Unlike other high level languages, Occam is targeted specifically at distributed architectures.

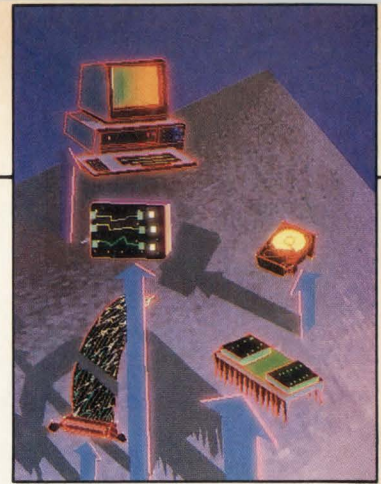
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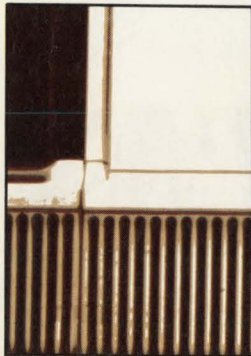
Special report: system components '83

129 This summary of the most significant product introductions of 1983 shows a year of progress from personal computers to superminis. Disk drives increased storage and speech while shrinking in size, and optical disks offered gigabytes of storage. Nonimpact printers using new technologies entered the market, while dot-matrix printers improved print quality. Increasing function density contributed to integrated circuit progress as entire systems appeared on chips. Design, test, and development techniques began to converge as logic analyzers were interfaced directly to development systems. Reasonably priced computer aided workstations appeared. Finally, new packaging, interconnection, and power supply techniques evolved to help make other advances possible.

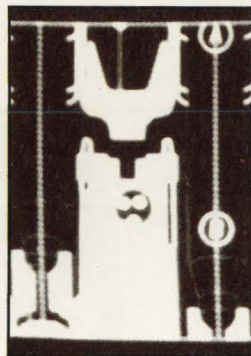
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- 169 Peripherals**
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- 201 Test & development**
- 213 Power sources & interconnection**



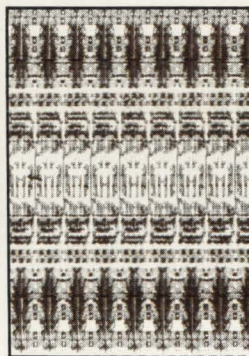
This month's cover was created and designed by Mark Lindquist on the Digital Effects Video Palette III and D-48 high resolution camera system.



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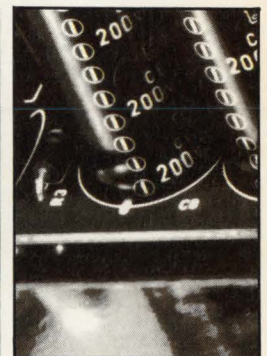
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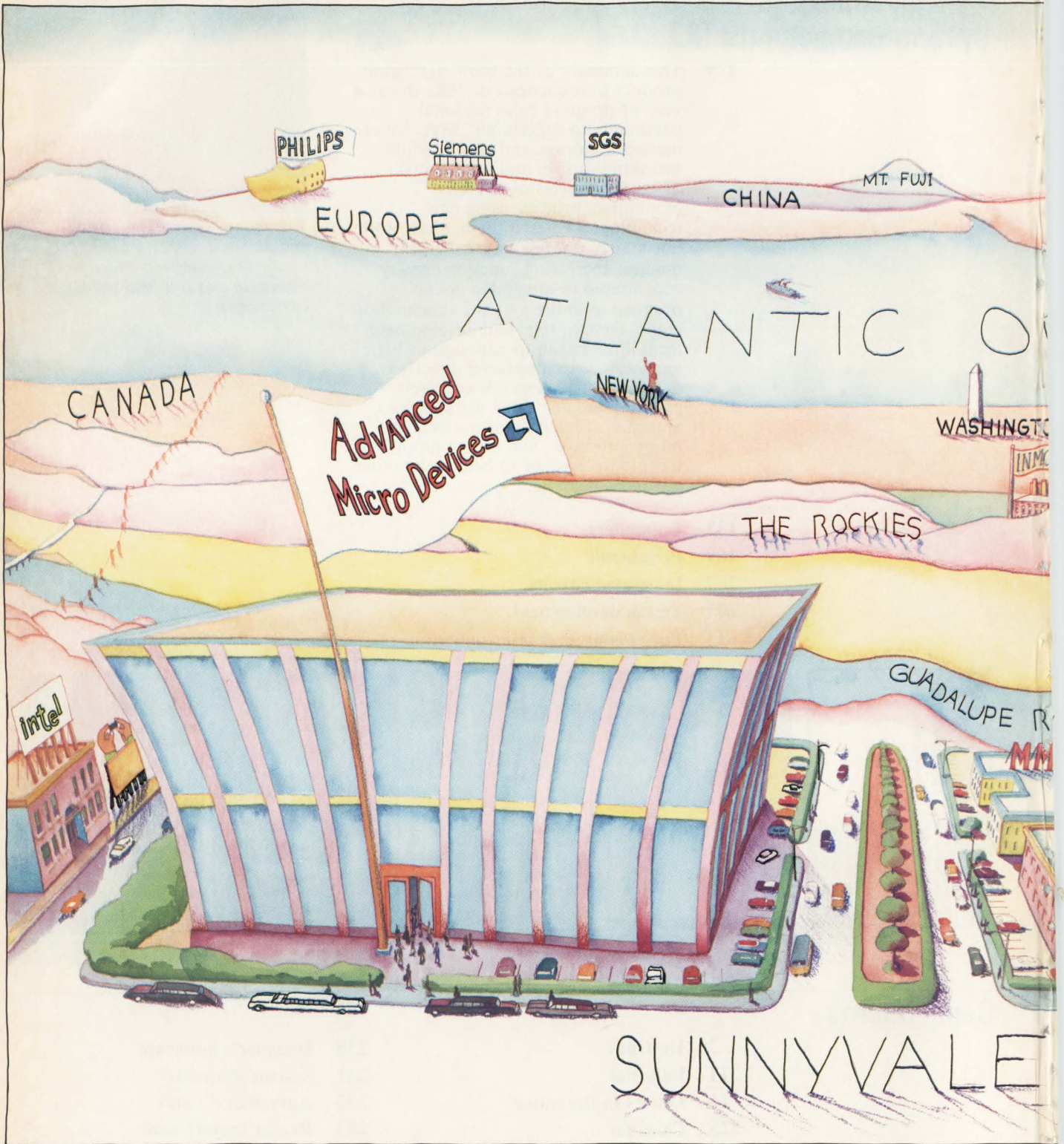
Designers' preference survey*

- 235 Components, assemblies & power supplies**

*Appearing in Domestic issues only

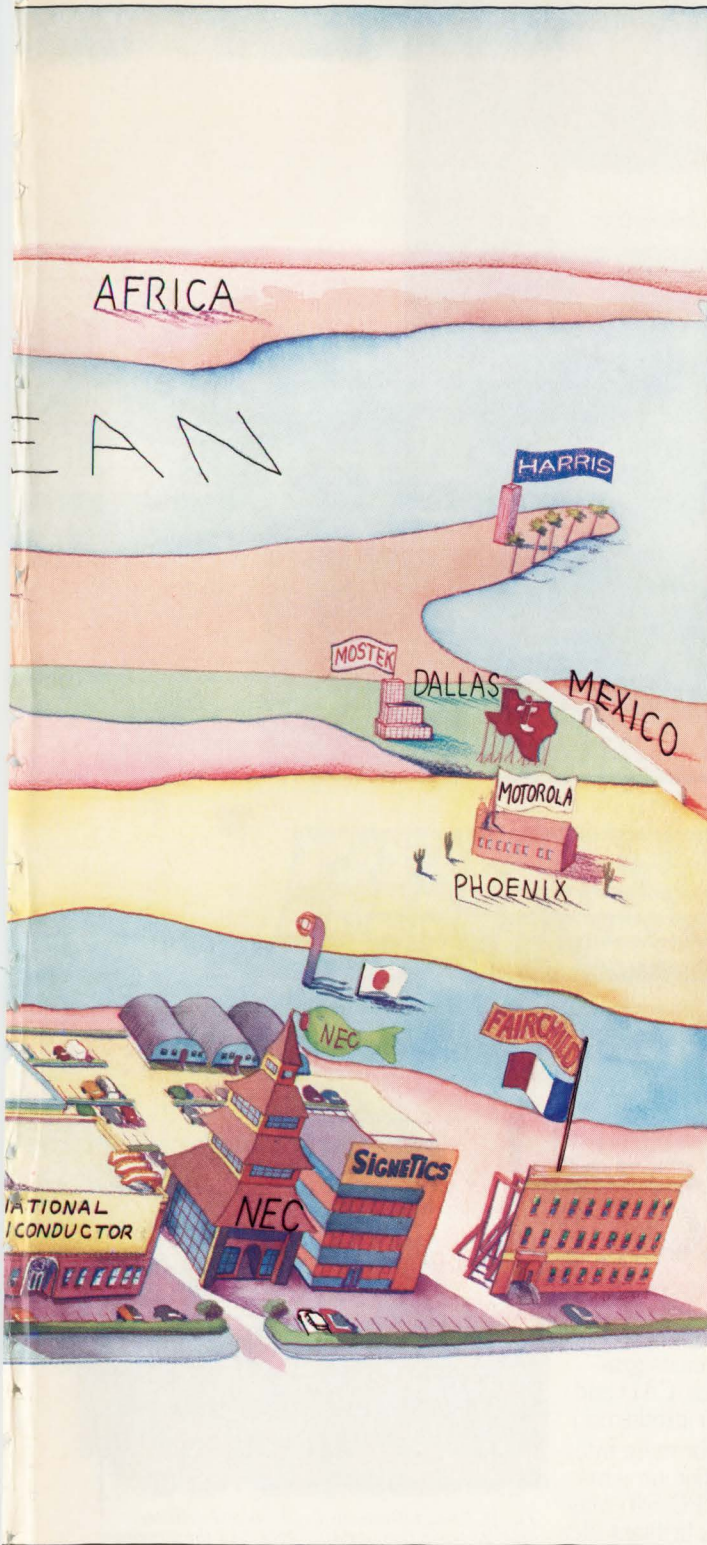
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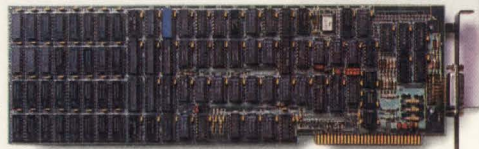
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CHOOSING THE MVP

As year-end approaches, achievement awards activity rises to a crescendo. There are all the college football games with their associated "most valuable player" awards, and the hoopla over who is really "number one." Just about every magazine, newspaper, and TV station publishes lists of achievement awards. Depending on which magazines you read, you can get lists of just about everything from the best dressed men and women to the best golf courses and ski resorts.

Computer Design also contributes its own specialized lists. In this issue, for example, we selected the year's most significant new products and have identified the key technology trends. And, *Computer Design's* editors have recently been involved as both judges and contenders, thus devoting a lot of time to the business of achievement awards. Besides helping to plan this System Components '83 issue, I was on the panel of five judges who selected the "Top Five New Products" exhibited at this year's Mini/Micro West convention in San Francisco. Meanwhile, *Computer Design's* editors have been busy selecting entries for magazine achievement awards run by such organizations as the American Business Press, the American Society of Business Press Editors, and the Society for Technical Communications.

Perhaps we should be careful, however, not to become obsessed with achievement awards. Because the rewards in terms of status and compensation are so high for individual award winners, there is the temptation to set one's goals toward winning an award at the expense of an organization's primary activity—whether it be winning football games, publishing an informative magazine, or making profitable computer products. Also, because of the high stakes involved, there are inevitable questions about the objectivity, accuracy, and fairness of the judging process.

The most common problems, however, are not so much the quality or integrity of the judges, but the nature of the contest, the vast dissimilarities among contestants, and the incompatible ground rules for judging. Judges are frequently confronted with the task of choosing between, for instance, a quarterback and an offensive tackle; or, in our industry, between a realtime operating system and a switching power supply. Given choices like these, and all else being equal, glamour and human interest usually prevail over the less exciting contribution. Yet, the results then seem unfair because a quarterback cannot function without the other players on the team, and an operating system cannot run unless the computer system has a reliable and stable power source.

One solution to these problems is to divide contestants into categories and choose the best in each one. Then, for example, the most significant power supplies are not crowded out by exciting software products. Similarly, the existence of specialized magazine contests has allowed *Computer Design's* editors to win awards among technical magazines with material that would have been crowded out in a broader contest. Last year, we won several awards from the Society for Technical Communications, but none from the broader-based American Business Press.

Despite their limitations, however, individual achievement awards do reward and thus encourage excellence by providing peer recognition. The danger comes when we start to take them so seriously that we bend the rules, hurt other members on our own team, or quit to avoid losing. Frankly, I am not sure how we avoid getting so competitive that it becomes damaging. Please tell me what you think.

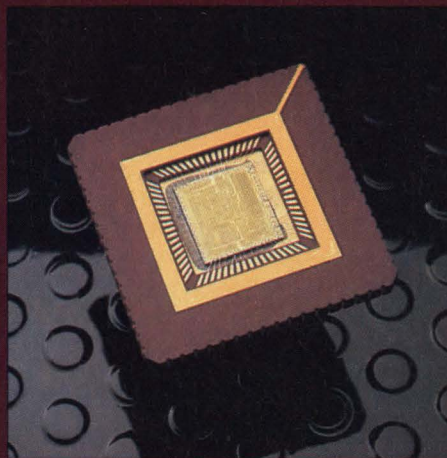


A handwritten signature in black ink that reads "Michael Elphick". The signature is written in a cursive, slightly slanted style.

Michael Elphick
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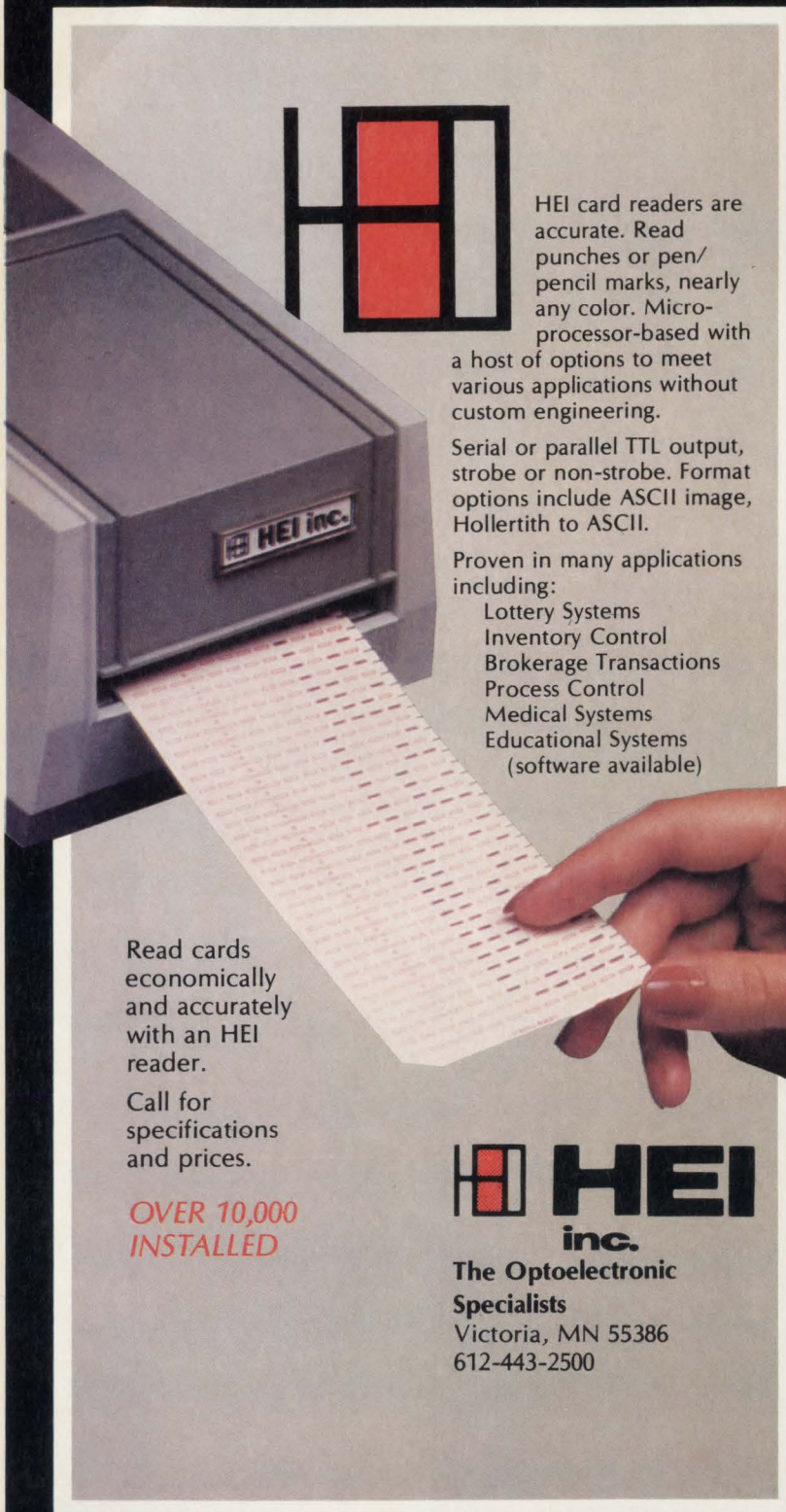
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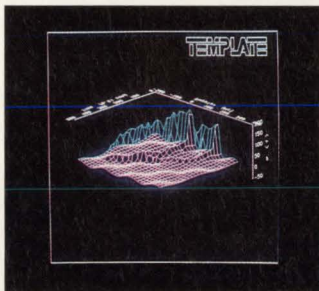
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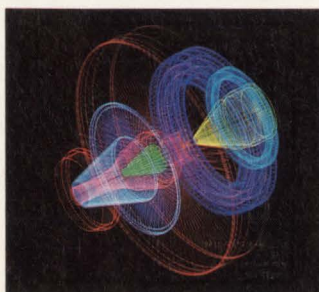
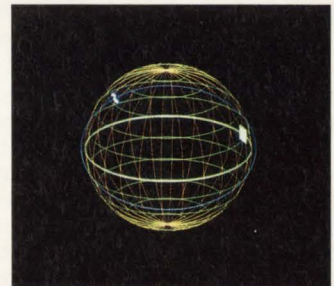
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Microprocessor facts and fancy

Being a microprocessor system designer, I appreciated the Special Report (Oct 1983) on Microprocessors/Microcomputers. However, there are a few pieces of misinformation in the article, "Microprocessors: Speed Up, Price Down, and CMOS Everywhere," that I would like to clear up.

In the panel "The designer's perspective" (third paragraph, p 179), Mr Peddle comments that the Z80 has a multiplexed address/data bus. This is untrue. Like the 6502, the Z80 has separate address and data lines. Other 8-bit processors, such as the Intel 8085 and the National Semiconductor NSC800, do have multiplexed buses, but there is still much controversy over the question of degraded performance due to bus multiplexing. The 6502 does do more per clock cycle than a Z80, but this is due to the internal instruction execution method (the use of internal microcode versus combinational logic) rather than multiplexing or anything else.

In the third paragraph (p 182), the author points out that the Intel 186 processor can handle a 4-Mbyte/s bus transfer rate. The actual value is 2 Mbytes/s. Having designed with the 186 processor, I have found it to be very impressive due to its high functional integration. Intel's description of "a board on a chip" seems to be a reasonably accurate way of describing this new-generation processor.

Finally, I wish to comment about the terminology in the statement (p 186), "in National's terminology, coprocessors are called slave processors." In fact, National makes a definite discernment between the terms "coprocessor" and "slave processor." A coprocessor is considered to be a processor that works in parallel with the main processor, and shares the same address and data buses. A slave processor is considered to be a processor that works under the control of a master processor, where the master processor provides the slave with the necessary data, and commands and receives the resulting data from the slave. The Intel 8087 math processor is considered a coprocessor by this definition, while the National 16081 FPU is considered a slave processor.

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Control-O-Mation
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Dexter, MI 48130

Unix versus Lisa

In his article, "Lisa's Alternative Operating System" (Aug 1983), Mr Daniels does the Unix operating system a disservice by lumping it together with other popular

microcomputer operating systems. Many of the revolutionary aspects of Lisa highlighted by Daniels' article have been available in Unix for years.

In particular, Unix supports compatible file, device, and interprocess I/O (ie, pipes). The I/O system is concerned simply with byte streams; the data structure is imposed by programs that use it, not by the system. Unix has the ability to initiate asynchronous processes (ie, the fork system call). The shell command language and its associated interpreter provide Unix with a uniform user interface. The C library includes system calls accessible to application programs enabling a high degree of compatibility to be achieved in the development of Unix application software. The recent ways in which Unix has been enhanced by window management software have been facilitated by its simple yet elegant design.

Lisa does embody many Unix-like ideas, and it is a pity that this fact is not acknowledged by Daniels. Lisa is an impressive attempt to simplify the user interface at the mechanical level by providing support for a pointing device, the mouse. However, the Lisa software in itself appears simplistic rather than simple and elegant when compared to Unix. Considering Daniels' example regarding deletion of a file, I cannot but agree that simple pointing is the easiest method. If, however, the user wishes to delete 50 files, a simple and elegant command language that easily expresses this has the advantage.

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Is Lisa revolutionary?

Unfortunately, I think that Ms Boldyreff's letter is based on a regrettable misunderstanding. She seems to take exception primarily to the section entitled Operating System Calls. In the copy of the article that I sent for publication, the first sentence of this section reads: "Although it is the user interface of the Lisa system that one first notices, it is the fundamental system calls of the Lisa operating system that makes all this possible."

In the article as published, this first sentence has been edited as "Although it is Lisa's user interface that one first notices, the fundamental system calls of the operating system are what make the software revolutionary." This new sentence can be interpreted to mean that it is, in fact, all of the Lisa operating system calls themselves which are revolutionary,

and revolutionary can mean "better than anything else."

I can certainly see where a Unix fan would take immediate exception to such a statement. I never intended to imply that all of our system calls, and the capabilities they represent, are better than those of other operating systems. To the best of my knowledge, a few of our operating system capabilities, such as the graphics capabilities, could perhaps be considered revolutionary. But it is the Lisa user interface itself that is revolutionary and that is the primary subject of this article.

Based on this criterion, I still think that it is reasonable to group Unix together with other popular operating systems. One interacts with such traditional operating systems by using a keyboard to type commands selected from a rigid and precisely defined command language. One interacts with Lisa by using a mouse to point at icons and other symbols on a graphical desktop. I claim that this is a significant qualitative difference and that Unix is much more like MS-DOS, CP/M, etc in this regard and that it is not at all like Lisa.

As to the fundamental capabilities of the underlying operating system calls, I never claimed that the Lisa OS calls were revolutionary or better than those of other operating systems. These underlying Lisa OS capabilities just exist to make the user interface possible. A few of our operating system capabilities, such as the graphics calls, could perhaps be considered revolutionary. But most of the Lisa OS capabilities were based on good ideas from lots of existing operating systems, including Unix, just as some of the important capabilities of the Unix OS mentioned by Ms Boldyreff actually came from previous operating systems such as Multics. She is indeed correct in that I should perhaps have given credit for the underlying Lisa OS capabilities that were derived from such other operating systems. However, such a list would be a long one.

As to her last point, I have never heard anyone describe the Unix command language as simple. Even compared to other traditional operating systems, the Unix command language is widely considered to be cryptic, complex, and difficult to learn. Finally, to delete 50 files using the Lisa user interface, one just points at the folder containing these 50 files and then drops it into the wastebasket icon. It is no more difficult than the deletion of a single file.

Bruce Daniels
Apple Computer Inc
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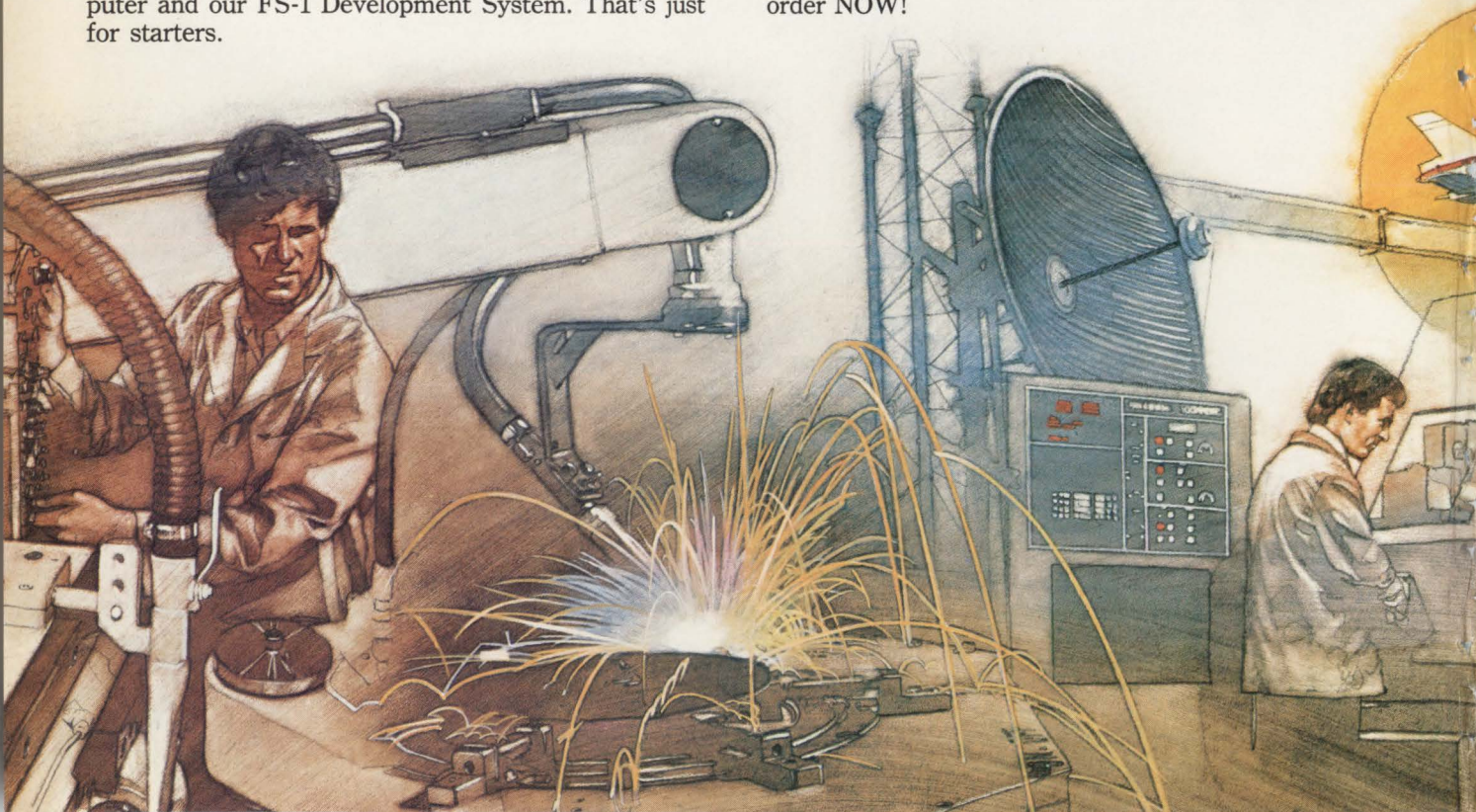
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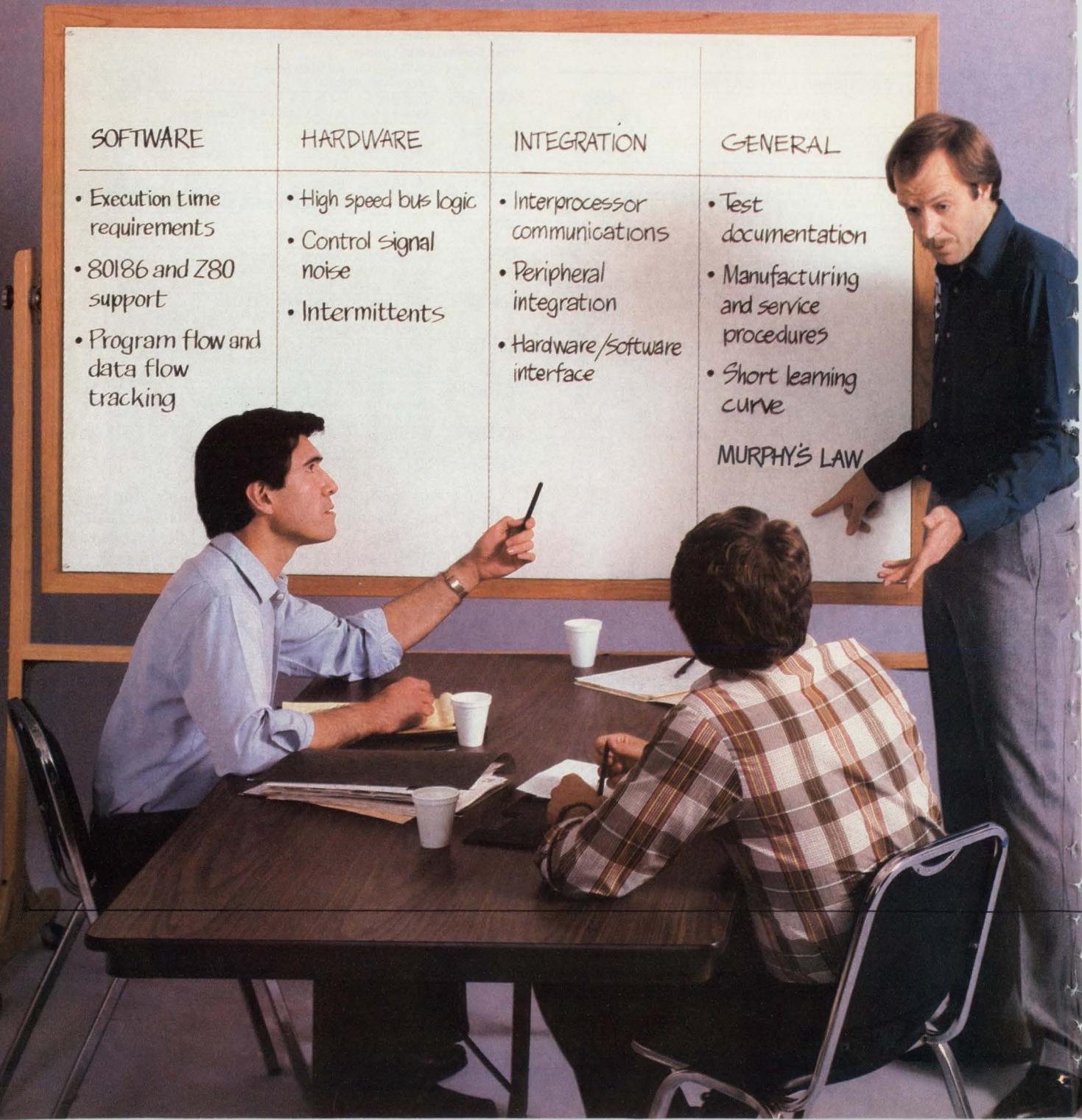
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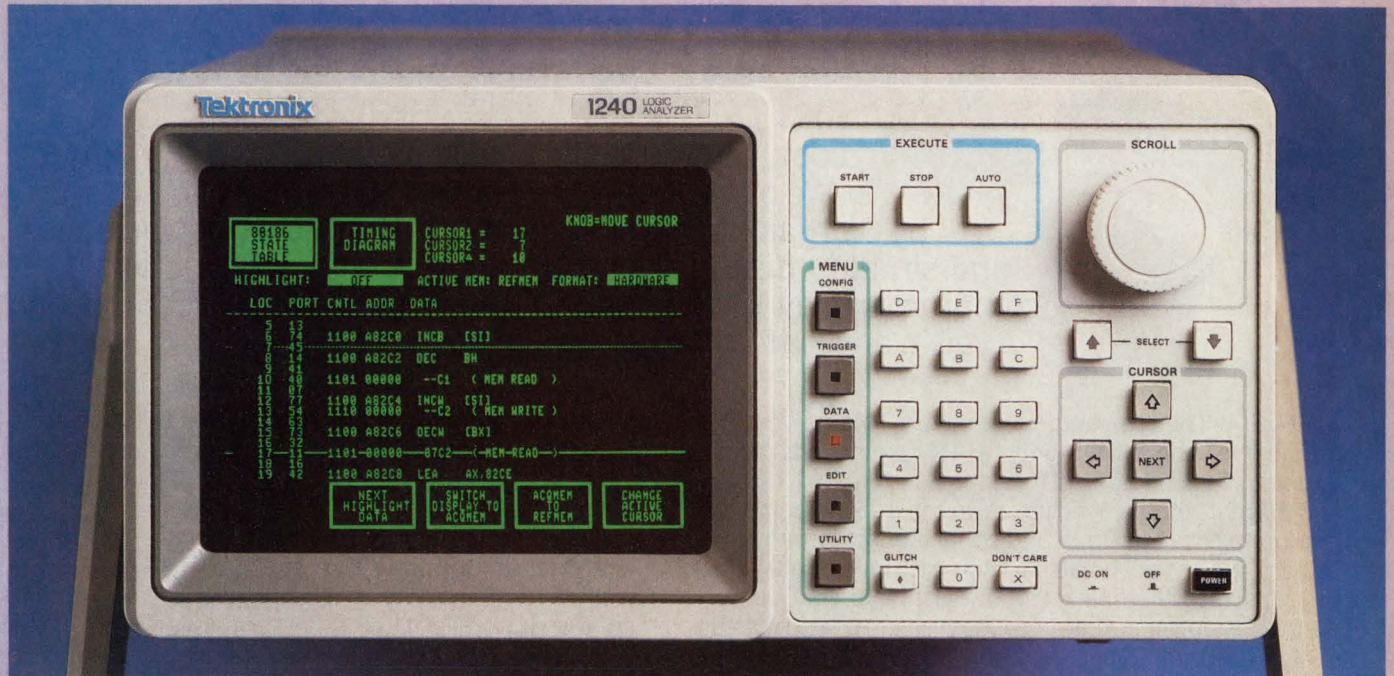
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	150	240	IMS2630-15
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	120	190	IMS2620-12
	150	240	IMS2620-15
64Kx1	100	160	IMS2600-10
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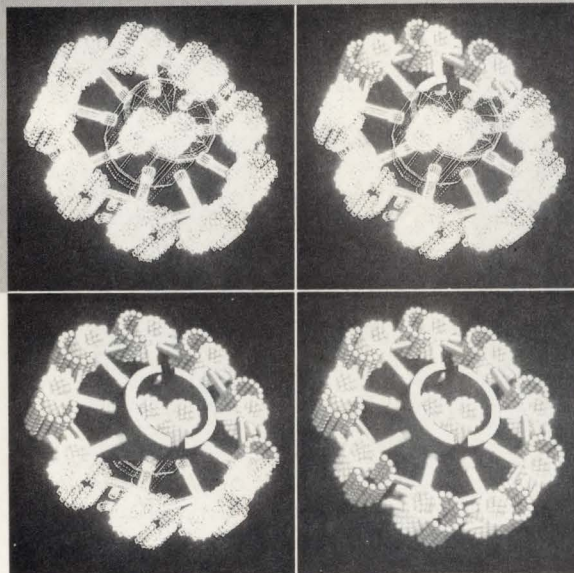
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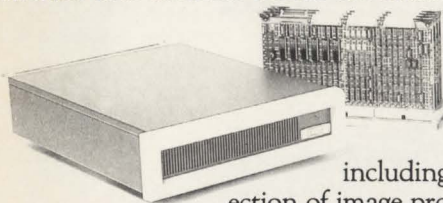
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CIRCLE 15

Third interface specification stirs rigid 5¼-in. dispute

A third challenger emerges in the 5¼-in. rigid disk interface melee. Seagate Corp (Scotts Valley, Calif) doubles the data rate of its present ST506 interface with the newer ST412HP specification, bringing transfers up to 10 Mbits/s. The higher data rate translates into roughly 40 percent greater capacity than present drive and controller designs.

The ST412HP specification requires few modifications to upgrade present ST506 drive and controller

data separator on the drive itself. A stepper mode within the ESDI specification is the principal casualty of the Seagate proposal since it retains the same commands and signal definitions of the ST506 interface.

Compatibility issues

Upward compatibility is the strongest advantage that vendors mention as they move to the ST412HP specification. Drive manufacturers implementing the new specification include Atasi (Milpitas, Calif),

mand contained in the storage module drive (SMD) interface, this mode allows the read/write head to microstep a specified distance from the center of the track. Designers can compensate for errors occurring from spindle runout or thermal expansion of the media in this manner.

Such problems typically affect drives with open-loop positioning systems. In these systems, the stepper motors translate the number of step pulses to the physical posi-

	<u>ST506</u>	<u>ST412HP</u>	<u>ESDI</u>	<u>ANSI BSR X3.101</u>
Maximum data rate	5 Mbits/s	10 Mbits/s	10 Mbits/s	10 Mbits/s
Data encoding scheme	MFM	MFM	NRZI	NRZI
Data separator	On controller	On controller	On drive	On drive
ST506 protocol	Yes	Except for Recovery	Step mode only	No
Cabling	34 and 20 pins	34 and 20 pins	34 and 20 pins	Single 50 pins
Drive vendors	Industry wide	Atasi Priam Seagate Tandon Vertex	Maxtor Memorex MPI/CDC Disctron	Priam
Controller vendors	Industry wide	Adaptec DTC Western-Digital	Adaptec DTC OMTI	Xebec DTC

designs, since it retains the modified frequency modulation (MFM) data encoding scheme with the data separator on the controller. As such, the Seagate proposal steals some thunder from two competing interfaces: the Enhanced Small Disk Interface (ESDI) and the American National Standards Institute (ANSI) BSR X3.101 specification (see *Computer Design* article, Oct 1983, p 32). These proposals also specify data transfer rates of 10 Mbits/s. However, they call for non-return-to-zero, change on 1 (NRZ1) data encoding with the

Priam Corp (San Jose, Calif), Tandon Corp (Chatsworth, Calif) and Vertex Peripherals (San Jose, Calif). Controllers will be available from Adaptec (Milpitas, Calif), Data Technology Corp (Santa Clara, Calif), and Western Digital (Irvine, Calif).

Most of the ST506 commands and signal definitions remain the same in the new interface, as well as the cable arrangement (34-pin and 20-pin). A Recovery mode is the main difference between the two. Similar to the Servo Offset com-

tion of the head, and previously could not compensate for data located off the center of the track. On the other hand, closed-loop positioning systems probably will not use the Recovery mode. Such systems usually rely on a dedicated servo surface to accurately position the head rather than the number of step pulses alone.

While the Recovery mode may be the major difference between the ST412HP and ST506 interfaces, existing controllers cannot support
(continued on page 26)

Interface dispute

(continued from page 25)

the newer drives, and existing drives cannot work with the newer controllers. The higher data rate called for in the ST412HP specification requires redesigning the data separator to account for a narrowed timing window.

With data and clock pulses combined in MFM encoding, the controller must be tuned to handle specific data rates. Data and clock signals must be extracted quickly enough to frame the data and detect errors during transmission. The overhead necessary to perform these operations ("window margin") is roughly cut in half when moving from the 5-Mbit/s transfer rate for the ST506 interface to the 10-Mbit/s rate called for by the ST412HP proposal.

Drivers and receivers might also change to accommodate the higher transfer rates. A product line manager with International Memories (Cupertino, Calif) notes that it may be too much to ask present drivers and receivers to operate at twice the speed of the ST506 specification without redesign. Furthermore, a spokesperson for Vertex Peripherals admitted that the increased bandwidth of the new interface forces the redesign of the read/write channel on the disk drive itself.

Related to the issue of data separation is error correction and detection. The narrower timing windows forces error correction code (ECC) circuitry on controllers to work more quickly, with the increased likelihood of 1- or 2-bit errors cropping up during transmission. Western Digital can provide only cyclic redundancy code (CRC) checking in its initial 412HP controller because its present chip set cannot handle ECC calculations at the increased transfer rate. However, Adaptec has announced that its controller will provide ECC checking at 10 Mbits/s.

Such capabilities will be critical as the ST412HP drives and controllers shoot beyond the present 10-Mbit/s transfer rate to 15 Mbits/s with run-length limited (RLL) coding. This data compression scheme increases capacity by as much as 50 percent over MFM encoding. Flux transitions are not converted on a one-to-one

basis in RLL coding (as is the case with MFM). Rather, RLL coding uses a translation table to generate a greater number of bits than flux transitions. For example, a two-flux transition might convert to a 3-bit pattern.

On the other hand, RLL coding schemes tend to amplify bit errors. What originally was a 1- or 2-bit error with MFM coding becomes a 7- or 8-bit error with RLL codes. Thus, RLL codes put a greater strain on ECC circuitry than does MFM coding.

Competing interfaces

These potential limits on the maximum data rate of the ST412HP interface leaves some glimmer of hope for the ESDI and BSR X3.101 proposals. Since data and clock signals are separated at the drive, maximum data transfer rates are largely determined by the clock rate. In addition, ECC computations are a lesser burden on the controller because the controller is less susceptible to narrowed timing windows as in MFM schemes. Finally, RLL compression schemes can bring effective data transfer rates to as high as 24 Mbits/s for either proposal.

As a result, vendors like Magnetic Peripherals, Inc (Oklahoma City,

Okla), Maxtor, Inc (Santa Clara, Calif), Disctron (Milpitas, Calif) and Memorex Corp (Santa Clara, Calif) remain committed to the ESDI interface. Lingering doubts about such issues as soft-sectored formatting, RLL codes, and maximum data rates were resolved in a revised specification, and products are scheduled for production early next year.

Such is not the case with the BSR X3.101 interface. No drive vendor besides Priam has publically committed to support the interface, although several controller vendors have products available. Much work remains to bring the specification from the 8-in. world to the smaller drives in such areas as soft-sectoring and RLL coding.

So it may still take six months to a year before one interface becomes the *de facto* standard as the ST506 had done. In fact, a spokesperson for Data Technology Corp (Santa Clara, Calif) believes that two interfaces can coexist. This spokesperson notes that sophisticated users may demand features such as diagnostics and serial transmission not found in the ST412HP interface. Only time will tell.

—Joseph Aseo, Field Editor

DATA COMMUNICATIONS

Network controllers grow smarter/smaller

Increasingly intelligent network controllers promise increased functionality in a more compact package. Network interface chip sets assume functions previously handled by discrete logic, while onboard 16-bit microprocessors off-load much of the communication processing from host computers. Furthermore, embedded software simplifies host interfaces to high level system calls.

Prime examples of this trend are the Ethernet Node Processor (ENP) family from Communication Machinery Corp (Santa Barbara, Calif) and the iSBC 186/51 COMMputer from Intel Corp (Santa Barbara, Calif). They take advantage of the large

number of functions integrated on the latest generation of interface chip sets (see *Computer Design* article, Mar 1983, p 170). Examples of these are the 82586/82501 from Intel itself as well as the LANCE, developed jointly by Advanced Micro Devices (Sunnyvale, Calif), Digital Equipment Corp (Maynard, Mass) and Mostek Corp (Carrollton, Tex).

VLSI magic

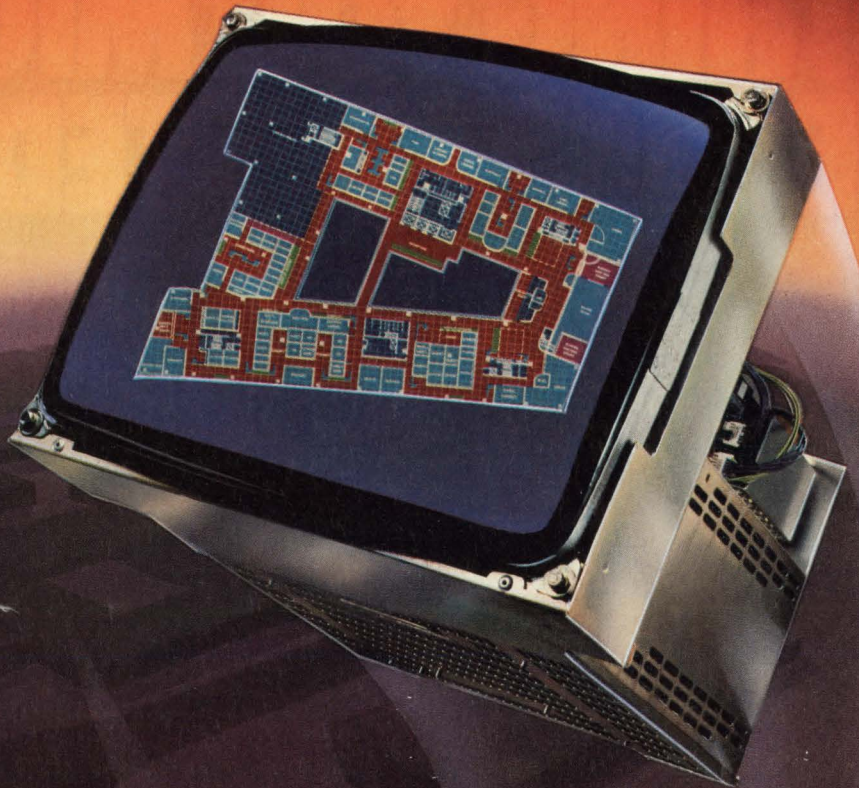
Both the 82586 and the LANCE handle functions associated with the physical link and data link layers of the ISO open system interconnect model including layers 1 and 2:

(continued on page 30)

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Network controllers

(continued from page 26)

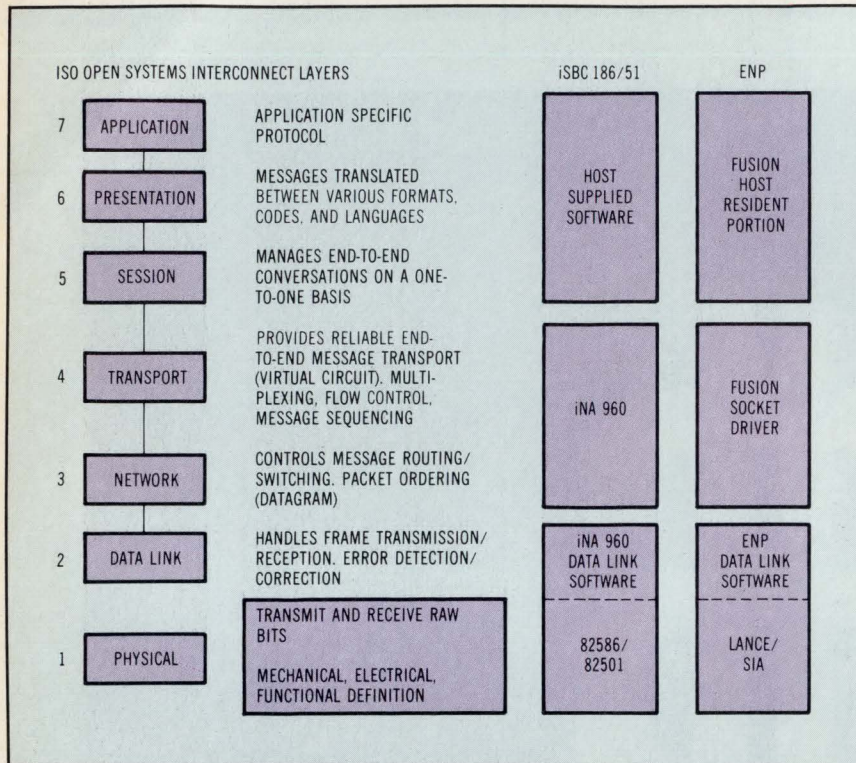


Fig 1 The iSBC 186/51 and ENP network interface chips supervise the operations of the serial interface through the data link software.

framing, addressing, bit-error detection, link management, and data modulation (Fig 1). Multiple memory buffers and compilation of network statistics (eg, number of error retries) are also supported.

Separate chips connect the controller with an Ethernet transceiver (Intel's 82501 and American Micro Devices Serial Interface Adapter). Functions include signal encoding/decoding, clock recovery, and signal level conversion. Loopback testing is also provided to identify internal errors as well as errors occurring during transmission on the bus itself.

This high level of integration in both chip sets makes them well suited for high performance applications like disk and printer servers. Earlier network interface chips such as the 8001 Ethernet data link controller from Seeq Technology (Milpitas, Calif) and 3Com Corp (Mountain View, Calif), or the MB61301 data link controller, developed jointly by Ungermann-Bass (Santa Clara, Calif) and Fujitsu-America, Inc (Santa Clara, Calif),

have limited capability. They provide only the essential functions (physical and data link) defined in the Ethernet specification. Furthermore, they manage only one transmit or receive buffer at a time.

High performance applications require multiple memory buffers for back-to-back or sequential incoming messages and sequential outgoing messages. With earlier chips, this required additional memory access logic to implement these capabilities. However, this may be beneficial if designers wish to tailor the network interface to a specific application, or when a lesser performance is desired.

Both the ENP and iSBC 186/51 fully utilize the multiple message buffering capabilities of the LANCE and 82586. The former uses the contiguous ring of buffer descriptors found in the LANCE, while the latter takes advantage of the linked list arrangement implemented on the 82586.

With the contiguous ring arrangement, the ENP controllers can configure as many as 128 active buffers

(continued on page 32)

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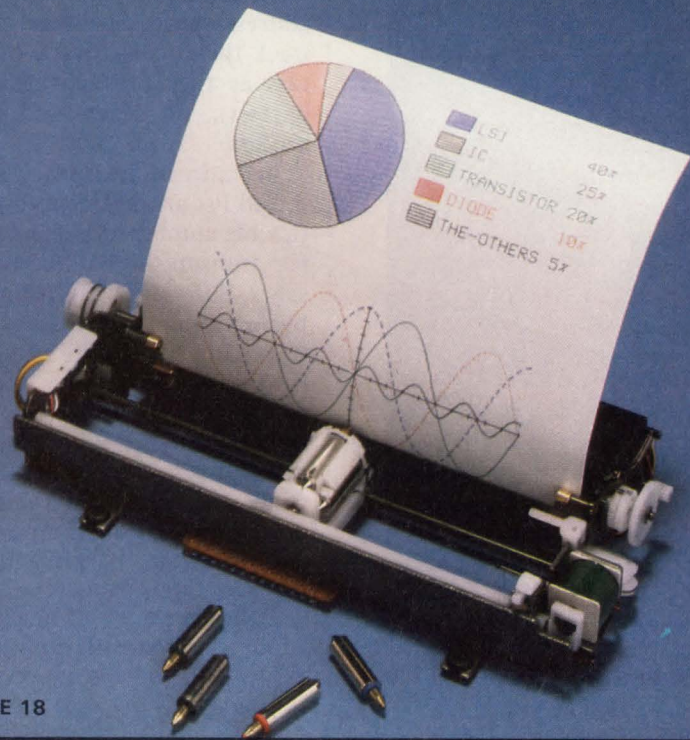
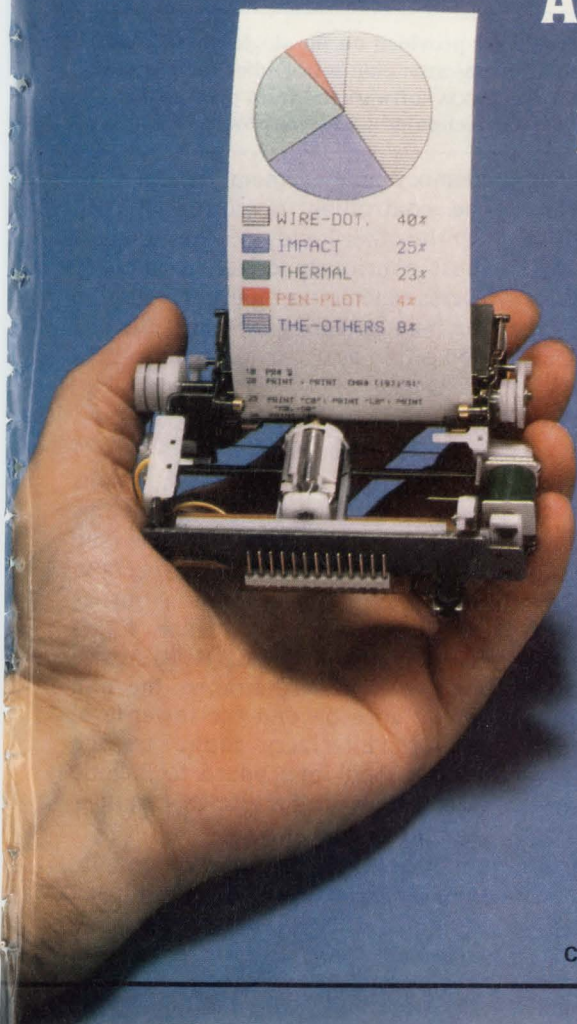


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Network controllers
(continued from page 30)

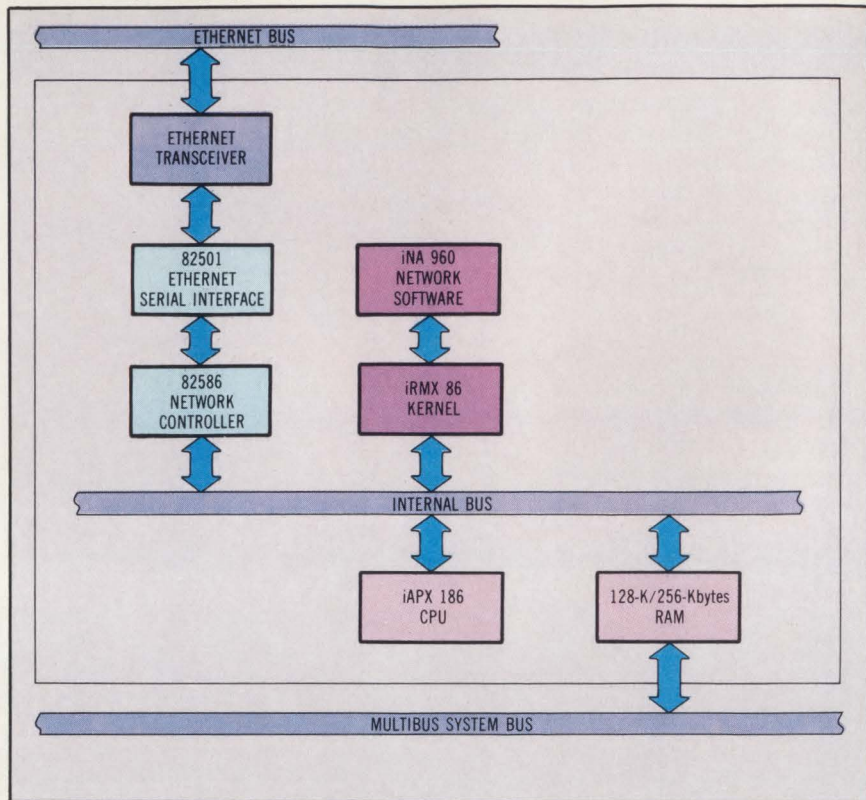


Fig 2 Necessary hardware and software are provided on the single-board iSBC 186/51 network controller from Intel. The 82586/82501 chip set handles the physical interface with Ethernet while the iNA 960/iRMX86 software modules process the messages. The iAPX processor provides the computational horsepower.

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*See Engineering Bulletin 27-0027-51 (part # 52-378-001). **Spectrum's testing facilities meet all FCC, VDE, CISPR, CSA and MIL-STD 461 A/B requirements.



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for both transmitting and receiving messages. These 8-byte long buffers are located in fixed areas in a 24-bit address space. Software must then track the circular queue of descriptors as they are activated (receive buffers), or deactivated (transmit buffers).

In contrast, the iSBC186/51 uses the linked list arrangement to provide a flexible number of buffers as needed for transmitting or receiving messages. Software handles linking new buffers, unlinking old buffers, and traversing the linked list. The 82586 controller itself fetches the address of the next buffer descriptor from the link field of the previous descriptor. With this flexibility, system designers can spread buffer descriptors anywhere in a 64-Kbyte address range, or place them in a block as the ENP does.

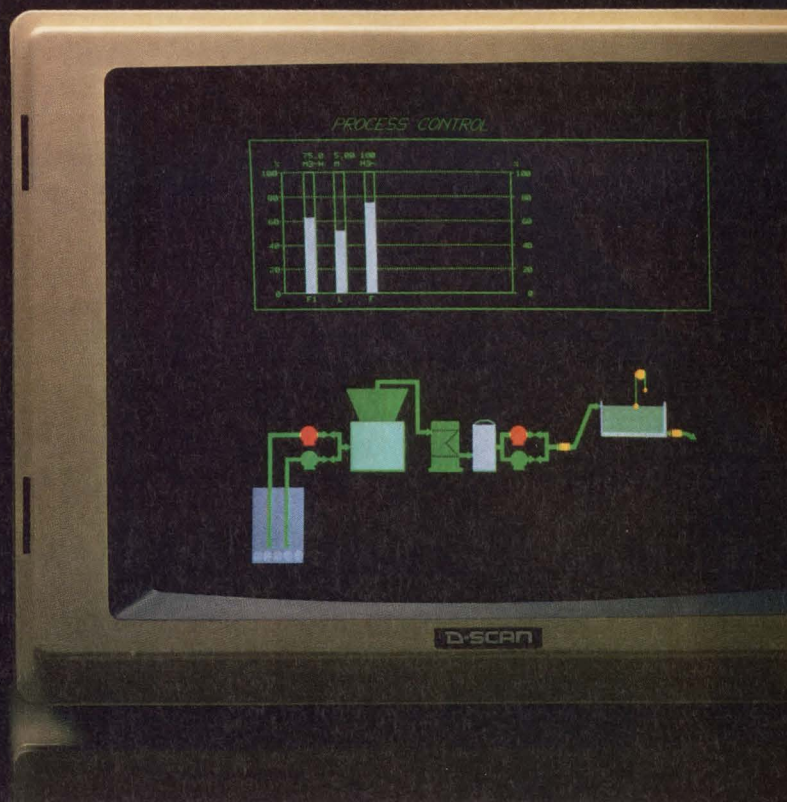
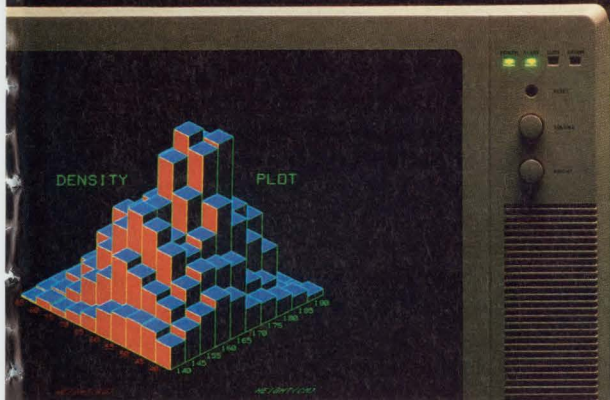
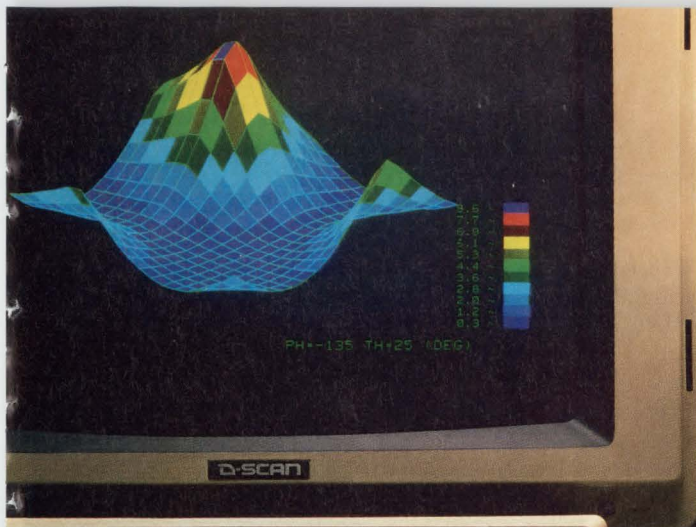
Either memory arrangement has enough software flexibility to mesh easily with the I/O supervisors and

memory management schemes of the controlling operating system. On the other hand, system designers must consciously design a memory access scheme that meshes well with the host operating system if the less powerful 8001 or MB61301 chips are used.

Controller comparisons

The large number of functions integrated on the interface chips reduces the board size that the iSBC 186/51 and ENP controllers occupy. Both share a single-board layout, as does the Excelan (San Jose, Calif) Exo/1 controller (see article, Apr 5, 1983, p 34). Furthermore, the ENP family goes beyond the lower-level network interfaces found on the Excelan and Intel board to include Xerox Network Service (XNS) upper layer protocols as well.

Previously, full network implementations required a multiboard
(continued on page 34)



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INSTRUMENTS

Network controllers

(continued from page 32)

controller like the FE-11/NS from Advanced Computer Communications of Santa Barbara, Calif (see article, May 1983, p 33) or the EC/1 from Bridge Communications (Cupertino, Calif) (see *Computer Design* article, Jan 1983, p 41).

Both controllers have dedicated 16-bit microprocessors to handle interrupts generated by the network. Thus the host computer is relieved of monitoring network traffic. In addition, higher level protocols can be off-loaded to free the host to handle only applications processing. The ENP family uses a MC68000 running at 10 MHz, while the iSBC uses an iAPX 186 processor operating at 8 MHz.

Onboard microprocessors also allow memory management to be tailored to the needs of the network interface chips. Both controller

boards incorporate 128-Kbytes of RAM for multiple message buffers (expandable to 256-Kbytes on the iSBC186/51). Memory on the iSBC186/51 can also be shared with other processors residing on Multibus.

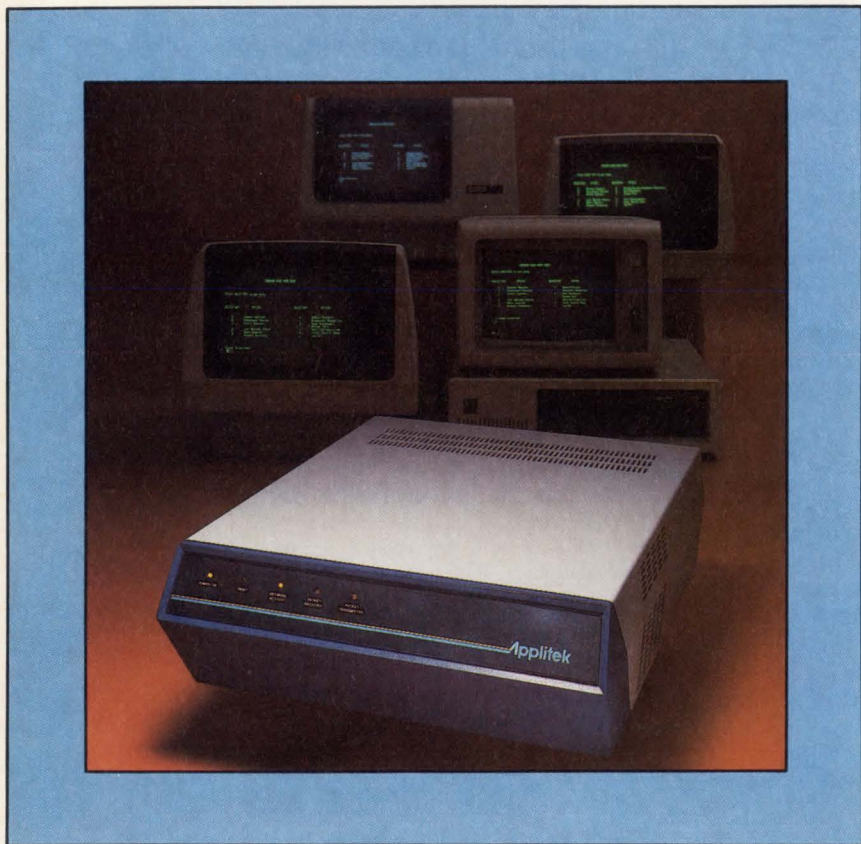
Embedded software executives not only manage the memory resources, but also supervise the transmission and reception of messages. The iNA 960 software module on the Intel board (Fig 2) also provides datagram and virtual circuit services. On ENP controllers, the FUSION package from Network Research Corp of Los Angeles, Calif (see article, Feb 1983, p 40) handles such services. Furthermore, the FUSION package implements XNS protocols that roughly correspond to layers 5 to 7 of the ISO model.

These layers include such services as file transfers to remote nodes, remote task execution, and terminal emulation.

Implementation of higher level protocols restricts the uses of the ENP controllers. For example, the FUSION program can run only on systems running under Unix, or VAX11 machines executing the VMS operating system. On the other hand, the iSBC 186/51 can run under iRMX86 already embedded, or interface with any host operating system. System designers need only write the interfaces to iNA 960 in the latter case since interfaces are already provided for iRMX86.

The iSBC 186/51 and the ENP-30 both fit on a single Multibus board. ENP versions are available for Unibus, Versabus, and VMEbus.

Local area network offers choice of access methods



Add another access method to those already available for local area networks. Slotted time division multiple access, contention, and token passing each serve one kind of application best. UniLINK, however, merges the benefits of several.

Environments needing a local area network (LAN) contain dissimilar devices with different communication needs. The traffic generated by synchronous and asynchronous devices differs, as does that from intelligent and nonintelligent terminals. To offer high performance under these varying traffic conditions, Applitek developed the UniLINK access method. This method adjusts automatically to traffic, thus providing both guaranteed and immediate access.

A universal LAN, UniLAN combines advantages of three network access methods to accommodate all device types under all traffic conditions. Based on the UniLINK access protocol, the network provides both guaranteed and contention network

(continued on page 36)

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LAN access methods (continued from page 34)

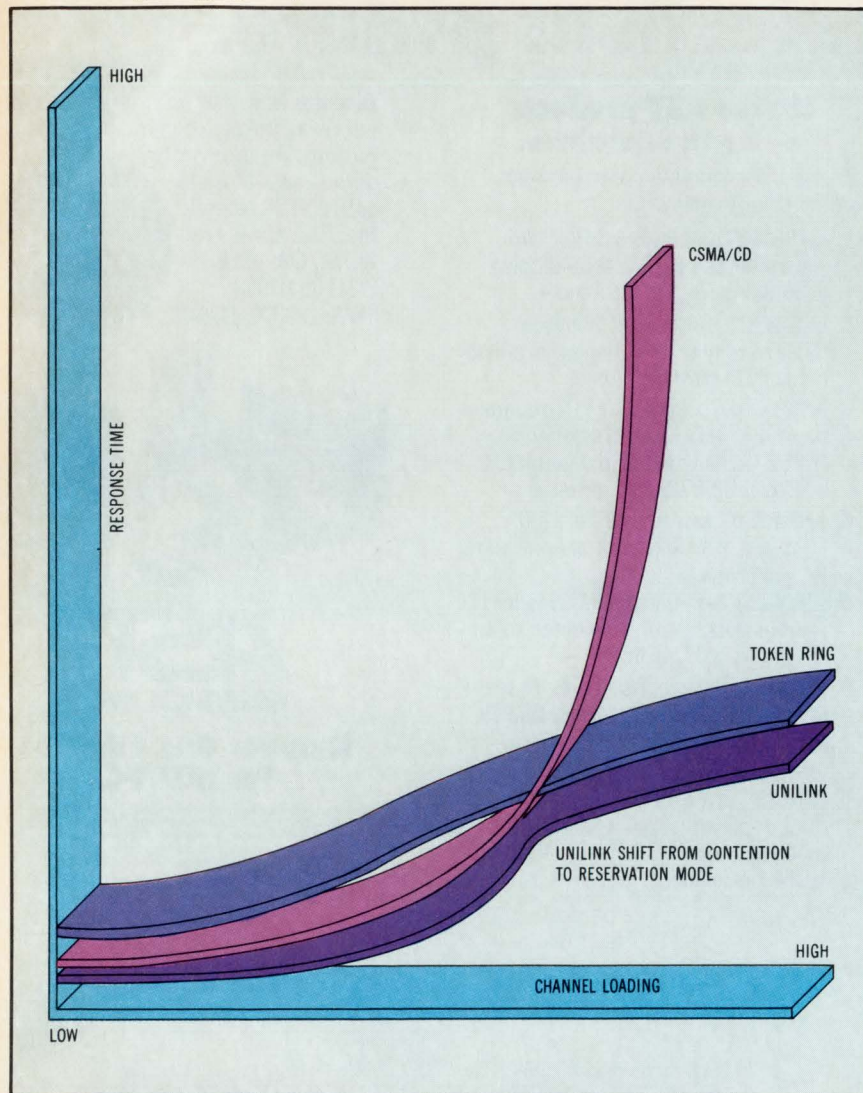


Fig 1 The UniLINK access method adjusts automatically to network traffic. Light terminal type traffic gets instant access of CSMA/CD systems. When the load increases or intelligent synchronous devices are added, the network automatically shifts to token-passing type access.

access simultaneously on the same channel and operates at 10 Mbits/s.

When the network is lightly loaded with asynchronous terminal type traffic, the quick access of carrier sense multiple access with collision detection (CSMA/CD) protocols is provided. When the traffic load increases, or intelligent synchronous devices are added, the guaranteed access of token-passing systems is supplied.

UniLINK is defined as an adaptive message division multiple access method. It operates in both contention and dedicated modes with variable and fixed message lengths. Adjustments to changing network

conditions are automatic, making unpredictable traffic patterns easy to manage (Fig 1).

This method uses two rules to access the network. The first rule requires that time on the network be broken into messages, with implicitly numbered messages grouped into message blocks. The second rule requires that interface units transmit messages only during their assigned number. Message numbers can be assigned for use on either a dedicated or a contention basis.

Performance is determined by the way message numbers are allocated to the interface units. If all message numbers are assigned to all interface

units, the network performs as a CSMA/CD network. If each message number is assigned to only one interface unit, and each unit has a set of message numbers to use, then the network performs like a token-passing network.

To provide both token-passing and CSMA/CD performance, dedicated message numbers are assigned to interface units with devices that require guaranteed access. Contention message numbers are assigned to interface units having asynchronous devices attached.

The method's use of an algorithm to allocate message numbers without using a central controller ensures dynamic configuration. This algorithm automatically assigns all message numbers as contention message numbers when the network begins operation. Interface units then request dedicated assignments as needed, and relinquish them when they are no longer needed. The dedicated-to-contention access ratio on the network can therefore be controlled.

The physical link between user devices and the network occurs through the network interface unit (NI10/T). This interface is designed to follow the seven layers of the Open Systems Interconnection (OSI) model of the International Standards Organization (ISO). Operating on baseband or broadband coaxial cable or optical fiber cable, the unit consists of a media access unit, network processor, subscriber processor, and device interfaces (Fig 2).

The media unit connects the interface to any common networking cable using IEEE 802 compatible baseband transceiver, RF modem, or optical fiber tap. The network processor has an 8-bit bipolar processor with firmware to implement the access method. It provides Manchester encoding/decoding for baseband and optical fiber networks. Packets are received from the network by 8 Kbytes of RAM that serve as receive/transmit (RX/TX) buffer. Packets to be transmitted are stored in 4 Kbytes of RAM. A resettable first in, first out memory increases data throughput.

(continued on page 38)

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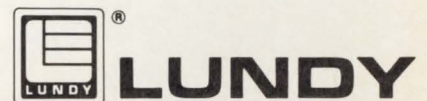
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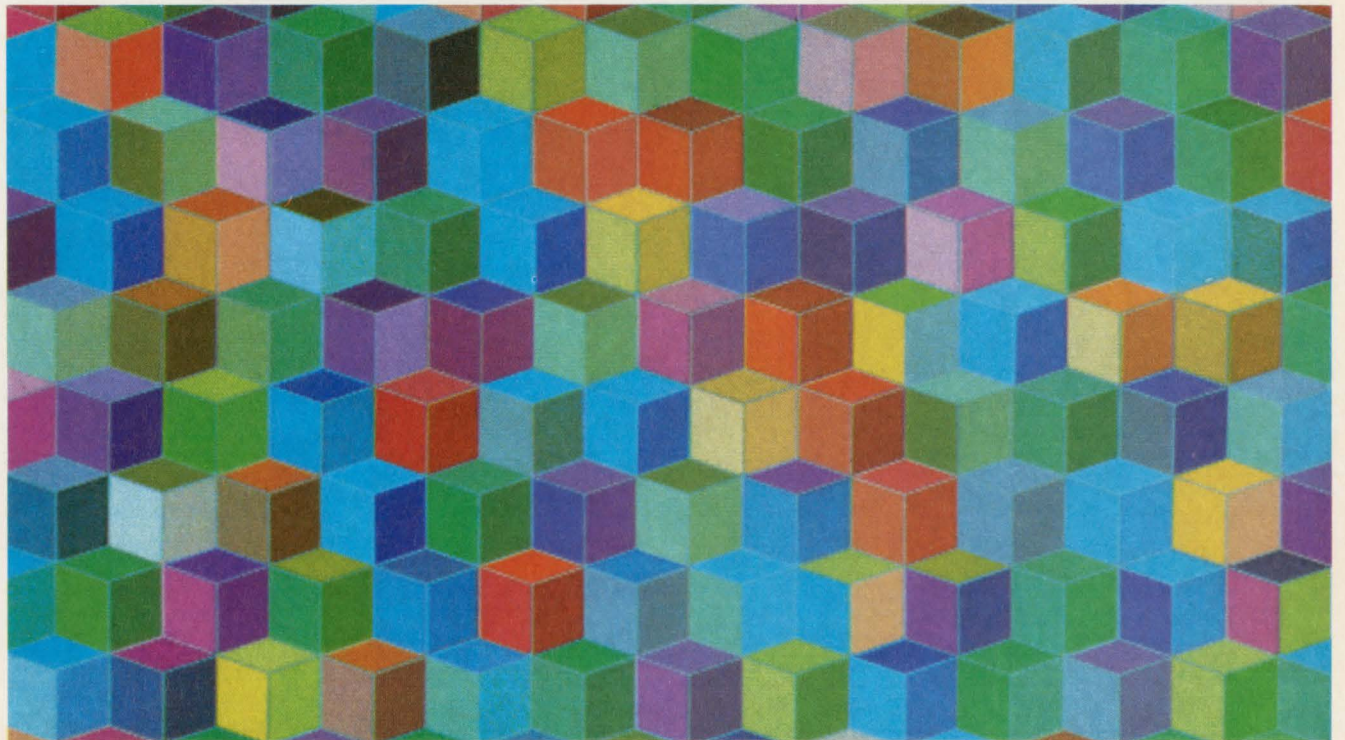
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LAN access methods

(continued from page 36)

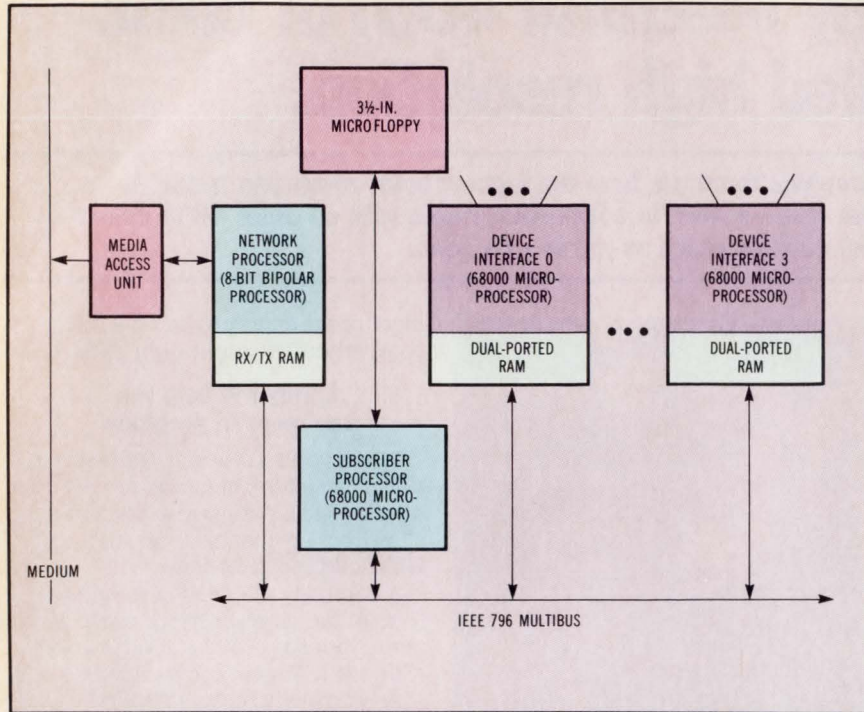


Fig 2 In the UniLAN system from Applitek, network interface hardware architecture is based on a system Multibus. Two modules, each containing boards using MC68000 microprocessors, perform device interface functions.

Handling all device interfaces, the subscriber processor is based on an MC68000 microprocessor. It coordinates device interface activities, RX/TX RAM DMA controller, and floppy disk. Up to four device interface boards connect to the system processors and RX/TX RAM via an IEEE 796 Multibus. Terminal interfaces, based on MC68000s with up to 32 Kbytes of dual-ported RAM, support up to eight RS-232/449 devices.

Network control can be performed from any network processor on the network. This distributes control and allows units to be added or subtracted from the network.

Modular software provides the user interface to the system. Presented in menu form, the command structure allows construction of sessions between devices. English language commands let ports be renamed and changes made to port configuration parameters. **Applitek Corp**, 107 Audubon Rd, Wakefield, MA 01880.

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Powerful custom VLSI chips drive graphics machines

Custom VLSI devices, fabricated by outside silicon foundries, will be increasingly important parts of hardware designs in the near future. Exploiting this capability, however, will require design automation—highly integrated design engineering workstations—and a detailed understanding of the specification requirements of the silicon foundry that actually builds the devices.

Two recent graphics products illustrate the power of this design approach. A two-board graphics engine from Weitek, based on custom floating point and image generating chips, provides extremely fast color image processing. In addition, a terminal/workstation from Silicon Graphics, Inc, is based on a VLSI geometry engine, which completes realtime display of three-dimensional images.

The graphics problem

Calculations needed to display a three-dimensional color image are

complex. Objects are normally described in terms of world coordinates (ie, the locations in space of their edges, the location of the viewer, and the direction of the light). From this description, the computer must calculate intensity values and colors for the nearly one million pixels in the rectangular display field of a typical high resolution color monitor.

Two approaches have traditionally been used to build display images. The first uses a powerful general purpose computer to calculate values and prepare files of values for later display. The Cray-1, used for some of the special effects in the movie TRON, is an example of this approach, and its drawbacks. The machine is expensive, and the process is relatively slow—several minutes to several hours per frame. The second approach has been to build specialized hardware for the graphic display calculations. While this may be faster and much cheaper than dedicating an

entire mainframe to the calculations, the custom graphics hardware still ends up with a six-digit price tag. Design and manufacture of a display processor with the size and complexity of a small minicomputer is likewise a long and expensive process.

A VLSI implementation of complex functions saves board space and power, allows greater speed by cutting transmission delays, and reduces costs. Silicon is cheap, while iron, gold, and PC boards are expensive. Shrinking the complex graphics functions onto silicon has allowed the two companies to integrate them with relative cost effectiveness into other products.

Weitek's two-board graphics engine uses two sets of fast proprietary chips to perform graphics calculations. The first two-chip set, located in the array processor, is a 32-bit IEEE standard floating point unit. The other, also a two-chip set, fills and colors
(continued on page 40)

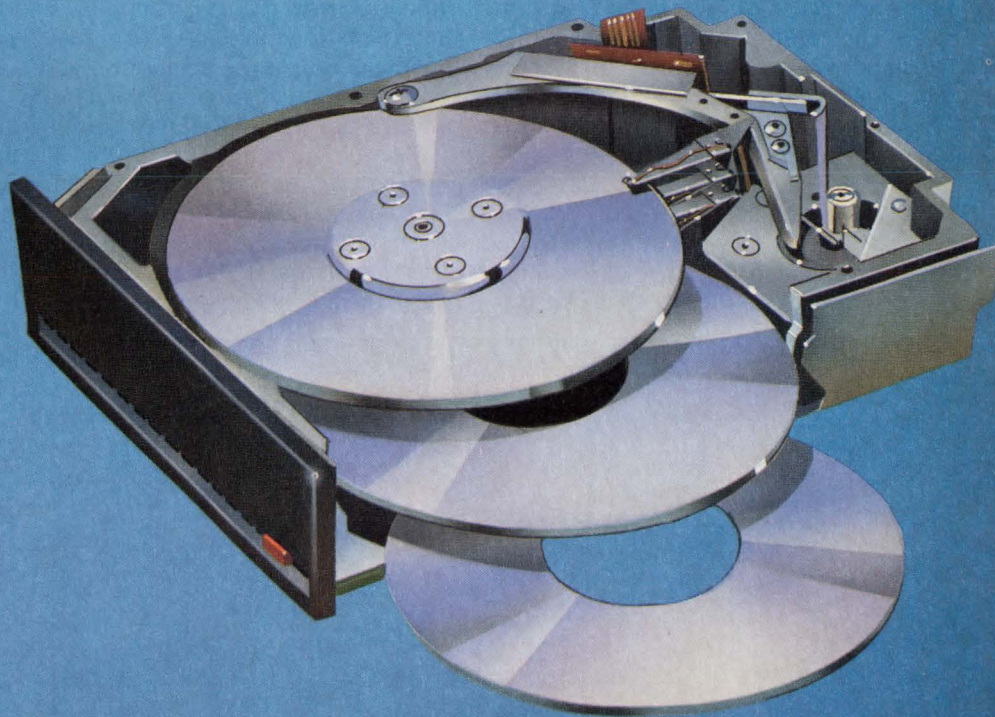
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13.34 MB

26.7 MB

40 MB



Custom VLSI chips

(continued from page 39)

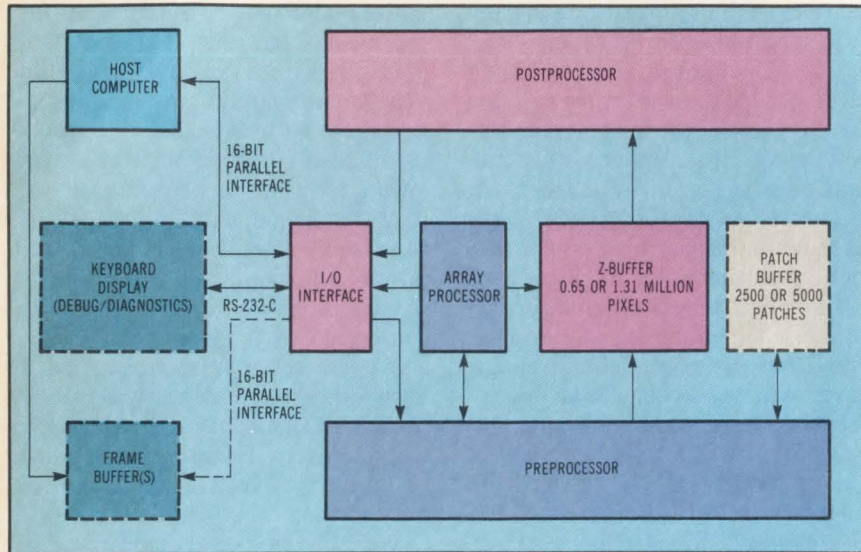


Fig 1 The twin hearts of Weitek's graphics engine are the floating point and tiling chip sets in the array processor and the preprocessor. The postprocessor is essentially a microcomputer that can be programmed to format pixel data for most frame buffers.

the small polygons and lines which make up the surface description (see Fig 1). The engine plugs into the backplane, and acts as a graphics coprocessor to relieve the host CPU of the computations. It takes image data from the host, performs graphics calculations, and returns bit-mapped data that is suitable for display on a raster monitor.

Calculations

The host processor transmits to the graphics engine the three-dimensional description of the object to be dis-

played, the location in space of the point from which it is to be viewed, and the direction from which light strikes it. Given this information, an onboard array processor completes the calculations necessary to rotate the image, introduce perspective effects, and clip off parts of the image that are not to be displayed in the view port. The image at this point is still a sort of glorified "wire frame." Locations and colors of the edges and vertices that specify the surface of the object are drawn in, but the area between them is left blank, or trans-

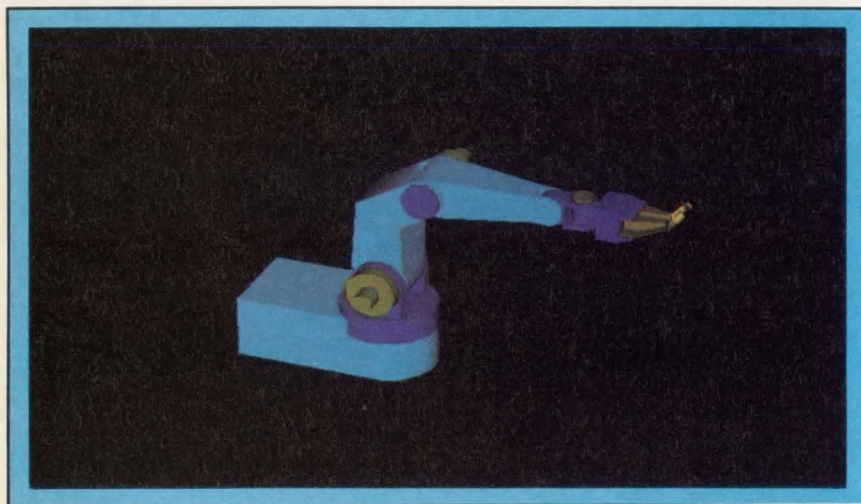


Fig 2 This robot arm image, produced by the graphics engine, is generated from a graphics data base and comprised of 1250 polygons. It was rendered on a 1280 x 1024 color raster display in less than three seconds.

parent. A preprocessor then takes over, and colors the blank areas, using one of a number of algorithms to simulate natural shading.

Images are then constructed in a Z-buffer, which lists points according to their distance from the view point. For each pixel value that the graphics engine calculates, it checks the Z-buffer to determine whether there is a point at a given X,Y position whose Z coordinate is less (closer to the view port) than that of the point being examined. If there is, it skips the calculation; if not, it enters the color and intensity data for that pixel, overlaying any point which have Z coordinates larger than the given point.

Data returned to the host is formatted in arrays of values to be loaded into a frame buffer. Each value specifies the intensity of red, green, or blue (RGB) to be assigned to a particular pixel onscreen by a raster display monitor producing a picture similar to that shown in Fig 2. The number of bits (levels of intensity) in each value can be controlled by the postprocessor to match the requirements of most frame buffers and monitors.

The graphics engine will be available for Digital Equipment Corp machines in the first quarter of 1984 for \$20,000 in OEM quantities. A standalone box implementation for other machines will also be available for \$75,000 to \$80,000 in small quantities. The company plans to make the basic chip sets and documentation available for OEMs to use in building systems.

The Iris terminal/workstation

The Integrated Raster Imaging System (IRIS) also transforms, clips, and scales as many as 65,000 coordinates per second to create raster displays. It is Multibus based, controlled by several MC68000 microprocessors, and designed for realtime creation and manipulation of two-dimensional and three-dimensional images (Fig 3).

In its terminal configuration, it is basically a very bright display device—a 68000, 10 to 12 graphics engines, a bit-slice frame buffer control, and 256 Kbytes of RAM to drive a 1024-x 1024-pixel display on a 19-in. color

(continued on page 42)

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CIRCLE 24

Custom VLSI chips

(continued from page 40)

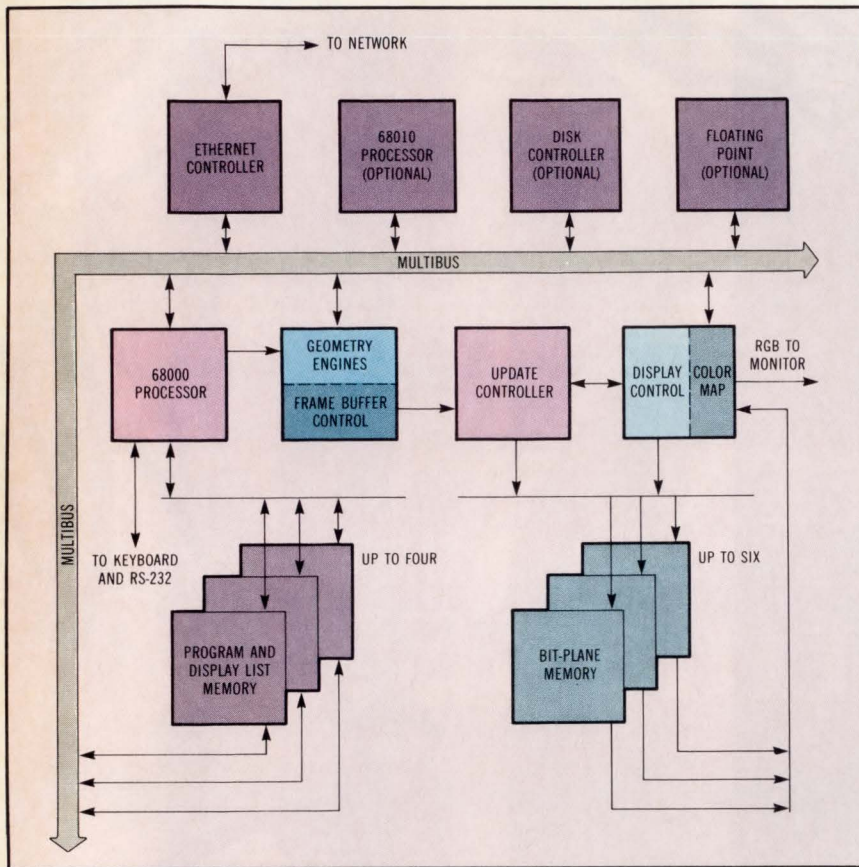


Fig 3 The IRIS workstation is built around a Multibus card cage, which allows a variety of peripherals to be added. An array of 10 to 12 geometry engines does the necessary calculations, and the bit-slice display processor controls the actual display to a high resolution monitor.

monitor. A keyboard, a three-button mouse, and an Ethernet interface complete the ensemble. For the workstation, another 68000, an additional 1 Mbyte of memory, a 46-Mbyte hard disk, Unix, and a graphics library are added.

The system offers a wide variety of colors, textures, and text fonts. It is also extremely fast—polygons are filled at up to 44 million pixels/s. The geometry engine, which makes the system's high performance possible, grew out of the 1979-80 VLSI project at Xerox Corp's (Palo Alto, Calif) Research Center. It was designed at Stanford University, and has received extensive coverage in academic journals covering both graphics and chip design.

The IRIS 1000 graphics terminal with 10-slot Multibus card cage ranges from \$37,500 to \$47,500, depending on options. The IRIS 1200,

an expanded version of the 1000 has a 20-slot card cage, and is priced from \$40,000 to \$50,000. The full graphics workstation, IRIS 4000, is \$59,500 to \$84,500. Evaluation units are currently available, with production slated to begin in early 1984.

Implications

Weitek's proprietary chips, a floating point unit and a graphics tiling engine, are actually general purpose coprocessors that would complement any CPU architecture, from a microcomputer to a Cray. By amortizing the cost of programming time involved in creating sophisticated routines across a large number of chips, the company provides an advantage to system integrators at a relatively reasonable cost.

Chip architectures are designed and specified by Weitek. The actual silicon is fabricated by merchant

houses which offer "silicon foundry" services, such as Intel, Toshiba, Synertek, and others. Weitek claims that it can go from specification to silicon in 18 months or less. This is roughly half the time usually required for development of a microprocessor chip of equivalent complexity in most chip houses.

Silicon Graphics, Inc was formed to capitalize on techniques that grew out of the Xerox/Stanford VLSI design methodology. The company projects that within three to five years, an equivalent system will be able to be built on a single chip.

As VLSI design experience is accumulated and design tools mature, this approach will become more common. Within three to seven years, it may become possible to build a computer system of almost any complexity from various vendor's component parts. Simple logic functions are today built from standard TTL parts in much the same way.

The focus of the computer industry (and the economic muscle) will then begin to shift from the manufacturer to the integrator. While chip houses will almost all continue to sell systems (especially development systems), the ability of OEMs to put together a high performance system tailored to custom needs will be vastly augmented. **Weitek**, 3255 Scott Blvd, Bldg 2B, Santa Clara, CA 95054. **Silicon Graphics, Inc**, 630 Clyde St, Mountain View, CA 94043.

—Sam Bassett, Field Editor

Circle 241

Circle 242

SYSTEM TECHNOLOGY

(continued on page 48)

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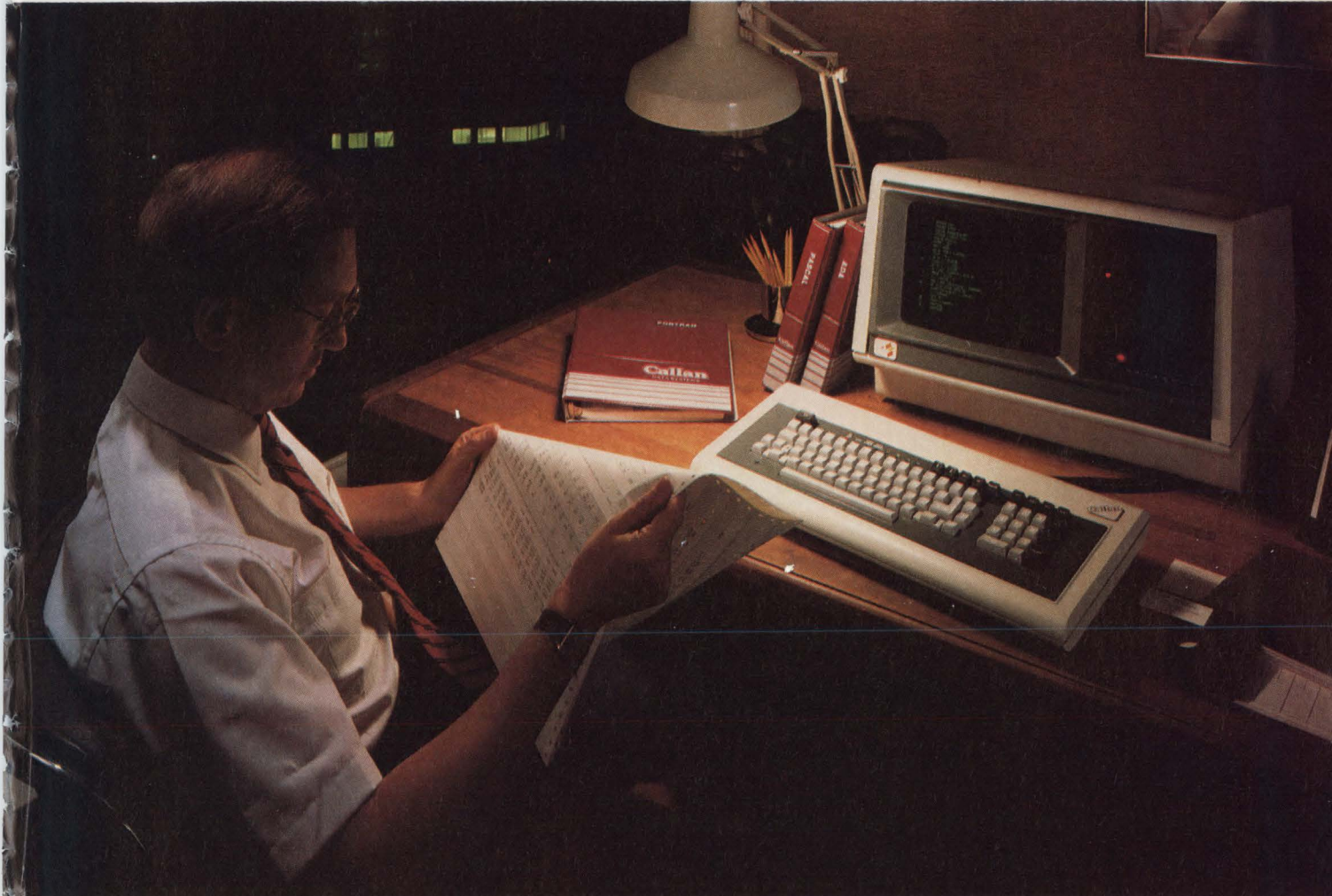
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CIRCLE 26

FACT NO.2:

**M68000 Family
microprocessors
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iAPX186
and iAPX286.**

**You still get top
system performance
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M68000 Family.**

Unadjusted, documented benchmark analysis proves M68000 superiority.

Decision makers clearly believe M68000 microprocessors outperform the other 16-bit MPUs.

The design-in rate for M68000 Family microprocessors, plus eager anticipation of the 32-bit MC68020 make this obvious. The perception is well deserved.

Yet, recent performance claims for the iAPX186/iAPX286 against the M68000 Family have raised serious issues. Examination reveals that these claims are based on "adjusted" parameters of benchmark procedures.

We went back to the original MC68000 code and repeated a series of well recognized independent benchmarks, then compared them to Intel's own published "adjusted" figures to set the record straight. What we found proves what you knew all along.

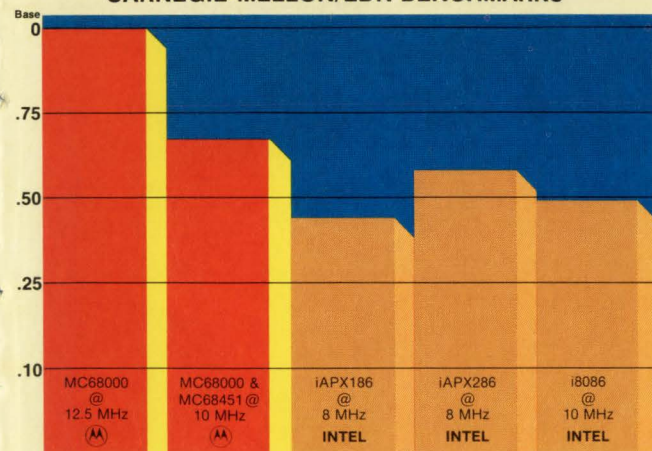
True results from independently specified procedures.

Comparison of these benchmark results, obtained in strict adherence to the unbiased specifications with the fastest devices available in all cases, demonstrates beyond a doubt the clear superiority of the 16-bit M68000 processors to the iAPX186/iAPX286. For the '286, we used the highest announced frequency.

We stress the unadjusted nature of our work and results, for, if independently specified benchmark procedures can be changed, what is the value of the benchmark? Only an unadjusted benchmark retains the intent of the original specification, and only an unadjusted benchmark result is valid.

It is axiomatic that benchmark results unsupported by a listing of associated source code are without credibility. The results summarized here are fully documented in a formal benchmark report.

CARNEGIE-MELLON/EDN BENCHMARKS



M68000: The only upward-compatible 8/16/32-bit microprocessor family.



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Source-code listings are documented.

Source-code listings in our formal benchmark report show clear, concise source code identical to the code used in familiar earlier benchmark runs. No M68000 source-code rewrites were required to mask incompatibility problems as exhibited by the MMU-protected '286 when compared to the old '8086. Our complete documentation is available. Will '186/'286 manufacturers produce anything comparable?

M68000 VS. iAPX '86—CARNEGIE-MELLON/EDN BENCHMARKS

	MC68000 @ 12.5 MHz	MC68000 & MC68451 @ 10 MHz	i8086 @ 10 MHz	iAPX 186 @ 8 MHz	iAPX 286 @ 8 MHz
I/O interrupt: Inc. & return	25.6 μ s	39.2 μ s	43.2 μ s	50.0 μ s	96.8 μ s
I/O interrupt: queue	259 μ s	393 μ s	396 μ s	446 μ s	357 μ s
String Search	127 μ s	177 μ s	201 μ s	250 μ s	128 μ s
Bit test/Set/Reset	55 μ s	83 μ s	127 μ s	158 μ s	98 μ s
Linked List	116 μ s	180 μ s	269 μ s	259 μ s	200 μ s
Quick Sort	13.9 ms	21.4 ms	38.3 ms	45.2 ms	36.1 ms
Bit Matrix Inversion	289 μ s	419 μ s	939 μ s	725 μ s	509 μ s
Avg. %	1.0	0.67	0.49	0.44	0.58

*Top number: 286 with higher priority. Lower number: 286 with task change.

Large, linear addressing is another M68000 advantage.

Other adjustments were necessary for the '186/'286 to compensate for their limiting 16-bit address-register structure. It's easy to see the handicap of the resultant 64-kilobyte segmented memory addressing with such an architecture.

The Linked List benchmark, for instance, can only be performed efficiently by an MPU with a large, linear direct memory addressing range. Its 32-bit internal architecture gives the M68000 MPU direct addressing of a linear 16-Megabyte memory. In contrast with the iAPX186 and iAPX286, lists must be held within 64K byte segments and may not straddle segment boundaries. These are serious concerns in the real world, where such limitations create an unacceptable obstacle.

And M68000 is the upward-compatible family.

A major decision like your choice of a microprocessor should be based on all possible information.

Therefore, consider the outstanding M68000 support hardware and software from both Motorola and independent suppliers - Motorola's history of high quality and production capabilities - and, the variety of major M68000 alternate sources.

Finally, of the utmost importance for transportability of your software investment and for your migration path to future products, consider the upward compatibility of the M68000 processors. It's the only 8/16/32-bit family with absolute user object-code compatibility.

It makes sense for pretenders to generate claims against the leader. It doesn't, however, alter the fact of that leadership.

Consider the overall cost/performance leadership of the M68000 Family and make your commitment. Your present and future generation products will be better for it.

Get the inside story. Ask your design engineering management.

Bridges carry software across hardware barriers

Manufacturers of relatively small (ie, non-IBM and look-alike) computer systems are beginning to realize that the concept of captive computer customers—those tied irrevocably to proprietary operating systems and applications—does not work. There is always a new spreadsheet program, a DBMS, or word processing system, that users ask for, along with the huge base of available software that runs on other vendors' machines. Building bridges has thus become good business.

A number of recent announcements indicate that this trend is accelerating. They also indicate that Bell Labs' Unix and its offspring are gaining ground as the standard operating systems for 16- and 32-bit computer systems.

In its recent report on hardware and software performance improvements, Fortune Systems (Redwood City, Calif) included compatibility with other systems as a specific tech-

nical and marketing goal. The company feels that having Unix as their operating system is a decided advantage, since independent software houses will find it cost effective to produce software with the widest possible market. The number of Unix (and Unix-like) systems available tends to support this contention. Fortune also sees compatibility with the Wang Laboratories, Inc (Lowell, Mass) word processor's user interface as necessary, even though the machines are not Unix based. This is because Wang has such a broad base of installed systems.

Documentation/software products

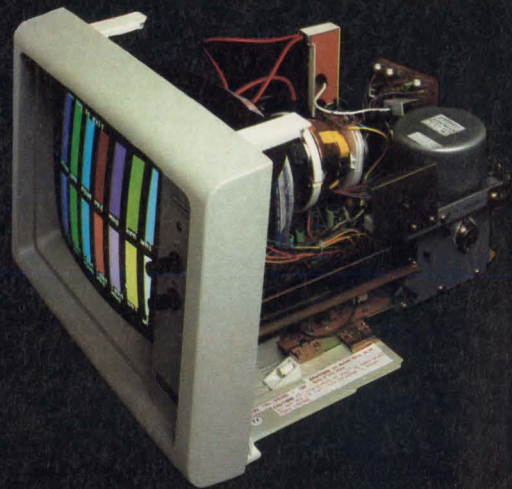
Wang, in turn, has announced the release of documentation and software products that facilitate communication with its systems. This documentation (which should help Fortune and others with a similar strategy) is a set of specifications that detail the internal structure of files

stored on its systems, including word processing image, graphics, voice, and data files. Wang explicitly encourages the exchange of editable documents between its systems and others. The Word Processing System Communication Specification (WPCS) is available now, and the Wang Information Transfer Architecture (WITA) specification will be available next June; both are \$500.

The software products will allow Wang systems to communicate with other systems via IBM 3270-compatible networks. The Information Distribution System (IDS) products connect Wang VS systems to each other or to IBM-compatible mainframe hosts through SNA or BSC networks. The Level I Host Pass-through program, priced at \$45,000, runs on an IBM host computer, and allows VS systems to communicate with one another. Level II, priced at \$58,000, allows Wang files to be stored on the
(continued on page 50)

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Bridges carry software

(continued from page 48)

IBM host and to be used by its application programs. The software, as well as VS-resident programs, will be available in March of next year.

Microsoft (Bellevue, Wash) recently announced that IBM Instruments, Inc, (Danbury, Conn) will offer the company's Xenix implementation of Unix in the 68000-based CS 9000 microcomputer. This announcement is interesting because it reaffirms the continuing relationship between the two companies. Microsoft already provides the operating system for IBM's PC and now its announced intention to make PC-DOS/MS-DOS more compatible with Xenix in the future is strengthened. Unix implementations for IBM's minicomputer lines (series 1 and model 3x) already exist, and preliminary Unix mainframe versions have been reported.

IBM is clearly not going to abandon its investment in proprietary operating system and application software. But, it does seem to be following the trend towards a standard operating system, instead of trying to establish one by fiat. If IBM decides to accept Unix as a standard operating system for its small to mid-range machines, and especially if it provides software for easy communication with its mainframes, Unix will almost certainly become the standard. IBM already provides a combination of hardware and software to link PCs to its mainframes, using 3270 protocols. More links can probably be expected within the next three years.

In regard to application software compatibility, Plexus Computers, Inc (Santa Clara, Calif) has agreed with three independent software vendors to distribute "bridge software" prod-

ucts that allow Plexus users to run software for other systems. The Sibol package (\$1295) from Software Ireland (New York, NY) is a Unix-compatible version of Digital Equipment Corp's (Maynard, Mass) proprietary Dibol language, in which all Data-system 300 software is written. Wang 2220 minicomputer software can be transported to Unix systems with TOMBASIC, a Wang-compatible Basic introduced by The Office Manager (TOM) Software, Inc (Seattle, Wash). SMC Thoroughbred Basic (\$695), from Science Management Corp (Bridgewater, NJ), makes available application libraries for systems manufactured by Basic Four (Burlingame, Calif). Combined, the three bridge products enable about 90,000 installations to move applications to Plexus machines with little trouble.

—Sam Bassett, *Field Editor*

File transfer software provides key to micro mainframe link

Existing hardware links between personal computers and multi-user hosts are complemented by software that completes the connection. Personal computer users benefit from the ability to access up-to-date information without creating multiple data bases with their attendant maintenance problems.

Access to a production data base stored on the host computer is one approach favored by many vendors. These include Cullinet, Inc (Westwood, Mass), Direct, Inc and Forte Data Systems, Inc (Santa Clara, Calif) and IBM Information Systems Group (White Plains, NY). Intel Corp (Austin, Texas) goes one-step further and separates the personal computer data base from those maintained on the host. Yet, the host still maintains overall control.

Interfaces to personal computer application programs (eg, spreadsheets, word processors) also invite different approaches. One scheme provides file interfaces to popular programs such as WordStar or Visi-

calc, while the other calls for the creation of custom programs for a specific configuration.

File transfers

Both application program interfaces and database access schemes rely on the ability to upload files from personal computers to mainframes. In the past, files could only move in one direction—from mainframe to personal computer. Typically, personal computers emulate terminal protocols when communicating with the host. No provision is made for local task processing or storage since terminals do not have these facilities. This is especially true with "dumb" protocols such as teletype (TTY) that accepts commands on a line-by-line basis. Even emulations for "intelligent" protocols like IBM System Network Architecture/Serial Data Link Communications (SNA/SDLC) only take into account screen and keyboard characteristics (see *Computer Design* article, Apr 5, 1983, p 42).

Especially lacking in any of the popular terminal protocols is a means to handle different file formats. For example, files transferred from an IBM 43XX mainframe cannot be used as direct input to a spreadsheet program running on an IBM PC emulating a 3270 terminal. Files can only be displayed locally at the PC, with programs executed at the host.

Several vendors overcome this barrier with file conversion software residing at the host as well as at the remote personal computer. An intermediate format, usually ASCII for data files and binary code for object programs then provides a common input for reformatting at either end.

With the exception of IBM, such file conversion occurs as part of the terminal emulation. Cullinet, Forte Data Systems, and Intel connect personal computers and IBM mainframes via 3270 synchronous terminal communications. Direct uses VT100 asynchronous communications to support Digital Equipment

(continued on page 52)



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File transfer software

(continued from page 50)

Micro-to-Mainframe Software Schemes					
	Cullinet	Direct	Forte	IBM	Intel
Host system	IBM 308x MVS/TSO VM/CMS	VAX-11 HP 3000	IBM 308x MVS/TSO VM/CMS	4300 MVS/TSO VM/CMS	IBM Sperry- Univac Honeywell
Personal computer	IBM PC	IPBC	IBM PC	IBM PC	Any with ASCII keyboard
Intermediate format	ASCII binary	ASCII binary	ASCII binary	ASCII	ASCII
Production database	Resides on host	Resides on host	Resides on host	Resides on host	Resides on iDIS 86/735
Application programs provided	Yes	No	No	Yes	Yes
Interface to existing software	No	No	No	Yes	Yes

Corp's PDP-11 and VAX-11 minicomputers, and HP 2622A/HP 2645A terminal personalities to connect with Hewlett-Packard HP 3000 systems.

On the other hand, IBM has selected the less powerful TTY emulation as the protocol to link its personal computers with its 4300 series computers. Software drivers already support TTY communications under the VM/CMS host operating system as well as MS DOS for personal computers. The company also has a 4994 protocol converter that supports 3270 terminal emulation, but has decided not to execute its departmental reporting system (ADRS/PC) with this configuration.

Software hooks

Beyond just file transfer capabilities, vendors also provide database query and extraction facilities. Personal computer users can browse within standard operating environments (eg, IBM VM/CMS) or data bases specifically configured for such users. An issue with either implementation is the question of database integrity.

In brief, many versions of the same file can be created and stored on separate disk drives since both mainframe and personal computer users have access. Such dispersion makes it difficult, if not impossible, to ensure that the central data base is updated with the latest revisions unless access is controlled by the database manager.

A popular scheme to restrict access partitions a section of the

host data base. Personal computer users can modify and update any file within this production data base, but cannot roam outside its boundaries. Thus, database managers can update affected portions of the master data base systematically.

Cullinet implements such a scheme with its information database (IDB) package running under IBM VM/CMS or MVS/TSO operating system. Direct, Inc and Forte Data Systems do not provide a separate data base for personal computers, although they recommend doing so within the confines of the existing database manager.

An illustration of this latter approach concerns the IBM scheme. In this case, personal computer users request data files formatted according to the particular operating system (VM/CMS or MVS/TSO). When these files are again uploaded, the database manager resident on the host then updates any records that have been updated. Updating can occur automatically for users with special ID numbers and passwords. Revisions from other users are held and the system operator then manually updates host files.

With its iDIS 86/735 database information system, Intel goes one step further and physically removes the personal computer data base from host memory. The iDIS 86/735 acts as both a file server and 3270-type cluster controller. With this scheme, it can buffer requests and download files in bulk.

Also residing on the Intel database processor are application programs for word processing and spreadsheet analysis. Both are geared for the file structure used in the resident Xenix operating system. Dedicated software can also be found on the Cullinet implementation.

Custom programs eliminate the need to reformat data for use in application programs. For example, many spreadsheets cannot use ASCII-encoded data as input. On the other hand, many personal computers already have existing programs providing the same functions. In this case, Intel also provides interfaces to popular programs such as WordStar or Multiplan. Such interfaces are similar in concept in file reformatting for different processor types.

Both Direct, Inc and Forte Data Systems plan to offer similar interfaces to existing packages. The IBM package generates reports directly from data extracted from host data bases as well as extract information produced by such display oriented programs as Visicalc and TKSolver that use the Data Interchange Format. However, screen formats and display information disappear when files are uploaded to the host. Only the ASCII-encoded data is transferred.

—Joseph Aseo, Field Editor

SYSTEM TECHNOLOGY
(continued on page 60)

MDB'S 32-BIT UNIX* SYSTEM IS WAITING FOR YOU

You've asked for a 32-bit computer system with unlimited expansion capabilities...one that is low-cost and compact yet powerful enough for multi-user, multi-tasking requirements.

So we created the MDB Micro/32¹, an MC68000 based system with 512KB memory (expandable to 4MB). This powerful system combines MDB's REGULUS with the incredible expansion capability of our in place Q-Bus repertoire of peripheral controllers... as well as our interfaces/multiplexors for all communication modes, protocols and disciplines.

The result: speed, power and versatility of systems design you can't get anywhere else!

REGULUS is MDB's UNIX... the

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They're fast, direct, and don't get in your way. The most user-friendly operator aid available today.

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Full-speed, full-range mapping in internal, external, and mixed modes. Single-word resolution. Full-range offsets.

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Eight 78-line real-time logical breakpoints for every chip, concatenated via logical switches and counters.

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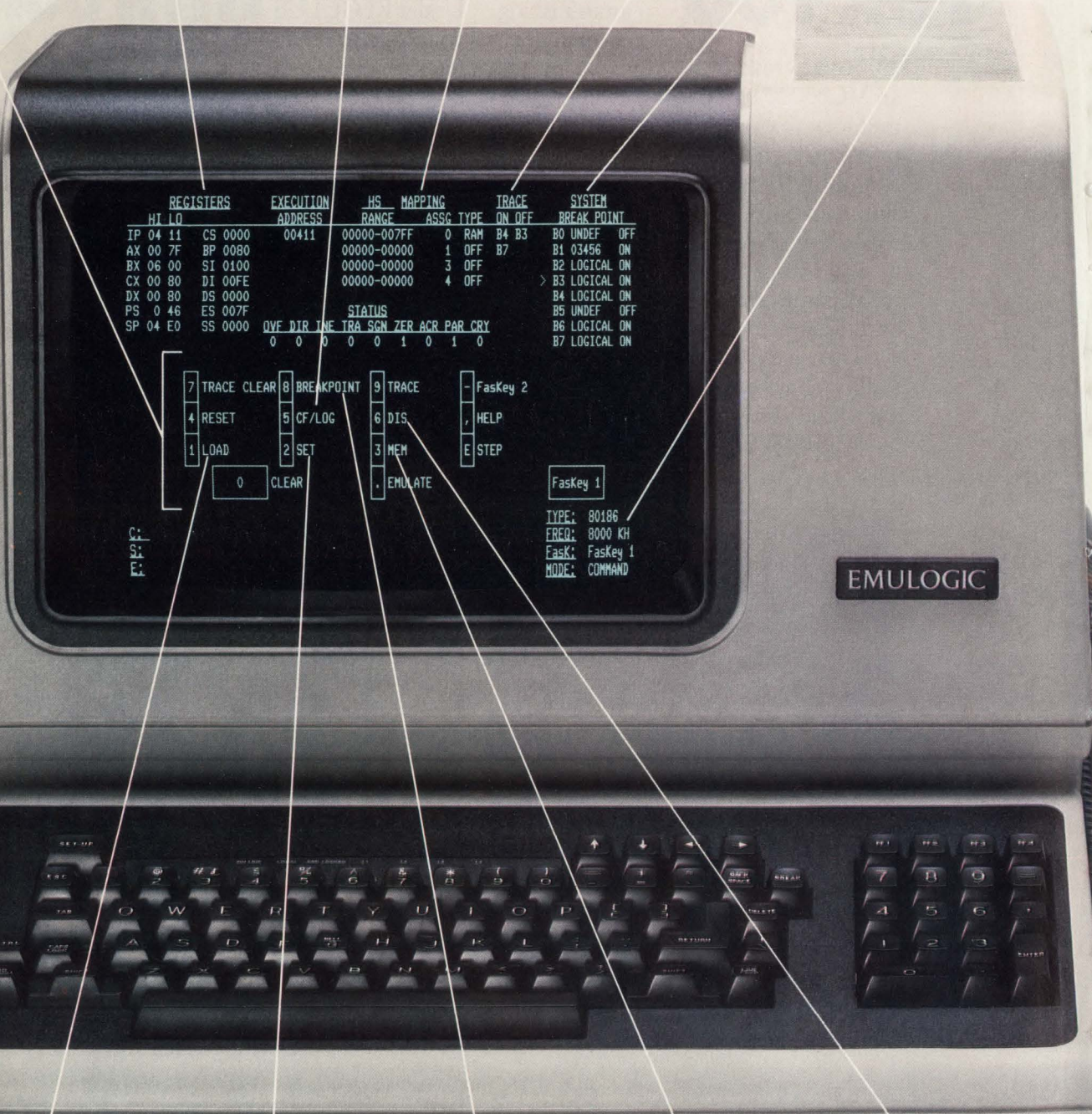
Selects screen with all Command File and Log function options.

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Breakpoint-controlled 511 x 72-bit real-time trace with precise disassembly.

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Multi-sourced time base—internal synthesizer or target clock.



REGISTERS		EXECUTION	HS	MAPPING	TRACE	SYSTEM
HI	LO	ADDRESS	RANGE	ASSG	ON	BREAK POINT
IP	04 11	CS 0000	00411	00000-007FF	0 RAM B4 B3	B0 UNDEF OFF
AX	00 7F	BP 0080		00000-00000	1 OFF B7	B1 03456 ON
BX	06 00	SI 0100		00000-00000	3 OFF	B2 LOGICAL ON
CX	00 80	DI 00FE		00000-00000	4 OFF	> B3 LOGICAL ON
DX	00 80	DS 0000				B4 LOGICAL ON
PS	0 46	ES 007F				B5 UNDEF OFF
SP	04 E0	SS 0000				B6 LOGICAL ON
STATUS						
OVF DIR INE TRA SGN ZER ACR PAR CRY						
0 0 0 0 0 0 1 0 1 0						

- 7 TRACE CLEAR
- 8 BREAKPOINT
- 9 TRACE
- 4 RESET
- 5 CF/LOG
- 6 DIS
- 1 LOAD
- 2 SET
- 3 MEM
- 0 CLEAR
- . EMULATE

FasKey 2
HELP
E STEP
FasKey 1
TYPE: 80186
FREQ: 8000 KH
FasK: FasKey 1
MODE: COMMAND

EMULOGIC

LOAD

Selects LOAD screen with all options.

SET

Selects screen with all SET options.

BREAKPOINT

Selects screen with all BREAKPOINT options.

MEM

Selects screen with all MEMORY options.

DIS

Selects screen with all DISASSEMBLY options.

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It's the best you can buy. Pure and simple.

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Up to the full rated speed of every chip with all features implemented. Doesn't steal any interrupts, stack pointers, stack space, or memory space. Handles all types of interrupts in any mapping configuration. Logical switches, counters, and trigger outputs manipulated in real time at no cost to user program.

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Now you can activate command files from breakpoints as well as the keyboard,

include pauses for user response, nest multiple files up to five levels deep. With the new LOG command you can store any sequence of operations for later use.

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Scheduled for 1984

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DEVELOPMENT SYSTEMS

CIRCLE 31

ACCORDING TO OUR THIS IS IM



Since we first entered the Winchester market two years ago, we've accomplished many things our competition claimed were impossible.

It was impossible, they said, for a floppy disk company to make a significant dent in the highly competitive Winchester market.

We've not only made a dent, we're the second-largest company in the business, and we have the capacity in place to be first.

It was impossible to expand our production capacity from 0 to 60,000 drives a month practically overnight. But we did it.

It was impossible to sell Winchesters at

such a low cost. But last year our 500 series drives were introduced at under \$500, 30% under then-standard industry costs. And since then, we've led the industry to ever-lower costs on full and half-height drives.

It was impossible to produce and ship high-performance plated media drives in high volume at prices lower than most vendors are charging for oxide media drives. One of our competitors backed away from plated media because they couldn't buy enough of it to build drives in efficient quantities.

We solved that problem by building our

OUR COMPETITION, POSSIBLE.



own plated media factory dedicated to plated media production in high volume. Because we make our own, our costs are low and we are independent of outside vendors for supply.

It was impossible for a start-up company to produce and ship a broad line of products: full and half-height drives, open and closed-loop, from 6.4 to 50 MB. But we've done it. With the help of one of the industry's best-funded R&D programs. And with our steady supply of plated media, we will soon be offering 5¼" drives that push Winchester technology to the limits of its

capacity. In high volume. At prices that are pure Tandon.

Impossible?

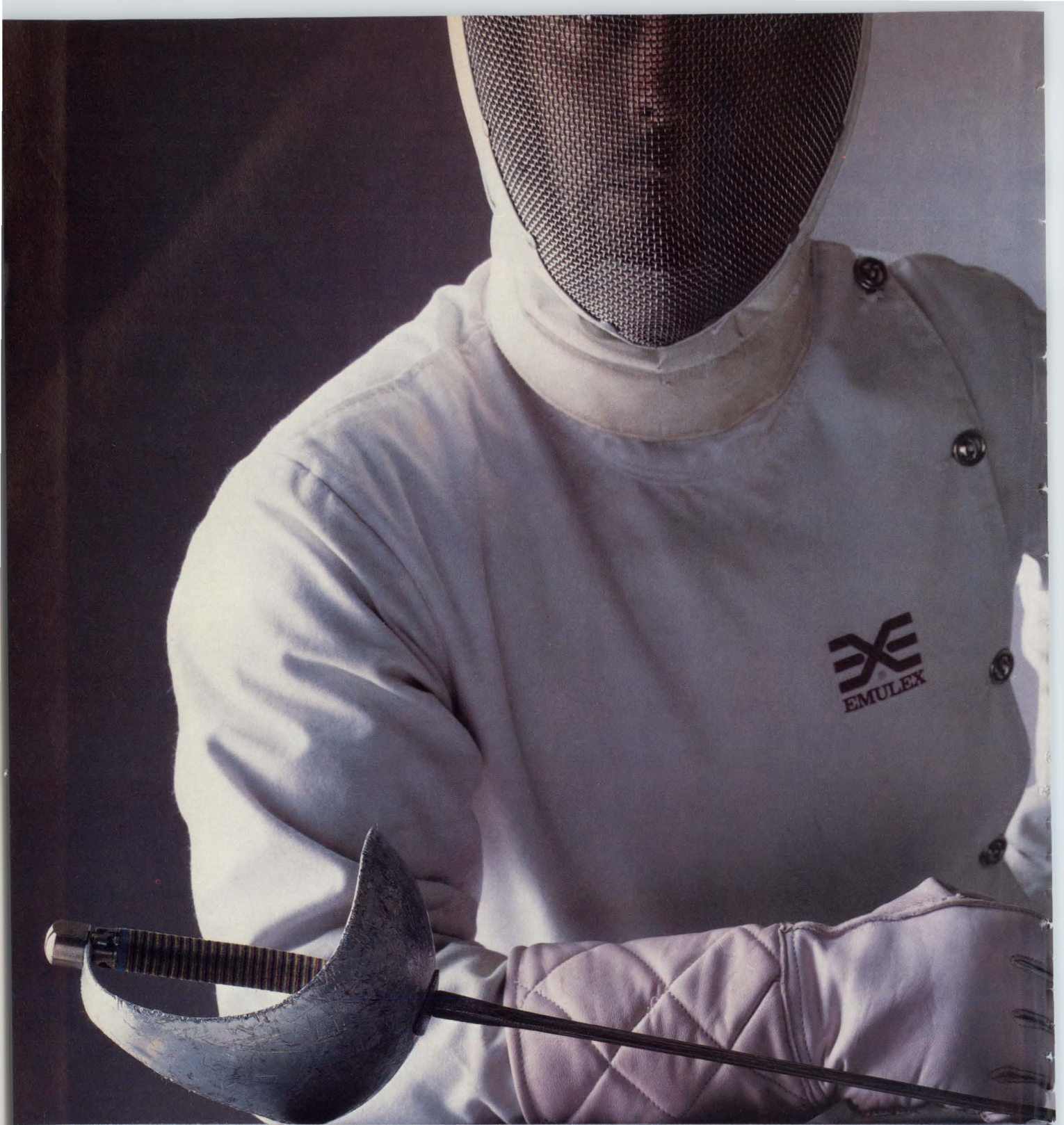
For our competition, yes.

But not for the Tandon Winchester Company.

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SABRE



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SABRE™ is a cut above anything on the market. It's a new concept in high-capacity, high-performance mass storage. A 5¼" Winchester/cartridge disk package for use with operating systems that run on DEC LSI-11 through 11/23+ microcomputers. SABRE's an innovative, RL02 software transparent storage alternative that puts 41.6 Mbytes on-line and delivers balanced backup through a versatile, removable cartridge disk. All in a compact, rack-mountable package.

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The ruggedized cartridge drive provides hard disk backup performance and reliability. Many times faster than either floppies or tape, it also provides the versatility to handle program entry, data storage and can function as a system disk. Overall, the 5¼" Winchester/cartridge disk combination gives system-level performance which exceeds multiple RL02's in many applications.

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Space-saving SABRE is 5¼" high, slips into any standard 19" Retma enclosure and comes complete with power supply, host adapter and connecting cables. It needs one-eighth the space and draws one-quarter of the power of four RL02's. Further, SABRE slashes hardware and installation costs by eliminating the need for a separate system bootstrap, bus terminator and clock control board.

For more information on SABRE or any of the high-quality Emulex communications, disk, tape and packaged subsystem products, call toll-free (800) 854-7112. In California (714) 662-5600.

SABRE's Features

Size	Compact 5¼" height x 19" width package contains 31.2 MB (3x RL02) 5¼" Winchester disk and 10.4 MB (1x RL02) removable 8" cartridge disk.
Capacity	Equivalent to four (4) DEC RL02's.
Speed	Overall performance significantly increased over tape and floppies, especially in throughput and backup time.
Transparency	Runs standard RL02 diagnostics and operating software.
Flexibility	Removable cartridge disk; SCSI Bus interface allows up to five (5) I/O devices; single-board host adapter.
Reliability/Durability	Winchester technology; ruggedized cartridge disk construction; shock mounts; hermetically sealed HDA for protection against contamination.
Price/Performance	Lower cost per box and per MB in virtually all applications.

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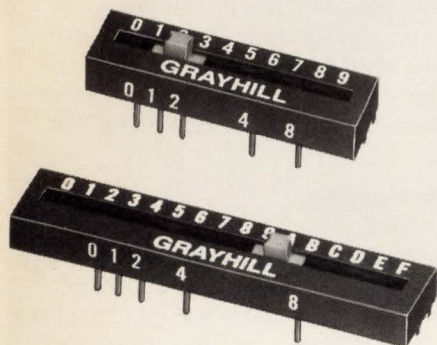


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CIRCLE 33

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Linear Action; 10 or 16 station

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Other linear action models include 10 or 16 station tap switches with common bus; and 10 or 16 station switches that selectively close adjacent contact pairs.

Like all Grayhill DIP Switches, these new linear action models are available off the shelf from the factory or from your Grayhill distributor. Call or write for your FREE catalog of DIP Switch specifications and prices.



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CIRCLE 34

Method cuts dropouts on flexible media

A successful error correction system for magnetic media must allow recovery from the temporary signal loss that results from physical dropouts. Problems of error recovery when dealing with flexible media are more severe than those encountered with rigid media. While there are techniques that adequately handle the errors typical of disk packs, flexible disks and magnetic tapes are potentially more susceptible to substantial data losses.

circle's diameter equals the width of the data track, total data loss occurs during a track length almost equal to the diameter. In fact, data loss occurs even when the dropout area occupies less than the full track width. Whenever it is large enough so that the read threshold level for the track cannot be reached, total data loss is experienced.

Read threshold levels are typically about 20 percent. Therefore, a dropout that is 80 percent of track width or wider, causes a total loss of data

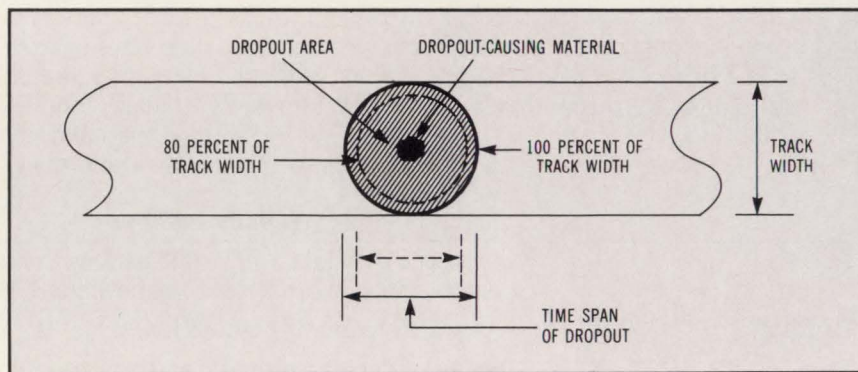
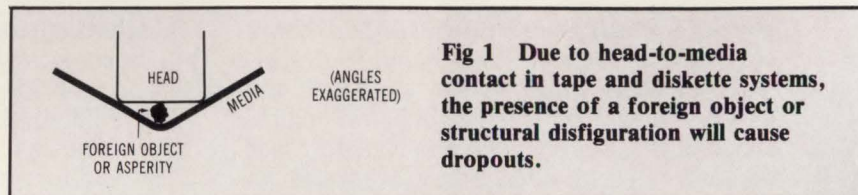


Fig 2 Because read threshold levels are about 20 percent of track width, any dropout that blocks 80 percent of the track will cause a total data loss.

One system, used with the 3M HCD-75 tape cartridge, however, ensures that no more than 1 in 2.75 million data blocks will have an unrecoverable error. The system corrects errors caused by both permanent physical aberrations and those resulting from transient conditions.

Usually caused by contamination, or in some instances, surface asperities generated during manufacture (Fig 1), dropouts are involved in at least 99 percent of media data loss occurrences. A major cause in tape and diskette systems is the presence of a foreign object or structural disfiguration that destroys the necessary head to media contact.

Forcing the media away from the head, the asperity creates a circular area that is too far from the head for adequate data recording. If the

for a track length equal to the 80 percent or more diameter (Fig 2). Dropouts even a minute amount larger than this threshold-crossing value cause a data loss. For example, in a 10,000-bit/in. system having a read-head track width of 0.009 in., a dropout equal to the track width will cause a loss of more than 50 bits. However, data losses of 100 bits or more are typical. While a great deal has been written about Fire and Hamming codes, and others with similar algorithms, these codes usually have an error correcting limit of 11 adjacent bits. This makes them unsuitable for use in correcting flexible media dropouts.

Total redundancy—recording all data twice—wastes storage space and recording time, but could nonetheless

(continued on page 64)

INTRODUCING LARGE-DISK PERFORMANCE IN DRIVES HALF THE SIZE

MODEL 9715 FSD. With 160 Mbytes in a sealed module, you get the same capacity, speed and performance as the CDC® Mini Module Drive (MMD) in a unit one-half the size.

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CIRCLE 35

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Require durable, custom-spec, EMI/RFI tested cable

Must be compatible with all IEEE 802 networks

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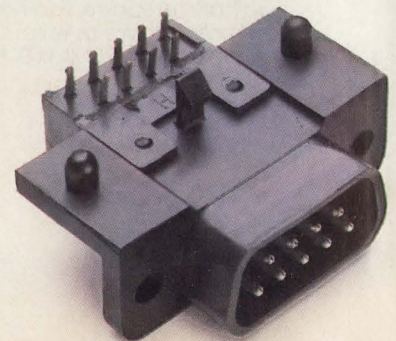
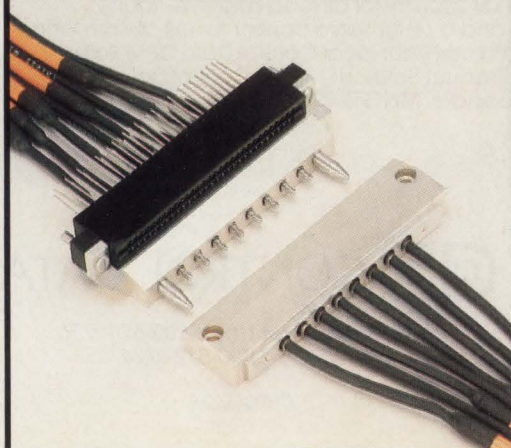
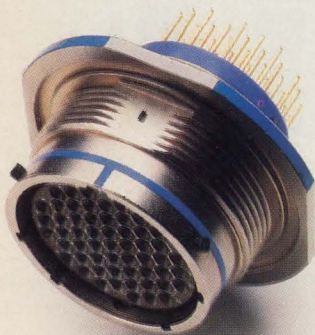
Need cable-end terminator for system impedance balance

Terminate with type N

PC Circular Connector

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For CATV, we developed a modular eight-channel fibre optic connector that mounts directly on a PC board. It takes the place of eight separate optical connectors with less space and complexity—but no loss in performance.

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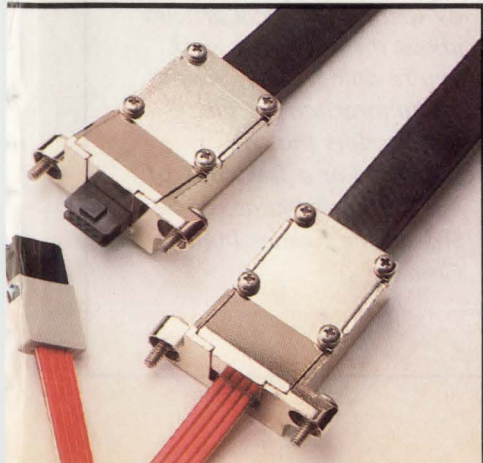
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CIRCLE 36

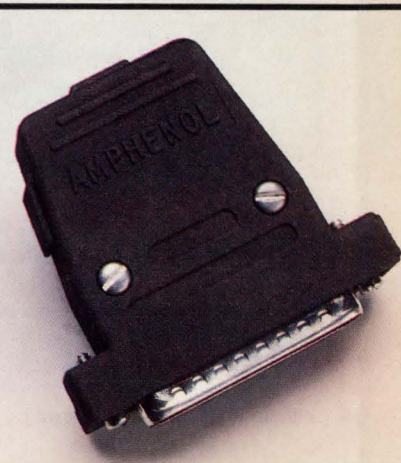
Planar Coax Interconnect Harness



Filtered Ribbon Connectors



Shielded D-Subminiature Connector





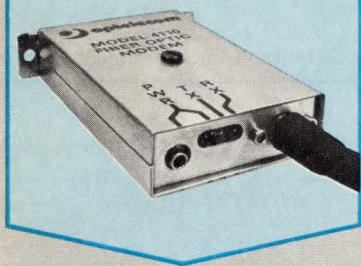
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CIRCLE 37

Method cuts dropouts
(continued from page 60)

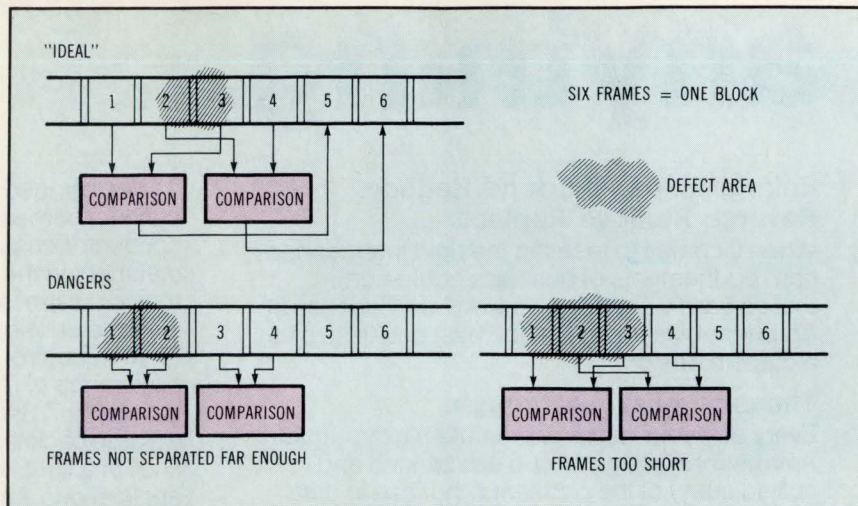


Fig 3 Too few or too many frames per data block can result in frames being destroyed.

ensure correct data retrieval. A more efficient system uses less than total redundancy, but still provides a high degree of error correction. Two basic principles govern the design of this error correction system. One is the finding that 50 percent redundancy provides a 1000-fold improvement in error reduction over a system with no error correction; the other is packet size limitation—the increment checked against itself for errors.

The 50 percent redundancy technique compares (during writing) two physically separated data frames, bit by bit, and generates a parity frame which records that bit by bit comparison. A parity system may generate a "1" if the compared bits are identical, and a "0" if they are opposite. Generating this extra frame creates 50 percent redundancy. If each incremental data block comprises too few frames, a dropout (typically 0.012 in.) could destroy not only one data frame, but the one to which it is to be compared (not physically distant enough). The same danger exists if the frame size is much smaller than the prevalent dropout size (Fig 3).

At the other extreme, if the block comprises too many data frames, the electronic storage system will be impractically large and cumbersome, since each frame must be temporarily stored. Blocks within the HCD-75 system are made up of six frames with 256 bytes of data each: four for data storage and two for parity patterns.

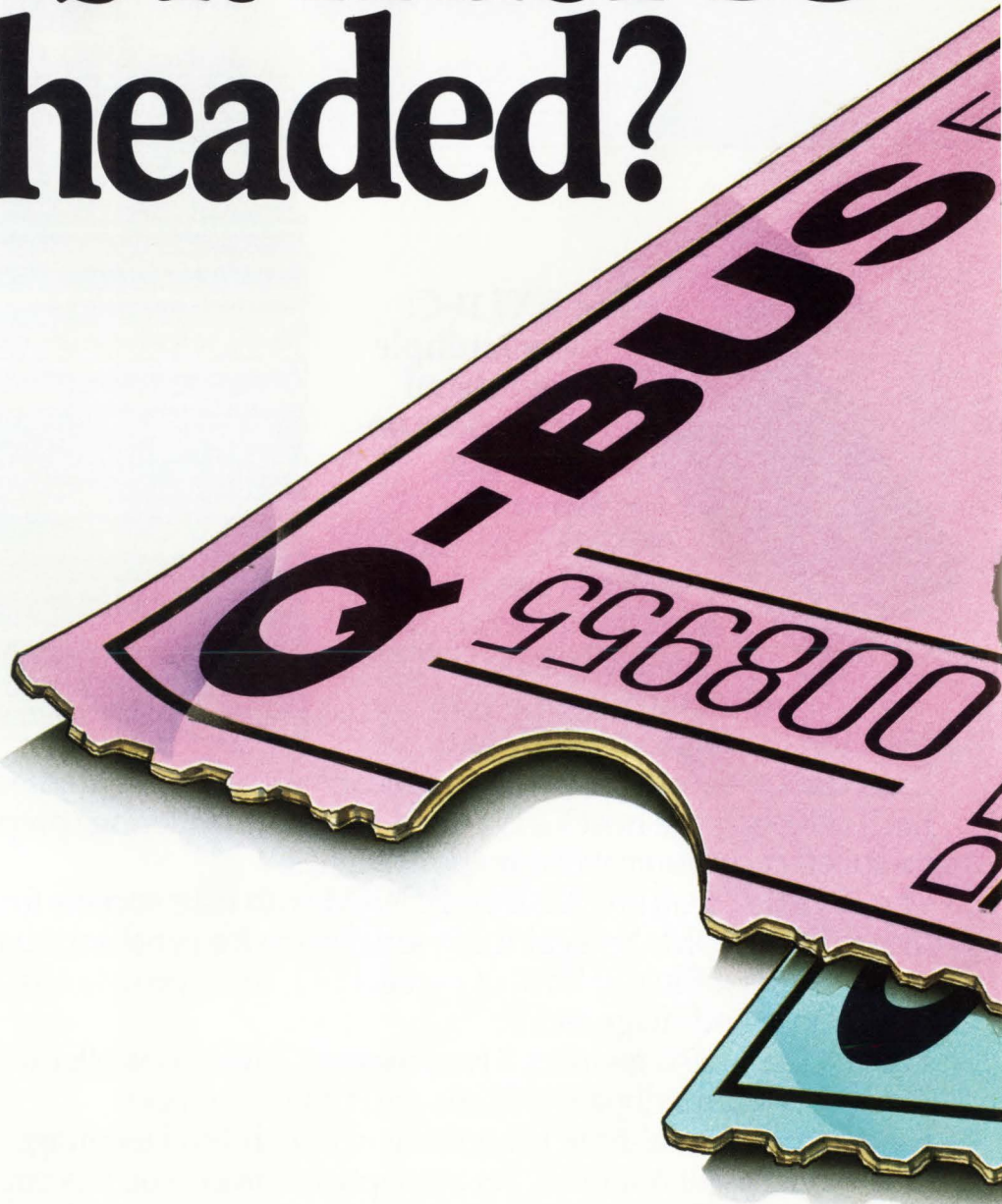
The maximum distance between compared frames is 1024 bytes. Thus, it is possible to destroy two contiguous frames without causing an uncorrectable error.

The system, therefore, is vulnerable only when two dropout-causing defects are so close together that two of the three frames involved in a specific error correction comparison are destroyed. Unless this happens, the system is totally transparent to the user, in contrast to most current "streamer" designs. 3M, PO Box 33600, St Paul, MN 55133.

Circle 243

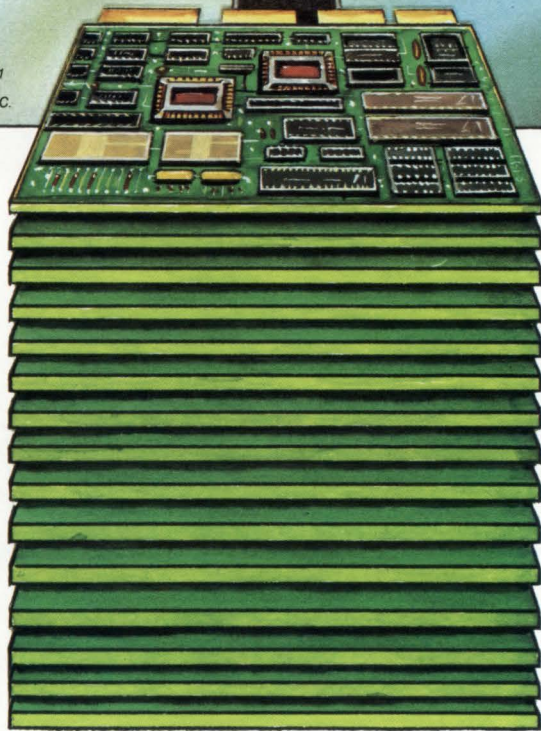
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Up to 14
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application throughput on Q-Bus.

Each can be task dedicated so applications can be segmented for efficiency. Each off-loads the host CPU of real-time data buffering, preprocessing and high-speed communications responsibilities.

The KXT11-C features 32Kb static RAM with user sockets for an additional 16Kb RAM or 32Kb ROM. You get three serial ports for synchronous/asynchronous design flexibility. Plus 20 lines of parallel I/O, three programmable interval timers, onboard boot and diagnostics.

The KXT11-C also features a two-channel DMA controller for high-speed data transfers between onboard devices and Q-Bus memory.

For concurrent real-time processing in a high-level language, the KXT11-C runs MicroPower/Pascal onboard. As a peripheral processor, it is supported under RT-11, RSX-11M, RSX-11M-PLUS and MicroPower/Pascal executing on the Q-Bus master CPU.

The intelligent new KXT11-C: An easy way to give your application an instant performance boost by consolidating I/O processing.

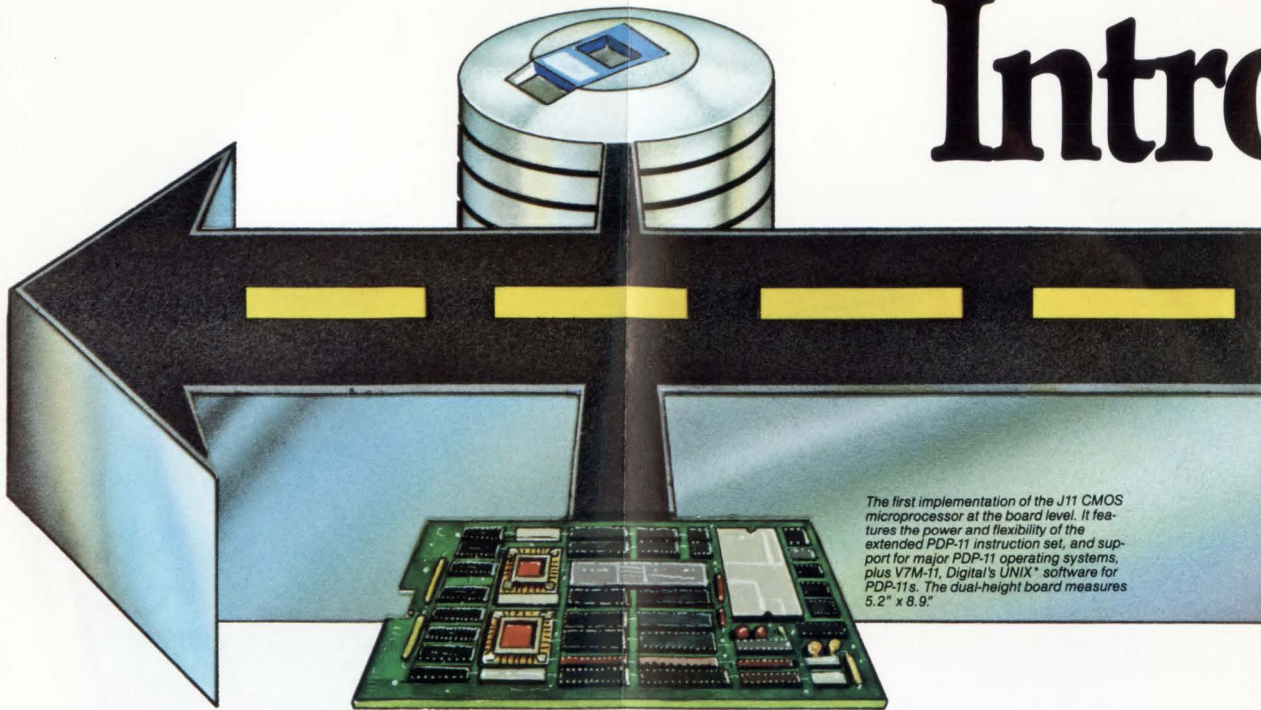
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LSI-III/73=PDP11/44 ON A BOARD

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Intro



The first implementation of the J11 CMOS microprocessor at the board level. It features the power and flexibility of the extended PDP-11 instruction set, and support for major PDP-11 operating systems, plus V7M-11, Digital's UNIX software for PDP-11s. The dual-height board measures 5.2" x 8.9".*

Introducing the LSI-11/73: PDP-11/44 CPU class performance on a single board. The LSI-11/73 has been designed to give you four times the processing power of the LSI-11/23.

Its J11 microprocessor features integral floating point, memory addressing up to 4 million bytes, sophisticated memory management, separate I & D space with kernel, supervisor and user modes.

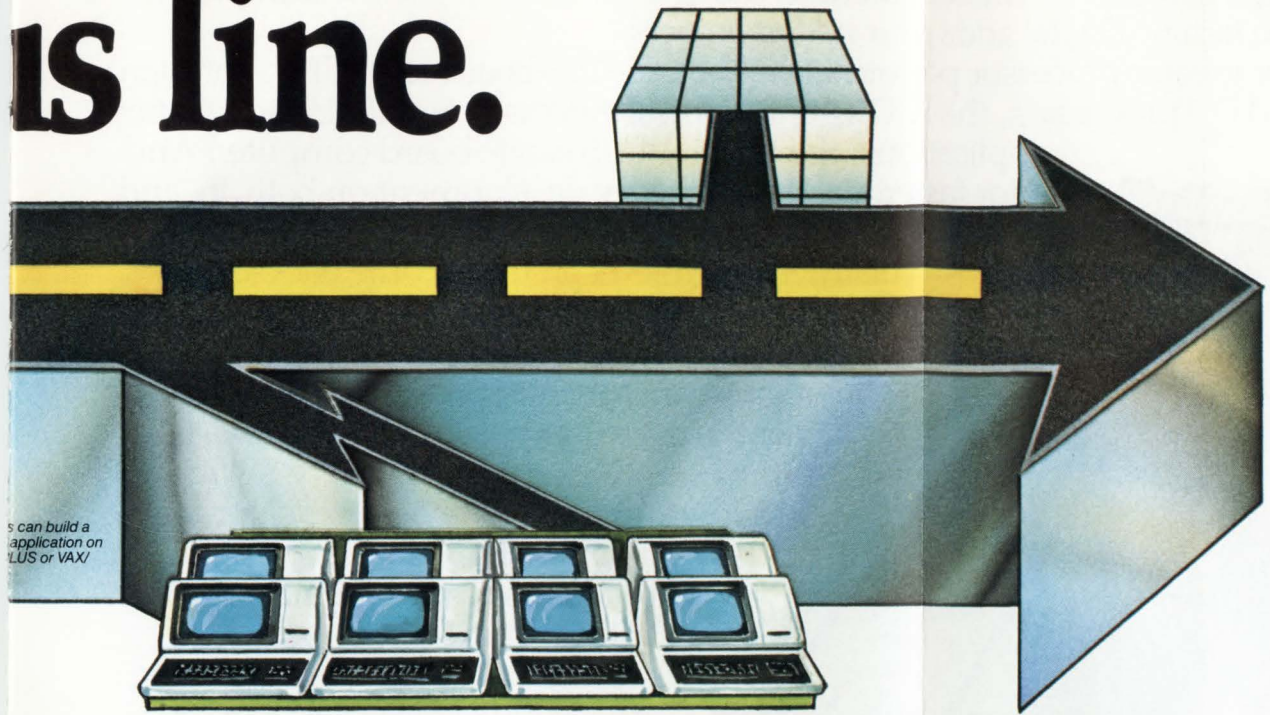
Featuring 8Kb of high-speed cache memory, the LSI-11/73 reduces execution times in many applications up to 60%. An onboard Q-Bus interface allows you to customize your configuration by selecting from hundreds of Q-Bus options available from Digital and third parties.

The LSI-11/73 supports Digital's popular PDP-11 operating systems—RT-11, RSX-11M, RSX-11M-PLUS, RSTS/E and MicroPower/Pascal software—plus V7M-11, Digital's UNIX* software for PDP-11s. This protects your investment in applications software as you migrate from existing Q-Bus processors.

The LSI-11/73: Digital's new high performance processor on the Q-Bus.



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MicroPower/Pascal is an advanced software toolkit that's a combination operating system and highly-structured programming language. It lets you optimize your Q-Bus configuration to implement real-time control, and features a globally optimizing compiler that generates code as efficient as many assembly languages.

With MicroPower/Pascal, programmers can build a runtime, ROMable application with an extended version of Pascal that supports concurrent real-time programming, process synchronization, and device register accessing.

Working independently on a single PDP-11 or VAX/VMS system, each programmer develops a portion of the target solution. These software modules are then compiled separately and linked to a customized kernel using special MicroPower utilities running under the host operating system. Debugging, in original Pascal terms, is also accomplished from the host system.

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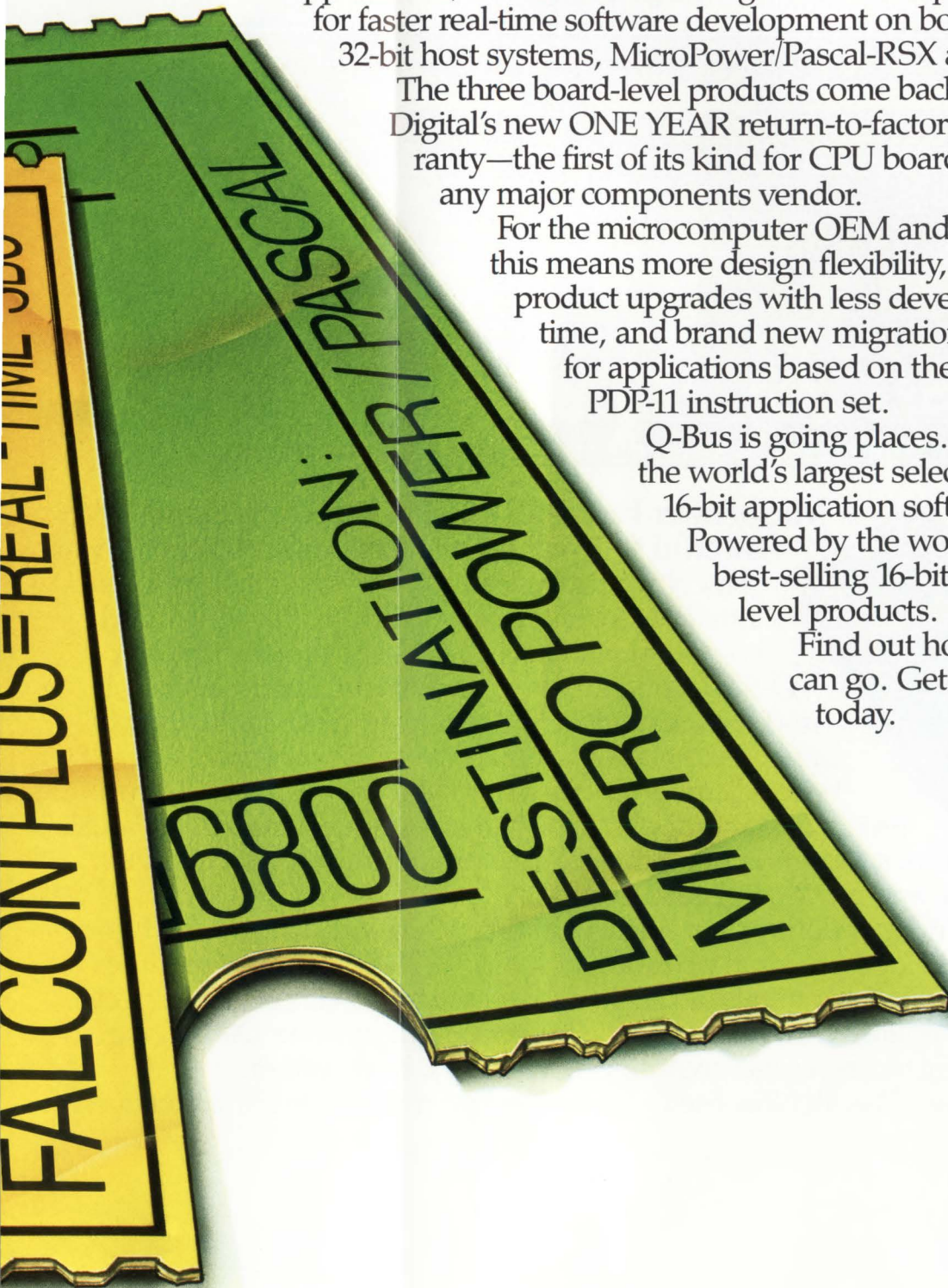
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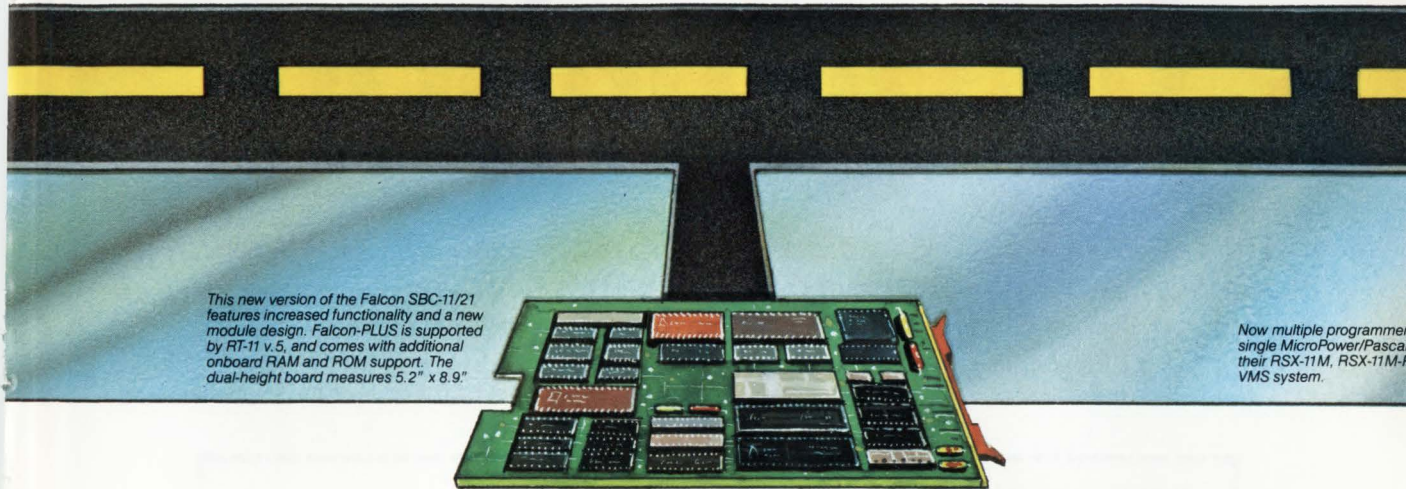
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This new version of the Falcon SBC-11/21 features increased functionality and a new module design. Falcon-PLUS is supported by RT-11 v.5, and comes with additional onboard RAM and ROM support. The dual-height board measures 5.2" x 8.9"

Now multiple programmed single MicroPower/Pascal, their RSX-11M, RSX-11M-VMS system.



Falcon-Plus: The industry's smallest 16-bit SBC is now supported by RT-11. Featuring Digital's T11 microprocessor and PDP-11 instruction set, the new Falcon-PLUS is a compact, powerful tool for an even greater variety of ROM- and RAM-based dedicated computing applications. And it's cost-effective with either.

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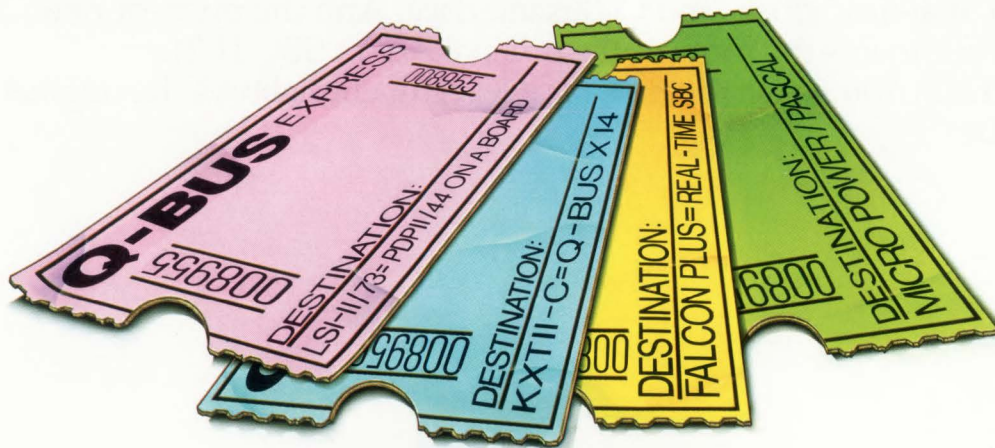
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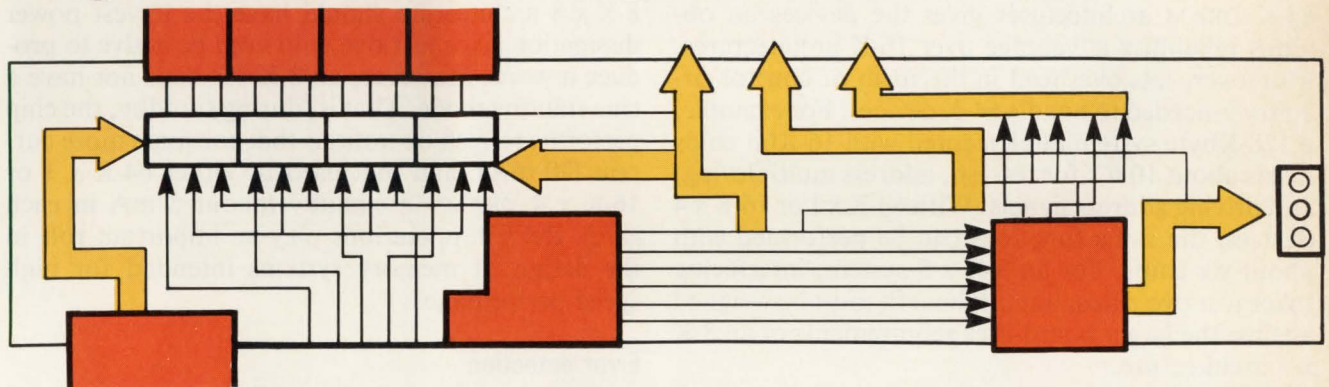
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MATCH DRAM ORGANIZATION TO MEMORY REQUIREMENTS

Differing architectures of 64-Kbit dynamic RAMs permit designers to optimize the design of memory systems.



by David W. Gulley

The arrival of 64-Kbit dynamic RAMs in a variety of chip architectures has put computer system memory design in a new light. For the first time, memory designers will be able to choose chip architectures best suited to important memory system parameters. Such parameters include chip count, board space, power consumption, error detection and correction capability, and others. Designers will find that small-capacity memories—64 Kbytes or less—call for DRAM architectural features that prove unsuitable in memory boards of 0.5 Mbytes or greater.

The current crop of 64-K DRAM chips is organized in four different architectures: 64-K x 1, 16-K x 4, 8-K x 8, and multiport. Of these, the 64-K x 1 (eg, TMS4164) stands out as the most popular since it fits the same 16-pin socket as the widely used industry standard 16-K x 1 DRAM.

Less well known is the 16-K x 4 architecture (eg, TMS4416), but this DRAM's potential is rising as designers begin to appreciate the benefits of a 4-bit

output in high-performance memory applications. A 1-byte output makes the 8-K x 8 architecturally attractive for small-capacity memory/microprocessor designs, but an assortment of packaging, power and control constraints could relegate this device to a secondary role in the 64-K DRAM hierarchy.

The multiport memory (eg, TMS4161) is configured as a 64-K x 1 array with an added 256-Kbit serial port to allow random access and serial access functions simultaneously. This device is attractive in high resolution graphics systems, communication systems, and any other systems where processors access to the memory is needed while transferring data to another device.

Trade-offs in DRAM architectures

Those DRAMs organized as 64-K x 1 permit the densest packaging of any 64-K architecture. While 16-K x 4 devices store the same number of bits/package as 64-K x 1s, they are housed in 18-pin dual inline packages (DIPs) to accommodate the 4-bit output. Thus, a 64-Kbyte memory built with 16-K x 4s sits on a board area of 4.0 in², slightly larger than the 64-K x 1's 3.6 in². Because of their 28-pin packaging, DRAMs organized as 8-K x 8 offer the least effective density. At 8.3 in², a 64-Kbyte system built with 8-K x 8s is more than twice as large as the same system using 16 x 4s. Fig 1 illustrates the three package outlines, while the Table compares the parameters of most interest to designers.

David W. Gulley is application engineering manager at Texas Instruments, Inc, 9901 S Wilcrest Dr, Houston, TX 77099, where he is responsible for MOS memory applications. He holds a BSEE from the Georgia Institute of Technology.

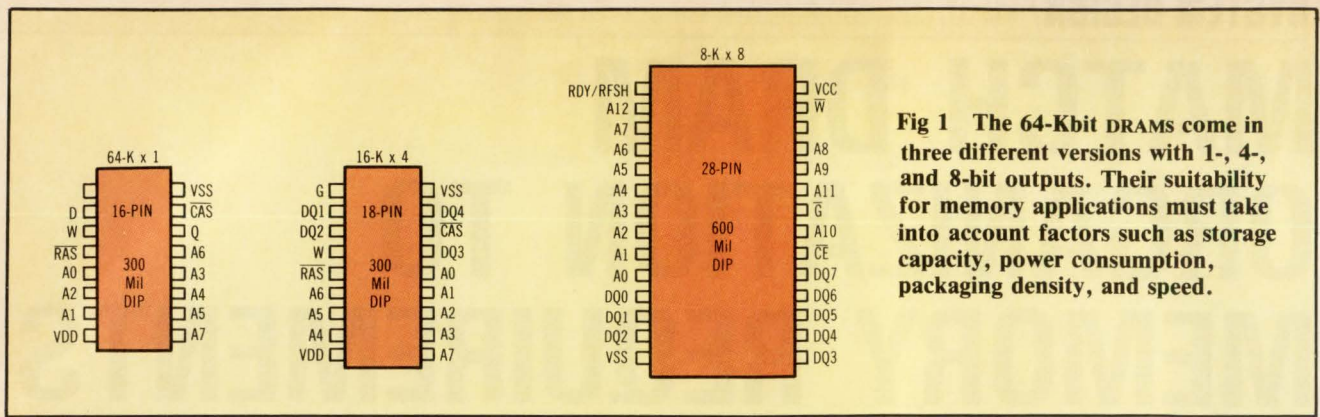


Fig 1 The 64-Kbit DRAMs come in three different versions with 1-, 4-, and 8-bit outputs. Their suitability for memory applications must take into account factors such as storage capacity, power consumption, packaging density, and speed.

Power consumption and reliability considerations go hand-in-hand in memory system design. The single 5-V supply operation and low chip count of 64-K DRAM architectures gives the devices an obvious reliability advantage over 16-K architectures. Moreover, less overhead in the form of control circuitry is needed to handle 64-K devices. For example, a 128-Kbyte system implemented with 16-Kbit chips needs about 10 ICs for refresh, address multiplexing, and driving address signals. With 64-K x 1 or 16-K x 4 devices, the same functions can be performed with about six chips. For an 8-K x 8 system, interfacing takes just two chips, but this benefit must be weighed against the larger board-area requirements of an 8-K x 8 architecture.

Within the 64-K hierarchy, an n x 1 organized device is more reliable than either an n x 4 or an n x 8. This occurs because a DRAM's output driver stage is the largest dissipating element on the chip. An n x 1 device contains one such driver, while an n x 4 chip has four drivers, and an n x 8 chip, eight drivers. In addition, an n x 8 device pays extra power/reliability penalties in the form of onboard address buffers which support the nonmultiplexed address operation. Further power/reliability degradation results from the inclusion of onboard refresh circuitry. Comparing 64-Kbyte memory systems implemented with the four different architectural types, the numbers come out as follows: 16-K x 1, 3.8 W; 64-K x 1, 1.4 W; 16-K x 4, 0.5 W; 8-K x 8, 0.8 W.

The 16-K x 4 design is the least power hungry, due to the chip's 4-bit wide output. If the memory system uses byte-size words, just two 16-K x 4 devices need be active at a time to produce a word; the remaining six devices can sit in the low power standby mode.

With 64-K x 1 DRAMs, all chips must be in the high power active mode to produce a word.

Based on this analysis, it would seem that the 8-K x 8 architecture should have the lowest power dissipation since just one chip need be active to produce a word. However, an 8-K x 8 does not have a true standby mode. That is, during standby, the chip performs refresh operations that consume more current (20 mA) than that used by either 64-K x 1 or 16-K x 4 DRAMs in standby (about 5 mA in each case). Refresh operations play an important role in the design of memory systems intended for high speed performance.

Error detection

One of the new design philosophies associated with 64-K DRAMs is the substitution of parity error checking for the more complex error detection and correction (EDAC) systems. The reason is that soft errors (such as those generated by alpha-particles) are not as prevalent in 64-K DRAMs as those based upon 16-K devices. Thus, parity can be used to detect the failure within a chip. In addition, the simplicity of parity checking schemes makes for less expensive boards than those equipped with EDAC.

To a great extent, the type of error checking technique used dictates the memory device architecture. In general, an n x 1 organized DRAM offers designers the greatest flexibility since it is adaptable to any number of error checking bits. By contrast, 4-bit devices become difficult to use in error checking schemes that employ bit lengths other than an integral multiple of 4 bits.

Typically, EDAC systems are found only in memories that employ a 16-bit or greater word length—ie,

Parameter Comparison			
	64-K x 1	16-K x 4	8-K x 8
Area at typical packing density (in. ²)	0.40	0.44	1.82
Relative area	1	1.1	4.5
Power active (500-ns cycle)	138 mW	150 mW	385 mW
Standby	27.5 mW	27.5 mW	82.5 mW
Cycle time (ns)	220-260-330	260-330	425-500
Access time (ns)	120-150-200	150-200	250-300



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large memories having capacities at least in hundreds of kilobytes. In a 16-bit system configured with $x 1$ devices—either 64-K $x 1$ or 16-K $x 1$ —the standard Hamming-code EDAC circuitry requires 6 error checking bits. These bits are added to the basic 16-bit word to give a total of 22 bits. Since 22 is not an integral multiple of 4, 4-bit wide DRAMs can be used only if bits are left unused, or if a combination of 4-bit and 1-bit wide devices are used together.

Unfortunately, the Hamming code cannot provide error detection or correction in a wide word system if an entire chip fails, since multiple bits are in error. For wide word DRAMs, an EDAC scheme that detects

The various 64-K architectures have brought about a new concept in memory technology called granularity.

the failure of an entire chip works better. This scheme, called a modified fire code, provides EDAC in 4-bit bursts. However, it requires 8 check bits to a 32-bit word, using $x 4$ devices, and involves more overhead circuitry for implementation. The situation for 8-K $x 8$ devices is even worse—EDAC requires an additional 12 check bits, resulting in complex, costly implementation.

The most practical approach to error detection (not correction) with 64-K DRAM architectures is

parity. Since just one extra bit is needed, it is simple to implement. Any 1-bit wide DRAM operates easily with a parity scheme; 4-bit devices can also use it when they are intermixed with an $x 1$. In fact, the 16-K $x 4$ package configuration with 18 pins permits the addition of a single 64-Kbyte $x 1$ DRAM to systems for parity implementation.

Surveying granularity

The various 64-K architectures have brought about a new concept in memory technology called granularity. The term refers to the smallest increment of memory that must be added to a system to increase its storage capacity. The degree of granularity depends entirely on DRAM architecture.

For example, assume that a 64-Kbyte memory system is built with 64-K $x 1$ DRAMs and uses an 8-bit data word. Such a system needs eight DRAMs for its storage requirements. Now assume that the original storage capacity must be increased to meet a new application. Because of the $x 1$ architecture, the system requires eight additional DRAMs (64 Kbytes) that increase its storage capacity to 128 Kbytes, thereby doubling its capacity. In many cases, small memories of this type need only 16- or 32-Kbyte expansion increments, but because of the $x 1$ architecture, a designer must add the entire 64 Kbytes. This is an example of coarse granularity, and gives designers little flexibility.

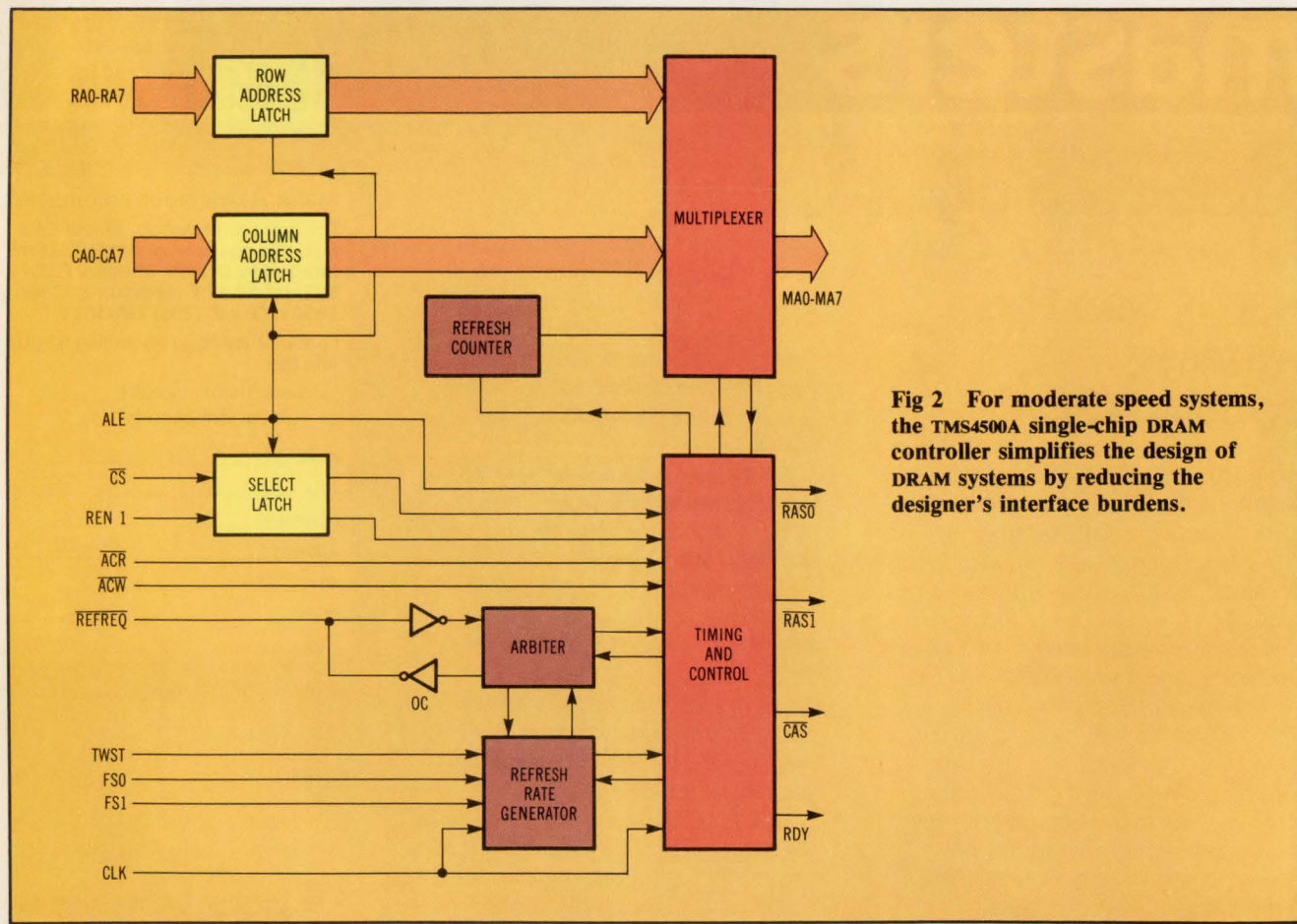
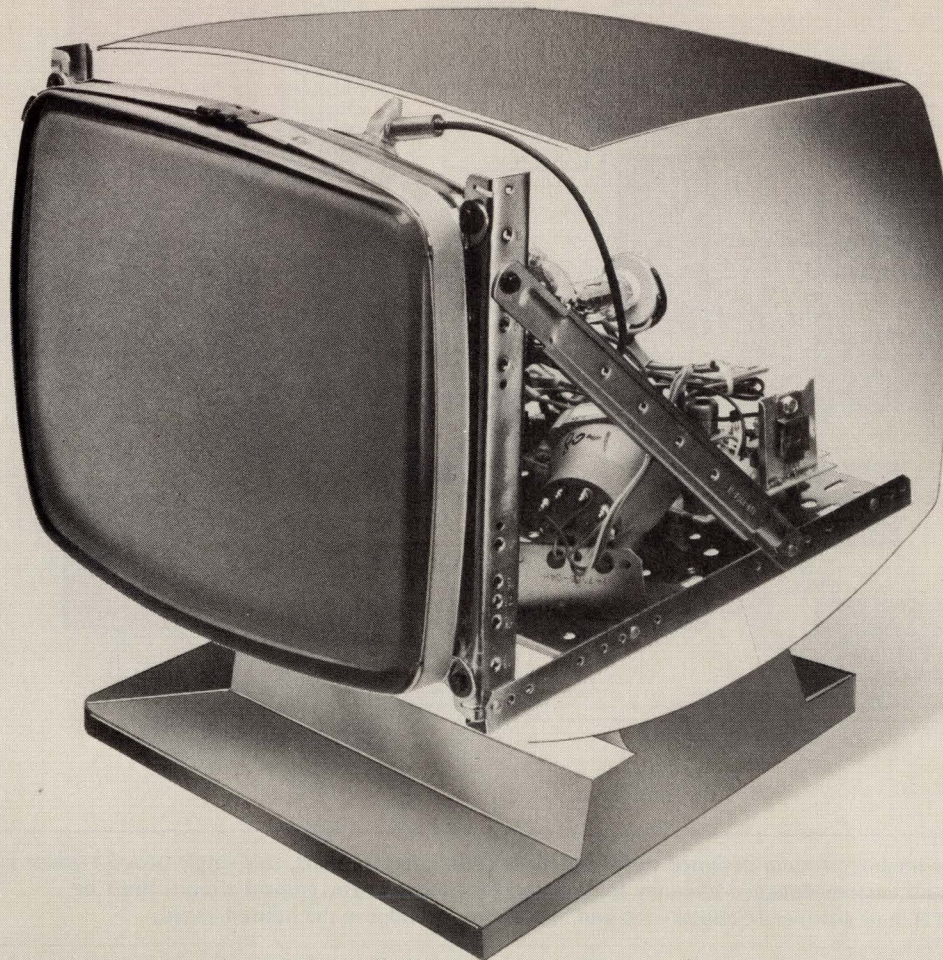


Fig 2 For moderate speed systems, the TMS4500A single-chip DRAM controller simplifies the design of DRAM systems by reducing the designer's interface burdens.

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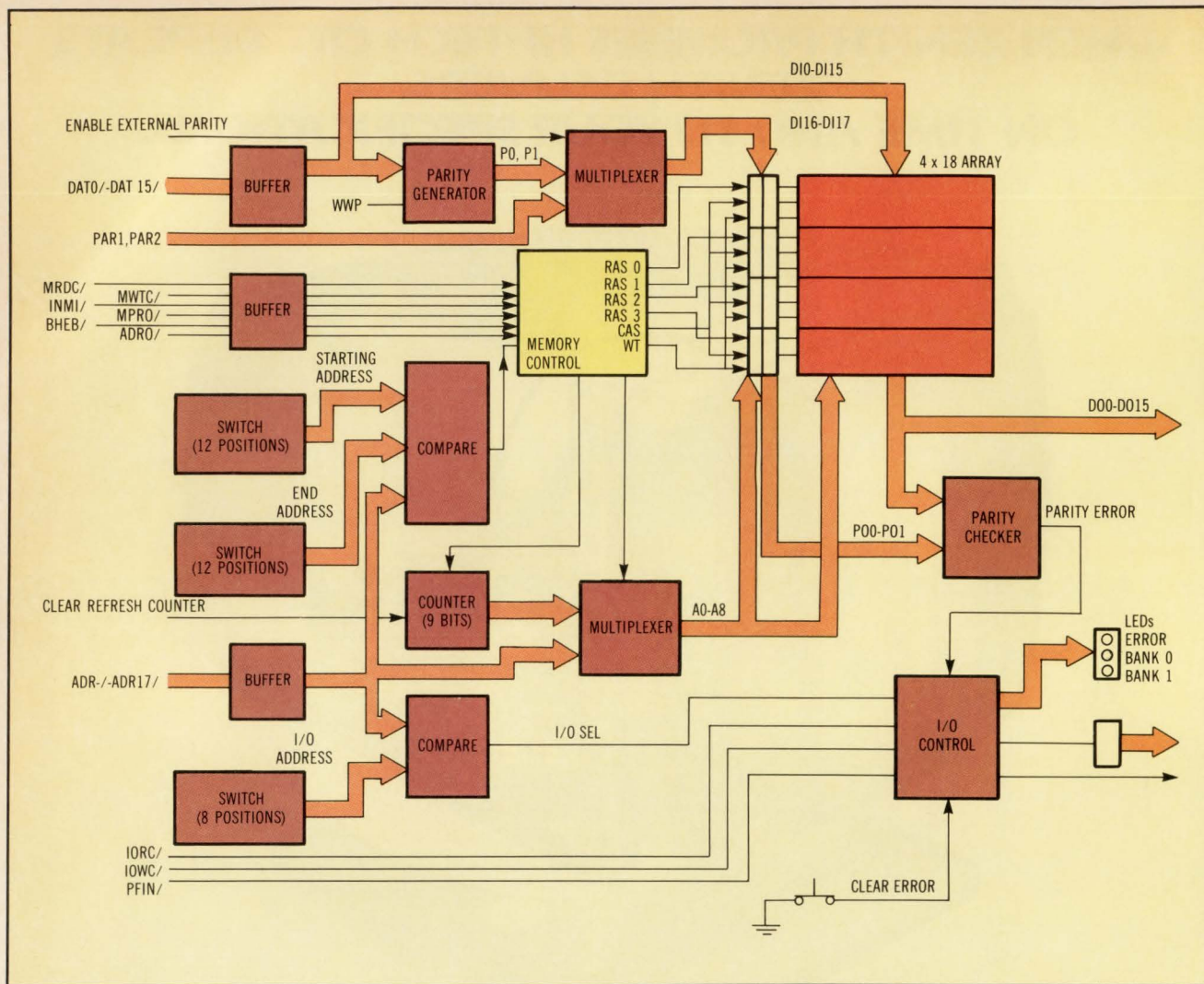


Fig 3 A 512-Kbyte memory system designed to interface with the Intel Multibus, this single-board TM40020 uses high speed DRAMs and custom-designed circuitry for the control function. The control circuits must be implemented with TTL and advanced-Schottky ssi and MSI devices to achieve the desired speed.

Assume that the same size memory, built with 16-K x 4 DRAMs, must also be expanded. With 4-bit wide DRAMs, just two chips need be added to the memory since they provide a complete word (8 bits). The two devices contain 16 Kbytes of storage; thus, the architecture granularity is four times finer than the 64-K x 1's 64 Kbytes. Using 16-K x 4s, designers can increment a small capacity memory with significantly more flexibility than with 64-K x 1s.

From these two examples, it is obvious that 8-K x 8 architecture offers the finest granularity. Just a single chip can be added to the example system to increase its capacity by 8 Kbytes. Considering only memory expansion capabilities, x 4 and x 8 devices are most applicable to small capacity systems. Large capacity systems are usually equipped with x 1s since granularity is not as important, and also because they are simpler to use in parity error checking schemes.

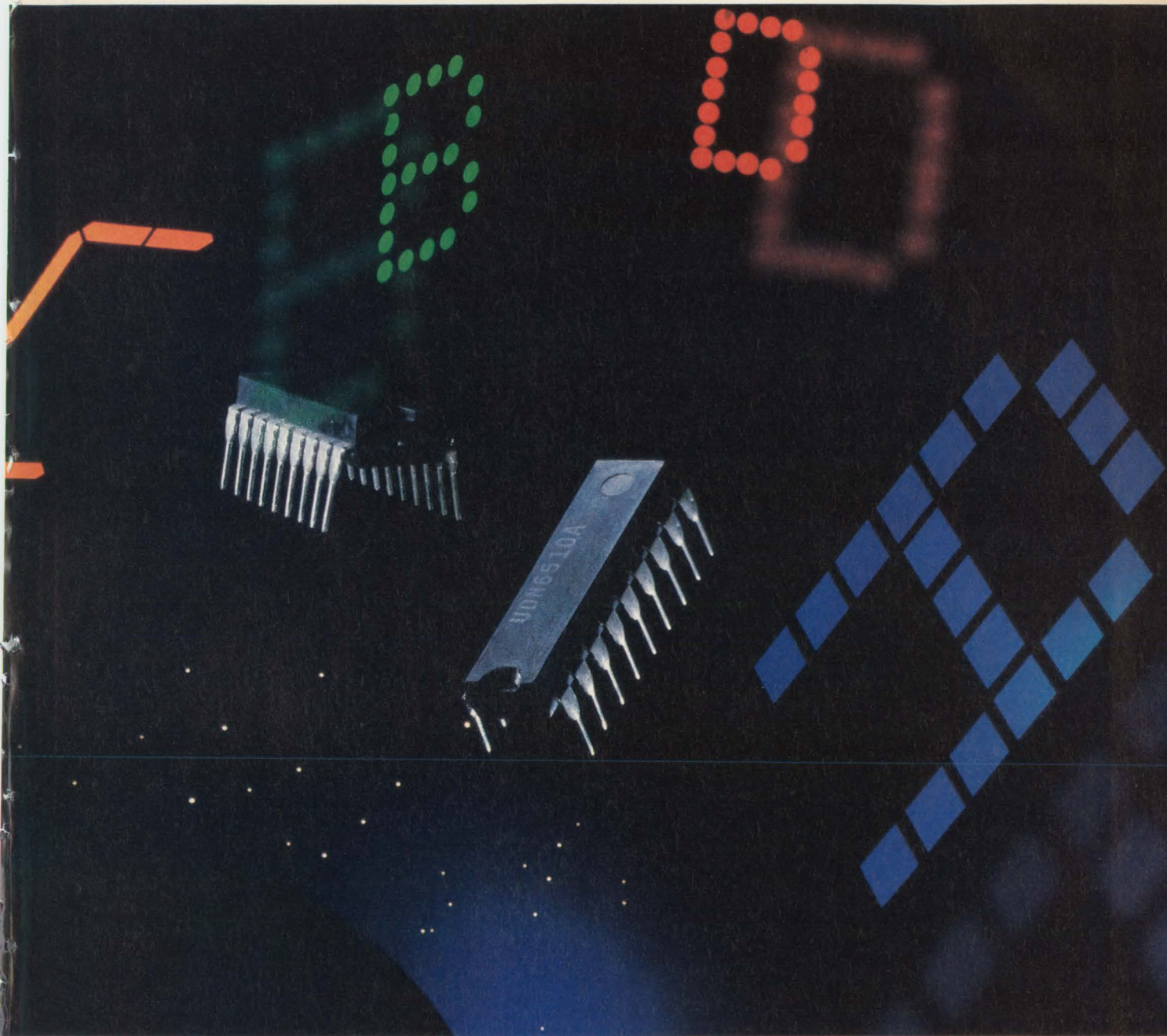
Control and speed

The type of control system selected for a dynamic memory depends heavily on the required operating

speed. For medium speed systems, a single-chip controller such as TI's TMS4500A (Fig 2) makes designing simpler because the chip solves many of the common DRAM interfacing problems. For example, this chip takes care of address multiplexing, cycle timing, and refreshing for any type of multiplexed-address DRAM. It operates directly from the system clock and needs no external crystals, RC timing circuits, or delay lines. Refresh-access arbitration is handled synchronously with the system clock to eliminate the arbitration delays and metastability problems often associated with asynchronous operation.

To design a memory system for high speed operation, it becomes necessary to design custom control logic using TTL devices or a mixture of TTL and advanced Schottky chips. One such design, shown in Fig 3, is TI's TM40020 memory board, intended for add-in memory applications on the Intel Multibus. Designed to provide 12 Kbytes of storage, the board contains TI's TMS4164-15 64-K x 1 DRAMs. This timing chain not only operates with 150-ns DRAMs, it accepts faster chips to meet the needs of higher speed

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computer applications. Moreover, the TM40020 can be upgraded to employ the coming generation of 256-Kbit DRAMs.

An important system-level consideration in large storage applications is the suitability of the memory management system. These are usually required in

For high resolution graphics, sixteen 64-K type devices would be required to store one picture plane.

multi-user environments in which the processor executes one user's task for a specific time period and then switches to the task of another user or process. Rather than completely reloading programs from the backup storage (disk) on each task-switch, the management system uses a paging scheme to bring the necessary data into main memory (DRAM) for the second task.

From the designer's standpoint, memory management systems degrade access time because the management system is, in effect, a fast RAM connected between the processor address and memory address lines. Simply inserting a device exacts a speed penalty of 20 to 80 ns. One way to compensate for this delay is to design the memory so that memory blocks correspond to the DRAM physical storage capacity.

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For example, memory can be partitioned in 4-, 8-, or 16-K boundaries to permit small groups of DRAMs to receive data coming in from the disk.

Memory systems need not be slowed down by the memory management system. On the contrary, a memory can be accelerated by using a cache, a small fast buffer located between the processor and main memory. As long as the processor executes out of the cache, accesses take place at full speed. But when a cache is used, it is usually small—about 8 to 16 Kbytes—to prevent adding extra power consumption and cost to the system. More importantly, a cache must be supported by an effective algorithm for swapping data between itself and the main memory.

Speedy systems

For systems that require high storage capacity, x 1 architecture is preferred for its packaging density and ability to operate simply with parity error detection schemes. But if high performance is the criterion, 4-bit wide devices are more suitable because of their inherent speed advantage in system operation. A typical example would be a system for servicing a video display terminal with dot-addressable graphics. If the display has medium resolution graphics (640 x 512 pixels), all the bits required to display data can be stored in five 16-K x 4 DRAMs.

Video systems need DRAM devices with sufficient speed to produce a cycle time which can update the display within the required time. In most cases, 64-K x 1 DRAMs cannot be cycled fast enough to obtain the desired bit rate. The 4-bit output of 16-K x 4 devices not only provides the necessary bit rate, but the memory can also perform other system functions.

For high resolution graphics (1024 x 1024 pixels), sixteen 64-K type devices would be required to store one picture plane. Multiport memory use would allow data updated on the screen to be shifted out of the serial port while a processor draws a new image to the random access port. None of the other 64-K DRAM architectures allow such a sharing of the memory array with the bandwidth of the multiport memory. Each of the four architectures has specific advantages and disadvantages for a given system, but the choice of which features to use is now at the system designer's discretion.

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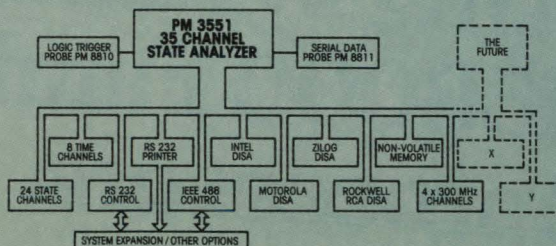
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CIRCLE 43



FACT NO. 3:

**80% of the
microcomputers
running UNIX[™]
and UNIX-derived
operating systems
use M68000 Family
microprocessors.**

And Motorola is the first microprocessor house to deliver System V.

Decision-makers have made the M68000 Family first choice for microcomputers running UNIX-like operating systems. The 32-bit architecture with large linear address space and regular, orthogonal instruction set make M68000 MPUs ideal for UNIX.

Research reveals that 80% of current microcomputers running UNIX or UNIX-derived operating systems use a '68000 MPU. A study by the independent Los Altos, California research organization, Yates Ventures, confirmed that the M68000 is the present microprocessor of choice in the UNIX field.

As the de facto standard for UNIX users, M68000 microprocessors become a principal asset in helping you stay abreast or ahead of the growing number of your competitors who are opting for this user-friendly operating system.

When the Bell System decided to enter the microcomputer software marketplace with UNIX, it was logical that Motorola would be selected among the first to begin joint development with Western Electric of a product derived from System V.

System V/68™ derived from UNIX System V, M68000 version, is the first System V operating system delivered by any merchant-market microprocessor house, bringing it under a common roof with the leading MPU for its use.

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Designed for high-level languages.

It's true, too, that years ago the M68000 family was designed to reduce your software development time, optimize code and hold your software costs in check by special attention to high-level language programming.

It follows that System V/68 will be available with an extensive set of programming languages, including C, FORTRAN, BASIC and Pascal, to carry these advantages forward.

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The kind of standardization System V/68 makes possible also ensures that a broad complement of support and applications software will be generated by independent vendors and systems integrators.

A strong M68000 software base.

The combination of this UNIX operating system and the M68000 Family is, in itself, a significant force in the microprocessor selection process. However, don't overlook the strong software base provided by the substantial array of Motorola M68000 software products already in place.

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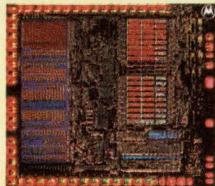
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When we last counted, we knew of more than 100 producers supplying independently-written M68000 software including everything from operating systems to languages and applications. The number continues to swell, and there are still others we don't yet know of.

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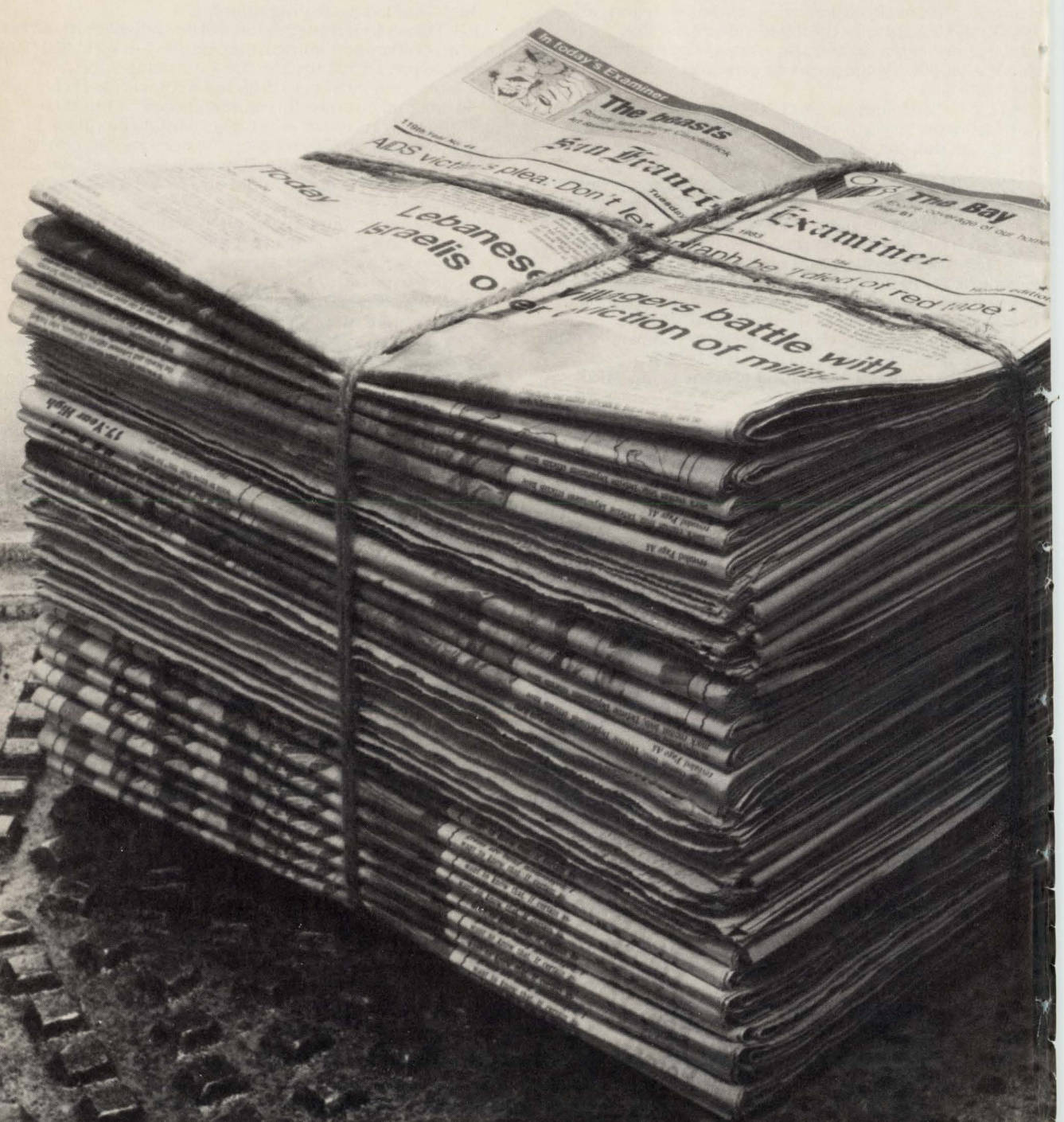
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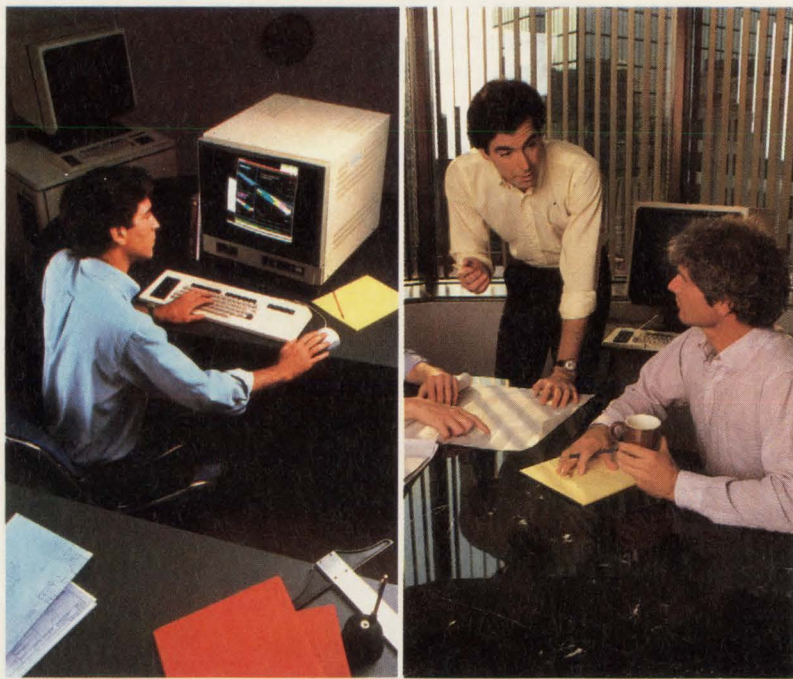
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CIRCLE 44

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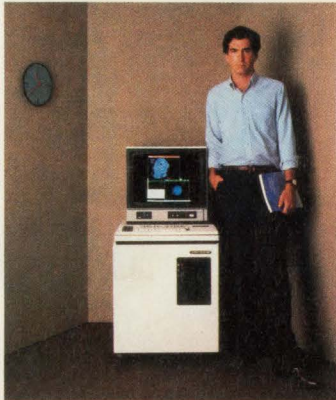
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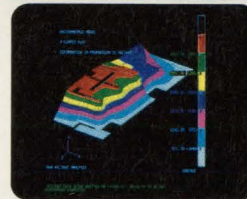
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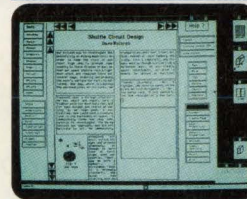
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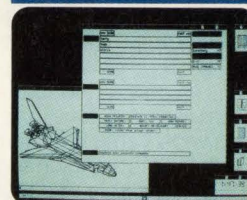
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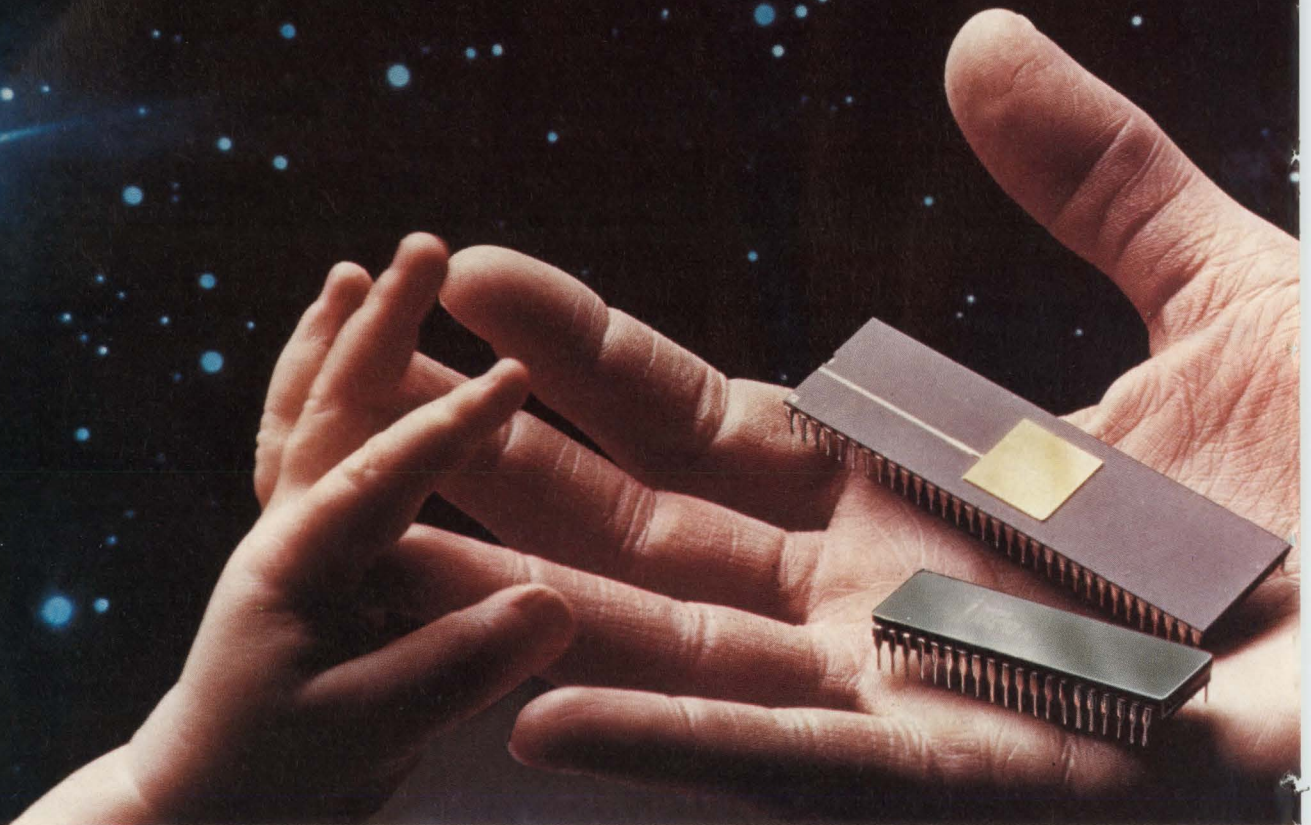
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CIRCLE 46

GRAPHICS SOFTWARE STANDARDS PROMOTE DEVICE INDEPENDENCE

Proposed standards permit software development independent of specific graphics hardware, as in this example of printer control.

by Paul Caron,
John Gray, and
Harold Schofield

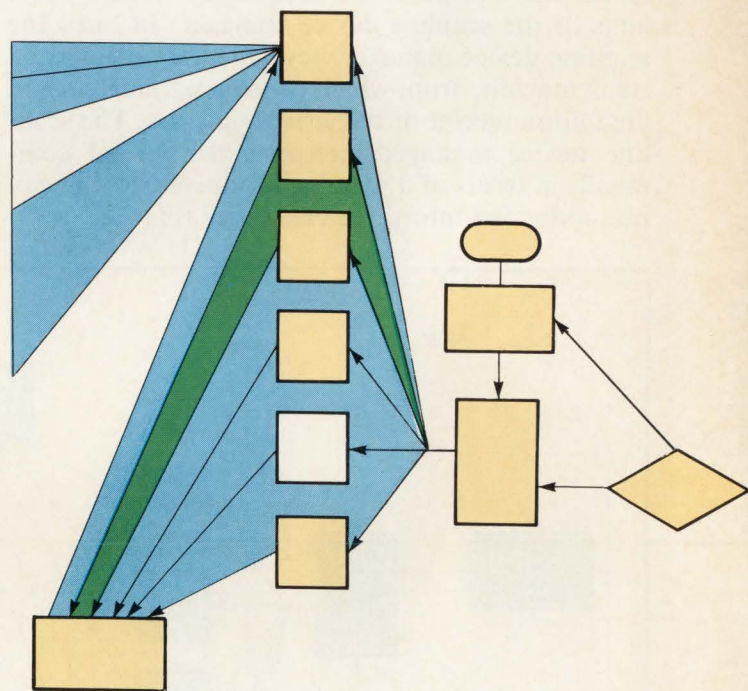
Device independent software standards have been proposed for graphics systems. This software, however, requires device managers to map application program requirements into display drivers. As a demonstration, a device manager was written for a scanline device in a thermal printer. It permits full vector graphics in 2 Kbytes of user-resident memory and allows users to tailor their data memory requirements. More importantly, it shows the feasibility of device independent graphics software for smaller systems.

This software is consistent with the Core graphics system proposed by the Graphics Standards Committee of the Association for Computing Machinery (ACM) Special Interest Group on Computer Graphics (SIGGRAPH). The device manager software, implemented on a microprocessor, controls

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John Gray is a professor of electrical and computer engineering and computer and information sciences at SMU. Mr Gray holds a BSEE from the University of Nebraska, an MSEE from New York University, and a PhD from Ohio State University.

Harold Schofield is design engineering manager at Gulton Industries, Inc, Gulton Industrial Pk, East Greenwich, RI 02818. Mr Schofield holds a BSEE from SMU.



the scanline device. (Scanline devices generate raster images, one scanline at a time, maintaining no frame buffer). This device manager functions between a virtual device interface (VDI) and the physical device interface (PDI). It interprets virtual instructions (opcodes and operands) passed to the VDI and passes specific device driver commands to the PDI.

In addition, it creates and maintains a record of the current picture to be displayed, which is called a virtual device metafile (VDM). This record contains the state of the picture that is updated by the manager at each scanline advance. Thus, a scanline device manager takes advantage of the print and advance time to calculate the next state of the picture. This data-driven feature requires far less memory than maintaining a frame buffer.

The scanline device manager was developed for a family of intelligent thermal printers, the Gulton

Industries' Microplot series, to demonstrate feasibility and to investigate cost trade-offs. The microprocessor chosen for the implementation was an Intel 8080/8085 because of its wide availability in the application area of interest. The graphics software is available from Gulton in the form of a complete library of user-resident subroutines contained on a floppy disk. It is compatible with several standard formats and operating systems.

Multiprocessor software distribution

Present microprocessor technology dictates systems that distribute the graphics software tasks among different CPUs to improve the system performance/cost ratio (Fig 1). The host CPU deals with application programs using device independent routines. These routines use a set of virtual instructions to provide virtual opcodes and operands to the scanline device manager. In turn, the scanline device manager views the host as a virtual stack machine from which to fetch parameters and data upon receipt of the virtual opcodes. The scanline device manager interprets the virtual commands in terms of a scanline primitives set that can be subdivided into three categories (Fig 2).

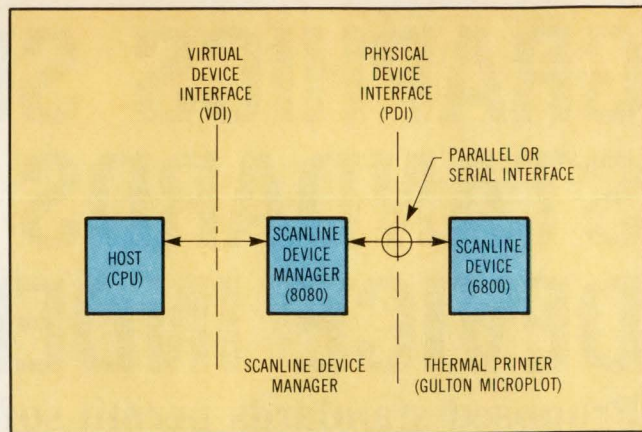


Fig 1 Graphics software tasks are distributed across three processors for improved system performance.

The first category, called VDI, includes user primitives that act at the VDI to interpret the user's virtual instructions and load the VDM. The second category, referred to as internal or data-driven primitives, consists of routines that perform the line-by-line housekeeping necessary to manage any scanline device. These routines are therefore general in nature. The third category, called PDI, features output primitives that provide the device

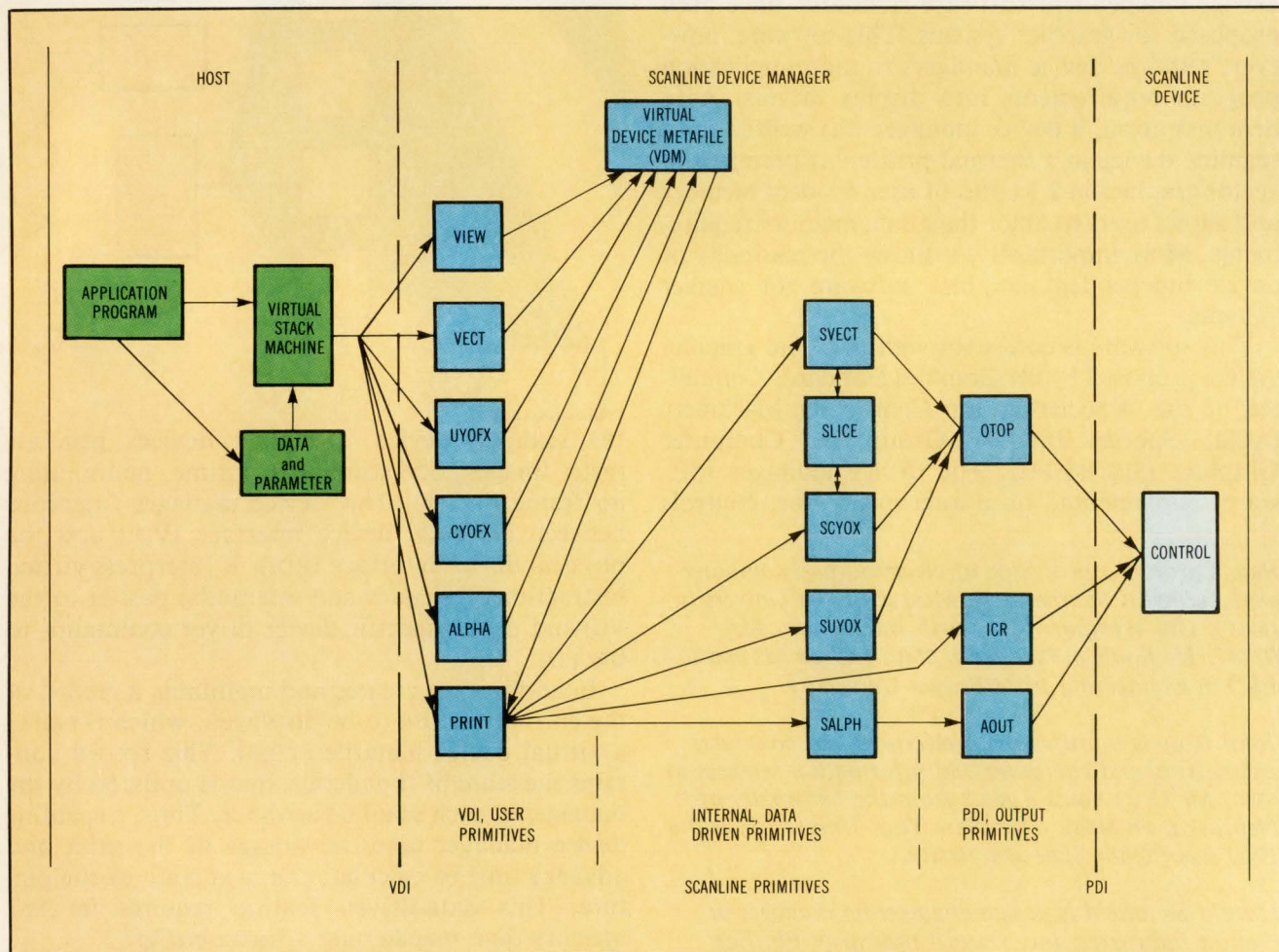


Fig 2 The scanline device manager has three categories of primitives: user, internal, and output.



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CIRCLE 47

CD-12

TABLE 1

VDI Primitives

Routine	Arguments	Functions
VIEW	XLOW YLOW XHIGH YHIGH BORDER	Initializes all the data pointers and parameter pointers, defines the viewing area, and indicates if the viewing area border is to be drawn.
VECT	XBEG YBEG XEND YEND	Installs a VECT from (XBEG, YBEG) to (XEND, YEND). These coordinates are relative to and limited to the viewing area.
UYOFX	@YDATA XBEG XINC XEND	Installs unconnected Y(X) data with beginning, increment, and end values along X-axis and a pointer to the user-supplied Y-axis data values. Values are relative to and limited to the viewing area.
CYOFX	@YDATA XBEG XINC XEND	Installs connected Y(X) data with beginning, increment, and end values along X-axis and a pointer to the user-supplied Y-axis data values. Values are relative to and limited to the viewing area.
ALPHA	@ADATA XBEG YBEG *XYFONT (XORY, FONT)	Installs ASCII data to be printed. Printing starts at (XBEG, YBEG) with YBEG truncated to the allowed tab positions, using user-supplied data (pointer = @ADATA), and printing direction and font chosen by XORY and FONT respectively.
PRINT	(none)	Uses the data installed by the above routines to implement plotting/printing.

* All variables are word (double-byte) variables. The high byte of XYFONT indicates print direction and the low byte indicates font.

driver functions and must be tailored to a specific device.

This modularization of primitives allows for a maximum of transportability between working environments. For example, a different scanline device may be attached simply by creating a new set of PDI primitives. The microprocessor basis of the scanline manager allows it to provide a high level virtual vocabulary of primitives that are independent of the specific hardware and are consistent with other device managers. Thus, identical application software can be bound to a variety of different hardware capabilities using different virtual device numbers, such as logical device numbers, to generate similar device images for different machines.

VDI scanline device primitives are implemented as subroutines written in Assembly language, which may be readily linked across the VDI. Table 1 lists these VDI primitives with a brief description of each. From a user standpoint, the printing of a picture could be a sequential set of calls as shown in Table 2.

The user must first do a call to VIEW to set up the viewing area followed by an arbitrary number (limited only by memory) of calls to vector (VECT), unconnected Y(X) (UYOFX), connected Y(X) (CYOFX), and alphanumeric (ALPHA), and terminated by a call to PRINT. Although only single calls to VECT, UYOFX, CYOFX, and ALPHA have been shown, clearly any mix is possible. Parameters associated with these subroutines are passed on the

A modularization of primitives allows a maximum of transportability between working environments.

stack and are assumed to be pushed onto the stack in the inverse order from which they are listed above.

The VIEW primitive corresponds to the SIGGRAPH primitive VIEWPORT, which defines a viewing area for graphics into which logical graphics are mapped. This primitive includes a clipping facility so that only those portions of objects that lie within the

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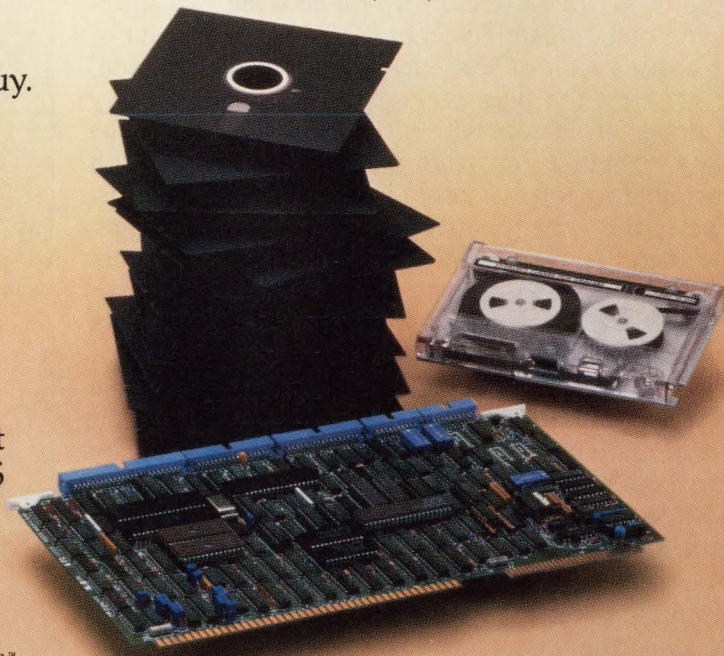
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TABLE 2

Printing Calls

- C INITIALIZE VIEWING AREA
CALL VIEW (XLOW, YLOW, XHIGH, YHIGH, BORD)
- C INSTALL PLOTTING/PRINTING DATA
CALL VECT (XBEG, YBEG, XEND, YEND)
CALL UYOFX (@YDATA, XBEG, XINC, XFND)
CALL CYOFX (@XDATA, XBEG, XINC, XFND)
CALL ALPHA (@DATA, XBEG, YBEG, XYFONT)
- C PRINT AND PLOT USING INSTALLED DATA
CALL PRINT
END

viewing area are displayed. A switch variable allows the user to dictate whether the border of the viewing area will be drawn or not. Viewing transformations, such as scaling, are assumed to be the host's responsibility. Thus, the scanline device manager receives its picture from the host in virtual device coordinates (VDC) and relates these coordinates to a metafile virtual graphics device (MVGD). In this case, the MVGD is the rectangular display surface generated as paper passes under the heads of the thermal printer. Using the location parameters provided by VIEW, the VDI scanline primitives VECT, UYOFX, CYOFX, and ALPHA provide data input to the manager's data structure or VDM.

Additional primitives and structures

The basic primitive needed for graphics is the ability to draw a vector or line between two specified points. Its implementation is the focal point of this discussion of scanline primitives. The opcode, VECT, lets the user define and print an arbitrary number of vectors within the viewing area via the data structure for vectors shown in Fig 3. Each installed vector uses seven words (14 bytes) of storage in the VDM for its parameters. These parameters bear the relationship shown in Fig 4 for vectors with slopes less than one. VXBEG, YBEG, VXEND, and VYEND correspond to the passed parameters (adjusted to the viewing area).

The VREM, VXDIFF, and YDIFF are used by the internal primitive SLICE that updates printing at each scanline advance. VXDIFF and YDIFF are large scale slope components ($VXDIF F = VXEND - VXBEG$ and $YDIFF = VYEND - YBEG$), and VREM is a small scale remainder used as a running variable needed at each scanline because of the quantized nature of the printing process. The remainder is thus the difference between the position of desired printing (for an exact rendition of the vector) and of the actual printing. This is due to the discrete nature of the device. This technique has no cumulative error. A call to VECT zero's VREM adjusts and installs the beginning and end values, computes the slopes, and sets up a pointer to this data in the vector scan table.

Since a scanline device is unidirectional, some primitives considered to be required in the standards such as MOVE and RETURN TO CURRENT POSITION have no utility and would be emulated at a software level above the VDI. In fact, these two primitives, since they assume a cursor, are device dependent and should not be required by a standard. Standard primitives should relate directly to the picture being painted and not the paint brush. Also, because of its unidirectional nature, the plotting of Y(X) data is a most natural function, and two primitives were included for this purpose. These Y(X) primitives, denoted UYOFX and CYOFX, provide unconnected point-by-point plotting and connected point-by-point plotting along the scanline device's natural X-direction, or the direction of paper flow. In the context of the standards, these primitives would be considered extensions. The intelligent thermal printer used had its own alphanumeric capability, which allowed code-efficient printing by tailoring the internal primitive ALPHA to the specific needs of the printer.

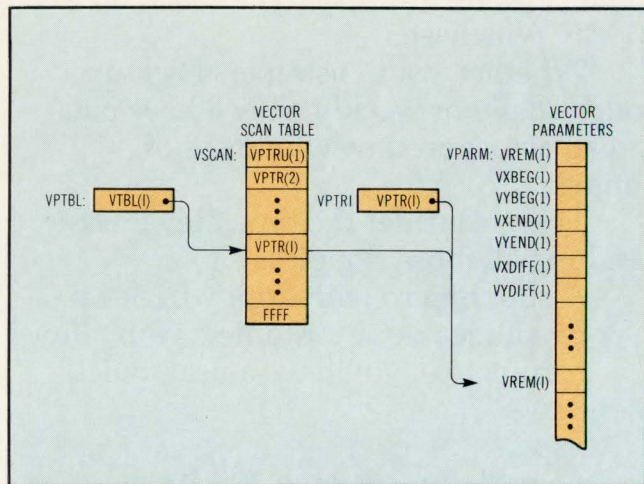


Fig 3 Multiple calls to VECT set up the data structure for vectors.

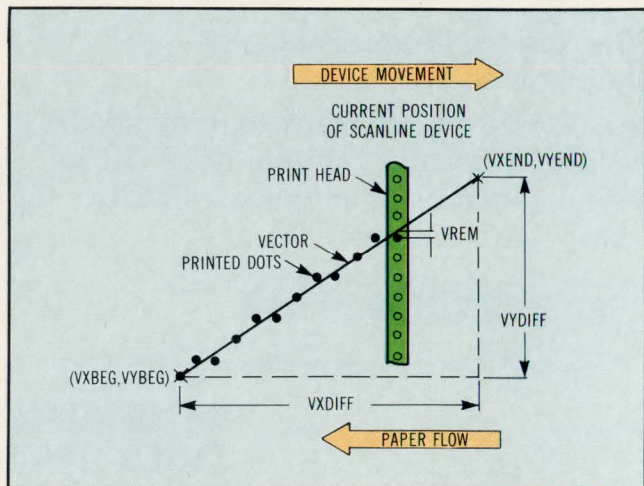
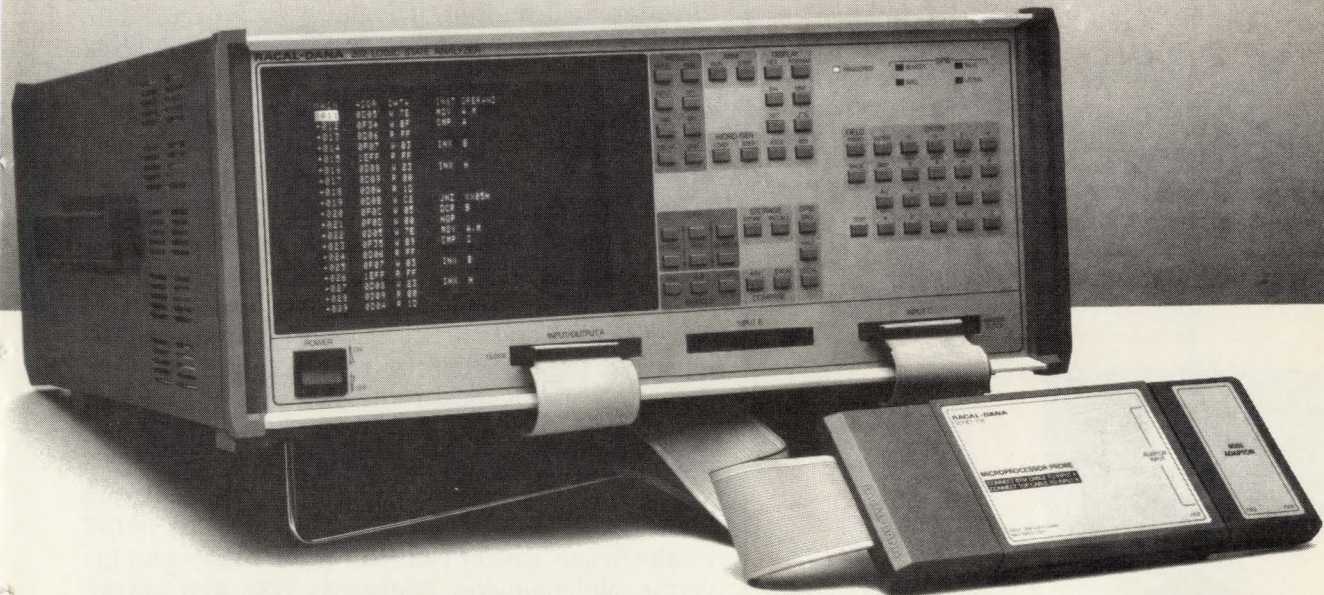


Fig 4 Vector parameters are passed to the scanline device for printing.

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TABLE 3

Plot Structures and Print Commands

VECT	ALPHA	Unconnected Y(X)	Connected Y(X)
VREM	@ADATA	@YDATA	@YDATA
VXBEG	AXBEG	UYBEG	CXBEG
VYBEG	AYBEG	UXINC	CXINC
VXEND	AFONT	UXEND	CXEND
VYEND			[7-WORD "LOCAL" VECTOR DATA STORAGE AREA]
VXDIFF			
VYDIFF			

The similarities between VDM structures for unconnected and connected Y(X) plotting and for alphanumeric printing are shown in Table 3.

They are similar to those shown in Fig 3. The components for alphanumeric (ASCII) printing include a pointer to the ASCII data, which is assumed to be terminated by an ETX (04) character, an X-axis begin point, a Y-axis begin point (which is limited to the allowed tab positions), and a double-byte variable which indicates the printing direction and the font. The unconnected Y(X) data follows the argument list for the corresponding subroutine UYOFX, and the first four words of the connected Y(X) also show this correspondence. However, the connected Y(X) data structure also reserves a seven-word local storage area into which vector-like data is repetitively installed at print time. Each data structure only maintains the setting of the scanline device at the thermal print head's current position. This is done with respect to the picture being printed and sufficient information to determine the setting after the next scanline advance. Thus, the current state of the picture is maintained.

Hub of the scanline device manager

The hub of the scanline device manager software is the PRINT subroutine (Fig 5). A call to PRINT results in subsequent calls to routines that scan the vector, alphanumeric, connected Y(X), and unconnected Y(X) scan tables. These tables contain pointers to corresponding parameter tables and the scan tables are terminated with PTR = FFFFH. The scanning process repeats with each scanline advance. Thus, the routines SVECT, SALPH, SUYOX, and SCYOX scan the corresponding scan table, and from the data contained in the corresponding parameter tables, plot points or ASCII data are issued. When all the data for one of the scan pointers has been issued, a null pointer is installed in the corresponding scan table so that subsequent scans may neglect this particular data.

A flowchart of the SVECT primitive used to scan the vector scan table is shown in Fig 6. The routine gets a pointer from this table. A return is executed if the scan is complete (pointer = FFFFH). If the pointer is null, or if the scanline advance has not reached the beginning of the vector, the pointer to the scan table is updated and the process is repeated. Otherwise, the subroutine SLICE is used to slice the vector into the proper Y-axis point(s) for the current scanline, or the X-axis point. SLICE also transmits an end-of-vector indicator, which is used to insert the null pointer. The blocks that show the vector parameter data being loaded into or stored from a fixed data area are not really necessary but decrease the running time for the 8080/8085 processor. More modern processors (eg, 6809, 8086,

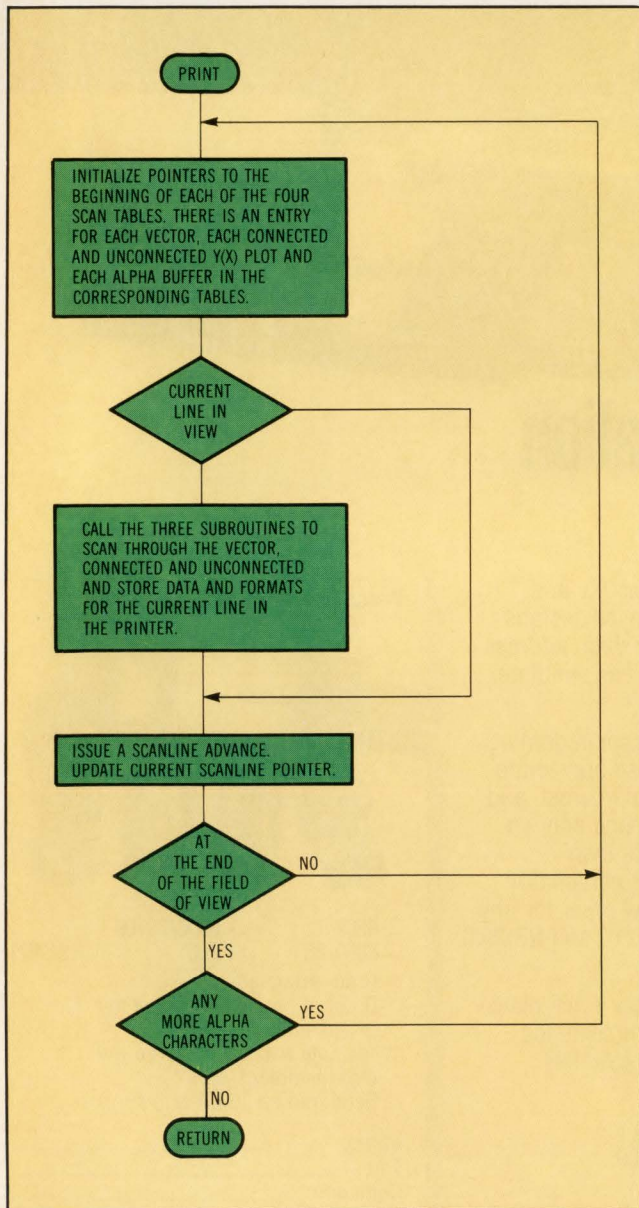
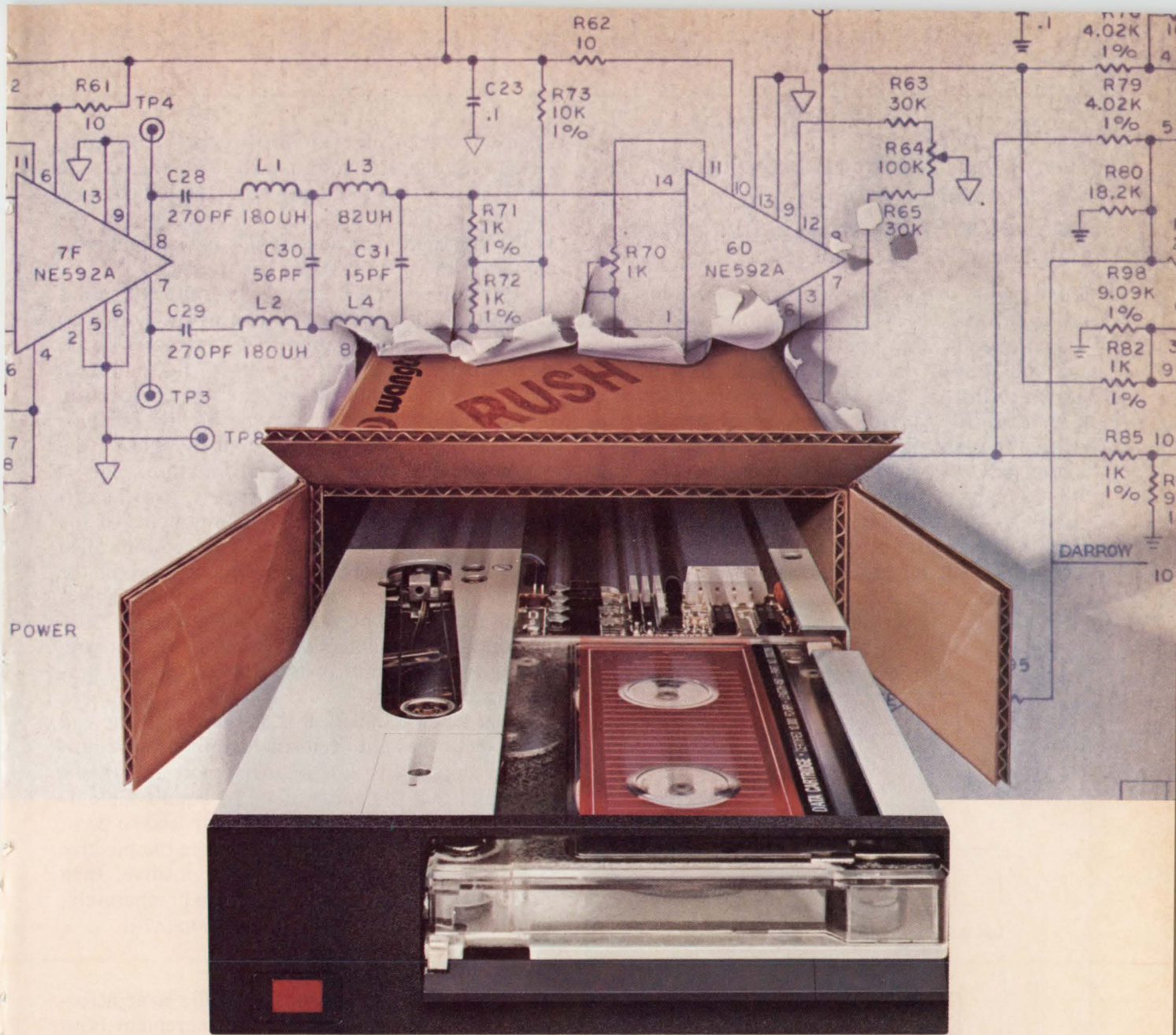


Fig 5 The PRINT subroutine is central to the operation of the device manager software.



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Plot data, which consists of either a single point or a line segment, is transmitted for each scanline advance.

68000), with better data handling and addressing mode capabilities, would not require this.

The routines that scan the two Y(X) data tables and the ALPHA data table proceed in a manner similar to that of VECT. In the case of unconnected Y(X), only the correct X-axis point needs to be located to place the corresponding Y-data. For the connected Y(X), it is necessary to install a local VECT as each plot point is encountered. This vector points to the next plot point and uses SLICE as above. The routine SALPH scans the ALPHA scan table with a similar protocol. However, in this case

when the current line equals the start of printing the ALPHA characters are issued using the routine AOUT. If all the characters are not issued, (eg, printing in the X-direction, or printing in the Y-direction and a carriage return is encountered), the new XBEG is updated by the font size.

The routine SLICE is used to determine the point or points in the current scanline to be plotted to give the best representation of any vector with no cumulative errors. That is, within the quantized constraints of the dot spacing, the best dot location is always determined. The data structure contains the location of the beginning and the end of the vector and the vector slope information. This is large scale slope information; that is, it is the difference between the X- and Y-components of the beginning and end points. A storage location called VREM is used to hold the equivalent error in the quantized location of the last point plotted. This is zero at the start. The values of VXBEG and VYBEG are continually updated with VYBEG always representing the next point or the start of the next segment to be plotted.

When SLICE is called, it is assumed that the end of the vector has not been reached, that point plotting, as opposed to line segment plotting, will be done, and that the value of DATA equals the current YBEG (Fig 7). The slope is compared to zero. Negative slopes are handled much like the positive slope case. Assuming the slope is positive, then three slope conditions are handled separately, namely slope >1 , slope = 1, and slope <1 .

Dealing with slope conditions

If the slope = 1, the process is quite straightforward since it is only necessary to increment both XBEG and YBEG and plot the current YBEG. If the slope <1 , the value of the Y-component of the slope is added to the remainder, and the result is compared to half of the X-component of the slope. This predicts if the next point should be considered to be quantized to the current Y location or should be updated by one. If it is updated by one, then the X-component of the slope is subtracted from the remainder to give a new remainder, which then incorporates the concept of both upward and downward (Y-direction) quantization.

A test is also made to see if the end of the vector has been reached, and, if so, this is transmitted back to the calling program. If the slope >1 , the need for line segment plotting is apparent. In this case, the end of the segment is first assumed equal to the start of the segment (the latter kept in the location DATA). A loop is then entered where the remainder is updated by the X-component of the slope in each pass until the remainder exceeds half of the Y-component of the slope. In each pass, the

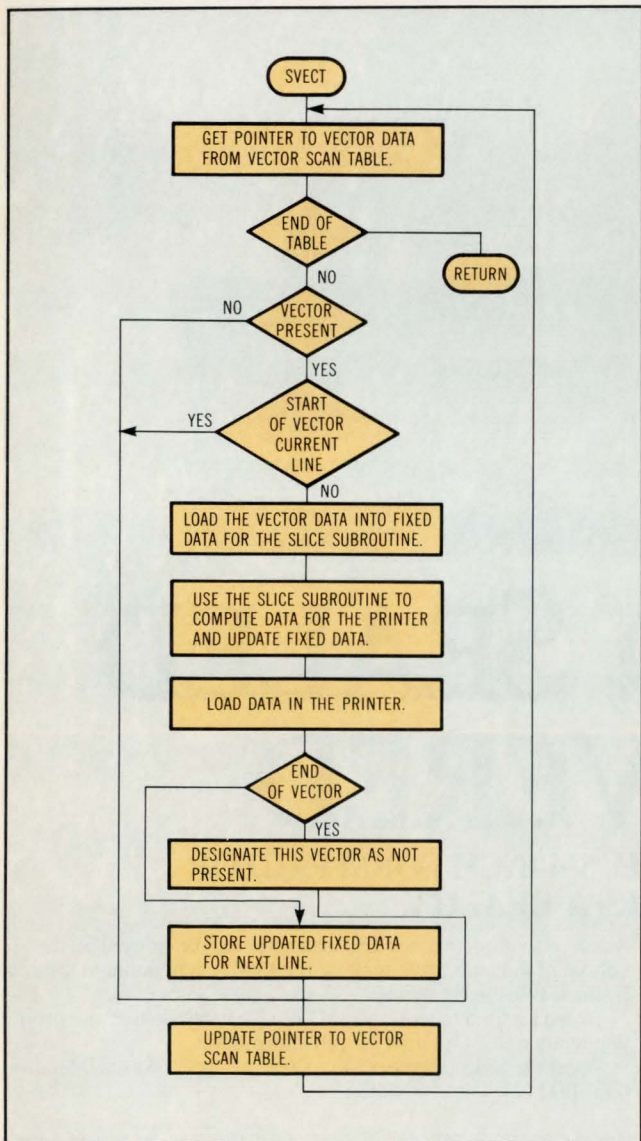


Fig 6 The SVECT primitive shown in the flowchart scans the vector scan table.

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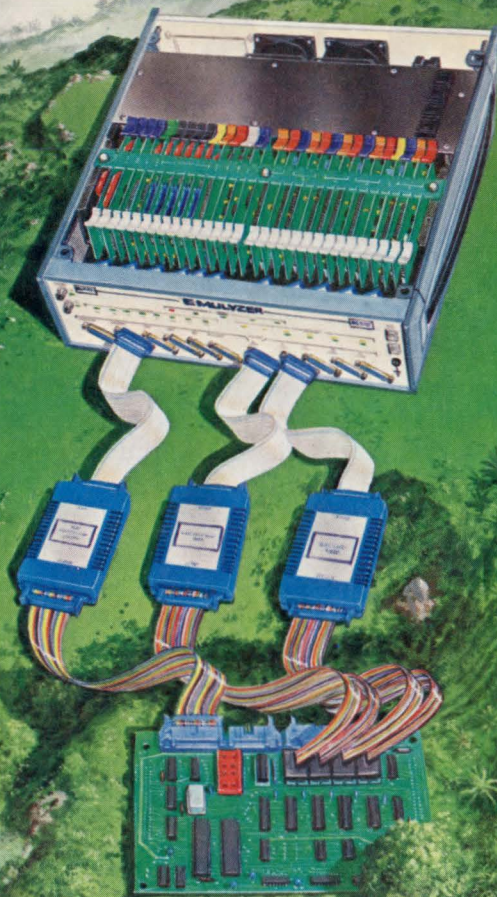
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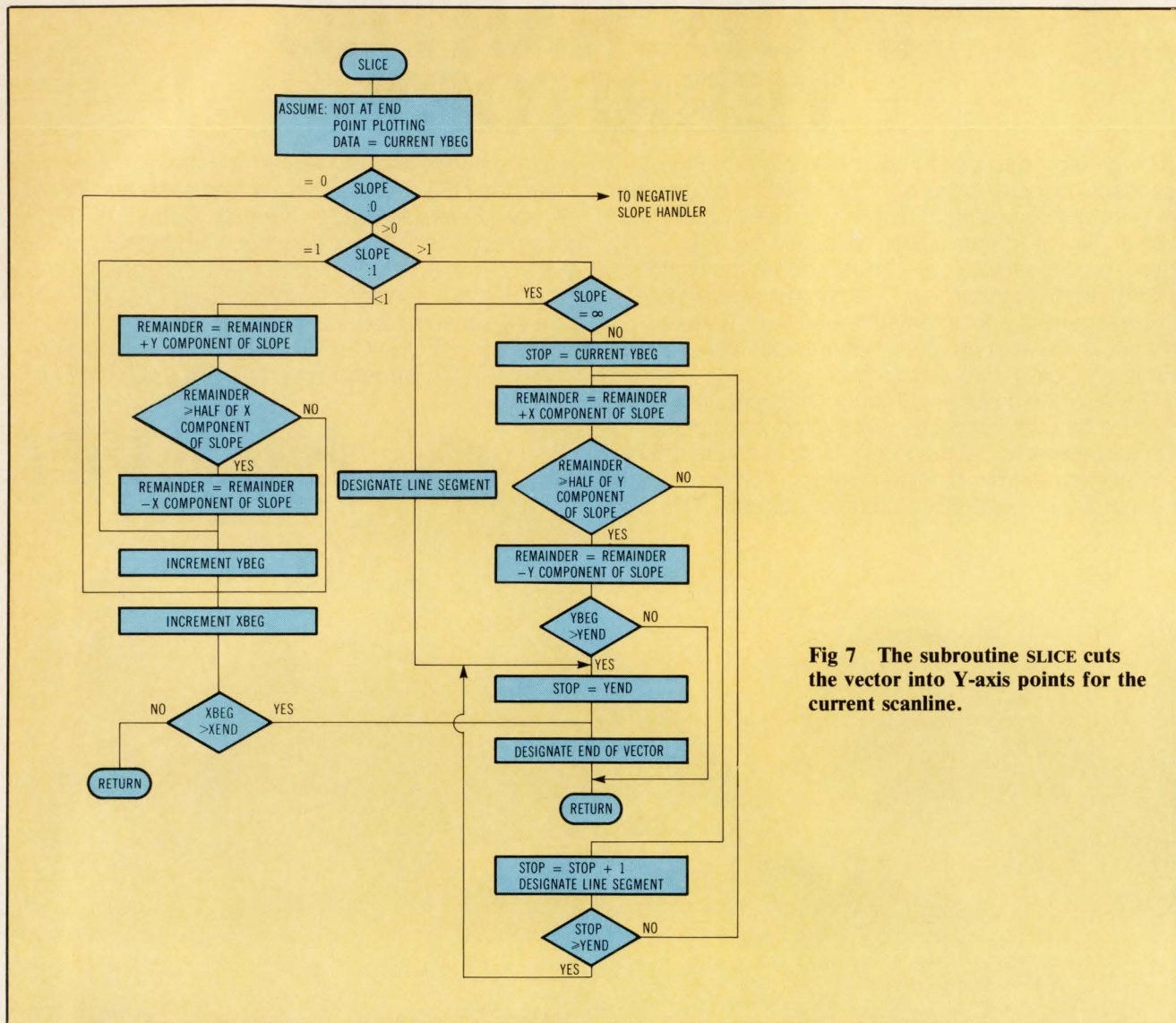


Fig 7 The subroutine SLICE cuts the vector into Y-axis points for the current scanline.

value of STOP is incremented. By this technique, the quantized points that must be plotted on the current line are identified. When this loop terminates, the next point or points must be quantized to the next line. This requires that the Y-component of the slope be subtracted from the remainder to incorporate the concept of X-direction quantization. The end-of-vector testing is done much like the other slope cases.

Upon return from SLICE, the SVECT routine calls a subroutine OTOP that contains the device-specific code to drive the PDI to the Microplot-80 or the Microplot-44, which are bit parallel/byte serial. The Microplot-80 also has a 9-bit parallel interface, and an optional serial interface for both devices is available. Running time of the software may be improved if interrupt-driven output is used. In this case, OTOP would output data to a first in, first out queue from which it is unloaded on an interrupt basis. This would efficiently use the hand-shake time.

Plot data, which consists of either a single point or a line segment, is transmitted for each scanline advance. ASCII characters are buffered and can be mixed with plot data. Various character fonts may be utilized. With mixed plot and character information, two modes of operation are possible: plot-slaved-to-print or print-slaved-to-plot. In the first case, a line advance or carriage return corresponds to a character line, and the plot information must be issued to the device in a prescribed time sequence dictated by signals the plotter issues. In the second case, each scanline advance is externally driven. Since the emphasis here was plot software, the second case was used.

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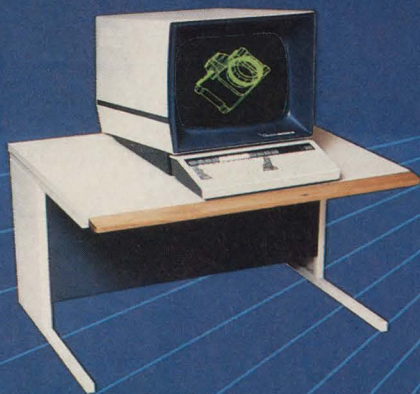
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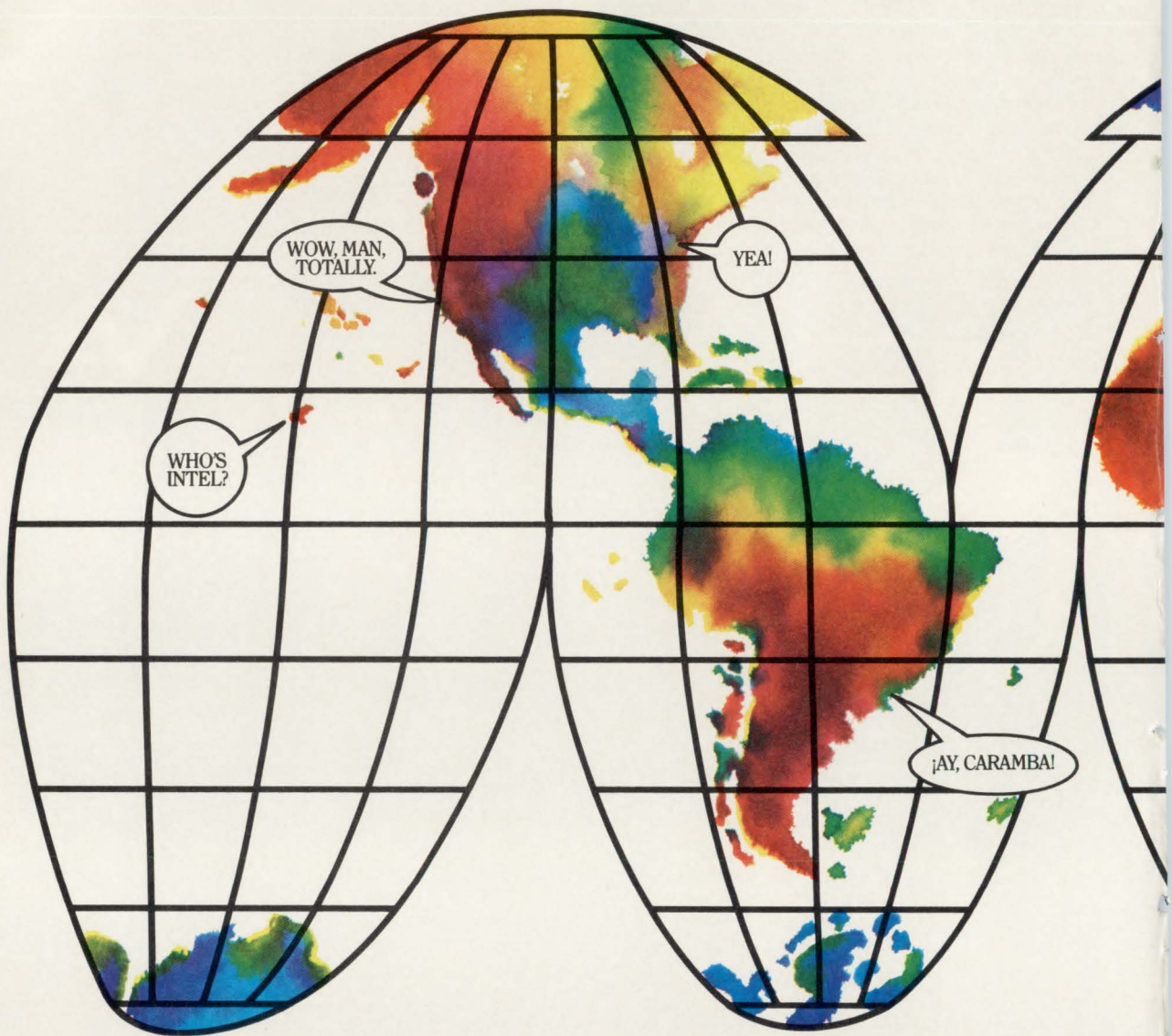
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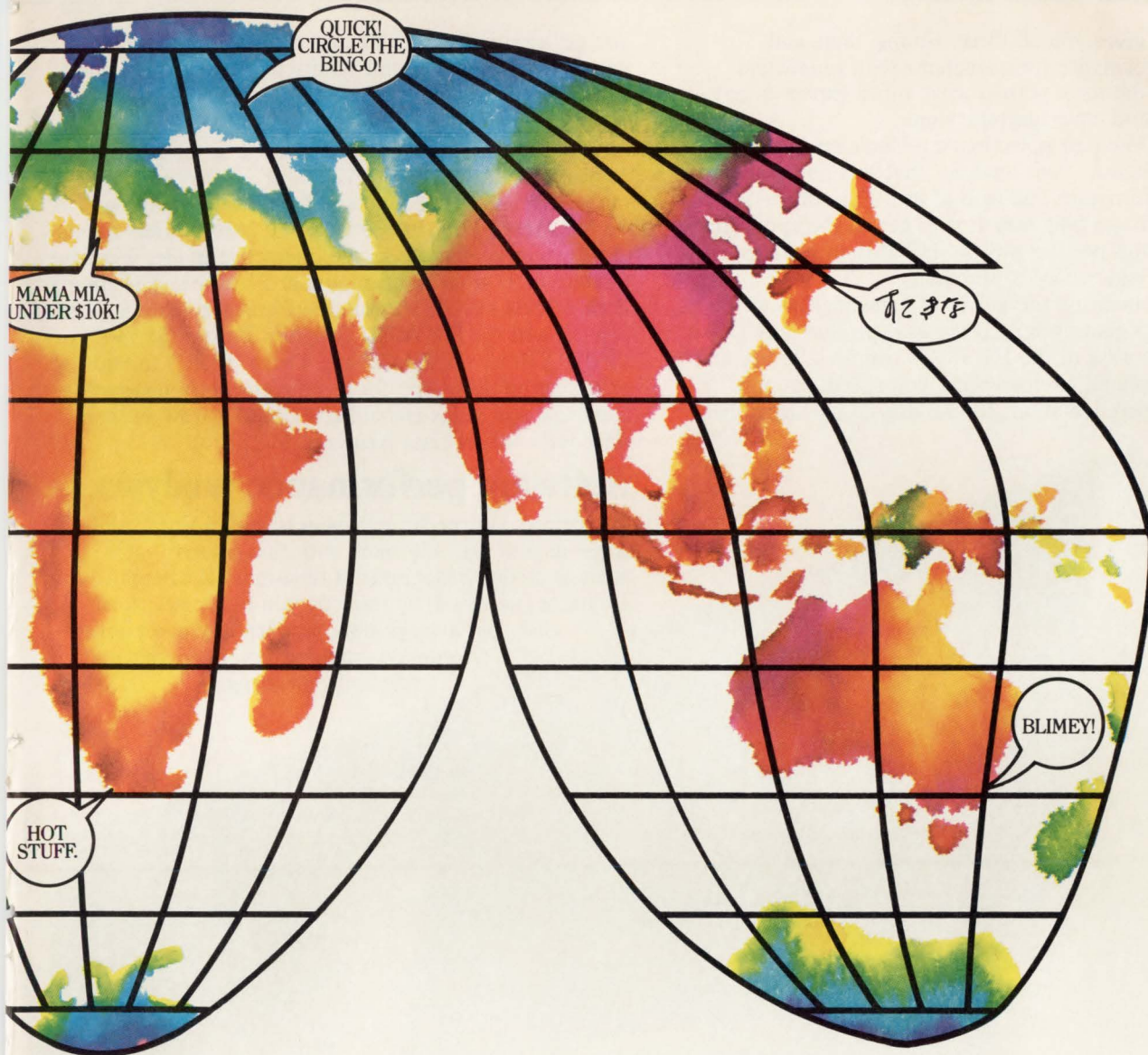
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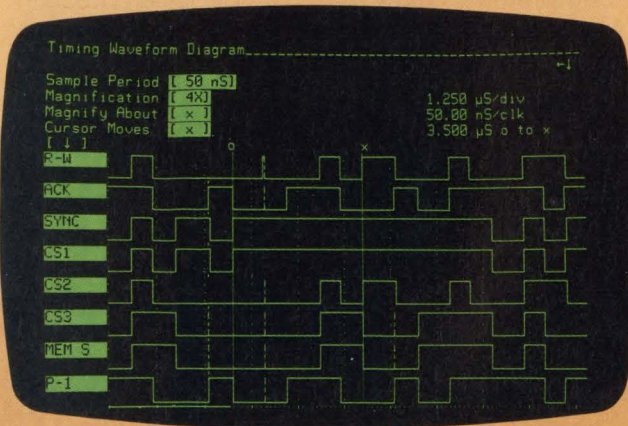
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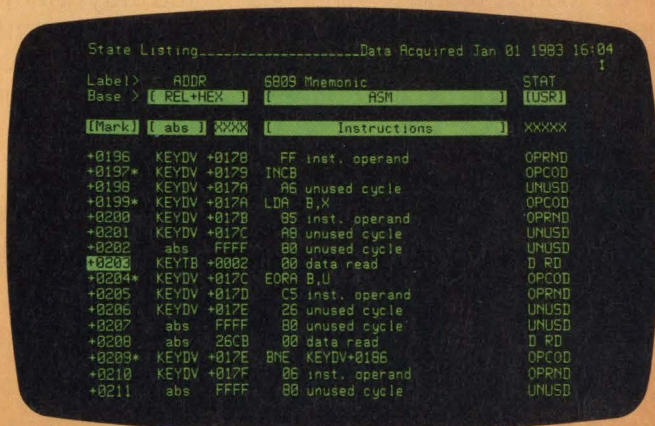


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LANGUAGE-BASED ARCHITECTURE EASES SYSTEM DESIGN—II

Unlike other high level languages, Occam is targeted specifically at distributed architectures.

by Pete Wilson

This is the second in a series of articles on Occam. (See Computer Design, Nov 1983, pp 107-115 for Part I.)

Programming languages can be viewed as providing two distinct facilities to a designer. One is the ability to instruct a computer in some course of action. The other facility is the use of the language's features as a design tool to allow the problem to be broken down into subproblems, and these into even smaller ones. This decomposition operation continues until the fragments are of manageable size so that the designer can start detailed coding.

To a large degree, normal system programming languages (eg, some variants of Pascal, C, and Ada) provide equivalent facilities for detailed coding. Major differences arise in their treatment of modularity. These differences are most apparent when the languages are used to construct real systems. Shifting specifications, needed optimizations, and the need for more than one programmer will severely test the modularity tools the language provides.

Occam's communicating process model provides a form of modularity that is very strong, yet simple to use and understand. Concurrent processes can only manipulate their own resources; indeed it is impossible in the language for such processes to even "think" of resources other than their own.

Pete Wilson is microcomputer applications manager at Inmos Corp, PO Box 16000, Colorado Springs, CO 80935. He holds a BS in physics and mathematics from Sheffield University, England.

The insulation between sequential processes is not as great, since these communicate by the reuse of shared variables. Thus, the ability to use multiple processors and strong modularity boundaries will urge designers to construct systems as collections of concurrent Occam processes.

This design style is unnatural for most programmers. They will generally accept the usefulness of modularity, but will use procedures as the module. Surprisingly, the change to using concurrent processes that have information passed to them down channels, rather than calling procedures with parameters, is not difficult to make given an appropriate language. Building a small graphics package for a personal computer using Occam in a sequential manner will help introduce the concurrent style. The completed program will then be transformed into a concurrent version. The mechanics of the transformation may be used as guidelines in the creation of concurrent programs.

Developing algorithms

Drawing lines is a computationally intensive task for general purpose computers. For the microprocessor considered here, its general slowness in multiplication and division makes the problem worse. To avoid using these operations, algorithms that rely purely upon repeated additions and comparisons have been developed. These are used in most personal computers either as program or embedded as hardware inside dedicated graphics controller engines.

The computer used in this exercise is the Victor 9000, which employs a bit-mapped raster screen. In the example, it allows 800 dots in the x direction, and 400 in the y. It is generally impossible to draw a smooth straight line between any two points on the

screen, since such a line will need to pass between the discrete addressable pixels. Instead, a set of horizontal or vertical line segments (adjacent pixels) must be drawn to approximate the desired line.

The pixels defining the line segments can be derived using simple geometric considerations. Consider drawing a line from (x0,y0) to (x1,y1). A very simple Basic program to do this might be written as follows:

```
FOR x=x0 TO x1
  y= ((y1-y0)/(x1-x0))*x+y0
  plot(x,y)
NEXT
```

The program would look very similar in Occam. The FOR loop in Basic (and other languages) is mirrored by Occam's sequential replicator. The equivalent Occam program fragment is

```
SEQ x = [x0 FOR 1+(x1-x0)]
SEQ
  y:=((y1-y0)/(x1-x0))*x+y0
  plot(x,y)
```

There are several superficial differences between the two programs. These arise from three causes. First, the Occam sequential replicator specifies a start value and a repetition count rather than start and end limits. Furthermore, the step value is always +1. To step by other values, the programmer would generally introduce a further variable (to be

incremented appropriately), thereby using the sequential replicator solely to count the iterations. Alternatively, a WHILE constructor could be used.

Second, the expression syntax differs. Occam has no operator precedence, so the programmer must explicitly spell out the order of evaluation. Although this is initially an irritation to those accustomed to other languages, it is quickly overcome. It is advantageous because complex precedence rules no longer need to be memorized and programmers are forced to understand that $(a - b) + c$, on a digital computer with a fixed word length, is not the same as $(a + c) - b$. For many values of a and c , the latter expression may cause overflow, while the former would not. It is useful to be able to specify that the second expression is the desired order, rather than leaving it in the hands of the compiler writer.

The third difference is the necessity to specify sequential execution of statements to compute y and to plot the point x,y . Basic assumes the sequence, while in Occam the two statements could be executed in parallel. In this particular case, the two statements could not be executed concurrently, since they share variables. (In Occam concurrent processes may not commonly share variables—although they may share read-only values.) Leaving concurrent case detection to the compiler would both complicate the compiler and make the language system more irregular.

Simple examples

While the program is too simple to be useful, it is clear that taking much of the computation outside the loop would accelerate it.

```
slope:=(y1-y0)/(x1-x0)
SEQ x=[x0 FOR 1+(x1-x0)]
SEQ
  y:=(slope*x)+y0
  plot(x,y)
```

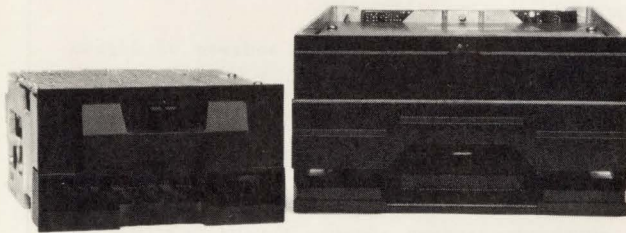
However, even this program version will not work effectively. The values are integers, so the result of the division will be inexact. The original version, with the division in the loop, might also suffer from this problem; but it can be modified to work safely by changing the order of evaluation so that $y:=((x*(y1 - y0))/(x1 - x0)) + y0$. With the multiplication done first, the result is more accurate, especially if the compiler can recognize the situation and work with the double-length result from the multiplication for the division.

The simplest way to make the program both fast and accurate removes the need for division and multiplication, and uses a loop to provide an iterative solution. The Occam program is shown in Table 1 and introduces another two language constructs.

TABLE 1
Simple Line Drawing Algorithm

```
PROC DrawLine(VALUE x0,y0,x1,y1)=
  -- line from (x0,y0) to (x1,y1)
  -- assumes y1 > y0 and x1 > x0
  VAR x, y, delta, dx, dy:
  SEQ
    x:=x0
    xwork:=x0
    y:=y0
    dx:=(x1-x0)<<1  -- shift has effect of *2
    dy:=(y1-y0)<<1
    delta:= x1-x0
    WHILE y<>y1  -- for all y between y0 and y1
      SEQ
        WHILE delta<= dx  -- for each value of y
          SEQ
            PlotPoint(x,y)  -- plot this point
            delta:=delta+dy
            x:=x+1  -- next x
          delta:=delta-dx
        y:=y+1:  -- next y
```

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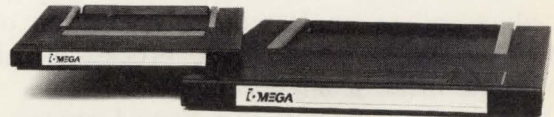
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The program fragment is named, allowing it to be called up simply. The declaration syntax looks very similar to the usual procedure declaration, but in fact is quite different in its semantics. The closest parallel is with a macro declaration, rather than a procedure. This choice was made because of Occam's application to multiple computer systems, where a copy of a particular process may be needed in each computer. Clearly, the notion of a macro better fits this situation than would that of a procedure, since separate expansion of the process in each machine is desirable.

There would be significant problems (given that the language designer's intentions were to provide simple and efficient semantics for the language) in adopting a procedure-like meaning. For example, it is not clear what would be meant by calling a procedure in another computer. The macro-like semantics need not be carried over blindly to the implementation. A compiler may reasonably use a procedure call to implement an invocation of a named process when the same process is called many times inside a single computer.

The formal parameters to a named process are typed. In current implementations, the types may be VALUE, VAR, and CHAN. These may refer to word-sized or vector objects. Parameters passed as VALUE may not be assigned to within the body since the abstraction is macro-like. VAR parameters may be assigned to (ie, written on the left-hand side of an assignment statement). The variables used as actual parameters in the "calling" process will be left with the values the called process assigns when it terminates. Thus, any number of parameters may be passed into or out of a named process.

The process also introduces the WHILE constructor. Again, both syntax and meaning are simple. Since the process to be repeatedly executed is multi-line (a collection of single line processes), a constructor—here SEQ—is needed to define the collection's bounds and its manner of execution.

Considering the plot process

Examining the code will show that the process plots a number of points whose y coordinates are the same, and then increments y by 1 and plots some more points with identical y coordinates. Since the plot process basically just sets a bit in memory, this loop can also be accelerated by creating a different process to plot horizontal lines, rather than just single points.

On the Victor 9000, the screen is mapped into memory as contiguous 16-bit words, arranged in columns. The first column is 400 words long, and represents the left-hand side of the screen. The next 400 words map into the next 16-bit stripe to the right, and so forth. The physical address of pixel (x,y) is therefore bit $(x \setminus 15)$ in word $((x/16)*400) + y$. Since the processor uses byte addressing,

this is bit $(x \setminus 15)$ in the byte pair at address $2*((x/16)*400) + y$. The division can be accelerated by converting it to a shift.

Occam requires all data objects to be local to a process. The screen however, is an object fixed in the processor's physical address space. There is no convenient way of providing a private process in order to manipulate it. Occam implementations provide intrinsic processes to read and write values to absolute addresses, thus sidestepping this problem. On 8086 family machines, these processes necessarily include a segment base address to allow the machine's complete address space to be accessed. Using the word access pair of intrinsics allows the point plotting process to be written as follows:

```
PROC plot(VALUE x,y)=
  DEF screen = #1000: -- base address of screen
  VAR wordvalue,address:
  SEQ
    address:=(((x>>4)*400)+y)<1
    getabsword(screen,address,wordvalue)
    putabsword(screen,address,wordvalue \/(x \ 15)):
```

Note the macrolike behavior of the intrinsics. The get process reads the address whose value is $(screen*16) + address$, and places the result in its third parameter, here wordvalue. The notion of a function is missing from Occam. For efficiency, implementations will generally expand these particular intrinsics into inline code rather than using the normal process invocation.

The horizontal line plot process is somewhat longer, but still straightforward. It speeds up plotting by doing the address arithmetic less frequently (just once per line segment, rather than once per point), and by setting many bits with each memory access. The process will draw a straight line at constant y from x0 to x1. To draw a line segment, it will need to set a number of bits. To save computation, it will use a pair of lookup tables to provide the bit-strings needed. The process is shown in Table 2.

The process again introduces some Occam syntax. For example, all Occam tables are defined and used as preset vectors. Here, the two tables are declared containing hex values; ordinary integers are also usable. Table or vector elements are accessed using an index, with the first element having index 0. Thus, lones[5] is the sixth element of the table.

The IF constructor is also shown. This subsumes both the conditional and CASE statements of other languages into a single simple construct. The IF constructor introduces a collection of conditions, each of which has a process associated with it. Here, the conditions are wordcount=0, wordcount=16, and TRUE. The constructor causes each

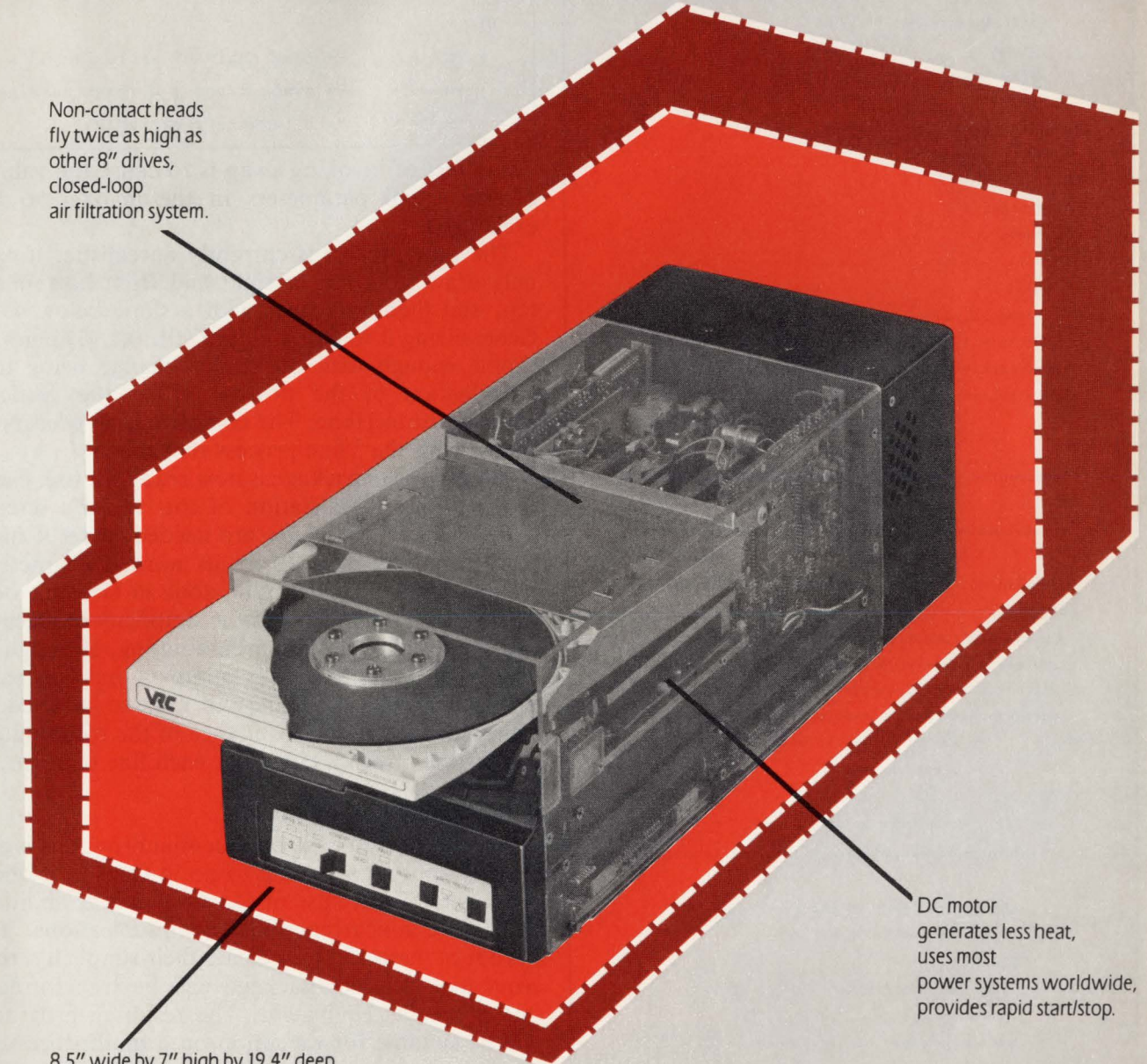
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TABLE 2
Horizontal Line Drawing

```

PROC Hline(VALUE y,xstart,xend)=
  DEF lzeroes = TABLE[#FFFF,#FFFE,#FFFD,#FFF8,
                        #FFFO,#FFE0,#FFD0,#FF80,
                        #FF00,#FE00,#FD00,#F800,
                        #F000,#E000,#D000,#8000],
    lones = TABLE[#0001,#0003,#0007,#000F,
                   #001F,#003F,#007F,#00FF,
                   #01FF,#03FF,#07FF,#0FFF,
                   #1FFF,#3FFF,#7FFF,#FFFF],
    xaddressincrement = 800,
    screen = #1000,
    addressmask = #FFFO

  VAR address,wordvalue,wordcount, x0, x1:

  SEQ
  x0:=xstart
  x1:=xend
  IF
  x0>x1
    swap(x0,x1)
  address:=(((x0>>4)*400)+y0)<<1
  wordcount:=(x1/\addressmask)-(x0/\addressmask)
  getabsword(screen,address,wordvalue)
    -- see if x0, x1 are in the same word
  IF
  wordcount=0 -- x0,x1 cohabit a single word
  SEQ
  putabsword(screen,address,wordvalue\/(lones[x/\15]\/
                                           lzeroes[x1/\15]))
  wordcount=16 -- x0 is in one word, x1 in the "next"
  SEQ
  putabsword(screen,address,wordvalue\/lzeroes[x0/\15])
  address:=address+xaddressincrement
  getabsword(screen,address,wordvalue)
  putabsword(screen,address,wordvalue\/lones[x1/\15])
  TRUE -- x0 and x1 are in words separated by at
    -- least one word

  SEQ
  -- first write ones to first word
  putabsword(screen,address,wordvalue\/lones[x0/\15])

  -- then write #FFFF to intervening words
  SEQ i=[0 FOR (wordcount-16)>>4]
  SEQ
  address:=address+xaddressincrement
  putabsword(screen,address,#FFFF)
  -- now write ones into last word

  address:=address+xaddressincrement
  getabsword(screen,address,wordvalue)
  putabsword(screen,address,wordvalue\/lones[x1/\15]):

```

of the conditions to be evaluated. The first one to evaluate to TRUE has its associated process executed. When the chosen process terminates, or if no condition evaluates to TRUE, the IF construct terminates. Use of TRUE in the example is analogous to an ELSE clause in other languages.

Finally, the Hline process includes an invocation of a swap process to exchange x0 and x1 in the case that x0 is to the right of x1. This allows Hline to be generally useful while keeping its internals simple. The swap process shown below is an example of the use of VAR parameters rather than VALUE ones.

```

PROC swap(VAR x,y)=
  SEQ
  x:=x > < y -- this chain of exclusive-OR's
  y:=x > < y -- swaps x and y without needing
  x:=x > < y: -- a temporary variable

```

The effect of invoking swap is to cause the values of the actual parameters in the invoker to be exchanged.

The Line process is currently unrealistic. It can only draw from left to right and from bottom to top, and then only lines with a slope below 45°. Generalizing it to cover all (x0,y0), (x1,y1) pairs is simple enough with the major change being the introduction of the process Vline, the vertical counterpart to Hline. The complete Line process is shown with the Vline process in Table 3.

The complete package is now ready for use, even though some initialization of the Victor's screen store and CRT controller are needed to set it into high resolution mode from its normal character-mapped mode. This may be done in Occam, too. The package demonstrates the simplicity of Occam use in normal sequential programming, although it could still do with further optimizations—in particular, expansion of Hline and Vline to inline code rather than calls, and avoidance of the recomputation of the screen address for each line segment.

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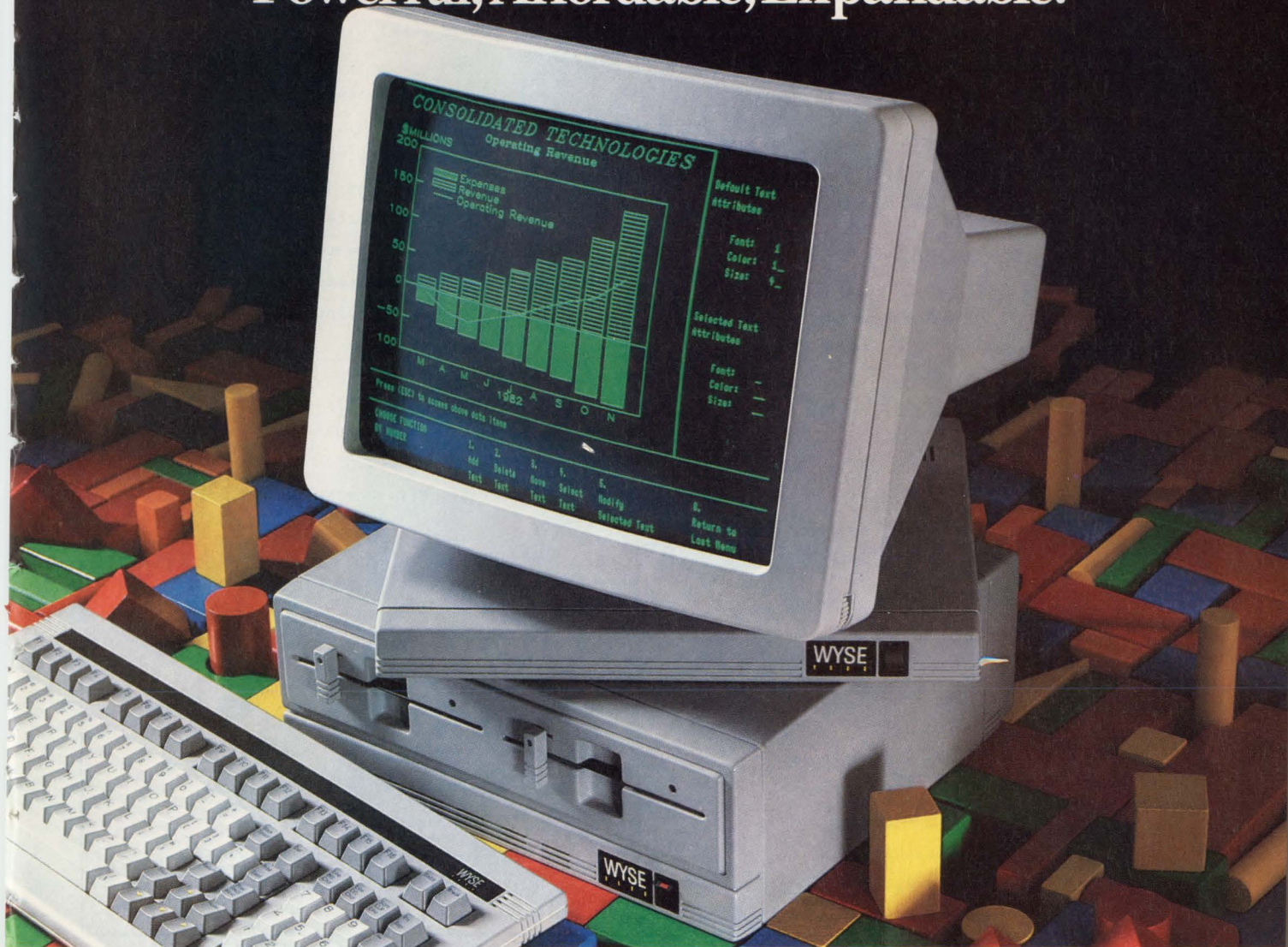
Although writing such sequential programs is an entirely appropriate thing to do in Occam, it does not make effective use of Occam's unique abilities to capture concurrency and communications. To introduce these and to indicate their simplicity, the sequential graphics package will be transformed into a parallel equivalent. The resulting program will be suitable for execution on a multiprocessor implementation, providing significant performance advantages with the correct processor architecture.

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TABLE 3
General Line Plotting Process

```

PROC Drawline(VALUE x0,y0,x1,y1)=
  VAR x, y, delta, dx, dy,
      xwork, ywork, xincrement, yincrement:
  SEQ
  x:=x0
  xwork:=x0
  y:=y0
  ywork:=y0
  IF
  x0>x1 -- right to left
    xincrement:=-1
    dx :=(x0-x1)<<1
  TRUE -- left to right
    xincrement:=1
    dx :=(x1-x0)<<1
  IF
  y0>y1 --bottom to top
    yincrement:=-1
    dy :=(y0-y1)<<1
  TRUE -- top to bottom
    yincrement:=1
    dy :=(y1-y0)<<1
  IF
  dy<=dx -- mainly horizontal line
    SEQ
    delta:=dx>>1
    WHILE y<>y1
      SEQ
      WHILE delta<=dx
        SEQ
        delta:=delta+dy
        x:=x+xincrement
        delta:=delta-dx
        Hline(y,xwork,x)
        y:=y+yincrement
        xwork:=x+xincrement

```

```

  IF
  x<>x1
    Hline(y1,x,x1)
  TRUE -- mainly vertical line
    SEQ
    delta:=dy>>1
    WHILE x<>x1
      SEQ
      WHILE delta<=dy
        SEQ
        delta:=delta+dx
        y:=y+yincrement
        delta:=delta-dy
        Vline(x,ywork,y)
        x:=x+xincrement
        ywork:=y+yincrement
    IF
    y<>y1
      Vline(x1,y,y1):
  PROC Vline(x,ystart,yend)=
    DEF screen = #1000:
    VAR address, bit, wordvalue, y0, y1:
    SEQ
    y0:=ystart
    y1:=yend
    IF
    y0>y1
      swap(y0,y1)
    address:=(((x>>4)*400)+y0)<<1
    bit:=1<<(x\15)
    SEQ i= [0 FOR 1+(y1-y0)]
    SEQ
    getabsword(screen,address,wordvalue)
    putabsword(screen,address,wordvalue\bit)
    address:=address+2:

```

invokes the appropriate procedures that are told what to do by their parameter values. A concurrent implementation will assign concurrent processes to the major tasks. These will be told what to do by having information passed to them down Occam channels. The very same decomposition of the problem may be used as the basis for concurrent implementation. Each process will have a similar form:

```

DO FOREVER
  read an input
  do what it says

```

This differs from a procedure-like decomposition, where the looping is done by the outer level of

the program that calls a given procedure only when it is wanted. When the various processes all coexist, each must keep itself alive so that having once done what it has been asked to do, it can prepare for the next request.

This introduces a responsibility for the process that an equivalent procedure need never worry about. The system as a whole presumably has to stop sometime. To achieve this, each process must power down individually. There are two straightforward ways to accomplish this. Either a "stop" value may be invented which will, when received, cause the process to halt tidily, or a separate "stop" channel may be started to each process. In the former case, the process must test the incoming

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values so it can decide to act or to terminate. In the latter case, it must accept input from either the data channel or the stop channel. Choice of solution rests with the designer, but it is generally more efficient to test for a value rather than ALT between channels.

The sequential program's mapping into the concurrent form is now clear. The body of each process remains largely unchanged, except that what used to be formal parameters are now local variables. It now has channel parameters. It loops, reading from its input channel to the appropriate local variables, and it tests for termination values. However, there is one "architectural" change. Both Hline and Vline need to write to the memory

The language's simplicity makes frontend compiler design and implementation straightforward.

defining the screen. Some way of housekeeping this contention is needed, and—as is usually the case—the simplest and clearest course of action is to create another process to handle writing to memory. So a fourth named process, screen-right, is invented and is requested to OR-values into screen store by Hline and Vline, which talk to it down two channels. Screen-right itself will act on just one request at a time. It chooses between Hline and Vline requests by using an ALT on the two channels. Since the changes to all the processes are similar, only screen-right and Vline are shown in Table 4.

The concurrent program can now make use of four processors, rather than just one. Of the four, one processor—screen—is rather simple since all it

does is write to memory. Its operation can safely be overlapped with the other processes, and this pipelining provides significant opportunity for increased performance. Hardware for the concurrent implementation exactly matches the Occam description.

Occam implementation

Occam is a concurrent language, but most processors (and certainly all microprocessors) are sequential. Occam's concurrency therefore requires some runtime support on current microprocessors to effect the illusion of concurrency. In fact, with a reasonable choice in support parts, limited true concurrency can be obtained with current microprocessors. The system is able to effect interprocessor transfers with a DMA chip while the processor is executing other processes.

Nonetheless, most of the concurrency will usually be accomplished by some runtime kernel. It will provide process scheduling and interprocess communication facilities in the form of either insertional code fragments or as subroutines for the compiler to invoke. A simple implementation is preferred. Because Occam programs written in a concurrent style indulge in substantial communication, there are many opportunities for process scheduling and a simple round robin scheme will often be sufficient.

In reality, a processor will have several levels of hardware-supported pseudoconcurrency, depending on the details of its interrupt structure. To allow the bulk of interrupt handling to be done in Occam, the language includes priority-setting versions of the PAR and ALT constructors so that processes can be given a priority to match the interrupt architecture needed. Implementations will generally

TABLE 4
Concurrent Line Plotting: VLine and Screen

<pre> PROC Vline(CHAN requests,demands)= VAR x,y0,y1,address,bit,going: SEQ going:=TRUE -- a control value WHILE going -- value input with each message to control SEQ requests ? x; y0; y1; going IF y0>y1 swap(y0,y1) address:= (((x>>4)*400)+y0)<<1 bit :=1<<(x\15) SEQ i=[0 FOR 1+(y1-y0)] SEQ demands ! address; bit address:=address+2: </pre>	<pre> PROC screen.write (CHAN hrequests,vrequests,stop)= VAR address,data, contents,going: SEQ going:=TRUE WHILE going ALT -- a specific "stop" channel used to -- halt the process since ALT unnecessary hrequests ? address, SEQ getabsword(screen,address,contents) hrequests? data putabsword(screen,address,contents\data) vrequests ? address, data SEQ getabsword(screen,address,contents) vrequests? data putabsword(screen,address,contents\data) stop ? ANY going := FALSE: </pre>
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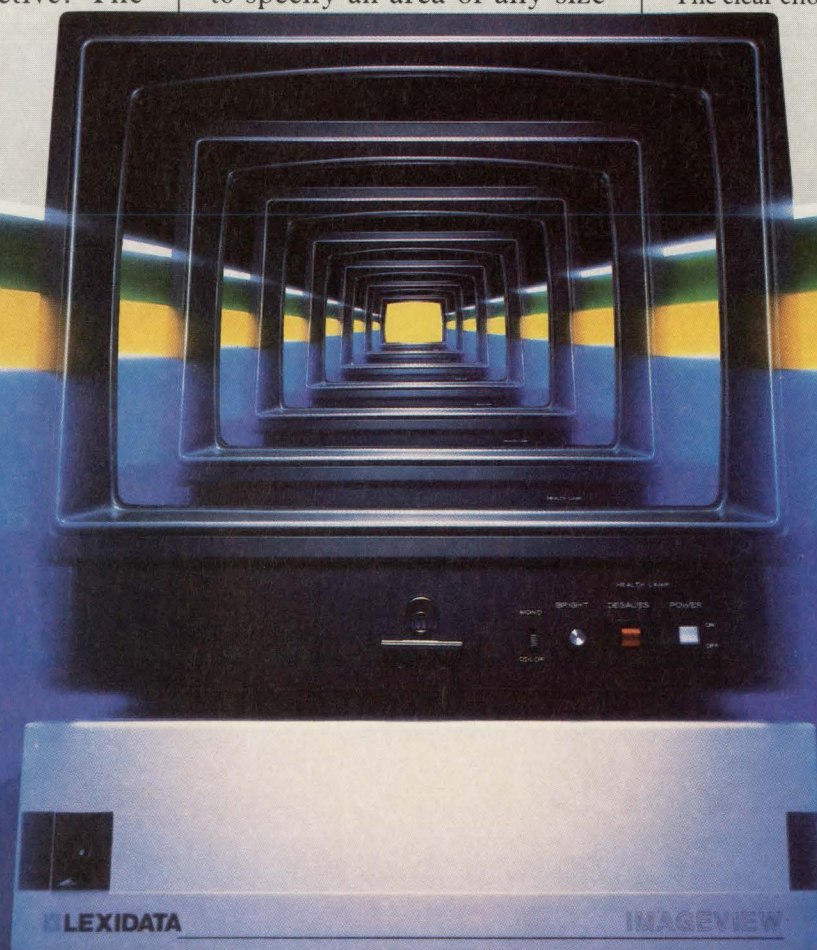
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restrict the number of priority levels to the number of discrete interrupt levels, thus allowing a simple mapping. The two constructors simply assign relative priorities to the processes collected in the order in which they are written.

```
PRI PAR
InterruptHandling
AllOtherProcesses
```

Thus, the above example allows both the interrupt and background processes to proceed in parallel, but ensures that the interrupt handling will preempt the background work when needed.

Considering hardware

Implementing Occam on a normal microprocessor is not difficult. The language's simplicity makes frontend compiler design and implementation straightforward, and the runtime kernel itself can be constructed for most machines in perhaps 200 instructions.

Occam is more efficiently implemented on the Inmos Transputer. This VLSI device is a 250,000 transistor die constructed using a two-micron CMOS process. The Transputer integrates a Reduced Instruction Set Computer (RISC) style pro-

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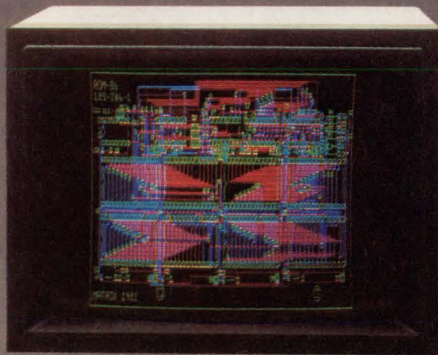
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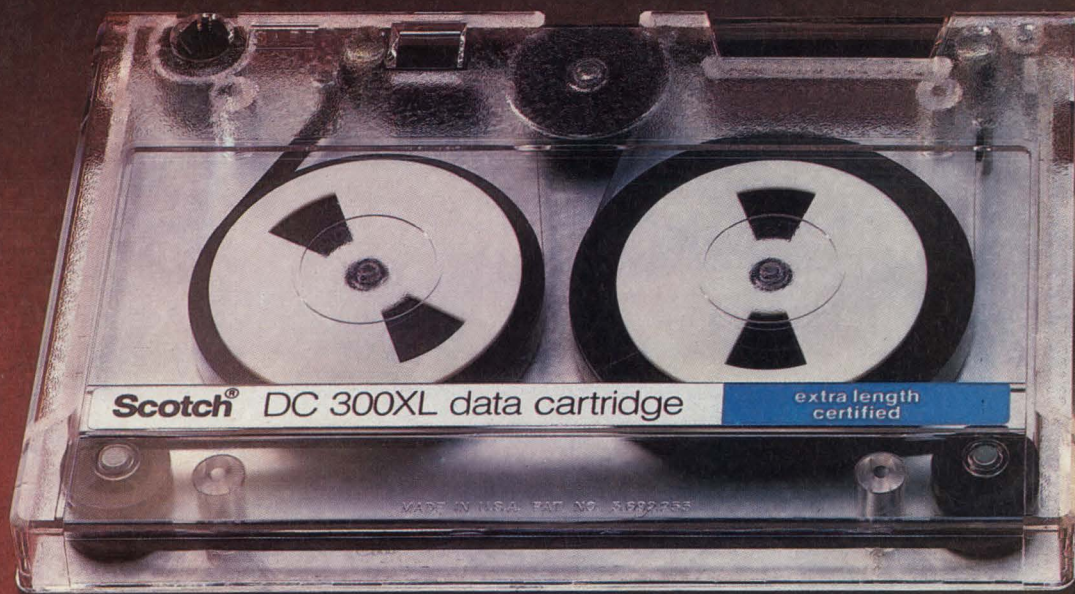
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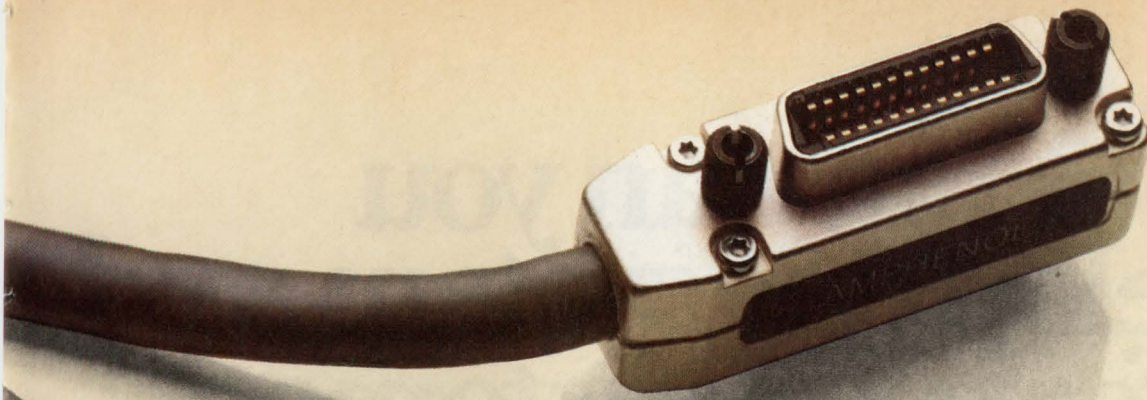
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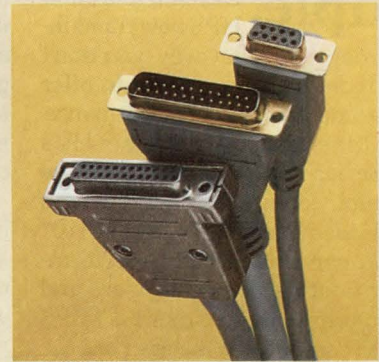
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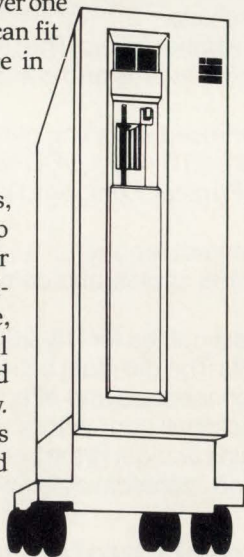
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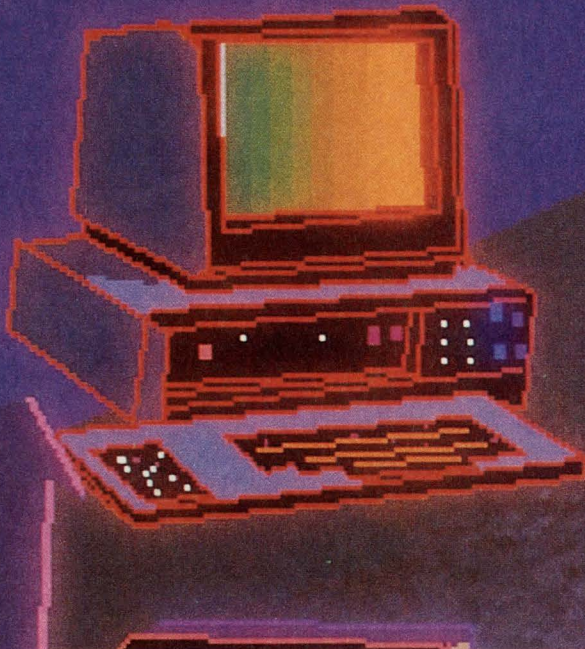
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CIRCLE 64

SPECIAL REPORT:

SYSTEM COMPONENTS '83



For this month's Special Report section, our editors have put together a summary of some of the most significant product introductions of 1983. Selections were based on reader response, company input, and editorial judgment. Each of the five sections has an introduction which looks at technology and product trends that emerged during the past year.

This was a year of progress at both ends of the spectrum—from personal computers to superminis. Artificial intelligence came out of the laboratory and new architectures began to appear. Supermicros, industry standard operating systems, and networks won our hearts and minds with introduction after introduction.

Not to be outdone, peripheral manufacturers continued their drive toward lower cost and higher performance in smaller packages. Disk drives increased storage and speed while shrinking in size, and optical disks offered gigabytes of storage. Nonimpact printers using new technologies entered the market, while dot-matrix printers began to rival daisy wheel units for print quality.

On the integrated circuit front, increasing function density made much of the progress possible. Entire systems appeared on chips. Controllers for disks, printers, and CRTs were joined by modems and other single-chip communication systems. Nonvolatile memory sizes sparked a trend toward silicon software and the first 256-Kbit dynamic RAMs appeared. Full 32-bit micros continued the move toward more processor complexity, and CMOS became a major VLSI contender. For ultrahigh speed, GaAs took a great leap forward with the premier of commercially available functions.

Design, test, and development techniques began to converge. High performance logic analyzers became easier to use and were interfaced directly to development systems. Reasonably priced computer aided engineering workstations appeared on everyone's desk. Even personal computers began to be used as engines for these systems. The year also witnessed the first signs of a long-range trend aimed at connecting everything from initial design to final test. Although such integrated systems are not here yet, the products introduced in 1983 clearly established the trend.

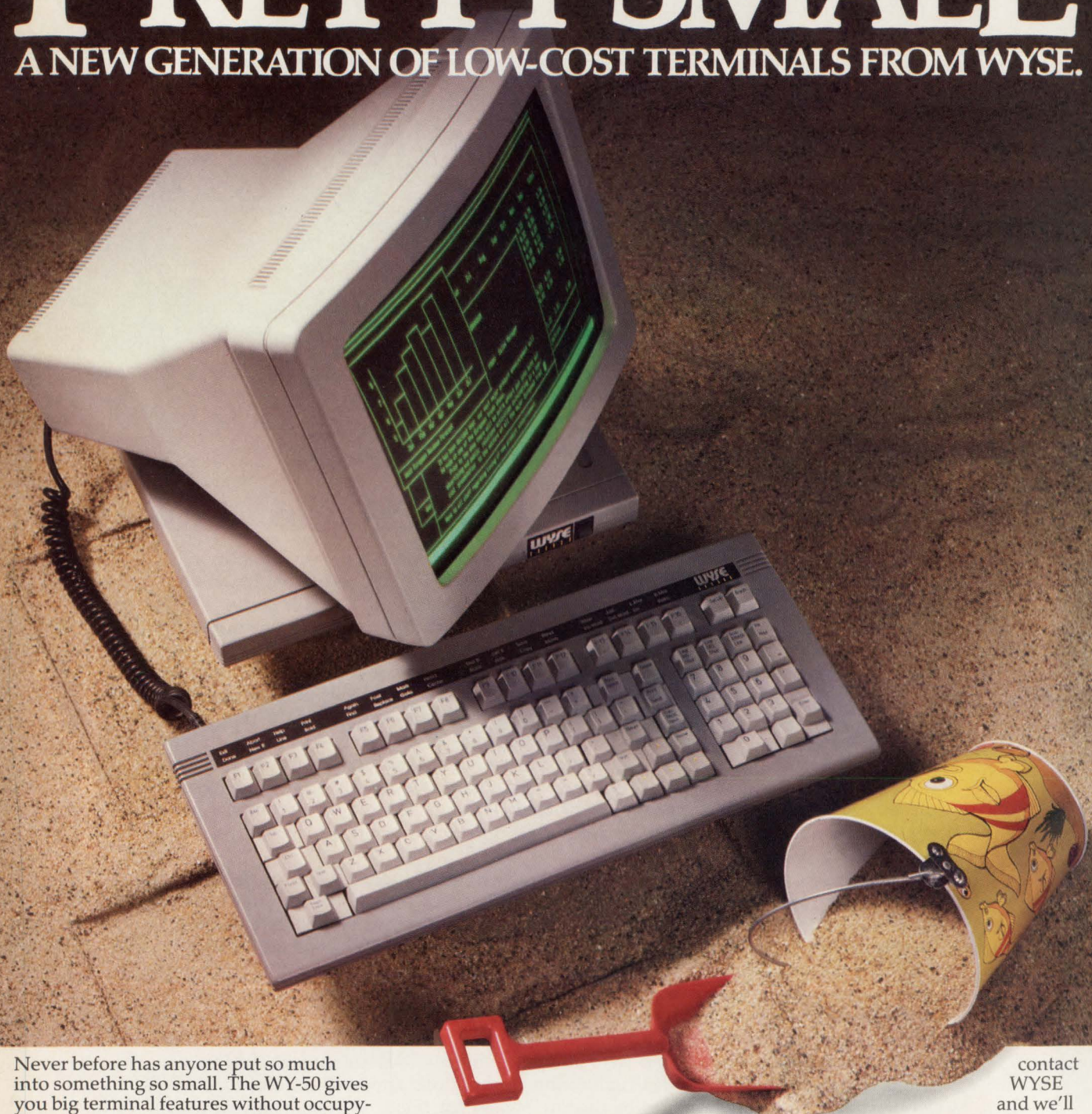
Finally, new packaging, interconnection, and power supply techniques evolved apace with the rest of the industry. Glamourless and unsung, such improvements help make other technological advances possible.

John Bond

John Bond
Senior Editor

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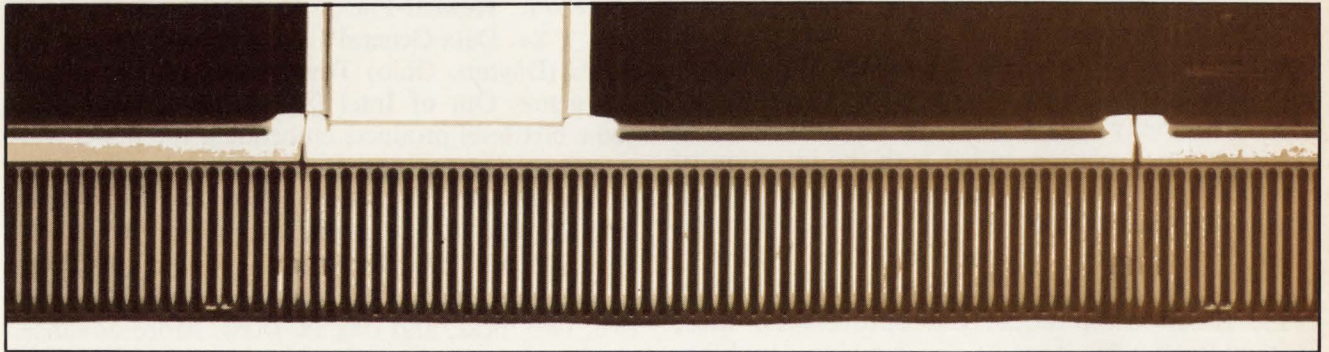
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CIRCLE 66



COMPUTERS TAKE ON NEW FACETS TO MOVE FORWARD



by **Peg Killmon,**
Senior Editor

Computer systems of every type, emerging from every corner, might cause a sense of disarray. Instead, this barrage hangs together. With the swelling stream of disparate systems comes a parallel torrent of software and communication products to tie it all together. Thus, instead of systems, attention tends to be focused on systems of systems.

Fueled in part by the Fifth-Generation projects undertaken by Great Britain, Japan, and the European Commission, recent architectural changes are affecting all systems from personal to mainframe levels. Goals of the Fifth-Generation are to make computers perform more functions, and faster, cheaper, and easier. Architectures aimed to accomplish these goals will spread multiprocessing and distributed systems, and with them communication networks.

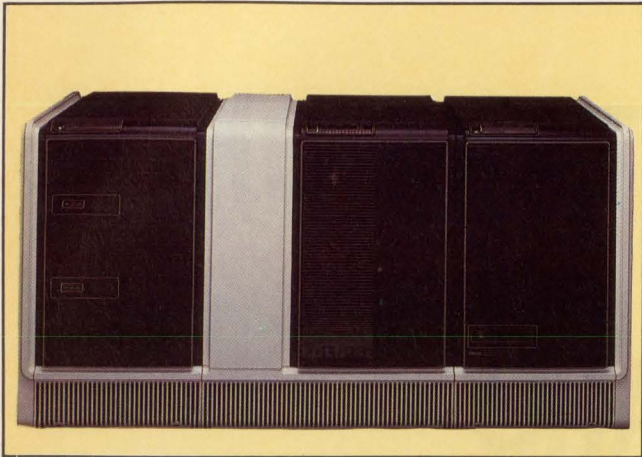
This year's crop

Although the U.S. is not formally involved in a Fifth-Generation project, work continues in the private sector in the supercomputer area. Cray

Research and Control Data Corp (CDC), both located in Minneapolis, Minn, have laid their plans. CDC set up ETA Systems, Inc (St Paul, Minn) to bring out its Cyber 2xx supercomputer.

Growth in the mainframe area continues with Honeywell's (Waltham, Mass) announcement of the DPS 88 and IBM's (Armonk, NY) disclosure of a top-of-the-line 3084 model Q96, an add-on to the 3081 that provides a dual dyadic system. Meanwhile, minicomputers are stretching toward mainframe levels with systems that use parallel processing techniques to push performance levels.

Among this year's introductions, Prime Computer's (Natick, Mass) 9950, Harris Corp's (Fort Lauderdale, Fla) H1000, and Data General's (Westboro, Mass) MV/10000, all use multiple internal processors to raise Whetstone ratings. Parallel processors also appear in Digital Equipment Corp's (Maynard, Mass) VAXcluster systems and in Perkin-Elmer's (Oceanport, NJ) 3200MPS series. These systems provide more power by connecting multiple 32-bit processors together and sharing a data base. A newcomer to the field, Elxsi Systems (Sunnyvale, Calif) extends multiple 68000-based processors over a wide system bus to achieve performance ratings claimed to approach 20 million instructions per second (MIPS).



Data General's MV/10000 takes the power of minicomputers one step further using multiple internal processors.

Multiple processors also play a part in fault tolerant systems. Tandem Computers, Inc (Cupertino, Calif) stood virtually alone in the fault tolerant area for many years with its 16-bit NonStop systems. This isolation ended with the injection of systems from Stratus Computers (Natick, Mass), Auragen Systems (Fort Lee, NJ), Tolerant Systems (San Jose, Calif), Synapse Computer (Milpitas, Calif), and No-Halt Computers (Farmingdale, NY). Based on multiple microprocessors, these systems take advantage of the growing capability of semiconductor technology to economically fill demands for continuous system availability.

Tandem's recently announced NonStop TXP, however, raises the performance threshold. Two to three times faster than previous 16-bit systems, this machine uses two 16-bit processors operating in parallel within the CPU to address high volume, online transaction processing applications. Hewlett-Packard's (Palo Alto, Calif) FailSafe 1000, ties series 1000 systems together in a system aimed at process control. August Systems (Tigard, Ore) uses multiple 68000s in its Can't-Fail computer that meets demands of the industrial control area.

Easier access to data

Other architectural changes stem from the need to make information easier to retrieve. This is the bailiwick of artificial intelligence and knowledge-based systems—other aspects of stated Fifth-Generation goals. Residing in university laboratories, languages like Lisp and Prolog are adept at forming relationships that enable data to be retrieved without requiring special programs to be written. The massive memories and fast processors necessary to store data and calculate relationships previously belonged only to mainframes. Now, these attributes are becoming available on affordable systems, bringing the languages out onto the open market. This year,

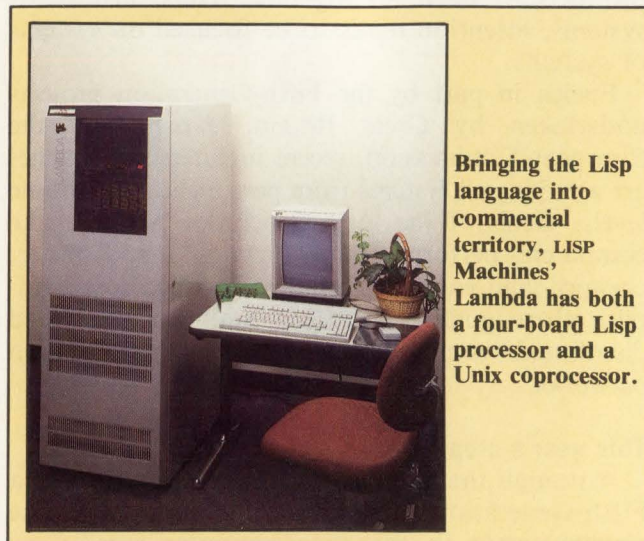
Symbolics (Chatsworth, Calif), and LISP Machines (Culver City, Calif) both produced minicomputer level systems that should make these techniques available on a broader basis.

Minicomputers have not only taken on power and flexibility, they have also continued to shrink in size. Rackmountable 32-bit processors occupying a single board emerged with advances in technology. With these miniature systems came 16- and 32-bit microcomputers housed in desktop packages.

Seizing the opportunity to stretch their area of influence, traditional minicomputer vendors have produced packages that sell for under \$10,000—the seemingly magic mark—yet run standard system software. Personal, yet professional, computers based on existing 16-bit microcomputers have come out. Hewlett-Packard's Model 150, IBM's PC and PC XT, Data General's Desktop Generation, and NCR's (Dayton, Ohio) Tower 1632 are examples of this genre. Out of Intel (Santa Clara, Calif) have come box level products embedding the newer 80286 processor. IBM's newest PC-based workstations further extend Big Blue's grasp on the desktop market. The XT/370 promises to run System/370 VM/CMS code, and the 3270 PC supplies concurrent operation of up to seven sessions (four host interactive, two local, and one PC-DOS). More advanced 32-bit microprocessors are found in NCR's 9300, Hewlett-Packard's 9000 series multiprocessor machines, and DEC's recently announced MicroVAX I.

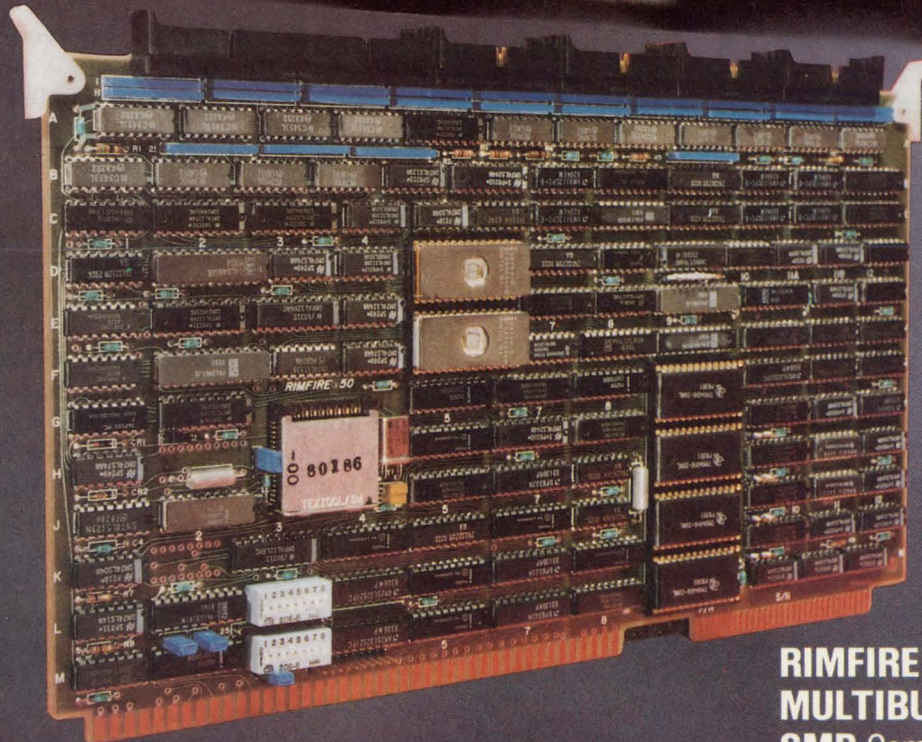
Making the connection

Dozens of vendors have introduced both hardware and software to implement a mainframe to personal computer connection. Making use of the personal computer products in a business-like fashion, the methods range from simple terminal



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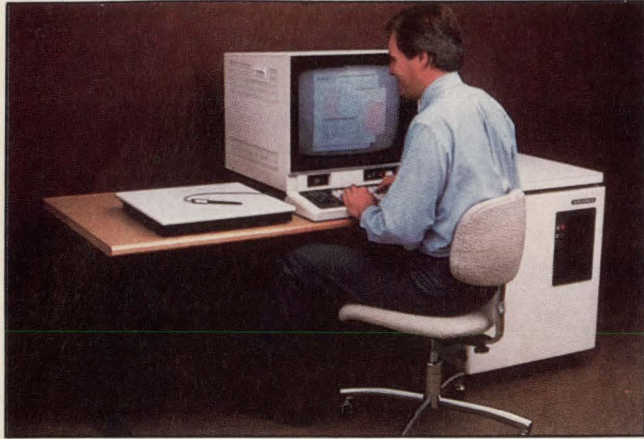
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DN600 workstations interconnect via Apollo Computers' Domain network to share data and processing capability.

emulators to packages that download data from the mainframe, allow the user to manipulate it, and then upload it to the mainframe. Among the vendors of products that accomplish this task are Cullinet Software (Westwood, Mass) with a relational DBMS for IBM PC to IBM mainframe, Intel Corp with a multi-user connection between its DBMS system and microcomputer applications, and Ryan-McFarland (Rolling Hills Estates, Calif) with a Cobol-based software development system that produces software to run on systems ranging from PC to mainframe.

Computer communication schemes, such as local area networks, have resulted in hosts of products.

Local area networks are also proliferating, providing another method to connect the plethora of diverse products with one another. These computer-to-computer communication schemes, whether Ethernet, Omninet, or some other networking scheme, have brought a host of products to market. One of the first to take this tack, Apollo Computer's (Chelmsford, Mass) Domain network uses 68000-based workstations. These nodes fit on a desk, interconnect to share data and processing capability, and provide the power to handle computation-oriented tasks such as computer aided engineering (CAE). CGX Corp (Acton, Mass) links model 2001 terminals together in an independent network to provide both two- and three-dimensional graphics capability.

Other workstations engaged in CAE and computer aided design (CAD) applications include Cadmus Computer Systems' (Lowell, Mass) 68000-based 9000 workstations that interconnect via Ethernet or fiber-optic cables. Telesis (Chelmsford, Mass) takes the

development process from schematic through board design and into production with automatic routing and placement programs and online continuity checks.

One result of this focus on communications is a single-board computer that provides onboard communication hardware and software. Intel's COMMputer serves as an example of how standards can serve in system integration.

Communication plays a role

Standards in all aspects of connection hardware and software already play a major role. The impact will only grow in importance as more complex and more transportable systems become available. In most cases, the missing link is the lack of standard software.

Applied to hardware and to software, standards should remove the need to design special purpose interfaces to connect computers and peripherals to a network. Likewise, communication software and application software will not need revisions when hardware is upgraded.

Developments of interest to those trying to cope with integrating unlike systems include the cooperative effort displayed between major micro-processor manufacturers and Western Electric. This group intends to port the Bell Labs' Unix System V operating system to chip, board, and box-level products, thereby making application programs portable between products.

This move will guarantee future integrators that products will move from one vendor's equipment to another's. It also solidifies Unix's position as a standard operating system—a move looked on with enthusiasm by the many manufacturers that have adapted Unix for use on their minis and micros.

While Ada was developed as a standard language by government decree, Unix followed the path of common hardware standards and rose because of user acceptance. Although many versions of the product exist, they all take Unix as their base, working out in individual ways the recognized problems with file handling and communications. Ada is also taking its rightful place. Data General and ROLM Corp (San Jose, Calif) worked together to produce a compiler that received its validation certificate in June. Intermetrics (Cambridge, Mass), although delayed, plans to release a production quality optimizing compiler in Nov 1984, and SofTech Inc (Waltham, Mass) intends to deliver its compiler in July 1984.

With projects like these bearing fruit, there is a sense that "everything's falling into place." Efforts being made to achieve standards in all areas will surely lead to easy access of expanded resources.

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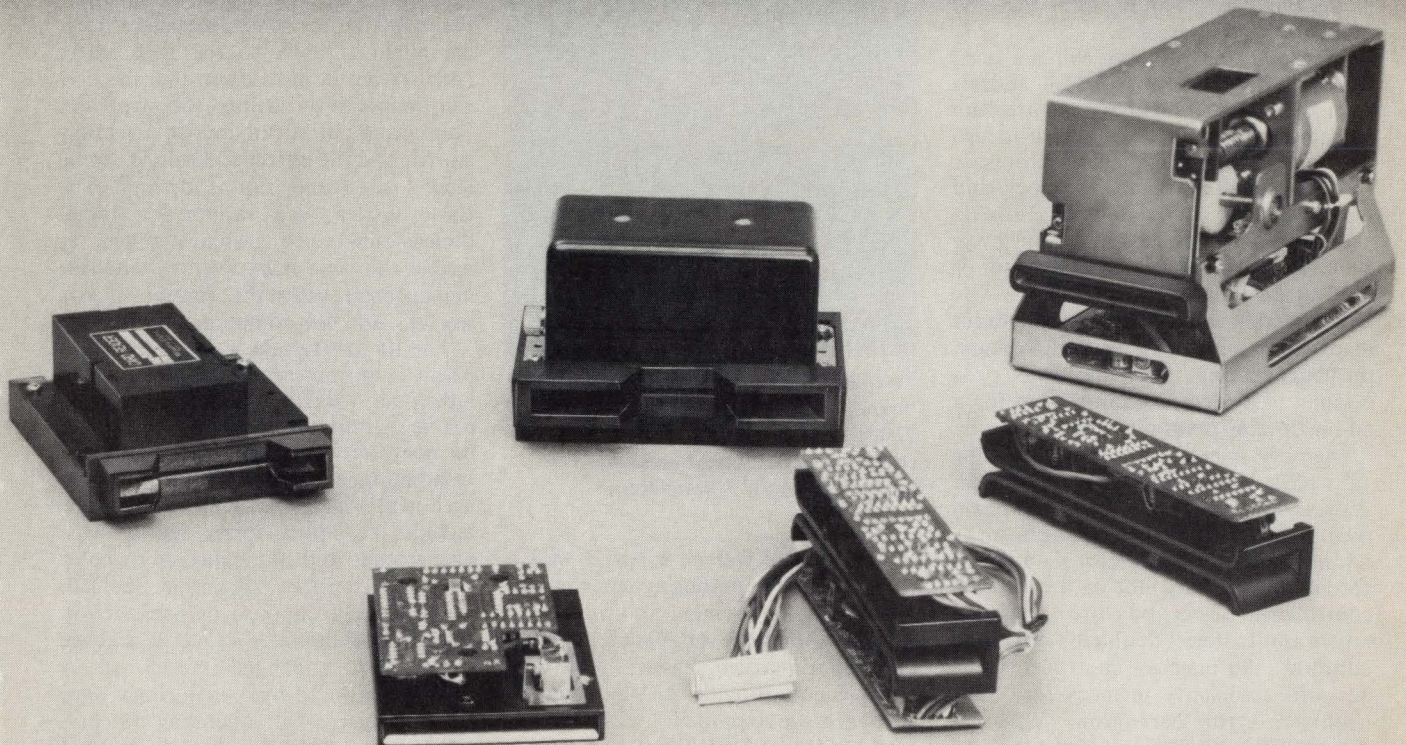


Model Number	Card Standard
Manual Magnetic	
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ZU-1402	IS02 (ABA)
ZU-1420	IS01/IS02
ZU-1601E	IS01 (IATA)
ZU-1602E	IS02 (ABA)
ZU-1601	IS01 (IATA)
ZU-1602	IS02 (ABA)
Magnetic Encoders	
ZU-2401	IS01 (IATA)
ZU-2402	IS02 (ABA)
Automatic Magnetic	
ZU-1507	IS02 (ABA)
ZU-1521	IS01 (IATA)
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ZU-XXXHR*	Type II, III
Vertical Optical Reader	
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Five-chip set packs mainframe power in compact station

A 32-bit single-user computer, the HP 9000 is available as a completely integrated desktop workstation, as a rack-mounted module, or in a standalone cabinet for building industrial and multi-user systems. Internally, it can be configured with up to three of the 32-bit CPU cards, as well as with one or more I/O processor cards, all of which can be plugged into the system's card cage.

The set includes CPU and clock chips, both on the CPU board; a 128K-bit RAM chip and a memory controller used in the 256K-byte memory boards; and an I/O processor chip. The I/O processor provides eight I/O channels per card with DMA transactions supported between all channels and the memory processor bus. This chip is microprogrammed with 4.5k 38-bit words of resident control store. In addition to the DMA transactions, it simultaneously handles CPU I/O and generates CPU interrupts.

The 450k transistor CPU chip is a stack oriented processor with 32-bit address and data buses. It handles pipelined data transfers at 36M bytes/s, which is also the bandwidth of the memory processor bus or system backplane. The clock chip generates two nonoverlapping 18-MHz signals to drive the CPU at a 55-ns cycle time. At these speeds the processor is able to execute 1M instructions/s. The 230-opcode instruction set includes instructions for IEEE math formats, multiprocessing, and multiple processors. A typical execution time for a 64-bit floating point multiply is 10.34 μ s.

Memory is provided on boards using HP's 128K-bit RAM chip in increments of 256K bytes for a maximum system main memory of 2.5M bytes. Each memory address contains 32 bits for data plus 7 for Hamming codes used by the memory controller to detect and correct single-bit errors and to detect double-bit errors. In addition, the memory controller has a 32-word associative memory for "self-healing" error correction. When it detects single-bit errors, it stores the correct contents in an associative word.

Any subsequent accesses to the defective address are automatically directed to associative memory with no performance loss. Double-bit errors or other malfunctions cause the memory controller to map

a 16K-byte block of memory out of the system, thus preserving system integrity.

A 12-slot card cage is cooled by a single muffin fan. Heat is dissipated by means of the circuit boards called "finstrates"—"fin" because the copper-core, Teflon coated boards serve as heat sinks or cooling fins, and "strate" because the chips are bonded directly onto the boards, which thus serve as the chip substrate.



Five-chip set in foreground mounts on boards (above chip set) as nucleus of 32-bit HP 9000 computer. Module in center is rackmounted version; background unit is standalone workstation.

The HP 9000 can be supplied with a choice of two operating system environments: an HP version of Unix with extended functions, or a tailored version of HP's Enhanced Basic. HP-UX, the Unix version, provides a Unix System III software environment with virtual memory for both programs and data. A maximum virtual address space of 1G byte can be allocated per process with up to 500M bytes of that space available for local code and data, and up to 500M bytes for shared system code. In addition to Fortran and Pascal, HP-UX supports

the Graphics/9000 family of display and design graphics.

A device-independent graphics language provides fundamental graphics functionality, output primitives, and color modeling. An advanced graphics package incorporates ACM Siggraph Core compatibility, two- and three-dimensional viewing, and clipping. Picture segment support with an "operator pick input" function allows interactive manipulation of graphics images.

An Enhanced Basic language system provides a single-user operating system environment with multiprogramming and job scheduling. Basic includes both an interactive editor and extensions aimed at engineering activity. Basic is implemented as a runtime compiler. Running a program in source code initiates line by line compilation, and only the first iteration of a loop is compiled—thereafter, the loop's source code is executed. After compilation, both source and object code remain in memory so that the user can interactively debug the program. Source and object can then be separately stored, and the object code alone can be later loaded and run if desired. The Basic system also supports a three-dimensional color graphics system as well as the same IMAGE/QUERY database management system that runs on HP 3000, 1000, 250, and 9845 computers.

The HP 9000 system is designed to put 32-bit mainframe computations into an individual workstation. It is also configurable within the card cage for CPU, memory, or I/O intensive applications. In addition, the card cage can be packaged in the OEM desktop model 20, which includes keyboard floppy and/or hard disk storage and monochrome or color CRT, and is priced starting at \$28,250. The card cage can also be packaged in the OEM rackmounted model 30 and the minicabinet packaged model 40. A model 40 with 1M-byte RAM, single CPU, and multi-user HP-UX operating system is priced under \$45,000. **Hewlett-Packard Co.**, 1820 Embarcadero Rd, Palo Alto, CA 94303.

—Tom Williams,
West Coast Managing Editor

Circle 260

REAL TIME AT THE RIGHT PRICE: NOW YOU CAN RENT THE MC68000 EMULATION PACKAGE.



The HDS-400 is the most versatile emulation system available for Motorola's 68000 series micro-processor. And now you can rent this system from Leasametric, the foremost renter of quality electronic test equipment.

Speed, simplicity and power. The HDS-400 runs up to 12.5 MHz clock speed, the fastest today. And it performs real-time emulation and analysis at clock speeds up to 10 MHz with no wait states. So you can gauge your prototype's true performance.

This emulation system is unique. It can download both the target system code and the debugging system from either the Motorola EXORmacs™ Development System, DEC VAX™ or Motorola VME/10 as hosts. The HDS-400 can serve as a fully functional substitute for the MPU in your target system. And its analysis commands are straightforward, so you can rapidly debug and integrate your target system.

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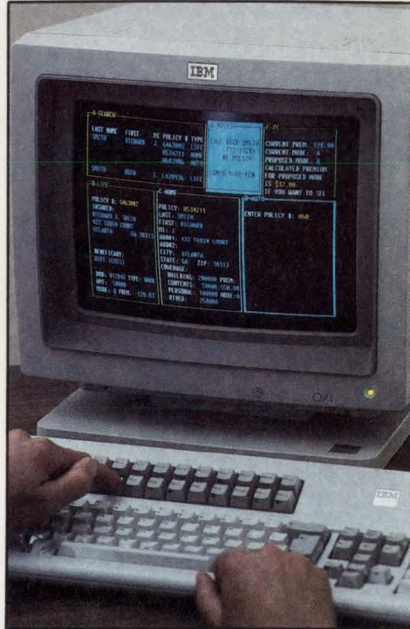
CIRCLE 69

IBM offers mainframe PC and terminal that does windows

An IBM/370 on a chip it is not. Coming very close to that concept, though, is a new version of the IBM PC that can run, create, edit, and generally manipulate software programs that have been written for the IBM/370 mainframe computer. The XT/370 connects to a host computer running System/370 virtual machine/conversational monitor system (VM/CMS) application programs, and brings them to the desktop system for processing. This system is really three workstations in one: a standard IBM PC, VM/CMS workstation, and an IBM 3277 display terminal that attaches to a host computer. Currently, it is a single-user workstation that has up to four million characters of virtual memory.

The XT/370 consists of the IBM PC XT with more than 250,000 characters of memory, a display unit, diskette drive with a 360,000-character capacity, a fixed storage unit that can hold either 10 or 20 million characters and three new cards within the PC that allow the computer to run /370 software. The processor card houses three microprocessor chips—two 68000s, of which one is an IBM custom design, and a third chip that is a custom IBM 8087. The first two micros execute data and control instructions for /370 fixed point software, while the Intel-based 8087 executes System/370 floating point instructions.

The second memory card provides an extra quarter million bytes of storage. It



has up to four million characters of virtual memory for interactive computing in the VM/PC mode of operation. The card also expands the available memory in the PC XT mode to 655,360 characters. The third card, a controller card, provides the coaxial attachments that enable the unit to act as a 3277 model 2 terminal when connected to a host computer by an 3274 display control unit. The IBM PC XT/370 will be available in the second quarter of 1984 and will start at \$8995

for the 10-Mbyte storage version and go up to \$11,690 for the 20-Mbyte option.

In direct competition to Apple's Lisa, IBM also introduced the 3270 Personal Computer (photo) which allows users to work on seven concurrent sessions in the display. Through a windowing function, portions of all seven sessions can be viewed on the screen simultaneously. What's more, any one session can be zoomed for full-screen view or scrolled vertically and horizontally. In addition, its data can be interchanged with data in any one of the other sessions.

The 3270 comes with a high resolution color monitor (720 x 350 pixels), which enables data to be highlighted in one of eight colors in any of the windows. The terminal uses a 122-key keyboard that combines both the functions of the IBM PC and the 3270 terminals. Thus, on the display the user can have both word processing sessions using DOS 2.0 application programs in one window, and VisiCalc financial and mathematical data in the other. Data from either window can be interchanged with the other. The 3270 comes in three model choices with prices ranging from \$4290 to \$7180. The color monitor sells separately for \$995. **IBM Corp, Information Systems Group, 900 King St, Rye Brook, NY 10573.**

—Nic Mokhoff, Senior Editor

Circle 261

Parallel processing scope snowballs with ring technology

Cyberplus multiprocessors offer a performance of 650 million instructions per second, and 65 million 64-bit floating point operations per second. This system incorporates a ring concept that allows expansion to the point that 64 processors can be used to run one application. This technique provides system speed, accuracy, and flexibility.

An interconnected network of individual processors makes up the ring technology used in the Cyberplus

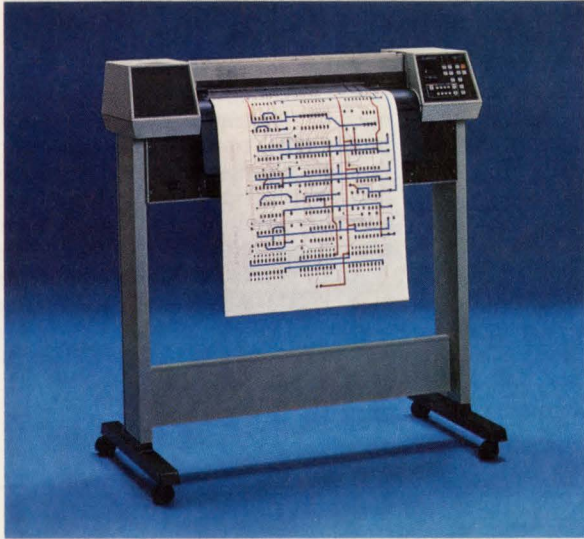
system. Linked to the series 800 computer, the ring forms a high speed communication channel for interprocessor control and data transfer. All processors are directly interconnected via the interface that the ring port function unit provides. Sustained data transfers occur concurrently among all processors at 800M bps per ring, and read/write operations from processor to ring occur at the same rate. A multiple processor system would then have an interpro-

cessor transfer rate of 1.6G bits multiplied by the number of processors.

Up to four rings can connect to computer memory, with up to 16 processors per ring. This allows 64 processors to run on a single series 800. In this maximum configuration, all processors operate independently and can execute on every clock cycle. The memory capacity of each processor is 256K 64-bit words expandable to 512K 64-bit words.

(continued on page 142)

Now you have a choice!



The best way to make the HP 7580 better was to make it bigger.

You asked for it!

Ever since its introduction two years ago, the HP 7580 Drafting Plotter has enjoyed an unparalleled reputation for price/performance excellence. User reaction has been overwhelmingly positive.

But some of you wanted *more*, and expressed the desire for even *larger* plotting capabilities. And now Hewlett-Packard has met your challenge.

The new HP 7585 Drafting Plotter maintains *all* of the many benefits of the HP 7580. The significant difference is the ability to output plots up to 36.5" x 48"

Now, *both* plotters can:

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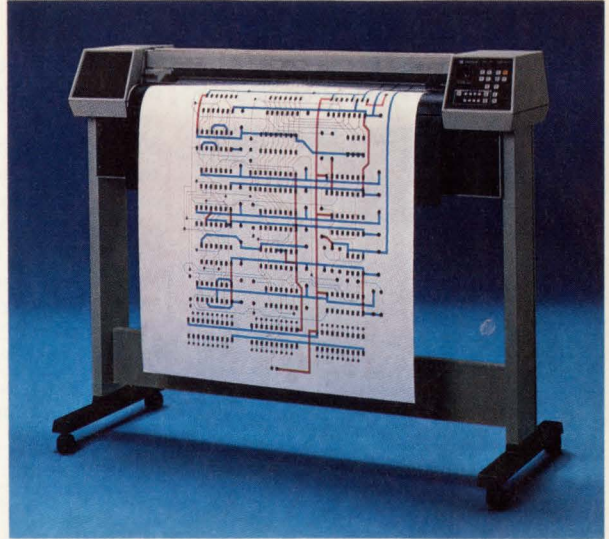
and other ASCII computers with RS-232-C or IEEE 488 (HP-IB, GP-IB) interfaces. (Both interfaces are standard on each plotter.) Also, a new capability for both plotters is modem operation for remote or timeshare applications.

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Give you high throughput and quality output.

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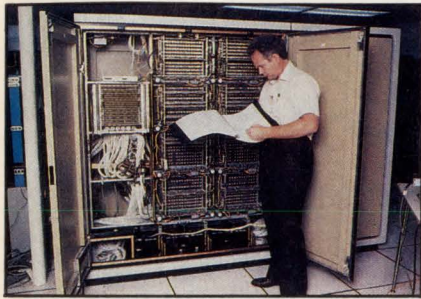
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Phone Number (____) _____

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Parallel processing*(continued from page 140)*

Two processors are available: a 16-bit integer unit and 32- and 64-bit floating



point units. The integer processor has 15 independent functional units. They perform 8-, 16-, and 32-bit mathematics and each accepts operands and output results every machine cycle (20 ns). A control functional unit executes an instruction every machine cycle and each instruction, in turn, can start up multiple functional units. Floating point processors extend the integer processor with 32- and 64-bit capability by adding three floating point functional units. A crossbar allows output of one unit to be passed and act as input to another unit(s).

System software interfaces with application programs running under the NOS2 operating system to load code into the processor(s), transmit data between the host and processor(s), and start and stop tasks. For software development, a cross assembler, an instructor load simulator, and a Fortran cross compiler are provided.

An entry level base processor is priced at \$735,000 including a 16-bit integer unit and 256K words of memory. **Control Data Corp**, PO Box 0, HQN10V, Minneapolis, MN 55440.

Circle 262

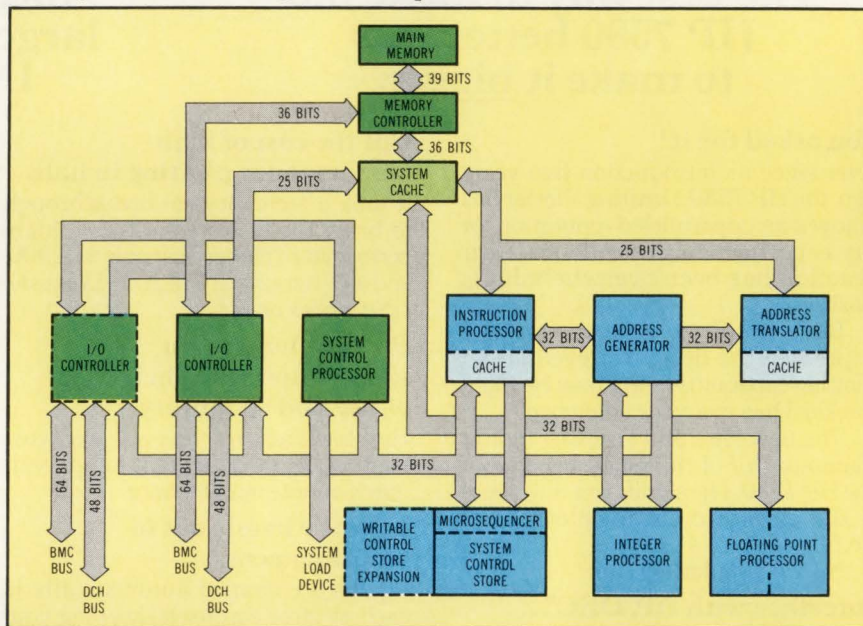
Superminicomputer doubles previous high end performance

Key features of Data General's latest bid in the mainframe-class superminicomputer arena include highly pipelined parallel architecture, Advanced Schottky TTL, fast static RAMs in dedicated caches, and hardware design innovations including a "board-slice" floating point processor and separate address generator. While doubling the performance of its earlier high end MV/8000, the company has cut cycle time in the Eclipse MV/10000 from 220 to 140 ns.

The 32-bit virtual memory machine gleans 2.5M-Whetstone/s double-precision performance for up to 192 users. This is backed by 16M-byte main memory, 18.5G-byte online storage, 4G-byte virtual address space, and 2G-byte program size. Cross development of AOS/RT32 realtime and AOS/VS virtual storage operating systems accommodates CAE and technical timesharing as well as real-time computational applications.

Two identical boards compose the floating point unit, which divides the execution task by using one board for single-precision (32-bit) and both boards for double-precision (64-bit) operations. Parallel design dedicates separate hardware ALUS for mantissa, sign, exponent, and multiply/divide functions. Accuracy is improved through 72-bit wide data paths that allocate 56 bits to the mantissa and 8 bits to the exponent, with 8 guard bits.

Four pipeline levels in the instruction processor provide for concurrent fetch, decode, and execution of macroinstructions. Each instruction sequence is carried through the pipeline in various stages of completion, with one exiting every 140 ns. The directly mapped instruction cache acts as a 4K-byte, lookahead/lookbehind buffer for the instruction stream, fetching 32 bits every



Dedicated pipelines, caches, and buses allow Data General's Eclipse MV/10000 subsystems to operate concurrently with minimal contention. Microcode has been extended from 80 to 104 bits to take advantage of expanded system organization and provide better control of parallel operation.

70 ns. Lookahead buffering prefetches and stores instructions from the system cache before they are executed—to improve performance in sequential instruction streams. Lookbehind buffering retains instructions after they have been decoded, reducing execution time for program loops.

A dedicated address generator creates logical addresses from the instruction stream and converts them to physical memory addresses. It operates concurrently with other processing subsystems so that operand fetches can overlap instruction execution. It also contains its own 32-bit ALU and register file that is

accessible to the instruction processor. This register file supports a fifth pipeline level that allows macroinstructions to reference a logical memory address within one 140-ns cycle. Under microprogram control, the address generator performs 32-bit arithmetic to offload the integer processor.

MV/10000 is hardware and software compatible with other Eclipse MV family computers. Languages supported include Fortran 77, PL/1, Basic, C, and Pascal. A basic system costs about \$211,000. **Data General Corp**, 4400 Computer Dr, Westboro, MA 01580.

Circle 263

"TWICE THE POWER FOR TWO-THIRDS THE COST."



*Jerry Sabath, Project Manager,
Applicon*

Applicon wanted to make still another mark in CAD/CAM.

They wanted to build a lower cost, compact, desktop workstation to use with their state-of-the-art Series 4000 CAD/CAM system. A unit that could deliver

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Tall microcomputer builds on standard subsystems



The 29" (74-cm) high Tower 1632 is built around a 16-bit 10-MHz MC68000 processor, a Unix III based operating system, a Multibus I/O subsystem, and fixed Winchester drives. The MC68000 supports up to 16 simultaneous local or remote users, each performing multiple functions. Up to six microprocessor based DMA controllers that handle the 5¼" disks, eight-channel I/O, and multiprotocol communications offload I/O functions from the CPU. Up to 2M bytes of main memory in 256K-byte increments and 60M bytes of Winchester disk mass storage in the main unit are supported. Add-on units can expand mass storage to more than 1G byte. Standard magnetic media interfaces include the SA400 for 1M-byte 5¼"

floppies, the ST506 for 10M-byte Winchester, an SMD for 8" Winchester, and the QIC II streaming tape. The six-slot Multibus I/O system is separate from the dedicated two-slot high speed memory bus. The buses function both simultaneously and independently to minimize contention and maximize throughput. Unix optimized memory management unit with 256K ECC memory uses a full 24-bit addressing field and provides a clear migration path to 32-bit technology.

Five "menu personalities," one for each of five programming sophistication levels, are part of the enhanced Unix. These personalities allow easy access to the system. To facilitate applications development, NCR's N-GEN dictionary-driven applications generator contains the needed software tools to generate quick computer programs. Cobol, Business Basic, Fortran, and C

languages are supported. Two RS-232-C ports provide ASCII teletypewriter and Bisync 2780/3780 communications. Other protocols supported are NCR's DLC, SDLC/SNA, X.21/X.25, and Unix networking.

Carrying features beyond industry standards, the Tower 1632 includes a power fail recovery system that preserves data in memory (without specialized applications programming) until power is returned after an outage. In addition, the intellectual properties protection system prevents both proprietary operating and applications software from running on unlicensed machines.

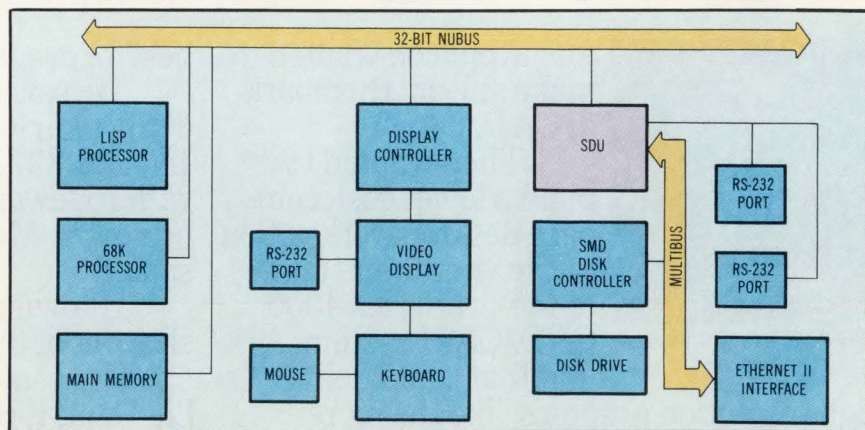
The \$12,000 Tower 1632 will be sold to computer systems houses, OEMs, distributors, and dealers who can add applications software, specialized peripherals, and other subsystems to suit customized needs. **NCR Corp.**, Dayton, OH 45479. **Circle 264**

Computer uses Lisp microcompiler to speed application processing

The Lambda computer achieves faster results by swapping speed-critical portions of an application program directly into the control store. A microcompiler converts already assembled Lisp object code into microcoded equivalents, thus simplifying microprogramming tasks.

The computer's flexibility also extends to its hardware design. A high speed bus primarily handles processors and memory devices, while slower peripherals such as disk drives and printers reside on a separate Multibus backplane. A system diagnostic unit (SDU) supervises interbus communications and automatically monitors the status of installed devices.

In addition to microcoding high speed application program sections, the microcompiler can be used for application-specific instruction sets and to secure proprietary software. Users can directly address 52K words of the 64K-word virtual control store memory without regard to the control store's actual size (a limitation in previous machines). Because 12K words are reserved for system programs that remain at all times, paging techniques load only 16 word segments at a time from disk into the 16K-word physical memory.



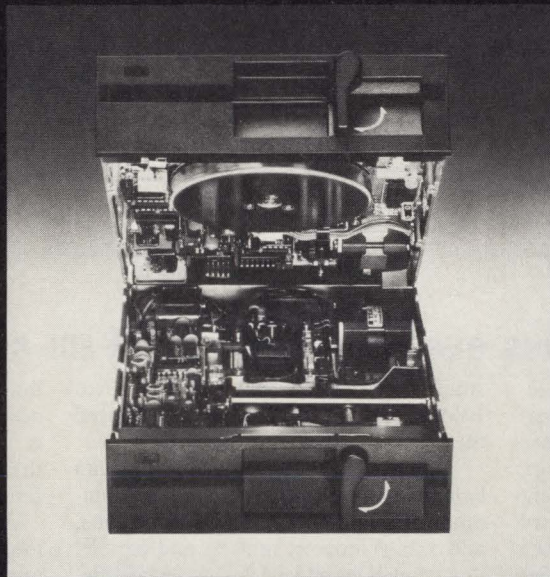
The SDU receives peripheral service requests from processors residing on Nubus. The unit schedules the necessary actions on Multibus peripherals, and returns the necessary acknowledgments upon completion.

Such microcompilation techniques more than double performance speeds as compared to conventionally compiled Lisp programs, according to the company.

A \$72,500 single-unit Lambda computer includes a 256K x 32-bit main memory with error correction, one 470M-byte storage module drive (SMD) type disk drive (the SMD disk controller

can handle four drives), a 16 x 16 matrix multiplier, and an 800- x 1024-pixel black and white display with mouse. Delivery is quoted at 8 to 12 weeks. A 40-bit version with 32-bit floating point arithmetic and 21.5G-byte virtual address space is expected early next year. **LISP Machine, Inc.**, 3916 S Sepulveda Blvd, Culver City, CA 90230. **Circle 265**

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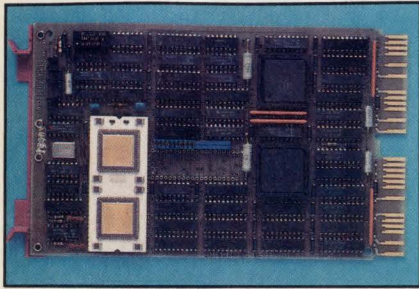
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CIRCLE 72

Advanced Q-bus offerings heighten single-board performance



A "new generation of Q-bus products" includes a board-level microcomputer with PDP-11/70 performance and a high speed peripheral processor to offload the Q-bus, an upgraded Falcon single-board computer, and an extension of Micro-power/Pascal that runs under VMS or RSX-11 operating systems in a multi-user environment.

For computation intensive applications, the most important of these Q-bus products is the -11/70 on a board, the

LSI-11/73. This is the first product built around the 20-MHz J-11 microprocessor introduced a year ago. Built on the same dual-height size module as an -11/23, it has four times the power. The J-11 microprocessor engine for the -11/73 has 32-bit internal and 16-bit external data paths and onboard floating point hardware. The J-11 also has onchip a four-level pipelined architecture, cache support, and memory management implemented in VLSI CMOS.

The LSI-11/73 is a powerful microcomputer with 22-bit memory addresses (4M bytes), 46 FP-11 single- and double-precision hardware floating point instructions, PDP-11/70 system registers, 8K-byte cache, and Q-bus interface. All PDP-11 operating systems can be run on the LSI-11/73 and, for the first time, Unix is sold and supported by DEC.

To increase throughput, the KXT 11-C peripheral processor was developed. This

single-board computer is based on the T-11 microprocessor and functions as an intelligent controller. With synchronous and asynchronous interfaces, parallel interface, and a two-channel DMA controller, the KXT 11-C is optimized to handle communications processing from a wide variety of DMA devices. This frees the arbiter CPU to perform other functions. In very I/O intensive applications, as much as an 80 percent gain in throughput can be achieved by using the KXT 11-C.

Up to 14 of the units can be added to the same Q-bus configuration. Only minor application software changes are needed. RT-11, RSX-11M, and Micropower/Pascal have utilities and drivers to support the board. **Digital Equipment Corp, OEM Group, 77 Reed Rd, Hudson, MA 01749.**

—John Bond, Senior Editor

Circle 266

Minicomputer expedites execution with 100K-ECL circuitry

The Harris 1000 computer system, designed with 100K-ECL technology, features a 4-MIPS Whetstone performance while using less power than earlier ECL circuitry. This advanced technology, combined with hardware for virtual memory and transcendental functions, gives the system a high speed application base that includes scientific and industrial areas.

The basic system configuration includes a CPU with 6K bytes of cache, 16 external interrupts, a line frequency clock and an interval timer, the VOS operating system, and dual cabinets. In addition, special functions are performed by the maintenance aid processor (MAP), the integrated memory subsystem (IMS), and the communication network processor (CNP).

As a separate microprogrammed processor, the MAP runs power-up diagnostics and checks memory, I/O channels, and CPU data paths before loading microcode. The IMS combines the memory controller with 1.5M bytes of memory on a

single board (with capacities to 12M bytes) for both main and shared memory.

Each CNP in the system (up to 14 can be added) simultaneously supports communication via async, sync, isochronous, and X.25 protocols. IEEE-488 and parallel line printer interfaces are also available. Single-board CNPs support up to 16 com-

munication lines for local or remote device connection. In addition, each line is individually programmable and has the ability to concurrently support different protocols at different speeds.

A soft control store implements the CPU microcode for instructions in RAM instead of PROM. Volatile RAMs are automatically loaded each time the machine is powered up. Any time the microcode is enhanced, the control store can be updated by distributing new microcodes.

The system's virtual memory is demand-paged and totals 48M bytes (configured in 3K-byte pages). The CPU includes one virtual address register for each page to track virtual to physical memory relationships.

Additional high speed features include pipeline processing, which allows seven instructions to be processed simultaneously with a CPU cycle time of 75 ns. Precisions ranging from 32-bit single precision to 96-bit quadruple precision are also possible with the system.

The basic system 1000 is priced at \$250,000. **Harris Corp, Computer Systems Div, 2101 W Cypress Creek Rd, Ft. Lauderdale, FL 33309.**

Circle 267



KONTRON Logic Analyzer/Slave Emulator

Your Most Powerful Micro Development Tools Have Been Combined

Now you can have timing and state logic analysis, slave in-circuit emulation, and full software development capability in one powerful, economical system. And, KONTRON's new Logic Analyzer/Slave Emulator (LASER) system can be configured to match your needs. With 32-, 48-, or 64-channel logic analysis to 100 MHz. With built-in dual 5¼" disk drives. With disassemblers, microprocessor interface, and slave emulation for all popular 8- and 16-bit chips. And, with all of the software development tools and ease-of-use features of the KONTRON/FutureData 2300 Series development system at your command, running under CP/M®*. With the flexible LASER system, you can reduce your investment in new development tools by as much

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Lisp-based machine solves artificial intelligence problems



Previously, massive artificial intelligence problems had to be solved with a mainframe computer. Now a superminicomputer from Symbolics can be used, promising significant price/performance advantages. This Lisp-based computer system is a high performance interactive workstation designed for symbolic rather than numerical processing.

It has a 36-bit tagged architecture with 32-bit data paths, and executes programs at an average of 1M high level instructions/s. Virtual memory contains

1,048,576 pages of 256 36-bit words. Basic system hardware features 2.3M bytes of MOS memory with ECC; one parallel and three standard serial I/O ports; a 10M-byte Ethernet interface, a graphics console that includes display, keyboard, and three-button mouse; and a 169M-byte SMD-compatible Winchester disk drive. Each memory board has single-bit error correction and double-bit error detection. Up to 15 memory boards can be installed in the standard chassis for a total of 34M bytes of main memory.

Hardware options include 1280 x 1024 high resolution color graphics display, with 8-, 16-, 24-, or 32-bit/pixel mapping at up to 10 bits/color (R,G,B); floating point accelerator; and 9-track tape drive. Also available are a 20M-byte cartridge tape drive; 1200-baud auto-dial/answer modem; 470M-byte Winchester or 300M-byte removable media disk drive (up to four); IEEE 796 (Multi-

bus) interface bus; and 10-page/min laser graphics printer.

An extensive, interactive programming environment includes sophisticated display system with multiple, overlapping windows for the black and white and color displays; realtime editor; and incremental compilers.

Zetalisp, an enhanced version of Lisp, is the primary language. Flavors, an object-oriented programming language, transcends essentials of Smalltalk in a manner fully integrated with the Zetalisp system. Fortran-77, C, Pascal, and Interlisp are also supported.

Zetalisp provides a single-level (virtual) memory system that automatically allocates memory space and reclaims memory space no longer needed by the running program. The system uses symbols or objects, with each symbol assigned to its own memory space. No syntactic or semantic distinctions are made between the system programming language and the application programming language. **Symbolics, Inc.**, 9600 De Soto Ave, Chatsworth, CA 91311.

Circle 268

Personal mainframe suggests alternative to time-sharing

The Canaan computer uses a new operating system giving users access to IBM System/370 VM/CMS software allowing individual time-sharing capabilities. System architecture runs /370-based programs, yet provides integrated graphics, concurrent processing, and a multi-window display—capabilities that the /370 architecture does not support.

Key to the computer is a proprietary, virtual memory operating system. It allows transparent file and data access across the network over a 10M-bps Ethernet link. Consequently, this parallel system does not need its own file system or I/O recovery. The virtual memory address space is 16M bytes with the number of concurrent processes/mode limited only by the memory capacity. Main memory capacity ranges from 1M to 4M bytes of RAM with ECC.

At the system's heart is a 32-bit proprietary processor that executes the IBM /370 instruction set in native machine code. Furthermore, the system architecture provides two buses. A 32-bit data

bus with 24-bit addressing supports the main processor and memory. Functionally, it transfers data and speeds program execution. The standard 16-bit Multibus supports the I/O processor and increases throughput. A separate microprocessor is used for I/O, device control, and network access.

One or two high resolution bit-mapped displays, each with a graphics controller, provide both portrait and landscape orientation. A 15" or 17" green and black display provides 1024-x-768-pixel resolution. A detached keyboard supported by the I/O processor has three sets of function keys. The three sets include 3270 keys, user defined keys, and system keys.

Software support includes System/370 CMS source programs, with directly transportable text and module files. Advanced facilities include multiple concurrent processes, overlapping multi-window displays, programmable fonts, and a separate I/O processor file system for file sharing and protection.



Peripheral support includes 35M- to 140M-byte random access storage on one or two internal Winchesters. Additional options include an IBM-compatible nine-track 1600 bpi tape drive and low and medium speed printers. In a typical network of six nodes with shared peripherals, the unit prices will be about \$35,000 per node. **Canaan Computer Corp.**, 39 Lindeman Dr, Trumbull, CT 06611.

Circle 269

Let Fluke rescue you from the landslide of μ p-board failures.

Four billion microprocessors will be built into countless products this year. We're filling the world with micro-systems. But *how* can we test and service them all?

Fluke's 9010A Troubleshooter puts some fast, simple answers at your fingertips. It's the first tester so easy to use, you'll start

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Fluke has pre-programmed the 9010A to find most common faults automatically. Press a single key and it checks for Bus, ROM, RAM, or I/O faults, displaying clear diagnostic messages. For faults beyond the bus, our smart probe uses both stimulus and measurement to

quickly track failures to the node.

With support for 32 types of microprocessors, the 9010A will test almost any product. Merely plug the correct interface pod into the microprocessor's socket and take control of the unit under test.

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Don't get buried in the PCB landslide. For less than \$5,000 you can own a Fluke 9010A, complete and ready for testing today. For more information, contact your local Fluke representative or call 800-426-0361.



Now write 9010A software off-line with our new Language Compiler and popular personal computers. It's a convenient tool that makes programming fast and easy.

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9010A Micro-System Troubleshooter

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For technical data circle number 74

Expandable computer adapts to diverse professional uses

Texas Instruments has taken several steps away from the game machines with its Professional Computer. This expandable system combines internal diskette and Winchester drives, enhanced communications, ergonomic keyboard, internal modem, and high resolution display. In addition, voice management and English language command capabilities will be introduced for the computer.

The compact system unit houses an 8088 16-bit CPU and 64K-byte RAM that is optionally expandable to 256K in 64K-byte increments. The computer's 8K-byte system ROM is expandable to 16K. A 320K-byte built-in diskette drive is standard; an optional 5M- or 10M-byte Winchester drive, or a second 320K diskette, can be installed internally by users. Also featured as part of the main unit are diskette controller, five-slot expansion bus, keyboard interface, parallel printer port, power supply, speaker, and monochrome or color CRT controller with 4K-byte video display memory.

High resolution data are presented on a 12" (30-cm) green phosphor monochrome display or on the optional 13" (33-cm) color display. Both CRTs use a 25-line x 80-col format and 720 x 300 pixels with the graphics controller option. Applications programs, even with extensive graphics, can operate with either display unit without modification. No reprogramming is required when changing displays.

Communications options provide a variety of protocols needed for smooth interaction with other computers and data bases. Both TTY and 3780 emulators are available for the computer in network environments. Standalone 3270 SNA, clustered 3270 BSC/SNA, 3101 emula-



tion, and communications to TI's Business Systems minicomputers are supported as part of the third-quarter 1983 enhancements. Either a 300- or 300/1200-bps internal direct connect modem, with auto-dial/answer capabilities, provides communications to other peripherals or data bases over ordinary telephone lines.

Also planned is the natural language user interface. Derived from TI's research in artificial intelligence, the interface combines common English words and phrases into computer commands. Users construct sentences from word groups shown in a set of windows displayed on screen. Selected items from

each window appear at the bottom of the video screen as standard English sentences describing the functions to be performed. The computer can also recognize and respond to voice commands through the voice management system. Combining speech processing, voice recognition, and telephone management functions in a single integrated internal unit, the 32-bit signal processing micro-computer based system recognizes an unlimited number of spoken words or phrases. The basic computer is currently selling for \$2595. **Texas Instruments Corp, Data Systems Group, PO Box 402430, H-651, Dallas, TX 75240.**

Circle 270

Improved processor line beefs up midrange computing

Additions to the 4300 processor line deliver powerful computing in IBM's midrange systems. The expanded series introduces the 4361 and the 4381 processors, both units for scientific and commercial applications.

Model 4361 uses a dense bipolar VLSI memory chip that provides four times the storage capacity of a similar chip in the 4331. This chip is used in control storage and in high speed cache buffer

storage. The system is available with up to 12 million characters of main storage and six I/O channels (or four DASD/8809 adapters and three I/O channels).

As with the 4361, model 4381 has up to 16 million characters of main storage, in addition to 12 I/O channels. The model 4381 can act as either a host or distributed processor.

The same high density memory chips that the 4361 employs are used in the 4381.

This custom logic chip contains 1100 logic circuits for increased processing power. In addition, the cache uses a new bipolar static RAM. Multichip modules, 2.5 in square, hold up to 36 of these logic and memory chips. Up to 22 such modules will plug onto a board in the new processors.

"Impingement cooling," a technique developed from the water-cooled thermal

(continued on page 152)

"BUBBLES ARE HELPING NIXDORF BREAK INTO NEW SALES FIGURES."

—Axel Hass
Sales Director of Retail Industry
Nixdorf Computer AG



Computer product codes. Each as unique as a fingerprint. Each representing a product and its cost. Designed to eliminate the time and expense of price tags and stickers, while providing critical up-to-the-second inventory updates.

In order to make efficient use of this system, a retailer must have fast and reliable access to thousands of codes, anytime. Unfortunately, a modular, computerized access has never been provided.

Until now, that is.

Nixdorf Computer has introduced an affordable system that is both easy to use and to install. A system that doesn't discount quality, performance or reliability. A system made possible with a purchase from Intel.

Rather than counting on more RAM for keeping the data base, Nixdorf depends on an Intel 7110 bubble featuring a full

megabit of non-volatile memory. Capable of storing thousands of codes for any store.

The solid state bubble also outperforms disks and floppies in this demanding environment. Which means Nixdorf's memory system runs maintenance-free 24-hours a day. So the downtime that means "no sale" is prevented. And the bubble's high speed access even helps keep check-out lines moving.

The 7110's small size also helps make Nixdorf's stand-alone system self-contained and modular. So the system fits smoothly into any size retail organization, can be easily networked, and can grow as the store's customer base grows.

Even if its customer base grows as fast as Nixdorf's.

Whatever your line in electronics, Intel bubbles just may be the break you've needed.

So write us for more information.
Lit. Dept. Y7, 3065 Bowers Avenue, Santa Clara, CA 95051.

Or call us, toll-free. (800) 538-1876.
In California, (800) 672-1833.

Then, perhaps, celebrate your new sales figures with a French bubble product. Its computer code is shown above.

Dom Perignon, 1975.

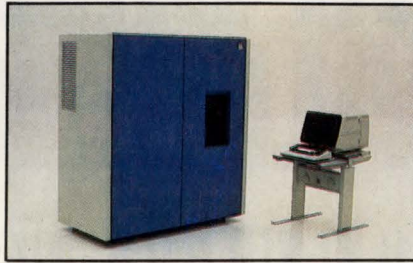
intel® delivers solutions
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Improved processor

(continued from page 150)

conduction method used in other processors, removes heat from the modules. It directs room temperature air onto the center of each chip, then expels it through the spaces between the modules.

The 4381's other features include an internal processor cycle time of 68 ns and an aggregate data transfer rate of 22 million characters per second in the data streaming mode. Data flow is 8-byte parallel within and between the processor, cache, and channels; between the cache and main storage data flow is 16-byte parallel.

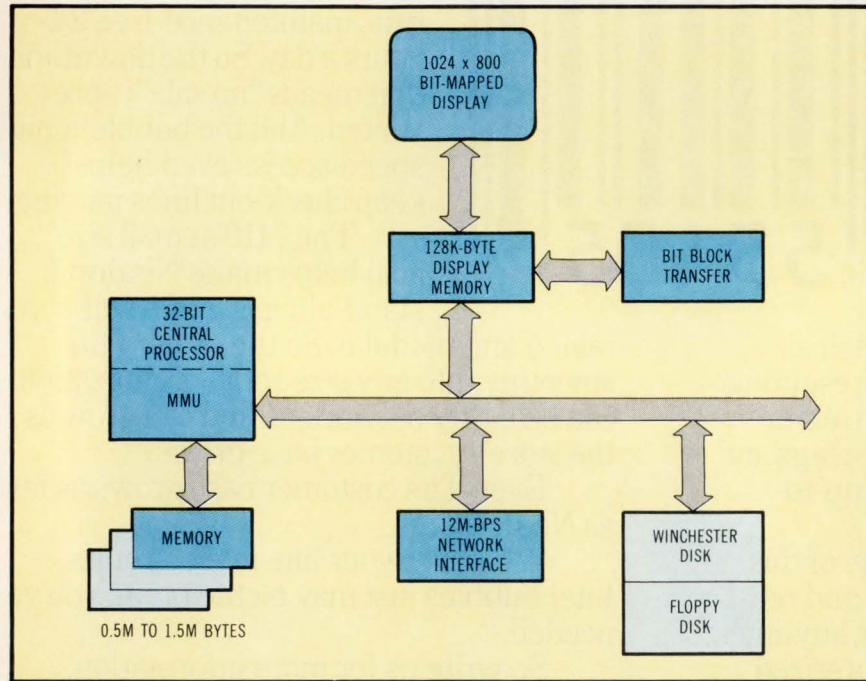


In addition to the improved processors, software developments support engineering and scientific users. Two problem-solving programs provide a

high accuracy arithmetic (ACRITH) subroutine library and VS Fortran interactive debug. The ACRITH library covers algorithm testing, research in numerical methods, and system analysis. The VS Fortran debug monitors Fortran program execution and can change program parameters at execution time.

Software prices range from \$1800 to \$2500. Model 4361 hardware ranges from \$150,000 to \$275,000, while 4381s range from \$370,000 to \$620,000. **IBM Corp, Information Systems Group**, 900 King St, Rye Brook, NY 10573. Circle 271

Nodes tie desktop supermini into 12M-bps local network



Based on the MC68010 microprocessor, DN300 delivers a 16M-byte virtual memory address space with 1.5M-byte main memory. Also included in a desktop package are high performance graphics and access to a 12M-bps network.

Eliminating the dependency on main-frame access, Domain network nodes make technical professionals independent by putting them in control of their own time. Apollo's DN300 computational node supports this concept by replacing mid-range superminis with a desktop unit. Operating alone or as part of a 12M-bps local area network, the unit

costs 20 to 30 percent less than competitive units. Resources such as mass storage, communication gateways, and printers can be shared across the network as though they were locally connected.

To achieve standalone power, the DN300 uses the Motorola MC68010 microprocessor and DMA controller. This virtual memory processor, combined with

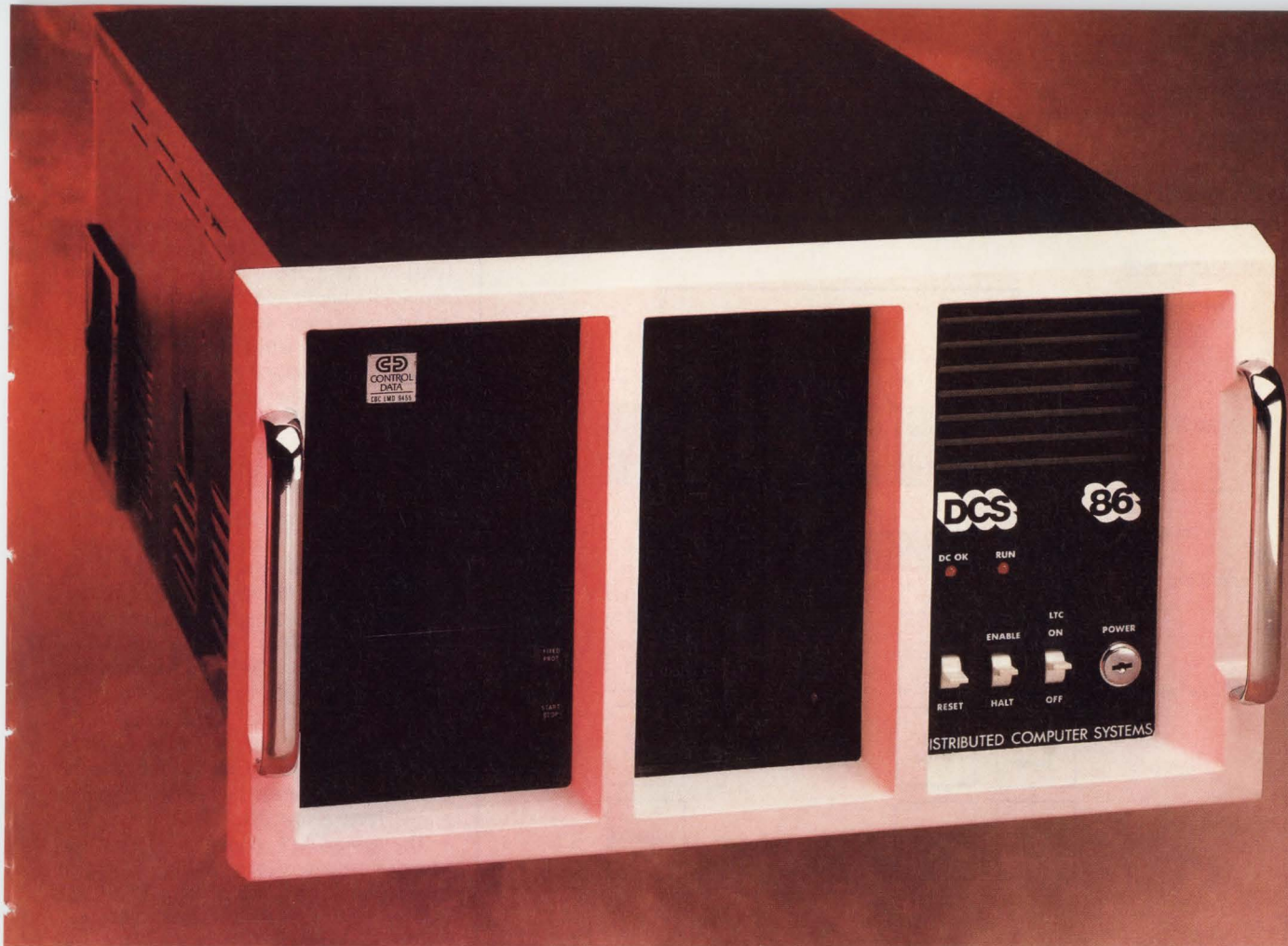
MMU, is claimed to deliver the power of a VAX-11/750. The dedicated VLSI processor supports up to 15 concurrent user processes. Each process gains a virtual address space of 16M bytes from the integral MMU. This MMU dynamically maps 24-bit virtual addresses into a 22-bit physical memory address space and maintains protection and usage statistics for each 1024-byte page of data.

The station is built around two printed circuit boards that contain the CPU with 0.5M-byte main memory, memory management hardware, display controller with 128K bytes of dedicated display memory, and network interface. The network interface provides a 12M-bps baseband data rate, made possible by self-synchronizing hardware bit stuffing techniques, ring topology, and token passing arbitration. Two separate RS-232-C ports provide independent, software selectable transmission rates from 50 to 19.2k baud.

The integral display provides a horizontally oriented 17" (43-cm) screen with 1024- x 800-pixel resolution. The 15 concurrent virtual memory processes can be viewed using the screen in a multiwindow mode; highest resolution is obtained by using the entire bit-mapped raster scan display. A dedicated 128K-byte dual-port display memory performs interlaced refresh at 80 kHz.

Prices for the node range from \$10,449 to \$27,900 depending on the amount of main memory and mass storage. **Apollo Computer Inc**, 15 Elizabeth Dr, Chelmsford, MA 01824.

Circle 272



BORN TO BE ABUSED!

Raised in a harsh environment, our DCS/86 16-bit Multibus compatible computer system can cope with industrial reality.

Industrial Ruggedness

Designed for industrial applications, the DCS chassis is solid metal with no plastic, injection-molded parts. The front panel is an aluminum casting and our Multibus card cage is aluminum with a low-noise multi-layer backplane. Only the finest mechanical components are used to insure structural integrity in the most adverse conditions.

Reliability

Industrial grade preburned-in chips are used. Our system modules are subjected to dynamic burn-in at 55°C for forty-eight hours in our environmental chamber. As a fully matured unit, every DCS system is completely tested for a minimum of 5 days with extensive system diagnostics. At DCS, reliability is not a slogan, it is our commitment.

Unmatched Modularity

Our DCS systems are created to meet virtually any industrial application. They permit the user to mix and match operating systems, high level languages, interfaces, fixed and removable storage with a complete range of Multibus peripherals. Hardware configurations in our standard 19" rackmountable

chassis can contain fixed and removable hard disks in 5 1/4" and 8" sizes as well as standard or slim line floppies. Operating systems supported are CPM/86*, MPM/86*, MS-DOS*, Concurrent CPM/86* and RMX-86*. "C", Fortran and Pascal are among the high level languages used. Whether your applications involve real-time data acquisition, multi-user software developments or data base management for factory automation, the DCS/86 family has a configuration to meet your budget.

Support

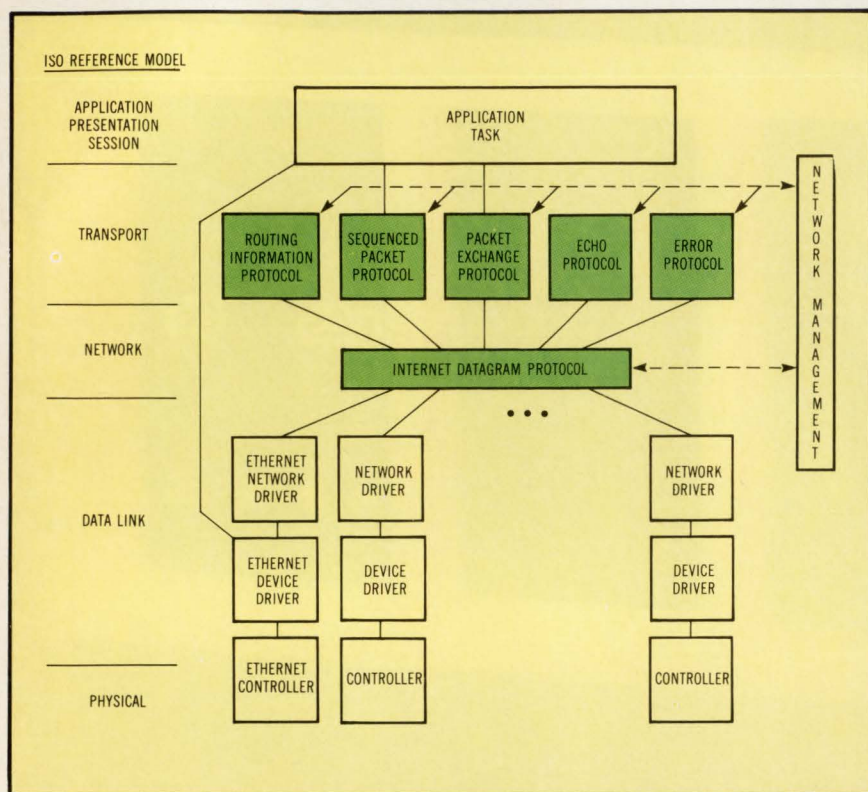
Since 1979, DCS has been designing and manufacturing rugged industrial micro-computer systems for process/industrial control, data communications and software development. The DCS family has been abused in harsh environments the world over. DCS provides total systems support through our expanding network of direct regional sales/support centers in conjunction with our corporate customer support group.

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*CPM and MPM trademarks of Digital Research
*MS-DOS trademark of Microsoft

Software for Ethernet LANs reaches transport level



Internet Transport Protocol (ITP) NS4200 software packages from Interlan, Inc, provide task to task communications over Ethernet local area networks (LANs) for VAX/VMS and RSX-11M systems. The software provides reliable, flow controlled, interprocess communications between Ethernet connected systems.

In addition to supporting high bandwidth communications over an Ethernet LAN, an internetwork router facility is

included for reliable end to end delivery between systems residing on different LANs. These LANs can be geographically distant and interconnected by long-haul channels or networks, or can consist of media such as baseband CSMA/CD, baseband token ring, or broadband token bus that are bridged together.

Transmission protocols were specified for use on an Ethernet channel, allowing the protocol's design to take advantage

of Ethernet's packet addressing, error detection, and delay bandwidth characteristics. As a result, each ITP package provides a high bandwidth virtual circuit communications service to a user's application task with minimum host CPU loading. The NS4200 ITP is specified to the Xerox Network Systems' Internet Transport Protocols, which are the architectural foundation for Xerox's distributed systems. As illustrated, the ITP protocols include internet datagram, routing information, sequenced packet, packet exchange, echo, and error protocols. With the NS4200 ITP package as a building block, the task of networking RSX-11M and VAX/VMS systems to Ethernet compatible systems is minimized. Only detailed file structures and command interpretations need be addressed to provide task to task communications between RSX-11M or VAX/VMS systems with other Ethernet compatible systems that use the Xerox Network Systems' higher level protocols.

The NS4200 ITP package contains a NETMAN menu-driven utility program that automatically tallies over 40 different network statistical values. NETMAN enables a network manager to acquire and display operational data from local/remote ITP nodes. NETMAN's parameters let a network manager identify connected ITP stations, identify congestion and flow control bottlenecks, understand traffic flow patterns, evaluate the performance of virtual circuit connections, and assess the quality of network service. **Interlan, Inc**, 3 Liberty Way, Westford, MA 01886.

Circle 273

Supermini runs multiple processors under one operating system

Linking 2 to 10 processors to shared global memory through a memory bus, the 3200MPS forms a tightly coupled asymmetrical multiprocessor system. The system achieves processing rates of 18.8M single-precision Whetstones/s.

High performance is achieved cost-effectively by adding auxiliary processors to the CPU. Built on 32-bit parallel architecture, the system uses 64-bit floating point arithmetic units with dual 32-bit data paths within the global memory bus. Memory modules,

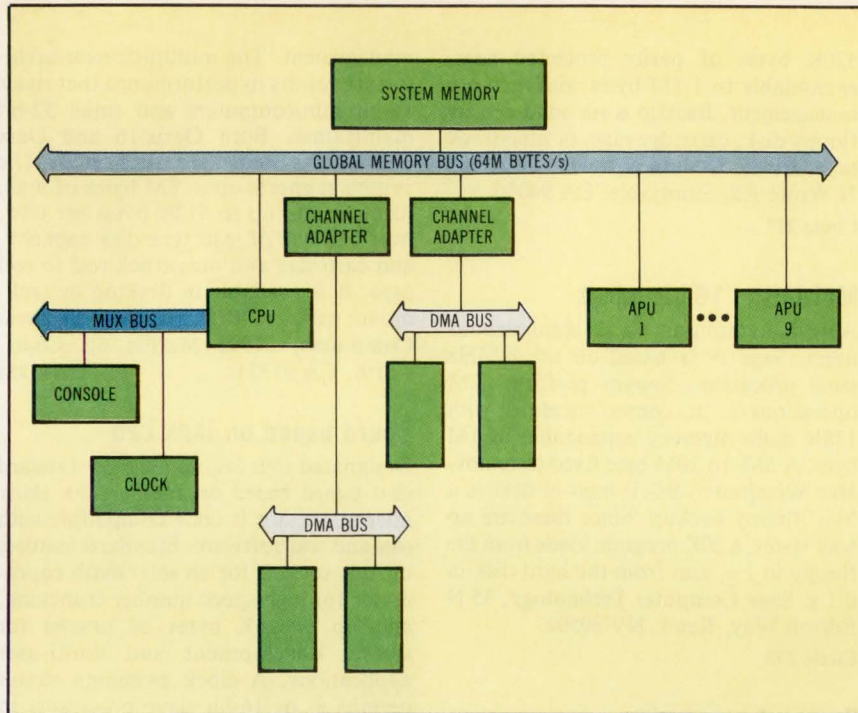
general purpose registers, and writable fixed control store also use 32-bit data paths.

Taking advantage of the multiprocessor architecture, extensions to the OS/32 operating system and Fortran 7 language are supported. Under OS/32, user written APU tasks run unmodified on the CPU unless they contain calls to the APU microprogram. Control mechanisms for the APU and associated tasks are available to both operator and privileged tasks. Task assignments to

APU or CPU can be changed during operation from the console or user written program.

A 32-bit CPU monitors all system activity, including I/O and memory management. It also loads all tasks and dispatches application tasks to APUS for execution, and it can perform computation, serving particularly well in I/O intensive tasks.

APUS are general purpose processing units, each with arithmetic processor, floating point processor, and global



Growing from 2 to 10 processors, Perkin-Elmer's tightly coupled multiprocessor system 3200MPS handles communications between processors through a 16M-byte global memory over a full 64-bit bus. I/O transfers occur over four independent buses with 40M-byte/s bandwidth.

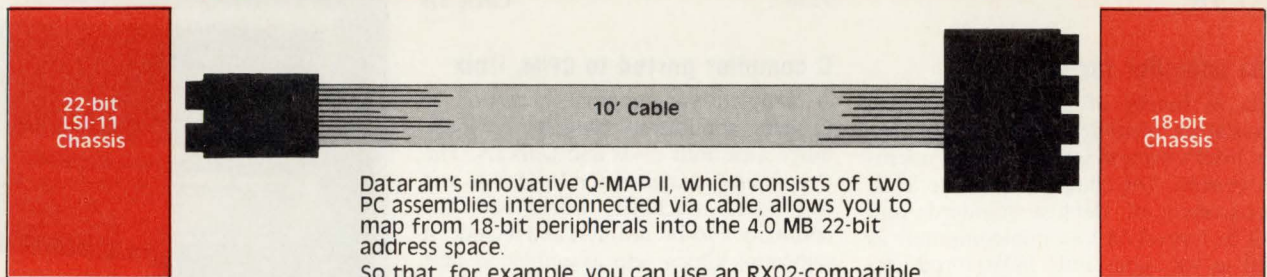
memory interface with its own 4K-byte cache.

The global memory system supports up to 16M bytes of directly addressable memory. All APUs and the CPU share global memory, which has a 64M-byte/s bandwidth on the memory bus. This bus, made up of two unidirectional asynchronous 32-bit buses, transfers addresses and data to be read or written on one bus and just uses the other for reading data.

A basic configuration of one CPU and APU achieves 4.7M-Whetstone/s performance. Each additional APU raises this number by another 1.8M Whetstones, achieving a total of 18.8M when a full 9-APU configuration is installed.

An entry level system is made up of CPU with 8K-byte cache, floating point processor, writable control store, two communication lines, universal clock, loader storage unit, 2M-byte two-way interleaved system memory, and I/O chassis; and APU with global memory interface with 4K-byte cache, floating point processor, writable control store, arithmetic processor, shared memory bank controller, and pair of RTSMS. Price is \$185,000. Additional APUs are priced at \$35,000 each. **Perkin-Elmer Corp, Data Systems Group**, 2 Crescent Pl, Oceanport, NJ 07757. **Circle 274**

LSI-11 users: Get 4.0 MB capability while supporting both 18-bit and 22-bit peripherals



Dataram's innovative Q-MAP II, which consists of two PC assemblies interconnected via cable, allows you to map from 18-bit peripherals into the 4.0 MB 22-bit address space.

So that, for example, you can use an RX02-compatible floppy disk subsystem in a 4.0 MB LSI-11 system and maintain complete software compatibility. By duplicating the functions of DEC's KT24 (which DEC offers only in its UNIBUS products), Dataram's Q-MAP II operates under RSX-11M, RSX-11M-PLUS, RSTS, UNIX, or any DEC operating system which supports the KT24.

Simply plug one end of the Q-MAP II into the chassis which you want to use for 18-bit addressing, and plug the other end into a second chassis for 22-bit addressing.

The Q-MAP II, in single quantity, is only \$1400. We can also provide the additional chassis for only \$1350, or 1.0 MB single-quad ADD-IN (with CSR and block mode capability) for only \$2200.

Call us today at (609) 799-0071 to discuss our Q-MAP II and other LSI-11 compatible products.

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DATARAM

Dataram Corporation □ Princeton Road □ Cranbury, NJ 08512 □ (609) 799-0071 □ TWX: 510-685-2542

Networking multi-user micro



Altos 586 microcomputer has five-user (upgradable to eight-user) capability. Interfaces to Ethernet and Altos-Net networks are provided. The 16-bit micro uses the Intel 8086 processor running at 10 MHz and has 256K or 512K RAM, expandable to 1M byte. An ergonomically designed terminal is available. Software includes Xenix/Unix and a business software package. Battery backed clock and calendar, Multibus architecture, proprietary memory management, power failure detection, and internal distributed intelligence are featured. Six RS-232 ports, upgradable to 10, are supported. Prices range from \$4990 to \$7990. **Altos Computer Systems**, 2360 Bering Dr, San Jose, CA 95131.

Circle 275

Ada compiler for iAPX 86

Ada 86 family of computer language translators compiles the Ada language for Intel's iAPX 86 series of 16-bit microprocessors. The compiler will meet U.S. Department of Defense standards and will be hosted on VAX minicomputers as well as on other Intel based products. Similar introductions include Ada 432 Version 1—an Ada compiler for the iAPX 432 micromainframe computer, and iMAX—an iAPX 432 operating system written entirely in Ada. **Intel Corp**, 3065 Bowers Ave, Santa Clara, CA 95051.

Circle 276

Micro with mini/Unix performance

A 68000/Unix based, multi-user Multibus configured microcomputer, the Codata 3300 comes standard as an eight-user system with integral 5 1/4" 33M-byte Winchester drive for \$9600. A two-user version with 12M-byte Winchester is priced at \$7800. An 8" 84M-byte Winchester configuration is \$13,500. System has

320K bytes of parity protected RAM, expandable to 1.5M bytes with memory management. Backup is via quad-density floppy disk, cartridge tape, or nine-track tape drives. **Codata Systems Corp**, 285 N Wolfe Rd, Sunnyvale, CA 94086.

Circle 277

Multi-user 16-bit micro

Accommodating up to six simultaneous users, Sage IV is based on the 8-MHz 68000 processor. System performs 2M operations/s. It comes standard with 128K main memory expandable to 1M byte. A 5M- to 30M-byte fixed or removable Winchester disk is built-in next to a 5 1/4" floppy backup. Since there are no wait states, a 20K program loads from the floppy in 1 s, and from the hard disk in 0.1 s. **Sage Computer Technology**, 35 N Edison Way, Reno, NV 89502.

Circle 278

Protocol converter

PCI 1076, an ASCII to 3270 SNA/SDLC protocol converter, lets personal computers, portables, microcomputers, and other devices including CRTs and printers communicate on a mainframe network. It connects to the host directly or by dial-up, allowing access to the host from virtually any location. Up to seven terminals can attach to one converter. **Protocol Computers, Inc**, 6150 Canoga Ave, Suite 100, Woodland Hills, CA 91367.

Circle 279

C compiler ported to CP/M, Unix

A complete systems implementation of C gives application program compatibility with both CP/M and Unix OS. The C compiler, designed for 16-bit 8086 and 8088 based machines, works with the company's 16-bit utilities, and includes a relocating linker and assembler as part of the package. The compiler also has built-in features of the Unix error checking LINT program. **Digital Research**, PO Box 579, 160 Central Ave, Pacific Grove, CA 93950.

Circle 280

Five-processor micro

Ensign is a fast five-processor computer system. Main CPU is a Motorola 68000 running at 8 MHz with no wait states. Two 6801 processors handle all serial I/O for up to 32 users. This frees the main processor for communications overhead. A 6-MHz z80B supervises all disk and tape I/O without CPU degradation. Another 6-MHz z80B is used for memory

management. The multiprocessor architecture results in performance that rivals 16-bit minicomputers and small 32-bit mainframes. Both Oasis-16 and Unix operating systems are supported. The system supports up to 8M bytes of main memory and up to 512K bytes per user, over 1G byte of SMD type disk capacity, and cartridge and nine-track reel to reel tape. It is available in desktop or rack-mount cabinet. **IBC/Integrated Business Computers**, 21592 Marilla St, Chatsworth, CA 91311.

Circle 281

Board based on iAPX CPU

Designated CPU 286, an IEEE 696 standard CPU board based on Intel's iAPX 286/10 microprocessor is code compatible with 8086 and 8088 software. Standard features include sockets for an 80287 math coprocessor for high speed number crunching, and up to 16K bytes of EPROM for system development and multi-user applications. A clock switching circuit permits 8- or 16-bit slave processors to run on the same bus at various rates, so that users can execute alternate software libraries. With a 24-bit address and 16-bit data bus, the board accesses 16M bytes of online system memory without segmentation. **CompuPro**, Oakland Airport, CA 94614.

Circle 282

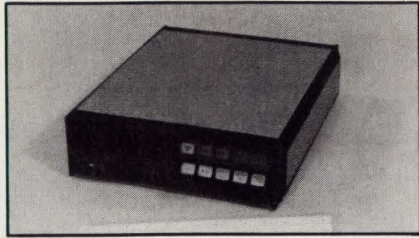
Portable 16-bit computer



The Compaq IBM PC-compatible system includes a high resolution 9" (23-cm) diagonal video display, 16-bit 8088 microprocessor with 128K-byte RAM (expandable to 256K bytes), a 5 1/4" floppy disk drive with 320K-byte storage, and room for an optional second 320K-byte floppy. Ports for an optional red-green-blue video monitor, for composite video, and for connection to a standard TV set are provided, along with parallel printer interface and socket for an Intel 8087 coprocessor. Asynchronous communications interface is optional. Price is \$2995. **Compaq Computer Corp**, 12330 Perry Rd, Houston, TX 77070.

Circle 283

Q-bus transportable



In a 22.5-lb (10.2-kg), 4" x 13" x 15" (10- x 33- x 38-cm) chassis, the 11/M12 packs an LSI-11/23 CPU with memory management and 256K bytes of RAM along with a half-height 10M-byte fixed Winchester disk (emulating two RL01s) and 512K-byte floppy drive (emulating an RX02). Four serial ports accept RS-232-C and 20-mA current loop. The box, which comes without display monitor, contains operator controls, a 110-V power supply, and a spare card slot. Standard DEC software, including RT-11, TSX-Plus, and RSX-11M, runs on the machine. Quantity-one, the system costs \$8400. **Andromeda Systems, Inc.**, 9000 Eaton Ave, Canoga Park, CA 91304.

Circle 284

Coprocessing micro board

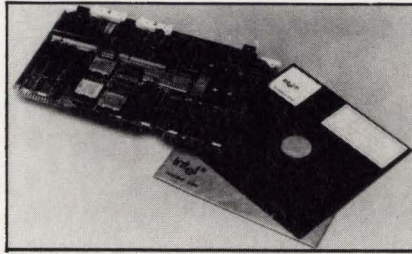
DS2 plugs into the IBM PC and allows users to run CP/M software or PC-DOS on the PC. The board consists of a Z80B processor, 64K bytes of RAM, and one serial port. The port can be used in one of three modes: RS-232, RS-422, or IBM's implementation of a 20-mA current loop. The DS2S board has all DS2 capabilities but four sync/async ports replace the serial port. It contains sockets for EPROM and/or EEPROM-stored programs. **BYAD, Inc.**, 95 W Algonquin Rd, Arlington Heights, IL 60005. Circle 285

Processor board based on 68000

The 68000-P processor board has an 8-MHz MC6800L and can optionally go to 12 MHz. It addresses 16M bytes of RAM. In addition, it features three 16-bit interval timers for use as watchdog or task switching timers in multitasking environments. Board accommodates 8K ROM and is supplied with a Forth based monitor. It features full 24-bit address space, 16-bit data transfers, and eight vectored interrupt lines. The standard 256 I/O mapped ports and extended 64K of I/O mapped ports are supported. Extended vectored ID interrupt is available as jumper option. Price range for the 8-MHz version is \$349 to \$695. **Inner Access Corp.**, PO Box 888, Belmont, CA 94002. Circle 286

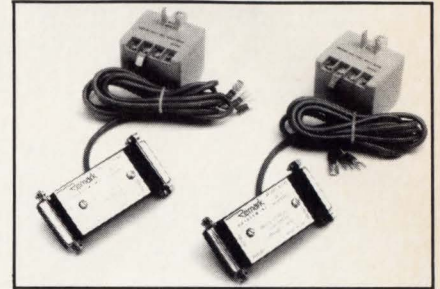
Networking single-board computer

The iSBC 186/51 COMputer board combines a single-chip micro, data communications capabilities, and industry standard networking software. Board includes iAPX 186 central processor, 80130 operating system firmware, 82586 LAN co-processor, and 82501 Ethernet serial interface. Device can run user programs, handle communication tasks, and operate as an intelligent front end. The board has 128K bytes of dual-ported RAM expandable to 256K bytes using a multimode board. Board sells for \$3000; network software sells for \$5000. **Intel Corp.**, 3065 Bowers Ave, Santa Clara, CA 95051.



Circle 287

Converters for RS-232 to RS-422



Models 63-3S and 63-4S are a series of RS-232 to RS-422 converters. Each model is self-powered via a wall-mounted transformer and internal regulation circuitry. Signals on the RS-232 connector swing over the range of ± 11 V while the differential signals are in the range of 0 to 5 V. Converters also act as modems designed to transmit and receive full duplex data at 100k baud up to 4000' over two twisted pairs. Each unit includes an 8' line cord and a transformer and sells for \$126 in singles and \$99 each in 100s. **Remark Datacom Inc.**, 4 Sycamore Dr, Woodbury, NY 11797.

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82C59A	CMOS Priority Interrupt Controller	Now
82C82	CMOS Octal Latch	Now
82C84A	CMOS Clock Generator	Now
82C88	CMOS Bus Controller	Now
82C52	CMOS Serial Comm. Interface	Samples

For full details, write: Harris Semiconductor CMOS Digital Products Division, P.O. Box 883, MS 53-035, Melbourne, Florida 32901.

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Handheld RS-232-C telecomputer

Model TC 103 telecomputer system for hardwired LAN installation in fixed or portable locations plugs directly into an RS-232-C port. System has a QWERTY-style full alphabetic keyboard, with control and shift functions to generate the 128-character ASCII code set. User friendly help keys facilitate development of computer-initiated dialoguing software to reduce or eliminate operator training. A 16-character LCD, variable scroll rate from 2 to 30 cps, and repeat key to allow review of the last 80 characters received are included. **IXO, Inc.**, 6041 Bristol Pkwy, Culver City, CA 90230. **Circle 289**

Array processor

A 64-bit array processor, model MAP-6410 allows micro, mini, or superminicomputers to perform iterative math functions with mainframe accuracy. All arithmetic operations are true floating point in a 64-bit hex format, providing over 16 decimal digits of precision. Three levels of software are available: MAXPAK, which allows Fortran programmers to use the device without knowledge of array processors; Snap II operating system with Fortran callable functions; and assembly language utilities. Prices start at \$50,000 for the basic system, which consists of 16-slot chassis with power supply, CSPU control processor, 64-bit wide arithmetic processor, 128K bytes of program memory, and 512K bytes of data memory. **CSP Inc.**, 40 Linnell Cir, Billerica, MA 01821. **Circle 290**

Unix for 68000 microprocessor

The QU/32 is a 12-MHz 68000/68010-based Unix system. Rated at 1.3 MIPS, the system supports 4M bytes of 100-ns physical memory without address space limitations inherent in other systems. Dual-bus architecture and ported memory together with memory management and arbitration techniques allow memory access without wait states. The

operating system is the Berkeley enhanced System III Unix with networking. Pascal, C, Fortran, Basic, Ada, and relational DBMS are available. System pricing starts at \$9900. **Integrated Solutions, Inc.**, 1350 Dell Ave, Campbell, CA 95008. **Circle 291**

High speed file system

MTOS-86 with the MTOS-86 nucleus allows the user to collect, store, and recall information in a realtime process control environment. Both file and record locking are provided. Two file organizations are available: runtime extensible and contiguous. Regardless of organization, a file can be accessed randomly or sequentially. The file system requires 5K bytes of ROM. A universal driver interface allows any block addressable/replaceable mass storage device to be used. **Industrial Programming Inc.**, 100 Jericho Quadrangle, Jericho, NY 11753. **Circle 292**

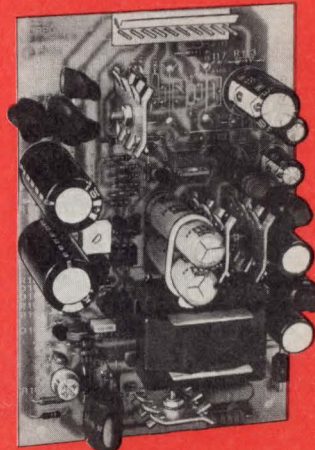
Lookalike IBM PC system

Series 1600 microcomputers use the Intel 8086 microprocessor at 8 MHz to operate at up to four times the speed of the IBM PC. Networking options allow up to 64 8- or 16-bit microcomputers and hard disk add-on storage to be linked together. A basic system consists of 128K bytes of RAM, 1M byte of 5 1/4" floppy disk storage, and 12.5M bytes of hard disk storage. Internal memory is expandable to 512K bytes. Eight expansion slots permit the addition of peripherals. Two hard disk add-ons, the File 10 and File 40, provide optional mass storage. These free-standing units provide 12.5M and 40M bytes of additional storage, respectively. **Eagle Computer, Inc.**, 983 University Ave, Bldg C, Los Gatos, CA 95030. **Circle 293**

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CIRCLE 78

COMPUTER DESIGN/December 1983

Xenix operating system

Developed for the iAPX 286 line of microprocessors and board-level products, the Xenix 286 operating system is a multitasking multi-user system for high performance OEM applications. The combination of the 80286 and Xenix provides improved performance, multi-user access, record- and file-locking, and power-fail disk recovery. Operating system also includes driver support for five controller boards ranging from terminal communications to tape support. Xenix for the 80286 and the 286/10 is priced at \$3000 with OEM volume discounts; licensing and support arrangements are available. **Intel Corp**, 3065 Bowers Ave, Santa Clara, CA 95051. **Circle 294**

Pascal version

Micro Concurrent Pascal (mcp) is a high level language for programming realtime embedded systems. The mcp provides process, monitor, and class constructs for Concurrent Pascal. It introduces the device-monitor constructs permitting hardware interaction directly from the software. Programs compile into

pseudo-code (p-code) that can be either interpreted or native assembly language code. Designed for microprocessors, the p-code is reentrant, relocatable, and completely PROMable. Features include interrupt handling capabilities and separate compilation and assembly language routine calls. **Enertec, Inc**, 19 Jenkins Ave, Lansdale, PA 19446. **Circle 295**

Validated Ada compiler

Fully implemented Department of Defense ANSI 1982 spec Ada compiler and Ada development environment (ADE) coupled with a multiterminal 32-bit computer, the Ada Work Center allows from eight to 128 simultaneous users to develop Ada language applications. The Work Center package includes hardware, software, and technical support for Ada development on a full range of ROLM 16- and 32-bit computers. The Ada compiler implements all defined Ada functions; compilation rate exceeds 1200 lines/min. **ROLM Corp**, 4900 Old Ironsides Dr, Santa Clara, CA 95050. **Circle 296**

Ethernet chips

An Ethernet chip set includes the MB8795 data link controller and the MB502 Manchester encoder/decoder. With CMOS technology, the controller is configured in separate transmitter and receiver sections. Each section has a parallel interface port and provides sync buffering, byte parity checking, and parallel to serial conversions. The MB8795 also provides four modes of address recognition and a loopback feature for self-testing. The encoder/decoder offers low power, fast lock-on, and minimal jitter. Featuring both ECL and Schottky logic, the MB502 is available in a 24-pin standard DIP. **Fujitsu Microelectronics, Inc**, 57 Wells Ave, Newton, MA 02159. **Circle 297**

Ada and Pascal ported to Unix

An Ada compiler for the Concept/32 family of 32-bit computers provides for application software development under Unix. Future validated versions of the compiler will accept the programs without modifications. The Pascal compiler, which also runs under Unix, is compliant with international standards. Both compilers generate machine code via the C compiler for Concept/32 computers. Object programs execute directly at raw machine speeds. Ada, Pascal, and C subprograms can be mixed in a single program. Usage charges are \$10,000 for Ada and \$6000 for Pascal. **Gould Inc, S.E.L. Computer Systems Div**, 6901 W Sunrise Blvd, PO Box 9148, Fort Lauderdale, FL 33310. **Circle 298**

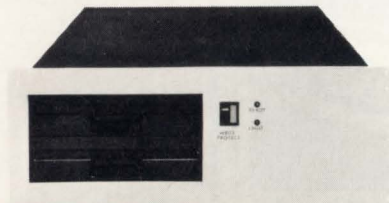
Modula-2 language

Modula-2 version 0.3 includes a module library, a compiler that runs 25% faster than the previous version, and a tutorial to easily update Pascal programmers. Low level machine access, realtime control, concurrent processes, and type-secure separate compilation with automatic version control are featured. Interrupt handling is fully supported. Language is designed for systems based on the 6502, 8080/Z80, TI 9900, and the 68000 microprocessors and interfaces to UCSD Pascal. Standard library provides console I/O, random access files, disk directory operations, format conversion, strings, decimal arithmetic, storage management, program execution, and process scheduling. **Volition Systems**, PO Box 1236, Del Mar, CA 92014. **Circle 299**

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Miniature modem



VA212LC is a Bell compatible switched network originate/answer, 1200-bps and 0- to 300-bps full-duplex modem. It features a combined microprocessor and LSI technology design configured on a single PC card. Modem is 1.5" (3.8 cm) high. Voice mode disables the auto-answer function. Five LEDs display modem's operational status. Modem (\$550) uses an automatic detection algorithm to handle both 9- and 10-bit character codes and an auto self-test routine. **Racal-Vadic**, 222 Caspian Dr, Sunnyvale, CA 94086. **Circle 300**

Ada compilers

Two software compilers generate Ada code for the z8000 16-bit microprocessor. Zilog/ICSC compiler runs on the System 8000 under an enhanced Unix operating system that produces code for the z8001 (segmented memory addressing) and the z8002 (nonsegmented) microprocessors. Also available is an Ada cross-compiler that produces code on the VAX-11 series. Compiler lists include all software updates for three months from purchase date. Zilog compiler is priced at \$8000/copy. **Zilog, Inc**, 1315 Dell Ave, Campbell, CA 95008. **Circle 301**

Operating system for VME/68000

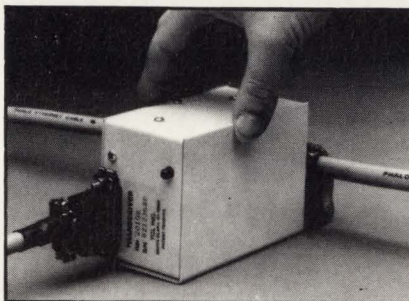
VMEFORTH/32 is a realtime operating system that uses the capabilities of the 68000 and 68010 processors in a VMEbus configuration. The 32-bit language system allows users to perform 16-, 32-, and 64-bit mathematical operations. Features include direct address to 16M bytes of memory with no paging, control from the resident system with no overlays, 2000G bytes of directly accessible disk storage capability, 230K bytes of user program space in a 256K partition, and unlimited size of user partitions. Full 32-bit operating system capability includes 32-bit stacks, 32-bit wide I/Os, 32-bit addressing without degradation, and 32-bit precision for math primitives. **Astraea Computer Corp**, 846 Del Rey Ave, Sunnyvale, CA 94086. **Circle 302**

Video disk computer

Touché is an interactive video disk system with an infrared touch-sensitive screen. The screen gives rapid, fingertip access to 54k frames of studio quality visuals, computer generated text and graphics, and stereo sound tracks stored on laser optical video disks. The unit consists of an Apple IIe microcomputer, video disk player, high resolution video monitor, and a 5 1/4" disk drive. The storage capacity is 300K bytes with space available for addition of a second drive or 5M- to 20M-byte hard disk. The complete system is priced at \$4995. **International Institute of Applied Technology**, 2121 Wisconsin Ave NW, Washington, DC 20007.

Circle 303

Ethernet transceiver kit



Operating at 1M, 4M, and 10M baud, the 2001E, 2004E, and 2010E LAN transceivers are small sized, lightweight, easy to install, and meet Ethernet protocol. They measure 5.4 x 7.0 x 10.2 cm, weigh 9 oz, and allow single-tap installation without shutting down the entire system. Priced at \$228 each in single-unit quantities (tap block included), transceivers have a one-year limited warranty. **TCL Inc**, 2066B Walsh Ave, Santa Clara, CA 95050.

Circle 304

Small micro with Basic

K-9000 series is available in 4-, 8-, and 16-MHz versions. It operates in a multiprocessing mode of up to 90 cards and comes with tiny Basic and up to 24K bytes of memory (8K bytes battery backup and 16K bytes EPROM). Features include DMA structured I/O buffers on the address data and control lines. RS-232 with handshaking is also included. EPROM is in an auto-start location and includes relocatable 4K bytes of utilities and firmware. Price is \$199. **Transwave Corp**, Cedar Valley, Box 489, Vanderbilt, PA 15486. **Circle 305**

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CIRCLE 79

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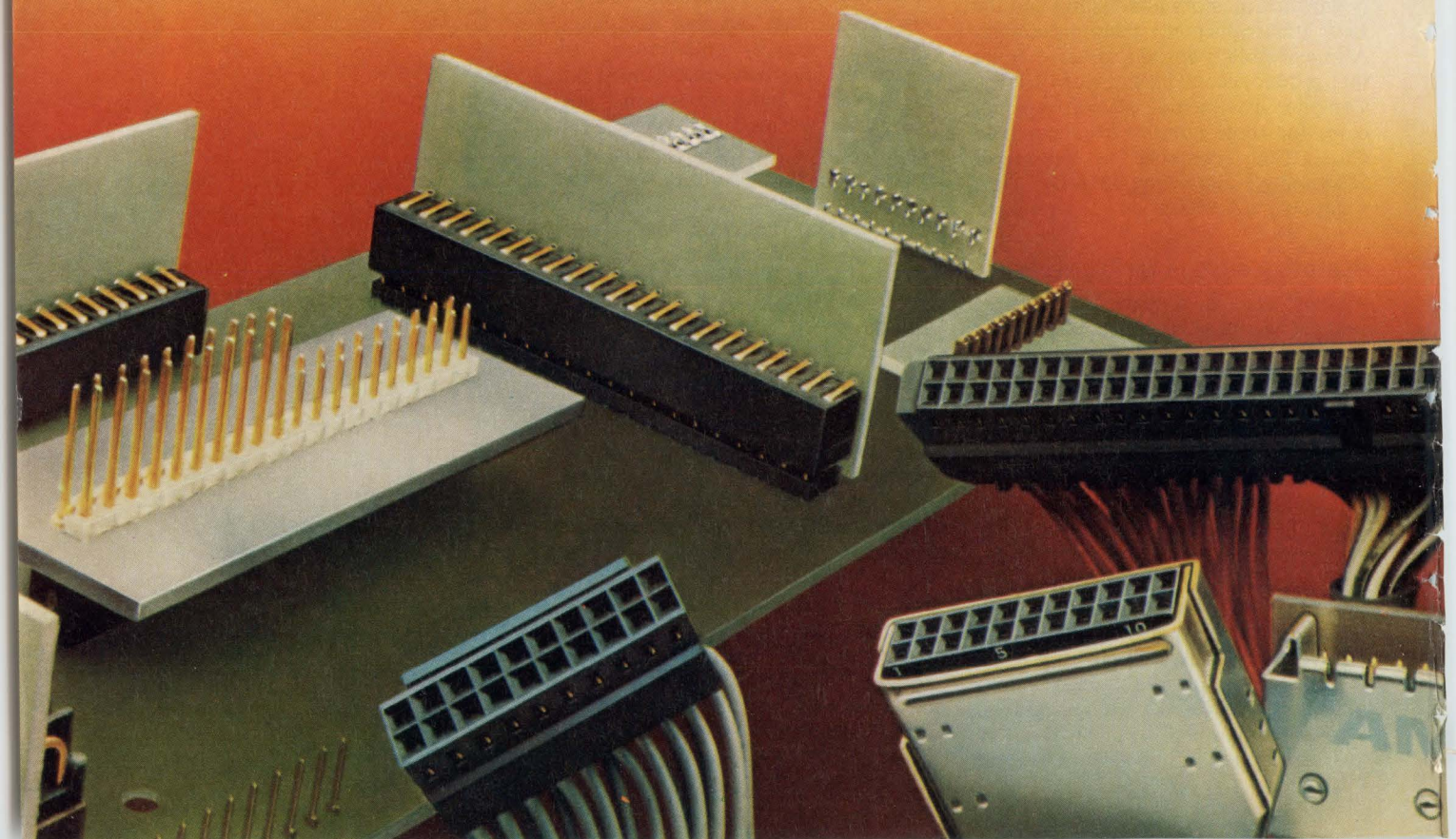
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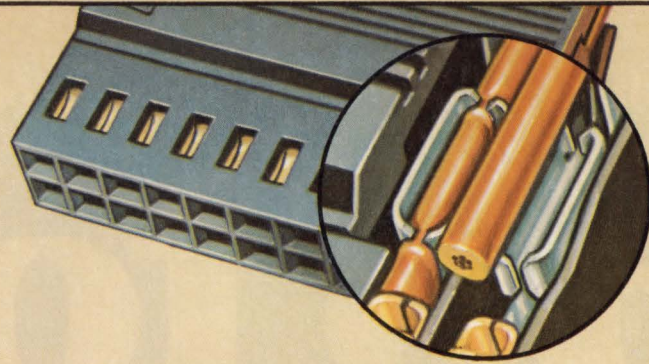
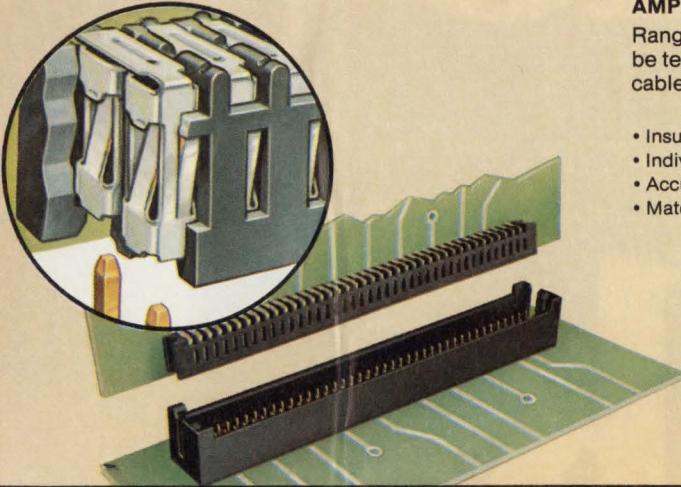


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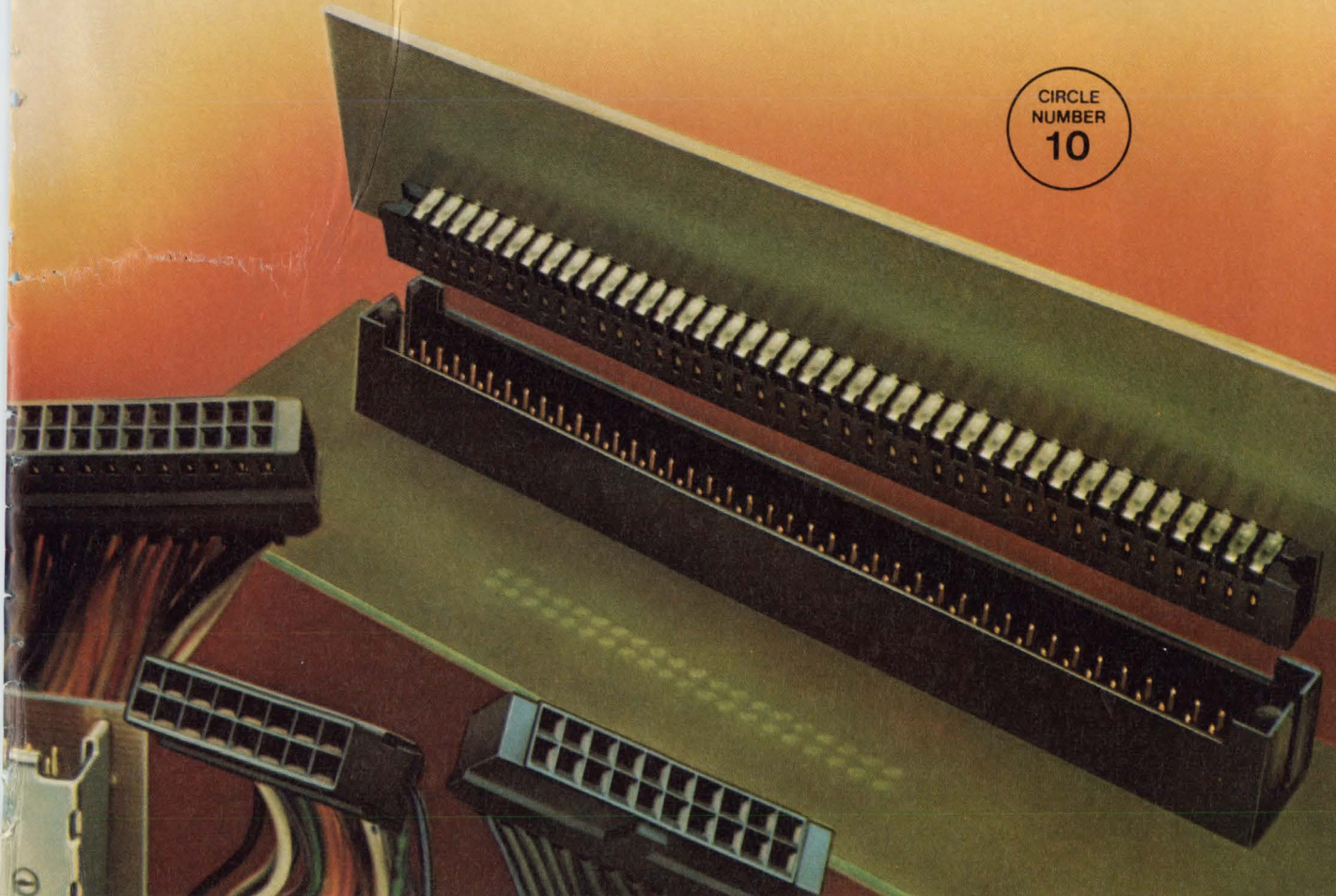
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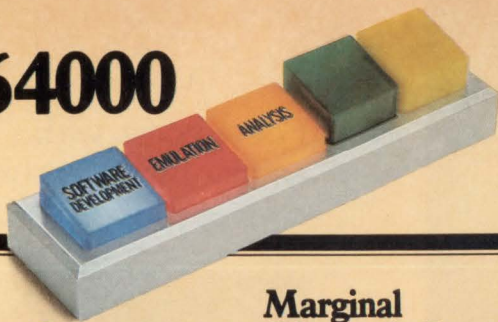


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CIRCLE 80

HP's 64000



Logic Development and you won't worry

Timely Processor Support

Ever have to settle for a second-choice microprocessor because language and emulation support wasn't available for your first choice? Put HP's 64000 Logic Development System in your lab and that frustration is gone.

That's because HP's microprocessor support strategy results in assemblers and emulators for virtually any 8- and 16-bit microprocessor...well ahead of the support available from manufacturers.

How is that possible? With the 64000 system, you can select the tools to build your own assembler and emulator. For assembler support all you need are the instruction set of your processor and HP's user definable assembler. Easy-to-follow instructions will have you assembling code in a matter of hours.

As for emulation, once you have the chip, our Universal Emulator lets you get to work in an execute-only environment in just a few days. And full emulation capability is typically just a matter of weeks. Because we supply hardware and software that's about 80 to 90 percent complete. You do some interface design and complete the software package. Everything you need is supplied, including step-by-step instructions and a design example using a popular microprocessor. Compare this approach to the year or two you'd wait for normal support...if you get it at all. HP also provides full support for a host of 8- and 16-bit processors, with more on the way. So don't let lack of support slow you down or compromise your designs.

Marginal Signal Conditions

No need to let marginal signal conditions and other timing related gremlins hold you up either. Because the 64000's timing analysis subsystem combines sophisticated triggering, high speed, 8k memory depth, and postprocessing for measurement capability not available in timing analyzers until now.

For example, our dual-threshold mode identifies noise problems and marginal signal levels. And helps you solve bus loading and bus conflict problems.

In the fast mode, 400 MHz speed yields the resolution necessary to resolve critical timing margin problems. New statistical analysis capabilities increase resolution and give useful data for system characterization. And the ability to trigger on transitions, pattern durations and post-processed data conditions give you valuable capabilities in studying control-signal timing relationships such as handshake related problems.

The 64000 Timing Analyzer sets new ease of use standards too. Directed-syntax softkeys simplify measurements. And label assignment lets you analyze results in terms of your system's nomenclature.

With this analyzer, you get to the root of timing problems fast.

Hardware/Software Fingerpointing

Whose fault? Software or hardware? The 64000, with both timing and state subsystems, and even emulation, can resolve that quarrel in short order. That's because one subsystem can arm or trigger another for real-time interactive measurements.

For example, you can set the timing analyzer to trigger on a middle threshold that lasts too long. Then view state flow to see the affect. Or, you can trigger on state and view timing, which is useful for debugging I/O port malfunctions.

In analysis/emulation interaction, you might monitor software activity with the analyzer, then send a signal to the emulator to halt operation if a specific trace specification occurs. Now, you can study the analyzer trace listing around the suspected problem area. Or, use the emulator to examine register contents and control further operation.

Take this logical path in settling fingerpointing debates and you'll push those designs closer to production.



System...standardize on a system like this about problems like these:

Software Bottlenecks

The 64000, with software performance measurement capability, quickly eliminates these nightmares. Symbolic tracing makes measurements a programmer's dream. And histogram displays give you a graphic picture of bottlenecks and software inefficiencies. This new tool shows system activity as a function of software modules so you can see where the concentrated action is. You can determine how long it takes to execute a given module of code as you vary input parameters. See software traffic patterns. And compare software modules in terms of the percentage of time and occurrence they require in your programs.

These measurements are real-time, not post-processed trace data, which means you can interact with trace displays as well as perform overview measurements on single-shot events.

Software in the Weeds

That's where new software often ends up. But the 64000, with the state analysis subsystem, gets you back on track quickly. First, because this analyzer speaks a programmer's language. Symbolic tracing lets you define parameters in familiar source-code symbols and labels. For example, you can instruct the analyzer to find sequences and trigger points by module names and labels. And with HP's directed-syntax softkeys, defining a measurement is usually just a matter of a few keystrokes.

Inverse assembly means this analyzer speaks your microprocessor's language, too. That makes it easy for you to interpret displayed information, because now you don't have to convert analyzer displays to microprocessor mnemonics and symbols. All this in a real-time analyzer, not a simulator or intrusive run-until-search type of analyzer.

But it's also important to be able to position the measurement window with precision. We do that too.

Extended trace specification features let you navigate through complex code to the portion you want...and display only pertinent information. That's because you can combine trigger, store and count functions in any combination, to a total of eight terms, each as wide as the number of channels installed (to 120). Add to that the ability to define up to 15 sequence terms, or a combination of sequence terms and enable/disable windows, and there aren't many nooks or crannies where software bugs can hide. That means you'll debug software pronto.

One System for Standardization

From start to finish of the development cycle, HP's 64000 Logic Development System can help you speed your designs along. It covers software development, downloading, emulation, hardware and software analysis, and system performance measurements. All with a single keyboard and display that speeds setups and simplifies measurements.

You can choose from two system stations, too. One benchtop station, with 10 card slots, gives you the most expansion capability. The transportable station, with 5 card slots, is a popular development unit for individual bench and field use.

Whichever station you choose, you can configure for dedicated function or combination measurements. You can use each in a standalone situation or as part of a multiuser, distributed processing network. It's a development system that makes sense for labs both large and small.

For details on the 64000 Logic Development System and available subsystems, call your local HP sales office listed in the telephone directory white pages. Ask for your HP field engineer in the Electronic Instruments Department.



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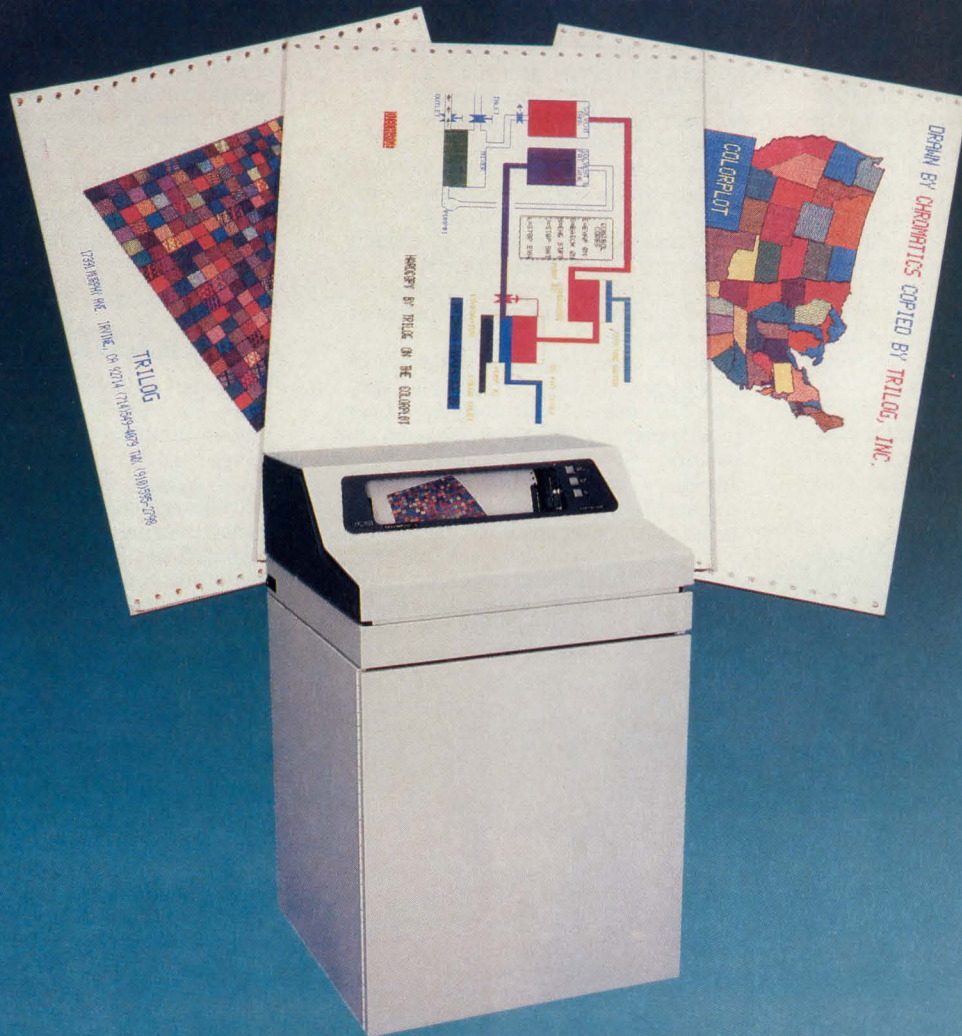


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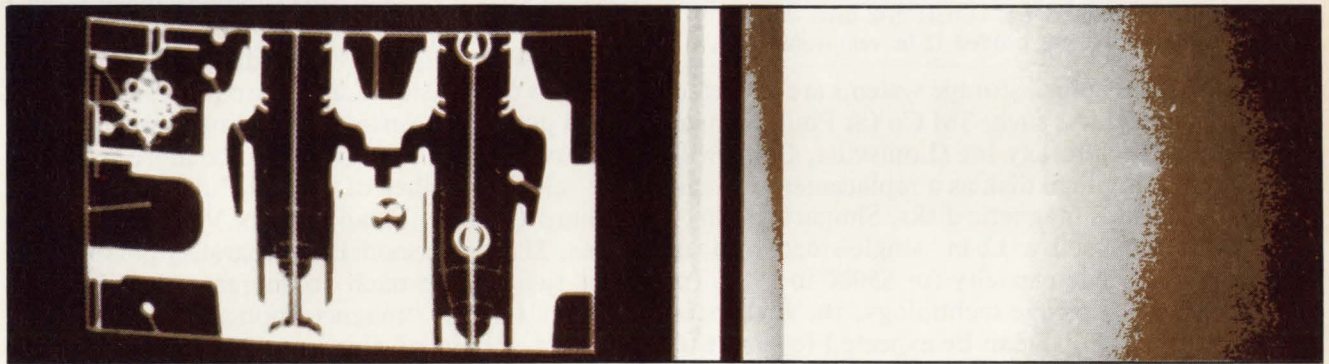
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CIRCLE 82



MASS MEMORY, TERMINALS, AND PRINTERS SPARKLE



by **Nic Mokhoff,**
Senior Editor

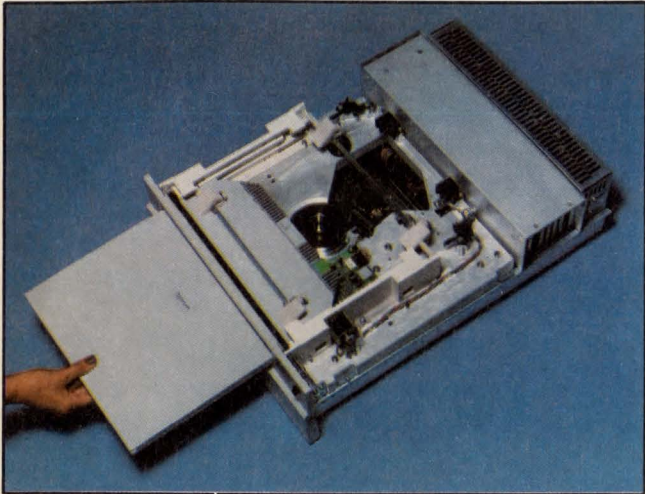
In the past year, mass storage media have increased in storage capacity while decreasing in size and cost. Witness the floppy disk arena, where a slew of microfloppies in the sub-4-in. size are boiling in the stew of their own standardization effort. These microfloppies have achieved the storage capacity of their 5¼-in. siblings, in some cases approaching that of 8-in. disks. Higher density in a smaller package with similar performance has resulted from the basic thermal and hygroscopic properties of the coated Mylar media. The magnitude of the thermal expansion increases proportionally with disk size. Thus, a smaller disk will expand less and thereby achieve a higher track density.

Despite the advantages of smaller drives, however, by not standardizing on one microdiskette, the overall benefit to manufacturers is diminished. Several standards currently exist that are being adhered to by such companies as Sony (Tokyo, Japan), Tandon (Chatsworth, Calif), Hitachi (San Jose, Calif), IBM (San Jose, Calif), Canon (Lake Success, NY), Toshiba (Tustin, Calif), and others. Their product capacities range from 40 to 500 kbytes and include

single- and double-density formats. Complementing this less than 4-in. community are, of course, a host of 5¼-in. floppies, and a new breed of 5¼-in. mini-Winchester drives just now appearing on the market. Plated thin-film media and thin-film heads allow up to 400 Mbytes to be stored on these 5¼-in. disks. For compatibility, two separate standard efforts have agreed on a 10-Mbit/s data transfer rate in a nonreturn-to-zero format with a separate clock signal.

Meanwhile in the 8-in. arena, Hitachi has developed a slim-line floppy disk drive that can store up to 9.6 Mbytes of unformatted data, which is about a sixfold increase over conventional 8-in. floppy disk drives. The drive's data transfer rate is 1.5 Mbits/s at a 168-ms access time. The track density of 96 tracks/in. and recording rate of 20,560 bytes/in. are the result of using a microprocessor-controlled stepper motor and spreading a fine epitaxial magnetic particle material on the media, according to Hitachi. Manufacturers of 14-in. Winchester disk drives also continue to enlarge capacity while reducing the physical size of their drives. Capacity of these drives has increased into the 5-Gbyte range.

But, a more exciting mass media, the optical read/write disk may make a moot point of the whole magnetic media standardization effort. As a first



Shugart Corp's Optimem 1000 optical disk drive stores 1 Gbyte of data on a single-sided 12-in. removable disk.

step, write-once optical storage systems are expected to be introduced. As such, 3M Co (St Paul, Minn), and Storage Technology Inc (Louisville, Colo) will be offering an optical disk as a replacement for the 8- and 14-in. hard magnetic disks. Shugart (Sunnyvale, Calif) will sell a 12-in. single-sided optical disk with a 1-Gbyte capacity for \$5000 in 1984. In the mainstay of storage technology, the high performance optical disk can be expected to beat the 14-in. removable disks, with capacities in the 2- to 4-Gbyte range, transfer rates of 3 Mbits/s, and access times of less than 100 ms. Twelve- and 5¼-in. optical disk replacements will follow suit as the market demands.

For secondary storage needs, the ubiquitous tape drives remain the most popular choice for backing up Winchester and hard disks. Tape types range from quarter-inch cartridges to half-inch streamers, and even videotape—for the 8-in. Winchesters. To minimize size and maximize appeal to desktop applications, manufacturers are housing tapes in various packages. MegaTape Corp (Duarte, Calif), for instance, has developed a drive that houses a half-inch cartridge tape—an industry first. Until now, only quarter-inch tapes were packaged in cartridges. The MegaTape unit is a dual-reel cartridge that records on 24 channels with a twin-channel read/write head. The unit strobes up to 300 Mbytes of data at a density of 9600 bits/in. As with disks, no two tape units are exactly the same. This leads to incompatibility problems.

Standardization efforts have proceeded for the quarter-inch tape devices. A group of about 30 companies has established the controller interface and recording format. For half-inch tapes, one company may upset all efforts by competitors to gain market share. IBM is expected to offer a half-inch tape drive as a backup to the IBM PC XT and the newly released

XT/370. As in other segments of the electronics industry, when IBM announces a product, its competitors either follow suit by trying to achieve compatibility with the product, or they simply drop out of the race.

One technique that is being increasingly applied to all sizes of storage media is perpendicular recording (see article, Jan 1983, p 89). Mass memory units that incorporate this technique are expected to boost capacity limits 50 to 100 times over current manufacturers who utilize horizontal magnetization techniques.

The most ambitious efforts in developing the vertical recording technique have been pursued by Japanese companies. Toshiba has announced a flexible disk drive that reportedly exhibits a linear density of 20,000 flux reversals/cm. With a track density of 57 tracks/cm, a 3½-in. disk can thus hold 3 Mbytes on one side. Lanx Corp (San Jose, Calif), is also pursuing a vertical recording storage media, but flux densities are expected to be more conservative—along the lines of 10,000 flux reversals/cm.

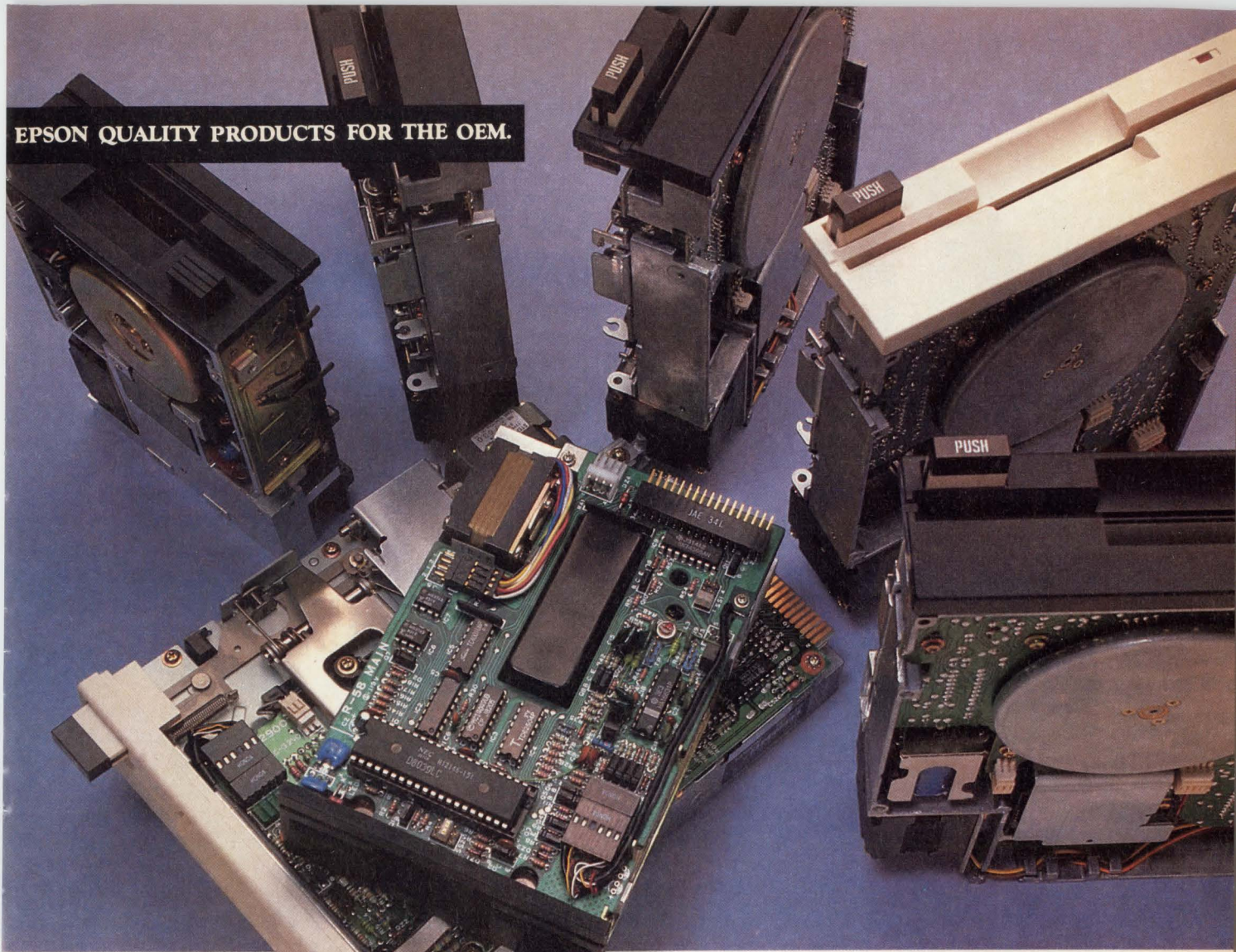
Sharp (Tokyo, Japan) and N.V. Philips (Eindhoven, The Netherlands) are separately pursuing the most radical approach to increase density on a medium. Labeled "magneto-optical recording," the chief advantage of this combination is that the reading operation is independent of the amount of magnetized material used. This results in potentially better signal-to-noise ratios for equivalent aerial densities. Prototype 2-in. disks released by Philips exhibit storage capacities 10 to 100 times greater than conventional 5¼-in. floppy disks.

Standards in doldrum

With a plethora of mass storage and drives available from as many companies, users are having trouble keeping up with new controller and interface requirements. To avoid disaster, disk manufacturers are starting to incorporate some intelligence within their drives to decouple the peripheral units from the computer they serve. In addition, serious efforts to define interface standards continue. Two factions have emerged. The first is the Enhanced Small Disk Interface (ESDI), derived from the long standing *de facto* standard developed by Seagate Technology (Scotts Valley, Calif) for their small drives. The second group of companies backs the standards proposed by the American National Standards Institute (ANSI), which are specific to 8-in Winchesters. The principle difference between the two proposals is the transmission media between the controller and the drive.

The ESDI specifies a serial interface using many single-conductor cables for both data and control. The ANSI, on the other hand, calls for a parallel bus

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Max. Capacity (2 Sides) (Unformatted)	500 KB	1000 KB	500 KB	1000 KB	1604 KB	500 KB
Drive Motor Speed	300 RPM	300 RPM	300 RPM	300 RPM	360 RPM	300 RPM
Track Density	67.5 TPI	135 TPI	48 TPI	96 TPI	96 TPI	48 TPI
Access Time	6 msec	3 msec	6 msec	3 msec	3 msec	15 msec

Extraordinary is the best word we could find to describe the new Epson family of 3 1/2" and 5 1/4" floppy disk drives. Because there is nothing ordinary about them.

The 3 1/2" drives, for instance, feature two-sided capacities up to 1MB. And some draw so little power they can operate on batteries.

The half-height 5 1/4" drives offer capacities from 500KB to 1.6MB and access times down to 3 msec. And the one-third height 5 1/4" drive is the industry's slimmest.

But that's only part of the story. What really makes them extraordinary is the fact that they're Epson drives. Designed and built by the people who have made "quality in quantity" their trademark around the world.

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The unique head stepping arrangement of MegaTape's MT-1220 high capacity cartridge streamer permits 30-s recovery of any stored file, making the drive ideal for archiving applications.

that uses a single 50-conductor flat cable carrying multiplexed data and control signals. Whose standard will predominate depends primarily on which company floods the market with products that incorporate one, or that use a better interface and control version.

Standards are also a hot topic in the graphical terminal arena. This was the year that the Graphical Kernel System (GKS) made a mark with American terminal manufacturers who are trying to be compatible within their graphics community. GKS gained a major backer when Tektronix (Beaverton, Ore) introduced its PLOT 10 GKS software package which, when used as the terminal operating core, can have application programs transported from one graphics system to the next. The standard was originally developed in West Germany and is considered easier to implement than Core, an older graphics standard



The Lundy S6100 workstation, with 448- x 1024-pixel graphics, introduces GKS functionality to the U.S.

specified and approved by members of the International Standards Organization (ISO). ANSI, for its part, is developing a virtual-device interface standard that would make all interfaced graphics hardware output from such devices as plotters, smart printers, and CRTs appear the same.

Lundy Electronics & Systems Inc introduced the first graphics workstation in this country to incorporate the GKS functionality. Its S6100 series of workstations are 1448- x 1024-pixel terminals that have all the fundamental GKS functions. These include displaying primitives with individual and bundled attributes, segmentation, workstation transformation, and an integral GKS input model with logical device support and Prompt/Echo types. Thus, applications can now be transported from the Lundy terminal into other terminals without having to rewrite the core software.

The printed word excels

Currently, of course, output from hardcopy devices is not all the same. Take the printer industry. This year printer introductions have become a weekly occurrence. For the most part, the distinguishing characteristic of the new announcements has been form and style more than function. There were some exceptions. Southern Systems Inc (Fort Lauderdale, Fla) started selling a page printer that is based on ion deposition—a technology developed by Delphax of Canada. The Mercurion 1 is a nonimpact, letter-quality page printer that can output 60 pages/minute and can be an economical alternative to laser xerographic printer systems and a direct replacement for high speed impact line printers. Its \$60,000 price tag is about half that of comparably performing xerographic printers. The printer uses plain paper and incorporates up to eight resident fonts. It can be installed as a direct replacement for an impact line printer without making any operating system software changes.

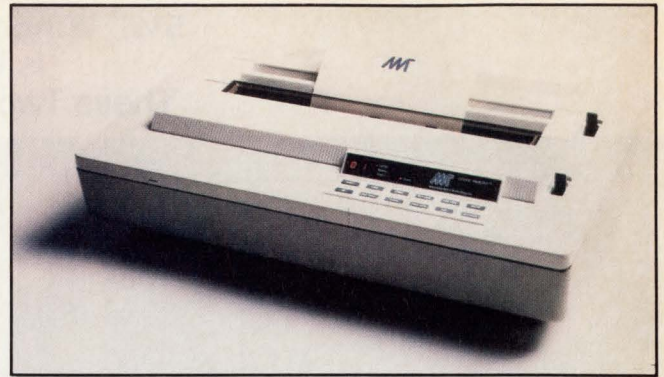
Compared to the xerographic process that usually requires six steps, the ion deposition method is hailed as more reliable since only four processing steps are necessary. The four steps include image deposition, development, transfixing, and cleaning. Couple that with the simplicity of using a dielectric drum instead of a sensitive photoconductor drum (used in laser printers) and the Mercurion 1 sustains only one failure per 500,000 copies. The company claims that the machine was designed to experience only one failure per month under heavy duty operation. The printer is compatible to run with major computer systems including those of IBM, Digital Equipment Corp (Maynard, Mass), Data General (Westboro, Mass), Harris (Melbourne, Fla), Gould/SEL (Fort Lauderdale, Fla), and others.

Although the nonimpact printer market is the fastest growing segment overall—it is expected to reach \$7 billion by 1987—the major segment of the current market is still in the impact area. And while it is true that the more innovative technologies are being developed for nonimpact machines, a few impact companies have advanced well-known techniques to offer a product that always seems a notch above its predecessor in form as well as function.

Innovations also do not always come from well-established firms. One startup company, for instance, has come very close to offering a dot-matrix impact printer that equals the letter-quality printing usually observed in full-character printers or in efficient, inexpensive nonimpact printers such as ink jets and thermal-transfer machines. Advanced Matrix Technology Inc (Newbury Park, Calif) embarked on its course last year to design what it calls its Office Printer. At this year's Comdex, the company was taking orders for shipments (beginning next year) of a letter-quality printer that outputs at 45 chars/s. It sports a black-and-white and color resolution of 240 x 720 dots/in., with a manufacturer large-quantity price of less than \$2000. The printer is a multimode device that carries the type fonts most commonly used in the business office and also has options for bar-code generation. Two other modes allow printing at 100 chars/s in the "memo" mode, and 250 chars/s in the "draft" mode. The Office Printer is a high quality printing unit for common business applications. It has all the daisy wheel and matrix printer features for performing data and word processing tasks where usually a number of printers are required, according to the company.

An elegant combination

Advanced Matrix Technology, for its part, attributes its high achievement to the close blending of mechanical and electronic engineering. Mechanically, the chassis unit consists of a single-piece stamped and deep-drawn metal part that accounts for minimum vibration during printing. This enables the carriage assembly to achieve a steady-state velocity without any rattling and rolling. A stepper motor and a lead screw-nut combination allow for accurate dot placement while software adjustments are constantly made to minimize printhead and system oscillations. Letter-quality printing is achieved by having the printhead make two consecutive passes in the same direction. Before the second pass, a microshift mechanism on the printhead shifts it 0.0042 in. in the vertical direction, which results in a quarter-dot displacement. Thus, there is a 240-dot resolution in the vertical direction. The printer achieves a 720 horizontal-dot resolution by ensuring a 1/720-in. position accuracy through firmware control.



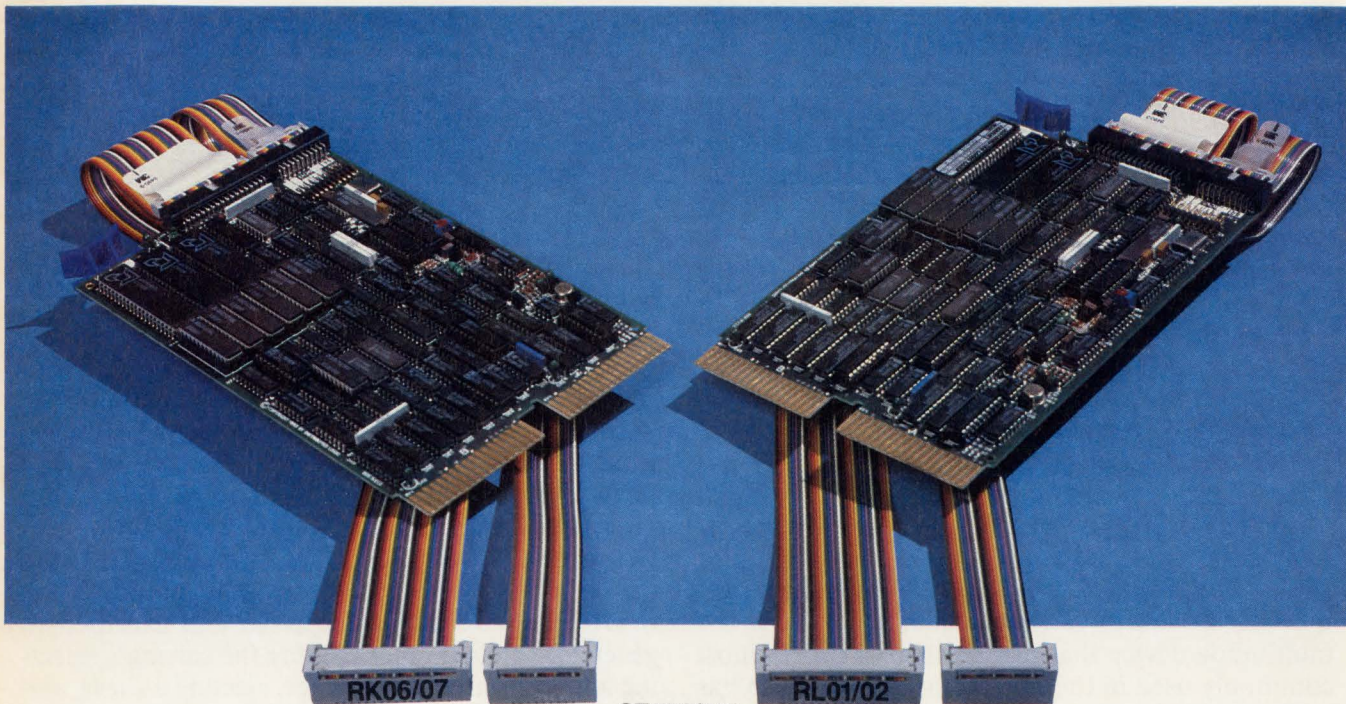
Printing 45, 100, and 250 chars/s, the Office Printer from Advanced Matrix Technology Inc can print in letter quality, memo, or draft mode in black-and-white or color.

Another achievement incorporated by the designers was a proprietary black nylon ribbon that—in contrast to Mylar single-pass ribbons (capable of producing 250,000 to 300,000 characters before replacement)—can be used for up to 20 million data processing characters and four million letter-quality characters. The electronic printer driver is software driven from the host computer, which sends codes to it. These are then interpreted and executed to generate such actions as moving the carriage, selecting a font, printing a character, ejecting a sheet, and others. Both serial (RS-232) and Parallel (Centronics) interfaces are supported. In addition, access is assured to the Z80 microprocessor control bus for custom configurations by manufacturers.

Other printer innovations this year included ink-jet machines that not only outputted paper copies but also printed on acetate transparencies, thereby offering the user a break in generating overheads. Ramtek (Santa Clara, Calif) and Siemens' Print-color subsidiary (Norcross, Ga) have introduced such units, and Advanced Matrix Technology plans to offer a transparency option on its dot-matrix printer.

Laser printers, for their part, have remained the workhorses of volume paper output applications. This type of printer is, however, decreasing in size. Two similar-sized units stand out among the crowd. Both the Xerox 2700 and General Optronics Corp's (Edison, NJ) Holoscan 28 are less than 40 in. high and less than 30 in. wide and deep. There are differences, however. The Xerox unit prints 12 pages/minute and costs about \$18,000 while the Holoscan 28 prints 28 pages/minute and costs \$12,000. Holoscan's 300- x 300-dot/in. resolution is achieved by a printing method that combines the xerographic process in the Xerox machine with a holographic process. In essence, a semiconductor laser beam raster scans the image and holographically deflects it onto a photoreceptor. The rest of the process is the xerographic image transfer onto plain paper.

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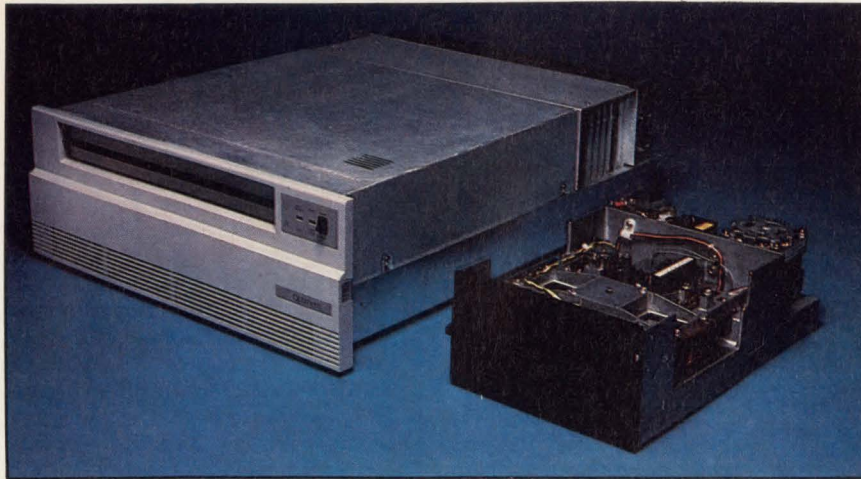


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High capacity optical disk system appears at last



Shugart Corp's Optitem 1000 laser-based optical disk drive (left) is shown beside an SA801 8" floppy for size comparison.

Until recently, optical memory aimed at computer systems has been basically a laboratory project. But the Optitem 1000, a 1G-byte optical disk from the Optitem Division of Shugart Corp (formerly Shugart Associates), is about to appear for 1984 systems.

The Optitem 1000 produces a "write-once, read-often" disk—it cannot be erased and rewritten, since the laser permanently deforms the reflective material in the process of writing. This was viewed as a disadvantage when the technology

was first investigated, but it is now seen as a way of creating archival computer records.

Magnetic records decay over time, and valuable data and imagery can be lost. However, the optical medium used in this system has a very long lifetime. Although no body of experience with the medium exists as yet, testing indicates that it should survive in readable condition for several decades.

The system uses a gallium aluminum arsenide semiconductor laser operating at

a nominal wavelength of 830 nm and a peak power level of 15 to 20 mW, to write data on one side of a 12" optical disk. Data are written as circular or slightly elliptical bubbles in the proprietary reflective disk surface developed by Thompson-CSF (Paris, France). Since the track width is, in effect, the width of a data bit, the bpi and tpi are equal at 14.5k. Reading is done with the same laser, but at much lower power (1 to 2 mW). Laser light is reflected from the data surface and detected by a photodetector. Lack of a signal, due to a dark area produced by a bubble in the surface, is interpreted as 1 bit.

The Optitem 1000's dimensions are 7" x 17.6" x 24" (18 x 44.7 x 61 cm), and it weighs approximately 50 lbs (23 kg). Price for the system is approximately \$10,000 in unit quantities, and \$6000 in quantities of 500, with appropriate OEM discounts. A Small Computer System Interface (SCSI) bus controller is in development, but pricing has not yet been determined. Evaluation units are scheduled for shipment in the first or second quarter of 1984, with volume shipments expected in the third or fourth quarter. **Shugart Corp, Optitem Div, 475 Oakmead Pkwy, Sunnyvale, CA 94087.**

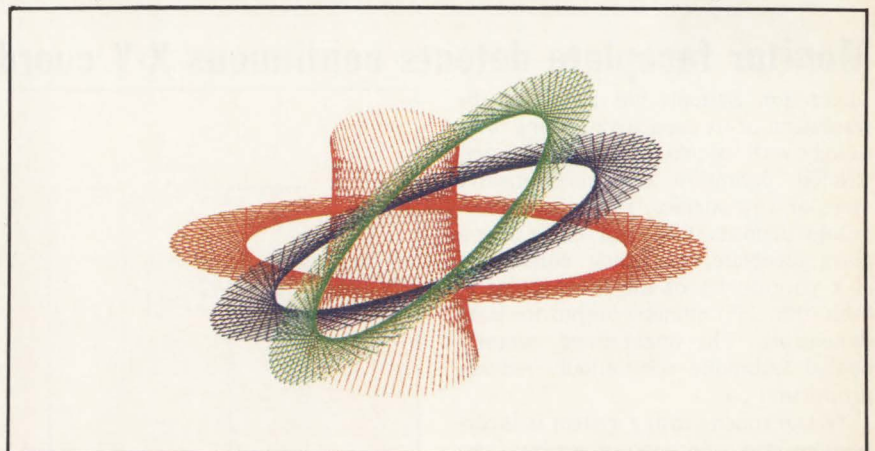
—Sam Bassett,
Field Editor

Circle 306

Ink-sheet copier blends color print and thermal transfer techniques

D-SCAN 5201 produces full-color copies of complex graphics directly from CRT displays in under one minute. To further enhance productivity, local video memory stores images before the output copies are generated, freeing the graphics workstation for continuous use. Copies come out on markable, fade-resistant paper with a 150-dot/in. resolution. Per-copy cost is \$0.25.

Seiko's ink-sheet technology forms copies over a line-type thermal head. The head transfers pigment dots from a wax-coated, three-color banded ink sheet to a sheet of normal grade paper that overlays the ink sheet. In turn, with images transformed onto plain paper, cyan, magenta, and yellow combine to create a palette of eight saturated colors, including red, green, blue, black, and white. Apart from the standard and ink-sheet paper rolls, no resupplies, such as toner or ink, are needed. Final copies are



automatically cut to standard 8.5" x 11" letter size.

One half of the D-SCAN 5201 controls critical ink-sheet and paper movements, and the other manages electronic duties such as input control, formatting,

storing, and CRT graphic data output. The machine measures 26" x 12.8" x 17.5" (66 x 32.5 x 44.5 cm) and weighs 130 lb (59 kg). **Seiko Instruments U.S.A., Inc, 2620 Augustine Dr, Santa Clara, CA 95051.**

Circle 307

Thin-film heads/plated disks are Winchester features

The Cricket Winchester disk drive (CDC 9270-6) consists of read/write and control electronics, read/write heads, a track positioning actuator, media, and an air filtration system. The 3½" disk drive was specifically designed for the OEM market.

The drive provides 6.38M bytes unformatted and 5M bytes formatted storage



capacity. It is timing and format compatible with the industry standard ST506 interface that transfers data at a 5M-bps rate. Average seek time is 117 ms using a band stepper positioning method. Linear recording densities are 15,390 bpi and 450 tpi.

Using LSI circuit technology, the Cricket fits all drive electronics on a single PC board that is approximately one-third the size of boards used in 5¼" Winchester drives. The drive measures 1.63" x 4" x 6.37" (4.14 x 10 x 16.18 cm).

The drive operates with a direct-drive, brushless dc motor that rotates the spindle at 3566 rpm. A closed loop digital servo system uses servo information written on each track at the index mark. When a seek operation is done, the servo information is read and an internal microcomputer corrects track misalignments. The band actuator (connected to the stepper motor shaft) positions the

read/write heads. Accurate positioning is performed by a stepper that stops at 0.9° per step.

These Winchesters use thin-film flying heads and a negative pressure air-bearing slider. Such a technique allows a lower head flying height and reduces the force of the self-loading heads. Thin-film heads and nickel-cobalt plated media also allow a design MTBF of 30,000 operating hours and an estimated service life of over five years. No preventive maintenance or operating adjustments are required.

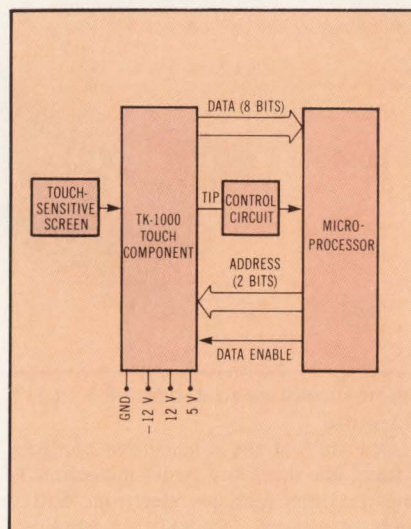
Data reliability specifications include recoverable read errors of 1 in 10¹⁰ bits read, unrecoverable read errors of 1 in 10¹² bits read, and seek errors of 1 in 10⁶ seeks. Power requirements are 5 V (±5%) at 0.6 A (0.7 A surge) and 12 V (±5%) at 0.9 A (1.6 A surge). Power dissipation is 14 W.

The drive has applications in small business systems, intelligent terminals, personal computers, word processing systems, and portable computers. In OEM quantities, the Cricket is priced at \$465. **Control Data Corp, OEM Product Sales**, PO Box 0, Minneapolis, MN 55440. **Circle 308**

Monitor faceplate detects continuous X-Y coordinates

Interaction Systems has improved the resolution of its capacitive-sensing technology with TK-1000, which allows unrestricted definition of touch-sensitive areas on one surface. Proprietary technology deposits indium tin oxide over a glass faceplate, providing continuous X-Y coordinates of the touch point in 8-bit (0 to 255) numeric output for both dimensions. The unpatterned, temper-coated technique substantially reduces production cost.

TK-1000 touch-sensing system is incorporated into a microprocessor bus, and will control both video-based and computer-generated displays. It consists of the faceplate, a connecting cable, and a 2.5" x 2.5" x 0.75" (6.4 x 6.4 x 1.9-cm) component that outputs 8 bits of data and a "touch in progress" (TIP) signal.



When a person touches the screen, the touch component detects an impedance change and lowers the TIP line. Control logic can program the microprocessor to monitor the TIP at intervals, or to provide an interrupt to the microprocessor. The microprocessor then reads X and Y coordinates from the touch position via address and data enable lines.

The system can be used alone or in conjunction with a keyboard. Moreover, with TK-1000 the computer will recognize letters drawn onto the video display. Directly touching the desired location will also move the cursor for adding or deleting text, which can replace conventional keyboard entries or "mouse" manipulations. **Interaction Systems, Inc**, 24 Munroe St, Newtonville, MA 02160. **Circle 309**

Color printers integrate text and graphics on plain paper



Series 200 EPM (photo) employs a solid state raster line printhead that produces 200 dots/in.² on smudge-free plain paper. Because the printer is based on nonimpact technology, it can be programmed to generate a virtually unlimited array of text and graphics characters and symbols.

The 8.27" (21-cm) wide printhead has over 200 nibs/in., with an "all points addressable" feature for graphics. The printer processes up to six pages each

minute—equivalent to about 300 lines/min. Built-in sheet feeder and output stacker manage paper flow.

Series 200 input is a 1-MHz video bit stream, which is buffered internally, then fed to the printhead one raster scan line (1680 pixels) at a time. The image is transferred to paper from the ink donor roll, which consists of thin backing material coated with a nondegradable dry ink. Thermal nibs melt the ink on the donor roll just before a pressure roller pushes it against the paper. Each donor roll produces up to 1300 pages.

A second release, the Series C ink jet printer, also uses plain paper—either cut sheets or rolls—and prints 20 cps with 120-dot/in.² resolution. Clay-coated paper can be used for high quality color printing. The ink dries on standard paper in 1 s.

Sixteen-nozzle head featuring drop-on-demand technology can put a dot of

ink virtually anywhere on the page. The desktop unit uses four nozzles for each of four colors producing a total of seven: cyan, black, magenta, yellow, violet, green, and red. The ink jet generates color backdrops, halftones, multiple color intensities, and complementary imaging. Five halftone levels are available for printing graphics.

When printing text, the unit employs a four-pass mode that generates 12 x 16 resolution; when printing special graphic mosaics or symbols, a five-pass mode prints with 12 x 20 resolution. The 96-character ASCII set and 64 mosaic characters are stored in PROM. Besides the U.S. configuration, five standard European character sets are available: French, Norwegian/Danish, Spanish, German, and British.

Series C ink jet printers will be available in the 3rd quarter 1983, at about \$1250. Series 200 EPM is available 90 days ARO and lists at \$4995 quantity-one. **Diablo Systems, Inc.**, 24500 Industrial Blvd, PO Box 5003, Hayward, CA 94545.

Circle 310

Winchester 5¼" drive packs 140M bytes on eight disks

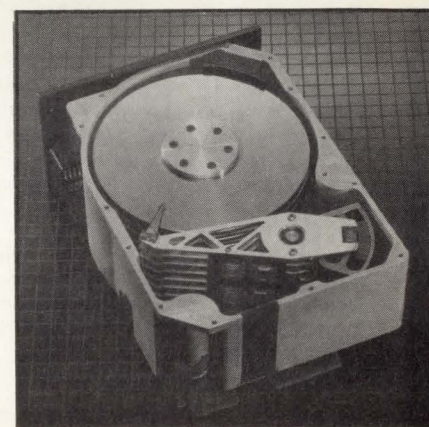
An innovative Winchester design gives the XT-1000 series 5¼" drives 140M-byte capacity and an average access time of 30 ms. The proprietary integral hub/dc motor design, with the spindle motor inside the disk hub, provides a deeper base casting and thus allows eight mini-floppy disks to be stacked inside the enclosure.

A flexure design derived from ferrite recording heads with Whitney-type sliders (IBM 3380 technology) is incorporated instead of the conventional 3350 style head flexures used on many smaller Winchester. This Whitney design allows a closer disk spacing to accommodate the increased number of platters per package. It also provides improved aerodynamic stability for the flying head, better head to disk compliance, and an improved signal to noise ratio. Additionally, the Whitney head/flexure design utilizes more of the disk surface to increase the total number of tracks per disk surface to 918. This flexure/head concept will also allow thin-film read/write heads that provide at least

50% increased recording densities to be easily incorporated as they become available in low cost production quantities.

Currently ST506/412 compatible, subsequent drives are planned that will utilize intelligent interfaces such as Shugart's SASI. Although the read/write channel design is already optimized to handle MFM codes, when SASI is implemented, user transparent run-length limited (RLL) codes may be used on future generations of the drives. Through RLL codes, a 50% increase in storage capacity per disk can be realized with no corresponding increase in flux density.

XT-1000 drives use the 30-ms access time Maxtorq rotary voice-coil actuator to position the heads on the disks. The rotary voice-coil design has 80% of its copper in the magnetic field throughout movement to improve torque. The closed loop servo system, dedicated servo surface, and plated recording media provide recording density of 980 tpi. Miniaturized LSI ICs packed on the single Maxpak PC board work as functional TTL circuit equivalents, while occupying 50% less



space. Rotational speed is 3600 rpm; average latency is 8.33 ms; and transfer rate is 5M bps.

Three models will be provided, ranging in unformatted capacities of the 65M-byte 4-disk XT-1065 (\$1520), the 105M-byte 6-disk XT-1105 (\$2100), and the 140M-byte 8-disk XT-1140 (\$2690). **Maxtor Corp.**, 5201 Lafayette St, Santa Clara, CA 95050.

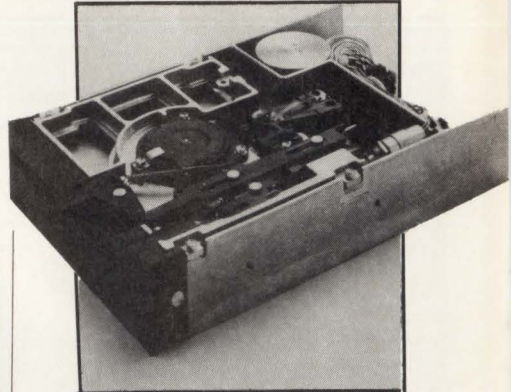
Circle 311

Half-height minifloppy holds 3.33M bytes

Drivetec's first product release, the 320 SuperMinifloppy, upgrades 8" and 5¼" floppy based systems and acts as backup for small Winchester based systems. It has 3.33M-byte unformatted capacity, 3-ms track to track access time, and a 500k-bps transfer rate. Double-sided, 192-tpi recording format maintains

downward compatibility with existing mini-diskettes.

A proprietary track-following servo system ensures ontrack read/write head positioning and diskette interchange between drives in different systems and environments. A two-stepper head positioning system moves one head to the



approximate track position, while the other adjusts the head in 200-µin increments to center it exactly.

Absolute vertical clamping gives accurate, repeatable diskette registration. A "gumball" head configuration positions two spherical heads opposite each other, so the elastic media following the heads forms a natural curve. This improves media wear characteristics over typical double-sided head configurations. Other key features include onboard microprocessor and brushless dc drive motor, buffered track seek, and door lock.

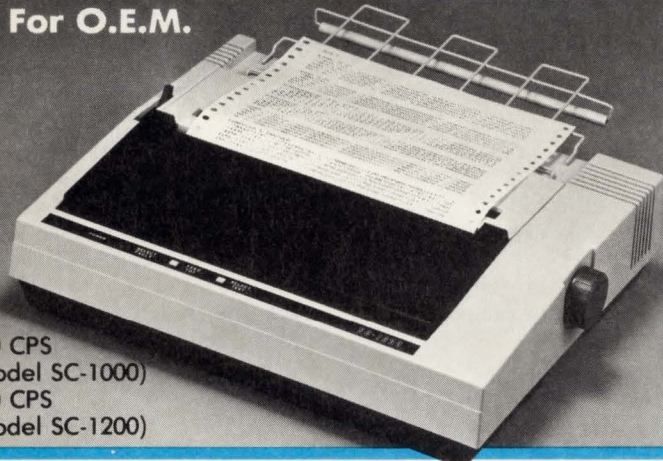
Each diskette contains 160 cylinders. There are 320 tracks (160/side), with 8192 bytes/track and 256 bytes/sector. MTBF is about 10k power-on hours. Soft read errors are approximately one in 10⁹, hard read errors one in 10¹², and seek errors one in 10⁶.

The desktop unit weighs 2 lb (0.9 kg) and measures 1.62" x 5.75" x 8.62" (4.11 x 14.61 x 21.89 cm). **Drivetec Inc**, 2140 Bering Dr, San Jose, CA 95131.

Circle 312

HIGH SPEED-LINE FEED DOT MATRIX PRINTER

For O.E.M.



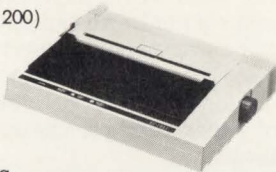
100 CPS
(Model SC-1000)
120 CPS
(Model SC-1200)

PRINTERS in standard models or built to meet your specific O.E.M. requirements. High Speed printing with totally 12 variations for character printing, including graphic printing.

Many, many fine features including:

- Low cost for volume users
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66 line/min. (SC-1000); 76 line/min. (SC-1200)

PLUS much more . . . write for illustrated literature and complete specifications on these High Speed, DOT MATRIX PRINTERS for quality computers, unsurpassed for value.



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Low cost color printer

Model 315 color printer has a four-hammer head design with a special rotating platen, with each of the four hammers printing one of four primary colors. Over 30 possible shades can be printed in a single pass of the printhead. This single-hammer/single-color design prevents color bleeding and contamination of the ribbon that can be caused by ink residue left on the hammer. The printer operates at 50 cps for both character and color graphics printing. Rated graphics throughput is 200 cps. Retail price is \$599. **Transtar, div of Omega Northwest, Inc**, Box C-96975, Bellevue, WA 98009.

Circle 313

Memory subsystems



Two peripheral subsystems combining an 8" Winchester disk drive, quarter-inch cartridge tape backup, switching power, and fan, come with a controller board that interfaces to most host computers. The 82.9M-byte model 8055 and 41.4M-byte model 4055 drives have a recording density of 9006 bpi and a data transfer rate of 1209k bytes/s. Average seek time is 30 ms (55 ms max), and the 3600-rpm spindle has an 8.33-ms average rotational delay. Companion four-track model 6455 tape transport uses serpentine recording. An adapter board converts its 8-bit bidirectional bus interface to meet the industry standard for half-inch tape transports. With this, the quarter-inch tape cartridge emulates a nine-track, reel-to-reel half-inch tape transport without operating system changes. Standard 3M-byte cartridges give unformatted capacities of 11.5M, 17.3M, and 23M bytes. Read/write speeds are 30 ips; data transfer is 192k bps with 6.4k-bpi recording density. Built-in 200-W switching supply provides Winchester, cartridge transport, and related electronics with 5, 12, and 24 V. Input voltage is from 110 to 240 V, 47 to 63 Hz. In quantity-100, system 8055 sells for \$5300, and system 4055, for \$4600. **Kennedy Co**, 1600 Shamrock Ave, Monrovia, CA 91016.

Circle 314

Double-density 3½" drive

An enhanced version of the 3½" micro-floppy disk drive is available. It is capable of storing 1M byte of data in double-density mode. The drive is approximately one-quarter the size and one-half the weight of conventional 5¼" drives and uses 50% less power. The

disk is encased in a semirigid cartridge-type housing for easy use and damage protection. Format specifications for the 3½" floppy disk are mutually compatible with 13 leading disk drive and media manufacturers. **Sony Corp, Data Products**, Sony Dr, Park Ridge, NJ 07656. Circle 315

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Touch-active system

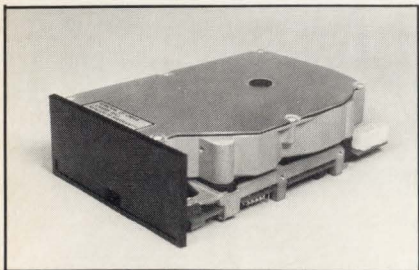


The Touch Information Display touch terminal uses opto-technology with no overlay. This technology gives a clear view of the screen and is difficult to damage. The display allows the user to define a variety of touch-active areas for more flexible programming in a wider range of applications. The interface is an RS-232-C and an ASCII port is standard. The display is 24 lines x 80 chars on a 12" screen, and the character set is 96 ASCII plus 32 special graphic symbols. The display sells for \$1400. **Electro Mechanical Systems, Inc.**, 801 W Bradley, Campaign, IL 61820.

Circle 317

Miniature Winchester

Series 350 hard disk 3 1/2" drives hold 5M and 10M bytes of formatted storage within one-quarter the volume of standard 5 1/4" Winchesters. The drives have the ST506 interface and 5- and 12-V power, but actual power consumption is less than half that of a standard 5 1/4" Winchester. Model 351 is a single-platter drive, and 352 a double-platter drive. Both use open-loop head arm positioning with a double-precision stepper motor. Data are recorded at 600 tpi with over 11,000 bpi. Average access time is 85 ms with a track-to-track access of 15 ms; data transfer is 5M bps. Physical dimensions are 1.625" x 4" x 5.25" (4.128 x 10 x 15.34 cm). **Rodime PLC**, 25801 Obrero, Mission Viejo, CA 92691.



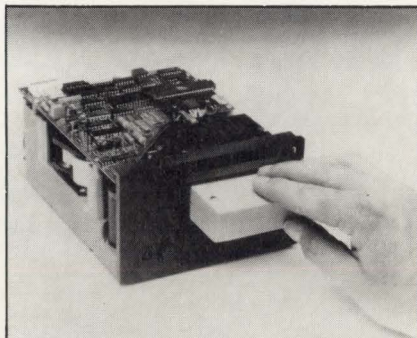
Circle 318

Small nonimpact printers

Two printers based on laser technology produce 300-dot/in resolution at a rate of 12 pages/min. Noise level under 55 dBA makes units suitable for the office environment. The HP 2687A desktop text model offers up to four character fonts/printed page; two reside permanently in the machine and two are user changeable. Several fonts, including Script, Courier, Letter Gothic, and Pica, are available in cartridge form. When used in conjunction with the company's word processing software, the HP 2688A text-and-graphics printer becomes a document generator that outputs charts, graphs, and diagrams. It also replaces preprinted forms by electronically storing them, then merging data and printing simultaneously. The 2688A combines up to 32 character fonts per page. Other features include page rotation and 2:1 or 4:1 reduction. Manufactured by Ricoh Co, the 2687A printer costs \$12,800. The 2688A combines Ricoh's laser printing technology with HP electronics and packaging. Including interactive formatting and graphics software, it costs \$29,950. **Hewlett-Packard Co.**, 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 319

Tape drive backup



A 1/2" streaming tape drive, the TM951 has a storage capacity of 50M bytes. Compatible with standard 5 1/4" flexible and Winchester drives, the device provides backup for computers with high capacity drives. Using a video-style single reel of 1/2" standard computer tape, the drive has a serpentine recording format on 20 tracks. Track density is 48 tpi, recording density is 6.4k bpi, recording speed is 40 ips, and data transfer rate is 250k bps. OEM prices range from \$500 to \$700. **Tandon Corp.**, 20320 Prairie St, Chatsworth, CA 91311.

Circle 320

Bidirectional four-density printer

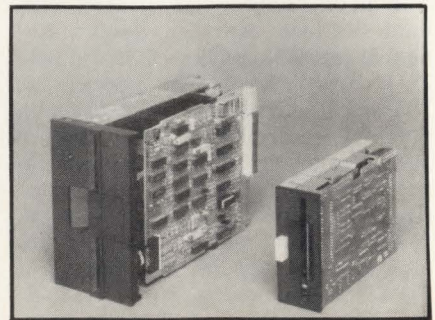


FX-80 bidirectional printer has 160-cps print speed and software selectable choice of elite (12-cpi) or pica (10-cpi) print spacing. Users can download special fonts into memory from the computer system. The 9 x 9 dot-matrix print has the same 1:1 graphics scale vertically as horizontally. Dot-addressable graphics capability and 2K-byte buffer are provided. Printer (\$699) provides characters with full descenders and is downward compatible with the Epson MX printer series. Proportional spacing, pin-and friction-feeds, standard parallel communication interface (serial or IEEE 488 interfaces optional), and four printing densities are featured. **Epson America, Inc.**, 3415 Kashiwa St, Torrance, CA 90505.

Circle 321

Microfloppy 3 1/2" drive

Standing 1.6" (4.1 cm) high, the single-sided SA300 3 1/2" microfloppy disk drive provides 500k-byte unformatted capacity, 135-tpi density, and 6-ms track to track access time. Drive's diskette is protected by a hard plastic shell, and the shutter is spring loaded to remain closed until media are inserted. With 80 tracks/surface and 300-rpm speed, the drive achieves 125k-bps (single-density) or 250k-bps (double-density) transfer rates. **Shugart Assocs.**, 475 Oakmead Pkwy, Sunnyvale, CA 94086.



Circle 322

Multi-axis hand controls

Force-operated hand controls feature four primary axes that can be expanded to as many as 10 proportional outputs. With application in teleoperator or robot programming, the 404 series has six different hand grip configurations with pure force in all axes or with force with limited motion in either two axes or all four axes. Model 531, a two-axis potentiometer type of joystick, features rugged all-metal construction. The unit provides direction or limit switches together with a finger-operated switch on the joystick handle as options. **Measurement Systems, Inc.**, 121 Water St, Norwalk, CT 06854. **Circle 323**

Double-sided 3½" drive

TM35 Microline disk drive provides 875k bytes on two sides of a 3½" diskette, 85-ms data access, and 3-ms track-to-track speed. TM35-2 is compatible with 5¼" standard interface, and provides 40 tracks/side, double-sided recording, 250k-bps transfer rate, and 500k-byte capacity. TM35-4 is compatible with the Sony OA-D30V microfloppy drive interface, software, and diskette, and has double-sided data recording. TM35-4 features 7610-bpi recording density, 135 tpi, and 70 tracks/side. TM35-2 model features 6255 bpi, and 135 tpi. Both models use FM/MFM recording. **Tandon Corp.**, 20320 Prairie St, Chatsworth, CA 91311. **Circle 324**

Reduced price printer

Dual-mode printer D-92 is available for \$399/unit, a 42.5% price decrease over the previous cost. Modular design enables specific upgrade selections by users. Dual-mode operation uses a 7 x 9 matrix font and an 11 x 9 matrix for near letter-quality documents. Features include 100-cps bidirectional printing, short line seeking logic, friction paper feed, parallel interface, 800-character buffer, six character sizes with each printing mode, 100M-character reusable printhead, and a 5M-character continuous loop ribbon cartridge. Full ASCII character set prints both upper- and lowercase characters at 40, 48, 66, 80, 96, or 132 characters/line. Options include RS-232-C serial interface, adjustable tractor feed, dot-addressable graphics, 9600-baud operation, 2K buffer, X-ON/X-OFF, control X/Y, and single-sheet feeder. **Data Impact Products, Inc.**, 745 Atlantic Ave, Boston, MA 02111. **Circle 325**

Smart optical mouse positioner

OptoMouse cursor controller encloses two rocker switches that roll on the X-Y axes of a flat surface, and communicates its movements to the computer and interface by a tail-like cord. Custom optical imaging system is incorporated for superior resolution. Unit requires

only 5 V from the host system. Controlled by its own microprocessor, it is designed with minimum parts count and can emulate existing graphics protocols such as Tektronix Plot 10 and Summagraphics bit pad. Host interface is via RS-232-C serial port. **USI International**, 71 Park Ln, Brisbane, CA 94005. **Circle 316**



Not communicating? The 232LT gets you talking.

Carroll's 232LT line tester/breakout box lets you examine the status of the RS-232 interface, simplifying troubleshooting and computer installation. Dual-color LEDs indicate the precise state—marking ($\leq -3V$), spacing ($\geq +3V$) or undefined (between $-3V$ and $+3V$)—for the twelve most frequently-used lines. An extra LED is provided for monitoring additional lines.

Each signal line contains a DIP switch which can be opened to allow cross-patching. Pins located on either side of the DIP switches are useful as test points for meters and oscilloscopes.

The 232LT is signal-line powered, eliminating the annoyance of batteries, and it has the additional advantage of using a minimum signal current. Each LED provides a 3mA load at typical voltage levels of $\pm 12V$. (Stacking three LEDs in parallel can provide a 9mA approximation to the 10mA current limit of RS-232 drivers).

Accessories include jumpers, extension cable, user's manual, vinyl carrying case, and a handy RS-232/ASCII reference card. Guaranteed for one year. Priced at \$175.00 (includes shipping); quantity discounts available. Distributor inquiries invited.

For immediate delivery or further information, call or write:



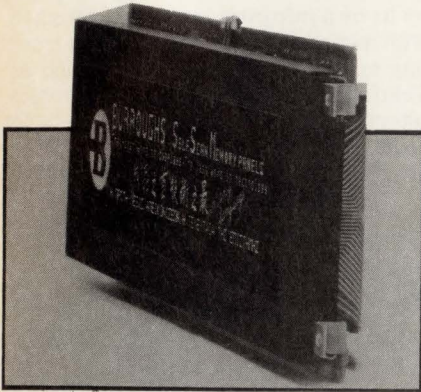
Carroll Touch Technology

a subsidiary of **AMP** Incorporated

2902 Farber Drive
Champaign, IL 61821

217/351-1700
TWX 910 245-0149

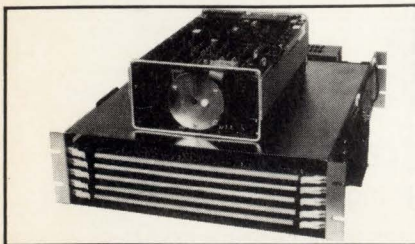
Flat-panel display



Self-Scan gas plasma display with memory is an 80-char line width, 400-char panel that can display both alphanumerics and graphics. The dc internal address feature is combined with a technology that incorporates an ac layer for storing data in memory indefinitely. The ac memory layer eliminates need for refresh memory electronics and, with 400-char display, reduces the number of required drivers from 656 to 25. Optional touch-sensitive overlay allows direct data input. Price for the 400-char model with driver electronics is \$625 in OEM quantities. **Burroughs OEM, Display Div, PO Box 1226, Plainfield, NJ 07061.**
 Circle 326

Voice processing subsystem

The VoiceStor model 30 is a voice storage subsystem for high level voice response and storage retrieval. The device records and plays back words, phrases, or sentences exactly as spoken. Its vocabulary is very flexible with no fixed limit on any element. Recording capacities vary from 100 s to 60 h, depending on the applications. It supports up to 32 simultaneous voice channels, allowing access to several sources on an async basis. The system interface is a standard RS-232-C control channel operating at a range of data transmission rates. **Voicetek Corp, 10 Dedham St, Newton, MA 02161.**



Circle 327

Touch-sensitive interface

Scanning infrared beams, rather than a screen overlay, are key to a touch-input system for two 12" VT100-compatible Datamedia terminals. Infrared LEDs and photo-transistor detectors mount around the video screen, creating a lattice of light beams in front of the display surface. A touch obstructs the light beams and causes X-Y coordinates to be transmitted to the computer. Optical devices are concealed by an infrared-transparent bezel, so the workstation looks like a conventional terminal. Choice of five operating modes for coordinate report format is user selectable. The touch-input system now works on the monochrome Excel 22 and the Colorscan 10 color graphics terminals. Single-unit price is \$1350. A version for the 14" Excel 24 is planned. **Carroll Touch Technology Corp, 2902 Farber Dr, Champaign, IL 61821.**



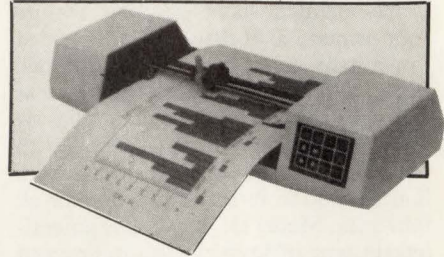
Circle 328

Cartridge disk drive

Beta-5, a 5M-byte capacity 5¼" disk drive, provides an ST506-compatible interface and conforms to industry standard 5¼" form factor. The drive uses flying media recording, rotary voice coil actuator, and track following closed loop servo to supply high performance, reliability, and areal density. The flexible media stabilization method, based on Bernoulli technology, supplies high resistance to shock and vibrations. This technology also requires no air filtration systems and results in fast cartridge replacement. Data transfer rate is 5M bps; recording is performed using MFM techniques at 17,373-bpi density. **Omega Corp, 4646 S 1500 W, Ogden, UT 84403.**

Circle 329

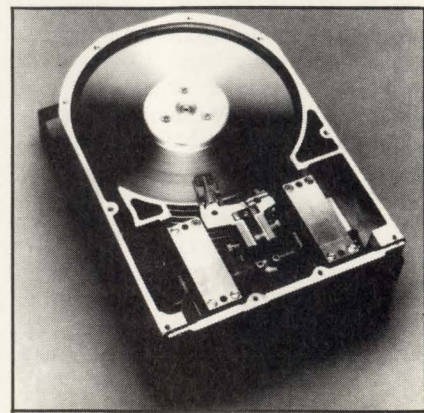
Portable plotter



DMP-40 single-pen drum plotter features pen speeds to 4.2 ips and format size to 11" x 17" (28 x 43 cm). Both pen and paper are directly driven by stepper motors. Step size is programmed to ensure resolution exceeding anticipated CAD/CAM or general plotting requirements. Unit generates circles, arcs, ellipses, and general curves on command. The five character sets resident in ROM can be presented normally or in italics with 255 sizes and 360° of rotation. Eleven line types are available. Plotter will also clip, window, viewport, and scale to size. Price is \$995. **Bausch & Lomb, 8500 Cameron Rd, Austin, TX 78753.**
 Circle 330

Winchester family

The 500 series of 5¼" Winchester disk drives features 32-ms access time and storage capacities ranging from 55M to 111M bytes. Model 502 has 4 disks storing 55M bytes while model 504 has 6 disks storing 86M bytes. Models 503 and 505 have 71M and 111M bytes of unformatted storage capacity, on four and six disks, respectively. The 502 and 504 specify a 0.625M byte/s transfer rate and 9212 bpi recording density. Specifications for the 503 and 505 are 0.806M bytes/s and 11,886 bpi. In quantities of 500, prices range from \$1550 to \$2500. **Priam Corp, 20 W Montague Expy, San Jose, CA 95134.**



Circle 331

Winchester 5 1/4" disk subsystems

V130, V150, and V170 offer 30.8M-, 51.4M-, and 72M-byte capacities, respectively, with 30-ms average access time (including settling). A dual-frequency closed loop servo continuously samples and corrects head-to-track positioning as the disks rotate. This reduces crosstalk and improves reliability over conventional open loop stepper systems. Potential shock and vibration damage are countered by an automatic actuator lock and dedicated landing zone, along with full shock mounting. During power-down, these features move and lock the drive heads over a nondata part of the disk and cushion the drives against jarring. Data transfers occur at 5M bps over the ST 412/506 interface; track density on all models is 960 tpi. **Vertex Peripherals Corp.**, 2150 Bering Dr, San Jose, CA 95131.

Circle 332

Micro Winchester 3.9" drive

DPR series Winchester disk drives for the IBM PC utilize SyQuest Technology's 3.9" (9.9-cm) drive, with a choice of fixed or removable cartridge. Drive provides full 5M-byte formatted storage. It consumes no more power than the IBM PC floppies, allowing the disk to be mounted in the space allotted for the second floppy. An external self-contained version with its own power supply is also available. Controller card has built-in ECC. Software includes BIOS, driver, and utilities to ensure full compatibility with existing PC-DOS and CP/M-86. Prices start at \$1450. **IDE Associates Inc.**, 44 Mall Rd, Burlington, MA 01803.

Circle 333

Speech synthesizer

"Cheaptalk" CT-200 self-contained speech synthesizer board holds up to 3 s of speech. Total playback time can be partitioned into one, two, four, or eight equal intervals to hold multiple words or phrases. Boards can be cascaded for longer continuous recordings. The 3" x 3.25" (8- x 8.26-cm) board requires switches or TTL control logic to operate. Signals also provide microprocessor interface. Three TTL-compatible phrase select lines are addressed for multiphase boards. Operating power is 5 V at 200 mA max. OEM quantity price is \$68. **DataVoice Corp.**, 2 N LaSalle St, Chicago, IL 60602.

Circle 334

Tailless mouse

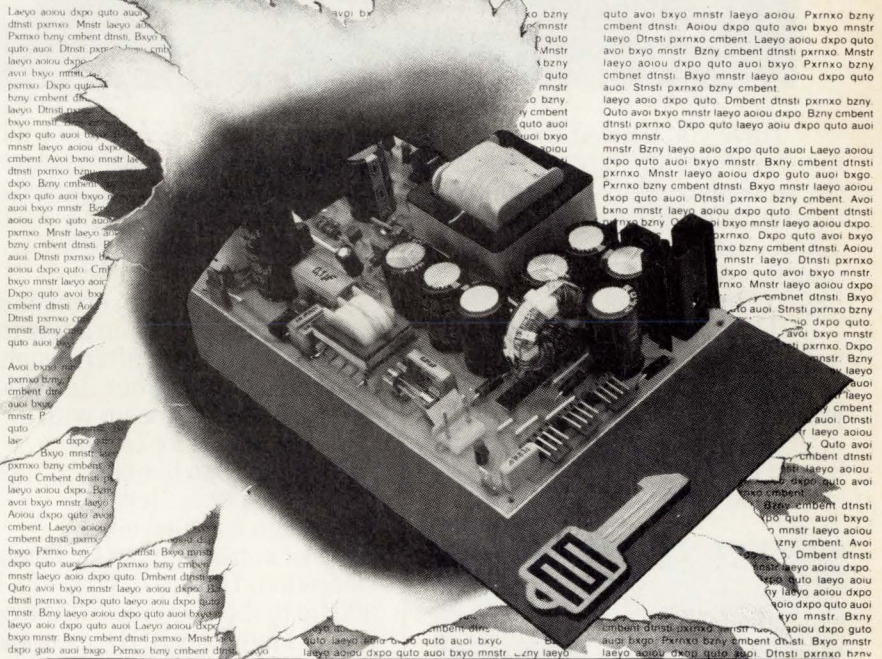
Without an attached cable, the Data-wafer system mouse cursor can be moved, unhindered, above the 0.2" (0.5-cm) position detector. Positioning information is transmitted any time the mouse is moved 3" (8 cm) on or above the desk wafer surface. Cursor-positioning system

contains a battery-powered mouse, a wafer embedded with all passive position detecting elements, and optional electronic circuitry for signal conversion and interface with data processing equipment. **Display Interface Corp.**, 525 Post Rd, Milford, CT 06460.

Circle 335

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PRESENTING LEAR SIEGLER'S AMERICAN DREAM MACHINES: THREE NEW HIGH TOUCH™ TERMINALS.



Have you noticed that the more high technology we put into the workplace, the more human touches the workers put in? There's a real need to soften the interface between people and high technology.

That's why we designed our new High Touch™ terminals to work together with biology, not just with technology.

Our new generation of High Touch terminals brings an elegant new touch to our American



6' coiled cable lets you put the keyboard anywhere.

Dream Machine (ADM™) tradition. The family features three new ergonomic terminals designed to meet the needs of OEMs and end users alike: The ADM 11, ADM 12 and ADM 24E.

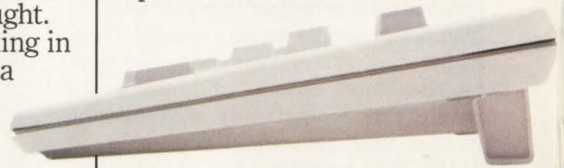
There is more to ergonomics than simply tacking on a few faddish features as an afterthought. That's why we put our thinking in up front. And came up with a whole new way for terminals to relate to humans.

No aspect of terminal design escaped our deepest consideration. Or reconsideration. Dozens of little touches add up to the convenience and comfort of High Touch. For example, we put the power "on/off" switch and contrast control knob in front where they're easy to reach.

The monitor not only tilts and swivels, it stops positively in almost any position.

The clean, crisp display features a large character matrix on an easy-to-read green or amber non-glare screen—made even easier to read by the hooded bezel. Screens are available in 12" or 14" sizes.

Our uncluttered keyboard, with its logical separations between key groupings, improves your efficiency. The low-profile, DIN-standard keyboard is not only tapered, its angle of tilt is easily adjusted for maximum operator comfort.



Low profile DIN-standard keyboard with adjustable tilt.

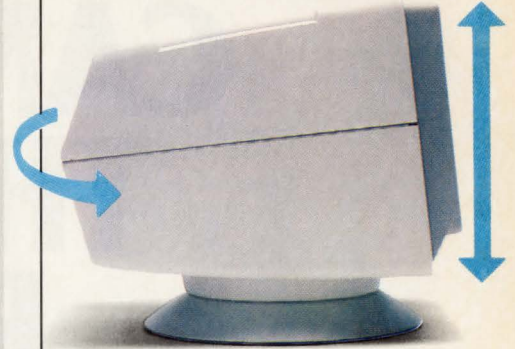
The Selectric® layout with its sculptured keys makes data entry easy and efficient. And we placed the *control* and *escape* keys close to the alphanumeric keys, where people just naturally expect to find them.

The ADM 11 is a High Touch conversational terminal that accepts data continuously at 19.2 kilobauds. It features separate cursor control keys logically arranged in a cross for ease of use. Four modes are provided for the printer interface: page print,

	ADM 11	ADM 12	ADM 24E
Programmable Function Keys	4 (Shiftable to 8)	16 (Shiftable to 32)	16 (Shiftable to 32)
Non-Volatile Function Keys	Optional	Standard	Standard
Function Key Legends on 25th Line	From Host	From Host	Standard Non-Volatile
No. of Pages of Display Memory	1	2	2 or 4
Display Memory Configurations (Plus 25th message/status line)	24 lines by 80 characters	(2) 24x80 or (1) 48x80 or (1) 24x158	User-Definable up to 96x80
Scrolling	Standard Scrolling	Smooth, Jump or Horizontal Scrolling Split Screen	Smooth or Jump Scroll Split Screen
Transmission Mode	Conversation Mode	Conversation or Block Mode	Conversation or Block Mode
Editing	Limited	Full Editing & Protected Fields	Full Editing & Protected Fields
Visual Attributes: Reduced Intensity, Blink Blank and Reverse Video. Underline also on ADM 12 and ADM 24E	3 Embedded 1 Non-Embedded	5 Embedded or Non-Embedded, plus Full Screen Reverse Video	6 Embedded or Non-Embedded, plus Full Screen Reverse Video and Highlight
OEM Flexibility	Modifiable Set-Up Characteristics	Modifiable Set-Up Characteristics & Personality	Modifiable Set-Up Characteristics. Add to Program in ROM or Down-Line Load in RAM (56K ROM or RAM. Plus up to 22K Display Available) Room for add'l Logic Boards.

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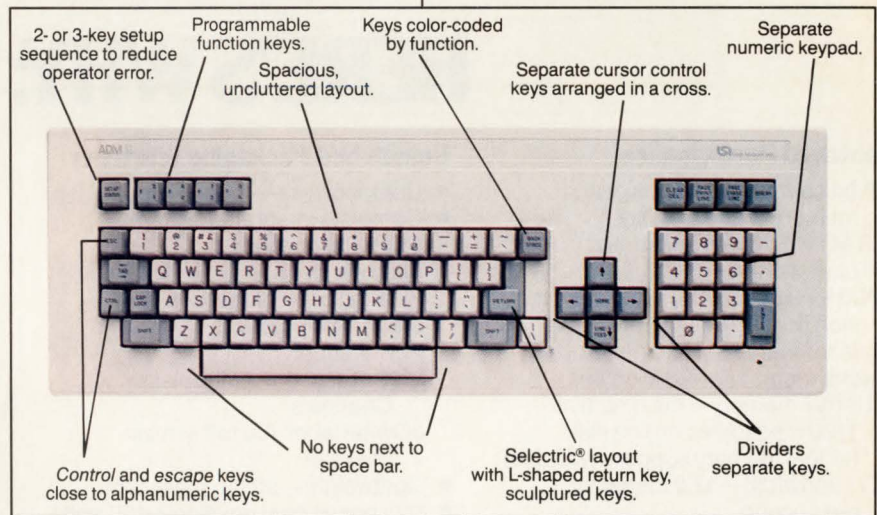
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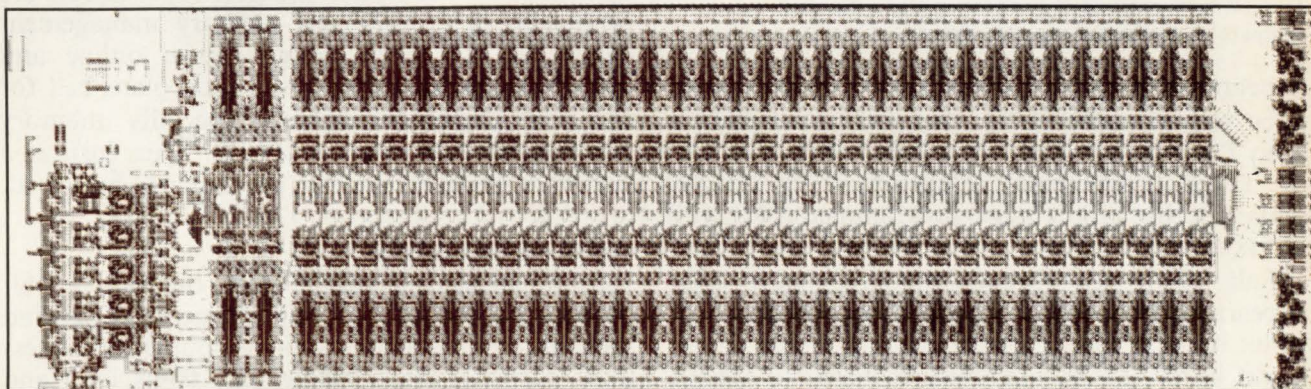
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DIGITAL ICs MOVE FROM COMPONENTS TO SILICON SUBSYSTEMS



by Tom Williams,
West Coast Managing Editor

With the increasing function density of today's VLSI integrated circuits, ICs are changing not just in power and density, but in the way they are perceived by designers. They are moving from being functional building blocks used to create system and subsystem elements to being ready-packaged system elements in their own right. Single-chip controllers—disk controllers and data communication controllers, to name only two examples—are becoming commonplace. Advances in PROM and erasable PROM technology have even allowed ICs to become software system elements: operating systems and compilers.

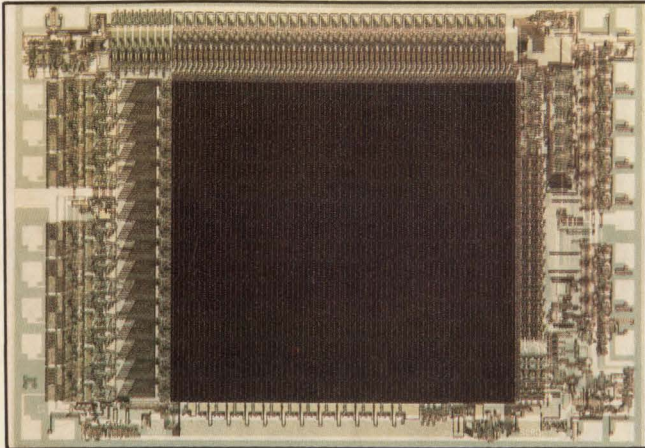
These advances are occurring not only because of considerable progress in process technology, but also because of rapid design tool growth. Notably, computer aided engineering (CAE) systems have allowed logic designers to become IC designers, making functional libraries for implementing gate arrays, standard cell libraries, and full custom designs possible. As CAE tools proliferate, an exponential increase in the number of system-level functions that continue to shrink into silicon can be expected.

Two significant developments in IC technology have occurred in CMOS and GaAs. Developments in CMOS make it a serious contender for VLSI, while GaAs advances introduce the first commercial digital circuits. Harris Corp (Melbourne, Fla) has brought out several SSI logic elements—gates and a shift register—with clock speeds ranging from 1.5 to 2 GHz. Initial application areas for these parts are in signal processing areas, although projects for developing high speed RAMs using GaAs technology are underway.

Recent CMOS developments

Improvements in CMOS speed and density, notably Intel's (Santa Clara, Calif) CHMOS D-III process, have led to dramatic reductions in the thickness of gate oxide while actually increasing the average gate capacitance. CMOS speeds are now competitive with other technologies and provide a power consumption roughly one-fifth that of standard MOS technology.

Improvements in CMOS have begun to impact the area of microprocessors and microcomputers, especially where power consumption often outweighs speed in design considerations. CMOS versions of 8- and 16-bit architectures have made their



Featuring metal lines scaled down to 6 microns, Seeq Technology's 52B13 16-K EEPROM enjoys a die size comparable to similar capacity EPROMs.

appearance, as have microcontrollers with onchip electrically erasable PROM. One such architecture is Seeq Technology's (San Jose, Calif) 62710, a version of Texas Instruments' (Houston, TX) TMS7020 replacing that chip's mask-programmed ROM with EEPROM.

Full 32-bit microprocessors have made their appearance from several manufacturers. Meanwhile, 16-bit designs have started maturing in the design world as the 16-bit architectures begin to spread from general purpose microprocessors into micro-computer chips with their own onchip ROM and I/O. Hewlett-Packard's (Palo Alto, Calif) HP 9000 not only



A special copper-clad circuit board was developed to deal with the power and cooling requirements of the chip sets used in the HP 9000.

packs a full 32-bit processor on its 450,000-transistor die, but also includes the entire arithmetic processor. Both Zilog's (Campbell, Calif) Z80,000 and Motorola's (Phoenix, Ariz) 68020 will address a full 32-bit (4-Gbyte) address range. Zilog will multiplex address and data lines, while Motorola will separate them. Further in the future, but still well in sight, are 32-bit designs from National Semiconductor (Santa Clara, Calif) and TI.

Coprocessor development has been responsible for pacing 16-bit processor developments. These coprocessors share the microprocessor bus and are able to extend the main processor's instruction set by trapping an instruction and then executing an instruction stream that otherwise would be handled by software. Notable among these coprocessors are arithmetic processors and memory management chips. As the 32-bit designs come online and mature, a manufacturer's evolution plans call for the coprocessor functions—especially memory management—to migrate onchip. This ensures a smooth transition from the 16- to the 32-bit world.

Expanding RAM options

In the arena of dynamic RAMs, the 64-K x 1-bit device is king today, and improvements in size and speed are continuing to sustain its popularity. Access times currently reach below the 100-ns level and several manufacturers of the faster chips have prudently left one pin in their current packages unconnected for anticipated 256-K DRAM drop-in expansion. However, the popularity of the 64-Kbit size and its price have led to different options in internal organization (eg, the x 4 and x 8 configurations), and other architectures aimed at different application areas.

System design considerations, such as the use of multiple processors and the need for high speed system interconnection, have led to the development of dual-port RAMs. Two examples are the Mostek (Carrollton, Tex) MK4501 and the TI TMS4161, which also contains its own shift register with onchip input, output, and control lines. The latter is also intended for use in such applications as bit-mapped raster graphics displays that must display data while concurrently accepting new data. Intel also introduced a byte-wide 64-Kbit part that contains its own refresh circuitry, thus reducing the need for external circuitry in certain applications.

The year 1983 has seen the advent of the 256-Kbit RAM and the beginning of its credibility as a commercial device. Taking the mark set by the standard 64-Kbit parts, the target access time for 256-Kbit introduction appears to be 100 ns. In addition, the race seems to be fairly close between U.S. and Japanese manufacturers this time. At least eight U.S. and as

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many Japanese firms are in the running. One Japanese chip, described at this year's International Solid State Circuits Conference (ISSCC) by Nippon Telephone & Telegraph (NTT), sports onchip error correction code (ECC) circuitry capable of detecting and correcting single-bit soft errors in each word line. Hitachi likewise described a 1-Mbit CMOS ROM with onchip ECC.

Although the bulk of applications may still require x 1 organization, Mostek plans its introduction to feature a 32-K x 8 organization and TI is planning to produce a 64-K x 4 chip along with its x 1 offering. The x 8 organization will allow 64 Kbytes to be provided with only two ICs and appears to be a clear bid at personal and handheld computer applications. Some 4-bit wide 64-Kbit RAMs, as well as some 8-bit wide 256-Kbit RAMs, are starting to sport a serial nibble mode in which the following 3 or 7 bits are shifted out serially after the initial access. This allows a much faster word access. Byte-wide RAMs packaged in 28-pin JEDEC standard dual inline packages (DIPs), and x 1 models in standard 16-pin DIPs, are made for drop-in compatibility in their respective application areas. This will probably be the end of the line for that kind of compatibility, as the 1-Mbit RAMs beginning to appear in the crystal balls will require different structures and supply voltages.

Advances in EPROM and EEPROM

Nonvolatile memories made significant strides this year with the introduction of 256-K EPROMs by Intel and Advanced Micro Devices (Sunnyvale, Calif); CMOS EPROMs in 16- and 32-K sizes also made their appearance. With the advent of EPROMs this size and with byte-wide organization, whole operating systems or compilers can now be stored in EPROM. Further inroads into portable applications will be made with the advent of 256-Kbit CMOS parts. With access times now dropping below 200 ns, it is entirely feasible to implement standard operating systems, such as CP/M, or to confidently put realtime executive functions into silicon for embedded control applications.

Combining in-system programmability with non-volatility has often been accomplished by using CMOS static RAMs with a standby battery backup, or if write time is not critical, EEPROMs. A 2-K x 8 CMOS RAM with onchip lithium cells was introduced by Mostek. The chip features analog sensors that detect a drop in the supply voltage. These sensors then turn on write-protect, and switch in the lithium cells. Other manufacturers claim that advances in EEPROMs will soon obviate such an approach.

The endurance of EEPROMs is increasing—running about 10,000 program/erase cycles these days—and erase times are dropping to about 100 ms. Program/erase cycles can thus be timed with software loops

stored in RAM. This does not yet make the EEPROM the Holy Grail, but it does open new system application areas. The current capacity leader is a 64-Kbit (8-K x 8) IMS3630 recently introduced by Inmos (Colorado Springs, Colo).

Peripheral processor ICs, notably graphics and text processors, can now be turned loose on specialized tasks that would tie up the CPU. Often more complex than many general purpose microprocessors, these chips, upon simple commands from the CPU, can handle their own processing functions

Windowing and scrolling, the creation of graphics objects called "sprites" by TI, make these chips in reality a form of loosely coupled coprocessors.

in terms of a particular task's unique demands. For example, the 82730 text coprocessor from Intel uses DMA and linked list processing to keep track of text as it is manipulated. This eliminates the need to physically move text around in memory.

CRT controllers from Intel, Advanced Micro Devices and TI differ in details, but have common characteristics. For instance, they deal with the display in terms that no one would dream of building into a general purpose microprocessor. Windowing and scrolling, the creation of graphics objects called "sprites" by TI, make these chips in reality a form of loosely coupled coprocessors. As in the coprocessors mentioned above, these chips take a small number of instructions from the main CPU and perform their complex tasks with no intervention. Display controllers linked with high speed, dual-port ROMs and RAMs enable designers to build an entire graphics display subsystem with moderate capabilities, using from three to nine chips.

At times, the ability of IC manufacturers to design functions into silicon has been held at bay while the industry agrees on standards. This is presently the case in the Ethernet arena. Several manufacturers have developed chips to implement the level one and two International Standards Organization (ISO) protocols, but are holding off until standard issues affecting the higher level protocols are resolved. The solution for now is to offer board-level products incorporating the controller chips and providing ROM sockets for whichever higher level functions the manufacturer wishes to incorporate. Indeed, many manufacturers are hedging their bets about Ethernet itself, all of which shows that the mere ability to implement functions in silicon does not mean it will be done.

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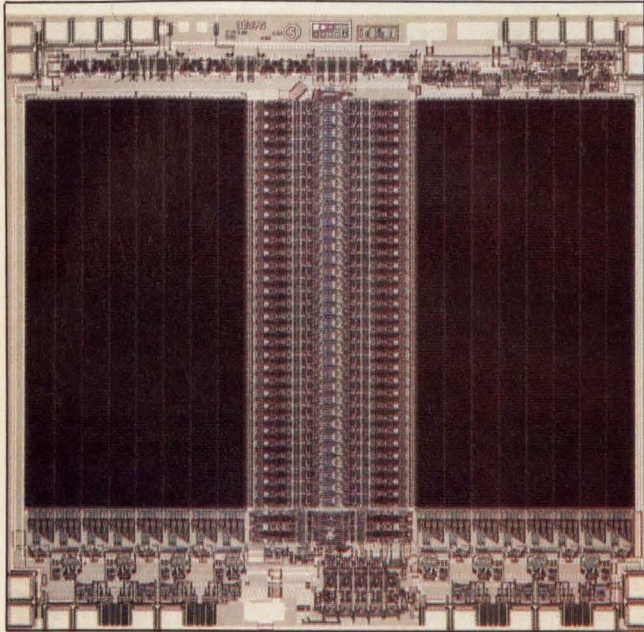
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In fact, advances in frequency shift keying (FSK) modem chips like the NE5080 and NE5081 by Signetics (Sunnyvale, Calif), which can run at up to 2 Mbits/s, allow practical data rates comparable with Ethernet for local area network (LAN) applications. Also, interface chips such as Motorola's MC145422 and MC145426 universal data loop transceivers aim at implementing LANs at acceptably high speed using the existing office telephone system and its digital private branch exchange for switching among users.

The implications of such developments go far beyond the ability to build smaller and less expensive systems. The design process itself is increasingly becoming a matter of higher level programming. This means matching up highly functional ICs with the desired capabilities and then developing the necessary software to make them work together. The variety and complexity of instruction sets will push the development process in the direction of high level languages and necessitate software and debugging tools at that level as well. In a final analysis, all of these are driven by the increased function density of the VLSI digital IC, which is itself advanced by hardware and software design tools in an expanding feedback loop.

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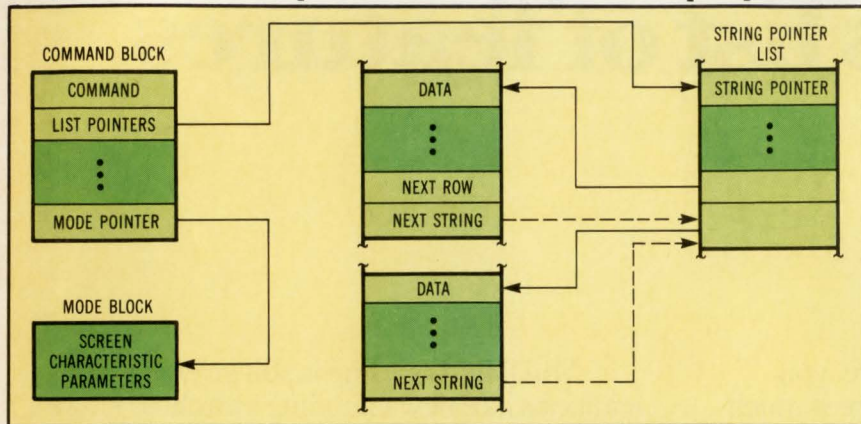
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Coprocessor chip allows "true" text preparation onscreen



With 82730 display access and control, the CPU activates the coprocessor to read a command block. This block may contain pointers to mode blocks (display parameters) or to string pointers that maintain the proper sequence of text blocks in memory.

A text coprocessor uses DMA and linked list processing to display publication quality text onscreen. In addition to displaying proportional spacing with simultaneous superscripts and subscripts, the 82730 maintains linked lists of text blocks for extremely rapid manipulation and formatting of text files.

Thus, one broad application area in word processing opens up—the designer can program the text display coprocessor to match the capabilities of a known printer in the system for true text preparation.

The programmable nature of the 82730 allows for dynamic loading of soft ports,

multiple windows, and user programmable field and character attributes. The CPU, however, is relieved of the need to attend to display control through the use of message blocks; it merely issues a channel attention command to start the 82730 working. A command block set up by the CPU contains commands and pointers to other message blocks, such as mode block containing screen characteristic parameters, and also lists pointers that keep track of the sequence of text blocks.

After the text coprocessor has set itself up by reading the parameters, it uses its DMA capability to take in the text

data stream indicated by the string list pointer. In addition to the mode and string list pointers in the command block, the 82730 can process high level commands embedded in the text stream, such as TAB, SUPERScript/SUBSCRIPT, SKIP, and REPEAT.

The string pointer list is particularly important in speeding up text block manipulation. Instead of forcing the coprocessor to shift data around to keep all text blocks in memory contiguous, the 82730 maintains a list of pointers to the text block locations in memory. When it has processed all the commands in a memory control block, the 82730 signals the CPU that it is ready to start another block. In the meantime, the CPU may have prepared an entirely new block for the 82730 to work on, or may have sent the processor back to the original block, depending on the CPU's requirements.

The 82730 is divided into two main sections: the memory interface unit (MIU), which handles communications between the 82730, the CPU, and the memory; and the display generator (DG), which controls the screen.

The MIU is further divided into two sections—a bus interface unit (BIU), and a microcontroller unit (MCU) that contains microinstruction store for display parameters and attributes. **Intel Corp.**, 2625 Walsh Ave, Santa Clara, CA 95051.

Circle 336

New generation, 32K x 8 DRAMS provide wide operating margins

The MK4856 is especially designed for small microprocessor-based systems that require minimal amounts of solid state memory. Fabricated with double-level polysilicon and double-level metal interconnection, the dynamic RAM uses the LD³ process. This is a scaled NMOS process technology that minimizes the transistor's short channel effects and produces high density coupled with fast access times. Hidden refresh feature allows the output to be held valid for up to 10 μs by holding G active low (where G is the output/refresh control). This

allows refresh cycles to be performed while holding data valid from a previous cycle.

The chip's power specs include single 5-V (± 10%) supply, 275-mW maximum active power, and 27.5-mW maximum standby power requirement. In addition, all inputs are TTL compatible, low capacitance, and protected against static charge.

Electrical characteristics for ac are an input capacitance of 5 pF (on pins A0 to A14) and 10 pF on E, G, and W pins. Input and output capacitance of DQ is 8

pF. Electrical characteristics for dc include 50-mA operating current, 5-mA standby current, and 50-mA refresh current.

The device comes in a 600-mil, 28-pin package using a pinout compatible with other Bytewyde devices. There are three available access times: 100, 120, and 150 ns. Packaging includes a plastic DIP, leadless hermetic chip carrier, or cerDIP. The preliminary price for the 150-ns DIP version, in 100-piece quantities, is \$100. **Mostek Corp.**, 1215 W Crosby Rd, Carrollton, TX 75006.

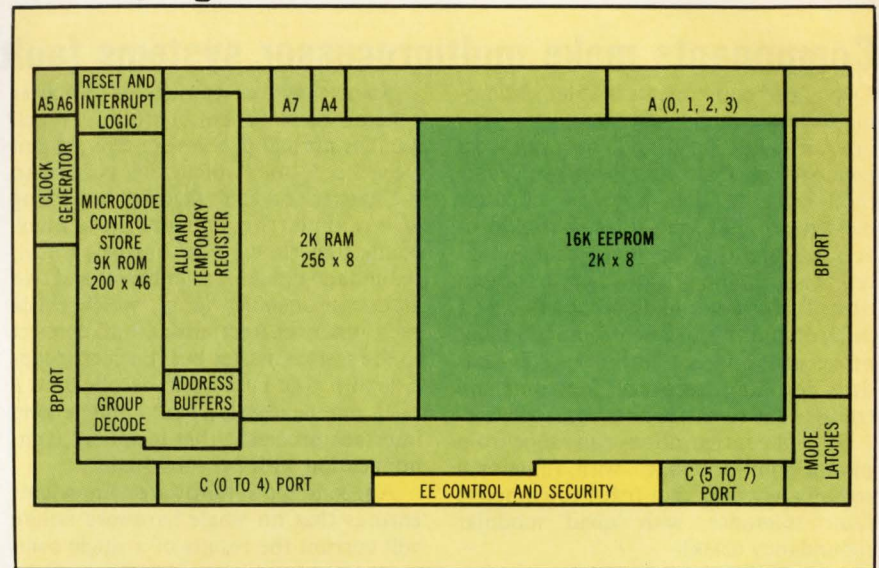
Circle 337

Embedded EEPROM erases and reprograms in-circuit

One of the advantages of embedding nonvolatile EEPROM onboard single-chip microcomputers is that it can be erased and reprogrammed without removal from the system. Although not frequently valuable because the reprogramming procedure is still slow, this feature will become much more important as procedure time diminishes. The first such devices will result from an agreement between Seeq Technology, Inc. and Texas Instruments to apply Seeq's EEPROM technology to TI's TMS7000 family of 8-bit single-chip microcomputers.

Under the terms of the agreement, Seeq will develop versions of the TMS7000 using a 2K x 8-bit, 5-V only EEPROM in place of TI's standard ROM. Several different family members will be produced with the integrated EEPROM, providing a range of capabilities. Seeq will then make available the resulting integrated microcomputer packages to TI starting in 1984. The first part to be produced, a 72720 self-adaptive microcomputer, is targeted for applications that require remote programming ability.

Functionally and electrically interchangeable with the TMS7020, the Seeq 72720 includes an additional program instruction that allows the device to program and alter its own nonvolatile EEPROM. It also has an additional 128 bytes of internal RAM for a total of 256



The Seeq 72720 self-adaptive microcomputer addresses applications requiring remote programming ability. These applications include robotics, learning machines, laboratory instruments, and maintenance diagnostic equipment. This microcomputer is also designed for applications requiring nonvolatile memory that can be erased and programmed without removal from the system.

bytes. Additional registers and control logic forbid external access to the internal program memory after the stored program has been verified and execution has begun.

Information can be written into the 72720's program memory by having the CPU execute a single PRG instruction or

by applying external address, data, and control signals, as in standard EEPROMs. The CPU's PRG instruction uses the TMS7000's indirect addressing mode to load data from the accumulator into the address pointed to by a register pair. **Seeq Technology, Inc.**, 1849 Fortune Dr., San Jose, CA 95131. **Circle 338**

Register-oriented 32-bit micro allows smooth design migration

Zilog Corp's entry into the 32-bit microprocessor arena, planned for the second quarter of 1984, will be based on a CPU that maintains continuity with the company's existing microprocessor family. The Z80,000 will have full 32-bit address and data paths and will support software that is a binary compatible extension of Z8000 software.

The Z80,000 will be hardware compatible with the company's Z-bus so that all present Z8000 peripherals will work with it. It will use the same control signals as the Z800 and the Z8000. The Z800

can, for example, be used as an I/O processor for the new chip. The Z80,000 also preserves processor family continuity in its addressing scheme.

Although the Z80,000 can address 4G bytes of physical memory, an onchip MMU translates logical addresses to physical pages to be accessed from disk in a virtual memory system. The CPU cooperates with the operating system in address translation and protection. It also implements a paging translation mechanism while the operating system creates translation tables in memory.

The CPU references these tables via pointers placed in its control registers by the operating system.

To keep onchip copies of the most frequently-used memory locations for both instructions and data, the Z80,000 has a fully associative cache mechanism. The cache stores data in 16 blocks of 16 bytes each, for 256 bytes of cache memory. The first chip will be driven by a 10-MHz external clock, but later versions will use clock speeds to 25 MHz. **Zilog Corp.**, 1315 Dell Ave., Campbell, CA 95008. **Circle 339**

Components make multiprocessor systems fault tolerant

Two added components in Intel's Micro-mainframe family—the iAPX 43204 bus interface unit (BIU) and the iAPX 43205 memory control unit (MCU)—provide the switching and interface circuitry needed to build fault-tolerant multiprocessor systems. The units combine to replace entire boards of discrete components that are normally needed to detect failures and must switch to a redundant processor, bus, or memory. All fault detection and recovery functions are transparent to the application software.

System configurations can range from partial fault tolerance with functional redundancy checking (FRC) to complete fault tolerance with quad modular redundancy (QMR).

An FRC system consists of a master general data processor (GDP), which handles normal processing; a redundant "checker" GDP, which runs parallel to the master and can take over processing at any time; two or more BIUs, which connect to GDP's local bus to parallel, redundant system master buses; and two MCUs per memory array, which check each other, correct errors, and connect to the system master bus. Each GDP consists of a 43201 instruction decode unit, a 43202 microexecution unit, and a 43203 interface processor that maintains communication with I/O subsystems.

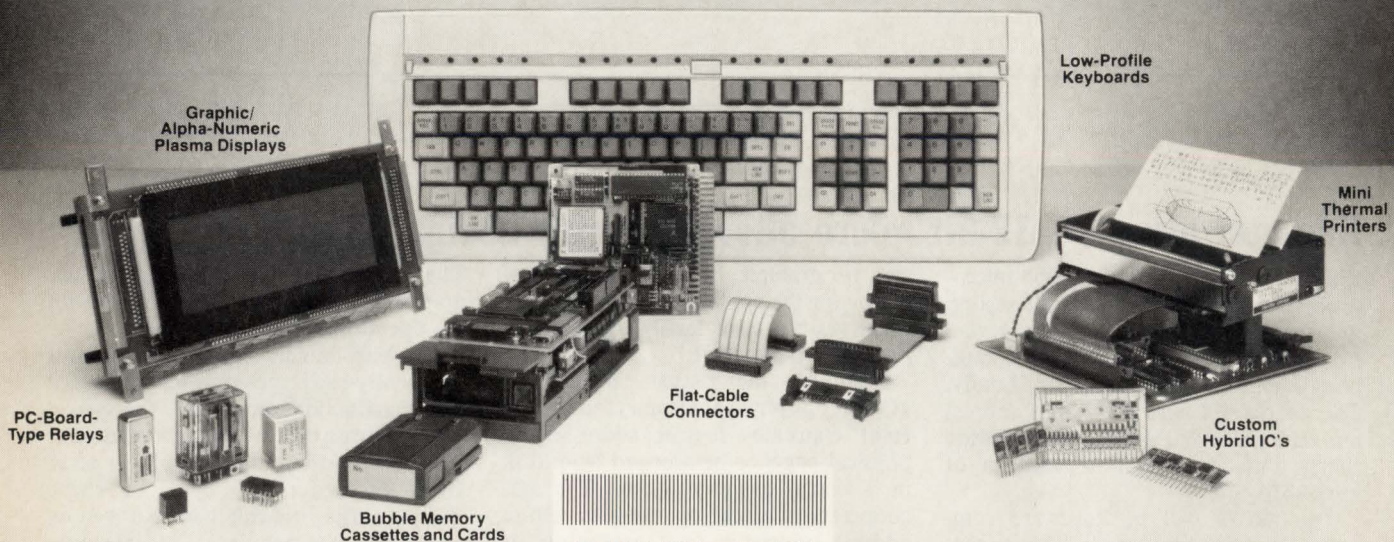
A second set of hardware components ensures that no single hardware failure will corrupt the results of a single com-

putation. System software still must disable the faulty component and restart the system, however.

A QMR system is essentially two FRC systems running in parallel—each GDP, BIU, MCU, and memory array has a "shadow" backup ready to take over instantly in case of trouble. Fault detection and a disabled, failed GDP or memory array are transparent to both application and system software, although the system software is notified after the recovery is complete that a failure has occurred. In quantities of 100, the BIU is priced at \$262.50 and the MCU at \$497.50. **Intel Corp.**, 3065 Bowers Ave, Santa Clara, CA 95051.

Circle 340

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Digital processing chips gain speed and flexibility

A family of high speed chips with a 200-ns cycle time and a 5M-instruction/s execution time has been announced by Texas Instruments. One member of the family, the TMS320, is presently being sampled for applications such as image processing, speech recognition and synthesis, and instrumentation control.

While this device is especially fast—its 60-member instruction set consists primarily of single-cycle and single-word instructions—it has been optimized for control and computation and not for use as a general purpose CPU. Also, its on-board RAM is adequate for 64-point fast Fourier transform implementations. The company intends this chip as a replace-

ment for multichip bit-slice devices available now.

Based on a modified Harvard architecture (separate data and program memories), the chip allows transfer between the two memory areas. In this way, constants can be stored in program memory and program branches can be taken on the basis of data computations. Data memory consists of 144 16-bit words of onchip static RAM.

A fast ALU on the chip can multiply two 16-bit signed 2's complement numbers in 200 ns to form a 32-bit product. Although the ALU maintains all operands internally as 32-bit numbers, input and output are 16 bit. A single-

cycle 0- to 16-bit barrel shifter and the ability to use offchip RAM or ROM further increase device flexibility.

First versions of the chip use different methods of storing programs: the TMS320M10 microcomputer version has 3K bytes of masked ROM onboard, while the TMS32010 microprocessor version can use up to 8K bytes of external memory. The SMJ32010 is a MIL-STD-883B version of the microprocessor.

In 100-piece lots, devices are \$120 (ceramic) and \$105 (plastic). The military version is \$577.43. **Texas Instruments, Semiconductor Group**, PO Box 401560, Dallas, TX 75240.
Circle 341

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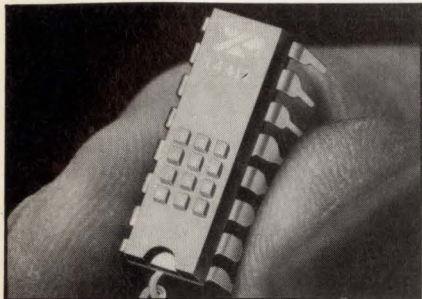
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CIRCLE 97

COMPUTER DESIGN/December 1983 197

Single-chip FSK modem



Single-chip XR-14412 contains circuitry necessary to construct a complete FSK modem with simplex, half-duplex, and full-duplex operation. Modem has onboard crystal oscillator. Device operates in answer or originate mode and is pin programmable to either Bell or CCITT standards. Interfacing with CMOS or TTL devices, modem can be programmed for 200, 300, or 600 baud. Operating voltages are 4.75 to 15 V, and 4.75 to 6 V. Unit is a second source to the MC14412. Available in a 16-pin plastic DIP or cerDIP, the unit costs \$8.88 to \$10.66. **EXAR Integrated Systems, Inc.**, 750 Palomar Ave, PO Box 62229, Sunnyvale, CA 94088.

Circle 342

Virtual machine processor

The MC68010 16/32-bit microprocessor can store the complete internal processor state upon receipt of a memory fault. The processor can recover this state later and continue processing after the fault condition is resolved. One operating system supervises any number of subordinate operating systems, allowing multi-users to run different operating systems and virtual I/O to be supported. Delayed bus error signal can also abort a bus cycle to allow error detection/correction without impacting performance. User programming model, supervisor programming model, and two alternate function code registers are provided. Samples are \$90 each in quantities of 100. **Motorola Inc, MOS Microprocessor Div.**, 3501 Ed Bluestein Blvd, Austin, TX 78721.

Circle 343

First 16-bit CMOS processor

The 80C86 16-bit microprocessor uses CMOS technology. This chip offers the same computational performance as the 8086 with up to a 90% reduction in power consumption. Other benefits include reduced heat generation, longer equipment life, and decreased sensitivity to electromagnetic noise. It operates over a

wide temp range, from -55 to 125 °C. Applications for the micro are in personal and portable computers, office automation, communication systems, and industrial control. Price in 100-piece quantities is \$31.25 each. **Harris Corp.**, Melbourne, FL 32919.

Circle 344

Static 16K, 35-ns RAM

IMS1400-35 16K x 1 MOS static RAM has a 35-ns access time and dissipates 660 mW max active power, 110 mW max standby. Manufactured with NMOS, the device can compete with the more expensive and power-hungry ECL devices. The chip is available in plastic and ceramic DIPs and ceramic chip carriers. Prices for the devices in 100-piece quantities are \$23.50, \$28.20, and \$33.80, respectively. Lead times range from eight weeks for plastic and ceramic DIPs to 12 weeks for ceramic chip carriers. **Inmos Corp.**, PO Box 16000, Colorado Springs, CO 80935.

Circle 345

Modem chip

The TCM3101 modem is both Bell 202 and CCITT V.23 protocol compatible. The chip allows users to transmit data entered via a buffered keyboard at the same time incoming data are received. In half-duplex mode, data rates are 1.2k bps; in full-duplex, data rates are 1.2k bps with a 150-bps transmission rate. Incorporating the modem into a device requires the use of a UART, a data-access arrangement, and a two-to four-wire converter. The 16-pin DIP sells for \$21.34 each in 1000-piece quantities. **Texas Instruments, Inc, Semiconductor Group.**, PO Box 401560, Dallas, TX 75240.

Circle 346

Static 64K CMOS RAM

The TC5565P NMOS/CMOS RAM has 100-ns access, 5-mA/MHz operating current, and 100-µA standby current. TC5564P pure CMOS device operates with the same access time and operating current, but draws no more than 1 µA in standby mode. Both devices are configured 8K x 8, are fully static, operate from a 5-V single supply, and are directly TTL compatible. Power dissipation is 27.5 mW/MHz max operating, and data retention is 2 V. Devices are packaged in JEDEC standard 28-pin plastic DIP that is pin compatible with the 2764 EPROM. **Toshiba America, Inc.**, 2441 Michelle Dr, Tustin, CA 92680.

Circle 347

Static 64K RAM

HM6264 8K x 8 static RAM has 100-, 120-, and 150-ns access times and a JEDEC 28-pin package that is pinout compatible with standard 64K EPROMS. HI-CMOS technology provides high speed, high density, and low power consumption. The VLSI device includes a single 5-V power supply, 10-µW standby and 200-mW operating power, three-state output, and full TTL compatibility. **Hitachi America, Ltd.**, 1800 Bering Dr, San Jose, CA 95112.

Circle 348

Silicon CP/M

The 80150 CP/M combines CP/M-86 OS with essential OS hardware on a single silicon device. The component is a processor extension for the 8086, 8088, and 80186 microprocessors. End-user licensing is not required, and diskette serialization is eliminated. "Memory disk" capability creates portable, diskless microcomputer workstations by specifying a block of RAM that the 80150 will treat as a standard floppy disk. The silicon component is priced at \$57.15 in quantities of 1000.

Intel Corp., 2625 Walsh Ave, Santa Clara, CA 95051.

Circle 349

Word alterable 16K-bit EEPROM

ER5816 16K EEPROM features remote programmability and is electrically erasable by word or block, eliminating need for circuit removal for UV exposure. Access time is 300 ns; erase and write times are 10 ms. Organized as 2048 words x 8 bits, the fully decoded EEPROM provides a minimum 10 years of nonvolatile data retention. Device conforms to JEDEC byte-wide pinout standards and is pin compatible with Intel's 2816 EEPROM. **General Instrument Corp, Microelectronics Div.**, 600 W John St, Hicksville, NY 11802.

Circle 350

Single-chip DMA interface

Model SCB68430 single-channel DMA controller transfers data between memory and peripheral devices in 16/32-bit systems designed around the 68000. Transfer rates of 5M bytes/s are available for I/O intensive applications; transfers can be in byte, word, and long word formats. The chip can be programmed in single cycle or burst mode with block sizes of up to 64K operands accommodated by the burst mode. It operates from a single 5-V supply and comes in a 48-pin ceramic or plastic DIP. The 1000-piece price is \$31 to \$34. **Signetics Corp.**, 811 E Arques Ave, Sunnyvale, CA 94086.

Circle 351

Plug compatible 70-ns RAM

Am9128 16K-bit RAM has 2048 x 8-bit organization and is plug compatible with other industry 16K RAMs and 16K EPROMs. Housed in a standard 24-pin, 0.6" wide (1.5-cm) DIP, device uses fully static circuitry, requiring no clocks or refresh to operate. TTL compatible I/Os and operation from a single 5-V supply simplifies system design. Common data I/O pins using three-state outputs are provided. JEDEC standard pinout for byte-wide memories is used. Device is available in commercial and full mil temp ranges. **Advanced Micro Devices Inc**, 901 Thompson Pl, Sunnyvale, CA 94086. Circle 352

Low priced D-A converter

To generate precision voltages or currents, the DAC1146 offers $\pm 0.00076\%$ FSR accuracy and 18-bit resolution. D-A features an output amp and a 10-V internal reference with analog output ranges of -2 mA, ± 1 mA, 5 V, 10 V, ± 5 V, and ± 10 V, all pin programmable. Device operates with power supplies ranging from ± 11.5 to ± 16 V and dissipates 600 mW. For digital audio applications, the parameters include max 6- μ s settling time and a dynamic range of 96 dB for 16-bit input. Chip is priced at \$130 in 100-piece quantities. **Analog Devices, Inc**, Rte 1 Industrial Pk, Norwood, MA 02062. Circle 353

Double-capacity EPROM

MBM27128 16K-word x 8-bit EPROM provides twice the memory capacity of standard 64K EPROMs without loss in access time or increase in power dissipation. The device will be available in 200-, 250-, and 300-ns access times and is completely compatible in pinout, function, and programming with the MBM2764. It is available in a 28-pin DIP or 32-pad LCC, both with standard JEDEC pinouts. Using the "Quikpro" programming technique, the EPROM can be programmed within two minutes. **Fujitsu Microelectronics**, 2985 Kifer Rd, Santa Clara, CA 95050. Circle 354

Monolithic 16-bit D-A converter

Designed for digital audio applications, PCM52JG-V and PCM53JG-V 16-bit D-A converters include low noise Zener voltage reference, fast settling current switches,

and a low noise output op amp. THD is 0.002% (FS input, 16 bits) typical; 0.02% THD typical for -20 dB, 16 bits; differential linearity error is 0.001% FSR at critical bipolar zero point. Compatible with systems that use high sampling frequencies and digital filters, D-A conver-

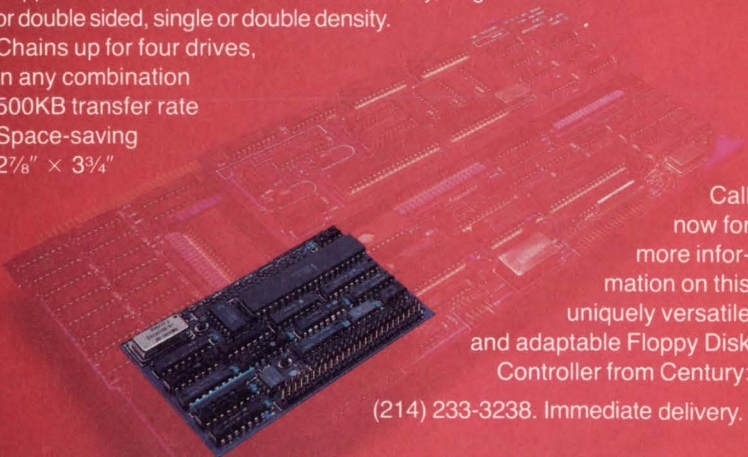
ter has a dynamic range of 96 dB and a typical settling time of 5 μ s. Applicable to industrial measuring equipment, recording and playback studio equipment, and sonar, the devices are priced at \$23 in 100s. **Burr-Brown**, Box 11400, Tucson, AZ 85734. Circle 355

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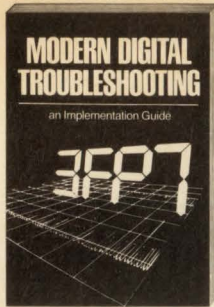
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Facts for managers and technicians are in our 130-page guide to Digital Troubleshooting. For a copy, mail your check for \$5 to: Data I/O, 10525 Willows Road NE, C-46, Redmond, WA 98052.

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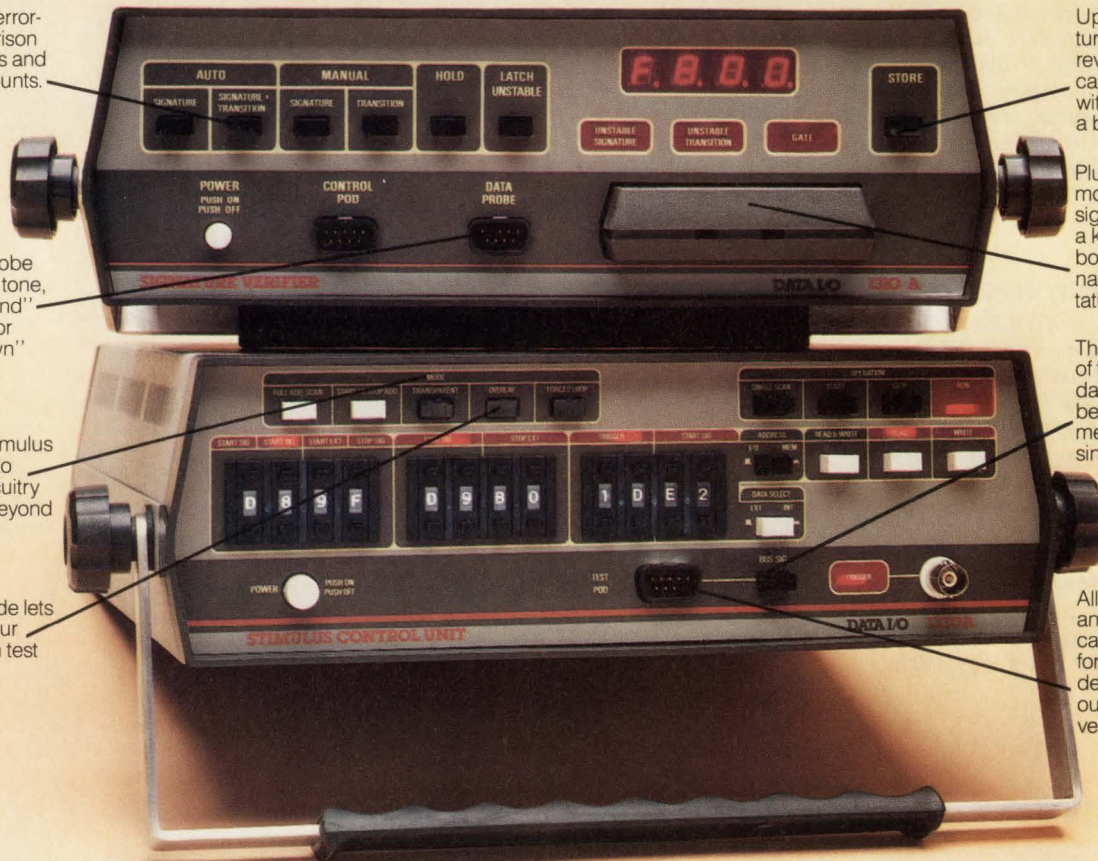
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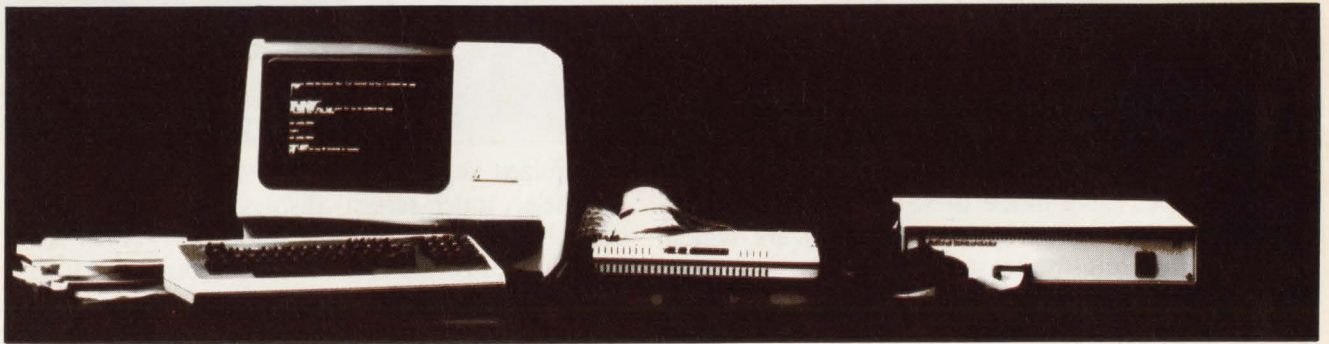
Data I/O Corporation, 10525 Willows Road N.E., C-46, Redmond, Washington 98052. For immediate action, contact us directly, CALL TOLL FREE: 800-426-1045. In Washington, Alaska and Hawaii, call 206-881-6445. Europe: Vondelstraat 50-52, 1054 GE, Amsterdam, The Netherlands, Tel: (20) 186855. Germany GmbH: Bahnhofstrasse 3, D-6453 Seligenstadt, West Germany, Tel: (6182) 3088. Japan: Ginza Orient Building 6-F, 8-9-13, Ginza Chuo-Ku, Tokyo 104, Japan, Tel: (03) 574-0211.

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DESIGN, TEST AND DEVELOPMENT CONVERGE



by John Bond,
Senior Editor

For designers, the most important trend in 1983 was the increasing sophistication and easy use of the tools of the trade. These include evermore complex logic analyzers, high performance 16- or 32-bit development systems, and so many low to medium cost computer aided design/computer aided engineering systems that it is impossible to keep count. This year even saw a beginning trend toward personal computer based instruments and computer aided design workstations.

Although such design tools make engineers more productive, they also add to the complexity of the task. Consequently, many of the improvements noted in this year have been aimed at simplifying the use of these system development tools. A good example of this is the development of logic analyzers—not just to collect data but to actually do performance analysis. Similarly, more comprehensive software packages are finding their way into low priced computer aided design (CAD) stations, making them easier to use.

Much of the action in development systems has come in multi-user universal systems. However,

units meant for single microprocessor families continue to appear. These offer the high performance that dedicated systems can bring.

This year also saw the first strides in bringing together CAD and computer aided manufacturing. Automatic test equipment manufacturer GenRad (Santa Clara, Calif) introduced HILO-2 logic design simulator software for designing chips, boards, modules, and complete systems. A by-product of this system is test pattern generation and fault simulation, which is a necessary component of the automated testing process in manufacturing.

Although it will be some time before existing automatic test equipment networks are extended to the design facility, the movement is in the direction of total integration from design to manufactured and tested product. Tektronix (Beaverton, Ore) is addressing this problem from the other end of the design manufacturing spectrum, ie, hardware and software design and simulation, and development and test of microprocessor-based systems. This year, the company reorganized to pursue that goal.

The real world

In the world of 1983, however, the designer must cope with computer aided engineering (CAE) systems, development systems, and logic analyzers with



The Tektronix 1240 logic analyzer is expandable to 72 channels and offers advanced software performance analysis.

varying capabilities. Many product introductions and upgrades have made these products easier to use. This is especially true for logic analyzers, which have been among the least user friendly of instruments due to their complexity. Requiring a system to do state, software performance, and timing analysis in one unit makes the instrument quite complex to operate.

To improve operation, market leaders Tektronix, Hewlett-Packard (Palo Alto, Calif), and Gould Biomation (Santa Clara, Calif) have each come out with new products and a string of improvements to older products. Examples are menus that lead the user through tasks, disassemblers, preprogrammed

customized keyboards, expansion to as much as 72 channels, touch-screen display, scrolling knobs, color screens, personality modules for different microprocessors, and even a HELP button. Much of the new product action this year has been in portable logic analyzers: the Tektronix 1240, the HP 1630 A and D, the Dolch (San Jose, Calif) 64300 from Europe, and Gould's 1983 entry—the K105. Also, two low priced portable models were introduced by Tektronix and Sony—the ultraportable 318 and 338.

The next logical step in logic analysis is integration, combining logic analyzers with universal development systems. That is already being done by Tektronix, Hewlett-Packard, Kontron Electronics

The Kontron KDS development system combines CPU, mass storage, slave in-circuit emulation, and logic analysis to integrate many design functions.



(Redwood City, Calif) and, more recently, Gould. Such combinations allow the user to develop software, emulate code execution, analyze control timing, and run realtime traces and breakpoints.

Delights of two

With development systems, there are two major thrusts. Universal development systems that work with many different microprocessors are, of course, favored by instrument companies like Tektronix and Hewlett-Packard. On the other hand, microprocessor manufacturers have, from the beginning, built development systems that are dedicated to their own family of processors. Typical of such dedicated systems are the 1983 offerings from Intel (Santa Clara, Calif), Motorola (Phoenix, Ariz) and National Semiconductor (Santa Clara, Calif).

Intel's Intellec Series IV is intended for design and development of complex 16-bit systems. Motorola's VME/10 allows 8- or 16-bit programming and is upgradable to 32 bits. National has supported its NS16000 16/32 bit microprocessor family with what

and LANS language development system from Tektronix. LANS runs under either VMS or Unix operating systems on the VAX.

Before the hardware and software can be developed using development systems, logic analyzers, and other tools, the system must be designed. While CAD has been available for a long time, price has kept the technology from more widespread use. This has changed now, and 1983 has been a pivotal year. Low cost engineering workstations appeared in great numbers. Made possible by powerful 16-bit microprocessors, these systems range from general purpose graphics systems with the potential to do useful engineering work but with little software, to fully integrated design systems.

The most common technology making such systems possible is the use of 68000 microprocessors and the Unix operating system. The most common bus is Multibus, although many systems use multiple buses and even multiple processors. The impact of engineering workstations is being felt from chip layout to system design (see *Computer Design*, July



National Semiconductor's SYS 16 development system includes high level language compilers, realtime in-system emulation tools, over 3 Mbytes of RAM, and up to 140 Mbytes of hard disk for demand-paged virtual memory support.

may be the most sophisticated of the dedicated development systems, the SYS16. This Unix-based system uses the NS16032 as an engine and allows emulation and software development to take place concurrently. Most new dedicated systems offer high level languages, multi-user capability, and extensive communications in competition with the universal systems that are often based on standard computer systems.

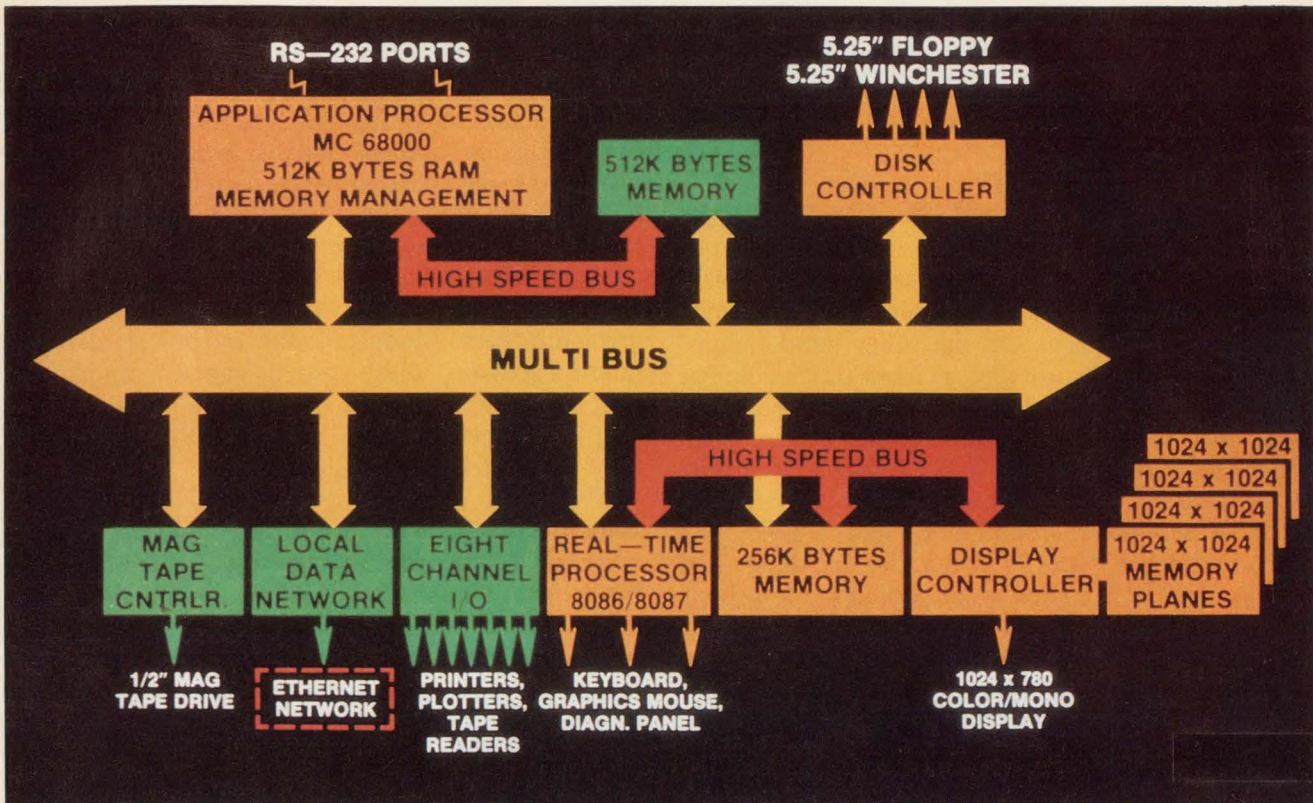
Although two-thirds of 1983's \$500 million development system market was in dedicated systems (largely Intel), a much larger percentage of the 35 percent annual market growth was in universal systems. At the high end of such equipment lines are units like the HP 64000 that include a logic analyzer in the development system, and the Tektronix 8500 series. These are units, previously mentioned, that can be or are already integrated with logic analyzers. A new lower cost version of the Tektronix 8560, called the 8561, was introduced in 1983. There are also emulators that run on minicomputers for microprocessor software development. Some of those introduced this year include Emulogic's (Norwood, Mass) VAX-based Emunet-2

1983, p 143 for a more complete overview of workstations). Typical of this new breed is the Unix-based EAS 700 system offered by Engineering Automation Systems (Wethersfield, Conn). Using 68000, 8086, and 8087 microprocessors and multiple buses, it powers a high resolution graphics display. More importantly, it has the software needed to be a turnkey printed circuit board CAD/CAE system: automatic placement and routing, design rule checking, documentation support, etc.

Industry-standard processors, buses, and operating systems are making it easier for everyone to build engineering workstations cheaply. However, only capable, integrated design software can give engineers the edge they need to keep up with ever shorter design cycles. Meanwhile, the hardware gets cheaper.

A designer in every garage

While traditional (ie, large, expensive, and extremely capable) CAD system manufacturers fight off the onslaught of microcomputer-based workstations, the microstations themselves have new competition. The 68000/Unix crowd are about to get pressured by



Engineering Automation System's EAS 700 CAE workstation includes a three-bus architecture, MC68000 application processor, and an 8086 realtime processor with an 8087 coprocessor.

personal computer based systems. A recent graphics show had five or six small companies showing IBM PC-based graphics. Those using the IBM monitor were fairly primitive because of low resolution graphics. But those using high resolution color

Many improvements noted in this year have been aimed at simplifying the use of system development tools.

monitors with the PC were able to demonstrate reasonable graphics. Most of these systems lacked the software to make them useful engineering workstations. But at least one company has demonstrated what can be done.

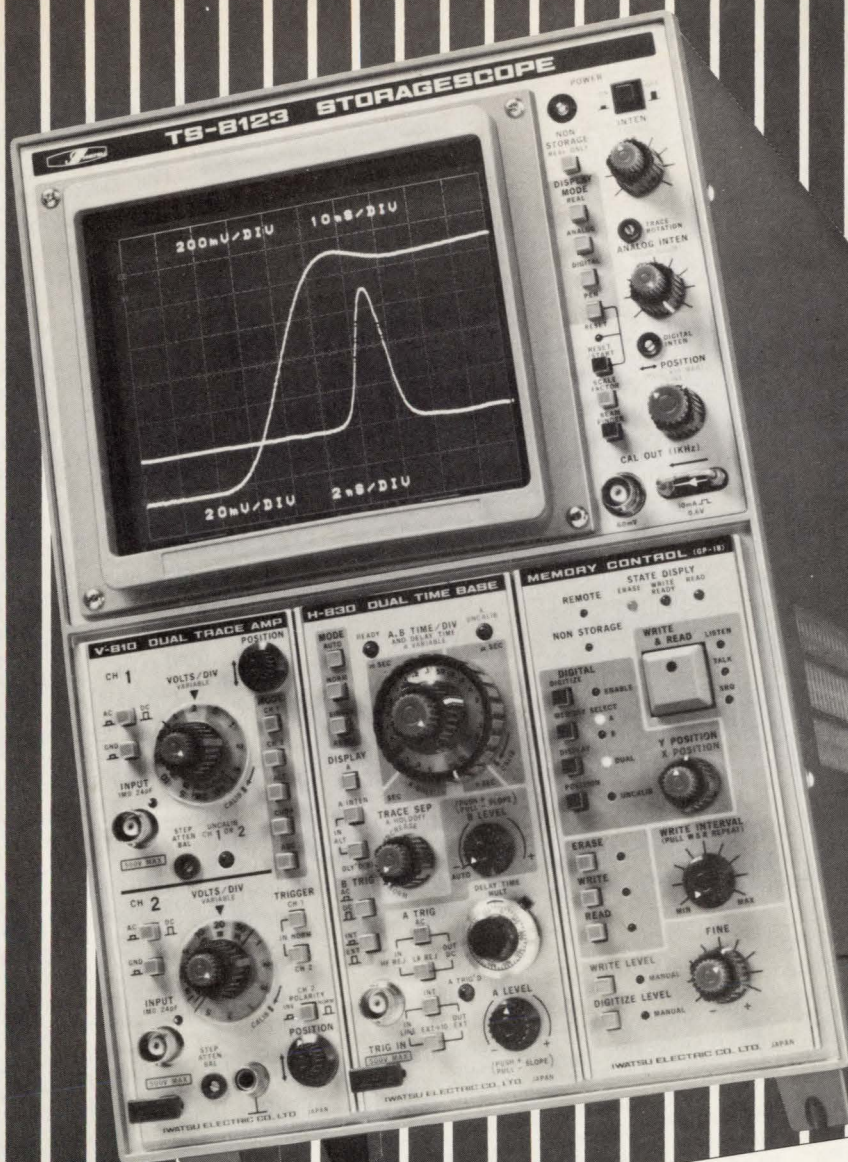
Chancellor Computer Corp's (South San Francisco, Calif) PC-based C2000 combines hardware and software with an effective engineering workstation. It uses an IBM PC XT with 512 Kbytes of memory, floppy and Winchester disks, a high resolution color graphics terminal, digitizing tablet, and optional printer and plotter. Software includes graphics entry and edit, schematic capture and netlist extraction, as well as an interactive logic simulator. It can be used alone or in multiterminal networks using Ethernet. A variety of communication protocols are also provided.

Such personal computer based systems may represent the future for low cost engineering workstations. Yet, there is no reason to limit it to IBM machines. CAD manufacturer Summagraphics (Fairfield, Conn), has built a system based on Data General's (Westboro, Mass) new desktop computer. Using the microEclipse in the Data General dual processor unit gives the system sufficient power to do architectural, mechanical, and construction work as well as printed circuit board design.

Advanced personal computers such as the HP 9000 will provide powerful engines for engineering workstations. The HP 9000 series 200 uses a 68000 processor while the series 500 contains a very powerful 32-bit single-chip CPU. Hewlett-Packard intends to compete in the CAE market with the product.

Getting closer

There are still gaps in the design-to-manufacturing spectrum, but the trend toward integration is clear. Chips and boards will be designed on CAE workstations and automatically produced. Hardware and software will be designed and tested by development systems combined with logic analyzers. In addition, the whole design and testing process will generate programs for automated manufacturing and automatic test equipment. This year brought the industry a step closer.



IWATSU'S CHALLENGE: TO FREEZE THE MOMENT

CAPTURING ONE-SHOT 100 MHz SIGNALS STORAGE OSCILLOSCOPE TS-8123

To this challenge, IWATSU has responded with the ultra-high writing speed of 2500 div/ μ s. High-speed analyses are being used with greatly increased frequency in such areas as semiconductors, lasers, ATE, CPUs, nuclear physics and communications. The TS-8123, using the scan converter tube and CRT display developed by IWATSU, has the required high speed capability. After a signal has been captured, A/D conversion can be performed at a speed of 1000 div/ μ s, equivalent to 40 ps, 25 GHz clock.

High-speed transient signals can then be processed simply in digital form via a GP-IB interface.

Main Features

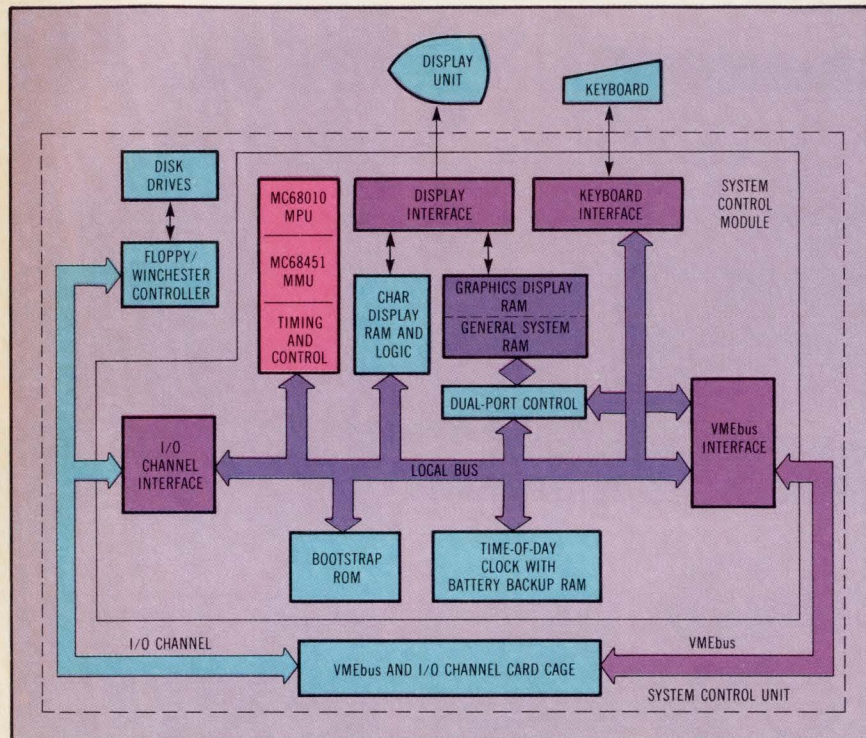
- CRT: 7", 8 div x 10 div (1 div = 12 mm)
- Analog: 2,500 div/ μ s
- Digital: 1,000 div/ μ s, 8 bit x 512 word
- Bandwidth: DC ~ 100 MHz
- GP-IB (IEEE-488) interface: Built-in



IWATSU INSTRUMENTS INC.
120 Commerce Road, Carlstadt, New Jersey 07072 Phone: (201) 935-5220 TLX: 7109890255 FAX: (201) 935-5220

CIRCLE 101

Microcomputer development system has complete set of tools



A single 12" x 16" (30.5- x 40.6-cm) card in the Motorola VME/10 microcomputer development system combines main system processor with memory management unit, 384K-byte RAM, and two bus interfaces.

Desktop microcomputer VME/10 serves three purposes. First, it is a complete development system for system OEMs working with Motorola 8- and 16-bit microprocessor and microcomputer chip sets. Second, it serves system integrators as a frontend microcomputer for use with larger equipment. And third, it can be a basic microcomputer for OEMs who add customized I/O and special software for dedicated applications. Although it now provides both 8- and 16-bit software, hardware, and instrumentation support, the microcomputer uses the MC68010 16/32-bit microprocessor. Therefore, it is upward compatible to 32-bit system configurations, such as the upcoming MC68020 microprocessor.

The VME/10 features built-in graphics capabilities and an optional 12" (38-cm) video display. Multislot cage and modular architecture permit system tailoring to desired level of complexity through compatible add-on modules. System performance combines the power of the MC68000 processor family with the international VMEbus standard and the full VERSADOS operating system, providing realtime operation and high level language compatibility. A separate built-in I/O channel, unique to the system, frees the VMEbus from handling the slower peripherals and significantly improves overall system capabilities.

A basic system consists of three interconnected physical elements: system

control unit, keyboard, and display unit. The system control unit, key to the system's flexibility and expansion capabilities, contains a system control module (together with VMEbus- and I/O-channel interface circuits), a 15M-byte fully formatted Winchester disk drive plus an 800K-byte fully formatted floppy disk drive, and a chassis (with power supply) that permits system expansion with up to five VMEmodules and four additional I/O modules.

Containing the MC68010 microprocessor and MC68451 memory management unit, the system control module permits several development tasks to proceed simultaneously (editing, program development, and system debugging) with full protection for each. A dual-port controller that allows shared access from both the local bus and the VMEbus, along with 384K bytes of onboard dynamic RAM, permit expansion to a high performance multiprocessor system by adding modules from the VMEmodule line of board-level products.

VMEbus and I/O channel interfaces provide configuration flexibility for a multitude of end applications. For example, with VERSADOS and the VMEmodule IEEE 448 GPIB controller, the microcomputer comprises a base system suitable for monitoring and controlling laboratory instruments. It can also be used to perform complex calculations on resulting experimental data, and then to graphically present the results.

Present system software includes the VERSADOS realtime operating system, MC68000/68010 macroassembler, MC68000 Pascal compiler, linkage editor, CRT editor, symbolic debugger, MC68000 Fortran, MC6800 family cross-assemblers, and PROM programmer drives. A Unix System v operating system with C compiler and an MC68000 Basic compiler are planned for the future. **Motorola Inc, Semiconductor Products Sector, 5005 E McDowell Rd, Phoenix, AZ 85008.**
Circle 356

Multiprocessor development stations improve productivity

Intellec Series IV takes us one step closer to the virtual engineering environment of the future. To improve productivity of designing and developing complex 16-bit systems, models 430/431 incorporate network-like functionality in stand-alone workstations. Combination of

hardware and software development tools results in improved designer productivity and shorter time to market for products.

Built on a multiple processor architecture, the system uses the 8088 running the INDX operating system for 16-bit devel-

opment projects. For 8-bit targets, projects run under the 8085 and the ISIS-N operating system. Even greater performance can be gained by upgrading the system with a 16-bit 8086-based board. This board increases throughput and adds 128K bytes of RAM to the system's

basic 384K bytes. Peripheral configurations of the system combine two 5¼" floppy disk drives with a standalone 35M-byte 8" Winchester or one 5¼" floppy with a 10M-byte Winchester disk drive.

Expansion with the NDS-II network development system improves productivity as shared peripherals and data bases are needed. With NDS, the foreground or background task of one workstation can be dedicated to a specific function, freeing other stations in the network for user interaction.

In conjunction with the integrated instrumentation and in-circuit emulator (I²ICE) system, the workstation supports full display of logic timing analyzer outputs. I²ICE combines 12-MHz in-circuit emulation, high level language debugging, and 100-MHz logic timing analysis for improved productivity.

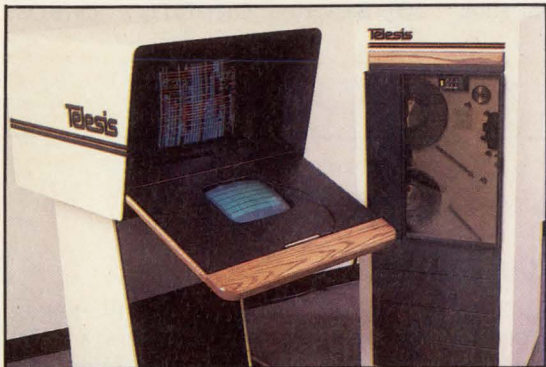
There are six system configurations: four standalone, and two networked workstations. The IMDX 430 WD standalone with two floppies and separate 8" 35M-byte Winchester sells for \$30,900. Incorporating an 8086 upgrade kit, this



system sells for \$34,900. The IMDX 430 WS network workstation has two floppy disk drives plus communication boards;

it sells for \$19,900. **Intel Corp**, 3065 Bowers Ave, Santa Clara, CA 95051. Circle 357

Graphics processor contributes roam, zoom, and high resolution



Using three microprocessors and a dual-ported architecture, Telesis Systems Corp's graphics processor produces picture resolutions up to 2000 x 1000 pixels. Several processor functions allow high performance processing in CAD/CAM systems.

Advanced processor functions are controlled through a proprietary "function screen." The function screen replaces the conventional array of I/O devices, computer languages, and menu codes with a single user-friendly device. English commands step the operator through design steps with an interactive approach.

The "roam" function allows the user to scan through a stored picture. This

function is accessible in two modes. The first is the "joystick" mode where the function screen takes on the characteristics of a velocity joystick. By using a lightpen, the user can roam the picture with a speed related to the displacement from the initial point on the screen. Therefore, the farther away one moves the lightpen from its starting point, the faster the picture will move.

Second, the "natural" roam mode allows the designer to work normally on the portion of a picture that is currently displayed. When the cursor is moved to the outer edges of the screen, the system automatically detects the limit and moves the picture in the appropriate direction.

Zoom control enables the designer to magnify picture size in increments of one, two, or four times. The designer can then focus on a particular section of the design for detailed editing. All functions and features are reentrant so that changes made in the zoom mode are automatically updated.

World window allows the designer to switch from a view of an entire schematic

or board design to a portion stored in the picture space. The switch occurs in less than 0.5 s, and synchronization is maintained between both representations. Window area can be increased or decreased at will, and, while in the world mode, the window portion is highlighted for visual verification.

There are two forms of cursor control. The system uses a full-screen vertical and horizontal crosshair to pinpoint the present cursor position. In addition, a dynamic cursor allows a symbol, a string of text, or a portion of a drawing to become the cursor. Once the cursor is chosen, it can be moved, in real time, to any desired location on the screen. No restrictions are placed on the dynamic cursor's size.

Implemented with a pipeline architecture, the system uses an 8-MHz 68000, an 8085, and the NEC 7220 graphics processor. Dual-ported memory and an optimizing cross compiler allow graphics software from the first-generation system to be downloaded to the 68000 for faster execution times. The 68000 also accesses data stored in pages on a Winchester disk, processes the data, then passes the data to the 7220 processor. The processor is \$7500. **Telesis Systems Corp**, 21 Alpha Rd, Chelmsford, MA 01824. Circle 358

Terminals and copier upgrade color graphics systems



A family of upwardly compatible color graphics products that span a wide range of functions has been introduced by Tektronix Corp. Included in the series are three low cost color terminals, a high end, high resolution color graphics terminal, and a low cost color copier. In addition, a graphics processing unit adds standalone graphics computation capabilities.

Highlight of the series is the 4115 terminal that Tektronix is adding to its 4110 graphics terminal line. The 4115 boasts a color raster scan display of 1280 x 1024 pixels, and a 32-bit coordinate space stores graphics. Up to 800K bytes of user RAM can be used to store a display list located anywhere within that 4G x 4G coordinate area. Improved vector drawing at 50k short vectors/s and 1 μ s/pixel lets the 4115 approach realtime pan and zoom operations. Area filling has likewise been accelerated, and the terminal can fill at a rate of 10k small rectangles/s, where a small rectangle is defined as 25 x 25 pixels. For each pan, zoom, and fill operation, the terminal completely traverses and redraws the entire display list.

Like other 4110 series members, the 4115 has RS-232 serial communication

capability up to 19.2k baud, but it also features a DEC VAX computer DMA channel that can transfer data up to 2000' (610 m) at 1M byte/s.

One innovation soon to become an option on the 4115 is autoconvergence. Autoconvergence is an extension of digital convergence, which uses a feedback method to sense and dynamically control CRT convergence. Like digital convergence, autoconvergence stores rough convergence values in ROM and fine adjustment values in CMOS RAM; there are 256 convergence areas on the screen. But unlike digital convergence, which requires a human operator to enter the fine adjustment values, autoconvergence enters this data itself.

Sensors look through the rear of the CRT envelope at phosphor dots on the back of the shadow mask. Each beam from the delta gun is swept separately. Sensors feed values back to the convergence processor and RAM until each beam successfully illuminates each dot and the display is properly converged. According to Tektronix, less than 0.2-mm misconvergence over the entire display results. **Tektronix, Inc.**, PO Box 500, Beaverton, OR 97077. **Circle 359**

Multi-user development system runs Unix derivative

Using Genix, a version of Berkeley Unix 4.1, SYS16 develops applications for the NS16000 16/32-bit microprocessor family. The system features access to assembler, C, and Pascal compilers, as well as real-time in-system emulation tools. Emulation and software development can be performed concurrently.

Two main units make up the system: a processor module, and a disk/tape module housing a 20M-byte 8" Winchester disk with 20M-byte $\frac{1}{4}$ " streaming-tape backup. Optional disk drive modules increase system capacity in 40M-byte increments up to 140M bytes.

Demand-paged virtual memory expedites development of systems that operate in multiprogramming and large database environments. Internal data paths, 32-bit registers, and an ALU provide fast pro-

cessing. Information is transmitted over a 16-bit data bus that links the CPU to 32-bit floating point, memory management, and custom processor chips.

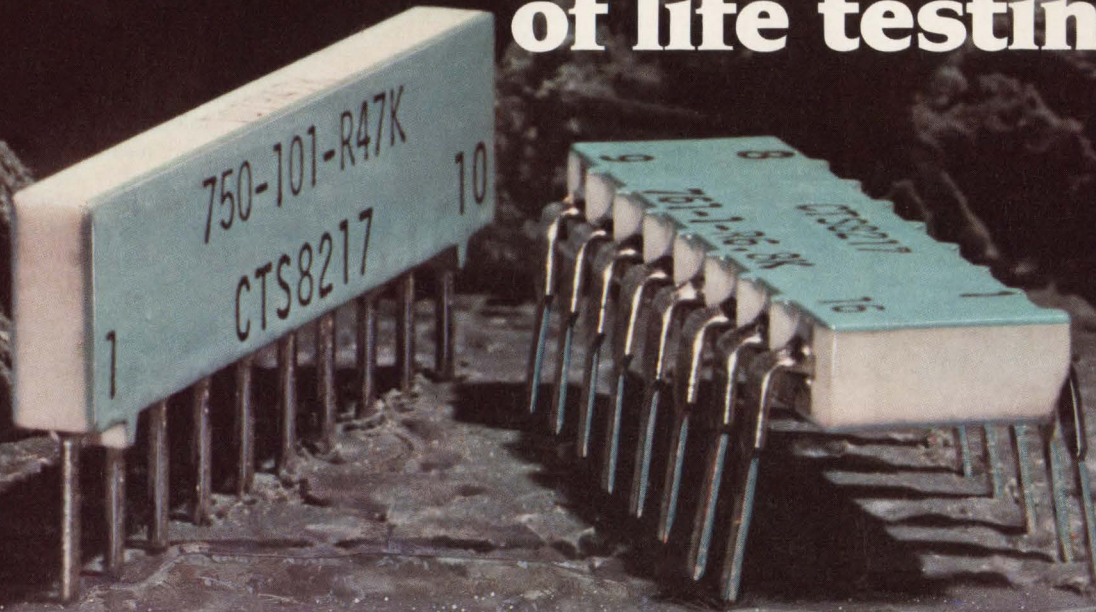
The system configures with up to eight terminals. Each user can independently address up to 16M bytes of memory, using virtual memory management to swap 512-byte pages of program or data directly between main and disk memories. Main memory itself consists of 1.25M bytes of RAM, expandable to 3.25M bytes with provision for error checking and correction.

In its standard configuration, the processor module connects CPU, serial I/O, memory, and disk/tape controller boards in four of six available slots. The remaining two slots accommodate optional memory boards.

The CPU board contains the NS16032 microprocessor with peripheral support chips. Diagnostic firmware; 256K bytes of RAM; and parallel, GPIB IEEE 488, and RS-232 ports also reside onboard. The intelligent serial I/O board contains logic to support the eight RS-232 user ports. Each port operates at up to 9.6k baud, with FIFO buffers to increase system throughput. The disk tape controller board manages up to eight disk drives with streaming-tape backup.

Hardware support for the system includes external PROM programming and an optional ISE/16 NS16032 in-system emulator. The SYS16 will cost around \$30,000. **National Semiconductor Corp., Microcomputer Systems Div.**, 2900 Semiconductor Dr, MS D3670, Santa Clara, CA 95051. **Circle 360**

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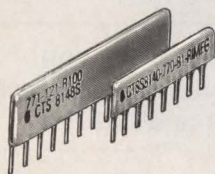
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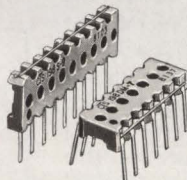
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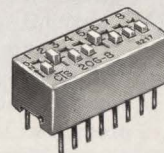
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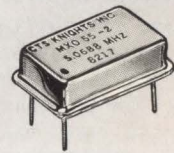
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Emulation support for 68000



ES-68000 provides the MC68000, 8080, Z80, and Z8000 families with in-circuit emulation, running the user's system in real time up to 10 MHz (12.5-MHz capability planned). Emulation debugging requires no space, uses no I/O ports, does not interfere with interrupts, and requires no modification to the system under test. Unit also features a 2046-step x 72-bit wide trace history, breakpoint system, and optional 16-channel logic state analyzer. The emulator can stand alone or run from a remote computer. Price with options is \$9950. **Applied Microsystems Corp**, 5020 148th Ave NE, PO Box 568, Redmond, WA 98052. Circle 361

Network analyzer

The 3577A provides high accuracy and resolution over the 5-Hz to 200-MHz frequency range. Measurements can be made over the analyzer's 100-dB dynamic range with up to 0.02 dB and 0.2 degree dynamic accuracy. Features include an auto-scale for measurement on the screen with a full scale display, user-defined vector math, and multiple display formats with electronic graticules for accurate displays in rectangular, polar, or Smith chart coordinates. The analyzer is priced at approximately \$23,000. **Hewlett-Packard Co**, 1820 Embarcadero Rd, Palo Alto, CA 94303. Circle 362

System 6502 analyzer

Interactive microprocessor in-circuit system analyzer for 6502 software development, the DA6502-A is \$279 in single quantity. The portable analyzer allows the user to easily examine processor registers, read/modify memory locations, halt a program at a specific

address, step through a program, and stop a program at a location after a number of loops has been completed. The standalone, clip-on microprocessor analyzer has an 8-digit hex display. Microprocessor is keyboard accessed with 24 switches. Unit is approximately 6.25" x 7.5" x 3.5" (15.88 x 19.1 x 8.9 cm). **DA-TECH Corp**, 92 Steamwhistle Dr, Ivyland, PA 18974. Circle 363

Graphics development system

The EROS/186 development system provides a complete 80186 based micro-computer system. It includes high resolution color graphics with full-function realtime multitasking operating system and high level runtime language support for program development. The unit operating system is the IRMX 86, which contains the UDI/URI interfaces. Hardware features include an 8" flexible disk controller, programmable interrupt controller, 64K bytes of RAM, and 512K bytes of system memory. Prices range from \$10,000 to \$60,000 (Canadian). **Datam Ltd**, 7 Slack Rd, Suite 206, Nepean, Ontario K2G 0B7, Canada. Circle 364

Modular logic analyzer

K105-D is a 72-input logic analyzer for digital system design and development. It sets up with 32 or 64 main (20-MHz) state and timing sample inputs and 8 or 16 high speed (100-MHz) state and timing sample inputs, along with RS-232 GPIB communication and disk storage. Eight levels of trace control, using up to 32 different word patterns, allow precise definition of the analysis path and selection of specific segments of system operation. **Gould Inc, Design and Test Systems Div**, 4600 Old Ironsides Dr, Santa Clara, CA 95050. Circle 365

Development system VMEbus

VMEbus Baseline system allows the evaluation and development of VMEbus-compatible systems. Standard is a 10-slot VMEbus-compatible backplane equipped with three VMEbus boards: the VME-SBC, VME-SIO, and VME-DRAM. These boards provide an MK68000 microprocessor, five RS-232 serial I/O channels, 256K bytes of DRAM with byte parity, 12K bytes of

static RAM, interrupt control, and two timer/counters. Monitor and debugger firmware perform initialization, DRAM diagnostics, display/modify memory, and program disassembler. Price is \$6995. **United Technologies Mostek**, 1215 W Crosby Rd, Carrollton, TX 75006. Circle 366

Software development

The DV286 80286 software development vehicle (\$2495) works with CP/M-80 and CP/M-86 based development systems, or Intel development systems running the 8086 assembler. A MACRO286 (80286 instruction macro package) and execution vehicle (IEEE 796 compatible board with iAPX 286 microprocessor and full virtual memory capability) must be installed. Software can be developed on the host and then loaded to the execution vehicle over an RS-232 port. PROM-based DEBUG286 provides single-instruction execution, breakpoint setting, memory disassembly, and examine/modify of memory, I/O, and registers. **Microbar Systems, Inc**, 1120 San Antonio Rd, Palo Alto, CA 94303. Circle 367

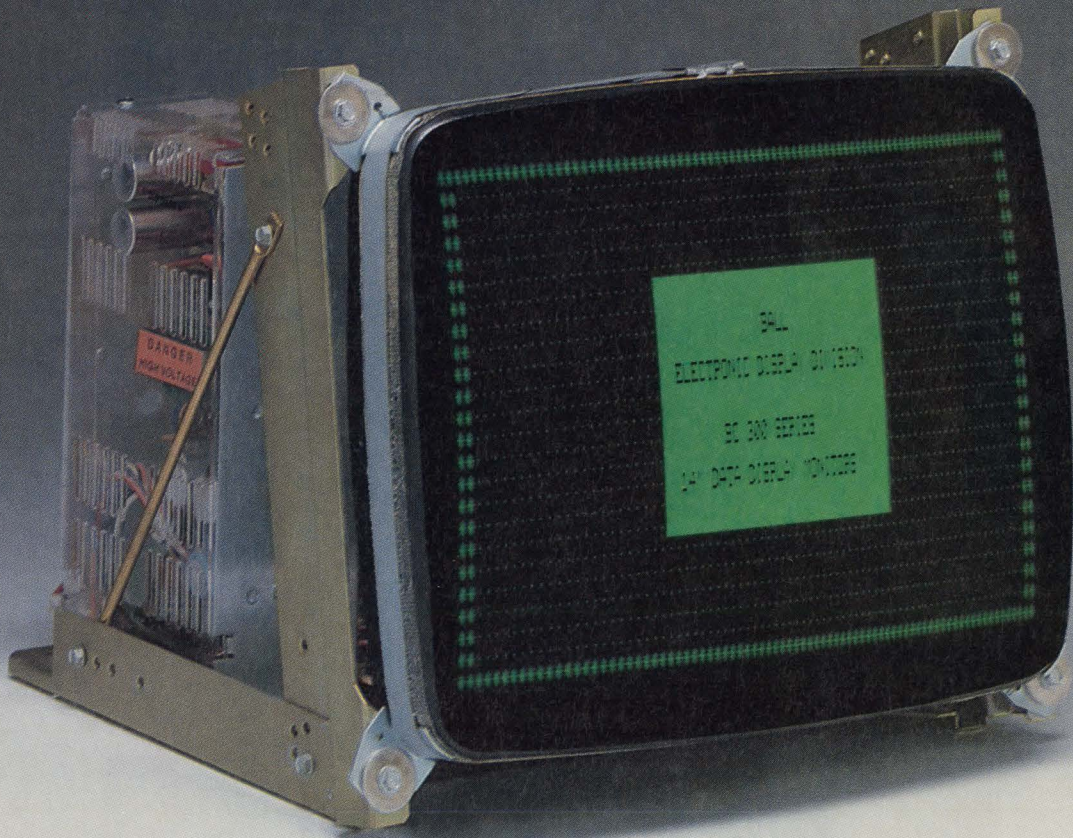
Communications tester

Chameleon is an adaptable development tool for X.25, SNA/SDLC, ADCCP (HDLC, SDLC, extended mode), and Bisync protocols using ASCII, EBCDIC, or hexadecimal format. With 700K bytes of online storage, the system will analyze traffic density and response times, develop and support hybrid protocols, and simulate DTE or DCE devices in bit- or byte-oriented environments at speeds to 128k bps. The portable system comes in a 17.25" x 8.75" x 16" (43.82- x 22.23- x 41-cm) case with integral 9" (23-cm) green screen. Weight is 35 lb (16 kg). Two high speed 3½" Sony disk drives provide 350K bytes each of formatted program/data storage, with a 500k-bps maximum transfer rate. **Tekelec Inc**, 2932 Wilshire Blvd, Santa Monica, CA 90403. Circle 368

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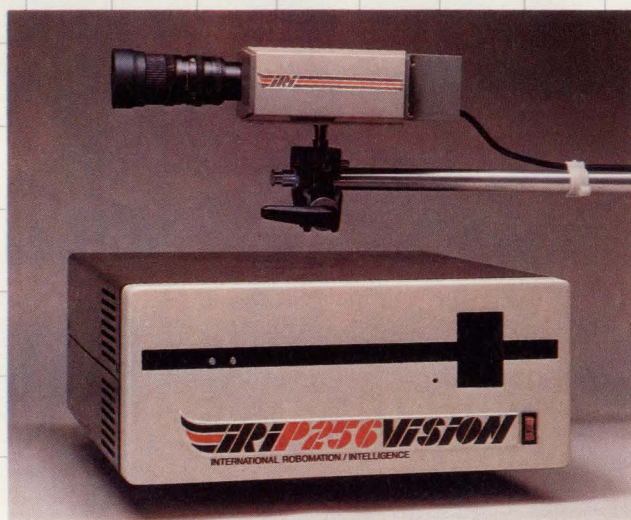


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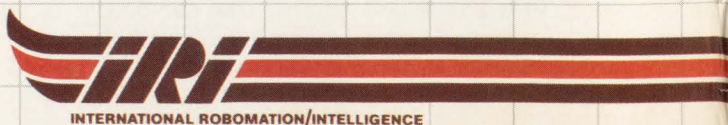
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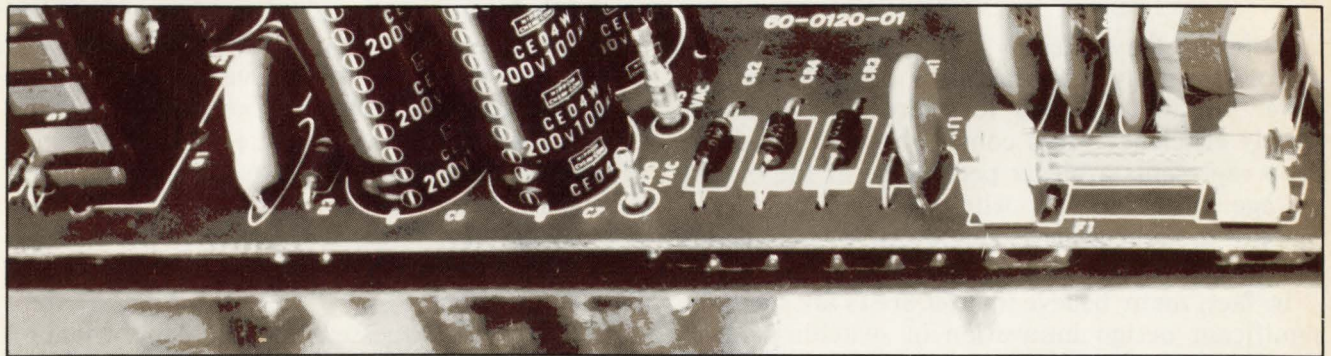
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POWER SUPPLIES COME TO GRIPS WITH MOS TECHNOLOGY



by **Deb Highberger,**
Senior Associate Editor

Charged in the past with being slow to respond to industry changes, in 1983 power supply manufacturers worked toward several important advances in the high technology market. Interdependent efforts with logic designers will most likely result in lower voltage specifications geared to next year's crop of denser components. The goal is to design power supplies that will facilitate scaled-down semiconductor technology while maintaining compatibility with today's 5-V universal standard for integrated circuits.

The Joint Electron Devices Engineering Council (JEDEC) is expected to approve a draft proposal to lower the 5-V specification during the first or second quarter of 1984. Recommended are a 3.3 ± 0.3 -V guideline for regulated power supplies, a 2.8 ± 0.8 -V standard for battery-powered devices, and a series of three interface parameters for various logic families.

Proposed specifications for battery-powered devices are intended to meet the operating supply limits of new-generation, high performance CMOS logic at the low end and the 3.6-V regulated specification at the high end. A 3-V regulated level has

already been recommended by the federal Very High Speed Integrated Circuit (VHSIC) program.

The original reason for considering a lower power supply voltage was to accommodate continuing density improvements in MOS devices, particularly gate-oxide thickness. In other words, according to William Huber, chairman of the JEDEC MOS memory committee responsible for coordinating the draft proposal and applications manager at General Electric's Microelectronics Center in Research Triangle Park, NC, a legitimate MOS scaling must include scaled-down power supply voltage. This will keep electrical fields within a reasonable range and avoid reliability problems caused by electron effects.

As it stands now, the proposed 3.3-V level and current-drive capability retain full TTL compatibility. However, the bipolar memory group—the only committee yet to approve the proposed voltage and interface standards—is expected to recommend a sacrifice in noise margin to match their low end power supply limits. In that case, the draft proposal will not match the full TTL noise margin, though it will probably come close.

The goal of the draft proposal is to create a target specification to guide future design efforts for both integrated circuit and power supply

designers. It is aimed at all integrated circuit logic families, with the probable exception of ECL. Proposed guidelines will allow designers to use a single power supply to drive the different technologies involved in a system.

Of course, designers will not convert to the revised standard guidelines overnight. While no components built to these specifications have been announced yet, it is a sure bet that System Components '84 coverage will begin to track their development. All the same, 5-V days are far from over. At least in the near term, TTL parts will probably continue to be used for glue chips, and 256-Kbit dynamic RAMs will continue to run off 5 V. However, Huber comments, "I see all parts—at least logic parts—eventually going toward the 3.3-V standard."

Questioning the switch

Power supply manufacturers observe that the lower voltage will lead to a drop-off in power supply efficiency. This comes about as the diode drop represents a bigger percentage of the output voltage. A shift to MOS switching power supplies in place of diode rectifiers is one way to overcome this efficiency decrease.

In fact, many believe that MOSFETs are the most significant design innovation in switching power supplies in years. Only a handful of manufacturers is firmly committed to these voltage-driven devices so far. However, MOSFETs may begin to supplant current-driven bipolar transistors in new switching power supplies over the next few years.

The MOSFETs achieve higher switching rates, which allows smaller magnetic components and, consequently, smaller overall size of the power supply package. Several commercial MOSFETs are specified at 100 kHz, although the class of devices operates at bandwidths several times that frequency.

When it comes to determining conformance with federal regulations governing emi/rfi, MOSFETs are advantageous because such interference is easier to control at higher bandwidths. As a result, power-supply designers are collectively increasing switching rates from the 30- to the 100-kHz range. The drawback to bipolar transistors is comparative slowness, particularly at higher power levels.

Meanwhile, bipolar manufacturers are claiming that price and yet-to-be-proven reliability keep them from making the switchover to MOSFET technology. Semiconductor manufacturers believe that MOSFETs will become cost competitive with bipolar transistors for power ranges under 500 W in the near future.

In general, regulated switching supplies are more attractive to computer and peripheral system designers than linear supplies because of their wide

input voltage range, small size, high efficiency, and cool operation. For example, typical input voltage range for switcher (versus linear) regulated power supplies is ± 20 percent (versus ± 10 percent), efficiency is 60 to 80 percent (versus 40 to 55 percent), and holdup time is 32 ms (versus 2 ms).

On the other hand, linear supplies remain active in an estimated 50 percent of installations for their own set of strengths. They continue to play an important role in computer equipment, particularly in test and measurement applications. For instance, linear load regulation is generally 0.02 to 0.1 percent (versus 0.1 to 1.0 percent for switchers), while linear line regulation is 0.02 to 0.05 percent (versus 0.05 to 0.1 percent).

Other typical performance comparisons of linear over switching are gains of 10^6 to 10^7 versus 10^2 to 10^3 , dynamic range of 100 to 120 dB versus 20 dB, output ripple of 0.5 to 2 mV rms versus 25 to 100 mV peak to peak, and transient recovery of 50 μ s versus 300 μ s. Such features often make linear power supplies the preferred option. In fact, many designers accompany a regulated switching supply with linear post regulators.

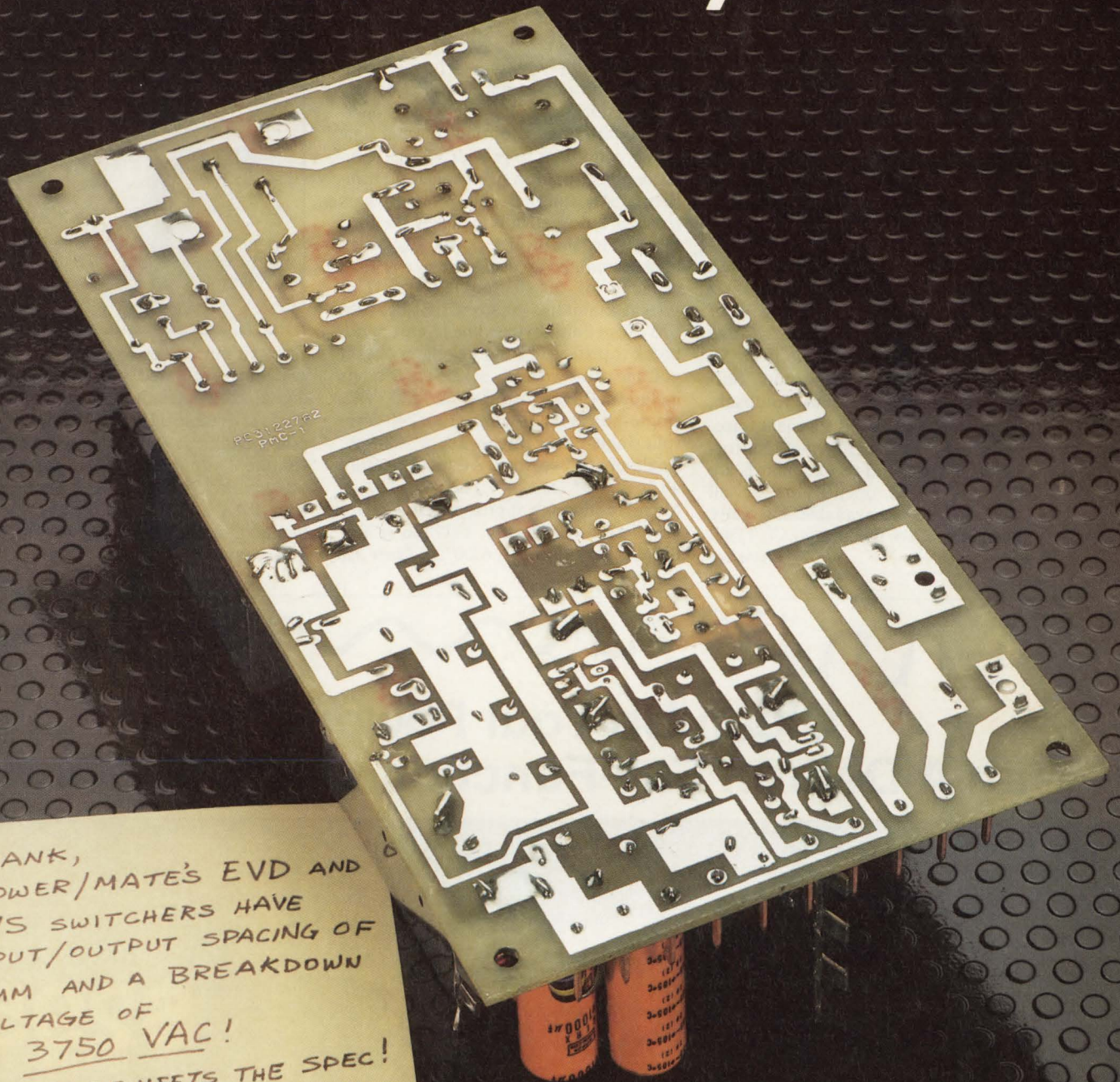
Backing up offline

This year also witnessed the rapid deployment of high performance, low cost microcomputers handling critical loads in broad-reaching applications. To keep uninterruptible power supplies apace with continuing cost/performance advances, power designers continued to extend the range of offline backup systems. Unfortunately, online approaches already popular in mainframe and minicomputer installations are usually too expensive a solution for today's bumper crop of low cost computer equipment. Instead, manufacturers are capitalizing on advances in switch technology to make inexpensive, offline power backup feasible. At 60 Hz, for example, target transfer times of 4 to 10 ms are connecting offline backup sources within that critical one-cycle interval.

Offline power protection for the ubiquitous microcomputer is outpacing its online alternative because of lower operating as well as lower production costs. Whereas online protection consumes power continuously, offline systems consume power only when they are needed. Offline systems also avoid the heat buildup that comes from an additional, constant online power source.

Finally, because most power losses and voltage fluctuations last less than 10 minutes (and many last only a few seconds), a growing number of power protection manufacturers are gambling on the trend toward these short-haul, offline insurance policies.

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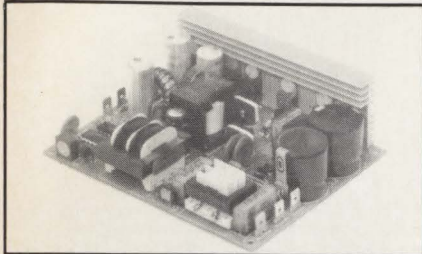
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CIRCLE 105

High frequency switchers

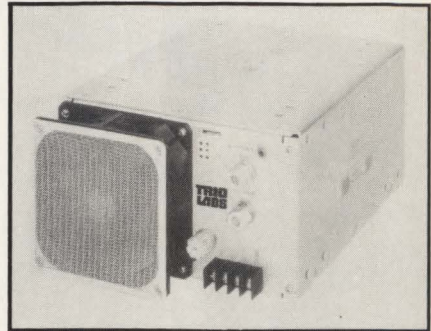


Delta series switchers have a 100-kHz switching frequency providing 60 W of dc power from both 120- and 240-Vac lines. Multi-output is available from 5-, ± 12 -, or ± 15 -Vdc fixed outputs. Soft start, isolated output, 50% foldback, $\pm 0.1\%$ regulation, 80-dB transient rejection, up to 80% efficiency, and conformance to FCC, UL, and CSA standards are featured. PC board, open frame, or full enclosure models are available. **Energetec Systems, Inc.**, 2204 Wellington Ct, Lisle, IL 60532. Circle 369

Online uninterruptible power

A 5-kVA supply maintains precise, conditioned ac power and reserves battery backup during total line failure. It operates continuously during normal line power conditions to provide voltage regulation plus isolation from noise and transients. An internal solid state bypass transfer automatically switches the load directly to the utility power line when load demands exceed system overload capacity of 200% for 167 ms. This system maintains phase match between UPS output and bypass line to ensure no-break transfer. The unit regulates output voltage to within $\pm 1.5\%$. Models include 60-Hz with I/O at 120 Vac, single-phase two-wire; 120/240-Vac, split single-phase three-wire; or 208-Vac, single-phase two-wire. All units measure 48" x 40" x 24" (122 x 102 x 61 cm), and weigh approximately 1000 lbs (454 kg). **Sola Electric**, 1717 Busse Rd, Elk Grove Village, IL 60007. Circle 370

Regulated switching supplies



The enhanced 682 series of 750-W switching regulated power supplies for digital and memory systems features dual, selectable 115/230-Vac input, full power output at 71 °C, and up to 2 W/in.³ volume. Output levels range from model 682-02 with 150 A at 2 V to model 682-48 with 19 A at 48 V. **Trio Laboratories, Inc.**, 80 Dupont St, Plainview, NY 11803. Circle 371

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tolerant to battery back-up systems.

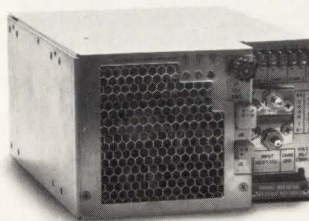
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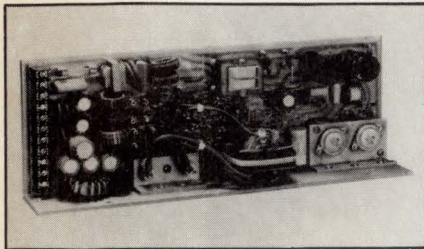
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Q150 designates a series of 150-W, quad-output switchers. They are available in four models and in open or closed frame chassis. Q150 Cool 1 supplies have input ratings of 90 to 132 and 180 to 264 Vac, field selectable links, 47 to 440 Hz. The units offer a tightly regulated output and auxiliary outputs can be quasi-regulated. Reliability features include two surge limiting varistors, two voltage clipping varistors, TO-3 hermetic switch transistors, and anti-saturation Baker clamps. Price of the units, in one to nine pieces, is \$290. **Deltron, Inc.**, PO Box 1369, Wissahickon Ave, North Wales, PA 19454.

Circle 372

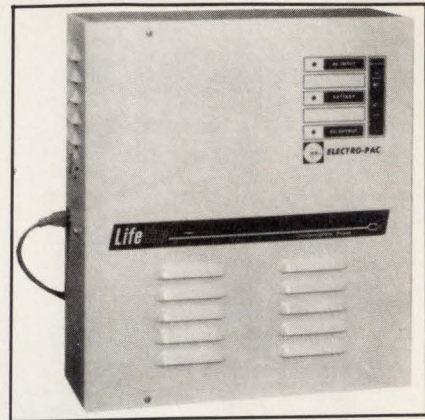
Small four-output switchers

XL50 family of four-output switching power supplies delivers 60 W in a standard 4.25" x 7.75" x 2" (10.80- x 19.69- x 5-cm) form factor. Proprietary current controlled feedback network yields tight regulation and low ripple/noise. All models have short circuit protection, input surge protection, 20-ms holdup time, and 90- to 132-Vac or 180- to 264-Vac user selectable input voltage. The supplies operate with no power derating in a 50 °C ambient range and have overvoltage protection on the 5-V output. In lots of 1000, price is \$60. **Boschert Inc.**, 384 Santa Trinita Ave, Sunnyvale, CA 94086.



Circle 373

Continuous standby ac



Lifeline power system provides clean, reliable 5 A of 120-V sine wave power for computers, memories, disk systems, communication terminals, and security systems. The unit requires no initial startup adjustments. Voltage regulation and filtering are provided at all times; an inverter supplies power during power outages, and a charger keeps the batteries at proper float and recharges them after a power outage. There is no transfer time and, therefore, no interruption of power to the critical load. **Instrumentation and Control Systems, Inc., Electro-Pac Div.**, 520 Interstate Rd, Addison, IL 60601.

Circle 374

Low Cost Microprocessor Development System —



Your Computer —

Our Emulator!



Huntsville Microsystems offers a line of high performance in-circuit emulators and linking software packages which will turn any computer into a full microprocessor development system. The emulators feature real-time transparent emulation, mappable memory, hardware breakpoints, RS232 interface, upload/download hex files and complete debugging facilities. The units can operate stand-

alone with a CRT or when combined with the power of your computer form a full microprocessor development system.

Software packages are available to allow operation with any CP/M™ or ISIS™ system including the Intel™ iPDS™. Currently, in-circuit emulators are available for the 8085, Z80™ and NSC800. Prices start at under \$2000. Write for complete specifications.



Huntsville Microsystems, Inc.
8200 South Memorial Parkway,
P.O. Box 12415
Huntsville, AL 35802

(205) 881-6005

Z80 is a registered trademark of Zilog, Inc. CP/M is a trademark of Digital Research. ISIS, Intel and iPDS are registered trademarks of Intel Corp.

Power modules for PC boards

Models 3.12.1000 and 3.15.1000 are triple-output power supplies designed for PC boards. The 3.15.1000 has ±15 V at 100 mA and 5 V at 1 A. The 3.12.1000 has ±12 V at 120 mA and 5 V at 1 A. Each unit has digital and analog outputs. A high efficiency regulator for the 5 V output helps it run cooler when fully loaded (up to 50 °C ambient temperature). Additional features are low noise level, isolated analog and digital grounds within each unit, and protection for all outputs against shorts. The supplies are priced as \$101.15 at the 100-piece level. **Calex Manufacturing Co, Inc.**, 3355 Vincent Rd, Pleasant Hill, CA 94523.

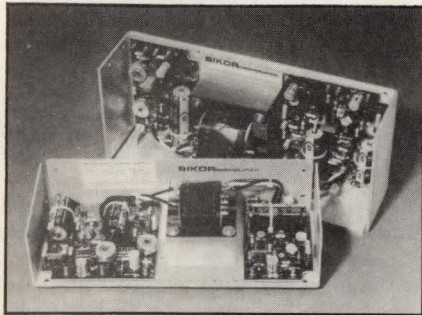
Circle 375

Power distribution systems

Guardsman, Isoshield, and Isoreg incorporate three common elements: power monitoring console, flexible conduits or shielded cables, and watertight junction box. Line is available in one- and three-phase models ranging from 22.5 to 225 kVA. **Isoreg Corp.**, 410 Great Rd, Littleton, MA 01460.

Circle 376

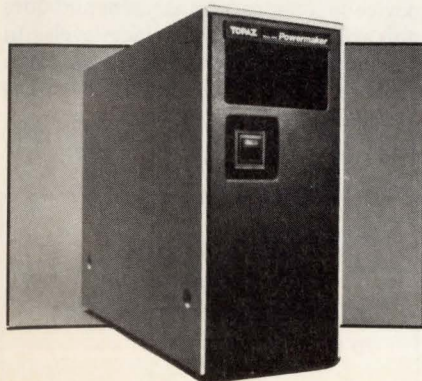
Open frame linear source



LT series multi-output power supplies feature full output ratings to 50 °C, 115- and 230-Vac inputs, and remote sense. Foldback current limiting overload protection, overvoltage protection, reverse voltage protection, and oversized components to run cooler are included. Seven case sizes with output voltage combinations from 5 to 24 V and 0.5 to 12 A are available. Line regulation is $\pm 0.05\%$ for a 10% change and load regulation is $\pm 0.05\%$ for a 50% change. Ripple is 5 mV pk-pk; dc outputs can be adjusted $\pm 5\%$ min. Price range is \$69.95 to \$126.95. **Bikor Corp.**, 1504 W 228th St, Torrance, CA 90501. **Circle 377**

Microcomputer backup

Powermaker protects small computers against blackouts, voltage sags, and power line noise. Standard features include maintenance-free lead-acid battery, and protection against overcurrent, short circuit, and battery discharge. Alarm sounds when output power is supplied by the battery. Typical backup times range from 6 to 35 minutes. Output ratings are 400 and 800 VA. Noise attenuation begins at 10 kHz and is 40 dB minimum over 100 kHz. Transfer time from power line to inverter is 4 ms typical, 10 ms max; for inverter to power line, 2 ms typical, 4 ms max. **Topaz, Inc., Electronics Div**, 3855 Ruffin Rd, San Diego, CA 92123.

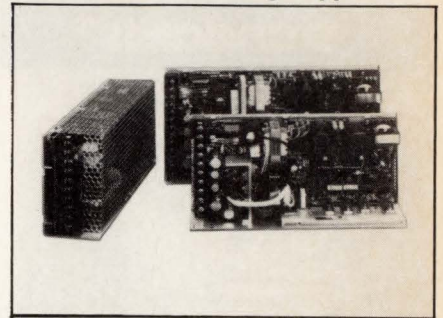


Circle 378

Single-output dc-dc converters

The EP series mini dc-dc converters include four models with 5-Vdc input and 5-, 12-, 15-, and 24-V output; four models have 12-Vdc input and 5-, 12-, 15-, and 24-V output. Four models have 24-Vdc input and outputs of 5, 12, 15, and 24 V. Additional models can be customized to specific requirements. **KSC Electronics, Inc.**, 543 W Algonquin Rd, Arlington Heights, IL 60005. **Circle 379**

Winchester switching supplies



Designed for Winchester disk drive applications, the KS100-05/06 and the KS130-05/06 provide 100- or 130-W switching power, respectively. Units have a second 12-V output that allows two 12-V outputs to be put in parallel, thereby doubling the current. This feature accommodates hard disk drives that require high surge current at startup and higher continuous current during operation. In one- to nine-unit quantities, the KS100 is \$188; the KS130 is \$205. **KEC Electronics**, 20817 Western Ave, Torrance, CA 90501. **Circle 380**

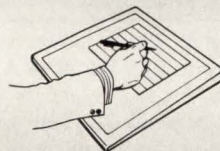
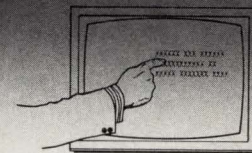
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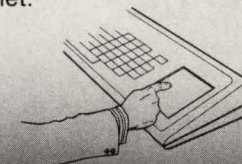
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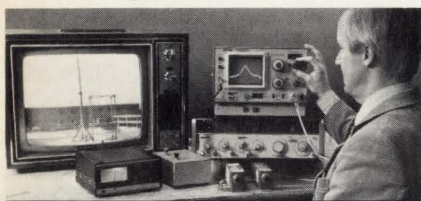
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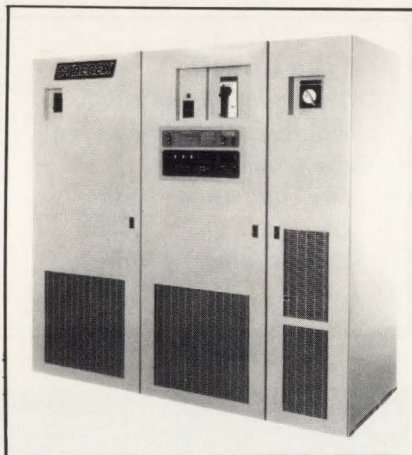
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CIRCLE 110

POWER SOURCES & INTERCONNECTION

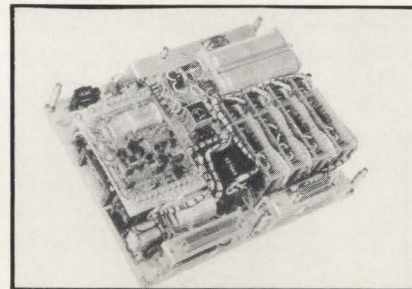
Transistorized power system

Uninterruptible system, in 60- or 415-Hz models, supplies high efficiency and fast response to power fluctuations. Removable dead front isolation panels minimize possible shock exposure. Mimic readout at front of cabinet monitors all operations. Digital meter displays system performance data. The units need 20% less floor space than comparable models; front-only access eliminates need for back and side space requirements. **Cyberex Inc**, 7171 Industrial Park Blvd, Mentor, OH 44060.



Circle 381

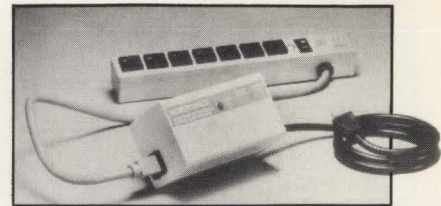
Modular switching supply



Model M7935 240-W power supply provides outputs of 5 Vdc at 15 A, 12 Vdc at 4 A, ± 15 Vdc at 2 A, and 28 Vdc at 2 A. Input voltage is 115 Vac at 400 Hz, single-phase. Op temp range is -40 to 85 °C; max cold plate temp is 75 °C using conduction cooling. Auxiliary outputs achieve high efficiency and synchronization to the 5-V output main rail via magnetic amplifier post regulated module. No high power switching or linear pass transistors are used. The 75% efficient unit is manufactured to MIL-T-28800B and MIL-STD-454. **CEAG Electric Corp, Power Supply Div**, 1324 Motor Pkwy, Hauppauge, NY 11788.

Circle 382

Voltage monitor/surge suppressor



Model CMP-905 combined voltage monitor and surge suppressor includes a rugged Lexan housing, an LED line voltage monitor, an internal overload fuse, and one outlet that can be used with a multi-outlet bus strip. Fast action, high capacity metal oxide varistor diverts voltage transients before system damage can occur. A two-pole LC filter reduces emi/rfi noise. **Nortronics Co Inc**, 8101 10th Ave N, Minneapolis, MN 55427.

Circle 383

Transient voltage suppressor

Series T-25 Clipper protects 18 lines against transients and surges that might enter the interface of an unprotected host system. All units operate at a serial baud rate from dc to 19,200. The transient voltage suppressor handles a maximum data signal amplitude of 40 V pk to pk. It has a surge rating of 64 A in each direction. Each unit has two female, D-subminiature 25-pin connectors. A 6" (15-cm) male ribbon cable is optional. **Dymark Industries**, 21 Governor's Ct, Baltimore, MD 21207.

Circle 384

Protection for RS-232

The Surge Sponge protects RS-232 interfaces from high voltage transients produced by inductive coupling of interface cables with high power cables. Model 21 has MOV devices to protect pins 2, 3, 4, 5, and 7 of the interface. On any of these pins, all voltages that exceed approximately 27 V are clamped to ground. All interface pins are wired through the device so it appears transparent and does not affect standard interface levels. In 100-piece quantities, it sells for \$32 each. **Remark Datacom Inc**, 4 Sycamore Dr, Woodbury, NY 11797.

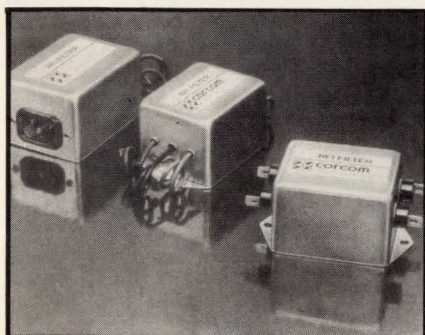
Circle 385

Talk to the editor

Have you written to the editor lately? We're waiting to hear from you.

Power line protection

The Q series rfi power line filters for switching power supplies control conducted emissions down to 10 kHz. High attenuation for both line-to-line and line-to-ground interference is provided throughout the frequency range and ensures no performance degradation due to peak currents drawn by equipment. Series is suited to applications that meet B level limits of VDE 0871 below 150 kHz, and FCC part 18 from 30 MHz down to 10 kHz. Standard leakage current (VQ series) and low leakage version (EQ series) are available. All models are UL recognized, with CSA and VDE approvals pending. Three case styles and rated current of 3 A at 115 Vac or 2 A at 250 Vac, 50 to 60 Hz, with a rated voltage of 115/250 Vac are available. **Corcom Inc**, 1600 Winchester Rd, Libertyville, IL 60048.



Circle 386

Enclosed/shielded switchers

A line of enclosed and shielded multi-output power supplies, the EMR series provides power in the 20- to 80-W class. Three or four outputs are rated for CRTS, logic, disk drives, CPUs, and memory. Designed with a computer, the supplies employ a proprietary hybrid micro-circuit to reduce part population. An onboard conducted emi filter meets the requirements for FCC Class B computing devices. The 80-W model has sufficient 24-V power to run an 8" floppy disk drive. **Kepeco Inc**, 131-38 Sanford Ave, Flushing, NY 11352. **Circle 387**

Backup power supplies

Programmed Power Centers offer efficiency and reliability at all standard load levels. They feature built-in paralleling for redundancy or expansion without modification. The systems conform to NEMA, IEEE, and ANSI standards. **Liebert Corp**, 1050 Dearborn Dr, PO Box 29186, Columbus, OH 43229.

Circle 388

Line-to-ground filters

The F2100 and F2200 international series filters feature IEC connectors for general purpose rfi control of line-to-ground noise. The filters are available in 1-, 3-, and 6-A models and meet low leakage current requirements of UL, CSA, VDE, and SEV. Rated voltage is 115/250 Vac. Max operating ambient temperature at rated current is 40 °C. Max leakage current each line to ground is 0.25 mA at 115 Vac, 60 Hz and 0.48 mA at 250 Vac, 60 Hz. **Curtis Industries, Inc**, 8000 W Tower Ave, Milwaukee, WI 53223.

Circle 389

Compact power systems

Designed for EIA rack, desktop, or wall mounting, the A52CP line requires 80% less space than previous models, making them suitable for laboratories, office, and production areas. These units supply continuous, disturbance-free computer grade power regardless of the ac line condition. Utilizing CMOS logic and highly reliable sine weighted pulse width modulation, the systems are equipped with electronic output voltage regulation, quartz time base, 120% current limit, and power walk in. **LaMarche Mfg Co**, 106 Bradrock Dr, Des Plaines, IL 60018.

Circle 390

Batteries back up memories

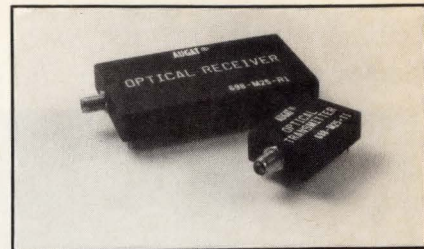
Lithium batteries can be soldered directly into PC boards and deliver a rated 3 V for memory backup. Three flat types have rated capacities from 120 to 200 mA, continuous discharge current of 0.1 to 0.2 mA, and pulse discharge current from 3 to 5 mA. Two cylindrical batteries have rated capacities of 160 to 1000 mA, and pulse discharge current of 30 and 70 mA. **Sanyo Electric Inc, Battery Div**, 200 Riser Rd, Little Ferry, NJ 07643.

Circle 391

Dense DIN connectors

RNE series DIN connectors provide up to 50% more I/O connectors per lineal foot with an installed cost approximating edge cards with gold PC board pads. Connectors come in two- or three-row bodies with 64 or 96 contacts. Termination styles include right angle or straight solder, wrap pin, or IDC for flat cable use. The three-row units come in standard or reverse mounting styles. Prices for mated pairs in 1000 lots range from \$2.56 to \$3.46 each. **Robinson Nugent, Inc**, 800 E 8th St, New Albany, IN 47150. **Circle 392**

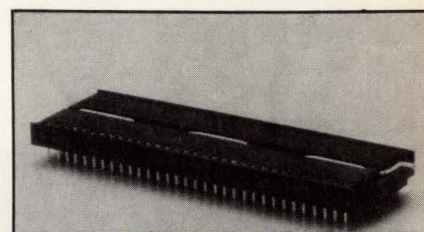
Data link



M25 transmits digital data at rates from dc to 25M bps with a 10^{-9} bit error rate. With a 16-dB system loss budget, transmission lengths greater than 2 km can be obtained. The system can simultaneously transmit an analog signal up to 10 kHz. Two connector systems are available, including Augat's DSC designed to the proposed EIA standards. Price for the data link, without cables, is \$259 in lots of 100. **Augat Inc, Interconnection Systems Div**, 40 Perry Ave, PO Box 1037, Attleboro, MA 02703.

Circle 393

Zero-insertion force socket



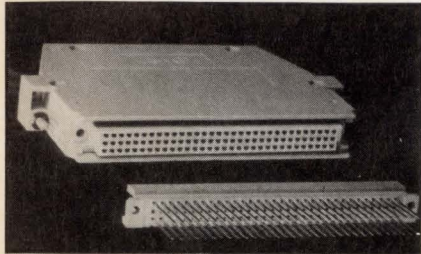
An addition to the Pro-Zif family features a center lever that requires no tools for opening/closing of contacts. The IC is inserted easily into socket body and held in place by rotating the lever 90° to its lock position. Single-facewip contacts on 0.9" (2.3-cm) centers, beryllium copper contacts plated with 30 μm of select gold or 50 μm of tin are provided. Socket meets MIL-S-83734 and is molded of glass reinforced UL94V-0 polyester. The 64-lead Pro-Zif costs \$2.80 each in 10,000 lots. **Wells Electronics, Inc**, 1701 S Main St, South Bend, IN 46613.

Circle 394

Let's hear from you

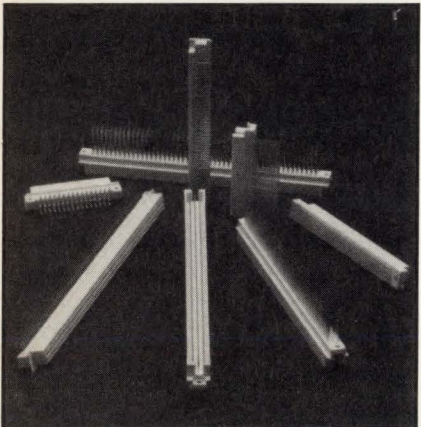
We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

Eurocard connectors



DIN 41612 Eurocard receptacles and headers have a two-part design to improve typical card-edge systems through three-row contact density and a shroud that provides polarized coupling reliability. Family includes two-row standard sex and three-row versions in standard and reverse sex configurations. Glass-filled polyester 94 V-0 housings have a dielectric rating of 1000 Vac between contacts for one minute. PC board mounting options include wrap type posts, solder tails, or compliant pins for solderless pressfit backplane construction. **AMP Inc**, Harrisburg, PA 17105. Circle 395

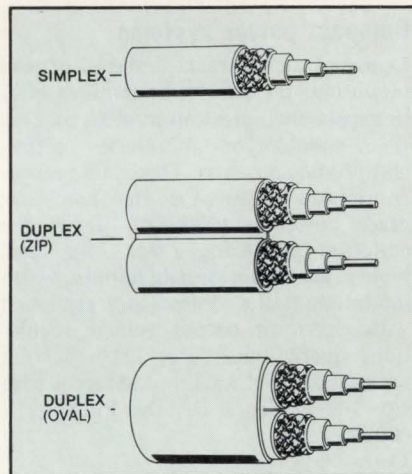
Expanded VG/DIN connectors



VG/DIN connectors with metal-to-metal reliability are available with up to 201 contacts (three rows of 67). In both standard and inverse gender DIN configurations, they feature select plating, low insertion forces, and positive alignment and mating. Connectors meet VG 95324, DIN 41612, and MIL-C-55302 standards. In addition to typical termination options, the inverse expanded DIN is offered in a preassembled compliant pin connector with application tooling. **Elco Corp, Connector Div**, Huntingdon Industrial Park, Huntingdon, PA 16652. Circle 396

Rugged fiber optic cable

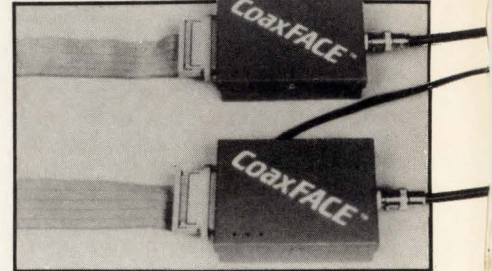
Available in simplex, oval duplex, and zip duplex construction, a plastic clad silica (PCS) fiber optic cable meets the requirements for factory automation and process control applications. Features include low loss optical signal transmission, rfi/emi immunity, high radiation resistance, and higher numerical apertures with simpler termination than communication cable with glass optical fiber. Individual lightguides within



the cable are silicone clad silica core covered with an opaque black buffer to protect the cladding and prevent crosstalk between adjacent lightguides. Cabling adds a tight tube, a braid over the tube, and an overall jacket of PVC or another compound depending on application specs. Attenuation is as low as 8 dB/km at 790 nm. The op temp range is -20 to 80 °C. **EOTec Corp**, 200 Frontage Rd, West Haven, CT 06516. Circle 397

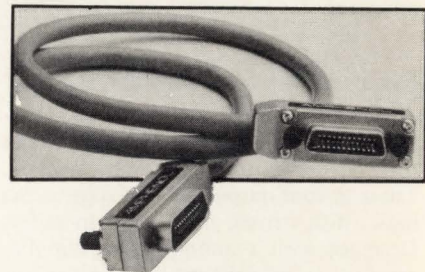
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Coax cable/RS-232 interface



CoaxFACE connecting interface allows use of existing RG-62 coaxial cable to avoid the cost of installing special RS-232 cable. The interface (\$150/pair) connects RS-232-C links and IBM coaxial cable and is an option on the company's 1076, 1071, and 1051 protocol converters. The PCI converter interfaces between an IBM SNA/SDLC host and ASCII CRTs, personal computers, printers, and other devices. CoaxFACE is a connecting link on the ASCII device. Digital pulses are transmitted through the cable 300 to 9600 bps without reducing the RS-232-C data rate. **Protocol Computers, Inc**, 6430 Variel Ave, Woodland Hills, CA 91367. Circle 398

Shielded bus cables



Six connectorized bus cable assemblies feature double-shielded cable, plus added shielding around inner layers to minimize crosstalk between control and data lines. The 488 series assemblies have reduced overall rfi levels to meet or surpass MIL-STD-461A, VDE 0871, and VDE 0875. Typical cable capacitance is 120 to 130 pF/m. The cables are terminated with 24-contact Amphenol 57 series rack and panel connectors. Features include die-cast nickel plated aluminum shell that resists corrosion, provides added shielding, and has an overlapped seam for enhanced ground/shielding. Price range is \$35 to \$97. **Amphenol, div of Allied Electronic Components Co**, 2122 York Rd, Oak Brook, IL 60521. Circle 399

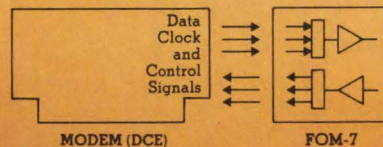
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Plus a whole lot more.

- Can also be used for standard modem applications
- Automatically accepts or supplies DCE/DTE clocks
- Fully supports all EIA handshaking signals
- Provides secondary data channel

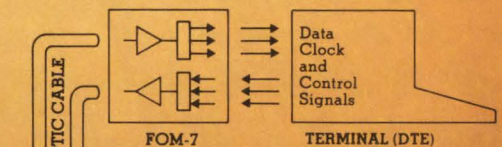
In short, you can use our new fiber optic modem between any two plug compatible units in your local area network. And it won't require any jury-rigging or looping clock and interface signals. That's because, from an operating standpoint, our fiber optic modem looks just like an EIA cable; whether you're going from a long-haul

modem to a remote terminal or from a CPU port to a printer. And it's just about as easy to install as a cable — we even provide two separate connectors (DTE and DCE) on each modem. YOU determine how our modem will function simply by selecting which connector you use!



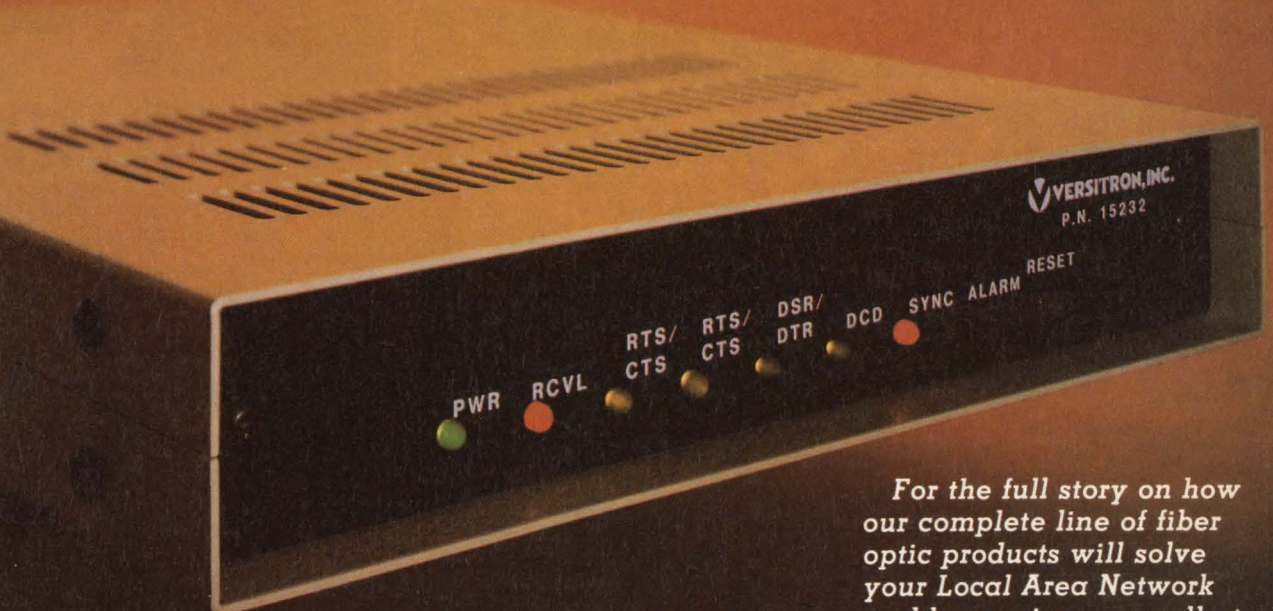
Once our fiber optic modem is installed and operating it'll really begin to shine. You'll benefit not only

from the advantages inherent with fiber optics (traffic security plus noise immunity) but also from the exceptional operating performance. Our very low error



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Versitron manufactures a complete line of fiber optic products for Local Area Networks. Our 20 years' experience in fiber optic is reflected in the performance capabilities of our products.



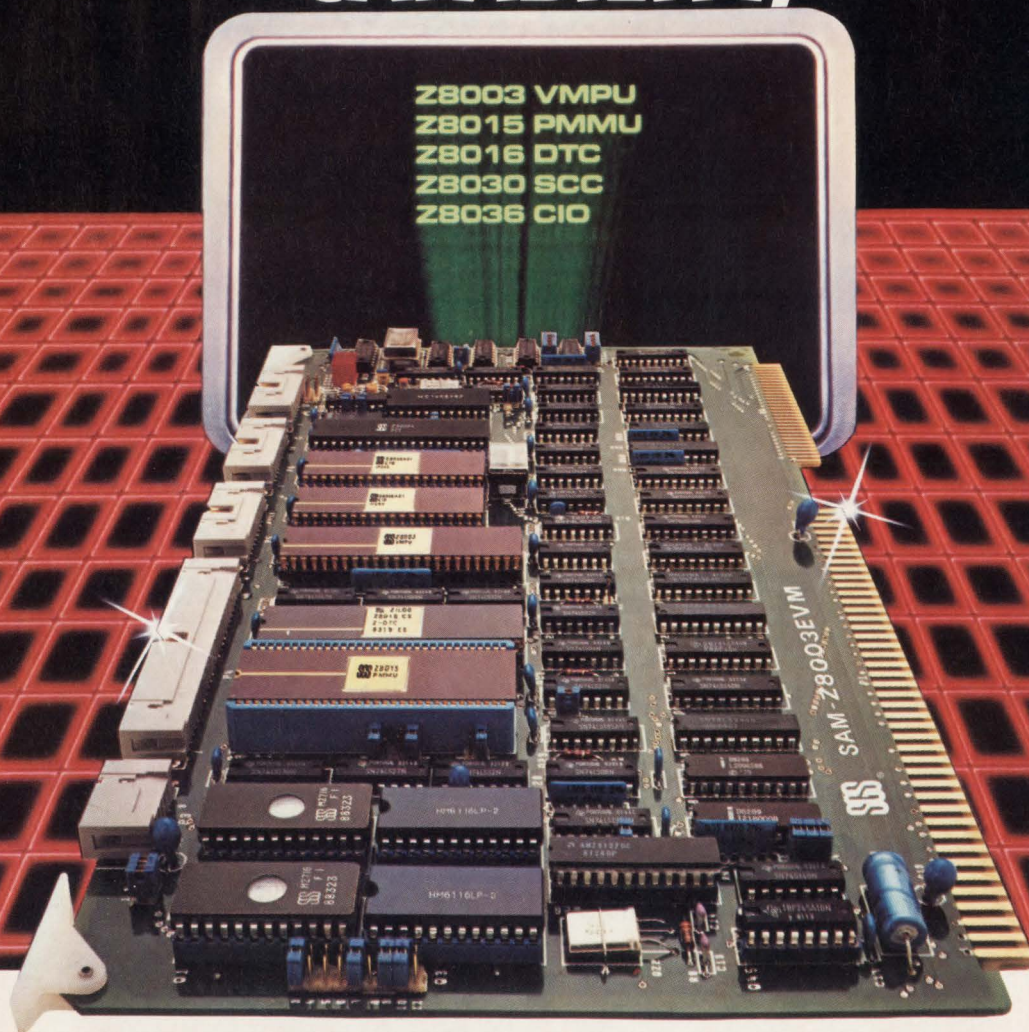
For the full story on how our complete line of fiber optic products will solve your Local Area Network problems, give us a call at (202) 882-8464. Or write:

VERSITRON, INC.

6310 Chillum Place, N.W., Washington, D.C. 20011, TWX: 710-822-1179

CIRCLE 111

MAINFRAME VIRTUAL MEMORY CAPABILITY,



Z8003 VMPU
Z8015 PMMU
Z8016 DTC
Z8030 SCC
Z8036 CIO

FOR THE PRICE OF ONE BOARD!

The SGS Advanced Modules now offers you single-board virtual memory capability previously available only on large mainframes. In fact, our new SAM-Z8003EVM is a complete IEEE 796-Multibus microcomputer designed to help you evaluate and develop the 16-bit Z8003 VMPU, Z8015 PMMU and other Z8000™ family devices. Just connect it to a standard terminal or a host computer through an RS-232C port. You're ready to design!

Multibus™ and SAM-BUS™ Architecture allows total flexibility and expandability to the other SAM's.

Top-performance on-board features include: Z8003 Virtual Memory Processor Unit (VMPU); Z8015 Paged Memory Management Unit (PMMU); Z8016 DTC (optional); Z8030 SCC; Z8036 CIO; 4K bytes static RAM; CMOS clock and calendar chip.

SAM and SAM-BUS are trademarks of SGS Semiconductor Corporation.

Built-in hardware and software debugging aids include cycle and instruction single-step. A resident monitor program allows interface and control of all programmable devices on the board.

If you want mainframe virtual memory capability and all the power of the new Z8003 CPU, at a virtually unheard of price, contact the SGS sales office nearest you, today!

Sales Offices: Atlanta, GA (404) 446-8686; Boston, MA (617) 890-6688; Chicago, IL (312) 490-1890; Dallas, TX (214) 733-1515; Indianapolis, IN (317) 241-1116; Irvine, CA (714) 863-1222; Long Island, NY (516) 435-1050; Los Angeles, CA (213) 716-6600; Phoenix, AZ (602) 867-6245; San Francisco, CA (408) 727-3404; Sao Paulo, Brazil (11) 647-245.



Franchised distributor: **WYLE** ELECTRONICS MARKETING LABORATORIES GROUP

Multibus is a trademark of Intel Corp.

Technology and Service

CIRCLE 112

CONFERENCES

JAN 17-19—Mini/Micro-Southeast, Orange County Convention and Civic Ctr, Orlando, Fla. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

JAN 17-19—Southcon, Orange County Convention and Civic Ctr, Orlando, Fla. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

JAN 31-FEB 2—Communication Networks Conf & Exposition, Washington Convention Ctr, Washington, DC. INFORMATION: Judie McDaid, Hajar Assocs, 280 Hillside Ave, Needham Heights, MA 02194. Tel: 617/444-3946

FEB-MAR—Invitational Computer Confs (European Series), Stockholm, Sweden; Paris, France; Munich, West Germany; Frankfurt, West Germany; and London, England; various dates. INFORMATION: Susan Fitzgerald, B. J. Johnson & Assocs, Inc, 3151 Airway Ave, Suite C-2, Costa Mesa, CA 92626. Tel: 714/957-0171

FEB 20-22—Office Automation Conf, Los Angeles, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

FEB 21-23—Softcon, Superdome, New Orleans, La. INFORMATION: Peggy Kilburn, Northeast Expositions, 822 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000; 800/343-2222 (outside Mass)

FEB 22-24—ISSCC (IEEE Internat'l Solid-State Circuits Conf), San Francisco, Calif. INFORMATION: Lewis Winner, 301 Almeria, Coral Gables, FL 33134. Tel: 305/446-8193

FEB 22-28—Imprinta (Internat'l Congress and Exhibition for Communications Techniques), Dusseldorf, West Germany. INFORMATION: Borman/Williams Inc, 222 Park Ave S, New York, NY 10003. Tel: 212/254-5400

FEB 28-MAR 1—Comcon/Spring, Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

MAR 12-15—Interface, Las Vegas Convention Ctr, Las Vegas, Nev. INFORMATION: Richard Katzeff, The Interface Group, Inc, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600; 800/325-3330 (outside Mass)

MAR 12-16—Internat'l Conf on Robotics, Atlanta Hilton, Atlanta, Ga. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

MAR 19-21—Phoenix Conf on Computers and Communications, Phoenix Hilton, Phoenix, Ariz. INFORMATION: David Gretton, Digital Equipment Corp, 2500 W Union Hills Dr, Phoenix, AZ 85027. Tel: 602/869-5273

MAR 26-30—Internat'l Conf on Software Engineering, Orlando, Fla. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

APR 2-5—Test & Measurement World Expo, Brooks Hall, San Francisco, Calif. INFORMATION: Meg Bowen, Interfield Publishing Co, 215 Brighton Ave, Boston, MA 02134. Tel: 617/254-1445

APR 4-11—Hannover Fair, Hannover, West Germany. INFORMATION: Delia Assocs, PO Box 338, Whitehouse, NJ 08888. Tel: 201/534-9044; 800/526-5978 (outside NJ)

APR 9-12—Powercon, Loew's Anatole Hotel, Dallas, Tex. INFORMATION: Ed Grazda, Power Concepts, Inc, PO Box 5226, Ventura, CA 93003. Tel: 805/656-1890

APR 10-12—Infocom, Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

APR 18-20—Optical Data Storage, Monterey Convention Ctr, Monterey, Calif. INFORMATION: Optical Society of America, 1816 Jefferson Pl NW, Washington, DC 20036. Tel: 202/223-8130

APR 24-27—Compdec (Internat'l Conf on Data Engineering), Bonaventure Hotel, Los Angeles, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

APR 30-MAY 2—Workshop on Computer Vision, Hilton Hotel, Annapolis, Md. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

MAY 13-17—Computer Graphics, Anaheim Convention Ctr, Anaheim, Calif. INFORMATION: National Computer Graphics Assoc, 8401 Arlington Blvd, Fairfax, VA 22031. Tel: 703/698-9600

MAY 14-17—Internat'l Conf on Communications, Congresscentrum Rai, Amsterdam, The Netherlands. INFORMATION: K. Teer, Philips Research Lab, 5600 MD Eindhoven, The Netherlands.

MAY 14-17—Internat'l Conf on Distributed Computing, Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

MAY 15-17—Electro, Bayside Exposition Ctr and Hynes Auditorium, Boston, Mass. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

MAY 15-17—Mini/Micro-Northeast, Hynes Auditorium, Boston, Mass. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

JUNE 5-7—Internat'l Symposium on Computer Architecture, Rackham Building, Ann Arbor, Mich. INFORMATION: Keki Irani, ECE Dept, Univ of Michigan, Ann Arbor, MI 48109. Tel: 313/764-8517

JUNE 5-7—Symposium on Mass Storage Systems, Marriott Mark Resort, Vail, Colo. INFORMATION: Bernard O'Lear, NCAR, PO Box 3000, Boulder, CO 80307. Tel: 303/494-5151

Announcements intended for publication in this department of *Computer Design* must be received at least three months prior to the date of the event. To ensure proper timely coverage of major events, material should be received six months in advance. Programs and dates are subject to last minute changes.

10th ANNIVERSARY
SPECIAL OFFER

\$3,995*



Intecolor VHR-19 challenges Tektronix® with 1024 x 1024 resolution, PLUS COLOR, and at less than half the price!

Comprehensive Graphics Capabilities: 1024 x 1024 workspace; 1024 x 768 displayable; 4096 x 4096 virtual addressing for extended Tektronix 4014 compatibility. High-level graphics primitives, including polygon fill. Bit-mapped 19" screen. Three dot-addressable bit planes. Separate alphanumeric plane. Hardware pan and zoom. Expanded peripheral support. Simple menu set-up. Host programmable function keys.

Fast Response: 2.5 million pixels/sec. direct screen memory access port.

Industry Standard Protocol: ANSI X3.64/VT100 command protocol.

Compatibility: VT100, TEK 4010/4014/4014-1 and enhanced Intecolor 8001R.

Raster Color: Palette of 4,096 colors, 8 concurrently displayable.

Advanced Processor Design: Three graphics processors (7220D-1); separate alphanumeric processor; plus terminal processor (Z80) and keyboard processor.

*100-piece OEM price and single-unit introductory price through 12-31-83; includes color monitor, graphics display processor and keyboard. Trackball is optional at \$330. U.S. Domestic prices.

From the same company that pioneered the world's first micro-processor-based color terminal (Intecolor 8000) way back in 1973. And the same company that continually leads the color graphics industry with new product innovations. NOW, a bold, new addition to the fastest growing area of the industry: *Intecolor VHR-19 high resolution graphics workstation.*

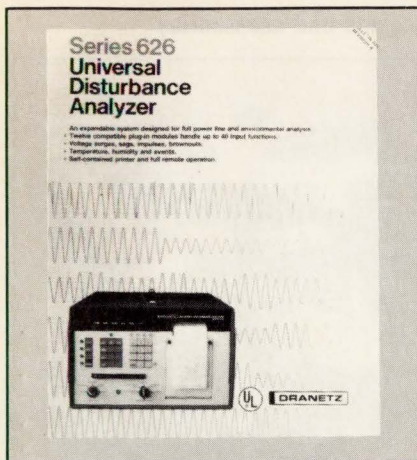
If you need more than a graphics preview terminal, but less than a turnkey CAD system, the VHR-19 delivers an unprecedented price/performance ratio. With an advanced design graphics display processor. With fine image detail and high-level resolution.

And, with an introductory, single package price of \$3,995. Unbeatable.

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Norcross, GA 30092, 404/449-5961, TWX 810-766-1581

Power/environmental monitors



Brochure examines how modular series 626 analyzes power line disturbances and computer room temperature/humidity, as well as how remote monitor units cover several sites simultaneously. **Dranetz Technologies, Inc.**, Edison, NJ. **Circle 410**

Image processing systems

Data sheets summarize several image processing alternatives. Descriptions of features, specs, and options accompany functional block diagrams of IP8500, IP6400, and FD5000 image processing systems; auxiliary graphics processor; realtime 300-Mbyte modified Winchester disk; and LIPS V 3.0 software library. **Gould Inc, DeAnza Imaging & Graphics Div.**, San Jose, Calif. **Circle 411**

Fail-safe brakes

Technical brochure profiles 1-, 3-, 7-, and 50-in-lb torque models of SBF series fast-response Silent Stop brakes. **Vernitech, div of Vernitron Corp.**, Deer Park, NY. **Circle 412**

Thin power supplies

Brochure gives diagrams and charts accompanied by technical and application data for the ESK series of dual-input 110/220-Vac low profile power supplies, which meet UL/CSA/VDE regulations. **KSC Electronics, Inc.**, Arlington Heights, Ill. **Circle 413**

Ferrite products

Bulletin lists dimensions, properties, and frequency characteristics of Ceramag products for power supplies/filters, CRT displays, emi suppression, and other electronic applications. **Stackpole Corp, Ferrite Products Div.**, St. Marys, Pa. **Circle 414**

Unix documentation

Technical documents and manuals for Unix include transitional aids for moving from System III to System V; user's manual listing commands, system calls, and subroutines; and an error message manual. **Western Electric**, New York, NY. **Circle 415**

Interface data book

Combined reference for bipolar LSI, bipolar memory, and programmable logic contains 25 application notes, as well as cross-reference information for replacement devices. Request (\$12 per issue) on company letterhead from: **National Semiconductor Corp.**, M/S 14-208, 2900 Semiconductor Dr., Santa Clara, CA 95051.

High speed CMOS logic

Reference to MC54/74HC family presents design considerations, device specs, and reliability data; function selector guide lists features for each of the 147 devices under 15 logic categories, with block diagrams for each. **Motorola Inc, MOS Integrated Circuits Group.**, Austin, Tex. **Circle 416**

Plasma/CRT display comparison

Article reviews operating principles of CRT and ac plasma displays, and evaluates physical properties, inherent memory, drift, and reliability of each. Diagrams show flat-panel construction and compare size of CRT tube and Plasmascope display. **SAI Technology Co.**, San Diego, Calif. **Circle 417**

Machine vision

Technical specs bulletin outlines ERMAC 2570 PC board inspection system, detailing features and operational procedures. **Everett/Charles Automation Systems Inc.**, Pomona, Calif. **Circle 418**

Revised PAL handbook

Third edition presents specs for full line of programmable array logic circuits and designs for over 50 applications. **Mono-lithic Memories, Inc.**, Santa Clara, Calif. **Circle 419**

Data communication equipment

Catalog highlights over 300 communication and computer support products; descriptions include specs, diagrams, photos, and ordering information. **Black Box Corp, a Micom Co.**, Pittsburgh, Pa. **Circle 420**

Integrated circuit index

One-volume desk reference cites cartridge and frame microfilm references to technical data sheets for about 50,000 circuits from nearly 450 manufacturers; major sections contain indexes by manufacturer's type number, original circuit number, and function. **Information Handling Services**, Englewood, Colo. **Circle 421**

Standard logic boards

Brochure illustrates 14 high density, bus compatible models having single and dual 68-pin JEDEC type A leadless chip carrier sockets; complete specs, dimensions, single/dual-voltage plane option, and optional accessories are described. **Methode Electronics, Inc, Logic Board Div.**, Chicago, Ill. **Circle 422**

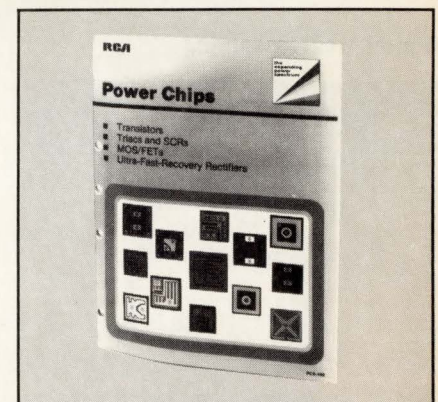
Thermocouple/sensor interface

Handbook describes computer interfaces and peripherals that link process functions to computers or microprocessor-based instruments; tutorial and glossary accompany product photos and specs. **Omega Engineering, Inc.**, Stamford, Conn. **Circle 423**

Technology trends

Bimonthly publication, *Solutions*, considers evolving applications and markets of VLSI, component systems, and software. **Intel Corp.**, Santa Clara, Calif. **Circle 424**

Power chips and wafers



Brochure specifies over 200 solid state power devices, such as MOSFETs, transistors, rectifiers, Darlingtons, and triacs; technical information includes process identification, chip dimensions, recommended assembly procedures, critical characteristics, and various device types deriving from each chip. **RCA/Solid State Div.**, Somerville, NJ. **Circle 425**

Telecommunication connectors

Booklet specifies Bantam jacks and accessories, and longframe products; photos, dimensional diagrams, and circuit configurations are included. **ADC Magnetic Controls Co**, Minneapolis, Minn.

Circle 426

Microelectronics guide

Technical literature features specs and brief functional descriptions of ROM, electrically erasable PROM, microcomputer, audio, video, data communications, and semicustom microcircuits. **General Instrument, Microelectronics Div**, Hicksville, NY.

Circle 427

Electronic wire and cable

Eighty-page catalog details construction, characteristics, and applications of various computer cables; over 7000 standard wire types are described. **Consolidated Electronic Wire & Cable**, Franklin Park, Ill.

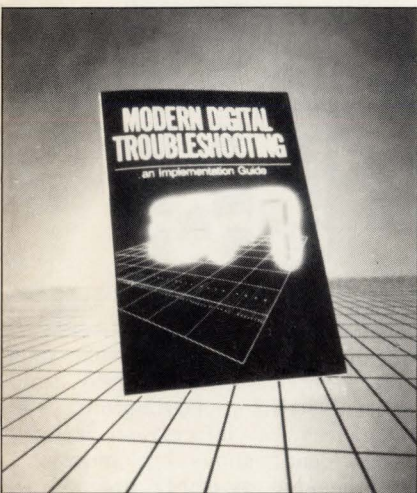
Circle 428

Optoelectronic components

Product reference highlights features, applications, and specs of phototransistors and photodarlington, photodiodes, light activated switches, photoswitches, infrared LEDs, and various optoisolators. **Vatec Inc**, St. Louis, Mo.

Circle 429

Digital troubleshooting



Guidebook explains signature verification method and its role in fault isolation. **Data I/O Corp**, Redmond, Wash.

Circle 430

Shielding wire and cable

Tutorial shows how to apply federal emi/rfi shielding regulations to computer wire and cable design; text describes and compares FCC Docket 20780, Tempest, and MIL-STD-461B guidelines and interprets them for specifying cable. **Mercury Wire Products, Inc**, Spencer, Mass.

Circle 431

Achieving plotter accuracy

Application note defines accuracy, interprets the accuracy specification, and suggests guidelines for maintaining it in an operating environment. **Hewlett-Packard Co**, Palo Alto, Calif.

Circle 432

Intelligent display modules

Eight-page booklet detailing Optel LCDs provides dimensions, specs, font table, interface connections, absolute maximum ratings, timing/electrical characteristics, and instruction codes. **REFAC Electronics Corp**, Winsted, Conn.

Circle 433

Switches and relays

Engineering catalog profiles wide range of rugged, tamper-proof mechanisms; complete specs, selector charts, circuit configurations, dimensional diagrams, and photos complement text. **Grayhill, Inc**, La Grange, Ill.

Circle 434

Data conversion components

A 376-page catalog contains complete technical information for a line of monolithic, hybrid, and modular products; function/performance tables accompany data. **Datel-Intersil**, Mansfield, Mass.

Circle 435

Subminiature coaxial cable

Folder gives electrical and mechanical characteristics of RG59 and RG62, which provide from 1 to 60 cables in each jacket; also described are accessory tools and connectors. **Computer Cable and Products, Inc**, Farmingdale, NY.

Circle 436

Micro-based CPU card

Four-page brochure details the CPU-100, a 6502-based CPU card designed for high speed STD-bus applications; electrical/mechanical specs, features, functions, and pin configurations are highlighted. **Techno Inc**, Pompton Lakes, NJ.

Circle 437

Sockets and accessories



Catalog covers IC sockets for single- and dual-beam DIPs, pin grid arrays, and VLSI leadless chip carriers; each socket description comes with a photo and cut-away drawing indicating design features, dimensions, and tolerances. **Augat Inc**, Attleboro, Mass.

Circle 438

Controlling emi

"Guide to Interference Control Using Beryllium Copper" discusses design and technology of effective emi shielding; technical data covers new assemblies for grounding high voltage static discharge with discrete contact points. **Instrument Specialties Co, Inc**, Delaware Water Gap, Pa.

Circle 439

Economical RS-232 interfaces

Eight-page booklet describes a range of interface options, including switches, printer buffers, data cables, and line boosters; diagrammed application information, technical specs, and prices are also covered. **Western Telematic Inc**, Santa Ana, Calif.

Circle 440

Multilayer ceramic capacitors

Catalog of military-qualified DIPs lists part numbers, failure rate levels, capacitance, capacitance tolerance, and dc rated voltage; also included are substitutability data and typical curves showing dielectric characteristics. Companion catalog lists qualified leadless components. **San Fernando Electric Technologies**, San Fernando, Calif.

Circle 441



Nice move, IBM.®

Well, IBM claims yet another first.

By offering the p-System™ on their Displaywriter and PC, it becomes the *only* operating system they market for both. They obviously know a good thing when they see it.

But then so did Apple®, Commodore, Corvus,™ TI, Digital, HP, Osborne,™ Philips, Sage®, Zenith, NEC, and Olivetti, for that matter.

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IBM did. And how often do *they* make a bad move?

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We use a conventional SMD interface.

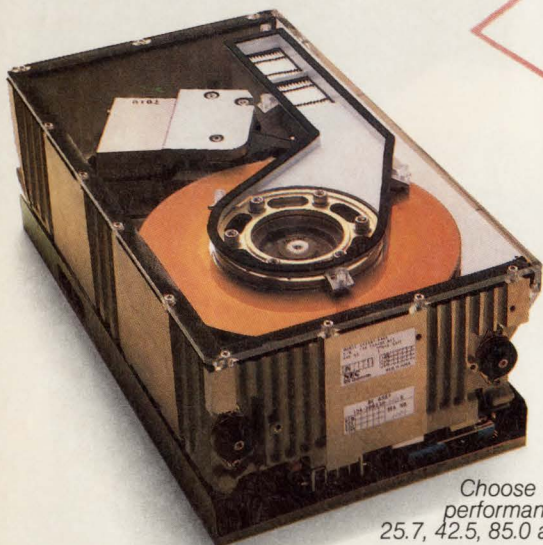
So our drives are easy to use.

It's simple to integrate NEC's 8-inch Winchester drives into your system. The reason is our standard Storage Module Device (SMD) type interface.

In addition, you wind up with significant savings in installation, packaging, maintenance and cost-of-ownership.

NEC. Technology drives us.

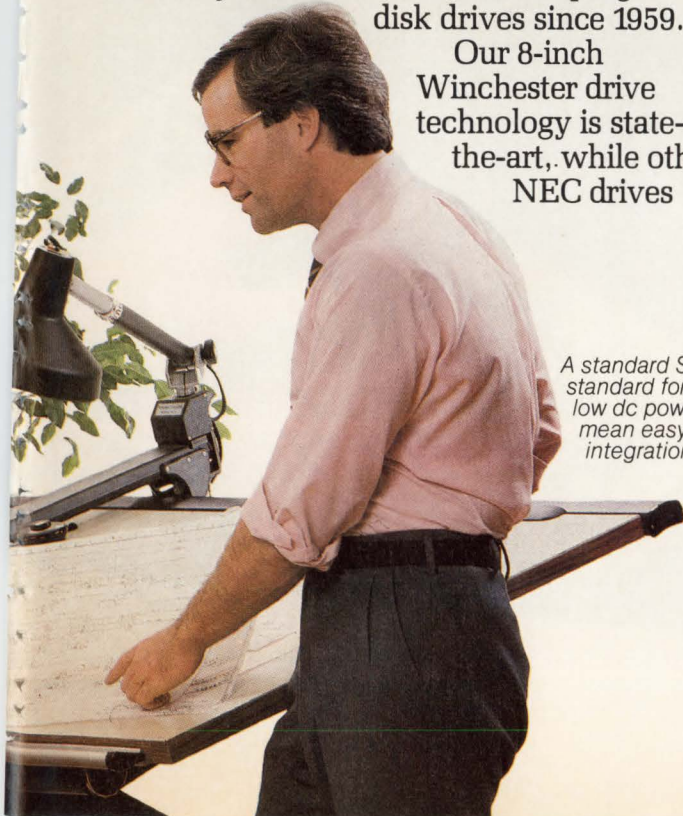
NEC has been pioneering advancements in electronics for



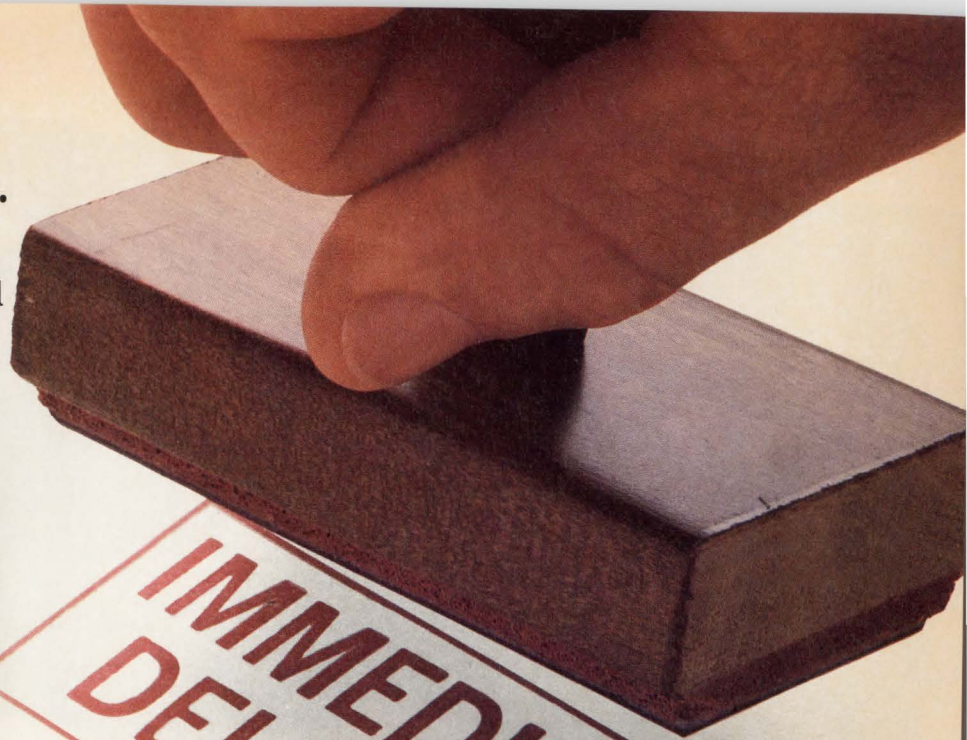
Choose from four high performance capacities: 25.7, 42.5, 85.0 and 167.7 MB.

almost 85 years. We've been developing disk drives since 1959.

Our 8-inch Winchester drive technology is state-of-the-art, while other NEC drives



A standard SMD interface, standard forms factor and low dc power requirements mean easy system integration.



IMMEDIATE DELIVERY

An evaluation unit will be shipped within 72 hours from the time your PO is received.

incorporate such advanced technology as plated media, thin-film heads and optical recording.

Clearly, NEC remains at the leading edge.

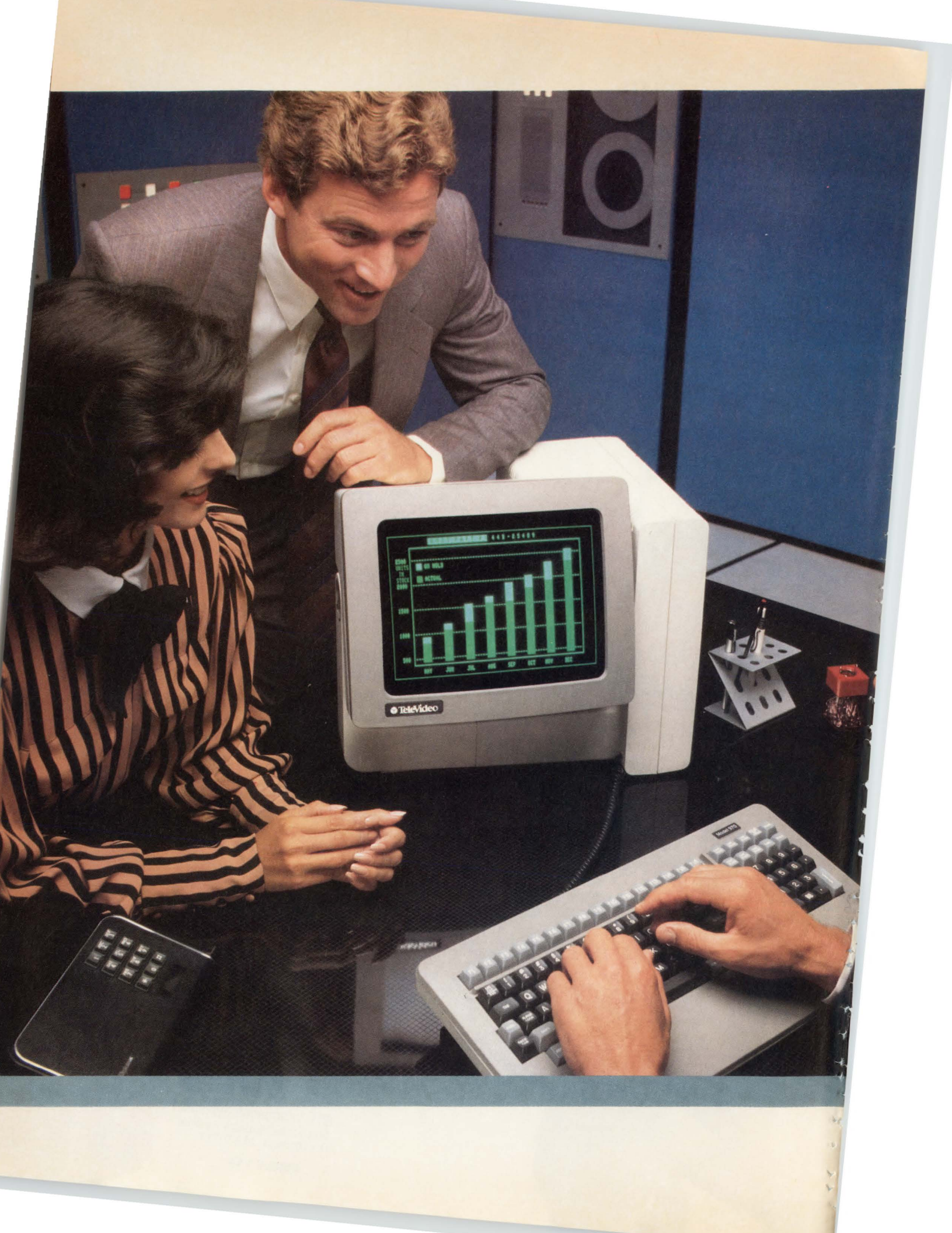
For more information on NEC 8-inch and 5 $\frac{1}{4}$ -inch Winchester and flexible drives, or the name of your nearest NEC representative, call 1-800-343-4418 (In Massachusetts, call 617-264-8635). You'll find out why more and more OEM's are saying "NEC and me."

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AND
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NEC Information Systems, Inc.
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Boxborough, MA 01719

CIRCLE 115





TELEVIDEO'S 970: GET IN ON THE ANSI BOOM.

The TeleVideo 970 Terminal. The computer professionals' most powerful ticket to the emergence of the ANSI standard.

The overwhelming acceptance of ANSI X3.64 has revolutionized the future of trans-system communication and software compatibility. Now TeleVideo steps forward with the ultimate complement to that revolution. The ANSI equipped TeleVideo 970 terminal.

The 970 takes the lead in utilizing the advantages of the ANSI code structure. Its 32 non-volatile function keys literally automate ANSI code command entry. Other features include VT-100 compatibility, block mode operation, block graphics and attributes and a totally reconfigurable keyboard. An RS232 printer port with built-in buffer is standard. All this is packaged in the 970's unique vertical convection cooling tower. It protects sensitive circuitry without the noise of conventional fan-cooled construction.

In terms of operator comfort the 970 has no equal. The keyboard with ten-key accounting pad is ergonomically designed with a naturally contoured palm rest and sculpted keys. The non-glare 14 inch screen allows maximum readability in either the 80 or 132 column format. And you can display double-high, double-wide characters on the same fatigue-free background we've been applauded for throughout the industry. Screen tilt adjusts at a touch to further fight operator discomfort.

Of course, as with all TeleVideo terminals, 970 service is available nationwide from General Electric Instrumentation and Computer Service Centers.

The 970. A combination of power, ease of use and TeleVideo reliability at a time you need it most. The ANSI boom is here. Get in on it with the TeleVideo 970.


Call us at 800-538-8725 for more information (in California call 408-745-7760) or contact your nearest TeleVideo office:

California/Santa Ana	714-557-6095
California/Sunnyvale	408-745-7760
Georgia/Atlanta	404-399-6464
Illinois/Chicago Area	312-351-9350
Massachusetts/Boston	617-668-6891
New York/New Jersey	201-267-8805
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GET IN ON THE BOOM.™



TELEVIDEO® TERMINALS

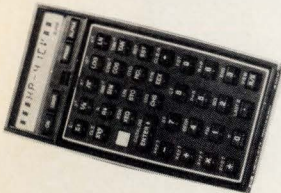
 TeleVideo Systems, Inc.

YOUR ANSWERS TO THESE QUESTIONS HELP US SERVE YOU BETTER

YOUR ANSWERS ARE IMPORTANT. The results of these surveys help our editors select topics, features and technical data that will be on target with your design activities. Your inputs also alert manufacturers to your needs and can result in the development of product speeds, ranges, capacities, and other specs that you require.

YOUR ANSWERS CAN ALSO WIN YOU A VALUABLE PRIZE!

Each questionnaire returned gives you a chance to win a special prize. Drawings are made after each issue, with a grand prize drawing at year end.



MONTHLY DRAWING — HP 41CV PROGRAMMABLE CALCULATOR

The HP 41CV offers advanced problem-solving power yet is easy to use. Communicates in words as well as numbers. Can be programmed to meet your specific needs. Fifty-eight popular functions, 130 total functions in program library. Memory expandable to almost 6,500 bytes.



ANNUAL DRAWING — HP 85 DESK TOP COMPUTER

This portable (20 lb.) unit includes an alphanumeric keyboard, tape drive, thermal printer, built-in 56K byte memory, CRT screen, and 150 built-in BASIC language commands. You can add peripheral and software packages to expand system capability. A \$2800 value!



A wider range of streamers you cannot get...

not with IBM format compatibility and over 40% common components.

Now, for the first time, there's a family of high quality 1/2 inch streaming tape drives to match almost every need and budget. We simply ask you to compare them with ordinary streamers and then make your choice from the world's smallest 1/2" machine our 9800, the high capacity low profile 9900, or the high performance 8900.

No worries about the future either. Plan now to meet your immediate needs, extend later to higher densities and capacities.

Compare these innovations, many unique, and all common to the THORN EMI streamer family. Then compare the price:-

- IBM/ANSI/ECMA 9-track formats
- Multi-mode, multi speed operation
- Autoloading on 9900 and 9800
- Maximum unformatted capacities, based on thin based tapes; 34.5 M bytes (9800) 138 M bytes (9900, 8900)
- 25, 50 and 100 ips streaming.
- 50 ips genuine start/stop-(8900)
- 1600 bpi and double density 3200 bpi PE
- 800 bpi NRZ (8900)
- 3-level diagnostics, operator and remotely controlled
- Unambiguous scrolled alphanumeric display
- 8 registers for status and error logging
- Common operator control sequences
- UL, CSA, VDE, FCC, BS & IEC Safety and RFI standards
- Spare pcb slot for cache memory, serial, parallel or user special interface
- Plug-in optimum sized pcb's
- Industry standard interfaces
- Integral power unit



**THORN EMI
Technology Inc.**

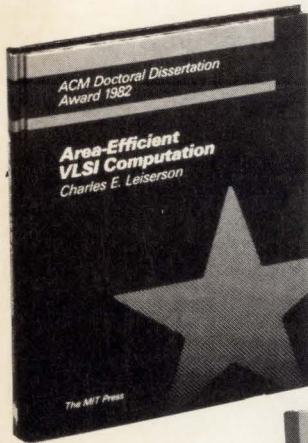
Computer Products, 8601 Dunwoody Place, Atlanta GA 30338
Tel: (404) 587-0017 Telex: 810-7662267.

REST OF WORLD: THORN EMI DATATECH LTD. Spur Road, Feltham,

CIRCLE 118

AREA-EFFICIENT VLSI COMPUTATION

by Charles E. Leiserson



The microelectronics revolution has obliterated the traditional distinctions between hardware and software. The complexity of very large scale integrated (VLSI) circuits has become so great that each integrated circuit chip is a complicated system. The award-winning research reported in this book shows how techniques of algorithm design, which are usually applied to software programs, can be applied directly to the design of VLSI systems. 136 pages, 41 illus., \$22.50

Circle 456

IMS PROGRAMMING TECHNIQUES

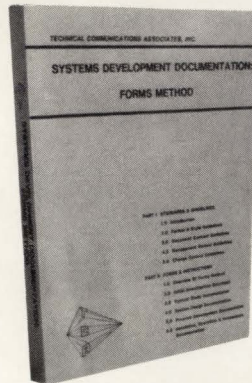
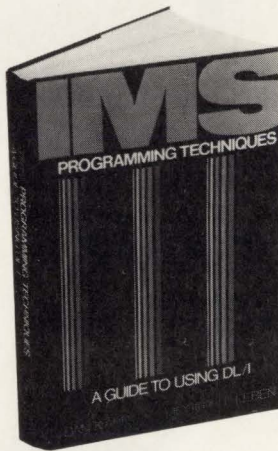
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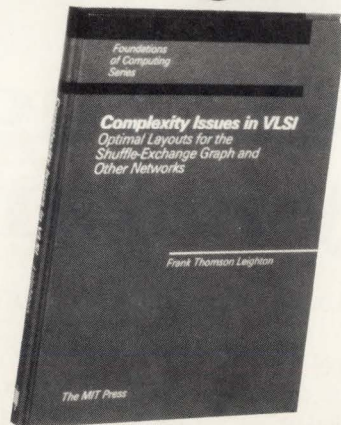
SYSTEMS DEVELOPMENT DOCUMENTATION: Forms method

By Technical Communications Associates, Inc.

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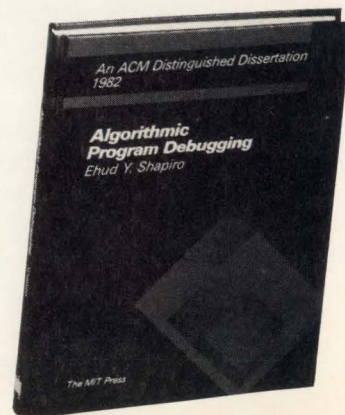
ALGORITHMIC PROGRAM DEBUGGING

by Ehud Y. Shapiro

This book formulates and explores a potentially productive new subarea of computer science that combines elements of programming languages and environments, logic, and inductive inference. It devises a theoretical framework for program debugging and develops techniques that will partly mechanize this activity. In particular, it formalizes and validates algorithmic solutions to finding and then fixing program bugs.

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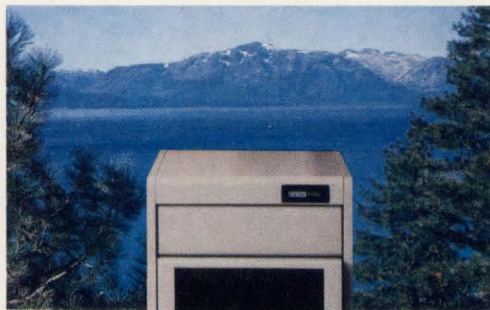
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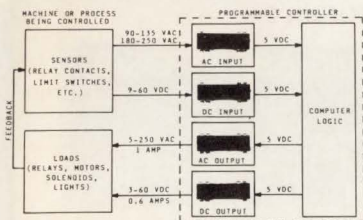
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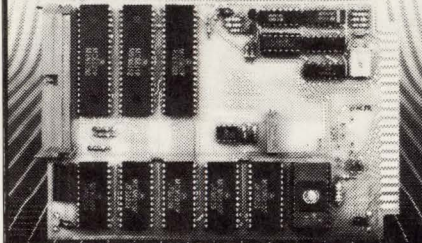


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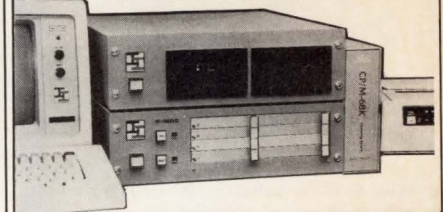
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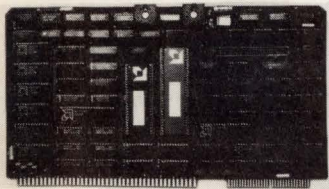


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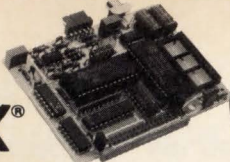
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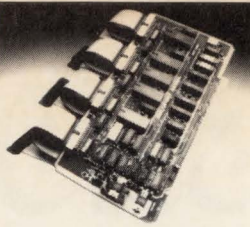
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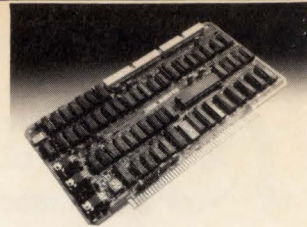


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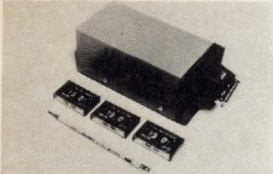


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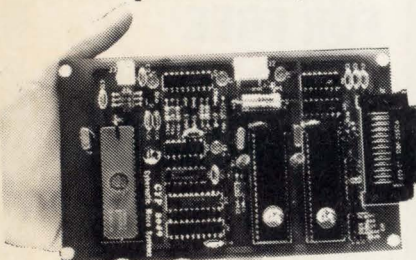
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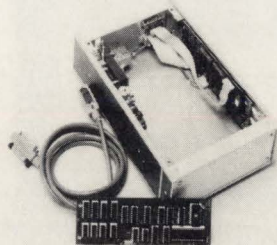
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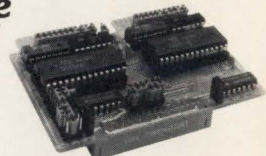
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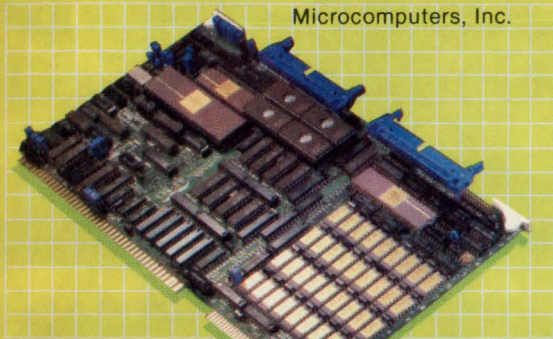
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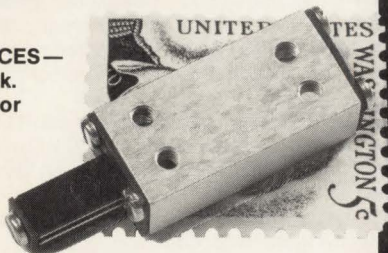
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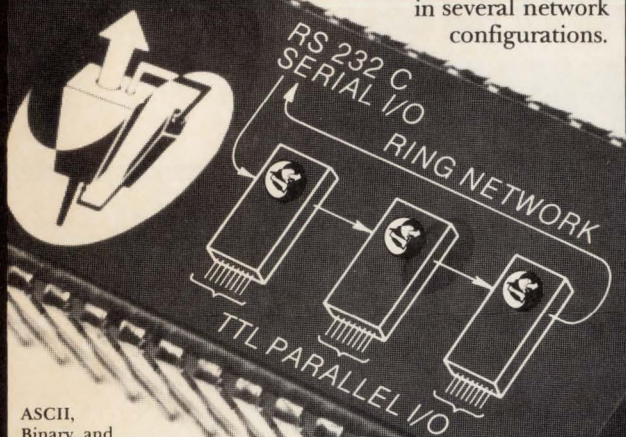
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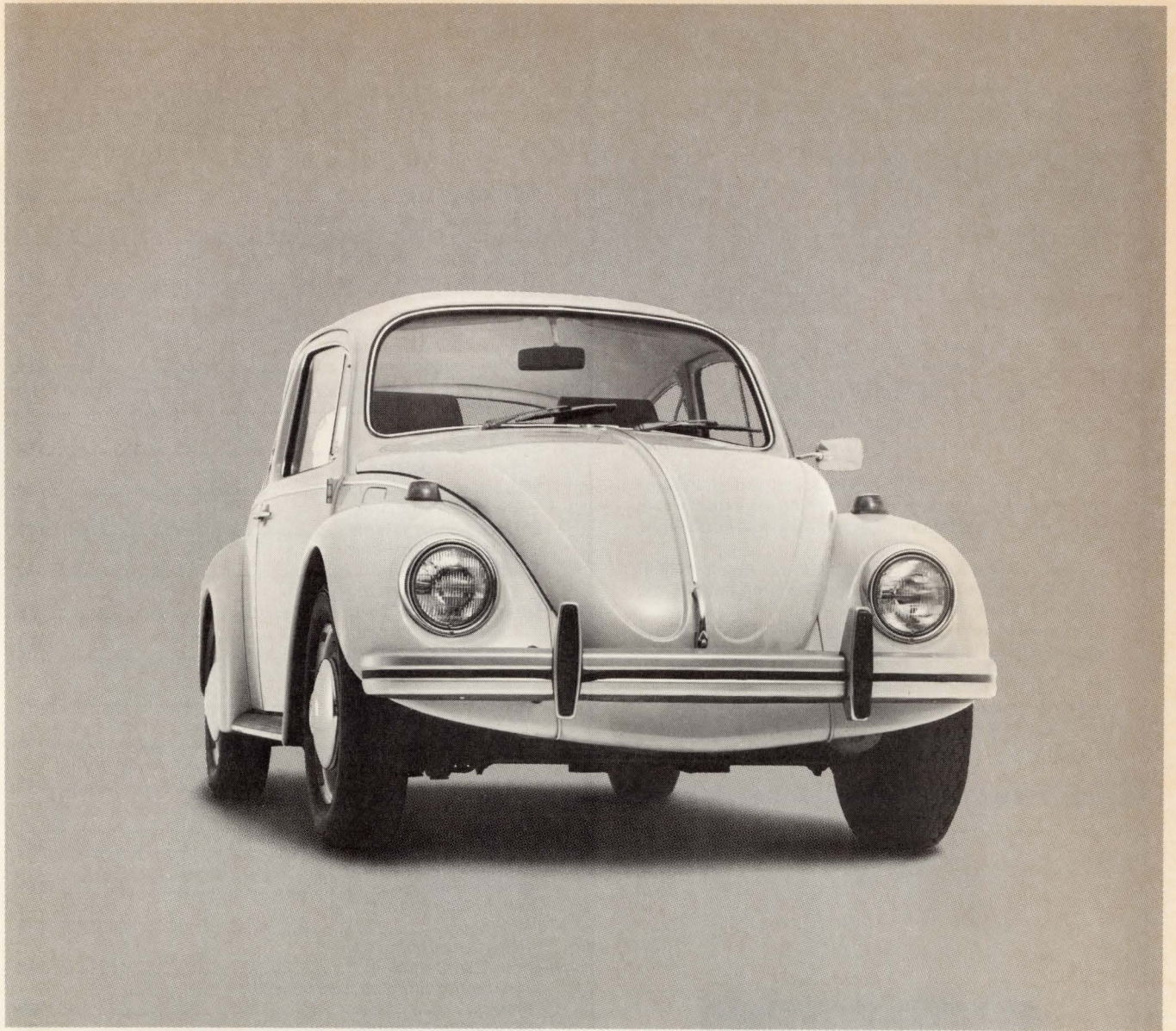
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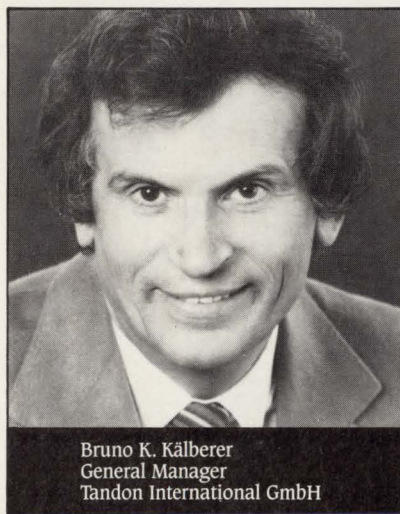
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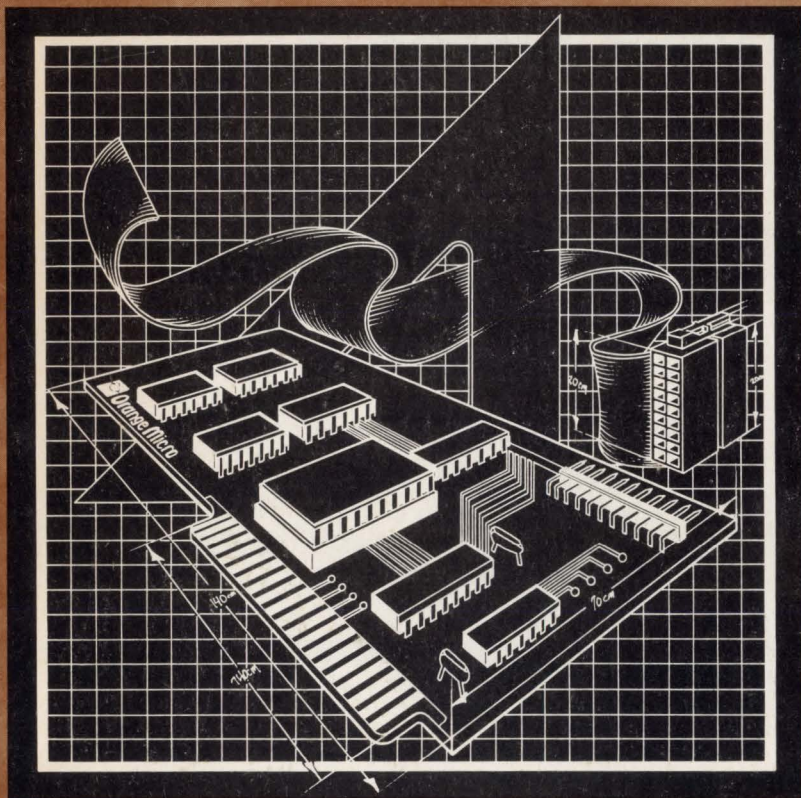
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