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JUNE 1, 1984

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

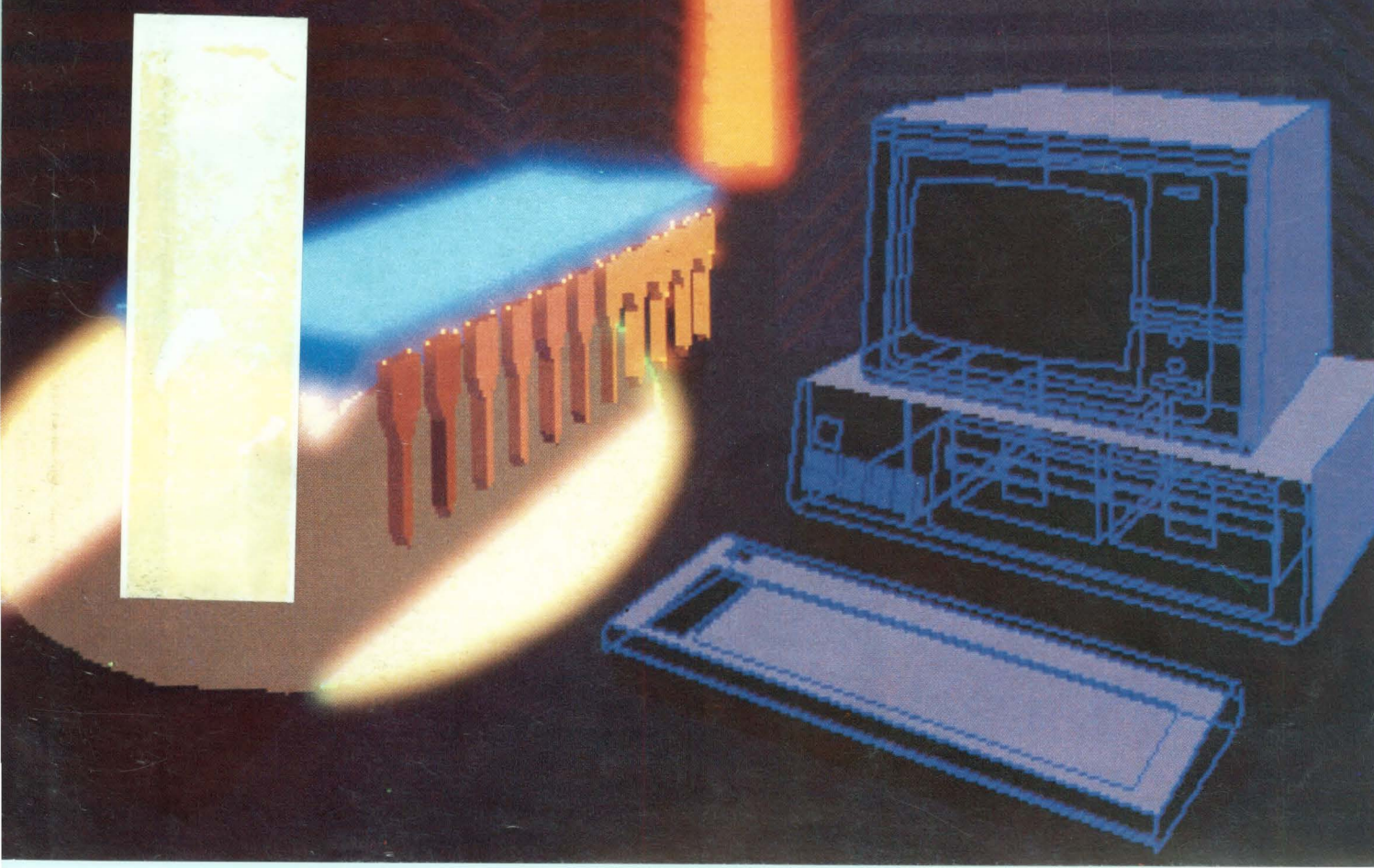
SPECIAL REPORT ON MICROSYSTEMS

EMERGING 32-BIT MICROPROCESSORS

LOCAL AREA NETWORK ADAPTS DYNAMICALLY

CHIPS ARE THE KEY TO LOW COST VIDEOTEX

CUSTOM LSI ENHANCES DOT-MATRIX PRINTING



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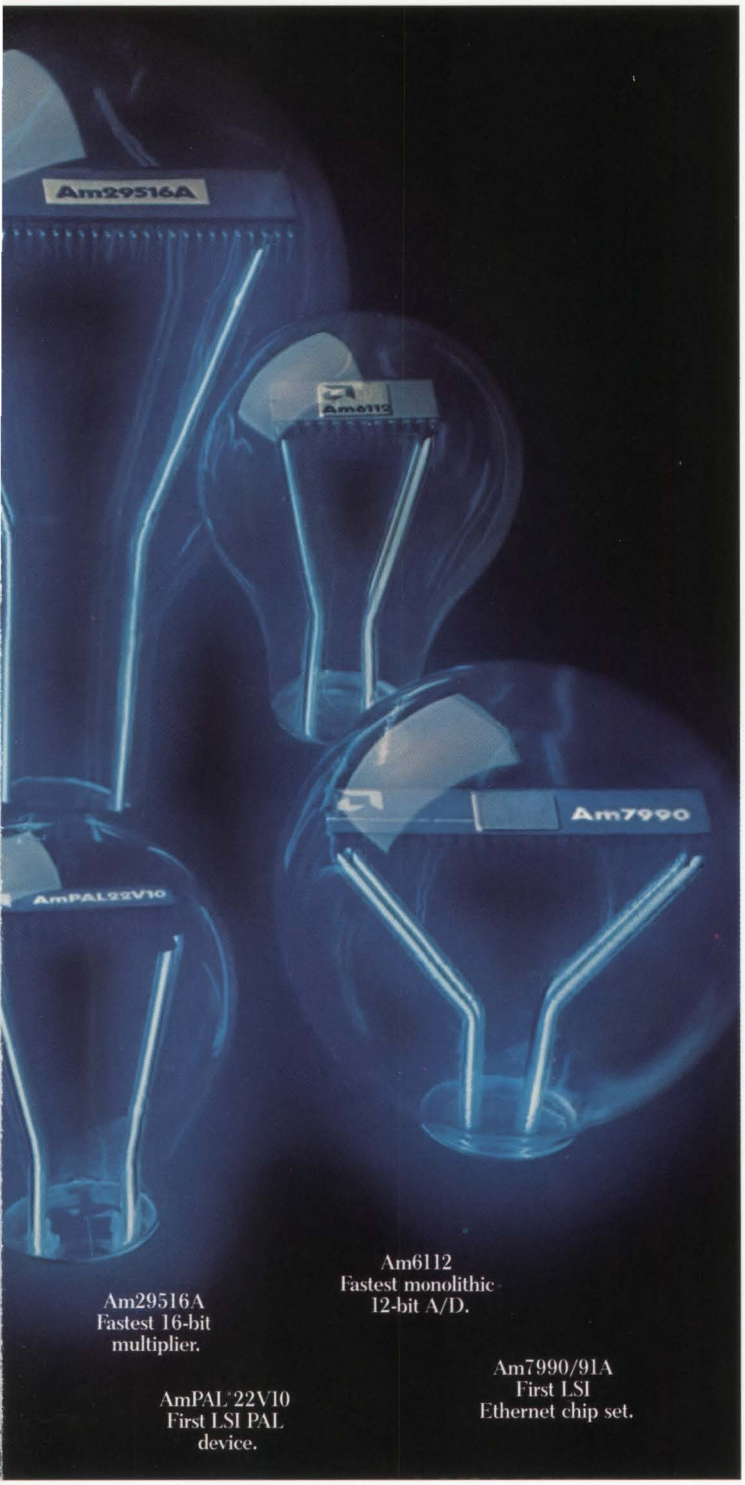

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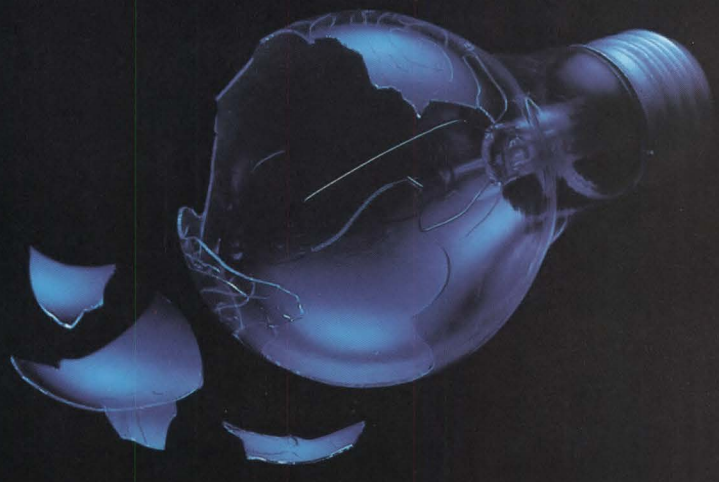

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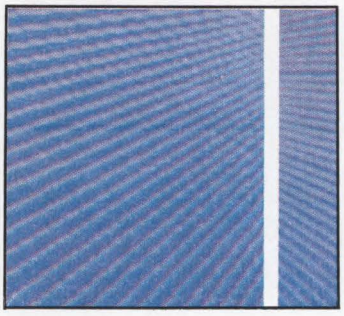
System technology



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by Ashraf M. Dahod—A local area network that dynamically adjusts to changes in the nature and volume of system traffic ensures that devices can obtain timely network access.

75 Computers: **Tagged architecture supports symbolic processing**
by Abraham Hirsch—Even though the Lisp programming language enables artificial intelligence functions on large computers, efficient processing necessitates a different architecture.

87 Integrated circuits: **IC decoder paves the way for videotex revolution**
by Gregg Ledford—Cost is key in public acceptance of videotex information systems. With a presentation-level standard ensuring transmission uniformity, attention turns to development of reasonably priced hardware.

105 Peripherals: **Shift register maneuvers data to add print features**
by Philip Gordon—Using custom LSI techniques, a special type of shift register allows dot-matrix line printers to offer upgraded print and data-formatting features.

NCC '84

55 The National Computer Conference, like its predecessors, offers a varied menu of technical sessions and seminars. Of particular interest to computer-based system designers are sessions such as those on hardware and architecture, computer communications, office automation, and artificial intelligence. Concurrently in the schedule, typical professional development seminars of interest include artificial intelligence, software engineering, computer graphics, supercomputers, and local networks.

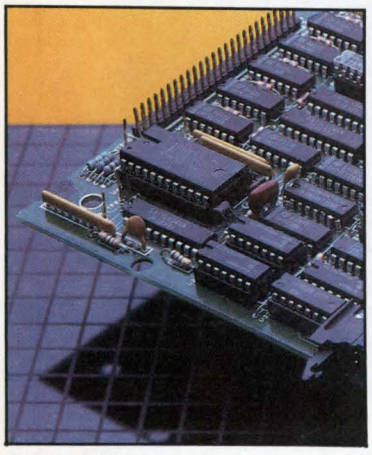
Vol 23, No. 6
June 1, 1984

Special report on microprocessors/microcomputers—Part I

121 The deluge of 32-bit micros is beginning with a trickle. However, by 1985 these wonder chips will be available in quantity to power the next generation of superminis and low end mainframes. Many will be implemented in CMOS, the technology of choice for the next generation of micros. A few will have unique architectures, but all will be designed to run the type of software expected on larger, higher performance computer systems.

This month's cover was created and designed by Mark Lindquist on the Digital Effects Video Palette III and D-48 high resolution camera system. Data bases were constructed by Joe Pasquale and Anezka Sebek.

System components



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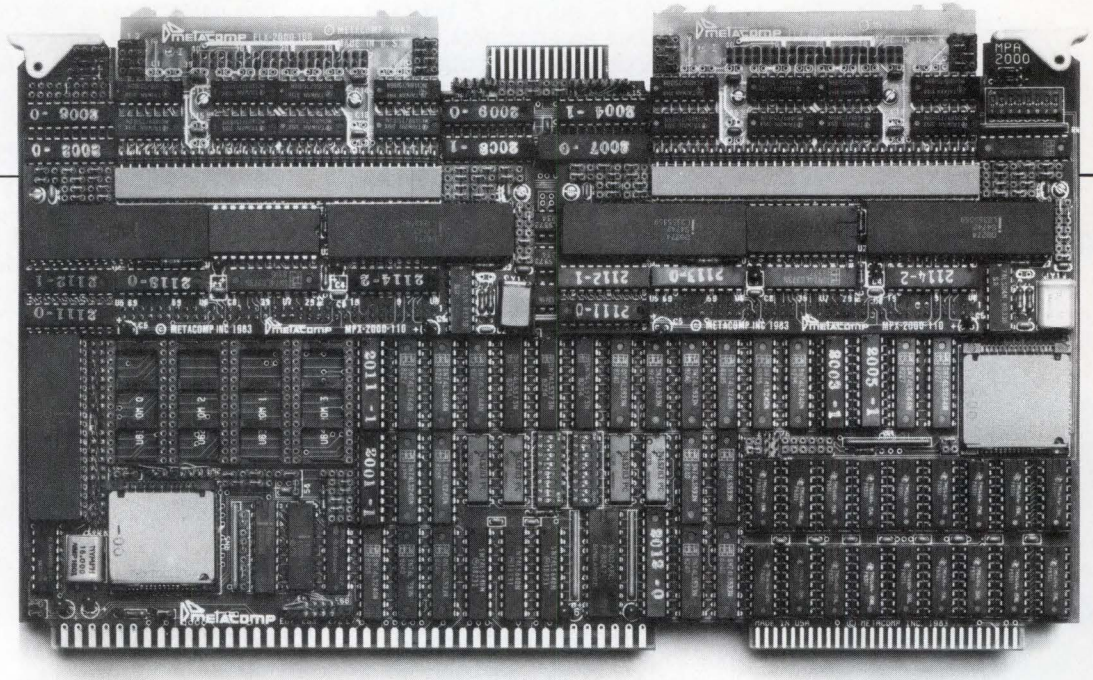
Chairman of the boards



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THE MULTIBUS BREAKTHROUGH PEOPLE

CIRCLE 2

UP FRONT

Superminicomputer features a realtime Unix operating system

The fact that AT&T's just out-of-the-closet 3B20D superminicomputer is suitable for a lot more than just telephony applications—the firm uses it for switching and database control—is clear to savvy computer system designers. They are already looking for it to compete with DEC and Data General's traditional offerings. What is not so well known is that the 3B20D's RTR operating system provides a realtime environment. To do this, the 32-bit processor-based (24-bit virtual and physical addressing) machine's Unix, in contrast to standard Unix, sports three partitions—process, kernel, and kernel process. The extra kernel process partition provides the realtime capabilities while the process partition supports the Unix Version V, Release 2 environment with up to 128 segments of 128 Kbytes each. The kernel process is equivalent to taking the device drivers out of standard Unix and giving each its own address space. Each kernel process can also have 128 of the 128-Kbyte segments but will not handle swapping. Realtime control is provided by 16 execution levels with a preemptive priority structure. Computer designers interested in RTR alone will have to wait to see if it will be unbundled from the 3B20D.—*H.H.*

Texas Instruments to produce National Semiconductor's 32-bit micro family

In a move to accelerate design-ins of the NS32000 family of microprocessors and peripheral chips, National Semiconductor (Santa Clara, Calif) has signed an agreement with Texas Instruments (Dallas, Tex) for TI to produce currently designed chips and to coordinate future designs in the NS32000 family of chips. The long-term agreement culminates in the development of the NS32C432, a CMOS 32-bit microprocessor that will run 7 million instructions/s compared to 1 MIPS for the currently available NS32032. All new collaborative designs will use CMOS processing, and TI plans to include all new designs in the company's extensive cell library of computer aided design tools. According to J. Fred Bucy, TI's president, the NS32000, which has now been relabeled the Series 32000, is the only commercially available true 32-bit microprocessor with a minicomputer VAX-like architecture that runs Unix and offers demand-paged virtual memory. These factors are essential for designing high performance products such as engineering workstations, some of which already incorporate the National part.—*N.M.*

Cell library creates 32-bit CMOS microprocessors

Using a semicustom CMOS library of 60 logic and memory cells, Sperry Corp (St. Paul, Minn) has designed an externally microprogrammable 32-bit microprocessor called Proteus. As presented in the Rochester, NY Custom Integrated Circuits Conference, the chip has nearly 42,000 transistors implemented in 1.2-micron double-level metal CMOS. Although originally designed to demonstrate the CMOS cell library, Proteus has the practical potential of emulating other processors. The chip has a specified cycle time of 120 to 200 ns, dependent on the set of microcode used and the access time of the external RAM or ROM that stores it. A major goal of the project was to show that semicustom design methodology permits fast low cost design. With less than four man-years of development time, Proteus has demonstrated to system designers the possibility of "rolling their own" microprocessors from standard cell libraries.—*J.B.*

UP FRONT

The VMEbus rolls as agreement is forged

A salvo of Motorola VMEbus product introductions has been reinforced by a multiple-source agreement with Signetics/Philips. Motorola Semiconductor Products Inc (Phoenix, Ariz) will become a second source for Signetics (Sunnyvale, Calif) VME boards, such as the System Controller Board (SMVME1500) and the Intelligent Multiple Disk Controller Board (SMVME4300). Signetics will in turn produce a version of the Motorola designed 68010 microprocessor. At the same time, Motorola has added nine new VME modules to its line. These include an Ethernet controller that connects VMEbus nodes to Ethernet, and a monoboard microcomputer based on the 68010.—*J.V.*

ISO computer communication protocols to replace proprietary standards

Practical application of the International Standards Organization (ISO) software protocols for computer communications is no longer a gleam in the standards maker's eye. For example, stimulated in part by the predicted success of next month's National Bureau of Standards sponsored ISO protocol demonstration at the National Computer Conference in Las Vegas, Data General will replace the proprietary network and transport protocols in its Zodiac networking package with the ISO Internet and Class 4 Transport protocols. Not to be left behind in what is becoming a race to "go ISO," Burroughs Corp will make the ISO protocols an integral part of the Burroughs Network Architecture. And, Tektronix says it will implement ISO software to allow its terminals, instrumentation controllers, and development systems to be ISO compatible. All of these conversions mean that computer system designers will be able to hook up more and more disparate computer-based gear regardless of manufacturer—without expensive protocol converters.—*H.H.*

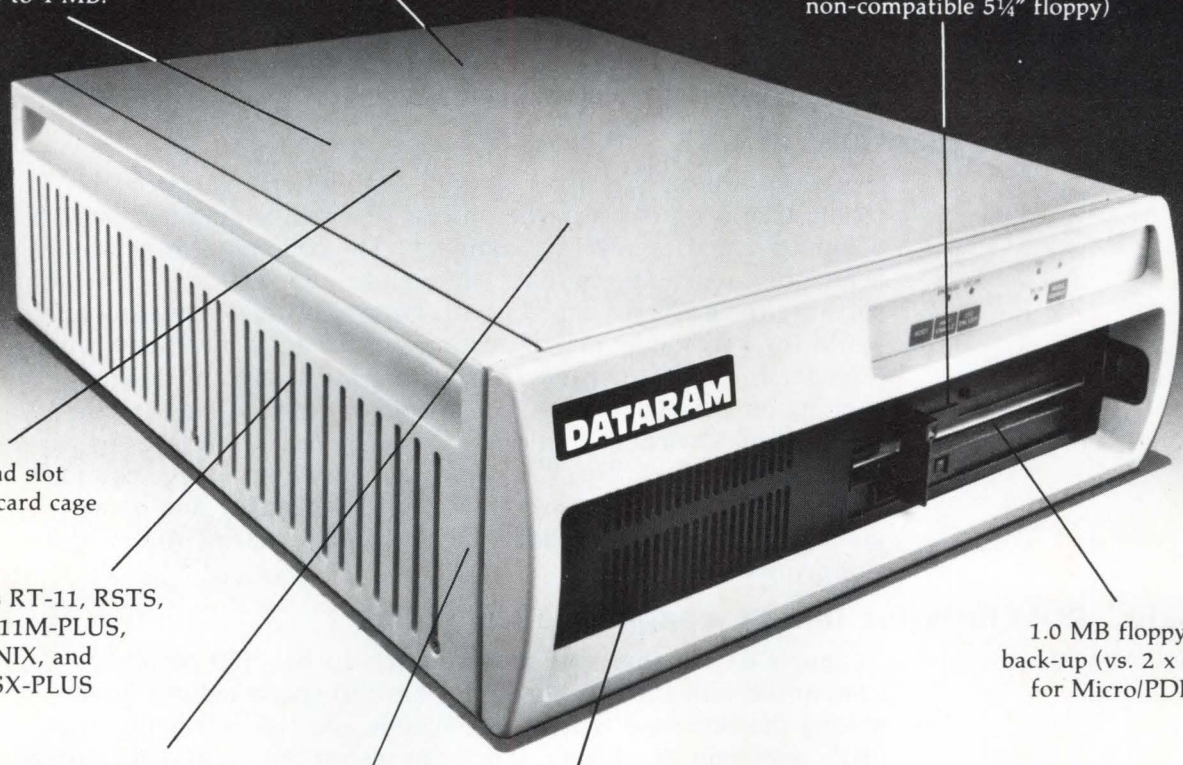
System design lags, VLSI advances

Setting the tone for the Custom Integrated Circuits Conference in Rochester, NY, General Electric (Triangle Park, NC) vice president James E. Dykes in his keynote address pointed out the growing gap between VLSI designers and system designers. He called for the establishment of standards for design systems VLSI and CAD tools as a first step toward bringing the two disciplines together. He also noted the need for better CAD systems to allow direct translation of systems to the chip level. Finally, Dykes proposed greatly expanded training for system designers to increase the number of engineers from the few thousand currently involved in the VLSI design to the hundreds of thousands needed to make VLSI system design meet its promise.—*J.B.*

Motorola adds a chip to the 256-Kbit pot

Introduction of Motorola's 256-Kbit dynamic RAM chip at this year's Electro conference is one more signal that U.S. manufacturers are finally responding to Japanese incursions. With substantial numbers of 256-Kbit RAMs from Japanese producers (including Fujitsu, Toshiba, Mitsubishi, NEC, and Hitachi) already on the market, stateside companies have to overcome a long lead. Samples of Motorola's chip will be available in the second half of 1984, with quantity production beginning late in the year. Mostek already has samples of a 32-K x 8-bit RAM in the field and will introduce a 256-K x 1 device next year. And, a few customers of both Texas Instruments and Intel have received some 256-Kbit chips for sampling.—*J.V./S.F.S.*

Like DEC's.



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CIRCLE 3

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UP FRONT

Algorithms to be developed to match new parallel computer speeds

Pipelining, data flow, multiple processors, and other parallel hardware architectures for tomorrow's faster computers show much promise. However, it's a poorly kept secret that the classic algorithms used to solve design problems are made for serial machines and just don't work well in parallel architectures. But, parallel hardware designers need not despair; the Air Force Office of Scientific Research at Bolling Air Force Base in Washington, DC is starting what it calls a Fast Algorithms Initiative. The program will address (and support) good algorithm ideas for large scale computation that are also suitable for emerging parallel hardware architectures. Both hardware and software designers will need to keep track of what this project turns out and may even want to submit some ideas themselves.—*H.H.*

Versatec enters the world of CAE

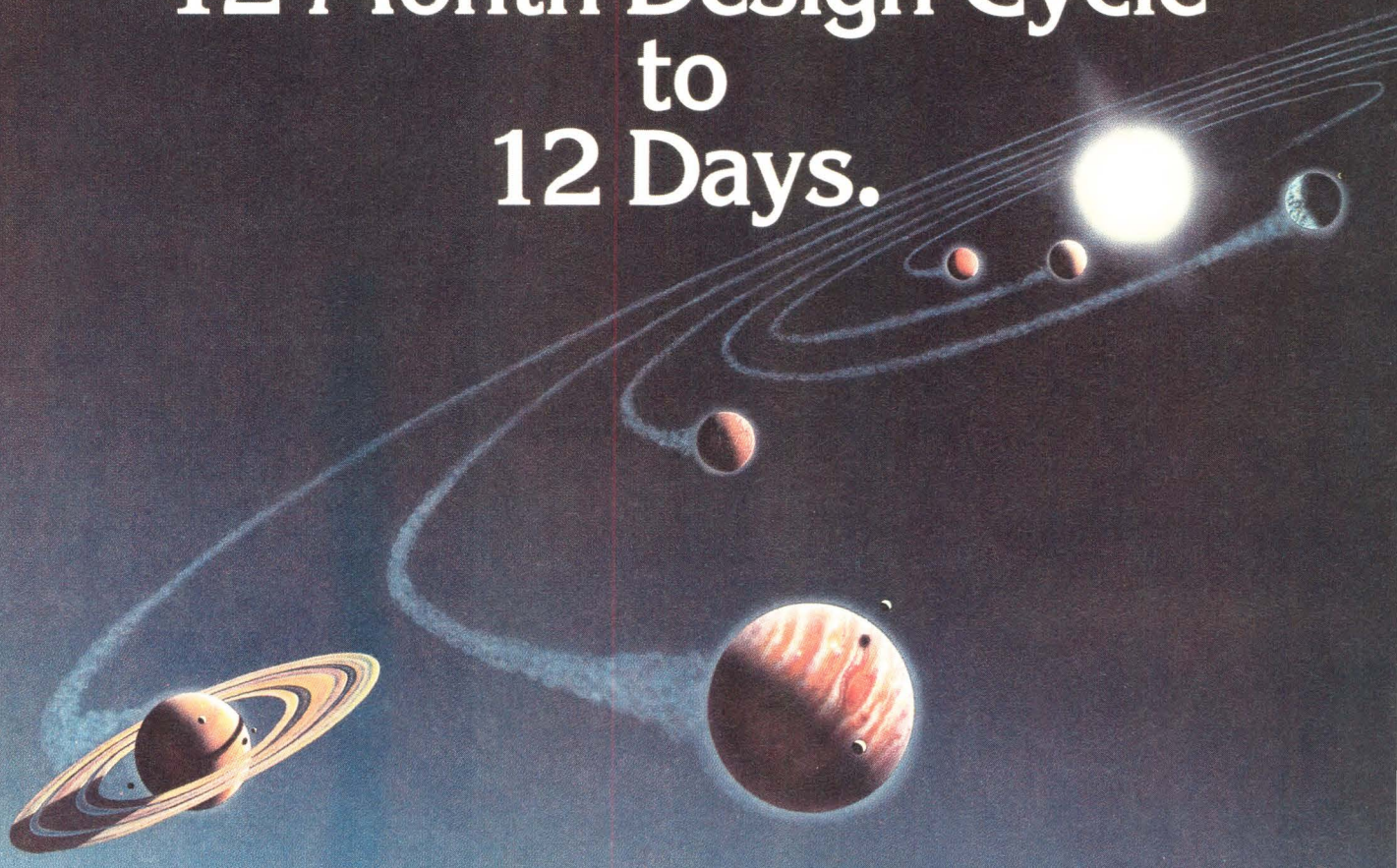
A well-known manufacturer of high end plotters, Versatec Corp (Santa Clara, Calif), is in the process of transforming itself into a computer aided engineering company. The company, owned by Xerox, is adapting schematic capture, place-and-route, and logic simulation software to the Xerox Star system, known in the office automation world for its window management in an Ethernet-based environment. Versatec is still in the process of getting a full suite of design software running on the Star system, but intends to incorporate the Star's flexible user environment along with such engineering packages to generate test vectors for ATE equipment. In addition, the company will call upon the existing software (eg, word processing and data management) already available on Star office systems to use as a competitive edge.—*T.W.*

"Safe" ROM BIOS for IBM PC-compatible computers

Designers developing personal computers to be "100 percent" compatible with the IBM PC do not have to spend tedious hours writing the Basic I/O System (BIOS) code and risk infringing upon IBM's copyright any longer. They can instead buy a PC-compatible BIOS package for $100,000, embed it in ROM, and be assured via a $2-million insurance policy against a copyright infringement suit that their newly designed PC-compatible computer does not infringe on IBM's BIOS. Phoenix Software (Norwood, Mass) went through meticulous procedures that company president Neil Colvin says was "a technologically unchallenging effort but an overwhelmingly difficult legal hurdle to overcome." Part of the procedure was to develop a functional specification for the IBM PC BIOS from IBM's reference manual and hand this specification to an independent software developer who knew nothing of the BIOS. Phoenix became the single interface point between the developer and the test group that was geographically distant from the developer and that developed the test procedures to ensure that the new BIOS was compatible with the PC. Only written communications describing problems were transmitted between test group and developer. Phoenix followed all these steps at the advice of legal counsel after numerous PC-compatible manufacturers were challenged in court by IBM with the claim that the BIOS written by their engineers infringed upon IBM's copyright.—*N.M.*

Networking Your System?

Change a 12 Month Design Cycle to 12 Days.



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CIRCLE 4

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CIRCLE 5

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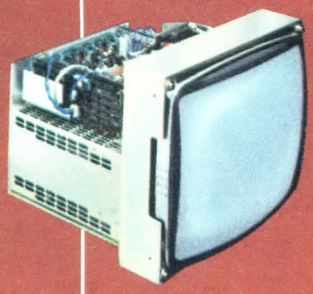

- 1280 × 1024 Resolution
- 60Hz, Non-interlace
- 100 MHz Bandwidth
- Compact, modular design

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HM 3619A

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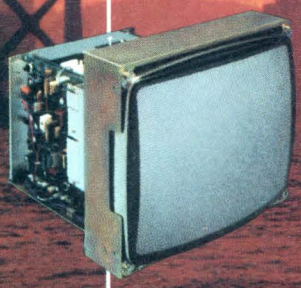

- 1024 × 1024 Resolution
- 40 MHz Bandwidth
- Compact

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HM 3719

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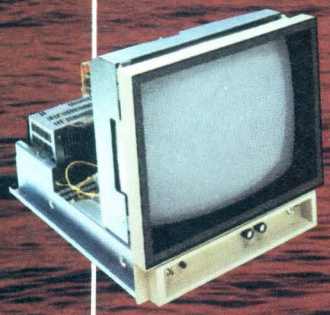

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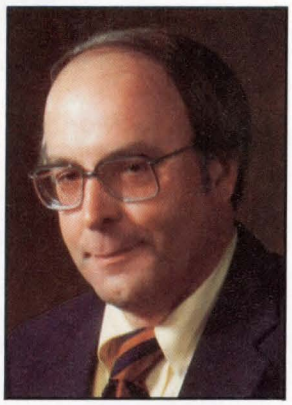
CIRCLE 6

WHAT'S A COMPUTER JOURNALIST?



One unfortunate by-product of the Watergate crisis was the emergence of a new generation of journalists who saw the profession as a shortcut to fame and fortune. Of course, journalism no more provides an automatic ticket to success than does engineering or any other profession. But, the new journalists are a determined crowd. In search of big bucks, the post-Watergate kids have swarmed to each and every new fad—most recently, personal computers.

Because objectivity, detachment, and humility don't carry much weight in their lexicon, the new journalists find ample opportunity to promote themselves and each other ("you mention me in your column and I'll mention you in mine"). In addition, to co-opt the glamour of the industry they claim to cover, they call themselves "computer journalists." A few weeks ago, for example, the *Boston Globe* ran an article in which the writer raved about a young woman who had taken over a successful newsletter and turned it into a slightly less successful one by renaming it and shifting its emphasis from semiconductors to personal computers. The *Globe* writer characterized the woman as the "doyenne of computer journalism."

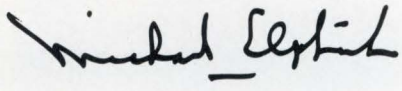
This could all be dismissed as just another passing fad, except that one of the "computer journalists" has reached a new level of arrogance by choosing to question the ethics of the technical trade press—the magazines that have been covering the technology while the "computer journalists" were writing their gossip columns. In his "Periscope" column in the *San Francisco Sunday Examiner and Chronicle,* John Dvorak launched his offensive with the headline: "The sorry state of high-technology journalism." After crediting himself with having written the most thorough analysis of Apple's Macintosh, he continued as follows: "Most of the specialized journals are written primarily by public relations firms for their clients. When you see an article in *Byte* or *Electronics,* for example, and it is supposedly written by some engineer or corporate president, you are being fooled. With few exceptions, the article was ghost-written by one of the many Silicon Valley hi-tech PR firms and put into the magazine because the company advertises a lot...Even most of the so-called news items are simply rewritten (if that) press releases. The public relations firms grind them out, and the "journalists" lightly edit them." Since Dvorak's column appeared on April Fools' Day, it is just possible that the joke is on me. However, the friend who sent me the clipping didn't think it was a joke—and I doubt if the editors of *Byte* and *Electronics* did either.

Unfortunately, there is just enough truth in what Dvorak says to trap the unwary reader into believing all of it. It is true that not all engineers write the articles that carry their bylines—just as not all celebrities write their own memoirs. Some do not have the time, and some do not have the ability. In *Computer Design*, for example, I would estimate that 20 percent of the contributed articles are initially ghost-written. But, the articles are then heavily rewritten by our editors and checked for accuracy by the bylined authors. Of course, if the manuscript is too commercial, it is not accepted. Articles are solicited, accepted, and edited solely to inform readers and fulfill our editorial plans—not "because the company advertises a lot."

The main reason magazines do a lot of editing, research, and original writing (and scrupulously avoid pandering to advertisers) is simple. It is known as competition. A magazine must serve its readers and maintain a high readership or it will soon die. The only publications that can get away with running unedited press releases are newspapers. By the time a monthly magazine appears, its readers already know the basic facts—they need in-depth and technically knowledgeable news analysis. Of course, Dvorak doesn't have to worry about competition because he works for a monopoly newspaper.

Furthermore, magazines such as *Computer Design* are able to do a better job because they hire engineers as editors. We have six graduate engineers on the editorial staff, and most of them worked as design engineers before switching to journalism. For example, John Bond—who wrote the staff report in this issue—is an engineering graduate of the U.S. Naval Academy. He has worked as an engineer for General Dynamics, the Air Force, and Texas Instruments. He also worked for two competing magazines and for Digital Equipment Corp, before joining our magazine. His report on 32-bit microprocessors certainly doesn't follow a script handed out by PR people of the companies advertising in *Computer Design*. In fact, less than half of the companies mentioned in Bond's report advertise in our magazine. And, their PR people don't send out press releases saying they are having trouble making 32-bit processors or that they won't be introducing them until next year. That sort of information has to be dug out the hard way.

So, if anyone can claim to be a computer journalist, I would think that a professional like John Bond should take precedence over a gossip columnist like John Dvorak. In fact, he may even be a doyen.



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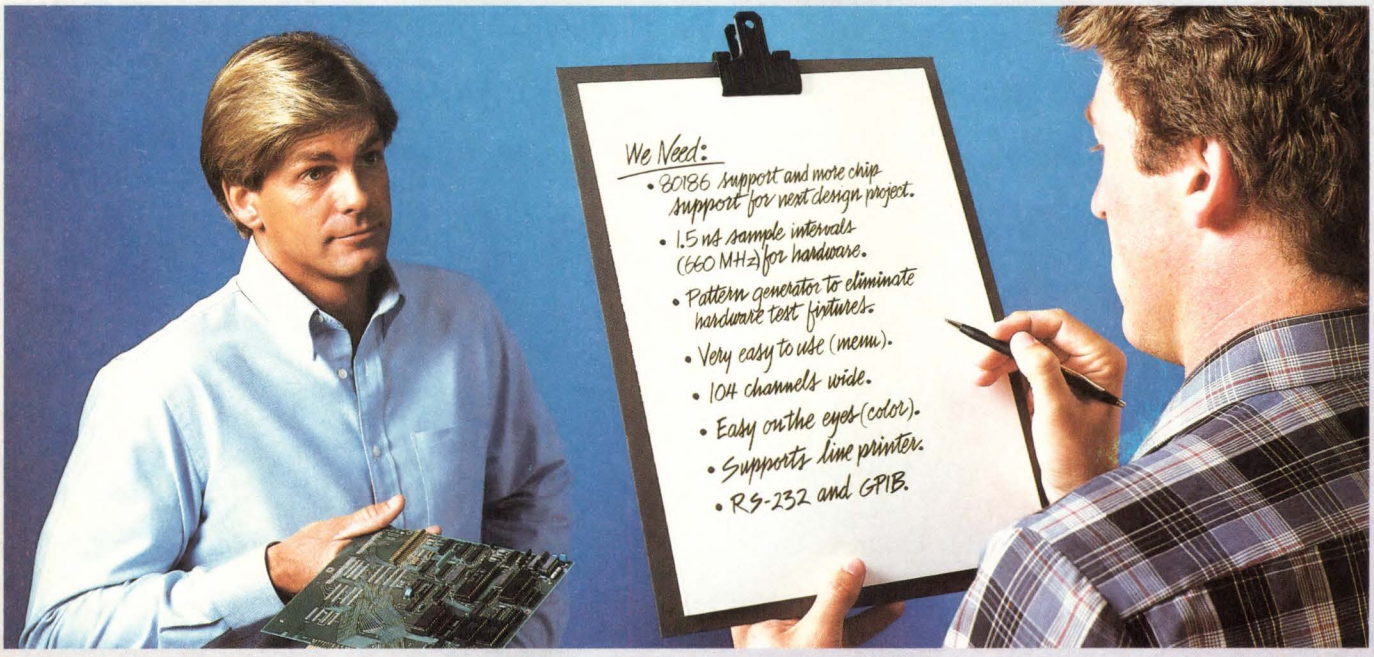

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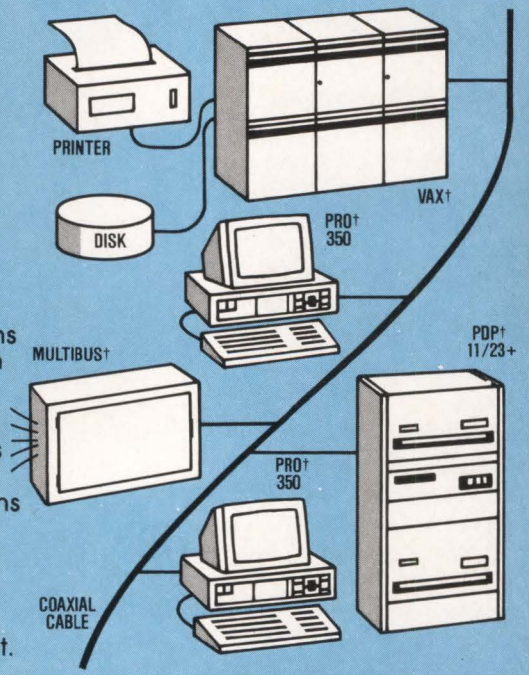

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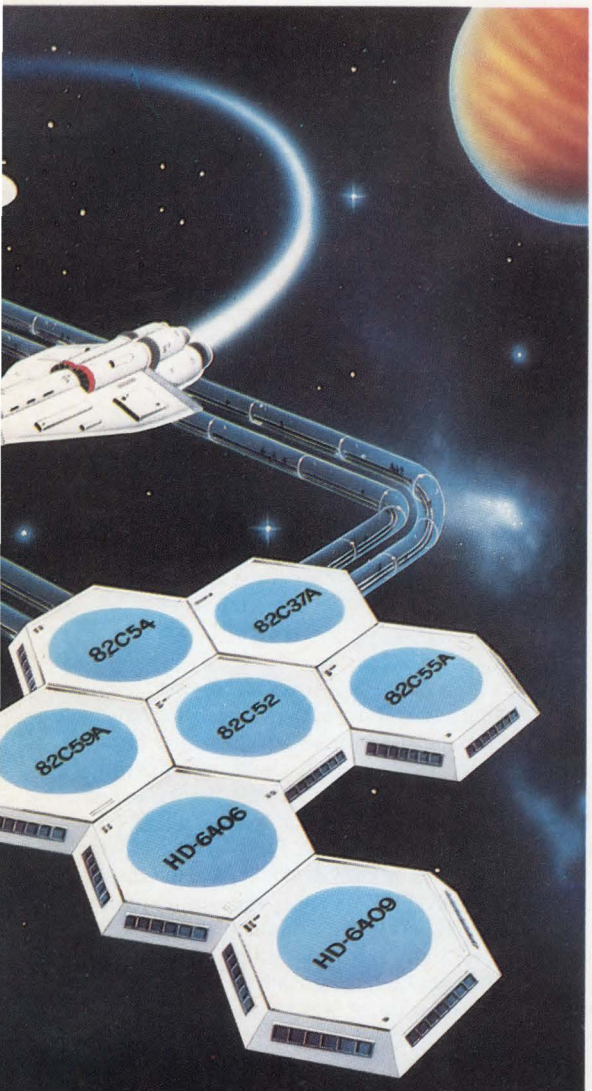

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CIRCLE 11

LETTERS TO THE EDITOR

Predicting microprocessor reliability

I read with interest Carl P. Oppenheimer's article, "Reliable Designs Begin with the Basics" (Aug 1983, p 93). The article treats microprocessor reliability predictions as a lost cause because design flaws can cause erratic operation. However, one of the basic rules of any reliability prediction is that the design be in accordance with generally accepted practices. Then a prediction can be made based on the reliability of the individual components.

This prediction can be quite realistic, since it is based on data that has been accumulated for over 20 years. In fact, many manufacturers are now using predicted MTBF as a part of their specifications. These predictions are also used to determine service and spare parts requirements.

Since it is relatively easy to predict microprocessor system reliability with the data base that is available today, one wonders why it is not used more as a sales tool. I have noticed it advertised heavily for many Japanese digital products. Could it be that they are about to beat us in this area too?

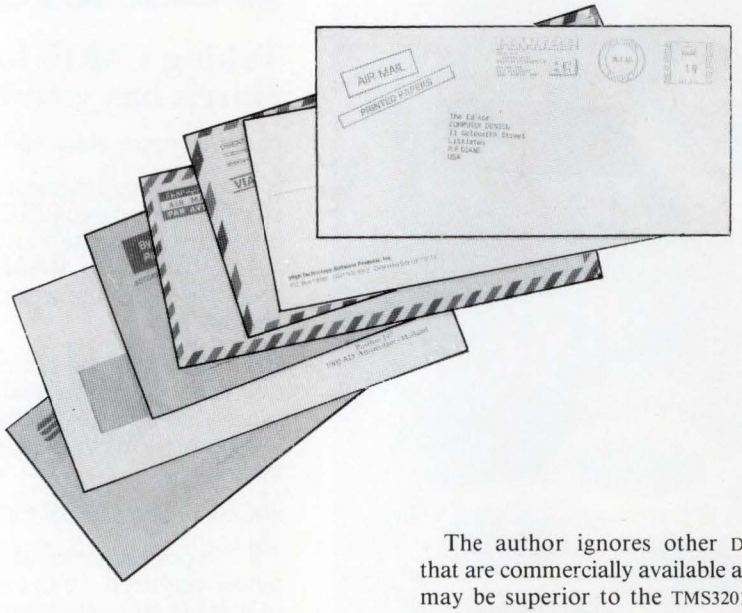
Michael Hordeski
Siltran Digital
2250 Monterey Rd
Atascadero, CA 93422

Educating the public

The February 1984 editorial, "The Computer Illiteracy Threat," is very much to the point. But it is not just excessive hype that is ruining the bright future for the industry. Just about everyone is ignoring that the public has been offered a tool that it does not know how to use.

Graphics capabilities are not only useless, they are a threat to a public that has been left untutored in the meanings of visual communication. Willful color manipulation because it is available and technically possible, is worthless for most. One must know how to channel, what the subliminal metaphor is that has been triggered, and what the human factors of the psychological response are.

Indeed, by creating this magic tool, and pushing it on the public, it is the responsibility of the industry (made up of those who have often detested the humanities)



to explain and relate, to equate and simplify. And, if the members of the industry cannot do this, then they should hire someone who can.

Odeda Rosenthal
East Hampton, New York

Industry teams up with academia

The increasingly common alliances between industry and academia (Apr 1984, p 6) portend further economic hardships for working engineers. Too much of the work previously assigned to industry's engineers is now diverted to the campus, where it is performed, in the guise of "research," by greedy professors and grossly underpaid graduate students.

It is a trend that must be resisted.

Irwin Feerst
Committee of Concerned EEs
PO Box 19
Massapequa Park, NY 11762

There's more than one DSP chip

I have just finished reading Surendar Magar's article "Signal Processing Chips Invite Design Comparisons" (Apr 1984, p 179). I was very disappointed to discover that *Computer Design* would print an article that appears to contain technical information, but turns out to be nothing more than a slanted opinion or an advertisement for a particular system.

The author ignores other DSP chips that are commercially available and which may be superior to the TMS32010. However, because of his choice of chips, the TMS32010 appears to be the best DSP chip available. That is far from reality.

For example, the Fujitsu MB8764 DSP, which is currently available, was not memtioned. Furthermore, the author completely neglected to mention the AT&T Bell Labs DSP chip which, although it may not be commercially available to anyone outside of AT&T, was the first DSP chip developed. In fact, recent generations of the chip continue to lead in the area. Also, any customers within AT&T would be comparing any other chip to the Bell Labs DSP chip.

My disappointment is that I expected that at least an editor of the article would catch the omissions.

Salomi T. Charalambous
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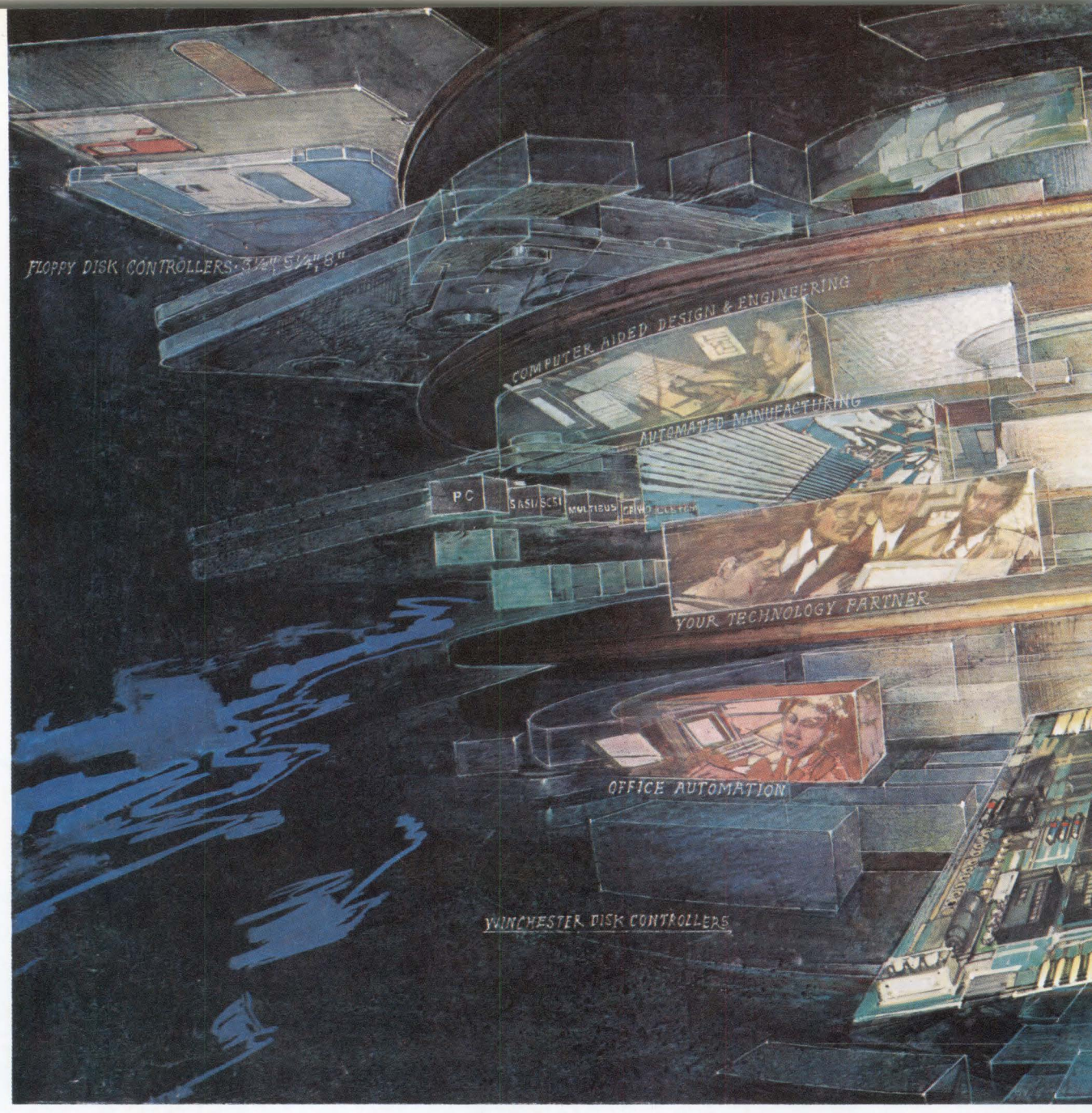

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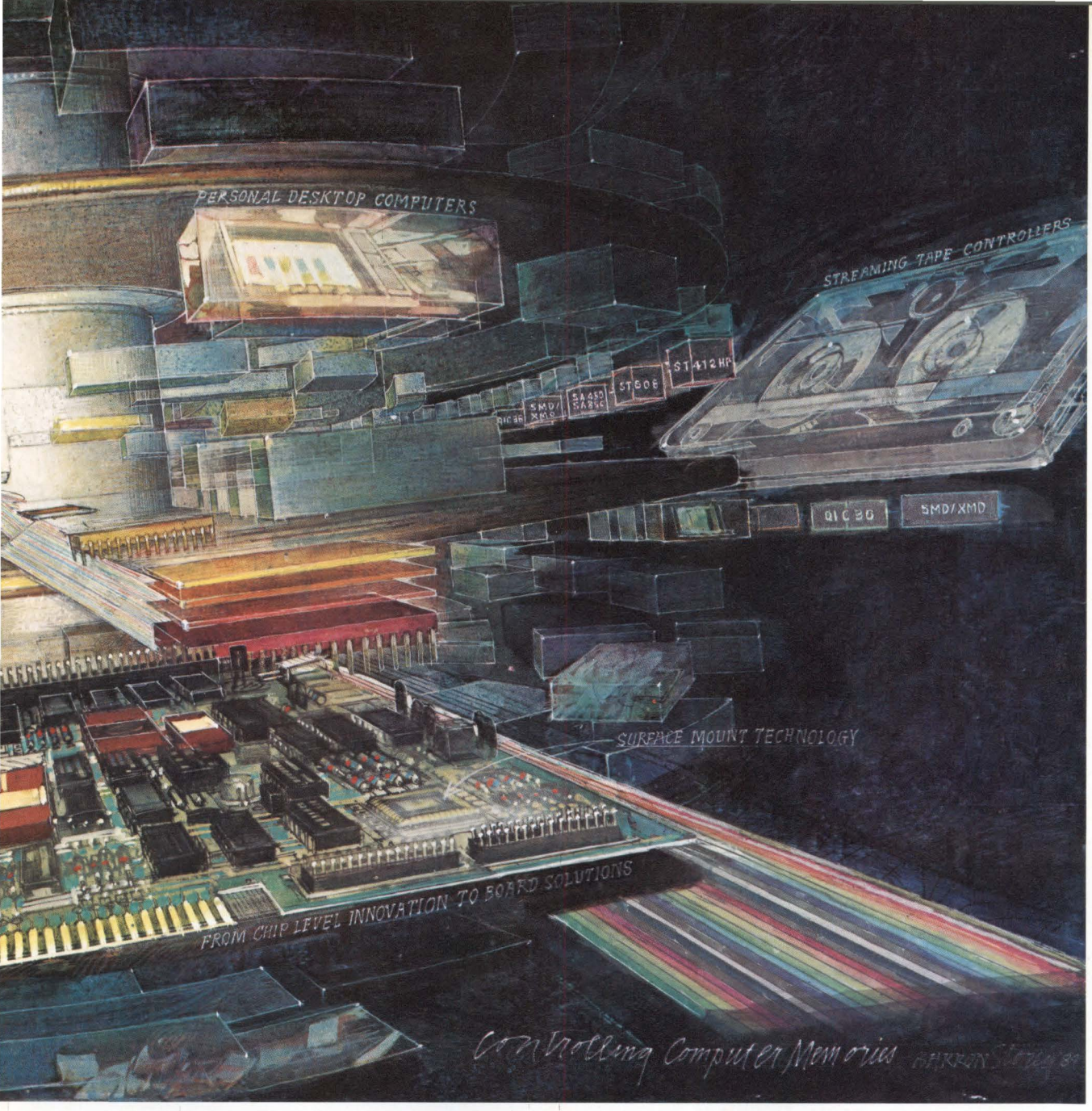

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CIRCLE 15

Superminis assert superiority through superior numbers

The flurry of recently released 32-bit minicomputers dampens rumors that micros have taken over the minicomputer world. Some say this renewed vitality stems from recognition of the need for an intermediary in the micro-to-mainframe link. Others maintain that minicomputers have always occupied a special niche because of their superior price/performance ratios, and interactive natures.

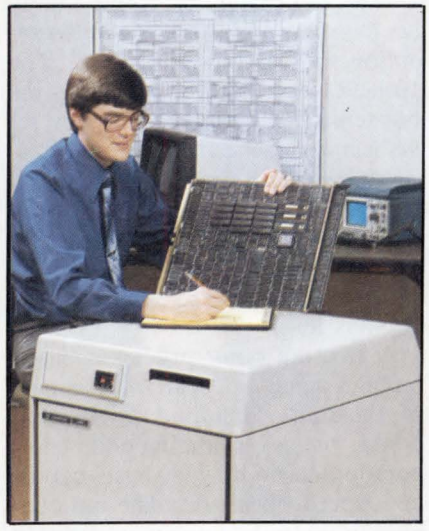
Heading for top ranking in the supermini field, Gould extends its Concept 32 family with the addition of the 32/97XX, and Digital Equipment Corp puts together a machine that supplies more raw power than the familiar VAX 11/780. Meanwhile, Harris Corp extends its 48-bit line with the entry level H60, and Modular Computer Systems Inc joins the 32-bit ranks with its Classic 32/85. In addition, AT&T launches its long-awaited line of mini and supermini machines.

Even more diverse than the companies promoting them, these machines fit every conceivable need. Common to all is a smaller sized package. This is made possible by increased use of VLSI to replace discrete IC packages, and the heavy use of 256-Kbit RAM in main memory. In addition, most support Unix, and remain compatible with other family members by running proprietary operating systems.

Cutting down on package size

Harris Corp's (Computer Systems Division, 2101 W Cypress Creek Rd, Fort Lauderdale, FL 33309) H60 has a 48-bit CPU, which is contained on only two boards. The 256-Kbit RAM allows 6 Mbytes of memory to reside on a single board, while retaining all standard error detection, error correction, and diagnostic features. An example of this is the optional single board integrated scientific arithmetic unit (ISAU) hardware processor that supplies a 50 percent increase in floating point performance over equivalent software routines. The ISAU contains 900 fewer ICs than the previous 5-board implementation, a reduction achieved through heavy use of VLSI and custom gate arrays containing more than 8000 gates.

Inside this 30- x 19- x 30.5-in. (76.2- x 48.3- x 77.5-cm) cabinet is a CPU, an 80-Mbyte, 8-in. Winchester disk drive, a 23-Mbyte cartridge tape drive, and a communication controller. The unit can support up to 32 interactive users, and its performance is rated at 80 to 110 percent of that provided by a VAX 11/780.



Operating at nearly 1 MIPS, the Harris 60 uses VLSI/LSI circuits, custom gate arrays with over 8000 gates, and a 256-Kbit RAM to decrease bulk. Performance enhancements such as the integrated scientific arithmetic unit (ISAU) increase reliability.

To supply this performance level, the CPU includes a 6-Kbyte cache memory formed of 150-ns bipolar RAM—half storing instructions, half operands. The unit currently runs the proprietary virtual memory operating system (VOS) to maintain software compatibility with more powerful family members. Unix support should appear by the end of the year.

Aiming for a similar sized box, Gould (Computer Systems Division, 6901 W Sunrise Blvd, Fort Lauderdale, FL 33313) fielded the PowerNode 6000 series. Composed initially of PowerNode 6030, 6050, and 6080, the series' performance is rated from 1.5 to 3 times that of the 11/780. The entry level 6030 packages 2 Mbytes of main memory with an 80-Mbyte Winchester drive and 60 Mbytes of cartridge tape in a 30- x 29- x 30-in. (76.2- x 73.6- x 76.2-cm) cabinet. It is based on a 3-board, 32-bit CPU.

The supermini architecture of the high speed TTL CPU accommodates a 32-Kbyte, 2-way set associative cache memory. This memory provides 150-ns effective access time. Virtual addressing for up to 16 Mbytes, in conjunction with demand-paged hardware memory management, allows handling of large programs.

A second processor in a tightly coupled configuration raises the computational power of the 6080 by as much as 80 percent. As in the Concept series, this internal processing unit handles computation-bound tasks for the CPU. The UTX/32 operating system for the series is based on the Berkeley 4.2 BSD Unix, with features from Unix System V. This operating system supports virtual memory management, as well as the tightly coupled dual processors used in the 6080.

The Classic 32/85 marks Modular Computer's (Modcomp, 1650 W McNab Rd, Fort Lauderdale, FL 33310) first venture into the high performance 32-bit world. With the CPU's effective cycle time of 100-ns and extended microinstruction word length that allows parallel internal operation, Modcomp leaves its traditional 16-bit realm. Aimed at answering needs for realtime response, this machine provides rapid movement between priority based tasks with extremely fast context switching.

The 32/85's instruction set processor is a complete ALU that consists of a functional microprogrammable processor with hardware multiply and floating point arithmetic. Its context file is a high speed RAM containing 128 sets of 15 general purpose registers. Operating under the control of independent status words, the vectored interrupt system is able to switch up to 16 mapping caches (each 128 registers) and up to 128 sets of

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Superminis assert superiority

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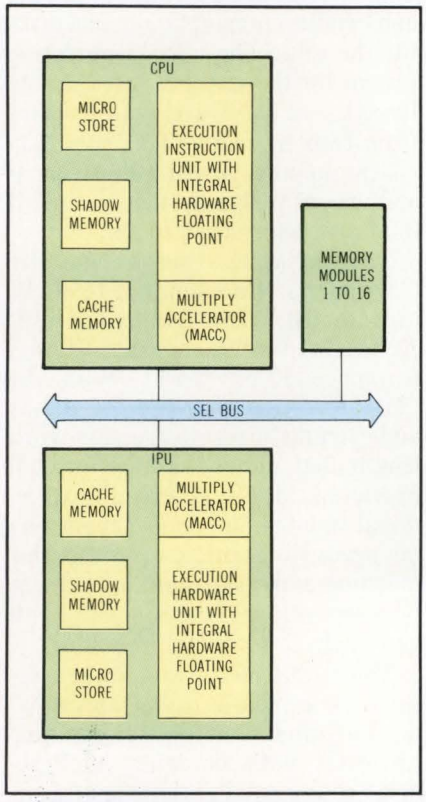
15 registers (each 32 bits wide) within a few microseconds. This arrangement eliminates the need to save and restore environments under software control, and allows the machine to handle fast changes when performing in realtime environments.

The system's multiported memory enables concurrent parallel transfers through up to six ports. Multiported memory also allows shared memory and multiprocessor configurations to be built. Such units fill needs for high performance applications by providing load sharing and high availability. This memory is overlapped, not interleaved as in other systems. Thus, failures are confined to a single memory module, rather than allowed to spread throughout multiple modules. In addition, the system uses cache memory to speed effective memory access time. This 64-Kbyte, 4-way set associative memory is broken into 16 Kbytes per set. A least recently used algorithm is used to maintain a record of the least recently used set for each group of four 32-bit words in the cache.



Functional units within the central and internal processing units that form the Concept 32/9780 are connected by internal buses that have 75-ns cycle times. During each 75-ns cycle, 4 macroinstructions are in various phases of execution, increasing the effective throughput of the system.

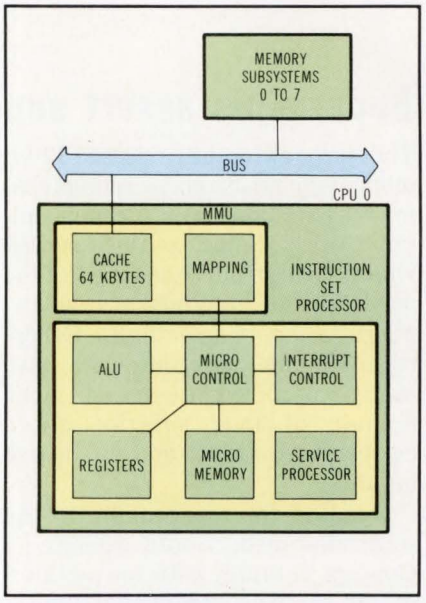
Raising the stakes

Gould's high end contribution to superminicomputer class machines supplies all the performance of previous Concept 32 systems, plus 16-Mbyte task addressing capability and modular performance enhancements. Moreover, in its basic configuration (with CPU, 4 Mbytes of main memory, and 32 Kbytes of cache memory), the 32/9705 provides performance rated at up to 4.67 million instructions per second (MIPS).

Low end machines in this family are based on an instruction unit/execution unit CPU architecture. The 10-K ECL CPU has a 75-ns cycle time bolstered by the use of a 4-way set associative cache memory and a 4-stage instruction pipeline. Optional performance enhancements—ie, multiply accelerator, additional cache, shadow memory, and dual processor—raise CPU performance to the 10-MIPS level.

A floating point processor based on high speed ECL is an integral part of the CPU. Handling single- and double-precision floating point computation, its 64-bit wide buses permit high speed operation. The optional plug-in multiply accelerator (MACC) adds 1 MIPS to the CPU's computational power by computing products for nine integer and floating point instructions. Comparable to a two-board plug-in VAX, but transparent to the software, the MACC makes its presence known only by the speed with which multiply computations are executed.

Main memory's 300-ns read, 150-ns write cycle is reduced still further by the use of cache memory that resides between main memory and the processor. The optional 32-Kbyte cache, structured with 4 banks of 8 Kbytes each, provides a double word to the CPU in 75 ns. Another option, user-controllable cache or shadow memory, consists of from 128 to 256 Kbytes of high speed RAM. Used in conjunction with the cache controller, shadow memory (like cache) can be accessed within a 75-ns cycle time.



The CPU in Modcomp's 32/85 executes two instruction sets; one compatible with the 16-bit Classic II/75, the other providing 32-bit addressability. The instruction set processor is a complete ALU consisting of a functional microprogrammable processor with hardware multiply and floating point arithmetic. Microinstructions are contained in a writable control store.

However, whereas addresses contained in cache are a function of recent processor utilization, shadow memory always contains the same set of addresses. This can raise the hit rate from the approximately 95 percent attained with a large cache to 100 percent, thus guaranteeing a certain level of performance in time-critical applications.

The long-awaited arrival of AT&T's (Computer Systems Division, 222 Broadway, New York, NY 10038) promised contributions to the superminicomputer world let established vendors breathe a sigh of relief. While extensions to the family promise significantly increased performance, the three mini level systems, the 3B20S, the 3B20A, and the 3B20D use readily available technology.

These systems use bit-slice bipolar technology and 64-Kbit RAM. The 3B20S architecture relies on programmable micro store with capacity for 8 Kbytes of 64-bit long instructions as well as cache memory, to attain speeds of 1 MIPS. With 8 Kbytes of cache enabled, the CPU can access its maximum 12-Mbyte memory in a 400-ns

effective access time. The single processor 3B20S machine that supports up to 100 users and performs at a rate of roughly 1 MIPS grows into a 3B20A attached processor system that nearly doubles performance. Rated at 1.8 MIPS, the 3B20A uses parallel processing, with both processors performing operating system calls independently. The unit supports 50 to 180 users and costs only 30 percent more than the 3B20S.

The 3B20D is a dual processor unit that provides fault tolerant performance. To supply high reliability (minimum downtime), one processor acts as a hot standby for use only when the other malfunctions. This unit runs the Unix realtime reliable (RTR) operating system to provide its fault tolerant features in a realtime environment. These reliability features are supplied by a fully duplexed architecture. Redundant self-checking logic allows automatic fault detection. All peripherals are dual ported and the operating system provides for automatic reconfiguration after failure. A crashproof file system and mirrored disk volumes ensure data integrity.

To stay competitive, DEC (146 Main St, Maynard, MA 01754) has introduced a new VAX, not the anticipated "Venus," but an adequate extension to the line. Along with this extension come promises that further additions will be made later this year. The new VAX 11/785 provides performance 50 to 70 percent greater than the 11/780, bringing it up to the 1.7-MIPS range. Improved circuit technology and internal performance enhancements in the traditional VAX architecture provide increased power. Improvements include implementation of the CPU from high speed advanced Schottky circuits, larger cache memory, new floating point accelerators, and writable control store for microprogram instructions.

CPU cycle time has been shortened to 133 ns to match the switching capability of the advanced Schottky logic. This accelerated cycle time allows operations to occur 50 percent faster. Synchronization circuitry allows the system to use unmodified /780 synchronous backplane interconnect interfaces, controllers, and peripherals.

Injection of a 32-Kbyte cache into the CPU reduces bus traffic by increasing the probability that data will be in cache. This reduces data transfers from main memory and improves I/O performance. Using the same technology and timing as the CPU, the FP785 floating point accelerator can improve floating point performance 47 percent.

Another change is the storage of microcode in RAM, instead of in ROM as in the /780. This provides enhanced CPU performance and facilitates microcode updates. All in all, this system can support 50 workstations or 100 interactive terminals, while maintaining compatiblility with existing software and peripherals.

In spite of all this activity, the performance improvements displayed by these machines are marked more by evolution than revolution, and may disappoint those looking for great strides forward. However, recognizing that these incremental achievements were enabled through simple circuit tweaking makes speculation about future advances even more exciting.

—Peg Killmon, Senior Editor

DATA COMMUNICATIONS

Simpler clusters emerge as local area network alternative

Monolithic local area networks may give way to a cluster concept. Based on multiple clusters, each operating within narrow geographical and organizational boundaries, the concept simplifies peripheral sharing and cuts connect costs. Simplicity results from tying fewer terminals together. The cost per connection is reduced because less data travels shorter distances at slower speeds.

This cost reduction is the goal of vendors such as AST Research with PCNet, Network Development Corp with its Device Network Architecture, and IBM with PC Cluster. These offerings serve fewer users (typically no more than 32) and run shorter distances than high speed networks such as Ethernet. However, they guarantee access to network resources with lower system overhead.

Developing alternative networks

Meanwhile, a related development focuses on cheaper implementations of the IEEE 802.3 baseband (read: Ethernet) specifications. National Semiconductor (Santa Clara, Calif) hopes that its upcoming network controller chip set will find its way into "Cheapernet" systems using inexpensive RG58AU coaxial cable rather than the more costly RG50AU cable Ethernet requires. Advanced Micro Devices and Seeq Technology, Inc (both in Sunnyvale, Calif) may also support this alternative, which lowers cost while retaining the 10-Mbit/s data transfer rate of its cousin.

Rather than competing directly with their more expensive counterparts, cluster nets actually increase high speed network effectiveness. By focusing on natural work settings (eg, groups of offices or a department), they concentrate resources where needed. Up to 95 percent of communication traffic involves accesses to local data bases or local peripherals, according to Albert Wong, vice president of AST Research (2121 Alton Ave, Irvine, CA 92714). Clustering reduces the amount of traffic over high speed networks. Network traffic consists only of requests to central

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Simpler clusters emerge

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Comparison of Clustered Networks

	Cheapernet	PCNet II	PC Cluster	Device Network Architecture
Transmit speed	10 Mbits/s	800 kbits/s	375 kbits/s	800 kbits/s
Topology	bus	bus	bus	bus
Access method	CSMA/CA*	CSMA/CA**	CSMA/CD	polling
Transmission medium	coaxial cable	twisted-pair wire	coaxial cable	coaxial cable
Maximum no. of connections	512	160	64	64

*Carrier sense multiple access/collision detection
**Carrier sense multiple access/collision avoidance

data bases and access to peripherals too expensive to dedicate to one cluster (eg, laser printers and SNA gateways).

Many local networks encourage contention among users since all users must contend for a single resource—the bus. Fairly inexpensive resources (eg, dot-matrix printers, 5¼-in. rigid disk drives) are connected to the same link as the expensive resources. As a result, it takes as much time to submit a print job to a $600 printer as it would to a $60,000 one.

Cost—the big issue

Clusters promote efficiency by attacking connection costs that approach $1000 per node for typical network implementations. Factors affecting these costs include the number of nodes on the network, network topology, access control method, overall distances that the network must cover, and the transmission speeds needed to support many nodes over extended distances. Faster speeds are needed to shorten delay times between nodes.

Of these considerations, distance and the number of nodes have the most impact. Long distances require extensive transmission medium shielding so that spurious noise from the environment does not disrupt transmission.

This is the major reason that the RG50AU cable used for Ethernet is much more expensive than the RG58AU cable used in Cheapernet. The more expensive version allows packets to be sent as far as 5000 cable-ft. RG58AU, however, limits transmissions to 2000 cable-ft maximum. The less expensive cable cannot be used in noisy environments, such as wiring conduits and ventilation shafts.

Total distance also impacts the number of nodes supported because a minimum gap between nodes (eg, the 36 in. required in Ethernet) is needed for sufficient delay between transmissions. Distance affects transmission speeds in a similar manner by determining the amount of delay incurred in sending a message from one node to the other. Higher transmission speeds (such as the 10 Mbits/s dictated by Ethernet) are needed to support a large number of nodes in geographically dispersed locations.

Network controllers must be more sophisticated (and hence more expensive) when many nodes are interconnected. This is because the probability of collisions rises. Access control surfaces as an issue with more nodes contending for overtaxed bus bandwidth. Prevalent schemes used to handle this challenge—collision detection and token passing—incur significant overhead that may be bypassed if there is a decrease in the number of nodes.

(continued on page 32)

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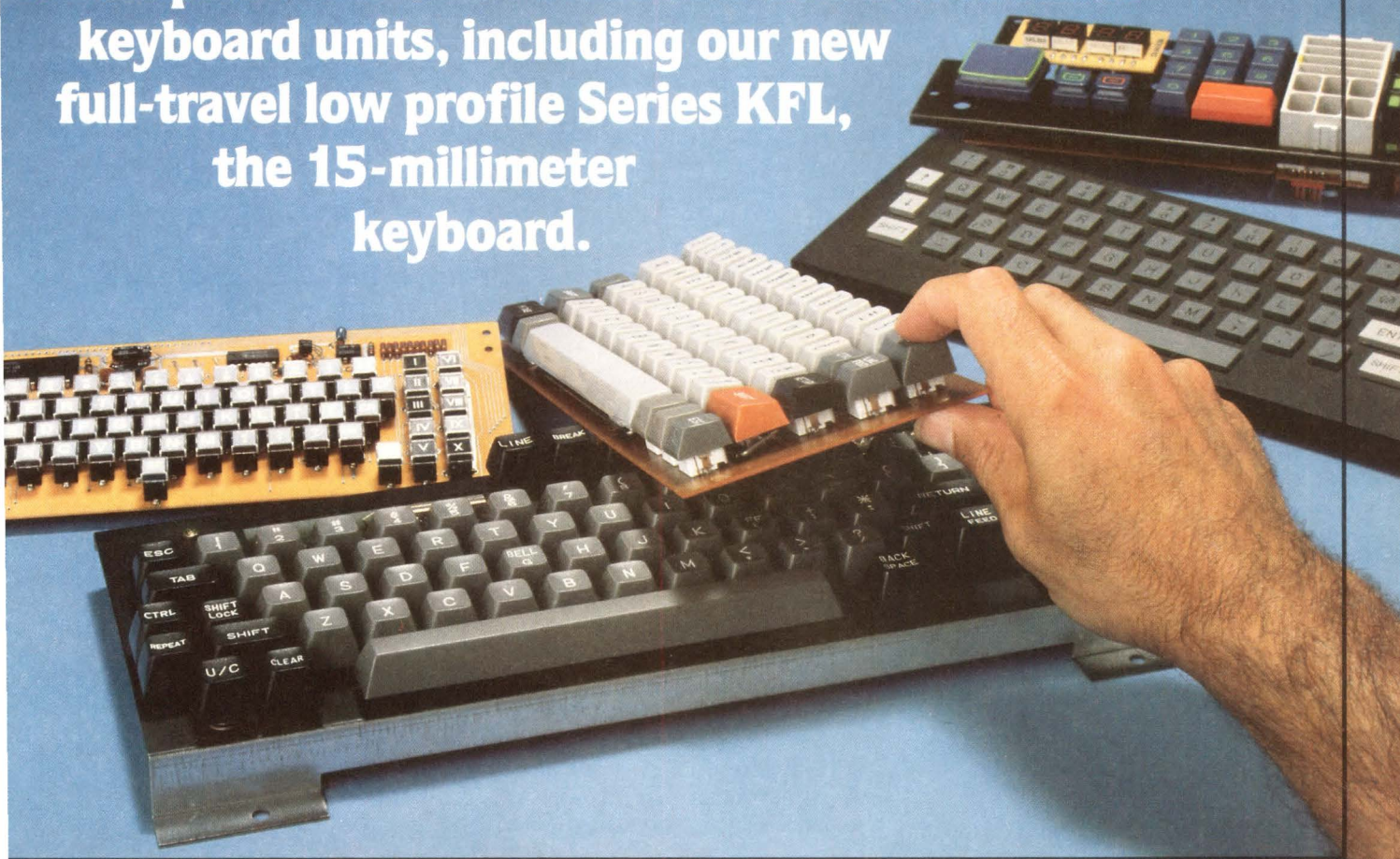

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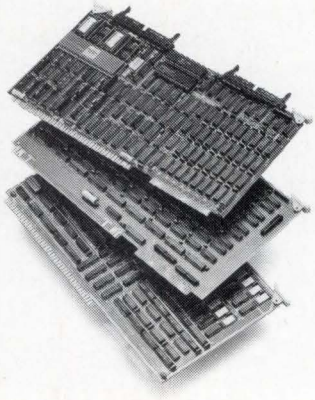

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CIRCLE 17

Simpler clusters emerge

(continued from page 30)

Fewer nodes also mean shorter cable lengths and slower transmission speeds. Shielding becomes less important since the chance of collsion decreases due to shorter distances traveled. Furthermore, terminals and personal computers can also be connected more closely together. Vendors such as AST Research, IBM, and Network Development Corp use these benefits to their advantage and lower connection costs to as little as $200 per node.

Much of this cost reduction comes from the use of cheaper transmission medium (cable TV-type coaxial and twisted-pair wire) and connectors. Simpler controllers can handle the slower transmission speeds (typically 1 Mbit/s) and simplified access control schemes.

Using predefined time slots

Instead of relying on probabilistic schemes that determine access by generating random numbers (eg, Ethernet back-off), the aforementioned vendors allocate predefined time slots to each user. The most popular schemes use the carrier sense multiple access (CSMA) method popularized by Ethernet. But they also employ collision avoidance techniques rather than collision detection.

With collision detection, more than one user can transmit a message concurrently. Errors are detected when collisions create a large voltage on the bus. Collision avoidance schemes, on the other hand, require that a user transmit a message request before actually sending the message. If the message returns without collision, then the user has sole control of the bus for transmission. To prevent one user from hogging the network, both AST Research and IBM Entry Systems Division (PO Box 2989, Delray Beach, FL 33444) implement priority schemes so that time slots are reallocated periodically.

National Semiconductor claims that collision avoidance schemes incur an overhead penalty not justified by traffic conditions. Design manager, R.V. Balakrishnan, says that collision avoidance schemes work best in networks where transmissions tend to be "bursty" rather than sustained, and peripheral services are seldom required. He notes that servicing multiple requests on collision avoidance networks requires that the peripheral wait for its turn, as determined by the priority scheme. Here, collision detection networks are better suited since requests can be serviced as often as each peripheral can transmit a message.

Network Development Corp implements a polling scheme whereby a master station periodically checks each satellite for requests. Multiple transmissions are avoided by allowing variable-sized packets (as large as 4 Kbytes) that fully utilize the timeslots allocated to each satellite.

Clusters can increase high speed network efficiency by handling the bulk of local processing, as well as by packaging individual packets into larger messages. As a result, traffic going across the high speed network would consist of intercluster messages, requests destined for central data bases, or services rendered on expensive peripherals. Thus, clusters and networks can work hand in hand to better serve the user.

—Joseph Aseo, Field Editor

SYSTEM TECHNOLOGY

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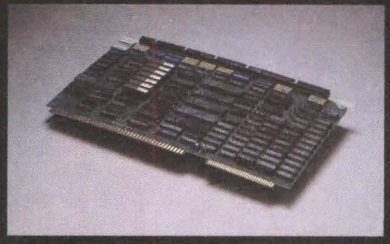

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CIRCLE 18

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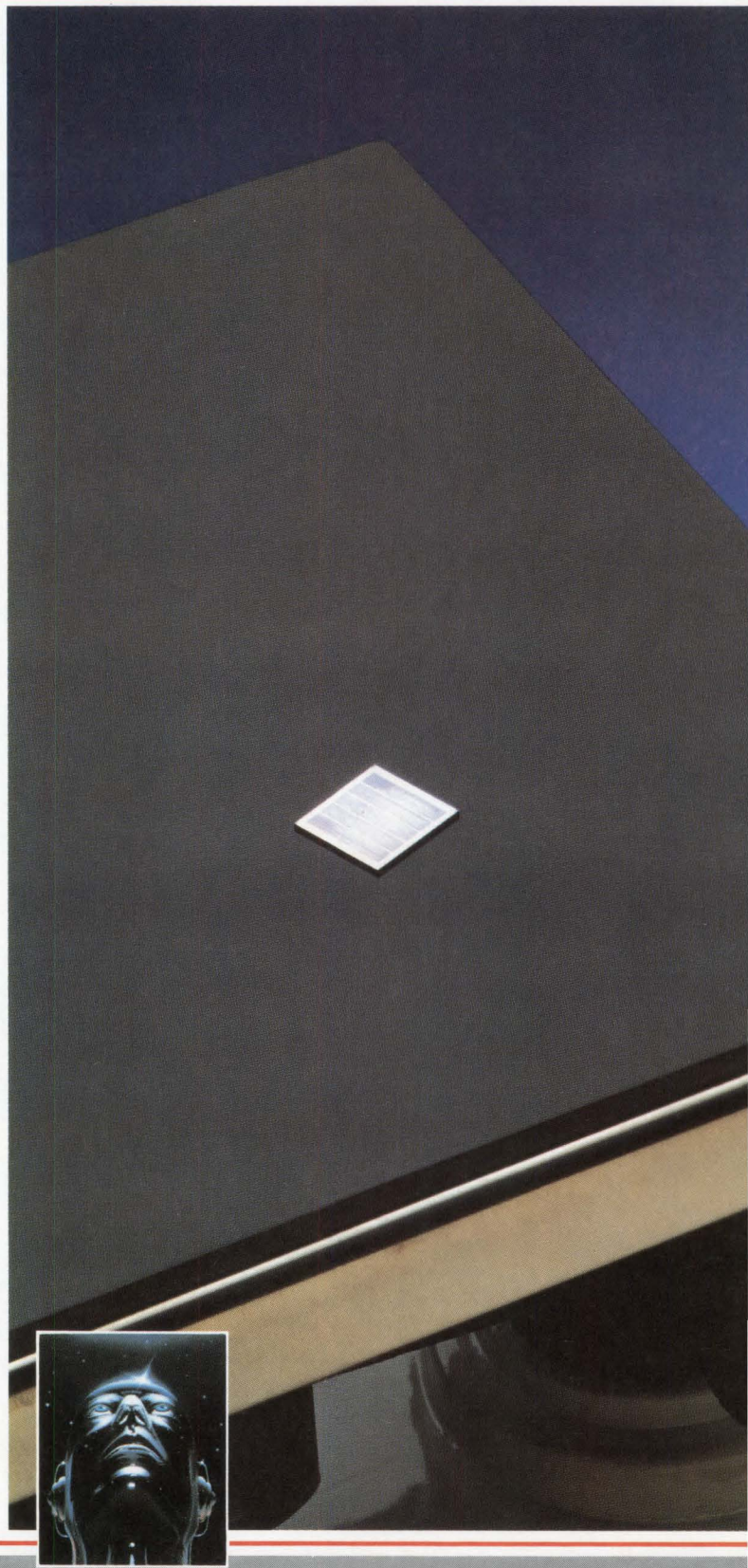

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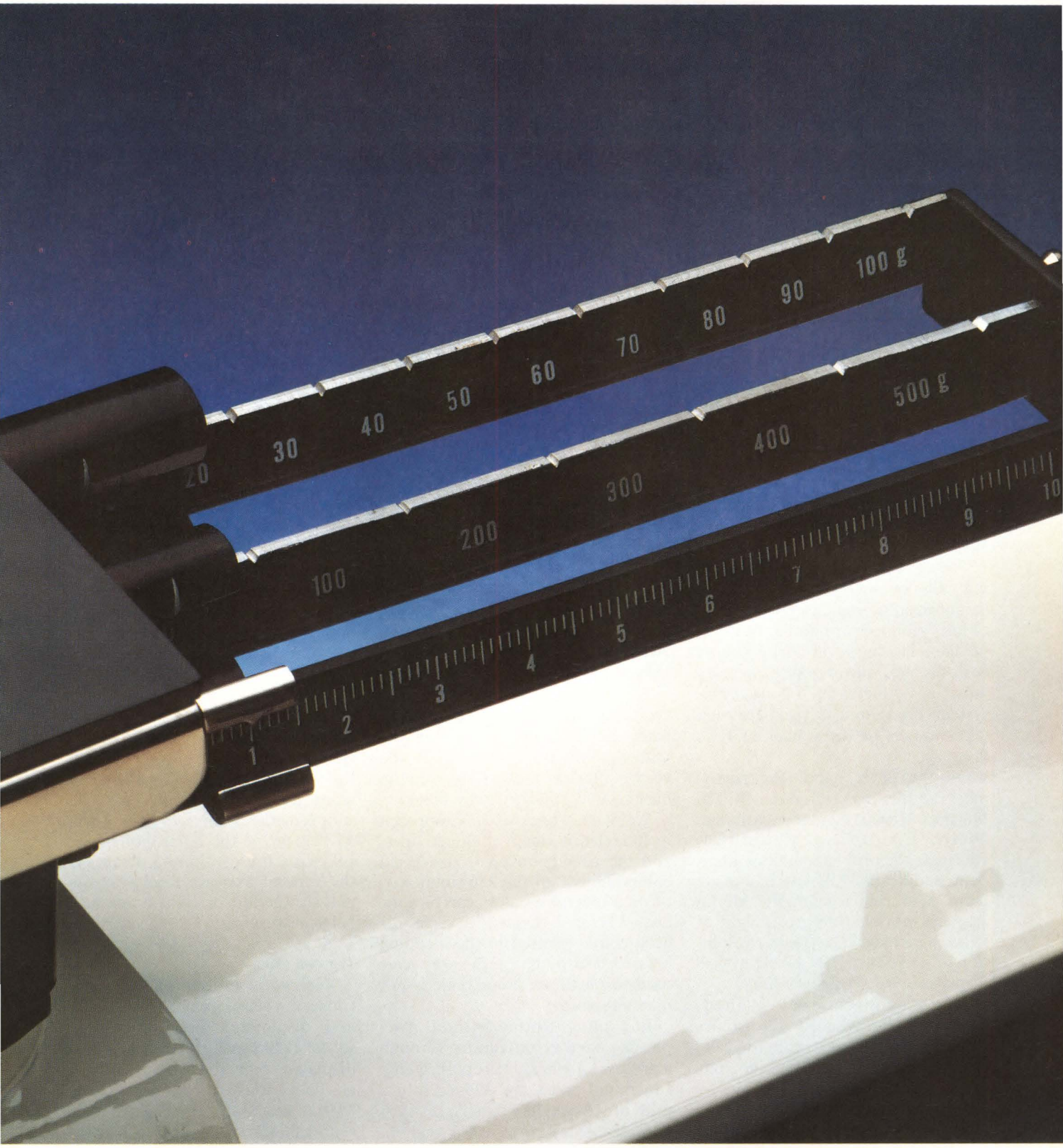

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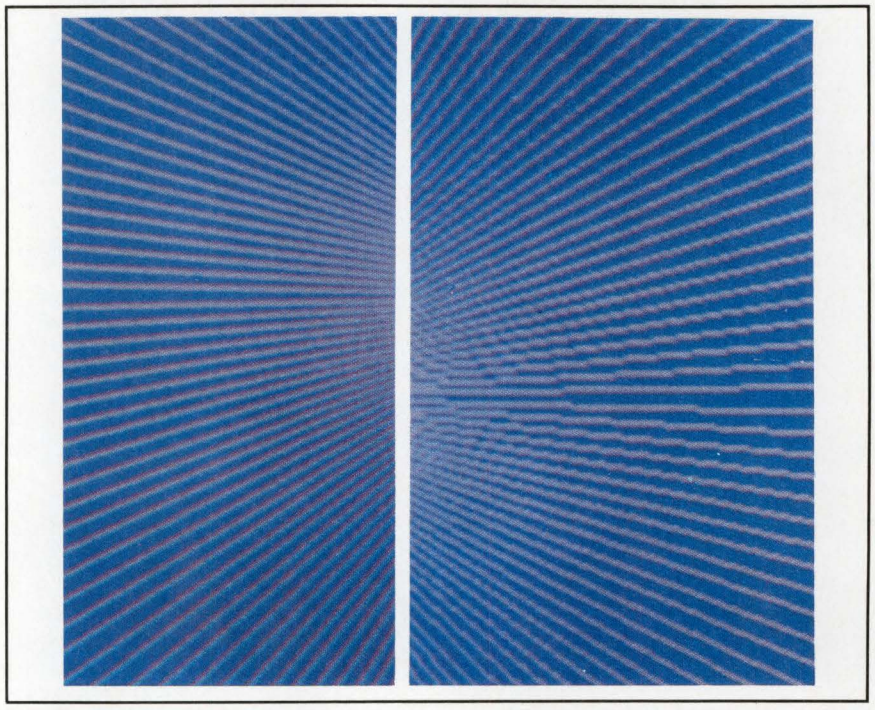
CIRCLE 19

Partial pixel addressing increases effective display resolution

Using a proprietary technique called pixel phasing, a graphics display can provide a significantly clearer image than conventional raster monitors and at little added cost. The technique allows portions of pixels to be addressed in order to smooth jagged lines. Pixel phasing thus overcomes the major disadvantage of raster-scan displays compared to vector drawn displays—aliasing.

Aliasing describes the stepped or jagged lines that occur for oblique lines, typically less than 20 degrees from the horizontal or vertical axis. Since pixel coordinates are locked into fixed locations within the raster plane memory, they cannot deviate from the locations of idealized pixels that lie along the line displayed.



With pixel phasing, a graphics workstation can address portions of individual pixels and eliminate jagged lines. For example, the Merlin 9200 offers an effective resolution equivalent to 3072 x 2304 pixels (left). Using conventional techniques results in vectors as shown on right.

Aliasing solutions versus pixel phasing

The conventional solution to aliasing calls for increasing the vertical and horizontal resolution (ie, number of lines scanned, or number of pixels per line). However, this incurs greater cost because raster plane memory must also increase. In addition, system throughput suffers because it takes longer to draw lines and fill in areas.

On the other hand, the partial pixel addressing technique within Megatek's (9605 Scranton Rd, San Diego, CA 92121) Merlin 9200 addresses the problem without attendant handicaps. Like its namesake from Arthurian legend, the Merlin graphics workstation uses sleight of hand to increase the effective resolution of its 1024- x 1024-pixel physical display to 3072 x 2304 points.

A less conventional method, favored by Advanced Electronics Design (440 Potrero Ave, Sunnyvale, CA 94086) for its AED767 color terminal, optically smooths the lines by blending vector slopes with the background. Firmware resident in the terminal (see *Computer Design*, May 1982, p 24) uses a process called ramping. This process involves a transition from one color to another so that both blend together. The vector slope determines the adjacent pixels to be blended, as well as the individual intensity. As a result, the vector color gradually fades into the background color (usually black).

Major drawbacks to this approach include the fuzziness of altered lines, and the restriction on user-defined colors. Only 8 of the 256 simultaneously displayable colors can be antialiased because 16 intensity values for each color are used in the blending process. Furthermore, the gray scale used to blend the color table is not user alterable.

In contrast to this method, pixel phasing handles antialiasing through a process known as micropositioning. Individual pixels are divided into a grid of 16 smaller subpixels, each addressable within a 4 x 4 grid. In addition, the grid boundaries can be shifted from one-quarter to three-quarters of its width or height.

Consequently, the shape of each pixel can be altered by shrinking or stretching. The pixel can also be shifted to better approximate the slope of the line. Microdeflection of the CRT beam within the monitor alters the vertical displacement of subpixels. This corrects lines within 45 degrees of the horizontal plane. Likewise, lines within 45 degrees of the vertical axis are drawn by displacing the left or right boundaries between pixels.

The real thing

Real-world objects replace visual trickery when it comes to modeling and displaying three-dimensional solids. Unlike many three-dimensional display systems that portray objects as collections of endpoints, the Merlin 9200 stores in its data bases representations that have such attributes as topology, surface texture, and depth. The amount of attribute information associated with the objects is so extensive that shading and hidden

(continued on page 38)

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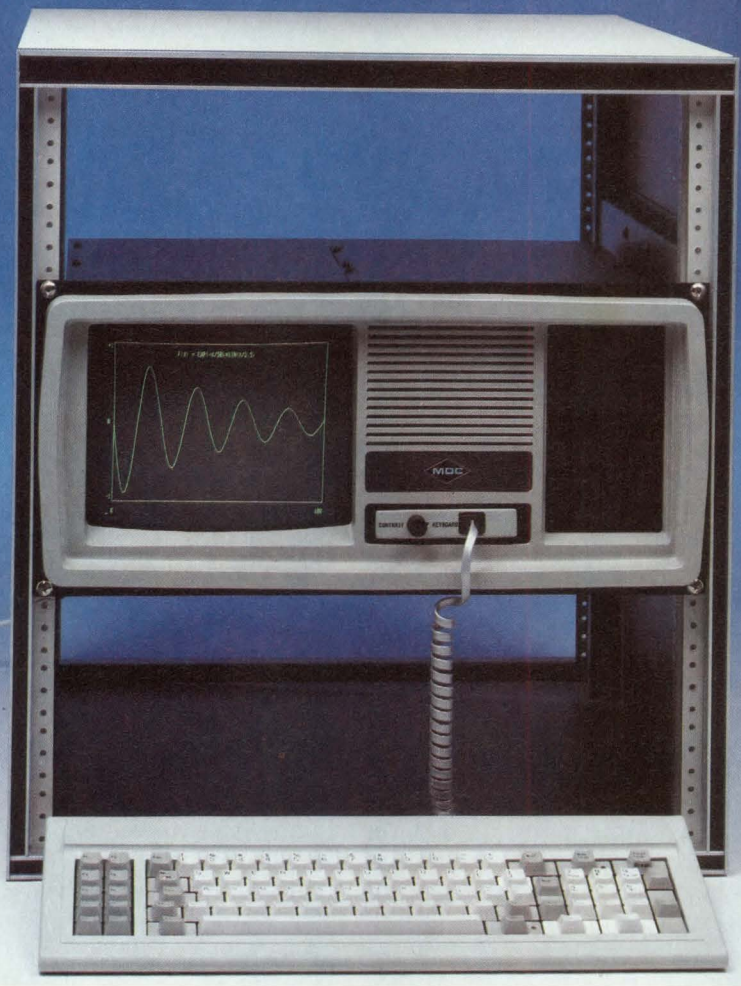

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CIRCLE 20

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CIRCLE 21

Partial pixel addressing

(continued from page 36)

surface removal occur automatically in hardware as objects are rotated or moved.

Typical graphics data bases, as illustrated by the company's own Template package (see *Computer Design*, July 1983, p 66) define real-world objects around a 3-axis coordinate system (ie, length, width, and depth) and as a unique entity (eg, three connected line segments form a triangle). Raster coordinates or vector endpoints generate an image of this object after absolute coordinates (independent of view orientation) are used to describe the image. This display list is what the user actually sees onscreen. Any changes the user makes to the screen do not alter the underlying mathematical model. In other words, raster coordinates are changed, not the mathematical model's coordinates.

This approach's primary weakness is that users must consciously define visible features to remove hidden features. Working with the display list, users must first describe the order in which polygon faces are defined (clockwise or counterwise). Users can then calculate normal vectors to each face, enabling all or a part of the polygon faces to be erased as they point into the screen.

Increased memory requirements

Defining hidden features for many views results in having to store multiple display lists. In addition, changes made directly to the underlying mathematical model require that new display lists be generated and displayed on the user's screen. Memory requirements further increase, because the three-dimensional model itself must be saved at the end of the session.

In contrast, the graphics data base found on the Merlin 9200 more closely resembles that used in the Anvil 4000 (see *Computer Design*, July 1983, p 66) from Manufacturing Consultants and Services (Irvine, Calif). In this case, the three-dimensional model also contains the graphical attributes. Thus, three-dimensional coordinates replace the two-dimensional coordinates that display lists typically use. This means that the physical characteristics (ie, height, width, and depth), geometrical relationships (eg, one face is perpendiular to another), and textual information (eg, parts lists) are all retained.

Even with an underlying three-dimensional mathematical model, implementations such as Template lose attribute information when display lists are generated. On the other hand, users can create classes of objects within the Merlin data base and then produce different versions. They accomplish this by merely altering the display list or the model itself (eg, defining a rectangle and then creating squares). Rather than work with polygon faces that only approximate the object (like Template), users manipulate that object's mathematical definition.

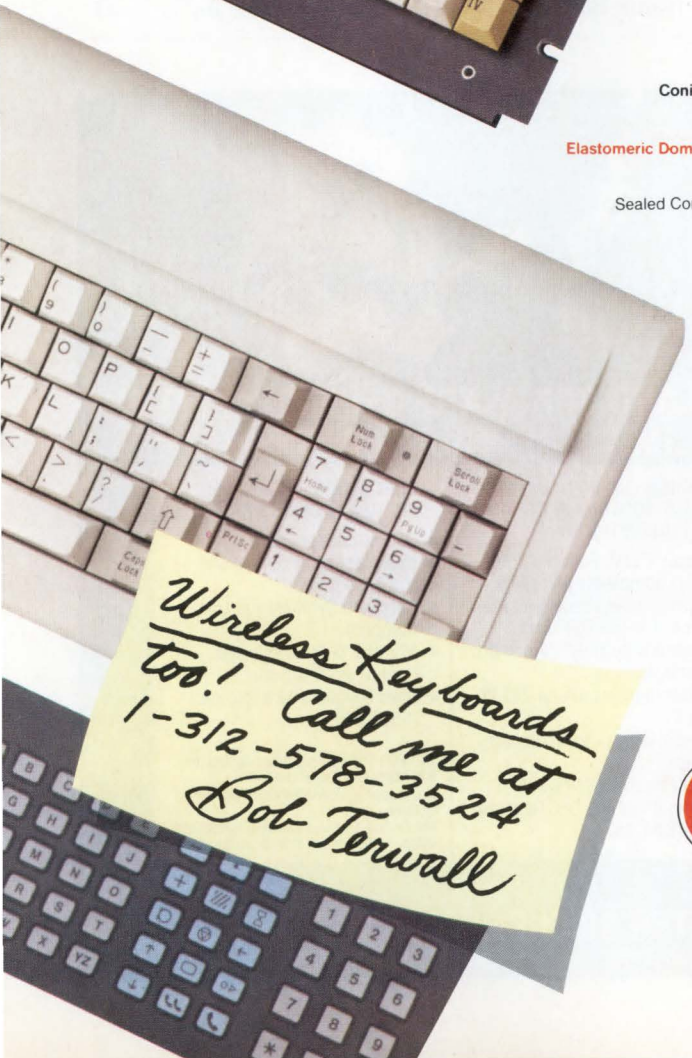
Associating graphics information with the three-dimensional model lets polygon faces hide all or a portion of other polygons without computations. The graphics data base recognizes each view to be displayed. Changes in one view, therefore, do not affect the display of other views.

In fact, the Merlin has a Z-buffer that features depth information on each displayed object. This buffer contains the Z-value (depth) closest to the front of the terminal for each X, Y coordinate. Where there is an overlap, the polygon point closest to the viewer is stored. Consequently, automatic hidden feature removal occurs as objects are translated or rotated to appear in front of each other. The system can also display translucent objects to allow background objects to show through.

Fitting the pieces

The Merlin 9200 distributes processing across several boards linked by a proprietary 32-bit bus. The 80186-based local task processor handles communications with all external interfaces (RS-232 serial ports, Centronics parallel port, floppy disk, and Multibus for memory or I/O expansion) and provides local task execution. An 80286-based database processor manages the local graphics data base, any symbolic references to named entities within the data base,

(continued on page 40)



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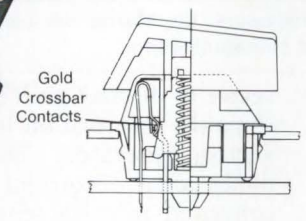

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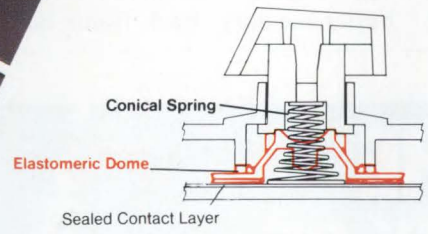

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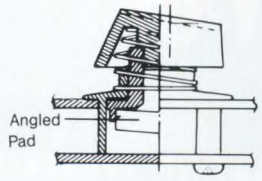

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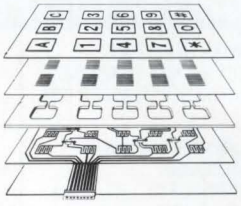

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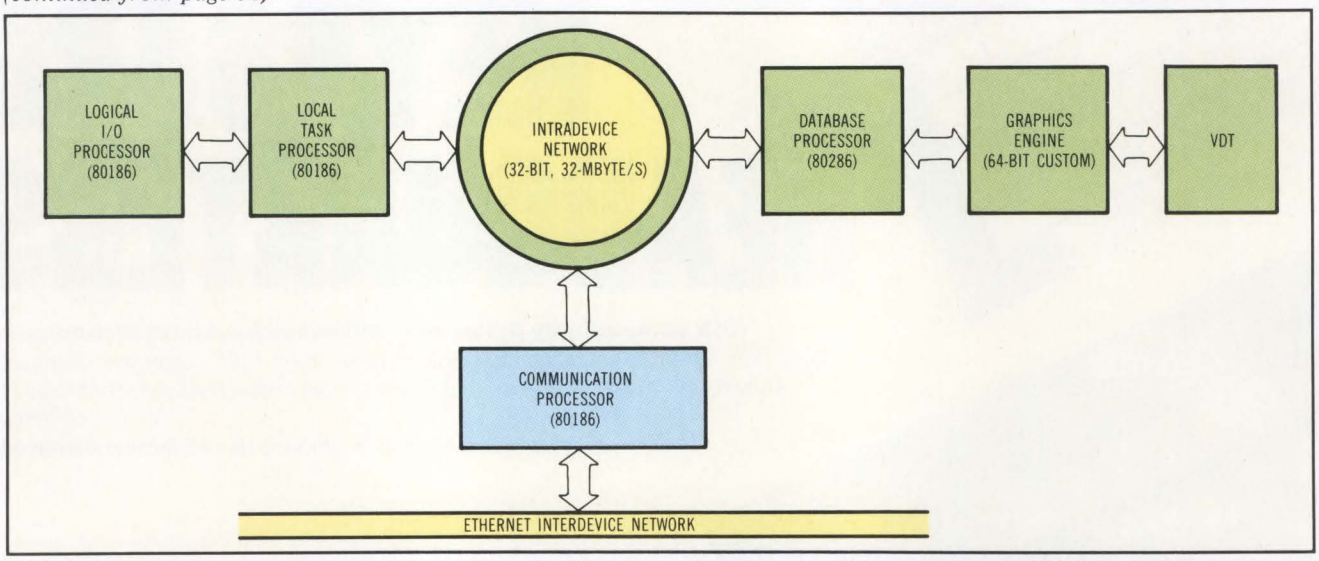
CIRCLE 22

Partial pixel addressing

(continued from page 38)



Distributing functions among several processors, the Merlin 9200 increases parallel processing. A 32-bit backplane serves as the network for interprocessor communications.

as well as graphics editing and text formatting. It also manages the routing of display instructions and data to the raster-display processor.

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—Joseph Aseo, Field Editor
SYSTEM TECHNOLOGY

(continued on page 45)

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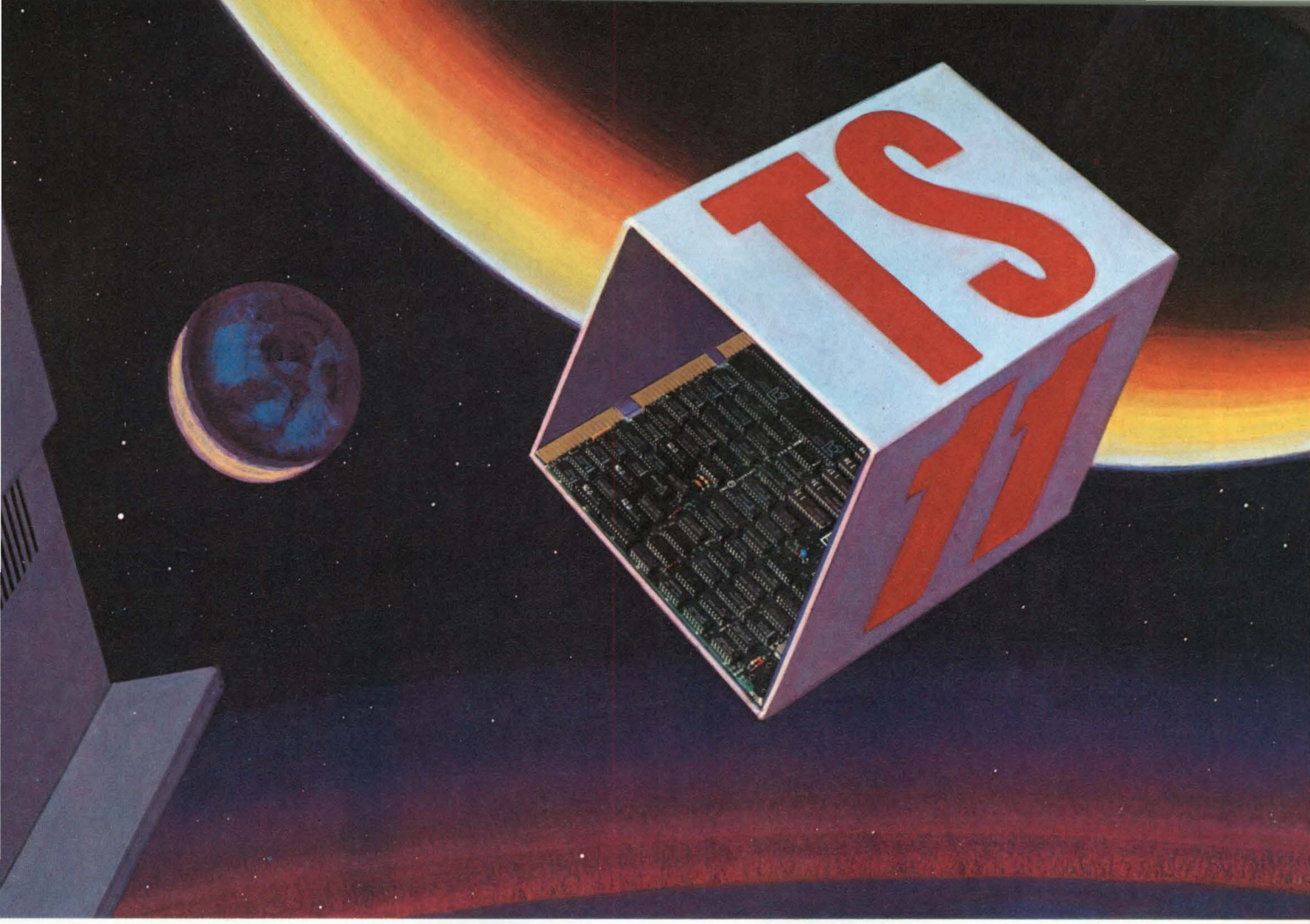

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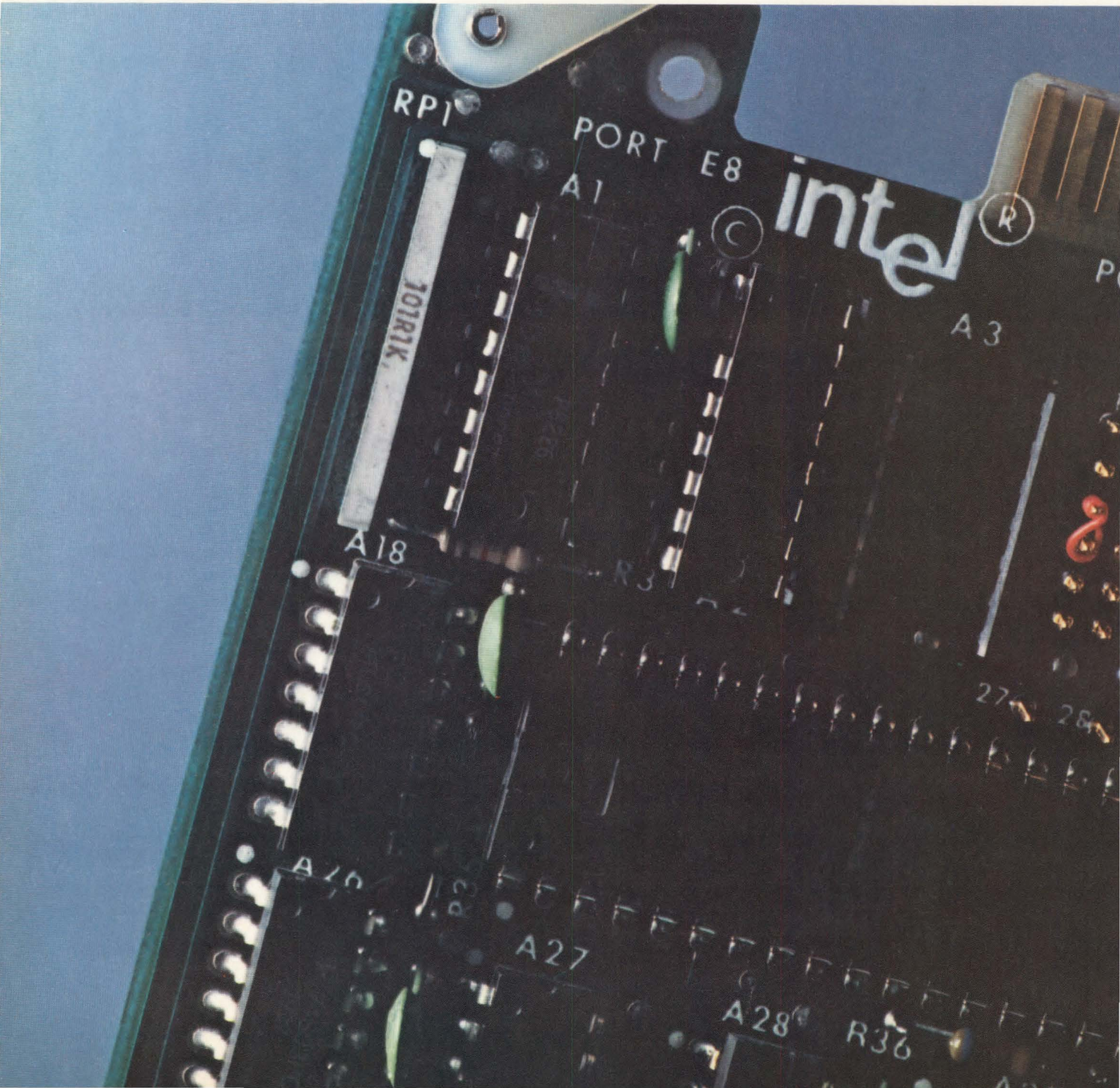

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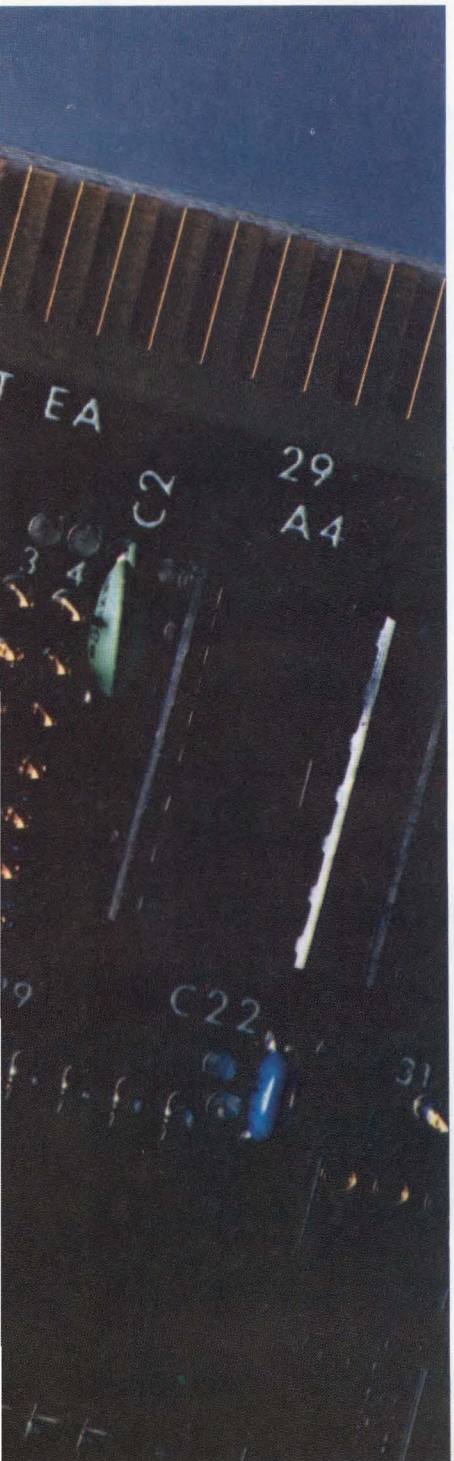

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CIRCLE 25

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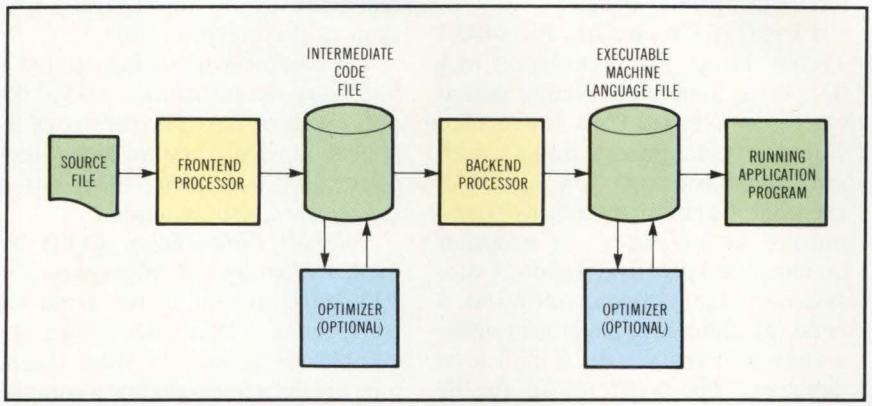
Multistage compilers move from mainframes to micros



Multistage compilers first process source-language (text) files to produce intermediate code files. These files can be further processed for efficiency by an optimizer. The intermediate code file is then processed by a "back end" that generates and (optionally) optimizes executable machine code files.

Although multistage optimizing compilers have been available on mainframe computers for a number of years, they have only recently become available for micros. A recent announcement from Language Processors, Inc, and forthcoming announcements from TeleSoft and Digital Research, Inc serve to illustrate this trend.

There are several advantages to multistage compilers. A multipass compiler creates intermediate code files, which describe the program as written for a simple abstract machine, rather than going directly to machine code for a particular microprocessor. This additional step allows the compiler writer to optimize the program's logic and storage use. Common intermediate code files also let the programmer "mix and match" routines from different languages to produce a given program. An example given by Language Processors includes writing the main logic of a program in Pascal, and including a Cobol routine for handling files.

Writing compilers for many languages also becomes easier. The architecture of the abstract machine, though simple, can be made powerful enough to handle all high level language constructs while still mapping easily onto a given microprocessor's instruction set. Furthermore, for a given microprocessor (eg, the 68000), only one machine language-generating "back end" needs to be written. Frontend compilers for transforming source files to intermediate code files can thus be given more time and attention.

Single-stage compilers generally handle functions including processing the source-code file, optimizing code, and generating machine code. Including these and other functions makes compilers large, complex, and difficult to program and debug. A multistage approach breaks the various functions into separate programs, making the programming effort much more manageable. Such modules are smaller and easier to understand, and more effort can be devoted to making them powerful and efficient.

Global versus peephole optimization

There are two different approaches to optimization—global and local (or peephole). Global optimizers look at the whole program structure, identify and eliminate sections of code that will never be executed, optimize register usage, and generally streamline the logic. Peephole optimizers, on the other hand, generally

(continued on page 46)

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Multistage compilers

(continued from page 45)

look at only a few instructions at a time. These optimizers move constant expressions out of loops and find more efficient machine instructions to perform a given function. In general, global optimizers are more suitable for processing intermediate code files, while peephole optimizers polish and accelerate machine language implementation.

Optimizing causes trade-offs

As with any technique, there are trade-offs in optimizing. The optimizer can be designed to produce fast code (reducing runtime) or compact code (decreasing storage requirements). A balance point exists between the two, and choosing depends on the experience and judgment of the compiler writer or designer. There are trade-offs in the degree of optimization too—the more detailed and thorough the optimization, the more time that compilation will take. Alternately, a fast compiler with an unsophisticated optimizer will produce less than optimal code.

Language Processors, Inc (400-1 Totten Pond Rd, Waltham, MA 02154) has announced compilers that run on 68000-based Unix systems for Cobol, RPG-II, Pascal, and C, with PL/I and Basic to follow soon. All use what the company calls its "component architecture," a modular architecture with five standard subsystems: a front end, an optimizer, a code (machine language) generator, a runtime library, and a high level debugger. The programs all use the same indexed sequential access method (ISAM) to handle data files. Thus, programs written in one language can address and use files written in another.

Common intermediate code files allow integration of routines written in different languages and simplify creation of runtime libraries. A multilanguage debugger recognizes the language in which a particular routine is written, and lets the programmer correct errors at the source level, rather than in the machine code.

The compilers are being offered to hardware manufacturers at $50,000 plus royalties, based on the size of the system on which they are used. Single copies with runtime distribution licenses are also available.

TeleSoft (San Diego, Calif) has made multistage compilers part of its Ada development effort from the start. Since Ada is such a large and complex language, the sheer magnitude involved in developing a compiler for it almost mandates a stage by stage approach.

Building on experience gained with the UCSD p-System, the company developed a proprietary operating system, called ROS. It has since moved on to produce compilers that run under Unix, IBM mainframe operating systems, on the VAX, as well as on the IBM PC and its clones. All of these implementations are presently in beta testing with Department of Defense validation expected very soon.

Digital Research, Inc (Pacific Grove, Calif) has announced its adherence to the philosophy of multistage compilers, and the firm is expected to introduce a C compiler early this summer. The compiler will run under the company's CP/M-86 and, presumably, CP/M-68K operating systems. With the ability of CP/M-86 to emulate MS-DOS, these C compilers should become widespread and affordable.

The company has announced that all of its languages will henceforth have multistage compilers, and be able to exchange object modules. It is also working on the Intel 80286 processor Unix implementation for AT&T, and has announced language and application support for Unix systems. Thus, a great many interesting developments can be expected in the next 18 months.

—Sam Bassett, Field Editor

SYSTEM TECHNOLOGY

(continued on page 48)

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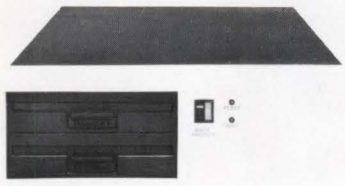

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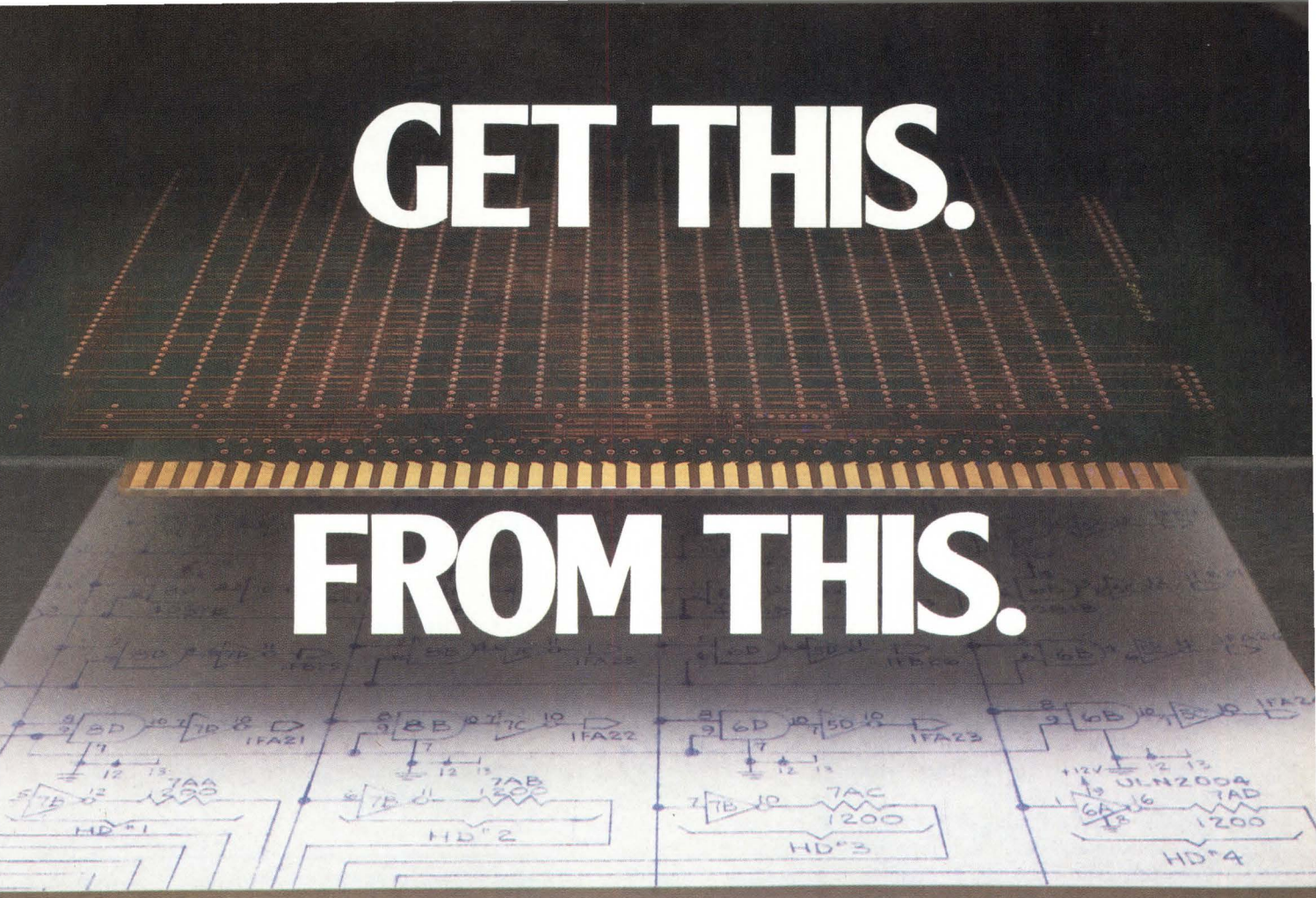
CIRCLE 28



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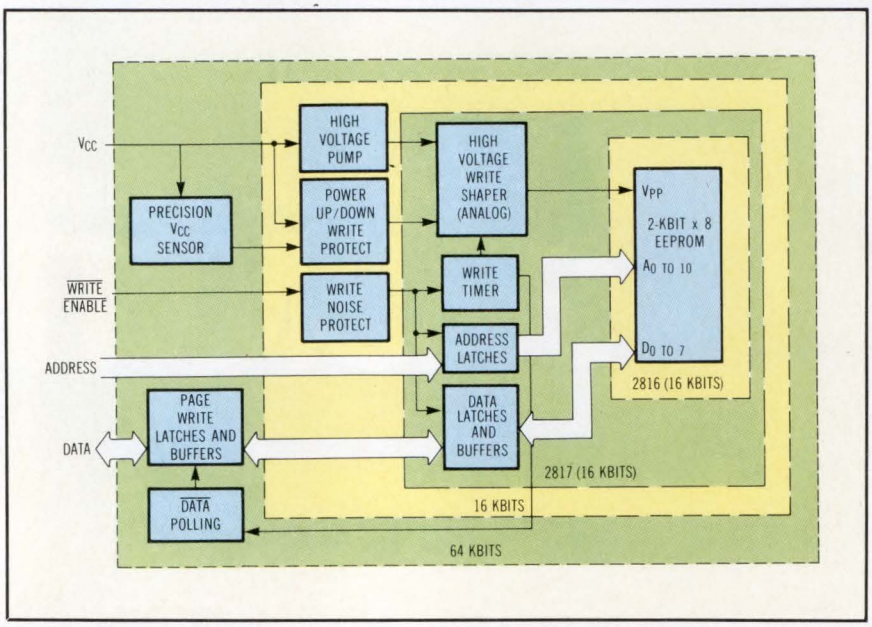
CIRCLE 29

As densities increase, EEPROMs grope toward standards

Electrically erasable PROMs have evolved dramatically in recent years. From relatively simple parts that needed a lot of peripheral support circuits, they have progressed to very dense (now reaching 64 Kbits) devices with most necessary functions contained on a single chip. On the way, a serious lack of function and pin assignment standards led to extensive incompatibility. With the advent of the 64-Kbit EEPROM, however, manufacturers appear to be reaching tacit agreement on most points. Thus, designers may soon be able to select chips based upon the presence or absence of certain features but remain relatively unconcerned with hardware compatibility.

Major issues affecting EEPROMs as they approach higher densities include protecting the device against false writes during power-up and power-down, providing a means of quickly writing the memory, and defining pin 1 in the 28-pin Joint Electron Device Engineering Council (JEDEC) standard package. The issue of pin 1 appears to be the most easily resolved. Some early 64-Kbit announcements define pin 1 as a ready/busy signal for sending an interrupt to the microprocessor when the write cycle is complete, but this may change. Although ready/busy was popular in 16-Kbit versions using a 24-pin package, the 64-Kbit designs tend to preserve their 28-pin site for anticipated 256-Kbit versions. A different method of signaling the microprocessor is used, reserving pin 1 for an address pin (A14) in 256-Kbit designs.



As EEPROM densities have increased, peripheral circuits and features incorporated onchip have grown. Features at the 16-Kbit level evolved through several stages. The 64-Kbit level has demanded even more. (Source: Xicor Corp)

Determining the write cycle complete

Xicor Corp (851 Buckeye Ct, Milpitas, CA 93035) has introduced DATA polling, a software method for determining if a write cycle is complete. A polling method of some sort has become necessary in EEPROMs as density has increased. Given the 10-ms typical write time per byte, microprocessors would be idling for far too long unless they performed other tasks while writing. DATA polling allows the processor to look at the data being written. If a write is still in progress, the buffers return the 2's complement of the data that is being written.

This offers two advantages. First, it frees the processor to perform other tasks during the write cycle. Second, it lets the system optimize the actual time consumed by write operations. Since systems may incorporate relatively large numbers of dense EEPROMs, the savings may be considerable.

EEPROMs are specified at a given time to perform a write, typically 10 ms for a byte, or in the newer parts, for a page of data. Since the devices are self-timed, however, the actual time needed to perform a write may vary over a range of shorter times. This depends on differences in temperature and manufacturing. DATA polling allows the processor to determine when a write cycle is complete without taking up an extra pin for a ready/busy signal.

Some manufacturers (eg, Intel) have assigned pin 1 as a ready/busy pin in their 64-Kbit, 28-pin designs. They apparently expect designs in the 256-Kbit range to use 16-bit word widths. This would require a different package altogether—possibly a 40-pin type.

Cutting write cycle time

The increased densities of EEPROMs have made their use conceivable in an ever-expanding range of applications. However, the time needed to program a single byte has become a major hindrance. At 10 ms per byte, the time it takes to program an entire 64-Kbit part exceeds 81 s. Where smaller devices latched single bytes to free the processor, the newer devices buffer and latch groups of bytes and write each group *en masse* while the processor is busy elsewhere. The method is called page mode.

There is a trade-off to consider here. Most applications do not require that the entire EEPROM be rewritten very often. Each time a group of bytes is changed to alter one byte, the erase/write endurance for the whole group is diminished. Although endurances typically reach 10,000 erase/write cycles per byte, not all designers feel entirely comfortable with that

(continued on page 50)

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SUPER. MICRO.

CIRCLE 30

EEPROMs grope toward standards

(continued from page 48)

figure. This is especially true in the newer application areas that are opening up for the larger capacities.

The page mode approach is thus a compromise between the desire to gain speed in writing data to the EEPROM and the reluctance to use up a given byte's erase/write cycle allotment. The balance seems tilted in favor of speed in writing data. Page sizes for Intel's projected 64-Kbit device and Xicor's 2864A are 16 bytes. The Inmos 48C64, on the other hand, and the Advanced Micro Devices AMD 2864 will have 32-byte buffers. A 64-Kbit part from Inmos, the 3630, sports a 64-byte page size.

Time savings for write operations using page mode can be dramatic. Xicor, for example, specifies a write cycle time of 5 ms. By latching and writing data 16 bytes simultaneously, the time to completely write 64-Kbits is cut to 2.5 s. EEPROMs with 32-byte pages would, of course, require half that time.

One manufacturer, Exel Microelectronics (2150 Commerce Dr, San Jose, CA 95131) has opted to dedicate its pin 1 to a special status word ($\overline{SW}$) function. This locks its 28-pin package out of the 256-Kbit arena, but gives it extra software features to support page mode in its 64-Kbit XL48C64. A set of onchip registers can be read or written by the microprocessor when $\overline{SW}$ pin 1 is low. This allows the chip to supply ready/busy status information to the processor when it reads a register during $\overline{SW}$ active. The processor can also write commands into the XL48C64 to set it for page, fast write, or chip erase mode.

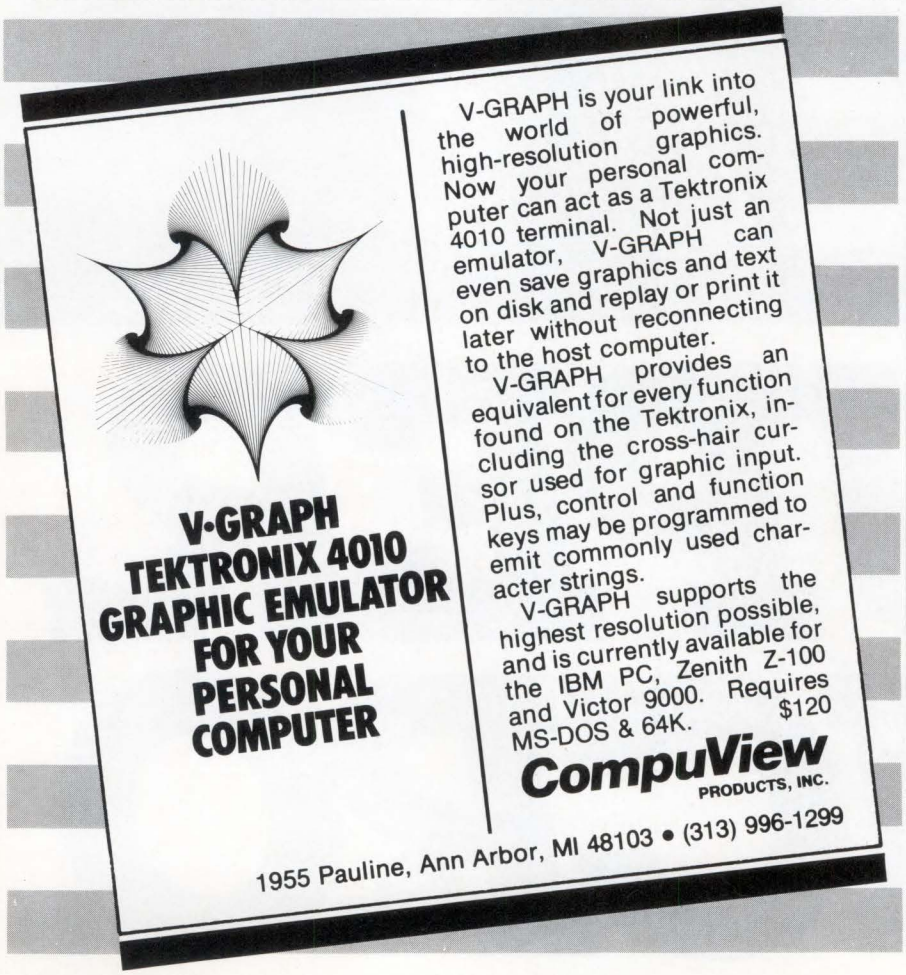
Banning unwanted writes

Protecting an EEPROM against inadvertent writes during power-up and power-down calls for a combination of voltage threshold sensors, noise filters, and timeouts. In addition to disabling write functions until the memory reaches V_{CC}, it is necessary to keep the write disabled for a certain amount of time thereafter to allow V_{CC} to settle. Intel and AMD for example, disallow writes if V_{CC} is below 4 and 3 V, respectively. Xicor has implemented a precision V_{CC} sensor that the user can use to set the threshold voltage by writing and locking an EE cell.

These companies also include a typical power-up timeout of 100 ms on initial power-up before the chip can be written. Thus, Vcc can become stable and noise does not initiate an unwanted write. Exel makes use of its status word pin by requiring that a pattern be written into a register that enables the charge pump to provide the 21-V programming voltage from the 5-V supply before a write can take place. An inadvertent write on power-up cannot take place because the registers are static, but the chip must be initialized.

It appears that, although higher density EEPROMs are inducing agreement about onchip features, there are several areas of choice among hardware-compatible parts, and areas of noncompatibility still exist. Users of the 28-pin JEDEC packages can be reasonably sure of hardware compatibility at the 64-Kbit level. There will, however, be software considerations in the use of Xicor's $\overline{DATA}$ polling and Exel's status word. As densities move to the 256-Kbit level, two distinct approaches are emerging. One will retain the 28-pin device using pin 1 for an address line, while those manufacturers who have already played their pin 1 card will pursue a different packaging arrangement.

—Tom Williams,
West Coast Managing Editor



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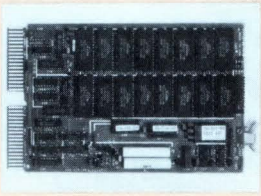
New Dual Height Function Cards For Q-Bus Boost Density And Performance For Data Acquisition And Control.

ADAC continues to expand the industry's widest line of function cards for Q-Bus (LSI-11 and MicroVAX compatible). The most recent additions represent significant advancements for high speed data acquisition, both in terms of improved performance and lower system costs.



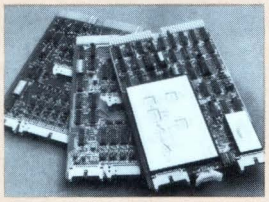
Battery-Backed 22-Bit Address CMOS RAM Improves Density 4 Times. PROM Board Added.

In its maximum configuration of 128K bytes, Model 1822CMOS provides 4 times the density previously available. Model variations from 32K to 128K bytes are offered.

Compatible with 16, 18 and 22-bit addressing, Model 1822CMOS features on-board batteries and power loss protection for 30 days or more. Batteries have a minimum 3 year life.

Model 1822PROM, another new high density memory board (to 512K bytes), is compatible with 16, 18 and 22-bit addressing backplanes Sixteen sockets accept EPROMS or ROMs of 2K × 8, 4K × 8, 16K × 8, and 32K × 8 configurations. Ideal for non-volatile program storage, 1822PROM can be used to configure unattended systems on automatic re-start after power interruption.

Both boards can be selected for addressing at any 4K boundary by switches on the edge of the board, that are accessible even when the board is in the backplane. For volume buyers, combinations of battery-backed CMOS RAM and PROM are available on a single board. CIRCLE 32



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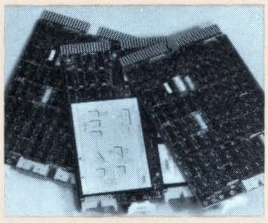
Inputs can be unipolar or bipolar with 8 software programmable gain settings and software selection of thermocouple cold junction compensation. CIRCLE 33



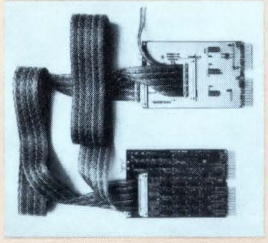
SILO A/D Provides Continuous Performance At 100 kHz.

A new ADAC three-board subsystem provides continuous data sampling to memory, for up to 16 input channels, with 12-bit resolution, at up to 100 kHz aggregate throughput. The 1023S consists of a high-speed, high-level A/D converter card with 64-word SILO buffer, coupled to two 1622 direct memory access controllers. A set of RT-11 installable software drivers is included.

The SILO buffer permits continuous conversion independent of CPU activity. The use of the two DMA controllers eliminates the latency induced by single controller initialization at the end of a buffer completion cycle. While one controller administers data transfers from the A/D over the system bus to memory, the other 1622DMA is available to be set up for the next buffer interval.

The A/D converter board features software gain selection of 1, 2, 4, and 8. An optional board allows expansion to 64 input channels.

Unique in its 22-bit addressing capability, the 1622DMA is available separately and in support of other ADAC A/D and parallel TTL interfaces. CIRCLE 34



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With high noise immunity, controlled rise times and on-board arbitration for both DMA and levels of interrupts, the 1953 offers plug-in ease of bus expansion. CIRCLE 35

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State-of-the-art...new developments...impact of technology...Such buzzwords and phrases abound in the little preconference information available on the NCC '84 technical program. As usual, the program seems to be a mixed bag, covering a wide range of interest areas.

There are a number of tracks of particular interest to the computer-based system designer. For example, among the program tracks included are Hardware and Architecture, Computer Communications, The Automated Office, and Artificial Intelligence. According to conference chairman Russell K. Brown, all sessions are chaired by "leading professionals" and "each will address contemporary issues critical to the industry." A sampling of both session organizers and topics confirms this. Certainly, the session titles and available abstracts promise that many sessions in at least the four program tracks mentioned above could be worthwhile for the system designer.

The exhibit portion of NCC '84 is a far different and far more promising matter. More than 650 companies have contracted for exhibit floor space. Unless NCC '84 differs entirely from previous NCCs, this area will be one of the most important for system designers.

Many U.S. (and a number of foreign) companies choose NCC each year as the site to introduce their latest products. Each year, somewhere on the exhibit floor—with appropriate fanfare—or quietly at private suites in nearby hotels, at least two or three truly notable new products are introduced. In addition, exhibitors display hundreds of important, but not necessarily revolutionary, products. Usually, the exhibit floor products are at or near production stage, while most of the suite introductions are of prototypes and may be shown only to a limited number of special viewers.

A sampling of the information on "to be introduced at NCC '84" products indicates that this NCC will follow the trends of previous ones regarding new products. A special section in the June 15 issue of *Computer Design* will describe most of these products—at least those that companies will discuss prior to the conference.

Of course, many other products will not be announced until the conference begins, but they will be on exhibit at the respective booths. Unfortunately, attendees will have to locate them on their own. As for the private showings, attendees will need to check out the perpetual rumors to determine which are real, and then find a way to view the actual products.

The technical program in brief

Concentration within the Hardware and Architecture program track will be varied. Yet, the one subject that will appear most noticeably is the 32-bit microprocessor. In particular, the architecture of both existing and near-future chip sets will be discussed. For example, one session (on Tuesday morning) will compare the architectures of five chip sets: two from Hewlett-Packard and Western Electric that are available only for proprietary products, one from National that is now in production, and two from Zilog and Motorola that will be available late this year or in 1985. (For a thorough discussion of 32-bit microprocessors, see the article "Architectural advances spur 32-bit micros," by John Bond, Senior Editor, on p 125 of this issue. The next session in this track on Tuesday morning concentrates on proposed standard P754, Draft 10.0, which is accepted by at least three of the now commercially available or near-future 32-bit microprocessors.

This program track will not ignore supercomputer systems and the "fifth generation." On Wednesday, discussions will include the parallel characteristics involved in operational supercomputers and the necessary upward compatibility of future systems. That will be followed by a review and update of the predictions made at NCC '83 on fifth-generation computers.

Computer Communications will address several key phases of that segment of the industry. Dominant in the discussion areas will be networks—local area, multi-vendor, and the necessary integration. But, much emphasis will also be on protocols involved and computer integrated automation with personal computers. As an example, a two-part session will concentrate on the need for manufacturers to coordinate their product designs to alleviate the problems of multi-vendor networks. These sessions will be tied to exhibit floor

(continued on page 56)

(continued from page 55)

demonstrations sponsored by the National Bureau of Standards, Boeing Computer Systems (with 13 vendors), and General Motors (with 7).

Office automation is another important subject for system designers. For example, as was discussed thoroughly in *Computer Design's* Special Edition on "Office Systems Design" (Fall 1983), the automated office involves system designers at almost all levels. Included as elements (ie, products) are the many systems and subsystems common to all computer-based systems: computers, disk drives, printers, terminals, and so on. System designers must be aware of both direct and associated technologies. For instance, designers must include considerations such as ergonomics and artificial intelligence either directly or indirectly into any office system design. It is impossible to ignore either the human element or the hardware/software aspects.

In line with this, participants in the program track on The Automated Office will concentrate their discussions on the design of office systems—in particular, the influence of the microprocessor on such systems. Voice technology (ie, voice messaging, voice synthesis, and voice recognition) and the future impact of such expected advances, will therefore be a key session (on Tuesday afternoon).

A focus on artificial intelligence

At least since the World War II era, and the crushing need to develop automatic cryptographic deciphering techniques and devices, artificial intelligence has been almost as cryptic a term as its initial application. Now, however, at least some phases of AI are attaining various levels of feasibility. Some could even be considered to be practical.

This phase of computer science, which enables some degree of symbolic reasoning and problem solving ability to be attained by mechanical/electronic devices (eg, robots) must be considered in any attempt to design equipment for the present as well as future systems. Closely tied to AI, however, is computer or machine vision. In many applications both must be included in the system design considerations.

The NCC '84 program track on Artificial Intelligence will include discussions of both AI, *per se*, and computer vision. In particular, a Monday afternoon session on AI techniques for signal interpretation is scheduled. Additionally, a Wednesday morning session will present applications of AI to the field of "expert systems." This session will evaluate several representative expert systems along with examples of their usage. Further discussions will encompass natural languages and interfaces to software systems. One session, for instance, will emphasize the importance of a computer's ability to respond to commands and questions in English. Still other sessions in this AI program track will discuss tools for commercial AI systems, software engineering techniques, and the impact of AI on fifth-generation systems.

Professional development seminars

Concurrent with the series of conference technical program sessions will be a series of 18 full-day professional development seminars. As with the program tracks, several of the seminars will be of value to the system designer. For example, the Monday seminar on Artificial Intelligence will cover language, expert systems, and fifth-generation computers in the morning; computer vision, brain, and robotics in the afternoon.

Wednesday seminars of interest include one on Software Engineering with Ada, and another on Introduction to Computer Graphics. The Ada seminar will cover both the language and its applications as they relate to the principles of modern software engineering. A full range of computer graphics aspects will be discussed in the second seminar, which focuses on the making and managing of pictures with computers. (As an example, see the front cover of this and previous issues of *Computer Design* of the past few years.) Portions of this seminar will tackle important developments in the field: data representation graphics, graphic arts, computer aided design and drafting, decision support systems, and system design.

Two other seminars, on Thursday, show promise. The first is on Super Computers: Why They Are Needed and Where Are They Useful, and the second on Local Networks. The Super Computer seminar first will provide an overview of the history and evolution of fifth-generation computers and will define just what a supercomputer is—from several different viewpoints. Then the attendees will learn of future trends, architectures, hardware, software, and applications, as well as the advantages and disadvantages of special purpose versus general purpose computers. In the Local Networks seminar, speakers will cover both equipment and system developments. The scope will include introductions to concepts, and illustrations of how those concepts can be implemented, as well as trends in both the technology and available products.—*S.F.S.*

NCC is sponsored by the American Federation of Information Processing Societies, the Association for Computing Machinery, the Data Processing Management Association, the IEEE Computer Society, and the Society for Computer Simulation. For further information, contact AFIPS. 1899 Preston White Dr, Reston, VA 22091. Tel: 703/620-8952.

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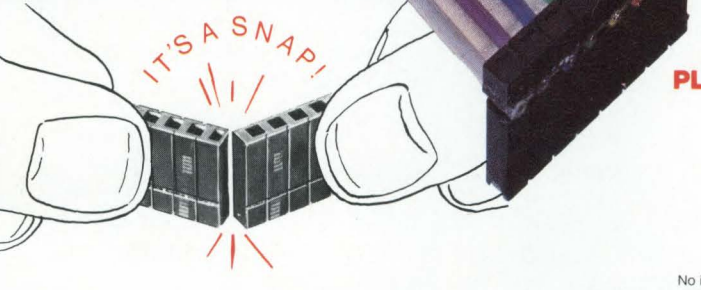

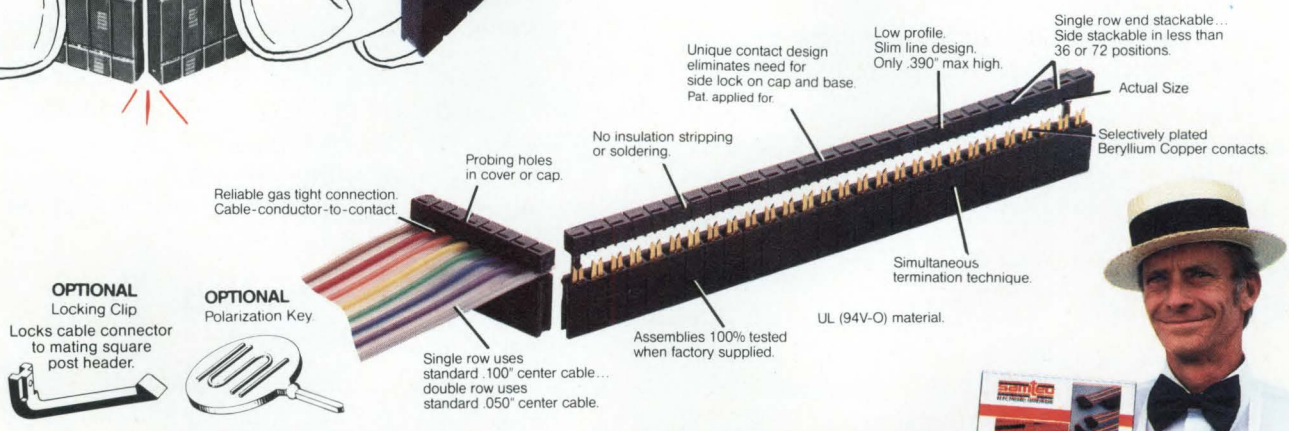

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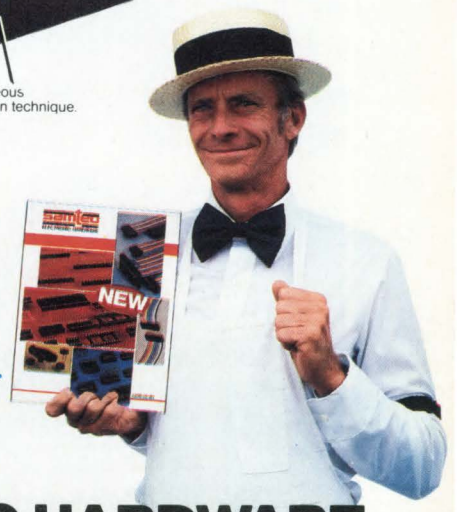

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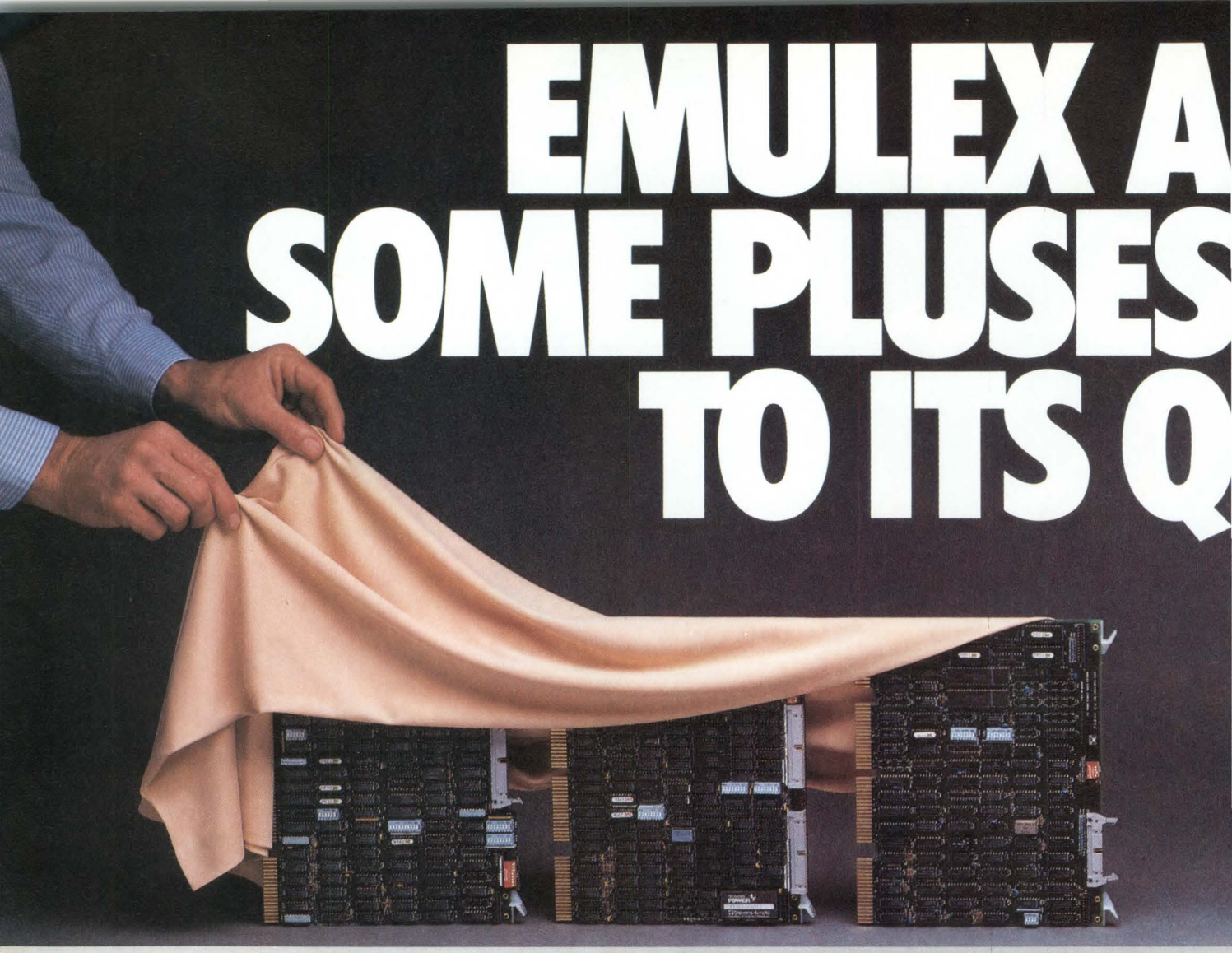
CIRCLE 37

EMULEX A SOME PLUSES TO ITS Q



New UC02 emulating host adapter using Mass Storage Control Protocol (MSCP).

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CIRCLE 38

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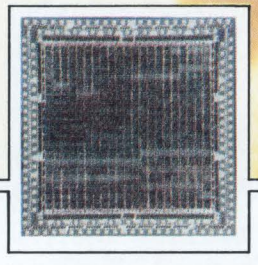

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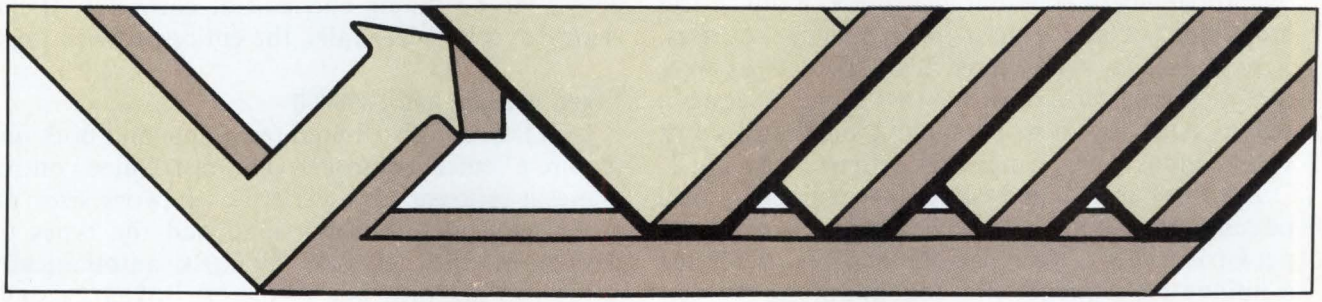
CIRCLE 39

LOCAL NETWORK RESPONDS TO CHANGING SYSTEM NEEDS

A local area network that dynamically adjusts to changes in the nature and volume of system traffic ensures that devices can obtain timely network access.



by Ashraf M. Dahod

Today's local area networks must often work with a variety of device types and handle a wide range of data traffic capacities. Unfortunately, most local networks are optimized to handle a narrow range of network conditions and prove to be inefficient in many commonly encountered operating situations. One local area network, however, dynamically adjusts to changes in the nature and volume of system traffic to maximize efficiency.

Before examining the details of this network, note that most commercial local area networks (LANs) are developed to serve specific types of user devices and data traffic. For example, devices that must perform highly time-critical, synchronized operations need a network that ensures access at preset, specific times. On the other hand, nonintelligent terminals typically generate short, burst-like data streams. Such devices require low access delays but do not need a LAN that provides time-specific access. Stressing the importance of yet another network characteristic, devices that must pass large static data files back and forth are best served by networks that do not devote undue resources to bus contention issues.

Unfortunately, the devices found on a single network might include dumb terminals, graphics systems, printers, common files, intelligent workstations, and mainframes. Each of these could benefit from different and often mutually exclusive network characteristics. The wide range of data traffic capacities further complicates the situation. Appropriate network operation at 20 percent of the maximum traffic capacity may be wasteful at 85 percent. Moreover, a single network device may be used in different ways, each requiring a different type of network access. A personal computer, for example, might transfer files at one time and then emulate a host computer terminal at another.

Ashraf M. Dahod is chariman of Applitek Corp, 107 Audubon Rd, Wakefield, MA 01880. He holds a BS in electrical engineering from the University of Michigan, a BS in physics and mathematics from the University of Bombay, an MBA from Harvard, an MS in engineering management from Northeastern University, and an MS in electrical engineering from Stanford University.

Methods for network access

Overcoming the drawbacks of LANs that provide optimal service only within a limited range of network conditions, Applitek's UniLAN incorporates the firm's UniLINK universal access method, which offers the benefits of three commonly used access methods: carrier sense multiple access with collision detection (CSMA/CD), token passing, and slotted-time division multiple access (STDMA). A brief look at these techniques can illustrate the

benefits and drawbacks of each and provides background for considering UniLINK's operation.

CSMA/CD, a distributed technique, provides immediate access and permits variable message length under low network loads. CSMA/CD is efficient for networking devices (such as nonintelligent terminals) that infrequently send messages. To avoid data collisions, CSMA/CD requires that each device listen to the network. When a device is ready to transmit, it proceeds with its message only if it does not hear another device transmitting. If, while transmitting, it hears another device transmitting, both devices stop and wait for a random amount of time before trying to transmit again. This random back-off time ensures that one device will subsequently gain access.

With CSMA/CD, devices can obtain immediate network access if the traffic load stays low. However, the probability of collisions increases as more devices are added, or as the message frequency increases. Ten years ago, when most network devices were nonintelligent terminals, CSMA/CD was adequate, but as networks began handling file transfers or synchronous devices, network efficiency declined.

Another distributed access technique—token passing— provides each device with a guaranteed network access. Token passing involves circulating a unique bit sequence (the token) among the network nodes in a specific order. Only the node that holds the token has network access. Because a node wishing to transmit must wait for the token before it can transmit, the method's efficiency drops when the traffic load is light. Furthermore, the explicit passing of the token makes the technique complex to implement and limits the maximum number of devices on a single network.

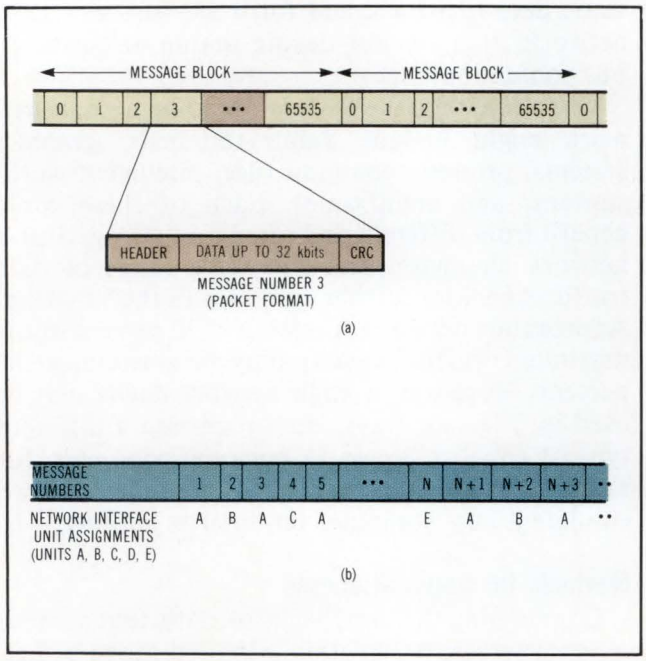


Fig 1 The UniLINK scheme divides time into numbered message blocks allocated to specific network interfaces. Each message includes a header, data, and cyclic redundancy check (CRC), as shown in (a). UniLINK operates on either a contention or dedicated basis. In the latter type (b), assigning more message numbers to certain interfaces gives these interfaces priority, thus improving on typical CSMA/CD schemes.

The third technique, STDMA, is a centralized access method that suits applications involving highly synchronized operations and those covering long distances. STDMA breaks the available network time into slots of equal duration and assigns these slots to specific devices. A device can send messages only for the duration of the time slot; if a message requires more than one slot, it must be broken up, transmitted in several slots, and reassembled at its destination. If a message requires less than one time slot, the remaining time in the slot is wasted. STDMA requires a central synchronizer, which allows all the devices on the network to detect the beginning and end of each slot. If the central synchronizer fails, the entire network fails.

Token passing and CSMA/CD

UniLINK is a distributed technique and does not require a central controller. This distributed control makes it efficient for a variety of network sizes. In accordance with network load and the types of devices on the network, UniLINK automatically adjusts to perform like CSMA/CD, token passing, or a combination of the two techniques. It supports variable- or fixed-length message packets, as does the STDMA technique. Thus, UniLINK can support the longer distances associated with STDMA.

UniLINK requires that user devices follow a set of rules on the network. Time is divided into message blocks, as shown in Fig 1(a). All messages—defined here as the times during which packets can be transmitted—are implicitly numbered and allocated (via a process called automatic message number allocation) to the network interface units. These units connect user devices to the network and keep track of the current message numbers. A device can transmit a fixed- or variable-length data packet only during the message whose number has been assigned to its network interface.

A technique known as pacing, which any network interface can perform, allows each interface to keep track of current message numbers. An interface becomes a pacer when, on power-up, it hears no activity and sends a block synchronization message that returns with no collision and no error. The pacer then sends out a block synchronization message within each message block. This allows each interface to keep an accurate count of message numbers. When the count value equals a certain interface unit's allocated message number, that interface is in pace and can transmit.

Messages are assigned on a dedicated or contention basis [see Fig 1(b)]. Assigning a message number to only one interface unit results in a

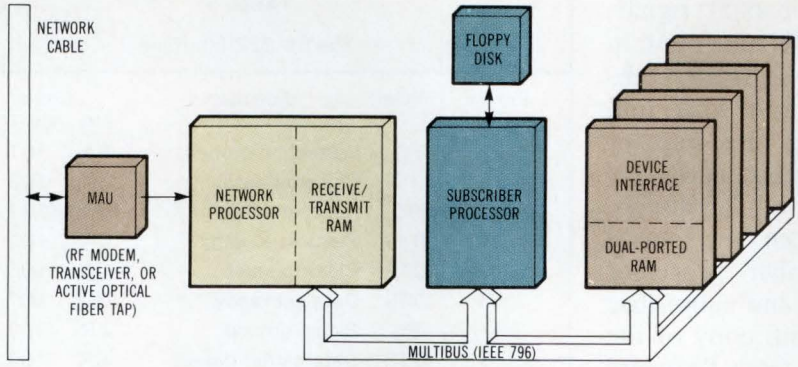


Fig 2 The network interface implements UniLAN's UniLINK access method and provides eight ports for connecting user devices to the network. The network interface consists of a media access unit (MAU), a network processor, a subscriber processor, a device interface, and a floppy disk.

dedicated message because only that unit can use the corresponding message to send information over the network. In contrast, a contention message number is assigned to more than one interface unit. Those units must contend for that message's use. Moreover, each interface unit can have multiple numbers assigned to it.

As in CSMA/CD, when an interface unit detects a collision, it stops sending and waits a random length of time before trying to send again. If a dedicated message number assigned to that interface comes up before the random wait period ends, the interface will use the dedicated message to transmit.

In contrast to the CSMA/CD technique, UniLINK's ability to assign dedicated message numbers significantly reduces delays caused by collisions and random waiting. Simply assigning more message numbers to certain interfaces gives those interfaces priority, as Fig 2 illustrates.

A network manager or a distributed automatic allocation algorithm embedded in each interface can perform the message number allocation function. Interfaces use the common (or contention) channel message numbers located within each message block to request message allocation. In a large network, message number allocation and other network management functions can be automatically performed by a network monitor unit.

Adapting to traffic conditions

When network traffic is light and the active devices primarily asynchronous (eg, nonintelligent terminals sending short, burst-like messages), UniLINK provides immediate network access, as would CSMA/CD under similar conditions. When synchronous devices or computers transmitting regular, frequent traffic are added to the network, UniLINK dynamically adapts to provide guaranteed token-passing type access (with bounded transmission delays) for those added devices and computers. If increased collisions persist, then all devices receive guaranteed access.

Network interfaces implement UniLAN's UniLINK access method. UniLAN supports several thousand network interfaces, depending on the cable chosen. Each network interface (Fig 2), which consists of a media access unit (MAU), network processor, subscriber processor, and a device interface, can perform all the functions necessary to keep the network operating.

The MAU connects the network interface to the network cable. Any IEEE 802 baseband transceiver for a baseband coaxial cable can serve as the MAU. To connect network interfaces to broadband coaxial cable, Applitek developed a radio frequency modem that provides 10-Mbit/s operation in one 6-MHz TV channel. This modem follows proposed IEEE 802 guidelines. Another MAU choice, the optical-fiber tap, connects the network interface to optical fiber cable.

The network processor employs an 8-bit processor as well as firmware to implement UniLINK. The receive/transmit buffer has 12 Kbytes of RAM to store packets to be received and transmitted. This buffer features resettable first in, first out memory for increased data throughput. For baseband and optical-fiber networks, the network processor furnishes Manchester data encoding/decoding. Moreover, a Motorola 68000 microprocessor and a 3½-in. microfloppy disk allow the subscriber processor to connect to as many as four device interfaces via an IEEE 796 bus (Intel Corp's Multibus). The disk stores programs and configuration parameters.

The device interfaces, each of which can support up to eight RS-232/449 asynchronous, bisynchronous, and synchronous data-link control (SDLC) devices, include 68000 processors as well as 32 Kbytes of dual-ported RAM. This RAM stores inbound and outbound message packets. When one packet is being assembled, another can be transmitted. Every 8-bit segment of RAM within the network interface has an odd-parity, error checking function. Network interface software generates a checksum to perform error checking on all packets in the system.

Software commands allow each interface, or port, to be configured individually in order to handle certain Electronics Industries Association (EIA)

RS-232 signals (specifically, RTS, DSR, CTS, DCD, and RI) in different ways. Table 1 lists the RS-232 signals defined by EIA as well as some signals not found in the definition. For each interface, software commands can separately set such functions and parameters as transmit mode, baud rate, number of stop bits, character-code selection, and local echo. Because of the hardware's modular design, UniLAN's software divides between the device interface boards and the subscriber processor board. Also, each device interface and subscriber processor has an independent onchip copy of the pSOS-68K operating system kernel, from Software Components Group, Inc (Santa Clara, Calif).

TABLE 1

The RS-232 Interface

Pin No.	Signal	Function	Circuit EIA	Circuit CCITT*
1	PG	Protection ground	AA	101
2	TD	Transmit data	BA	103
3	RD	Receive data	BB	104
4	RTS	Request to send	CA	105
5	CTS	Clear to send	CB	106
6	DSR	Data set ready	CC	107
7	SG	Signal ground	AB	102
8	DCD	Data carrier detect	CF	109
11	—	Spare input A	—	—
15	TC	Transmit clock	DB	114
17	RC	Receiver clock	DD	115
18	—	Spare input B	—	—
19	—	Spare input C	—	—
20	DTR	Data terminal ready	CD	108.2
21	—	Ext. transmitter clock	—	—
22	RI	Ring indicator	CE	125
24	ETC	Ext. transmitter clock	DA	113
25	MB	Make busy	—	—

*International Consultative Committee for Telephone and Telegraph

Splitting software into two process groups

The software further divides into two groups of processes (Fig 3). The operating system on the subscriber processor supports one group, which includes the session layer functions. Meanwhile, the operating system on each device interface supports the other group, which includes transport, presentation, and application layer functions.

The subscriber processor and device interface pass data and commands to each other through the dual-ported RAM that resides on the device interface. Both the subscriber processor and device interface have access to this RAM. Data intended for network transmission is transferred to the transmitter RAM on the network processor board. Data coming from the network intended for the subscriber processor or a user device is removed from the network processor's receiver RAM by the subscriber processor.

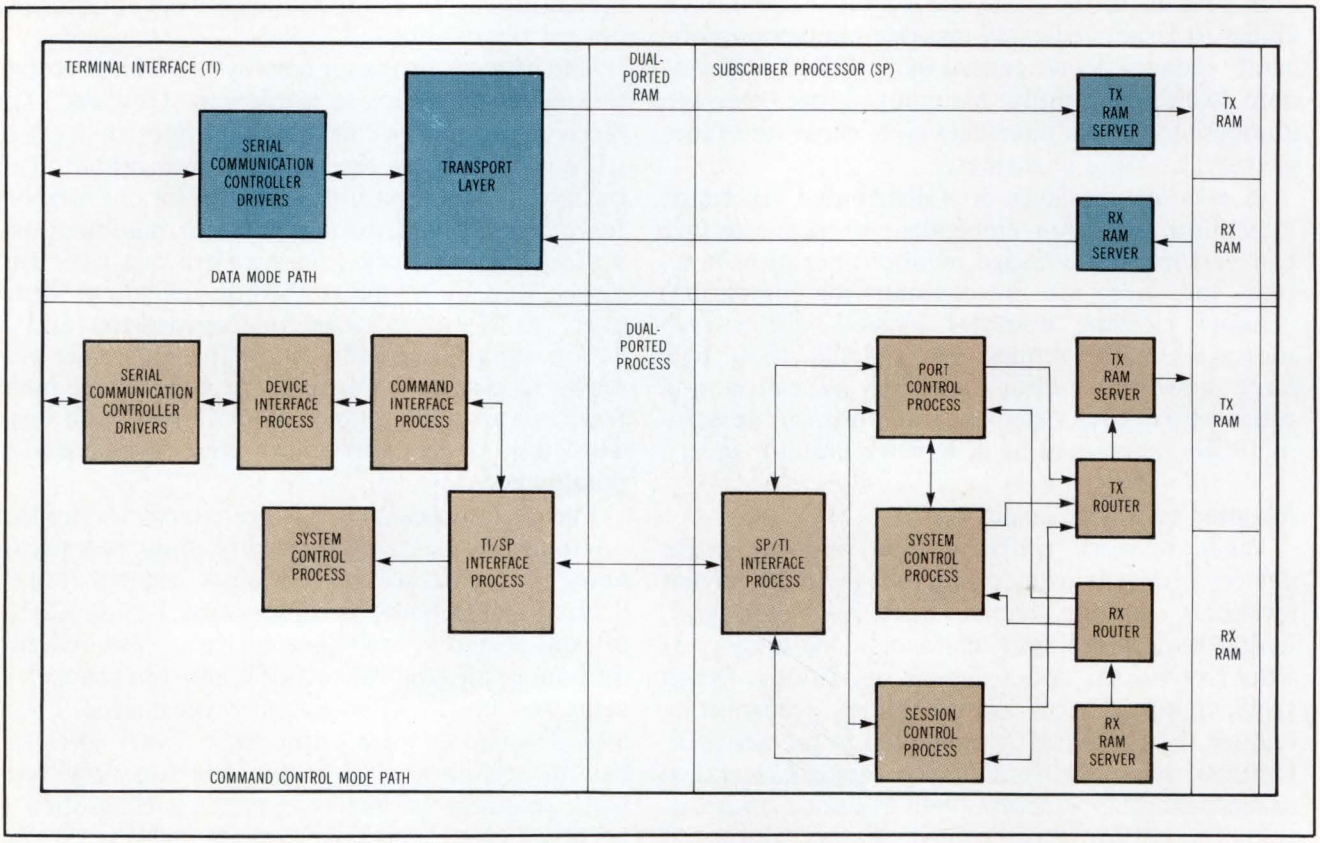


Fig 3 This modular software design follows the layering scheme promulgated by the International Standards Organization in its Open System Interconnection model. Software residing in the subscriber processor supports session layer functions while software on each device interface supports transport, presentation, and application layer functions. Transmit (TX) and receive (RX) RAM resides on the device interface.

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- 24 bit address
- Master or slave operation

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CIRCLE 40

TABLE 2

Software-Alterable Port Configuration Parameters

Parameters	Options
Transmit mode:	Full duplex Half duplex
Baud rate:	50 to 19,200 bits/s
Stop bits:	1.1.5.2
Parity:	Odd, even, none
Character code:	ASCII, EBCDIC, none (transparent)
Local echo:	Echo or no echo
End of packet Condition:	Normal packet size (selectable) and end of message character (selectable) Normal packet size (selectable) and timer (selectable) Echoplex
XOFF threshold:	16 to 4,000 characters
Broadcast group name	(selectable) (Control mode only)
Flow control:	X-ON X-OFF (selectable), DSR, CTS
Port type:	Asynchronous, Bisynchronous, SDLC, HDLC, DDCMP
Rotary port name:	(selectable) (control mode only)
Terminal mode:	Data mode only Data and command mode
Data mode session:	No predefined session Permanent predefined session EIA signal controlled predefined session
EIA control signal options (NI as DCE):	RTS–ignored, valid TD indicator DSR–on, off, follows DTR CTS–on, off, follows RTS DCD–on, off, valid RD indicator RI–on, off, indicates connect request received, on during session, off during session DTR–indicates DTE power-on, ignored
EIA control signal options (NI as DTE):	DTR–on, off RTS–on, off, valid TD indicator DSR–ignored, indicates DCE power-on DCD–ignored, valid RD indicator CTS–ignored, enables NI transmitter
Enable disable: User access to configuration options:	(selectable) (control mode only)

To make UniLAN easy to use, the software uses a command structure similar to the English language. This is presented in menu form. A help facility provides online support. Software creates virtual circuits, called sessions, for passing data between devices on the network. By using simple software commands, users can connect or disconnect sessions, configure port parameters, and send broadcast messages (or datagrams) to other users on the network.

Software sets parameters

After a session is connected, data passes between devices in packets. The packet size for each port is one of the port-configuration parameters that software sets. Error detection and error control procedures ensure data integrity. Other password-protected functions are available only to the network manager, who can reconfigure any port on the network, reinitialize the network, connect or disconnect users anywhere on the network, change port buffer sizes, get status information on any device or session, and perform various diagnostic activities.

Three modes of operation—command, control, and data—provide different types of user services. Separate paths handle the flow of data mode data and command and control mode data through network interface software to ensure high throughput and quick response times.

The command mode allows users to connect or disconnect sessions, use a network directory, configure port parameters, and send messages to other users on the network. Password protected, the control mode provides remote session control, network control, and diagnostic functions for the support staff. Diagnostic functions include access to an error history log, which the system automatically maintains, and the ability to put ports into a loopback mode, thereby helping to pinpoint the location of problems. Control mode also allows third-party connection and disconnection of sessions as well as remote port configuration and renaming.

Once a session has been established, data mode expedites the actual passing of data between devices. For devices that communicate solely with one destination, predefined sessions can be established for that device's port. This procedure keeps the device connected to that port in data mode, making network operation transparent to the user.

On system initialization, software loads from the network interface local floppy disk, which serves as each network interface's original source of software

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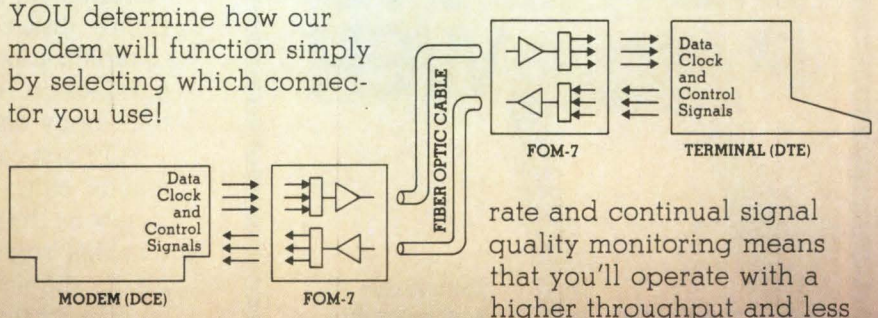

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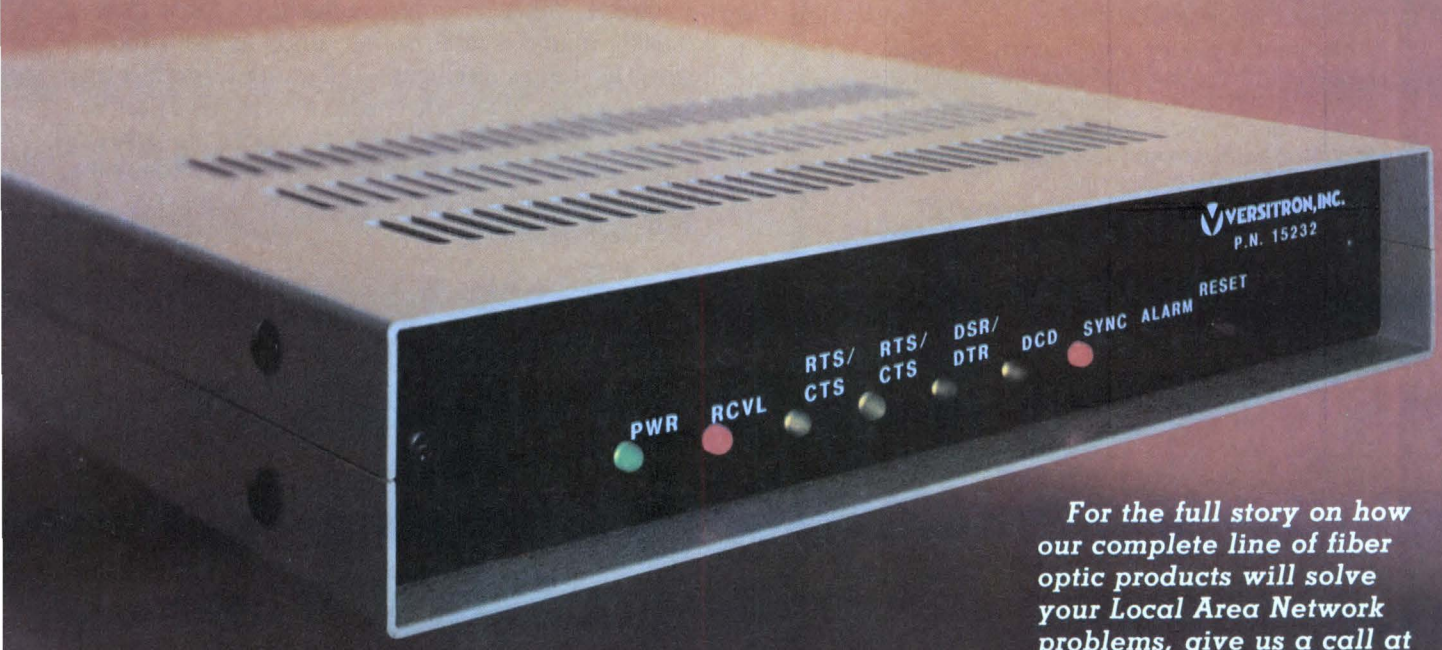

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CIRCLE 41

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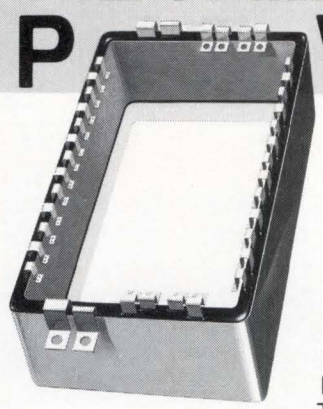

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code as well as configuration parameters. Software revisions can be downloaded onto the floppy disks from other floppy disks, facilitating software updates. The floppy disk also holds help files, the local network directory and the field-support error log file. During network operation, these files are accessed when a user requests help with a command or wants to see or alter the network directory, and when the system logs an error.

Most environments today require a LAN to connect dissimilar devices that have different communication needs.

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CIRCLE 42

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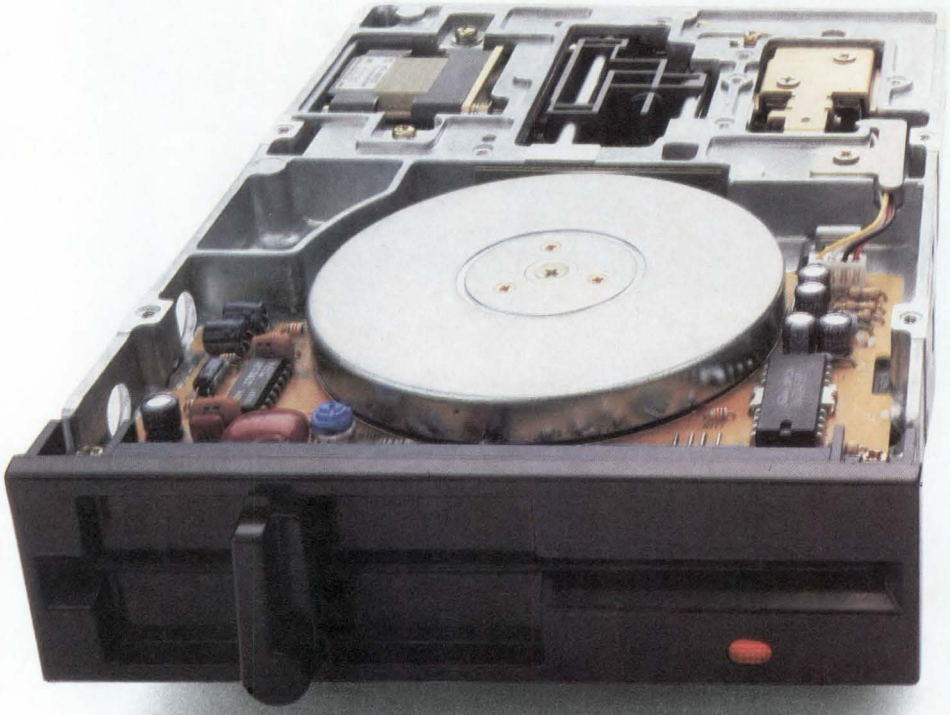

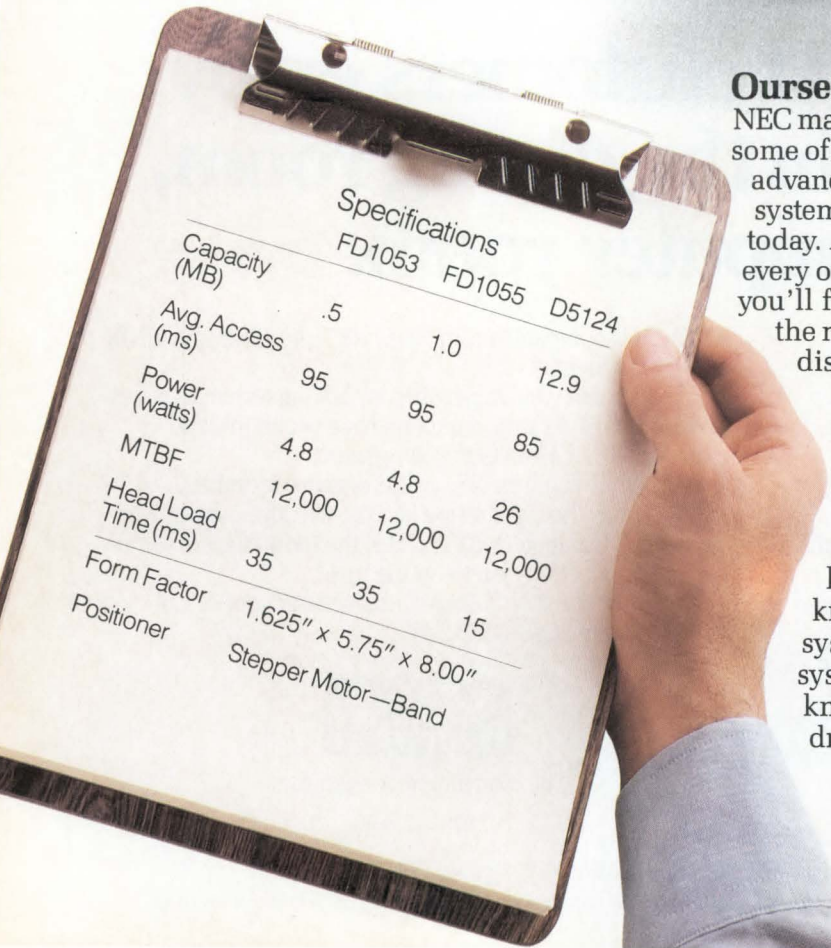

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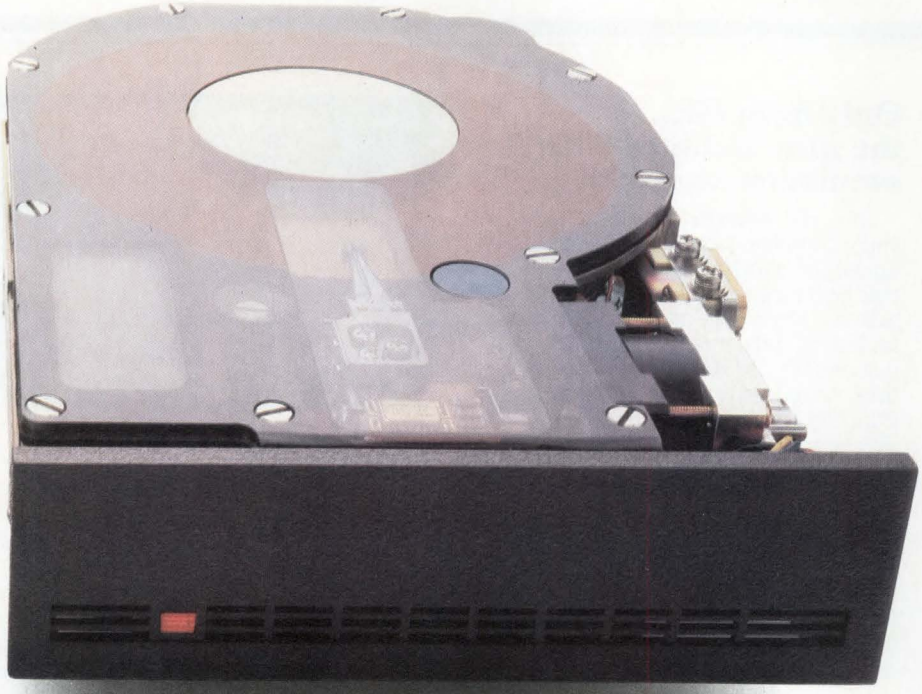

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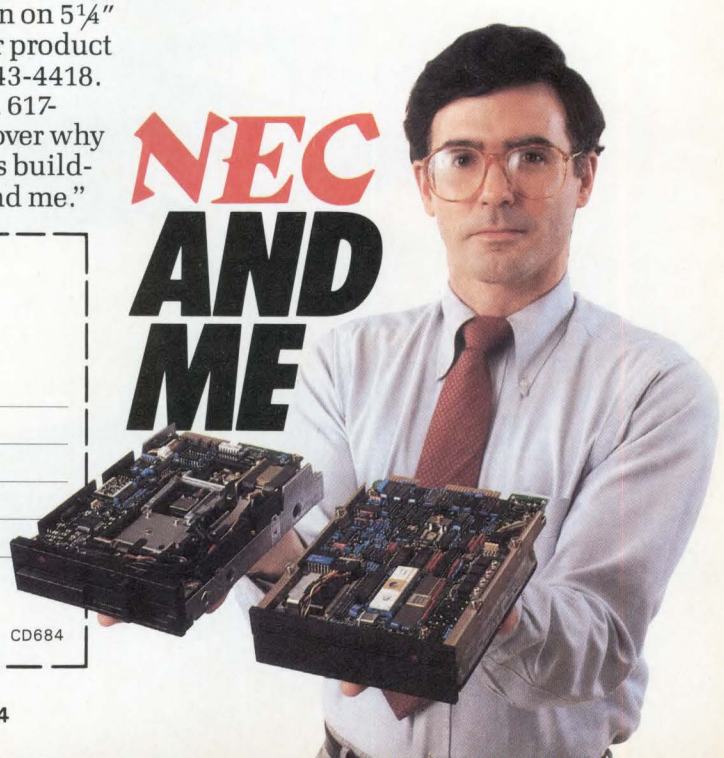

CIRCLE 44

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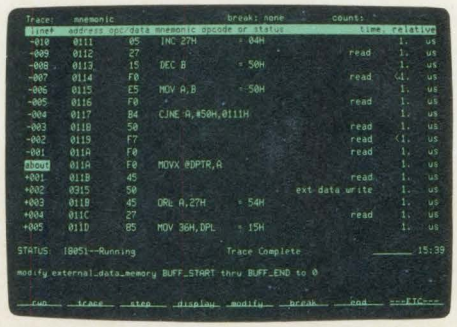

Trace photo of internal data bus is example of how the HP 64264S Emulator shows you more of the 8051 internal operation than ever before.

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8048	6802	Z8001
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	6809E	**80186 (NEW)**
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	8085	8086
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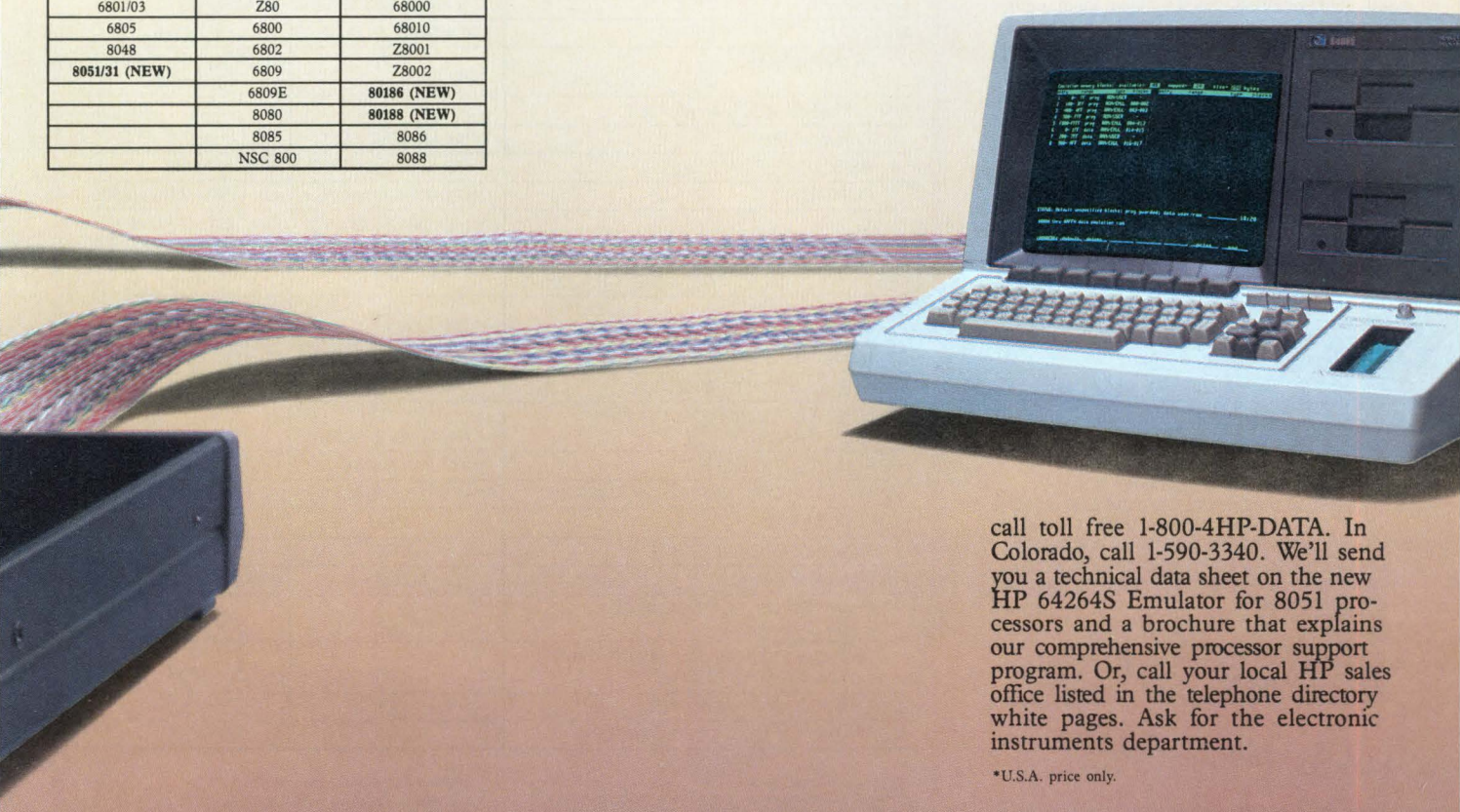

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CIRCLE 45

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- **ZETALISP-PLUS™ software,** an enhanced version of the famous MIT ZETALISP environment.
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Features[1]	LMI Lambda™	Symbolics™ 3600
HIGH-SPEED MULTIPROCESSOR BUS ARCHITECTURE	YES	NO
UPGRADE TO FULL-PERFORMANCE 2-USER LISP SYSTEM	AVAILABLE JULY	NO
68000 CO-PROCESSOR W/UNIX™ Version 7 (SWAPPING)	AVAILABLE NOW	NO
68010 CO-PROCESSOR W/UNIX™ System V (PAGING)	AVAILABLE AUGUST	NO
EXTENDED-STREAMS INTERFACE	YES	NO
USER-PROGRAMMABLE VIRTUAL CONTROL STORE IN LISP CPU	YES - 64K X 64 BIT	NO[2]
LISP MICROCOMPILER FOR EASY MICROCODE DELIVERY	YES	NO
BUS SPEED	37.5 MEGABYTES/SEC	20 MEGABYTES/SEC
MULTIBUS™	STANDARD, INTEGRAL	OPTIONAL
IN MAINFRAME	YES	NO, ADD-ON CABINET REQUIRED
OTHER LANGUAGES AVAILABLE:		
CommonLISP	AVAILABLE MAY	?
PROLOG	YES/MICROCODED	?[3]
FORTRAN-77	IN 68000/68010/UNIX	ON LISP HARDWARE
C	IN 68000/68010/UNIX	ON LISP HARDWARE
PASCAL	IN 68000/68010/UNIX[4]	ON LISP HARDWARE
OPTIONAL ½-INCH STREAMING TAPE DRIVE	YES	YES
IN MAINFRAME	YES	NO, ADD-ON CABINET REQUIRED
OPTIONAL ¼-INCH TAPE DRIVE	YES	YES
HIGH-RESOLUTION B&W DISPLAY	YES	YES
MEDIUM-RESOLUTION COLOR WITH FRAME GRABBER	AVAILABLE APRIL	NO
HIGH-RESOLUTION COLOR	AVAILABLE AUGUST	YES
WINCHESTER DISK DRIVE(S) — CAPACITY	UP TO 1.8 GIGABYTES	UP TO 1.8 GIGABYTES
LISP PROCESSOR	32-BIT	36-BIT
TAGGED ARCHITECTURE	YES	YES
FULL ZETALISP DIALECT, INCLUDING:	ZETALISP-PLUS	ENHANCED ZETALISP
FLAVORS OBJECT-ORIENTED PROGRAMMING	YES	YES
WINDOW SYSTEM, INSPECTOR, ZMACS, WINDOW DEBUGGER ...	YES	YES
ETHERNET-II™ NETWORKING	YES	YES
VAX™ VMS™ & UNIX™ INTERFACES	YES	YES

(1) Some of the features detailed may not apply to certain Lambda configurations. The LMI Lambda system offers many advanced resources not listed here, and a detailed technical summary and software overview are available on request. This table is based on data available from Symbolics' published data sheets and advertisements, and may not reflect changes or improvements made by Symbolics concurrent with or subsequent to the release of this comparison.
(2) The Symbolics 3600 has an 8K X 112-bit control memory. User microprogrammability is not encouraged.
(3) A non-microcode-optimized PROLOG version is available for the Symbolics 3600 from LISP Machine Inc.
(4) Available August

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LMI LAMBDA

TAGGED ARCHITECTURE SUPPORTS SYMBOLIC PROCESSING

Even though the Lisp programming language enables artificial intelligence functions on large computers, efficient processing necessitates a different architecture.

by Abraham Hirsch

Lisp has capabilities lacking in other computer languages in that it permits manipulation of complex structures and symbolic information. Because of its ability to manipulate symbols, it is used for expert systems, visual recognition, and other subcategories of artificial intelligence. Its major drawback, however, is that its large size and flexibility can easily swamp a conventional mainframe. This flaw is more a result of conventional computer architecture than of any shortcomings of the Lisp language itself. Efficient Lisp processing thus requires a new type of computer architecture.

Complex knowledge and data are described by physical or abstract symbols in natural language (eg, words and numbers) with lists of properties to describe them. The properties consist of a variety of data types, such as text and numbers, that form a long itemized list attached to each symbol. This is different from most computer languages where variables have only one numerical value, because of computer limitations. The closest analogue to symbols are records in a data base. However, database records are full of fixed-length fields that are difficult to manipulate. Symbols take the database concept several steps further. Fields are totally arbitrary in terms of data type, length, and order, with no fixed structure among symbols, as in data records.

As noted, symbols are defined by lists of properties that can be processed dynamically, unlike those in a normal data base—ie, they can be broken apart or combined to form new symbols. Also, because the symbols are processed dynamically at run time, there are certain memory allocation/deallocation problems that do not occur with conventional programming languages.

Most computer languages define variable and fixed arrays, and allocate memory space at compile time. If the computer needs more space than is allocated during compile time, and it is unavailable, the program will abort. Symbolic processing, however, is so dynamic that the operating system does not know at compile time how big the data structures are going to be, or what they will look like when the program executes.

Lisp, a mnemonic for list processing language, deals efficiently with these lists and data structures, but it can bog down the performance of a conventional mainframe and use up all its memory trying to process symbols dynamically. Despite such difficulties, large conventional computers were originally used to develop Lisp and prove its viability as a symbolic computer language.

Lisp advantages

Given the problems that Lisp presents for traditional computer architecture, it is only natural to ask whether it is worth all the trouble. The characteristics of the language as it has developed to support symbolic processing provide an answer to the question.

Lisp, a computer programming language that originated as a tool to facilitate artificial intelligence (AI) research, was invented in the 1950s by Professor John McCarthy of the Massachusetts Institute of Technology (MIT), who is now of Stanford University. Since intelligence involves thinking about objects, how they relate to each other, and their

Abraham Hirsch is manager of product management at Symbolics, Inc, 4 Cambridge Center, Cambridge, MA 02142. He holds a BS in electrical engineering and an MEng from Cornell University.

Examples of Generic Operations

Conventional computers	Symbolics 3600
A minimum of three add instructions in hardware are required: – Add two fixed point numbers – Add two single precision floating point numbers – Add two double precision floating point numbers Unable to mix integers with floating point	A single add instruction in hardware for all data types Ability to mix data types Fewer instructions Simple software Higher throughput

properties and uses, Lisp represents arbitrary objects and the relationships among them. Lisp also allows the modeling of procedural knowledge (ie, "how to do something" as opposed to "what something is"). Procedural knowledge is expressed by functions—computational entities that know how to perform some specific action or computation upon supplied objects.

The language imposes no penalty for dividing a program into dozens or hundreds of functions, each one the expert in some specific task. Thus, Lisp promotes "modularity"—the clean division of a program into unique areas of responsibility—with well-defined interaction. Lisp also features extensible syntax or notation. This means that language constructs are not limited to those supplied, but can include new constructs. Defining new language constructs does not involve modification of the supplied software, or expertise in its internal details, because it is a standard feature.

Lisp also frees programmers from the detailed management of memory in the computer. Although it is possible to construct fixed-size arrays, Lisp excels in providing facilities to represent arbitrary-size objects, sets of unlimited numbers of elements, and objects in which the number of details or parameters is totally unknown.

New computers designed specifically for Lisp provide an interactive environment in which both data and functions coexist and can be inspected or modified easily. Functions can be tested as they are written, and problems found quickly. These features have made Lisp the preferred tool of AI researchers. If Lisp and computer interactions seem flawed, the fault lies within the architectural rigidity and limitations of conventional computers.

Lists of properties contain different data types. As they are processed, the computer must be able to identify which can be added to, subtracted from, or combined. This involves an enormous amount of data-type checking, which requires the use of long strings of instructions at compile and run time. Conventional machines cannot do this in hardware.

Another deficiency of conventional computer architecture involves the dynamic nature of property lists. To use Lisp, a process must be created to reclaim user memory at run time. In a normal computer, this is a very memory-expensive process; all of the list structures in memory must be periodically checked to see if they are still in use so memory can be reclaimed. Every structure in virtual memory must be read. Doing this requires a large program called a "garbage collection" algorithm.

A third flaw of most computers is the size of the virtual memory space available. Programs used in AI applications are often large and complex, and their data sets are even larger. Examples of these are satellite images, speech, and sensor input. As a result, the total memory requirements of Lisp programs are enormous, outstripping the memories of even the largest computers.

Developing an architecture

To solve these problems, researchers at MIT's AI laboratory began the Lisp machine project in 1974. Initially, a simulator was written on a time-shared computer to permit software development to proceed while the hardware was under development. CONS was the first machine designed, in 1976. It was superseded in 1978 by a second-generation Lisp machine, the CADR. This machine was a model for the first commercially available Lisp machines, including the Symbolics LM2.

The third generation, represented by the 3600, is based on a completely new architecture. Like the LM2, it runs the Zetalisp dialect for software compatibility. Zetalisp is a Lisp dialect, developed for the Lisp machine project that adds many features and improvements. Foremost is the Flavors system for object-oriented programming with message passing. A full range of data types, modern control constructs, flexible function calling, multiple value returns, and stream-oriented I/O add to basic Lisp features. Additional improvements include macros to permit syntax extension, multiple name spaces, and predefined functions to support such operations as sorts, hash tables, linear equations, and matrix operations.

As the Symbolics first Lisp machine, the LM2 had microprogrammed Zetalisp instructions so that it was the assembly language on the system. This addressed the question of how to build a new environment using Lisp. It also allowed Lisp to deal with itself as a data structure by taking advantage of its power to deal with symbols. In addition, it made it very easy to build incremental compilers, whereby each function may be compiled as it is entered or modified. That makes debugging and recompilation faster, more interactive, and allows more powerful test and debug tools.

The LM2, like its MIT prototypes, solved many problems with its 32-bit microprogrammed virtual memory architecture. However, because it was found that a great deal of processor bandwidth was

expended on data typing and dynamic memory allocation and deallocation, a better way was needed to deal with these functions. Tagged memory architecture was the method used to solve these remaining problems. It proved to be a simple, elegant, and very powerful concept that resulted in a new machine, the Symbolics 3600 Lisp processor.

Lisp normally stores data in a complex data format. An extra word attached to each data word identifies the nature of the data. This can be fixed or floating point, a rational or complex number, an object known to Lisp, an array, a string, or compiled object code or source code. Normally, numerous data types are tagged in software so that there are as many words in memory identifying the data type as there are words of data. This is not very efficient, however, since a great amount of computer time is spent just reading and checking these "tags." It is done throughout memory on virtually every piece of data and code structure in the system.

The tagged architecture concept, as implemented in the 3600 processor, performs this function in hardware. Simply by adding 4 extra bits to the end of the 32-bit word as "memory tags," the same data that previously was put into memory serially can be placed in memory in parallel, and in the same location. Therefore, the 3600 was built with some unique features—ie, 36-bit architecture (register and memory) and hardware to handle the memory tags. The processor can detect those tags and perform the proper operations in hardware and firmware. As a result, all the overhead of extra instructions disappears, and there is nearly an order of magnitude increase in performance. This increase in speed is accomplished by performing data-type checking in parallel with instruction execution.

Data tagging

Data-type checking occurs at run time because compile-time, data-type checking is not compatible with Lisp's flexibility. Runtime-type checking is supported by the tag field appended to every word processed by the processor.

All macroinstructions are generic. (See the Table.) One add instruction, for example, handles all appropriate data types: fixed point, floating point, double precision, etc. The behavior of a specific instruction is determined by the operand type read in the tag fields. Because data-type checking is performed in parallel with the instruction, there is no performance penalty. Thus, one macroinstruction, by using generic instructions and tag fields, can do as much as several instructions on a conventional computer. The result is a compact storage of compiled programs and fast execution of those programs.

The 3600 processor's 36-bit word has two formats (Fig 1). The one most often used is called a tagged pointer format and consists of a 6-bit tag, 2-bit contents of data register (CDR) code, and 28 bits of an address pointing to a data structure. The other, an immediate number format, has a 2-bit tag, a 2-bit CDR code, and 32 bits of immediate numerical data. In main memory, each word is supplemented with an additional 7 bits for error correction code and a spare bit to make a 44-bit word.

In Lisp, the first element of a list is called the contents of address register (CAR) and the remainder of the list is called the CDR. The amount of storage needed to hold the list is reduced by coding CDR into 2 bits. Values of the CDR code indicate whether it is a conventional CAR and CDR pointer list element pair or represents a more efficient vector in memory (Fig 2). The new vector format takes only half as much memory as usual, and therefore only half as many memory fetches. Thus, the performance doubles over conventional Lisp implementations.

Because of the recursive nature of Lisp applications, efficient processing requires a stack-oriented machine. Although not a pure stack machine, the 3600 is stack oriented and designed to make function calls and returns as fast as possible. Most instructions, but not all, use the stack to get operands and store results. The processor contains multiple stacks and buffers used for fast storage of temporary data. Stacks are used to pass arguments. The processor controls the stack pointers and buffer manipulation (which takes only one machine cycle). A given computation is associated with a particular stack group.

Each stack group contains three stacks for control, binding, and data. The control stack, containing the control environment, local environment, and caller list, is formatted into frames that correspond to function calls. A frame consists of a fixed header followed by arguments and local variable slots. Binding is the process by which a variable is temporarily given a value (a special variable). The binding stack contains special variables and previous values of those variables to be restored later. The data stack,

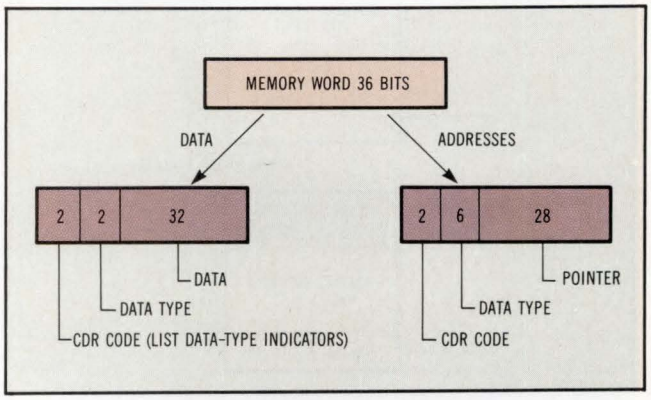

Fig 1 There are two basic formats for 36-bit words. The immediate number format consists of a 2-bit tag, a 2-bit contents of data register (CDR) code and 32 bits of immediate numerical data. The tagged pointer format consists of a 6-bit tag, 2-bit CDR code, and 28-bit data structure address.

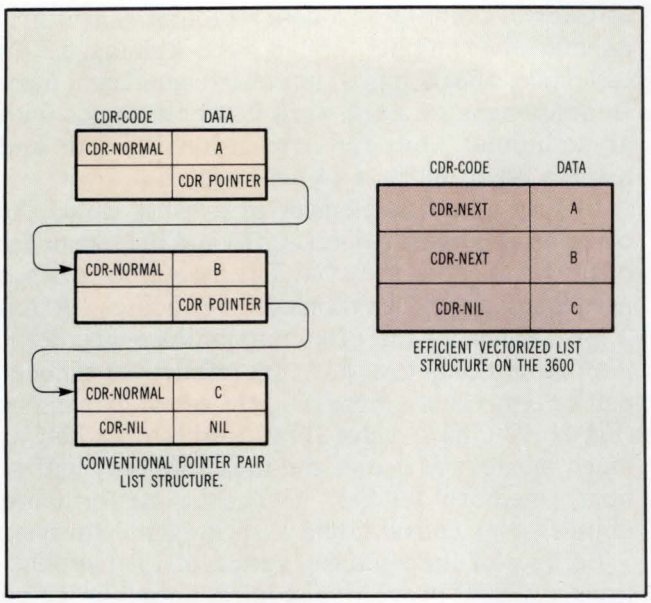

Fig 2 An analysis of Lisp CDR coding, comparing conventional computer architecture Lisp implementations (a) to tagged architecture (b), is shown.

which helps reduce garbage-collection overhead, contains dynamic Lisp objects, such as temporary arrays and lists.

There are two major Lisp variations: Maclisp from MIT; and Interlisp, developed at Bolt, Beranek & Newman (BBN) and used extensively at Stanford. Zetalisp, derived from Maclisp, was influenced by others as well. Xerox Corp's learning research group (Palo Alto, Calif) has done extensive work with children to investigate natural ways of communicating

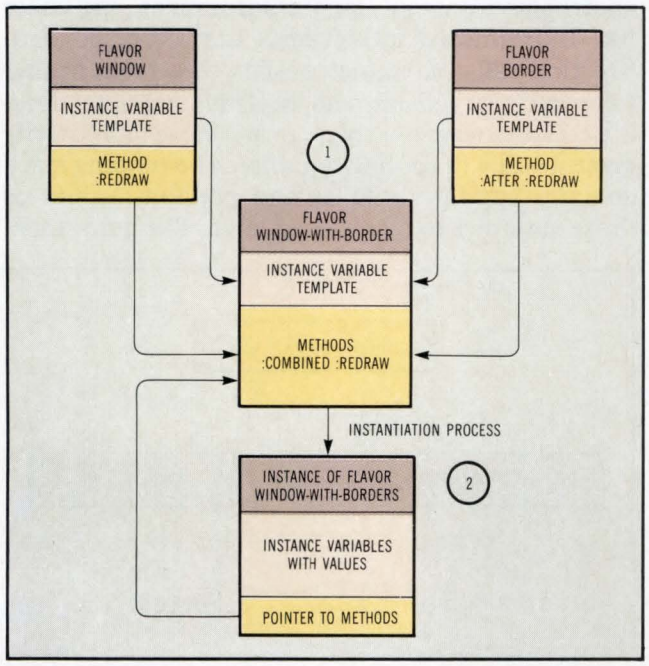

Fig 3 The Flavors system (abstract type) can be combined to form new flavors (see No. 1). When generic flavors are provided with specific variables, flavor instances (objects) that can be manipulated by sending messages (requests for specific operations) are produced, as shown in No. 2.

with computers. Out of this research came the object oriented programming language, Smalltalk, that was developed in 1972 and has since undergone numerous iterations. Smalltalk, recognized as a simple but powerful concept, is more limited in scope than Lisp. At MIT, the concept was altered and extended to become the Flavors system.

Surveying system characteristics

Although this system contains many Smalltalk constructs, it also permits multiple inheritance, a characteristic that earlier versions of Smalltalk did not have. Multiple inheritance is the ability to inherit characteristics from classes (similar objects) that are hierarchically unrelated. Another major difference is that Flavors is a fully-integrated extension of Lisp. Consequently, the Zetalisp dialect used on the 3600 incorporates the features of both Lisp and Flavors.

Flavors represents generic objects. For example, a generic "ship" with its description could be a flavor. An aircraft carrier with the addition of its unique (nongeneric) descriptors would be an instance of the flavor "ship." (The process of going from the generic to the specific is called instantiation.) Such instantiated flavors are manipulated by sending messages that request specific operations. Since the procedures are already contained within the object, it responds by performing the operation requested. Complex-dependent relationships can be declared among flavors and can be modified as needed (Fig 3).

The 3600 machine instruction set corresponds closely to Zetalisp. No programming is done directly in the instruction set and no assembler is supplied. Programmers may encounter the Lisp-like instruction set when using the inspector or disassembler, but programming will normally be done in Zetalisp. Although the Lisp dialect is an extension of Maclisp and has numerous enhancements, it is compatible with the other dialect of Lisp through the use of the Interlisp compatibility package. Other languages supported by the system are Fortran and Pascal. Hardware ties it together.

The 3600 CPU, designed to support Lisp and provide very close coupling with the software, is built around a 36-bit memory tagged architecture, with 32-bit external data paths (Fig 4). The tagged architecture permits runtime data-type checking with no overhead. The machine is stack oriented with high speed buffering of the top stack frames. The instruction prefetch is overlapped with normal execution to permit many opcodes to execute in as little as 200 ns. Runtime checking is assisted by hardware to find data-type mismatches, uninitialized variables, and array bound errors. Fast array indexing and IEEE standard floating point operations are additional processor features.

Memory efficiency is enhanced by another processor feature—hardware-assigned garbage collection.

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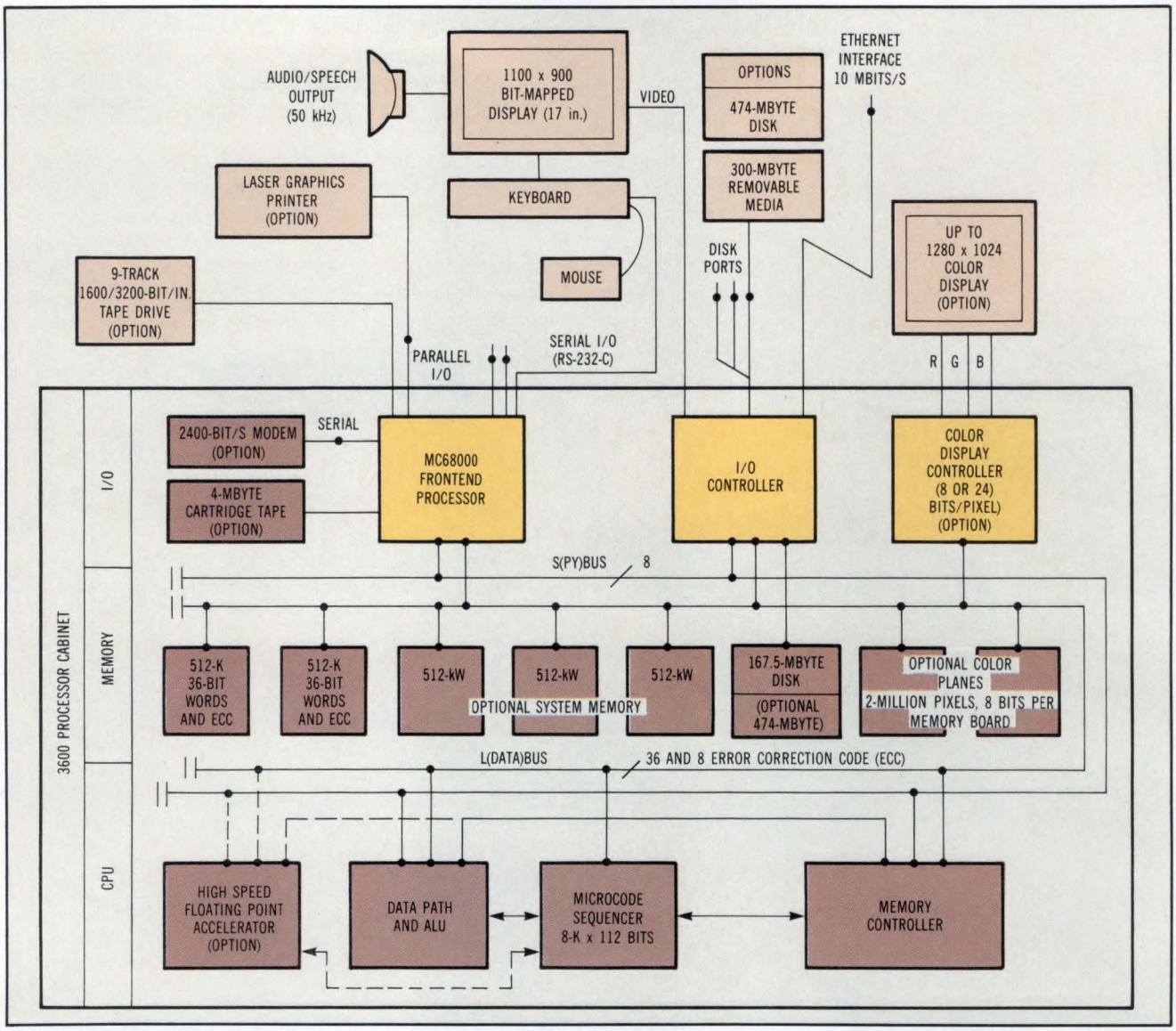

Fig 4 Like all computers, the 3600 symbol processor consists of three sections: CPU, memory, and I/O. However, the stack-oriented CPU and memory tagging provide an organization specifically designed for Lisp processing.

Given the requirements of Lisp processing and the size of the demand-paged memory, it is needed. Up to 256 million, 36-bit words (1 Gbyte) can be directly addressed. Also, up to 7.5 million words (30 Mbytes) of error-corrected physical memory can be configured in a system.

For I/O, the 3600 also includes a 68000-based front-end processor that controls low and medium speed I/O devices and is used for system diagnosis. But for higher performance, the 3600 has an I/O board that handles 10-Mbit/s Ethernet, disks, and the high performance graphics console.

Symbolic processing allows computers to deal with complex knowledge and data in such a way that it appears to mimic human intelligence. The Lisp computer language evolved to handle the constructs of symbolic processing. It now enables computers to be easily programmed to represent objects and the relationships among them. The high overhead costs resulted in a new, stack-oriented, tagged memory architecture designed around Lisp. Complex AI techniques are now out of the laboratory and have become commercially and economically practical. For this reason, the future will see many new applications for Lisp machines as AI techniques are applied to whole new classes of non-numerical problems that, up to now, have been unsuitable for traditional computer methods.

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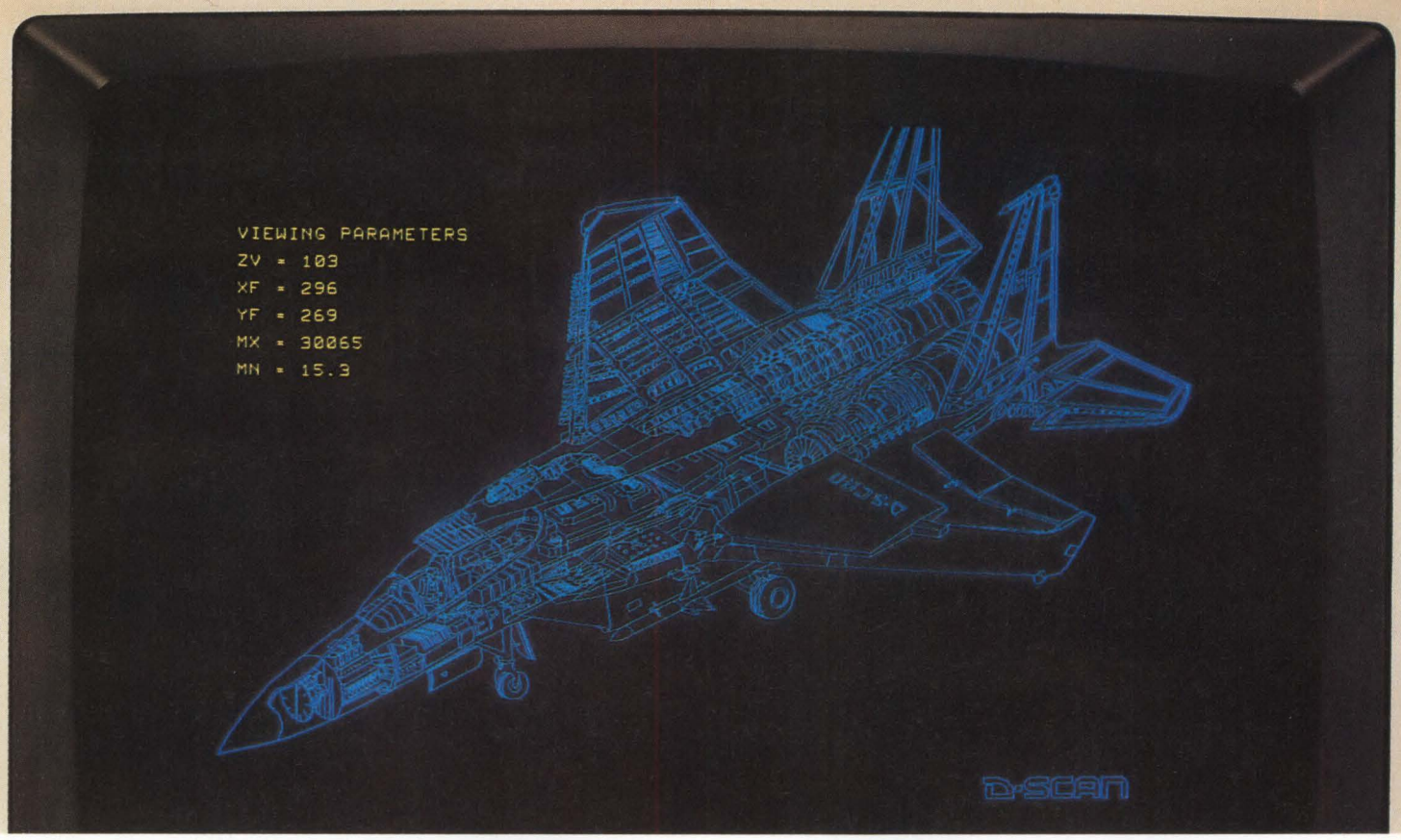

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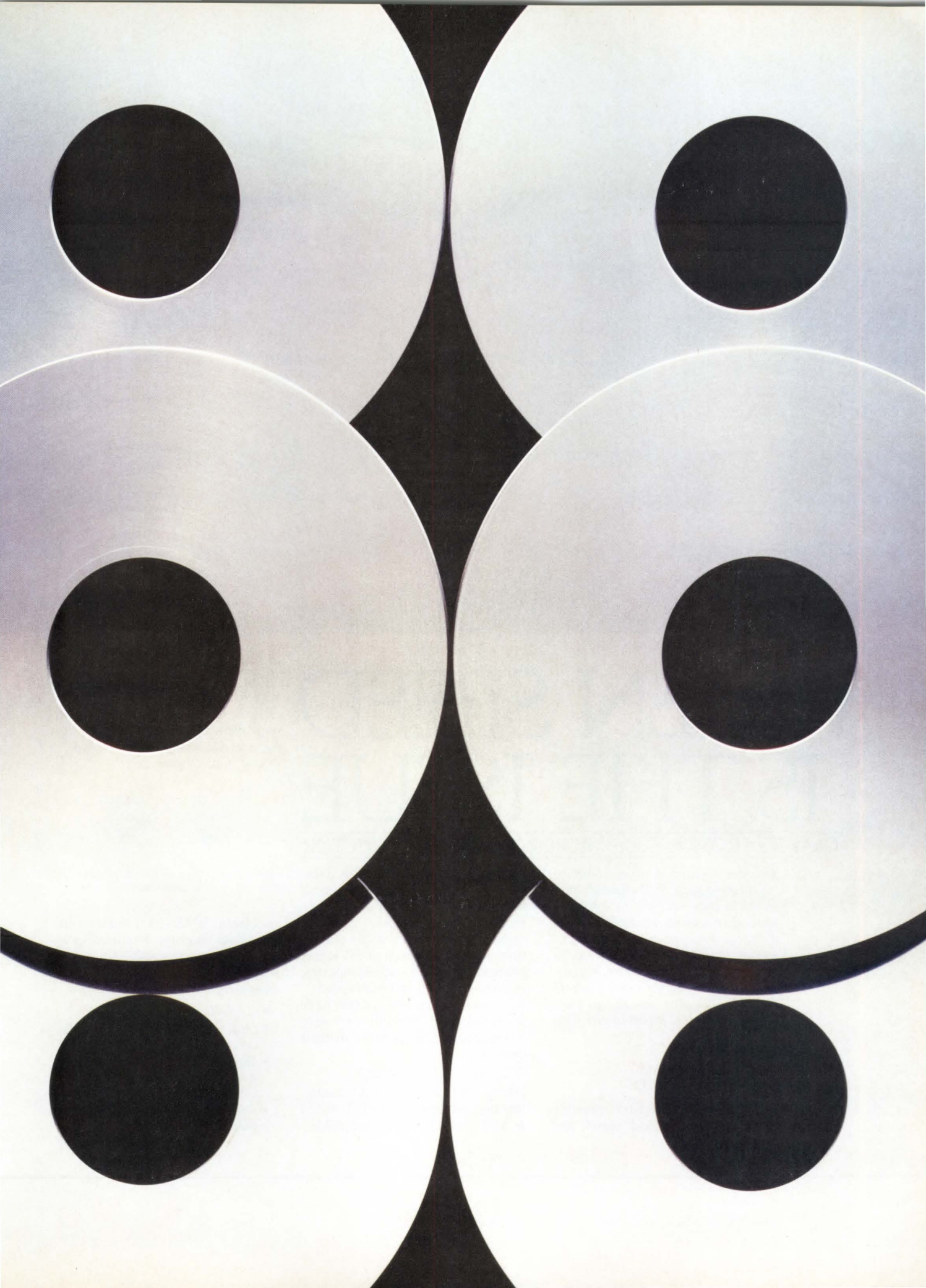

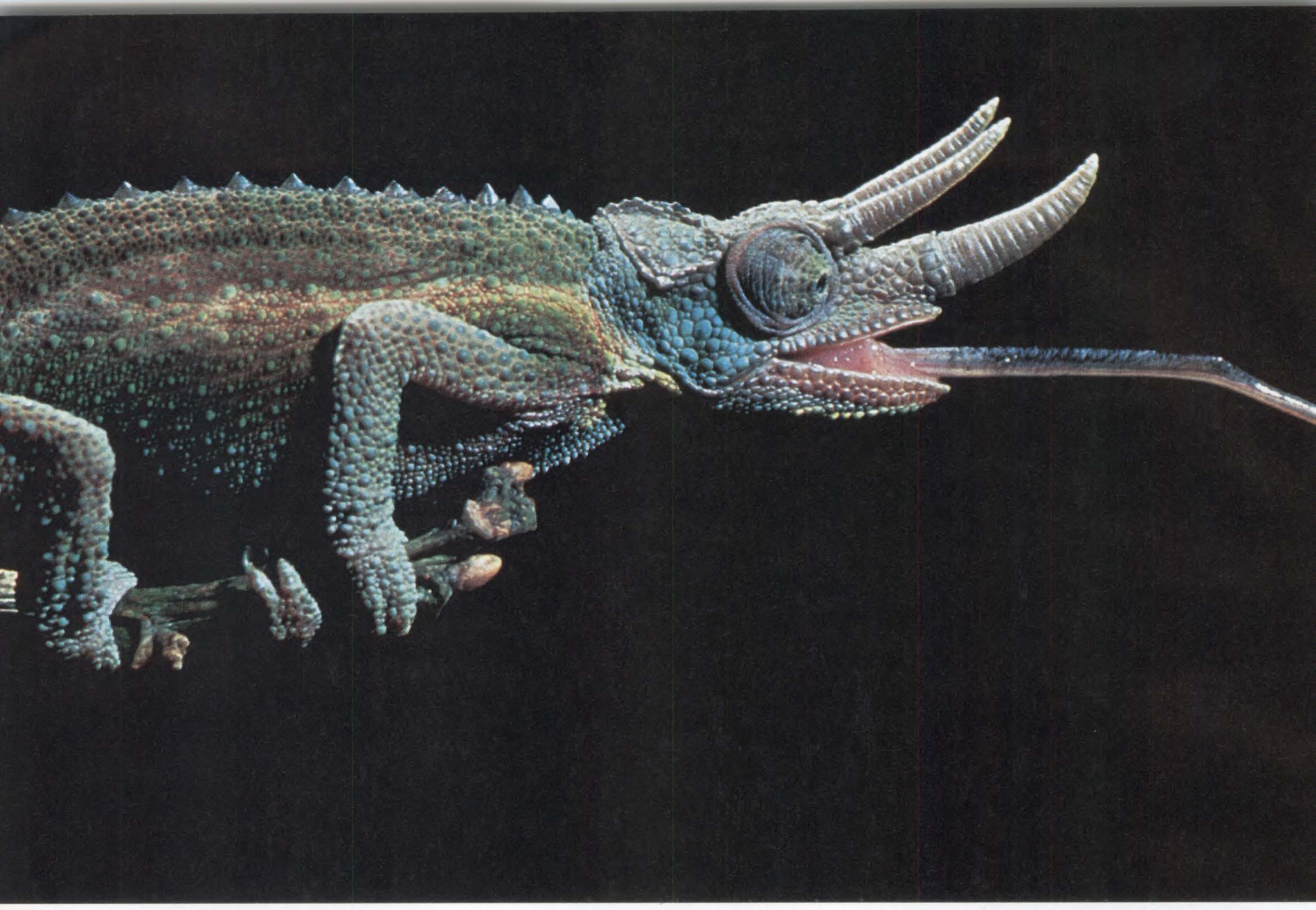

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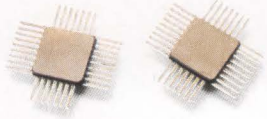

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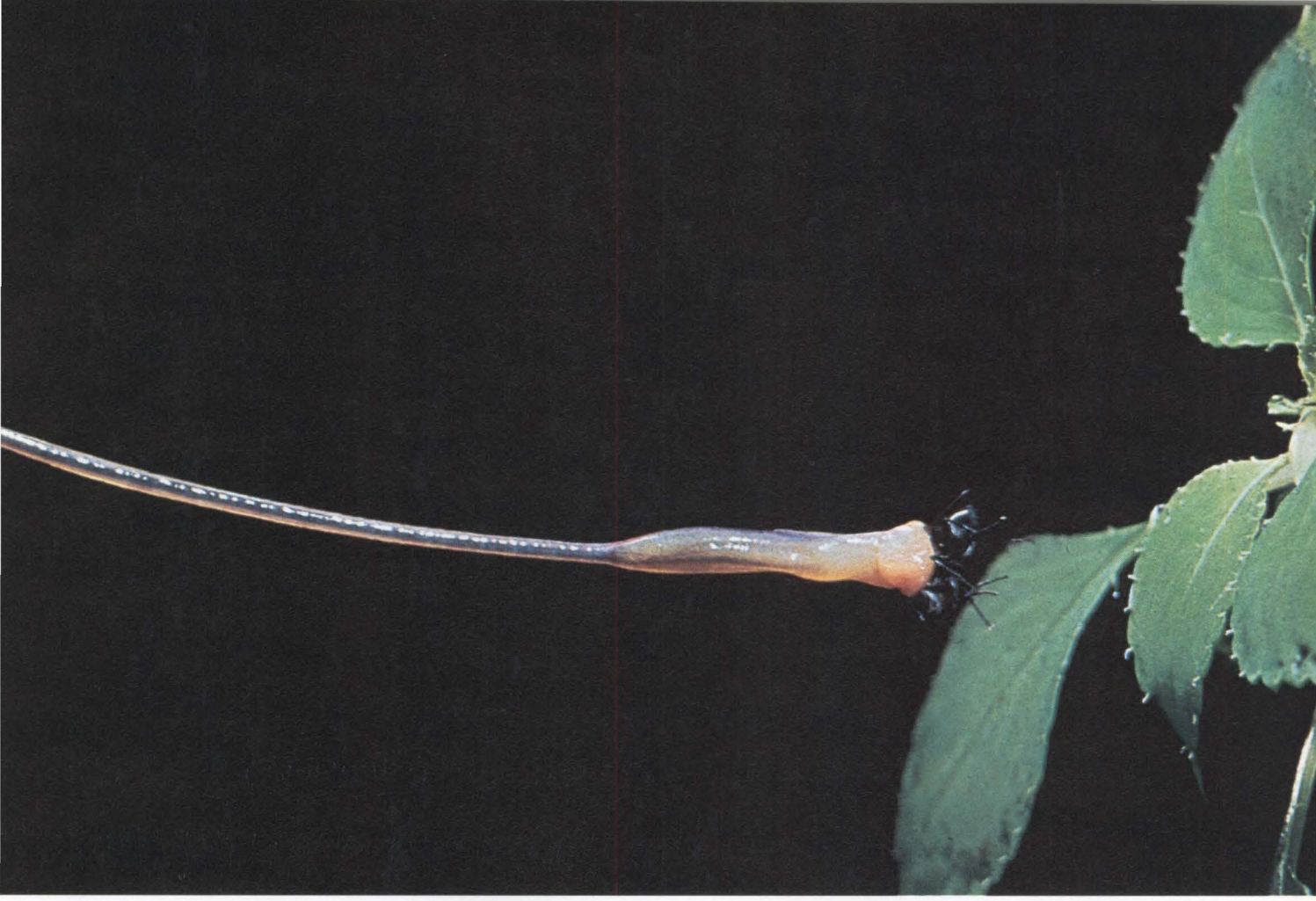

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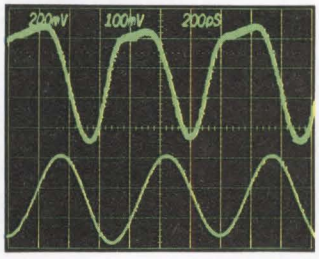
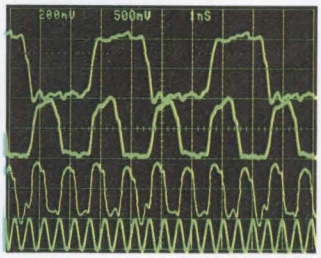


High toggle rate HMD-11141-1 Shift Register showing clock (lower trace) and output functions.



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CIRCLE 51

IC DECODER PAVES THE WAY FOR VIDEOTEX REVOLUTION

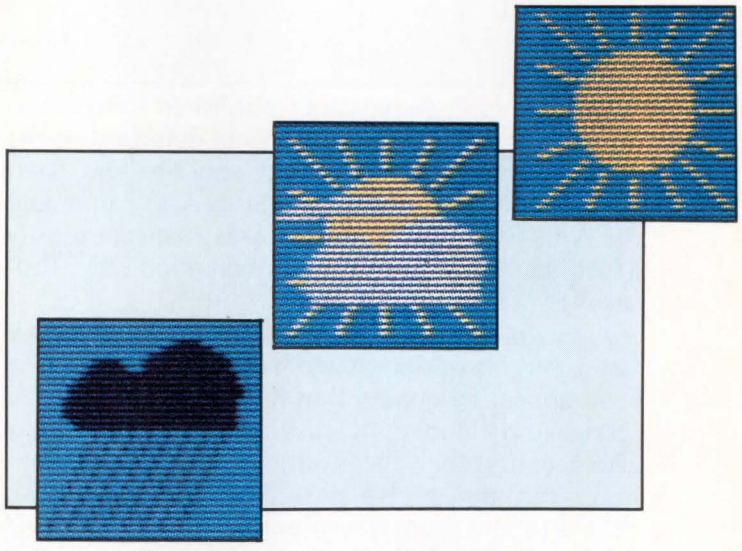
Cost is key in public acceptance of videotex information systems. With a presentation-level standard ensuring transmission uniformity, attention turns to development of reasonably priced hardware.

by Gregg Ledford

For the last several years, videotex/teletext services have but hinted at their potential capabilities. Soon, however, they will offer the United States a wide array of information services. The public, already familiar with the power brought to personal computing by the microprocessor, is prepared for real application of processing power in what it sees as the most important job—facilitating important day-to-day exchange of information. The introduction of interactive data systems, complete with vivid graphics, promises a reshaping of the way an individual will read, write, and communicate with the rest of the world.

Although Europe pioneered the way, the joint cooperation of U.S. and Canadian interests cemented a standard for the interactive transmission of data and spurred interest on this side of the Atlantic. The North American Presentation Level Protocol Syntax (NAPLPS) standard gives engineers a starting point for the design of home videotex or teletext decoders. But, because the standard is so well-defined, currently available off-the-shelf hardware gives end-equipment designers NAPLPS compatibility in a minimal amount of time and at minimum cost.

Videotex has been available in the United Kingdom since 1979 through Viewdata, a service based on the



Prestel coding scheme. It provides customers with alphamosaic graphics—pictures built from character-sized blocks. Like Britain, France's telecommunications agency recognized the potential future of videotex services and developed its own system, called Antiope. In addition to alphamosaics, the French service uses semigraphics characters as well. Unlike the British system, which uses serial coding for mosaics, Antiope uses parallel coding.

The Antiope system produces better graphics than its British counterpart. However, the Conference of European Posts and Telecommunications has endorsed the British technique, causing similar systems in other parts of Europe to be derived from it.

The Canadian Department of Communications, after watching developments in Europe with interest, came up with its own system, called Telidon. Here, graphics elements are defined by points connected by picture description instructions (PDIs). The instructions include such art elements as points, lines, rectangles, arcs, and polygons. After points on the screen are identified, a drawing instruction is used to connect them with the appropriate art element. In that manner, detailed images can be produced.

Gregg Ledford is a systems and software design engineer at Texas Instruments, Inc, 9901 S Wilcrest Dr, Houston, TX 77099, where he is responsible for the definition and prototyping implementation of videotex systems and software based on the NAPLPS standard. Mr Ledford holds a BS in electrical engineering from Louisiana State University.

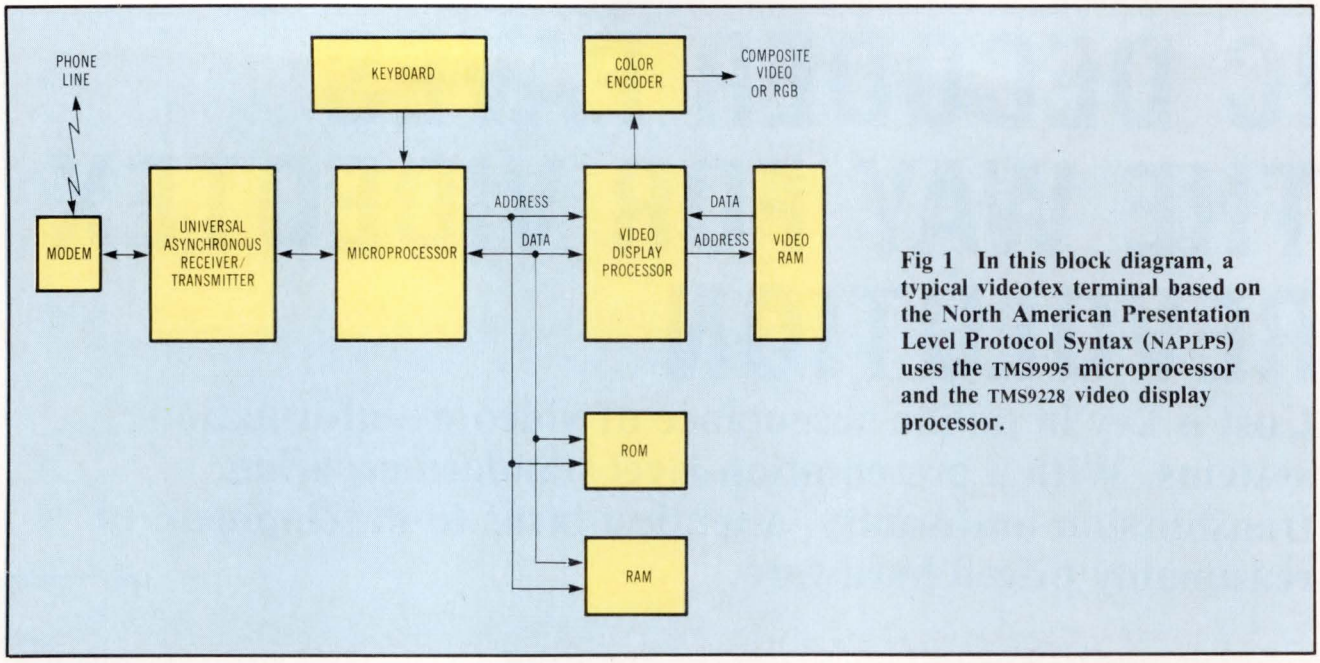


Fig 1 In this block diagram, a typical videotex terminal based on the North American Presentation Level Protocol Syntax (NAPLPS) uses the TMS9995 microprocessor and the TMS9228 video display processor.

In 1981, U.S.-based AT&T published a Presentation Level Protocol (PLP) to help standardize the manner in which videotex data would be sent. Two years later, the Canadian Standards Association and the American National Standards Institute jointly issued the Videotex/Teletext Presentation Level Protocol Syntax, also called the NAPLPS.

A videotex system allows the user to tap into a vast reservoir of data. Color text and graphics give it an appealing quality that not only helps sell the service to the public, but also makes it an extremely effective tool for education. News, business, shopping, banking, and a host of family services all extend to and from the subscriber's own home via existing cable television or telephone installations.

But, for those who must design the hardware that accomplishes all that, the "elegance" of a simple chip set is beyond compare. A typical chip set (Fig 1) to implement a NAPLPS decoder includes a microprocessor with ROM and RAM, a video display processor to handle the text and graphics, and a modem to handle the communications. The NAPLPS standard, because it specifies the precise manner in which both text and graphics information must be sent, eliminates any vagarities about what will be demanded of the end product's performance.

Rules to use in design

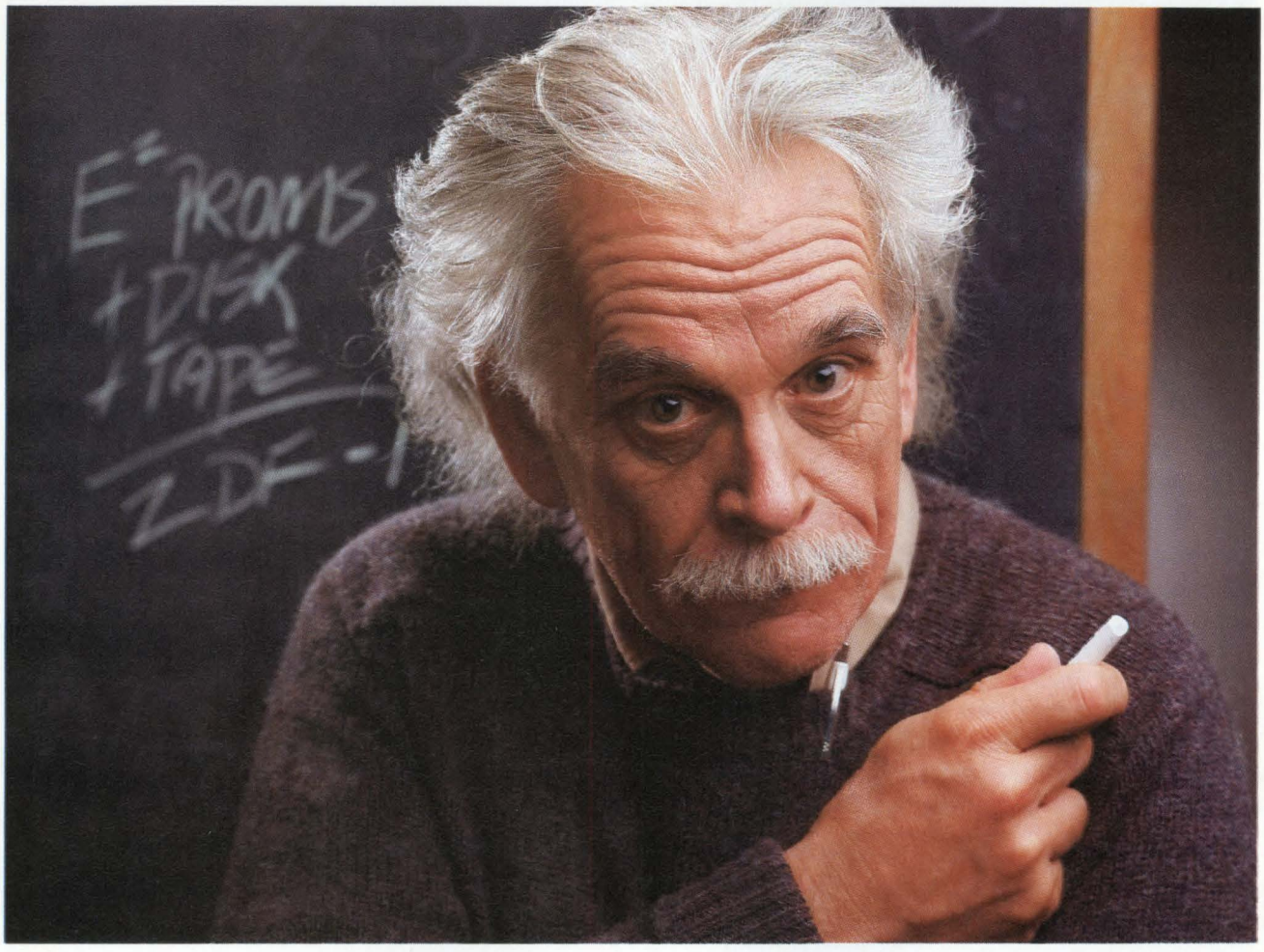
Videotex is a two-way transmission and reception service primarily associated with, but not limited to, phone lines. A subscriber to a videotex system can tap into such interactive services as home banking, shopping, or news. Teletext, on the other hand, is a one-way service from the provider to the subscriber. Its data, usually broadcast over the air, carries such services as news and similar features.

The NAPLPS establishes the rules, formats, and coding schemes that facilitate the interchange of text and graphics information without regard to specific hardware. That is, a picture coded according to the NAPLPS standard will appear the same on different CRT terminals, even if their resolutions differ. The only requirement is that they all decode NAPLPS data in accordance with the standard.

Implementing a videotex system allows the user to tap into a vast reservoir of data.

The designers of NAPLPS had the advantage of hindsight, since several coding schemes had already been written—the previously mentioned Telidon system and the PLP coding scheme. Although the end product carries some traces of the British Prestel standard and France's Antiope system, it is unique. It incorporates data-compression techniques that save time and money in transmitting pictures. It also has a rich assortment of text, graphics, and control functions that should please a technically savvy and discriminating public.

Videotex is interactive in that it accepts information from data bases for transmission to the user. But, it can also accept user information for transmission back to the service provider. Teletext is a one-way service that can only display information sent from the source. The latter is less expensive since its data can be sent on such traditional one-way media as broadcasting stations. The vertical blanking intervals between successive frames on a TV picture are ideal slots into which teletext information can be fit. Videotex, on the other hand, requires a two-way path for which the dial-up telephone network or cable television lines are most immediately practical but which can also include dedicated lines.



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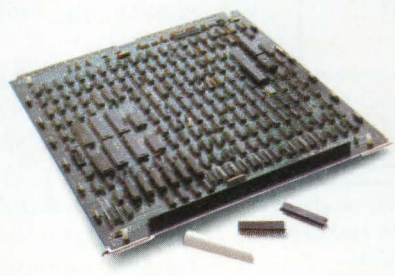

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CIRCLE 52

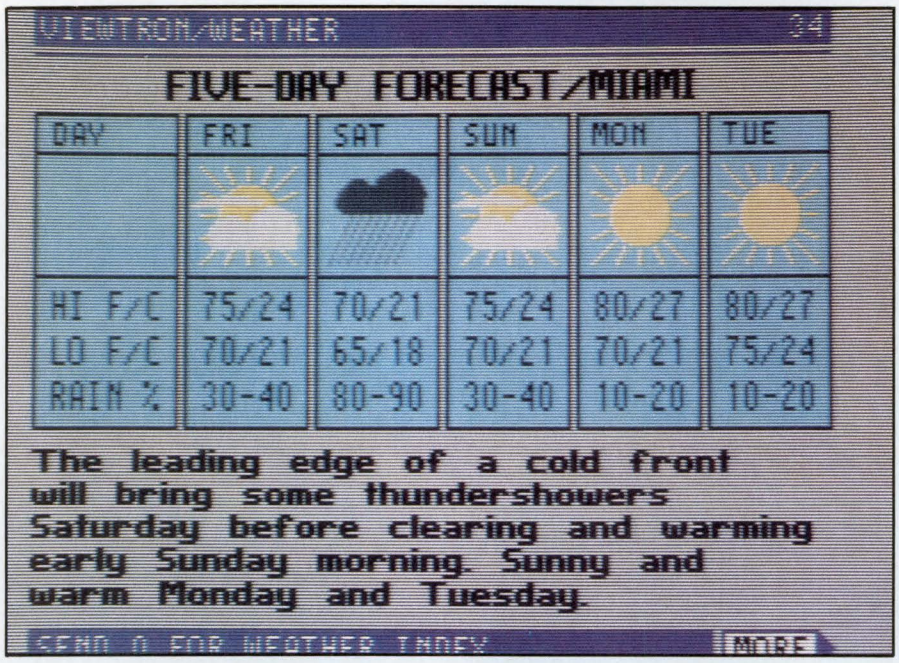


Fig 2 Shown is a sample picture from the Viewtron videotex service currently operating in the south Florida area. This videotex service is based on the NAPLPS standard.

To implement a videotex system, the user needs a terminal; a modem that converts digital to analog; a decoder; and, of course, the transmission lines. The service on a videotex system is usually presented in menu form with the user advancing from a main menu to increasingly more specific offerings. The desired information might be delivered as alphanumeric text, graphics, or a combination of the two (Fig 2).

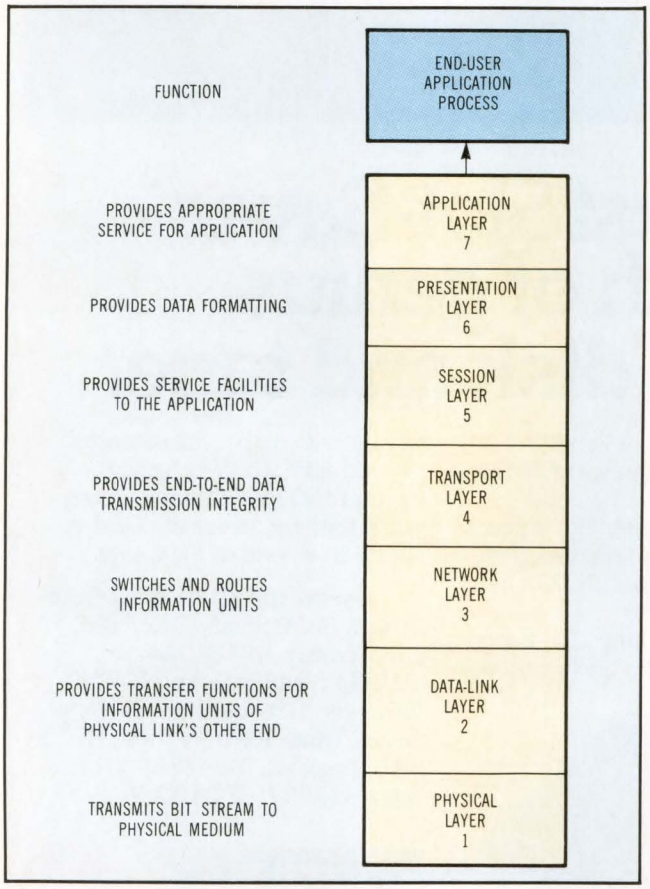


Fig 3 The Open System Interconnection (OSI) model is based on seven functional layers. The NAPLPS standard corresponds to OSI level 6, the presentation level.

Fundamental to NAPLPS is the layered architecture that facilitates the Open System Interconnection model (Fig 3). Basically, data can be easily exchanged between participating systems. The architecture is an assembly of interrelated protocols, which define the entire communication system. Each layer addresses a unique aspect of the system, allowing other protocols to be substituted at various layers. In this way, the data exchange can be accomplished over different transmission media.

Common to videotex and teletext is the presentation layer, which provides a way to represent information in a coding format so that it retains its meaning. There are, however, seven layers that can be portioned into two major groups. Layers 1 to 4 deal with how data is transferred; layers 5 to 7 concern the data itself and how it is processed and used.

The functional layers and what they do

Layer 1 describes the mechanical, electrical and procedural functions that help establish, maintain, and release physical connections. Following that physical layer is the data-link layer, which determines the data-transmission link across one or more physical connections. Included here are error correction, sequencing, and flow control to help maintain data integrity.

The third layer serves the fourth by providing routing, switching, and network access. The succeeding layer, or transport layer, is thus unburdened with how underlying transmission resources are used. It is concerned only with the end-to-end, transparent, virtual data circuit that crosses over one or more tandem network transmission facilities.

Service facilities are provided by the session layer. Here, the procedures for establishing a session connection and supporting the orderly exchange of data and related control functions are detailed. Following the sixth, or presentation layer, are the applications. These protocols provide the actual service sought by the end user. In the seventh layer, for example, information retrieval service commands might be found.

Making use of device independence

Because the entire standard is based on the concept of an abstract Cartesian coordinate system, the NAPLPS is device independent. This system defines all pictorial, textual, and incremental drawing operations. For two-dimensional drawings, the plane consists of a square area called the unit screen. Its points along the X and Y axes range from 0,0 inclusive in the lower left corner to 1,1 exclusive in the upper right corner (Fig 4). In three dimensions, the drawing space is a cube with a Z axis that defines 0 as the furthest point from the viewer.

Since most TVs and monitors have an aspect ratio of 4:3, the entire unit screen will not fit into the active display area. Thus, the unit screen mapped to those devices would range from 0,0 to 1,0.75. Although terminals with different resolutions map the unit screen to their device coordinates differently, the pictures are the same as long as the NAPLPS data is properly decoded.

Coordinate data is transmitted as signed 2's complement binary fractions representing fractions of the unit screen. Because the fractions are written in the abstract terms of the unit drawing area, they may not be represented exactly in the receiving terminal's internal arithmetic. Thus, some approximation is implemented by eliminating unrepresentable LSBs via a truncation process, if necessary.

Data in a NAPLPS system is read from an input stream 1 byte at a time (ie, a byte-oriented protocol). Each byte is interpreted with the aid of a decoding table, the size of which is dependent on the coding scheme. For example, in a 7-bit format, the MSB is not used. That allows a table of 128 entries. On the other hand, an 8-bit format gives a table of 256 entries. The decision to use either format is established by prior agreement of the information provider and the user. It can also be accomplished by commands issued at another appropriate protocol layer.

The decoding mechanism in a NAPLPS system consists of two groups of control functions called C-sets (containing 32 entries each), and four groups of text and graphics functions called G-sets (containing 94 or 96 entries), depending on whether two character codes have previously been assigned the meanings for space and delete. In a 7-bit format, the decoding table will contain one C-set and one G-set at any given time (Fig 5). However, in an 8-bit environment, the table contains two C-sets and two G-sets at any instant (Fig 6).

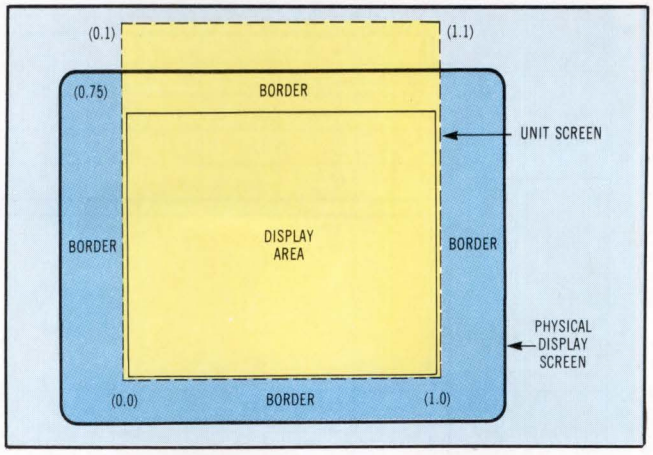


Fig 4 The NAPLPS standard adheres to the unit screen concept. This means that all coordinate data is transmitted as fractions of the unit screen, thus making the NAPLPS standard resolution independent.

The control sets are called C0 and C1 and each has a function. The C0 set contains commands to position a cursor, clear the screen, change the contents of the decoding table, and initiate escape control sequences. The C1 set expands the control-function capabilities of the NAPLPS. It provides commands to turn the cursor on or off, start and stop a blinking function, set the text size, and define operations.

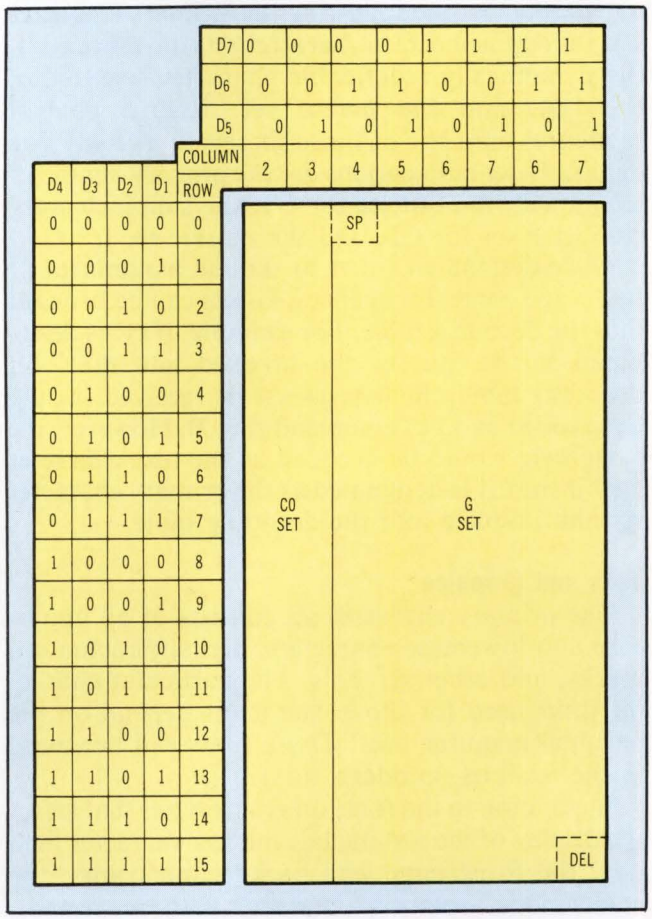


Fig 5 In a 7-bit code environment, the in-use decoding table consists of 128 entries. Here, the table can hold one C-set and one G-set concurrently.

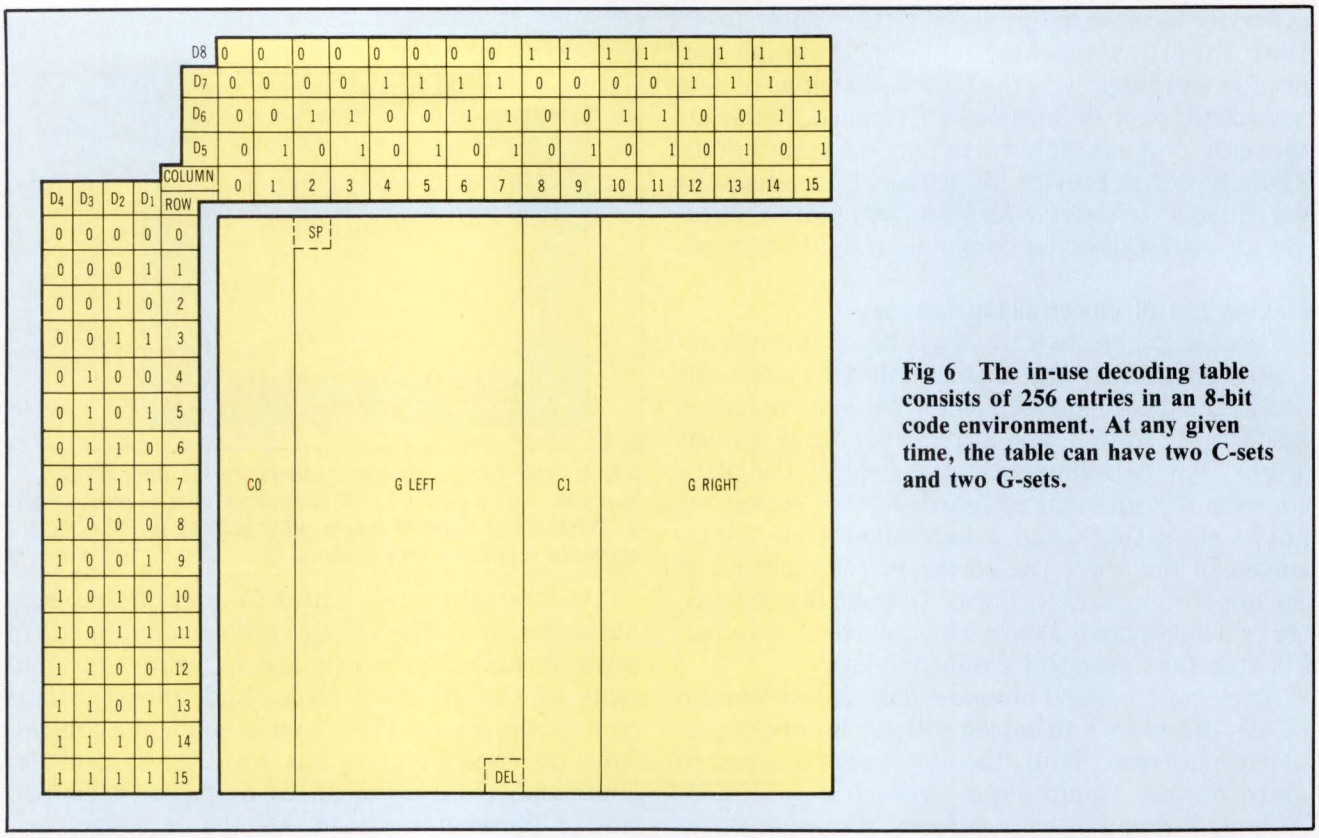


Fig 6 The in-use decoding table consists of 256 entries in an 8-bit code environment. At any given time, the table can have two C-sets and two G-sets.

Each of the four G-sets, G0 to G3, can be designated as one of the following: the primary character set, the supplementary character set, the mosaic set, the dynamically redefinable character set (DRCS), the PDI, and the macro set. Escape control sequences map one of those six sets to a G-set. The default G-set designations are the primary character set for G0, the PDI set for G1, the supplementary character set for G2, and the mosaic set for G3.

Once designated either by default assignment or by escape control sequences, G-sets can be brought into the decoding table. For example, if G1 is designated as the PDI set and invoked into the 7-bit decoding table, the byte Hex31, if received, would be decoded as a PDI command (Fig 7). However, the same byte would be decoded as the text character "1" if the G1 is designated as the primary character set and invoked into the decoding table.

Text and graphics

The primary character set consists of all uppercase and lowercase characters, digits, punctuation marks, and other symbols. The particular character fonts used for those characters depend on the terminal manufacturer. Those fonts will be stored in the NAPLPS decoder's ROM.

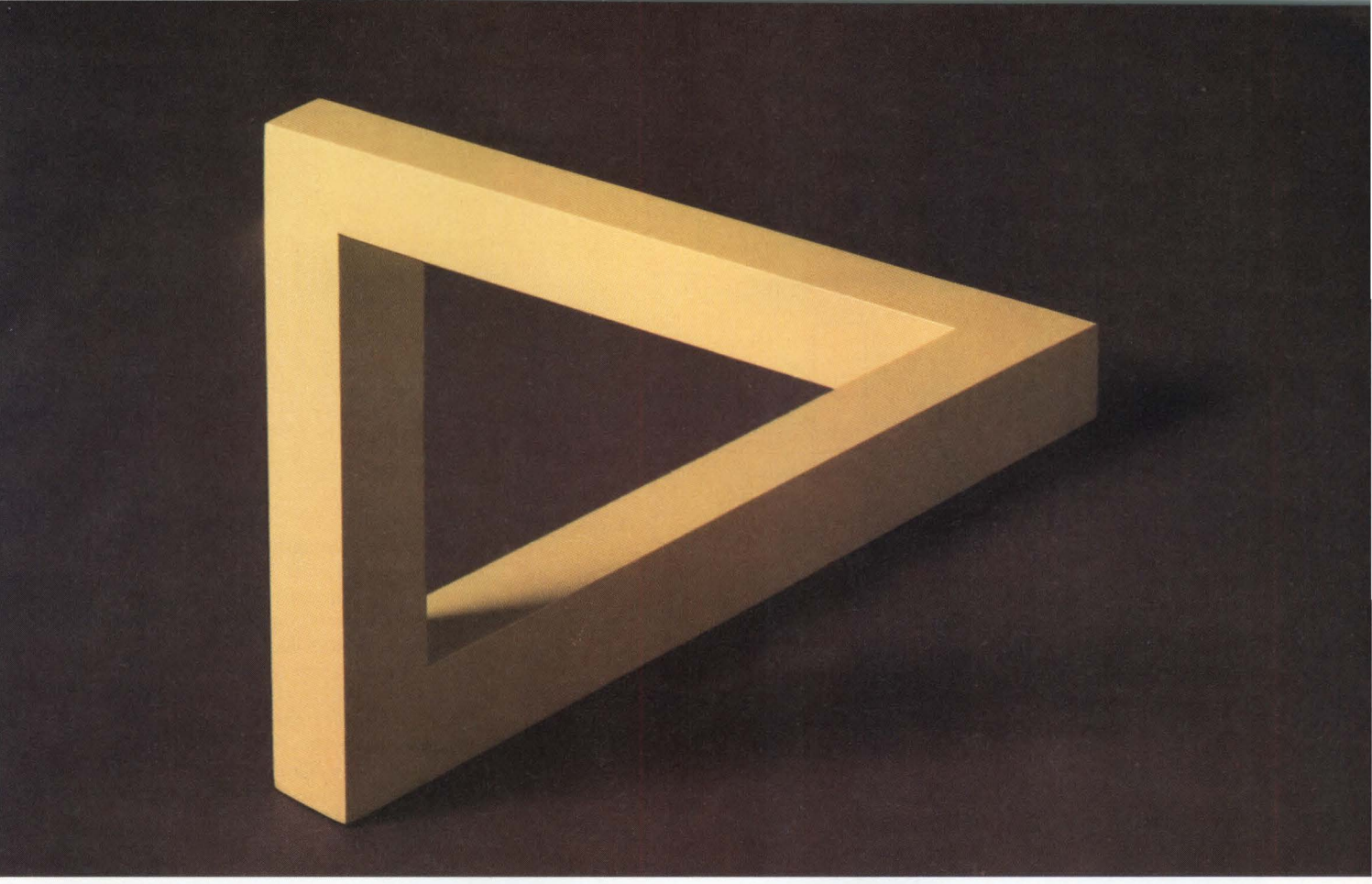
In addition to the font, other attributes that affect the display of the text include the text character field size, the foreground and background colors, the color mode, rotation, character-path movement, intercharacter and interrow spacing, word wrapping, scrolling, and underlining. All are set by using either a PDI control command or a C1 command.

The supplementary set expands the number of characters available and includes accent marks and special characters. Some are nonspacing, so the accent marks can be placed on top of characters. More flexibility is added by the mosaic set, which generates course-resolution graphics. Here, each character cell is divided into six blocks, any of which can be turned on or off. The character code associated with each mosaic determines the representation of the character. Thus, the character fonts need not be stored in ROM. Instead, they can be dynamically generated as the mosaic character codes are received.

To cover all bases, the NAPLPS standard includes a DRCS. This allows the host system to define a special set of characters and use them for generating a display image. These DRCS characters can be defined by implementing any of the various NAPLPS commands.

The picture description set can be divided into three major groups of commands—control commands, geometric drawing primitives, and incremental primitives. The first consists of eight commands that perform such functions as resetting, selecting a drawing color, or choosing a particular line texture.

There are 20 geometric drawing primitives that allow the host system to draw points, lines, rectangles, arcs, and polygons. All are implemented with attributes that have been defined by previous NAPLPS commands. The four incremental drawing primitives permit transmission of pixel maps and allow groups of lines or filled polygons to be represented in a compressed manner.



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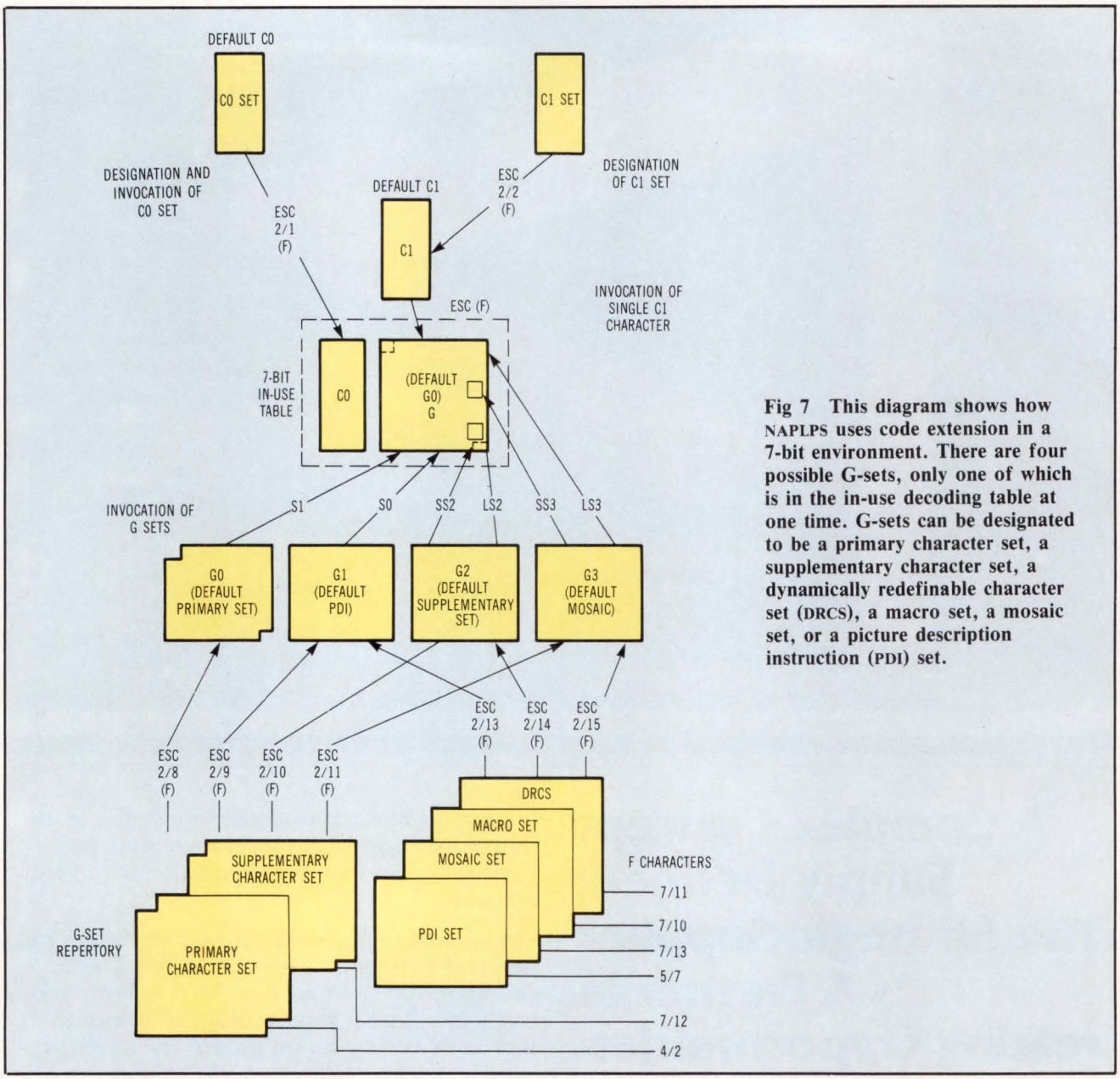

Fig 7 This diagram shows how NAPLPS uses code extension in a 7-bit environment. There are four possible G-sets, only one of which is in the in-use decoding table at one time. G-sets can be designated to be a primary character set, a supplementary character set, a dynamically redefinable character set (DRCS), a macro set, a mosaic set, or a picture description instruction (PDI) set.

Coordinate data for graphics representation is transmitted as signed, 2's complement binary fractions with from 1 to 8 bytes used to specify a coordinate pair. To distinguish a PDI command from coordinate data, the former have bit 7 equal to 0 and the latter equal to 1.

In a two-dimensional system, X, Y coordinate values are coded. Each byte represents 3 bits of X data and 3 bits of Y data. The first byte specifies the sign bit, followed by the MSB to the right of the decimal point. Each byte that follows specifies more data with each bit of lower significance.

In a three-dimensional system, the X, Y, and Z coordinate values are encoded. Each byte represents 2 bits of data for determining the X axis, 2 more for the Y axis, and 2 bits for the Z axis.

The eight PDI control commands help determine the specific attributes of the displayed graphics and text. Reset selectively reinitializes control parameters and attributes to their default values. The screen can be cleared and the screen border color reset. The color mode can also be reset with or without changing the drawing color. Attributes set by other PDI control commands, such as text, domain, and texture, can be reset to default values, as can blinking, unprotected fields, macros, and DRCS character definitions.

The domain command sets the length of both single-value and multiple-value operands. These operands signify the length of byte strings for the numeric data fields of the PDI command, which specifies control, attribute or coordinate parameters required by the commands. It also determines dimensionality and the size of the logical pel—a geometric construct whose size determines the stroke width and height used in drawing the graphics primitives. The NAPLPS document advises that although the terms pel and pixel are often synonymous, for the purposes

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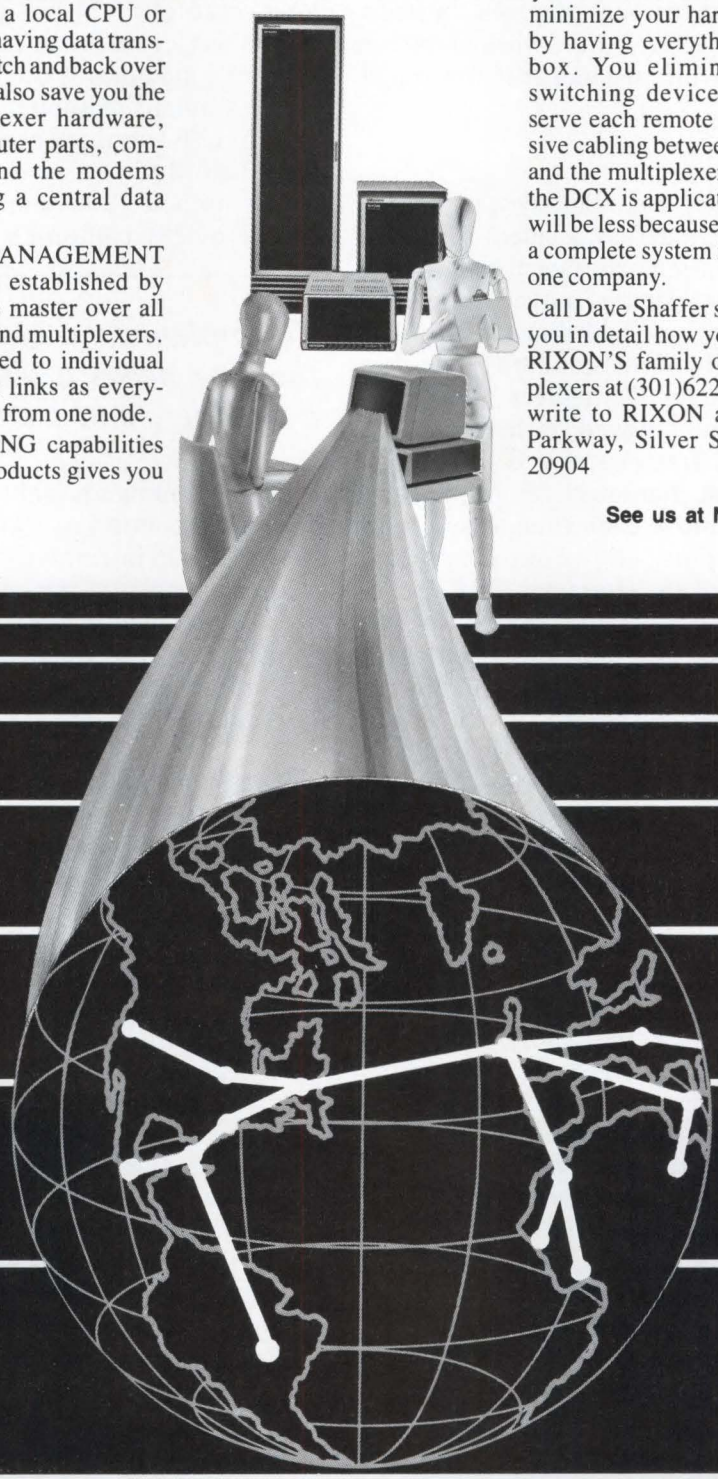

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CIRCLE 54

of the document, pel is a logical picture element, but pixel refers only to a physical picture element. Thus, the logical pel can map onto several pixels.

A single-value operand can range in length from 1 to 4 bytes and can specify color indexes and the timing value of a blinking function. On the other hand, multiple-value operands can be up to 8 bytes long and can determine coordinate data and the values of color maps. Dimensionality can specify either two- or three-dimensional graphics construction. At present, the latter is not considered, but the NAPLPS does provide mechanisms for future standardization.

Moving text

The content of the text command determines the movement of characters across a videotex screen. Such attributes as rotation, character path, intercharacter and interrow spacing, move parameters, cursor style, and character field dimensions come into play. The versatility of the standard allows text to be rotated 0, 90, 180, or 270 degrees. Characters can also be automatically moved to the right, left, up, or down as the character string is displayed.

The spacing between characters determines how much the cursor will move each time a new character is displayed. A choice allows movement in 1, 5/4, or 3/2 multiples of the character field size. In addition, characters can be proportionally spaced. The precise intercharacter distance is determined solely by the character being displayed. A choice is also available for interrow spacing, which can be 1, 5/4, 3/2, or 2 times the character field size.

The cursor is used to position text and the drawing of point position graphics. Both are repositioned with regard to each other by use of the move parameters. Both can move together, independently, or with either leading. Plus, four cursor styles are provided: an underscore, a block cursor, a crosshair, and a custom cursor. Finally, the character-field dimensions determine the size of the displayed text characters. A default character field size is 1/40 by 5/128 of the unit screen.

Line textures can be varied for different effects. For example, they can be solid, dotted, dashed, or a combination of the latter two. Highlighting can also be turned on or off for perimeters of filled arcs, rectangles, and polygons. Textures for filled areas can be solid, vertical, horizontal, or cross-hatched. The thickness of the hatch is determined by the logical pel size. Also permitted are four host-defined texture masks.

The NAPLPS specifies three color modes: one direct and two indirect. Direct color mode 0 specifies a color that is written directly into the graphics bit-mapped memory whenever it is the color currently being used. Indirect modes 1 and 2 apply when color paletting or mapping is used. Color index values are written into the graphics memory, which in turn will address the color palette to provide the required color information. Color mode 1 handles foreground color paletting; mode 2, both foreground and background. In modes 1 and 2, the set color command sets the values in the palette.

Set color operands can range in length from 1 to 8 bytes for a total of 48 bits of information (6 bits of color information to a byte). On the other hand, select color operands can be from 1 to 4 bytes long—a total of 24 bits of information.

The service reference model (SRM) for NAPLPS is a set of guidelines specifying a conformance level to the standard. Although the videotex/teletext SRM specifies 16 simultaneous colors from a palette of 512, the full NAPLPS provides the capability for up to 16 million (2^{24}) simultaneous colors from a palette of 281 trillion (2^{48}).

To implement a videotex system, the user needs a terminal, a modem, a decoder, and transmission lines.

Other commands include wait, which puts delays into the execution of NAPLPS data. The exact time is specified in intervals of 0.1 s. The blink command causes an entry in the color map to blink between two colors. The process first specifies the color to which the current color should change, and sets the on and off intervals as well as the start delay. Here too, all intervals are in 0.1-s units.

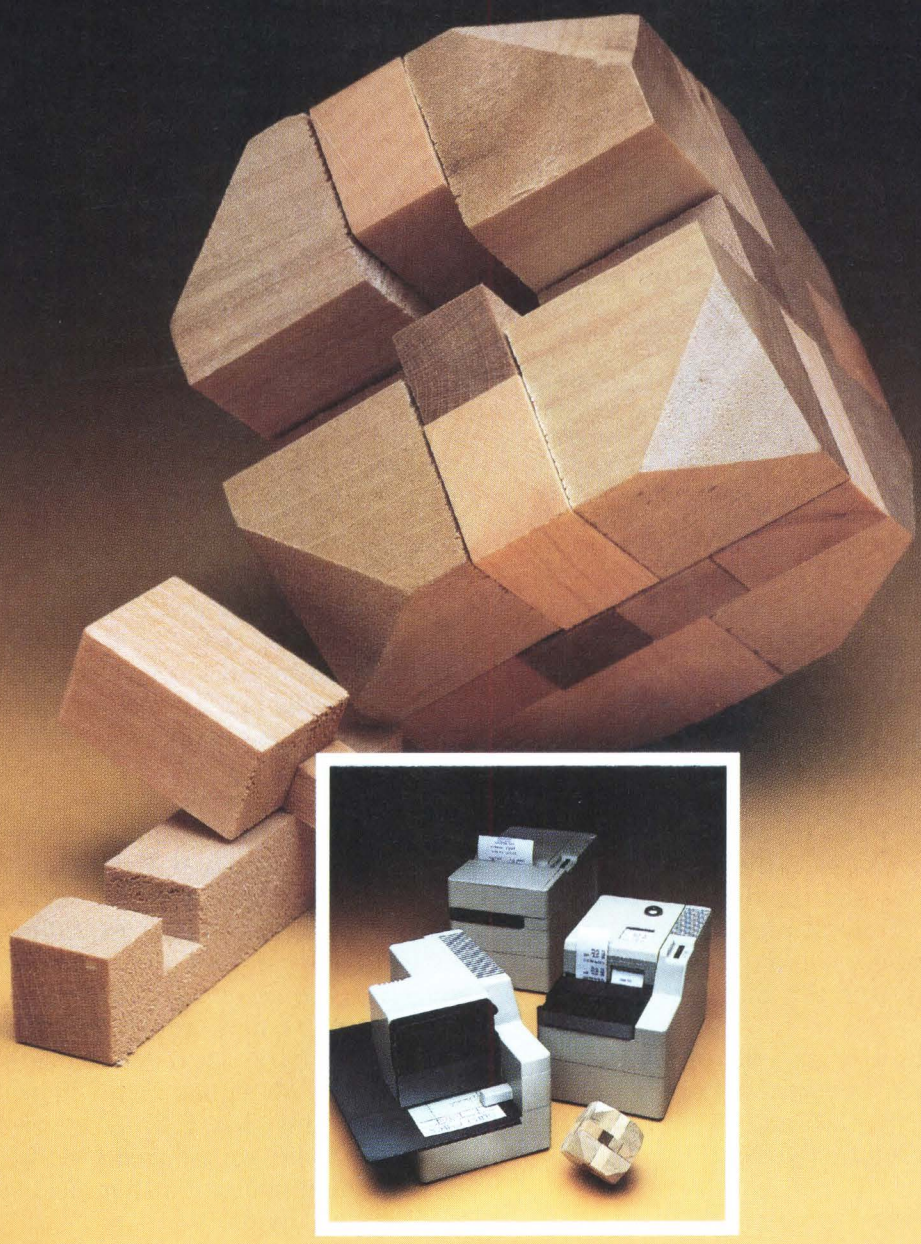
Filling in the blanks

The point command positions the drawing point but may or may not display a point itself. Coordinate data following the point can be interpreted as either absolute or relative. That gives four types of commands: absolute/invisible, relative/invisible, absolute/visible, and relative/visible. The visible point is drawn with the dimensions of the logical pel.

There are four line commands as well: line absolute, line relative, set-line absolute, and set-line relative. The first two use the current drawing point position as the first point of the line. The set-line commands specify both end points of a line. Absolute coordinates give the position of the end point directly. Relative coordinates, on the other hand, add to the current position of the drawing point to generate an end point position.

Unlike the line, three points are needed to draw an arc: the starting point, an intermediate point on the arc, and the end point. Arc-outlined and arc-filled commands use the current position of the drawing point as the starting point of the arc. Set-arc commands give the starting point in absolute coordinates.

Arcs can be either outlined or filled. When filled, the area between the arc and the chord connecting



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An advanced video display processor

The TMS9228 video display processor is an upgraded version of the TMS9918A family of video display processors found in the TI-99/4A home computer, ColecoVision, Coleco Adam home computer, and the Japanese MSX standard. The software-compatible processor implements the same 40-char/line text mode, graphics I mode, and graphics II mode as its predecessor. In addition to these modes, the unit has an 80-char/line multicolored text mode, and graphics modes III, IV, and V. Graphics modes I to IV are pattern graphics modes, while the graphics mode V is fully bit mapped.

The graphics V mode of the TMS9228 is designed primarily to cost-effectively implement the requirements of the NAPLPS service reference model (SRM). The SRM has a set of guidelines defining a minimum conformance level of the NAPLPS standard that both data providers and terminal manufacturers should follow. This mode is a full bit-mapped graphics mode with a 256 x 210 resolution with 4 bits/pixel. There are 16 simultaneous colors selectable from a color palette of 512. The onchip color palette replaces a large amount of external circuitry found in other graphics systems.

Other major features include 32 multicolored sprites with up to 10 sprites on one line. A block move command relieves the CPU from having to move large amounts of data in the video RAM. A programmable interrupt signals the CPU on completion of any specified horizontal scan line.

An onchip sound generator is compatible with the TI SN76489. Video outputs include color difference signals, or RGB. There is the ability for the CPU to perform DMA operations into the video display processor's video RAM. The external video interface allows the cascading of multiple video display processors or the ability to synchronize an external video signal for graphics overlay capability.

the two end points is filled. Circles are drawn simply by making the arc's starting point equal to its end point. Alternatively, circles can be drawn by defining an arc command with just two points that specify the diameter of the circle. If more than three points define the arc command, a curvilinear spline is drawn.

Like arcs, rectangles can be outlined or filled. The set-rectangle command gives the beginning point in absolute coordinates and the diagonal point in relative coordinates. Conventional rectangle commands use the current drawing point as the beginning point and then give the diagonal point in relative coordinates.

Polygon commands process a list of coordinate data that is interpreted as vertices. Polygon edges should not cross each other and the number of vertices supported should be at least 256.

More drawing primitives

Several incremental drawing commands enhance a display. For example, the field command defines a rectangular region in the unit screen, while the default field is the entire screen. The field, once defined, can be used for columnating text—specifying areas of the screen that are protected and unprotected, as well as an area of the screen used by the incremental point command. That command helps download a bit-mapped graphics image into a previously defined field on the screen. Of the two operands that follow the command, the first is a packing counter that determines how to group bits of the bit stream to form the color information for each point. The second operand is the data bit stream.

If the packing counter is 4, every 4 bits from the bit stream will be grouped together. The incremental point is executed by taking color information from the bit stream and placing it in the graphics bit-mapped memory corresponding to the position of the drawing point. That point is automatically moved to its next position, depending on the dimensions of the logical pel. The point size also depends on the logical pel. The entire process is repeated until the end of the bit stream.

Complex line drawings, such as personalized signatures, can be drawn using the incremental line command. This command presents such drawings in a compact and compressed form and, like the incremental point command, is followed by two operands. The first gives the dx and dy step size parameters. The second is a series of bytes that supplies the move and draw instructions.

The step size parameters determine the distance, in the dx and dy directions, that will be used by the move instructions that follow. Every 2 bits, excluding the 2 MSBs, are grouped together to indicate a line drawing instruction. That yields three move instructions per byte.

The incremental polygon command is very similar to the incremental line command with the exception that the draw-flag indication is always on. If a modifying parameter is received that attempts to change the draw flag, it is treated as a null.

Finally, the macroinstruction set provides mechanisms for data compression as well as for creating pictures with structure. A macroinstruction is a string of locally buffered NAPLPS commands. These commands are stored in a decoding terminal's RAM. Once a macro is defined, it can be executed by sending a single byte of information—the macro name. That requires the macro to be part of the 96 commands that are designated to a G-set and are in the currently used decoding table.

Implementing a NAPLPS decoder

Most NAPLPS-based videotex decoders built today are designed using CRT controllers and many MSI

and SSI components to achieve the functionality required by the NAPLPS SRM. As a result, these videotex decoders are not very cost effective. Widespread commercial videotex is on the horizon and has been for some time. In order for videotex to become a nationwide commercial reality, the cost of the NAPLPS videotex decoders must be reduced to a price acceptable for the consumer. When this happens, the long-awaited videotex explosion will occur.

There are many problems that relate to cost in designing a NAPLPS-based videotex terminal. In order to conform to the NAPLPS SRM, the resolution should be on the order of 256 x 200 pixels with 16 simultaneous colors. This is usually implemented with 4 planes of bit-mapped graphics memory, yielding 4 bits/pixel. In addition, a 512-color palette is necessary to provide the color shading and flexibility demanded by videotex advertisers and graphics artists. The color palette, in most designs to date, has been implemented external to the CRT or video display processor controlling the graphics memory. This amount of external circuitry is one of the reasons NAPLPS videotex decoders are so expensive today.

Texas Instruments has developed a video display processor, the TMS9228, which was designed in parallel with the NAPLPS standardization efforts (see Panel, "An advanced video display processor"). Now, a NAPLPS-based videotex terminal can be designed to completely conform to the NAPLPS SRM at a low cost. The graphics V mode of the video display processor is a full bit-mapped graphics mode with 4 bits/pixel with a 256 x 210 resolution. There are 16 simultaneous colors available selectable from a color palette of 512. The onchip color palette reduces the chip count and overall system cost considerably.

This video display processor can also be used in applications besides videotex. Its powerful animation capabilities, such as multicolor sprites, are used in videogames. Also, its 80-char text mode can be used in personal computing applications such as word processing, accounting, and spreadsheet analysis.

Ultimately, there will be the home information system. The functional characteristics of personal and home computers, videotex, videogames, education, and many other features will merge together into one unified system. The TMS9228 video display processor is one graphics device that can serve all of these needs.

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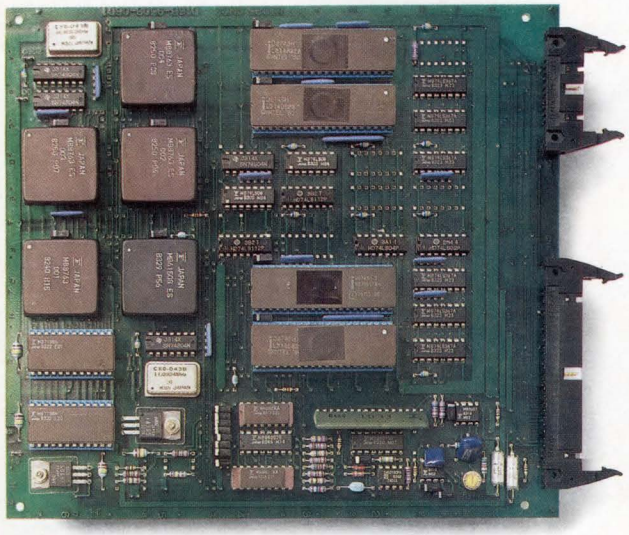

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CIRCLE 56

THE CASE F

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CIRCLE 59

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SHIFT REGISTER MANEUVERS DATA TO ADD PRINT FEATURES

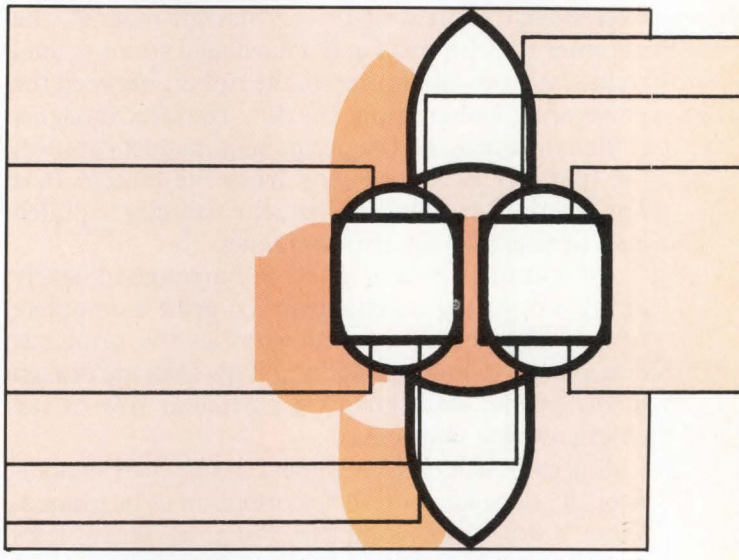
Using custom LSI techniques, a special type of shift register allows dot-matrix line printers to offer upgraded print and data-formatting features.

by Philip Gordon

With today's increasingly sophisticated data processing applications, users of dot-matrix impact line printers often require flexible document formatting and other advanced features. When printers were simpler, the physical structure of the print mechanism posed few interfacing problems for designers of printer controllers. However, earlier dot-matrix printers offered limited features compared with today's models. Thus, because of the growing complexity of printers, a new electronic design technique is recommended to format and sequence the dots that drive the print-mechanism hammers.

Sequencing problems would be eliminated if the impact printer mechanism could accept direct raster-scan type data. For example, the printer's control electronics, called dot-generation logic (DGL), would be quite simple if designers used a single, large shift register loaded with an entire print row's bit image during the nonprinting print-bar turnaround time. Such a shift register has one storage cell for each dot that can be placed across the print row during a single pass of the bar. The shift register also has taps spaced evenly over its length—one tap for each hammer in the printer. Each tap, therefore, drives a single hammer. This basic shift-register concept yields such advanced printer features as mixed character-set pitches and proportional line spacing.

Until a few years ago, implementing a large shift register of the type described was a technological



disaster. Large static shift registers—512 to 2048 bits—are unsuitable since they are accessed serially (no taps are provided). A TTL shift register can be built from standard MSI devices, but this approach is prohibitively expensive. However, an economical and viable alternative for a controller designer capitalizes on advances in custom LSI technology. A custom LSI component using standard MOS processing costs just a few dollars. Design expenses and risks are also minimized because the chip layout is a repetitive series of shift-register partitions.

This strategy has been adopted by Hewlett-Packard for its two recent dot-matrix line printers, the 300-line/min model 2563A and the 900-line/min 2566A. With improved DGL circuitry, character text is printed at several fixed pitches, and proportional spacing is planned.

At the heart of the 2563A and 2566A DGL models is a Hewlett-Packard designed and fabricated MOS LSI shift register. The device contains a 2772-bit, single-direction main shift register having 132 output taps stationed every 21 bits. It also includes an

Philip Gordon is a development engineer at Hewlett-Packard's Boise Division, 11311 Chinden Blvd, Boise, ID 83707, where he is responsible for digital system design for printer controllers. He holds a BSEE from the University of California at Berkeley and an MSEE from Stanford University.

132-bit bidirectional parallel-to-serial output shift register. The main register is cleared and filled in 2 ms, well within the 4-ms print-bar turnaround and paper advance time of the faster 2566A printer. When the shift register is used in the 33-hammer 2563A printer, an external divide-by-four circuit loads every fourth bit from the output shift register into a 33-bit hammer-driving shift register. Proper synchronization guarantees that 99 of the 132 output bits are discarded and not externally stored. This effectively programs the LSI device as a 2772-bit main shift register with 33 useful taps 84 bits apart, and a 33-bit output shift register.

Covering the dot-matrix basics

The basic dot-matrix impact printing operation involves the electromagnetic release of a spring-steel tine called a hammer. In a captured-hammer design, the hammer tips are drawn away from the paper by a small permanent magnet. When the electromagnet overcomes the field of the permanent magnet, the hammer flies forward and a hardened stylus or ball welded near its tip impresses the ribbon between the paper and platen to print the dot. The electromagnet is then disabled and the permanent magnet captures the hammer as it rebounds from the platen. In a noncaptured-hammer design, the hammer is pulled and released by an electromagnet.

All hammers and magnets are arranged linearly along a print-bar mechanism. To print a complete row of characters, a motor shuttles the print bar horizontally to multiple dot positions. Dots are printed in the proper locations of a particular row of the character dot matrices.

Any combination of hammers can be fired simultaneously, depending on the information to be printed. When a dot row is complete, the print bar reverses direction while a stepper motor advances the paper the distance of a vertical dot row; the next row of dots for the characters is then printed on the line.

A full-width line printer must print text at a density of 10 chars/in. (10-pitch) across at least 13.2 in. of the paper. Most dot-matrix printers use 132, 66, 44, 33, or 17 hammers spaced evenly along the print bar at intervals of 0.1, 0.2, 0.3, 0.4, or 0.8 in., respectively. Theoretically, if both the print-bar direction reverse (turnaround) and paper-step advance times are 0, a printer with 132 hammers moving approximately 0.1 in. will print twice as fast as a similar printer having just 66 hammers that must travel 0.2 in. Both times are significant considerations in printer design, so the ultimate speed is not merely a linear function of the number of hammers. Still, high speed printers usually have more hammers than their slower speed and lower cost counterparts.

A dot-matrix impact line printer's control electronics can be organized for convenience into I/O, control-microprocessor, and DGL sections. Data must pass through the I/O system, be parsed for control information and nonprintable characters, and be formatted by the microprocessor. Finally, it must be converted into dots and passed to the print mechanism in the proper order by the DGL.

The DGL usually includes a buffer memory for all active characters to be printed on a line; either a microprocessor or algorithmic state machine with arithmetic and programmable dot-extraction capability; various character-set, dot-image ROMs; and frequently, a dot-image buffer. Fig 1 shows the organization of these elements. The dot-position detector at the bottom generates print strobes each time the print bar passes a printable dot location. The hammer-driving electronics comprise a series of identical latches and high voltage current-switching circuits for the electromagnets.

While conversion of ASCII-coded information into the proper dot images is not difficult, the DGL's formatting and sequencing of the dots to the hammers can be troublesome. Although a dot-matrix printer appears to print a single dot row at a time,

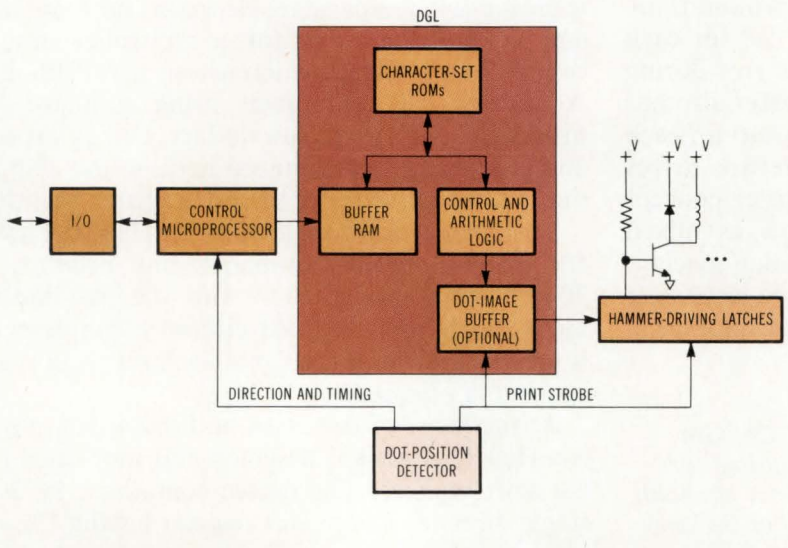


Fig 1 The basic control electronics of a dot-matrix line printer include an I/O section, a control microprocessor, and dot-generation logic (DGL). If a large shift register is used in the DGL, the overall logic is much simpler than in conventional implementations.

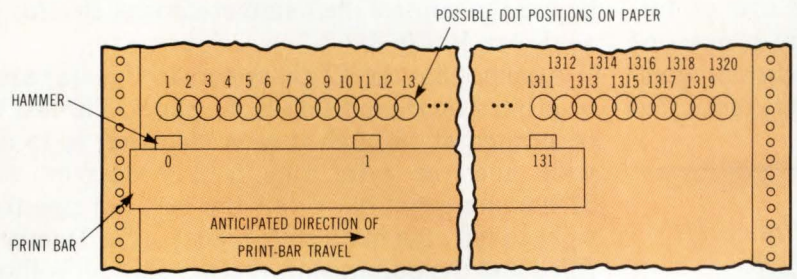


Fig 2 Dot routing and sequencing are important tasks of the DGL. The print bar begins this print pass at the far left of a page, and prints a single row of 1320 dots as it moves to the right.

the hammer-driving circuits cannot collectively accept simple raster-scan dot data like a video display unit. For example, as the print bar on a 132-hammer line printer moves from one extreme position to the other, each hammer passes across its exclusive 0.1-in. print area. Each hammer prints as a 0.1-in. mini-raster scan, but the print bar, viewed as a unit, appears as a conglomeration of 132 disjointed raster scans.

Dot-image data must be ordered to compensate for the print mechanism's physical geometry. If the print bar mentioned above covers 13.2 in. of paper at a dot density of 100 dots/in., the first 132 dots printed simultaneously as the bar passes across the first printable position are those numbered 1, 11, 21,...1311. The next 132 dots printed simultaneously are numbered 2, 12, 22,...1312. The final group of 132 dots will be numbered 10, 20, 30,...1320. Fig 2 illustrates the printer mechanism and the various dot positions that can be printed.

The importance of hammer spacing

Spacing between print hammers on simple dot-matrix line printers is an exact or integral multiple of the printable horizontal character width. This lets the DGL be quite simple, and characters are not divided between adjacent hammers. Division between hammers can accentuate any alignment inconsistencies. In a simple printer, the ASCII-to-dot conversion and dot-sequencing algorithm are uncomplicated. No matter where the print bar is during a pass, all hammers print the same dot column of the characters at the same time. Each printable character is mapped through its dot-image ROM, yielding 8 bits. Then, based on the column being printed, 1 bit is extracted and passed to the hammer-driving electronics. All printers can easily print standard 10-pitch characters. It also follows that DGL could print 15-pitch characters if its hammers were spaced 0.2, 0.4, or 0.8 in. apart. It could print 13.3- or 16.7-pitch characters if its hammers were 0.3 in. apart.

An enhanced DGL is required to print character text at a density that does not explicitly fit the hammer spacing. In addition, dots from characters that are printed simultaneously can originate from different columns within the characters. Modulo arithmetic can supplement the logic required for the most simple case above. That would allow for processing and simultaneous printing of, for example, the first column of the first character, the third column of the second character, the fifth column of the third character, and so forth.

Logic of greater complexity is required if the instantaneous character pitch is permitted to change within a print row. Although rare in existing line printers, this is required for printing proportionally spaced text, and for performing character kerning and a more efficient right-margin justification.

Proportional spacing requires variable-width characters. For example, the letter I is narrower than a W. Kerning goes a step further by selectively narrowing letter widths if adjacent characters can be squeezed close together. Right-margin justification adds blank characters between words on the print line. Variable-width blank characters can eliminate visibly irregular interword spaces by making all spaces appear equal. These features require either a dedicated microprocessor or more substantial arithmetic logic to track changing character widths and dot positions, and to send the dots in proper order to the print hammers.

The ASCII-to-dot conversion process is inefficient in DGL subsystems that do not include buffering for the entire dot-image row. Each byte-wide, dot-image ROM location can be accessed up to 8 times—1 bit at a time—along a print row. In the highest speed and/or highest dot-density printers, this can limit performance since the time between print strobes (hence the dot-image generation time) is relatively short. A RAM buffer that stores an entire line of dots is included sometimes to allow storage of the 8 useful bits from each ROM access. The RAM's logic can be complex because the number of hammers on a bar, the range of dots for each hammer, the character width, and the printer's horizontal dot density are rarely exponents of 2, which is preferred.

A raster-scan system for printing

If an impact printer mechanism could accept raster-scan data, the DGL would be very simple. A large shift register with a storage cell for every dot and a tap to drive every hammer has this capability. The shift register can be clocked on each hammer activation, bringing the next printable set of dots to the taps in preparation for the next hammer sequence.

The shift register acts as an ideal and complete line buffer that complements the geometry of the print bar exactly. The DGL builds the row of dot-image print all at once, so no duplicate accesses of the character-set ROMs are required. With progressive LSI technology, such a shift register, fabricated in low cost MOS, is easily built.

To hold down system cost, the shift register should be as small and inexpensive as possible.

In operation, the DGL's algorithmic state machine fills the shift register with the exact data image to be printed during the next pass of the print bar. Either a single-direction or bidirectional register can be used. A single-direction register, however, must be filled differently for each direction the bar travels. Both types require a tap multiplexer or tap gathering bidirectional output shift register to compensate for the direction of bar travel.

To hold down system cost, the shift register should be as small and inexpensive as possible. By folding a large, but less complex, single-direction main shift register together with a small, but more complex, bidirectional shift register into a custom LSI design, the number of package pins can be limited to 14. Multiple 8-bit TTL single-direction shift registers adapt well to the LSI device's serial output and can be used to control the hammer-driving electronics, as shown in Fig 3.

Assume that the 12 characters in Fig 4(a) are to be printed on the left side of the paper. The text will be printed at 10-pitch if each character is 15 dots wide and the print rate is 150 dots/in. If a 33-hammer print bar prints the next dot row from right to left, the main shift register (Fig 3) must be filled and the output shift register shifted as shown in Fig 4(a). The hammers begin the pass just to the right of D, H, and L, as shown. If the bar prints from left to right, the main shift register must be filled in reverse, and the output shift register shifted with the hammers beginning the pass just to the left of A, E, and I, illustrated in Fig 4(b).

DGL processing begins with the information held in its buffer RAM. Assume that the left-most character on the print row is always stored at address 0 and character ordering follows upward (higher addresses). Assume further that the ROMs hold the character-set dot images. Since each character image can be up to 15 dots wide, 2 bytes representing one dot row are packed, one after the other, in the ROMs. Byte 0 stores the right-most bits (dots) and byte 1, the left-most bits. The general ASCII-to-dot conversion algorithm that yields the results in Fig 4 can be summarized by the following examples.

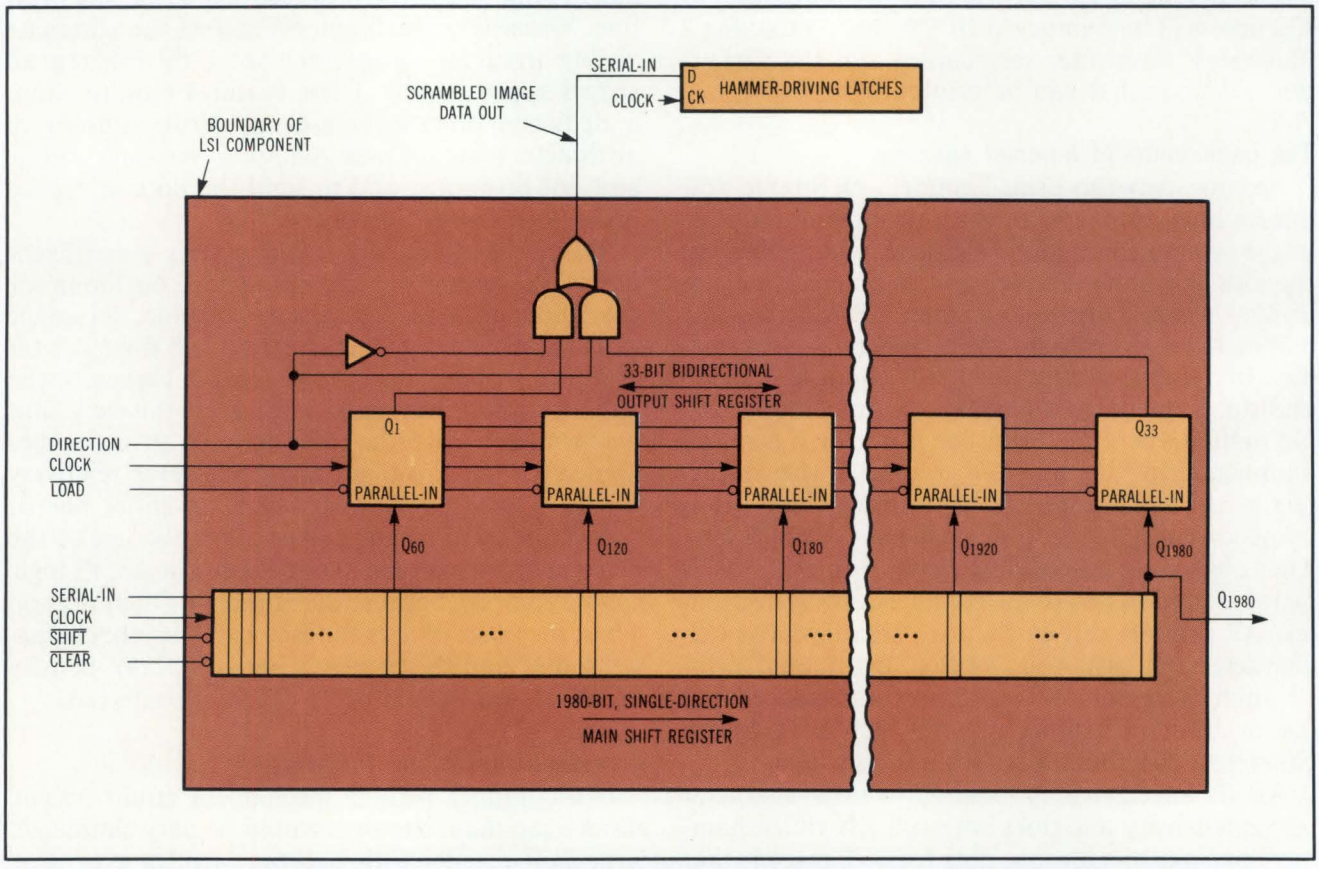


Fig 3 This 1980-bit LSI shift-register component supports a 33-hammer line printer at 150 dots/in. The hammers, 0.4 in. apart, can reach and print 60 dots. A 33-bit bidirectional shift register supports the main register and compensates for the print-bar direction.

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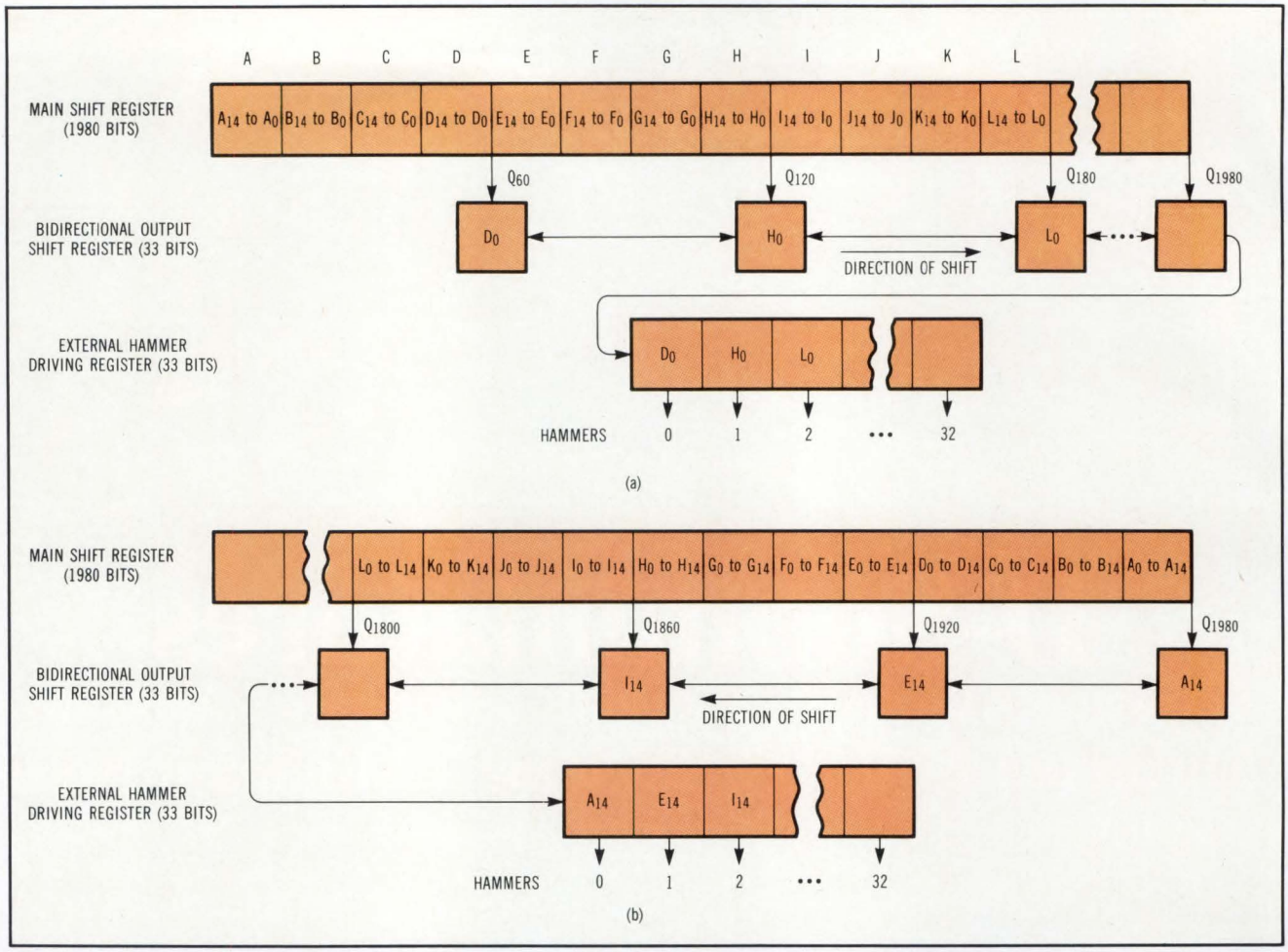

Fig 4 Each of the 12 characters above (a) is 15 dots wide and the printer prints at 150 dots/in. If the print bar prints from right to left, the hammers begin the pass just to the right of the D, H, and L. When the main register is filled, the output register is shifted (b). If the print bar moves from left to right (hammers begin the pass just to the right of A, E, and I), the main shift register must be filled in the reverse order, and the output shift register is shifted.

If the print bar prints from right to left, characters in buffer RAM are addressed from the highest possible address down to 0. Dot-image bytes in the character-set ROMs are then accessed in order—0 to 1—while first shifting in the LSB (ultimately, the right-most dot on the paper) of each byte. This continues for all characters until the last character (left-most on the paper) at RAM address 0 is completely processed.

If the print bar prints from left to right, with the main shift register clear, a dummy 1 bit is injected as a termination flag. Characters in the buffer RAM are addressed from 0 upward. Dot-image bytes in the character ROMs are accessed from 1 to 0, shifting the MSB (left-most on the paper) of each byte first. This continues for all characters until the termination flag leaves the end of the register. If the buffer RAM is filled with variable-width characters, the termination flag provides the easiest way to know when the bits of the first character reach the precise end of the main register.

Using a more complex bidirectional main shift register, the algorithm would operate as though the print bar always traveled right to left, except that the register would be filled from its other end in the true left-to-right direction. Other algorithm changes include the absence of a termination flag, but the end result would be the same as in Fig 4.

After the main register is loaded and the turnaround interval complete, each print strobe generated by the dot-position detector should parallel-load the output shift register and then shift the main register by 1 bit. The next 33 clocks to the output register should pass the register's contents to the external hammer-driving shift register. These bits represent the dots to be printed on this strobe.

Implementing a fill algorithm

Fairly elementary DGL can support a full-featured 150-dot/in. printer. It can offer popular fixed-character pitches such as 10 (width = 15), 15 (width = 10), and 16.7 (width = 9). With intelligent computer or control-microprocessor firmware, features such as proportionally spaced characters, kerning, and a more smooth right-margin justification can be completed.

Assume the buffer RAM holds 512 bytes, divided into 256 character text entries, each 2 bytes. The

SUDDENLY THE TAPE CONTROLLER IS OBSOLETE.

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first byte is the 7-bit ASCII code; the second byte is the character-set ROM number in the upper 4 bits and the character width in the lower 4 bits. This allows for 16 selectable character sets and character widths up to 15 bits (dots) wide. ASCII blanks can fill much of the buffer. Fig 5 illustrates a logic system that implements such DGL. The shift register fill algorithm for the system is shown in Fig 6. Each of the seven states in Fig 6 operates in the following manner.

Fairly elementary dot-generation logic can support a full-featured 150-dot/in. printer.

State 0, for example, is the normal nonprocessing state. At the start of the print-bar turnaround period, the control microprocessor updates the dot-row number and passes other relevant data to the DGL. Then, it commands the DGL to convert the characters from buffer RAM into dots for the main shiftregister. Inserting the termination flag into the main register is state 1, if the print bar is to travel from left to right. State 2 draws byte 1 from RAM and stores the character-set number into its register, the width into counter 0 and, depending on the bar direction and how the dot-image bytes are to be serialized, either the width itself or 0s into counter 1.

In addition, state 3 draws byte 0 from RAM and stores it into the ASCII character latch. Counter 0 is decremented to set it up properly for state 5. Moreover, state 4 prepares counter 1 to be the correct value to drive the parallel-to-serial multiplexer, while state 5 is the workhorse state that passes a dot into the main register. The latter is executed successively as many times as the character is wide. This is indicated by the character-width counter reaching 0. Row processing is complete if the termination flag appears.

Finally, state 6 checks for a terminal value of the RAM addressing counter. This is 0 or FF, depending on the print-bar direction. This is an alternative way to indicate completion of a dot row. The addressing counter is either incremented or decremented, depending on bar direction, to address the next character in the buffer.

Higher density and multiple-pass character text can be processed with this procedure. Direct raster-graphics processing requires that dot-image graphics data in buffer RAM be passed directly to the parallel-to-serial multiplexer and not through a character-set ROM.

Variable dot-density capability can be added to the DGL. This accommodates the applications in which a dot density less than the maximum

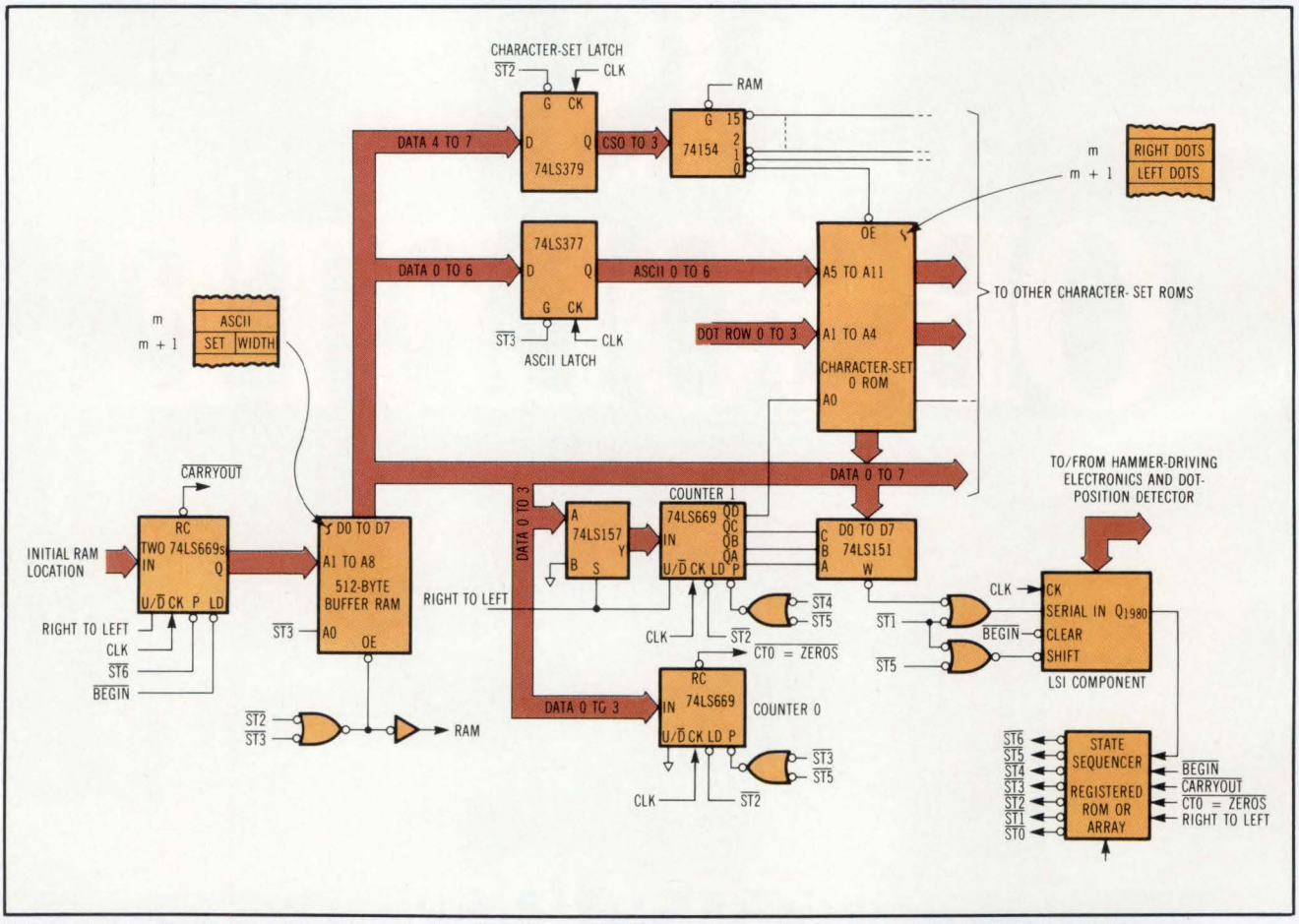

Fig 5 A simplified DGL schematic excludes circuitry needed by the control microprocessor to load the buffer RAM and other support circuitry. However, implementing a full-featured DGL for an impact line printer may require only a handful of common TTL devices.

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	SPECTRA 15*/ SPECTRA 25	SPECTRA 111*/ SPECTRA 121	SPECTRA 12*/ SPECTRA 21
BUS	Q-BUS (Block-mode)	UNIBUS	UNIBUS
Disk Emulation	RM02/05, RM80, RP06 (2 drives)	RM02/05, RM80, RP06 (4 drives)	RK06/07 (4 drives)
Tape Emulation	TS11 (4 drives)	TS11 (4 drives)	TS11, TM11 (4, 8 drives)
Disk Transfer Rate (SMD)	2.0MB/sec	2.0MB/sec	2.0MB/sec
Configurable On-Line	Yes	Yes	No

*Single function disk controller

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SPECTRA LOGIC

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CIRCLE 61

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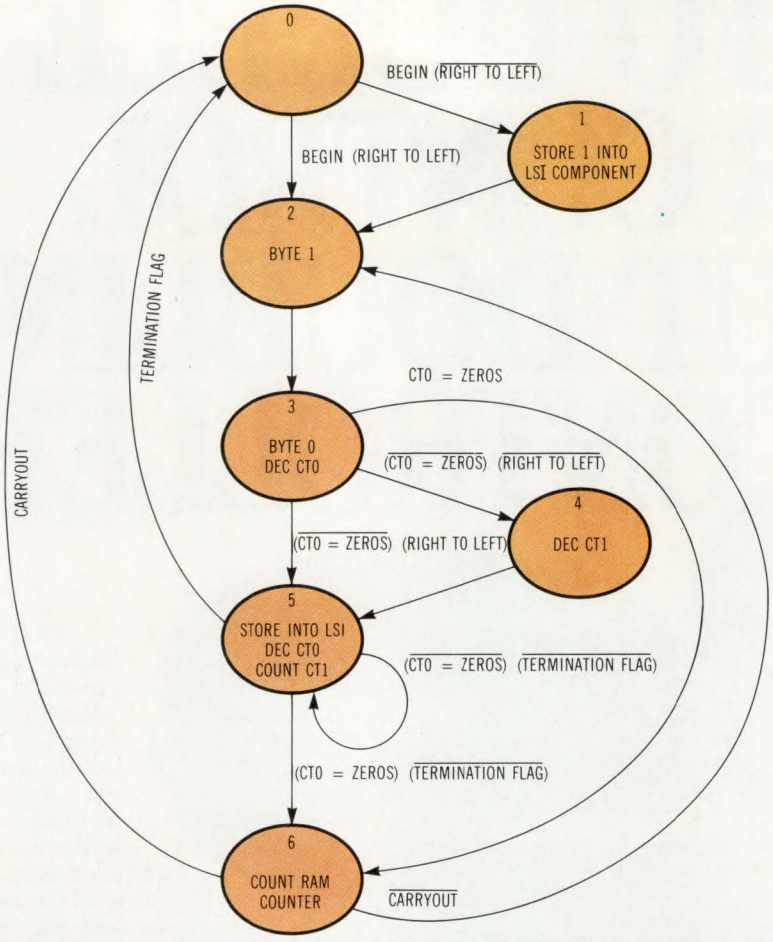

Fig 6 A serial-fill algorithm for the DGL shift/register is relatively straightforward. If directional dependent decisions are eliminated, the algorithm is even simpler. States 1 and 4 are unnecessary if a more complex bidirectional main shift register is available.

established by the design of the main register is desired. But, this requires additional logic and a supplementary counter programmed with a value that can interrupt the fill algorithm of Fig 6 after the programmed of printable dots passed into the main shift register.

Assuming a hammer spacing that is an integral multiple of 0.1 in. permits the printer to operate under program control at any multiple of 10 dot density (eg, 70 dots/in.) on a line-by-line basis. Dummy fill bits, whose number is simply the difference between the programmable value and the number of dots per hammer at maximum density, can be injected periodically to pad the main shift register. For example, if the maximum dot density is 150 dots/in. in a 33-hammer printer, and a 70-dot/in. density is desired, the new programmed counter will be 28 (ie, 28 dots in 0.4 in.).

For every 28 printable dots passed to the main register, 32 dummy bits follow, resynchronizing the printable dots to a 60-bit (0.4-in. when printed) intertap boundary. This padding process ensures that at the completion of main-register filling, the valid printable bits are directly beneath the taps in the main register. The dot-position detector generates the properly timed number of strobes equal to the programmed value in the new counter.

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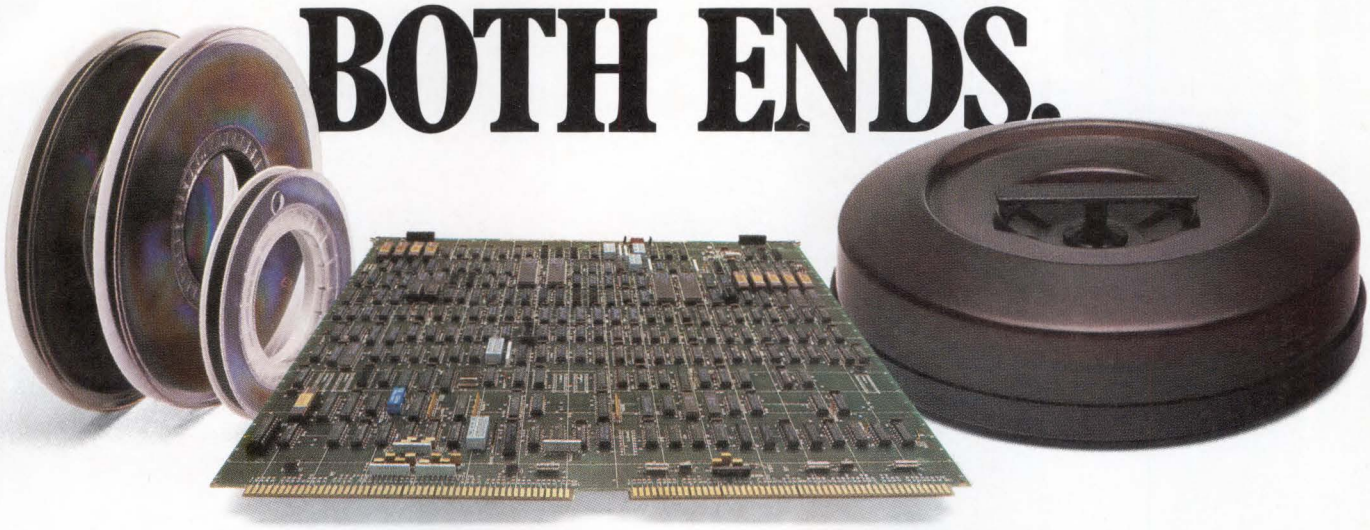

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BUS (Disk)	Burst Multiplexor Channel	Data Channel	Data Channel
Disk Emulation	606X, 6122, 6160, 6161 (4 drives)	606X, 6122, 6160, 6061 (4 drives)	606X (4 drives)
Tape Emulation (Data Channel)	6021	6021	6021
Operating Systems (without OS patches)	RDOS, AOS/VS	RDOS, AOS	RDOS
Disk Transfer Rate (SMD)	2.0MB/sec	2.0MB/sec	2.0MB/sec
Supports FCC Chassis	Yes	Yes	No
*Single function disk controller			

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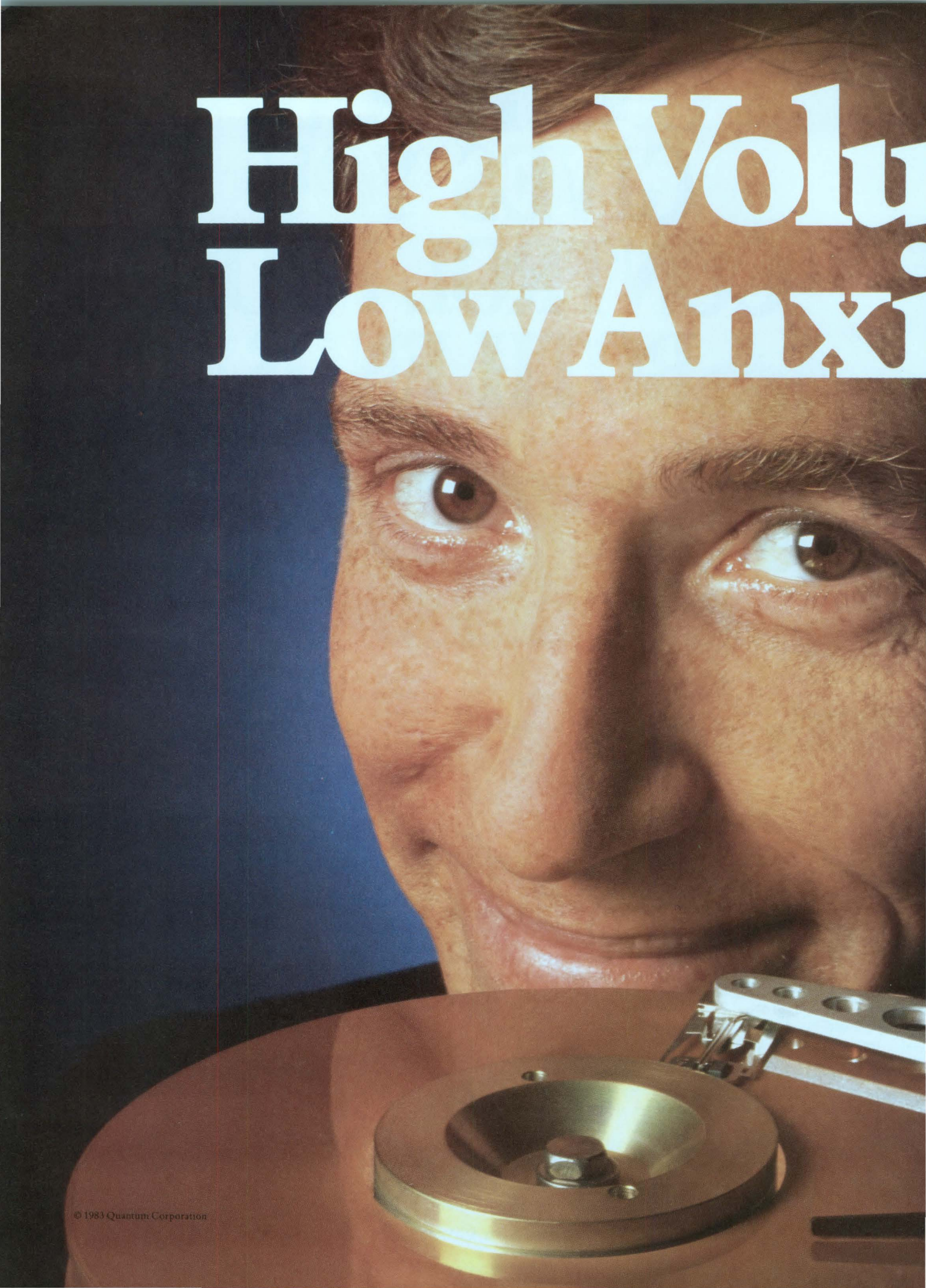
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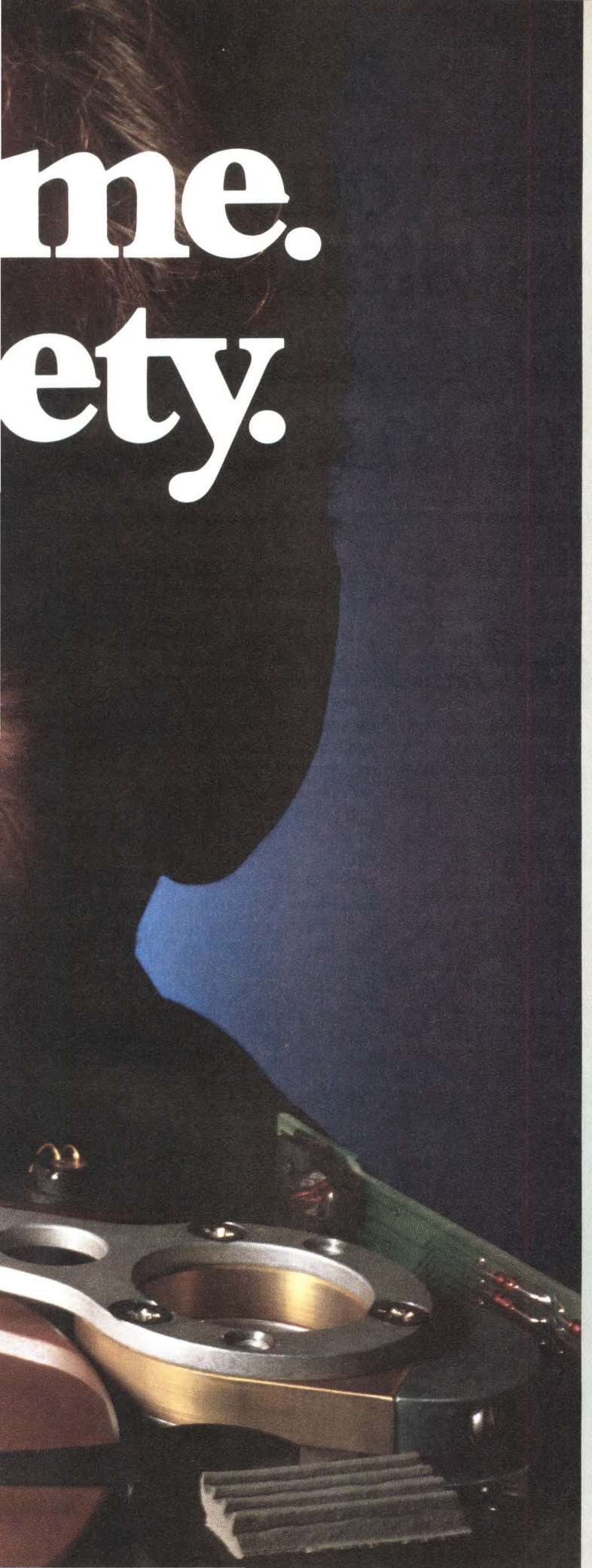

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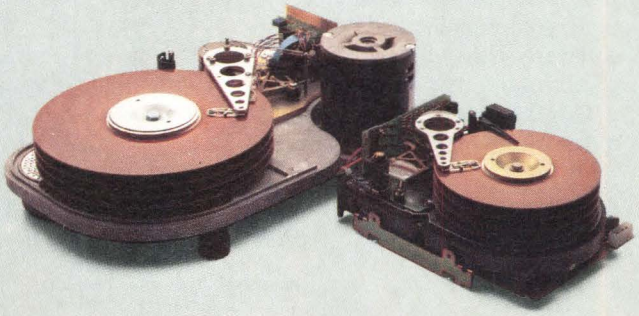

CIRCLE 63

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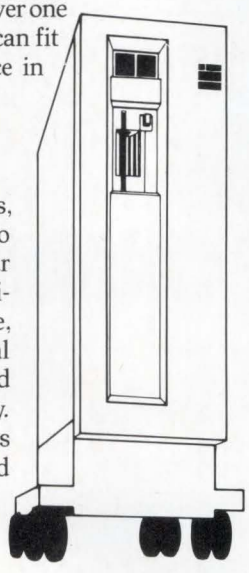

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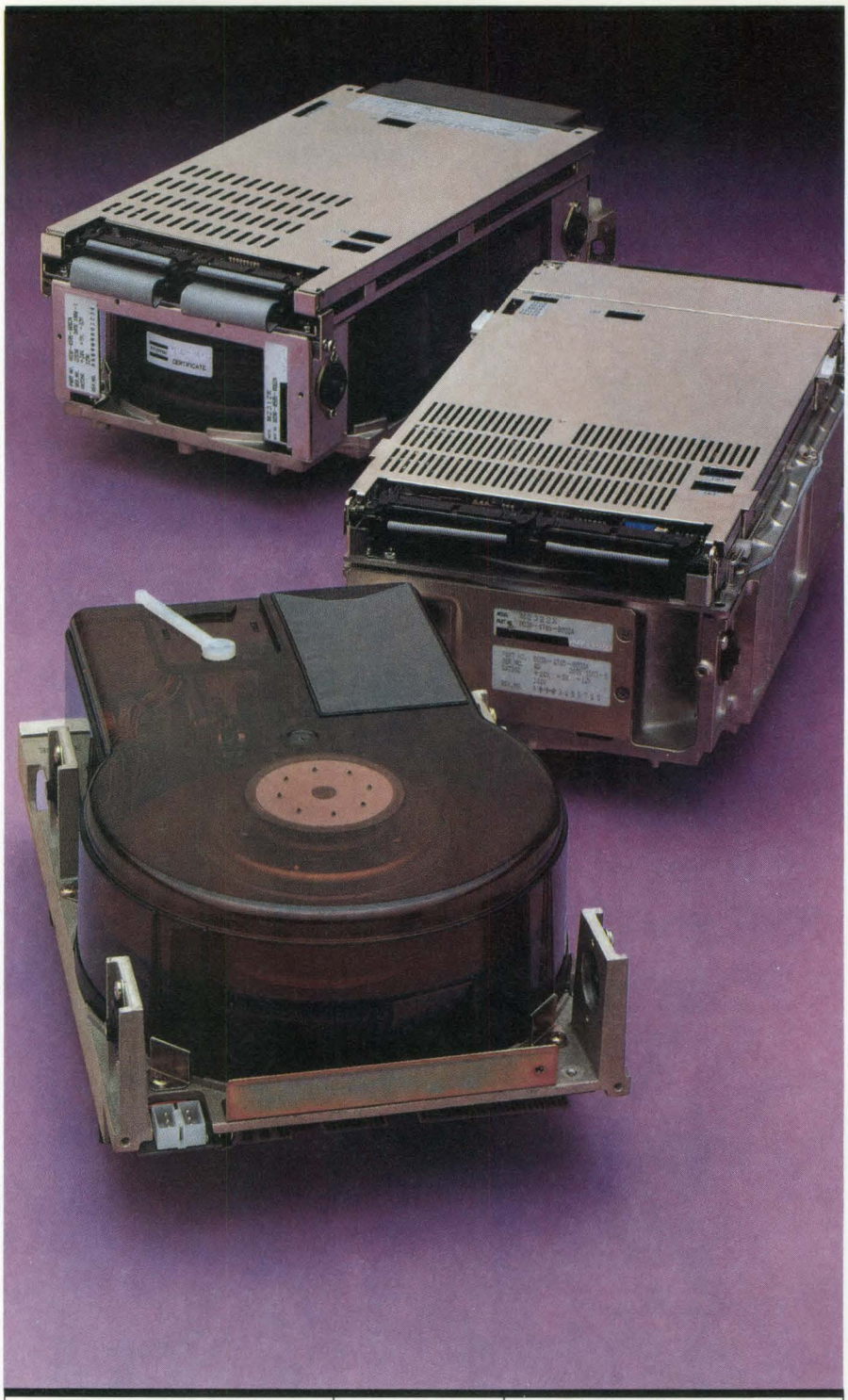

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AVG. POSITIONING TIME (ms)	70	20	20
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INTERFACE	SA4000	SMD	SMD
POSITIONING METHOD	Buffered Stepper	Rotary Voice Coil	Rotary Voice Coil

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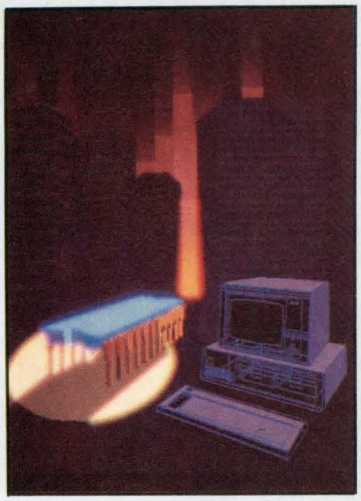

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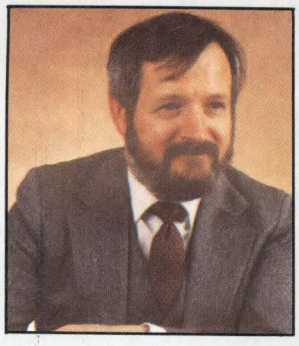


SPECIAL REPORT ON

MICROPROCESSORS/ MICROCOMPUTERS—PART I

The ubiquitous microprocessor has changed the entire electronics industry. In particular, its effect on computer systems has been amazing. The CPUs of mainframes and superminis have, so far, seemed immune to the micro invasion—but the introduction of 32-bit microprocessors is about to change that. Two such microprocessors are already here, and more are scheduled for late '84 and early '85 introductions.

The new generation of microprocessors is heavily influenced by the architectures of existing mainframes and superminis. This is because they are aimed at the same jobs. Thus, the micros support large physical memory, virtual addressing, high level languages, hardware floating point operations, and large operating systems. They offer most of the software advantages of larger computer systems.

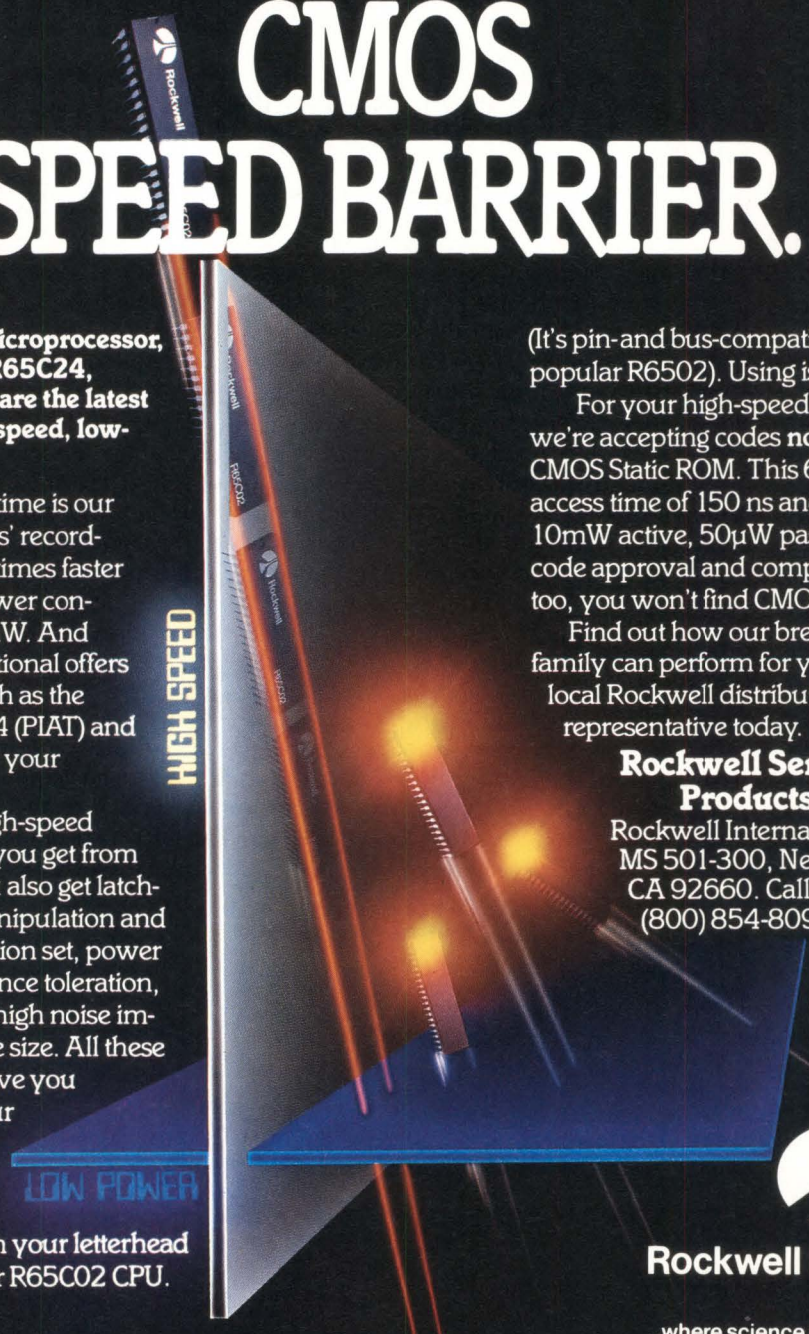
At least one of the new micros can emulate the instruction sets of midrange mainframe computers through its external microprogrammability. Another has a unique architecture that allows multiprocessing. A more common approach is the evolutionary extension of existing 16-bit chip architectures. This evolution includes 32-bit instructions, data types, addressing modes, registers, and data paths. In some instances the process has been made easier because the original 16-bit chips were designed from the outset with 32-bit features or with the extension to 32 bits in mind.

Meanwhile, CMOS has become the technology of choice for this new microprocessor generation. Not only does CMOS offer the lower power consumption that paves the way for the needed chip density, it also permits features unobtainable in NMOS. As proof, many of these unique features are already available in 8- and 16-bit CMOS designs.

Software, of course, is a major issue for micros. The hardware has been designed to support multitasking, to permit easy compiler development, and to allow Unix and other complex operating systems to be easily ported to the new chips.

John Bond
Senior Editor

ROCKWELL SEMICONDUCTOR TECHNOLOGY BREAKS THE CMOS SPEED BARRIER.



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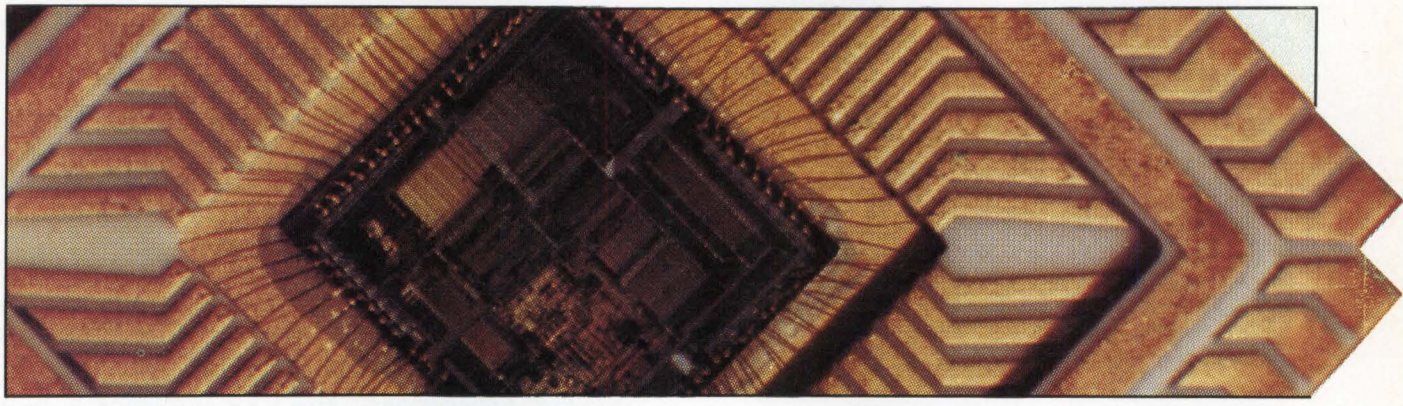
CIRCLE 67

ARCHITECTURAL ADVANCES SPUR 32-BIT MICROS

With promised advances that vary from evolutionary to revolutionary, most of the long-awaited 32-bit microprocessors remain long awaited. Only two are actually available for designers.



by John Bond,
Senior Editor

The stampede of 32-bit microprocessors, promised for 1984, has slowed to a walk. Despite promises in the trade press, most of these 32-bit chips will not be available before the end of the year and it will be 1985 before the industry sees production quantities. The complex architectures and advanced process technology that make such chips possible have also conspired against manufacturers' schedules. Not only must chip designers deal with a new, more complex chip design but, in some instances, a change in process from NMOS to high speed CMOS. Often, the design must proceed concurrently with the design of floating point or other coprocessor chips. The result is an enormous drain on manpower and sophisticated computer aided design tools, leading to missed schedules. Despite that, successful designs have been completed, and at least two of these are currently available on the market. Those not yet ready may be worth waiting for because of their sophisticated architectures or because of software compatibility with existing microprocessor families.

Some promise, some deliver

At present, there are only two 32-bit microprocessors actually available on the market. They are the NS32032 from National Semiconductor Corp (Santa Clara, Calif) and the NCR/32 chip set from NCR Corp (Colorado Springs, Colo). The National chip is the newest member of the NS16000 family of 8-, 16-, and 32-bit data bus chips. Each has an internal 32-bit architecture and implementation, but only the NS32032 has a 32-bit data path to memory.

The NCR micro exhibits one of the most unique features of any chip or chip set either in production or promised. This micro consists of a set of four VLSI chips and two LSI chips, which together form a very powerful CPU. It is unique in its use of

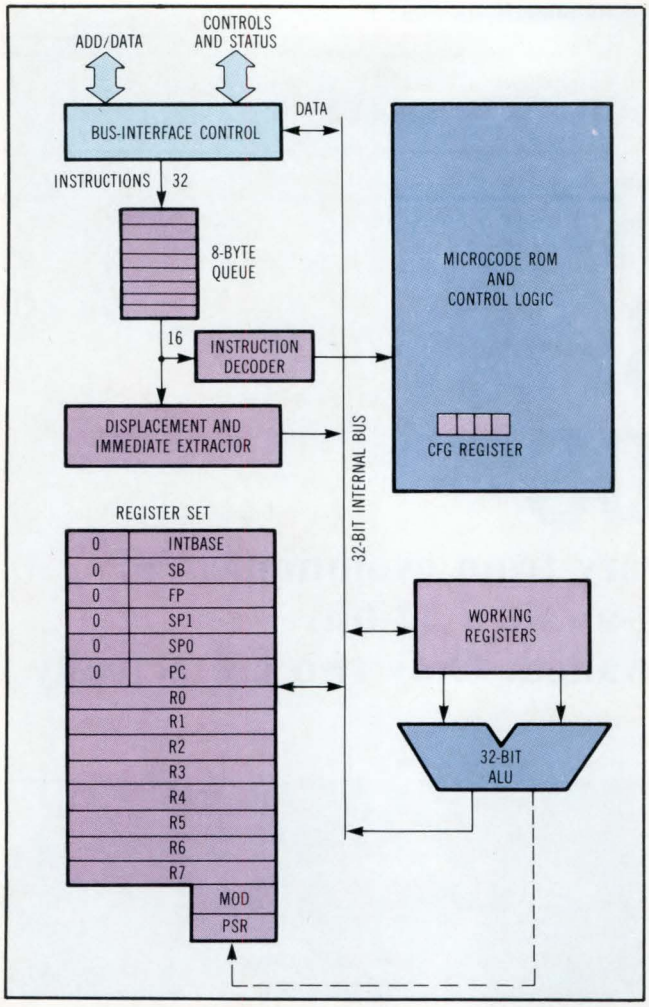


Fig 1 The NS32032 bus interface control unit makes 4-byte instruction transfers into an 8-byte queue. From there, instructions are decoded and passed to the execution unit. An intermediate preprocessor selects and runs microcode for address computation, operand fetching, execution, and result storage.

externally programmable microcode that enables the NCR/32 to emulate other computers.

There are at least two other 32-bit processors in production but they are not commercially available. One of these, Hewlett Packard's (Palo Alto, Calif) Focus, fabricated in 1-μm NMOS, is probably the most advanced processor yet manufactured. It is used in the HP 9000 computer. The other chip is the AT&T Technologies Inc (New York, NY) WE32000, which was formerly the Bellmac-32. This 2.5-μm CMOS chip is used in several AT&T products.

The second generation of that processor, the WE32100, was recently announced. Fabricated in 1.75-μm CMOS, the new chip offers a threefold performance improvement over its predecessor. The chip uses a 64-word instruction cache and a new I/O controller that supports both multiprocessor and coprocessor architectures. Microcode is extensively changed to improve instruction cycle efficiency and take advantage of the separate address and data ports. A companion circuit, the WE32101 memory management unit (MMU) is twice as fast as the original MMU. Both processor and MMU operate at 14 MHz and are packaged in 132-pin packages.

It once seemed likely that AT&T would offer the WE32000 commercially, but now the official line from the company is that they will not. Therefore, 32-bit system designers have only two choices at the present time—National and NCR. The microprogrammable NCR/32 is considered by NCR to compete primarily with bipolar bit-slice processors such as the AMD 2901. And that leaves the NS32032 out there alone as the only mainstream 32-bit microprocessor available in the merchant semiconductor market. It is helpful to compare its architecture and implementation with presently available 16-bit devices that have some 32-bit features.

Instruction sets influenced by VAX

While most 16-bit microprocessors were heavily influenced by PDP-11 architecture, National's NS16000 family was influenced by VAX. Initially conceived as a 32-bit architecture, it was first introduced in a 16-bit external bus version, the NS16032. Shortly thereafter, the NS32032 was brought out. It was essentially the same chip except for a 32-bit bus. Although the NS32032 could be claimed as the first full 32-bit implementation, earlier processors have had numerous 32-bit features. The Motorola 68000, for example, has 32-bit registers even though it is externally a 16-bit chip. Intel's 432 is another example of an innovative 32-bit architecture, although it has a 16-bit data path to memory.

Instruction sets have evolved in a similar way. Again, most 16-bit instructions were influenced by the PDP-11. The Zilog (Campbell, Calif) Z8000 also had some IBM influence with IBM-style string moving instructions. The VAX influence is most apparent in the NS32032 instruction set and addressing modes that provide high level language support. The chip's designers felt that in the future there would be much greater emphasis on high level languages, an approach common to all the new 32-bit designs. In addition to eight general-purpose 32-bit registers in the NS32032, several special-purpose registers support high level language addressing modes (Fig 1). For example, a stack pointer register handles temporary storage of intermediate results, a frame pointer allows access to parameters and local variables on the stack, and a static base pointer is used for global variables. Support of stack-based addressing simplifies implementation of reentrant procedures and is especially useful for block-structured languages such as Pascal.

Addressing is divided into four modes that are standard for microprocessors, and an additional five modes (Fig 2) that are used for high level languages. Addressing is uniform rather than segmented. All registers, and therefore all addressing modes, use the

same style of addressing. The advantage to this is that a compiler writer does not need a different type of code generation for static variables, local variables, or stack variables.

A major objective of the NS32032 design is to achieve good code using mediocre compilers. Since compilers take time to mature, programmers must often work with immature compilers, which generate mediocre code. To demonstrate this advantage, National engineers performed high level language benchmarks, using a new version of the company's own Pascal compiler. This was benchmarked against a 68000, running a Motorola (Phoenix, Ariz) Pascal that had been refined for years. The National Pascal ran about 47 percent faster. This occurred, not just because the National chip is better, but because it produces superior code from National's own, admittedly less mature, compiler.

National's 32-bit chip performs floating point operations in a slave processor (NS16081) that differs slightly from a coprocessor. The CPU stops when it sends an instruction (and possibly data) to the floating point processor (FPP) that performs the instruction. The FPP then sends back a response (and data, if required) and the CPU continues processing. The Intel 8087 and 80287 coprocessors work only with their appropriate Intel processors because, unlike the NS16081, they are more closely coupled to their processor chips. The National FPP will work with other processors and, in fact, it is used in a number of 68000 applications. Because Intel has matched the pipelines of processors and coprocessors it makes for an efficient combination. But, it prevents the coprocessor from being effectively used with non-Intel processors. Using a slave processor also makes it easier to bring that function onchip when process advances permit it.

The NS16082 MMU is also a slave processor. The entire mapping of the logical address space is described by tables in memory and the MMU has automatic, direct access to those tables. The MMU maintains an internal cache of the 32 most recent translations. It updates the cache automatically when it gets a request for a page that is not in cache. It simply holds the processor, accesses the table in memory, gets the new translation, and continues. The whole process takes 2 μs.

Because the NS16082 MMU is designed for demand-paged virtual memory and the NS16081 is available to support IEEE standard floating point operations, an entire system can reside on one board. This is an important consideration when designing low cost systems. The NS16000 series does not have onchip cache but does provide an instruction prefetch. Because the instruction set is designed with variable instruction size, however, instruction alignment is necessary. This does not slow the system because an instruction is always ready for execution in the 8-byte

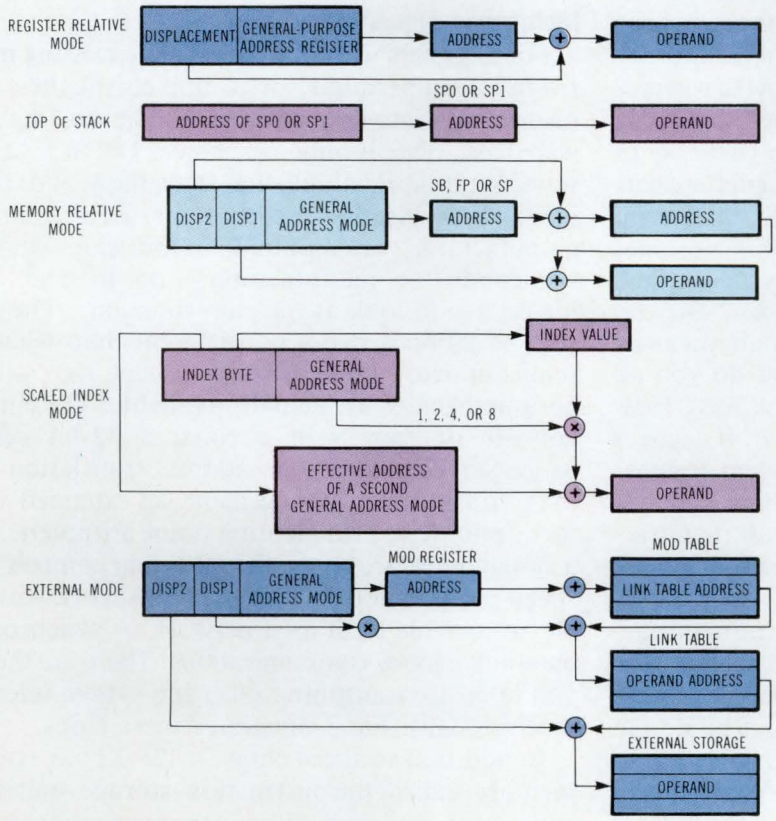


Fig 2 Along with standard addressing modes, the NS32032 and other NS16000 family members offer five addressing modes to support high level languages. These are memory mode (register relative), top of stack, memory relative mode, and scaled index and external modes. External mode and top of stack are unique to the NS16000 family. External address mode allows modules to be relocated without linkage editing. Top of stack addressing permits the currently selected stack pointer (SP0 or SP1) to specify operand selection. It allow manipulation of an operand on the stack by all instructions, unlike other microprocessors where top of stack addressing is limited to a small number of instructions.

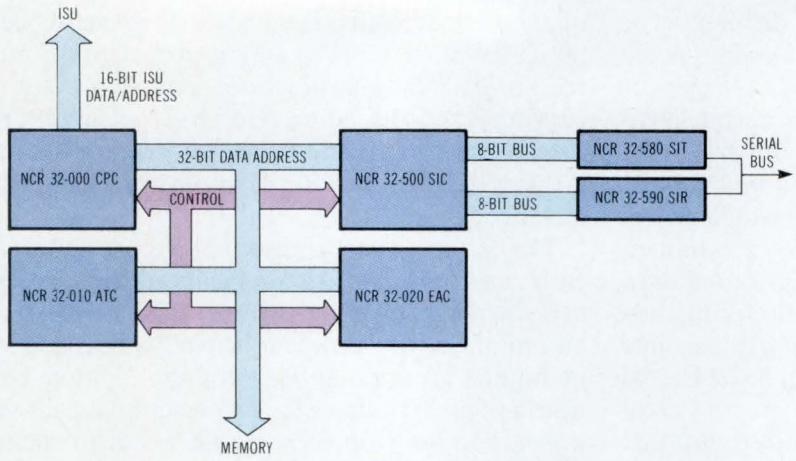


Fig 3 The NCR/32 is composed of four VLSI chips: a central processor chip (CPC); address translation chip (ATC), extended arithmetic chip (EAC) and a system interface controller (SIC). The system interface transmitter (SIT) and receiver (SIE) provide high speed conversions between the byte-wide SIC and bit-serial communication channels.

prefetch queue that is loaded with aligned transfers. The CPU fetches 4 bytes at a time from the instruction stream. Whenever the bus is free, it reads another instruction.

On the other end of that queue is a unit that decodes instructions while functioning as the interface between the execution unit and the instruction stream. In most cases, the instruction is already decoded and ready to execute in what is essentially a three-stage instruction pipeline. One stage performs the fetch and decode while the next stage executes.

Although the NS32032 does not have a data cache, a future version of the chip will use a bus protocol designed to support a high speed external cache. National elected this approach because the size cache that can be put on a chip with today's technology is not very large (typically, about 256 bytes whereas an optimal computer system cache would probably be about 2 Kwords). Also, an onchip cache locks the system designer into the chip designer's cache policy. If the cache is external, however, the system designer can choose a cache policy that provides answers to several questions: Do you write through the cache, continually updating memory? Do you save changes and only write back to main memory with an update when necessary? What do you do about multiple processors on the same bus? How is DMA handled? According to National, if cache is on the chip, it is difficult to give the system designer the flexibility needed to configure a high end system. Nonetheless, there are several chip manufacturers who disagree with National's position and are building caches into their chips.

National beat the other semiconductor manufacturers to market with a 32-bit chip because the company was very conservative from a process standpoint. The family was brought out in 3.5-μm NMOS, which is not National's most advanced technology. The company has a 2-μm CMOS process in gate arrays and will eventually migrate the NS16000 family into that technology or some other advanced process. But for this iteration, the designers avoided complications by bringing out microprocessors in a technology that they fully understood.

The chip is currently available in a 6-MHz version, but a 10-MHz chip will be in production in the third quarter of '84. When the die is shrunk, the whole family will be upgraded to a 15-MHz clock. So, while the present NS32032 uses current technology, competitors have had to slip introductions because of more complex architectures or processes they have pursued. National, however, expects to bring out advanced versions of the chip by the time more advanced, competing chips are in production.

Mainframe emulator

For designers who want to emulate existing mainframes or superminis, or to implement their own instruction set to take advantage of an existing software base, there is only one choice. The NCR/32 chip set allows that flexibility and is available. For those inclined to dismiss the chip set as a computer manufacturer's attempt to do in four chips what the semiconductor manufacturer's do in one, it is instructive to look at the chip functions. The division of labor is really no different than what the semiconductor houses offer—except that all the peripheral chips are actually available. The chip set consists of four VLSI circuits: a 32-bit central processor chip (CPC), an address translation chip (ATC) for memory management, an extended arithmetic chip (EAC) for floating point arithmetic, and a system interface controller (SIC) that controls slow speed peripheral I/O. Two LSI chips work with the SIC to provide local area network or synchronous data-link control communications. These are the system interface transmitter (SIT) and system interface receiver (SIR). Fig 3 illustrates these chips.

In addition to these chips, a 128-Kbyte external memory called the instruction storage unit (ISU) contains the external microinstruction program that tailors the system to the user's needs. It is accessed

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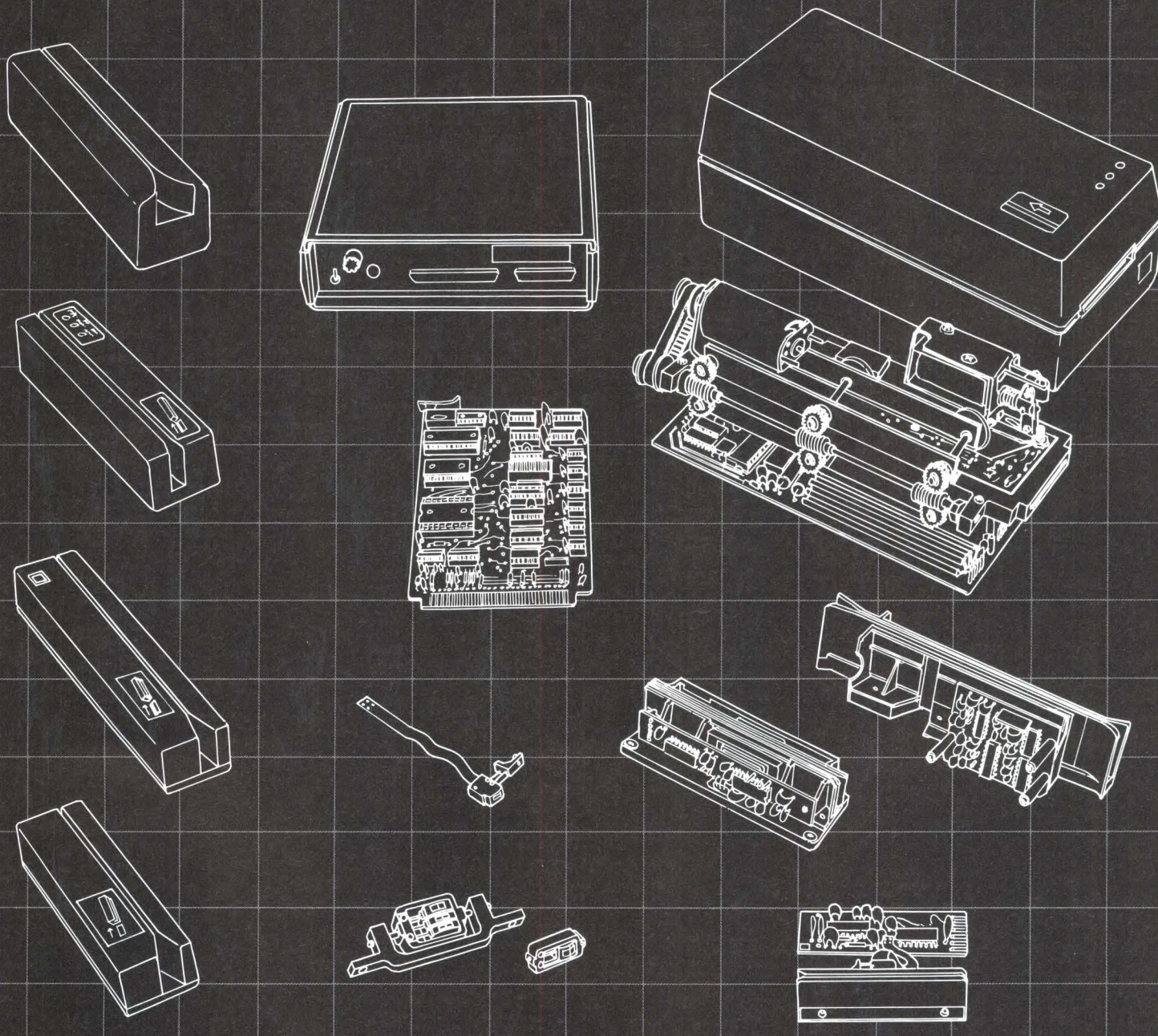

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by the CPC over the 16-bit multiplexed ISU bus. The main bus, however, for interchip as well as offchip system communication is the processor memory bus. This is a 32-bit multiplexed data/address bus with associated control lines capable of transfer rates in excess of 50 Mbytes/s.

The CPC contains a set of 179 primitive instructions in onchip ROM. These microinstructions are designed to execute in one clock cycle of 150 ns. This is similar to the single-cycle instruction execution found in Reduced Instruction Set Computer (RISC) applications. It is responsible for the speed advantage of the chip's native-mode instructions.

To emulate existing mainframes or superminis, there is only one choice.

In emulation mode, a virtual machine's instructions can be emulated to permit the use of existing software. Since the external ISU must be used for this, emulation mode runs more slowly than native mode. The simplified microinstructions, resident on the CPC, free up silicon that would normally be needed for control functions. This is put to good use to provide a RISC-like, register-rich architecture.

A three-stage instruction pipeline (fetch, interpret, and execute) and 13.3-MHz clock add to the performance of the chip set. But, program execution speed varies according to whether the chip is used in native or emulation mode or what type or processor is emulated. For example, setup registers for virtual machine emulation are tailored for the IBM 370 instruction set. Also, the EAC supports IBM-compatible floating point. So it is not surprising that the NCR/32 can run IBM MVS at about the same speed as an IBM 4331. When emulating Digital Equipment Corp's (Maynard, Mass) VMS, however, it runs three to five times slower than a VAX 11/780. By comparison, when each runs the same task in its own native code, the NCR/32 will run two to three times faster than a VAX. NCR uses the chip set in the NCR 9300 system and Honeywell has announced plans to use it in a new small-to-medium mainframe family.

Not available yet

The big three of microprocessors—Intel (Santa Clara, Calif), Motorola, and Zilog—have not yet introduced their 32-bit offerings to the world. Of these, the Motorola 68020 is probably the closest to production. Originally scheduled for the end of the first quarter 1984, introduction has slipped to the summer of 1984 and some industry sources indicate the chip may not appear until nearly the end of the year. Since Motorola's long awaited floating point coprocessor will not be produced until after the 68020, users are in for a still longer wait for that part. Motorola has recently taken a closed-mouth approach to officially releasing information about the 68020 to the press. However, Motorola personnel have presented papers at conferences that detail many of the features of the new microprocessor.

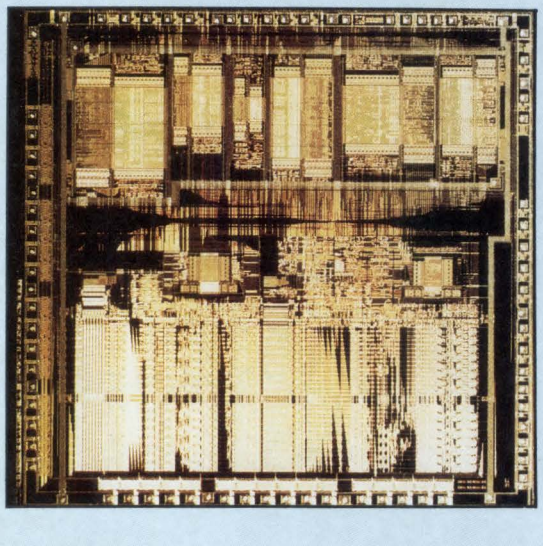
Intel has said even less about its entry, the iAPX 386, except that it is an extension of the 8086/286 family architecture. Since the introduction data is in the first half of 1985, Intel spokesmen obviously do not want to discuss a design that may still be somewhat fluid. However, a clear picture of the company's direction may be obtained by looking at the existing family and extrapolating that to the 32-bit world.

Zilog's position regarding the Z80,000 has been much more open. The product has been announced in considerable detail, including trade magazine articles. Unfortunately, the project has not kept pace with promotion and has been dogged with delays. Zilog now estimates the sampling data as mid-February 1985, some six months after the company sees first silicon on the part.

A step beyond

The 68020 uses the basic 68000 instruction set but adds new instructions and addressing modes. Six instructions are extended to larger data types. Sixteen new instructions are added for additional data types and seven more new instructions provide support for coprocessors.

Since the 68020 will be the first 68000 family member to possess a full 32-bit ALU, several



The WE32000 32-bit microprocessor has been available within AT&T for some time. A more advanced version, the WE32100, was recently introduced. However, there are no plans to make either chip available outside AT&T.

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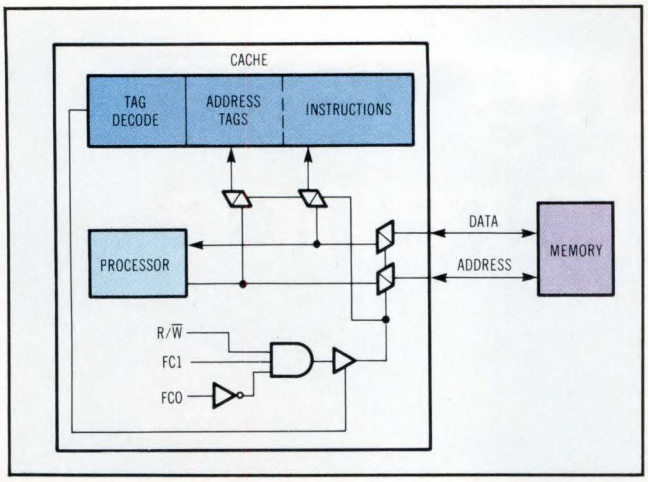


Fig 4 Because of the pipelined internal architecture of the Motorola MC68020, the ALU can execute instructions faster than they can be fetched from external memory. To permit the chip to run at full speed, an instruction cache is built into the chip. This cache is used only for instructions, not for data.

instructions had to be enhanced to support 32- and 64-bit data. Other new instructions provide aid for multiprocessing and compiler writing. Additional addressing modes include scaled indexing and memory indirection.

Memory management will be supported by an instruction continuation mechanism as it is in the 68010. Demand-paged virtual memory requires this feature because the CPU must be able to suspend an instruction at any point and continue it later. The 68020 extends that ability and adds new registers and instructions to support a virtual memory environment.

A coprocessor interface to support the MC68881 floating point coprocessor is an important addition, or at least it will be when that chip becomes available. Adding to the speed of the chip, the pipelined architecture can execute instructions faster than they can be fetched from offchip memory. To prevent slower, external memory from limiting the speed of the device, an onchip instruction cache was included to allow faster instruction fetches (Fig 4). For programs that fit within the cache, the 68020 will run six times faster than the 68000. Most programs will actually run four times faster on the 68020. This chip will be fabricated in a combination CMOS/NMOS process that offers high speed and low power consumption.

Evolutionary developments

Given the current development schedules in the industry, Intel could be the last one out with a 32-bit microprocessor. But don't count on it—Intel may be the only company with a realistic schedule. In any event, there should be no great surprises. The iAPX 386 is an evolutionary extension of the basic 86 architecture. It is bit compatible and allows migration of existing software to a 32-bit environment (Fig 5).

Like the iAPX 286, the 386 will have a four-level protection mechanism implemented in the microcode. Software can be assigned to any of four priority levels and access controlled between levels. The 386 will be fundamentally the same in other ways, as well. The primary difference will be that the 386 will have 32 bit addresses, registers, and data paths. Moreover, the 386 will be implemented in CMOS, unlike the NMOS 286.

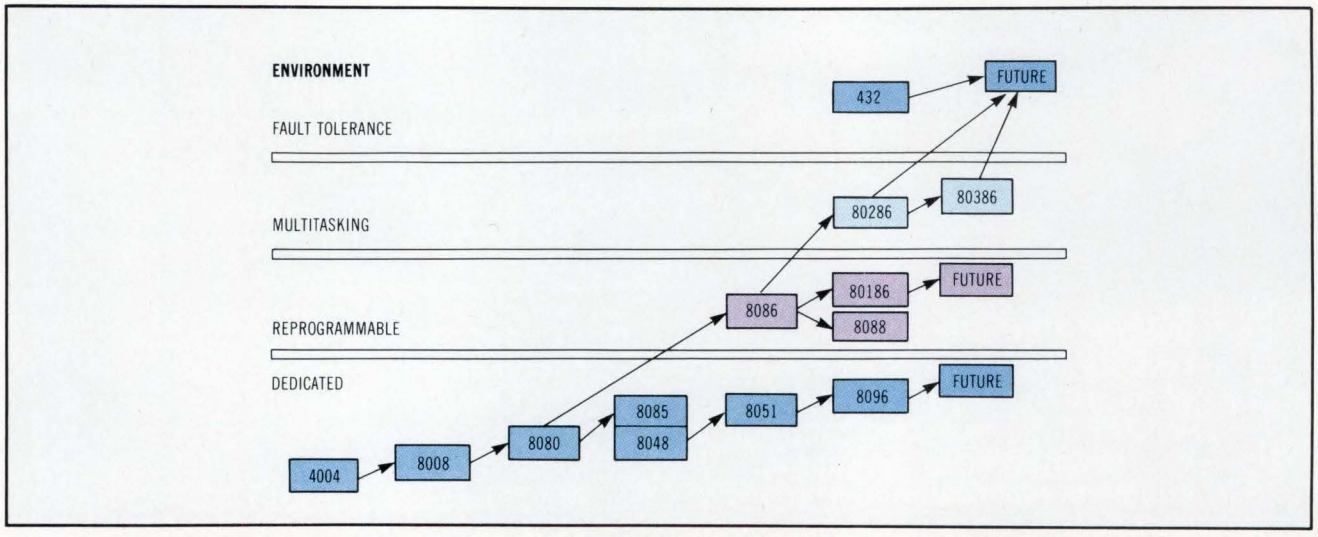
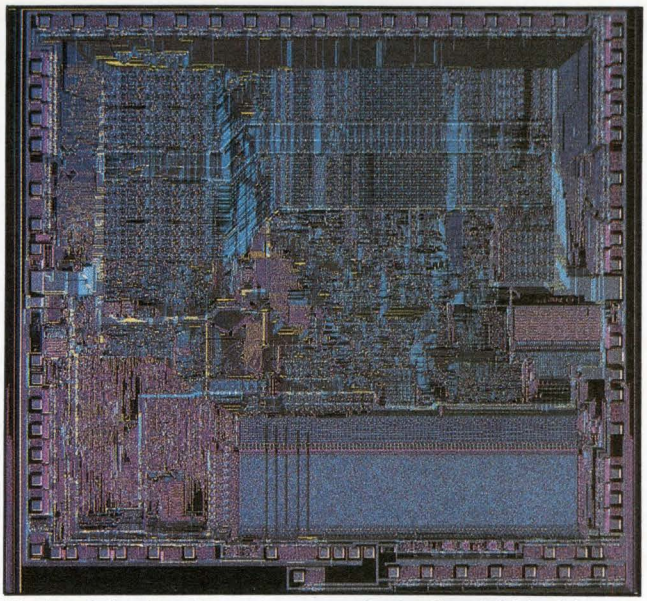


Fig 5 Intel's approach to microprocessor family evolution is best understood in terms of the environment for which each is intended. The basic 8-bit processors (and one 4-bit) are aimed at dedicated applications such as controllers. The reprogrammable processors are aimed at the first level of computer applications. Starting with the 8086, the basic CPU evolved into the 8-bit external, 16-bit internal 8088 and 80186. The latter brought many of the support functions onchip to lower system costs. The next level is capable of multitasking. It includes higher performance processors like the 16-bit 80286 and the 32-bit 80386. These CPU's can handle extensive physical and virtual memory. They are designed for high level language support. Finally, for fault tolerant processing, the 432 is unrelated to the rest of the 86 family but some, as yet unspecified, future chip may pull it all together.



National Semiconductor's NS32032 is the first 32-bit chip available from a mainline semiconductor supplier. Like other members of the NS16000 family of microprocessors, it is organized to optimize support for high level language.

A major consideration at Intel is software compatibility across a family of products. Intel has made the entire 86 family instruction set compatible with extensions, as appropriate. For example, the 286 has (and the 386 will have) extensions for a memory management protection mechanism similar to the Motorola 68010. But according to Intel, the 386 will exhibit tighter coding and a more byte-efficient instruction set than the 68010. Memory space and performance are improved because the fewer bytes required for an application reduce bandwidth requirements. Features of the family instruction set include coprocessor escape mechanism (to support coprocessors) and string instruction (operating string primitives) to develop instruction loops for higher level instructions (almost like macros with very few bytes). As an example, the move operation is a single byte. A contiguous move operation that transfers an entire block of memory from one space to another takes only 2 bytes. Therefore, something that would require substantial looping capabilities in a traditional instruction set can now be done in 2 bytes.

The 8086 has a 1-Mbyte address space. The 286 provides a 16-Mbyte physical address space and 32-Gbyte virtual address space (each of 32 users have 1 Gbyte). The 386 will support even larger physical and virtual address spaces. Both support virtual memory and swapping.

In the 8086, the user views address space as a set of segments. These can be linked to support large data structures or treated individually. The 286 and 386 retain the same addressability but treat it as virtual memory. Consequently, total available address space grows from 1 Mbyte to the gigabyte range.

It is consistent from the programmer's point of view because it treats addresses alike whether they are physical or virtual. So, software is portable from a low cost processor such as the 8088 up to the higher cost 286 and 386.

To programmers familiar with PDP-11s, memory segmentation, as implemented on the Intel chip may be an unfamiliar concept. But those used to programming IBM or Burroughs equipment will find the concept not only familiar but will appreciate the benefits it confers. Among software designers, segmentation is much more readily understood and appreciated. Visi Corp, for example, has used segmentation to implement VisiOn software packages. Windows are controlled on a segment basis.

The memory management chips from Zilog and Motorola also use a segmented concept, but their processors have a linear address space. Intel chose to build segmentation into the processor chip as a fundamental concept. The Intel chips have fewer registers than Motorola's, however, the register set in the family is more oriented toward, and optimized for, high level languages. Because these registers are useful for high level languages, they allow for compactness of instruction set and relative efficiency in register utilization.

Addressing, register sets, and instruction sets are attributes that remain consistent from member to member of the family including the 386. This is because they are the attributes visible to the programmer. But, there will be new instructions for vectors and bit fields and to support 32-bit data types.

The family is basically organized with a 16-bit ALU. The 386 takes that to 32 bits. The 386 is also very fast, with a high degree of pipelining. Fetch, queue, decode, and address calculations are all done in parallel. Thus, at any point there are three instructions undergoing execution. (The 8086 used prefetching as a first step toward some degree of parallelism.) Intel's approach with the 286 and 386 is that virtual addressability is totally independent of the I/O pins. By bringing it onchip, Intel has allowed virtual address space to be totally independent of the number of physical pins.

The 386, along with other family members, offers onchip memory management. It also has an onchip instruction queue but not a true cache for both instructions and data. The new instructions, a bus that supports fault tolerance, and a much faster floating point coprocessor round out the evolutionary advances in the product line.

A revolution in silicon

Though well publicized and billed as a "mainframe on a chip," the Zilog Z80,000 development program has been delayed and the company has not yet produced first silicon. This may be due to the complexity of the design, since the performance claimed for the chip is extraordinary. Zilog is attempting nothing less than to leapfrog the entire industry and produce the highest performance 32-bit microprocessor (see the Table).

Comparison of 32-bit Microprocessor Features

Features	Zilog Z80,000	Motorola 68020	National NS32032	Intel 80386
MMU onchip	yes	no	no	yes
Instruction cache onchip	yes	yes	no	yes
Data cache onchip	yes	no	no	no
Pipeline	yes	no	no	yes
Burst memory transfer	yes	no	no	no
Bus scaling	yes	no	no	no
Addressing (linear/segmented)	both	linear only	linear only	segmented only
Orthogonality	no	no	yes	no
Floating point support	yes	yes	yes	yes
General-purpose registers	16	16	8	6-segment 8-data

Source: Zilog, Inc

It is all part of a plan to orient the company's product lines toward two distinct function areas—control and computation. Zilog realized that although the Z80 architecture was well suited for control applications, computation-oriented tasks required a different architecture, a different register model, and a different instruction set. So, the company developed a new 16/32-bit computational family.

Since chip densities at the time would not allow the implementation of a 32-bit processor, the 16-bit Z8000 was first built as a downward-compatible member of the Z80,000 family. Thus, the Z80,000 has its foundation in the Z8000, although the 16-bit chip was hardwired and the Z80,000 will be microcoded.

Zilog has chosen to implement the Z80,000 in NMOS. The 2-μm design-rule process used permits four different transistor types. This allows the designer to optimize the speed and power needs of each individual logic element. High value polysilicon resistors permit large, fast onchip static RAMs for cache memory. Multiple interconnect levels allow higher packing density of logic elements. The power dissipation of this NMOS process approaches that of CMOS.

Although initial versions of the chip will run at 10 MHz, the process will enable speeds up to 25 MHz. A Z80,000 at 25 MHz will have a peak instruction execution rate of 12.5 million instructions per second (MIPS), and a sustained rate of 6.75 MIPS. The sustained instruction rate takes into account 32-bit instructions, the full instruction set, cache misses, and pipeline interlocks, making the Z80,000 almost four times as fast as the VAX 11/780 . Since the chip does not yet exist, such performance estimates are based on Zilog's simulations and may not reflect the real-world characteristics of the chip.

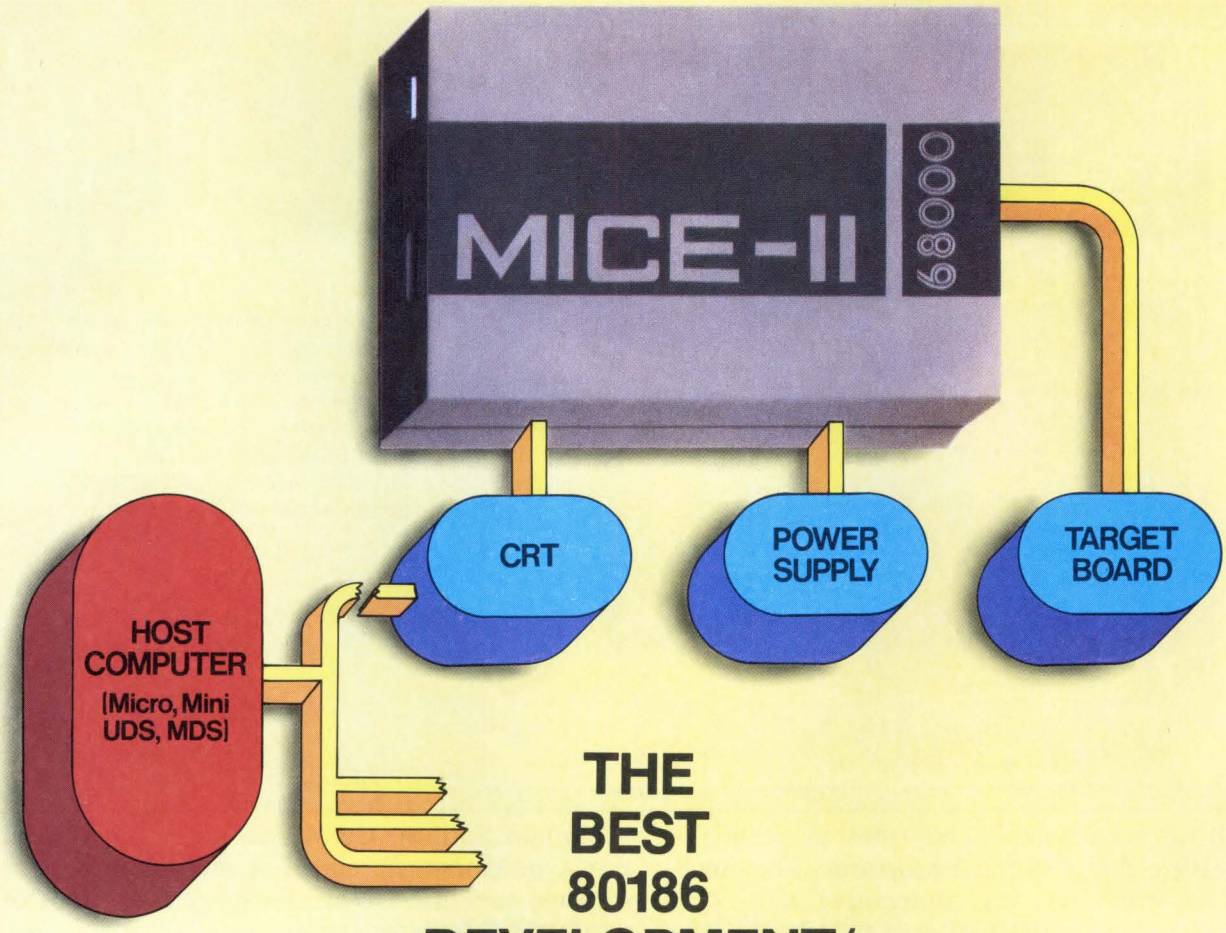
To facilitate execution of complex 32-bit instructions, particularly those requring extensive operand address artithmetic, the chip uses a multistage instruction pipeline with both an execution stage ALU and an address calculation ALU. The Z80,000 breaks instructions into six phases: fetch, decode, operand address calculation, operand fetch, execution, and operand store. This pipeline improves execution speed significantly. To keep the pipeline full, the Z80,000 has a 256-byte fully associative cache memory. The cache always contains the most recently used instructions and data. It may contain instructions only, data only, instructions and data together, or be used as a fixed memory as needed by the user.

To maximize bus bandwidth without requiring faster memories, the Z80,000 uses a burst mode that permits memory transactions to use the nibble mode or page mode feature of some RAMs. This mode allows multiple data transactions to follow an address transaction without intervening address transactions. Thus, memory bus bandwidth is effectively doubled.

The onchip demand-paged memory management unit maps the pages of logical memory into the frames of physical memory. To implement this scheme, a translation look-aside buffer (TLB) is incorporated onto the chip. This buffer contains the 16 most recent maps between logical and physical memory. The Z80,000 automatically checks the TLB for the proper map. If there is a match, the corresponding physical frame address is read and a memory access made. If there is no match, the Z80,000 automatically accesses translation tables in main memory to obtain the proper map. This new map is then loaded into the TLB in place of the oldest entry. As in the case of the cache, the least recently used algorithm is used to ensure that the TLB always contains the most recent entries.

Other voices, other chips

For all the talk of VAX-like 32-bit architecture heard from the micro makers, there can be no doubt that the most "VAX-like" chips were those described in three DEC papers given at the International Solid State Circuits Conference (ISSCC) earlier this year. The presentations covered a four-chip VLSI VAX CPU implementation with 1,220,550 transistors, an interface chip for a new 32-bit bus with



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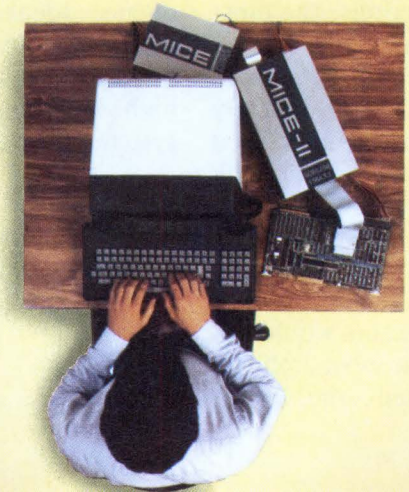

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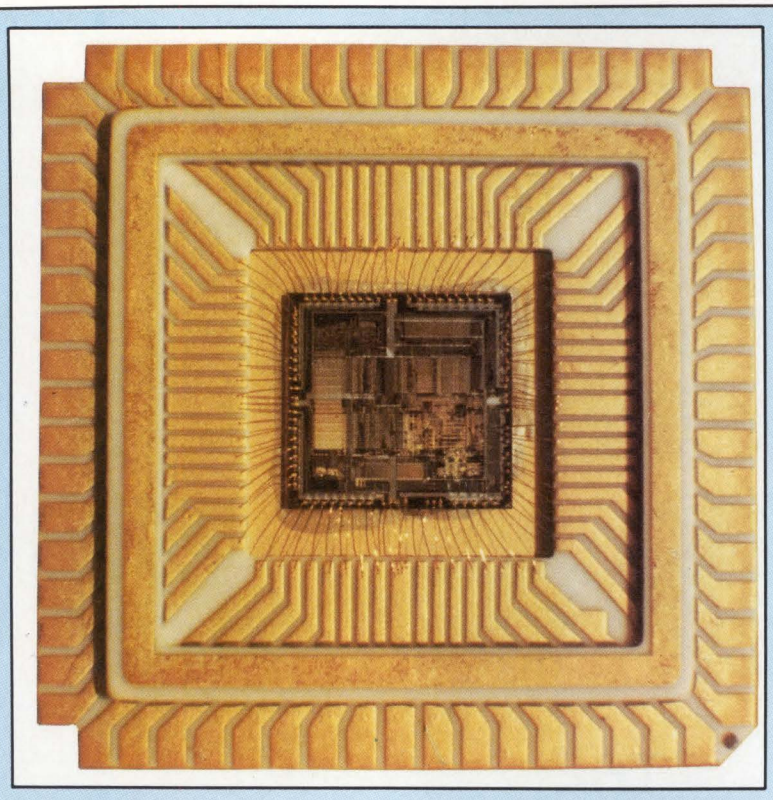

The NCR/32 VLSI processor family contains the only micros designed to emulate existing midrange mainframes. Shown here is the NCR 32-000 central processor chip, the heart of the chip set. This externally microprogammable VLSI system is currently available.

13.2 Mbytes/s bandwidth, and—most interesting of all—a single-chip VAX microprocessor. The single-chip VAX could be very competitive with other 32-bit processors on the market, if DEC should offer it for sale. The company's present position is that a decision has not been made whether to sell the chip (or the chip set). Both will undoubtedly appear in future VAXes, but whether the single-chip VAX will be offered generally shall be decided on the basis of yields and marketing considerations. However, since DEC does offer LSI-11 processor chips to their OEM customers, it is likely that VAX chips will eventually be offered as well.

The firm's 20-MHz device places 125,000 transistors on an 8.5- x 8-mm die. It is a full 32-bit chip that executes the instruction set and demand-paged virtual memory management of the VAX-11/780. Implemented in NMOS, the chip, which is packaged in a 68-pin chip carrier, has a worst-case power dissipation of 3 W. The design features overlapped instruction prefetching and parallel instruction decoding. Of the VAX's 304 instructions, the most commonly used 175 instructions are microcoded onchip, 70 are in a separate FPP chip, 27 are in microcode-assisted macrocode, and 32 are entirely in macrocode. Dynamic RAMs can be interfaced without wait states and the chip has an internal clock generator. Physical address space is 1 Gbyte and virtual memory is 4 Gbytes. The chip contains 16 general registers, 20 microcode scratch registers, 32-bit ALU, and a barrel shifter.

A discussion of 32-bit microprocessors would not be complete without a mention of the most architecturally unique chip yet announced—the Inmos (Colorado Springs, Colo) transputer. This 32-bit RISC-type computer, aimed at multiple processor systems, uses the Occam language (see series of articles in *Computer Design*, Nov '83 to Jan '84). It includes processor, memory, and communications on the same 250,000 transistor CMOS chip. Like so many of its 32-bit cousins, it is not expected before 1985. In the meantime, another article in this special report section (see pp 143, "Thirty-two Bit Micro Supports Multiprocessing" by Pete Wilson) provides details about this unusual and controversial chip architecture.

Two of the new 32-bit microprocessors are already here. By mid-1985, or sooner, more will be available to help change the way we build computer systems. The system designer need only look at computers in current use to foresee the 32-bit microprocessor future. This is because architecture, instruction sets, and addressing modes have less to do with 8, 16, or 32 bits than they do with the passage of time and the state-of-the-art in computer science. Ideas that appear first in mainframes and superminis, eventually show up in silicon. This generation of 32-bit chips will be oriented toward high level languages—much like the computer systems in use for some time now.

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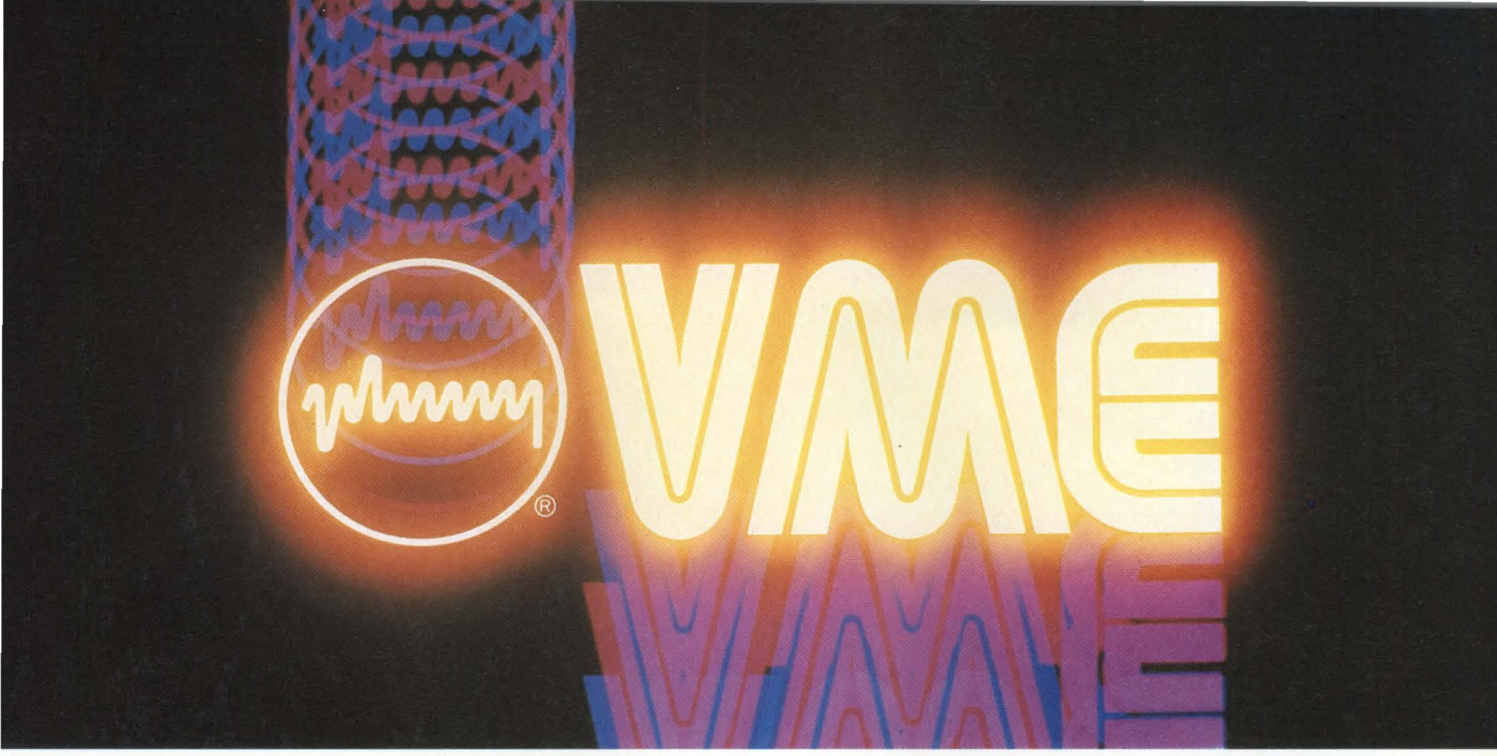

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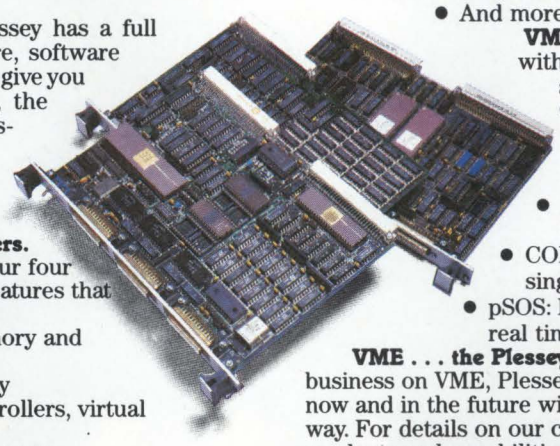

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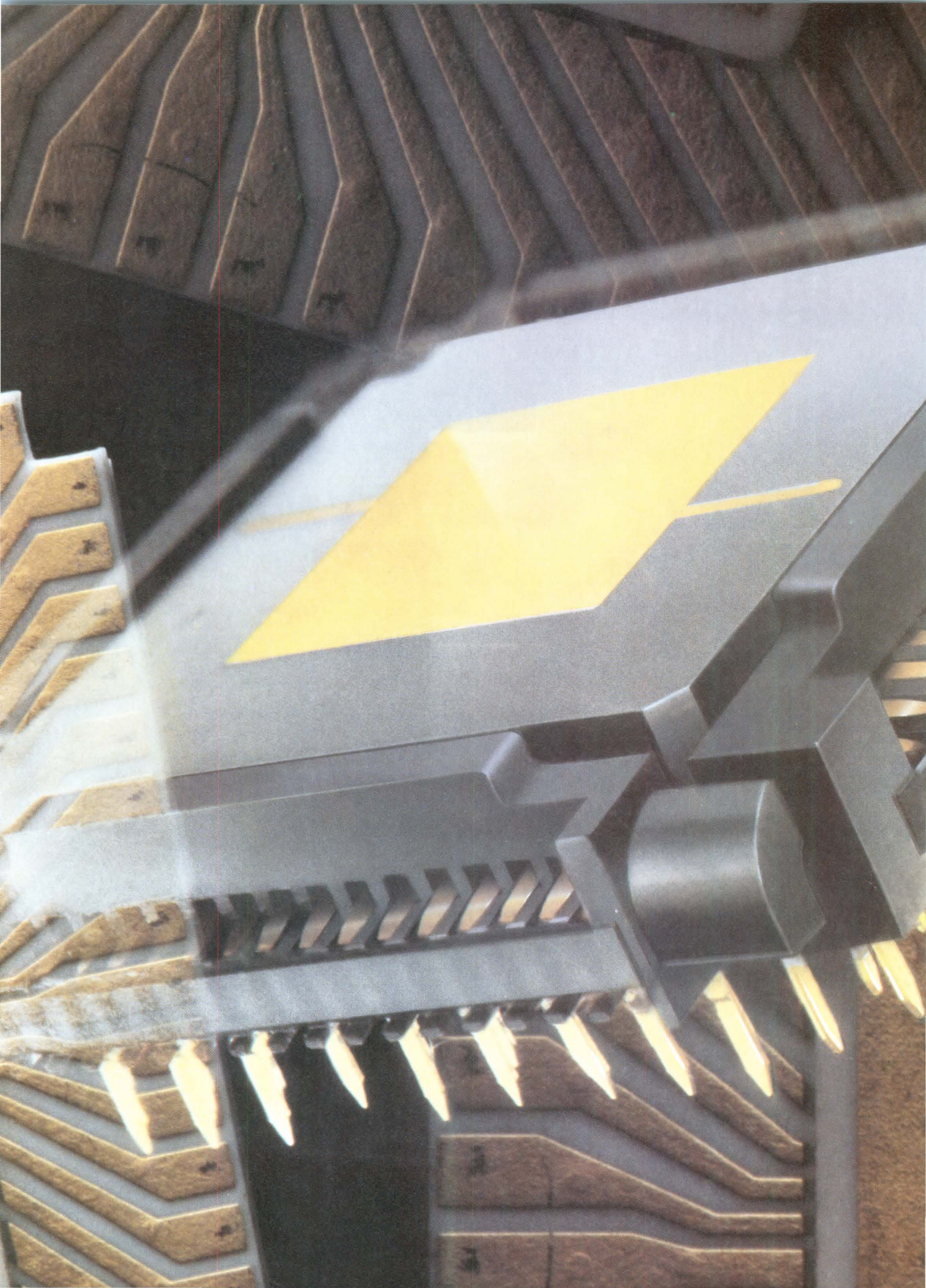

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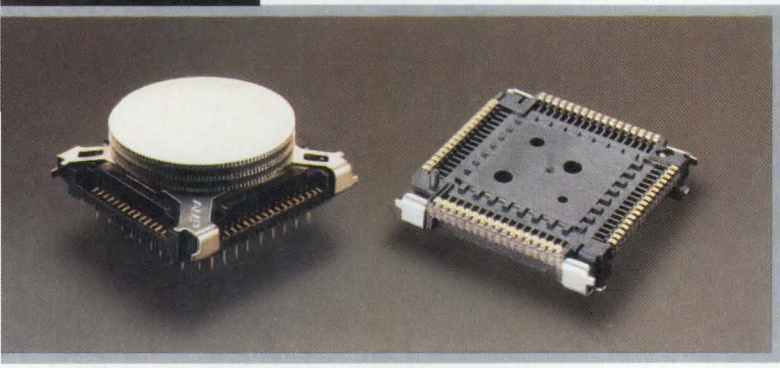

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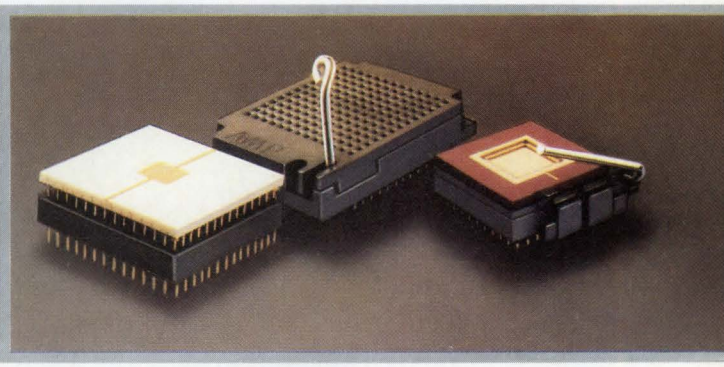

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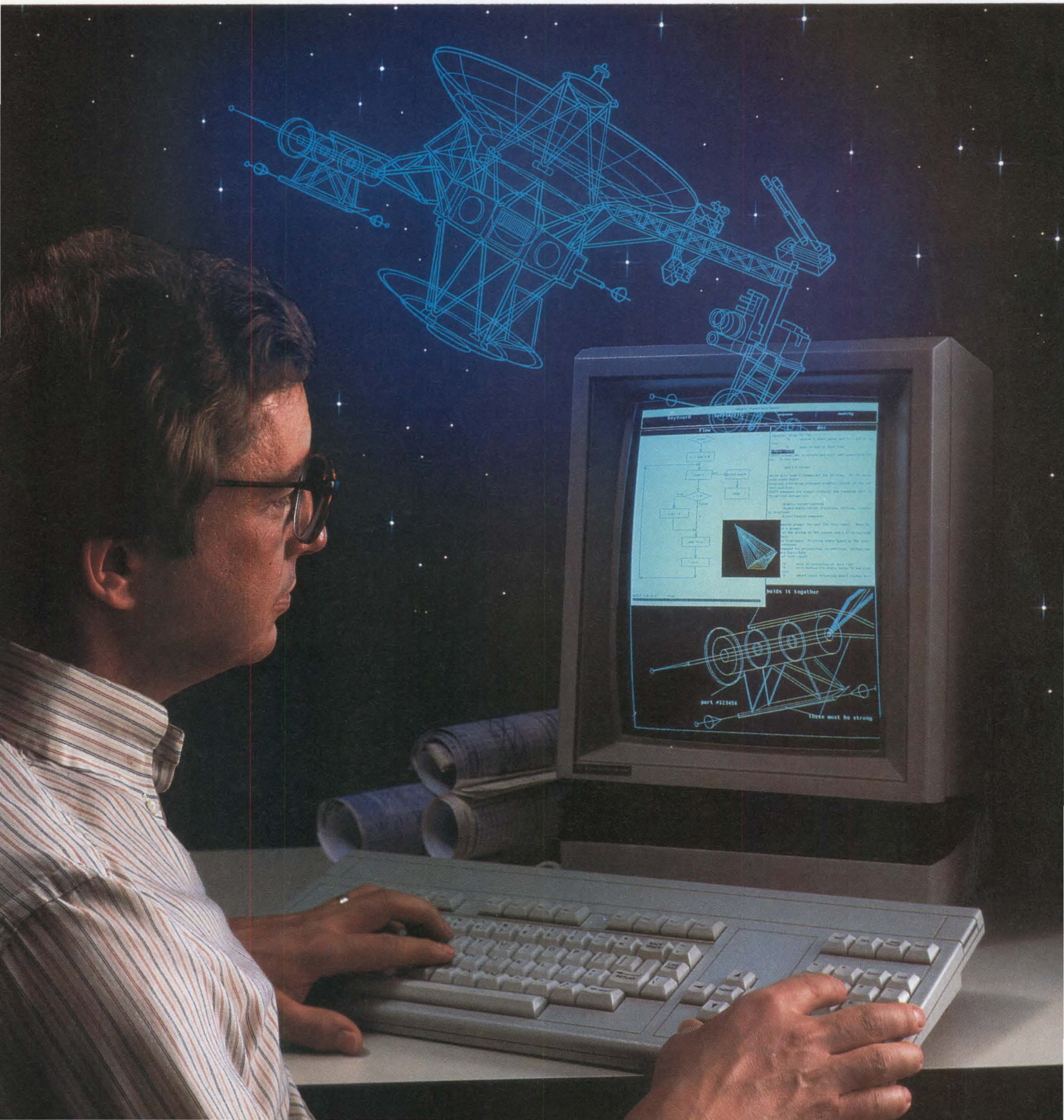

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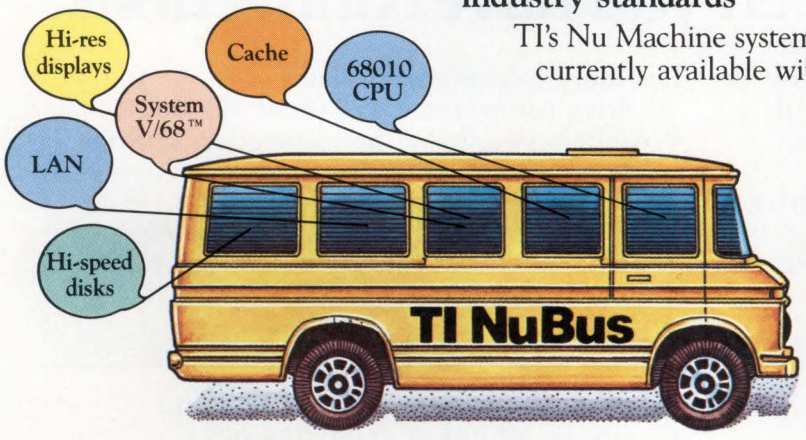

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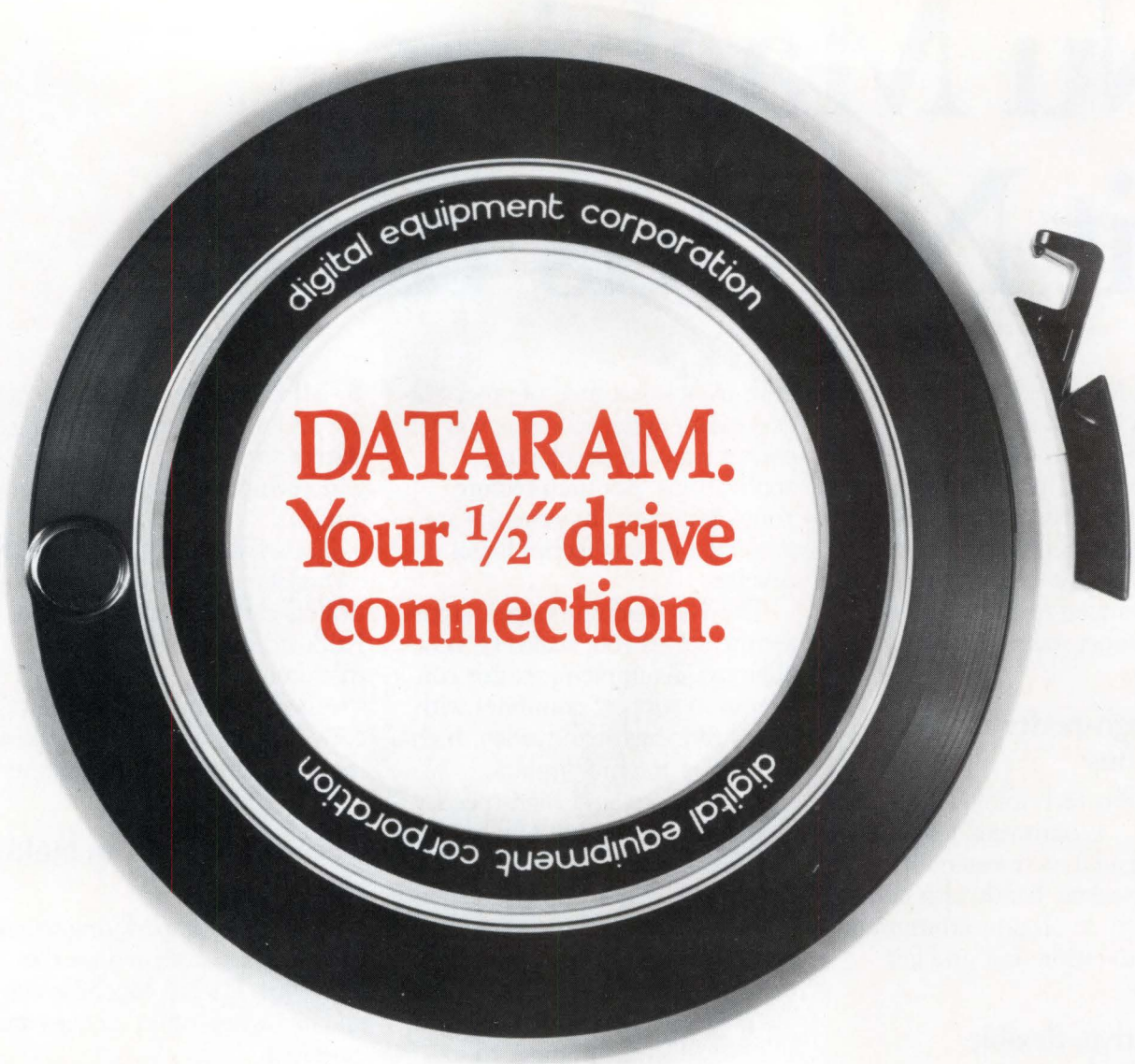

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THIRTY-TWO BIT MICRO SUPPORTS MULTIPROCESSING

Combining processor, memory, and I/O in a 32-bit RISC-like, single-chip architecture allows multiple microprocessors to work in parallel.

by Pete Wilson

With the 16/32-bit microprocessor arena already crowded, introducing yet another family is no trivial task. It requires that the new machines offer something beyond what is currently available. Inmos's transputer family meets this challenge by providing a major performance increase over current micros. The family's first product, the 32-bit IMS T424, executes programs about 10 times faster than a 10-MHz 68000. Since simply outperforming the competition does not guarantee the future, the transputer family is designed with an innovative architecture able to deal with future advances in process technology and wafer-scale products.

Just deciding to be innovative is inadequate. To understand the final decisions made for the transputer family, the 1980 microprocessor marketplace must first be reexamined. Fig 1 gives an accurate picture of repeated attempts to put the processing engine of a decent modern minicomputer onto a single chip. In the attempts, two things are clear: all machines have the same system architecture (a single processor with a single bus issuing from it to which many slave devices are attached), and each new attempt has more transistors in it than the previous one. However, the performance of these designs rarely reflects the effort put into them. Compare, for example, the Z8000 with a 432.

Pete Wilson is microcomputer applications manager at Inmos Corp, PO Box 16000, Colorado Springs, CO 80935. He holds a BS in physics and mathematics from Sheffield University, England.

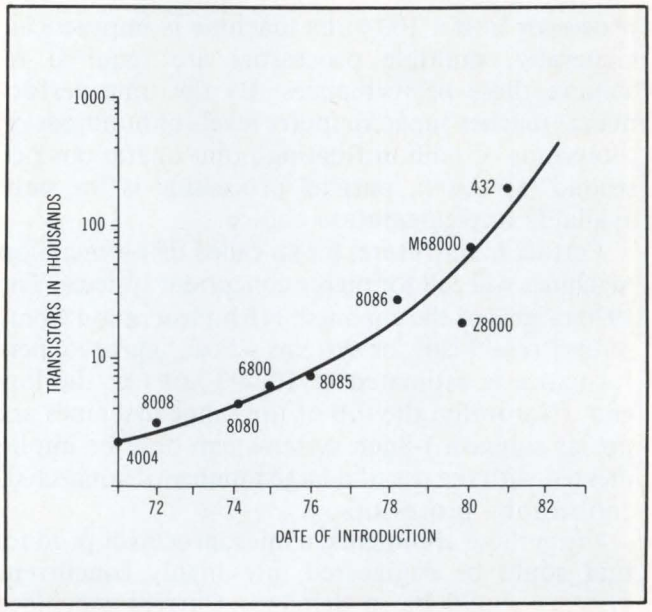

Fig 1 A microprocessor development curve shows the growth of transistor density, over time, in the attempt to wring more performance from what is essentially the same architecture.

Choosing such a complex design does not make good use of the technology. Simply consider what can be built today on a single 4-in. wafer. Approximately 40 million transistors can be put on the wafer and connected to form either memory or processors. They can make around 2 Mbytes of dynamic RAM. Thus, the technology's own costs show that a processor is worth around 4 Kbytes of memory. If current machines reflected this in their architectures, it would be as easy to build a 128-Kbyte, 32-processor system as it is to build a 256-Kbyte, one-processor system. However, this is not the case.

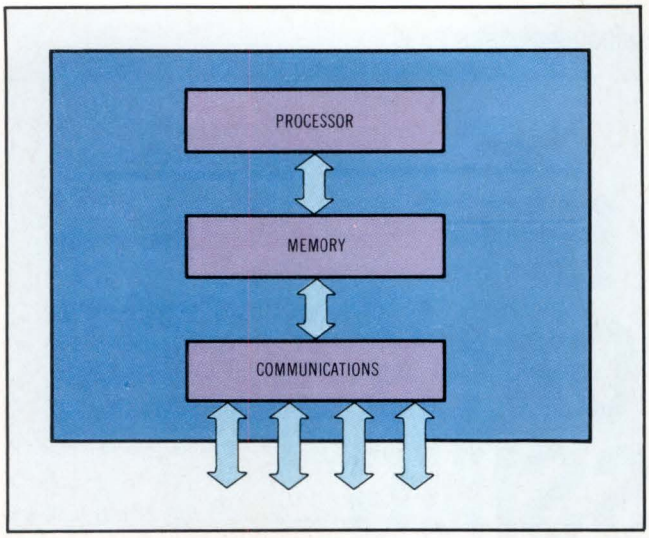

Fig 2 An architectural view of the transputer shows processor, memory, and communications on a single chip.

Nonetheless, the ability to build multiprocessor systems is key to more powerful systems. Redesigning a 1-million instruction per second (MIPS) processor to create a 10-MIPS processor is difficult, but not impossible. However, changing a 10-MIPS processor into a 100-MIPS machine is impractical. Generally, multiple processors are required to achieve these performances. By the time performance reaches supercomputer levels of hundreds or thousands of million floating point operations per second (MFLOPS), parallel processing is the only available implementation choice.

Further in the future, the so-called fifth-generation machines will call for highly concurrent systems. The 1990 targets of the Japanese Fifth-Generation Computer Project call for systems whose aggregate performance is estimated at 10,000 MIPS at the low end. (Naturally, the top of the range machines are not as sluggish.) Such systems can only be implemented with the use of a large number of connected, cooperating processors.

From these arguments, a microprocessor product that could be engineered into highly concurrent systems would be in demand. Current machines simply could not compete effectively. Naturally, it is vital that the concurrency capability does not compromise the microcomputer's abilities in single processor systems. For obvious commercial reasons, the device should outperform traditional microprocessors on their own ground, at the same or lower cost.

With the established aim of a high performance microprocessor well-suited to highly concurrent systems, it is necessary to reexamine the technology to decide on the product's internal architecture. It is accepted, more or less without question, that transistors are getting smaller each year. As transistors shrink, the number of devices per die goes up. This is instantly reflected in design time. The problems of design time explosions and the resultant uncontrollable designs are well-known. The software industry has had consistent difficulties in creating stable operating systems.

As the devices shrink they operate faster, because they need to switch smaller amounts of energy. Regrettably, this speed improvement is lost the moment the signals have to go offchip. The interchip world is still locked in the protocols of TTL, switching relatively large amounts of energy. Interfacing involves a long chain of buffer amplifiers in steadily increasing size and delay, which throws away the speed advantage. This problem, like the design time explosion, will merely get worse while the technology improves. Curing both design time and performance problems while ensuring suitability for use as a parallel system building block are the goals of the transputer.

A transputer is a single-chip product combining processor, memory, and communications (Fig 2). Each chip has multiple high speed communication channels, allowing the device to be connected to other transputers without extra interfacing logic. Each transputer has at least four full-duplex links that allow multi-transputer systems of arbitrary size to be built. Each link has a bandwidth, approximating normal microprocessor bus rates. Topologies are restricted only by the number of links per part.

A transputer can execute programs from its on-chip memory, thus avoiding the performance bottleneck of having to go offchip for each instruction and data access. Since the processor is physically small—a 32-bit version contains about as many transistors as an 8086—it was a manageable design problem. Nearly half of the die area is occupied by the memory, which is (on the first products) 4 Kbytes of static RAM. Redundancy techniques are used, ensuring yield control.

High speed approach yields denser code

The processor's instruction set reflects the design philosophy of the new generation of Reduced Instruction Set Computer (RISC) machines, although the design owes nothing to extant RISC designs. The RISC philosophy implements complex operations as a sequence of simple, very tightly encoded, high speed instructions. This is in stark contrast to the traditional microprocessor/computer approach, which provides a complete repertoire of complex instructions, including all combinations of address modes. This results in physically large (ie, multibyte), and relatively slow instructions. A RISC machine, by careful instruction set and encoding, can produce significantly denser code than a traditional design. Also, a compiler may easily achieve code densities very close to the machine's capabilities. Thus, the transputer is programmable in high level languages without losing efficiency.

Just providing hardware suitable for high performance, highly concurrent systems is insufficient. A

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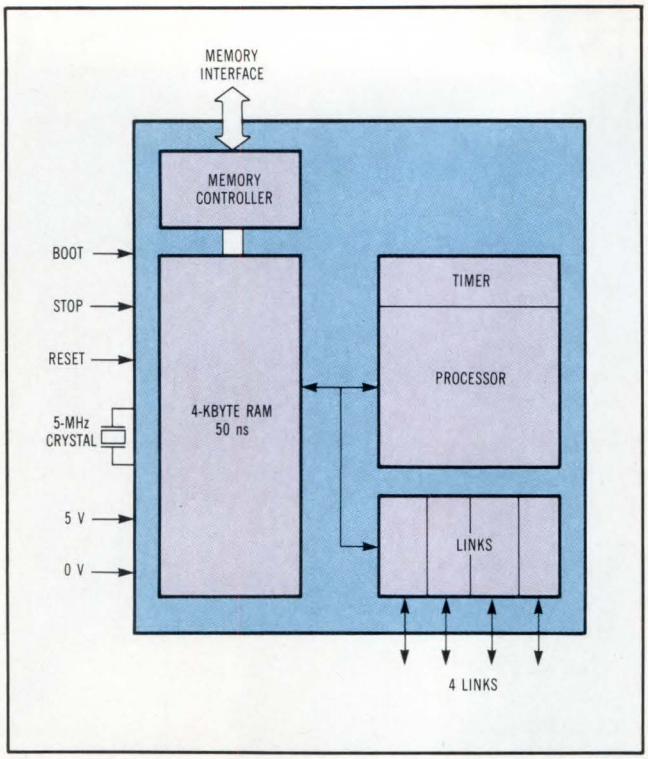


Fig 3 The IMS T424, 32-bit transputer contains a 10-MIPS processor, 4 Kbytes of 50-ns RAM, and four 1.5 Mbyte/s full-duplex communication links. It addresses 4 Gbytes of memory and has an external memory bandwidth of 25 Mbytes/s. Implemented in a 2-μm CMOS process, the chip contains 250,000 devices.

design technology allowing systems to be designed, sized, and programmed is also needed. No traditional programming language is sufficient for programming collections of thousands of connected computers. Those that might (eg, Lisp or Prolog) assume that some other language has arranged the coordination of the machines and the partitioning of the work. These are application languages, not system languages. More modern languages like Modula 2 and Ada capture a degree of concurrency, but assume systems with relatively small numbers of processors—generally below 100—that are normally connected by a bus or shared store. In addition, they make assumptions about system application requirements that may be entirely inappropriate for upcoming novel architectures.

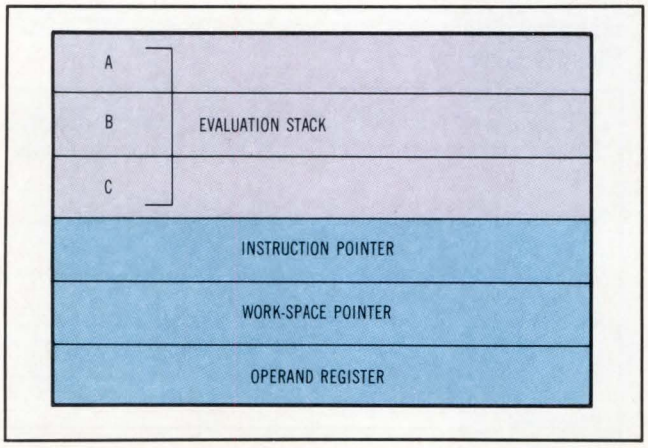


Fig 4 The register set consists of a small set of function specific registers to minimize process swap time and simplify compiler design.

Thus, Inmos has developed Occam, a language suitable to the task. Covered in a series of articles in *Computer Design* from November 1983 to January 1984, Occam takes the same building-block view of the world as the transputer. It considers the world to be constructed from independent, concurrent processes with their own local concerns. These processes can occasionally interact by sending or receiving messages.

The Occam communication model is simple and universal, involving minimum overhead and allowing very efficient hardware implementations. An Occam program can be written independently of the transputer on which it will eventually be executed. When there are more processes than processors, a transputer will time-share itself between the processes requiring attention. The transputer's instruction set includes facilities to directly support the Occam process and communication model. The result is that process communication is no more expensive than multiplication.

The first transputer product is the IMS T424 32-bit transputer. Fig 3 gives an overview of the machine. It contains a true 32-bit processor, 4-Kbyte onchip static RAM, 4 Inmos links, and a parallel interface for the connection of extra offchip memory and traditional device controller chips. The numbering scheme chosen for Inmos transputers provides a short-form definition of each part; the first "4" in T424 indicates 4-byte internal working, the "2" is the n in 2^n, indicating 4-Kbyte onchip memory, while the last "4" denotes a 4-byte wide data path to external memory. Future transputer family members will implement a variety of the obvious possible combinations; the second transputer is a T222.

The device is clocked by a 5-MHz signal. This can be either a directly connected crystal, or a signal from a separate clock. The machine itself, in standard form, operates with a 50-ns minor cycle, and obtains this by multiplying up the 5-MHz external clock to provide the required internal clock.

Registers and functional units are regular bit-slice designs with data buses flowing through them. Control signals are generated from a microcode ROM, optimized to match both the size and control line pitching of the data path.

The register set is shown in Fig 4. Rather than keeping variables in general purpose registers, the T424 keeps them in store, copying their values to and from registers attached to the ALU for computation. This has a number of benefits. First, context switching is very efficient since variables do not need saving and restoring. Second, in conjunction with the instruction set, compilers may be very simply designed to generate dense code without the

problems of register optimization. Third, there is no arbitrary limit set on the number of local variables, as there would be if a fixed number of registers were used to hold the values of variables.

The work-space register points at the address of the first variable in store. On a procedure call, the pointer value changes to point at the first variable of the called procedure. This allows simple and efficient implementation of normal high level languages.

The A, B, and C registers form an evaluation stack that is the source and destination for most arithmetic and logical operations. Loading a value into the stack pushes B into C, and A into B, before loading A. Storing a value from A, pops B into A, and C into B. A stack size of three was chosen as the minimum that was practicable. Three words are needed for operations like multiply and divide, although in evaluating complex expressions, a compiler may need to create some temporary variables for partial results. However, simulations showed that a significantly greater stack size would be necessary to improve substantially on the three. This would have used extra silicon area with a concomitant slowing of the processor.

Direct functions

There is just one instruction format—each instruction is 1-byte long, and is divided into two 4-bit parts. The 4 MSBs of the byte are a function code, and the 4 LSBs are a data value (Fig 5). The representation provides for 16 functions, each with a data value ranging from 0 to 15. The 16 functions are split into three groups to provide direct functions (one-address instructions, generally pushing data to, or popping data from, the evaluation stack); indirect functions (zero-address instructions manipulating values held in the evaluation stack); and operand extension instructions (work with the operand register to allow data values larger than 4 bits to be constructed).

Thirteen of the direct instructions provide a general purpose set of functions listed in the Table. The most common operations performed by a program are loading and storing one of a small number of variables, and loading small literal values. The load constant instruction enables values between 0 and 15 to be loaded with a single-byte instruction.

The load-local, store-local, and load-local pointer instructions all access locations in memory relative to the work-space pointer. The load and store nonlocal and load nonlocal pointer instructions behave similarly—except that they access locations in memory relative to the A register. Compact sequences of these instructions allow efficient access to data structures, and provide simple implementation of the static links or displays used to implement block-structured programming languages.

One direct function causes its data value to be interpreted as an operation on the values held in the evaluation stack. These zero-address instructions are also listed in the Table. This allows up to 16 operations to be encoded in a single instruction. The operand extension instructions access many more operations via instruction sequences. In choosing which functions to encode in the base, single-instruction operations (the results of an investigation into programs compiled for the transputer) were used. The most frequently used operations were chosen to be encoded into single instructions. These include add, subtract, multiply, and divide.

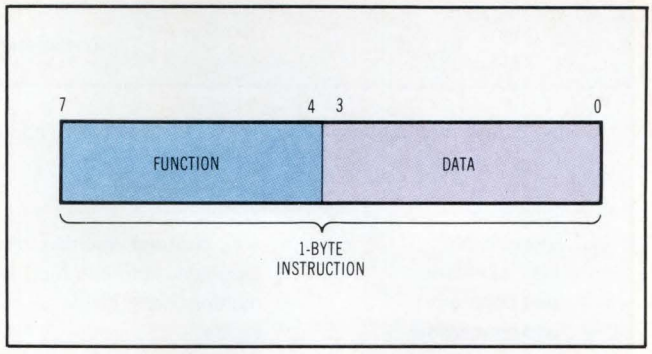


Fig 5 In the instruction set, all instructions are 1 byte long. The 4 MSBs represent a function code and the 4 LSBs are data.

Measurements show that about 80 percent of the executed instructions are encoded in a single instruction.

Three further instructions provide comparisons and conditional behavior. The equal-zero instruction loads the A register with a truth value; true if A is initially zero, false otherwise. Similarly, the greater than instruction loads the A register with true if B > A, false otherwise. True and false are represented by 1 and 0, respectively. Consequently, the conditional jump instruction also serves as jump if true. True and false can be loaded with single-byte load constant instructions. All conditional testing and branching can be compactly implemented using the instructions equal-zero, greater than, difference, and conditional jump.

In addition, further instructions provide addressing capability with both byte and word subscripting provided. These instructions treat A as holding a base address and B as the subscript.

Measuring performance

Measurements show that about 80 percent of the executed instructions are encoded in a single instruction. Many of these instructions, such as load-local and add, require just one 50-ns processor cycle.

The T424 addresses its memory one word at a time, thus providing four instructions for each memory access. The processor has an instruction buffer and a prefetch buffer, allowing four instructions to be worked on while the prefetch is getting

Transputer Instruction Set

One-address instructions	Zero-address instructions
load local	arithmetic:
store local	add, subtract, multiply, divide remainder, normalize
load constant	long add, long subtract, long multiply, long divide
add constant	multiply, long divide
add to memory	logical:
load local pointer	and, or, xor, shift left, shift right
load nonlocal	comparison:
store nonlocal	difference, greater than, equal zero
load nonlocal pointer	general:
jump	load byte, store byte, byte count, word count, byte subscript, word subscript, check subscript, extend to word, check partword, extend to double, check word, reverse, return, minimum integer, initialize
conditional jump	
call	
adjust workspace	concurrency and communications:
	move message, input message, output message, start process, end process, start, enable channel, enable timer, disable channel, disable timer, ALT wait, read timer.

the next four. This pipelining is effective because while the processor rarely has to wait for an instruction, the pipeline is short enough for jumps to cause only a minimal time penalty when prefetched instructions need to be discarded.

Because of the direct mapping of most high level languages into the transputer instruction set, it is possible to provide a lookup table to estimate program size and execution time. The lookup table gives the execution time and object-code size of program fragments (eg, the name of a variable, or an addition). Total program size and execution time are the sum of the values of its fragments. The lookup table provides average values, including the effects of the compiler creating temporary variables and operand extension instructions. Generally, the lookup table will give results accurate to around 10 percent for medium-sized and larger programs.

To put the T424's performance in perspective, a simple benchmark, the sieve of Eratosthenes, is run against an 8-MHz 68000. The T424's performance is estimated under the worst conditions of onchip execution and offchip data access. The conditions are considered the worst because instruction pipelining cannot conceal the relative slowness of offchip memory. Moreover, although the sieve is a small program, the performance table is used to estimate speed. This means that figures for variable access are those appropriate for a bigger program. Finally, the comparison is of a compiled high level language program (ie, Occam) against a handcrafted 68000 assembler. Nonetheless, the T424 performs nearly four times as well as an 8-MHz 68000, and requires a significantly smaller code size.

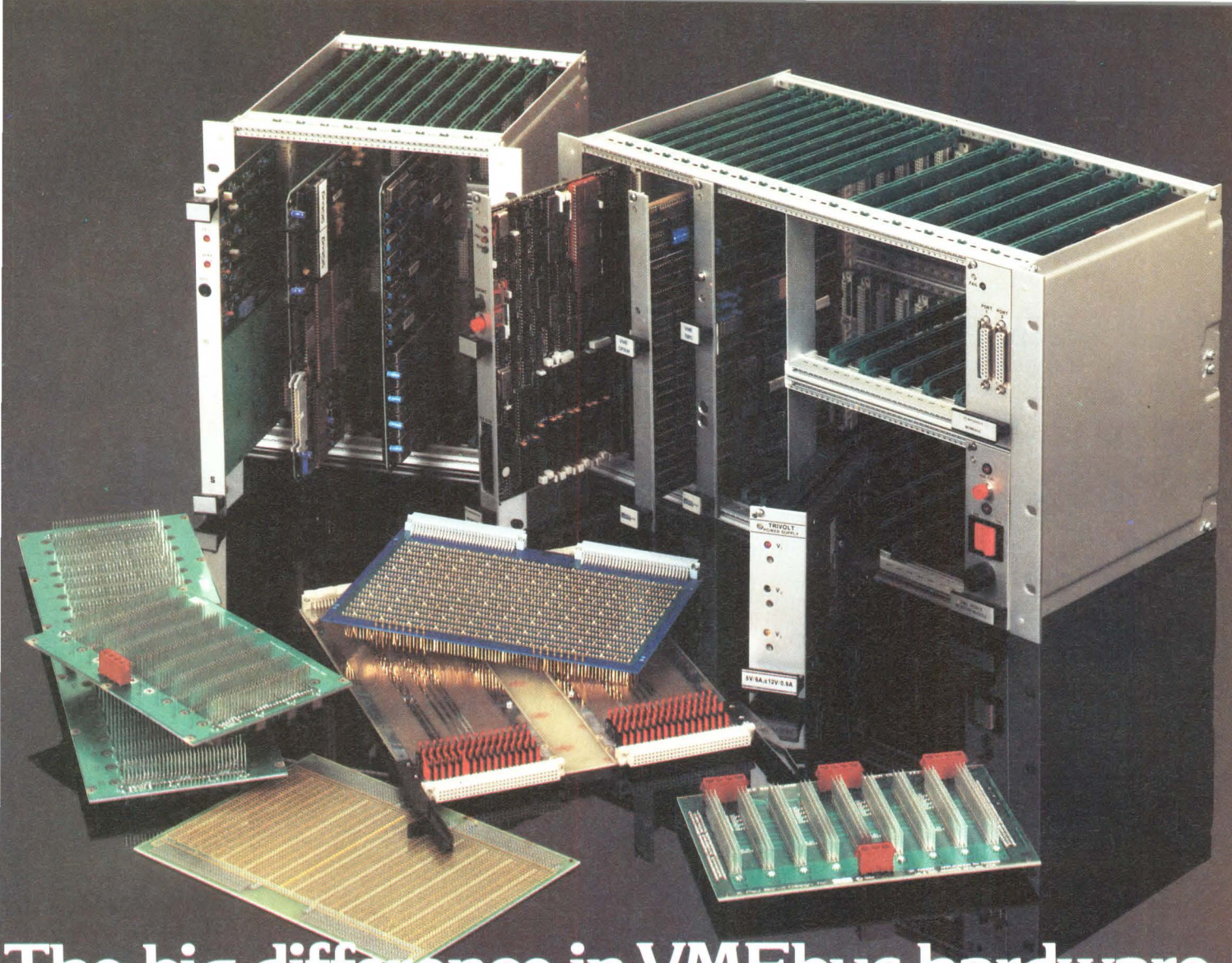
Most microprocessor applications call for more than a 4-Kbyte memory. The parallel interface provides the ability to connect a large amount of external memory to the T424. Both static RAM and dynamic RAM are supported. For DRAM, the interface can provide a 9-bit refresh address as well as explicit column address strobe (CAS) and row address strobe (RAS) signals.

The interface is configurable. Up to sixteen popular "programs" built in to the interface are available. They are selectable by connection of a configuration pin. If other configurations are desired, they can be selected from an external ROM at power-up time. The configuration includes the ability to set the following times: access, cycle, address-setup, address-hold, precharge, write-data setup, write-data hold, and the timing of each of these nonspecific strobe lines individually to within a 25-ns tolerance within a cycle.

The processor perceives the external memory to be a linear extension of onchip memory. As with all transputers, the internal width of the machine defines the address space, so the T424 can address up to 4 Gbytes of memory. Both program and data can be freely positioned anywhere in the address space. The only difference between on- and offchip memory, as far as the processor is concerned, is that offchip memory will generally be slower.

Replacing traditional microprocessors

The description thus far is of a high performance microprocessor that happens to have some very fast local RAM onchip. As such, the T424 can be looked upon as a straight replacement for traditional microprocessors (eg, the 68000, 8086 family, or Z8000). Any system designed around these machines can be simply reimplemented, without significant redesign, using a T424. The changes will be limited to aspects such as different PC board layout to reflect the simpler interfacing. Porting the software should be no problem either. Not only does Inmos provide compilers for C, Fortran, Pascal, and Occam (with



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mixed language capabilities), it actively encourages third-party software vendors to retarget their compilers and operating systems to the transputer family. The most obvious results of the change to a T424 include smaller PC boards, a three- to tenfold improvement in performance, and perhaps a 20- to 40-percent reduction in program memory requirements. However, the T424, designed to act both as a traditional microprocessor and as a computing component in a highly concurrent system, includes many features to make such systems very efficient.

First, the designer of a highly concurrent system generally wants to create software that is not tied to a specific number of machines. It is more convenient to trade cost and performance by varying a system's transputer count. Using Occam to design and implement the software makes this fairly straightforward. However, when running software aimed at thousands of connected transputers on fewer machines, those machines must be multiplexed so that they behave to the software in the same way that a larger number of machines would.

Constructing multiprocessor systems requires some form of interprocessor communication.

Processor multiplexing is implemented in the T424's instruction set. Both interprocess communication and the sharing out of the processor are done by special instructions. Each process is represented in the machine by a work space. The work space contains both the local variables of the process and necessary red tape for the processor to housekeep the communications and multiplexing. The processor executes just one active process at a time. The work space pointer points at the current process, while the remainder are held in a queue. They are looked after by a pair of registers indicating the first and last entries.

In practice, the scheduler provides two priority levels; normal and priority. Priority processes can perform tasks commonly accomplished with interrupt routines. If a normal process is being executed, and a message arrives for a priority process, the processor typically starts to execute the priority process within 650 ns (ie, the average 50 ns for the current intrustion to complete, plus a 600-ns switch time). Multiplication and division take approximately 2 μs, slowing the switch. Block move operations are interruptible. Normal processes resume execution only when no priority processes can proceed.

The current process will cease being executed if it attempts communication with a process that is not yet ready; the processor suspends the process and chooses the next process from the front of the active queues. When the partner process eventually attempts communication itself, the processor transfers data, places the suspended process on the back of the appropriate queue, and continues execution of the partner. This communication-driven scheduling is frequent enough in concurrency-oriented programs intended for multiprocessor applications to share processor time fairly. However, some sequential programs may, if left to themselves, unfairly hog processor time. So, mechanisms to implement time-slicing are also provided.

Constructing multiprocessor systems requires some form of interprocessor communication. Rather than shared-store or bus-oriented schemes, the T424 provides four links, each of which implements a pair of Occam channels (one in each direction). The links work full duplex at rates up to 20 Mbits/s in each direction simultaneously, and look to the processor just like channels. The hardware distinguishes between channels connecting multiplexed processes (which are implemented as a single word of memory), and link channels by address. Thus, by appropriate parameterization, processes can be written to communicate with other processes without knowing whether their partners are on the same chip or on a different one. The compiler produces the same instruction sequence for either.

Each link has two pins, so that a transputer is connected to another by two one-directional signal lines. Each signal line is used to carry data and control information.

Links are primarily intended for use on a single PC board, or between boards on the same backplane. They are straightforward to use. The only requirements are that the maximum capacitance specification is not exceeded, and that the input clock frequencies of two interconnected transputers are within 100 ppm. Because the input and output pins of the link are TTL compatible, the range of a link can be extended by inserting standard (eg, RS-422/423) line drivers and receivers in each of the two signal lines.

The instruction-set architecture chosen for the transputer has one very important side effect. It is no longer necessary to consider programming in assembler, since compilers can do as good a job of code generation as the best assembler hacker. Indeed, Inmos has no intention of providing an assembler for the transputer family, although the details necessary to write compilers will, of course, be available.

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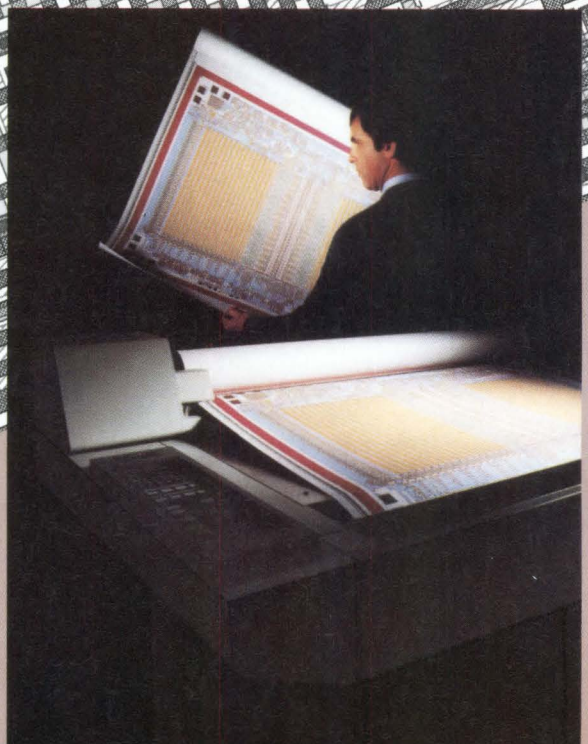

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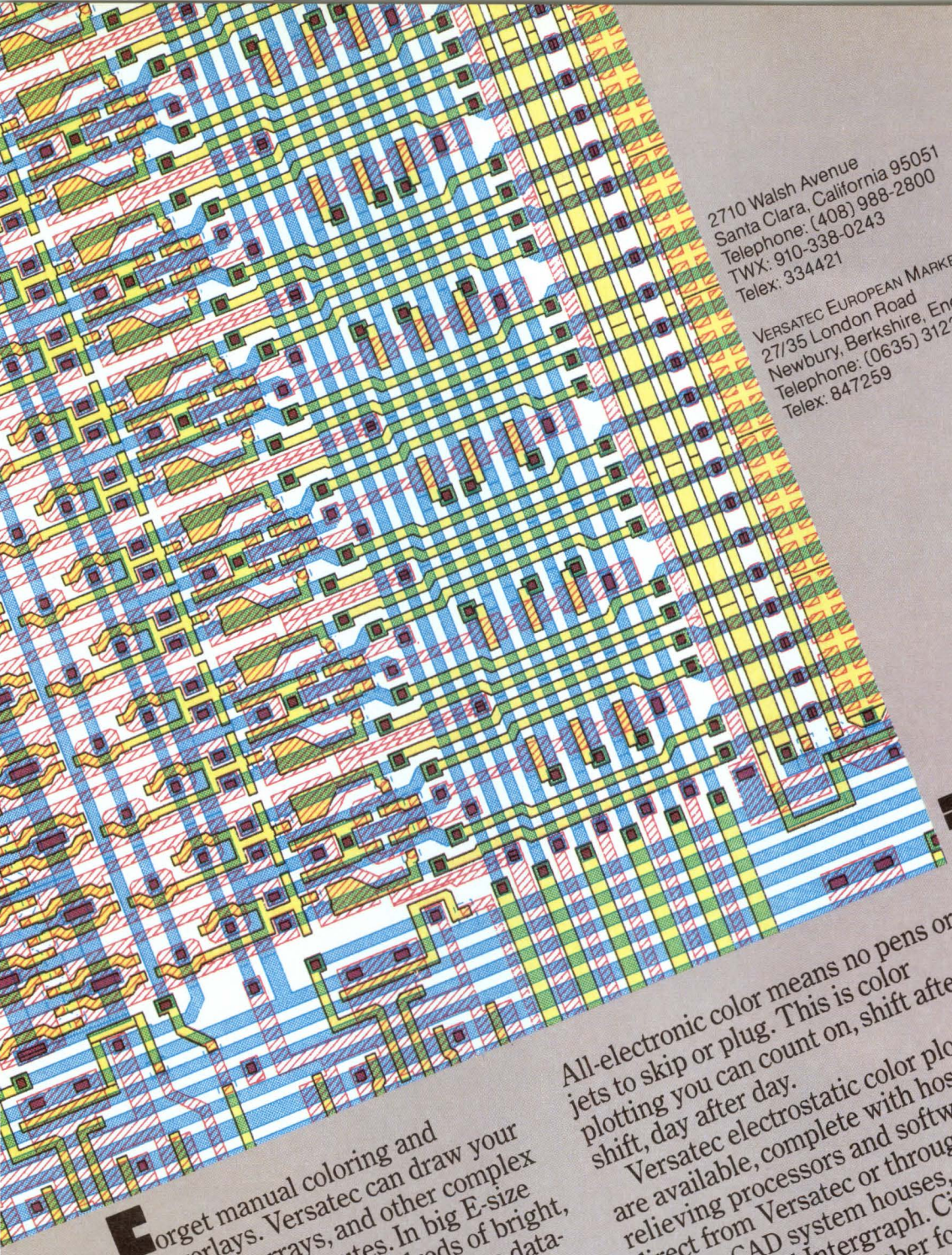

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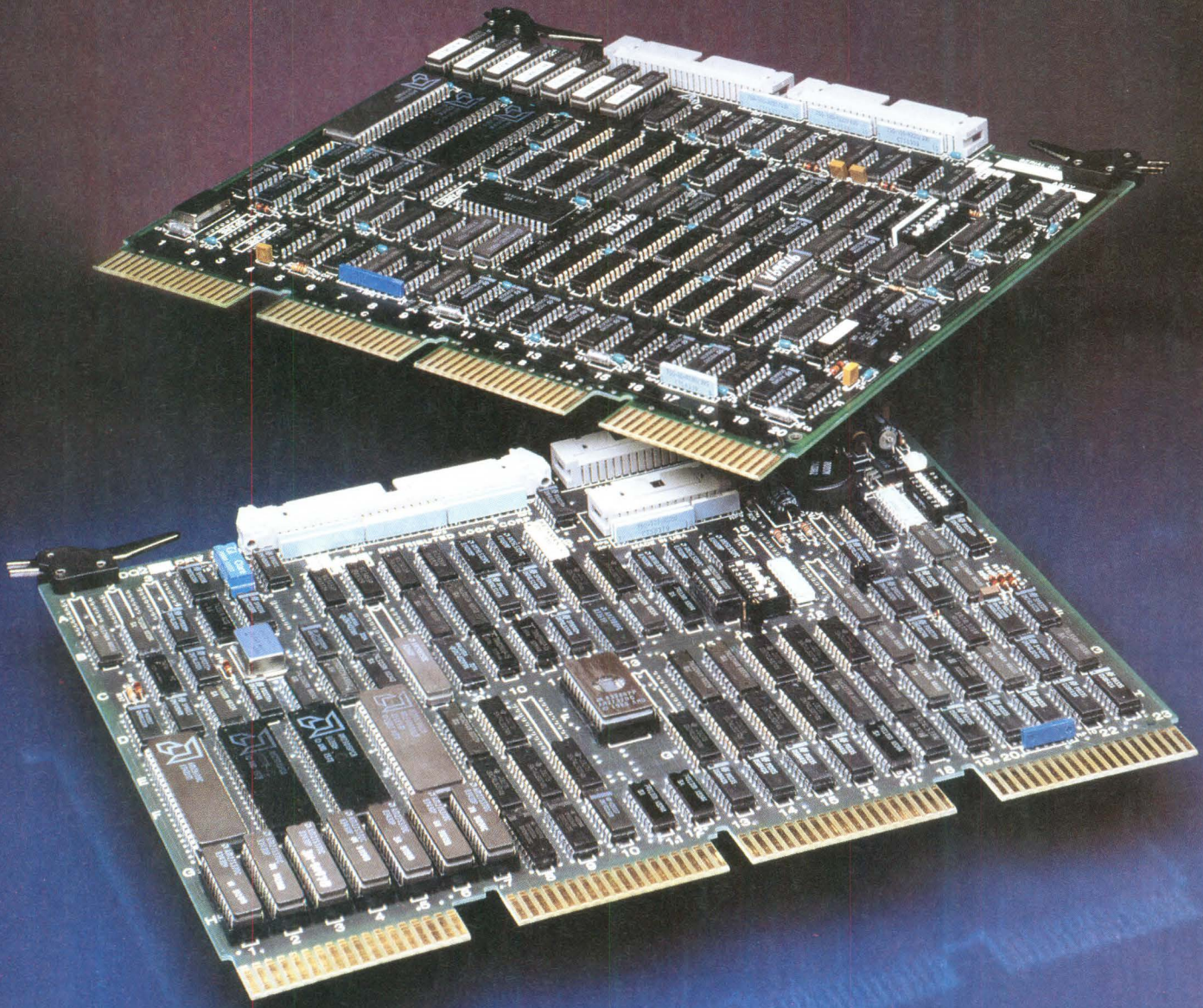

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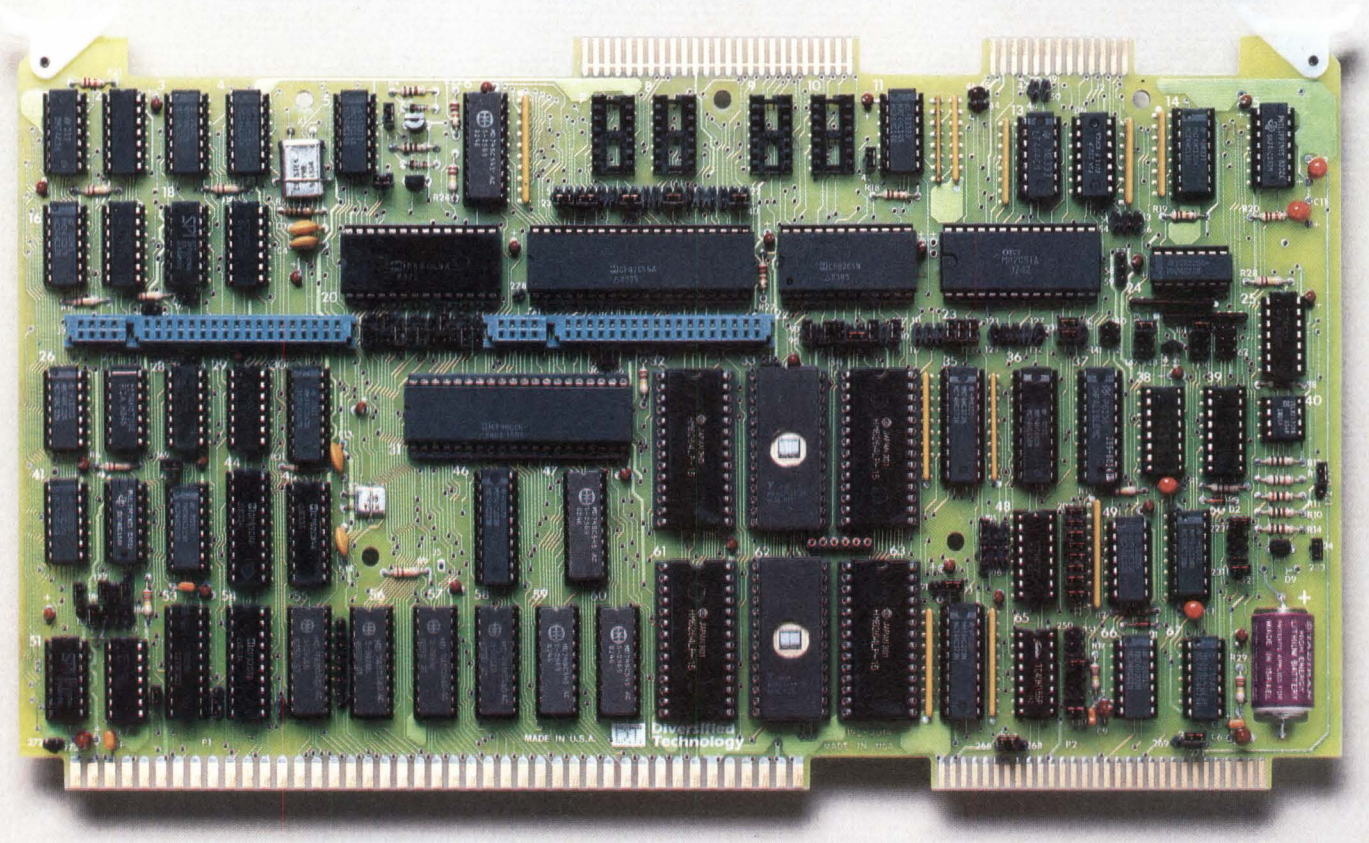

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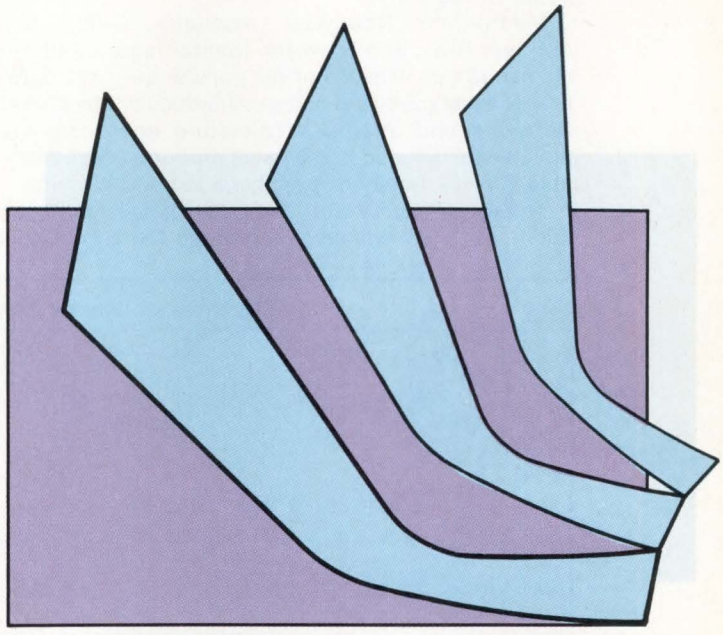
CMOS MICROS ENTER THE MAINSTREAM

The technology of choice for future 32-bit microprocessors is CMOS. In fact, current 8- and 16-bit CMOS microprocessors already offer features that are unavailable in NMOS.



by Walter J. Niewierski

Trends in CMOS microprocessors follow two paths. Major architecture developers dedicate new designs directly to CMOS while CMOS manufacturers, with no foothold in architecture development, convert existing NMOS designs to CMOS. Regardless of the approach taken, however, special attention is given to enhancing the inherent benefits of CMOS in low power systems. Thus, each CMOS CPU has specific features that offer advantages over comparable NMOS products. These include static design, extended instruction set, power-down instructions, and internal architecture enhancements (see the Panel, "An overview of CMOS microprocessors").

Mainstream microprocessor architectures implemented in CMOS, with additional low power features to enhance the already low power CMOS, provide the most popular route. This path offers low power benefits and takes advantage of the established base of hardware and software designs that exist for the NMOS processors. This method not only provides a path for CMOS microprocessor product development in those companies that are not architecture trendsetters, but it also extends the life of existing NMOS architectures by opening new low power system design possibilities.

The major architectures that have been implemented in CMOS are the familiar Intel (Santa Clara, Calif) 8085, 8086, and 8088; Zilog (Campbell, Calif) Z80; and the Commodore (Norristown, Pa) 6502. A smaller portion of the CMOS microprocessor market (in terms of device type available, but not in quantity shipped) has featured those processors with architectures or pin definitions that are unique when compared to NMOS products. The microprocessors comprising this portion are the Harris (Melbourne, Fla) 6120, National Semiconductor (Santa Clara, Calif) NSC800, and the RCA (Somerville, NJ) 1802.

Of these, the RCA 1802 is the only one that has a truly original architecture. The rest borrow from other areas, whether it be NMOS microprocessors or minicomputer architectures; hardware or software. The NSC800 from National Semiconductor is derived

Walter J. Niewierski is currently a technical marketing engineer at Harris Corp, Semiconductor Digital Products Division, PO Box 883, MS54-130, Melbourne, FL 32901. He is responsible for technical support of the CMOS 80C86 microprocessor family. He holds a BS in electrical engineering from the University of Michigan.

from both the Z80 and the 8085. The Harris 6120 is designed to be software compatible with the Digital Equipment Corp (Maynard, Mass) PDP-8E.

In this context, microprocessors create an entirely new ball game when compared to logic or memories. Support is the key in the microprocessor market. Extensive support in terms of development systems, hardware designs, software operating systems, and people is needed to generate significant levels of design-ins. This makes the existing-architecture conversion to CMOS the simplest route for both the manufacturer and the designer.

Another reason why many manufacturers have changed to CMOS is the power barrier into which NMOS is running. Exemplified in Fig 1, second-generation NMOS 16-bit microprocessors are hitting the upper limits of package power dissipation capabilities. Dissipation levels of 2 to 3 W per package are becoming commonplace in high complexity NMOS processors.

An overview of CMOS microprocessors

In considering the CMOS microprocessors available, 8-bit microprocessors are still the most common (see Table). For example, OKI Semiconductor (Santa Clara, Calif), has announced the 80C85. This device is compatible with the NMOS 8085 and is supported by several CMOS peripheral products. The OKI design of the 80C85 is not static and requires a constant clock with a minimum frequency of 500 kHz to refresh internal dynamic registers.

Meanwhile, Rockwell (Anaheim, Calif), GTE (Tempe, Ariz), and Synertek (Santa Clara, Calif) are shipping CMOS versions of the popular 6500 microprocessor family. Several pinout variations are available. Software and internal architecture enhancements have been included in the CMOS products. Also available is a full family of peripheral support circuits.

Toshiba (Tustin, Calif), with a CMOS version of the Zilog Z80, is scheduled to introduce the Z84C00 this year. The model is static in design with TTL-compatible inputs over the industrial temperature range. Although no version is completely compatible with the NMOS product, several other versions of the Z80 exist in CMOS. The National Semiconductor NSC800 will execute the instruction set of the Z80, although it is not pin compatible.

For controller applications in severe environment situations, and for portable battery-operated systems, RCA has developed the 1802. It has been augmented by several processors of varying architectures, all designed to focus on specific applications. Complete 1802 peripheral and memory circuit support is available along with several development systems and higher level languages. The 1802 is static in design.

The NSC800 has also coupled the internal architecture and instruction set of the Z80 with a unique pinout resembling the external bus structure of the

Performance Characteristics of CMOS Microprocessors

	Operating frequency		Operating current at maximum frequency	Standby	Guaranteed V_{CC} range	Temperature range guaranteed*	Sources
	Minimum	Maximum					
8-bit							
80C85	500 MHz	3 MHz	22 mA	NA	5V ± 5 percent	I	OKI
65SC02	dc	4 MHz	16 mA	10 μA	5V ± 10 percent	C,I,M	GTE, Synertek, Rockwell
NSC800	32 kHz	4 MHz	—	NA	5V ± 10 percent	C,I	National Semiconductor
1802	dc	5 MHz	6 mA maximum	200 μA maximum	4 to 6.5 V 4 to 10.9 V	I,M	RCA, Hughes
6120	dc	5 MHz	10 mA maximum	500 μA maximum	5V ± 5 percent	I,M	Harris
Z84C00	dc	2.5 MHz	15 mA maximum	10 μA maximum	5V ± 10 percent	I	Toshiba
8/16-bit							
80C88	dc	5 MHz	50 mA maximum	500 μA maximum	5V ± 10 percent	C,I,M	Harris
65SC802	dc	4 MHz	20 mA maximum	—	5V ± 10 percent	I	Western Design Center, GTE
16-bit							
80C86	dc	5 MHz	50 mA maximum	500 μA maximum	5V ± 10 percent	C,I,M	Harris
J-11	—	15 MHz	200 mA typical	—	5V ± 5 percent	C	DEC

* C = Commercial (0 to 70 °C)
I = Industrial (−40 to 85 °C)
M = Military (−55 to 125 °C)

To overcome this power problem, many new third-generation 16- and 32-bit processor families are being initially developed in CMOS. This represents a major shift in philosophy for NMOS houses. CMOS is no longer merely a nice little low power technology for special applications; it is the technology that will allow microprocessor architecture developers to create advanced generations of their devices.

The most significant benefit of CMOS microprocessors is the power they save compared to NMOS and bipolar devices. In systems where direct replacement is possible, an immediate (but not optimum) reduction in power is achieved. Although a power supply reduction may not occur, reduced power usage will. Direct replacement of ICs for lower power is a relatively simple matter, but redesign of existing systems to reduce power supplies, fans, and other cooling equipment may not be economically feasible. In order to take full advantage of the low power characteristics of CMOS, systems need to be designed for low power from conception.

8085. The NCS800 has three operating frequencies: 1, 2.5, and 4 MHz. Several peripheral combination chips are also available in CMOS. The NSC800 is not static and requires a minimum clock frequency of 32 kHz.

From Harris, the 6120, developed for Digital Equipment Corp, provides a CMOS processor that is software compatible to the DEC PDP/8E. The HD-6120 is actually a 12-bit machine and emulates the instruction set of the DEC PDP/8E. Completely static design allows operation from dc to 5 MHz. Simplified I/O and memory control signals make the 6120 easy to use with standard memories and peripherals.

Microprocessors with 8/16-bit CMOS are also available. The 80C88, introduced by Harris in May 1984, is directly pin-for-pin, hardware and software compatible with the NMOS 8088. With an operating frequency range of dc to 5 MHz, the 80C88 is static in design. Power supply current specifications are the same as the 80C86 with a standby current of 500 μA maximum, and an operating current of 10 mA/MHz. Intel is a licensed alternate source for the 80C88. A complete family of peripheral and bus circuits to support system design is available.

Western Design Center (Mesa, Ariz) has announced a CMOS 16-bit upgrade of the 6502, 8-bit processor. Two versions will be available: the 65SC802 (completely 6502 hardware and software compatible with an 8-bit external bus, an expanded instruction set, and internal 16-bit architecture), and the 65SC816 (8-bit data bus with expanded addressing to 16 Mbytes of memory). GTE will also produce the part.

Harris is currently in production with the 80C86, a CMOS 16-bit microprocessor that is hardware and software compatible with the industry standard NMOS 8086. The completely static CMOS design has an operating frequency range of dc to 5 MHz. Stopping the CPU clock yields a standby current of 500 μA maximum while the operating current is 10 mA/MHz. Intel is a licensed alternate source for the 80C86.

The J-11 from DEC is a CMOS microprocessor chip set that emulates the DEC PDP-11. Designed and manufactured by the Harris Semiconductor CMOS Digital Products Division, the J-11 is a two-chip CMOS processor. Each device is packaged in an 84-pad leadless chip carrier (LCC) and both are mounted on a 60-pin dual-inline ceramic substrate. Completely static in design, the Micro J-11 will execute the PDP-11 instruction set and has many advanced hardware features such as complete PDP-11-70 equivalent on-chip memory management, a 32-bit internal data path, and 4-Mbyte addressing capability. Operating frequencies from dc to 15 MHz are possible with the static design of the two chips.

Designing low power CMOS systems

The best approach is to do initial CMOS system design with low power systems in mind. Designers must consider the global implications of reducing operating power by more than 90 percent—ie, what can be reduced, replaced, or eliminated when power and heat are significantly reduced. The biggest reduction will initially be in size and weight. Large, bulky power supplies can be eliminated and replaced with small converters or batteries. Even if a standard power supply is necessary, it will be much smaller as long as CMOS plays a dominant role in the system design. The system should include not only the processor, but also peripheral support circuits, logic RAM, and nonvolatile memory.

With the lower operating temperatures of CMOS, heat-related hardware such as fans, heat sinks, and dissipation panels can often be eliminated. Without the need for cooling equipment and airflow, sealed enclosures become possible. Sealed enclosures reduce electromagnetic interference (emi) and lead to higher device and system reliability. Less weight leads to true portability for instrumentation and personal computers. Moreover, lower power and lower heat dissipation allow high density system packaging in space-critical designs. This would not be possible with NMOS and bipolar components.

All aspects of low power system design are manifested in lower system cost. In the application shown in Fig 2, a typical NMOS/bipolar system is redesigned for CMOS and low power. The system cost is broken down into three areas: semiconductors, power supply, and cooling equipment/fans/enclosures.

Costs for CMOS semiconductors are somewhat higher than those for NMOS and bipolar devices. Most CMOS microprocessors are relatively new, low volume products. As products mature, CMOS manufacturing costs decrease, driving prices lower due to higher volume. Also, the extra cost of processing CMOS can be recouped if system design is truly low power, because expensive cooling equipment and power supplies are eliminated. A reduction in from 25 W (5 V, 5 A) to 1 W (5 V, 200 mA) can result in a power supply cost reduction of approximately $50 to $100, depending on the type of power source. The use of batteries makes it even less expensive.

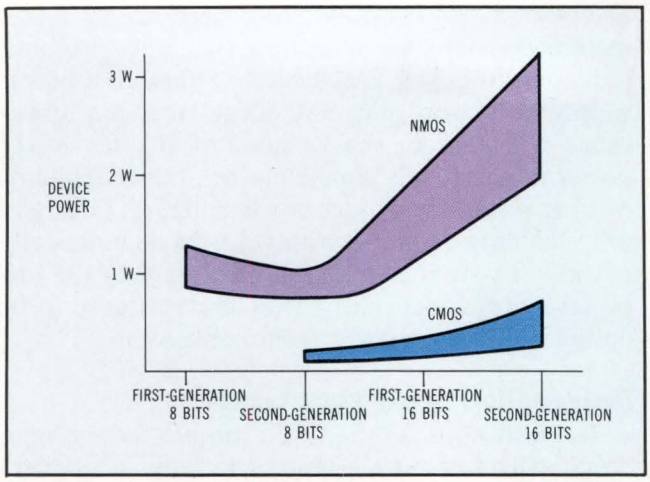


Fig 1 As shown, the power dissipation of complex 16-bit NMOS microprocessors is reaching a limit. This is causing a move to CMOS.

Although there is a rise in overall semiconductor cost from 26 to 33 percent, the 15-percent cost reduction in power supplies and the 11-percent reduction in cooling costs result in an overall system cost reduction of 19 percent. Designing for low system power also allows products to have value added features: portability, battery operation, desirable ergonomic features (eg, quiet operation, reduced maintenance, and greater in-field reliability). All of these features make premium system pricing possible.

One reduction leads to another in CMOS design. This is especially true when system concepts begin with the idea of low power system development completely done in CMOS.

Circuit design to minimize power

Many CMOS microprocessors have design features that can be used to enhance low power operation. Static circuit design, input termination circuits, and power-down capabilities significantly reduce the operating and standby power requirements of CMOS microprocessor systems.

Several CMOS microprocessor features offer significant advantages in power savings if properly used in system designs. Software and hardware

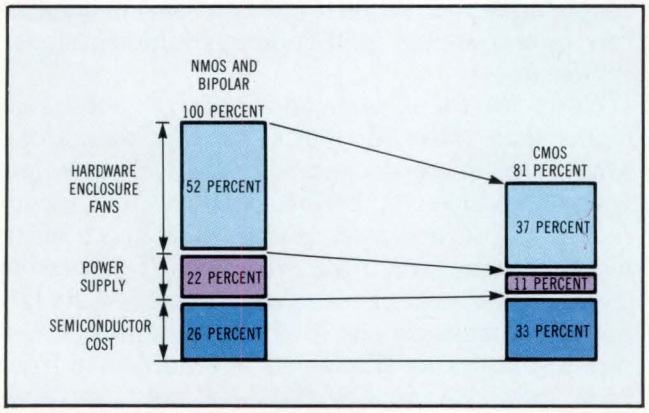


Fig 2 Despite higher semiconductor costs, CMOS reduces overall system costs by decreasing both cooling and power supply equipment.

power-down capabilities allow manipulation of system frequency for absolute control of system power. This type of control is not possible, however, unless the CPU is static in design. Therefore, static design is critical. Finally, floating inputs, which can severely impact power requirements, are important in designing absolute low power systems.

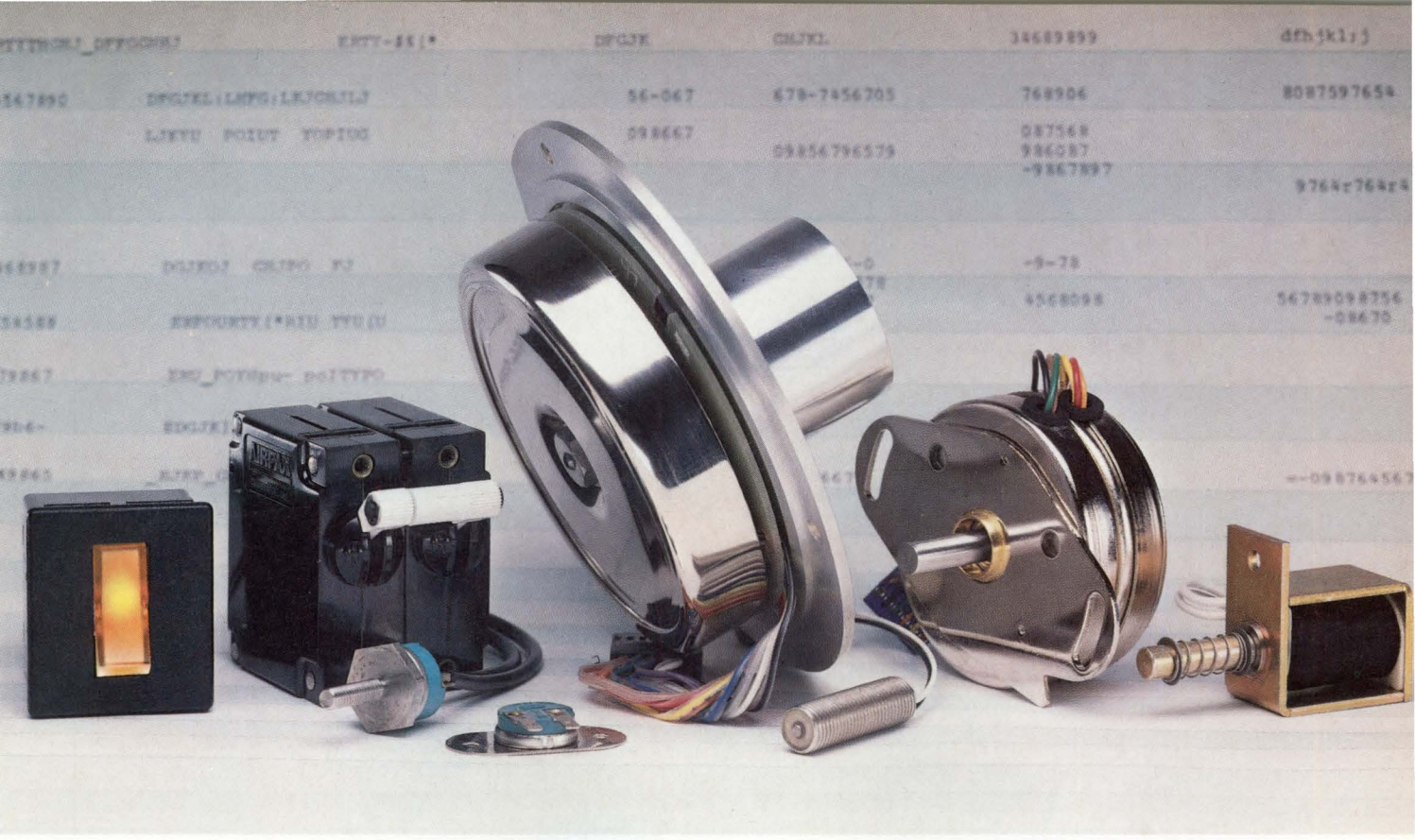
A CMOS 80C86 system shows the advantages of CMOS and the circuit design techniques necessary for optimizing the low power and high performance benefits of CMOS. This prototype system (Fig 3) is developed to show the effect that high speed CMOS can have on system power and performance. The key features of the prototype all-CMOS system include a CMOS 80C86 static 16-bit microprocessor, completely static design with a dc to 5-MHz operation, and a parallel interface using the 82C55A programmable peripheral interface. The serial port for terminal interface uses an HD-6406 universal asynchronous receiver/transmitter/bit-rate generator (UART/BRG) and the local area network (LAN) (1-Mbaud data rate) uses an 82C52 UART/BRG and HD-6409 Manchester encoder/decoder. The 82C59A interrupt controller provides eight-level interrupt capability, while the 82C54 interval timer supplies the three independent timers. The 44 Kbytes of CMOS memory are made up of 36 Kbytes of static CMOS RAM (an HM-6516 2-K x 8 CMOS RAM and an HM-92560 CMOS RAM module) and 8 Kbytes of CMOS fuse-link PROM (HM-6616 synchronous PROM).

The power comparison chart (see the Table) details the current requirements for the CMOS 80C86 system and its NMOS/bipolar equivalents. These numbers are worst-case operating currents seen over the full operating temperature device range. There is a 90-percent decrease in power when doing a straight replacement of NMOS/bipolar with CMOS. An even greater savings can occur when CMOS design techniques are used to their full advantage.

The CMOS system discussed here (Fig 3) has a room temperature of 25 °C, typical current of 95 mA, and has been powered by four AA batteries for more than 10 hours. System-clock frequency is 5 MHz and the system regularly transmits message information to a terminal during this period. Power supply current figures are for 25 °C, 5-V operation.

Hardware power-down capability is added at two levels: stop-clock and stop-oscillator. By stopping the clock to the CPU, 95 percent of the devices are put into a standby mode. The 82C84A clock generator continues to run and provides a clock to the HD-6406 in order to receive incoming serial data and to the 82C54 in order to continue any ongoing timing functions.

When the clock to the 80C86 is stopped, the system power supply current drops from 95 mA (full operation) to approximately 30 mA. Execution of software begins again immediately after the control line for stop-clock operation becomes inactive.



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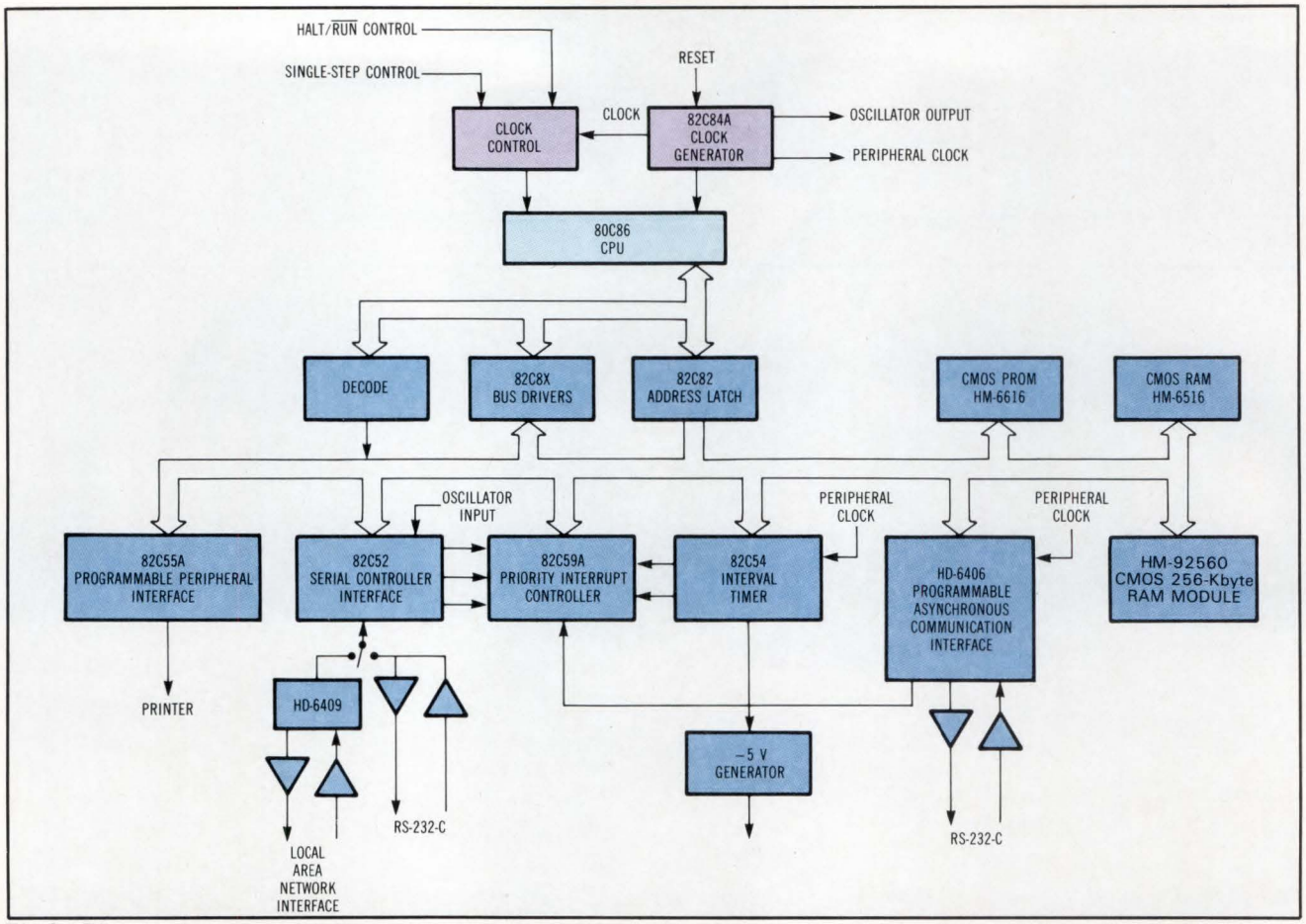

Fig 3 The CPU input board built around the 80C86 processor chip shows a CMOS approach to building a 16-bit processor. This prototype system also features a completely static design and a parallel interface using the 82C55A programmable peripheral interface.

Stopping the 82C84A oscillator results in an even greater power reduction with the system power supply current (I_{CC}) falling to less than 2 mA. This standby current includes a bias current for a negative voltage generator in the system for the RS-232 interface. Actual CMOS system standby current is less than 1 mA for room temperature (25 °C) typical operation.

Using the Harris 80C86 CMOS 5-MHz, 16-bit CPU, along with CMOS peripheral and memory products, this design operates at less than 100 mA (5 V, 25 °C). This power reduction of over 95 percent, when compared to the equivalent NMOS/bipolar system, is achieved with no sacrifice in performance. In addition, trade-offs that will minimize power dissipation can occur in a CMOS system. Evaluation of speed/power requirements for a system should take place early in a project so that long term power goals can be met.

One of the biggest advantages of CMOS microprocessor systems is the ability to stop circuit operation, either through a software command or hardware control. Two types of software power-down functions are now in use. The first type stops only the clock to the internal registers and CPU logic. This will result in approximately 50- to 70-percent power savings for the CPU and the clock driver circuit. This type of software power-down capability is available on the NSC800.

Stopping only the clock to internal circuitry allows an immediate restart from the power-down situation. Since the oscillator is left running, there is no

Worst-case Power Comparisons between CMOS and NMOS/Bipolar

PART TYPE	CMOS I_{CC}*	NMOS I_{CC}*	
80C86	50 mA	340 mA	5-MHz operating frequency
82C52	16 mA	120 mA	for NMOS 8251 current and BRG current
82C54	10 mA	140 mA	at 8-MHz count frequency on all timers
82C55A	1 mA	120 mA	—
82C59A	1 mA	85 mA	—
82C8X	14 mA	1120 mA	Seven 82C8x latches and transceivers
82C84A	25 mA	162 mA	15-MHz crystal frequency (5-MHz system)
PROM	60 mA	250 mA	8 Kbytes of PROM
RAM	110 mA	770 mA	44 Kbytes of RAM
	287 mA	3107 mA	

*Specification maximums over full temperature and voltage ranges, where available. Worst-case estimates are used in other cases.

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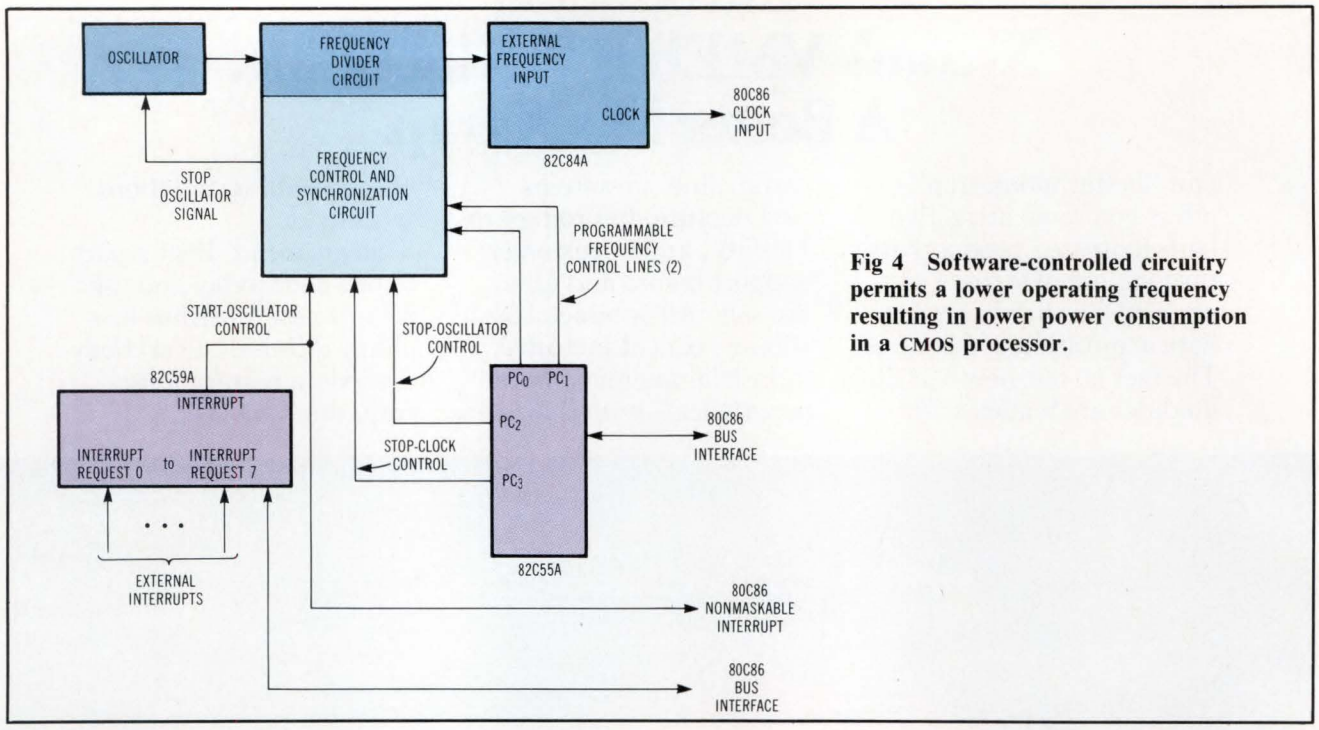

Fig 4 Software-controlled circuitry permits a lower operating frequency resulting in lower power consumption in a CMOS processor.

oscillator startup time needed. Because of the continuing oscillator operation, however, the CPU and associated clock circuit, whether internal or external, will still dissipate power. In addition, the 30 to 50 percent of the original power required is in the 10- to 45-mA range.

A second option is becoming popular on some single-chip processors. This power-down command stops the oscillator and brings the entire system power down to the standby levels. All clocks and oscillators are stopped and the entire system is put into a standby or quiescent state. Standby current totals for all-CMOS systems can be in the range of 1 to 3 mA, depending on system size and complexity. The 146805 single-chip microcomputer from Motorola has this power-down command. This can be accomplished on existing general-purpose, static CMOS microprocessors (including the 80C86) with the use of external circuitry.

Surveying static operation

All devices in the 80C86 family are designed with fully static circuitry. This allows device operation from dc to the individual maximum rated frequencies. Since operating power is critical in low power applications, this parameter can be controlled by the user, based upon system operating frequencies. CMOS operating power is directly related to frequency; the lower the frequency, the lower the operating power dissipation. At a dc frequency, device standby currents are typically less than 10 μA.

Under normal, full-power operating conditions, an 80C86 system runs at a standard 5-MHz operating frequency and keeps full operating power to a minimum. If, however, the microsystem power fails independently of the main power, operation can be maintained. With a backup battery power supply, the system can transfer from main power operation to battery supply. With system power levels approximately 10 percent that of equivalent NMOS/bipolar circuits, full 5-MHz operation is still possible.

A major advantage of CMOS micro systems is the ability to stop circuit operation via a software command or hardware control.

As primary power is diminished (battery discharging) or removed (power interruption or battery-backup operation) in portable or remote battery-powered applications, the need to run at a lower frequency to conserve power may become important. Operating power is critical in low power applications and CMOS operating power is directly related to frequency. With the static design of the 80C86 family, power requirements can be controlled by the user; reduced operating frequency lowers power. Static design allows this reduced operating frequency without the fear of causing data loss or invalid operation.

One method of low frequency operation is shown in Fig 4. The system clock is divided by software-controlled external circuitry to provide a lower operating frequency—eg, 100 kHz. The system power consumption is significantly reduced while complete computational powers remain available. The low frequency mode of operation is unavailable with some CMOS microprocessors and most NMOS processors, including the NMOS 8086. Dynamic register designs in the nonstatic CPUs need to be refreshed at a minimum rate and do not allow very low operating frequencies or stopped-clock standby operation.

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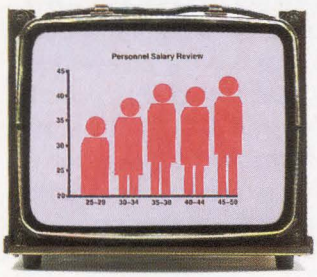

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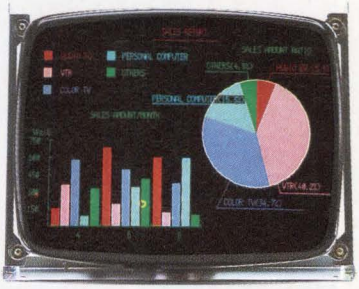

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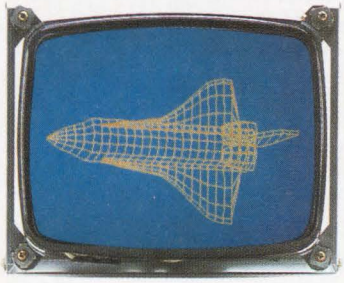

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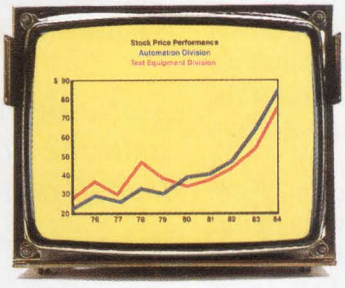

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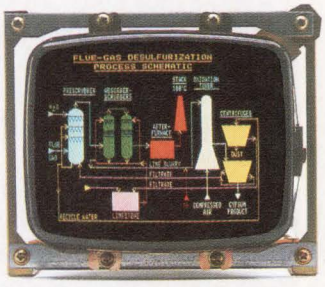

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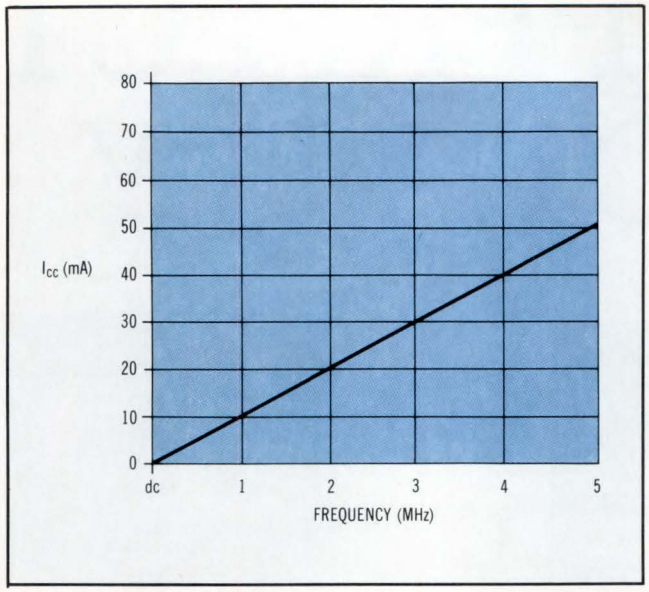

Fig 5 Power supply current of the 80C86 (and other CMOS micros) is linearly related to the operating frequency.

Worst-case operating current for the 80C86 CPU at 5 MHz is 50 mA, derated linearly as frequency is reduced (Fig 5). This means that the operating power supply current for the 80C86 CPU is approximately 1 mA at 100 kHz. Similar deratings are valid for the power dissipations of the peripheral, support, and memory circuits.

Finally, given a power critical situation where power is diminished to the point where even continuous, low frequency operation is not desirable, the 80C86 static internal circuits allow the clock to be stopped. This eliminates the power dissipation associated with switching and reduces device currents to standby levels. At standby, individual 80C86 peripheral device currents are guaranteed to be less than 10 μA with the 80C86 CPU less than 500 μA.

In order to meet minimum 80C86 clock timing requirements, the clock frequency reduction must be timed properly. Therefore, synchronization is required between the system clock and the low frequency/stop-clock control signals. Cases of asynchronous timing errors caused by irregular clocks outside the CPU specification limits must be avoided. Additional circuitry allows control of this power-down mode using a bit from the 82C55A for stopping the clock. The output from the 82C59A priority interrupt controller is used to restart the clock to the CPU upon demand from an external source.

Another advantage to static design is the ability to stop and single step the system clock during system prototyping. This valuable method of debug allows the designer to inspect the system bus and look at specific operations in the system. The realtime complications of 5/8-MHz bus transfers are eliminated and system debug is significantly simpler.

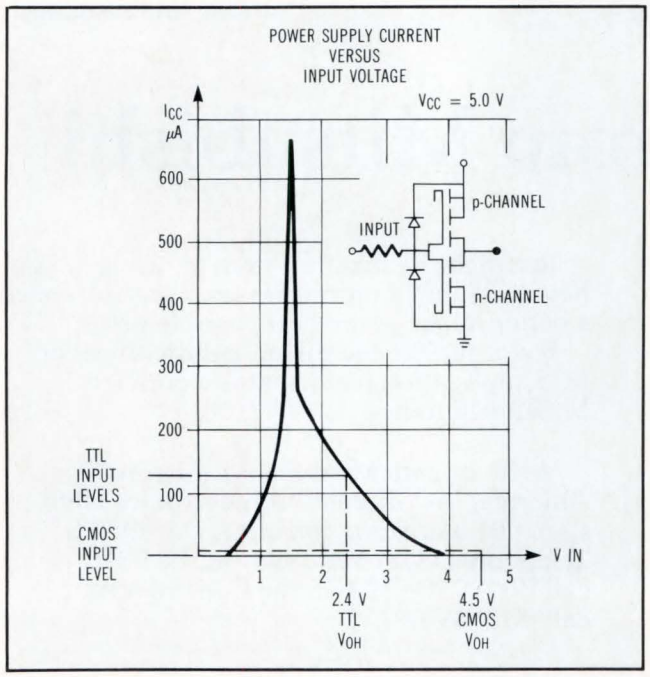

Fig 6 CMOS input circuit transfer characteristics show the danger of allowing the input voltage to float within the active region of the device. The floating inputs will settle at the threshold voltage where current flow is greatest. Consequently, unused inputs must be tied to either V_{CC} or ground.

Static design debug eliminates the realtime complications of 5/8-MHz bus transfers and simplifies system debug.

Undefined input voltage levels are forbidden in CMOS system design. Undefined input states allow the input circuitry to "float" within the active device region. Unfortunately, floating CMOS inputs tend to settle at the threshold voltage, where current flow is the greatest. This will increase I_{CC} in most CMOS devices and can thus cause irregular or incorrect operation.

Fig 6 shows the CMOS input circuit transfer characteristic. As input voltage moves away from either power supply rail, both the n-channel and p-channel are turned on and current increases. Therefore, all CMOS inputs, if unused, must be tied to V_{CC} or ground by one means or another. This will avoid high I_{CC} conditions and oscillation.

If non-CMOS input voltages exist in a mixed technology system (TTL, NMOS, etc), system power can be increased again. Since these other technologies can have less than ideal output voltages, both the p-channel and n-channel input transistors can operate in their linear region. This defeats the complementary function of CMOS, which yields its low power.

Pull-up/pull-down resistors offer the most common method of defining CMOS inputs when no driving source is present. This technique has several disadvantages. First, additional components (resistors) that increase production costs and board real estate are necessary. Second, more power dissipation

can actually occur when using pull-up/pull-down resistors. Since the driving output must supply extra current when switched to the opposite state of the pull-up/pull-down resistor, a significant increase over normal CMOS leakage currents can occur.

The role of bus-hold circuitry

To eliminate external resistors along with the high power effects of "floating" inputs, the 80C86 CPU uses onchip "bus-hold" circuitry to provide valid input voltages when there is no driving source (ie, a no-connect or a driving input that goes to a high impedance state). The bus-hold circuits maintain these pins, internally and externally, as the last valid logic level until they are overdriven by another source. A driver must supply 400 μA of sink or source current at valid input voltage levels to overdrive the bus-hold circuits. Since this circuitry is active, and not a passive resistive-type element, 80C86 standby current is kept to a minimum.

System needs and overall compatibility dictate the placing of bus-hold circuits on the CPU. The 80C86 CPU has bus-hold devices on selected pins (AD0 to AD15, A_X/S_X, S0 to S3, and control lines on pins 29 to 32 and 34) that are common to the local bus. This eliminates the summing of overdrive current, which would occur if all 80C86 family members had bus-hold circuits on common pins.

The 82C82/83/86/87 octal latches and transceivers have specialized input circuits that minimize I_{CC} transients occurring due to switching and undefined inputs. These circuits also help eliminate the need for external resistors. Inputs are gated off on the 82C82 by the falling edge of the strobe input, while input inverters are isolated from V_{CC} by turning off the upper p-channel and lower n-channel. Thus, there is no current path, other than leakage, between V_{CC} and ground during input transitions once data is latched into the 82C82. Internal circuitry is also isolated by gated inputs. Invalid logic states from floating inputs will not be transmitted to succeeding stages when the inputs are gated off. Pull-up resistors can be removed.

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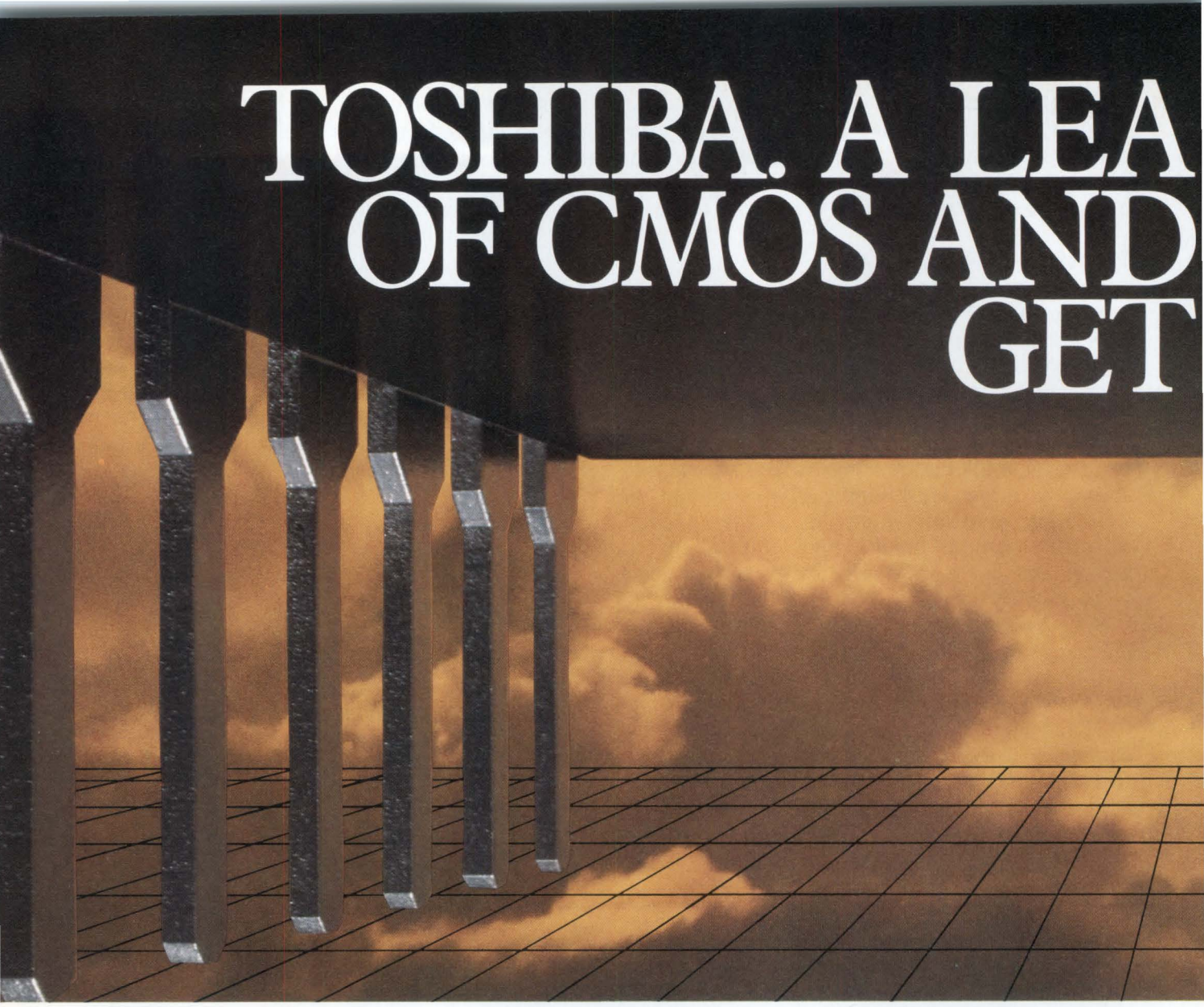

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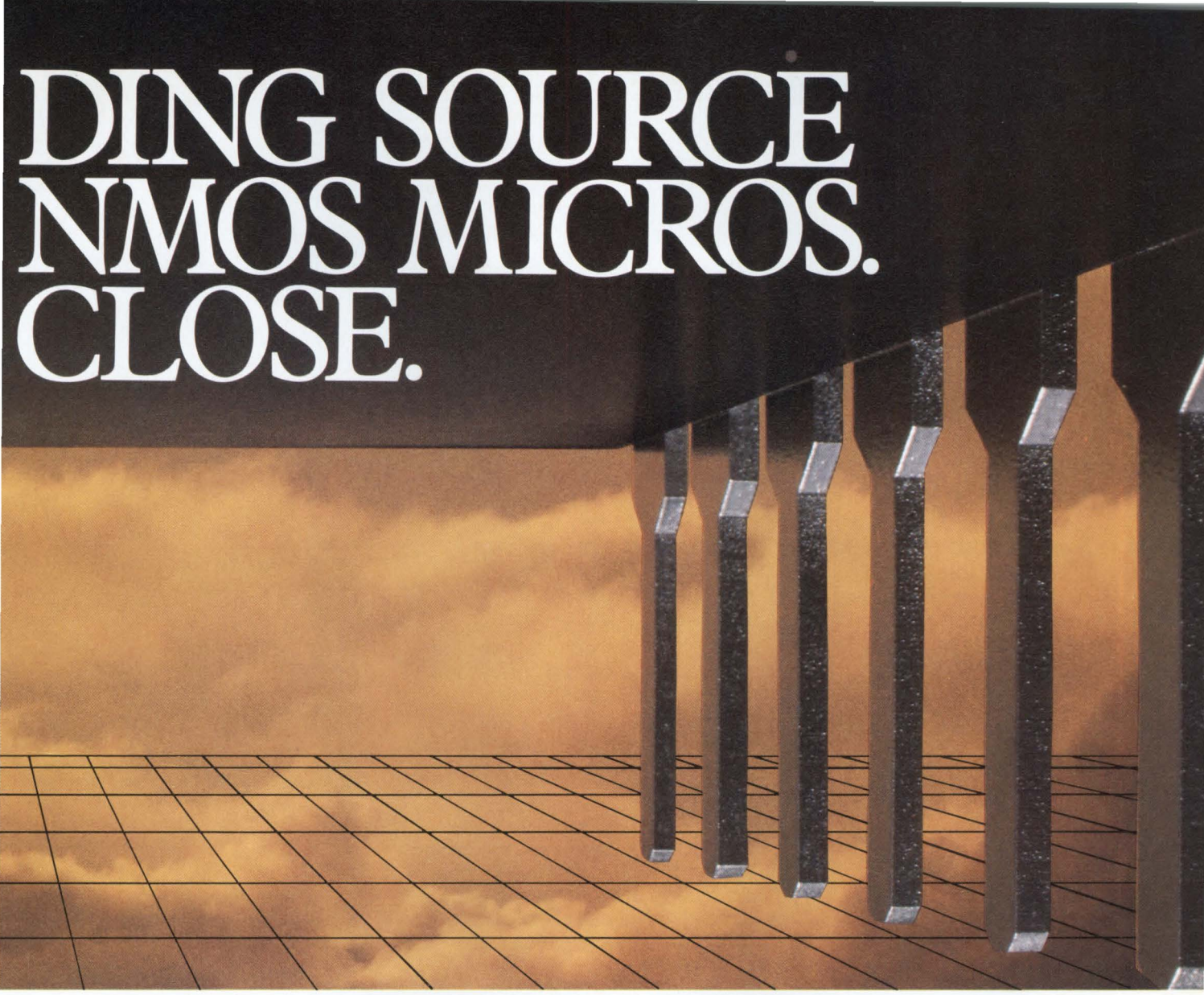

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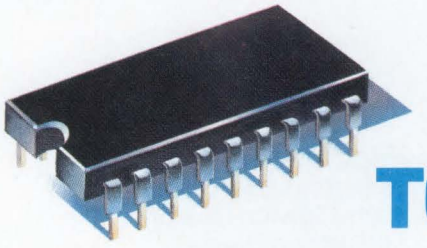

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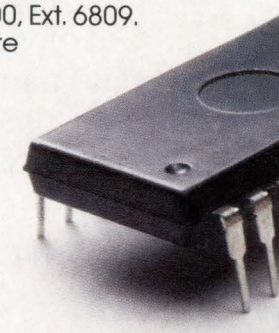

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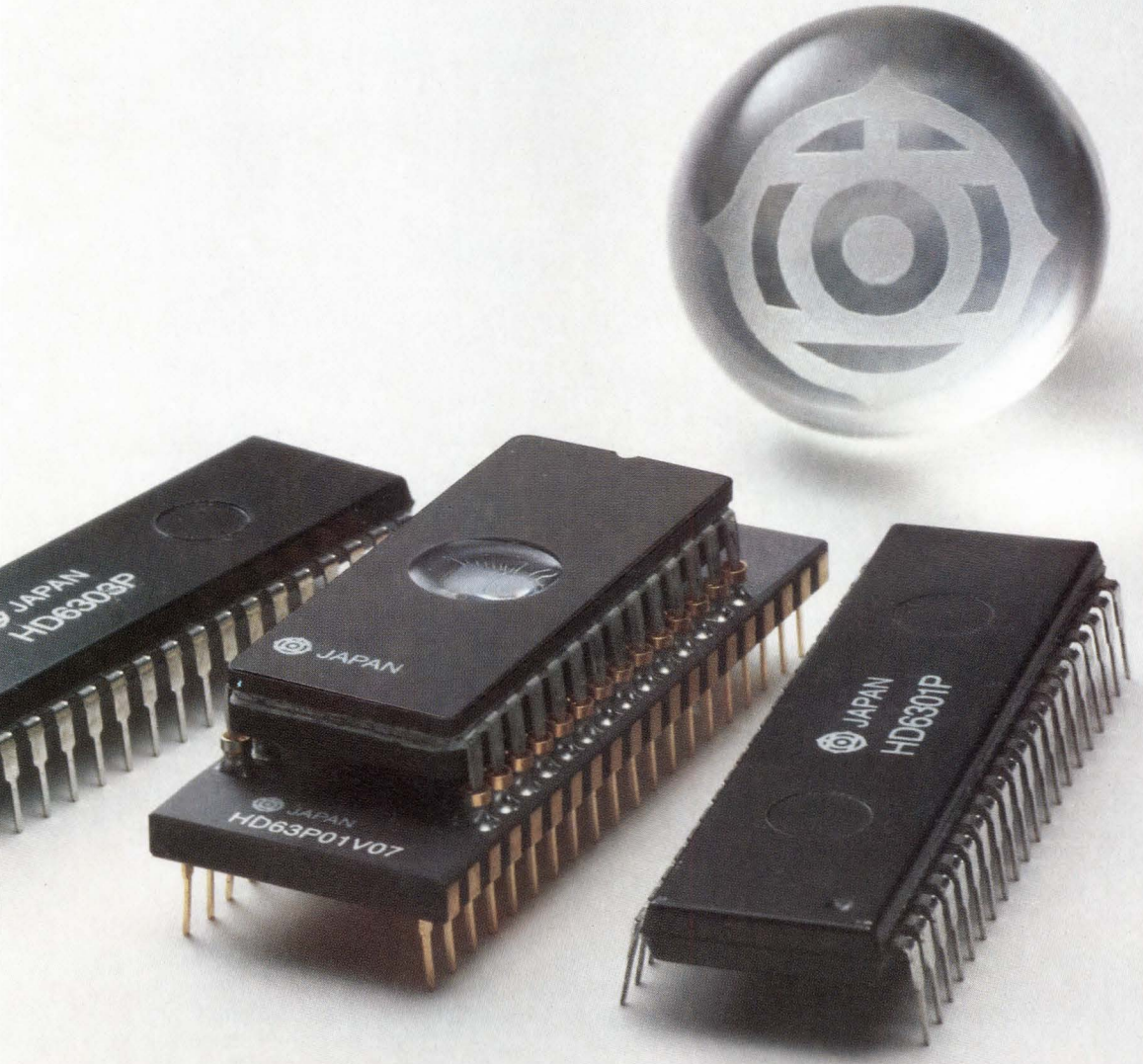

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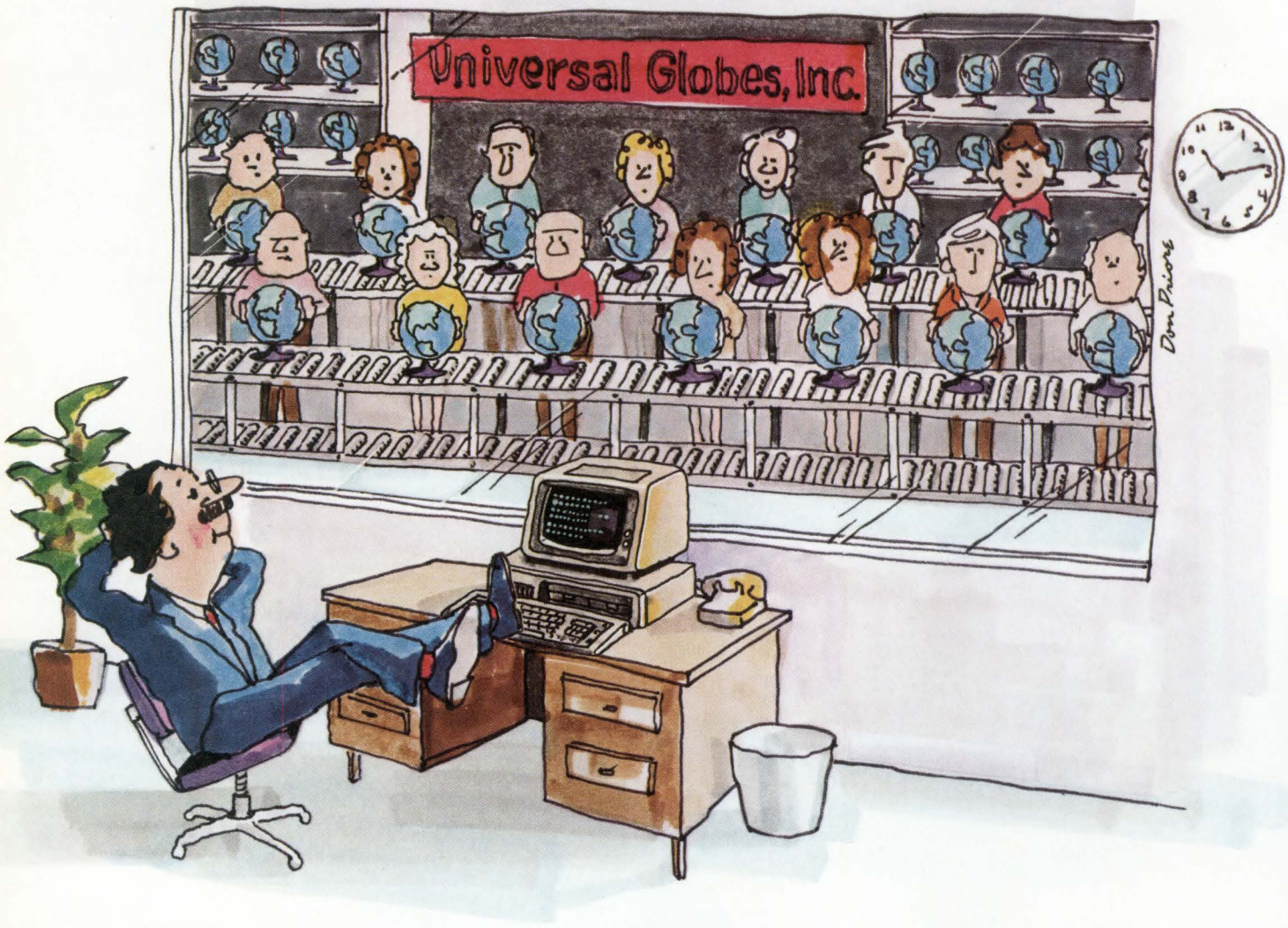

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CIRCLE 86

HOW TO PORT UNIX TO A NEW MICROPROCESSOR

CPU architecture has a significant effect on the process. Compromises must be made between the capabilities of the chip and the purity of Unix.

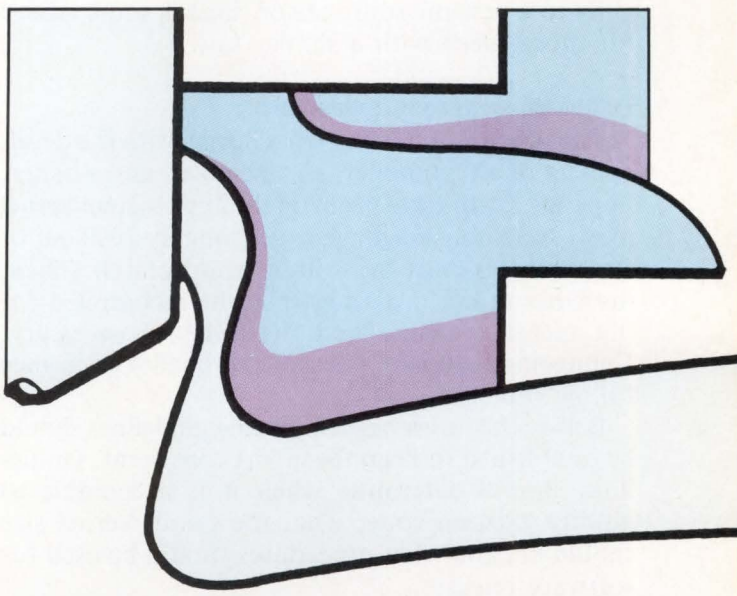
by Nai-Ting Hsu, Glenn Skinner, and Jay Zelitzky

Without a doubt, Unix is moving out of the laboratory and university and into the commercial marketplace. During this year, the availability of Unix System V on the National Semiconductor 16032, Motorola 68000, Intel 286, and Zilog Z8000 microprocessors will help bring Unix solidly into the world of microcomputers. Small microprocessor-based machines running Unix will be able to provide many of the powerful functions of larger computer systems, but at a lower cost.

Nai-Ting Hsu is currently senior engineering manager at National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. He holds an MS and a PhD in computer science from the University of Wisconsin—Madison.

Glenn Skinner is engineering section head at National Semiconductor Corp. He holds a BA and an MS from Cornell University.

Jay Zelitzky is a systems programmer at National Semiconductor Corp. He has a BA in computer science from the University of California at Santa Cruz.



From a microprocessor manufacturer's standpoint, the task of taking existing, working Unix code and moving it to a new machine is not as difficult as starting from scratch with a proprietary operating system. Nor does it require as much manpower. Moving Unix to one of these advanced microprocessors, although easier than starting from scratch, can still be a challenging task. At National Semiconductor, the Berkeley 4.1 BSD version of Unix is ported to the NS16032. This product is called Genix.

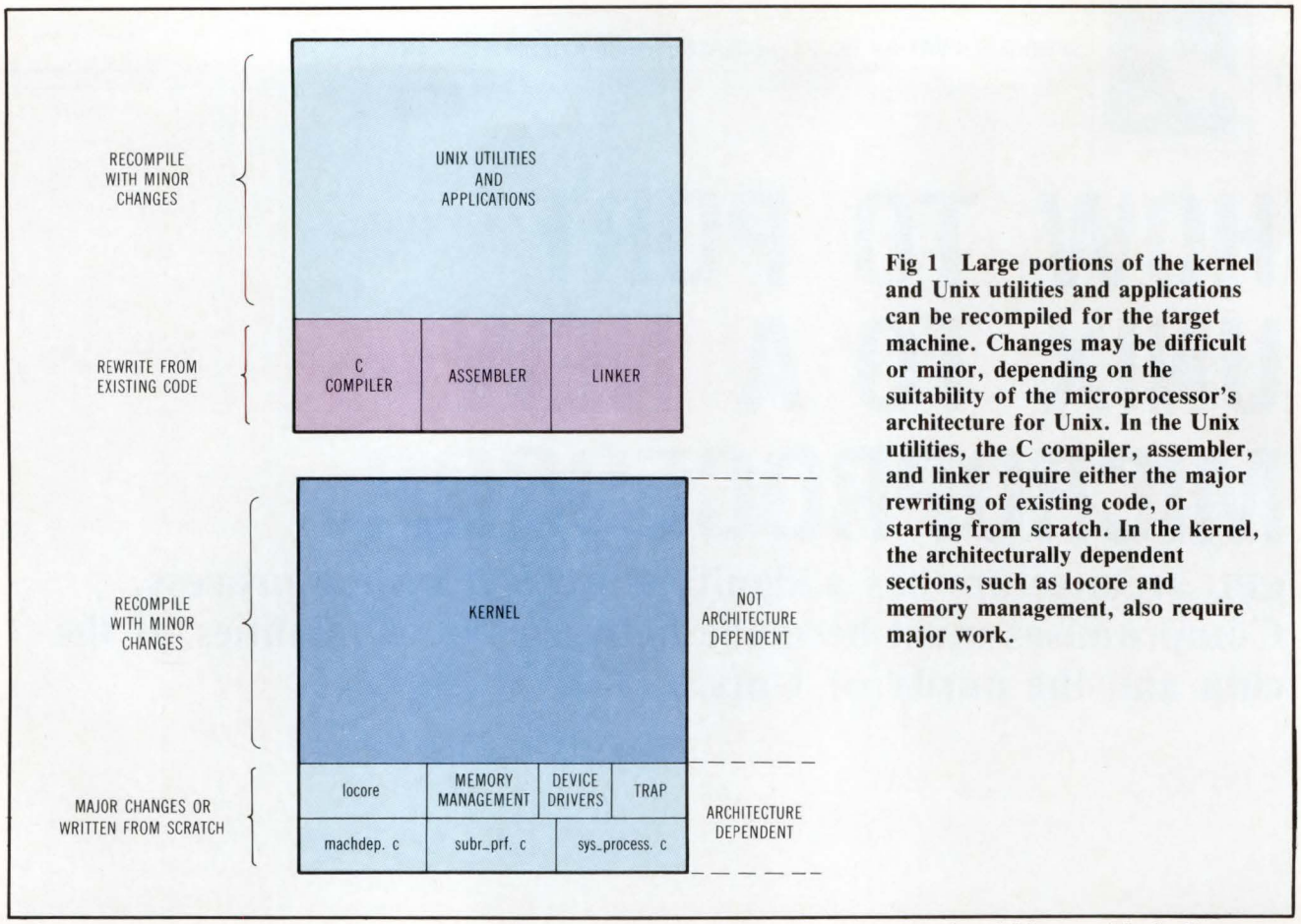


Fig 1 Large portions of the kernel and Unix utilities and applications can be recompiled for the target machine. Changes may be difficult or minor, depending on the suitability of the microprocessor's architecture for Unix. In the Unix utilities, the C compiler, assembler, and linker require either the major rewriting of existing code, or starting from scratch. In the kernel, the architecturally dependent sections, such as locore and memory management, also require major work.

With the experience of having successfully moved Unix to a new microprocessor, here is some advice for those faced with a similar task.

Establishing porting guidelines

The process of porting Unix begins with the development of a C compiler, an assembler, and a linker. In parallel, work can begin on the Unix system kernel itself. Assembly language code (roughly 2000 out of 40,000 lines) must be written from scratch. Then, the Unix utility programs must be recompiled for the target machine and modified if necessary. Debugging, software release, and quality assurance follow (Fig 1).

Before this work begins, porting guidelines should be established to keep the effort consistent. Guidelines should determine when it is acceptable to modify existing code, what the target kernel size should be, and what procedures should be used for software releases.

Depending on the needs of the porting team, the Unix porting process can bring competing goals face to face. On the one hand, because a new chip offers a range of features and capabilities, the operating system could be made to exploit these features, whether or not it was designed to do so. For example, if a microprocessor offers demand-paged virtual memory, users should be able to take advantage of it. On the other hand, changes in the operating system that would affect the compatibility of application programs should be avoided. Compromises must be made.

Other porting teams may want their porting goals to include minimum changes in the existing code. If time is extremely short, this may be the best choice. National Semiconductor's accomplished goals allow existing code to be changed when chip features could be exploited. This is done while keeping the modifications inextensive and maintaining the basic Unix structure.

Regarding the kernel itself, keeping a microprocessor-based operating system as small and clean as possible ensures low overhead. To improve the system's efficiency, avoid introducing new bugs or unnecessary complications, and find and fix old bugs in existing code. Finally, adhering to a structured design approach will result in a finished product that is easy to understand and maintain.

Quality is a big issue in American industry, in software as well as in other products. In an effort as large as porting Unix to a new microprocessor, it is essential to build in quality from the beginning of the project. Software quality-assurance personnel should be involved from the earliest stages of the project to ensure that proper equipment and software are available when it comes time to test the system. Software modules should be coordinated while they are in the development process to maintain consistency between modules. Engineering managers should plan revision control.

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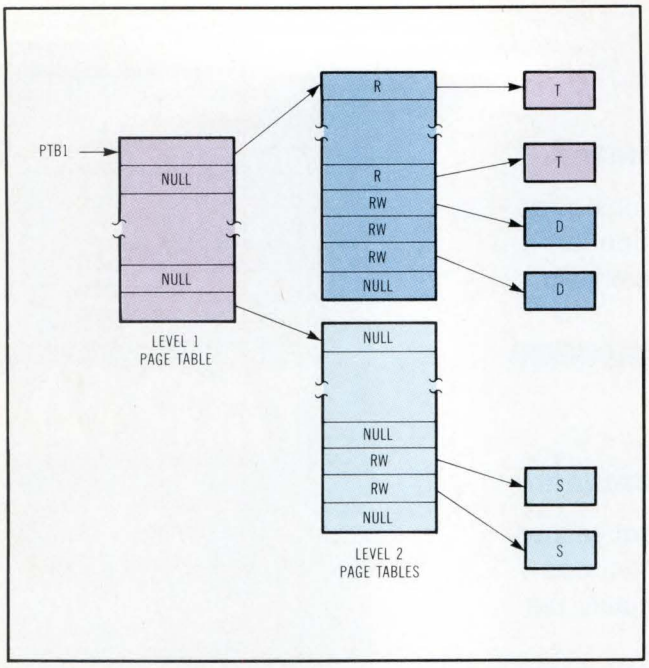

Fig 2 This user process map shows that in the NS16000 memory management scheme, the first-level page table entries point to second-level page table entries, which in turn point to the text (T), data (D), or stack (S) areas. Protection is provided in hardware. Text is read only (R), data is read/write (RW), and the stack is read/write.

In the case discussed here, the final software release is automated. The software recompiles the source code, loads it onto the SYS16 development system, and instructs the development system to perform a certain set of tests on the code. This minimizes human intervention in the release process.

Written in the high level C language, Unix is a highly portable operating system. It is not, however, entirely machine independent. Early in the porting effort, team personnel should (if they have not done so already) learn the requirements of the operating system, the architecture of the machine that the software is being ported from, and the capabilities of the target microprocessor. The porting effort's degree of difficulty is governed by how well the microprocessor's architecture can provide the features needed by the operating system.

Microprocessor architecture affects Unix port

Unix was not designed to accommodate a segmented architecture such as that of the 286, although it is a useful feature for some other operating systems. Rather, at the root of Unix structure is the need for a uniform, linear address space that can be divided into three regions: the text area, data area, and stack area (Fig 2). Unix assumes that, for an executing process, the lower section of the address space will contain the text, the data will follow the text, and the stack will begin at the highest address and grow downward. Since segmented architectures do not support this kind of layout, Unix will run on them only after considerable programming effort. However, because the NS16032 has a uniform, 16-Mbyte address space, none of this was a problem.

For a single-user target system, virtual memory is not an issue. If the target microprocessor is intended to function in a multitasking environment, accomplishing virtual memory management can be a major benefit. As a multitasking operating system, Unix context switches between processes, diverting the CPU's attention from one to the other. Whenever the context is switched, the map for the old process must be saved and the virtual memory map for the current processes must be established. The means of mapping a process's virtual addresses to physical addresses is highly dependent on the available memory management architecture. The microprocessor should also provide protection. Thus, this architecture determines the success of the multitasking scheme.

Once the porting effort guidelines are established, the next key decision is choosing which C compiler to port. Ideally, the compiler should be highly reliable, with as few bugs as possible. In addition, consider the compiler's ability to produce compact code. The Berkeley 4.1 BSD portable C compiler was chosen, for example, because it was a well-debugged compiler that had been used extensively in the field.

A compiler goal should be adopted before porting is begun. The program aim (once a reliable, efficient compiler is chosen) should be to use as much existing code as possible and change only those elements that are directly affected by the microprocessor architecture. With minor revisions, this can shorten both development and debugging time. Attempts to optimize compiler performance should be done carefully. Be aware of what changes in the compiler can improve performance considerably, and what changes would result in little improvement. Consider debugging time when deciding on changes.

Once the porting effort guidelines are established, the next key decision is choosing which C compiler to port.

The target microprocessor's architecture affects how easily the C compiler can be ported. Because the NS16032 has a regular instruction set, it allows the use of any instruction on any register and in any addressing mode. With other microprocessors, there can be odd registers for special purposes, various rules for different instructions, and exceptions to the exceptions. These exceptions make the resulting code difficult to read, optimize, and debug. Programmers porting the compiler should always keep these exceptions in mind.

Assembler choice is a big decision and one that is not easily reversed. Before trying to develop an assembler, find out if there are already assemblers

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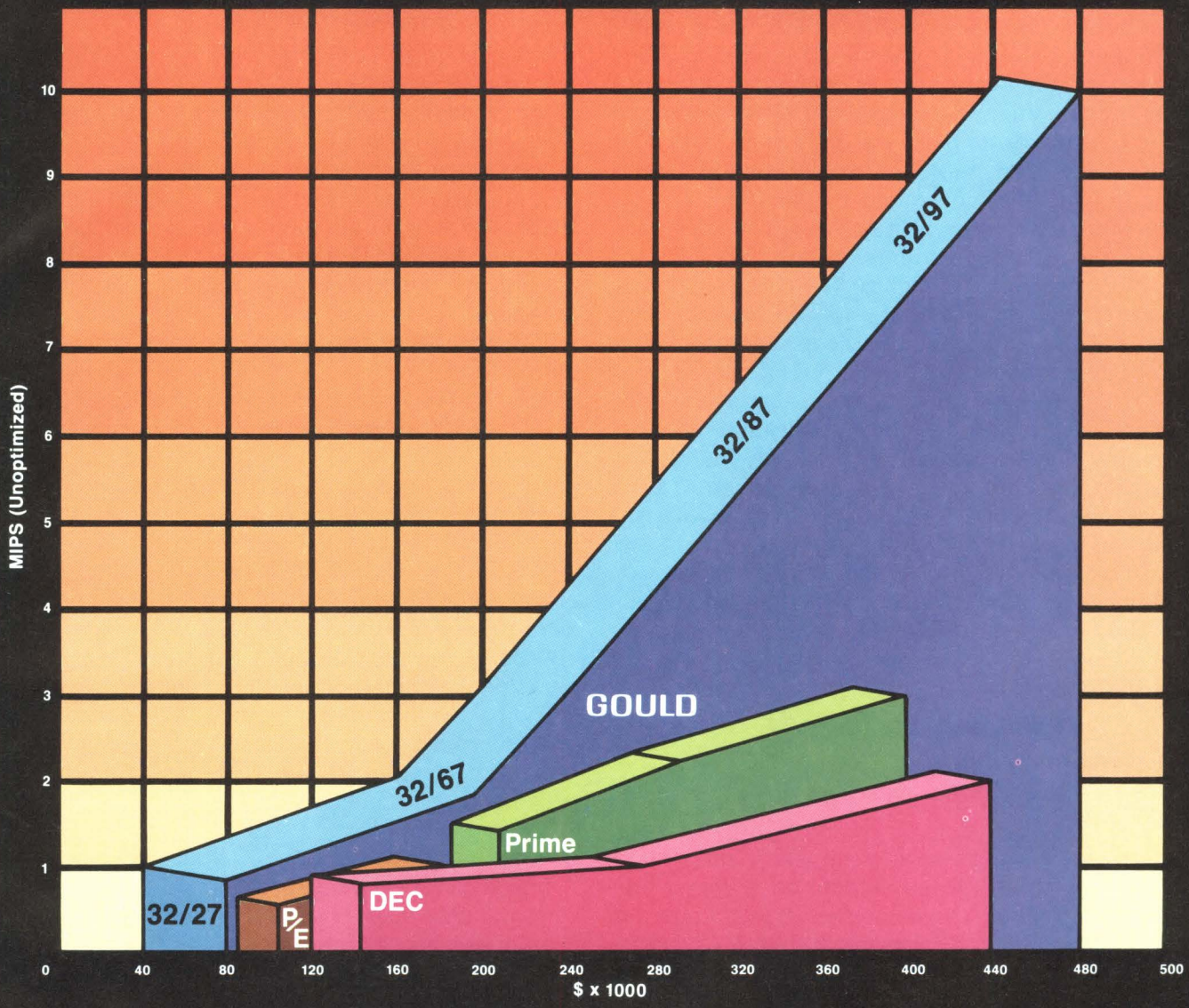

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available for the CPU that could be suitable for use with Unix. If none are available, consider moving an assembler from a different CPU. Compare these options to the effort involved in writing an assembler from scratch.

Pointer and integer sizes

Machine architecture affects the kinds of applications that a compiler can support. Although Unix ran originally on 16-bit machines, the restrictions imposed by this architecture limited the power and size of application programs that they could run. Just as the 32-bit VAX architecture supports applications that are too limited by the 16-bit PDP-11, microprocessors (eg, the NS16032) can handle larger, more complex applications.

Microprocessor architecture affects pointers, pointer sizes, and integer sizes. To support the C language, a CPU should be able to support pointers and integers that are the same size. If it cannot, many programs will be difficult to port to the new system. Moreover, it will sacrifice application software compatibility because most C programs mix pointers and integers. Some microprocessor manufacturers have tried to get around this problem by offering various versions of their C compiler, each with a different combination of pointer and integer sizes. Users have to hunt for compilers that will be compatible with their existing software.

Before trying to develop an assembler, find out if there are already assemblers available for the CPU that could be suitable for use with Unix.

Preferably, a CPU should support 32-bit pointers and integers in order to accommodate larger programs. No system could hope to support a program as large as a fully implemented version of "vi"—the most popular Unix text editor—without 32-bit pointers and integers, for example. Trying to support 32-bit integers and pointers when the CPU's natural pointer size is less than 32 bits, will result in having to pay the associated overhead costs. With an Intel 8086, 8088, or 286, several additional instructions must be included for every 32-bit pointer manipulation done within a program. Microprocessors such as the NS16032 have natural pointer and integer sizes of 32 bits.

Demand-paged virtual memory management is not essential but is very desirable for a multi-user Unix system. Conventional swapping suffices for some applications, but if users are running large programs, the system can end up spending most of its time swapping processes at context switching.

Even the VAX architecture (from which Berkeley 4.1 BSD was ported) has memory management restrictions. The page tables that contain the map between virtual and physical memory are a fixed size, must reside in main memory, and must be located in contiguous memory locations. Transferring the 4.1 BSD memory management scheme would have been easier than writing code from scratch, but the resulting Unix kernel could not have taken advantage of the microprocessor's advanced memory management features.

Variable page table sizes, and provisions for second-level page tables to page out to memory, allow the whole 16-Mbyte address range to be used. Thus, a user program could conceivably fill the entire process space. Writing general virtual memory subroutines treats the kernel as just another address space, allowing certain pieces of the kernel itself to page out. A kernel that can page pieces of itself out to disk is convenient for running very large programs.

There are also a few added features not included on the 4.1 BSD version. A VSPY function allows the kernel to point a virtual address space at a particular physical address space. VLOCK locks memory into place so that programs can execute DMA into user memory. VMAP copies pages from one address space into another, allowing the PS and W programs to obtain the command arguments for any process easily.

This version of the Unix kernel's virtual memory management is not necessarily better than 4.1 BSD in all respects. For instance, 4.1 BSD includes some more efficient routines for swapping. Instead of swapping one page at a time, for example, it can swap 50 pages at a time. To keep paging as general as possible, it pages when necessary, but uses a read-ahead paging optimization routine to collect paging requests and perform them in bunches.

Debugging the chip set

Initially, every new microprocessor and its support chips will have bugs, regardless of the manufacturer. Waiting for another group to debug the chips and fix them would mean that a software team will have less trouble porting Unix or any other software to the chip. But by that time, the competition will be miles ahead. A better approach to developing software of any type for a new chip is to plan the effort to work with prototype hardware, thereby isolating hardware bugs from software bugs. Often, this means building software from a simple skeleton and substantiating it as bugs are found and fixed.

Developing the memory management section of the Genix kernel began by debugging the NS16032 CPU. Initially, the NS16032 main memory unit (MMU) was unavailable. Consequently, the kernel and a user process had to share the same address space, with the user process residing above the kernel. Because the CPU's modular table is limited to the first 64 Kbytes of the address space, a stripped-down kernel was built to fit into 56 Kbytes, reserving some of the modular table entries for the user process.

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Context switching was performed by moving all memory above the kernel to or from the swap space.

Next, MMU bugs were isolated by using the MMU chip with the CPU in a limited way. A static page map mapped the user addresses one to one (ie, virtual address 10,000 was mapped directly to physical address 10,000). At the same time, access was disallowed to the kernel's memory. The MMU was instructed to translate only user mode references, so that kernel mode references still went straight to physical memory. Taking precautions against user programs or MMU bugs affecting the kernel itself resulted in the isolation of those MMU bugs that did exist.

Expanding the kernel

Virtual addresses were shifted so that programs began at zero, but remained mapped to one contiguous section of memory above the kernel. Once this scheme worked, the next step was to expand the kernel above 56 Kbytes and start to change it into the standard 4.1 BSD kernel. Once convinced that the MMU was translating reliably, it was tested in supervisor mode, again with a one-to-one static map. Finally, kernel mode translations were used to context switch the user area.

A rudimentary paging system kept a very simple free page list, searching for the first available memory page to swap out when memory was full. Second-level page tables were never swapped and texts could not be shared. Swapping was synchronous, so that the kernel did nothing else while I/O was in progress. There was no virtual memory scheduler, but the software could take page faults from user mode and handle them.

As the MMU bugs were found and fixed, features were added to the kernel to make it more efficient. Using the reference and modify bits, swapping second-level page tables, and implementing asynchronous paging resulted in demand loading of text segments and prepaging. Swapping parts of the kernel enabled page faults to be taken from kernel mode. In addition, a virtual memory scheduler was added to swap out whole processes.

During this development process, several large bugs were found. For some time, the reference and modified bits worked improperly. Moreover, the MMU instruction to read or write the user data space from the kernel did not work, so the copy in/copy out subroutines were used instead. Early on, there could be no page fault in the user text or the process would fail. Therefore, temporary code was added to the kernel that would lock user text into memory while context switching. Beginning with a simple kernel and adding features one at a time, these bugs could be identified as hardware (not software) problems and worked around.

In every kernel there is a section of code that is written in assembly language. On the VAX, this section, locore.s, consists of about 2000 lines. This particular section is not so much ported as it is rewritten from scratch. The first step is to understand precisely what the original code does. This requires expertise in the machine's assembly language from which Unix is ported. Next, code must be written in the target system's assembly language to duplicate the function of the original code.

Routines for other machine-dependent sections of Unix must also be developed in this manner, even if they are written in a high level language. The serial I/O drivers' code for the SYS16 system, for example, had to be written essentially from scratch. The serial I/O board resembled a hybrid between two DEC peripheral boards, therefore, very little of the original code for this routine remains.

Porting the Unix utilities can be easy if the target processor closely resembles the system from which Unix is ported. In this case, the NS16032 so closely resembled the VAX that porting the utility programs only meant recompiling existing VAX utilities with a compiler. A large fraction of the programs were ported with no modifications whatsoever (Fig 3).

Problems arise when the target architecture is dissimilar to that of the original machine. In the case of the 68000 processor, the integer formats differ from those used by the VAX. With integers, the VAX and 68000 store the bytes in the opposite order. However, 68000 character strings are stored in the same format as on the VAX. Consequently, programmers must know the actual layout of the data in question to switch sections where the formats must be reversed.

A good debugging environment helps a porting effort considerably. Unix is equipped with a standard

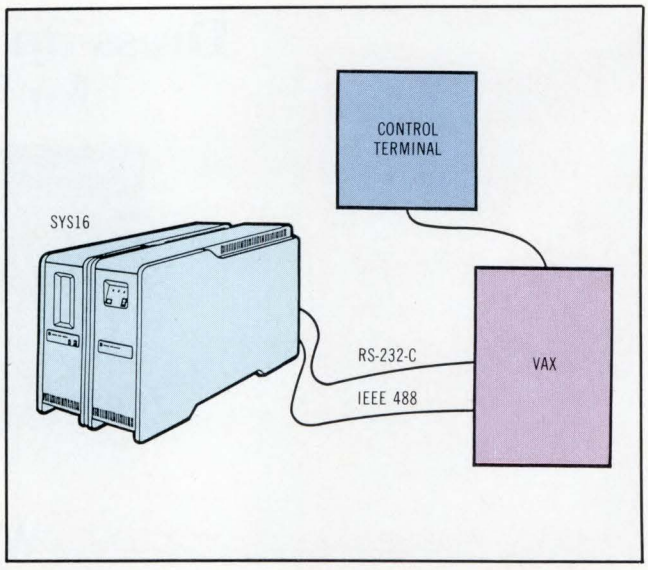

Fig 3 Developed on a VAX host, the Genix operating system is downline-loaded onto the NS16032-based SYS16 system. It accomplishes remote debugging by communication from a control terminal via the VAX and an RS-232-C line to a ROM monitor in the SYS16. The IEEE 488 bus provides fast file transfer.

source level debugger (SDB). The problem with SDB is that it contains quite a few bugs itself. Relying on it is risky. In addition, SDB can be utilized only to debug user programs under Unix and is useless for debugging a kernel. Consequently, instead of porting SDB to its system, the company developed its own debugging tools and had them ready at the time of the Unix port.

Porting the Unix utilities can be easy if the target processor closely resembles the system from which Unix is ported.

The company's debugger is structured in two pieces: one is a user interface and the other a ROM monitor. Resident on the target hardware, the ROM monitor supports a set of primitive debugging commands that make it possible to find what is stored in memory at a particular address, insert values at certain addresses, and set breakpoints, for example. By connecting the NS16000 hardware to the company's VAX host via a serial line, the company could run the frontend user interface on the VAX and still control the target system.

This debugging environment proves to be extremely useful in debugging the Unix kernel itself. Instead of having to scatter printouts strategically throughout the software, they were able to single-step through instructions in the kernel to see exactly how it was behaving. They were also able to substitute a native resident equivalent of the ROM monitor for native debugging. Debugging continued throughout the porting effort. Additional debugging was performed when the Unix modules were assembled and released.

The task of porting Unix to a new microprocessor can be challenging. However, a chip's architectural features can make the job easier, and thereby contribute to the commercialization of the Unix operating system.

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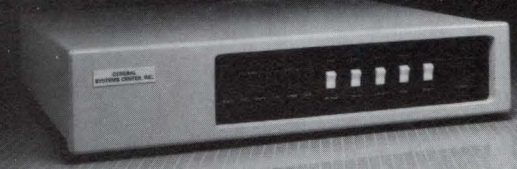

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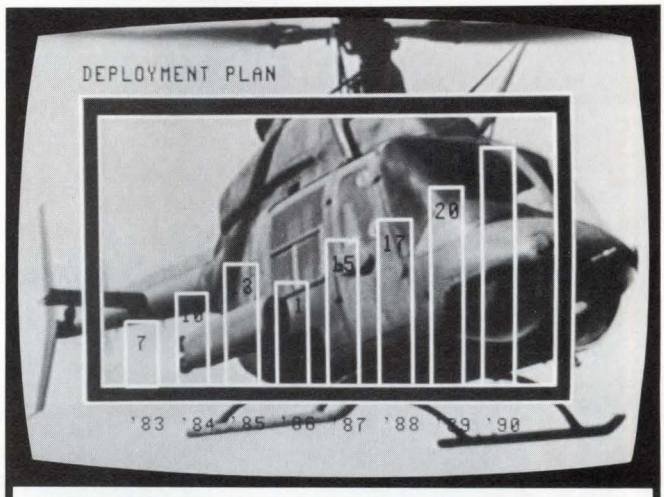

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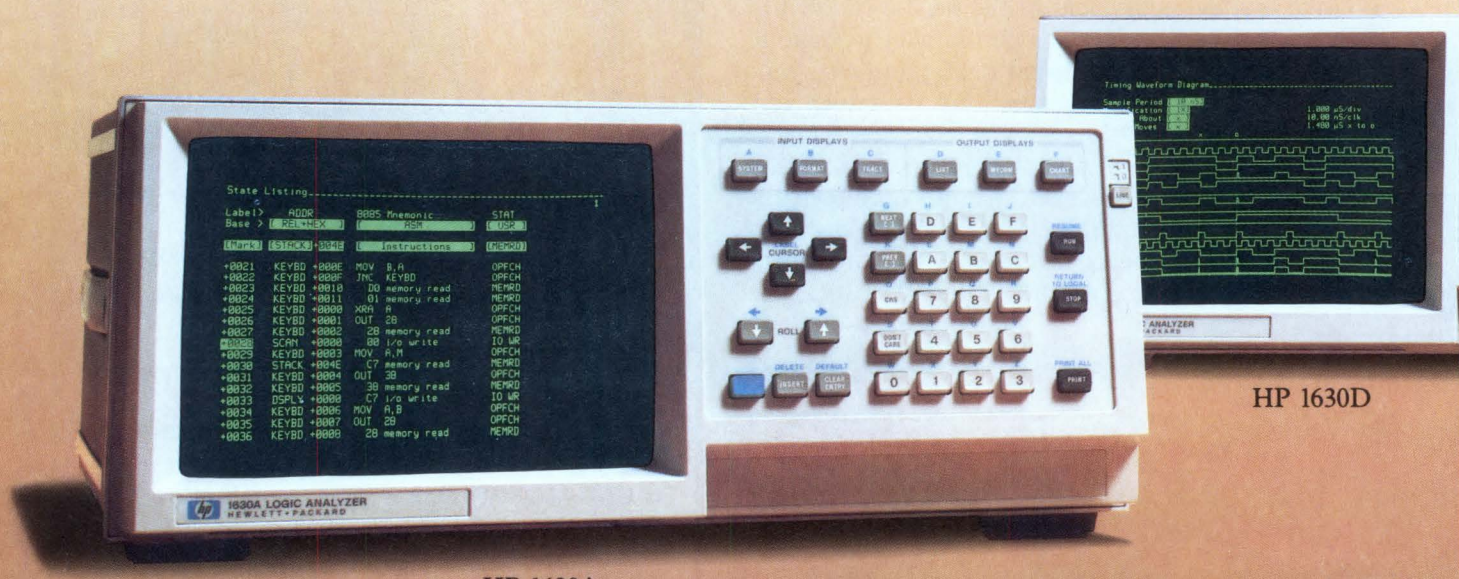

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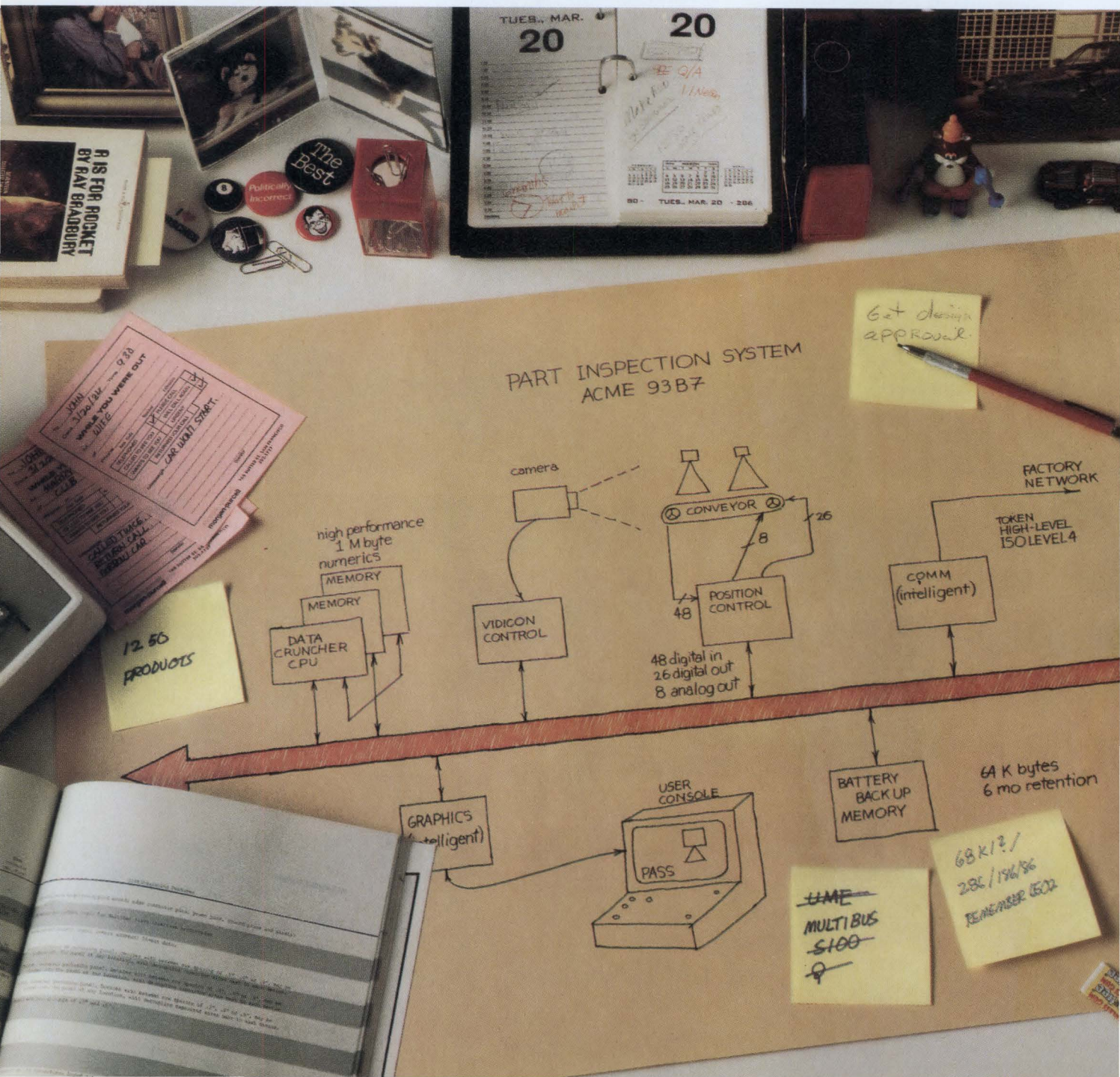

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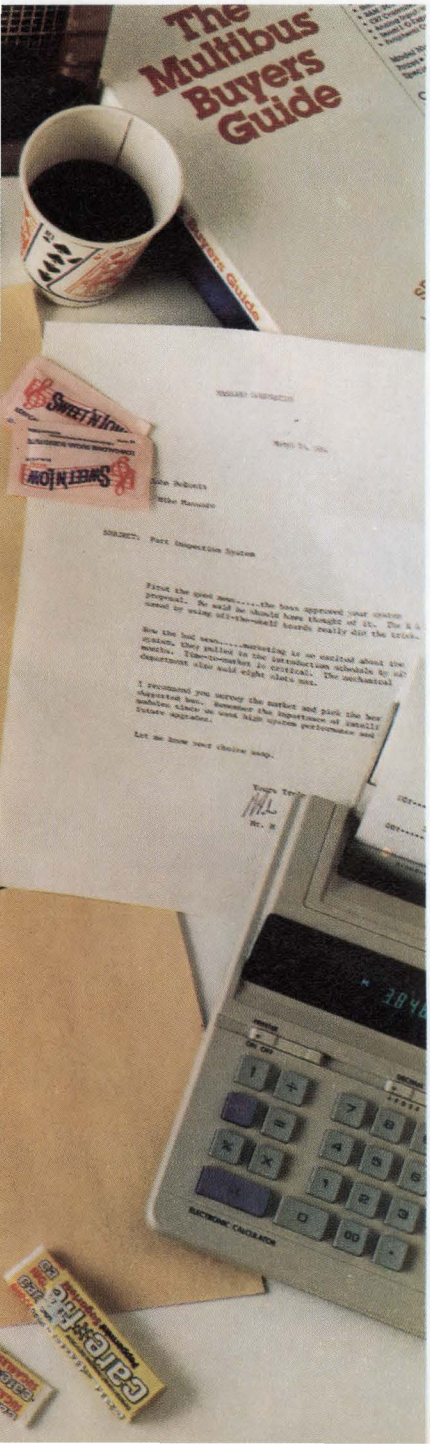

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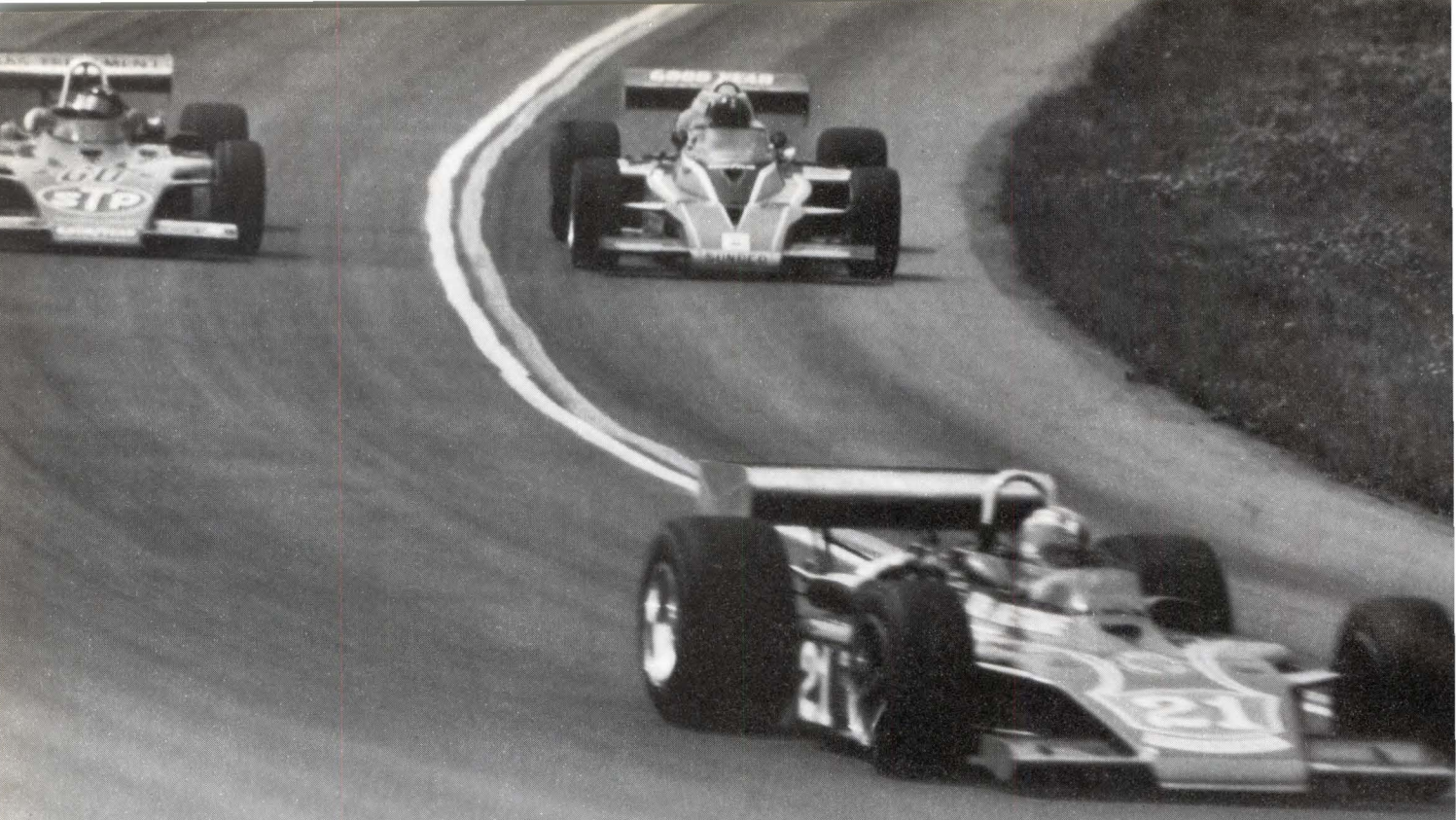

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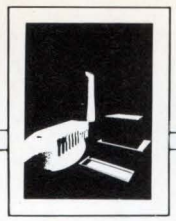

MICROPROCESSOR DESIGN SUPPORTS MULTITASKING

Hardware segmentation corresponds to modular software, easing design of current applications.

by Paul Wells

The spread of personal computers in the workplace has created a need for integrated software packages that juggle several tasks simultaneously. In the past, such facilities have been supported by multitasking operating systems running on larger computers. Bringing multitasking down to the level of microprocessor-based personal computer systems takes a high degree of cooperation between hardware and software. Some examples of this cooperation are Microsoft's Windows and VisiCorp's VisiOn. Both integrated software systems make good use of memory segmentation found in Intel microprocessors. Such segmentation is specifically designed to meet the heavy demands of a multitasking environment. Segmentation is further extended in the 80286 CPU through onchip implementation of key functions needed to support concurrency. Moreover, special coprocessors cooperate with this multitasking hardware to boost performance without imposing additional overhead.

As with its predecessors in the iAPX 86 family—the 8086/8088 and 80186/80188—the 80286 views its system memory as a collection of individual blocks (or segments) of data and executable code. This memory model, as a collection of individual segments, corresponds directly to the way software designers think of data and programs—as a set of individual modules. For example, in creating an integrated software package, programmers might place a software program for word processing in one or more segments, spreadsheet routines in others, and communication software in still other segments.

Segments serve as the fundamental units of all operations in the 80286. The processor deals with a segment through a consistent data structure (called a segment descriptor) for all multitasking support, memory management, or memory protection operations. Just as efficient programmers build pointers to manipulate a physical block of data or program code, the CPU handles descriptors that contain all the information needed to access a segment (Fig 1).

Code and data segment descriptors contain a 24-bit field that specifies the physical memory address of an associated segment, permitting a 16-Mbyte physical memory. A 16-bit field specifies segment size, allowing it to range between 1 byte and 64 Kbytes. Because the 80286 packs its pipelined architecture with dedicated onchip hardware registers for each class of descriptor associated with critical system operations, the CPU outraces even the VAX 11/780 in performance tests.

Memory management

Besides enhancing overall system performance, the onchip registers relieve programmers of low level details in implementing CPU-specific mechanisms. Furthermore, as in the 80286's virtual addressing mechanism, these onchip registers provide a path for migration of the large installed software base for the 8086/8088 and 80186/80188 to the next generation of personal workstations.

Paul Wells is a technical marketing manager at Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. He received a BS from the University of Santa Clara.

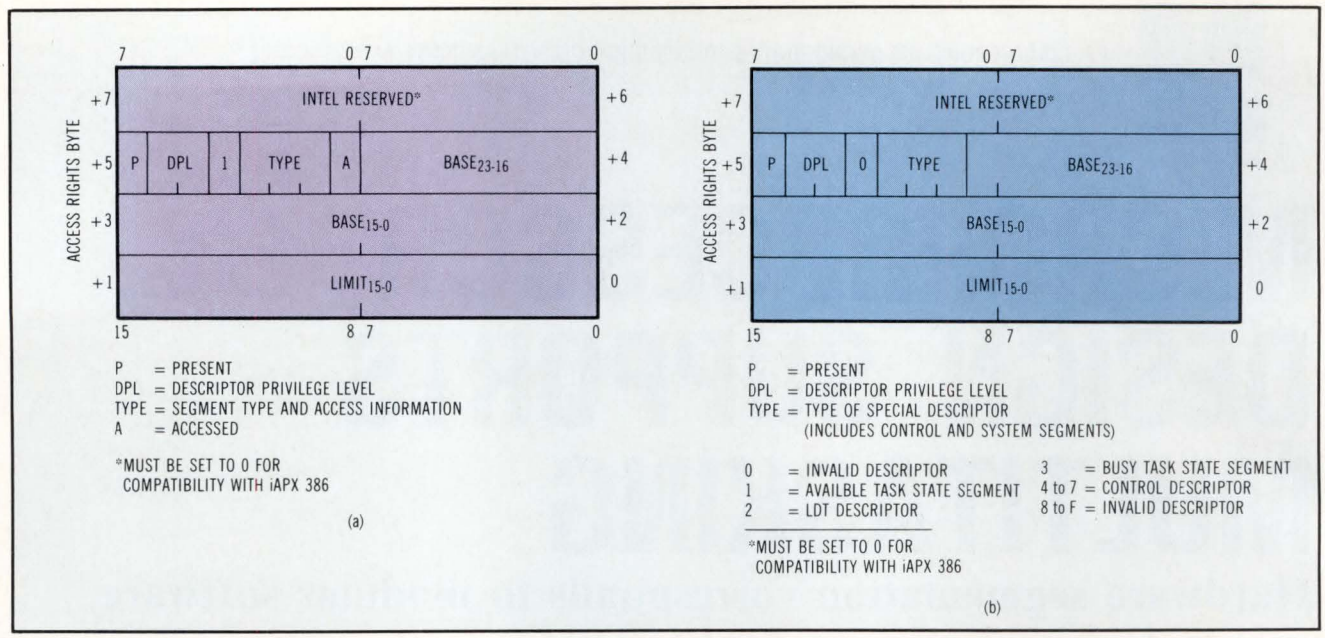

Fig 1 The 80286 segments all operations. To refer to these segments, the CPU uses one type of descriptor for code and data (a) and others for maintaining special structures like those used in multitasking (b).

Increasingly sophisticated user interfaces and large information bases will strain memory resources in future personal computers. Although the 80286 sports a 16-Mbyte physical address space, most desktop personal computers will not be fully packed with costly semiconductor memory. They will instead exploit the economic advantages of virtual memory management—a strategy that has proven effective in mainframes and minicomputers.

In a virtual memory environment, system memory is logically extended beyond the confines of available physical memory. The system accomplishes this by using mass storage to store data and code segments not needed by currently running tasks. The application software issues references to logical memory and relies on the operating system both to ensure that needed segments are in physical memory and to translate the logical reference into one that addresses data or code within the segment once it is in physical memory.

In order for the system to determine which segments to bring from disk and where to put them, the operating system uses flags associated with each segment. For example, an operating system can use the "present" and "accessed" bits in 80286 segment descriptors to check if a segment is present in physical memory and if the segment has been recently accessed. Once it loads a segment, the operating system updates tables that indicate where a logical segment is located in physical memory. Drawing from these tables, a memory management unit (MMU) sets up tables in its own internal cache, which it uses to convert a logical address supplied by the CPU into a physical address (Fig 2).

In traditional virtual memory systems, when an application program loads an address pointer with a value that is not in the MMU, operating system routines must execute a cumbersome series of procedures to update the MMU. This includes loading the MMU with the translation information, verifying access rights to the missing segment, verifying that the segment actually exists in physical memory, and reconstructing the state of the CPU before the address fault. Traditional systems could easily waste a millisecond of precious CPU time to handle this form of virtual memory management. Thanks to the memory management capability built into the 80286 CPU, users enjoy the performance advantages of rapid address translation, while programmers gain an extended memory reach with little apparent effort.

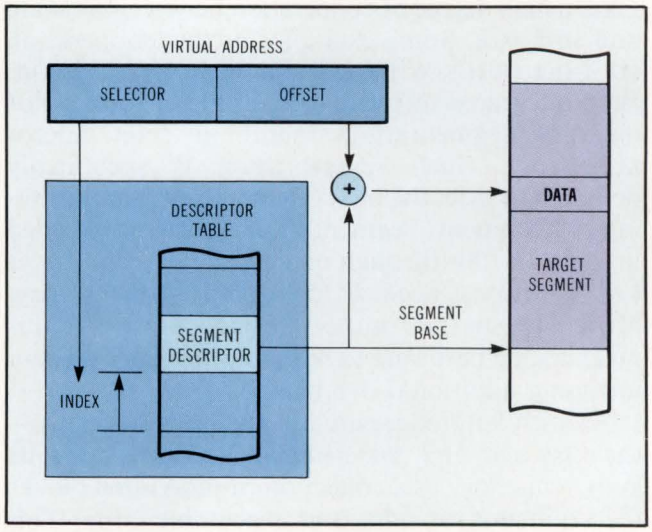

Fig 2 An address in the 80286 is comprised of an offset and a selector. In virtual addressing, the selector is used as an index into a table of descriptors for building the physical address. In real address mode, instead of the operation indicated in the shaded portion of the figure, the CPU multiplies the segment selector by 16 and adds the result to the offset to point to the desired location in memory.

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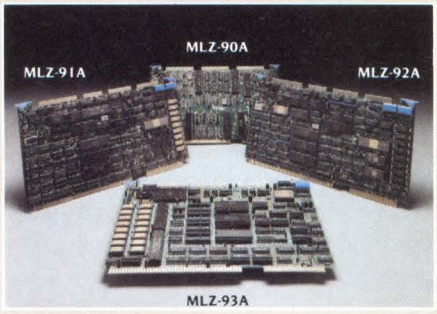

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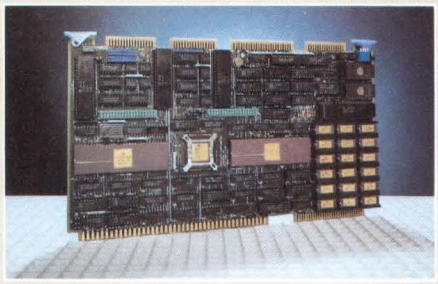

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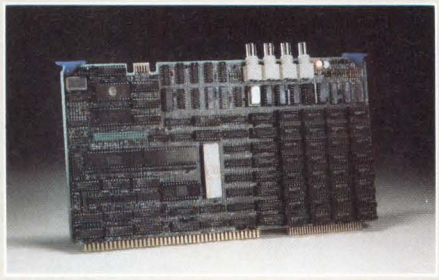

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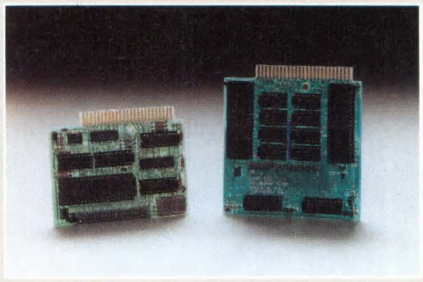

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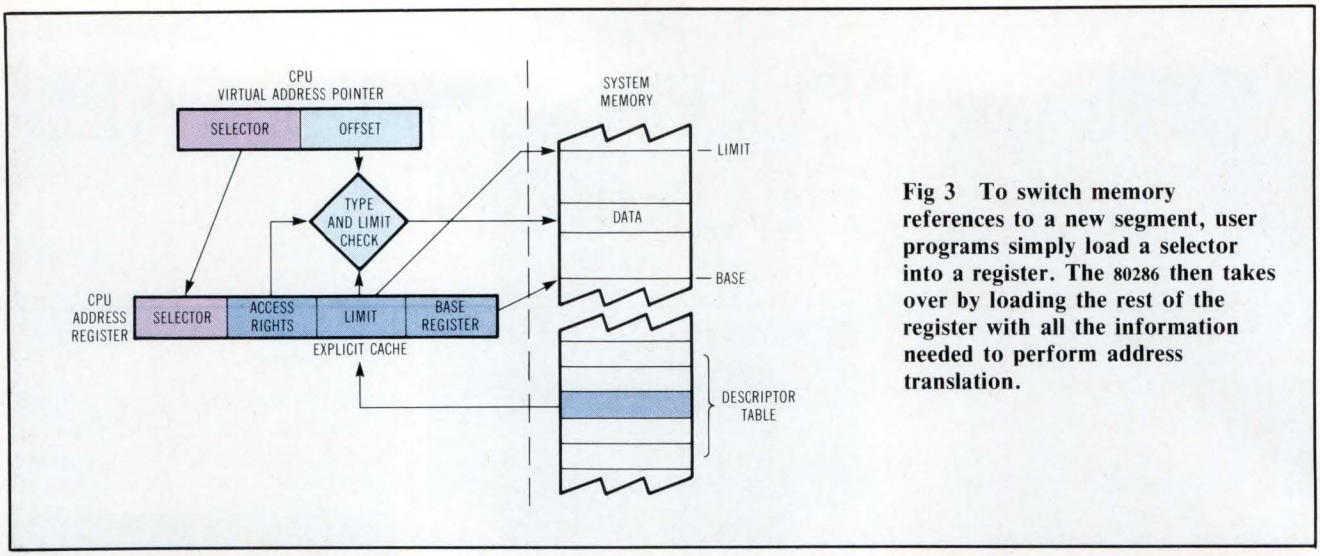

Fig 3 To switch memory references to a new segment, user programs simply load a selector into a register. The 80286 then takes over by loading the rest of the register with all the information needed to perform address translation.

As in the earlier members of the iAPX 86 family, an address in the 80286 is a 32-bit value, comprised of a 16-bit field that selects a particular segment and a 16-bit field that pinpoints a byte within the target segment. However, the 80286 treats the segment selector differently in its real address and virtual address modes.

In virtual address mode, the 80286 can complete a translation in a single clock cycle, using an onchip cache of registers that contain translation and access rights information drawn from the associated segment descriptor (Fig 3). When a program needs to change segments, software simply loads the selector to the associated descriptor. The 80286 automatically loads the needed memory management information into the onchip registers. Until a program specifies a new segment, the 80286 uses these registers to translate subsequent address references.

Programmer's helper

The 80286 chip further strengthens multitasking systems with direct hardware support for the critical mechanisms of multitasking. In a multitasking environment, system level software normally maintains minimal information for each task likely to be executed. When a user activates one of these tasks, such as pointing to a symbol with a mouse, system level software routines use this information to begin executing the corresponding programs. For example, a user might start transferring a document through electronic mail and then open both a spreadsheet and a document file to prepare a report. Thus, the CPU is forced to juggle a number of active tasks simultaneously.

System-level software maintains information on the state of each of these active tasks. This information typically includes data on both the physical status of the task, represented in the contents of the CPU registers, and its logical status—such as whether the task is waiting for another task or device to complete some action. When system software finds that a task has satisfied all the logical conditions needed to enable its execution, the operating system then loads the physical information corresponding to the task so that the CPU can commence (or continue) its execution. The process is called a task switch.

This logical status information is closely connected to the particular design and implementation of a multitasking system. Consequently, a general purpose CPU cannot include special purpose hardware that ties the hands of software designers by requiring them to use a hardwired scheme for these system level algorithms. However, manipulating this physical information is an inescapable part of a multitasking system—and one that can result in severe system overhead. Consequently, 80286 hardware directly supports this physical aspect of a task switch.

Traditionally, software manages this task-related information. To effect a task switch in these systems, software must exercise a series of procedures, including copying the CPU registers and pointers into system memory. Several hundred milliseconds are usually required to complete this process. In an integrated software system intended to provide a reasonable electronic analogue to the physical environment, this delay is unacceptable.

Speedy switch

The 80286, on the other hand, needs only 21 μs to effect a task switch because CPU hardware directly recognizes a special data structure, called a task-state segment, that is fundamental to task switch operation. The CPU keeps track of the current task with a dedicated register that contains the address of the task-state segment descriptor.

The system programmer is not concerned with the low level details of a task switch, but simply loads the task-state register with the selector to a stack-state segment descriptor. Consequently, to the programmer, a task switch is just a JUMP instruction, rather than a set of special instructions. The 80286 saves the state of the currently executing task in the previous task-states segment and it then

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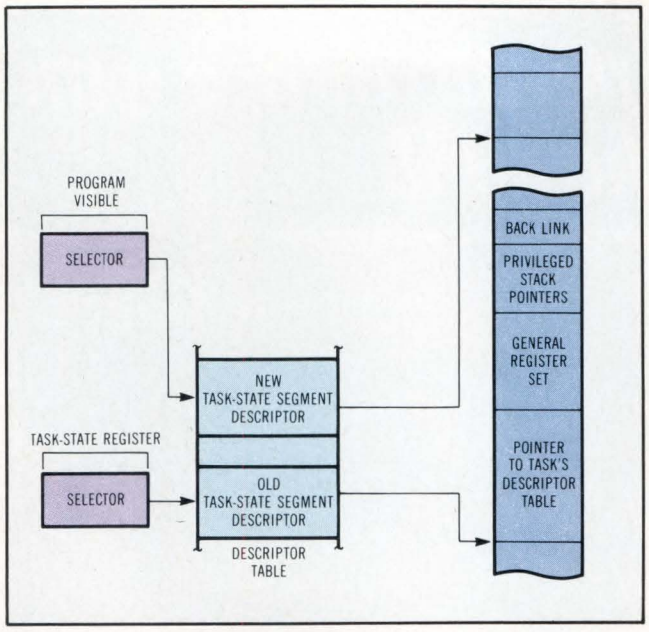


Fig 4 Just as with address translation, programmers are not bothered with the details of a task switch. Instead, after loading the task-state register with the selector to a new task-state segment's descriptor, they let the CPU bring in the information that specifies a task's state. This is contained in the task-state segment.

automatically loads the information contained in the new task-state segment (Fig 4).

Just as a typical business day is filled with a continuous series of interruptions, a typical multitasking operating environment is continually bombarded with a flood of hardware interrupts from keyboard and mouse interaction, disks, and peripheral devices such as printers and modems. To the 80286, these interrupts simply occasion a task switch.

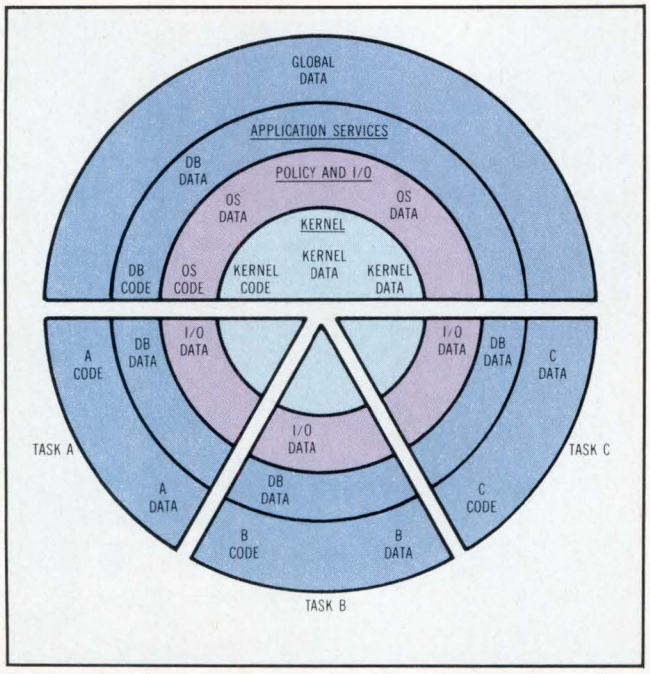


Fig 5 With four privilege levels, the 80286 can support a number of different protection policies. Typically, the most trusted inner ring holds code and data for the kernel—the most fundamental mechanisms of an operation system.

In fact, the task-state segment contains a special field that holds the address of the interrupted task-state segment. In a series of interrupts, the CPU uses this back-link pointer to maintain a record of interrupted tasks. The 80286 then unravels this chain of tasks and finally returns to the task that was running before the interrupts occurred.

In an iAPX 286 system, coprocessors like the 80287 numeric coprocessor, 82586 local communication controller, 82501 Ethernet serial interface, or 82730 text coprocessor impose no extra burden on the task switch mechanism. A CPU task switch does not change the coprocessor's own internal state. Instead, the 80286 simply sets an internal bit whenever it executes a task switch.

The next time an instruction specifies use of a coprocessor, this set bit causes the CPU to trap to a system handler that determines if the last task that used the coprocessor is the same task currently requesting its use. The trap handler needs to switch the coprocessor's internal state only if the current task is different. In this way, if a task that is using a coprocessor is interrupted, it may continue to use the coprocessor without necessarily executing a coprocessor context switch following the interrupt.

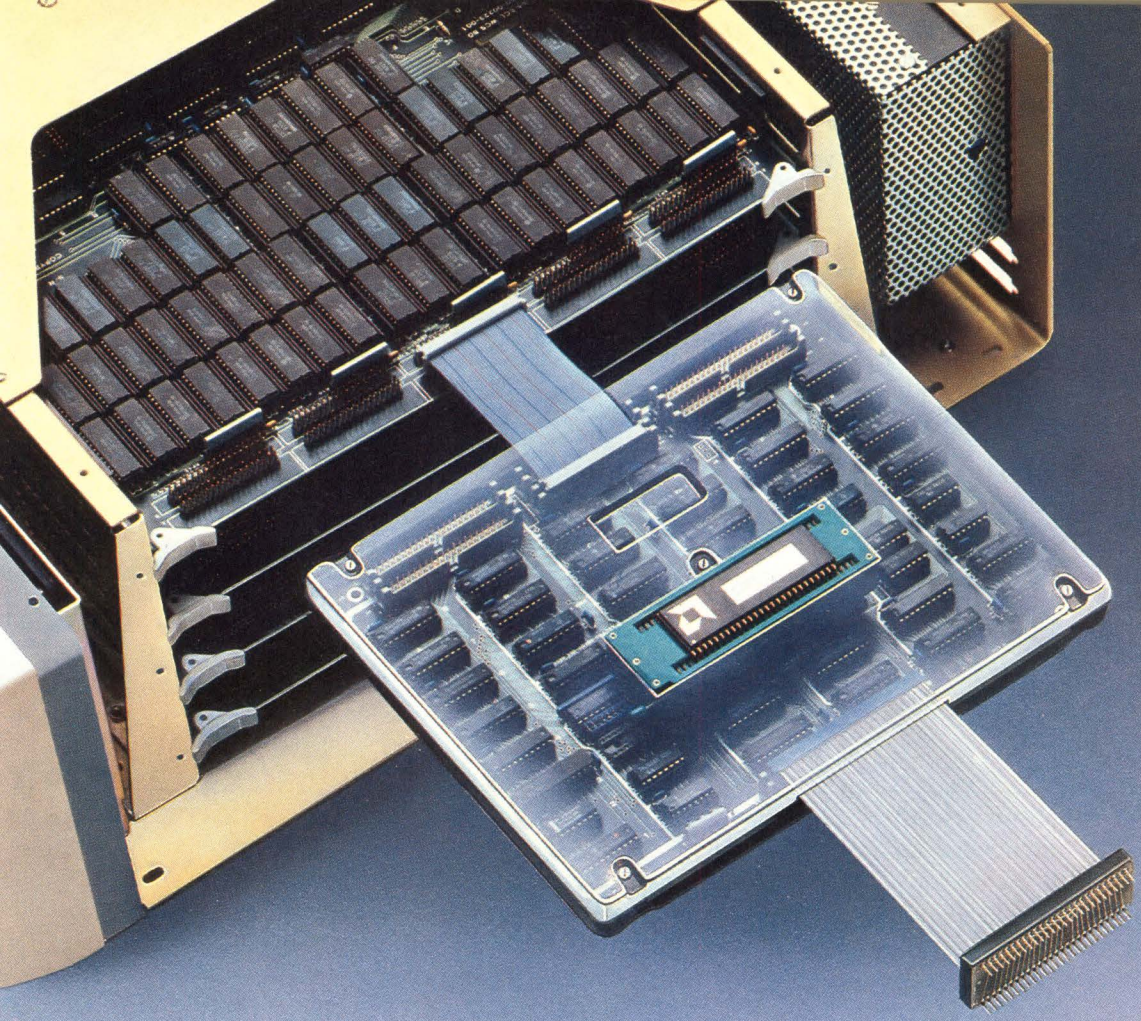
Segments anchor protection

The ability for individual systems to communicate across networks translates into a need for effective software protection. Systems must constrain access to programs and data. In addition to challenging illegal attempts to break into a system, protection also serves a more mundane function. It must ensure reliable system operation even when a software bug sends a program into space normally reserved for the operating system and related functions.

To control this situation, computers usually provide a simple pair of privilege levels—executive and user—in which a program may execute. But even user programs must be able to execute system level functions such as I/O. Consequently, truly secure systems extract user accessible system software and place it in its own level—requiring that the CPU support at least three different execution levels. Going one better, the 80286 provides four privilege levels, numbered 0 through 3. Programs executing at a given level may only access data (or programs) at a numerically greater (less trusted) level.

A typical system would normally apportion its services over a number of these levels. For example, a system might place the fundamental mechanisms, or kernel, of an operating system in the most trusted level (PL0), system services in the next level, library services in the lower level, and application programs in the least trusted level, which is PL3 (Fig 5).

In this type of multidomain operating environment, the protection mechanism must nevertheless leave a door open for less trusted tasks to access segments at the more trusted levels. In the 80286, these



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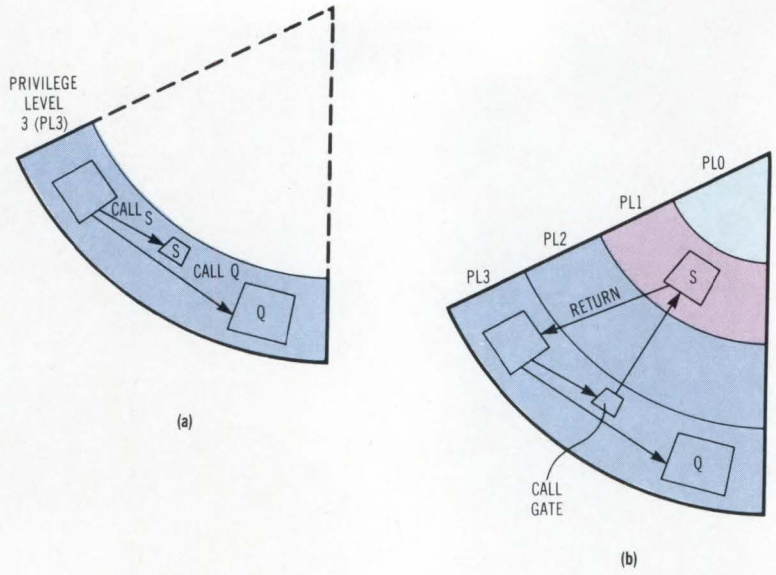

Fig 6 Although 80286 hardware shields programmers from seeing any difference between calling a subroutine Q at one privilege level (a) and using a gate to call a subroutine S at a more trusted level, (b) the mechanisms differ. When the call gate passes control to subroutine S, the gate also passes a copy of the calling subroutines stack to S.

portals between levels are special descriptors, called gates. The CPU permits a less trusted task to access the segment associated with a gate only if the gate descriptor is located at the same level or a less trusted level. From the programmer's point of view, access through gates to segments at a more trusted level looks just like a normal subroutine call (Fig 6).

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However, when a task passes the access rights check, the underlying mechanism of passing control to the associated segment is much more complex than when a task accesses another segment through a normal descriptor. Tasks typically pass parameters to subroutines through the system stack. But in the interests of maintaining system security, the CPU must maintain separate stacks for a task at each privilege level.

Gates resolve both these requirements by copying a specified number of words from the calling task's stack to the corresponding stack at the target segment's privilege level. A special field in the gate descriptor permits up to 32 16-bit words to be passed in this manner.

Gate-mediated access also results in more streamlined calls to operating system routines. In traditional operating systems, the program executes a trap or software interrupt to a separate system handler when a program requests a system function. This software routine must first copy the parameters from the user stack to the system stack and then call the appropriate system subroutine. With this method, a typical system call takes 80 to 200 μs. Because the 80286 permits application programs to execute a simple subroutine call to operating system services while handling the related housekeeping in hardware, a typical operating system call takes only about 12 μs.

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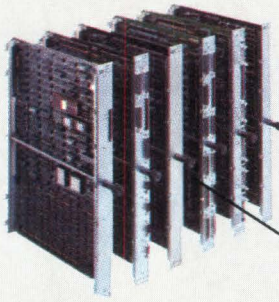

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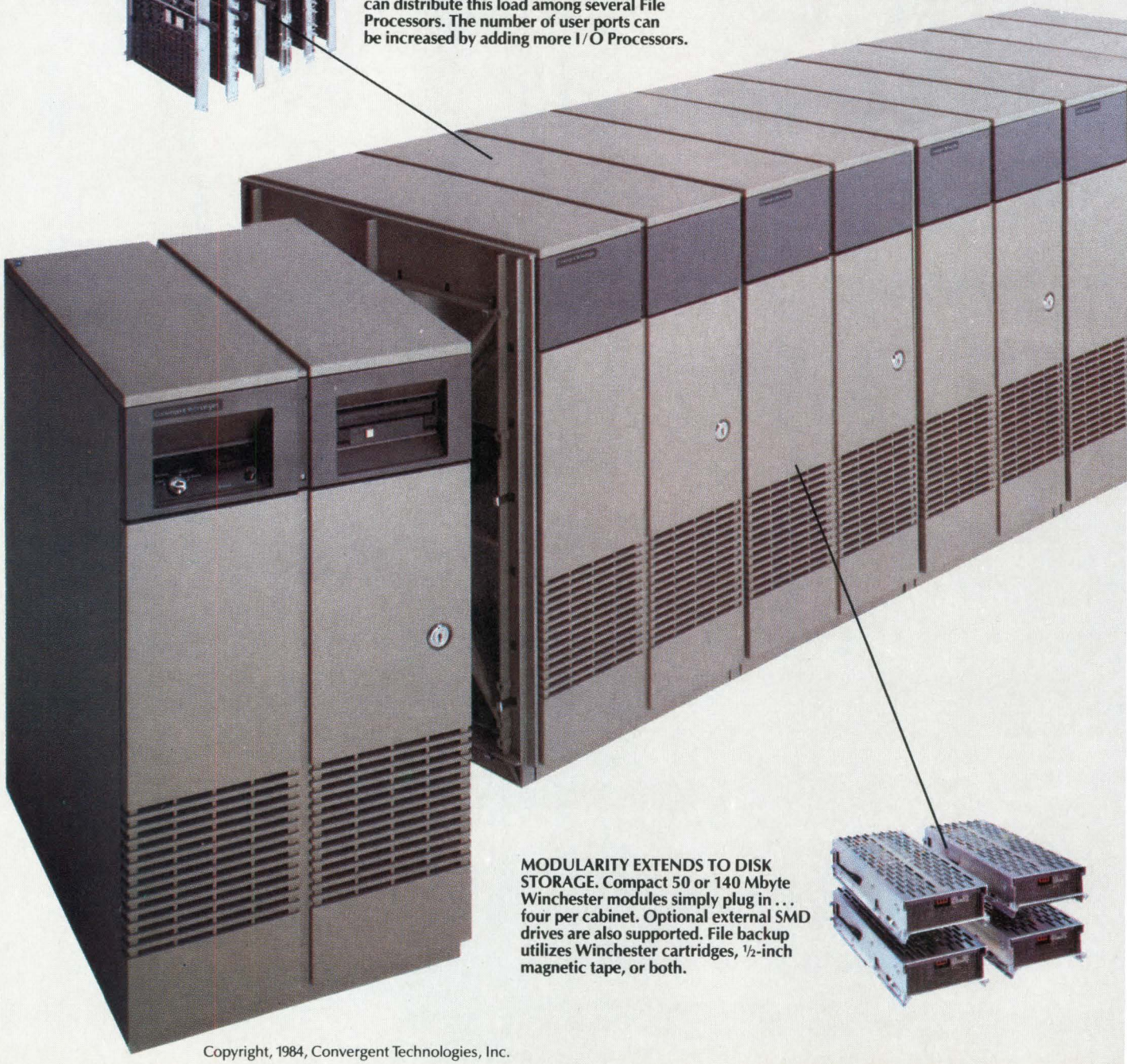

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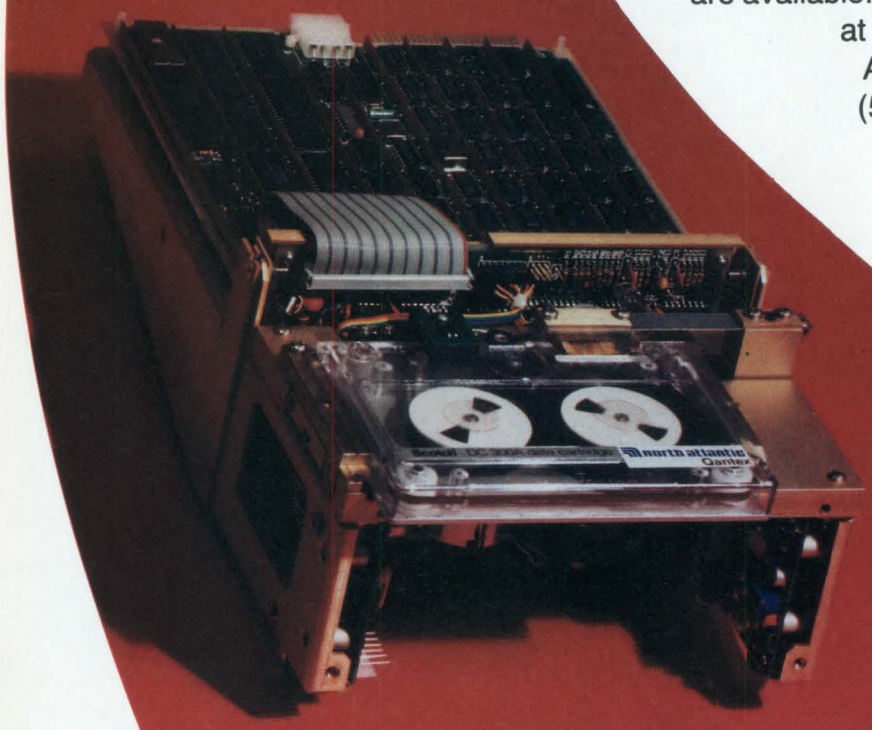

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CIRCLE 102

JETSTREAM™16

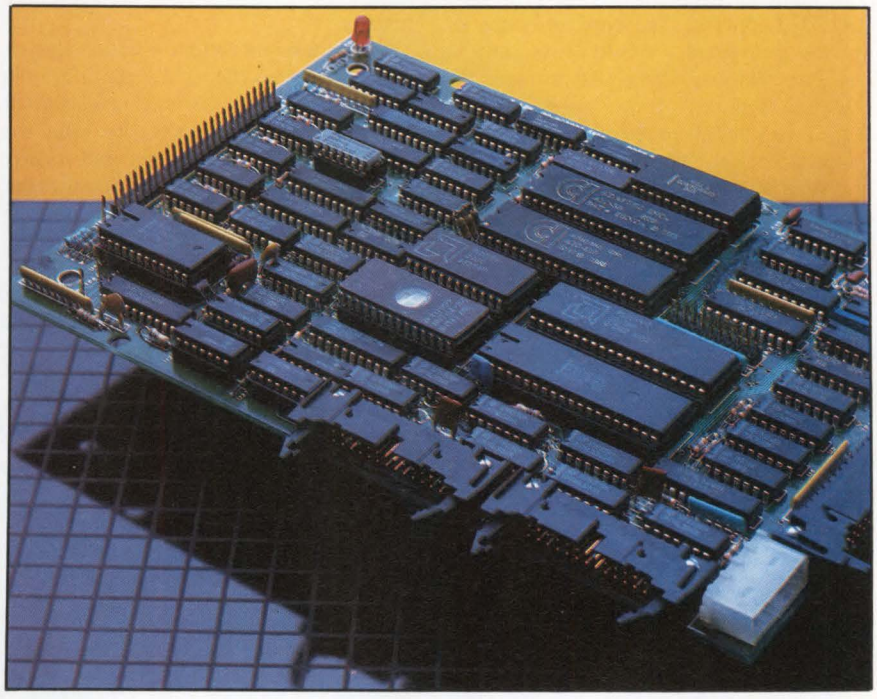
Controller joins host adapters to step up performance

Addressing multi-user/multitasking systems that require high I/O subsystem performance, model ACB-5580 provides full support for the SASI/ANSI SCSI bus implementation. The rigid disk controller includes arbitration and disconnect/reconnect functions, and an SMD interface. At the controller's core is a 10-Mbit/s custom chip set, making it responsive to SMD drive performance requirements. The controllers can now handle disk memory capacities ranging from 5¼-in. Winchesters to large SMD drives.

As part of the SCSI implementation, the boards have a straightforward bus structure that includes 8 data bits, 1 parity bit, and 9 control bits. An easy-to-use command set provides access to virtually all functions using only read, write, and format commands. Variable block sizes and multiple block transfers are allowed with a single read or write command. The I/O is fully buffered with a dual-ported FIFO. Buffer size ranges from 1024 bytes to 65 Kbytes.

Furthering the concept of maximized I/O performance, the board supports up to seven host CPUs through the SCSI bus and up to four SMD drives. It drives either 8- or 14-in., 9.6-Mbit/s SMD drives and includes all the features of the company's 5500 board for 5¼-in. Winchesters. This includes disconnect/reconnect, file sharing, and noninterleaved operation.

The disconnect/reconnect feature of the bus allows a system to run concurrent tasks by handling multiple seeks and read/writes with the I/O bus disconnected. It reconnects only when a drive has data ready for the read/write operation. The controller, therefore, completes the tasks in the most efficient order, regardless of the order in which they were received. The result is increased speed and efficiency of I/O transfers. In addition, multiple drive access time is decreased, resulting in up to a five time increase in system I/O performance.



The board relieves the operating system of managing shared disk functions in a networked system through a reserve/release command. This command manages multiple access to files maintaining data integrity. Moving these functions to the disk controller increases operating system speed and improves file-sharing reliability by simplifying the operating system.

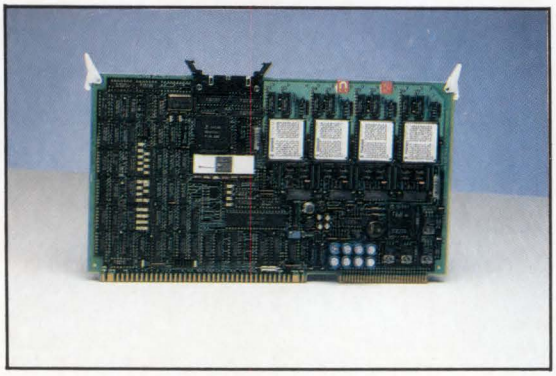
Data throughput increases by implementing noninterleaved operation. All information on one track of the disk is accessible in one rotation. Other controllers can require up to four or more rotations of the disk (in interleaved operation) to access all the information on a single track.

Complementing the board's multitasking operation capability, the AHA-1510 and the AHA-1530 are intelligent host adapters that support the S-100 host bus and the Multibus, respectively. They sit between the host bus and the SCSI bus to improve system performance by functioning as I/O processors, working with the I/O supervisor of the operating system.

Both host adapters support high speed DMA at 1.5 Mbytes/s from the SCSI bus to the host's local memory. This support, together with monitoring bus handshake protocols and interrupts, maximizes hardware performance. Developed using IBM's concept of a block multiplexer channel, the adapters handle up to eight concurrent I/O requests. The operating system is then freed of its I/O management duties and can execute more application functions.

Price for the ACB-5580 is $980 with production beginning in the third quarter of this year. The AHA-1510 is $425, while the AHA-1530 is $460. **Adaptec Inc,** 580 Cottonwood Dr, Milpitas, CA 95035. *—M.B.*
Circle 260

Memory bubbles packaged to ride high on the Multibus



Offering built-in 1-Mbit bubble devices, the FBC504M4M series provides four different memory capacities—128, 256, 384, and 512 Kbytes. The card operates as memory-mapped I/O requiring only a 64-byte memory space. Advantages include a single 5-V power source, an internal power fail protection circuit, and data retention even without power.

All bubble memory operations are controlled by commands that are set by 5 separate bits in the command register. Several registers act as the interface between the host and the bubble device. A 4-byte FIFO data output register holds data that is read from the bubble. When a data read command is set in the command register, data transfers from the bubble memory to the data output register at a 80-μs/byte rate. Page changes increase this transfer time by 0.3 to 1.5 ms. As the data transfer begins, the number of pages (as specified by the host system) goes to the data output register at the same 80-μs rate. Also a 4-byte FIFO register, the data input register functions in the same manner when the data write command is in the command register.

Other registers include a status register, which indicates the card's condition via flags. An error status register lists error contents; a page address register holds the starting address of a page; and a page count register keeps track of the number of pages that will be transferred. In addition, a DMA band select, write only register is accessed for DMA transfers.

The bubble device operates in various software-controlled modes. The read/write command sets the interface registers to execute the read/write operation. It begins by sending the start page from the host to the page address register and the number of pages to be transferred to the page count register. The command register is then set with a command, allowing a sequence of operations to execute. First, bad loop data is automatically read from a boot loop. An error occurs if the bad loop data is invalid or if the data cannot be read. Next, the page indicated in the page address register is searched. Data is then written to the bubble via the data input register or read from the bubble via the data output register. During the transfer process, the controller continuously refers to the bad loop data storage so bad loops are skipped. When all the pages indicated by the page count register transfer without errors, a status register bit is set.

Other memory card features are 12.5-ms average access time, subpage read/write commands, and error correction. Prices range frim $620 to $1410 in 100s. **Fujitsu America, Inc, Component Div,** 918 Sherwood Dr, Lake Bluff, IL 60044.—*M.B.*

Circle 261

Source control tools help manage large software projects

A set of software tools designed to help manage and maintain large software projects currently runs on DEC's PDP-11 RSX and RSTS, as well as VAX/VMS environments. Called SourceTools, the package is a collection of version management, file building and file comparison programs that work with any computer language and allow programmers to use their favorite text editors and utilities.

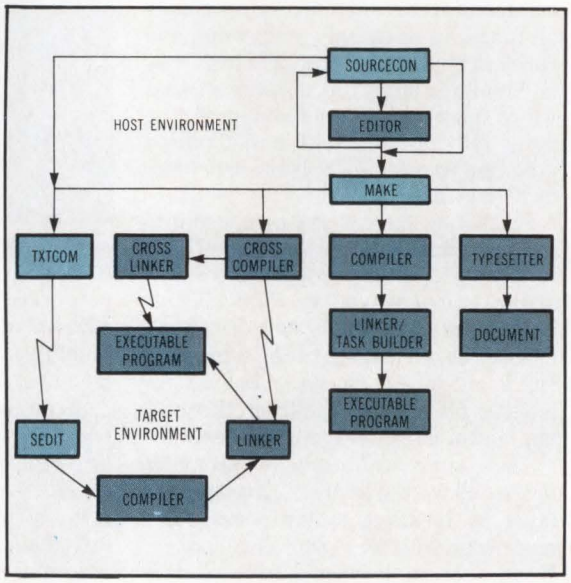
SourceTools consists of three groups of programs that work together to create an integrated software development environment. The first of these is SOURCECON, a control package that handles the creation and modification of source files. User-defined information can be required via prompts, so that an accurate history of each module can be maintained.

SOURCECON also ensures a disciplined modification order for modules. If a programmer checks out a module for editing, other users may check the same module out for other purposes, such as reference, compiling, running, linking, documentation, etc, but may not alter it.

Only when users decide that their editing changes are to be included in the module do they invoke UPDSRC, which updates that module. The module remains locked to changes by other users until the update is completed, thus ensuring integrity of modules. When a module is updated, it registers all changes, who made them, and when they were made. It also prompts the programmer to state and explain the most recent changes.

Such prompts painlessly create a history of each module that can be retrieved and printed using the PRTSRC function. The history includes the reasons for updates, as well as a record of all changes. A file comparison utility lists all changes that have been made to a file.

A file builder program called MAKE keeps programs under development up to date as modules are changed. This avoids lengthy recompilations of the entire program at every change. The programmer supplies a description file that indicates which modules depend on others. MAKE then looks at the description file to decide which modules to compile and use to build the main program. In this way, the user may simply build different description files to create different configurations of the same basic program.



The price of SourceTools is $4500 for RSX and VMS in RSX compatibility, and $3600 for the RSTS version. Prices include one year of customer support. **Oregon Software,** 2340 SW Canyon Rd, Portland, OR 97201. —*T.W.*

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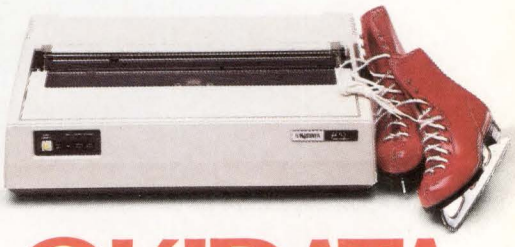

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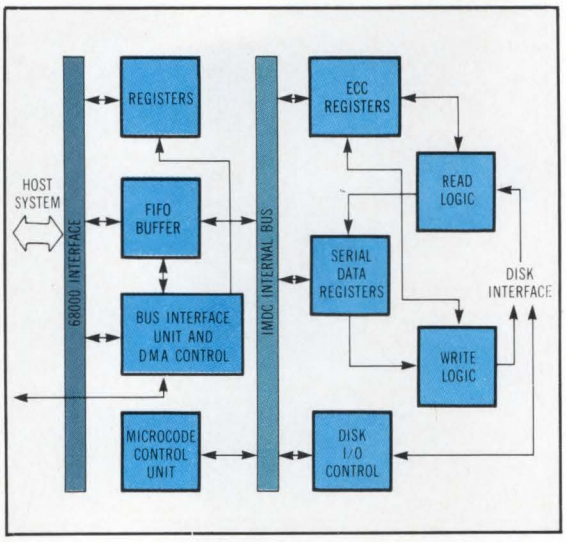
CIRCLE 103

Smart disk controller locates and searches strings

The general trend in chip building is to put progressively more intelligence on silicon, and off-load control functions from the host CPU. The Intelligent Multiple Disk Controller (IMDC) SCN68454 does just that by offering the system designer a versatile programmable disk controller. In addition, it provides a sophisticated string matching function that can be used to create a disk-based database system.



Bus compatible with the Motorola 68000 microprocessor, the chip supports vectored interrupts, a 31-bit address counter, and either 8- or 16-bit data transfers. It supports up to four floppy or hard disks, and uses either SA1000 or ST506 protocols to control the drives.

Capable of handling serial data rates up to 10 Mbits/s, the IMDC has a range of commands that allow the programmer to specify disk parameters, and to read soft or hard sectored disks, as well as standard IBM floppy formats. The chip has a DMA controller, and a 128-char FIFO buffer onboard, handles bus arbitration automatically, and uses tables resident in the host's memory to get and send status and control information to and from the host.

Error-handling functions include automatic bad sector handling, 32- and 40-bit ECC, and support for host-generated ECC. It handles FM and MFM data encoding, and can read or write multiple sectors automatically.

Using parameters supplied in a control block in system memory, the IMDC locates a specified string of characters within any logical data block on the recording media. It can then retrieve and store the contents of the block, use a pointer value to access data within the block, or locate all data blocks that contain a string that matches a given search string.

Both fixed- and variable-length records can be searched, and pointers can be used to search for key fields within the record. With fixed-length records, the index will be an integral number of bytes from the beginning of the record, but in variable-length records, it will be the "nth" field in the record. To support variable-length records, the IMDC lets the programmer specify a field delimiter. Using the separator as a marker, the IMDC simply counts fields, and retrieves the proper one for key processing. **Signetics Corp,** 811 E Arques Ave, PO Box 409, Sunnyvale, CA 94086. —*S.B.*

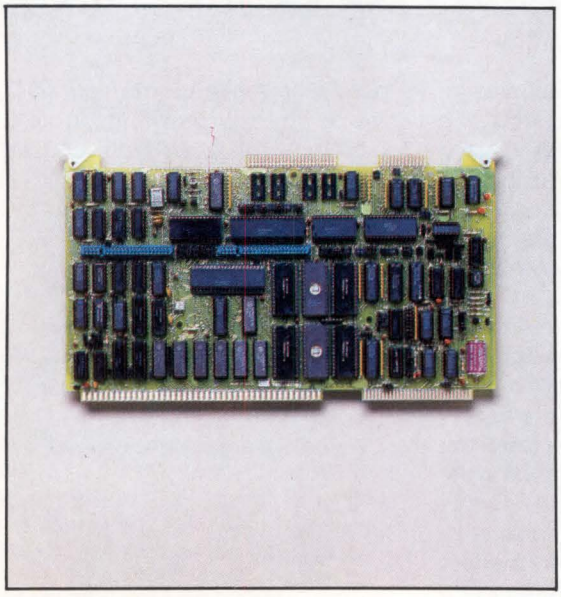
Circle 263

Board counts on CMOS for low power CPU processing

Both hardware and software compatible with Intel's iSBC 86/05, the CBC 86C/05 captures the low power prize of CMOS without sacrificing system performance. Based on the Multibus, the board features an 80C86 CPU operating at 5 MHz, up to 48 Kbytes of a CMOS RAM/ROM mix, and onboard battery backup.

Standard ROM/EPROM memory capacity is 96 Kbytes maximum. With an optional CMX 1600 expansion module, the maximum reaches 160 Kbytes. With a RAM/EPROM mix, standard onboard capacity is 48 Kbytes, expandable to 80 Kbytes with the CMX module.

The onboard lithium battery provides over 2.5 years of continuous data retention without system power. Voltage sensing logic ensures data integrity during both short- and long-term power outages. An onboard 5-V power fail detection circuit can be used to protect RAM contents during power down and power up. An external memory protect signal can also be applied to disable RAM access.



In addition to the Multibus interface, the board uses a programmable peripheral interface that provides 24 parallel I/O lines. These lines are software configurable into any combination of uni- or bidirectional I/O ports. All Multibus and parallel I/O signals are TTL, or optionally, CMOS. A programmable synchronous/asynchronous RS-232-C serial interface results from a USART.

Asynchronous serial communication characteristics include 5- to 8-bit characters, 1, 1½, or 2 stop bits, framing, parity, and overrun error detection. Synchronous specs include 5- to 8-bit characters with internal character synchronization and automatic sync insertion. Asynchronous baud rates range from 75 to 9600, while synchronous baud rates range from 1760 to 38,400 baud.

The board also contains three 16-bit programmable counter/timers with various counting modes. A programmable interrupt controller handles nine maskable interrupts—eight with programmable cascading inputs for expansion to 64 interrupts.

The 80C86 CPU's word size for instructions is 8, 16, 24, or 32 bits and data word size is 8 or 16 bits. Memory addressing for ROMs and EPROMs in 2-, 4-, 8-, or 16-Kbyte devices is selectable on compatible address boundaries. With RAM, 8-K x 8 devices are selectable on 8-Kword boundaries.

Single-piece pricing is $1395 for the 16-Kbyte RAM version with quantity discounts available. Delivery is from stock to six weeks. **Diversified Technology, Inc,** PO Box 748, Ridgeland, MS 39157. —*M.B.*

Circle 264

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- Top to bottom functional panel layout.
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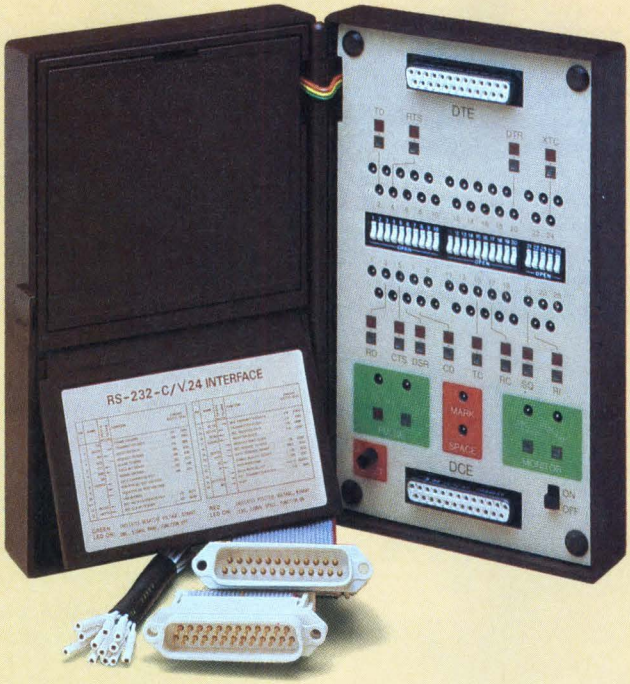

- Polycarbonate face (lettering can't wear off).
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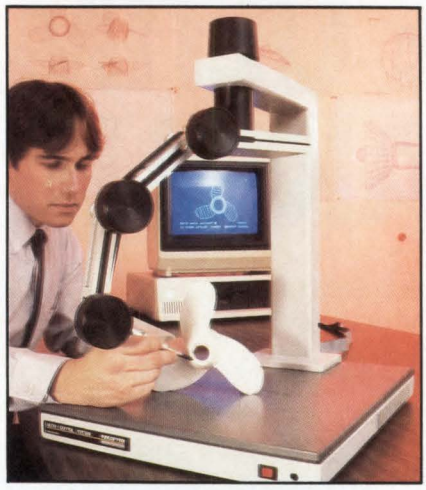
CIRCLE 104

Interactive CAD digitizer enters the third dimension

Dubbed an intelligent CAD peripheral that takes advantage of existing software, the Perceptor creates computer models of 3-D objects. Because its handheld pointer moves about the area to be digitized, an engineer can directly convey X, Y, and Z input coordinates—however irregular the physical reference.

Typical CAD workstations conform to 2-D design conventions and contain parts information in a special data base. For instance, X-Y coordinates are input using cursors, lightpens, or mice, and a digitizer tablet. Afterward, the Z coordinate is entered through the keyboard or constructed by software.

As an interactive, relatively low cost peripheral, the Perceptor can simplify desktop computer graphics and engineering tasks. Prospective applications include CAD, for creating and modifying 3-D designs under software control. Other applications include analyzing contours, tracing nested patterns, and modeling complex user-defined surfaces. Moreover,



the unit maps fields when sensors for sound, temperature, and radiation replace the standard pointer tip.

Mounted on a ground aluminum reference plate, the digitizing arm captures up to nine X, Y, and Z coordinates per second at 9600 baud. The arm has five standard joints; a sixth comes with an optional rotational platform. Embedded pots inside each joint convey the electrical information the system needs to calculate rotation angles. Maximum arm reach is about 42 cm.

A Z80A microprocessor board inside the 41- x 46- x 61-cm platform controls electrical data acquisition and converts analog readings from the pots. In turn, the digital signals can be sent over RS-232 interface to any computer that accepts serial input. The processor board also controls digitization modes and rates, baud rates, and calibration. Digitization modes are point, stream, delta distance, and delta time; baud rates are switch and/or software selectable at 300, 600, 1200, 2300, 4800, and 9600. Resolution is 0.018 to 0.025 cm.

Test units are scheduled to ship this month. Price will be under $7000. **Micro Control Systems, Inc,** 143 Tunnel Rd, Vernon, CT 06066. —*D.H.*

Circle 265

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The TransTerm® family of data terminals has the following common features:
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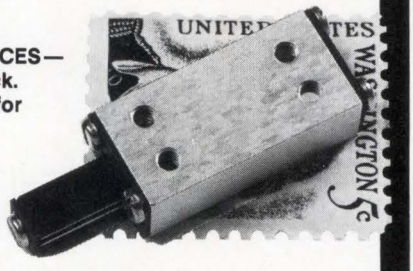

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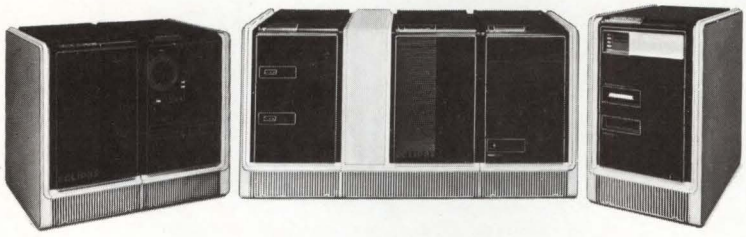

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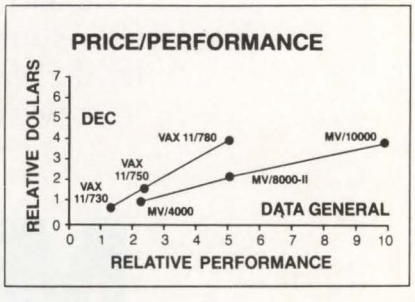

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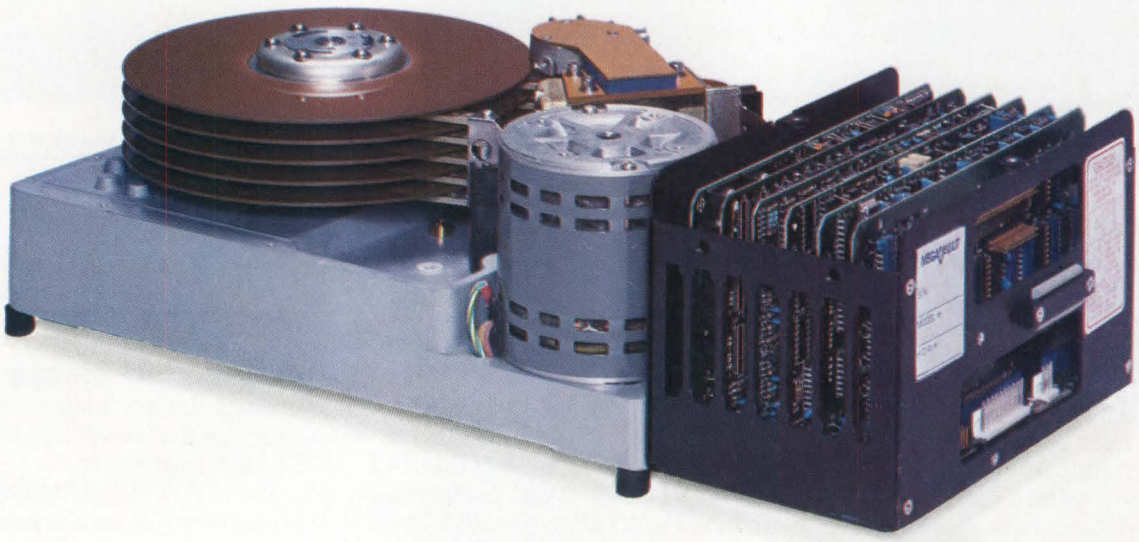

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CIRCLE 108

Analyzers feature automatic protocol analysis and interpretation

Intelligent about both character and bit-oriented protocols, the 200, 400, 600, and 800 analyzers can tell the operator what went wrong with the protocol and which device caused the problem. The 200 has a removable EEPROM pack, auto-setup, and full-protocol decodes. The 800 has a 10-Mbyte Winchester, color CRT, Sony microfloppy, and multilevel program operation. **Digilog Inc, Network Control Div,** 1370 Welsh Rd, Montgomeryville, PA 18936.
Circle 266

Network operating system pivots on message concept

The QNX operating system allows tasks to communicate with each other by sending messages. The tasks need not know the node on which another task is running in order to communicate with it. There are no restrictions upon the resources, which can be used by any task, nor are there any restrictions on the processor on which a task may execute. All workstation resources connected to the network are available for every task. **Quantum Software Systems Ltd,** PO Box 5318, Station F, Ottawa, Ontario, Canada K2C 3H5.
Circle 267

Networking device permits direct connection of host and RS-232

Microprocessor controlled, the Robin can network any four computers or terminals and a parallel device. Each unit carries its own control electronics based on a Z80 micro, 64 Kbytes of user memory (plus 2 Kbytes of nonvolatile memory), four RS-232 ports, one bidirectional parallel port, and configuration control. Autoconnect presets a port to a chosen destination. The network incorporates an adaptive time division multiplexing protocol. It is designed for round-robin scheduling and requires no collision detection or token passing. Signaling rate is 2 Mbits/s with a maximum aggregate user data rate of 1.8 Mbits/s. Cost is $1950. **Metapath, Inc,** 73 Lincoln Centre Dr, Foster City, CA 94404.
Circle 268

Protocol converter interfaces ASCII devices to an IBM mainframe

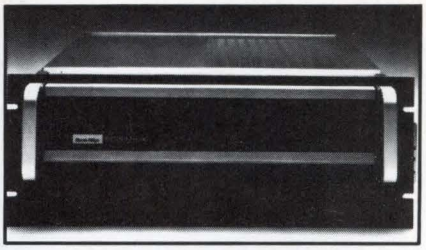
With 4, 8, 12, or 16 ports, the PSA 300 converter supports interactive sessions through the 3276 protocol and batch sessions through the 3770 SLU protocol. The SNA/SDLC converter is a diskette-based unit allowing configuration and/or diagnostic control to be assumed by any terminal attached on either local or remote basis. It supports up to 31 different CRT or microcomputer terminal types. Prices range from $4800 to $13,500 per unit. **Perle GSD, Ltd,** 600 S Dearborn St, Chicago, IL 60605.
Circle 269

High speed modems use LSI technology for small size

Models HD9600FP (9600 bits/s) and HP4800FP (4800 bits/s) are point-to-point and multipoint fast polling modems using the maximum capability of the processor. Other models are general-purpose CCITT-type modems appropriate in both dial-up and leased-line networks, point-to-point, and multipoint. Modem dimensions are 8.3 x 11.8 x 2.0 in. (21.1 x 29.9 x 5.1 cm) and weight is 5 lb. Power consumption is 13 VA. All modems use signal processor and micros to perform scrambling/descrambling, modulation/demodulation, encoding/decoding, and filtering. **Hitachi Denshi America, Ltd,** 175 Crossways Park West, Woodbury, NY 11797.
Circle 270

July Preview
A Special Report on System Software

Modem communicates with microwave and satellite networks



The Modem 112K operates full duplex and features manual sound speed switching. Line equalization and filtering methods eliminate both distortion and line noise often found in microwave/satellite networks. Diagnostics include analog loopback, DTE loopback, and data test. The modem offers a CCITT V.35-compatible interface. An integral multiplexing option permits two-port operation, each port having a 56-kbit/s data rate. Other options include elastic buffer and alarm relay. Price is $16,500. **Racal-Milgo,** 8600 NW 41st St, Miami, FL 33166.
Circle 271

Data-switching capacity increases in large data network

The PACX IV SE data-switching system has a 100-percent increase in bandwidth. The switches serve as large centralized switches or as nodes in the Pacnet data communication network. With this 19.6-Mbit/s capacity, the system can handle up to 2048 attached devices. Microboard design enables units to provide up to 1024 data channels operating simultaneously at 9600 bits/s (asynchronous) and 19.2 kbits/s (synchronous). **Gandalf Data Inc,** 1019 S Noel, Wheeling, IL 60090.
Circle 272

Modem uses parallel interface to ease design configuration

The XCOM modem is Bell 212A compatible. With the parallel interface baud rate, it is independent and therefore requires no host intervention to adjust between different rates. This permits automatic selection of baud rates. Other versions are available for use with the Apple, TRS-80/2000, S-100-based systems, and the PCjr. **Delta Communication Products, Inc,** 3213 Ramos Cir, Sacramento, CA 95827.
Circle 273

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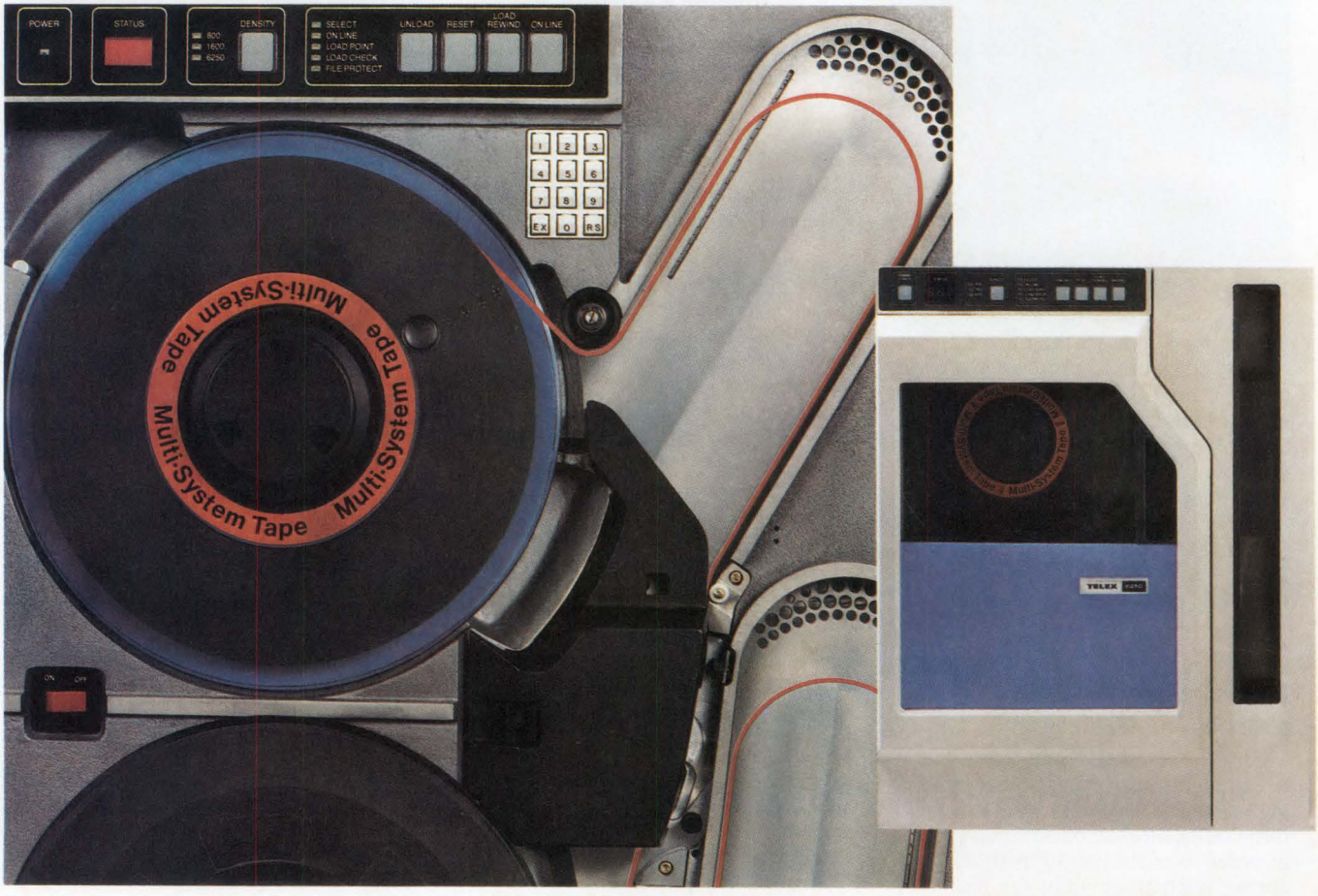
The new Telex 9250 tape subsystem

Finally! Full-Performance GCR Made Affordable. Telex Shamrock



It took Telex to introduce a GCR subsystem with all the performance, all the reliability of larger subsystems — and make it affordable for minicomputer and mid-range mainframe manufacturers.

The Telex 9250 GCR tape drive is the first 50 ips unit to appreciably lower the cost of GCR without sacrificing performance. Advanced LSI gate array technology and vacuum column design offer advantages like low cost, low power and low noise (before offered only on old tension arm systems) — plus all the performance that only vacuum column technology can deliver, including . . .

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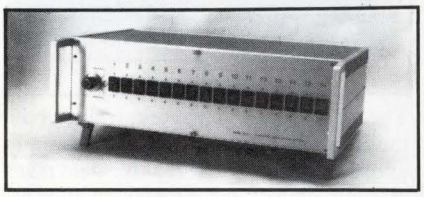
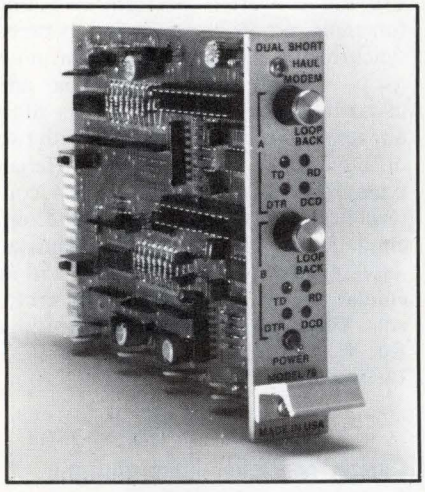
CIRCLE 109

Switcher has 16 channels for information display systems



Designed for IBM 327X-type systems, the 9316 accepts inputs from display stations and either switches them in bulk to controller A or B, or switches them in a preprogrammed mix between two controllers. When in mix mode, individual channels can be switched. All channel connections to the display stations and controllers are made at the rear panel via male BNC coaxial two-stud lock connectors. Channel-to-channel isolation is maintained. Price is $1050 as rackmount and $1100 as desktop. **Electro Standards Laboratory, Inc,** PO Box 9144, Providence, RI 02940.
Circle 274

Short-haul modem incorporates independent handshaking



A high density package offering bidirectional handshake/control signals, the model 79 provides full-duplex operation at speeds to 19.2 kbaud. Distances are up to 10 mi over two twisted pairs. Designed for asynchronous operation, the network cabling must provide dc continuity and be of the nonloaded type. Handshake/control signal is implemented by the DTR and DCD pin. Transmission between models is via ±12 mA current loop controlled by optocouplers. In quantities of 250, prices are $180. **Remark Datacom, div of Telebyte Technology, Inc,** 148 New York Ave, Halesite, NY 11743.
Circle 275

Full-duplex modem simultaneously handles voice and data

Enabling transmission of voice and data over one telephone line, the SPM-94B creates two data channels. One is in the forward direction, one in the reverse, all within a portion of the voice band. Data is transmitted at speeds to 300 bits/s. Five front-panel LED indicators monitor the unit's operation for system diagnostics. Interface modules are available in standard protocols with special modules available on request. **Coherent Communication Systems Corp,** 60 Commerce Dr, Hauppauge, NY 11788.
Circle 276

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Network performance monitoring merges with matrix switching

Identifying and correcting network problems and analyzing network performance, the Intelli-MAX runs on one CRT. Dynamic rotational monitoring checks critical portions of networks continuously while monitoring less crucial lines on a rotational basis at user-defined intervals. The device produces color graphics displays of up to seven layers of network activity. The system displays network activity minute by minute and in 5-min color trends. It will also verify normal operation after corrective action on the network has been taken. Fully configured systems start at $61,400. **Data Switch Corp,** 444 Westport Ave, Norwalk, CT 06851.

Circle 277

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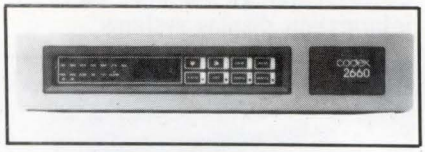
High speed modems use the 68000 as a controller



The 2600 series features trellis-coded modulation for improved performance above 9600 bits/s and reliable data transmission up to 16.8 kbits/s. Automatic speed adjustment to changing line conditions is designed for maximum throughput. Built-in network control monitors and tests lines and devices directly from the control panel or from a central site control system. The modems have integral dual-dial restore with auto-call/auto-answer capability for dial backup in case of leased line failure. The series consists of three models for transmissions, ranging from 4800 bits/s to 16.8 kbits/s. **Codex, sub of Motorola Inc, Information Systems Group,** 20 Cabot Blvd, Mansfield, MA 02048.

Circle 278

Protocol converters network multiple hosts and mixed computer types

Tru/Blu converters perform switching functions, as well as conversions between synchronous EBCDIC and asynchronous ASCII, speeds, and coaxial cable and RS-232 interfaces. These functions allow one terminal or printer to work with two or more host computers of different types. Model 74 emulates a 3274 controller, 78 allows PC to provide full-screen emulation of 3278 terminal, 87 adapts an ASCII printer to coaxial cable, and 80 emulates 3780, 2780, 2770, and 3774 protocols. **Timeplex, Inc,** 400 Chestnut Ridge Rd, Woodcliff, NJ 07675.

Circle 279

Cluster controller links multiple hosts, PCs, and terminals

The Netway 274 multidissimilar host controller supports up to 16 workstations and connects up to 5 multipoint and 16 point-to-point connections. It includes a floppy disk system for loading system software configuration information, a parallel printer port, and optional networking software. The controller supports 3270 BSC, SNA/SDLC, Burroughs poll/select, and asynchronous start/stop protocols. Prices start at $9150 with a typical configuration at $12,510. **Tri-Data,** 505 E Middlefield Rd, Mountain View, CA 94043.

Circle 280

CIRCLE 111

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PAC-139

CIRCLE 112

High resolution CRT displays over 8000 characters

The 15-in. M38-200 resolves the equivalent of 3000 TV lines (3.9 million pixels) in a scanning area of 7⅞ x 10⅝ in. It is available in standard P-4 (white) and P-31 (green) phosphors with approximately 46-ft-L brightness for use in high ambient light. A special deflection coil reduces distortion and deflection defocusing, and eliminates raster pincushion effects. The tube and deflection unit combination is designed for use in both vertical and horizontal screen formats. Price is $575. **Amperex Electronic Corp, Slatersville Div,** Providence Pike, PO Box 278, Slatersville, RI 02876.
Circle 281

Wideband operational amplifier settles in 70 ns to 0.01 percent

The AM-1435 provides high open-loop gain (100 dB), flat frequency response beyond 10 kHz, and a 6-dB/octave rolloff beyond 100 MHz. Gain bandwidth product is typically 1 GHz and slew rate is 300 V/μs. DC characteristics include 1-MΩ input impedance, initial offset voltage of ± 2 mV, and input offset voltage drift of ± 5 μV/°C. Minimum common mode rejection ratio is better than 80 dB, and full power frequency is 8 MHz minimum. Prices in 100s range from $68 to $102. **Datel,** 11 Cabot Blvd, Mansfield, MA 02048.
Circle 282

Thin-film recording heads designed for Winchester drives

Developed specifically for 8-, 5¼-, and sub-5-in. Winchesters, the Cyber 100 series is based on advanced air bearing and suspension technology. If features an inductive read/write transducer, and is directly deposited on a ceramic slider via a proprietary semiconductor-like process. Units come as slider/suspension or head/arm assembly. The heads operate at track densities ranging from 345 to 1200 tracks/in. Resolution is in excess of 70 percent, at flux densities of 8000 to 15,000 flux changes per inch. In evaluation quantities, price is $1000 for 10 heads. **Cybernex Corp,** 6580 Via Del Oro, San Jose, CA 95119.
Circle 283

SOFTWARE

Micro-mainframe link provides full file-transfer capabilities

Via software addition, the dual processor-based (Z80/8088) TC3278 terminal converter transforms an IBM 3278/3178 into an intelligent workstation. The software runs in the CMS, TSO, and CICS operating environments and under DOS/VS, OS/MVS, or VM/370 operating systems. IBM files are accessible to all TC3278 units as a shared data base. The link connects coaxially between the terminal and cluster controller for both a nonintrusive Line mode and a Local mode for file transfer, personal computing, and software terminal connection to host. One-time charge for the IBM host environment is $500; $200 for each terminal converter. **Avatar Technologies Inc,** 99 South St, Hopkinton, MA 01748.
Circle 284

Graphics software packages provide high performance

Designed for use with NEC's advanced personal computer, the Designer package is one of four in a series. Each graphics system contains a graphics board and 128 Kbytes of RAM. Autocad software for the system allows a user to zoom at the rate of a trillion to one. Input is via keyboard, mouse, or digitizer, and output is to a pen plotter. Other software packages include an integrated spreadsheet, an executive system for graphics presentations, and a presenter for screen- and plotter-oriented presentations. Prices range from $1948 to $2258. **NEC Information Systems, Inc,** 1414 Massachusetts Ave, Boxborough, MA 01719.
Circle 285

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Protocol analysis software fully interprets SNA protocol

The SNA Trace software is specifically designed for use on the Chameleon—a portable data communication protocol analyzer/simulator. The software allows user access to line header, transmission header, request response header, and request response unit. Display options view the link unit components in hex and/or EBCDIC characters. The user can select traffic on only one address or all addresses. In addition, if any frame components are not immediately needed, they can be suppressed for later review. Entire hardware/software system is priced at $18,000. **Tekelec Inc,** 2932 Wilshire Blvd, Santa Monica, CA 90403.
Circle 286

Software package captures and lays out on single workstation

The Starline family consists of integrated, application-specific bundled software that runs on Apollo 32-bit workstations. Stardesigner features design capture and MOS logic simulation modules; Stargate has gate array design, MOS logic simulation, and layout; and Starcell contains cell design, simulation, and layout. Other packages provide PC board design with behavioral and functional simulation, as well as switched capacitor circuit design. All packages run under the control of a database management nucleus. Prices start at $41,000. **Silvar-Lisco,** 1080 Marsh Rd, Menlo Park, CA 94025.
Circle 287

Debugging tool works with Z8000, 68000, and 8086 CPUs

Designed to quickly and accurately aid in locating and correcting program bugs for microcomputer software, the debugger is aimed at realtime application software. Features are breakpoint control, symbolic debugging, register setting and display, symbol value listing, and single-step execution. In addition, it provides complete symbol management and a full expression analyzer. The debugger is available for use with the OS/RT realtime operating system, but will run under other operating systems. **The Destek Group,** 830 E Evelyn, Sunnyvale, CA 94086.
Circle 288

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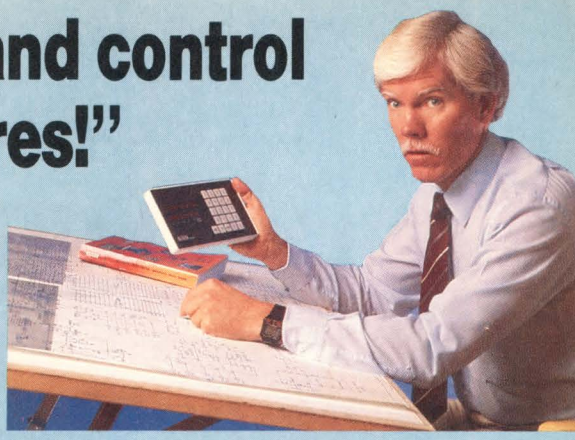

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Unix port to IBM PC-XT adheres to standards

UNX-II is an implementation of AT&T's Unix III with Berkeley 4.1 enhancements. It will be offered both in a bundled package and in unbundled form. The basic product includes the system III kernel, basic (Bourne) shell, and utilities. Hardware requirements include 320 Kbytes of memory and optional installation of an 8087 math coprocessor for enhanced performance. Optional utilities are PC-DOS shell and text processing utilities. Basic price is $595. **International Data Services,** 122 Saratoga Ave, Santa Clara, CA 95050.
Circle 289

Standard-cell layout system automatically places and routes

Cadicell CAD software places cells within a design and interconnects them. The portable software runs on Mentor's workstations as well as the VAX, IBM, and Apollo systems. Cadicell's interactive placement and routing tool is Cellgraph, which uses menus and automatic prompts. It offers interactive floor-plan generation and manipulation. Cells within the library can be created by text entry or graphics design. Users can enter cell information via keyboard or use a pointing device to draw cell characteristics onscreen. Available in the third quarter of 1984, price is $60,000. **Mentor Graphics Corp,** 8500 SW Creekside Pl, Beaverton, OR 97005.
Circle 290

Software package runs CAD/CAM on 32-bit processors

Interactive graphics capability is the heart of the exclusive 32-bit Unigraphics II. It has an associative data base that permits the user to establish and manipulate links among various information for automation of design, drafting, and manufacturing. A macro capability captures a sequence of menus and increases process speed. Other features include Fortran-based post processors, file management, drafting protocols, and multisurface machining. **McDonnell Douglas Corp,** 5552 Cerritos Ave, Cypress, CA 90630.
Circle 291

Software automatically converts PLAs to gate arrays

The Angop package accepts as input the logic equations defining a PLA design and produces as output a gate array net list. This net list is then processed on MDS's GateMark workstation. The workstation contains a library of structured cells and features 3-μm CMOS technology. The resulting gate array parts reduce power consumption while offering improved speeds. The software offers PLA benefits while lowering development costs and cutting design cycle time. **Matra Design Systems,** 2840-100 San Tomas Expwy, Santa Clara, CA 95051.
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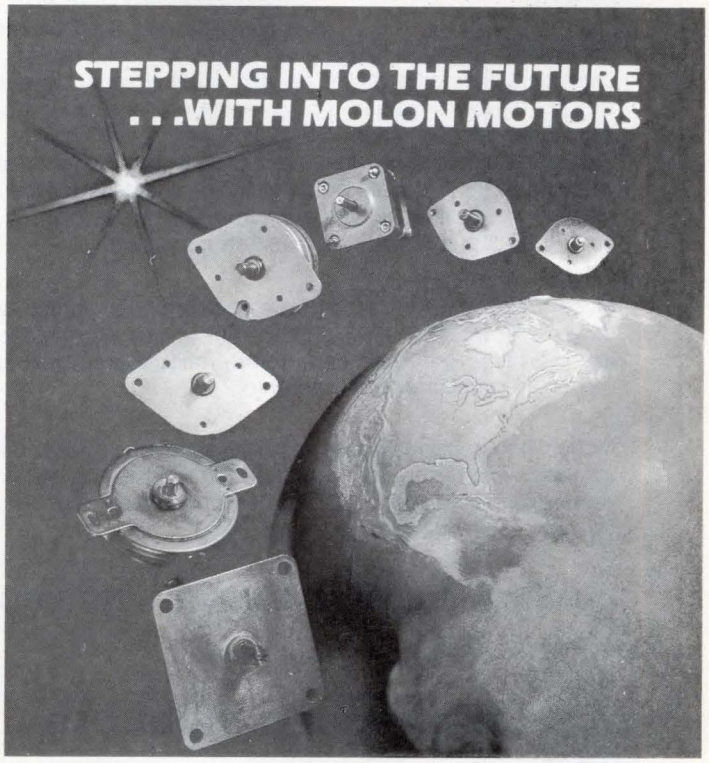

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CIRCLE 118

Single-board 68000-based computer runs on the STD bus

Running at 8 MHz, the 68008 processor provides a throughput of approximately 60 percent of the equivalent 8-MHz 68000. STD bus signals are buffered for easy expansion. The board features three 28-pin JEDEC sockets for a total of 32-Kbyte-wide onboard memory. An EPROM monitor is optionally available. Full 1-Mbyte 68008 addressing is available. Nonmultiplexed offboard addressing is implemented by 1 of 8 decoder/drivers that selects additional memory boards via a front connector. Baud rates can be individually programmed for each port. **Peopleware Systems Inc,** 5190 W 76th St, Minneapolis, MN 55435.
Circle 293

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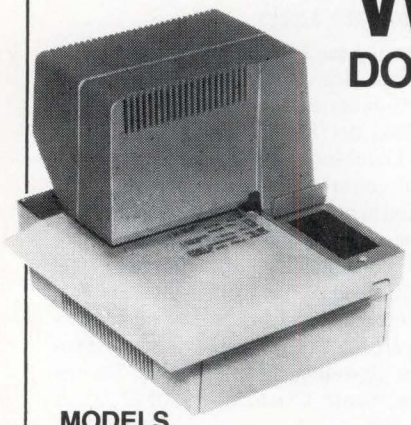

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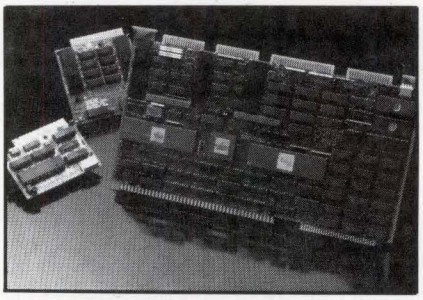
Single-board Unix system has half or whole megabyte



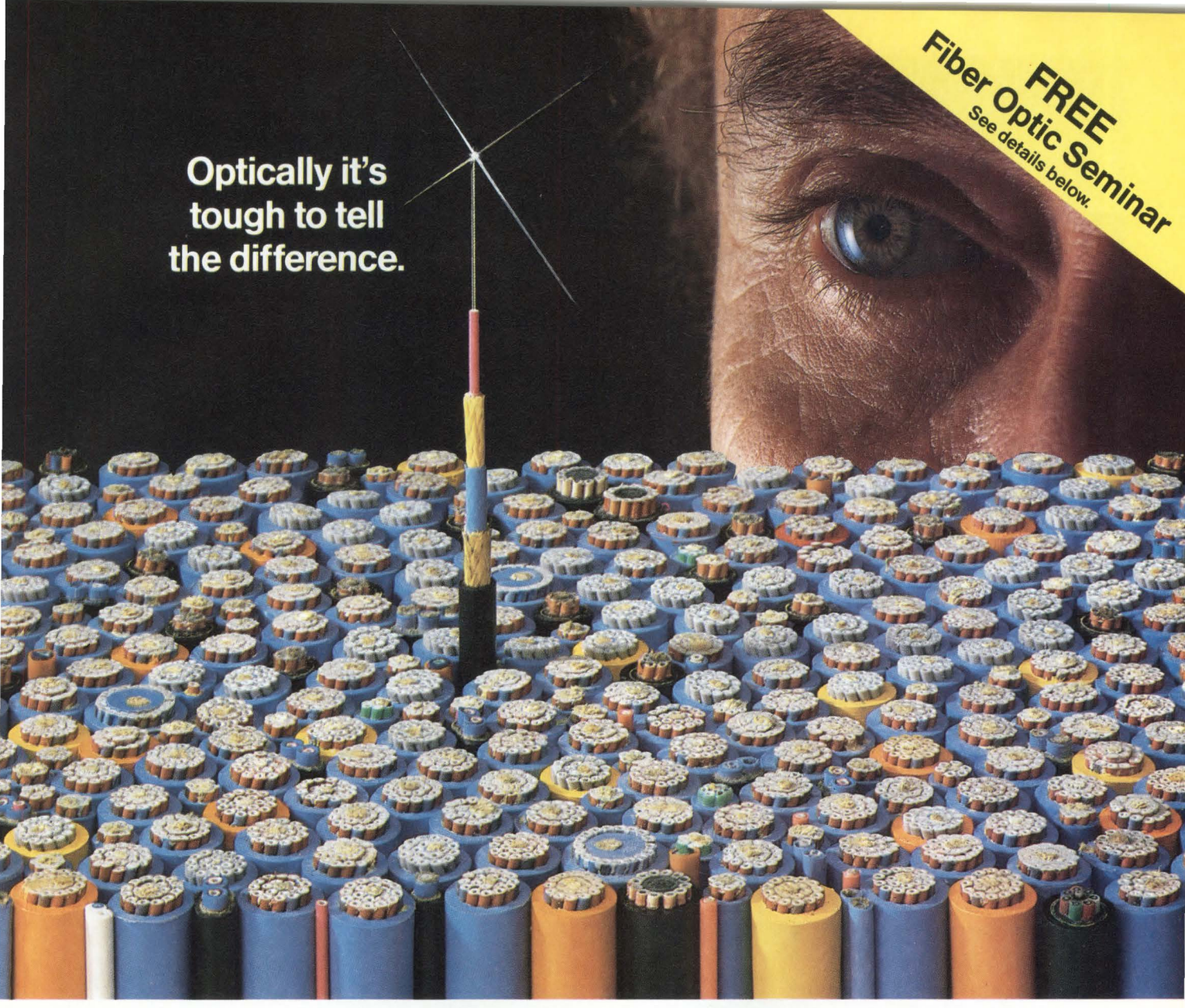
The HK68A includes Winchester and tape interface, four to eight serial ports, two iSBX I/O expansion plugs, one quad channel DMA, and MMU. Other features include 32 Kbytes of EPROM, user programmable LEDs, and three programmable 16-bit counter/timer channels. Currently supported are Unix System III and V with drivers for Ethernet, SDLC/HDLC, and floating point processors. Other operating systems include CP/M-86K, poly-Forth, and Regulus. **Heurikon Corp,** 3001 Latham Dr, Madison, WI 53713.
Circle 294

Two high performance processors are Z8000 and 68000 based

An iLBX interface for the Multibus gives two processor boards a high speed memory path. The boards support a demand-paged virtual memory operating system, and each offers a control circuit tailored to high speed operation. The Z8000 board runs at a clock frequency of 10 MHz, while the 68000 board runs at 12.5 MHz. A state machine uses a PROM as the sequencer to control all cycles on the boards. Complete bus vectored interrupts are supported, as well as normal level/edge triggered interrupts. **Central Data Corp,** 1602 Newton Dr, Champaign, IL 61821.
Circle 295

Virtual memory microcomputer is built on a single Multibus card

The 32-bit demand-paged GVC-16 is based on the NS16032 processor. It combines the complete NS16000 chip set with up to 2 Mbytes of RAM, Winchester disk interface, and peripherals for a multi-user system. Large onboard memory allows a 10-MHz CPU to run without wait states. Hardware floating point uses the 16018 FPU; up to 32-Kbyte EPROM is available. In a standard configuration, which includes 512 Kbytes of memory and the interrupt control unit, the price is $3295. **GVC Inc,** 222 Third St, Cambridge, MA 02142.
Circle 296



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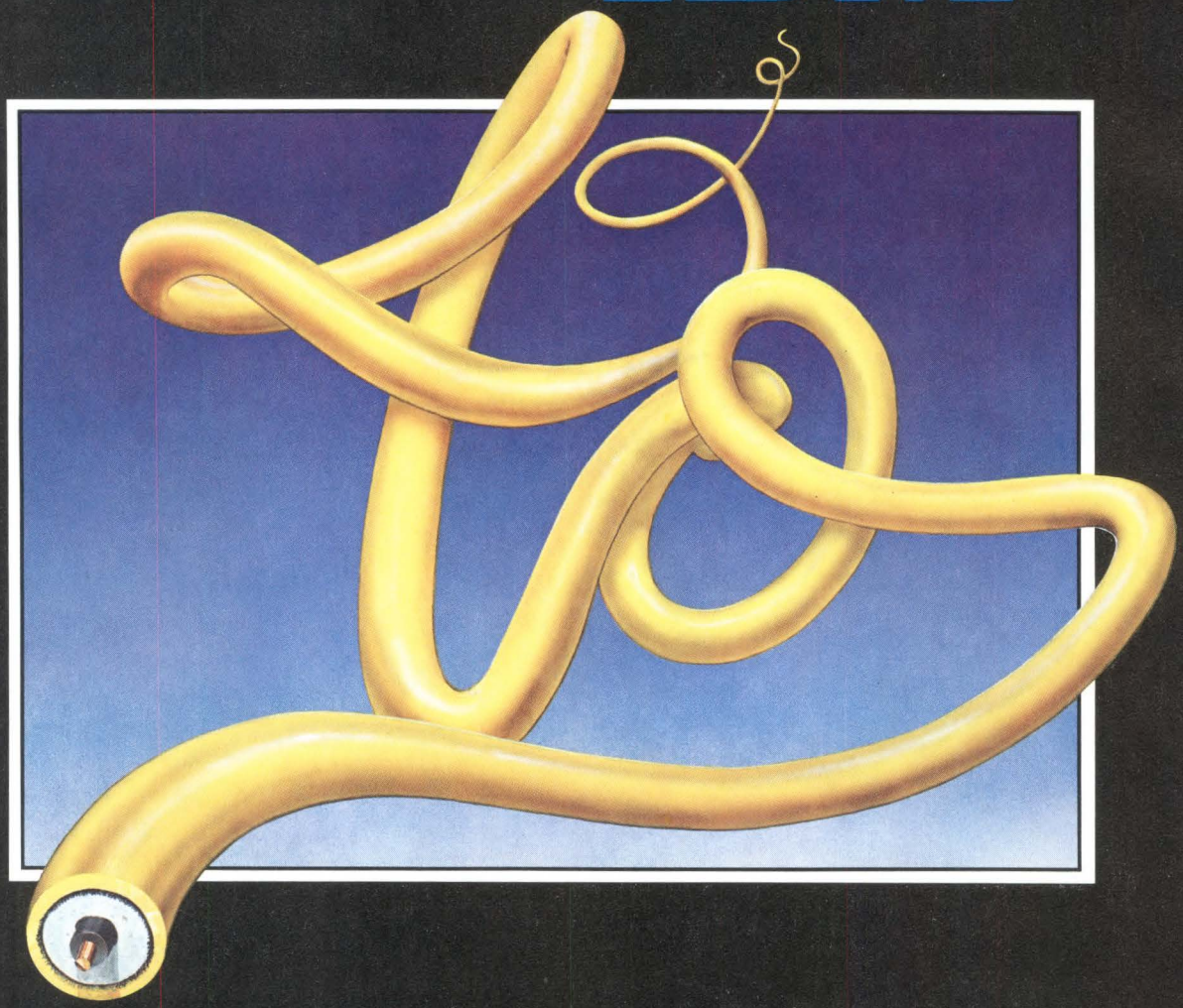

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CIRCLE 121

Single-chip microcomputer implements 16-bit instruction set

Configured either as an embedded standalone controller or an intelligent peripheral controller, the MK68200 offers high speed execution and code space efficiency. The instruction set includes bit manipulation, extensive BCD arithmetic, and high speed multiply/divide operations. The micro provides full-duplex USART capable of data rates of up to 1.5 Mbits/s. Three 16-bit multimode timers are provided for interval timing, pulse-width generation/measurement, and baud rate generation. In 100s, price is $75 each. **Mostek Corp, div of United Technologies Corp,** 1215 W Crosby Rd, Carrollton, TX 75006.
Circle 297

Telecom microcomputer comes on CMOS chip

The G65SC150 communication terminal unit is optimized for telephone line signaling and data transmission. The monolithic system integrates an 8-bit micro, 2 Kbytes of ROM, 64 bytes of RAM, a dual 26-step sine wave generator, 27 I/O lines, a timer, and two counters. Compatible with the 6500 and the 6800 bus structures, the product can operate as a standalone terminal or as an intelligent peripheral to another micro. Prototype units, without a programmed ROM, are available in 68-pin LCCs. In quantities of 100 or more, the unit price is $38. **GTE Microcircuits Div,** 200 W 14th St, Tempe, AZ 85281.
Circle 298

Multibus-compatible computer board achieves 10-MHz operation

A plug-in replacement for and software-transparent to Intel's iSBC*86/05, the Am97/8605/010 features serial and parallel ports, three counter/timers, and 8 Kbytes of static RAM. In addition, it provides sockets for up to 64 Kbytes of EPROM, three iSBX connectors, and an interrupt controller. The 16-bit board's power requirements are 5 V at 2.8 A, 12 V at 40 mA, and −12 V at 40 mA. Connectors allow a variety of SBX modules to plug in to change the board's function. Price in quantities of 1 to 9 is $1995. **Advanced Micro Devices Inc,** 901 Thompson Pl, Sunnyvale, CA 94086.
Circle 299

Single-board computer functions on the STD

The STD-145 8085A features a battery backed time-of-day, full-duplex serial USART port, 24-bit programmable parallel I/O and three programmable counter/timers. ROM/RAM implementations as small as 2 Kbytes or up to 64 Kbytes can be accommodated. Peripheral functions are I/O mapped, and occupy 32 consecutive locations in the map. A write only control port takes care of memory sockets 1 and 2 on/off, bus on/off, and boot enabled/disabled. Baud rates are programmable to 19.2 kbaud. Price is $325. **Micro-Link Corp,** 14602 N U.S. Hwy, Carmel, IN 46032.
Circle 300

CIRCLE 122

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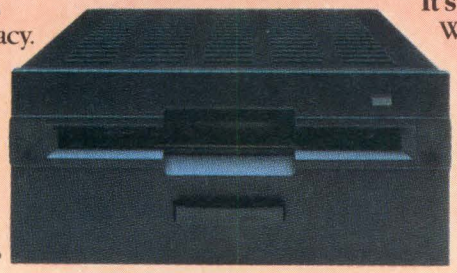

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The high performance 68000/68010-based VME-68K board allows up to 16 Mbytes of memory with no wait states at 12 MHz. This provides a 1.4-MIPS performance. Located on the CPU card are two programmable serial ports—one with modem control. The high speed memory management unit supports an 8-Mbyte logical process and up to 16 Mbytes of physical memory. Also available are an intelligent multifunction I/O card, an SCSI host adapter, a QIC-II tape host adapter, and a VME-compatible add-on memory card. **Integrated Solutions, Inc,** 1350 Dell Ave, Campbell, CA 95008. **Circle 301**

Peripheral functions and PC compatibility reside on CPU

The FE 6410 series 2-layer boards offer 64 or 128 Kbytes of parity checked RAM, 32 Kbytes of EPROM space, and both serial and parallel ports. BIOS software supports PC-DOS, MS-DOS, CP/M-86, and concurrent CP/M. The boards have the option of a floppy disk controller and/or monochrome video display controller integrated on the CPU board. External dimensions of the boards are physically identical to the PC CPU. Prices for the series run as low as $275 in quantity. **Faraday Electronics,** 1029 Corporation Way, Palo Alto, CA 94303. **Circle 302**

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CIRCLE 124

SYSTEM COMPONENTS/ COMPUTERS

Array processor system takes on multiple users' multiple tasks

Mini-MAP Plus 4 consists of up to four 32-bit floating point array processors interfaced to one VAX-11/780, /750, or /730. Each processor can be accessed by a separate user with different task requirements. The VAX can then accommodate four separate computation-extensive tasks simultaneously, each with 5 MFLOPS of processing speed. Basic configuration includes four array processors with 64 Kbytes of data memory packaged in a single 10.5-in. chassis. Software development tools are also provided. Price is $78,700. **CSP, Inc,** 40 Linnell Cir, Billerica, MA 01821.
Circle 303

Talk to the editor
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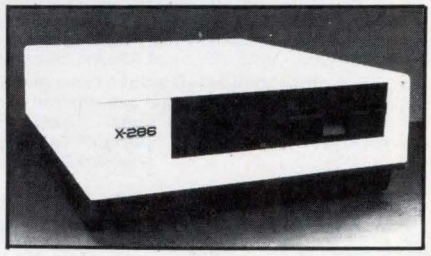
Desktop microcomputer internally processes 32 bits at a time

The 9002 can be used as a powerful desktop workstation for one user, or with its optional Xenix operating system as a host supporting up to three additional users through attached terminals. The processor is a 68000 with 32-bit registers and 16-bit data flow. Memory capacity is 128 Kbytes of RAM expandable to 5.2 Mbytes in 256-Kbyte increments, and 128 Kbytes of ROM. Four drives, either 5¼-in. 640-Kbyte or 8-in. 985-Kbyte type, can attach to the system. Computer is priced at $6495. **IBM Corp, Information Systems Group,** 900 King St, Rye Brook, NY 10573.
Circle 304

Supermicro implements Xenix on 80286 processor

The X-286 supports 5 users (expandable to 16) and incorporates the iAPX 286 processor, an 80-bit 80287 numeric co-processor, and 512 Kbytes of error detecting and correcting RAM. RAM is dual-ported between the Multibus and a private high speed local extension bus. The local bus allows access to offboard memory as if it were local. A micro-based terminal controller unburdens the host CPU by processing terminal interrupts, storing data in onboard, dual-ported buffers. The disk system includes a pipelined controller and either 65- or 140-Mbyte Winchesters with 30-ms average access times. Prices start at $15,900. **BDS, Inc,** 1400 Shepard Dr, Sterling, VA 22170.



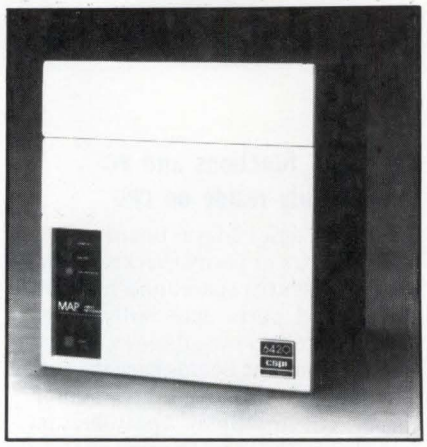
Circle 305

Virtual processor works in network and standalone applications

The 32-bit, Unix-based PowerNode 6000 is available in three versions: the 6030, packaged in a 30-in. tall cabinet with an integrated disk and tape; the 6050, in a 71-in. tall cabinet with ample space for a variety of disks and tapes; and the 6080, with an internal processing unit that handles computation bound tasks for the CPU. The architecture for the series is centered around a high speed bus with a throughput of 26.67 Mbytes/s. A 32-Kbyte, two-way set associative cache increases performance. Prices start at $80,000. **Gould Inc, SEL Computer Systems Div,** 6901 W Sunrise Blvd, PO Box 9148, Fort Lauderdale, FL 33310.
Circle 360

Array processor computes in double precision

Designed for scientific applications, the MAP-6420 floating point processor is based on a high performance parallel architecture with Fortran programming.



When interfaced to a host, it provides a programmable peripheral to offload numerical algorithms and execute them at greater speeds. The basic configuration has 4 Mbytes of memory and an independent control processor. Data memory is expandable to 64 Mbytes. The address space is 1 Gbyte. Floating point word size is 64 bits with 16 decimal digits of precision. **CSP Inc,** 40 Linnell Cir, Billerica, MA 01821.
Circle 307

Microcomputer system supports multi-user and application software

The high performance MTX-11 includes either 15.9 or 32 Mbytes of hard disk storage, 1-Mbyte DEC/IBM-compatible floppy disk drive, 256 Kbytes of memory, and four serial 9600-baud ports. Built around the LSI-11/23 16-bit CPU, the system can use the large library of PDP-11 software. The operating system accommodates large programs in memory; when available memory runs out, the operating system uses a priority and time-slice scheduling system to determine which jobs to swap to the Winchester. Transparent spooling allows the user to print files without degrading terminal response and program performance. **Scientific Micro Systems, Inc,** 777 E Middlefield Rd, Mountain View, CA 94043.
Circle 308

July Preview
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CIRCLE 125

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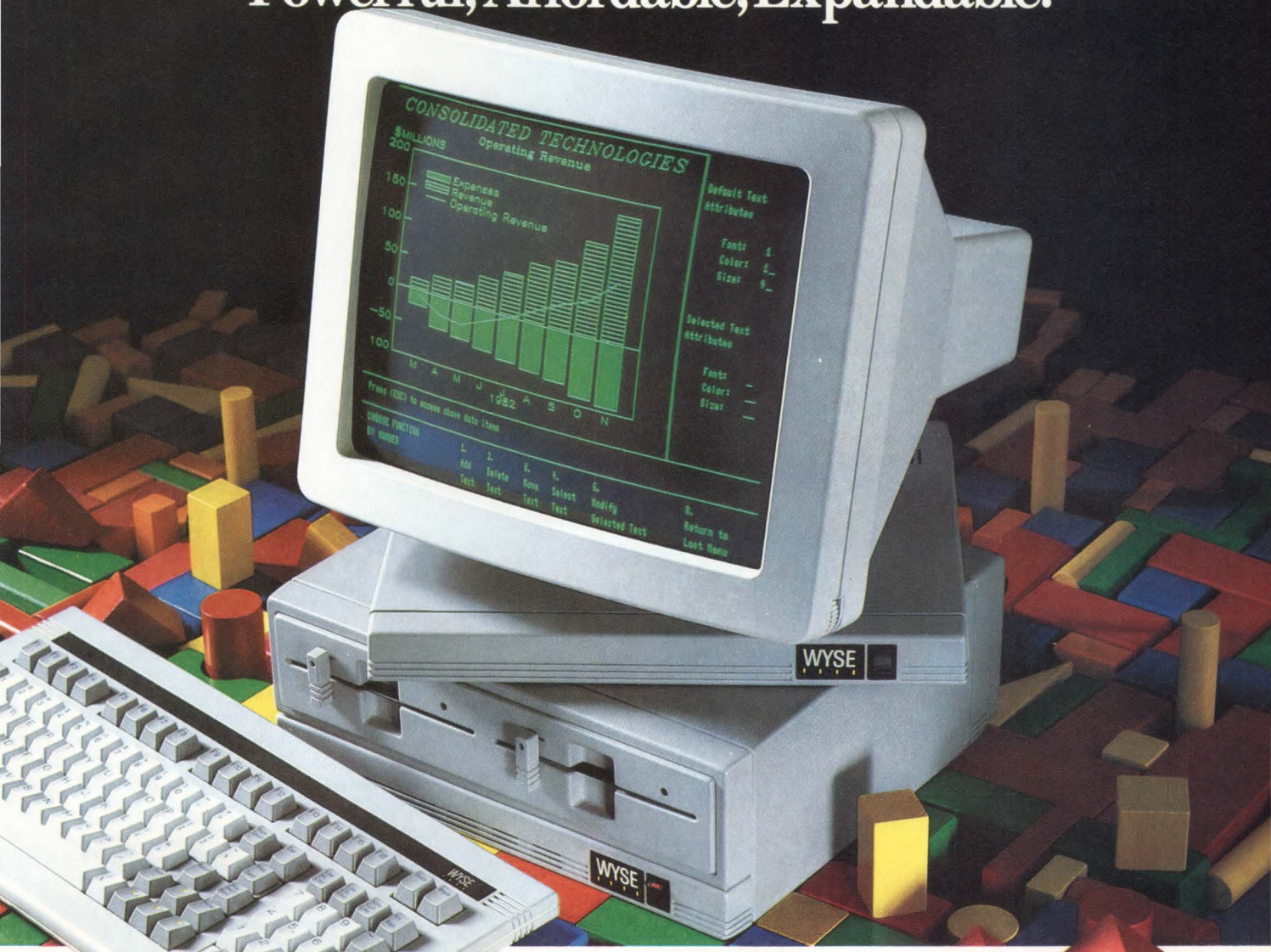

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CIRCLE 126

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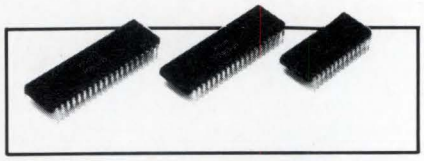
Keyboard encoder family simplifies hardware/software requirements



The KR9600 is an improved, single 5-V power supply version of the industry standard KR3600. The 9601 adds caps-lock and auto-repeat, while the 9602 is designed for detached keyboards and provides serial data output. The encoders automatically scan, debounce, and encode up to 90 single pull, single throw switches. They provide selectable n-key or two-key rollover. The 9600 and 9601 provide a parallel, TTL-compatible data output of up to 10 bits, as well as four operation modes in a 40-pin package. The 9602 comes in a 28-pin package. **Standard Microsystems Corp,** 35 Marcus Blvd, Hauppauge, NY 11788. **Circle 309**

Fast FIFO saves power without losing speed

TTL compatible, 67L401 has a fall-through time of 4 μs, yet consumes no more than 110 mA. The 5-MHz FIFO accommodates differing data rates, easing communications between computers and peripherals. The memory is organized as 64 words x 4 bits and can be cascaded to expand word and bit dimensions. Designed for asynchronous operation, it features structured pinouts, with outputs directly opposite inputs. The 16-pin chip, in 100s, is priced between $15.50 and $16.76 each. **Monolithic Memories, Inc,** 2175 Mission College Blvd, Santa Clara, CA 95050. **Circle 310**

Semicustom gate array operates at high speed and low power

Combining current mode logic with ECL 10K/10KH I/O cells, the HE2000 array is suited for mini, supermini, peripheral, and test instrument applications. It offers the functional equivalent of 2000 logic gates on a chip and has typically demonstrated internal gate delays of 300 ps while consuming 3.1 W. The HE2000 consists of 539 cells: 399 CML internal cells, 96 ECL to CML receivers, and 64 CML to ECL drivers. Nonrecurring engineering costs are approximately $40,000, including 10 working prototypes. **Honeywell Digital Products Center,** 1150 E Cheyenne Mountain Blvd, Colorado Springs, CO 80906. **Circle 311**

Nonvolatile memory family expands with 5-V RAM

The NCR 52002 NVRAM is a byte-wide device that operates from a single 5-V power supply. The 2-Kbit chip consists of a 256 x 8 RAM array with duplicate EEPROM array for backup. Typical access time is less than 300 ns. Maximum access times for commercial and military use are 300 and 450 ns, respectively. Number of possible store cycles is guaranteed to be at least 10^4 with one-year data retention. Each store cycle takes only 10 ms. Price is $18.70 each in quantities of 100. **NCR Corp, Microelectronics Div,** 8181 Byers Rd, Miamisburg, OH 45342. **Circle 312**

Small PROMs figure in random logic replacement

The 82S130A/131A are configured as 512 words of 4 bits and are function and pin compatible with industry standard 2-Kbyte PROMs. The 126A/129A are 256 words of 4 bits and carry 2 chip-enable inputs. The 23A and 123A have 32 words of 8 bits and carry 1 active-low chip-enable input. All parts have a 50-percent increased performance over their predecessors. Packaging options include plastic and ceramic DIPs. Prices range from $1.25 to $6.95 in quantities of 100. **Signetics Corp,** 811 E Arques Ave, PO Box 409, Sunnyvale, CA 94086. **Circle 313**

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Circuit modem meets Bell 212A and CCITT specs

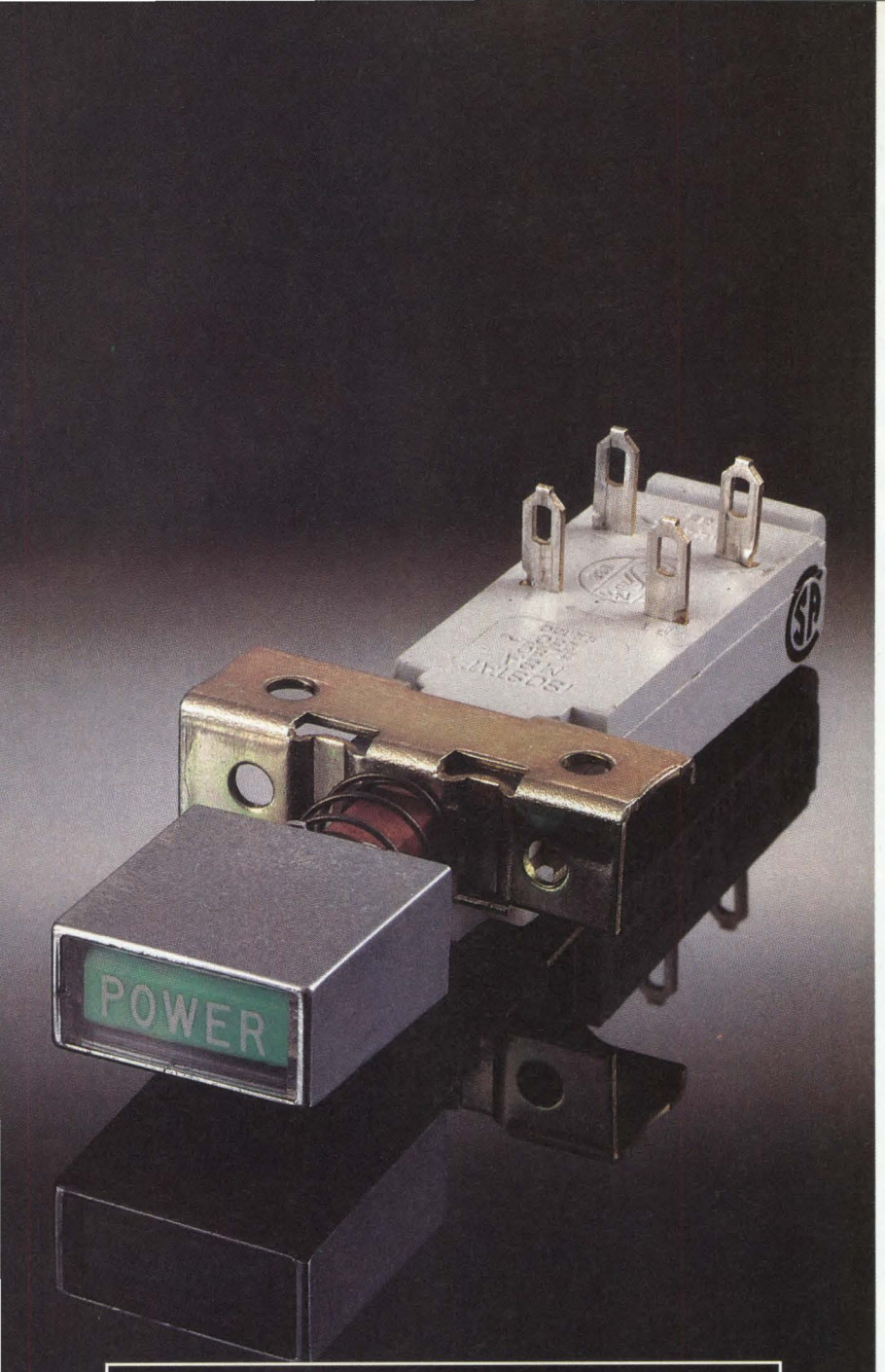
A 28-pin CMOS device forms the heart of a full-duplex, 1200-bit/s modem. The MP7223 requires a crystal-controlled clock, filters, and a line interface to emulate various modems. It uses phase shift keying modulation and digital demodulation. The chip is divided into three sections: demodulator, modulator, and timing control circuitry. A synchronized digital phase-locked loop maintains the basic timing and initiates all phase shift detection operations. Prices range from $15 to $27, depending on quantity. **Micro Power Systems, Inc,** 3100 Alfred St, Santa Clara, CA 95050. **Circle 314**

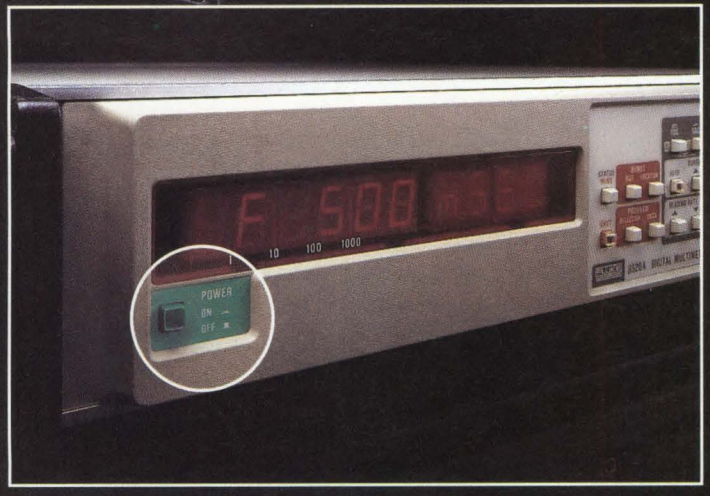
Dynamic RAMs feature 100-ns and 250-ns access times

Organized in 65,536 single-bit words, the F4164 family of 64-Kbit devices operates on a single 5-V source. The chips have low capacitance, TTL-compatible inputs that employ overshoot and antistatic protection to ensure data and address input integrity. With an unlatched output at cycle end, the unit allows for page boundary extension and 2-D chip selection. Operation modes include random write or read, read/write, read/modify/write, and page cycles. In 100s, the prices range from $11 to $13. **Fairchild Camera and Instrument Corp, Microprocessor Div,** 450 National Ave, Mountain View, CA 94024. **Circle 315**

Logic circuits combine transceivers with latches

Two circuits—the ZX74HCT/LS646 for transmitting noninverted data and the 648 for inverted data—ease high speed multiplexed data transmission. Maximum propagation delay is 25 ns and 80 mA is the quiescent supply current. Both are fully TTL equivalent, providing a 12-mA drive current at 0.4 V and 24 mA at 0.5 V. Each chip features two D-type flipflop latches and offers six control inputs: output enable, direction, two clocks, and two data-source selections. Devices are priced at $4.25 in 100-unit lots. **Zytrex Corp,** 750 E Arques Ave, Sunnyvale, CA 94086. **Circle 316**





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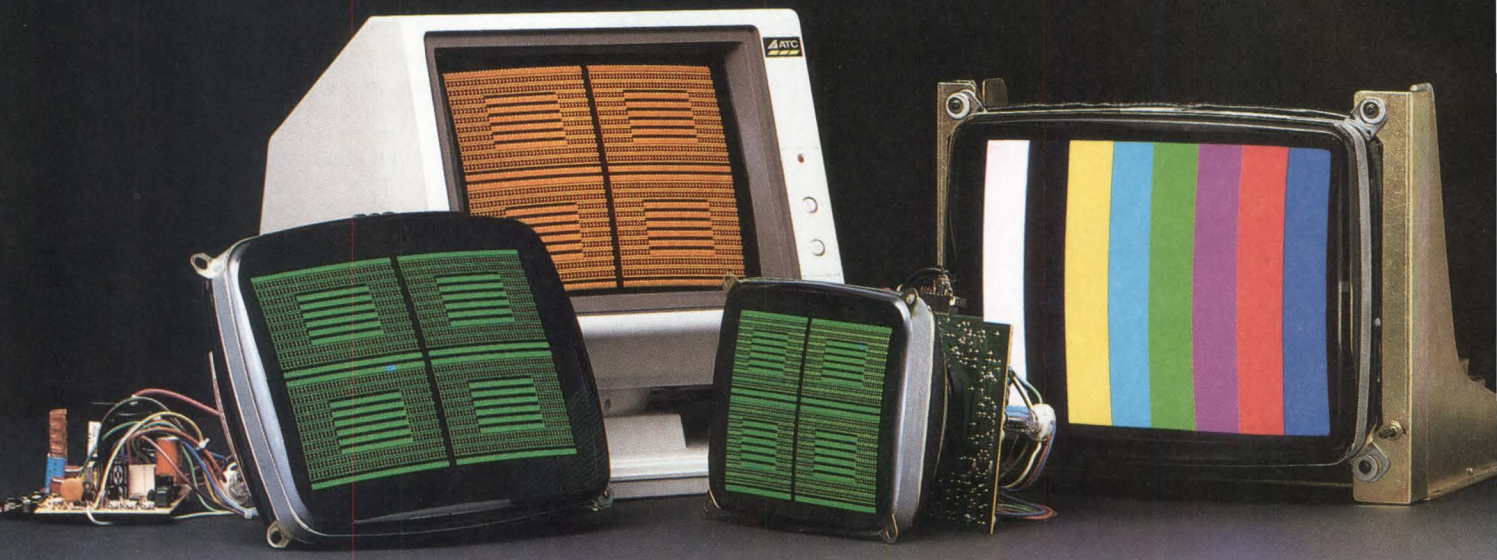

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CIRCLE 128

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Static RAMs speed at 55 ns in address access specs

The HM6287 is a 64-Kbit device organized as 65,536 words by 1 bit. The TTL-compatible RAM runs from a single 5-V supply and consumes 300 mW in operation and 100 μW in standby. The HM6267 is a 16-Kbit device that has an address access time of 35 ns. High speeds are attained via a 2-μm design rule and Hi-CMOS technology. Also contributing to high speed is the provision of address-pulse transition detector circuitry. **Hitachi America, Ltd,** 1800 Bering Dr, San Jose, CA 95112.
Circle 317

Dynamic RAM multiplexes address inputs for standard packaging

The MCM6664B/65B is a 64-Kbit device organized as 65,536 one-bit words. Complete address decoding is done on-chip with address latches incorporated. Both devices have $\overline{RAS}$ only on refresh mode. The 64B version has the automatic refresh control function available on pin 1, providing two additional modes of refresh, automatic and self-refresh. All inputs and outputs, including clocks, are TTL compatible. Data out is controlled by $\overline{CAS}$, allowing system flexibility. Prices range from $7.80 to $8.65 in 100s. **Motorola Inc, MOS Integrated Circuits Group,** 3501 Ed Bluestein Blvd, Austin, TX 78721.
Circle 318

Multiplying D-A converter contains onboard data latch

As a replacement for the AD7545, the MP7645 precision monolithic 12-bit DAC interfaces directly to most 12- and 16-bit bus systems. Its data latch is loaded by a single 12-bit wide word. Data loads into the input latch under the control $\overline{CS}$ and $\overline{WR}$ inputs. Gain error is 2 ppm/°C maximum with output capacitance at 50 pF maximum. Amplifier offset sensitivity is 330 μV/mV. Typical applications are in data acquisition, process control, and industrial control. The chip is offered in 20-pin plastic or ceramic packages, with prices ranging from $11.20 to $38.10. **Micropower Systems, Inc,** 3100 Alfred St, Santa Clara, CA 95050.
Circle 319

Worst-case access times are 250 ns in 256-Kbit ROMs

Made with proprietary Selectox silicon gate CMOS technology, the SMM6325 and 6326 use 1/5 the operating power and 1/10,000 the standby power of comparable NMOS parts. The devices are pin compatible with industry standard 61256 and 23256 types, respectively. Customer's EPROMs from breadboarding and system verifications are used to communicate programs. The data in the EPROMs is converted by computer into the metal mask patterns of the finished ROM. Both devices are $10.65 at the 10,000-piece level. Mask charge per program is $2800. **S MOS Systems, Inc,** 50 W Brokaw Rd, San Jose, CA 95110.
Circle 320

Controllers place terminal functions on one circuit

Providing complete display and memory control, the CRT 9028 and 128 video terminal logic controllers interface directly to 8085, Z80, 8051, and 6500/6800 micros. Each features a video timing generator and controller, character generator, graphics generator, video attributes controller, video-shift register, and memory controller. The chips have 32-, 64-, and 80-col displays with up to 25 data rows. Display features include bidirectional smooth scroll, wide and thin graphics, and user-programmable character fonts. Prices in 100s are $22.50. **Standard Microsystems Corp,** 35 Marcus Blvd, Hauppauge, NY 11788.
Circle 321

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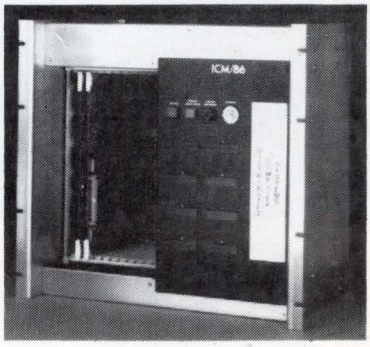

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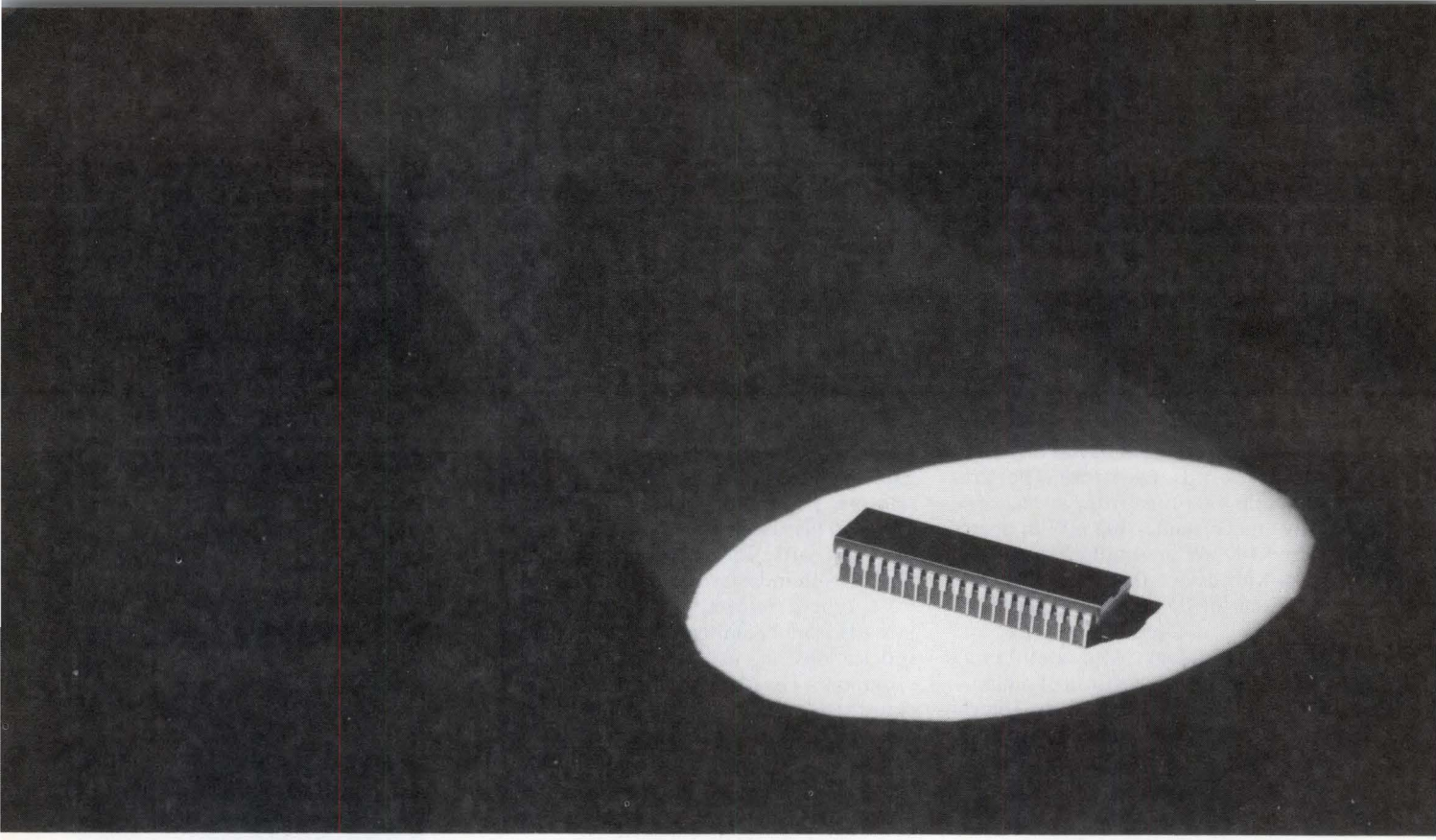

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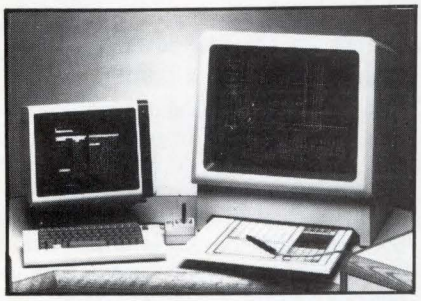
High resolution CAD system offers two monitors



The Cascade X provides a standard 12-in. monochrome CRT as well as a 19-in. nonglare monitor with 1024 x 798 resolution. The dual monitors allow the user to view the menu on one screen and draw on the other. The system uses a 68000 microprocessor backed by 756 Kbytes of RAM for nearly instantaneous processing of graphics input. Up to eight workstations can be networked. The complete unit also includes keyboard, tablet, joystick, 5 Mbytes of hard disk storage, and a 5¼-in. floppy. **Cascade Graphics Development, Inc,** 1000 S Grand Ave, Santa Ana, CA 92705.
Circle 322

Instrumentation mainframe solves logic problems with plug-in modules

The COLT 300 is a virtual instrument with a slot that accepts a single plug-in instrumentation module. Various modules allow state or timing, universal or micro-specific logic analysis, in-circuit emulation and digital pattern generation. The device's mainframe includes two 5¼-in. floppy drives that load a module's program, data files, and setups. Also included are two RS-232-C ports, parallel printer port, and IEEE 488 bus interface. Base cost is $9500. **Dolch Logic Instrumentation, Inc,** 3052 Orchard Dr, San Jose, CA 95134.

Circle 323

Software resolves CAD interface by simplified data sharing

The CAD-VANTAGE software runs on the HP 3065 and extracts data from CAD systems for use in the test area. Instead of depending on CAD-supplied postprocessors, this approach takes standard CAD outputs and reformats them in the test system. It adds terminal-emulator software routines for accessing CAD systems and supports nine-track mag tape interface. Once a data transfer process is complete, the in-circuit program generator can test a board in a fraction of the time required by many conventional test systems. Prices range from $5000 to $10,000, depending on configuration. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.
Circle 324

Mainframe graphics capability extends to IBM PC and XT

A combination software and board package, Forte-Graph allows a PC or XT to act as a full-function color graphics terminal linked to an IBM mainframe. It provides enhanced emulation of an IBM 3279 model S3G terminal with programmed symbols and seven colors. While online, individual text or graph screens can be captured for printing or storage. Hardware consists of program symbols option board, which mounts on an emulator adapter board called the Forte-PJ. Together the boards occupy one expansion slot. Forte-Graph is priced at $2590. **Forte Data Systems, Inc,** 1500 Norman Ave, Santa Clara, CA 95050.
Circle 325

Multiprocessor system links mainframe and graphics

The Lynxystem 1000 series attaches to a Control Data Cyber 170 channel permitting the attachment of interactive graphics devices. System software dynamically downloads the micro at run time according to the application requirements. It is based on a high speed bus that has two to five single-board 68000s, each with 128 Kbytes of dual-ported memory, two serial ports, and an I/O expansion bus. The recommended minimum configuration is priced under $25,000 including software. **Lynxys, Inc,** PO Box E, West Lafayette, IN 47906.
Circle 326

Unix tools link to software development for range of microprocessors

With development for micros including 8086 and 68000 and operating systems including MS-DOS and CP/M, the Workshop allows programs to be developed on computers running under Unix, Xenix, or Berkeley 4.1 operating systems. Workshop operates by linking Unix tools to cross-development and host target communication software. All programs are developed under Workshop on the host and are tested on the target system. Source code can either be passed across as text or compiled code output by the cross-development tools on the host. **Logica,** 64 Newman St, London, England W1A 4SE.
Circle 327

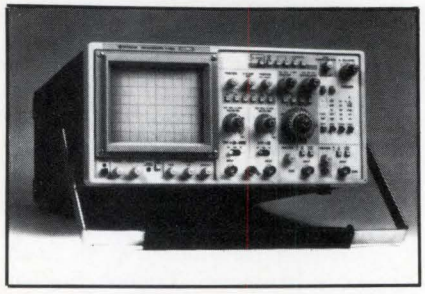
Workstations provide fast interactive solids modeling

The PowerStation 3100 and 5100 systems include a minicomputer, high resolution color graphics terminal, and mechanical CAD/CAM software. The devices have numerical control capabilities so tool paths can be simulated on the solids representations, not just on the outline drawing. The 3100 is based on a 16/32-bit computer, while the 5100 is based on a 32-bit virtual processor. Both workstations are Unix based and use a mechanical CAD/CAM package. Prices start at $69,900 with dual systems, while the 5100 ranges to $152,500. **Gould Inc, Computer Systems Div,** 6901 W Sunrise Blvd, PO Box 9148, Fort Lauderdale, FL 33310.
Circle 328

Printed circuit board for CAD/CAM system is priced low

Supporting up to 16 workstations, the series 300 network system allows simultaneous independent design tasks. It links to workstations over a fiber optic local area network. The system is configured around a system manager with associated 12-in. terminal and full ASCII keyboard. The processor is a 15-MHz DEC LSI-11/73 with 32-bit internal architecture. The unit can produce all design and fabrication PC board documents; all wire list/bill of material input is subject to comparison checking. Prices start at $35,000. **Paragon Technology Corp,** 2199 Norse Dr, Pleasant Hill, CA 94523.
Circle 329

Microcomputer is central to portable oscilloscope



The V-1100 features CRT readout that displays frequency counter and DVM functions as well as constant ground level display. The 100-MHz unit shows the measurement of voltage value between ground level and reference cursor or two cursors and the time difference between two points. Additional features include quad channel with independent position controls, 8-trace with alternate sweep, maximum sweep time of 2 ns/division, and variable hold off. **Hitachi Denshi America, Ltd,** 175 Crossways West, Woodbury, NY 11797.
Circle 330

Alignment disk supports 3.5-in. Sony standard

A single-sided disk compatible with both the 600-rpm Sony machine and the 300-rpm Shugart machine provides head alignment control for data interchange between flexible storage subsystems. The disk is available in quantity with a double-sided version coming soon. **Dymek Corp,** 1851 Zanker Rd, San Jose, CA 95112.
Circle 331

Tell us what you like
Did you remember to rate the articles in this issue of Computer Design? A special editorial score box is provided on the Reader Inquiry Card.

Measurement plotting system enhances and simplifies lab graphics

Combining the benefits of digital plotters, waveform and X-Y recorders, and data acquisition systems, the 7090A provides 1 Kword x 12 bits of buffer as a waveform recorder. Also in this capacity it has a 30,000-sample/s A-D converter on each channel with sine response at 3 kHz. As an X-Y recorder, it offers three high-sensitivity CMRR inputs of X-Y or Y-T recording. The unit can also plot when connected to a controller or smart instrument. Six pens in 10 different colors and two line widths are available. Cost is $4400. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.
Circle 332

Development station converts PC to engineering workstation

The PC7 closely links the Step-7 firmware integration test station with the IBM PC. It takes extensively used disk files and puts them onto RAM disk in the PC, reducing file access times. Using the PC as a host computer, it is possible to define bit-slice designs, assemble programs, format object code, and debug microcode. To provide 1-key operation, the 10 function keys on the PC keyboard now replace the most heavily used multi-character commands. Prices range from $10,000 to $25,000. **Step Engineering,** 757 Pastoria Ave, Sunnyvale, CA 94086.
Circle 333

Computer prototyping board builds add-on interfaces

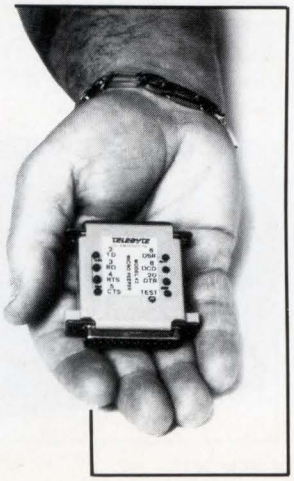
The eZ board is a solderless experiment system. Features include a glass epoxy PC board mounted with a set of solderless breadboarding units for building circuits. Four separate distribution buses with 50 tie-points each can be used for power, ground, clock lines, and reset commands. The breadboarding area consists of 1460 tie-points with a capacity of sixteen 14-pin DIPs. Components with lead diameters up to 0.032 in. plug in and connect with ordinary solid hookup wire. Price is $174.95 each. **S.E. Corp,** PO Box 1132, Yorba Linda, CA 92686.
Circle 334

System for CAE/CAD designs custom integrated circuits

Generating both logic and layout for custom ICs, Chipgraph IC editor speeds up and simplifies VLSI design. It supports user-defined links between logic and layout hierarchies as well as top-down and bottom-up methodologies. The system's variable-screen windows provide simultaneous viewing of logic and layout. The system provides both symbolic and composite (mask-level) capture of layout information and automatically converts the symbolic designs to mask level. The layouts can be mixed on a cell-by-cell basis for optimal speed within chip requirements. Price is $50,000, with availability in the third quarter of 1984. **Mentor Graphics Corp,** 8500 SW Creekside Pl, Beaverton, OR 97005.
Circle 335

Data line monitor determines status of major RS-232 signals

The low cost model 42 Micropeeper provides a LED display to check the seven main signals and an eighth user-selectable signal. The device monitors transmit data, receive data, request to send, clear to send, data set ready, data carrier detect, and data terminal ready. The monitor is equipped with female and male type DB-25 connectors and is transparent to the operation of any standard interface since all 25 leads are passed through. In 100s, price is $43 each. **Telebyte Technology, Inc, Remark Datacom Div,** 148 New York Ave, Halesite, NY 11743.



Circle 336

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For operator convenience, the ADM 1178 terminals come with a full tilt and swivel monitor that stops positively in any position, an easy-to-read non-glare screen, and a detached, low-profile DIN standard keyboard.

The ADM 1178s are available with a standard 12″ green or amber screen and an RS-232C serial printer port. They can be easily modified for OEM applications and are available with such options as 14″ green or amber screen, answerback memory, current loop or RS-422 interface, and international character sets.

These Lear Siegler High Touch terminals are made in America-designed, engineered, manufactured and shipped from Anaheim, California. With this total, on-shore capability, and a complete worldwide network of sales and service centers, OEMs as well as end users can be assured of the best local support available in the industry.

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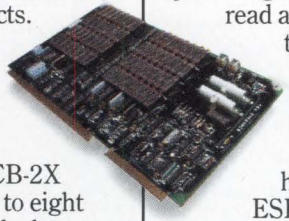
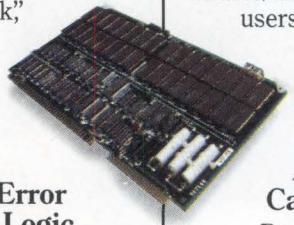


MCB-364

Superior Dynamic Memory Relocation.

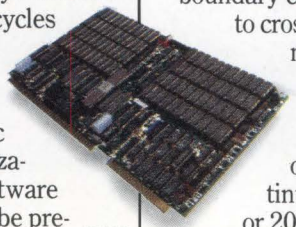
The new MCB-2X can relocate up to eight 64K or 256K blocks independently—making it a very powerful tool for "RAM disk," graphics display or multiple table look-up applications.



MCB-332

Expanded Error Correction Logic.

All single bit errors are automatically scrubbed during refresh cycles without system interruption. And thanks to the automatic memory initialization feature, software doesn't have to be preconditioned.



MCB-512

On-board ECC detects all single and double bit errors, while providing 370ns read access through standard 64K or 256K RAMs. Plus, the MCB-2X has CSR and ESR interrogation capability and software control of ECC enable/disable, allowing users to provide comprehensive system-level diagnostics.

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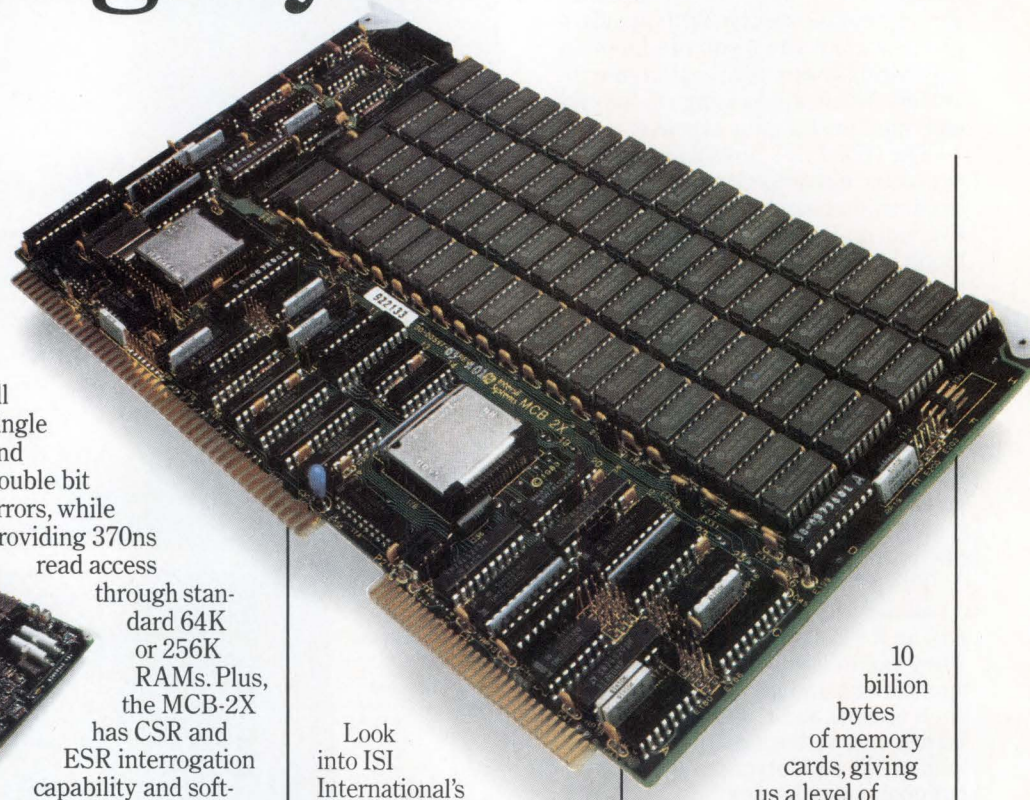
Board addresses starting on any 4K boundary can be mapped to cross 1 and 4 megabyte boundaries. The MCB-2X can also occupy a continuous 512K or 2048K memory space within its 16 megabyte range.



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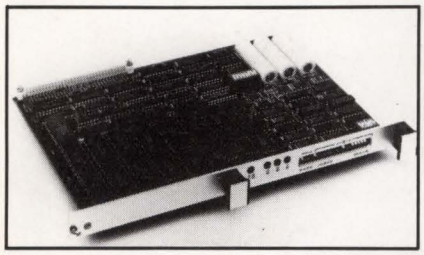
CIRCLE 133

Nonvolatile VMEbus board provides calendar/clock



Providing 128, 64, or 32 Kbytes, the MM-6500C employs low power, 8-K x 8 or 2-K x 8 CMOS static RAMs. Three redundant, onboard, parallel, and separately fused backup batteries ensure reliable operation in the event of power failure. Both lithium and NiCad batteries are available. Rechargeable NiCads provide three-month data retention; nonrechargeable lithium batteries permit five-year retention. Realtime calendar/clock provides programmable, periodic, switch-selectable interrupts that occupy 32 locations in the memory map. Other features include 24-bit addressing up to 16 Mbytes, cycle and address time of 220 ns, and variable delays. The 128-Kbyte version is $1175. **Micro Memory, Inc,** 9436 Irondale Ave, Chatsworth, CA 91311.
Circle 337

Removable cartridge Winchesters are IBM-XT compatible

The Micro-Magnum 11/11 and 11R feature an 11-Mbyte cartridge. Track density has increased to 908 tracks/in. with 9254 bytes/in. Fully retracted heads never touch the disk surface, protecting the media and heads from damage and wear. The self-sealing drives prevent contaminants from entering critical areas of the head disk assembly. The cartridge is protected by a spring-loaded door, which covers the head access and air exit ports when not in use. In 1000s, the 11/11 drive is priced at $1525; the 11R is $1190. **DMA Systems Corp,** 601 Pine Ave, Goleta, CA 93117.
Circle 338

Hard disks and floppy backup combine in one storage module

The Discovery 1604 storage array accommodates up to four 5¼-in. Winchesters and four minifloppies or superminifloppies. A power sequencer automatically powers up the Winchesters sequentially. Four independent access arms result in throughput greater than a single-arm drive. Initial release is of CP/M Plus and dpc/os 3.0 systems in limited configurations. The tabletop version is priced at $3700, including one 22-Mbyte Winchester and a 40-Kbyte floppy. **Action Computer Enterprise, Inc,** 430 N Halstead St, Pasadena, CA 91107. **Circle 339**

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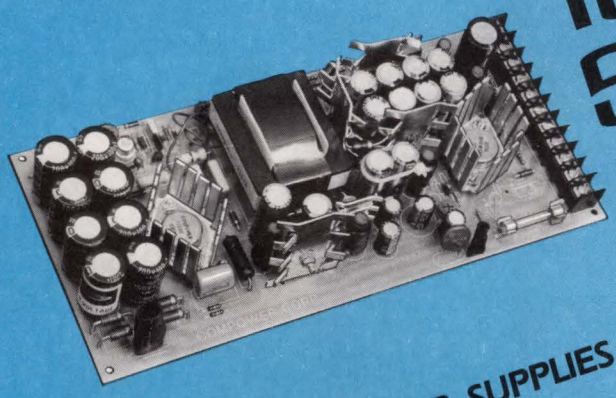

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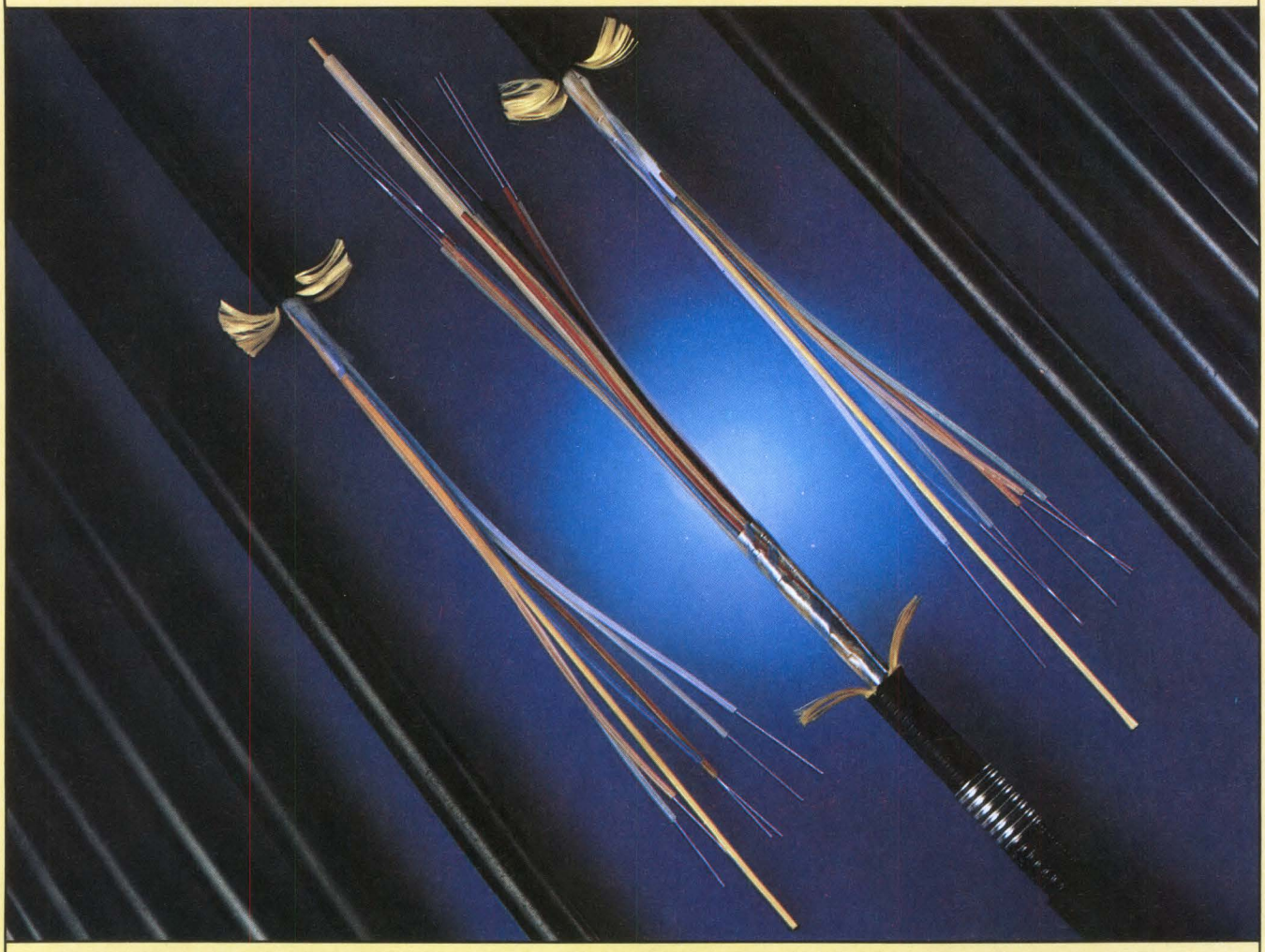
CIRCLE 134

STRAIGHT.....



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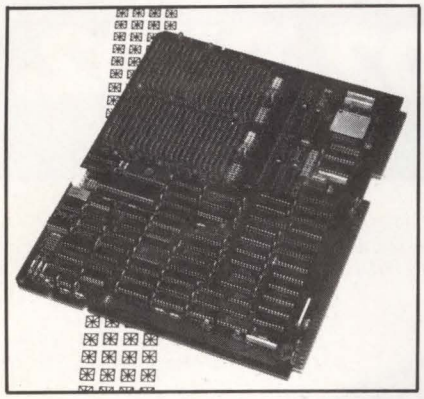
CIRCLE 135

Error detection and correction occurs on 1-Mbyte Multibus board



The EDMB series features dynamic memory boundary relocation, serial communication port, interleaving on bank level, and onboard processor. EDC can detect and correct single-bit, double-bit or multiple-bit errors. Configuration flexibility to the host CPU is through I/O commands. The processor supports transparent memory scrubbing, distinguishes hard and soft errors, and does error stats. Both the ½-Mbyte and 1-Mbyte versions operate on 5 V with typical read access times of 250 ns and maximum write access times of 130 ns. The 1-Mbyte version is approximately $4000. **Electronic Designs, Inc,** 35 South St, Hopkinton, MA 01748.
Circle 340

Data storage and backup subsystem saves space

The free-standing DataTower is a combined 8-in. disk drive, intelligent controller, and streaming tape drive. A main system component, the DS-101 intelligent controller handles most processing required to support data storage peripherals through five basic commands. The unit features a disk-drive defect management system, plus the ability to perform concurrent backup during normal system use. The system uses a 45-Mbyte streamer and an 86-Mbyte drive. **Priam Corp,** 20 W Montague Expwy, San Jose, CA 95134.
Circle 341

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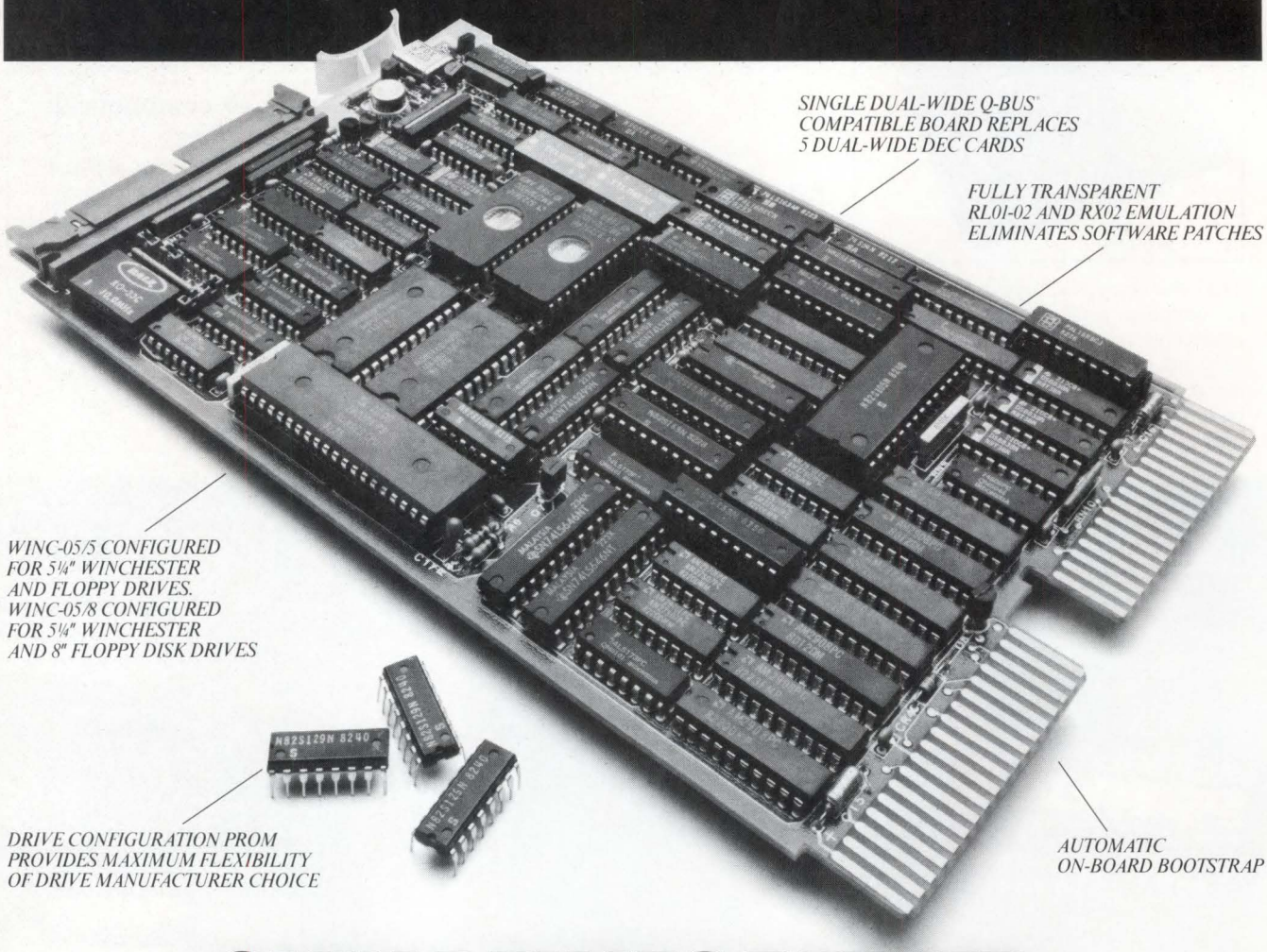

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CIRCLE 137

Controller configures in simple PID or more complex fashion

The MOD 30 is a universal micro-based instrument that works as a simple controller with alarms, or as a controller with feedforward/feedback and adaptive reset. Software resides in 72 Kbytes of PROM. Eleven major function blocks contain all the parameters and conditions necessary for cooperation and control. Up to 500 entry parameters can be applied to a given control loop or function. The configuration data base allows the control strategies without PROM burning or rewiring. **Taylor Instrument, a div of Combustion Engineering, Inc,** PO Box 110, Rochester, NY 14692.

Circle 342

Hardware/software package provides industrial graphics

The Classicmate II can be paired with General Electric Series Six programmable controllers to provide a complete man/machine interface for process control. It integrates the 2200 terminal featuring bubble memory, with an easy-to-use graphics development package. It eliminates the need for user software programming to link the graphics to the PC. By keyboard and display, an operator can monitor and change variables in a process controlled by the PC. **Industrial Data Terminals Corp,** 173 Heatherdown Dr, Westerville, OH 43081.

Circle 343

Programmable controller expands memory size

Offering increased user logic storage, the 884A-200 contains from 2000 to 3500 nodes of relay ladder logic. It provides storage for over 1000 numerical registers and an additional 1024 on/off (discrete) variables for a total memory capacity of nearly 5000, 16-bit words. Features include battery backup for CMOS RAM with capacity for a minimum of 35 weeks without power. A memory-protect keyswitch prevents unauthorized program changes. Memory security option provides four-level pass-code system in which the pass-code levels start with monitoring functions and progress to configuration programming. Cost is less than $2000. **Gould Inc, Programmable Controller Div,** PO Box 3083, Andover, MA 01810.

Circle 344

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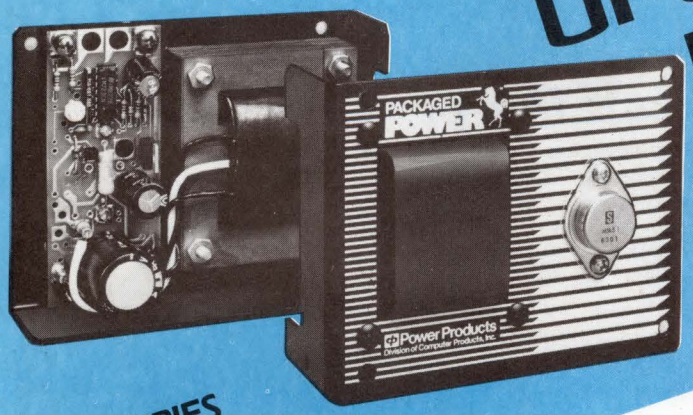

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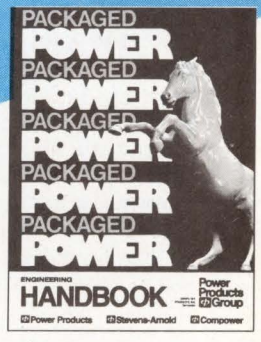

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Half the price.

Next compare the FP-2000 against the old industry standard for reliability. After evaluations, large OEMs have reported reliability every bit as good, print quality better, and the price almost half. They have also found comprehensive diagnostics, modular construction, IBM plug compatibility, and a quiet, compact design engineered for ease of use, ease of service and low-cost of ownership.

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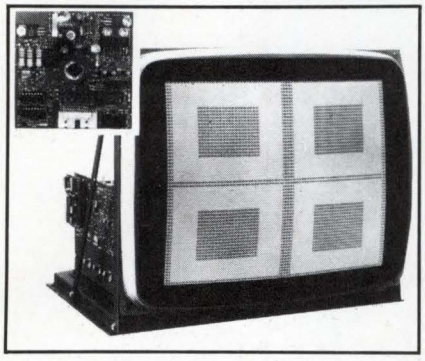
CIRCLE 139

Monitor interface addresses FCC emission test



High resolution, VR-Series 20-in. monitors have a horizontal frequency of 31 to 68 kHz. The raster-scan device displays up to 1100 noninterlaced lines refreshed at 60 frames/s. The display runs at a pixel level of up to 100 MHz. At that point, the video has a rise/fall time of 40 ns using either ECL or TTL inputs. It provides 100 lines/in. at 60 Hz or 200 lines/in. in both vertical and horizontal dimensions. **Moniterm Corp,** 7160 Shady Oak Rd, Eden Prairie, MN 55344.
Circle 345

Workstation is compatible with DEC computers

Full-featured display station WY-75 incorporates the ANSI X3.64 standard and is fully software compatible with the VT-100. The alphanumeric display station is a smart editing unit that features a 14-in. screen with nonglare green phosphor and user-selectable 80- or 132-col widths. The video module has a fully tilting and rotating display. Keyboard is detached and has 16 programmable function keys with 32 separate control codes. It also includes a nonvolatile memory that eliminates the usual DIP switches. Cost is $795. **Wyse Technology,** 3040 N First St, San Jose, CA 95134.
Circle 346

User-friendly voice entry improves 327X productivity

The VS1000 provides voice data entry, local user screen formatting, and help center facilities. It reduces data entry keyboard activity by allowing users to simultaneously enter/access data while performing other job functions. With total IBM host transparency, no host programming changes are required. Specs include a vocabulary of up to 300 utterances for each local user screen, realtime word identification, and better than 99-percent accuracy for digit entry. It communicates with 3274/6 controllers via coaxial A and allows either 3278/9, 3178, IBM PC, or VT100 displays to be used. Price is $7500. **Sphere Technology, Inc,** 222 Richmond St, Providence, RI 02903. **Circle 347**

Synthesizer module adds natural sounding speech to Multibus

The EV-8950 module is based on the TI 5220 voice synthesis processor, which places little demand on the host CPU. It also contains a standard voice synthesis memory chip. The chip is a 128-Kbit ROM featuring either the 206-word industrial vocabulary or optional vocabularies. The data is compressed by linear predictive coding techniques and drives the processor on a time-varying electron digital filter model of the human vocal tract. **Symbicon Assocs, Inc,** 89 Rte 101A, Amherst, NH 03031.
Circle 348

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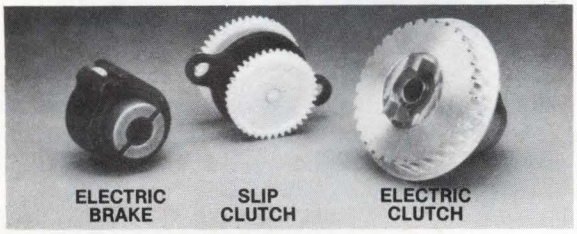

RPM clutches and brakes have solved many rotary motion problems for OEMs. That is our specialty. We design and manufacture our products to meet your special performance needs. Of course, we also offer standard units.

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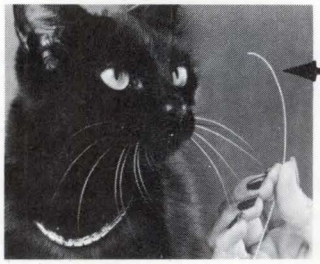
RPM offers free analysis of your OEM clutch and brake applications requiring up to 50 in-lbs. of torque.

CIRCLE 140

ZEUS SUB-LITE-WALL™ HEAT-SHRINK TUBING



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Inert! Highly dielectric. Slippery. Abrasion-proof. Permanent. Stands temps to 500°F. Uniform ID's down to .001"; thin-walls to 1.5 mils. Heat-shrinkable or permanently extruded around wires to AWG 44. Available expanded to heat-shrink ratios of 4 to 1 around irregular shapes, delicate equipment, to encapsulate against damage or corrosion. Special requirements welcome. IF YOU CAN USE IT, ZEUS MAKES IT!

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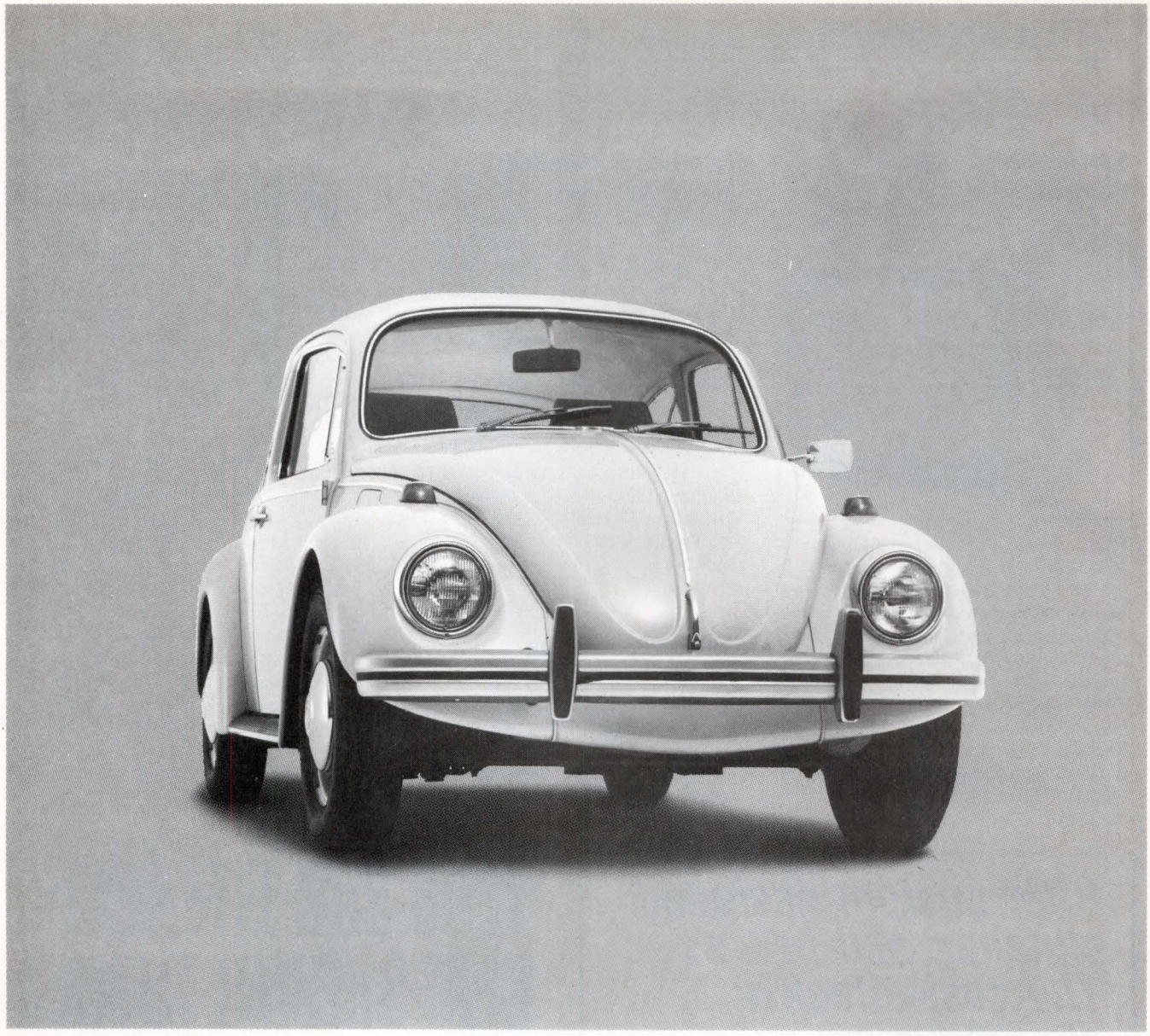
CIRCLE 141



Get a bug if you find a bug.

Show us a bug in our VRTX® real-time operating system and we'll return the favor. With a bug of your own to show off in your driveway.

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Since VRTX is the only microprocessor operating system completely sealed in silicon, finding a bug won't be easy.

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And since it's delivered in 4K bytes of ROM, VRTX will perform for you the way it's performing in hundreds of real-time applications from avionics to video games.

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Describe your application and the microprocessors you're using—Z8000, Z80, 68000, or 8086 family. We'll send you a VRTX evaluation package, including timings for system calls and interrupts. And when you order a VRTX system for your application, we'll include instructions for reporting errors.*

But don't feel bad if in a year from now there isn't a bug in your driveway.

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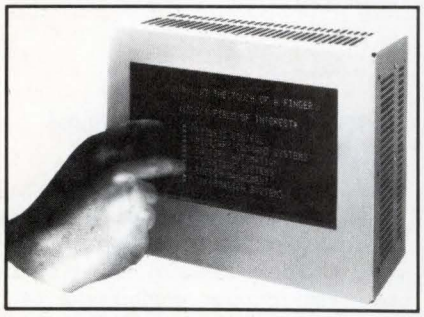
Operating Systems in Silicon.

*Call or write for details. But, considering our taste in cars, you might want to accept our offer of $1,000 cash instead. © 1983 Hunter & Ready, Inc.

CIRCLE 142

Touch-interactive display develops 480 orange or green characters



The VuePoint II has 12 lines x 40 chars and a 12-line x 20-col optical touch screen with up to 240 touch points. The gas plasma display has a standard three-page memory expandable to 7, 19, 35, or 51 pages. Smart features include multiple touch response formats, auto-scroll, protected fields, multiple blink rates, dual intensity, and random cursor positioning. Other features are menu setup of self-test, baud rate, and audible feedback. Regular single quantity price is $2295. **General Digital Corp,** 700 Burnside Ave, East Hartford, CT 06108.
Circle 349

Display stations feature IBM 3278/79 compatibility

The 3179 color and 3180 monochrome displays provide a modifiable keyboard with layouts that can be defined with a 3274 control unit. Standard workstation features include highlighting, reverse image, and tilt and swivel. The 14-in. terminal displays 1920 alphanumeric characters in either four or seven colors. The 3180's display, when attached to a 3274 control unit, can be changed to accommodate four format options from 1920 to 3564 alphanumeric characters. Prices range from $2195 to $2295. **IBM Corp, Information Systems Group,** 900 King St, Rye Brook, NY 10573.
Circle 350

Intelligent terminals offer high performance at low cost

Featuring soft setup using nonvolatile RAM, the Ovation 1041 and 1051 also provide firmware customization and expansion for custom logic. The 1051 has 256 graphics chars and 128 alphanumeric chars. Display formats are 80 or 132 cols. Standard 16 Kbytes of memory expands to 64 Kbytes. Based on the Z80A, the terminal off-loads functions from the CPU for faster response time. The 1041 is 8085A based and features 84 graphics chars and 8 function keys. The 1051 is $1295, while the 1041 is $1095. **Zentec Corp,** 2400 Walsh Ave, Santa Clara, CA 95050.
Circle 351

Color graphics pen plotter works with VAX computers

The LVP16 draws on either plain paper or transparencies and offers a choice of 6 colors from a palette of 10 (for paper) or 7 (for transparencies). The plotter provides graphics with 0.001-in. accuracy, at a maximum speed of 15 in./s. It weighs 16 lb, and is designed for installation on desktop or stand. With a standard RS-232 interface, the unit can communicate with systems that support the HP-GL protocol. Once pens are loaded, color selection is totally under software control. Price is $1995. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754.
Circle 352

Graphics terminal provides APL capability and text editing

In graphics mode, the 16GRF/APL is Tektronix 4010/4014 and PLOT 10 compatible, with a 240- x 640-bit mapped display resolution. A transparent printer port transmits data in LA102/LA34 format. APL mode can be accessed any time by entering the shift out code. The terminal has four resident character sets in addition to APL—line drawing, mosaic, superscript/subscript, and ASCII. Macro keys can be encoded with any alternate characters or sequences. The standard 12-in. model lists at $2940. It is also available in 9- and 15-in. styles with amber, green, or white CRTs. **Teleray,** PO Box 24064, Minneapolis, MN 55424.

Circle 353

THE $2395 DEVELOPMENT SYSTEM

Turns any personal computer into a complete microcomputer DEVELOPMENT SYSTEM. Our integrated control/display program runs under PC/MS-DOS, CP/M, or TRS-DOS, and controls the UDL via an RS-232 port.

Up to 128K bytes of **ROM EMULATION** (8K standard) allows you to make program patches instantly. Since the target ROM socket connects data and address lines to both the analyzer and the emulator, no expensive adaptors or personality modules are needed.

The powerful **BUS STATE ANALYZER** features four-step sequential triggering, selective trace, and pass and delay counters. $99 symbolic trace disassemblers are available for Z-80, 8048, 6500, 6800, 8031, 8085, 3870, Z-8, 1802, 8088, & 8086.

The **PROM PROGRAMMER** also doubles as a **STIMULUS GENERATOR.** For a brochure and list of cross assemblers call or write:
172 Otis Ave., Woodside, CA 94062
(415) 851-1172
ORION Instruments

CIRCLE 143

Graphics/imaging systems display medium resolution

Expanding the 9460 and 9465 lines, the terminals offer 640- x 512-pixel resolution supporting high performance graphics processing with medium resolution. Through a context-switching feature, either system can share its graphics controller and have multiple workstations perform independent graphics and/or imaging operations from a single host interface. Features include local pan and zoom, arithmetic image combinations, logical image manipulation, and entity detection. Prices start at $10,450. **Ramtek Corp,** 2211 Lawson Ln, Santa Clara, CA 95050.
Circle 354

Touch-sensitive monitor targets small computer use

The Point-1 monitor allows users to select from menus, position the cursor, and create and manipulate graphics by touching the screen. Resolution is 1024 x 1024 touch points. It includes a 12-in. monochrome CRT and an intelligent controller, as well as an RS-232-C port for communication. The screen technology incorporates a sandwich constructed of two transparent resistive sheets that detect touch by measuring voltage drops. Either green or amber phosphor displays are available. Price is under $665. **Micro-Touch Systems, Inc,** 400 West Cummings Park, Woburn, MA 01801.
Circle 355

Smart video display terminal enters at low end

The Freedom 110 features tilt and swivel styling, a detached 94-key DIN standard keyboard with numeric keypad, and a nonglare green phosphor display. Amber display is optional. Standard are a 24 x 80 display, 10 programmable function keys, 15 thin-line graphics characters, and 8 editing keys. It emulates the TeleVideo 910, ADDS Regent 25, ADM 3A/5, and Hazeltine 1420. Setup modes are either full page or line, and character attributes require no display space. The terminal also provides built-in self-test. Prices range from $535 to $595, depending on quantity. **Liberty Electronics,** 625 Third St, San Francisco, CA 94107.
Circle 356

Terminal offers multifunctional data communications

The Sigma-Data 3200 provides three fully concurrent communication ports. Line protocols are Telex; TWX; DDD; and private wire protocols 81D1, 83B3, 85A1, and 8A1. The terminal combines a 14-in. amber CRT with dual 5¼-in. floppy disks storing 1.3 Mbytes. Features include preparation and editing of information for ongoing transmission, formatting of all messages, and verify with answer-back and auto-redial. Line speeds are up to 9600 bits/s. Word processing functions are multiformatted with split screen, and concurrent I/O. **Telecomet Inc,** 820 Second Ave, New York, NY 10017.
Circle 357

Speech inputs through universal interface with MS-DOS

Conversion of MS-DOS software packages to speech input occurs with the Oto-1* speech recognition system. The system consists of a single circuit board that plugs into any auxiliary slot in an IBM PC, PC-XT, or compatible. A proprietary firmware/software combination provides a transparent interface with the application program, allowing voice input to be used interactively with a keyboard or other data entry device. The system has a better than 98-percent word recognition accuracy and 16 Kbytes of RAM, expandable to 64 Kbytes. Single-quantity price is $795. **Microphonics Technology Corp,** PO Box 7411, Federal Way, WA 98003.
Circle 358

Host interface unit adapts SCSI to S-100 specs

This IEEE 696 board allows a system to talk to drives employing the SCSI standard. The SCSI handshake status information is decoded to simple signals. User-controlled, software-readable switch changes host device; multiple host adapters expand control of multiple disk drives. The board requires only 4 consecutive I/O mapped ports and has a 16-bit extended addressing mode. Interrupts are generated on read data or status from SCSI controller. Pricing in quantity is $80. **Inner Access Corp,** PO Box 888, Belmont, CA 94002.
Circle 359

Network controller hooks up with the STD bus

Control module for S871 provides STD bus users with a simple interface to ARCNET local area networks. Individual modules provide users with transparent network operation, control, and protocol in the passing of data within the ARCNET system. ARCNET networks support up to 255 nodes and data rates up to 2.5 Mbits. **Contemporary Control Systems, Inc,** 4949 Forrest Ave, Downers Grove, IL 60515.
Circle 363

Converter takes binary angle and gives BCD equivalent

The SBD227 accepts up to a 22-bit binary digital input angle and converts it into a 26-line BCD output with a resolution of 0.0001 degrees and a full-scale reading of 359.9999 degrees. The 3-state output is available in 4 bytes, allowing it to be compatible with an 8-bit data bus. Timing and control signals are not required. Conversion time is limited only by the propagation delays of the components used. It supplies sufficient output to drive 5 TTL loads. Single-unit pricing starts at $295. **Natel Engineering Co, Inc,** 4550 Runway St, Simi Valley, CA 93063.
Circle 361

Microprocessor-based printer buffer offers programmable functions

The EXS-PB module is EXORbus compatible and is connected between the computer printer port and the printer. The maximum character transfer rate is 10,000 chars/s, typical values are 1000 chars/s. Storage capacity is 131,000 chars. Programmable functions allow deletion and copying of files in the buffer, pause functions, and built-in self-diagnostics. In case of paper confusion, listing may be repeated from the beginning of the file. **Dataware,** Hamngatan 9, SF-22100 Mariehamn, Finland.
Circle 362

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It is the highest performance, most reliable 5¼" cartridge disk drive in the industry.

It features more resistance to shock and vibration than any other disk drive, fixed or removable.

Its cartridge is the least expensive among formatted 5-megabyte cartridges on the market today.

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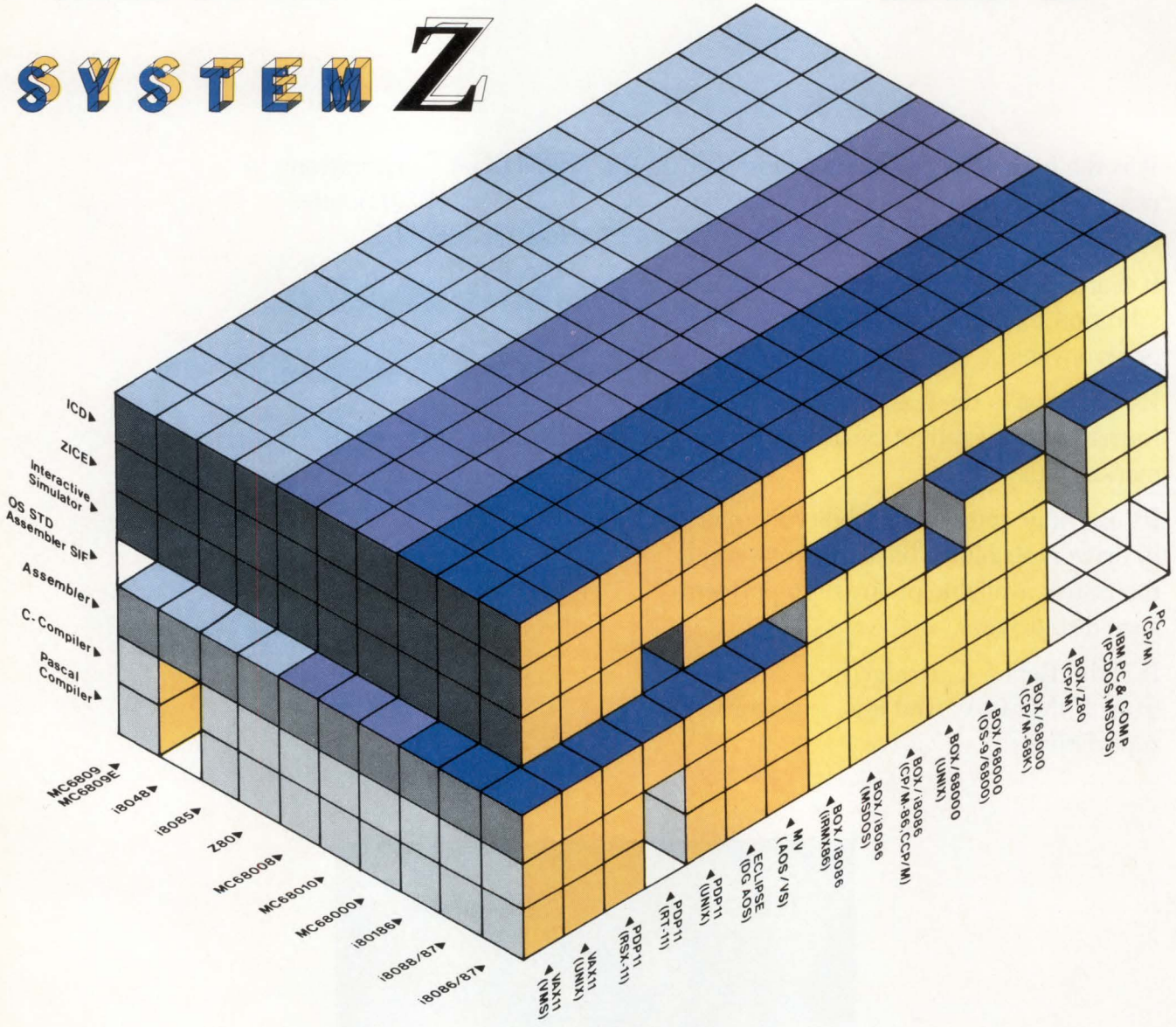
CIRCLE 144

System Z is going to change the way you look at microprocessor development systems...forever



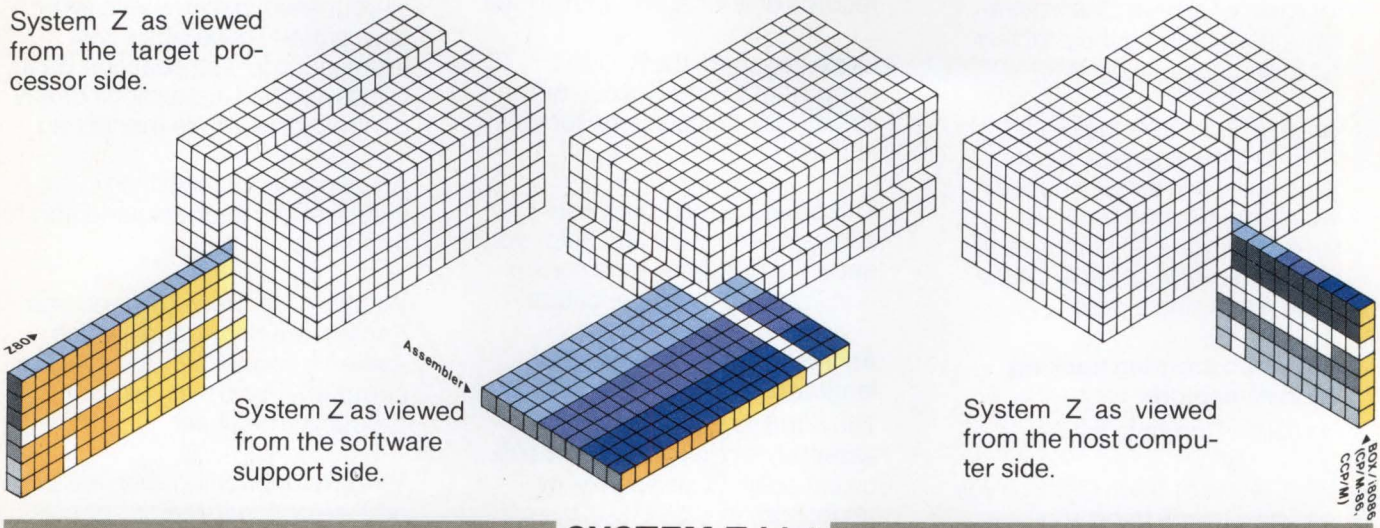
System Z is not an individual product, not a single technique, but an incredible complete development system born from Zax's total-product planning philosophy, Z...ing.

This total-system approach results in a fully-integrated development program that is compatible with *any* operating system, in *any* environment, on *any* level.

System Z emphasizes flexibility and efficiency by allowing the design engineer to choose the most effective combination for a particular requirement. So nothing — not time, materials or money — is wasted.

The versatility of System Z permits the use of any personal or minicomputer. Additionally, the proven power and reliability of Zax's own microcomputer, the BOX, may be used to deliver outstanding performance at a very economical price.

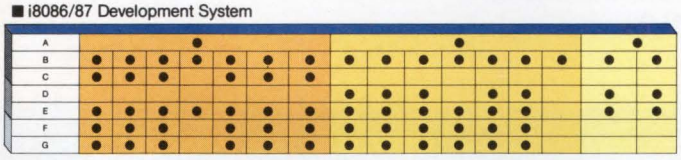
...because there's never been a system that's this flexible, this powerful and this efficient.



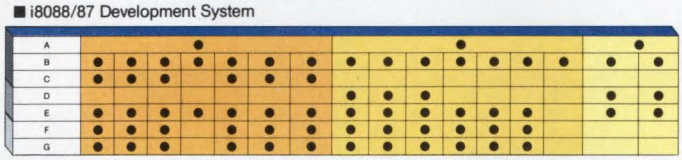
SYSTEM-Z List

HOST SYSTEM	Minicomputer System Series							BOX System Series								PC Series	
	VAX 11		PDP 11			ECLIPSE	MV	BOX/i8086			BOX/68000			BOX/Z80	IBM PC IBM PC COMP.	PC
	VMS	UNIX	RSX11	RT11	UNIX	DG AOS	AOS/VS	iRMX86	MS DOS	CP/M86 CCP/M86	UNIX	OS-9 /68000	CP/M68K	CP/M80	PC DOS MS DOS CP/M86	CP/M86

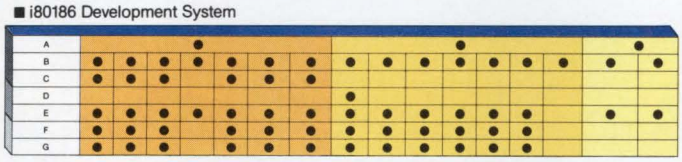
■ i8086/87 Development System



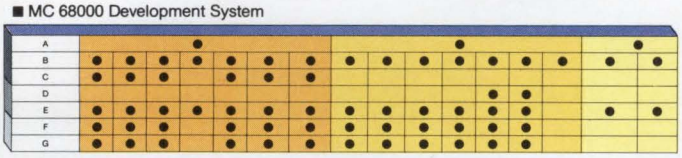
■ i8088/87 Development System



■ i80186 Development System



■ MC 68000 Development System



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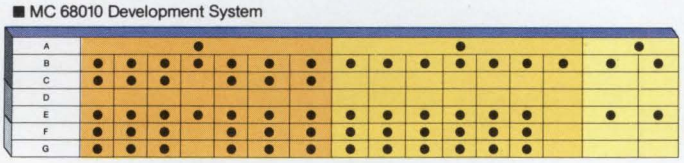
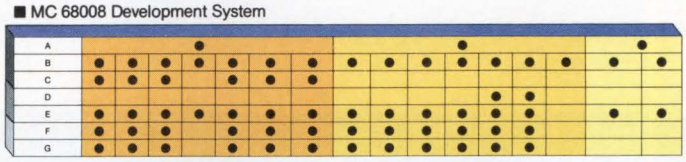
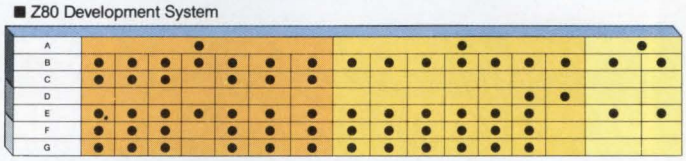


HOST SYSTEM	Minicomputer System Series							BOX System Series								PC Series	
	VAX 11		PDP 11			ECLIPSE	MV	BOX/i8086			BOX/68000			BOX/Z80	IBM PC IBM PC COMP.	PC
	VMS	UNIX	RSX11	RT11	UNIX	DG AOS	AOS/VS	iRMX86	MS DOS	CP/M86 CCP/M86	UNIX	OS-9 /68000	CP/M68K	CP/M80	PC DOS MS DOS CP/M86	CP/M86

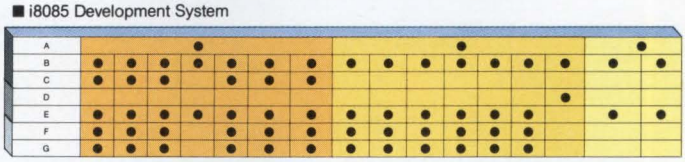
■ MC 68008 Development System



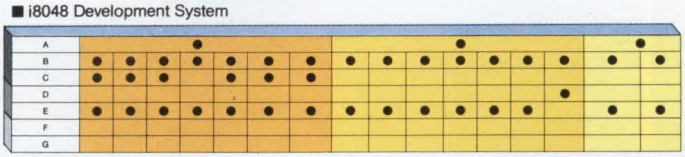
■ Z80 Development System



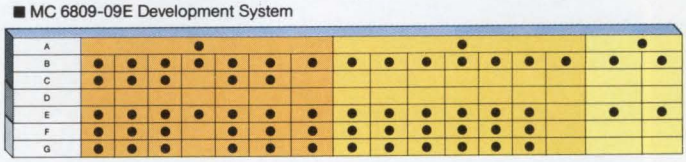
■ i8085 Development System



■ i8048 Development System



■ MC 6809-09E Development System



A ICD In-Circuit Emulator Debugger

B ZICE ICD's System Software

C Interactive Simulator

D OS STD ASM

E Assembler

F C-Compiler

G Pascal Compiler

SYSTEM Z-from Z...ing

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CIRCLE 145

The K105-D analyzer with Trace Control™ helps you find faults quickly and easily.

For most engineers, the frustration is not in solving the problem. But in finding it.

Not anymore. Take the Gould K105-D logic analyzer. It can help you isolate errors and their causes quickly and easily. Because now you can capture and examine several possible cause areas with a single pass.

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Flexibility is the key.

With 8 levels of Trace Control, you can follow every bend and turn in your program flow. No matter how complex. And capture widely-separated slices of code better than any other triggering method.

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Clear, concise pattern definitions.

With the K105-D, you can define all your event patterns with symbolic labels. These labels can represent address locations, data values, fetched instructions or any control signal you're monitoring.

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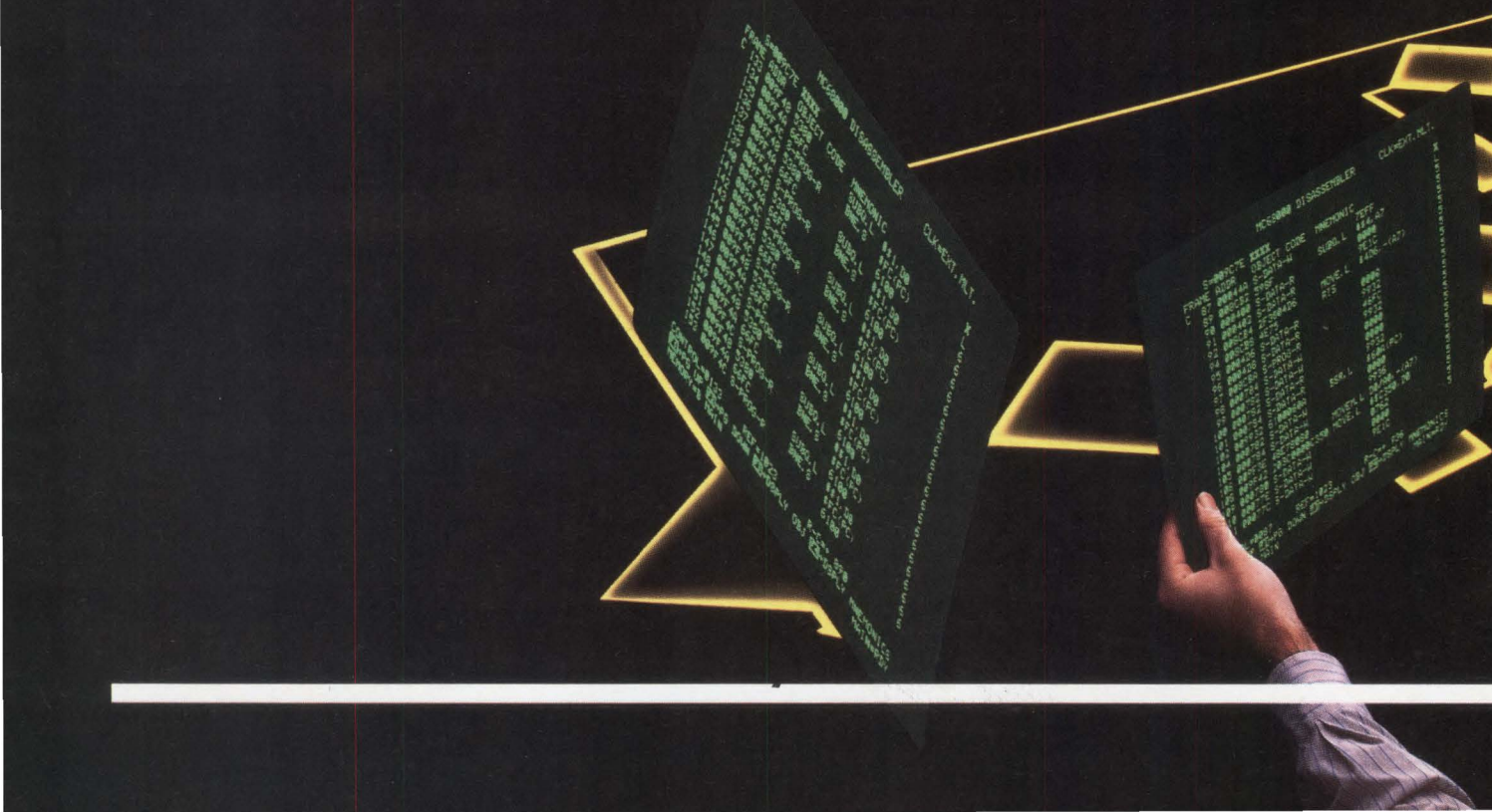
What's more, Trace Control uses English-like commands which make for shorter set-ups. Quicker comprehension. And a more productive engineer.

To make debugging even easier, add the optional dual floppy disk drive. With it, you can store up to 35 set-ups and associated recordings on a single diskette for instant recall.

Now, capture up to 4 segments of complex program flow to pinpoint problems fast.



You won't get caught in a loop.
By using the K105-D's loop counter, you can follow a sequence of events for a specific number of iterations. Then stop at will.

It's a quick way for you to test the repeatability of a program function. And verify that your code is having the predicted effect.

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For the hard part (hardware/software integration), now there's a simpler solution. The K105-D's 100 MHz high speed link.

It's an extremely precise way to see how timing affects software execution. And vice-versa.

Again, for this task, Trace Control can help you track down hard-to-find faults. So you end up with a program that flows smoothly. Error free. In a fraction of the time it used to take.

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At Gould, we engineer every instrument to be clearly the best in its class.

So now with your insight and the K105-D analyzer, you can capture the problem. And solve it. Fast.

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United Kingdom: Gould Inc., Design & Test Systems Division, Hainault Operation, Roebuck Road, Hainault, Essex 1G6 3UE, United Kingdom. Phone: (44) (1) 500-1000.

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The K105-D gives you two levels of HELP at the touch of a button. First, step-by-step operating instructions that appear along the bottom of the analyzer screen. Second, a menu that allows you to select more detailed "help" should you need it.

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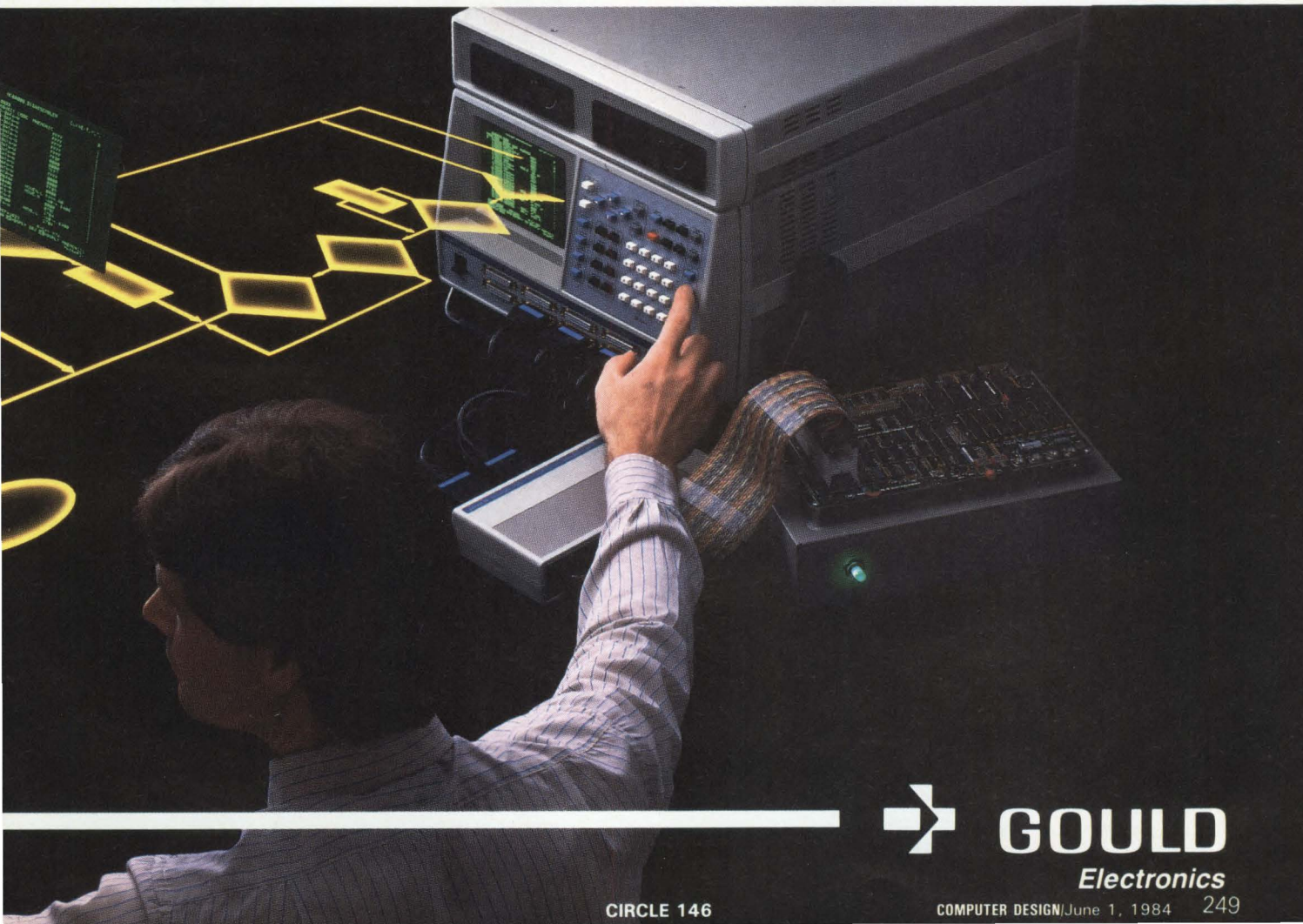
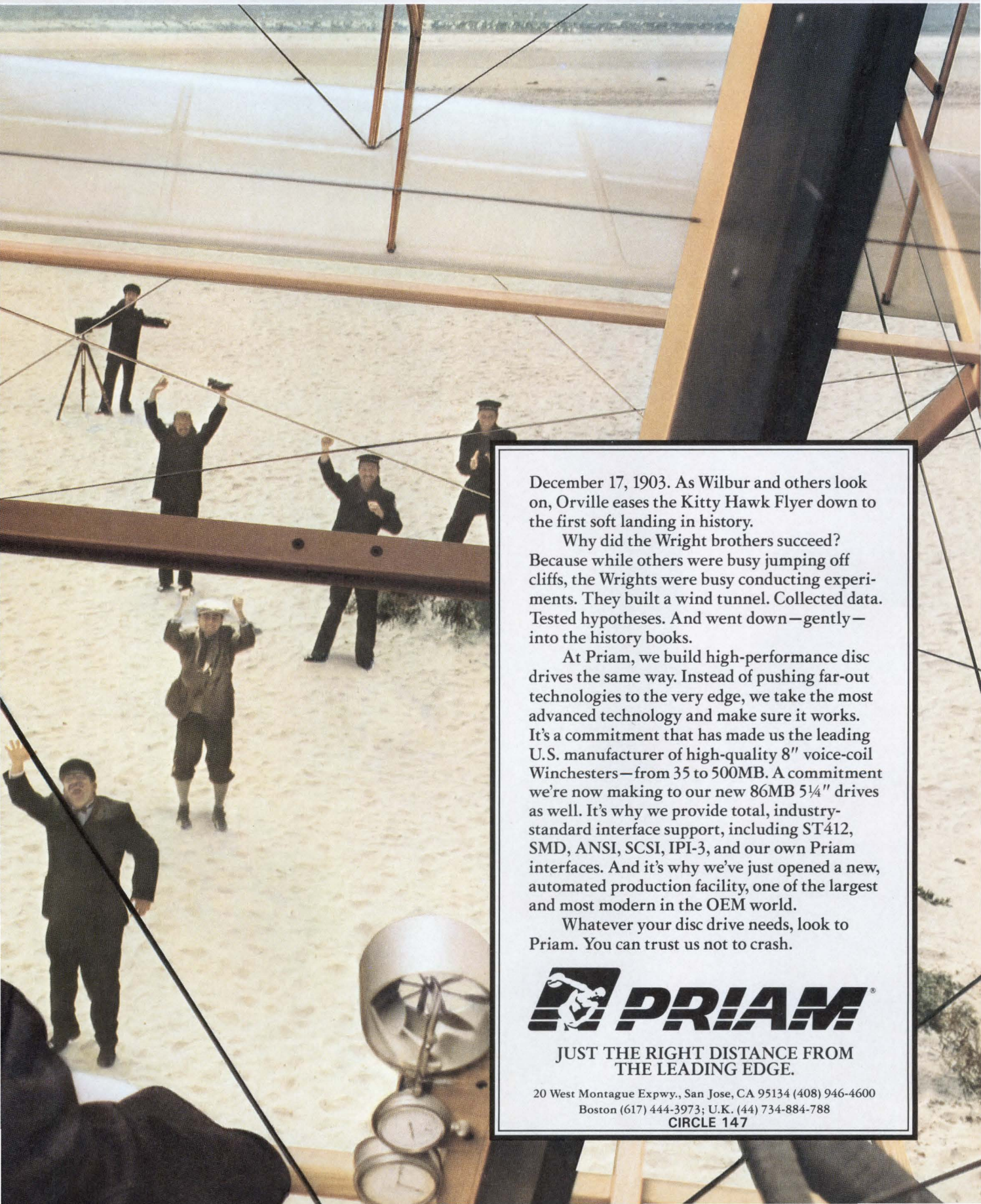


GOULD
Electronics

CIRCLE 146

THE WRIGHT BROTHERS
THEY WERE JUST THE

WEREN'T THE FIRST TO FLY. FIRST NOT TO CRASH.



December 17, 1903. As Wilbur and others look on, Orville eases the Kitty Hawk Flyer down to the first soft landing in history.

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CIRCLE 148

Measurement handbook

Full-color, 200-page reference guide contains technical and application guides for pressure and strain measurement/control applications; prices are included. **The Omega Group,** Stamford, Conn.

Circle 410

Seminar bulletin

A 29-page bulletin includes seminars about technology and management; overall, a variety of sessions runs through December 1984. Registration form and price included. **Worcester Polytechnic Institute,** Worcester, Mass. **Circle 411**

Interfacing A-D

Six-page application note discusses techniques for interfacing A-D converters with microprocessors for different conversion data rates; seven figures illustrate interfaces, circuits, and software flow. **ILC Data Device Corp,** Bohemia, NY.

Circle 412

Packaging system

Metric series packaging system offers stitch-wire, wire-wrapping, and insulation displacement pin wiring options to provide optimum-performance development on production system. **Interconnection Technology, Inc,** Huntington Beach, Calif.

Circle 413

Fiber optics and optical communication

Selection guide for fiber optic and optical communication and systems provides specs, photos, and schematics for fiber optic LANS, links and systems, and line-of-sight beam links. **Codenoll Technology Corp,** Yonkers, NY. **Circle 414**

Bibliography of metric guides

The American National Metric Council (ANMAC) has published a metric practice guide listing 56 items for metric transition; copies are available for $5, plus a large self-addressed envelope (37¢ postage). **ANMAC,** 5410 Grosvenor Ln, Bethesda, MD 20814.

Software for PDP-11

Two-volume PDP-11 sourcebook covers application and system software programs for PDP-11 minis and microcomputers; over 1500 applications in 33 categories are described. Prices, vendors, addresses, and phone numbers are listed. **Digital Equipment Corp,** Northboro, Mass.

Circle 415

Applications for Domain

The second application catalog for the Domain system contains over 200 third-party software, hardware, and value-added supplier applications; the 256-page book covers 13 different areas. **Apollo Computer,** Chelmsford, Mass.

Circle 416

Systems for the STD bus

Brochure details wide range of STD bus board and system-level products; separated by function, general specs are provided for the entire product line. **Applied Micro Technology, Inc,** Tucson, Ariz.

Circle 417

Consensus standards

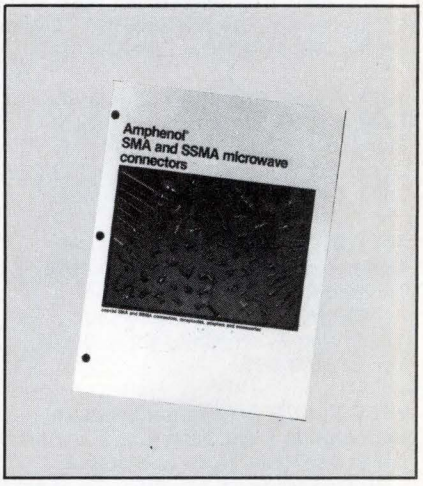
Nine standard guides and one specification compile voluntary guidelines for computerized systems and services; the book covers project definition; functional requirements; functional design; implementation design; assembly, installation, and test; and evaluation for most system sizes and types. Price is $15.20 for ASTM members; $19 for nonmembers. **ASTM (formerly American Society for Testing and Materials),** 1916 Race St, Philadelphia, PA 19103.

Multibus products

Catalog features Multibus-compatible horizontal and vertical, rackmountable card cages, universal pattern panels, and such accessories as connectors and fans; each description includes photos and drawings. **Augat Inc, Interconnection Systems Div,** Attleboro, Mass.

Circle 418

Microwave connectors



Illustrated, 104-page catalog details SMA and SSMA microwave connectors, receptacles, adapters, and accessories; quick-reference photos and functional selection charts are provided. **Amphenol Products,** Oak Brook, Ill.

Circle 419

Trimmer catalog

Catalog details trimmer models according to features, specs, and dimensions; sections on multiturn, single-turn, and MIL-spec versions, plus selection and designer guides, are included. **Bourns, Inc, Trimpot Div,** Riverside, Calif.

Circle 420

Binary to BCD converter

The SBD227 22-bit binary to BCD converter is described in two-color data sheet; the converter accepts binary digital representation of an angle and provides a scaled BCD equivalent angle. **Natel Engineering Co,** Simi Valley, Calif.

Circle 421

Filtering CRT video

Technical bulletins specify video/filter CRT anti-glare panels for many types of display terminals; applications and options are examined. **Panelgraphic Corp,** West Caldwell, NJ.

Circle 422

Power conditioning and monitoring

Catalog features complete line of power monitoring and conditioning equipment, covering computers, telecomm, word processors, and machine tool controls. **Registration Electric,** Linden, NJ.

Circle 423

CONFERENCES

JULY 9-12—NCC (National Computer Conf), Las Vegas Convention Ctr, Las Vegas, Nev. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JULY 23-25—Computer Simulation Conf, Copley Plaza Hotel, Boston, Mass. INFORMATION: Society for Computer Simulation, PO Box 2228, La Jolla, CA 92038. Tel: 800/225-7654

JULY 23-27—SIGGRAPH Conf on Computer Graphics and Interactive Techniques, Minneapolis, Minn. INFORMATION: Lynn Valastyan, 111 E Wacker Dr, Chicago, IL 60601. Tel: 312/644-6610

JULY 30-AUG 2—Internat'l Pattern Recognition Conf, Montreal, Canada. INFORMATION: ICPR Secretariat, 3450 University St, Montreal, Quebec, Canada H3A 2A7. Tel: 514/392-6744

AUG 2-6—Autofact Japan Conf and Expo (held conjointly with **Mechatronics**), Osaka, Japan INFORMATION: Leslie Hossack, Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48121. Tel: 313/271-0023

AUG 12-15—Computers in Engineering Conf and Exhibit, Las Vegas Hilton, Las Vegas, Nev. INFORMATION: Mary Benedict, American Society of Mechanical Engineers, 345 E 47th St, Suite 13M, New York, NY 10017. Tel: 212/705-7100

AUG 19-24—Technical Symposium on Optics and Electro-Optics and Instrument Display, Town & Country Hotel, San Diego, Calif. INFORMATION: Rich Donnelly, Information Services, SPIE, PO Box 10, Bellingham, WA 98225. Tel: 206/676-3290

AUG 21-24—Conf on Parallel Processing, Hilton Shanty Creek, Bellaire, Mich. INFORMATION: Tse-yun Feng, 1604 Stormy Ct, Xenia, OH 45385. Tel: 614/422-1408

AUG 30-SEPT 1—Conf on Solid State Devices and Materials, Kobe, Hyogo, Japan. INFORMATION: Susumu Namba, Osaka Univ, Faculty of Engineering Science, Toyonaka, Osaka, Japan 560.

SEPT 5-8—Conf on Digital Signal Processing, Florence, Italy. INFORMATION: A. G. Constantinides, Dept of Electrical Engineering, Imperial College of Science & Technology, Exhibition Rd, London SW7 2BT, England. Tel: 01/5895111

SEPT 10-13—Advanced Control Conf, Purdue Univ, West Lafayette, Ind. INFORMATION: Edward Kompass, Editor, *Control Engineering* magazine, 1301 S Grove Ave, PO Box 1030, Barrington, IL 60010. Tel: 312/381-1840

SEPT 11-13—Electronic Imaging, Westin Hotel, Boston, Mass. INFORMATION: Morgan-Grampian Expositions Group, 2 Park Ave, New York, NY 10016. Tel: 212/340-9780

SEPT 11-13—Midcon Electronics Exhibition and Convention, Dallas Convention Ctr, Dallas, Tex. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 11-13—Mini/Micro-Southwest Computer Conf and Exhibition, Dallas Convention Ctr, Dallas, Tex. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 11-13—Voice Input/Output System Applications Conf, Marriott Crystal Gateway Hotel, Arlington, Va. INFORMATION: Robert Burgess, Public Information Office, Lockheed Missiles & Space Co, Inc, Sunnyvale, CA 94086. Tel: 408/742-6688

SEPT 11-14—Unix Systems Expo, Los Angeles Convention Ctr, Los Angeles, Calif. INFORMATION: David Sudkin, Computer Faire, Inc, 181 Wells Ave, Newton, MA 02159. Tel: 617/965-8350

SEPT 16-20—Compcon Fall, Hyatt Regency Crystal City, Arlington, Va. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

SEPT 17-21—FOC/LAN (Fiber Optic Communications and Local Area Networks) Exposition, MGM Grand Hotel, Las Vegas, Nev. INFORMATION: Michael O'Bryant, Information Gatekeepers, Inc, 138 Brighton Ave, Suite 212, Boston, MA 02134. Tel: 617/787-1776

SEPT 19-21—Connector and Interconnection Technology Symposium, Disneyland Hotel, Anaheim, Calif. INFORMATION: Electronic Connector Study Group, Inc, PO Box 167, Fort Washington, PA 19034. Tel: 215/279-7084

SEPT 26-28—Eurocon: Computers in Communications & Control, Brighton, England. INFORMATION: Brian Atkinson, IEE, Savoy Place, London, WC2R OBL England.

OCT 1-4—AUTOFACT 6 Conf & Exh, Anaheim Convention Center, Anaheim, Calif. INFORMATION: Soc of Manufacturing Engineers, 1 SME Dr, PO Box 930, Dearborn, MI 48121. Tel: 313/271-0777

OCT 2-4—Northcon Electronics Conf & Exh, Seattle Center Flag Pavilion, Seattle, Wash. INFORMATION: Nancy Hogan, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

OCT 2-4—Mini/Micro Northwest Conf & Exh, Seattle Center Flag Pavilion, Seattle, Wash. INFORMATION: Nancy Hogan, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

OCT 8-9—9th Conf on Local Area Networks, Minneapolis, Minn. INFORMATION: Harvey A. Freeman, Architectural Technology Corp, PO Box 24344, Minneapolis, MN 55424.

OCT 8-10—ACM Annual Conf: The Fifth Generation Challenge, San Francisco Hilton Hotel, San Francisco, Calif. INFORMATION: Karen Duncan, Chairman, ACM '84, 15 Parsons Way, Los Altos, CA 94022.

SHORT COURSES

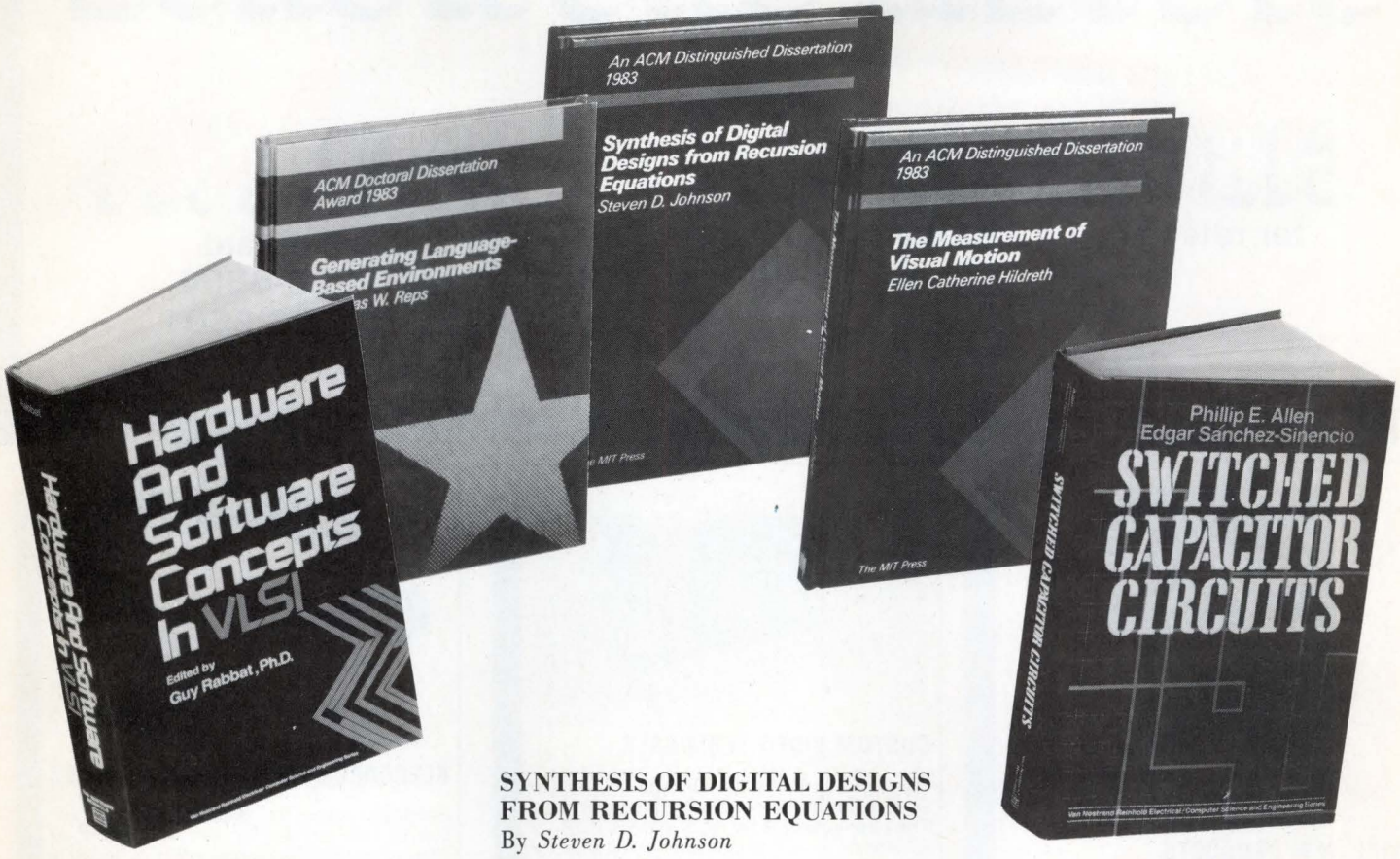
AUG/NOV—Applications-Oriented Approach to Artificial Intelligence, Ottawa, Canada and Washington, DC. INFORMATION: George Harrison, The George Washington Univ, Washington, DC 20052. Tel: 800/424-9773

SEPT 10-14—Decision of Digital Control Systems, Washington, DC. INFORMATION: George Harrison, The George Washington Univ, Washington, DC 20052. Tel: 800/424-9773

SEPT/OCT/NOV—EMI Seminars, One and two days each, Boston, Philadelphia, Washington, and Chicago. INFORMATION: Trish Puhl, R & B Enterprises, 20 Clipper Rd, W Conshohocken, PA 19428. Tel: 215/825-1965

SEPT/OCT—World Conf on Ergonomics in Computer Systems, various U.S. and European cities. INFORMATION: Robert W. Bailey, Computer Psychology, Inc, 54 E Main St, PO Box 16, Mendham, NJ 07945. Tel: 201/543-9009

Designer's Bookcase



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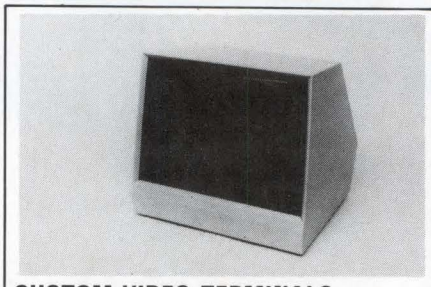

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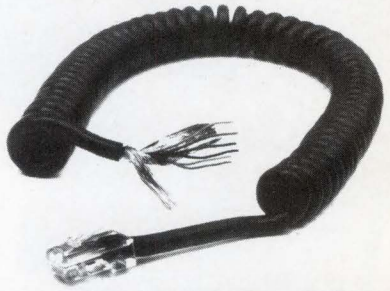

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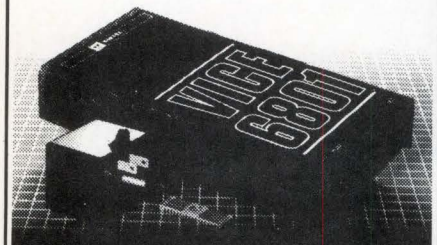

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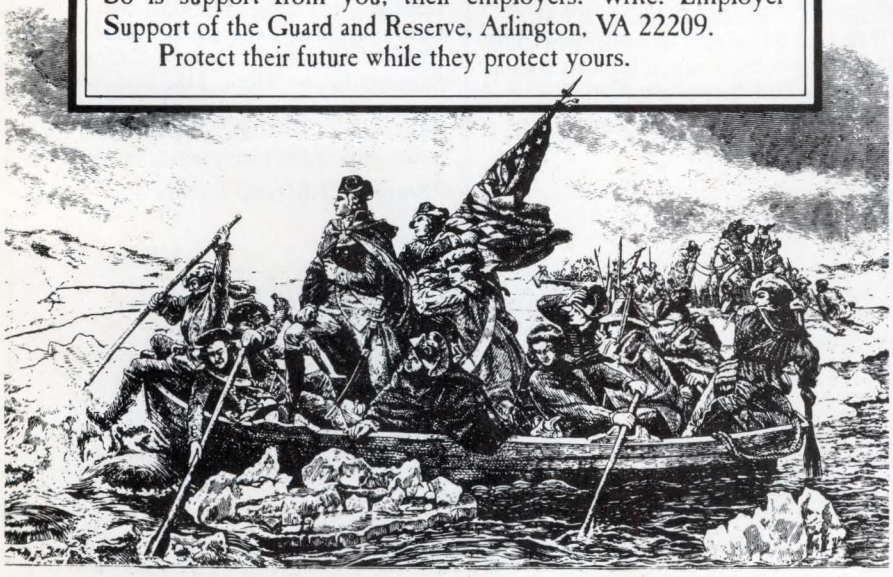

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Technical Marketing Specialist

In this challenging position, you will make detailed architectural and applications comparisons of the Series 32000 with other 32-bit microprocessors, write papers for trade press and conferences, and prepare and evaluate benchmark studies. Additionally, you will have the opportunity to work with engineering and with key customers in conceiving and introducing new products. A strong computer science background and some project management experience required, as well as good analytical, writing and speaking skills.

Section Head and Senior Engineers

You'll be directly involved with performance evaluation and improvement, characterization, chip-to-chip communication and new design evaluation for the Series 32000. Also involves intimate coordination with design, applications, systems integration and testing. Requires BS/MS/PhD in EE or CS, or equivalent, plus microprocessor experience, including testing and characterization. Packaging experience a plus.

Design Engineering

Senior Circuit Design Engineers

With design responsibility for National's Series 32000 circuits, this position provides the opportunity to work with advanced architectures and high-performance MOS technologies. You will be responsible for all phases of microprocessor circuit design, including logic and circuit design, project scheduling, circuit evaluation and resolution of testing issues. BS/MS/PhD in EE or CS, or equivalent, plus MOS/LSI design experience required, including experience in successfully transferring designs to production.

Get the Full Story.

The breadth of National's technologies, and the depth of our commitment to advancing those technologies, makes National the ideal place for you to pursue your career. Send your resume to National Semiconductor, Dept. MS, Professional Employment, P.O. Box 62499, Sunnyvale, CA 94088. We are an equal opportunity employer, m/f/h/v.

*Formerly NS16000 Family

Together, We'll Do Even More.

National Semiconductor

SHAPE YOUR OWN FUTURE.

General Dynamics Data Systems Division helps shape the future of many significant programs at its major locations in San Diego, California; Fort Worth, Texas; and Norwich, Connecticut; as well as at satellite locations including Detroit, Michigan, and Pomona, California. We provide diverse support functions for such high-technology programs as the F-16 multimission fighter/attack aircraft, the M1 main battle tank, nuclear-powered submarines, and the entire family of cruise missiles. Throughout our division you'll find a variety of opportunities to apply your own scientific and engineering expertise to create a more exciting future.

The Data Systems Division gives you the chance to join one of the most skilled teams in the industry today, and offers excellent salaries and benefits.

If you're interested in shaping your own future on our innovative support team, one of our opportunities listed below may be just right for you.

For immediate consideration, send your resume to the Vice President/Director at the Data Center of your choice.

PRODUCT SOFTWARE

— Bachelor's and/or Master's degree, and 3-8 years' experience.
— SKILLS: FORTRAN, JOVIAL, PASCAL, Ada, Assembly Languages, Applied Math, Data Bases, Operating Systems, Documentation (MIL Standards).
— APPLICATIONS: Command & Control Software (Guidance, Navigation, C^3I, Display Systems, Executive & System Support Software), Mission Planning, Data Handling & Communication, Automatic Testing Equipment/ Simulations, Image Processing, Estimation & Control Theory.
— Embedded Systems: Real-Time Software.

CAD/CAM

— Bachelor's and/or Master's degree, and 3-8 years' experience.
— SKILLS: FORTRAN, Ada, Assembly Languages, IBM, CDC & VAX Operating Systems, Computational Geometry, Information Modeling & Data Dictionaries.
— APPLICATIONS: Turn-key Graphic Systems, Solid Modeling, Robotics, CNC-DNC, Real-Time Processing Control, Group Technology.
— CADAM, CAT/A, Computervision, SC/CARDS, Model 204, Systems Engineering, Group Management.

ENGINEERING SYSTEMS

— Bachelor's and/or Master's degree, and 3-8 years' experience.
— SKILLS: Simulation Languages, FORTRAN, COBOL & IBM Assembler, TSO, SPF, DISSPLA, RAMIS, Scientific Programming and Microcomputer experience.
— APPLICATIONS: Simulation, SLAM, Manufacturing, Operations Research, Image Processing, Graphics Application Development, Sneak Circuit Analysis, Program Marketing.

U.S. CITIZENSHIP REQUIRED
Equal Opportunity Employer, M/F

GENERAL DYNAMICS

Data Systems Division

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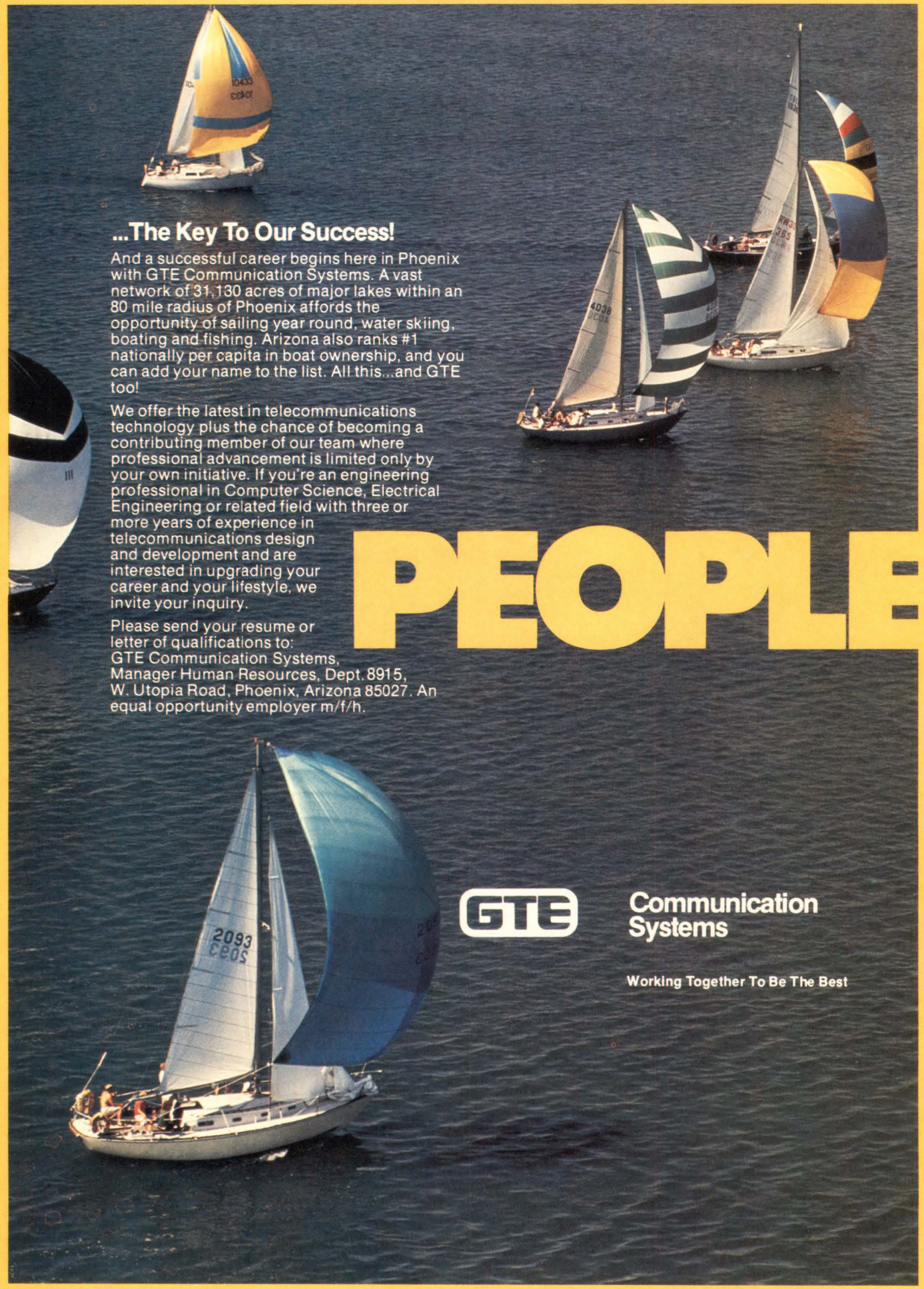
San Diego, CA 92138

CENTRAL CENTER
P.O. Box 748, Drawer 002
Fort Worth, TX 76101

EASTERN CENTER
100 Winnenden Rd., Drawer 002
Norwich, CT 06360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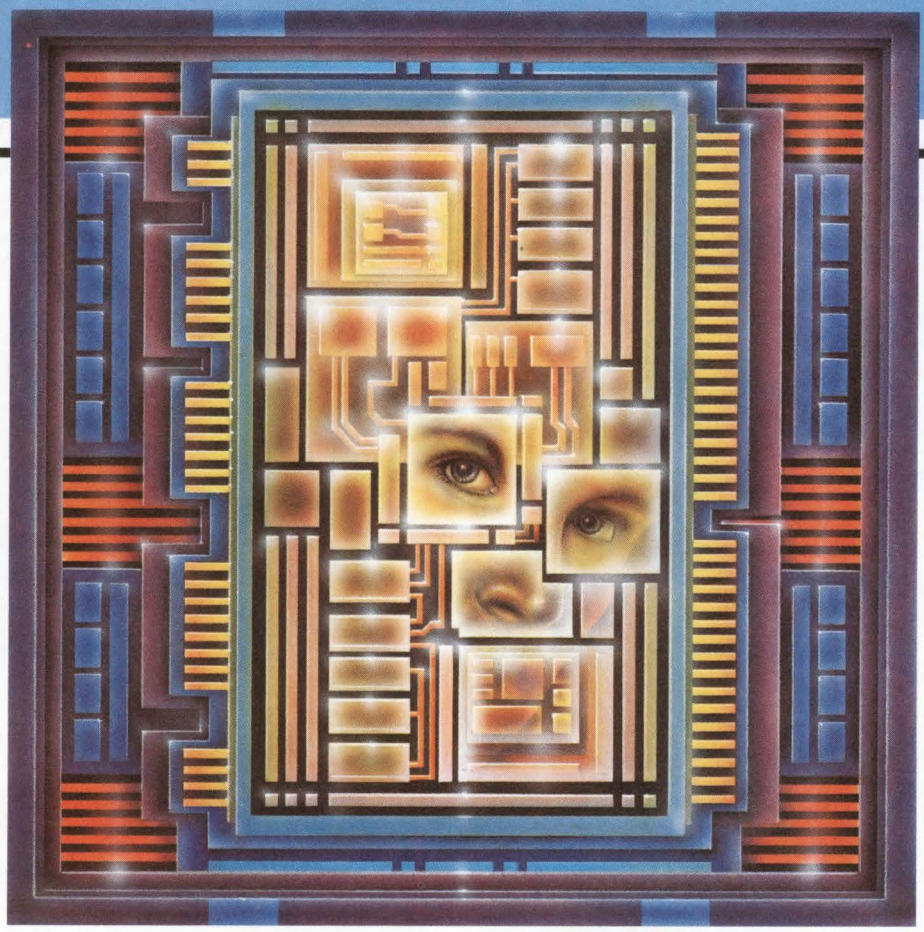

Progress, the by-product of innovation, is an Intel tradition. This leadership quality is well documented on the components side. Now, we're putting that same tradition to work in the area of systems with advancements such as our super-powerful, supermicro system for OEMs, the 286/310, to date the most powerful we've ever made. When it comes to systems integration, we're out in front with our iDIS Database Information System. Our iTAPS Transaction Processing System handles up to 16 users and allows for the development of individual application software 50% faster.

While we have grown in size, strength and technology, we have not lost sight of the qualities that put us out in front. You will still find a highly charged atmosphere of discovery and mutual respect. We still place a high premium on finding people who have inquiring minds, strong technical skills, and the ability to adapt quickly to changing situations. If you're an engineer involved with **SOFTWARE EVALUATION, PRODUCT MARKETING, HARDWARE SYSTEMS, DIAGNOSTICS, CUSTOMER SERVICE, SYSTEMS SOFTWARE, CAD, PRODUCT EVALUATION, GRAPHICS, HIGH-LEVEL LANGUAGES, OPERATING SYSTEMS, COMPILER, RELIABILITY, TECHNICAL MARKETING, or DATABASE MANAGEMENT SYSTEMS,** and want to see your work integrated into sophisticated new systems, let's talk.

Intel offers competitive compensation, advancement based on achievement, and the chance to work with some of the best minds in American industry. For consideration at Intel sites in Phoenix, AZ; Santa Clara, CA; Portland, OR; and Austin, TX, please direct your response to: Mike Gore, Intel Corporation, Dept. 8828, 2402 W. Beardsley Rd., Phoenix, AZ 85027. All inquiries will be answered promptly and held in strict confidence. An Equal Opportunity Employer M/F/H.

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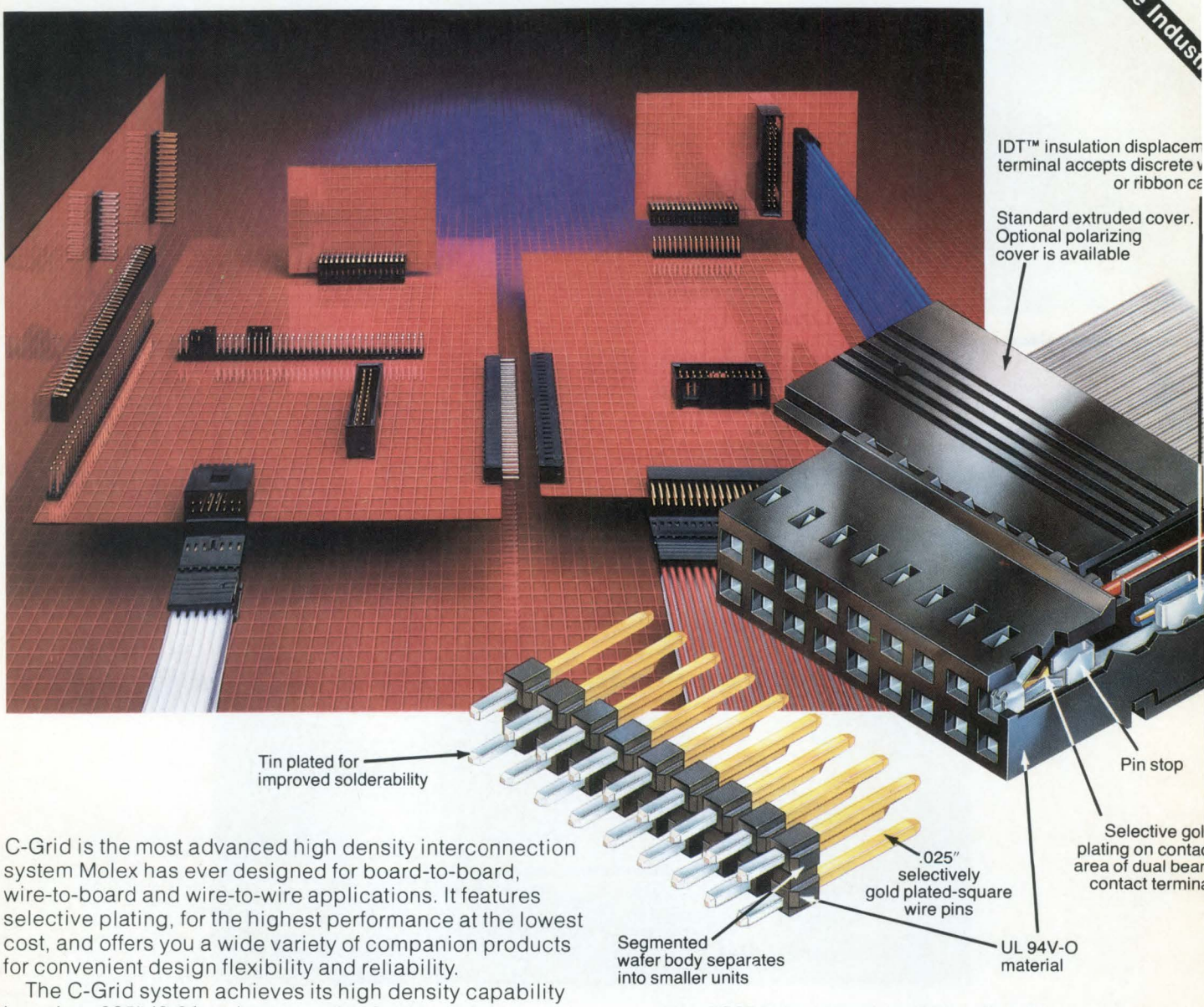
C-Grid: the Molex .100" x .100" PCB interconnection system.

Shortest Leadtimes in the Indust



C-Grid is the most advanced high density interconnection system Molex has ever designed for board-to-board, wire-to-board and wire-to-wire applications. It features selective plating, for the highest performance at the lowest cost, and offers you a wide variety of companion products for convenient design flexibility and reliability.

The C-Grid system achieves its high density capability by using .025" (0,64mm) square pins for the male connector parts, set in a .100" x .100" (2,54 x 2,54mm) matrix. The pins can either be placed directly in the board or used in volume with wafer bodies.

To load loose pins into the PC board, Molex offers a patented single- or Multi-Pinsetter® capable of up to 156,000 insertions per hour—the fastest on the market.

Shrouded and unshrouded headers are available in straight and right-angle wafer bodies.

The #8676 dual-row, insulation displacement connectors are stackable, end-to-end, and feature IDT™ terminals with mass termination application tooling available to help you achieve greater cost savings in your assembly operations.

Molex closed-or open-end shunts make it easier and less expensive to retrofit board circuitry by avoiding DIP switches.

Molex also offers a female connector (7990-series) to b soldered to one board and mated with the .025" (0,64mm) pins on another. Its features include low mating force, eas of insertion and improved solderability.

For more information on our C-Grid interconnection system, contact the Molex office nearest you.

First in Customer Service ...Worldwide

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Corporate Headquarters: 2222 Wellington Court, Lisle, Illinois 60532 Phone: (312) 969-4550 Telex: 27-0072/25-4069
European Headquarters: Molex House, Church Lane East, Aldershot, Hants, England GU11 3ST Phone: (0252) 318221 Telex: 851858988
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CIRCLE 149

The fastest...the largest memories... the easiest to program...

MARS-432 Array Processor Speed
A high-speed programmable arithmetic processor used as a peripheral to a general purpose computer.

MARS-432 Array Processor Memories
Program and data memories compatible with programs written for today's array processor applications.

MARS-432 Array Processor Software
An architecture specifically designed to support a FORTRAN compiler and other software development tools.

The state of the art in 32-bit floating point array processors. Direct addressability of up to 16 million words (64 megabytes) of data memory and direct access to the high-speed internal data bus assure the user of highest throughput rates.

MARS-432 Array Processor Features Include:

- Add and multiply times of 100ns
- Computational power of 30 megaflops
- Computes a 1024-point complex FFT in 1.7ms
- DMA transfers at I/O bus rates of 20 megabytes/sec
- Data memory read or write in 100 ns
- Memory paging for uninterrupted processing during I/O transactions.

Program Memory
Virtual and physical address space of 4K words – standard. Expanded configuration uses a 4K cache memory to extend total memory to 64K words.

Data Memory
Data I/O is supported by DMA transfers into data memory with a physical address space of 16 million words. A data memory page-loading feature provides the option of zero overhead background loading of data during time critical program execution. No DMA cycle stealing overhead is incurred. Uninterrupted processing can occur simultaneously with high-speed I/O transfers.

FORTRAN Development System (FDS)
FORTRAN compiler, linker, and trace/monitor provide high-level language access to the MARS-432.

Microcode Development System
Off-line development package includes macro-assembler, microcode diagnostics, and a unique utility for automatic microcode optimization.

AP Run Time Executive Support Package (AREX)
As the interface to the MARS-432 at run time, AREX provides processor initialization, I/O operations, and array function execution.

Applications Libraries
Extensive applications libraries include math, signal processing, and image processing.

NUMERIX

For additional information on the MARS family of high-speed Array Processors, write or call:
Numerix Corp., 320 Needham Street, Newton, MA 02161 Tel. 617-964-2500 TELEX 948032

CIRCLE 150

Network Designers— Introducing the simplicity of a Remote Procedure Call ...ACCES XNS.

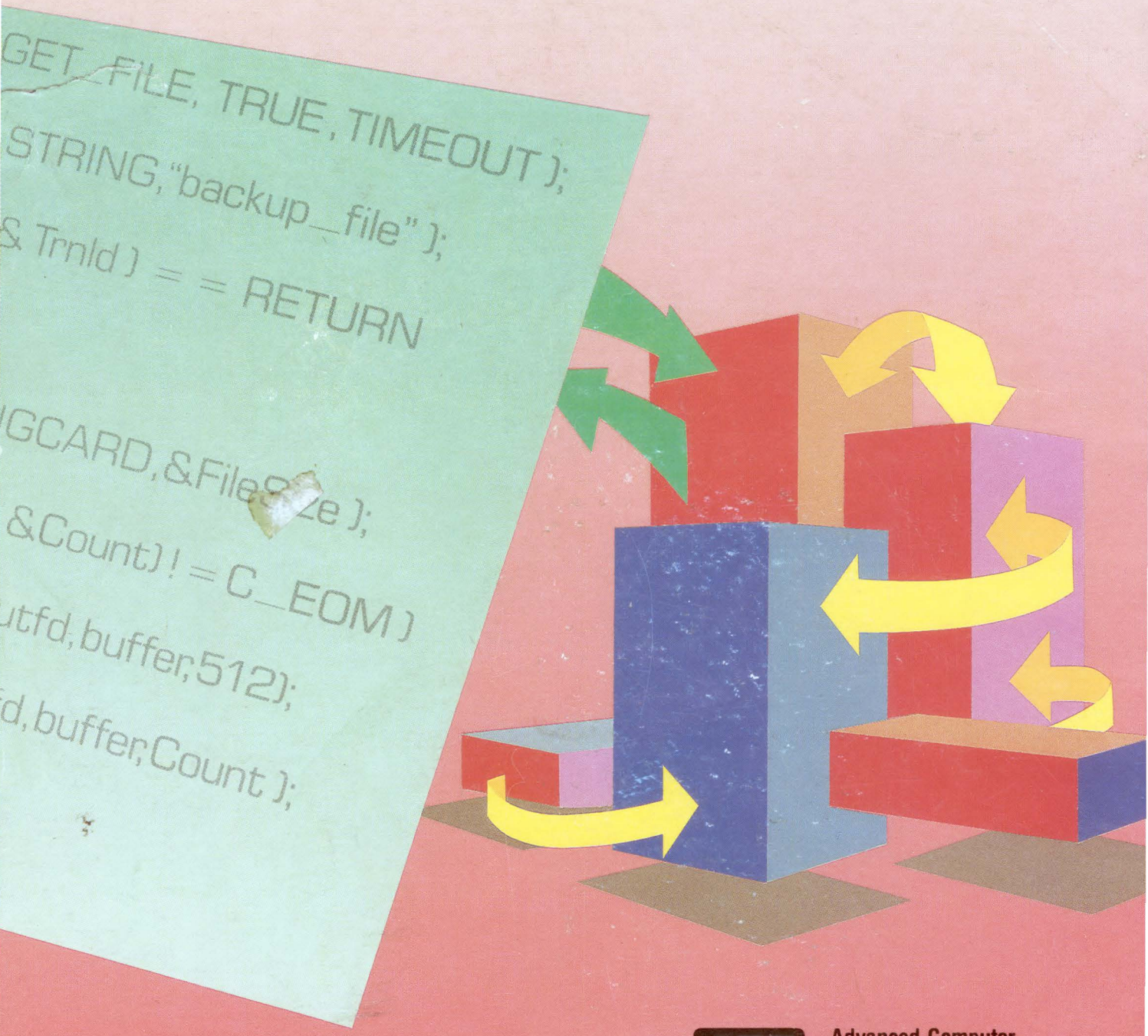
ACCES XNS is ACC's networking protocol package ready for use on popular minicomputers and work stations. It links applications and system level programs to data files and processing services in your distributed computer environment...through simple Remote Procedure Calls.

The ACCES XNS Protocol Package adheres to Xerox protocol standards: Courier, SPP, and IDP—making it compatible with other standard products, present and future.

Whether you are responsible for designing a communication environment around your company's product line, or interconnecting your company's computer resources, ACCES XNS meets your network design requirements.

To learn more about ACCES XNS, Courier, and Remote Procedure Calls, phone ACC at (805) 963-9431 and we'll gladly send you the ACCES XNS Brochure.

We Make Advanced Computers Communicate.



ACC **Advanced Computer Communications**

720 Santa Barbara Street
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CIRCLE 151