Wayne Gutschick on:
Programmable logic

A PENNWELL PUBLICATION SEPTEMBER 1991

COMPUTER DESIGN

Technology and Design Directions

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS

Enhancing the performance of standard buses

Framework vendors hammer out standards

Performance pushes RISC chips into real-time roles

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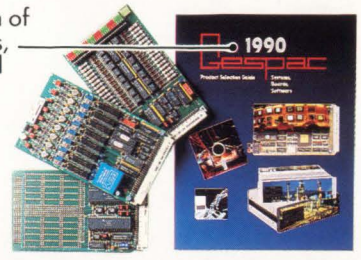

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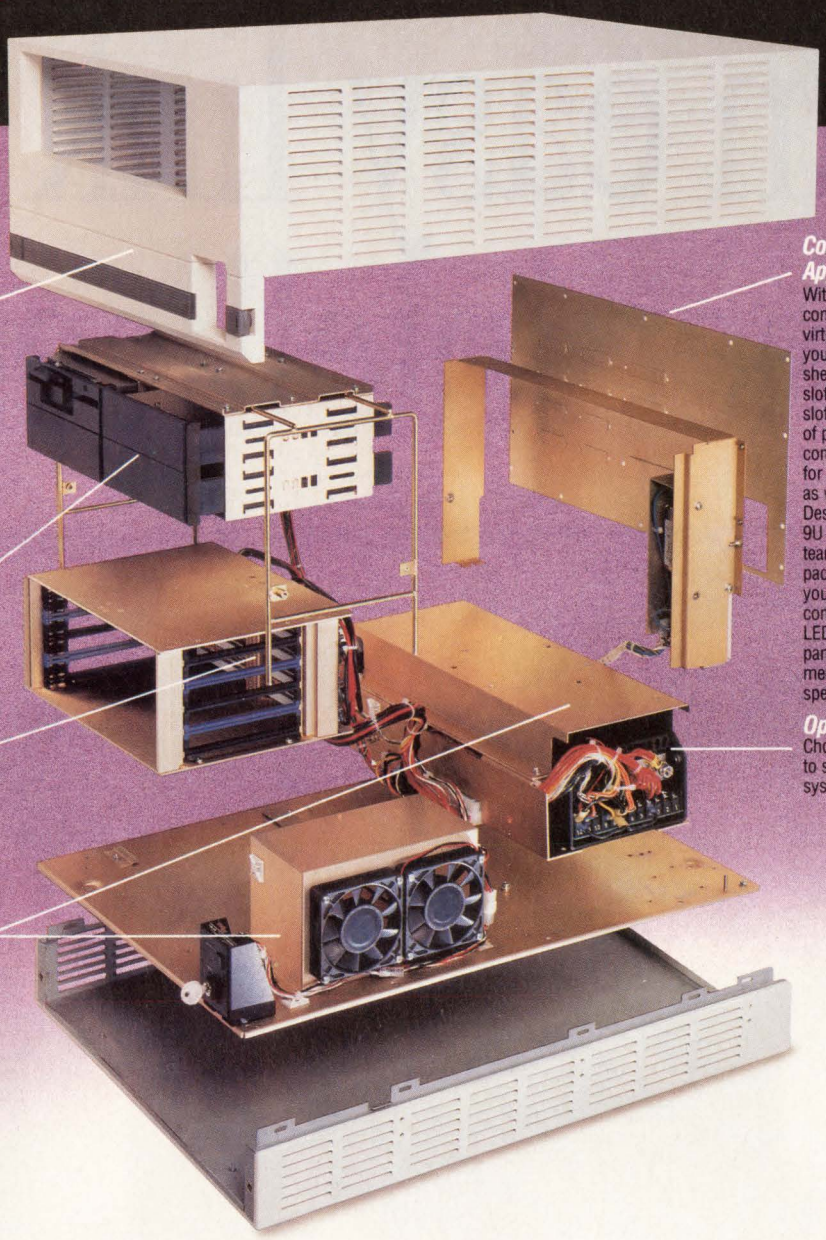
CIRCLE NO. 1

O M E G A

New



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Up to eight half-height 5¼" peripherals simply slide into their mounting brackets.

The Quietest Backplane Available
Plug your VME system into the quietest backplane ever! Our new 10-LAYER VME backplanes handle the fastest VME signals with the absolute minimum distortion, crosstalk, and noise.

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Choose from 175 to 1000 Watts to satisfy the demands of your system.

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Now you can benefit from 12 years of design experience and innovation that has made Electronic Solutions the industry leader in system packaging. The Omega™ Enclosures will give your VME or Multibus system the attractive exterior your image demands with a rugged, well-designed interior to withstand the most demanding environments. And besides the Electronic Solutions' full 3-Year warranty, the Omega bears FCC approvals and is UL, CSA, and TUV listed to get your system to an international market in the shortest time possible.

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CIRCLE NO. 2

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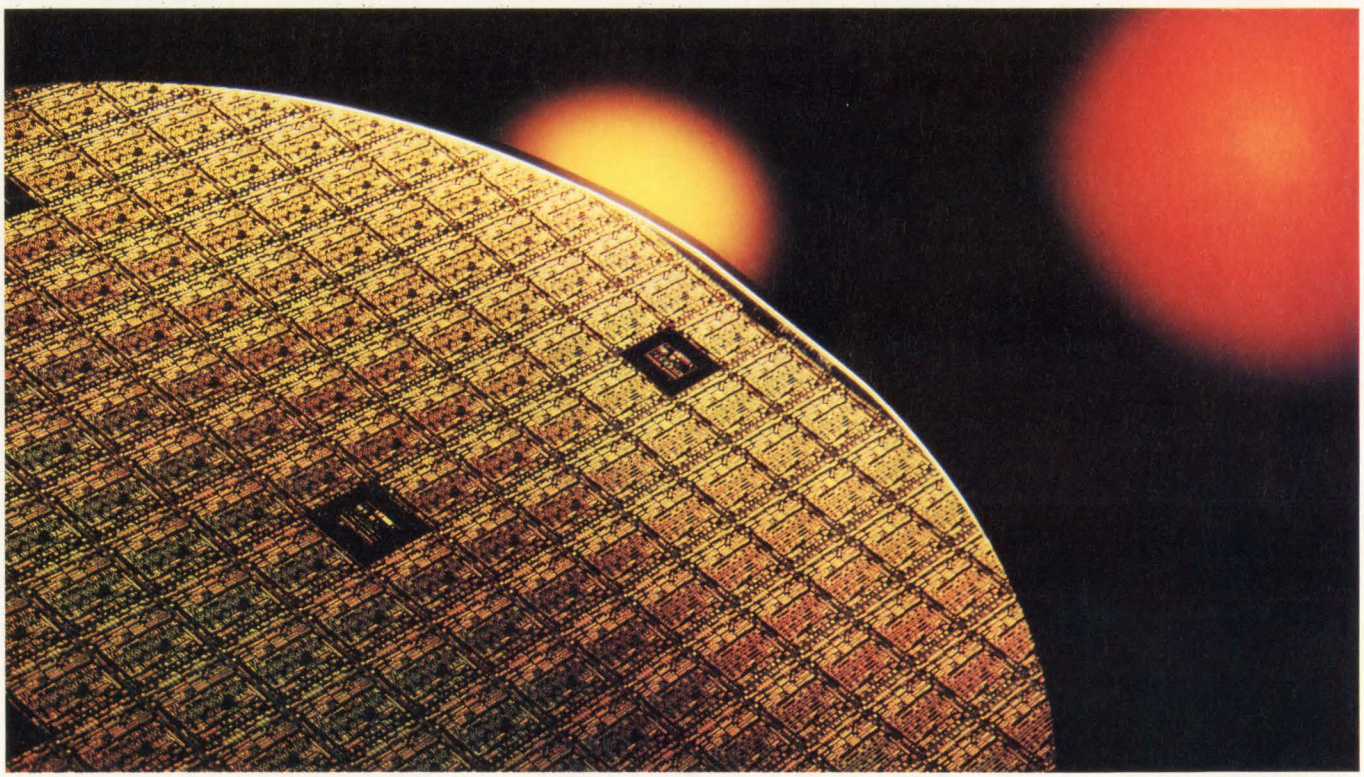

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The M650's dual-port mode architecture accomplishes in hardware what you can't do as well in software. Even after you've linked up multiple UARTs and messed with glue logic.

So the M650 can take the heat off your CPU and function comfortably as a communications sub-processor. And, in power-down mode, be sensitive to the low power demands of your laptop and notebook PC designs.

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VOL. 30, NO. 12 SEPTEMBER 1991

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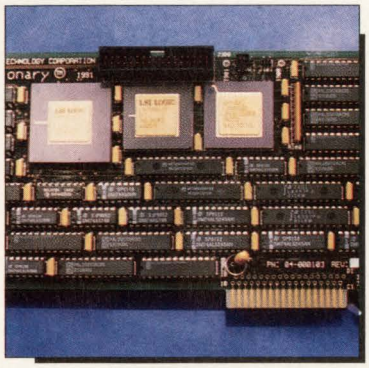

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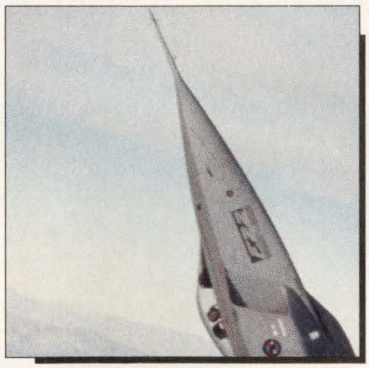
TECHNOLOGY DIRECTIONS



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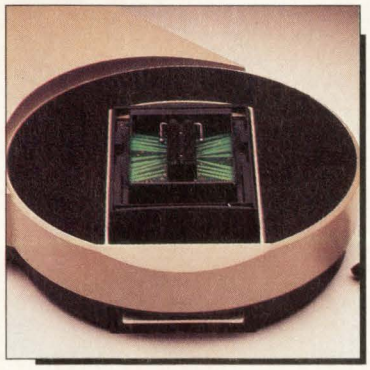
TECHNOLOGY AND DESIGN FEATURES



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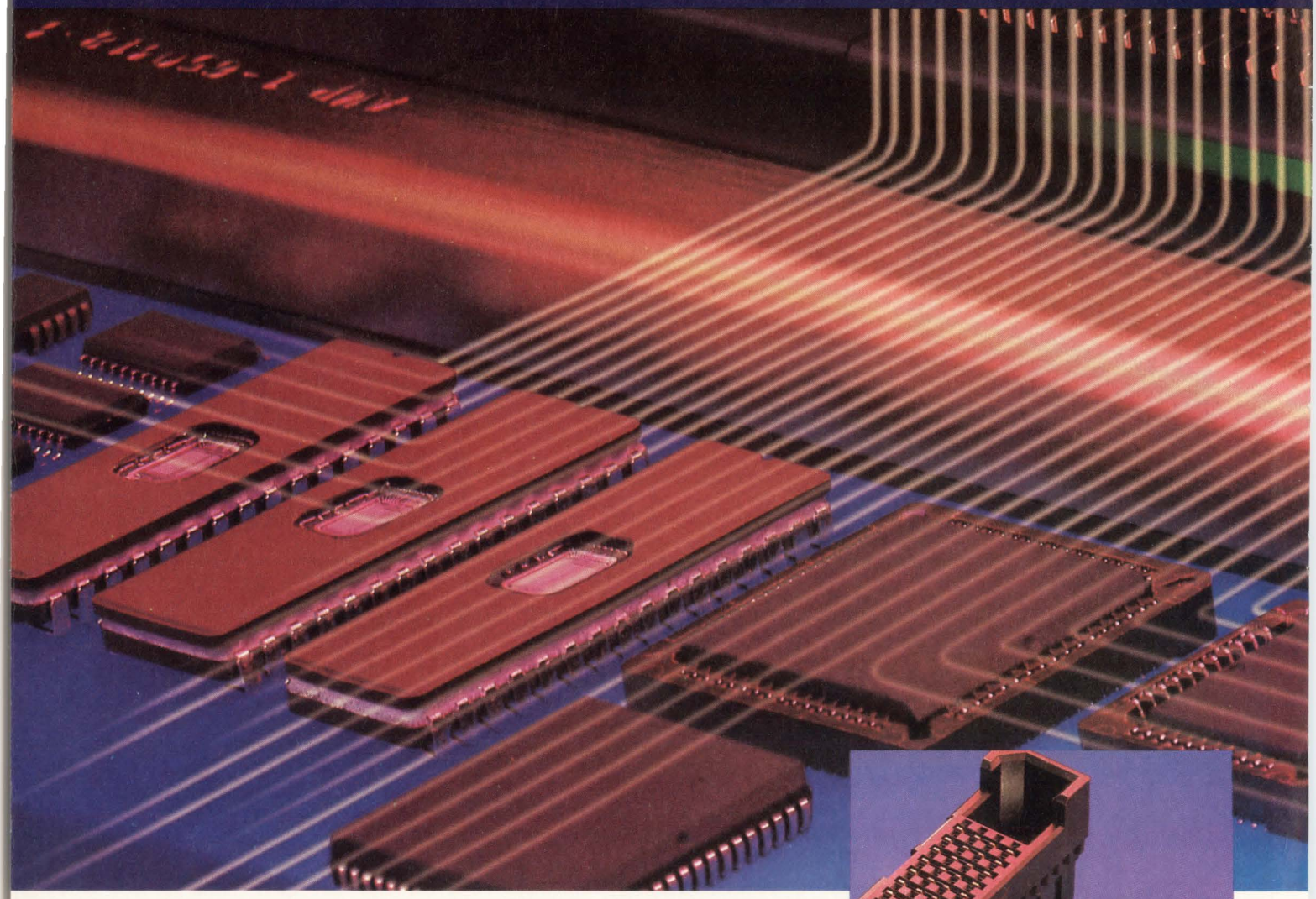
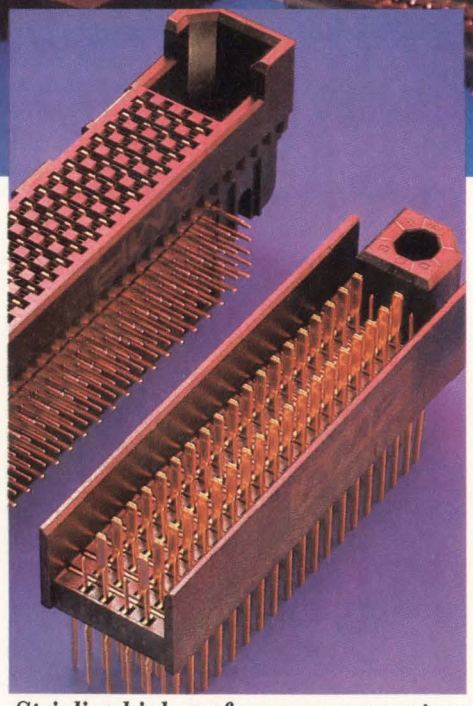
NEW PRODUCT HIGHLIGHTS

DEPARTMENTS

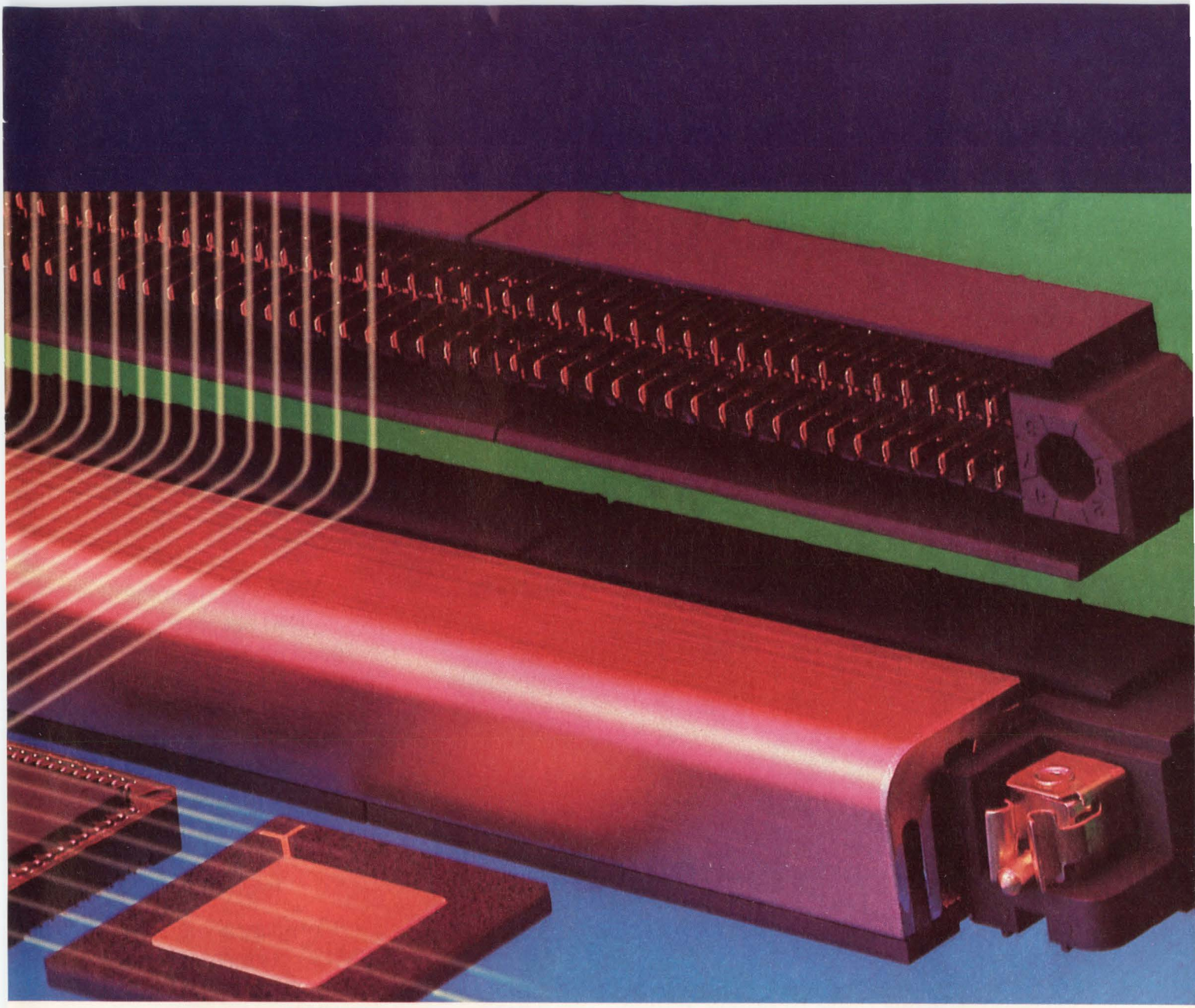
Making the interface transparent to sub-nanosecond rise times.



THIS IS AMP TODAY.



Stripline high-performance connectors.



'Fast silicon' (rise time≤1 ns) requires strict impedance control. Conventional connectors give up half their pin count for this – a sacrifice you can do without.

Our modular, scalable Stripline 100 connector system can accommodate edge rates of 250 ps (500 ps at <3% crosstalk), and still give you 40 signal lines per inch – all four rows on a .1"x.1" grid. Reference planes isolate individual signal columns within the standard grid geometry, creating an interface completely transparent to high-speed logic.

Stripline 100 connectors deliver more than raw speed, too. Each reference plane can distribute three amps, and sequenced mating is available for ground, power, and two signal levels.

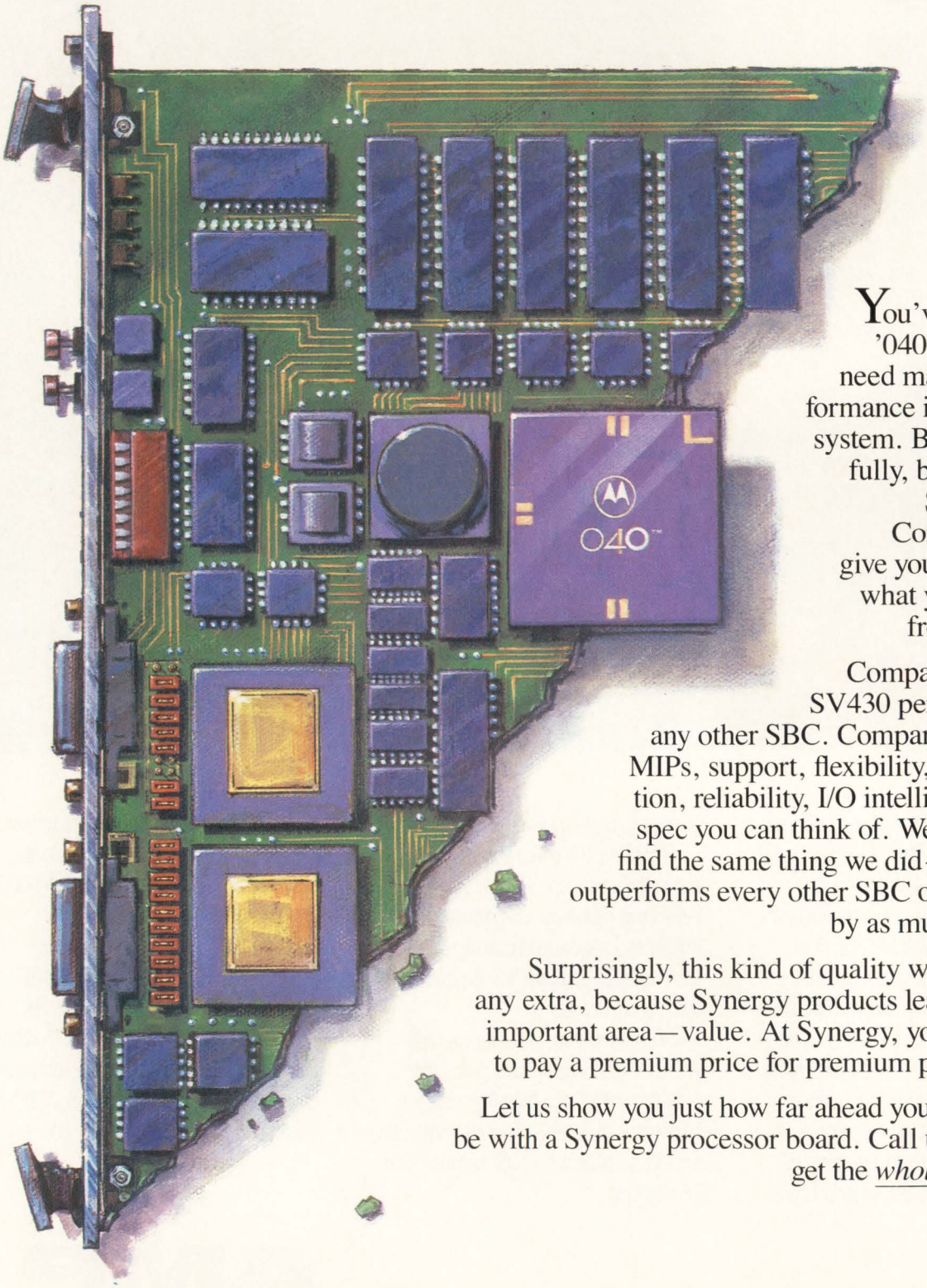
Manufacturing is easier as well. ACTION PIN compliant posts (for existing 0.040" pcb holes) simplify backplane assembly, and all materials are compatible with high-temp reflow processing.

In fact, sub-nanosecond logic just got easier all around, and there's an easy way to 'bring yourself up to speed' on this exciting technology: call our Product Information Center at 1-800-522-6752 (fax 717-561-6110). AMP Incorporated, Harrisburg, PA 17105-3608. In Canada call 416-475-6222. For design assistance in characterized backplane assemblies, contact AMP Packaging Systems, 512-244-5100.

AMP

CIRCLE NO. 5

Why Settle for ½



You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may give you only half of what you expected from the '040.

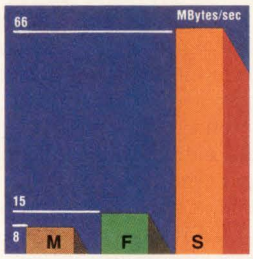
Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPs, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the SV430 outperforms every other SBC on the market by as much as 150%.

Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

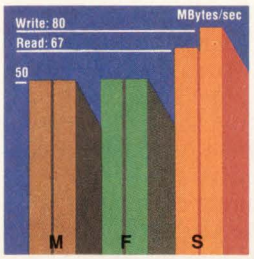
an '040 Board?

Compare our specs. Synergy is superior across the board!



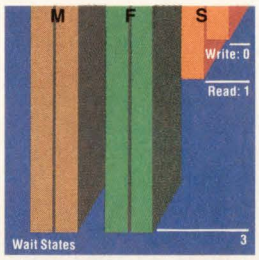
VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



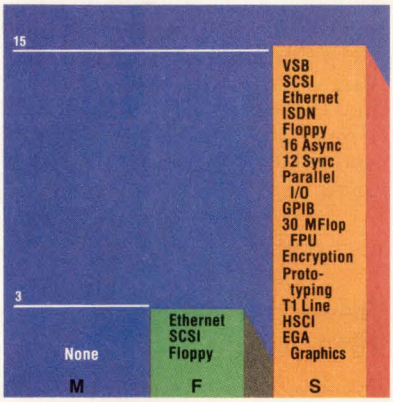
DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.

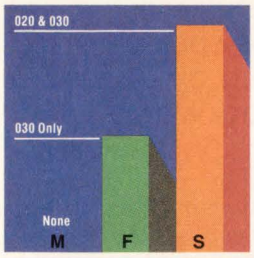


I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.

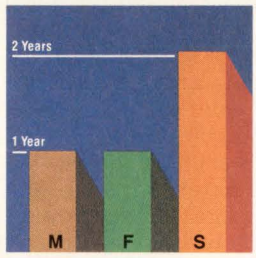
Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.



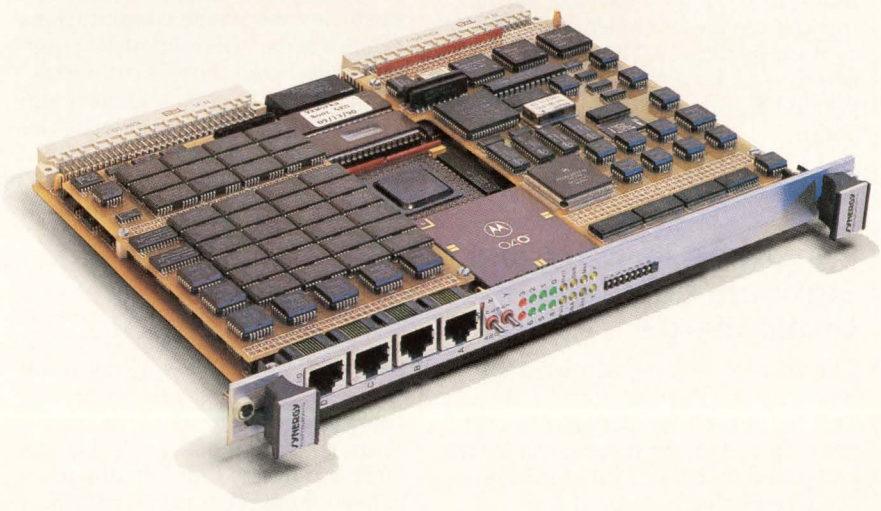
'020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



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SYNERGY microsystems

CIRCLE NO. 6

NEWS BRIEFS NEWS BRIEFS NEWS BRIEFS NEWS BRIEF

Tough act to follow from Actel

It seems that Actel (Sunnyvale, CA) is no longer willing to let competitive field-programmable gate array (FPGA) maker Xilinx (San Jose, CA) walk away with a majority of market share. About two weeks ago, Actel strengthened its position in the FPGA market by expanding its Industry Alliance Program and, at the same time, introduced the second member of the ACT 2 family, claiming it to be the industry's fastest FPGA.

Unlike Xilinx, Actel recognized early that FPGAs would often be used for prototyping rather than for production, and has thus committed itself to providing a migration path to masked gate arrays. With the addition of alliance members Aldec, Gould AMI and Teradyne, Actel now offers design support to users through technical relationships and cooperative marketing efforts with 16 design automation, gate array, synthesis, and PLD tool vendors. "Our expanding relationships with industry leaders such as these reinforces the Actel Industry Alliance Program's goal of providing customers with technology-transparent design solutions to meet their design-to-production needs," says John East, Actel's president and CEO. "Actel clearly is becoming the device of choice for today's system designers," boasts East. It remains to be seen whether market figures will live up to the claim.

—Barbara Tuck

Integrated Systems and Software Components Group merge

The merger between Integrated Systems Inc (Santa Clara, CA) and Software Components Group (San Jose, CA) brings together two companies whose individual areas of expertise complement one another for the designers of real-time embedded systems. ISI's strengths lie in the control engineering and simulation fields, while SCG's strengths are in real-time operating system kernels, pSOS+ and associated software modules, such as file system managers, multiprocessing software and debuggers. ISI's CASE and development tools include ones that simulate the execution of embedded code, as well as the behavior of real-world devices such as motors, gears, sensors and actuators. The company's SystemBuild development tool can also generate documented compilable code automatically. One of the fruits of the merger is the integration of a real-time operating system into ISI's development and simulation environment—something that was previously missing from ISI's repertoire—and the ability to produce completely integrated embedded code using only the tools from a single vendor.

—Tom Williams

DSP chips speed processing by doing math "backwards"

A digital signal-processing filter IC developed by researchers at Queen's University (Belfast, Northern Ireland) can perform 250 multiplications and additions per second; about 10× the speed of current commercial devices. The infinite impulse response (IIR) filter performs recursive computations "backwards." Instead of starting with the least-significant operations, it starts with the most significant operations and feeds the results back immediately instead of waiting for the entire process to be completed. The result is an almost tenfold speed-up.

The IIR filter is expected to find applications in a variety of radar and telecommunications systems as well as in high-definition television (HDTV). Ten working prototypes of the chip have been fabricated at the VLSI Technology foundry in San Jose, CA. The design is patented and can be licensed from a company called Integrated Silicon Systems, established by Queen's University.

—Tom Williams

CFI demos IC standard prototype

The CAD Frameworks Initiative (CFI) has just completed its first public standards demonstration outside the area of traditional electronic CAD. CFI's Technology CAD (TCAD) Framework group has unveiled working prototypes of its first two proposed standards at Stanford University (Palo Alto, CA). TCAD comprises computer-aided engineering for semiconductor device and process design, technology characterization for circuit design and IC design for manufacturability. It includes modeling fabrication processes and electrical simulation of devices and circuits.

As is the case with all of CFI's efforts, the TCAD offering represents cooperation among IC vendors, computer and communications manufacturers, software vendors, and universities. IBM (Armonk, NY), Digital Equipment Corp (Maynard, MA), Intel (Santa Clara, CA), and Texas Instruments (Austin, TX), as well as the University of Michigan, Stanford and MIT are among the participants in the TCAD effort.

—Mike Donlin

Reverberations of IBM/Apple

It seems everything that could be said of the IBM/Apple letter of intention has already been said and repeated. And while it's true on a number of fronts, there's been little speculation on any kind of I/O platform. Apple has been increasing the use of its version of the early NuBus format, most recently incorporating the faster version in its newest computers. And while technically an open standard, the bus has a relatively limited following among add-on board vendors.

IBM, with its MCA bus, on the other hand, has seen a number of board makers jump on the bandwagon to provide needed functions for the PS/2. But with the introduction and subsequent mushrooming sales of its RS-6000 workstation products, IBM has been caught

Continued on page 10

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Continued from page 8

short in its ability to support OEMs needing specialized I/O.

So IBM executives are making serious inquiries into other possible I/O bus architectures that will meet its requirements: fast I/O and a large contingent of board makers offering a wide variety of board types. While IBM has flirted with Futurebus+, it seems to be taking VMEbus or SBus more seriously.

Though a big departure for IBM—and Apple—such an approach might not be inconsistent with IBM's needs. And while Sun's SBus is certainly in contention—and consistent with IBM's desire for a small-form-factor, low-power bus—political considerations and/or, SBus' tie to Sun/OS and Sparc might be a problem. VMEbus is less encumbered with technical and political baggage, but still carries some vestige of Unix System V. But should Motorola's computer group start thinking of a RS-6000 approach to its Multi-Personal Computer line, things might become very interesting. (You can send us your comments on all this by using the Reader Inquiry Card.)

—Warren Andrews

Shielded VMEbus connector

The VFEA (VME Futurebus+ Extended Architecture) technical committee of VITA (VME International Trade Association) is reviewing the virtues of a new Eurocard connector. The new connector, developed by AMP (Harrisburg, PA) is intended to provide shielding protection at the board/backplane interface.

But the VFEA technical committee seems more entranced with the power-handling capability of the new connector than its EMI protection. According to tests run by AMP, the lower ground plates wired in parallel will handle just under 50 A, while the upper plates will handle just over 50 A. "We'll have to include something in the specification," says VITA technical director, Ray Alderman, "to make sure people don't try to use the connector to its full power capacity. There'll be no way of getting that kind of heat out of a VMEbus box." The committee is expected to make a decision about what to include in the specification in the next few weeks. Currently, many are more concerned with getting the power to VME boards and then "we'll figure out what to do with the heat when the problem arises," they say.

—Warren Andrews

New complementary technology for GaAs

Researchers at Honeywell (Minneapolis, MN) have developed a complementary gallium-arsenide technology that offers significant improvement over traditional GaAs. Dubbed C-HFET, this new complementary technology is based on p-channel and n-channel heterostructure field-effect transistors. C-HFET combines the speed of other GaAs and ECL technologies with the low-power consumption and density of CMOS, according to Honeywell. Devices based on C-HFET technology could become a viable alternative for future supercomputer and workstation designs.

The most recent device to use C-HFET is a 4-kbit SRAM that operates at a clock rate of 250 MHz. At 100 mW, the C-HFET SRAM's power consumption is only one-fifth that of equivalent GaAs memories with similar speeds. According to Honeywell, its C-HFET circuits consume significant power only during the short gate-switching period. As a result, the total power consumption is much less than devices based on n-channel GaAs or ECL technologies.

—Jeffrey Child

i960MX shoots at military designers

With its multiple data and address buses, Intel's (Chandler, AZ) i960MX, the $1,500 high-end military processor, poses some tough interface problems. Even for Intel. Intel representatives admit that to get a board product to market, they've contracted out the design of an MX-based Multibus II-based CPU board to none other than Tadpole Technology (Cambridge, England). And although photographs of the Tadpole MX board have been distributed by Intel, it admits that the product won't really be ready until next year. The good news is that Intel is working on a multichip module (MCM) based around the i960MX processor that may take some of the pain out of building a second-level cache subsystem around it, since the MCM will include a second-level cache controller. While the design world holds its breath for the Intel products, i960 Ada aficionados might like to look at an i960MX Ada simulator and cross compiler developed by Irvine Compiler Corporation (Irvine, CA—if they can. "We're under contract to build an Ada compiler for the i960MX chip," says Joe Kohli, vice-president of sales and marketing, "but I can't tell you when it will be available."

—David Wilson

Sparc in the news

Just as Cypress Semiconductor's Ross Technology subsidiary (Austin, TX) gets set to unveil its Sparcore set of MBus modules, some of Cypress' own customers have already been made privy (under nondisclosure agreements) to future Cypress plans in the superscalar arena. The Mile, or Multiple Instruction Launch and Execute, is Cypress' next-generation processor design scheduled for official unveiling in the second quarter of next year. In another Sparc-related development, Tadpole Technology (Cambridge, England) has switched to Ross Technology to supply it with chips for its Sparc notebook, to be launched at Comdex in Las Vegas this year. The company previously had disclosed that it was using LSI Logic's Sparkit chips in the design of the product.

—David Wilson

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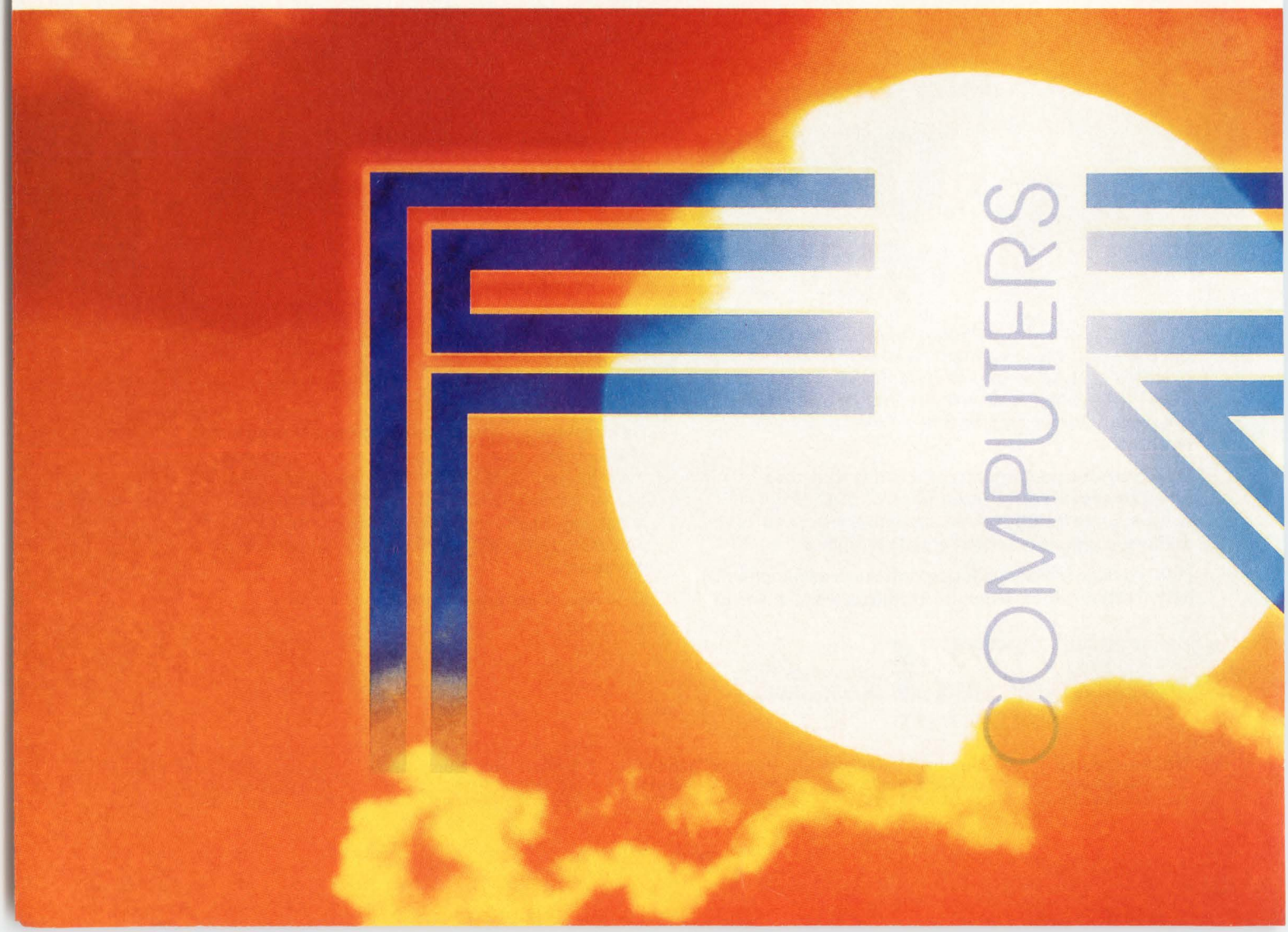

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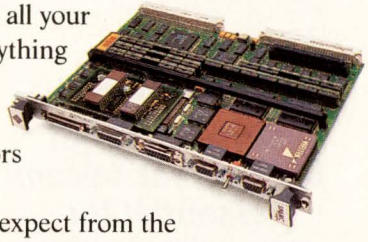

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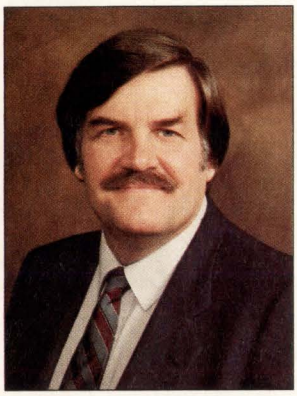
David beat Goliath only in the Bible

I'm afraid that bigness has become essential for economic survival, whether it's in electronics, in computers or in banking.



John C. Miklosz
Associate Publisher/
Editor-in-Chief

I don't like big business. I don't like big league sports because they've become big business. I don't like big-time entertainment because that's become big business, too. And most of all, I don't like big government. I don't like them because sooner or later, big business, big government—big anything—abuses its power, grows out of touch with the people it's supposed to serve and stifles creativity. It leads to obscene CEO salaries and bonuses, to immovable bureaucracies and S&L debacles, to Roger Clemens pocketing $100K a game (more or less) and Bruce Willis getting 10 million bucks for making a bomb.

Like a lot of other folks, I fantasize about small, tightly knit entrepreneurial companies with great bosses and happy, innovative, well-paid employees; about many Mr. Smiths in Washington; the Bailey Bros. Building & Loan in Bedford Falls; Babe Ruth, Ty Cobb and Joe Dimaggio playing on grass; and Spencer Tracy and Katherine Hepburn who made more, and more memorable, films than all the Bruce Willises, Robert Redfords and Warren Beatties combined. The fantasy may have been reality at one time, but the world's needs today can't be met by small scale efforts. And even if they still could, the size and complexity of today's world economy relentlessly fuels the drive to bigness. Our fantasies may keep us fighting the reality, but other societies and economies that don't entertain the same fantasies will ensure that our's become true and that our industry, our banking and our economy becomes small by today's standards.

This need for bigness to compete and survive in today's world shouldn't be forgotten when we look at developments in our industry. We can comment interminably on AT&T's acquisition of NCR; on Microsoft's "tyranny" of the PC world; on the IBM/Apple/Motorola deal; on IBM's deal with Siemens; on Borland's acquisition of Ashton-Tate; on the Intel/AMD battle over the 386; on whether or not U.S. Memories was a good idea. And we can bemoan the evils of big companies, and big deals and market dominance ad nauseam; or the evils of regulation or industrial policy to the same degree. But even if we threw all of the companies we've been talking about lately together, they wouldn't match in size the largest of the Japanese industrial groups. NEC, for example, may not be an IBM or an AT&T, but it's part of the Sumitomo group, one of several *keiretsu* in Japan that boast annual revenues of between $200 billion and $400 billion. Compare this with IBM's $70 billion and AT&T's paltry $37 billion. And the Sumitomo group is headed up by the Sumitomo bank, only one of the seven Japanese banks counted among the top 10 in the *world*. To put *that* in perspective, the recent Chemical Bank/Manufacturers Hanover merger still didn't put them among that select group.

No, I don't like big business, or big government, or big sports or big entertainment. But I'm afraid that bigness has become essential for economic survival, whether it's in electronics, in computers or in banking. David beat Goliath only in the Bible. That was also in an earlier, simpler time.

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CIRCLE NO. 10

CALENDAR

CONFERENCES

September 11 - 13
BUSCON/91-East

BUSCON/91-EAST
SEPTEMBER 11-13, 1991
OMNI SHOREHAM HOTEL
WASHINGTON, D.C.

Omni Shoreham Hotel, Washington, DC. The industry's leading board- and systems-level show makes its mid-Atlantic debut this year in Washington, DC. The first glimpse of advances in bus architecture, from Multibus II to VMEbus, Futurebus+, SBus, and Turbochannel, plus the newest offerings among other elements of systems architecture—boards, backplanes, chips, embedded software and operating systems—will highlight the show. At the technical seminar program, attendees will have the opportunity to learn about new bus architectures directly from the people who developed them. Information: Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06856, (800) 243-3238, fax (203) 857-4075. **Circle 202**

September 24 - 27
Embedded Systems Conference

Santa Clara Convention Center, Santa Clara, CA. The Third Annual Embedded Systems Conference will offer 75 intensive lectures, panel discussions and workshops on real-time programming, microprocessors, microcontrollers, CASE, embedded project management, programming languages, debugging and algorithms. Tutorials will be offered on building software teams and synthesis. Information: Angela Hoyte, Miller-Freeman, PO Box 7843, San Francisco, CA 94120-7843, (415) 905-2354, fax (415) 905-2630. **Circle 203**

October 1 - 3
SysComp/91-East

SYSCOMP

Royal Plaza Trade Center, Marlborough, MA. The industry's first exclusive OEM systems/sub-systems components conference and exhibition. Workshops and technical sessions will focus on technical solutions and directions involving microprocessor system architecture, OEM systems and software, power sources, interface technology, mass storage, systems packaging and manufacturability. Exhibitors will include vendors of critical systems building blocks, including software, boards, complex microcircuits, power sources, storage systems, displays and other ancillary products. Raytheon's famous Patriot missile system will also be on display. Information: Betsy Anderson, marketing specialist, *COMPUTER DESIGN*, One Technology Park Dr, PO Box 990, Westford, MA 01886, (508) 392-2209, fax (508) 692-0525. **Circle 204**

October 7 - 9
Connectors and Interconnections Technology Symposium

1991 IICIT SAN DIEGO

Sheraton Harbor Island Hotel, San Diego, CA. The 24th Annual Connectors and Interconnections Technology Symposium sponsored by the IICIT will feature over 50 technical presentations, seven tutorials, including a special session by a DESC representative, special forums and guest speakers, and a trade show. Information: Kathy Billa, IICIT Headquarters, 104 Wilmot Rd, Suite 201, Deerfield, IL 60015, (708) 940-8800. **Circle 205**

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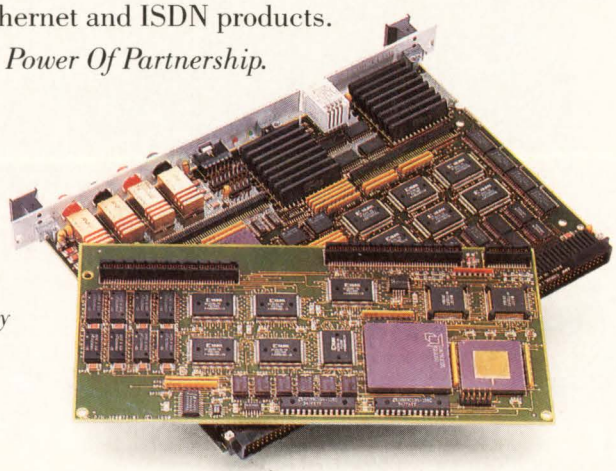

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CIRCLE NO. 13

CALENDAR

CONFERENCES

October 21 - 25
COMDEX/Fall '91

Las Vegas, NV. The 13th international fall trade show for computer distribution professionals has been expanded into three programs: the main conference program, the network computing conference and the multimedia conference. The main conference will feature discussions about the industry in transition; marketing; new technology; pen-based computing; resellers and vendors coping with changes in distribution channels; applications software; and portable computing. The network computing conference features more than 25 detailed technical sessions about fundamentals, applications, designs, and managing and planning of network computing. Also, this series will coincide with a network computing exhibition. The multimedia conference features sessions about the evolution, applications, software, and hardware of multimedia. Information: The Interface Group, 300 First Ave, Needham, MA 02194-2722, (617) 449-6600, fax (617) 444-0165. **Circle 206**

October 26 - 30
International Test Conference 1991

Opryland Hotel, Nashville, TN. The 22nd International Test Conference offers technical programs and exhibits of test-related hardware and software. A three-day technical program reflects the theme: "Test: Faster, Better, Sooner." This program consists of a plenary session, 40 formal paper sessions, a poster session and panel sessions. Papers and posters will cover numerous aspects of test from chip through system-level and present innovative ways to solving today's design and test problems. The test week is rounded out by two days of tutorials that explain or expand on test topics presented in the technical session. Information: International Test Conference, 514 Pleasant Valley Blvd, Suite 3, Altoona, PA 16602, (814) 941-4666, fax (814) 941-4668. **Circle 207**

October 30 - November 1
Analog & Mixed-Signal Conference

Santa Clara Marriott, Santa Clara, CA. The Analog & Mixed-Signal Conference is dedicated to the unique needs of mixed-signal design. Over 50 lectures and workshops will focus on subjects including transmission line effects in high-speed design; mixed analog/digital design; modeling, simulation and test; and much more. Information: Angela Hoyte, Miller-Freeman, PO Box 7843, San Francisco, CA 94120-7843, (415) 905-2630, fax (415) 905-2630. **Circle 208**

Would you like your event listed here?

Computer Design *can include a calendar announcement for your upcoming conference or seminar as long as it's received at least three months prior to the date of the event. Be sure to include a specific location, a description of the conference/seminar content, and a contact name, address and telephone number.*

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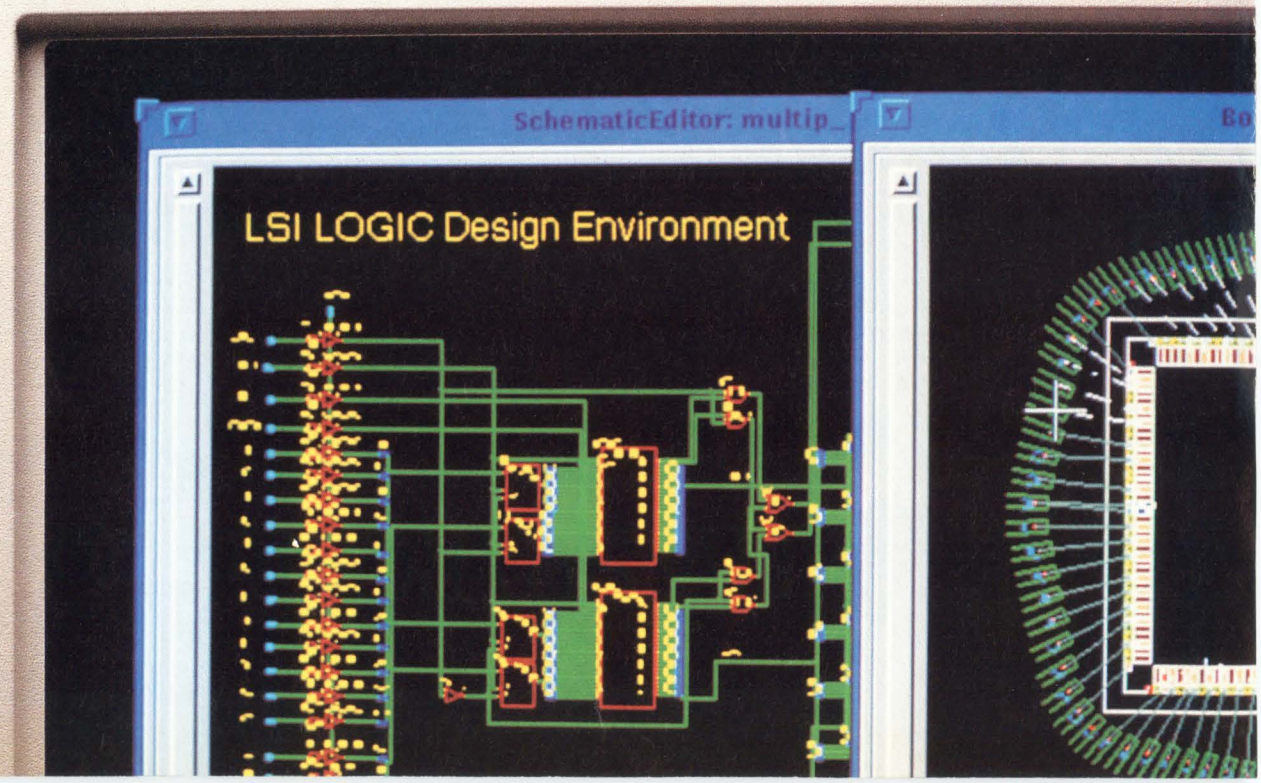

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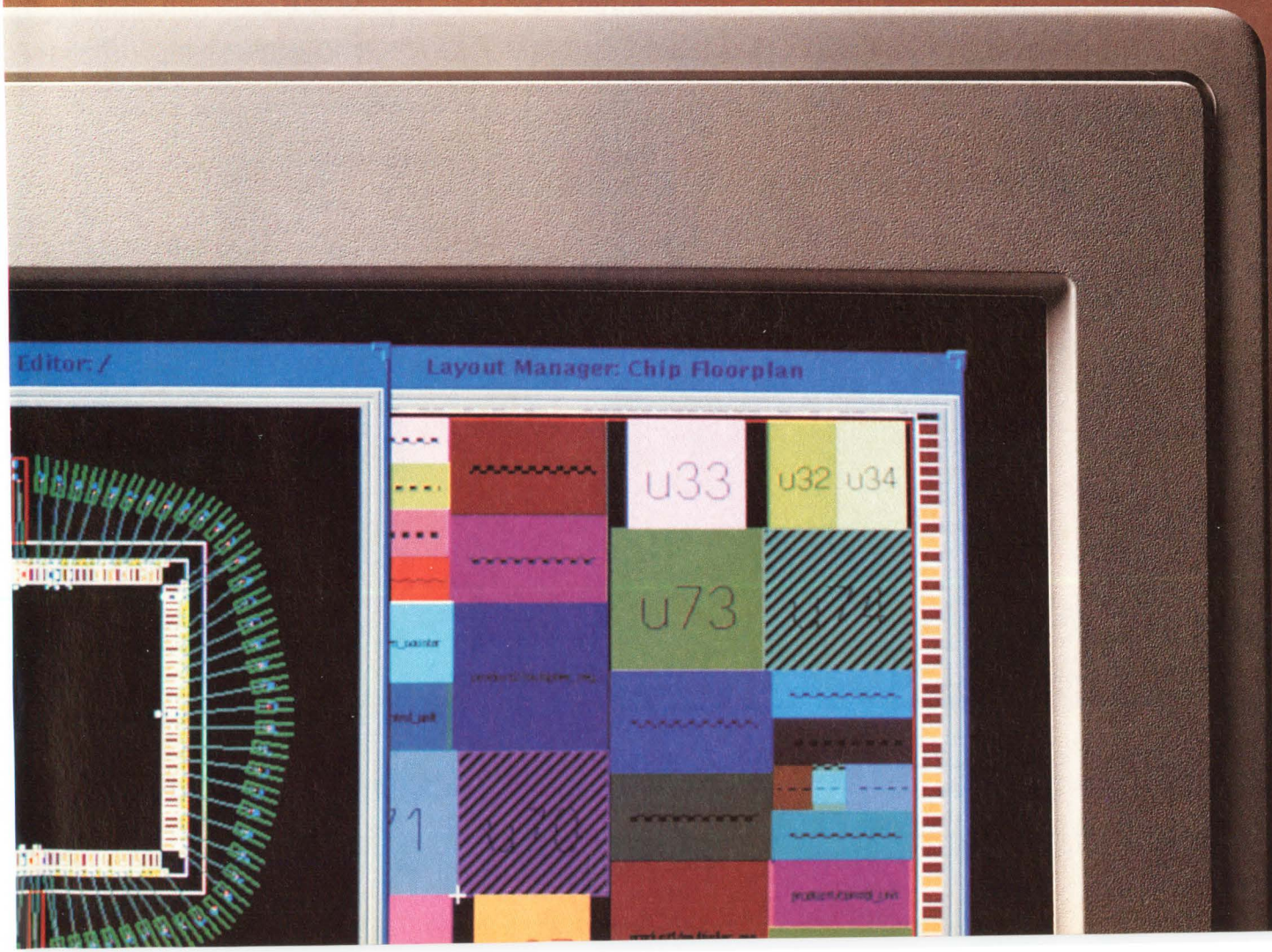

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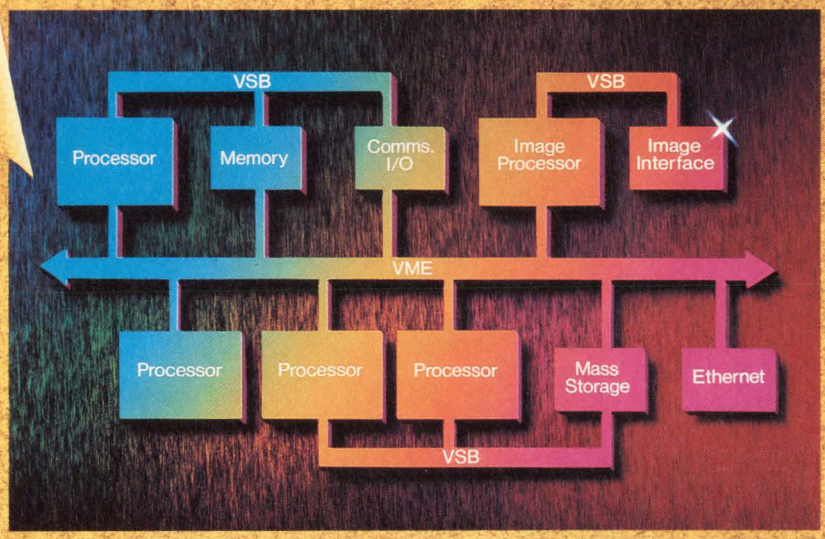

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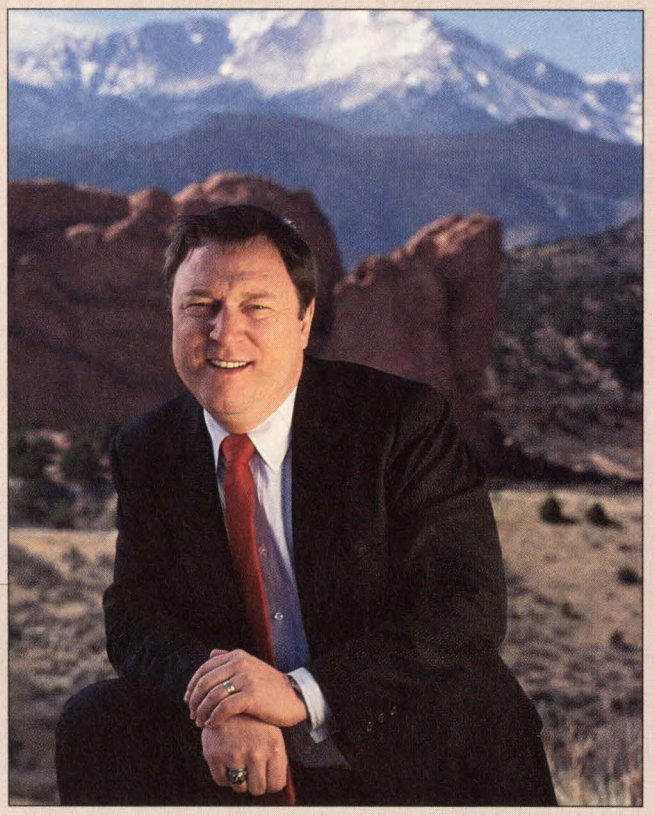
Wayne Gutschick on: Programmable logic



Programmable logic is well on its way to replacing standard LS logic. Programmable logic had its beginning when a design team led by John Birkner (then of Monolithic Memories) developed the first PAL in 1976. It has since advanced from limited use as specialty devices to wider use in digital design.

Asprogrammable logic's use increased, so have the capabilities of the design software supporting it. Programmable logic design software tools have evolved from early programmable logic device compilers to today's sophisticated design synthesis software that's fully integrated into CAE design environments. These design tools will continue to grow more powerful and will begin to incorporate industry standards such as VHDL.

Users of programmable logic have also progressed. Early adopters wrestled with the technical challenges of limited silicon capabilities and the rudiments of programming devices via fusemaps. Designers of today's more complex hardware face complex technical and strategic challenges in responding to changing customer needs while reducing time-to-market for their products.

Programmable logic today

While some programmable logic manufacturers have used different names and terminology to position their respective products, all of today's technologies can be placed into one of the three general categories: programmable logic devices (PLDs), programmable multilevel devices (PMDs) and field-programmable gate arrays (FPGAs). The chart titled "Relative merits of digital logic solutions" indicates the relative strengths of these technologies. Note that design time is best with LS, PLDs, and PMDs, while full custom and standard cell technologies shine in the category of complexity and added features. Also note that PLDs consume more power than the other technologies.

The percentage of gates used in programmable devices is a function of the application, the efficiency of the design, and the quality of the design software used. Using LS, most gates will be utilized because LS devices were developed for specific applications. Because PLDs are general purpose in nature, it's extremely rare to find all the gates of a particular PLD used. If cost is not a consideration, the best combination of both speed and usable gates is found in gate array and standard cell technologies.

According to Andy Rappaport, president of Technology Research Group, the programmable logic segment of the digital logic market is the fastest growing segment. This segment is projected to grow from 764 million dollars in 1990 to 1.765 billion dollars in 1995, representing an average compounded growth rate of 18.2 percent.

The PLD segment of the market is driven by speed. These devices are now available with delay times of 5 ns. Devices with 3.5-ns speeds will be available in the near future. The combination of increasing speeds and higher densities is responsible for the erosion of the standard LS market. Wayne Spence, vice-president of worldwide design support for Texas Instruments' semiconductor group, supports this idea. "We will continue to see programmable logic devices replacing TTL logic devices. More and more, the basic building blocks of digital design will be programmable devices."

At the other end of the programmable logic spectrum, FPGAs continue to make inroads into what was considered the low-end gate array market. FPGAs are still in their infancy. As Wes Patterson, executive vice-president and chief operating officer of Xilinx, points out, as we continue to learn more about the architectures and processing of these devices, their performance will improve at a compounded rate of 50 percent.

The PMD segment, such as Altera's Max, and AMD's Mach families, addresses the middle ground between PLDs and FPGAs. PMDs, which are also in their infancy, offer the designer an effective tradeoff between speed and density. "PMDs will extend beyond

what used to be considered complex PLDs, and will start competing with FPGAs," says Andy Robin, director of marketing, programmable logic, AMD.

What's driving the growth of programmable logic? There are a number of factors: increasing pressure on manufacturers to deliver products to market in shorter periods of time; their desire to pack more functionality into a given space; and the insistence of manufacturers to protect the proprietary nature of their products. There are 4.5 PLDs on the average digital PCB. This number will continue to grow as more digital design engineers take advantage of programmable logic technology.

Early devices were easy to understand and with its low density, designers could easily mark on a fusemap which fuses were to be blown. As density increased, it became more cumbersome for engineers to deal at the fusemap level. Recognizing this problem, MMI developed the first software tool to aid PLD design engineers, and introduced Palasm in 1978. Palasm allowed engineers to describe their design in terms of Boolean equations. It also provided some basic logic equation-reduction algorithms. The introduction of Palasm was a significant milestone, allowing digital hardware designers to take advantage of PCs.

RELATIVE MERITS OF DIGITAL LOGIC SOLUTIONS

	Standard Logic (LS)	PLDs	PMDs	FPGAs	Gate Arrays	Standard Cells	Full Custom
Average Unit Price at high volume	1	3	5	4	2	2	3
Average Unit Price at Low Volume	1	4	6	5	9	10	20
Design Entry Costs (CAD System)		1	2	4	5	6	20
Non-Recurring Engineering Costs	N/A	N/A	N/A	N/A	9	10	20
Space Consumption	10	6	5	4	2	1	1
Design Time	1	1	1	2	5	6	20
Complexity and Added Features		8	6	4	2	1	1
Redesign Flexiblity	2	2	1	2	9	10	200
Test Program Devel.		1	2	3	6	8	20
Speed (gate)	1-5	1	6	5	4	3	3

Programmable logic software

Following Palasm, as new PLD IC manufacturers entered the market, they introduced their own proprietary compiler software for equation entry and logic equation reduction. By 1984, the first third-party tools, Data I/O's Abel and Assist Technologies' Cupl had been introduced. The advantage of these early compilers was that they supported devices from several IC manufacturers.

In 1988, Minc introduced the first synthesis tool which targeted programmable technology. Synthesis technology lets engineers describe larger and more complex designs. It frees them from learning all the intricacies of a device's architecture. In 1989, Mentor Graphics was the first CAE vendor to fully integrate PLD synthesis technology into a total design environment. Since then, many other leading CAE companies have integrated programmable logic synthesis technology into their design environments.

Compiler software and synthesis technology address different needs of the digital hardware designer. Engineers use compiler software to describe a design that will fit into a single device. When a design does require multiple devices for its implementation, and compiler software is used, these designs are approached as a single device application. These device-specific tools require designers to have intimate knowledge of the particular device that the design will fit into. Designers often will focus on only a small number of architectures. Because compilers are device specific, designs too large to fit into a single device must be manually or interactively partitioned across multiple devices. Similarly, test vectors used for simulation also need to be partitioned manually or interactively. Partitioning is a difficult and time-consuming manual process. In some cases, not all of the functionality of the device selected is directly supported by the compiler.

Today, compilers such as Data I/O's Abel can handle designs up to 1,000 gates. It's an excellent choice for PLD designs requiring a single device implementation. When PMDs or FPGAs are the targeted technologies, however, designers must divide the design into a series of modules with gate counts less than 1,000. "Abel works best as a module generator," says David Kohlmeier, engineering manager of Data I/O's design software business unit, in a recently published article. But, the design must still be manually or interactively partitioned into modules. Also, since compilers function well up to 1,000 gates, it isn't possible to simulate the entire design when this limit is exceeded. One advantage of compiler software is that it's relatively inexpensive. Prices for compiler software running in a DOS environment range from $500 to $3,000.

Synthesis technology addresses the needs of designers who want to functionally simulate an entire design prior to fitting or routing. Larger, more complex designs can be described in a single source file. The entire design can then be simulated prior to technology or device selection. Once the designer is satisfied with the simulation results, synthesis tools will automatically target various technologies and architectures. If the design is too large to fit into a single device, the

tool automatically partitions the design and its test vectors across a multiple-device implementation.

With most of these tools, the user can also input design constraints and criteria. The tool will consider this information and automatically select from its device library the device(s) that will fit the design and meet the design criteria. These tools also provide flexibility for manual intervention into device partitioning and the device-fitting process, which allows "tweaking" the design, should that be desired. Another attribute of synthesis tools is that they generate a number of solutions for the designer to evaluate. Price is the major disadvantage of these tools, they cost from $2,000 in the DOS environment to over $10,000 running in networked Unix environments.

Synthesis technology has been fully integrated into the design environments of the leading CAE vendors. Programmable logic parts of a board can be designed with the same design methodology used for designing the remainder of the board, including ASICs. Also, the entire board can be simulated, including ASICs and other circuitry present on the board.

Software tools can be classified by the types of technologies they support. Most compiler suppliers rely on the IC manufacturer to provide fitters for the support of PMDs and FPGAs. But, since compilers handle designs of up to 1,000 gates, FPGA vendors have had to develop their own tools or work with third-party synthesis companies. "The importance of software grows in proportion to the sophistication of our devices," observes John East, president of Actel. To support these larger devices, FPGA vendors have had to rely on schematic capture as their primary input method. The drawback of schematic entry is that it's a structural approach, which is effective for designing "glue" logic, but is less effective for describing behavioral designs such as state machines. "Integrating VHDL with synthesis tools makes it possible for digital designers to use the industry-standard language for high-level behavioral design," says Erich Marschner, president of CLSI.

Programmable logic users

New FPGA synthesis tools allow the ASIC designer to design using the ASIC library of choice. Once the design has been completed and synthesized through the ASIC tools, the output of the ASIC tool is fed into the FPGA synthesis tool. This tool then optimizes the design and places the low-speed portion of the design into FPGAs, while allowing the high-speed or critical nets to be placed into high-speed PLDs. Using this approach, the designer makes all the design tradeoffs in favor of the production silicon—the ASIC—rather than in favor of the prototype silicon—the FPGA.

There's a fundamental change occurring among device users. When programmable logic devices were considered specialty devices, they were designed as an adjunct to the board design. This process involved: the programming of a device; plugging the device into a breadboard; debugging the device using traditional instrumentation; modifying the design; reprogramming the device; placing the device back into the breadboard, debugging, and repeating this process until the correct functionality was achieved. Today, designers depend more on simulation and less on breadboarding for debug. "The days of building multi-breadboards and prototypes are numbered. This expensive and time-consuming process will be replaced with board-level simulation which includes programmable logic devices," claims Lutz Henckels, president of North American Operations, Racal-Redac.

To address what users want, programmable logic synthesis technology is becoming more important in the overall design process. The technology is moving from point tools to fully-integrated design solutions. "PLD and FPGA synthesis tools are beginning to play a more important role as design engineers look to concurrent engineering to help reduce time-to-market and improve their productivity. The programmable and reprogrammable nature of these devices will lead to interesting applications as concurrent engineering continues to evolve," says Gerry Langeler, president of the systems group, Mentor Graphics.

Programmable logic—the future

As manufacturers of electronic equipment continue to face cost and time-to-market pressures, the attraction of PLDs will increase. A number of factors will influence the future. Among these factors are increased silicon performance, in terms of speed and density, as well as device pricing. We have already witnessed substantial price reductions. As use increases, prices will decline. Additional device flexibility, allowing a device to be used in a number of different applications, will also impact pricing.

Software development tools will play a critical role as devices become more complex. The challenge is to continue providing tools that are flexible, powerful and easy to use. These tools will also have to conform to various industry standards.

For silicon, look for densities greater than 60,000 usable gates, and speeds approaching 1 ns with increased versatility. Standard LS functions will be incorporated into PLDs. In the mid 1990s, we'll see the integration of processors and PLDs on the same substrate. We'll also see digital signal processors and PLDs combined to offer new capabilities.

For software, we'll see third-party tool vendors and IC manufacturers working closely together. The first step in this direction occurred at this year's DAC where leading vendors and users embraced VHDL as the standard language for programmable logic design. And as programmable logic technology improves, and the market for programmable devices grows, VHDL will become the medium of choice for "programming" logic.

Advances in automatic partitioning, presently available for PLDs, will be extended to include PMDs and FPGAs. Finally, programmable logic synthesis technology will be further integrated into CAE design environments. PLDs have progressed from being considered specialty devices to the threshold of becoming the basic building blocks for digital design. Companies presently using PLDs will increase their usage. Companies who are not currently using PLDs must get on board to stay competitive.

Wayne Gutschick is president of Minc (Colorado Springs, CO).

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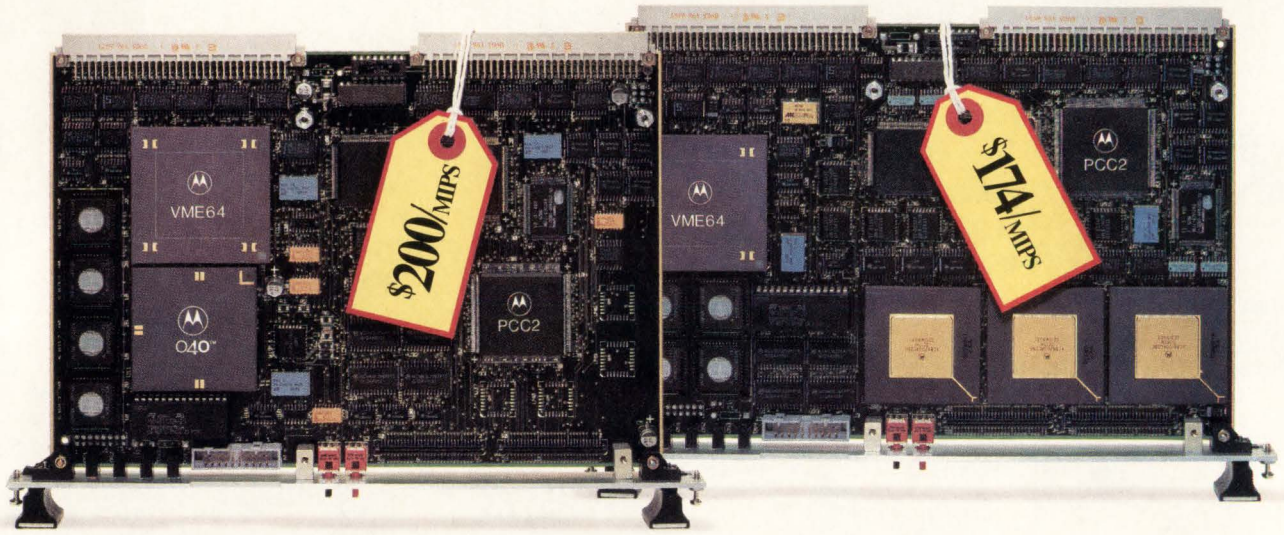

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Putting the magic in multimedia

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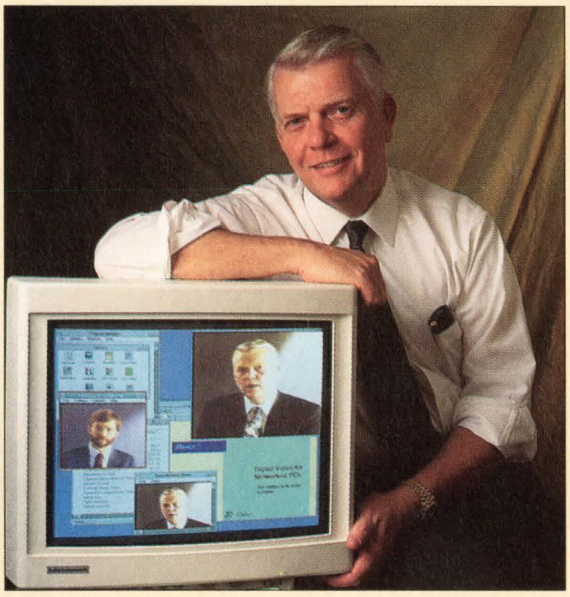
When any technology becomes sufficiently complex, it's tempting to regard it as "magic." When magic is too simple a term, then "multimedia" is often used in its place. Dave Nelson, cofounder of Apollo Computer and now chairman of Fluent Machines (Framingham, MA), doesn't use the word at all. But that's not because his new product doesn't fit the multimedia mold. Indeed, it may fit the mold better than the rest.

Multimedia is an "umbrella" term. Unlike the terms "graphics" or "local area networking," that convey some kind of software and hardware solution to a computer problem, "multimedia" systems embrace many technologies, including video and audio capture, compression, and LAN. Software and/or hardware must be part of a multimedia offering. If one is omitted, then the system isn't complete.

Dave Nelson's Fluent Machines has a complete multimedia solution, even though he will not say so. He's been busy working on it since he founded his new company in 1989. Fluent Machines already has over 35 people working for it, and the company's multimedia architecture solution, called Fluency, recently left the starting gate.



Fluent Machines' Dave Nelson has crafted a multimedia architecture, dubbed Fluency, that will allow both audio and video to be shared among networked machines.

Full-motion video networks

Fluent's focus lets developers integrate full-motion digital video and synchronized audio into computer systems. But Fluent doesn't stop there. What differentiates Fluent from the rest of the pack is an architecture that promises to allow both audio and video data to be served up over a network of machines. That means that Fluency can't stop at just acquiring video and audio data by hooking a microphone and video camera up to a PC. The data must be processed, compressed and the results stored to disk and retrieved. In some applications the data must be transmitted over a network. Fluent plans to let both audio and video be transmitted over a network no matter what the available bandwidth of that network might be. That implies measuring the network's bandwidth and dynamically altering the compression ratio of the data to fit the bandwidth available.

Any multimedia scheme such as this, of course, is quite useless unless software developers can take advantage of the underlying software and/or hardware provided to them. For Nelson that meant Fluent had to provide its own application programming interface (API) that would accommodate developers wishing to integrate video and audio capture, playback and editing into their Windows 3.0 PC-based applications. The API consists of a group of functions that can be used to perform different operations on the data.

Acquiring, displaying, compressing and transmitting audio and video data today means building some hardware. Fluent Machines has already unwrapped an i960CA RISC-based two-board AT-compatible set for capturing, digitizing, compressing, storing, and playing digital audio and video on PC-based machines.

Nelson says, however, that it's the company's multimedia software architecture, rather than the specifics of the hardware itself, that sets it aside from others in the multimedia pack. "Fluent is not a hardware company, even though we have built some hardware," he says. Aside from capturing the video and audio data, the hardware is simply used to accelerate the processing and display process. "There's no reason, that given faster workstations, the whole processing function shouldn't be carried out by the host," Nelson says.

Fluentstreams is key

Fluentstreams is Fluency's software architecture. Nelson's engineering team developed real-time operating system software, data structures and control logic to manage synchronization, scheduling, storage and display of multiple video and audio data streams, in addition to the task of executing algorithms for video and audio compression and decompression. Nelson estimates that Fluentstreams comprises over 20,000 lines of C code. When a PC is configured to run with the AT board set, Fluentstreams software is partitioned between the host and the board set. The board set runs a custom operating system, compression and decompression algorithms as well as analog-to-digital conversion code. The call-based API resides on the host.

At the center of Fluentstreams is a language-based encoding system called Smartstreams. Nelson hopes Smartstreams encoding methodology will become a standard for audio- and video-data representation such as Postscript became the standard for data representation in laser printing.

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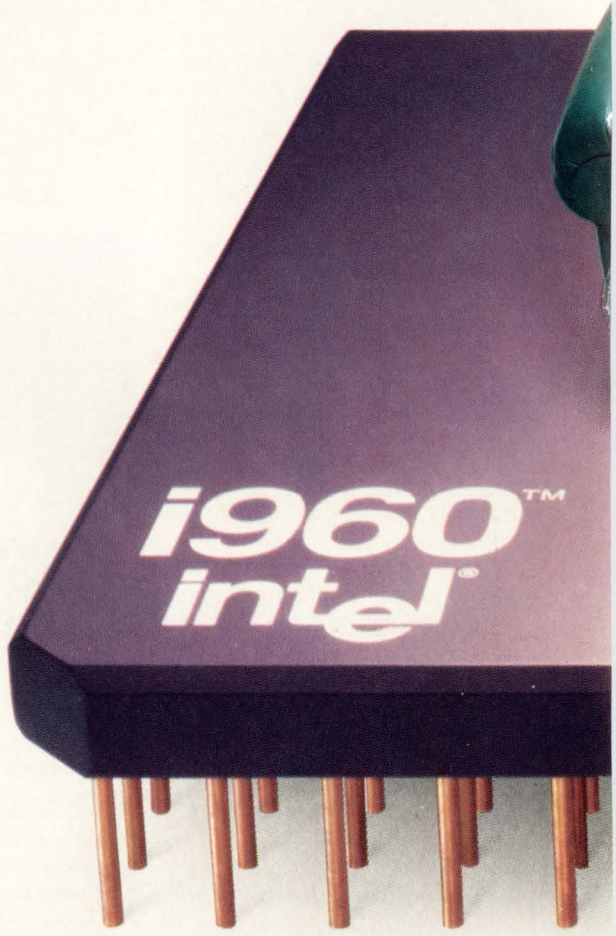

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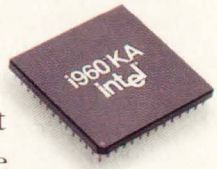

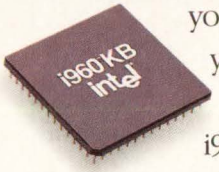

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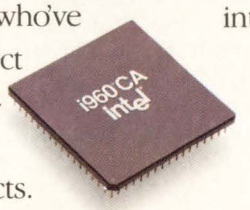

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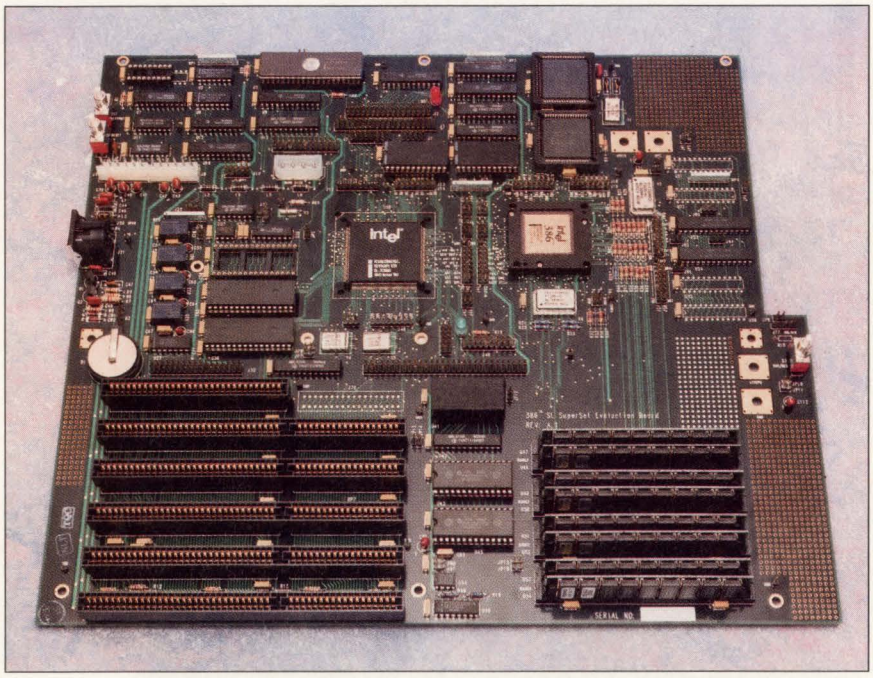
Portable systems get boost from power management



This $4,000 board is the primary component in the Intel 386SL Microprocessor Super-Set Evaluation Kit. With it, designers can experiment with the modes and functions of the 386SL. The board provides a separate connector for the peripheral interface bus, switches for disabling the SRAM cache memory and multiple power-monitoring locations.

Dave Wilson, Senior Editor

Power and battery management are critical in the design of low-power equipment such as laptop computers. Power-management techniques can be applied to all the components in a system—from LCDs and disk drives to active ICs. They can be controlled by methods such as reducing the clock rates on ICs or controlling a power-down mode for peripherals based on the system's need for their services. Battery management, however, is intended to monitor and maximize the power available from a system's batteries, rather than minimize the system's power consumption. Both issues may involve hardware and firmware or BIOS design. But since no "industry standard" methodology exists to perform either function, it's left in the designer's hands.

Battery management is a different beast than power management, according to John Landau, vice-president of marketing at Benchmarq Microelectronics (Carrollton, TX). In his view, rechargeable systems must include three key features. First, the system electronics must let the user accurately know how much energy remains in the system. Second, the system must support fast battery charging. And third, the battery capacity should be kept as high as possible for as long as possible. To support his argument, Benchmarq recently introduced the bq2001 chip specifically for battery management in notebook computers. But the company isn't the only one that has identified the need for battery management, nor does the bq2001 represent the only approach.

BIOS companies like Phoenix Technologies (Norwood, MA) have also recognized the need to solve battery- and power-management issues. Phoenixmiser, Phoenix's software package, for example, controls the power use of the system as a whole by dynamically changing power-consumption modes based on specified system-inactivity times. It also provides power control of individual components through inactivity timers and/or simple enable/disable settings. Phoenixmiser resides in the system ROM in the ROM BIOS address space. Designers can use the power-management software in conjunction with a battery-management software package called Battery Watch. This software estimates power levels in hours and minutes and warns the user when the power is running low. It can also allow NiCADs to be deep discharged, allowing them renew their charge to maximum capacity. Phoenix OEMs the software custom-configured for particular hardware parameters of a manufacturer's system.

Finding the right approach

Designers have several options when it comes to installing low-level power- and battery-management software in their system. It might be installed as a system BIOS routine, as Phoenix has chosen to do. And, in designs based around the Intel two-chip "low-power" 386SL processor, it could be a system management mode software routine. The extended address space of the 386SL processor can be used to ensure that power-management software routines don't conflict with any of other BIOS routines. In fact, one of the biggest challenges facing laptop designers is where to place the power-management software routines to interfere the least with other software. Putting them in at the BIOS level is generally sound, at least for DOS applications, according to Benchmarq's Landau. "But if Unix or OS/2 are used, where the BIOS is bypassed, then battery-management and/or power-management options may be limited," he says.

Three commonly used methods exist for avoiding such conflicts. First, the software can be installed within a keyboard decoder microcontroller, such as an 80C51, which can run double duty as a power-management/battery-management

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microcontroller. Second, a dedicated off-the-shelf device, such as the Benchmarq bq2001 energy-management controller may be used. Third, some newer chip sets, such as Oak Technology (Sunnyvale, CA) three-chip OakNote, offer operating-system-independent power-management schemes implemented by using activity monitors that track system activities such as keyboard activity. Since the monitors operate independently of the BIOS, the chips can enter power saving modes without calling on the system firmware.

Unix needs power management

The 386 and 486 notebooks will be used to run Unix, not just DOS, says Al Safarkis, vice-president of new products at Ogivar Technologies (Quebec, Canada), a designer of laptops and notebooks. In the company's Interport 386SX, 386DX and 486 products, Ogivar makes use of the unused idle cycles of an Intel 8042 keyboard controller to handle power-management and battery-management functions. "When you use 386 and 486 processors, the user wants to run Unix, and you must have hardware power management. You cannot depend on the BIOS or any other firmware that you might have in the system," says Safarkis. "That's why we've used the 8042. It performs screen power down, brings DRAM refresh to a minimum, hard disk power-down and monitors the battery off-line," he adds. In the design of the Dell laptop, Mike O'Dell, vice-president of systems development at Dell Computer (Austin, TX) also chose to use a microcontroller to handle the power functions—in his case the Cops microcontroller from National Semiconductor.

Battery management isn't easy, or that accurate, whatever approach is taken.

Solving battery problems

Battery management isn't easy, or that accurate, whatever approach is taken. David Bell, CEO of Bell Associates, a Los Altos, CA design firm says that you can estimate the charge in lead acid batteries reasonably well by measuring the voltage across the battery. Unfortunately, portables use NiCads. And with a NiCad, the discharge voltage curve over time is reasonably flat. So regardless of its state of charge, a NiCad delivers a very constant voltage. "Its simply impossible to obtain much information by looking at the voltage," he says. "In fact," he con-

tinues, "there's no really reliable method to tell what the state of charge of a NiCad battery is at any given time," he says.

Nevertheless, Bell likes the Benchmarq approach and may use it in future designs. "If you know the battery is fully charged, then you can keep a record of how much charge there is in the battery at any given time by measuring the charge that's being used and any recharging that occurs while the notebook is in use," he says. That information can be stored in nonvolatile RAM in the Benchmarq 2001 chip. "That's really the best mechanism for estimating the charge within a NiCAD," he adds.

The 2001 chip can also be used to calculate self-discharge. "If the battery has not been used, you might estimate that a certain charge has leaked off through self-discharge. Having the date of last discharge is important for estimating the state of charge of the battery," Bell says. But, he adds, there's really no accurate way to measure the self-discharge within a battery cell. "Since leakage occurs within the battery, the best you can do is to estimate what the self-discharge might be based on the characteristics of the battery."

Better batteries on the way

As far as battery technology is concerned, designers are stuck with what vendors have to offer. Today, that means rechargeable NiCad batteries. But newer batteries based on NiMH (nickel-metal-hydride) are on their way from companies like Gates Energy Products (Gainesville, FL). Sporting 30 percent better energy density and a 20 to 40 percent longer life than high-capacity NiCads, they are also better for the environment. Even so, at present, NiMH batteries cannot sustain the high charge rates available with NiCads, according to Gates. And OEMs must pay a premium for them over NiCads. Nevertheless, Ogivar, for one, already offers NiMHs with its machines. But like their NiCad counterparts, they will still need to be managed to get the most out of them. ■

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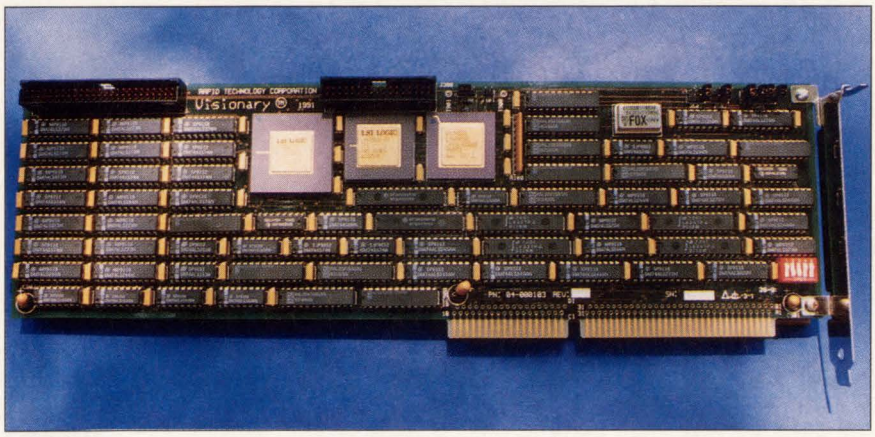
New multimedia chip sets aimed at niche applications



Rapid Technology's "Visionary" PC AT real-time JPEG compression board uses LSI Logic's new JPEG chip set. The board can achieve CCIR-601 resolution at video speeds.

Dave Wilson, Senior Editor

While it may seem obvious that "multimedia" systems must acquire, process, store and retrieve video and audio data, industry standards associated with potential application environments are so diverse that no one "multimedia" chip set stands to win sockets in all applications. Even though JPEG (Joint Photographic Experts Group) and MPEG (Motion Picture Experts Group) are the new multimedia compression/decompression "standards," in some applications, JPEG- or MPEG-compliance is not required. Noncompatible compression schemes, in these cases, may present more cost-effective solutions. Understanding the application requirements is essential for designers of multimedia chip sets. And recent announcements from Philips/Signetics (Sunnyvale, CA), LSI Logic (Milpitas, CA) and Zoran (Santa Clara, CA) testify to the fact that IC houses intend to produce chip sets tailored to the needs of specific slices of the multimedia marketplace.

Designers' approaches

With the introduction of the Philips/Signetics digital video encoder, personal computer designers can now build products that let users output digital video to television monitors or to videotape recorders for storage. LSI Logic's chip set is largely a feature-processing solution, aimed at applications where users need to compress and decompress video data to and from storage-devices in real-time. For its part, Zoran has taken the approach of linking up with Fuji Film to define a compression solution that appears to be cost effective for the designer of digital still-photography equipment.

The new Signetics chip fits with the companies Diva (Digital Video Architecture) and complements two other devices in the Diva family—the SAA7191 video decoder and the SAA7192 color space converter. The SAA7191 accepts digitized composite video and converts the signal into brightness, color and timing data. The SAA7192 converts the SAA7191 output into primary RGB video.

So far, those devices have seen a number of design wins. RasterOps (Santa Clara, CA), a manufacturer of graphics display controller boards for the Apple NuBus, has used the decoder/conversion chips in the design of its 24XLTV board, which provides 24-bit graphics capabilities, real-time digital video in a window and built-in QuickDraw acceleration.

The digital video encoder

Introduced at Siggraph in July, the new Signetics SAA7199 digital video encoder accepts seven different digital formats, including CCIR601 and VGA. The encoder can generate analog output signals in NTSC or PAL formats. Furthermore, it can operate in three user-selectable modes. In the master mode, the SAA7199 accepts timing from the graphics system. In the stand-alone mode, it generates graphics-timing signals based on a video clock. In genlock mode, the device locks to an analog video signal and generates all graphics-timing signals. Genlock mode allows graphics to be overlaid on any video source.

Signetics has no feature-processing devices at present. As a result, the designer must choose another device, such as a RISC processor or dedicated custom device, to run feature-processing algorithms. While many systems based on the Signetics devices have already hit the market, they are only the tip of the iceberg. More advanced products that use JPEG and MPEG standards are currently underway. Many of these products may still use the Signetics chips as the front-end for systems that send and receive video data to and from storage and networks.

The color space converter

Like the Signetics SAA7192, the LSI Logic L64765 is also a color space converter. The device is an addition to LSI Logic's image-compression chip set that includes the L64735 discrete cosine transform processor and the L64745 JPEG processor. Developed in conjunction with Rapid Technology (Amherst, NY) the LSI Logic device not only converts between RGB and YUV color spaces, it provides the control logic to convert pixel data in either direction, between a raster-ordered signal and a JPEG block-ordered signal. Rapid Technology's PC-based image compression board, dubbed Visionary, is the first commercial implementation of the device. The board can be used to continuously read or write video to a disk. The board uses a JPEG compression scheme, and achieves CCIR-601 resolution at full-motion speeds of 30 frames/s, according to Steve Levine, Rapid Technology's president.

Working with Fuji Photo Film (Tokyo, Japan), Zoran has developed a two-chip set that has already been used by Fuji in several products,

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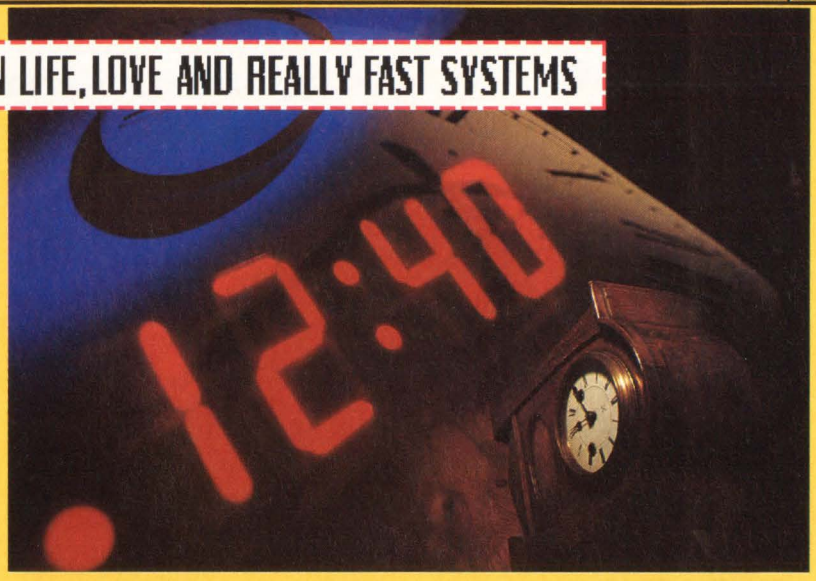

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Editorial contributions: Tim Wilhelm, Luis Pineda, Ali Mesri and Cynthia Jones.

MAKE 1600 X 1280 YOUR NEW YEAR'S RESOLUTION

The continued evolution of workstation monitor resolution is about to write a new chapter. The evidence: 1600 x 1280 displays have dropped into the $4,000 range, just the price point that made today's widely popular 1280 x 1024 monitors "acceptable" several years ago.

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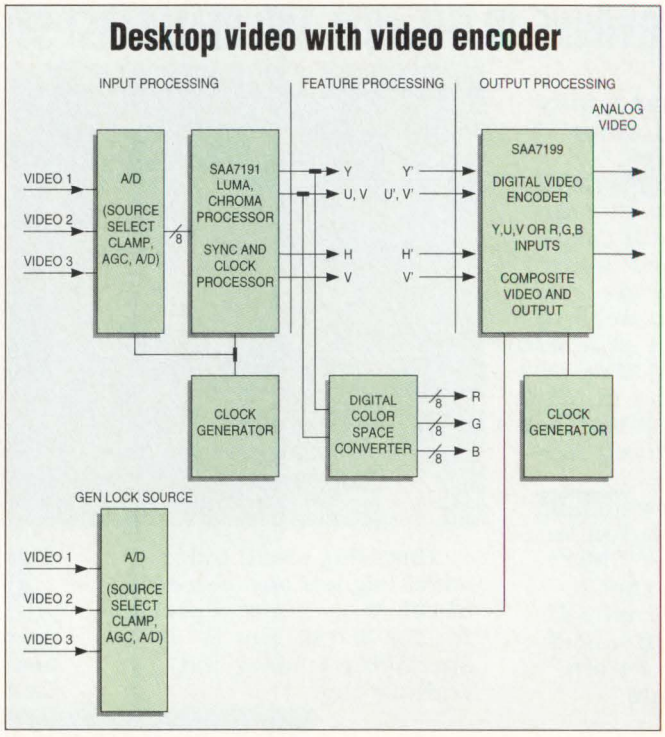

Philips/Signetics SAA7199 digital video encoder lets computer graphics and digital video be displayed on television monitors or stored on videotape. It joins a multimedia lineup that already includes digital converters, video processors and clock generators.

including digital still-video cameras, memory card players, and video graphics printers. The two-chip set comprises the ZR36020 discrete cosine transform processor and the ZR3603X quantization and coding chip. Together they implement a JPEG-compliant image-compression system for the compression of a continuous-tone color image. The processor combination goes beyond the JPEG specification because the device can perform on-the-fly, real-time statistical spectrum analysis of a still video image, according to Zoran's president Levy Gerzberg. The spectral analysis is used to dynamically determine a compression ratio that can be applied to the data, while retaining the required quality. Naturally, in applications such as still-digital cameras that may use 8-Mbit memory cards to hold data, the compression ratio applied to the image data has a direct relation to the number of pictures that can be stored on the card itself. Zoran plans to develop a family of devices based on JPEG-compatible technology. These will include JPEG-compatible and extended JPEG-compatible (JPEG-Plus) in addition to non-JPEG-compatible devices differentiated by price. ■

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INTEGRATED CIRCUITS

Hippi vendors hop on serial bandwagon

Dave Wilson, Senior Editor

Vendors dissatisfied with the price, performance or capabilities of their network standards have taken the LAN into their own hands. The result is that more cost-effective, high-speed networks will soon be sprouting from new computers. The Hippi (High Performance Parallel Interface) Serial Implementors Group, which began work in October 1990, completed its serial version of the Hippi ANSI specification in April 1991. Now that the specification is finished, vendors will be racing to bring products to market.

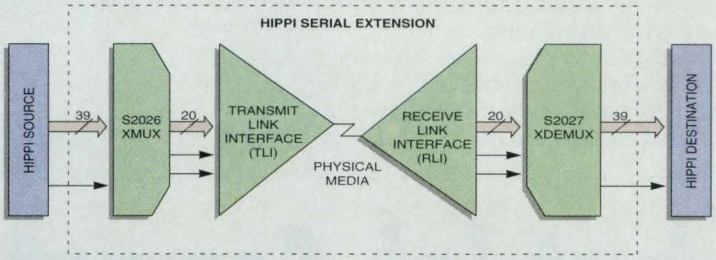
Hippi-Serial, as it's called, was defined by a group of over 40 companies. It specifies a 1.2-GHz data communications interface that will make it more cost-effective for designers to connect the Hippi interface to workstations and supercomputer systems. The Hippi-Serial specification agreed upon by the group overcomes previous limitations associated with cable-based Hippi hardware. It describes not only the physical fiber, laser and electrical requirements, but also the encoding scheme to be used.

The specification is an extension to the current proposed Hippi ANSI standard that defines a point-to-point communications link over 32- or 64-twisted-pair data lines. Operating at a 25-MHz signaling rate, the parallel Hippi data rates of 800 or 1,600 Mbits/s are supported. Hippi specifies channel electrical requirements, packet protocols and a 100-pin connector. Furthermore, it's limited to a rather short 25-m copper cable.

The motivation behind serial Hippi was to enable computers to be connected at distances up to 10 km with a lightweight cable, such as fiber, according to Marc Friedmann, vice-chairman of the Hippi-Serial Group. Although Hippi-Serial was intended for fiberoptic interconnects, coax can be used for distances up to 100 m.

Unlike the parallel Hippi standard, the serial interface has nothing to do with ANSI standards efforts. Rather, it's an "agreement among vendors" to ensure the interoperability of equipment from different manufacturers, according to Digital Equipment Corp's Marty Halvorson, chairman of the Hippi-Serial Group. The Serial Specification involves the multiplexing and encoding of the Hippi parallel data and control signals into a high-speed serialization device on the transmiter side. On the receiver side, the reverse process of decoding and demultiplexing occurs.

Parallel-to-serial interface



In the serial Hippi specification, data is multiplexed and transmitted down a fiber-optic cable at over 1 Gbits/s. Interface silicon from Applied MicroCircuits (shown here) and Hewlett-Packard may soon make Hippi-Serial a cost-effective means for high-end workstations to communicate.

Hippi as a network?

Despite the fact that Hippi was originally intended as a point-to-point interconnect on large computers, certain vendors are trying to make it into more of a network. Network Solutions (Minneapolis, MN), for example, manufactures a range of Hippi crosspoint switches that have been installed at several supercomputer sites. The company signed an agreement, last year, with Sun Microsystems to develop an interface for Sun's workstations to let them work with Network Systems' Hippi switches in supercomputing networks. In certain respects, then, serial Hippi is in competition with another ANSI network standard still under development—Fiberchannel. Another Gbit/s interface, Fiberchannel is intended to be more of a full networking approach, like FDDI (Fiber Distributed Data Interface), rather than just a channel or a point-to-point solution. There are some who feel that Fiberchannel will offer a complementary, compatible networking environment to Hippi. But Jim Toy, president of Broadband Communications Products (Melbourne, FL) is not one of them. "The Fiberchannel format is completely incompatible with the Hippi format," says Toy. "To couple a Hippi port to a Fiberchannel channel, you have to store the data, deformat the data, then reformat the data for Fiberchannel before sending it down the link. A lot of people who are implementing Hippi today just need a simple extension box that does nothing more than parallel-to-serial data conversion and vice versa. They don't want to go to the expense of reformatting and storing the data."

In the new Hippi serial specification, a coding scheme from Hewlett-Packard, dubbed 21b/24b, was chosen over an encoding scheme called 8B/10B+ forward error correction, developed by DEC. "There was a lot of debate over the two approaches," Friedmann explains. "In the end, there was only a one vote difference, so it was very close." While Friedmann thinks that both encoding schemes are excellent, he says that the DEC approach requires an extra 300 MHz of bandwidth to perform the forward error correction. "Some people thought that might be more expensive, although the forward error correction should enable a lower bit-error rate for the Digital approach," he adds.

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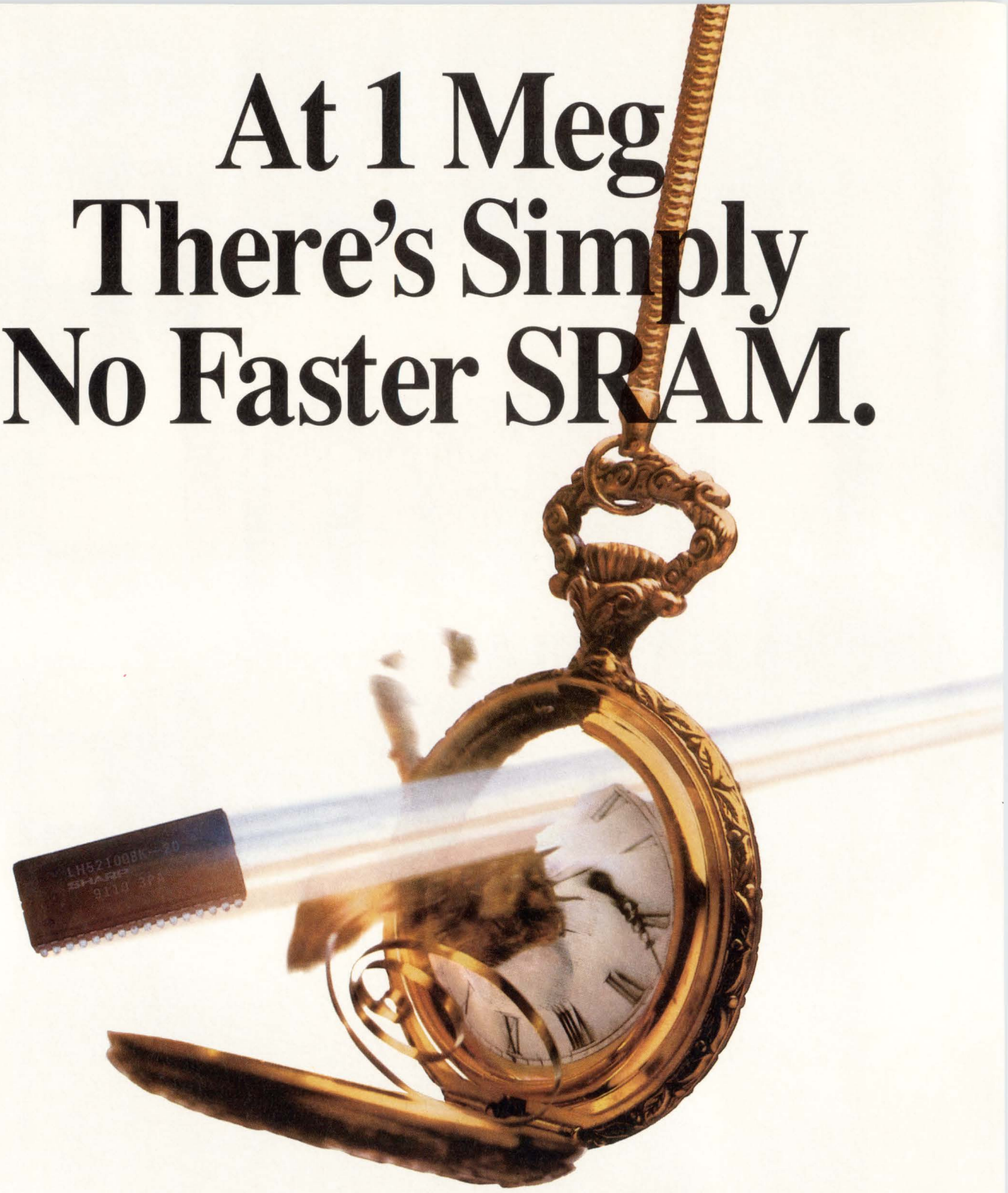

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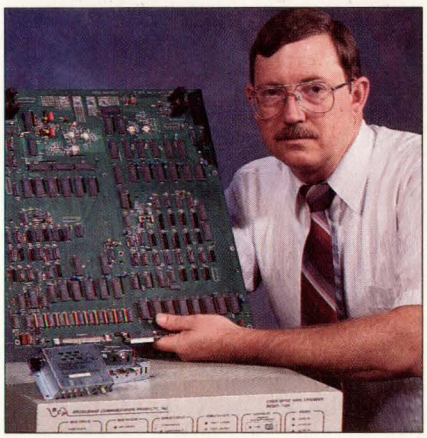
CIRCLE NO. 30

INTEGRATED CIRCUITS

Hewlett-Packard (Palo Alto, CA) stated that it will develop a bipolar transmit and receive chip set to implement the Gbits/s Hippi links. But the chip set isn't scheduled for delivery until 1992. It will perform serialization and deserialization using the HP 21b/24b encoding scheme. According to HP, the transmitter IC will include data encoding and multiplexing as well as a phase-locked loop (PPL) for user data retiming and clock synchronization. The receiver IC will also include



Jim Toy, president of Broadband Communications Products, shows the Model 1200 Hippi extender product with the multiplexer/demultiplexer PCB and fiberoptic modules.

clock extraction, demultiplexing and decoding, as well as state machine functions to handle link start up, idle and maintenance.

Support for Hippi-Serial

Aside from HP, Hippi-Serial chips from other vendors will hit the streets soon too. Applied MicroCircuits (San Diego, CA), a vendor that presently offers a chip set that implements parallel Hippi, has announced its intention to support the new serial specification as a complement to its existing Hippi chip set. Its S2026 and S2027 devices are currently in development. ECL compatible, and built in BiCMOS technology, they're designed to encode the Hippi control signals, sequence the bit stream and multiplex/demultiplex the datapath from 16 to 32 bits. Further support for Hippi-Serial comes from BT & D (Wilmington, DE) in the shape of fiber optic transmitters and receivers.

Broadband Communications Products announced a fiberoptic Hippi serializer in March. Its model 1200 allows the systems integrator to extend a full duplex Hippi channel to lengths up to 10 km. "The extension process includes the parallel to serial extension process plus the electrical to optical conversion and vice versa on the other end," says BCP's Toy. But because no Hippi interface devices were available at the time the product was designed, the company designed its own custom ECL device. And since the design was completed before the HP encoding scheme was chosen, BCP doesn't use the 21b/24b encoding scheme. Instead, a proprietary encoding approach was chosen that uses a scrambler/descrambler technique. But the company does intend to incorporate the HP encoder/decoder into its next-generation products next year, adds Toy.

However effective the Gbits/s Hippi-Serial might prove to be, it's still not cheap. Two Broadband links, for example, cost well over $25,000. It's likely, therefore, that Hippi-Serial will stay in the Cray/IBM world for some time—at least until the silicon vendors can introduce more cost-effective interface solutions. In the high-end environment, however, applications such as real-time visualization should benefit from the time and effort invested by the Hippi-Serial group. ■

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CAE/CAD TOOLS

CrossCheck testability solution extended with interface to ATE

Barbara Tuck, Senior Editor

Anticipating how much impact any new technology will have on the industry is always difficult, especially if that technology is high-priced and perceived by the user as risky. But a major technological development that promises a front-to-back-end solution to the problem of testability for high-density ASICs is worthy of careful scrutiny. Later this month, CrossCheck Technology (San Jose, CA) will fill in the missing piece of its hardware/software testability solution with the introduction of its workstation-based CX-Probe diagnostic software that automatically isolates and identifies functional failures in ASIC devices. By linking Unix-based workstations to automatic test equipment, CX-Probe completes the loop of CrossCheck's testability solution and reduces the debug cycle from weeks to days or hours, according to CrossCheck. Until now, the CrossCheck solution has consisted of a test-point matrix on the base wafer that functions as an on-chip grid of sense probes, and the CX-Test fault simulation and automatic test program generation (ATPG) software (see "High-density ASICs force focus on testability," *Computer Design*, April 1, p 59).

Convincing customers isn't easy

Because it demands a total commitment from ASIC vendors, the CrossCheck testability solution has been hard to sell from the beginning. Though device performance doesn't suffer with the CrossCheck approach, device density can drop by as much as 25 percent and device price can increase by 25 to 50 percent. Despite costs, the licensee list has consistently grown. Currently, it includes Fujitsu, Harris Semiconductor, LSI Logic, Oki, Raytheon, and Sony. Within the last six months, both LSI Logic and Oki have introduced silicon that incorporates CrossCheck technology.

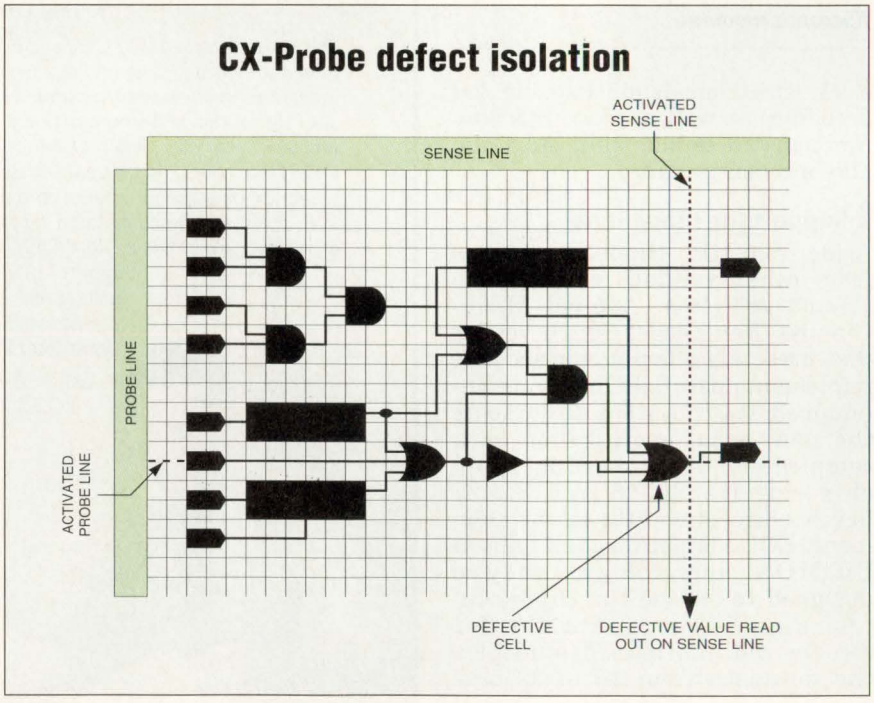
LSI Logic (Milpitas, CA), the first of CrossCheck's ASIC partners to make silicon samples available for customers, is discovering that users are somewhat slow to be convinced of the potential of CrossCheck-based silicon. LSI Logic hopes the availability of the CX-Probe failure-analysis software will make a more convincing argument for its CrossCheck-based LFT150K gate arrays (see "CrossCheck testability reaches commercial gate array family," *Computer Design*, March 1, p 48).

The workstation-based CX-Probe software uses the outcome of ATE to diagnose functional failures in ASIC devices incorporating the CrossCheck test structures. The combination of the workstation CX-Probe and the ATE constitute an automatic logic analyzer. When the large number of embedded sense probes on CrossCheck-based silicon are attached to that logic analyzer, an automatic chip-level analysis tool with massive cell-level observability results. CX-Probe isolates and identifies functional failures caused by: manufacturing defects such as open and shorted FETs; metal bridges and opens, and conventional stuck-at V_{ss} and V_{dd} faults; CAD errors such as mask faults; and design errors in macrocell libraries.

CX-Probe, which has no inherent limitation on the size of the device it analyzes, requires a Sun 4, Sparcstation 1 or Sparcstation 2. Memory use depends on the number of simulation and test vectors, which vary with design complexity. The software operates with almost any modern ATE, according to CrossCheck, via a suitable file interface. CrossCheck provides datalog translators for Advantest 3320, Ando 8034 and 9035, Schlumberger Sentry 50, and Credence ASIX-2 and advises that the ATE and workstation are connected by Ethernet to speed data transfer. CX-Probe accepts netlists and functional patterns in either Verilog or LSI Logic's Lsim format.

Few early customers expected

It's expected that customers for CX-Probe will initially be limited to CrossCheck's ASIC partners who will use the diagnostic software to debug prototypes, analyze production test yields, debug macrocell libraries; and for quality and



For ASICs with CrossCheck on-chip test structures, the new CX-Probe diagnostics software isolates a defect by determining the probe- and sense-line coordinates of the test point nearest the defect.

CAE/CAD TOOLS

reliability assurance analysis of life-test, burn-in, and field failures. The long-term benefit of CX-Probe, though, lies in its being a tool that customers will be able to buy to look at system problems themselves, according to Bill Alexander, LSI Logic's product marketing manager for advanced products and test services. "Production test is clearly our problem but once we've shipped prototypes, it's questionable whether a field failure is an LSI Logic or a customer's problem," says Alexander. If customers have CX-Probe, Alexander suggests, they can debug field failures themselves and thus manage their complex designs at a system level.

LSI Logic's sample base for CrossCheck-based silicon is relatively small, and every device that has reached test so far has passed, Alexander says. But without CX-Probe, if failures were to occur, options for diagnosis and debug would be the same as for any other ASIC. Engineers would have to go back to the simulation environment to generate debug programs for getting down to a specific gate or transistor, and/or use e-beam investigation. "With CX-Probe, debugging can be done at the tester, with no recompilation of test vectors," says Alexander. LSI Logic doesn't have CX-Probe in-house yet, but Alexander thinks it will be a tremendous advantage for the engineer to have the ability to electronically probe to the transistor level to reach the actual point of failure. "Between oxides and so much metal, defects can be well hidden in complex ASICs," he says.

Where e-beam and/or electro-mechanical investigation is desired, CX-Probe can function as a front-end tool, supplying data to speed the investigation, according to CrossCheck. The nondestructive nature of CX-Probe's failure analysis is clearly a benefit over e-beam investigation that destroys the package, says George Bouhasin, manager of Fujitsu's technical resource center (Gresham, OR). Like LSI Logic, Fujitsu doesn't have CX-Probe in hand yet. But Fujitsu hopes, according to Bouhasin, CX-Probe will let engineers gather data for yield improvement on the actual silicon rather than on special test vehicles. "We're not sure what the reality is," he admits, "and we're concerned about the turnaround time of gathering a reasonable number of data points to improve yield."

He refers to CrossCheck technology as a "canned solution that's easy to grab onto." The new interface to ATE is something that Fujitsu really needs because the natural commingling between designers and test engineers that might result in an internally developed design-for-testability solution doesn't take place at Fujitsu, Bouhasin says. "CrossCheck's link of Unix-based workstations and up-front design for testability strategy with ATE is unique," he says.

A long road to credibility

Because neither LSI Logic nor Fujitsu have actually used CX-Probe yet, its promise hasn't been validated as of presstime. Benchmark data will soon be available from Raytheon which has been beta-testing CX-Probe for CrossCheck. And, of course, CX-Probe will hardly be able to make a significant impact on the industry before CrossCheck silicon's business picks up. It's expected, though, that as other CrossCheck licensees join LSI Logic and Oki and make silicon available, the technology will gain credibility. LSI Logic's Alexander says that LSI Logic, the sole vendor of CrossCheck silicon until recently, has been battling customers' concerns of being tied exclusively to LSI Logic. "Having competitors will help," says Alexander. And as reliability becomes more difficult to maintain at higher complexities, it's likely that CrossCheck technology will appeal to more than workstation and computer makers and telecom companies.

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COMPUTERS AND SUBSYSTEMS

Serial bus looks to standardize connections for peripherals

Warren Andrews, Senior Editor

In an effort to bring some order to the interconnection of a broad range of accessory devices such as keyboards, locators, bar-code readers and others, Digital Equipment Corp (Maynard, MA) has introduced a new serial connection scheme. In developing the approach, dubbed Access.bus, DEC joined forces with a team from Philips/Signetics (Sunnyvale, CA) using that company's previously developed I^2C (inter-integrated circuit) technology. The companies have specified both the physical definition and protocols and are offering them to the public domain with no strings attached.

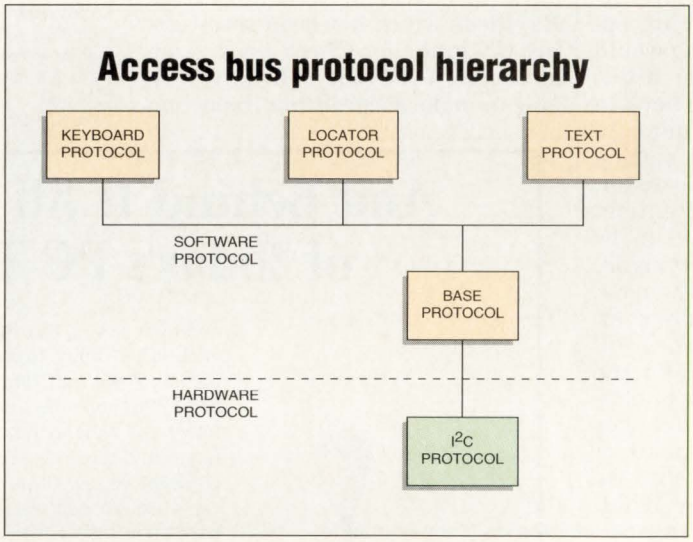
The Access.bus

As implemented by DEC, Access.bus is designed to handle relatively slow input devices such as keyboards, mice, bar-code readers, magnetic card readers, modems and some signal transducers for real-time control applications. It's intended to handle up to 14 different devices on a single serial cable which can be as long as 8 m. The bus uses the basic I^2C configuration and can handle data rates up to 80 kbits/s (100 kbits/s minus overhead). In addition, the Access.bus cable also carries a +12-V supply voltage for powering each device. According to the specification, the cable carries up to 500 mA.

According to DEC's Paul Nelson, senior engineering manager of input devices, video, image and printer systems group, adding an Access.bus interface to any peripheral device requires only an 8051-family microcontroller with I^2C circuitry. "The use of this circuitry should add a maximum of about $.50/accessory device in OEM quantities," he says. Alternately, he adds, discrete I^2C circuitry can be used to implement the interface, but there's little—if any—advantage. Nelson also hinted that sometime in the future, the basic I^2C maximum clock rate might be updated so faster devices such as scanners and/or video and imaging functions could be attached to the bus.

Devices sharing Access.bus are attached with a four-conductor shielded cable connected with a DEC-developed connector (available from both AMP and Molex). The shielding is required to keep the system within FCC radiation requirements. The connector is similar to the standard RJ22 telephone connector only it's slightly larger to accommodate shielding. The four conductors include the 12-V supply line, a line for data (called SDA for serial data), a line for the clock (labeled SCL for serial clock) and ground. Typical Access.bus devices will have two connectors to allow chaining of devices. "T" connectors, however, may be used with smaller, hand-held devices.

The Access.bus protocol comprises three levels: the I^2C protocol, the base protocol and the application protocol. The basic discipline of Access.bus is defined as a subset of the Philips I^2C. This is a symmetric, multi-master bus which allows for arbitration among contending masters without loosing data. It also provides for cooperative synchronization of the serial clock for exchange of data between bus partners with different maximum clock rates. The scheme allows addressing, framing of data bits and bytes, and byte acknowledgement by the receiver.



Access.bus begins with basic I^2C protocols and adds a baselevel common to all devices and other device-specific protocols, which all operate over the same bus.

Base protocols

The base protocol is common to all types of Access.bus devices and establishes the bus characteristics. The host plays a role as manager of the bus specifying communication between the host and peripheral devices—never between two peripherals. While the I^2C protocol allows either a sender or receiver to be the master in a bus transaction, the Access.bus protocol restricts masters to sending and slaves to receiving. The host and all attached devices are, by definition, both master and slave devices and will act as either at the proper time.

The base protocol defines the format of the Access.bus message envelope which is made up of an I^2C bus transaction with additional information appended. One item of appended information is a checksum for reliability control. The Access.bus base protocol also specifies a set of seven control and status message types which are used in the system configuration.

The configuration process is designed to permit auto addressing and hot-plugging. Auto addressing refers to the way that devices are assigned unique bus addresses in the configuration process without the need for setting jumpers or switches on the devices. Hot plugging lets users disconnect and reconnect devices to the system while it's running without having to reboot the host.

The top level of the Access.bus protocol defines message semantics that are specific to particular

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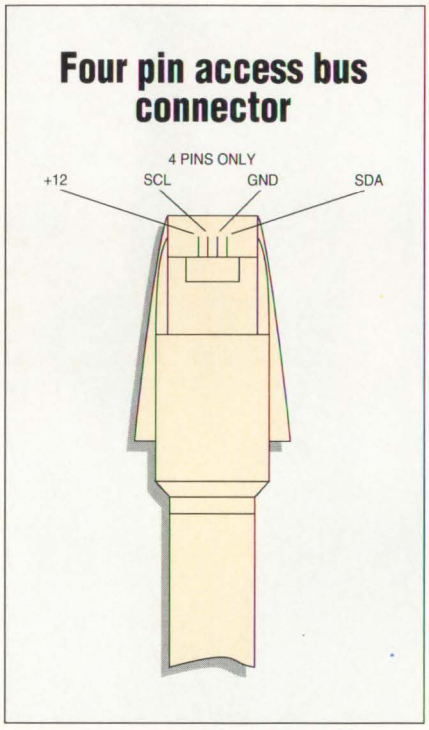
COMPUTERS AND SUBSYSTEMS

functional types of devices. Different device types have thus far been divided into three classes: keyboards, locators and general text devices. Each class is relatively broadly defined, leaving room for a variety of different devices. The definition for keyboards, for example, allows for the monitoring of a device with up to 255 keys. Locator devices can include not only mice, tablets and trackballs, but also valuator sets (such as dial boxes) with up to 15 valuators and function button boxes with up to 16 buttons. Text devices are defined to include devices providing character streams such as card readers, printers, barcode readers or modems.

In developing the three basic application protocols DEC has attempted to define most of the standard applications. "But there's no restriction on the development of other application protocols as the needs occur. In fact, I anticipate that many additional application protocols will start appearing as Access.bus comes into broader use," says Nelson.

DEC plans to form an Access.bus committee which will help define other standard device-specific application protocols. In addition, any device vendor is free to define its own special device protocol within the general message envelope defined by the base protocol.

At the electrical level, Access.bus functions as Philips initially defined its I^2C setup. The host and devices are connected to both the data and clock lines in a "wired-AND" logical configuration. The wired-AND is implemented by connecting the data and clock output stages of each bus



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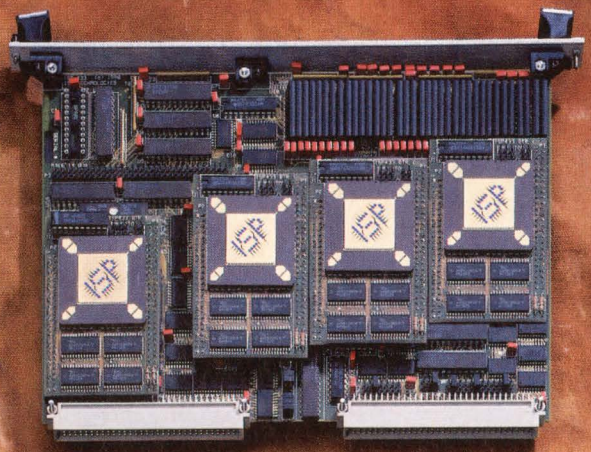

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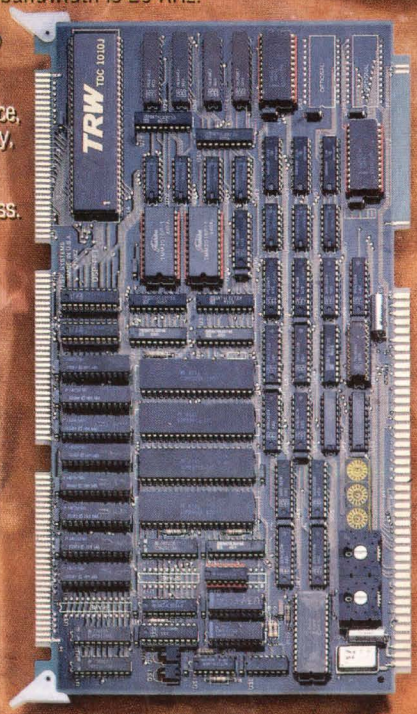

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node to the lines through open-collector or open-drain transistors. These devices are included on existing I^2C components. The wired-AND configuration allows any of the bus nodes to force either line low. When there's no output from any bus node, the lines are held high with pull-up current sources in the host. All devices sense the level on both the clock and data lines.

When two devices on the bus simultaneously attempt to assert mastership, the logical wired-AND circuitry takes over. While putting data on the data line, each master independently is sensing the state of that line. Whenever a contending master detects that the state of the data line is different from the data value it's putting out during a clock-high, the contending master backs off and waits for a stop condition before trying again. Thus, two contending masters will both put data on the bus only for as long as they are putting the same data on the data line. The first bit where they differ will cause the contender that put out a "1" (level-high) to back off. For example, two masters trying to send to different bus addresses will resolve the contention by the end of the first byte of the bus transaction. Since the second byte is the address of the master, if both masters are attempting to send to the same address, the contention will be resolved by the end of the second byte.

Industry standard

Both DEC and Philips/Signetics plan to support the Access.bus link as an industry standard. Through its TRI/ADD program, DEC will offer hardware, software and marketing support to peripheral makers using the bus. Philips/Signetics will offer technical support and a range of components for peripheral designers. Each company will also provide development kits. DEC also plans to sponsor an Access.bus consortium to validate the bus as an industry standard. In this direction, the ACE (Advanced Computing Environment), a consortium of 42 major computer makers, has designated Access.bus as an option in the Advanced RISC Computer (ARC) specification. ■

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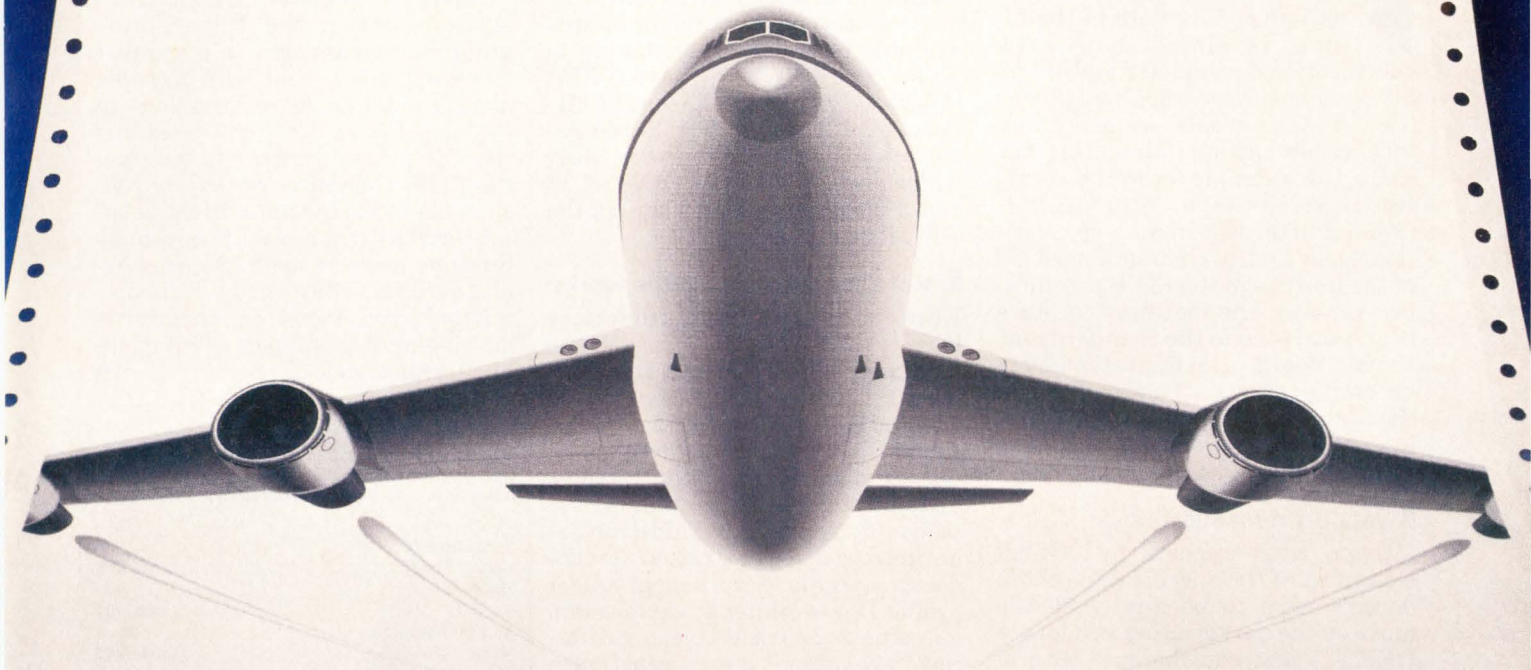

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COMPUTERS AND SUBSYSTEMS

IEEE sanction expected for Futurebus+ by year's end

Warren Andrews, Senior Editor

Futurebus+, the bus many said will always remain in the future, is almost here. The specification is completed and orders for products have reportedly been booked. After what's seemed an interminable battle of dissenting factions, the logical layer (P896.1) and the physical layer and profiles (P896.2) of the Futurebus+ specification have finally cleared almost all of the hurdles in the IEEE specification process. The specifications have been presented to the Standards Activities Board—the final step before becoming official. Following that, there's only a final review and printing—expected to be completed before year's end.

Vendors remain cautious

Despite what appears to be final clearance of the specification, there doesn't seem to be any wholesale move on the part of either vendors or OEMs to jump on the bus. Most of the early product bookings—with the exception of the 300 system orders reported from a French telecommunications company—appear to be for prototype quantities.

In the United States, most VME vendors are keeping a close eye on Futurebus+, but have not made any large commitment. One exception has been Force Computers (Campbell, CA), which made a major commitment to Futurebus+ early on and is involved in the U.S. Navy proof-of-concept Futurebus project as a subcontractor to Litton. Force has also worked with Texas Instruments (Dallas, TX) to develop a new controller chip for next-generation Futurebus+ projects.

"The availability of faster performance on VME through the SSBLT (source synchronous block transfers) is likely to delay some immediate need for Futurebus+," says Abe Hirsch, marketing director for Heurikon (Madison, WI). If SSBLT on VMEbus becomes a reality, it will provide performance that will match—and exceed—32-bit Futurebus+ in its present incarnation. "Implemented as a 32-bit bus, current prototype Futurebus boards are able to transfer at rates up to about 120 Mbyte/s," says VFEA (VME-to-Futurebus Extended Architecture) International Trade Association's technical director Ray Alderman. SSBLT is expected to boost VMEbus to somewhere in the 160-Mbyte/s area.

More specifications in the works

Even though the first hurdles have been cleared, the Futurebus+ group continues to forge ahead. In recent months, the working group was granted status as a subcommittee by the IEEE. The subcommittee immediately formed new working groups, including those for a military and telecom profile. In addition, it authorized three new projects for the desktop profile: a working group for profile D, a working group to establish a new electrical layer specification (low-voltage, low-current) and a working group for a mezzanine-type board mechanical specification (FSCEM) for the desktop profile that can be used for all Futurebus+ profiles.

The fledgling sponsor group also approved a project aimed at standardizing Open Boot, an autoconfiguration and autobooting firmware interface standard between the hardware and operating system. Open Boot, developed by Sun Microsystems (Mountain View, CA), uses Forth for its commands. The Futurebus+ group hopes to be able to adapt the Sun Microsystems' approach to Futurebus+ as well as to promote it as a common formula for system configuration.

In addition, the committee established a study group to work on formally standardizing the SBus mezzanine-bus specification. Initially developed by Sun Microsystems, SBus has been released to the public domain and, until recently was governed by a committee known as SBusSpecCom (SBus Specification Committee). With the formation of an IEEE-sanctioned group (under the umbrella of the Futurebus+ Standards Committee), members of SBusSpecCom have agreed to relinquish control of the bus to the IEEE group. Force Computer's strategic marketing director, Wayne Fischer, has been named as chairman of the group.

Since its formation as an IEEE subcommittee, the Futurebus+ group has meandered in a number of varied areas, and will probably branch out into more directions in the near future. This has prompted the committee leaders to petition the IEEE Computer Society to consider changing the name of the sponsor activity from the Futurebus+ Subcommittee to the "Open Bus Architectures Standards Subcommittee" and focus on standards development in support of all open-bus technologies. ■

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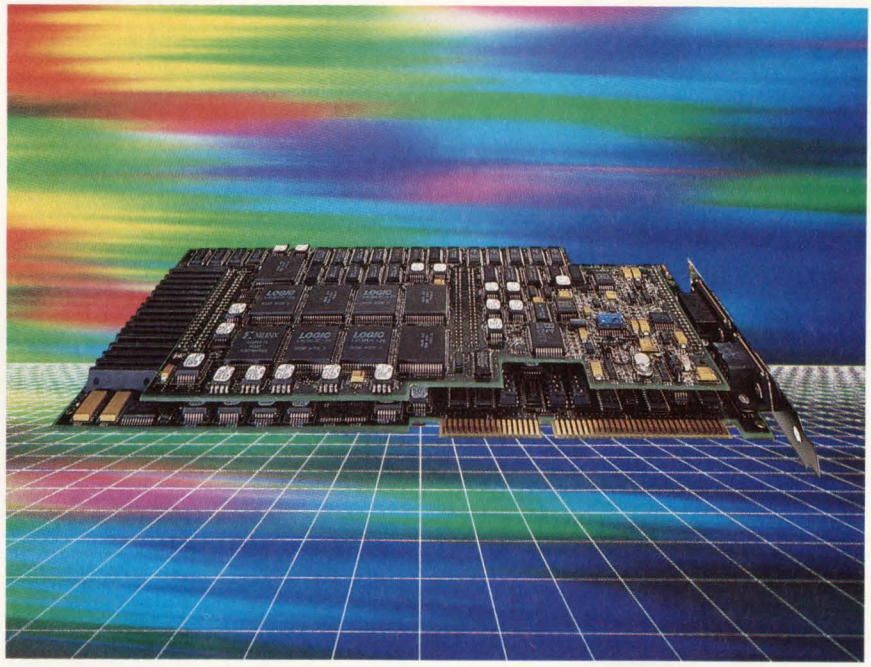

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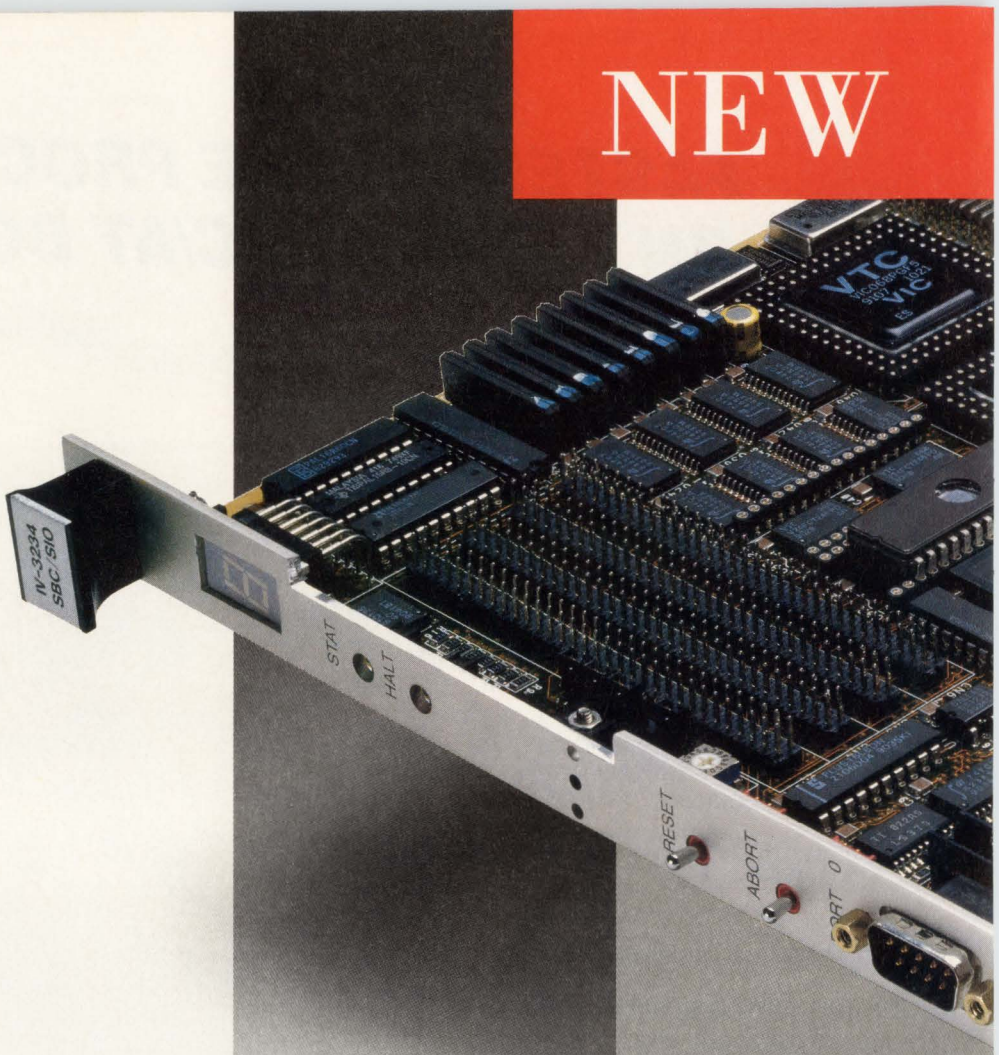

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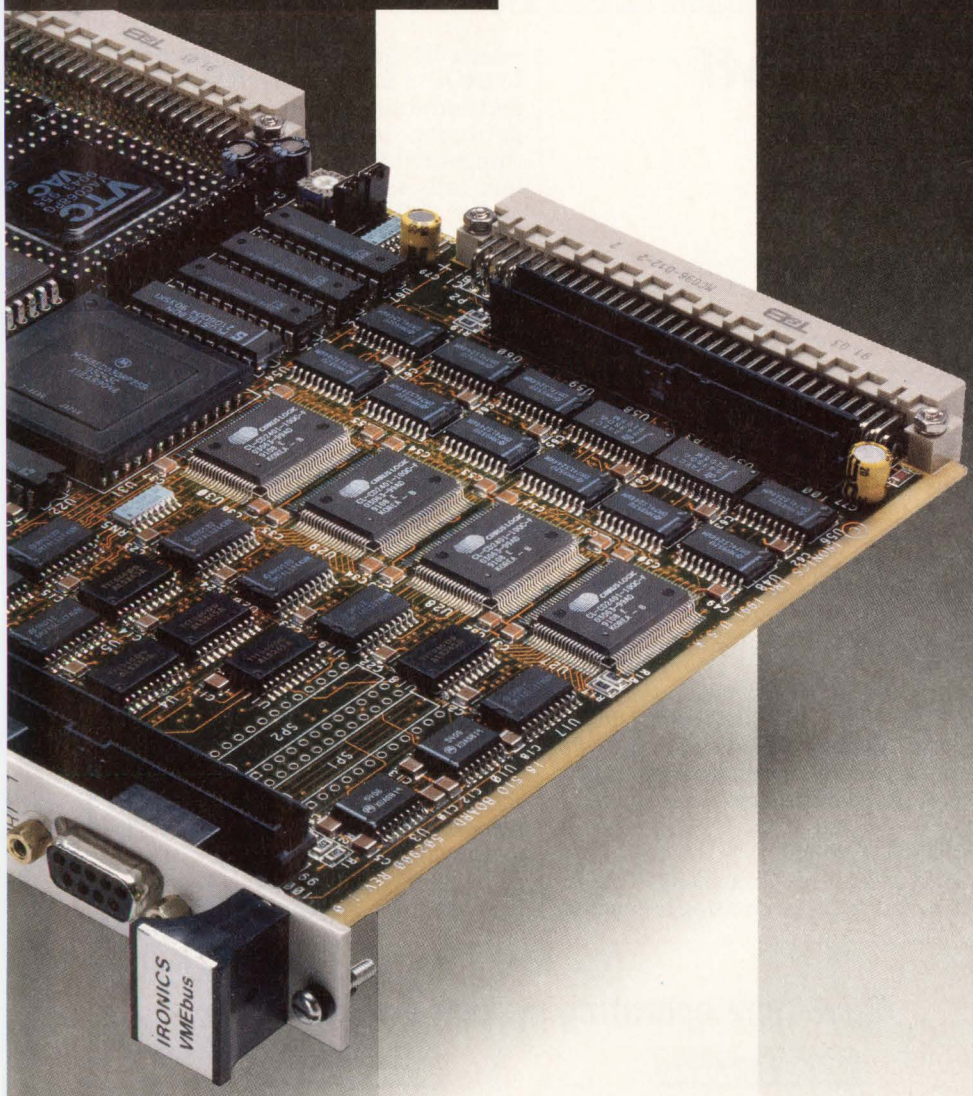

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CIRCLE NO. 40

SOFTWARE AND DEVELOPMENT TOOLS

Competitors' claims kickoff real-time Unix squabble

Tom Williams, Senior Editor

The technical challenges of selecting a real-time version of Unix for a specific application should be more than enough to keep designers on their toes. But with all the claims and counter-claims being made by vendors, designers must be doubly careful in evaluating competing products. The key is to keep the true requirements of the design foremost in the evaluation criteria.

True Unix flows from only one source—AT&T. Of course, there's also the Berkeley version of Unix used by many vendors. Berkeley, or BSD, Unix also originated with AT&T, but is no longer compatible with AT&T's version. This incompatibility confuses many users as to what constitutes true Unix.

While determining what is a true Unix is difficult, determining what is a true Unix for real-time applications is even more so. The first point to remember is that Unix is not a real-time operating system. To make Unix behave like one, companies have made changes in two ways. The first way is to license Unix from AT&T and then modify the kernel to make it preemptable and deterministic. The second approach has been the "clean room" method that builds a Unix-compatible operating system with real-time behavior without looking at the AT&T source code. To claim compatibility, such a system would have to exhibit binary and source-level compatibility at the interface level.

Introducing the combatants

Accusations have been flying once more between two vendors of operating systems that claim Unix compatibility and real-time performance. The antagonists are VenturCom (Cambridge, MA) and Lynx Real-Time Systems (Campbell, CA). VenturCom has accused Lynx of making misleading claims about Unix compatibility of its LynxOS. Lynx countered with its own charges and clarifications.

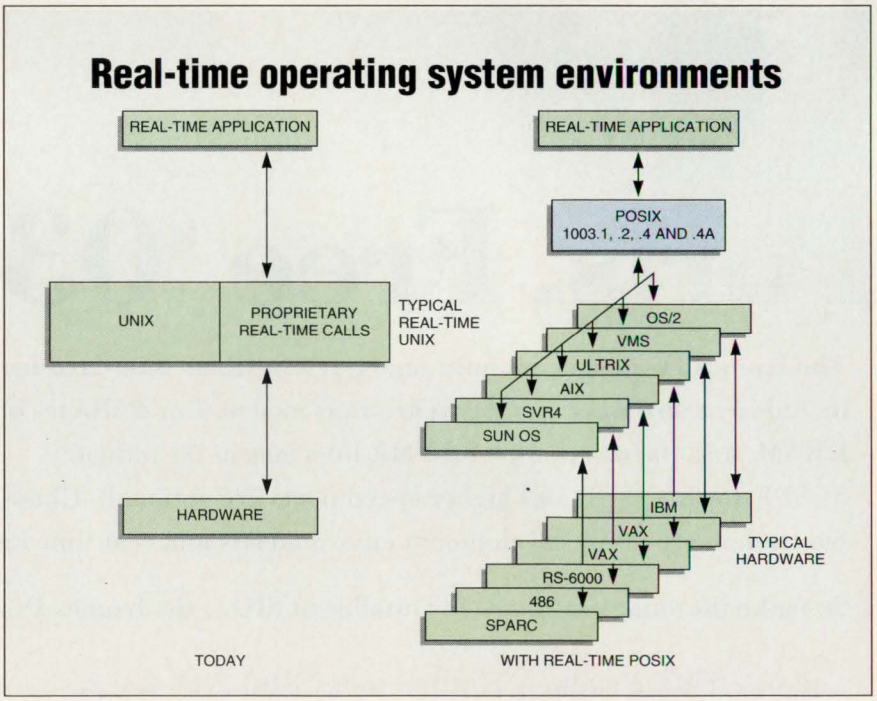
Whether VenturCom's Venix is Unix-compatible doesn't appear to be at issue, since VenturCom has licensed Unix from AT&T and modified it for real-time functionality. LynxOS was developed using the clean room method.

Both companies' operating systems are open to the description "nonstandard" or "incompatible with Unix" when it comes to the real-time functions. That's simply because Unix is not a real-time operating system and there aren't, as yet, any balloted and agreed-upon standards for real-time extensions to Unix. To take advantage of real-time functionality, in both systems, therefore, the user must make proprietary system calls. Any application which makes proprietary system calls will not be portable to another operating system environment.

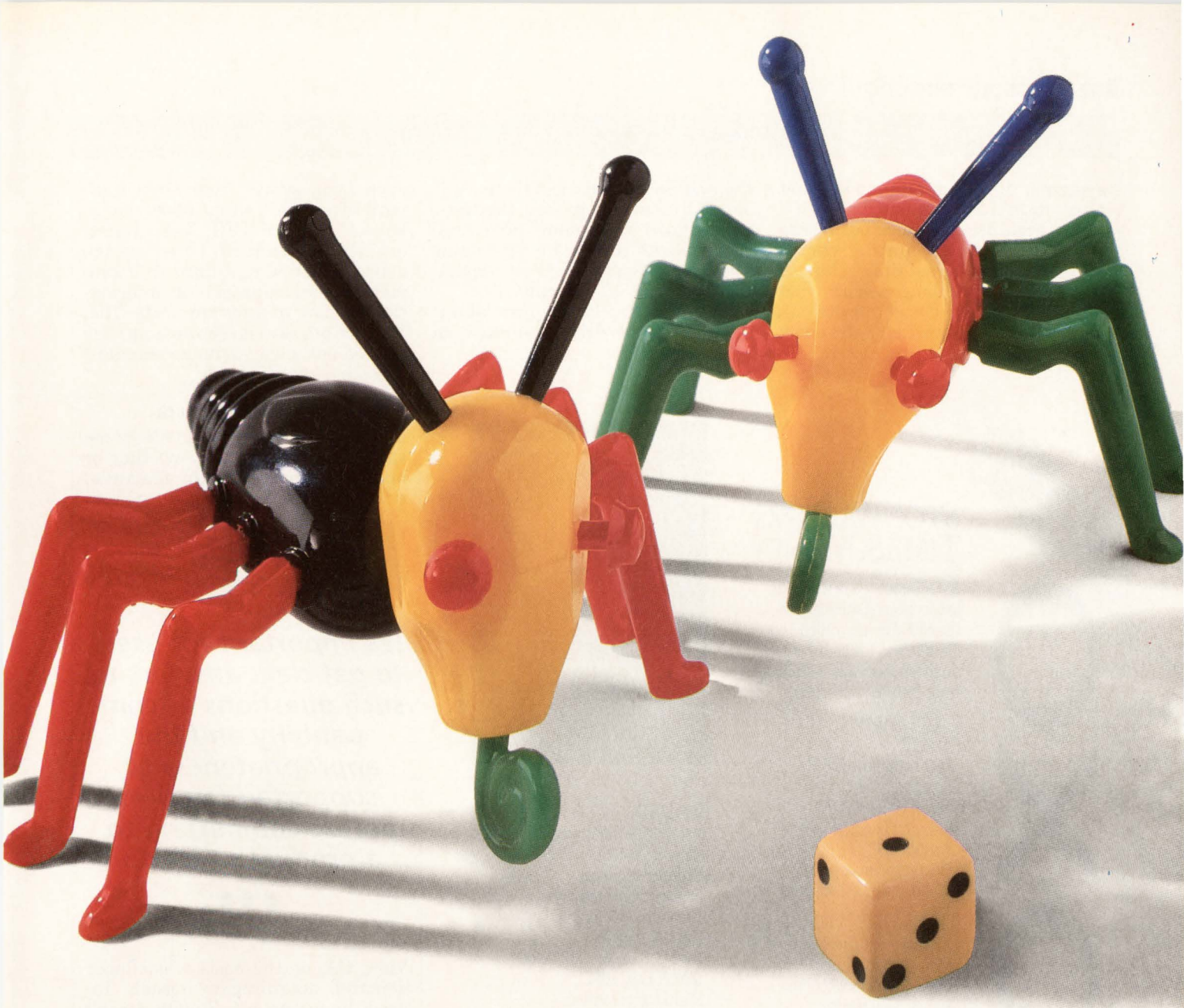
The first salvo

So what's all the fuss about? VenturCom has been circulating a paper in which it claims to have examined LynxOS 1.2.1 against AT&T Unix and found significant areas of incompatibility. It claims, among other things that eight of the 69 Unix system calls were omitted and that 70 of the 142 Unix subroutines were missing from that version of LynxOS. Lynx counters that VenturCom's claims are, "just flat out wrong," according to vice-president of marketing Moses Joseph. "System calls are a fundamental part of binary compatibility," Joseph says. In addition, he notes that the report, which was written last April was based on LynxOS version 1.2, for which he says Lynx doesn't claim full Unix compatibility. According to Joseph this was done at a time when Version 2.0, for which Lynx does claim Unix compatibility, had been shipping for several months—since January 9, 1991.

Joseph says there were four Unix system calls—not eight as claimed by VenturCom—that were unsupported in version 1.2.1, three were Streams calls and all but one are now supported in Version 2.0. The as yet unsupported call is the *acct( )* call which provides accounting information for multiuser commercial



Today's real-time Unix operating systems depend on proprietary calls to get deterministic performance, an approach that prevents real-time applications from being portable. The emerging real-time extensions to Posix will provide a consistent interface to Posix-compliant operating systems and allow portability for real-time applications.



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systems. It's understandable that Lynx didn't feel supporting *acct( )* was a high priority since burdening the CPU with accounting chores isn't conducive to real-time behavior. Nonetheless, the danger exists that an off-the-shelf Unix application might make a call to *acct( )* and crash the system if it were not there. Version 2.1 (now in beta test), therefore, will support a "dummy" *acct( )* call that will not return any accounting information but will allow applications that call it to execute.

There's also a dispute about standard device drivers. VenturCom says Lynx strays from Unix compatibility with a proprietary device kernel interface (DKI). Lynx counters that standard Unix device drivers can't be real-time, so it provides device support and information on how to program to its DKI. VenturCom says it (VenturCom) has figured out a way to make standard Unix drivers real-time.

Attack and counterattack

Lynx has admittedly made some value judgments about whether or not to support certain features, notably the remote file system (RFS), which it doesn't support. Lynx chose instead to support the network file system (NFS) developed by Sun Microsystems (Mountain View, CA) on the basis of customer demand, according to Joseph. Indeed, he points out, SunOS doesn't have a number of the library calls cited in the VenturCom report and nobody is accusing SunOS of being incompatible. It's a spin-off of Berkeley Unix as is LynxOS, Joseph points out. Anyone contemplating use of a "Unix" would be well advised to consider these differences. So again, what is "true" Unix as defined by the market?

It's important for users to get clear answers to such questions as compatibilty and the appropriateness of supported features before committing to a product selection.

Much of the discussion about compatibility gets down to a somewhat juvenile, "Is not! Is so!" level. VenturCom's marketing director Kim Carpenter, for example, claims that Lynx, "starting from the ground up as it has, doesn't have the capability of doing this [achieving 90 percent Unix compatibility]." Lynx counters that it certainly does have the capability. The proof of compatibility rests in the execution of code.

VenturCom also attacks Lynx for

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nonsupport of certain capabilities supported by VenturCom, but which appear not to be issues of Unix compatibility per se. The ability to run DOS applications under Unix, for example, is seen as a compatibility issue, as is Lynx's lack of support for the Weitek math coprocessor. Although the statements made by VenturCom are true, they don't always address issues directly affecting Unix compatibility. It's left to the user to decide how important they are.

The issues surrounding real-time functionality get absolutely surreal. It seems bizarre for VenturCom to criticize Lynx for supporting draft 9 of the 1003.4 real-time extensions to Posix—calling that nonstandard—while it requires the user to make proprietary calls to access real-time functions in Venix. Lynx's Joseph explains that when Lynx got a very large contract from NASA, which decided to use LynxOS for the space station Freedom, a key requirement of the contract was to support Posix 1003.4 draft 9, which has since been rejected by the committee. "NASA estimated that Posix real-time would be balloted, finished and ready by 1991," says Joseph. Now the standards committee is expected to ratify draft 11 or 12. "But from the operating system level, the changes are minute," Joseph says. "Whatever happens to the draft, it will be a very trivial task for Lynx to supply the customer with a patch."

The aftermath

Unfortunately, it ultimately remains the users' task to determine how well a product suits their needs. In fact, for embedded real-time applications, as opposed to those that involve a large amount of user interaction or the use of off-the shelf programs, the advantages of Unix lie primarily in the development environment rather than in having a Unix-compatible kernel in the final embedded system. And other non-Unix kernel vendors, such as Wind River Systems (Alameda, CA) to name one, provide a Unix-based development environment and a huge number of development tools for many systems running under Unix. Users must decide if the seamless combination of the real-time aspects of an application with standard Unix services and features are important for their final systems—and in many cases they are.

The accusations raised by VenturCom appear to be a tempest in a teapot. It certainly would have added credibility to their charges if they had used the currently shipping version of LynxOS. Nonetheless, the issues raised are ones that are not trivial. It's important for users to get clear answers to such questions as compatibility and the appropriateness of supported features before committing to a product selection. Unfortunately, it seems that users will still have to dig those answers out by themselves.

A copy of the VenturCom report is available from VenturCom along with a technical overview of AT&T Unix. Likewise, a copy of the detailed Lynx response is available from Lynx Real-Time Systems. ■

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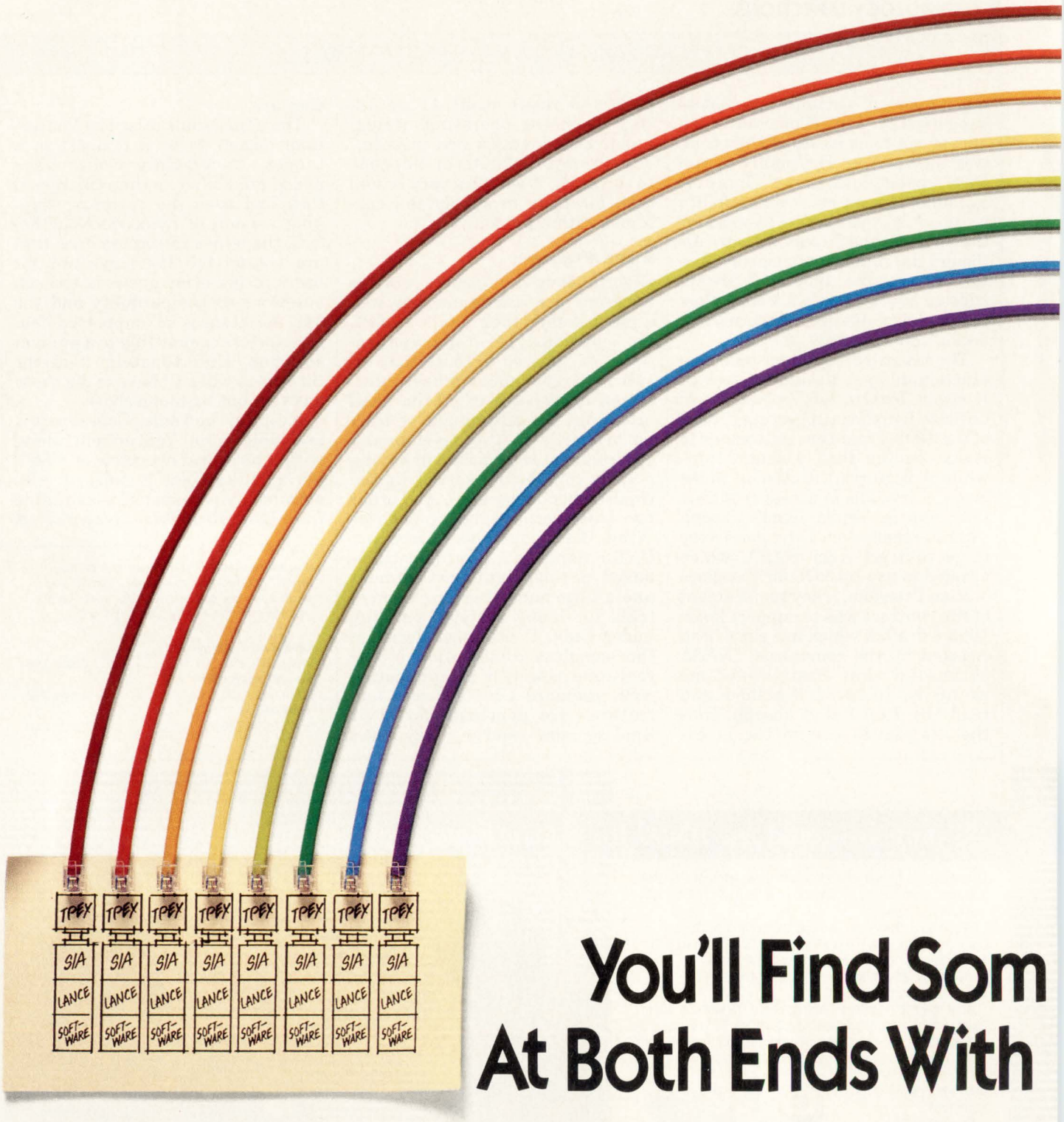

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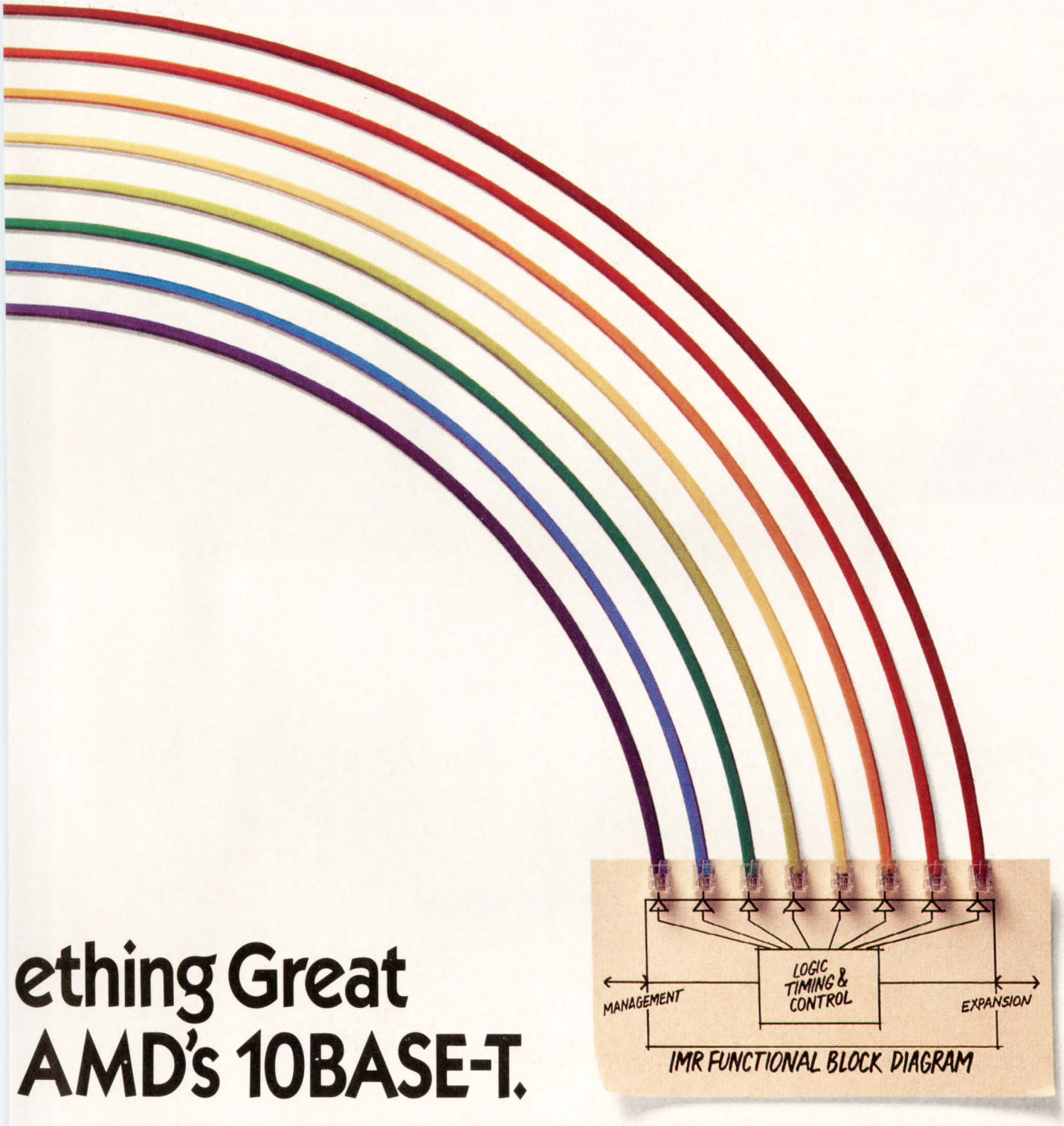

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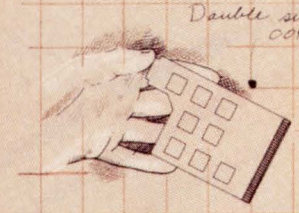

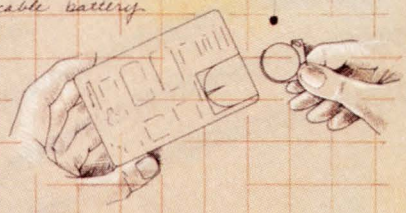

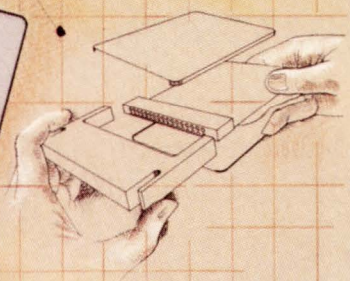

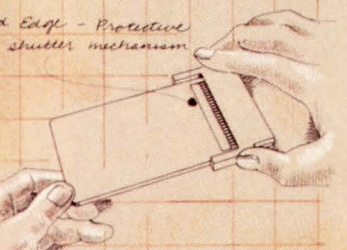

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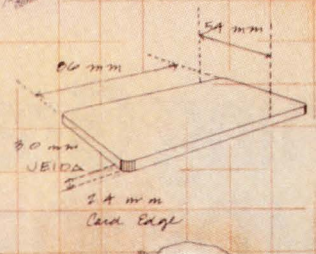

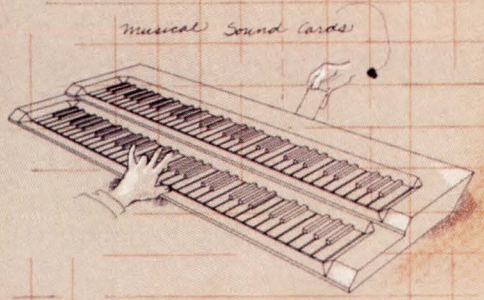

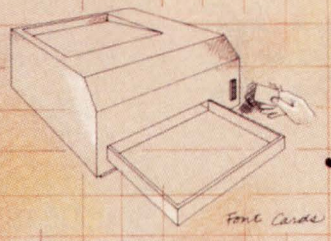

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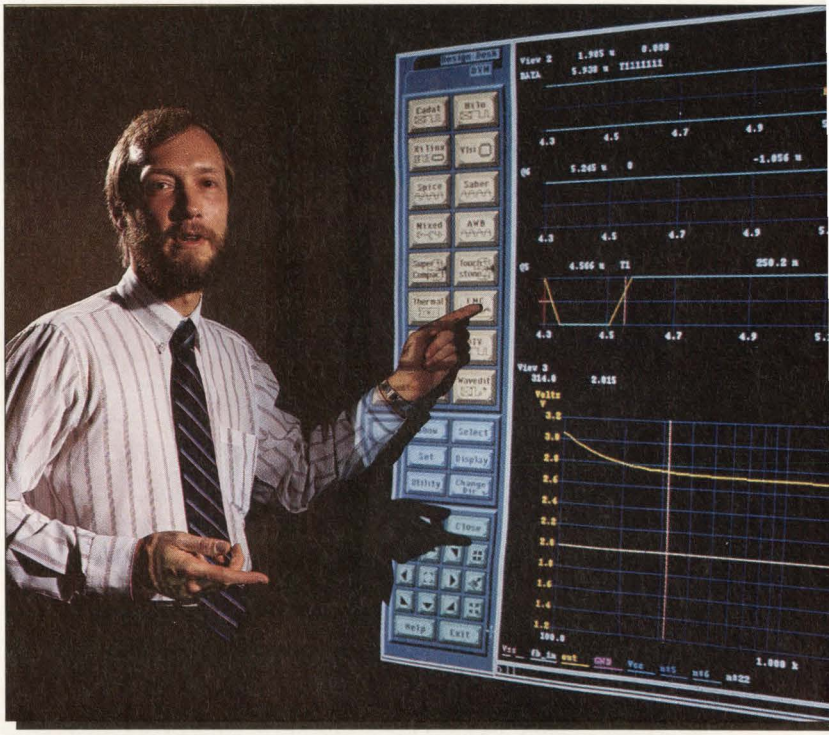
CIRCLE NO. 47

Framework vendors hammer out standards

While users demand plug-and-play framework architectures to customize design environments, EDA vendors are trying to agree on standards that won't compromise performance.

Mike Donlin
Senior Editor



"No single vendor can supply every tool a user needs," says Bernard Gilbert, senior technical consultant for Computervision's Theda framework-based tool suite. "So it's important for a framework vendor to provide an open environment . In this example, we've incorporated tools such as HiLo, Saber and Spice for a mixed-signal simulation environment."

It's almost marketing suicide in the EDA industry to admit that you don't have a framework, or at least believe in the idea of a software standard for design tools. Every tool vendor, from the largest offering complete suites of design tools, to the smallest niche supplier, has hopped on the framework bandwagon and promises cooperation with CAD Framework Initiative (CFI) efforts to provide a software infrastructure which will let multiple tools from multiple vendors work on multiple platforms. But anything that tries to accommodate that many architectures and corporate strategies is bound to run into problems. The challenge for EDA vendors is to remain open to an evolving standard while developing competitive tools without sacrificing too much of the existing product line. The fact that the EDA industry started with closed, proprietary tools running on dedicated hardware platforms further complicates this transition to open, standards-based tools.

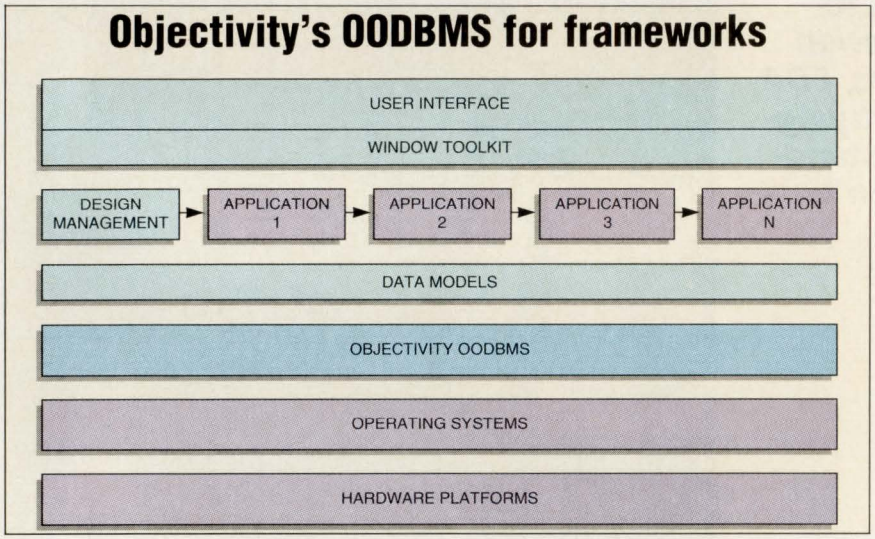
In spite of these obstacles, CFI's efforts are producing results, and a standard is slowly emerging. At this year's Design Automation Conference (DAC), tools from different vendors were sharing data across a number of different platforms. "This year we showed the tools using what we call a design representation server," says Andy Graham, president of CFI. "The server is a place where a tool can request data and get it. The data can come from a database, another tool or anything that owns the design data."

CFI enlisted over 22 organizations to modify their tools to use the newly developed specifications. EDA vendors from North America, Europe and Asia worked together to integrate 34 different software products using the same set of CFI-developed standards. The project was composed of three parts. Part one focused on uniform methods for integrating tools into the framework. Part two emphasized a single way for representing design data, while part three allowed tools to communicate with each other in an open,

non-proprietary fashion. Participants provided either a framework "cockpit" for controlling the tools, a design representation server for storing information or an application tool that produced or consumed netlist information.

This level of cooperation among competitors is impressive and, according to the CFI members, will have to continue because of pressure from EDA users. These users don't really care how the tools work together, as long as they can get the best tool for a job and integrate it into a coherent suite of design tools.

"I've talked to engineers who use tools from many different vendors and they say that for every dollar they spend on a tool, they spend one or two dollars integrating them into their design environment," says Jayaram Bhat, director of frameworks at Cadence Design Systems (San Jose, CA). "That's a hidden cost that frameworks and standards must address. If we don't lower that cost of integration, we won't be able to sell tools and everyone loses."



Some EDA vendors are turning to third-party database companies such as Objectivity, to supply database management systems (DBMS) for their frameworks. The DBMS must support teams of users working at different locations on networked workstations from multiple vendors. Objectivity's DBMS resides as an extension of the operating system to provide transparent distribution of data control. Multiple databases may be located anywhere on the network with administrative control by individual users, groups or departments.

Agreeing on model standards

Cooperation, of course, means compromise, and though the CFI members have been able to hammer out some standards in the areas of procedural interface and design data representation, much work remains in sensitive areas such as component information representation (CIR)—data that's at the heart of each company's product line.

"One of the hottest issues right now is CIR," says Graham. "If we talk about data representation as the way that the components of a design are hooked together, then CIR describes the library elements behind the tools. We can't have real integration until we have some standards in the area of libraries."

Because there is such a difference in the way tool vendors, model developers and even silicon houses represent library models, it's clear that a standard might force some companies to rework their models. That requirement could cause problems for simulators that are tightly tied to the way that devices are modeled. "It's going to be tough to arrive at a CIR standard until we agree on a simulation language," says Stephen W. Director, dean of the college of engineering at Carnegie Mellon University (Pittsburg, PA). "Eventually, there will be two or three simulation languages with interfaces to support the various core models. One of the disadvantages of this approach is that performance might suffer, but as more powerful workstations come on the scene, I don't think that will matter too much."

No one will welcome standards for models more than the silicon vendors who are being pushed by their customers into the modeling business. For them to sell silicon, these vendors have to provide models of their products for simulators early in a system's design cycle. Writing models for all the different simulators, however, gets to be an expensive proposition, so the responsibility for writing models is reluctantly shared by simulator vendors, silicon houses and customers. But because inadequate or inaccurate modeling information can render a simulation useless, there's intense pressure from EDA users to get coherent library information, preferably written in a standard hardware description language such as VHDL or Verilog. "Right now we have to invent coupling software so our models will work on all the different simulators," says Robin Steele, manager of software development/CAD products at NCR (Fort Collins, CO). "CFI is helping by developing procedural interfaces that will eventually let us plug and play with a framework standard. We still will have to optimize our data on a tool-by-tool basis, but we won't have the integration nightmare that we have today."

Managing the data

Even with all the effort being placed behind the development of standards for tool integration and communication, it's clear that for a while the EDA industry will have to deal with the complexities of multiple subsets of standards to accommodate different vendors' tools. After all, no tool vendor is going to throw out major parts of its product line to adhere to a standard. This will mean that most design environments will have several frameworks, each tailored to a specific part of a system's design. Such an environment can quickly get unwieldy unless some sort of management software—a sort of super framework—is used to oversee the various phases of a product's design. "One of the biggest problems our customers have is the proliferation of data across a design environment," says Fred Langhorst general manager of the framework products division at Mentor Graphics (Wilsonville, OR). "The design of a typical system can involve literally hundreds of thousands of data files, all of which need to be tracked and managed. Product data management will be a broad-based approach to this task

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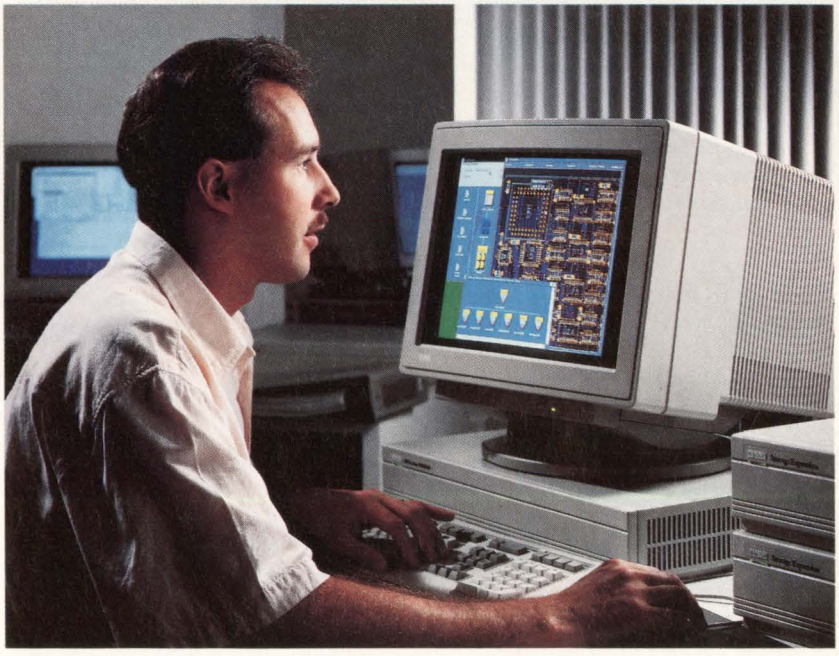

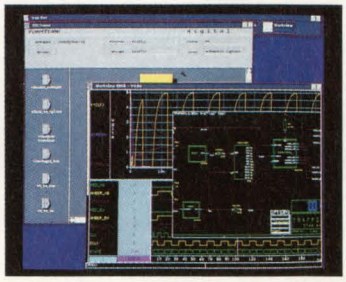

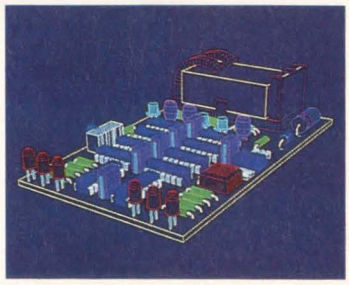

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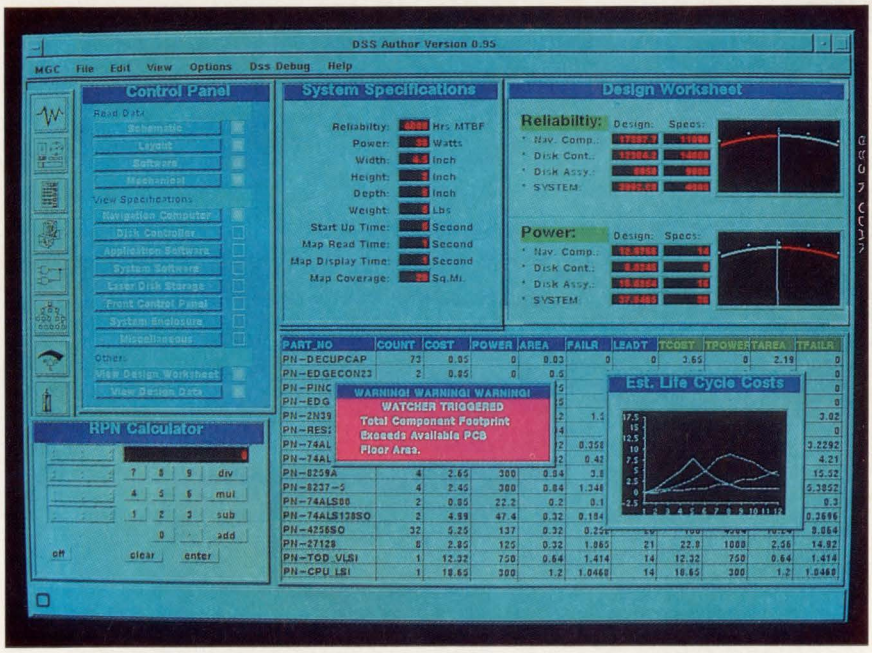
and will stretch beyond a single discipline, so that the electrical, mechanical, manufacturing and software pieces of the design cycle can be managed."

The need to manage design environments that span all aspects of EDA—electrical, mechanical and manufacturing—is causing tool vendors to break down the walls that have existed among these disciplines. Companies like Mentor Graphics have incorporated some mechanical tools into their electronic design environments, while Computervision (Bedford, MA) and Dazix (Boulder, CO) are capitalizing on an established base of CAD tools by incorporating them into their EDA frameworks.



Mentor Graphics' Decision Support System (DSS) manages multiple tasks through the Falcon Framework. Applications built within DSS can include action buttons, gauges, dials and constraint watchers. Here, DSS has triggered a warning indicating that the footprint of the components used in the design will exceed the available circuit board area.

Because the data that each of the various tools uses is so different—mechanical design data might contain gears, while electrical data contains gates and components—managing them will be a challenge. For a tool like this to work across multiple environments, it must be able to check the status of the individual parts of a design, without actually manipulating the data that these disparate databases hold.

The database debacle

This critical point—how the unwieldy data in a design environment is represented, addressed and manipulated—is being debated among framework vendors. "Years ago we tried unifying tools with a hardwired approach," says Larry Rice, senior product marketing manager at Valid Logic Systems (San Jose, CA). "But over the years, as we acquired tools from other companies, we realized that we couldn't continue to do that. We decided on a multi-database approach which gives a tool its own database that can share information with other tools on a need-to-know basis. Not every tool needs to share data with every other tool." Valid's Design Process Framework revolves around the coordination of multiple open databases. According to Valid, this not only lets a tool operate at peak performance by using its own separate database, it's easier to integrate a third-party tool into the framework, because the process doesn't involve proprietary database constructs. Valid is using a commercially available object-oriented database management package from Objectivity (Menlo Park, CA) to handle the administrative part of its framework.

Proponents of a single database structure, such as Mentor Graphics, counter the arguments of multiple database advocates by explaining the mechanism behind its unified database approach. Valid points out that there's a difference between the data-access mechanism (the part that knows how to get the data) and the data that's used (the data model). An IC layout editor, for example, needs to work from a data model that's different from the one that the simulator's using. This doesn't mean that there's a different data-access mechanism for every tool, it means that there are multiple data models with a common access mechanism.

It's possible that CFI can stay out of the database fray by proposing a standard that lets either approach work within interface guidelines. "People have gotten excited about databases for quite some time now," says Carnegie Mellon's Director. "But I don't think we'll ever have a database that's the official EDA database, mainly because every tool is working with a different set of objects. Within each domain we'll have a certain type of database and we'll have to find ways to let these databases interact with each other."

In spite of the soothing promise that databases can be proprietary or commercial and still fit into a framework standard, there's another issue that can make a potential tool buyer nervous. They want to know who eventually will own the data. "Remember, in a lot of customers' minds if you own the framework, you own the data," says Will Herman, senior vice-president of engineering at Viewlogic Systems (Marlboro, MA). "That's the political side to a framework. In the end, when a customer has produced a chip or board or system, it doesn't matter what tool they used to produce it. The critical point is how tied the data is to an EDA vendor. That's where a lot of the jockeying among EDA vendors is taking place."

A source of agreement

Though the dust is settling over which database approach is best, there seems to be a consensus among large EDA vendors that the object-oriented database (OODB), rather than a relational database (RDB), is the best approach. In addition to letting users model complex design automation data without compromising storage efficiency, an OODB has an extensible base, which lets data models, files and tools establish relationships

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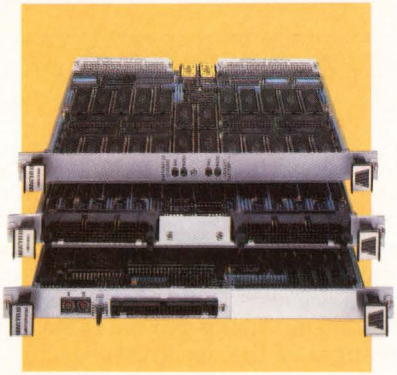

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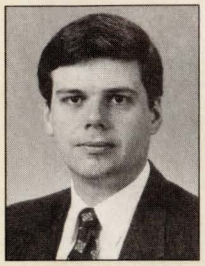
Database technologies in the CAD environment



The CAD database challenge is to accommodate increasingly complex design data while providing rich data modeling services, large capacity, high performance and data access. In addition to managing data, CAD database solutions must manage the relationships between data. Relationship information and other data about the design data is often referred to as meta data.

Many approaches to database solutions have been used by the CAD industry including the file system, relational database management systems (RDBMS) and object-oriented database management systems (OODBMS). The simplest solution to providing data storage is to store data in a file using the file system. Data can be stored in either binary or textual representations. A binary representation uses disk space efficiently and is usually closely related to the in-memory representation of the data. Textual representation allows a human readable format and simpler data extraction. While certain data, such as a bill of materials, may be easy to extract from simple file-based storage, extracting dependency or hierarchy information can be quite difficult.

The file-based management system has no modeling capability and hierarchy information has to be determined by the process requiring the hierarchal data. The file-based approach also makes it difficult to evolve the design applications that use the data.

Relational databases organize data into tables composed of rows and columns. The rows of the tables, called tuples, store information about entities in the database. Relationships between tables can also be specified. By taking advantage of this technology, design data can be easily scanned to provide information such as a bill of materials. Modeling methods are also available to aid the CAD developer in creating a schema or data organization for design data.

The biggest disadvantage to relational database technology for CAD use is that it's difficult to model the relationships that exist in typical design data. A relational database has a flat view of data and most CAD data has strong hierarchy and many associations between elements.

The other significant disadvantage is that relational databases typically only have intrinsic knowledge about a few primitive types of data such as numbers and strings. These data types don't correspond well to CAD data which has many types of data, such as electrical nets, pins and symbols. These types of CAD data have to be represented in some alternate form and reconstructed when reading from the database. And evolving the relational database to meet changing requirements can be difficult.

Object-oriented database technology is an emerging technology that offers a new way to meet the needs of the CAD industry. An OODBMS can represent relationship information and model heterogeneous data by letting the database developer specify the objects and the relationships between objects in the database schema. The objects can be arbitrary entities and are not limited to a certain set of primitive types. Objects can be CAD entities such as electrical nets, pins and symbols. Object-oriented databases also place a strong emphasis on modeling the relationships between objects. One-to-one, one-to-many and many-to-many relationships are usually directly supported. These relationships can be used to model CAD design data hierarchy directly.

An example of an OODBMS-based system is the Design Data Management System (DDMS) used in the Falcon Framework. The DDMS provides an object-oriented design object interface to design data. Data models inherit their basic behavior from the DDMS. This includes common access methods to all data models which lets groups of applications easily work together on common data. Each application manages its own data through its data model to ensure high performance and storage efficiency.

Meta data management is also provided through the DDMS design object interface. This lets design applications and designers create references between design objects, attach properties to design objects and to their references, and perform other design management functions such as copying, moving or releasing configurations of design objects. An interface to design objects is made available through the Falcon Framework extension language, Ample. The DDMS also allows CAD integrators to register their own tools and data types. Once a type has been registered, design objects of that type can be created and used.

A. Remy Malan, product manager, Framework Products Division, Mentor Graphics

with each other. "Overall, relational database technology is best suited for static data, while object oriented technology is best for dynamic data," says Steven Schulz, a member of the group technical staff in the automation engineering and technology division at Texas Instruments (Plano, TX). "Both technologies have disadvantages directly related to the way that data is organized and stored. CAE data is a mixture of both static and dynamic data, with most data consisting of static information such as internal part numbers or component delay values. But as clock rates rise and concurrent engineering concepts take shape, more accuracy will be required, and that means using dynamic data that changes as the design evolves."

Regardless of which database technology or architecture framework vendors embrace, it's clear that many of them would like to get out of the database business altogether and concentrate their R&D efforts on the performance of their tools. And third party database vendors such as Objectivity and Object Design (Burlington, MA) will allow EDA vendors to do just that. For its part in the database debate, CFI will probably avoid dictating specifics altogether and provide an interface standard so that any tool can access any database. This will let EDA vendors migrate their products over to third-party databases

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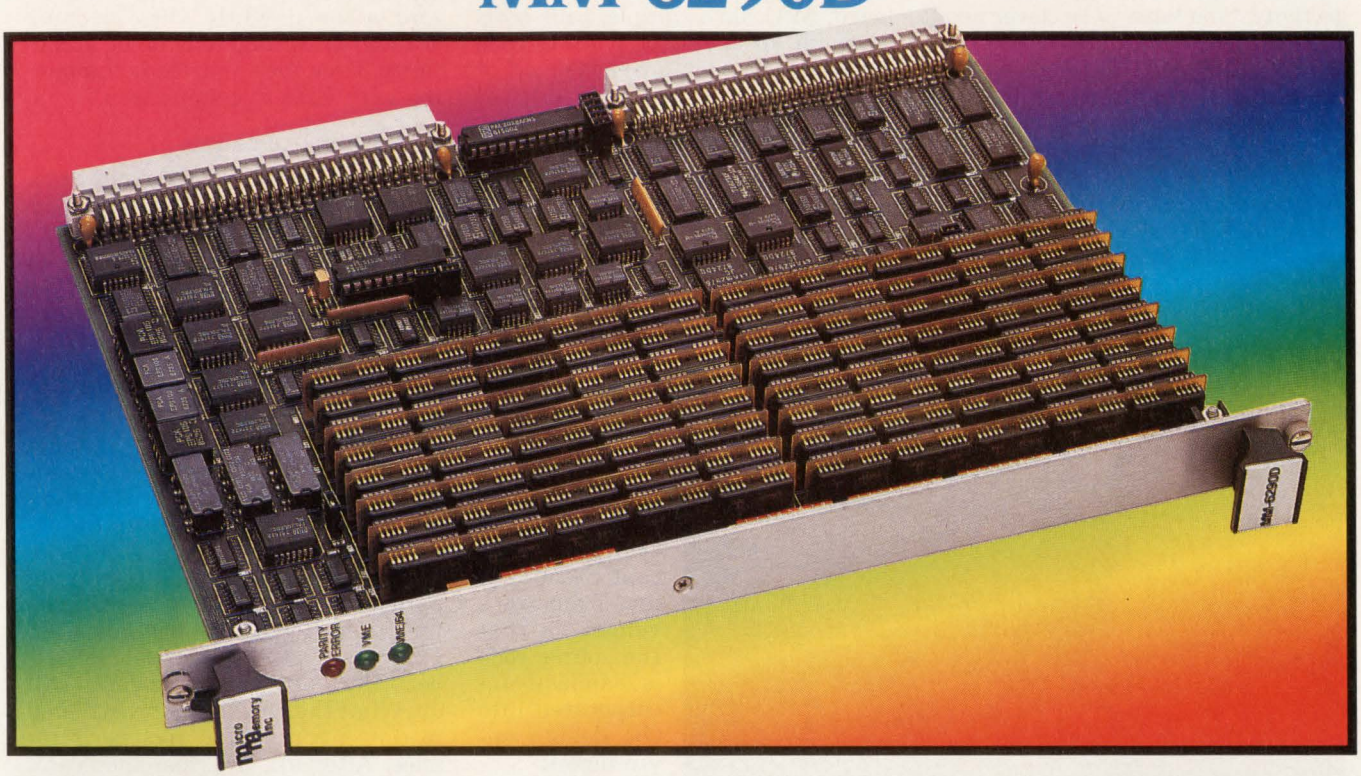

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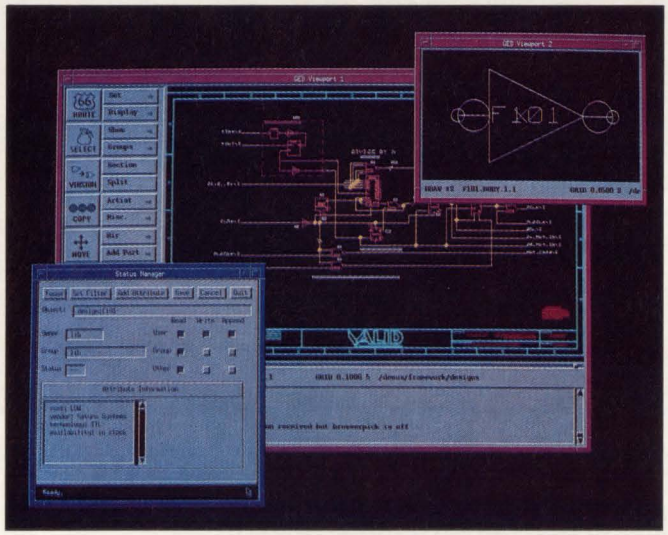
which are optimized for speed. "Performance relates directly to how much you can do in memory as opposed to having to go to the disk," says Andrew Wade, vice-president at Objectivity. "You have to be clever about clustering the data and manipulating it efficiently. It takes a lot of R&D effort, which many EDA companies would like to avoid."

Tools working together

Another critical part of an open framework is its ability to easily accept tools into a design environment. Many IC designers and systems houses have a collection of favorite tools, both proprietary and from third-party vendors, that they will undoubtedly want incorporated into any frame-work they purchase. "We're responding to customer pressure to provide links so that our tools work with other tools," says David Potts, senior systems architect at GenRad (Fareham, Hants, UK). "And we're going to have to provide those with or without CFI. As a vendor of tools that must work in frameworks, our very survival hinges on our tool interoperability, as well as performance."

There's a considerable difference, however, between the two methods of incorporating a tool into a framework—encapsulation and integration. Encapsulation is the simpler of the two because it doesn't involve modification of a tool's source code. Often, file-based interfaces are all that's needed to encapsulate a tool for an environment. Powerframe from Digital Equipment Corp (Maynard, MA), for example, calls tools through an agent, or piece of code written in C. A window-based tool or template provides a graphical means to represent a tool's inputs and outputs. The user can define operating parameters and default options, though the template's generic routines will handle only about 30 percent of typical encapsulation code. DEC provides training courses to assist designers through the manual portion of the encapsulation process.



Valid Logic's Design Manager provides design data management and administration capabilities across its ValidFrame framework. The tool automates library management through workspaces that facilitate distribution and authorized use of part libraries. Using the Design Manager, library administrators can assign user-access privileges and define pertinent status attributes for parts.

Tool integration, on the other hand, requires close cooperation between a tool developer and framework vendor so that the source code is seamlessly incorporated into the design environment. Many EDA vendors have penned agreements with niche tool suppliers to do just that, with the resulting tool taking on the look and feel of the framework rather than the third-party supplier.

Though providing integration and encapsulation services can become a problem that tool vendors, VAR's and end-users all may want to handoff rather than handle, the hope is that standards from organizations such as CFI will make all levels of tool interoperability much easier. This will require active participation by computer hardware vendors in the development of these standards so that many of the services provided by frameworks today will become extensions of a computer's operating system (O/S). "If standards are to be successful, they have to be supported by a broad constituency," says Aart de Geus, senior vice president of engineering at Synopsys (Mountain View, CA). "It's going to take more than just cooperation of EDA vendors. It's easier for us to buy a database bundled with the O/S from Sun or IBM than it is from a direct competitor. Graphics packages are often bundled with an O/S and after a while they become standards through customer acceptance. I see the same thing happening with EDA tool standards."

Performance counts

With all this talk of frameworks, cooperation and tool interoperability, it's easy to lose sight of the fact that they actually exist to support tools. When all is said and done it's the individual tool's performance which will win customer's dollars. "We've heard from our user's group that a framework isn't the most important consideration when they're looking at tools," CFI's Graham points out. "Actually, whether a company has a framework isn't as important as what their future framework plans are. That tells a customer how open that company plans to be, and that's very important to a user. It's ironic, but often I'm trying to tone down people's expectations of what frameworks will do. What the EDA industry still has to concentrate on is tool performance. After all, if a customer can't get a tool to work, why would they buy more?" ■

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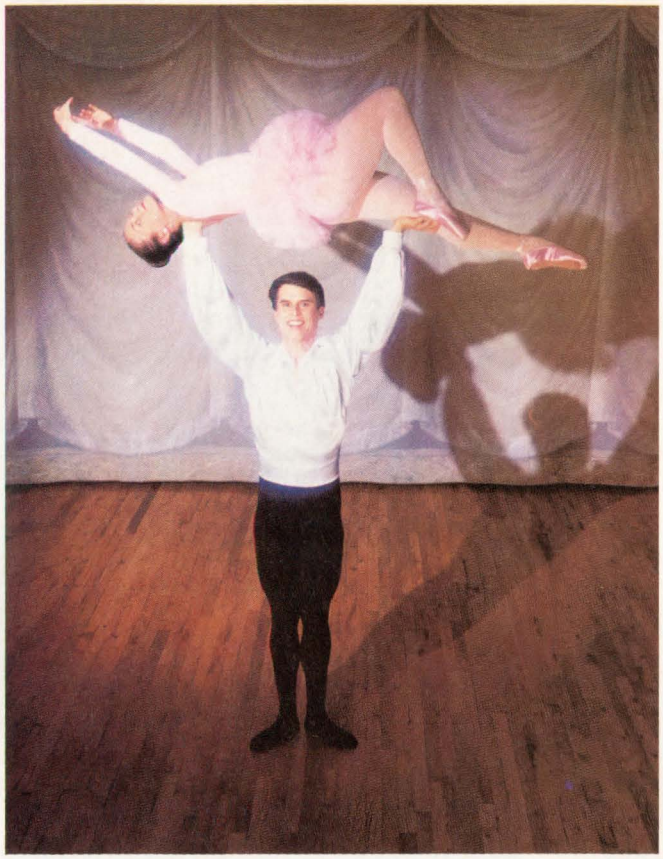

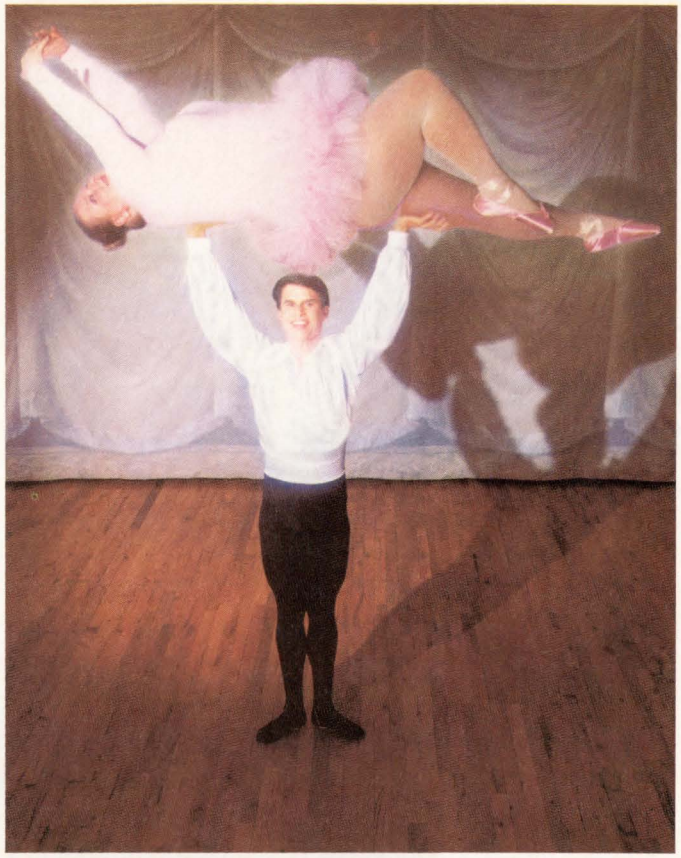

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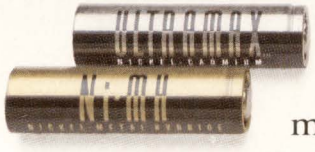

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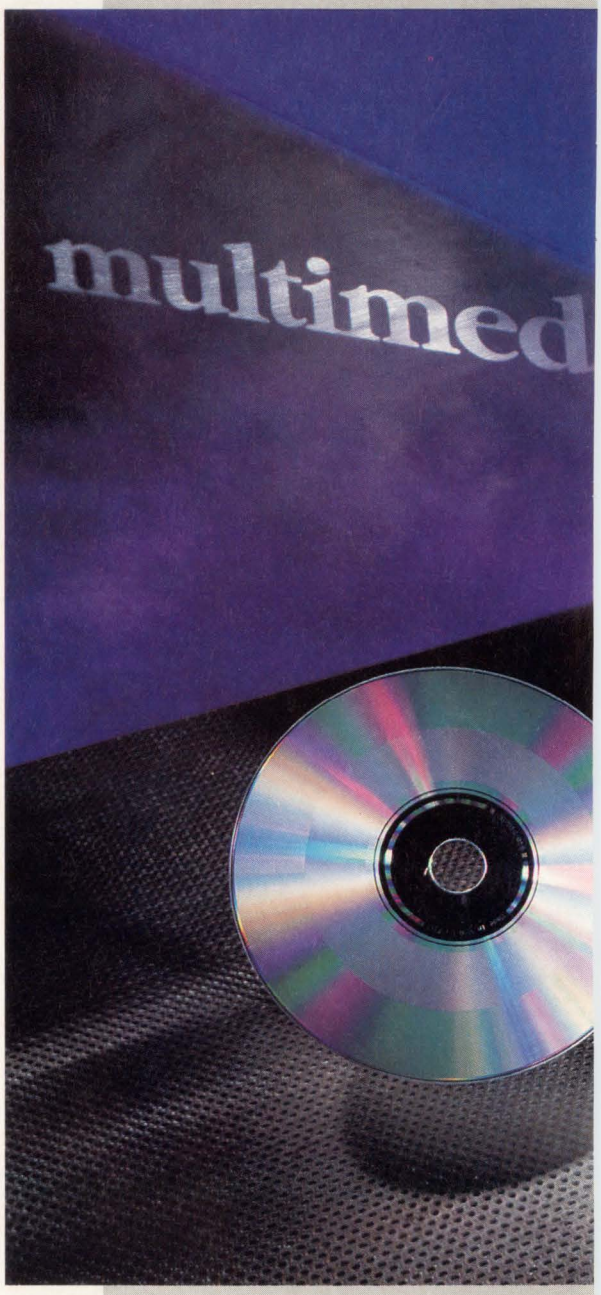

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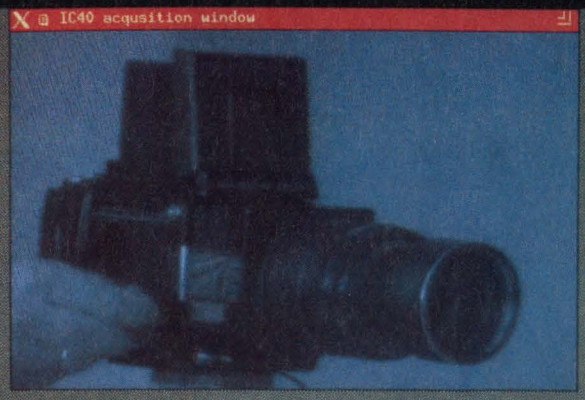

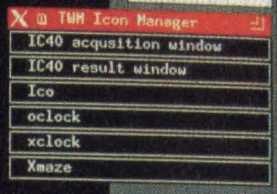

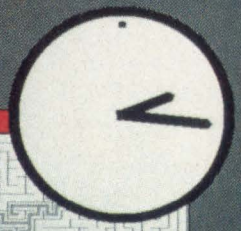

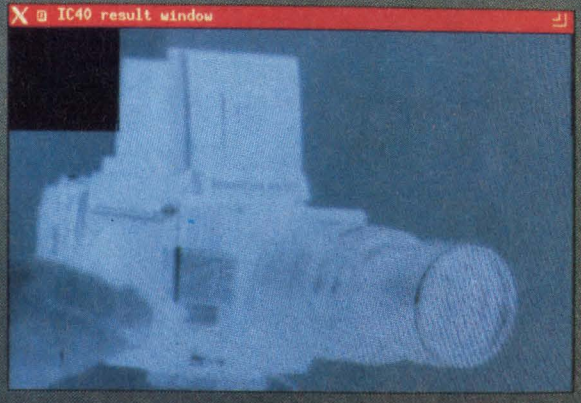

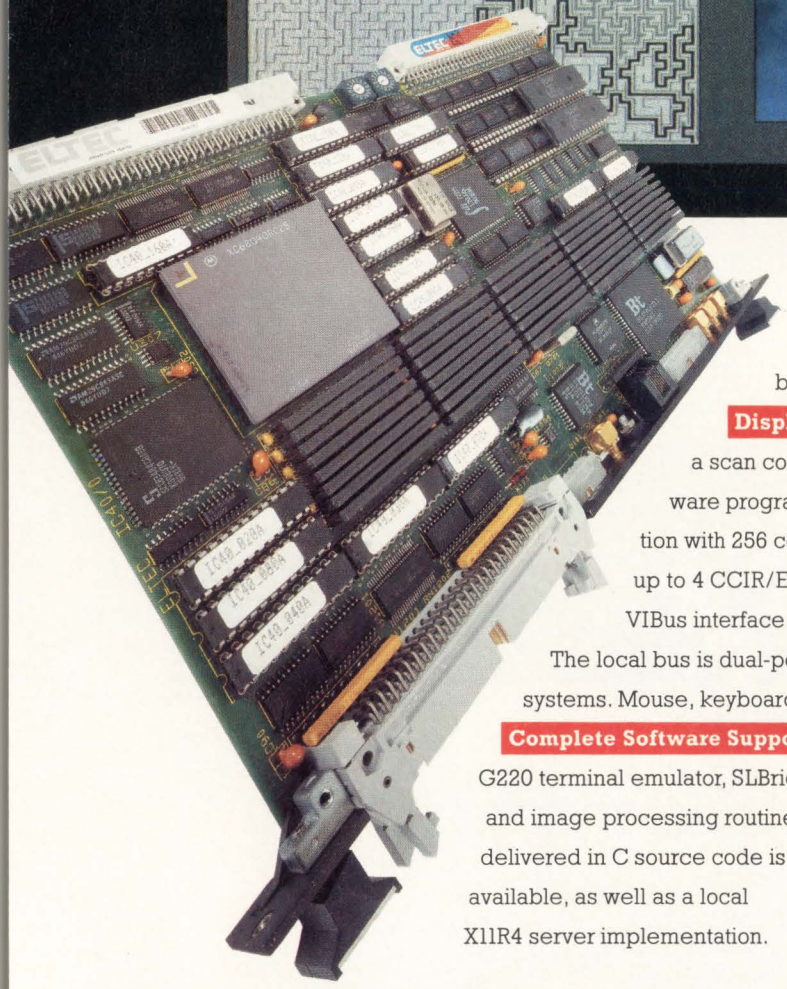

Photograph of Original Monitor

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CIRCLE NO. 53

Performance pushes RISC chips into real-time roles

The latest RISC processors are attractive for high-speed real-time applications. But advanced architectures aren't enough to win design-ins. Final system cost, availability of tools and other factors figure prominently in the design decision.

Tom Williams, Senior Editor

The F-22 uses Intel's i960 processor as its standard processor for all avionics, sensor and navigation functions.

When selecting processors for real-time applications, "people are going to RISC for pure performance," says Jerry Kirk, president of Microtec Research (San Jose, CA). "They want 50 to 60 Mips at the lowest possible price." The fact that the processors happen to be based on reduced instruction set computer (RISC) architectures, he points out, is incidental. Designers' real concerns are performance, system cost, time-to-market and a flexible path for future upgrades.

Vendors, however, are acutely aware that embedded applications of 32-bit processors represent a potentially large market. They know much is at stake; the processors that make significant gains in the embedded world will also be the most successful in other applications. So in their competitive zeal to push one technology over another, marketers of processors dream up RISC wars and other fantasies that obscure the real interests of design engineers.

RISC meets real-time

Designers have avoided using RISC for real-time applications for two reasons: the impact of large register sets on task context-switch time and performance penalties associated with cache misses. Cache misses affect the performance of RISC processors in particular because these processors are designed to operate with an unbroken stream of instructions, leading chip architects to build them with the largest possible on-chip caches. Both problems, however, can be addressed (see "Suiting up RISC for real-time," p 82).

Context-switch time comes up in almost every discussion about the use of RISC processors for real-time applications. For a RISC chip with relatively few

registers, such as the Motorola 88100, benchmarks show a performance advantage over a comparable CISC design (the Motorola 68030, for example) of about two-to-one. The key to dealing with larger register sets is to find a way to avoid saving all the registers to memory every time an interrupt occurs.

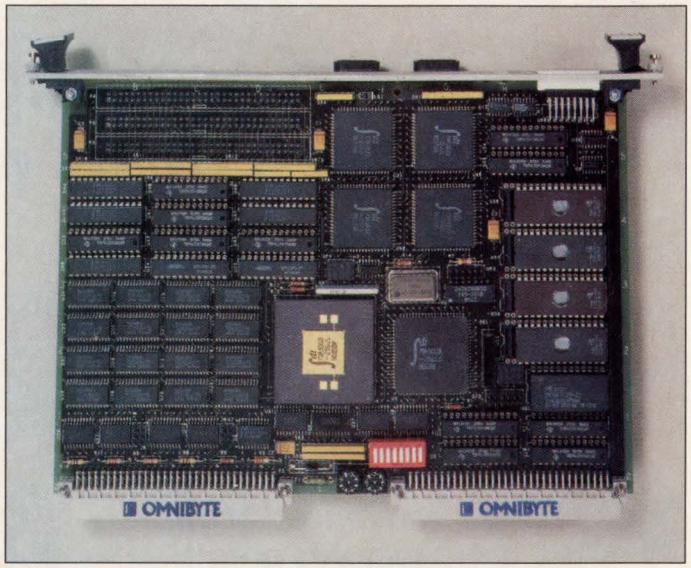
The MIPS R3000 processor, for example, reduces register-to-memory saves by grouping its 64 registers as 32 general-purpose and 32 floating-point. With this register grouping, developers of compilers and operating systems can choose not to save floating-point registers to memory when a context switch doesn't involve these registers. Once the compiler and operating system support that decision and the timing is established, the designer can deal confidently with known context-switch times.

The matter gets more complex with processors that have significantly larger register sets. The Sparc chip, for example, has at least 120 registers in most of its current implementations. Sparc is an architecture specification, however, not a device specification. This means it's possible to have a Sparc implementation with as many as 520 registers.

With 192 registers, the Am29000 processor, from Advanced Micro Devices (Austin, TX), has a very large register set. Its registers are not partitioned into groups, but rather in one large register file. The key to using such an architecture in a real-time environment is figuring out how to optimize context switching by determining which registers need to be saved for a given situation.

Real-time operating systems were written with CISC architectures in mind and simply save and restore all registers. This is clearly not an efficient method of oper-ation when these operating systems are ported to the Am29000 processor. Another alternative is to compute which registers are affected by each save and restore operation. "Both extremes probably have unacceptable effects on timing," says Norbert Laengrich, president of Embedded Performance (Santa Clara, CA), which supplies a development toolset (including an emulator and debugger) for the 29000. "Going too much to the optimizing extreme will send context-switching time back up because you're taking too much processing time figuring out what to do. And the possibility of errors increases."

Trying to find a happy medium between these extremes, AMD has classified context switches into six general categories. "What, after all, is a context switch," asks Brett Stewart, AMD's 29000 business development manager. "Far and away, the most common context switch in a procedure-oriented lan-



RISC processors are rapidly moving into high-performance board-level controller products. The Pulsar 3000 VME single-board computer by Omnibyte sports a 25-MHz MIPS R3000A. C Executive and VxWorks real-time operating systems are available for the board along with an extensive library of software development tools.

Sparc in real-time: The complexities of large register sets

Dealing with the uncertainties of context-switching times becomes more complex as the size of a processor's register set increases. Sparc processors provide a useful example of this complexity because most current implementations have at least 120 registers. But because Sparc is an architecture specification (not a device specification), it's possible to have an implementation with as many as 520 registers.

Overlapping register windows

Sparc's registers are arranged in logical windows of 24 registers, comprising eight input, eight output and eight local registers. Each window shares eight input and eight output registers with its immediate neighbors. For two adjacent windows, the eight physical registers that appear to one window as its input registers will appear to the adjacent window as its output registers. As a result, when two processes share adjacent windows, they can transfer data with no physical movement of data.

Sparc doesn't require that a process be limited to one window, so normally a context switch would simply save all active registers. That may be acceptable for a multitasking operating system, but it makes context-switch time unpredictable and possibly unacceptably long for real-time applications.

Companies adapting Sparc for real-time include Microtec Research, which is building a Sparc development toolset (compiler, debugger, etc.) and Metaware (Santa Cruz, CA), which is designing a C compiler.

Register windows in real-time

The approach taken by the two companies turns Sparc's large register set from a performance disadvantage into an asset. By dedicating a register window to each process, Microtec and Metaware make 32 registers available to each process (24 window registers and eight global registers). If a process requires more than 32 registers, then it must spill off into memory (it can't use another process' registers). In this scheme, a Sparc implementation with eight register windows could support four dedicated processes. The normally overlapping registers couldn't be shared, so the local registers of four windows would have to be invalid. The result is very fast context switching between processes in dedicated windows. If there are more than four processes (and there usually are), one window would have to be set aside for context switching with external memory, so only three processes could benefit from the improved context-switching times.

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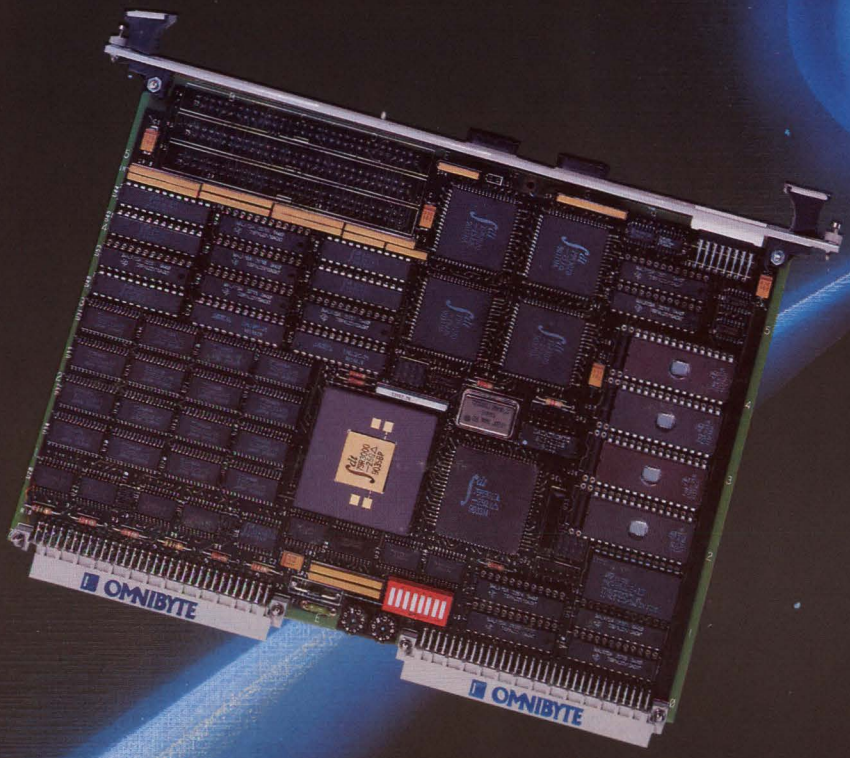

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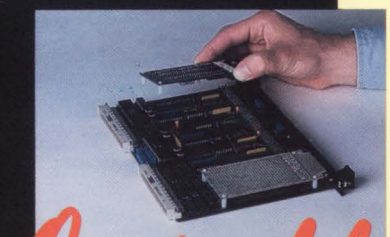

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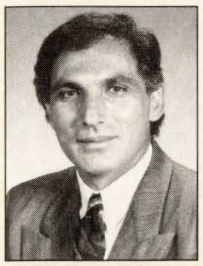
CIRCLE NO. 119

Suiting up RISC for real-time



Computer systems for real-time applications should provide high computational performance, efficient interrupt-handling capabilities, and high I/O throughput. Because real-time processing is deterministic, it also requires predictable, guaranteed response times. RISC technology provides significantly higher computational performance than CISC. The question is whether RISC also provides a similar increase in real-time performance.

Cache memory and a large register set—two architectural features of RISC—have been recently criticized as representing drawbacks for real-time applications. These drawbacks, however, can be addressed at the real-time operating system/kernel level, rendering them transparent to application programmers.

Cache problems

RISC processors rely heavily on cache memories. The predictable, guaranteed response time, therefore, must be calculated as the worst-case event (assuming that all critical tasks are not in the cache). To solve the unpredictability of cache memory, some developers propose running the RISC chip in uncached mode. Although designers would achieve absolute predictability, they also might lose most of the advantages of RISC as well.

Let's look at the cache drawback from another standpoint. First of all, the cache problem is not unique to RISC processors. Current CISC processors, such as the MC68040, also have built-in cache memory, and the same problem exists when such a processor is used in real-time.

The cache drawback may also affect the worst-case response time. In many real-time applications, the most important requirement is to meet the deadline for a specific task. For these applications, the overall time, which consists of the response time and the task execution time, is important and has to be predictable. Even if the response time is relatively slow because of cache drawback, a fast RISC processor will make up the time and meet the deadline.

For applications that require very fast, deterministic, and guaranteed response times, designers can still solve the cache problem. The Modcomp 2000 system, a tightly-coupled, symmetric multiprocessor that uses MC88100 RISCs, for example, targets the processor for interrupt handling. The developer can select a processor that will handle interrupts and nothing else. If the processor contains a large enough cache, and the developer carefully designs the interrupt tasks in such a way that all tasks can fit into the cache, it should be expected that everything will be in the cache when an interrupt occurs. In this way, the worst-case response time is significantly improved.

It's still questionable which RISC processor among a half dozen offered today performs better in real-time.

Another similar solution for the cache problem consists of incorporating high-speed local memories into a RISC multiprocessor system, in which all critical tasks can be locked.

Large register set problems

RISC architectures are register-oriented architectures, which typically assume a large register set. A large number of registers can significantly affect the context-switch times because the large register content must be saved.

Though the RISCs are based on register-oriented architectures, some RISC chips have relatively few registers. For example, the MC88000, i860, and MIPS processors all have only 32 registers. As a result, the context switch is fast. Some RISC processors, such as the MC88000, use a register scoreboarding technique, which allows all instruction units to share the register file. This can further improve context switching, because the registers don't have to be saved as often. In RISC chips with relatively few registers, a compiler plays a key role in allocating the registers.

Some RISC chips have a large register set, which may require more context to be stored during the context switch. The Am29000 processor and Sparc chips, for example, with 192 registers and 120 or 136 registers, respectively, are less suitable for real-time applications.

Problems with a large register set, nonetheless, can be overcome. For example, in the Am29000, the whole register set need not be saved during the context switch. The developer decides how many registers to save. This can reduce the context switch times, although it's a burden to application developers, who have to be extremely careful about using registers.

Other problems and solutions

Another drawback to RISCs, specifically the MC88000, involves certain operations that are critical at the operating system kernel level. When an interrupt occurs on a MC680X0 processor, the entire system state is automatically pushed onto the system stack. The operating system developer has to write code to save the state of the machine. This drawback is solvable. It has no impact on real-time performance. New revisions of RISC chips will solve this problem by moving the solution from software back to hardware.

Another misconception about RISC is that it's much more difficult to port operating systems and kernels from CISC to RISC platforms than from CISC to CISC platforms. Our experience in porting the REAL/IX operating system, a real-time implementation of the AT&T Unix System V, is that porting from CISC to RISC is the same as it is from CISC to CISC.

Our experience proves that RISC technology is well suited for real-time applications. Increased computational performance linearly improves real-time performance. Further, the architectural drawbacks of RISC processors in real-time are solvable. With a good, fully-preemptable real-time operating system, a powerful real-time RISC computer can be built. It still remains a question, which RISC among a half a dozen offered today, performs better in real-time. I would recommend one with relatively few registers.

Dr. Borko Furht is senior director of Research and Advanced Development, Modular Computer Systems, Inc.

guage is the procedure call." Where a CISC machine such as the 68000 has to save and restore registers for every procedure call, the 29000 uses a stack cache mechanism in the local register file. For lightweight interrupts, which don't involve a large amount of context, such as timer clicks or checking a queue, the 29000 has a freeze mode. When a lightweight interrupt occurs, one copy of the current program counter or status word is frozen. After the interrupt is serviced, processing resumes with the frozen copy. Four other categories of interrupts including two types of general interrupt handlers, synchronous and asynchronous context switches are defined according to the amount of overhead needed and the frequency at which they normally occur in applications.

According to Embedded Performance's Laengrich, his company is in the process of fine-tuning Ready Systems' VRTX32 29000 real-time executive to more closely match the Am29000's architecture. "The architecture and how you adapt the real-time operating system to the architecture is the key to performance," says Laengrich. Embedded Performance also will be integrating the real-time kernel into its Epic 29000 development toolset.

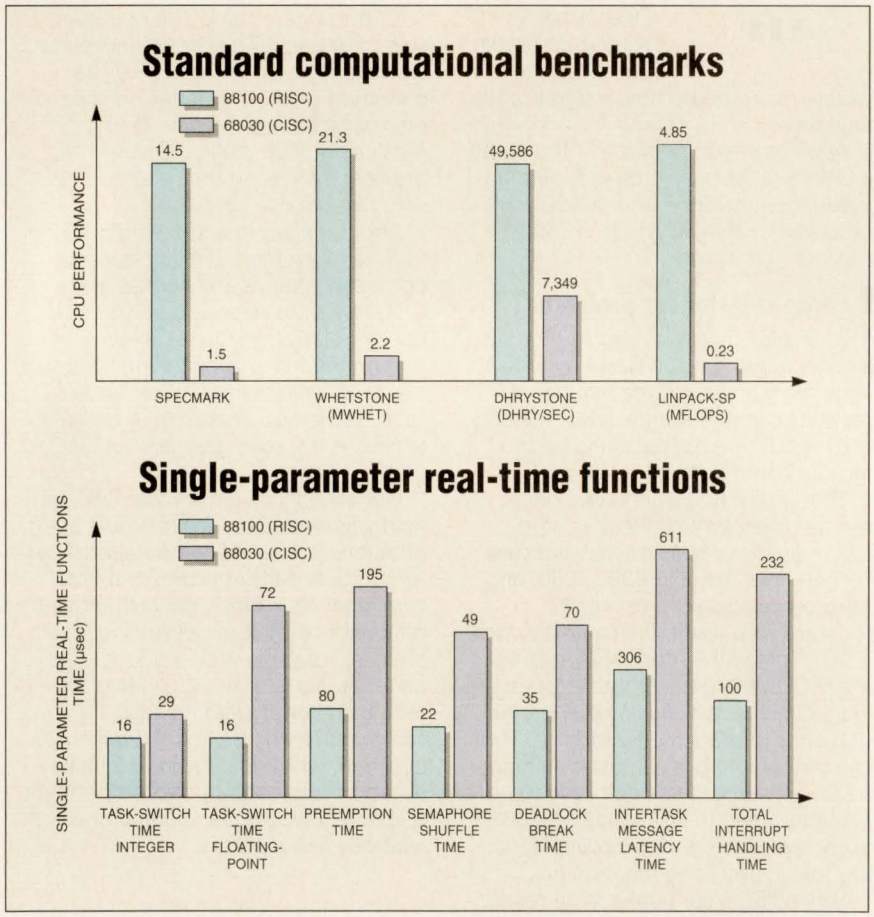
Taming cache behavior

One of the rationales of RISC (and of any modern highly-integrated processor) is to minimize the need to go off-chip. To that end, cache memories are either coming on-chip or being designed outside the chip so that they're directly controllable by the processor, yielding the benefits of large on-chip caches in many applications. According to Microtec Research's Jerry Kirk, "Good RISC performance means keeping the pipeline filled and always having the code right there in the cache." But these conditions can't always be met in an event-driven system. When an interrupt occurs in these systems, the pipeline must be flushed and refilled, resulting in a performance penalty. But pipelines and on-chip caches aren't unique to RISC architectures.

A cache is a statistical solution and as such is ill-suited to the hard determinism sometimes demanded by real-time applications. Because one can't be certain what's in a cache at every moment when an interrupt may occur, it's impossible to impose strict timing deadlines without accepting the worst-case delays associated with a cache miss. The solution for such demands is simply to use the cache memory in a way for which it wasn't originally intended by locking specific routines into or out of cache memory to ensure deterministic behavior.

"Real-time is at odds with the original intent of a cache," notes Dane Elliot, director of component marketing for MIPS Computer (Sunnyvale, CA). For example, the upcoming R4000 RISC processor from MIPS will have a primary cache on-chip as well as the ability to control a secondary off-chip cache. The R3051, a microcontroller based on the MIPS R3000 from Integrated Device Technology (Santa Clara, CA), has on-chip data and instruction caches. On both of these, it's possible to specify an address range and declare all or part of the cache locked. Critical interrupt routines can thus be kept in the fastest available memory and the designer can be confident of their timing behavior.

Given the ways that compiler and operating system vendors can adapt to take advantage of the features of RISC chips, there really should be little doubt as to whether RISC is suitable for real-time. Indeed, the raw speed of RISC alone usually eclipses performance of CISC processors. Optimization for context switching is really just icing on the cake. And most importantly, system designers don't have to do much differently when designing with a RISC—providing that they have a properly designed and integrated set of tools.



In benchmark tests performed by Modcomp, an 88100 RISC and a 68030 CISC processor were both run at 25 MHz. The standard computational benchmarks show that the 88100 processor performed about 10 times faster than the CISC machine. For a set of single-parameter real-time functions, the speed advantage is still about 2:1.

RISC development tools

When using RISC processors in real-time applications, it's critical to have operating systems and development tools available. "Not taking an off-the-shelf-operating kernel has some catastrophic time-to-market effects in short-term projects," warns Richard Jensen, vice-president for new business

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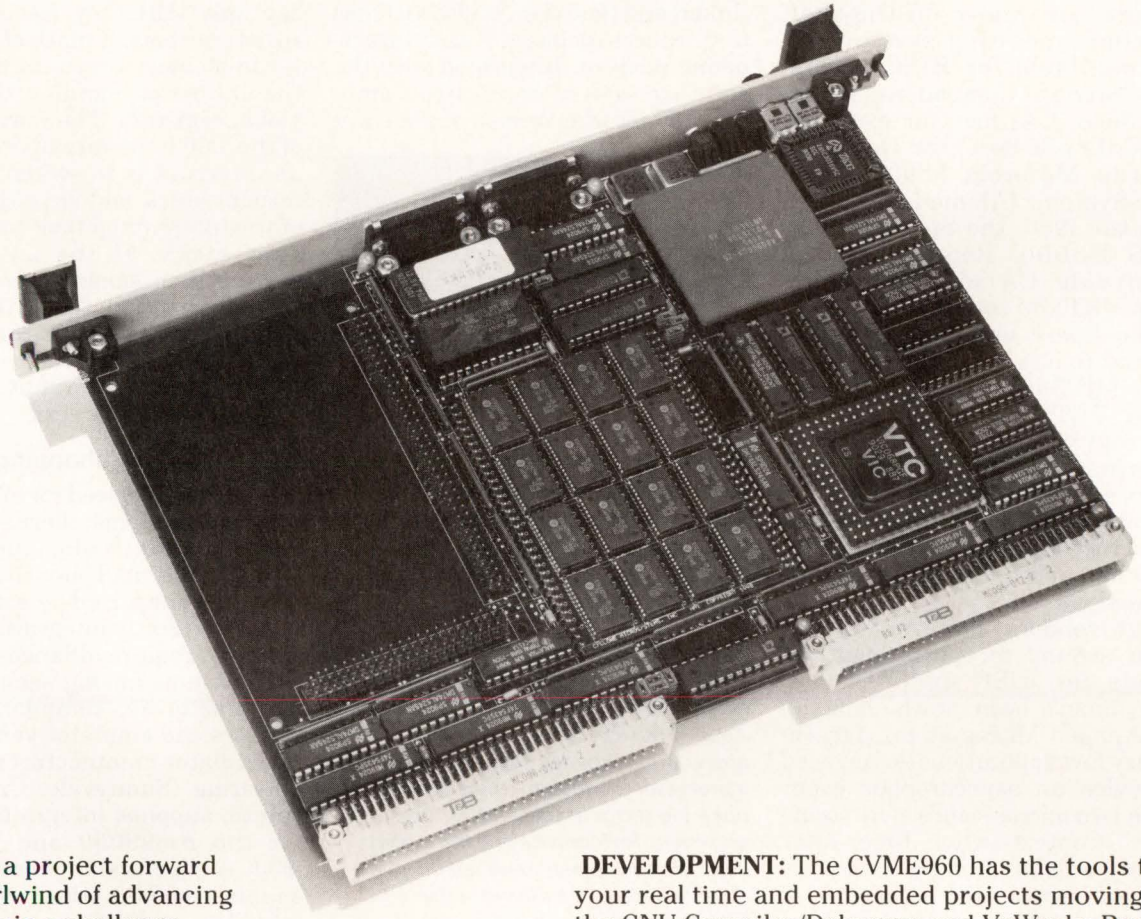

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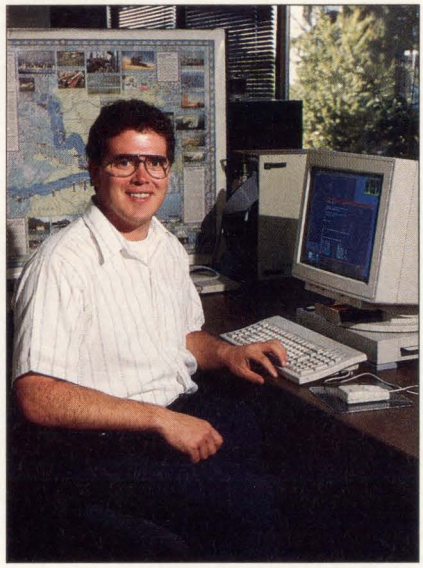
development at Applied Microsystems (Redmond, WA). This is especially true for processors such as the Intel i960, which require extensive start-up code (including tables) just for the chip to initialize itself. "The reason that you buy an off-the-shelf kernel is that everything is written down—the processes and procedures—and your applications people know how to call the required routines the day your project starts," Jensen adds.

There are many off-the-shelf real-time operating system kernels available for RISC processors. Software Components Group (San Jose, CA) has, for example, ported its pSOS+ to the Intel i960 and the Motorola 88000. Wind River Systems (Alameda, CA) supports the i960, the Sparc and the MIPS R3000. Ready Systems (Sunnyvale, CA) offers a version of its VRTX32 real-time executive for the Sparc architecture and is reported to be working on a version for the MIPS R3000. Ready has also ported VRTX32 to the Am29000, then sold the rights to Embedded Performance, which is working on enhancements. JMI Software Consultants (Spring House, PA) has ported its C Executive to the R3000, Am29000, and Sparc, as well as the i860 and the i960.

Most vendors, however, haven't gotten around to optimizing their kernels for RISC architectures. There hasn't been much demand, says Applied Microsystems' Jensen. "In very few applications do you need to service an asynchronous event within two microseconds of its occurrence." Context-switch time, after all, only affects interrupt latency—the time between the occurrence of an event and when the machine starts processing the interrupt.

Some operating system kernels are now being optimized for RISC. Jensen wonders, however, about the motives. "Are we doing this for technical purity or because our projects demand it?" he asks.

Embedded Performance is adapting VRTX32 to the Am29000 architecture, but in more ways than just context switching. "A real-time operating system for a CISC processor assumes a two-bus architecture," says EPI's Laengrich. "That means you should always be able to access your instruction memory via the data bus, which is important if you're going to access constants that reside in instructions." The Am29000 has a three-bus architecture, and unless there's a physical crossover link between data and instruction buses, "VRTX as written can't access constants contained in instructions," Laengrich observes. Making such constants accessible without the crossover hardware is one of the goals of EPI's enhancements to VRTX32 29000. Integration into EPI's EPIC 29000 toolset is another. The toolset consists of an optimizing C compiler, assembler, linker, and librarian. It also includes a C source debugger and target-debug monitor. Integrated with the software tools is an in-circuit emulator. The turbo version of the emulator can perform Am29000 or 29050 emulation up to 33 MHz (a 40-MHz version is in development).



Applied Microsystems' senior design engineer Brian Crowley says that whether a processor is a RISC machine or not is not a big factor in selection for design engineers. Performance and the availability of development tools are the prime considerations. "If a processor doesn't have tools, why touch it?" he says.

Compiler technology is essential in developing optimized kernels for RISC chips such as the Sparc. By using a compiler that follows the dedicated register window model, designers can build a kernel in which they can specify the tasks that will overlay with other tasks and the register windows to which the tasks will be dedicated. Of this approach Kirk says, "We're doing something in software to change the calling convention of the Sparc to make it more adaptable for real-time environments."

JMI's Ed Rathje, vice-president, agrees that the compiler is important. "Assembly language programming on RISC architectures should be avoided at all cost," he advises. "No human can keep track of the dozens (and in some cases hundreds) of registers. Delayed branches, to a programmer, are the Devil's invention."

JMI is trying to patent its proprietary porting of C Executive to the Intel i960. Officials there will say only that they use register-to register copies in place of the register-to-memory copies in the part of the interrupt handler that saves global registers. The normal action of the i960 hardware upon receiving an interrupt is to switch to the interrupt stack and save the context of the interrupted task to the interrupt stack. If the interrupted routine then causes preemption of the interrupted task, the kernel must copy the task's context to a task-specific memory location. Otherwise the interrupt would destroy the saved context.

One-stop tool shopping

But beyond the need for off-the-shelf operating systems, there's a need for development tools, specifically, tightly integrated ones that are supplied and supported by a single vendor. Such tightly integrated toolsets, however, require alliances and close partnerships among semiconductor manufacturers, compiler/debugger vendors and emulator vendors.

Emulator manufacturer Step Engineering (Sunnyvale, CA), for instance, supplies integrated toolsets for the Am29000 and the Intel i960CA superscalar processor. Step supplies combinations of its own compilers and debuggers as well as compilers and debuggers it offers under OEM licenses from Intel and Microtec Research. In another example of a strategic alliance, Step worked closely with Intel to develop its Express Plus and Express III i960CA emulators.

Ready Systems, in preparing its MIPS R3000 version of VRTX32, is also bringing over its entire Velocity development environment to support the R3000. Wind River's support of three RISC machines likewise includes the entire VxWorks environment. In addition, Applied Microsystems integrates and supports Microtec's C compiler and X-Ray debugger into the i960CA development system based on its

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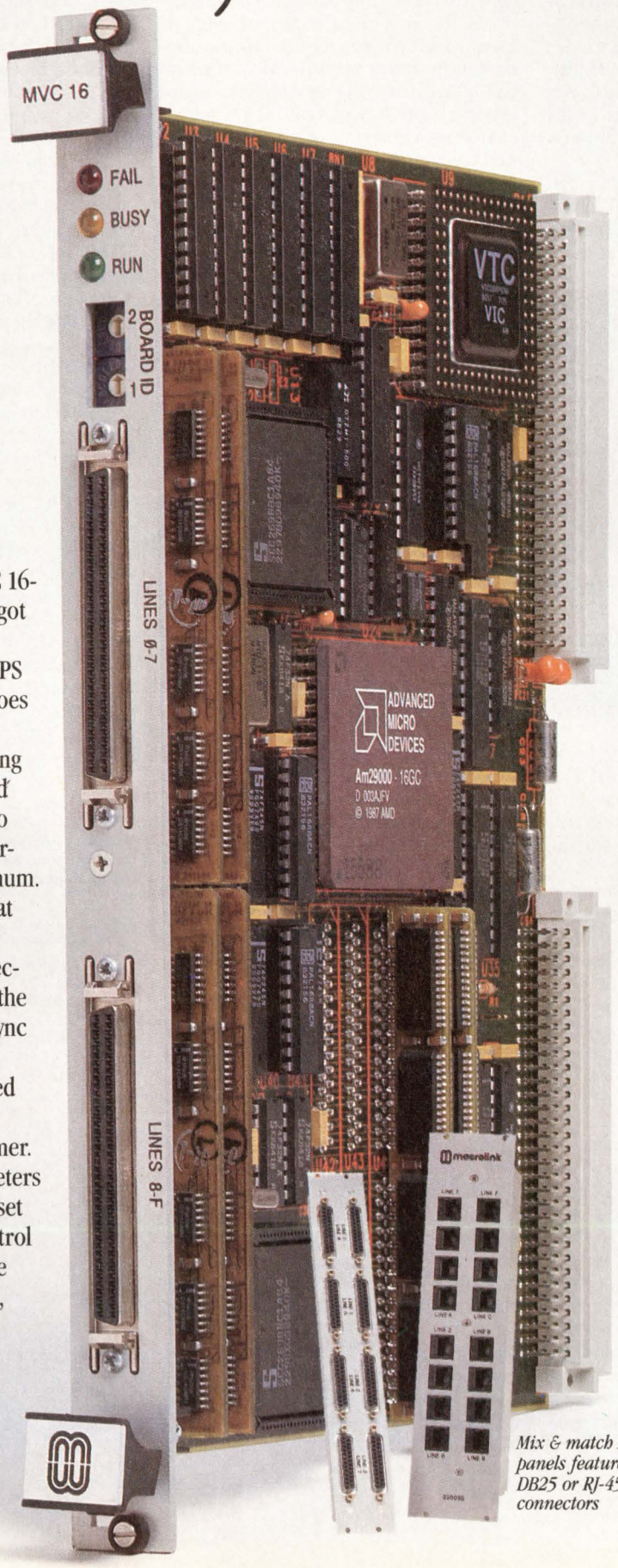

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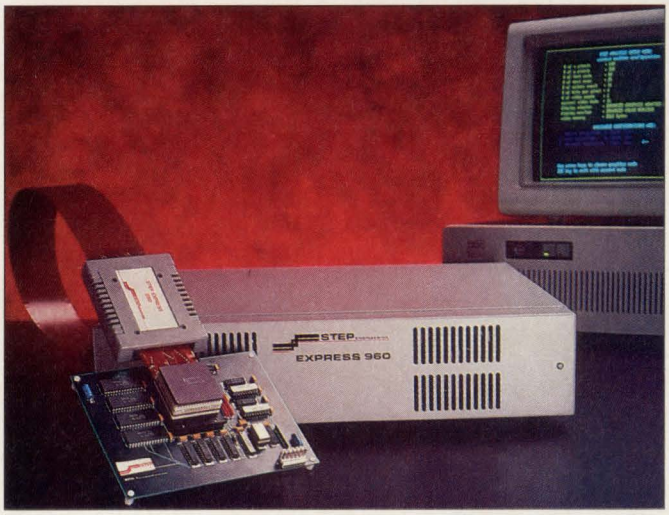
emulator. One of the major benefits of such an integrated set of tools is to shield the application programmer from the details of chip architecture. "Most software engineers today work in C, so they don't even see the machine," explains Brian Crowley, senior design engineer for Applied Microsystems and project manager for the i960CA development system.

The Applied Microsystems EL 3200/i960CA emulator, which is the product of Crowley's design team, uses a Motorola 68302 as a control processor. "RISC development tools are still new," says Crowley. "If I'm going to choose a RISC processor to do a real-time embedded system, I'm going to choose it for its performance, because I want to go fast. Otherwise I'd be better off using a 68020 or a 68030 because there are really mature tools on the market." Crowley is in a good position to see the point of view of both user and tool vendor. "We use our own tools to make new tools," he says, "and we're happily doing 68000 development on Sun Sparcstations."



Real-time development tools for RISC processors are rapidly becoming available. The Express Plus by Step Engineering is an emulator for the Intel i960CA superscalar processor which can run at up to 33MHz. The emulators are available with a selection of integrated compilers, debuggers and other development software.

Looking beyond the core

Beyond a direct comparison of various RISC architectures, the selection of a RISC processor can have significant effects on a system's cost and design. Because they run so fast, RISC processors require a larger memory bandwidth to keep them fed than do CISC machines. As performance is increased by running up the clock frequency, especially beyond 40 MHz, tricky board-design issues appear. What about peripheral devices included on 32-bit CISC microcontrollers like the 683XX family?

The fact that RISC is a newer technology and has not yet evolved the highly-integrated control functions that currently support CISC architectures figures in selection as well. It means that the processor must be supported by more peripheral devices on the board, making system hardware design more complex. "Embedded real-time comes down to more than just cache support," says Applied's Jensen. "When they're really attacking real-time, they have counter/timers on-chip, DMA setup, and peripherals you might need for dealing with outside world events."

Fortunately, it looks like RISC processors will be catching up in that arena as well. Specific designs aimed at real-time control are emerging, such as the R3001 and R3051 by Integrated Device Technology and the LR33000 family by LSI Logic (Milpitas, CA). The R3001 includes circuitry to control and lock external cache memory. The R3051 sports an on-chip table lookaside buffer for memory management, a clock generator, as well as data and instruction caches which can be used to lock time-critical routines into the fastest on-chip memory. The 3051 also includes read/write buffers, a DMA arbiter and bus interface unit. The LR33000 family includes models with various combinations of MMU, cache controllers, counter/timers and read/write buffers. Both IDT and LSI Logic supply extensive sets of development tools, including prototyping systems such as LSI Logic's Pocket Rocket evaluation board for the LR33000.

AMD has recently announced two new additions to its Am29000 family. The Am29030 and Am29035 include 4-kbyte and 8-kbyte instruction caches on-chip, and scalable clocking, which allows the bus to run at half the processor speed to help simplify board design. The Am29035 also has programmable bus sizing for 16- or 32-bit operation for systems with varying price/performance levels. EPI has announced development system support for the new AMD chips.

Whether designers will use RISC in real-time applications will depend more on product maturity than technical issues. Before they will choose RISC for real-time applications, designers will need to see more real-time operating kernels become available. They'll also be waiting to see to what extent these kernels will be optimized for RISC machines. Other pieces of the puzzle include a higher level of tool support and higher level of peripheral integration. Says AMD's Brett Stewart, "Customers don't choose processors because they are RISC or CISC. That's only of interest to the extent that they give superior system performance, superior system cost, superior time-to-market and an upgrade path."

RISC architectures certainly provide a leap in performance. It's only a matter of time until they mature to provide significant system improvements in all the other areas and become much more widely used by designers. ■

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Enhancing the performance of standard buses

Warren Andrews
Senior Editor

System designers must deliver the performance promised by advances in microprocessors and other integrated devices. To do this, they're working to upgrade existing buses to meet the demands of next-generation systems.

Translating semiconductor advances into equivalent gains at the system level often requires some engineering magic. Handling faster clock speeds, for example, requires special consideration of transmission-line effects and enhanced protection from signal cross-talk or interference. And keeping one-instruction-per-clock-cycle RISC processors supplied with data at a 40-MHz or greater clock rate can be a real memory-design headache.

If these difficulties aren't enough, semiconductor researchers are still working to boost the speed and shrink the geometries of semiconductor devices, but they haven't rescinded any of the laws of physics. They must still deal with the limits on signal propagation and the special requirements for driving capacitive loads. As a result, standard backplane/bus designs are still grappling with tradeoffs between power dissipation and levels of integration.

And there are always the issues of the bus standards themselves. Established standards such as VME, Multibus and STD Bus are slow to change. But engineers continue to work to boost the performance of standard buses while maintaining compatibility with previous generations. These efforts have resulted in a number of proposals, some of which have been welcomed by the vendor community while others have been shunned.

Moving standard buses ahead

Almost every major open-standard bus architecture has performance enhancements in the works. VME vendors have already made VME64 a commercial reality despite delays in making it part of the specification. And work is under way to add a number of other enhancements to VME including a noncompelled or source-synchronized, block-transfer mode, an open-boot PROM for auto configuration, and perhaps even a mechanism for hardware semaphores.

Not to be left behind, Multibus II vendors are working on a true hardware and software hot-insertion capability, stepping up the clock to double transfer rates, boosting the efficiency of the Message Passing Coprocessor (MPC) function with a more powerful processor, and extending the 21-slot system limit. STD Bus is also in on the act with a small group of vendors pushing to get acceptance for the 32-bit version developed by Ziatech (San Luis Obispo, CA). What's more, Ziatech has some multiprocessing software under development that could have a major impact on the acceptance of the 32-bit standard and system performance.

Even non-IEEE sanctioned buses have been looking to boost performance. SBus, for example, recently introduced a revision that increases the bus width from 32 to 64 bits. And IBM's Micro Channel Architecture (MCA) is on schedule in the series of upgrades which the company anticipates will end up with a 160-Mbyte/s bus. It's also rumored that the MCA competitor, EISA, has significant upgrades up its sleeve that will more than double bus-transfer speeds.

And, of course, Futurebus+ represents the ultimate in bus-performance enhancement. Still in the throes of final specification, Futurebus+ is expected to represent the fastest-possible bus architecture, limited only by semiconductor performance and the basic speed of electrons through conventional conductors.

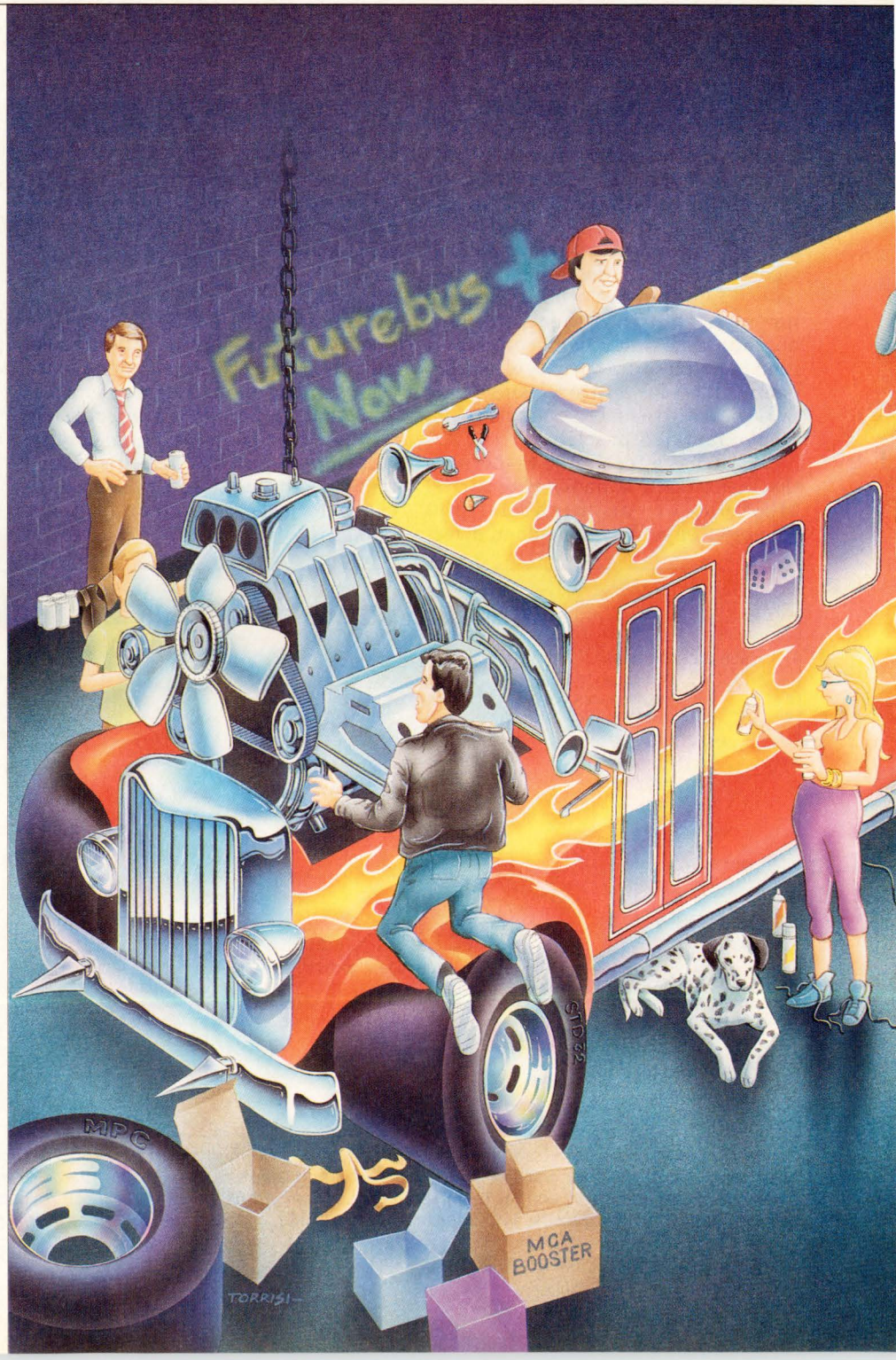
What price performance?

Despite one's particular opinion on whether developments in board products are pushed by technology

or pulled by demand, when higher performance is accompanied by a significantly higher price tag, lower-performance systems often win out. "There's only a certain percentage of OEMs out there that are looking for increased performance," says Bill Mahuson, vice-president of technology for Performance Technologies (Rochester, NY). "When we developed VME64," he says, "we knew that it would address only the small percentage of our customers who needed the extra performance. Additional enhancements such as SSBLT (source synchronous block transfer) will appeal to even a smaller number of users," he says.

"Right now we don't see the need for many full 32-bit systems, and that's why we offer only 16-bit CPUs now," says Ziatech vice-president, Jim Eckford from the STD perspective. But Eckford believes that as new applications for STD emerge—and new software to take advantage of full 32-bit transfers—demand for 32-bit parts will mushroom.

Similarly in the Multibus II world, no immediate need for increased performance is perceived. "We're looking at Multibus II enhancements because we know they'll be called for sometime in the



future," says Mike Richmond, Intel's product group Multibus manager. "But at present, Multibus II has no problem keeping up with—and in many cases it's ahead of—any of the applications it's used in."

VME directions

While the Multibus Manufacturers Group (MMG) has mapped out the future of Multibus II in some detail, VME makers are debating the next level of performance enhancements to append to the specification. "VME64 is a logical extension to the bus and, as incorporated in the current proposed Rev. D, represents a significant performance upgrade," says Mahuson. But some VFEA (VME-to-Futurebus Extended Architecture) International Trade Association members are anxious to cram as many additional enhancements into the latest revision as possible. The most desired enhancements are SSBLT, Open Boot and hardware semaphores (see "Semaphores and reflective memory," p 95). Other proposals dealing with cache coherency and message-passing protocols have been tabled for a future revision or will be addressed separately as "recommended practices."

"SSBLT is a technique to increase the basic VME transfer rate to 160 Mbyte/s—or as high as 200 Mbyte/s," says Wayne Fischer, director of strategic marketing for Force Computers, (Campbell, CA), (see "SSBLT: Raising the limits of VME64", p ??). "The VMEbus protocol has several delays built-in that simplified implementation during its early years. Now, however, high-speed, high-density VLSI and ASIC technology allow more advanced protocols to be used," he says.

In an SSBLT, the data source is also the source for the data-transfer clock, which runs at a rate that is negotiated between the source and receiver boards. In a way not yet specified, this negotiated rate will be determined at configuration time for each board. In an SSBLT transfer, the address phase is the same as a conventional VME block transfer. However, after the initial address is set up, the DTACK (Data Transfer Acknowledge) handshake is eliminated and data is free to be strobed across the bus at the data-source clock speed.

Agreeing on a rate

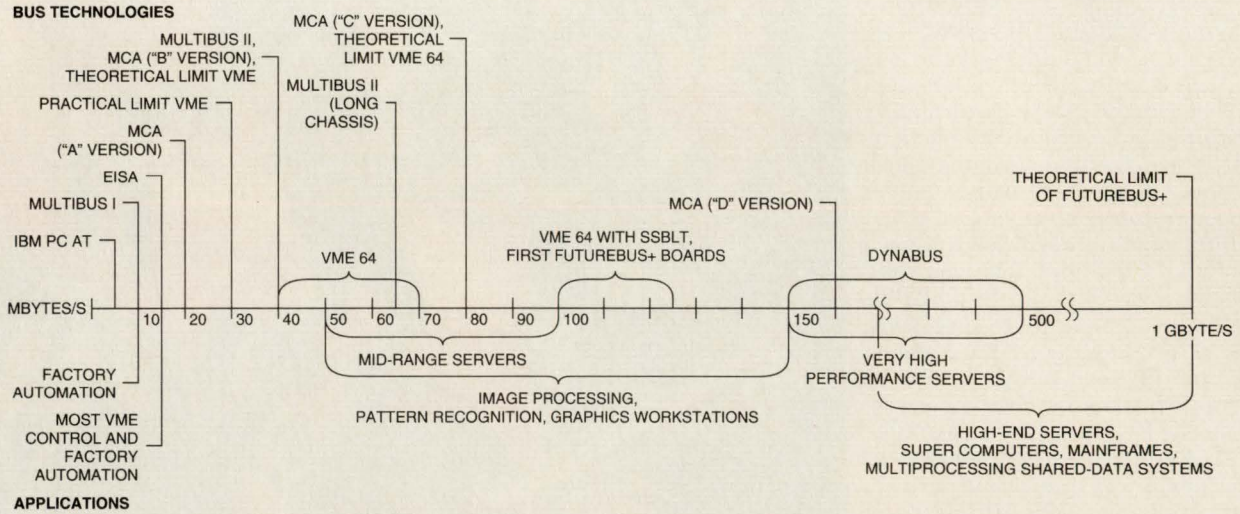
Secure transfer of the data is dependent on the fact that the transmitting and receiving node understand and agree on the transfer rate, and that the rate of transmission will be less-than or equal-to the receiver's capability. But this agreement on a negotiated rate may be easier for the boards than for their makers.

At presstime there seems to be three factions within the VME64 committee: one group doesn't want to alter the VME64 specification; one group wants the addition to the specification to be as simple as possible, hopefully garnering a broader usage; and the third group wants a far more-elegant solution, increasing flexibility and maximum transfer capability.

The major undecided issues facing the second two groups are transfer rate, block size, use of VME address modifiers, and the encoding of block length. The block length has been proposed as information to be put on the four least-significant bits of the address field. Because all transfers are on 16-byte boundaries, these lower four bits are not used and would be free to be used for block-length information.

Those board makers who are most opposed to the idea of incorporating SSBLT into Rev. D of the VME specification say that most applications do not need the higher transfer rate, and those that do will be better served by going off the VME system bus to some subsidiary, high-transfer-rate bus. They add that while SSBLT will increase transfer rates, it won't deliver enough improvement to serve most high-bandwidth applications. They conclude that SSBLT will only result in new—and potentially more troublesome—bottlenecks on the bus. (It

Standard bus technologies and applications



Today's standard buses serve the majority of applications for multiboard systems, but demand from users and the pressures of advancing microprocessor and semiconductor technologies are forcing the standards to evolve. The enhancements in the work for existing bus standards will let them serve more applications, particularly those demanding higher performance. And new bus standards, such as Futurebus+, will address the needs of applications at the highest end of the spectrum.

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also been pointed out that those most vocally opposing the addition have recently released—or are about to release—VME64 silicon. Almost any of the proposed SSBLT schemes would require significant redesign of that silicon.)

Another bottleneck?

Even many board makers showing tacit support for the SSBLT proposal are not completely convinced of its effectiveness. "The idea of increasing the transfer speed on VMEbus sounds desirable, but may serve only to frustrate designers with high-bandwidth applications," says Ed Schulman, vice-president of marketing for Ironics (Ithaca, NY). "Even VME64 doesn't begin to solve the transfer problems in high-bandwidth applications such as graphics and imaging," he says.

"There's nothing wrong with the idea of a source-synchronized transfer mechanism," adds Schulman, "we've been doing it for years." Ironics, he explains, has used the technique to increase transfer rates in its MCPL (Multi Crate Pipe Line) products and in some of its DMA mezzanine boards on its VME products. "Using the approach, we've been able to achieve some very high sustained transfer rates," say Schulman, "on products that have been commercially successful."

But Schulman is less than enthusiastic about putting SSBLT into the regular VME specification. "In applications where we've used the high-speed transfer rates, we've needed all the performance we could get. If we had to handle VMEbus system information and housekeeping on the same bus, we'd be in trouble," he says. For the same reason, Schulman believes that even VME64 may be pushing the limits of practicality.

SSBLT: Raising the limits of VME64

Source synchronous block transfer (SSBLT) is the latest idea for boosting the transfer speed of VMEbus. "I don't know exactly where the initial idea came from, but it seems to have come along at the right time and mates up nicely with the VME64 specification," says Heurikon's Clarence Peckham.

While no one may be certain who should get credit for the idea behind SSBLT (which began as the "non-compelled" mode), a number of individuals have been playing with the idea for some time. Kim Clohessy, vice-president and CTO of Dy 4 (Nepean, Ontario, Canada), was reportedly working on some similar—if not identical—technology for some of that company's military customers within the last year.

When it was formally introduced to the committee by chairman and director of internal marketing for Motorola's computer group, Shlomo Pri Tal, Force's Jack Regula, a hardware engineer, already had a paper in hand that fully detailed his approach to the faster transfer rates. Apparently, Regula had worked on noncompelled transfers at Ironics before moving to Force, and had proposed a similar approach to Ironics' management.

"SSBLT appears to be a technology whose time has come," says Performance Technology's CTO, Bill Mahuson. "But I'd hate to see us rush into drafting a spec without having it completely thought out and tested. For example, VME64 was thoroughly tested prior to bringing it to the world. Performance simulated, built and thoroughly tested VME64 prototypes. Thus, when the VFEA (VME-to-Futurebus Extended Architecture) VITA committee settled down to examine the specification, they were working with a known quantity."

With SSBLT, it appears to be a somewhat different scenario. Non-compelled transfers have been used for a number of years on proprietary buses, but always in cases where the end justified an unconventional implementation. Here, the SSBLT rules will have to be confined within the VME format. "Even though it hasn't been tested yet," says Force's Wayne Fischer, "we've done enough VMEbus design work to have a high level of confidence that it will work right off the bat."

"The ones who are too often not listened to in the inner spheres of the VME community are the customers," laments Synergy's Tom Powell. "Even without the complexity of VME64, customers still have difficulty in making boards of different manufacturers work together. Those problems still haven't gone away and SSBLT—particularly if further levels of complexity are included—will only aggravate the situation," he says.

However, those in support of the SSBLT proposal—which at this time seems to include the majority of VME vendors represented on the VFEA (VME-to-Futurebus Extended Architecture) technical committee of VITA—believe that a high-speed VME transfer capability would be valuable. "We have many applications, particularly in graphics, where SSBLT would be extremely valuable," says Abe Hirsch, marketing director at Heurikon (Madison, WI). "Many of our customers and potential customers are looking for a solution which will provide better performance than VME can offer now. In many cases, however, they have a major investment in VME software, and in other cases a large investment in the 6U form factor. They're not anxious to jump into something like Futurebus+ unless there are no other choices. VME with SSBLT has that extra bit of performance, yet lets board makers keep the best part of their VME platforms," says Hirsch.

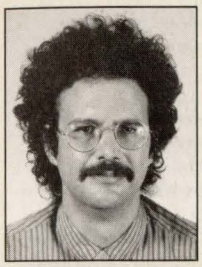
"Many VME users have large investments in VME boards they've developed. They aren't about to redesign these from scratch," says Tom Powell, vice-president of marketing for Synergy Microsystems (Encinitas, CA). Synergy has fully backed VME64 and was among the first to offer a 68040 CPU featuring VME64. But Powell is uncommitted in the case of SSBLT. While many of Synergy's customers are involved in graphics and imaging applications—areas calling for fast transfers of large amounts of image information—Powell, like Schulman, believes that in many cases it's better to offload the VMEbus from excessive data traffic and let mezzanine or secondary buses handle the high-speed traffic.

Block sizes

"Unquestionably SSBLT in some form will become part of the VME specification very soon," says Fischer. But exactly what it will look like may not be resolved at least until later this year, despite some efforts to railroad the specification through for passage by January 1, 1992. There are a number of proposals in the offing: one calls for simply a fixed block size, another for an unlimited block size, or for no encoding during the address phase.

In addition, various schemes for encoding block sizes have also been proposed. These include using a sep-

Semaphores and reflective memory



In any real-time and/or multi-tasking system, a significant amount of system bus bandwidth is used by processors repeatedly reading a location and waiting for some other processor to update that location (called spinning on a semaphore). This is the fundamental activity addressed by most resource-allocation and synchronizing protocols.

Numerous ingenious schemes have been devised to minimize or hide the performance penalties due to bus-bandwidth loss and latencies in semaphore updating. But one simple mechanism can satisfy the needs of semaphore handling in all systems, if all boards in a system adopt it.

The properties of a semaphore

Semaphore-based protocols are inherently synchronous to the receiving process, since it's the receiving process that determines when it inspects the state of the semaphore. With event-based protocols, events are issued by the sending process and by some means asynchronously announce their arrival to the receiving process (usually by an interrupt-based mechanism).

This difference gives rise to the main reasons for the popularity of semaphore-based protocols, because they are easier to validate (the receiver only changes its behavior, based on the received signal, at a known point and state in its execution), they are simpler to write, they do not have the context-switching overhead often associated with event-based protocols, and they do not have the problem of a limited number of available support mechanisms (most systems are limited in the number of interrupt sources which can be handled).

The penalty paid for these advantages is that typically for each "relevant" change of a semaphore (a write to it), there are many reads returning the same data each time until the change occurs. To reduce the bus bandwidth used by these reads, a "reflective memory" mechanism is used, which results in only atomic (indivisible) read/writes to semaphores appearing on the VMEbus, all normal reads being performed from a local copy of the semaphore and, therefore, not appearing on the VMEbus. This mechanism provides most of the practical advantages of cache coherence for the support of semaphores, at a fraction of the complexity and cost.

Reflective memory

A reflective memory is one which appears to be global but is actually local. In other words, every board in a system has a memory physically local to it (on-board), which "reflects" the state of all the other such memories in the system. Thus reads performed locally on any given location in this memory will return the same data as a read performed by another board's processor at the same location in its own memory. To achieve this, writes must never be made locally to this memory, but are always performed over the VMEbus, and modify all memories, including the initiator's memory, simultaneously and identically (this is known as an "inclusive" broadcast).

Using reflective memory

Since the reflective memories used to hold semaphores have special properties, they need to be uniquely identified and handled. This is done by defining a new address space, by AM encoding, for accesses to them. Since 32 kbytes reserved for semaphore locations should be more than adequate for any VMEbus system, this is an A16, D08(O) space (i.e., 32-kbyte semaphores for counting semaphore protocols, or up to 256,000 single-bit semaphores, the use of which is defined by system software). For ease of decoding, two previously reserved AM encodings, 0x21 and 0x25 are now specified as semaphore space. The two encodings have identical meaning, and AM2 need not be decoded.

Because all devices supporting the semaphore mechanism must respond to accesses in this space, a single master will write to multiple slaves. This requires a change to the definition of DTACK generation by addressed slaves. Since multiple slaves (including the slave function of the board containing the master) will respond, they will all assert DTACK (multiple drivers on a line is allowed on VMEbus, due to its open collector nature). To ensure that faster slaves do not terminate the cycle before slower slaves are ready, an extended minimum time from DSI reception to DTACK assertion of 100 ns is mandated for accesses in this space, and all slaves responding in this address space must be capable of capturing the data on the bus within this 100-ns period. DTACK release is irrelevant, since the slowest slave to release will control the state of the signal line seen by the master.

All boards supporting the semaphore mechanism should carry memory responding at an address within the semaphore address space, and extending contiguously upwards. If a board supports the semaphore mechanism, and the amount of memory it has in the semaphore address space, up to the maximum of 32 kbytes, must be made visible to system configuration software through the CSR mechanisms.

When software wishes to access a semaphore, it should read the semaphore using normal reads (which will be made from the local copy without acquiring the VMEbus). Once the semaphore is seen to be available, the software must perform an atomic read/write (RMC) to modify the semaphore. Both the read and write parts of this atomic access will appear on the VMEbus, ensuring that no other device can modify the semaphore between the time the first device saw it available and the time the device claimed the semaphore by modifying it. If the read part of the atomic read/write shows that the semaphore has become nonavailable since the last normal read, the write does not occur and the software should revert to reading its local copy of the semaphore until it again is seen to be available. The master interface therefore needs to distinguish between normal reads (which do not cause VMEbus mastership to be requested), and the read part of an atomic access (RMC) which is required to appear on the VMEbus. If normal reads to semaphore space are permitted (not for modifying semaphores, but as part of the mailbox-event mechanism described below), these must also appear on the VMEbus.

Thanos Mentzelopoulos, senior engineering group leader, Ironics

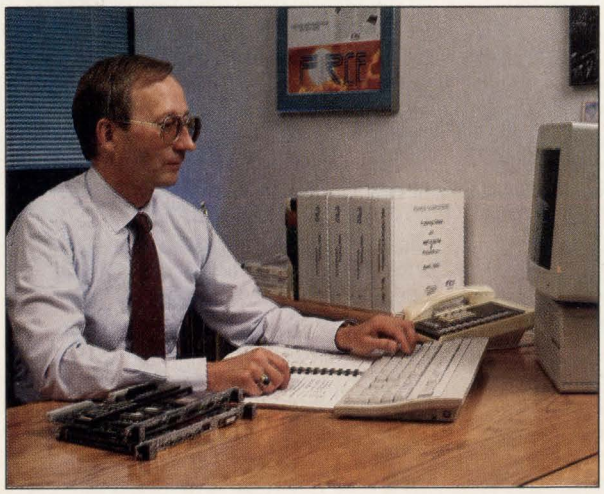
arate address-modifier code for each block size, using the data bus during the address cycle and using the lower four bits of the address to encode block length. "AM [address modifier] codes," says Fischer, "are limited because there are only six AM lines. The codes should be reserved for future VME64 extensions."

One early SSBLT proposal suggested reassigning AM codes currently used in VME64. This brought a chorus of outrage from almost the entire VME vendor community because most have already committed to the existing VME64 proposed specification. And the 32 data lines are used for A64 mode in VME64 and are not free for use in determining bus size, says Heurikon's vice-president of engineering, Clarence Peckham. While use of the lower four bits of the address lines might work, "this is something that is completely different from anything that's ever been done on VME," says Peckham. "It goes against the way the bus has been structured," he adds.

The remaining possibilities include using only one fixed data length such as 2 kbytes, or not including any transfer length during the address phase. "In the later case," says Fischer, "either a master or slave can terminate the transfer at any time. All transfers will remain on 16-byte boundaries and can be of any length within an A32 address space. Whenever the master or slave needs to refresh the address, or the master has transferred its packet of information, or the slave can no longer receive information, the SSBLT cycle is terminated."

Heurikon's marketing director Abe Hirsch (standing) sees a market demand that makes a high-speed transfer capability, such as SSBLT, very desirable for VME. The company's vice-president of engineering, Clarence Peckham (sitting), notes that a fixed block length version of SSBLT would have almost the same performance as a variable block length version, but reduce the complexity of building systems.

"Though a fixed length may not be the most efficient transfer mechanism, it eliminates a lot of problems of setting boundaries or, in the case of unlimited transfers, keeping the SSBLT transfer from hogging the bus," says Peckham. "Further," says Mahuson, "even though fixed-length transfers are less efficient than unlimited-length transfers, the overhead is small. The additional address phase needed to string transfers together requires only one or two bus cycles, resulting in as little as a 1 percent penalty." Mahuson adds that that's not much sacrifice to eliminate a lot of additional hardware and programming complexity.



Though many VME supporters agree on the value of the proposed SSBLT enhancement, not all agree on its form. One of its chief proponents, Wayne Fischer of Force Computers, hopes to see a version of the specification accepted that will allow variable length and variable speed block data transfers.

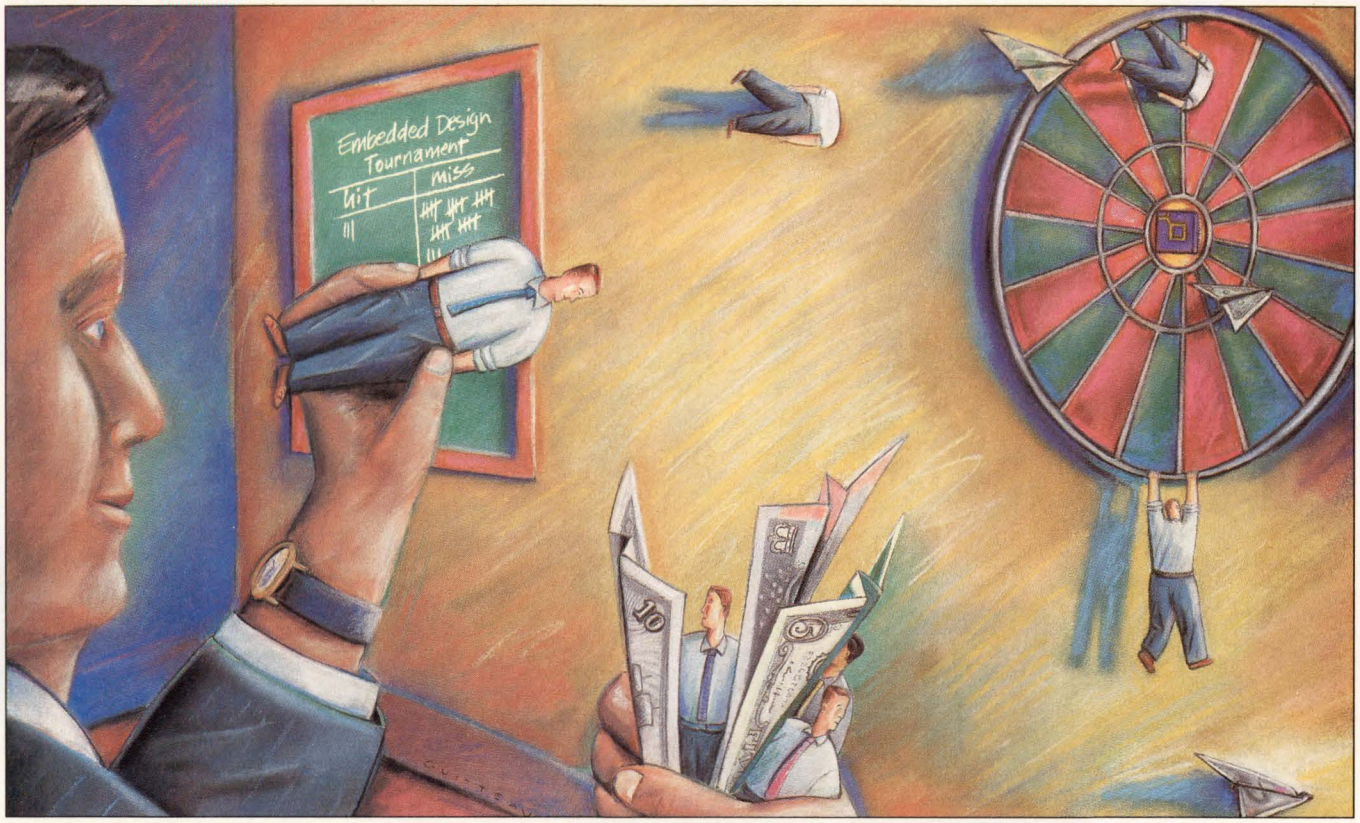
Similar issues arise with maximum transfer rates. The minimalists see no reason a fixed transfer rate can't be agreed on to essentially double the current VME64 rate. But others, such as Force's Fischer, opt for a variable rate where boards are set for their maximum transfer rate at configuration time. "This can be done via jumpers, or automatically when the VME community approves some kind of automatic configuration procedure such as Open Boot," says Fischer.

Fischer envisions a maximum cycle time of 50 ns (that translates to a rate of 20 Mtransfers/s) and a minimum of 30 ns. This range may be even lower as new backplane and transceiver technologies become available. "This approach may be fine for VME vendors that have full control of the system," says Mahuson. "However, OEMs that depend on a variety of manufacturers' boards may find some difficulty in making systems work. A single SSBLT transfer rate would at least minimize, if not solve, many problems," he says.

Another unresolved issue in the VITA technical committee is how to handle large transfers when the local bus on the destination node can't handle the flow of traffic. At least a pair of proposals for "throttling" data flow have been put forth, one using the VME64 Retry line, the other using both the VME64 Retry line and the standard VMEbus BEER (error) line.

Open Boot

Though debate is still raging on SSBLT, VITA's technical committee is also tackling other issues. The consideration of Open Boot is one more proposed addition to the growing Rev. D proposal. "The industry is going increasingly in the direction of auto configuration," says VITA technical director, Ray Alderman. He believes that with the increasing sophistication of the bus, some form of auto boot will be needed to con-



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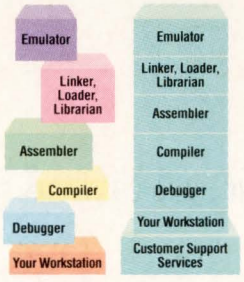

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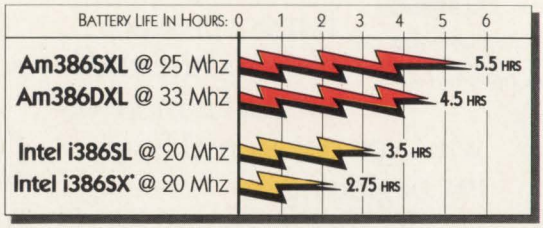

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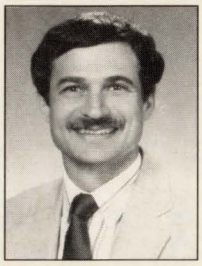


When intelligent I/O boards first appeared in industrial board-level products about a decade ago, they were not a new concept. Borrowing from the mainframe concept of dedicated channel processors, each board becomes an independent subsystem attached to an I/O channel such as Ethernet, FDDI (Fiber Distributed Data Interface), or serial communications. These "protocol engines" relieve the central CPU from low-level processing details as they stream data packets across the backplane. Another way to describe it would be "distributed I/O"—a form of multiprocessing, even though there may be only one CPU in the system.

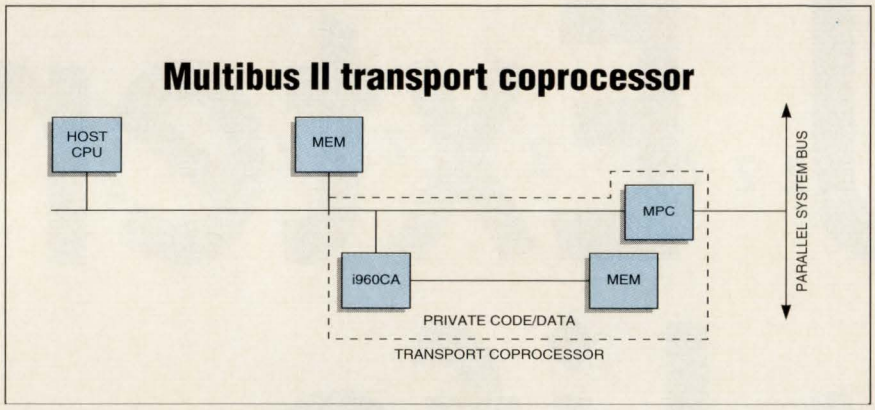
Multibus II is well suited for distributed I/O. The message-based architecture defines clients and server devices which carry out the clients' request. Client/server relationships are dynamic—at system boot time the MSA (Multibus System Architecture) firmware scans the backplane to see which modules are present and watches for boot server requests. Once clients are matched with servers, the system boots itself and becomes operational.

Message passing deals with the low-level functions of bus arbitration, packetization, byte ordering, and error handling. These services are provided by the operating system, or through message-passing libraries. Most programmers view the bus at the transport level, through a limited number of system calls. The Multibus II backplane thus becomes a very fast, very local, LAN, with up to 21 nodes per backplane segment.

Of course, there is a price to pay for all this elegance. The overhead of preparing these packets for transmission and reliably receiving them can be quite significant. In most cases the CPU handles this load, leaving fewer cycles for other processing tasks. The Transport Coprocessor (TPC) is designed to relieve the CPU of that burden.

The diagram shows how the bus interface, normally handled by the MPC alone, now becomes a subsystem which includes the i960 CA embedded controller. This controller was chosen because DMA transfer rate is usually the limiting factor in point-to-point message delivery time and the i960CA is capable of a maximum DMA transfer rate of 66 Mbytes/s. The controller can also handle other board level functions such as interconnect space (a series of configuration registers) and transport level services. Made practical by the relatively low cost of this device, the TPC subsystem improves communications throughput while conserving CPU cycles.

The data bears out this conclusion. An 80486-based processor board was designed to test the TPC theory. Compared to another Multibus II board which has no TPC, a communications-intensive benchmark program showed CPU utilization drop from 49 percent to only 5 percent for the TPC board. Message passing throughput was also improved by 20 percent because the i960 CA component is a fast superscaler RISC-based processor. The transport code runs faster on the i960 CA controller then it would on the 80486 processor, and the number of interrupts to the host CPU has been reduced.



With the addition of a Transport Coprocessor based on Intel's superscalar i960CA, the interface to Multibus II becomes a subsystem that includes local memory.

The first TPC based products are now available on Multibus II. Aeon Systems (Albuquerque, NM) has introduced a VAX processor board on a Multibus II form factor. "We took the TPC reference design offered by the MMG, and within two months we had a functional Multibus II board," says Steve Kadner, president of Aeon. The MMG also offers a transport source code module to its members.

Roger Finger, technical director, Multibus Manufacturers' Group

figure VME systems. "Without this capability, it will require specialized knowledge of the board and system configuration to even swap boards in a system. Open Boot will totally eliminate that problem and provide a smooth migration for combining VME with other systems such as Futurebus+," says Alderman.

While many agree with Alderman's basic idea, there's some sharp criticism of the particular Open Boot implementation being discussed as the potential standard. Open Boot, developed by Sun Microsystems (Mountain View, CA), encodes configuration information in a variant of the Forth language and embeds it in a small PROM. Sun has successfully implemented Open Boot on SBus cards, and the Futurebus+ committee is in the process of including it as part of the specification.

"This is clearly a case of the interests of Sun and other companies involved in Sun-compatible products coming before the good of the VME community in general," says Peckham. "I don't think that Open Boot should be in the specification at all. First of all, Open Boot is written in Forth and is very convenient for Sparc-based boards. Designers put-

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CIRCLE NO. 61

Multibus II timing

The factors involved in determining the bus clock rate in Multibus II are clock skew, setup-and-hold times of the MPC, bus transceivers and bus loss. Timing for the existing and proposed enhanced bus clock are illustrated in the results of a detailed timing analysis done by Taufik Ma, senior design engineer at Intel.

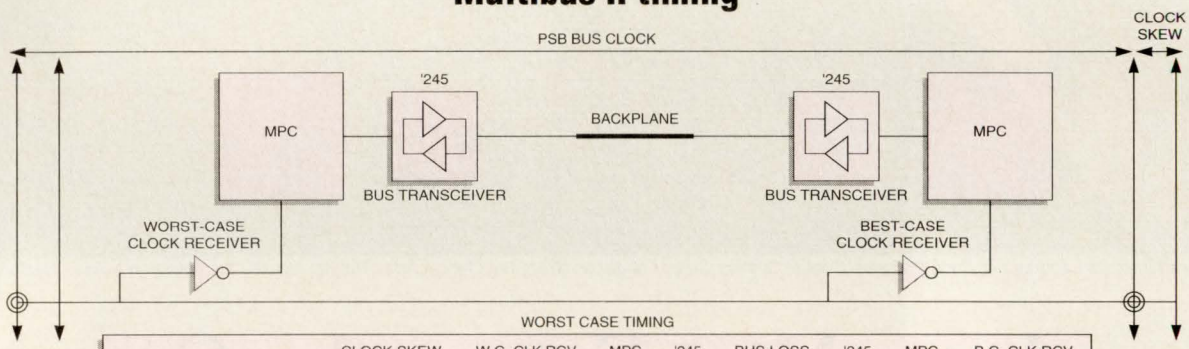
The clock skew is constant for both the existing and enhanced versions since the physical arrangement of the backplane remains the same. Similarly, the worst-case clock receiver buffer delays (4 ns) minus the best-case clock receiver at the other end (1 ns) result in 3-ns delays.

The MPC setup-and-hold times are the most critical since shifting to a 20-MHz clock immediately drops these times by almost half (from 29 to 15 ns). The net effect of this alone speeds up bus transfers by some 35 percent.

Next in consideration are the 74F245 bus transceivers which, as currently specified, provide a 7-ns propagation delay. A recently announced pin-for-pin replacement from Signetics that uses its Advanced BiCMOS TTL (ABT) version drops that delay to 4.6 ns. Additional savings are realized because bus loss is also minimized. The new transceivers have a strong internal pull-down resistor resulting in significantly faster high-to-low transitions. The faster transitions mean faster settling for the bus. As a result, the enhanced timing specification allows one transit time for bus-settling while the older specification called for a bus-settling delay of three transit times.

Totaled up, the savings in time allow for a 50 percent increase in bus speed. In a full 20-slot system this translates to an increase in clock speed to 16 MHz (assuming a radial distribution pattern) or a transfer rate of 64 Mbytes/s. For a card cage with only 10 slots, the resultant skew would be much smaller and the clock rate could easily be increased to 20 MHz, permitting data transfer at 80 Mbyte/s.

Multibus II timing



WORST CASE TIMING

	CLOCK SKEW	W.C. CLK RCV	MPC	'245	BUS LOSS	'245	MPC	B.C. CLK RCV
EXISTING SPECIFICATION:	5	4	29	7	25	7	24	-1
ENHANCED TIMINGS:	5	4	15	4.6	12	4.6	12	-1

This timing analysis of Multibus II compares the timing requirements for the existing and enhanced specification. The analysis considers the effects of best-case and worst-case clock receivers, and assumes the use of an improved bus transceiver for the enhanced configuration.

ting together 68000, MIPS or Intel-based boards have a problem. The Forth interpreter required puts you a year behind the Sparc pack and it doesn't solve any real problems. Not only is the Forth interpreter somewhat Sparc specific, but is pretty much lined up with Sun-OS. There's not another operating system that will work with Open Boot today," he says.

While there's strong opposition to Open Boot in some quarters, many within the VITA community believe that some form of configuration boot PROM should be implemented. On one side, these factions agree that with Open Boot, "Sun has done most of the homework and the VME community gets the advantage of this groundwork." On the other side, they agree with Peckham: "Open Boot may create more problems than it solves it the VME world. The perceived advantages of common device drivers and auto configuration are attractive, but would put non-Sparc-based system makers at a disadvantage."

Multibus II doubles rate

While the VME world is working on higher transfer rates, Multibus II supporters have also been busy. "Multibus II doesn't have the same bottlenecks as VME because its message-passing approach decouples the local processor from the backplane, letting transfers occur in noninterrupted packets," says Peckham. Thus all messages travel at the maximum speed of 40 Mbytes/s and, in all but severe cases, bottlenecks are eliminated. "But there are cases when even the 40 Mbyte/s rate isn't fast enough," says Peckham.

And while the MPC approach is intended to keep transfers running at close to the system's maximum rate, even the MPC can become a bottleneck. Len Schulwitz, executive director for Multibus Manufacturers Group, explains that there are cases when a card cage full of boards all want to send messages to a single CPU, taxing its MPC and

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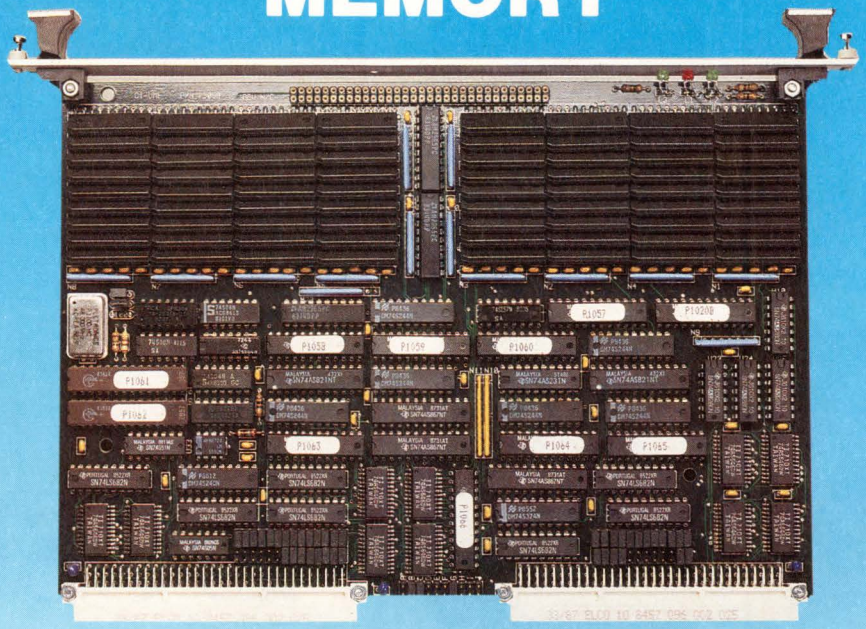

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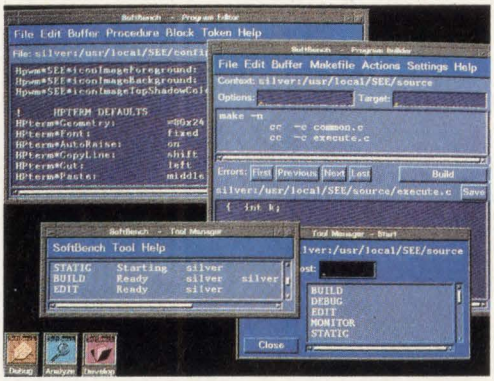

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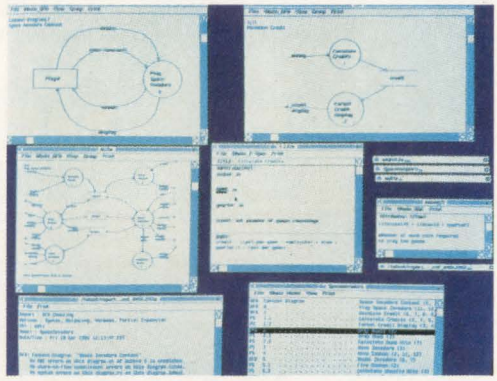

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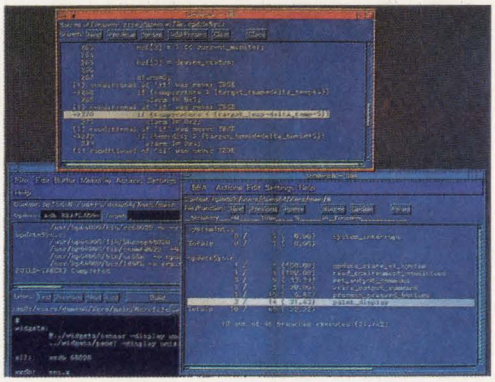

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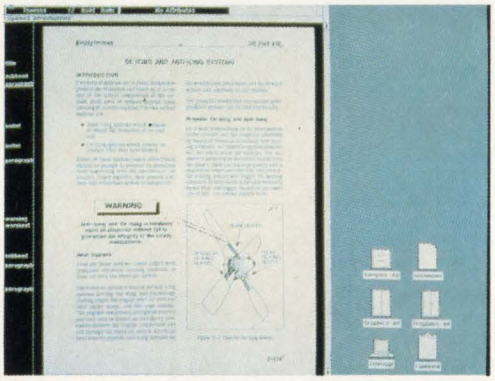

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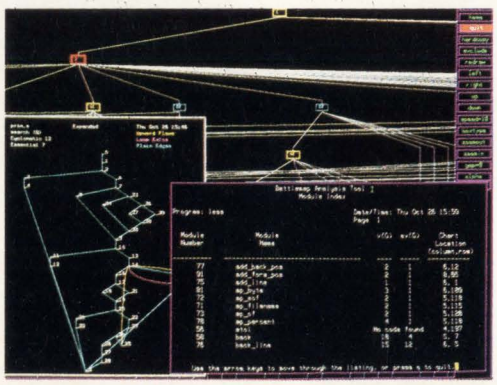

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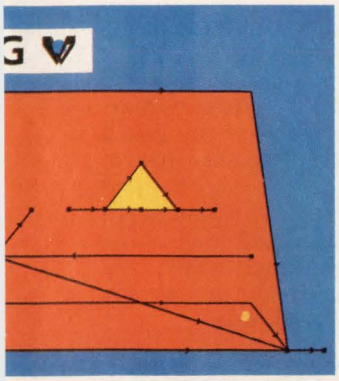

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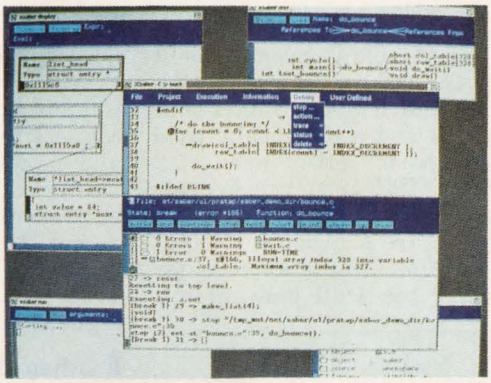

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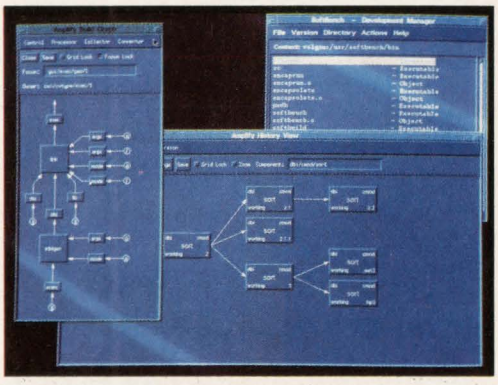

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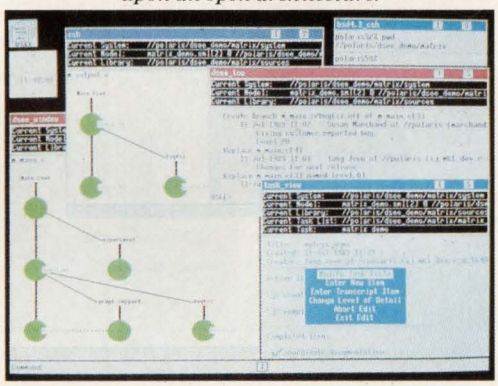

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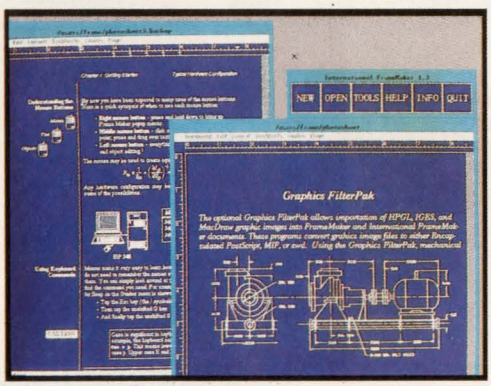

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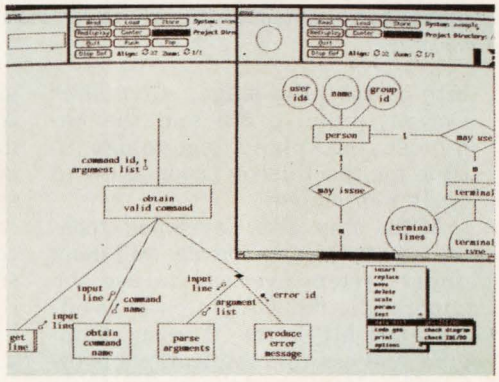

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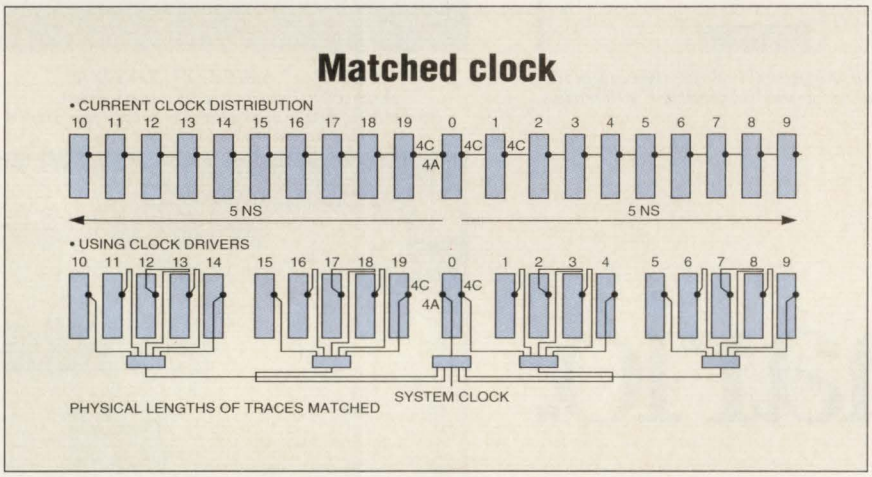
slowing system performance.

The MMG has addressed these potential shortcomings and others in a series of enhancements to the bus. The enhancements have recently been completed and are now undergoing testing. "We hope to have operating models of a system incorporating both the hot-swap (live insertion) capability (see "Multibus II hot-swap spec moves into prototyping stage," *Computer Design*, June, p 33) and the enhanced backplane technology in time for the Buscon trade show in early September.



Running bus-based systems at higher backplane speeds means tightly controlling bus timing. To reduce clock skew across a system backplane, the MMG has developed an enhanced backplane technology. The original clock distribution method (top diagram) used a single clock signal distributed to all boards from a central point, leading to a clock skew of 5 ns between boards only 10 slots distant. The enhanced backplane technology (lower diagram) uses two stages of clock drivers and balanced lead lengths to eliminate clock skew across the backplane.

MMG has also developed technology to allow boards suffering under system overload to use the superscalar i960CA processor to offload the MPC (see "Transport engine reduces communications overhead", p 100). In addition, the group has uncovered a technique that lets systems made up of multiple crates of boards transfer data between boards as if all boards were in the same crate.

20-MHz backplane

The key to Multibus II is the MPC which handles most of the bus transactions. The 78,000-gate ASIC comprises FIFOs, DMA control, buffer control, and a processor-independent interface. The chip was initially developed in a 2-μm technology providing ample latitude for a 10-MHz bus clock. "Earlier this year the MPC was converted to a 1-μm process to allow for a militarized version of the chip. A side benefit was that the smaller die was capable of running much faster. Subsequent testing revealed a significant yield of 20-MHz parts," says Finger.

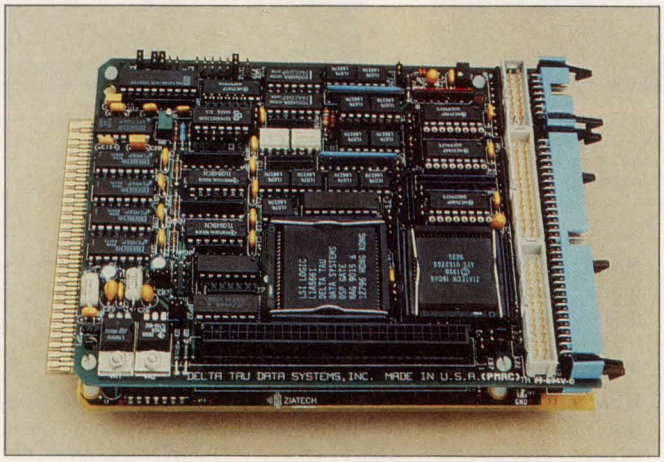
"A faster MPC doesn't necessarily translate into a faster bus clock rate—there are a number of other considerations. Nor does a faster transceiver by itself guarantee a significantly faster bus clock rate. Although at first glance it would appear that transfers can be easily speeded with a fancy transceiver," says Finger. But the actual transceiver, asserts Finger, is only one component in the overall processor-to-processor communication link, and it turns out, a relatively small one (See "Multibus II Timing," p ??). "All the talk about BTL (Backplane Transceiver Logic) in the Futurebus+ world can quickly lead designers to incorrect conclusions," he says.

"Obviously in systems where older 10-MHz boards are mixed with enhanced 20-MHz products, the clock has to operate at the lowest common denominator," says Finger. One proposal, to keep everything in harmony, is to use an interconnect register to store the speed and capability level of each board. During system reset, the central services module (CSM) would begin operating at 10 MHz. After checking the capabilities of each board, the CSM would then shift up to the highest possible clock rate.

Other contenders

While VME and Multibus II seem to be the main competitors in the race for the highest possible bus transfer rate, it's much more than a two-horse race. IBM (Armonk, NY), with its MCA (Micro Channel Architecture) has mapped out its game plan to increase the bus-transfer rate to 160 Mbyte/s, doubling it in stages from the original 20 Mbyte/s to 80 Mbytes/s using burst-mode techniques similar to those of VME. First, it developed its data streaming mode (modified block transfer) to increase transfer rates to 40 Mbytes/s. Then it used the address lines to effectively increase the bus width to 64 bits, doubling the transfer rate again to 80 Mbyte/s. In its next move to enhance the bus' transfer rate, IBM plans to halve the cycle time from 100 to 50 ns, doubling again the maximum possible transfer rate to 160 Mbytes/s.

In the STD arena, a handful of STD board makers have rallied behind Ziatech's STD 32 proposal which uses a clever connector arrangement to make 32-bit boards fully compatible with the earlier



This motion control board uses Ziatech's EISA-based STD 32, a proposed enhancement to the STD standard. The proposal includes a connector arrangement that makes its 32-bit boards compatible with the older STD 80, 8-bit specification.

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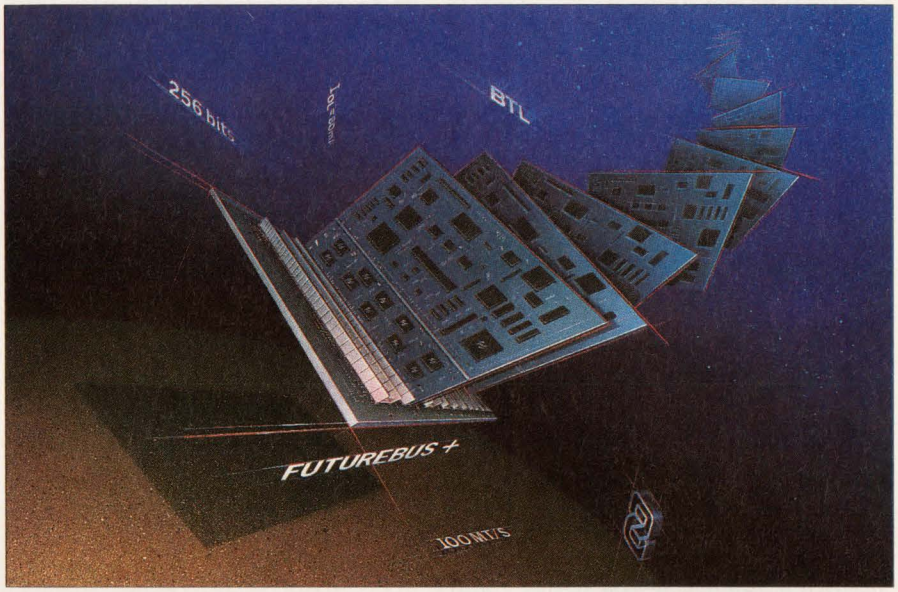

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STANDARD BUSES

STD 80, 8-bit specification. Many of the traditional STD board makers haven't followed the lead of what is now called "Task Group 32" because earlier versions of multiplexed 16-bit STD cards are incompatible with the newly proposed 16- and 32-bit specification. At this time, neither the older 16-bit or Ziatech's 32-bit versions have been blessed by the IEEE or the STD Manufacturers' Group.

But STD 32 is slowly gaining acceptance in a number of areas, according to Ziatech's Eckford. "One of the strong points is that the spec is based on the EISA specification and incorporates the standard EISA chip set," says Eckford. This allows full compatibility with EISA-based software, as well as the future promise of multiprocessing." Ziatech will soon release a multiprocessing version of DOS that will operate in the EISA environment, according to Eckford.

"We expect this to bring a significant number of applications into the STD camp that are looking for a less expensive or smaller form factor than VME. It will also address the needs of current STD or ISA users that need to add multiprocessing capabilities to their designs," Eckford says.

And in this corner...

Waiting eagerly in the wings, and sporting full cache coherence, message passing, packet mode, and transfer capability up to a Gbyte/s is Futurebus+. Alternating between moments of rapture and despair, ardent Futurebus+ supporters still don't have any commercial hardware or software to point to. Though it's broadly rumored that a number of bids for "A" profile boards have been circulated, there's been little industry acknowledgement that such products will be made and delivered this year. Nor is there any confirmation of the magnitude of these bids (rumored to be worth almost $50 million).

But despite what might seem to be setbacks, true believers continue to hammer out the specification in excruciating detail. "There are now so many options and choices that it's really going to be very difficult to determine exactly what Futurebus+ is," says Heurikon's Peckham. Other critics deride the emerging bus as being too expensive, too slow to emerge and having too many options and profiles for it to realize a critical mass of supporting board vendors.

Other factors are also expected to erode the future impact of Futurebus+. The emergence of multichip modules (MCMs)—compact processor/memory management/cache subsystems—will permit large multiprocessor systems to be implemented on a single VME or Multibus II card. In many applications, this will eliminate the need for extremely fast transfers and cache coherency on a standard backplane bus. Early Futurebus+ boards are expected to be developed on the hard metric format resulting in a 300×300mm board. But many OEMs have significant tooling investments in the form factor of VME and/or Multibus II.

But there will be those demanding applications that won't be satisfied with anything short of Futurebus+. To its credit, the Futurebus+ committee has created the ultimate in bus enhancements. When it's through, there will probably be little left for future generations of bus designers to modify. When it's called up for its mandatory review five years after final acceptance, the committee may well look at the Futurebus+ spec and say, "there's nothing to add." ■

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Postscript

For engineers, faster is never fast enough, and better is never good enough. Almost as soon as a new product or idea surfaces, there's a consortium of engineers out there to improve it. And this certainly has been the case recently with open-standard buses.

While I applaud the efforts to continuously improve bus performance, there are at least two major cautions that must guide these. The first is that vendors and OEMs do not attempt to force irrelevant technology on their customers. The second is that the fundamental concepts of interoperability of open buses be preserved.

In reviewing the progress of enhanced buses for this article, it seems that both of these cautions are being ignored to some extent. The open bus business is growing. It's likely to become a major base of technology development in this country. But developing bus technologies in an ivory tower, failing to pay attention to customers' real performance needs, and ignoring the requirement for backward compatibility could deliver this market into foreign hands.

In the early 1980s U.S. semiconductor manufacturers were broadly leading the industry in the development and manufacture of dynamic RAMs. In their rush to the latest and greatest technology, the fastest access times, the most elegant processing and cleverest architectures, U.S. vendors neglected their most important asset, their customers. The rest, of course, is history.

If the standard board industry makes it too difficult to follow standards, provides too many standards to follow, or dilutes the efficiency of using a standard bus by offering too many "options," it too may suffer from fatal elegance.

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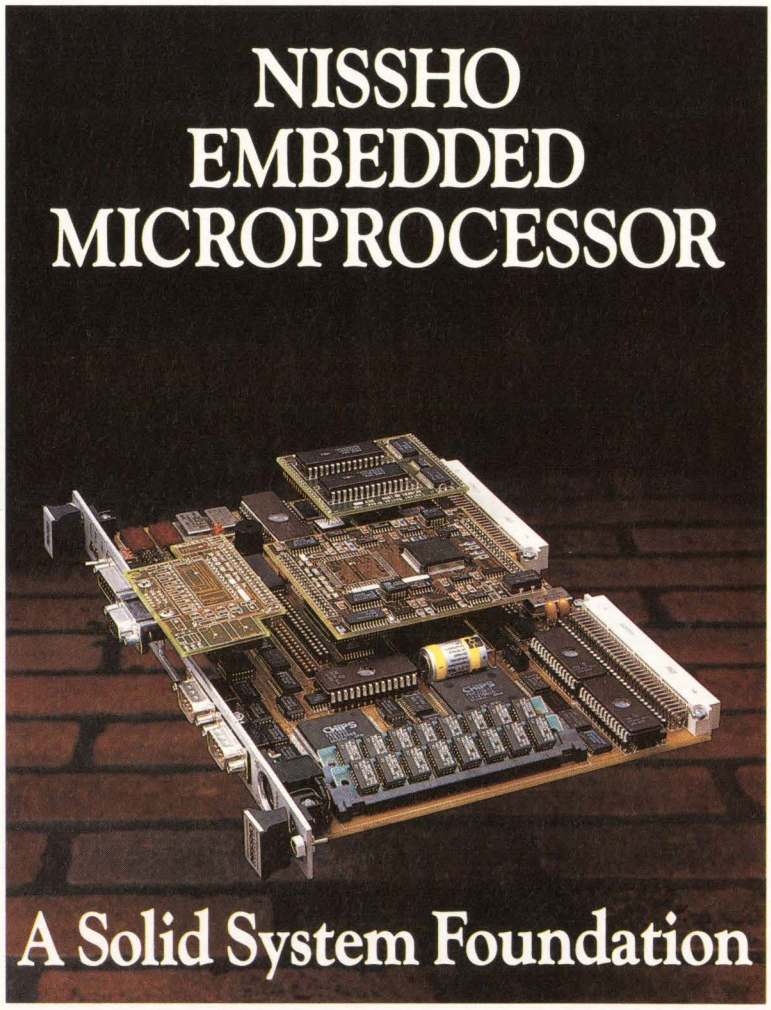

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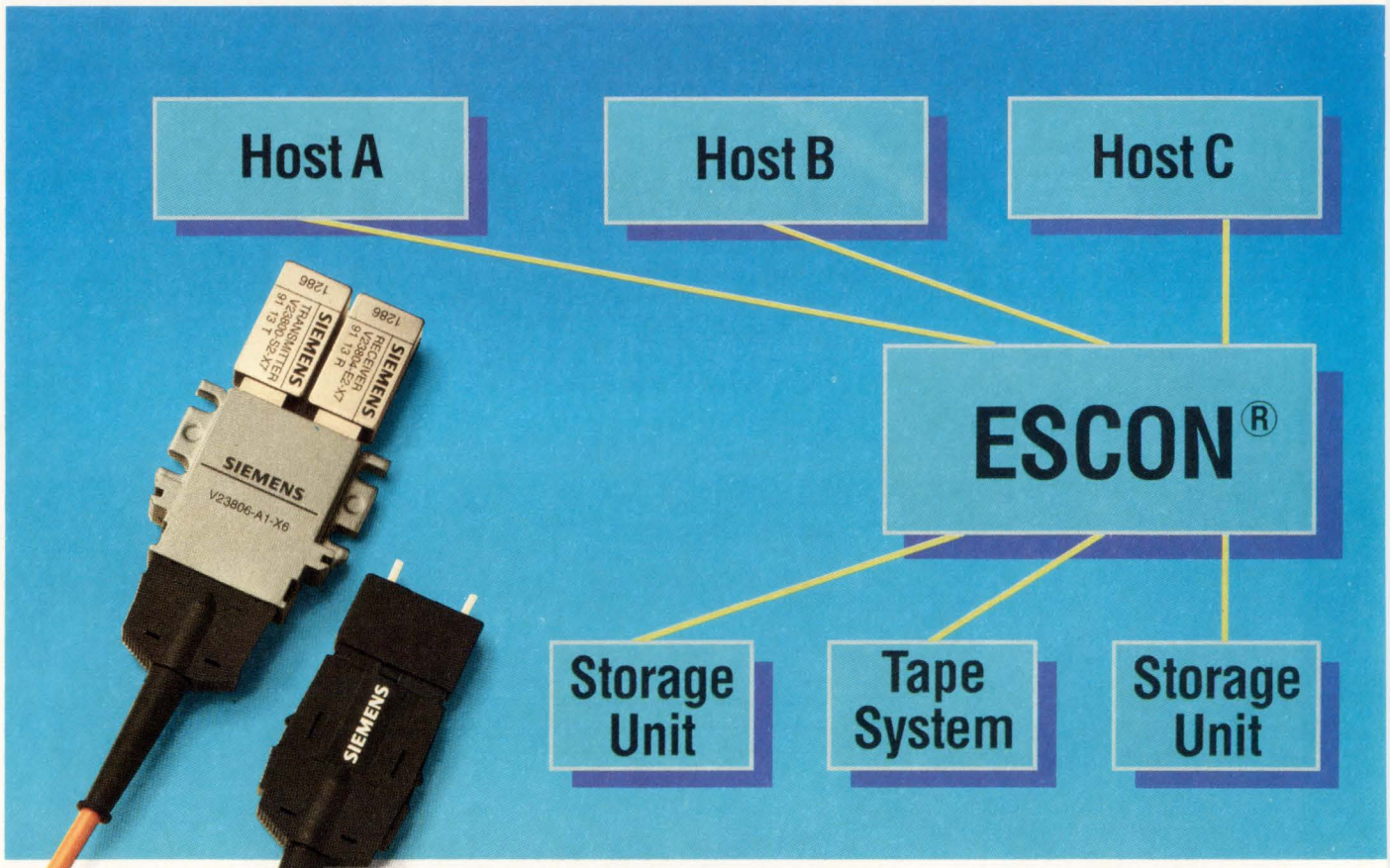

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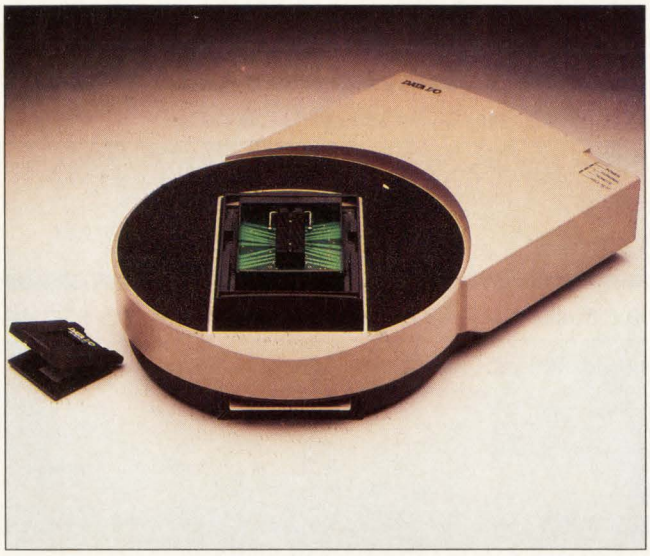
Jeffrey Child, Associate Editor



Built to handle problems associated with high-speed devices, Data I/O's 2900 universal device programmer features test and debugging aids that address problems such as ground bounce. The 2900 integrates pin-driver circuitry into a few ASICs, allowing for a much smaller, portable system.

There's a universe of programmable devices available to system designers these days. In this universe there are a dizzying array of programmable logic devices, field-programmable gate arrays (FPGAs), microcontrollers, EPROMs, and EEPROMs. The sheer number of devices, especially PLDs, poses problems for device programmer manufacturers, who must keep up with the of package types, architectures, speeds and pin counts of all the latest products.

Because it's impossible to predict which devices will be needed for the next design, it's vital that designers choose a programmer to suit both their current and future needs. They need to find a programmer that accommodates all the device types used in their designs, especially if they want to use the latest and greatest chips on the market. In the near future, if designers anticipate using new devices in the design, they must consider how the programmer is updated and how frequently the vendor provides those updates. Another consideration will be how the programmer handles the package types that the new chips will be in.

The challenge for device programmer vendors is to meet changing needs of designers, while staying on top of the proliferation of new devices and new packaging styles. They're striving to meet designers' demands for a reliable programmer that's as universal as possible. The best programmers can send any number of signals and programming voltages to any pin on a device. To accomplish this, programmer vendors are employing sophisticated hardware and software technologies. Such solutions are making programmers more expensive to build. As programmers get more complicated to make, programmer vendors are facing pressure from customers to keep their prices down.

The challenge for device programmer vendors is to meet changing needs of designers, while staying on top of the proliferation of new devices and packages.

Choosing a device programmer is further complicated by two trends. First, the emergence of low-cost, PC-based programmers selling at prices that are hard to resist. This trend has stirred up some debate, however. While some PC-based programmers are well-designed, several others are very cheaply made and not very reliable. Second, there's a trend toward the use of in-circuit programming. Once only used in military applications, in-circuit programmers are becoming cost-effective for commercial users. By allowing chips to be programmed right on the board, the problem of handling different packaging styles is avoided.

Cheaper isn't better

As the accompanying chart shows, a significant number of device programmers are not stand-alone systems. The programmers require an interface board that plugs into the card slot of a PC-compatible computer. By using processing power and memory to replace some of the electronics necessary to program a device, the programmer's building cost is reduced. While this approach makes a lot sense, a problem arises when designers of PC-based programmers try cut costs in other ways. Many designers try to cut corners on software, according to Barry Clarke, senior applications engineer at Stag Microsystems, (Santa Clara, CA). "Many of them don't take into account the different speeds of various PCs. The timing of the programming pulses depends on the speed of the PC on which the software is running," says Clarke. If the timing is off when programming an EPROM, for example, it can appear to be programmed, and will pass the in-program verify, but its cells may become overstressed during the programming process. This can dramatically reduce the device's lifetime to only a few months.

But PC-based device programmers are not all bad. The well-designed ones take the speed variations into account, according to Clarke.

Model	Devices supported	Maximum device pins	Package types supported	Tests (see key)	Maximum memory (bytes)	Upgrade method	Stand alone operation	Price	Comments
Actel 955 E Arques Ave, Sunnyvale, CA 94086 (408) 739-1010									**Circle 301**
Activator 1	FPGAs	84	LCC, PGA, QFP	B, TV	—	floppy	no	$1,500	optional diagnostics and debugger
Activator 2	FPGAs	176	LCC, PGA, QFP	B, ST, TV	—	floppy	no	$4,000	same as above, programs 4 FPGAs simultaneously
Advin Systems 1050 E Duane Ave, Bldg L, Sunnyvale, CA 94086 (800) 627-2456									**Circle 302**
Pilot-U24/28/32/40/84	EEPROMs, EPROMs, flash, GALs, µCs, PALs, PEELs, PLDs, PROMs	84	DIP, LCC, PLCC, SOIC	B, C, P, RI, ST, TV,	unlimited	floppy, modem	no	$995-$2,995	industrial grade, qualified by AMD
Pilot-I42/43/44/45	EEPROMS, EPROMs, flash, µCs	40	DIP, LCC, PLCC, SOIC	B, ST	unlimited	floppy, modem	no	$495-$795	same as above
Pilot -G/G/GCE	EEPROMs, EPROMs, flash, GALs, PALCEs	32	DIP, LCC, PLCC, SOIC	B, ST, TV	unlimited	floppy, modem	no	$495-$795	same as above
Altera 2610 Orchard Pkwy, San Jose, CA 95134 (408) 984-2800									**Circle 303**
PL-ASAP	EPLDs	208	DIP, JLCC, PGA, PQFP, SOIC	B, ST, TV	2M	floppy	no	$1,995	PC-based programmer for Altera EPLDs, socket adapters optional
American Reliance 9952 E Baldwin Pl, El Monte, CA 91731 (818) 575-5110									**Circle 304**
9820	EEPROMs, EPROMs, PLDs	28	DIP	B, RI, ST, V	72k	—	yes	$1,495	gang programmer, PC remote option
9850	EEPROMs, EPROMs	28	DIP	B, RI, ST, V	64k	—	yes	$395	built-in UV-eraser option
9860	EEPROMs, EPLDs, EPROMs, GALs, PLDs, PROMs, µCs	40	DIP, LCC, PLCC	B, TV, V	1M	floppy	no	$995	—
BYTEK 543 NW 77th St, Boca Raton, FL 33487 (407) 994-3520									**Circle 305**
Multitrack-4000	EEPROMs, EPROMs, µCs, PLDs	94	DIP, PLCC, QFP, TSOP	B, ST, TV	64M	floppy	yes	$4,995	programs up to 32 devices simultaneously, RS-232 and parallel ports
135H-E	EEPROMs, EPROMs	40	DIP, PLCC	all (except TV)	4M	firmware	yes	$1,495	supports 8-, 16-, and 32-bit data paths, RS-232 and parallel ports
135H-U	EEPROMs, EPROMs	88	DIP, PLCC	all	8M	floppy	yes	$2,495	same as above
Gangsite	all	32	DIP, PLCC	all	2M	firmware	yes	$995	Gang and set duplicator, RS-232 port
145H-AD/C	PLDs	88	DIP, PLCC	all	4M	floppy	yes	$1,995	universal, RS-232 and parallel ports
145-AD/E	PLDs	88	DIP, PLCC	all	4M	floppy	yes	$2,695	same as above
145H-BP	bipolar PROMs	88	DIP, PLCC	TV	4M	floppy	yes	$1,795	same as above
EZ-KF	EEPROMs, EPROMs	44	DIP, PLCC	all (except TV)	2M	firmware	yes	$995	RS-232 and parallel ports
EZ-C3	EEPROMs, EPROMs	32	DIP, PLCC	all (except TV)	2M	firmware	yes	$495	RS-232 port
Data I/O 10525 Willows Rd NE, Redmond, WA 98052 (206) 881-6444									**Circle 306**
UniSite	all	188	DIP, JLCC, LCC, PGA, PLCC, SOIC, QFP	B, ST, STT, TV	8M	floppy	yes	$9,995	—

Key: AI = auto identify; B = blank; C = continuity; ESD = electrostatic discharge; IB = illegal bit; MV = marginal verify; P = parametrics; RI = reverse insert; SST = silicon signature test; ST = self test; STT = structured test; TV = test vector; V = verify

Model	Devices supported	Maximum device pins	Package types supported	Tests (see key)	Maximum memory (bytes)	Upgrade method	Stand alone operation	Price	Comments
Data I/O 10525 Willows Rd NE, Redmond, WA 98052 (206) 881-6444									**Circle 306**
2900	FPGAs, memories, µCs, PLDs,	44	DIP, JLCC, LCC, PGA, PLCC, QFP, SOIC	B, ST, STT, TV	2M	floppy	yes	$3,750	—
BoardSite	memory, µCs, PLDs	—	custom adapters	B, ST, STT, TV	8M	floppy	yes	$13,995	—
Digelec 20144 Plummer St, Chatsworth, CA 91311 (800) 367-8750									**Circle 307**
934	EEPROMs, EPROMs, µCs	40	DIP, PLCC	B, IB, RI, ST, V	2M	firmware, floppy	yes	$1,495	RS-232 port
928 Gang Programmer	EEPROMs, EPROMs	40	DIP, PLCC	B, IB, ST, V	4M	floppy	yes	$3,495	RS-232 port, PC remote option
Eden Engineering 12505 Loma Rica Dr, Grass Valley, CA 95945 (916) 272-2770									**Circle 308**
XP-386-20	all	40	all	all	PC memory	floppy	no	$1,295	—
XP-386-28	all	40	all	all	PC memory	floppy	no	$1,775	—
XP-386-40	all	40	all	all	PC memory	floppy	no	$2,495	high-speed pin drivers
Elan Digital Systems 538 Valley Way, Milpitas, CA 95035 (800) 541-3526									**Circle 309**
3000	EEPROMs, EPLDs, EPROMs, flash, GALs, µCs, PALs, PEELs,	88	CDIP, DIP, LCC, PGA, PLCC, QFP, SDIP, TSOP	B, IB, P, ST, TV, V	2M	firmware	no	$995	—
5000	same as above	88	same as above	B, IB, P, ST, TV, V	2M	firmware	yes	$1,495-$2,395	batch modes, in-circuit programming
1000	same as above	88	same as above	B, IB, P, ST, TV, V	2M	firmware	yes	$2,995-$3,595	supports bipolar PROMs
Logical Devices 1201 NW 65th Pl, Fort Lauderdale, FL 33309 (800) 331-7766									**Circle 310**
Allpro 4i	EPROMs, µCs, PALs, PLDs	40	DIP, PLCC	B, ST, TV	PC memory	floppy	no	$1,295-$2,495	D-A converter per pin, RS-232 port
Allpro 88	EPROMs, FPGAs, µCs, PALs, PLDs, high-density PLDs	88	DIP, PLCC	B, ST, TV	PC memory	floppy	no	$3,995-$8,995	same as above
Allpro 88XR	same as above	88	DIP, PLCC	B, ST, TV	8M	floppy	yes	$12,995	D-A converter per pin; RS-232 and parallel ports; optional keyboard, monitor, hard drive
Oliver Advanced Engineering 320 W Arden St, Glendale, CA 91203 (818) 240-0080									**Circle 311**
Omni	all	128	all	B, IB, P, ST, TV, V	32M	floppy	yes	$6,395-$14,995	optional ESD, MIL-spec margin test, and AC test
Promac/United Exporters 1095 Market St, Suite 701, San Francisco, CA 94103-1630 (415) 255-9393									**Circle 312**
Promac P2	EEPROMs, EPROMs, µCs	28	DIP	B, MV, RI, ST	512k	firmware	yes	$1,195	menu-driven remote control, serial and parallel ports

Key: AI = auto identify; B = blank; C = continuity; ESD = electrostatic discharge; IB = illegal bit; MV = marginal verify; P = parametrics; RI = reverse insert; SST = silicon signature test; ST = self test; STT = structured test; TV = test vector; V = verify

Model	Devices supported	Maximum device pins	Package types supported	Tests (see key)	Maximum memory (bytes)	Upgrade method	Stand alone operation	Price	Comments
Promac/United Exporters 1095 Market St, Suite 701, San Francisco, CA 94103-1630 (415) 255-9393 **Circle 312**									
Promac P2A	EEPROMs, EPROMs, µCs	40	DIP	B, MV, RI, SST, ST	4M	firmware	yes	$1,895	menu-driven remote control, serial and parallel ports
Promac P16-IV	EEPROMs, EPROMs, memory cards, µCs	40	DIP, memory cards, PLCC	B, MV, RI, SST, ST	32M	firmware	yes	$3,300	gang/set programmer, automated remote control, serial and parallel ports
QuickLogic 2933 Bunker Hill Ln, Santa Clara, CA 95054 (408) 987-2000 **Circle 313**									
QP-PL68	FPGAs	68	PLCC	TV	—	floppy	no	—	programmer for QuickLogic's pASIC FPGAs
Red Square 11770 Warner Ave, Suite 226, Fountain Valley, CA 92708 (714) 751-1373 **Circle 314**									
Uniwriter 28	EEPROMs, EPROMs, PEELs, PLDs, bipolar PROMs	28	DIP	B, TV, V	unlimited	firmware, floppy	yes	$1,495	—
Uniwriter 40	EEPROMs, EPROMs, µCs, PLDs, bipolar PROMs	40	DIP	B, TV, V	unlimited	—	yes	$1,995	—
Omnisite 128	same as above	128	DIP, SMT	B, P, TV, V	unlimited	—	yes	$2,995	—
Retnel Systems PO Box 1348, Lawrence, MA 01842 (508) 683-4659 **Circle 315**									
ZAP-A-PAL Model-1	EEPROMs, EPROMs, FPLAs, GALs, µCs, PALs, PLDs, bipolar PROMs	68	DIP, PLCC	B, ST, TV	8M	floppy	no	$395	certified FCC Class B
ZAP-A-PAL Model-2	EEPROMs, EPROMs, GALs, µCs, PALs, PLDs	96	DIP, PLCC	B, ST, TV	8M	floppy, modem	no	$495-$695	—
Stag Microsystems 1600 Wyatt Dr, Santa Clara, CA 95054 (800) 227-8836 **Circle 316**									
System 3000	ECLs, EEPROMs, ELPDs, EPROMs, flash, FPGAs, µCs, PLDs	84	DIP, LCC, PLCC	B, C, IB, RI, ST, TV, V	8M	memory card	yes	$6,495	built-in CRT, menu-driven operation
ZL30A	ECLs, EPLDs, PLDs	52	DIP, PLCC	B, C, IB, RI, ST, TV, V	128k	firmware	yes	$2,995	interface for automatic handling
PP39	EEPROMs, EPROMs, µCs	40	DIP	B, C, IB, RI, ST, V	512k	firmware	yes	$1,195	PC remote control
PP40	EEPROMs, EPROMs, flash, PROMs	40	DIP, SOP	B, C, IB, RI, ST, V	none	firmware	yes	$1,195	copies master devices to 8 slave devices
PP41/42	EEPROMs, EPROMs, flash, PROMs	40	DIP, PLCC, SOP	B, C, IB, RI, ST, V	8M	firmware	yes	$1,795	programs in 8-, 16-, or 32-bit modes
Stratos	EEPROMs, EPROMs, flash	32	DIP	B, C, IB, RI, ST, V	PC memory	floppy	no	$495	can use any speed PC as host
MC6030	memory cards	—	—	B, C, IB, ST, V	PC memory	floppy	no	$695	can function as a programmer or as a PC disk drive
Cardeck	memory cards	—	—	B, C, IB, ST, V	PC memory	floppy	no	$16,495	programs up to 10 memory cards with full isolation
ICP9000	Any board with EEPROMs, EPROMs, EPLDs	—	—	B, C, IB, ST, V	8M	floppy	yes	$11,195	in-circuit programmer, programs up to 128 address lines and 64 data lines

Key: AI = auto identify; B = blank; C = continuity; ESD = electrostatic discharge; IB = illegal bit; MV = marginal verify; P = parametrics; RI = reverse insert; SST = silicon signature test; ST = self test; STT = structured test; TV = test vector; V = verify

Model	Devices supported	Maximum device pins	Package types supported	Tests (see key)	Maximum memory (bytes)	Upgrade method	Stand alone operation	Price	Comments
Sunrise Electronics 524 S Vermont Ave, Glendora, CA 91740 (818) 914-1926									**Circle 317**
T-816	EEPROMs, EPROMs, µCs	40	DIP	all	256k	firmware	yes	$1,895	portable programmer, contains an EPROM/µC emulator
T-2000	EPROMs, µCs, PLDs	—	—	all	—	floppy, modem	no	$3,995	in-circuit programmer
T-5000	EPROMs, µCs, PLDs	—	—	all	—	floppy, modem	yes	$19,950	self-contained PC with an in-circuit programmer
T-10	EPROMs, µCs, PGAs, PLDs, bipolar PROMs	40	DIP, LCC	all	—	floppy, modem	no	$999	available as gang/set programmer
T-1600	EEPROMs, EPROMs	32	DIP	all	—	floppy, modem	yes	$2,495	gang/set programmer, programs 16 devices at a time
Z-3000	EEPROMs, EPROMs, µCs	40	DIP	all	256k	firmware	yes	$5,995	gang/set programmer, programs up to 32 EPROMs at a time
System General 510 S Park Victoria Dr, Milpitas, CA 95035 (408) 263-6667									**Circle 318**
SGUP-85A	all	128	DIP, PLCC, SOIC	B, C, IB, MV, RI, SST, ST, TV, V	1M	firmware, floppy, modem	yes	$3,450	universal programmer, auto-handler interface
Turpro-1	all	128	DIP, PLCC, SOIC	B, IB, MV, P, ST, TV, V	PC memory plus 32k	floppy, modem	no	$1,695	PC-based, auto-handler interface
Turpro-832	EEPROMs, EPROMs, flash	32	DIP, PLCC	AI, B, IB, MV, ST, V	4M	firmware, floppy, modem	yes	$1,950	gang/set programmer, auto-handler interface, fully isolated sockets
Xeltek 764 San Aleso Ave, Sunnyvale, CA 94086 (408) 745-7974									**Circle 319**
Superpro	all	68	DIP, LCC, PGA, PLCC, QFP, SOIC, SOJ	B, TV	PC memory	floppy, modem	no	$795	optional algorithm library generator

Key: AI = auto identify; B = blank; C = continuity; ESD = electrostatic discharge; IB = illegal bit; MV = marginal verify; P = parametrics; RI = reverse insert; SST = silicon signature test; ST = self test; STT = structured test; TV = test vector; V = verify

"They effectively do a benchmark of the PC speed before they program a device. Then they scale the width of the pulses so that they're identical no matter what the speed of the PC you're running them on," says Clarke. A reliable PC-based programmer should also offer cell tests to check the integrity of the programming electronics, he says.

Including these safeguards, of course, adds to the programmer's cost. But the cost of not having them can be far greater. "If you want to get 99.9 percent programming yield you have to pay for it," says Clarke. "To pay for that last 0.9 percent of programming yield, it costs you a lot more than it costs to pay for the first 99 percent. That may not seem like much of a difference until you consider that every field failure of your product can cost a lot of money. So it can very easily be a false economy to select a cheaper programmer."

While many programmers are PC-based, there are others, such as Stag Microsystem's System 3000, that are stand-alone systems that can interface with a PC. The 3000 has its own built-in keyboard and CRT. Two RS-232 interfaces are included, mainly for interfacing to computers. While the system operates as a stand-alone unit, it can also be controlled externally from a PC. It also offers a handler interface for those who want to link the System 3000 up to an automated device handler. A universal programmer, the System 3000 can program nearly every device that's in a dual in-line package on the market. An adapter, enabling it to program devices in leadless-chip-carrier packages, plugs into expansion slots on top of the machine. Each pin has universal pin drivers and the system can drive up to 84 pins.

In-circuit programmer

Another option available to designers is in-circuit programming. In military and aerospace applications, where socketed devices are not used, in-circuit programming has been a fact of life. Today, driven

CAE/CAD TOOLS

by demands for quality manufactured products and the adoption of just-in-time programming, interest in in-circuit programming is growing among commercial users. In the past it was difficult to justify the cost of buying an expensive in-circuit programmer. "Up until just recently you were talking $20,000 for an entry level in-circuit programmer," says Dick Erickson, president of Sunrise Electronics, (Glendora, CA).

When designers decide to move to in-circuit programming, they will, of course, have to design their boards to support it. But this shouldn't be a deterrent. According to Stag's Clarke, these changes aren't very drastic. "The programmer has to gain access to all the control lines of the EPROM (or whatever is being programmed)," says Clarke. "On most designs the changes required are really small. You might have to add some decoupling capacitors here and there, and it's possible in some applications that you would have to add a buffer to something. So, the board might cost slightly more in terms of components. But those costs are more than outweighed by the fact that in-circuit programming simplifies both the factory production of the board and upgrades made in the field."

While its benefits in the production environment are obvious, in-circuit programming may also be a useful tool in engineering labs. An in-circuit programmer designed specifically for engineering applications, the T-2000 from Sunrise Electronics, automates the board programming task. Designers, for example, don't have to program individual devices and break up their program in the blocks to get them in the right EPROMs. The T-2000 comes with its own wire-wrap board that the user can configure to a particular application.

Currently, senior design engineer, Tom Baillio and his design team at Mercury Computer (Lowell, MA), don't use in-circuit programming. Baillio agrees, however, that in-circuit programing would prevent a lot of headaches. "On some of our boards over 50 percent of the devices are programmable logic," he says. "We solder everything in, but eventually an engineering change order (ECO) comes done the line and we're unsoldering chips. I could see in-circuit programming being a big help in that area."

Ground bounce

As devices get faster and faster, their edge rates are also getting faster and faster. From this arises a problem known as simultaneous-switching noise or ground-bounce, which is causing headaches for both device programmer designers and users. This phenomena forces system designers to treat PC board traces as transmission lines. Many semiconductor vendors are now specifying up to 1.5-V of bounce from the ground pad on the die to the part's pin, according to Keith Miller, engineering section manager at Data I/O (Redmond, WA). "That doesn't leave much room for device

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programmer designers to wiggle around on ground any more," says Miller. "It's especially a problem for the programmer manufacturer who's trying to build a universal machine that can handle various pin-outs. These days ground isn't always the lower-left corner pin of the part any more."

Miller was the engineering manager who built the 2900, Data I/O's universal device programmer. To address speed-related problems, the 2900 features a number of test

When designers decide to move to in-circuit programming, they will have to design their boards to support it.

■■■

and debugging aids, including a serial vector test. Normally a programmer stimulates all pins in parallel. Using the serial vectors option lets the user stimulate each pin separately. This helps determine if it's a sequence-related problem. Another test, called the compensated vector test, anticipates what the part is going to do and lets the programmer adapt itself, and adjust the loads on the outputs. This decreases the chance of any ground bounce errors.

According to Miller, the 2900 uses the same style pin drivers used in Data I/O's high-end Unisite programmer. Reducing the performance a little bit, Data I/O integrated the pin driver into a number of ASICs. This let the 2900 be much smaller and more portable than the Unisite. Like many automatic test equipment machines, its shape is round in order to locate the pin drivers a consistent distance away from the sockets. At the heart of the 2900 is a 4200-gate array which is basically an algorithm coprocessor. A 68000 processor deals with user interface and the general housekeeping chores. The "coprocessor" takes over when it's time to transmit critical wave forms out to socket. The 2900 also uses two semicustom analog ASICs, and another gate array that was borrowed from Unisite's design. ■

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SOFTWARE AND DEVELOPMENT TOOLS

Object-oriented CASE tool lets user tailor his own methods

The power of object-oriented software-development tools lies not only in its ability to develop modular, reusable code, but also in its own inherent flexibility. An object-oriented tool produces object-oriented code but it can be easily customized by the user to suit his or her own methodology and personal taste. Such a tool is ObjectMaker, a member of a new generation of CASE analysis and design tools from Mark V Systems (Encino, CA). ObjectMaker offers structured analysis and design as well as behavioral (state) analysis and design. In addition, there's a reverse-engineering facility that can produce diagrams from existing, poorly documented code to give insight into its design and functionality. Automatic code generation for Ada, C and C++ is also supported.

ObjectMaker supports over 20 off-the-shelf analysis and design methods and notation conventions including Buhr, Chen, Ward-Mellor, DeMarco, Yourdon, and many others. For the novice CASE user, ObjectMaker also contains a rule-base with rule checking to enforce a chosen methodology. But the user isn't constrained to even one of the many supported methods. The ObjectMaker tool-development kit provides the ability to customize any methodology by means of an extension language that lets the user modify the actions of accelerator keys, modify existing method rules, create custom methods including rules and semantic mapping and develop custom-code generation directly from diagrams.

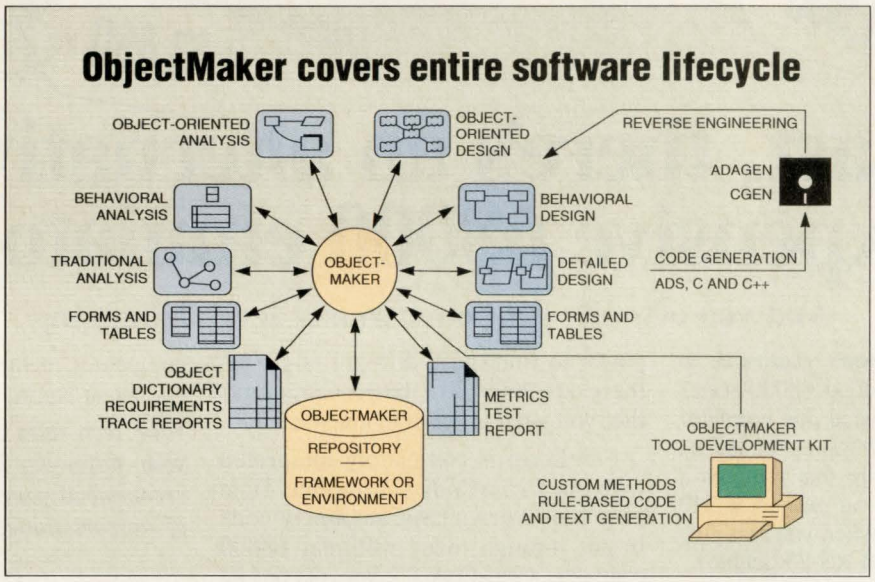
Being able to tailor the tools is important because, for example, C++ methods development is still in its infancy. Today's popular techniques may be overtaken by new developments that might render a CASE tool obsolete. The ability to define new methodologies and integrate them into an existing tool environment is expected to be a hedge against the danger of obsolescence.

ObjectMaker is conceived as a life-cycle project tool to be used from the initial generation of proposals through requirements analysis to code generation and maintenance. It includes an underlying data repository that maintains the intricate relationships between symbols and diagrams and the project dictionary. Document and diagram data can be output to a number of popular publishing software packages including Pagemaker, Ventura Publisher, Microsoft Word and Wordperfect.

The automatic code generation facility maintains consistency between the code templates and the design diagrams and their naming conventions. Code generation modules are available for Ada, C and C++. Mark V states that the actual percentage of automatically generated code can be as high as 60 percent, but will vary depending on the level of detail of the source diagrams, the availability of class libraries and the nature of the application.

ObjectMaker runs on a variety of PC and workstation platforms including Hewlett-Packard/Apollo, IBM RS6000, AT and PS/2, MIPS, Sun, Evans and Sutherland, Data General and Digital Equipment Corp. It's also adapted to three window environments: Macintosh, X Windows X11R4 and Microsoft Windows. ObjectMaker is available now, and depending on configuration and options, it's typically priced at about $6,000 a seat.

— Tom Williams



ObjectMaker provides object-oriented structured design and analysis from original concept through code generation and maintenance supporting over 20 existing methodologies. A reverse-engineering facility generated structured diagrams from undocumented code and a tool-development kit allows the user to customize the method of working.

ObjectMaker at a glance

- Off-the-shelf support for over 20 object-oriented and structured methods
- Binding for all methods to a single integrated repository
- Code generation and reverse engineering for Ada C and C++
- Operates with X Windows, MS-Windows and Macintosh
- Methods are customizable by the user
- Extensible to keep pace with evolving CASE technology

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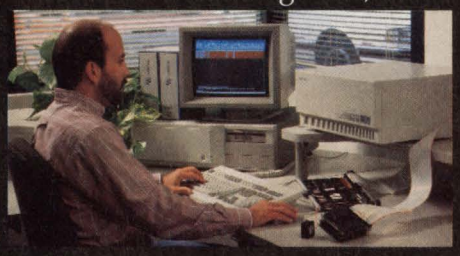

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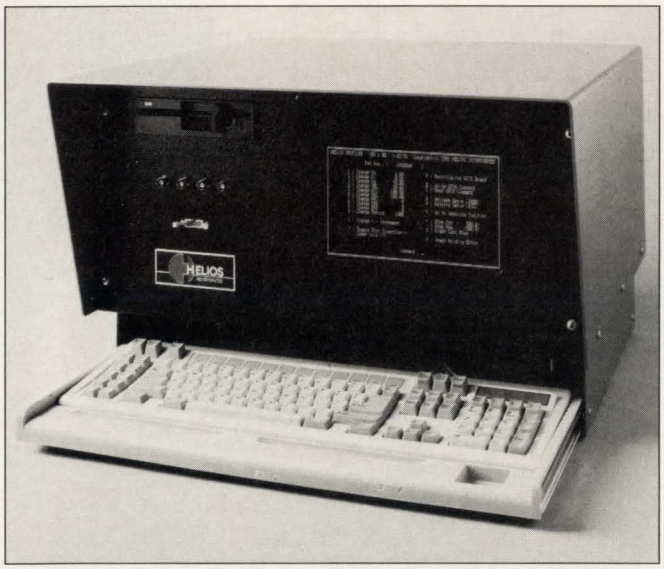
CIRCLE NO. 71

CAE/CAD TOOLS

Servo simulator trims months off disk drive design cycle

Traditionally, development of disk-drive electronics has been delayed until two critical stages were achieved: the manufacture of drive hardware and the development of the servowriter. The drive castings with actuator, head and media had to exist, and the servowriter had to write the servo patterns (reference information used to position the read/write heads) on the disks before the electronics could be tested and debugged. In many cases, this wait could add four to six months to a drive's design cycle. A product from Helios called Proteus, however, may change all that. Proteus simulates the servo signal of a drive before the drive is built. This permits the design engineer to develop and debug the drive servo electronics months before the hardware is ready.



The Proteus system simulates a disk-drive's servo signal and mechanical HDA characteristics before the drive is built.

Proteus

"We've been in the business of providing servowriters to high-volume, high-density disk-drive manufacturers since 1985," says Richard Freedland, president of Helios, "so we've seen first hand the delays that took place while our customers waited for the hardware and servowriter. We took our servowriting experience and developed a simulator that lets a company have the drive electronics debugged and rolling off the assembly line by the time the rest of the drive is ready."

Proteus simulates the composite servo-signal output of a disk drive as though the signal was derived from magnetically reading the servo pattern from the disk surface. The simulation of this signal is unique because it's created by the interference of two separate channels used for position reference. The channels exhibit an interdependence when changing states that indicates head positioning and movement. This simulated signal indicates drive head positioning when staying on a track or in seek mode. The system can also simulate closed-loop, complete feedback operation.

Proteus is fully programmable to simulate the head/disk assembly (HDA), including the voice coil motor, mechanical characteristics and the movement of the read/write head across the media. The designer can program a seek profile, media defects and servo patterns, as well as repeatable and nonrepeatable runout.

"Runout is a term used to describe anomalies in a disk drive's bearings," explains Robert Benson, marketing adviser at Helios. "Repeatable runout happens at regular intervals during a drive's rotation, whereas nonrepeatable happens at random, when a ball inside the bearing wobbles because it isn't perfectly round. In either case, it's important to see how much runout your servo system can handle to keep the heads on track."

Proteus can also be used in the manufacturing process to improve product quality. "Drive electronics are currently production tested by connection to a test drive or testing with the actual drive mechanics," Freedland points out. "This means that the test is run under normal conditions and shows how the electronics behave with that specific drive under that one set of conditions. Extreme conditions aren't tested."

Proteus can be programmed to simulate any conditions, including worst-case mechanical characteristics, to test the drive electronics' tolerance and recovery capability. By testing the boards under worst-case conditions, the electronics can be optimized for the degree of ruggedness required.

Proteus is a stand alone PC/AT-based system that includes a built-in keyboard and a high-resolution display. It's available now and is priced at $29,000. — *Mike Donlin*

Proteus at a glance

- Simulates servo signal of a disk drive before the drive is built
- Simulates worst-case conditions so drive electronics can be optimized for rugged environments
- Fully programmable to simulate the HDA, the voice coil motor, mechanical characteristics and read/write head movement
- Designers can program a seek file, repeatable and nonrepeatable runout, media defects and servo patterns
- PC/AT-based system with built-in keyboard and high-resolution display
- Available now for $29,000

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See Us At COMDEX.
CIRCLE NO. 74

CAE/CAD TOOLS

Mixed-signal ASIC toolset offers analog design for testability

For use at both customer sites and at Gould AMI, the new Mixed-Signal Design Solution (MSDS) incorporates analog model generators as well as analog design-for-testability features. Gould AMI claims that the proprietary and third-party tools within MSDS will keep time-to-market and development costs for analog/digital ASICs equivalent to those for complex all-digital ASIC designs.

The Gould AMI-developed Analog Model Builder which automatically captures customers' specifications and generates pre-layout simulation models for a variety of analog functions is among the MSDS tools that can be installed on customers' workstations. The Analog Model Builder checks customers' analog performance parameters against tester-specific rules and advises users if an analog function can't be tested as specified. It also captures users' test requirements for each of the analog blocks supported by the analog model builder. Employing an analog scan design technique, Gould AMI has coupled these analog blocks to test multiplexer cells, which along with an analog test bus, make the blocks observable and controllable, according to Gould AMI. Customized analog behavioral models for use with the Saber/Cadat mixed-signal simulator are output by the Analog Model Builder.

Also for installation at customer sites is Gould AMI's Design Critiquer, a knowledge-based tool that offers the nonexpert, built-in analog IC design expertise, according to Gould AMI. Customers can use the Design Critiquer at the schematic stage, with Mentor Graphics' design capture software, to identify combinations of functional blocks that can create design failures. Types of errors identified include power-supply bussing problems, insufficient drive and sense levels, as well as crosstalk and noise generation.

Gould AMI has also developed application tool interfaces for each MSDS tool installed on a customer workstation. These interfaces generate all of the information needed to run a tool for a given mixed-signal design project and automatically keep track of design-specific information needed to perform a given design task.

MSDS tools installed at Gould AMI include the proprietary Parameterized Analog Building Block Generators (PABBGs) and MSTEST testability software. Each PABBG captures, in software, the electrical and physical design expertise

needed to create an analog block from the specification provided by the Analog Model Builder. Each specialized PABBG enables Gould AMI to synthesize analog cells that meet the area and performance demands of a customer's application without substantial cost penalties, according to Gould AMI.

In addition to enabling customers to incorporate design for testability into their circuits, MSTEST speeds the creation of ASIC manufacturing test programs at Gould AMI. The performance parameters output by the Analog Model Builder are used by engineers at Gould AMI to create a test module for each analog block. Such a test module can be implemented in any test program where that particular design block is used.

Integrated under a single X-Windows-compliant graphic user interface, MSDS tools run on Apollo workstations. MSDS is supported by Gould AMI's range of high-density CMOS manufacturing processes. Available now, pricing for the MSDS toolset begins at $75,000.

— Barbara Tuck

MSDS at a glance

- Generation of custom analog models at customer site
- Expert analog design tools
- Production of a test module for each analog block
- Saber/Cadat mixed-signal simulator

Gould AMI
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OEM PRODUCT UPDATE

Canon Laser Beam Printer Family

The Canon family of OEM Laser Beam Printer Engines comprises the largest installed base in the laser printer market. This success has been built on Canon's well-documented reputation for reliability and low maintenance, innovation and high quality images.

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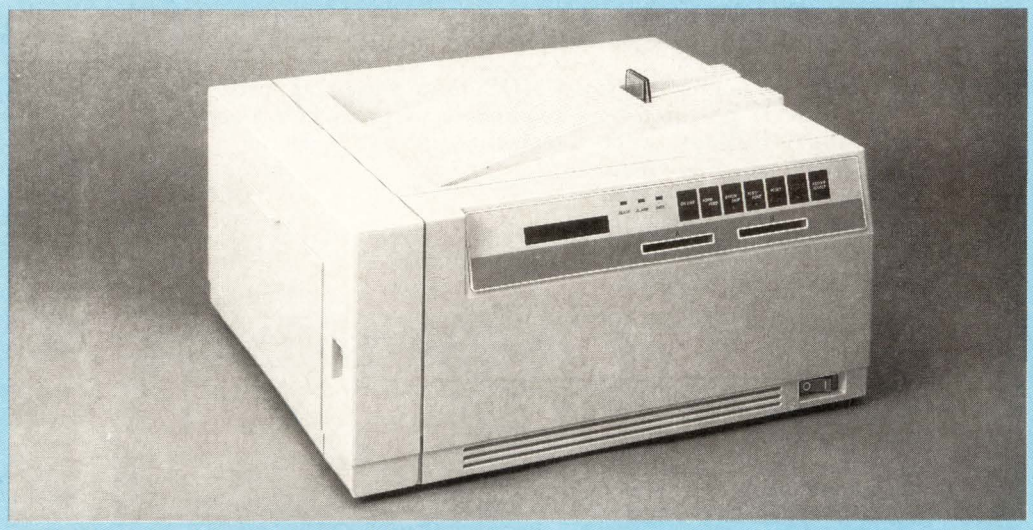
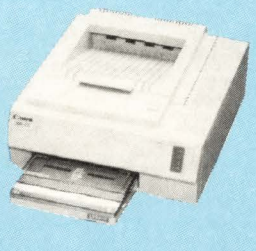


LBP-LX Laser Beam Printer Engine

A compact, affordable printer engine ideal for desktop applications. Utilizes the disposable EP-L cartridge. Available in both Video (external OEM controller) and PCB (internal OEM controller) models.

Monthly prints:	750
Resolution:	300/400 dpi
Print Speed (PPM):	4
Dimensions:	16.7"W x 14.1"D x7.6"H

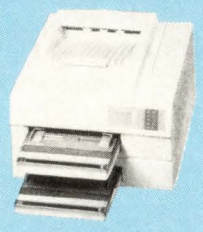
LBP-SX



The most popular laser beam printer in the world. Clamshell top cover permits easy access to paper path and disposable EP-S image cartridge. Available in Video and PCB models.

Monthly prints:	5000
Resolution:	300/400 dpi
Print speed (PPM):	8
Dimensions:	18"W x 19.5"D x 9.1"H

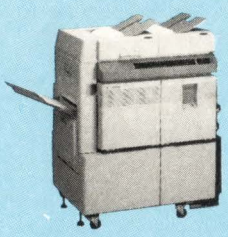
LBP-TX and LBP-RX



Hard-working laser beam printers featuring expanded paper handling. The RX model offers duplex capability. Dual cassettes hold up to 400 sheets and two types of paper. EP-S cartridge in all versions. Available in Video and PCB models.

Monthly prints:	5000
Resolution:	300/400 dpi
Print speed (PPM):	
TX Simplex	8
RX Duplex	7 (impressions)
Dimensions:	TX 18"W x 19.5"D x 12.5"H
	RX 18"W x 25.0"D x 12.5"H

LBP-20



A heavy-duty laser beam printer for large-format printing. Modular design allows multiple product configurations.

Monthly prints:	30,000
Resolution:	300/400/480 dpi
Print speed (PPM):	
Simplex: Letter	20
11" x 17"	10
Duplex: Letter	14 (impressions)
11" x 17"	8 (impressions)
Dimensions:	29"W x 24"D x 20"H

LBP-DX

Our largest-format laser beam printer. Outputs high-quality photographs, halftones and line art prints on vellum or paper. Ideal for engineering and graphics production. Handles 500-foot rolls of 24" wide paper or cut sheet sizes up to D (24" x 36").

Monthly prints:	5000
Resolution:	400/508 dpi
Print speed (PPM):	
D size (24" x 36")	3
C size (18" x 24")	5
Dimensions:	30"W x 39"D x 46"H

CAE/CAD TOOLS

Implicit mixed-mode simulation for analog/digital ASICs

The ANAsim mixed-mode simulator from ANAmation integrates relaxation and event-driven methods to simulate analog and digital circuits with a single engine. With ANAsim, users don't have to designate circuit elements as being analog or digital prior to simulation. Instead, as the design process progresses, the system informs the user of the quality of the signal at any node and the type of simulation needed for any element, as well as the results of the simulation. "The simulation happens implicitly, with the determining factor being the quality of the signal itself," says Robert Bowman, president of ANAmation.

The ANAsim behavioral modeling language, constructed using functions as extensions to the netlist format commonly found in analog simulators such as Spice, lets designers model components using equations. ANAmation has developed a built-in library of functions to model I/O behavior in mixed-signal circuits and to describe common analog behavioral qualities. ANAsim implements a variety of nonlinear functions including trigonometric, polynomials, complex, notch, etc. A filter designer, for example, can specify the characteristics of a filter as a ratio of two polynomials in a matter of seconds, according to ANAmation. Moreover, a superset of Spice includes a model description for every logic element type in ECL, CMOS, and TTL.

Though ANAsim runs as a standalone utility on Sun workstations as well as PCs, ANAsim is initially being offered only within ANAmation's ANAvision object-oriented environment which includes schematic capture, a cell library manager, plus a waveform analysis package called ANAscope. When ANAsim is used within ANAvision, system designers can switch from behavioral models to macromodels or schematic models. The design system provides simulation results by showing signal flow paths and the state of the elements (saturation, linear). For setting values, users simply double click on any device and set values via a notifier panel.

The ANAscope plotting package accepts input from ANAsim and lets users display and manipulate waveforms created by ANAsim. ANAscope displays the mode in which a signal is being interpreted and the nature of the signal. Users can store reference plots in the system's memory for later examination and comparison with different simulation runs.

ANAsim, bundled with ANAvision, is available now at $25,000 per seat.

— Barbara Tuck

ANAsim at a glance

- Automatic switching from analog to digital simulation as required
- Behavioral modeling capabilities in Spice format
- Built-in library of mixed-signal circuits and analog function behavioral models
- Implements many nonlinear functions
- Analog and digital waveforms can be displayed and plotted using ANAscope
- Complete object-orientated design environment for schematic capture and analysis
- Runs on Sun Workstations and PCs

ANAmation
30 State St, Suite 210
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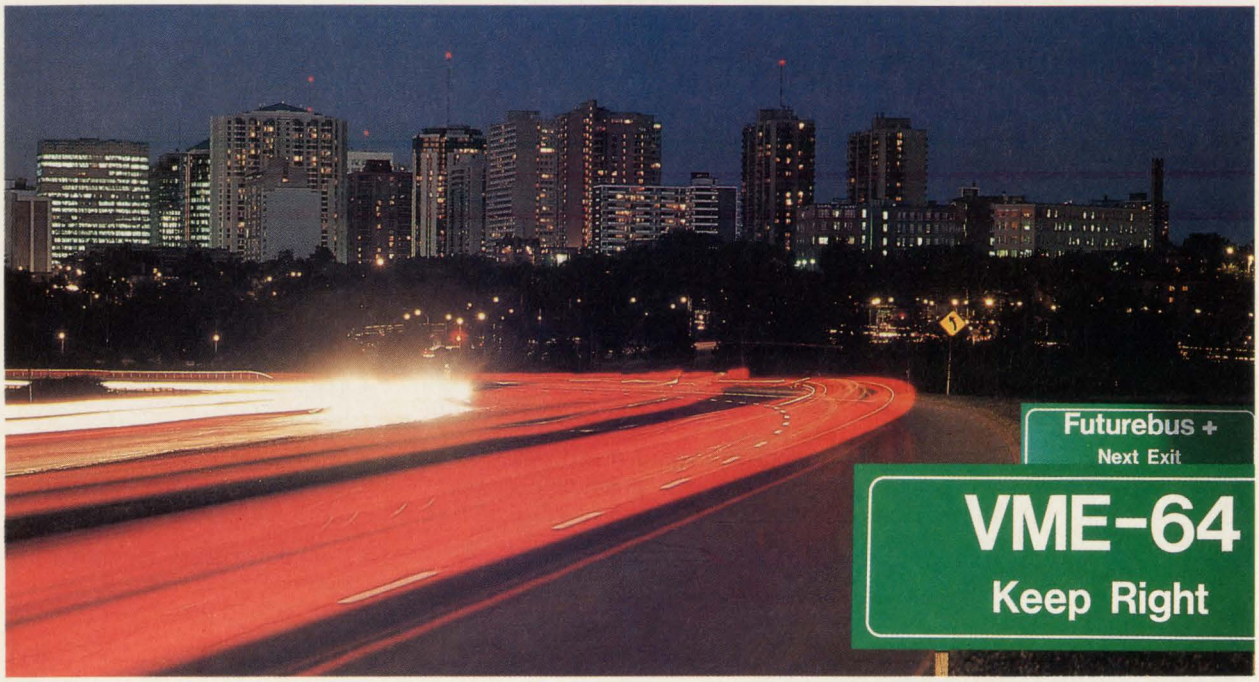
Whatever your destination on the open bus highway...



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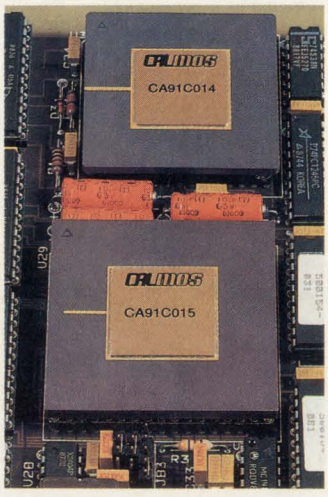
Leading the way with our 32-bit VME chipset that supplies a full high performance VMEbus interface, we provide a pin-for-pin compatible migration path to VME64. Our product direction extends beyond VME to devices and VHDL models for emerging Futurebus+ protocols.

The CA91C014 and CA91C015 VME chipset provides:

- IEEE 1014/VMEbus Rev C compliance
- Full VMEbus interface implementation
- High performance VMEbus decoupling with on-chip DMA functionality
- Bus Isolation mode for system diagnostics and fault isolation

For those applications demanding even higher performance, the CA91C064 VME64 device will offer users of our 32-bit chipset a pin-for-pin compatible upgrade to VME64.



Newbridge Microsystems is also developing a highly flexible solution for entering the Futurebus+ market quickly. The CA91C896 and CA91C897 Futurebus+ chipset will feature:

- Generic local bus and decoupled Futurebus+ interfaces to support split transactions for multiprocessing and burst transfers for higher performance
- Support for scalable external performance enhancements for use across a spectrum of applications
- Portable VHDL models to minimize design effort — and your time to market

Our second generation Futurebus+ products will include processor specific single chip devices, such as the CA91C880 for the Motorola 88K RISC processor family.

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CIRCLE NO. 77

CAE/CAD TOOLS

Timing tool eliminates data path vector requirements

Quad Design has equipped the latest version of its system-level analytical timing verifier—Motive—with several features that target ease of use. Motive Release 4.0 features a new algorithm called States (symbolic transition analysis of timing events) that automatically detects and evaluates the effects of complex, multicycle data path logic on system timing without requiring the specification of data path vectors. This enhancement delivers the benefits of using dynamic timing-verification tools, i.e., the ability to uncover multicycle timing relationships while eliminating the time-consuming task of generating data path vectors. This feature also reduces reports of false paths—predictions of delay paths that cannot occur.

"To correctly evaluate the timing behavior of digital circuitry controlled by multicycle logic," says Chuck White, vice-president of engineering for Quad Design, "a timing analyzer must be able to determine during which clock cycles a given circuit node or device changes logic state. Motive achieves this without the need for data path vectors by accepting and analyzing logic state information from any simulation tool, using a simple but powerful simulation data control file. Motive also lets a designer pick any number of nodes in a design for timing verification. The more data it's given, the more dynamic the verification will be."

In addition to the States algorithm, Quad Design has equipped Motive 4.0 with the ability to perform dynamic Boolean logic operations, which automatically eliminates many classes of false paths from timing analysis. The tool also features an algorithm that lets users identify multicycle, false or inferior signal paths and instructs the program to take that information into account, without having to specify such paths by hand. Motive also sports a new graphical user interface—the Open Software Foundation's Motif—which makes the tool interactive and easy to use. Motive users can eliminate false paths from their timing analysis results via a button displayed on their workstation screen.

According to Quad Design, Motive is the first EDA package that can analyze transparent latch behavior and complex skew relationships between system clocks. Its "explanation mode" provides detailed explanations about the characteristics of a signal delay as a signal moves between devices along a trace. With this information, designers can determine the right approach to solving a timing error, then implement the solution before prototyping. Motive also provides an EDIF (Electronic Data Interchange Format) translator that accepts database information from other EDA tools.

Motive 4.0 will be available in the fourth quarter of this year and will be priced at $10,000 to $50,000 depending on the platform.

— Barbara Tuck

Motive 4.0 at a glance

- Evaluates effects of complex, multicycle data path logic on system timing
- Dispenses with data path vector requirements
- Evaluates multicycle timing relationships to reduce reports of false paths
- Performs dynamic Boolean logic operations
- Features the OSF Motif graphical user interface
- Available Q4 and priced from $10,000 to $50,000 depending on platform

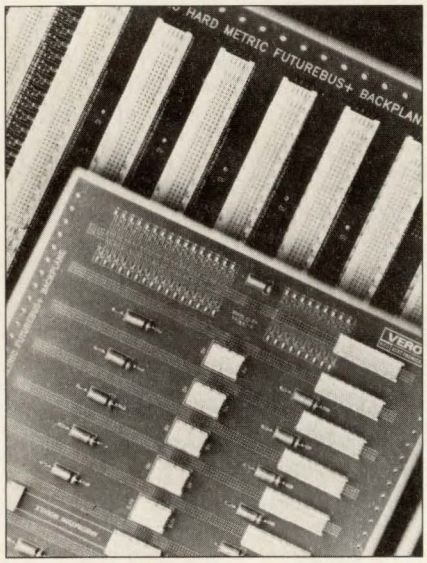
Quad Design
1385 Del Norte Rd
Camarillo, CA 93010
(805) 988-8250
Circle 279

COMPUTERS AND SUBSYSTEMS

Futurebus+ "F" backplane designed for maximum transfer rates

The first Futurebus+ backplane designed to meet the "F" profile of the P896.2 specification will be making its debut at Buscon/91-East in Washington DC later this month. The high-performance 64-/128-bit backplane has been designed by Bicc-Vero Electronics (Hamden, CT) to meet and exceed the maximum transfer rates specified by the "fast" profile.

The new backplane is made to conform to the IEEE 1301 "hard metric" specification, providing 13 slots positioned on 30-mm spacing. It's designed to accept 12-SU (300-mm×300-mm) boards. Bicc-Vero has been among the leaders pushing the Futurebus+ specification. It has also provided the first soft-metric backplane for Raytheon as part of the U.S. Navy's proof-of-concept Futurebus+ project. (That operating backplane will also be on display at Buscon.)



Bicc-Vero's new Futurebus+ backplane features a multilayer circuit board configured to a accommodate the fast Futurebus+ profile. The backplane is designed to accommodate up to 13 full-sized, hard-metric Futurebus+ boards using the 2-mm metric connector.

Profiles A, B and F are the only ones that have reached the final approval stage. The profiles are waiting for the IEEE's approval to become a completed standard. Though all three profiles share the hard-metric configuration, they each differ in some respects. Profile A is a full implementation of the P896.1 logical definition of Futurebus+, yet it leaves some performance parameters to be implementation dependent.

Profile B is referred to as the I/O profile and comprises a subset of the P896.1 protocols. It's profile B that has been projected as the market leader because of its strong support by Digital Equipment Corp, Stardent and other large computer makers. But these companies have yet to make any product announcement. It's also been considered that profile F, however, will be one of the early market leaders because only those interested in blazingly fast performance will be willing to pay the Futurebus+ price tag in the immediate future.

"We expect the profile F backplane to be the most popular version with designers, at least for now," says Mike Humphrey, vice-president of strategic marketing at Bicc-Vero. "System designers now realize that Futurebus+ packaging hardware actually exists and that backplanes conforming to the specification will offer levels of throughput not previously available on open architecture systems," adds Humphrey.

The major feature distinguishing the profile F backplane from profile A is the routing of the central arbitration circuitry, which is very rigidly defined. In the profile F version, all arbitration circuitry must be tracked from the lower pin-field in connector E. In the profile A version, this connector is used for I/O. The two profiles are otherwise similar to the extent that profile F boards will operate in a profile A system, but not vice versa.

As more companies start to investigate Futurebus+ and devote engineering resources toward design, they can't be in doubt about the availability and performance of backplanes, says Humphrey. "Silicon is already available and that demands a backplane in full compliance with the Futurebus+ specification," he says. He adds that Bicc-Vero's new backplane is the result of more than two-year's development and will satisfy the most demanding performance requirements.

Inherent in the 16-layer backplane design are Bicc-Vero's new surface-mount termination techniques. This minimizes signal skew and allows all the benefits of BTL (backplane transceiver logic) circuits to be realized. The approach calls for 33-Ω, surface-mount resisters and high-speed capacitors to be arranged to exactly match the length of each signal trace, thus minimizing skew. The capacitors provide local high-speed charge storage directly to each line, which is further protected from the effects of ground bounce by multiple power and ground planes together with a pattern of ground tracking.

Power for each power rail is brought to the backplane via Bicc-Vero's Lomet connector, developed to counteract the skin effect experienced with fast-rising edges associated with BTL drivers. Lomet provides a low impedance interconnect to the multiple main power and ground planes with power studs being used to bring less-critical voltage levels (±V and 5-V battery-backup/standby) to the bus.

In addition, Bicc-Vero's system provides full thermal management of the power-conversion module, which is fully self-contained and contains its own cooling system. Three, large-capacity variable-speed fans mounted at the rear of the rack, draw air across the board area and exhaust it through the rear. Remote sensors monitor the cooling efficiency of each fan and adjust the speed accordingly.

— Warren Andrews

Futurebus+ backplane at a glance

- P896.2 Compatible
- 13 slots
- Hard metric
- Profile "F"

Bicc-Vero Electronics
1000 Sherman Ave
Hamden, CT 06514-1336
(203) 288-8001
Circle 276

COMPUTERS AND SUBSYSTEMS

VisionMaster scores with high-performance graphics and image processing

A new graphics-processing module combines high levels of image generation and graphics processing in a single module. VisionMaster, the first high-performance graphics board to come from Radstone Technology (Montvale, NJ), is a fully compatible VMEbus module, calling for three VMEbus slots in its minimum configuration, and is capable of displaying up to 2048×1024 pixels, interlaced or non-interlaced, RS-343 compatible.

The module offers a fully programmable video format and will drive any standard RGB monitor and accept an input from any standard video format, including all television standards including PAL, NTSC, D2MAC and SECAM. The module comprises 4-Mbytes of video memory divided into two 2-Mbyte blocks, which is backed up by as much as 256-Mbytes of optional extended memory. The later extends the module's storage capability up to 30 seconds of real-time PAL television.

The standard 8-bit pixel depth allows the display of up to 256 colors and/or gray shades from an overall palette of 16.7 million colors. The module features a front-panel video bus interface designed to control and synchronize as many as three VisionMaster modules to extend the total system capability. This allows the system to provide as many as 24-bits/pixel and for the entire palette of 16.7 million colors to be displayed. For CMYD applications, four modules can be combined.

On-board processing

The module's pixel-processing capability comprises four, 4-×16-bit, bit-slice processors operating in parallel to provide peak execution speed in excess of 160 Mips. The processor can perform almost all standard graphic functions including line drawing, area filling, Gouraud shading, edge detection, filtering, anti-aliasing, affine transformations and more. Sun Microsystems' Pixrect and many X11.4 functions are available directly from firmware. There are more than 100 graphics and imaging functions built into on-board firmware.

Typical performance of the module exercising its processors includes 4-Mpixel/s vector-draw rate, 160-Mpixel/s block-fill rate, 20- to 160-Mpixel/s Gouraud-shading rate, and 10-Mpixel/s anti-aliasing rate. Other benchmarks include 5.3-Mpixel/s rate for 9-point convolution, 8.4-Mpixel/s binary-erosion rate, 26-Mpixel/s histogramming rate and 14-Mpixel/s correlation.

A built-in RS-343-compatible frame grabber combines 8-bit resolution with a maximum sample rate of 30-Msamples/s. Eight Gamma correction tables including one that's programmable, are available for camera-input correction. The module has on-board hardware to support up to two cursors which can be either cross hair and/or 64-×64-bit maps. It also provides zoom in both directions with a magnitude of one, two, four, eight and 16 times.

In operation, video input is fed to the frame grabber then to the main video memory through a I/O multiplexer. The video signal proceeds to a data switch and processor or optionally to the extended memory. Video timing is provided by the on-board timing generator which also interfaces to the VMEbus.

The pixel processor (comprising the four bit-slice processors) is controlled from the main program, or from an included microcode assembler sequencer (MICAS) and returned to either the main- or extended-video memory. The data switch is also connected to the VMEbus interface and DMA controller. VisionMaster's price hasn't been determined yet.

— Warren Andrews

VisionMaster at a glance

- 2048×1024 pixel display
- Interlaced or non-interlaced
- RS-343 compatible
- Built-in frame grabber

Radstone Technology
20 Craig Rd
Montvale, NJ 07645-1737
(201) 391-2700
Circle 275

COMPUTERS AND SUBSYSTEMS

Dual-i860 board delivers 160 MFlops

Using multiple microprocessors on a single board is becoming an attractive way to maximize overall performance. CSPI has taken this approach with its latest vector processor card, the SC-2XL/VME, by sporting two 40-MHz Intel i860 chips. Specifically designed for applications in signal processing, such as sonar, radar, seismic, simulation, and real-time processing, the SC-2XL/VME offers 160-MFlops performance, 16-Mbytes memory, and a 40-Mbyte/s VME subsystem bus (VSB) interface.

At the heart of the SC-2XL/VME board are two Intel i860 microprocessors. The i860s operate together in a master/slave relationship, forming a high-performance processing engine. During each clock cycle, each 40-MHz i860 can perform a floating-point multiply and add. CSPI offers a hand-coded library to help designers make full use of this architecture.

The SC-2XL/VME delivers 160-MFlops performance for functions like fast Fourier transform, convolution and correlation. Illustrating its performance, it takes just 133 ms for the board to perform a 512×512 real, two-dimensional FFT (including bit reversal.) According to CSPI, finite impulse-response filtering runs on the board at rates approaching the board's 160-MFlops peak due to the balanced architecture of the two i860 chips. Memory on the board includes 2-, 8-, or 16-Mbytes of page mode DRAM. Page mode allows data fetches at the boards architectural limit of 160 Mbyte/s.

Data from external devices can be transferred across either the VMEbus, the VSB or the daughter I/O port at rates approaching 160 Mbyte/s. Through a daughterboard I/O port, both DMA and shared-memory access is permitted to the SC-2XL/VME's main memory. I/O daughterboards for VSB or custom I/O configurations are available. Occupying the same slot with the 6U form factor SC-2XL/VME, the I/O daughterboards add extra I/O capability without using any additional slots in a VME backplane.

Software available for the SC-2XL/VME includes advance signal-, image-, and seismic-processing libraries, along with C and Fortran compilers. Operating systems available for the board include the pSOS+ real-time operating system kernel and the Unix-compatible Unison operating system. Unison combines Unix system calls with the network file system (NFS), TCP/IP (Transmission Control Protocol/Internet Protocol), and X Windows support.

Multiprocessing is supported by SC-2XL/VME. Up to 16 of these boards can be controlled from a single application. By taking advantage of the multiprocessing/multitasking features of pSOS+ and Unison, users can easily develop and debug multiprocessing applications for the board.

Available now, prices for SC-2XL/VME start at $8,500.

—Jeffrey Child

The SC-2XL/VME at a glance

- Two 40-MHz Intel i860s
- 2 to 16 Mbytes
- 6U form factor
- Maintains 160-Mbyte/s performance doing FFTs, convolutions, and correlations
- Up to 16 SC-2XL/VMEs controllable from one application
- C and Fortran compilers
- Signal-, image-, and seismic-processing libraries
- VME, VME subsystem bus and I/O daughterboard interface
- VSB or custom I/O daughterboards
- Supports pSOS+ real-time kernel and Unison

CSPI
40 Linnell Circle
Billerica, MA 01821
(617) 272-6020
Circle 290

INTEGRATED CIRCUITS

SRAM revamped for more speed, less noise

As clock frequencies race past 33 MHz, one of the first components to feel the pressure has been the SRAM. Used as cache, high-speed scratch-pad memory, vector arrays, and as main memory in high-performance systems, SRAMs struggle with different problems that vary from one subsystem to another. But all these applications share the problems of high-speed design, particularly those related to transmission line effects, capacitive loading and crosstalk due to long parallel paths.

Despite these new concerns, most SRAMs continue to be designed using old habits. However, at least one SRAM vendor, Electronic Designs (EDI), has taken some new approaches with its 1-Mbit, 17-ns SRAM. To enhance the speed and power of the device the company cast out some old ideas, while adding some new ones.

Increased speed and overall performance improvements were achieved through the elimination of address transition detection (ATD). Redesigned output buffers provide further speed enhancement by reducing the package induction. And the routing of the signal and power lines is optimized to reduce noise.

Goodbye ATD

While many memory chips still use ATD by force of habit, it's not necessary with today's high-speed designs, EDI claims. In fact, ATD often creates problems due to edge sensitivity.

To further reduce sensitivity to reflections, the SRAM uses hysteresis technology. Hysteresis reduces sensitivity to reflections caused by unterminated address and control lines, or reflections in certain terminated bus structures. According to EDI, hysteresis lets users put more memory devices on the same address lines without worrying about false triggering of the part and the extra power consumption it causes.

Further enhancing the SRAM's speed, EDI designed the chip's output buffers to better cope with package inductance. Most SRAM designs end up significantly limiting the edge rate of their output buffers to keep internal noise at an acceptable level. This tends to raise the impedance of the driver. In contrast, EDI's designed a buffer that sets the impedance much lower than other approaches. Also, the buffer uses special circuit techniques to reduce internal noise. This technique adjusts the driver to turn on at the same time regardless of the transistor gain.

Although noise problems are not usually given top priority in most SRAMs produced today, EDI decided to tackle it head-on through careful routing of the SRAM's power and signal lines. Paying particular attention to bus and signal placement results in a part that's more tolerant of the noisy environments of today's high-performance systems, according to EDI.

Offered in organizations of 128k×8, 256k×4 and 1M×1, this line of 1-Mbit SRAMs offers speeds from 17- to 35-ns built in a 0.8-µm CMOS process. The 128k×8 is available with either the single- or dual-chip module and the 256k×4 can be configured with either common or separate I/O. The 1-Mbit SRAM has been designed so that any one of the five possible configurations can be selected at bond-out, rather than through a mask option. As a result, full device characterization data applies to the entire family of 1-Mbit SRAMs.

Available in sample quantities, prices range from $64 to $221.

— Jeffrey Child

1-Mbit SRAMs at a glance

- Access speeds up to 17 ns
- Available in 128k×8, 256k×4, and 1M×1 organizations
- 128k×8 version available with single- or dual-chip enable
- 256k×4 version available with either common or separate I/O
- Performance enhanced by abandoning address transition detection (ATD)
- Output buffer design reduces package induction
- Routing of the signal and power lines optimized to reduce noise

Electronic Designs
42 South St
Hopkinton, MA 01748
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Circle 289

INTEGRATED CIRCUITS

Sparc gets smaller still

Add another vendor to the burgeoning list of chip houses now building Sparc compatible processors and chip sets. Rather than make the processor itself, however, the strategy at Tera Microsystems (Santa Clara, CA) is to sell its peripheral chip set, dubbed Microcore, by leveraging off the Sparc CPU/floating point unit expertise of other semiconductor suppliers, like Weitek, Fujitsu and LSI Logic. Microcore comprises four devices, the TM5610 system control unit (SCU), the TM5620 I/O controller (IOC), the TM5630 SBus interface chip (BXP), and the TM5640 color video display controller (CXP). The level of integration offered by this approach reduces the component count of a full Sparc system to less than 20 components.

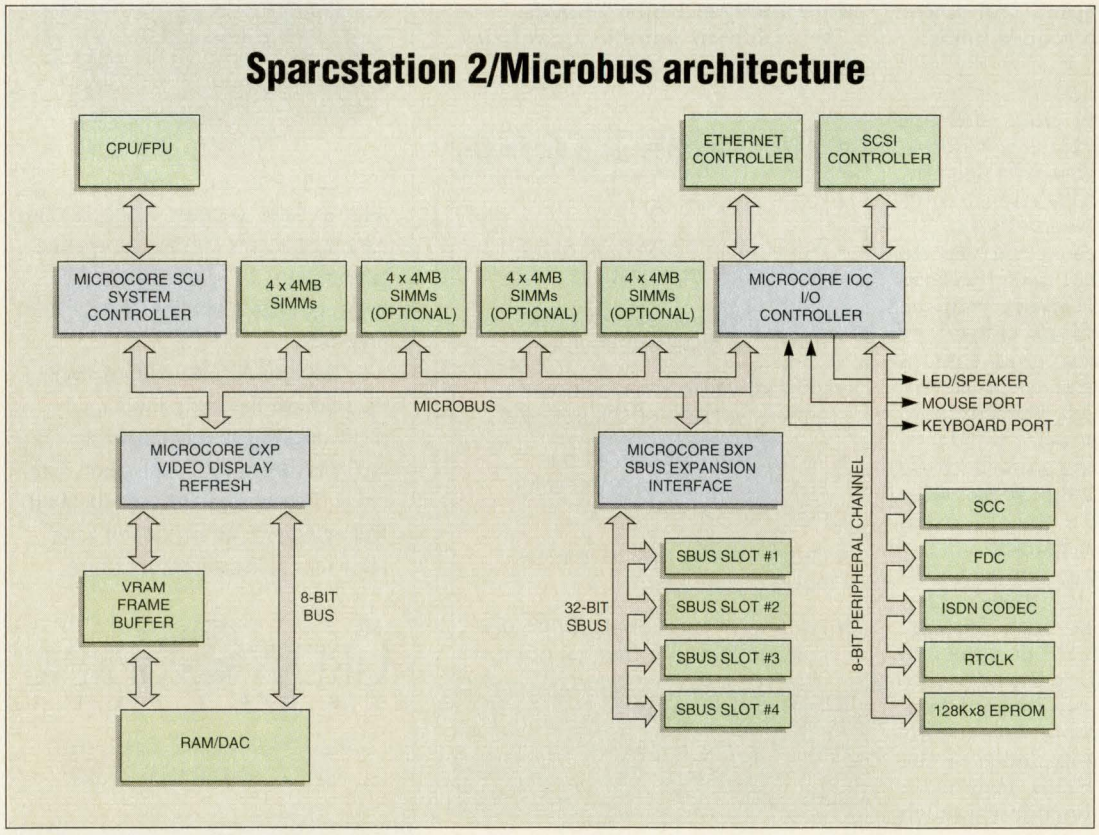
The 5610 System Controller interfaces to a Sparc CPU. It combines a Sparc reference MMU, 8 kbytes of cache memory (4 kbytes data and instruction) as well as a DRAM controller and write buffer on-chip.

The I/O controller, the 5620, offers buffered interfaces to AMD's Lance Ethernet controller and the 53C90 SCSI controller. A peripheral/memory channel, offering three undedicated DMA channels, supports up to eight byte-wide devices. Integrated peripheral functions include an interrupt controller, three counter timers and two serial ports. In addition, the IOC offers monochrome video display support, utilizing a DRAM-based frame buffer. An X-compatible hardware cursor has also been included.

Two optional Microcore components allow the implementation of a full-color system with SBus support. The color video display controller, the 5640, supports 8-bit color and gray scale displays with resolutions up to 1280×1024. Video RAMs and RAM D-A converters are the only external components required. For standard SBus support, the SBus interface chip implements the SBus B.0 specification and will let the designer build a system with up to four SBus slots.

With the integration of cache memory and main memory interface control on the SCU chip, Tera has optimized the time required to transfer blocks of data from memory into the cache. In particular, interchip communications involved in sending address and control information to the memory controller, and the overhead of arbitrating for the bus and initiating bus transactions are reduced. A further reduction in miss penalty is achieved by reducing the amount of time that the CPU is stalled during a cache line fill and by overlapping the remaining fill cycles with continued CPU execution. Tera's implementation supports this with line wraparound, interleaving accesses to the data caches, as well as streaming, if the CPU requests the next word in the cache line being filled, the CPU is sent the data as it's being written to the cache.

The key to keeping the cost of the chip set and hence the architecture of the system down, is the Microbus itself, the bus through which all the Tera devices communicate. While several Sparc chip set implementations have been based on MBus, Tera chose to define the Microbus. Tera sees the MBus as appropriate for multiprocessor systems, and for moderate to high-cost designs in



Microbus connects the four Microcore Sparc system chips from Tera Microsystems together. By designing its own bus, and focusing on building peripheral chips, rather than core processors, Tera hopes to target the under $5,000 Sparc clone market, an area as yet untouched even by Sun itself.

which the cost of upgrading the CPU module is attractive. But the company felt that these weren't important in the desktop and portable system designs for which the Microcore chip set was intended.

Microbus uses a simpler bus protocol than MBus and has a smaller number of signals. Both buses support the 36-bit physical address space defined by the Sparc MMU specification. The Microbus provides a 32-bit-wide (plus optional byte parity) data bus versus the 64-bit-wide data bus provided by MBus. In total, Microbus requires 44 signal pins on each component interfacing to the bus. This contrasts a total of 74 signal pins on each component interfacing to MBus. This reduction in pin count lets the Tera chips be packaged in quad flat packs and hence offered at a lower cost.

The SCU and the IOC will be sampling during 3Q91 with production volumes available by the end of the year. The color video display controller (CXP) and SBus interface (BXP) will sample in the fourth quarter. The SCU and IOC combination at 25 MHz is priced at $400. The full 33-MHz Microcore chip set will be $745. — *Dave Wilson*

Tera chip set at a glance

- Sparc-compatible four-chip set
- Optimized memory/cache interface
- System reduced to 20 components
- Simpler bus interface than Sun's MBus

Tera Microsystems
5200 Great America Pky
Suite 250
Santa Clara, CA 95054
(408) 987-5600
Circle 277

INTEGRATED CIRCUITS

FPGA enables fast, 16-bit counter designs

The virtue of field programmable gate arrays (FPGAs) is that they help designers build smaller, cheaper and faster systems. Using an FPGA, dozens of packages worth of TTL can be crammed into a single package. But to win with an FPGA requires the right combination of functional capacity and speed. With its A1240 FPGA, Actel appears to offer both, touting it both as the fastest and as the second highest-density FPGA in the industry.

The second member of Actel's ACT 2 family of gate arrays, the A1240, offers high-performance by delivering 66-MHz overall system speed. The part also offers impressive performance in specific common circuit functions. For example, it enables the design of 16-bit counters performing at 75 MHz. Furthermore, the FPGA permits the design of 33-MHz, 16-bit accumulators. The device has 4,000 equivalent gates which translates as 3,200 available gates, assuming an average automatic design efficiency of 80 percent, according to Actel.

The A1240 can be designed and programmed using Actel's Action Logic System Release 2.01. Advanced routing algorithms and ample routing resources deliver 100 percent routable designs, fully automatic, at 95 percent module use.

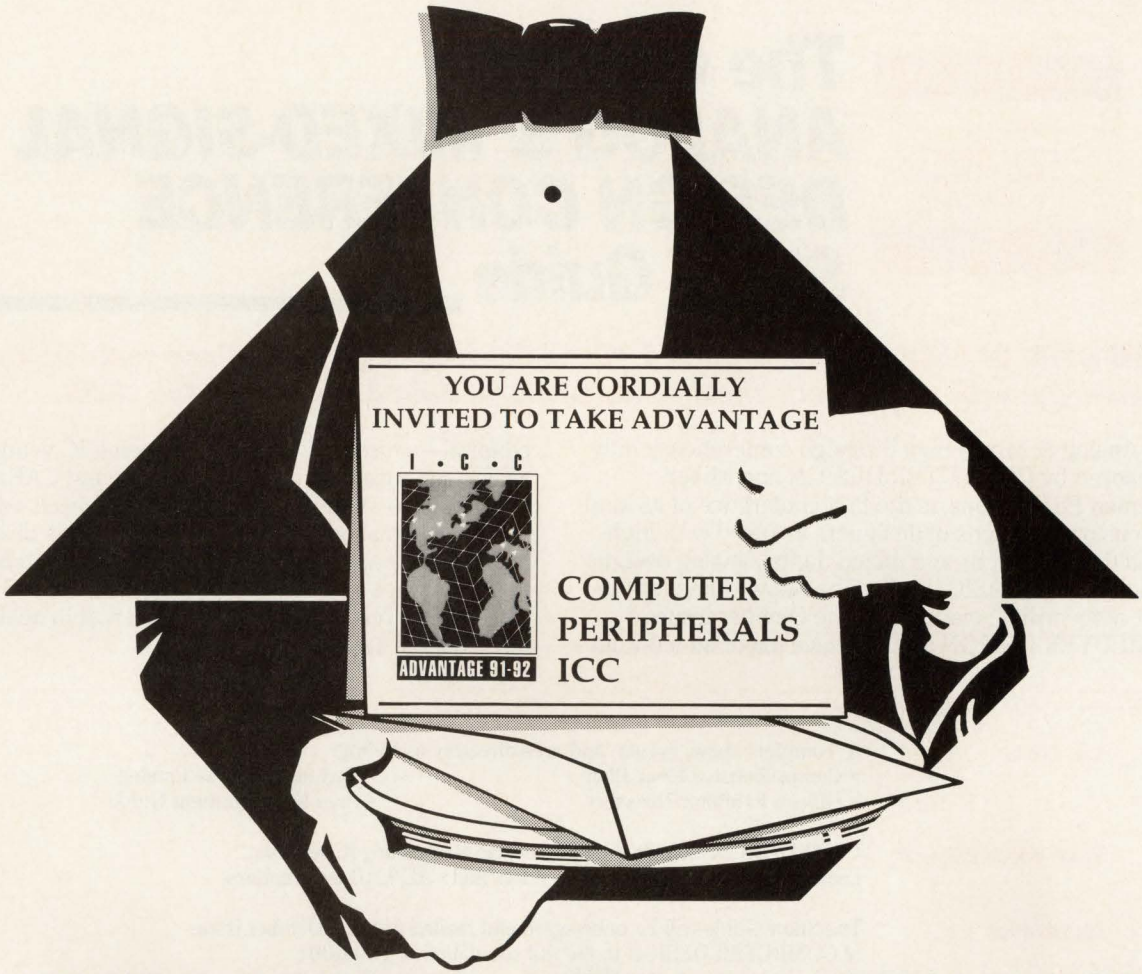
Processed in 1.2-μm CMOS, the A1240 offers 104 user I/Os, a maximum of 565 flip-flops, and 684 logic modules. The A1240 shares the same architectural attributes as its other family member, the A1280, Actel's 8,000-gate device. This architecture includes a two logic module design that optimizes performance and logic module use. One module type builds high fan-in combinatorial macros and can handle up to seven input functions. The other module configures sequential macros. It can accommodate a latch or flip-flop and/or many combinatorial macros of one to seven inputs. State machines with up to five product terms, each with five inputs, require only two module delays.

Available now in a 132-ceramic pin-grid array package, the A1240 is priced at $210 (100s). A 144-pin plastic quad flatpack version is priced at $150 (100s). —*Jeffrey Child*

The A1240 at a glance

- 4,000 equivalent gates, 3,200 available for design
- 66-MHz overall system speed
- 100 percent automatic place and rout
- 104 user I/O pins
- Up to 565 flip-flops
- Combinatorial and sequential logic module types
- 684 logic modules

Actel
955 E Arques Ave
Sunnyvale, CA 94086
(408) 739-1010
Circle 291



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PUBLISHER: David L. Allen, 508-392-2111 • ASSOCIATE PUBLISHER Tim L. Tobeck, 508-392-2116• NATIONAL ACCOUNTS MANAGERS: • WESTFORD, MA, Tim Pritchard, 508-392-2217 • SPRING, TX, Eric Jeter, 713-353-0309 • SAN JOSE, CA, Diane Palermo, 408-292-6837 • STRATEGIC ACCOUNTS REPRESENTATIVE: • WESTFORD, MA, Sue Nawoichik, 508-392-2118 • INTERNATIONAL SALES OFFICES: • SURREY, ENGLAND, David Round, 81-686-7655 • PARIS, FRANCE, Daniel R. Bernard, 1-39-14-6780 • MUNICH, GERMANY, Johann Bylek, 089-903-8806 • MILAN, ITALY, Luigi Rancati, 02-70-30-0088 • TOKYO, JAPAN, Toshio Equsa, 81-33-536-5404 • ASIA, AUSTRALIA, NEW ZEALAND, TOM GORMAN, 852-833-2181

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A starter kit enables system designers to introduce fiberoptic link products to their customers. Augment's AL 100 Series links are board-level fiberoptic products that enable direct, high-speed point-to-point links between VMEbus, NuBus, and DEC Unibus and Q-bus computers. Consisting of two AL 100 Series boards, 150 ft of fiberoptic cable, and special engineering support, the starter kit lets OEMs buy a single fiberoptic link at a discount for evaluation and development.
Augment Systems **Booth 419**
(617) 271-0230

Telecom interface card sports 12 DSPs

The VME9U12 combines 12 digital signal processors with a T1 phone line interface on a 9U VME board. The DSPs, each with up to 512 kbytes of SRAM each, talk to each other and the T1 line via four software configurable serial buses. The board also has a bus master and slave controller for DMA and memory-mapped transfers. Communications are performed by C-callable functions. An optional mezzanine card adds 12 codecs that can access the serial buses for individual voice input and output. Fully populated with all 12 DSPs, the board costs $29,000.
Communication Automation & Control **Booth 319**
(800) 367-6735

Dual-i860 vector processor delivers 160 MFlops

The SC-2XL/VME combines two 40-MHz i860 chips in a master/slave relationship to form a processing engine. Each i860 can perform a floating-point multiply and add during each processing cycle. Targeted for signal-processing applications, the board offers 160-MFlops performance for functions such as fast Fourier transform, convolution and correlation. The card comes with up to 16 Mbytes of page-mode DRAM. Data from external devices can be transferred over the VME, the VSB or the a daughterboard I/O port at rates approaching 160 Mbyte/s. Prices for the SC-XL/VME start at $8,500.
CSPI **Booth 314**
(617) 272-6020

System enclosures feature improved cooling

The MaxChassis II enclosures are designed to fit large systems into a standard 19-in rack or on a tabletop. Rack space accommodates both VMEbus or Multibus II standard systems. Available in 12- and 20-slot configurations, the enclosure features a cooling technology that keeps cards well within temperature specifications. The 12-slot box has a mounting assembly providing front access for two full-height or four half-height 5¼-inch disk drives. System designers can choose from over 200 models, including special order combinations and numerous front-panel alternatives. Prices for the MaxChassis II enclosures start at $3,000.
Electronic Solutions **Booth 1007**
(619) 452-9333

Portable VME enclosures

A family of small portable tower enclosure systems fits up to 12 6U×160mm VME cards. Designed for optimum air flow dynamics, the enclosures allow air intake from the front and exhaust at the back. The systems include a power supply located on a hinged rear door. Available in 3-, 5-,7-, and 12-slot versions, all systems are fully wired, tested and ready to run with power supply, fans and backplanes. Price of a typical 3-slot version starts at $1,200 in quantities of 20.
ELMA Electronic **Booth 229**
(415) 656-3400

68040-based VME board offers extensive I/O

The GMS V49 is a real-time, multiprocessing SBC for the VMEbus. Based on the 68040, the board features an Ethernet/Cheapernet transceiver interface, a SCSI interface and eight channels of RS-232 or RS-422 serial I/O with five lines of optically isolated digital I/O. To facilitate embedded design, all I/O is

routed through the P2 connector, allowing cabling to be attached to a break-out board on the back side of the VME J2 backplane. Custom I/O functions can be added via a selection of 16-bit expansion modules. Memory on the board includes up to 4 Mbytes of battery-backed SRAM, up to 4 Mbytes of EPROM, and either 2 or 8 Mbytes of two-way interleaved DRAM. The V49 is priced at $3,600 (100s).

General Micro Systems **Booth 1109**
(714) 625-5475

68EC030-based VME CPU board

The HK68/V3D, a VME board based on the 68EC030, features clock speeds of 33 MHz, 2 to 16 Mbytes of static column DRAM, two RS-232 serial ports and optional Ethernet and SCSI controllers. Also included on the board are 128 bytes of nonvolatile RAM and sockets for two 1M×8-bit EPROMs. Software support for the V3D includes VxWorks 5.0 and OS-9 2.4 operating systems. The board is priced from $1,795 to $3,995, depending on memory configuration.

Heurikon **Booth 908**
(608) 831-0900

386 EISA board offers 32-kbyte cache

The EI1120 is an 33-MHz 80386DX-based EISA plug-in SBC featuring a high-speed cache. Governed by an Intel 82385 cache controller, the cache consists of 32 kbytes of high-speed memory. Also integrated on this AT-form factor card are a hard disk interface, a floppy disk controller, two RS-232 serial ports, and a Centronics parallel port. Strict adherence to EISA design specifications allows users to take advantage of extensive software available for XT/AT and EISA systems.

International Control Systems Pte Ltd **Booth 619**
(65) 278-8288

Expansion module exceeds 30 Mbyte/s

The DB-PCOMM is a parallel communications module that transfers 32-bit data above 30 Mbyte/s. This expansion module attaches to any double-height host CPU with a Dbus-68 interface. Designed for systems that must capture incoming signals with no loss of data, the module features a large FIFO to prevent such losses. Besides the high-speed parallel port, the DB-PCOMM also interfaces to the VME subsystem bus (VSB). Operating independently of the host CPU, an on-board DMA controller handles block transfers between the FIFO and either a parallel I/O port or the VSB interface. The module is priced at $2,995.

Matrix **Booth 1100**
(919) 231-8000

68040-based CPU boasts advanced design

Based on a 25-MHz 68040, the MVME167 is a CPU card for the VMEbus that combines extensive use of ASICs, advanced manufacturing techniques and economies of scale. On-board ASICs include memory controllers, networking, and serial and parallel communications, and a bus interface chip incorporating the VME64 specification. In addition, the MVME167 has both SCSI and Ethernet ports. Residing on a daughterboard module, the board includes 8 to 32 Mbytes of DRAM, 128 kbytes of SRAM and 512 kbytes of EPROM/EEPROM. The MVME167 is priced at $3,995.

Motorola Computer Group **Booth 924**
(800) 624-8999

VME board offers 64-kbit switching

The PRI-48 is an intelligent VME-based Dual T1 hardware/software platform that provides data formatting and 64-kbit switching. Maintaining frame integrity, the switch matrix can operate on time slots of both T1 spans, the data formatter and a local serial time-division-multiplexed highway accessed via the P2 connector. The PRI-48 can run as a stand-alone module or in a multiboard VME system. Software drivers implement both link-level and network-level protocols as specified by ANSI and CCITT, with

support concentrated on ISDN. The board is priced at $3,990 (100s).
Primary Rate **Booth 505**
(603) 898-1800

Military-rated VME enclosure

The 96 ATR-CD is a conductive cooled VME enclosure designed for survivability of system cards. Holding up to 16 6U VME boards, the unit features temperature monitors in power supply and card cage areas. To increase reliability and lower repair time, the enclosure is constructed with a minimal number of separate subassemblies. Designed to meet military requirements for temperature, shock and vibration, the unit meets MIL-STD-810E and several other military specifications. The chassis is available with a shock/vibration tray.
Prototek **Booth 418**
(513) 874-5094

VME embedded PC for control applications

The EPC-6 is a PC-compatible controller for the VMEbus that lets designers quickly embed PC-developed applications into VME-based systems. It can be used as a stand-alone PC or in tandem with other VMEbus CPU cards in a multiprocessing environment. Based on a 20-MHz 80386SX with 16 kbytes of cache, the EPC-6 includes Microsoft's ROM version of MS-DOS, 512 kbytes of flash EPROM, up to 4 Mbytes of DRAM, and two serial ports. Price is $1,995.
RadiSys **Booth 1213**
(800) 950-0044

SBus dual-port communications

The SB-302 is a dual-port adapter card for SBus systems that need an interface to serial lines running at speeds up to 2.048 Mbits/s. Supporting X.25, LAPB and other WAN protocols, the SB-302 uses a 20-MHz 68302 microprocessor for E1 speeds, and has a 16-MHz option for T1 requirements. Two serial ports support multiple protocols. Expansion modules enable each port to be independently configured to meet EIA-232D, EIA-449, EIA-530 or V.35 requirements. SunOS and X.25 device drivers are available to facilitate WAN connectivity on Sun workstations.
SBE **Booth 1107**
(415) 680-7722

VME CPU offers advanced I/O arrangement

Based on a 20-MHz or 30-MHz 68030, the TP34V is a single-board computer for VMEbus systems. To maximize I/O performance and offload the main CPU, all of the board's I/O controllers are advanced 32-bit

devices with local intelligence. SCSI and Ethernet interfaces reside on the TP34V main address and data buses. Comprised of 4, 8, 16, or 32 Mbytes of DRAM, the board's memory architecture supports the 68030's burst bus interface, sustaining a 44-Mbyte/s burst transfer rate, while providing a 22-Mbyte/s random access transfer rate at 33 MHz. Price of the 33-MHz version is $3,940.

Tadpole Technology **Booth 410**
(512) 338-4221

SCSI capabilities enhanced on VMEbus analyzer

The XMEM-PB is a SCSI-based piggyback module for use on the VBT-321B, VMETRO's bus analyzer for the VMEbus. Two new SCSI capabilities have been added to the XMEM-PB. First, an on-board SCSI host adapter has been added to support post capture storage of a single 64- or 256-kbyte trace into a Unix-compatible file structure. Second, a two-bank interleaved trace memory has been added to support real-time continuous storage of multiple XMEM traces. The enhanced XMEM-PB with SCSI host adapter and File System Firmware is priced at $2,850.

VMETRO **Booth 1121**
(713) 266-6430

486-based computer for the VMEbus

The XVME-687 is a complete PC/AT computer in a 6U double-wide VMEbus form factor. The board offers a 20-MHz 80486SX processor, both VMEbus and PC/AT bus interfaces, hard and floppy disk controllers, and a VGA graphics controller. Also featured are 4 to 16 Mbytes of dual-access DRAM, programmable byte-swapping logic, two serial ports, and a parallel port. Suitable for industrial applications, the board works under adverse temperatures, shocks and accelerations. Price is $5,400.

Xycom **Booth 210**
(313) 429-4971

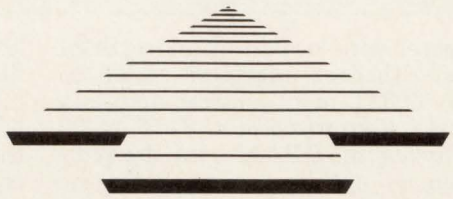
STD32, DSP motion controller runs at 10 Mips

Jointly developed by Ziatech and Delta Tau Data Systems (Canago Park, CA), the ZT8931 is DSP motion controller for the STD32 bus. Based on the 10-Mips Motorola DSP56001 chip, the board controls four axes of motion control, providing a 100µs servo update rate per axis. Comprised of a two-board sandwich, the ZT8931 requires an additional board to control eight axes. All axes can be controlled simultaneously, independently, or coordinated with each other. The ZT8931 controls DC brush, DC brushless, AC induction, stepper, and variable reluctance motors.

Ziatech **Booth 1029**
(805) 541-0488

Coming in January from COMPUTER DESIGN...

The Official BUSCON/92-WEST Show Guide



COMPUTER DESIGN and BUSCON team up to provide you with a complete Show Guide package before and during the show.

The Guide: The Guide will include the full exhibitor listing and descriptions, a dining and entertainment guide, a major value-added bus/board market overview and analysis— plus, a new products section— and inquiry card.

Value-added Editorial: This winter's official Buscon Show Guide, mailed with the January issue of COMPUTER DESIGN and distributed to all show attendees, will feature the usual show information — technical session descriptions and schedule, exhibitor listing, dining and events in the Long Beach, CA area — but will be enhanced by two editorial features of special interest to COMPUTER DESIGN readers, Buscon attendees and exhibitors:

- First is a marketing overview of the bus/board industry written by Warren Andrews. This overview will analyze the often confusing and contradictory data on the size of the board business and projections for its future development and growth.
- The second feature will be New Products, in which the products being introduced at Buscon, or which were introduced to the marketplace since Buscon/91-East, will be highlighted.

Distribution: The guide will be polybagged along with the Western portion of COMPUTER DESIGN's January issue for a total distribution of 50,000+. In addition, a special mailing will go to all of the pre-registrants...and it will be distributed to each attendee at the show.

Issue Date: January, 1992

Pricing: $2,200 Per Page — including color.

Savings Opportunity: Advertise in the February Show issue of COMPUTER DESIGN and save $500 per Show Guide page.

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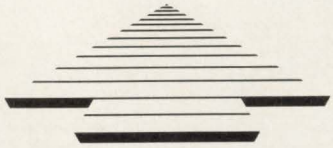

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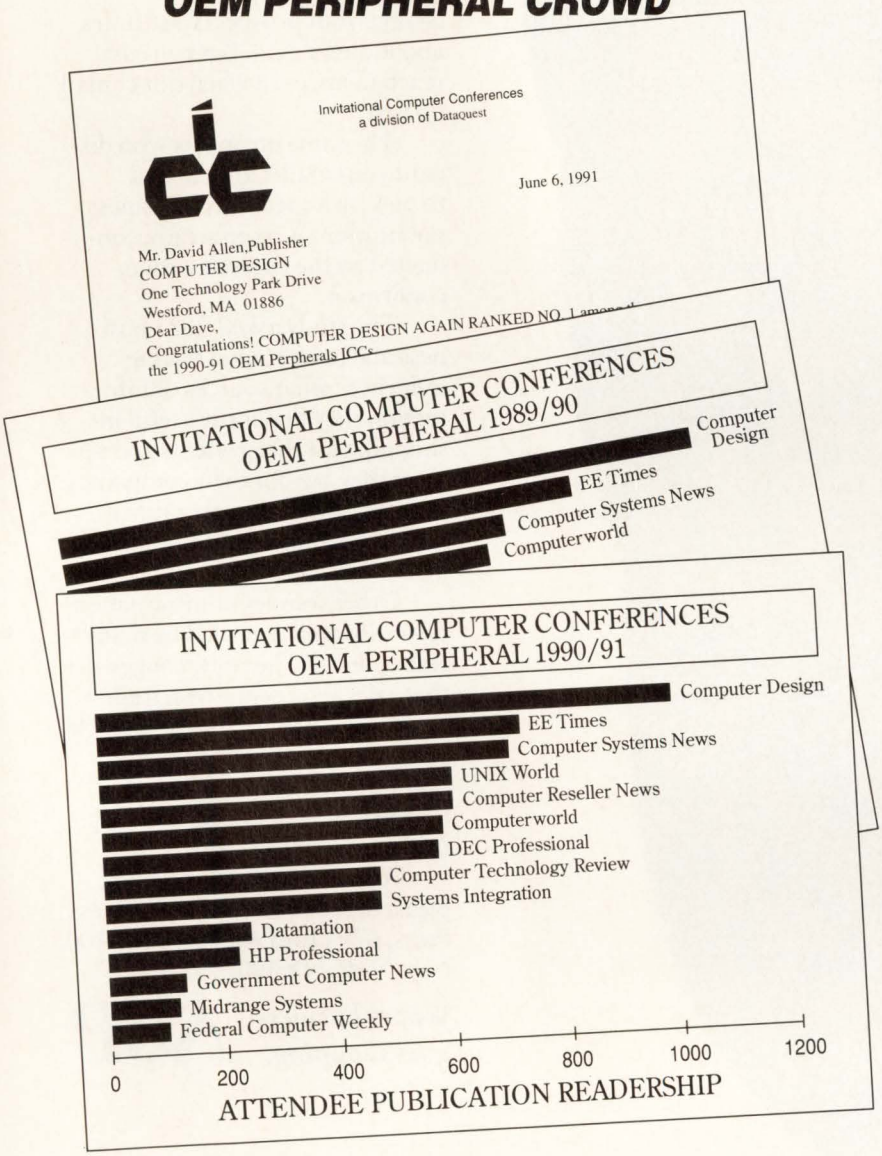

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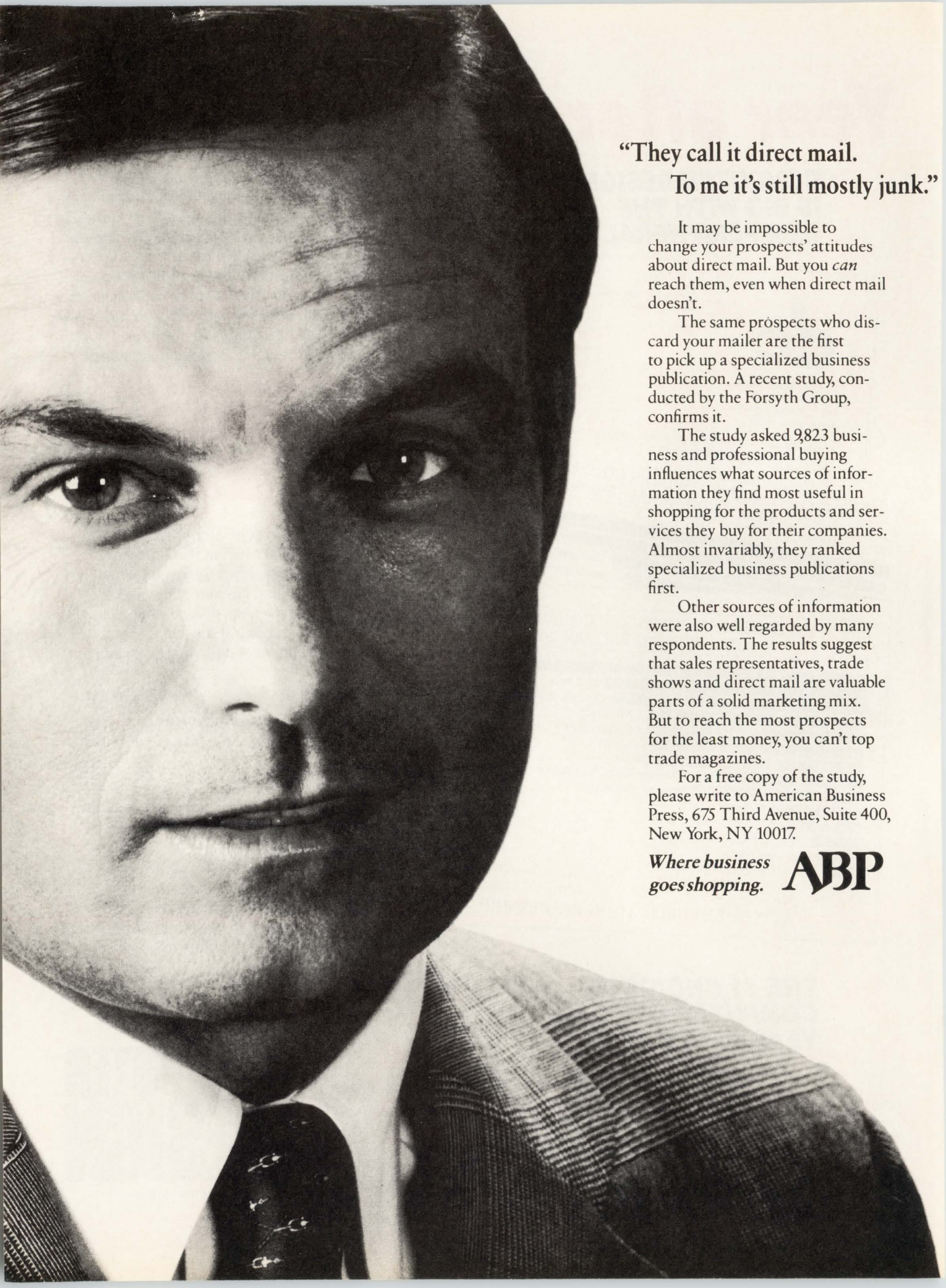

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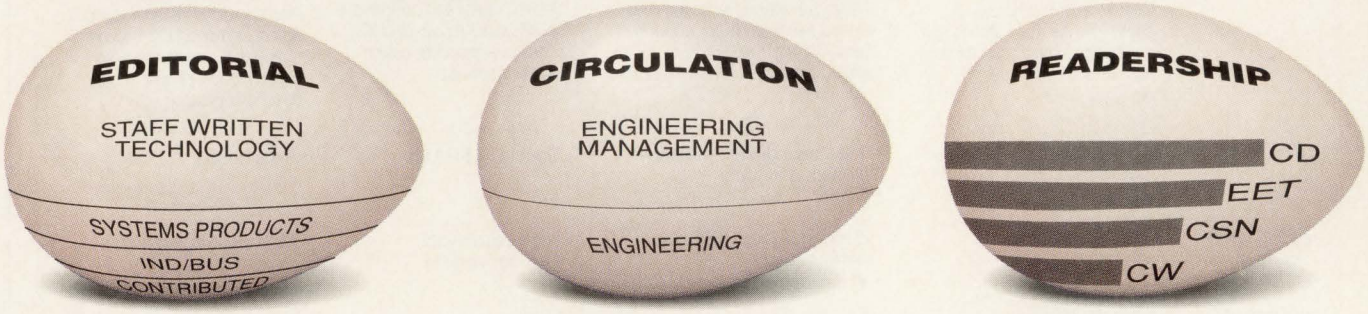

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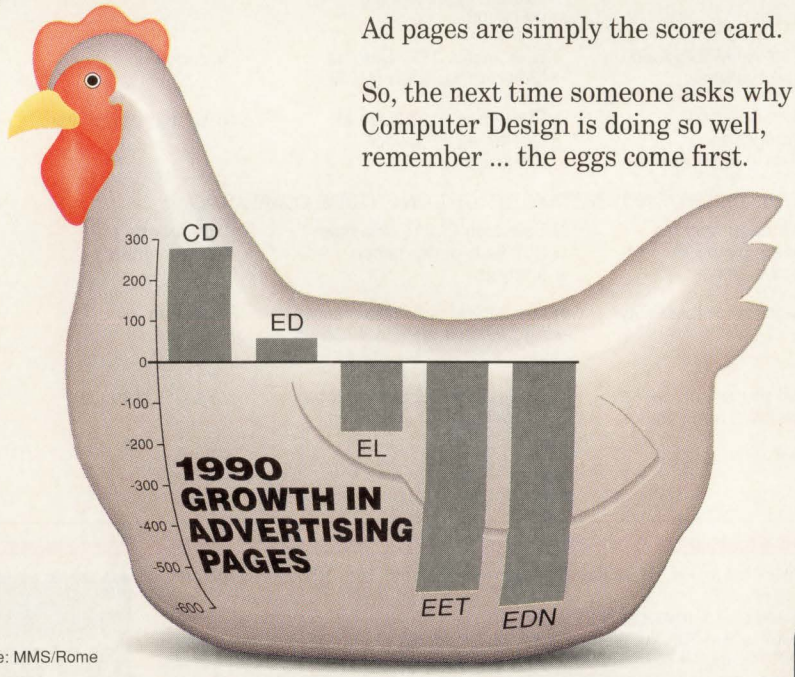

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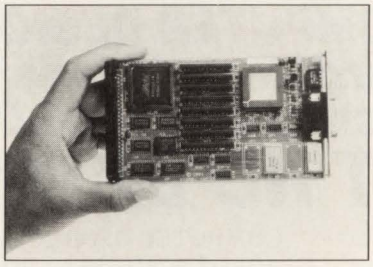

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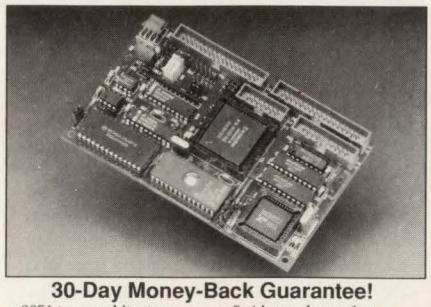

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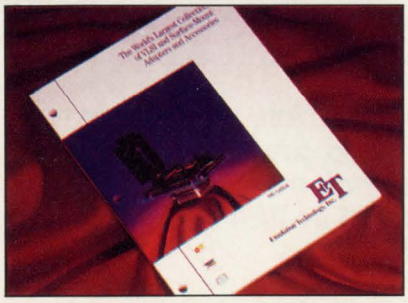

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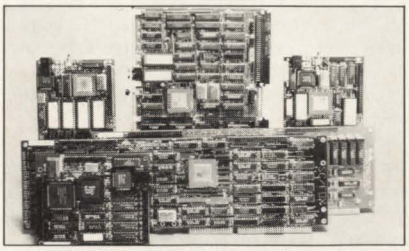

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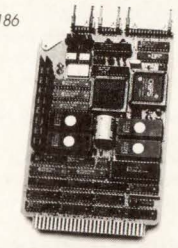

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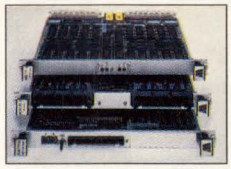

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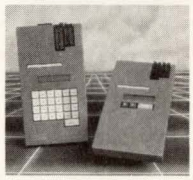

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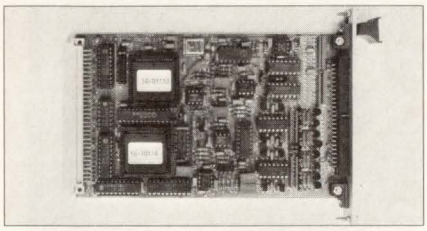

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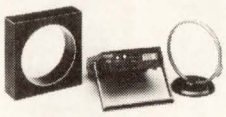

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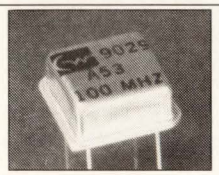

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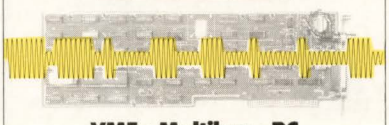

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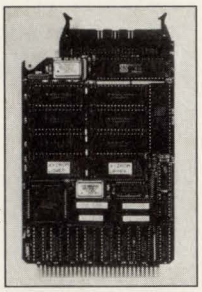

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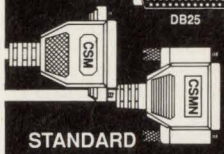

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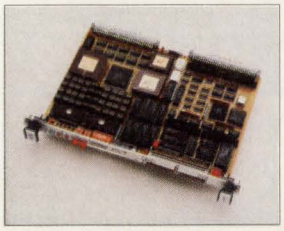

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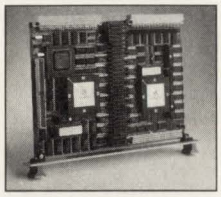

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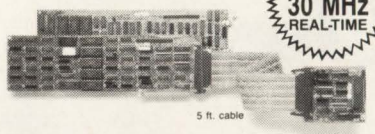

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COMPUTER DESIGN (ISSN-0010-4566) is published monthly by PennWell Publishing Company, 1421 S Sheridan, Tulsa, OK 74112. Second-class postage paid at Tulsa, OK 74112 and additional mailing offices. Editorial offices are located at One Technology Park Dr, PO Box 990, Westford, MA 01886. Annual subscription price: $88 in the U.S.A., $139 in Canada, $148 for Europe via air, and $192 other foreign via air. Call (918) 832-9263 for subscription information. Microfilm copies of COMPUTER DESIGN may be purchased from University Microfilms, a Xerox Company, 300 N Zeeb Rd, Ann Arbor, MI 48106. POSTMASTER: Send change of address form to COMPUTER DESIGN, Circulation Department, PO Box 3466, Tulsa, OK 74101.

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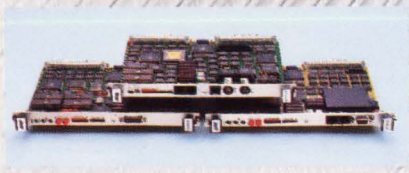

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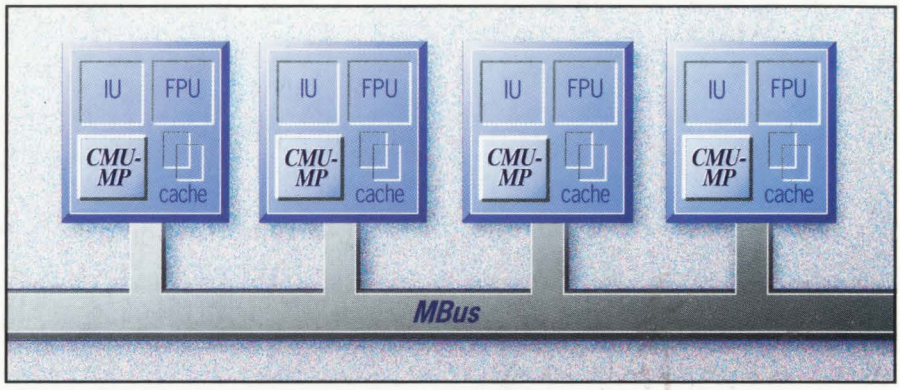

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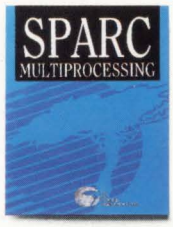

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