A PENNWELL PUBLICATION MAY 1992

COMPUTER DESIGN

Technology and Design Directions

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FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS

National Semi's Johnson on: Wireless Systems

Analog vs DSP: balancing speed and precision against cost

CAE vendors strive to improve link between design and layout

Minimizing energy consumption through power management

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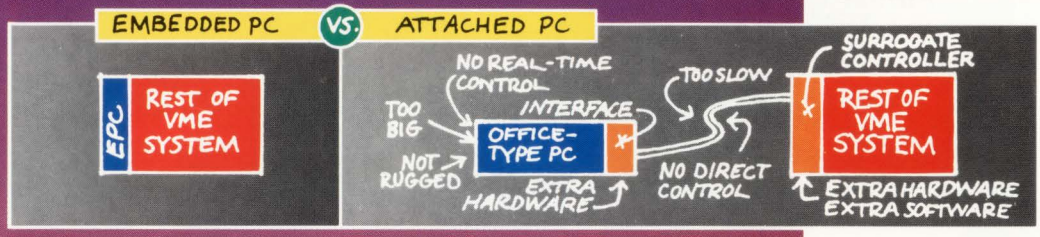
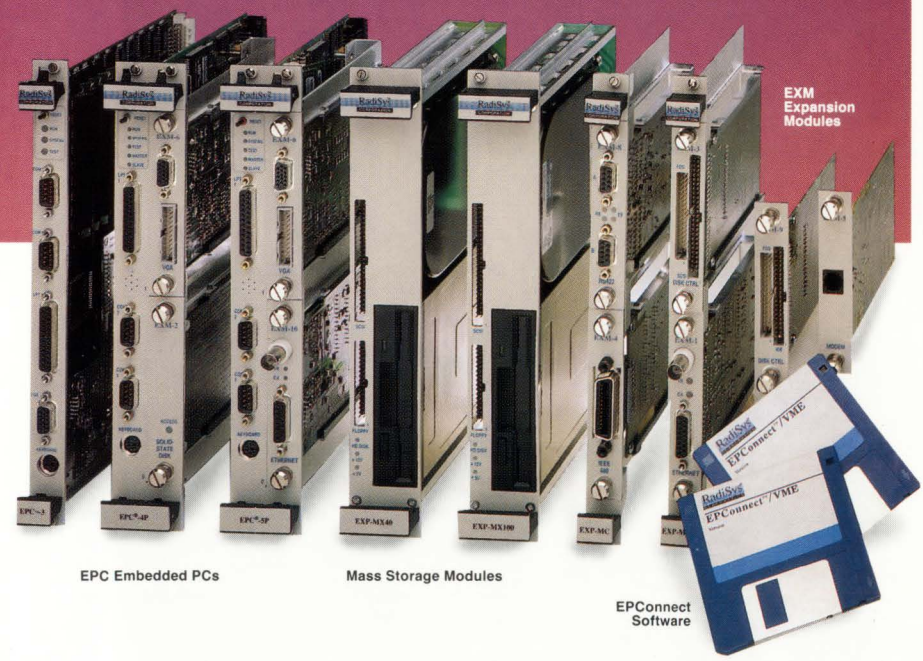
RADISYS GIVES VME THE INSIDE ADVANTAGE





Integrating a PC with your VME system is a smart move. The "PC advantage" provides a superior human interface and access to the PC's huge base of system, application and development software.

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EPC MODEL	EPC-1 (shipping since Aug '88)	EPC-3 (shipping since Aug '89)	EPC-4 (shipping since Mar '90)	EPC-5 (shipping since Oct '90)
Processor Modules:				
CPU	80386	80386SX	80386	80486
CPU Clock	16 or 20MHz	16MHz	25 MHz	25 or 33 MHz
DRAM	1 or 4 MBytes	1, 2 or 4 MBytes	4, 8 or 16MBytes	4, 8 or 16 MBytes
Graphics	EGA (640 x 350)	VGA (800 x 600)	VGA (800 x 600)	VGA (800 x 600)
Mass Storage Modules:				
Hard Disk Capacity	40 MBytes		40, 100 or 200 MBytes	
Floppy Drive Size/Cap.	3.5" / 1.44 MBytes		3.5" / 1.44 MBytes	
Expansion Capabilities:				
PC Add-in Cards	Yes		Yes	
EXMbus Expansion	N/A	EXM Expansion Modules:		
		EXM-1 Ethernet	EXM-5 Modem	EXM-9 IDE/Floppy Ctrl
		EXM-2 Solid State Disk	EXM-6 VGA Graphics	EXM-10 Ethernet
		EXM-3 SCSI/Floppy Ctrl.	EXM-7 RS232 Serial I/O	EXM-11 Timer/Counter
		EXM-4 IEEE 488	EXM-8 RS422 Serial I/O	EXM-12 Prototyping Card
Software Support:	EPConnect development, run-time, and multiprocessing software package for DOS, Windows, UNIX,and OS/2			

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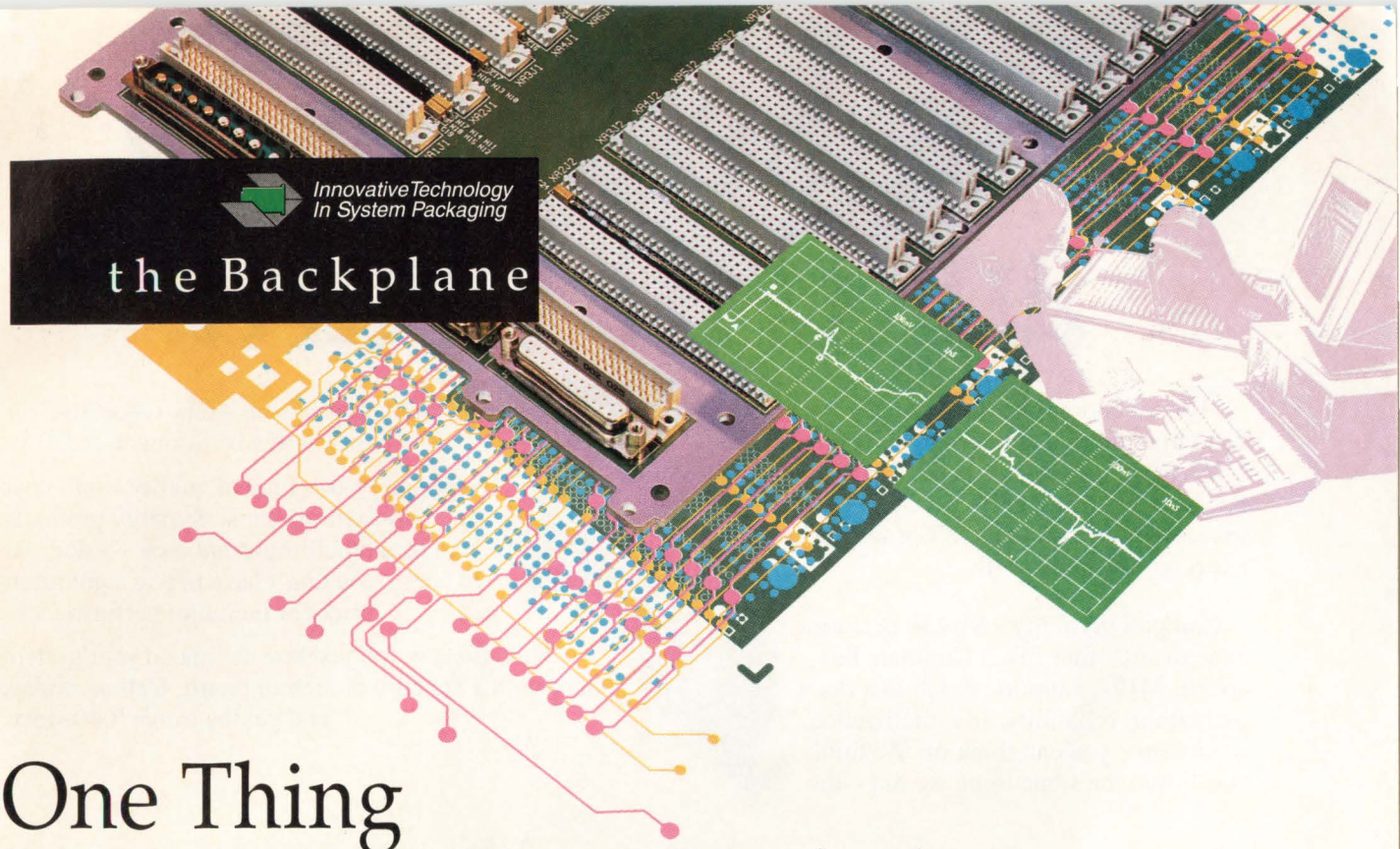
CIRCLE NO. 1



One Thing Separates a Great Backplane from a Good One.

It's the innovative application of cutting-edge technology to your specific requirements. It's what we do at Electronic Solutions.

There was a time when a backplane was little more than a few connectors mounted to a simple pc board. But today's higher performance systems require higher performance multilayer backplanes. Someone has to resolve the difficult issues faced in designing a backplane that will handle your high-speed system—a balancing act between design parameters that affect crosstalk, reflections, impedance, ground shift, and power distribution.

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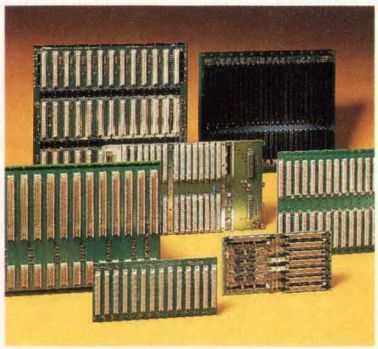
For industry standard backplanes such as VME, Multibus I or II, Sun, VXI, or Futurebus+ we have a line of high performance backplanes available off the shelf. Our backplanes have been independently tested and ranked as the "Best Balanced" backplanes available.



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VXI bus
Sun bus
Multibus I
Multibus II
Futurebus+
Mixed buses
Proprietary buses

For proprietary backplanes, no matter how exotic or unusual, we'll apply the same design expertise exemplified by our standard products and build you a backplane tailored to your specific requirements.

Let us prove it to you! Just call and request information on our backplane design capabilities and we'll FAX the FACTS right to you. Or ask to talk to one of our Applications Engineers who will help you translate your requirements into a backplane spec.

For standard or proprietary applications, there's only one way to get a backplane that's just right for your system. That's to call Electronic Solutions and put our experience to work for you.

One example of our design innovation is our patented **Active Automatic Daisy Chaining** which eliminates the number one field service probem— improperly placed Bus Grant Jumpers. It's superior to the passive auto-daisy chaining touted by other vendors, and it's available *free of charge* on our new VME backplanes.

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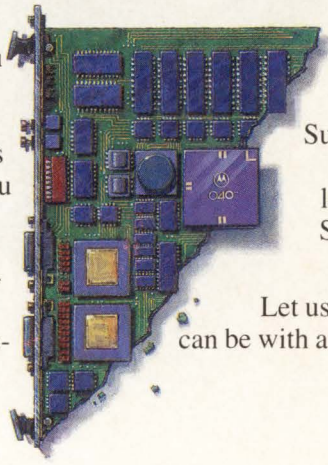
CIRCLE NO. 2

Why Settle for ½ an '040 Board?

You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may only give you only half of what you expected from the '040.

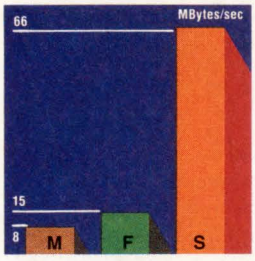
Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPs, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the SV430 outperforms every other SBC on the market by as much as 150%.



Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

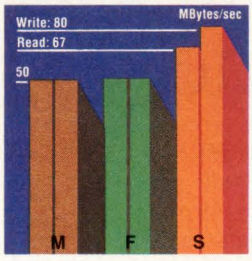
Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

Compare our specs. Synergy is superior across the board!



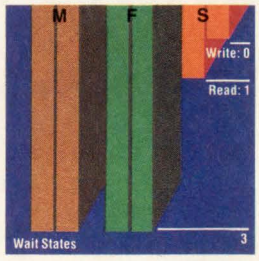
VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



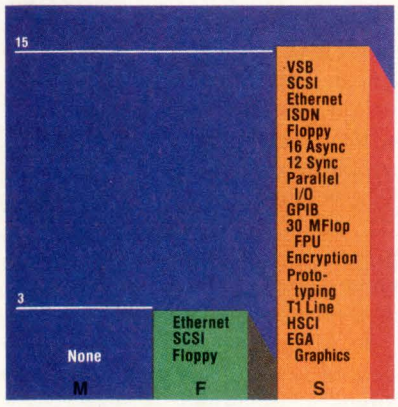
DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



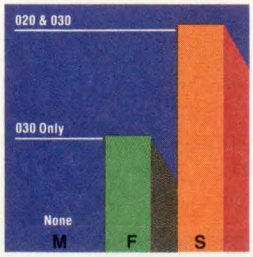
DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.



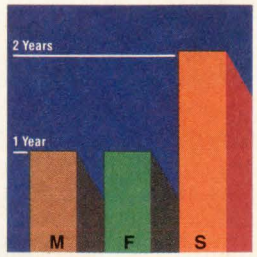
I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.



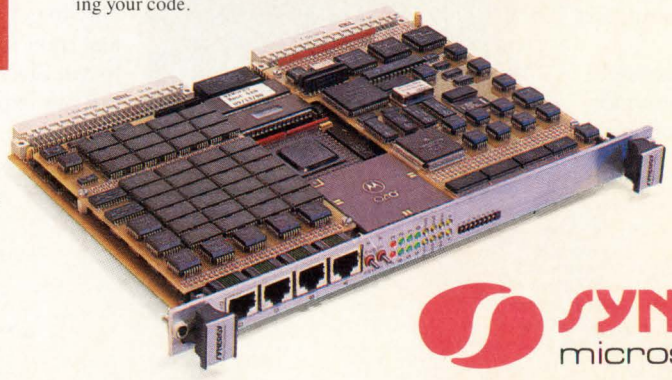
'020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.

SYNERGY microsystems

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CIRCLE NO. 3

A PENNWELL PUBLICATION VOL 31, NO 5 / MAY 1992

COMPUTER DESIGN

Technology and Design Directions

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS

This month's cover story probes some of the trade-offs involved in choosing analog versus digital techniques for signal conditioning and processing. As usual, the illustration has some buried symbolism. Why not see if you can find it all **83**

Illustration by Bill Morrison

NEWS BRIEFS

TECHNOLOGY DIRECTIONS

Computers & Subsystems

Integrated Circuits

CAE/CAD Tools

Software & Development Tools

NEW PRODUCT DEVELOPMENTS

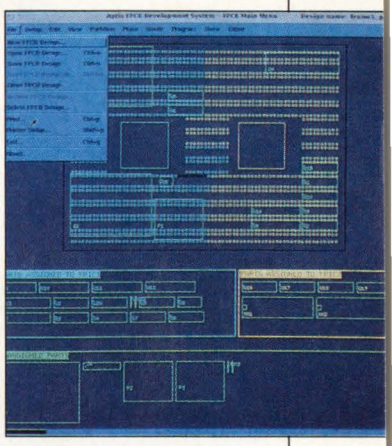
Integrated Circuits

Software & Development Tools

CAE/CAD Tools

ASICs & ASIC Design Tools

MORE ON PAGE 5



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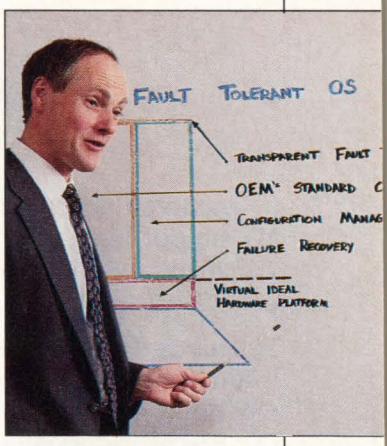

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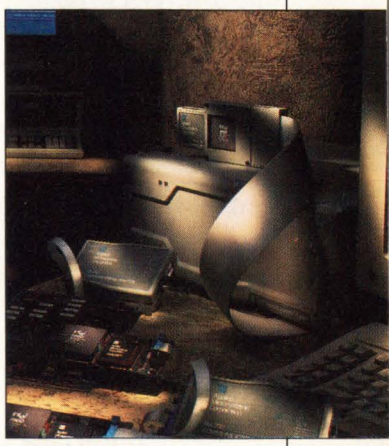

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Designing with Motorola's

Microprocessors?

Then you need HMI's development systems. We support the entire 68000 family. As Motorola enhances and increases integration of its microprocessors, you can count on HMI to be there with high-quality development products to support your projects. HMI believes in supporting the entire family of products for the Motorola family. Ease of use and familiarity are common in all the emulators.

Features of HMI's development systems includes:

- Run at real-time with no wait states.
- Window driven source level debugging—SourceGate®
- C, Pascal and ADA compiler source level support for all major compiler companies.
- Real-time hardware performance analyzer.
- Works with IBM PC family and UNIX based machines including Sun and Apollo.
- RS232 Interface up to 115.2K.
- Parallel Interface for high-speed code downloading.
- Complex events and sequences for break and trigger conditions.
- Two independent 4K deep trace buffers.
- 1 μsec resolution interval timer.
- 100 nsec resolution Time-stamp in trace buffer.
- Logic state analyzer capabilities built into the emulator.
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If you are looking for one emulator company that provides support for the entire Motorola family, then look to HMI for total support. Write or call for further information and *free* demo disk.

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CIRCLE NO. 4

A PENNWELL PUBLICATION VOL 31, NO 5 / MAY 1992

COMPUTER DESIGN

Technology and Design Directions

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS

CONTINUED FROM PAGE 3

National Semi's Gary Johnson on: Wireless systems
The same highly charged spirit of innovation and global competition that led to the development of radio a hundred years ago resonates in today's wireless communications design community 25

TECHNOLOGY & DESIGN REPORTS

CAE vendors strive to improve link between design and layout

The walls that once insulated PCB designers from manufacturing are crumbling. But whether the responsibilities that go along with the change will be accepted remains to be seen. —*Mike Donlin* 57

Minimizing energy consumption through power management

Battery-powered portables will benefit from 3-V ICs, but system-level design priorities such as clock speed and use of a disk drive, rather than the 3.3- versus 3.0-V LVCMOS standard, will have more effect on cumulative power consumption. —*Stephan Ohr* 69

COVER STORY

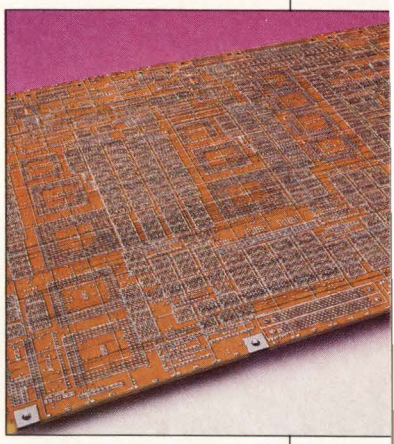
Analog vs DSP: balancing speed and precision against cost

There are many applications where an analog approach is best in terms of accuracy, speed and cost. But the proliferation of higher-speed components, signal processing algorithms and easy-to-use development tools will soon make DSP the solution of choice. —*Stephan Ohr* 83

PRODUCT FOCUS

RISC chips continue conquest of embedded realm —*Jeffrey Child*

Promising greater performance through pipelining, multiple execution units and more efficient code execution, RISC processors have won design win after design win. Setting their sights on the lower-end, cost-sensitive embedded systems, RISC chip vendors are expanding their product lines to fit a wider range of price and performance. 103



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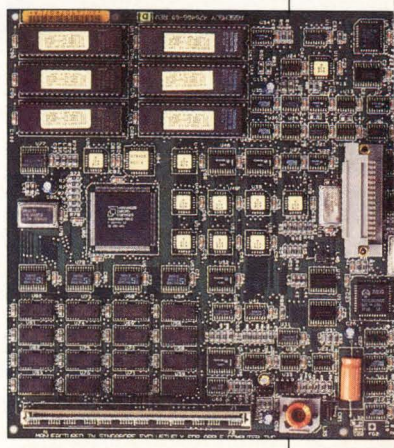

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COMING NEXT MONTH

Integrating PC-based tools into the design environment

I/O buses and interfacing

Real-time kernels and OS's

Workstations

Now you can afford to

Presenting a very small development in Ethernet.*

Chipsets that are matched to your system and your budget. In fact, they cost you as little as 5 square inches. Which, by the way, is less total real estate than any competitive solution. But sizable reductions don't stop with board space, because we're also reducing the price up to 30 percent.

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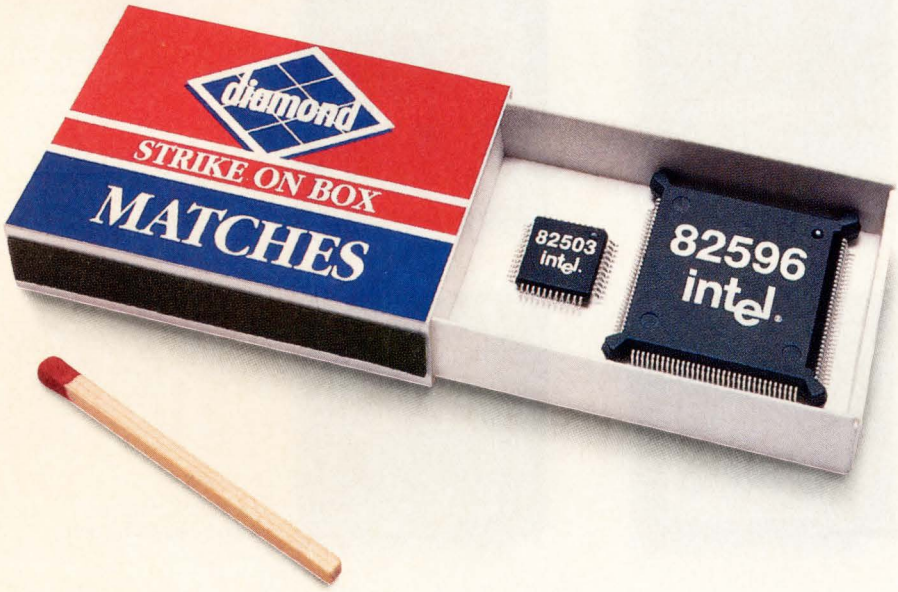

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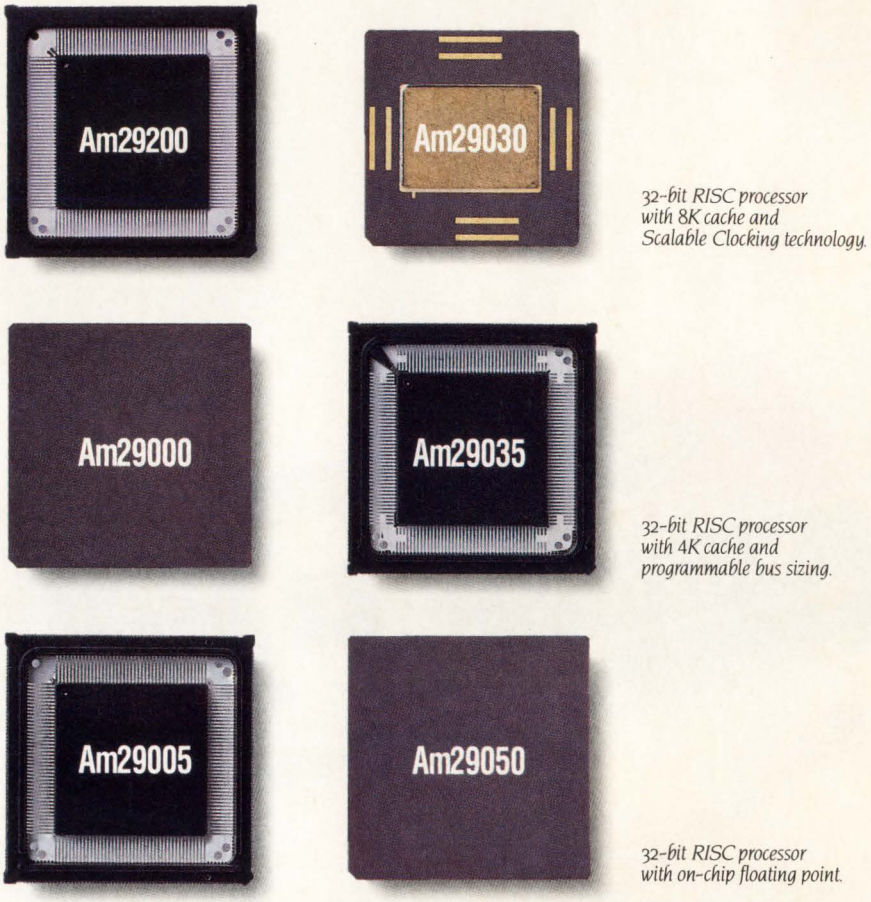

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The 29K Family.

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Advanced Micro Devices

CIRCLE NO. 6

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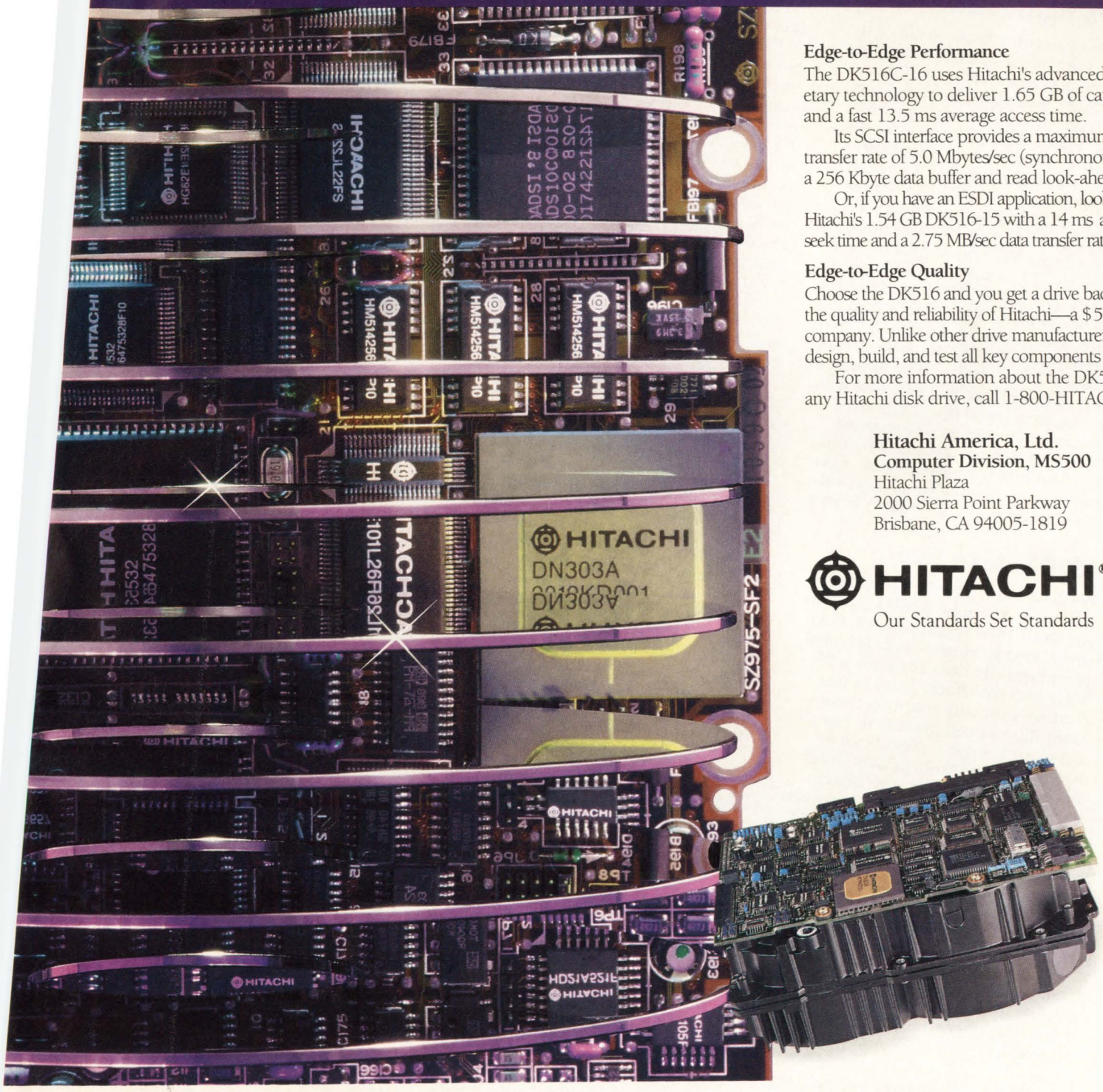

Edge-to-Edge Performance

The DK516C-16 uses Hitachi's advanced proprietary technology to deliver 1.65 GB of capacity and a fast 13.5 ms average access time.

Its SCSI interface provides a maximum data transfer rate of 5.0 Mbytes/sec (synchronous), with a 256 Kbyte data buffer and read look-ahead cache.

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CIRCLE NO. 9

MIPS fights back

MIPS Computer Systems (Sunnyvale, CA) has described a number of new processors that will be available later this year and has outlined plans for future processors. The R4000 processor family will hit 75-MHz clock speeds by year-end, then move to 100 MHz by 1993. By mid-1993, the R4000 will be followed by the R5000, a part that will offer 150 Specmarks of performance. One year later will come the T5, a superscalar implementation of the MIPS architecture.

For its part, NEC (Mountain View, CA) plans to develop a 2-W, 80-MHz version of the R4000, dubbed VRX, that will be available in the second half of 1993; this will be complemented by a high-end floating-point device, codenamed TFP, that will be developed by Silicon Graphics (Mountain View, CA) and made available by several silicon vendors. *—Dave Wilson*

486DX: take two

While it runs at a 50-MHz internal clock, the new 486DX2 processor from Intel (Santa Clara, CA) interfaces to slower motherboard peripheral devices through a 25-MHz bus interface. Intel hopes that by isolating manufacturers from high-speed system design issues, midrange systems can be brought to market quickly. Intel notes, however, that the higher core speed of the 486DX2 may conflict with existing system designs. The 486DX2 consumes about 40 percent more power than a 33-MHz 486 CPU; consequently, DX2-based designs may require more cooling. Furthermore, the higher core speed may cause problems for software that uses instruction loops for timing. Some BIOS code, for example, uses such loops to time the operation of peripheral devices. *—Dave Wilson*

AT&T expected to reveal details of FPGA silicon and software

Later this month we can expect to learn more about AT&T Microelectronics' (Allentown, PA) much-touted FPGA silicon and design tools, to be available third quarter. Though it's been producing logic cell arrays through an agreement with Xilinx (San Jose, CA), AT&T has been claiming that none of the FPGA architectures or tools have been optimized for performance or migration. As a broad-line silicon vendor, offering gate array and cell-based technologies as well as FPGAs, AT&T contends it's in a position to offer state-of-the-art silicon technology (down to 0.5-µm, perhaps?) as well as software tools closely coupled to FPGA architecture and a flexible migration path to and from other silicon technologies.

AT&T has intimated that its FPGAs will be reconfigurable and will have a coarse-grained architecture with the option to configure as several small grains. The FPGAs are likely to have 15,000 to 20,000 gates and more than 200 I/Os. As for tools, we can expect AT&T to offer an end-to-end design capability including ASIC-like timing tools such as static timing and hazard analysis, plus timing-driven map, place and route tools.

Though a proponent of user-defined benchmarks for FPGAs, AT&T has not yet joined Programmable Electronics Performance (PEP), the new semiconductor benchmark industry association of PLD, FPGA and design tool vendors establishing speed and functional capacity benchmarks for their products. *—Barbara Tuck*

Verilog and VHDL to coexist rather than compete?

Verilog proponents have adopted a new strategy toward VHDL: "If you can't fight 'em, join 'em." Rather than focusing efforts on slowing the momentum of VHDL, Open Verilog International (OVI) members are now studying the possibilities of interoperability between the two languages. Verilog and VHDL do, after all, appeal to users for different reasons, and it's expected that many users will be involved in parallel development efforts for some time to come. Certainly, from a user's point of view it would make more sense to put less emphasis on which of the two languages is used and more on how VHDL and Verilog might work together, at least over the short term.

VHDL backers will no doubt be discussing their reactions to the possibility of interoperability with Verilog this week at the spring meeting of the VHDL International (VI) Users' Forum. The choice of Cadence Design Systems' (Lowell, MA) Joe Costello as keynote speaker there indicates that VI has also softened its attitude from a year ago, when Cadence's intimate association with Verilog was seen as reason to exclude it from an invitation to be a founding VI member. Since then, Cadence has come into possession of a seat on the founding members' board through its acquisition of Valid.

VHDL pioneer CLSI/Solutions' (Concord, MA) decision to join OVI also indicates that vendors won't back one language to the exclusion of the other. CLSI will, in fact, market and support the Cadence-developed Open HDL Toolkit, which eases the development of Verilog-based design tools, more and more of which are becoming available. *—Barbara Tuck*

Model vendors to merge

The two leading providers of simulation models, Logic Automation (Beaverton, OR) and Logic Modeling (Milpitas, CA), have agreed to merge into a company that will become the industry's largest source for software and hardware component models. The combined company, called Logic Modeling, will continue to support the software simulation models of Logic Automation and the LM hardware modelers from Logic Modeling.

Both companies have long held that hardware and software modeling are complementary, rather than competitive, technologies and have been conducting joint marketing for some time. "We know that designers want to do more board simulation," says L. Curtis Widdoes, president of the new Logic Modeling, "but the lack of a comprehensive modeling solution has been hindering those efforts. We believe that our merged company can remove model availability as a barrier towards simulation."

William Lattin, who was president and CEO of Logic Automation, will be CEO and chairman of

Continued on page 14

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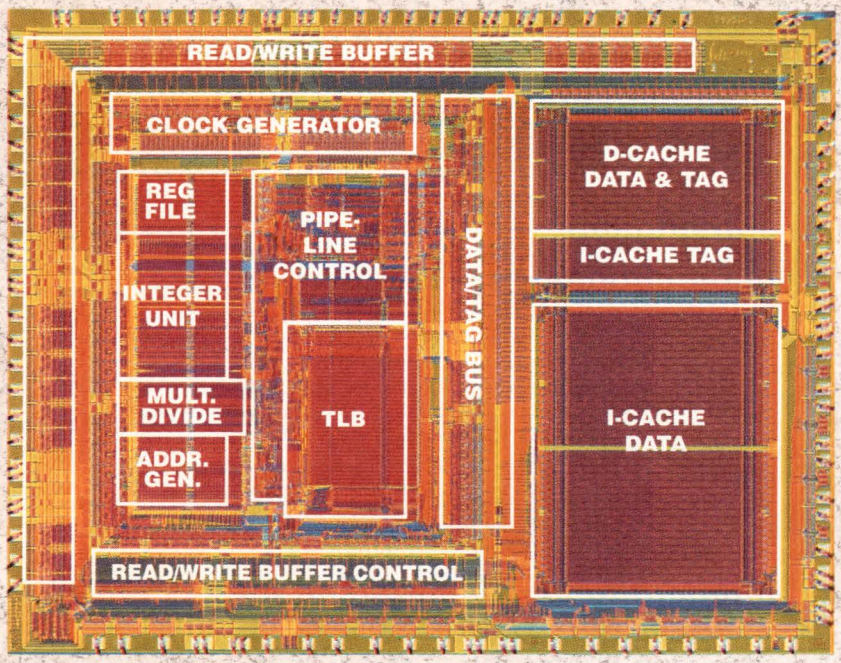

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CIRCLE NO. 11

Continued from page 12

the board for the new Logic Modeling and will focus on sales and marketing. *—Mike Donlin*

Verilog intensifies standardization efforts

The Verilog standardization effort is entering a critical phase that will include a push for IEEE approval, according to Bruce Bourbon, chairman of Open Verilog International (OVI) and president of Vertex Semiconductor (San Jose, CA). Addressing attendees at this week's OVI users' group meeting, Bourbon announced plans to work with the IEEE Design Automation Subcommittee toward standardization and approval of Verilog. Another priority for OVI is model interoperability between Verilog, VHDL and proprietary languages. Though these efforts will require a large amount of flexibility and openness from the Verilog camp, Bourbon reassured the group that any additions to the language will preserve core Verilog features and users' investment in existing model libraries.

There was a cautionary note from computer pioneer Gordon Bell, keynote speaker at the meeting. "You may not want the IEEE involved in your thing," Bell warned. "It's the world's third most bureaucratic organization, aside from the government and the Defense Department."

—Mike Donlin

Massively parallel

With the rash of RISC processors, as well as multi-chip modules (MCMs) comprising processors, cache, memory management, cache-coherent bus, and other goodies, promising dramatic performance gains, the race for massively parallel machines is on. Regardless of who the winners will be, VMEbus might well be one of the peripheral beneficiaries.

It's believed that VME may be the I/O board of choice for a number of emerging machines from Cray, Dolphin, Harris, Motorola, and others. In addition, there are hints that at least one company plans to use conventional 6U VMEbus cards with as many as 32 individual processors per card, each with massive amounts of memory.

All the major RISC architectures will be represented. Motorola's 88110 will be spoken for by Harris, Dolphin and probably Motorola itself in its own massively parallel processor (MPP). Digital Equipment's new Alpha architecture will be the core of Cray's first massively parallel machine, according to a wide-ranging marketing and technology exchange agreement between the two companies. Hewlett-Packard is also getting in on the act with its PA (Precision Architecture). A recent deal secured HP a 5 percent share in Convex Computers, which is reportedly working on a—you guessed it—PA. Not to be left out, IBM has made a deal with Bull for its RISC 6000 chip set, ostensibly to be used in a parallel machine. Sparc, too, has its followers, some of whom are well along—for example, FPS Computers. And Intel, with its stake in Alliant Computers, will also be in the running. *—Warren Andrews*

Silicon Graphics' 3-D language spreading to other platforms

Standards aren't always produced by committees; they sometimes issue from a single source and are simply accepted because they're complete, stable and useful. The only serious contender for a 3-D standard to date, PHIGS and its X Windows version, PEX, appear now to be challenged by GL Graphics Library, which was developed by Silicon Graphics (Mountain View, CA). Silicon Graphics has made its IRIS GL 4.0 available for porting to other platforms.

At least two licensees of Silicon Graphics appear to be bent on porting GL to the Sparc workstation world and beyond. DuPont Pixel (Newark, DE) has developed a version of GL for the Intel i860, and is now offering an i860 SBus accelerator for Sun workstations that runs GL fully integrated with Sun's window environment. In the near future, DuPont Pixel will be offering GL to run as native code on the Sparc processor, without needing the SBus board. Nth Graphics (Austin, TX) has already ported GL to the Sparcstation, compatible with the X-11 version of X Windows, so that it will run in either the Motif or Open Look versions of X Windows. While nobody is saying so openly, the probability of GL appearing on other processors is quite high.

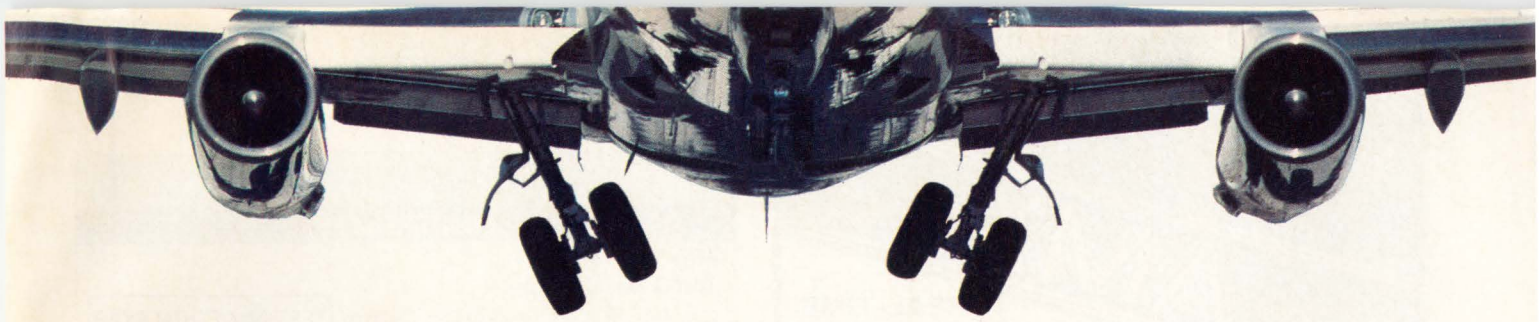
—Tom Williams

Equipment sales may buoy Sematec prospects

Sales of U.S.-made semiconductor production equipment showed a significant increase in 1991, putting the share of the market for U.S. manufacturers about even with the Japanese. This may represent a recovery, after a long decline from American dominance in the 1980s. Each country now has about 47 percent of the world market. It's a little early to extrapolate a conclusion from this—for example, that the semiconductor industry is making a comeback. The Japanese, who purchase all but a few systems from Japanese suppliers, have limited capital investment due to a drop in demand for memory.

The figures, however, are making a case for the effectiveness of the Pentagon and a privately funded consortium, Sematech, whose charter is to help U.S. semiconductor manufacturers improve and develop fab equipment. The news comes at a favorable time for Sematech, which is trying to maintain its approximately $200 million a year in financing.

—Tom Williams



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CIRCLE NO. 12

CALENDAR

CONFERENCES

May 11 - 14
Test & Design Expo

Garden State Convention Center, Somerset, NJ. The Test & Design Expo is the first show to revolve around the concurrent engineering process. Test equipment and design products will be showcased side-by-side on the exhibit floor. The conference will feature sessions, tutorials and mini-courses that are structured for test and design professionals, emphasizing concurrent engineering, boundary scan and VXI/systems integration. Contact: Miller Freeman Expositions, 1050 Commonwealth Ave, Boston, MA 02215-1135, (800) 223-7126, Fax (617) 730-5708. **Circle 366**

May 12 - 14
Electro/92 International

Hynes Convention Center, Boston, MA. This show focuses on software in the engineering environment. There will be 60 technical sessions on semiconductor device technology, software engineering, computer automation systems, and more. There will be six all-day technical courses on such topics as "Programming with the X Windows system." Five management seminars will also be held. More than 800 exhibits, plus a special HDTV demonstration, will also be featured. Contact: Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045, (800) 877-2668, Fax (213) 641-5117.

Circle 367

May 18 - 22
Interop 92 Spring

Washington Convention Center, Washington, DC. The 7th Interoperability Conference & Exhibition has been divided into deployment and technology tracks. The deployment segment has 25 sessions on SNA integration, ODA, EDI, CALS, and several case studies. The technology segment has 30 sessions on OSI network management, LAN/WAN integration, Gigabit LANs, and more. There will be a special track titled "PC LAN in the corporate network." This session will be devoted to TCP/IP connectivity, NFS integration, SNA gateways, and more. Contact: Interop, Inc, 480 San Antonio Rd, Ste 100, Mountain View, CA 94040-1219, (415) 941-3399, Fax (415) 949-1779.

Circle 368

June 8 - 12
DAC

Anaheim Convention Center, Anaheim, CA. The 29th Design Automation Conference is geared toward electrical engineers, computer scientists and management and will offer technical programs, tutorials and vendor exhibits. New at DAC are sessions on real-world EDA user problems/solutions targeted at high-level company executives. User sessions include "Why is today's CAD inadequate for designing tomorrow's computers?" Contact: MP Associates, 29th DAC, 7490 Clubhouse Rd, Ste 102, Boulder, CO 80301, (303) 530-4333, Fax (303) 530-4334. **Circle 369**

Continued on page 18

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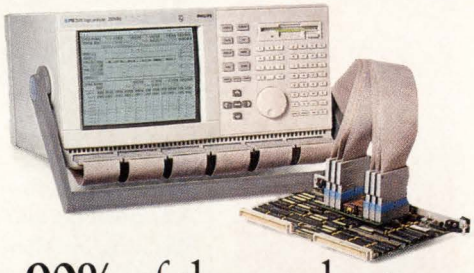

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CIRCLE NO. 15

CALENDAR

CONFERENCES

Continued from page 16

June 16 - 18
Nepcon East '92

NATIONAL ELECTRONIC PACKAGING AND PRODUCTION CONFERENCE NEPCON

Bayside Exposition Center, Boston, MA. This conference will feature products and technologies for design, fabrication, assembly, packaging, inspection, and test of printed circuits and electronic assemblies. Technical session topics address surface-mount technology, pollution problems when switching from solvent cleaning, concurrent engineering, and surface-mount components. There will also be a workshop on low-volume SMT. Contact: Reed Exhibition Companies, Cahners Plaza, 1350 E Touhy Ave, Des Plaines, IL 60018, (708) 299-9311, Fax (708) 635-1571. **Circle 370**

June 23 - 25
AFCEA 46th International Convention & Exposition and ITEMS '92

AFCEA

Washington Convention Center, Washington, DC. This convention is the world's largest communications, intelligence and information systems event. The show focuses on professional development and information exchange for military, government and industry personnel. Panel topics include: "The electronic battlefield: tomorrow's approach to training, rehearsing and testing," and others. Also AFCEA will launch Imaging Technologies & Evolving Management Systems Conference and Exposition (ITEMS), featuring the latest imaging software and hardware. Contact: AFCEA Programs Office, AFCEA International Headquarters, 4400 Fair Lakes Ct, Fairfax, VA 22033-3899, (703) 631-6125, Fax (703) 631-4693.

Circle 371

June 23 - 25
Tenth Annual PC EXPO

PC EXPO

Jacob K. Javits Convention Center, New York, NY. This 10th annual trade show and conference focuses on the latest computer hardware and software, including graphical user applications, multimedia, pen computing, and connectivity. The seminars will feature in-depth tutorials on the latest computer trends. Contact: Bruno Blenheim, Inc, Fort Lee Executive Pk, One Executive Dr, Fort Lee, NJ 07024, (800) 829-3976, Fax (201) 346-1602. **Circle 372**

June 30 - July 3
HIIPC '92

HIIPC'92

Sheraton Waikiki Hotel, Honolulu, Hawaii. The Hawaii Intergovernment Information Processing Council's 7th annual information management conference and exposition. Comprehensive programs will be geared toward managers and end users. HIIPC's objective is to provide high-quality, low-cost training on current and emerging information resource management technologies and issues. Seminars and product briefings will be given by government and industry leaders. Contact: HIIPC '92, c/o J. Spargo & Assoc, 4400 Fair Lakes Ct, Fairfax, VA 22033, (703) 631-6200, Fax (703) 818-9177. **Circle 373**

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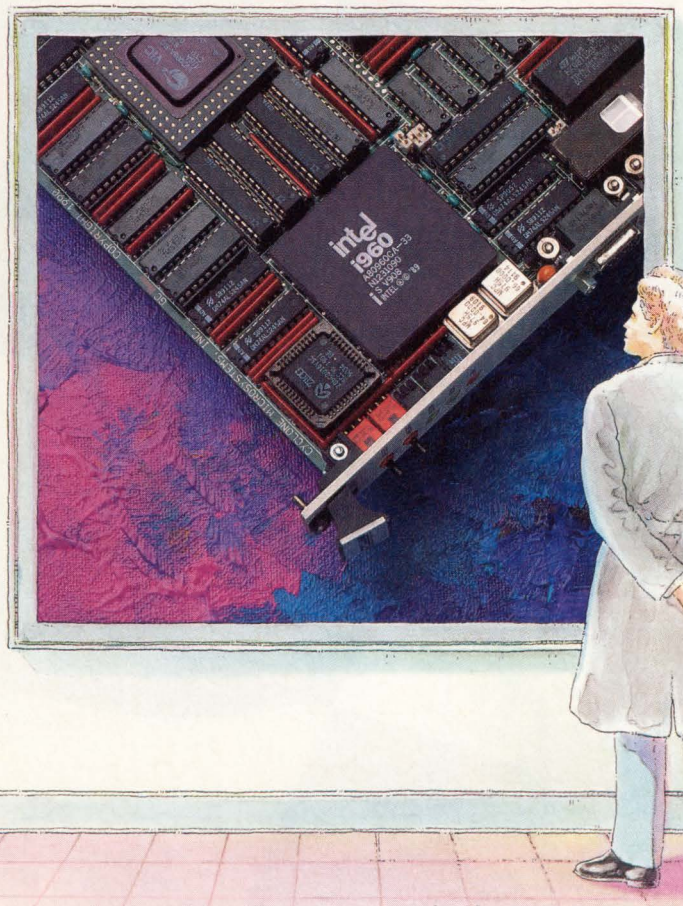

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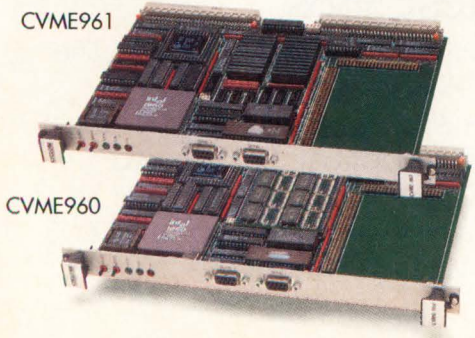

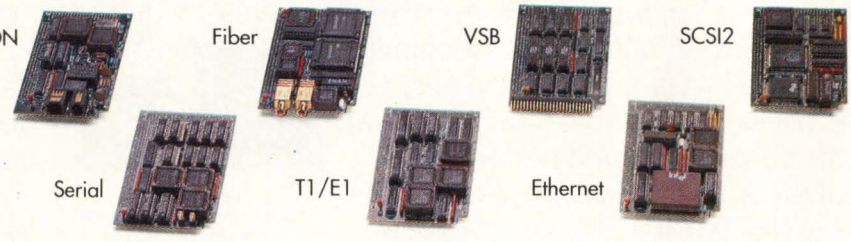

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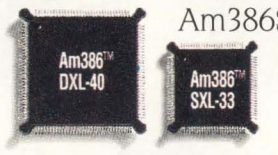

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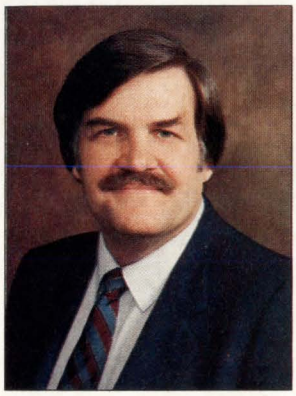

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Sorting the facts from the fiction in advertising claims, promotional material and the statements of enthusiastic salesmen has never been easy. Unfortunately, design engineers and engineering managers in the OEM computer/electronics business don't have the equivalent of a *Consumer Reports* that they can turn to. The PC world, on the other hand, has been more fortunate in that all of the major publications have test labs that run personal computers, peripherals and software through their paces. We don't have the equivalent on the OEM side of the business simply because the great diversity of products, in type and complexity (from ASICs to microprocessors to peripheral chips to single-board computers to workstations to synthesis tools to simulation to layout to real-time kernels to compilers to etc., etc. etc.) makes it prohibitively expensive for any publication to run comprehensive performance evaluations.

The next best thing to the benchmarks and performance figures generated by a *Consumer Reports*, a *Byte* or a *PC Magazine* are benchmark criteria developed and subscribed to by a consortium of hardware and software vendors under the leadership of an objective third party. The Programmable Electronics Performance (PEP) consortium, with initial funding and staffing provided by one of our competitors, *Electronic Engineering Times* (I'll give credit where credit is due, even if it hurts my ego), has been set up to do just that for programmable devices. PEP's charter members are Actel, Advanced Micro Devices, Altera, Cypress Semiconductor, Data I/O, Lattice Semiconductor, QuickLogic, Texas Instruments, and Xilinx. The goal of the consortium is to develop a suite of benchmark circuits that a designer can use to evaluate the capacity and speed of devices ranging from small PALs through the largest FPGAs.

The benchmark circuits in the PEP suite include small and large state machines, counters, arithmetic functions, and data path elements. The benchmark circuits were selected to show individual device strengths, to contain widely used and easily recognized functions and be small enough so that instances will accurately reflect device capacity and performance. Most important, they were not selected to identify "winners" or "losers."

Among the ground rules that consortium vendors must follow are that they must report both the capacity and worst-case speed for the *entire* suite of benchmark circuits, they must provide data on the *largest* device in a family being benchmarked, all the tools used to layout the device must be listed and available, and the results must be reproducible by an independent third party.

Benchmarks, like the ones from PEP or any other source, can never be a panacea for the problems and pain associated with making a design decision. But they can remove some of the fog that surrounds vendors' claims and achieve some consistency in the way the performance of a piece of hardware or software is described and reported. We applaud PEP's efforts and will support it in every way we can. What this industry needs is a lot more PEP(s).

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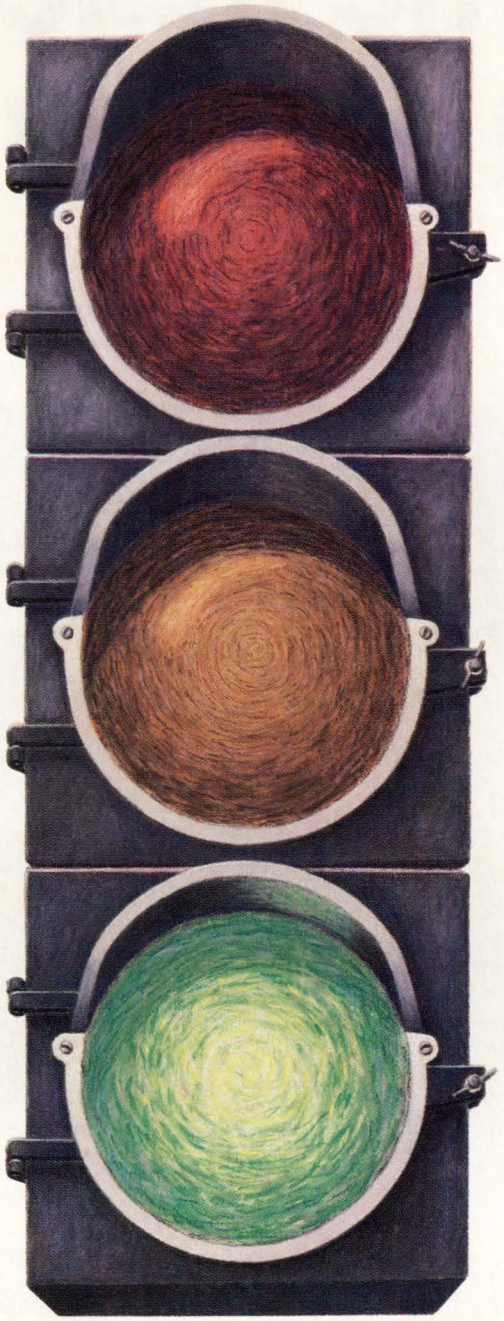

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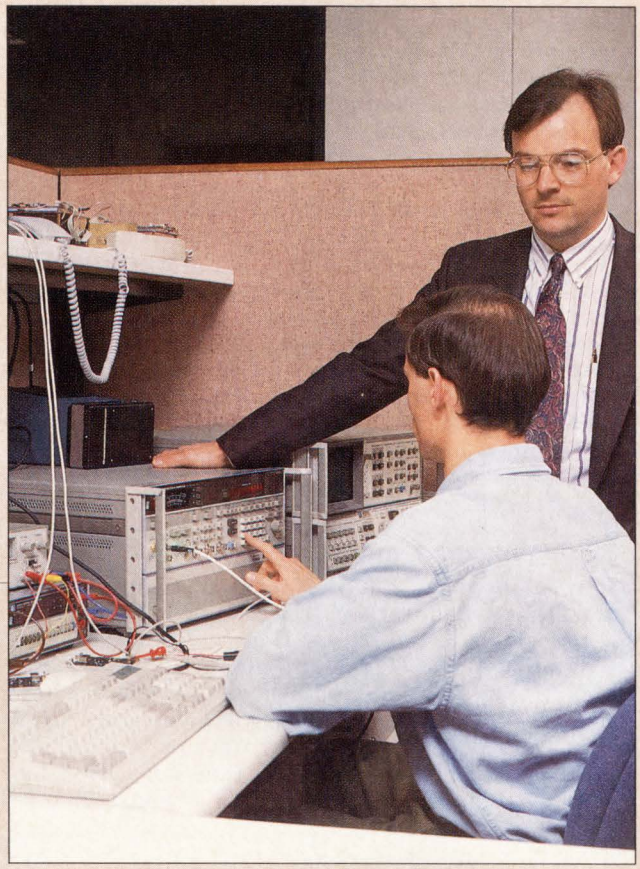
CIRCLE NO. 21

Gary Johnson on: Wireless systems



The same highly charged spirit of innovation and global competition that led to the development of radio a hundred years ago resonates in today's wireless communications design community. A full century after the invention of the Audion triode tube, modern designers face the challenge of emerging digital systems. The arrival of inexpensive, mobile digital communications, however, is dependent not only upon the ingenuity of wireless system designers, but also upon the availability of radio spectrum.

The driving forces in the transition from analog to digital systems include increasing system capacity, improving quality of voice and data and adding security features to discourage or eliminate eavesdropping. Because of overcrowding of the radio spectrum, analog systems that operate at 450- and 900-MHz frequencies will be augmented by more efficient digital systems that use the 1.5- to 2.5-GHz bands.

The economic and personal value of mobile communications continues to fuel the market for wireless systems. The tremendous growth of portable cellular communication in the U.S. is a case in point. Beginning in 1983 with just hundreds of subscribers, the market has swelled to over eight million to date. The rapid acceptance of cellular and cordless telephones has created a time-to-market race for the coming "wireless office." To keep pace in this global race, project teams must complete system design iterations within a nine-month window.

New industries emerging

In the near future at least three major new digital wireless industries are expected to emerge—personal communications systems (PCSs), wireless local area networks (WLANs) and wireless private automatic branch exchanges (WPABXs). The development of these new markets is, in large part, dependent upon the availability of spectrum and the formulation of standards.

Gary Johnson is the director of operations of the Wireless Communications Group at National Semiconductor in Santa Clara, CA.

The spectrum for these systems represents a new arena for North American design teams and standards committees, and the quest for it has engendered an ongoing effort of the telecommunications industry for the past several years. The Federal Communications Commission (FCC), for example, has moved toward allocating spectrum in two successive policy statements.

The critical events leading to allocation of new spectrum include:

- October 24, 1991: FCC policy statement to allocate PCS spectrum somewhere in the 1.8- to 2.2-GHz range.
- December, 1991: FCC/Industry En Banc hearing in Washington, DC, to consider expert testimony on the spectrum issue.
- January 17, 1992: FCC decision to allocate 220 MHz of spectrum in three frequency bands to be used for PCS (1850-1990 MHz, 2110-2150 MHz and 2160-2200 MHz).

Although the particulars of allocating these bands still need to be addressed, the new spectrum is the foundation for the wireless systems of the future. New spectrum may start to become available by the end of this year. If the spectrum for PCS opens up in late 1992, standards may emerge as early as mid-1993.

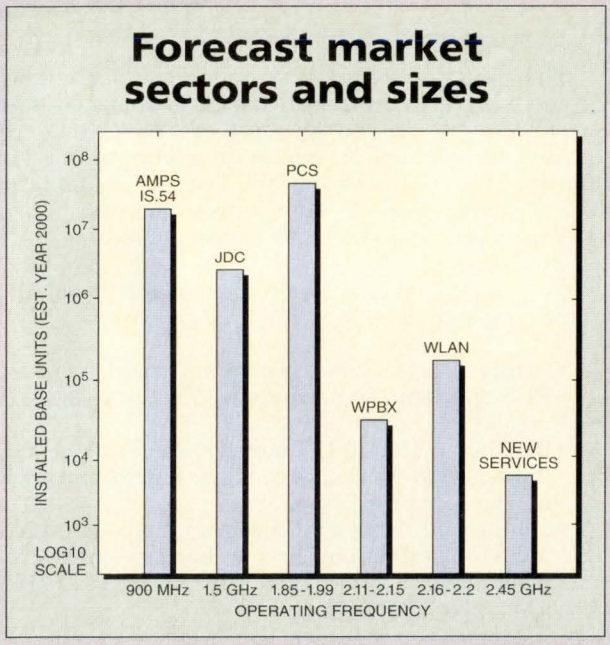
The availability of spectrum will give designers the option of implementing systems based upon the time-division multiple-access (TDMA) transmission technique rather than just upon the "spread spectrum" techniques currently under investigation. Lacking

dedicated spectrum, aggressive manufacturers have built proprietary voice systems, some of which operate in the existing cellular bands (824-894 MHz); others have chosen unlicensed operation under FCC Part 15.247 using spread spectrum transmission in the industrial, scientific and medical (ISM) bands (915 MHz, 2.45 GHz, 5.7 GHz).

On a global basis, the World Administrative Radio Conference (WARC) has focused international attention on the worldwide allocation of spectrum. The meeting held this spring put pressure on the FCC to make its spectrum decisions for North America. At WARC '92, the International Telecommunications Union (ITU) met regarding the spectrum needs for its Future Public Land Mobile Telecommunications Systems (FPLMTS) proposal. While the ITU's vision is still many years from implementation, the group has made progress in identifying some of the key spectrum and technological requirements.

Bridging voice and data

Europe has taken a unified approach to its spectrum and standards questions. The European Community is committed to the Digital European Cordless Telecommunications (DECT) system, a 1.9-GHz TDMA system that is unique in its capability to carry both voice and data. At Telecom '91 in Geneva, Switzerland, Dancall Radio A/S, in cooperation with National Semiconductor, demonstrated the first DECT-for-voice system. In addition, Olivetti demonstrated its DECT-based 1.152-Mbps Sixtel system for wireless LAN applications. Olivetti plans to push the data rate of this system to more than 10 Mbps.



The European Telecommunications Standards Institute (ETSI) has established an ad hoc Radio LAN (RLAN) Committee. This group is considering a system based on the DECT standard and its associated 30 MHz of spectrum, which is being held in reserve for DECT expansion.

The basic architectures and demands on a voice system are vastly different from those of a data system. The DECT standard can serve both voice and data, however, thanks to its ability to implement isochronous data transfers. Although the isochronous mode is not required for traditional data transfers, the real-time demands of voice and video applications—for example, multimedia—will make this mode a necessity.

Numerous attempts by PABX (private automatic branch exchange) manufacturers to offer data capabilities have met with limited market acceptance. Today, the data market in the U.S. is still dominated by large LAN suppliers such as IBM, Digital Equipment Corporation, Hewlett-Packard, and PC-LAN manufacturers, not by the PABX suppliers. Existing data communications suppliers have provided integrated, easily installed, computer-driven data networking equipment not offered by PABX vendors. The new wireless spectrum, however, offers PABX suppliers a chance to offer competitive data services with their equipment.

One problem for the industry has been a lack of standards that work efficiently with both voice and data. DECT offers a proven system approach that can support both voice and data, although the standard is limited to European applications at present. With pioneering work already done by research labs, Post Telephone and Telegraph (PTT) administrations and major system suppliers in Europe, a number of U.S. manufacturers have suggested that the U.S. adopt and adapt the DECT standard for the North American market. This could prove to be faster than inventing a completely new standard from scratch.

A modified version of DECT, which has been referred to in the industry as DUCT (Digital U.S. Cordless Telecommunications), is being promoted as a method of implementing in-building wireless communication systems using unlicensed, dedicated spectrum. The DUCT specification could make up the core of a new "Part 16"-type standard for in-building use. To prevent interference, a standard access method and modulation scheme such as could be provided by a DECT-like standard would be beneficial.

The wireless "LANscape"

In the past, the focus for wireless developments has primarily been voice-based systems. With the proliferation of notebook and palmtop computers there comes a new demand for wireless LAN capability. Standards for wireless data transfer, however, pose significant technical problems in the areas of throughput performance and immunity from interference. Furthermore, bridging both voice and data on the laptop will require new standards.

Since market players are working without standards, proprietary wireless PABX and wireless LAN systems are becoming available. The promise of large profits has drawn eager manufacturers into the market even before standards have been set. Although licensed high-frequency systems are available—for example, Motorola's 18-GHz Altair—many system houses are building proprietary WLAN systems using the ISM bands and spread spectrum transmission—take, for example, NCR's 915-MHz WaveLAN.

When using the ISM bands under the restrictions imposed by FCC Part 15.247, it may be difficult to

Key North American wireless standards

Specification	AMPS	IS.54	ISM	DECT
Frequency range (MHz)	824-894 MHz	824-894 MHz	0.915/2.45 GHz	1.88-1.9 GHz
Access method	FDD	TDMA/FDD	Three types *	TDMA/TDD
Modulation	NBFM	π/4DQPSK	Spread spectrum	GMSK
Bit rate	N.A.	48.6 kbits/s	Varies	1152 kbits/s
Voice/channel coding	N.A.	CELP	Varies	ADPCM
Power output (W)	0.6, 1.2, 3 W	0.6, 1.2, 3 W	0.7 mW-1W	250 mW peak
Carriers	832	832	Varies	10
Carrier spacing (kHz)	30	30	Varies	1.728 MHz
Channels/Carrier	1	3,6	Varies	12
Status of standard	Mature	In testing. Revision B is now being approved.	England and Sweden are considering "Part 15."	Recommended to the FCC for new "Part 16."

Source: National Semiconductor

Transmission using spread spectrum Access Methods: Direct Sequence (DS), Frequency Hopping (FH), Pulsed FM.

achieve the practical solutions necessary to compete with Ethernet's 10-Mbps or Token Ring's 16-Mbps raw data rates. Even though ISM-based systems may be susceptible to interference problems, they may be very suitable for the lower data rates required by portable data applications. It's likely, then, that ISM-band systems will make inroads into the residential cordless telephone market.

Many waiting for spectrum allocation

Major system manufacturers and standards groups are finding it difficult to plan out future wireless systems without prior spectrum allocation. Given their concerns, many established telecommunications companies seem to be waiting for spectrum and standards to be settled before entering the market. A drawback of having multiple competing proprietary systems is that the end users will not enjoy the aggressive price erosion that results from economies of scale associated with a common standard.

The FCC's recent move toward spectrum allocation in the 1.8- to 2.2-GHz range will make it easier for the IEEE-802.11 Wireless Data Communication Committee to consider high-frequency, narrow-band approaches. The key players on the committee, which includes Apple, AT&T/NCR, IBM, Motorola, numerous Japanese laptop manufacturers, and several start-up companies, are busy weighing the alternative PHY and MAC proposals formulated during late 1991 and early 1992. ANSI's T1E1.4 PCS Committee will also benefit from the FCC decision on spectrum. Definition of PCS services and alternatives for technical implementation—access method, modulation, data rate—are currently under consideration.

While the new markets outlined promise to transform our work and our world, a great deal remains to be done by regulatory bodies, standards committees and engineering firms. The task is one of optimizing these high-frequency digital systems for performance and reliability while minimizing power consumption, weight, and, of course, cost.

The challenge for today's design teams is to channel the existing digital radio frequency technologies, which have been manufactured primarily for military use, into the high-volume consumer domain. If designers choose to utilize existing RF-component technologies, they must struggle with the high cost of hybrids and the extensive effort required to design with discrete components.

Alternatively, they may leverage emerging standardized, highly integrated RF semiconductors that will reduce time-to-market and lower overall development costs. In these new digital systems, breadth of design expertise will challenge design teams.

The design of wireless portables and base stations embodies the following design techniques:

- Audio analog design for the user handset interface.
- Ranging levels of embedded real-time software.
- DSP design for channel and codec functions.
- Complex mixed-signal design—multiple A-D, D-A converters.
- Advanced RF design with integration paramount.

Designers must reduce time-to-market for consumer designs while balancing the ability to differentiate products. The semiconductor industry will do much to implement standardized portions of these systems, in particular the RF subsystem (BiCMOS) and the algorithms for bandwidth compression—adaptive speech coding algorithms such as Vector Sum Excited Linear Prediction (VSELF) and error protection (channel coding). Bringing tested, highly-integrated, mixed-signal RF semiconductors to market will enable designers to work quickly. Given the provision of industry-standard silicon, the differentiation of wireless products will be realized with embedded software, power management features, quality, reliability, and brand recognition. ■

Acronyms

AMPS (Advanced Mobile Phone System, cellular in North America)
DECT (Digital European Cordless Telecommunications)
IS.54 (Digital cellular specifications for North America)

FDMA (Frequency Division Multiple Access)
FDD (Frequency Division Duplexing)
TDMA (Time Division Multiple Access)
TDD (Time Division Duplex)

π/4DQPSK (π/4 Shifted Differential Quadrature Phase Shift Keying)
GMSK (Gaussian Minimum Shift Keying)
ADPCM (Adaptive Differential Pulsed Code Modulation)

COMPUTERS & SUBSYSTEMS

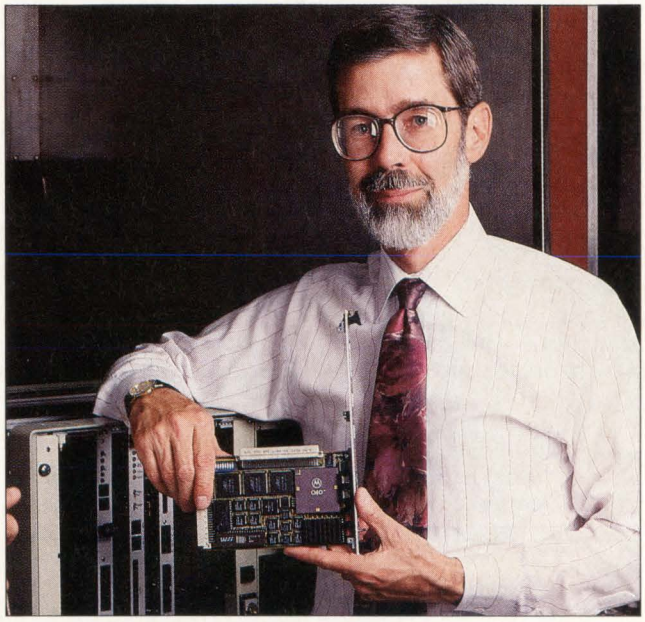
Agreement on key issues gives single-high VME new life

Warren Andrews, Senior Editor

Long obscured by its bigger and more powerful double-high brother, 3U VMEbus is now poised to step into the spotlight. While the modifications to the specification currently under discussion won't immediately turn 3U VME into a competitor for Futurebus+, they may well open up the architecture to new applications, particularly in the industrial automation area.

As 6U-VME manufacturers met last month on proposed Revision D modifications to the IEEE 1014 specification for VMEbus, a small group of 3U board makers got together for the first time to discuss changes to the smaller-profile VME. Since both single- and double-high form factors share the same basic specification, the 1014 meeting was the logical venue.

The 3U board makers first met unofficially at Buscon 92/West in early February; there the group agreed on some basic objectives to advance the technology of the bus and to make it competitive in some newer application areas. The principals at the meeting were from GreenSpring Computers (Menlo Park, CA), Matrix (Raleigh, NC), Mizar (Carrollton, TX), and PEP Modular Computers (Pittsburgh, PA).



Mizar's Ernest Godsey would like to see the 3U VME group put together a "minimalist" specification for Autobahn, a high-speed serial bus that can add 400 Mbytes/s transfer to that of the basic 3U VME. "Once the approach is available," he says, "the installed base will drive the standard."

32 bits or bust

"One of the drawbacks of the 3U VME," says Matrix CEO and president David Mosier, "is that it remains a 16-bit bus at a time when other approaches—not to mention all the major microprocessor architectures—are moving to 32 and even 64 bits. Without the proposed enhancements, 3U VME is at least perceived as a disadvantage, being only a 16-bit bus." (The P2 connector on 6U VME is required for the additional pins that make it a 32-bit bus.)

So, one of the first items to be addressed in revising the 3U specification has been a mechanism to let the bus handle 32-bit transfers. "We looked at the work done in the 6U VME Committee, and at the VME64 [MBLT] specifically," says Ernest Godsey, Mizar's vice-president for marketing and sales, "and that seems to be working pretty well. We looked carefully at the approach, and saw that it would be possible to multiplex the data bus in much the same way that was done in the VME64 specification. This essentially gives 3U VME a 32-bit data bus." This doubles the maximum theoretical transfer rate to 40 Mbytes/s.

The VME64 approach also provides another advantage; it lets the address bus be expanded from its present 32 bits. By multiplexing the lower eight bits, the address space can be increased to 40 bits. "This is increasingly being called for as systems become more and more complex," continues Godsey. "In addition, if it's possible to agree on some kind of Autobahn specification for high-speed serial data transfer, the additional address space will be needed to handle the high-speed data channel."

According to X. Kim Rubin, executive vice-president of GreenSpring Computers, "once the multiplexing scheme is established, it's just a logical move to take the next step to SSBLT [source-synchronous block transfer], doubling again the potential transfer rate of MBLT. This could give 3U VME a theoretical bus transfer rate of 80 Mbytes/s. But we're not counting on that yet. We'll wait and see how the 6U group does with that specification."

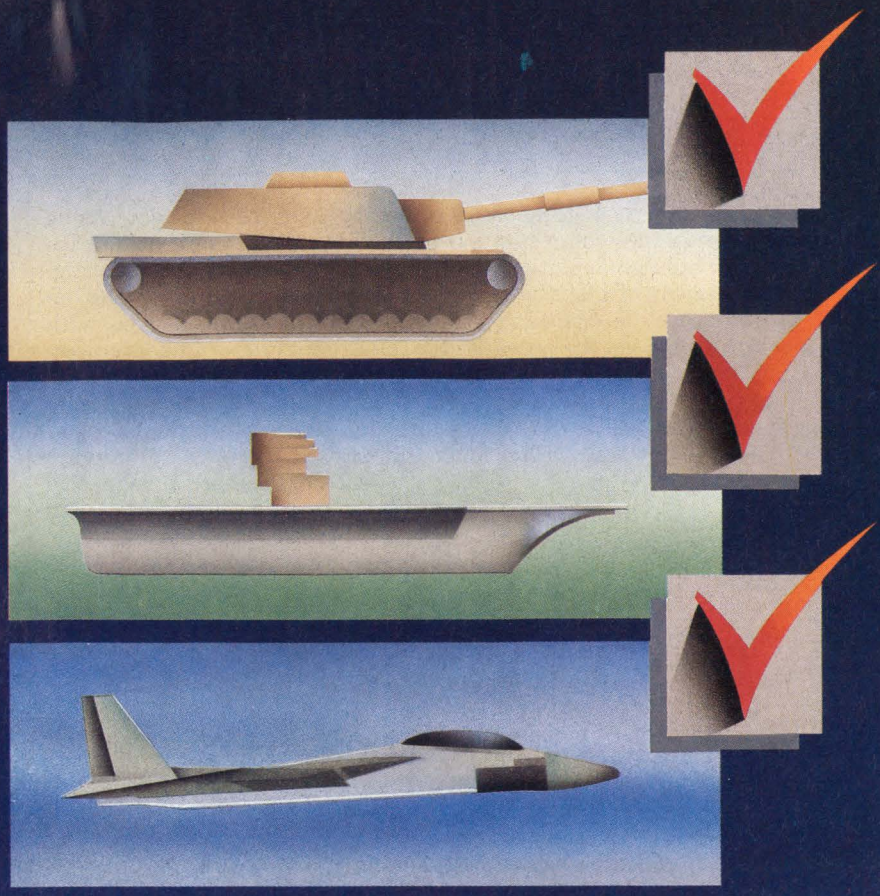
To establish both SSBLT and MBLT, the 3U group decided to add three new address modifier codes to the specification. The decision to increase the address space to 40 bits has provided added flexibility for the SSBLT and MBLT modes by multiplexing only the upper 8 address lines, while maintaining A32 for conventional 3U designs.

Other additions

While the acceptance of MBLT and SSBLT seems to have gained almost universal approval by the group—provided the 6U committee can make it work—there are three other proposals that have met with less enthusiasm in some quarters. They relate to Autobahn, a high-speed serial bus; a standard, high-density, front-panel, connector; and the use of Industry Paks as a 3U-VME mezzanine standard.

Autobahn, at 400 Mbytes/s, is a high-speed serial bus which PEP has proposed to add blazingly fast transfer capability to VME. It's being considered to augment both the 6U and 3U form factors. Not unexpectedly, most of the objections are coming from the 6U camp.

The serial channel was originally designed to carry data only—arbitration, addressing and control sig-



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nals were to be carried on the parallel VMEbus. "One of the problems with this approach," says Wayne Fischer, strategic marketing director for Force Computers (Campbell, CA), "is that the fast serial channel can easily be bogged down waiting for arbitration—or simply traffic—on the main parallel bus."

It's been suggested that the Autobahn approach be amended to include addresses, as well as its own arbitration. Addresses could simply be added to the data stream, so they would have little impact on the transfer rate. A relatively simple collision avoidance mechanism or a token-based scheme could be implemented for arbitration.

"That way," says Fischer, "the utility of the bus will be greatly enhanced. Not only will it be suitable for 3U, but with the modifications, it can operate independently on any backplane—6U VME, Multibus II and even Futurebus+. In addition, it could be used to tie multiple crates together over either copper wire, or perhaps, optical cable."

GreenSpring's X. Kim Rubin is pretty ecstatic about Industry Paks. He says that both their physical and electrical characteristics make them ideal for the 3U VME specification. "The architecture and design have been open from the inception," he adds.

Keep it simple

"I'd hate to see the Autobahn approach bogged down forever in the specification process," says Godsey. "It's just possible that we're trying to make this too sophisticated—suffering from some kind of creeping elegance." While Godsey admits there may be some problem in getting the protocol straightened out, he adds, "Let's go for the minimalist thing, get it working and let the installed base drive the standard—that's what's going to happen anyway."

Others agree. If the Autobahn approach gets bogged down, either PEP will have to back off from its ambitious timetable or the company will make the project an independent venture, hoping a handful of others will follow and make Autobahn a de facto standard. Those "others" may well be the cadre of 3U vendors that huddled at the 1014 meeting.

While many of the 3U makers agree there's a need for some kind of standardized front-panel connector for 3U VME with enough density to handle a wide variety of I/O, there may be difficulty in determining how to specify the pinout. Because 3U cards are used in such a wide variety of applications, including some very specialized ones, it will be difficult to define what functions should be part of the pinout. Some boards, for example, require multiple serial I/O ports and little else. Others call for SCSI, SCSI II, Ethernet, or other functions.

Industry Paks

While the relative merits of Autobahn continue to be argued, GreenSpring's Rubin is offering his company's Industry Pak technology to be integrated into the 3U approach as an industry standard. "Unlike other mezzanine bus approaches," he says, "the Industry Pak has been designed specifically to be a mezzanine bus on both 3U- and 6U-VME cards."

"Industry Paks," continues Rubin, "were designed from the start to provide a compact, cost-effective mezzanine card, two of which can fit on a 3U module, and four on a 6U card, without using a second slot. Aside from the physical considerations, Industry Paks are designed with rugged connectors accommodating either 8- or 16-bit address space, with full DMA capability. The architecture and design have been open from the inception, and already more than a half-dozen manufacturers offer Industry Pak products, and over a dozen more design and use the standard with products of their own."

But settling on a standard mezzanine card for 3U VME may not be that as easy. "Even within one company," protests Godsey, "a single mezzanine specification can't be arrived at. I just can't see different companies getting together on any one standard." There are just too many specific junctions that require a special mezzanine configuration to consider only one mezzanine bus as a standard.

It's expected the modifications to 3U will continue to roll along, much as they've done in the 6U world. VME64, for example, is now in relatively widespread use, despite the fact that it's not yet officially part of the VME standard. Therefore, it's expected 3U VME will be in the market long before the players will be able to decide on how to implement the various proposals. Autobahn, too, will probably be available from at least a handful of board makers long before actual standards are finalized. ■

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COMPUTERS & SUBSYSTEMS

Hot swap broadens Multibus II horizons

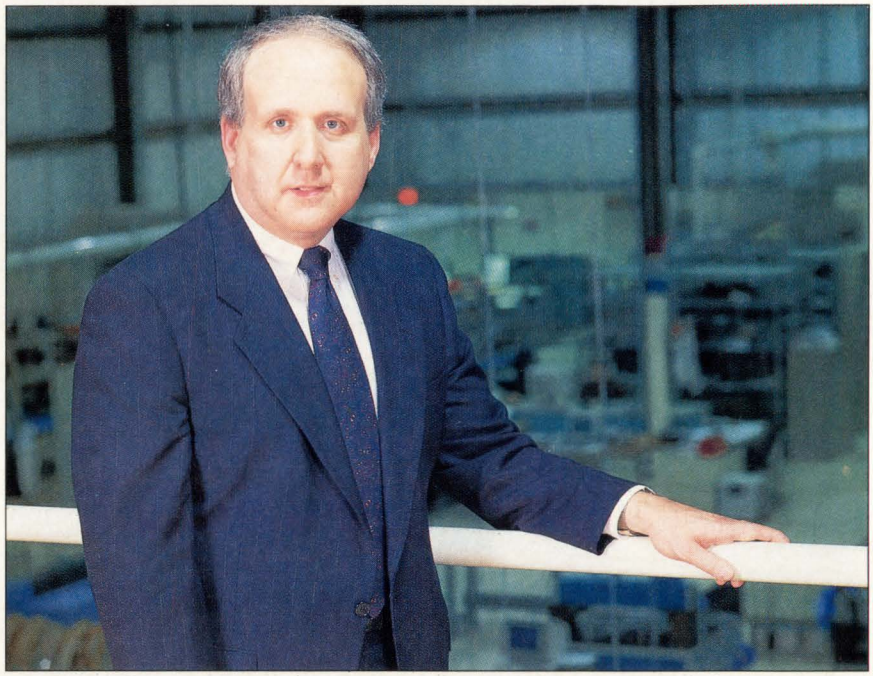
Warren Andrews, Senior Editor

Final prototyping has begun on the first of a series of MultibusII upgrades for live-insertion, or hot-swap, capability. Although efforts started in 1988, the final version of the hot-swap specification is only now going through the Multibus Manufacturers Group (MMG) approval cycle. Other planned upgrades include scaling up bus speed, increasing intelligence in the message-passing coprocessor (MPC) and extending the 21-slot backplane. These are expected sometime in September.

"Though requirements have been around for some time, live insertion is a feature that is now dramatically increasing in demand," says Roger Finger, MMG technical director. "The first applications that we see jumping on the bandwagon are [from] the communications companies. The telephone companies have had live insertion in their line card systems for years."

Finger expects these companies will be extending this capability into other areas. "Manufacturers of network concentrators," he says, "are showing a high level of interest. In fact, almost anyone needing a system with 100 percent on-line performance—network controllers, servers, gateways, routers, and other critical hardware—will be migrating to systems with live-insertion capability."

According to Len Schulwitz, MMG executive director, "Even before the live-insertion capability, there's been a very strong interest in Multibus II from many communications companies, both U.S. and European-based." Novatel and other non-Motorola-based cellular phone companies have steered toward the Intel processor and Multibus II. In addition, there are a number of large European communications vendors picking up on Multibus II. The idea of Multibus II as a backplane LAN is attractive to such communications companies because they are already familiar with the approach and technology. Live insertion—with the attendant on-line servicing and 100 percent on-line performance—gives these firms yet another peg to hang their hats on.



Micro Industries is the first to implement the MMG's live-insertion capability. In its approach, the company implements the technology using a stand-alone board which connects to the backplane. By making the board independent of the backplane, the same approach can be easily used on VME. In fact, says Micro Industries president Michael Curran, "We'll have a working VMEbus version for the fall Buscon."

Already in the spec

At a system and software level, live insertion is provided for in the Multibus II specification. "Multibus II offers more than an electrical and mechanical specification," says Finger. "It allows for such things as individual board reset and rebooting in an operating system. These functions are addressed in the Intel-developed MSA [Multibus System Architecture], which is now distributed by the MMG."

Though the road to mechanical and electrical implementation of live insertion on Multibus II began in 1988, the capability hasn't been realized until now because early versions failed to preserve full compatibility with existing Multibus boards. "The original concept," Finger states, "involved redefining some bus signals, which would have made existing boards incompatible with live-insertion boards." The current approach requires no modification to the Multibus signals and lets any existing Multibus II board automatically take advantage of live-insertion capability.

Needs modified backplane

While the individual cards may not need any modification, live-insertion capability depends on an upgraded backplane with power FETs to switch current and some intelligence to turn the FETs on and off. "One of the first considerations in live insertion," according to Finger, "is the need to provide power to the connector after the board is plugged in—or at least to provide power to the board before signal lines are connected—and vice versa. In addition, it's critical that grounds are connected before B+ voltage is applied. Failure to do this could cause a potentially catastrophic reverse voltage to appear across some of the ICs."

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Instead of using staggered-length pins—the longest for ground, the next longest for B+ and the shortest for signals—the MMG approach calls for active power control at the backplane. Power FETs capable of 50 A at 50 V and stable over a broad temperature range are readily available at low cost with on-resistances as low as 0.01 Ω. By simply including one such FET per connector on the backplane, the power to each Multibus slot can be turned off for removal and automatically turned on after a replacement board is inserted.

When the board is removed and another inserted, the system is apprised through the system reset signal. The reset signal nominally governs the system's activity, minimizing down or inactive time. However, it must be selective, so as not to affect the entire system.

Minimizing disturbance

When a new board is inserted into a system which is already running, the problem becomes one of how to assign a valid card slot and arbitration identification to the new board without forcing other boards into a reset cycle. The solution, developed as part of the MMG's live-insertion approach, is to connect independent RST and RSTNC (reset and reset not complete) lines to each slot in the backplane and gather them at the P2 connector of one of the boards in the system. This board then serves as a "slot controller." It includes some intelligence (probably a small microcontroller) for managing the RST and RSTNC signal lines as well as FET power controls. The slot controller can also provide LEDs to guide operators through the removal/insertion procedure.

According to Finger, the selective reset works because only agents which actually receive the RST signal are receptive to taking a new arbitration and slot ID. The RST line is isolated from other boards in the system and will ignore the reset event, provided there are no other transactions pending on the bus. The RSTNC signal must also be isolated for each board, because other agents will not resume bus traffic if the line remains uncleared.

Other problems can arise during live board insertion. First, stray capacitance on signal lines of the unpowered board being inserted could introduce bus errors if there is active traffic on the bus at the time of insertion. Second, the MPC and board initialization firmware may try to drive some of the bus control lines while waiting for a slot and arbitration ID from the central services module (CSM). In addition, there's no knowing the state of the bus transceivers and control lines on the newly inserted board until it's had time to stabilize. This could also result in errors to bus traffic.

The simplest solution to these problems is to let the slot controller

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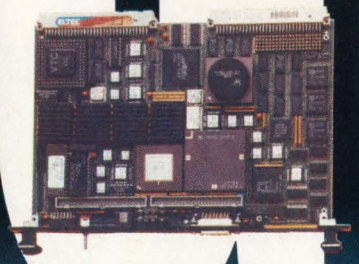
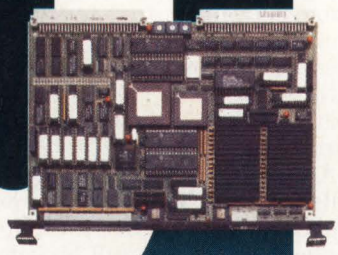
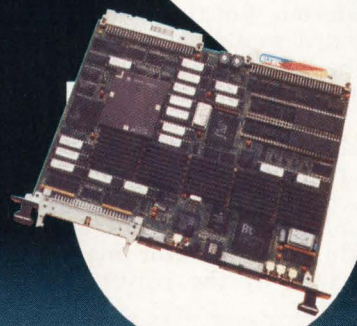


EUROCOM 7 CPU board; 25 MHz 68040



OPAC-200 Color Graphics Interface board



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CIRCLE NO. 27

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arbitrate for and acquire the bus in a normal arbitration cycle during the insertion and selective reset procedure. In operation, the slot controller continues driving the open-collector arbitration lines until it wins bus ownership. Once accomplished, however, there's no way to prevent other agents from starting a new arbitration cycle, creating contention for the arbitration lines during the reset sequence.

Another problem is that the bus reset takes at least 50 ms, exceeding the normal bus timeout of 1 ms. The timeout function can be disabled, but it would have to occur prior to the slot controller taking bus ownership.

"Fortunately," says Finger, "the Multibus II hardware specification provides a mechanism to handle such problems, and it appears in the unlikely form of the bus error line. This open collector line is normally driven by the parity checkers on each board. The effect of driving it low is that all boards must remove their arbitration requests from the bus and suspend all activity until the error is cleared. The bus error condition has no effect on a reset sequence."

During the time a board is being removed and a new one inserted, however, the bus is inactive. This duration is determined by how fast an operator can physically make the swap. Finger estimates that even a relatively clumsy operator can make it in only a few seconds. To minimize system downtime, there must be some mechanism to detect a transition from "slot empty" to "board present." As soon as a transition is detected, the bus release command is issued, letting the system resume normal operation.

Although the hot-swap capability calls for some additional hardware, Finger estimates that the total incremental cost in a full Multibus II configuration should be no more than $50. The simplest configuration calls for a gate array or a set of EPLDs connected via an 8-bit bus to either a CPU's I/O bus or the interconnect of an on-board microcontroller. A 21-card-slot backplane, with 19 slots set up for hot-board insertion—and one slot for the CSM and another for the slot controller—will call for 81 I/O pins, in addition to the 8-bit bus. ■

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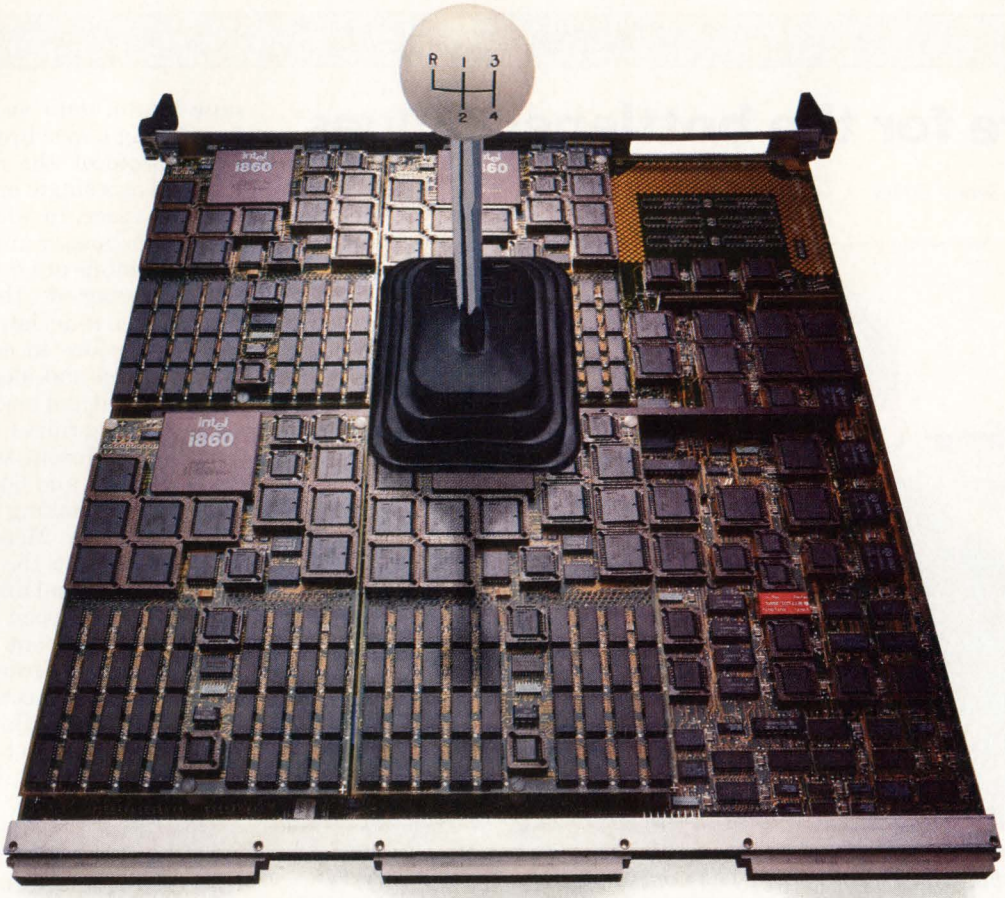

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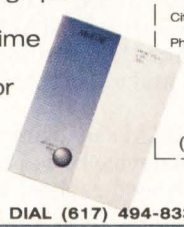

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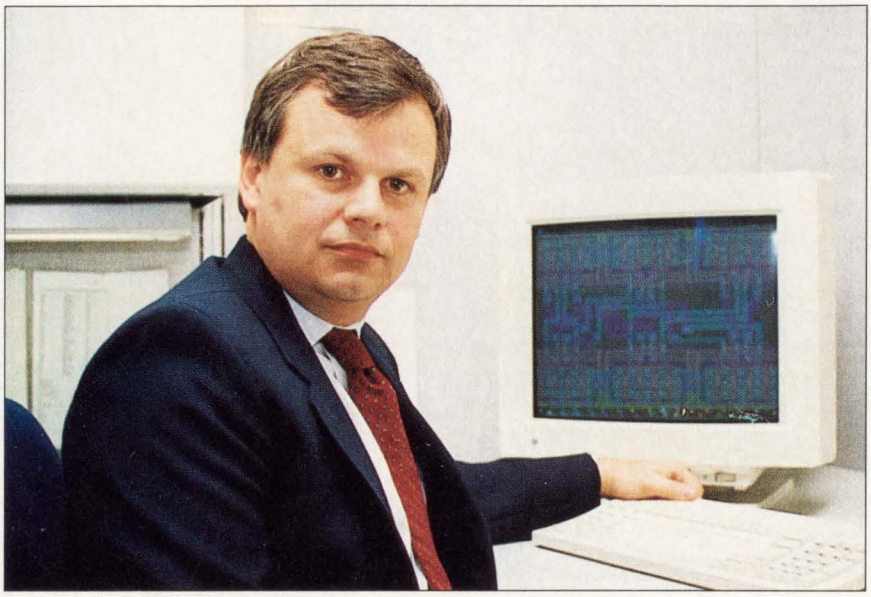
INTEGRATED CIRCUITS

A cure for the bottleneck blues

Dave Wilson, Senior Editor



Geoff Tate, president and CEO of Rambus, has announced a processor/memory interconnect bus with a memory bandwidth of 500 Mbytes/s. To support the fast system bus, three Japanese memory vendors—and probably some other companies as well—are working on a new type of memory, the RDRAM, to meet the Rambus specification.

Personal computer-based memory systems display a simple hierarchy of first- and second-level SRAM caches and somewhat slower main memory, usually based on DRAM. Now, a new 500-Mbyte/s processor/memory bus architecture from start-up Rambus (Mountain View, CA) challenges the traditional way of building such memory subsystems—especially ones with clock speeds over 50 MHz. The Rambus solution goes beyond a simple processor-to-memory bus definition, providing a novel DRAM architecture as well.

The Rambus device is not very wide—only nine bits—and yet it provides a very high bus bandwidth—500 Mbytes/s—by using both edges of a 250-MHz clock. Small signal swings of 600 mV are used instead of more conventional (and noisy) TTL signals. At high speed, the bus looks like a transmission line; to minimize clock skew and capacitive loading, phase-locked loops must be used on bus masters (or processors), as well as on slaves (or memories), to synchronize them. A direct chip-to-chip interface between the processor and the memories eliminates control and decoder logic, buffers and cache controllers, so that you can reduce the size of the memory subsystem used in your design.

A new type of DRAM

The fast system bus is only part of the equation. To support it, Rambus needed some unique memories. Working with three leading Japanese semiconductor companies—Fujitsu (San Jose, CA), NEC (Mountain View, CA) and Toshiba America (Irvine, CA)—Rambus got them. Supporting the Rambus specification are what the company calls RDRAMs—CMOS DRAMs with modified architectures and Rambus interface circuitry. The high bandwidth of the RDRAMs lets them functionally replace DRAMs, SRAMs and video RAMs in a system design.

All DRAM sense amplifiers on the Rambus device have been converted to high-speed caches, which deliver nine bits of data every 2 ns to the bus. Using a synchronous block-oriented protocol, the memory can be mapped as a single large, contiguous address space. In addition, the clock rate of the master and the frequency of the Rambus are decoupled, which lets you upgrade the master with virtually no redesign to the memory.

The interface to each RDRAM is standardized and identical in pinout and electrical and mechanical characteristics—regardless of the DRAM's capacity. Different-sized devices (4 Mbit, 16 Mbit and 64 Mbit) have the same pinout, making the architecture highly scalable. Memory subsystem overhead due to the memory interface, DRAM signal timing and refresh control has all been eliminated. All DRAM management is on board the RDRAM and is performed automatically. Rambus expects systems to be built using 4.5-Mbit RDRAMs in 1992. In 1993, Rambus expects chip vendors to be building 18-Mbit RDRAMs in volume.

Geoff Tate, president and chief executive officer of Rambus, admits that the Japanese companies aren't the only ones working on devices to meet the Rambus specification. Two other vendors may well be developing processors with Rambus interfaces, but they've yet to announce products. Certainly, any RISC or CISC processor designs with a Rambus interface built directly on-chip appear to offer a competitive advantage in the marketplace. At present, though, very few processors have the capability to interface directly to 2-ns memory at anywhere near 500 Mbytes/s. For example, an older 50-MHz Intel 486 without the Rambus interface theoretically requires memory with an access time of just 20 ns. The new 200-MHz Alpha processor from Digital Equipment Corp. (Hudson, MA), on the other hand, is a much likelier candidate for the technology.

Support available

For ASIC designers who wish to build their own processor/memory interface bridge chips, Rambus will provide the tools to do so—a Rambus ASIC cell, documentation and other support is available from the company. Rambus, however, does not make Rambus-compatible processor chips, bus interface chips or memory chips—nor does it intend to.

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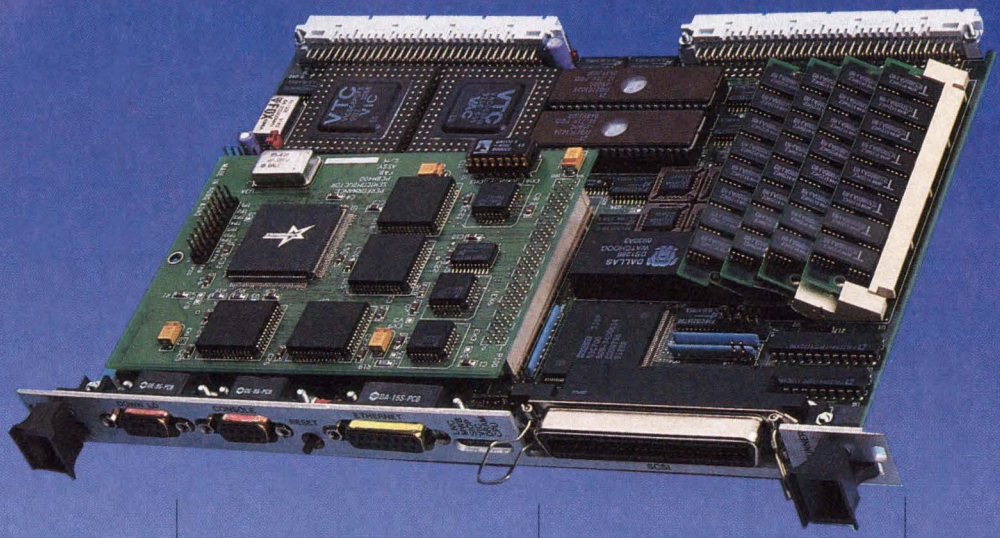

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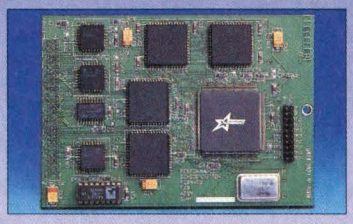

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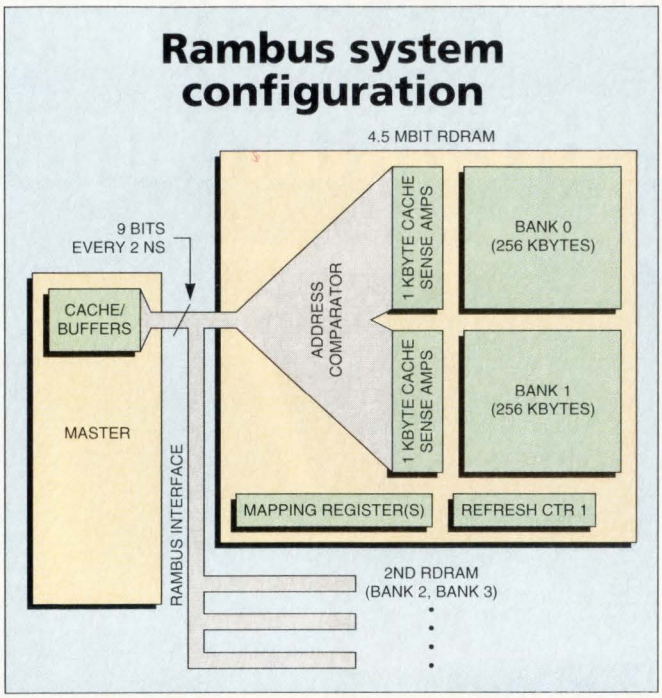

In this illustration of a Rambus system configuration with memory modules, the processor interfaces to the high-speed processor/memory subsystem through an ASIC.

Furthermore, since the company is promoting the Rambus interface as an open standard, users of the Rambus interface won't pay a license fee or royalty to the company. Instead, Rambus will make its money from license fees and royalties it gets from other chip companies that use Rambus technology in the design of Rambus-compatible ASICs, processors and memories. ■

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MT5C2561 LP	256K x 1	Now
MT5C2564 LP	64K x 4	Now
MT5C2565 LP	64K x 4 $\overline{OE}$[5]	Now
MT5C2568 LP	32K x 8	Now

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INTEGRATED CIRCUITS

IBM, National union yields integrated token ring controller

Dave Wilson, Senior Editor

As a first step in a joint networking technology relationship, IBM (White Plains, NY) has licensed its newest token ring IC to National Semiconductor (Santa Clara, CA). This means IBM's device and associated microcode will now be available to outside manufacturers for the first time.

The device was first used in IBM's Micro Channel Token Ring adapter cards, announced last November. Built in a flip-chip PGA package, the $130 DP8025 token ring protocol interface controller (Tropic) implements system bus interfaces, an IEEE-802.5-compliant and IBM-certified ring interface, and MAC/LLC (media access control/logical link control) functions per the IEEE-802.5 specification. Due to the device's high level of integration, a complete token ring adapter can be built from the Tropic chip, transmit and receive buffers, a MAC/LLC microcode program, ROM, system interface, and passive components.

Tropic provides three external interfaces: to the token ring, to the host bus and to local memory. The front-end macro within the Tropic chip supplies a ring interface providing signals and inputs for external equalization and transformer circuits for the actual token-ring serial interface. The external interface must provide filters, switching circuitry, line conditioning, and protection and conditioning components.

The host bus interface lets the host transfer data to and from Tropic. It includes a 24-bit address bus and a 16-bit data bus with optional parity and control signals that lets the device be attached as a bus slave to the ISA, MCA or 68000 bus. The local storage interface provides direct attachment to local memory—PROM and RAM—which Tropic uses exclusively. "This chip is aimed at the PC adapter market in that it has the bus interface circuitry right in it," says Carl Hayssen, a principal engineer at Ungermann-Bass (Andover, MA), a supplier of token ring solutions.

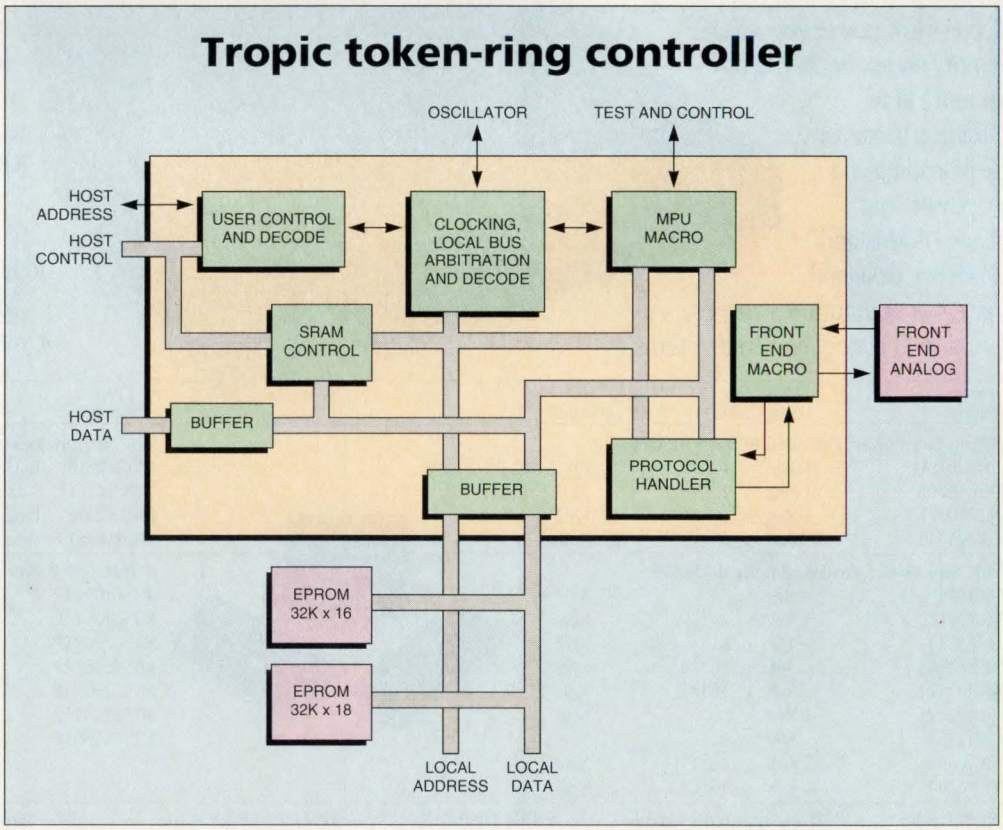
Not the first

Still, as highly integrated as it is, Tropic isn't the first token ring chip. Texas Instruments (Dallas, TX) also manufactures a token ring solution, the TMS380. And Chips and Technologies (San Jose, CA) announced its own token ring device last year. "From a functionality point of view, [the National Semiconductor chip] may be better for some designs; it's a single chip, whereas the TI and C-and-T solutions are two-chip sets," notes Nick Grewal, vice-president of engineering at Proteon (Westboro, MA), another vendor of token ring solutions.

Nevertheless, the IBM-National Semiconductor alliance doesn't necessarily mean that TI and Chips and Technologies have lost the token ring battle. "Not at all," says Grewal. "The chip is not as fast as the Texas Instruments chip, and it's too expensive." (TI's chip set is well under $100.) But Grewal says that he's keeping an eye on the chip, because "you never know when the price is going to drop."

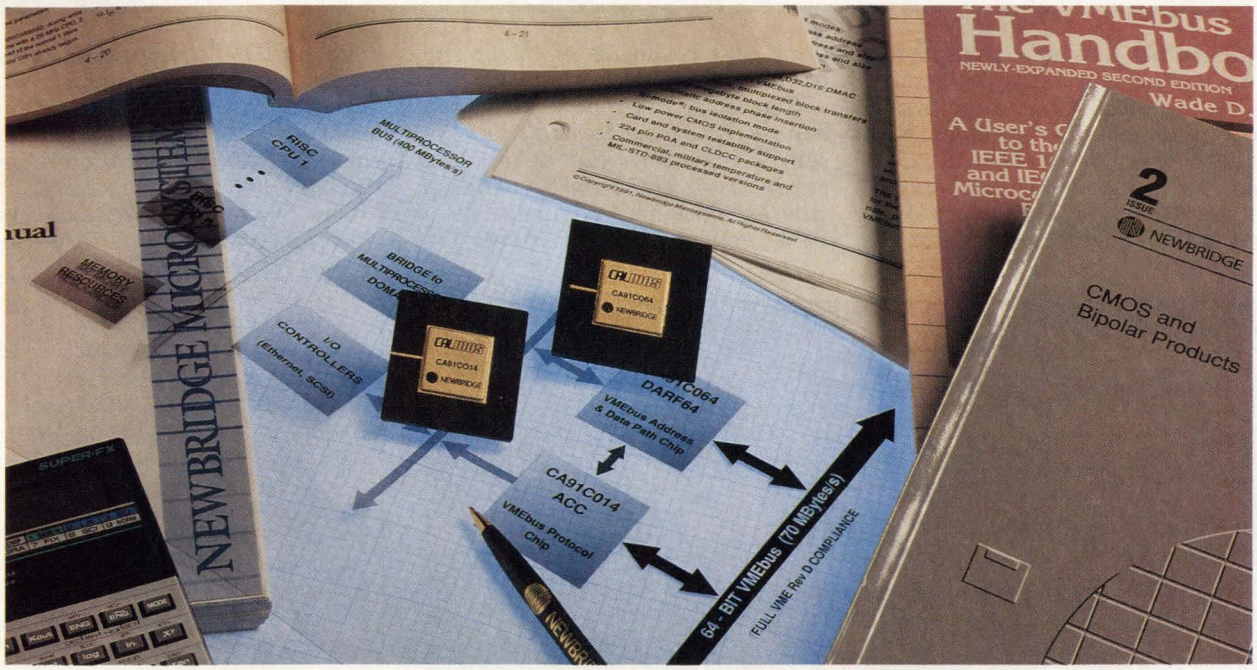
Standard problems

Even as National Semiconductor claims that Tropic's physical layer meets the current IEEE-802.5 standard, Ungerman-Bass' Hayssen notes that the current standard isn't as "robust" as it could be. In fact, the



Licensed by IBM and supplied by National Semiconductor, the Tropic is a highly integrated, single-chip token ring controller solution. It implements system bus interfaces, an 802.5-compliant and IBM-certified ring interface, and the MAC and LLC functions per the IEEE-802.5 specification—all in a 175-pin package.

70 Mbytes/sec...



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"A second generation VMEbus interface chip set from Newbridge Microsystems (Kanata, Ontario) offers both a pin-for-pin compatible upgrade from the company's earlier chip set and full support for the proposed VME64 performance upgrade."

"Newbridge currently has the advantage, it would seem, in having incorporated the bells and whistles for distributed processing and multi-processing."

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standard has had more than its fair share of interoperability problems—issues the 802.5 Committee is currently addressing. The problem with the 802.5 standard is that the margins of certain key technical specifications are too wide, leaving room for a number of different interpretations and resulting in token ring products that won't interface.

Certainly, interoperability problems become most obvious when system integrators mix token ring cards from third-party vendors, whereas designers relying solely on IBM products may experience less difficulty. IBM token ring products, in fact, provide a de facto industry standard—although IBM keeps quiet about how it has exceeded or tightened the 802.5 specification to make its own products interoperable.

The 802.5 Committee has been working on problems with the specification, mostly involving jitter, for months. "While jitter buildup around the whole ring isn't a problem, very fast transients in jitter can occur over a small group of stations that aren't easy to track. If there are stations on the ring that are particularly quick in responding to jitter, followed by stations that are somewhat slower, the slower stations will have a hard time operating," says Hayssen.

What is a token ring?

A token ring is a 4-Mbit/s or 16-Mbit/s LAN that uses a token-passing access method to ensure the orderly transmission and reception of data on the network.

A 24-bit token is passed around the network in a specific sequence. The token conveys the exclusive right to transmit on the network.

If a computer has data to send and the token is available, it attaches its message to the token with source and destination addresses. When the package of token and message reaches its destination, the receiving computer copies the message. The package is then put back on the network, where it continues to circulate until it returns to the source computer. The source computer removes the returned package and then releases the token for the next computer in the sequence.

One device on the network, designated the token monitor, generates the token. If that device is turned off or fails, another device will assume the role of token generation. Logically configured in a ring, the network is physically wired in a star configuration. This arrangement lets each computer be wired directly to a multistation access unit that can automatically recreate the ring in case of a failure on one computer.

The maximum number of computers that can be connected to a single token ring LAN is 256, but multiple access units themselves can be connected to expand the network.

The Committee is working to tighten up three key token ring characteristics that will help solve interoperability problems: filtered accumulated phase slope, data delay time and filtered correlated jitter. The numbers associated with these characteristics won't be available until later in the year; once they are, however, the tightened specifications should help designers and integrators alike.

And if you can't wait

National Semiconductor's chip won't be available in production quantities until the third quarter, although samples are available now. Until then, you could consider a PC solution from National Data Communications (San Jose, CA). Len Palmer, vice-president of sales and marketing at the company, explains that it got its PC card to market quickly through an OEM agreement with IBM that let National Data Communications use the token ring chip set already manufactured by IBM, rather than the one licensed to National Semiconductor. "IBM provides us with a 'minicard' with a lot of the token ring logic on it," he says.

Having the fully integrated minicard is important to National Data Communications because through it the company can offer all of the same logic IBM uses to support token ring functionality. "We don't get any of the problems that everyone else has got," says Palmer—admitting, however, that his company has experienced "tremendous trouble" trying to provide 4- to 16-Mbit/s token ring capability with its TI-based products. "There are so many compatibility issues that the minicard solved for us," Palmer adds with relief.

Palmer says that he doesn't have any idea how National Semiconductor will resolve the analog problems associated with using the Tropic. But Bruce Watson, marketing manager for token ring products does. Watson says that the company will provide a schematic and design and layout rules for the analog front end, as well as all the values for the parts. "We will be sending out a design that will be 100 percent compatible with the same circuits that IBM is using. It is an IBM-certified design," says Watson. ■

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Innovative technologies reduce prototype turnaround time

Mike Donlin, Senior Editor

As high-speed components and surface-mount device (SMD) technology make hard-wired prototypes obsolete, designers are looking for alternatives to test their designs. Claims of EDA vendors notwithstanding, simulation is still impractical or inaccurate for most PCBs, and designers need a working model to observe the effects of interconnect delays, crosstalk and thermal problems before committing their ideas to production. Several companies have addressed these needs, either with systems that manufacture prototypes in a matter of hours, or by offering programmable interconnect devices to replace hard-wired breadboards.

Programmable interconnects

One such company is Aptix (San Jose, CA), a start-up that has just introduced its family of field-programmable interconnect (FPIC) devices, letting you test your designs on a field-programmable circuit board (FPCB). The Aptix family includes two devices—the FPIC/R and the FPIC/D—that integrate an array of universally programmable interconnects packaged in a 1,024-pin, multilayer ceramic package. Comprising a regular grid of attachment points, the FPIC devices house segmented routing tracks with multiple sections that are configured in an array topology. The array configuration lets you access about 1,000 externally accessible interconnects from a single package.

The FPIC/R is a reprogrammable SRAM-based device with bidirectional paths and pin-to-pin path delays as low as 5 ns. The device targets applications where prototype replication and dynamic in-system programming are required. It integrates over a million transistors and is processed in 0.8-μ CMOS technology.

The FPIC/D is a reprogrammable interconnect device that hosts a 64-channel diagnostic port with a logic analyzer interface. Once attached to a logic analyzer, the diagnostic port lets any signal passing through the FPIC be observed under software control. The 64 diagnostic signals from the FPIC/D connect directly from the device package to a flex cable, which in turn attaches to a logic analyzer interface pod.

As stated earlier, Aptix has also unveiled a FPCB, a board which is divided into FPIC regions so that any pin on the board can be programmed to connect to any other pin. Because each FPIC has between 140 and 200 pins dedicated to global interconnect, signals will only have to travel through a maximum of two FPIC devices to access any other device.

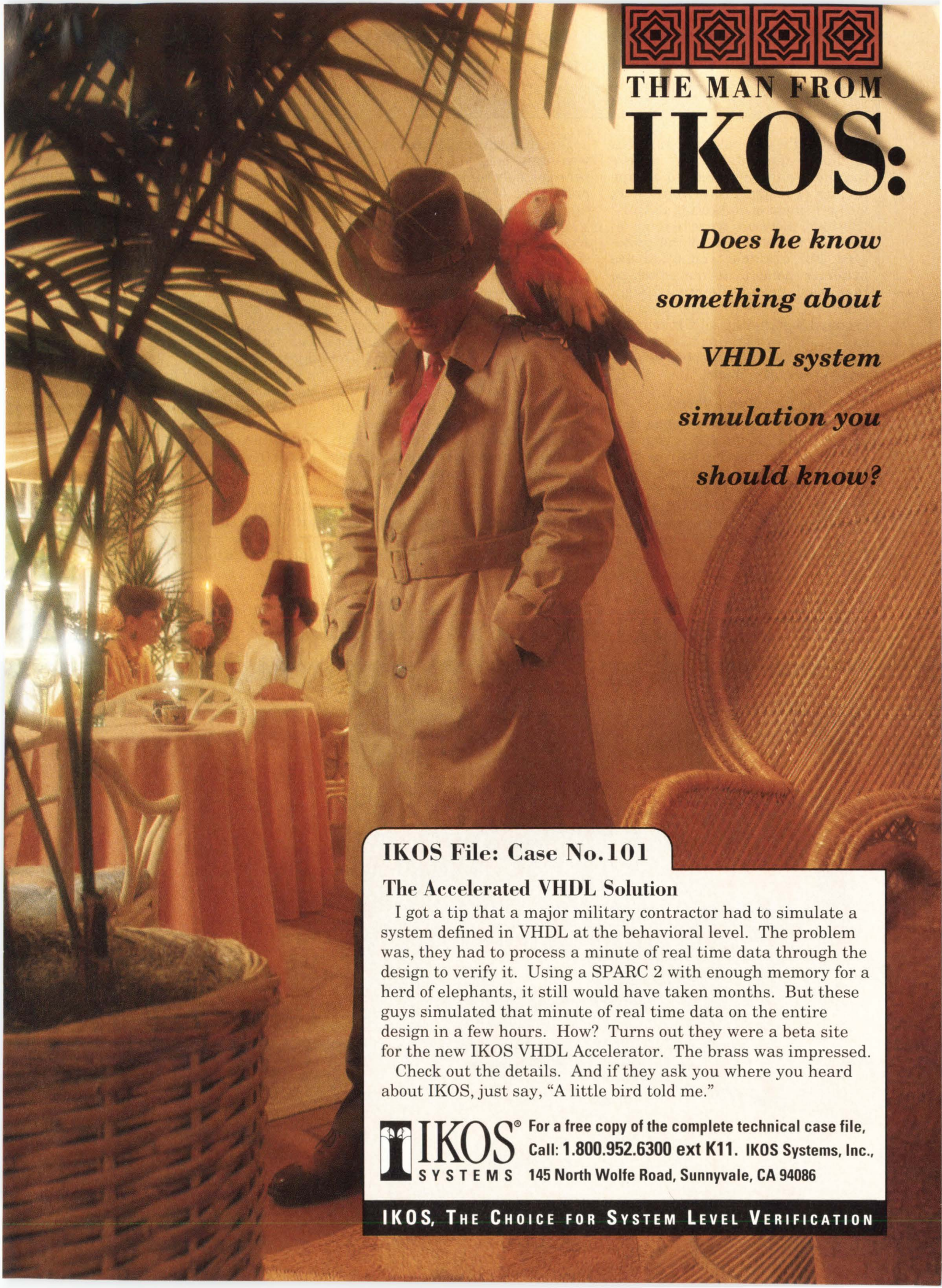
Initially, the FPCB will be available in two form factors. The FPCB-AT is a full-sized PC/AT-compatible board that accommodates up to three FPIC devices and more than 2,000 connectable component pins. The board incorporates through-hole spacing that accommodates SMD adapters. The FPCB-GP2 is a general-purpose 7- × 10-in. board that features identical pin spacing and accommodates up to two FPIC devices.

To support the development of other FPCB form factors, Aptix has developed the FPCB compiler, a software system that produces standard Gerber output files which can interface to most PCB layout systems.

Potential problems

Though the Aptix reprogrammable technology holds promise for designers looking for prototypes that eliminate jumper wire, there are some potential problems inherent in a solution that depends on routing signals through devices to get to the other side of a circuit board. With such a scheme, delays are necessarily introduced because the signals have to go through a matrix in the interconnect chips to get across the board. Aptix acknowledges that the 5-ns path delay might be a barrier for some high-speed signals, but ar-

The Aptix Development System lets you partition a design so that every component on a board is addressable through field-programmable interconnect devices (FPICs). Here, a circuit board has been divided into two parts, with selected devices assigned to the two available FPICs. Unassigned components are at the bottom of the screen.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gues that the technology is sufficient for many applications. "We believe that our solution applies to a large number of designs," says Bob Osann, vice-president of marketing at Aptix. "Besides, there are ways to compensate for some delays in the prototype. For example, you could use faster components in your prototype than you'll need in the final design. Usually the fastest components are grouped together on a PCB anyway, so it's unlikely that you'll be routing signals to the highest-speed devices across the entire board."

Getting prototypes faster

For those of you with designs that aren't suitable for the Aptix approach, there are alternatives that provide relief from the typical two-week wait for a working prototype. Systems built by Direct Imaging (West Lebanon, NH) can produce a prototype in a matter of hours from CAD data.

Direct Imaging's System Two uses wax-based solid ink applied to copper-clad polyimide film to produce prototypes of up to 12 layers in a number of form factors, including VME, NuBus, Microchannel, PC-AT, Futurebus, and Multibus. The system, an adaptation of solid ink jet, dot matrix technology, was developed to meet the needs of designers who found that software simulation and hard-wired prototypes weren't meeting their needs, but who still wanted a working PCB to debug their circuits.

"Simulation works fine for synchronous digital designs," says Bill Schillhammer, vice-president of marketing at Direct Imaging, "but with asynchronous, event-driven or analog designs, simulation starts to break down. Traditional prototype techniques depend on adding jumper wires for debugging purposes, but those wires don't act like the fine-pitch traces of the finished product, especially when they're carrying high-speed signals. Quick prototype turnaround is a necessity if you want to reduce time-to-market, so we think our system addresses the needs of designers who need to produce a prototype in hours instead of days."

Direct Imaging's system uses a six-step process to produce a prototype. First, it captures the circuit design file from your PC or workstation and groups each layer of the design into sheets for conversion into plot format. These circuits are then plotted on a sheet of flexible copper-clad polyimide film that has been inserted into the system. A resist pattern is deposited on the copper in the circuit design pattern and then a salt solution etchant is sprayed onto the film, removing the unprotected copper. Only the printed circuit remains. Finally, a rinse phase removes any etchant, and the flexible printed circuit is

Breakthrough multichip modules

ready to be bonded to a rigid core that has been drilled for through-hole connections, where necessary.

"A typical AT-sized board with six layers and 1,000 holes takes about four to five hours to produce," Schillhammer points out. "You can add layers without a substantial time penalty, because the time-consuming part is the drilling of the holes."

The main drawback of Direct Imaging's prototype solution is cost, with a fully loaded system sporting a price tag of around $40,000. "Of course, we have numbers that prove that it's cheaper in the long run to buy our system," Schillhammer explains, "because the cost of a six-layer prototype from a PCB shop is around $1,600, and takes two weeks to procure. Unfortunately, many companies can justify a couple of thousand dollars here and there, but balk at a one-time capital expenditure of $40,000."

Though both Direct Imaging and Aptix's prototype methods hold promise, there are many designers who can't spend the money for a prototype system or who don't want to use unproven technology for their designs. For these engineers, the best hope comes from EDA tools that ensure that their designs will produce a working prototype with a minimum number of iterations. To this end, PCB manufacturers are developing tools that assist you in the design phase of a PCB, so that it's both manufacturable and performs according to spec.

"About 90 percent of our customers require us to build some samples for prototype and qualification before production," says Steve Laney, marketing manager for custom manufacturing services at Micron Technology (Boise, ID), a PCB manufacturer. "So it's in everyone's best interest to know the rules for manufacturing before a design is carved in stone. We provide tools that pass manufacturing guidelines along to the designer, so that there aren't any unpleasant surprises when it's time to turn out those first critical samples. It's a slow transition, but the roles of manufacturer and designer are overlapping, and each has to know the needs of the other if a working PCB is to get out the door on time." ■

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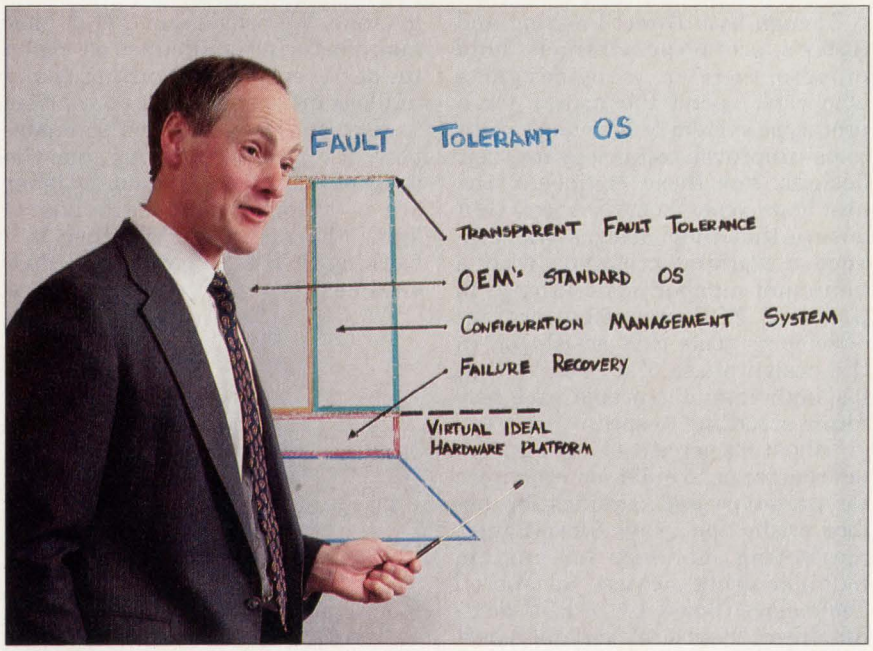

Brian Knowles, vice-president of the OEM technology division at Integrated Micro Products (IMP), says that the trend today is to "push fault tolerance down to the hardware level. That lets you run Unix from Unix System Laboratories and take advantage of the evolution in operating systems." IMP's Open FT3 technology lets OEMs incorporate fault tolerance in their product lines without massive software incompatibilities.

New approach allows painless move to fault tolerance

Tom Williams, Senior Editor

New fault-tolerant technology makes it possible for an OEM to incorporate such a system into existing product lines without exotic redesigns or incompatibilities. The result will be fault-tolerant systems that will run the OEM's own operating system, use the same processors and have the same general look and configuration as other members of the product line. The basis for this claim is a licensable hardware/software technology called Open FT3 from Integrated Micro Products (Los Gatos, CA).

IMP calls Open FT3 a third-generation fault-tolerant technology because it has largely pushed fault tolerance down to the hardware level. First-level fault tolerance called for not only proprietary hardware and a special operating system, but also required applications to be written, according to Brian Knowles, vice-president of IMP's OEM technology division. Second-generation fault tolerance required a proprietary operating system and hardware, but the operating system offered a standard Unix interface for applications. Third-generation fault tolerance now lets a standard Unix operating system be ported to the fault-tolerant hardware environment, although it still requires some specialized drivers and monitor software.

A foundation of CPU sets

IMP is offering Open FT3 in the form of its own 68040-based fault-tolerant Unix system, called XTM, which is both an OEM platform in its own right and a proof-of-concept for the licensable Open FT3 technology.

Open FT3 is built around the concept of redundant "CPU sets." A CPU set can consist of one or more processors, their coprocessors, cache and shared memory—whatever is in the OEM's particular design.

Fault tolerance is implemented by having two or three CPU sets running in synch, comparing their outputs and using a dual, fault-tolerant I/O bus, mirrored peripherals, and multiple uninterruptible power modules. In the case of the XTM, the CPU set consists of one or two Motorola 68040s with local and shared memory on a single board. Multiple boards can be added to make a multiprocessor set of up to eight CPUs—a maximum of four boards containing two processors each. Up to three such four-board, eight-processor sets can be configured in a full-blown system. Adding CPUs to a set permits scaling for performance; adding additional CPU sets supplies a greater degree of fault tolerance.

CPU sets compare outputs. In the case of a three-set system, they simply vote. If two CPU sets are in a conflict, they go to a diagnostic routine to figure out which CPU is at fault. This takes about 100 ms longer than the three-CPU set. "A two-set system is pretty close to perfect," Knowles says. If you're paranoid, add a third set."

A "perfect" system?

The result is a "perfect" core system with an "imperfect," but duplicated, I/O system. The perfect CPU system can, however, ensure the integrity of data by means of protocols. In the case of disks, for example, the system derives checksums and stores them with the data being tested. When the data is read back, the system compares the checksums. By also rereading data from the duplicate disk, the system can isolate and correct failures. The same type of protocol comparison is also done for other peripherals at the driver level. The failure recovery capability, therefore, resides in the drivers, which must be designed to understand the matched-pair concept used for I/O.

The system software environment sits on this combination of redundant, self-checking hardware and failure recovery software that provides coverage for I/O exceptions and ensures data integrity among CPU sets. The combination creates what IMP calls a "virtual ideal hardware platform." The OEM's Unix or other operating system can be

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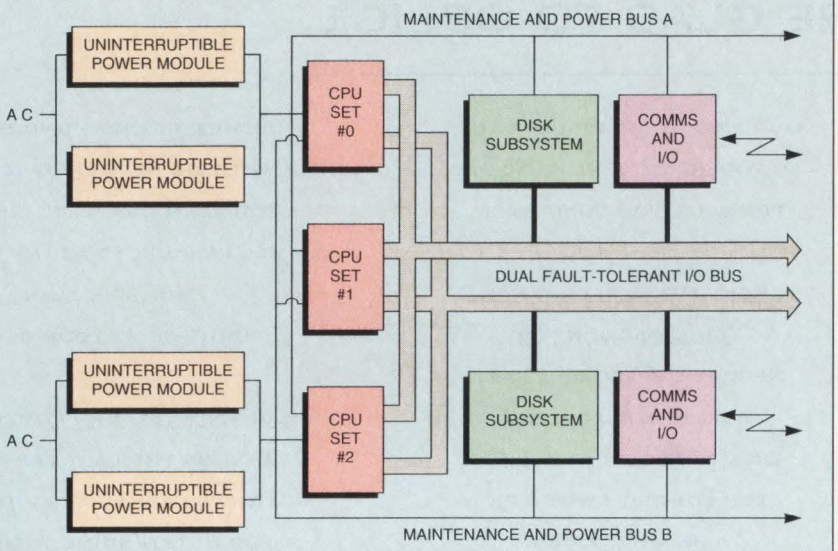
Open FT3 fault-tolerant architecture



IMP's fault-tolerant architecture uses redundant CPU sets that compare and check inputs and outputs, dual I/O buses, mirrored peripherals, and multiple nonstop power supplies. Special failure recovery routines are built into the peripheral drivers to resolve differences, find faulty modules and alert management software. Configuration management software can automatically signal a user, dial a service facility and let subsystems be taken off-line for replacement while the system is running.

ported to the hardware environment, along with a configuration management system (CMS) provided by IMP. "The ability to run the OEM's operating system," says Knowles, "lets you take advantage of Unix's evolution rather than having to reinvent a proprietary operating system over and over."

Other OSs ported

Operating systems other than Unix have been ported to the Open FT3 technology. Motorola (Schaumburg, IL) has built a call processing system for police, government and utility emergency communications that has hard real-time requirements in addition to needing standard Unix. Motorola was able to integrate Unix along with the pSOS+ real-time kernel from Integrated Systems (Santa Clara CA) on the XTM platform, according to Arun Sobti, Motorola's vice-president and director of private trunked systems. One processor in a two-processor CPU set runs Unix while the other runs pSOS+.

The two operating systems communicate via TCP/IP (Transmission Control Protocol/Internet Pro-

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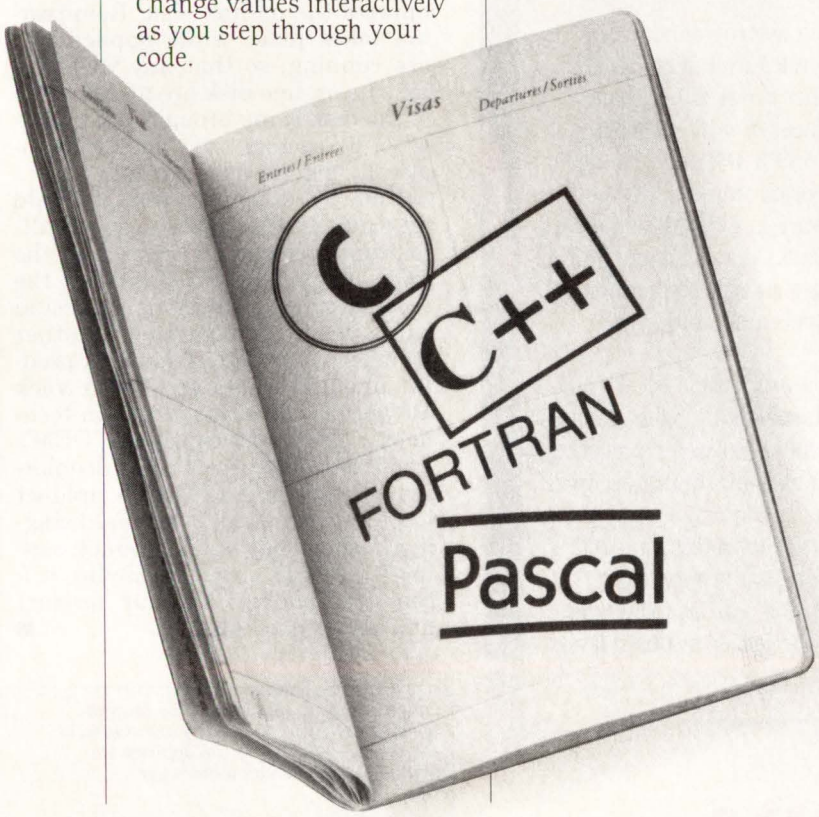

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tocol) on a logical LAN set up in the on-board shared memory space. "The advantage is we put everything inside one box and fault tolerance covers both the pSOS+ and the Unix portion," says Sobti. "Under Unix, we developed the management part of the system- and pSOS+ handles channel assignment and switch control."

The ability to use the Open FT3 technology, however, goes beyond a specific processor, operating system or bus architecture. "If you have some architecture—multiprocessing, caches, shared memory—we say, 'We're going to make two or three of those,'" says Knowles. Each processor set has its own clock, but each is lock-step synchronized using IMP's phase-locked loop technology. On the other side, the OEM needs to add IMP's comparison checker and multiple I/O bus interface technology. "We're talking about a board re-layout," Knowles says, "not using the physical, existing boards."

Doing maintenance

To take boards off-line for replacement and provide for failure recovery, IMP has added a maintenance bus to its fault-tolerant I/O bus. Normal peripheral cards are adapted to the fault-tolerant bus by means of bridge extenders that add to the length of the cards but allow diagnosis and power shut off for on-line replacement. IMP has already created such bridges for VMEbus, MCA and Multibus I.

If the component being replaced is a disk drive, there's disk remirroring software that enables the new disk for write-only until it completely mirrors the on-line disk. Remirroring takes place while applications are running, so that any writes to the one on-line disk are also written to the disk being brought up. Otherwise, its sectors are copied systematically when cycles permit.

Knowles estimates that it would take nine to 15 months to do a fault-tolerant redesign of a system on the order of the IBM RS/6000. But the result would be a system that could run all the applications of other members of a manufacturer's product line and would be able to track advances in operating system technology. "FT3 merges with an OEM's architecture to become a fault-tolerant member of the OEM's product line," says Knowles, "because bringing in somebody else's product, selling it as your own and having it a complete oddball in your product line isn't a good idea." ■

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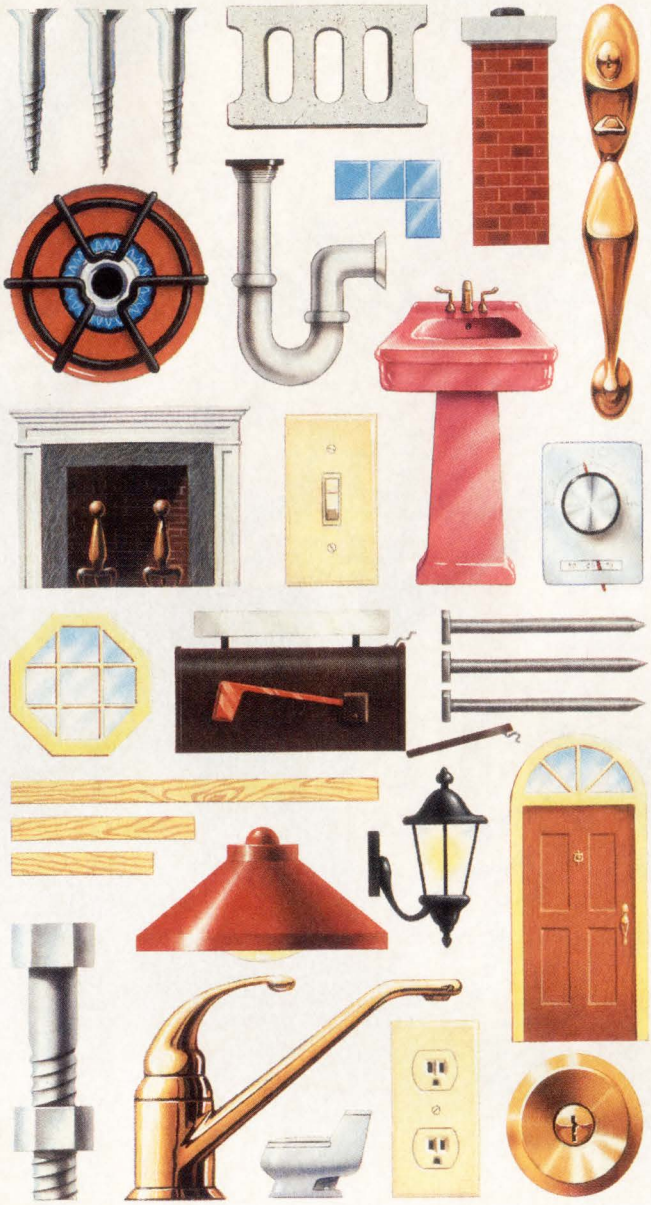

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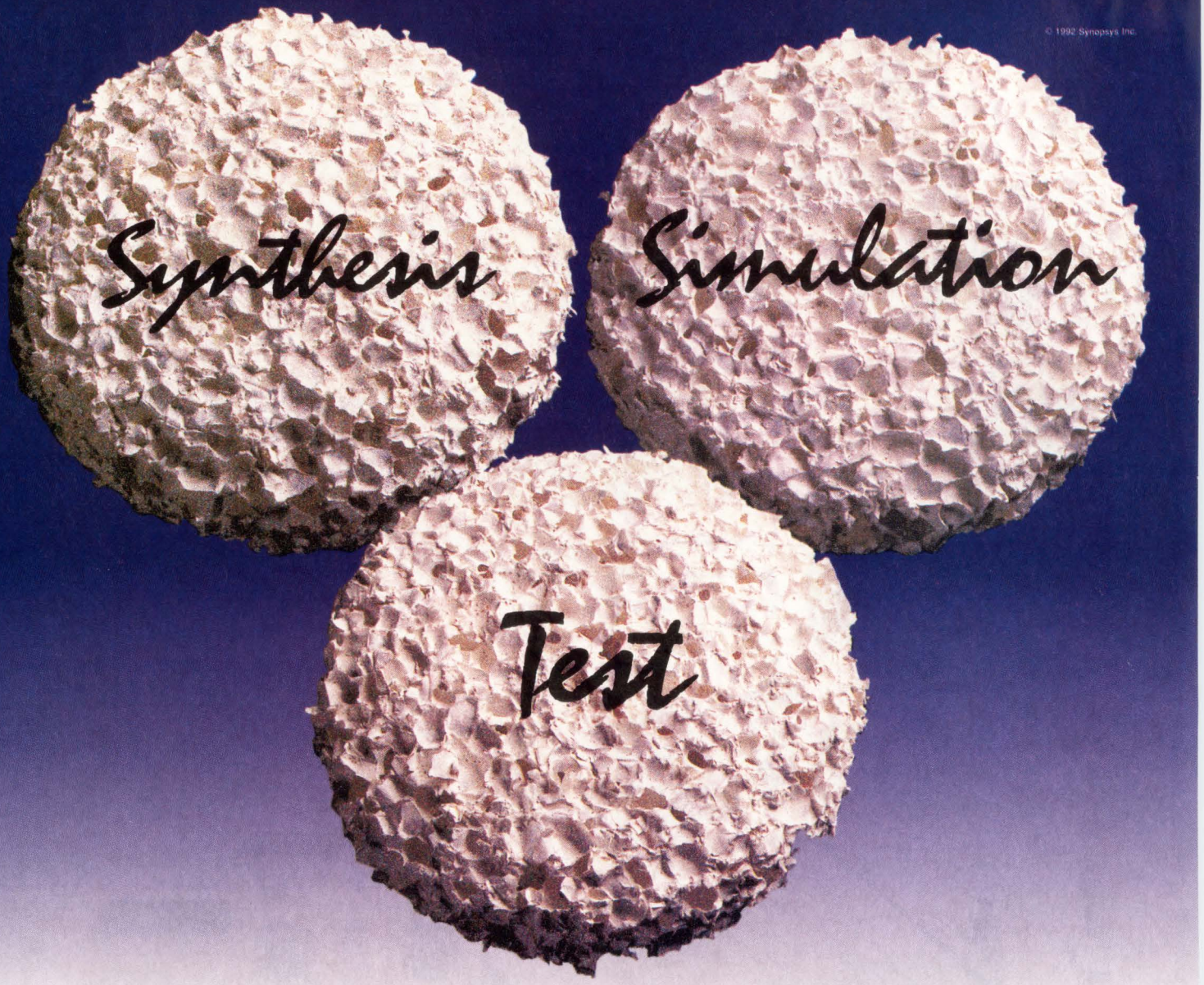

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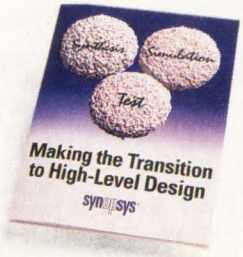

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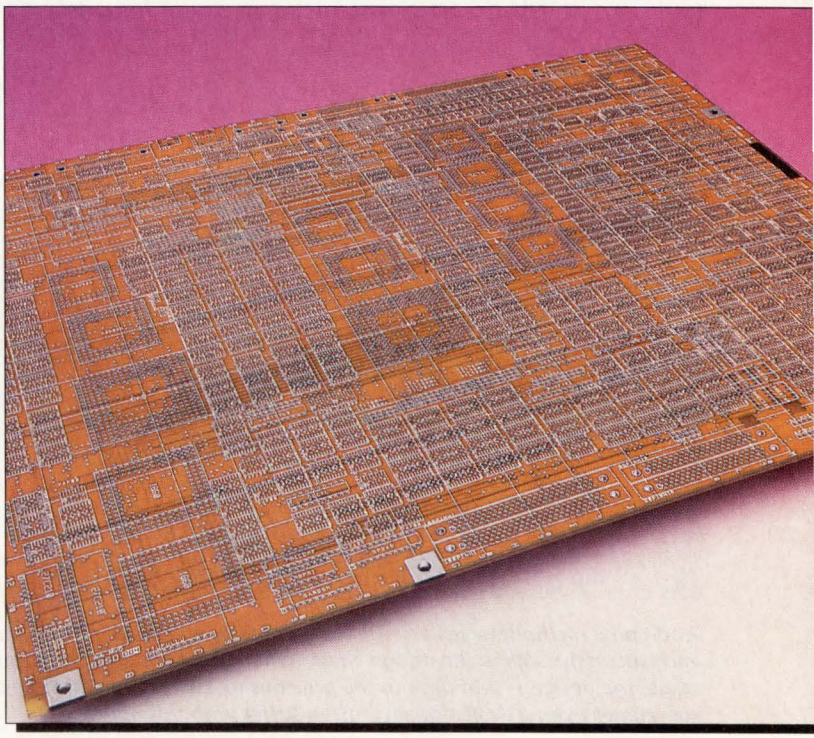
CAE vendors strive to improve link between design and layout

The walls that once insulated PCB designers from manufacturing are crumbling. But whether the responsibilities that go along with the change will be accepted remains to be seen.

Mike Donlin, Senior Editor



This circuit board, a 3-D graphics workstation motherboard, exemplifies the challenges that are invading the realm of the PCB designer. It measures 16 × 18 inches, is composed of 16 layers with surface-mount devices on both sides, and has 23,000 device leads, 3,500 nets, and 8,000 wires.

Printed circuit board (PCB) design and layout are no longer simple electrical and mechanical tasks performed by separate groups of engineers and layout specialists. In the past, PCB design strategy was characterized by individual groups finishing their tasks almost in a vacuum, and then tossing the design "over the wall" to the next group. This leisurely design mentality assumed flexible time-to-market windows and regarded multiple prototype iterations as a way of life.

But international competition is sending a jarring message to defenders of this tradition, and corporations are realizing that teamwork must replace the insulated fiefdom mentality that has characterized American engineering. "We keep hearing this term 'concurrent engineering' and it's slowly starting to sink in," says Shawn Larson, product manager at Teradyne EDA (Santa Clara, CA). "The Japanese have used concurrent engineering techniques for years. We see smaller, faster-moving companies adopting these methodologies pretty quickly. But the mature industries, like automotive and aerospace, will take a little longer because they have such an established order. Sooner or later, however, time-to-market is going to sound the death knell for purely sequential design strategies."

From a technical standpoint, the constraints of high-speed components, evolving packaging techniques and the inherent manufacturability and testability concerns that come with these technologies are also changing the way that PCBs are designed. Decisions must be made early in the design cycle to ensure the performance of the finished product without making it too expensive to build or impossible to test.

EDA vendors are responding to these changing managerial and technical developments with tools that will bring intelligence to the design process, so that manufacturability and testability will be built into a design, along with all the rules to ensure a PCB's proper electrical and thermal behavior.

The first challenge is for tool vendors to bring enough expertise to a tool without compromising its performance or making it impossible to use. The second challenge, which is perhaps as daunting, is to change the way that design engineers think.

"There's a big push these days to design by committee," says Lee Ritchey, vice-president of engineering at Shared Resources (San Jose, CA), a PCB design service. "Rules are being imposed from a lot of different disciplines, and designers are told that they have to account for these as well as for the behavior of their designs. I don't know if it really makes their job much more difficult, but it does take a toll on their egos. Many designers think of themselves as artists and don't want to have their ideas compromised by the grim realities of manufacturing or test. There are some engineers who resent the new way of doing things, but a growing number seem eager to embrace it. It's not hard to predict who will survive. Those who want to retain their prima donna status will be eliminated."

Challenges of the serial design process

Design issues	PCB layout issues	Fab issues	Test issues
• Meet performance specs • Keep project on schedule • Keep project within budget	• Specified component not available yet • Too many components specified for the board • Components fit, but there's no room to route • Designer's placement constraints don't fit with the geometry of the board • Not enough information to route critical lines	• Design/layout used more layers than approved vendors can manufacture in volume • Components not automatically insertable • Trace widths too small or tight to be manufactured • Pad sizes too small to fall within drill and location tolerance	• Not enough test points in design • Design too dense to be testable—bed of nails testers can't touch pins • Board fails in environmental test (designer specified wrong part) • Timing tolerance too tight for reliable operation

Traditional methodologies assume that problems will be identified and corrected by each successive link in the design chain. When problems are encountered at any stage, the design is sent back to the previous phase for rework. Time-to-market, and sometimes overall design quality, often suffer with this approach.

Tools facilitate choices

To convince design engineers to take responsibility for what were once considered mundane concerns, EDA vendors are developing tools that help them understand the implications of their design decisions, particularly in component choice. While the electrical needs of a design dictate the behavior of a device, there are other decisions, such as package type and component location, which are flexible and need to be taken into consideration for automated manufacturing.

"The traditional ways of solving these manufacturing problems might have worked with older technologies, where all the design rules were spelled out in little books," says Dick Pommer, manager of product development at Litronics (Costa Mesa, CA), PCB designers. "But if you're designing with new technology, the guidelines are shifting constantly and you need to know the latest assembly rules. In fact, the manufacturing equipment that your design will encounter might not even be installed yet."

The key to keeping abreast of these ever-shifting design rules is flexibility, something that EDA vendors are starting to build into their front-end tools. Mentor Graphics (Wilsonville, OR), for example, has introduced Manufacturing Advisor PCB, a tool developed by Texas Instruments' Information Technology Group (Plano, TX). It warns you of parts-related manufacturing problems early in the design cycle.

Before beginning a schematic capture, you can enter a parts list for preliminary analysis. The tool monitors the consumption of PCB area as parts are added to a design and, if real estate constraints are exceeded, provides guidelines for alternative mounting possibilities to produce a smaller footprint. Manufacturing Advisor also assesses the autoinsertability of the chosen components on the PCB. As the design is refined through schematic capture and layout, the tool identifies parts that may have unusual labor requirements, special manufacturing processes, high risk of manufacturing rework, and failure to comply with standards.

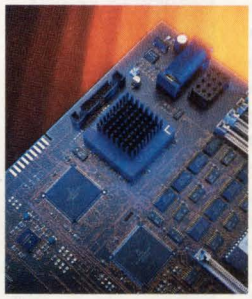
"These issues are at the heart of real concurrent engineering," says Jim LeBrun, board station product marketing manager at Mentor. "Package choice is important for performance, but it also impacts the manufacturability of a PCB. Because of this, most designs today are mixed-package types, and design rules become very important. For example, if you have through-hole devices, you have to use wave solder. Surface-mount devices, on the other hand, take some kind of paste application for infrared or a reflow chamber. When you mix the two on a single side of a board, you have a whole different set of problems. You have to place components so that tall devices don't overshadow smaller ones, for example, or watch that surface-mount components don't come loose during wave solder applications. These have traditionally been the concerns of the layout department, but today's high-speed designs can limit the amount of flexibility that they have in altering layout, so the design engineer has to get involved."

Post-layout analysis

Post-layout analysis tools are helping engineers address the concerns of manufacturing and evaluate their designs for soldering rules—an unglamorous but necessary consideration for design integrity. "Soldering represents over 45 percent of manufacturing failures," says John Roth, vice-president of operations for Pacific Numerix (La Jolla, CA). "That means that there's a huge potential to improve design quality by analyzing component placement during the design phase of a PCB, as well as by optimizing existing designs that have some solder-related manufacturing problems."

MOTOROLA. THE NeXT™ CHOICE.

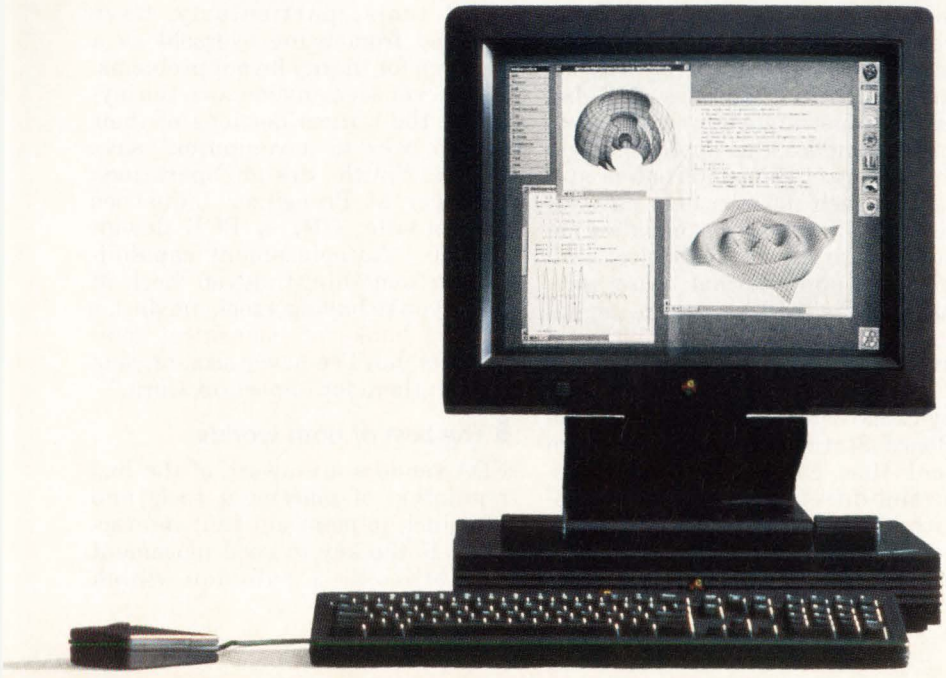
There's a very good reason why the machine shown here is called NeXTstation™ Turbo. Its speed. *Incredible* speed, thanks to NeXT's decision to upgrade to Motorola's lightning-fast 33MHz 040 processor. NeXT was determined to design a machine that offers both speed and an unprecedented number of system features at an affordable price, and they did it. With system solutions from Motorola, an industry leader in advanced ASIC.



The 33MHz 040 processor is only one of the Motorola contributions that turned NeXT's vision into reality. Among the essentials NeXT wanted for the NeXTstation Turbo was super-fast memory transfer, so they chose Motorola's CMOS ASIC for their NeXT-designed VLSI chips. The result is the Turbo Memory Controller (TMC), capable of supporting up to 128MB of fast, interleaved RAM, with prefetching.

The NeXTstation Turbo also boasts a Peripheral Controller (PC) which NeXT designed with Motorola's CMOS ASIC technology, enabling the Turbo system DMA architecture to offload I/O functions for maximum system output - a NeXT key objective. And still another benefit NeXT gained by using Motorola high-density CMOS gate arrays is JTAG Scan Design, which allows utilization of Motorola Mustang™ ATPG software to achieve a dramatic reduction in design cycle time.

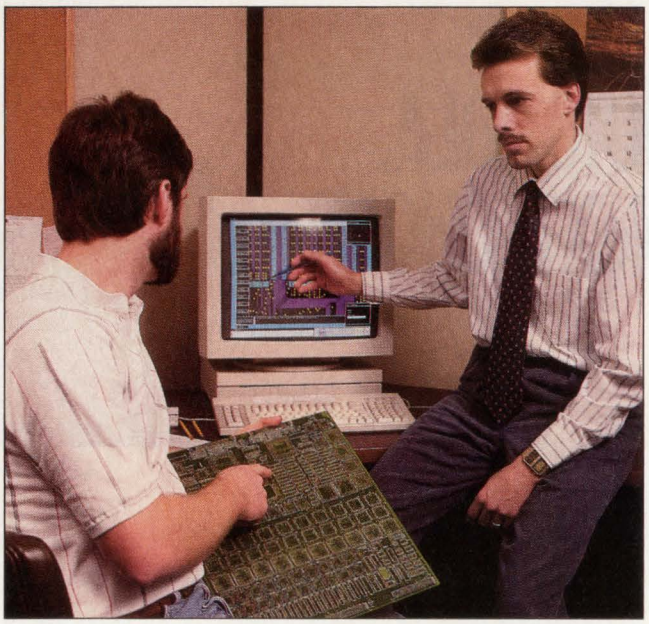
In designing the NeXTstation Turbo, NeXT's primary goal was to be able to offer customers the most machine for the least money. Working with Motorola, they achieved it. Indeed, the NeXTstation Turbo offers state-of-the-art solutions that come from good old fashioned teamwork.



MOTOROLA

Pacific Numerix's tool, SolderSim, lets you validate component placement to detect and correct manufacturing problems such as cold solder joints, solder starvation, board warping, and interconnect cracking. The tool also provides a method for evaluating the performance of soldering equipment and supplies data to assess the effects of manufacturing stresses on the reliability of the PCB.

Manufacturing constraints are also creeping into routing tools, a domain that was previously reserved for adherence to electrical rules and signal integrity. The newest autorouter from Cooper and Chyan (Cupertino, CA), Specctra 3.0, takes manufacturing rules into consideration during routing of surface-mount devices (SMDs). The tool must consider, for example, the escape distance from a surface-mount pad to the first bend point in a wire. A wire bend that's too close to the surface-mount pad increases the risk of an acid trap that could cause a solder bridge between the wire and the SMD pad. To remedy this condition, Specctra provides a special clearance rule to control this distance and avoid shorts and manufacturing defects.



"We're getting called for advice earlier in the design cycle than ever before," says Steven Smith (right), operations manager at Praegitzer Industries, a PCB design bureau. "For controlled impedance boards, for example, you need to make a lot of decisions before you route your first line. These decisions can impact a lot of other areas in the design cycle, particularly test and manufacturing."

Other pitfalls lurk

Predicting and satisfying manufacturing rules at the front end of the design cycle is only one piece of the puzzle. There are many other constraints, such as signal integrity, thermal management and testability, that must be addressed before a design is ready for manufacturing. This trend toward "correct-by-constraint" or "correct-by-design" is forcing EDA vendors to develop tools that let you insert electrical rules into your design to avoid costly prototype iterations.

"There are two ways generally to embed expertise in a design tool," says Shiv Tasker, vice-president of marketing for packaging and interconnect at Cadence Design Systems (San Jose, CA). "One type of tool gives you information about specific parts as you choose them. These are the manufacturability guideline type of tools. The other lets you build rules into your design, so that at each phase, problems are addressed before the design is sent to the next group. This type lets a designer's specific area of expertise accompany the design so that it's corrected along the way. The finished product should be relatively free of bugs."

Cadence's latest version of its PCB design tool, Allegro CBD (Correct By Design), lets you assign design and technology constraints early in the design cycle. The tool, a layout system for PCBs, hybrids and multichip modules (MCMs), groups constraints into sets. According to Cadence, this approach offers more control than alternative systems, which consider only physical length of traces or parallelism rules. With Allegro CBD, electrical, physical and thermal constraints may be defined to ensure signal integrity, reliability, testability, and manufacturability.

Mentor's entry into the "correct-by-construction" competition is the Board Station 500, a PCB design tool that combines timing-constraint-driven place-and-route algorithms and high-speed analysis capabilities. The tool lets you specify a set of electrical rules such as method of interconnect, topology constraints, allowable interconnect delays, and impedance characteristics. The system then automatically maps these rules into a set of physical rules for subsequent use by automatic and interactive place-and-route algorithms.

Too good to be true?

If there's a danger in all of these tools, it's that they might lull you into a sense of false security, content in the knowledge that the computer is at the helm and will prevent catastrophes. "There's a persistent belief that EDA vendors can put all the expertise in a tool and relieve you of engineering," says Shared Resources' Ritchey. "Some engineers are looking for that silver bullet that will let them abdicate responsibility and rely solely on a tool. Unfortunately, there are some EDA vendors out there who will sell you a tool that promises to do just that. The simple truth is that tools will never replace engineering expertise."

Unfortunately, the EDA industry's unrealistic claims for many of its tools over the years have fueled a backlash, so that even tools which deliver what they promise might encounter skeptics who have been burned by exaggerated claims in the past. Placement tools, particularly, have suffered from being oversold as a panacea for thorny layout problems. "I've never seen anyone turn the layout of the critical portions of their design over to a computer," says Steven Smith, design operations manager at Praegitzer Industries (Wilsonville, OR), a PCB design bureau. "Autoplacement capabilities are something that you check off when you're buying a tool, maybe for placing banks of noncritical components, but I've never seen anyone rely on them for important work."

The best of both worlds

EDA vendors are aware of the bad reputation of placement tools and are quick to point out that interactivity is the key to good placement capabilities—a solution which

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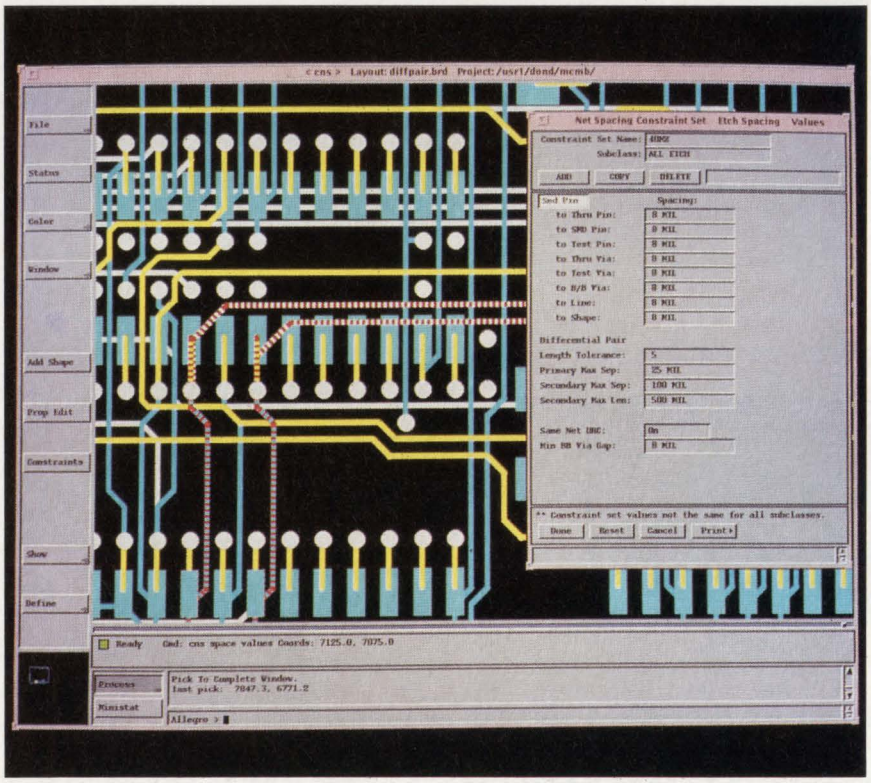
CIRCLE NO. 45

would let the tool guide you toward a rule-driven placement without wresting authority or ignoring human expertise. This combination of human/computer abilities seems to be a necessary partnership, especially when you lay out high-speed boards. "The PCB we just finished was a challenge for our designers and our tools," says Jim Stone, technical manager at Intergraph (Huntsville, AL). "The board was a 24-layer PCB, mainly SMD, with nine pin grid arrays. We couldn't use autoplace tools on the boards, because most of them just look for Manhattan distances, the shortest routable distance between PCB pads. We needed to place components close enough for the fast signals to get where they were going on time without putting them so close that crosstalk became a problem."



Cadence Design Systems' Allegro CBD crosstalk-driven router addresses on-line signal integrity concerns imposed by performance and quality constraints. In this picture, the router has computed the backward crosstalk generated by the new addition of a line segment and indicated (striped traces) that a user-specified electrical constraint has been violated.

One of the critical deficiencies of placement tools is their relative ignorance about routing constraints. Currently, most placement tools work on a user-defined grid, which is often much coarser than the grid the router will use, so the placement tool is limited in its capabilities. These limitations might make the tool too slow, or restrict its ability to rotate parts. EDA vendors are trying to adapt their already-established routing algorithms for placement, so that the two tools will work together—parts will be placed with real routing needs in mind, not just by considering the shortest distance between two points.

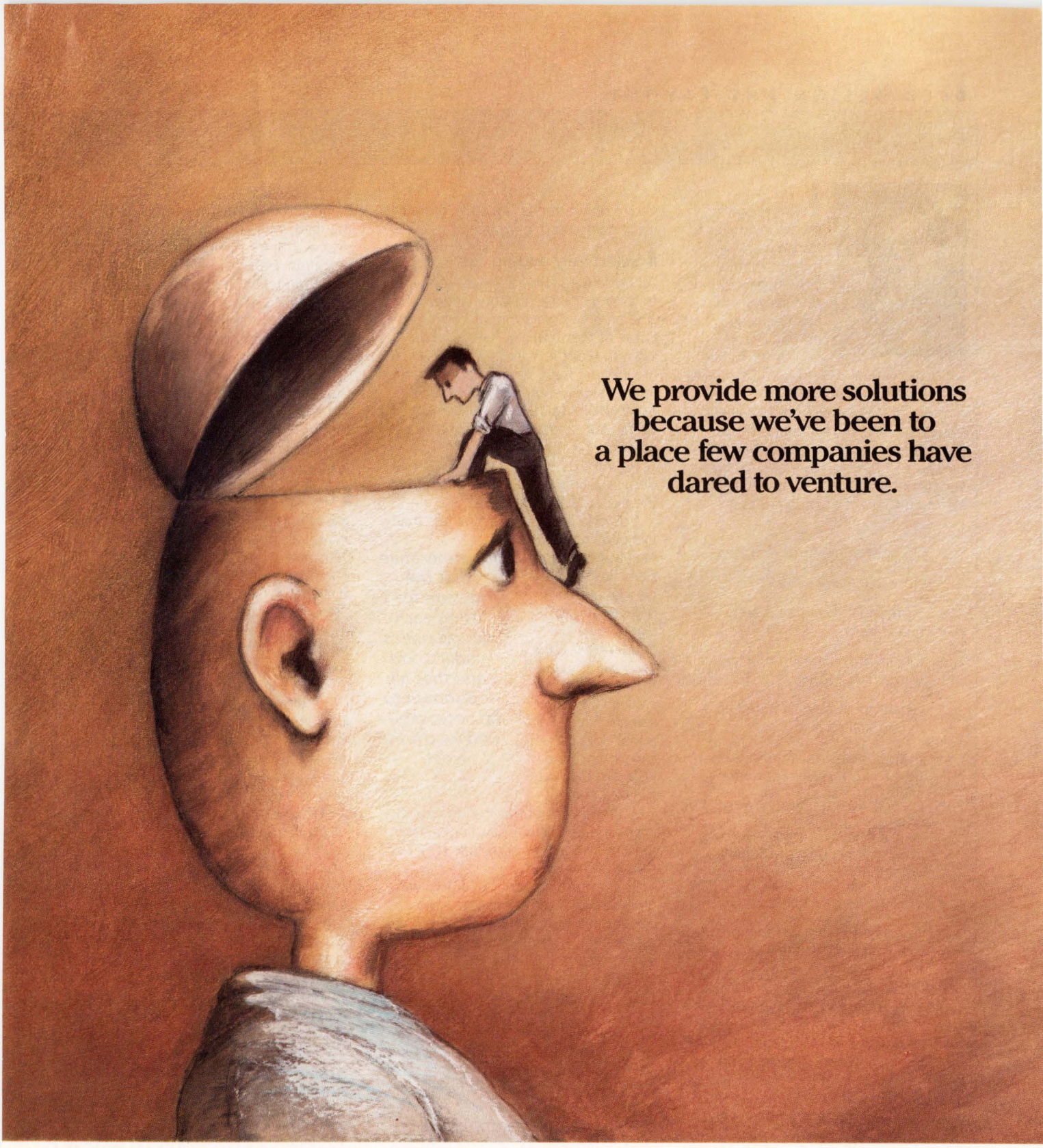
"Our autorouter was developed because that's where the real design bottleneck was," says Andy Slade, project manager for high-performance engineering tools from Racal-Redac (Mahwah, NJ). "We got a lot of customer input to make sure our router did what they wanted, not just incorporate a lot of design rules which would slow it down unnecessarily. We found out that balanced line routing, matched delay routing and even shielded routing was more important than crosstalk. But adapting those same rules to placement is difficult because there are so many more rules—thermal, manufacturing and test—that keep anyone from designing the ultimate autoplacement tool. We think it's best to keep it interactive."

To keep tools from getting bogged down with so many design rules that performance suffers, EDA vendors will have to find ways to let you prioritize the needs of the finished product or modify design rules for your design environment. This presents tool developers with the unenviable task of providing software that's flexible enough to adapt to changing user needs while offering competitive performance. "The idea is to give the engineer the tool that he needs to do the critical part of the design, then pass it on," says Steve Taft, product manager for CAE tools at Harris/Scientific Calculations Division (Fishers, NY). "This means that you let designers weight the priorities for a particular design and give them the ability to change the rules for the next design. For example, are thermal characteristics of prime importance because the product is going to operate in the desert, or is speed the critical capability because your design is going to be hooked to a Cray?"

User-friendly tools

In addition to any technical limitations that layout and design tools face, there are other barriers to their complete acceptance—ease-of-use and ease-of-integration into existing EDA environments. Though many tool suites try to cover all of the needs of designers—from concept to final design and test—most users are leery of buying into a solution that promises this "cradle to grave" approach. Buying into such an environment is disconcerting, mainly because it binds you to a single vendor and keeps you dependent on the vendor's continued success in solving your design problems. It's also unnerving to admit that your past and future designs are tied to a company that might someday go out of business or be purchased by another EDA vendor. And it's just plain naive to believe that any EDA vendor can corner the market on design expertise, particularly in predicting the behavior of a moving target like system designs. For these reasons, users like to remain independent and buy the best point tools for their applications.

Getting the tool to work, however, is a different story. "A lot of the larger vendors want you to marry your design process to their suite of tools, but it's not very practical and it's very expensive," says Joseph Pinzarrone, CAD services manager



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CIRCLE NO. 46

Playing by the rules

In the following list are examples of transmission-line rules that often appear as part of a design specification for high-speed printed circuit boards (PCBs). More often than not, these rules are collected from a variety of sources. They may come from semiconductor applications manuals, an old friend, the last place you worked, and some may even originate in the literature of CAD system suppliers—as reasons to buy that CAD system instead of a competitor's.

- No right angle turns in traces
- No vias in clock lines
- Surround critical traces with guard traces
- Clocks must be routed only on special clock layers
- Clocks must be distributed as differential pairs
- Critical traces must be routed next to layers called ground
- Every active component must have a bypass capacitor
- Route critical traces on outer layers only
- Vias cause reflections
- Transmission-line impedance must be as high as possible

Too often, these design rules are accepted without question as necessary to a successful design. Since they serve as the foundation on which products are built, it's imperative that the reason for using each one is understood and that all are shown to be necessary—and worth the cost. If the only reason given for using a rule is, "We've always done it this way," or "I got this rule from Charlie and his design works," the case can be made that it should be dropped. Because, if you don't understand what you're doing, there's an equal probability of doing harm or good.

Selectively adding cost

All these rules add some cost in the form of extra design labor, added design time and extra manufacturing cost. Some of them can even result in designs that don't work because the rules are inappropriate, and others make it impossible to complete a design. Still others have resulted in replacement of a CAD system because it was unable to comply with the rules.

How these rules can impact the cost or design time of a PCB is illustrated by the examples given below:

1. Clock lines represent far less than five percent of all nets in most designs. Insistence on dedicating a layer or layer pair to clocks results in adding more layers than are required if the clocks are routed with other signals. These additional clock layers can increase the PCB cost by more than 20 percent.

It's imperative that the reason for using each design rule is understood and that all are shown to be necessary—and worth the cost.

2. Prohibition of vias in clock or other lines requires hand routing rather than autorouting, which adds time (and cost) to the design cycle.

3. Surrounding "critical" traces with guard traces is almost always a manual operation that doesn't lend itself to autochecking. Also, the guard traces require space that could be used for routing active signals.

There is strong evidence from analytical tests and research that such rules are either ineffective or unnecessary in cases involving TTL, CMOS and ECL signals. Therefore, selecting a rule set that is both effective and cost-effective should be done by engineers who understand the electrical phenomena at work in transmission lines. Implied in this statement is the need for engineers to acquire a new set of skills. Acquiring these skills in a short period of time can be achieved by locating an "expert" in the field and contracting for a seminar on the subject. Another approach is a thorough search of periodicals and technical libraries for books and articles covering the subject. After the search is complete, a reference manual covering the areas of interest can be assembled.

Once this new set of skills is acquired, rule set development can begin. The first criteria for adding a design rule should be an understanding of the reason for using it and a demonstration that it provides a degree of control at least equal to its cost.

Design rules well-known

The effects of all the rules listed above, as well as most other topics related to transmission-line design, have been studied at length. Papers covering each of them have been published in technical periodicals or presented at conferences. From these and other sources, engineers can get information to weigh how important each will be to the success of his or her design.

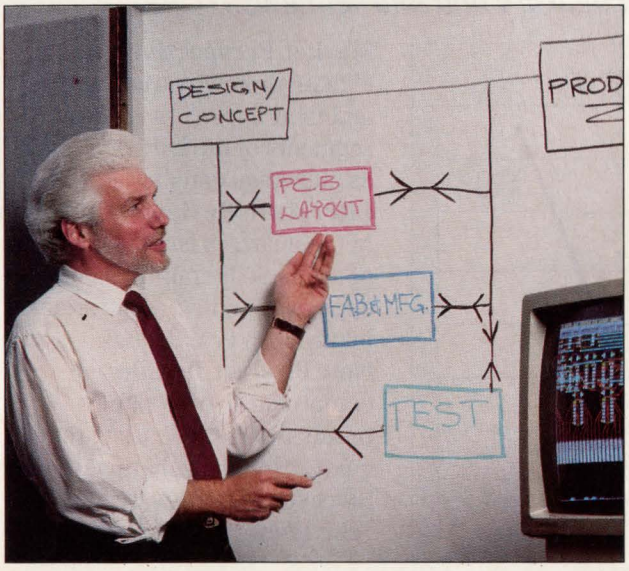
The effects of other phenomena, such as stub lengths, loading effects and net lengths, can be studied using simulation tools. In some cases, the accuracy of simulations is uncertain because of the inaccuracies of the models or components. In these cases, a carefully constructed prototype is the only way to verify the value of a rule.

Collecting a set of high-speed rules from different sources and using them without question or understanding is certainly the easy way out of a tough problem. It's also the easy way into an even tougher problem—a product that doesn't work, is late to market or costs too much. Relying on a set of CAD tools to provide proper design rules is just as easy—and just as dangerous.

Success calls for good, old, engineering knowhow. It's much slower to do the legwork, but much more likely to result in a design that's successful coming out of the chute. This kind of engineering was done in the past as a matter of course—maybe it's time to get back to it.

Lee Ritchey, vice-president of engineering, Shared Resources, San Jose, CA

at Logitech (Fremont, CA), a manufacturer of peripherals. "So we often choose point tools for particular problems. The problem with that approach is getting a good interlinking between the tools. If you don't buy into a single vendor's family, you've got to take data from a simulation package, for instance, and try to drive a PCB design package, or backannotate into simulation. Different companies have different philosophies. I'd shy away from any company that's not willing to help you integrate tools into its suites."



"The only way to control all the elements that make up a successful PCB design," says Shawn Larson, product manager at Teradyne EDA, "is to incorporate the needs of layout, test and manufacturing into the concept phase. One of the keys to implementing this strategy is to have strong database and data management tools so you can access information across design disciplines."

Even if you manage to integrate a good point tool into your environment, you still have to learn how to use it. This problem, ease-of-use, is yet another stumbling block for corporations trying to get design engineers to expand their areas of responsibility. After all, engineers are being told to keep an eye out for problems that used to be the sole domain of layout and test departments. If the tools that let them address these problems are cumbersome, most designers will resist using them or sabotage attempts to make them a part of their design environment. "We've evaluated quite a few of the analysis tools out there and they seem to work pretty well," says Dave Bulfer, principal engineer at MassPar (Sunnyvale, CA), a computer vendor. "But most of them take a full staff just to run them. No matter what any vendor tells you, the sophisticated analysis tools don't integrate well and take a lot of up-front input or they can't tell you anything. Even the best tools take a lot of human intervention or they'll give overly pessimistic predictions. It's true they'll cut down on prototype bugs, but it's hard to bite the bullet and commit staff toward integrating and using them."

Letting engineers engineer

If PCB layout tools are to gain acceptance, EDA vendors will have to find ways of relieving engineers of the tedious task of data input and tool tweaking—tasks that are more appropriate for software departments than design departments. The problem is that a tool is only as good as the data that's put into it. Irrelevant information entered into a tool can slow it to a crawl and produce useless results. Conversely, skimpy data will produce unreliable predictions, and the tool will end up in the heap with the rest of EDA tools that promised more than they could deliver. The problem boils down to what is fast becoming the universal complaint among EDA users—lack of adequate data models.

"The problem with developing models is finding someone to input the data," says Joseph Tanous, vice-president of marketing at OrCad (Hillsboro, OR). "It's a boring job for an engineer, but it's too complex for a data entry person. We think the solution lies in the hands of the IC vendors, who can characterize their parts correctly. The way I see it, these vendors have to publish data books anyway, so why can't they provide the same information in an ASCII format that could be directly fed to the tools? Engineers could simply choose what data they needed for results without the burden of keying in data."

The paradox in all of this is that engineers are being told to get involved in all facets of PCB development, but not to waste time performing tasks that could be done by other departments. Frustration levels are sure to rise when you're told to take responsibility for something but advised against getting so involved that new designs are neglected. "It's clear that PCB layout is getting to be more a part of manufacturing than of design, but engineers are getting pulled into it anyway," says Lorne Cooper, vice-president of product development at Viewlogic Systems (Marlborough, MA). "But if electrical engineers have to do too much by hand, they lose a lot of the benefits of up-front design tools like synthesis, because they're involved in hands-on stuff at the back end. And let's face it, the more intervention at the back end of the design cycle, the worse. This all means that there's more pressure than ever on engineers to get it right the first time."

EDA vendors will have to rise to these challenges if they want to sell tools to a skeptical audience of engineers who are watching the walls that once insulated them from mundane considerations crumble. Foreign competition is forcing their hands, however, and concurrent engineering is an idea that will play to a receptive audience if the right balance of intelligence and accuracy can be built into PCB design tools.■

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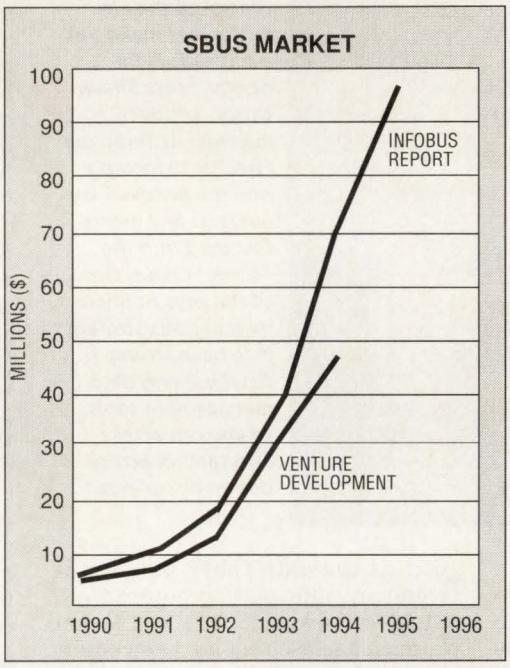

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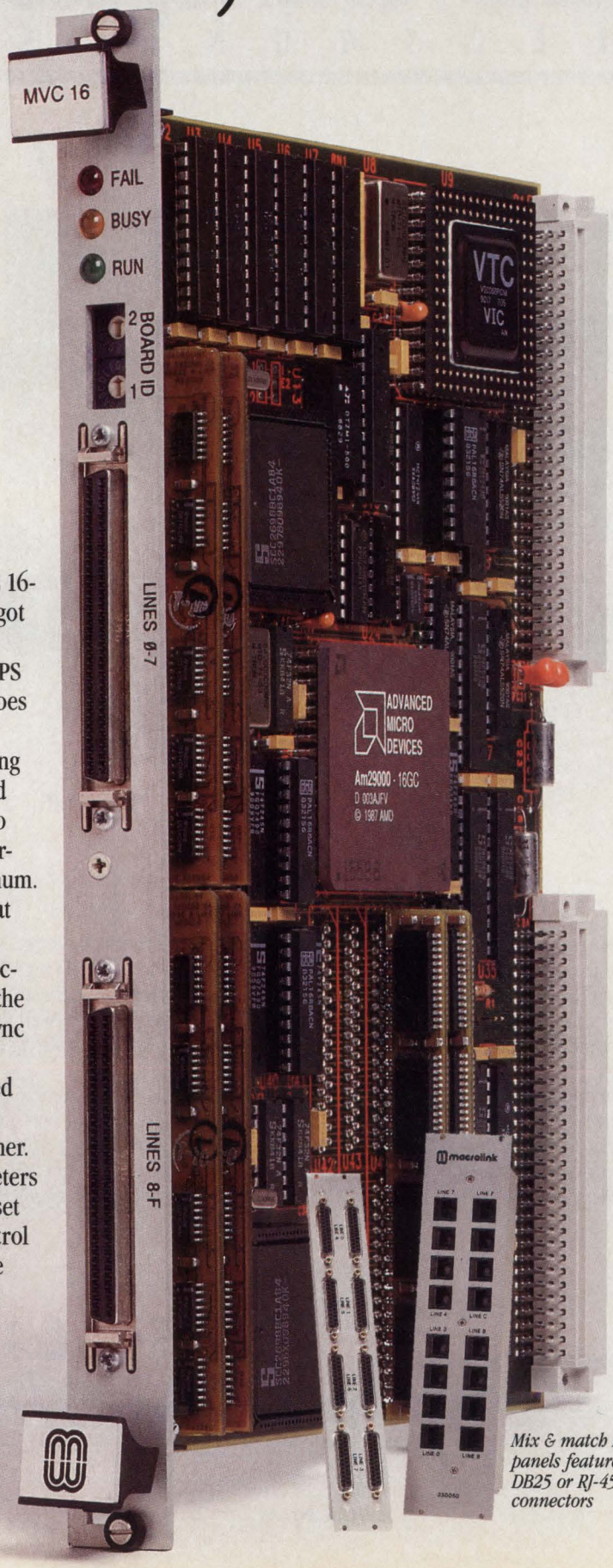

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Minimizing energy consumption through power management

Battery-powered portables will benefit from 3-V ICs, but system-level design priorities such as clock speed and use of a disk drive, rather than the 3.3- versus 3.0-V LVCMOS standard, will have more effect on cumulative power consumption.

Stephan Ohr,
Contributing Editor

John Fairbanks designed the Poqet computer to run for days from two AA penlight cells. To meet this goal, he eschewed disk drives and graphics applications—and even chose a slower processor (a CMOS 8088).

Early purchasers of laptop computers found themselves struggling with two problems related to nickel-cadmium (NiCd) battery stacks. First, the weight of the computer was excessive. Second, the 3-hr advertised battery life was more like 1 hr and 15 mins.

Let's face it—managing the power consumption of laptop computers is a bit like attempting to manage the federal deficit. Once you've budgeted for the VGA screen, the 60-Mbyte hard disk, the keyboard, the 386 processor, and several Mbytes of main memory, there's no power left for glue logic and peripherals such as modems and bus managers. It's a losing proposition from the start. No matter how few microamps of quiescent current the individual ICs consume, the cumulative total is likely to be too much.

Not surprisingly, portable computer makers, in thinking about these two problems, are starting to view their customers as split into two groups with different needs. One group requires a "desktop for the road," a fast graphical computer that runs Windows software and manages big files. This may often serve as the user's main personal computer—the one he or she uses to work at home—with the extra advantage of being portable. The other group is already anchored to a fast graphical desktop, but needs a "supplementary" computer when traveling. Rather than a graphical display or large disk, the more urgent requirement here is lightweight (under five pounds), long battery life (say, five hrs—enough for a cross-country plane trip) and compactness. Ideally, the machine should be small enough to fit with other materials in a briefcase, yet workable on an airplane tray table.

The second group, in fact, may be willing to trade off computer features, such as the ability to run graphically intensive programs like Windows 3.0

or to pull from 60-Mbyte files, for longer battery life. As palmtop computer makers such as Poqet and Hewlett-Packard are proving, it's possible to reduce the size and weight of a portable by using AA penlight cells rather than a NiCd battery stack. But the resulting machine won't have a strong graphics capability or much disk space. It will have a text processor and a spreadsheet capability—enough to keep the business traveler occupied on a plane.

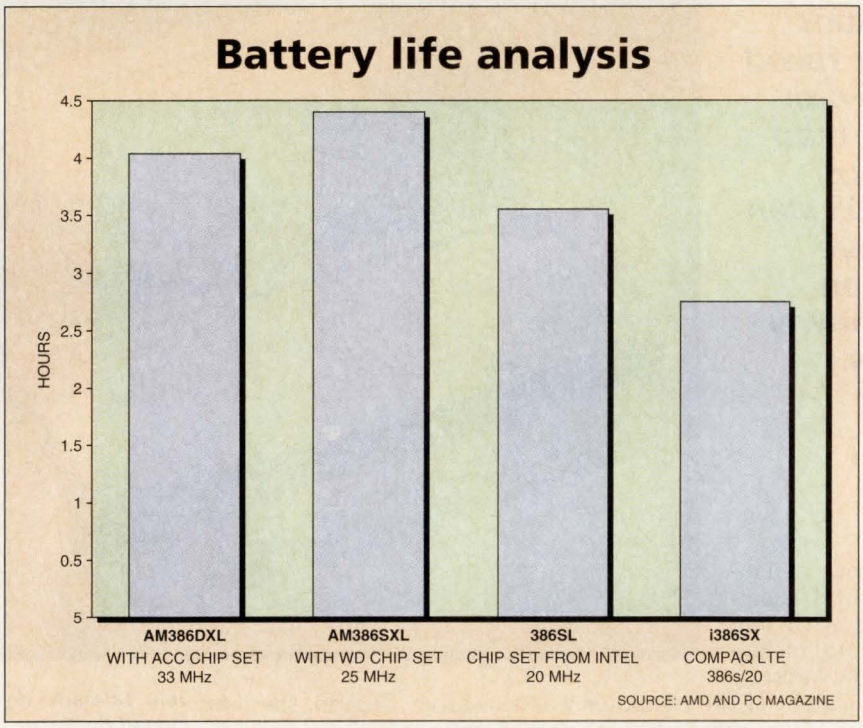
Making compromises

"Power conservation rules against speed," says John Fairbanks, senior vice-president of advanced technology at Poqet Computer (Santa Clara, CA). The design philosophy adopted by Poqet ignores traditional "power users;" Poqet believes that the computer should run no faster than it needs to. Text processing or spreadsheet analysis on an airplane doesn't need blazing speed. By concentrating on these applications, rather than the more glamorous ones requiring graphics, Fairbanks and his team were able to make a series of design choices that resulted in a functional unit with long battery life—100 hrs, using the Poqet for what Fairbanks calls "light data entry."

The power consumption of the microprocessor system is always a function of both voltage and clock frequency (i.e., V^2f). The largest power saving can be realized by using 3 V—two 1.5-V penlight cells, or AA batteries—to power the system rather than 5 V. The second largest power saving comes from turning down the clock speed when the CPU is not fully utilized. Rather than a 386, the Poqet uses a CMOS 8088 microprocessor that's driven by a variable speed clock. The CMOS ICs in the system, because of their small quiescent current consumption, remain on constantly, monitor system activity and turn the clock on or off.

"Power management to computer designers," says Fairbanks, "is really clock management." The computer clocking system in the Poqet design functions like a power regulator—ramping up and down with the frequency of a voltage-controlled oscillator (VCO).

To progressively lower the clock speed, processor interrupts are generated by unused system elements. Activity/inactivity timers generate the interrupts in hardware, although operating system maintenance tasks can obscure inactivity. "It's hard to tell when a DOS-based system is done processing," says Fairbanks. The technique is to turn the clock off quickly at the first sign of inactivity but give the user a quick recovery in case he or she hasn't finished the task. "The system clock becomes a managed system of interrupts," comments Fairbanks, whose power supply is efficient over a 1,000:1 load range. "Most digital designers find this difficult."



In laptop computers, the 3.3-V Am386DXL running at 33 MHz provides almost twice the battery life of a slower 5-V 386SX processor. The key, many semiconductor manufacturers believe, is that a 3.3-V logic standard lets the ICs be connected directly to battery supply lines without going through a lossy power regulator.

The argument for 3 V

Poqet acknowledges that the choice of a 3-V power supply was probably the most important decision in terms of power consumption. There's currently no standard, however, for portable computer batteries, and IC manufacturers are split on whether the reference point for low-voltage CMOS (LVCMOS) should be 3.3 V—a JEDEC standard driven by logic system suppliers—or 3.0 V ±10 percent, a standard that would support portable systems powered by readily available alkaline batteries, and one that recognizes 2.7 V as a logic level high.

For example, Brett Fox, business management director for Maxim Integrated Products (Sunnyvale, CA), sees two markets for 3-V parts. One is 3.3-V logic, which he believes was never intended to support portable operation but rather was meant to get higher speeds from +5-V sources. The other is a real 3-V—or, more properly, 2.7-V—market for ICs designed to operate from batteries.

There are many technical trade-offs between 3.3- and 3-V parts—though these will be somewhat less difficult for logic system suppliers to handle than for voltage converter makers such as Maxim. For the former, the threshold between a logic high and a logic low can be lowered from 5 to 2.7 V. (The 5-V TTL standard, in fact, recognizes anything above 2.4 V as a logic high.) The trade-off is in speed; a 3.3-V logic system, driven from a +5-V rail, will be lightning fast. But the same system, driven from a 3.3-V rail, will not be as fast as an equivalent 5-V system, and the 2.7-V supply will make the system even slower.

For Maxim and other dc-to-dc converter makers, the problem is converting 2.7, 3 or 4.8 V (a typical three-cell NiCd stack) to ±5- and ±12-V rails for use by LCDs, disk-drive motors and communications

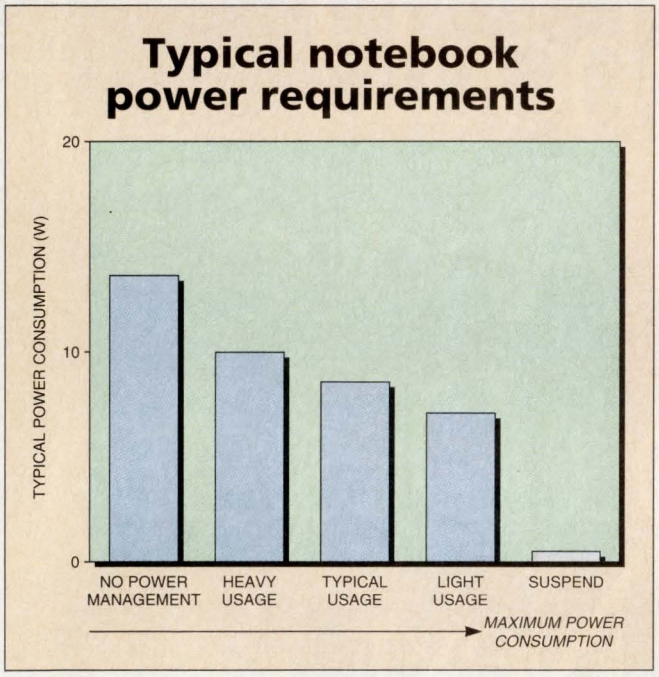
ports. The Maxim technology uses charging capacitors to amplify voltage levels—for example, to produce ±12- or ±5-V swings from a single +5- or +3-V power supply. All voltage converter devices use basically the same capacitor size. While the 3.3-V systems need a charge-pump doubler, 3-V systems require a charge-pump tripler to generate the higher voltage rails. Maxim is committed to providing parts for both 3.3- and 3.0-V applications.

The argument for 3.3 V

The 3.3-V standard for portables was boosted by Advanced Micro Devices (AMD; Sunnyvale, CA and Austin, TX), with the introduction of its 3.3-V Am386DXL microprocessor. AMD claims a 33-MHz Am386DXL processor will provide more battery life than an Intel-type 20-MHz 386SX. Intel has been slower coming on board with a 3.3-V part. AMD cites a *PC Magazine* lab test which compared the AMD processor to the 386SX in a Compaq LTE portable. The machine with the AMD processor lasted 4.04 hrs; the Compaq with the 386 lasted 2.75 hrs.

The machine with the longest battery life—4.41 hours—used an Am386SXL, a 25-MHz clock and a WD76C10 chip set from Western Digital (Irvine, CA). The chip set consists of a system controller, a floppy disk controller and IDE interface, and a peripheral controller.

Western Digital's marketing manager of systems logic, Stephen Ford, believes a 3.3-V logic standard will eliminate power supply losses—typically 10 to 20 percent—by letting manufacturers connect logic devices directly to battery lines rather than be buffered by a power supply—a voltage converter and regulator. Three NiCd cells, for example, will deliver from 3.0 to 4.8 V, depending on the manufacturer, but this voltage needs to be up-converted and regulated to run a 5-V logic system. Even with a highly efficient regulator, up to 12.5 percent of the battery's energy—some 22 mins of battery life—can be eaten up by power supply inefficiencies. A 3.3-V system lets you bypass the power supply and connect logic devices directly to the battery terminal.



Power management—the ability to monitor intermittent I/O activity and shut down inactive devices—will increase the battery life in full-featured portable computers. Just letting the hard disk drive and display module "sleep" when not in use will practically double battery life.

Palmtop of the future

The palmtop of the future, insists VLSI Technology (Phoenix, AZ), will run from unregulated supplies—using 3.3-V rather than 3.0-V logic. VLSI Technology's 82C315 core logic controller will work with 3.3-V circuits functioning at 25 MHz. The 33-MHz systems using the 82C315, however, still need to function at 5 V. The part needs to be fine-tuned for 3.3-V operation at 33 MHz. The 82C315 is supported by a power management unit, the 82C322, which monitors interrupts and I/O activity—read/writes to a device, for example—and turns off unused units.

After the migration to LVCMOS, the most important power-conserving element will be a power management system—one which monitors and shuts down unused peripherals. According to Western Digital, such a system will provide an overall 35 to 40 percent savings in system power. The battery of a typical notebook computer—one with a 20-MHz 386, 2 Mbytes of RAM, a 40-Mbyte, 2.5-in (or 1.8-in) hard disk, a 1.44-Mbyte floppy, and monochrome VGA LCD—will last about two hours. The current drain of the system, with disk drive spinning (but not reading or writing data), is approximately 750 mA. By progressively shutting down various intermittently used functions—hard-disk rotation, floppy-disk access, CPU refresh functions—battery life can be extended beyond three hours. With everything shut down, the total current drain is less than 20 mA and battery life can be as great as 250 hrs.

The biggest consumers

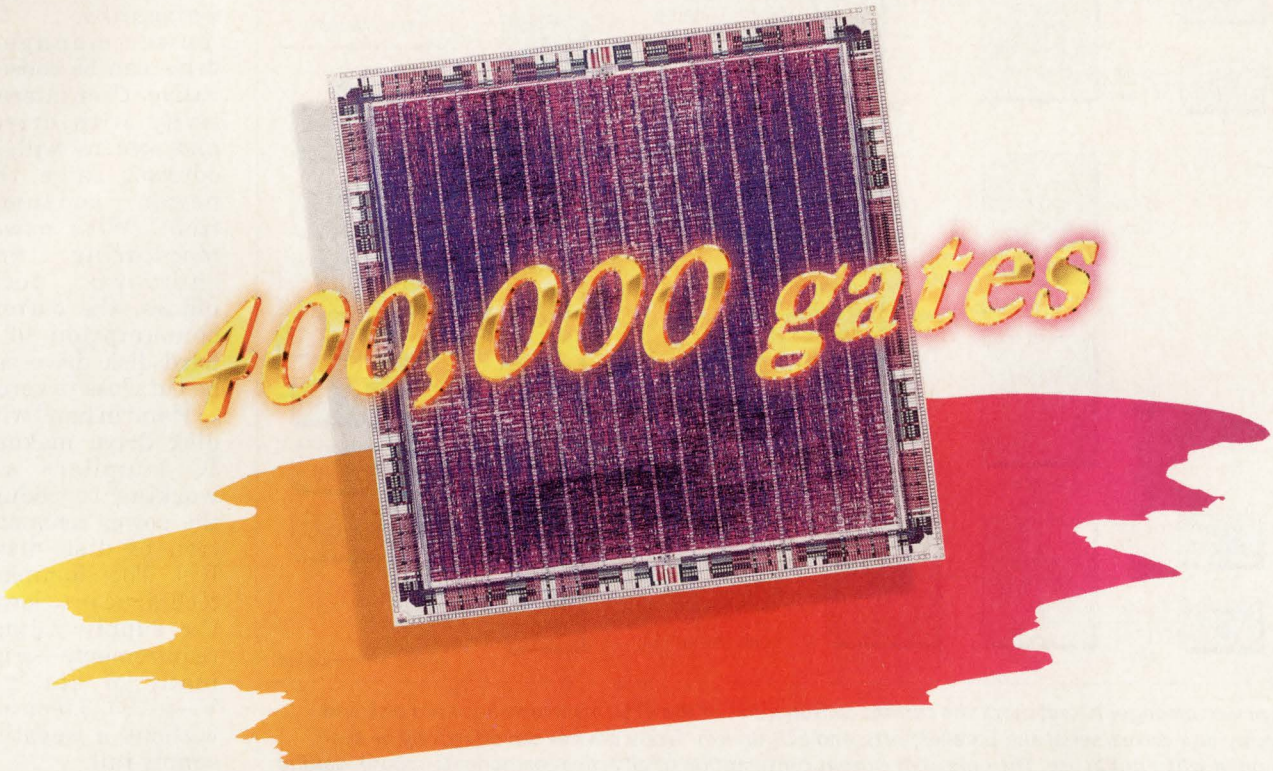
LCDs, hard disk drives, floppies, and communications ports, however, remain the biggest consumers of power. The best power management systems will provide separate monitors for each of these.

The LCD display, for example, requires row and column voltages—along with an illumination voltage—typically higher than the supply voltages. Poqet's Fairbanks used multiple voltage converter ICs, rather than a single high-voltage generator with a power consuming resistor divider, to provide the necessary LCD supply rails. Another power saving—needed by the larger laptop systems—can be realized by selectively dimming the LCD.

The power budget for laptop LCDs is in the vicinity of 600 mW, says Robert Wong, director of standard products for S-MOS Systems (San Jose, CA). To conserve power, the company offers a SPC8100 graphics VGA controller, part of its Dragon chip set. The set integrates a VGA controller, a RAMDAC, a flat-panel interface, and buffer memory. The part has four command-driven power-down modes which progressively dim the LCD screen. The active mode, for example, provides 100 percent power. The power-down modes selectively provide 46, 12, 10, and 0 percent of full power.

Low-power products have been a

Think Performance.



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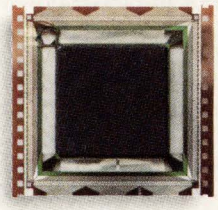

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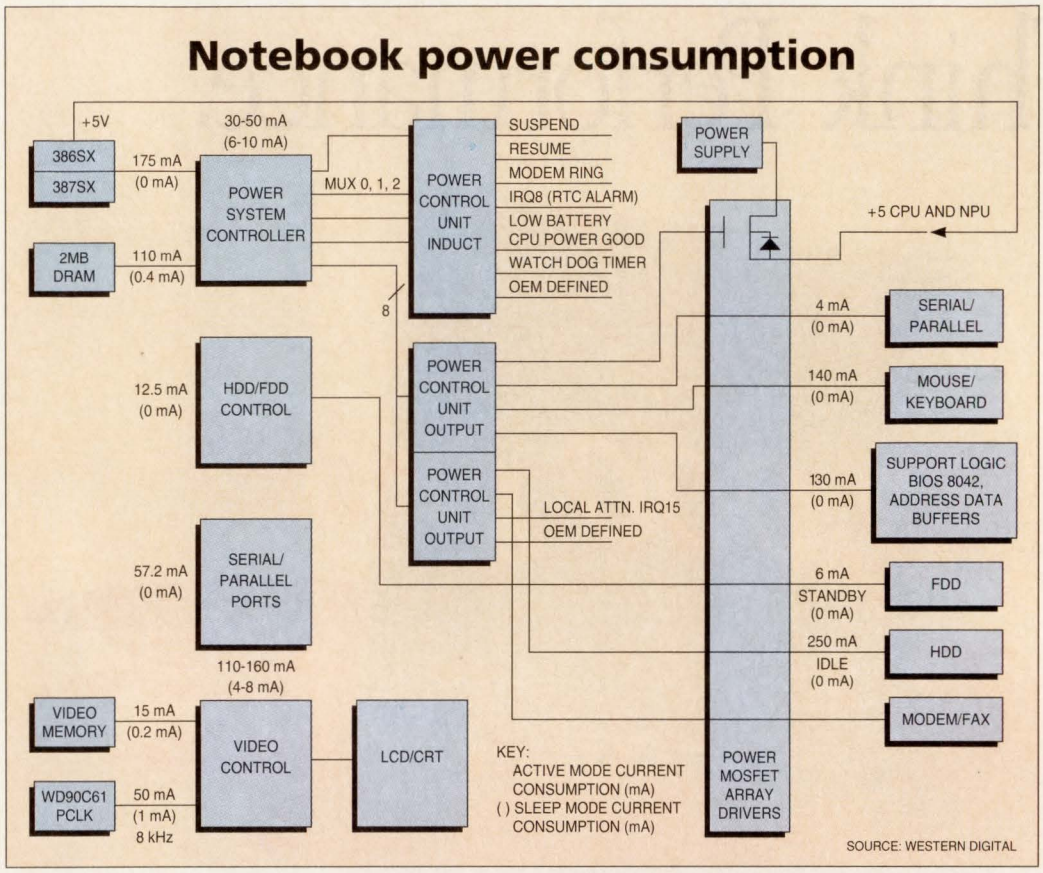

A power manager IC will check the current consumption of the CPU, main memory, hard disk and floppy disk drives, serial and parallel ports, and LCD drivers. These devices can effectively be suspended when not in use. The quiescent current consumption of all active components—those waiting for signals but not reading or writing data—is close to 750 mA. With idle components put to sleep, component current consumption drops to less than 20 mA.

focus of the company, says S-MOS's Wong, since its affiliation with Seiko. As a precision watchmaker, Seiko has consistently sought ICs with low power consumption, low operating voltage and ultrasmall packaging technology. S-MOS's standard products include graphics controllers, LCD display drivers, 3-V SRAMs, and 3-V disk controllers. Since it's uncertain whether 3.3 or 3.0 V will be the low-voltage standard, S-MOS has ASIC cell libraries characterized for both 3.3- and 3.0-V (2.7-V) operation.

Another peripheral IC maker, Cirrus Logic (Fremont, CA), believes that the slow acceptance of a 3.3-V standard means that 3.3 and 5 V will likely coexist in the same portable system. This, in fact, works well for LCDs, which rely on a differentiation between row and column driver voltages. The central core of Cirrus' CL-GD6412 LCD VGA controller is LVCMOS which runs on 3.3 V, while the controller's video memory, host bus interface and screen drivers let you mix 3.3- and 5-V components in any combination. Even with 5-V peripherals, suggests Cirrus product marketing manager Mark Singer, the low-voltage core offers a 50 percent power savings over other video controllers.

Replace the hard disk

While it's impossible to eliminate a display system from a portable computer, it may be preferable to replace a hard disk drive with a large flash or CMOS memory system. Current-generation disk drives can consume 250 mA in an idle, or spinning, condition, and 1 W when writing data, though newer devices such as 1.8-in hard disks from Intégral Peripherals (Boulder, CO) and SunDisk (Santa Clara, CA) are promising considerably less power consumption. The hard disk announced by SunDisk, for example, is expected to draw 3 mA in a sleep mode, 100 mA when reading data, and 200 mA when writing and erasing files.

Poqet's decision to leave out a hard disk drive was made based on space and weight considerations, not on power consumption. "The disk drive is not the consumer," says Fairbanks. "A 'power-managed' drive can be conservative. User interactivity with drives and screens will, of course, raise the power consumption." With power monitoring and shutdown techniques, the current consumption of a hard disk drive can be cut close to zero.

Hand in hand with disk drive makers, IC suppliers are working to reduce the power consumption of disk drive ICs. The dominant technique is to lower the supply voltage requirements—originally ±5 and ±12 V—to 3.3, 3.0 or 5 V without a negative supply rail.

For putting motor drive transistors on the same chip with microcontrollers, Silicon Systems (Tustin, CA) has a 5-V servo and spindle motor driver—the SSI 32H6810—that consumes less than 1 mA in power-down mode. The SSI 32H6810 delivers up to 700 mA of drive current when you need it. Silicon Systems was also the first to introduce a 3-V disk drive controller. The 32C9301 will function from supply voltages which range from 2.7 to 5.5 V, although the maximum data rate will be dependent on supply voltage. At 2.7 V, the maximum data transfer rate is 30 Mbits/s. At 5.5 V, the highest data rate is 48 Mbits/s.

The communications challenge

If you decide to conserve space and weight by eliminating the disk drive, you must provide a means for users to link into their base-computer files. If the user can't carry files on a shrunken, lightweight disk drive, he or she must be able to link into the base-computer through high-speed modems and other com-

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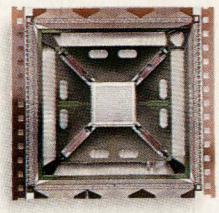

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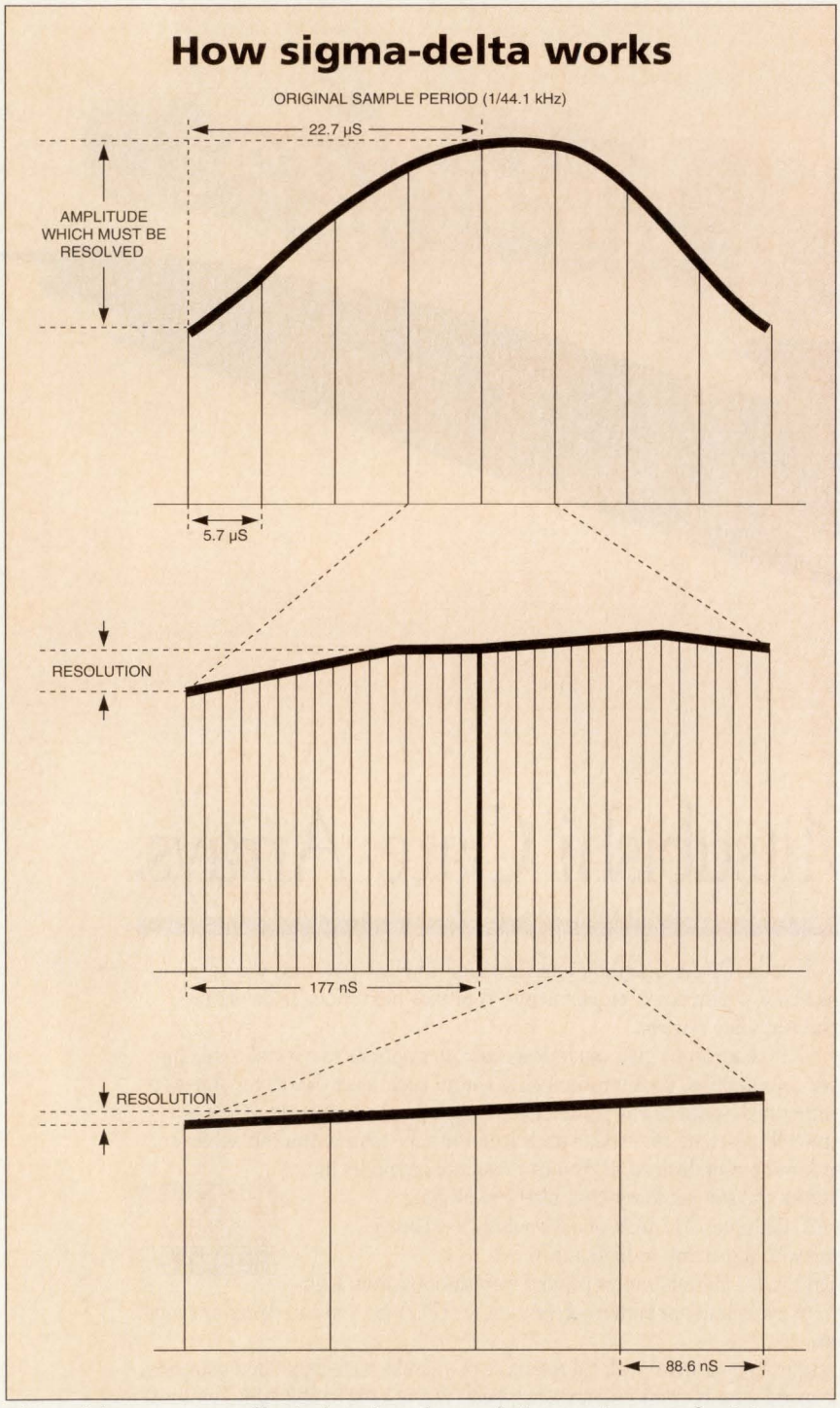
munications devices. But this presents a different challenge for makers of power conserving ICs. Two AA batteries will last 100 hrs for light data entry tasks, but only 10 hrs with modem transmissions.

The problem gets worse as you factor in wireless communication. The super- or ultraportables, such as those produced by Poqet or Hewlett-Packard, keep the disk drive off the unit—not as a means of saving power but as a means of reducing weight—but then use wireless networks as the means of linking the user to his or her database. Poqet, for example, is building a link to a wide-area packet data network called Ardis. This will be supplemented with a short-range network for interoffice communications. From the point of view of IC selection, the problem with this type of communication is that the Ardis wireless network frequency assignments require spread-spectrum encoding and decoding, a form of frequency hopping. This communication scheme-requires a bigger battery to support a powerful transmitter.



Sigma-delta converters effectively reduce the resolution requirements for A-D conversion by dramatically increasing the sampling frequency—by as much as 256 times. In this way, sigma-delta effectively replaces a high amplitude resolution (Y-axis) with a high timing resolution (X-axis). Instead of sampling an audio waveform at 44.1 kHz, for example, sigma-delta converters would sample at 11.2896 MHz. As a result, the difference in amplitude between one sample and the next is so small that it can be expressed as a directional 1-bit.

The problem, of course, is much less severe for modem and serial data communication, where the data rates are only a fraction of wireless communication frequencies. Even with "laplink" communications, the maximum speed is 116 kbits/s, compared to several GHz for a wireless network. Even a RS-232 transceiver, however, can be challenging, reminds Maxim's Brett Fox. "There's no shutdown mode when you're transmitting," he says.

Like the disk drive IC suppliers, semiconductor manufacturers are looking for smaller voltage swings at the communications ports. The RS-232 has two voltage swings, ±12 V in the line drivers and ±5 V elsewhere. A newer Electronics Industry Association/Telecommunications Industry Association specification, 562, is built around a 3.7-V swing, but with a higher allowable data rate. While RS-232 is actually limited to 20 kbits/s, the EIA/TIA 562 goes to 64 kbits/s.

Maxim will deliver low-power RS-232 driver/receivers for both 3.3- and 3.0-V applications. The MAX 560 series is specifically geared toward such applications. The MAX 561, for example, is designed for 3.3 V. It absorbs 12 µA quiescent current at 3 V—about 30 percent of the power of traditional RS-232 transceivers. The part offers partial shutdown by monitoring the line and turning on the RS-232 port only when its receiver sees activity. Parts like these are used in the HP Palmtop Computer.

Reduce the clock speed

As the Poqet example so clearly indicates, reducing the clock speed is an important means of conserv-

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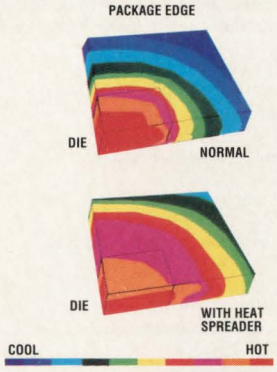

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ing battery power. For notebook computers, Philips/Signetics (Sunnyvale, CA) offers an optimizer circuit based on the 8XC752 microcontroller—a variation on Signetics' 80C51 family. It monitors power lines, and powers down unused portions of the system by turning down the system clock.

"The Philips/Signetics microcontroller can control the speed of the system clocks via frequency select pins on the frequency generator," says Thomas Brenner, the microcontroller product manager, referring to a June 1991 application note. "On-board frequency generators such as the Avasem AV9127 can change the processor clock speed gradually and continuously without violating the minimum high or low times."

The Signetics power management system operates like a state machine, says Beard. It has five states: full power, doze, sleep, suspend, and off. The full power mode is the normal operating mode, obtained when you first turn on the computer. The doze state is entered from the full power state, and is typically controlled by an activity timer. In this state, the frequency generator is instructed to reduce the clock speed. In sleep, power to a peripheral or group of peripherals is removed. Disk drive rotation and LCD illumination are among the first functions to be removed. In suspend, practically all activity ceases, and the power manager takes over the task of refreshing memory and keeping the monitors minimally alive. Any I/O activity, however—keyboard inputs, modem or RS-232 port calls—can singlehandedly bring the system into a full power mode.

The activity sequence is almost exactly the same for the Western Digital WD7600LP power management chip set. With timed inactivity, a 16-MHz clock can be shifted down to 32 kHz, the CPU as well as peripherals shut down, and memory refreshed with a 1 μs pulse. The CPU off-time can be as high as 96 percent.

Texas Instruments (Dallas, TX) makes a one-chip data acquisition system, the TSS400, that may have some utility to battery-powered portables. It's a 4-bit microcontroller with a high-resolution data converter, and offers four different power-down modes. Other devices used to monitor progressively reset power levels include Maxim's MAX 705/707 microprocessor supervisory circuit, which monitors power supply and battery functions in microprocessor systems and provides several watchdog and reset functions.

Improvements in traditional power supply design, such as super-efficient voltage regulators, will also improve the battery life of portables. Linear Technology (Milpitas, CA), for example, has become expert in producing linear 5-V regulators with something like a 0.2-V dropout. For battery-powered portables, the company recently introduced a family of dc-to-dc converters that absorbs about 300 μA quiescent current. The LT1110 converter, to give one example, will produce 5 V at 150 mA from a 1.5-V penlight cell—or 12 V at 120 mA. Like Linear Technology, Unitrode Integrated Circuits (Merrimack, NH) makes a highly efficient pulse-width modulator for switching power supply control.

After we've chiseled down the clock and data transmission rates, lowered the operating voltage for system ICs, halted disk drive activity—and harnessed some new-generation power management devices—there may yet be places to conserve a mA of power. ■

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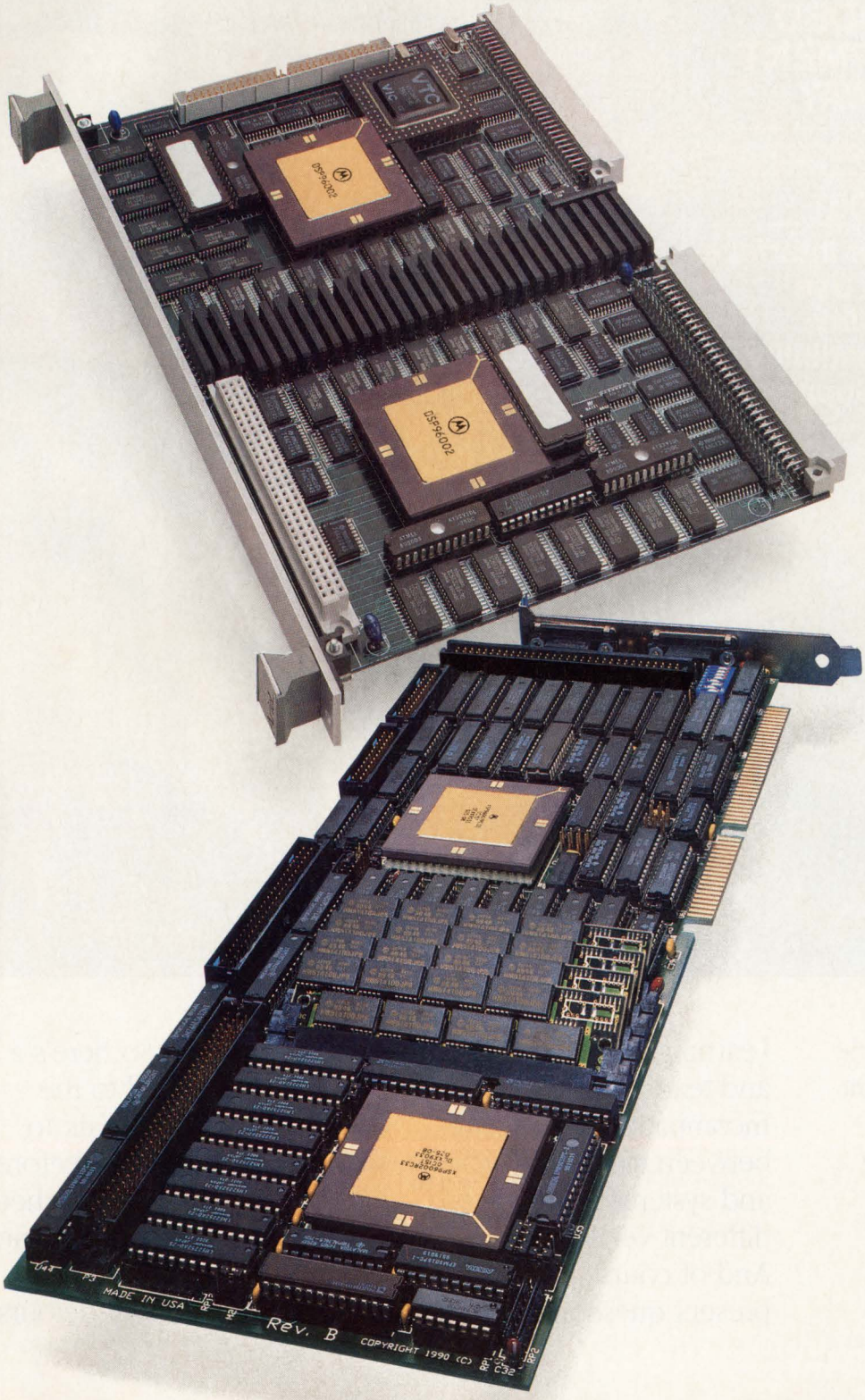

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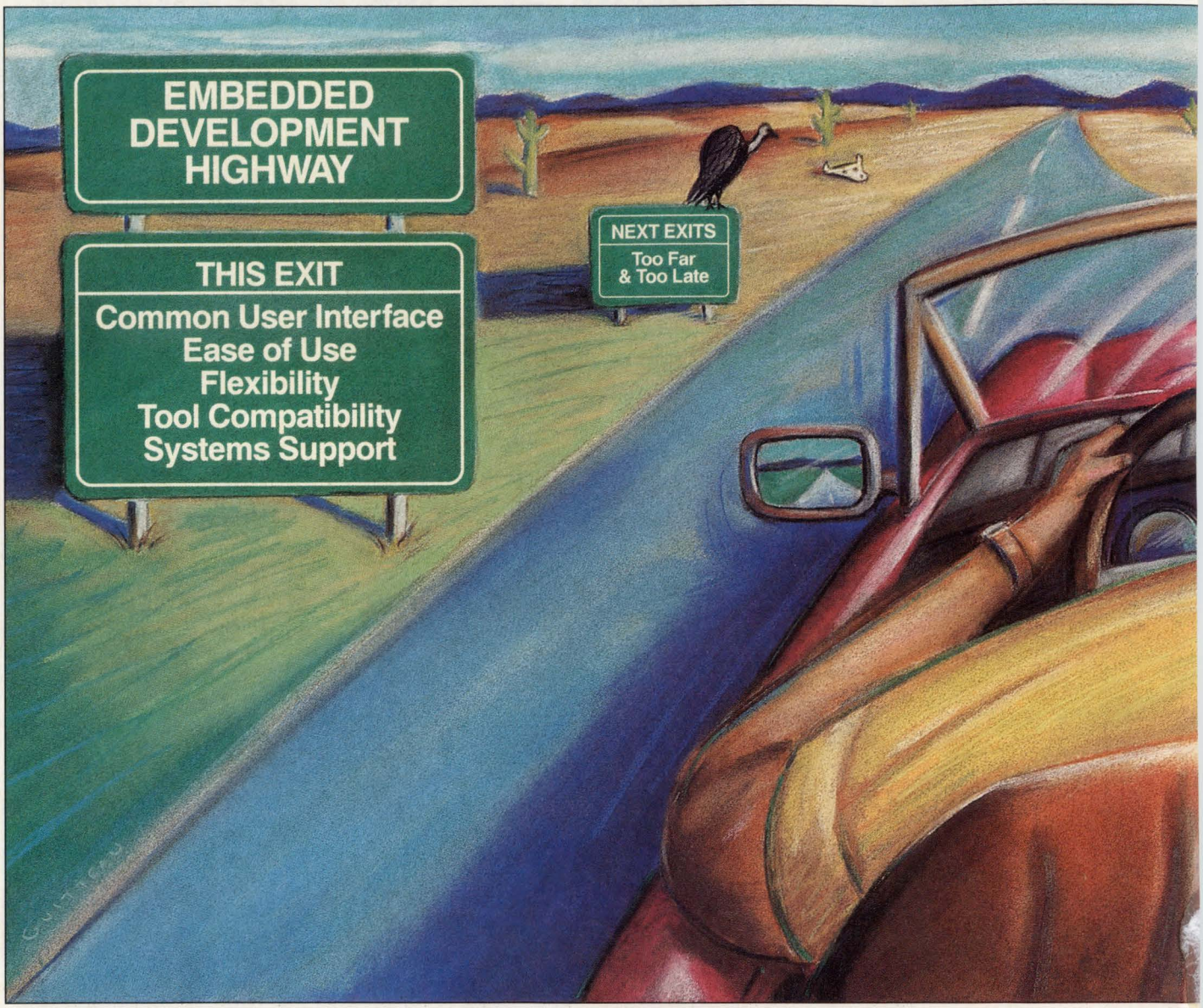
CIRCLE NO. 54

Before you get too far



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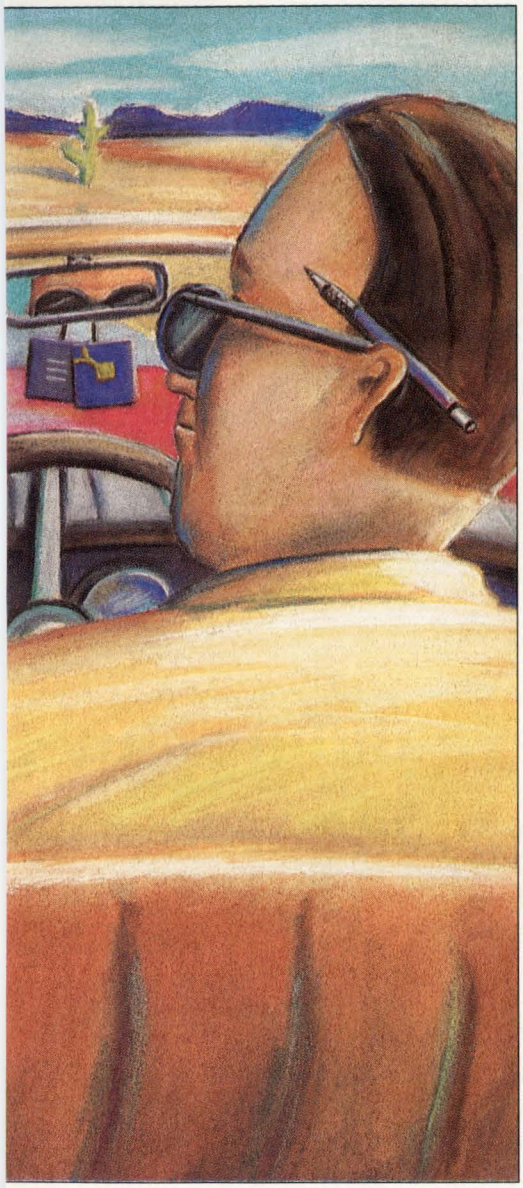

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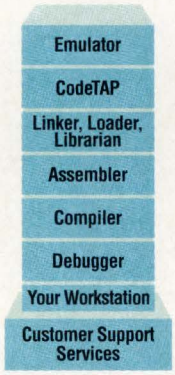

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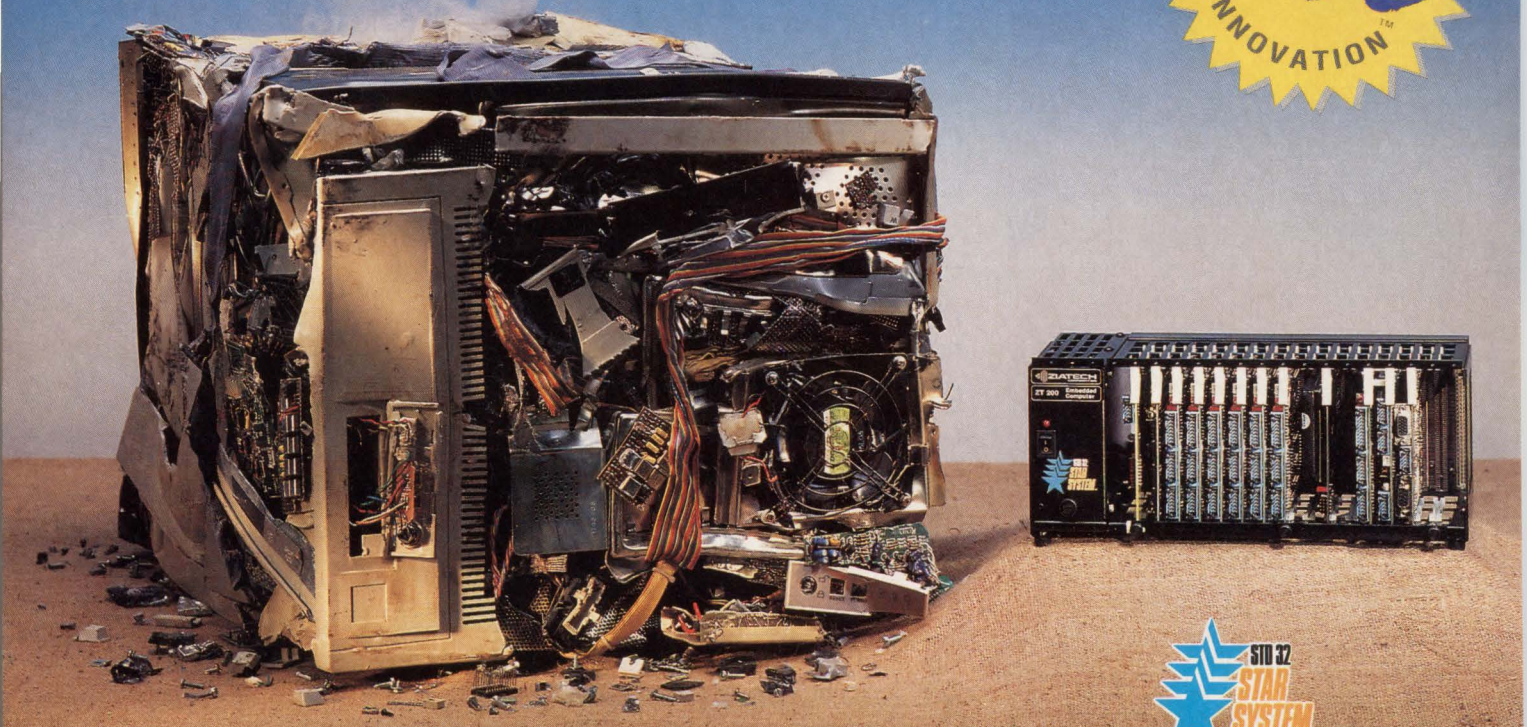

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CIRCLE NO. 56

Analog vs DSP: balancing speed and precision against cost

There are many applications where an analog approach is best in terms of accuracy, speed and cost. But the proliferation of higher-speed components, signal processing algorithms and easy-to-use development tools will soon make DSP the solution of choice.

What's the best way to bend, shape or otherwise transform an analog signal—with analog components and tools, or with DSP? If programmability and precision were the only design criteria, the answer might be obvious. But if you need to balance high accuracy and speed against low component costs and programming effort, your solution will inevitably tilt toward analog.

The future is digital

It's clear that the technology trend line favors digital solutions over analog. You may need a reminder, however, that the microprocessor, digital ASICs and DSPs haven't solved every signal conditioning problem. Although significant ground has been covered, the march toward a totally DSP solution is still advancing—along three fronts.

- The use of DSP depends on the ability to accurately convert a complex analog waveform into digital form. Low-cost, video-speed analog-to-digital/digital-to-analog converters will open new high-frequency applications for DSP.
- DSP will be advanced by new algorithms which consciously replace age-old analog filtering and processing techniques with digital facsimiles. These algorithms are showing up in modem communications, digital audio playback and, soon, disk drive read channels.
- DSP will move ahead thanks to new development systems. A new generation of tools now coming on-line offers graphical methods—not just for

Stephan Ohr, Contributing Editor

developing DSP algorithms, but for programming existing DSPs or synthesizing new silicon.

The biggest drawback to the widespread use of DSP has been its cost, both in silicon real estate and programming effort. While a TMS320—the popular DSP from Texas Instruments (Dallas, TX)—will go for less than $3, you still need an A-D converter on the front end and a D-A converter on the back to implement a minimal filter. With a little engineering talent and a fistful of usable analog parts, the analog gurus point out, you can piece together some remarkably good filters for as little as 38¢.

In fact, many analog component manufacturers offer filter design cookbooks which show you what components to use for each type of filter you want to build—Butterworth, Chebyshev, or Bessel, to name a few. Burr-Brown (Tucson, AZ), for example, provides an active-filter design program that runs on a DOS PC. In operation, you specify the filter parameters and cutoffs, and the software reports the best resistor, capacitor and op amp values to use in a particular circuit. The Filter Pro, as it's called, is naturally keyed to Burr-Brown's precision op amps and universal filter ICs, but its free-for-the-asking and remains useful for many applications.

Medical imaging, such as computer-aided sonography, is one of the few high-performance applications in which much of the signal processing must be performed with precision analog circuitry. State-of-the-art sonography machines, like this one from Acuson, can image cancer cells on the surface of a body organ several inches beneath the surface of the skin. While sonographic scanners operate at frequencies of 2 to 10 MHz, the resolution required is typically greater than 16 bits—a sampling resolution requirement stretching the capabilities of commercially available data converters. Shown on the screen in this photograph are red blood cells in an artery.

Analog signal conditioning circuits—those using resistors, capacitors and op amps—are used extensively in cost-sensitive consumer electronics, such as stereos and telephone answering equipment. The engineering trade-off with many of these low-cost circuits is that the filter functions they implement will never be precise, and the processed signal may reflect a measurable (if not audible) amount of ripple and phase shift.

A DSP, in contrast, provides a much more precise filter function—one that exhibits zero phase shift, and functions adaptively, if need be. The trade-off here is in silicon real estate and the programming effort required to implement a filter function.

But these gross contrasts no longer fully characterize the trade-offs between analog and digital filters. Significant product developments in both analog and digital components and tools make the strategic choices somewhat more difficult. As is the case with disk drive read channels, we'll see analog filters that are extraordinarily precise and programmable. On the digital side, we'll see drop-in DSP solutions—low-cost parts that require no programming. Analog emulation technology, in fact, will make it difficult to tell the difference between analog and digital parts.

Medical electronics

One area in which the transition to all-digital signal processing has been difficult is medical electronics. Ultrasound imaging of internal body organs without surgery or destructive contact requires precision analog circuitry, as well as digital finesse. "The key is to maintain the fidelity of the acoustic waveform coming in from the body," says Ron Buchege, manager of product development for Acuson Corporation (Mountain View, CA), a leader in computer-aided sonography. Like the best signal processors, Acuson's products rely on both analog and digital elements. The digital portion of the system is less for capturing the image than for manipulating it and displaying it on the screen. Acuson's equipment can depict the proportion of red blood cells flowing through a vein or artery, fetal heart anomalies, even prostate cancer cells.

Sonographic imaging systems such as Acuson's are essentially radar processors. Acuson uses a 128-element phased-array antenna, pressed against the surface of the skin, to direct a concentrated beam of energy—which varies in frequency between 2 and 10 MHz—at a particular organ, which is sometimes several inches beneath the surface of the skin. The reflections of the beam are collected by piezoelectric transducers, and then amplified and summed by an analog front end. The key to sonographic accuracy is in the control of the radar beam and in the capture, amplification and manipulation of the reflected signal.

The choice confronting Acuson was where in the signal processing chain to implement DSP. The limitation was not the speed of the A-D converters, according to Acuson engineers, but their resolution. The dynamic range required to distinguish the weak secondary reflections representing tissue textures within an organ from the strong primary reflections from the edges of the organ is greater than 60 dB. While there are A-D converters which function at 20 MHz—the minimum sampling frequency required to capture a 10-MHz signal without aliasing—8-bit converters don't have the resolution to capture the weakest echoes. "A fast, noiseless, distortionless 12- or 14-bit conversion," says Buchege, "was not realizable with monolithic off-the-shelf components."

This need for dynamic range discouraged the use of a single A-D converter for each sensor element in

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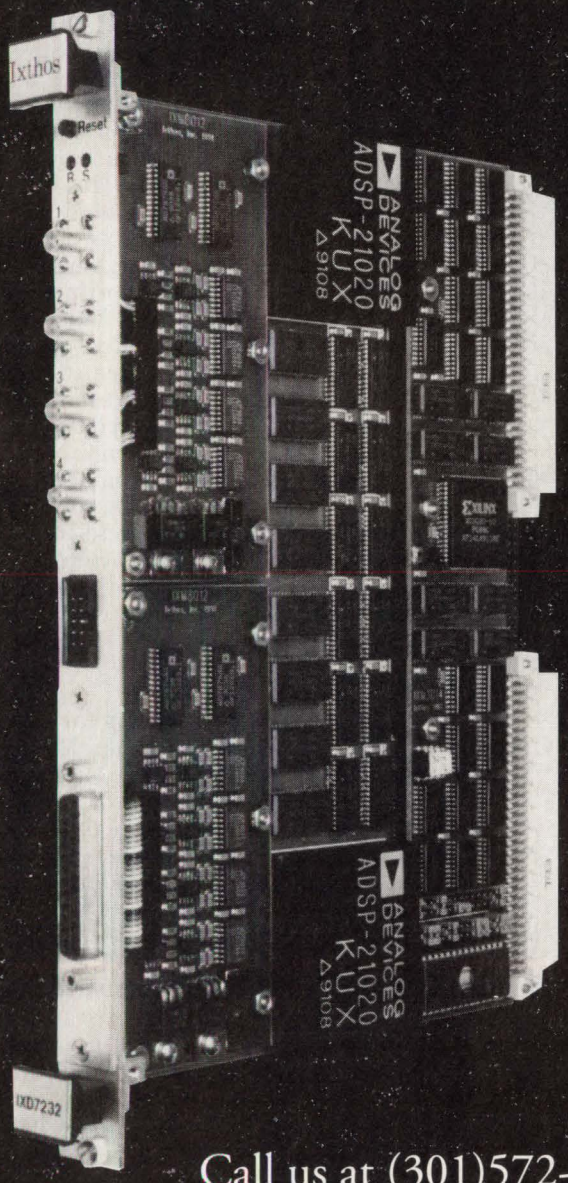

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CIRCLE NO. 57

the phased-array antenna. Rather, much of the engineering went into the analog signal conditioning system which amplifies each of the antenna elements, sums them through precision analog delay lines and then compiles a video composite—at 30 frames/s—from the conditioned signal.

Resolution frequency-dependent

As Acuson's example makes clear, the use of digital wave shaping techniques is dependent on both resolution and frequency. An application where DSP is much more common is speech processing. Telephone systems, for example, use DSP for voice compression, transmission and recording.

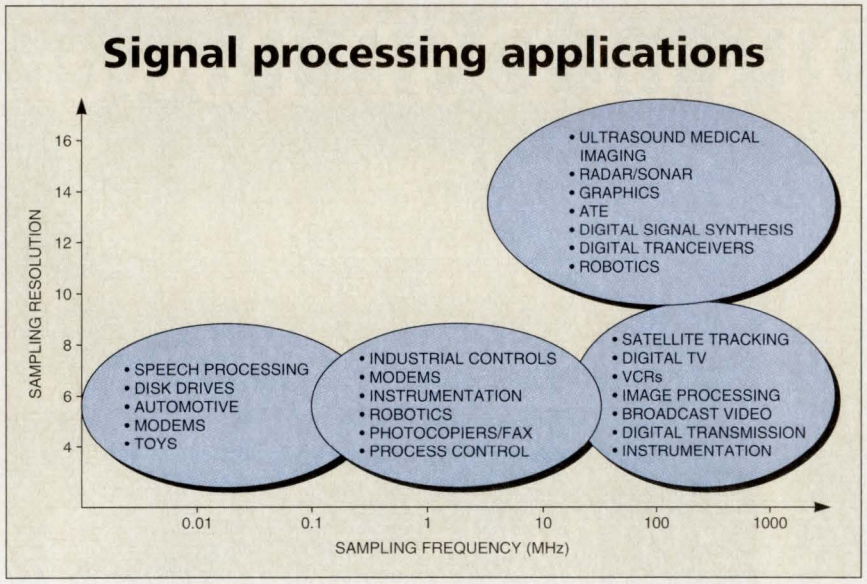
Communication Automation and Control (Allentown, PA) builds single-board computers and PC insert cards used as telephone communication aids for people with hearing impairments. By performing a fast Fourier transform on collected voice data and analyzing it in the frequency domain, the speech processor finds those special frequency components of the voice signal to which the deaf person might be sensitive. The telephone system then amplifies those components. "FFTs are prohibitive in the analog realm," says Jim Bridges, president of Communication Automation and Control, whose boards use the AT&T DSP-32C processor.

But voice processing applications, although complex and rewarding, exist on the opposite end of the scale from medical imaging. They manipulate a lower-frequency signal and have a smaller dynamic range requirement. How high up in the frequency spectrum can DSP be used? "It depends on how exotic you want to get," says Bridges. He sees 3 MHz as the sensible sampling rate for DSP.

DSP techniques have become firmly entrenched in applications where the sampling frequency and the resolution requirements are well below 10 MHz. Yet there are an increasing number of analog signal processing systems that have benefited and will increasingly benefit from DSP. These systems include stereo playback systems—in theaters and auditoriums, as well as private homes—and servo control systems such as disk drive head positioners and automobile brakes. Newer applications of DSP—and the most challenging in terms of frequency—are video image compression and transmission, wireless and radio frequency communications, medical imaging, and radar systems.

Whether the cutoff for DSP's capabilities for particular applications is 1, 10 or 100 MHz really depends on what kind of DSP application you're implementing, says Brian Mathews, strategic planning manager of the linear product development engineering group at Harris Semiconductor (Melbourne, FL). "There are certain applications," he says, "in which the processing is geared toward analog signals; that is, the inputs and outputs are both analog waveforms. The frequency limits will be much greater than data acquisition systems whose input is analog, but whose main purpose is digital analysis and display." The frequency limits of these systems, in turn, will still be greater than those of industrial controls whose output, though analog, is intended to produce some kind of mechanical motion.

Pure analog applications include stereo audio (which can go up to 100 kHz), video signal processing (up to 40 MHz) and wireless radio frequency communications (up to 500 MHz). Most data acquisition systems, in contrast, top out around 100 kHz, and many, like scales, don't require even a 1 kHz bandwidth. Medical ultrasound scanning, in which the signals can go as high as 40 MHz, is an extreme for data acquisition. But it's the high-frequency applications—video, ultrasound and radio frequency communications—that present the biggest challenge to system designers and their IC suppliers. For this reason, says Mathews, manufacturers are under pressure to develop new high-speed IC processes and to perfect methodologies that encourage a transition from analog to digital signal processing realms (see "The high-frequency challenge," p 93).



DSP applications are bounded by frequency and resolution. At one end of the spectrum, voice processing requires an 8-kHz sampling frequency with 8 bits of resolution, and is consequently supported by a wealth of processors, peripheral chips and development tools. At the opposite end of the scale, applications like cellular telephones, video image compression and medical imaging demand components with more than 20 MHz sampling and 12-bit resolution. In such applications, special tools need to be harnessed.

Turning to digital

"People are looking for digital solutions", agrees Dr. Surendar Magar, president and CEO of Array Microsystems (Colorado Springs, CO), which is pushing DSP into video realms. Dr. Magar points out that color processing—the ability to filter and manipulate video frequencies—is critical to implementing new image-compression algorithms such as JPEG and MPEG for HDTV and for interpreting medical images such as CAT scans. In conjunction with Samsung Electronics (San Jose, CA), Array Microsystems is developing a dedicated video DSP chip set, called the A77, which will perform two billion operations (GOPS), and 500 million mathematical operations per second using a 50-MHz clock.

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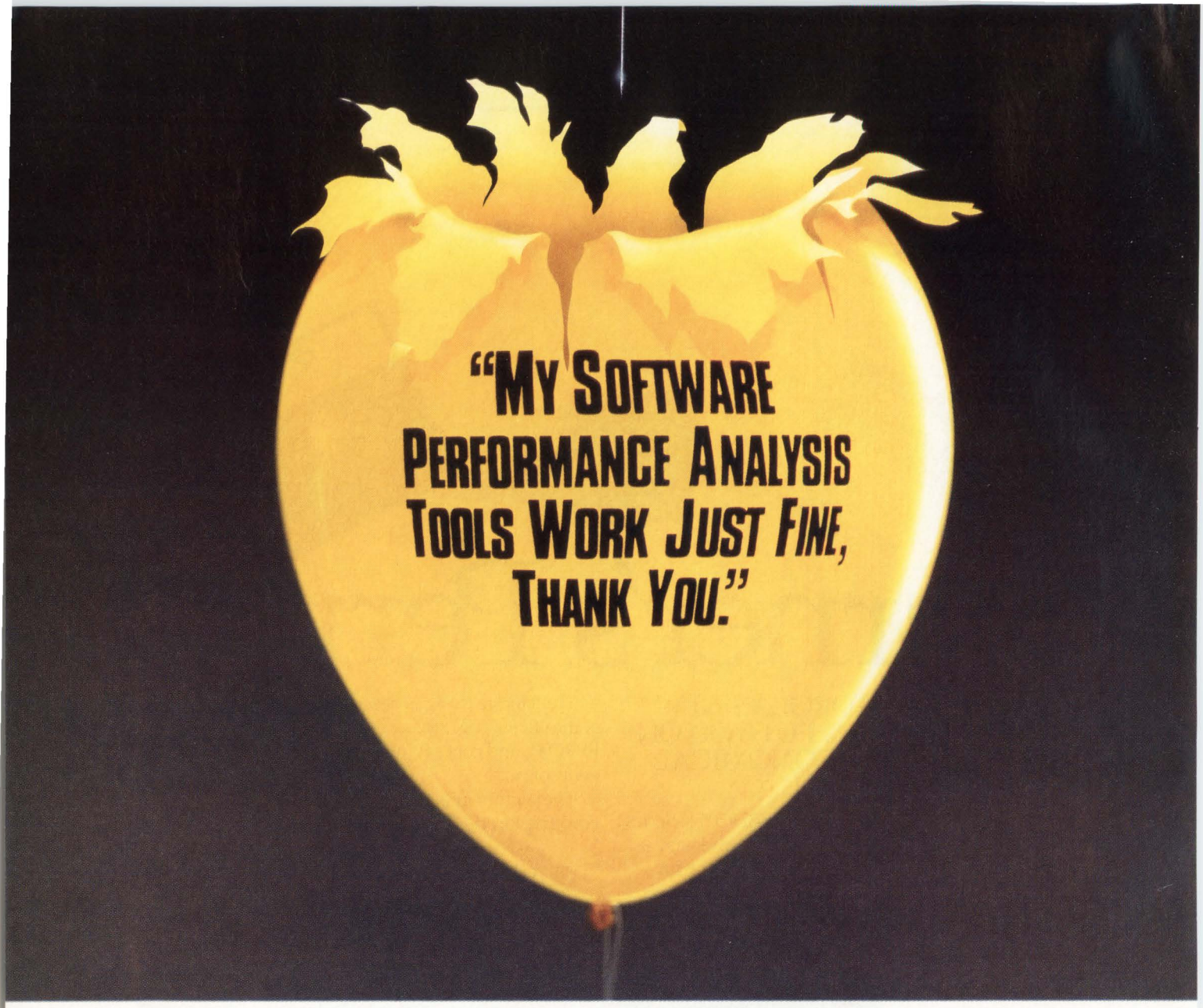

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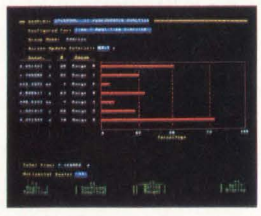

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Test and Measurement

CIRCLE NO. 60

Dr. Magar, however, doesn't see high-speed data converters as a limiting factor for DSP. "Formerly, 500 kHz was the upper limit," says the man who helped develop the TSM320 product family, and also served at Signal Processing Technologies, "but 5 to 10 MHz is not a big problem today. With the newer data converters, like the ones from Signal Processing Technologies, we can just manage at this stage. By the mid-1990s, we will be there."

The SPT9712 from Signal Processing Technologies (Colorado Springs, CO) is one of two recently-introduced A-D converters that elevate the resolution and speed expectations for monolithic A-D converters—an essential ingredient for DSP. The SPT9712 is a 12-bit converter with a 20-MHz sampling rate. The other breakthrough product is the AD872 from Analog Devices (Norwood, MA), which will resolve 12 bits at 10 MHz rates. Both data converters use multiple stages, with a low-resolution flash converter to supply successive stages.

A single-stage flash converter can offer data samples in excess of 40 Msamples/s. The problem with monolithic flash converters is that they rely on a network of parallel comparators to resolve each bit, and the number of comparators required increases exponentially with bit resolution. A 6-bit flash, therefore, will need 64 (2^6) parallel comparators. An 8-bit flash, already a power-hungry device with 256 (2^8) parallel comparators, can't easily form the foundation of a 10-bit flash with 1024 (2^{10}) parallel comparators—at least not as a single chip. Other converter architectures are required to provide both video speed and high resolution.

A-D converter costs a factor

As a consequence, DSP applications will be gated by A-D converter costs. "The 30 Mbit/s and higher DSP solution may be too costly," says Bill Schweber, a technical marketing engineer at Analog Devices, whose company provides both high-performance analog and DSP floating-point solutions. "In fact, over 1 Mbit/s will impose costs." With DSP, he says, you also need to carefully consider your error budget. With analog it's relatively easy. (Op amps are analog multipliers).

Dickson Wong, an engineer with Fujitsu Microelectronics (San Jose, CA), is optimistic about A-D and D-A converters for high-frequency DSP applications. His company is developing video-speed A-D converters capable of processing 60 Msamples/s—albeit at resolutions considerably less than 12 bits. "The trick," says Wong, "is to sell these for $5."

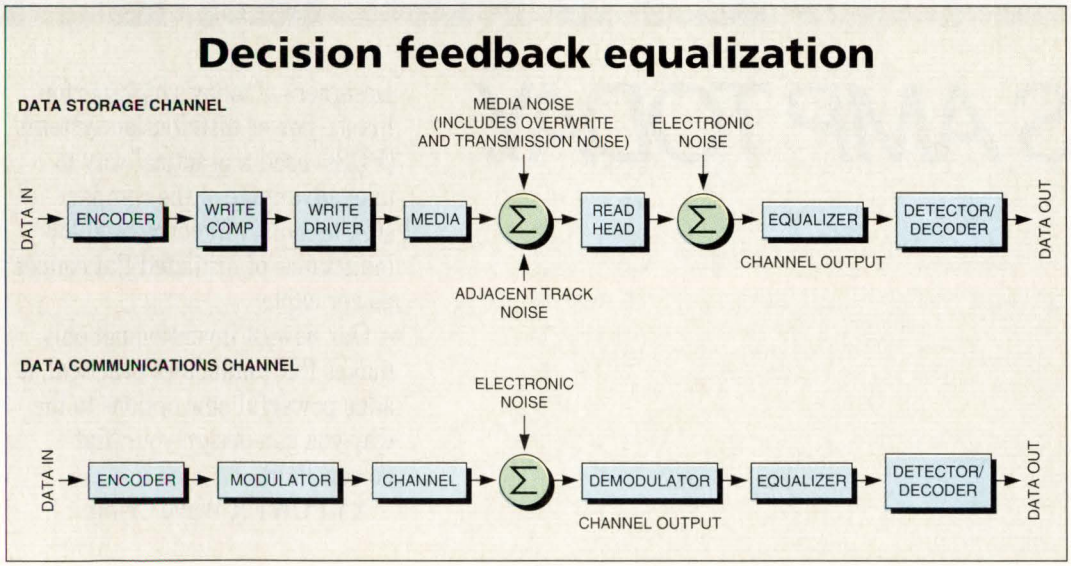
A major worry, according to Wong, is the amount of noise that shows up in the video image. "In video, there's a need to worry about glitch energy," he explains. There are hybrid 10-bit A-D converters capable of producing 20 Msamples/s, using current-weighted switches which produce video noise. A smoother scheme for weighting bits is required.

For applications with more modest frequency requirements, even the TMS320 is getting good support. "The general trend is to go digital as soon as possible," says Steve Brightman, a marketing branch manager for new products in the Linear Products Group at Texas Instruments (Dallas, TX). Consequently, much analog expertise has gone into developing analog interface circuits (AICs) for the TMS320 family. Devices like the TLC32046/47/48 include multiplexers, filters, A-D converters, serial data ports, D-A converters, output multiplexers, filters, and differential output amplifiers; they also provide (sinx)/x correction. The converters on these parts offer a 14-bit dynamic range (16 bits with programmable gain), 10-bit linearity and 8-, 9.6- or 19.2-kHz sampling rates. They are $10 parts, what Brightman calls "DSP peripherals," and are good for speech recognition and storage systems, data modem applications and some biomedical instrumentation applications.

Even TI's operational amplifiers, says Brightman, are now tweaked for DSP applications. The TLE027 and TLE037 series, for example, are otherwise industry-standard precision op amps (OP-27/37), which are manufactured with TI's Excalibur bipolar process to provide exceptionally low input offsets for the needs of precision DSP. (For the analog experts, these parts have 25-μV offsets, with 2.5 nV/√Hz noise, and a unity-gain bandwidth of 15 MHz.) "There's no point in processing 16-bit numbers," says Brightman, "if you don't have the analog accuracy up front."

New algorithms for analog

After data converters, new algorithms will help spread DSP tech-



These flow diagrams highlight the similarities between modem communications data encoding techniques and the all-digital disk drive read channel developed using those techniques. Both depend on decision feedback equalization (DEF), which promises to increase bit density by up to 50 percent.

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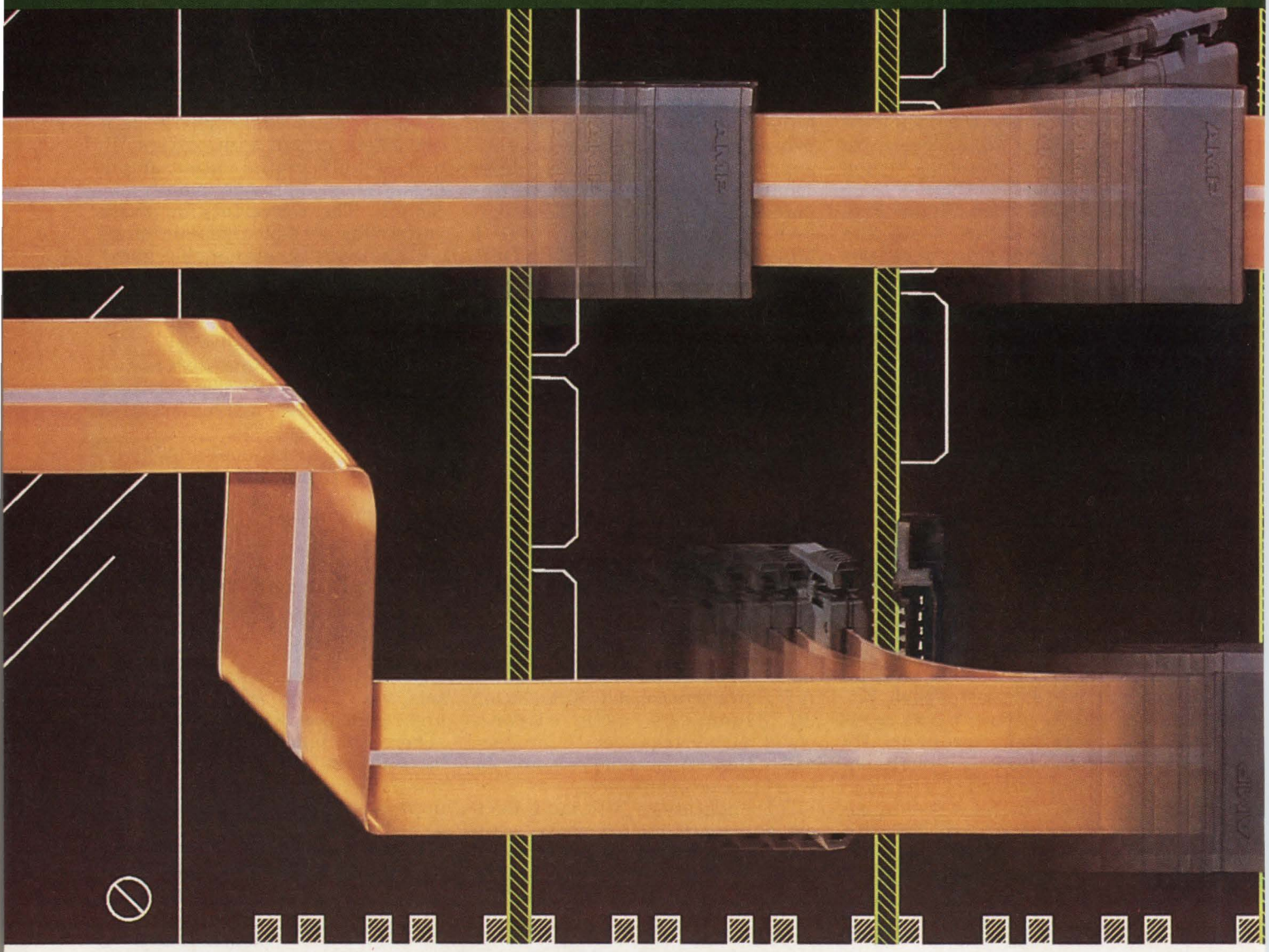

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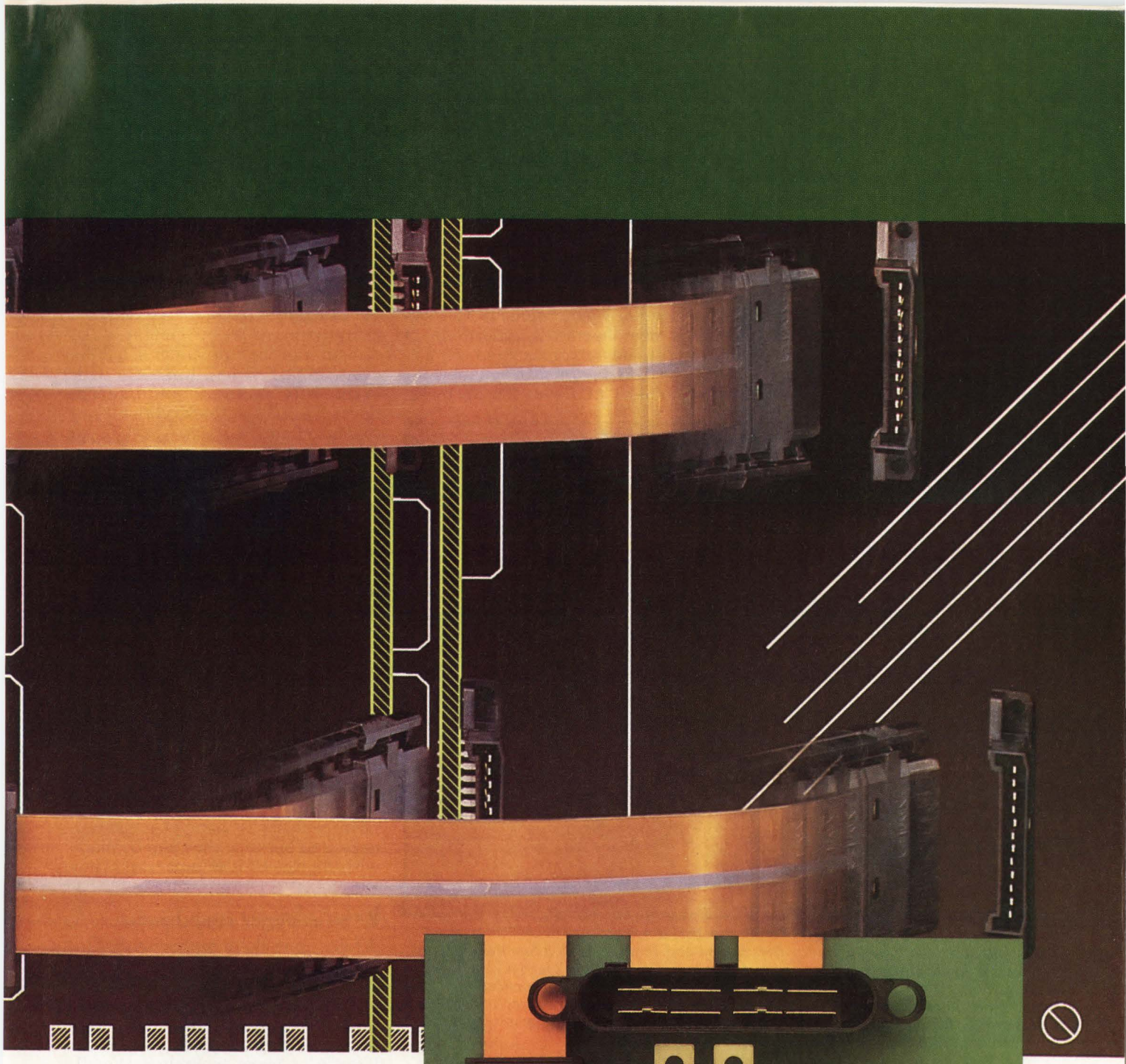

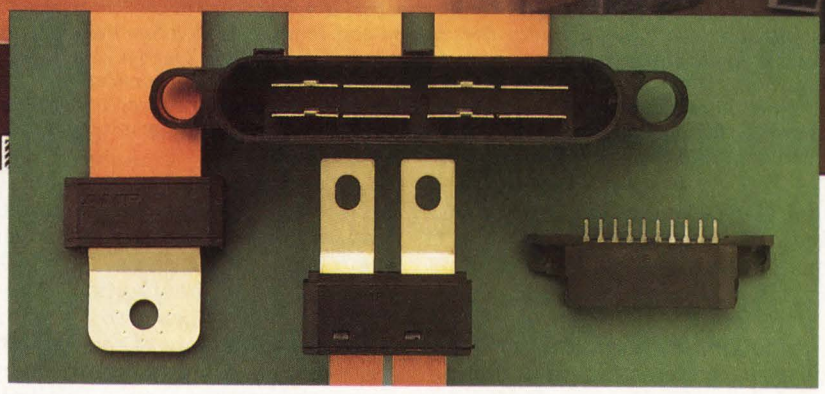

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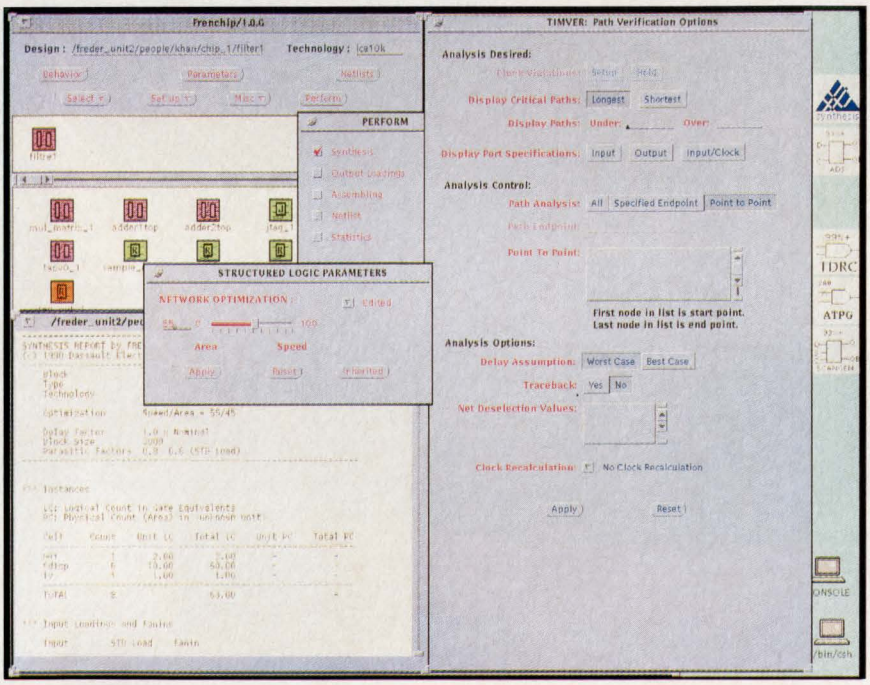
niques. The development of new algorithms is part of the movement to replace analog elements in the signal processing chain with digital elements. In some cases, it represents an effort to replace precision analog components with easier-to-manufacture digital components. In other cases, it represents an entirely different approach to system-level problems. Cellular telephones are one application, for example, where the pressure to integrate electronics into an ever-smaller number of chips



One of the factors that makes DSP more practical is easy-to-use design tools. New systems such as Mentor Graphics' DSP Station and Teradyne's MultiSim Architect not only provide user-friendly development software, but they also make it easy to synthesize new chips or partition programmable logic devices for DSP applications. Shown is Teradyne's MultiSim Architect, which offers specialized capabilities for DSP designs, including DSP synthesis, static timing verification and test synthesis. On the screen is a finite impulse response (FIR) filter.

is forcing designers to come up with digital solutions to the problems of voice encoding, transmission and radio signal manipulation.

Perhaps the best example of this is the sigma-delta conversion technology perfected by IC manufacturers such as Crystal Semiconductor (Austin, TX), Motorola (Austin, TX) and Philips/Signetics (Sunnyvale, CA). The well-publicized job of the sigma-delta converter is digital audio conversion—translating a 16-bit serial data stream into a complex audio waveform. Here, digital signal processing techniques are applied to an analog function. The result is a 16-, 18- or 20-bit part that is easier to manufacture than strictly audio playback converters, and one, many enthusiasts would argue, that offers greater fidelity.

The key to sigma-delta technology is strenuous oversampling. Ordinarily, you need to sample a 20-kHz audio signal at 40 kHz or more—at least twice the fundamental frequency—just to avoid aliasing, the interference generated by the signal's own harmonic reflections. If you grossly oversampled at 256 times the Nyquist frequency for audio (44.1 kHz)—in the 11- to 12-MHz range, for example—you would find two predictable things happening to your audio signal. First, the distribution of quantization noise—the glitches imposed by the bit-weighting elements of the A-D converter itself—would be in the higher frequency ranges beyond the limits of human hearing. Second, the stream of serial bits produced would show very little difference in amplitude from one bit to the next.

Sigma-delta technology effectively trades a resolution in amplitude for a resolution in timing. It captures information in an exceedingly narrow time slice, and only determines if the amplitude of the signal is rising or falling relative to preceding slices—information that can be represented with one highly directional bit.

For this reason, sigma-delta converters for digital audio playback, dubbed "bitstream" by Philips, are called "one-bit" by stereo equipment manufacturers such as Matsushita. Using DSP techniques such as linear interpolation and digital noise generation, bitstream converters transform a 16-bit serial data stream into the equivalent of a 256× oversampled signal, complete with artificially induced quantization noise. Each bit in the stream is then converted to a voltage—part of an analog waveform—by a switched-capacitor summing amplifier.

This may seem like an unnecessary amount of work, in terms of processor clock cycles, compared with traditional data conversion methods, which simply put the 16-bit digital audio word into a summing network made up of laser-trimmed thin-film resistors. But for 16 bits, the thin-film resistor ladder needs to have a ratiometric accuracy of 0.0015259 percent, and, though manufacturers like Analog Devices and Burr-Brown have automated the laser-trimming processes, converters such as these are not easy to make. The sigma-delta playback converters are far more accurate than converters using resistor ladders, and because they can be made with digital CMOS processes, they are easier to manufacture.

The all-digital read channel

While sigma-delta represents an application of digital technology to solve an analog signal conditioning problem, there are other applications in which DSP provides a new way of looking at system-level problems. A primary example is the all-digital hard disk read channel. This will not only contribute to the development of single-chip read channels for small-form disk drives (2.5-, 1.8-in. or smaller), but it will also increase the bit density of a disk by as much as 50 percent. Dr. Roger Hoyt, manager of fundamentals of storage channels and devices at IBM's Almaden Research Center in San Jose, CA—where one form of digital encoding, PRML (partial-response/maximum likelihood), was developed—believes that the all-digital read channel is still five years away

Though entrusted with the encoding and storage of serial data, current-generation disk drive read channel electronics is primarily

The high-frequency challenge

Manufacturers of analog and mixed-signal ICs are facing three challenges in the realm of signal processing. First, signal processing, like digital logic, is requiring ever higher levels of IC integration. Second, with so much attention focused on video and wireless communications, there's increasing need for high-frequency signal processing. Third, there's a tendency, even at elevated frequencies, to replace analog signal processing chains with digital circuits.

These challenges are particularly stressful for broadbased semiconductor manufacturers—especially logic and memory makers—who, because of competitive pressures, have found themselves shipping ever higher volumes of product with ever narrower profit margins. While the market for signal processing ICs is less volatile in terms of price and provides more opportunities for product differentiation, there's been a proliferation of relatively low-cost devices—op amps, for example—optimized for one characteristic over another, but with only subtle differences between them.

New technologies needed

Manufacturers must develop new technologies to stay on the leading edge. For the integration of analog and digital signal processing elements for operation at high speeds poses severe technical difficulties for even the most talented analog IC manufacturers.

Integration levels for analog signal processing, as well as speeds, have been moving up slowly. But unlike digital logic, which seems to gain speed with increased packing density, analog performance is often compromised with higher levels of integration. Op amps have been used for many years in dc and low-frequency applications such as instrumentation and audio. The upper bandwidth for simple ac-coupled video amplifiers has been 50 MHz until recently. Technological advances over the past few years have led to op amps with bandwidths of up to 100 MHz. While these devices are currently used for video, radar and automatic test equipment signal processing applications, devices with nearly 1 GHz of bandwidth are being released at the present time. Even with these advances, the leading edge in performance for ultrafast amplifiers is still attained only by those with analog design expertise in discrete transistor-based circuits. As with lower frequency applications, it is usually desirable to replace even the fastest discrete-based circuits with highly integrated ICs. ATE pin drivers, for example, need to conserve board real estate in 256-pin testers. Additional integration goals include reduced cost, higher reliability and, ideally, increased performance. It's no longer sufficient to simply put a single op amp on a chip. Devices such as switched input video amplifiers, which combine a four-input video multiplexer with a 50-MHz video op amp, set the expectation for future integration levels.

The highest levels of integration, however, require processes with different characteristics to be integrated onto the same die. Integrating digital signal processing on the same chip with data converters requires that IC designers combine analog bipolar, analog CMOS and digital CMOS process technologies. This is only beginning to happen today, but further developments are required before we see the long-awaited "mixed-signal system on a chip."

With the continued drive toward smaller, lighter, more reliable, and less costly systems–handheld portables, for example—there's increased use of signal processing ASICs. It's also becoming more apparent that general-purpose ICs are giving way to more specialized application-specific standard products (ASSPs). These standard catalog products can be modified quickly and economically for specific customer needs. For these reasons, there's renewed interest in analog arrays, and, in addition to new entrants in the field, major manufacturers who have shifted their focus to digital data processing are coming back to signal processing.

Replacing analog with digital

Within the signal processing arena there is a pervasive trend toward replacing analog with digital signal processing. This trend can easily be seen in cellular and wireless communications systems. A communications system typically processes signals with widely varying frequency content. The radio frequency signal is received and amplified and then mixed down to an intermediate frequency signal. Filtering and demodulation of the IF signal results in baseband signals, which may be as high as video or radar frequencies or as low as audio. These baseband signals are processed, then remodulated, up-converted and transmitted as RF.

The replacement of analog with digital in this application began in the late 1970s with the advent of microprocessors specifically optimized for DSP. These early DSPs were capable of performing some of the low-frequency processing previously done in an analog fashion. Starting in the late 1980s and into the 1990s, the DSP is finally starting to encroach upon the long-held analog monopoly on high-speed, real-time signal processing. High-speed, dedicated-function ICs made of DSP building blocks are now displacing analog in the baseband video processing and IF processing—filtering and modulation/demodulation—sections of the system. These function-specific DSP ICs perform at much higher speeds than software-driven DSP microprocessors, because, essentially, they don't require software. Such devices are hard-wired algorithms in silicon, configurable through register or pin programming. They require no additional instructions nor is there any data-fetch delay time.

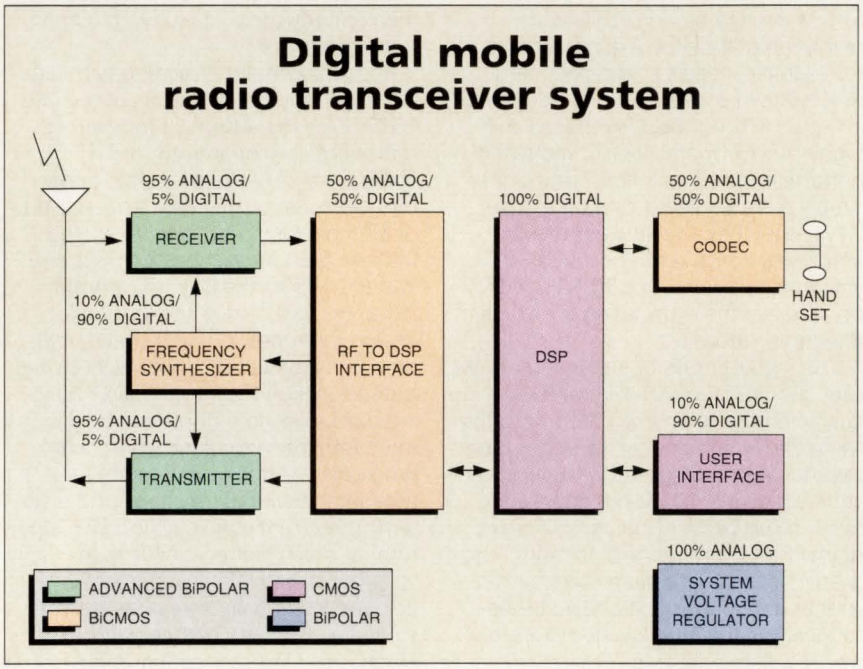
Advances provide opportunities

One might think that this encroachment of digital into the realm of analog would shrink the total slots for analog ICs. But advancements in analog IC technology provide the opportunity for IC makers to improve upon designs once implemented exclusively with high-frequency transistors and other discrete components. Discrete IF and RF amplifier designs are already giving way to silicon monolithic microwave integrated circuits (MMICs). Discrete diode-based mixers are being replaced by IC Gilbert cell-based mixers.

These advances in technology create new opportunities on many fronts—and system developers and, ultimately, end-users are the beneficiaries.

Brian Mathews, strategic planning manager, Harris Semiconductor, Melbourne, FL

analog. This is because an analog sine wave rather than a digital pulse stream is more effective in charging and discharging the coils of the write head, and ultimately in planting a magnetic spot on the thin-film surface of the disk. The bitstream going onto the surface of the disk, consequently, is a frequency-shifted sine wave. In principle, disk data density can be increased by simply increasing the serial data transfer rate, and disk drive manufacturers have moved from 5- to 10- to 15- to 24- to 30- and 36-Mbit/s data rates with corresponding increases in disk data density. But with high data rates, intersymbol interference becomes a problem—that is, it becomes increasingly difficult to distinguish one sinusoidal data bit from another in a closely-spaced pulse stream.



Cellular phone systems are one area where there's not only a high demand for system integration but also an urgent need to perform digital signal processing. RF signals must be converted to digital form for frequency synthesis. This requires a high level of process as well as component integration, as is illustrated in this diagram of a wireless communications system.

Sensitive analog filters needed

Currently, analog read channels all use some form of peak detection, in which the sine wave representing the recorded data signal is rectified (or changed to dc pulses) and put through some sort of threshold detector. In effect, the amplitude of the sine wave is used to mark the bit patterns. On playback, the read channel must not only capture and decode closely-spaced serial data patterns, but it must also distinguish these from trackinginformation—analogservo bursts—embedded within the incoming sine waves. The key to doing this well is special analog filters, essentiallywindow filters, that are sensitized to information at particular frequencies.

Companies which specialize in filters for this application include International Microelectronic Products (IMP—San Jose, CA), GEC Plessey Semiconductors (Scotts Valley, CA) and Silicon Systems, Inc. (Tustin, CA). New entrants include AT&T Microelectronics (Allentown, PA) and Micro Linear (San Jose, CA). Micro Linear's ML6006 read channel filter/equalizer, for example, consists of a 6th-order Bessel low-pass and a 2nd-order cosine equalizer implemented as a continuous-time filter with a transconductor and integrator. It's a $6 part which provides filtering and pulse slimming for data rates up to 36 Mbits/s.

There are many, such as Phil Welsh, strategic marketing manager at GEC Plessey, or Rich Nesin, manager for strategic marketing for mass storage at AT&T, who believe that disk drive read channel electronics must necessarily be analog. Welsh says that only analog will provide the performance necessary to pick servo bursts out of a 36-Mbit/s data stream, while Nesin believes DSP filtering in the data channel is overkill. DSP may be useful for controlling the head positioning servo, Nesin acknowledges, but he believes it will require more instructions and memory in that application than a general-purpose microcontroller. As a consequence, AT&T's integrated disk drive servo controller, the ATT93C010, is based on the 8030 microcontroller architecture.

The new digital approaches to data recording and reading replace peak detection methods with sampling detection, in which the entire sine wave, and not just its peak, is sampled by a high-speed A-D converter. This lets the read channel make assessments according to the phase and shape of the wave as well as its amplitude.

The IBM Almaden development, PRML, is an encoding technique that increases the density of data pulses by shaping to a particular polynomial—quite similar to what a V.32 modem does when it puts a 9.6-kbit/s data stream onto a voice line with a 3-kHz bandwidth. Projections suggest PRML will increase disk density 1.5 to 4 times, but actual experiments with 120-Mbit/s data transfers—four times the current rate—indicate it won't work without some specialized equalization or frequency control.

Decision feedback equalization (DFE) is an adaptive mechanism developed at Stanford University by associate professor of electrical engineering John M. Cioffi, who was earlier at the IBM Almaden Research Center. The project was funded by disk drive makers IBM, Maxtor and Quantum. Some early funding also came from Digital Equipment Corporation and the State of California, though these backers are less visible now.

DFE outpaces PRLM

"DFE goes one step further than PRML," says Professor Cioffi. It increases the number of bits per second available over a spectrally continuous region. "It doesn't shape or slim the pulse," he says, "but it plays with the phase, making the pulse energy look 'one-sided.'" Where PRML has proved it will increase disk data density 30 percent over current encoding techniques, DFE has actually demonstrated density

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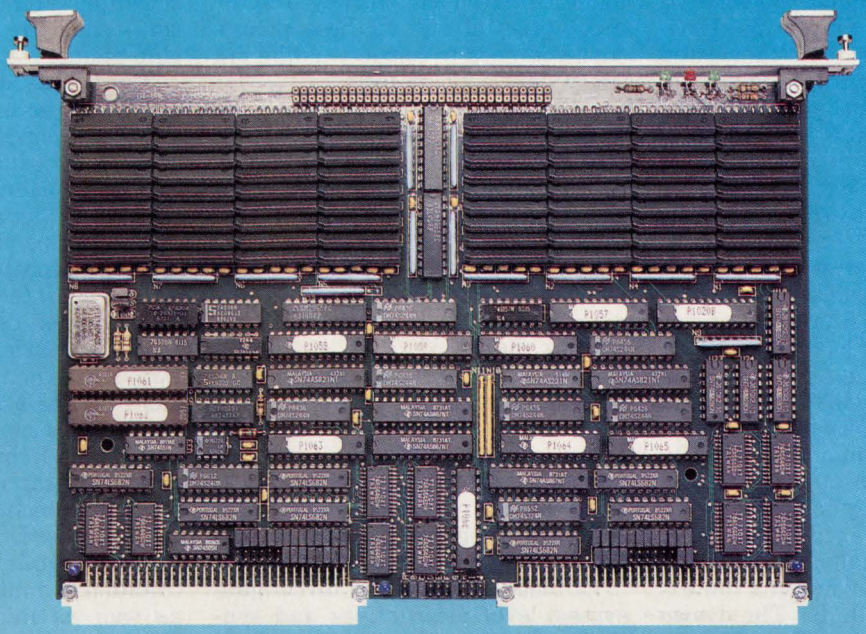

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improvements as high as 50 percent. What's more, the first chips (Revision 2, in fact) are being fabricated by Signetics. As with sigma-delta, Philips/Signetics believes that the all-digital approach will lead to higher chip reliability and better manufacturing yields.

The movement to replace analog signal processing techniques with digital ones puts pressure on programming and modeling tools. The Saber models from Analogy (Beaverton, OR), for example, contributed to development of a new encoding/decoding chip for movie theater sound systems developed by the Precision Monolithics division of Analog Devices. The Dolby Pro-Logic surround-sound decoder chip is essentially a frequency-sensitive adaptive servo loop which continually balances left-right stereo channel outputs (for example, L, R, L+R, L–R). The device contains some 30 op amps, 10 low-noise voice-controlled amplifiers, two dual-output rectifiers, two log-difference amplifiers, comparators, a new circuit element called an operational conveyor amplifier, as well as random logic and a digital noise source.

Newer Saber models for DSP which proved helpful include signal sources and noise source templates, as well as "Hyper models" for A-D and D-A functions.

The Mast modeling language within Saber, in fact, is being considered by DARPA—and especially by the Electronic Devices Lab of the U.S. Army Labcom at Ft. Monmouth, NJ—as a possible model for an analog hardware description language (AHDL) that will be used to define new-generation Mimic (millimeter and microwave integrated circuits) as well as low-frequency analog ICs.

DSP programming gets easier

Traditional DSP development tools are built around circuit boards with TI's TMS320, Motorola's 56000, AT&T's DSP-32C, or Analog Devices' ADSP-2100 DSPs. Spectrum Signal Processing (Burnaby, British Columbia) offers boards for each of these processors, as does Ariel (Highland Park, NJ). If you want to develop a DSP system using one of these processors, you have what could be called a "done deal." The proliferation of hardware and software subroutines should make development relatively easy—even for developers whose primary experience is analog. But, if you're looking to implement a DSP which isn't keyed to the capabilities of one of these processors, you need to consider a different set of development tools.

Comdisco Systems (Foster City, CA) is the early leader in tools for DSP algorithm development, though this position is now being challenged by other EDA tool vendors. Mentor Graphics (San Jose, CA) and Teradyne EDA (Santa Clara, CA) are both following Comdisco in introducing tools that will not only help DSP algorithm development but will also ease the transition to custom silicon.

Mentor's DSP Station is based on Interuniversity Microelectronics Center (Imec) design tools, developed at Leuvens University in Belgium with backing from Motorola, Philips/Signetics and TI. "The tools let designers investigate system-level alternatives and synthesize new parts from standard cell or FPGA device libraries," says Bob Owen, DSP marketing director at Mentor Graphics. Alternately, they can be used to develop DSP code for Motorola or TI processors.

While Teradyne's MultiSim Architect tools already provide VHDL simulation and logic synthesis, the "Frenchip" series, developed in conjunction with Dassault Electronique of Saint Cloud, France, synthesizes several DSP functions. These include a 36-MHz digital frequency synthesizer, a 10-MHz 2-D correlator and a 20-MHz Fourier transform processor—one that produces 800 MOPS.

Another option

These tools whittle away at the problem of crafting your own custom DSP processor. A real breakthrough, however, comes from Star Semiconductor, a Warren, NJ startup. Star's Sproclab couples easy-to-use programming tools with a specially architected DSP processor. The Sprochip is similar to the Motorola 56000,a 24-bit fixed-point processor, but is more specifically geared toward stream processing applications. "The problem with conventional DSPs," says Star founder Jeff Robinson, "is that they are typically conventional microprocessors—event schedulers—forced to process (often with a good deal of math) analog data whose frequency doesn't correspond to any particular schedule." The Star solution effectively solves this problem by partitioning the DSP into two architectural elements—the microprocessor scheduler and the signal coprocessor—which are married through on-chip memory.

The beauty of the system is that DSP code becomes much easier to write and compile because it's segregated from what Robinson calls the "decision-oriented portion of the CPU." The signal processing portion, in fact, can be programmed with PC-based graphical tools which automatically generate and download code. The Sproclab development system—the code development tools and the Sprochip—then become the equivalent of PLDs for analog and DSP applications, inexpensive and easy-to-implement. Robinson sees the optimization of graphical tools with dedicated architectures as the dominant trend line for DSP development—one that will certainly popularize DSP for traditional analog system designers as well as microprocessor system developers (see "The evolution of DSP development tools," p 97).

Cellular telephone, wireless networks and other forms of RF communications are the newest frontiers for DSP. Simple DSP operations include voice coding, echo-canceling and RF modulation. But more complex DSP operations are now required to cope with the increased crowding of the RF spectrum in the United States and Europe. Traditional speech coding mustn't just convert microphone inputs into digital form, it must also compress speech so that it takes up little space on a digital transmission network.

One second of speech is ordinarily 64 kbits, though frequency-sensitive linear predictive coding (LPC) compresses this to 13 kbits for use with the European Group Speciale Mobile (GSM) standard. GSM is a near-term digital standard for cramming multiple voice channels in the same space needed for one analog channel. Introduced in 1991 and expected to be commonplace during the mid-1990s, it's supported by European phone and cellular suppliers Alcatel, Centre National d'Etude des Telecommunications (CNET—France's equivalent of Bellcore), Italtel, and Philips TRT.

Standards coming soon

American digital standards will appear this year and in 1993. The US Digital Cellular (USDC) specification uses a speech coding technique called vector sum excited linear (VSELP) coding, developed by Motorola. VSELP successfully com-

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The evolution of DSP development tools

The transition from analog to digital signal processing is occurring at a rate that threatens even the most experienced designer with competitive obsolescence. As a consequence, one of the major challenges and business opportunities of the 1990s is bringing complex and specialized technologies such as DSP to market in a form that system designers can use with a minimum of training and preparation.

DSP is more precise, robust and flexible than analog. It also opens up a whole new world of applications that couldn't be addressed with older technologies. Current examples include adaptive systems of various sorts, patient monitors, V.32 modems, speech recognition systems, and video compression systems. But sadly, the tools that would let you take advantage of all these benefits are lacking. The challenge for tool system developers is to take the industry's collective wealth of DSP know-how and put it in the form of easy-to-use tools. These tools should let designers integrate DSP systems into their end products in a timely fashion, without having to become experts in DSP theory, but also without compromising the efficiency of the implementation.

OOP addresses the challenge

The software development world is currently attempting to address this challenge by rapidly integrating new algorithms with techniques such as object-oriented programming (OOP). OOP is an attempt to contain and present knowledge in a manner that readily lends itself to a hierarchical structure and top-level thinking. The data, the activity you perform on it and the form in which the results appear are all separate concepts or objects. If you want to plot a graph on the screen, for example, you send a message "plot to screen" to your data, and the plot appears. In principle, there's no need to worry about the low-level details of how the plot was created.

For the traditional computing world, the transition to OOP techniques involves trade-offs between the difficult learning curves associated with higher-level languages such as C++ and the sometimes reduced efficiency of the resultant OOP code. It's reminiscent of the transition in the microprocessor world from assembler to C in the late 1970s and early 1980s.

Microprocessor evolution

Today, the signal processing world is retracing the evolution of microprocessor development tools. The vast majority of current DSP chips is still coded in assembler. But coding real-time systems is much more complex than coding non-real-time systems. Even though higher-level approaches have been tried, mainly by utilizing graphical front ends, true higher-level tools have been very slow in coming. The tools that now exist to aid in DSP coding are principally limited to the C language.

Graphical front ends of various sorts for signal processing simulators have existed since at least the 1960s. Ones that generate code for processors are much more recent. Massachusetts Institute of Technology was working on such a system in the late 1970s. The University of California at Berkeley picked up the baton in the mid-1980s, first with Gabriel and now with Ptolemy. Commercially, companies such as Comdisco have been selling a graphical approach to simulation since the mid-1980s, and now they're producing extensions for code generation.

If graphical front ends have been around for so long, why are designers still primarily using assembly coding techniques? The answer is twofold. First, the resultant solutions are mainly constrained to signal-processing-only applications. They don't provide for the incorporation of state machines or similar controlling techniques or for interfacing to such systems. Second, the code produced by these graphical systems is often very inefficient in comparison to hand-coded solutions.

The principal limitation of these graphical front ends has little to do with software and everything to do with the hardware architectures they're forced to target. In fact, there's a growing number of engineers and vendors who've become convinced that translation from such a high-level description to an efficient implementation requires more than a purely software solution on top of existing architectures. What's required is an entirely new overall architectural approach to both hardware and software that addresses the real killer in creating real-time code—an efficient and robust event scheduler.

Decision processing

It's difficult or almost impossible to create a robust and efficient scheduler that contains both code blocks with hard real-time constraints (signal processing) and code blocks with data-dependent execution time (decision processing). Yet this is precisely the situation that every designer faces in the creation of DSP applications on the single-CPU implementations available today. However, if these two computing models can be separated and optimized independently without compromising the interaction that needs to take place between them, then the complexity of the problem is greatly reduced and efficiency greatly enhanced.

The first of these systems, in which computationally intensive but deterministic signal processing is separated from the data-dependent decision-oriented processing, are just starting to appear. It's highly likely that others will follow with similar architectural approaches. This DSP architecture is essentially a tightly coupled, two-architecture solution. By optimizing one architecture for signal processing only, the creation of a scheduler for the signal processing is straightforward, robust and efficient. The other architecture is optimized for the decision-oriented portion of the application and is most often a traditional microprocessor tightly coupled in both software and hardware to the signal processor. Code for the microprocessor is designed in the conventional interrupt-driven manner and is free of the tough real-time constraints that signal processing imposes. In this approach, the signal processor becomes more of a signal coprocessor. The architecture of the signal coprocessor is such that communication with the microprocessor is seamless, fast and efficient.

Jeff Robinson, founder, Star Semiconductor, Warren, NJ

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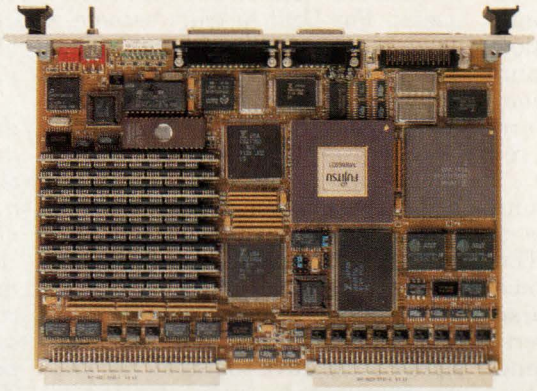

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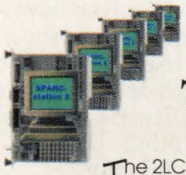
2 040 x 2 =28.5

With 28.5 Mips of integer performance, the 40 MHz SPARC MPU is more than twice as fast as the 68040. A larger 64KB cache and combined MPU/FPU put the SPARCcard 2LC in a class of its own.

64/32 64-Bit Architecture

The SPARCard is the only SPARC VME SBC built on the MBus, Sun's sophisticated 64-bit local bus. Used in the SPARCserver 600 MP Series, the MBus offers 64-bit paths to internal devices and memory for *fast* system throughput. Advanced ASICs designed specifically for the MBus guarantee performance and reliability.

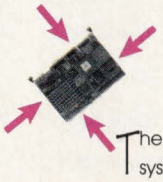


7 The Future

The 2LC is just the beginning. Themis is producing an entire family of SPARC 2-based products for every embedded application, including those requiring SBus modules. For more information contact Themis Computer, the sole source for VME SPARCstation 2 performance.

SPARC 100% Pure SunOS

We're partnered with SunSoft, a division of Sun Microsystems and developer of Solaris, Sun's newest operating system. So we guarantee full SunOS compatibility including: SunOS 4.1.1, Open Look, Open Windows, and ONC/NFS. All Sun application software and development tools run on a SPARCard without modification.



5 Fully Loaded

The SPARCard 2LC is a complete system on a card. Everything's on-board, including: 8-32 Mbytes DRAM, Ethernet, SCSI, VME interface, Open Boot PROM, Non-volatile SRAM, and two Serial Channels. Its MBus/VMEbus Controller has data FIFOs and hardware DMA for blazing VME performance.

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presses speech from 64 down to 8 kbits. The coded voice signals are used to modulate an RF carrier frequency which is multiplexed onto a common channel.

Time-division multiplexing funnels several voice conversations into an interleaved stream of digitized packets. Discontinuous transmission, meanwhile, lets phones stop transmitting during pauses in speech, thus conserving channel capability. Voice activity detection (VAD) recognizes gaps in speech and inserts "comfort noise." In addition, DSP equalization techniques are used to remove distortions from received signals.

As a cellular and communications system supplier, Motorola has a leadership position in this area. The Motorola 56100 DSPs and voice codecs (coder/decoders) are also widely used in other manufacturers' equipment. But increasing demand for cellular telephones and other portable wireless communication systems establishes a need for single-chip, high-frequency A-D converters, D-A converters, integrated RF transmitter/receiver/down-converters, and frequency synthesizers. Manufacturers ready to answer this need with high-frequency components include Harris and Plessey, as well as Analog Devices and National Semiconductor.

RF signal processing is one of the obvious areas in which digital signal processing must make the transition from the seemingly exotic to the commonplace—but reducing component price is only part of the issue. Analog components and signal processing techniques present an efficient solution to wave-shaping problems—especially at high frequencies—and will continue to be useful. For DSP to truly become a done deal, the migration from analog to digital must be simple and painless. Low-cost high-frequency A-D converters offer one possibility. New digital processing algorithms offer another.

If you're currently working with digital logic circuits, you know it's easy to transform your ideas—at any level, and at almost any price point—into custom silicon. For DSP to become commonplace, the designer must have the same capability. Fortunately, we're starting to see toolsets which not only facilitate algorithm development but also make the vital connections to real silicon—both off-the-shelf programmable components and custom signal processors. It's this 'roll your own' capability, perhaps, that will provide the best springboard for analog engineers to embrace a largely digital future. ■

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

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Postscript

For a large majority of DSP applications with sampling frequency requirements below 1 MHz, there are a great number of boards, semiconductor components and software development tools which support the processors of TI, AT&T, Motorola, and Analog Devices. However, in applications with operating frequencies above 1 MHz, analog signal processing still dominates.

Three things are required to make digital signal processing techniques and components, still relatively new, more practical than analog signal conditioners in video, image processing and RF communication applications. We need (1) faster high-resolution data converters, (2) new DSP algorithms and (3) software tools that take the pain out of algorithm and DSP code development. There are promising developments in each of these areas.

In the first case, we are struggling with a trade-off between resolution and speed. Applications that require 12-, 14- or 16-bit resolution—medical imaging, for example—can hardly find converters that are fast enough. Emerging now are single-chip 12-bit A-D converters that offer 10- and 20-Msample/s rates, but cost over $100.

One way around this problem is to develop algorithms that substitute digital finesse for analog signal conditioning techniques. Sigma-delta conversion, for example, is a technique which allows high-fidelity audio converter ICs to be manufactured with economical digital CMOS processes.

And, with the aid of easy-to-use toolsets, we'll see an upheaval in practical algorithms and code generators—even architectures—for digital signal processing.

Steve Ohr

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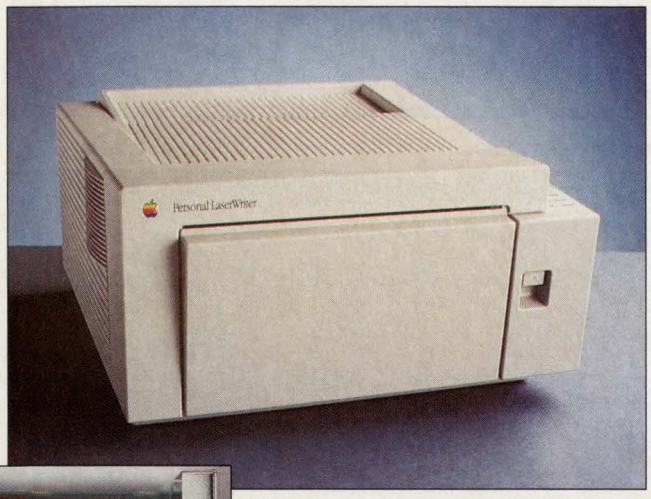
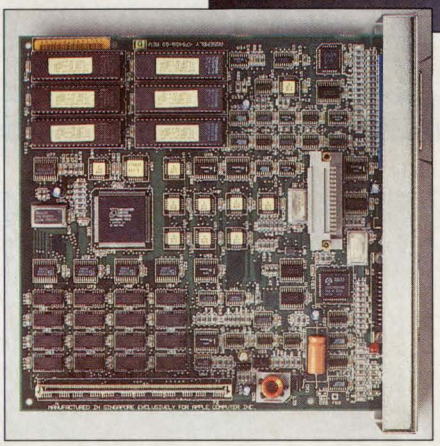
INTEGRATED CIRCUITS

RISC chips continue conquest of embedded realm

Jeffrey Child, Associate Editor





Even the 680X0 diehards at Apple Computer have been wooed away to RISC. The Apple Personal Laser Writer NTR printer uses an AM29005, one of AMD's 32-bit RISC processors for low-cost, high-volume applications (see inset).

Driven by the demands of applications ranging from LAN systems to Unix workstations, RISC processor vendors are offering devices with more and more computational muscle. Promising greater performance through pipelining, multiple execution units and more efficient code execution, RISC processors have all but taken over the high end of microprocessor-based system design. Now, setting their sights on lower-end, cost-sensitive embedded and desktop systems, RISC chip manufacturers are expanding their product lines to fit a wider range of price and performance.

RISC processors run faster thanks to simplified instructions and addressing modes. They optimize only the most basic processor operations, such as loads and stores. They offer pipelined architectures and multiple execution units to aid parallelism. RISC processors also employ large sets of registers to minimize memory accesses that slow down operations.

Running to RISC

Because RISC processors are traditionally used in Unix workstations, they're perceived by many as expensive. But as they gain design wins in lower-cost, high-volume applications, this perception is rapidly changing. Exemplifying this trend, even such 680X0 diehards as the designers at Apple Computer (Cupertino, CA) have switched to RISC and selected the Am29005, one of AMD's 32-bit RISC processors, to power their entry-level Personal Laser Writer NTR printer. Illustrating the viability of RISC, even for cost-sensitive applications, the printer sells for only $2,100, yet prints documents up to six times faster than Apple's earlier 68000-based laser printer.

As the accompanying chart shows, at one end of the spectrum are high-end devices that reside mostly in Unix workstations. These chips feature superscalar architectures and high-performance floating-point processing. At the other extreme are the so-called embedded RISC chips that boast impressive performance at a variety of price points. Also under the RISC umbrella are processors appropriate for both desktop and embedded applications. For the purpose of comparison, the chart also includes a few chips that are proprietary, such as Hewlett-Packard's PA-RISC processors.

While the performance and capabilities of the available RISC processors vary, many of them share the same basic architecture. It's interesting that RISC vendors don't wage the kind of architectural battles that were common in the CISC realm—for example, the segmented 80X86 versus the flat 680X0 debate. "A lot of the RISC architectures are very similar. The i960 actually looks like a superset of the MIPS architecture," remarks Alan Steinberg, marketing director for the i960 at Intel (Santa Clara, CA). "These newer architectures are all pulled out of the same architectural basket—large register sets, load/store architectures, simple instruction set." In the RISC arena, Intel offers nine variations of its i960 architecture. They range from high-end parts, such as the $1,500 i960MX, sporting a superscalar CPU, FPU and MMU, to the i960SA at the low end, an under-$50 part with 32-bit core only.

An easy RISC

One reason some designers of embedded systems have shied away from RISC is because it's seen as a relatively expensive architecture that's difficult to design with. For less than $50, designers can instead use a 68000 with a gate array, for example. Advanced Micro Devices (Austin, TX) addresses such concerns with its latest RISC offering, the Am29200. In volume, the 29200 sells for less than $40. It combines a 29000 CPU core with a complete subsystem of peripherals built around it, including a DMA controller, a DRAM or ROM controller, 2-channel DMA, serial port, parallel port, timer, autohandling capabilities, chip selects, and wait-state

Model	Clock rate (MHz)	External bus width (bits) (addr,data,instr)	Number of registers	Instruction Cache (bytes)	Data cache (bytes)	On-chip FPU (bytes)(Yes/No)	On-chip MMU (Yes/No)	Performance (VAX MIPS, MFlops)	Price	Comments
Advanced Micro Devices 5204 East Ben White Blvd, M/S 561, Austin, TX 78741 (800) 292-9263										**Circle 301**
Am29005	16	32/32	192	—	—	N	N	10 VAX Mips	$37	Binary compatible with all 29k-family processors
Am29000	16, 20, 25, 33	32/32	192	256	—	N	Y	22 VAX Mips at 33 MHz	$47	Same as above
Am29030	20, 25, 33	32/32	192	8k	—	N	Y	20 VAX Mips at 33 MHz	$79	Same as above
Am29035	16	32/8, 32/16, 32/32	192	4k	—	N	Y	10 VAX Mips at 16 MHz	$38	Same as above
Am29050	20, 25, 33, 40	32/32/32	192	512	—	Y	Y	27 VAX Mips at 40 MHz, 80-MFlops peak	$145	Same as above, separate instruction data bus
Am29200	16.667	32 8/16/32 8/16/32	192	—	—	N	N	8 VAX Mips	$37	Microcontroller based on 29k core
Cypress Semiconductor 3901 N First St, San Jose, CA 95134 (408) 943-2600										**Circle 302**
CY7C601	40	64/64/64 multiplexed	136	—	—	N	N	24 VAX Mips, 7-MFlops SP	$235	604 & 605 support chips allow multiprocessing
CYM6001K Sparcore CPU	40	64/64/64 multiplexed	136	64k to 256k	64k to 256k	Y	Y	32 VAX Mips, 7-MFlops SP	$1,450	Module (single)
CYM6002K Sparcore CPU	40	64/64/64 multiplexed	136(x2)	64k to 256k	64k to 256k	Y	Y	50 VAX Mips, 13-MFlops SP	$3,200	Module (dual)
CYM6003K Sparcore multiprocessor	40	64/64/64 multiplexed	136	64k to 256k	64k to 256k	Y	Y	32 VAX Mips, 7-MFlops SP	$1,675	Module
Digital Equipment Corporation 77 Reed Rd, Hudson, MA 01748 (800) 332-2717										**Circle 303**
DEC-21064	150	34/64 34/128	64	8k	8k	Y	Y	300-Mips peak, 150-MFlops peak	$1,650	Available in July, sampling now, 64-bit Alpha architecture, 3V
FRISC, a Micron Technology subsidiary 2805 E Columbia Rd, Boise, ID 83706-9698 (208) 368-4400										**Circle 304**
FRISC	50	64	64	—	—	Y	N	50-MFlops DP, 100-MFlops SP	—	Direct support for 32-way bank DRAM interweave memory; 8 instruction buffers
Fujitsu Microelectronics 77 Rio Robles, San Jose, CA 95134-1807 (408)456-1160										**Circle 305**
IU/FPU, MB86903	33,40	32/32	136	—	—	Y	Y	29 Mips, 5 MFlops	$199	—
Sparclite, MB8693X	20, 30, 40	32/32	136	2k to 8k	2k	N	Y	37 Mips	$50	—
Hewlett-Packard 3000 Hanover St, Palo Alto, CA 94304 (415) 857-1501										**Circle 306**
PA 7100	100	64/64	64x32 FP, 32 IP	8k to 1M	8k to 2M	Y	Y	120 Specmarks	Proprietary	Two-way superscalar
PCX-S	66	64/64	96, 32 IP	8k to 1M	8k to 2M	N	Y	76.7 Mips, 23 MFlops, 77.5 Specmarks	Proprietary	Two-chip set

Key: DP = double precision, SP = single precision

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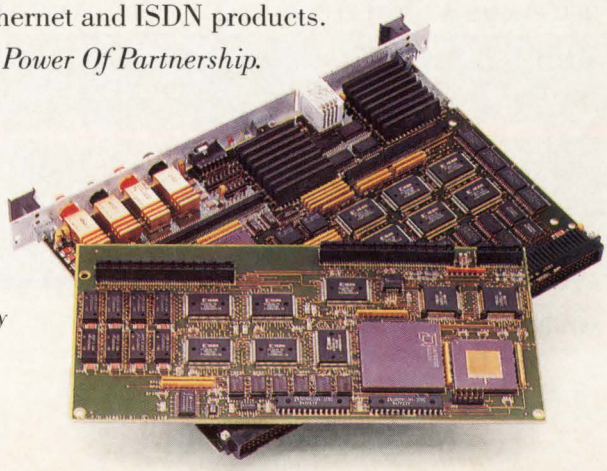

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Model	Clock rate (MHz)	External bus width (bits) (addr,data,instr)	Number of registers	Instruction Cache (bytes)	Data cache (bytes)	On-chip FPU (bytes)(Yes/No)	On-chip MMU (Yes/No)	Performance (VAX MIPS, MFlops)	Price	Comments
Integrated Device Technology 3236 Scott Blvd, Santa Clara, CA 95054 (408)727-6116										**Circle 307**
IDT79R3051/52	20, 40	32/32	32	4k to 8k	2k	N	Y	16-35 VAX Mips	$30	—
IDT79R3081	20, 40	32/32	48	16k	4k	Y	Y	16-35 VAX Mips	$98	—
IDT79R4000 PC/SC/MC	50	64/64	64	8k	8k	Y	Y	38-60 VAX Mips	$940-$1,240	—
Intel 5000 W Chandler Blvd, Chandler, AZ 85226 (800) 548-4725										**Circle 308**
i960SA/SB	10, 20	32/16	40	512	—	Y	N	16 VAX Mips at 16-MHz	$17.45-$27.15	Built-in interrupt controller, software compatible with i960KA/KB/CA, FPU on SB only
i960KA/KB	10, 16, 20, 25	32/32	40	512	—	Y	N	25 Mips at 25-MHz	$20.90-$50.25	Built-in interrupt controller, FPU on KB only
i960CA	16, 25, 33	32/32	50	1k	—	—	—	66 Mips at 33-MHz	$64.85-$104	Built-in interrupt controller, DMA
i960MC/XA	16, 20, 25	32/32	36	512	—	Y	Y	9.4 VAX Mips	$995	Mil-qualified/B Avionics grade
i960MM/MX	25	32/32	36	2k	2k	Y	Y	25 VAX Mips	$1,738	Superscalar military processor
i860	25, 33	32/64	32	4k	8k	Y	Y	41.5 Dhrystone	$1,429	—
LSI Logic 1551 McCarthy Blvd, Milpitas, CA 95035 (408) 433-8000										**Circle 309**
MIPS LR33000	25, 33, 40	32/32	32	8k	1k	N	N	35 VAX Mips at 40 MHz	$89	Built-in DRAM controller, 3 counter/timers, write buffer
MIPS LR33020	25, 33, 40	30/64	32	4k	1k	N	N	32 Vax Mips at 40 MHz	$129	BitBlt coprocessor video controller, DRAM/VRAM controller, 4 DMA channels
MIPS LR33090	25, 33, 40	32/32	32	4k	1k	Y	N	7 MFlops at 40 MHz	—	Compatible with LR33000
Sparc L64801	25	32/32	136	—	—	N	N	18.5 VAX Mips	$75.20	Pin-compatible with Fujitsu 901
Sparc L64811	40	32/32	120	—	—	N	N	2.9 VAX Mips	$104	Pin-compatible with Cypress CY7C601
Motorola, RISC Microprocessor Division 6501 William Cannon Dr W, Austin, TX 78735 (512) 891-2000										**Circle 310**
88100	16, 20, 25, 33	32/32	32	64k or 16k	64k or 16k	Y	—	14-29 Mips	$49	Multiprocessing support
88110	50	32/64	64	8k	8k	Y	Y	100+ Mips	—	Two graphics execution units on-chip
National Semiconductor 2900 Semiconductor Dr, Santa Clara, CA 95052 (408) 721-5000										**Circle 311**
NS32SF640/41	50	32/64	80	4k	1k	Y	N	100 Mips, 50 MFlops	$325	Superscalar processor
NEC Electronics 401 Ellis St, Mountain View, CA 94039 (800) 632-3531										**Circle 312**
VR3000A	25, 33, 40	32/32	32	—	—	N	Y	30-45 Specmarks	$250	MIPS processor
VR3010A	25, 33, 40	32/32	32	—	—	Y	—	30-45 Specmarks	$150	MIPS-based coprocessor
VR3600A	25, 33, 40	32/32	32	—	—	Y	Y	30-45 Specmarks	$400	MIPS processor
VR4000PC	50, 66, 75	64/64	32/32	8k to 32k	8k to 32k	Y	Y	61-91 Specmarks	$1,000	MIPS processor with primary cache
VR4000SC	50, 66, 75	64/64	32	8k to 32k	8k to 32k	Y	Y	61-91 Specmarks	$1,500	MIPS processor with secondary cache
VR4000MC	55, 66, 75	64/64	32	8k to 32k	8k to 32k	Y	Y	61-91 Specmarks	$2,000	Multiprocessor version of MIPS R4000

Key: DP = double precision, SP = single precison

68040 + '030 I/O Bus = 39 MIPS

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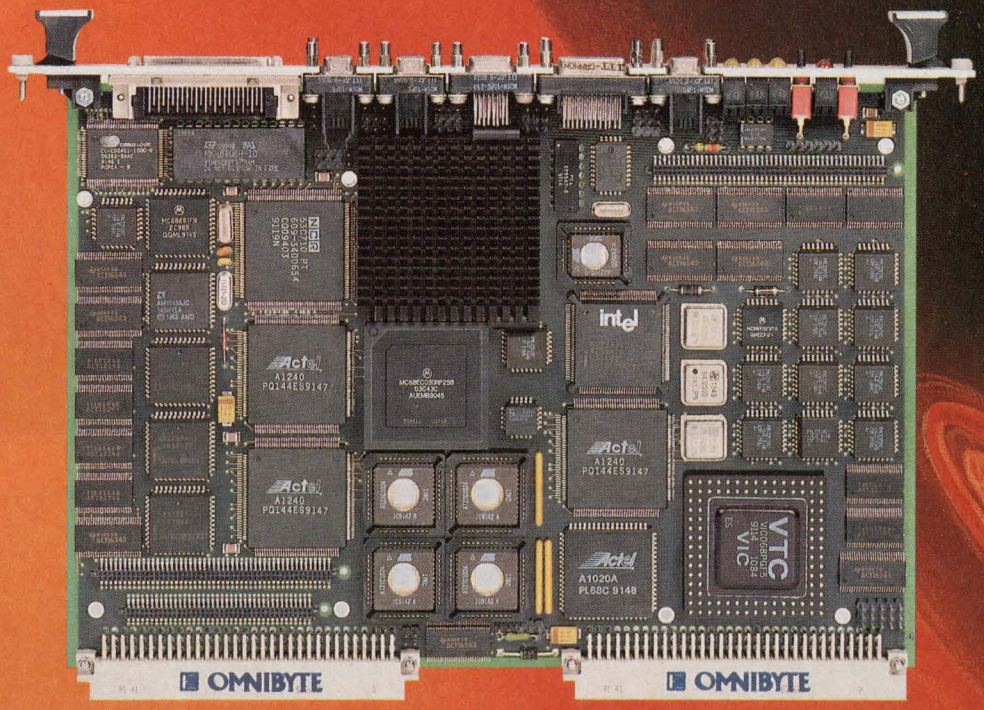

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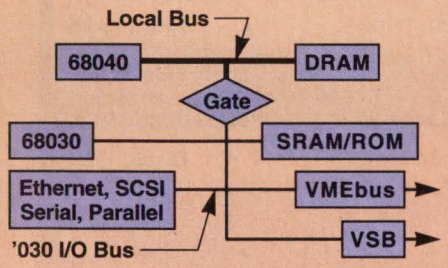

Taurus Dual Bus Architecture

The Taurus is a dual-processor, dual-bus, single slot VME board. Its dual-bus architecture allows the 68040 to execute code uninterrupted, while the '030 processes on-board I/O. This optimizes the 68040's performance. Using the '030 as an I/O processor simplifies writing your code. You only need to write high level code to the 68040. The '030 handles the device level code. You also can use the '030 as a DMA controller, while the 68040 directly controls all on-board I/O devices. The '030 uses the SRAM with the 128KB of EPROM code provided by Omnibyte.

Performance	68040: 29 MIPS, '030: 10 MIPS, VME: 50MB/sec, VSB†: 50MB/sec
Intelligent I/O	Ethernet: i82596CA†, SCSI: NCR53C710†, 4 RS232D: CD2401
Standard I/O	2 RS232D: 88C681 DUART, 32 Lines Parallel I/O, or 16 w/ Centronics Printer Port
Memory	4MB to 128MB† DRAM, 512KB SRAM†, 8KB NVRAM, 1MB FPROM†, 4MB EPROM
Other	VSB†, VME64†, Watchdog, Calendar Clock, Mailbox, (6) 16-bit Timers, Snooping, Advanced Omnimodule™ Socket
Software	VxWorks[1], OS-9[2], UNIX[3] VRTX[4], CrossCodeC, FreeForm[5] C EXECUTIVE[6], OMNIbug

† Denotes optional features.

The Taurus extensively uses intelligent, on-chip DMA devices for Ethernet, SCSI and serial I/O. This helps reduce processor intervention. Up to 2 stackable modules contain the DRAM. This allows upgradable options from 4-128MB.

Advanced Omnimodules provide additional custom I/O. You can stack Advanced Omnimodules up to 3 high. The Taurus can accept 1 memory module and 1 Advanced Omnimodule and still fit into a single slot.

To learn more contact Larry Snow:

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CIRCLE NO. 120

Model	Clock rate (MHz)	External bus width (bits) (addr,data,instr)	Number of registers	Instruction Cache (bytes)	Data cache (bytes)	On-chip FPU (bytes)(Yes/No)	On-chip MMU (Yes/No)	Performance (VAX MIPS, MFlops)	Price	Comments
Performance Semiconductor 610 E Weddell Dr, Sunnyvale, CA 94089 (408) 734-9000										**Circle 313**
PR3000A	20, 25, 33, 40	32/32	32	4k to 256k	4k to 256k	N	Y	34 VAX Mips, 11.36-MFlops SP at 40 MHz	$108	MIPS processor
PR3010A	20, 25, 33, 40	32/32	32	4k to 256k	4k to 256k	Y	N	Same as above	$89	MIPS processor
PR3020	25, 33	32/32	—	—	—	N	N	—	$12.60	MIPS processor, 4-deep write buffer
PR3100A	25, 33, 40	32/32	—	—	—	N	N	—	$64.90	MIPS processor, 8-deep write buffer, 32-deep read buffer
PR3400/3400L	25, 33, 40	32/32	64	4k to 64k	4k to 64k	Y	Y	34 VAX Mips, 11.36 MFlops SP at 40 MHz	$148-$158	MIPS processors
PR4000P/S/M	50, 60	64/64	64	8K	8k	Y	Y	42.3-2.5 Specmarks at 50 MHz	$615-$1,170	MIPS processors, 3.3V and 5V; 256k to 2M secondary instruction and data cache on PR4000S
Piper	35, 40, 45	32/32	64	4k or 8k	2k or 4k	Y	Y	22.5 Specmark at 50 MHz	$192	MIPS processor
Siemens Components, IC Division 2191 Laurelwood Rd, Santa Clara, CA 95054 (408) 980-4528										**Circle 314**
SAB-R3000A	25, 33, 40	32/32	32	—	—	N	Y	25 Specint at 33 MHz	$85	MIPS processor
SAB-R3500	25, 33, 40	32/32	32	—	—	Y	Y	25 Specmarks at 33 MHz	$170	MIPS processor
SAB-R3051/51E	20, 25, 33, 40	32/32	32	4k	2k	N	Y	16 VAX Mips at 20 MHz	$45-$50	MIPS processor, 4-deep read-write buffer
SAB-R3052/52E	20, 25, 33, 40	32/32	32	8k	2k	N	Y	35 VAX Mips at 40 MHz	$67-$75	MIPS processor, 4-deep read-write buffer
SAB-R4000 PC/SC/MC	100	64/64	48	8k	8k	Y	Y	45-70 Specmarks	$885-$1,150	MIPS processors; primary cache, secondary cache, and multiprocessor multiprocessor versions
Toshiba America Electronic Components 9775 Toledo Way, Irvine, CA 92718 (714) 455-2000										**Circle 315**
TC85R4000 PC/SC/MC	100	64/64	32	8k	8k	Y	Y	42 VAX Mips	$700-$1,130	MIPS processors; primary cache, secondary cache and multiprocessing versions
United Technologies 1575 Garden of the Gods Rd, Colorado Springs, CO 80907 (800) 645-8862										**Circle 316**
UT1750AR	16	20/16	21	—	—	N	N	800 Mips	$791	Meets rad-hardened military spec; 9600 baud UART on-chip, DMA support, 64-kword address space, Harvard architecture
UT69R000	16	20/16	21	—	—	N	N	8 Mips	$1,415	Same as above; microcontroller, 2 on-chip timers
VLSI Technology 1109 McKay Dr, San Jose, CA 95131 (408) 434-3000										**Circle 317**
ARM 60	25	32/32	31	—	—	N	N	14 VAX Mips	—	JTAG support
ARM 600	25	32/32	31	4k	4k	N	Y	14 VAX Mips	—	JTAG support, coprocessor interface, object-oriented MMU
Zilog 210 E Hacienda Ave, Campbell, CA 95008 (408) 370-8000										**Circle 318**
Z32H00 Hyperstone CPU	25	32/32	83	128	—	N	N	25 Mips	$25	64,000 mil-squared die, 40-ns cycle time, 16-bit instructions

Key: DP = double precision, SP = single precision

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CIRCLE NO. 71

logic—all in a single device. Without any glue logic, the device can interface with both DRAMs and EPROMs. All the timing, multiplexing and drivers needed for such memory devices are built into the 29200.

Besides the 29200, AMD offers five variations of its 29000 architecture, from the low-end Am29005 to the high-end Am29050. Like Intel, AMD has focused its RISC efforts on the embedded systems. But while Subodh Toprani, director of marketing at AMD, agrees that superscalar is the logical next step for RISC technology, he feels that the time isn't yet right for superscalar in embedded designs. He says, "I think the time [for superscalar] is right for workstations, but not for embedded. In the embedded systems, it's not performance at any price; it's the best performance at a given price."

The super step

According to Steinberg, the i960 architecture, unlike some other RISC architectures, was designed from the very beginning to support the parallelism necessary for superscalar processing. "We had scoreboarding and branch look ahead capability built into the architecture, as well as built-in hooks to anticipate the need for parallelism," he says. While superscalar wasn't implemented in the i960K series, the basis for it was already part of the architecture. As a result, Intel designers were able to offer superscalar capability on the i960C series without redoing the basic structure of the pipelines.

Lack of such forethought in anticipating future requirements is a likely reason, says Steinberg, why other RISC vendors have had to scramble to develop their superscalar products. "Some RISC architectures, in order to do parallel operation, now have to redo their pipelines, since those pipelines are very sensitive to position of the instruction set," he says. "You can see examples of that in the marketplace, where superscalar was not that easy to implement. I think a lot of people overlook how easy it was to do that on the i960CA."

For RISC architectures that already support parallelism, adding more performance is a relatively simple matter of adding execution units, which enhances the superscalar operation. On parts like Intel's i960MM—its military version of the 960—this approach was taken. "[For the MM] we just added another ALU to the execution string, so you get more instructions executing in parallel," says Steinberg. This is similar to the 88110, the latest RISC processor from Motorola (Austin, TX).

An extended version of the original 88100 architecture, the 88110 is code-compatible with the 88100. A superscalar design, the chip issues two instructions per clock cycle. The part also features several schemes for executing instructions, including out-of-order completion, speculative execution and dynamic reloading of loads and stores. Because the chip's pipelines are interlocked, all out-of-order execution occurs so that it's hidden from software. Now being sampled, the chip will be introduced by Motorola later this year.

"I think the time [for superscalar] is right for workstations, but not for embedded. In the embedded systems, it's not performance at any price; it's the best performance at a given price."

—Subodh Toprani, AMD

MIPS and Sparc

Among the choices for embedded control are various derivatives of popular workstation RISC architectures, including chips based on the MIPS and Sparc architectures. Among the embedded MIPS players are LSI Logic (Milpitas, CA), with its LR33000, and IDT (Santa Clara, CA), with the R3051 and R3052. The R3051 includes on-chip DMA control and read/write buffers. LR33000 integrates counter/timers, a DRAM controller, write buffers, and wait-state generators. On the Sparc side, Fujitsu (San Jose, CA) offers the MB8693X Sparclite. The Sparclite supports DRAM with some on-chip logic and features a 32-×-32-bit multiplier to boost math-intensive applications. LSI Logic offers a Sparclite which is compatible with the Fujitsu chip.

Although RISC processors have simpler instruction sets, their complex architectures can make the task of writing compilers for them quite difficult, affecting compiler availability. In some cases, the ability of RISC processors to take advantage of their full potential has been hampered because it's taken compiler technology much longer to catch up to advances in hardware. Dick Jensen, vice-president of new business development at Applied Microsystems (Redmond, WA), puts it well in defining RISC as "Relegate the important stuff to the compiler." "That's part of the problem facing software engineers [with RISC processors]: the compiler's making all these decisions for them," says Jensen. "This moves the level of abstraction away from the hardware, where it's never been before." With this in mind, designers should consider the availability of good compilers when choosing a RISC processor.

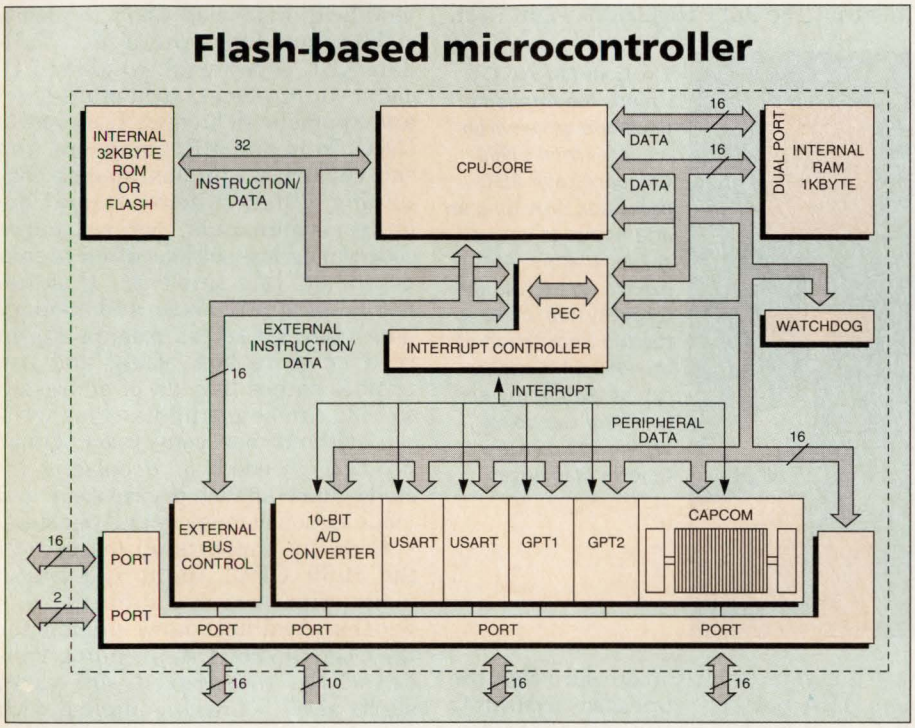
Designers at Mentec (Dublin, Ireland), a maker of i860-based Multibus II boards, have found that compilers make a significant difference in performance. "You can get over 20 percent increase in performance out of the 860 depending on what C compiler you use," says Chris Fairclough, managing director at Mentec. "A lot of C compilers don't optimize the characteristics of some of the RISC machines, like multiple execution of instructions. You can have two or three instructions executed in parallel on the 860." Fairclough, looking at the 21064, the new 64-bit RISC processor from Digital Equipment Corporation (Hudson, MA), mentions the chip's ability to have two instruction streams as a potential problem for compiler writers.

Despite the fact that the acronym RISC stands for "Reduced Instruction Set Computer," almost no designer, when asked, will cite the size of the instruction set as a good reason for switching from CISC to RISC. Unless there's a significant price/performance advantage, there's little reason to make the switch. "It's really old architectures versus new architectures," Steinberg adds. "And the new [RISC] architectures still have a lot of maturing to go through in terms of tool and environment support." ■

INTEGRATED CIRCUITS

16-bit microcontroller packed with peripherals

It might seem that there isn't much room for yet another player in the 16-bit microcontroller marketplace, but SGS-Thomson Microelectronics (Phoenix, AZ) is betting that there is. The company has recently debuted a new generation of 16-bit microcontrollers stashed with high-performance peripherals. The ST10X166 family of processors is built around a standard 16-bit core processor. Three derivatives are currently available—a ROMless version (10R166), a version with 32 kbytes of ROM (10C166) and one with 32 kbytes of flash memory (10F166).



The ST10X166 16-bit microcontroller from SGS-Thomson Microelectronics comes in three flavors: one ROMless, one with 32k of ROM and one with 32k of flash memory.

"DSP-like" features

The core of the CPU consists of a 16-bit ALU with a 4-stage instruction pipeline. SGS has complemented the microcontroller core with some "DSP-like" hardware functions, including a separate multiply and divide unit as well as a bit-mask generator and a barrel shifter. Because of these hardware provisions, most of the processor's instructions can be executed in just one clock cycle—that's 100 ns at a 20-MHz CPU clock.

For fast execution, all multiple cycle instructions have been optimized—a 32- or 16-bit division can be performed in 1 µs, a 16 × 16 multiplication takes just 0.5 µs and program branches take 200 ns. Another pipeline optimization, the "jump cache," lets you reduce the execution time of repeatedly performed jumps in a loop from 200 to 100 ns. An on-chip dual-port internal RAM of 1 kbyte provides fast access to general-purpose data registers, user data and the system stack.

For analog signal measurements, a 10-bit successive-approximation A-D converter with 10 multiplexed input channels and a sample-and-hold circuit has been integrated on-chip. Serial communication with other microcontrollers or external peripherals is provided by two serial interfaces with identical functionality. They support full-duplex asynchronous communication up to 625 kbaud and half-duplex synchronous communication up to 2.5 Mbaud.

A capture-and-compare (Capcom) unit supports the generation and control of timing sequences on up to 16 channels, with a maximum resolution of 400 ns. Typically, the unit is used to handle high-speed I/O tasks such as pulse and waveform generation, pulse-width modulation, D-A conversion, software timing, and timing of external events.

The Capcom register array contains 16 dual-purpose capture-and-compare registers, each of which may be allocated to two 16-bit timers and programmed for a capture or compare function.

A general-purpose timer (GPT) has also been included on-chip. It may be used for event cycling and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication. The GPT unit incorporates five 16-bit timers organized in two separate modules; each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

The "R" and "C" versions of the ST10X166 are priced at $25 to $35 each in quantities of 10,000. The "F" version is priced at $70 each for lots of 1,000. The chip family will be available later this year. —*Dave Wilson*

ST10X166 at a glance

- 16-bit architecture
- 20-MHz clock
- 100-ns machine cycle
- 10-bit A-D converter
- 2 serial interfaces

SGS-Thomson Microelectronics
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Circle 352

SOFTWARE & DEVELOPMENT TOOLS

i960 CA software tool fills the tool gap

Expanding on its integrated development system for the i960 CA microprocessor, Applied Microsystems (Redmond, WA) has introduced the CodeTap 960 CA, an in-circuit development tool for software engineers debugging embedded code for Intel's i960 superscalar microprocessor.

The CodeTap 960 CA rounds out Applied's development environment for Intel's i960 CA superscalar RISC processor, providing an alternative to expensive emulators. Able to run transparent to the target system at up to the full clock speed of the i960 CA, CodeTap can do everything an emulator can do except locate complex time-related errors.

There's long been a gap in the kind of tools needed in the development cycle. Problems relating to the logical flow of software are easily solved by software monitors, while emulators are primarily used for solving time-related problems at system integration. CodeTap addresses the in-between phase of solving physical problems involving the architecture and physical assignments required for the software to control the hardware.

"Codetap is an emulator with the cost taken out," says Richard Jensen, vice-president of new business development at Applied.

Like an emulator, for example, CodeTap can be substituted for the processor on a laser printer controller and can run it just as it was intended to be used in the system. "If you weren't getting, say, a laser strobe output, you could set a breakpoint right on that area of the data and find that data wasn't coming in," says Jensen. "Then you could find where in the software that data was sent to the wrong I/O port."

Unlike an emulator, CodeTap isn't able to find bugs due to timing errors. "Let's say you had a problem where the logical decision tree was based on data that's updated at a DMA port," says Jensen. "[With CodeTap] you could have made sure that the data was in the right spot, but you couldn't make sure that the DMA port was updated accurately at a time before you took that information and made a logical flow decision off of it."

Code-compatible

CodeTap 960 CA is fully compatible with Applied's existing high-performance EL 3200 emulator and uses the same powerful Validate/XEL user interface and debugging software. With Applied's system, engineers can easily move between CodeTap and an emulator without learning a new user interface or debugger. The system is supported by a comprehensive range of application engineering support and services.

CodeTap consists of a target access probe, which uses emulation technology to provide access and control for executing and debugging code; an RS-232 communications adapter, which connects to a personal computer or Sun workstation; and fully integrated debugging software.

CodeTap provides transparent code execution in the target up to the maximum clock frequency of the i960 microprocessor with no wait states. Unlike software monitors, it's nonintrusive and requires no target memory, I/O ports or interrupts. No monitor linking other code modifications is necessary to use it.

The product includes Validate/XEL, a powerful, windowed C-code source-level, assembly-level and symbolic debugger. It supports GNU, Intel and MRI compilers. You can construct complex macros containing C-like statements and debugger commands; access source code variables; set execution breakpoints on line numbers, C statements, program labels, and memory addresses; set access breakpoints on read or write bus cycles; and use symbol names instead of addresses so code can be manipulated as written without hex conversion. Other functions needed for debugging include start and stop execution and modification of memory and registers.

CodeTap supports all features of the i960 CPU, including burst mode, pipelines and different bus widths. Available now, pricing for the CodeTap 960 CA, including Validate/XEL integrated software, starts at $7,500 when bundled with Applied's total system offering. Unbundled prices are slightly higher. —*Jeff Child*

CodeTap 960 CA at a glance

- Code-compatible with Applied's EL 3200 emulator
- Runs transparent to target at up to full clock speed of i960CA
- Supports burst mode, pipelines and different bus widths of the i960CA
- Supports MRI, GNU and Intel compilers

Applied Microsystems
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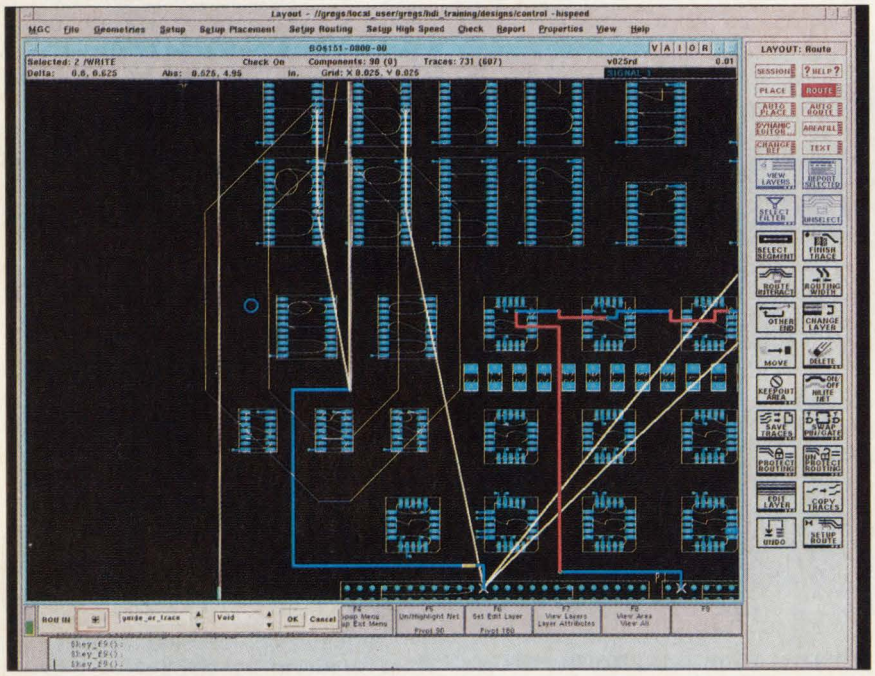
Circle 360

CAE/CAD TOOLS

Tool ports high-speed design rules to PCB layout

The latest addition to Mentor Graphics' PCB design tool suite is Board Station 500, a system for high-speed boards and multichip modules (MCMs). The tool combines timing constraint driven place-and-route algorithms and high-speed analysis capabilities to control and analyze physical effects and maintain signal integrity.

With the Board Station 500, Mentor has brought the physical rules that affect a high-speed circuit's behavior to the front end, or layout phase, of the design cycle, where they can be used to guide the correct placement of components. By incorporating topology constraints into the layout phase, for example, you can decide whether to allow stubs in the design or choose daisy chaining as the only acceptable interconnect method. When routing the same signal to multiple loads, you can implant rules that route the signal to components in a predefined order.



In this photo of the Board Station 500 design system, length requirements have been specified by the designer to guide component placement. On the left of the screen, the inside diamond shows the distance allowed to meet the minimum length requirements, while the outside diamond shows the distance allowed to avoid violating maximum length requirements.

Board Station 500 lets you specify a set of electrical rules, such as method of interconnect, topology constraints, allowable interconnect delays, and impedance characteristics. The system then automatically maps these parameters into a set of physical rules for subsequent use by high-speed automatic and interactive place-and-route algorithms. By using this approach, you can match the physical representation of the PCB with the electrical performance characteristics needed for signal integrity and circuit performance.

Controlling topology

By specifying topology as a group of names which represent a particular order of nets, a logic designer can precisely control an arbitrary, complex topology for subsequent physical layout. This method ensures that the logic designer's directions are not lost or misinterpreted during the physical design phase.

The Board Station 500 also lets you specify the allowable interconnect delays that can be assigned to a single net or group of nets to ensure clock skew minimization. The tool's impedance control feature lets you specify impedance requirements for a single net or group of nets. If you specify that a 50-Ω impedance be maintained, the tool will take this information and translate it into interconnect length and width specifications. Balanced pair routing can also be included in a design's specification, so that specific lines will be routed in parallel and adhere to matched length constraints.

Mentor has integrated a set of high-speed analysis tools from Quad Design Technology into the Board Station 500 tool. The Preroute Delay Quantifier provides placement-based interconnect delay calculation and placement evaluation. The Crosstalk Tool Kit analyzes multiconductor crosstalk noise and includes an electromagnetic field solver and a multiconductor crosstalk network simulator.

Board Station 500 is available now for $125,000. It runs on Hewlett-Packard Apollo Series 700 and Sun workstations.—*Mike Donlin*

Board Station 500 at a glance

- Design system for high-speed PCBs and MCMs
- Lets designers specify electrical rules to guide component placement and physical layout
- Principal rule categories are: net topology, minimum/maximum length control, stub length control, matched length control, layer restrictions, balanced pair routing, and shielding generation
- Available now on HP Apollo Series 700 and Sun workstations for $125,000

Mentor Graphics
8005 SW Boeckman Rd
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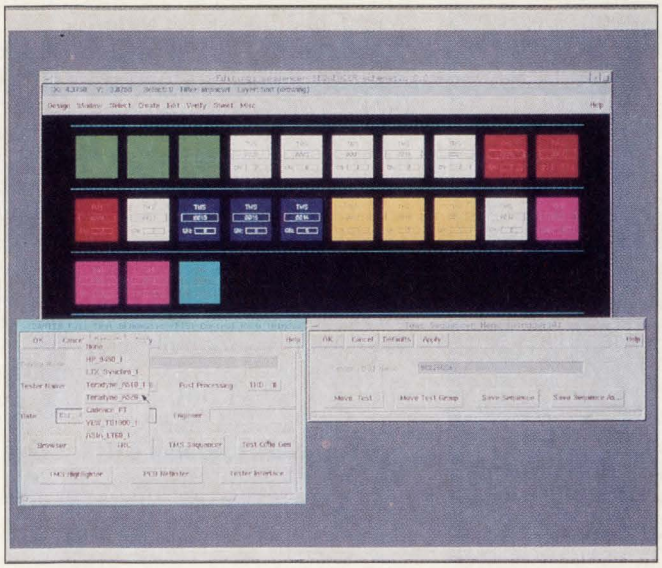
CAE/CAD TOOLS

Design-for-test suite targets analog and mixed-signal ICs

Designers and EDA vendors alike are moving the needs of test engineers to the front of the design cycle. This means altering designs for testability and providing test engineers with as much information as possible early in a product's development, so that test programs can be ready for the first prototype.

Cadence Design Systems (San Jose, CA) has unveiled Dantes, a bidirectional design-and-test environment for analog and mixed-signal ICs that addresses these needs.



In this display of the Dantes test sequencer, the test module schematics (represented by multicolored icons in the top window) are grouped together for optimum tester resource management. The lower left window shows a list of possible testers, while the lower right menu shows the operations that can be performed with the sequencer.

Joint effort

By using Dantes, design and test engineers can work on a design concurrently and pass information back and forth through Cadence's Design Framework II. Tools within Dantes are the result of a joint effort between Cadence and selected automatic test equipment (ATE) vendors—Hewlett-Packard, LTX, Teradyne, and Yokagowa—who provided ATE-specific tester modules and criteria for automating the test process. This vendor-specific test information is stored in Dantes' tester symbol library.

While symbols may be viewed as generic or tester-independent, the actual function and property list associated with each symbol is tester-specific. A tester specification file in the tool contains detailed information about a given tester, such as the number of resources and their parameters, resource value ranges, tester specifications, and special connectivity requirements.

A schematic editor lets you capture test module schematics (TMSs), which include tester functions and a symbolic abstraction of the device under test (DUT). It also captures schematics in a modular form, where schematic represents a single test module. A test module represents a single set of connections between the tester and DUT.

Mixed-signal test

One of the key features of Dantes is that it allows mixed-signal simulation of the entire tester environment, including the DUT, load board and tester resources. The netlister automatically partitions and sends separate analog and digital netlists to the circuit and logic simulation engines. The netlister then automatically inserts the appropriate A-D and D-A interface models at the interface nets and provides full interactivity to both simulators. An integrated waveform display shows digital and analog signals.

After individual test module schematics are captured, they're compiled into a full test schematic, which provides a top-level view of the TMSs, relays, DUT connectivity, and other interface circuitry. On-screen windows show the number and types of resources still available and a library of common interface circuit structures with connectivity information for each pin on the DUT.

Dantes' test sequencer lets you graphically arrange the order of test sequences, depending on factors such as test time, setup condition and number of faults detected by that test. This lets you place high-dropout and short-duration tests first to reduce overall test time. A source code generator then automatically creates individual test functions in the language of the target tester. The program uses the parameter values entered under each tester symbol and provides tester setup conditions such as resource setting, loading, storing, connecting or disconnecting, initializing, and starting.

Dantes will be available in the third quarter as an option to Cadence's Analog Artist Design System and will sell for $80,000. Testers initially supported will be the HP 9480, LTX Synchromaster, Teradyne A 500 Series, and Yokagowa TS-1000. —*Mike Donlin*

Dantes at a glance

- Brings ATE-specific information to the design phase of analog and mixed-signal ICs
- Test rule checker ensures that designs are testable on equipment from Hewlett-Packard, LTX, Teradyne, and Yokagowa
- Composer tool assists in the development of the DUT load board design
- Test sequencer orders and prioritizes tests
- Test program generators automatically create test programs
- Available in the third quarter for $80,000

Cadence Design Systems
555 River Oaks Pkwy
San Jose, CA 95134
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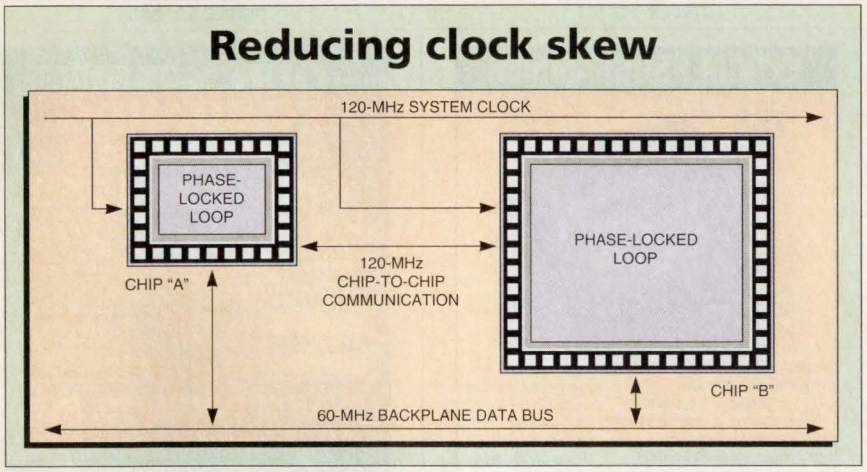
Circle 354

ASICs & ASIC DESIGN TOOLS

0.6-μm CMOS ASICs offer system performance solutions

The 300K ASIC family from LSI Logic is based on a 0.6-μm CMOS process and has up to 600,000 usable gates per device. The family includes gate array, cell-based and embedded array technologies. "All three technologies are vital in order to offer a total solution to system designers," says Peter Santos, product line manager for advanced array products. "All are cross-compatible, giving the user the ability to move from one to another. Some customers will use all three in one system." With I/O counts greater than 800, the new 300K products target high-complexity, high-performance system designs in electronic data processing, telecom, consumer, and military applications.

The three product families—the LCA300K compacted array series, the LCB300K cell-based series, and the LEA300K embedded arrays—share many application-oriented system features. To ease the design of complex electronic data processing systems, on-chip phase-locked loops (PLLs) eliminate chip-to-chip clock skew, and "balanced tree" clock distribution, which takes resistance-capacitance (RC) loads into account, reduces cross-chip skew. NMOS transceiver logic (NTL) I/O increases chip-to-chip and chip-to-backplane throughput rates. In telecom applications such as FDDI (Fiber Distributed Data Interface), PLLs ease the recovery of clocks from high-speed data streams. And in Sonet applications, with chip-to-chip frequencies of 156 MHz and greater, the 300K NTL I/O capability is useful. Pseudo-ECL I/Os and termination resistors (25- and 50-Ω) round out 300K system features.



Advanced system features substantially reduce clock skew in LSI Logic's 300K ASICs. On-chip PLLs eliminate chip-to-chip clock skew up to 160 MHz. "Balanced tree" clock distribution reduces cross-chip skew by up to 90 percent. With NTL I/O, chips can communicate at 120 MHz, with 60-MHz communication taking place on a backplane data bus. Data registers can boost the performance of such systems by bypassing the I/O bottleneck in pipelined designs.

For pad-limited designs, LSI Logic offers a two-layer metal option, and for core-limited designs, three layers of metal. The capability to stack vias enhances routability and minimizes RC delays. Though the 0.6-μm process technology is optimized at 5 V, LSI Logic is also offering libraries characterized at 3 V for battery-operated applications and at 3.3 V to meet IEEE standards. For 3-V operation in consumer applications, power dissipation is 0.4 μW/gate/MHz, datapath average, and 1.1 μW/gate/MHz, random logic average.

The LCA300K compacted array comes in 14 gate array masterslices with from 10,000 to 500,000 usable gates. A hierarchical block compiler facilitates integration. Gate delays are typically 215 ps, with operating frequencies to 75 MHz. With LCA300K you can put 96 kbits of SRAM or 384 kbits of ROM on-chip and still have 250,000 gates to play with.

The LCB300K cell-based ASICs have up to 600,000 usable gates. On a single chip you can implement 200,000 gates, 512 kbits of SRAM, and 1 Mbit of ROM. Library options include a silicon-efficient datapath library, advanced macrofunctions, megafunctions, and megacells.

Among LCB300K layout tools are a hierarchical block compiler, interactive datapath placer and router, I/O ring compiler, pad ring compiler, and memory compilers.

With the LEA300K, you can embed LCB300K cell-based memory—up to 512 kbits of SRAM or 3 Mbits of ROM—and complex logic functions into customer-defined masterslices. You can also incrementally add functionality, since the embedded arrays come in variable die sizes. After a trial layout defines minimum core size, the I/O compiler finishes the masterslice design and allows base wafer manufacturing.

LSI Logic is now accepting designs for its 300K family, which it supports with industry-standard packages and advanced packaging options. Nonrecurring engineering expenses start at $30,000. Production shipments will begin in the fourth quarter. —*Barbara Tuck*

300K CMOS ASIC family at a glance

- 0.6-μm drawn gate length—up to 600,000 usable gates
- Two- and three-layer metal options
- I/O count over 800, four-pad pitch options
- Library support for 5-V, 3.3-V, and 3-V designs
- System-design features including "balanced tree" clock distribution

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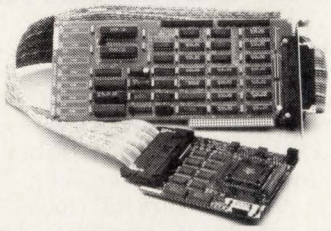

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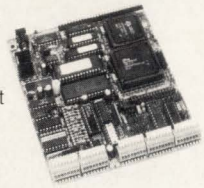

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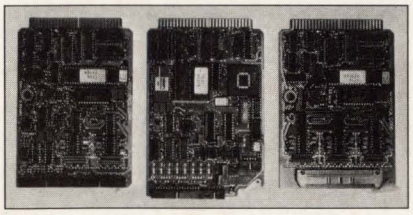

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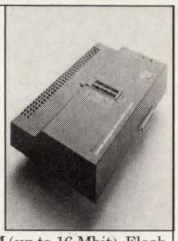

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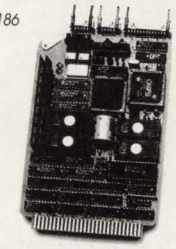

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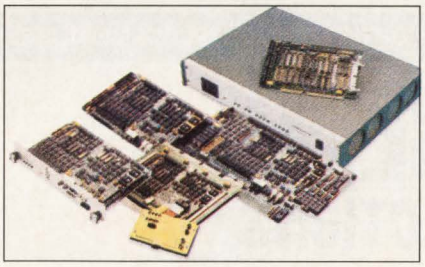

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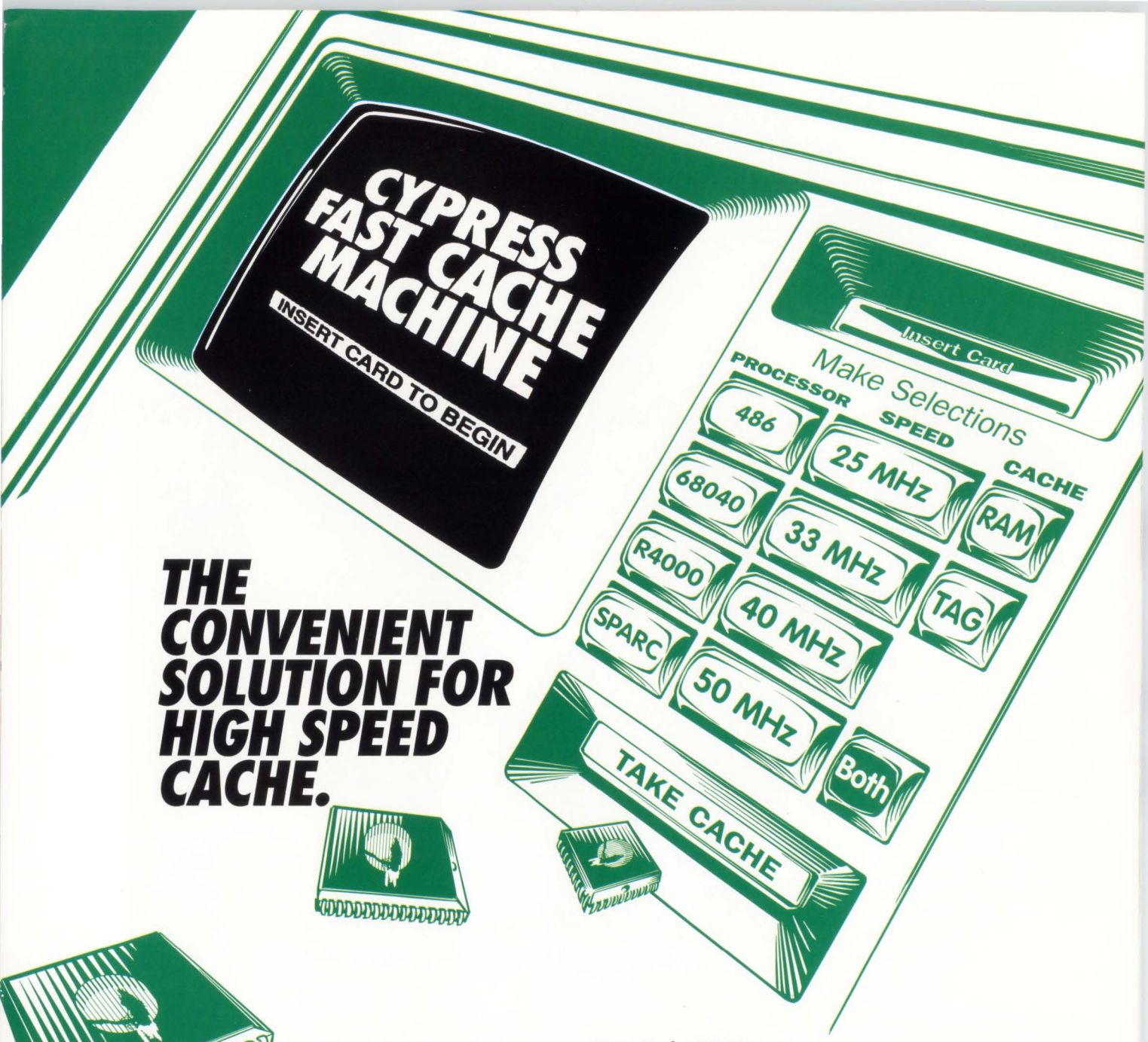

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