A PENNWELL PUBLICATION AUGUST 1992

COMPUTER DESIGN

Technology and Design Directions

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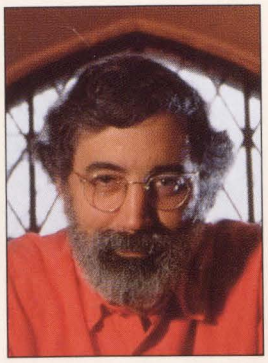

Ariel's Tony Agnello on: DSPs in multiprocessing

Making the 400-MHz computer a reality

MCMs push design and test tools to the limit

DSP boards reach performance highs

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CIRCLE NO. 1

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EMI/RFI Testing. We subject our enclosures to *in-house* testing per MIL-STD-285, providing an attenuation profile of each unit. When it comes time for you to pursue FCC or VDE approval of your system, we can perform these tests for you and resolve any problems immediately.

Whether it's off-the-shelf or something special that's off-the-drawing board, there's only one way to get the enclosure that's just right for your system. That's to call Electronic Solutions and put our experience to work for you.

VMEbus
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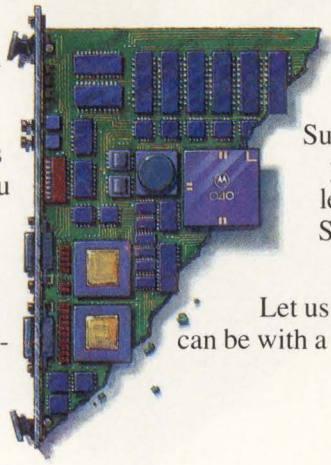
CIRCLE NO. 2

Why Settle for ½ an '040 Board?

You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may only give you only half of what you expected from the '040.

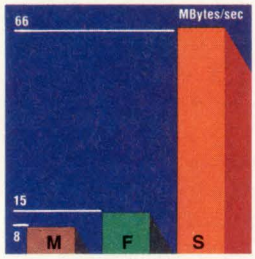
Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPs, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the SV430 outperforms every other SBC on the market by as much as 150%.



Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

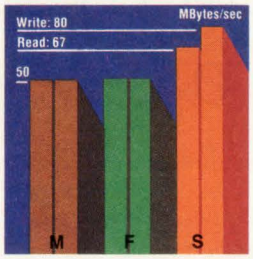
Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

Compare our specs. Synergy is superior across the board!



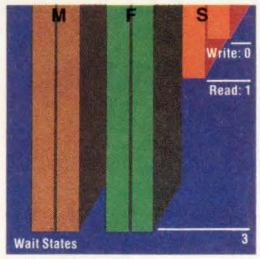
VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



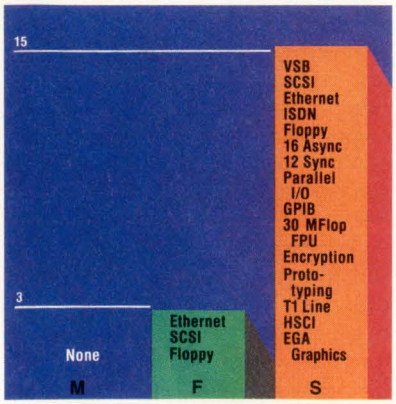
DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



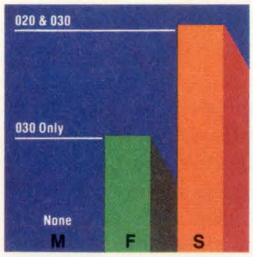
DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.



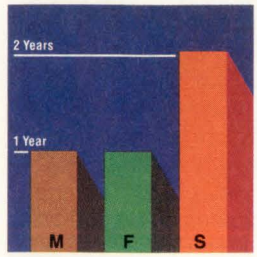
I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.



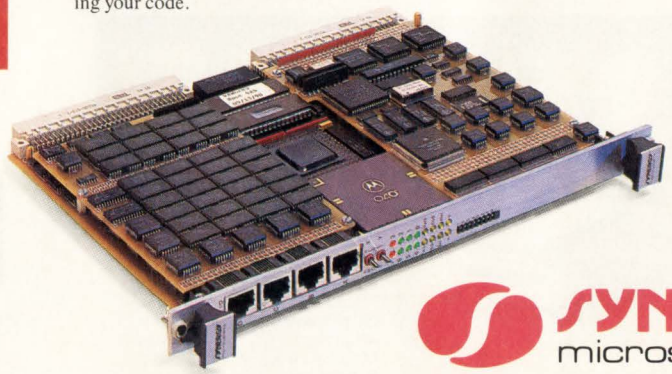
'020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.

SYNERGY microsystems

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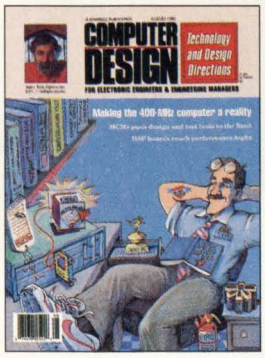
COMPUTER DESIGN

Technology and Design Directions

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



On this month's cover our engineer is surrounded by the trappings of high-speed digital design. Can he break the 400-MHz barrier? **83**

Illustration by Bill Morrison

COMING NEXT MONTH

Object-oriented languages in real-time applications

Futurebus+ and beyond

Designing ASICs for testability

16-bit microcontrollers

Data acquisition

SBus

NEWS BRIEFS

TECHNOLOGY DIRECTIONS

ASICs & ASIC Design Tools

Computers & Subsystems

CAE/CAD Tools

Software & Development Tools

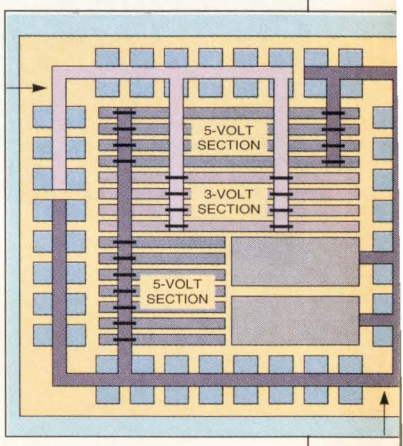
NEW PRODUCT DEVELOPMENTS

Computers & Subsystems

ASICs & ASIC Design Tools

CAE/CAD Tools

Software & Development Tools



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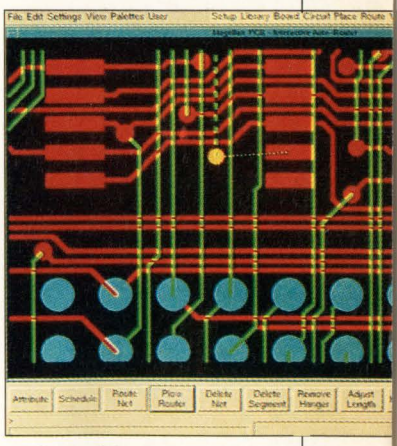

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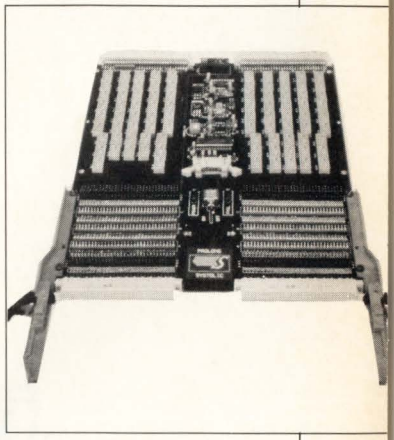

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Real-Time Software Performance Analysis and Test Coverage

HMI's Performance Analysis Card (PAC) provides real-time software performance analysis and real-time software test coverage for all HMI-200 series in-circuit emulators. This option operates completely transparent to the system under test and collects its data in real-time to establish a true profile of the software execution.

Features:

- Hardware implemented
- Up to eight modules can be defined
- Histograms for each module are displayed
- Minimum, Maximum and Average time duration for each module displayed
- Coverage mode displays which pieces of the code did and did not execute
- Trace data has a time stamp

Benefits:

- More efficient code produces higher performance products for your company
- Better tested code eliminates bugs generated from untested code and creates higher quality software for your company
- The Emulator and Performance Analysis together shorten the design cycle time allowing your company to have its window of opportunity in the marketplace

Available Emulators:

68000	68302	6809/6809E	68HC001	8085
68008	68301/303	68EC020	8051 Family	64180/Z180
68010	68330/333	68EC030	DS5000	Z80
68020	68331/332	68HC11 including F1 and D3	8096/80196 Family	68HC16 Family
68030	68340			

Now supporting 68040 Series

Write or call for further information and *free* demo disk.

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CIRCLE NO. 4

COMPUTER DESIGN Technology and Design Directions

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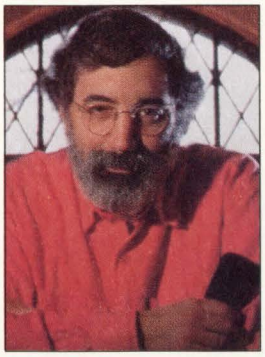


Ariel's Tony Agnello on: DSPs in Multiprocessing
DSPs are attacking the issues in multi-processing at all levels—chips, board and systems. **25**

TECHNOLOGY & DESIGN REPORTS

MCMs push design and test tools to the limit

Do multichip modules represent an exciting new technology or an exotic curiosity? Until the vexing problems of testability and yield are ironed out, few people are willing to hazard an answer to this question. —*Mike Donlin* **59**

DSP boards reach performance highs

Despite a slow start as a mainstream technology, DSP is performing tasks ranging from speech and image processing to embedded control. — *Warren Andrews* **69**

COVER STORY

Making the 400-MHz computer a reality

After clock distribution and caching architectures, the design of high-speed digital systems demands careful component selection and attention to physical layout. —*Stephan Ohr* **83**

DESIGN STRATEGIES

Calculated risk and aggressiveness pay off for Elan Graphics

When the Personal Iris deskside graphics workstation was unveiled to the world back in October, 1988, Marc Hannah, vice-president and cofounder of Silicon Graphics, had already begun thinking about his next design. **101**

COLUMNS

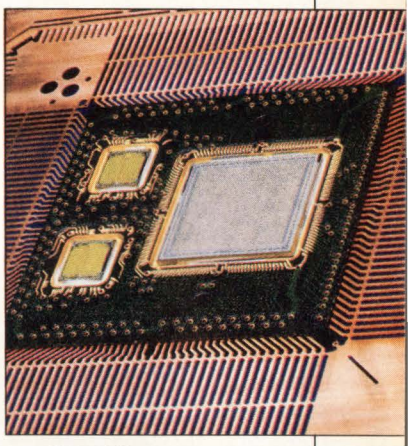
MIXED-SIGNAL DESIGN —*Stephan Ohr*

A&M-S: The place to see and be seen **109**

PRODUCT FOCUS

Video op amps get flatter and faster

As the electronics world shifts from analog to digital, video monitors are one of the last pure analog systems you're likely to find these days. —*Jeffrey Child* **115**



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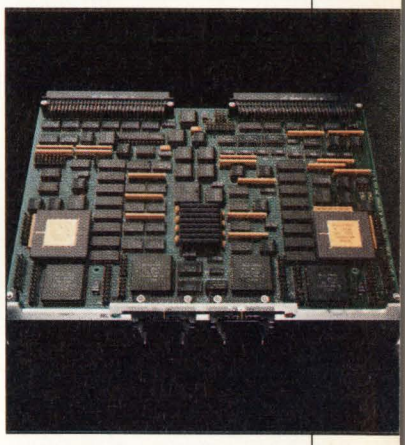

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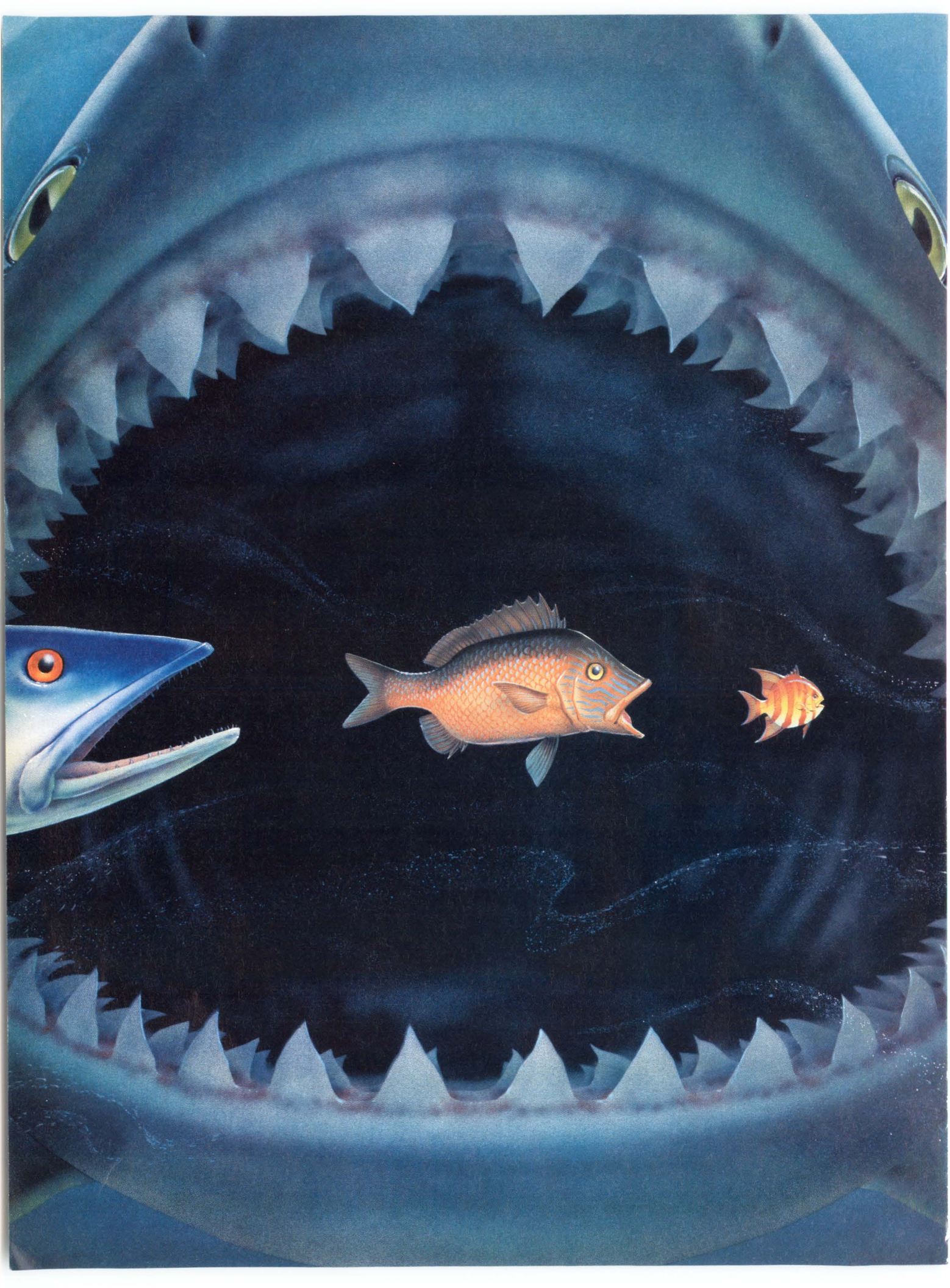


10ns BiCMOS 1 Megs from Motorola. Everything else is dead in the water.

1 Meg BiCMOS Fast SRAMs from Motorola demonstrate a simple evolutionary principle: survival of the fastest.

With 10ns access times at 1 Meg densities, nothing else even comes close enough to compare – for speed *and* density.

MCM6726	MCM6728	MCM6729■	MCM67282▲	MCM6727
128K x 8 bit	256K x 4 bit	256K x 4 bit	256K x 4 bit	1 meg x 1 bit
10●, 12, 15ns	10, 12, 15ns	10, 12, 15ns	10, 12, 15ns	10, 12, 15ns
MCM6706A	**MCM6705A**	**MCM6708A**	**MCM6709A■**	**MCM67082A▲**
32K x 8 bit	32K x 9 bit	64K x 4 bit	64K x 4 bit	64K x 4 bit
8, 10, 12ns	10, 12ns	8, 10, 12ns	8, 10, 12ns	10, 12ns

● 3Q92 ■ Output Enable ▲ Separate I/O

And as if that weren't enough to scare off the competition, these 1 Meg Fast SRAMs support both TTL and ECL I/O. They also feature an advanced pinout, with power supply, ground, and I/O pins centered on the package for reduced inductance and improved ground and power bussing.

Looking for even more speed? How about 8ns? That's the access time on our 256K BiCMOS Fast SRAMs.

Choose whichever speed-and-density combination is right for you. Either way you'll get the built-in quality and reliability of Motorola's high volume, sub-micron manufacturing.

Reel in the power of our BiCMOS Fast SRAMs for your next design, and get ready to throw everything else back in the water.

To request technical information or a sample device, just mail in the coupon or FAX it to Motorola's Fast SRAM FAX line at **1-800-347-MOTO (6686)**.

CD 8/92

Let's make some waves, Motorola.
Send me more on BiCMOS Fast SRAMs today.

Motorola, Inc. Fast SRAM Operations, P.O. Box 1466, Austin, Texas 78767

Name _____ Title _____

Company _____

Address _____

City _____ State _____ Zip _____

Phone _____

Application _____

Production Start Date _____ Estimated Usage: 1992 _____ 1993 _____

SRAM :

1 Meg TTL I/O		1 Meg ECL I/O		256K TTL I/O		
☐ 1 meg x 1	☐ 10ns	☐ 1 meg x 1	☐ 10ns	☐ 64K x 4	☐ 8ns	
☐ 256K x 4	☐ 12ns	☐ 256K x 4	☐ 12ns	☐ 32K x 8	☐ 10ns	*10 & 12ns Only
☐ 128K x 8	☐ 15ns		☐ 15ns	☐ 32K x 9*	☐ 12ns	

If you like what's new, wait 'til you see what's next.

MOTOROLA

Motorola offers a complete portfolio of BiCMOS and CMOS Fast SRAMs with densities from 16K to 1 meg, plus 2 and 8 meg modules. CMOS access times are as fast as 15ns (256K) and 20ns (1 meg).

NATIONAL KNOWS NETWORKING

In fact, National is the only silicon supplier to offer solutions across all three major networking standards: Ethernet, Token Ring, and FDDI. We know the market demands improved connectivity, performance, quality, **INTEROPERABILITY** and network management. And at National Semiconductor, we're providing market-driven mixed analog + digital silicon solutions to make all this a reality. Our first **ETHERNET** silicon helped foster the

THE NATIONAL

worldwide acceptance of LANs. In fact, well over 13 million Ethernet adapter cards have been designed using National's silicon — more than all other suppliers combined. National's ST-NIC™ was the first single-chip **10BASE-T** controller to put 10Mbps Ethernet on standard unshielded twisted pair wire. And our newest 16- and 32-bit solutions are making the first "Network Ready" PCs, MACs and peripherals a reality. National is also developing solutions to simplify the role of **NETWORK MANAGEMENT.** Our Product of the Year Award-winning RIC™ + SONIC™ chipset is the first to fully support the IEEE 802.3 mandatory and optional repeater management requirements. We're

also creating silicon solutions to ensure full interoperability of **MIXED MEDIA** and multiple protocol environments and to deliver new desktop services and applications. We've joined efforts with IBM, the leader in Token-Ring technology, to make it easier for your customers to seamlessly connect Ethernet and **TOKEN-RING** protocols. And we recently introduced TROPIC™, the industry's first fully-integrated single-chip Token-Ring controller. That's just the first step in a joint IBM-National relationship that will deliver new levels of flexibility to the world of networking.

STANDARD.

National is also providing new levels of performance with breakthroughs like **100BASE-T™** technology and our upcoming 2-chip FDDI solution. 100BASE-T is the first silicon solution proposed for **FDDI** across twisted pair copper wire. These solutions will drive affordable FDDI performance to the desktop. We're supplying proven "National Standard Silicon" today. And together we're **SETTING THE STANDARDS** that will take you where networks are going in the future. For more information, give National a call at **1-800-NAT-SEMI (Ext 191).** We'll show you why no one knows networking like National Semiconductor.

National Semiconductor

Xilinx enters PC-card market with FPGAs in TQFPs

In the same pioneering spirit to which it owes its past success, Xilinx (San Jose, CA) just announced that its XC2000 and XC3000 FPGA families are available in a thin quad flat pack (TQFP). By doing this, Xilinx has become the first FPGA supplier to enter the PC-card market. "The TQFP package provides up to 3,000 user-programmable gates in the space of a dime," notes vice-president of marketing Lee Farrell. Measuring 0.5 mm in pitch, 14 × 14 mm in body size and with a maximum height of 1.5 mm, the TQFP fits onto the tiny PC cards being used to add memory, storage and I/O capabilities to the growing numbers of notebook and handheld systems.

"The PC-card market has huge potential, and we expect to sell tens of thousands of our modem cards a month," says Xilinx user Carl Perkins, president of New Media (Irvine, CA). "Because the market is not sound, the reprogrammability feature of the Xilinx FPGA makes it ideal for rapidly changing standards and needs."

It's expected that by 1995 the majority of portable systems will be using from three to five PC cards each, creating a $1-billion market. Xilinx already has ten design wins worldwide for its FPGAs in TQFPs.

It won't be surprising if the next "first" from Xilinx involves 3-V capability for its FPGAs.

—Barbara Tuck

Signetics and start-up develop cell-based arrays

The recently announced Hi-IQ (High-Integration Qubic) arrays are neither conventional sea-of-gates arrays nor are they embedded arrays. Fabricated using Signetics' (Sunnyvale, CA) submicron BiCMOS Qubic process, the cell-based array family incorporates the BiNMOS-CBA architectural design of SiArc, a start-up specializing in silicon architectures and design tools for complex digital ICs. With 0.7-mm (L-effective) feature size and a bipolar transistor cutoff frequency of 13 GHz, BiNMOS achieves significantly higher performance than CMOS without the inherent high cost of BiCMOS, according to Signetics.

Hi-IQ arrays use two primary cell types—small MOS compute cells and larger MOS and bipolar drive cells—to increase efficiency and functionality over the typical sea-of-gates implementation. Since the density and performance of generated SRAMs are competitive with cell-based SRAMs, Signetics claims it's possible to implement SRAM-intensive designs normally requiring all-layer customization in metal-mask-programmable Hi-IQ arrays instead. "By blending a new architecture with advances in our BiCMOS process technology, these arrays will change the way designers create systems on a chip," says Signetics marketing manager of custom products Ray Becker. *—Barbara Tuck*

Firms ink deal to make advanced DSP chip

Analog Devices (Norwood, MA), Electronic Designs (Hopkinton, MA) and Westinghouse Electronic Systems Group (Baltimore, MD) have signed a multi-million-dollar contract with MIT/Lincoln Laboratory (Cambridge and Lexington, MA) to produce a single-chip DSP for high-performance radar and IR applications, image analysis, missile guidance, FIR filtering, and high-performance graphics. According to Analog Devices, the CMOS DSP devices will advance VLSI process technology with 0.6-µm geometry and 3.3-V operation, and will lead to commercial products for the open market.

Under the contact, Analog Devices is designing and fabricating the ICs, which are based on the company's 100-MFlops ADSP-21020 floating-point core. For its part, Electronic Designs is implementing the large on-chip memory. (Neither company would comment on how much memory would be required.) Westinghouse is managing the program and providing radar and electronic systems expertise. By late 1993, parts are expected to be delivered for building a multiprocessing system such as a 64-processor array with 6.4-GFlops peak performance.

—Jeffrey Child

Ricoh claims fastest learning neural chip

Japanese-based Ricoh has reportedly introduced a neural net chip that is the fastest of its kind. In a single die, the chip implements a 256-synapse neural net of 16 synapses by 16 neurons. The chip is a 200,000-gate array built using 0.8-µm CMOS technology. According to reports, the device offers a forward process speed of 3 billion connections per second and a learning speed of 1.5 billion connections per second. The learning speed is achieved using pipelines running at 12 MHz. By the end of this year, Ricoh expects that the chip will be designed into several robotics and factory-automation systems. Ricoh also has plans to use the chip in its own systems—as a processing controller for a copier machine, for example.

Called the RN-200, the new device is Ricoh's second neural chip. In 1990, the company developed the RN-100, a one-neuron chip with a total of eight synapses. Running at 10 MHz, the chip achieved speeds of 80 million connection updates per second for forward process and a learning speed of 40 million connection updates per second. *—Jeffrey Child*

Cadence develops model for DEC's Alpha chip

Cadence Design Systems (San Jose, CA) has sent a strong signal to the EDA community by announcing the first simulation model for the Alpha 64-bit RISC microprocessor from Digital Equipment Corporation (Maynard, MA). Cadence plans to offer the fully functional simulation model for the DECchip 21064-AA in this quarter, which will coincide with DEC's volume shipments of silicon.

The model was taken from Digital's internal design database. It works only with Cadence's Verilog-XL and VHDL-XL simulators and can run roughly nine CPU cycles/CPU second on a DECstation 5000.

Traditionally, complex microprocessor models have been developed by the silicon vendor and third-party modeling companies such as Logic Modeling, not by

Continued on page 12

Continued from page 10

EDA vendors. The move by Cadence signals that EDA vendors may be getting more involved in early model development, something that their customers have been wanting for years.

—Mike Donlin

MCM group hooks up global network

Dazix (Huntsville, AL), a subsidiary of Intergraph, recently launched the Advanced Packaging Consortium, a worldwide network of multichip module (MCM) designers and suppliers. The consortium, which boasts membership of about 380 companies and 2,900 individual users worldwide, kicked off its first meeting with a two-day conference that highlighted the materials and processes used in MCM development and production.

A unique feature of the network is that it allows instantaneous transfer of both textual and graphical data among members—data which can be used for presentations, design reviews and multisite development of MCM technology. The network's data management and conferencing capabilities were developed by Intergraph for NASA's *Freedom* space station effort and will now be used to form what Dazix claims will be the world's largest technical network of remote sites and engineers.

—Mike Donlin

Windows NT making triumphant noises

The arguments over the relative merits of and chances for Microsoft's (Redmond, WA) new Windows-NT operating system versus IBM's OS-2 2.0 continue to bubble. IBM (Armonk, NY) is shipping its OS but has so far met with a lukewarm response. Meanwhile, Microsoft staged an NT preview and conference in San Francisco for some 5,000 potential software developers, who appeared to come away starry-eyed. Not only did they get a chance to sit at machines and put NT through its paces, but they also got a beta copy of the operating system to take home with them. Microsoft also passed out NT software developers' kits to the attendees.

Whatever the differences between OS-2 2.0 and NT—and they don't appear to be enormous—it looks like NT has definitely generated some excitement in the community of independent software vendors. The OS-2 boxes available in stores use unsettling words such as "most" and "many" to describe the software's ability to run Windows and DOS applications. NT claims to be able to run them all. If it makes good on that claim—and succeeds in not damping the excitement it's already generated—it will probably emerge the winner, even though it's not scheduled to ship until early 1993.

—Tom Williams

Intel to license 386SL technology to crack handheld market

Intel (Santa Clara, CA), which is otherwise known for jealously guarding its 386 and 486 processor technologies, is entering into an agreement with VLSI Research (San Jose, CA) in which Intel will license the core technology of its 386SL processor. VLSI will then use the core technology as a basis for specialized processors for handheld products. Chips designed by VLSI Research around the Intel core will be manufactured at Intel fab facilities, but will be marketed by VLSI Research.

Intel is said to be investing $50 million to buy up about 20 percent of VLSI Research. The arrangement, which is a departure from Intel's usual way of dealing with companies wanting to manufacture 386-type products, may be a move to head off AMD and Chips & Technologies, companies which already have 386 functionality and are doubtless eyeing the potentially lucrative handheld market as well. *—Tom Williams*

SCI on the move

SCI (Scalable Coherent Interface) has cleared the final hurdle and has officially become IEEE Standard 1596-1992. SCI is often thought of as a bus, but in reality it's a packet-based protocol which transfers information over a number of independent unidirectional links. While the approach offers many bus-like characteristics, such as tightly coupled processor communication, loosely coupled I/O, message passing, and cache coherency, it does so at far higher speeds than can currently be achieved on buses. SCI is specified at 1 Gbyte/s to transfer data over a 16-bit-wide differential cable. Other options call for the same data transfer rate with a bit-serial protocol over coaxial cable of up to 20 meters, or over fiberoptics for up to several kilometers.

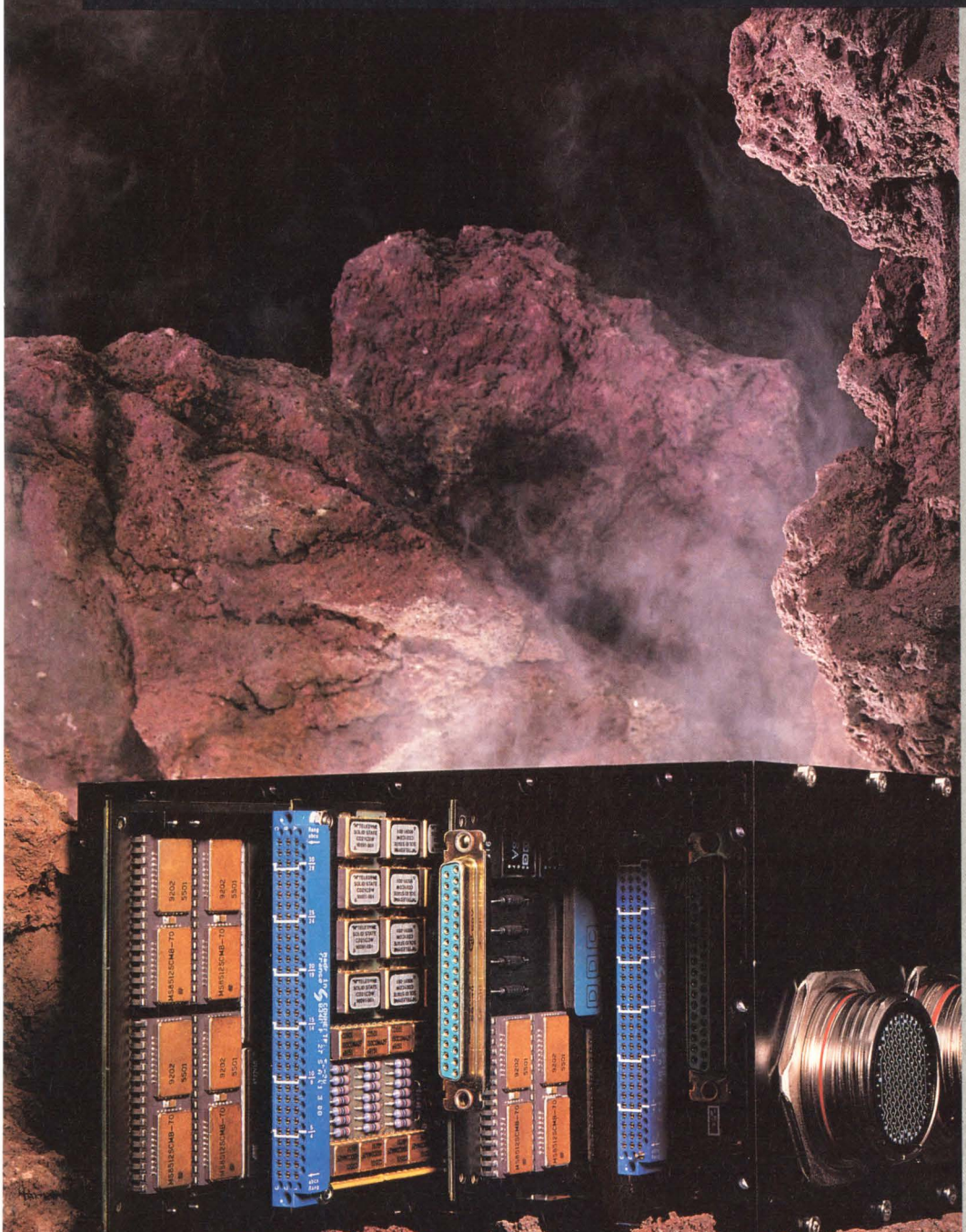
Because SCI relies on several independent point-to-point connections, multiple transactions can be going on simultaneously, unlike the case of a backplane bus, where only one node can have the bus at a given time. In addition, because of its flexible interconnection scheme, SCI can serve as an internal bus in a PC environment, a multiprocessing server or a network interface.

Hard on the announcement of the specification, SCI transceivers and protocol ICs are expected to emerge. In fact, Vitesse Semiconductor (Camarillo, CA) is currently completing a GaAs chip designed by Dolphin SCI (Long Beach, CA); a formal announcement is expected soon. It's also been reported that a somewhat slower CMOS version of the chip will be available later this year.

While SCI has been slow to get to market, its scalable architecture and flexible protocols, which let it interface to other buses, make it a promising technology. In addition, since the specification defines module, crate, connector, and power distribution systems based on IEEE Standard 1301.1-1991 ("Convection-cooled with 2-mm connector"), SCI is likely to emerge as a strong competitor to Futurebus+ in many applications.

—Warren Andrews

Rugged-MIL VMEbus: Setting New Standards



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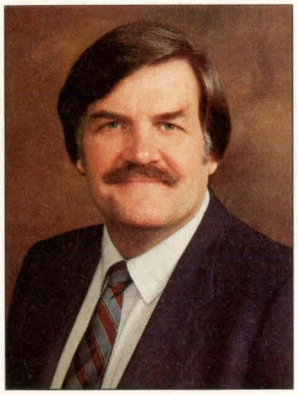
CIRCLE NO. 6

Dave Wilson is a tough act to follow

"We've found the person to pick up where he [Dave Wilson] left off."



John C. Miklosz
Associate Publisher/
Editor-in-Chief

Regular readers of *Computer Design* have probably noticed the absence of Dave Wilson's byline during the past couple of months. Unfortunately, serious illness in his family called him back to England and his contributions to *Computer Design*—and to the success we've been enjoying lately—had to end after a brief 11 months with us. Fortunately, Dave found himself a comfortable editorial spot outside of London and is settling in to his new, but definitely more routine, lifestyle.

Among his contributions to *Computer Design*, Dave brought a unique passion for talking to designers and readers and probing beneath the surface of the press releases and marketing hype that so often accompanies much of the information coming from vendors and suppliers. He helped immeasurably in sharpening our focus on designer/user/reader input and was a driving force behind integrating it with the usual input from vendors and suppliers into every part of the magazine. That input's added a unique dimension to our technology- and solutions-oriented "why-to" editorial, and it's another factor that we believe distinguishes us from the traditional product-oriented, "how-to" design publications.

No doubt about it, Dave is a tough act to follow. But we think we've found the person to pick up where he left off. More than that, we think we've found the person to help *Computer Design* move another step forward in its coverage of ICs and system design. That person is Don Tuite.

Don comes to us from Cypress Semiconductor, where he was a technical article editor ghostwriting and editing magazine articles, conference papers and technical backgrounders. (By the way, I'd like to take this opportunity to apologize to John Hamburger, Don's boss at Cypress and a long-time friend of *Computer Design*, for stealing Don away. He *is* too good to lose.)

Since receiving a BSEE in 1965 and an MS in technical writing in 1966, Don has done stints as a documentation manager, TV writer/producer, marketing communications manager, and public relations manager. In short, he has experience in—and understands—the engineering, management, PR, and publishing sides of the electronics/computer business. That puts him in an ideal position to probe "beneath the surface of the press releases and marketing hype." But Don has one advantage that Dave Wilson didn't have; he'll be based where the IC action is, in Silicon Valley. Don's presence there will give *Computer Design* an edge we've never enjoyed before. You'll start seeing the results of that edge in the next few months.

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Hynes Convention Center, Boston, MA. Buscon '92 East is the event where the products, technologies and components related to bus- and board-level design can be seen. The technical conferences, designed and coordinated by *Computer Design* and *Military & Aerospace Electronics*, are highly focused, in-depth seminars that explore the hottest issues from SCI to Futurebus+, RISC and embedded PCs. Contact: Registration Department, Buscon '92 East, 200 Connecticut Ave, Norwalk, CT 06856-4990, (800) 243-3238, Fax (203) 857-4075. **Circle 240**

September 20 - 24
International Test Conference

INTERNATIONAL TEST CONFERENCE 1992

Baltimore Convention Center, Baltimore, MD. This year's theme for ITC, the conference for the test and design community, is "Discover the new world of test and design." ITC will focus on the test and design techniques that companies need to compete globally, with emphasis on the integration of test factors into product design. There will be 16 tutorials and more than 35 technical sessions. Topics include: new test and design methods, MCM testing, BIST design techniques, test synthesis, and more. Contact: ITC, 514 E Pleasant Valley Blvd, Ste 3, Altoona, PA 16602, (814) 941-4666, Fax (814) 941-4668. **Circle 241**

September 21 - 24
Embedded Systems Conference

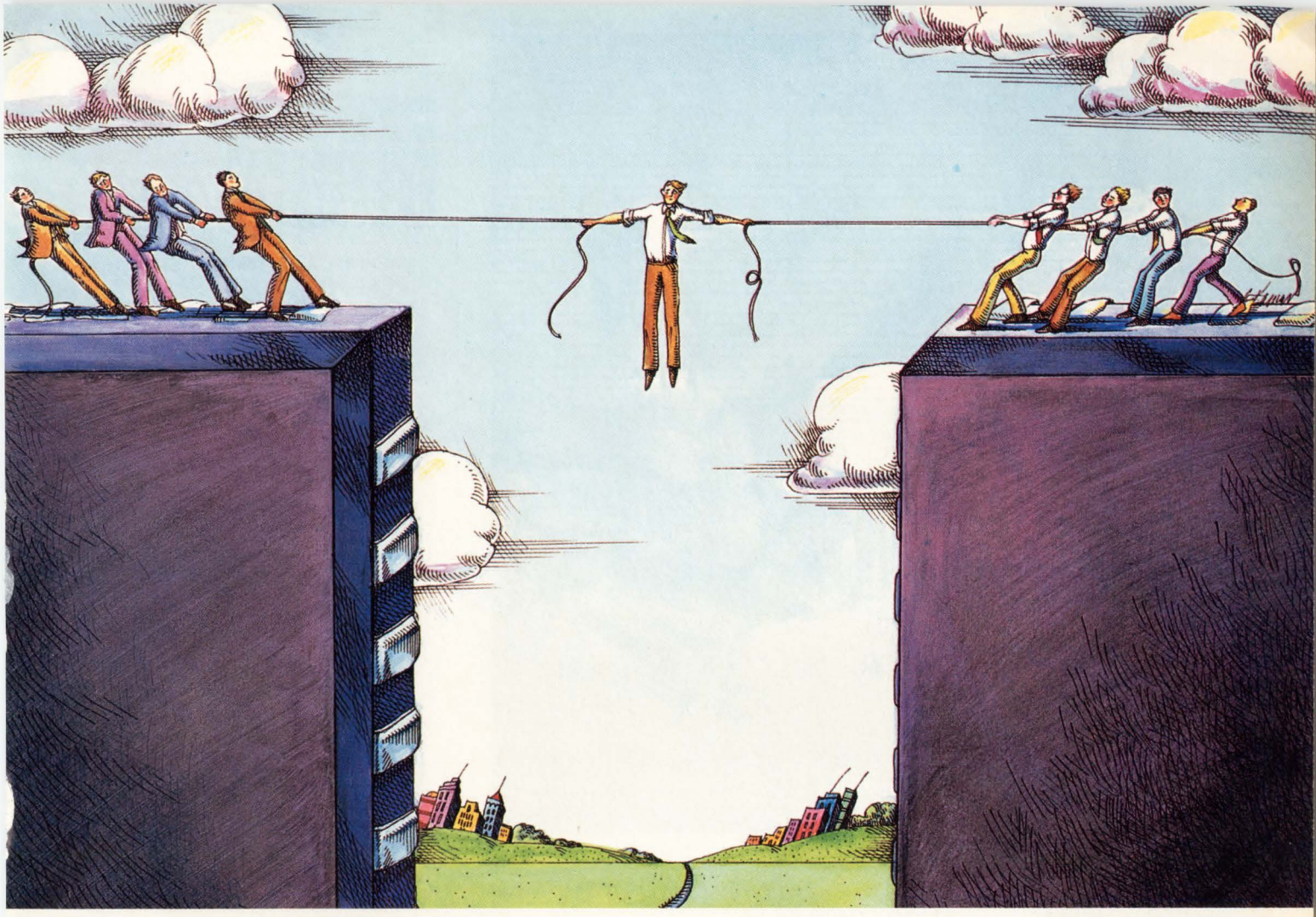
EMBEDDED SYSTEMS CONFERENCE

Santa Clara Convention Center, Santa Clara, CA. The Embedded Systems Conference and Exposition offers more than 80 lectures, workshops and tutorials about current tools, technology and theories in embedded programming. Full-day tutorials will include: object-oriented analysis, meta models for system development, event modeling for embedded systems programmers, and more. Contact: Miller Freeman, 600 Harrison St, San Francisco, CA 94107, (415) 905-2354, Fax (415) 905-2242 **Circle 242**

October 28 - 30
Analog & Mixed-Signal Design Conference

ANALOG & MIXED-SIGNAL DESIGN CONFERENCE

Hyatt Regency, San Francisco Airport, Burlingame, CA. The Analog & Mixed-Signal Conference is an intensive, three-day educational seminar and exhibition. The heart of the conference is a technical program organized by *Computer Design* and targeted at engineers and engineering managers working on high-speed digital, mixed-signal and analog designs who need to better understand design problems and the capabilities and limitations of the analog and mixed analog/digital ICs, ASICs and CAE/CAD tools they use, as well as the best approaches for implementing their designs. Contact: Betsy Anderson/Marketing Communications Manager, Computer Design, One Technology Pk Dr, Westford, MA 01886, (508) 392-2209, Fax (508) 692-7780. **Circle 243**



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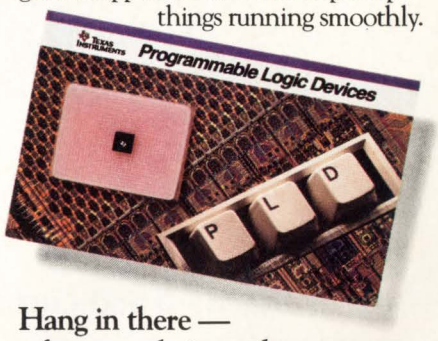

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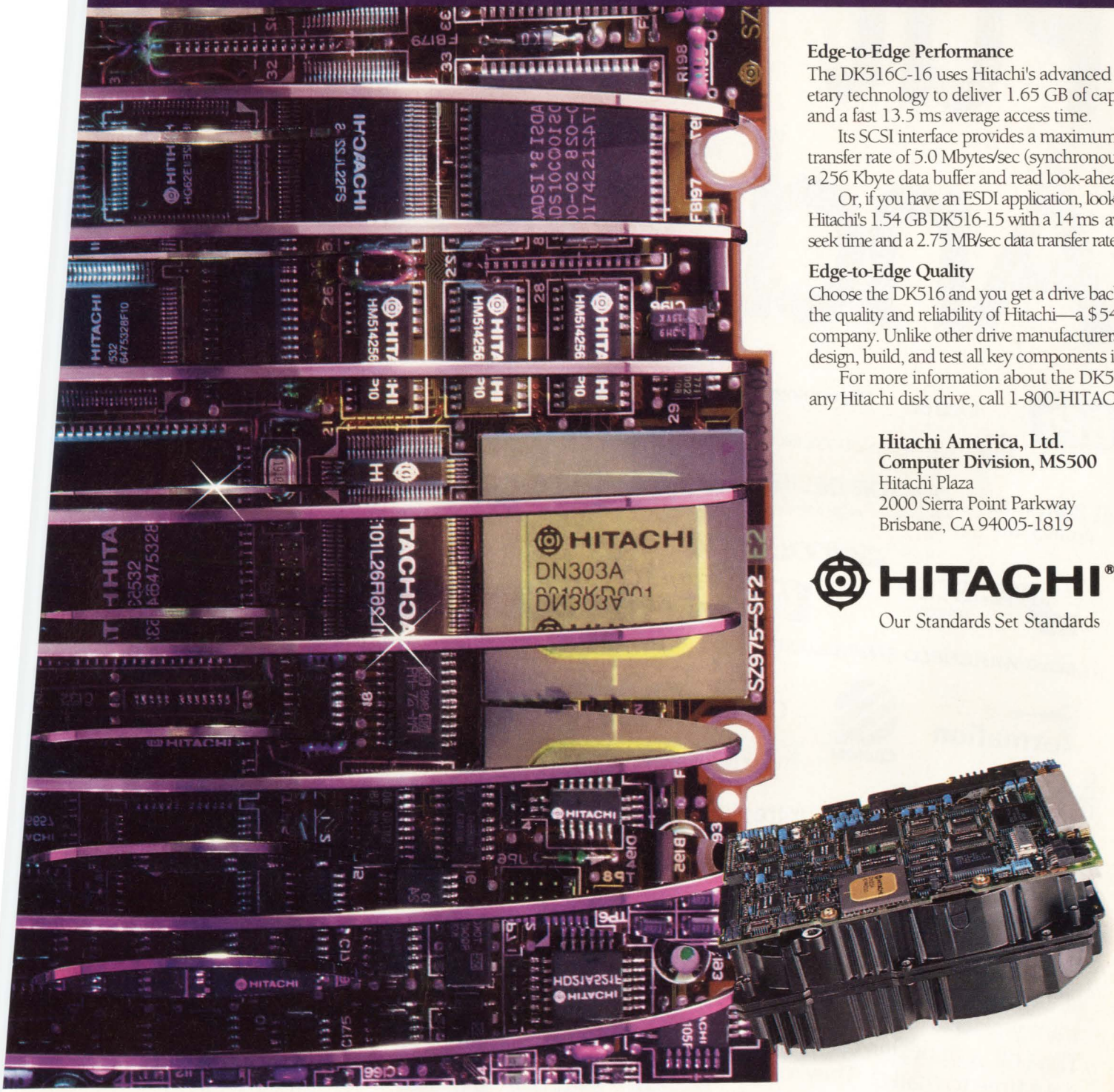

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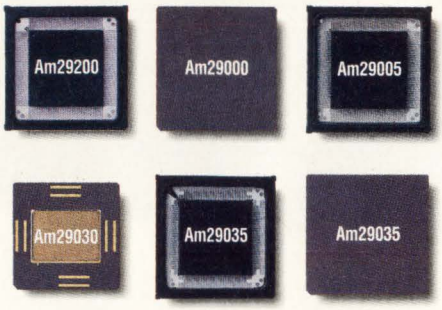

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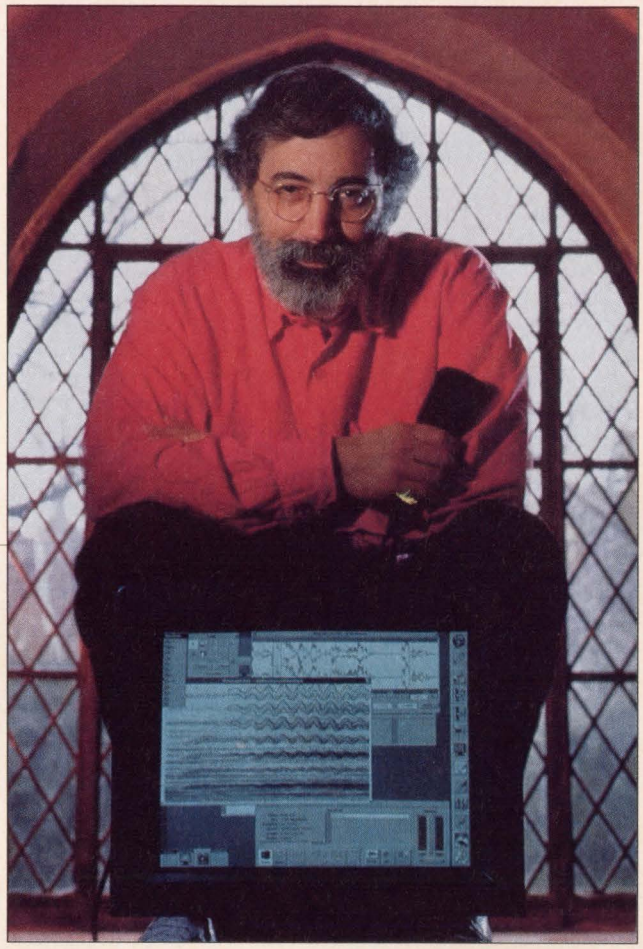
CIRCLE NO. 16

Tony Agnello on: DSPs in multiprocessing



As digital signal processors (DSPs) are applied to increasingly challenging, compute-intensive applications, multiprocessor architectures are becoming common. In support of these architectures, vendors of DSP chips, boards and development tools are beginning to add hooks that specifically address multiprocessing.

At the chip level, vendors are adding more powerful I/O and interconnect options that let designers combine multiple DSPs more efficiently and with greater flexibility. At the board level, vendors are packaging multiple DSPs using a broad range of point-to-point and shared-memory configurations. They're also supplementing the board's system bus interfaces with a host of specialized, high-bandwidth I/O channels that can be used for both data acquisition and multiprocessor communications.

And multiprocessor innovation hasn't been limited to hardware. To facilitate development of multiprocessing applications, vendors are offering parallel-processing emulators, debuggers and optimized libraries. At an even higher level, they're providing tools that can automatically generate code for multiple DSPs based on a block diagram specification.

For the run-time environment, DSP-based, real-time, multitasking operating systems offer synchronization and intertask communications mechanisms that can easily be extended to multiple DSPs. The most advanced OSs even provide scheduling mechanisms that automatically distribute tasks across multiple DSPs and provide load balancing.

Chip-level multiprocessing

One of the important ways chip vendors are adapting their DSPs for multiprocessing is through more sophisticated I/O. DSPs have long supplemented their memory bus interfaces with high-speed serial and parallel ports to support data acquisition and host communication. AT&T's DSP32C is a good example, providing a 25-Mbit/s serial port and a 16-bit, 12-Mbyte/s parallel I/O port with independent DMA.

Increasingly, however, DSPs are providing additional capabilities designed to facilitate high-speed, point-to-point communications between multiple chips. The Motorola DSP96002, to take one example, provides two 32-bit, non-multiplexed address/data memory buses, which in turn provide an effective means of connecting multiple 96002s.

For applications that require large numbers of closely coupled DSPs, the TMS320C40 by Texas Instruments takes a different approach. Like the DSP96002, the 320C40 features a pair of 32-bit external memory ports. In addition, however, the 320C40 sports six high-speed parallel I/O ports with independent DMA; these are ideal for implementing point-to-point links with other DSPs.

In many respects, the 320C40 is a throwback to the transputer, the original multiprocessing CPU. Over the last five years, considerable work has been done to support transputer-based multiprocessing. Regrettably, the transputer has enjoyed rather meager success, due primarily to its poor interprocessor communication rate. The transputer's four 10-Mbit/s serial ports give it an aggregate I/O bandwidth of 5 Mbytes/s. The 320C40, by contrast, features six byte-wide 20-Mbyte/s parallel ports, giving it an aggregate I/O bandwidth of 120 Mbytes/s. This 24× increase in interprocessor bandwidth makes practical a broad range of high-speed, point-to-point DSP networks—

Tony Agnello is president of Ariel Corporation, Highland Park, NJ

for example, 4-D hypercubes, 2- and 3-D grids and hexagonal arrays.

Board-level multiprocessing

Until recently, most board-level products carried only a single DSP. Consequently, if designers wanted to build a multiprocessor system, they did so by linking multiple DSP boards via a common system bus. The migration of DSP technology to larger form-factor buses such as VMEbus, together with advances in both VLSI and packaging technologies, has made it possible to combine several DSPs on a single board.

In most board-level multiprocessor architectures, each DSP executes programs out of high-speed local SRAM, which it accesses via an external memory bus interface. Inter-DSP communications are typically handled via some combination of shared-memory and point-to-point links.

Naturally, the DSP's I/O architecture dictates board-level multiprocessor options. AT&T's DSP3210, for example, is designed to use shared memory for multiprocessing, though conceivably multiple 3210s can be interconnected via the chip's single serial port, albeit with very low communications bandwidth. Motorola's DSP96002, by contrast, provides two completely independent 32-bit-wide ports, which are considerably more sophisticated than simple memory interfaces and lend themselves to a variety of multiprocessor architectures. And by providing a transputer-like interconnection scheme, TI's 320C40 facilitates any combination of shared-memory and point-to-point architectures.

Ariel has taken advantage of both these capabilities in a quad-320C40 VMEbus board known as Hydra. Each DSP on the Hydra accesses two banks of private SRAM memory via separate 32-bit external memory interfaces. One of these memory interfaces also connects each DSP via an isolation buffer to a shared-memory bus of up to 64 Mbytes, which is shared between the four DSPs and the VMEbus. In addition, each DSP is linked directly to the board's other three DSPs via dedicated byte-wide links called communication ports. Communications between DSPs can be conducted either through the communication ports or via shared memory.

System-level multiprocessing

In addition to providing an effective means of linking multiple DSPs on a particular board, the extended I/O capabilities of today's DSPs provide an effective means of linking multiple boards. Frequently, multiple-board systems rely on system-bus interfaces such as VMEbus, with shared memory to provide a host interface and to support interboard communications. Unfortunately, such interfaces lack the bandwidth required to support large numbers of boards, and are frequently tied up handling normal host-bus traffic.

Multiport DSPs such as the 320C40 make it possible to create arrays of unlimited size because they let you establish deterministic point-to-point communications between large numbers of DSPs on multiple boards. These point-to-point links not only provide higher bandwidth than most system buses, but they also avoid the overhead associated with bus contention and arbitration.

Ariel also adopted this approach in designing Hydra. On each Hydra board, three of the six parallel ports on each DSP are used to link it to each of its three DSP neighbors. The other three ports on each DSP are made available through an external VMEbus front-panel connector. Using these 12 ports (three per DSP), you can establish direct connections between any two DSPs on any two Hydras.

The New Jersey Institute of Technology (Newark, NJ) has leveraged the Hydra's I/O capabilities to develop a 64-processor system, which will be used to study advanced neural networks. Configured as a four-dimensional hypercube, the system uses 16 Hydras to achieve a peak performance of 17.6 billion operations/s.

The NJIT system is unusual because it combines traditional hypercube message passing with shared-memory communications. In the system, message passing is used to provide communications between neighboring DSPs, either on the same or on different boards. Shared memory, on the other hand, is used for transmitting information between remote nodes, managing shared resources and broadcasting information to multiple DSPs on multiple boards. Together, these two communications mechanisms let the NJIT system efficiently simulate a broad range of neural networks.

Software support the key

Even as more diverse DSP I/O capabilities expand multiprocessor hardware options, the real challenge will be developing application software that can take advantage of these architectures. Fortunately, parallel-processing development tools and run-time environments are emerging to help simplify this process. Among these are parallel-processing emulators, shared libraries that are optimized to execute on multiple processors and real-time operating systems with support for multiprocessor scheduling and load balancing.

Ideally, developing a C application for a multiprocessor DSP network shouldn't be much more difficult than developing one for a single processor. Essentially, the programmer writes the application as a series of tasks, assigns the tasks to the appropriate DSPs and defines the communications mechanisms between the tasks.

While these tasks may be compiled to run on the DSP in a bare-bones mode, there are advantages to running under a real-time operating system such as Spectron's Spox, 3L's Parallel C, and Perihelion's Helios. The biggest advantage is that these OSs simplify design by providing standard OS services—real-time, preemptive multitasking and memory management. They also provide synchronization and interprocess communications mechanisms, such as mailboxes and variable- and fixed-size FIFOs, which simplify the coordination of multiple tasks, both on a single processor and across multiple processors.

One way that both Parallel C and Spox simplify multiprocessor development is by supporting virtual channels. Virtual channels let you implement interprocess and intertask communications without specifying physical connections in your application programs. The actual communications mechanism is determined by a driver, which you select via a con-

figuration table.

The advantage of this technique is that it lets you change the system configuration without changing the source code. If you want to change the connection between two DSPs—for example, from shared memory to a direct communications port link—you simply select a new device driver in the configuration table.

In addition to providing convenient interprocess communications mechanisms, some DSP OSs are beginning to add advanced multiprocessor capabilities that enable them to automatically schedule, distribute and interconnect tasks running on multiple DSPs. An example is Perihelion's Helios real-time OS. Originally developed for the transputer, Helios now supports mixed networks of transputers and 320C40s.

With Helios, you develop your applications as a collection of tasks that are linked via virtual communications channels, just as you would for a single processor. You then provide the OS with network configuration information such as the parallel-processing programming model (sockets, farming or communicating sequential processes) and system resources (such as, the number of processors, communications and I/O options).

Once you've developed your program and specified the system configuration, Helios automatically dispatches tasks to the appropriate DSPs and establishes the appropriate communications mechanisms (for example, a FIFO, adaptive routing or parallel message transfer). Moreover, if you want to add DSPs or change the system configuration, you don't have to change your source code or redefine the system's communications links. Helios automatically redistributes the tasks to multiple DSPs and reroutes the communications channels.

Consider, for example, the addition of a DSP to a uniprocessor system running a program with two tasks. In the uniprocessor system, Helios might establish communications between the program's two tasks via a mailbox in local memory. When a second processor is added to the system, Helios can automatically move one of the tasks to the second processor.

If the two DSPs are linked via their parallel ports, Helios might also change the communications mechanism between the DSPs from a shared-memory mailbox to a FIFO-based, point-to-point parallel link. The designer simply tells Helios that a new DSP has been added and how it is connected. Based on that information, Helios automatically determines an optimal message-passing strategy and task distribution.

Shared-memory multiprocessing

Operating systems such as Helios are optimized for scheduling and routing applications that are developed for large numbers of interconnected point-to-point DSPs. For small numbers of DSPs executing out of shared memory, AT&T's VCOS (Visible Caching Operating System) offers an interesting approach.

VCOS, which was developed for multimedia applications, consists of two parts: a real-time multitasking kernel that runs on the DSP and an applications server known as VCAS (VCOS Application Server) that runs on the host computer. VCAS is responsible for scheduling and loading tasks from personal computer or DSP local memory onto AT&T's DSP3210. VCOS provides interprocess synchronization primitives and manages the sequencing and execution of both real-time and non-real-time tasks in a time-sliced manner.

Neither VCAS nor the VCOS kernel provides any specific multiprocessing capabilities. This capability is provided through a separate software component known as the VCOS Resource Manager (VRM), which maintains the information needed to perform task distribution and load balancing.

When a PC-resident application requires a DSP's services, it makes a function call to an Application Programming Interface (API), which asks the VRM for information about the function or task, such as the current system load and each task's compute requirements. The VRM, in turn, tells VCAS which DSPs are available and where the tasks can be loaded.

To boost performance and maximize bus bandwidth utilization, VCOS uses a technique known as visible caching. Visible caching lets you lock the instructions and data required for each processing frame (prior to the execution of the frame) in a cache on the DSP3210.

By caching this information, VCOS is able to ensure a 100-percent hit rate for each frame, minimizing external memory accesses. At the same time, moving data a block at a time rather than a sample at a time enables VCOS to minimize bus arbitration overhead and leverage high-speed memory access modes, such as page mode. Together, visible caching and block processing let VCOS greatly reduce the bus bandwidth required for each DSP. This, in turn, lets it efficiently support a greater number of DSP3210s in a shared-memory architecture.

A high-level approach to parallel programming

Development tools such as parallel-processing emulators, compilers, shared libraries, and operating systems provide software developers with a solid foundation for building parallel-processing applications. Increasingly, however, a new breed of even higher-level development tools is emerging that separates designers from the underlying details of the DSP hardware.

One example of such a tool is Comdisco's MultiProx, which supports both Motorola DSP96002- and TI TMS320C40-based multiprocessor platforms. Using MultiProx, you describe your applications by interconnecting blocks that represent functions such as FFTs, filters and I/O. You then draw bounding blocks around the portions of each diagram that you want implemented on a particular DSP. MultiProx, in turn, will automatically compile the block diagram and establish the communications mechanisms needed to execute the program on multiple DSPs.

Tools such as Comdisco's MultiProx are an important step in helping to insulate you from the details of the underlying DSP hardware. As multiprocessor configurations become more complex, high-level tools will be critical in making the raw MFlops inherent in big bunches of DSPs available to mainstream computer users.

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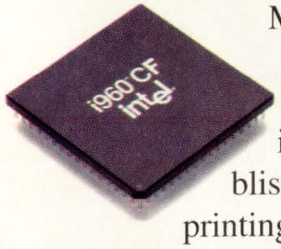

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CIRCLE NO. 17

ASICs & ASIC DESIGN TOOLS

ASIC choices increase for mixed 3-V/5-V designs

Barbara Tuck, Senior Editor

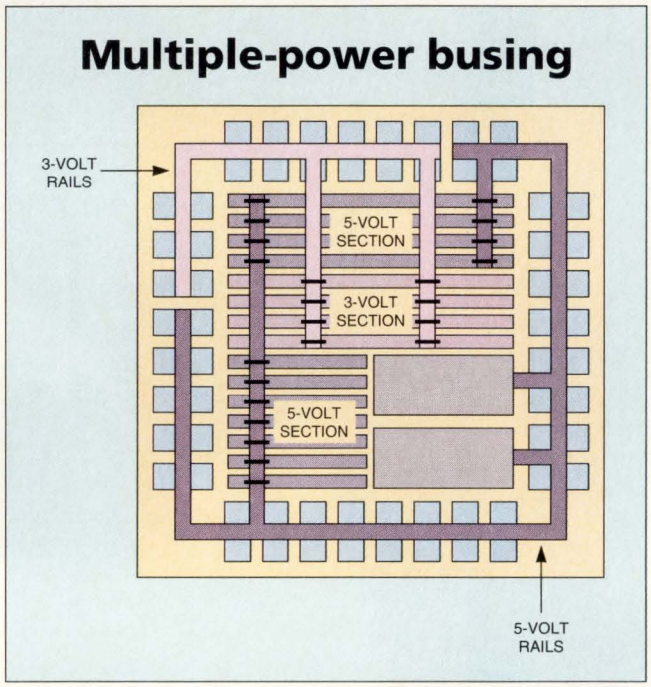
Leading ASIC vendors have been preparing for the rush to notebook, palmtop and pen-based computers by introducing low-voltage cell-based and gate array products. Among the latest to turn out 3-V libraries for portable and handheld computing systems is AT&T Microelectronics (Allentown, PA), whose 0.7-μm (0.6-μm L-effective) standard cell libraries let you mix and match 3-V and 5-V cells and macrocells on the same chip. While not as flexible as AT&T's offering, standard cell libraries from NCR Microelectronic Products (Fort Collins, CO) and new gate arrays from Atmel (Colorado Springs, CO) and Texas Instruments (Dallas, TX) also let you build mixed-voltage systems.

While designers are waiting for all the pieces to make systems that are exclusively 3-V, ASIC vendors have been offering chips for dual-voltage systems. Although low-voltage DRAMs, SRAMs, microprocessors, and logic devices are available, 3-V peripherals are hard to find. Before shrinking geometries to 0.5 μm—as Toshiba America Electronic Components (Irvine, CA) has done with its optimized-for-3-V TC180G gate arrays (two-input NAND gates with fanout of two have a gate speed of just 210 ps)—most ASIC vendors are delivering transitional solutions based on 5-V processes and characterized for operation at about 3 V.

Each standard cell in AT&T's new library has been completely characterized for delay behavior over a selected range of V_{DD}, input slew rates, temperature, process variations, and capacitive loads.

A drawback of this current low-voltage technology is lower performance for 3-V devices compared to 5 V. For AT&T's new 3-V, low-power LP600C CMOS standard-cell library elements, for example, the typical delay for a two-input NAND gate at 25°C with a fanout of two is 0.88 ns, while the same gate in the 5-V high-speed HS600C library has a delay of just 0.48 ns. And while system speeds for the LP600C library go to about 70 MHz, the 5-V HS600C library features system speeds above 100 MHz.

Nevertheless, once vendors go to 0.5 μm and optimized-for-3-V processes with higher performance, most, like Toshiba, won't offer the flexibility of dual-voltage systems, although SGS-Thomson Microelectronics (Paris, France and Agrate, Italy) plans to relax design rules in its 0.5-μm process to accommodate mixed-voltage I/Os.



Designers using AT&T's 0.7-μm CMOS LP600C and HS600C standard cell libraries can mix 3-V and 5-V cells and macrocells on the same chip. Macrocells characterized at both 3 V and 5 V include an 8-bit controller, UART, DMA controller, interrupt controller, real-time clock, memory mapper, and programmable timer.

Making the change

In the meantime, to achieve increased reliability and extended battery life, as well as to utilize the lower-cost plastic packaging made possible by the reduced power consumption of 3-V devices, system designers have had to make the transition from 5-V to 3-V systems. ASIC technologies such as AT&T's 0.7-μm libraries—characterized at 5 V as well as 2.7 to 3.6 V and supporting JEDEC 8.0 for CMOS, JEDEC 8.1 for TTL and the proposed JEDEC JC-16 for battery-operated systems—plus 3-V/5-V ASIC macrocells should, for the time being, help you build systems that have to operate for many hours on batteries. Kevin Kolwicz, department head of ASIC technology and libraries at AT&T Bell Laboratories, says that if you work with AT&T, you can easily mix 3- and 5-V cells and macrocells, minimizing power with 3-V elements while pushing the performance of critical paths as needed with 5-V elements.

"This offering dismantles the 'Berlin Wall' separating power-sensitive design from high-performance design," remarks Dan Di Leo, AT&T's ASIC marketing director. "You don't have to sacrifice performance at 3 V. Compact 0.6-μm circuitry is one reason. And where part of a circuit simply can't run fast enough at 3 V, you can put in 5-V cells."

Tools mix it up

What does all this mean for design tools which up until now have had the luxury of assuming a global power supply? To support 3-V/5-V systems, AT&T offers single-pass timing calculation for accurate simulation, translator cells for interfacing 3- and 5-V core logic blocks with 0 dc power to maximize battery lifetime, a family of 3- and 5-V I/O cells

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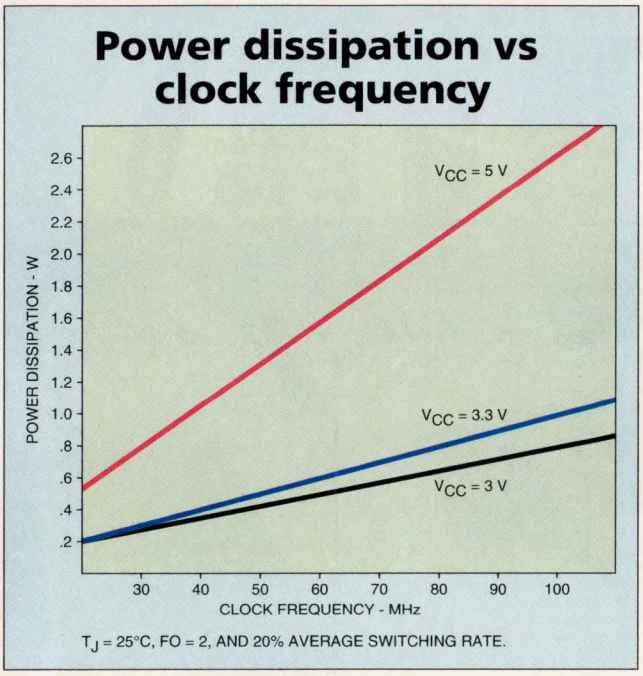
CIRCLE NO. 18

ASICs & ASIC DESIGN TOOLS



This graph from Texas Instruments illustrates how, in a 50,000-gate design with an average of 20 percent of the gates switching during each clock cycle, dropping the supply voltage from 5 V to 3 V can reduce power dissipation as much as 70 percent. TI claims its 0.8-µm CMOS TGC1000LV gate arrays achieve up to three times the battery life for portable and personal communications systems.

for interfacing with other devices, netlist audits for verifying connectivity between 3- and 5-V logic, and, most significantly, concurrent cell placement for 3- and 5-V logic during layout to minimize die area and routing parasitics. Synchronous and asynchronous SRAM compilers, a ROM compiler and a register-file compiler are available with the 0.7-µm libraries. And if you're working with AT&T's older 0.8-µm 900C CMOS standard-cell library (46 MHz at 3 V, 67 MHz at 5 V) and 0.9-µm BiCMOS HD750BC library (91 MHz at 3 V, 133 MHz at 5 V), you can mix 3- and 5-V cells as well as CMOS and BiCMOS on the same chip.

NCR, now part of the AT&T family, is also committed to supporting customers with mixed-voltage systems. NCR's first low-voltage library, the 0.95-µm (0.7-µm L-effective) VS700LV CMOS 3.3-V standard-cell library (the 3-V version of NCR's workhorse VS700H submicron library), has undergone an extensive specification process guaranteeing accurate functionality at 3.3 V, according to NCR. Careful characterization of each cell to determine its unique performance ensures that the ASIC and the system in which it resides will function exactly as specified. With the new library, you can mix 3- and 5-V I/Os to interface to a mixed-voltage system. You can't mix 5 V with 3 V in the core, however. Michael W. Morrissey, vice-president of NCR, says, "The new 3-V library will provide a solution for developers who need low-voltage ASICs, especially those customers who already have 5-V ASICs in their systems and want to upgrade to 3 V or transition to a mix of 3- and 5-V chips. They will be able to migrate a design from the 5-V to the 3-V library very easily, with only resimulation to the low-voltage design requirements." If you're developing a new product, Morrissey says this library will help you get to market at less cost.

NCR's VS700LV library requires less than half the power required by its 5-V counterpart. If you need embedded RAM, NCR is offering a 3-V customer-configurable RAM and plans to add other macro functions to the library. The company has incorporated JEDEC Standard 8.0 for CMOS and 8.1 for TTL into the library-specification process to ensure compatibility with standard devices being released for low-voltage products.

A balancing act

Atmel went through a fairly elaborate design process, according to John Ford, marketing manager for ASIC products, to balance the performance of 5- and 3-V library elements in its new 0.8-µm three-layer-metal ATL80 gate array family (11 arrays with routable gate counts to 180,000 gates and up to 490 pins). A two-input NAND gate with a fanout of two, at 25°C and 5 V, has a 200-ps gate delay; at 3 V, that delay goes up to only 270 ps. "Three-volt technology can't have a huge sacrifice associated with it," says Ford. "It's got to be optimized enough that it will be an attractive option." The ATL80 family library is specified from 5.5 to 3 V, and the devices will operate down to 2.4 V. Some I/O can operate at 3 V, some at 5 V, and the core at either 3 V or 5 V.

TI has developed a CMOS base cell to improve the low-voltage performance of its new 0.8-µm CMOS 3-V TGC100LV gate arrays. The enhanced base cell gives reliable performance in high-speed, high-density memory structures and in low-power logic gates when operated from supplies as low as 2.7 V, according to TI. "The conventional base cell does not provide effective memory density, reliable memory

Where do the low-voltage standards stand?

Three separate task groups of the JEDEC JC-16 Committee on Low Voltage and Interface are currently at work.

The task group addressing a 3.3-V unregulated standard reports that a ballot to establish the supply voltage operating range as 2.6 V to 3.6 V recently failed. The task group agreed to letter ballot an alternate proposal—2.7 V to 3.6 V.

The task group working on a 2.X-V standard has agreed to letter ballot a proposal for setting the supply voltage range to 2.5 V ±0.2 V. A proposal to set the supply voltage range in unregulated applications to 2.0 V to 3.3 V has recently failed passage via a committee letter ballot. An alternate proposal of 1.8 V to 2.7 V has been suggested.

The task group assigned to the revision of Standard 8.1 for LVTTL has had its work presented and approved for submission to the JEDEC Council with minor edits.

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functionality or reasonable memory performance when powered by low-voltage supplies," explains ASIC marketing manager Dave Berrill. "The new base cell is the most efficient yet reported when it comes to implementing memory." Metalized single-port SRAMs use only one base cell per bit. TI's CMOS base cell is useful in systems based on the JEDEC 3.3-V, ±10 percent, regulated voltage standard and the proposed JEDEC JC-16 for battery-operated systems, as well as the 5-V, ±10 percent supply of standard applications.

The TGC1000LV and the TGC1000 series of gate arrays, which support 5-V operation if higher performance is required, include 12 base arrays with up to 455,000 gates and 70 percent utilization. The TGC1000LV provides a direct interface to both 3-V and 5-V systems. The products support mixed 3-V and 5-V systems architecturally through separate output I/Os and specialized library macros. The macros will accept 5-V input signals when a device is powered by 3 V.

Like AT&T, TI is offering complementary CMOS and BiCMOS products. The new CMOS arrays and TI's BiCMOS TGB1000 arrays share common CAD tools, design flows and libraries. The low-voltage arrays are also supported by the Synopsys Test Compiler. Memory and datapath compilers are available.

Among other low-voltage submicron ASICs on the market are the LSI Logic (Milpitas, CA) 0.6-µm CMOS 300K family of gate arrays, cell-based and embedded arrays with libraries characterized at 3 V, 3.3 V and 5 V. For 3-V operation in consumer applications, power dissipation for 300K devices is 0.4 µW/gate/MHz, datapath average, and 1.1 µW/gate/MHz, random logic average. LSI Logic's 0.5-µm 500K ASIC family at 2.7 V, 3 V and 3.3 V is scheduled for release in late 1993. ■

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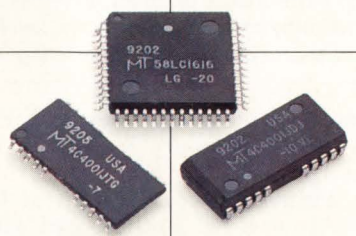
MT4LC4001 L	1 Meg x 4	4Q92
MT4C4256 VL	256K x 4	Now
5 Volt, Low Power, Extended Refresh DRAMs		
MT4C1004J L	4 Meg x 1	Now
MT4C4001J L	1 Meg x 4	Now
MT4C8512 L	512K x 8	3Q92
MT4C16256 L	256K x 16 DW[1]	3Q92
MT4C16257 L	256K x 16 DC[2]	3Q92
MT4C1024 L	1 Meg x 1	Now
MT4C4256 L	256K x 4	Now
MT4C1664 L	64K x 16 FPM[3]	Now
MT4C1670 L	64K x 16 SC[4]	Now



Part Number	Memory Configuration	Availability
3.3 Volt, Low Power Specialty SRAMs		
MT5LC2818 Latched	16K x 18	Now
MT58LC1618 Synchronous	16K x 18	Now
MT5LC2516 Latched	16K x 16	Now
MT58LC1616 Synchronous	16K x 16	Now
5 Volt, Low Power, Low Voltage Data Retention SRAMs		
MT5C1001 LP	1 Meg x 1	Now
MT5C1005 LP	256K x 4	Now
MT5C1008 LP	128K x 8	Now
MT5C2561 LP	256K x 1	Now
MT5C2564 LP	64K x 4	Now
MT5C2565 LP	64K x 4 $\overline{OE}$[5]	Now
MT5C2568 LP	32K x 8	Now

*Self Refresh [1]DW– Dual Write Enable [2]DC– Dual $\overline{CAS}$ [3]FPM– Fast Page Mode [4]SC– Static Column [5]$\overline{OE}$– Output Enable

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CIRCLE NO. 21

COMPUTERS & SUBSYSTEMS

PCI promises solution to local-bus bottleneck

Warren Andrews, Senior Editor

The demand for graphical user interfaces (GUIs) and other high-bandwidth peripheral functions in PCs has reached a point where traditional EISA, ISA and MCA buses can no longer keep up with the I/O requirements.

In an effort to keep up, designers are interfacing peripherals directly to the processor bus. This solution, however, often proves awkward and requires a lot of glue logic to adapt the bus to peripheral functions. In addition, peripherals can bog down the processor bus with I/O traffic when it should be handling processing-related tasks. To further complicate matters, processor buses tend to change with different generations of processors, making such approaches a temporary solution as well as a bottleneck in the design process.

There have been attempts at a better solution. The most notable comes from the Video Graphics Standard Association (VGSA—San Jose, CA), which has its VL local bus now in the final stages of development. A new local-bus specification from Intel (Santa Clara, CA), dubbed PCI (Peripheral Component Interconnect), is also emerging and will be directly competitive with VL.

Going its own way

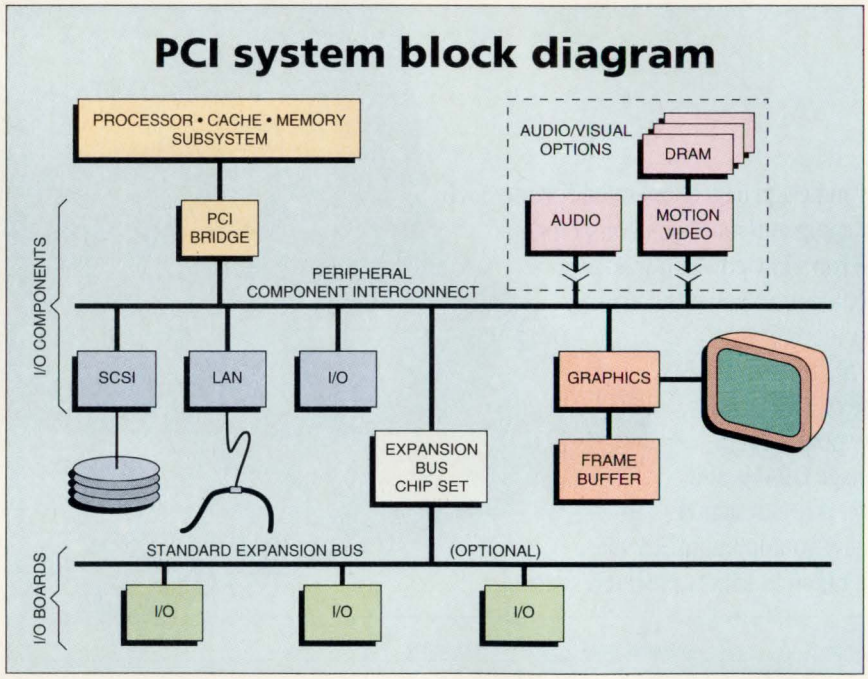
Intel was an early member of the VGSA group, but departed early to pursue its own ideas. The company now claims support from almost 40 major players, including Compaq, Dell, Digital, Hewlett-Packard, IBM, Microsoft, National Semiconductor, NCR, Siemens Nixdorf, Texas Instruments, and VLSI Technologies. This could set the stage for conflict, but much depends on the actual level of commitment from those in the Intel camp.

The proposed PCI specification defines a processor-independent, multiplexed, 80486-like data and address bus complete with enhancements for PC features. The multiplexed approach keeps pin count to a minimum to conserve board space and limit design complexity. It provides a peak bandwidth of 132 Mbytes/s, using 32-bit address and data lines. The bandwidth can be doubled by increasing the datapath to 64 bits. PCI also provides low latency—60-ns write access latency to slave registers from a master parked on bus—for I/O devices and networks and includes parallel bus arbitration, allowing for multiple bus masters with peer-to-peer access.

Processor and memory technologies have outstripped the capabilities of traditional buses, leaving designers to fend for themselves in providing high-performance graphics, LANs and I/O on PC motherboards with custom interfaces. PCI was designed to provide a standard electrical interface and a set of rules for adding low-cost peripheral ICs directly to a PC motherboard without the need for complex glue logic. In addition, the approach insulates designers from the continual changes in processor and memory technologies and architectures by providing a standard interface.

Intel's developers, however, stress that PCI is not a mechanical, a power, a connector, or a loading specification, even though some maximum guidelines are offered. The specification also doesn't give a single frequency for a bus clock, nor does it specify the arrangement of bus loads, nor does it consider layout issues. The disclaimer is to let designers know that PCI is not intended as a multiprocessor or general-purpose expansion bus, although it can be used with connectors for adding features.

What PCI defines is a pin-level interface that's intended to connect directly to components (ICs). It includes interface protocols, as well as ac and dc electrical specifications. And while it includes timing parameters, they're specified for maximum bus loading and frequency; this gives you the freedom to use the parameters with reduced bus loads or frequencies. The specification also calls for what Intel refers to as "innovative reflective wave signaling" to reduce costs while achieving



Intel's PCI specification calls for a high-speed motherboard peripheral bus to handle high-performance graphics as well as more demanding I/O. With a peak bandwidth of 132 Mbytes/s, PCI achieves the level of performance required for the latest megapixel approaches without interfering with the host CPU/memory bus.

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the performance goal of 33-MHz operation.

Forces driving PCI

Graphics was one of the computing areas driving the new interconnect standard, and PCI handles graphic functions at its peak bandwidth of 132 Mbytes/s. Expansion of the data bus to 64 bits is included to permit even faster transfers. For multimedia functions, the specification lets peripheral devices operate concurrently with CPU/memory operation, while still addressing the arbitration requirements of a multiple-master environment.

For network and disk I/O devices, PCI provides low latency and lets the system offer a guaranteed minimum bandwidth. It also features programmable-burst-size bus arbitration for single accesses, resource locks and support for look-ahead arbitration. In addition, PCI offers synchronous operation at up to 33 MHz, and is designed to be compatible with standard ASIC processes, separate configuration space and support for soft configuration, soft address mapping and three-party DMA.

Covering all the bases

The PCI specification is an inclusive document covering all aspects of what a peripheral bus should do—and then some. In addition to the regular bus transfer, control and arbitration functions, it deals with such features as parity, exclusive access, message passing, and other special bus extensions. It also includes options for other features. The specification, for example, covers support for cache, since entry-level or laptop systems may include part or all of the system memory and cache on PCI.

The caching support for shared memory is implemented by two optional pins, which transfer cache status information between the bridge/cache and the target of the memory request. The bridge/cache snoops all memory accesses on PCI and determines what response is required by the target to ensure system memory coherency. To avoid snooping overload, the bridge may be programmed to signal a "clean snoop" immediately on frequently accessed address ranges which are configured as non-cacheable.

Overall, PCI is a complex specification, and it will probably require significant support if it's to achieve the universal acceptance Intel hopes for. It's this same complexity, however, that makes it so appealing to so many players.

First, it provides the kind of performance needed for megapixel graphics systems and other high-speed I/O subsystems. Second, it takes a major load off designers by taking the processor/memory bus out of the I/O interface picture. Since PCI is processor-independent, processor buses and attendant

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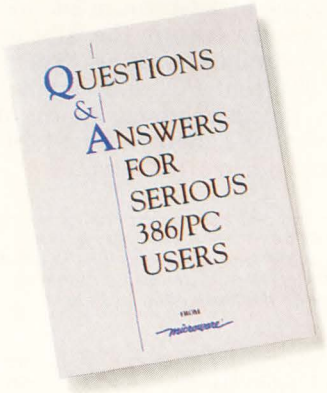

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memory architectures can continue to be the family jewels of high-performance design without having any interference from I/O interfaces.

Another major benefit of the approach is that it extends the life of many peripheral chips and chip sets, because they now will share a standard interface with the processor bus on one hand and the I/O bus on the other, without having to change with each new generation. This actually extends the life of a design in industrial or longer-lived implementations, as well as saving precious design time in upgrading to next-generation processors in such applications.

The other edge

But Intel's PCI may prove to be a two-edged sword. While its complexity and performance are the very features that make it attractive, they also increase design and layout difficulties. Intel suggests that "system designers will provide their own proprietary solutions in these areas. It is possible that such solutions may become standardized to some extent." This obviously leaves the door open to possible suggested or recommended practices covering a variety of potential problems.

Another potential problem is what Intel refers to as a "bridge," which sounds a lot like a bus controller. Such a bridge (or bus controller chip, chip set, board, or module) performs many functions, including acting as a buffer between the CPU and PCI buses while maintaining the PCI bus in synch with the processor. It must also handle bus arbitration and some level of cache coherency between buffers on the peripheral bus and those in the rest of the system and between memory and caches on the PCI bus itself.

VGSA's VL bus, by comparison, is relatively simple and can be manufactured now with existing silicon and no change to current peripheral chips. But it only supports a limited number of peripheral devices—four or five compared with the nine of PCI—and doesn't offer the flexibility or performance of the Intel offering. The differences between the two approaches, however, are sufficiently great that there probably won't really be any showdown between them. VGSA's approach will serve the short-term needs of system vendors until the silicon required for PCI matures. Then, it's expected that PCI will step in and take its place among many other significant computer standards to emerge during this decade. ■

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COMPUTERS & SUBSYSTEMS

Ring datapath speeds 200-Mbyte/s transfers

Tom Williams, Senior Editor

Over the last decade, "processors, memory and disks have all increased in speed and capacity by one to three orders of magnitude," notes Paul Sweazey, "Ringleader" of the advanced technology group for Apple Computer (Cupertino, CA). What hasn't advanced is the ability to move data between boards in a system. "That's why really high-performance systems tend to be 'pizza boxes' or very, very expensive," he adds. "It's not that modular isn't still good; it's that modular doesn't work because the performance of the bus connecting the modules didn't scale with everything else."

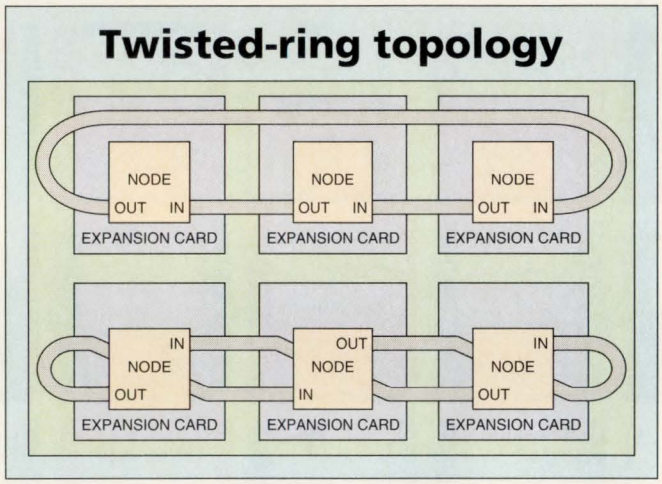
Of course, very expensive systems do implement high-speed internal datapaths. The trick is to do it cheaply. Now Apple, working with National Semiconductor (Santa Clara, CA), along with cable and connector manufacturer Beta Phase (Menlo Park, CA), has developed a cost-effective, point-to-point connection technology that can move data among boards in a system at 200 Mbytes/s. Apple's QuickRing technology will be held by the company for about six months, but then the chips and connector technology will become generally available to system designers for use in personal computers, workstations and other systems where high-speed transfer of large amounts of data is needed.

One application envisioned initially by Apple is for use in multimedia graphics and video. The data rate would make possible full-motion color image processing and animation in real time.

Take a cable...

QuickRing is based on a cable and connector technology developed by Beta Phase, and on a switching chip developed by National. As implemented by Apple, QuickRing requires a slight design modification—a notching—in the top of a NuBus board to accommodate the cable connector and on-board connector traces. Beta Phase, which designed the internal cabling and connectors for the new Cray machines, uses "microstrip geometry," a flexible photolithographiccable design that allows a high aspect ratio between the size of conductors and the space between them relative to the distance to the ground plane.

The result is signal crosstalk of less than one percent. According to Beta Phase general manager Charles Byer, "You can't achieve anything near that with standard pin-and-socket connectors." Beta Phase also designed a connector that maintains the pin spacing while clamping securely onto the traces on the board. Having developed cabling systems capable of speeds of up to 500 MHz and with signal densities of up to 500 lines/in., Beta Phase has found QuickRing connectors, with 66 lines/in. density and 200-MHz signal frequency, well within its capabilities, Byer says.



The arrangement of QuickRing (below) differs from that of a ring for boards plugged into a backplane (above). The standard backplane ring has a long return segment that's "twisted" with QuickRing to ensure equal spacing between all nodes.

...and add a chip

National's contribution is its QuickRing chip, which acts as a switch at every node on the ring. A "twisted ring" arrangement ensures that the physical distance between all nodes on the ring is the same. This solves the problem of how to use a ring topology with cards that are also plugged into a backplane—in this case, the NuBus.

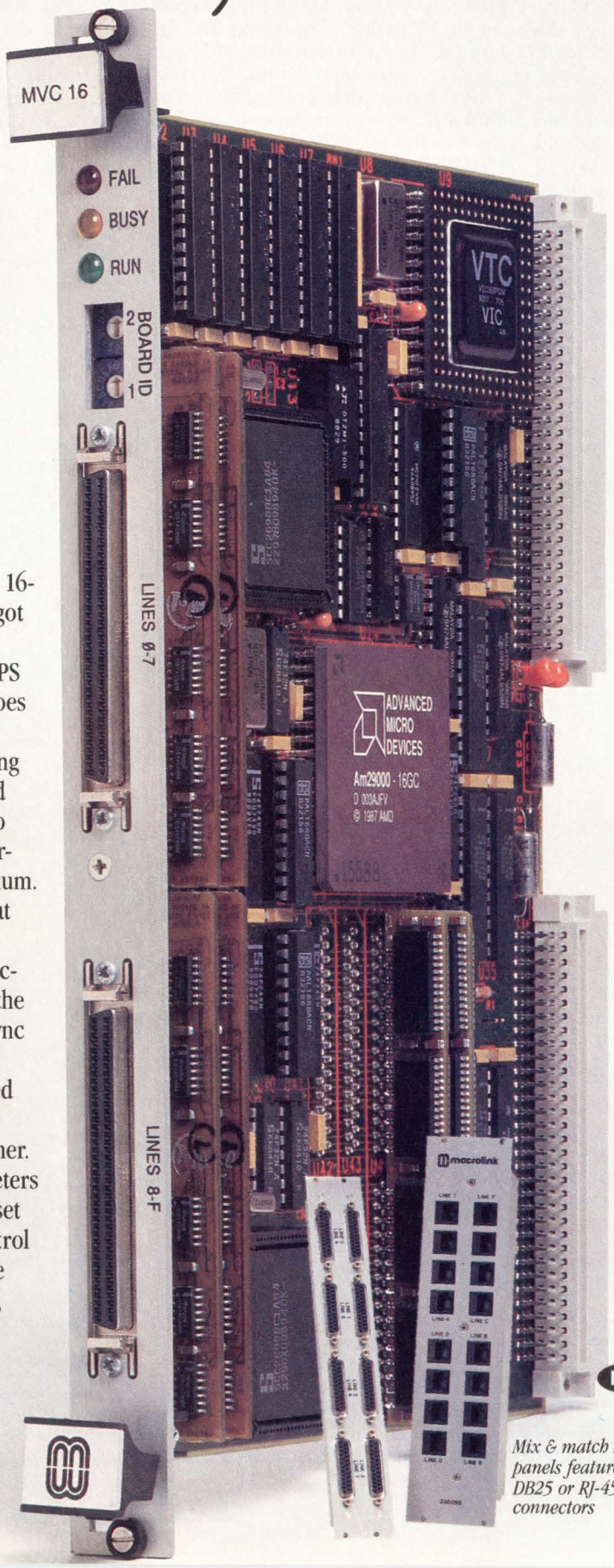
On one side of the board is the chip, which acts as a switch for the incoming and outgoing signals; on the other side is a loopback segment. This segment ensures that each transmitter sends the signal through two connectors and one card before encountering a receiver, guaranteeing that there's equal distance between all nodes on the ring—and that there's no long return path bypassing all the cards between the ends of a row. The datapath of the ring in this design includes six serial lines plus clock.

The signals pass into the receive port of National's QuickRing chip, one of which sits at each node of the ring; signals then pass out of the transmit port via 1 kbit of internal buffering. Also, there are two 33-bit ports for on-board memory read and write. The chip can simultaneously read and write four bytes, plus have a bit for framing into and out of memory at up to 50 MHz, which equals the 200-MHz bandwidth of the ring. The chip monitors the data stream as it passes through and decides what data is meant for it; it pulls this data off, depacketizes it and writes it to memory. It simply passes through data meant for another node.

The internal protocols with which the chip packetizes and multiplexes the data onto the ring are hidden within the chip and are as invisible to the designer as to the user, says Apple's Sweazey.

"It's important to remember," says National's marketing manager for

16 lines, No waiting.



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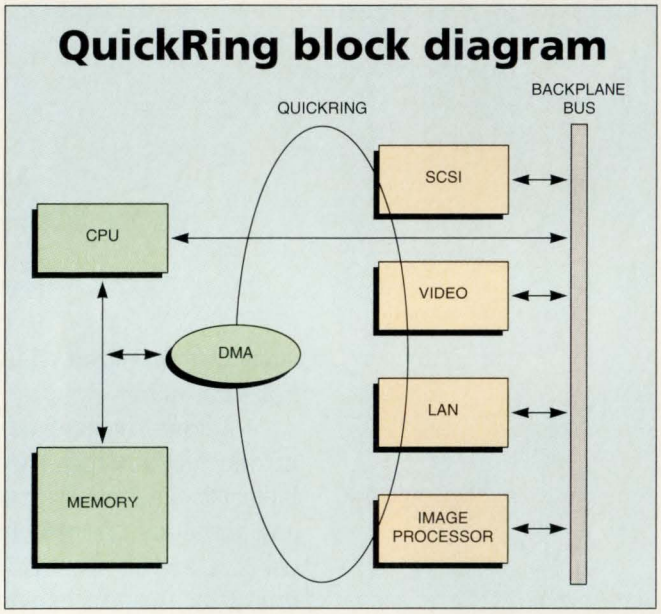
high-performance bus products, Phil Hughes, "that QuickRing is not a control bus; it's a data pipe." As such it isn't intended for random access of data in memory. Each transmitter sees the nodes farther along the path as logical FIFOs, and data moves in one direction around the ring. The backplane bus is still used for loading control programs, setting registers and randomly accessing data. "Theoretically," Hughes notes, "you could hook QuickRing into the CPU memory bus via a DMA bridge."



QuickRing is designed to work in a system that also incorporates a backplane bus. The high-speed datapath handles large, fast data transfers among modular boards, while the backplane bus serves for instructions and control. A DMA bridge to the main CPU memory bus could also be included.

Beyond 200 Mbytes/s

Both National's Hughes and Apple's Sweazey point out that the 200-MHz bandwidth is the maximum data rate between any two segments. By pipelining and overlapping data transfers, it's possible to obtain a higher overall system data throughput than 200 Mbytes/s. For example, if in a four-node system there was a transfer at 80 Mbytes/s between nodes A and B, and at the same time an 80-Mbyte/s transfer between nodes A and C, the total bandwidth load between A and B would be 160 Mbytes/s. If there were also an 80-Mbyte/s transfer between B and C (160 Mbytes/s total), the overall system throughput would be 320 Mbytes/s.

The overlap of data transfers takes place in the time domain up to the full bandwidth limit of any segment path involved. The current implementation of QuickRing allows up to 16 nodes. The chips are designed for a maximum efficient packet size to be put onto the ring. When bandwidth is available, the chip will put on an amount of data up to the maximum packet size. Packets have headers to identify the destination node. The chips are responsible for putting data on the ring and seeing to it that it comes off in the proper order. The programmer, then, can deal with simple transfer commands and can concentrate on processing the data once it's arrived, as well as sending it on when it's ready.

There are, of course, trade-offs in using this method versus a backplane bus. One of these trade-offs is latency. Although the ring is very fast, you're dealing with a round-trip scenario, so the maximum latency to get at data is the longest distance around the ring—less than 1 µs per block. On the other hand, the latency is predictable. You don't have to worry about bus contention and handshaking. A backplane bus becomes less efficient as it reaches saturation, while the ring becomes more efficient because there's little or no overhead to the data transfer.

More needed from interconnects

Both Beta Phase's Byer and National's Hughes agree that the microstrip geometry of the cable and connector technology could have far broader applicability. "There's a growing disparity between density and signal speed available from ICs and what's available through standard connector technology," Byer says. Witness the trend toward building processors with internal and external clocks, so they can process data more quickly internally and still transfer it via circuit boards. Microstrip connectors could conceivably be routed along critical high-speed datapaths on circuit boards.

In addition to the interboard version of QuickRing, Apple is looking to Beta Phase for a longer cabling technology—on the order of one meter—that would allow interconnection between two or three systems located very close together.

According to Hughes, National plans to be delivering QuickRing chips to Apple developers by the first quarter of 1993. He adds that the first QuickRing products would appear on the market by mid-year. National will be free to release the chip to the general market by the fourth quarter of 1993.

Beta Phase's Byer notes that the connector and cable technology isn't proprietary to Apple. His company, however, is committed—along with its partner, Molex (Lisle, IL)—to supply Apple's needs first through the initial period. ■

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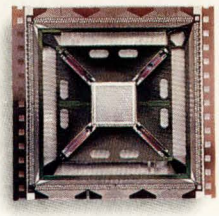

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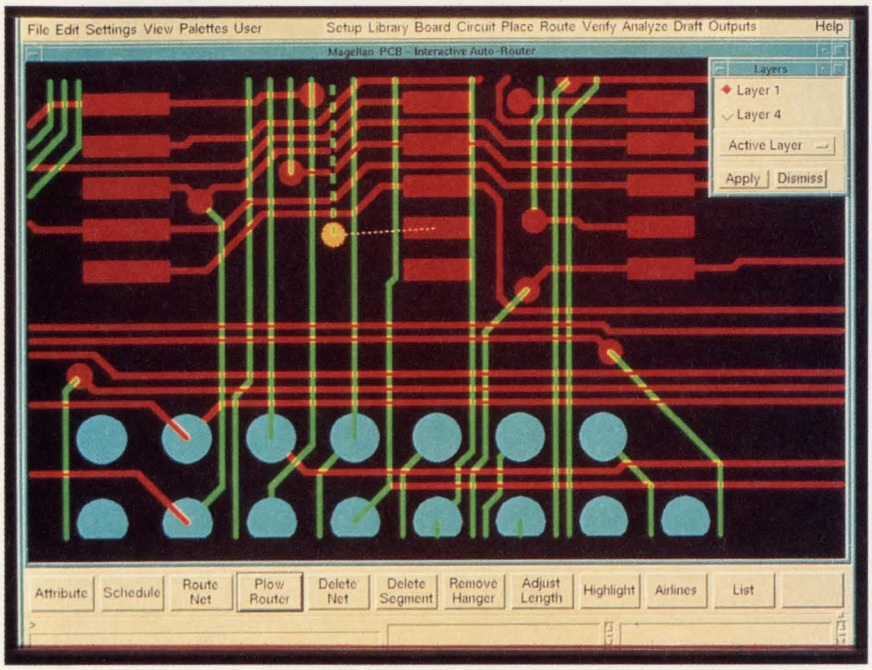
PCB routers keep up with tougher design constraints

Mike Donlin, Senior Editor



In this screen shot of the Dazix auto-interactive router in action, the dotted green line shows a trace routing path passing over trace obstructions (red lines) with a yellow dot where the system would place a via. The yellow dotted line indicates the remainder of the path to be connected. This information lets you make informed choices for manual routing of problem traces.

In the complex realm of PCB design, the debate about which is better, engineer or autorouter, has been going on for at least 20 years. EDA vendors have long held that using the power of the computer to lay traces on a board is worth the cost of the tool, while many board designers claim that automatic tools are inefficient and can increase the price of a board.

"There are a lot of technology advances that are making autorouters a necessity," says Keith Felton, senior product manager in the CAD group at Racal-Redac (Mahwah, NJ). "High-speed signal integrity control, advances in packaging and shorter time allowances for engineering changes are all making the task of routing a board increasingly difficult. An auto-interactive router is the best tool to meet these challenges, because it combines the computer's ability to keep track of design rules with the engineer's expertise to produce an efficient, manufacturable PCB."

Finding the right angle

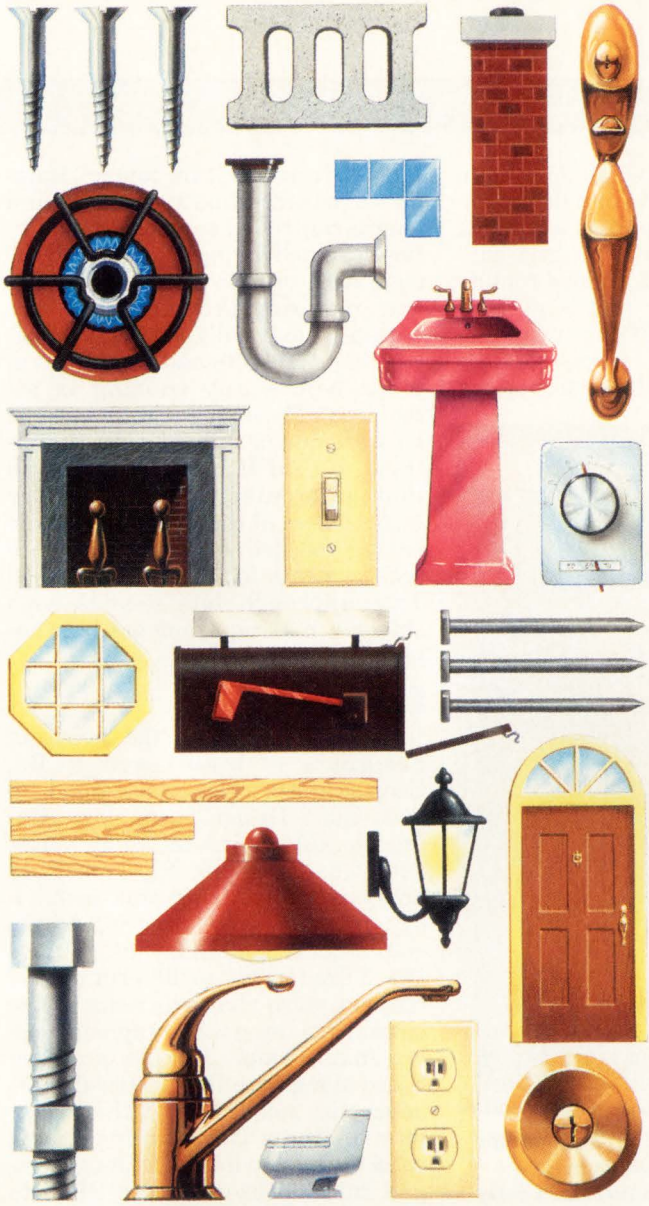
Racal-Redac's latest entry in the router arena is a graphical, auto-interactive router built around the architecture of its gridless Bloodhound autorouter. The new release, 3.0, features angle-free routing and graphical min/max delay constraints routing with real-time analysis capabilities. "There's a trend toward using new packaging techniques, such as offset pin layout, to reduce device size and maximize lead-outs," Felton explains. "The increased use of ASICs, FPGAs and PALs has caused a dramatic increase in device pin counts. This, coupled with the physical compaction of systems on boards, has led to a huge rise in data I/O channels and the need to accommodate these I/Os in connectors of ever decreasing size. To achieve this density, an offset pin layout technique is often used for board layer minimization, but it means that traditional orthogonal routing is no longer practical."

According to Racal-Redac, most routers have gotten by with a 45° routing capability, but today's latest devices need 30°, 60° or even angle-free routing features. To meet the needs of PCB designs with advanced device packages, Racal-Redac's router will automatically switch to angle-free routing mode whenever required.

As impressive as such router features are, designers are still reluctant to turn routing completely over to a computer. Interactivity, therefore, is essential, and most EDA vendors provide some level of editing capability in their routers. Racal-Redac's router provides this interactivity, while keeping design rules firmly in the design. Its Route Editor provides min/max delay constraints routing while you edit the route. This feature immediately identifies critical signals that have propagation delay constraints and lets you visualize the boundaries of the constraints with a pair of octagons. To obey the constraints, you have to construct a route within the boundaries of the largest octagon, but outside the boundaries of the smaller octagon. The display shows you the required target constraint values and the router's current value status.

Reconciling differences

Because interactivity is high on the wish list of so many designers, it seems an obvious feature for EDA vendors to provide. Unfortunately, it's a feature that's easier described than provided. "Most routers that have editing capabilities use separate algorithms for the automatic batch routing and the interactive editing portions of the software," says Walter Katz, director of advanced routing at Dazix (Huntsville, AL). "This limits the interactive capabilities rather severely. If you want to stitch in a path, for instance, you have to specify all the vertices along the way, which can be time-consuming. Even then the router might not have the push-and-shove or rip-up-and-retry features that the batch router would have, so the trace might meander around the board."



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Integrating the autorouter with the editor is difficult because the batch router's algorithms are usually an established product in an EDA vendor's suite. "Trying to tie a new algorithm, such as one for interactive capabilities, into a router that's been around for a while takes quite of bit of expertise," Katz points out. "And if you're a tool vendor who wants to unveil interactive features in a timely fashion, you're probably going to find it easier to just write a separate algorithm."

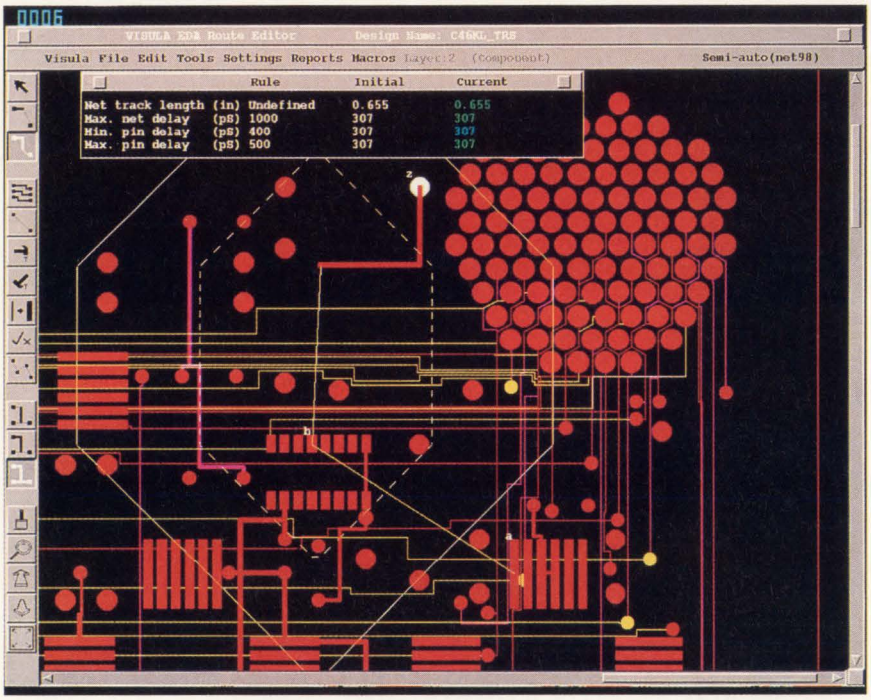
The Dazix auto-interactive router lets you route by component, window, net, or "from-to" points. High-speed design rules are automatically obeyed by the tool when routing nets with scheduling, min/max trace length and matched length requirements, as well as differential pair constraints and stub length controls.

Avoiding gridlock

Although the Dazix router is targeted at complex, high-speed PCB designs, its competitors point out that, because the Dazix tool is built on a grid, it will take an inordinate amount of memory to handle the numerous traces and pads of a complex PCB. Though innovative grid-handling techniques let gridded routers such as the Dazix tool work with mixed-technology PCBs, some vendors claim that only a truly gridless router has the flexibility and memory efficiency to handle complex, fine-pitch architectures.

"True gridless routing requires less memory because it doesn't use as many reference points to place a trace," says Shelley Boose, director of marketing at Cooper and Chyan Technologies (Cupertino, CA). "Our router uses a shape-based approach which looks at a line across the screen as a rectangle that's so many millimeters wide by so many millimeters long. While a gridded router sees hundreds of points on a line, we treat it as one shape. The advantage of this approach is that it provides the flexibility to deal with mixed-trace pin spacings, while using far less memory than gridded routers do."

Cooper and Chyan's newest router, the Specctra SP50, features table-driven crosstalk control, automatic balanced-pair routing and length-controlled routing—capabilities designed for high-speed PCB design. According to Boose, "Sensitive nets requiring ground shields are normally manually routed to specific requirements and then fixed in place before any routing is attempted. These fixed nets become barriers during autorouting. In contrast, the SP50 uses a technique that autoroutes the net and the guard traces at the same time, while letting you define special clearance requirements for the shielded nets. This approach lets boards with shielded net requirements be completely autorouted."



In this photo of Racal-Redac's Route Editor 3.0, twin graphical octagons highlight the minimum and maximum delay constraints for critical nets. To stay within these constraints, you construct a route staying outside the inner octagon (minimum delay constraint), but staying inside the boundary of the outer octagon (maximum delay constraint).

Avoiding noise

In a further bow to the needs of designers of high-speed PCBs, Cooper and Chyan has teamed up with Quad Design Technology (Camarillo, CA) to link the SP50 router with Quad Design's XTK crosstalk analysis tools. Using this technology, crosstalk prevention is a three-step process. Before layout, you use the XTK toolset to determine the coupled noise characteristics of the circuit. This step is accomplished using small sample circuits on a test board along with the electrical characteristics needed by XTK to perform analysis. The resulting data is used to develop a table of length-vs-gap rules utilized by the SP50 to control parallelism.

After developing the rules, you autoroute the circuit with the SP50, which can follow the tabular parallelism rules. Once autorouting is completed, use the XTK tools to take measurements of crosstalk in the finished circuit. This final check assures you that the model used by the router agrees with the electrical analysis provided by XTK. If discrepancies are found, you can change the route with the interactive editor. ■

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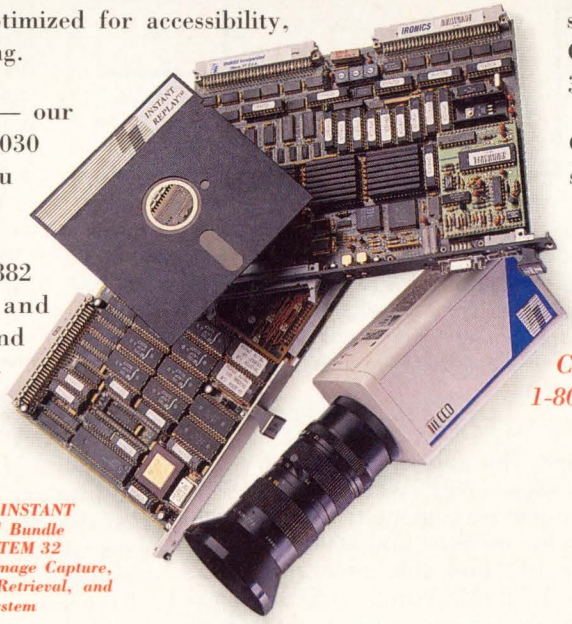

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CIRCLE NO. 72

SOFTWARE & DEVELOPMENT TOOLS

Tools help move applications between different GUIs

Tom Williams, Senior Editor

With the proliferation of graphical user interfaces (GUIs) for many different platforms and operating systems, it would be easy to despair of solving the problem of porting applications. As it turns out, the application programming interfaces (APIs) of GUIs tie them very closely to the display functions of the system, as well as to almost all the other OS services. Since the application gets to all the system services via the API, it should be possible to move applications among well-behaved GUIs via their supposedly stable APIs.

Of course, nothing is ever quite as simple as it sounds, since different GUIs have different capabilities, looks and feels. But because today's GUIs are well-defined, vendors of application porting utilities are finding ways to move almost the full capability of an application developed on one platform, OS or GUI to another.

Two approaches

Two approaches to the problem are presented by Bristol Technology (Ridgefield, CT) and XVT Software (Boulder, CO), each solution appealing to a different class of software developer. Bristol's approach takes the application calls to the Microsoft (MS) Windows API and translates them into calls to the OSF Motif flavor of X Windows/Unix. XVT, on the other hand, provides an API at a more abstract level. The developer writes code that can later be linked to facilities letting it run under six different APIs, including those for Macintosh, Open Look, OS-2, OSF Motif, and Windows.

A system using the OSF Motif flavor of X Windows has a layered API in which the application makes calls to different levels for different services. Window management calls go to the Motif and Xtool layers, while display functions use the Xlib library of graphics primitives. System services such as file I/O call the Libc client library layer, which interfaces to Unix.

In MS Windows, on the other hand, the application calls a single Windows API, which provides all window management and graphical device services and routes calls for file I/O into the underlying DOS level. The MS Windows API also provides OS services not available from DOS, such as memory management and task switching, as well as advanced intertask communications such as dynamic data exchange (DDE) and object linking and embedding (OLE).

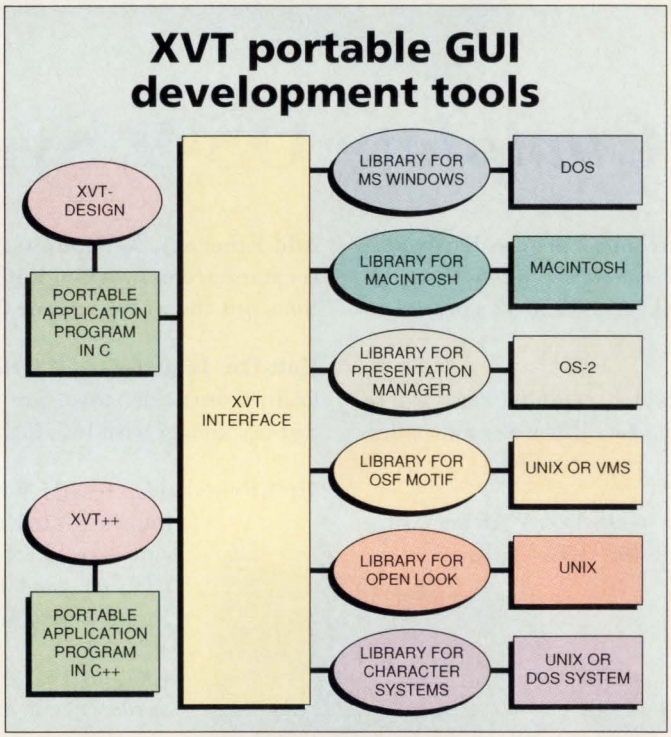
Bristol's Wind/U library consists of window manager functions, graphical device interface (GDI) functions and system services functions. When the MS Windows application is recompiled and linked with the Wind/U library, the latter maps MS Windows function calls to the equivalent Motif and X Windows calls.

Windows vs. Motif

According to Ken Blackwell, Bristol's chief technical officer, there's a disparity between the functionality of MS Windows and Motif. "In GUI respects," he says, "MS Windows has much more functionality. It's much richer." Of course, as an operating system the underlying Unix is much more powerful than either DOS or DOS combined with Windows. But for the independent software vendor moving an MS Windows application to Motif, the underlying OS levels "aren't much of an issue, because the API defines the functionality," according to Blackwell.

Certain Windows features not supported by Motif, such as combo boxes, have been added using widgets from the Xtool layer of X Windows. MS Windows DDE is mapped to Unix remote procedure calls, and Bristol's Blackwell says that OLE will be supported in an upcoming release. In addition, the Wind/U package adds a printer support feature that can be used by all the applications on the system.

The MS Windows GDI deals with graphic devices including printers and plotters, as well as display devices, and is, therefore, more general than the Xlib layer. A module called Xprinter has been added at the Xlib level—below the part of Wind/U that maps GDI calls to the



The XVT GUI Portability Kit lets developers write C or C++ programs to XVT's abstract GUI level. GUI, OS and hardware-specific libraries translate the XVT GUI calls to the characteristics of their respective environments. For C developers, the XVT-Design package lets you lay out windows, menus and dialog boxes in graphic form and produce the abstract API code for later conversion to the environment of choice.

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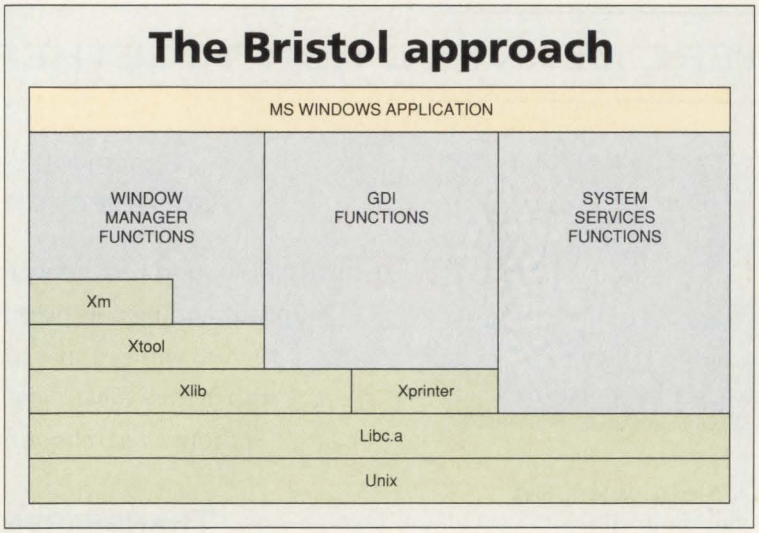

The Wind/U library from Bristol Technology maps application calls to the MS Windows API to the different API layers associated with the OSF Motif version of X Windows. System services such as file I/O, which MS Windows maps to DOS functions, are sent to the client library, which interfaces X Windows to Unix. Printer support is added to X Windows with Xprinter, which lets the MS Windows GDI write directly to a Postscript printer.

display via Xlib. Xprinter can accept Xlib calls from either a converted Windows application or an X Windows application; it supports Postscript printers. Support for the Hewlett-Packard PCL printer language will be added soon. "We will also license this portion directly to X Windows developers," says Blackwell, because printer support under X Windows is still pretty much a "roll-your-own" proposition.

Taking the high road

To write a single application and have it run on a variety of APIs, OSs and hardware platforms creates a different set of problems from porting an existing MS Windows application to the OSF Motif version of X Windows. First, you don't start out with existing code. The XVT Portability Toolkit from XVT Software is designed to offer you a thin API at an abstract level. Writing an application to this API lets the same application be characterized via libraries linked for the different GUI environments.

According to XVT president Marc Rochkind, "XVT is an invention of a new API intended to be higher level and divorced from any bias toward one toolkit or another, much the same way a programming language should be divorced from bias toward any machine." For instance, the XVT API doesn't draw and operate its own scroll bars. It declares an interface to the native scroll bar implementation. Similarly, you don't cre-

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ate windows with XVT by laboriously calculating coordinates; you simply create a window with a single call. The environment-specific library provides the actual window code.

For those of you who want to visualize what you're doing graphically, XVT provides a package called XVT-Design that lets you lay out windows, dialog boxes and other items interactively using a mouse. The completed XVT design then generates C code that calls the XVT API functions. That code is merged with the other application code, which can then be characterized for the specific environments in the same manner as code written directly for the XVT API.

A short-term solution

XVT's Rochkind sees his company's goals as different from those of Bristol. "The MS Windows API is, we think, a temporary solution, because it's not at a high enough level to represent a long-term API that can respond to changes in the technology, such as object-oriented APIs," he says. Bristol's approach is to aid developers who have existing applications written in MS Windows and who want to move them to the OSF Motif environment. It also helps those who have been supporting two versions of the source code and who now only have to maintain one version with links to the two environments.

Porting to environments other than OSF Motif will create different levels of difficulty for the Bristol approach. Moving to Open Look mostly involves changes in the part of the library that talks to the Motif layer. Moving to other OSs, such as a Macintosh's, would involve far more environment-specific changes. Bristol probably won't move in that direction, because Microsoft itself is reported to be working on a way to move MS Windows applications to the Macintosh.

Still, GUIs as well as OSs are not going to stand still. Taligent from Apple/IBM can be expected to have an impact, and more object-oriented GUIs will doubtless appear. Developers are going to need tools such as those from Bristol and XVT to save their enormous investment in existing code and to let them concentrate on the functions of their applications while being able to run in these different environments. ■

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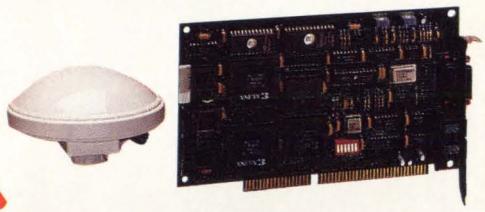

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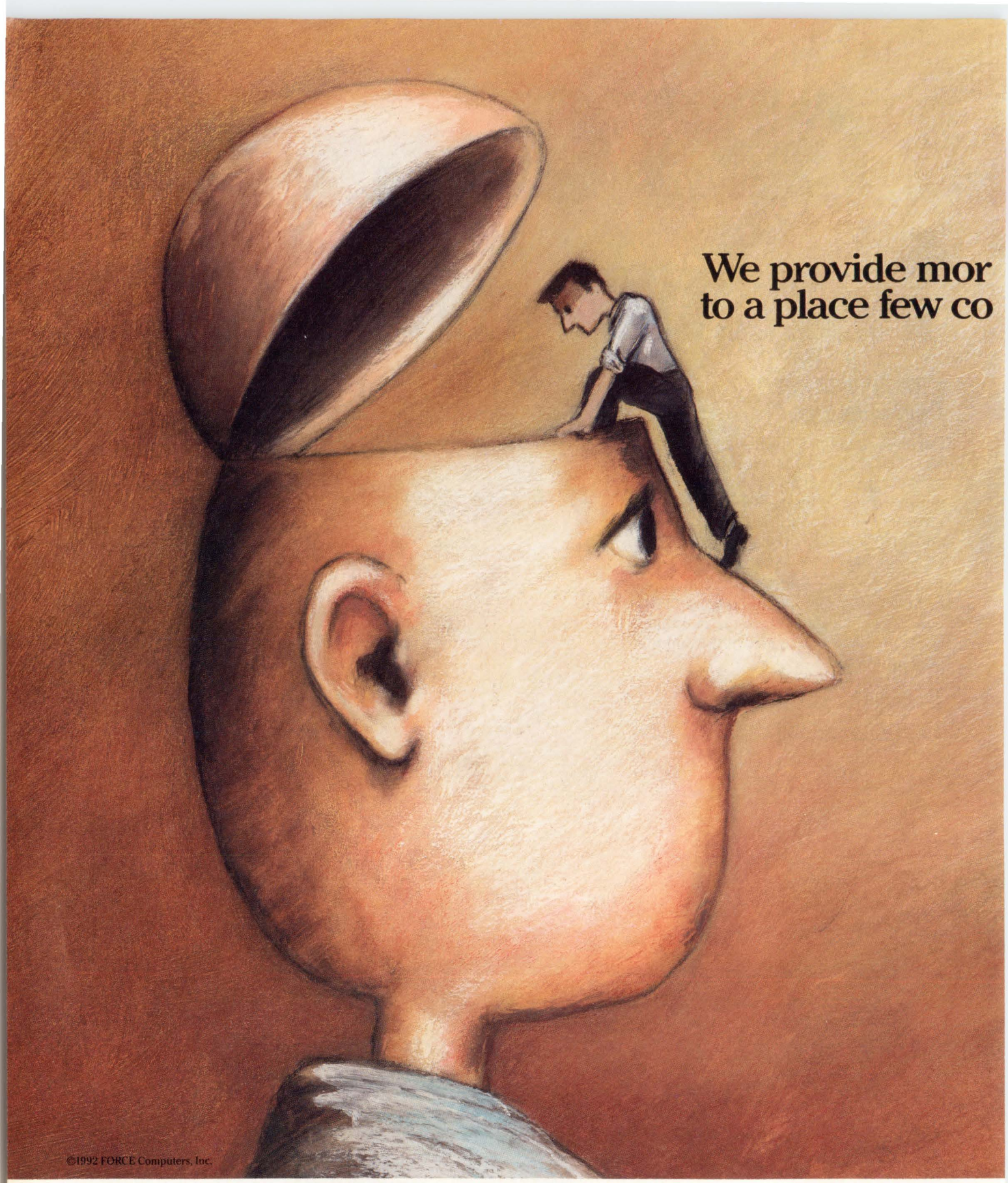
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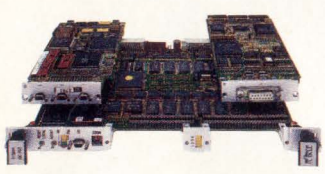
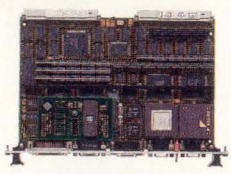

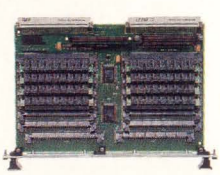

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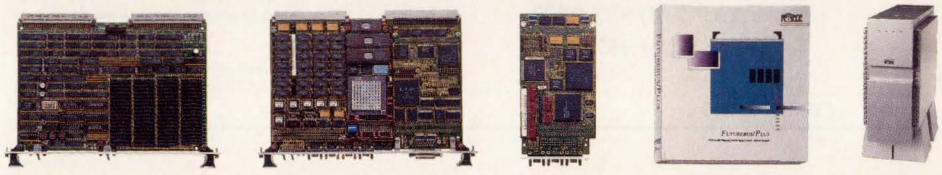

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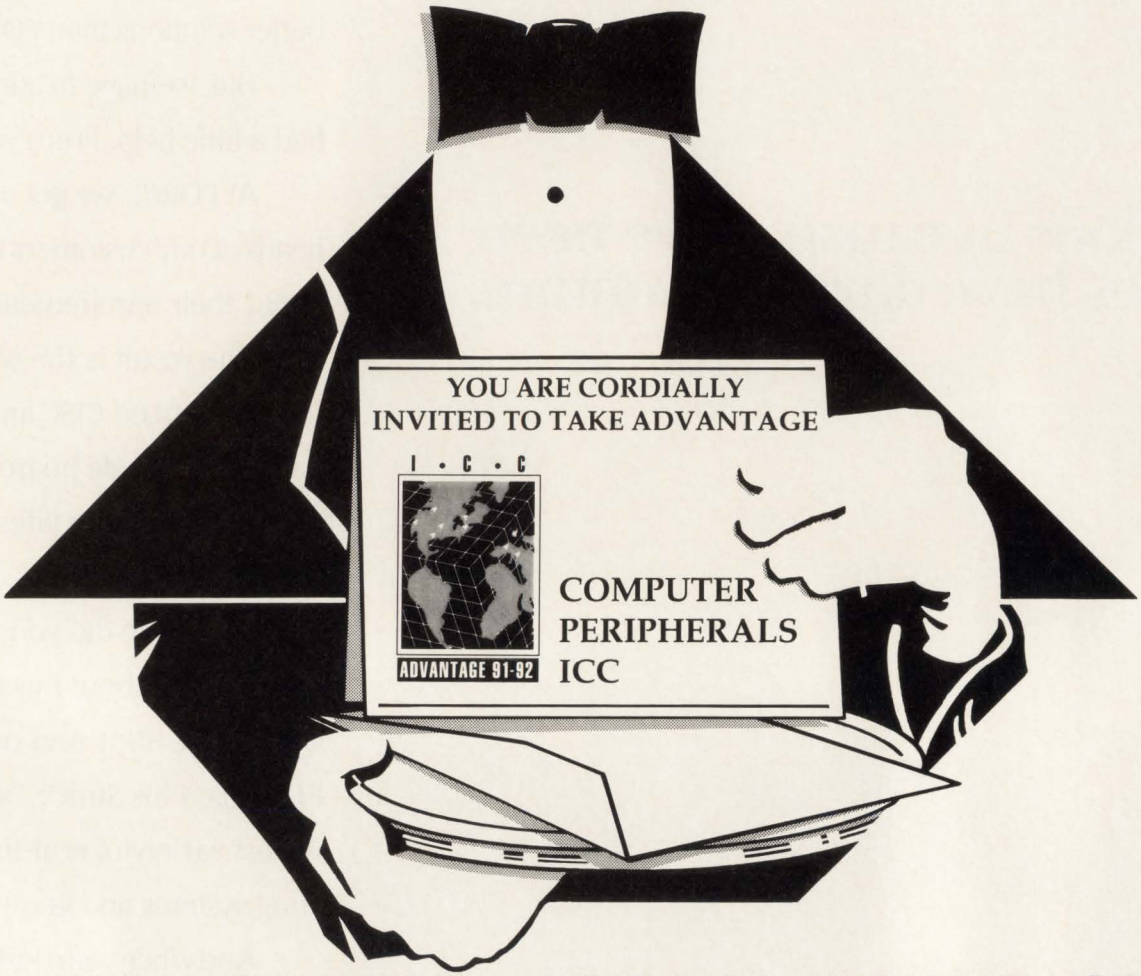

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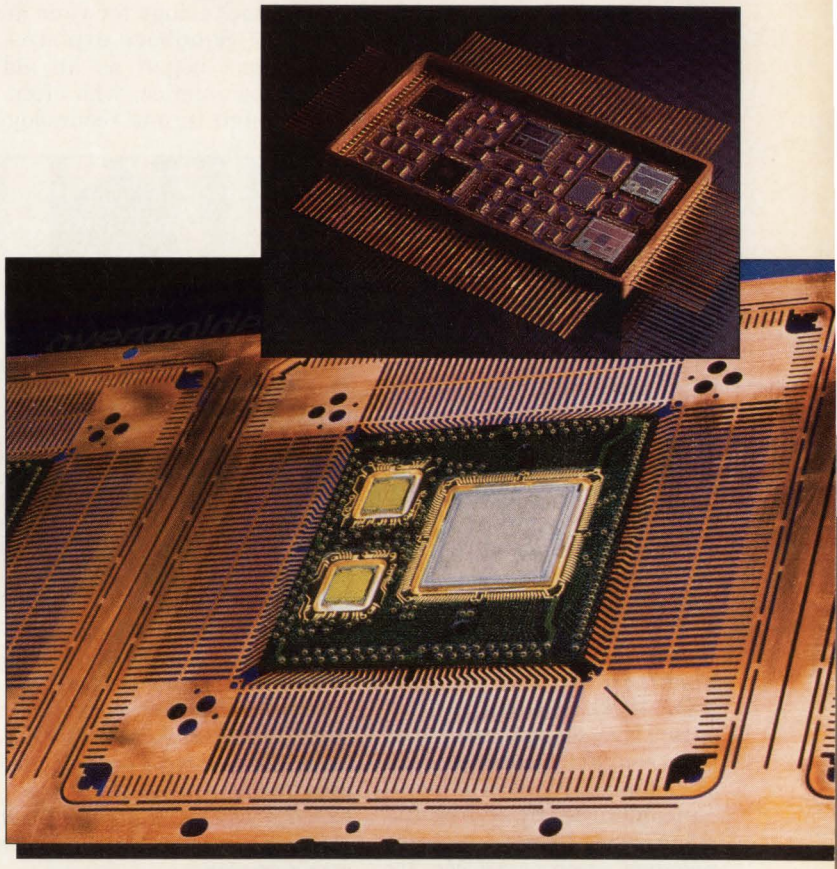
CIRCLE NO. 36

MCMs push design and test tools to the limit

Do multichip modules represent an exciting new technology or an exotic curiosity? Until the vexing problems of testability and yield are ironed out, few people are willing to hazard an answer to this question.

Mike Donlin
Senior Editor



MCMs can run the gamut from relatively simple devices mounted on low-cost substrates to complex, multilayer systems on silicon. The MCM in the foreground is a low-cost QFP module with the lead frame built into the PCB substrate. The MCM in the inset is a complex digital signal processing device which uses a nine-layer, thick-film substrate to interconnect 44 IC dies with 1,850 wire bonds.

If you're a designer looking for a next-generation technology to solve your system performance problems, multichip modules (MCMs) are either the answer to your prayers or a Pandora's box of design, manufacturing and test problems. The idea of mounting bare dies on a substrate seems like the solution to interconnect delays that slow a system's performance, but wary designers worry that the cost of an MCM could outweigh its benefits, particularly when you consider the high cost of prototyping, the difficulty of testing and the possibility of low yields. Design tool vendors and test companies have been releasing products to address these concerns, but an evolving technology such as MCMs dictates that no tool can have all the answers at once. This means that costly errors await designers who think of MCMs as warmed-over ASICs, tiny PCBs or hybrids.

At first glance, MCMs appear to be an extension of ASIC, PCB and hybrid technologies—particularly of hybrids, which have been around for more than 30 years. But a closer look reveals that MCMs use different substrate and interconnect materials and introduce difficulties in package design, thermal management, signal integrity, testability, and ultimately cost which are far more complicated than the problems raised by a traditional hybrid device. The burden of helping designers solve these problems has fallen on EDA vendors, who've been busy adapting existing tools and developing new ones to solve the unique problems caused by MCMs. These tools can't come soon enough to engineers who are wondering whether MCMs are feasible for their designs.

"Every time a new technology comes along, there's the usual rush to implement it and the usual headaches for early adopters," says Don Kuk, director of advanced packaging at Dazix (Huntsville, AL). "It's reminiscent of when designers jumped on the surface-mount bandwagon a few years ago and soon found that implementing it could be more trouble than it was

worth. It's the same with MCMs. People embrace exotic, high-performance technologies before they realize the pitfalls and often blame the EDA industry for not being there to support them. I'm concerned that a mad rush to use a technology prematurely can ultimately do more harm than good. Our competitors overseas are taking a more conservative approach, using low-cost, laminated substrates while we're pursuing thin-film and silicon technologies that are only applicable for about one to two percent of the design community." Caveats such as this bring up the question of exactly when to adopt a next-generation technology, as opposed to a tried-and-true ASIC or a densely packed PCB approach.

Fortunately, there are major efforts under way to help you decide when MCM technology is appropriate for your designs. One such program, the Multichip Systems Design Advisor (MSDA), has just begun at the Microelectronics and Computer Technology Corporation (MCC—Austin, TX). MCC is a cooperative enterprise whose mission is to strengthen and sustain the competitiveness of member companies by addressing R&D issues in evolving technologies, such as MCMs. Its members include a diverse group of companies from the aerospace, computer, EDA, electronics, and manufacturing industries. The MSDA project, instituted at the beginning of this year, focuses on providing the CAE tools needed to design and manufacture multichip systems. The tools developed under the project will provide designers, who may not necessarily be packaging and test experts, with the mechanisms for performing technology trade-off assessment while satisfying test requirements from the system down to the chip level.

"This project doesn't aim to reinvent existing design tools, but to fill gaps where tools are presently not available," says Peter Sandborn, senior member of the technical staff at MCC and MSDA project manager. "The idea is to help people narrow the playing field when they're making technology decisions. The MSDA tool will collect information about design choices, bonding methods, technical design rules, and packaging methods, and then give an assessment based on performance, cost, thermal data, routability, and delays on critical nets. This will give you the ability to perform 'what-if' analyses and choose the appropriate technology for your design."

Sandborn explains that the project began as an aid for member companies, who often started a design in one technology only to find out that another would have been better suited to the task. "It's hard to do early analysis with existing point tools because they're too detailed," Sandborn points out. "So we're developing a tool that will act as an advisor, with the combined expertise of design, packaging, test, and manufacturing engineers."

Members of the Dazix/Intergraph design team, Tom Ponder (left), design engineer; Don Kuk (center), director of advanced packaging; and Wade Patterson (right), director of advanced electronic design, review a completed MCM-L design project. "I think the next generation of MCM tools will focus on tight integration of design disciplines throughout a project's cycle," says Kuk. "That suite would ideally take in constraints on the front end and apply them throughout layout and routing with good ties to manufacturing

Because MCMs demand a tight integration of tools and expertise from so many different disciplines, EDA vendors are touting the advantages of concurrent engineering more than ever. An MCM must have input from everyone in the design cycle—from concept to manufacturing—or else an expensive prototype won't work. Debug and repair are a risky proposition because of the delicate nature of MCMs, so the burden of getting a design right the first time looms large in MCM development.

Another fledgling program designed to bring various design disciplines together is the recently announced Technical Alliance for Multichip Engineering (Tame) initiated by Harris EDA (Fishers, NY). The Tame program is an alliance of companies that offer products and services key to the use of MCM technology. "Tame is obviously aimed at promoting MCM designs," says Tony Mazzullo, director of product marketing at Harris. "We're looking to provide access to services such as design software, technology consulting, design service bureaus, university research organizations, fabrication companies, semiconductor suppliers, and test service companies. Some people have asked us how this effort is different from what's going on over at MCC. While MCC is a worthwhile organization, they're not aimed solely at promoting MCMs. And MCC demands some pretty hefty dues from member companies. Tame is free for qualified members."

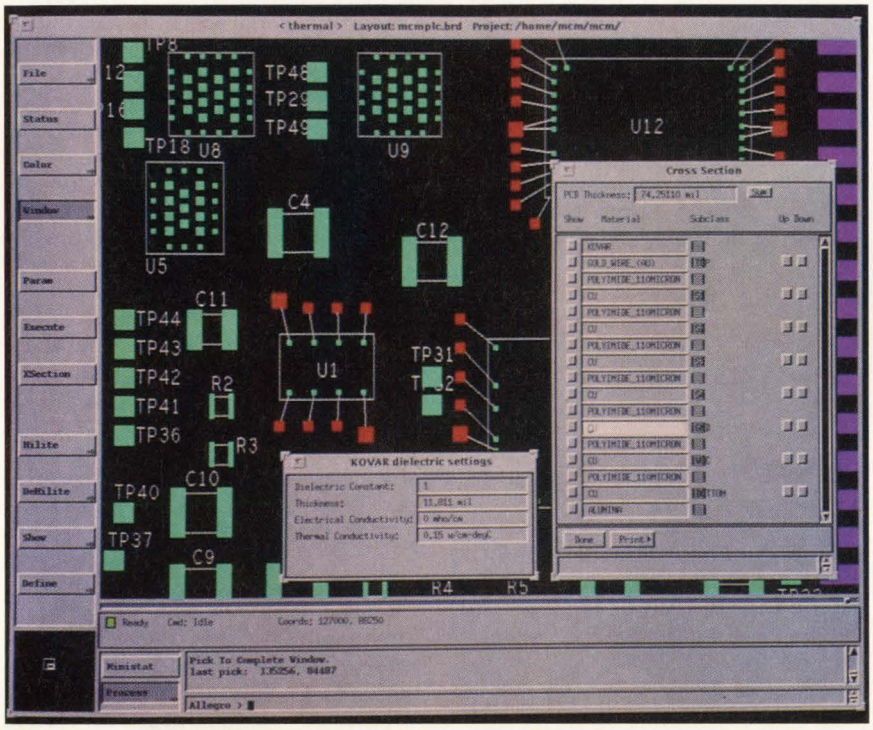
If there's one thing MSDA and Tame have in common, it's the idea that emerging technologies require cooperation from companies in previously separate disciplines. "MCM design has to be a collaborative effort," says Frank Boyle, product marketing manager for MCM design tools at Cadence Design Systems (San Jose, CA). "The task is going to demand cooperation between EDA vendors, silicon houses, MCM foundries, and customers, or costly mistakes will be made."

Choosing the best tool

Perhaps the most significant things to consider when approaching an MCM design are thermal management, testability and manufacturability. The EDA vendors who have unveiled MCM tool suites have at least partial elements of these three disciplines embedded in their tools. Most suites are also adaptations of existing products—either IC, PCB or hybrid tools. Many designers are partial to PCB tools because they produce designs that are correct by construction—the interconnect is driven from the schematic or netlist and if all connections are routed, the design is correct. But PCB tools

don't possess the necessary routing rules that are unique to MCMs and must be modified to work properly.

"Many PCB systems are still using outdated Lee algorithms," says Pam Russ, applications engineering director at Racal-Redac (Mahwah, NJ). "These are fixed-cell-type rules that have already reached their limits in surface-mount technology. Routers using these algorithms are gridded and each time the routing grid is made smaller, the memory required to store the grid locations increases exponentially."



Cadence's Allegro-MCM tool lets you define and store material characteristics and provides a basis for all subsequent thermal and signal integrity analysis. In this photo, the selection menu in the window on the right lets you choose a material for substrate or interconnect and displays its associated dielectric data. Replacing one set of materials with another gives you "what-if" analysis capabilities prior to beginning a design.

In addition to solving the routability problems that MCMs generate, router vendors have to provide rules-driven tools or the routed device might be unmanufacturable. And because the design rules for MCMs are different from PCBs, existing routers have to be modified. "It took us months to get a router to work on our designs," says Bruce McWilliams, president of nCHIP (San Jose, CA), an MCM supplier. "Even though many commercially available routers could handle the task of laying out the interconnect, they didn't understand our unique design rules. For instance, most routers are set up for an arbitrary number of layers and ask you if you want to add layers when things get dense. In our thin-film designs, you can route almost anything on two layers. But in MCM technology, the router can't route under bond pads or arbitrarily jog over another line. When you have a circuit running at a few hundred megahertz, a router simply can't handle all the design rules."

Because the rules for MCMs are complex, EDA vendors will undoubtedly tackle pertinent problems at each stage of the design process. Rules-driven layout, for instance, can ease the burden on routing tools by placing components in locations that take routability and, ultimately, manufacturability into account.

In Racal-Redac's Visula tool suite, for example, the automatic and interactive placement routines adhere to a number of rules that can be defined early in the design process. The basic algorithm is tree-based and considers every pin on the net for placement, as opposed to a connection-based algorithm that only looks at point-to-point connections.

Though the rules-driven tools can lend valuable assistance to a designer, it's important to keep the tools interactive or designers will be reluctant to use them. "Auto-interactive placement tools have the power of the automatic tools but give control to the layout designer," says Racal-Redac's Russ. "The tools can consider, for instance, thermal and mechanical constraints during placement."

These mechanical or manufacturing constraints aren't usually built into most EDA suites, but tool vendors are adopting them for their MCM software because they're a critical part of design and layout. Dazix's tool suite, MCM Engineer, supports the industry-standard manufacturing data format, GDSII. With MCM Engineer, you specify which elements are to appear on a given mask and the system generates the required GDSII data files. The software also provides a mechanism that lets you read data into MCM Engineer format, so old designs can be loaded and modified.

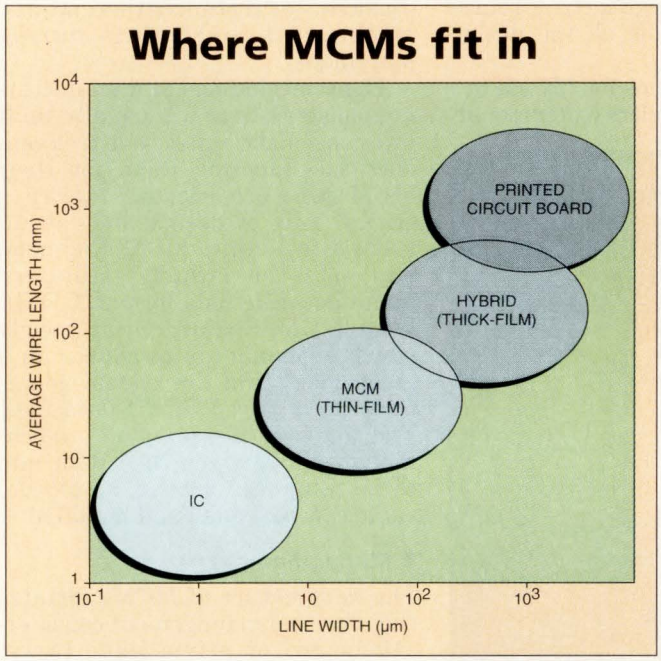
Managing heat

The very nature of MCMs dictates that thermal management considerations are of prime importance. After all, the rationale behind adopting an MCM design strategy is to increase performance. This necessitates packing components close together, which in turn makes thermal management a key part of a design. Because silicon will be connected directly to a substrate, many of the traditional ways of dealing with excess heat, such as mechanical heatsinks, will be impossible or unwieldy to use. "We do extensive thermal analysis during layout," says Bill Sullivan, MCM design and development manager at AT&T (North Andover, MA). "We try to determine if we can put the silicon on a dielectric layer or on a substrate, or cut a hole in the substrate, or even design in a heatsink."

Because of the importance of thermal management, most MCM tool suites have temperature evaluation software that gives thermal maps of components after they've been placed in the design. These tools, whether proprietary or purchased from companies such as Pacific Numerix (La Jolla, CA), usually use a finite-element method to model heat transfer across components. MCM Station from Mentor Graphics (Wilsonville, OR), for example, uses

a tool called AutoTherm to analyze thermal behavior.

When modeling forced convection with AutoTherm, you define a flow boundary around an MCM and specify any number of flow inlets (with inlet air speed and temperature) and flow outlets. The tool then calculates convection coefficients for every point on a substrate, using the local flow velocity and standard data or any custom formula you specify.



Average interconnect line widths of MCMs span the gap from one micron for ICs to 1,000 microns for thick-film hybrids and PCBs. This illustration gives a comparison between average wire lengths and line widths for various technologies.

Simulating reality

All of these tools are aimed at one thing—trying to predict the behavior of an MCM before you have to make it. Because MCMs are expensive and difficult to repair, simulation of electrical and physical behavior is particularly important. "Right now, most simulation tools give pretty good results, but they're cumbersome to use," says nCHIP's McWilliams. "The big problem is trying to simulate an MCM as a component. To do that you need a behavioral model of every chip and have to merge that with interconnect models and simulate everything as one function. As far as I know, no EDA vendor can do that. For the present, we do some Spice-level and some behavioral-level simulation and some transmission line modeling to predict what's going to happen. Integrating all of that together is difficult."

While EDA vendors are wrestling with integration problems that prohibit seamless simulation, designers will have to use the "divide-and-conquer" approach to solve their problems. Fortunately, there are point tools which address the unique problems of MCM designs, particularly in the field of transmission line analysis.

"The key difference in MCM design is the small dimensions of the wires involved," says Larry Rubin, president of Quad Design Technology (Camarillo, CA). "A lot of these wires are extremely fine in width and height, which means their cross-sections are small. This means you have higher ohmic loss and, at high frequencies, skin effects loss. In addition, there's more potential for crosstalk between layers, so you need to look at the three-dimensional aspects of transmission line modeling." Quad Design's 3-D field solver analyzes crossovers, corners and connectors that can't be analyzed by traditional 2-D field-solver tools.

In addition to transmission line effects created by tightly packed circuits, you must also pay closer attention to power and ground relationships in the close confines of MCM topology. A tool called PG-Plane from OEA International (Santa Clara, CA) has just been released that promises to help you deal with these effects. The tool is a 3-D inductance simulator for analyzing power and ground bounce due to simultaneous switching noise on MCMs, PGAs and other dense devices.

"Simple methods of calculating or measuring effective inductances won't give the correct solution to this problem," says Ersed Akcasu, president of OEA, "because the values change and depend on which outputs are switching at any one time in the circuit." According to Akcasu, PG-Plane gives you the Spice deck to study the problem under a variety of simultaneous switching conditions.

Models are key

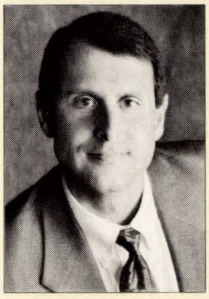
Though there's little disagreement about the importance of simulation in MCM design, there's a lot of controversy about how and where to get the device models to drive that simulation. Silicon vendors are the logical suppliers of such models, but getting them to cooperate is an uphill struggle. Traditionally, silicon vendors don't provide device models or test vectors for bare dies. Not only would such data give away proprietary process information, but it also wouldn't be terribly useful for most of the design community, which uses packaged devices. This is bad news for MCM designers.

"Getting bare die test vectors from silicon vendors is like pulling teeth," says Vern Little, product marketing manager at Pacific Microelectronics Centre (Burnaby, British Columbia), an IC and MCM supplier. "Some companies won't supply information on test vectors, some won't give it for I/O pads or interconnect. We've found the formula for success is controlling everything ourselves and writing our own models. You have to get to know the silicon vendors who will help you out. Anyone who thinks they can buy a device from company A, another from company B and a third from company C and string them all together is going to end up with an MCM that doesn't work."

To be fair to silicon vendors, it's important to note that testing bare dies is a tricky proposition. Most silicon manufacturers are set up to do a low-speed test on wafers, categorize them according to spec and then do a full-speed test on the packaged die. Testing bare dies is slow, difficult and potentially harmful to the silicon, and most silicon vendors are reluctant to invest the resources necessary to provide tested die or test information because the market is still so small.

"Some companies use mechanical probes to test their silicon," says

Design tools: necessary, but not sufficient



EDA suppliers have made great strides recently toward providing capable toolsets for MCM design. When nCHIP made its initial design tool purchases three years ago, comprehensive design systems for MCMs weren't available. We had to patch together a variety of tools originally developed for different aspects of IC and PCB design. Building the system involved significant tuning of the tools, as well as writing many of our own interfaces and translators.

Since then, MCM-focused design systems have become available, making it much easier to get started in MCM design. Tools are useful, however, only when they are working with good data, so data availability should be considered as early in the design cycle as EDA tool and MCM technology selection.

Data required

Design data—particularly data on the ICs—is always on a project's critical path at the start of a design. The impact that data gathering has on the overall design schedule can be highly dependent on the parties involved and the relationships that are established early in the program. Ideally, the module (or system) architect, the MCM supplier and the IC manufacturers will all take an active interest in the success of the product.

The IC data required for a good MCM design is more comprehensive than that required for most board or system designs. The usual data sheet information is needed, of course, as are logic and timing models. In addition, physical information on the bare die is needed (dimensions, bond pad locations and metallurgy), as well as accurate I/O driver characteristics. Such data always exists at the IC supplier, but it's not always simple to acquire.

We have found that IC suppliers are usually willing to provide the necessary information, but the data isn't typically available from published materials or even from the marketing person's desk drawer. Bare die sales aren't yet routine for most manufacturers, so the support infrastructure may not be in place. Suppliers must often do some legwork to figure out where the data is, and then sanitize it before release. Because of this, it's valuable to establish a good relationship with IC suppliers. Furthermore, bare die users need to understand that seemingly simple requests aren't always easy to respond to; patience and persistence must be carefully balanced.

Even the IC information that's published and available should be examined carefully. Items like logic models, testability information and power dissipation data assume added importance for chips that are to be used in MCMs. Because the die will be in a different and less accessible environment, good simulation and design-for-test techniques are critical. There's a tendency for modules to be overdesigned both electrically and thermally. If accurate information on the ICs is available and applied with good judgment, better-informed, more cost-effective design decisions can be made.

An example of the value of careful application of good data is a fast processor module we recently built for a systems customer. The MCM was going to be used in a desktop system, so audible noise restrictions limited the amount of airflow that could be used for cooling the module. A thermal calculation based on worst-case power consumption figures from the IC data sheets indicated that a thermally enhanced MCM package would be required to keep the chips reasonably cool. However, packaging the ICs in an MCM sharply reduces the interconnect capacitive load driven by the chip outputs. For CMOS designs, power dissipation is directly related to output loading. Further investigation showed that the actual MCM power would be substantially lower than the data sheet figures implied. As a result, it became clear that a less expensive package without thermal enhancements could easily meet the system requirement.

In the early stages of design, the IC data typically required is the most difficult information to obtain. But good information about the other MCM components, namely the substrate and the package, is also critical. That data is usually easily available from the MCM foundry, but early discussions about the content and format of data exchange are advisable. In many cases, electrical simulations of critical paths will be performed by both MCM buyer and foundry. To accommodate this, the foundry must be able to provide both finished simulator output and raw interconnect electrical characteristics in usable formats.

System requirements

A final, and typically neglected, category of data is in the realm of system requirements. A few examples are:

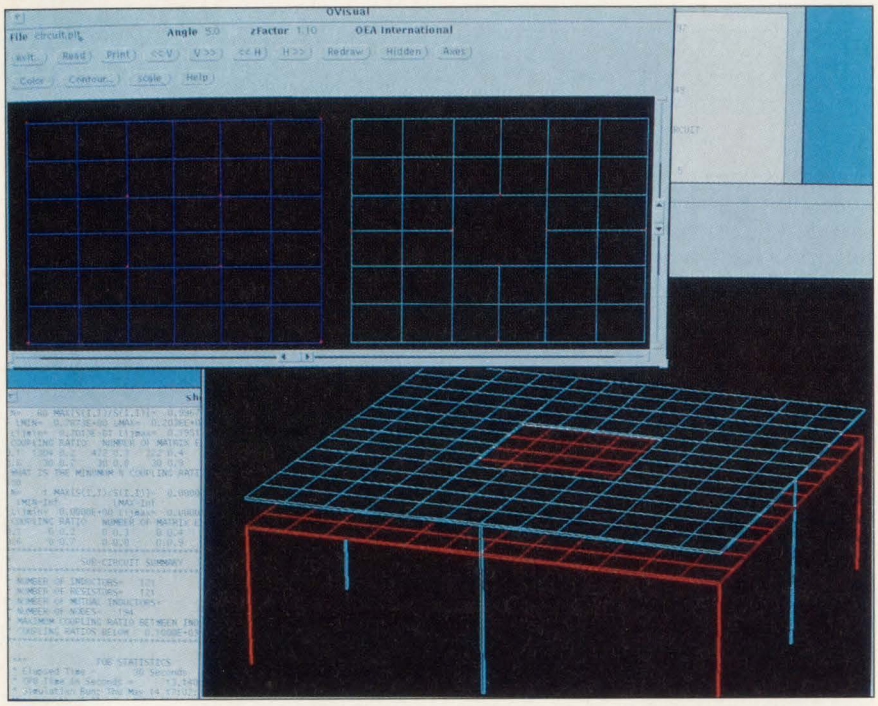
- detailed definition of the system's thermal environment (airflow, ambient temperature),
- maximum allowable crosstalk and ground bounce (noise margin budget), and
- mechanical envelope (module footprint and weight constraints).

Module designers can always strive for "best possible" if no absolute limits are available, but that can result in an overdesigned product that is more expensive and longer in development than necessary. If all the constraints can't be met, choices will have to be made; the choices will be better if trade-offs are made with specific goals in mind. The MCM supplier can often be helpful in assessing the relative importance of different issues in the overall design.

The general design process for an MCM is quite similar to the process used for ASIC design, although at a less mature stage of development. Designs usually start with a netlist, which is placed, routed and simulated before the design is signed off. After sign-off, masks are made, substrates are fabricated and prototypes are assembled. The concept is familiar to those experienced with ASIC design; the only difference is that the collection of macros or cells in an IC is replaced by a collection of ICs on a substrate.

As the market develops, MCM design will evolve from "ASIC-like, but more complicated" to "ASIC-like, but simpler." Die libraries with the information needed for MCM design will be available from IC manufacturers and third-party library vendors. Technology design kits will be supplied by MCM foundries for their products. EDA tools will handle MCM designs with ease, taking die, substrate, package, and system characteristics into account. And system and subsystem designers will consider MCMs as much a part of their toolkits as they do now with ASICs.

Stan Drobac, vice-president of products and services, nCHIP, San Jose, CA



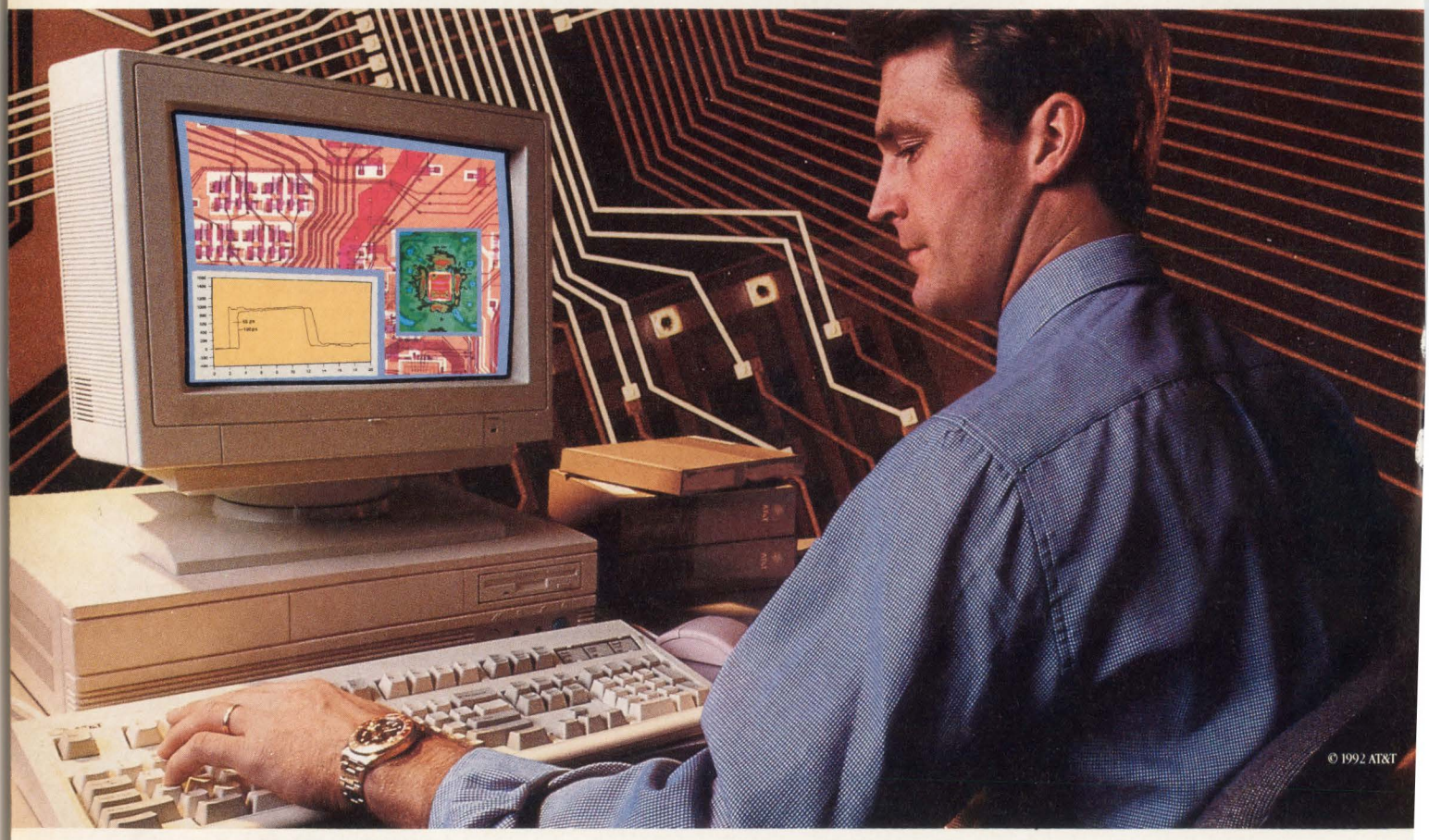
Because zero inductance for power and ground can't be assumed in high-speed circuits, full 3-D modeling of power and ground planes is required to predict simultaneous switching noise or ground bounce. This picture of the PG-Plane tool from OEA International shows both a profile and a 3-D view of a power and ground plane with pins connecting to the substrate.

Chris Talbot, product marketing manager at Schlumberger (San Jose, CA). "That method takes time—you can only test about one to 10 pads a second. Noninvasive methods like E-beam probers are much faster, anywhere from 100 to 1,000 pads a second. MCM designers can use that method to test the substrate, but then you have the problem of obtaining known good silicon."

Testability is actually a threefold problem. MCM designers need methods to test their substrates for connectivity faults. Then they need known good dies which have been tested by silicon vendors so they can be sure they're putting good parts on their substrates. Finally, they need a method to test the finished MCM. Representatives from silicon vendors, MCM fabs and EDA vendors have been wrestling with these problems over the last few months, trying to hammer out agreements and standards, but progress has been slow.

"It's a classic chicken-and-egg problem," says John Isaac, advanced packaging product manager at Mentor Graphics. "The industry

Breakthrough multichip modules



isn't going to go to high-volume, low-cost MCM production until it solves the test-and-rework problem. And they're not going to put the resources into solving those problems until there's a high demand for the answers. It's going to take a lot of cooperation among the various players to get production up to speed."

Until these issues are resolved, MCM designers will have to come up with creative ways to test their silicon and finished devices. "We've developed a lot of methods on our own," says Dick Pommer, product development at Litronics (Costa Mesa, CA), a PCB and MCM design firm. "We've had some luck with mechanical probes and we've developed a thin-film test head for the substrate. We've tried single-point capacitance probes, but haven't had good results. They can miss a pad or slide off and create shorts."

While all these problems are being ironed out, most designers are taking a wait-and-see approach to MCMs. Surely the technology is appealing. Squeezing more performance out of existing designs by eliminating packaging and interconnect constraints seems like an elegant way to overcome performance barriers. But the test and manufacturing obstacles are daunting.

Help is on the way in the form of test methodologies such as boundary scan and built-in self test (BIST). And there are at least two companies that are supplying tested silicon for MCM designs—Intel (Hillsboro, OR) and Micron Semiconductor (Boise, ID). But until more EDA vendors, silicon houses and MCM fab facilities get together, MCMs will remain a technical curiosity for all but the largest of system manufacturers.

"Right now MCMs are a big prototype exercise," says Mike Baglino, assembly and test manager at Teradyne (Boston, MA). "We don't know if the industry will begin to produce some less exotic MCMs, like two- or three-chip modules on a ceramic substrate, to get things started, or if MCM development will be slow until complicated devices get into production. It's all still very experimental, and no one's really sure how it will shake out." ■

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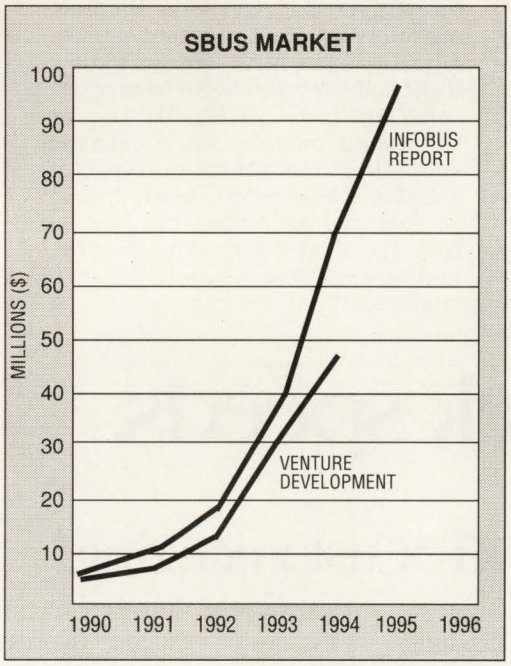

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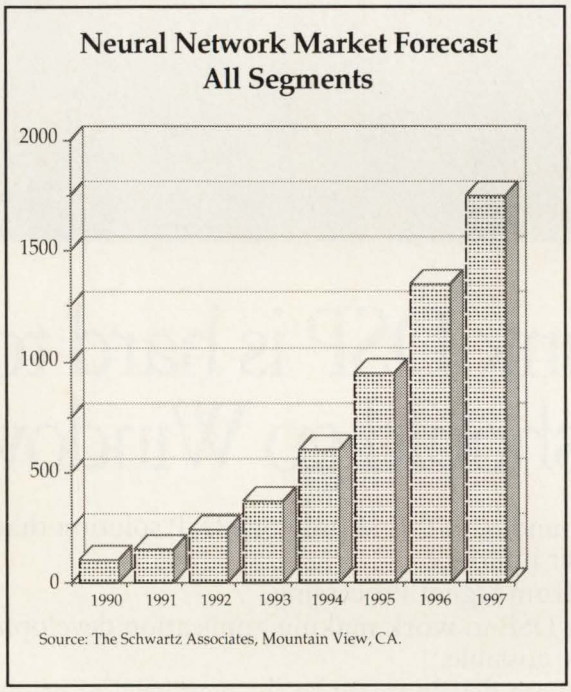

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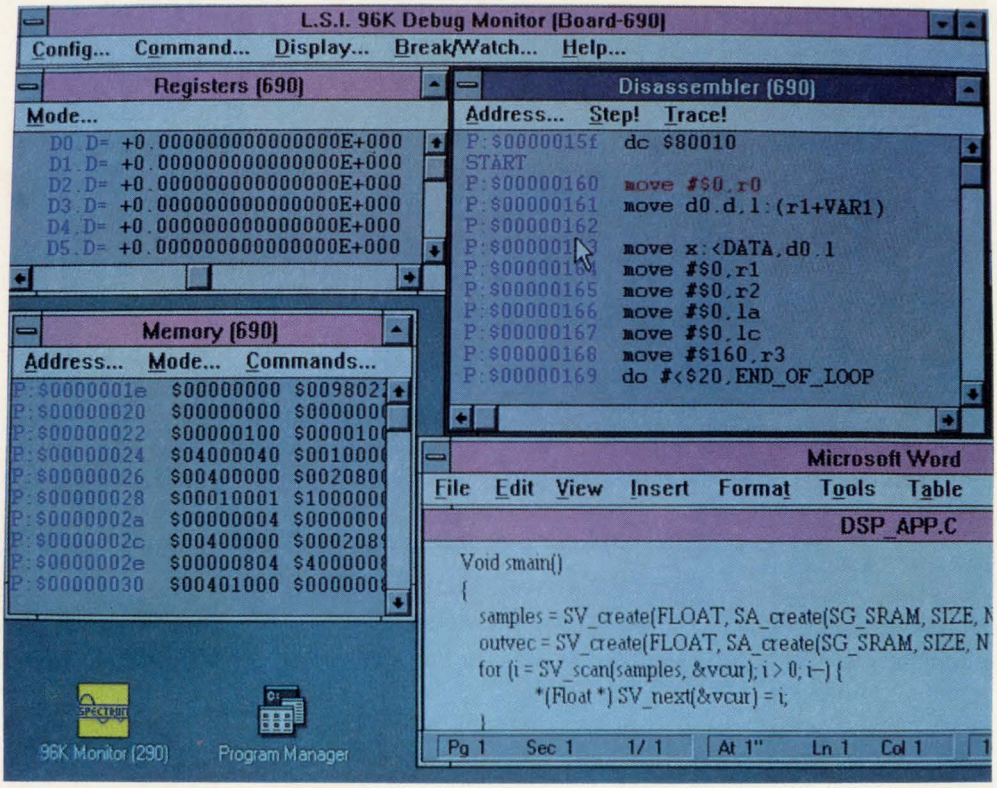

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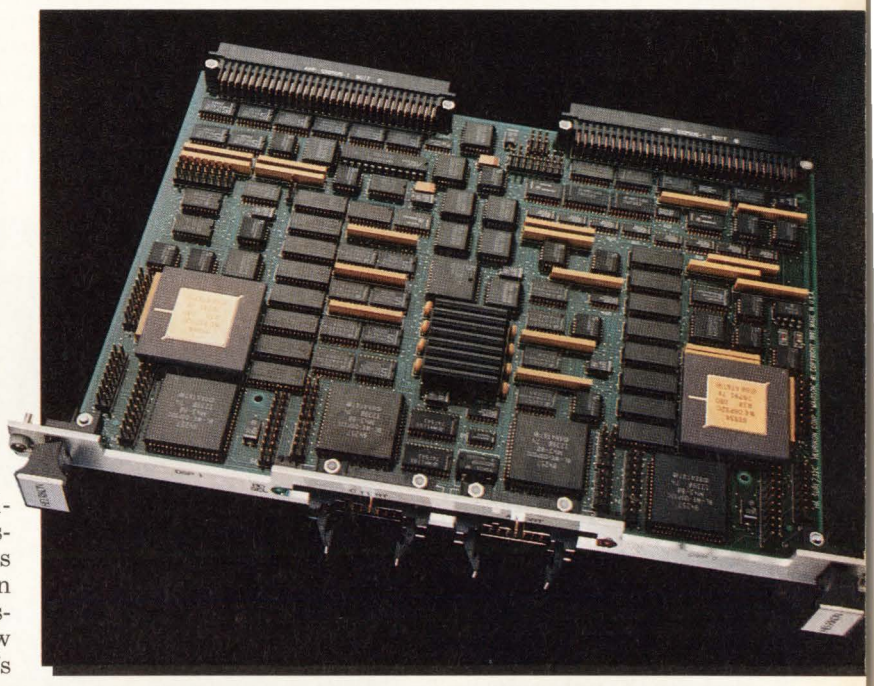
DSP boards reach performance highs

Despite a slow start as a mainstream technology, DSP is performing tasks ranging from speech and image processing to embedded control.

Warren Andrews
Senior Editor



The growing trend toward using multiple DSP chips in a single system is apparent in this DSP board from Heurikon. It includes six 32-bit floating-point chips on a single 6U VMEbus card. The board uses AT&T's DSP32C.

Standard-bus, board-level digital signal processing (DSP) technology has achieved mixed success in the commercial and industrial worlds over the past few years. At many times, it's shown the promise of becoming a mainstream technology, only to flounder while awaiting the "next" level of enhancements. Now the technology seems to be on the verge of yet another, and perhaps more significant, upswing, as hundreds of military and commercial applications demand the level of performance possible only with DSP techniques.

This latest surge in activity is occurring because significant hunks of technology, missing in earlier generations of DSPs, are now being put into place. Yet some areas are still slow in coming up to the maturity level needed to make DSPs widespread. "We're just now starting to see engineers coming out of school that are comfortable with DSP," says Jeffrey Milrod, product manager at Ixthos (Silver Spring, MD), a DSP board maker. Besides a shortage of experienced designers, another impediment to widespread acceptance of DSP technology has been a lack of good, solid design tools. And despite the efforts of major DSP IC manufacturers, C compilers and software tools often fall short of what's needed.

Nevertheless, DSP approaches are gaining ground because the existing problems are countered by positive trends in at least three directions. First, designers are leaning toward the use of multiple DSP processors in a system. This often means multiple processor boards in a cage, as well as multiple processors per board. Second, software tools and DSP operating systems are emerging which will greatly simplify the task of harnessing DSP horsepower for a broader variety of applications. And third, DSP technology is becoming sufficiently widespread that more application-specific designs are starting to emerge. These combine front-end signal conditioning with a powerful DSP processor and a full-fledged analog back end, all on a single board.

Another factor that will have a positive impact on the use of DSP over

the next several years is the growing interest of personal computer, workstation and industrial control designers in multimedia approaches. The recent agreement between Apple and AT&T for AT&T's 3210 DSP device, as well as the proposed joint project of IBM and Texas Instruments to develop a similar device for IBM PCs are two examples.

And finally, designers are beginning to look at DSP solutions for some problems that have traditionally been solved with mechanical or analog fixes, such as active automobile suspension.

The RISC alternative

While these factors are working in favor of DSP's wider acceptance, RISC-based approaches to solving many DSP problems abound, most of which take advantage of the processing power of the Intel i860. "For those applications that need real high-level performance," says Barry Isenstein, product planning manager at Mercury Computer (Lowell, MA), "starting at a half-GFlop and going up, with high I/O rates, lots of memory and multiple channels, a RISC approach is the best, and perhaps the only, solution."

"A good part of the architectural challenge in putting together a machine with the type of throughput and performance needed in the DSP world is dealing with the memory architecture," he adds. The system has to be capable of feeding the processor, but without cost becoming unreasonable. This means using DRAM. Mercury, for example, provides a minimum of two Mbytes in its leading application accelerator, with options for up to 64 Mbytes.

But the ability to address a large memory is only one of the pluses of the i860 approach to DSP. The i860 uses address pipelining, which lets it issue three instructions before using the first. It also has register scoreboarding. Both features combine to let the chip process data at speeds which outstrip even the fastest conventional DSP devices.

"In addition," says Isenstein, "the programmability of the i860 makes it appealing to many designers. When it's not clear at the outset what's needed, the fact that the i860 comes from the RISC world and can handle operating-system-type functions easily also makes it an attractive choice."

And when RISC solutions aren't quite enough, highly specialized array processors can be invoked (see "Integrating vector and scalar DSP boards in frequency-domain processing applications," p 72). In such applications, particularly in highly focused spectrum analysis, you have to deal with filters in the frequency, rather than the time, domain. And when very high I/O rates are also involved, traditional approaches can't cope. Array Microsystems (Colorado Springs, CO), for example, provides boards with custom-array processor chips to handle these higher processing needs.

Spectrum Signal Processing's Ross Mitchell looks at one of the company's latest signal processing boards. The company pioneered VME DSP boards, but it now offers a broad selection of boards in a variety of formats, including SBus.

The flip side

But no one approach solves all problems. RISC approaches, including those that use the i860, have drawbacks as well as advantages. "High-throughput DSP applications frequently have a real-time component, as opposed to the type of continuous processing done by accelerator/coprocessor approaches such as those of the i860," says Ross Mitchell, business unit manager for workstation products at Spectrum Signal Processing (Burnaby, British Columbia). "The i860 is a good solution in a specific area, where all that's being done is continuous operations. The i860's the fastest floating-point device out there, without question, but its interrupt latency can be measured in days. And with all its registers to store, it can't really do context switching for real-time applications effectively."

But often, RISC solutions such as the i860's are thrown at problems because of the high level of floating-point performance. "In many cases," says Ixthos' Milrod, "those applications just need more power. But what's surprising to me is that, in many cases, problems are not strictly a 'flop-page' problem, but really a systems-level I/O real-time-response problem." Milrod cites the example of an application where a user has a large number of sensors that have to be correlated. "Even though the correlation itself was a very simple algorithm and could probably be done with no problem in a 68000," he continues, "it could not get all the data in and out and talk between channels and still get real-time response. To handle all these requirements took the resources of multiple DSP devices." He says that such distributed processing is driving many of today's solutions for a broad range of applications.

Milrod goes on to make the distinction between distributed and parallel processing. "Parallel processing, the kind of approach used in the transputer and often found on devices such as Texas Instruments' TMS320C40, is the approach one would use when the application simply calls for more power." But distributed processing, more of a loosely coupled approach, lets the system perform a lot of smaller tasks or computations and coordinate them through some kind of host processor

There's no question that a growing trend in the industry is to keep throwing more processors at a prob-

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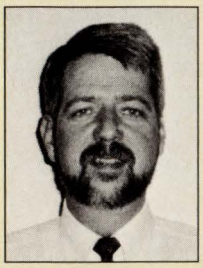
CIRCLE NO. 41

Integrating vector and scalar DSP boards in frequency-domain processing applications



With the maturation of Intel's i860 RISC processor and its related software, and the recent introduction of Texas Instruments' TMS320C40 digital signal processor (DSP), use of commercially available DSP technology for high-performance applications is now possible. In spite of these advances, however, applications requiring real-time frequency-domain conversion (FFT) of image and radio frequency spectrum data call for significantly more computational horsepower.

One limitation of these processors is that the i860 and C40 are scalar in nature, optimized to process one point at a time. High-performance applications in imaging and high-frequency spectral analysis require that data sets be processed as a single unit or vector. Many board-level vendors have developed hardware products based on these scalar processors and market them as vector processors. This has been accomplished by layering "vectorizing" software on the board to emulate a vector processor. With this approach, though, performance is still limited to the inherent capability of the scalar processor.

DSP system design options

One alternative to meeting the demands of these higher-performance DSP applications is to design systems which use multiple scalar DSP boards. Although you can achieve a very high number of Mips, Mops or MFlops with this approach, it's difficult to apply 100 percent of the theoretical computational power to the application. Commercial software supporting parallel distribution of processing tasks across multiple boards or systems isn't available, and the user consequently is burdened with a complex programming task. Although companies such as Cray, Intel and Thinking Machines are investing immense resources in developing parallel-processing software, applications are still limited to the proprietary supercomputing environment and have yet to transfer to open systems platforms.

Another alternative utilizes only function-specific FFT vector processors in frequency-domain applications. Function-specific processors typically perform an FFT seven to 20 times faster than the scalar processors mentioned above. Unfortunately, function-specific vector processors are limited in their algorithm flexibility and have almost no scalar processing capabilities.

Since high-performance DSP applications are neither 100 percent scalar- nor completely vector-processing oriented, combining the benefits of both approaches would yield an optimized solution. The function-specific processor can best be used as a coprocessor to offload the compute-intensive FFT task from the scalar processor. The scalar processor can then be used to evaluate FFT results on a bin-by-bin basis and perform other post-processing functions.

High-performance applications

Applications for this type of combined board-level solution include systems that require lossless data capture and processing, minimized slot and power consumption and maximized spectral resolution with dynamic range. These high-performance applications include digital receivers, military radar, communications, electronic countermeasures (ECM), medical imaging, test instrumentation, and video processing.

In wide-band signal analysis, the vector processor calculates the spectrum of the signal. The scalar processor then analyzes the FFT output bins to detect the presence of a signal within subsets of the wide-band frequency range. The scalar processor can then tune a receiver to that frequency to listen for or collect more data. This process of coarse analysis followed by fine-grain analysis is an important consideration in many intelligence-based applications. The system also profits from implementing the ultra-high-performance FFT function in a single card slot.

Another application example is that of an adaptive filter system, which requires the filter transfer function to be updated in real time based upon the frequency content of the incoming signal. In this environment, a vector processor is programmed to perform a finite impulse response (FIR) filter in the frequency domain. A scalar processor analyzes the FFT output and determines if modifications are required to the transfer function. If changes are required, the scalar processor will generate the new transfer function, which will be used in the execution of the FIR filter.

Frequency-domain filters are preferred when the number of filter taps is large or when precision notch filters are required. This process requires that the filter response be transformed into the frequency domain along with the signal data. The filter is performed by multiplying the FFT of the incoming signal with the FFT of the transfer function. An inverse FFT returns the filtered signal to the time domain.

System integration issues

In a parallel-processing environment, hardware integration is complicated because a single vector must be intelligently distributed among multiple boards in real time. By comparison, the integration of a combined function-specific vector processor with a scalar DSP board is uncomplicated. The physical interface between the boards is only dependent upon transferring complete vectors between the vector and scalar processors. Due to the independent functionality of each board, the system requires only a very simple point-to-point synchronous interface, which can transfer data at up to 80 Mbytes/s.

Software integration is easier with the combined vector-scalar processing architecture than it is with parallel-processing architecture, because the vector-scalar solution implements a serial-processing flow. In serial processing, the segregation of tasks is well-defined and the functional software for each board can be developed independently. In a parallel-processing flow, software can't be developed independently, because each board is interdependent with all other boards in the parallel-processing system.

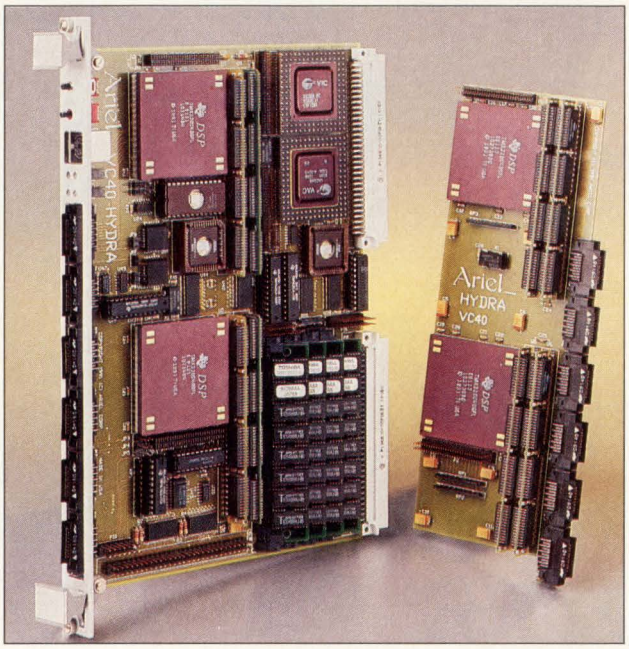
System designers struggling with the unending trade-off between performance and resolution should consider using function-specific processor boards in their high-performance DSP applications. With the combination of a function-specific board and a scalar processor, they can realize the benefits of both performance and resolution in a compact system. Although there is a wide variety of scalar processors available today, none are as efficient as the combination of the scalar and function-specific processors.

Anthony DiRenzo, vice-president of board products, Array Microsystems, Colorado Springs, CO

lem—whether in a parallel or distributed architecture, a RISC or a DSP. Early designs included one or perhaps two DSPs on a board. Today, there are several offerings with four processors on a single 6U VME card, and at least two companies, Communication Automation and Control (Allentown, PA) and Heurikon (Madison, WI), are using six DSP chips. Even in the RISC world, the tendency is to include more than a single processor.

While RISC-type processors will continue to be great fits for a variety of applications, new chip designs and dramatic improvements in software and design tools continue to make inroads into many would-be RISC applications. "Many DSP designs veered to RISC because they couldn't find full-function ANSI C compilers," says Bill Maxwell, president of Quantiwave (Marlborough, MA).

Maxwell cites the example of a designer using an i860 for neural net simulation. "Neural nets are basically a lot of multiplies and adds," he comments, "and for this, DSP chips are extremely well-suited. The reason the i860 was used, despite the superiority of DSP over RISC approaches for such neural net simulation applications, was the availability of a full-function C compiler."



Ariel joins the multiple-processor floppage mart with its VME offering, which includes four Texas Instruments 320C40 ICs. The company claims 200-MFlops performance and over a billion operations per second. The mezzanine board lets Ariel increase the complement of DSPs to achieve maximum performance.

"We're starting to see some really big systems out there, as well as some smaller ones, and to some extent the performance requirements can change rapidly," says Mercury's Isenstein. "The solution is to let systems be scalable, so users can select the performance level required and step up or down from that without major redesign."

Need for more power continues

This doesn't dilute the need for more processing power on a single card. In fact, Mercury plans to accomplish just that in the near future. But, as Isenstein explains, "The limiting factor in processor density on a single card is power consumption. Even on standard 6U VMEbus, a slot is specified at 15 W. Most vendors push that limit to 25 W, while others stretch to double the 15-W specification to 30 W." Isenstein believes that the heat generated could severely impact system reliability—particularly in high-reliability medical and government applications.

But that scenario is slowly changing, as chip makers and third-party software houses start to put the pieces together. While gradual improvements are being made in compilers for AT&T, Motorola, TI, and other families of DSP devices, Ixthos' Milrod thinks that the 21020 floating-point chip from Analog Devices (Norwood, MA) has a leg up on most of the other contenders. "I think Analog Devices' C compiler represents a change in the traditional type of compiler design," says Milrod. "The TI and Motorola C compilers, from my perspective, are really hard to use, with a lot of bugs, and haven't been the kind of mature compiler technology that most engineers have come to expect when programming such devices as the 68000 and i860."

"Analog Devices," Milrod continues, "being the last guy to the table, has been able to see the mistakes of the other makers and has kept everything in-house."

Real men don't use Pascal

The tendency to use C compilers for traditional DSP applications is partly due to some old—and not altogether incorrect—notions about assembly code. "The need for writing application code in assembly has largely evaporated, now that good compilers and libraries are available," says Milrod.

Libraries have become so sophisticated, says Anthony Agnello, president of DSP board maker Ariel (Highland Park, NJ), "that they not only look at very specific functions such as a DTMF [dual-tone multifrequency] function, but the library cells now provide broader functions, such as an entire V.32 modem." Such libraries, continues Agnello, are easier to use and cover far more applications than those in the past.

But despite the improvement in tools, according to Milrod, "there are many designers and programmers from the old school of DSP. They don't trust the compilers and, even if they do trust them, they believe they won't get any code that's usable. Some of these designers are from the school that insists on the superiority of assembly code." And though the tightest program loops will always be hand-coded, there are many around who still believe that "real men don't use Pascal."

"I think that's changing," Milrod adds, "and we're encouraging everyone to write code in C and only break down modules if they have to." Libraries are hand-coded, provide optimized performance for particular applications and now include functions for a very broad category of applications.

But libraries aren't the only portion of DSP technology tuned to a specific function. "There's a growing trend toward incorporating more front-end and back-end functions onto DSP cards, essentially making them more application specific," says Agnello. Most DSP boards have at least some analog-to-digital and digital-to-analog capability, but more and more are including some specialized signal conditioning hardware and software to focus on a specific application.

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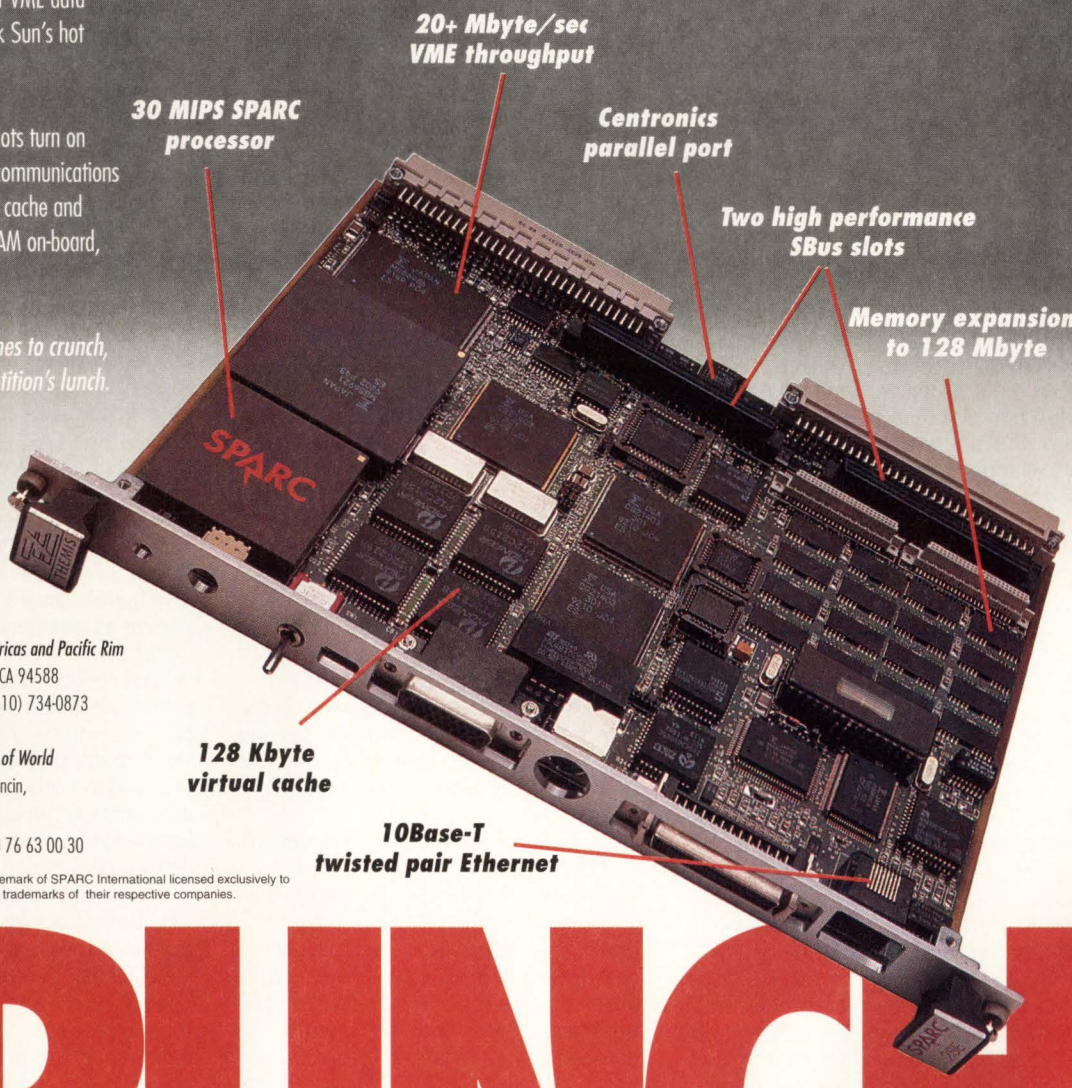

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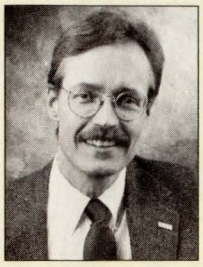
CRUNCH

VMEbus CPU and DSP boards team up for embedded control applications



VMEbus digital signal processing (DSP) boards are frequently used as coprocessors in DOS and Unix systems to accelerate compute-intensive functions such as graphics, speech analysis and image compression. Increasingly, however, DSP boards are finding their way into embedded applications such as closed-loop control and simulation that require deterministic real-time response.

To address these applications, system designers are beginning to integrate general-purpose CPU and DSP boards under a common real-time operating system in a closed-loop configuration. In a typical scenario, the CPU board acts as a main controller, running the main application program and servicing interrupts. The DSP board serves as a coprocessor, executing compute-intensive tasks and performing data acquisition. Communications and data transfer between the two boards are conducted via interrupts.

DSP boards are ideal for a variety of real-time, closed-loop control applications. Consider, for example, vibration cancellation for an active suspension used to house a space-based telescope. In such an application, the DSP would be used to generate motor control signals that compensate for vibrations in the structure. When the structure vibrates, a laser interferometer supplies the CPU/DSP board tandem with position information for the structure. The DSP, in turn, translates the position information into compensating signals for piezo motors that control the structure.

DSPs are also ideal for real-time simulation. The effectiveness of a sonar system, to take one example, could be determined by using a DSP to simulate a variety of acoustic environments. Similarly, the effectiveness of an on-board flight control system might be determined by using the DSP to simulate the space environment. In both cases, an application program running under VxWorks would be used to determine the characteristics of the environment, with the DSP generating the actual signals driving the target system's sensors.

One factor that simplifies the integration of a DSP board into a real-time control loop is that most DSPs provide very fast interrupt response. Many, in fact, respond to interrupts more than an order of magnitude faster than conventional microprocessors. For example, the AT&T DSP32C provides a worst-case interrupt latency of under 200 ns.

DSPs provide fast interrupt handling because they don't have to save as much context as general-purpose microprocessors. When the DSP32C receives an interrupt on one of two interrupt pins (one for high, one for low priority), for instance, it automatically saves the state of its arithmetic unit and pipeline into shadow registers. At the same time, the DSP vectors to an interrupt service routine that resides in an on-chip, relocatable exception table. Both operations occur in a single clock cycle.

If the handler for the interrupt is simple enough—for example, a serial I/O port read—then it can be incorporated directly into the two-word exception table entry. More complex handlers can be implemented by inserting a jump instruction to a location in the DSP's on-chip RAM into the table entry.

CPU/DSP communications

The principal challenge in combining VMEbus CPU and DSP boards in real-time closed-loop systems is providing for high-speed, two-way, deterministic communications between the boards. Ensuring real-time response for host-to-DSP communications is relatively easy for two reasons. One is the DSP's fast interrupt response. The other is that DSPs often run relatively few tasks and no real-time OS. Consequently, there is less competition for the DSP's resources and a greater likelihood that the handler will be executed promptly once the DSP is interrupted.

To invoke a DSP routine on Heurikon's HKDSP/V32C, for example, the host-based VxWorks or Lynx application makes a system call such as IOCTL (I/O control) and supplies parameters for the routine that it wants to invoke. This system call invokes a device driver, which issues a VMEbus interrupt and writes to a memory-mapped control register on the V32C. Writing to this control register, which provides one bit for each of up to six DSPs, causes the hardware interrupt pins for the appropriate DSP or DSPs to be toggled.

Because each of the DSPs is treated as a separate device, it's possible for multiple DSPs to communicate with multiple host processors simultaneously. The host can transmit any data associated with the interrupt by writing to either the DSP's parallel I/O port or to the V32C's shared memory, which is mapped into the VMEbus and host processor's address space.

DSP-to-host communications

Ensuring real-time response for DSP-to-host communications is more challenging, because the host typically runs multiple tasks under the control of a multitasking OS. Consequently, the handler for the interrupt may have to wait, depending on its relative priority and the task that was executing at the time of the interrupt.

In a conventional Unix system, for example, the handler must wait for the current task's time slice to expire. Moreover, because the user can't set the handler's priority (Unix sets the priority based on the system load and the task's prior run time), there is no way to ensure that the handler will be executed in a timely manner, even after the CPU becomes available.

Real-time operating systems such as HKLynx and VxWorks simplify matters because they are pre-emptive and enable users to set the handler's priority. With HKLynx the programmer implements the handler as a thread (task), which waits on a location in memory known as a semaphore. When the DSP board sends a VMEbus interrupt, an interrupt service routine clears the semaphore, which causes the thread to be placed on the active task list. By setting the thread's priority higher than that of the system's others processes, the programmer can ensure that the thread will be serviced as soon as the CPU becomes available.

By integrating a DSP board with a CPU board, designers can address compute-intensive applications that are beyond the reach of conventional CPU boards. At the same time, integrating them under a common pre-emptive, real-time OS with support for user-definable priorities lets them forge a real-time link that opens a broad range of closed-loop, real-time applications.

Steve Tesmer, DSP product marketing manager, Heurikon, Madison, WI

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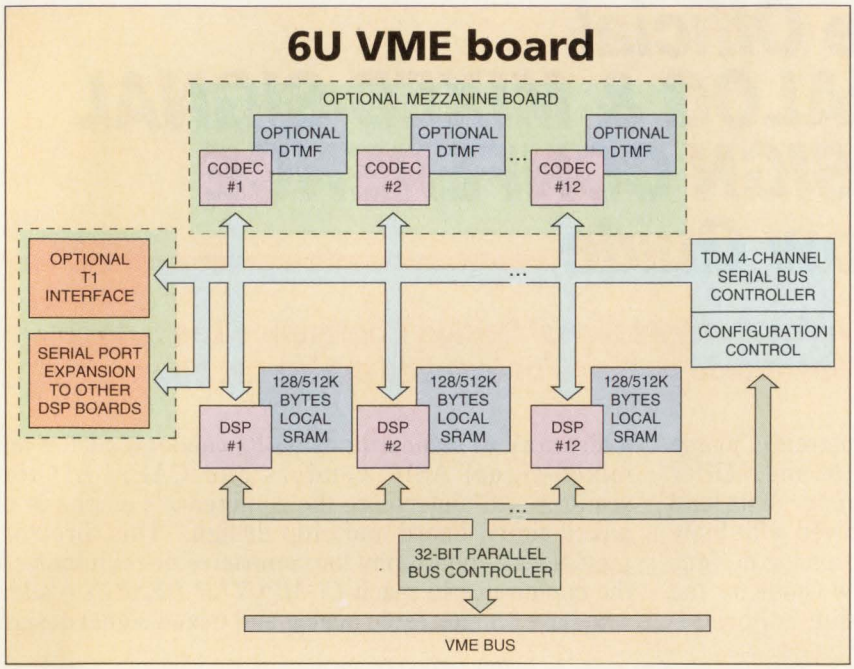

Communication Automation and Control's 6U VME board is one of the few to sport six 50-MHz floating-point DSP chips. Designed for applications in telecommunications and neural networking, the board is based on the AT&T DSP32C, and is capable of turning 150 MFlops and 75 Mips. In application, it can be combined with T1 and codec daughtercard options, with optional expansion to additional DSP boards.

This tendency toward application-oriented approaches is epitomized by Data Translation's (Marlborough, MA) DT 3801 instrumentation board. Based on a TMS320C40 and designed as a total test solution, Data Translation's device includes an analog waveform digitizer subsystem for analog signal input, an analog waveform synthesizer subsystem for analog signal output, a dynamic digital input subsystem, a dynamic digital output subsystem, and host communications over a standard bus.

But Data Translation's instrumentation isn't the only place application-specific DSP boards are showing up. "Ariel, for example," offers Agnello, "makes two very application-specific products, its Speech Station and Sys ID boards." The Speech Station, he says, is a speech spectrogram analysis board that lets speech researchers use a spectrogram, cut and paste speech segments and give both FFT (fast Fourier transform) as well as LPC (linear prediction coding) analysis.

Sys ID is an FFT-based, two-channel device that outputs a stimulus, such as a chirp, that's programmed by the user. The board then records the system's response on one or both of its input channels and examines the complex frequency response. The board outputs the stimulus synchronously and repeatedly so that it can do time-domain averaging. Any spurious noise in the system is uncorrelated and tends to disappear, while the signal tends to be reinforced. This lets the board provide measurements with dramatic dynamic range—exceeding 100 dB. The technique, according to Agnello, is widely used for everything from monitoring hair cells inside the cochlea of the ear to measuring the vibration of suspension bridges.

Ixthos has taken a somewhat different approach to application-specific boards. "We've created our own mezzanine standard, which we call the IXI bus," Milrod says. "It's essentially a pinout of the data bus of the AD21020 with some of the flags, interrupts and control signals. We've made that available to users, and we, as well as some of our customers, have developed a number of front- and back-end signaling add-on cards."

Ixthos has just introduced one such board with four Analog Devices AD1849 sound port chips. These are signal-conditioning chips, each of

which includes a codec, two 16-bit inputs, two 16-bit outputs, gain control, attenuation on output, anti-aliasing filters, and sigma-delta capability for programmability. In addition, to foster more pre-conditioning, the card features a 2101 fixed-point processor to do any pre-filtering or post-processing and take the load off the host floating-point DSP.

There's little question that DSP technology will continue to find uses in specialized areas with needs for traditional signal processing. These needs are addressed by general-purpose as well as special-purpose boards, including both RISC- and DSP-based products. But such special applications are just the tip of the iceberg. DSP boards are starting to emerge in an ever-broadening range of applications. With new software tools, it's now easier to design vector processing systems with DSP than it is with RISC machines. And it's easier to link several DSP chips together—for example, TI's 320C40—than it is to join other RISC-based processors.

DSP technology is also starting to gain a foothold in the embedded control area, as well as finding use as an intelligent UART. Some applications are taking the technology to extremes, using DSP-based boards as CPUs. But these developments are just a beginning, and as semiconductor companies leapfrog each other with processor developments, even more applications for DSP technology will emerge. ■

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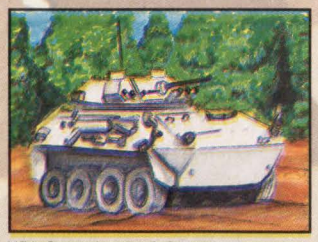
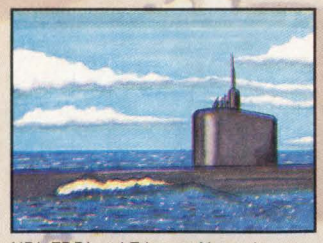


NDI: Control and I/O Systems



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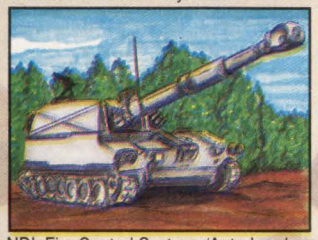


NDI: Fire Control Systems/Auto-Loader

NDI: Gun Control/Auto-Loader

Making the 400-MHz computer a reality

After clock distribution and caching architectures, the design of high-speed digital systems demands careful component selection and attention to physical layout.

Stephan Ohr, Contributing Editor

It's no secret that the high-performance workstations of today—especially the RISC machines—are based on the supercomputers of yesterday. The vector processor Seymour Cray designed for Control Data Corporation embodied all the principles we've come to associate with RISC microprocessors: a simplified instruction set, a register pipeline for instructions and data and an extremely fast clock. In fact, Cray built a huge register chain around the CPU because he regarded main memory, with its addressing, access and refresh cycles, as oppressively time-consuming.

Today's computer designers are building personal computers and graphics workstations that embody the same assumptions: avoid addressing memory, do as much work as you can with a fast SRAM cache and, if you really want performance, keep your clock cycles as short as possible. PCs which use a 50-MHz clock are starting to feel commonplace, and already we're starting to hear

about "clock doublers" which let a CPU run twice as fast as its bus interface—not to mention Intel's P5 and MIPS' R6000, which run at 66.7 MHz, and the high-end Sparc processor that's being designed to run at 80 MHz. What's more, technologists at Intel's workgroup computing division (Hillsboro, OR) believe the technology exists to build a 50-million-transistor microprocessor running at 400 MHz, and that desktop PCs embodying such technology will be commonplace by the year 2000 (see "Toward a 400-MHz, 50-million-transistor microprocessor," p 85).

There's no question about what we'll do *with* all that processing power. The problem is what these ultra-high clock rates may do *to* our designs.

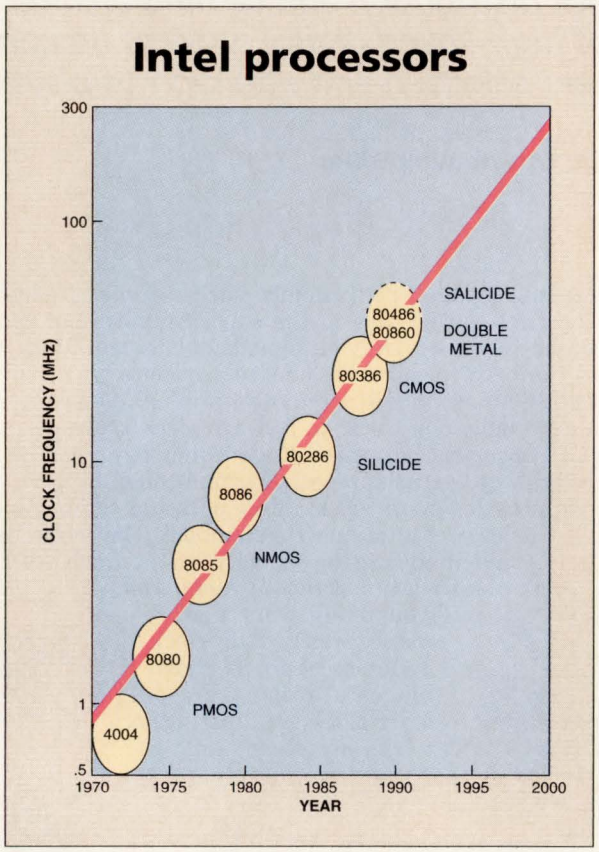
Memory and I/O buses may not be able to run at the same speed as the CPU, forcing us to design computers as concentric circles, hierarchically organized according to data transfer rates. We may need to develop and harness specialized IC technologies to ensure that all components run at the same speed—at least within the same circle. And unless we want to make new contributions to the already crowded radio frequency bands, we'll need to pay much more attention to physical layout.

Three paths to success

The success of a high-speed design, then, is pegged on three issues. Architecture is the first concern. You need to control what happens at each clock cycle—what system elements need to be closely tied to the system clock and what elements can function asynchronously. Specialized high-speed components will be applied to clock distribution and to the interfaces between processor and cache, cache and main memory. In fact, one significant trend is the emergence of processor-specific SRAM components.

Next, component selection will be an issue at very high clock rates. You'll need to choose between systems that utilize high-speed CMOS and those that use a bipolar technology such as ECL. The logic levels of the two technologies aren't compatible, and level translators will consume clock cycles and power. BiCMOS will be used to facilitate higher fanout loading rather than to increase speed, and digital GaAs will have a place in mainframes and minis—as well as in supercomputers.

The third issue is physical layout, and the design tools which help visualize the analog effects of physical layout. Required aren't just critical-path and other timing analyzers, but tools that model the impedance effects of IC lead lengths and PCB trace widths. The effects of impedance mismatch—the "invisible monsters" of noise, ringing, crosstalk, and ground bounce—will destroy a high-speed design. Increasingly valuable will be the modeling tools that let you visualize these monsters on a workstation screen. IC vendors, however, will need to contribute models showing the effects of lead length and package type on the performance of their parts.



Intel believes that smaller processor geometries, coupled with special fabrication technologies, will make possible microprocessors with 50 million transistors operating at 200-MHz clock rates—400 MHz with the help of "clock doublers." While machines such as this may be common in the year 2000, the increase in system clock rate from 50 to 66 and 75 MHz will pose some severe design challenges in the near term. Intel's processors, along with their fabrication technologies, are plotted here by clock frequency and year of introduction.

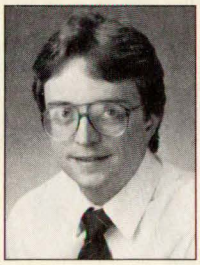
Integration reduces delays

If there's a single goal for high-speed design, it can probably be expressed as the need to keep propagation delays short. Computer system architectures, as a consequence, will take advantage of the high levels of semiconductor integration as a means of reducing the interconnect delays that result in moving a signal chip-to-chip. According to Hal Dozier, vice-president of advanced development at supercomputer maker Convex Computer (Richardson, TX), the level of IC integration was key in his company's decision to use gallium arsenide (GaAs) devices in the company's high-end C-3 computers.

There are two models in the C-3 series, the C3800 and C3400, each configured with up to eight parallel processors. While both machines will do the same job—they're binary compatible, in fact—the peak rating for a C3800 performing 64-bit, double-precision, floating-point operations is about 1 GFlops (960 MFlops, to be more precise). The peak rating for a C3400 performing the same operation is 400 MFlops. The differences between the two models are a function of their instruction cycle time: the C3800 is a GaAs machine with a 16.7-ns cycle time, the C3400 is a BiCMOS machine with a 40-ns cycle time.

Dozier was the project chief on the C3800, which was built with GaAs parts from Vitesse Semiconductor (Camarillo, CA). There were two advantages to using the Vitesse parts, he says. First, the interface circuitry is very similar to ECL, which provides 1-V logic swings, from –0.8 to –1.8 V. This avoids the need for level-shifters, and makes for an easier transition from the earlier C-2 to the C-3. Secondly, Vitesse offered a relatively high level of integration for GaAs parts. "Vitesse did an excellent job of pushing GaAs density up," says

Toward a 400-MHz, 50-million-transistor microprocessor



The demand for higher-frequency microprocessors will continue to rise. This will result in CPU frequencies of 400 MHz by the end of the decade, and some changes in computer implementation will be required unless we want all of our digital designers to hold radio frequency licenses. This dramatic increase in CPU frequency will depend upon advances in process technology, manufacturing, packaging, and design techniques—but not one of these areas will present a substantial impediment to the construction of a commercial desktop PC with an aggregate performance exceeding 2,000 Mips. Machines such as this should be available in volume by the end of the decade.

Semiconductor process technology has accounted for the dramatic increase in transistor budgets and clock frequency scaling over the past 20 years. Geometry reduction has been used extensively since the early 1960s to simultaneously improve chip density and device performance. Advances in lithographic and dry etching techniques have already reached the submicron level, improving the density of transistors per unit area at a rate of 25 percent per year.

Transistor count still doubling

The obvious consequence of reduced transistor geometry and increased die size is that the total number of manufacturable transistors per die is increasing—at a rate of about 40 percent per year. This rate falls within Gordon Moore's 1975 prediction, which called for a doubling of transistors every two years. This suggests that logic devices with 50 to 100 million transistors will be manufacturable by the end of the decade.

A 50- to 100-million-transistor device operating at 400 MHz must also clear new hurdles in packaging and power management. The power dissipation of a microprocessor, for example, increases with the square of its operating frequency, so this end-of-decade microprocessor may require more power than we can economically provide.

Several trends, however, are likely to alleviate this dilemma. Power supplies will move from the current 5.0 V to 3.3 V, and possibly even to 2.5 V to 1.8 V by the end of the decade. This will reduce the power, both internally to the chip and in the input and output buffers. The reduced supply voltage also means smaller voltage swings for signaling, enabling higher-speed operation. The input and output buffers will continue to drive the external "real-world" capacitance. For this reason they'll have to be very much larger than the microprocessor core transistors and won't be able to operate at the core's frequency.

Reduced parasitic capacitance packaging will also be required. One possibility may be to mount the microprocessor die onto a silicon substrate that has matched impedance drivers built into it. Finally, local refrigeration techniques may be needed to extract power dissipated by the microprocessor. It's important to note that CMOS, when cooled, increases in speed; this may yield even higher performance.

A 50- to 100-million-transistor device, operating reliably in a cooled, special package at 400 MHz, will pave the way toward higher levels of addressability and data size. Microprocessors have moved quickly from the original 4-bit 4004, to 8 bits, 16 bits and 32 bits. This follows similar trends in minicomputers and mainframes.

There's also been a migration of architectural and system features onto a single die. For example, mainframes had support for memory management through the 1970s, when paged virtual memory was introduced with the VAX minicomputer; these features have now migrated into the microprocessor. Data transfer between the processor and memory is an important bottleneck in computer designs. IBM introduced the cache memory with its 370 series of mainframes, and this feature too has been integrated into the microprocessor.

Based on this trend toward including and integrating architectural features, let me propose a new law of computing and semiconductors: "Every concept proven useful in mainframes or minicomputers has migrated or will migrate onto the microprocessor." There's been much discussion lately about RISC technologies—simpler, faster instructions, superscalar architecture and pipelining. These techniques were pioneered for the mainframe and minicomputer, and all are expected in the microprocessor shortly.

Decoupling the CPU

As clock rates continue to increase, the need to decouple the CPU core speed from its external bus speed is becoming essential. This technique has, again, been used with mainframes, and was recently introduced with the 'speed-doubled' Intel 486 DX2 microprocessor, whose CPU core, internal cache and write buffers operate at 50 MHz while the bus operates at an easy-to-design 25 MHz. Expect to see multiple clock divisors in the future, with the 400-MHz frequency only visible to the CPU core, while external frequencies are in the range of 50 MHz to 100 MHz.

Running the microprocessor core at a higher frequency than its external bus can create performance bottlenecks if the core makes excessive demands on the bus unit. Cache memory filters many requests for system memory, but only simple write-through caches have been implemented on microprocessors to date. An increased transistor budget will let a larger, higher-performance write-back cache be implemented.

A conservative estimate of the size of a general-purpose CPU is about four million transistors. This estimate is based on increasing transistor counts to include various microarchitecture extensions for a 64-bit processor and compatible floating-point unit, such as cache for branch targets, multiple execution units, larger page-translation buffers, and stack-top caches. Such a CPU should perform at approximately 700 Mips at 400 MHz. Within our budget of 50 million transistors, we could include four of these CPUs, each with a 256-kbyte cache, a special-purpose graphics unit, two vector units—and still have two million transistors left to implement a designer-friendly bus interface unit.

Very high-frequency design will be contained within the microprocessor component itself, but there will still be many design challenges to support its external bus. The high-frequency, cache-coherent, multiprocessor system bus of today will become the component bus of tomorrow.

Pat Gelsinger, general manager of microprocessor division six, Intel, Hillsboro, OR

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MACH 220	2400	96	15ns	50 MHz	68	MASC 220
MACH 130	1800	64	15ns	50 MHz	84	MASC 130
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Dozier. "With 20,000 to 30,000 gates per chip, it's almost as dense as ECL."

Supercomputers such as the Convex C-3 are essentially vector processors, in which one or two instructions operate on an extremely long set of operands (a number string). The key to keeping the data moving through the CPU is to "bump it" register to register. The Convex keeps up to 128 operands in one register. When you're building long register chains, Dozier explains, the length of the interconnect path between chips can impose unwanted delays. By using GaAs chips with a high level of integration, the interconnect delays can be minimized.

Hal Dozier (foreground) examines a color plot of a GaAs chip. The vice-president of advanced development at Convex Computer says that the key factor in his company's decision to use GaAs devices in its high-end C3 machines was the level of IC integration that could be achieved.

Similar principles are showing up in the design of new-generation workstations and PCs. As is the case with supercomputers, new designs in these areas must deal with extremely short clock cycles. Workstations also make the supercomputer-like assumption that main memory accesses are slow and are to be avoided until absolutely necessary. Unlike supercomputers, however, workstations must reflect more of a general-purpose architecture, in which many different instructions are loaded and executed in rapid succession. The long register chains of the vector processor are replaced with shorter pipelines. Large caches are used for instructions and data, and "subcaches"—cache tag RAMs (T-RAMs)—are used to keep track of the information in cache.

Running at different speeds

To be sure, not every part of a system needs to run at the same speed. But those parts of a system that must run fast—the CPU, cache and cache tag logic—must run *very* fast. It's important that all elements within this "inner circle" be synchronously tied to the same clock. In this realm, every nanosecond is significant.

With such timing constraints, three types of specialized components are proving invaluable for high-speed design of caches, datapaths and control logic. One type consists of low-skew clock distribution chips, which are used to precisely synchronize inner-circle components to the same fast clock. Another type consists of processor-specific SRAMs, which shave nanoseconds from the cache-access cycle by incorporating cache control logic on-chip. High-speed cache and datapath design need support from customizable logic. A third type of component, consequently, consists of specialized PALs and PLDs—even 7400-series logic components—which are optimized for speed.

At high clock rates, the fanout loading on the system clock and the length of the wiring path between clock elements can create significant timing differences between these elements—a situation described as clock skew. Assume, for example, that the logic elements in a caching system or datapath all trigger on the rising edge of the system clock pulse. While the clock frequency remains the same in all parts of the system, inductances and capacitances in the clock distribution tree will vary the phase of the clock pulse along different branches of the tree. It is possible, then, for system elements to trigger asynchronously, paving the way for delays and timing errors. The possibility for error increases if multiple clock generators are used in an effort to minimize fanout loading.

"Logic"al alternatives

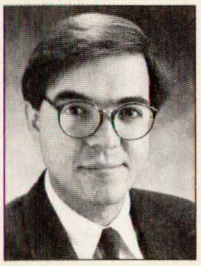
You can consider alternatives available with standard high-speed logic, such as Fast, fast CMOS technology and similar logic families. With propagation delays in the range of 3 to 6 ns, Fast family logic can be used in the datapath as latches, buffers and registers. But there's a problem with using Fast family parts for clock distribution, according to Randy Frederick, who manages the FCT family for Integrated Device Technology (IDT—Santa Clara, CA).

In principle, these parts have a clock skew specification as small as 500 ps. The problem is that this spec is contingent on the ambient temperature of the device, and even min-max figures for clock skew will produce widely divergent results without temperature derating. A better solution, suggests Frederick, is to use a dedicated clock driver, in which clock skew is specified edge-to-edge as well as part-to-part.

Low-skew clock drivers, such as the IDT49FCT805/806, provide multiple outputs with controllable phase relationships. The maximum skew between clock outputs from the same package is specified as 1 ns. The maximum skew between connected drivers in different packages is 1.5 ns.

Another clock control technique is to treat the clock generator and each

High-speed cache design demands novel components



Caching schemes for data and instructions are among the available techniques for improving workstation and personal computer performance. Yet increases in processor clock rates have made system design more difficult by taking away much of the timing margin necessary for reliable operation. Architectural techniques that provide zero-wait states at 25 and 33 MHz, such as interleaved cache banks, may prove troublesome at 50 MHz and above. Not only is there a loss of granularity, but the asynchronous SRAMs become more expensive and the control logic becomes difficult to implement. One evolving solution to this problem is novel cache components, such as processor-specific SRAMs.

Timing margin problems are most acute in the datapaths that are close to the processor. While clock rates for mainstream systems are up to 40 MHz, more sophisticated designs are being implemented at 50, 67 and even 75 MHz. Some processors—for example, the Intel 486 DX2 and the MIPS R4000—even use internal clock rates that are twice the frequency of the external bus clock. And one version of the AlphaMicro from Digital runs at three times the external bus clock. This clever design technique builds very high-performance systems, while maintaining practical costs for both the interface and external components.

Faster clock rates

Whether the external interface follows a straight or submultiple clocking scheme, increasing clock rates leave very little timing margin near the CPU. A 50-MHz clock, for example, allows only a 20-ns cycle time. The 67- and 75-MHz interfaces provide 15- and 13.3-ns cycle times respectively. Asynchronous SRAMs have benefited from advances in submicron CMOS and BiCMOS, which have produced 32k × 8 and 64k × 4 devices which operate at 10 ns, and 128k × 8 and 256k × 4 devices which operate at 15 ns. The price premiums associated with these parts, however, may be prohibitive for most desktop computers. Frequently, the only economical way to implement a cache at these cycle rates is with specialty memory or processor-specific SRAM components.

Although some high-speed processors, such as the MIPS R4000 and Hewlett-Packard's Precision Architecture, offer flexible interfaces that can take advantage of asynchronous fast SRAMs, many other systems clearly benefit from the processor-specific approach. Examples of processor-specific SRAMs include 32k × 9 devices for the Intel 486 and P5, 16k × 16 devices for older versions of the Sparc, 128k × 9 for newer versions of the Sparc, 32k × 9 SRAMs for the Motorola 68040, and 16k × 9 × 2 or 8k × 20 SRAMs for the MIPS R3000/3500. The speeds of these processor-specific SRAMs vary between 10 and 25 ns, but the real story is that generic SRAMs would have to work much faster to perform the same task.

Speeding up SRAMs

As an example, consider what happens with the 50-MHz version of Intel's popular 486. To guarantee zero-wait state operation during burst reads, a sub-10-ns cache SRAM is needed—a difficult proposition for 32k × 8 SRAMs, the preferred 486 secondary cache components. Of the nominal 20-ns cycle time, 5 ns are taken as the propagation delay of a PAL counter delay, 4 ns are required for setup, and 2 ns are lost with skew and derating. The SRAM cache must operate in a 9- or 10-ns window.

Some SRAM manufacturers have attacked the problem by incorporating the burst counter inside the SRAM, bringing back 4 or 5 ns and relaxing the required access time to approximately 14 ns. This strategy minimizes component count by eliminating the typical expensive external PAL, and can reduce the cost of cache SRAMs in many systems.

Another alternative which supports zero-wait state writes in the 486 architectural environment is to integrate self-timed write logic inside the SRAM. Since writes are completed internally and referenced to a clock edge, the need to operate from an asynchronous write pulse is eliminated.

The result of this process is the transformation of an ordinary fast SRAM into a tightly coupled, processor-specific component that solves a number of speed-related problems for the designer—and the establishment of a new set of specifications. Since the internal timing logic now operates synchronously with the cache memory, the key design parameter is no longer access time (T_{aa}), but rather clock-to-data time (T_{cd}). T_{cd} for 486-specific cache SRAMs is as fast as 10.5 ns, making them useful for 67-MHz systems, where the need for tailored cache SRAMs is even more critical.

Cache tags are yet another example of specialized SRAMs that facilitate the implementation of no-wait state caches in 50-MHz systems. These very fast SRAMs incorporate an address comparator on-board that permits the quick identification of blocks inside the cache. The critical parameter here is T_{adm}—address-to-match. Cache tags are now available in T_{adm} speeds as fast as 10 ns, and in sizes as large as 8 kbytes.

RISC processors also benefit from the use of tailored SRAMs. The MIPS R3000 and R3500, for example, use split external instruction and data caches. At 40 MHz, both cache banks are accessed within the 25-ns clock period; the address for each cache is latched on alternate clock edges. A bus contention problem emerges, however, as one bank is enabled while another is disabled, which increases pressure for faster access speed. A typical cache implementation uses 30 16k × 4 SRAMs with a speed of 7.5 to 8.0 ns—a costly solution that utilizes substantial board space. New bicameral (two-bank) MIPS-specific 16k × 9 × 2 SRAMs eliminate the bus contention problem, while reducing the necessary access time to 12 ns and the parts count to seven components. The approximate space savings is 70 percent, and the cost reduction is easily 70 percent.

The future introduction of more processor-specific SRAMs and fast logic building blocks will continue to track increases in processor clock rates.

Manuel Alba, strategic marketing and applications manager, Integrated Device Technology, Santa Clara, CA

branch of the distribution system as a transmitter-receiver combination, and to regenerate the clock pulse at each branch using a phase-locked loop to capture the original clock pulse. Such a regeneration scheme, recently introduced by Vitesse, lets multiprocessor systems—hypercube architectures, for example—be synchronized to the same clock. Maximum clock skew for multiple connected Vitesse parts is 1.25 ns.

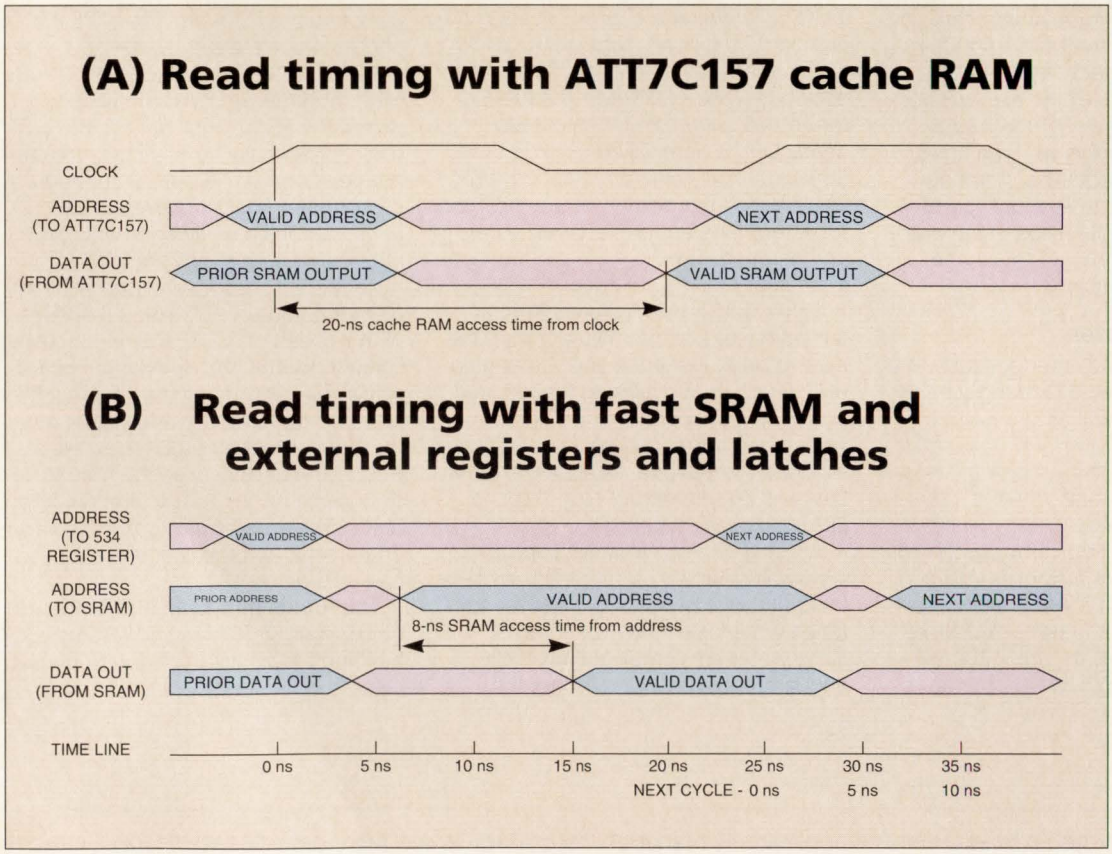
Intel's OEM computer group, which manufactures PCs for companies such as Digital and Unisys, is using a similar "copy clock" technique in its modular, scalable PC architecture, although it doesn't foresee the use of GaAs in its PCs. Intel's clock distribution scheme insists that all elements of the CPU and cache subsystem run synchronously. Ordinarily, asynchronous elements, such as the memory and I/O subsystems, are synchronized to the CPU by regenerating the system clock—across the backplane of the PC, if necessary.

Timing is almost everything

Like clock skew, the timing relationships between the CPU and cache remain critical in a high-speed system. The cache is intended to replicate information that's in main memory, but it makes it easier—by making it faster—for the CPU to get to this information. The cache typically has two elements: a small, ultra-fast cache tag which determines what's in the cache, and the cache itself, a larger entity which replicates information that's in main memory. The speed of the cache tag RAMs, or T-RAMs, is most critical. T-RAMs are typically 8k × 8 bits, and have a clockless (asynchronous) 10-ns access time. The SRAMs used for caching are somewhat larger, and use access times defined by the system clock—for example, 20 ns for a 50-MHz clock—but aren't necessarily synchronous with it.

While the Convex C3800 supercomputer uses self-timed SRAMs—5.5-ns devices—as the crossbar to vector memory, these devices tend to be too expensive to use as cache memory in workstations and PCs. Workstation and high-performance PC designers, as a consequence, are coming up with what Manuel Alba, strategic marketing and applications manager from IDT, calls "architecturally creative" solutions to cache timing problems. For example, T-RAMs and cache memory SRAMs specifically optimized for 486-based systems are beginning to appear. Ordinarily, the 50-MHz 486 allows a 20-ns access cycle. Because the 486 has its own on-chip cache, any secondary cache would be used for data writes to memory. A processor-specific SRAM such as the IDT71B589 uses self-timed write cycles. The organization of the SRAM is 32k × 9 bits, and it offers what's called a 'clock-to-data' parameter (metric) of 14 ns. (The IDT71B589 offers a 10.5-ns access in BiCMOS.) The major advantage of these parts over conventional SRAMs is that all the functional blocks—all the signal generators—necessary for a 486 processor to write to an SRAM cache are incorporated in the specialty SRAM.

A similar part, a cache device for the MIPS R3000 RISC microprocessor, is the IDT71B229. This part provides a divided "bicameral architecture" (16k × 9 × 2) in which the cache is used for both instructions and data. It lets you simultaneously access both parts of the cache with no wait states at 40 MHz. The only alternative to the convenience of architecturally creative solutions such



Processor-specific SRAMs, such as the ATT7C157, a 16k × 16 bit cache RAM optimized for Sparc applications, include on-chip address registers and data latches. Cache data can be written within 20 ns from the first clock edge (see A). General-purpose SRAMs, in contrast, provide a narrower 8- or 9-ns window in which to write cache data (see B).

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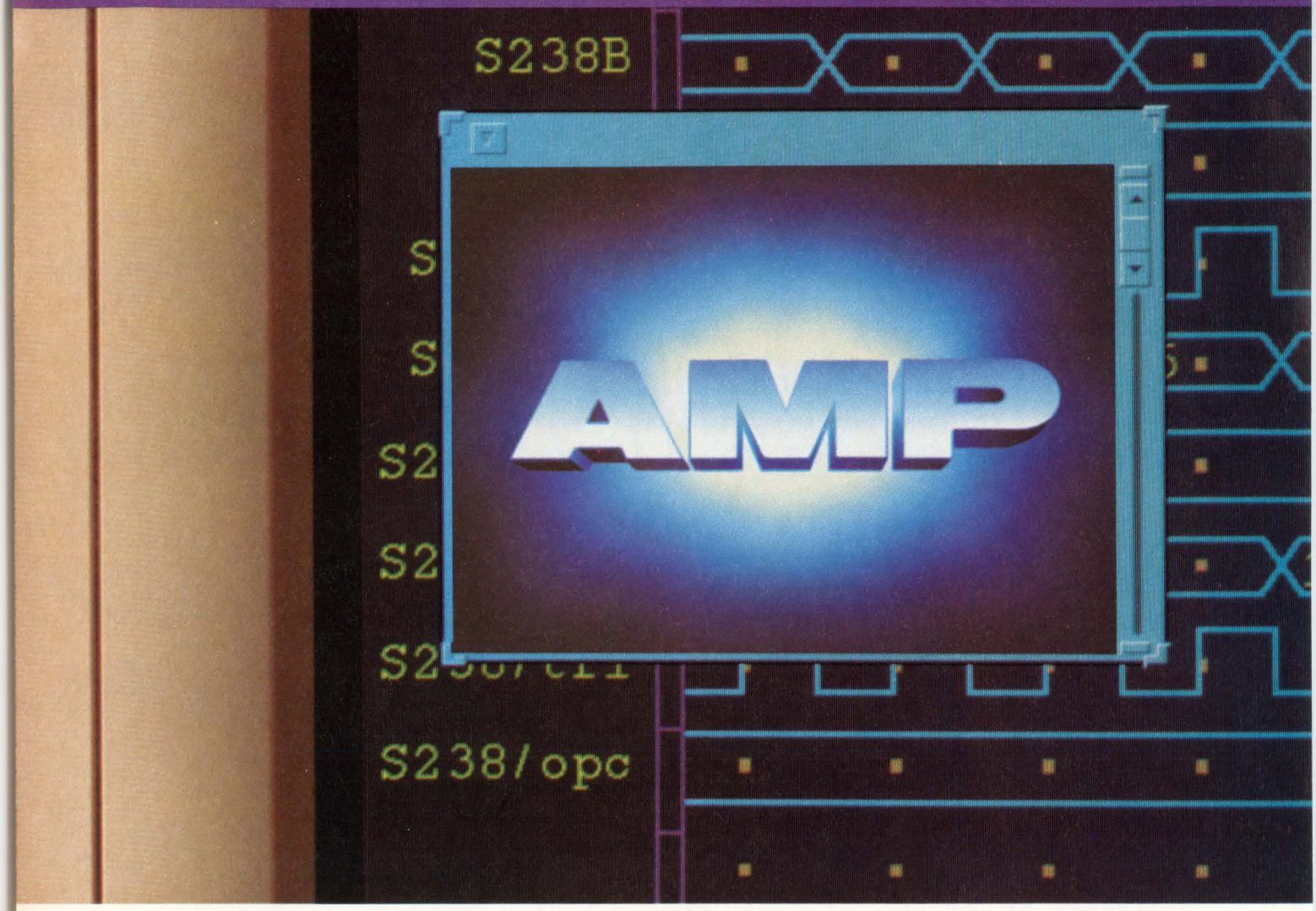

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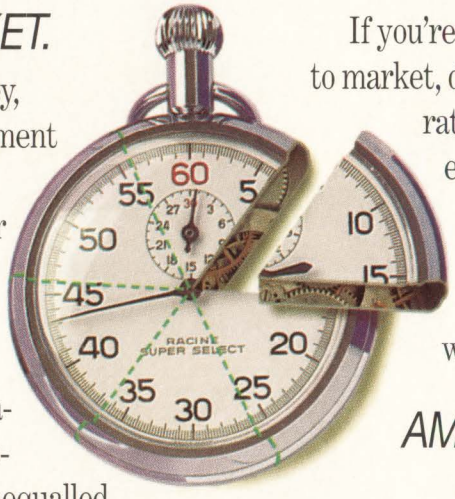

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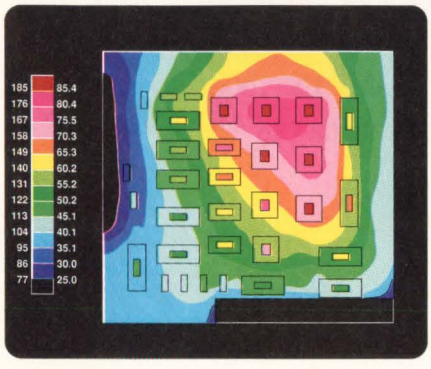

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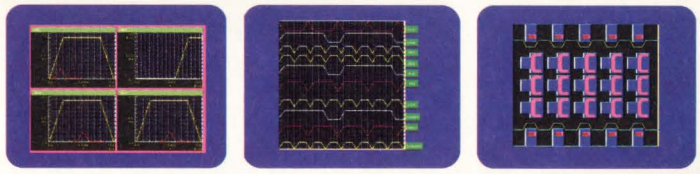

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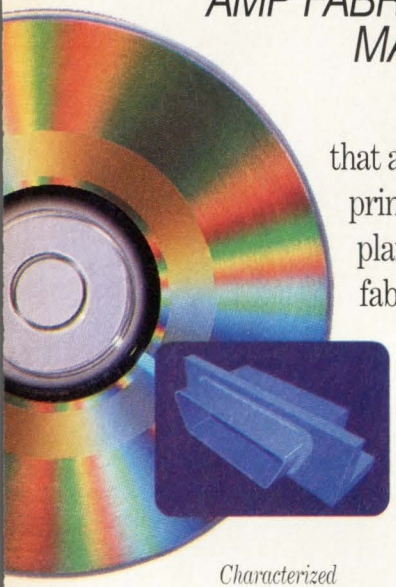

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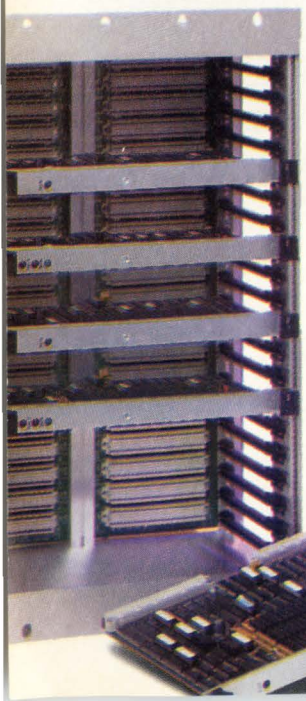

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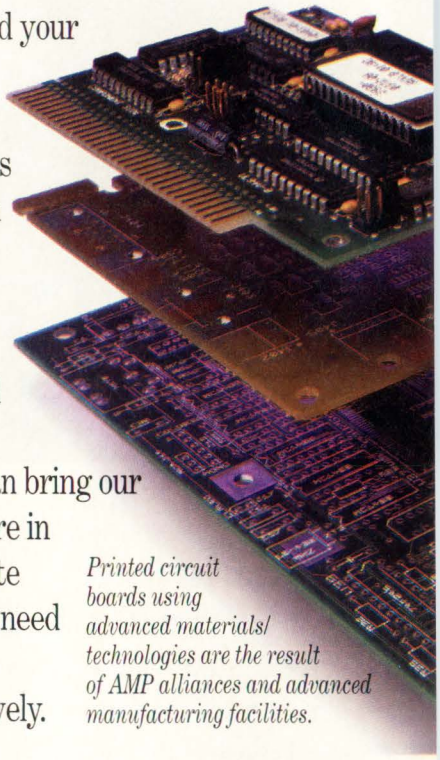

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as these, says Alba, is to use general-purpose SRAMs with sheer speed (see "High-speed cache design demands novel components," p 89).

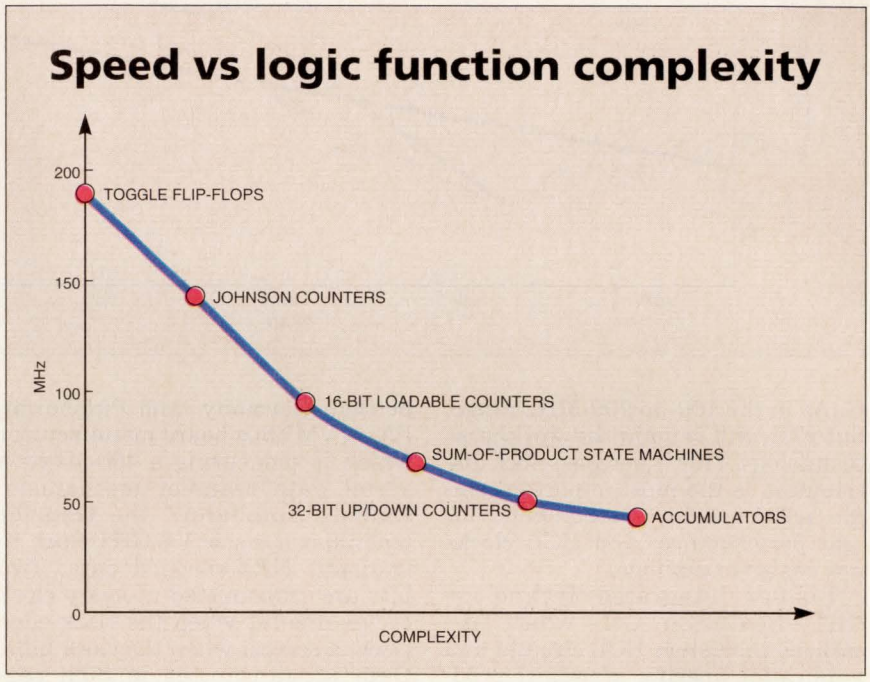
Losing time from the budget

Without specialized SRAM caches, the timing budget for even a 40-MHz system may be unmanageable. There's a 25-ns window in which to perform a cache write operation, confirms Charles Hochstedler, memory product planning director for AT&T Microelectronics (Allentown, PA). "There's just not a lot of time left to use a generic device in that setting," he explains. Typically, 5 ns is lost to clock skew and interconnect delays. On a standard SRAM system, 6 ns will be lost going through the address registers, and another 5 ns will be lost at the data latch point. This leaves only 9 ns to perform the necessary SRAM access. By putting the address registers and data latches on-chip with the SRAM, suggests Hochstedler, approximately 11 ns can be saved, leaving up to 20 ns to perform the SRAM access. (Also, two $35 parts, such as ATT7C157s, 16k × 16 cache RAMs optimized for Sparc applications, can replace eight $40 8k × 8 standard SRAMs, letting you build a less expensive cache.)

In addition to processor-specific SRAMs, we're also seeing a trend toward cache RAMs organized with wider word widths, says Hochstedler. Previous-generation parts, organized as 32k × 8 (or 32k × 9, if you include a parity bit), needed to be multiplied and clock-synchronized to couple properly with 32-bit processors. Emerging now are parts organized as 64k × 16 (or 64k × 18) for 1-Mbit caches. We'll also see SRAMs that are 128k × 36 for 4-Mbit devices. These wide-word devices minimize the cache parts count, provide easier clock synchronization and optimize timing budgets by reducing the capacitive loading on cache data lines. While high-performance 486-based systems are already utilizing 128k × 36 cache RAMs, 586-based systems will likely use a 72-bit-wide device, Hochstedler speculates. He also thinks the currently used 12-ns T-RAMs will be superseded by specialized 10- or 8-ns devices.

You may still need to construct high-speed interfaces between CPU and cache or register pipelines and the control logic for the pipelines. One alternative is to use custom logic in conjunction with very high-speed SRAMs. For this purpose, you can use very fast PALs, such as those available from Lattice Semiconductor, FPGAs from QuickLogic or standard cells from Bipolar Integrated Technology (BIT).

Inevitably, there is a trade-off between logic complexity and toggle rates. Each layer of logic between input and output can cost almost a full clock cycle in propagating a signal through the device.



At QuickLogic, there's a trade-off between logic complexity and toggle rates. Each layer of logic between input and output can cost almost a full clock cycle in propagating a signal through the device. Simple flip-flops, for example, can be programmed to operate at close to 200 MHz. Johnson counters used for one-shot state machines can operate at up to 150 MHz. The 16-bit loadable counters require one logic cell delay and reduce maximum toggle frequencies to a little better than 100 MHz. Complex sum-of-products state machines require two cell delays rather than one. The four-cell-delay parts—those embodying arithmetic functions, for example—are limited to 40 MHz.

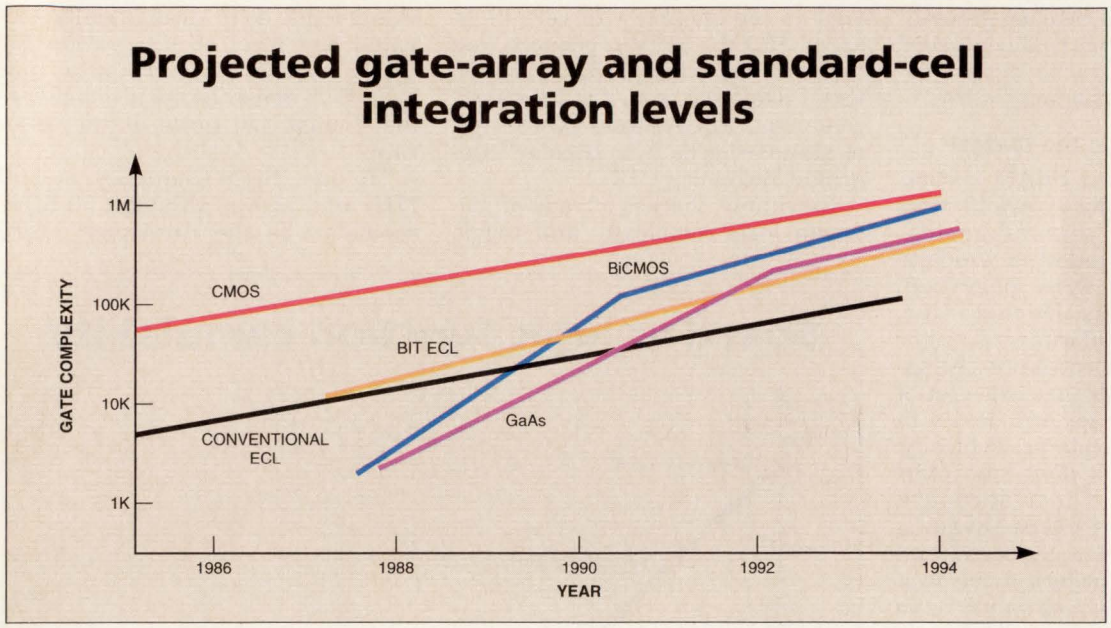
Technology choices

Because of increased clock frequencies, the technology choices for custom memory arrays and interface logic are more imposing. Higher speeds generally require trade-offs in power consumption and levels of integration. Traditionally, bipolar technologies such as ECL have been preferred for speed, while the main advantage of digital CMOS has been high packing density and low power consumption. GaAs offers extremely high speed, but has been plagued by low levels of integration and has required special interface logic.

This is now changing. Process developments have dramatically elevated the level of integration for GaAs, to over 100,000 gates per chip. ECL densities are also increasing, though not quite at the same rate.

"To me, high frequency is 500 MHz and above, although 50 MHz seems to be the threshold where things get nasty," says Todd Pearson, the strategic product planner in Motorola's logic division (Mesa, AZ). He insists that processor clocking schemes are more important in this frequency range than the technology choices. CMOS, he believes, is useful up to 100-MHz clock rates. Although you can also use TTL at up to 100 MHz, "we try to talk designers out of it," says Pearson.

ECL and GaAs operate in the same high-frequency ranges; the choice of one or the other, Pearson says, will depend on the required power dissipation. For modest levels of integration (MSI and SSI logic), ECL is the best choice. Because of its lower power dissipation, GaAs is a better choice for LSI and VLSI devices. BiCMOS has been coming on and will be competitive with



Process developments have dramatically elevated the level of integration for all technologies over the past few years. GaAs densities, for example, are over 100,000 gates per chip.

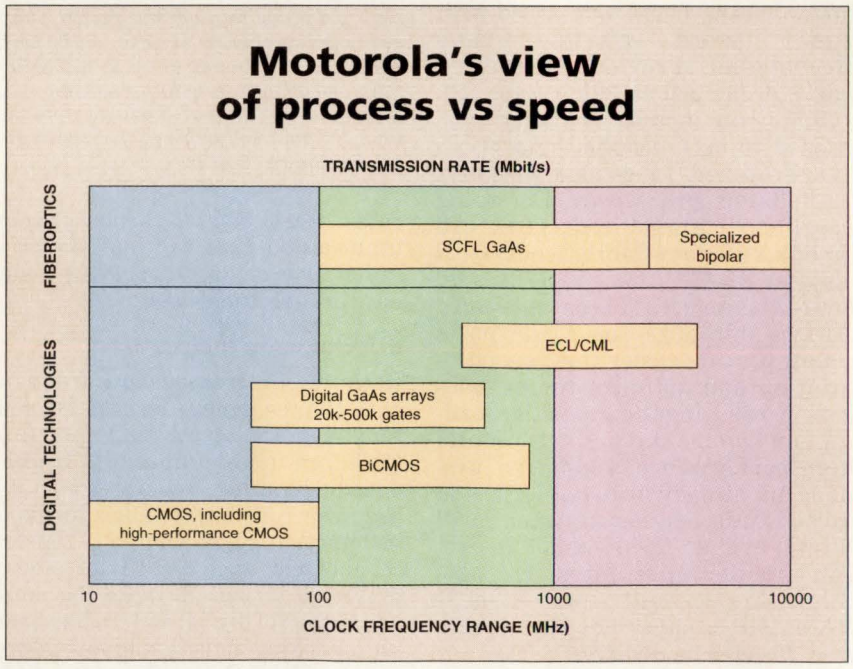
GaAs in the 100- to 200-MHz range, but ECL will remain the workhorse technology. This is because clock distribution is the most important single influence on system behavior and performance, and ECL clocks are easier to manage.

Bipolar Integrated Technology (BIT—Beaverton, OR), which specializes in custom ECL circuits and application-specific standard products (ASSPs), isn't convinced the speed-power product necessarily favors GaAs. BIT sees power dissipation of its P201 family of ECL devices as being on the order of 380 µW/gate when operating at 50 MHz—about the same level as the Vitesse FX Series (200 µW/gate) and significantly lower than other ECL processes. BIT product manager Abhi Talwalkar attributes the difference to the small geometries used with the company's P201-series arrays.

One advantage of ECL over GaAs is that it produces 'softer' clock edges. GaAs is one of the few technologies in which a transmitted square wave is still very much a square wave at very high frequencies, but this can be problematic in many applications. Ultra-fast edge rates mean that logic transitions (low-to-high and high-to-low) will be steep—too steep, in fact, for logic systems whose activity depends on capturing a transition or edge.

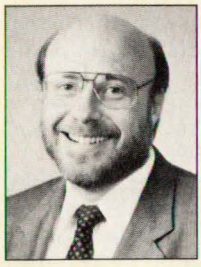
Rounding off the edges

Fast edge rates were a problem for PEP Modular Computers of Kaufbeuren, Germany (and Pittsburgh, PA), a VMEbus board manufacturer which is pioneering a 400-Mbyte/s serial data transfer mechanism. Called "Autobahn," the transfer technique uses a 1.8-GHz clock to transmit NRZ-encoded data. Two bits are transmitted at every clock cycle—one bit when the clock edge rises, a second when the clock falls. Data is transmitted in 8-bit segments, with a ninth bit inserted as a means of synchronizing transmitter and receiver with a forced logic transition. Because the technique is keyed to transitions, it could easily be confounded by sharp transitions or ringing. Early prototypes designed with GaAs were abandoned in favor of Motorola ECL parts, says PEP's vice-president and technical director, Gunter Rücker. The softer



Many manufacturers, among them IDT, are enamored with BiCMOS, and believe that adding bipolar output drivers will extend the usable clock frequency for CMOS devices. Motorola, on the other hand, sees CMOS and ECL as the workhorses for high-speed digital technology. The diagram shows Motorola's view of the technological future.

Tool requirements for high-speed digital systems



As computer designers respond to higher performance requirements and shorter clock cycle times, they begin orienting their methodologies and toolsets toward high-speed design. These methodologies require that the electrical and mechanical design of a circuit be considered concurrently with logic design and simulation to ensure the system functions at its intended speed and is manufacturable. The densities posed by IC, MCM and PCB layouts, combined with the complexity of the underlying logic, mean that an even greater number of physical effects need to be included in the analysis.

Design styles are being reorganized to facilitate the overall verification process. By producing designs that can be mechanically proven to be correct in a straightforward manner—that is, if there's a mechanical process for verifying electrical integrity—this "design for verifiability" philosophy can yield significant benefits in the quality, manufacturability and time-to-market of high-speed digital systems.

Timing verification

One example of this approach is in the area of timing verification. Modern CPU designs are likely to have many thousands of logic memory elements, such as flip-flops and latches. Each of these must have setup and hold timing constraints satisfied on its inputs under all possible process parameters and operating conditions. Short cycle times force the verification process to include interconnect effects such as transmission line delays. The use of timing simulation approaches will, in general, have limited practical utility for this type of verification. Compared to the number of test vectors required for node coverage in such a fault simulation, the number of test vectors required to stimulate every possible circuit path is huge.

By employing a strictly synchronous design methodology, however, it is possible to utilize static timing verification tools to perform the necessary checks. These tests can be performed rapidly, exhaustively and without the need for test vectors. The use of this type of synchronous methodology is becoming increasingly popular for large, high-speed designs.

Except for the fastest systems, optimizing digital system performance has historically involved a reduction of the propagation delay of the logic elements comprising the system. At higher clock rates, however, interconnect delays increasingly dominate the cycle-time budget. This is becoming true at all levels of the design hierarchy—at IC, MCM, PCB, and system levels—although for somewhat different reasons.

A "design for verifiability" philosophy can assist in the timely creation of high-quality and manufacturable high-speed designs.

At the IC level, loading effects due to metallization capacitance are typically most important, whereas trace resistivity phenomena such as ohmic loss and skin effect are often more dominant for MCMs. At the PCB and system levels, transmission line effects such as signal velocity propagation bounds are typically the limiting factors, due to the large physical dimensions involved.

Signal distortion, degradation

In addition to accounting for the interconnect issues associated purely with delay, consideration must be given to signal distortion and degradation due to interconnect effects. Such transmission line artifacts as overshoot, undershoot, pedestals, ringing, and multiple threshold crossings are exacerbated by the fast transition times exhibited by very high-speed logic. These effects can strongly influence the behavior of digital circuitry and must be understood to guarantee optimum high-speed operation. At very high frequencies, additional effects such as dielectric dispersion and frequency-dependent losses due to current crowding must be taken into account as well.

The use of transmission line simulation tools as part of the high-speed design methodology can assist in establishing appropriate pre-layout design rules for signal distribution and termination strategies, and can serve as a post-layout signal integrity check on all system nets.

Analyzing the noise

A third area for consideration in high-speed design is the analysis of noise. Noise can arise from a variety of sources, including intersignal coupling (crosstalk), ground bounce effects and electromagnetic interference. Each of these effects is intensified by the use of high-speed, high-slew-rate logic. Analyzing crosstalk requires parametric analysis and simulation of multiconductor transmission line configurations in the presence of signal transients to determine passive line crosstalk amplitudes. Ground bounce analyses require an understanding of the relationship between output pin transitions and device power/ground lead current transients, resulting in ground and supply voltage shifts due to inductive effects at the leads. High-speed EMI effects can be caused by PCB surface traces acting as miniature antennas and radiating into neighboring equipment.

As with signal delay and distortion, the use of transmission line simulation tools for noise analysis as part of a high-speed design methodology can both aid in the establishment of design rules for such layout parameters as trace separation and maximum parallelism and serve as a post-layout verification step by allowing an exhaustive system-level network simulation.

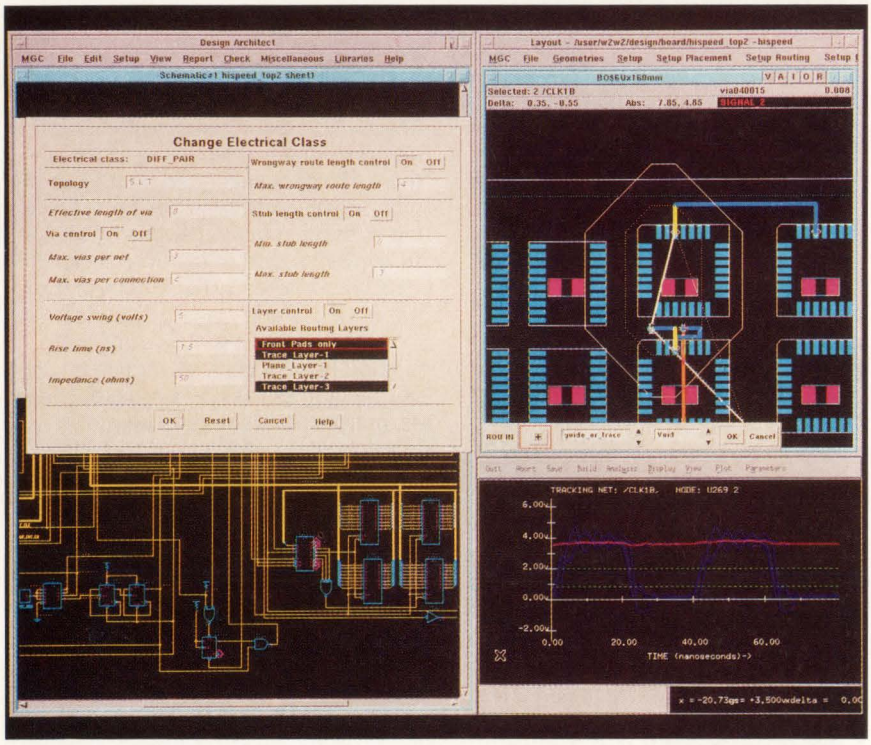
The effective design of high-speed digital systems can be facilitated, then, by adopting design rules and methodologies that support the automated verification of system performance and correctness as early in the development process as possible. A "design for verifiability" philosophy, used in conjunction with appropriate CAE design and analysis tools, can assist in the timely creation of high-quality and manufacturable high-speed designs.

Lawrence M. Rubin, president, Quad Design Technology, Camarillo, CA

edges produced by ECL, says Rücker, make it easier to capture data at these ultra-high speeds.

Mercury Computers (Lowell, MA), a manufacturer of vector-processing add-in boards, uses slew-rate control buffers in conjunction with fast Intel PALs. The boards are capable of 320-MFlops peaks, and their PALs are used for datapath control. Even with a modest 40-MHz clock rate, says Mercury principal engineer Bob Frisch, it's important to ensure that wiring delays are always shorter than transition times. Ordinarily, a high-speed CMOS signal will propagate through a wiring path at a rate of about 1 ft/ns. Heavy fanout loading, however, can slow propagation to about 1 in./ns, creating the possibility of a logic transition occurring faster than the wiring path can propagate it. This will show up as ringing on the signal line. The slew-rate control buffers, however, work to elongate the transitions. "The softer the edge rate," says Frisch, "the better off you are."

"CMOS today is where ECL was two, three years ago," adds Jacob Ben-Meir, a marketing manager in the high-density interconnect (HDI) business unit of Mentor Graphics (Wilsonville, OR). He sees CMOS as still being key to more than 80 percent of digital systems. Even with CMOS, though, you're likely to encounter problems with non-terminated devices whose rise and fall times are less than 1 ns. What's more, if you're working at 50 MHz, says Ben-Meir, you still need to look at activity in the 250-MHz range and above because of the harmonics generated by an unterminated 50-MHz signal. Regardless of the process technology used, the design of high-speed systems remains contingent on physical layout.



Used in conjunction with Mentor's Board Station or MCM Station layout tools, Quad Design's signal analysis suite is designed to interactively reveal transmission line effects—ringing, crosstalk, noise, and others—on particular signal lines. Designers can easily visualize the results of changing the width or length of a trace, rounding a corner or inserting a bypass capacitor or termination resistor into the layout.

Invisible monsters

Without careful attention to layout, you get a series of analog phenomena jokingly referred to as invisible monsters. Engineers may confess to seeing spurious signals that appear out of nowhere, clock edges that perpetually shift and logic devices that run hot with only a small fanout loading. At very high frequencies, there are no limits to the precautions that need to be taken to prevent transmission line effects.

The Convex C3, for example, uses a stripline technique which sandwiches printed circuit conductors between two ground planes. The previous-generation supercomputer, the C2, employed a microstrip technique in which the groundplane is used on only one side of the circuit board. The stripline technique, says Convex's Dozier, results in somewhat lower crosstalk.

Intel, to give another example, provides "reference layouts" to help you when working with its 66-MHz P5 processor. The company also provides simulation models which take into account loading and impedance effects.

Toolsets for designing

There are essentially two kinds of design tools required for high-speed system designs—primarily printed circuit and MCM designs. One toolset consists of very sophisticated timing analysis tools. Such modules are built into a tool suite for PCB layout called Visula HPE (for High-Performance Engineering) from Racal-Redac (Mahwah, NJ).

The other category is analog simulation tools: designed to reveal the "invisible monsters" of ringing, crosstalk, ground bounce, and other transmission effects resulting from impedance mismatch, unterminated lines and casual layout. Many of these monsters are a consequence of density and packaging technology, as well as high clock speed. Mentor's Ben-Meir points out that there are up to 600 I/O pins on some of the newest ASIC devices—a high potential for crosstalk.

A majority of layout tools are driven by electrical connectivity rules, rather than physical design elements like lead length, trace width and spacing. Even performance-driven layout tools which often use timing as the criterion for judging performance will be inadequate, according to Steve Carlson, manager of methodology consulting with Synopsys (Mountain View, CA), a maker of IC synthesis tools, if they don't translate timing into physical elements. "I'll debate with anybody who says their timing constraints work better than their physical constraints in determining an optimum implementation," says Carlson. "The real trick is to translate the logic domain into the physical domain."

New-generation PCB layout tools, however, are attempting to provide tighter integration between physi-

cal layout variables and electrical connectivity. The Allegro-PCB toolset from Cadence Design Systems (San Jose, CA), for example, models the parasitics generated by analog and high-speed digital board layouts. But designers need to specify parallelism rules—that is, the maximum length of parallel lines allowed to prevent signal crosstalk between the lines. Layout engineers also need to specify layer restrictions—whether a board will be laid out with microstrip or stripline techniques. And they need to specify terminations for high-speed devices and subsystems (see "Tool requirements for high-speed digital systems," p 97).

Mentor Graphics has partnered with Quad Design (Camarillo, CA) on analysis tools for high-speed and high-density board layout. Used in conjunction with Mentor's Board Station or MCM Station layout tools, Quad's signal analysis suite is designed to interactively reveal transmission line effects—ringing, crosstalk, noise, and other effects—on particular signal lines. Tool vendors such as HyperLynx (Redmond, WA) are making similar transmission line analysis packages accessible to PC users.

Lossless lines are modeled as inductance, capacitance and resistance models; lossy lines, more typical of the higher-frequency interconnects, are described with impedance. By changing the width or length of traces, rounding a corner or inserting a bypass capacitor or a termination resistor on the layout, you can eliminate such monsters—and the analysis tools will reveal the impact of each incremental change.

None of this works, however, without the availability of good models. Designers working with MCM-L (laminated) technology must have models for stripline and microstrip interconnects, as well as PCB dielectrics. The MCM-D (silicon-on-silicon) technology is characterized by very short interconnects, which should be modeled as a distributed resistance-capacitance network. Contec Microelectronics USA (San Jose, CA) has done considerable work in Spice, modeling the packaging and interconnect effects for very high-speed devices. Quantic Laboratories (Winnipeg, Ontario) similarly has an entire library of transmission line models for PCB traces and cross-sections. But if you're working with MCM-D packaging, you must have usable models for devices as bare dies. Industry consensus is building that, with increased dependence on CAE modeling and simulation tools, IC vendors need to provide accurate models of their high-speed parts—both in their packages and as bare dies for use in MCMs.

Model alliance formed

To encourage the availability of models—at least, of those that can be used with the HSpice Signal Integrity (HSI) toolkit—Meta-Software (Campbell, CA) has formed what it calls the Signal Integrity Alliance. The alliance includes IC vendors such as AMD and Xilinx who are willing to encourage designers to use their parts by providing accurate HSpice models of their high-speed drivers. The HSI toolkit will include a suite of models and analysis components for MCM and PCB design. This alliance will also include companies that provide Spice models of connectors and transmission line models for PCB and MCM elements. ■

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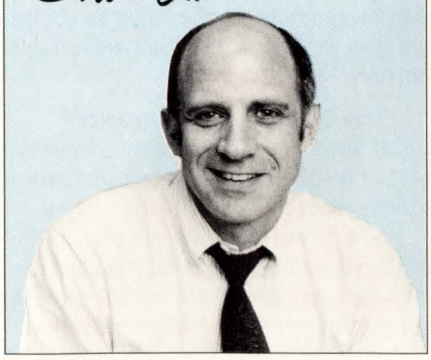
Postscript

Analog transmission-line effects such as ringing, noise, crosstalk, and ground bounce are some of the invisible monsters designers must worry about when they start clocking systems at 50 MHz and higher. The monsters are worrisome because they can destroy the integrity of a digital signal, making it unreadable. All the experts surveyed for this report advise designers to pay careful attention to PCB (and MCM) layout, to use analysis software to visualize the transmission line effects of a particular layout and to iteratively (or interactively) adjust the layout to minimize signal degradation. But as this report shows, a considerable number of design choices must be made before you get to the layout stage.

If you are building high-speed computer systems, you must make strategic choices in system architectures and in components. In the next few years designers will work with 50-, 66- and 75-MHz clock rates. Large caches will be used for instructions and data, replicating some of the supercomputer register chains, and design attention will focus on cache and datapath design.

As an emerging trend, we're seeing self-timed specialty SRAMs used for cache implementation. These include both processor-specific SRAMs—SRAMs specifically designed to interface with the Intel 486 and P5, and the Sparc—and SRAMs with extraordinarily wide word widths (up to 72 bits). For very high-speed cache design, engineers will need to implement custom logic and make choices between CMOS, ECL and GaAs devices.

Steve Ohr



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Calculated risk and aggressiveness pay off for Elan Graphics

The Elan Graphics design team—from right to left, standing: Chandlee Harrell, director of graphics technology; Luther M. Kitahata, manager, graphics system software; left to right, sitting: Dr. Marc Hannah, vice-president and chief scientist; Stephen J. Moffitt, manager of graphics software. Absent from photo: Ta-Wei Chien, director of VLSI engineering. In the center of the photo is the Elan Graphics CPU board.

When the Personal Iris deskside graphics workstation was unveiled to the world back in October, 1988, Marc Hannah, vice-president and cofounder of Silicon Graphics (Mountain View, CA), had already begun thinking about his next design. Offering the fastest workstation graphics for its time and using the fastest CPU available, the Personal Iris was a tremendously successful product. But the workstation market waits for no one. With this in mind, Hannah and the company's entry systems design team adopted an aggressive strategy and set out to challenge the toughest competitor of all: themselves.

With the success of the Personal Iris, the team felt it had gained enough room to take greater risks on the next design. Dubbed the Iris Indigo RISC PC, the new design was targeted as the ultimate desktop visualization machine. The objective of the overall product line was to bring the price under $10,000 for the low end, while maintaining the performance of the Personal Iris, and to push the performance to the limit for the high-end configuration, while keeping the price under $30,000.

The high-end configuration of Iris Indigo was named Elan Graphics. To achieve the desired level of performance within desktop space and price limitations, the team

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employed the most advanced technologies and methodologies available. According to Chandlee Harrell, director of graphics technology and program manager for the project, "One of the key goals of the Elan Graphics program was to be very, very aggressive. We really pushed the limits of architecture design and we really pushed technology—particularly in VLSI processes, design methodologies and packaging technology." The resulting design contains 25 custom ASICs, totaling over 700,000 custom gates—15× the level of integration of the previous product.

Aggressive architecture

Stated in the simplest terms, the function of the Elan Graphics subsystem is to receive graphics commands from the host computer and send them to a high-resolution screen. Residing in the host computer's memory, these commands are part of Silicon Graphics' Iris Graphics Library (GL), a set of over 300 function calls. Users and application developers use these calls to simplify the task of programming highly interactive real-time graphics.

Given the wide variety of graphics algorithms available and the diverse ways in which they're used, the Elan Graphics architecture needed to perform optimized processing of the various types of algorithms, as well as handling several types at once. One of the keys to achieving this was the Geometry Subsystem, composed of four Geometry Engine (GE7) ASICs (see "Elan Graphics: how it works," p 104).

According to Harrell, who conceived the GE7 chip, the GEs operate in parallel using a single-instruction/multiple-data (SIMD) architecture. In other words, commands are sent out to each GE and the ASICs process them in unison. GL commands from the host system are sent to Elan Graphics subsystems over a 32-bit I/O bus. The commands go to a Command Parser that takes and distributes them to the various GE7 chips.

"Geometry Engines are floating-point processors," explains Harrell. "They take a description of a 3-D object and rotate it, scale it to different sizes, add lighting to it. Our Elan Graphics boxes let you look at objects from different angles and change colors. The floating-point engines do the calculations to move things around. The 3-D objects are then mathematically compressed into a 2-D plane so they can be displayed on a monitor. Next, the Raster Engine, another custom ASIC, takes the mathematical descriptions of objects and draws them into a Frame Buffer. The Frame Buffer stores the RGB data value for every dot on the screen. This data value is continuously read out of the Frame Buffer through a RAMDAC, and then it's fed out to the screen."

More goes on in the Frame Buffers than just simple buffering, according to Stephen J. Moffitt, manager of graphics software. "A lot of the window-management operations are done in the X-Map ASICs," he says. "They let you run different kinds of windows all at once. You could be running a 24-bit window, while another window is running in color-index mode. The X-Map chips supply an ID for each pixel that determines which mode the pixel is in."

Moffitt stresses that one of the goals of the architecture is to enable graphics applications to be written so they take maximum advantage of the system by balancing the number of instructions running on the host with those running on the graphics system. "Some applications may be doing more intensive work on the host, which means graphics commands can be taken care of very fast," says Moffitt. "Or, if the application is sending down a lot of graphics commands, the host would normally have to wait for the graphics to complete. Microcode from Elan Graphics is essentially grabbing the GL commands as fast as possible, so you have a host running at one speed, sending commands down the pipeline while graphics are executed at their own rate."

Putting Elan into chips

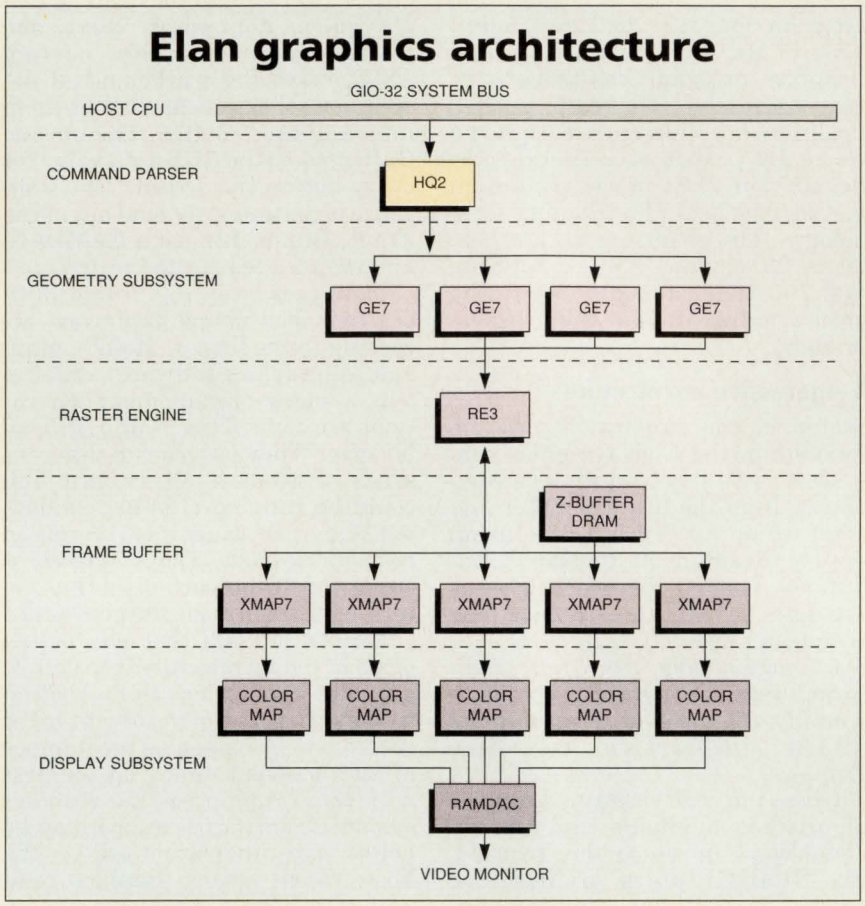
To achieve the mix of integration and performance the company wanted, it was clear early on that the Elan Graphics design would require custom silicon. The design team had to push its Geometry Engines between datapaths, special busing structures and data stores to let the algorithms run fast. They needed to create a Raster Engine that was heavily pipelined to let the system make use of available video RAM bandwidth. "We designed our own chips because the stuff available off-the-shelf didn't live up to the kind of performance we thought we

Elan Graphics: how it works

Aiming to achieve an order-of-magnitude leap in graphics processing power over the highest-performing workstations currently available, designers at Silicon Graphics needed 25 custom processors for their Elan Graphics architecture. These chips are arrayed across five subsystems: the Command Engine (or Parser), the Geometry Subsystem, the Raster Engine (or Subsystem), the Frame Buffer, and the Display Subsystem. Visual data from the RISC host system is processed through five pipelined graphics subsystems before being displayed on the screen.

The RISC-based Iris Indigo host CPU provides the Elan Graphics subsystems with descriptions of 2-D and 3-D objects. These objects, in the form of Iris Graphics Library commands, are bundled with world-coordinate data. Described are the object's geometric position with respect to the viewer, together with various light sources, color, surface properties, and surface-normal vectors used for complex lighting calculations. Elan Graphics takes these objects and performs transformations and other graphics operations to calculate specific pixel values for each of the 1.3 million pixels on the 1280 × 1024 high-resolution display.

Specific duties of each subsystem are as follows:



Command Engine

Elan Graphics is connected to the host CPU via the 32-bit GIO-32 bus and the Iris Indigo graphics interface channel. The Iris commands, combined with world-coordinate data, are passed across the GIO-bus and written into the graphics output FIFO within the HQ2 chip. Latencies in the computation speeds between the CPU-based application program and the Graphics Engines are buffered through the FIFO.

The Command Engine (CE) monitors the output of the FIFO and passes the stream of commands and data down to the Geometry Subsystem. The CE analyzes the command stream to determine the types of graphical primitives being received and to uncover the boundaries between these primitives. Based on this analysis, the CE delegates primitives to each of the four Geometry Engines (GE7s). As data is read from the FIFO into the specified GE7, the Command Engine adds any other required graphics parameters to form a complete packet of parameters for the GE7s to process.

Geometry Subsystem

The vital organs of the Geometry Subsystem are the four GE7 Geometry Engines, which are floating-point datapath ASICs.

Under the control of a centralized sequencer, the custom-designed GE7s execute together as a single-instruction/multiple-data (SIMD) machine. The sequencer addresses a wide microinstruction memory space, the contents of which are distributed to each of the four GE7s simultaneously. Each GE7 operates on a separate primitive, with the four GE7s operating on four primitives concurrently.

Raster Engine

The Raster Engine performs the operations required to boil a vector or triangle description down to the individual pixels to be written to the Frame Buffer. The core of the Raster Engine is Silicon Graphics' custom third-generation Raster Engine chip (RE3). The RE3 accepts initial pixel values and parameter slopes from the Geometry Subsystem and iterates either a vector or a triangle.

Frame Buffer

Elan Graphics includes an optional 24-bit Z-buffer which stores the Z-axis coordinate for each pixel. When hidden-surface removal is performed, the Z coordinate of an incoming pixel is compared to the current depth value already stored in the biplanes. Color values are updated if the incoming Z coordinate is closer to the user's viewpoint, and, therefore, visible.

Display Subsystem

The last part of the Elan Graphics architecture, the Display Subsystem, receives pixel information from the Frame Buffer, routes it through the appropriate display mode, and sends it through the RAMDAC converter for display.

really needed," says Harrell. While Silicon Graphics was an early user of the TMS320C30, a graphics processor from Texas Instruments, the team felt the chip had too many bottlenecks; it also lacked the performance required by the Elan design. "We also looked at the i860, which had come on the market at that time," recalls Harrell, "and there were a lot of bottlenecks in that part as well. We didn't feel satisfied with the performance we could get with it."

Once Harrell, Hannah and others had defined the architecture, it was time to determine what design work would be needed to make the chips. Ta-Wei Chien, director of VLSI engineering, played a major role in selecting the aggressive methodologies and technologies that would fit the design strategy.

A VHDL first?

"We looked at the problem and said, 'In this scheduled time frame how can we achieve this kind of aggressive architecture?' " says Chien. At the time there were two methodologies available for synthesis—Verilog and VHDL. "We chose VHDL because we believed it would be the standard." Using tools from Synopsys, VHDL synthesis was carried out to do the basic chip design, and it was also used to do simulation. "We started in 1989—the Indigo product is probably the first VHDL design-based workstation," claims Chien.

VHDL synthesis and simulation were critical to achieving the team's integration goal of making a huge number of gates work together. While its previous product line used 50,000 design gates, the Elan Graphics design team employed 700,000 gates, or 3 million transistors—and these were not simple gate configurations. "We're really pushing the edge of the technology," says Harrell. "The HQ2, with its 80,000 gates of control logic, was very hard to design. The GE7 is an embedded master/slave ASIC—a new technology. And the RE3, at 100,000 gates, was the biggest chip at that time. For a chip that runs at a clock rate of 50 MHz, that's a lot of gates."

Because the chips were so big and complex, the ASIC technology choices were important, but time constraints were also a factor. "Most of the chips we designed were gate arrays, because we needed quick time-to-market," says Chien. "Gate arrays are easier to change and debug at the last moment."

One chip, the GE7, however, required a different approach. Instead of being a gate array, a mixed-array technology was used for it. "The basic idea is that we have a floating-point unit coupled with a lot of memory in a standard cell," states Chien. "And the surrounding control logic we can put in as a gate array." The result is a mixed technology using both gate arrays and standard cells. "So we have the performance we want, as well as the density we want, and we can get to market quickly," he adds.

Another issue was selecting a chip vendor to build the chips. After talking with several, the team settled on LSI Logic and used its 1-µm CMOS gate array technology. "We needed a vendor that had automatic test pattern generation [ATPG] capability," says Chien. Silicon Graphics was actually LSI Logic's first customer for its ATPG process.

Simulating it all

The VHDL simulation played a key role in the design process. Simulation was done at different levels—simulation of the VHDL single-chip model, as well as simulation of the VHDL multichip models within the larger VHDL model. When those models appeared to work, they were translated into LSI Logic netlists to ensure that the vendor netlist performed in the same way as the VHDL netlist.

Using a complete system simulation methodology required involvement from not only the hardware and chip designers, but from the software designers as well. The entire system was run as one simulation model, and the team was able to run real code through it. "We mixed VHDL with C code and created sockets. The key benefit of this level of simulation is that it lets you identify all the interface problems that you may have missed and the various architectural 'gotchas' that you might not notice when going through the initial design," says Harrell. The VLSI groups, the hardware systems, software groups, all had to come together to make this happen.

Luther M. Kitahata has emphasized the point that getting together early in the design process with software people really makes for a better system mix. Kitahata is the

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graphics system software manager responsible for the operating system graphics support and X Windows systems support. "The simulation environment lets us start writing code before hardware is available," he says. "Since we [the software engineers] participated in setting up the hardware simulation, it was great because a lot of software people were able to gain an intimate knowledge of how the hardware worked."

A situation came up during the design cycle that clearly demonstrated the value of early involvement by software engineers. Most of the emphasis was originally put on the Graphics Library portion of the system, when it was becoming fairly obvious that X Windows was on its way to becoming a standard. Because of the simulation, it wasn't too late to modify the graphics architecture to make Elan Graphics into a good X Windows system as well. For example, hardware was included that supported multiple types of screens; also offered was the ability to switch between screens. The kernel was modified to allow for X-related issues—such as handling high-speed transfers of pixels, for example.

While Moffitt agrees that simulation was a good way to integrate hardware and software, he points out that the technique still has some limitations. "The goal was to make the simulator as close to the hardware as possible," says Moffitt. "As we found bugs, we were updating the simulators to match the hardware. Since these are behavioral simulations, not gate-level simulations, they're not going to be exactly like the hardware."

It wasn't possible to simulate some aspects of system behavior. "We could test the context-switching microcode, but we didn't do the simulation of the interface between the Frame Buffer and the microcode," he says. "We also didn't add a return path. Sometimes you have to get state information out of the microcode in the Frame Buffer. That wasn't part of the simulation package, though we may add that next time around."

Despite its limitations, however, the simulation offered a look into the operation of the larger chips that would have been impossible otherwise. For example, simulation provided a view into the operation of the RE3 chip, with its 100,000 gates. Using VHDL simulation, the team created an image on the screen that looked exactly like the one that came out of the hardware, pixel for pixel.

Did anything unexpected come up during the simulation? "It was unexpected that the process worked," jokes team leader Harrell. "Seriously, at times while we were doing it, we thought the project was so complex that it would be amazing if it all just worked. It was a very aggressive design, and we were taking risks, but it all made sense that it would work. With 700,000 gates, it was very complex architecture, and we had to have everything covered—and luckily we did."

Lessons learned

Summing up what the Silicon Graphics team learned from designing the Elan Graphics system, Harrell emphasizes the value of calculated risks and aggressiveness, as well as having front-line goals. Also, the teamwork aspect, letting each person feel he or she had equal responsibility and that the product was his or her "baby," was important. "We've learned over and over again that calculated risk and aggressiveness do two things," says Harrell. "One, they provide a great environment to work in. It's easy to get psyched and excited about the project. Two, you get a great product. It's definitely an approach we'll take again." ■

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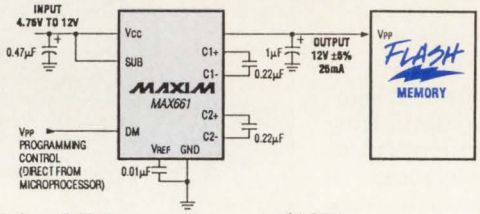

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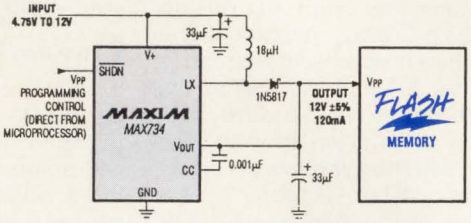

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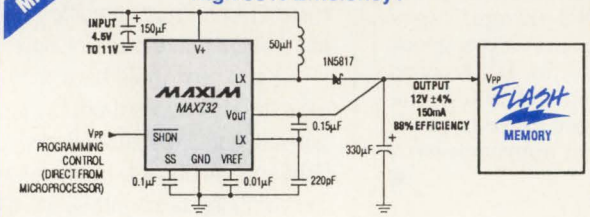

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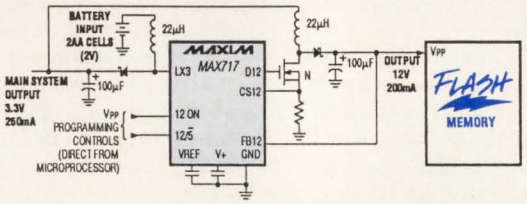

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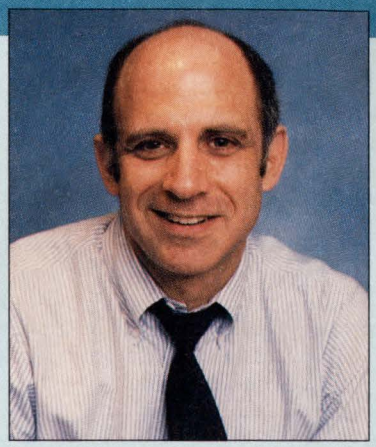

A&M-S: The place to see and be seen

It might be presumptuous to identify the second annual Analog and Mixed-Signal Design Conference as "the place to see and be seen" for manufacturers and users of mixed-signal ICs, ASICs and design tools. There are other forums and events. But the technical conference—jointly sponsored by *Computer Design* and Miller-Freeman publications—seems to be attracting the best minds on mixed-signal technology.

As a result, the program for this year's conference, scheduled for October 28-30 in Burlingame, CA, will showcase some of the best mixed-signal toolsets, modeling techniques, ASIC cell library developments, and applications know-how that companies have to offer. What my DOS computer files identify as A&M-S may not yet be an industry event, but it's certainly beginning to feel that way.

All the big guns in analog and mixed-signal IC technology are sending speakers: Analog Devices, AT&T Microelectronics, Burr-Brown, Gould AMI, Harris Semiconductor, National Semiconductor, Signetics, Texas Instruments, and so forth. All the tool makers are represented: Analogy, Cadence Design Systems, Dazix, Mentor Graphics, Racal-Redac, and Viewlogic Systems. Even manufacturers whose expertise is specialty analog rather than mixed signal—Elantec and Linear Technology, for example—will send speakers this year.

While last year's Mixed-Signal Conference in Santa Clara had similar support from semiconductor manufacturers, the presentations were dominated by ASIC concerns such as how to check out a cell library, what's the best process technology for mixed-signal designs, and how to work with an ASIC vendor. This year will offer a much stronger program in mixed-signal IC applications. The range includes computer graphics and video (two papers), disk drive read channels and servos (three papers), wide-band amplifiers (four papers), and digital audio (three papers). There will be at least three presentations on sigma-delta converters and at least two presentations on switched-capacitor filter design and simulation.

In the CAE tools area, A&M-S will also showcase mixed-signal design-for-test—an emerging trend—and will feature a progress report on AHDL. The panels on mixed-signal modeling and simulation issues will demonstrate consensus as well as controversy. Benchmarking analog and mixed-mode simulators and simulation backplanes are among the issues to be debated. The technical program, I believe, represents a good cross-section of current concerns among designers and users of mixed-signal circuits.

Balanced presentations

As was the case last year, presentations by ASIC vendors this year will be balanced to show alternatives among fabrication processes. TI's Lou Hutter will do the honors on BiCMOS, Bill Gazeley of NCR Microelectronic Products will do a talk on CMOS ASIC design issues, SGS-Thomson's Carlo Cini will return to talk about smart power processes (how to build a power op amp), and Harris' Brian Matthews will discuss the possibilities of the company's ultra high-speed bonded-wafer process. But the almost naive tone of last year's ASIC presentations (for example, "How to work with an ASIC vendor") has been replaced by a more sophisticated applications orientation (e.g., "let me show you something interesting you can build"). To give one example, a proposal for an unusual ASIC library cell—an optical sensor/amplifier element—will be presented by TI's Lisa Schartz in the context of a rotary digital encoder application. J. Ron Gadway, similarly, will concentrate on wireless network circuit applications of Fujitsu Microelectronics' radio-frequency custom components.

One of the best proposals on process technology, in fact, will be given by Steve Moore of GEC Plessey Semiconductors. Moore will describe partitioning alternatives for disk drive read channels. With disk drive form factors shrinking, there's pressure on semiconductor makers to build a single-chip disk drive. But not everything can be done in CMOS, or even BiCMOS. If Steve Moore does his job well, he'll present a disk drive circuit and discuss some of the ways it can be partitioned to utilize process technologies efficiently.

Capturing a trend, Gus Richard and newcomer Ha Nguyen of VLSI Research are collaborating on a paper

exploring the consequences of the 3.3-V logic standard for mixed-signal IC designs. There will be quite a few presentations on the application of specialized digital technologies to the problems of analog signal processing, a technology I call "analog emulation." Analog Devices' Doug Grant and two people from ADI's Limerick, Ireland facility, Mike Byrne and Mike Curtin, will do presentations on sigma-delta technology. TI's Daryl Sartain will show the application of sigma-delta to digital audio circuits. Philips/Signetics' Enjeti Murthi will be the first to do a presentation on digital disk drive read channel implementation, another variation on the analog emulation theme.

There will be two presentations on DSP algorithm and IC filter development. One, in fact, will come from the Warren, NJ start-up Star Semiconductor, and will be given by either Steve Sheslow or Star founder Jeff Robinson.

Among the most popular sessions last year were those that offered digital designers basic instruction on analog thought processes. One repeat from last year will be Kerry Lacanette's half-day (3 1/2-hour) tutorial on monolithic analog-to-digital converters. (Kerry Lacanette, some of you may be aware, was a Bob Pease protege at National Semiconductor.)

Another repeat from last year will be Bob Leonard's talk on static A/D converter specifications. Though this will be presented as a tightly focused one-hour lecture, Bob's presentation is based on a popular three-hour seminar he gives for Datel. A half-day tutorial on analog filter design will be given by Geert De Veirman and Richard Contreras of Silicon Systems, Inc. Both are well published in the field of filter topologies.

Also popular last year were the tutorials on Spice modeling and an introduction to transmission-line analysis. This year, the Spice tutorial will be given by Jeff Deutsch of Deutsch Research. Jeff, you may remember, developed some of the MOS relaxation algorithms for Spice at Berkeley, where he got his Ph.D.; he remains one of the most accessible authorities on Spice. The transmission-line tutorial will be given by Al Wexler of Quantic Labs, and will be supported by hands-on simulation exercises. Engineers will have a chance to sit at an HP/Apollo workstation, input a circuit layout and examine some transmission line effects for themselves. Al's talk will

be based on a half-day teaching seminar Quantic conducts for its customers.

Among Al's competitors in transmission line analysis software—he identifies them as "friends"—are Jon Powell of Quad Design and Paul Wang of Contec Microelectronics USA, who will be doing specialized presentations on behavioral modeling and pole-zero analysis.

An update on AHDL

In the CAE tools area, interest in mixed-signal test and design-for-test (DFT) is running quite high, judging by the number of presentations to be offered at this year's conference (no less than four). Steve Dollens of IMP and Mani Soma of the University of Washington—co-chairs of IEEE 1149.4, the committee charged with assembling a scan test standard for mixed-signal testing—will do a stand-up presentation, essentially a progress report, on the development of the standard. This will perhaps be one of the first public presentations on 1149.4 outside the International Test Conference and assorted DFT meetings. Dollens and Mani's presentation will be supplemented by one from Richard Hulse of Gould AMI Semiconductors, which participates in the 1149.4 committee and has begun developing a scan test methodology for mixed-signal ICs. Another 1149.4 participant, Stephen Bateman of Cadence, will do a presentation on the use of tester models with analog and mixed-signal simulators—a process guaranteed to improve DFT. Luke Hsieh of LTX, similarly, will do a presentation on tester models that can be used in the design environment.

The popular sessions on mixed-signal simulation and modeling, meanwhile, will be supplemented with panels and discussions. To give us an update on AHDL—the analog hardware design language—*Computer Design* is assembling a panel of experts. Prominent among them will be David Smith of Analogy, whose company is well represented at MHDL working group meetings and whose Mast modeling language is considered a candidate for an MHDL or AHDL standard.

MHDL, a microwave hardware description language being developed under a contract from DARPA, was previously endorsed by SCC-30, the IEEE stand-

ards coordinating committee charged with exploring a high-level design language for analog, as a possible driver for development of an AHDL. Since the SCC-30 endorsement 18 months ago, the boundaries and relationships between MHDL, AHDL and, yes, VHDL, have become increasingly confused. To shed light on the issue, we hope to hear from Dave Barton of Intermetrics, the contractor charged with developing the preliminary MHDL language specification for Darpa; Mark Brown of CLSI, who is collecting proposed analog extensions to VHDL; and Cadence's Andrei Vladimirescu, who participates in SCC-30 meetings. The panel will be chaired by a firm believer in AHDL, *Computer Design*'s Barbara Tuck.

We made a promise at last fall's conference that can only be partially kept this year. During a panel on the BCTM challenge—the simulation exercise conducted at the 1990 Bipolar Circuits and Technology Meeting—we said we would obtain a "benchmark" circuit, distribute it to simulation tool vendors (and others interested in participating), and encourage them to present their results at this year's conference. That suggestion, we now believe, would be premature without a consensus as to what a simulation benchmark is intended to show.

We can say we are looking to assess speed and accuracy, but as the BCTM presentations and subsequent arguments revealed, very little of this will allow an easy "apples-to-apples" comparison. What does it mean when one simulation run took 9 min 13 s on a VAX, another took 6 min 56 s on an HP/Apollo, or a third took 3 min 29 s on a Sun Sparc—but it took three days to tweak the netlist? There is a part of me that agrees with Shawn Hailey of Meta-Software who believes that as long as you're not tying up a machine for hours at a time, simulation speed may not be the most important criterion. Without a standardized benchmark, we'll undoubtedly get a repeat of BCTM, where panelists try to do a 15-minute summary of a process that may have taken months to complete, something that comes across as a "feel-good" session but leads to behind-the-scenes sniping and bitterness as panelists—ordinarily, business competitors—begin to posture over "who won."

As a consequence, the panel session on benchmarking simulators will attempt to encourage agreement among simulation tool vendors rather than controversy—agreement as to what constitutes a good benchmark and why. Participants in this session will include Mark Chadwick of Analogy (it was his idea, actually), Dündar Dumlügol of Cadence, Graham Bell of Microsim, and others. If you've got a circuit that might make a good industry-standard benchmark, bring it to the session. The discussion will either be chaired by me or Mike Donlin of *Computer Design*.

There'll be a hopefully heated panel discussion on simulation frameworks. The panelists include Hal Alles of Mentor Graphics, James Spoto of Cadence, Harish Sarin of Dazix/Intergraph, and Graeme Nash of Racal-Redac. Each of these companies is working on getting multiple simulators to play together in the same environment, but all are taking somewhat different approaches to the problem. (Harish Sarin, in fact, will be presenting an adaptive backplane arbitration algorithm he developed in a separate session.)

In the past, I've thanked my panelists for participating by taking them to lunch or dinner before the presentations. We've used the meal together as an opportunity to do last-minute organizing, but I'm not sure if this is good for debating. I've found that when the panel actually begins, the presenters, having dined together, are feeling very warm and conciliatory toward each other. Perhaps I should take them to lunch *after* the session.

Stephan Ohr is president of Indian Forest Research and editor of the monthly newsletter, Mixed Signals.

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INTEGRATED CIRCUITS

Video op amps get flatter and faster

Jeffrey Child, Associate Editor

To build video amplification circuitry into Intergraph's high-performance color workstation monitors, designers have traditionally found discrete transistor-based circuits to be the most cost-effective. But now that video op amp vendors have improved the performance and dropped the price of their devices, Intergraph engineers have decided to design them into the company's next-generation color monitors.

As the electronics world shifts from analog to digital, video monitors are one of the last pure analog systems you're likely to find these days. In monitors, however, as well as in other video applications such as professional video, multimedia and high-definition television, video op amps are now providing solutions where only circuits consisting of several discrete components could do the job in the past.

Recognizing video as a large and growing market, op amp makers are defining parts with greater sensitivity to the needs of this area. Companies are striving to offer a mix of speed, low distortion and low power at a price that will play in high-volume commercial applications. To accomplish this, op amp makers are relying on processes such as complementary bipolar and dielectric isolation to produce competitively priced devices that offer flat frequency response at ever higher bandwidths.

Two extremes

For some time now, mainstream video monitors such as VGA displays have been using specialized ICs that handle the complete video amplification function, all the way from the low-amplification input to the signal that drives the CRT. This approach has some speed limitations that have forced designers of high-end workstation monitors to stick to building amplifier circuits based on discrete transistors and filters using resistors and capacitors. As video op amps have improved in performance and dropped in price, however, designers of high-end monitors are beginning to consider using designing in op amps.

Basically, the video interface between a workstation and a monitor consists of a low-level RGB video feed to the monitor. It produces a signal that has to be amplified before it's applied to drive the CRT.

While most other workstation vendors purchase their monitors on an OEM basis from manufacturers overseas, Intergraph (Huntsville, AL) still designs and manufactures its own color graphics monitors. "In the past, we've looked at video op amps and felt their performance was not adequate, and their price was too high to play in our environment," says Chris Thomas, executive technical manager of advanced display design at Intergraph. "In the last year, the performance of op amps from a number of vendors has improved significantly, and the price has come down quite a bit—to where that seems to be a very viable approach. In the past, we've designed discrete transistor amplifiers because that's allowed us to get a level of performance at a cost that's attractive."

Red, green, blue together

For its part, National Semiconductor (Santa Clara, CA) has had chips out for several years that handle all the main video application chores for a low-end color monitor. The company's LM1203 and LM1204 chips perform all the pre-amp contrast, dc restoration and differential drive adjustments for all three color channels. To address high-performance requirements, National has announced the LM1202, a 230-MHz integrated video amplifier. Because of the power dissipation problem, the LM1202 is a single-channel part, although it still integrates the same set of functions as the LM1203 and LM1204.

Because a separate LM1202 chip is needed for each color channel (red, green and blue), the problem of making the chips work together efficiently had to be addressed. "The problem when three independent color channels drive separate electron guns is that everything has to track very closely over the full range of speeds, with the color matching and the gain adjustment within range," says Peter Himes, segment marketing manager at National. "That's very difficult to do, especially with the discrete approach using transistor arrays and sample-and-holds." To address this point, the LM1202 has been specifically designed so that the contrast adjustment, or gain control, can be tied together across three separate chips. In this way, one control slaves three separate chips.

Model	Unity-gain Bandwidth (MHz)	Max slew rate (V/μs)	Typical settling time to 0.1% (ns)	Gain flatness (MHz to limit of 0.1 dB)	Differential gain error (%)	Differential phase error (degrees)	Quiescent power supply (mA)	Output drive (mA)	Supply voltage range (V)	Price
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AD811	140	2,500	25	35	0.01	0.01	16.5	150	±4.5, ±18	$8.35 (100s)
AD817	50	350	50	—	0.03	0.08	6.0	30	±2.9, ±18	$1.79 (100s)
AD830	60	530	25	10	0.05	0.08	14.4	50	±3.5, ±18	$2.95 (100s)
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WB05	70	15,000	22	—	2	—	36 (3.5 sleep mode)	1,500	±5 to ±15	$79.80 (100s)
Burr-Brown 6730 S Tucson Blvd, Tucson, AZ 85706 (602) 746-1111										**Circle 303**
Buf 600	650	3,400	—	94	0.5	0.02	3	20	±5	$5.68 (100s)
Buf 601	820	3,600	—	119	0.4	0.025	6	20	±5	$5.83 (100s)
OPA620	300	250	13	43.5	0.05	0.05	23	150	±5	$8.85 (100s)
OPA622	230	1,600	—	33	0.2	0.05	3-8	70	–5	$7.10 (100s)
OPA623	280	2,000	—	41	0.05	0.05	6	70	±5.5	$4.40 (100s)
OPA660	500	3,000	25	72.50	0.06	0.02	20	15	+5	$5.85 (100s)
OPA678	200	350	15	29	0.03	0.07	26	40	–5	$5.95 (100s)
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ChC411	235	2,300	15	30 (0.05 dB)	0.02	0.03	11	70	±15	$4.99 (100s)
Datel 11 Cabot Blvd, Mansfield, MA 02048 (508) 339-3000										**Circle 305**
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AM-1435	1,000	250	20	—	—	—	30	14	±12 to ±16	$95
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EL2030	120	2,000	40	30	0.01	0.01	15	65	±5 to ±15	$3.25 (100s)
EL2070	200	1,600	10	60	0.02	0.01	16	70	±5	$4.95 (100s)
EL2073	200	250	13	50	0.01	0.015	21	70	±5	$4.95 (100s)
EL2090	100	600	50	20	0.01	0.02	14	70	±5 to ±15	$6.75 (100s)
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HFA1130	850	2,500	11	100	0.02	0.05	21	60	±4.5 to ±5.5	$9.95 (100s)
ILC Data Device 105 Wilbur Pl, Bohemia, NY 11716-2482 (516) 567-5600										**Circle 308**
SL9999	400	1,300	24	120	—	—	17	50	+12, –5	—
Linear Technology 1630 McCarthy Blvd, Milpitas, CA 95035-7457 (800) 637-5545										**Circle 309**
LT1223	100	1,000	—	—	0.022	0.12	—	50	±18	$2.85 (100s)
LT1227	140	1,100	50	—	0.01	0.01	250	30	±18	$2.45 (100s)
LT1229/30	100	1,000	—	—	0.04	0.1	—	—	±18	$3.95, $7.25 (100s)
Maxim Integrated Products 120 San Gabriel Dr, Sunnyvale, CA 94086 (408) 737-7600										**Circle 310**
MAX404	80 (gain=2)	500	70	30	0.05	0.01	30	50	±5	$2.65
MAX405	180	650	35	20	0.03	0.01	35	60	±5	$4.25
MAX440 MAX441 MAX442/3	160	370	65	—	0.04	0.03	40	40	±5	$8.95 $5.90 $4.45
National Semiconductor 2900 Semiconductor Dr, Santa Clara, CA 95052-8090 (408) 721-5000										**Circle 311**
LH4117	150	2,500	—	50 (0.3 dB)	0.01	0.01	45	200	±12 to ±18	—
LH4118	250	2,500	15	50 (0.3 dB)	0.01	0.1	25	100	± 5 to ±18	$18.00 (100s)
LM1202N	230	2,666	—	—	—	—	48	12 to 15	8 to 12	$6.50 (100s)
LM1203AN	100	1,212	—	—	—	—	70	12 to 15	10 to 12	$4.00 (100s)
LM1204N	150	1,538	—	—	—	—	100	12 to 15	10 to 12	$4.75 (100s)
LM6181	100	2,000	50	—	0.05	0.04	7.5	100	±5 to ±15	$2.95 (100s)
Raytheon, Semiconductor Div 350 Ellis St, Mountain View, CA 94043 (415) 968-9211										**Circle 312**
AMP05	160	1,400	20	—	—	—	3	15	±5	$10
Siliconix 2201 Laurelwood Rd, Santa Clara, CA 95056 (408) 988-8000										**Circle 313**
Si582	180	700	12	—	0.1	0.01	15	50	±7	—

INTEGRATED CIRCUITS

Since video encompasses a wide range of applications aside from monitors, choosing the best mix of specifications depends a lot on what's being done. To be appropriate for video, a part must have more bandwidth and a higher slew rate than a general-purpose op amp. While ordinary op amps offer bandwidths of up 2 MHz, broadcast video standards such as NTSC (the U.S. standard) require a minimum of 5 MHz. For such uses, a part with low differential gain and phase error means less distortion in the video image.

An application such as high-resolution graphics is another place where video op amps can play a key role. Here, a different type of distortion is most critical—the distortion introduced by gain flatness limitations.

In other words, when high-performance video processing is done on the separate red, green and blue signals, the flatness of the gain is especially important.

Geared for video

"Video signals are very complex and have spectral elements at many different frequencies," says Chris Henningsen, marketing manager at Harris Semiconductor (Melbourne, FL).

"If you don't have a good low differential gain and phase, it really shows up as distortion or color shifts in your video image."

—Jay Cormier, Analog Devices

"If your amplifier has a certain gain for one frequency and a different gain for another frequency, then the signal will be distorted by going through the amplifier. Certain portions of the spectrum will be amplified or attenuated more than others. You want all the spectral components to go through the amplifier equally." Achieving this is easier if the op amp provides flat signal response at high bandwidth.

As the accompanying table shows, a number of vendors offer parts with unity-gain bandwidths well over 100 MHz at high slew rates. But these high speeds usually reflect a 3-dB bandwidth measurement, and therefore don't necessarily indicate a flat response at high frequencies. Video designers should also look at the gain-flatness specification, which describes the frequency at which the op amp's gain doesn't vary more than ±0.1 dB. High gain flatness lets you avoid adding circuitry to filter or adjust the signal.

Harris' flagship family of op amp products is the HFA1100 series. With

a 3-dB bandwidth of 850 MHz, it's the world's fastest family of monolithic op amps, according to the company. The series also features a slew rate of 2,500 V/μs, and a power consumption of 20 mA. Gain flatness, to a limit of 0.1 dB, is rated at 100 MHz.

Phase and gain

Jay Cormier, new product marketing manager at Analog Devices (Norwood, MA), agrees that gain flatness is an important op amp specification, but points out that differential gain and phase shouldn't be overlooked. "If you don't have a good low differential gain and phase," he says, "it really shows up as distortion or color shifts in your video image." Video systems usually have several stages; because differential gain and phase errors are additive, the lower they are, the better.

With this in mind, Analog Devices made the AD811, the company's ultimate video part, to have the lowest differential gain and phase possible. Its differential gain is 0.01 percent, while differential phase is 0.01°. The part also offers a gain flatness specification of 35 MHz. A bandwidth of 140 MHz is required to achieve that flatness. Targeted for HDTV and professional video applications, the AD811 also offers a slew rate of 2,500 V/μs, and a settling time to 0.1 percent of 25 ns.

Another video-related feature of the AD811 is its ability to drive cables effectively. Because video signals are typically sent between several systems—such as from cameras to VCRs to displays—op amps often have to drive those signals over one or more cables. At a minimum, you typically have to drive one back-terminated cable with 150 Ω of effective resistance. In many designs, several cables are driven by op amps. For that reason, the AD811 was designed with a high output current of 100 mA so it can drive multiple cables. It will drive at least two cables at the specifications shown on the chart, and up to six cables with some degradation in performance.

Prices continue down

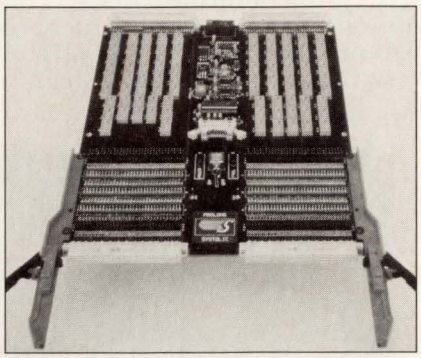
One clear trend in video op amps is a steady decline in price. As a result, the technology is becoming available for more and more applications. "If you looked at the price of video amplifiers three years ago," says Bill Gross, design manager at Linear Technology (Milpitas, CA), "you'd be lucky to get one for $4 or $5 in quantities of 100." Exemplifying the attractive performance levels of today's video op amps, Linear is offering the LT1227, its 140-MHz op amp, for only $2.45 in 100-quantity lots. The LT1227 features differential gain and phase error of 0.01 percent and 0.01°, respectively. The part has a slew rate of 1,000 V/μs and operates from a single 5-V power source up to ±15 V.

COMPUTERS & SUBSYSTEMS

Extender board brings live insertion to VME systems

While full-fledged live insertion on VME may still be some way off, VMetro (Houston, TX) has a head start on the capability with its latest Prolong extender board. The extender provides for live insertion and removal of any VMEbus board into or out of a system with no disruption of signal integrity. The board, available through VMetro but manufactured by Systolic in Sarl, France, uses a novel system of active relays. The isolating relays are activated by a simple on-board toggle switch, or under external control using TTL signals.

According to VMetro vice-president John Simpson, the relays have a super-low-inductance armature and minimal-inductance contact leads to minimize any contact bounce or spurious effects from switching transients. "In fact," says Simpson, "we've checked the system out with two bus analyzers, one in the system and one in the Prolong extender board, and we were unable to find any signal anomalies during insertion or removal cycles."



VMetro's Prolong live-insertion board extender provides active relays which properly sequence VMEbus signals, power and ground so that boards can be inserted into an operating system with no disruption to the existing system. It also has many of the same features as conventional extenders, such as isolating jumpers on all P1 and P2 signals, male DIN sites before and after the isolating jumpers, and easy-to-use ejector/insertion levers.

Keeping the power on

On-board circuitry in the extender monitors the power-on sequence and prevents the module being installed from introducing shorts into the system, or from drawing excess current. Further sequencing of the signal relays minimizes loading on the bus, says Simpson. In addition, it bypasses critical daisy-chain signals during power-on to ensure that the board doesn't generate potentially destructive signals, such as SYSRESET (system reset), onto the bus. Once bus connection is verified, the connection sequence is invoked, assuring a glitch-free power-up.

The board also contains a complete set of logical DIP switches which let you disconnect any signal or set of signals from the board to be inserted. For example, this would let you test a board supporting VSB in a system which may have a proprietary set of signals on its P2 connector. You can disable the VSB signals by disconnecting rows A and C on the P2 section. Other signals (including power and ground) and other voltages (such as ±12 V) can also be isolated from a particular board.

While a toggle switch is used to activate and deactivate a board connected to the Prolong extender, the optional TTL control element can also be used, and is suggested for automated test applications. In such use, a board under test is inserted into the extender and an operator keys in a "go" signal. The system can then automatically sequence through a test routine and indicate that the unit has passed or failed the test—and if the latter, why—then automatically remove power from the board, so it can be withdrawn and another inserted.

Variety of uses

The Prolong extender was initially designed as an aid for VMetro's VBT-321B Advanced VMEbus Tracer. It serves well in support of on-line field service applications where power cycling the system to install the VBT-321B isn't possible. Similarly, the live-insertion extender eliminates the need for forced system shutdown to install the VBT-321B during critical development and test sessions in lab environments.

While the Prolong extender is suited for use with bus analyzers and in automated test facilities, it can also be invaluable in other applications where CPU, I/O or memory boards have to be inserted into an operating system. The ability to jump in or out of the available signal lines provides you with a wealth of options for testing different boards.

The Prolong extender also provides many of the features and benefits of conventional extender boards, including male DIN sites before and after isolating jumpers and easy-to-use ejector/insertion levers which significantly reduce the effort of mounting and removing modules. The extender board is available now from VMetro, and carries a list price of $2,590. — *Warren Andrews*

Prolong extender card at a glance

- Allows live insertion
- Install CPU, memory and I/O without disrupting power
- Use with bus analyzer without disturbing cycle operations
- Active system sequences P1 and P2 connectors
- Bypasses daisy-chain during power-on
- Isolation jumpers on P1 and P2
- Male DIN sites before and after jumpers
- Easy-to-use ejector/insertion levers

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ASICs & ASIC DESIGN TOOLS

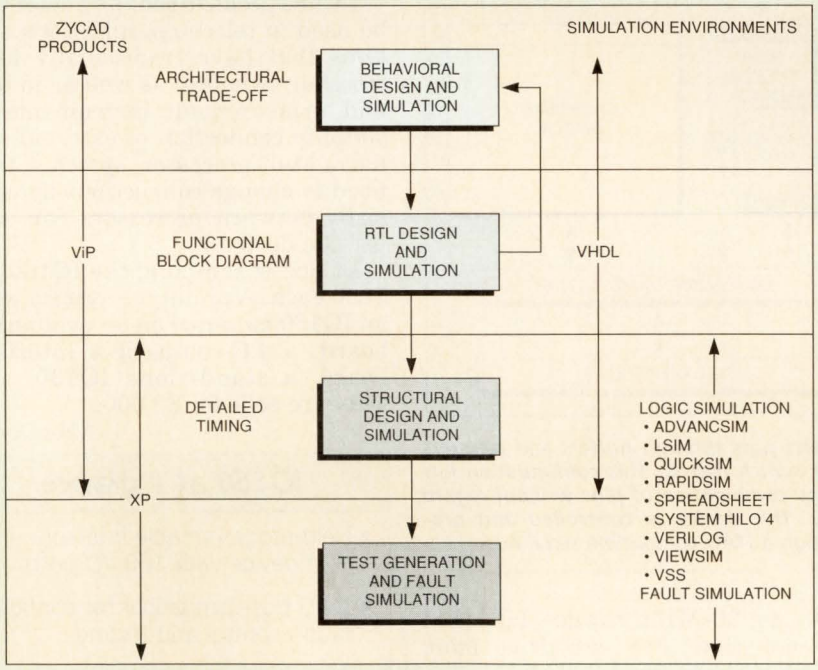
Simulation accelerator speeds behavioral-level VHDL

Unlike current simulation accelerators, which only speed the execution of synthesizable register-transfer-level and structural-level VHDL, the VHDL Instruction Processor (ViP) from Zycad accelerates VHDL at all levels of abstraction, including the behavioral level. By combining superscalar parallel computer architecture and hardware acceleration technology, a single-board ViP offers the performance of a 70-Mips workstation such as the HP-750, claims Zycad. And a 16-board system can execute as much as four million lines of code.

"Up until now, VHDL has always held promise as a way to speed up large-system designs, but that promise hasn't been substantial in the real world because of performance issues," says Zycad president and CEO Phillips W. Smith. "For the first time, designers will be able to accelerate all levels of their VHDL designs, giving them the freedom to explore its full power and flexibility."

ViP is designed to work with leading VHDL software simulators. So far, Cadence Design Systems, Dazix, Synopsys, Vantage Analysis Systems, and Viewlogic Systems have announced they'll be offering their VHDL simulators integrated with ViP through a procedural interface (PI). The PI lets the ViP software perform code generation, design partitioning and loading, and also lets the ViP and VHDL simulator run concurrently.

ViP and XP cosimulate



ViP accelerates VHDL at all levels of abstraction—behavioral, RTL and structural—and complements the older XP gate-level accelerator and test generator/fault simulator.

Processor network

The ViP architecture is a hierarchical network of high-performance processors. At the system level, as many as 16 ViP accelerator boards can be connected through a high-speed backplane. Each ViP board contains seven superscalar processors, each with private memory, that work in parallel. Four sequential processors perform the process execution phase of the simulation cycle. A pair of signal-system processors perform signal evaluation and driver updates. And a single communication processor is responsible for synchronization, message passing and VHDL simulation cycle tasks.

The processors are connected by high-speed buses. The signal-system processors, for instance, communicate over a 350-bit-wide bus.

Though these seven processors don't achieve 100-percent parallelism, their combined performance gives the ViP a strong advantage over a general-purpose workstation.

On top of that, since ViP executes only VHDL instructions, its arithmetic logic unit can incorporate VHDL-specific constructs to speed execution. These constructs include type conversion functions and multivalue logic arithmetic.

Both the ViP and Zycad's XP gate-level accelerator fit into the same cabinet, and they can cosimulate through the backplanes of EDA partners. The XP accelerates non-VHDL simulations and is also used for fault simulation.

First product shipment of ViP is expected in the first quarter of 1993. Zycad's starting price is $60,000.

— Barbara Tuck

ViP simulation accelerator at a glance

- Accelerated VHDL at behavioral level
- Superscalar parallel computer architecture
- Processors connected by high-speed buses
- With 16 boards, executes up to four million lines of code
- Five VHDL software simulator vendors integrating into VHDL environments through procedural interface

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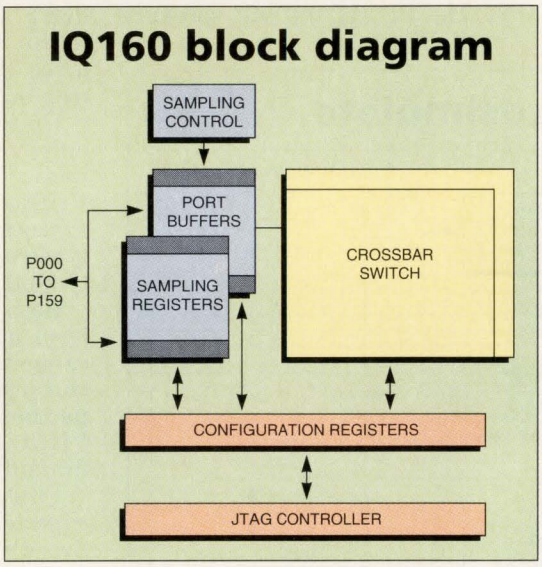
CAE/CAD TOOLS

JTAG device provides programmable interconnect capability

Startup I-Cube Design Systems (Santa Clara, CA) has entered the emerging programmable hardware market with its introduction of a VLSI device, the IQ160. The chip, the first in a family of field-programmable interconnect devices (FPIDs), brings programmability to board-level interconnect, which lets you build reconfigurable hardware such as ASIC/logic prototypes and programmable circuit boards.

The IQ160 is packaged in a 208-pin PQFP, which provides 160 programmable ports and eight lines for tristate control signals. The rest of the pins are used primarily for power supplies to ensure low-noise operation.

The heart of the IQ160 consists of a crossbar switch matrix. Every signal line in the switch matrix can be configured to connect to any other signal line. Connectivity between external signals is established by configuring the FPID through a JTAG interface, and each interconnect port can be programmed to be a buffered input, a buffered output, tied high, tied low, or bidirectionally buffered. In addition, the output voltage level, pull-up current and propagation delay can also be selected.



The IQ160's ports pass through buffers and registers into a crossbar switch matrix. This configuration lets you connect any combination of pins without regard for routability. The device is controlled and programmed through a JTAG-compatible serial bus.

Signal integrity guaranteed

These buffers can sense which side of the port is being driven and can actuate according to where a signal is coming from. In addition to ensuring signal integrity, the buffers also reduce interconnect delay, although they introduce a fixed delay. According to I-Cube, this port-to-port delay is typically about 17 ns for the 1.2-µm CMOS device.

"Though our buffered ports cause some delay, they provide advantages over other solutions which aren't buffered," says Shrikant Sathe, director of marketing at I-Cube. "First of all, they guarantee signal integrity, even in applications with large fanouts. And we believe that it's all right during the prototype or logic verification phase to run at less than speed. After all, that's what people who use emulation systems do. It's true that the buffered ports consume more power—about 1 W in the 20- to 30-MHz range—but that means that they can drive more load, perhaps up to 300 pF."

A 15-bit sampling register behind every interconnect port is used to store successive signal values. The sampling is controlled through an external sampling clock. The sampled signals are read back using the JTAG bus.

Fully compatible

Because the IQ160 uses standard JTAG port configurations, you can use the device on any JTAG-compatible board. The JTAG port programs the transistors in the crossbar array, as well as the function bits in each buffer.

The IQ160 can be configured at power-on, or dynamically while the target system is in operation. By using JTAG's load and execute capabilities, a new set of bits can be loaded and latched all at once. This lets you program the part incrementally while it's in use. The crossbar configuration of the IQ160 also lends itself to dynamic programming applications.

"It's important to avoid unpredictable delays when you're programming a device dynamically," Sathe points out. "And with our interconnect architecture, you not only have a predictable delay, you are also guaranteed a connection."

I-Cube predicts that its device will be used in telecommunications systems that have traditionally used crossbar switches, as well as in test and measurement instruments to simplify connection of external signals. Multiprocessor systems that need to change connections dynamically between processors can also use the device.

I-Cube is sampling the IQ160 for $150 each. A prototype system with an IQ160 mounted on an evaluation board, a PC-compatible interface board, a stand-alone IQ160, and software sells for $2,000.

— Mike Donlin

IQ160 at a glance

- Field-programmable interconnect device with 160 I/O ports
- JTAG bus-compatible for configuration control and testing
- Typical port-to-port delay of 17 ns
- Eight signal lines for tristate control
- Dynamic and incremental reconfiguration capability
- Available now for $150; evaluation system with interface cards and software available for $2,000

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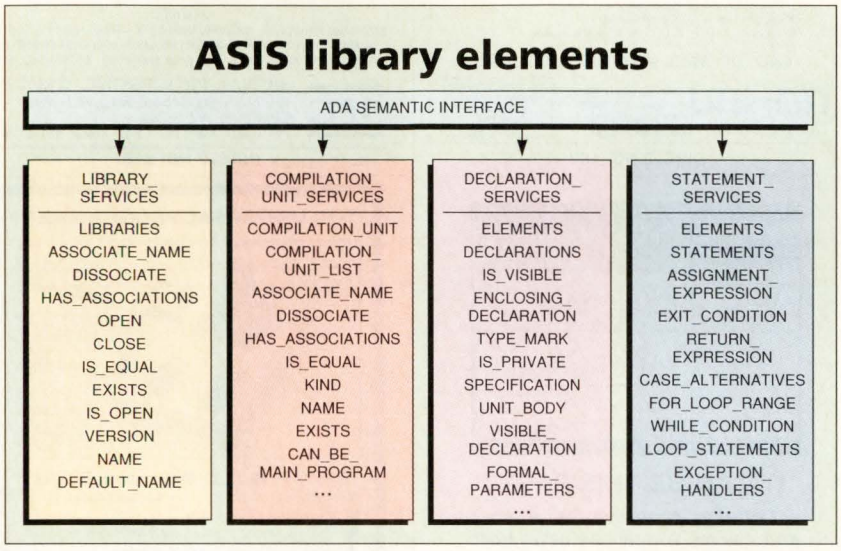
SOFTWARE & DEVELOPMENT TOOLS

Toolkit lets CASE vendors adapt to Ada compilers

In the past, third-party CASE tool vendors haven't been able to adapt their tools readily for Ada development. They've been hampered by the difficulty of using the internal data representation of the Ada library system, which may differ from compiler to compiler. Although CASE tools such as graphical design editors have been able to produce syntactically valid Ada designs, their inability to access internal data representations has yielded Ada designs that weren't necessarily semantically valid.

An open interface standard that lets third-party CASE tools access the Ada library system may change all that. Recently developed cooperatively by TeleSoft (San Diego, CA) and Cadre Technologies (Providence, RI), the first product implementing the Ada Semantic Interface Specification (ASIS) has been announced by TeleSoft.

Previously, some third-party CASE vendors have been able to integrate their tools through agreements with compiler vendors who granted them access to proprietary compiler technology. The advent of ASIS as a public-domain specification means that CASE vendors will be able to bridge the gap between their tools and Ada libraries for any compiler that supports the ASIS interface. To accomplish this, vendors will use TeleSoft's ASIS Toolkit, or similar toolkits that may be developed by other companies.



The Ada Semantic Interface Specification gives CASE tools (such as graphical editors) access to library information generated by Ada compilers, including library, compilation unit, declaration, and statement services via a public-domain interface. An individual compiler vendor's internal data representation can change without affecting the tool/compiler interface.

At present, vendors can access Ada semantic information generated by TeleSoft's TeleGen2 Ada compilers and stored in the TeleGen2 Ada library without having to understand the complexities of the library's internal representation of data. As more Ada compiler vendors adopt the ASIS interface, the choice of compilers for CASE vendors who use the toolkit will increase.

Looking beyond the trees

In the past, if a compiler vendor wanted to supply a CASE vendor with access to Ada semantic information, it meant using some intermediate Ada representation such as Diana trees or abstract syntax trees (ASTs). Such information was difficult to work with because it was stored in cryptic trees that needed to be processed and decoded for a user to traverse them. In addition, if the internal representation of the compiler's libraries changed, the interface to the CASE tools would break. With the stable interface provided by the ASIS specification, such internal representations can change without affecting the compiler's ability to integrate with the CASE tools.

ASIS was developed under the military's Software Technology for Adaptable Reliable Systems (Stars) program. It's also being submitted to the National Institute for Standards and Technology for possible inclusion as part of the Application Portability Profile (APP).

Already Cadre, TeleSoft's partner in the project, has used the ASIS Toolkit to give its Teamwork/Ada reverse-engineering tool access to TeleSoft's Ada library. The original tool was based on an Ada syntactical analyzer. The adaptation was accomplished in two weeks, and Cadre is expected to incorporate the product version of ASIS in a future release of Teamwork/Ada.

The ASIS Toolkit is available immediately for use with TeleSoft's RISCAda/Sparc development systems, TeleGen2 for VAX/VMS and the IBM AIX Ada/6000 compiler for the IBM System/6000. Single-license pricing ranges from $13,500 to $36,000, depending on hardware configuration. The tools which utilize the ASIS integration technology may be distributed with no further end-user license fees to TeleSoft.

— Tom Williams

ASIS Toolkit at a glance

- Conforms to public-domain Ada Semantic Interface Specification
- Allows CASE tool adaptation to libraries of compilers supporting ASIS
- Presently works with TeleSoft TeleGen2 Ada compilers
- One-time purchase price; no further product royalties

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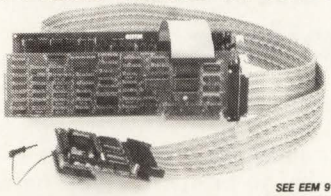

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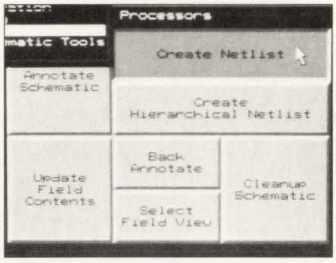

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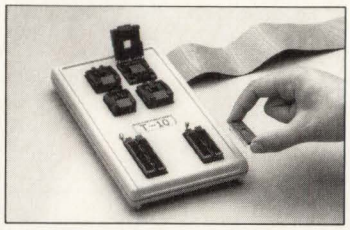

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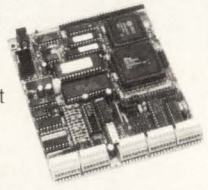

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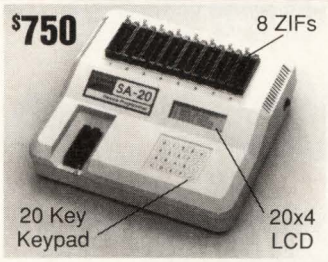

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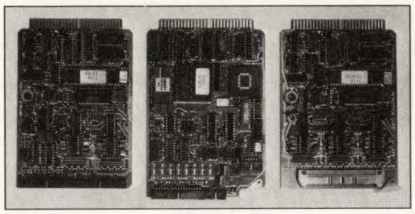

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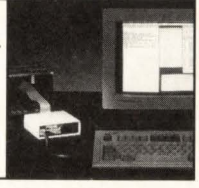

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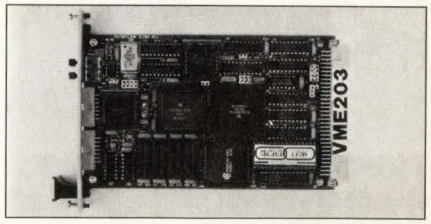

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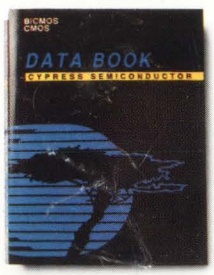

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