A PENNWELL PUBLICATION SEPTEMBER 1992

COMPUTER DESIGN

Technology and Design Directions

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FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS

Vertex's Bruce R. Bourbon on: High-level design

Object-oriented methods transform real-time programming

ASIC testability tools force trade-offs in silicon, performance and coverage

Silicon, tools and specs join to drive Futurebus+ growth

Special in this Issue:
Buses & Embedded Computers

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SIGNAL PROCESSING. GRIZZLY?

Designing a signal processing system can be a bear of a problem—immense, mean, and unforgiving. Engineers grappling with conventional analog or digital technologies face risk and unpredictability at every turn, with no guarantee of success. Designers invest months of development time in a brutal design process that's as lengthy as it is frustrating. Productivity and time to market are devoured in the struggle!

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Closed-loop vibration controller	analog	3 months	**2 weeks**	**$240,000†**

†Total system savings including project overhead, engineering resource, and system hardware costs.
*Estimated savings in engineering resource based on cost of $10,000 per man month.

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The Signal Processing Company

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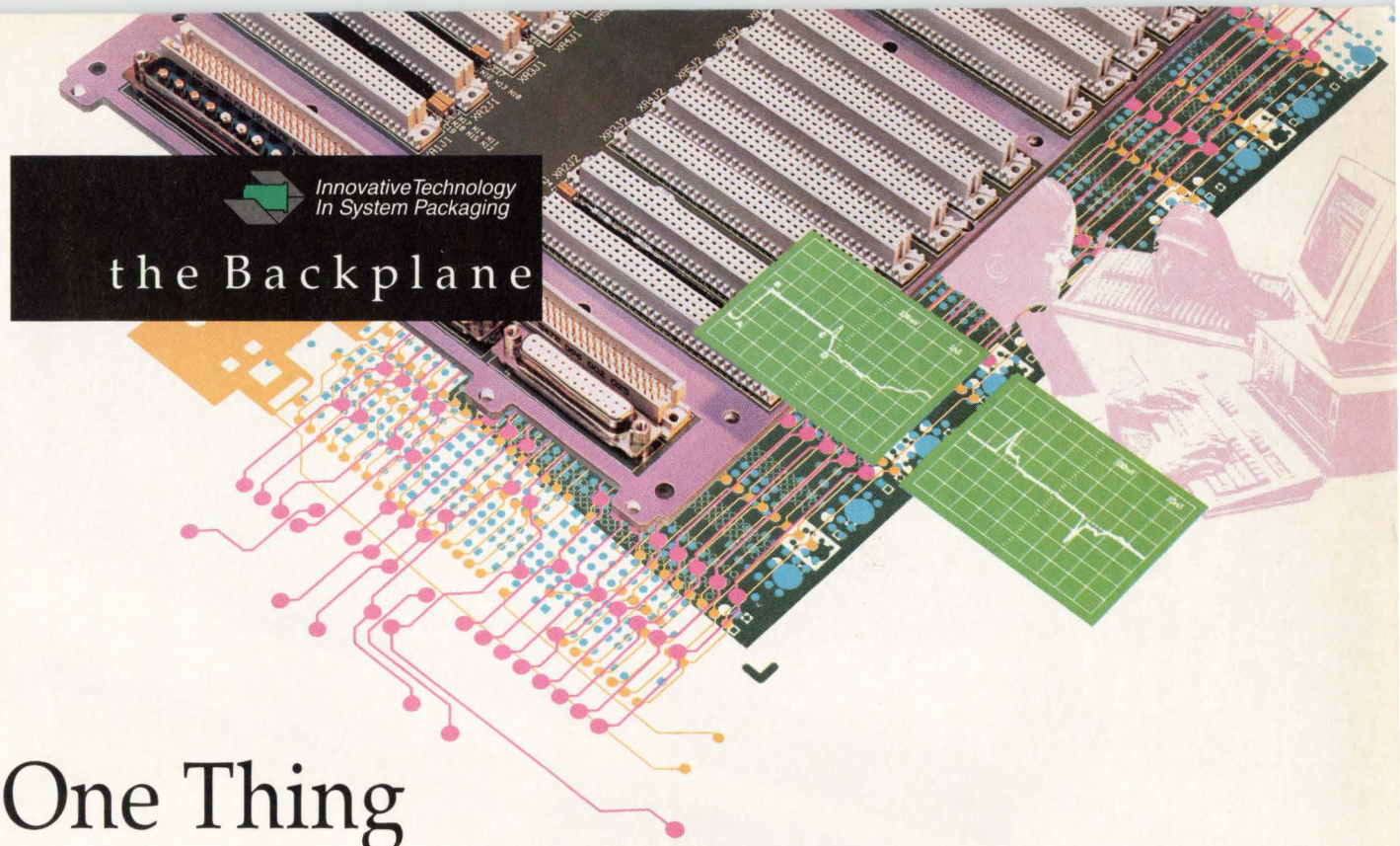
CIRCLE NO. 1



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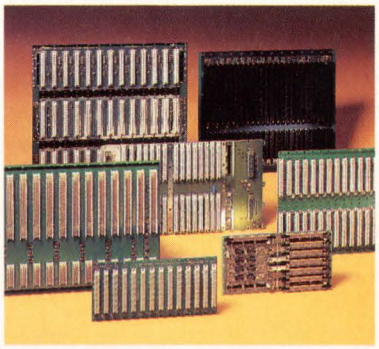

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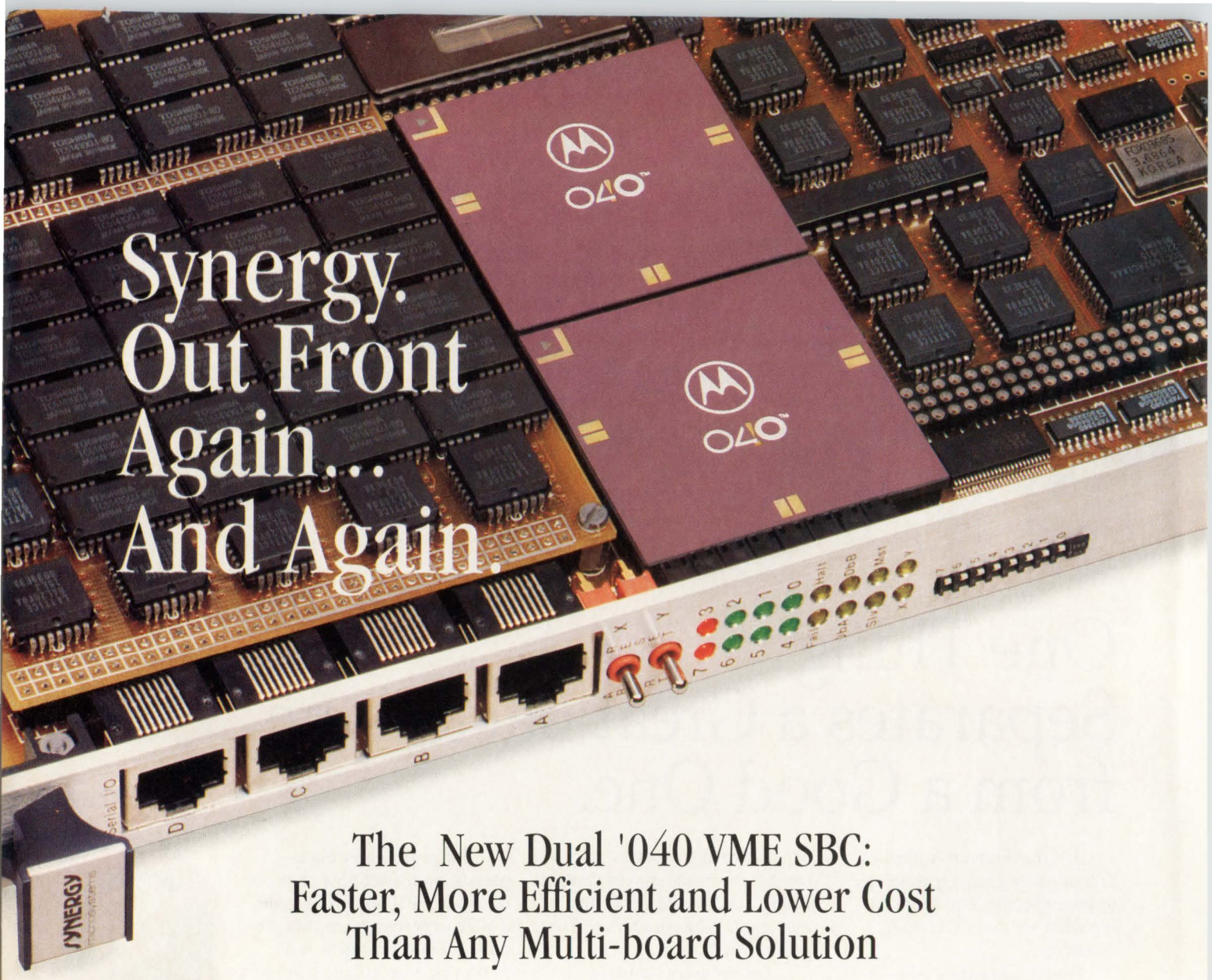

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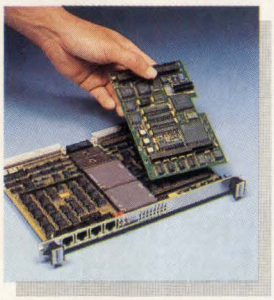
The New Dual '040 VME SBC: Faster, More Efficient and Lower Cost Than Any Multi-board Solution

Get on-board multiprocessing and an astounding **40 MIPS** throughput, when you power your system with Synergy's new SV420 single-slot SBC. The SV420's dual-CPU design means you'll need fewer boards in your VME chassis, with no VMEbus bandwidth bottlenecks between the '040s, and system-wide cost saving of more than 40%.

And even if you don't need multiprocessing right now, the SV420 still puts you out front. Use the second '040 as a super-smart DMA controller. When combined with the SV420's **66 MByte/sec** VME64® circuitry, nothing communicates faster over the VMEbus.



Over a dozen smart, powerful I/O modules fit Synergy's '020, '030, '040 and Dual '040 SBC's.

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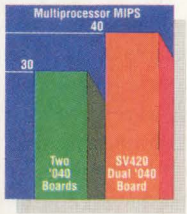

Better yet, just tell us what you need. We're the company you can talk to about your VME system design problems. You'll find that we listen *and deliver* (every Synergy I/O module on our list started as a customer request). We mean business when we say customer support is our most important mission.

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CIRCLE NO. 3

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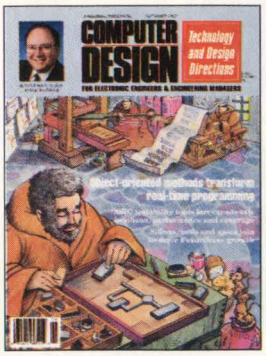
COMPUTER DESIGN

Technology and Design Directions

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



Just as movable type revolutionized printing, object-oriented software development has the potential to transform real-time programming.....**101**

Illustration by Bill Morrison

Special Report: Buses and Embedded Computers

Applications, not technology, drive embedded computers

"Business as usual" is no longer the rallying cry of standard-bus technology at the board level.

See Page 83

NEWS BRIEFS

TECHNOLOGY DIRECTIONS

ASICs & ASIC Design Tools

CAE/CAD Tools

Computers & Subsystems

Software & Development Tools

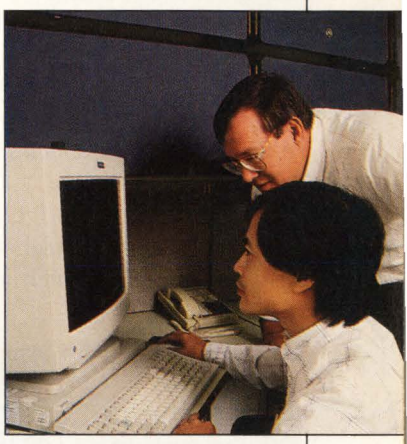
NEW PRODUCT DEVELOPMENTS

Integrated Circuits

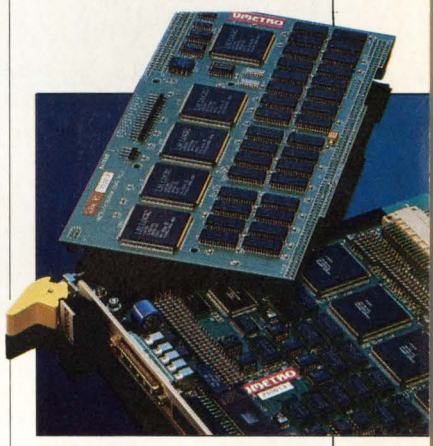
Software & Development Tools

ASICs & ASIC Design Tools

Computers & Subsystems



Page 33



Page 40

Page 146

CONTINUED ON PAGE 5

HMI development systems do it all!

HMI provides complete development systems—in-circuit emulator, window driven source level debugger and software performance analyzer—that address all aspects of the microprocessor system design cycle, from prototype to production:

HMI Emulators Feature:

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- Work with IBM PC family and UNIX based machines including SUN and Apollo.

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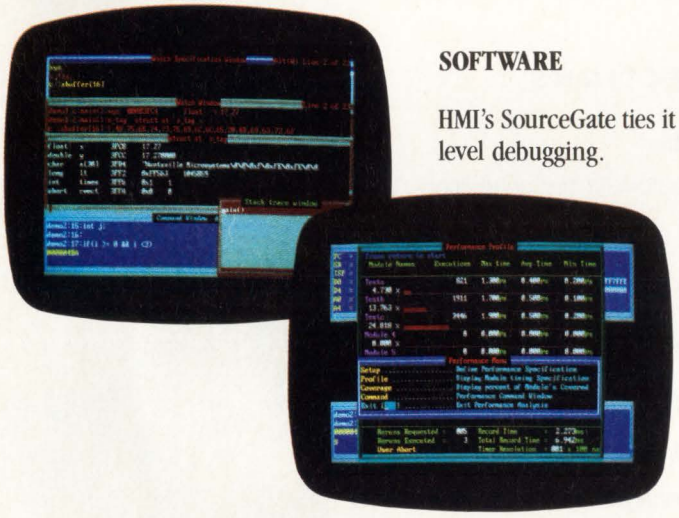

SOFTWARE

HMI's SourceGate ties it all together, so emulator features aren't sacrificed to gain source-level debugging.

HMI SourceGate® Features:

- Custom window configuration determined by user.
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68020	6809/6809E	8096/80196 Family
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68302	68EC030	64180/Z180
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CIRCLE NO. 4

COMPUTER DESIGN Technology and Design Directions

CONTINUED FROM PAGE 3

Vertex's Bruce R. Bourbon on: High-level design

A look at the market fundamentals behind the top-down design methods everybody is talking about..... **27**

TECHNOLOGY & DESIGN REPORTS

ASIC testability tools force trade-offs in silicon, performance and coverage

Will you trust your complex ASICs to test synthesis? Can you take hits in silicon and speed in exchange for quality? Does integration or tool performance come first for you? —*Barbara Tuck* **57**

Silicon, tools and specs join to drive Futurebus+ growth

The first Futurebus+ systems are now emerging, but introductions are lagging far behind expectations. The bandwagon is rolling, however, and the players are jumping on. — *Warren Andrews* **71**

COVER STORY

Object-oriented methods transform real-time programming

Making the change to object-oriented approaches for software development isn't free. It takes time, training, tools, and organization. But for those willing to invest, the payoff can be enormous—for small jobs and big ones. —*Tom Williams* **101**

DESIGN STRATEGIES

Borrowing from earlier design helps speed Microflash to market

Holometrix, in response to market demand, downsized its Thermaflash instrument by reusing both hardware and software.—*Jeffrey Child.* **121**

PRODUCT FOCUS

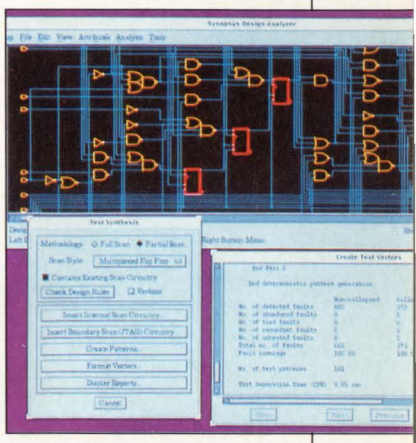
16-bit MCUs advance along many paths

Trying to stake out territory between less expensive 8-bit and more powerful 32-bit parts, 16-bit microcontrollers have evolved along traditional paths as well as in some interesting new directions. —*Jeffrey Child* **127**

COLUMN

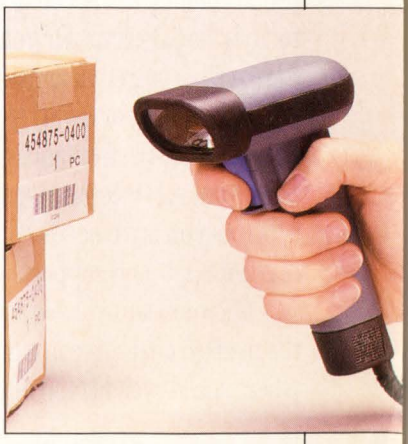
MIXED-SIGNAL DESIGN —*Stephan Ohr*

Mixed-signal test: balancing hardware and algorithms **156**



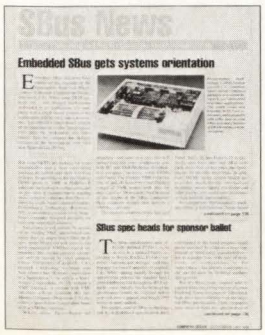
Page 57

Page 71



Page 127

SBus News


SBus News

Embedded SBus gets systems orientation

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SBus spec heads for sponsor ballot

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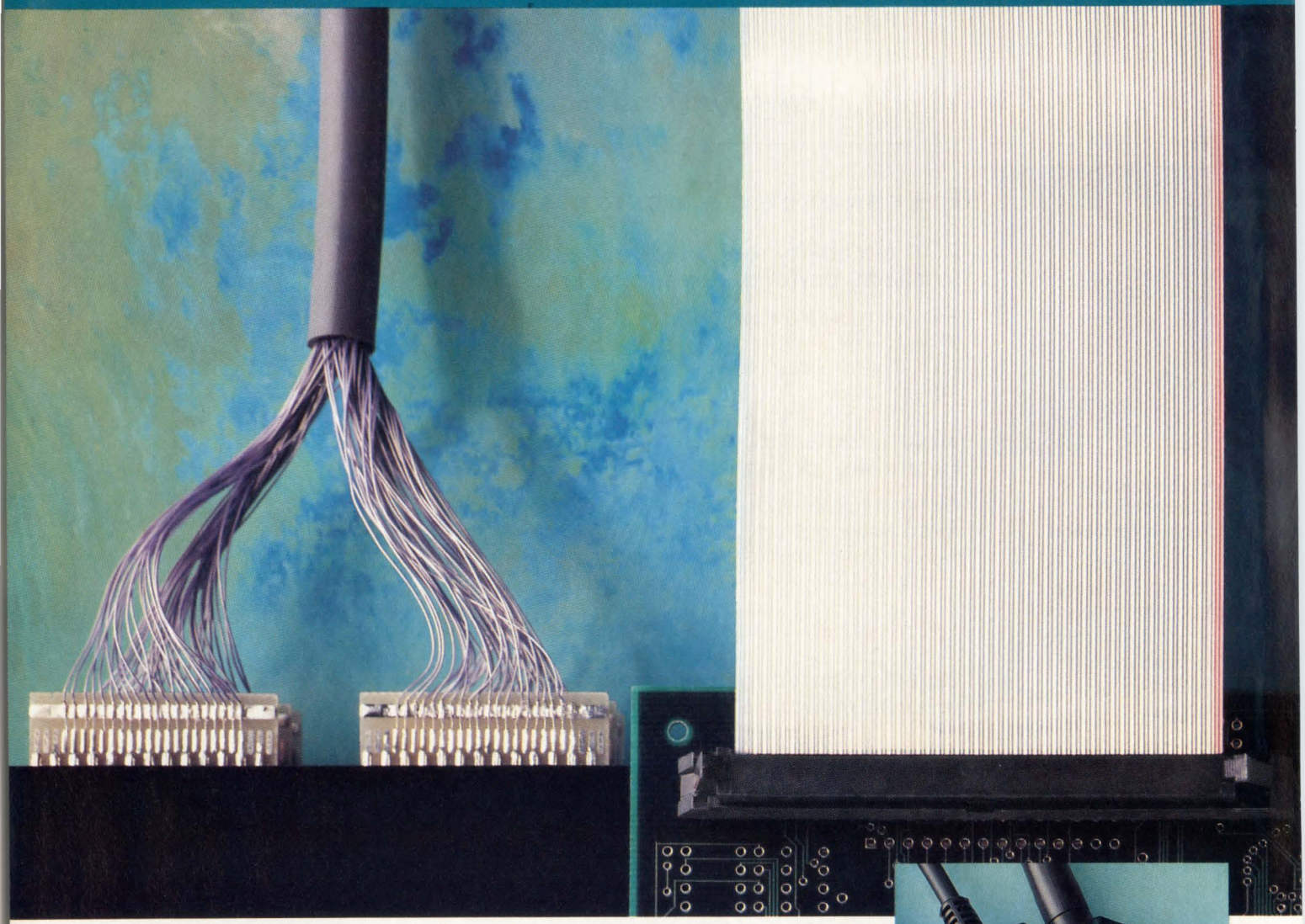
See page 135

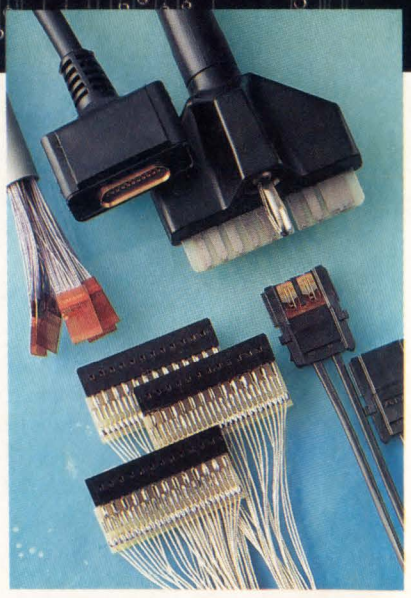
Cable assemblies for your toughest applications. Or your tenderest.

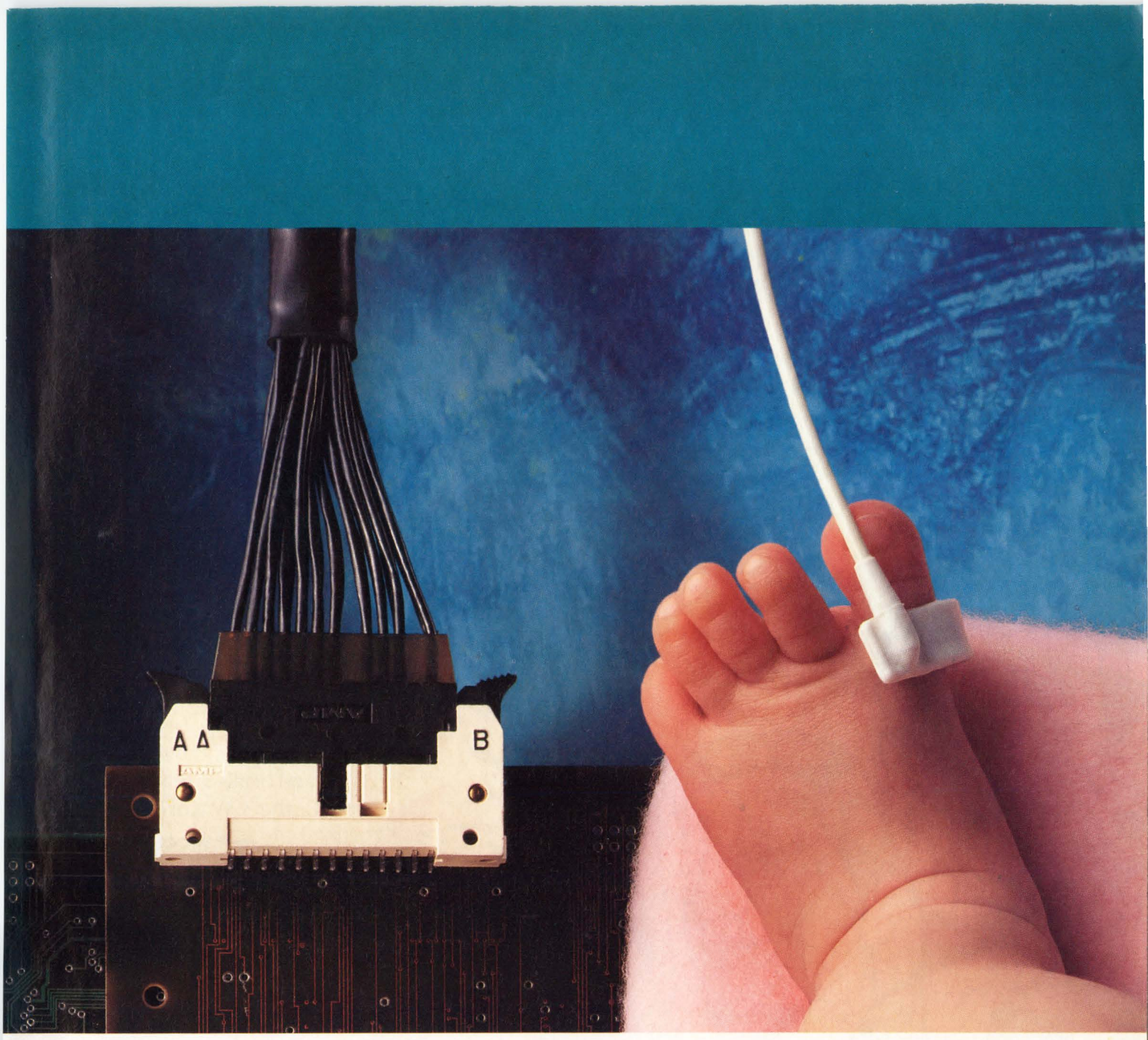


Your need may be defined by signal requirements: the speed demands of today's 'hot' designs. Or your need may derive from the environment a signal passes through, or even the signal's source. High-performance cable assemblies from AMP come in just as many types as you have needs. With the level of reliability – and support – you require.

Microminiature cable assemblies for the medical field serve in environments where space, weight, and maneuverability are critical, and 'friendliness' isn't a nicety, but a necessity. We design and manufacture assemblies to meet your most demanding requirements. They offer outstanding signal fidelity. They're rugged enough for heavy use. Yet they're astonishingly small, flexible, and easy to handle.

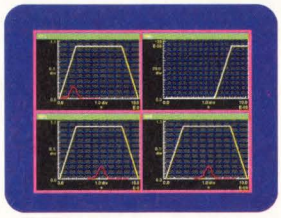
Our cable assemblies for high-speed data applications answer to a different challenge: moving your signals transparently. Fast data streams require coaxial or transmission-line assemblies for

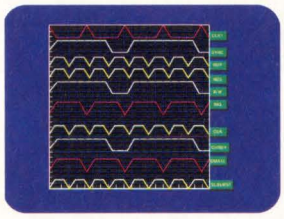


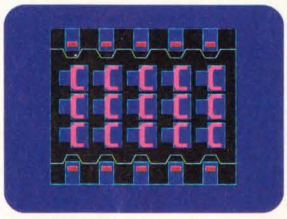


effective signal management. We custom-engineer around your performance requirements – matching cable, connector, and termination technology to the critical impedance/risetime needs of your design. And meeting your critical business needs for a cost-effective, time-effective solution.

The know-how we bring to your high-performance interconnect needs can be extended as much as you need, too: we offer services that pick up from your initial design concept and take you all the way to production. Starting with in-depth analysis and verification, we can provide board layout and routing, full software simulation of and proof of first article, thermal and electrical analysis, package design, and fabrication.







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CIRCLE NO. 5

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The cry for low-noise 3-volt logic has never been louder. That's why we're leading the charge with our new LVQ (Low Voltage Quiet) logic.

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ounces the in 3-volt logic.

battery-operated computing. As a result, LVQ is ideal for everything from laptops and notebooks to palmtops and pen-based systems.

LVQ is extremely quiet. Its reduced voltage swings go a long way towards minimizing noise on octals (guaranteed $V_{OLP}/V_{OLV} = \pm 0.8V$) and EMI—especially critical to miniaturized designs, where there's simply no room for elaborate and cumbersome shielding.

LVQ is low power. Make that ultra-low power, as in 50μA. And that's a specification we guarantee. So now you can count on much longer battery life, while maintaining the speeds required to optimize your 33MHz designs.

LVQ is also very compact. Its revolutionary new package design (QSOP, or quarter size outline package) not only makes LVQ smaller, but provides greater functionality and enhanced thermal conductivity. Not to mention increased board space.

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And while the family comprises 19 parts, it's just the beginning. In fact, LVQ is part of a much larger, company-wide commitment to provide a comprehensive selection of innovative low-voltage solutions—now including EPROMs, power management, interface, data acquisition, audio/video, and voltage reference products.

All of which proves that our quiet revolution is definitely a movement in the right direction.

LVQ FEATURES

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- 9ns prop delay
- Hands-on application assistance on dual voltage designs
- Samples available for 5- to 3-volt translation (LVX244)

LVQ PORTFOLIO

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74LVQ02	74LVQ174
74LVQ04	74LVQ241
74LVQ08	74LVQ244
74LVQ14	74LVQ245
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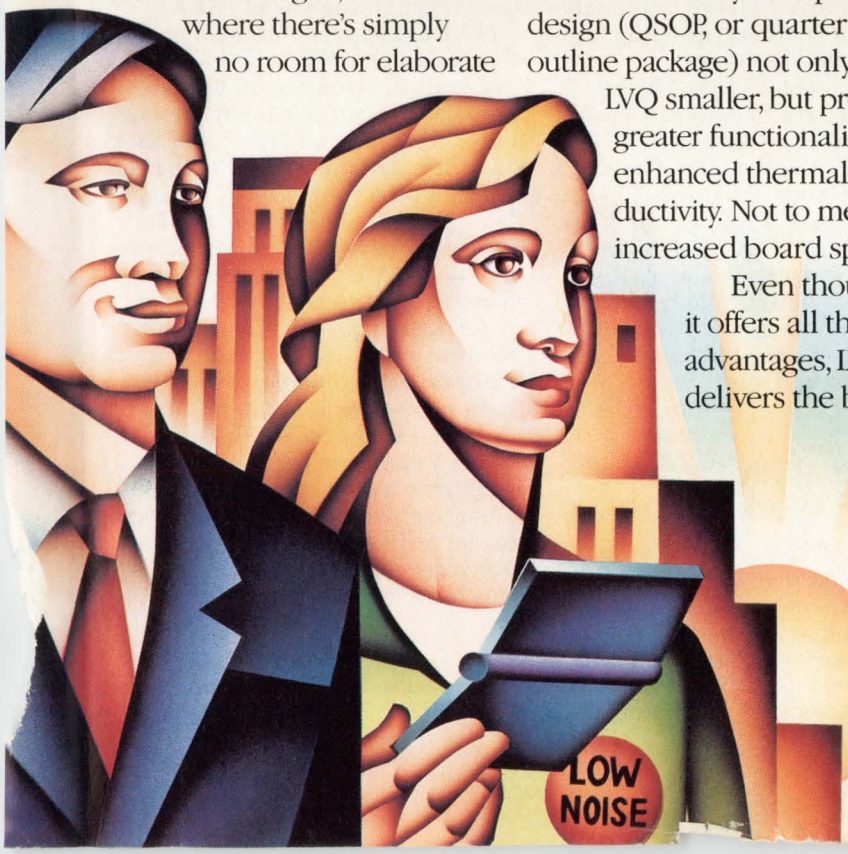
74LVQ74	74LVQ373
74LVQ86	74LVQ374
74LVQ138	74LVQ573
74LVQ151	



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High-temperature superconducting MCM unveiled

The world's first high-temperature, superconducting multichip module is a ring oscillator/counter introduced by Superconductor Technologies, Inc. (STI—Santa Barbara, CA). Developed under a DARPA contract, it consists of nine conventional CMOS inverters connected by lines of superconducting thallium HTS.

STI has the world's only HTS foundry. Frank Patten, DARPA Defense Sciences Office program manager, says, "By using HTS for the interconnects between silicon ICs, we will be able to build modules that have less signal delay." He believes this demonstration "opens the door for full-scale development." *—Don Tuite*

Digital to launch MCM partner

Digital Equipment Corporation (Maynard, MA) is hoping that the fledgling multichip module (MCM) market will bring some much-needed capital into the company's coffers. Digital is set to launch MicroModule Systems (Cupertino, CA), an MCM design and fabrication facility that will target systems houses, telecommunication companies and defense-related contractors that want to incorporate MCMs into their designs.

MicroModule has a 24,000-ft^2 wafer fab and a staff of about 85 people. Until now, Digital has been using the facility to design and manufacture MCMs for its VAX 9000 systems, but the need for cash is forcing it to spin off the company as a money-making partner.

—Mike Donlin

Actel cuts FPGA prices; still more coming

For the second time this year, Actel (Sunnyvale, CA) has cut its FPGA prices, keeping a commitment it made last February to continue to pass on its own cost reductions to users. "Actel has been able to meet its commitment because we have continued to benefit from our technology, which uses the extremely small PLICE antifuse programming elements in combination with our optimized architecture," says senior vice-president of sales and marketing Doug Rankin. "This technology results in smaller die sizes and lets Actel continue to reduce prices."

Prices for the ACT 1 family, currently in production, have been cut up to 10 percent for high-volume sales. Across-the-board reductions also apply to the newer ACT 2 family, now moving into production applications. The 8,000-gate A1280, for example, has been reduced up to 33 percent.

Price cuts apply to all packages, temperature ranges and speeds for both families. More good news for users— further reductions will probably be announced next year.

—Barbara Tuck

European consortium launches OS project

A project aimed at ensuring the viability of open-systems computing has been launched by a consortium of European companies, including Alcatel Ashthom, Chorus Systems, Olivetti, Siemens Nixdorf, SGS-Thompson, and Unix System Laboratories. The $14-million project is part of the European Community's Espirit III initiative to create advanced European-developed information technologies. The project, called Ouverture, will aim at advancing Unix System V Release 4 technologies into new areas, including real-time embedded systems.

The main goals of the Ouverture project are to optimize the integration of microkernel technology, based on the already available Chorus/Mix from Chorus Systems (Paris, France), into Unix SVR4 for massively parallel and real-time applications, as well as to introduce object-oriented interfaces, while researching the benefits of object-oriented technology, to mainstream Unix.

—Tom Williams

TI teams with Cadence on ASIC Workbench

The effectiveness of ASIC design tools rests on the silicon expertise built into them, so Texas Instruments (Dallas, TX) is an ideal candidate to partner with Cadence Design Systems (San Jose, CA). TI and Cadence's goals are to enhance Cadence's ASIC Workbench toolset by creating tighter links between synthesis, floorplanning and layout; to put into users' hands the ability to incorporate RAM and other customized functions into base arrays; and to automate the process of designing fully testable ASICs.

TI will be installing ASIC Workbench in its worldwide customer design centers. Its engineers will also work on-site at Cadence's San Jose facility to directly influence the development of an enhanced ASIC Workbench.

According to George Barber, manager of ASIC products at TI's Semiconductor Group, "Advanced design environments are needed to take full advantage of the next-generation silicon technology. We are working with Cadence, so that when the next-generation ASIC Workbench is introduced, we'll be there with the libraries and support necessary to have our customers hit the ground running."

—Barbara Tuck

Intel and HP team up for test

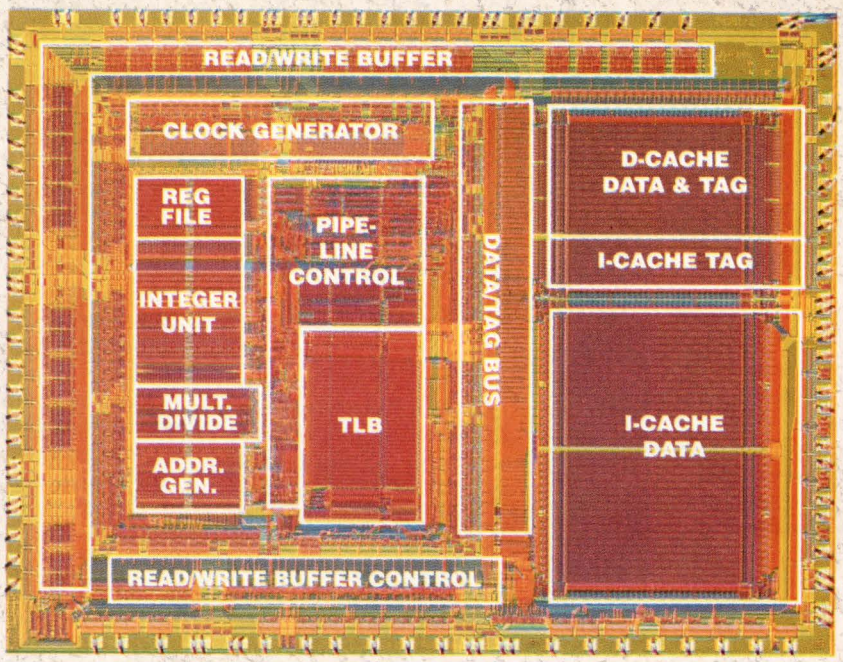
Intel (Santa Clara, CA) has signed an agreement with Hewlett-Packard (Santa Clara, CA) which will ensure the testability of Intel's present and future microprocessors through the use of IEEE-1149.1 boundary-scan technology. The deal gives HP access to boundary-scan information on specific chips, including pertinent pin-out data, cell type and order, and the 1149.1 instructions that have been incorporated into each IC's design. HP will convert this information into a boundary-scan description language (BSDL) that Intel can distribute to its customers.

As further proof of its commitment to providing testability information to its customers, Intel has even placed some of the BSDL files on a Compuserve bulletin board forum, Ionline. The files don't give away any secrets about a microprocessor's core logic or internal technology, but they do let users develop test vectors for circuit board scan testing.

—Mike Donlin

Continued on page 12

The Next World Standard for Embedded Systems



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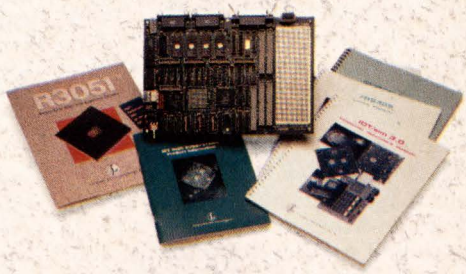
Call our toll-free hotline to get an IDT RISC Product Roadmap and complete information on the R3051 Evaluation Kit, so you can evaluate the next µP standard for embedded systems today.



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Integrated Device Technology, Inc.

CIRCLE NO. 6

Continued from page 10

PC/104 as a mezzanine

The trend toward using mezzanine buses in creative ways has been evident lately. Now, two companies are using PC/104 as a mezzanine bus. ZyCom (Saline, MI) has introduced a VMEbus board sporting a PC/104 socket, and it's reported that WinSystems (Arlington, TX) is evaluating PC/104 as a mezzanine bus for its STD family of CPUs.

PC/104 has some advantages for such applications. The bus's form factor is small enough to easily fit on a VME board and even an STD board with little sacrifice. Also, more than 20 vendors support the specification and proponents are driving hard to have it accepted as an IEEE standard in the form of an extension to the existing ISA specification. Finally, a handful of PC/104 boards provide a full PC CPU; vendors can use them as mezzanine boards to provide PC-compatible support for front-end interface functions, graphics or other applications where it's necessary to save both space and cost.

—Warren Andrews

Alliance offers test and measurement solutions

Three companies are teaming up to offer users VXI- and GPIB-based instrumentation, along with the software to integrate and control those instruments and the platforms to run the software. Sun Microsystems (Mountain View, CA), Tektronix (Beaverton, OR) and National Instruments (Austin, TX) will see to it that their respective products work together and will cross-train their sales forces on them.

Sun will offer its Sparcstation and Sparcserver workstations, which will run the graphical instrumentation and control software and hardware from National Instruments. National's LabView software lets users set up virtual instruments in windows on a workstation and integrate and analyze the measurements gathered by hardware instruments under its control. Tektronix will offer VXI- and GPIB-based instruments which can be integrated with the workstation-based bus controllers and controlled via the National Instruments software.

The alliance will also see to it that these systems can easily be linked to equipment from other vendors. You'll be able to purchase products separately from the three vendors, as well as through systems integrators and value-added resellers offering integrated systems. *—Tom Williams*

VME/Futurebus+ bridge board debuts

Cable and Computer Technology (CCT—Anaheim, CA) will debut the industry's first Futurebus+-to-VME bridge later this month at Buscon. The Profile A- and B-compatible system has its own intelligence, so no other processor is required in the system. A memory windowing technique is used to interconnect the two systems, mapping memory addresses from one to the other. The system comprises two boards, a VME board and a Futurebus+ card interconnected with a round, EMI-shielded cable. The system also lets multiple VME and Futurebus+ systems connect in a star, daisy chain or combination configuration.

CCT will also demonstrate its software- and hardware-application development station. The system consists of a special split backplane card cage containing a 7-slot Futurebus+ backplane and a 9-slot VMEbus backplane. In the VME section is a 386-based MS-DOS computer and the Futurebus+-to-VME bridge card. On the Futurebus+ side is the Futurebus+ bridge card. The system can be enhanced with other VME cards, Futurebus+ bus analyzers, CPUs, or CCT's array processor.

—Warren Andrews

Moto, BT to develop 6000-Mips MM chip set

Motorola (Austin, TX) and British Telecom (BT—Martelsham Heath, Ipswich, England) have announced plans to develop technology that may bring multimedia into the mainstream. Through the partnership, BT and Motorola will share their respective expertise in videoconferencing and semiconductor manufacturing. The specific goal of the partnership is to employ Motorola's chip expertise to integrate BT's standards-based video coding technology into a personal computer multimedia communications chip set capable of simultaneously processing real-time video, still images and data.

According to Motorola and BT, the 3-chip set will consist of a shell processor, an I/O processor and a 6000-Mips kernel processor. The chip set will comply with international standards, including MPEG (decode and encode), JPEG and several H- and G-series video standards (including H.261 and G.728).

Motorola plans to fabricate and market the chip set. For its part, BT will incorporate the chip set into future video communications products such as PC add-in cards. Motorola anticipates volume pricing for the chip set to be approximately $100. To put that into perspective, currently available implementations of MPEG alone, without encoding, cost from $100 to $200. Commercial availability is targeted for 1994, with samples ready by the end of 1993.

—Jeffrey Child

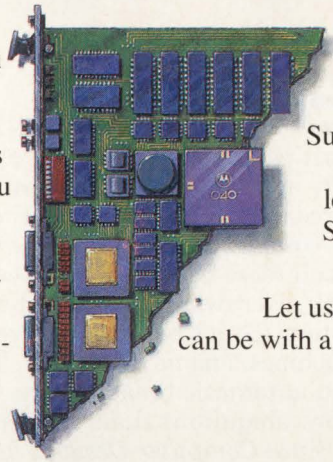
Chips talk over powerlines

Despite skepticism that a powerline could be turned into a medium for network communications, Adaptive Networks (Cambridge, MA) has developed a spread-spectrum technology that's seen a flurry of design wins. Among these is a proposal by CSK, Japan's largest system integrator, to use powerline communications to let Japanese vending machines communicate to a central location, thereby improving inventory and maintenance. Other designs include automated meter reading by a company in Spain and statewide lottery machine LAN/WANs in Providence, RI. While Adaptive Networks has offered the technology for over a year in module format, a chip set solution, announced last fall, becomes available in production quantities this month. *—Jeffrey Child*

Why Settle for ½ an '040 Board?

You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may only give you only half of what you expected from the '040.

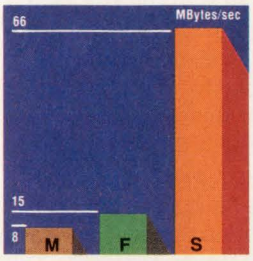
Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPs, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the SV430 outperforms every other SBC on the market by as much as 150%.



Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

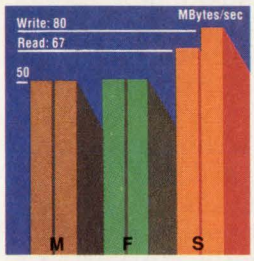
Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

Compare our specs. Synergy is superior across the board!



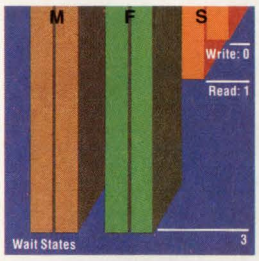
VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



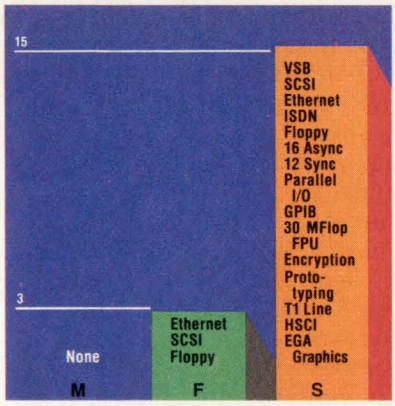
DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



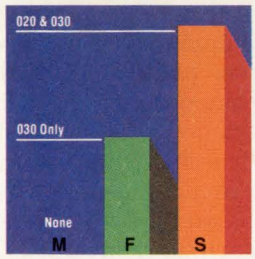
DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.



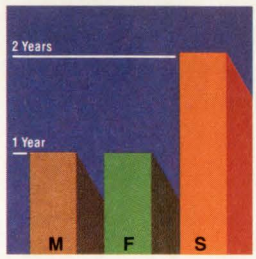
I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.



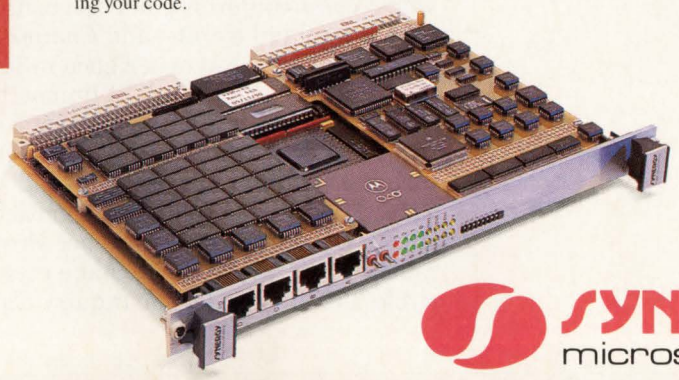
'020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.

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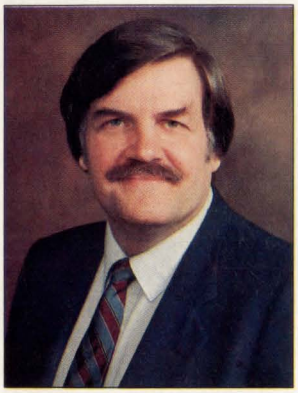
Embedded computing is what it's all about

"What makes ECC different from other conferences and exhibitions is its focus on providing solutions for embedded computer applications."



John C. Miklosz
Associate Publisher/
Editor-in-Chief

Every time someone uses the word "computer," what comes to most people's minds is first the PC or Apple Macintosh, then probably an IBM or a DEC mainframe/mini, and then, perhaps, a supercomputer. Pretty much the same is true when someone refers to "computer design" and *Computer Design*. But computers are much more than PCs or Macs or DECs or Crays. Computers are truly everywhere; it's just that most of them don't look like computers. That's because they're embedded in things like ultrasound machines, engine controllers, laser printers, PBXs, cellular phones, and automatic bread bakers. Today, embedded computers are more ubiquitous than "conventional" computers.

Since *Computer Design's* focus from its inception has been hardware and software designers, as well as the design of OEM systems or the equivalent, we've kept in step with the evolution and dispersion of computing technology and power into the embedded realm. Because of that history, and our desire to deliver the best, most up-to-date information about the technology, design and product issues surrounding embedded computers, we recently accepted an offer that was, simply, too good to resist.

The offer was to take on the responsibility to formulate and organize the technical program for the *new* Embedded Computer Conference and Exposition (ECC) scheduled for April 14-16, 1993, at the Santa Clara Convention Center. ECC is being produced by BAV Expositions, a professional show management group based in South Norwalk, Connecticut.

What makes ECC different from other conferences and exhibitions is its focus on providing *solutions* for embedded computer applications. A focus on solutions, not just products, leads naturally to a holistic approach to embedded computer design and integration that gives equivalent weight to issues in the selection and application of microprocessors and microcontrollers; custom and semicustom board designs; standard-bus single-board computers and peripheral boards; operating systems, real-time kernels and compilers; development systems and debugging tools; embedded PCs, workstations and even embedded minicomputers.

The similarities between ECC's charter, BAV Expositions' goals and *Computer Design*'s editorial philosophy have made for an ideal match. BAV has the management skills to stage a truly world-class conference and exposition—not just a narrowly focused, regional event—and *Computer Design* has the technical depth, breadth and experience in its editorial team to develop a technical program that's of unmatched excellence.

If you would like more information about participating in the technical program (i.e., giving a technical paper, presenting a tutorial, or running a workshop) call Warren Andrews at (508) 283-2102. It will be two to three months before the technical program is complete and the Conference Preview (with registration information) hits the mail. To make certain you receive the Preview, circle 199 on the Reader Inquiry Card.

The new SPARC®2SE has serious crunch power. 30 MIPS and 5 MFLOPS change the definition of single board computer performance. Workstation features? This board is loaded.

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Choose SunOS or VxWorks to tackle embedded and critical real time applications. Our MBus architecture is *the* high speed path for VME data and the only way to track Sun's hot new product moves.

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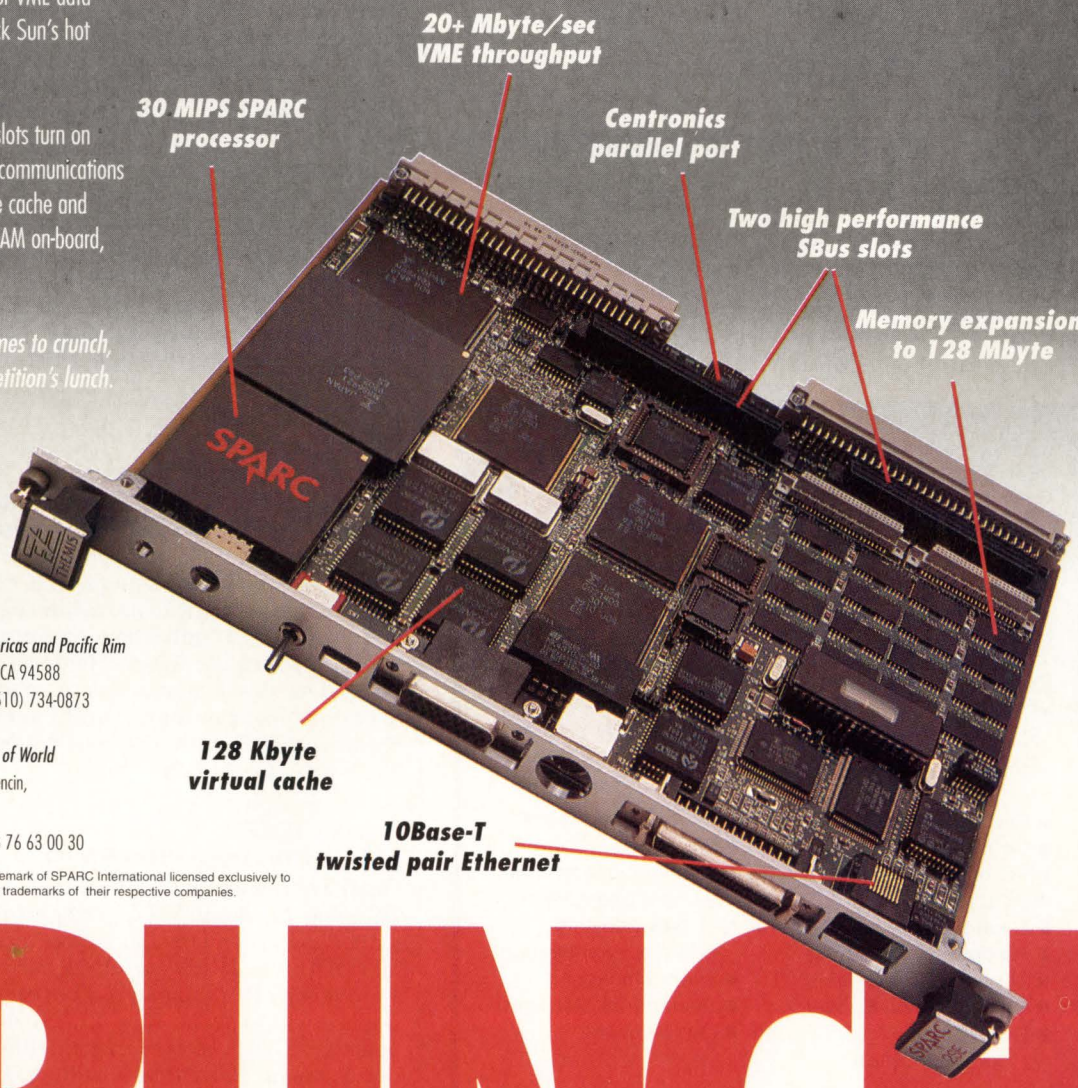

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CRUNCH

CALENDAR

CONFERENCES

September 15 - 17
Buscon '92 East

BUSCON/92-EAST℠
SEPTEMBER 15-17, 1992
HYNES CONVENTION CENTER
BOSTON, MASSACHUSETTS

Hynes Convention Center, Boston, MA. Buscon '92 East is the event where the products, technologies and components related to bus- and board-level design can be seen. The technical conferences, organized and coordinated by *Computer Design* and *Military & Aerospace Electronics*, are highly focused, in-depth seminars that explore the hottest issues from SCI to Futurebus+, RISC and embedded PCs. Contact: Registration Department, Buscon '92 East, 200 Connecticut Ave, Norwalk, CT 06856-4990, (800) 243-3238, Fax (203) 857-4075. **Circle 366**

September 20 - 24
International Test Conference

INTERNATIONAL TEST CONFERENCE 1992

Baltimore Convention Center, Baltimore, MD. This year's theme for ITC, the conference for the test and design community, is "Discover the new world of test and design." ITC will focus on the test and design techniques that companies need to compete globally, with emphasis on the integration of test factors into product design. There will be 16 tutorials and more than 35 technical sessions. Topics include: new test and design methods, MCM testing, BIST design techniques, test synthesis, and more. Contact: ITC, 514 E Pleasant Valley Blvd, Ste 3, Altoona, PA 16602, (814) 941-4666, Fax (814) 941-4668. **Circle 367**

September 21 - 24
Embedded Systems Conference

EMBEDDED SYSTEMS CONFERENCE

Santa Clara Convention Center, Santa Clara, CA. The Embedded Systems Conference and Exposition offers more than 80 lectures, workshops and tutorials about current tools, technology and theories in embedded programming. Full-day tutorials will include: object-oriented analysis, meta models for system development, event modeling for embedded systems programmers, and more. Contact: Miller Freeman, 600 Harrison St, San Francisco, CA 94107, (415) 905-2354, Fax (415) 905-2630. **Circle 368**

October 18 - 21
VHDL International Users Forum

VHDL INTERNATIONAL

Omni Shoreham Hotel, Washington, DC. The biannual VIUF brings together users, vendors and supporters of VHDL, the IEEE standard hardware description language. This conference will focus on how VHDL serves as an enabling agent for the effective management of system design and development. Participants will explore the use of VHDL for specification, design documentation, trade-off analysis, and as an aid in system production. A wide range of technical sessions and tutorials will be offered. The newest VHDL products will be presented. Contact: VHDL International, 407 Chester St, Menlo Park, CA 94025, (800) 554-2550 or (415) 329-0578, Fax (415) 324-3150. **Circle 369**

Continued on page 18

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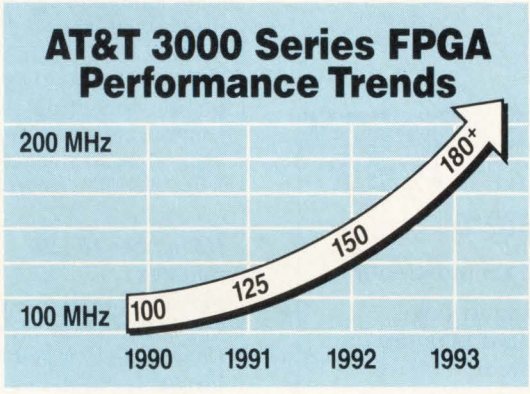
"Customerizing" means giving you the freedom to design-in the most popular FPGA architecture, without worrying about the future. While providing the logic you need to support the fastest microprocessors at the lowest possible cost. Introducing AT&T's ATT3000-Series 150 MHz FPGA, equipped with 2000 to 9000 gate densities, and ready for design-in today.



AT&T led the way with 125 MHz and 150 MHz FPGAs, and we'll continue to set the pace with even faster FPGAs, priced even more competitively. In 1993, AT&T will deliver ATT3000-Series FPGAs that can handle 66 MHz microprocessors. So as your microprocessor gets faster, you won't have to compromise system speed with slow logic.

Meanwhile, take advantage of the substantial savings now being offered on AT&T's ATT3000-Series 150 MHz devices, available from AT&T Microelectronics or your authorized AT&T distributor.

For a free 150 MHz Speed File to update your XACT* Development System, plus our FPGA Information Package, complete and mail the attached card, or call AT&T Microelectronics at 1 800 372-2447, ext. 905.

AT&T Microelectronics

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CIRCLE NO. 11

CALENDAR

CONFERENCES

Continued from page 16

October 19 - 21
Northcon

Northcon/92

Washington State Convention and Trade Center, Seattle, WA. More than 8,000 are expected to attend this electronics design show which will introduce Northcon-EDA, a dedicated show featuring the latest design automation tools and OEM products. Dr. Thomas Furness, director of the Human Interface Technology Lab at the University of Washington, will be a guest speaker on the subject of virtual reality. Contact: Northcon/92, 8110 Airport Blvd, Los Angeles, CA 90045, (800) 877-2668, Fax (310) 641-5117. **Circle 370**

October 28 - 30
Analog & Mixed-Signal Design Conference

ANALOG & MIXED-SIGNAL DESIGN CONFERENCE

Hyatt Regency, San Francisco Airport, Burlingame, CA. The Analog & Mixed-Signal Conference is an intensive, three-day educational seminar and exhibition. The heart of the conference is a technical program organized by *Computer Design* and targeted at engineers and engineering managers working on high-speed digital, mixed-signal and analog designs who need to better understand design problems and the capabilities and limitations of the analog and mixed analog/digital ICs, ASICs and CAE/CAD tools they use, as well as the best approaches for implementing their designs. Contact: Betsy Anderson/Marketing Communications Manager, *Computer Design*, One Technology Pk Dr, Westford, MA 01886, (508) 392-2209, Fax (508) 692-7780. **Circle 371**

November 16 - 20
Comdex

COMDEX/Fall '92

Several locations in Las Vegas, NV. The 14th annual Comdex/Fall is one of the largest trade shows in the country for computer and communications products, including networking, multimedia, imaging, and OEM business. More than 130,000 attendees are expected, as well as 2,000 exhibitors. This year's show is divided into five programs: new media; connectivity; the channel—addressing the channel network and OEM business issues; corporate computing; and international seminars on doing business in Japan, the changing European market, Latin America, and Southeast Asia. Contact: The Interface Group, 300 First Ave, Needham, MA 02194-2722, (617) 449-6600, Fax (617) 449-2674. **Circle 372**

Would you like your event listed here?

Computer Design can include a calendar announcement for your upcoming conference or seminar if it's received at least three months prior to the date of the event. Be sure to include a specific location, a brief description of the event and a telephone, fax number and address of a contact person. Please address calendar items to: Annette Staron-Wilson.

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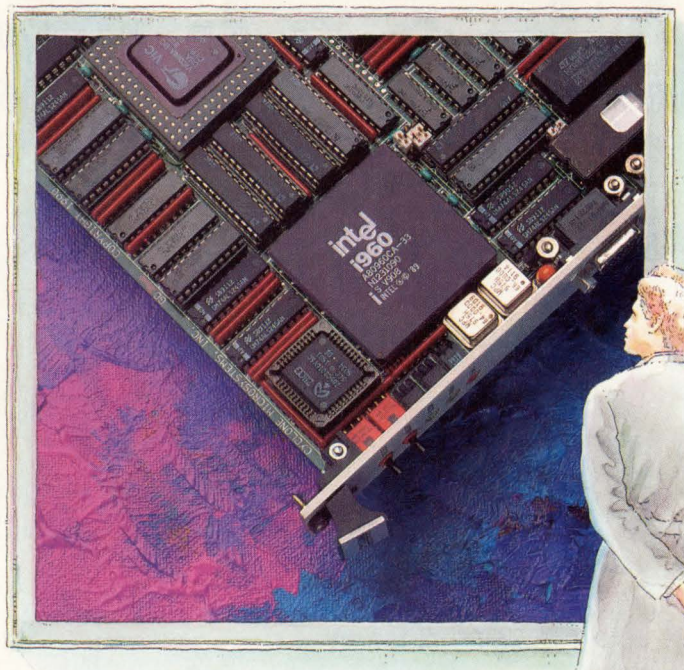

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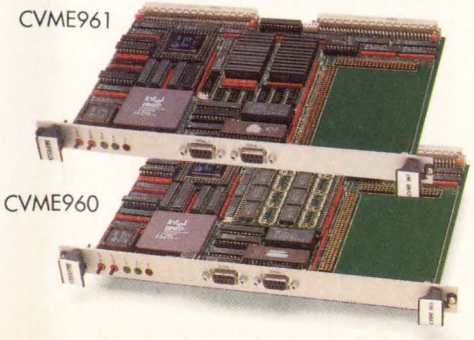

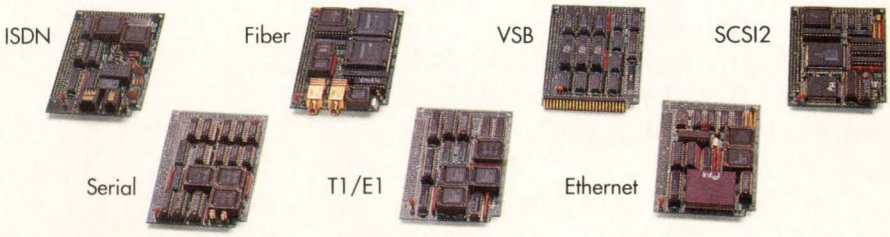

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CIRCLE NO. 15

An Object Less For Absolutely Pr

The MACH™ Family From AMD: The Fastest, Most Predictable High Density PLDs Available Today.

Oops! You're a couple of nanoseconds shy this time, and it's going to hurt. Perhaps next time you'll choose a more predictable vehicle. And the most predictable high speed, high-density PLDs available are the MACH family from AMD.

Only the MACH Family offers you worst case delays of 15ns* or less. Because MACH parts are essentially PAL® devices, just like the kind you already know. Not some hybrid PLD/FPGA, where you don't know how it performs — until it's too late. So you don't have to guess your delays or clock speeds, you just read them right off our datasheet.

But they're not just ordinary

Model Number	Equiv. Gates	Macro Cells	Max. Delay	System Speed	I/O Pins	Hard-Wired Option
MACH 110	900	32	12ns	66.7 MHz	44	MASC 110
MACH 210	1800	64	12ns	66.7 MHz	44	MASC 210
MACH 120	1200	48	15ns	50 MHz	68	MASC 120
MACH 220	2400	96	15ns	50 MHz	68	MASC 220
MACH 130	1800	64	15ns	50 MHz	84	MASC 130
MACH 230	3600	128	15ns	50 MHz	84	MASC 230

*In applications with a full 16 product terms. Every MACH part is specified using real-life conditions with all outputs switching.

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PAL devices. They're bigger and better, with densities ranging from 900 to 3600 gates, all in our submicron CMOS technology.

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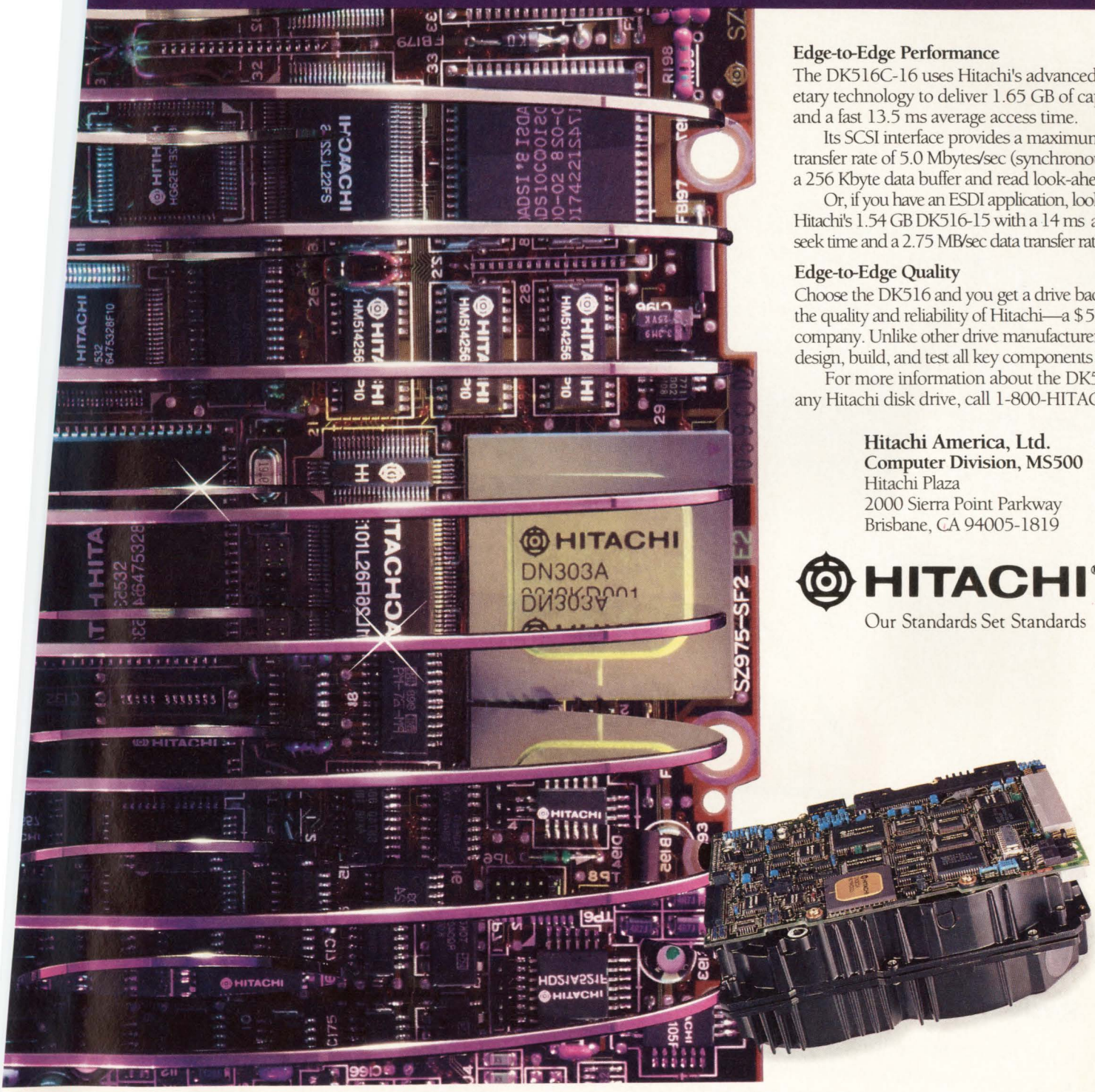

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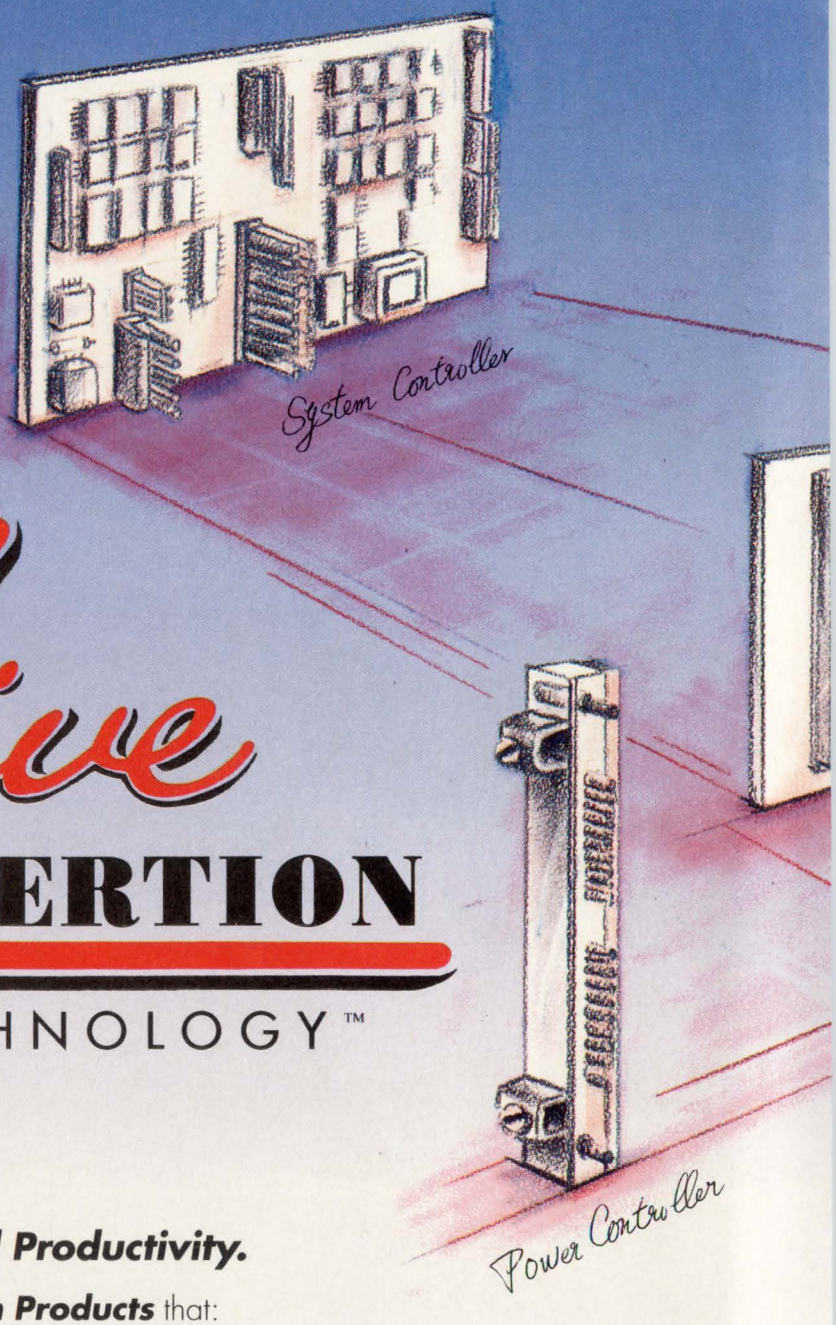

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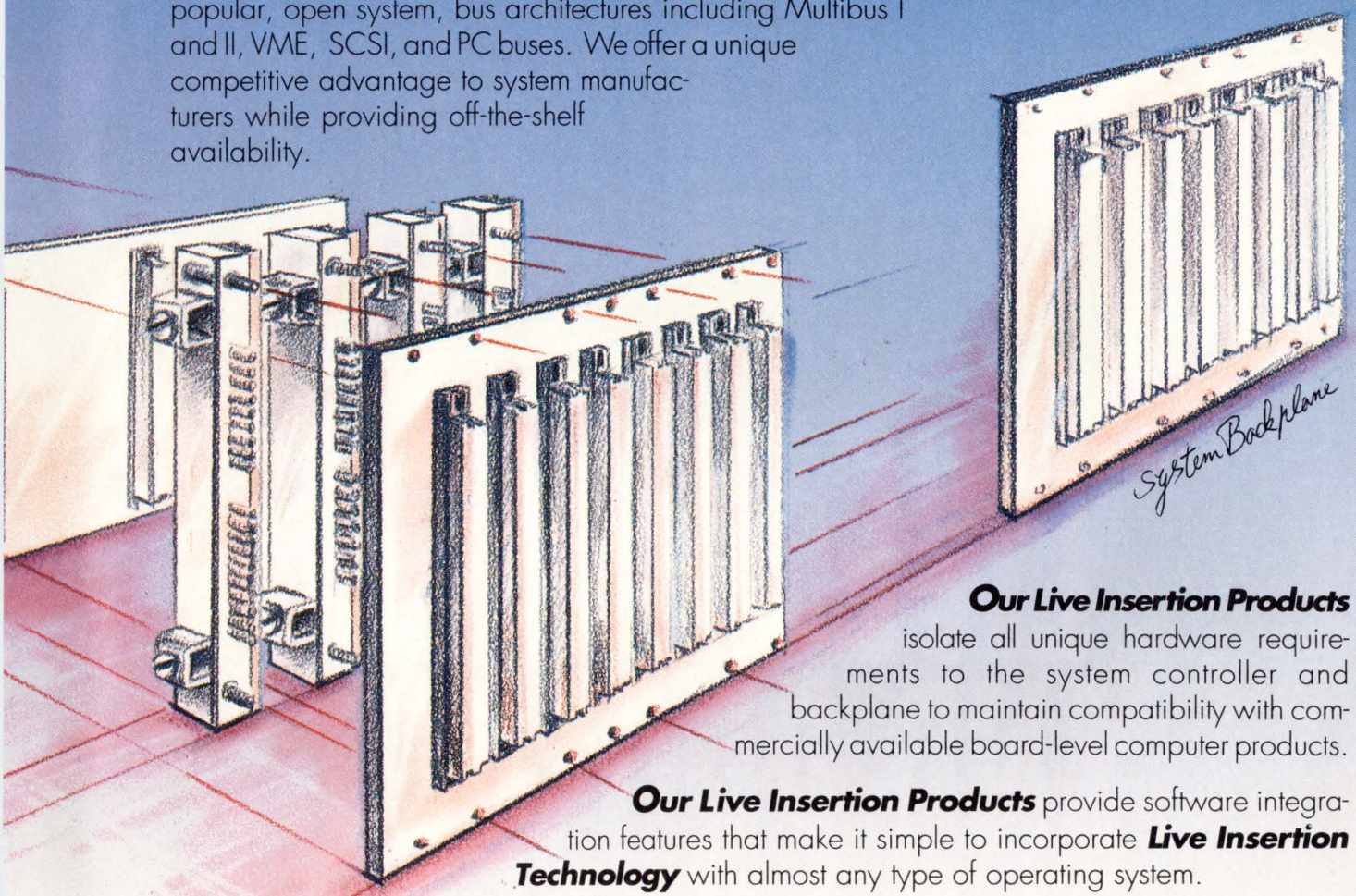

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CIRCLE NO. 22

Bruce R. Bourbon on: High-level design

High-level design, top-down design, hardware description languages, logic synthesis—we regularly read and hear about these new design methods. As is the case with many subjects that become popular in the trade press, however, the context is often unstated and the implications unexplored. Let's look at the market fundamentals that are behind these new design methods.

Many electronics and computer companies have adopted an increased pace of new product introduction as either a major strategic weapon or a survival tactic. We've all seen the widely published analyses suggesting that being six months late into a market can reduce lifetime product revenue by about 25 percent. And it's only going to get worse. End-market demand for new products will not abate.

The convergence of computer, graphics and communications technologies will create a demand for new categories of products, increasingly directed at the large and temperamental consumer market. Product lifetimes will continue to shrink as market windows stay open for ever shorter time periods. To maximize the profit earned from new products, there must be fundamental changes in design methods to reduce design time. This accounts for the increasing noise level about high-level design, HDLs and logic synthesis.

HDLs are coming

MJ Associates (Milpitas, CA) recently completed a report, *HDL Market Analysis*, based on a survey of 1500 design engineers and design managers. About 29 percent of the deliverable surveys were returned. Such a high-percentage response produced a large enough sample to yield statistically significant results. The large sample also suggests a high level of interest in HDLs.

In the report, MJ Associates states that "the use of HDLs in electronic design is on the upswing. Thirty-three percent of designers use HDLs today, and it's estimated that by 1995 70 percent of designers will use HDLs to design electronic systems." The company further notes that most of the respondents using HDLs have been doing so for less than two years. Finally, the survey verifies that the design of ASICs and application-specific standard products (ASSPs) are driving the use of HDLs.

MJ Associates estimates that only 15 percent of the ASICs designed in 1991 were designed using an HDL; that percentage is expected to reach 45 percent by 1995. Although the trend toward high-level design is clear, its penetration of the design community is still quite low.

The case against standard ICs

So why not design new products using only standard ICs? Surely that's the obvious way to get the design done more quickly. Wrong! The design of the next generation of electronic products is inextricably tied to next-generation processor and memory products, so the design of these generic or "standard" ICs must accelerate as well. Designers in semiconductor companies who are designing generic standard-product ICs and ASSPs are increasingly using ASIC design methods to shorten design times. Designers in systems companies must continue to use ASICs to differentiate their end products from the competition. Both groups need to boost design productivity to handle ever more complex designs in ever shorter design times.

Almost every type of IC has become more application-specific in the market's quest to tailor IC solu-

Bruce R. Bourbon is president and CEO of Vertex Semiconductor (San Jose, CA) and chairman of Open Verilog International (Sunnyvale, CA).

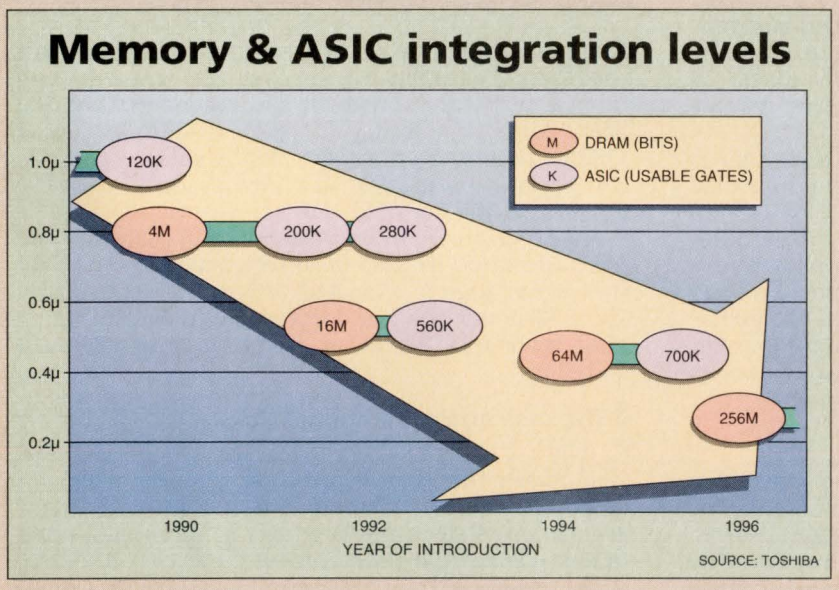
tions to the needs of a specific class of products or to a specific function within multiple classes of products. Most of these ICs are designed using ASIC design methods.

Even memories are becoming more application-specific. Today, we find more logic implemented on memory devices, and in the last several years there's been a proliferation of different types of memory devices directed at solving performance problems in specific system architectures. Customer-specific ICs are also needed to differentiate a product from competing products—by offering lower cost, smaller size, less power dissipation, more features. This suggests that ASIC design methods will be applied to all types of IC designs to ensure the designs can be completed in the time available.

Programmable devices pave the way

FPGAs, EEPLDs, ASIC emulation systems, and the recently announced programmable interconnect devices are primary ways for designers to deal with the reduced time available to develop new products. Even with these advances in design methods, however, we still can't exploit all the available silicon integration density. Let's look at some facts.

The illustration below shows the history of and future road map for memory and ASIC integration levels. Notice first that memory process technology drives ASIC process technology, and that the gap between the two is closing for a given generation. Also note that we can build gate-array architectures with 800,000 available gates and about 560,000 usable gates with triple-layer-metal interconnect technology. Implementing more than a half-million gates on a die presents some significant design challenges. How do we design such a complex circuit in a reasonable amount of time? And how do we adequately test the manufactured circuit to guarantee quality levels?



The progress in silicon integration has outstripped the capabilities of EDA tools and associated design methods. ASIC designs in excess of 100,000-gate equivalents still aren't commonplace, even though we can fabricate 500,000-gate equivalents.

High-level design methods aren't enough if we're to successfully deal with this complexity problem. Advocates of high-level design tend to concentrate on the logical part of the problem. That's necessary, but not sufficient. Let's examine the various pieces of the solution to this daunting design complexity problem.

Solving the design complexity problem

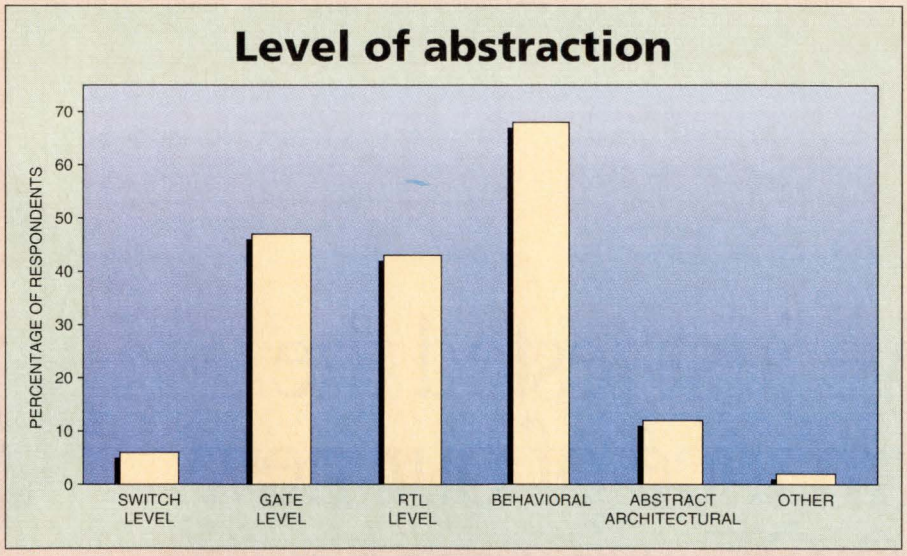
First, we must finally see the emergence of application-specific cell libraries with complex blocks designed specifically for a given class of products. Reusable, fully characterized blocks (megacells or megafunctions) reduce design time and are compatible with the dominant ASIC implementation style for complex designs—a sea-of-gates architecture with multiple embedded blocks placed anywhere on the die. Reusable design elements have been discussed for a long time. Now this idea must be used to reduce design times.

There are two primary ways to develop blocks that are intended for reuse. Software that automatically compiles the block, based on input of information about the desired memory configuration, is a good choice for regular structures, such as memory blocks. Memory blocks must be generated in a variety of size configurations, with one to *n* ports, and with built-in self-test (BIST) circuitry. Because of the regular structure and the variations in configuration, the use of a software compiler is the best approach—design knowledge is captured in the software, and that knowledge is easily reusable. Compilers may be developed for any class of block for which the block architecture is fully defined.

For high-performance blocks, such as core processors, a combination of handcrafted cells and automatically generated cells using row-based, standard-cell logic is often used. In this approach, tight control of the physical placement of cells is necessary to meet high-performance critical path constraints. High-performance blocks can be synthesized directly from an HDL description, albeit with less than optimal size and performance. As synthesis software and the associated physical design software continue to improve, more cells will be synthesized from an HDL description. In essence, the HDL description becomes the reusable form of the cell.

All types of cells require full characterization. Cells generated through compilation or synthesis are often characterized through simulation. Other cells that have a single design form may be characterized either through simulation or through measurements made on test silicon.

The second piece of the solution to the complexity challenge is describing the design at a level of abstraction above the gate level to reduce the amount of information that must be specified to completely capture design intent. This is the application space of HDLs and the various graphical means of describing the functional and timing behavior of the design.



Referring again to the MJ Associates report, "46 percent of the respondents who use HDLs use Verilog HDL, 39 percent use VHDL, and 25 percent use proprietary HDLs. Overall, we believe 15 percent of all designers use Verilog HDL, 13 percent use VHDL, and 5 percent use proprietary HDLs. Thirteen percent for VHDL is higher than expected. This is because several companies [whose employees responded to the survey] use both Verilog HDL and VHDL. Our estimates [of the number of] pure VHDL users is less than 10 percent in the United States."

The chart above shows the distribution of responses to the question, "When capturing a design, what levels of abstraction do you specify in HDL?" As expected, gate, register-transfer and behavioral are the dominant levels of abstraction in today's use of HDLs.

HDL usage will continue to increase as we adopt top-down design methods to take advantage of the available silicon density. This trend toward top-down design is being aided by the emergence of many new players in the HDL simulation market. In the last year, for example, the number of simulation products compatible with Verilog HDL increased from one to ten. But it doesn't really matter whether you prefer VHDL, Verilog HDL or a proprietary HDL. The real issue is the ability to automatically synthesize to the gate level those portions of the design description for which predesigned functions don't exist.

Design-for-testability

The third piece of the solution to the complexity challenge is design-for-testability. At 500,000-gate equivalents, using a DFT method is no longer discretionary—you must adopt a strategy to ensure adequate testability. A good DFT strategy is transparent to the design team. Software must synthesize the test logic, optimize the design for testability and automatically generate the test patterns for manufacturing test. Although the most obvious current choice is some flavor of scan testing, increased use of BIST for reusable blocks will gradually emerge.

The fourth piece is attention to system design issues. Today, this attention is focused primarily on clock skew minimization. With a 15-ns cycle time, giving up 3 ns to clock skew reduces the available clock period by 20 percent. Clock skew across a given chip and skew across the board must be minimized using a set of circuit design and physical implementation techniques.

The next system design issue is design planning—intelligent partitioning with ample consideration of power budget and packaging constraints at the system, board and IC levels. Design planning is one of the frontiers of design automation. Because it has, by definition, system-level scope, design planning is very application- and user-specific. As the EDA industry tackles this problem, care must be taken to ensure early tools are easily malleable to match user habits and preferences.

The fifth piece is physical design. In the IC realm, this means cell placement and interconnect routing software. Physical design of complex ICs has again become a real challenge. The problem was first solved in the latter half of the 1980s when place-and-route software first came into widespread use. Now complexity increases have made place-and-route elapsed times uncomfortably long. We need place-and-route software that handles embedded block IC architectures and completes its task in hours, not days.

The packaging dilemma

Sixth and last is packaging technology. As integration levels and operating frequencies have increased, so has the power dissipation. For ICs we need packages that can dissipate more than 5 W without junction meltdown or high-volume air flow across the package. These packages must also have excellent electrical characteristics—low parasitic inductance and capacitance—to facilitate higher operating frequencies. The move toward 3.3-V systems will help for a time, but the march is relentless. Major advances in packaging are needed to allow exploitation of all the available complexity.

Time-to-market pressure will not lessen, but will continue to increase. Can we manufacture the complex ICs to build the products needed to meet market demand? Our challenge is design. The increased popularity of HDLs and the growing availability of simulation and synthesis software tools are accelerating the trend toward top-down design methods. Continued advances in design methods, software design automation tools and packaging technology are all needed to ensure we can complete the design task in the available time, while using all the complexity offered by today's and IC fabrication processes.

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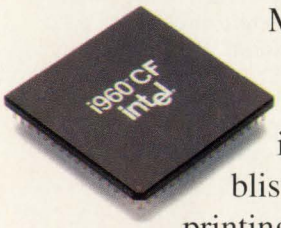

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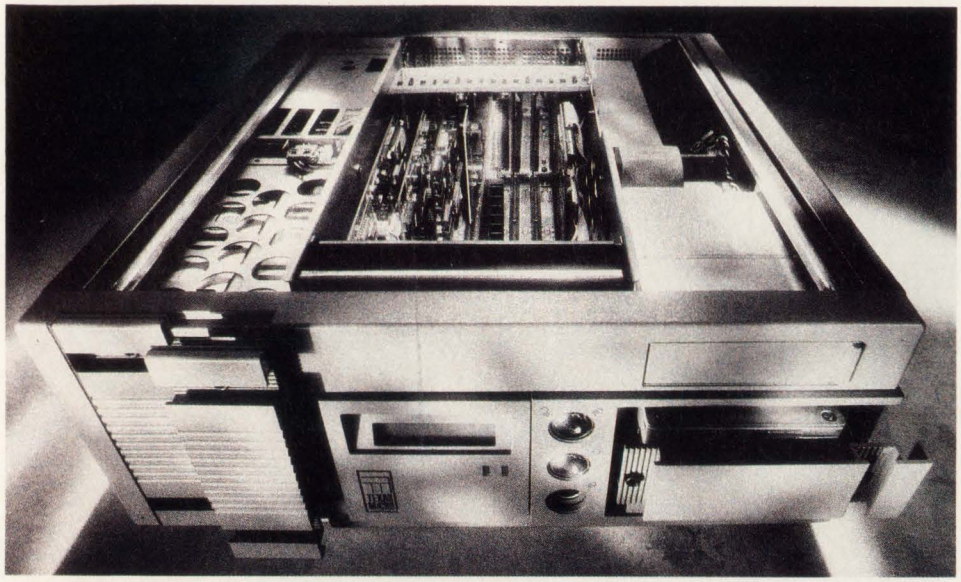

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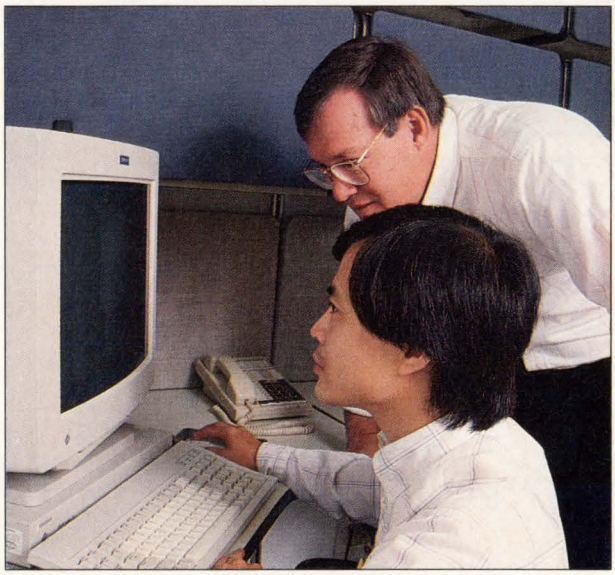
ASICs & ASIC DESIGN TOOLS

EDA leaders getting serious about automatic test generation

Barbara Tuck, Senior Editor

The complexity of both silicon and the systems into which it's going is forcing designers to higher levels of abstraction for complex ASICs, and the use of synthesis is putting distance between designers and implementation details. Both of these developments are making it increasingly difficult to generate test programs manually. While CAE/CAD vendors make testability trade-offs more palatable by enhancing tools already on the market (see "ASIC testability tools force trade-offs in silicon, performance and coverage," p 57), broad-line EDA suppliers such as Cadence Design Systems (San Jose, CA), Dazix (Huntsville, AL), GenRad (Milpitas, CA), Mentor Graphics (Wilsonville, OR), and Viewlogic Systems (Marlborough, MA) are just beginning to ship testability products that have been incorporated into their integrated toolsets.



Texas Instruments' Bob Gruebel, ASIC test development manager (standing), and Robert Wong, ASIC test development engineer, review test efforts of a new beta version of Cadence's design-for-test software. TI's early involvement with Cadence in defining testability tool specifications has been instrumental in ensuring compatability between Cadence software, and TI's ASIC design flow and libraries.

Real-world ATPG support

Cadence, which expects to ship Release 1.0 of its Test Solution product in November, signed Ericsson Telecom AB (Stockholm, Sweden) as its first Test Solution partner in June, and just weeks ago announced participation in a similar partnership with Texas Instruments (Dallas, TX). As an ASIC vendor, TI is very interested in its customers' ability to develop netlists and test vectors. Bob Gruebel, TI's ASIC test development manager, says that, while both Cadence and Mentor have done a good job supporting users in netlist development, both have had "gaping holes" in automatic test pattern generation (ATPG) capability. "They've given users no support in delivering test vectors," he says. "Older ATPG tools didn't seem to comprehend a real design, and they tended to generate test vectors that had no relationship to what a tester would use or an ASIC vendor would need."

The development work of Cadence and Ericsson is taking place within the context of an actual complex-ASIC design project. The goal of that project, according to Ericsson, is to get from specification to first silicon in one year. To do that, Ericsson is looking for a top-down design methodology to master complexity, a smooth design flow with few iterations and a powerful design automation solution to minimize lead times. According to Jorgen Hjert, manager of microtechnology at Ericsson, "both Cadence and Ericsson agree that test issues can't be addressed through a point-tool approach, but must be an integrated process throughout the design cycle."

What are some of the specific testability demands that Ericsson designers have written into the test specifications for Cadence? One is that testability synthesis must be a well-integrated part of the synthesis activities. Another is that designers must be able to apply both testability synthesis and test pattern generation to subblocks of the design.

Rick Friedman, Cadence's test products marketing manager, says that the key demand of designers is that test to be made part of the design environment. "They're looking for us to make design tools smarter about test, from front to back end, not for us to make smarter test tools," he says. "The concept of using synthesis and testability requires a new way of doing things. For test synthesis, we have to look at what designers do and enter that into the tool."

With Cadence's Test Solution, users will add testability at the functional level before synthesizing to gates. Optimization for area and performance will take place after scan insertion. Cadence will be offering a full-scan strategy "without the impact of full scan," claims Friedman. "The synthesis program will analyze the logic and take advantage of what's already there."

Test Solution will be an option of the Synergy synthesis family. The tools will be built around Cadence's Framework II-based Composer front end. In addition to test synthesis, the test environment will include logic and fault simulation and ATPG. JTAG synthesis will require some designer input, and BIST will be available later.

Will test synthesis be connected to Cadence's Preview floorplanner? "Yes," says Friedman, "since Preview is linked to synthesis, and test synthesis is part of synthesis." Friedman says full integration of the tools will take place by November.

Testability built into 8.0

Steve Eichenlaub, sales and marketing development manager of Mentor Graphics' simulation, synthesis and test division, says that Mentor's new ATPG products are on schedule for shipment this quarter. Mentor is offering both a full-scan-based, combinational ATPG tool (to be used with AutoLogic synthesis) and a partial-scan, sequential ATPG tool devel-

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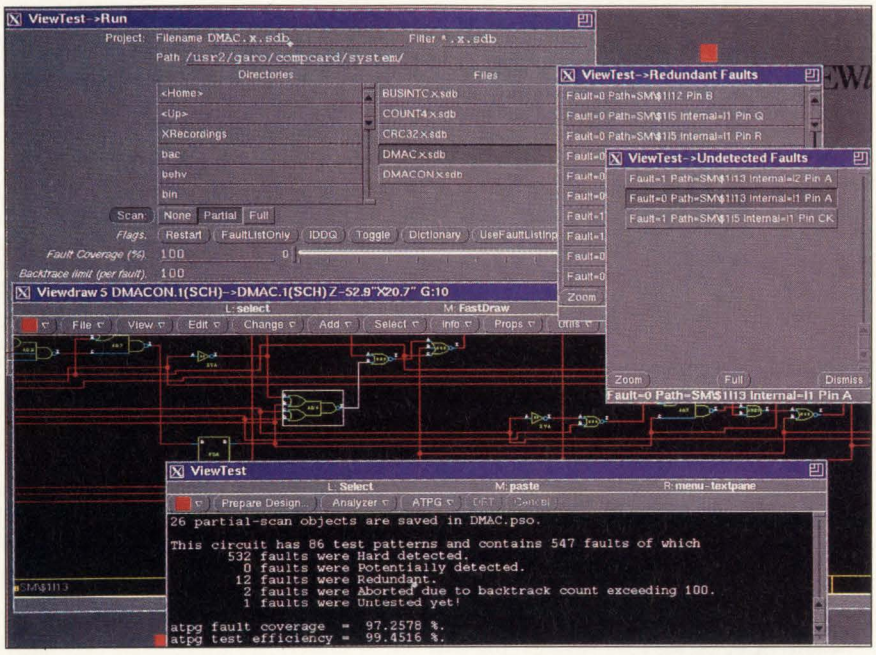

Viewlogic has integrated the ViewTest family of automated ASIC test programs into its new Unix-based Powerview toolset. ViewTest test synthesis works with Powerview's synthesis package, ViewSynthesis, to build highly testable ASICs.

oped by CheckLogic Systems (San Jose, CA). Eichenlaub didn't indicate whether Mentor has completed integration of the ATPG tools with AutoLogic at the database level.

Mentor's ATPG tools will fit within a language-based, top-down design flow as well as a more traditional, schematic-driven design flow. Although integrated into Mentor's Version 8.0 Falcon Framework, the ATPG products will also run well on designs that weren't created within 8.0, according to Eichenlaub.

Viewlogic shipped beta copies of its ViewTest testability tools about a month ago. Integrated into the company's new Unix-based Powerview toolset, ViewTest is scheduled for next-quarter shipment to its first customers. ViewTest test synthesis works with Powerview's synthesis package, ViewSynthesis, to build highly testable ASICs. The test technology, licensed from start-up Syn-Test Technologies (Sunnyvale, CA), supports partial-scan, non-scan and BIST methodologies, as well as full-

scan. Viewlogic hasn't yet officially announced JTAG support.

Synthesis-based solutions

GenRad users might want to look at TestDesignA test synthesis from Design Automation Products (Fareham, Hampshire, UK), a division of GenRad. TestDesignA is catching up to the other half of GenRad's HiDesignA synthesis package, the LogicDesignA logic synthesis module, which has been shipping since June. Both logic and test synthesis are part of GenRad's VHDL solution and are integrated with System HILO 4 verification tools. The first release of TestDesignA incorporates support for full-scan, fault-simulation and combinational ATPG.

Although GenRad plans to link its sequential ATPG tool to its test synthesis, early users will have to manually specify partial scan. GenRad also plans to extend its support to JTAG and BIST. In addition, the company offers a tool that can turn around a library for test, simulation and synthesis in two to six weeks.

A feature that will be useful, according to GenRad, is that scan-cell connection is driven by physical layout. The test synthesis program extracts the coordinates of scan cells and connects those that are physically closest. TestDesignA incorporates pin-to-pin and path-based timing analysis, as well as concurrent fault simulation.

Dazix also ships a test synthesis product. TestSyn is one of five new synthesis engines comprising Dazix Synergy. (Synergy is a synthesid technology developed by AT&T Bell Labs and marketed exclusively by Dazix.) TestSyn and the other modules have been tightly integrated at the database level with all existing Dazix applications, including VHDL simulation, gate-level logic simulation, IC layout, and schematic capture and analysis. TestSyn introduces test logic into the synthesized circuit and automatically generates test vectors. It operates with the timing-driven logic synthesizer and optimizer to ensure that the modified testable circuit meets area and timing constraints.

You'll have to benchmark these tools to discover if they measure up to competitive products on the market. Assuming you're looking for the highest performance tools, that is. You may be more interested in adequate tools that are well integrated into a familiar design flow. ■

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CAE/CAD TOOLS

Vendor alliance to offer encrypted Spice models

Mike Donlin, Senior Editor

As system speeds climb to 30 MHz and beyond, Spice models can help predict the analog behavior of digital components, even if their behavior has been validated with a digital simulator. The problem is finding accurate Spice models for high-speed drivers, buffers and device packages that will let you simulate analog behavior along critical paths. IC vendors have the necessary information, but are reluctant to get into the modeling business and are wary of including data in a model which would disclose proprietary process information.

Meta-Software (Campbell, CA) hopes to address this problem with its Meta Signal Integrity Alliance (MSIA) program. Meta is making an effort to organize IC vendors to provide modeling information to tackle ground bounce, noise problems, propagation delays, and other common effects that digital circuits encounter at high speeds. The alliance will also include companies that can provide Spice models for connectors and PCB transmission lines. In addition to providing accurate analog modeling capabilities through the alliance, Meta will ensure that proprietary process information remains safe.

Security is guaranteed

"One of the key ingredients in the success of MSIA will be the encryptor service," says Girish Kumar, applications engineer at Meta-Software. "Encryption ensures that proprietary data such as buffer models and netlist information is hidden from the user. The encrypted models will let you achieve a level of accuracy that you can't get using behavioral models or other approximation techniques. As far as winning the vendor's confidence is concerned, we can assure them that their proprietary data is safe, because we use the same encryption techniques for their models that we write for our own proprietary models. That's about the best guarantee we can give."

Shawn Hailey (standing), president of Meta-Software, discusses with applications engineer Anthony Stone the way in which encryption can protect proprietary information about a device.

Protected by this guarantee and strict non-disclosure terms, MSIA member companies will provide Meta-Software with detailed descriptions of the circuits they want to let their customers simulate. Meta then converts the circuit information to a vendor-independent format to avoid inconsistencies in circuit labeling, local ground definition or supply voltage parameters. Then the data is encrypted to protect proprietary information.

At present, there are five members in the alliance besides Meta-Software: Actel (Sunnyvale, CA) will provide models for its ACT2 PGAs; Advanced Micro Devices (Sunnyvale, CA) for its Mach PLD family; AMP (Harrisburg, PA) for its single-line connectors; Concurrent Logic (Sunnyvale, CA) for its CLi6000 series of FPGAs; and Xilinx (San Jose, CA) for its Series 4000 FPGAs.

Squelching the noise

Member companies see the alliance as a way of providing information about their products which some customers have wanted, but have been unable to obtain. Until now, demand for this information has been low, mainly because it's only used to analyze noise in high-speed digital designs. But as clock rates routinely climb over the 30-MHz threshold, alliance members realize they'll be asked to provide detailed information about their devices.

"These models are admittedly more complex than the average designer needs," says Atsuko D'Amour, product line manager at Xilinx. "Most of our customers can get by with the purely digital models to verify the behavior of their designs. But for those who need to analyze analog effects on critical paths, an accurate Spice model is essential."

Because Spice simulation is compute-intensive, it's unlikely that anyone will use it for full PCB simulation. But for critical path analysis, it can simulate noise that can hamper or cripple the performance of a circuit, even if its behavior has been adequately simulated from a

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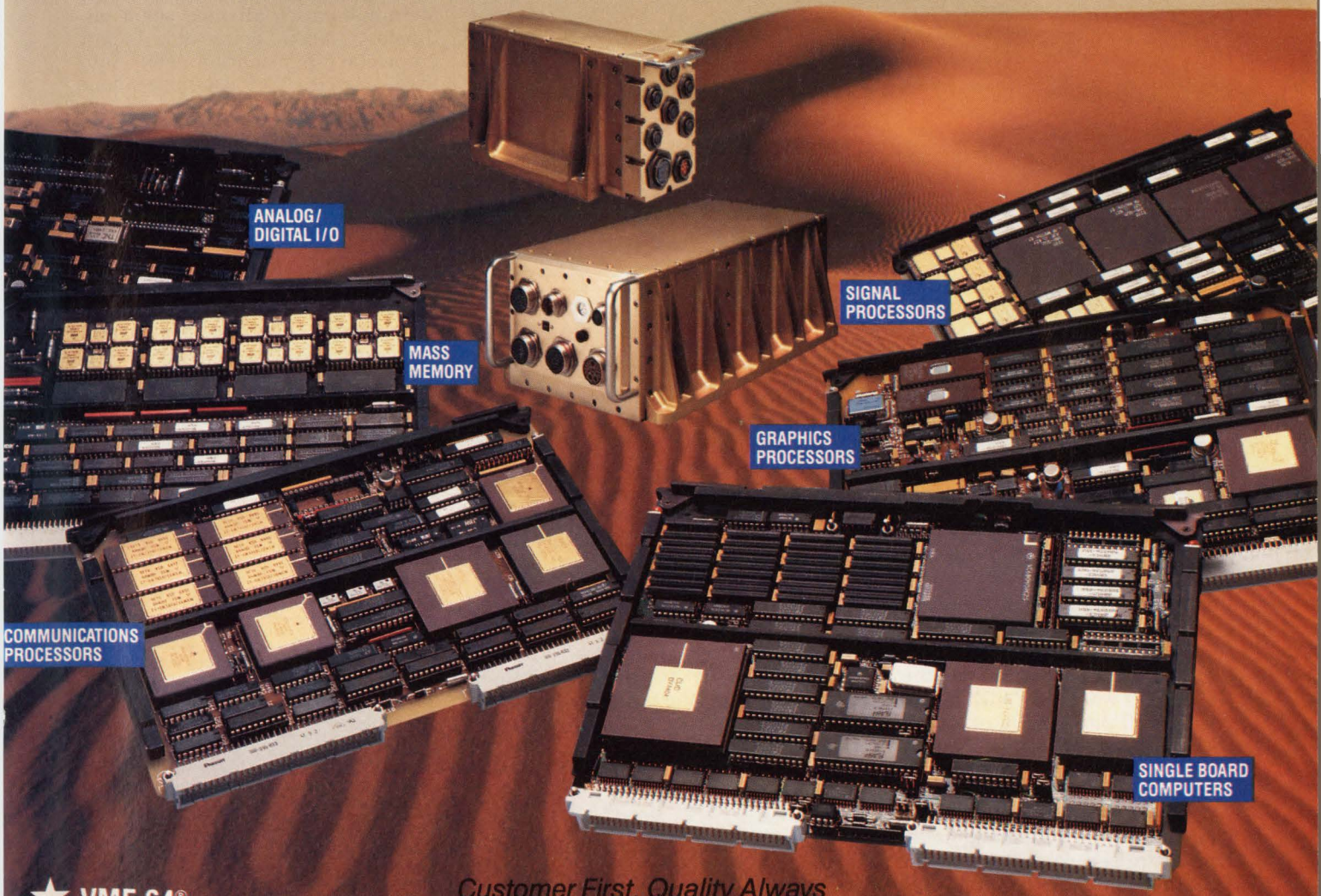

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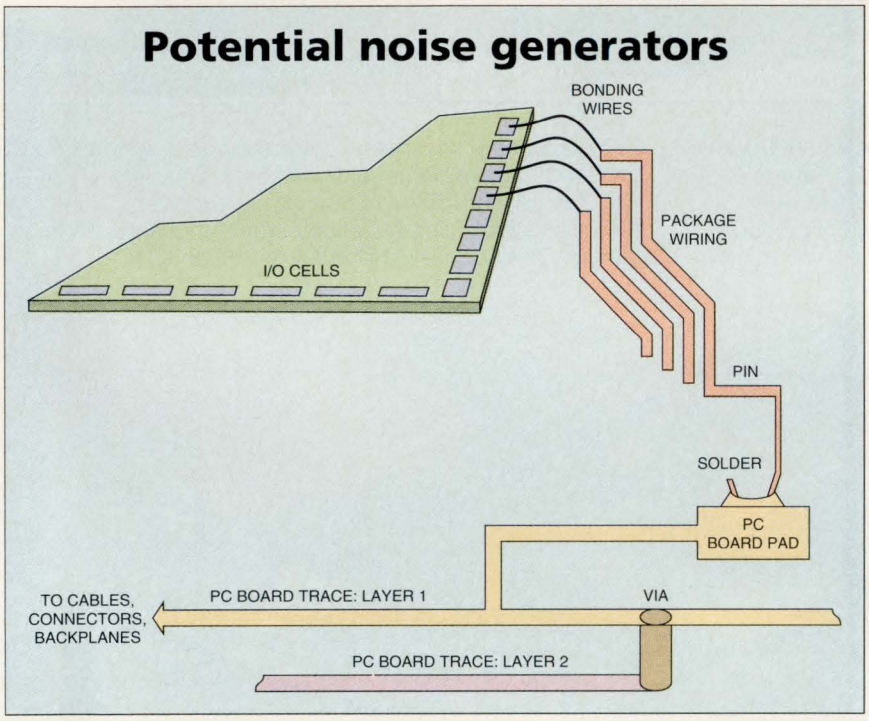
digital perspective.

"The roadblocks to effective high-speed digital designs are noise and delay," says Shawn Hailey, president of Meta-Software. "Ground-bounce noise, for instance, is generated where leadframes or other circuit wires can't be formed into transmission lines. The resulting inductance creates a voltage in the ground circuit, the supply circuit and the output driver circuit. Ground-bounce noise lowers the noise margins for the rest of the system."

The models produced by the alliance will work only with Meta-Software's HSpice simulator, mainly because they incorporate temperature and local ground planes into the simulation—a feature that Meta-Software says is unique to its simulator. "We let you change the temperature per element in the model," Meta-Software's Kumar explains, "and that information would confuse another simulator. We also let you create a local ground plane inside a subcircuit, because as you travel along a circuit, the ground level degrades. It rises up and the power supply goes down. It's important to be able to model this, so that you can compensate for those effects when you build your circuit."

Other effects besides ground bounce can be extracted with the models. Crosstalk simulation, for instance, can extract the coupled noise between two transmission lines—one quiet and one driven by the output of a tristated buffer. Delay differences resulting from driving data between slots in a backplane can also be simulated. Data is driven from the center of the backplane and examined at its extreme ends. The traces between slots are modeled as HSpice lossy transmission lines.



Signal integrity analysis becomes necessary on high-speed digital circuits when passive components generate analog effects. Every piece of the interconnect path illustrated here is repeated for all signals on the board. Singly and in groups, these pieces create crosstalk, noise, delays, skews, excessive load, and ground bounce.

A word of caution

Although alliances such as MSIA portend an era of model availability for users, there's a problem inherent in such agreements. Because the models work only with Meta-Software's HSpice, users of other Spice simulators will have to wait for similar alliances to get the model information they need.

"There's always a potential problem when you start to encrypt model information," says Paul Wang, CAE division president of Contec Microelectronics (San Jose, CA). "The process of hiding proprietary information means that the resulting models will be simulator-specific, unless there is a standard that everyone can write to. I don't think that a standard is feasible right now, because everyone alters Spice to give it their own added value. So the only way to provide every simulator with this information is to have an alliance with each vendor. That's an unwieldy scenario."

Caveats aside, the members of Meta-Software's alliance seem enthusiastic about being able to put proprietary information safely into their models. "I'm not sure about other alliances in the future," says Joel Rosenberg, marketing director at Concurrent Logic, "but I do know this gives us an avenue that we didn't have before. For some of our customers, true simulation of critical paths necessitates two operations—digital simulation, to verify the logic in the design, and analog simulation, to address the harsh realities of the real world. It's good to know we can provide all of the needed information without giving away the store." ■

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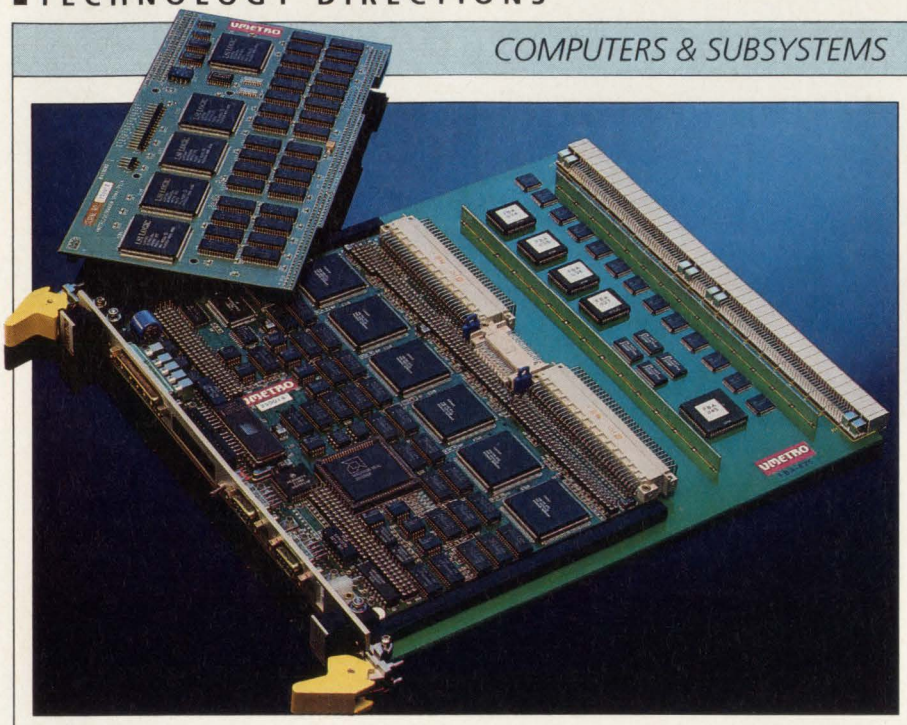

VMetro's Futurebus+ analysis system is the first modular approach with both a VMEbus analyzer and a Futurebus+ adapter. Shown are the company's latest VMEbus analyzer, the VBT-325, the add-on 200-MHz timing analyzer and the FBT-625 adapter board. Combined, they provide a complete Futurebus+ analyzer with the capability to look at 282 signal lines, yet occupying only a single Futurebus+ backplane slot.

Futurebus+ analysis tools ease transition from VME

Warren Andrews, Senior Editor

Futurebus+ systems will soon be commercially available as Digital Equipment Corporation and other manufacturers introduce products later this year. The development of boards and the emergence of systems will undoubtedly create a heavy demand for debugging and analyzer tools—particularly those that will simplify VME-to-Futurebus+ design. While a few analyzer products have been announced, the only one that's available to date is a product from Future+ Systems (Westford, MA). The Future+ Systems analyzer comprises a Futurebus+ extender card with interface and protocol circuitry, which can be connected to a logic analyzer to evaluate the signals captured by the front end.

This single-product market is about to change as VMetro (Houston, TX) introduces a Futurebus+ analyzer this month. It's been designed to provide some significant advantages to board and system developers coming from (or bridging to) a VMEbus background. "VMetro has broad experience in developing VMEbus analyzers," says company vice-president John Simpson, "and recognizes the need to address the Futurebus+ market. Initially, the company planned to develop a specialized Futurebus+-only analyzer."

Simpson explains that, given the way the technology's developing and the pace at which VMEbus board and system developers are migrating to Futurebus+, a logical first step was to make a VME-compatible device. The first component of the new Futurebus+ system, then, is a VMEbus analyzer the company calls the VBT-325.

This advanced version of VMetro's earlier products is a full-featured, 50-MHz, VMEbus and VME/P2 state and timing analyzer. It can be enhanced with the TIM-200, a 200-MHz timing analyzer that can be piggybacked on the VBT-325, providing additional signal capability for VME and VME/P2 lines.

The second major component of the VMetro Futurebus+ analyzer, the FBT-625, is a Futurebus+ adapter card. This is a Profile A-, B- or F-sized Futurebus+ card which can accept the VBT-325 VME analyzer with or without the piggybacked TIM-200. The adapter card includes Futurebus+ transceivers and BTL-to-TTL translation, control and glue logic needed to acquire and sample Futurebus+ signals, circuitry to implement on-board system reset and a central arbiter that lets the analyzer function as the system controller in a Futurebus+ system.

Single-slot design

Although it's a three-tiered piggyback design, the analyzer takes up only a single slot in the system backplane and can be operated through a variety of standard platforms, such as ASCII terminals, PCs or Unix workstations. The basic unit is capable of sampling all 177 Futurebus+ signals and storing up to 32,000 cycles. It provides protocol-sensitive, multiple-edge sampling, automatically aligning arbitration, command, address, data, and status lines into one line in the trace buffer. In addition, it offers four full-speed, 177-input-event comparators with RANGE, DON'T CARE and NOT operators in the analytical engine.

The analyzer also supports complex trigger generation based on precision time delays and variable event counts at each trigger level. It also stores time tags in a buffer, with each bus cycle allowing absolute and relative timing measurements down to 20-ns resolution.

With the 200-MHz timing-analyzer option, the system samples an additional 105 Futurebus+ signals at 200 MHz, storing an extra 32,000 cycles on all channels. This extends the total sampling capacity to 282 simultaneous channels, with a high-speed (163.84-µs) timing window on the 105 signals aligned around the trigger in a separate 32,000-cycle trace. The option card operates simultaneously with the 50-MHz state analyzer to produce automatically aligned, time-corrected, state/timing displays, with timing

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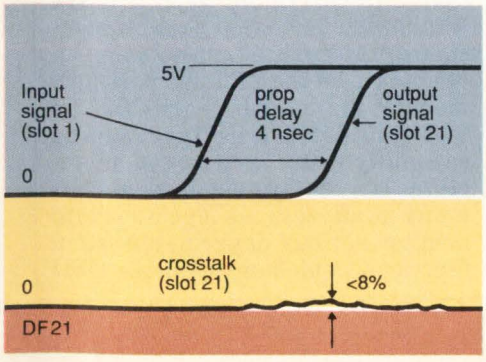

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Leveraging

"VMetro's solution," says Simpson, "lets engineers and designers leverage off the hardware, the software and—as important—the accumulated body of problem-solving knowledge acquired in the VME world as they move to Futurebus+. Any Futurebus+ team which is migrating or embedding an existing VMEbus design into Futurebus+ will have the opportunity to use the new analyzer to fully characterize the design on both buses, using effectively the same instrument. Only the protocol semantics necessary to describe the unique properties of the target bus will change in the user interface."

Simpson remarks that the inherent "look, touch and feel" of the analyzer will remain constant for both buses. This will undoubtedly save VME and Futurebus+ project engineers many hours of learning-curve time and defer the cost of dedicated test equipment.

But providing a composite Futurebus+ analyzer is just part of VMetro's strategy. Simpson says that the company is currently using flash memory in its FBT-625, but plans to migrate to a PC/workstation-hosted, window-driven user interface called InsideView for both Futurebus+-based and VMEbus-based products. In addition, the company will retrofit existing products to the new interface.

Such an interface provides two major advantages to designers, according to Simpson. First, it lets VMetro turn out product capabilities much faster on floppies than on EPROM, making it more responsive to emerging requirements. Second, by migrating the user interface away from the core analyzer, the company can focus on the front end and user interface as different entities. The result: the user interface will be richer, since VMetro no longer has to create the interface environment; it simply has to map to a standard PC host.

Another advantage

"Rehosting the user interface onto a machine with multiple interactive display capabilities," states Simpson, "has yet another advantage. It gives engineers the ability to use multiple bus analyzers simultaneously in a given system, providing integrated control over all functions and views of all aspects of the target system. To realize this opportunity, VMetro is also developing an adapter to let the VBT-325 passively monitor the local bus activities on 68K/88K VME boards. The resulting capability will let you install an analyzer on the system bus, and as many analyzers as necessary to monitor various desired subsystem functions implemented inside CPU

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and I/O boards using a single, interactive point of control."

While VMetro's composite technique provides a systematic approach to Futurebus+ bus analysis, it also offers one of the first Futurebus+ carrier boards sporting a VME mezzanine. Although it still isn't known exactly what the Futurebus+-to-VME bridge will look like, it's possible that carrier boards such as that used by VMetro might provide a convenient I/O connection when only a single VME I/O board is required. In such approaches, bridge functions could be limited, since only a small subset of the VME specification need be accounted for in interfacing to a single board. ■

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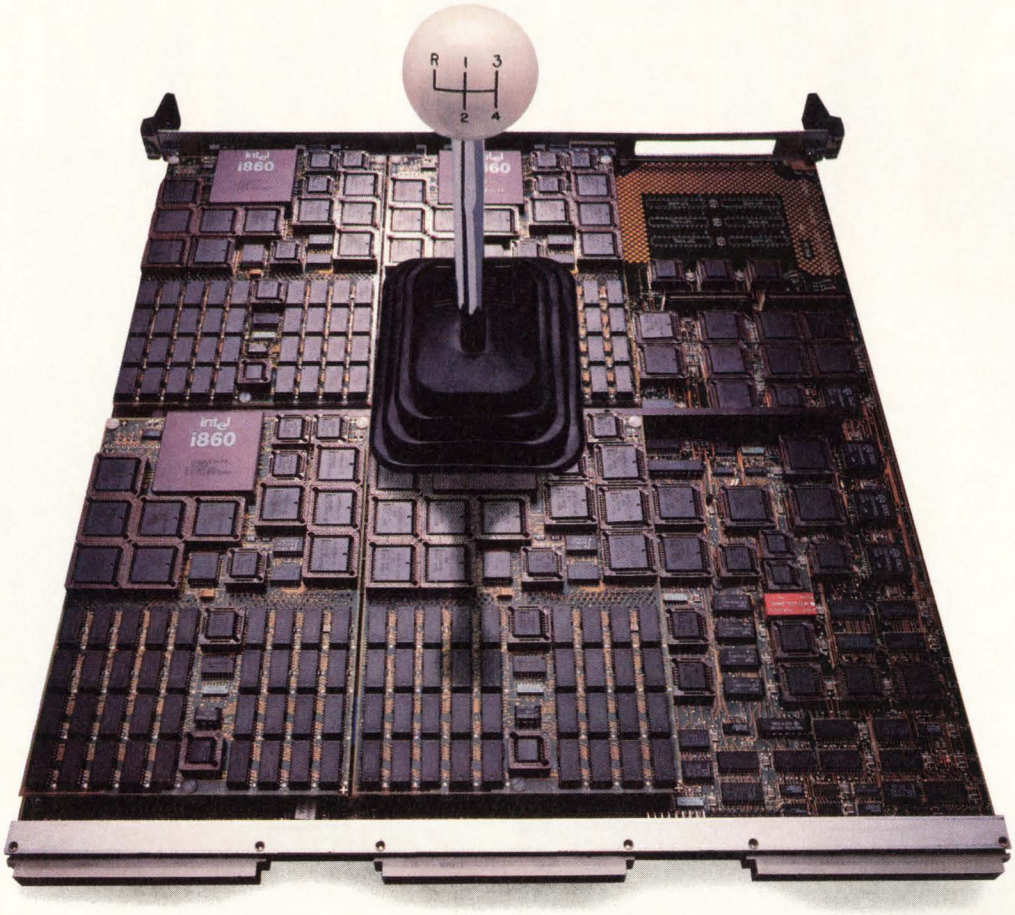
A New Product Development article entitled "Simulation accelerator speeds behavioral-level VHDL" appeared in the August issue of Computer Design describing Zycad's VHDL Instruction Processor (ViP). In that piece we stated, "...a single-board ViP offers the performance of a 70-Mips workstation...." According to Zycad, the ViP offers 40 times the performance of a 70-Mips workstation.

That performance estimate was contained in the article as orginally filed by Barbara Tuck but was deleted by an over-exhuberant Editor-in-Chief during a final review of editorial pages. The Editor-in-Chief sincerely apologizes and regrets any problems the error caused.

If you would like more complete information on the ViP product, contact Pamela Mayer Bernal, vice-president of marketing, or Charlie Cheng, product marketing manager at Zycad, 1380 Willow Rd, Menlo Park, CA 94025, (415) 688-7400.

And while we're admitting our errors, the telephone number given for American Arium in the Product Focus on logic analyzers in the July issue had an incorrect area code. American Arium is located in Tustin, CA and the correct number is (714) 731-1661. No over-exhuberance here, just a typo.



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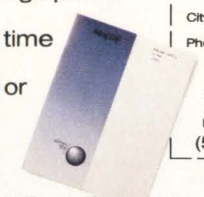

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SOFTWARE & DEVELOPMENT TOOLS

CASE tool breaks away from traditional development model

Tom Williams, Senior Editor

A CASE environment for C code has broken with the development model followed by most CASE tools. Instead of using the requirements analysis model for software engineering, the Ensemble toolset from Cadre Technologies (Providence, RI) focuses on what the company calls an "implementation model," which it claims more closely matches the way people are approaching software design and development problems today.

Most CASE tools adhere to the waterfall model, where structured analysis is first used to specify the requirements of a system. These requirements are used in the design stage to create the overall structure of the program. Next comes implementation (or coding), followed by the testing and maintenance stages. With the waterfall model, there's little thought given to going back "upstream," and it's generally difficult to do so. This inability to smoothly move up and down the model has been a major complaint of early users of CASE tools—and an important factor in the slow acceptance of such tools.

The reality is that 80 percent of the design community doesn't follow the waterfall model. "We're finding there are almost no clean-sheet starts. They're always reusing something," says Caine O'Brien, director of marketing for Cadre's Portland, Oregon operation, "and we're not going to force a waterfall process onto the mass market."

Recycling possible

Cadre describes Ensemble as following an "implementation-focused" model, where you usually begin by implementing some old and some new code, do some testing and maintenance work and maybe a little upfront analysis—but you don't have to do these things in any rigid order. With Ensemble, "you can use structured design as a starting point if you want to, but you can also use pieces of existing code," says O'Brien.

Ensemble is a modular toolset aimed at providing understanding of existing code both at the higher system level and the lower functional level. It lets you produce code from designs, automate and verify the testing of code and automatically produce documentation.

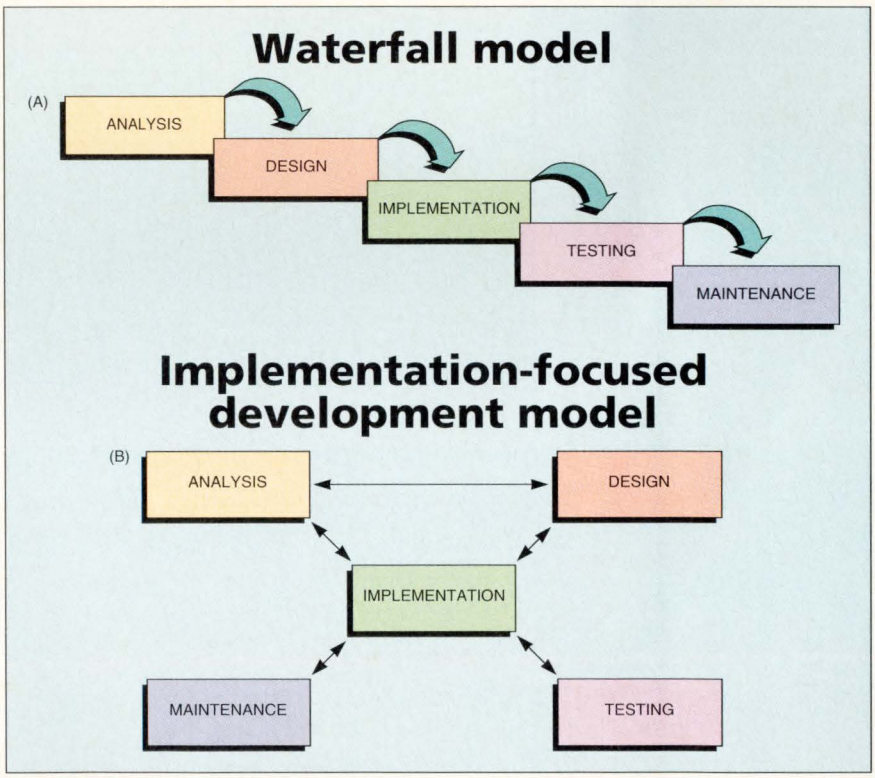
Working with the Teamwork database used by Cadre's family of Teamwork CASE tools, you can integrate Ensemble into the Teamwork environment if desired. In addition to the shared database and user interface, Ensemble consists of system-level and function-level understanding modules, a construction module, test generation and verification modules, and a documentation module.

Reverse engineering supported

The system understanding module supports reverse engineering of existing code. It can also extract a complete structured design representation of an existing program, including a data dictionary with all its definitions, any comments contained in the source files and information on what functionality came from which source files. In addition, the diagram created by the module shows the flow of both control and data in the system.

"Our goal is to walk in and help people figure out code in a matter of hours and create tests for code about the same time, " says O'Brien. To accomplish these ends, you usually start with the system understanding module and the database. The other modules can be added as needed.

The function understanding module, for example, lets you view a different level of what the system understanding module generated. By clicking on a box at the system level, you open up a diagram of that function's control flow. The control flow diagram looks much like a flow chart, with each decision point, for



The classic CASE waterfall model of software development (a) supposes an orderly progression from analysis through design and test down to maintenance. CASE tools following this model have seemed awkward to users in the past. Ensemble (b) assumes that development activity is centered on implementation and lets you move freely between design, analysis and test.

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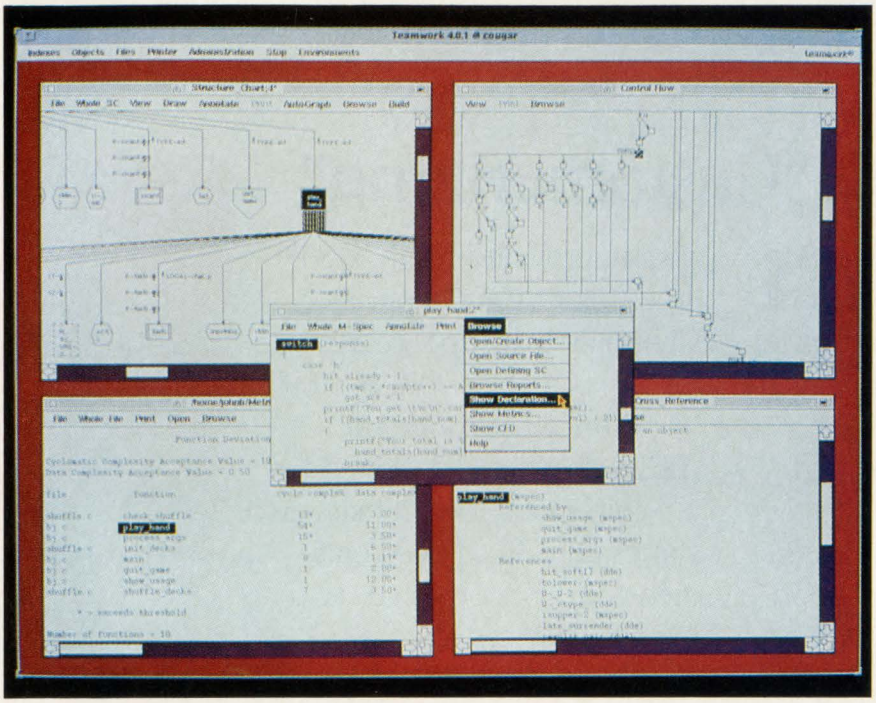
SOFTWARE & DEVELOPMENT TOOLS



Cadre's Ensemble toolset lets you migrate from high-level structure charts to control flow diagrams and source code in adjacent windows.

example, represented by a diamond shape. Clicking on a point in the control flow diagram—or at the structure chart level—will take you to the corresponding place in the source code. If you happen to be at a decision point at the control flow diagram level, you will end up indexed to the line in the source code representing that decision point.

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Ensemble's ability to produce complexity metrics aids in the auto-

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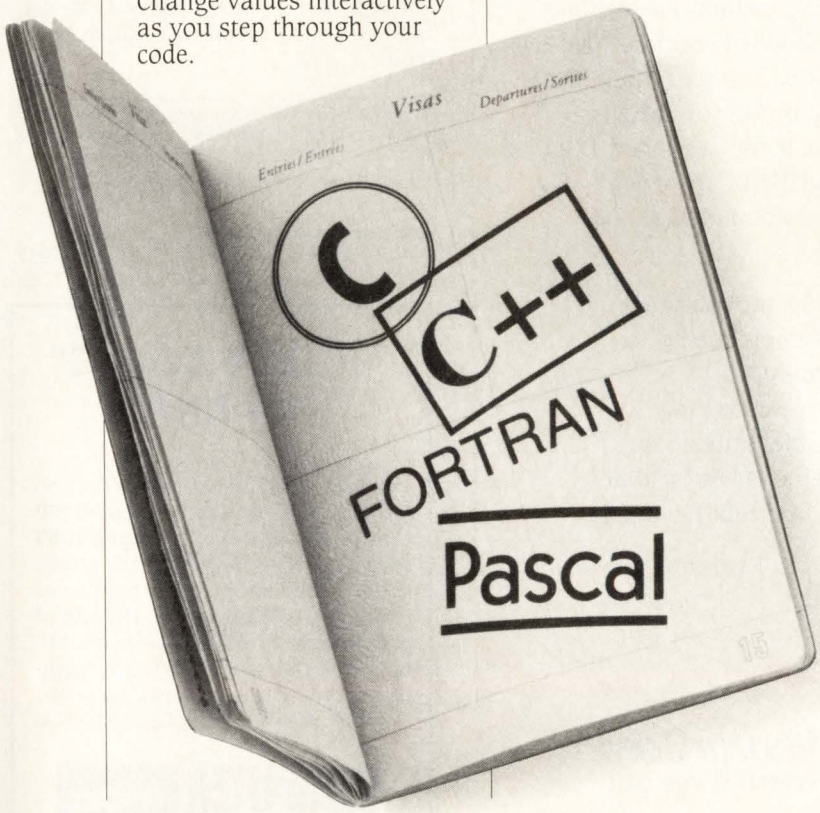

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CIRCLE NO. 38

matic generation of test cases. There are metrics for both data and control complexity because the two are not always the same. This lets you concentrate on those sections of code most likely to contain problems. The automated test generation module takes advantage of the contents of the data dictionary to produce test suites. It can use the data dictionary, for example, to determine the upper and lower boundaries of variables. It can then automatically generate test cases that break these boundaries to see how the system reacts. "It should be possible for code created today to be automatically tested tonight and the results examined tomorrow," says O'Brien.

Test verification uses the same design database to produce information on test coverage. The module inserts software probes into the code to determine which statements have been exercised, as well as which branches have been taken and which haven't. It marks source code to indicate coverage, but it also lets you look at the diagrams. At the control flow level, solid lines connecting elements indicate paths tested, while dotted lines show paths that haven't been tested. Automated test case generation and verification, along with the ability to identify complexity, make it easier to test what most needs testing and to assure the desired level of testing has been achieved.

The ability to move around freely in the development cycle lets you work in a way that's more comfortable, especially in small to medium projects. "We want Ensemble to fit into the environments that developers are using today," says O'Brien, "rather than trying to replace their tools." ■

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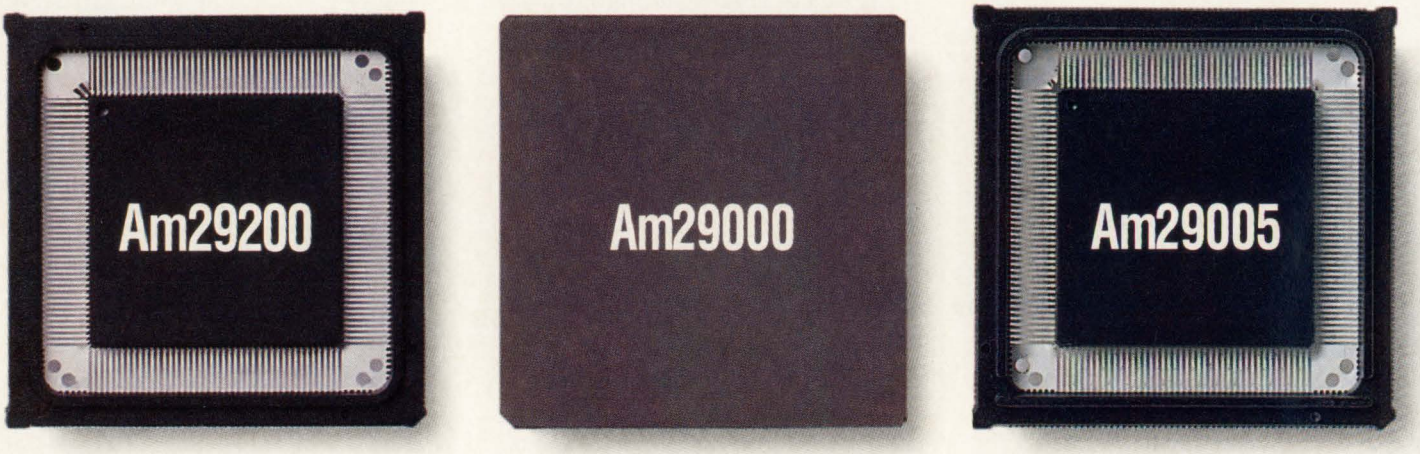

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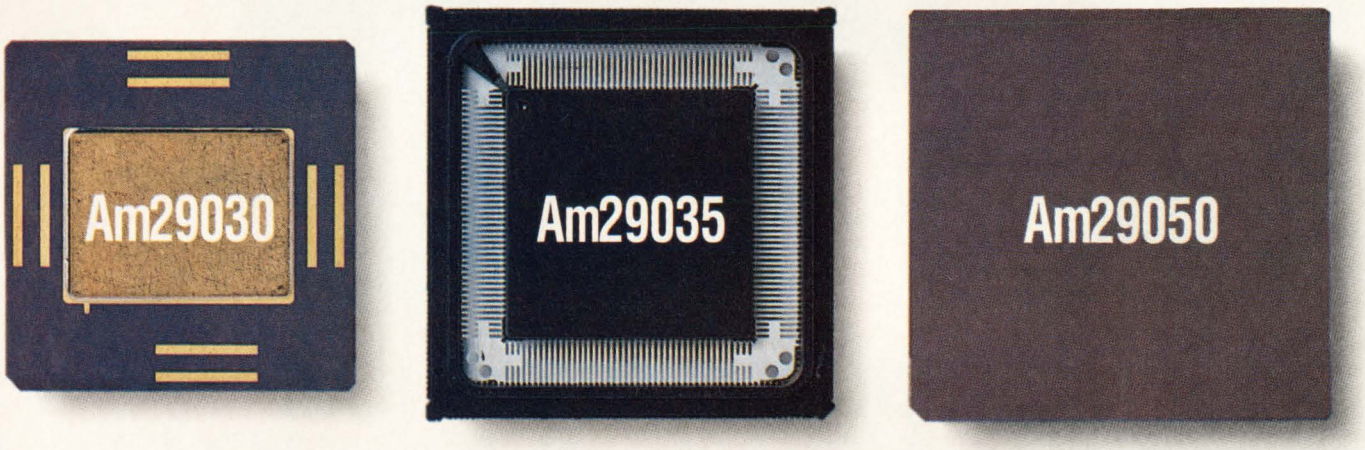

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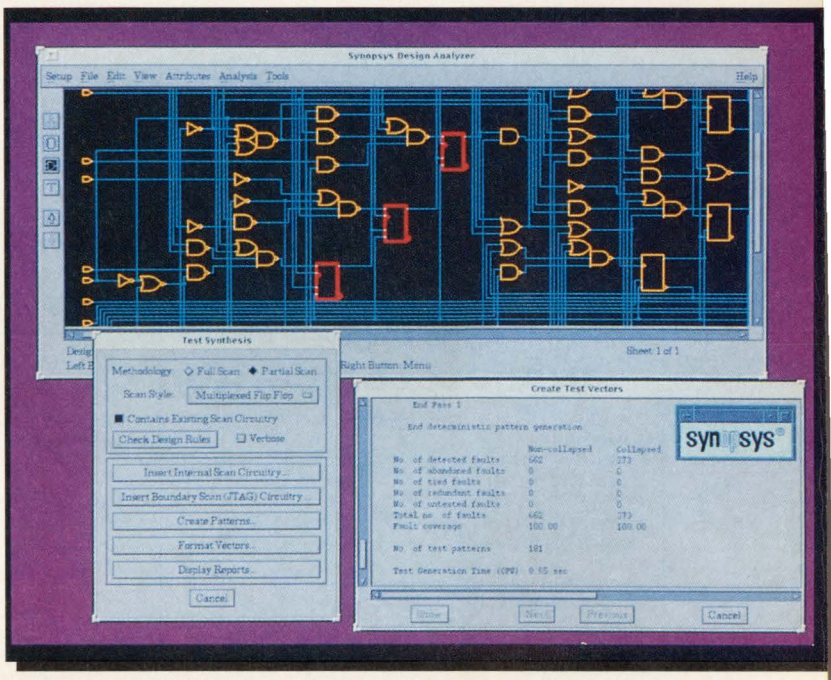
CIRCLE NO. 42

ASIC testability tools force trade-offs in silicon, performance and coverage

Will you trust your complex ASICs to test synthesis? Can you take hits in silicon and speed in exchange for quality? Does integration or tool performance come first for you?

Barbara Tuck, Senior Editor



Synopsys test synthesis automates various testability methodologies (bottom left). Constraint-driven partial scan, which ships with Test Compiler Plus at year's end, combines constraint-based scan selection, timing analysis and sequential ATPG to provide predictable high-fault-coverage results (bottom right) with minimal impact on design area and performance (top).

Although testability is finally getting the respect it deserves from both vendors and users, it's clear that if you're designing testability into complex ASICs using today's tools, you'll still have to make trade-offs. But if you're familiar with the strengths and weaknesses of the tools and techniques, there's a good chance you won't have to sacrifice what's most important to you.

Now is a good time to evaluate and benchmark such tools, since a number of products on the market have just been enhanced and new testability tools from broadbased EDA suppliers will be shipping over the next few months (see "EDA leaders getting serious about automatic test generation," p 33). Before you do, however, you have to know what to look for and what the trade-offs are.

Extending synthesis to test

If you use Verilog or VHDL, you may want to leverage your synthesis capabilities to build ASICs that are highly testable as well as providing high-performance. Although the term "test synthesis" is being used very loosely today as an umbrella to include almost any testability enhancement tool, its strict interpretation implies tight integration with a synthesis tool; the ability to select the best scan strategy based on area, performance and testability goals; scan-insertion capability; and optimization with test structures in place.

Test Compiler from Synopsys (Mountain View, CA), with an installed base of 200, for example, is limited to full-scan implementation but otherwise fills this bill. The new Test Compiler Plus, due to ship at year's end, extends to constraint-driven partial scan and sequential automatic test pattern generation (ATPG).

Jim Kleidon, a member of the technical staff at Sun Microsystems' (Mountain View, CA) SBus engineering group and a first-time user of Test Compiler, is in the middle of the SBus Goldchip design project. With 90,000

to 100,000 used gates, including FIFO RAMs, the SBus Goldchip is a general-purpose 64-bit DMA interface chip for the RISC bus architecture. "The complexity of the chip mandated that we find a more efficient way to incorporate scan," says Kleidon, who previously wrote HDL code structurally and hand-instantiated macros. "The Test Compiler selects the fastest and most efficient scan macros from the vendor-specific target library."

Since Test Compiler is integral to Sun's standard Verilog/Synopsys design flow, the impact of integrating and learning new tools was minimized. Designing with Motorola H4C libraries, though, did mean designers had to use the Mustang ATPG tool, a requirement for Motorola's release.

A very straightforward design with a single clock domain and purely synchronous operation, the SBus Goldchip is an ideal candidate for full scan. To identify and fix testability problems at an early stage, the design group applies Test Compiler to each block as it's synthesized, checking design rules, correcting errors and generating initial fault coverage results on blocks as they're developed. Test Compiler can be directed to exclude faults covered by built-in self-test (BIST).

First-pass fault coverage for the entire SBus Goldchip design, excluding RAMs, was 95 percent, reports Kleidon, and the design group is now approaching 98 percent. Sun designers have seen a silicon overhead that's typically been 6 to 8 percent and a penalty of 1 ns or less in the overall timing. Estimates on savings in schedule, however, are on the order of four to six weeks.

But Kleidon warns others, "When shopping for test synthesis tools, be sure the vendor-specific target library has scan-equivalent D flip-flops (D FFs). If this isn't the case, Test Compiler won't substitute the non-scan FFs with equivalent scan versions." (Twelve ASIC vendors currently have certified ASIC libraries for Test Compiler.) Kleidon also notes that his company's designers had to exclude JTAG macros because, without a complete functional description of such macros, Test Compiler can't generate tests for that logic.

The forthcoming Test Compiler Plus does include boundary-scan synthesis, which automatically synthesizes the JTAG 1149.1 test specification and formats test patterns in the 1149.1 protocol. "You can set performance, area or test coverage as your most important issue. It'll give you a balanced design," Kleidon says.

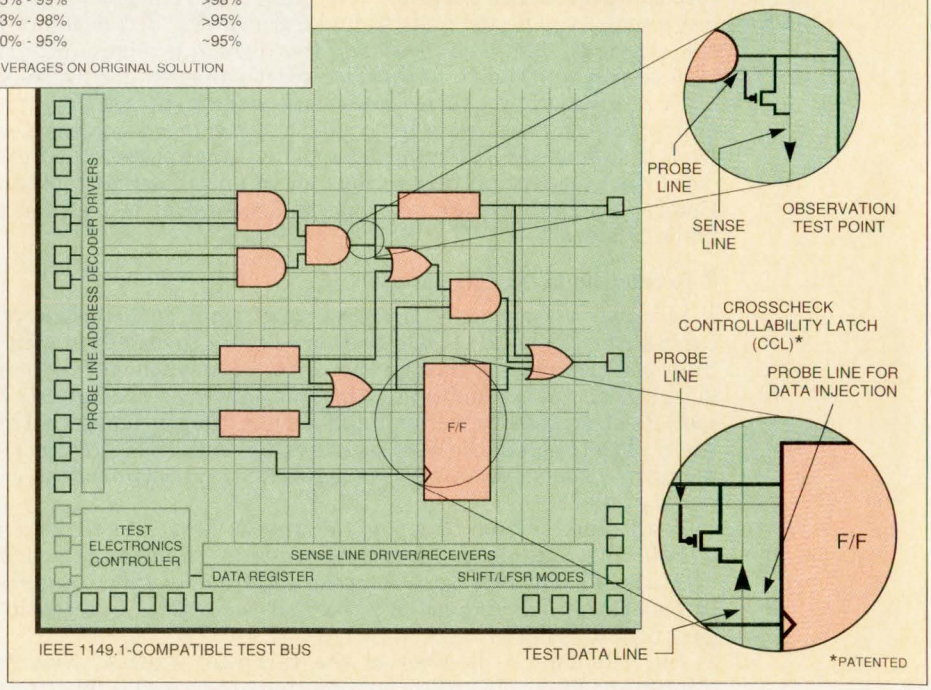
To offer partial-scan technology, Synopsys had to rewrite the core of its timing optimizer. Now, with timing-driven sequential optimization, Synopsys synthesis can be applied to multiclock, multicycle and multiphase designs. Another benefit of

CrossCheck product comparison

	ORIGINAL SOLUTION	CX-ARRAYTEST
FEATURES		
OBSERVABILITY	YES	YES
CONTROLLABILITY	NO	YES
ATPG	NO	COMPLETE
AREA IMPACT	10% - 18%	10% - 20%
LIBRARY IMPACT	—	CCL
BENEFITS		
DESIGNER INPUT	NODE TOGGLE*	NETLIST
NETLIST MODIFICATION	NONE	NONE
DESIGN STYLES	ANY	ANY
PERFORMANCE IMPACT	NEGLIGIBLE	<2%
FAULT COVERAGE		
SYNCHRONOUS	95% - 99%	>98%
GATED CLOCK	93% - 98%	>95%
ASYNCHRONOUS	90% - 95%	~95%

*100% NODE TOGGLE REQUIRED FOR FAULT COVERAGES ON ORIGINAL SOLUTION

CrossCheck on-chip test engine



If you use a silicon vendor that licenses the CrossCheck Technology (San Jose, CA) alternative to scan methodology, you don't need to be involved in test development at all. CrossCheck's new CX-ArrayTest solution, which combines its On-Chip Test Engine with design analysis and ATPG software, can perform fully automatic test pattern generation without modification of your netlist. The CrossCheck Controllability Latch (CCL) is the key. It permits the CX-Array software to inject data into a latch independent of the netlist. The CCL uses two embedded probe lines plus a sense line to control the latch data injection. The table compares CrossCheck product attributes before and after CX-Array Test.

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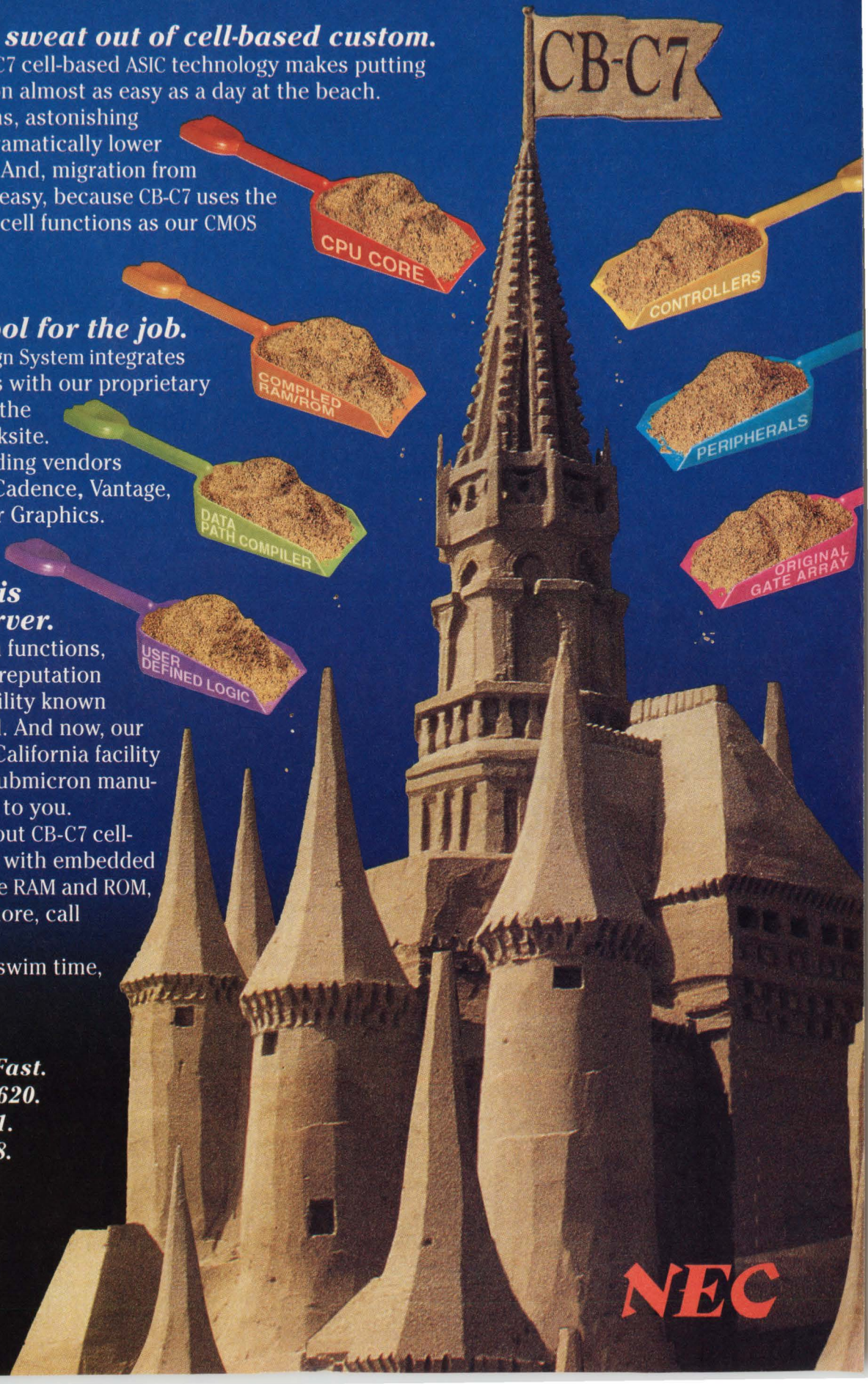

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the new technology is automatic time borrowing, which lets you optimize latch-based designs for faster clock speeds.

Months off the design cycle

Although staff engineer Mark Spiotta of the Motorola Land Mobile Product Sector (Schaumburg, IL) suffered a 20-percent area penalty using Test Compiler's full-scan methodology on a heavily register-oriented design, he says he'd use it again over the new partial-scan methodology. "We got working silicon first pass," boasts Spiotta, referring to a 57,000-gate ASIC that functions as a data and audio interface to a DSP chip in a two-way radio repeater.

This ASIC project was Spiotta's introduction to VHDL and logic synthesis, as well as to automated test. "We paid a price in silicon," he reports, "but we got 99-percent fault coverage and shaved three months off the development project." As long as the 20-percent increase in area didn't force a move up to the next H4C array size, there wasn't a problem, according to Spiotta. "Silicon overhead can bother you a lot or not at all," he adds. Motorola's H4C library goes from eight gates/FF for a non-scan FF to a dozen gates/FF for an equivalent scan version.

To design full scan into 11 ASICs going into a multiprocessing server, VLSI manager Rajiv Deshmukh of the Computer Products Division of Silicon Graphics (Mountain View, CA) chose the TestGen partial-scan sequential ATPG tool from Sunrise Test Systems (Sunnyvale, CA). It handles up to 100-percent scan. He is using the LCA200K ASIC family from LSI Logic (Milpitas, CA) for his 50,000- to 80,000-gate ASICs, with clock rates up to 75 MHz. Until this design project, he used LSI Logic's scan ATPG tool (SATPG), which operates on a structurally correct netlist at the end of the design cycle. "This time," Deshmukh says, "I didn't want to wait until the last step in the process."

Although he uses Verilog and Synopsys synthesis, Deshmukh chose TestGen over Test Compiler. "When I evaluated Test Compiler, I found it still buggy. If you do your design hierarchically, Test Compiler works at the individual block level, but when it comes to rethreading scan for the entire design at the top-level synthesis step, it gets hung up. It's great for 20- and 30-MHz logic, but it's kludgey for high-performance logic running at 50 to 75 MHz."

Asked about Deshmukh's experience with Test Compiler, Synopsys product marketing manager Kelly Gomes said that for certain design structures in Deshmukh's circuitry, there was indeed a bug that has since been fixed. "We'll be running the design through the new software," says Gomes. "There's no limit with regard to speed." As to density, Gomes points to Test Compiler's success with Sun's 100,000-gate SBus Goldchip.

Performance over integration

In the meantime, Deshmukh traded off the integration and synergy he would have had with Design Compiler/Test Compiler to go with Sunrise's TestGen—much to the chagrin of his CAD manager. "Our CAD manager is overstressed," he says, "because we're mixing the best point tools to get high performance instead of working with a single, integrated toolset." For the multiple ASIC project, Deshmukh is using Verilog, Synopsys synthesis, Sunrise's TestGen, a proprietary scan insertion tool, LSI Logic's floorplanner, and Quad Design's Motive for full-chip timing analysis.

What were the trade-offs the Silicon Graphics team was willing to make when it considered tools? According to Deshmukh, "We looked for a tool that could run on partial netlists. The run had to be overnight—time was of the essence. The exact percentage of fault coverage wasn't as important as how quickly we could insert scan and compile scan chains."

Although Sunrise touts the partial-scan and sequential ATPG capabilities of TestGen, the Silicon Graphics team tapped only the combinational capability, since it implemented full scan. Deshmukh reports that the LSI LCA200K library overhead for a scan-equivalent FF is an extra two gates/FF (from seven to nine gates/FF). Silicon overhead varied across the 11 ASICs, from 6 percent in some instances to 10 to 12 percent in others. The full-scan penalty on timing was 0.75 ns nominal and between 1.2 and 1.5 ns maximum.

How did a design-for-testability philosophy affect cycle time? "We had test vectors before sign-off rather than after," says Deshmukh. "We had been in the habit of sending a prototype out with preliminary vectors and then spending two to three man-months between prototype release and production release, developing a full set of vectors. With that methodology, we sometimes ended up compromising on coverage."

Ravi Bhatnagar, vice-president of new product development at Chips & Technologies (San Jose, CA), also reports that Sunrise's TestGen gave the best results for his particular application, which involved implementing full scan in Chips & Technologies' 350,000-transistor

IBM still adamant about full scan

IBM, which has been practicing level-sensitive scan design (LSSD) full scan for more years than most, is now looking for your ASIC business. Christine King, the ASIC product development manager at IBM Technology Products (Burlington, VT), says that now that IBM is pursuing the merchant market business, it will make its ASIC libraries available on third-party tools. "We want to give our users the same advantages with regard to ASIC testability we've had internally," she says.

"The impetus to partial scan has been driven by the false notion that scan costs silicon area," says Steve Oakland, advisory engineer at the facility. "In a wiring-limited ASIC product, 20 percent of the silicon area could be wasted anyway." He also says you shouldn't calculate overhead for full scan based on gate count. "Transistor count would be a lot closer. We typically see a 5-percent transistor overhead, translating to something less than 5-percent silicon area."

IBM's test approach incorporates LSSD, boundary scan and BIST capabilities. Like Synopsys, IBM uses timing-driven testability tools to optimize for area and performance with test structures in place. The tools cover transition faults as well as stuck-at faults.

With ASIC complexities climbing, IBM has been especially active, according to Oakland, in incorporating techniques to reduce manufacturing test costs

Super386, a completely synchronous, fully static CMOS design. Bhatnagar's team begins thinking testability at the very beginning of the design cycle. "By the time we finish writing functional specifications, we have testability specifications," he says.

There are areas that need improvement in the tools, and he advises you to watch for links to floorplanners. "We had to do the scan-chain ordering manually by modifying the schematics," according to Bhatnagar.

Although the version of TestGen Bhatnagar used was of no help in testing memory portions of the Super386, you can now get a version from Sunrise that's been upgraded to include behavioral modeling. With TestGen's Version 1.1, you'll get single-primitive RAM and ROM modeling as well as dynamic vector compaction, enhanced fault reporting, improved test generation, and new design audit features. TestGen also now includes interfaces to toolkits from Cadence Design Systems (San Jose, CA) and Mentor Graphics (Wilsonville, OR).

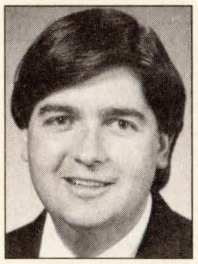
Behavioral models guide ATPG

If you're looking for a testability tool that's driven by behavioral models, you might also look at Test Design Expert (TDX) from ExperTest (Mountain View, CA), especially if you're interested in a minimum amount of scan. An expert system, TDX uses register-transfer-level (RTL) models to guide ATPG through your circuitry. Though TDX supports full scan, partial scan, BIST, and boundary scan, ExperTest encourages functional testing, claiming TDX gets higher defect coverage with far less design impact than is possible with scan or partial-scan methodologies.

Sun Microsystems design engineer Mike Parkin is evaluating TDX by running an 80,000-gate controller design through it. Destined for a Sun workstation, the controller has several register files and RAMs. Parkin, a Synopsys and Verilog user, chose TDX for his chip design over other tools, "primarily because the chip doesn't require scan."

"We can start with no scan and insert the minimum amount of test points or scan. We can use datapaths built into the circuitry to exercise the chip. Also, because TDX creates functional vectors, it detects delay faults and bridging faults in

Will ASIC test patterns be executable?



Many ASIC designers embrace internal scan hoping it will automate the test generation process. And scan automatic test pattern generation (ATPG) tools do produce test patterns quickly and automatically, but not typically in the form needed by logic simulators or automatic test equipment (ATE). Unless scan test patterns can be transformed and augmented quickly and automatically at each step of the test development process, the time and cost saved using scan design-for-test (DFT) methods will be frittered away re-entering test data.

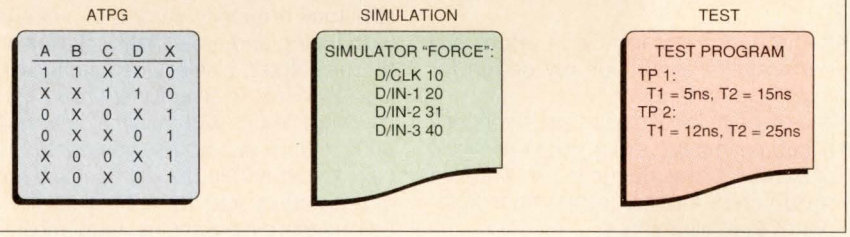
Same data, different form

Although ATPG, logic simulation and manufacturing test all employ scan test patterns, these ASIC development steps each require a different form of the test data, because each views the same data differently. In addition, simulation and manufacturing test need supplemental test information beyond that required by ATPG to implement test patterns in their own environments.

ATPG tools provide test patterns as a set of logic states—a form convenient for fault analysis but not directly usable by simulation or manufacturing test. Since scan ATPG typically treats all scan cells as primary inputs and outputs, ATPG tools don't need to provide information about how to get the scan data into or out of the scan chain. The tools need only create a table of ones and zeros, with the columns representing specific scan cells and the rows representing individual scan patterns.

Logic simulators, on the other hand, need to simulate the shifting of data into and out of the scan cells to verify scan chain functionality. To shift data in and out of the scan chain, you need both the scan chain topology and the protocol. Obtained from the schematic or layout, the scan topology defines scan chain shift order and inversions—when the inverted output of one scan cell drives the input of the next cell in the chain. To simulate the scan chain operation, topology-ordered test patterns and the corresponding scan protocol must be written in the event-based force statements of a specific simulator. In a similar manner, ATE must have the topology and protocol information to load and unload the logic states of the scan chain through the scan I/O pins. A manufacturing test needs the scan data in a form executable by a specific tester on a physical device.

Three views of scan data



Transforming scan data

Using internal scan to automate the test development process requires more than simply running ATPG. To verify the scan test logic and ultimately test actual ASICs, the development team must transform and augment ATPG test patterns. If the team uses programs that accurately transform the scan data at each step, designers can rest assured that their DFT efforts will contribute to shorter time-to-market.

Third parties provide such programs. TSSI, for instance, provides a neutral test database where all scan test data can be stored and accessed by all of the major ATPG tools, simulators and ATE testers.

Frank Binnendyk, director of marketing, TSSI, Beaverton, OR

High fault coverage isn't enough

When evaluating test solutions, aim for more than just the highest fault coverage. A test solution must also ensure minimal impact on the area and speed of a design, along with minimal impact on the ASIC design cycle .

Scan is an effective test method for addressing high fault coverage, but it incurs area, speed and schedule costs in an ASIC design. When evaluating a scan solution (full or partial), you're faced with minimizing the cost to your designs while maximizing fault coverage. You can typically measure the cost of scan by answering these questions.

- Performance impact: Can I afford any performance impact on my design for test? If so, where?
- Area impact: What die size am I targeting?
- Schedule impact: What's the right level of scan for my design? Can I afford several iterations to get the right number of scan elements?
- Fault coverage: What's my fault coverage goal?

Test cost management important

Traditional approaches to scan test solutions have focused on providing automatic test pattern generation (ATPG) that will produce high-fault-coverage test patterns. But this is only relevant once a testable design has been created. ATPG tools do nothing to address the issue of how to create a testable design—and it's this step where the primary cost management of scan is done. Scan is a cost-effective solution for ASICs only when additional tools are used that minimize impact on area and performance and ensure predictable results (to minimize schedule impact).

Constraint-driven test synthesis combines test, synthesis and timing analysis to address all dimensions of the test challenge: cost management and high-fault coverage. This type of test solution, based on full- or partial-scan methodology, addresses the challenge by automating scan architecture selection (which registers to scan), implementation for minimal design impact (how to put in scan) and DFT (how to ensure predictable results), as well as providing ATPG for generating high-fault-coverage test patterns.

Constraint-based scan selection automatically generates the optimal scan architecture for a design based on area, performance and testability, and eliminates the need to manually do time-consuming scan selection. It also combines structural testability analysis of a design with timing and area analysis. Based on these analyses, it selects sequential design elements to scan for optimal fault coverage results with minimal area and performance impacts, so you don't have to determine the right percentage of registers to scan for optimal results. Percentage of registers scanned means little to an ASIC designer; with constraint-driven test synthesis, you provide only the parameters which have meaning to you—performance, area and target fault coverage.

Integrated timing analysis is key

A key element of constraint-based scan selection is integrated timing analysis. Only when timing analysis is done during scan selection can you be assured that performance goals are met with the optimal scan architecture in place. Replacing a register by a scan version can affect set-up and intrinsic times and can change the input load and output drive, which affects net transition times. All these factors must be taken into account to accurately assess the performance impact of introducing scan into a design. By leveraging timing analysis, constraint-driven test synthesis can automatically select the scan architecture to ensure that no critical paths are affected. The critical path would then remain the same for the scan version of the design as for the non-scan version.

Constraint-driven test synthesis combines constraint-based scan selection with other DFT technologies—such as redundancy removal, testability rule checking and feedback and optimization of a design within the context of test to ensure predictable results. With these capabilities you expose and resolve testability problems early in the design cycle, ensuring the creation of a highly testable design so that there are no "testability surprises" at the back end of the design cycle.

Finally, constraint-based test synthesis provides ATPG, which is key to generating high-fault-coverage test patterns once a highly testable design has been created. Combinational ATPG is used for full-scan, and sequential ATPG for partial-scan designs.

Sequential ATPG is necessary with a partially scanned design since the circuit no longer appears as a simple combinational arrangement. Sequential ATPG generates sequences of patterns to establish known states for all of the sequential elements in a design (including those that aren't scanned) and generates high-fault-coverage test patterns. Sequential ATPG will take longer to run than combinational ATPG.

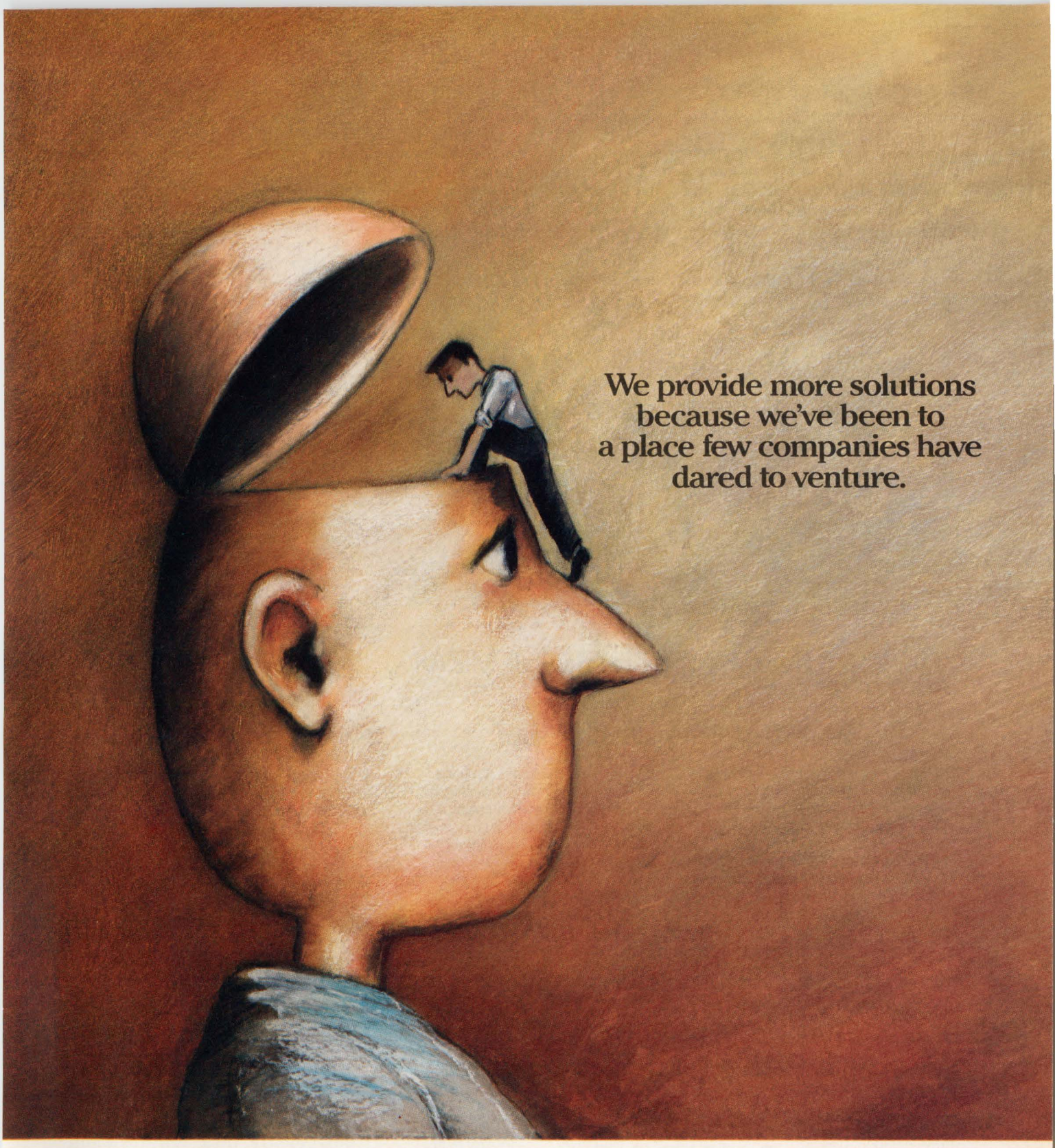
Synopsys has developed constraint-driven test synthesis in its Test Compiler product family to provide predictable, high-fault-coverage results with minimal design impact. By integrating testability, synthesis and timing analysis, Synopsys provides designers with a cost-effective solution for implementing scan in ASICs.

Kelly Gomes, product marketing manager, Synopsys, Mountain View, CA

addition to stuck-at faults. There's a whole class of faults that simple scan tests don't cover." With the design of Parkin's chip 80 percent complete, first-pass fault coverage was 85 percent. The minimum fault coverage he's looking for is 95 percent.

To get higher fault coverage, Parkin says he'll use ExperTest's new Synthesized Test Enhancement Program (Step), available now as part of the ExperTest integrated test generation and fault simulation environment. With Step, the ATPG engine of TDX can pinpoint the cause of any problems it's having. Step can then synthesize a small number of enhancements into the circuit netlist, so that TDX can run more efficiently. In the worst case, TDX can resort to partial scan to increase fault coverage of an ASIC.

Like Sun's Parkin, TDX user Chris van Staden, design engineer at Scientific Atlanta (Atlanta, GA), put very little effort into an up-front design-for-testability strategy. "I'm designing for functionality more than doing an up-front analysis for testability," he says.



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Intended for satellite receivers and cable descramblers, the television video product van Staden's designing—especially the error correction and encryption portion he's responsible for—requires a lot of vectors. "Scan vectors are really expensive, especially with counters," he warns. A VHDL and Synopsys synthesis user, van Staden admits he's not currently leveraging his use of synthesis for testability.

Mark Mallory, team leader of test technology at Kodak (Rochester, NY), sees an advantage to linking his use of Synopsys synthesis to his testability strategy. He says, however, that the link would have to be made during the original synthesis step for him to switch from his present methodology. "Test Compiler does test analysis and scan insertion after logic synthesis," he states. "It doesn't put behavioral-level knowledge of the circuit to work for testability purposes. I'd like to put test enhancements right into the VHDL code and run the testability rules checker during the original synthesis step. Otherwise, if you violate a design rule, you have to go back and change your code."

Since Mallory switched from manually generating vectors two years ago, he's been using Racal-Redac's (Mahwah, NJ) Intelligen sequential ATPG tool and Cadat for logic and fault simulation on cell-based digital ASICs that average about 20,000 gates in density and include RAMs and FIFOs. In the future, Mallory says he'll be evaluating and benchmarking tools.

Asked whether he's looked at Racal-Redac's Silc RTS (register transfer scan) test synthesis/ATPG tool, which incorporates the sequential ATPG engine of Intelligen, Mallory states, "With synthesis tools, the overriding factor is ASIC vendor support."

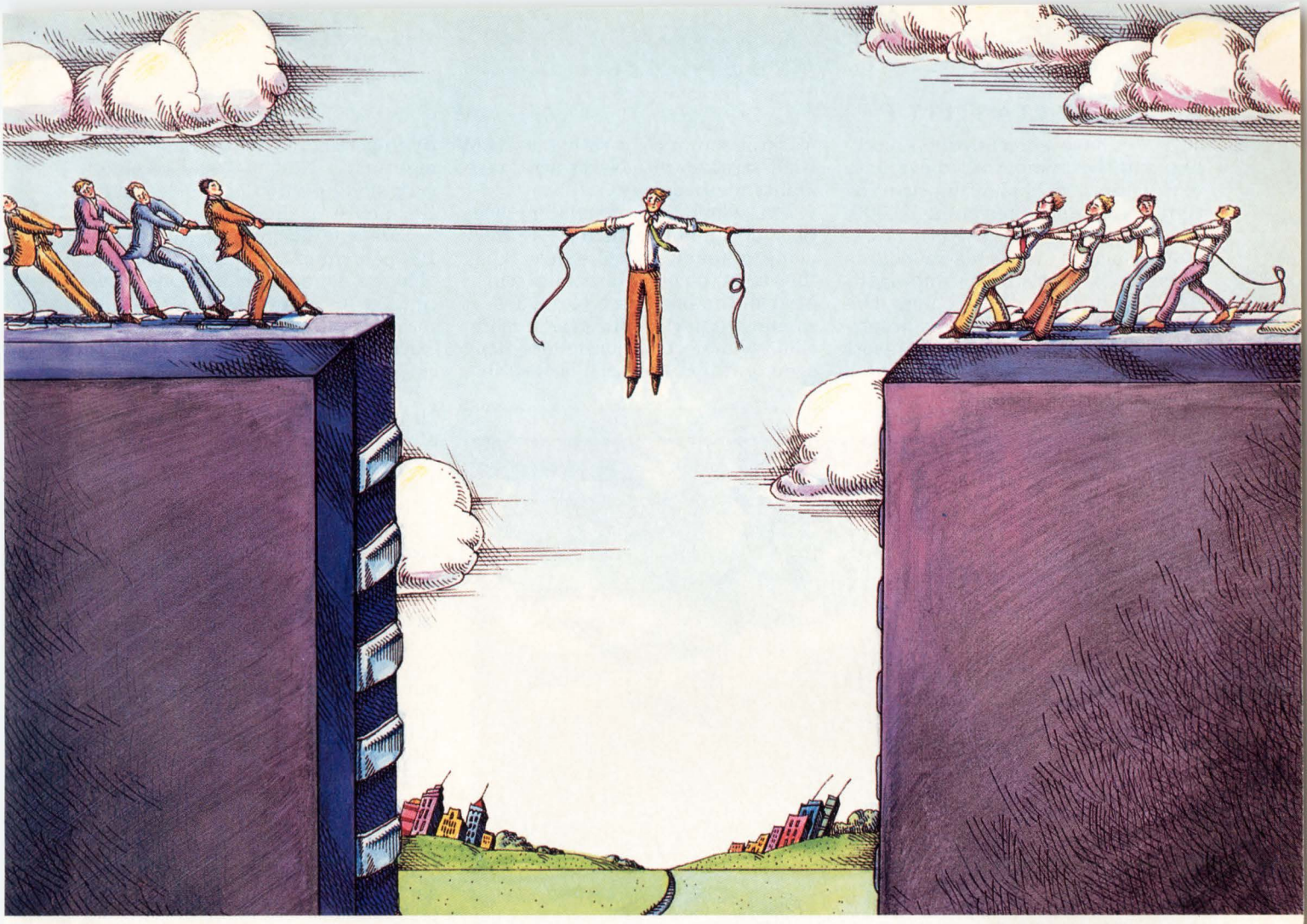
Silc RTS test synthesis/ATPG is linked to Racal-Redac's SilcSyn II synthesis, renamed Silc VHDL. With Silc VHDL, automatic RTS test synthesis happens as part of the architectural synthesis step, with ATPG occurring after the logic synthesis step. Racal-Redac is looking at year's end for the first customer shipments of Silc RTS, which accommodates full, partial and JTAG boundary scan.

Like Mallory, test engineering specialist Andy Halliday, who works at the Texas Instruments (Dallas, TX) Defense Electronics Group, is using Intelligen as a stand-alone sequential ATPG tool for ASICs that vary in density from 5,000 to 100,000 gates. "I'm using all different pieces," he says, "but it's getting me by right now. I'm anxious to evaluate test synthesis, though."

Halliday is up against DOD requirements that are getting tougher and tougher with regard to VHDL. "The DOD has this idea you can have synthesizable VHDL," he adds. "They want us to put the test requirements into synthesizable VHDL code." Halliday says there have been big strides in test synthesis in the last year, "but I want to play with it first, and see if it does what the vendors say it does."

Look for links to floorplanner

Hardware engineer Sanjay Bajaj at Next Computer (Redwood City, CA) is evaluating the newer tools, but, he



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says, "we have a process that's working, and the manpower to evaluate tools is limited." Following scan design rules, Bajaj is designing 20,000- to 100,000-plus-gate ASICs for Next motherboards and plug-in boards using Motorola's H4C and HDC ASIC families. Bajaj uses the Mustang ATPG tool, and a proprietary tool, to automatically insert JTAG boundary scan. He's also working on incorporating a RAM BIST strategy into Next's ASIC testability methodology.

The switch from manual methods to a design-for-testability strategy using automated tools, says Bajaj, "has been the biggest cultural win at Next in the last three years. Test is so much a part of our design methodology now that designers don't even question the need for testability. Inserting JTAG by hand was a nightmare. Now test has become a very small portion of our design cycle, almost negligible."

Target fault coverage at Next is 100 percent of non-redundant logic. "There's not a single node where we can say it's okay if there's an undetected fault. We end up getting closer and closer to our target," claims Bajaj.

Scan overhead, he adds, is about 10 percent of used gates (8 percent of silicon area), not including JTAG. To implement JTAG in Motorola's 1-µm technology, which offered no cells for JTAG, it took 5,000 gates in a 200-pin gate array. "But now," relates Bajaj, "with its 0.8-µm technology, Motorola provides JTAG built into pads, and it takes another 700 or 800 gates for the controller logic."

Advice from Bajaj concerning the significance of a link to a floorplanning tool echoes that of other users implementing scan. "We can't afford to have a single scan chain," he says. "Most are split, with maybe 16 scan chains on a chip—16 lines through a rectangular piece of silicon." Next designers rely on a proprietary floorplanner for such designs.

Be sure to follow testability tools as they evolve. As a pioneer of the test synthesis technology, Synopsys will get some bum raps, just as Xilinx has in the FPGA arena. For a true picture, you have to look beyond all that—to an installed base of 200 and the support of a dozen ASIC vendors. Then evaluate and benchmark the software yourself. ■

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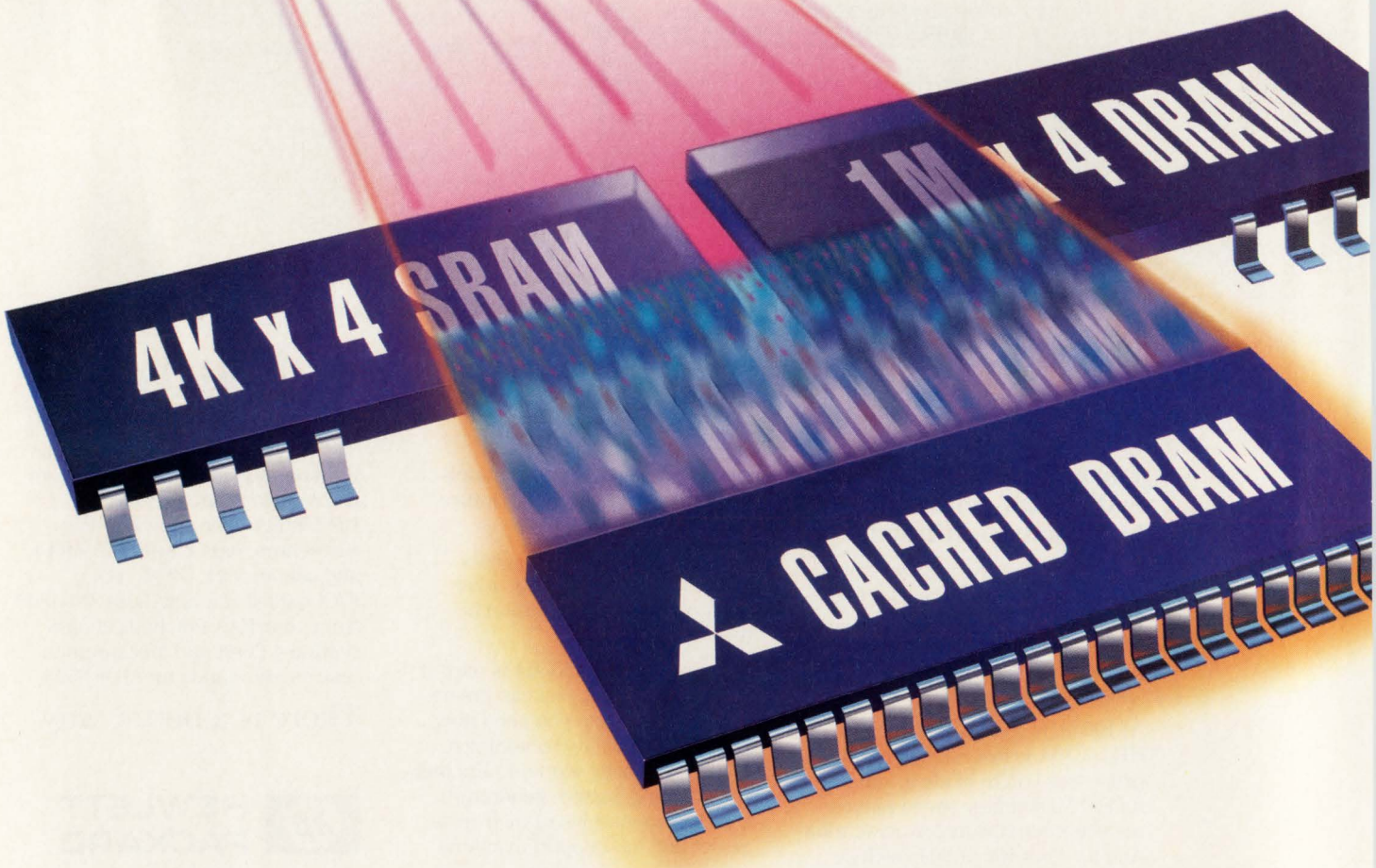

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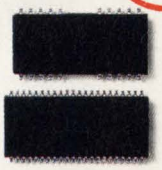

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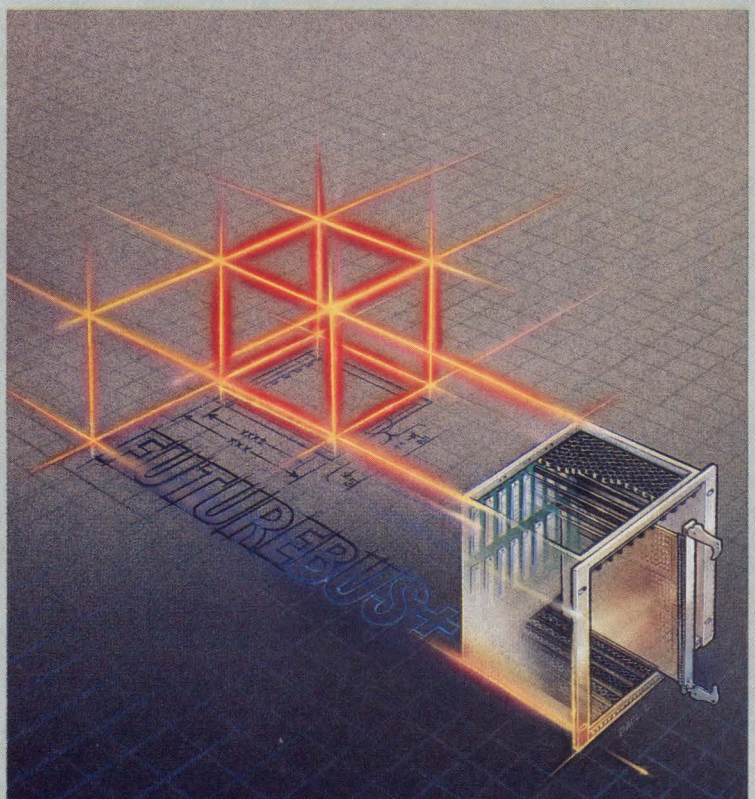

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Silicon, tools and specs join to drive Futurebus+ growth

The first Futurebus+ systems are now emerging, but introductions are lagging far behind expectations. The bandwagon is rolling, however, and the players are jumping on.

Warren Andrews, Senior Editor

CCT is one of three prime contractors for the U.S. Navy's Futurebus+ system. Pictured are some of the components the company developed as part of its contract, including an i860-based processing board (upper right), a 68030 CPU (upper left) and a Safenet II network controller (bottom).

The Futurebus+ specification—at least the logical layer and the first three profiles—has been complete for almost a year. Yet systems based on the approach are hard to find. Even more scarce are Futurebus+ boards from conventional board-level suppliers. But this picture is likely to change as the necessary pieces start falling into place.

First, National Semiconductor (Santa Clara, CA), Philips/Signetics (Sunnyvale, CA) and Texas Instruments (TI—Dallas, TX) have improved the performance of their transceiver chips and will be showing real protocol controller silicon later this month. (Philips/Signetics has already introduced one member of its controller family.) Second, system makers are beginning to develop system hardware and software and have begun to look for third-party vendors to supply I/O and other boards. Third, vendors who've been struggling with Futurebus+ designs are starting to learn the value of extensive computer modeling before building prototypes. The first generation of boards from these vendors should be out of the lab by year-end. And finally, tools for testing and debugging are emerging that offer interfaces to both general-purpose logic analyzers and protocol-specific devices.

In addition, two profiles—M for military and T for telecom—are in the final stages of specification, with completed documents expected by the end of the year. Both are dependent on high-availability technology, including fault tolerance and live insertion. It's expected that these profiles will have a significant impact on the future demand for Futurebus+ systems.

But the area with perhaps the greatest potential, the desktop version (Profile D), is still undergoing revision and probably won't see daylight until late in 1993. When it surfaces, it won't be recognizable as one of the standard Futurebus+ profiles. Instead, Profile D will look like a mezzanine card, foregoing the classic BTL transceivers and full Futurebus+ interface.

Although much activity is expected to take place over the next several months, there are likely to be some major shortfalls in the availability of key components—starting with silicon—for complete Futurebus+ systems. Features such as full cache coherency and packet mode, for example, may

well have to rely on proprietary ASIC or discrete silicon solutions—or they may simply have to wait for the next generation of controllers, perhaps a year off.

First system is military

"One of the key elements needed for Futurebus+ to become a reality is some level of highly integrated protocol controller," says Bruce Kimble, product line manager for Futurebus+ for Cable and Computer Technology (CCT—Anaheim, CA). Although CCT is the first Futurebus+ maker to deliver a system with all the features of Profile A—including cache coherency—it's been at the expense of significant board space and a lot of discrete logic.

CCT delivered its first system, complete with a 68030-based CPU board, to the U.S. Navy earlier this year. One of three proof-of-concept projects, it was the first such system with cache coherency to be demonstrated to the Navy, and accepted. The other two contracts were let to Raytheon (Marlborough, MA) and Litton (Pascagoula, MS) respectively; only Raytheon has submitted its system for approval.

The Litton project, which includes Force Computers (Campbell, CA) as a major subcontractor, has been stalled for many reasons, one of them being that Force has been unable to get its protocol controller silicon ready. "We expect to receive first silicon of the protocol controller no later than September," says Force's director of strategic marketing, Wayne Fischer, "and it will probably take about four or five months to wring out the chips and board." Force's Futurebus+ CPU board is based on the Intel 80486 processor.

Raytheon, working with BICC Vero, was the first to incorporate VME and Futurebus+ in the same chassis. Pictured is a Raytheon system which was developed as part of the Navy's NGCR (Next-Generation Computing Resources) program. Raytheon was the first to deliver a partially completed system for evaluation in the Navy's program.

The interface silicon is supposed to be a joint development between Force and Texas Instruments. Its delivery has been delayed many times, but now TI claims it's ready. It has reportedly been so thoroughly simulated that first silicon is expected to work without problems.

Slow silicon

Despite the feverish activity by semiconductor makers, Futurebus+ silicon has been slow to emerge. Signetics was first out of the chute with its FB2000 family of Futurebus+ chips. A protocol controller is now available, with an arbitration device and a datapath chip on the way. In addition, the company offers a complete family of BTL transceivers.

National Semiconductor, the inventor of BTL, has also had a family of BTL transceivers available for some time, releasing its first performance upgrade early this year. The company will debut a protocol controller this month. Similarly, TI has been readying a controller, and like National, the company plans to reveal it to the world this month.

This generation of protocol controller chips, however, doesn't have all the bells and whistles the Futurebus+ specification calls for, particularly for profiles A and F. The Signetics and TI devices include some of the enhancements of the full Profile A specification, but lack the critical cache-coherency circuitry. The National device, jointly developed and marketed by National and Newbridge Microsystems (Kanata, Ontario), also lacks cache-coherency circuitry. It's been designed to support the Futurebus+ Profile B, although it includes some hooks for the A and F profiles as well.

Christopher Koehle, of National's Futurebus+ product marketing group comments, "National's controller focuses on the B profile, primarily an I/O profile, because we believe that most of the activity in the near future will revolve around this profile." National's controller supports only the compelled or handshake transfer mode, as the company awaits solidification of the packet-mode specification.

Koehle also reports that many new BTL designs still aren't based on the Futurebus+ specification. "In some cases," he says, "these are totally proprietary systems, while in other cases designers are looking to get experience with the BTL technology and will probably switch over to Futurebus+ once the interface silicon is available."

System designs ramping up

Protocol controllers may be scarce, but some Futurebus+ systems are debuting. Apart from those connected to the Navy's Next-Generation Computing Resources (NGCR) project, Oki Electric (Tokyo, Japan) has announced a server based on Futurebus+. Digital Equipment Corporation (Maynard, MA) has also said it's releasing a server, as well as an advanced workstation based on its new Alpha microprocessor architecture.

Thus far, neither company has shipped these systems in volume,

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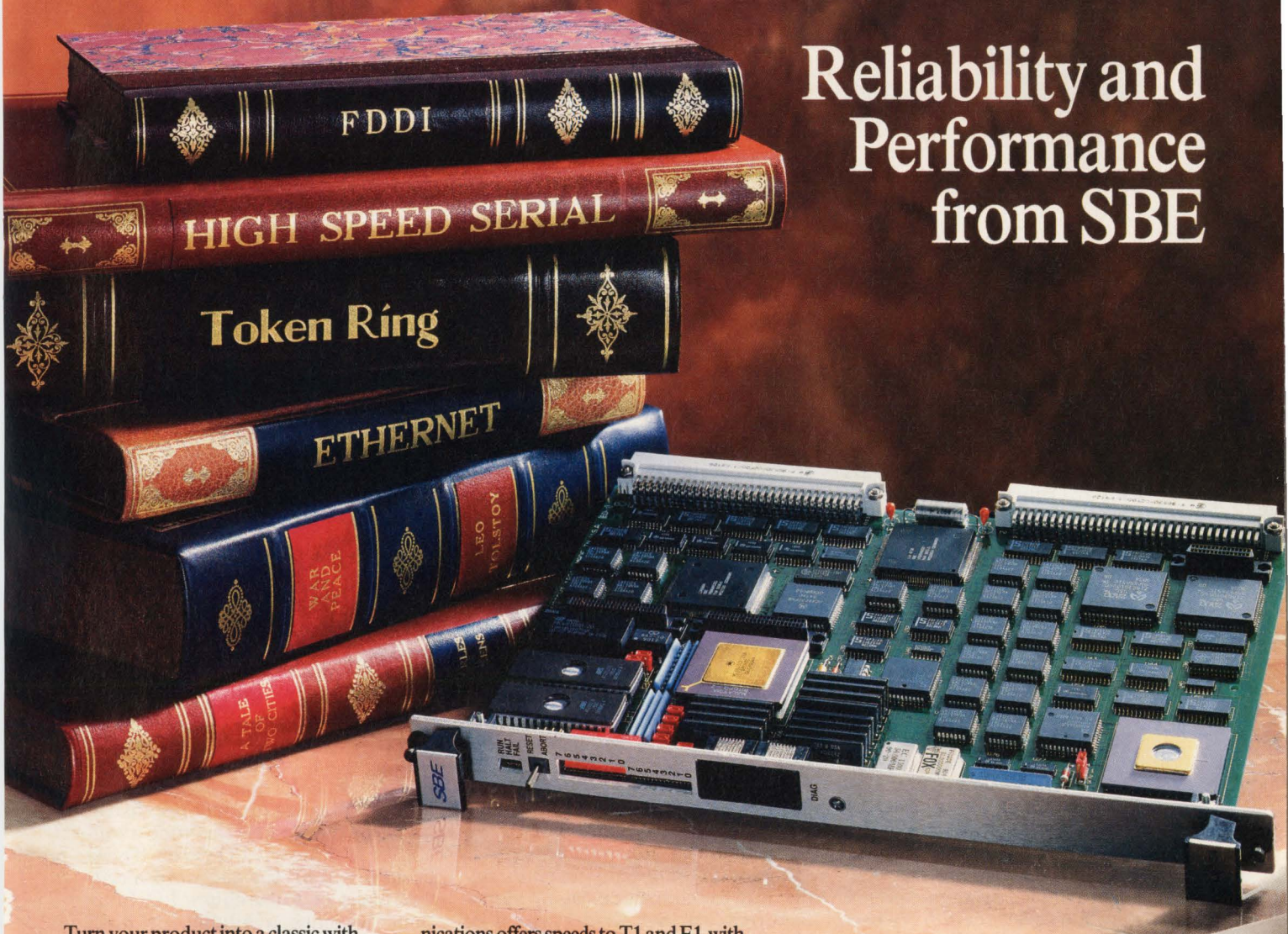

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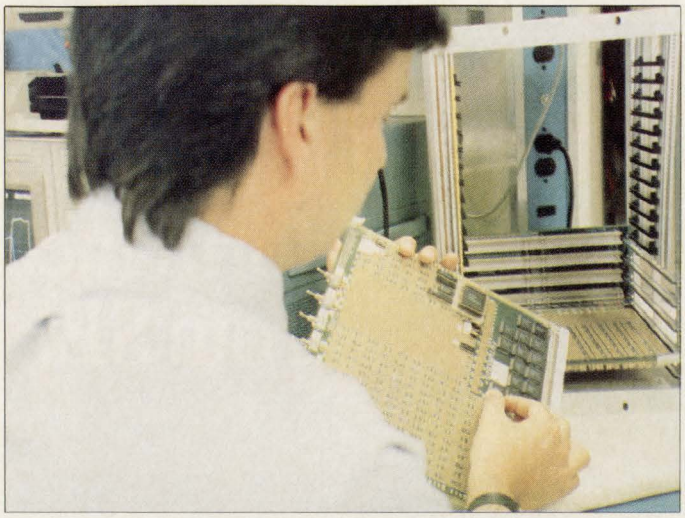


National Semiconductor's Chris Koehle believes in the future of Futurebus+. "We're just starting to see more BTL transceiver parts going into Futurebus+ than proprietary systems. And when the interface silicon emerges, we expect to see a major step up in activity."

and it may be a few months before they're available on a broad commercial basis. But, industry sources report that Digital is actively seeking sources for a Futurebus+-to-VME bridge, as well as other Futurebus+ modules.

Digital's I/O marketing manager, Stephen Justus, says that the company expects to start shipping Futurebus+ systems based on its Alpha processor before year-end, adding, "We hope to have a full-scale prototype up and running later this month [at Buscon]."

It's potentially Digital that many smaller Futurebus+ board makers are setting their sights on. Conversely, Justus says Digital is counting on third-party board makers to supply many of the I/O functions that will be required by the company's Futurebus+ systems.

To date, however, there have been precious few Futurebus+ boards to try in systems. Digital recently sampled two of the commercially available boards in its Alpha-based systems; the company was pleased to report that it was able to get at least one of them up and running with little or no difficulty. The board that passed this test was from CCT, the first reported instance of boards from different vendors—and designed for different systems—operating in the same Futurebus+ backplane.

"The fact that early in the life of the Futurebus+ specification, boards from two different systems and two different vendors were able to work together," says CCT's Kimble, "prophesies well for future developments. That Futurebus+ cards can actually plug and play at this early stage is encouraging. This may help avoid the painful experience of VME vendors during the early years, where nothing worked together." And while this is strong testimony in favor of the board and system, the result also bodes well for the specification itself, since neither board was based on standard interface silicon.

"Digital will be the market maker," says Kimble, "creating in the short term most of the Futurebus+ slots with its Alpha-based Futurebus+ workstation." He adds that, clearly, some kind of VME-to-Futurebus+ bridge will be an early key to success, since it will take time for potential Futurebus+ vendors to ramp up.

Digital's Justus reports much activity among potential third-party board makers; in fact, he's counted 13 or so different board designs currently under way from almost as many manufacturers. Further, there's been a lot of interest in the company's TRI-ADD program, which helps designers get up to speed on Digital-compatible modules.

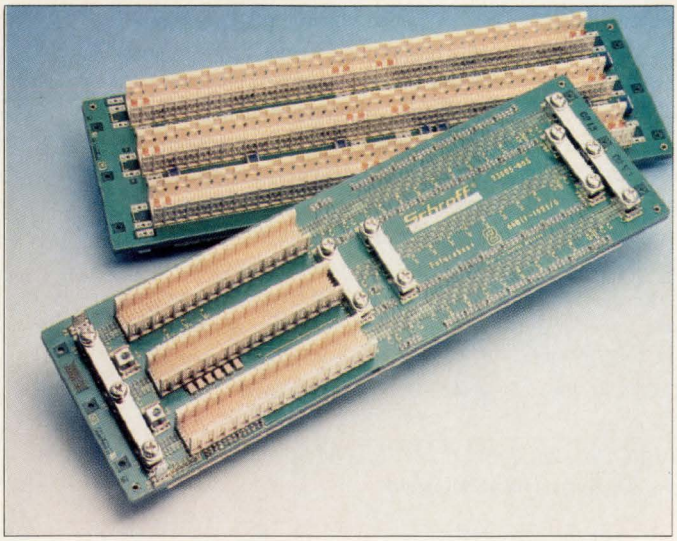
"For 1993," says Justus, "we expect to see a substantial number of products that can take advantage of the high-performance server technology Digital will be offering." He anticipates that a wide array of different devices will become available in high-speed communications and networking areas such as HiPPI, FDDI and Fiber Channel.

Following on the heels of conventional workstation I/O, according to Kimble, will be networking and telecommunications I/O. Even before the telecom profile is defined, there will be a need for boards and systems that can serve as bridges and routers capable of handling T1 and T3 data rates. "It makes a lot of sense," Kimble continues, "for Futurebus+ to be used in many of the high-rate, serial-stream systems where multiple data streams can be included on a single card."

Bridges to Futurebus+

It appears, then, that some of the early Futurebus+ board offerings will be bridges from other buses. A number of companies are already working on Futurebus+-to-VME bridges, and Digital has reportedly contracted a third party to develop aVME/Futurebus+ bridge for its Alpha-based Futurebus+ workstation. VME is the most logical choice for a first bridge product because of its performance and the wide availability of different I/O cards. These bridges will fill the gap until a critical mass of Futurebus+ I/O functions becomes available, or until other solutions are developed.

Certainly, for medium- and low-

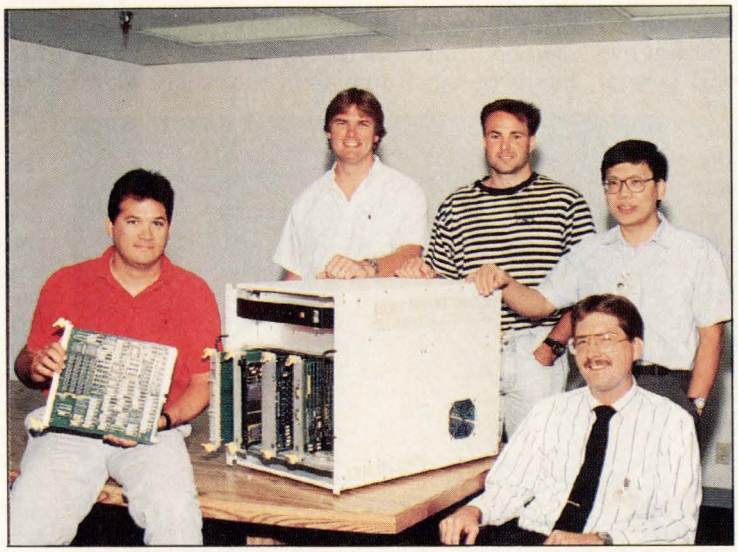


Futurebus+ backplanes using the Metral 2-mm connector are now available from a number of sources. The advantage of the modular connector is that it can accept optical modules as well as electrical connections for fiber-optic communications schemes or networks. (Picture courtesy of Schroff)

performance I/O, the use of a full-sized Profile A, B or F module would be prohibitively expensive. The cost of the transceivers, interface IC and printed-circuit board alone—not to mention the extra Futurebus+ slot—would dwarf the expense of comparable basic I/O functions such as are provided by Ethernet or SCSI.

Despite the availability of a broad range of VME I/O boards, board developers feel strongly that some interface to a workstation bus such as SBus or Turbochannel will be needed. Turbochannel is the most obvious initial choice, since it's a Digital-developed standard and Digital will be an early leader in Futurebus+ systems. Digital is looking to double the speed of Turbochannel, from 100 to 200 Mbits/s, to handle the requirements of Futurebus+-based workstations.

Although many third-party developers believe a Turbochannel-to-Futurebus+ bridge will be a significant factor in the development of Futurebus+—especially early in the game—Digital's Justus was cautious about commenting on anything beyond the VME bridge. He did indicate, however, that the Turbochannel approach was being evaluated.



CCT is one of the early leaders in Futurebus+ technology, having fully completed its system for the Navy and developed the first Futurebus+ board that worked right off the bat in a Digital Equipment Corporation Alpha workstation. CCT's team of engineers plans to bring out an entire family of Futurebus+ boards over the next several months, beginning with a VME-to-Futurebus+ bridge, local- and wide-area networking products and telecommunications boards. Pictured is the Futurebus+ engineering development team (left to right): Erasmo Brenes, Tim Lipsky, Ivo Rusich, Jeffrey Chen, and John Eden.

Digital is highly visible in the Futurebus+ camp and the company's approach is focused, but the view of the technology's future that's emerging is still somewhat confused. "Usually we get an early look at how system demand will emerge," says Michael Thompson, technical manager at Schroff (Warwick, RI). Schroff, along with BICC Vero, Hybricon, Mupac, and a few others, is among the leading manufacturers of Futurebus+ backplanes and card cages. Orders for these items usually give a strong indication of how future business will ramp up. Based on this fact, says Thompson, there's just not much going on now outside a few of the larger companies.

"The big companies, such as Digital and many of the others currently designing Futurebus+ systems, tend to make their own backplanes and card cages, so we really don't have a solid feeling for what's going on in the market," he adds. "While they may purchase a few units from us for prototyping, we really don't have any hint of what their production forecasts are."

With what he can see, Thompson views the Futurebus+ timetable as moving right in line with what he anticipated—which is a lot slower than what was forecast by many analysts and Futurebus+ advocates. "Futurebus+ is going to take a while to reach any kind of volume," he says. "Just as it took a long time for VME to mature, Futurebus+ isn't going to make it overnight. Futurebus+ is difficult to design around, and development times tend to be a lot longer than VME. There's a big learning curve to get over, and a huge mass of knowledge is needed to design Futurebus+ boards. A lot of people have to get educated, and that education has to take time. Futurebus+ is a lot more complicated than VME, and that complexity is reflected in the design time."

Still other delays have bogged down potential developers. "With Futurebus+," says Force's Fischer, "it's almost imperative to completely model a board on a computer before attempting to make a prototype." By contrast, more traditional design approaches, such as those used in VME, let you put together a prototype and debut the board in hardware. "With Futurebus+," continues Fischer, "it's not that easy. Some designers have painfully discovered that about the only way to fully develop a Futurebus+ card is to model and simulate it thoroughly before touching a prototype."

"In addition," says Ray Alderman, technical director of VITA (VME/Futurebus+ International Trade Association), "there have been delays in getting the standard printed and circulated to developers, which have resulted in designs lagging expectations. It took eight months from the final approval of the specification until it was in final form, printed and readily available."

Still other delays in getting Futurebus+ product out the door have revolved around the silicon. "Semiconductor makers are going through revisions to get Futurebus+ chips where they want them with respect to performance," states Digital's Justus. He points out that it's been difficult to figure out what to include on an interface chip and what cost-to-functionality ratio is optimum. "Profile B tends to be less expensive and less complex to design," he says, leading to the expectation that the fastest ramp-up will be for that profile. Justus is echoed by National's Koehle, who comments that he sees the largest opportunity in Profile B, but he adds that "when the demand shifts over to one of the more complex profiles, National will have interface silicon ready."

M for military

While developers are just getting started on the existing profiles, the Futurebus+ Committee is aggressively working on additional profiles that will swell the Futurebus+ flock.

Chief among the emerging profiles are M and T, the military and telecom profiles respectively.

"The M profile was delayed right off the bat with some connector issues," says VITA's Alderman. Originally, the 2-mm connector was planned for, and manufacturers were ready to militarize it, but in the middle of the process it was decided to opt for a blade-and-fork connector pioneered by Teradyne (Nashua, NH). This technology is used in a 396-pin connector in the SEM-E form factor, as well as in the 10-SU form factor with a 556-pin connector version. While swapping the connector isn't significant by itself, redefining the signal, power and ground pins from the initial 2-mm Futurebus+ connector to the revised blade-and-fork approach has been a time-consuming process, slowing down other parts of the profile.

"Another factor which delayed both the M and T profiles," continues Alderman, "was that fault tolerance and live insertion became such critical issues that a special task group had to be formed to address them. The task group has defined the scope of the objectives, which proved so wide-ranging, complex and lengthy that a totally separate document had to be established for fault-tolerant characteristics." Profiles M and T will then be able to point to sections of that new document to provide required performance parameters.

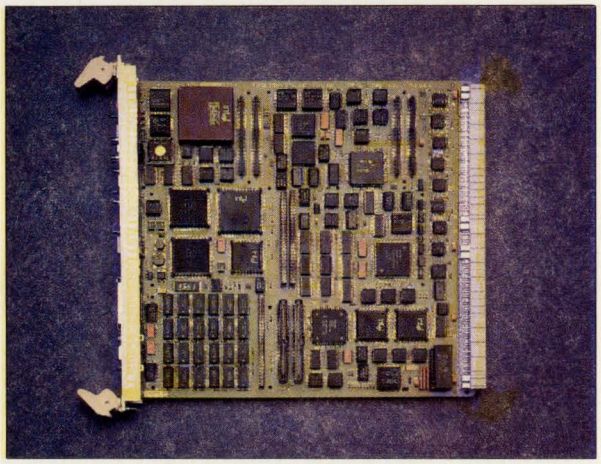
Alderman says that "these organizational issues are now behind Profile M, and the mechanical and electrical definitions are sound. All that remains is for the committee to put the finishing touches on the protocol and identify the pointers to the fault-tolerance and live-insertion document." The group anticipates that this will be done and the specification completed and sent out on an IEEE sponsor ballot by year-end.

Even though the specification for the military profile isn't yet completed, at least two DOD contracts in the works call for Futurebus+. The first is a J-Stars project using an Alpha-based implementation in a conduction-cooled, SEM-E form factor. The other contract is for a 10-SU-sized board with an R-3000-based CPU.

Both include the basic Futurebus+ specification, but on different mechanicals. The SEM-E form factor is typically for avionics use and measures about 6 in. on a side, while the 10-SU is 250 mm high and about the size of a VME card. One feature of the 10-SU system is that it provides for redundant Futurebuses for fault-tolerant applications.

T for telecom

"Profile T has experienced delays similar to those of Profile M," continues Alderman, "in that it is also dependent on the fault-tolerant specification." But since that specification has been separated from the basic profile, progress is being made. The mechanicals have been completed, using a 2-mm, Metral-type connector similar to that of the existing profiles. In addition, the pin-outs have now been defined.



Force Computer developed this 80486-based Futurebus+ CPU in its role as a subcontractor to Litton in the Navy's NGCR program. Delays in getting the interface silicon which it jointly developed with Texas Instruments have resulted in the company falling behind its delivery schedule. According to Force, the board will be up and going later this year.

Two different form factors have been defined, one calling for a 300 × 300-mm board, the other 300 mm wide by 450 mm tall. "Because the telecom industry is so heavily I/O-intensive," says Alderman, "it needs the 450-mm-tall form factor to handle the I/O lines."

The logical layer of the T profile is still undergoing some revision because of the special requirements of the telecom industry. According to Alderman, "When you have a parallel bus controlling computer resources that deal with the integration of some of the newer, high-performance technologies such as Sonet, there are some special problems." The Metral connector, for example, is modular and capable of handling optical as well as electrical connection modules. While the mechanics of these connections have all been worked out, some of the implementations and interfaces to high-speed serial inputs and outputs continue to raise questions.

In addition, much of the logical layer depends on the definition and interface level of the fault-tolerant/live-insertion specification. This is because the telecom industry is potentially the largest user of fault-tolerant computer hardware and software. "When the telephones go down," says Alderman, "people write books about it."

"In addition, the challenges to the telecom industry are dramatic. Not only does the new family of computers have to handle the traditional telecom chores, but it must also deal with brand new technology. On one side, faster communications schemes such as Sonet are needed to handle greatly increased traffic. On the other side, telecom hardware and software have to address data communications, video and even entertainment as the role of communications broadens."

On the desktop

While the telecom and military profiles push Futurebus+ technology to new levels of performance, especially in the area of fault tolerance, the desktop group is working on the leading edge of technology in yet another direction—smaller, faster, cheaper, and lower power dissipation.

At the electrical layer, members of the committee are trying to define a new transceiver technology based not on BTL, but on a version of CTL (CMOS transistor logic). This transceiver is meant to provide high-speed, ultra-low-power transmission; the minimum transfer clock speed is in the area of 250 MHz, with a goal of about 500 MHz. The ultimate object is to make the profile compatible with portable, battery-operated computers, as well as true desktop and deskside units. As was the case with BTL, all the physics of the CTL interface have yet to be worked out to accommodate transmission line and other high-fre-

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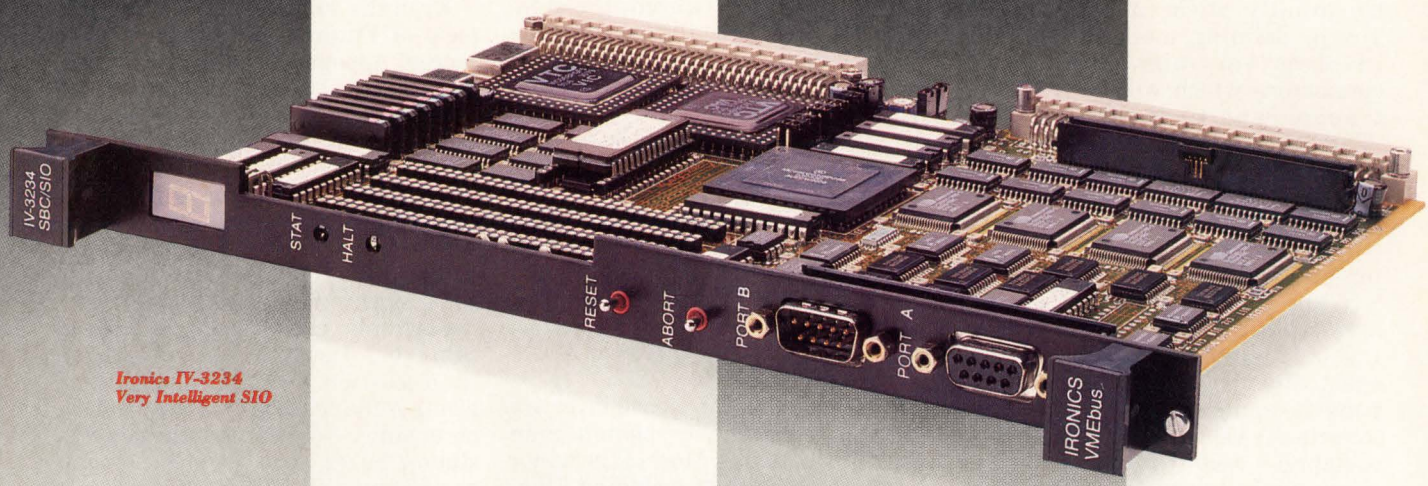

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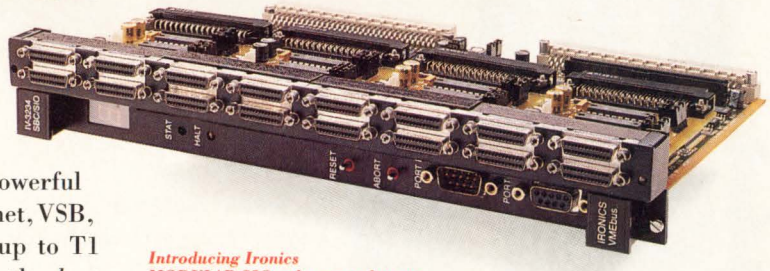

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quency effects.

Another subgroup within the Profile D Committee is working orthogonally with the transceiver group, defining mechanicals. This involves very-high-performance connectors which will be relatively transparent to the transceiver. "The connector has not yet been defined," Alderman says, "but the committee is currently accepting proposals ranging from elastomeric polymers to high-density, stackable pin-and-socket connectors."

While most committee members agree that the form factor of Profile D should be small and stackable, the exact dimensions will probably depend to some extent on the connector scheme selected. The objective is to define a card that can be used as a mezzanine card for Futurebus+ Profiles A, B, F, and others as the specifications are completed; it must also sit on a variety of different proprietary motherboards.

According to Force's Fischer, Profile D will continue to pose real challenges to the specification writers. Thus far, only the transfer rate of 100 to 250 Mtransfers/s and the bus width of 64 bits have been agreed on. But Fischer speculates that the board will probably be close to 3 × 5 in., or the post-card size of SBus and Turbochannel, with a height of only 15 mm, so extra Futurebus+ slots won't be needed when a board is added to an A, B or F card. To achieve the low power and high speed, Fischer believes the electrical characteristics of the bus will look something like RAMbus, with low voltage swings.

The logical layer

Efforts to define the logical layer are lagging even farther behind than the physical layer. Most of the major system companies, including Digital, Hewlett-Packard, IBM, Sun, Unisys, and others, have been sitting at the Profile D meetings and have brought up a number of larger philosophical issues. These range from the fundamental transfer protocol to more global issues such as what the specification should or shouldn't include.

Even the source-synchronous protocol of Futurebus+, thought to be sacred, appears to be under attack. But the 896.1 specification provides for a synchronous as well as a source-synchronous protocol. Among other things, the committee is questioning whether a tightly coupled resource such as a mezzanine bus should be synchronous or asynchronous. Or should it at least have some synchronous capability?

Certainly we're seeing shades of SBus and Turbochannel reflected in the discussion. It's being asked, in fact, whether the desktop profile is a follow-on to either—or both—of those workstation buses. And, to some extent, participants are learning what would have happened if either of those buses had been designed by committee, rather than by a single group within a single company.

The process of defining the logical layer is just beginning, and it's already apparent that Profile D won't join Profiles M and T in going out for sponsor ballot by year-end. It's been forecast that the committee might have the specification ready in 1993, but skeptics believe it will take longer for so many major systems houses to agree on enough parameters to make a specification.

Force's Fischer, on the other hand, believes committee members will be able to keep to a more rigid timetable. "Through our work on other parts of the specification," he says, "we've learned how to handle committee work, and how to establish realistic goals. Profile D will come into line once realistic goals are established."

As chairman of the committee on the Futurebus+-to-VMEbus bridge, Fischer reports that the most recent draft included many comments; most problems, however, have already been resolved. He hopes that the specification can go out for sponsor ballot later this month. (The bridge specification will become part of the VME 1014 specification rather than the Futurebus+ specification.)

Optimism still high

Despite delays in completing parts of the Futurebus+ specification, scarce silicon and slower-than-expected emergence of systems, most players within the Futurebus+ camp remain very optimistic. "We started with transfer rates around 125 Mbytes/s,

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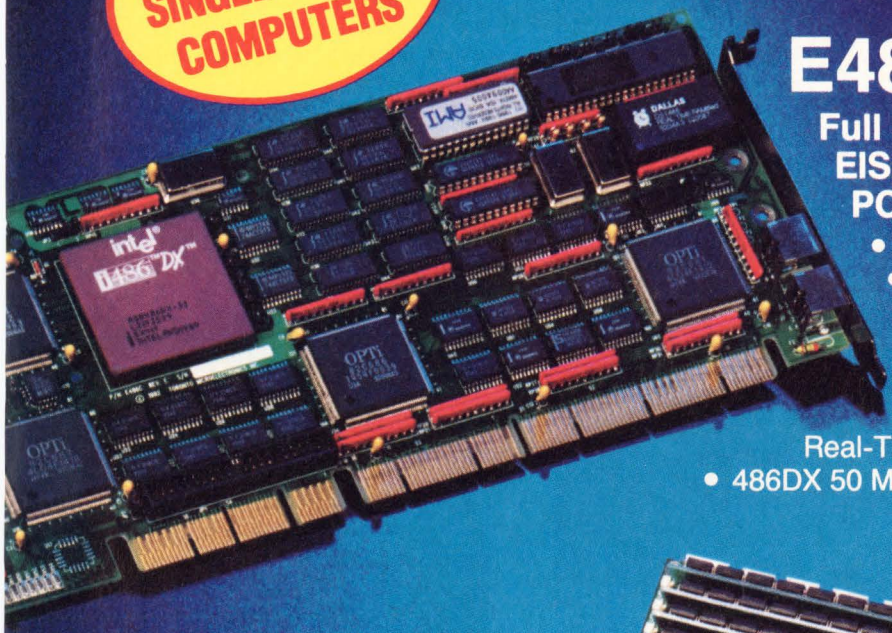

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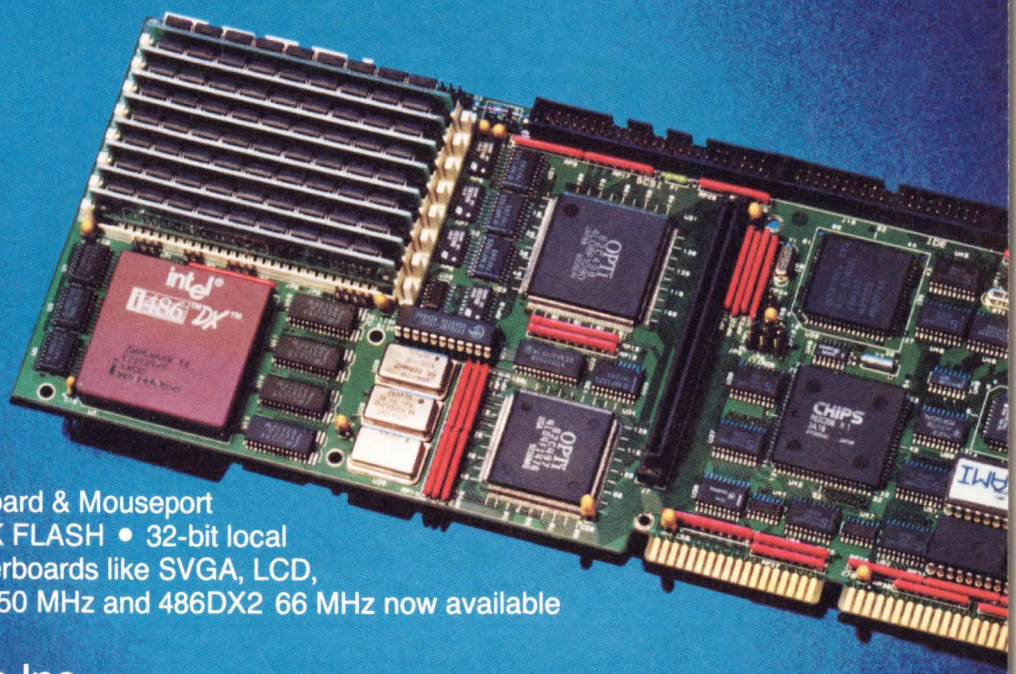

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and are now approaching 160 and still improving with each generation," says CCT's Kimble.

Kimble also thinks that other bridges, including a Futurebus+-to-Turbochannel product, will be significant over the next several years. And as Digital workstations begin to break the ice for commercial Futurebus+ systems, other companies are expected to follow rapidly, offering a broad selection of high-performance servers and parallel systems.

This marks the beginning of the Futurebus+ revolution. Where it goes will largely depend on how fast manufacturers can ramp up to provide a critical mass of available hardware—and, just as important, software. At this critical juncture, most of the initial pieces are in place, but the infrastructure still has a number of vulnerable spots. Expectations have already exceeded reality. Board makers are still treading very gently, reluctant to expend significant resources on a technology for which there is no significant demand. And extensions to VME and Multibus II continue to push those standards closer to initial Futurebus+ performance levels—and at a fraction of the price.■

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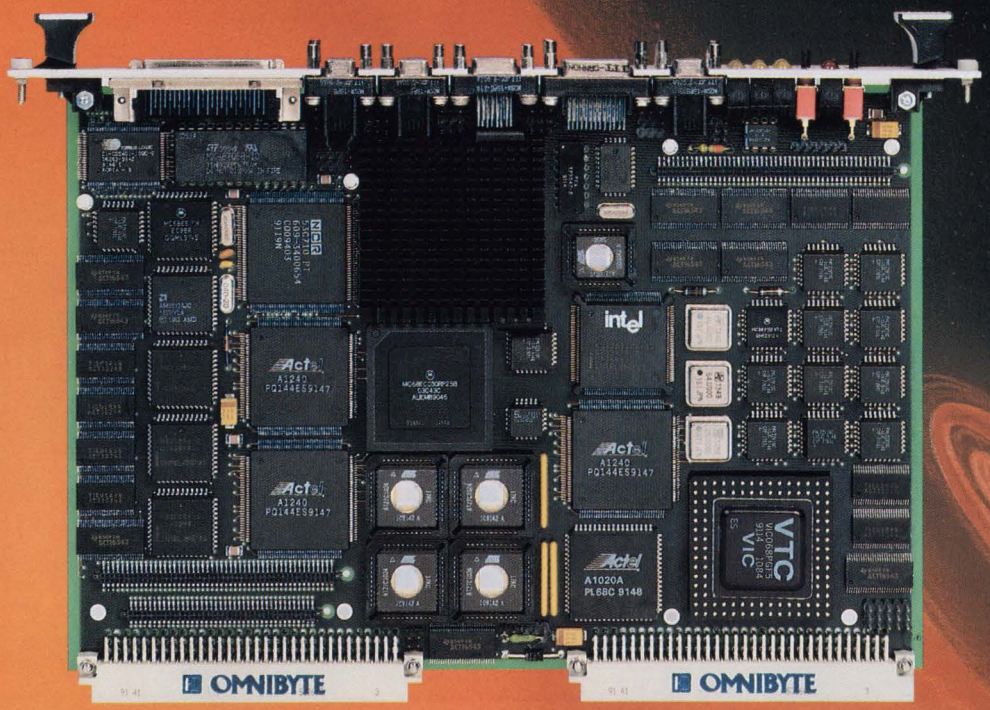

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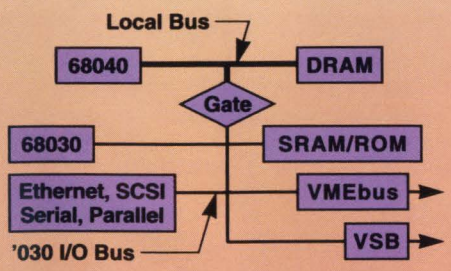

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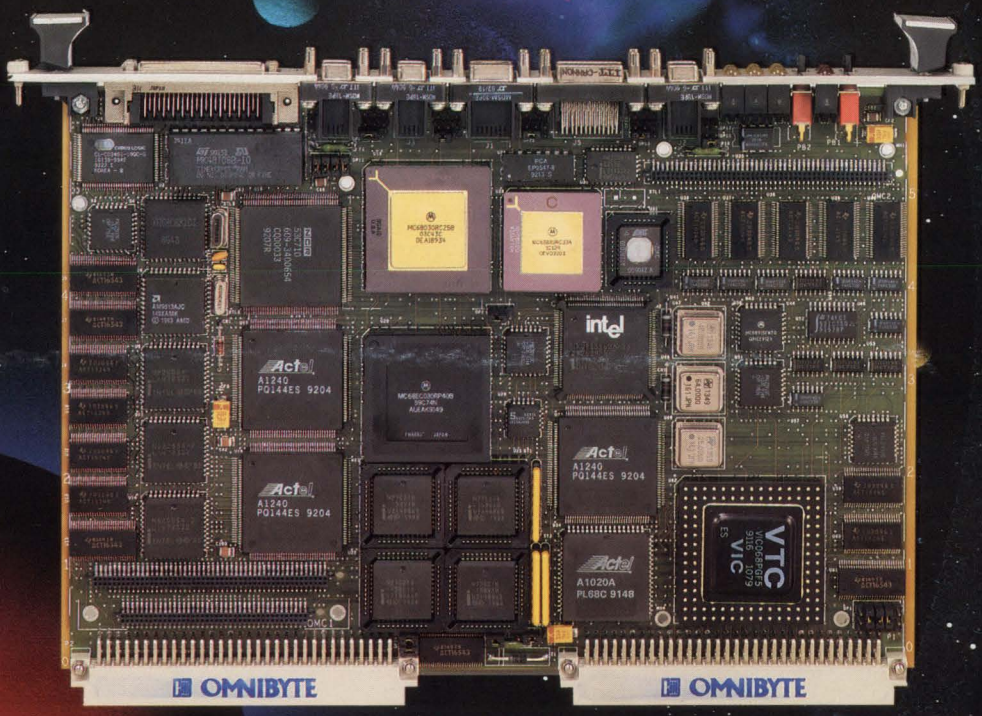

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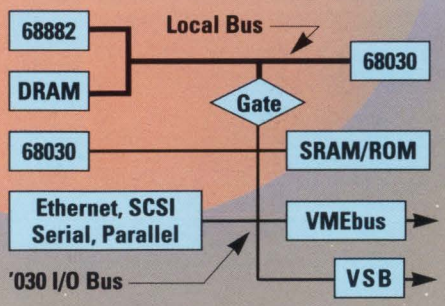

Aries Architecture

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Standard I/O	2 RS232D: 68C681 DUART, 32 Lines Parallel I/O, or 16 w/ Centronics Printer Port
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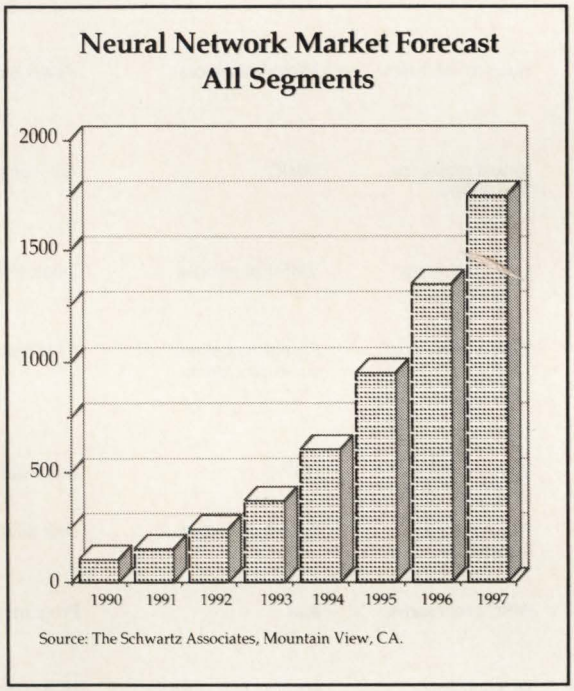

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Applications, not technology, drive embedded computers

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"Business as usual" is no longer the rallying cry of standard-bus technology at the board level. The key is finding real solutions—not just throwing more advanced technology at the problems. And major technical conferences like Buscon, the Embedded Computer Conference and Exposition (ECC) and the Embedded Systems Conference are helping engineers and engineering managers find the key.

Warren Andrews, Senior Editor

The next chapter in the history of standard-bus, board-level computers is now being written, and it covers a lot more ground than the chapter before. A number of factors are contributing to the complexity of the scenario; prominent among them are changes in the embedded-computer industry, the incredible shrinking transistor, the availability of high-performance CAD, competitive market pressures, and a general acceptance of software and hardware standards.

Traditionally, board-level products end up in embedded applications ranging from high-performance, system-level controllers to imaging and CNC or machine control. The basic idea remains the same: these computers are going into an end product that's not itself a computer.

Board-level computers based on standard buses are essentially a subset of embedded computers. The two groups aren't synonymous, but there's a growing thread of commonality, based on the fact that both

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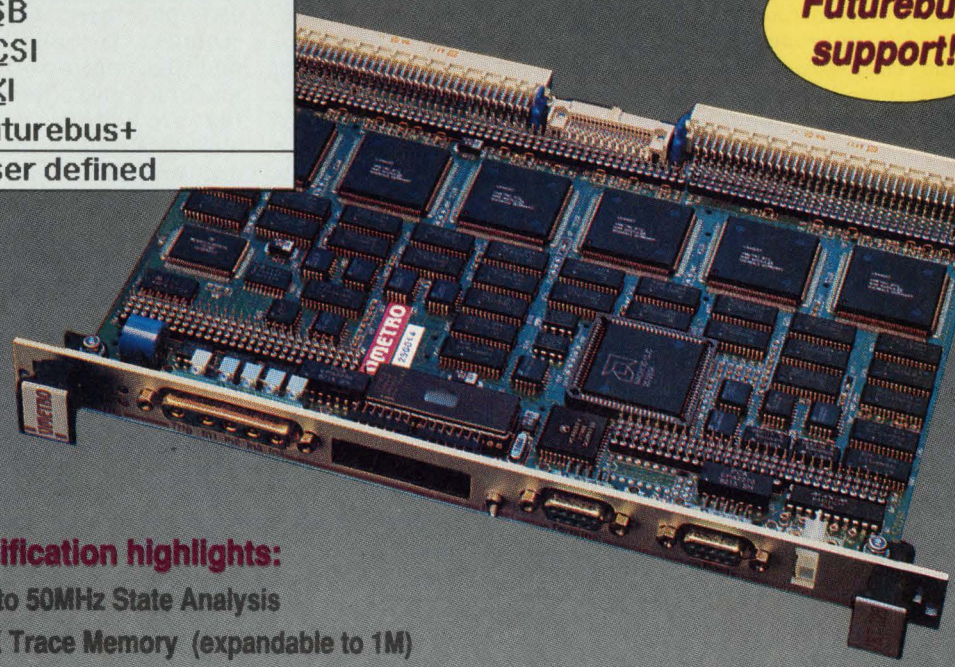

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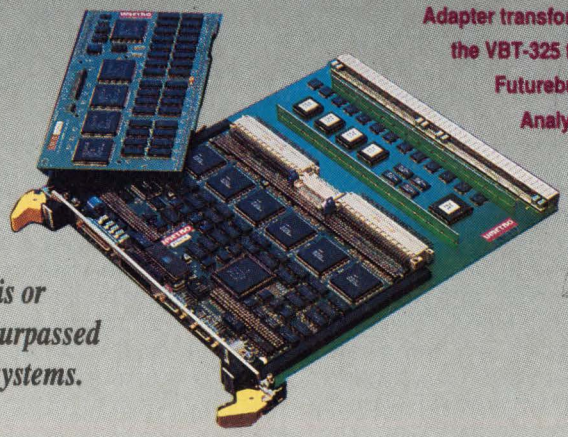

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hardware and software standards are becoming increasingly critical. On one side, all embedded solutions, from the simplest single chip to the largest embedded supercomputer, are groping for such standards. On the other, standard-bus approaches, architectures and companies are reaching out to accommodate existing and emerging embedded applications by redefining how standards are applied.

Making the situation even more dynamic, traditional embedded computer systems are themselves rapidly changing. Throughout the 1980s, embedded systems were the domain of a design-from-scratch mentality featuring in-house production. The results, often spectacular in terms of price, size and performance, incorporated highly optimized hardware and software in a custom-tailored form factor. The solutions were also notable for the development cost and time spent.

Typical of this approach are computers used in automotive applications. Starting with the CPU, all components of the automotive computer are custom-designed. Even the software is painstakingly coded in assembly, and by hand, to optimize performance and reduce memory space.

But such highly customized approaches are rapidly falling out of favor—even in the automotive industry. Standard chip and system architectures are becoming the rule, replacing custom designs. And standard operating systems are being used widely, for everything from microcontrollers to DSP. Even standard high-level languages are slowly replacing hand coding in critical applications, including automotive and DSP.

Also, new embedded computer applications are emerging almost daily, sorely taxing available design resources. Such custom techniques cause design budgets to soar and development times to stretch out. Both can spell disaster in a highly competitive market—but perhaps most critical are time-to-market issues. Computer-aided tools are only part of the answer; the other part is standards: standard operating systems, languages and computer architectures.

Applications skyrocket

Recently, there have been two important changes in the embedded computer world. First, the number and complexity of embedded computer applications have both skyrocketed. Products exist today that weren't dreamed of only a few years ago. In medical instrumentation, for example, there are CAT and PET scanners, portable blood analyzers and EKG machines, and IR imaging machines and other diagnostic tools that are a direct result of the availability of high-performance embedded computers.

Nor is the medical industry the only one calling for advanced embedded computers. In the machine tool industry, everything from the smallest benchtop lathes and milling machines to building-sized forming and casting machines is controlled with embedded computers. On the highways, traffic lights and warning signs depend on such systems, while similar devices compound fuels, brew beer and control a variety of other processes.

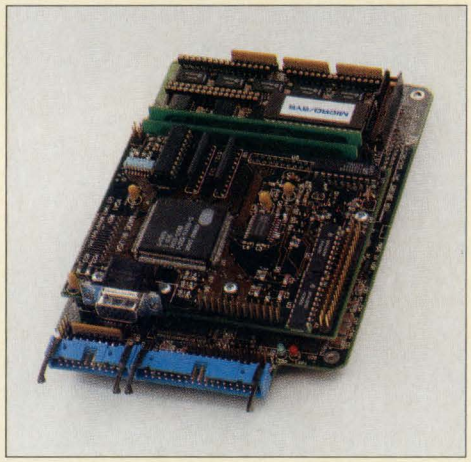
Computers embedded in equipment ranging from oil and coal generators to plating machines are constantly monitoring our increasingly threatened, fragile environment. Still others are embedded in instruments of exploration, from earthbound photometry devices to thermal imaging systems orbiting the planet. And the military depends on computers embedded in aircraft, missiles, tanks, and simulators to increase precision and lower cost.

Computers aren't just being embedded into new products, either; they're also finding their way into everyday items, from familiar household appliances such as the washing machine, refrigerator or oven to games, TVs and other entertainment devices. They're used as well in all areas of telephone, data and video communications, whether business or consumer.

Standards taking hold

The second important change has been that there's a growing trend toward adopting software and hardware standards to simplify design, speed development time, better utilize resources, reduce testing requirements, and raise overall quality. Among the issues in this area: standards are more a moving target than in the past because de facto market standards have become as important, or more so, than legislated standards. And recently, standards are looking more at logical and architectural, rather than physical, embodiments.

New SBC from Micro/Sys



Indicative of the trend toward nonstandard bus-embedded computers is a new single-board computer from Micro/Sys (Glendale, CA). Best known for its STD-based products, Micro/Sys has abandoned the standard-bus form factor in this product for MS-Windows and PC-architecture standards. It's WindowCard/486 is a compact SBC based on the Cyrix 486SL that measures only 4.5 x 7.8 in. The system can accommodate up to 8 Mbytes of system RAM and a complement of semiconductor disks specifically targeted at Microsoft Windows 3.1. The flash memory that's included eliminates the need for mechanical disks when embedding Windows into larger systems. This flash memory takes the form of a "read-mostly" disk that stores up to 20 Mbytes of Windows, DOS and user executables, as well as data-link layers and other system files. A separate battery-backed-up RAM disk is used to store other, more frequently written-to files, such as .INI and swap files. The board is made for mounting on a flat surface using a set of standoffs, although the company offers an optional STD Bus card-edge connector.

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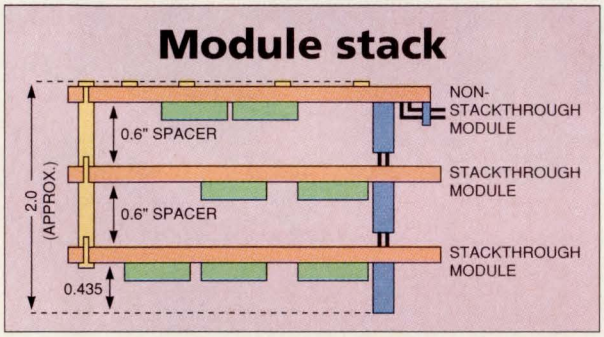
CIRCLE NO. 59

For example, the IBM PC and its compatibles follow a standard, but the standard I/O bus—ISA or EISA—has been supplemented by embedded solutions that use neither; rather, they modify the basic architecture of the PC itself. These approaches include PC/104, STD and a variety of single-board PCs. Also, with the introduction of Intel's Peripheral Component Interconnection (PCI), ISA and EISA may largely disappear—or at least be relegated to systems with specific, nonstandard I/O requirements.

Similarly, the Sparc-based Sun workstation, along with its compatibles, is setting a de facto standard.



While many manufacturers have chosen single-board solutions, it's not always possible when using them to include all the features and I/O that OEMs need. Responding to this need, more than 20 manufacturers have formed a consortium to back a miniature version of the ISA standard. Both stackthrough and non-stackthrough modules are illustrated.

There are now about a dozen manufacturers of Sun-compatible workstations, including a number of companies that offer boards and subsystems exclusively for embedded applications.

Of course, these examples depend on standard operating systems and software—DOS in the case of the PC and Unix (or SunOS/Solaris) in the Sun environment. Without these operating systems, and the body of readily available, shrink-wrapped software accompanying them, such standards probably wouldn't survive. Beyond software and OS compatibility, however, these de facto standards depend on a common computer architecture to provide hardware compatibility. And that common architecture is supplied in virtually all cases by complete chip sets.

Just as board-level interface chips—the MPC of Multibus II and VIC/VAC chips for VME—solidified standards at that level, computer-architecture chip sets are establishing a new set of standards in their area. Until now, these standards have been fluid, but that appears to be changing. With the release of the PCI interface standard and the emergence of PCI silicon, PC computer-architecture chip sets will be removed from—and so become transparent to—the computer interface. Similarly, Sun's M bus isolates processor, memory and cache architectures, whether on chip, module or board, from the computer interface. And with formal release this month of SBus interface ICs—the Goldchip and SLIC—standard SBus interface silicon will be available that supports both 32 and 64 bits.

While there's little question that the 80X86 is a standard, and that Sun has been at least partially successful in attracting a following for its Sparc architecture, there are at least two, and possibly three, other processors that could develop into architectural standards in coming months.

Digital Equipment Corporation (Maynard, MA), with fanfare fit for a bet-the-company announcement, declared its Alpha processor the beginning of a new generation. While it hasn't attracted a following of thousands yet, there are at least a dozen companies with Alpha-based projects currently under development.

What may add to the popularity of Alpha is the fact that it will debut on the industry's first Futurebus+ workstation later this year. And with Alpha-based Futurebus+ cards emerging from at least four manufacturers, Digital's device could well thrust Futurebus+ into the forefront as a market—as well as an IEEE—standard. If Alpha-specific Futurebus+ interface silicon emerges, with Alpha as a local bus, the chip will become even more important—particularly in the military and telecom areas.

Still avoiding the spotlight is IBM (White Plains, NY), with its RISC 6000 chip set and, in conjunction with Motorola (Tempe, AZ), its All-American RISC offering in the works. IBM has held its technology close, keeping it proprietary, perhaps because of its experience with personal computer clones. The company's strategy, however, has been very successful if measured by the reception of the RISC 6000 family of workstations. The success of this line as a leading computer architecture, though, depends on many factors—including its relationship with Apple, Motorola, Microsoft, and others.

Perhaps the most difficult trend to forecast at this time is the relative potential of the MIPS Computer (Sunnyvale, CA) architecture. When it first came out it seemed destined for market dominance, garnering as it did the support of Digital, Compaq, Silicon Graphics, and 138 other companies looking for a standard-computer architecture. Billed as the Advanced Computing Environment (ACE) consortium, this group of software and hardware vendors embraced the MIPS architecture as the basis of an entire family of products, from operating systems to workstations.

But between then and now things have gotten bogged down. Digital, although it still professes its support and makes MIPS-based workstations, has eclipsed its own MIPS activity with its Alpha announcements. Compaq has dropped MIPS and its ACE activity in a corporate reorganization. Silicon Graphics, hoping to keep the technology alive, has purchased MIPS Computer. But while MIPS keeps cropping up in products, no complete chip sets have emerged, as was the case with Sparc and the PC, and it's doubtful that Silicon Graphics has a large enough following to support the architecture single-handedly. It's even questionable whether Digital, with a far larger installed base, can make its Alpha a market standard.

Board-level split

Although the emergence of computer-architecture standards may bode well for the standard-bus, board-level community, it's certainly a double-edged sword. Currently, the bus industry is solidly focused on the medium-performance, medium-price arena, with systems calling for multiple boards, card cages, power supplies, and other components. But both existing and new applications are moving quickly in two other directions.

In one case, applications are calling for smaller, more compact, less expensive, and more power-stingy products.

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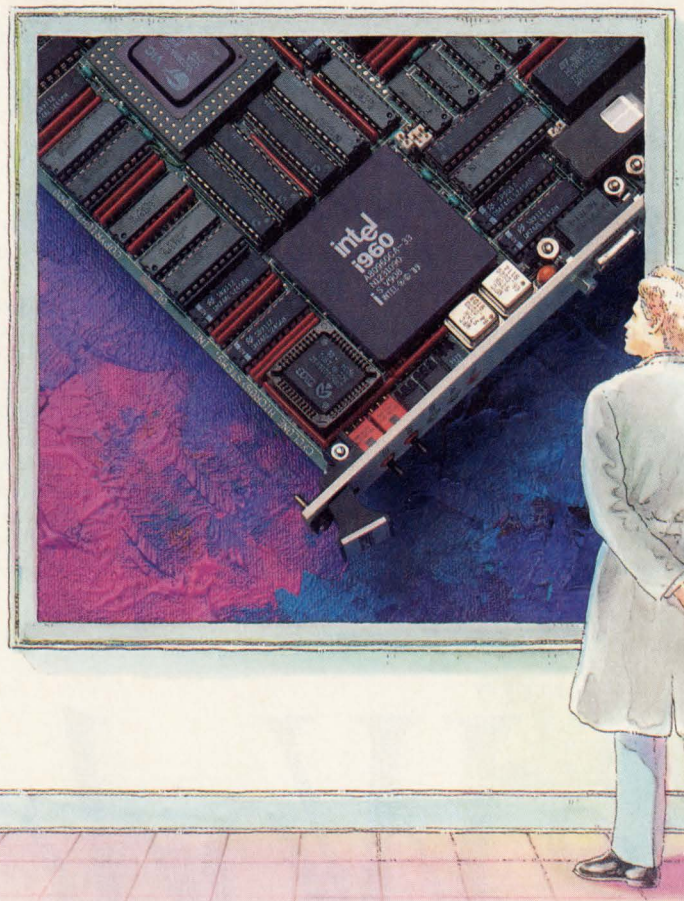

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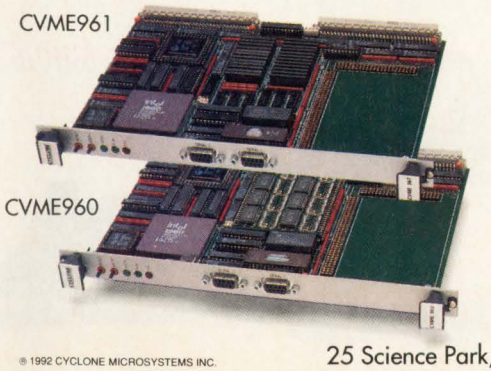

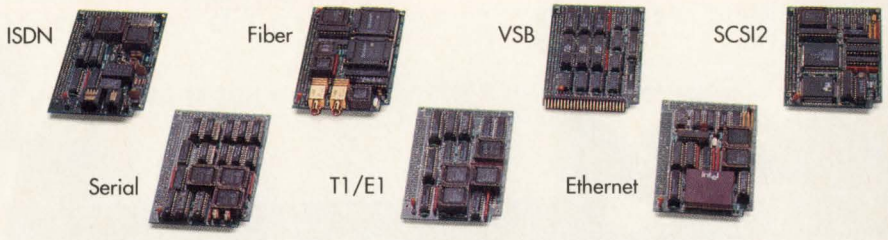

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CIRCLE NO. 60

At the other end of the spectrum, embedded applications require supercomputer power with ever faster I/O. In both cases, end users are demanding that standards be built in for hardware and software.

At the low end of the performance spectrum, the ubiquitous PC has commandeered applications that might otherwise have gone to other bus architectures, such as VMEbus, Multibus or STD. But special, industrially hardened versions of conventional PCs are needed for many of these applications, or else they've gone to other form factors or buses, because desktop PCs don't work well in harsh environments.

Other reasons for switching from the traditional PC form factor, which includes motherboard and ISA or EISA adapter cards, vary depending on the application, but size, power dissipation and reliability have often been cited as reasons. In applications for more robust physical and computing environments, standard bus architectures such as Multibus II, VMEbus or STD Bus are employed, with an embedded PC on the host bus.

The small-form-factor computer

More and more, however, applications are calling for embedded computing power in a small form factor customized for particular functions. In the past, such solutions took the form of custom designs, with engineers working from scratch to design and lay out the embedded machine. While this approach may ultimately lead to the most efficient computer optimized for the application, practical considerations make other alternatives look attractive.

At the low end of the performance spectrum, the ubiquitous PC has commandeered applications that might otherwise have gone to other bus architectures, such as VMEbus, Multibus or STD.

Standard off-the-shelf or semicustom computer approaches based on the PC architecture are now available from a number of vendors in different form factors with a variety of options. One of the leaders in providing such technology and disseminating it to other manufacturers and users has been Ampro Computers (Sunnyvale, CA). The company has standardized a subset of ISA bus attributes in a compact form factor and rallied more than 20 manufacturers to support the concept, now known as PC/104. The group produces a variety of CPU and I/O modules.

While bringing standard-PC hardware and software to small-form-factor embedded applications may seem unnecessary in an age of

full-function chip sets, the benefits of the PC approach are often overlooked. In many applications, particularly those with relatively low volumes, the cost of a custom-designed computer can be prohibitive. But even in large-volume applications, a standard board may be as effective as an in-house design.

Quality, cost and time-to-market

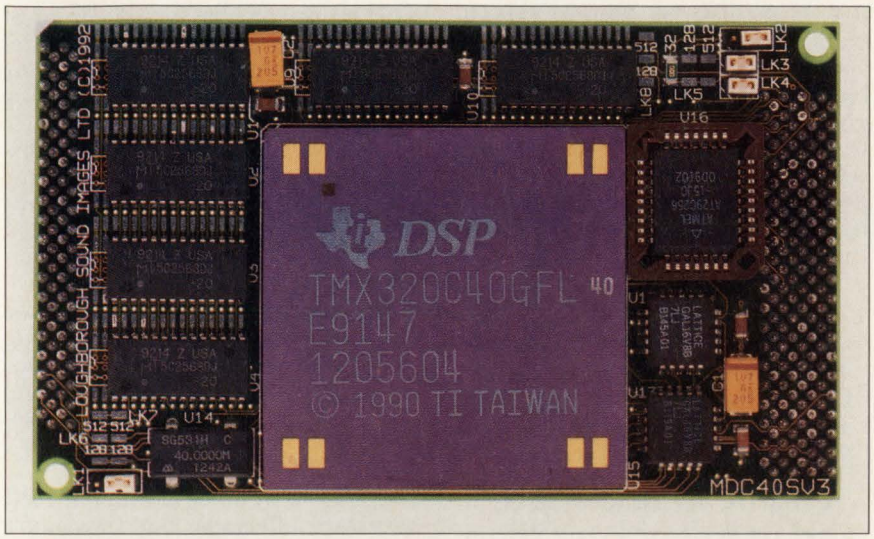
In the first place, specialty manufacturers of small computers can often realize significant economies of scale, because they sell to many different customers. Second, designs are rigorously tested, guaranteeing a level of reliability not easily achieved with design-your-own approaches. Third, specialty houses often make deals with semiconductor makers that guarantee a certain "life of product" by buying end-of-run quantities of critical chips. In the volatile PC environment, this can be an important factor, particularly if subsystems must pass exhaustive qualification tests. Fourth, design houses developing small, embeddable computers are highly specialized. They can often assemble a general-purpose computer engine in less space and at lower cost than a less experienced designer could accomplish with a fully custom design. Fifth, add-on or mezzanine modules such as PC/104 devices or IndustryPacks are frequently available to perform a broad range of functions. And for specialized functions, custom-I/O mezzanine boards can be designed either in-house or by the vendor.

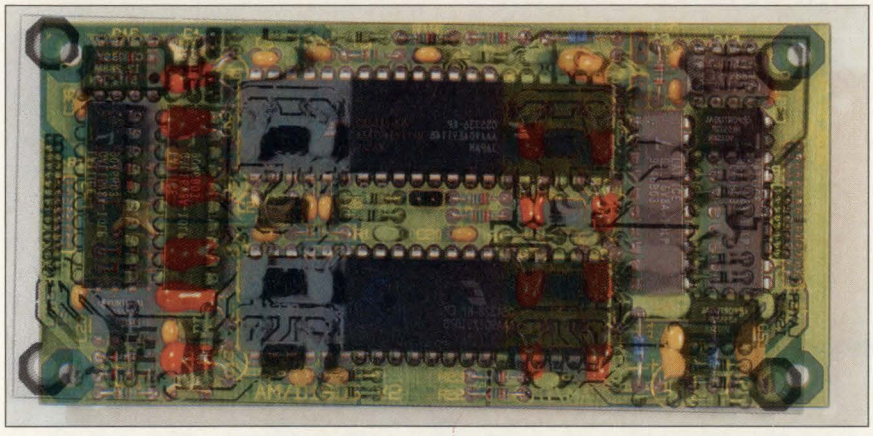
Specialty manufacturers . . . can often assemble a general-purpose computer engine in less space and at lower cost than a less experienced designer could accomplish with a fully custom design.

Finally, and perhaps most important, makers of packaged computer systems sell time-to-market. Dedicated design time for an embedded computer subsystem goes from a significant interval to zero in this scenario. And not only does design time go to zero, but inspection, testing and evaluation times for both incoming components and completed subsystems are reduced almost to zero.

No single solution

There are a number of standard PC hardware offerings, but they don't quite fill every application niche. To satisfy those uncovered applications, some companies offer quick-turnaround capabilities ranging from semicustom approaches to full-custom designs. Semicustom approaches such as that of Ziatech (San Luis Obispo, CA), called ASAP





Underscoring an industry trend toward mezzanine boards is this DSP module (upper photo) based on Texas Instruments' 320C40; it's from Spectrum Signal Processing. The board can be plugged into existing platforms, such as VME or PC carrier boards offered by Spectrum, or it can work well with any single-board CPU. The DSP module uses a standard pin-out developed by Texas Instruments for its C40 family of DSP devices. Spectrum Signal Processing has also developed an analog-to-digital converter mezzanine module (lower photo) that can be plugged into a broad variety of hosts. Aside from providing systems with much flexibility, the module increases the fidelity of the analog section because it's isolated from the carrier.

(application-specific automation processor), provide a standard architecture and form factor onto which a variety of standard and custom functions can be added. Using board- and system-level CAD, the company is able to turn fully functional designs around in only weeks.

When more customization is required—for example, a different form factor—there are several companies capable of clever designs and, in many cases, they can provide complete library functions for CPUs, computer subsections and I/O. S-MOS Systems (San Jose, CA), for example, does highly specialized packaging and has state-of-the-art printed-circuit and mounting techniques that include everything from flexible mounting materials to ultra-fine board geometries.

Still, there are many embedded applications where a PC, in spite of a variety of offerings and a growing installed base, just won't do. These applications were originally design-and-build-your-own as a rule. Some, where standard boards such as VME or Multibus were used, were primarily proof-of-concept or prototyping tools; production went to in-house design and manufacture.

Two-step migration

Over the past few years, many of these applications have migrated to standard-bus architectures. This has in part been the result of board makers who've gotten their acts together to provide some level of plug-and-play compatibility—and perhaps also to remain flexible in a fast-paced technology market.

But a bus-based solution requires a card cage, two or more relatively costly boards and, of course, all that software—such as drivers and RTOS—to make the boards work together as a system. This can result in a costly, large and cumbersome end product that often takes time to get up and running. Also, the incredible shrinking transistor has hit again. With greater transistor counts, functions that previously needed an entire circuit board can now comfortably reside on a single chip.

As a result of such developments, industrial-strength, board-level technology is rapidly changing. Applications met by medium-performance, standard-bus, multiple-board technologies are migrating toward single-board solutions supplemented by mezzanine boards to add flexibility and customized I/O. While some of these applications are shifting over to PCs, many need the higher performance level of the Motorola 68000 family of RISC processors or the networking and multitasking capabilities of a Unix platform.

The first move to single-board solutions came when Sun Microsystems Computer Corporation (Mountain View, CA) announced it would offer a board version of its Sparcstation for use as an embedded computer. Sun already had a large following of users for its single-board and board-set Sun 3 and 4 computers, which it offered as both 6U and 9U VME platforms for embedded applications. Its new approach simply consisted of a Sparc-based motherboard with a pair of connectors for SBus modules.

Follow the leader

Sun's approach was so successful that this past June it relinquished all VMEbus business—over $25 million in sales at its peak. The company has converted, or will convert, 70 percent of its VME customers to its Sparcengine/SBus platforms. It plans to continue to serve the remaining VME traditionalists through a technology exchange agreement with Force Computers (Campbell, CA), which will continue to offer the latest Sparcstation technology on a VMEbus platform.

Force too was quick to see emerging opportunities, though; through good planning, serendipity or delays

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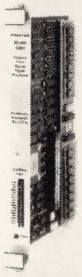

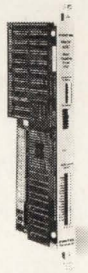

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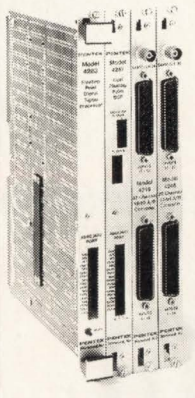

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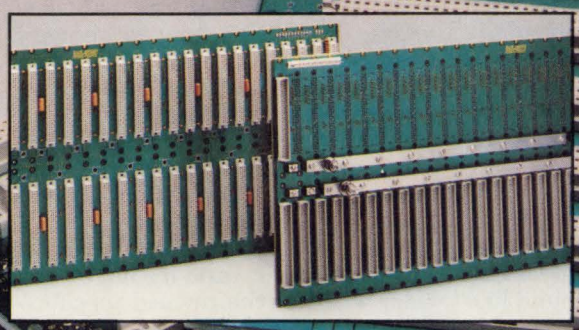

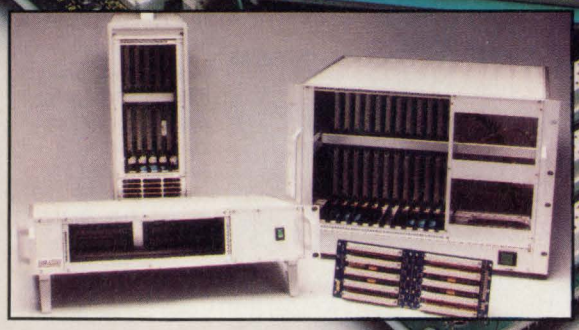

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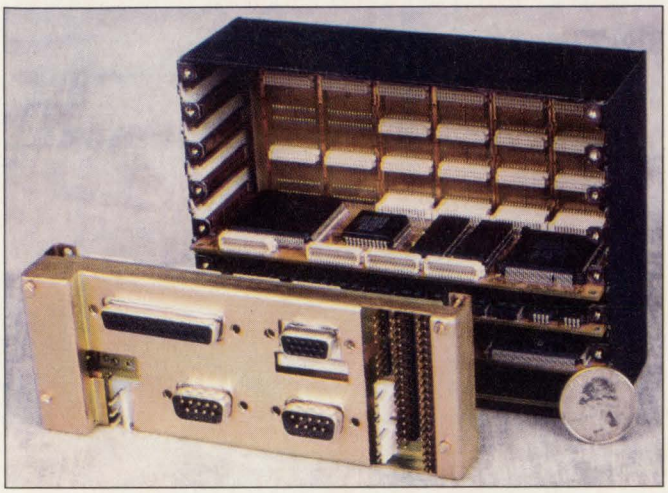


Dover Electronics has developed its own miniature PC-bus-based standard, for which it provides a variety of different modules, including a single-board computer, modem, fax modem, network interface, SCSI, data-acquisition systems, memory, and others. Pictured is its extremely small package (ESP) evaluation system.

in getting its latest VME interface completed, the company recently announced a 6U Sparcengine 2 without a VMEbus interface. A version with the full VMEbus interface is expected to be released later this month. Both carry a pair of SBus slots.

While the Sparcengine has taken off as a single-board embedded computer, there are still applications looking for a more comprehensive but flexible solution. The trend here, it would appear, is away from component-based solutions. Performance Technology (Rochester, NY) is the first of the Sparc/SBus vendors to provide a complete embedded system with its SBus/System. Performance packed a Sparc-based motherboard with most of the regular features, such as Ethernet, SCSI-2 and serial ports in a box with a power supply and up to eight SBus slots.

This box-level product is targeted at real-time embedded applications, although the company is currently looking to port to Sun's Solaris operating system. According to company executives, the approach is getting an encouraging reception, especially from users of single-board solutions. Once again, passing along mounting, power supply and other hardware aspects to the subsystem vendor lets the application developer concentrate on his or her own area of expertise.

Further underscoring the shift to single-board as opposed to bus-based solutions, Motorola, the world's leading VMEbus manufacturer, introduced its latest single-board computer (SBC) with the announcement that it would be available with or without a VMEbus interface. To provide I/O flexibility, the board, Motorola's MVME162, includes sockets for up to six IndustryPack modules. GreenSpring Computers (Menlo Park, CA), the creator of the IndustryPack, also offers a busless board with IndustryPacks for I/O that's based on the Motorola communications processor, the 68332.

And PEP Modular Computers (Pittsburgh, PA), the leader in 3U VMEbus technology, has been a pioneer in offering busless 3U VME boards. The offerings are part of the company's industrial-automation platform, tying stand-alone SBCs and card cages together with an industrial serial communications scheme, Profibus.

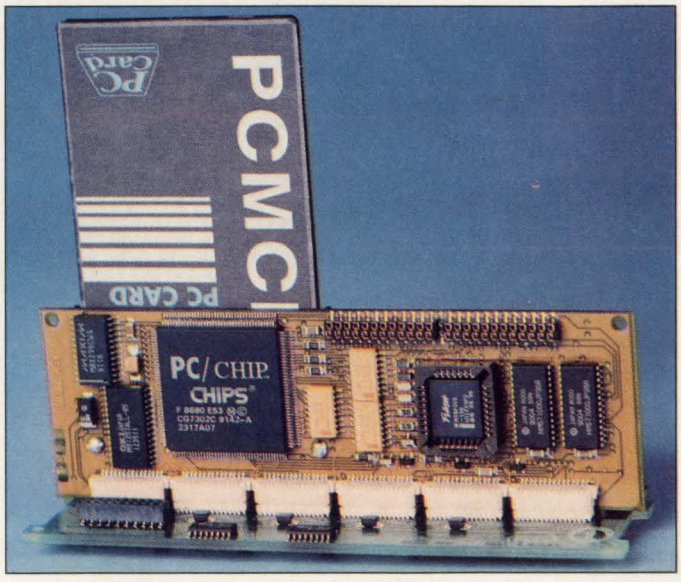
Standard buses alive and well

Focusing on the migration to single-chip and single-board design for embedded systems makes it sound like the conventional board business is disappearing. That's not the case at all. Standard-bus, multiple-board solutions abound and the market will continue to grow, although not necessarily in many of the same applications or using the same technology as was previously the case.

Multiprocessing, for example, is the undisputed domain of standard-bus approaches. Digital, as mentioned earlier, seems to have a leg up in the Futurebus+ arena with its Alpha architecture. There are also currently two other functioning Futurebus+ boards available—a 68030-based board from Cable and Computer Technology (Anaheim, CA) and a MIPS R-3000 board from Nanoteck (Idaho Falls, ID). Still another CPU based on Intel's 80486 is under development at Force Computers, with completion expected late this year. But the Alpha architecture will be first to ship in volume in a commercial system, and this will undoubtedly lead—at least in the near term—to a move to Futurebus+.

Too often, however, press for Futurebus+ overshadows activity in other areas, particularly VMEbus. Many VMEbus manufacturers have had to claw their way through tough economic times over the past few years, but there are some very bright spots on the horizon. Revision D of the specification, for example, which includes the formal definition of VME64 as well as SSBLT and some much-needed revision to the basic timing specification, is just about ready for acceptance.

While there are some political hurdles to clear—and it's not totally clear whether the revised specification will be an IEEE or an ANSI specification—the result will be a



Dover Electronics offers a 386-based single-board computer in its ESP format. The CPU contains a 16-, 20- or 25-MHz 80386 processor and a PC chip set. The device also provides a slot for an optional 80387 coprocessor. Unlike other small-form-factor CPUs now on the market, it's equipped with a connector for a PCMCIA card (shown) in the rear, while still filling only one ESP slot.

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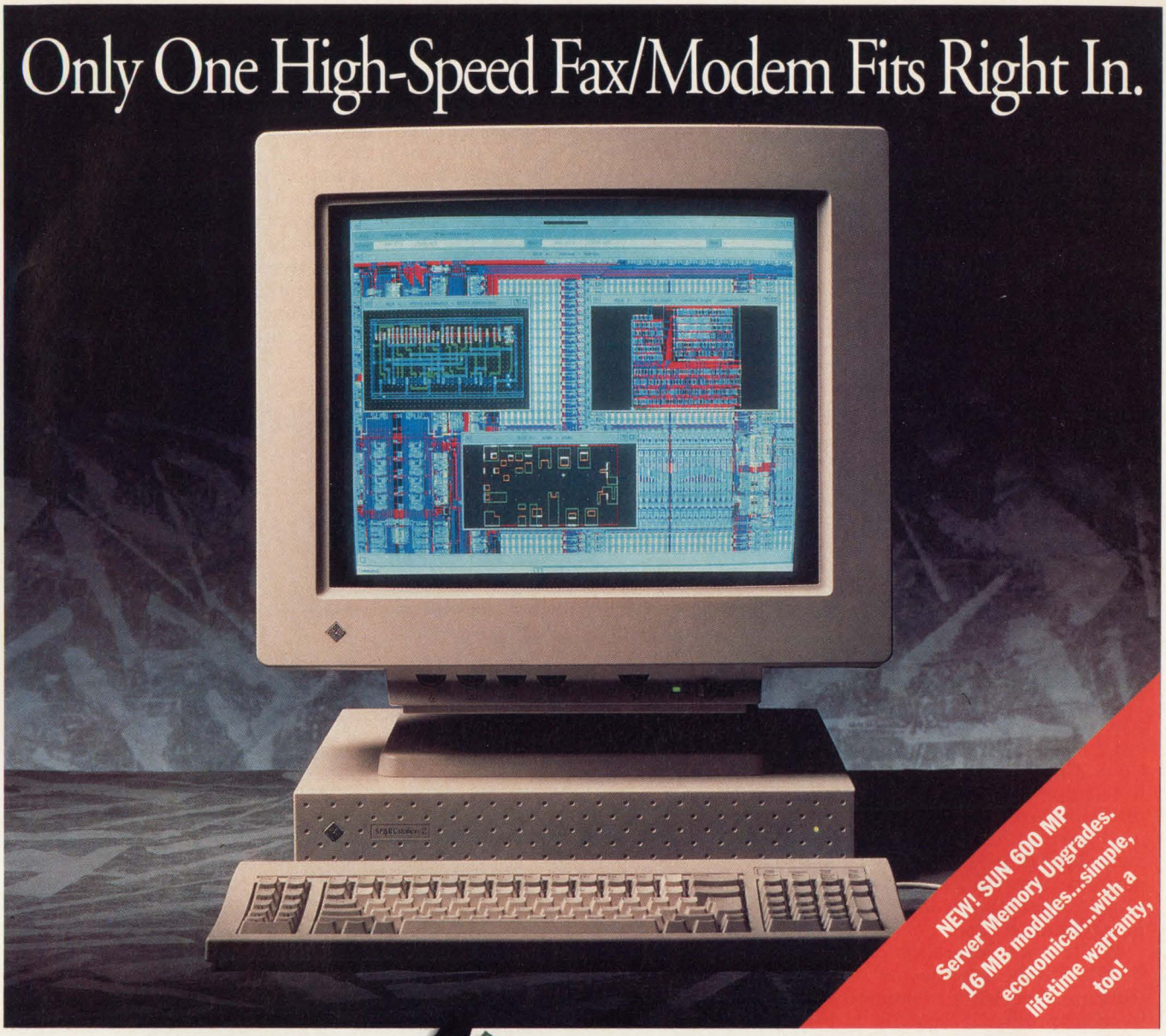

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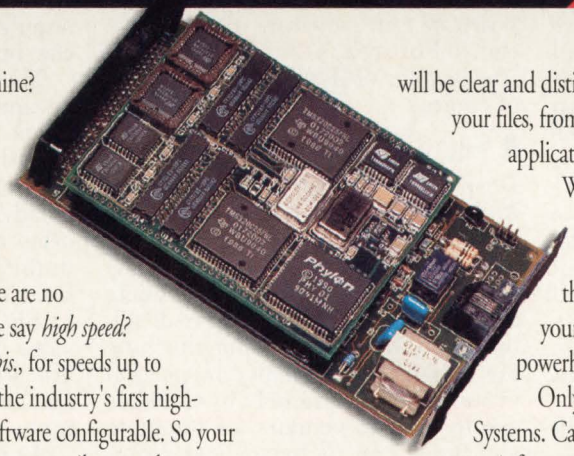

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revitalized VME with transfer-rate capabilities in the 150 Mbyte/s range. In addition, a separate subcommittee within the VME group is finalizing details of a relatively simple live-insertion/hot-swap technique it expects to unveil later this year.

Similar developments have been taking place in the Multibus II camp, where a die shrink on the MPC and new transceivers let Multibus II manufacturers double the transfer rate. Also, the Multibus II group was an early proponent of hot swap and live insertion, and has developed a technique that was demonstrated over a year ago.

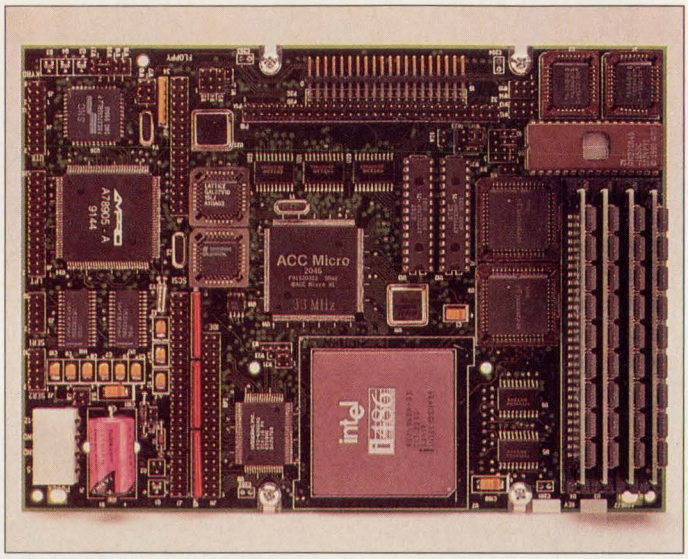
The combination of hot-swap capability and the revised specification will give what many in the industry refer to as the "midlife" kickstart VME needs to be viable through the 1990s. The enhanced VMEbus will take its place in many communications-based applications, which are expected to form one of the hot application areas over the next several years. Similarly, Multibus II will experience a revitalization, but it operates from a much smaller base.

While the Futurebus+ Profile T Subcommittee is working feverishly to complete the telecom profile, it's not likely to go to sponsor balloting much before year-end—if then. Final approval isn't expected until late spring or early summer of 1993. And even then, there are no silicon solutions to address the protocol, with all its required features.

Profile T hardware and software probably won't see daylight until 1994 or 1995, and even then it will take time to ramp up production and develop the critical mass of products required to support a standard bus. Meanwhile, the applications that have been waiting for Futurebus+ can't wait any longer, and VME will be filling those slots. Futurebus+ hardware will be debuting throughout the last half of the decade, but VME will still remain the dominant architecture.

A similar scene will be played out in the military market, but because military procurement is done on a contract basis, it's likely some Futurebus+ offerings will be adopted as standards-based hardware, when in truth the approaches will be largely proprietary. At least two contracts have been let for Futurebus+ hardware, although there's no commercial off-the-shelf (COTS) hardware yet available.

The military will undoubtedly use more and more COTS equipment for prototyping and noncritical applications, reserving full military-hardened gear for those applications calling for it. While it's expected the military will continue in the direction of Futurebus+ for the balance of the decade, VME will still be the bus of choice.



Ampro Computers now offers a LittleBoard/486 single-board computer in the same format it used in its LittleBoard/386. While the SBC has a variety of commonly used features on-board, it also provides a PC/104 port for OEMs that might want to add options not included on the base board.

Solutions, not just boards

Despite all this activity for VME, Multibus and other leading bus architectures, fewer and fewer OEMs are interested in assembling the computer segment of their products from scratch. Whether they're developing an automated teller machine for a bank or a quality inspection system for an assembly line, OEMs are looking to vendors for complete solutions, and no longer just a couple of boards they have to painstakingly assemble and wrap software around.

For this reason, some traditional board-level manufacturers expect to provide systems rather than just boards. This is apparent in Performance's Sparc/SBus system, but even VMEbus manufacturers are looking in the same direction. OEMs today are less concerned about what's in the box, as long as performance and reliability parameters are met, and provided the product fits mechanically, is priced right and does the job.

Over the next few years, we can expect to see more traditional VME board makers providing systems—boards, backplane, rack, power supply, OS, and, in some cases, even applications software. Such a systems orientation will apply to both conventional bus-based approaches with multiple boards and single-board versions of VME, Multibus, PCs, and other platforms.

At the same time, the traditional market for VME and Multibus II equipment—large-scale multiprocessing—will continue to prosper, but not at the rate it's experienced previously. The applications that benefit from a loosely coupled multiprocessing architecture—particularly in simulation, specialized image and signal processing, and specialized factory automation and control applications—will continue to rely on traditional bus architectures, even though they won't supply the growth needed to sustain the business.

The 1990s will undoubtedly be a decade of change. VMEbus and Multibus will continue to experience growth, but not in traditional process control and automation areas. Instead, the growth will take place in other application areas, such as communications. The once-exclusive domain of bus-based solutions will shift to SBCs with mezzanine bus extensions. Futurebus+ will begin its slow but steady climb to dominance and Scalable Coherent Interface (SCI) will make its commercial debut.

As is the case with any advanced computer technology, however, these application areas will be driven by the availability of interface silicon. And the complexity of the silicon seems to grow exponentially as each new approach increases transfer rates and promises sophisticated features. ■

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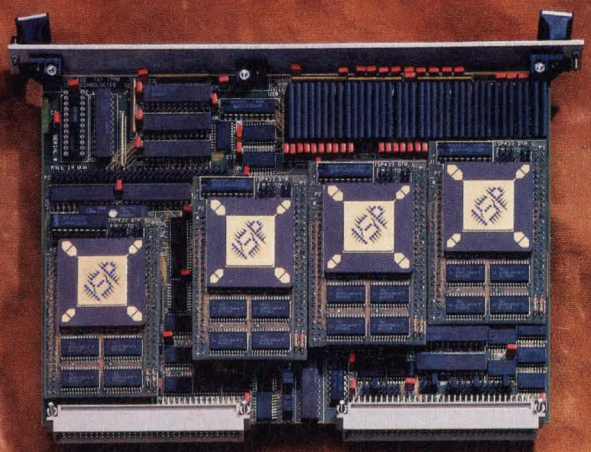

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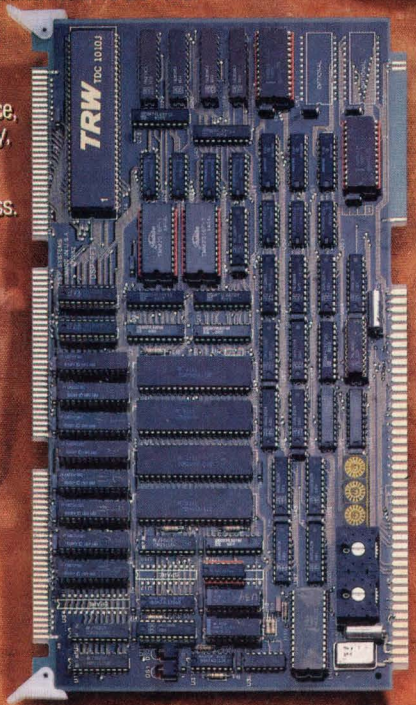

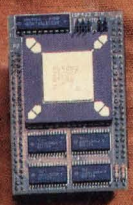

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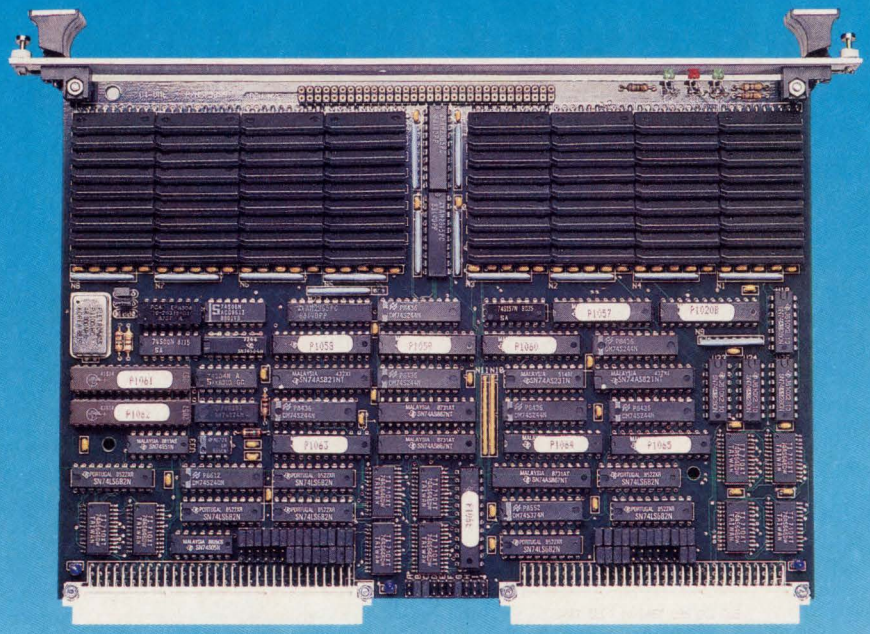

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Object-oriented methods transform real-time programming

Making the change to object-oriented approaches for software development isn't free. It takes time, training, tools, and organization. But for those willing to invest, the payoff can be enormous—for small jobs as well as big ones.

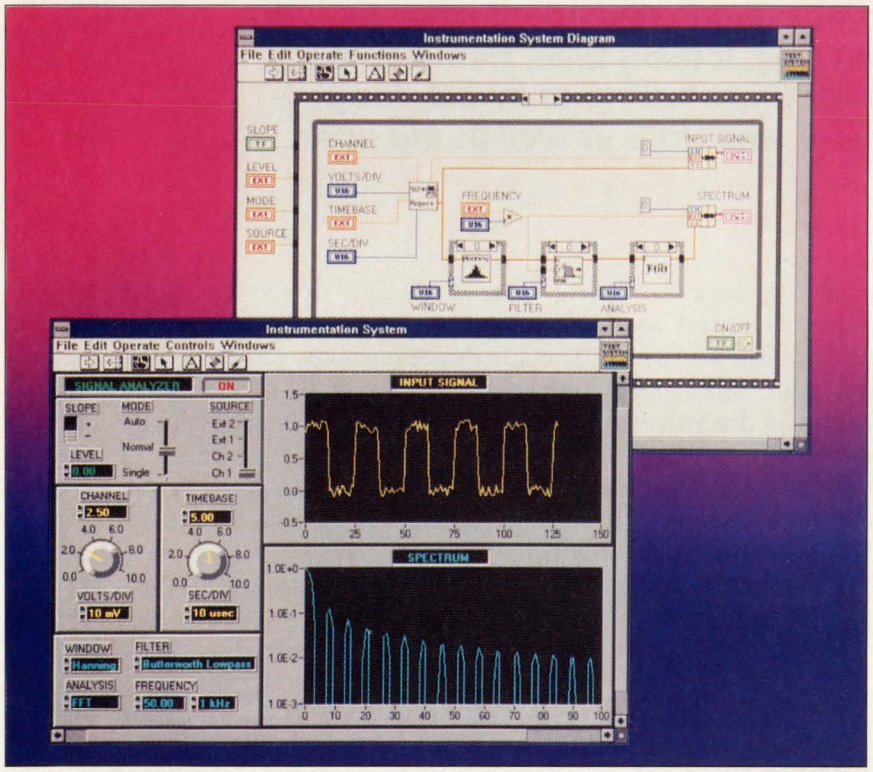
It's often said that software developers moving from a design approach using procedural languages to object-oriented methods must undergo a fundamental transformation in the way they think and work. But for developers of real-time and embedded systems, that shift isn't nearly as great as it is for other programming disciplines. Real-time programmers are already accustomed to thinking of their systems as "networks of cooperating machines," in the words of Garth Gullekson, senior marketing manager for Bell Northern Research (BNR—Ottawa, Canada).

The independence and intercommunication of distributed computing nodes on a network naturally encourages one to think of them as distinct objects. Nodes have well-defined inputs and outputs; they perform precisely defined operations on their inputs; they can be arranged in hierarchies to form larger machines out of smaller ones. Even in a single-processor multitasking system, different tasks must be encapsulated.

Tom Williams, Senior Editor

Since the designer of an interrupt-driven system can never know how often or in which order the tasks will be invoked, he or she must see to it that they can run as independent entities when called.

The trouble is, this intuitive approach to building real-time systems lacks the formalism and discipline of true object-oriented design. For example, the interfaces between modules aren't strictly defined, and this makes it hard to build systems based on a hierarchy of small modules. As a result, code is seldom reusable without modification.



Object-oriented technology has promise for both large and small applications that let non-programmer experts more effectively use computers to attack their problems. LabView by National Instruments lets you design your own custom virtual instruments with a graphical programming environment. The front panel is designed by placing object-like knobs and displays on a screen. The "instrument" is then programmed by "wiring" together functional objects within program control structures and then connecting them to symbols for the front-panel devices and physical I/O.

Doing what comes naturally

Adoption of object-oriented design and programming approaches can help a real-time developer work in a way that more naturally maps to the inherent nature of the systems being built, while providing the advantages that object-oriented design bestows on all branches of programming. These include the abilities to deal more easily with complexity, to create libraries of reusable code and to begin designs at a higher level of abstraction, where you can effectively examine trade-offs before you commit to actually coding a prototype.

Object-oriented design also lets you produce system design and architecture tools that permit experts who aren't programmers to bring their knowledge to the development process. Much in the same way that spreadsheets relieve people whose primary expertise is in business from the burden of thinking in Cobol, object-oriented design can let experts more easily use computers to accomplish their goals.

It's still true, however, that developers must go through some significant changes in the way they approach problems, and they must have tools that help them work in the areas of object-oriented design and development. Recognizing that objects are still pieces of code, object-oriented design concentrates more on what those pieces do rather than on how they work internally.

What objects do is send messages to other objects, which operate in terms of "methods," or well-defined behaviors. The interfaces between objects and object types are clearly defined, so that your main task is to select the proper objects and combine them into larger objects that aim toward the goal of the design. Once larger objects are built and tested, they can be added to the stockpile or library of classes for reuse in other applications.

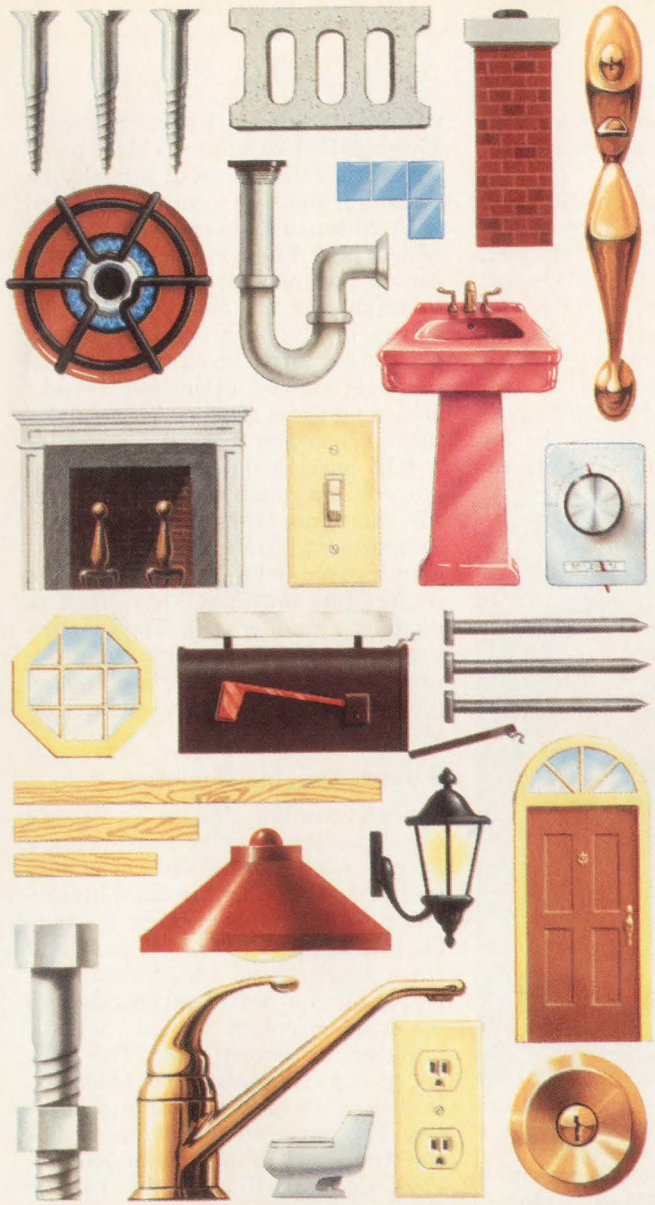
Classes can best be described as potential objects that become true objects when they're instantiated with data for use in an application. Individual objects, as well as subclasses and superclasses of objects (and their members), can inherit behavior, even if they're given additional characteristics. This eliminates the need to write so much repetitious code.

One major difference between working in a structured language such as C and using object-oriented development techniques is that in C you've got a relatively small set of key words and a group of syntax rules. The programmer's skill consists in being able to combine these key words and syntax rules to build all kinds of elaborate applications. In object-oriented development, you've got a large library of classes that can be instantiated as objects to do specific things. The programmer's skill resides in browsing through the class libraries, selecting the right classes and creating out of them the application—along with new classes that can be added to the library for reuse.

Making the transition

The two most popular languages for object-oriented programming are C++ and Smalltalk, both of which are available from a variety of vendors for a wide range of computer systems. But languages alone don't ensure success in object-oriented development. In addition to getting used to a new thought process, you've got to have tools to help manage the process, to aid thinking in the new mind-set and to access the richness of functionality contained in the class libraries.

For larger companies, the shift to object-oriented development means changes not only in organization but also in the expectations of management, ranging from the initial return on investment to ideas about incentives and the way employees are rewarded for their work.



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Anyone making this move must accept the fact that the rewards of an object-oriented approach, although substantial, aren't immediate. It takes time to get people adjusted, to put new tools in place, to create novel forms of organization, and to build up that stockpile of reusable code everyone's always talking about. The first project isn't going to have a positive impact on the bottom line.

"Many people tend to look at incorporating object-oriented methods into their operation as basically a tool purchase issue," says BNR's Gullekson. Still worse, some think of it as simply switching to an object-oriented language.

Without an enforced discipline to maintain an object-oriented approach (which isn't provided by a language such as C++), "all you've done is change the size of the gun you can shoot yourself in the foot with," says Richard Jensen, vice-president of new business development for Applied Microsystems (Redmond, WA). "A procedural language is designed to solve a problem that was thought out procedurally, so when you try to do an object design off that, it's inconsistent with the programmatic interfaces you need to do the job correctly."

The proper mind-set

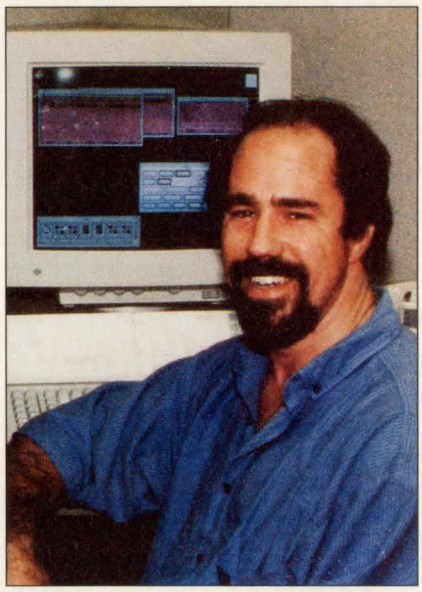
If object-oriented development is really gluing a bunch of things together to make something happen, then it's best to retain that mind-set, so that any incongruencies you encounter aren't solved by dropping out of object orientation and writing some procedural fix. Rather, such problems are solved by creating a new object, with the view that you'll be able to use it again sometime.

So just turning a C programmer loose with C++ will inevitably lead to procedural quick fixes, because C++ doesn't demand an object-oriented method. As Bill Hazard, manager of teamwork technologies for Cadre Technologies (Providence, RI), notes, "Object-oriented languages are much more dependent on tools to make them really useful than structured languages like C." People need to learn to think in terms of objects rather than procedures to make such tools really useful.

Putting people through the "paradigm shift" to get them thinking in terms of objects and abstractions can take about six months. Another major requirement, then, is a strong commitment by management to a long-term move to object-oriented operation.

That commitment shouldn't be precipitous, however. Grady Booch, director of object-oriented products for Rational (Santa Clara, CA), says, "The last thing you want to do is bet your next project on the new language and methodology, because you'll probably fail."

Although Rational provides software engineering facilities for implementing design notation, process



Rational's Grady Booch cautions that, in real-time applications, the way people analyze problems to build their abstractions (classes) can vary widely depending on the application domain. "I can't build a perfect abstraction that will work across all domains," he says. "So companies over time evolve libraries that are best fitted to the vertical application domain they're playing in."

and management of large projects, as well as a suite of CASE tools for object-oriented development, Booch recommends that a company first initiate a pilot project in which a team takes some piece of an existing system or a system under development and builds an object-oriented version of it. "You may ultimately throw it away," says Booch, "but the experience of doing it will help in that six-month period to get you into the mind-set of thinking with abstraction."

Interactive Development Environments (IDE—San Francisco, CA) also recommends a pilot project to ease the transition to object-oriented development. IDE will soon release its C++ Development Environment as a part of its Software Through Pictures line of CASE products. The company will initially be releasing the C++ product bundled with its consultation service, part of which is a Pilot Project Program. Among the goals of this program "are to make sure the customer's expectations are properly set at three levels: the executive level, the technical manager's level and the user's level," according to Ed Mueller, IDE's director of marketing.

IDE assigns one of its own employees as a consultant to work with the customer through the entire first project. "The customer has his own people who understand the project but may not know how to model it," Mueller says. The consulting service makes that marriage between application expertise and an understanding of how to define the problem via objects.

Restrictive, but flexible

Object-oriented design is in one sense more restrictive than using a procedural language—it works only with objects and within class hierarchies. But at the same time it's very flexible, because the way classes and class hierarchies are defined depends on the user's perspective on his or her problem.

Rational's Booch says, "The reality of object-oriented technology is that it's very incremental and iterative. I've never written a class right the first time." You have to define a class and see if it really fits the problem domain you're working in; then you have to refine it. As an example, Booch notes that if you're building an airplane, you might define it in terms of objects such as wings and engines. But if you're in air traffic control, airplanes might be perceived in terms of position, velocity, passengers, and altitude.

The flexibility of object-oriented approaches results from the fact that you can define objects using nouns found in a requirements specification. You create these objects out of more general-purpose, existing objects, or, in rare cases, you might write new classes from scratch, all the while making sure they follow all the rules of encapsulation. It's very important, then, that application experts have control over how problems are broken down and how class hierarchies are built, because the true value of reusable class libraries comes because they're tailored to the specific appli-

Real-time object-oriented programming systems

Despite the much publicized benefits of object-oriented technology (OOT), developers of real-time and embedded applications have been slow to adopt it. Most experimentation has been with C++, and then only as a "better C." As a result, there are widespread fears that object-oriented programming suffers from performance problems.

Meanwhile, OOT has taken the rest of the software world by storm. Software developers have found that objects model the problem domain much more effectively than procedural software. OOT lets you build systems from reusable components. Encapsulation and inheritance provide powerful tools for building software analogs of real-world objects. Productivity is dramatically enhanced—some reports claim by an order of magnitude—and code is more reliable and maintainable. Garbage collection eliminates memory management errors.

Diving into OOT

Those few real-time developers who have taken the plunge into OOT are completely sold on these advantages. The rest continue to sit skeptically on the sidelines. So, what's going on here?

It's a common misconception that real-time systems must be "fast"; the real requirement, in fact, is to be "fast enough." Raw speed doesn't automatically translate into better performance. For large software systems, most performance problems can be traced to the complexity of the application. Unfortunately, programmers aren't very good at predicting where such performance bottlenecks will occur.

This is where OOT comes in. Developers using a high-productivity environment such as Smalltalk can build an application quickly and collect performance data early in the development cycle. Because encapsulation results in strong, well-defined interfaces, it's easy to change the OO application to eliminate performance problems as they're identified. No guesswork is needed to identify bottlenecks and no time is lost optimizing code that doesn't lie on the critical path.

How much reworking will be needed? This is difficult to predict, but the old maxim that 90 percent of the time is spent executing 10 percent of the code suggests that only a small fraction of the program will need to be changed.

This strategy is often more effective than programming in a language such as C and relying on optimizing compilers to deliver the required performance boost. A bias toward sophisticated optimizing compilers often means delays in shipping leading-edge products, since compilers are usually a generation behind the current hardware technology. Moreover, optimizing compilers create side effects that make performance measurement more difficult. The biggest performance gains come from smart programmers, not smart programs.

What about garbage collection?

Critics of OOT claim that garbage collection leads to unpredictable execution times and slow response. The proposed solution is to write code that doesn't create garbage—the "real men manage their own memory" approach. This would be a fine strategy if it worked. The trouble is that most interesting applications demand some dynamic storage allocation, and large, complex systems require lots of it. Multiprocessor systems in particular present real memory management challenges. There's almost no chance to successfully handle this without automated assistance.

OO systems such as Smalltalk use generation-scavenging collectors which are very efficient. In typical interactive Smalltalk applications, measurements show that garbage collection uses less than 3 percent of CPU cycles. By carefully analyzing the rate and type of new object allocation—and so of garbage creation—real-time implementers have been able to tune their systems to work very successfully with these scavenging collectors.

It's true that real-time applications would be easier to implement if the garbage collector was designed to have predictable, bounded behavior. Current systems don't support such real-time features because they were designed for workstations. This is an area of active development, however, and we expect that real-time collectors will be commercially available within the next two years. This will radically change perceptions within the real-time community.

Real-time Smalltalk

Although OOT got off to a slow start in the real-time arena, the situation is gradually changing. This is best illustrated by the growing number of embedded Smalltalk applications. When Smalltalk emerged from the laboratories of Xerox PARC ten years ago and started the OO revolution, it was a large, slow, single-user, workstation-bound environment. Today, with modern packaging technology, Smalltalk applications can be placed in ROM and can operate with as little as 50 kbytes of DRAM.

Team programming environments let multiuser Smalltalk teams develop complex applications in a disciplined, version-controlled and configuration-managed environment. Remote interfaces, integrated network support, embedded Smalltalk requiring no external I/O devices, and multiprocessor Smalltalk have all been demonstrated. Expert system toolkits are becoming available which provide the components needed to build embedded knowledge-based applications.

Examples of successful embedded Smalltalk applications include:

- An integrated wafer fabrication facility being developed by Texas Instruments,
- A radar receiver built by the Canadian Defence Research Establishment,
- A network analyzer being marketed by Hewlett-Packard,
- A network management system for process control developed by Allen-Bradley,
- The Tektronix TDS540 500-MHz oscilloscope, and
- An automatic test and evaluation system for printed circuit boards developed by NCR.

Looking ahead, it seems clear that as the technology continues to mature, the productivity and quality advantages of OOT will be increasingly attractive to real-time developers.

Brian M. Barry, vice-president of R&D, Object Technology International, Ottawa, Ontario

cation domain that a company is working in—in almost the same way as a set of proprietary, custom-designed parts.

Stumbling blocks to recycling

Creating truly reusable classes, however, is only half the battle. BNR's Gullekson notes that "organizationally and culturally, very few organizations are set up for reuse." Two things have to happen for an organization to effectively reuse its code. First, there has to be a group in the company that's in charge of the base components, admitting them to the class libraries and making people aware of their existence and what they do. "Otherwise," says Gullekson, "you'll have everybody doing their own little project-specific things, but nobody will be focusing on a common set."

The second requirement is cultural. The reward and recognition system in most companies is biased toward people producing many lines of code, rather than being based on reusing code. A better metric for an object-oriented operation is to ask how much existing code was reused. In the same way that logic designers can fashion new ICs with existing libraries of elements and not have to worry about device physics, software designers need to be rewarded for their creativity in combining objects to build new things. "From a software background, that's a pretty new concept," says Gullekson.

Tools for large projects

The fundamental problem with large projects, according to Rational's Booch, is complexity. "In such cases managerial issues kick in. In small systems, you don't worry about configuration management and version control. At the big end, you live and die by them."

Booch says that the requirements for success are notation, process and tools. Notation, which usually represents a design methodology, provides a common language for management and engineering across the different phases and levels of a project. The process defines the steps needed to create the product and explains how to measure the products created. Finally, the tools must support both the notation and the process.

Rational, which offers a range of software engineering tools, also has an object-oriented analysis and design environment called Rational Rose. Rose uses an object-oriented notation developed by Booch which is seamlessly applicable to both the analysis and design stages of development—especially important given the iterative nature of a designer's activity when moving back and forth between analysis modeling and design implementation in the course of refining the design.

Rose includes browsers, analysis and design checkers, document generators, forward and reverse engineering tools, animation tools, and hooks to other tools, all of which communicate via a common object-oriented data repository. You work with the system via an OSF Motif/X Windows graphical user interface.

"In small systems, you don't worry about configuration management and version control. At the big end, you live and die by them."

—Grady Booch, Rational

The browsers, working within the data repository, are able to help you search for appropriate classes and components, not only within the bounds of the current application, but also across project boundaries. Rational also supplies a design library of ready-made, extensible components, called Booch components, which can quickly be integrated into Rose to serve as the basis for developing domain-specific class libraries. These component are available in a C++ version now, with an Ada version to follow.

Building up class libraries and application components or even whole applications that can be reused is increasingly recognized as the way to get productivity out of object-oriented technology. A CASE tool called ObjectMaker from Mark V Systems (Encino, CA) lets you select from some 20 design methods and notations to produce objects and applications which can then be used to automatically generate Ada or C code. ObjectMaker also has a reverse engineering capability that lets you analyze the structure of existing code so it can be assigned graphic diagrams that describe its functions.

In creating designs with ObjectMaker, you can browse in graphical libraries, looking not only for classes and objects called for in the design but also for complete applications that might be used in a current project. An application that must be modified in some way to meet the needs of such a project can be traversed in terms of the objects that compose it using this software. You can then identify those objects that need to be modified to fit the application to current needs.

"ObjectMaker, in the absence of existing classes, gives you a general-purpose design tool and the ability to do code generation," says Mark V's marketing manger, Mo Bjornestad, "but the graphics can be pre-existing and already linked to completed code as well." An ObjectMaker design will automatically pull in the code associated with pre-existing graphic objects and will then let you generate code for those objects that don't exist yet.

On the CASE

Cadre Technologies is now adding object-oriented analysis and design to its Teamwork line of CASE tools. The analysis tool is used to construct a representation of a real-time system, generating system specifications that focus on objects and their relationships. An intelligent editing system consisting of six types of editors lets you graphically produce a complete requirements document that's automatically checked for consistency and accuracy.

An entity relationship diagram editor models the information structure among objects and their attributes. A state transition diagram editor models the life cycle of each object in the entity relationship diagram. The models show the states in the life cycle and the processes that occur in each state. A data flow diagram editor shows the processing for each state, and an object communication model describes the communication between objects. A matrix editor works with state matrices, which are tabular representations of state transition diagrams. The process specification editor lets you enter textual descriptions of how objects transform inputs into outputs. And finally, the data dictionary entry editor lets you define the attribute types and definitions for objects and the relationships, transitions,

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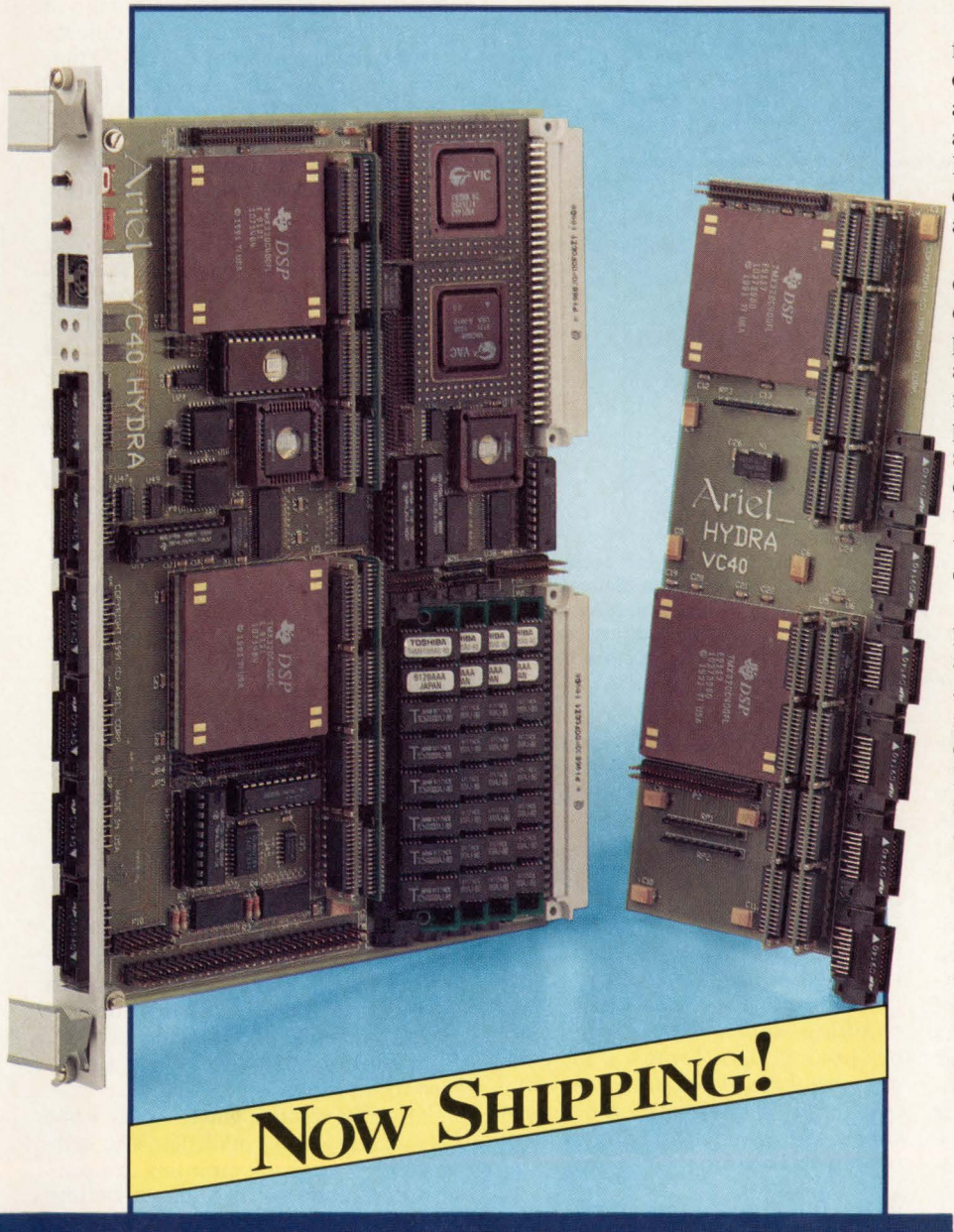

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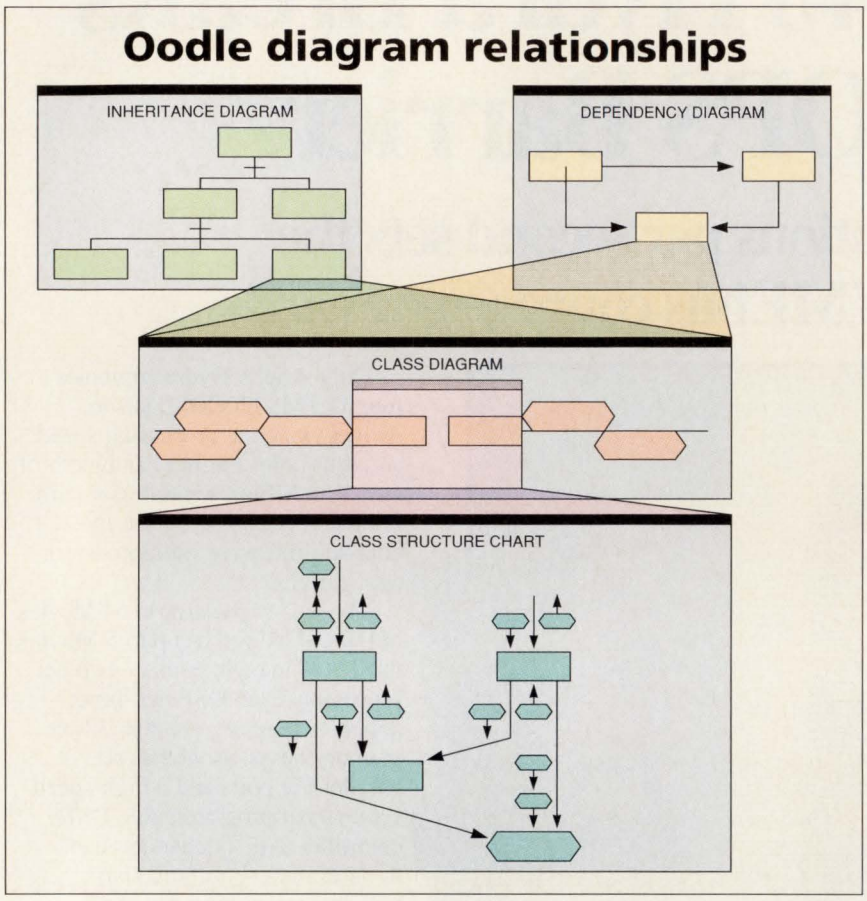

Cadre's Oodle provides diagrams that let you view classes from four perspectives, in terms of: 1) their inheritance relationships to other classes (inheritance diagram), 2) client-server relationships between classes—that is, who invokes whom (dependency diagram), 3) the external view of a single class, such as inputs, outputs and behavior (class diagram), and 4) the internal structure of a class (class structure chart). The diagram shows how the various levels internest.

stores, and data flow that each object represents.

Cadre's object-oriented design (OOD) tool, called Teamwork/OOD, is the programming environment that takes the system specifications through to code. It uses Cadre's object-oriented design language environment (Oodle), a form of notation that supports the iterative, recursive design that's characteristic of object-oriented methods. Oodle lets you view classes in terms of their external specifications (such as inputs, methods and outputs), their position with regard to inheritance from other classes and their dependency (for example, client-server relationships) on other classes. The notation also lets you view the internal structure chart of a class, which shows the flow of control and the structure of the code.

The Teamwork/OOD tool includes a C++ source builder that analyzes design diagrams and produces C++ code frames that can be compiled. True to the iterative nature of object-oriented design, the tool includes a C++ capture utility that lets you edit the output of the source builder and reinject information back into the design. Such a dual-function tool is necessary, according to Cadre's Hazard, "because you need something that lets you navigate around C++ code while you're thinking about objects. In object-oriented design, there's a lot going on behind your back, like overriding, overloading, streams, and inheritance, and you need a support infrastructure behind you."

The Smalltalk alternative

Object-oriented design tools aren't limited to C++, however. There's growing support for Smalltalk, a language that was conceived from the ground up to be object-oriented. As a result, Smalltalk successfully enforces an object-oriented programming methodology.

"Smalltalk really consists of a core plus a lot of components you add," says Brian Barry, vice-president of research and development for Object Technology International (OTI—Ottawa, Ontario). Object Technology has adapted the Smalltalk V language licensed from Digitalk (San Diego, CA) for real-time applications.

OTI's real-time product, Envy/Smalltalk, consists of the Smalltalk virtual machine, a kind of interpreter and a number of objects needed for the system to run. "Then everything else in the environment is added," says Barry. OTI has added objects to deal with problems specific to real-time (such as the abilities to handle interrupts), to interface to a real-time operating system and to place a Smalltalk image in ROM. In addition, there are mechanisms to see that certain Smalltalk operations such as garbage collection (the reclaiming of allocated memory space) doesn't take place when user primitives are executing. This ensures deterministic behavior for real-time applications.

Envy/Smalltalk can be integrated with OTI's second major product, Envy/Developer, to form a multiuser software engineering environment. Envy/Developer is aimed at larger projects and integrates version control and configuration management with the Smalltalk programming environment. It includes a tool called Envy/Manager, which provides an intelligent view of classes from the point of view of the application. This configuration management tool can keep track of different development streams, platform dependencies and software releases. By knowing which platform it's targeted for, it can put together a configuration from the proper modules in the library. So you might write an application and then set up different configurations of that application for different hardware or OS target environments.

Envy/Developer works with what OTI's Barry calls modules; the software knows which modules are part of other modules and which belong together for a given target application. Barry says that modules form the truly reusable components of the system. "A class by itself really doesn't do anything for you," he says, "because you have to instantiate a class and make it into an object. It usually takes several clas-

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ses working together to do something interesting."

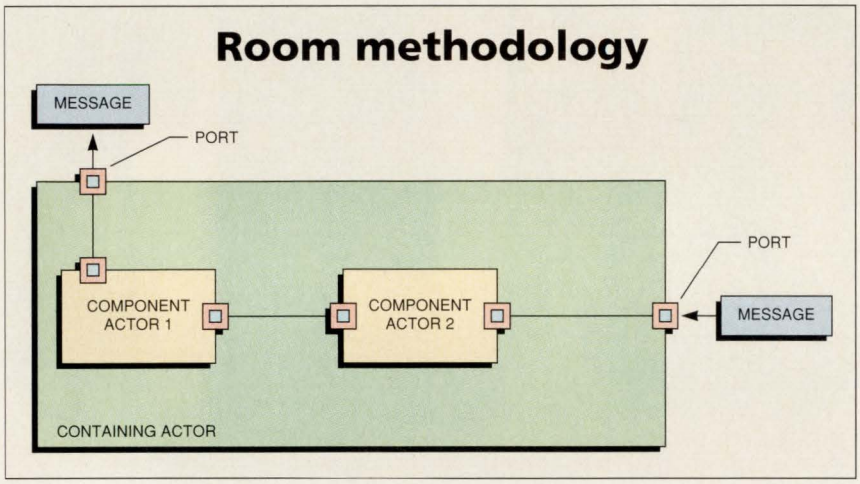
The Envy/Developer tool, then, helps design teams get beyond the class browsing level so they can look at functions as groups of classes. "This," says Barry, "is the thing that then becomes reusable and modular, because it actually provides services—you kick it and you get an answer back."

"Kicking it and getting an answer back" is one of the advantages of operating at a higher level of abstraction than source code. This makes it easier to prototype object-oriented applications at the architectural level and play "what-if" games before committing to a design.

The ObjectTime object-oriented CASE tool from Bell Northern Research integrates the ability to diagram system requirements in terms of objects with the capability to execute the model at the architectural level. ObjectTime uses a methodology called Room (real-time object-oriented modeling), which is consistent over all levels of the design.

Room models a system in three dimensions: structure, or the graphical decomposition of the system into encapsulated objects; behavior, graphically represented by hierarchical state machines; and inheritance, which provides a basis for abstraction and reuse. With inheritance, objects can be derived from other objects already defined by merely specifying their distinguishing characteristics. For example, a tiger inherits all the attributes of "cat," but adds the distinguishing properties of size and stripes.

Objects in the Room methodology are called "actors"; they have behaviors (state machines) and communicate via defined protocols called ports. Multiple actors can be connected and contained within a larger actor, which communicates with the outside world via its own ports and is also linked to the actors within. The Room system, then, embodies two of the major attributes of good object-oriented discipline: encapsulation and inheritance.



The real-time object-oriented modeling (Room) methodology, which is incorporated in Bell Northern Research's ObjectTime tool, conceives of objects as "actors" that send messages to each other via communication protocols called ports. They act on data via internal methods. Actors can be bound together and contained within larger actors, whose methods are externally defined.

ObjectTime is written in Smalltalk 80, a version of Smalltalk from Parc Place Systems (Mountain View, CA). Using the tool's simplified notation, you can define objects and their internal state machines and have the system compile the graphical design content into Smalltalk 80; then you can run it on your workstation.

The ability to define hierarchical state machines means that you can run the design at the level of abstraction you desire. You can then further refine the design by defining the state machines that make up higher levels of abstraction. At the lowest level of detail, you can specify operation in C++ or ObjectTime's rapid prototyping language (RPL). RPL will compile to Smalltalk, while C++ output lets you reference other C++ classes developed outside the tool. But BNR's Gullekson notes that "programming languages are used to express detail, not design. At the language level, it would be too much trouble to prototype a number of design alternatives."

Given the ability to model at a very abstract level—or, indeed, at any level—ObjectTime doesn't lock the development process into distinct phases as does the classic "waterfall model" so beloved by CASE theorists and so scorned by most real developers. (Its components are analysis, design, implementation, testing, and maintenance.)

Rather, ObjectTime lets you move freely back and forth between the analysis stage, where you try to gain comprehension of the problem through modeling, design and implementation. Design and implementation really use the same concepts as analysis, but with more emphasis on object decomposition. Components that were modeled on an abstract level in analysis are fleshed out in later stages by having their internal state machines defined in detail. These components are in turn reused in another round of analysis to make sure the implementation is meeting requirements. Eventually, the analysis model and design implementation should converge in the completed product.

OOD in-the-small

The promise that object-oriented development holds for managing the complexity of large systems, providing for the reuse of code and letting non-programming experts build systems based on their understanding has already been realized in several application areas on a small scale. These small-scale—and often graphically oriented—"application builders" aren't as semantically rich in general as are programming languages. But they do let users within a bounded application domain rapidly assemble, test and utilize applications in the terminology and metaphors of their own disciplines—such as instrumentation, process control or more generalized real-time control.

National Instruments (Austin, TX), for example, is a pioneer in using computers to control and coordinate the use of multiple instruments with personal computers, primarily the Apple Macintosh. National Instruments today offers a family of products called LabView for the Macintosh, the PC with MS-Windows and Sun workstations. LabView lets scientists and engineers program entirely in terms of

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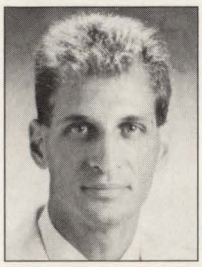
Real-time spreadsheet speeds R&D projects



Southwest Research Institute (SwRI) has patented an active suspension system that controls pumps powering hydropneumatic suspension struts used to support vehicles. The development process was greatly facilitated by using RTware's ControlCalc, a multitasking spreadsheet that lets you quickly design, test and implement a variety of control and acquisition schemes on Microware's OS-9.

The computer chosen for the project was a 16-MHz Motorola 68020 with 1.5 Mbytes of memory on-board, a 68881 FPU and a SCSI controller with 1 Mbyte of RAM. I/O was performed with IndustryPacks. All this hardware was placed in a VMEbus chassis mounted in the vehicle.

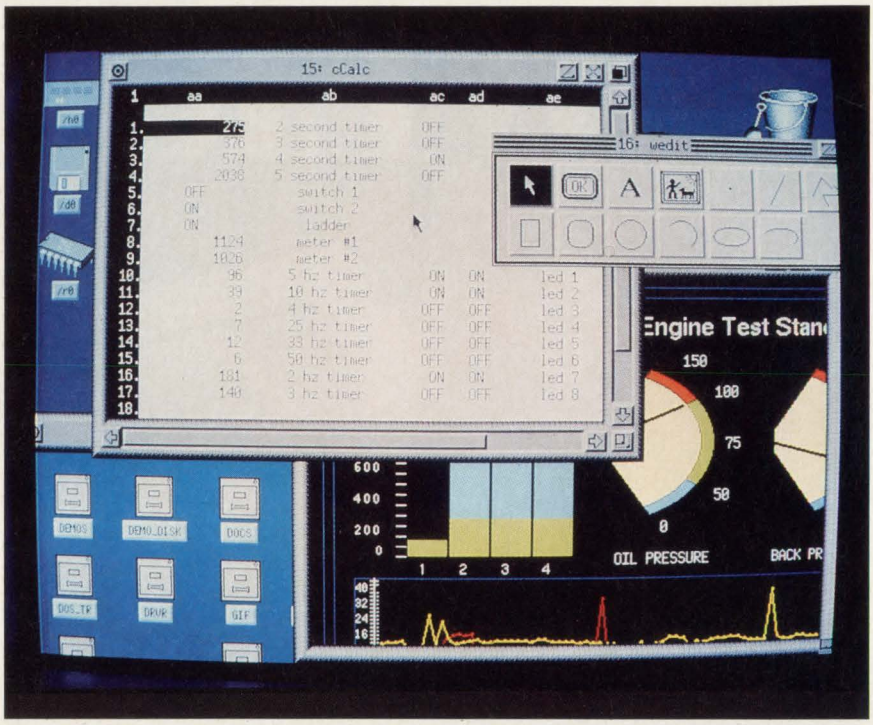
Spreadsheet helped simulation

With ControlCalc, the use of multiple pages of the spreadsheet for both multitasking and object design let parts of the system be prepared and integrated into the whole template when completed. The spreadsheet's ability to provide memory I/O for simulation permitted the software template to be tested without requiring hardware.

The control algorithm was broken into several parts, corresponding to pages in the spreadsheet. The sections included sensor input and filtering, control output and filtering, position control, pitch and roll control, skyhook damper control, data acquisition, and operator interface (for example, constant adjustments and display of important variables).

ControlCalc eased the design effort by letting SwRI treat each page as a black box, providing output to and taking input from other pages. If a section of the template wasn't completed, the page could be programmed to provide fixed values, run through an array of values, or produce outputs as the result of a simple function. As each page was completed, it could then be incorporated into the overall template by simply replacing the dummy page.

Since ControlCalc let us add functions, either by coding and linking them to ControlCalc libraries or by coding them as software interrupts, we were able to add a timer call to time each page. Our algorithm calculated almost everything as floating-point numbers. We measured approximately 20,000 Flops per algorithm cycle. Calculating the time for the various operations, as well as the housekeeping performed by the spreadsheet, gave us a theoretical throughput of 34 ms, which was in fact what we measured.



Graphic screens modeling plants, machines or other systems under control can be attached to real-time programs created with RTware's ControlCalc. Shown on this screen is a spreadsheet-like program that underlies a graphical user interface (GUI). On the GUI, animated objects are mapped to cells in the spreadsheet containing output values. Each page of the spreadsheet represents a task which is assigned a priority and can be invoked by interrupts. Programmers can think of pages as reusable objects.

Improving performance

Two approaches were considered to improve performance, should future control systems require faster loop times. The first was simply to upgrade the hardware. Doubling the PU/FPU speed would nearly double performance. The second used built-in capabilities of ControlCalc. By scaling all of the input operations into the integer range and then converting them back upon output, all of the math could be performed by the integer math unit. This was calculated to provide a performance of approximately 7 to 9 ms per control loop. This technique is currently being reviewed for testing.

ControlCalc considers each cell to have a data type that is wholly dependent on the type of calculation being performed. This affords the developer a simple way to change from floating-point to integer math—or to ignore the details of variable type altogether. This capability facilitates the testing of ideas, making users more productive.

By hooking the spreadsheet to a graphical interface, we're able to design screens that clearly show our test cell operators what's going on with each aspect of the test or data being gathered. ControlCalc supports a wide variety of gadgets that can insulate an operator from the test template. Graphics, along with the ability to page templates together, offers a flexible approach to testing, data acquisition and control.

Josef Zeevi, research engineer, Southwest Research Institute, San Antonio, TX

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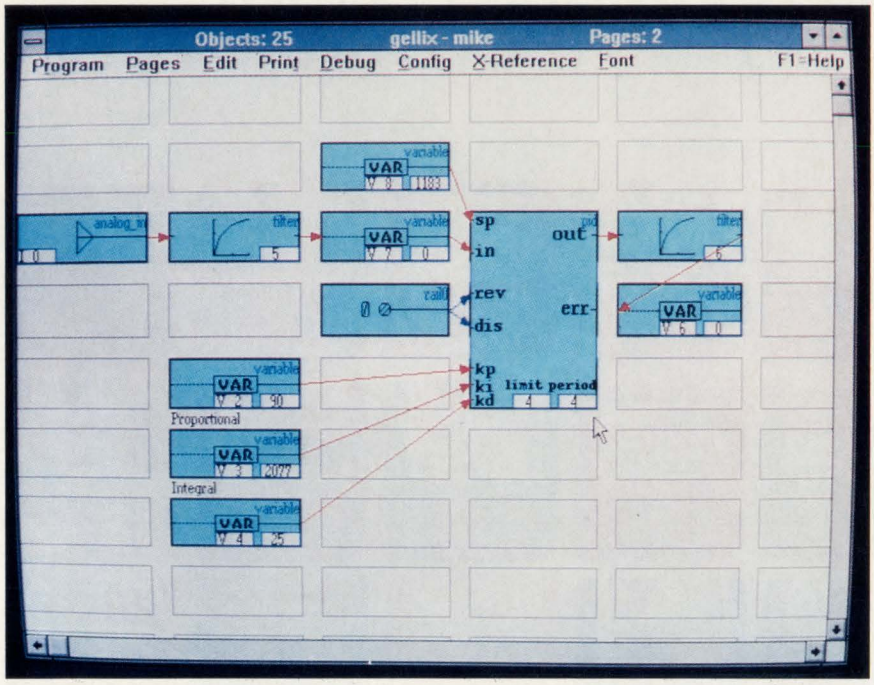
graphic objects, building software modules called virtual instruments (VIs). Virtual instruments can, in turn, be represented as icons and used as building blocks for more complex VIs.

To build a VI, you first define a front panel by selecting typical front-panel items from a menu. A strip chart, CRT display, slider switches, knobs, and indicator lights correspond to classes in the object-oriented sense. They become objects when you instantiate them by placing them on the front panel and giving them values such as scale, color, a range (for example, 0-200 V), or a size.



Engineers can visually program programmable logic controllers (PLCs) using Gello by Event Technologies. You assemble objects representing familiar things such as contacts, relays, coils, and logic gates on the screen. A screen of such objects can define a given function. The function can then be represented as a single object icon and saved as a separate reusable object. Programs created with the Gellix editor on a PC or workstation are downloaded and run on the Gello engine in the target environment.

The second step in programming a VI is performed in the diagram window by wiring together icons representing function and control objects. You literally "wire" them together using a cursor that looks like a little spool of wire. The diagram window contains symbols representing connections to the objects in the front panel.

Functions can be as simple as a numeric constant or as complex as a finite impulse response filter. Do you need to use some equation not contained in the menu? Just pop up the formula node, attach symbols representing the input terms and the output of the equation, write the equation inside the node, and wire it up.

Also included in the LabView graphical programming environment are programming structures such as sequence structures that let you define groups of operations that must happen in a specific order. Loops are available too, letting you enclose a set of objects within a graphic loop. You then assign a time constant so the loop—data sampling, for example—repeats every so many milliseconds. The data flow along the "wires" that connect objects determines the sequence of operation within a structure. For each object supplied with LabView, there's a help window that displays the object's inputs and outputs and describes its function.

"Engineers and scientists could really care less about how we implemented LabView," says Jack Barber, product marketing manager for National Instruments. "All they really know is it seems to match the way they think about their problems. LabView addresses people who are looking for an alternative to C and Basic."

LabView can be used to create VIs entirely within the computer by means of a family of plug-in data acquisition boards which are also treated as objects by the programming environment. The software can also be used to control multiple physical instruments over a GPIB or VXI bus. In such cases, LabView takes advantage of the high signal bandwidth and processing power internal to the instruments and turns its own power on the task of analyzing the data they measure.

In addition, LabView can output via the add-on boards and so can be used in some control applications where high speed isn't a requirement. Graphic images of physical plants can be imported and linked to VIs as well. Recently NASA engineers used an animated image of the space shuttle Columbia in LabView, which was in turn connected to the shuttle's internal sensors to track down a hydrogen leak that had delayed the launch. "They used it because they were able to put a system together so quickly," says Barber.

PLCs like Gello

Quickly putting control systems together is the forte of Gello by Event Technologies (ETI—Indianapolis, IN). Gello (Graphically Enhanced Ladder LOgic) is specifically aimed at simplifying the task of programming programmable logic controllers (PLCs). PLCs are typically programmed with ladder logic, which is based on techniques for wiring electromechanical relays. Basic objects in Gello represent relays and contacts, counters, timers, inverters, and AND and OR gates. In addition, there are analog inputs and bit operations, to name a few.

Gello consists of two parts. The Gellix editor runs on a PC under MS-Windows or on a Unix workstation under X Windows. The Gello engine can run on a variety of target processors, including the 80X86 and 680X0, and is being shipped with a number of single-board computers from companies including ProLog (Monterey, CA) and Heurikon (Madison, WI). The Gello engine actually contains the basic set of objects supplied with the system. The programs written with the Gellix editor define the parameters and the data flow between the objects. In a sense, the programs instantiate what are more properly called classes within the engine into the actual programming objects.

The Gellix editor lets you select rectangular objects from a menu

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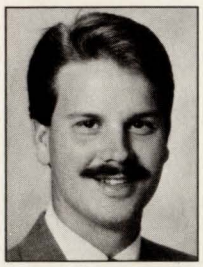
The need for application-specific software tools



Over the years, personal computers have redefined the way people approach and solve their problems. The power and performance of computers make them much more efficient tools for solving problems than the old way of tackling them by hand. Application software is key to problem-solving, however. If the available software is too primitive or too far removed from the user's application area, computerization can create bottlenecks and reduce productivity.

Programming with pictures

Everyday experience reveals that people are visually oriented; they often draw pictures or diagrams to communicate ideas and concepts to others. It's no surprise, then, that graphical application software is easier to learn and more accessible to many non-computer experts. Graphical software lets those who otherwise don't have the time, education or skill to learn programming using conventional text languages develop their own programming systems. Giving non-programmers the ability to program is especially important today, since the need for software is fast outstripping the capacity of the relatively few programmers available.

The advantages of graphical application software go far beyond the elimination of syntactical knowledge required to program in a conventional language. Text-based programming is an inherently linear process and forces humans to think and express their ideas in terms constrained by the architecture of a computer. With graphical software the users conceptualize applications in their own terms. Users can easily examine a graphical depiction for relevant features and complex relationships that would be hidden in the code of a text-based program.

The challenge to the software developer is to do more than simply paste a graphical user interface on top of a software system. He or she must actually produce a high-level software layer that insulates the end user from the programming details of the underlying computer architecture. The developer must find a computational model, a programming metaphor and building blocks that match the user and the application area. If this is done correctly, the user interacts with the computer, not as a bit-crunching machine, but as a more intuitive tool for solving the application problem.

First, the software developer should consider the end users: how do they think about their problems, how do they conceptualize their solutions and what tools do they use to implement solutions? By supplying familiar tools and terminology, the software package serves as a productivity enhancement rather than a hindrance to the application development.

Tools of the trade

Probably the most famous and widely used application-specific tool is the spreadsheet. The average businessperson isn't a computer programmer, but still needs to use the computer for its computational power. Before the spreadsheet, the businessperson hired a professional programmer who used Cobol to write cumbersome text-based programs. The spreadsheet delivered an application-specific tool that matched the way the businessperson thought about and conceptualized the application—in rows and columns of numbers.

Another well-known application-specific tool is LabView from National Instruments, which is used to automate instrumentation applications. Although engineers and scientists are very technically minded, they aren't necessarily computer scientists; application-specific tools that remove the tedious programming details are welcome to them. Realizing that test and measurement programs are like instruments, except that the user interacts with a terminal rather than a front panel, National Instruments devised the virtual instrument (VI) concept.

By mimicking the proven interface provided by hardware instrumentation, the front panels of VIs create a familiar environment giving the user intuitive control of the software system. LabView also offers an innovative block diagram programming methodology—a natural design notation for engineers who think about and solve their problems with flow charts and block diagrams. Finally, LabView's modular approach, in which the user connects VIs together to build more sophisticated systems, matches the way technicians connect laboratory or industrial equipment.

The payoff

Are high-level, domain-specific programming environments effective? Judging from the popularity of existing application-specific products such as LabView, the answer is yes. Such products have gathered enthusiastic and loyal followings. Users have reported that not only can they solve their problems more rapidly, but that programming can actually be fun.

While implementing application-specific software tools calls for a significant investment to research the needs of end users, the result can be tools that dramatically increase the productivity of end users while also reducing their frustration. Such products can be very successful, as well as redefining how users approach and solve their problems.

Jack Barber, LabView product marketing manager, National Instruments, Austin, TX

and place them on a screen grid. Each object has a name, an icon, up to three inputs, an output that can be either analog or binary, and up to two variable options. When you click the mouse on one of the variable options, a window opens requesting the definition of the variable. Objects are connected by drawing lines between them on the page.

The hierarchical nature of Gello lies in the fact that a page that contains objects can itself be collapsed into an object icon, which can in turn be used on the next higher page in the design hierarchy. The user can move down through the design, opening objects to view the other objects that make them up. Pages can be saved in a library for reuse in other designs.

For those who need to create new objects at the Gello engine level, Event Technologies provides a developer's kit. Creating a new object means developing a function that will then be linked into the Gello

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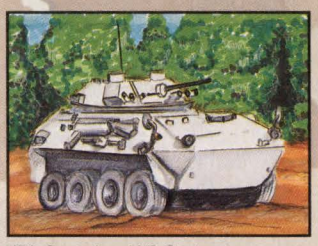
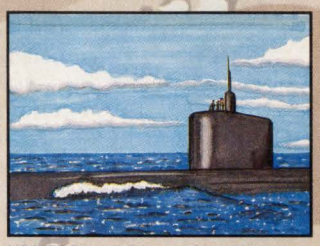


NDI: Control and I/O Systems



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NDI: Gun Control/Auto-Loader

engine and associated with an icon (created by a paint program) in the Gellix editor.

"We're an object-oriented language," says ETI's vice-president of marketing, William Lydon, "but we're bounded because we're for industrial and process control applications." As PLCs are increasingly programmed via front-end computers for more complex operations, there's a need to bring the long-established knowledge of the process engineers along. "A guy who understands pneumatic and electrical diagramming that he's been using for 70 years can take his mouse, draw on a screen like a piece of paper, download it, and he's created an application," says Lydon.

Flexibility vs specialization

While object-oriented environments for real time gain competitive advantage by intentionally targeting the boundaries of an application domain, the lure of remaining flexible is also enticing. The spreadsheet is a general-purpose metaphor from the business domain that's now being used in the real-time control domain as a kind of canvas upon which designers can paint their process-control applications. RTware (Durham, NC) has applied the spreadsheet model to real-time programming with a product called ControlCalc.

"In a fairly simple sense, all spreadsheets are object-oriented," says Laurent Meilleur, vice-president for sales and marketing for RTware, "in as much as each cell and each sheet contains its own data and its own definition of equations." There are different classes of cells, including types such as expression, macro, display, and setpoint cells, even ladder logic diagrams. But Meilleur admits, "You're not able to add new objects or create higher classes of objects. But in its operation, it's object-oriented."

Pages created for one application can be saved in libraries and reused for others. During design prototyping, you can set up dummy pages to supply data that will be generated later by the finished application, or you can map I/O cells to data files rather than the final hardware ports.

ControlCalc is organized like a spreadsheet, with cells that contain expressions, data, text, or references to other cells or screen display objects. Each page, which can have up to 256 cells, is considered a task in a real-time application, and so each page is assigned a priority. ControlCalc runs by scanning each page from the upper left to bottom right and executing those cells that contain expressions. Interrupts that invoke a higher-priority task (or page) suspend scanning of the interrupted page until the page invoked by the interrupt has executed.

ControlCalc runs under the OS/9000 real-time operating system from Microware (Des Moines, IA). It also incorporates a graphic mapping window that lets you map the values in a cell to graphic objects on the screen, such as gauges, dials and strip charts. As with LabView, you can create your own models of plants or other objects under control, and you can tie limited animations to changing values within cells.

"Gluing a bunch of things together in a set of sequences to make something work" is Applied's Jensen's somewhat irreverent summary of what object-oriented technology is all about. Of course, it requires formal definition and standards—and, of course, not all systems calling themselves object-oriented conform to the formal definition of that term. ■

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Post Script

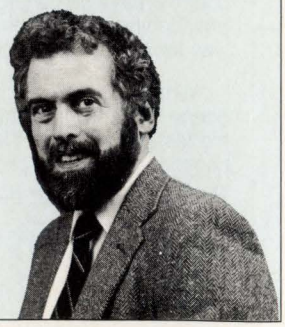
Object-oriented software development is a response to a need—a need for less confusion, for less repetitious work—and is a natural outgrowth of the human mind's tendency to think in visual metaphors. That's why there is such emphasis on graphical representation in the field.

But object-oriented technology also has implications for the future role of the programmer. People who write, compile and debug code have been intimately involved in the engineering of all manner of specialized products. Studies of software engineering have shown that application expertise is more important to the success of a project than programming expertise. The job of the programmer, as we move ever more deeply into object-oriented technology, will be to create application-specific tools that nonprogrammer engineers and scientists can use to solve their problems.

This is not to suggest that "true" computer programmers will become a dying breed. But the emphasis of their job activity will shift. The dialogue between the expert who understands his or her application needs and the programmer who must translate those needs into code will diminish. Instead, programmers will identify the architectural needs of application domains and supply tools in the form of class libraries and tool environments.

Of course, the need to get down deep into the code will never really go away. Especially in real-time applications, there's always something that needs tweaking or that doesn't fit quite right and requires a kind of digital Mr. Goodwrench to come in and fix it.

Tom Williams



Borrowing from earlier design helps speed Microflash to market

The Holometrix team from left to right: Tony O'Leary, product development engineer; Helen Shaw, sales engineer; Zbyszek Brzezinski, senior software engineer; Joe Chervenak, senior scientist; John Morin, product development engineer; David Haines, director of sales and marketing. In the center of the photo is the Thermaflash 2200. Borrowing several design ideas from the Thermaflash, Holometrix designers were able to bring their lower-cost Microflash product to market in just over six months.

There's a growing awareness that the development and exploitation of new materials are critical to maintaining competitiveness. As a result, the demand for instruments which measure the physical properties of such materials continues to grow. With this in mind, in 1989 Holometrix (Bedford, MA) developed the Thermaflash 2200, an instrument that measures the thermal properties of materials at temperatures of up to 2000°C.

The company sold several systems at a price of over $150,000, but feedback from potential customers revealed that a lower-cost instrument would have a much broader appeal. "We've had customers in the electronics industry who've been looking for a low-temperature unit," says Helen Shaw, sales engineer at Holometrix, "but they're not prepared to pay over $100,000 for a capability they don't need."

Hoping to capitalize on this demand, Holometrix began thinking about a benchtop thermal analysis system, with the base system priced under $40,000. The company envisioned a system that, like Thermaflash, could measure the diffusivity, specific heat and conductivity of materials, but one that operated without the high-temperature capability. Designers were given six months to do the basic design of the follow-on

Jeffrey Child, Associate Editor

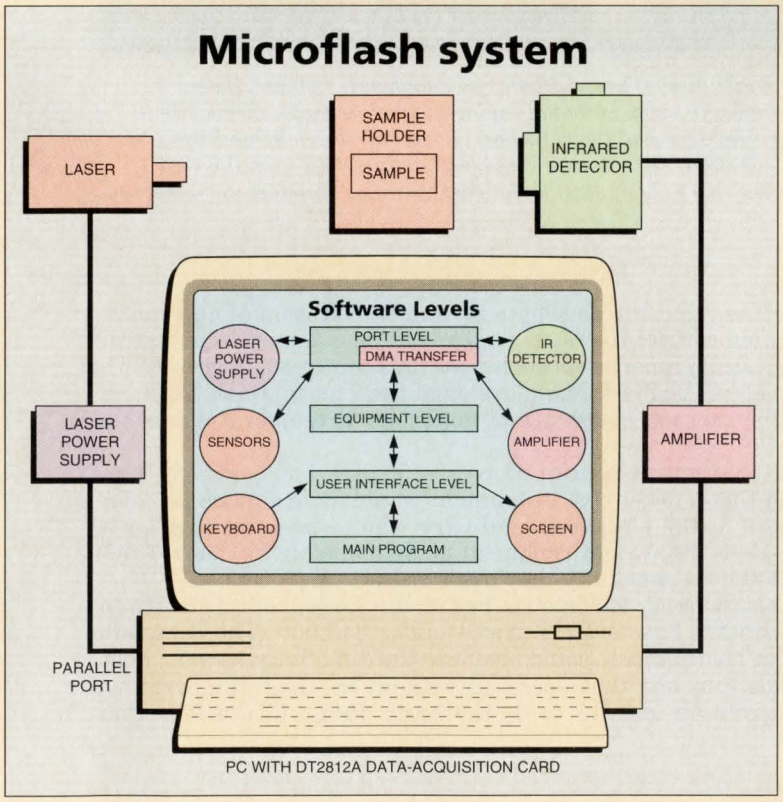
Microflash: how it works

The Microflash system was designed to meet the need for a low-cost laser flash instrument that measures the diffusivity and specific heat of materials at room temperature. Designers at Holometrix borrowed many elements from their earlier, more expensive Thermaflash 2200, a system that measures material properties at extremely high temperatures, to create Microflash, a benchtop instrument that incorporates an external personal computer.

To operate Microflash, a dime-sized, disk-shaped sample of the material to be tested is placed in the sample holder. The sample's thickness, mass and volume are entered into the PC, along with the test temperatures. The program is run, and when the test temperature is reached, the laser fires a single pulse which strikes one side of the sample. The infrared detector monitors the temperature rise of the back surface of the sample and this data results in a curve. The points of the curve are then matched to a set of theoretical curves stored in the PC. The software basically goes through a curve-fitting process and picks out the theoretical curve that is appropriate. The shape of that curve determines the diffusivity of the sample.

To determine specific heat of the sample, the absolute temperature rise of the sample is analyzed. This works on the principle of comparing the temperature rise of the test material to a material with a known specific heat. The reference material must be similar to the test material—for example, alumina is a good reference material for ceramic materials and molybdenum for metals. Assuming that the test and reference samples absorb roughly the same amount of energy, the specific heat of the sample is calculated. The mass of both samples and the specific heat of the reference material are all known values. By comparing the temperature rises of the two samples, the specific heat of the test sample is easily calculated.

Once the sample is set up and the test parameters entered, the instrument runs by itself. At room temperature, a single test takes only a few seconds.



product, called Microflash, knowing that special options would be added later to serve more specialized customer needs.

Scaling down

The basic design philosophy for Microflash was to create a scaled-down, lower-cost version of the Thermaflash 2200. While the Thermaflash could do measurements over a wide range of temperatures, the Microflash was optimized specifically for moderate and room temperatures. Cutting out the high-temperature capability meant designers could eliminate a lot of the expensive components used in the earlier system and optimize the architecture for room-temperature measurement.

For Thermaflash's high-temperature measurements, the testing sample needed to be held in a furnace. But since the Microflash would work at room temperatures, the equipment's infrared (IR) detector could be closer to the sample. "We were trying to optimize the geometry of the system to collect a lot more light at a higher signal-to-noise ratio," says Joe Chervenak, senior scientist. "We wanted to optimize the detector, because at room temperature, the IR wavelengths of the signal picked up off the back of the sample are longer." As a result, the indium-antimonide IR detector used in the previous design was replaced by a mercury-cadmium-telluride IR detector.

Perhaps the most visible change in the Microflash design was the replacement of an embedded computer with a personal computer. While the Thermaflash system was housed in one large enclosure, the Microflash system consists of a dedicated PC with the other components—laser, sample holder, IR detector, amplifier—outside on the bench. Lower cost of the PC versus an embedded system is the main reason. "The cost of the computer is negligible in the cost of the system—1 percent or 2 percent at most," says John Morin, product development engineer. "We were using 286-based PCs at first, but we're talking about using 386-based PCs now, just because they're so cheap."

Buying instead of building

Most of the data-acquisition and control operations of the Microflash system are handled by a single board. Given the resources, staff

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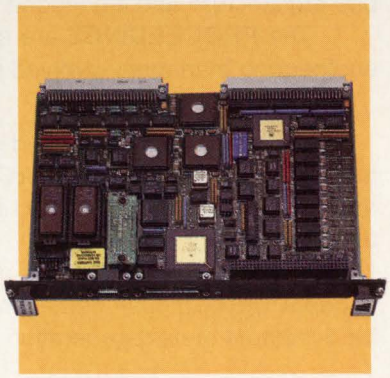

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and available time, designing a custom board was out of the question. So, Morin went searching for an off-the-shelf card that would meet the appropriate speed, resolution and cost requirements. The Thermaflash system used a 16-bit, 100-kHz data-acquisition card from Data Translation (Marlborough, MA) and a separate card for digital I/O. For the Microflash, Morin decided a 12-bit, 100-kHz card would be sufficient. After considering cards from Keithly-Metrabyte and National Instruments, he settled on the DT2812A, a 12-bit, 100-kHz card also from Data Translation.

With OEM discounts, the board is priced at $715. "The cost was probably the deciding factor," says Morin. "It would be very difficult to justify much of an effort to design something custom while there are standard products available at the same cost." The fact that the DT2812A had 16 digital I/O channels was also a plus, eliminating the need for a separate digital I/O card.

Another major system component of the Microflash system is the amplifier, designed and built by an outside contractor to Holometrix's specifications. Using output signals from the IR detector, the amplifier reads the background temperature before the laser is fired. It then zeros that value, so that when the laser's fired, you get a signal that's referenced to the background signal. An analog subsystem, the amplifier is made up of a sample-and-hold and several op amps. Because the sensitivity of the IR detector changes with background temperature, the amplifier has three preamps, each for different beam ranges. The gain of each is set digitally.

While the amplifier design didn't change from the earlier machine, the means of controlling it did. The Thermaflash system had a separate card with 48 digital I/O channels. Besides setting the amplifier gain, this card was used to switch all the controls for the furnace, such as the vacuum system, the input sensors for water shutoff and the aperture. For Microflash, which has no furnace, there's enough digital I/O right on the DT2812A data-acquisition card. The device uses the 8-bit outputs on the data-acquisition card to set the amplifier gain.

Once the gain is set, the DT2812A card sets up and executes a DMA transfer. The laser then fires. The scanning frequency on the DT2812A is set based on the amount of time you want to scan the back of the sample. The card acquires 4000 points of data, which determines the frequency and the total scan time.

A sensor triggers an interrupt when it detects that the laser has fired. The laser's charging and firing is controlled by the PC via a parallel port connected to the laser power supply.

Aside from monitoring and controlling the amplifier and laser, the DT2812A has a number of other data-acquisition and control responsibilities. For example, the temperature is read through one of the analog-to-digital channels on the data-acquisition card.

Software design

The original plan for the Microflash system called for a Microsoft Win-

dows-based software implementation. But given the time-to-market pressure, the team decided that a Windows-based software design would take too long to complete. Furthermore, the overall design philosophy was to reuse whatever could be used from the Thermaflash. It was decided, therefore, to write the software under DOS and leave Windows as a future upgrade. "We'll definitely look at doing that [a Windows implementation] at a later date," says Zbyszek Brzezinski, senior software engineer. "There's a perception these days that software is no good unless there's a mouse. We would have written the original program under Windows if Windows Version 3.0 had been available at that time [1989], but it wasn't."

To save time, Brzezinski used as many routines from the old design as possible. The user interface was redesigned to focus on room-temperature measurements. All the programming was done in C, except for a few key time-critical routines, which were done in assembler. Aside from Microsoft's 6.0 C compiler, which was used to compile the code, the team used only its own custom-made graphics and analysis tools.

While the original software required a lot of development work just to make it function, modifying it for the Microflash product was a relatively straightforward task. One reason for this was that the original software had a layered structure. As a result, hardware changes could easily be made that affected only a single layer of software, not the whole program.

The code is divided into four layers: port, equipment, user interface, and the main program. The port level handles all the I/O communication to the board in the computer. This includes a DMA transfer routine which was written in assembler. Next, the equipment level controls the various devices in the system from a high level. Other parts of the program send simple commands to the equipment level to operate the IR detector, the laser and other devices. The equipment level calls the port level to handle the specifics of the I/O operation.

This strategy let the design team make changes to the software without rewriting too much code. "If you fire the laser, you don't care whether its done through the serial output or parallel output," says Brzezinski. "That's the port level's job to decide." While the equipment level played more of a role in the old system, with its larger mix of hardware devices, it made sense to leave it in the new design. Finally, the highest level was the user interface level, which dealt with all the inputs from and outputs to the user.

According to Brzezinski, the decision to use the DT2812A board didn't have much impact on the software design. The fact that it was a Data Translation board helped because this meant fewer changes to the code. While the DT2812A board package includes a library of routines, Brzezinski didn't use any of them. "We used a lot of code from the old system," Brzezinski explains. "If I didn't have the software written already, I probably would have used the Data Translation library." ■

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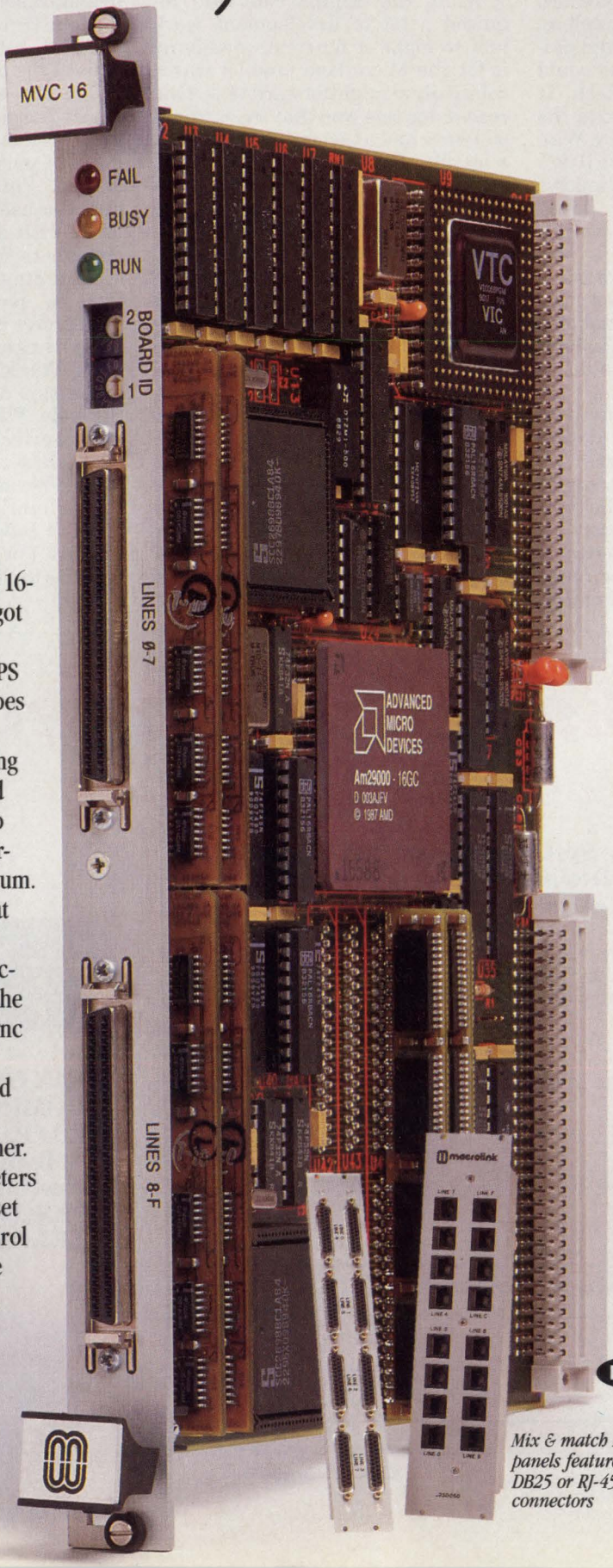

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INTEGRATED CIRCUITS

16-bit MCUs advance along many paths

Jeffrey Child, Associate Editor

Designers of a portable bar-code scanner at Spectra-Physics migrated from an 8-bit to a 16-bit microcontroller to get better performance and more features. Located on a small PCB inside the handle, a Motorola 68HC16 processes algorithms 4 to 6 times faster than a previous 8-bit MCU design.

Trying to stake out territory between less expensive 8-bit and more powerful 32-bit parts, 16-bit microcontrollers have evolved along traditional paths as well as in some interesting new directions. Microcontroller makers continue to add RAM and ROM, while squeezing more timers, interrupts, I/O ports, and other peripherals onto the die. At the same time, less traditional moves—from integration of RISC and DSP hardware to inclusion of smart peripherals to incorporation of special power-saving features—are having an impact.

First high-volume win

Designed jointly with the Ford Motor Company in 1982, the 9096 from Intel (Chandler, AZ) was the first 16-bit microcontroller to gain a high-volume design win. Intel, which dominated the 8-bit world at the time, wanted to base this 16-bit family on its 8-bit 8051 architecture. Unfortunately, the 8051 lacked the headroom needed for the targeted automotive application.

Intel's most recent addition to its 16-bit family is the 87C196KD. An upgrade of the 87C196KC, the new microcontroller offers 32 kbytes of ROM and 1 kbyte of RAM. The added memory will facilitate the use of high-level languages such as C. The KD is available in a 20-MHz version—a 25-percent speed increase over the KC. The part's other features include a high-speed I/O subsystem, a full-duplex serial port, pulse width modulated outputs, two 16-bit hardware timers, and a 16-bit watchdog timer. Because the peripherals on the KD are the same as on the KC, you can use the KD as a plug-in replacement for the earlier part.

According to Steve McIntyre, applications manager of Intel's embedded microcomputer division, one of the strengths of the 80C196 architecture is its register-based nature, which alleviates bottlenecks in the accumulator and provides faster context switching. "Because the 80C196 has a register-based architecture, it can perform any instruction on any of its three registers at any time," says McIntyre. The 80C196 differs from other chips such as the 8051 and Motorola's 68HC11 and 68HC16, which can't run directly out of their registers without the overhead of switching techniques.

A late entrant in the 16-bit race, Motorola (Austin, TX) announced the 68HC16, its first 16-bit microcontroller offering, two years ago. While Motorola wanted to maintain code compatibility with its 8-bit 68HC11 family, it also needed to leverage the technology advances achieved with the 68300 series, its highly integrated 32-bit microcontroller family. The solution was to use an intermodule bus (IMB) with the 68HC16. The IMB lets the chip access the sophisticated peripheral modules developed for the 68300 family, as well as the 68HC11's simpler modules.

While traditional development of microcontrollers usually involves straightforward improvements in CPU frequency and higher integration, Motorola found alternative ways to boost overall performance. "There's a second level of integration going on here," says Pat Heath, technical marketing manager for advanced microcontrollers at Motorola. "The first generation involves putting serial ports, timers and such on-chip. Now we're seeing the integration of things such as RISC and DSP hardware onto the MCU." The point of such techniques is to offload the chip's CPU core as much as possible. Exemplifying such techniques is Motorola's addition of instructions to the 68HC16 architecture specifically for DSP. These instructions control special hardware on the chip suited for running DSP algorithms.

Another state-of-the-art feature included on the 68HC16-Y1 version is a time processor unit (TPU). "The TPU has a RISC engine that can perform very complex timing functions without intervention of the CPU," says Arie Brish, marketing manager for advanced microcontrollers at Motorola. Only after it accomplishes the whole function does the unit interrupt the CPU. In contrast, traditional 8-bit timers interrupt the CPU on every clock edge. With a TPU, "you can perform a very complex instruction, such as accelerating a motor, for example," says Brish. "The TPU generates all the

Model	RAM (bytes)	ROM (bytes)	EEPROM (bytes)	Bus speed (MHz)	Interrupts (internal/external	Timers/DMA channels	Emulator available	Peripherals	Price	Comments
Advanced Micro Devices 901 Thompson Pl, PO Box 3453, Sunnyvale, CA 94088 (408) 732-2400										**Circle 301**
80C186	—	—	—	10,12.5, 16, 20	—	3/2	yes	—	—	fully static CMOS
80C188	—	—	—	10, 12.5, 16, 20	—	3/2	yes	—	—	same as above
Hitachi America 2000 Sierra Point Pkwy, Brisbane, CA 94005-1819 (415) 589-8300										**Circle 302**
H8/510	—	—	—	6, 8, 10	18/5	4/yes	yes	4 channels,10-bit ADC, 2 UARTs, 60 I/Os,wait-state cntl, RAM refresh	$11.85	16 Mbyte addrs space, 8 16-bit registers, orthogonal instr set
H8/520	512	16k	—	6, 8, 10	18/9	4/yes	yes	8 channels, 10-bit ADC, 2 UARTs, 54 I/Os, wait-state cntl	$22.25	same as above
H8/532	1k	32k	—	6, 8, 10	19/3	8/yes	yes	8 channels, 10-bit ADC, 1 UART, 65 I/Os, wait-state cntl	$25.80	same as above
H8/534	2k	32k	—	6, 8, 10	23/7	8/yes	yes	8 channels, 10-bit ADC, 2 UARTs, 65 I/Os, wait-state cntl	$29.60	same a
Intel 5000 W Chandler Blvd, Chandler, AZ 85226 (602) 554-8080										**Circle 303**
8XC196KB/ 8XC196KB16	232	8k	—	10,12,16	28	2/—	yes	1 serial port, 8 analog inputs, 48 I/Os, 10-bit ADC	$22.05 (2,000s)	
8X9XBH	232	8k	—	12	30	2/—	no	1 serial port, 8 analog inputs, 48 I/Os, 10-bit ADC	$5.90 (2,000s)	
8XC194/ 8XC198	232	8k	—	16	28	2/—	yes	1 serial port, 4 analog inputs, 48 I/Os, 10-bit ADC	$8.45 (2,000s)	
8X98	232	8k	—	12	20	2/—	no	1 serial port, 4 analog inputs, 48 I/Os, 10-bit A/D avail.	$5.00 (2,000s)	
8XC196KC	488	16k	—	16	28	2/—	yes	1 serial port, 8 analog inputs, 48 I/Os	$23.15 (2,000s)	
8X9XJF	232	16k	—	12	20	2/—	no	1 serial port, 8 analog inputs, 48 I/Os	$7.90 (2,000s)	
8XC196K0/ 8XC196K020	1k	32k	—	16/20	28	2/—	yes	1serial port, 8 analog inputs, 48 I/Os, 8- or 10-bit ADC	PLCC-OTP 16 MHZ $32.95 each per 2K	
8XC196KR	488	16k	—	16	39	2/—	yes	2 serial ports, 8 analog inputs, 56 I/Os, 8- or 10- bit ADC	$25.95 (2,000s)	
8XC196MC	488	16k	—	16	16	2/—	yes	1 serial port, 13 analog inputs, 53 I/Os, 8- or 10-bit ADCs	$15.25 - $26.50 (2,000s)	

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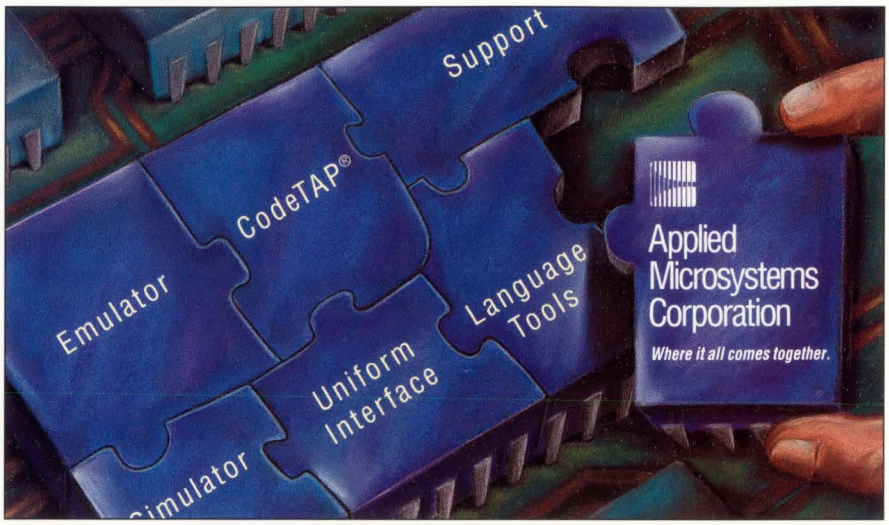

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M37730	1k	—	—	8, 16, 25	19/3	13/—	yes	23 I/Os	—	2 channel pulse ouput mode
M37732	2k	—	—	8, 16, 25	19/3	17/—	yes	37 I/Os, 8-bit 8-channel ADC	—	same as above
M37702	512 to 2k	16k to 32k	—	8, 16, 25	19/3	17/—	yes	68 I/Os, 1 UART, 1 synch 8-bit 8-channel ADC	—	3-V operation, 16 Mbytes addrs space
M37703	512	16k to 32k	—	8, 16, 25	—/3	14/—	yes	53 I/Os, 1 UART, 1 synch 8-bit 8-channel ADC	—	block move, exchange instructions
M37720	512	—	—	8 or 16	23/2	17/—	yes	53 I/Os, 1 UART, 1 synch 8-bit 8-channel ADC	—	DRAM controller, 4-bit real-time output
Motorola Advanced Microcont. Div. 6501 William Cannon Dr West, Austin,TX 78735 (512) 891-2000										**Circle 305**
MC68HC16Z1	1k	—	—	8.4	253/7	11/—	yes	2 serial channels	$15.87	timer processor unit (TPU) offloads core CPU, DSP instructions
MC68HC16Y1	2k	48k	—	8.4	253/7	27/—	yes	3 serial channels	$27.90	same as above
NEC Electronics 401 Ellis St, PO Box 7241, Mountain View, CA 94039-7241 (415) 965-6000										**Circle 306**
78322/324	640 to 1k	16k to 32k	—	16	13/8	2/yes	yes	8-channel 10-bit ADC, watchdog timer, UART, synch I/F, 39 I/Os	$11.40 (10,000s)	on-chip band rate generator; DMA-like macro service
78352	640	32k	—	32	13/5	3/yes	yes	2-channel PWM, watchdog timer, 44 I/Os, 6 inputs	$13.50 (10,000s)	DMA-like macro service; MAC instructions; fast context switching
78356	2k	48k	—	32	19/6	5/yes	yes	2 8-channel UARTs, 10-bit ADC, 2-channel 8-bit DAC, 2-channel 8/10/12-bit PWM, watchdog timer, UART, 69 I/Os, 8 inputs	$16.00 (10,000s)	same as above
National Semiconductor 1111 West Bordin Rd, Arlington,TX 76017 (800) 272-9959										**Circle 307**
HPC46100	1k	—	—	40	8	7/—	no	8-channel 8-bit ADC, 31 I/Os, full-duplex UART	$14 (10,000s)	DSP capability, MAC unit, watchdog timer, 16×16 mult, 32×16 divide
HPC464064	512	16k	—	20, 30	8	8/—	yes	4 full-duplex UARTs, 52 I/Os, serial I/O	$10-$13.30 (10,000s)	16×16 mult, 32×16 div; idle & halt modes
HPC46400E	256	—	—	20	8	4/—	no	4 full -duplex UARTs, 36 I/Os	$19 (10,000s)	2 full-duplex HDLC channels for X.25, 4- channel DMA cntl

Model	RAM (bytes)	ROM (bytes)	EEPROM (bytes)	Bus speed (MHz)	Interrupts (internal/external	Timers/DMA channels	Emulator available	Peripherals	Price	Comments
SGS-Thomson Microelectronics 100 E Bell Rd, Phoenix, AZ 85022 (602) 867-6100										**Circle 308**
ST107166	8k	—	256k (flash)	20	32/16	3/8	yes	2 UARTs, 10-bit ADC w/ 9.75 µs settling, 76 I/Os, watchdog timer	$53.00	4-stage pipeline, 10 Mips, performs 16×16 multiply in 500 ns
ST10166	8k	256k	—	20	32/16	3/8	yes	same as above	$25.00	same as above
ST9040	3.8k	128k	4k	12	13/9	2/6	yes	8-bit ADC	$14.00	
Siemens Components 2191 Laurelwood Rd, Santa Clara, CA 95054 (800) 456-9229										**Circle 309**
SAB 80C166	8k	—	—	16	16	6/yes	yes	2 UARTs, 10-channel 10-bit ADC, 16 capture/compares, 76 I/Os	$32.00	typical instruction executes in 100 ns at 20 MHz
SAB 83C166	8k	262k	—	16	16	6/yes	yes	same as above	$35.00	same as above
SAB 88C166	8k	—	262k (flash)	16	16	6/yes	yes	same as above	$95.00	same as above, bank segmented flash
SAB C167	16k	65k	—	20	48	6/yes	yes	1 synch/asynch serial port, 110 I/Os, 16-channel 10-bit ADC	$30.00 ($10,000s)	16 Mbyte addrs space, 5 chip selects, instr extension for HLLs
Zilog 210 E Hacienda Ave, Campbell, CA 95008 (408) 370-8000										**Circle 310**
Z86C95	2k	—	—	24	6/4	3/—	yes	UART, ADC, DAC, PWM, mux/demux ADC	$10.00 (10,000s)	2.7-V version available
Z89120	2k	20k	—	10	9/3	4/—	yes	ADC, PWM, watchdog timer, 8×16 mailbox, 47 I/Os	$11.25 (10,000s)	TI DSP translator available
Z89C00	—	4k	—	10	3	—/—	yes	16-bit I/O port, 16-bit programming port	$8.20 (10,000s)	TI DSP translator avail, single-cycle 100-ns instructions

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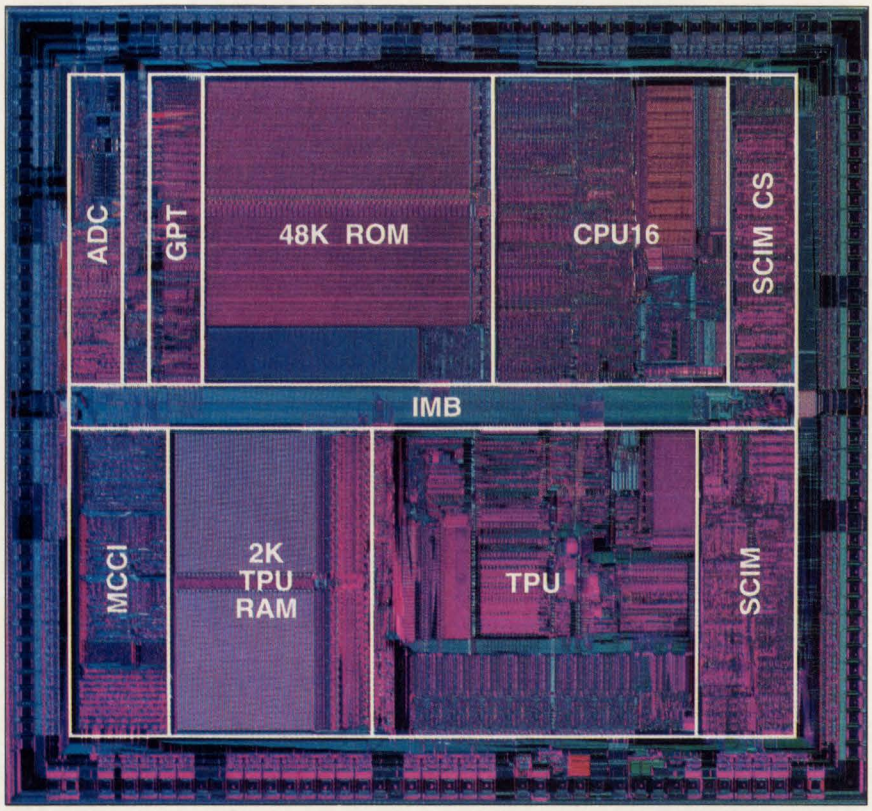
CIRCLE NO. 79



Even though it used precious die area, Motorola felt it was important for strategic reasons to add an intermodule bus (IMB) to its 68HC16 microcontroller architecture. The IMB lets the chip access the sophisticated peripheral modules developed for the 32-bit 68300 family, as well as the 8-bit 68HC11's simpler modules. As a result, you can expect a smooth migration path across a wide range of performance levels.

waveforms needed without interrupting the CPU."

Moving up from eight bits

Typically you decide to use a 16-bit microcontroller to upgrade a design that's currently based on an 8-bit device. To accomplish this, engineers at Spectra-Physics Scanning Systems (Eugene, OR), a company that makes bar-code scanners for supermarkets, chose a Motorola 68HC16 for its next-generation line of portable bar-code scanners.

Brad Reddersen, the company's R&D manager for portable products, describes why there was a need to migrate: "We wanted to speed up the coding. In a bar-code scanner, you capture input data and record the time that it comes in. It's a fairly time-intensive software operation: looking at the incoming data on the fly and deciding not only which bar-code symbology it is but also interpreting what the data says. Moving from the 8-bit part to the 16-bit part, we probably saw a 4× to 6× improvement in throughput of our algorithm."

Another of Spectra-Physics' design goals was to interface its bar-code scanner with different types of data terminals. This calls for many different interface protocols—for example, to the RS-232 and the RS-485. Many such protocols have incompatible baud rates. "Traditional MCUs limit you to rates that can be derived from whatever the clock frequency is," says Phil Shepard, digital systems engineer at Spectra-Physics. "One of the nice things about the 68HC16 is that it uses a voltage-control oscillator internally to drive any number of clock frequencies."

The 68HC16 did, however, have one drawback. "One thing that Motorola didn't do as well as we would have liked is [handle] power consumption of the [68]HC16," says Shepard. "We operate in a portable environment. A lot of the portable data terminals operate off a battery. That was one of the trade-offs in moving up to a 16-bit family, either in the overall power consumption or in ways to manage it down during parts of the operating cycle."

Power plays

Ike Saeed, marketing manager for MCU products at Mitsubishi Electronics America (Sunnyvale, CA), sees integration and 3-V operation as the two important trends for 16-bit microcontrollers. "In our 16-bit family we offer parts that operate from 2.7 V at clock speeds up to 8 MHz," says Saeed. "The resulting power dissipation is just 4 mA. We're finding a great deal of interest in low-power versions for applications such as cellular telephones and other handheld products."

The standard M37702-series chip, Mitsubishi's 16-bit microcontroller architecture, has up to 32 kbytes of on-chip ROM or EPROM, and 2 kbytes of SRAM. A standard device also has up to eight 16-bit timers, and each timer has a variety of modes. The device also has two full-duplex UART channels with a watchdog timer.

For its part, Siemens (Santa Clara, CA) has expanded its 16-bit SAB 80C166 microcontroller family by adding an enhanced part, the SAB-C167. The new part features an impressive interrupt sample rate of 50 ns, the fastest in the industry. Built for automotive engine control, the part offers a 50-ns counter resolution and a 100-ns instruction execution time at 40 MHz. The C167's expanded feature set includes a 78-kHz pulse width modulation unit, with four independent channels and a 32-channel capture/compare unit.

There are some microcontrollers that are difficult to classify as being either 8-bit or 16-bit. For example, the H8/500 series of 8/16-bit microcontrollers from Hitachi America (Brisbane, CA) has a 16-bit core with an external datapath that's eight bits wide. Benchmark tests suggest its performance is 60 percent better than that of popular 16-bit microcontrollers. With that level of performance, the H8/500 series perhaps reflects the potential of 16-bit microcontrollers to capture territory from more powerful 32-bit devices. ■

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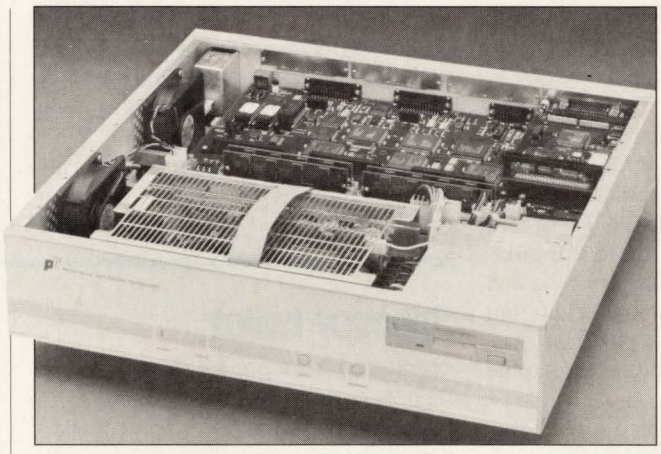
SBus News®

Technology and Market Update for SBus Users and OEMs

Embedded SBus gets systems orientation

Embedded SBus solutions have ridden on the coattails of the Sparcstation from Sun Microsystems Computer Corporation (Mountain View, CA). While some OEM systems use a full-fledged workstation embedded in an application, it's more likely that a single-board version of the workstation will be used. Sun, for example, has offered a single-board version of its Sparcstation (called Sparcengine) ever since the workstation was introduced. And the company has updated releases of the Sparcengine with each new Sparcstation offering.



Performance Technology's SBus/System provides a complete Sparc-based computer packaged as a system designed for embedded real-time applications. The system comes with Ethernet, SCSI-2 and serial ports, and is available with either four or eight SBus slots and a number of DRAM and mass memory options.

More function, better package

But some OEMs are looking for more functionality and a more convenient package to embed into their real-time systems. Responding on the one hand to OEMs prone to VME or Multibus II solutions but looking to reduce costs, and on the other to manufacturers wanting more complete solutions than those offered by single-board computer makers, Performance Technology (Rochester, NY) is providing a system-level, Sparc-based computer designed primarily for real-time embedded solutions.

Sun claims it will convert 70 percent of its existing VME single-board customer base to single-board SBus products, while 30 percent will elect to stay with traditional VMEbus-based approaches. This second group of customers will be served by other vendors. Force Computers (Campbell, CA), through a technology exchange with Sun, offers a Sun 1E board—equivalent to a Sparcstation 1—as well as a Sparcstation 2 equivalent, the 2S, without a VME interface. A version with VME interface will be available this fall. Themis Computer (Pleasanton, CA) also offers a Sparcstation 2-equivalent board with a VMEbus interface.

While these Sparc-based approaches—and some new ones that will surface later this year—continue to gain both PC and VME/Multibus II embedded computer business, some OEMs want more. The existing VME solutions (the 1E and 2E from Force and Themis) consist of VME boards with slots for only a pair of SBus cards. And because of the height of the SBus connector, these solutions occupy two slots in a VMEbus card cage.

The busless solutions from Sun and Force, Sun's 2E and Force's 2S respectively, also have only two SBus slots each, while Sun's latest entry, the Sparcengine 10, provides three slots. In addition, OEMs using single-board approaches must handle mechanical mounting, power-supply placement and other factors that could have an impact on functionality and reliability.

In comparison, Performance's package offers a full-function, Sparc-based

continued on page 136

SBus spec heads for sponsor ballot

The SBus specification, now officially dubbed P1496.1, is on its way to a sponsor ballot, according to Wayne Fischer, P1496 Committee chairman and strategic marketing manager for Force Computers (Campbell, CA). While zipping rapidly through the specification process, the standard hasn't moved lightning-fast through the IEEE obstacle course. Initially Fischer believed the specification would be finalized before year-end; now it appears that March 1993 would be more realistic.

The mature state of SBus technology and its well-defined specification have contributed to the rapid progress made on the standard. In addition, a large contingent of third-party manufacturers—not to mention Sun, with tens of thousands of workstations in the marketplace—has already committed to the specification by building modules and systems.

But it's these same vendors who've caused delays in getting the specification finalized. Some designers of SBus hardware have taken liberties with the original SBus specification. Their companies have tried to bend the specification to

continued on page 136

Embedded SBus

continued from page 135

computer complete with Ethernet, a SCSI-2 FAST port and a pair of serial I/O ports. The motherboard comes packaged with a power supply in a rack-mountable rugged enclosure. Performance's box also includes sites for up to eight SBus option cards.

"We're finding a lot of interest from users that have been struggling with packaging and power-supply issues in embedded applications," says Don Turrell, SBus product manager for Performance. "In some cases, these users are looking to get out from under the cost and size constraints of a VMEbus card cage and backplane. In the VME environment, not only can the card cage and mounting take up additional space, but OEMs are often forced to purchase relatively expensive VME cards for simple I/O functions."

The availability of up to eight SBus slots gives Performance's system an advantage over competing boards, especially in systems that call for SBus option modules occupying two slots. Because of the small form factor of SBus, many functions, such as high-speed communications, call for two slots to provide enough PCB area as well as supplying needed power.

Option selection

OEMs want as complete a package as possible, so Performance offers a number of options that let them tailor a package to fit their needs. The shell is a rugged modular aluminum enclosure, which comes in standard form as a desktop unit with optional wings for 19-in. rack mounting. The system is equipped with an integral 50/60-Hz power source which includes a pair of dc fans.

"While our original intention was to supply a completely packaged unit," says Turrell, "we've had an increasing number of requests for board-only-based systems for users who want the flexibility of the additional SBus slots, but want to use their own enclosure. Performance plans to make a board-only version available soon."

Other options include a customizable polycarbonate front panel. The PT-SYS500X (with the X being either a 4 or an 8 for the number of SBus slots), offers DRAM options from 2 to 64 Mbytes. Memory expansion is through field-installable memory modules available from Performance. The system is provided without floppy or hard disks, but a number of disk option kits are available.

Performance's system is designed for real-time embedded systems, and as such it offers the Lynx real-time operating system as an option. The Lynx port on the SBus/System, as Performance dubs its package, is a derivative of the LynxOS Sparcstation port built in conjunction with Sun Microsystems. "While we developed this product primarily as a real-time embedded engine," says Turrell, "we've already had some requests for a regular SunOS/Solaris Unix-type operating system."

The introduction by Performance—a leader in the VMEbus community—of a stand-alone, Sparc-based embedded computer system underscores the trend toward smaller, less expensive single-board solutions with mezzanine-board options. The fact that demand is for more complete systems, including package, power supply and even OS software, indicates that OEMs are beginning to look at an embedded computer as a single system component, and not necessarily as a differentiating factor in the final solution. ●

Sponsor ballot

continued from page 135

their benefit during the working-group balloting. The same issues may resurface during the sponsor balloting.

"Because of the large number of comments in the working group ballots," says Fischer, "the process of getting working-group approval took about five weeks longer than we planned. But the specification has come out a lot stronger because of the attention paid to each comment. And because we addressed each comment in the working-group ballot, I expect relatively quick passage through the sponsor ballot."

The fact that there's been some abuse of the specification in the past points to the need for its solidification, comments Ray Alderman, technical director of VME/Futurebus+ International Trade Association (VITA—Scottsdale, AZ). Although the specification isn't yet formalized, Alderman says that copies of the preliminary document are available through VITA, so developers don't have to worry about designing to the wrong specification. "I don't think there will be any substantive changes to the specification as a result of the sponsor ballot," adds Fischer.

Sponsor ballot

The sponsor ballot is the final hurdle in the IEEE standard approval process. The specification is sent to a group of members selected in advance because of special knowledge or interest in the area. These individuals review the document, checking it for technology and language. While sponsor balloting is supposed to take 30 days, it usually takes about twice that long. Any negative comments must be resolved before the document passes sponsor balloting. If, in the course of this resolution, the document is modified, it must then be approved once again by the entire sponsoring body.

Based on the condition of the SBus specification, few negative comments are expected. But there may be some sponsor members with an ax to grind, and this could hold the document up in the sponsor approval process for another 30 to 60 days.

"The working group took a middle ground in finalizing the specification," says Fischer. "It's impossible to guarantee that every SBus module—or, for that matter, every SBus host—will be 100-percent compatible with the specification, but the group put together an SBus standard it felt was right."

While there may still be a few bumps in the road, most SBus developers—including Sun—are eager to have the standardization process complete. It will solve any current or future problems with host and board compatibility, and it assures manufacturers of a consistent specification for at least the next several years. If nothing more, the IEEE sanction guarantees developers that the specification—good or bad—will not change at the whim of any individual or company. ●

The status of P1496

***Bob Snively**, Sun Microsystems Computer Corporation, Mountain View, CA*

Since Sun Microsystems publicly introduced SBus in 1989, there's been a continuing effort to make it an open, standard interface. An SBus Committee was established in 1991 to initiate the transfer of architectural control of SBus to the public. The committee quickly decided that the best way to advance its goal was to transfer its activities to the IEEE. The P1496 Study Group, chaired by Wayne Fischer of Force Computers, was subsequently set up in July of 1991 by the Bus Architecture Standards Committee of the Technical Committee on Microprocessors and Microcomputers of the IEEE Computer Society. Over 180 individuals representing many companies have participated in P1496 Working Group activities.

The P1496 Working Group used SBus Specification B.0, published in December of 1990, as its base document. The SBus B.0 document was the most widely used reference for SBus until the publication of the P1496 draft standard, revision 2.0, in July of 1992. Now that the P1496 document is nearing the status of a standard, it's important to understand how it differs from the SBus B.0 document.

The P1496 document will not seem familiar to users of the SBus B.0 specification, since the former had to be completely rewritten to conform to the requirements of an IEEE standard. Redundancies were eliminated and references to proprietary information and nonstandard implementations were removed. Considering the logical functions of SBus controller, master and slave separately simplified the structure of the document. Open boot information previously contained in the SBus B.0 document was removed, since it will be included in IEEE P1275, the proposed standard for boot firmware.

In spite of the complete rewrite of the document, however, very few technical changes were required to turn SBus B.0 into the P1496 document. Most of the changes were associated with conflicting, unclear or incorrect statements in the original SBus B.0 document. A few were linked to improvements that had been requested by the Public SBus Committee.

Other changes to the P1496 document include items in the following areas:

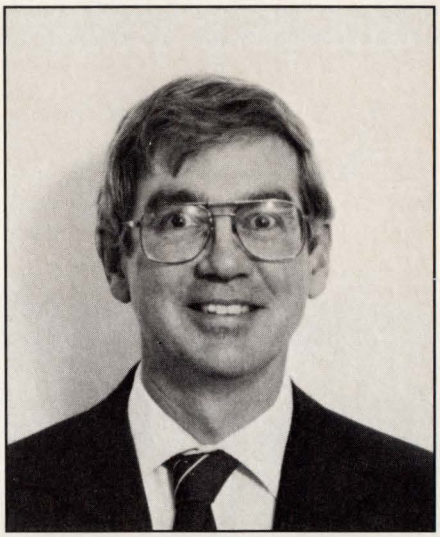
ATOMIC OPERATIONS: After much discussion, atomic operations were removed from P1496. The SBus B.0 definition of atomic operations couldn't be implemented, especially when SBus was used as an I/O bus bridged from a host memory bus. In addition, inconsistent interpretations of the original definition had created incompatible implementations among those few devices that had attempted to include the functions.

64-BIT EXTENDED TRANSFER OPERATIONS: This capability was moved from an appendix of the SBus B.0 document into the normal description of SBus. The extended lock protocol was clarified and modified to allow locking a shared SBus slave resource to a particular SBus master.

RERUN: The rerun function was renamed "retry" to correctly define its actual behavior. The definition of retry was extended and modified so that it behaves correctly in the presence of errors and lets SBus cycles be divided into two parts, one to initiate the SBus transfer and the second to complete the operation.

PARITY: The description of parity checking was completed, so that individual SBus master/slave pairs could check parity even if the remainder of the system didn't do so.

RESET: A 100-ms wait period was recommended after completion of a reset to allow SBus cards sufficient time to initialize themselves. Since this was not made a requirement, it's still good practice to implement an SBus card so that it's ready for operation immediately after a reset is completed.



ELECTRONIC REQUIREMENTS: The drive and termination requirements were more completely explained so that compliance with the standard could be verified. Capacitive loading tolerance for the clock signal was tightened to decrease the influence of loading on clock skew timing.

TIMING: The method for measuring timing was defined more strictly to allow compliance verification. The total skew budget was apportioned more realistically. The new skew budget requires clock skew timing specification to be tightened and clock-to-signal timing to be decreased. These modifications allow reliable operation of all SBus cards in any SBus system.

MECHANICAL DRAWINGS: These were modified to correct errors and to resolve inconsistencies. The component height definition for connectors was clarified. Future work of the Electronics Industry Association will standardize the present SBus connector.

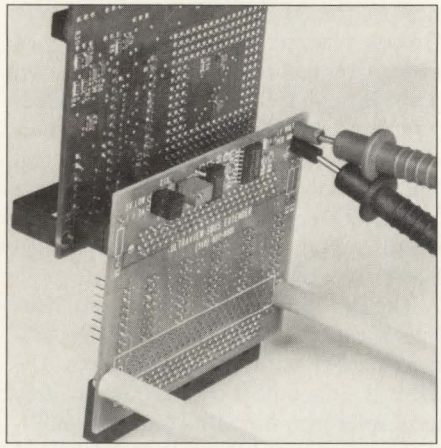
The P1496 Working Group reviewed all these changes very carefully to be sure that the original intent of the SBus B.0 specification was retained. Now that sponsor balloting is beginning, the working group is expecting the IEEE review to identify any other corrections required in the proposed standard. The P1496 Working Group is confident that the new standard will be an important aid to the expanding SBus marketplace. ●

SBus gets tester/analyzer support

Although SBus has gained much momentum as a result of the support of Sun Microsystems Computer Corporation (Mountain View, CA) and its installed base of Sun workstations, the infrastructure needed to make the technology a truly universal standard is just emerging. That infrastructure includes, in addition to a well-documented, stable standard, a critical mass of active module developers, readily available software support and tools for testing and debugging the bus.

The official standardization of the bus by IEEE should provide the needed stability, and will also guarantee that the specification is well-documented. Sun claims that well over 100 third-party vendors are developing and manufacturing SBus modules. And at least one SBus analyzer has been announced.

Now, a smart SBus extender board is being made available that lets you easily access all 82 SBus signals from a set of in-line, logic analyzer-compatible test points. The extender, from Ultraview (Freemont, CA), is called the SBext-82; it lets the board under test be placed in a vertical orientation, giving you easy access to both sides and leaving all components on the board in full view.



Ultraview's SBus extender card is the first such device to arrange the pins of all 82 SBus signals in logical order (rather than in pin-out order) to permit organized connection to a logic analyzer. In addition, the card provides circuitry to constantly measure power dissipation of the card under test.

In addition, the SBext-82 has a 33-mΩ shunt that's combined with an on-board differential amplifier circuit to continually measure the 5-V current consumption of the board plugged into the extender. Connection for meter probes lets you directly read a voltage that's proportional to the current drawn by the board under test. In addition, a set of LEDs constantly monitors the 5-V supply for the tested device. Any deviation below the 4.75-V low-voltage limit, or current in excess of the specified 2 A, will be signaled by the LEDs. ●

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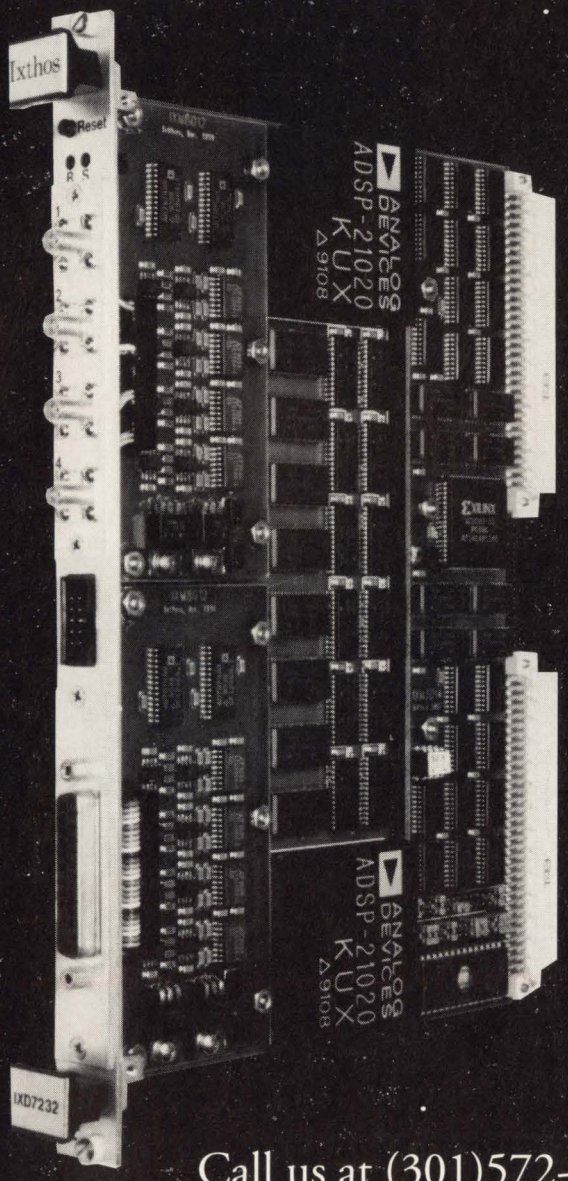

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SBus Shorts

Prices down, capabilities up

SBus is reaching the level of maturity where prices are starting to drop and second-generation or enhanced products are emerging. This is the case at Aurora Technologies (Waltham, MA), which has dropped the price of its 8- and 16-port intelligent line serial cards by 33 and 25 percent respectively. At the same time, the company announced software and hardware enhancements to two of its other I/O products: a Centronics-compatible parallel port device (Model 10S) and a multiport device, Model 210S.

Sun affirms support

In an issue of Sun's *SBulletin*, the company indicated it was curtailing its support of third-party SBus option-card developers. In a later issue of the same publication, however, the company affirmed that it would continue to support these developers, but with a refocused effort toward software requirements. The company said it "will continue to provide phone, fax and E-mail support on demand for hardware, firmware and software queries from the SBus developer community. Because of the focus on the Solaris 2.0 software transition, we will probably respond less quickly to your requests than we have in the past." But Sun added that it would acknowledge messages and respond to them as quickly as the workload allowed.

Sparc chip set for compatible workstations

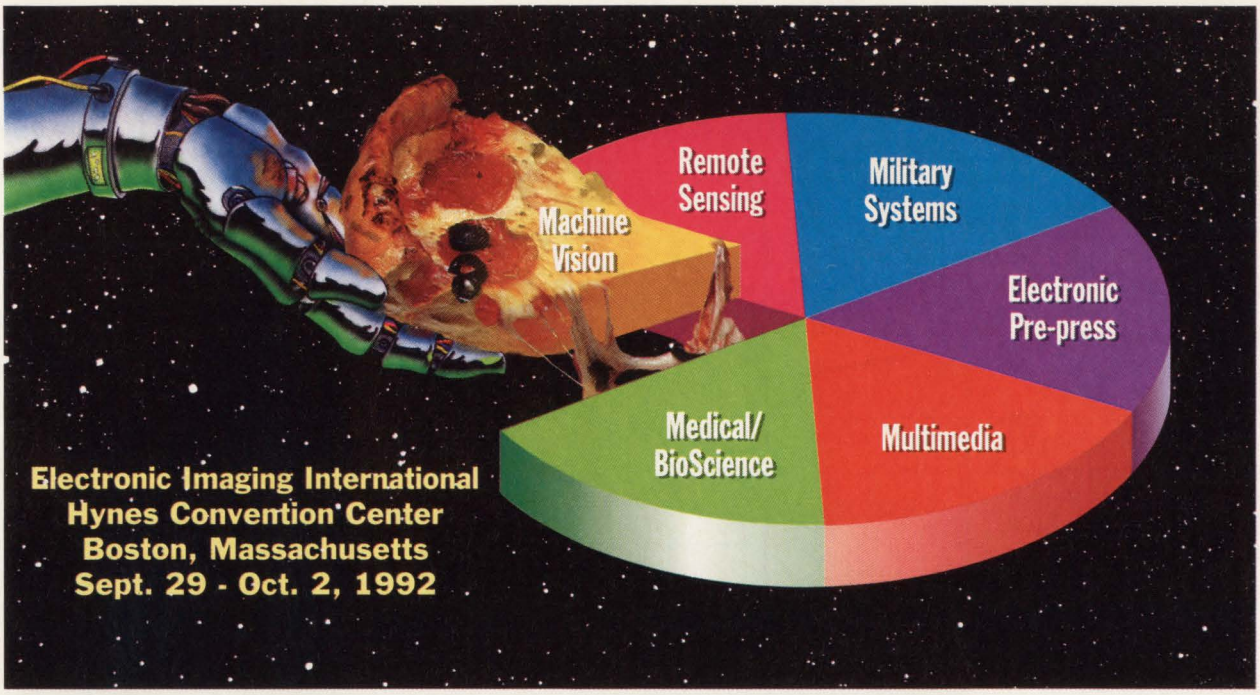
Cypress Semiconductor (San Jose, CA) unveiled a set of peripheral chips plus a licensable motherboard design for would-be Sparc-compatible system makers that will lead to a new, more powerful generation of workstation products. Cypress believes its chip set will let Sun-compatible workstation manufacturers significantly reduce costs and time-to-market, letting them focus their efforts on specific value-added features. The chip set includes a graphics controller, a complete M bus-to-SBus interface, a 2-chip main memory controller, and a pair of I/O chips that let Sparc-compatible makers use low-cost controllers made for 386SX bus products. In addition, Cypress provides all the technical data necessary to build 8-layer motherboards that exactly fit the standard Sparc workstation enclosure.

Sparc architecture extended to 64 bits

A collaborative effort of more than a dozen companies working within the Sparc International organization has developed Version 9 of the Sparc architecture, extending it to 64 bits and adding several new instructions. Full details of the specification will be made available by the group next month. The previous version, Version 8, was the basis for the SuperSparc and HyperSparc families of chips; it was developed by Sun with the aid of several semiconductor companies. After completion of that version, the responsibility for the architecture was turned over to Sparc International.

SBus Showcase

At Electronic Imaging International,



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Banding controller cuts printer memory demand

Intel has introduced a coprocessor for its i960, the 82961KD graphics processor, that handles 600-dpi laser printers and provides hard-wired graphics processing functions that keep up, in real time, with anything a desktop publishing program can throw at it.

The architecture embodied in the 82961KD was developed by Peerless (Redondo Beach, CA) and licensed to Intel. The 82961KD incorporates a programmable system controller that integrates memory and I/O logic. Also included are a DRAM controller, an interface to font or other enhancement cartridges and a video-engine interface.

The secret of the new coprocessor is banding. With four times the number of pixels per unit area as a 300-dpi printer, 600-dpi units would be memory hogs if they used the same page-at-a-time processing and buffering techniques as today's desktop units. A 300-dpi printer, for example, requires 8 to 10 Mbytes of memory to buffer an 11-ö-17-in. PostScript page.

Banding is a technique in which the printer's processor deals with the image sequentially in horizontal segments, or bands. This reduces memory requirements to an amount sufficient to support only a few bands at a time.

The first printer to use the 82961KD, the CCL 600 from CalComp (Anaheim, CA), requires only two Mbytes of memory to print 11-×-17-in., 600-dpi pages on its Canon BX print engine. The CalComp printer uses a Peerless Model KD-16 controller that's based on the combination of an i960 and an 82961KD. Selling for less than $5,000, the CalComp printer is priced considerably below competitive 600-dpi printers, and even below some 300-dpi models.

The i960 functions as a controller in the device. In addition to general housekeeping, it interprets page description language (PDL) files sent from the host to build display lists of graphics instructions for each page.

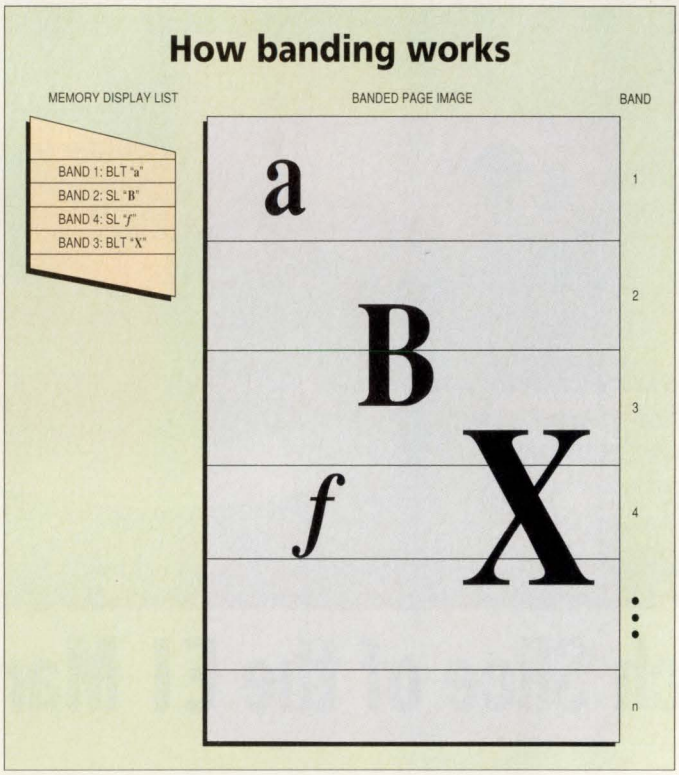
A graphics execution unit (GEU) in the 82961KD processes the display list, a band at a time, sending the resulting raster lines to the printing drum in real time. The GEU accelerates line drawing, font rendering, polygon fills, shading, and halftones.

Much of the processing in the 82961KD takes place in parallel. Bit boundary block transfer (bitblt) operations, for example, are split into separate tasks: calculating and applying masks, moving bit fields and aligning source and destination addresses. These tasks are then performed in parallel, resulting in performance four times faster than current graphics accelerators.

Peerless provides several techniques to keep the i960 and the 82961KD running efficiently in parallel. The controller maintains multiple display list buffers, for example, letting the CPU start on the next page while the GEU is still operating on a current page. This also lets the CPU work with different levels of graphical complexity without slowing the print operation.

Available now, the 82961KD is priced at $51.70 in lots of 1,000.

— Don Tuite



Banding is a technique for reducing laser printer memory requirements by segmenting a page into narrow bands, which are processed sequentially. At left, in page description language (PDL), is a memory display list mapping the different graphic elements to appear on the page (right). Bitblts (marked BLT) designate rectangular pixel arrays used mostly for small fonts; scan-lines (SL) designate polygonal arrays used mostly for larger fonts. The PDL doesn't have to take the graphic elements in order. The graphics processor sorts out the elements to drive the print engine. Using banding, a printer needs memory for only three bands at a time—to print the last band, process the current band and read in the next band.

82961KD graphics processor at a glance

- Needs only 2 Mbytes of memory to print 600 dpi
- Integrates printer memory and I/O logic
- Hard-wired parallel architecture works simultaneously on different parts of graphics operations

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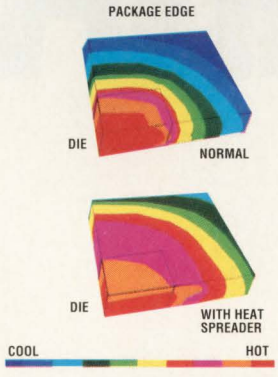

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SOFTWARE & DEVELOPMENT TOOLS

The 3001 GPX logic analyzer (below) addresses the needs of both hardware and software engineers with high-speed analysis of state and timing, disassembly, real-time performance analysis, and ROM emulation on the target system.

High-speed state and timing analysis at a midrange price

With tools that make it attractive to both software and hardware engineers, the 3001 GPX general-purpose logic analyzer from Tektronix integrates 1-GHz timing analysis capabilities across 16 channels, or 200-MHz transitional timing over 80 channels. It's also capable of 80-MHz state analysis on all 80 channels. And it does this for less than $9,000.

Simultaneous 80-MHz state and 100-MHz timing measurements can be made through the same probe by assigning either or both time bases to any channel or group of channels. The analyzer's trigger state machine can tell it when to store data and what time base to use. You could, for example, monitor the microprocessor in state mode to look for a given event. When the machine detects the event, it can switch to store data at the higher-speed timing for greater resolution.

The GPX has 27 preprogrammed trigger conditions, so new users can get a quick start and use existing triggers to build their own later. Trigger conditions include "trigger on word within range," "measure pulse width" and "trigger on Nth occurrence of word."

The probing system is optimized for 1-GHz operation, with signal conditioning and only 5-pF capacitive loading at the tip. Signal leads can be used individually or grouped into convenient podlets. Groups of podlets, in turn, snap onto the probe body. Several probe bodies can also be easily snapped together, letting the instrument monitor up to four microprocessors.

The GPX supports popular microprocessors and microcontrollers from Intel and Motorola, including the Intel 8031/8051 through the 80486, the Motorola 680X0 family and 68302/331/332 microcontrollers, as well as DSP chips from Motorola and Texas Instruments.

Target: software engineers

The GPX includes several tools targeted at the needs of software engineers. Disassembly software can display the program at five levels of abstraction: subroutine, control flow, software, hardware, and state. It's possible to download the symbolic information generated by a compiler and designate program routines by name. This lets you correlate what you're seeing on the analyzer with a high-level source listing (in a language such as C or Pascal) that may be present in a debugger running on a workstation. Real-time performance analysis (PA) gives you a graphical overview of where the system is spending its time. The GPX's performance analysis is real-time in that data is acquired continuously and processed in the background. Ranges of interest such as memory addresses or program subroutines can be set up by name and monitored. Up to 12 channels can be set up for one PA. Up to four PAs can be run simultaneously to monitor four processors, or four PAs can monitor a processor covering 48 real-time ranges.

The GPX uses a ROM emulator to control the target microprocessor, download code and set breakpoints. Target-resident code can also be patched from the keyboard via the emulator, which is called the prototype development tool. The abilities to download and patch target code and even to write test routines from the logic analyzer are features which can replace some functions that normally require an emulator.

The 3001 GPX logic analyzer, priced at $8,995 as a stand-alone, is available with an optional 40-Mbyte hard disk. — *Tom Williams*

3001 GPX at a glance

- 1-GHz, 16-channel timing analysis
- 200-MHz timing over 80 channels
- 80-MHz state analysis over 80 channels
- Simultaneous state and timing measurements
- Supports 8031/51, 80X86, 680X0, and 68302/331/332
- Real-time performance analysis
- ROM emulation

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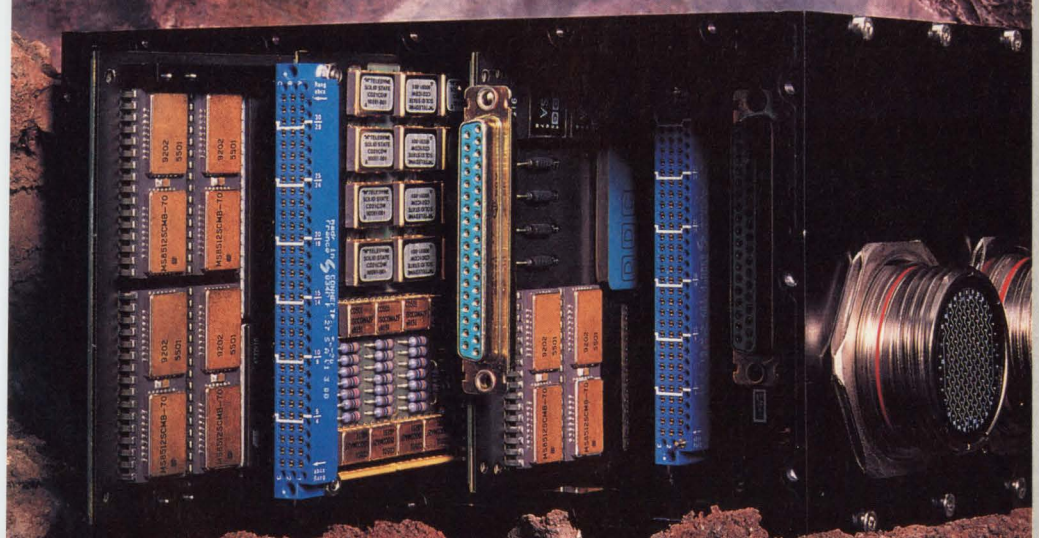

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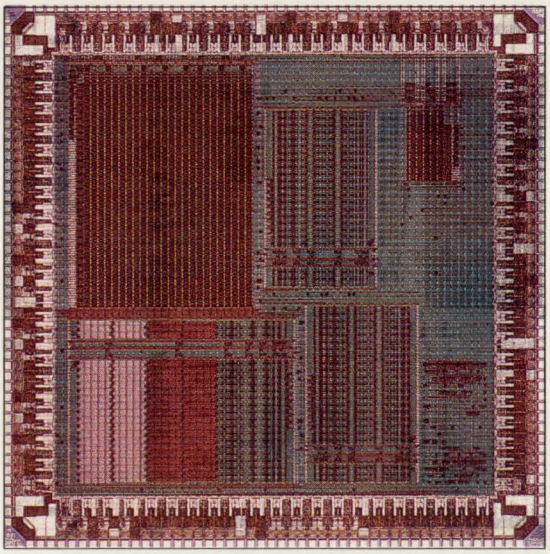
ASICs & ASIC DESIGN TOOLS

New cell-based arrays better CMOS sea-of-gates densities

Fabricated using Signetics' QUBiC BiCMOS process and the BiNMOS-CBA architectural design of start-up SiArc, Signetics' new Hi-IQ cell-based array family conforms to neither the typical sea-of-gates architecture nor the embedded array concept.

BiNMOS achieves significantly higher performance than CMOS without the inherent high cost of BiCMOS. With small MOS compute cells and larger MOS and bipolar drive cells, the Hi-IQ arrays support 80-MHz system speeds. For typical logic functions, they offer density improvements of up to 65 percent over CMOS sea-of-gate arrays, and for SRAM, they approach standard-cell densities, according to Signetics.



The Hi-IQ array features a new architecture called BiNMOS-CBA, which uses both CMOS and BiCMOS to implement logic and SRAMs efficiently at high speeds and low power. The device's core is configured as a channelless array of small MOS compute cells and larger MOS and bipolar drive cells.

Flexible technology

"Designers are asking for flexible technology that delivers faster turnaround with improved performance to keep up with an ever-changing market," says Ray Becker, Signetics' custom products marketing manager. "By blending a new architecture with advances in our BiCMOS process technology, these arrays will change the way designers create complex systems on a chip." With a 0.7-μm (L-effective) channel length and a bipolar transistor cutoff frequency of 13 GHz, Hi-IQ arrays come in five sizes, from 40,500 gates to 262,205 gates (of which up to 104,882 are usable); they offer up to 120 kbits of configurable SRAM, and as many as 284 signal I/Os, with a configurable output drive of up to 48 mA.

The BiNMOS circuit configuration addresses a critical performance limitation of large digital subsystem designs implemented in CMOS gate arrays—the poor pull-up capability of p-channel (PMOS) transistors at the output of macrocells. BiNMOS replaces these with bipolar NPN transistors.

The Hi-IQ array core is configured as a channelless array of compute and drive cells. Each compute cell consists of eight CMOS transistors of varying sizes. The drive cell consists of a single NPN pull-up transistor to improve drive, a pair of large NMOS pull-down transistors and a small PMOS level-restoring transistor to provide high speed for all fanouts. The compute and drive cells are arrayed so that two adjacent drive cells can use additional large NMOS pull-down transistors to optimize performance and area. The array architecture is designed to share drive resources among multiple compute cells.

One compute cell in a Hi-IQ array can implement a single bit of a single-ported SRAM. With the SiArc SRAM Compiler, you can generate SRAMs of arbitrary size that can be placed anywhere within the array core. The first set of output files generated by the Compiler contains a schematic symbol; a Verilog simulation model with timing information; a data sheet including timing, area and power estimates; and functional test vectors. The second set of output files contains physical layout models that can be used by place-and-route tools and the physical dimensions of the compiled SRAMs.

Macro library

SiArc has developed a library containing 350 macros that feature multiple drive strengths, low-skew clock drivers and high-drive I/Os. SiArc's CBA design system has been integrated with third-party tools to support the Hi-IQ arrays. Front-end tools include Synopsys synthesis, Verilog, SiArc libraries (with EDIF descriptions for macro symbols), and SRAM Compiler. Back-end tools include Cadence's Gate Ensemble place-and-route tools.

Packages available for the Hi-IQ arrays are a 100-pin PQFP and a 300-pin PGA. Prices range from $10 to $300, depending on gate quantities and packaging. Nonrecurring engineering expenses depend on individual design. *— Barbara Tuck*

Hi-IQ at a glance

- Supports 80-MHz system speeds
- Compiled SRAMs match density of standard-cell SRAMs
- Library of 350 macros created from small MOS compute cells and larger MOS and bipolar drive cells
- Five array sizes range from 40,500 to 262,205 gates
- Fast prototype and production delivery with metal-mask-programmable technology

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COMPUTERS & SUBSYSTEMS

Vector processor family gets 200-MFlops member

Using a pair of Intel's latest 50-MHz i860XP processors, gallium-arsenide ASICs and lots of memory, CSPI has added a VMEbus SuperCard to its vector processor family that boasts performance of up to 200 MFlops. The company claims the SC-3XL/VME is the first VME card to incorporate Intel's latest vector processor.

CSPI also says it now has the highest performance, single-processor-architecture 6U VME board. The 6U VMEbus board is available with one or two processors and a complement of anywhere from 8 to 64 Mbytes of DRAM memory supplied on a daughtercard. For easy upgrades, all memory resides on the daughtercard, and it fits within a single VME slot.

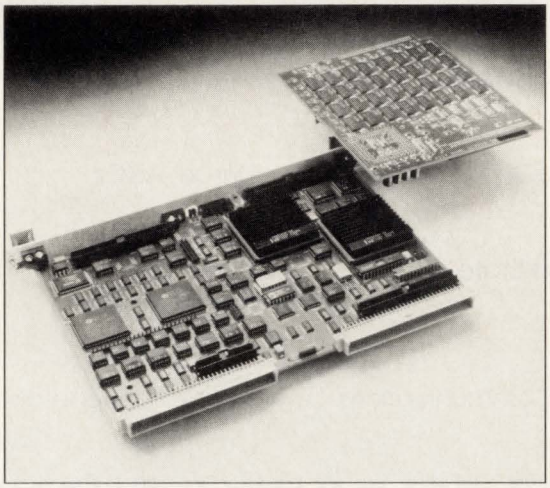
The motherboard incorporates a host of ASICs, one of which is a GaAs memory controller zipping along at 50 MHz. This controller lets the memory operate at 200 Mbytes/s. The board also supports cache coherency with bus snooping and has a provision for parity. "The snooping and cache coherency," says CSPI marketing director Geof Cohler, "are designed more to keep the cache coherent with other processing boards, and not so much to keep the two processors on the single board operating together."

The SC-3XL/VME, like its precursors in the CSPI family, will be primarily used in multiprocessing systems. There, the abilities to snoop the bus and to handle cache coherency are critical.

CSPI has worked closely on the product with Multiprocessor Toolsmiths (Nepean, Ontario), which offers its Integration Toolkit software for developers of multitasking and multiprocessing systems. This software environment includes both a real-time OS and Toolsmiths' set of Unix-compatible libraries and servers.

The pair of i860XPs is designed to operate on the board as if the two parts were a single processor. That's why the company claims the highest performance of any single-processor-architecture board—although there are boards with more processing horsepower in both the array processor and DSP environments.

CSPI claims its board is the only VME board currently using Intel's XP processor. There are several differences between the XP and XR versions of the processor, aside from the 40- vs 50-MHz clock speed. The major differences are larger caches (2×) and hooks for bus snooping and parity. While parity hasn't been a major issue in many past VME systems, it will be of increasing importance as system memory continues to grow. That's why the company designed the capability into the GaAs memory-controller ASIC.



CSPI's SC-3XL/VME is the first 6U VMEbus card to incorporate a pair of Intel's latest i860XP processor chips. The chips provide 200 MFlops of processing; when combined with a GaAs ASIC, they support bus snooping, cache coherency and parity. In addition, the board includes VME64, VSB and CSPI's own I/O channel. The SC-3XL/VME holds up to 64 Mbytes of memory on a separate daughtercard (pictured), yet it uses only a single VME slot.

Heavy-duty I/O

To enhance I/O control and eliminate possible bottlenecks, the board supports three independent I/O channels, all with DMA and all based on interface ASICs developed by CSPI. The board supports VME64, with a 72-Mbyte/s transfer rate; it includes a VME subsystem bus, with a 40-Mbyte/s transfer rate; and it has the capability, through an optional daughtercard, to utilize CSPI's own CSPIO interface. (CSPIO is a 64-bit interface standard designed to run at 200 Mbytes/s.) CSPI has worked with third parties to develop special daughterboards to take advantage of this speed to get raw data into the system quickly.

Handling all these options taxes the power budget allotted to VME. Fully equipped with maximum memory and both processors, the board eats up almost the full slot capacity of 45 W. Testing so far suggests it will require a little less than the full amount, however—perhaps more like 41 or 42 W.

The board is the logical successor to earlier CSPI cards—the SC-1, SC-2 and SC-2XL/VME—and is fully software-compatible with the company's other products. In addition, CSPI provides software support for platforms from Silicon Graphics, Sun Microsystems and others. The company believes that the new board will be useful for applications in sonar, radar, simulation, and image and seismic processing.

The SuperCard SC-3 and SC-3XL/VME will be available this quarter, with prices starting at $12,000. *— Warren Andrews*

SC-3XL/VME at a glance

- Dual i860XPs operate at 50 MHz
- 200-MFlops performance
- Up to 64 Mbytes of DRAM
- Cache coherency and bus snooping
- Parity option available
- Three high-performance I/O ports
- Implements VME64

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CIRCLE NO. 90

COMPUTERS & SUBSYSTEMS

Scalable 486-based STD32 CPU

The ZT 8911, the latest high-performance STD32 CPU board from Ziatech, is the first to implement the Intel 80486 architecture as well as take advantage of all the extensions of the STD32 bus. The board is designed to operate as the CPU in single-processor systems or as a master in multiprocessor systems.

Key to the board's scalability is a replaceable CPU module that accommodates several options, ranging from the low-cost 486SX up to the 66-MHz 486DX2. The module will also be compatible with Intel's next-generation processor. The ZT 8911 includes a standard 8-kbyte CPU cache and an optional second-level cache of 64 or 128 kbytes.

The board's memory architecture supports from 4 to 128 Mbytes of DRAM in four SIMM sockets. The memory is organized at a width of 128 bits for optimum cache fills and maximum performance. The ZT 8911 also offers most of the features called for in an STD32 CPU, including a printer port, two serial ports, a real-time, battery-backed-up clock, a pair of interrupt controllers, two high-performance DMA controllers, a speaker interface, extra counter/timers, a 24-point digital I/O interface, flash memory for a BIOS/file system, watchdog timers, a push-button reset, and an ac/dc power-fail detect circuit.

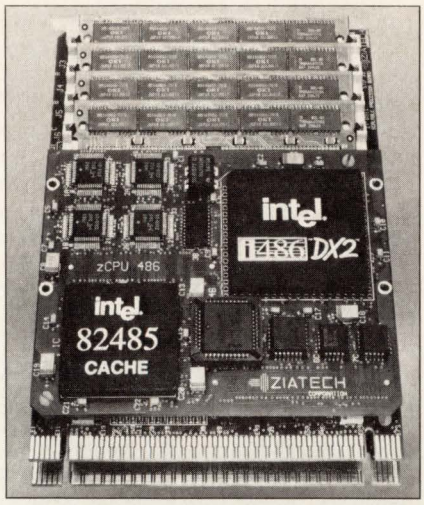
All the power of STD32

And, of course, the board takes advantage of the full STD32 interface, including the full bandwidth transfer capability of 32 Mbytes/s. Like all STD32 implementations, the device is compatible with existing STD80 systems and is built to rugged standards. The on-board flash EPROM provides solid-state disk space and boot support for MS-DOS and other operating systems, plus the ability to modify boot behavior. The ZT 8911 is supported by Ziatech's industrial BIOS, but it also supports other operating systems such as Microsoft Windows, OS/2, QNX, and Unix.

In multiprocessing environments such as Ziatech's STD32 Star System, the ZT 8911 operates as both the arbitration card and the permanent master. It occupies both slot X and the first user slot, and implements the full STD32 feature set, including bus arbitration, multiple high-speed DMA channels and slot-specific interrupts. A special 32-kbyte RAM space supplies the common memory for interprocessor communication in a Star System.

The ZT 8911 takes up just a single STD user slot. The board is available now, and prices start at $3,500, but they will vary depending on CPU and memory options.

— Warren Andrews



Ziatech ushers in the age of full STD32 Extended Architecture (EA) support with a scalable 486 CPU board. The piggybacked board uses only a single STD slot, yet packs a host of added features and allows for a number of optional processors.

ZT 8911 at a glance

- 486-based, scalable for present and future processor options
- 8-kbyte cache with 64- or 128-kbyte second-level option
- 4 to 128 Mbytes of DRAM
- STD32 compatible, with full support for STD80 peripherals
- 32-Mbyte/s transfer rate

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INTEGRATED CIRCUITS

New superscalar chip joins i960 family

The release of the i960CF adds a ninth member to Intel's i960 family of RISC microprocessors. Following the i960CA, the chip is the second in the company's i960CX series. Early press reports have lumped the i960CF with other superscalar processors such as the TI SuperSparc, Cypress Pinnacle and Digital Alpha chip, but it clearly belongs in a separate category. Unlike other RISC chips targeting desktop computers, the CF is meant for embedded applications with a computer requirement but more stringent cost considerations. These embedded applications include networking systems, page printers, mass storage, scanners, and telephony systems.

A key distinction of the i960CF is the robustness of its on-chip memory subsystem. In keeping with Intel's ongoing strategy for the i960 architecture, one of the CF's goals is the decoupling of compute and system costs. To achieve this, the CF features a 128-bit internal memory subsystem. The load/store internal buses and the path between caches are all 128 bits wide. As a result, you don't have to feed data into the chip from an external cache using expensive, fast, static RAM. Ordinary DRAM can be used instead, lowering overall system cost.

An enhanced version of its i960CA predecessor, the i960CF achieves higher performance with a new 1-kbyte instruction cache on-chip; the cache is four times the size of the i960CA's. According to Intel, alpha-site customers have credited this added cache with providing more than a 20 percent increase in data handling efficiency.

The processor's superscalar RISC core executes multiple instructions per clock cycle. Other features of the i960CF include an on-chip register cache, a 1-kbyte on-chip data RAM, four DMA channels, a 32-bit multiplexed burst bus, and a high-speed interrupt controller.

Because the part is both code- and socket-compatible with the CA version, designers currently using the CA can replace it with the CF and achieve a performance boost without any design changes. Furthermore, tools designed for the i960CA are compatible with the new chip.

RISC, but not RISC

Another interesting aspect of the CF is that, although it has the pipelining and performance typical of a RISC chip, its instruction set architecture is fairly complex. Although

this strategy strays from the RISC philosophy, it permits sophisticated instructions that can boost overall efficiency when running algorithms from the cache, according to Intel.

"A lot of people think that when they go from a CISC architecture to a RISC architecture, they'll have to expand their code quite a bit," remarks Alan Steinberg, director of strategic marketing for Intel's i960 line. "With the i960 architecture, that doesn't happen as much. We get more use out of smaller cache sizes because our instructions are a lot more efficient."

The i960CF processor is sampling now, with production volumes expected by the fourth quarter of 1992. It's available in ceramic 168-lead pin grid array (PGA) or 196-lead PQFP formats. Prices range from $105.80 each in quantities of 10,000 for the 16-MHz PQFP to $165.30 each in quantities of 10,000 for the 33-MHz PGA chip. *— Jeff Child*

i960CF microprocessor at a glance

- Superscalar RISC core
- 4-kbyte two-way set-associative instruction cache
- 1-kbyte direct-mapped data cache
- 1-kbyte on-chip data RAM
- Four DMA channels and a flexible on-chip interrupt controller
- Code- and socket-compatible with i960CA
- Works with ordinary DRAM

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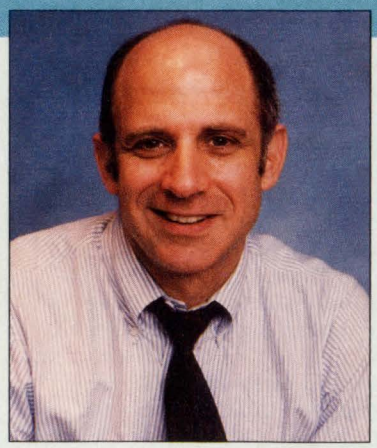

Mixed-signal test: balancing hardware and algorithms

With the ever increasing proliferation of mixed-signal devices, semiconductor manufacturers are giving increased consideration to the issue of testing. Because mixed-signal devices must handle voltages and currents, as well as 1s and 0s, the procedure for testing is more complicated and time-consuming than it is for straight digital devices, even VLSI parts. But emerging markets such as cellular telephones, image compression and desktop video, with their peculiar algorithms and frequency requirements, are giving birth to mixed-signal ICs which may stress the capabilities of the most advanced mixed-signal testers.

To be sure, automatic test system manufacturers such as Teradyne (Boston, MA) and LTX (Westwood, MA) have evolved modular equipment that can be configured for a variety of analog and mixed-signal part types. "We test anything from dc and precision through 4-GHz RF," says Randy Kramer, Teradyne's manager of applications engineering. "We also test power components and low-current devices—things that produce current in the femtoamp range."

But even if the parametrics of the device fit well within the capabilities of the tester, providing a definitive production screening test for a complex device that doesn't take hours will remain a challenge. An 18- or 20-bit audio A-D converter, for example, generates 262,144 (2^{18}) samples over its full range. "That's a ton of samples," suggests Kramer, and they'd take an "outrageous amount of time" to collect.

As with audio converters, many mixed-signal devices require a trade-off between the thoroughness of a test suite and the time it takes to complete it. An overly elaborate production test suite can delay shipment and raise costs, but an incomplete test runs the risk of sending a faulty device into the field.

Deciding what to test for and how to conduct the tests is still something largely left up to test engineers after the part has been built. Unlike digital IC design, which is increasingly supported by design-for-test tools and built-in self-test (BIST) logic cells, DFT for analog and mixed-signal is still very much in its infancy. Just emerging now are the first tools bringing models of IC test systems into the simulation environment, but the success of these tools will depend on more than just fuller model libraries. An understanding of the strategy used to verify the functionality of a particular part on the production line will also be required. Many of these analog and mixed-signal test issues are bound to get attention when the International Test Conference (ITC) convenes in Baltimore later this month (September 20-24).

Computer peripherals lead demand

Most ATE manufacturers identify computer peripherals—disk drive controllers and read channel ICs, fax/modem chips and network transceivers—as the predominant part types mixed-signal IC vendors want to test. The small size and light weight demanded by the notebook computer market is putting strong demands on IC vendors for high levels of integration—what Mike McCaffrey, LTX's marketing manager for communication and computer peripheral test systems, calls "circuit consolidation." But these demands put additional stress on test systems.

New read channel ICs, for example, what McCaffrey calls "disk drive combo chips," include RF filters, pulse peak detectors, data separators, and encoder/decoders (such as the Endec). The data separator converts the FM waveform into two serial pulse streams (one for the clock, the other for data), while the Endec decodes a particular data compression scheme, such as Huffman coding or, more typically, run length limited encoding.

The question is: How does one test such a device? The traditional test paradigm requires the tester to provide a clean stimulus and then a measurement of how the device-under-test (DUT) responds. In principle, you inject some carefully chosen analog waveforms and see whether the read channel produces the correct data stream.

Complications created

But the new combo chips create several complications, as well as imposing a new set of specifications which must be verified. For example, McCaffrey says that the tester must gauge the jitter on the read data

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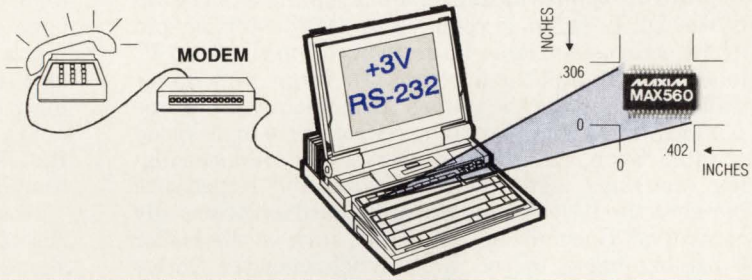

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CIRCLE NO. 95

I/O—that is, the amount of spontaneous phase shift in the serial data pattern emerging from the combo chip. LTX uses a time analyzer instrument specifically designed for jitter measurements; it will resolve a time interval as small as 5 ps. For the test to be valid, however, the test system must ensure the integrity of the signal going in, as well as the integrity or cleanliness of the measurement.

Among the test problem McCaffrey identifies are the transmission line effects produced by the combination of very high speed and small-outline packaging. While testers have evolved a complete stimulus/response measurement system for every pin of the DUT—what is referred to as a tester-per-pin architecture—variable interconnect lengths from IC lead to test probe can result in large impedance differences among the probes. This means that probe pins will show widely varying responses to high-speed stimuli. Even a 24-Mbit/s data rate can produce ringing (spurious signal reflections) if the impedance between the IC leads and the probe card isn't carefully controlled. Specialized test heads, such as the HiPer Card extension to the LTX Synchromaster Series testers, minimize the impedance mismatch between the probe card and the DUT by controlling the interconnect length between probe pins and IC leads. Since the pin drivers must handle a 15-pF load, there's a need for high drive capability within a small space, sometimes requiring the test head to be supported with liquid cooling.

Another problem is the shift from 5-V to 3-V devices. While read channel ICs are frequently derated for low-voltage operation, disk drive designers will still look for 24- or 30-Mbit/s data transfer rates. "We test at speed," says McCaffrey, "even at low voltage." The combination of high speed and low voltage will increase what McCaffrey calls the "noise margin" for the part. The ratio between the data signal and the noise level of the IC becomes smaller, making it increasingly difficult to distinguish data and noise, both in the disk drive and the test environment.

Teradyne's Kramer makes a distinction between functional testing, in which the device is treated as a system in its environment, and component testing, in which the device is treated as an isolated element with a series of ac and dc specifications attached to it. The CCITT standards, for example, specify a number of necessary tests, largely component tests for verifying the operation of telecommunication parts. Teradyne's recommendations, suggests Kramer, typically attempt to strike a balance between functional and component testing.

New test strategies

Kramer sees current demands for mixed-signal test systems being driven by the needs of disk drive, telecommunications and smart-power IC manufacturers. There are also increasing needs among manufacturers of radio frequency and cellular telephone components. While Teradyne's A500 series machines will test "every frequency from audio to RF," Kramer believes that new part types will require new algorithms to resolve the paradox between the quality of the test and its throughput in production.

One example is mathematical oversampling, in which detailed information on a data converter is derived from a relatively small number of captured data samples. While the technique requires careful control of the frequency of the stimulus, information about the linearity of, say, an 8-bit data converter, which produces 256 output codes, can be mathematically interpolated from fewer than 32 samples.

Another example is the chirp-Z transform, an algorithm for converting sampled data from the time domain to the frequency domain that works much faster than either the fast Fourier transform or the discrete Fourier transform. Frequency-domain measurements are required to understand the noise, phase shifts and jitter produced by disk drive ICs, high-speed palette D-A converters and ISDN templates.

Another test system vendor, Schlumberger (San Jose, CA), believes that while the predominant mixed-signal test systems are primarily analog testers with some sort of digital capability, it may be useful to harness a digital tester for certain types of mixed-signal parts. Telecommunications chips, for example, especially those which perform a DSP function, have more of a "digital heart," argues Schlumberger marketing manager Nadim Ahmad

Analog emulation devices

These are the kinds of devices that VLSI Research describes as "digitized analog"—and that I've referred to as analog emulation. They're typically devices that use digital techniques to perform an analog function. Ahmad calls them ISPs (for integrated signal processing), and he believes their use will grow by 23 to 25 percent per year. Like modems, faxes, cellular telephone ICs, and feature phones, ISPs need to be exercised digitally—with 1s and 0s.

Ahmad agrees with the analog test set manufacturers that such devices must be able to depict noise thresholds and jitter, but that it's also important to synchronize analog and digital test elements. One way of accomplishing this, he suggests, is to build thorough mixed-signal simulations and use them to inform the test routine.

Currently, there's no complete automatic test generation package for analog and mixed-signal ASICs, but there are very promising developments. Most prominent is the Dantes testability analyzer introduced recently by Cadence Design Systems (San Jose, CA). Dantes offers the ability to simulate mixed-signal test procedures—in a sense, to develop production tests in the design environment. The analyzer, used in combination with the Schlumberger ITS 9000-MX, makes mapping a mixed-signal IC simulation into a usable test procedure much easier.

Stephan Ohr is president of Indian Forest Research, and editor of the monthly newsletter, Mixed Signals.

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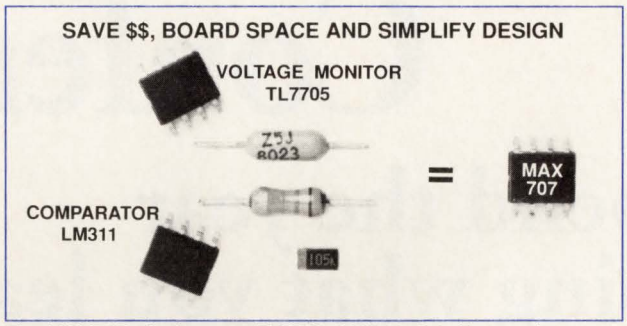

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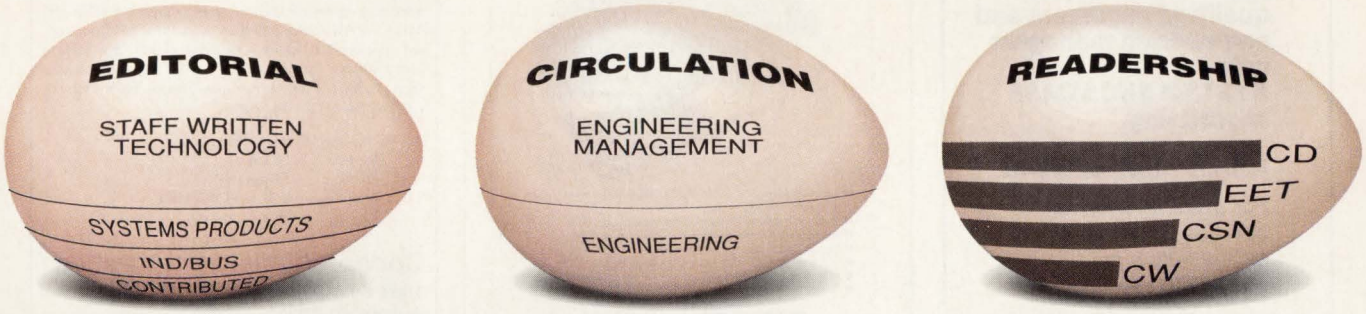

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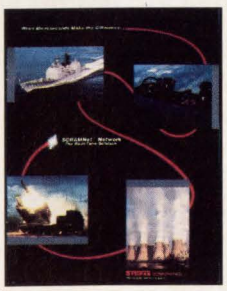

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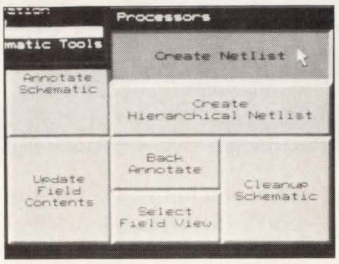

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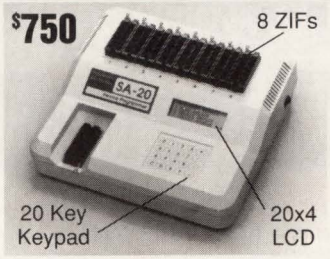

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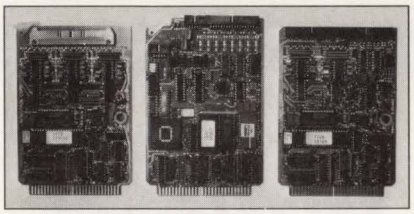

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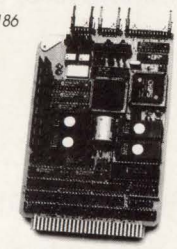

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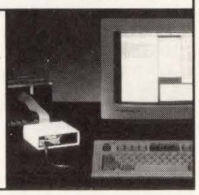

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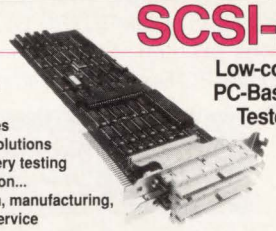

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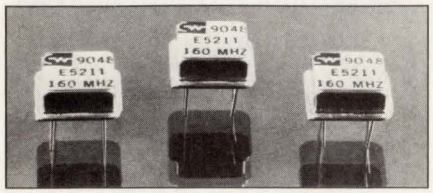

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FEBRUARY *Buscon West, EDAC/Euro ASIC*	Bridging the buses	•Software tool integration •ICs for desktop video	Flash EEPROMs	Process control	
MARCH *RISC '93, PCB Design*	Memory architectures	•Multithreaded operating systems •PC-Based CAE/CAD Tools	SCSI host adapter boards	Data acquisition	•Input devices •Printers & output devices
APRIL*	*EMBEDDED COMPUTER CONFERENCE (ECC)** SHOWGUIDE*				
ECC	PC/AT architectures in embedded applications	•Developments in 3-V ICs •Evaluating simulation strategies	Device programmers	Peripherals	
MAY	*SPECIAL REPORT ON FUTURE COMPUTING: Virtual Reality*				
Comdex Spring, CICC	New applications for DSP	•Benchmarking programmable devices •Bus standards	Video D–A converters	Portable computers	•Networking interfaces, standards & components
JUNE* *DAC*	High–level synthesis and architectural design	•Small form factor VM •Data comp standa	Ultra–fast SRAMs	Graphics	
JULY *Fuzzy Logic '93*	Advances in IC packaging	•Int • C, neural upd	–time kernels and operating systems	Imaging	•Display devices & monitors
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ADVERTISER	PAGE NO.	CIRCLE NO.	**IDA NO.
Mercury Computer Systems	45	33	
Micro Industries	24-25	21	
Micro Industries	87	59	
Micro-Sys	163	180	
Micron Technology	56	42	
Microware Systems Inc.	39	27	
†Military & Aerospace Electronics	48	77	
Military & Aerospace Electronics	149	88	
Mitsubishi Electronics	143	85	
Mitsubishi Electronics	50	37	
Mitsubishi Electronics	68-69	48	
MIZAR	64	45	
Mupac Corporation	41	28	
N			
National Semiconductor	8-9	–	
NEC Electronics, Inc.	59	43	
Needham's Electronics	163	177	
Nohau Corporation	162	167	
O			
Oasys, Inc.	51	38	
Odetics	140	188	
Omnibyte Corporation	80A	119,120	
OrCad Systems	163	176	
Orion Instruments	90-91	61	
P			
Pentek	93	62	
PEP Modular Computers, Inc.	120	75	
Phase Three Logic	164	185	
Pinnacle Data Systems	18	13	
PRC Inc.	162	171	
Q			
Quantum Software Systems, Ltd.	53	40	
R			
Radstone Technology	43	30	
Rapid Systems, Inc.	44	31	
Robotrol Corporation	163	179	
RTMX, Inc.	18	14	
S			
SBE, Inc.	73	50	
Signal Processing Group	164	186	
Star Semiconductor	CV2	1	
Synergy Microsystems	13	7	1042
Synergy Microsystems	2	3	
Systran Corporation	163	175	
T			
Teknor Microsystems	46	34	1028
*Texas Instruments	65	–	
Texas Microsystems, Inc.	32	24	
Themis Computer	15	8	
Toronto MicroElectronics, Inc.	79	53	
Trenton Terminals, Inc.	172	102	
Truetime Inc.	154	92	
U			
Ultraview	140	190	
V			
VHDL International	94	63	
VenturCom	52	39	
Vigra, Inc.	134	81	
Vista Controls	117	73	1052
VMETRO, Inc.	66	46	
VMETRO, Inc.	85	58	
W			
Wescon '92	151	89	
Brian R. White Company, Inc.	16	9	
Wind River Systems	103	68	
X			
Xycom	109	70	
Z			
Z-World Engineering	162	172	
Ziatech Corporation	CV3	103	
Zwick Systems, Inc.	163	182	

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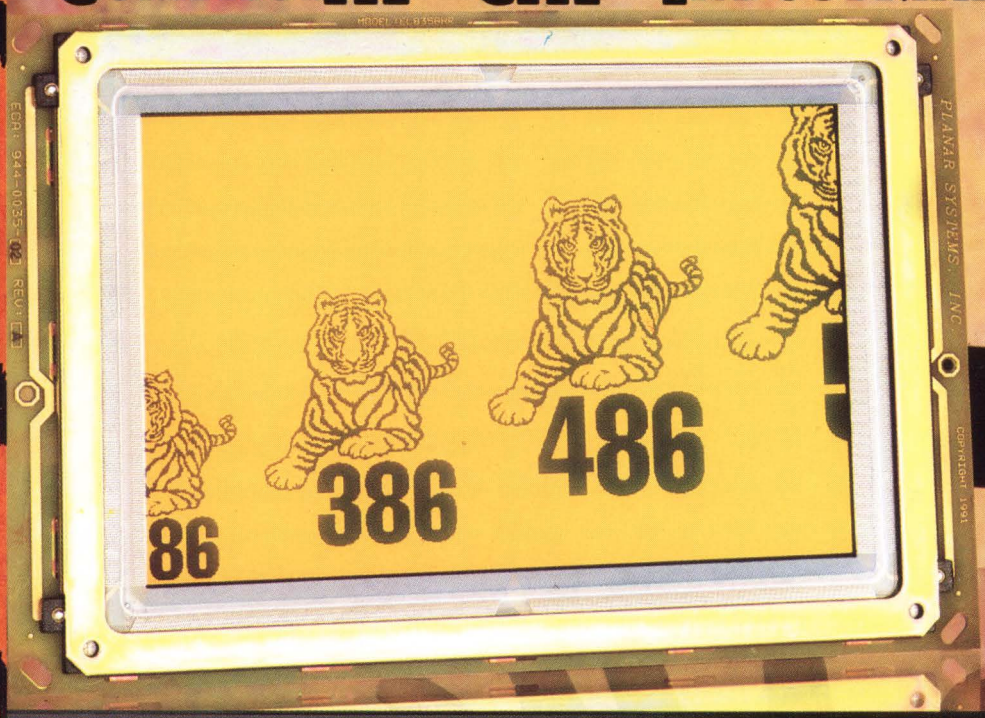

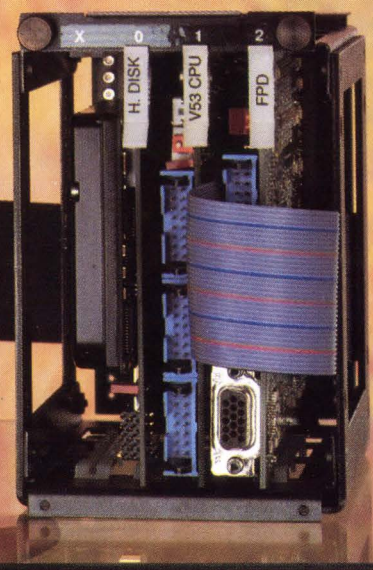

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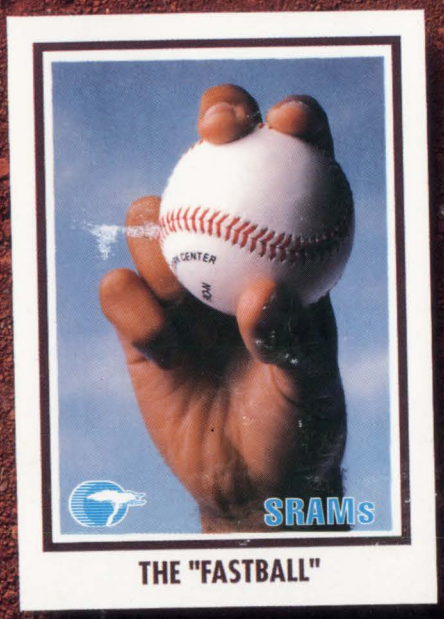

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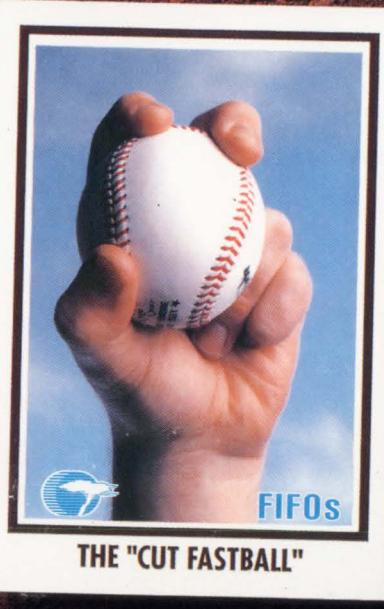

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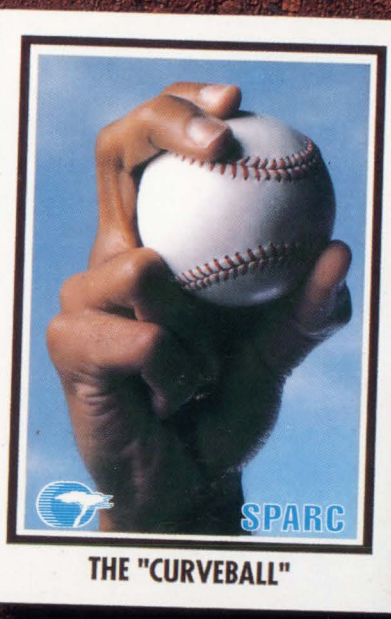

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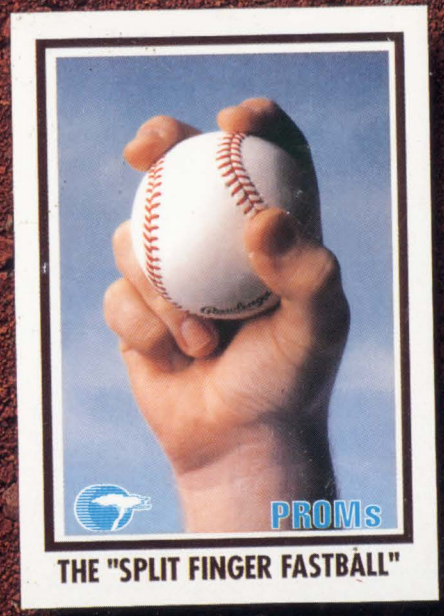
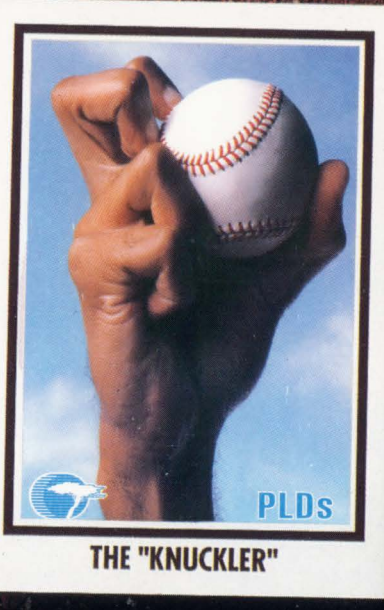


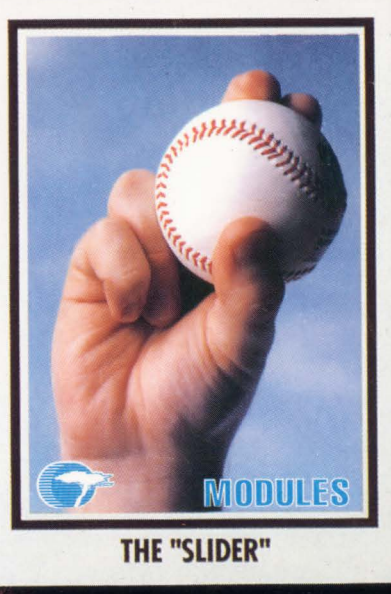
THE "SPLIT FINGER FASTBALL"

The fastest access in every PROM density. Broad options make these hard to beat.



THE "KNUCKLER"

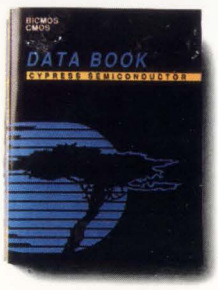
PLDs allow crafty designers to mix Gate Array density with 40 MHz performance; even support 125 MHz state machines.



THE "SLIDER"

Just when you thought the board was full, multichip modules slip 1 MB SRAMs into a 1/8" space.

PLAY HARDBALL WITH THE COMPETITION.



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