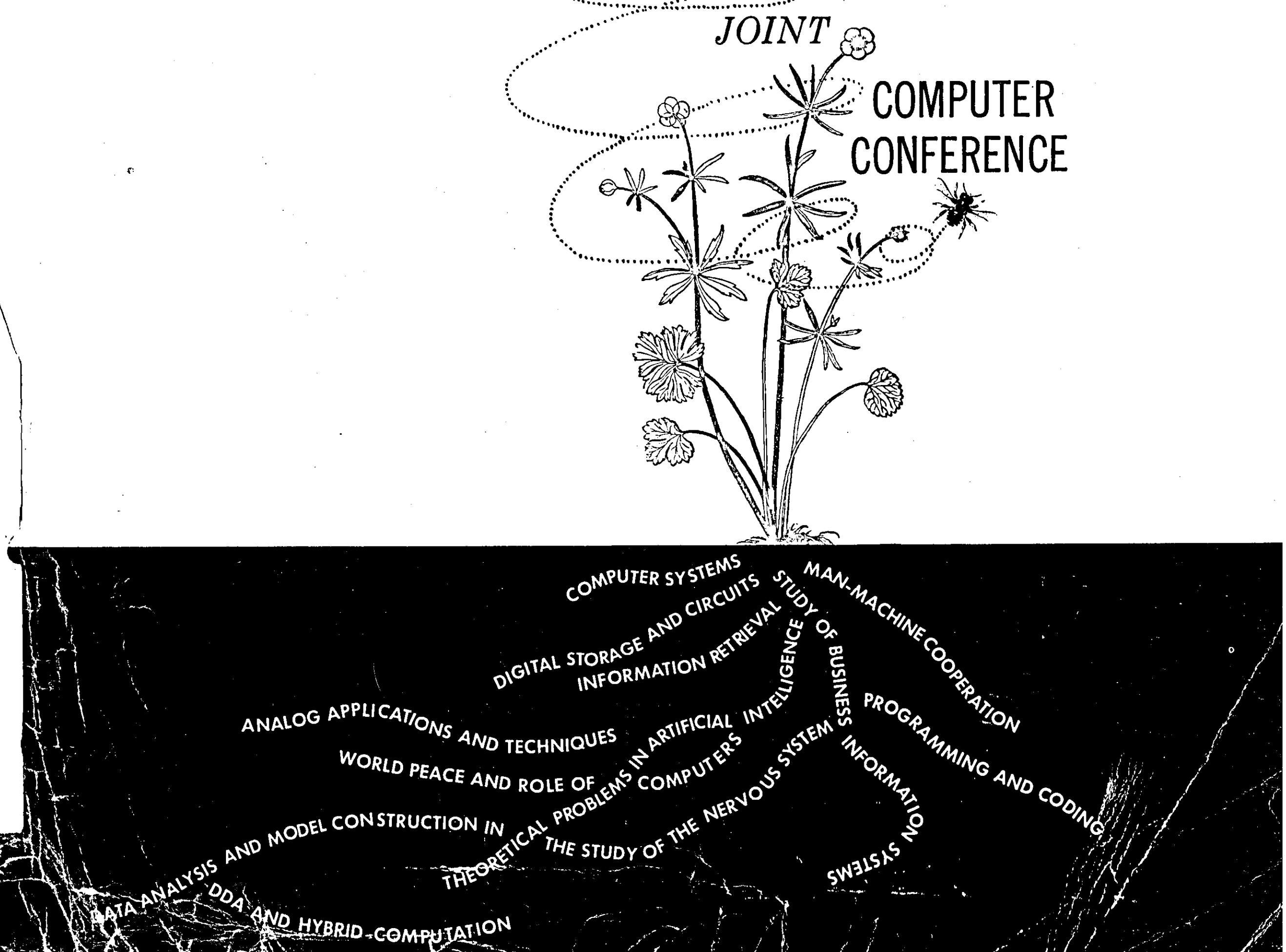
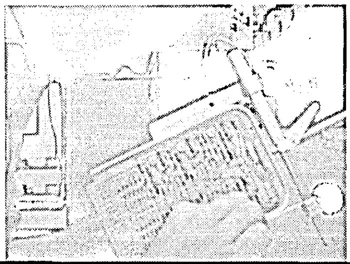
62

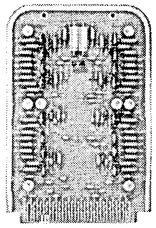
®

April

SPRING *JOINT* COMPUTER CONFERENCE

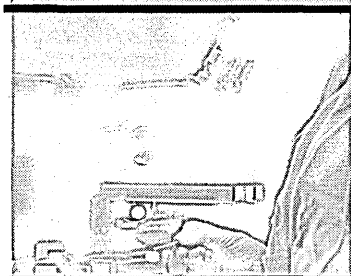


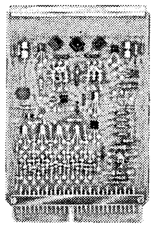




S-PACS

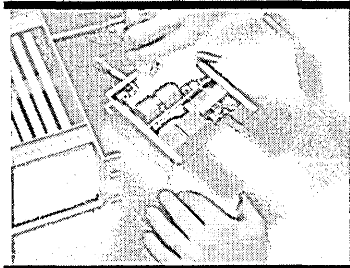
One and five megacycle digital logic modules possessing outstanding customer acceptance based upon quality, reliability, convenience of usage, and economy. New 28-page S-PAC catalog describes entire line plus planned new product additions.

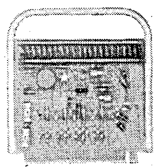




H-PACS

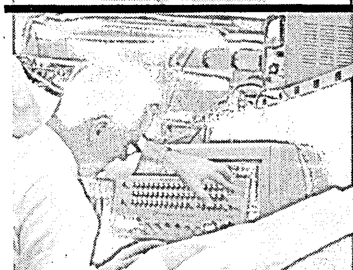
Ultra high-speed digital logic modules which operate at clock frequencies to 16 megacycles with exceptional fan-in and fan-out ratios. H-PACs utilize ordinary wiring techniques. They do not require twisted pairs or shielded cabling. Twelve-page Catalog H-1 provides comprehensive technical data.

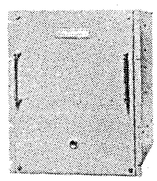




T-PACS

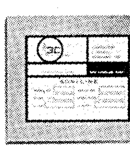
One megacycle synchronous-logic Series T modules feature plugboard interwiring, complete independence from timing or phasing problems, and low impedance outputs with large fan-out ratios plus low power consumption. Twelve-page Catalog T is completely descriptive.





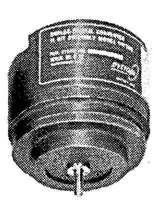
RANDOM ACCESS MAGNETIC CORE MEMORIES

New series of TCM Magnetic Core Memories offer access times as low as three microseconds, unexcelled engineering and construction, and outstanding reliability. TCM brochure available on request.



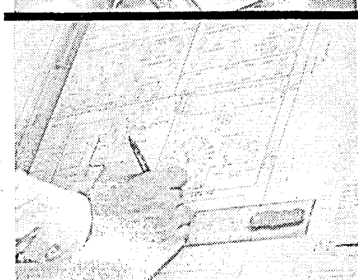
SONILINES

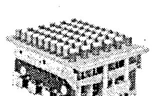
Soniline magnetostrictive wire delay lines are distinguished by top quality construction and concise operating performance. Many standard modules with delays tailored to customer specifications are available for delivery in less than 30 days. Four-page Soniline brochure offers more detailed information.



DICOTRONS

Dicotron precision optical shaft angle encoders are available with accuracies up to 16 bits per revolution. Also available are sine cosine encoders, incremental encoders, and special-coded custom engineered units. Twelve-page Dicotron catalog and supplementary bulletins are available on request.

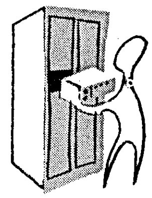




CODE BAR SWITCHES AND KEYBOARDS

These mechanical input devices provide direct conversion of key depressions into standard or special binary coded outputs per digit. Ruggedized and environmental models are available on order. Microswitch output contacts provide high reliability and freedom from dust or moisture. Descriptive literature contains detailed information.

CIRCLE 4 ON READER CARD



3C's array of digital building blocks includes the product families shown in column form at the left:

QUALITY PRODUCTS FOR DIGITAL DESIGNERS

New products are continuously being added as the result of extensive programs of research and development. These programs are maintained at a rate consistent with the most stringent requirements of sound engineering, quality manufacturing, and ultimate "in-systems" reliability. If the requirements of your system indicate this kind of approach to product development and manufacture, we earnestly invite your consideration of our products and special design services. Your direct inquiry will receive prompt attention.

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COMPUTER CONTROL COMPANY, INC. 3C

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WESTERN PLANT:
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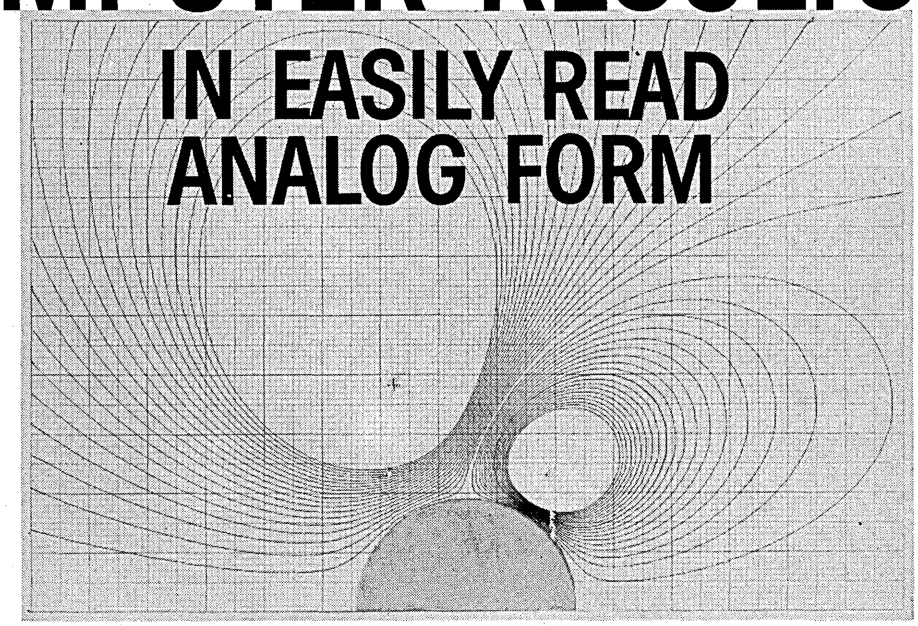
PLOT COMPUTER RESULTS IN EASILY READ ANALOG FORM

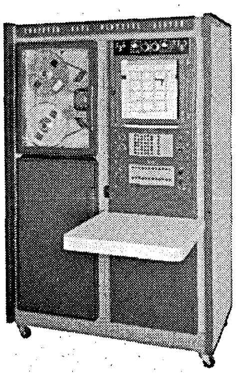


With Dymec Data Reduction Systems

You can make X-Y or strip-chart recordings from digital data at rates of up to 100 conversions per second with Dymec digital-to-analog conversion techniques. Data recorded at computer speeds on magnetic tape, punched cards or punched tape can be automatically plotted at slower speeds for visual examination and analysis. Additional data can be entered manually with an auxiliary keyboard.

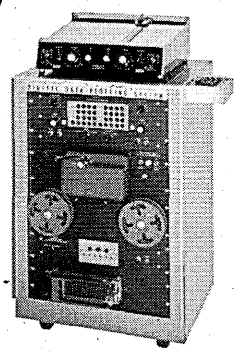
Two moderately priced Dymec Data Reduction Systems are available. One extracts data from magnetic tape; the other is used with punched cards, punched tape or typewritten records. These systems include three types of digital-to-analog converters which are also available separately or as building blocks for custom designed data reduction systems.

DY-6575, A complete system, magnetic tape to X-Y recording



You can increase the efficiency of your high-cost computer with the DY-6575 Magnetic Tape Plotting System. Tape written at 75 inches per second on the computer is read at 3 inches per second for recording. The Dymec system makes 100 conversions/second from digital data on magnetic tape for continuous plotting on a Moseley Autograf Recorder. Accepts binary or BCD inputs, includes search mode and visual display for check-out or calibration. Overall accuracy of plotting system, ±0.2% of full scale. Complete system about $29,750.00.

DY-6242, A complete system, punched cards, punched tape or keyboard to X-Y recording



Plotting speeds of 50 points per minute with punched cards and 80 points per minute with punched tape are yours with the DY-6242 Plotting System, which also is supplied with a 10-key serial entry keyboard for recording tabular data. Overall accuracy of plotting system, ±0.2% of full scale. The Dymec system consists of a digital-to-analog converter, a tape reader and a Moseley Autograf Recorder with character printer. Complete system about $8,700.00.

Three digital-to-analog conversion building blocks

Dymec Model 2742 Digital Data Translator accepts data from IBM cards, perforated paper tape or a serial keyboard and converts for recording up to four decades of data plus a sign for each axis. The transistorized instrument provides a front-panel display for monitoring translator contents, plus controls for calibration, single cycle or automatic operation. D/A conversion accuracy, 0.1%. Price, including manual keyboard, about $4,500.00.

Dymec Model 2743 Series Digital/Analog Converters accept binary, binary-coded-decimal or decimal data for conversion to analog voltages. Up to four channels in one unit. Each can process up to 12 bits of binary, up to 4 decades BCD or decimal data. Price about $3,800.00.

Dymec Model 2744 Series Magnetic Tape Units include tape control unit and tape converters for recording binary and binary-coded-decimal data. The control unit, Model 2744A, accepts data from tape and provides an output to drive one of the converters, Model 2744B for binary data and Model 2744C for BCD data. Price, about $14,700.00, including 2744B or 2744C Converters.

Data subject to change without notice. Prices f.o.b. factory.

Call your Dymec/Hewlett-Packard representative or write direct for information on Dymec digital-to-analog conversion capabilities.

Visit Dymec Booth 903, Spring Joint Computer Conference

DYMEC

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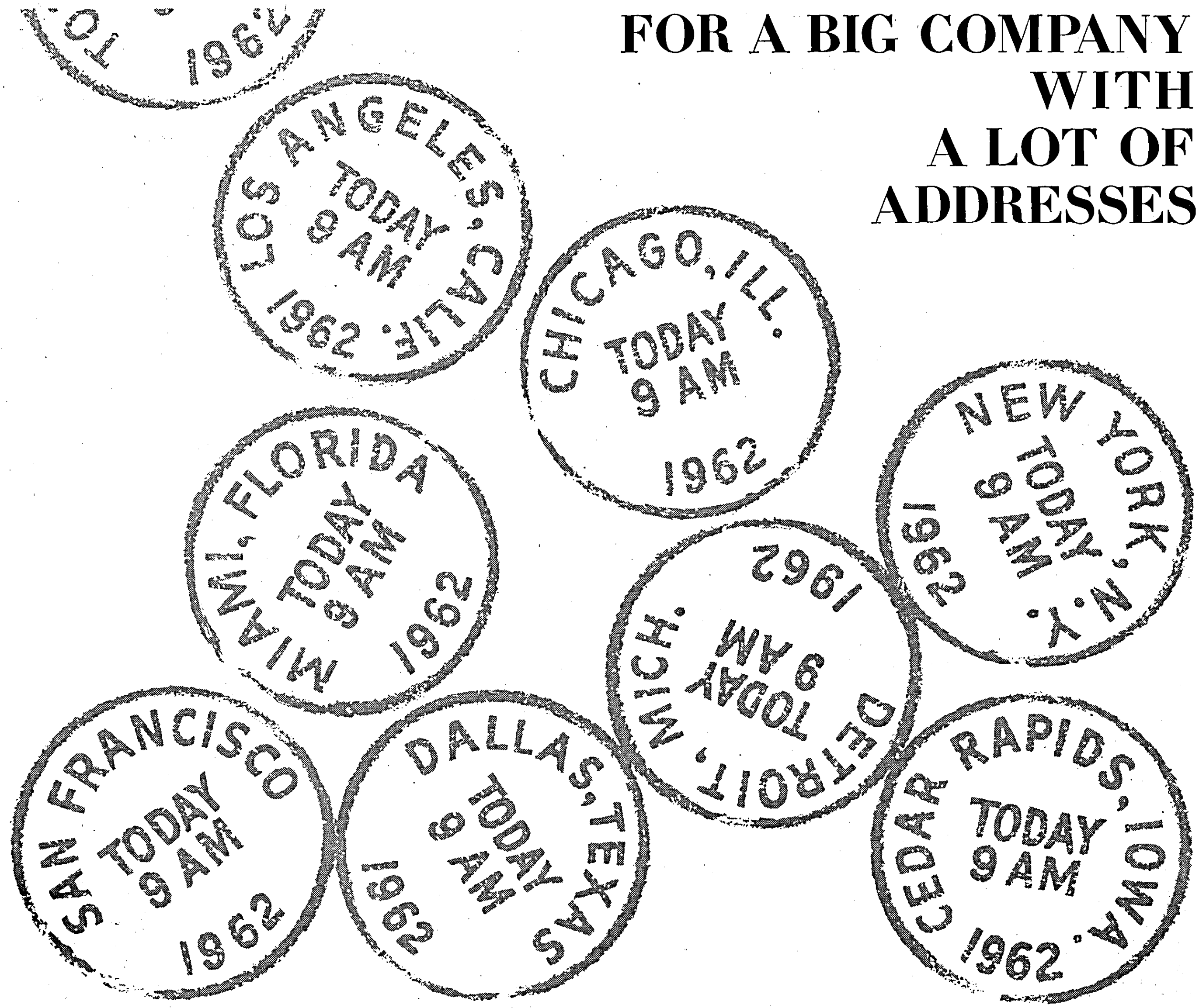
FOR A BIG COMPANY WITH A LOT OF ADDRESSES



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Today, some of the nation's most widely scattered organizations have the fastest reactions. They gather facts and transmit reports from coast to coast as quickly as most companies communicate from office to office in the same plant. Even outlying locations have instant access to the most powerful computers. □ *Kineplex makes it possible.* □ This patented data transmission technique from Collins is the speediest way to move information over a telephone line. Kineplex terminals handle digital data at rates up to 13,500 words a minute. Using wireline or radio, they form a fast, reliable information network that can span thousands of miles to link a company's plants and computers. □ The speed, dependability and adaptability of Kineplex has established Collins as a leading source of equipment for the new age of data communication. COLLINS RADIO COMPANY, Communication and Data Systems Division, Dallas, Texas.

COLLINS

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DATAMATION 62

the automatic handling of information

volume 8, number 4

Staff

Feature Articles

Departments

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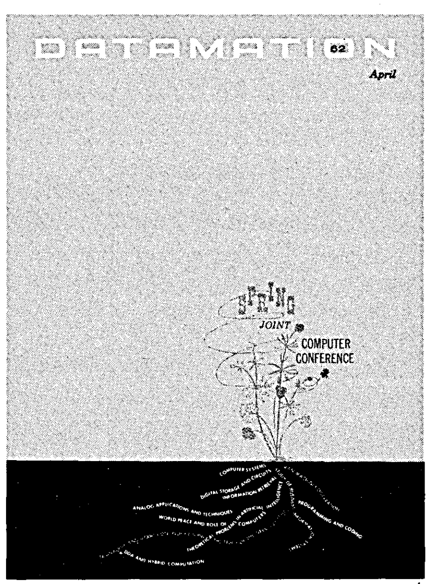

Cover

While delegates to next month's Spring Joint Computer Conference may not find spring flowers adorning the streets of San Francisco, the roots of the conference will be very much in evidence as principal sessions for the SJCC. Complete details for the May 1-3 conference may be found in a special section beginning on page 55. Cover design is by *Datamation* Art Director Cleve Boutell.

Circulation audited by Business Publications Audit — BPA

Member, National Business Publications — NBP

DATAMATION is published monthly on or about the tenth day of every month by F. D. Thompson Publications, Inc., Frank D. Thompson, president. Executive Circulation and Advertising offices, 141 East 44th St., New York 17, N.Y. (MUrray Hill 7-5180). Editorial offices, 10373 West Pico Blvd., Los Angeles 64, Calif. (BRadshaw 2-0817). Published at Chicago, Ill. Accepted as controlled circulation at Columbus, O. Form 3579 to be sent to F. D. Thompson Publications, Inc., 201 N. Wells St., Chicago 6, Ill.

important DATES

• The 1962 Spring Joint Computer Conference, sponsored by the American Federation of Information Processing Societies, will be held May 1-3 at the Fairmont Hotel, S.F.

• "Electronic Information Display Systems" is the subject on an institute to be held May 21-25 at the American University, Wash., D.C.

• A conference on Self-Organizing Systems will be held on May 22-24 at the Museum of Science and Industry, Chicago. It is co-sponsored by the Information Systems Branch, Office of Naval Research, and the Armour Research Foundation.

• A Symposium on Mathematical Programming sponsored by the Graduate School of Business of the University of Chicago, the ACM, and USAF Project RAND, will be held June 18-22 at the University of Chicago, Chicago, Ill.

• The Ninth Annual Symposium on Computers and Data Processing sponsored by the Denver Research Institute of the University of Denver is scheduled for June 27-28 at the Elkhorn Lodge, Estes Park, Colorado.

• The 1962 Rochester Conference on Data Acquisition and Processing in Medicine and Biology is set for July 17 and 18 for the Whipple Auditorium, Strong Memorial Hospital, Rochester, N.Y.

• The 1962 WESCON will be held Aug. 21-24 in the California Memorial Sports Arena and Statler-Hilton Hotel, Los Angeles.

• The 1962 IFIP Congress is set for Aug. 27-Sept. 1 in Munich, Germany.

• The ACM National Conference will be held Sept. 4-7 at the Onondaga Country War Memorial Auditorium and Hotel Syracuse, Syracuse, N.Y.

• The 3rd annual Symposium on Switching Circuit Theory and Logical Design will be held Oct. 7-12 in Chicago, Ill. under the sponsorship of the AIEE Computing Devices Committee.

• The 1962 Fall Joint Computer Conference will be held Dec. 14-17 at the Bellevue Stratford Hotel, Philadelphia, Penna.

ODDS ARE NOTHING CAN

With this surprisingly versatile system, the EAI Series 3440 DATAPLOTTER®, you can plot your digital or analog data in easy-to-read, easy-to-interpret graphic form. Far more accurate than hand plotting and many times faster, the DATAPLOTTER will convert virtually any input from almost any computer, digital or analog, into plots as large as 45 by 60 inches. It will plot from magnetic or punched paper tape, punched cards, manual keyboard or analog-type signals. It will seek plot starting point and stop automatically at a preselected value. Output modes, include point, symbol or continuous line. The host of features includes solid state reliability, speeds to 4500 line segments per minute, fully automatic commands and dial control data selection. Full information on this new standard in digital plotting equipment may be obtained by writing for Bulletin DP 6188.

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CIRCLE 9 ON READER CARD

letters

authorship denied

Dear Sir,

Mario *did* seem a little irritated, didn't he?

I can't possibly start the first computing comic strip. That was done many years ago, at the RAND Corporation!!! The hero was a Chebyshev polynomial and the creator, Cecil Hastings.

HERB GROSCH
Bern, Switzerland

chiding the kiddies

Dear Sir,

The ACM, DATAMATION, Rubin, and Grosch all deserve to be severely castigated for their childish behavior. The multi-million-dollar a year computer field certainly could use two publications (with or without biases). However, if these journals have nothing better to do than throw brickbats at one another, then the time has come for one or the other (or both) to retire rather than contribute to the technical literature "explosion."

Enough of this nonsense, children! Roll up your sleeves, and get down to "brash tacks." There is a lot of useful work to be done.

LEWIS C. CLAPP
Arthur A. Little, Inc.
Cambridge, Massachusetts

gamesmanship

Dear Sir,

The article on "How To Make A Computer Appear Intelligent" which appeared in the February issue stimulated a number of requests for further information. We hope that a single letter may be responsive to all separate inquiries.

The game was programmed on a Transac S-2000 computer located at the General Electric Atomic Power Equipment Department in San Jose, California. Since the program was purely experimental, no attempt was made to achieve program efficiency. Length of program and running times are therefore of no interest. Input-output is via console typewriter. The player enters the coordinates of his move (i, j) into the typewriter, the machine then responds with its own move. It is up to the player to have at hand coordinate paper on which to plot his and the machine's moves. In addition, the machine types out a diagnostic of each move consisting of the high and low position value moves it could have made, the value of the move it did make, the highest value move open to the player, and the value of that move. This diagnostic information could have been put on tape for post mortem analysis. As it was, it was not revealed to the player in that the output format was not explained to him. The time taken by the machine to make a move was on the order of a few seconds, i.e. well within "psychological" time.

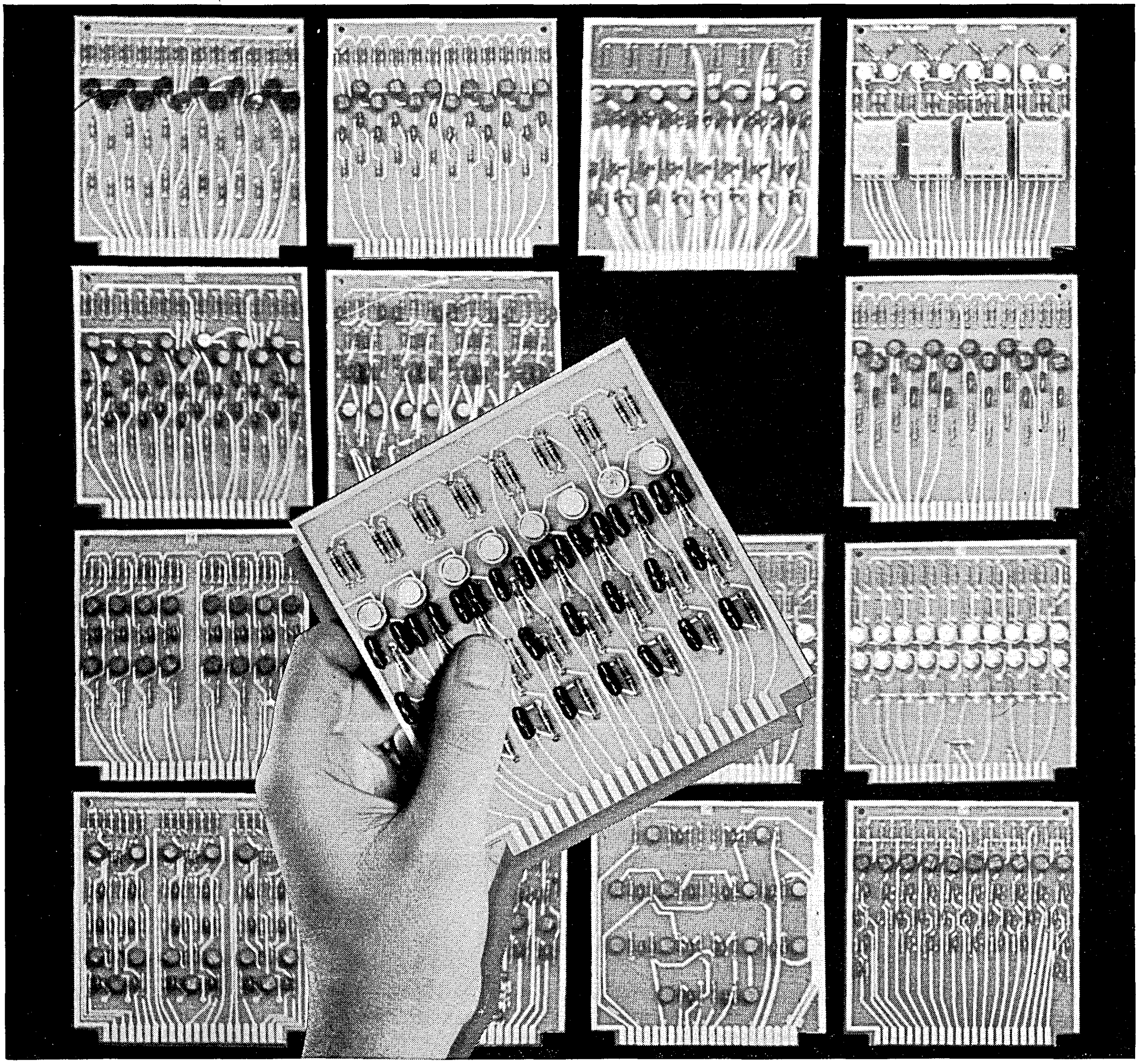
The paper mentions a few modifications which could (perhaps should) be made in the program. None of these were actually made. In fact, the program has been permitted to become dormant except that the operators on the subject machine occasionally amuse themselves with it in lieu of reading Davis on computability.

It seems to us now that the most important modifications which we would make on the program, were we to seriously pursue it from this point on, would be the following:

1. The introduction of look-ahead. This could easily be done if the program were written in a list language. Then position evaluations, tentative moves, etc., could be pushed down on stacks, all of which could then be popped up when the final move was decided upon. The important problem which would have to be solved is the usual one in heuristic programming; namely, that of deciding on how to pare the decision tree, i.e., which moves to follow, which to abandon and at what depths.

2. As was mentioned in the paper, it seems fairly clear that really strong moves, i.e. moves which subsequent post mortem reveal to be the decisive ones for the player, generally have the characterization that they have low position values from the point of view of the algorithm. Moves of this type could be identified. The machine response to such moves should then be purely defensive. In particular, candidates for response to such moves should be restricted to positions with which the subject move is *associated* (see text). It would appear that the algorithm given in the paper is sufficient to lead to a machine win in the absence of such unorthodox moves on the part of the player. Perhaps a new set of heuristics should be brought into play when such moves are encountered.

J. Weizenbaum and
R. C. Shepardson
Computer Laboratory,
General Electric Co.
Sunnyvale, California



Take this 1 mc Solid State Printed Circuit, for example . . .

Intermountain Branch of Curtiss-Wright Electronics Division designed and manufactured it to meet exacting standards of quality, reliability and performance in a wide variety of digital logic systems. These precision built 1 mc units are available in a broad selection of standard "off-the-shelf" circuits, or Intermountain will custom design and manufacture solid state printed circuits and systems to your specifications.

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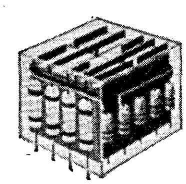
Write for information and prices on standard units, or a quotation on your specific requirements.

NEW—MAXPAK® Digital Modules are welded, high density modules, encapsulated in HEATCON® high conductive plastic. Offer substantial savings in space and weight, flexibility and reliability at modest cost. Standard units available, or your circuits can be packaged to specification. For complete information, write: Advanced Miniaturized Electronics, Inc., 55 Kearney Rd., Needham Heights, Mass.



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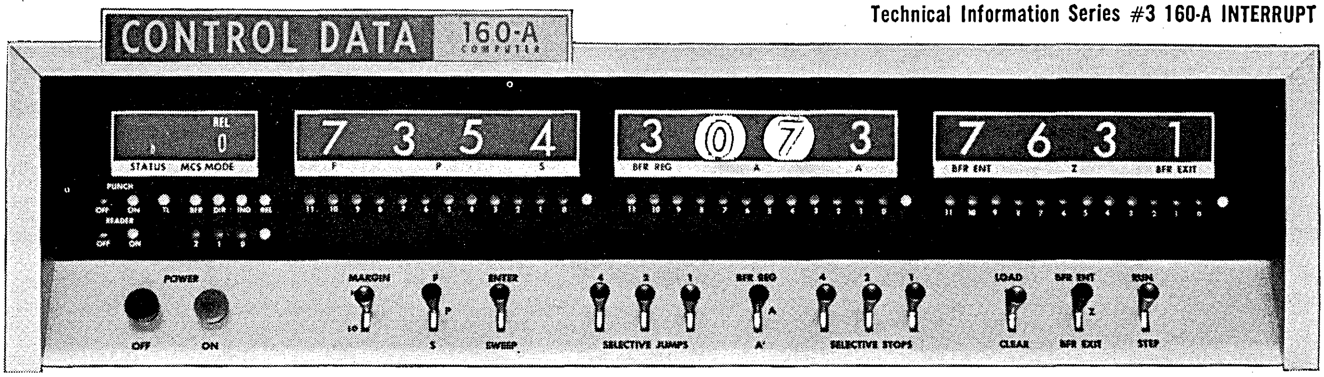


GREEN LIGHTS INDICATE INTERRUPT STATUS.

NEW CONTROL DATA 160-A COMPUTER

Desk-Size Computer with Large Computer Capabilities

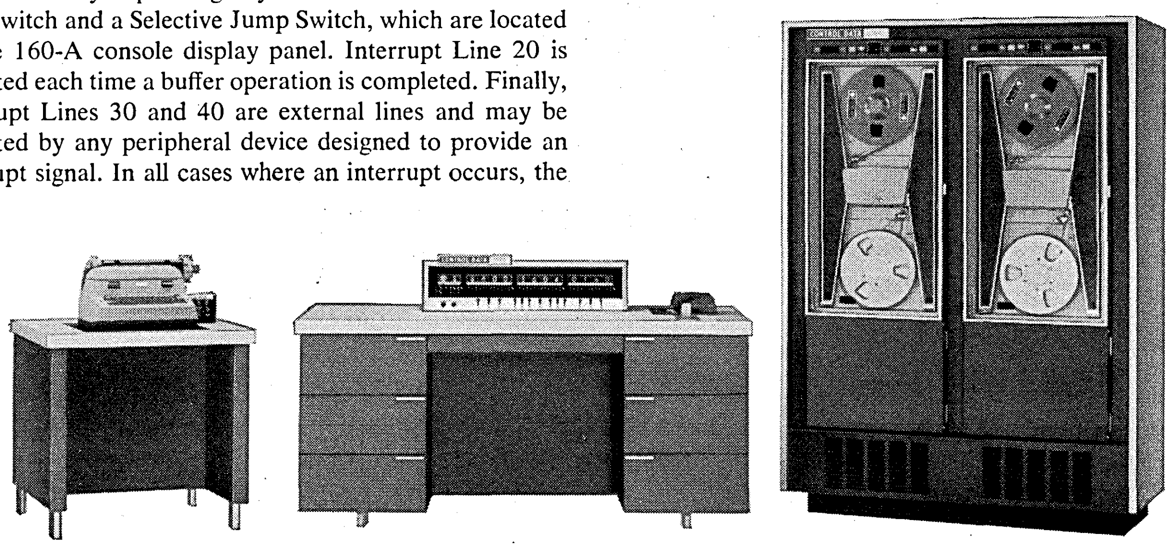
In evaluating desk-size computers, the flexibility and capability of the computer to perform interrupt functions is of great importance. Similar to the interrupt feature employed in many advanced, large-scale computers, the 160-A Program Interrupt allows the normal program sequence to be interrupted by various external conditions . . . such as a peripheral equipment completing its function, operator action, and end-of-buffer sequence. Few desk-size computers on the market today have this capability.

The 160-A has four interrupt lines: two internal and two external. When an interrupt signal occurs on one of these lines, the computer executes a special RETURN JUMP instruction to one of four fixed memory locations, depending upon the line generating the interrupt.

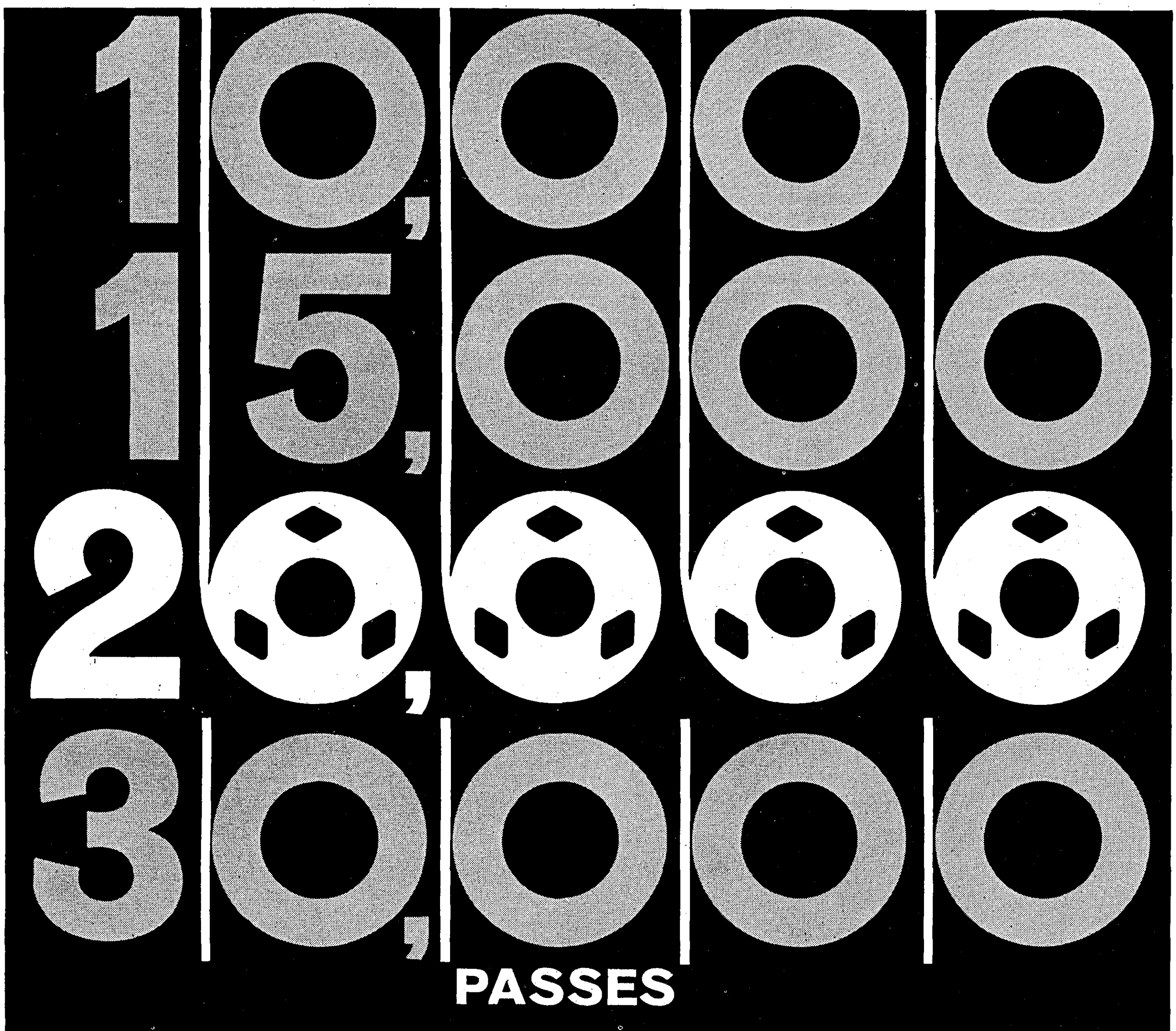
For example, the operator can activate Interrupt Line 10 by momentarily depressing any combination of a Selective Stop Switch and a Selective Jump Switch, which are located on the 160-A console display panel. Interrupt Line 20 is activated each time a buffer operation is completed. Finally, Interrupt Lines 30 and 40 are external lines and may be activated by any peripheral device designed to provide an interrupt signal. In all cases where an interrupt occurs, the 160-A executes a special RETURN JUMP instruction to a fixed memory location.

Interrupt signals are recognized in a priority sequence, the lower-numbered lines being recognized first. Thus, where an interrupt occurs simultaneously on Lines 10 and 20, Line 10 will be recognized first. Once an interrupt signal is placed on a line, it remains until recognized or until a console MASTER CLEAR instruction is executed.

A desk-size computer, the Control Data 160-A has the speed, capability, and flexibility of many large-scale computers. For more detailed information about the 160-A Program Interrupt and other standard features, write for Publication #B12-61.



CONTROL DATA CORPORATION
COMPUTER DIVISION
501 PARK AVENUE, MINNEAPOLIS 15, MINNESOTA



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Longer life, flawless performance! These are the advantages of Soundcraft LWD heavy duty/high density tape—the most advanced computer tape available today! In specific tests, Soundcraft new LWD achieved more than 20,000 passes across recording heads with absolutely no sign of breakdown. Heretofore, 15,000 passes had been considered maximum for a heavy duty magnetic recording tape. Soundcraft combines a unique binder system with Mylar*base, producing superior adhesion and cohesion. Result: a heavy duty tape with blemish-free oxide coating, superior surface characteristics and a pulse packing capability that exceeds the requirements of all existing computer systems. Furthermore, Soundcraft LWD more closely approaches the ideal hysteresis curve than any competitive computer tape. Its improved square BH characteristic makes the computer system less susceptible to non-repetitive errors. For an LWD "confidence—level" test in your system, write:

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*DUPONT T.M.

CIRCLE 14 ON READER CARD

BUSINESS & SCIENCE

A COBOL SUCCESSOR??

DETAB-X, DEcision TABles which utilize COBOL-61 as the basic descriptive language, may ultimately supersede COBOL as a new language which combines systems analysis, description and programming into a single function. The DETAB-X language has been developed by the CODASYL Systems Group, part of the Development Committee of the Conference on Data Systems Languages for initial experimentation. A Joint Users Group-sponsored DETAB-62 symposium has been set for June.

At a recent Executive Committee meeting of CODASYL, it was agreed that there will be no COBOL-62 and changes or new features which the Maintenance Committee approves will be used as a supplement to COBOL-61.

ATLAS PROGRESS

As the only giant-scale computer presently commercially available anywhere in the world, DATAMATION correspondents in Great Britain have obtained the following report on sales and operations of Ferranti's Atlas computer.

The first prototype of Atlas is now experimentally on the air at England's Manchester University. Expectations are that it will be fully operative by July. Two other sales of the 10-megabuck machine have been reported; one to the United Kingdom Atomic Energy Authority and another to London University.

At Manchester, Atlas will be used for problems in aircraft design and for applying linear programming techniques to agricultural problems. Manchester also intends to sell time on the computer.

The AEA Atlas has actually been ordered for the National Institute for Research in Nuclear Science (NIRNS). The computer will be housed at the Institute's Rutherford High Energy Lab at Harwell for common use by universities, the AEA, various government departments and NIRNS itself. It is expected to be fully operational by 1964. At AEA, Atlas will be used for a behavior study on plasma mass. Universities will use the Harwell machine in the fields of astrophysics, cosmology, fluid dynamics and molecular structure. The Meteorological office of the British Government may with the help of Atlas, make some progress predicting the unpredictable British weather.

London University plans to put their Atlas to work on calculations on crystal and mechanical

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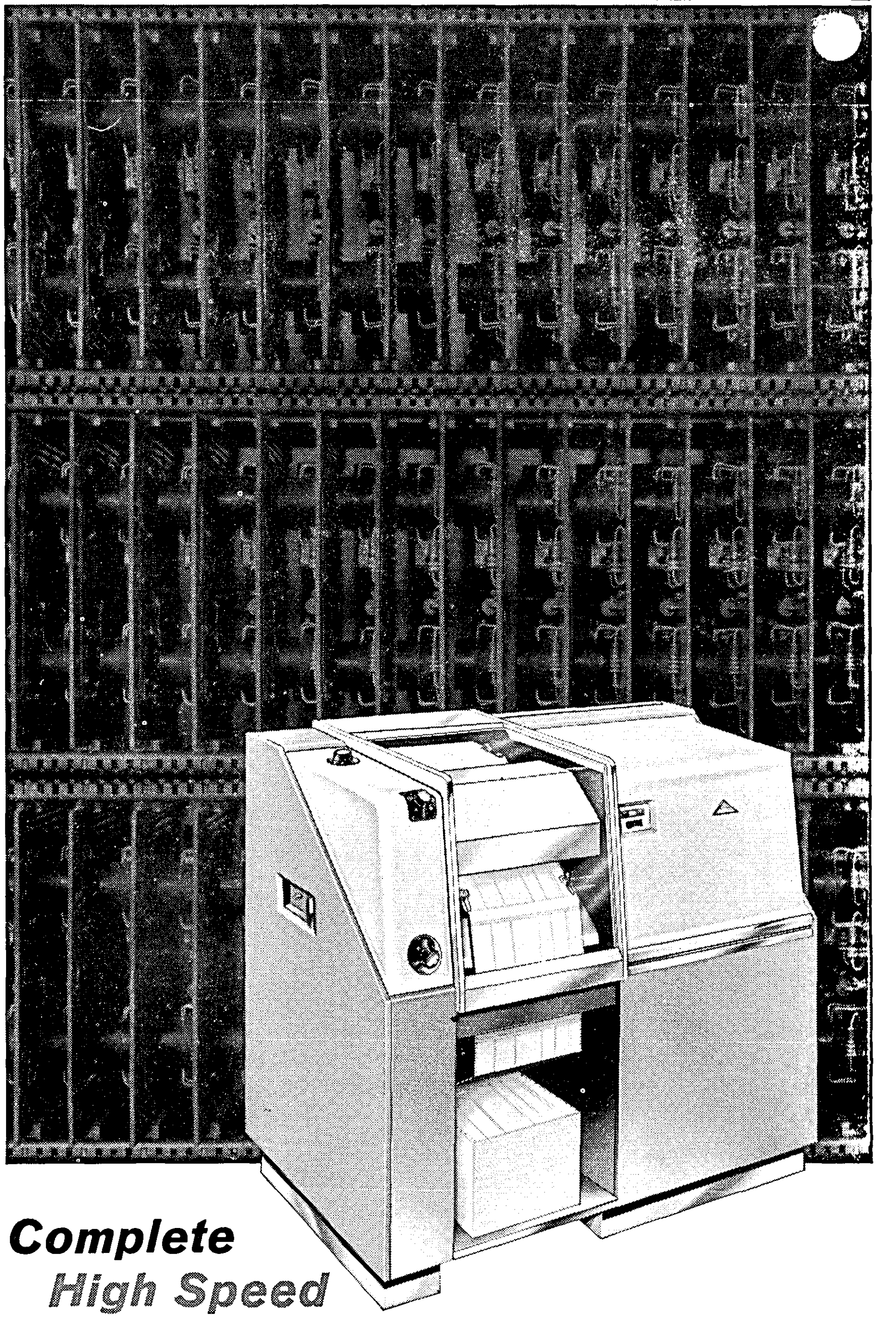

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PROGRAMMERS
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Artificial Language Construction
Language Analysis.
Compiler Writing.
Systems Design-(Hardware and (Programming).
Symbol Manipulation.
Artificial Intelligence.
Automatic Programming.
Operations Research

. . . or if this list has not provoked your interest, client company will consider your specialty with a view toward developing mutual interest.

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CIRCLE 87 ON READER CARD

structures and simulation of psychological processes such as learning.

A considerable interest has been generated on the Continent, particularly in Germany, by Ferranti sales teams. The Soviet Union has sent a letter of intent to purchase an Atlas, but the order could not be accepted because of the British government's embargo on exporting goods to Russia that have a military potential.

While Ferranti feels that at least 25 computers in the Atlas class could be sold in the U.S. since Stretch was taken off the market, sales efforts here have proven fruitless. There are no firm orders in the house.

Reasons for the lack of U.S. sales are the three year delivery date quoted on Atlas and of course, U.S. government import restrictions on foreign computing equipment to be used by federal agencies.

However, Ferranti has hopes of launching a fresh attack on the U.S. market when all of the bugs in the Manchester installation have been eliminated. A series of on-the-scene demonstrations for U.S. computer personnel have been planned.

BENDIX "CONSOLIDATES"

Suffering under the strain of corporate timidity in the financial backing of its computer division, Bendix recently issued a three page news release describing what was termed "consolidation of its position in the computer field."

In substance, the report quoted Bendix president M. P. Ferguson as planning to expand computer sales to the military while "realigning its sales organization" in the general purpose, commercial field.

With the closing of field offices in Oakland, Tulsa, Boston, Kansas City and Denver, and the departure of a large number of key personnel including computer division manager Charles Edwards, the use of the word "consolidation" was translated by industry rumor into "capitulation."

While the outlook for Bendix Computer may not appear as the brightest light on the horizon, a modest amount of optimism can be justified. First, an r&d effort is progressing on a transistorized version of the G-15 and Bendix has amassed a tidy backlog of over 300 G-15 users which could be profitably converted to a new solid state should it appear within the not-too-distant future.

Secondly, G-20 installations are progressing at a reasonably steady rate although admittedly, no production records have been shattered to keep pace with the 20 orders in house.

Finally, software development for the G-20 is largely on schedule, a rarity among most computer manufacturers. ALCOM, an algebraic compiler, and the SPACE executive system were both shipped last month. FORTRAN II will be delivered to users this month and COBOL will be ready in the last quarter of this year.

With the added potential of beneficent favors from the military and hopefully, the financial patience of its Eastern management, it is probable that Bendix will not leave the computer field regardless of the implications of its own news releases.

ROYAL McBEE BOWS OUT

In what may be termed a most uneventful tossing-in of the financial towel, Royal McBee pulled out of the computer field last month.

With virtually no advance fanfare and little effect on its employees or 400 LGP-30 users, RM sold its 50 per cent interest in Royal Precision for 5-megabucks to General Precision Equipment whose Librascope division has been producing the commercial equipment RM has marketed.

As of last July, Royal McBee's investment in Royal Precision was $11,162,047 with an equity in the firm's net assets of more than 3-megabucks. Royal Precision has not returned any profit to its owners. A loss of nearly 7-megabucks has been incurred.

RM will now concentrate on a new typewriter line as well as the development of peripheral gear for edp systems such as a 50 cps paper tape punch and reader.

The split between the manufacturing of a computer system by one company and its marketing by another has long been a major bone of contention between Royal McBee and Librascope as well as somewhat of a curiosity in the industry. RM's departure should ultimately result in an improved product line from Librascope and of course, a more realistic competitive position in the commercial field.

ALWAC REMAINS

In the midst of multi-million dollar losses and gains, bullish prognostications by corporate chiefs, and belt-tightening bearism from others, the weeniest of them all, ALWAC, a division of El-tronics, Inc., persists in doing little more than persisting. There are 38 users of the ALWAC III and four machines remain for off-the-shelf, ultra-speedy delivery.

Talk of the ALWAC IV also remains although work has been delayed due to a recent splitting off of certain assets of El-tronics into a new firm known as El-Tek, Inc., which will specialize in computer modules, read-write heads, peripheral gear and small, special purpose machines.

COMPUTER EXPORTS CLIMB 194 PER CENT

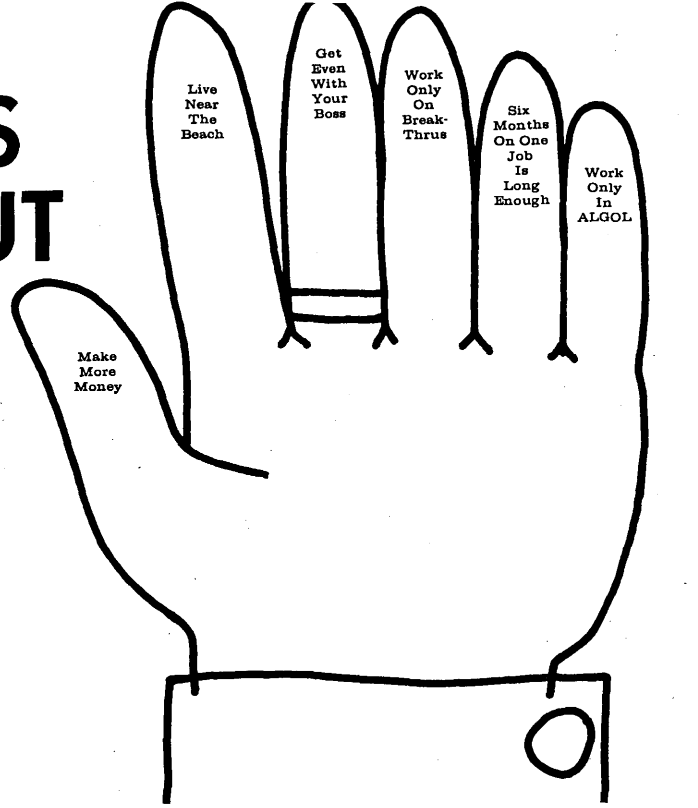
Impressive proof of the growing market for hardware abroad was attested to recently by a Commerce Dept. report that computer exports increased 194 per cent during 1961 over 1960. By far the leading category in all business machine exports, it may be noted that the closest competitor to computers was cash registers with a 44.6 per cent increase over 1960.

The dollar volume of computer exports for nine months in '61 was $79,615,539 or 34.8% of the total value of business machines shipped abroad. Second in line as far was punched card equipment with $44,497,494 shipped last year or 19.4% of the total. Exports of both computers and punched card equipment totalled more than 54% of all business machine exports.

Since the balance of trade may hardly be considered properly balanced, it should be noted that imported computers accounted for only 4.7% of the total imports of business machines with a dollar value of slightly more than 3-megabucks. Their increase over '60 was 15.9%. Typewriter imports were highest in volume and mag tape recorders showed the highest percentage increase over the previous year -- 172.6%.

DATAMATION

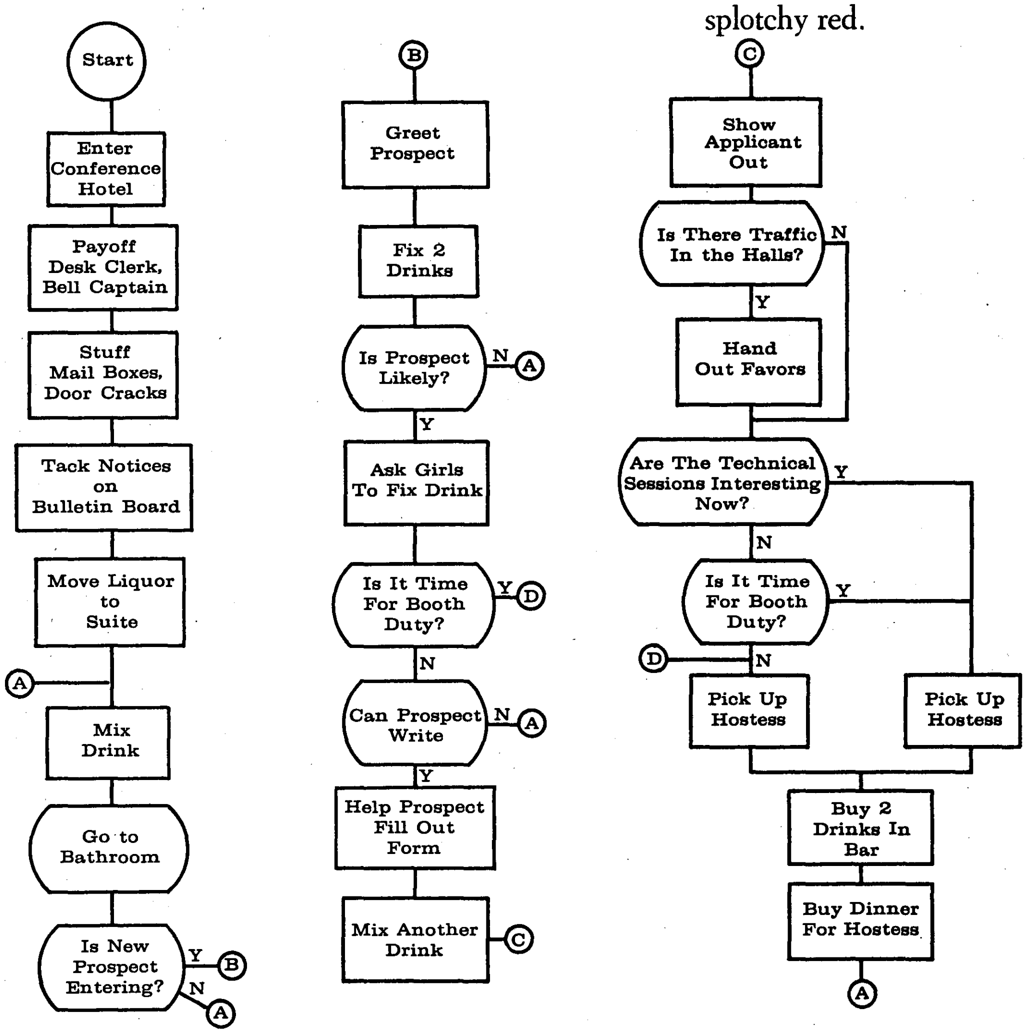
EDITOR'S READOUT



THE CONFERENCE RECRUITER . . . IN COLOR

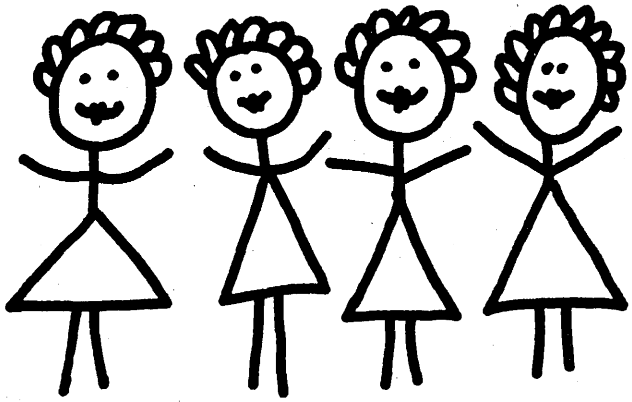
Sincere apologies are formally tendered for adapting the delightful motif of Hans, Altman and Cohen's *Executive Coloring Book** for the following accouterments of the computing conference recruiter. For the minute minority of *Datamation* readers who have not been thoroughly immersed in this activity, a crayon set may be purchased most anywhere. For conference planners and other erudite noblemen, this offering may be properly viewed as a plea for professional decorum in the burgeoning field of body swapping.

This is my hand. It has six fingers, one for each of my virtues. It is a happy hand and will shake your hand. Squeeze it and it squeezes back. Color it a splotchy red.

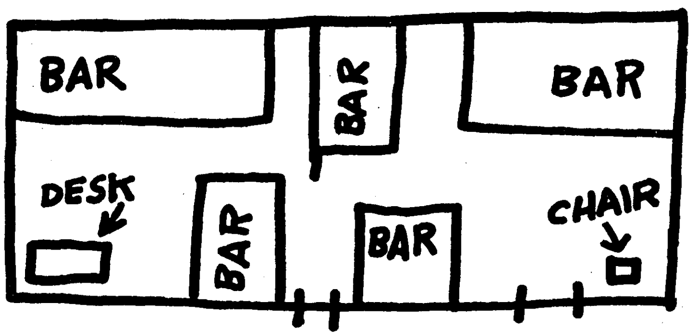


This is my flow chart. It is a closed loop leading to drink. Color it looped.

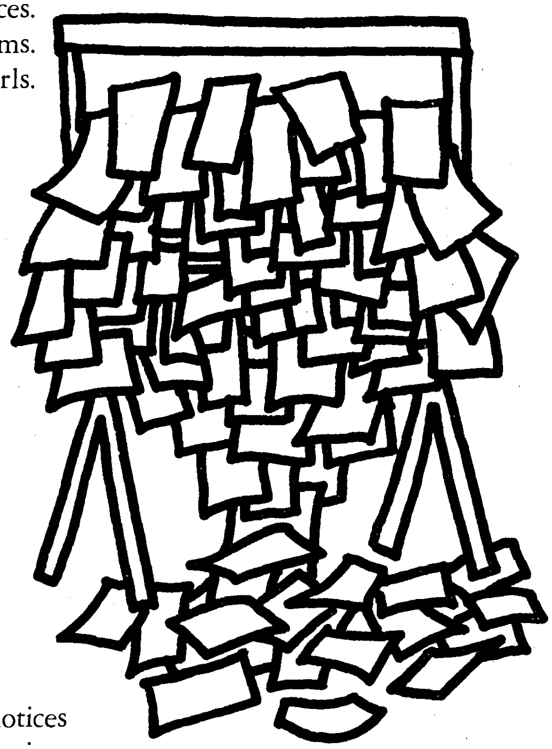
*Published by The Funny Products Co., Chicago, Ill., 1961, $2.98.



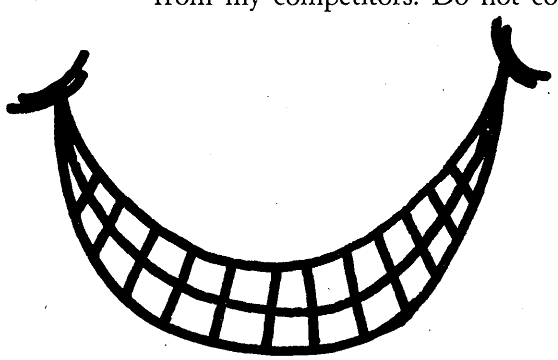
These are my girls. They attend all the conferences. They will help you fill out your application forms. They will bring you drinks. They are nice girls. Color my girls pink.



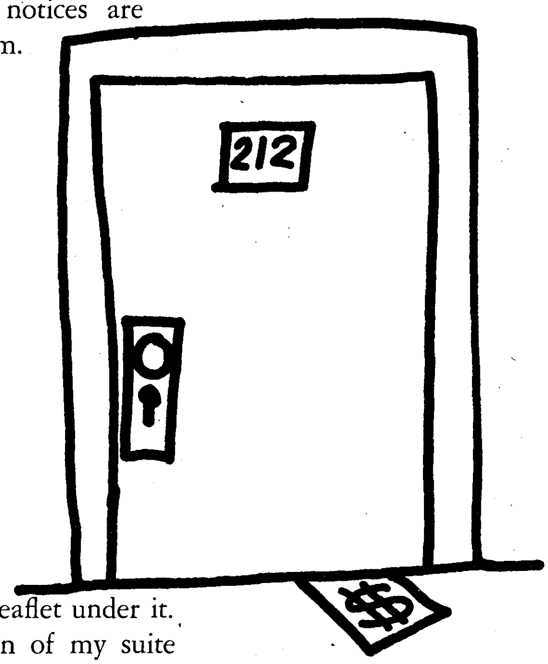
These are my rooms. I have a hospitality suite. Some of my competitors only have one room. I have a suite. Color my suite Scotch.



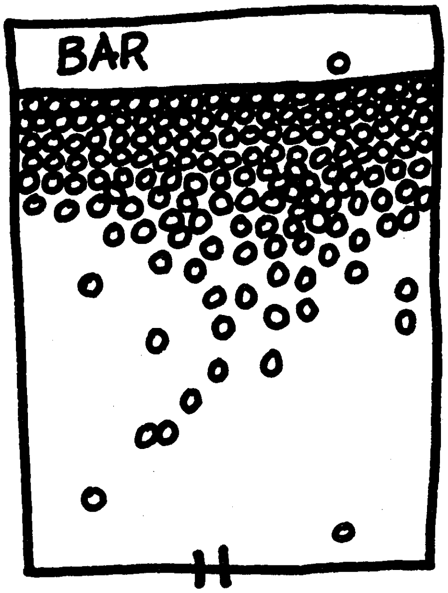
This is the bulletin board. There are many notices on the bulletin board and most of them are mine. Color them differently. Some of the notices are from my competitors. Do not color them.



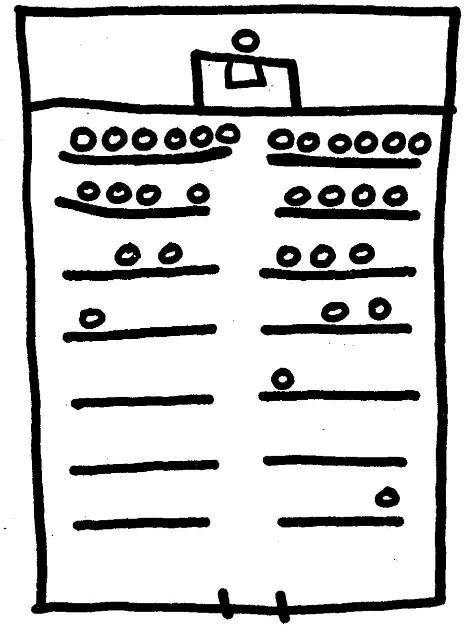
This is my smile. It is a handsome smile. I use it all the time. Color it fake.



This is a hotel door. I have slipped a leaflet under it. It keeps you informed of the location of my suite which sometimes changes. Color the door faded walnut and my leaflet luminescent green.

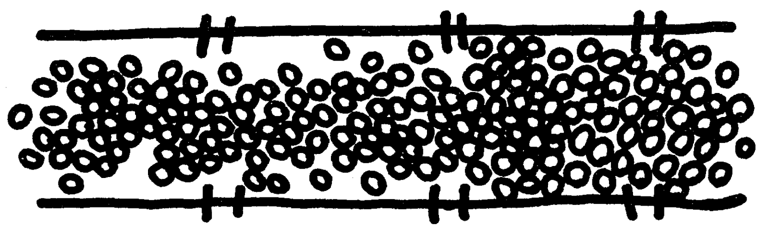


This is the conference cocktail party. I am here. I am working. If you find me, color me sober.

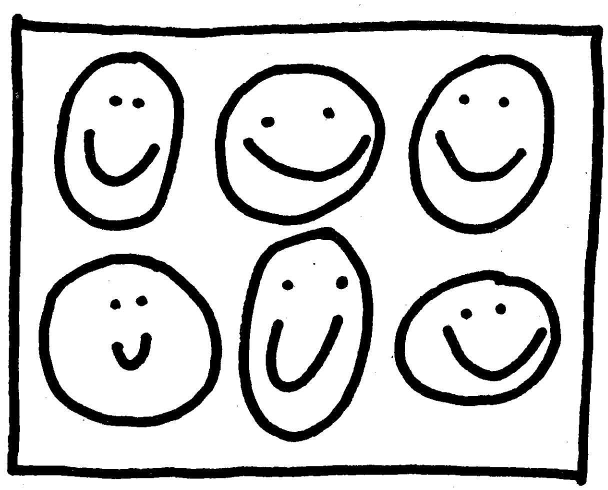


This is the General Session where technical papers are read. I am never here. Technical matters confuse me. Color the speaker dull.

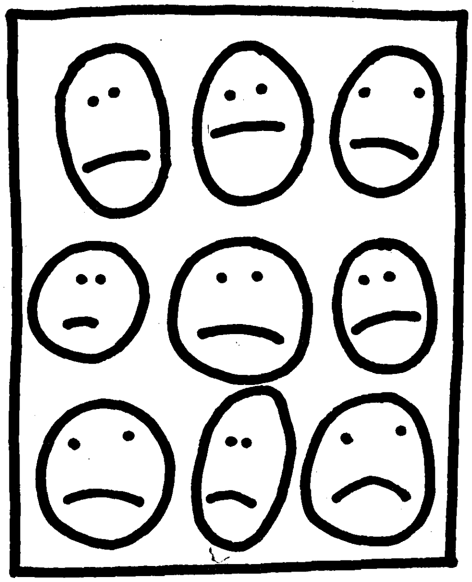
This is my form letter. It is very intimate. I sent it to everyone. It was written by an advertising agency. I received a three per cent return. Color it intimate.



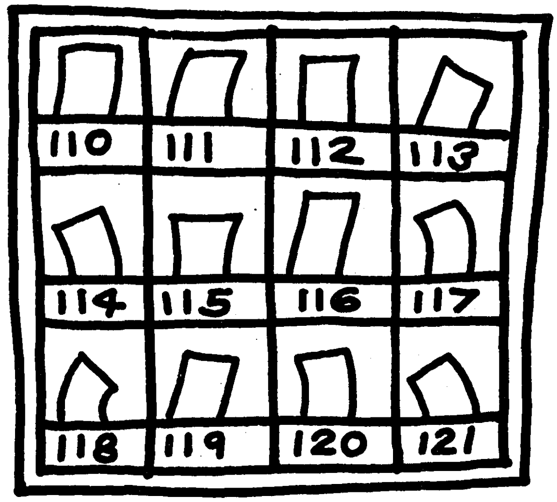
This is a crowded hallway. I am working here. If you find me, color me black.



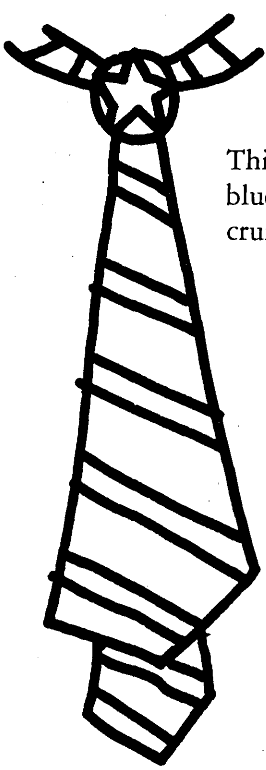
This is my staff. Sometimes we recruit one another. We call each other "Dr." Color us all the same.



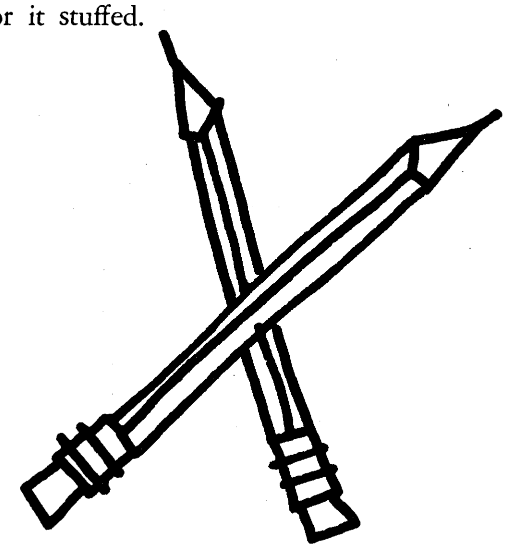
These are the people we recruit. They are programmers. One of them is a logic designer. We call them all "Dr." Color them gold.



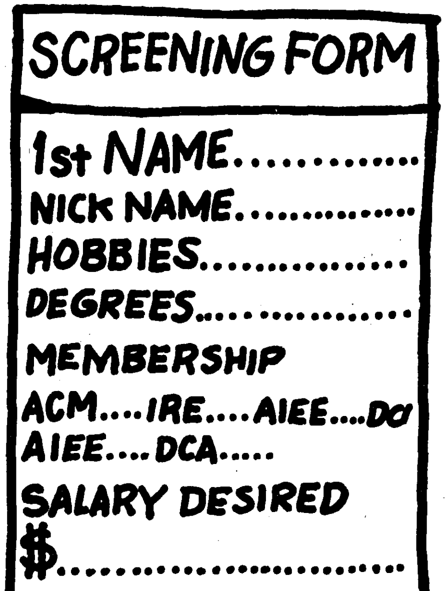
This is the mail box at the registration desk. It is filled with my leaflets which keep you informed of the location of my hospitality suite which sometimes changes. Color it stuffed.



This is my necktie. Color it red, white and humble blue. The government is very generous about recruiting and we do not like to boast about it.



These are my pencils. I take two to every conference. They are not very heavy. I use them to mix drinks. Color them wet.



This is my application form. It is the culmination of all my work. Do not color it. Fill it out. If you do not feel like filling it out, just sign it.

Dr. John W. Mauchly (left) and J. Presper Eckert (right).

More than 15 years since the invention of ENIAC, the world's first, general purpose, digital computer, the starters-of-it-all have undergone almost as dramatic a revision in their outlook and present-day roles as their original invention.

To provide our readers with some unusual and specific prognostications and an occasional amusing reflection, DATAMATION enlisted the patient cooperation of J. Presper Eckert, vice president of RemRand UNIVAC, and Dr. John Mauchly, president of Mauchly Associates, for the better part of a mid-February afternoon.

During the course of the taped interview, there were no ground rules and few restrictions on topics for discussion. The following manuscript has been edited only for cogency, and not for syntax or sensitivities.

a merger of recall and look ahead

AN INTERVIEW WITH ECKERT & MAUCHLY

by HAROLD BERGSTEIN, Editor

Q: Since the ENIAC was a direct result of your efforts and government money during World War II, when would you speculate that the digital computer might have been invented a) if there had been no war, and b) if there were no Eckert and Mauchly to invent it?

E. I think you certainly would have had computers about the same time. There are a lot of things which cannot linger long without being born. Actually, calculus was invented simultaneously by two different individuals. It's been the history of invention over and over again that when things are kind of ready for invention, then somebody does it.

What puzzles me most is that there wasn't anything in the ENIAC in the way of components that wasn't available 10 and possibly 15 years before. Even two tubes in one envelope were available 10 or 15 years before they were used. Knobs, switches and resistors weren't quite as good and a little more expensive, but they weren't so different. The ENIAC could have been invented 10 or 15 years earlier and the real question is, why wasn't it done sooner?

M: In part, the demand wasn't there. The demand of course, is a curious thing. People may need something without knowing they need it.

E: Such as paperwork?

I was thinking back to 1930. Only about one third of our labor force was doing paper work instead of the half today with the computer.

M: The demand was being met, as far as office clerical jobs were concerned, by a growing battery of punched card equipment.

Q: Is it your contention that sooner or later, by some devious means, a punched card machine would have turned into an integrating calculator?

M: One of the books which I had available at the time we were working on ENIAC was written by Dr. Wallace Eckert of the Watson Scientific Computing Bureau, on how to do scientific computations using punched card machines. This was the kind of thing that was going on at the Naval Observatory.

E: How to do scientific calculating with a machine that was made for entirely different purposes!

Q: Who made the now classic prediction that the total requirement for computing power in the U. S. would be six machines?

E: There's some confusion here. John said, 'Let's get orders for six machines to get us enough backlog to make it worthwhile to go ahead with the ENIAC project.' And then, Howard Aiken made a remark that if six machines were built (and I don't know whether he was referring to the six machines we were building or whether he was referring to some other source), we'd never be able to train enough people to program enough problems for these machines. Of course, he was thinking of just hand programming. And, of course, he didn't take automatic programming into account.

M: I don't think he took into account the fact that some of those machines would be devoted to repetitive tasks such as running payrolls weekly for which you can keep these machines busy without large programming efforts producing new problems all the time. Some people of course, made the opposite error and assumed that it was a one-shot effort in programming and once a payroll was programmed, why there you sat.

E: I don't think Aiken thought of sorting and collating and file maintenance and all that sort of thing which take up hours and hours of time on these machines and yet you're not really doing any computing in the ordinary sense of the word.

Q: The technological progress which has taken place in the past 15 years may best be brought into focus by a suggestion of Willis Ware (AFIPS Board Chairman) made at last year's ACM Conference. He felt that if all hardware development were frozen for a period of time, we might learn how to apply existing technology more efficiently. Would you care to comment on this point of view?

E: Its certainly true that we haven't learned to use the computers we have to the best advantage, and I suppose the real force of his remark is that if we did freeze such development it would force us to turn our attentions to better uses. However, I don't really believe we'd be better off.

M: I would agree. I think this is kind of automatic in the way we work in this country. If it were better to make progress doing software development rather than hardware, this is in fact, what we'd be doing. I think you work in any area that has a little softness to it, and when you push, it gives a little. There's some give in both directions, so why not work in both directions until you run up against a stone wall?

E: Just because a lot of guys are screaming that they can't hire the programmers they want, doesn't mean there's a stone wall and that you can't train more people or that we have run out of ideas for improving programming. There are stone walls only when you finally get to the point where you can't beat the speed of light in a wire.

Q: What do you feel is the single most important problem that the computing industry faces today?

E: I think the programming problem is the most serious problem at the moment, but it's not one in which progress is not being made. I think it is certainly getting a much larger percentage of RemRand's budget than it was some years ago. This is probably true in the other companies as well. I think these things are self equalizing; that is, a solution is sought where it can make the most progress the easiest way. But there is also some awfully good work being done in hardware, and if you can improve speed by a factor of 10 or 50 in the hardware, I don't see why you shouldn't do it.

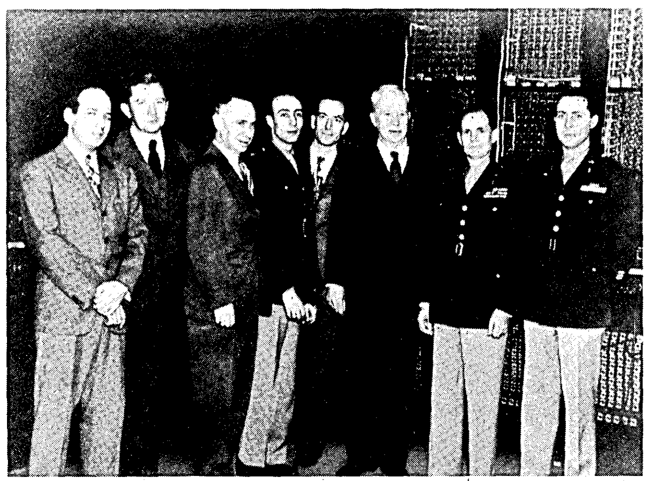
M: Some people think that the most important problem is to make money out of the computers.

E: Well, there again you have to decide whether you mean in the next year or the next five or ten years. Your approach can be different on that, too.

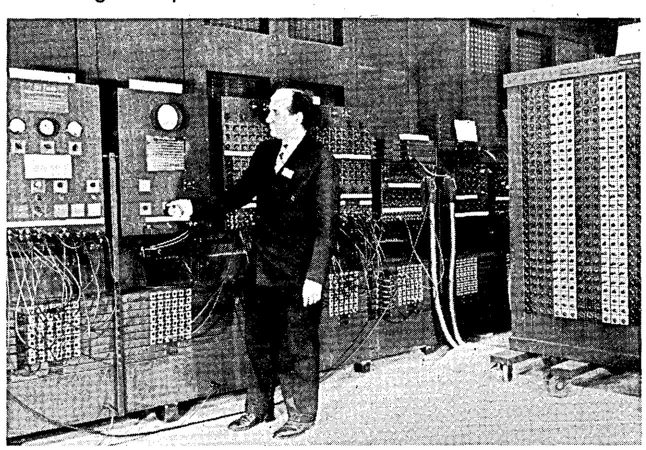
Q: Do you feel that the software problem will not be as serious in five years as it is today?

M: I wouldn't be surprised if it was a worse problem five years from today, but that would be a purely relative point of view. I view this type of activity as an expanding

Present when ENIAC was announced, February, 1946 were (left to right): J. Presper Eckert, chief engineer; Professor J. G. Brainerd, project supervisor; Sam Feltman, chief engineer for ballistics, Ordnance Dept.; Capt. H. H. Goldstine, liaison officer; Dr. John W. Mauchly, consulting engineer; Harold Pender, dean of the Moore School of Electrical Engineering, University of Pennsylvania; Gen. G. M. Barnes, chief of the Ordnance R&D Service; Col. Paul N. Gillon, chief, Research Branch of the Army Ordnance R&D Service.



J. Presper Eckert checks pattern on CR tube during ENIAC demonstration, February, 1946. Large unit on caster (extreme right) is portable function table B.



horizon as most scientific problems are. You don't have very many problems on which you can sit in a closed room with the window shades pulled and try to think of nothing.

E: You mean the problem is how do you think of nothing? I think I can bring back to John a problem on that point that was never solved. In the original ENIAC, we had a facility we never made much use of. We designed each of the panels with its own separate programming element in such a way that we could program the operation of a number of panels in parallel. In practice however, we found this sufficiently difficult to plan that we rarely did it, except in certain problems. Now I think they're going to run out of pulse rate in a few more years, and they're going to get back to wanting still more performance. They're going to find new methods, and so on, and still want more performance. They're going to try doing several things in parallel. At that point I think all hell is going to break loose in the programming business again.

You see, in pure speed we haven't got very far to go. One has to view this thing as on a logarithmic scale because certainly LARC and STRETCH, as two examples, will compute a million times as fast as a fellow who does calculating by hand. And yet, on pulse rate alone, you've only got about another factor to go. So on a logarithmic scale, we're 70 per cent or so from the end.

Now, the reason you must think it's a logarithmic scale is that we certainly aren't doing the amount of work that we could do with 10 million people. Certainly people wouldn't work it this way and speed therefore, is only one of the ways a human being presents himself. He has other dodges to get around the speed problem.

Q: Now that you've brought it up, why was LARC withdrawn from commercial availability?

E: I think that we just didn't have the necessary sales force to sell it and all the other products we have. Of course, there's a little more than that to LARC. The computer tended to require a lot of custom engineering. One customer wanted one kind of output and another wanted another and still another wanted different kinds of tapes. We were getting into more custom engineering than we could manage. This takes a lot of special sales handling and we wanted to get out of it and apparently so did IBM.

Q: Is RemRand going to stay out of the super-computer field?

E: I think that what we'd like to do is see what the other companies are going to do and take faster basic circuitry such as some film memory work we have which is basically faster than the other people's memory work, and see how far we have to go. I think what we'd like to do then is to build a machine that was as simple as possible and that was still better in overall performance without going all out for performance. In that way we can go at these other people from a cost angle.

In LARC (and the same holds true for STRETCH) we said let's pull all the stops out, push the limit of the circuitry and not worry too much about the cost of the machine. This is a pretty expensive way to go. I think the next time we'd like to strike a better medium between cost and performance.

M: In a sense, this was the spirit in which the UNIVAC I was designed. The ENIAC was a highly parallel machine, parallel as to handling the digits and parallel as to handling the program. In UNIVAC, we went to the serial machine, completely serial as far as program was concerned. The idea was that this would cut the cost down while retaining a very useful standard of performance.

Q: What is your estimate for the development of the first nanosecond machine?

E: It has taken about five years to generate a LARC or STRETCH from the back-of-the-envelope stage, and we might be able to generate a nanoscond machine in five or six years from the time we started. I presume someone will start in the next year.

Because people are a little scared of too much complexity in programming these days, and because of the great cost for STRETCH and LARC programs, I think we'd probably start on something that was logically a little simpler. And while some ideas in logic may have produced a gain of a factor of two or three and circuity is 20 times faster, I don't think that the actual machine produced would be 20 or 50 times faster than STRETCH, but something like 10 times faster and it would turn out to be smaller, simpler and less expensive.

Q: When will the first computer with a large section of thin film memory be commercially available?

E: In two to five years.

Q: What do you expect will be the reduction in costs for thin film circuitry within this period?

E: We have two different ways of producing thin film. One of them would seem to be about the same in cost and the other would cut the cost in half.

Q: Can you describe them?

E: They're both thin films, except that one of them is a little thicker. It may be referred to as thick thin films.

Q: At present, RemRand's thin film computer, the 1107, has only a 128 word memory of thin film and 32K of core. Of what real value is 128 words of thin film?

E: It's considerably faster than core and by using the thin film, the user is able to get higher effective speed out of the 32K. They feel that the presence of a thin film memory on some problems can make a 4 to 1 difference and on others, it makes relatively little difference. But they think that across the board it makes a 2 to 1 difference. Obviously, it depends on the type of problem you get.

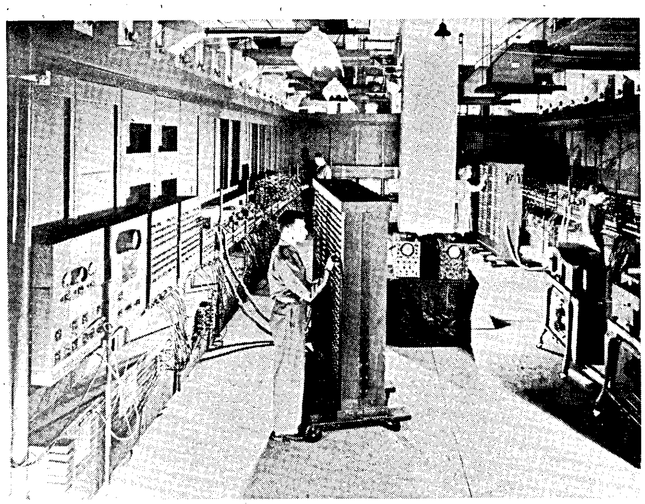
Q: Practically speaking, there may not be too many problems where you can effectively use 128 words of memory.

E: Well, they bring in pieces of problems. Af course, we have military devices with larger thin film memories.

Q: Dr. Mauchly, since the conception of UNIVAC I and the sale of the first commercial machine, have you received any royalties on the invention of the computer?

M: These patents which were jointly held were assigned to our original company when we started business and these in turn became the property of RemRand. So we

ENIAC as it appeared when installed on the first floor of the Moore School of Engineering.



have received some payments which could be counted that way but this is no gigantic figure.

Q: A subject of some speculation in the industry was your decision to leave RemRand. Would you care to comment on this?

M: Well, this is a situation which has many facets to it of course, but I felt that I would be happier doing things that I wanted to do and there wasn't any opportunity to do them at the time I was at RemRand.

I was very much interested in various kinds of applications which Critical Path Method (CPM) is just one and yet, many of these have not been explored. I still have very ingrained desires to get back to some other problems of a statistical nature which aren't very much further advanced than when I was working at them in the 1930s and decided that computers were needed to proceed further. I'm hoping that in the years to come there will be opportunities to do this. I have not yet found the right combination of money and time to do it.

Q: Has there been any consideration on your part of returning to RemRand?

M: None at all. I have new headaches but I'm happy with them.

Q: If you received an offer from a computer manufacturer that promised an attractive salary and the freedom to do whatever you wish, would you consider this offer?

M: Not very seriously.

E: It seems to me he would get this kind of offer without much trouble.

M: This has happened actually, but once you've started a new business you have responsibilities to other people besides yourself. You just don't walk off and leave them.

Q: How large is Mauchly Associates?

M: Counting the people in Canada and England where there are subsidiaries of our company, there are about 45.

Q: Would you describe your present activities?

M: By far the largest portion of our business is in both the training and implementation of scheduling systems, anything from a construction job to the rather complicated research and development programs that go into our efforts such as shooting rockets and missiles into orbit. We are not only training people in basic methods of network scheduling but also improving and building on these methods and training people in how they may for instance, make a more uniform demand upon their various limited manpower requirements, so as to even out the flow of manpower usage and yet, complete their work.

Q: You have just recently introduced Sked-u-Flo (see *Datamation*, p. 104 March). Are you planning any extensive marketing of this analog device or any expansion of your firm into hardware development and sales?

M: This device is in a stage in its history where it's hard to say what's going to happen. It's in a stage very similar to the Critical Path Methods which it was built for. These methods were relatively unknown and no attention was being paid to them a few years ago. But in the intervening time, more and more organizations have decided this was of great value to them and we're expecting that there will be more people who will not just use the simplest network methods but will want more advanced methods. This computer actually embodies some of the rather sophisticated concepts which although worked out several years ago, have not as yet come into use. Minimum cost expediting for example, is at a degree of sophistication which most network users have not yet come to.

Q: To switch tracks briefly, neither of you gentlemen are listed as members of the ACM. Any comments?

M: I was a founder and early president of ACM. You've just uncovered a serious lapse in my domestic accounting system which failed to pay dues.

E: I didn't belong because John did. He was doing so much in ACM and I was doing other things.

Q: Do you have any general comments about the role of ACM in the computing profession?

M: I consider the Association had and still has a very important role and I think I've already told my secretary to see that I get back in.

Q: Mr. Eckert, since your major sphere of interests are more in the engineering field rather than in programming, is this one of the reasons why you are not an ACM member?

E: Yes, John was more interested in applications and programming and I tended to follow the hardware element. I felt that IRE with all its subdivisions kept me supplied with enough mail.

Q: Dr. Mauchly, you are not a frequent speaker at industry meetings. Is there a reason for this?

M: I respond to most of the invitations I get, but laziness is probably the reason why I haven't written as many papers as I should have. In the beginning of this computer industry, Pres and I were so busy doing things that we spent very little time writing. It was sort of a forced labor to write the reports at the university on ENIAC.

Q: Hasn't the role of the university changed considerably since the days of ENIAC when the development of computer technology was a primary responsibility of the schools?

M: I don't know of any philanthropic organizations setting up universities with departments of research to improve computers. They feel this can be better accomplished today in the larger laboratories of computer companies.

Q: Mr. Eckert, it has been said that you are exploring the field of bionics. Would you care to comment on this?

E: There's that rumor again!

Q: It was mentioned during the dedication ceremonies of RemRand's Whitpain Center last year.

E: No, I didn't! Mr. Bibby mentioned it. I personally regard biological physics as a terribly important field very likely one which we still have to look forward to for future breakthroughs. I have felt this way since the time we started to build computers. It's not a new feeling, nor is it a feeling which was greatly influenced by computers.

When I was still a student I became interested in some work that was being done in Texas of measuring potentials along the stems of plants, and we found potential varied when you shined lights on the plants, and all sorts of interesting things which we don't know very much about and still don't know much about.

Dr. John Mauchly and J. Presper Eckert discuss the design of ENIAC with Major General Gladeon Barnes, chief of army ordnance, in Feb., 1946.

I think that when we learn more about these things we're going to see more and more connections between the two, but when it comes to some of these blue sky articles on bionics, the thing that comes to mind is that we don't understand our own subconscious thinking operations very well. This means we have inputs that we're not even conscious of and that we use these inputs in making decisions by methods we don't understand. I find it pretty hard to consider how to program that on a computer until we understand more about it.

Q: Then you have no active research team currently engaged in the field of bionics working in the basement at Whitpain or elsewhere?

E: No!

Q: Do you have any comments on the field of bionics, Dr. Mauchly?

M: I feel that there are many directions in which the study of all-purpose scientific problems can be tied in with computers, using computers as a tool or computer sciences, if you like, as a sort of model of living systems. But, my native interests go back to meteorology and the weather, and I'm happier when I find that someone has recently confirmed an effect of the moon on precipitation which I worked out in 1954.

Q: Do you have any interests in third generation computers?

M: I feel I have no active part to play in the generation of new types of hardware, new components, and new ways of doing things faster. This is being adequately handled by large research teams. I'm very anxious to see the developments and make use of them. My interest centers more in the applications of these things.

Q: Why do you feel that IBM, as a comparative latecomer to the computing field, has obtained such a position of dominance in the industry?

M: People feel their sales force is a good one. There's also another factor which seems to me to have something to do with it. IBM's business except for typewriters and now dictating machines, is almost entirely in the computer field. In almost every other company, computing is just a sideline or a division at most.

Q: What is RemRand currently doing about shifting this balance of power more toward its favor?

E: The recent trend seems to be to restrict operations somewhat and not to be in so many different areas but rather concentrate on the areas where we have been making progress.

Q: Such as business as opposed to scientific applications?

E: I wasn't thinking of that . . . We've done a lot of basic work in mass storage largely because we think systems have to be designed around mass storages, and we don't think any of the existing systems have been effectively designed in this manner, with the possible exception of the 490, which is somewhat designed to work along with mass storage and real time. That's a large system however, and not really small enough for many businesses. Smaller machines designed more around the mass storage or in line with the real time concept is the area in which we hope to make the biggest dent in our competitors in the future.

Q: Why doesn't RemRand produce a disc file?

E: We made one and stuck it in mothballs because it had too many damn parts to change around; in fact, we made three disc files, and all of them turned out to be awkward, complicated devices. We put out these drum devices which had more storage capacity than the disc files and a lot fewer parts and were a lot more reliable, and so why put out the disc files?

Now that doesn't mean that we're irretrievably against disc files. We are still carrying on research on some disc files but with a great attempt to reduce the number of parts and increase flexibility in ways that haven't been discussed as yet. Actually, if you have big drums or discs, it's kind of a minor difference anyway; it's all magnetic surface recording.

One of the things we've got to trade on is how many bits you can get to the inch on these surfaces. On Randex II we do 650 bits to the inch in one direction and 50 tracks to the inch on the other. We will be putting out equipment in the next few years which will be a thousand bits to the inch and a hundred tracks to the inch. We've done better than that in the lab.

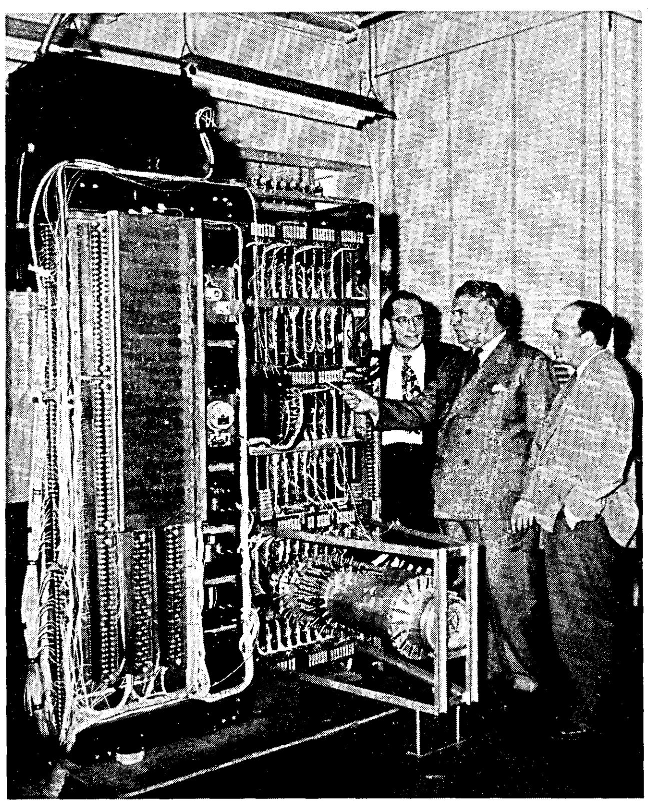
Q: Would you comment on the state-of-the-art as far as automatic programming is concerned, particularly as it concerns efficiency vs. compatibility of compilers such as COBOL.

M: In the early days of our work at Eckert and Mauchly I thought that the development of automatic programming was one of the most important things to be done and actually I was instrumental in seeing that Dr. Hopper got started in that direction.

Obviously, in any attempt at standardization of software systems it's always hard to say how much you're putting things in a straight-jacket and how much you're helping people by reducing the number of different systems that they have to attend to, and try to make work with each other.

In the problem of efficiency vs. compatibility, we must ask what kind of efficiency do you obtain by compatibility? What kind of efficiency do you obtain by departing from some normal or standard system? You have to weigh one against the other. It would be a mistake at first to say that any one system was the final system and never improve it. Yet those improvements must

Dr. John Mauchly (left) and J. Presper Eckert (right), inspect the mercury memory of UNIVAC I with Lt. Gen. Leslie R. Groves, U.S. Army (Ret.) in the Fall, 1950.



always be departures. The same problem comes up when trying to standardize on magnetic tapes.

E: I think it would be a delightful situation if compatibility was possible because I think it's a very important aspect of trying to keep this field competitive, and not just becoming a monopoly. You see, this whole computing business can become a software monopoly by one supplier who for generations will use nothing but his equipment. To the extent to which COBOL and those things work, you're going to avoid this monopoly and the more you avoid the monopoly the better equipment you're going to get. And the better COBOL you're going to get, too.

Q: In the near future, will we see a preponderance of larger or smaller machines?

E: Both.

Q: With one or the other dominant?

M: It's a question of what dominant means. If you make your count by machines you get one answer. If you make your count by dollar volume you get another.

Q: In terms of dollar volume.

E: Dollar volume is almost certainly on the smaller machines. On the question of using large computers for time sharing, I believe there has to be considerably more study.

Q: Do you believe that the number of manufacturers presently in the computing field will remain somewhat static?

E: I think that the companies selling larger machines will be dropping these entries and that there will be more small machines announced because the technology is going to make it possible to have a lot of small machines; maybe little digital machines which can sell for under $1,000.

M. For many years the emphasis, not only the general public's, but the computer buyer's emphasis, seemed to to have been on speed, but it should have been on economics: what do you get for your dollar? Well, although there are ultimate limitations on the speed with which you can do computations—the speed of light through a wire, as Pres was saying—I don't know that there are any such serious, forseeable limitations on the economics of computing.

We will continue to learn how to make these things cheaper and cheaper, and will continue to be training more people who will naturally think in terms of computers just as we now naturally expect everybody to read and write. Literacy is taken for granted in this country. Well, someday, they're going to be literate about computers, too. It is actually easier to teach elementary children about computers than it is adults. Adults start off with a closed mind.

Q: But will the average individual ever reach the austere heights of a programmer?

M: If you can get the machines small, then you get more smaller users, and you'll have more stereotyped problems, too. We have more people now who can do arithmetic. It's not just a question of being able to read and write. It used to be quite a chore for someone to just add a column of figures. If you're going to be employed in a restaurant, why any waitress is supposed to be able to add up a check. In general, you expect these abilities from the person on the job. You expect everyone to be able to dial a telephone number and to use the telephone correctly.

In that sense, to my mind, the computer of the future fits in with the way of life of the common person. He doesn't have to be a programmer, in any glorified sense, but he has to know what uses can be made of computers, how to get access to them to do what he wants.

Q: Is there any primary field of application which you think is going to receive special attention within the next year or two?

M: In one sense the answer to that, one could gather from the consensus of what people are talking about in business management and information analysis. More and more you find the schools of business like Carnegie Tech where I was visiting professor of systems engineering last year, and other well-known schools, are putting emphasis on management methods whereby you get decisions worked out on a rational basis. Quite often the computer is the essential instrument for providing the analysis of information and reduction of the data necessary in order to make a rational decision.

Q: There has been a great deal of public attention directed at displacements of the labor force because of computing. In England some years ago, mobs were incited to the point where they tore apart the looms. Can we expect a similar action against the 90s and solid states?

M: There certainly may be temporary outbursts but if these occur they will merely be sporadic events.

E: I think there would be more clerical jobs if it weren't for computers. However, I doubt whether we have put people out of work because the number of clerical workers is still on the increase and the percentage only stopped increasing last year and it's up to 52 per cent of the work force. Therefore, it hasn't really put anybody out of work; so far, it's just about stemmed the extended explosion.

But suppose you go further and it does eventually start to put some people out of work. So does everything else which may be considered as progress. So did the printing press. So did the rotary presses, as compared to the hand press. And so does medicine. If you cured the common cold tomorrow, you would put one per cent of the labor force out of work because at the present time, you have about one per cent of the labor force sick at any one time with a cold. Therefore, you have to employ enough extra people on your staff to allow for this.

Therefore, if you solve the problem of the cold, it follows that you should tear down the research laboratories where they're doing medical research on the common cold.

Or, if you make people live longer you are contributing to the same problem since such people are really beyond retirement or the same as being out of work and they have to be supported by the remaining people. Therefore, anyone who does anything to prolong human life should have his laboratories destroyed, and so on. Where do you stop? You have to have some rules to go by before you start throwing rocks at the computers.

M: Other dislocations that have occurred such as the use of oil for fuel instead of coal, have made a lot of coal miners unhappy. In recent years there have been a lot of dislocations of this sort which no one has done very much about. The use of government funds to retrain workers seems to be a useful way of spending money. This is the positive action method.

Q: One final question. What are your definitions of the word "automation?"

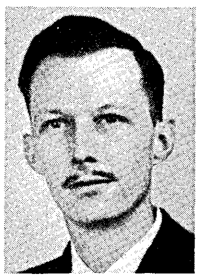
M: Do you have to ask that one?

E: This is one of those words which has meant so many things to so many people. It can mean an assembly line in the Ford factory which means we had automation long before the word "automation" was coined. Or it can mean flush toilets. ■

COBOL AT WESTINGHOUSE

corporate policy urges rapid implementation

by ARTHUR J. WHITMORE, Business Systems Dept., Westinghouse Electric, Pittsburgh, Pa.



More than 50 general purpose, digital computers have been installed by the decentralized manufacturing divisions of Westinghouse in the past five years and many more are scheduled for installation in the near future. Initially, computers were installed to solve the mechanization requirements peculiar to a specific manufacturing division and as a result, there are 20 different types of digital computers presently in use in Westinghouse, each with its own programming language.

Investment in program development has increased more rapidly than machine rental and in 1960 amounted to one-half the total rental expenditures. The current rate of increase in program development costs for the many different types of computers in use indicates that by 1965 this could equal the total machine rental cost.

One of the factors contributing to this rising cost of computer program development is the lack of compatibility between the 20 different types of digital computers. Programming dollars are being spent on duplicate development because of differences in equipment and methods of documentation. Communications problems in the control of computer installations exist due to the lack of a language understandable to programmers and management. Reprogramming costs, when changing equipment, are in many cases, so prohibitive that new equipment is not considered even though a substantial reduction in machine rental can be realized.

For this reason the Westinghouse Business Systems Department has evaluated the use of COBOL (**CO**mmon **B**usiness **O**riented **L**anguage) as a means of controlling computer program development costs. As a result of this evaluation, the Westinghouse corporate policy regarding implementation of COBOL has been determined. This policy states:

> COBOL shall be applied as rapidly as possible in programming data processing applications throughout the corporation and the use of other computer languages for data processing shall be minimized within the limits of good economic practice. To this end —
>
> 1. All new data processing computers shall have a COBOL compiler available or announced. (Some small scale equipment and card systems are exempt.)
> 2. Programming for computers for which a COBOL compiler exists shall be done in COBOL and documentation will include an up-to-date listing of these COBOL statements.
> 3. Programming for all data processing applications will include a COBOL procedure flow-chart. Card systems and small scale computers noted above will be programmed from these procedure flow-charts in the available symbolic language.

COBOL is particularly applicable in the area of program development control because of its features of standard documentation and improved communications. Far too often program documentation has been left to the discretion of the programmer with the result that in the rush to put an application into production, little or no documentation is accomplished. This lack of adequate program documentation has contributed greatly to duplication of development effort and is a significant factor in the cost of re-programming for new equipment. In order to establish proper documentation practices a "Computer Application Documentation Standards" manual has been developed which relates in detail those features necessary to insure adequate documentation. The COBOL procedure flow-chart, noted in the Westinghouse corporate policy on COBOL, is a required feature.

The basic element of a COBOL flow-chart, an English language statement, substantially reduces the problem of communication between persons engaged in the process of mechanizing a business application. The "audit trail" characteristic of a COBOL flow-chart shortens the orientation period required when assigning new or additional personnel to an application in the process of mechanization. This can be significant where programmer turnover is a problem and also when it is necessary to assign additional programmers to an application in order to rush it to completion. The COBOL flow-chart is a definite advantage in "de-bugging" a computer application as this "de-bugging" can be done at a logic level rather than machine-language level. This enables a programmer to spend more time on problem definition and solution for he is relieved of concern of many machine details.

COBOL will be used to advantage in the Westinghouse Modular Programming effort. In modular programming, a complex problem is divided into its logical parts and each part is programmed separately as an independent routine. For example, F.I.C.A., local tax, and employe purchase deductions might constitute three independent parts of a gross-to-net payroll program. These routines are controlled by a separate executive routine. Initial tests on "payroll" and "accounts payable" applications in several manufacturing divisions indicate that a considerable reduction in development effort is possible through an exchange of application modules. These modules will comprise a continually expanding central library which will permit manufacturing divisions, in many cases, to program by exeption (i.e., it will be necessary to program only that portion of an application not available in the module library). Various compiler limitations with reference to

COBOL elective features, and hardware restrictions such as memory size, will be considered when programming these modules in COBOL in order that maximum machine compatibility can be effected.

The evaluation of the importance of COBOL to Westinghouse necessitated an examination of language features considered advantageous and also of language features considered disadvantageous. The comment is often made (usually by programmers) that COBOL is overly wordy and therefore requires a great deal of writing on the part of the programmer as opposed to the abbreviated forms of coding available. This seems to be a prejudiced view when considering the advantage of COBOL in documentation. A data field named "ADSLFT" may be meaningful when the program is being written but might be extremely vague, even to the original programmer, six months later when making a program change. This same data field when labeled ADJUSTED-SALES-FORECAST, while requiring additional writing on the part of the programmer, is much more definitive of the data content. Many programmers when using a symbolic language resort to "comments" or "title" cards which are unnecessary in COBOL. The amount of re-writing is reduced when using COBOL as fewer errors are made when employing the higher level language. The ability to "unitype" or keypunch directly from the COBOL flow-chart has proved feasible thus reducing transcription work. We feel that the slight increase in writing required when using COBOL is more than justified considering the documentation it affords.

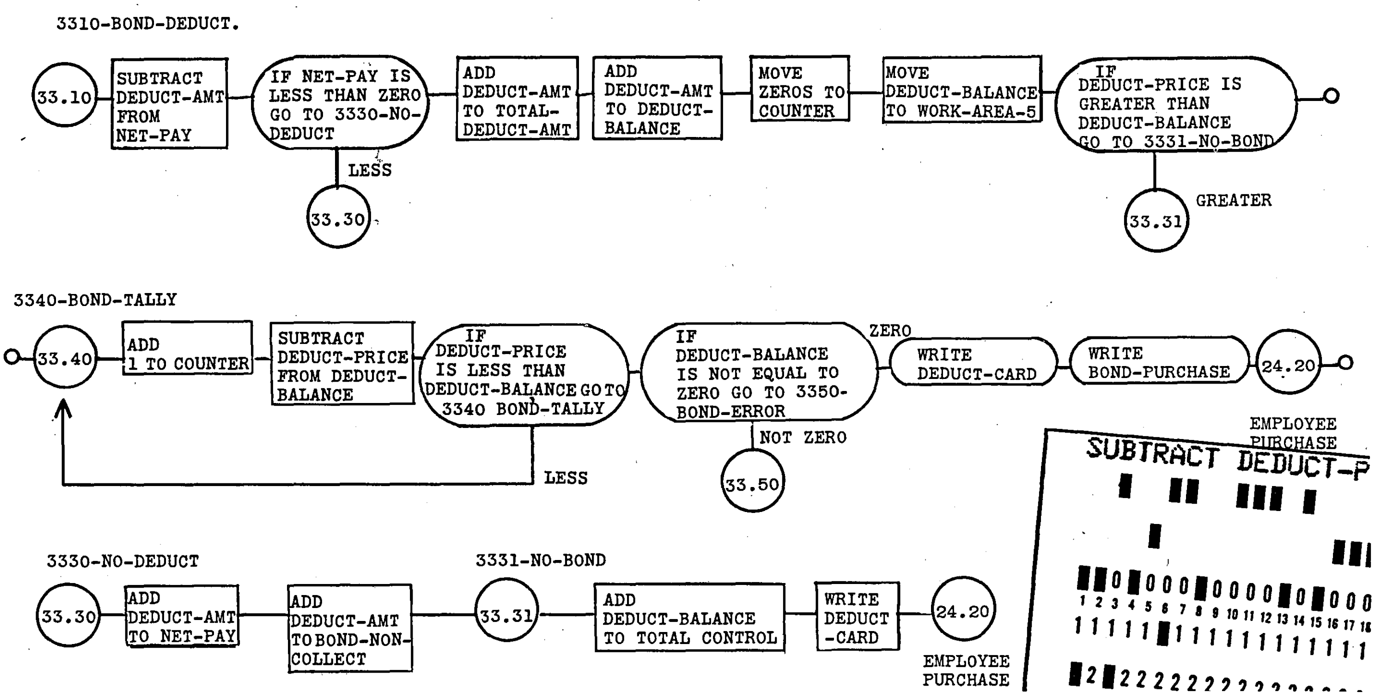
Another criticism leveled at COBOL is that is it not a true business language because its vocabulary does not include many of the functions necessary for business data processing such as sorts, merges, report writing, and similar functions. The ability to perform these functions is certainly important in mechanizing business applications. COBOL, however, is a dynamic rather than static language and these very functions (as well as many others) are currently in the development stage and will be included in the vocabulary in the near future. Incidentally, some computer manufacturers have already included some of these vocabulary features in their COBOL compilers as extensions to the existing language. The use of these extensions in their present form may result in a non-compatible program. These features must correspond to the COBOL specifications when they are officially added to the language.

It should be realized that compiling time of early COBOL compilers will more than likely be substantially greater than that of existing symbolic coding systems, and the efficiency of object programs will temporarily suffer. The computer manufacturers, however, are making every effort to improve their compilers with the assistance of the users and some manufacturers are advertising 90 to 100 percent object program efficiency and card reader compiling speeds. To further facilitate our implementation of COBOL, we have offered to assist in testing and improving the COBOL compilers furnished Westinghouse.

A further criticism of COBOL is that a programmer trained in COBOL must also be quite familiar with machine language to be truly effective. We realize that every installation will have and need one or more persons familiar with machine language, but not all programming personnel need be so trained for problem solution is relatively machine independent and the computer manufacturer's COBOL should specify how to write in COBOL to best utilize machine capabilities.

In light of the analysis noted above, the Westinghouse policy regarding implementation of COBOL has been determined and a COBOL education program has been developed. This program consists of a two-day course on the introduction to COBOL and its use in standard documentation procedures and is supplemented by a manufacturer's COBOL course usually of a one-week duration. This program will be continued to bring about and maintain company-wide COBOL education. COBOL does not replace the necessity for proper systems analysis, input document preparation, or proper programming techniques and we do not view COBOL as the answer to all data processing problems; however, COBOL is the best vehicle available to accomplish the goal of effectively utilizing the data processing capabilities and program development effort in Westinghouse. ■

NOTE: SAVINGS BOND DEDUCTION ROUTINE; DEDUCTIONS ON CARD INPUT



IMPROVING DEBUGGING EFFICIENCY

a study in program testing service

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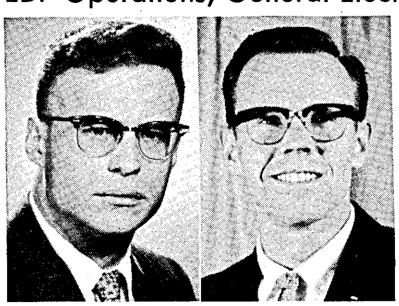


One of the facts-of-life concerning the operation of an electronic data processing installation is the lengthy time period required to develop a computer program. Simple economics and the desire to improve service requires (1) reducing the time required to program an application, and (2) meeting the demand for computer program-testing (debugging) service.

In general, organizational effort up to now has been concentrated on the improvement of programming language systems. The results of this effort have paid off handsomely in the simplification of program coding and increased the feasibility of automating more complex applications. In fact, it has been so successful that it is believed that the day is rapidly approaching when coding may present a secondary demand upon the time of data processing programmers.

Recently, studies concerning the level of computer program-testing service were conducted by management of the Electronic Data Processing Operation at the Hanford Atomic Products Operation[1] of the General Electric Company. From these studies, we found that with improved planning, clarification of operating policy, increased peripheral operations capacity, and revised work methods, we could drastically reduce the amount of time required for debugging programs.

The essence of what General Electric learned from its studies are contained in the four sections that follow. Some of the problems are peculiar to the specific installation but any data processing installation endeavoring to improve its programming service can learn from General Electric's experience.

The data processing operation at Hanford operates an IBM 7090 computer, and associated peripheral equipment which includes two IBM 1401 systems. Processing on the equipment is conducted through twenty-four hour periods with four rotating shifts. The programming workload includes scientific computing, the development and maintenance of business data-processing applications, and the development and maintenance of technical data-processing applications. During the past three years, Hanford's data processing installation has experienced a considerable growth—in computing capacity, in demand for its services, and in the size of the programming staff.

analysis of programming effort

The studies referred to above, while qualitative, indicated that as much as one-third of the programming man-hours expended, and one-half of the elapsed time required to program a business or technical data processing application, were debug related.

From this information, it was evident that the level of program-testing service, (i.e., the rapidity with which a programmer could get the results from his debug attempt), played a significant role in the productivity of the installation. After further evaluation, we found that a programmer could ordinarily expect to get only one or two debug attempts within a twenty-four hour period.

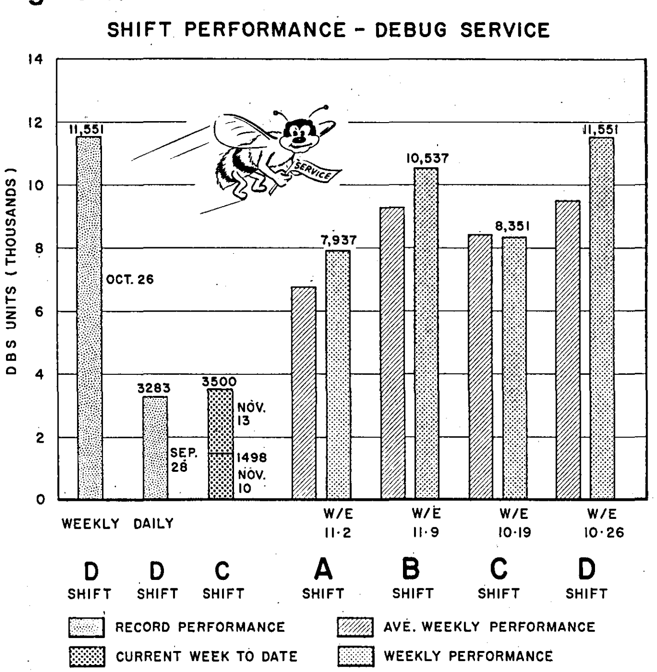
From the analysis, we concluded that with improved planning, clarification of operating policy, increased capacity in peripheral operations, and revised work methods, it would be possible to achieve a one-hour debug processing cycle. With one-hour processing cycle, programmers would routinely get up to five attempts within a twenty-four hour period.

results of the initial analysis

Primarily, one of two processing systems, FORTRAN or 9PAC, is used during program-testing at Hanford. At initiation of this study, it was found that on the average, a FORTRAN debug required four hours for processing, and a 9PAC debug required eight hours. This meant that a programmer could ordinarily get two FORTRAN debugs or one 9PAC debug per day. Interestingly, the total processing time, including putting a job on tape, processing it on the computer, and printing the results, rarely exceeded one-half hour for the typical job. Therefore, a bulk of the total processing cycle was due mainly to "operating delay." This in turn resulted in excessive debug turn-about time.

Detailed observation of the debug processing cycle was undertaken in an effort to isolate and evaluate the cause of this delay, with the result that nearly twenty contributing factors were identified. Each factor could generally be placed in one of the following categories:

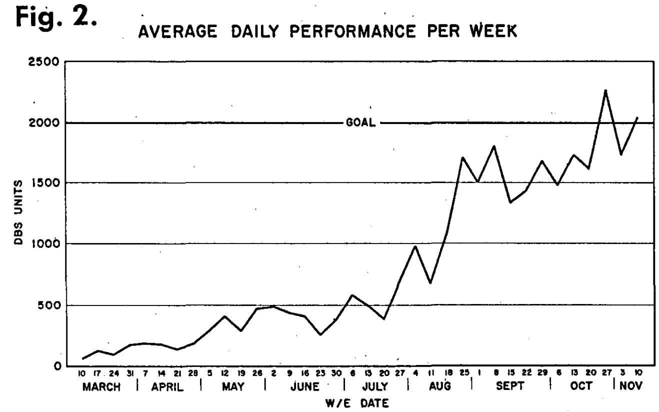
Figure 1.



POLICY: Operating policy did not assign a specific period each day for program testing. As a result, program-testing service often received secondary consideration with respect to systems maintenance, routine production, and preventive maintenance.

SCHEDULING: The scheduling of computer work, to a considerable extent, was at the discretion of operators or individual programmers. This method, which was entirely adequate for a small programming staff, was not adequate for the expanded staff, since it emphasized the achievement of the goals of individuals at the expense of organizational goals.

Fig. 2.



TRADITIONAL OPERATING PRACTICE: The pattern of processing debugs had arisen when equipment of smaller capacity was used, and when, consequently, computer time was at a premium. Upon installation of the IBM 7090, the same criticality on computer utilization no longer existed; but the traditional operating patterns continued. These traditional patterns manifested themselves in numerous ways but the ones which were to be most severely questioned were the following:

1. CHIEF OPERATOR RESPONSIBILITY: Traditionally, the chief operator had centered his attention upon performance and utilization of the computer. As a result, peripheral operations and work flow were given secondary attention.
2. PREVENTIVE MAINTENANCE SCHEDULE: Traditionally, preventive maintenance had been scheduled for the first hours of day shift. This schedule significantly limited the level of program-testing service.
3. JOB-BATCHING TECHNIQUES: The traditional method of processing debugs had been to accumulate a large number of debugs and then to process them as a single batch. This method reduced the amount of tape handling by operators and consequently improved the utilization of the computer. However, this method also forced each job to wait in a queue at each processing step while every member of the batch was processed.

development and implementation of revised operating policy

Armed with detailed knowledge of operating methods, and with the knowledge of the significance of program-testing service, management established specific operating goals in order to bring the operating policy more in harmony with organizational goals.

ESTABLISHED OPERATIONAL GOALS:

1. The programming staff would benefit most from improved debug service during day shift, (i.e., during their normal working hours). Therefore, except for

the processing of high priority plant operating reports, day shift was to be devoted to program-testing service.

2. Under the existing workload, a goal of one hour turn-about cycle was established. Of course, the one-hour cycle cannot be maintained if the number of debugs submitted for testing increases significantly over the present workload. Therefore, a goal was established to maintain a day-shift debug service level of 2000 DBS units.[2]
3. Eliminate any discrimination in service between business and technical applications.

POLICY FORMULATION: Specific operating policy concerning the utilization of the computer during program-testing periods was formulated. Basically, this policy gave priority to program-testing service during day shift operation and relegated other computer activities (i.e., preventive maintenance) to less critical time periods.

SCHEDULING: Scheduling criteria, which were a restatement of policy in operating terms, were established. A primary result of these criteria was to give greater scheduling responsibility and control to the processing activities, and to reduce the influence of the individual operator or programmer.

PREVENTIVE MAINTENANCE: Preventative maintenance schedules were revised in cooperation with the customer engineering representatives. A maintenance schedule was selected on the basis of mutual goals.

WORK METHODS AND PROCEDURES: Operation crews worked closely with the study team to evaluate current operating methods and to experiment with improved methods. As a result, several improvements in methods and procedures were achieved which significantly increased the level of service. The most significant of these are:

1. CHIEF OPERATOR RESPONSIBILITY: Where formerly the chief operators had given primary attention to operation of the computer, they now give balanced attention to all phases of debug processing; that is, they are to treat the computer operation as one step of a multiple-step process.
2. JOB-BATCHING TECHNIQUES: As noted in the initial study, the prevailing goal was to obtain the best utilization of the computer. However, under the revised goal it was to optimize programming effort rather than equipment utilization. In general, operating procedures call for the processing of debugs in small batches of two to six jobs on a single input tape, instead of the prevailing twelve to twenty-five jobs. While this means additional tape handling and lower computer utilization, it also drastically reduces the size of the multiple queues and consequently improves service.

   It was determined that no batch size was optimum for all conditions. For example, the size of backlog, the type of debug, and the time of day all affected the optimum batch size. As a result, batching guides were formulated and suggested to the operators.
3. EQUIPMENT LAYOUT: A revised equipment layout was installed to simplify the debug process and to improve communications between personnel involved. Jobs, as soon as received from programmers, went immediately to a card-to-tape staging area, and then to a computer staging area. This enabled operators to evaluate continuously the size and type of the backlog, and, thereby, maintain closer control over the process.
4. TRAINING OF OPERATORS: It should be emphasized that both before and after the study the operators had and retained a great deal of operating freedom. They are highly skilled and are in the best position to make most of the routine operating decisions. The training objective under this philosophy was to acquaint them with the revised goals of the organization, to advise them of their new areas of responsibility, and to review with them the results of the various methods and procedures which had been explored. This training was of the informal, round-table type, and was conducted by the manager of the data processing organization.
5. SERVICE-LEVEL MEASUREMENT: Because of the installation's rotating shifts, each crew works one week on days every fourth week. Therefore, a daily and weekly service-level report, measured in DBS units, was prepared for each crew's day shift performance. The reporting chart, as shown in Figure 1, was developed to create a degree of competition between crews. The purpose was to encourage the operators to improve their work habits. Also, by charting the daily DBS units, a degree of control would be maintained on the level of program-testing service.
6. EQUIPMENT CAPACITY: During the study, the capacity for conducting peripheral operations was brought into balance with computer capacity, which made improved service physically possible.

results of the study

The growth in service is portrayed in Figure 2. The service-level as shown is measured in DBS units and gives the average daily performance for each week. As can be seen, the goal of 2000 DBS per day has not yet been consistently achieved.

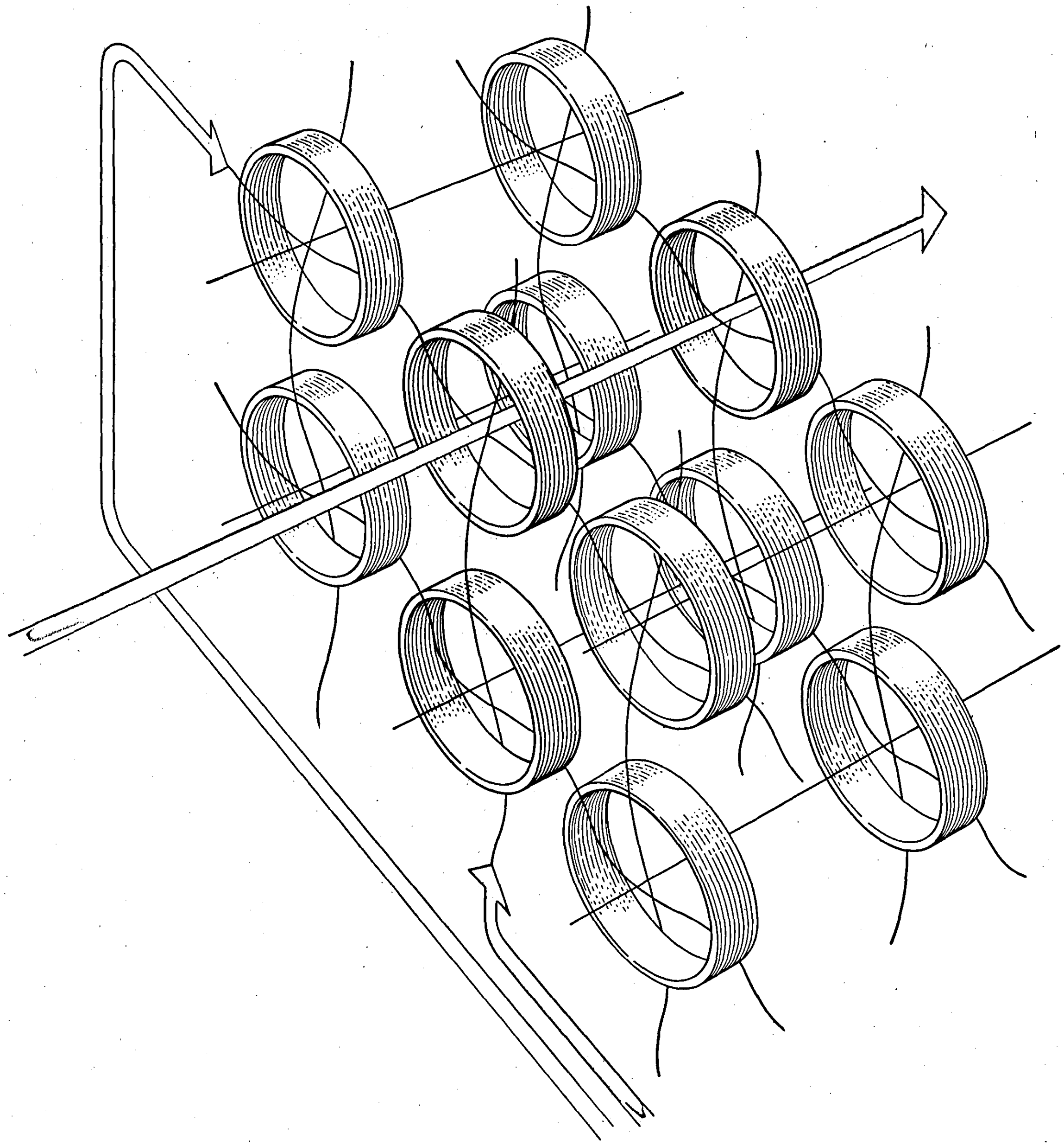
A natural question is, how has this benefited the organization? The evidence, based upon the statements of programming personnel, indicates the debugging delays are ceasing to be a factor in their programming efforts. The lead-time required for program development has been drastically shortened. Scheduling efforts are now approached with a more realistic attitude. Also, as programming commitment dates are routinely met, an organization will realize a savings in programming effort.

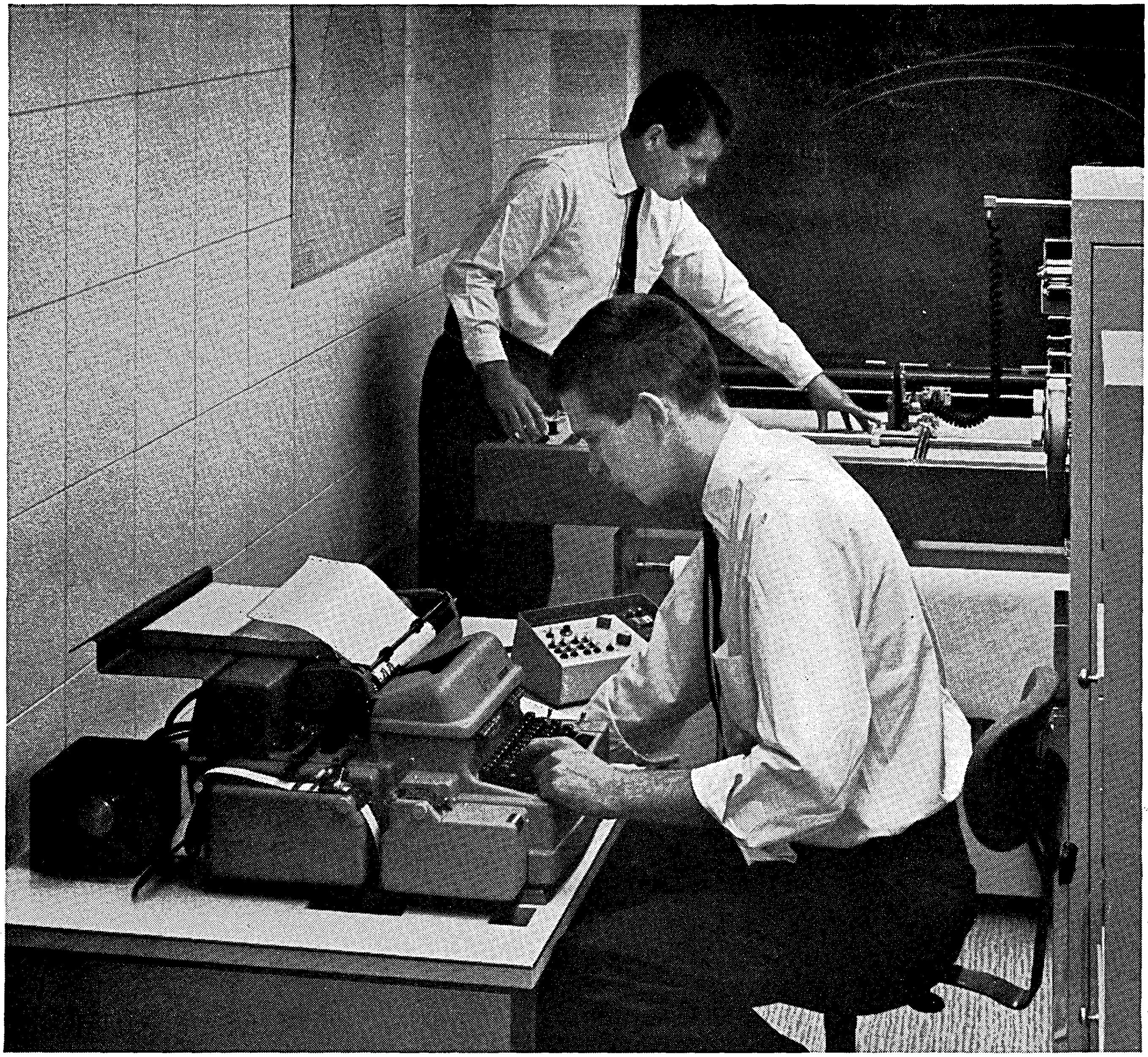
Basically a data processing installation is analogous to a production organization. Its job is to design (engineer) a structure for the processing of information. One does not have to stretch the analogy very far to come to the conclusion that a data processing installation can be sudied with many of the same techniques that are used in manufacturing. ■

NOTES

[1]Hanford Works of the United States Atomic Energy Commission is operated by General Electric under contract with the Commission.

[2]In order to adequately measure the level service, some quantitative unit of measurement was required. To meet this need a DBS (meaning Debug Service) unit was defined which relates, (1) the number of debugs processed within a given period, (2) the average processing time per debug and (3) the average turn-about time per debug. Processing more debugs, within a given period, and/or reducing the average turn-about time per debug, will raise the service level measured in DBS units.





Jet Propulsion Laboratory will use Recomp III for processing data from NASA deep space tracking antennas.

JOINING FORTRAN SUBPROGRAMS

an old problem with new complications

by ASCHER OPLER and MARTIN E. HOPKINS,
Computer Usage Co., N.Y.C.

When algebraic compilers such as FORTRAN were first developed, it was necessary to prepare the source program for any problem in its entirety before compilation could be successfully performed. It was also necessary to recompile the entire program when any statement was found to be erroneous.

Before too long, the concept of compiling a program in smaller sections (subprograms) was developed. It then became possible to compile (and correct) each program and then to use the whole in the form of a collection of subprograms.

With the development of the subprogram concept, there also arose the idea of a data region common to several subprograms. This facilitated the compilation and checkout of individual subprograms, provided an economy in data storage and simplified (often eliminated) the transmittal of arguments of the CALL statement.

This group of concepts which initially constituted the FORTRAN II modification of IBM 704 FORTRAN were well received and have become part of nearly every FORTRAN Compiler developed both for IBM and non-IBM computers. The statements FUNCTION, SUBROUTINE, CALL and RETURN, have been identified with the subprogram concept and the COMMON statement with the use of a common data storage area.

There have been two general methods of implementing this: at a binary relocatable code level and at a symbolic (assembly language) level. The basic problem is one of collecting the main "program" and all its subprograms, allocating space in the object computer for non-common areas, the linking required whenever a SUBROUTINE subprogram is CALLed or whenever a FUNCTION subprogram is referenced, and allocating and referencing COMMON so that the common areas designated by each program will be properly aligned.

binary method

In the older of the two methods, the binary relocatable scheme, the object memory might typically be organized as illustrated in Figure I. The object computer is divided into major areas: a single block of COMMON storage, non-common portions of the main program and its subprograms and a series of transfer points isolated from each subprogram coding (transfer vector).

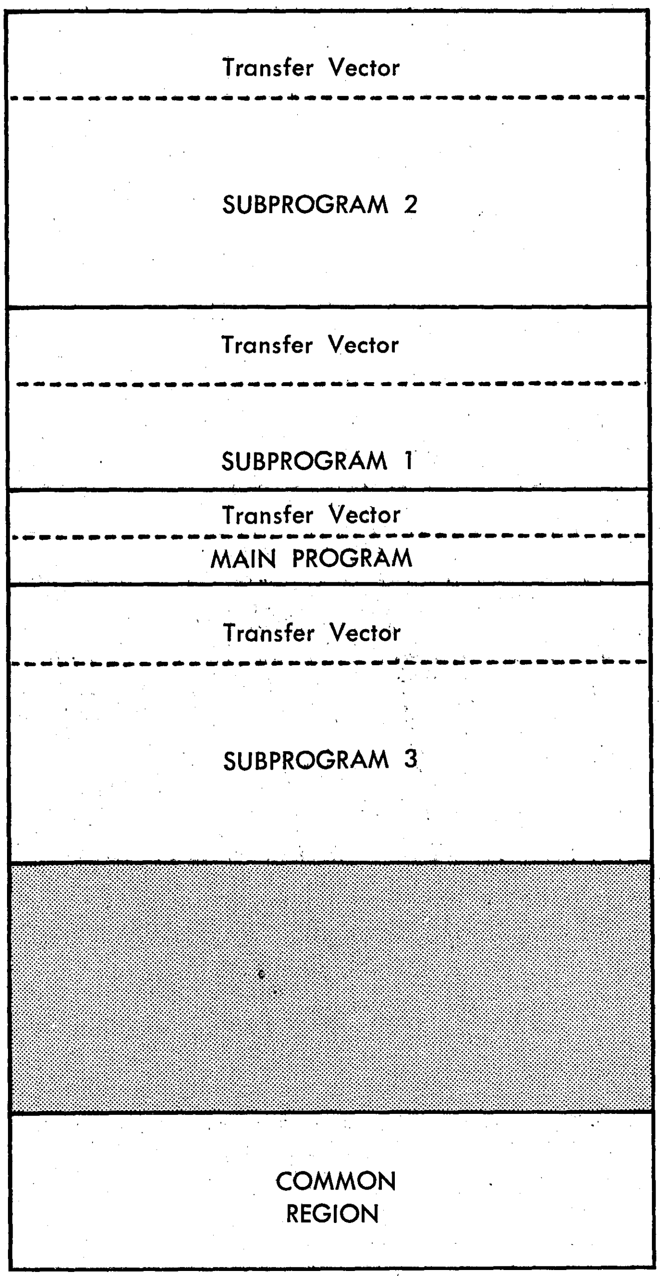
In producing the binary output, a relatively simple scheme is used for assigning compiled words to the COMMON region, to transfer vectors or to the general program area. The machine codes produced by the FORTRAN compiler contains relocatable binary coding for the general area, special coding for the transfer vector and special non-relocatable words for the COMMON region.

The loading of the addresses of the subprograms into the transfer vector is performed in the first portion of a two-phase loading process. This is often done by replacing the symbolic name of a subprogram with a transfer to its actual location in memory.

symbolic method

Several of the FORTRAN-type systems that have been prepared make considerable use of the computer's symbolic assembly program. These FORTRAN-type compilers produce as output a series of symbolic assembly cards (or

Figure 1



card images on magnetic tape). A post processor works the groups of card images into a single symbolic program that can be assembled, loaded and executed. This has not been a simple problem for the implementors. In several of these compilers, the main program and all its subprograms must be compiled as a single batch. Either the assembly program is capable of directly assembling the combined output or a small processor has been built into the compiler. Figure 2A illustrates this technique.

In preparing an algebraic compiler for the Honeywell 800, we were faced with the same problem (with several additional considerations). Because the processing of a main program and all subprograms in a single batch seems to defeat one of the aims of the subprogram method (allowing separate compiling and correcting of subprograms), we devised a technique we termed COLLECTION. This permits the Honeywell Algebraic Compiler to handle any desired programs in a batch independent of the relation to each other as programs or subprograms. Those programs which are successfully compiled (no serious diagnostics) are added to an installation library of active programs called the Collector Program is loaded and the names of *main* programs desired are read in on control cards. The Collector Program collects all subprograms required for each main program and all required library and system routines (input-output, floating point hardware, simulator routines, etc.). After collecting the programs in the form of symbolic card images, the entire program is fed to the ARGUS system for assembly and subsequent execution (see Figure 2B). It is, of course, possible to Compile-and-Collect a batch of programs as a single operation.

the collector program

In the preceding paragraph we spoke of a few additional considerations related to collection. Some of these arise because parallel processing can be performed on the Honeywell 800. (For example, several programs may be run in parallel with other programs.) Operation in this environment requires extremely flexible allocation facilities for programs so that memory may be re-allocated in a variety of layouts. Index register groups and input-output units must also be capable of reassignment in order to permit the widest possible sharing of these components.

The object programs produced by the Honeywell Algebraic Compiler consists of six sections which may be individually assigned. For a program consisting of a main program and 20 subprograms, for example, this means that the Collector may assign up to 126 individual pieces of symbolic program.

To accomplish this, the compiler, when it updates the Collector Tape, prepares an index for each program or subprogram. This contains the number of words of memory required by each section and the names of all lower level subprograms required. When the Collector Program receives the instructions to collect a particular main program, it first operates on the program index and precomputes the proper origin of each section of the main program and each of its subprograms. Then, with the knowledge of the origin of each piece of coding, the Collector Program reads the card images from tape, merges in SETLOC (origin control) cards and writes out the entire reorganized object program. In order to assist the user, an index table is produced (see Figure 3) showing the location of each major section of each subprogram.

To illustrate the extent of relocation, Figure 4 shows a main program and its subprograms as compiled and as they appear following Collection.

additional problems of symbolic collection

Since each compilation is done independently of every other one, the symbolic tags produced as compiler output are often identical in many subprograms. (For instance, the nth executable statement produces a symbolic tag of the form nA.) Thus, all programs will have the symbolic tags 1A, 2A, etc. In order to prevent double definition at symbolic assembly time, the tags for each program have appended to them pairs of additional letters AA BB CC, etc. These may be seen by inspecting Figure 3.

Certain symbols, such as the entry points to subprograms, have ZZ appended to them to prevent their being made unique. Similarly, many systems symbols were

Figure 2-A

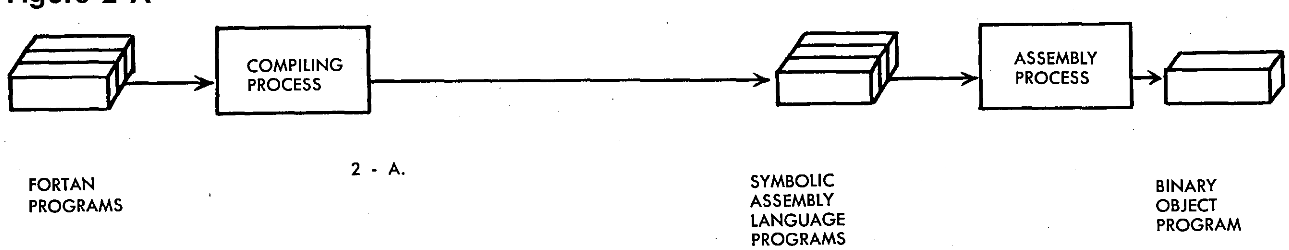
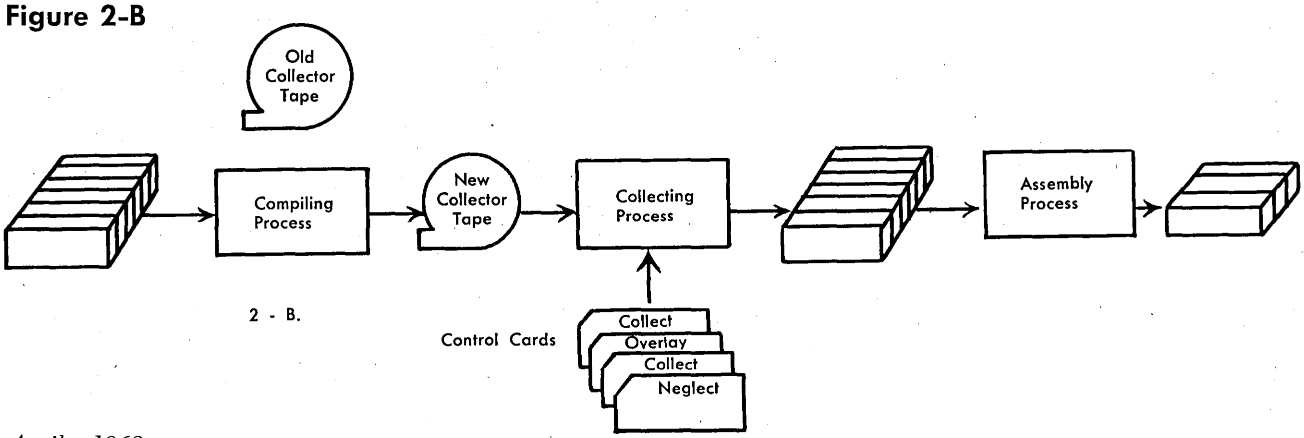


Figure 2-B



devised so that they would not be altered by the Collector Program.

other features of the collection program

Since post processing is a convenient time to make operating decisions, the Collector is able to arrange for the operating system to handle overlay of portions of programs too large to fit in available memory. In the technique used with the Honeywell Algebraic Compiler, overlaying pieces must be SUBROUTINE subprograms. The overlay is controlled quite simply by using the CALL statements. When a SUBROUTINE is CALLed, if it is in memory, the conventional link to it is made; if it is not in memory, control is transferred to a program which brings it into memory before linking.

Naturally, this requires a special type of allocation to make certain that required parts of the program are not destroyed by the overlay action. When the Collector is informed that a SUBROUTINE may overlay, it inserts the overlay control program and produces a special memory allocation. With such a post-processing technique available, the same program may be operated differently in different situations. If the program, for example, may use 8 K of memory on one day and the total program will fit in memory, no overlay will be produced. On another day, perhaps only 4 K of memory is available. Without recompilation, the same program may be collected to execute with overlay.

Another useful option is NEGLECT. Very often, with large systems, several of the required subprograms are not completed at the time when testing must be started. If NEGLECT control cards are fed to the Collector, instead of inserting the named subprogram, a return jump is used. This is in lieu of the subprogram to be neglected it has not yet appeared on the Collector Tape.

The advantages and disadvantages of FORTRAN-type compilers producing symbolic output is still being debated. The symbolic route provides a more readable output which may be readily modified, and may utilize advanced features of the assembly program (e.g. multiple sequence counters, macro-instruction generators, etc). On the other hand, the symbolic route is generally more time consuming, may need more manipulation, and may require post processing between compiling and assembling. Post processing provides better control over selection of subprograms and library routines and permits better control of overlay mechanisms.

Recently announced improvements in FORTRAN and the development of consistently improved ALGOL processors will surely bring forth new approaches to this problem which continues to divide compiler writers. This should surely lead to improved implementation of tomorrow's compilers. ■

Figure 3

	PROGRAM SUMMARY	BANK	LOCATION
ABER	AA		
	COMMON SPECS	01	0273
	ERASABLES	01	0384
	PROGRAM STRING	01	0291
ACER	BB		
	COMMON SPECS	01	0273
	ERASABLES	01	0440
	PROGRAM STRING	01	0386
AEER	CC		
	COMMON SPECS	01	0273
	ERASABLES	01	0533
	PROGRAM STRING	01	0442
AHER	DD		
	COMMON SPECS	01	0273
	ERASABLES	01	0616
	PROGRAM STRING	01	0535
AJER	EE		
	COMMON SPECS	01	0273
	ERASABLES	01	0705
	PROGRAM STRING	01	0618
BIFTEST	FF		
	UNCOMMON ARRAYS	01	0204
	COMMON SPECS	01	0273
	ERASABLES	01	1045
	PROGRAM STRING	01	0707
IKER	GG		
	COMMON SPECS	01	0273
	ERASABLES	01	1132
	PROGRAM STRING	01	1048
IMER	HH		
	COMMON SPECS	01	0273
	ERASABLES	01	1191
	PROGRAM STRING	01	1135
INER	KK		
	COMMON SPECS	01	0273
	ERASABLES	01	1272
	PROGRAM STRING	01	1193
IPER	LL		
	COMMON SPECS	01	0273
	ERASABLES	01	1360
	PROGRAM STRING	01	1274
*CONSOLE			
	PROGRAM STRING	00	0576
*OBJIO			
	PROGRAM STRING	00	0760
*MASKOBJ			
	PROGRAM STRING	00	0512
COMMON			
	COMMON ARRAYS	00	1982

BIFTEST SEG 1

COLLECTED INDEX

Figure 4

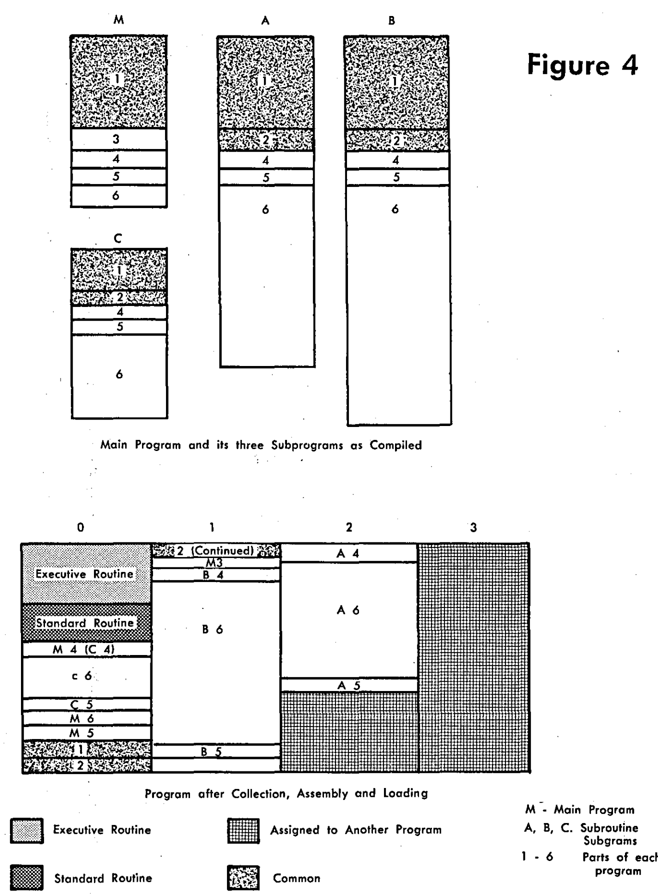
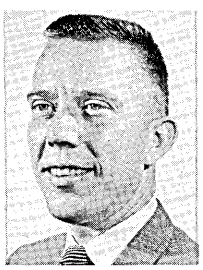


Figure IV

PITFALLS & SAFEGUARDS IN REAL-TIME DIGITAL SYSTEMS

with emphasis on programming

*part one, by W. A. HOSIER, Systems Engineering & Management Operations, Sylvania Electric Products, Waltham, Mass.



Ever since the advent a decade or so ago of fast and reasonably reliable digital computers, such computers have tended to play an increasingly important central role as controlling devices in systems. *Datamation* readers should require little introduction to digital systems as such. Some systems serve primarily for record-keeping or simulation, and can compress or expand time to suit their convenience, in that machine operations of any hour may represent indifferently a minute or a month in the real world. But when such a system attempts to control or monitor a rapidly-changing real physical environment, or even to simulate one for realistic training of personnel, it must employ real time as its basic independent variable. Hence the term "real-time system." Such a system might be small, simple, and slow, but in that case a modern stored-program computer would probably not be needed to control it. To the contrary, most real-time digital systems involve a lot of farflung apparatus with complicated interaction, make pressing time demands, and cost several million dollars.

This is the type of system with which the present discussion is concerned. It always has an organization like that shown in Fig. 1, although the various subsystems differ internally from one task to another, and subsystems of any type shown may be added, omitted, or combined into dual-function subsystems.

Since they are among the most complex and delicately coordinated of modern engineering enterprises and involve a wide variety of equipment and techniques that frequently tax the state of their respective arts, it is hardly surprising that large real-time digital systems pose peculiar problems of technical management. The most perplexing area is commonly that of the central-control device, where inadequacy impairs performance of the entire system, and safety factors are often very ex-

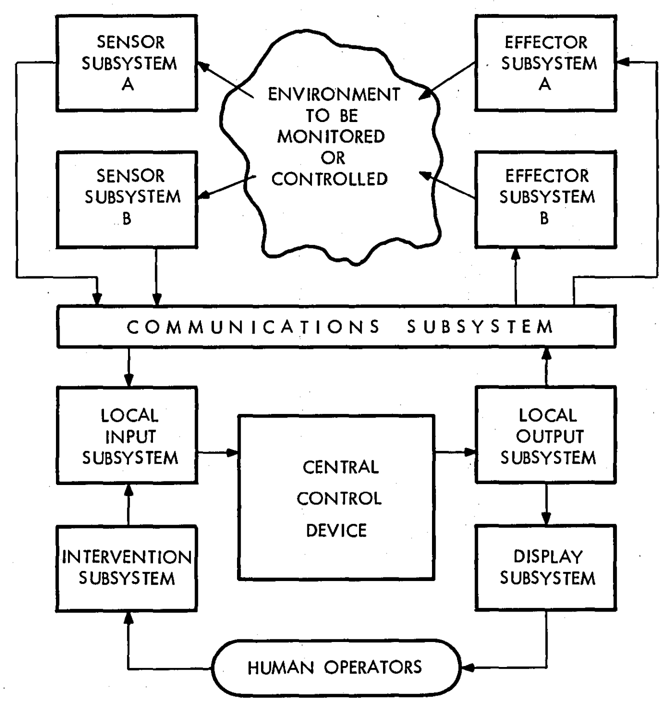


Figure 1. Typical Organization of a Real-Time System

*W. A. Hosier was first associated with digital computing at M.I.T.'s Lincoln Laboratory from 1952-1957 where he participated in the design, programming and testing of the prototype SAGE system, and supervised the first computer (MTC) which used a coincident current ferrite memory. Since 1957 he has been at Sylvania with responsibilities for the design of the Plato anti-missile system, and the selection and configuration of computer equipment for BMEWS.

The following article is the first of a two part series, the second part will appear in May. In a different format, it was first published in IRE Transactions, June 1961, but has been substantially revised by the author to better suit the specific interests of *Datamation* readers.

pensive indeed. Furthermore, the perplexity is aggravated by the need to program this device. Program and hardware in a real-time digital system are so intertwined that changes in either will almost always have repercussions in the other; yet the capabilities and limitations of computer programming are frequently not well understood by system managers. Real-time digital systems thus present, in their central-control devices, a unique combination of stringent hardware requirements and an elusive programming task. Experience has indicated that it is on proper conceiving and handling of this central area that such systems usually stand or fall, and it is to this area that the present discussion is addressed.

Closely allied to this is the task of testing the system and its control equipment, both during its construction and after installation. It is characteristic of large real-time digital systems that they have only partial control over their environment. The rest is not easily manipulated and is subject to wide variation of many interdependent parameters (consider, for example, an air traffic control situation). This makes thorough testing difficult and expensive, and it puts a premium on the intelligent design of experiments, sampling, and simulation.

system genesis

The decision to proceed with full-scale development of a particular real-time digital system will normally have been preceded by studies of feasibility, economic merit, and broad definition of function. Starting from these, the real design work begins.

The preliminary studies will have indicated approximate subsystem makeup and critical technical areas. As a first step toward making specific choices, competent technical people representing each of the significant subdivisions must be gathered together to produce a tentative design plan. At least three suggestions are pertinent to the makeup of this group: 1) that it be as small and as competent as possible; 2) that programming be represented in it from the start; and 3) that all its members be able to communicate with each other. This last is not as trivial as it may sound: technical specialists in the diverse fields of a typical system often use quite different terminology and confuse or misunderstand each other. It may be necessary to add one or two men of more general system experience to bridge these gaps and to help resolve differences of viewpoint. As a final general suggestion, 4) this group should be kept closely knit until it produces a written document adequate to guide further specialized work. Too often, an ill-considered so-called "plan" will emerge from a loosely-connected series of meetings where no real meeting of minds has ever taken place. Early effort to define tasks clearly and to make them consistent with a common system goal will more than repay its cost when balanced against duplications and contradictions that would otherwise ensue.

The following less general points should also be noted.

1) In establishing the design boundaries of subsystems, their functional autonomy and future ease of testing as subsystems should weigh at least as heavily as their suppliers' capabilities and preferences.

2) A policy should be adopted on monitoring and checkout equipment – specifically, on how elaborate and centralized it is to be. Something of this nature is indispensable; it is bound to affect subsystem design; and working it in as an afterthought can be quite awkward and expensive.

3) An analytical effort should usually be set up to study the effects on the system of errors and delays, of queueing and traffic variations, and whatever other special problems the system engenders. Part of this will need to be responsive to designers' problems on a job-shop basis, but part should also be free to search the system for such neglected corners as no individual subsystem is likely to attend to.

4) Provision should be made for orderly growth of system documentation.

5) It is axiomatic (but often flouted) that design responsibility and its companion authority ought to be clear cut. Almost as obvious, but apparently more difficult to observe in the face of competing projects and promotions of personnel, is the need for continuity in this responsibility and authority. Sudden personnel shifts without sufficient break-in periods are always characteristic of poor management, but especially so in closely-coordinated system engineering.

selection or design of central digital equipment

Selecting the best digital computer for any task big enough to warrant one is never an easy decision. It is further complicated in a real-time system for at least the three following reasons:

1) The computer must be reasonably matched to the rest of the system. If it turns out to be too small or too slow, the system will be inefficient or even worthless; if it is much larger or faster than necessary, its initial cost and upkeep will be an expensive luxury. There can be no "second shift" to deal with overloads.

2) The input-output problem is vastly more complicated than cards, tapes, and printer. Special buffering and control are almost always required, although modern high-speed memories have greatly reduced this problem.

3) Real-time applications usually demand continuity of operation, although the critical period (as in the case of missile guidance) may be brief. The consequences of errors are likely (as in the case of industrial process control, or ICBM interception) to be disastrous. This implies a highly-reliable machine with fail-safe features, an easily maintained machine, and frequently one or more standby machines with complicated quick-switching apparatus.

Let us consider these three questions in more detail:

Matching Machine Capability to the Task: The matching of a complicated digital computer to a complicated real-time task is a formidable intellectual undertaking that no one has yet succeeded in attacking by more than crude empirical methods. Hopefully, a second John von Neumann will appear among us and figure out an approach; but until that day, system designers will have to make do as best they can, try to err on the safe side, and keep their fingers crossed. What is lacking is a measure theory. Some aspects of the problem, such as gauging the amount of arithmetic and sorting and table searching, are straightforward, though tedious; but these are only the beginning. Machine time and high-speed storage requirements in any given case are quite sensitive to many less tractable aspects of the problem. One is the interrelatedness of the data; this determines the size of data-blocks that must be handled as units and the amount of cross-posting and cross-checking. Another is the detailed format of each input and ouput item: taking these apart and putting them together can be awkward and time consuming if they are carelessly arranged. A third item, often hard to determine until the system design is well along, comprises the timing constraints which external apparatus imposes on the computer: the precision with which certain operations must be synchronized and the time that data must be allowed to accumulate in certain "hoppers" (buffers) before they can be emptied.

Physical and environmental constraints imposed by the system frequently narrow the choice of machine further.

Some loosely-defined systems may be so open-ended that expandability of the central control equipment enters heavily into selection.

In any event, the capacity of a digital machine relative to a task is some sort of compound of

1) the size of its high-speed internal memory;
2) its execution speed, which usually means its internal memory speed;
3) the suitability of its instruction repertoire and word make-up to the particular task;
4) the efficiency of its input-output equipment, and
5) the skill of its programmers.

Theoretically at least, trade-offs in all directions are valid among these five constituents. Practically speaking, however, in large systems with present technology, one usually finds that condition 1) is the critical item. Since it may be quite awkward to expand memory size after a computer has been built, this item warrants as close scrutiny as designers can give it.

Estimation of Storage Requirements: Sometimes the program of a real-time system can operate piecemeal, only part of it being in high-speed storage at any one time. If this is the case, then it is necessary to estimate the size of the largest single piece that must operate as a unit, making due allowance for a supervisory routine and buffer space to effect the speedy interchange of pieces.

Whether dealing with the whole program or its largest part, an estimate must be made of the number of words to be stored, and the more accurate the better.

By whatever means the figures are arrrived at, the following categories must be covered:

1) Stored program and fixed data (the latter covering constants, function-tables, and what are known as "masks")
2) Space required for data in process. This includes input buffer space, intermediate tables where data must accumulate between processes in the program, output buffer space, and a "miscellaneous" allowance to cover control, cross-referencing, and odd bits of bookkeeping.
3) If routine access is to be had to blocks of data (or program) in auxiliary storage devices, allow adequate buffer space for manipulating these blocks with a minimum of interference to other operations.
4) Finally, a safety factor of twenty-five per cent or more, depending on the estimator's self-confidence and the likelihood of expansion in program requirements. (They *always* expand).

Estimation of Speed Requirements: Although the swiftness of moden computers usually makes speed a less critical factor than internal storage (which of course bears on effective speed), nevertheless the system designer must satisfy himself that the speed of the machine is sufficient for the heaviest traffic likely to be imposed on it. Most of the time consumed by a program is likely to be used by a few often-iterated loops of instructions. To estimate the total with any accuracy, the number of instructions in each frequently repeated loop must be rather closely known, as well as the number of repetitions demanded of that loop. Seldom-repeated parts of the program can be roughly estimated or even ignored. Since the number of repetitions of loops will usually depend on the density of input traffic, and secondarily on output requirements, these must be defined as specifically as possible. Average and peak data characteristics will be needed, as well as the degree of repetition or redundancy which may permit the machine to ignore part of the data under overload conditions. Formats, hold times, and randomness or regularity of occurrence are pertinent; likewise are any special constraints such as quick-response demands or need to use certain output channels with maximum efficiency (*i.e.*, minimum idle time).

This procedure of predicting time requirements is an exercise in cost accounting, where time is the currency. Like cost accounting, its success will depend on how shrewdly materials, processes, and products are categorized and on how detailed and accurate a breakdown of costs is available. Many real-time digital systems, especially military defense systems, have as a cardinal requirement the need to handle unpredictable peak loads. Since these loads are arduous and expensive even to simulate, a sound analytical cost-accouting approach, refined at intervals by experimental feedback, is the only practical way to predict the program's time behavior under stress. It is particularly useful in the fateful initial step of machine selection.

One should bear in mind (and the cost-accounting formula should reflect) that the time consumed will probably be a nonlinear function of input density, varying rather as the square of some higher power. This is especially true where the program is required to find correlated items in the input.

If external signals requiring special responses play a significant role in the system, the trapping or multi-sequencing facility built into a given computer can have an important influence on program time requirements.

Instruction Repertoire: The suitability of a machine's instructions to the specific system task has bearing on speed, storage requirements, maintenance and cost.

The details will have to be studied in the light of requirements; general considerations of convenience and speed will govern much as they do in any machine application.

For example, the number of index registers and the ease of manipulating them may be important. Floating-point may be mandatory in one system and superfluous in another. Programmers who have studied the problem are the persons best qualified to make this sort of judgment.

Any machine is likely to have certain selling points ideally suited to one system and useless or even detrimental to another. Automatic square root is an example, "scratch-pad" registers another, "microprogramming" a third. The important consideration when presented with such extra features in a sales pitch is to know the problem so as to assess their specific utility and not to let them bias one's judgment of the machine's other (and probably more important) characteristics.

The degree of saturation of a machine's instruction repertoire is also pertinent, for the reason that use of the machine in a real-time system is quite likely to require addition of a few special instructions for communication between the program and external elements of the system. These will probably be simple "on-off" signals in both directions, but it can be quite awkward to install them if the necessary spare circuit logic is lacking.

Input-Output: If the data traffic is to be heavy, one or more fully autonomous channels will be highly desirable; if not, the expense of such channels is an unnecessary luxury, but the I—O system should still interfere with and delay the internal processing as little as possible. At a minimum, the internal memory access which receives input or yields output (as distinct from the *initiation* of an I—O operation) should occur as an automatic "break" timed by external equipment, independent of program attention.

There are two aspects to computer input and output in most real-time systems: the potential ability afforded by the design of the selected central processor and the specific ability built on this by adding special equipment designed to fit particular system requirements.

The potential ability is of course the important thing in machine selection; but between two machines of roughly equal potential, inspection may show that special system devices are easier and cheaper to add in one than the other, or even that one machine eliminates the need for some of these devices.

One thing that must be known within rather close limits in order to assess input-output requirements intelligently is the detailed timing of data flow to and from external devices in the system. Preliminary bounds will have to be set in order even to select a machine; to proceed with the construction of special equipment and of the program, a whole category of detailed effort, taken up below under "Definition of Interfaces," will be required.

Continuity of Operation: Most writers would head this paragraph "Reliability," but this is a misleadingly simple term in the system context. Simple circuit reliability and mean error-free operating time are fundamental, to be sure; but easy maintenance and the smooth substitution of standby equipment are almost equally important. Despite much theoretical treatment of automatic error correction, any computer which a system can afford to buy now or within the next decade will make an occasional mistake. The error rate for a good modern machine is impressively low: probably less than one error per 50 billion instructions; but it can not be ignored. The useful attitude toward errors, as toward death, taxes, and sin, is not how to abolish them, but rather how to keep them within bounds and live in spite of them.

The first thing to do with errors is be aware of them, or at least of any that are serious enough to affect system performance.

Let it be said to begin with that it is flatly impossible to check every internal detail of computer operation; nor is this necessary. For most purposes, a large stored-program computer, shrewdly programmed, is its own best monitor.

The machine selected should have enough spare capacity to permit including self-checking in the program. Unfortunately, a computer can always stop, or depart from its intended cycle, and thus fail to check itself. No real-time system should be without the means of promptly detecting this condition. The simplest solution is usually to provide an independent clock that will set off an alarm unless the computer "punches in" every few seconds like a watchman making his rounds.

Extra circuitry for automatic error detection is helpful in small amounts. A common example is single-bit parity checking of each word stored in high-speed memory.

As long as such extra circuitry is simple by comparison with what it is supposed to check, it is probably justifiable; but increasing its ratio adds noticeably to expense and raises the old question, "Who guards the guards?"

If the expense is warranted by system requirements, added confidence in operation can be had by using two identical machines in parallel and comparing their outputs.

In addition to checking the central processor's internal operations, it will be desirable to check the integrity of its input and output channels. The machine can not do this unaided. Either an external checking device should introduce simulated inputs and verify the resulting outputs, or provision should exist for connecting the machine's output channel through a buffer to its input channel, thus forming a closed loop whose integrity the machine can verify.

It is thus quite feasible to obtain error indications sufficient to monitor the machine's effect on system performance. What to do with them after one has them is quite another matter. They must be displayed; the operator must take remedial action; some remedial action can be made automatic; but no general answers can be made to the questions of how and what. This issue is sure to provide vigorous debate among human factors experts, system analysts, and equipment designers.

After fault detection, maintenance is a question of localization and repair. Repair is mainly facilitated by modular packaging and adequate spare modules; it is the localization that is usually difficult in a device as intricate as a digital computer. Out-and-out failures are not too hard to locate, but subtle intermittent troubles have been known to take weeks to track down. Many things can contribute to quicker diagnosis, and attention should be paid to as many of them as possible. In the machine itself, simplicity and regular arrangement are helpful, both logically and physically. In addition, physically accessible construction and the clear and systematic marking of terminals are important. It is desirable to be able to run the machine in "slow motion." The "on" or "off" state of all significant switchable elements (there may be thousands) should be visible somewhere, if only on back panels. Local fault-detecting circuits, if simple (as discussed above), are good. Peripheral units (input-output channels, etc.) should have test controls independent of the central processing element and memory. Marginal checking facility deserves further discussion (see next paragraph). As adjuncts to the machine, there are, first, its maintenance manuals: are they well-organized, complete, and specific? There should be diagnostic programs carefully designed to locate and indicate faults. Finally, there is the care given to selection and training of maintenance men. Their task is quite analogous to a physician's; good ones are rare.

Marginal checking, alluded to above, is a rather special feature not found in all machines, which can be quite expensive and whose merits are hotly contested.

If it is to aid in localization, it must be possible to segregate small parts of the machine for stressing; further, if the general procedure is not to be too time consuming, it needs to be automatized—*i.e.*, built so that the program can control the stressing. Altogether this is a large order. If marginal checking plays a significant part in determining machine choice, a real expert ought to examine it.

Decentralization: There are obvious virtues in dividing system control among two or more central machines if the logic of system-data flow permits. This is more true if the division is a parallel one with each machine doing a similar task than for serial division where each machine does a different task. However, if there is much interdependence among machines, the resulting problem of coordination and control can easily outweigh the limitations of a single machine. If such load sharing is contemplated for reliability reasons, system analysts should make sure that they are strengthening the weakest link in the system. For example, if a system depends on long communication lines, over-all reliability may be better served by augmenting these lines than by decentralizing and duplicating control devices. Decentralization is more a system question than a computer question.

Influence of Machine Choice on Program Production: In selecting a computer for real-time system control, delivery schedules will certainly be a paramount consideration. A point that is likely to be overlooked by system managers is that program delivery is just as important as machine delivery, and that this can be drastically and adversely affected by a machine choice that seems innocuous from other standpoints.

If a machine is chosen for which utility programs are not immediately available or for which no equivalent is immediately available on which to assemble and test system programs and simulation, there will be an unavoidable lag in performing essential programming tasks.

To alleviate programming delay, it may be proposed to simulate one computer on another that is logically different. This is not impossible, but it is seldom satisfactory. System managers should be skeptical about it and about relying on new and untried utility programs. Both procedures are likely to harbor subtle difficulties that no one anticipates; these erupt like delayed-fuse bombs and play havoc with program scheduling.

As a last admonition on the definition of system hardware, it is preferable to design initially as much of the system function as one can afford into the hardware, rather than to impose unnecessary tasks on the program of the central machine. Trade-offs between program and hardware are usually numerous, and it will appear that putting the burden on the program is cheaper. Frequently, especially if change can be foreseen (which is usually easier and cheaper to reprogram than to rebuild), the program should bear the burden. It is a great temptation, as small shortcomings of hardware design are brought to light, to "correct for that in the program." But as many small tasks accumulate, the program's capacity to perform its more basic function can be impaired. This may not be realized until too late. At the end of the game, in the system integration phase, these are bound to be oversights that *must* be compensated by program additions. If spare capacity is left in the program by absorbing all feasible changes in hardware, this cushion against eleventh-hour blows will help to avoid what has come to be known as the "agonizing reappraisal."

interface definition

It was pointed out at the beginning of this discussion that a real-time system will embrace a variety of devices which must communicate with each other. They are seldom designed so that nothing more has to be done than plug them in.

Each interface may have peculiar requirements of its own and these must be stated in minute detail if the gap is to be bridged successfully. The exact interpretation of digital formats, the rise and fall times of waveforms, load impedances and their limits of variation, special restrictions as to when each type of data may or may not be sent—these and sundry other details must be agreed on by all parties concerned and clearly written down. Accomplishing this is apt to be a monumental and tedious chore, but every sheet of accurate interface definition is quite literally worth more than its weight in gold. This is a basic responsibility of the system manager; it probably will have to be done in several passes of increasing detail; but the sooner it is down in black and white, the clearer everyone's job will be.

A system will have many interfaces other than those at the central digital device. Getting proper electrical or mechanical matching at the computer interfaces is much the same problem as elsewhere; but the question of logical matching—*i.e.*, digital format and its precise interpretation, a secondary concern to the equipment engineer—is especially important because it bears, as will be more fully explained in the following section, on that impalpable and elusive thing, the computer program. ■

an 8-year-old "learns by doing"

JEREMY & THE G-15

A new method of instructing college students in the operation of the Bendix G-15 is now being tested on a group of junior and senior engineering students at UCLA. If it doesn't work, there may be some red faces because it has been successfully tried by an 8-year-old boy.

The new method is outlined in a manual entitled "Auto-Instructional Text on the Operation of the Bendix G-15 Computer — 1000S Interpretive Routine," written by Richard S. Pierce, Arnold Roe and Arie Y. Lewin of the UCLA engineering faculty.

The 8-year-old boy who read the manual and then operated the computer (assisted by some verbal coaching is Jeremy Kramer, son of Mr. and Mrs. Henry P. Kramer of Santa Barbara.

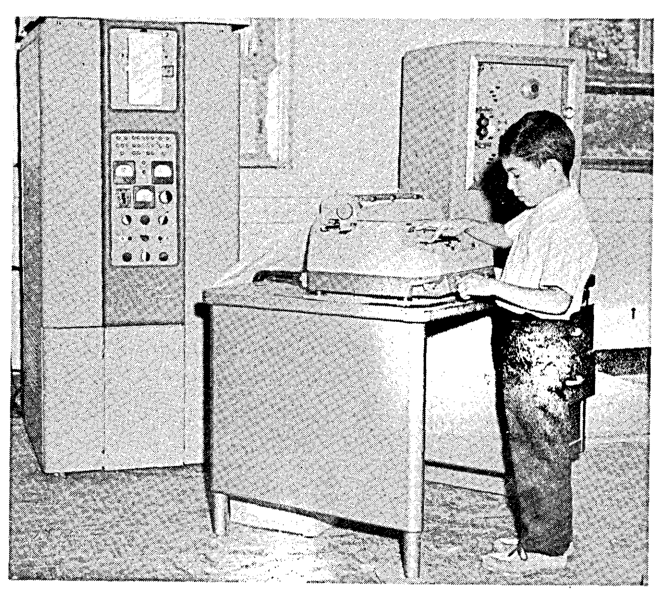
Jeremy got "into the act" when he accompanied his father, a mathematician, on visits to UCLA last summer. The elder Kramer is a friend of Roe and was interested in techniques embodied in the manual.

The new system calls for the student to read instructions in the manual and then operate the computer. It is a "learn by doing" method.

Jeremy, who learned to read the New York Times at the age of 4 and is one grade ahead of his age group in school, became interested in the manual and before long was able to carry out the fundamental steps involved. He is in the fourth grade at the Roosevelt School in Santa Barbara, and may be the youngest computer operator in the world.

For the UCLA students, a prerequisite to use of the manual is a knowledge of Intercom programming. Only four students will be engaged in the new teaching system at one time.

During the semester, half of a group of students will be taught by the conventional lecture method used heretofore and the other half will be taught by the new manual system. Results will be compared at the end of the semester. ■



While admittedly a surface skimmer of a highly involved, sometimes sensitive subject, author Kolence nevertheless tersely expounds on the pros and cons of computing's geographic sociology. And although his balance scale rests delicately on a base of highly personal value judgments, his conclusions have the virtue of more than a modicum of geographic experience.

From 1953-1955, Ken Kolence worked on the ILLIAC at the University of Illinois followed by a Navy tour at the David Taylor Model Basin in Washington, D.C. where the UNIVAC I drew his attentions. In 1958, he shifted his environment to New Jersey where his efforts were directed at a 709 on RCA's BMEWS project. Early in '61, the Eastern climate encouraged relocation to Los Angeles and NAA's flock of 90s.

COMPUTING CHARACTERISTICS EAST vs. WEST

an edge for the latter

by KEN KOLENCE, General Supervisor, Programming, Business Automation Section, North American, Los Angeles, Calif.

Trying to characterize computing on the East Coast and again on the West Coast is like trying to talk about the differences between alligator farms in Los Angeles and Miami Beach. A lot of roaring goes on, hides have got to be thick, and there is a lot of bull in both places. It is not until you observe closely that you can begin to tell them apart.

To begin with, there is really no such thing as East Coast Computing because a fairly heavy concentration of machines exists all the way from Boston to Cape Canaveral. West Coast Computing, on the other hand is a very real thing — an omnium-gatherum of Los Angeles installations and scattered West Coast Aerospace Industries, wherever they may be. However, the substance of West Coast Computing is not only the closeness of the installations, but the spirit of camaraderie and co-operation that has existed locally since the beginning of computers. It is this spirit that the East Coast lacks, and which makes the concept of East Coast Computing so vague and in truth, lackluster.

The co-operation on the West Coast is greatly encouraged by the problem mix, of course, which is similar in several different areas. The Aerospace industry uses the same type of computer almost universally, and therefore faces many similar problems regarding machine configurations and operations. The people in computers get together more often socially too. The L. A. Chapter of the ACM has over one thousand members—out of less than nine thousand nationally—and two other large chapters are in the metropolitan area. The Special Interest Committees of the ACM have their only local chapters in Los Angeles, and are beginning to attract more and more good people to work on them. In general, the people who constitute West Coast Computing are active people, forming the backbone of User's Groups and the "young Turks" of the ACM.

West Coast Computing is intensely interested in computing as a profession, and accordingly provides many means by which people can get together after work and talk shop. Also, because of this interest and the heavy concentration of machines, the Universities and local colleges offer a truly astounding number of special courses in various aspects of computers. They range from the usual "Elements of Data Processing" level in a continuum up to courses on compiler theory and the use of IPL V. Even more amazing (to Easterners) is the fact that courses are available on almost any machine on the market. Without a doubt, the West Coast — and particularly the Los Angeles area — provides more educational facilities for computer people than any other geographical region in the world.

The number of people working in West Coast installations must be upward of 20,000. Although this is a guess, it is an educated guess based on the ratio of ACM members to non-ACM members in groups I have known. This means that this many people have been brought into computers on the West Coast in the last 6 or 7 years. It also means that the west Coast has scraped the bottom of the barrel as far as *outstanding* talent is concerned. The first generation of such talent has been on the scene for some time, the second generation has yet to arrive.

The East Coast, on the other hand, is characterized by the isolationist attitude toward information exchange between installations. However, this is breaking down more and more as the density of computers increases, as it has in New York and Washington. The East is also improving its educational facilities at the college level quite rapidly. Since the East Coast has a much larger manpower pool to draw on, we may expect to see more oustanding talent coming up from that area. Strangely enough, the combination to date of comparative isolation and low density of computing personnel has given the East Coast a definite lead in producing original ideas in the field. Symbolic coding, GPS, the monitor concept, CL-1, Decision Tables, the BEFAP macros—all came from Eastern Installations (not manufacturers.)

Another thing the East Coast has in its favor is the wide variety of problems, in many different applications areas, that are being programmed. The West Coast, with a much smaller variety of industries, cannot begin to match the mix of programming available in Eastern installations. This in turn, seems to attract high caliber people into computing at a faster rate than on the West Coast.

It would therefore seem that the primary advantage the West Coast presently holds over the East Coast is the higher density of computing people, with the correspondingly high degrees of communication and interaetion between them. The quality of East Coast programming may be spotty, but there is enough good work going on to be assured the West Coast will have to work hard to maintain whatever slim lead it may presently hold. ■

IFIP-62 CONGRESS

21 countries to be represented

Three main areas of interest will form the nucleus of the second Congress of the International Federation for Information Processing (IFIP 62) to be held in Munich, Germany, from August 27-September 1. The Congress, expected to be attended by several thousand information technologists from 21 countries, will follow this format:

I. Scientific Program:

To consist of three sessions on hardware development including peripheral equipment; one general, state-of-the-art session of invited papers; 20 sessions of submitted papers of broad interest, and 26 symposia of specialized interest including several panel discussions.

II. IFIP Interdata:

The exhibition of edp equipment will be held at the Munich Exhibition Ground from Sunday, August 26, to Sunday, September 2. Exhibition hours are from 9 a.m. to 6 p.m. every day, except August 28 and 30, when the exhibit will be open until 9 p.m.

III. Plant Tours:

During and after the Congress, five plant tours will be held for limited groups. There will be no charge for the tours, and transportation will be provided by the firms conducting the visitations. However, food and lodging will be paid by the tour participants.

The scheduled tours are:

a. Munich: Siemens & Halske. One half-day during the Congress.

b. Germany: IBM Deutschland, Sindelfingen; Standard Elektrik-Lorenz, Stuttgart-Zuffenhausen; Telefunken, Heilbronn. Begin at Munich on Sept. 3 and end at Heilbronn on Sept. 5.

c. England: International Computers and Tabulators Ltd.; Elliot Automation Ltd.; EMI Electronics Ltd. Begin at London on Sept. 6 and end at London on the following evening.

d. France: Cie. des Machines BULL; Cie. Industrielle des Téléphones; Cie. Européenne d'Automatisme électronique; Societé pour l'Exploitation des Procédés S.E.A. Begin at Paris on Sept. 6 and end at Paris on the following evening.

e. Italy: CEA-PEREGO Milano; Olivetti Divisione Commerciale Elettronica, Milano. Sept. 6, one day.

Applications for the plant tours must be made on the registration form for the Congress, and will be considered in order of receipt.

The opening session of the Congress will be held at the Exhibition Ground, in the "Bayernhalle," on August 27 at 10 a.m. From 9 to 9:50 a.m., bus service will be available from the Technische Hochschule (location of the Congress Bureau) to the Exhibition Ground.

Main Congress sessions will take place at the Technische Hochschule. A lounge and several discussion rooms have been set aside for Congress participants.

The closing session with invited survey papers will be held in the "Bayernhalle" on Saturday afternoon, Sept. 1.

The IFIP Program Committee has provisionally accepted 100 abstracts of papers from the 650 submitted. American authors submitted 350 papers, of which 28 were accepted. The final selection of 88 papers was made last month.

Included in the American papers are: *Extending Management Capability by Electronic Computers,* by Andrew Vazonyi, Thompson Ramo Wooldridge; *Mathematical Analysis of Merge Sorting Techniques,* by W. C. Carter, IBM; *The Multi-List System for Real-Time Storage and Retrieval,* by N. S. Prywes and H. J. Gray, Moore School of Electrical Engineering; *Computer to Computer Communication at 2.5 Megabits/Sec.,* by N. Clark, Control Data Corp., and *System Requirements for Direct Execution of a Data Processing Language,* by James P. Anderson, Burroughs Corp.

Subjects to be covered by papers include: business data processing; partial differential equations; information retrieval; digital communication; machine learning; artificial perception; programmed languages and their processing; memory techniques, and switching theory.

The series of symposia and panel discussions will feature industrial simulation; modern techniques of language translation; coding theory; pattern recognition; languages for processor construction; ultra high-speed computers; multiprogramming; university education in information processing, and optimum routing in large networks.

Selection of panel leaders and participants is currently underway, and a complete roster will be announced shortly.

A full round of social events is planned, ranging from a beer party, a visit to Munich's Rokoko Theater, an excursion into the Bavarian Alps, and a Congress banquet.

The United States delegation to IFIP is headed by Dr. E. L. Harder (Westinghouse), vice president of the American Institute of Electrical Engineers and representing the American Federation of Information Processing Societies.

An executive committee, appointed by Dr. Harder, is comprised of Isaac L. Auerbach (Auerbach Electronics Corp.), president of IFIP; Dr. Alston S. Householder (Oak Ridge National Laboratory); Dr. Walter F. Bauer (Thompson Ramo Wooldridge); Dr. D. L. Thomsen, Jr. (IBM), in charge of U. S. exhibits; Dr. Werner Buchholz (IBM), travel arrangements; and Gene Jacobs (System Development Corp.), publicity and communications.

Further information on the Congress may be obtained from Dr. Harder, Westinghouse Electric Corp., East Pittsburgh, Pa., any of the committee members, or the travel firm of Thos. Cook & Son, which has offices in principal cities. ■

DATAMATION'S QUARTERLY INDEX OF COMPUTING

Ops/Sec increases 31.5%; dollar rental up 19%

Based on information presently available to *Datamation*, estimates as shown below are offered as reasonable approximations derived for the most part, from the specifications of larger systems since their speeds and monthly rentals overwhelmingly dominate the Indexes.

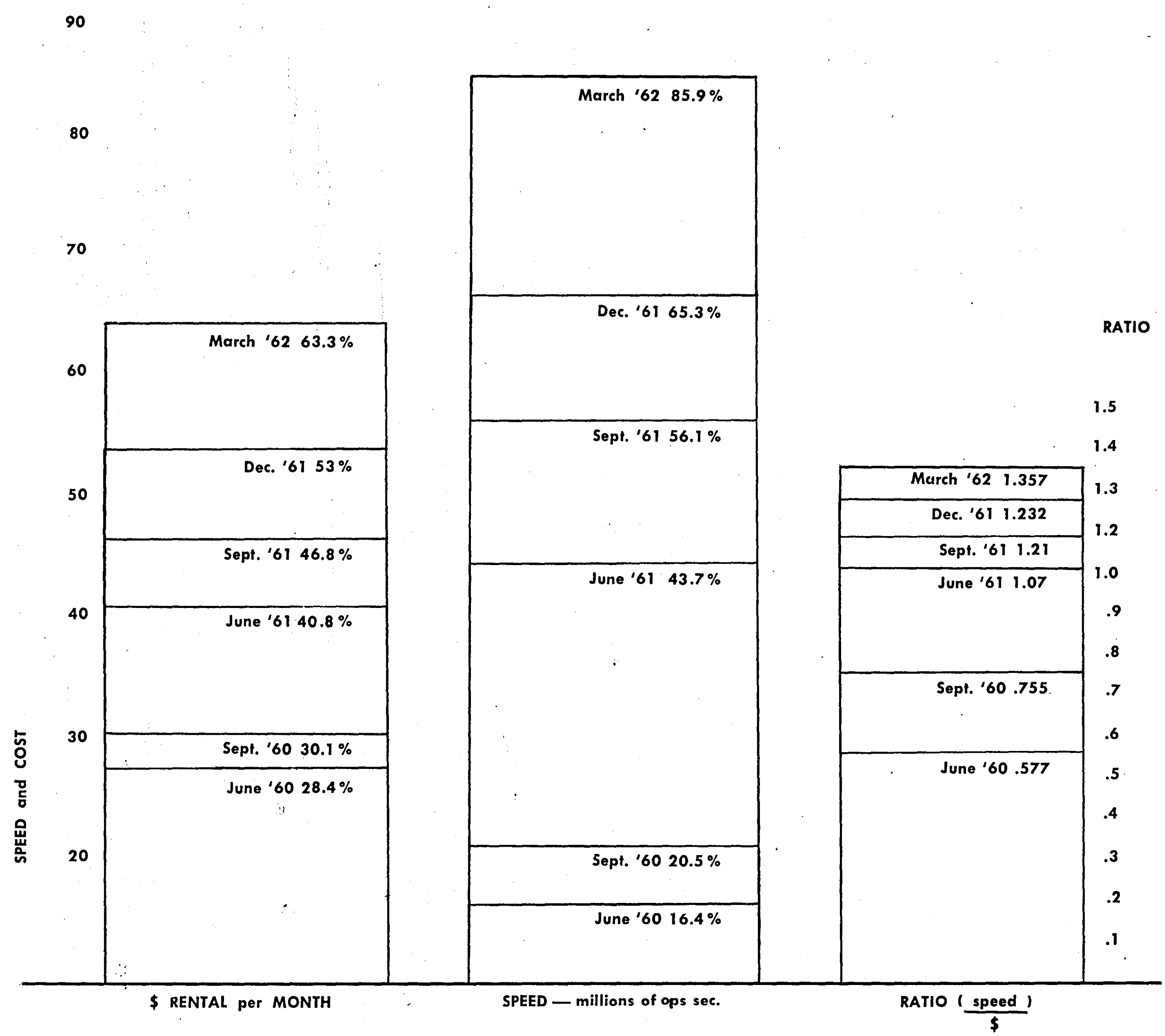
Speed (additions per second) and monthly rental figures are based on the Charles W. Adams' Computer Characteristics Quarterly, published in *Datamation*, December, 1961.

The ratio of computing power per dollar represents the quotient of the Speed Index and Operations per Dollar Index. Since the Ratio Index represents an indicator or measure of a condition, the units (operations per second) ÷ (dollars per month) need not be meaningfully related to provide an intelligible result.

A healthy increase in the number of ops/sec during the first quarter of 1962 is evidenced in the latest Quarterly Index of Computing. Rising from 65.3 million ops/sec as reported in December, 1961, updated figures show an increase of 31.53% to 85.9 million ops/sec, the highest increase, percentage-wise, since June, 1961.

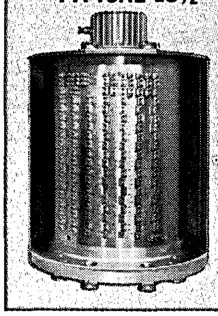
This upward trend can be traced largely to the continuing installation of 1604s, 7070s, 7090s, 1620s and 1401s. The latter is now located in some 2,100 sites while the 1620 is a shade below the 1K installation figure.

On the cost side, dollar rental per month is up 19.4 per cent, to over 63 megabucks. In December, the rental figure stood at 53 megabucks, while the speed to dollar ratio at that time was 1.232. The first quarter's ratio is 1.357, up by 10.14 per cent. ■



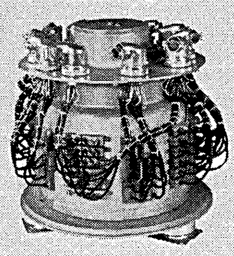
HERE'S PROOF YOU STILL CAN'T BEAT A BRYANT DRUM

TYPICAL 18½" DRUM APPLICATIONS

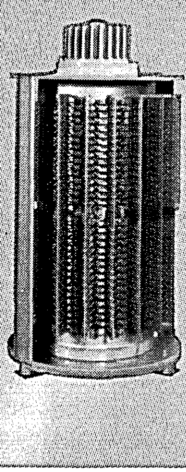


Teleregister Corporation
Airlines Reservation System
Banking Systems
Melpar, Incorporated
Military System

TYPICAL 7½" DRUM APPLICATIONS



Bailey Meter Company
Bailey 700 Systems
General Precision, Inc.
RPC 4000 Computer

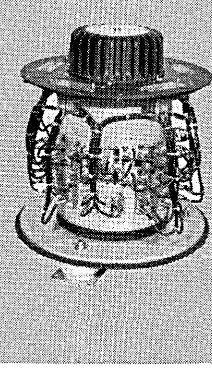


TYPICAL 10" DRUM APPLICATIONS

Rabinow Engineering Company, Inc.
Post Office Sorter
Consolidated Avionics Corporation
Security System

No other manufacturer offers you Bryant's proven experience in the design and production of magnetic data storage drums. Since 1953, Bryant has produced more than 1,500 memory drums for over 100 customers . . . a few of which are shown here. Included are drums for commercial data processing computers . . . for industrial process control systems . . . for rugged airborne and military applications. Some represent drums only, others are complete data storage systems. Some have fixed heads, some flying. In sum, they are your assurance that you still can't beat a Bryant drum.

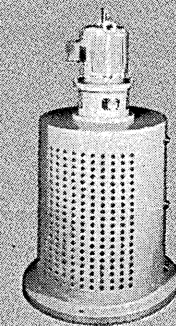
For additional proof, see your Bryant Representative, or write direct to: 850 Ladd Road, Walled Lake, Michigan, MArket 4-4571.



TYPICAL 5" DRUM APPLICATIONS

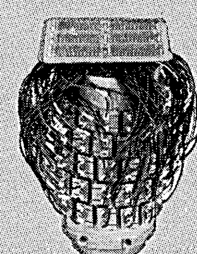
The Martin Company
BIRDiE Computer
Sandia Corporation
Check-out System

TYPICAL CUSTOM UNIT APPLICATIONS



Philco Corporation
20" Drum (Philco 2000 Electronic Data Processing Systems)
Radio Corporation of America
18,000 RPM Disc

TYPICAL 3" DRUM APPLICATIONS



ITT Kellogg
Telephone Switching System
Burroughs Corporation
Airborne Computer

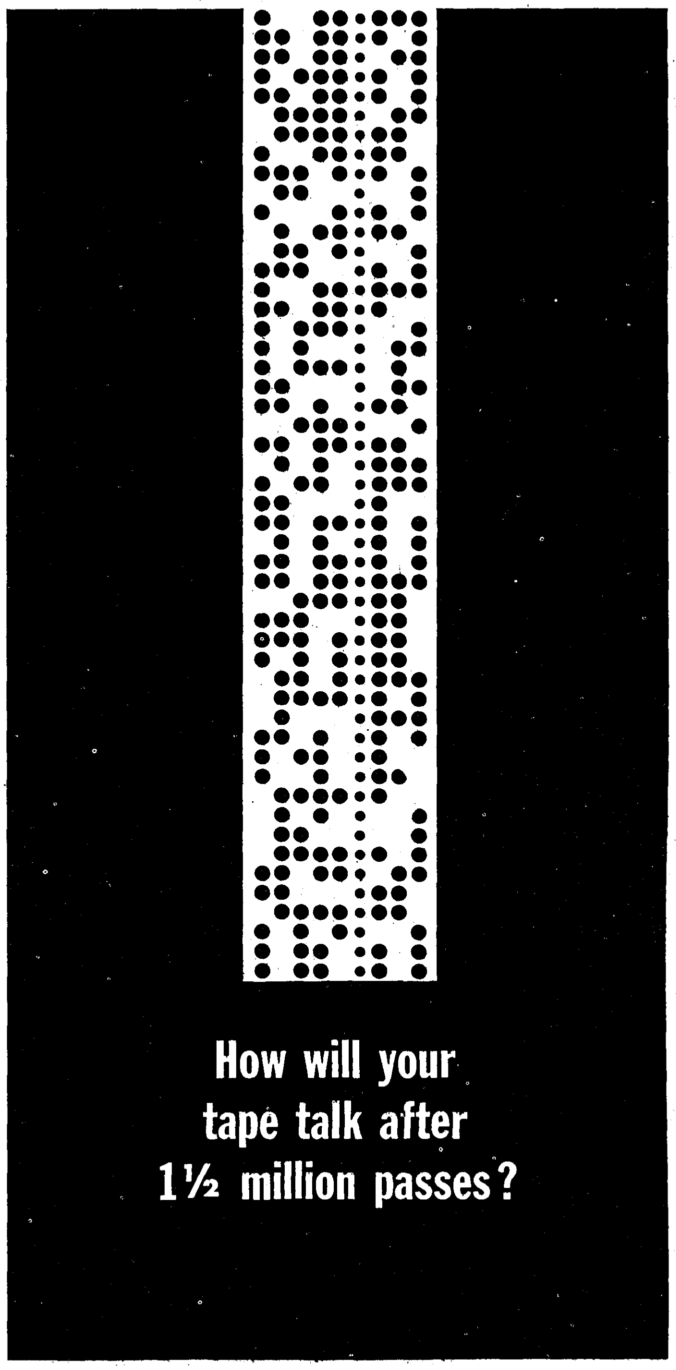
62-43 CP

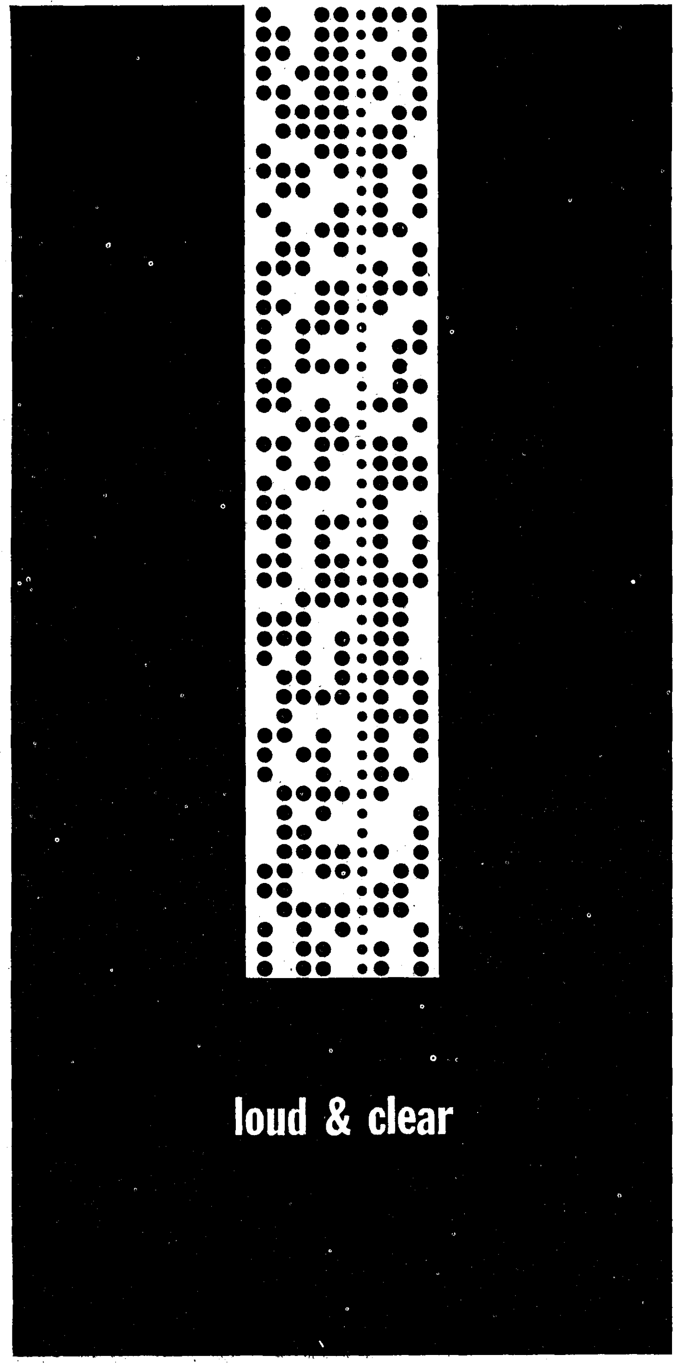
BRYANT

COMPUTER PRODUCTS

Disc File and Magnetic Drum Memories for Every Storage Application

A DIVISION OF EX-CELL-O CORPORATION XLO





A Digitronics' customer asked for a photo-electric tape reader that would read a piece of looped, perforated paper tape at least 1½ million times without any change in signal output because of tape deterioration. Digitronics filled the order —and guaranteed performance.

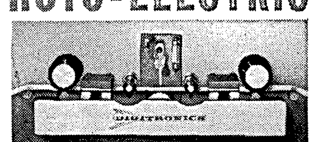
Tape on a Digitronics photo-electric reader is handled just that gently and smoothly.

But that's only part of the story... self-adjusting brakes allow you to interchange tapes without resetting clearances; the reader stops, reliably, before the character following the "stop character" at 1000 cps; the photo diodes are self-cleaning because they poke up above the reading head, and the circuitry is all solid state.

To meet any of your perforated tape reading requirements, Digitronics photo-electric units are designed on the modular principle. These readers are capable of accommodating 5 to 8 level tape interchangeably at 60 to 5000 cps. Tape handlers are also available for 5 to 8 level tape up to 1000 cps.

For more information write Digitronics Corporation, Albertson, New York.

DIGITRONICS PHOTO-ELECTRIC TAPE READERS



Where every bit counts

See these readers in Booths 401, 402, 403 at the 1962 Spring Joint Computer Conference, San Francisco.

CIRCLE 24 ON READER CARD

SPRING *JOINT* COMPUTER CONFERENCE

reflections on a revolution

a conference welcome

by GEORGE A. BARNARD

General Chairman, Spring Joint Computer Conference

That February morning when the world watched and listened to the progress of Friendship 7 and its gallant passenger, there must have been a surge of pride within every professional man active in computer technology. We learned that the Mercury Control Center was being supplied from Greenbelt, Maryland with a constant flow of data – every 1½ seconds – predicting where the space capsule might land if the flight were to be terminated at any given moment. Here was a dramatic application of computers to what President Kennedy has termed "The New Ocean."

Accustomed to the role of computers in banking, automated industries, chemical and petroleum processing, insurance and department store billings and other behind-the-scenes operations affecting our daily lives, the public now understands that the computer is indispensable to man's conquest of space.

We of the computer industry are swept up in the mainstream of world events and cannot rest on our achievements, no matter how solid they may seem. Facing forward to new challenges, we must continue to explore and discover anew. Computer conferences such as we have been privileged to organize for San Francisco in May offer us the best opportunity to assess the individual and collective effort.

Since our computer conferences started some ten years ago, we have seen the evolution–or *re*volution–of the transistor from an embryonic laboratory development to the preferred, active computer component. Now the cryotron seems to be going through a similar process. And thin-films are intruding their techniques into both. We even hear rumors that someone is "growing" memories in organic "soups."

Computers can perform more work today than ever before. But, as they become faster and more efficient, as their logic takes on more complex tasks, paradoxically they are diminishing in size. And they are due to get even smaller. Packaging techniques and structural design are beginning to catch up with the phenomenal progress in logic and programming.

Recently-spawned microelectronics are coming into their own, and a fusion of production engineering with basic elements studies is already affording glimpses of "brain"-size machines. At the moment, space exploration is foremost in this research, but commercial interests are beginning to look at its potential, aware that today's visions formulate tomorrow's products. The electronic desk calculator we breadboarded yesterday we use today!

"Magic Brain!" Remember the smiles that catch phrase provoked a decade ago? "Machines will never be able to think!" it was said. But some "thinking" has been going on. Those who once scoffed are now planning schemes for "intelligent" machines; they have been simulating neuron circuits and then trying them out as active decision networks. Memories can now be addressed by content rather than by location, even by association with other contents. Machines are being built to function efficiently and taught to accommodate themselves to the vagaries and limitations of their human masters.

We are being asked to cooperate with our products! We still have to teach them all they know, but they need to be told only once and they seldom forget. It is increasingly difficult to deny that some of our computers can perform in ways which the dictionary calls "thinking" or can exhibit characteristics termed "intelligent."

Some cases seem exotic, while others are becoming commonplace. The complex systems which control space exploration make valid the wildest schemes of science-fiction. We think nothing of trusting computers to account for our bank deposits; we believe the computers of insurance companies which tell us how long we may expect to live. And this month we cower under the authority of computers which watch how we report our income taxes!

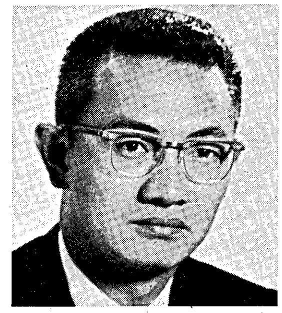
We must continue to reason together and to pool our knowledge. We have a responsibility and we have an opportunity. In San Francisco May 1-3 we hope to move things forward a bit and welcome all those who will share in this exciting prospect. ■

the program

an interdisciplinary theme

by RICHARD I. TANAKA

Technical Program Chairman, Spring Joint Computer Conference



highlights

Perhaps the predominant aspect of the program is the diversity of topics which are now pertinent to computer technology, ranging from papers which report on basic technological developments within the field, to applications in business system planning and to modeling of biological processes. Distinctive areas of specialized interest are difficult to define, and the computer field itself seems to be developing into an interdisciplinary topic, encompassing not only the physical sciences, but extending into fields such as sociology, medicine, psychology, etc. The Conference Program is not representative of all of these areas, of course, but does reflect much of the breadth of interest now appropriate.

Papers of the most probable general interest include:

"A simulation of a Business Firm," by Charles P. Bonini: This paper describes a comprehensive model for studying a business firm to help determine answers to the complex questions which relate to its internal operation. This is an example of the current attempts to apply technical principles to what is still largely an empirically determined field.

"MH-1, a Computer-Operated Mechanical Hand," by Heinrich A. Ernst: The work leading to the MH-1 device combines the topics of artificial intelligence and digital control. The device itself has receptors which are used to control its performance; the basic control, however, is affected by a computer program which is involved in the decision process and which is designed to function in the absence of explicit instructions. A movie illustrating operation of the mechanical hand will demonstrate the salient properties of the device.

"A Superconductive Associative Memory," by Paul M. Davies; "A Cryogenic Data Addressed Memory," by V. L. Newhouse and R. E. Fruin; "Circuits for the FX-1 Computer," by Kenneth H. Konkle: The three describe potential applications for cryogenic devices, with attempts made to use the unusual characteristics in ways which affect computer operation. The associative memory characteristics derive somewhat naturally from the attributes of present cryogenic elements; it seems natural, therefore, to propose such systems at this time.

"Are the Man and the Machine Relations?," by Burton H. Wolin: This paper describes work which attempts to define further the attributes of humans, in a complex environment, so that their relationship to computer systems can be better established. The entire Session on Man-Machine Cooperation, in fact, is concerned with the problem of specifying systems which use the machine and its operator in an optimum and agreeable way.

"Problems in the Study of the Nervous System," by Belmont G. Farley: This paper is intended as a general survey of the status of computer techniques in studying the nervous system. The topic is closely related to what is called artificial intelligence; the problems are complex, the approaches are varied, the results interesting.

"Neural Analogs," by Leon D. Harmon: Harmon's paper is more specialized in scope than Farley's, but nonetheless serves as a comparison and summary of two of the main approaches now used in studying the nervous system. The two approaches are: simulate, as faithfully as practical, known attributes of biological components, or, explore the resultant properties of networks of relatively simple devices which have some resemblance to neural nodels. The two approaches will be discussed, in general, with specific examples stemming from the first of the two approaches mentioned.

"Integration and Automatic Fault Location Techniques in Large Digital Data Systems," by Donald W. Liddell: This paper describes fault location techniques which use programming a computer to locate failure automatically. Successful results would lead to systems with minimal need for external monitoring, and would be a step toward fault-free, reliable long-term operation.

"The Storage and Retrieval of Physiological and Medical Data in a Modern Hospital," by Paul C. Tiffany: An information retrieval system which appears applicable to the needs of hospital operation and also the medical research worker is described.

selection

Each of the Joint Computer Conferences represents a major opportunity for discussing at one meeting, information generated within the full and sometimes diverse range of computer technology. It is important that the technical program present information, which, in some measure, is of pertinence to each segment of the computer community. In the early planning stages for the 1962 Spring Joint Computer Conference, it was decided that this objective would be met for this conference by organizing the technical program around a series of specialized sessions, each session to be as representative of its specialty as possible, both in subject material and in the detail presented. To do this, certain policies were adopted

Complete drafts of each submitted paper were required to be made available for evaluation. The advantages of having the full text are obvious, primarily in eliminating the too common occurrence where an excellent abstract or summary was followed by a paper which did not, in some sense, fulfill the promise of the preliminary information. At the same time, the availability of the whole paper imposed additional burdens on the Review Committee, both for the additional time required to perform reviews, and also for the obligation to return, in kind, the authors' cooperation in preparing a complete paper prior to acceptance.

A representative and widely situated review committee was solicited. The assistance and cooperation of several of the computer journal editors was of material assistance. Attempts were made to have some diversity in geographical distribution, to prevent any regional bias (if such a thing exists). Each man on the Review Committee was selected for his contribution to the field or for the excellence of his reviews in connection with the various computer publications.

The Session Chairmen were appointed very early in the formulation of the program, and in fact, have played a major role in the selection of the papers and in the organization of this part of the Conference. A tentative list of appropriate topic areas was used in selecting the Session Chairmen; however, wide latitude was given for modifying the Session topics, as influenced by the availability of papers and participants. The early appointment of Session Chairmen proved to be highly advantageous. It appears to be a wasteful neglect of ability and experience to limit a Session Chairman's function to that of conducting the mechanics of the presentation. Early involvement of the Session Chairman enables him to bear a significant part of the responsibility for maintaining quality standards. He was asked to utilize the review committee organized by the Program Committee; he was asked to solicit further reviewers to supplement the main review committee; he was asked to evaluate in detail the papers in his specialty, given to him after an initial screening process.

An additional function of the Session Chairman was that of soliciting invited papers. Papers were invited on the basis that they contain new material and results not represented in the submitted papers, that they be knowledgeable summaries of the field, or that they contribute, in some way, to the value of the session, perhaps by introducing an opposing or controversial point of view. Invited papers were subjected to the review process, just as were the submitted papers.

There was no pressure to present full-length sessions; indeed, a short session was encouraged in preference to a full length session which might have been padded by the inclusion of papers of lower quality. At least two of the sessions proposed were cancelled because the appropriate material was not available. The chairman for the sessions which were voluntarily cancelled deserve much credit for their role in organizing the Conference; their action indicated an acceptance of, and an adherence to, the philosophy of presenting quality material.

In the end, of course, the program belongs to the authors. The function of the Program Committee is to review, to select and to modify; it is the privilege and the responsibility of the authors to generate the information, and to present it properly.

We trust that most of the information presented is of immediate interest and will stimulate thought and discussion; we hope that some of it will form a lasting and valuable contribution to the computer community. ■

SPRING JOINT COMPUTER CONFERENCE featured speakers

DR. EDWARD TELLER, Professor of Physics at Large, University of California, will deliver the Keynote Address on Tuesday, May 1st, in the Gold Room, Fairmont Hotel, 10 a.m.

PROFESSOR ADRIIAN VAN WIJNGAARDEN, Mathematisch Centrum, Amsterdam, Netherlands, will address the SJCC Luncheon on Wednesday, May 2nd, in the Tonga Room, Fairmont Hotel, 12 noon.

SPRING JOINT COMPUTER CONFERENCE

conference particulars

Nearly 4,000 industry delegates are expected to attend the 1962 Spring Joint Computer Conference, to be held at the Fairmont Hotel in San Francisco, May 1-3. Sponsor of the conference is the American Federation of Information Processing Societies.

Thirty-seven **technical papers** will be presented during the three-day conference. All technical sessions will be held in the Fairmont Hotel except for sessions "G" and "K" which will take place in the Mark Hopkins Hotel (across the street from the Fairmont) on May 2 and 3, respectively. Among the topics to be covered will be "Computer Systems," "Circuits and Memory Devices," "Information Retrieval," "Programming and Coding," "Study of Business Systems," and "DDA and Hybrid Computation."

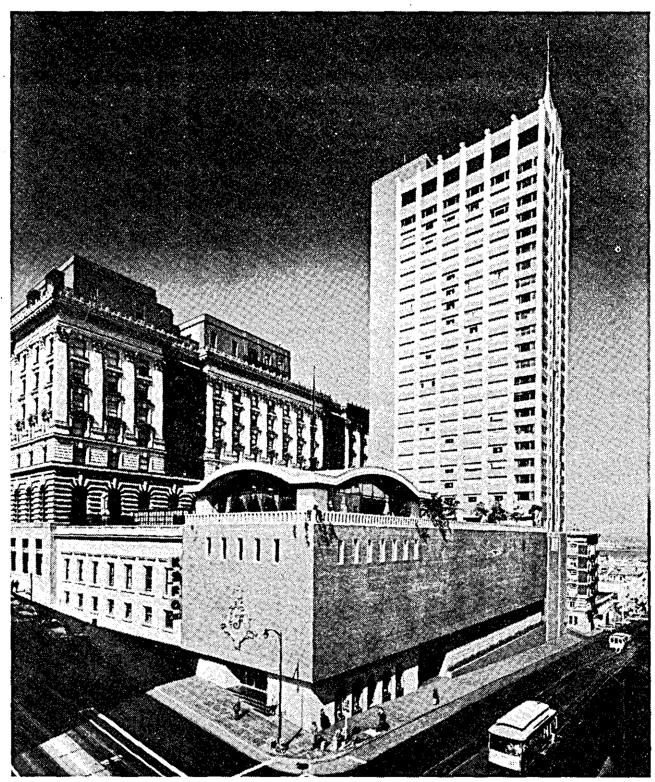
Dr. Edward Teller will deliver the **keynote address** on May 1 in the Gold Room of the Fairmont at 10 a.m. Principal speaker at the **conference luncheon** on May 2 will be Professor A. van Wijngaarden, Mathematisch Centrum, Amsterdam, Holland. The luncheon will be held in the Fairmont's Tonga Room at 12 noon.

The exhibit area will consist of the Grand Ballroom, Terrace Room, and Vanderbilt Room of the Fairmont. Sixty-six exhibitors—including eighteen full-frame manufacturers — will show their wares from 128 booths. Exhibit hours are from 12 noon to 6 p.m. on May 1 and 3, and 10 a.m. to 9 p.m. on May 2. A special exhibitors program will be held at the Mark Hopkins Hotel from 8 p.m. to 11 p.m on May 1 and 2.

For members of professional groups interested in data processing, a special educational program on dp will be presented concurrently with the SJCC.

Registration for the conference will be from 6 p.m. to 9 p.m. on April 30; 8:00 a.m. to 4 p.m. on May 1; 8:30 a.m. to 4 p.m. on May 2; and from 8:30 a. m. to noon on May 3. Registration desks will be in the main lobby of the Fairmont. Fees for the SJCC are: $6 for members of sponsoring societies (ACM, AIEE, IRE); $10 for non-members, and $2 for students.

Proceedings of the SJCC will be published in clothbound form, and will be available at no charge to registrants (members and non-members); students desiring copies may purchase them at the regular price of $4.



The Fairmont, conference hotel on Nob Hill. View from Powell and California streets showing the new Fairmont Tower and skylift to Crown Room.

Social events will be limited to the previously-mentioned conference luncheon and a cocktail party on May 1 in the Venetian Room of the Fairmont, from 6 p.m. to 8 p.m. Fee for the cocktail party is $4.50. No banquet is scheduled.

Field trips are not included in the SJCC program. ■

an educational bonus:

tutorials not for the erudite

As a departure from past conference programming, a special education series exploring some of the broad applications in computer technology is planned in conjunction with the Spring Joint Computer Confeernce.

A schedule of events to be held in the Mark Hopkins, opposite the Fairmont, is as follows:

On the opening morning of the conference (May 1), J. H. Herrett, president of Business Electronics, Inc. of San Francisco and an instructor in the Sloan Fellowship Program at Stanford University, will conduct an hour's session on "Computer Orientation."

Following will be an "IBM Computercade," featuring a demonstration of "The World's Slowest Computer" — illustrating storage, data transfers and programming via a special display system linked to an IBM 604-521.

Completing the first morning's events will be a review of systems design, programming aids and Electronic Data Processing terms by Dr. Ned Chapin of San Francisco State College.

for auditors and accountants

An afternoon session opening day has been designed to appeal to auditors and accountants and is being coordinated by Bryce Ells of IBM, San Jose.

John Scott, partner in Peat, Marwick, Mitchell & Co., San Francisco, will make the initial presentation comparing a computer audit with standard auditing procedures. He will emphasize the correlation between classic auditing techniques and those required for EDP systems.

"A Case Study of a Computer Audit" will be given by William R. Margerm, manager of Management Advisory Services of Price Waterhouse Co., San Francisco.

C. E. Hemphill, partner in Arthur Anderson & Co., San Francisco, will discuss two types of controls of a computer operation — those built into the machine as a part of the hardware and those established as operating company controls.

applications of computers to systems

Special education features for the second afternoon (May 2) will deal with applications of computers to systems and will be led by William Gerkin and Earl Means of Remington Rand, San Francisco.

Dr. George Evans, manager of the Mathematical Sciences Department, of Stanford Research Institute, will discuss simulation of accounting management as performed by computing machines. A second presentation will be made on data communications from remote terminal to control computer.

Concluding this afternoon program will be a panel discussion on "Rental versus Buying," "Centralized versus Decentralized Data Processing Installations" and questions raised from the audience.

Appearing on the panel will be William Mitchell, manager of Data Processing at McClellan Air Force Base, Sacramento; Don Jackson, manager of Scientific Engineering for Aerojet at Sacramento; Charles Clayton, data processing manager for Chrysler Motor Parts, San Francisco; and Vincent LaCoste, data processing manager at Hewlett-Packard Co., Palo Alto.

'Information Retrieval' for final day

The concluding session of the special education program will take place Thursday afternoon, May 3, with Adolph Bodine of IBM, San Jose, as coordinator for a series of talks on information retrieval. Dr. I. A. Warheit of IBM, San Jose, will be session chairman.

Robert S. Meyer of Lawrence Radiation Laboratory, Livermore, Calif., will give an introduction to indexing and retrieval. F. G. Stockton of Shell Development Co., San Jose, will speak on "Search for Legal and Patent Data."

Additional presentations on information retrieval systems for management reports and a library cataloguing system to be developed into an information retrieval system are being planned.

the planners '62 SJCC committee

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Exhibits Management, J. L. Whitlock Associates, Oakton, Va.

Public Relations, W. C. Estler, Palo Alto, Calif.

SPRING for the distaff side

MARGARET CONLEY
Chairman, Ladies Program

Over 200 women who are expected to be in San Francisco while their menfolk are engaged at the 1962 SJCC can expect a round of pleasant diversions arranged by the distaff side of the conference planners.

Opening day—Tuesday, May 1—will find the morning hours centered about the Fountain Room of the Fairmont, the conference hotel, where the ladies will register and sip coffee.

In the afternoon there will be a Computercade, a special demonstration of computer logic tailored for the uninitiated, in the Room of the Dons at the Mark Hopkins Hotel across from the Fairmont on Nob Hill.

In the evening the ladies will join their escorts for the conference cocktail party in the Fairmont's Venetian Room.

Wednesday morning there will be a tour (limited to 50) of Jackson Square, San Francisco's outstanding decorating center. Privileged visits to several of the nationally known establishments have been arranged.

Luncheon at Yamato Sukiyaki House at the base of Nob Hill will follow. In the midafternoon there will be a sightseeing cruise of San Francisco Bay aboard a chartered vessel.

Thursday — the final day of the conference — motor coaches will depart the Fairmont at 10 a.m. for Saratoga, via the scenic Skyline Drive. At Saratoga the ladies will visit the mountain winery of Paul Masson Vineyards for a wine-tasting and al fresco luncheon on a dining balcony overlooking the Santa Clara Valley.

Leaving the hilltop, the touring party will go next to Paul Masson's Champagne Cellars in the valley for a demonstration of the art of champagne-making.

Enroute back to San Francisco the motorcade will stop for an hour at Sunset Magazine in Menlo Park to inspect the regional gardens, test kitchens and architectural attractions of "the West's Own Magazine." ■

Above: The gardens of Sunset Magazine, scene of ladies' field trip.

the sponsor: AFIPS

American Federation of Information Processing Societies

AFIPS was created on May 10, 1961, to better organize the advancement and dissemination of information about the processing sciences at all levels and to all media. AFIPS is a direct outgrowth of the National Joint Computer Committee (NJCC) which was established for the sole purpose of sponsoring and coordinating conferences. The founding and participating societies of AFIPS are: The American Institute of Electrical Engineers; The Association for Computing Machinery; The Institute of Radio Engineers. Also cooperating is the Simulation Councils Inc., representing analog computer activities. This and future computer conferences sponsored by AFIPS will be held twice yearly as Spring and Fall events.

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Dr. W. Buchholz, IBM Corporation
Dr. A. A. Cohen, Remington Rand Univac
F. E. Heart, Lincoln Laboratory
H T. Larson, Ford Motor Co.

JOINT COMPUTER CONFERENCE

the exhibitors

To augment the booth displays, exhibitors will participate in a separate forum to provide additional information about their equipment and services. Each exhibitor will be allotted time from 8 p.m.-11 p.m. Tuesday and Wednesday, May 1 and 2. A schedule of the Special Exhibitor's Program will appear in the final conference program available at the registration desk.

Aeronutronic 512-513
Division of Ford Motor Company
Newport Beach, California

AMP, Inc. 217-219,
Harrisburg, Pennsylvania 317-319

Ampex Corporation 505-508
Redwood City, California

ANelex Corporation 204-205
Boston, Massachusetts

Applied Dynamics, Inc. 702
Ann Arbor, Michigan

Bell Telephone System 107-109
Pacific Telephone Company &
Long Lines Department
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The Bendix Corporation 501-504
Bendix Computer Division
Los Angeles 45, California

Berkeley Division of
Beckman Instruments 308
Richmond, California

Brush Instruments 802
Division of Clevite Corporation
Cleveland 14, Ohio

Bryant Computer Products 105-106
Walled Lake, Michigan

The Bureau of National Affairs, Inc.. 304
Washington 7, D.C.

Burroughs Corporation 703-706
Detroit, Michigan

California Computer
Products, Inc. 417-418
Downey, California

C-E-I-R, Inc. 823-824
New York 17, New York

Collins Radio Company 815-818
Dallas, Texas

Comcor, Inc. 514
Denver, Colorado

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Computer Control Company, Inc. 410-411
Los Angeles 64, California

Computer Systems, Inc. 609-610
Monmouth Junction, New Jersey

Consolidated Electrodynamics Corporation 820
Pasadena, California

Control Data Corporation 201-203
Minneapolis 15, Minnesota

Data Display, Inc. 412-413
St. Paul 8, Minnesota

Datamation 305
New York, New York

Datapulse, Inc. 415
Inglewood, California

DI/AN Controls, Inc. 611
Dorchester 25, Massachusetts

Digital Equipment Corporation . 211-214
Maynard, Massachusetts

Digitronics Corporation 401-403
New York, New York

DYMEC 903
Division of Hewlett-Packard Company
Palo Alto, California

Electro Instruments, Inc. 515
Sunnyvale, California

Electronic Associates, Inc. 404-405
Long Branch, New Jersey

Electronic Engineering Company of California 315
Santa Ana, California

Electronic Memories, Inc. 701
Los Angeles, California

Engineered Electronics Company 313-314
Santa Ana, California

Epsco, Inc. 215-216
Cambridge, Massachusetts

Fabri-Tek, Inc. 416
Amery, Wisconsin

Fairchild Semiconductor 406-407
Mountain View, California

Ferranti Electric, Inc. 509
Plainview, L.I., N.Y.

Friden, Inc. 102-104
San Leandro, California

General Dynamics/Electronics . . 112-114
Information Technology Division
San Diego, California

General Electric Company 808-811
Computer Department
Phoenix, Arizona

The Hallicrafters Company 902
Berwyn, Illinois

Indiana General Corporation . . 110-111
General Ceramics Division
Keasbey, New Jersey

International Business Machines Corporation 601-605
New York, New York

International Telephone and Telegraph Corporation 803-804
New York, New York

Invac Corporation 517
Natick, Massachusetts

Kearfott Division, General Precision, Inc. 316
Little Falls, New Jersey

Laboratory for Electronics, Inc. . . 208-209
Boston, Massachusetts

Litton Systems, Inc. 812-813
Beverly Hills, California

McGraw-Hill Book Company, Inc. 518
Corte Madera, California

Memorex Corporation 801
Santa Clara, California

Midwestern Instruments, Inc. 807
Tulsa, Oklahoma

Moxon Electronics Corporation 516
Beverly Hills, California

The National Cash Register Company . . . 206-207, 306-307
Dayton, Ohio

Omnitronics, Inc. 819
Philadelphia, Pennsylvania

Packard Bell Computer Corporation 612-615
Los Angeles, California

Philco Corporation 606-608
Computer Division
Philadelphia, Pennsylvania

Photocircuits Corporation 814
Glen Cove, New York

Potter Instrument Co., Inc. 511
Plainview, L.I., N.Y.

Raytheon Company 821-822
Waltham, Massachusetts

Radio Corporation of America. 825-826
Semiconductor and Materials Division
Somerville, New Jersey

Remington Rand UNIVAC 301-303
New York, New York . . . .

Rese Engineering, Inc. 510
Philadelphia, Pa.

Rheem Electronics 210
Division of Rheem Manufacturing Company
Los Angeles, California

Rotron Manufacturing Company, Inc. 901
Woodstock, New York

Royal McBee Corporation 805-806
New York, New York

Scientific Data Systems, Inc. . . 309-310
Santa Monica, California

The Service Bureau Corporation . . . 414
New York, New York

Soroban Engineering, Inc. 408-409
Melbourne, Florida

Tally Register Corporation 311-312
Seattle, Washington

Teletype Corporation 904-905
Skokie, Illinois

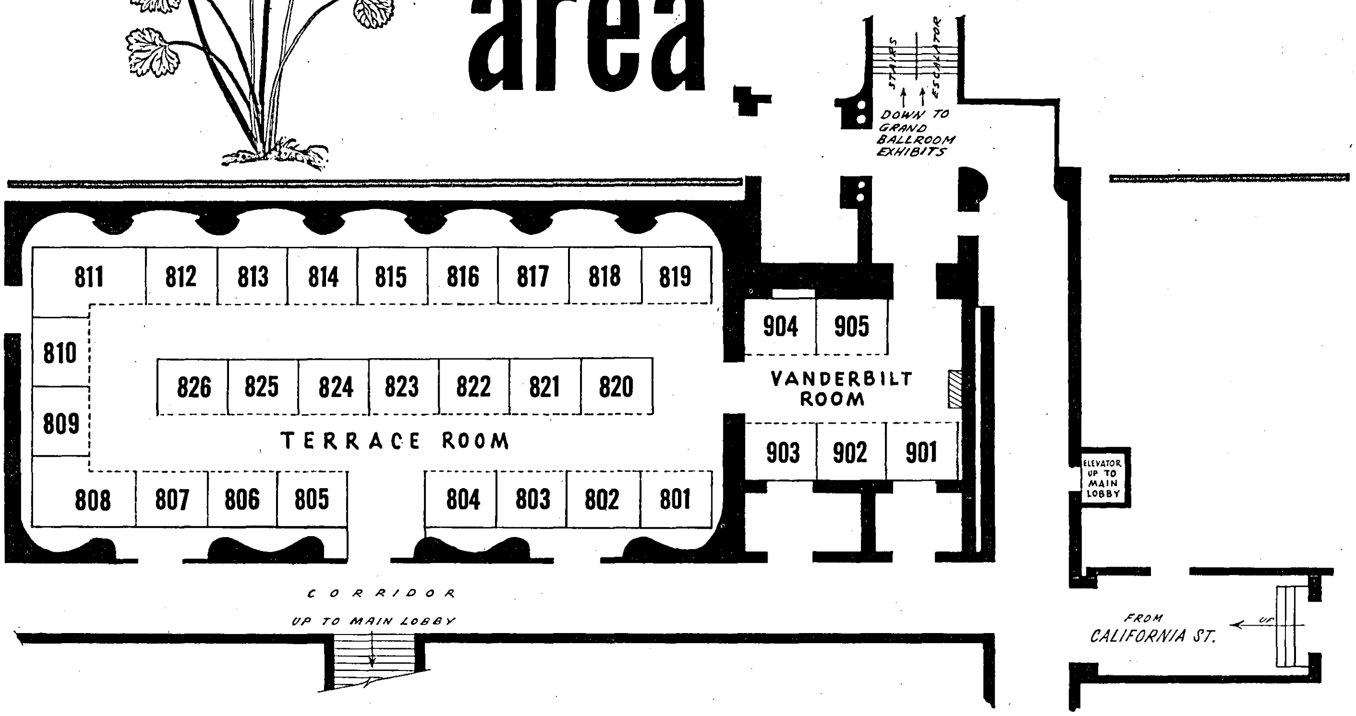
Telex, Inc. 616-618
Data Systems Division
St. Paul, Minnesota

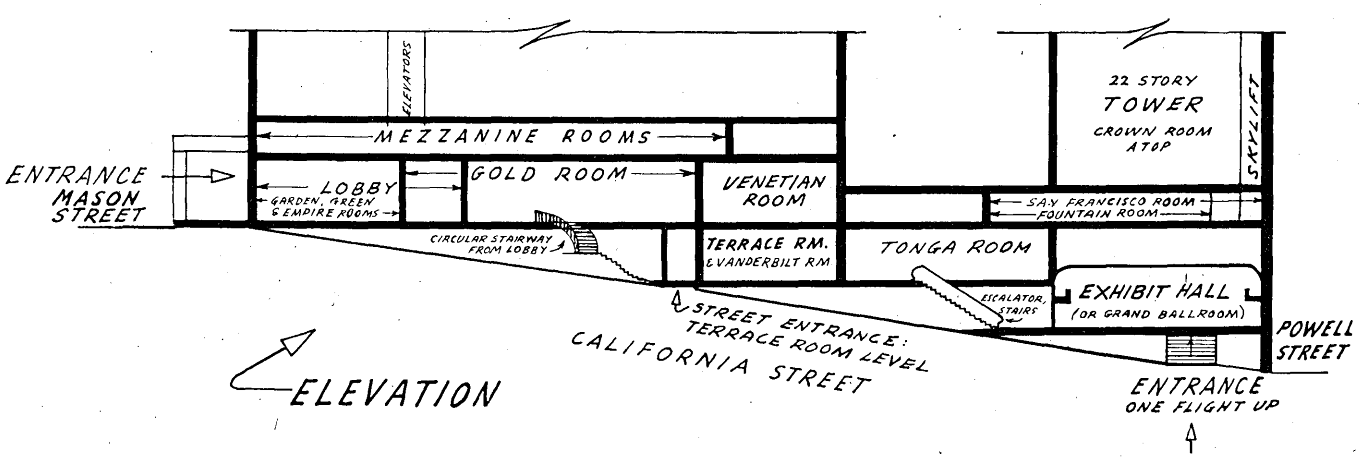
John Wiley & Sons, Inc. 101
New York, New York

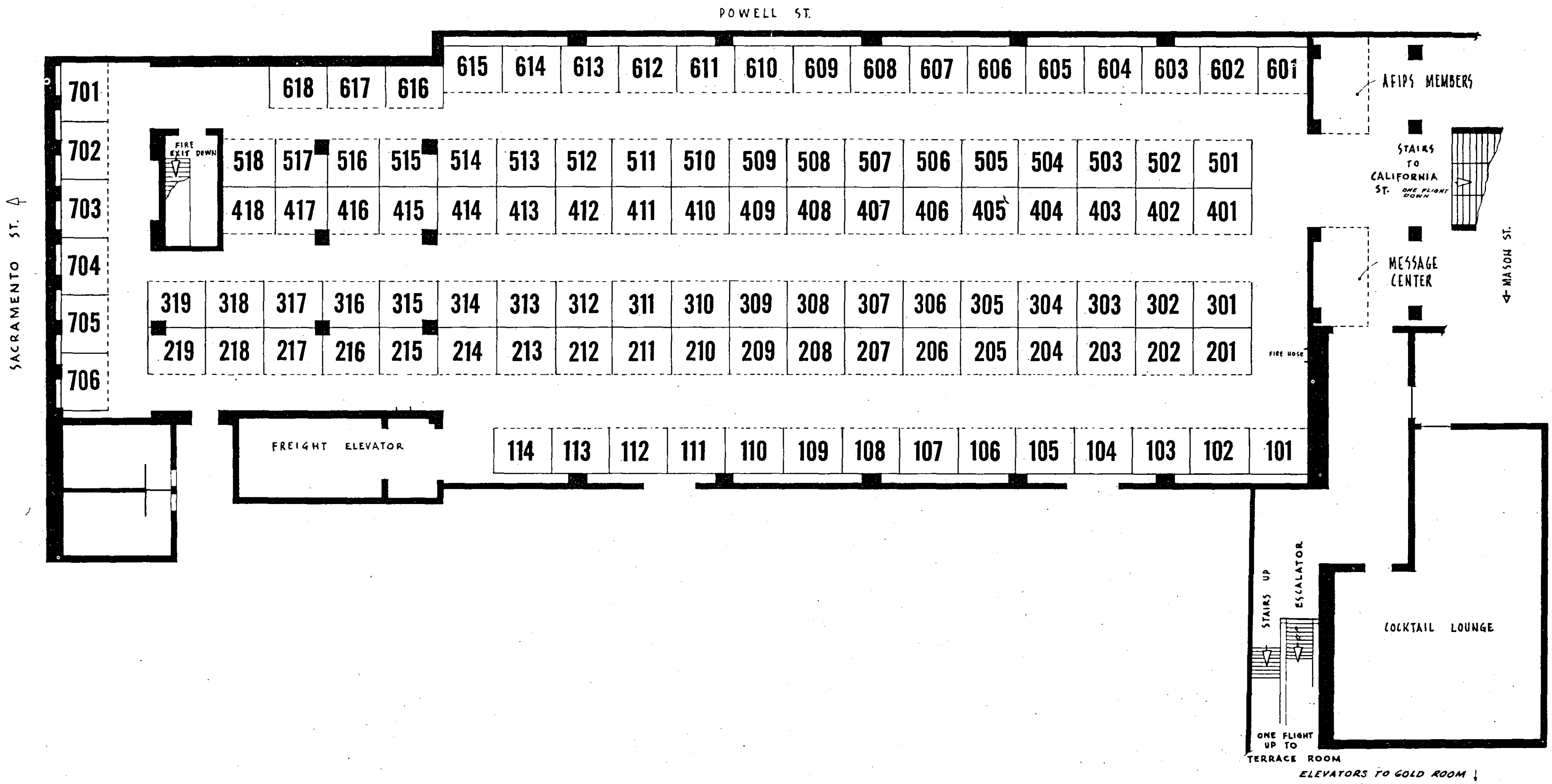
(See Exhibit Map on pages 64-65)

SPRING JOINT COMPUTER CONFERENCE

the exhibit area



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MASON ST.
AFIPS MEMBERS
STAIRS TO CALIFORNIA ST. ONE FLIGHT DOWN
MESSAGE CENTER
FIRE HOSE
FIRE EXIT DOWN
FREIGHT ELEVATOR
STAIRS UP
ESCALATOR
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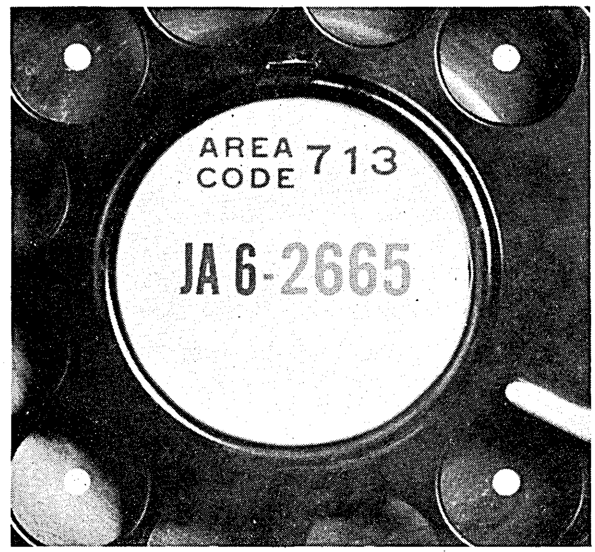
BOSTON: IBM 7090/1401/1401



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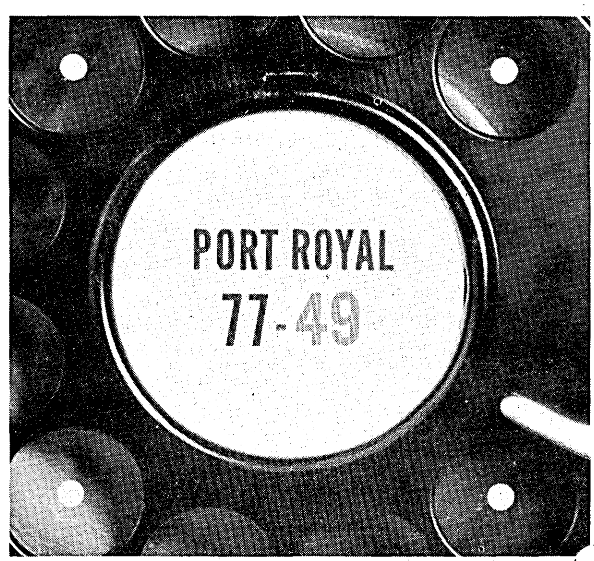
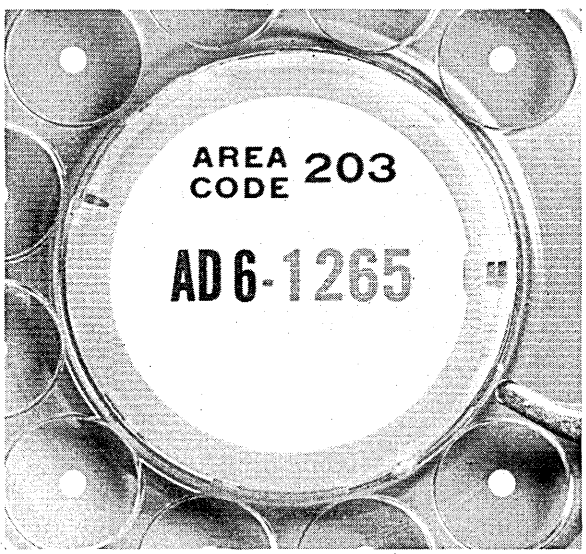


PARIS: IBM 7090*/1401*/1620*

Linear Programming/Operations Research/Market Research/Electronic Data Processing/Computer Programming/Syste

NEW YORK: IBM 7090*/1401/1401

LOS ANGELES: CDC 1604/IBM 7090/1401/704*



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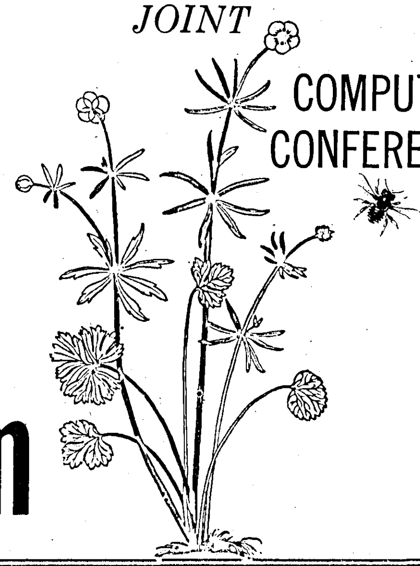
CIRCLE 30 ON READER CARD

SPRING JOINT COMPUTER CONFERENCE

the technical program



OPENING SESSION

Tuesday, May 1

Gold Room—10 a.m. to 12 noon.
Note: Addresses will be relayed via public address system to the Venetian Room in the event of an over-capacity audience.

Introduction:
Dr. Richard I. Tanaka,
Lockheed Missiles and Space Co.
Program Chairman of 1962 SJCC.

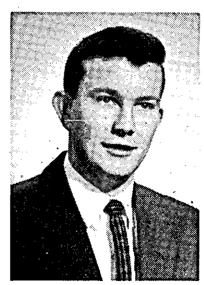
Opening Remarks:
George A. Barnard,
Philco Western Development Laboratories.
General Chairman of 1962 SJCC.
Dr. Willis H. Ware,
Rand Corporation.
Chairman of AFIPS Governing Board.

Keynote Address:
Dr. Edward Teller,
Professor of Physics at Large,
University of California, Berkeley, California.

Tuesday, May 1, 2 p.m. to 5 p.m., Venetian Room

SESSION A

Study of Business Information Systems



Chairman:
FRED M. TONGE
Stanford University

Panelists:
C. B. McGuire, University of California, Berkeley
Richard L. Van Horn, The Rand Corporation, Santa Monica, Calif.

Organizations have always had information systems. The computer has focussed increasing attention on these systems by magnifying both their potential benefits and their directly attributable costs. Since the problems of constructing, using and improving these systems are largely ill-structured, optimizing techniques that have served in other areas cannot be transferred intact. There is much to learn about how to effect such systems and about how they affect the organization.

Within the framework of the study of business information systems we propose the following areas for specific discussion, to relate the formal papers and to explore their implications.

1) What useful formal descriptions exist of business information systems, and what techniques are available for manipulating and extracting consequences from such formal descriptions? 2) What specific studies have been made of these systems, and what are their implications? 3) Of what relevance are disciplines such as information theory, theory of teams, feedback control systems theory? 4) What will be the impact of hardware and programming developments in such areas

as display systems, pseudo-English input, etc? 5) What is the appropriate division of research between industry and the university? 6) How can we best profit from the ongoing diverse systems activities in industry?

Toward a General Simulation Capability

Michael R. Lackner
System Development Corporation, Santa Monica, Calif.

Simulation of a system by digital computer require:

a model of the system which is intelligible to the student of the system while compatible with the limitations of the computer, translation of the model to computer code, movement of the model through time, recording the performance of the model.

SIMPAC, a "simulation package," incorporates coherent techniques and devices for the accomplishment of these objectives: modeling concepts for building a computer-compatible model, a vocabulary for encoding the model, a computer program for moving the model through time and recording its performance, and an output presentation program.

A model of a hypothetical business system has been implemented with the first version of SIMPAC for the purpose of studying management controls in a complex system.

This paper discusses digital simulation and SIMPAC, and introduces modeling concepts which may lead to a set of simulation systems which would assemble models of varying complexity from descriptive statements and analyze the models prior to simulation.

A Non-Linear Digital Optimizing Program for Process Control

Raymond A. Mugele
IBM Corporation, San Jose, Calif.

A new program has been developed for optimizing a computer-controlled process. This program applies probing and restraint-following algorithms which permit solving the optimization problem in difficult cases. These cases include non-linear or discontinuous restraint functions, and non-convex domains.

The program requires relatively little storage for program and data, and no special modifications of objective or restraint functions. It is primarily applicable to some medium-sized digital computers now used in process control.

Various control strategies are compatible with this program. It can be used to generate an operator guide for a process operating in the steady state. It can also be used for optimizing the control of a process with perturbed inputs, *i.e.*, in the transient state. It can also be interrupted, before completion, in order to determine the degree of improvement available, or to impose new restraints.

A Simulation of a Business Firm

Charles P. Bonini
Graduate School of Business, Stanford University

This paper describes a simulation model of a hypothetical business firm. The model was constructed to include not only the accounting and economic factors of costs, profits, sales, units produced, etc., but also psychological and behavioral concepts. Individuals in the firm have aspiration levels, feel pressure, and react in accordance with behavioral theory.

The purpose of the model is to study the effects of informational and organization factors upon the decisions of a business firm. We have had limited knowledge of such variables as: the effects of tardy information, the effects of different distributions of information within the firm, the effects of differing degrees of centralization or decentralization, etc. A comprehensive model, such as the one proposed, is nec-

essary to answer such questions.

Eight specific hypotheses involving changes in the organization and information system of the firm were formulated and tested using a factorial experimental design. The results of this experiment demonstrate the usefulness of this model as a research tool.

Tuesday, May 1, 2 p.m. to 5 p.m., Gold Room

SESSION B

Theoretical Problems in Artificial Intelligence

Chairman:
RUSSELL A. KIRSCH
National Bureau of Standards
Washington, D.C.

Panelists:

Edward A. Feigenbaum, University of California, Berkeley, and Rand Corporation, Santa Monica, California

Marvin L. Minsky, Computation Center, Massachusetts Institute of Technology, Cambridge, Massachusetts

Norman Z. Shapiro, National Institutes of Health, Bethesda, Md.

The three papers in this session represent contributions to artificial intelligence from diverse sources. Ernst draws upon techniques related to heuristic programming to solve a problem in tactile and visual sensing and control of a real environment. Reiss draws from classical associationist psychology to provide models for machines that would exhibit association of ideas. Cannonito draws from mathematical logic to study the nature of fundamental limitations on the behavior of intelligent machines.

The papers and the subsequent discussion will be directed more to the specialist in artificial intelligence than to the specialist in the source disciplines from which the contributions derive. To the computer specialist this session will be of interest because artificial intelligence research makes essential use of computers in non-trivial ways and because some of the by-products of such research (most notably the design of programming languages) contribute directly to the further development of computers.

MH-1, a Computer-Operated Mechanical Hand

Heinrich A. Ernst
IBM Research Laboratory, San Jose, Calif.

MH-1 is a motorized and sensitized servomanipulator operated by the TX-O computer at the Massachusetts Institute of Technology. Unlike in a conventional digital control system, the computer in the MH-1 system is not used to process quantitative information. Its function is rather to perceive and appreciate the environment of the hand qualitatively. On this basis, the computer determines a reasonable course of action after a goal has been specified for the hand.

Because of the automatic execution of these higher control functions, the system, by itself, in its attempt to reach that goal, behaves sensibly even in unexpected situations for which no explicit instructions have been given. For example, it makes reasonably successful attempts to resolve inconsistencies between the plan of action and the situation in the environment, it finds a way around obstacles hindering the hand, or it accepts help from a human assistant without fighting back, but it still resists unwanted interference. A film of MH-1 in action, demonstrating these properties, will be shown.

An Abstract Machine Based on Classical Association Psychology

Richard F. Reiss
Librascope Division, General Precision, Inc., Glendale, Calif.

Classical association psychology (circa 1750-1900) described, and proposed to explain, human thought processes in terms of a few kinds of forces operating on discrete entities called "sensations," "images," "ideas" etc. The classical theory was not given a precise, quantitative formulation and has been generally abandoned for a variety of reasons. However, the problem of developing artificial intelligence in digital machines provides new grounds for evaluating and perhaps extending association theory.

One method of evaluation is the synthesis by postulation of abstract "machines" which reflect the fundamental insights of association theory, and analyses of their behavior. In this paper a minimal machine is defined and certain aspects of its behavior are examined. It is restricted to a finite system of discrete objects coupled by two types of associative bonds, some of which are modified by passage of the objects through an "attention" register. The system grows in size by the admission of new objects via a "sensory" register. Although this "machine" constitutes an over-simplified interpretation of association theory, it does display some of the diverse behavioral potentialities of such systems.

The Godel Incompleteness Theorem and Intelligent Machines

Frank B. Cannonito
Grumman Aircraft Engineering Corp., Bethpage, N. Y.

This paper considers whether or not Godel's Incompleteness Theorem implies that machines are incapable of operating as intelligent robots. The paper's view is that the theorem does not limit machines in this sense. To support this belief, the concept of a recursively enumerable set of integers is developed via the intuitively appealing properties of programs made up from basic instructions similar to the well-known initial functions of primitive recursion. Productive sets of integers are then introduced and after some remarks relating formal languages to sets of integers via the Godel numbering technique, a formal axiomatic arithmetic language L is defined and the recursive enumerability of L's set of theorems is asserted. The notions of w-consistency and interpretation of L are then given and Godel's Incompleteness Theorem is stated and interpreted vis-a-vis digital computers.

The paper then attempts to modify the concept of a program so that the theorem of De Leeuw, Moorse, Shannon and Shapiro can be introduced to argue that nonrecursively enumberable sets of integers can be generated by the modified programs under suitable restrictions. This is regarded as removing the restrictions on the use of machines as creative robots, implied by the Godel Incompleteness Theorem.

Wednesday, May 2, 9 a.m. to 12 noon, Gold Room

SESSION C

Digital Storage and Circuits

Chairman:
JACK I. RAFFEL
Lincoln Laboratory
Massachusetts Institute of Technology
Lexington, Mass.

Panelists:

Kent D. Broadbent, American Systems, Inc., Inglewood, Calif.

Munro K. Haynes, Thomas J. Watson Research Center, IBM Corporation, Yorktown Heights, N.Y.

The session on digital storage and circuits will emphasize the continuing attempt on the part of components designers to perform more complicated functions faster and cheaper. Two of the papers are devoted to cryogenic associative memory work, the third to a technique for high-speed transistor logic. While they represent widely different ends of the component spectrum with respect to environment, switching speed, stage of development and familiarity, they, as well as all other developments, will be measured ultimately in common units of bits, dollars, and microseconds. It is hoped that this session will make some contribution to this difficult process of evaluation.

A Superconductive Associative Memory

Paul M. Davies
Abacus, Inc., Santa Monica, Calif.

The general properties of an associative memory are explained, and their advantages relative to a random access memory discussed. Then a superconductive mechanization of such a memory is described which is based upon the cross film cryotron. The memory requires 5 cryotrons per bit and 9 cryotrons for a control module associated with each word. Any combination of bits of the word can be used as the key, and any number of records in the memory can be identified and read out as the result of a single association. The speed of various circuitry is approximated and some applications are suggested.

A Cryogenic Data Addressed Memory

V. L. Newhouse
General Electric Research Laboratory, Schenectady, N.Y.
R. E. Fruin
General Electric Heavy Military Electronic Dept., Syracuse, N.Y.

A computer storage system which is addressed by content rather than location is described. The design has been verified by constructing and successfully operating a three-word module consisting of 81 crossed-film-cryotrons on a six-inch by three-inch substrate.

Circuits for the FX-1 Computer

Kenneth H. Konkle
Massachusetts Institute of Technology, Lexington, Mass.

A set of circuits capable of 50 megapulse operation is described. Included are gated and mixing pulse amplifiers, a static flip-flop, a diode logic unit with current-steering amplifier, a passive delay line, and an active variable delay circuit; all of which are designed to operate with terminated 75 ohm transmission lines. Ten nsec. pulses and 20 nsec. flip-flop transition times are provided through use of very-high-speed MADT transistors. The circuits have been successfully employed in the FX-1, a small general purpose computer with high-speed magnetic film memory.

Wednesday, May 2, 9 a.m. to 12 noon, Gold Room

SESSION D

Man-Machine Cooperation

Chairman:
DOUGLAS C. ENGELBART
Stanford Research Institute
Menlo Park, Calif.

Panelists:
Frederick P. Brooks, Jr., IBM Corporation, Poughkeepsie, N.Y.
Richard S. Hirsch, IBM Corporation, San Jose, Calif.
Herbert Martin Teager, Massachusetts Institute of Technology, Cambridge, Mass.

Bringing the human into on-line association with the computer, to interact in real time, is a trend motivated by several goals. Computerized systems, with real-time missions, often need to utilize some of the still-unique human capabilities, such as pattern recognition and judgment. Here the goal is to get best possible system performance, and the problem in the man-machine relationships is to try to couple the man in the best manner to this end. This goal has prompted most of the man-machine work to date.

Another goal, still to be generally appreciated and pursued, is that of extending the individual human's self-directed problem-solving capability by means of more intimate cooperation with the computer. This session is concerned, relative to both goals, with the current possibilities and problems of real-time, on-line, man-computer cooperation.

On-Line Communication Between Men and Computers

J. C. R. Licklider
Bolt Beranek and Newman, Inc., Cambridge, Mass.
Welden Clark
Bolt Beranek and Newman, Inc., Los Angeles, Calif.

The paper first reviews briefly the main problems and existing techniques of on-line communication between men and computers, and then describes three current developments:

1. A time-sharing system that permits several operators with independent problems to use one computer simultaneously, each operator having sensibly continuous access to its facilities.
2. A set of programs and techniques to facilitate planning and design of buildings.
3. Techniques that provide pictorial displays of what is going on inside the computer and reveal basic characteristics of traced-operating programs.

The paper concludes with a brief discussion of man-computer communication problems that call for basic advances in concept and hardware.

Solution of Non-Linear Integral Equations Using On-Line Computer Control

Glen J. Culler
Ramo-Wooldridge, a Division of Thompson-Ramo-Wooldrige, Canoga Park, Calif.
Robert W. Huff
University of California Radiation Laboratory, Berkeley, Calif.

This paper contains results from some computer experiments performed as part of a study concerning more effective utilization of computers as research tools for scientific problems. A display and analysis console permitting direct control of the computer was used to solve a non-linear integral equation occurring in the Bardeen-Cooper-Schrieffer theory of superconductivity. This equation gives the energy gap in a superconductor a function of energy after three physical parameters have been specified. In each case, the method of solution was constructed by the problem solver through direct interaction with the computer, the strategy of solution of each stage being based on information obtained from the computer in the course of the solution process. Thus, characteristic features of the problem and the pitfalls involved were discovered and controlled during the process of solution.

According to the parameter values specified, the problems ranged from very easy to quite difficult, and thus provided a basis for testing our approach. Extension of this technique to other digital equations, to more general one-dimensional problems, and to a wide class of physical and mathematical problems appears entirely feasible.

Are the Man and the Machine Relations?

Burton R. Wolin
Systems Development Corporation, Santa Monica, Calif.

As environments requiring control have become more complex, and the speeds of events in those environments have increased, there has been a trend to use computers to supplement or replace men or the functions they have traditionally performed.

The decision as to how to use computers in systems has been influenced by beliefs about what men can and cannot do or should and should not do.

Additionally, attempts to employ computers have frequently failed because not enough has been known, either about the function, or how to program the computer to perform the function.

A research program is described which has two objectives: First, to study the behavior of men in complex environments to find out *what* they can and cannot do well, and what factors limit or extend their effectiveness. Second, to study the behavior of men to determine *how* they perform complex functions, using the men as analogues of general-purpose computers, so that computers can be better programmed to perform such functions when it is necessary to do so.

A brief description of the computerized laboratory in which the research is being done, and how the laboratory is being used, is included.

Wednesday, May 2, 2 p.m. to 5 p.m., Venetian Room

SESSION E

Data Analysis and Model Construction in the Study of the Nervous System

Chairman:
BELMONT G. FARLEY
Lincoln Laboratory
Massachusetts Institute of Technology
Lexington, Mass.

Panelists:
T. H. Bullock, UCLA
M. H. Goldstein, Jr., Massachusetts Institute of Technology
Josiah Macy, Jr., Albert Einstein College of Medicine, New York City

The complexity and non-linearity of the problems encountered in the study of the nervous system make necessary the use of the most capable available tools for progress toward their solution. Problems arise both in processing experimental data, and in constructing theoretical models. The theme of this session is the application of advanced analog and digital techniques to analysis and synthesis of experimental phenomena observed in both animal and human nervous systems. Emphasis will be placed on problems and methods peculiar to the study of biological systems, but an attempt will be made to assess the present status of the field and relate it to others.

Problems In the Study of the Nervous System

Belmont G. Farley
Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, Mass.

A survey is given of the main experimental and theoretical difficulties encountered in the study of the nervous system. These difficulties are illustrated by specific examples of the uncertainties still existing in knowledge of the behavior of neurons, both individually and in groups, and in the interpretation of experimental observations. Concepts of the reduction of data from electrophysiological experiments are discussed and compared with those in physical experiments. Some theoretical problems are similarly treated. Examples of analog and digital computers having both special and general-purpose features which have been used to attack these problems are given, with a brief discussion of some of the results.

Neural Analogs

Leon D. Harmon
Bell Telephone Laboratories, Inc., Murray Hill, N. J.

Information processing in the nervous system is receiving increasing attention by researchers in the communications sciences. One of the most prolific areas of activity has been neural modeling. Simple electrical and mathematical models were described over a half a century ago; in recent years there has been a growing array of chemical, electronic, mathematical and computer-simulated analogs.

Two quite different kinds of neural modeling have resulted. In one category the intent is to simulate the complex parameters of the biological original closely in order to consider functions of the nervous system, hopefully to supplement neuro-physiological research. In the second kind of neural modeling the idea is to explore the single-element logical behavior or the self-organizing properties of ensembles of relatively simple quasi-neural elements.

It is the purpose of this paper to emphasize the differences between these two approaches, to review briefly some of the main streams of activity in neural modeling, and to show, by way of example, the results of one particular line of investigation — the work dealing with real-time electronic neural analogs.

The Caudal Photoreceptor of the Crayfish: A Quantitative Study of Responses to Intensity, Temporal and Wavelength Variables

William R. Uttal
IBM Research Center, Yorktown Heights, N. Y.

This paper describes the results of a study which has been made of the caudal photoreceptor of the crayfish. Pooled pulse potentials evoked by photic stimuli were recorded from the ventral nerve cord and these data digitized and recorded on magnetic tape. A digital computer was then used to analyze the data and recognize certain specific features. The coding of the nerve action potentials, as a function of the stimulus dimensions, was investigated and it was determined that the stimulus amplitude-response magnitude relation was a power function with the same exponent as that found in human perception. Furthermore, the spectral luminosity curve was determined to coincide with that of the human eye.

The similarities of these two functions suggest a common photochemical medium which thus allows a detailed study to be made of these human perceptual processes in a highly reduced model preparation.

A Theory and Simulation of Rhythmic Behavior Due to Reciprocal Inhibition in Small Nerve Nets

Richard F. Reiss
Librascope Division, General Precision, Inc., Glendale, Calif.

An elementary theory predicts that neurons which inhibit each other, and which suffer "fatigue" with repeated firing, can produce alternate bursts of pulses, a "multivibrator" effect, under certain conditions. Fragmentary physiological evidence suggests that reciprocal inhibition does occur in sensory and muscle control systems, and may in particular explain rhythmic behavior of the sort seen in alternating reflexes responsible for animal locomotion.

On the basis of a specific conceptual model of signal processing in neurons, analog and digital simulation models have been constructed and used to explore the multivibrator effect. The effect is rather easily produced with model neurons operating in either "coincidence" or "relaxation" modes, and is facilitated within limits by asymmetric parameters.

The reported simulation experiments are restricted to reciprocal inhibition of just two neurons and indicate that a neuron couplet, with a few sensory inputs and proprioceptive feedbacks, could provide an economical control system for alternating reflexes or for synergetic muscle groups which time-share a common load. Such a system could rapidly adapt to varying loads and would require minimal control from higher nervous centers. The exploration of many other possible functions for two (and more) multivibrator effects in small nerve nets has only begun.

Wednesday, May 2, 2 p.m. to 5 p.m., Gold Room

SESSION F

Computer Systems

Chairman:
JAMES H. POMERENE
Thomas J. Watson Research Center,
IBM Corporation
Yorktown Heights, N. Y.

Panelists:
Erich Bloch, IBM Corporation, Poughkeepsie, N. Y.
Howard R. Nonken, Burroughs Laboratories, Paoli, Pa.
Herbert Martin Teager, Massachusetts Institute of Technology, Cambridge, Mass.

Faster computer systems can usually be expected from faster technology, but there are other areas where improvement is needed and can be obtained. Some of these are described.

The processes themselves can be defined in new ways which make solution of many problems more convenient. The use of content-addressed, or "associative" memories can greatly speed up and simplify the searching operations characteristic of many nonnumerical problems. Final results can often be presented to the user in visual displays conveying the essential information compactly and in minimum time; the example described primarily concerns maintenance but has implications for operation results as well.

The Maniac III Arithmetic System

Robert L. Ashenhurst
Institute for Computer Research, University of Chicago, Chicago, Ill.

Unlike most computers, for which there is a formal distinction between "fixed-point" and "floating-point" numbers, the University of Chicago Maniac III computer handles all numbers in a single format (exponent and coefficient, with the coefficient in general not normalized). This permits several types of arithmetic to be defined, which differ in that results are adjusted (coefficient scaled) according to different rules. For example, a "floating-point" operation adjusts the result according to a "significant digit" criterion, while a "specified point" operation adjusts the result to the exponent of the first operand. Normalized arithmetic and a fourth type called "basic" are also available. Since the format for operands is the same for all these types, they can be processed by the various arithmetics without intermediate conversion, thus adding a dimension of flexibility to the computing process.

This paper discusses the arithmetic rules in some detail, showing how consistent conventions for rounding, adjustment of zero and formation of low-order parts are established. The trapping system used for the detection of anomalous results is also described.

An Organization of an Associate Cryogenic Computer

Robert F. Rosin
Department of Electrical Engineering, University of Michigan, Ann Arbor, Mich.

This paper is concerned with the organization of a computer built entirely of cryotrons and operating with an associative (content addressed) memory in which the location of words stored or retrieved is determined by all or part of the contents of the words.

Since cryogenic circuitry is used throughout, the speed of the machine is relatively uniform in both memory and other functions. Thus, the traditional balance of operation time is changed from that existing in more contemporary devices. Moreover, the problem of hardware maintenance has changed due to the very cold environment which must exist for the machine to operate.

A design approach to these and other considerations is evolved which includes putting more logic than usual into the memory and eliminating the necessity for a distinct instruction location counter, address decoder, etc. Problems considered include multi- and parallel processing, indexing and indirect addressing, input-output processing and self-monitoring functions.

Integration and Automatic Fault Location Techniques In Large Digital Data Systems

Donald W. Liddell
U. S. Navy Electronics Laboratory, San Diego, Calif.

A digital computer, if used with proper programming techniques, can be a powerful tool during the process of physical integration of complex digital data processing systems. After system integration as such has been completed, the same techniques may be used to provide performance monitoring and daily calibration status data for all or any part of a system.

Investigation of such programming techniques during system integration of the Developmental Naval Tactical Data System (NTDS) at USNEL produced results which indicated the possibility of using the computer for automatic fault location in the system. Some progress has been made in this area, and a program which allows the NTDS computer to identify a failing logic card associated with its own memory logic and switching circuitry has been successfully demonstrated. The final objectives of this approach are to provide facilities to perform on-line performance monitoring and automatic fault location, reduce to a minimum the external test equipment required for a system, and eliminate insofar as possible the high degree of training presently required in the system maintenance technician.

Wednesday, May 2, 2 p.m. to 5 p.m., Peacock Court (Mark Hopkins Hotel)

SESSION G

Analog Applications and Techniques

Chairman:
VERNON L. LARROWE
**Institute of Science and Technology
University of Michigan
Ann Arbor, Mich.**

Panelists:
Arthur D. Bridgman, Sylvania Electronic Defense Laboratories, Mountain View, Calif.
P. J. Hermann, Dept. of Aerospace Engineering, Iowa State University
Hans E. Meissinger, Hughes Aircraft Company, Culver City, Calif.
James E. Wolle, Analog Computer Laboratory, General Electric Company, Philadelphia, Pa.

The modern electronic analog computer, when intelligently programmed, is capable of solving accurately many engineering problems which arise in current technological research and development.

The papers scheduled for presentation at this session represent a sampling of the many applications of the analog computer to contemporary problems. They are intended, not only to introduce ideas and stimulate thinking, but also to serve as valuable references for persons engaged in solving similar problems on electronic analog computers.

The Use of Computers in Analysis

Walter J. Karplus and Ladis D. Kovach
Department of Engineering, University of California, Los Angeles, Calif.

The computer is recognized as an important engineering design tool permitting the student to test the efficacy of a large number of design hypotheses to determine an optimum design. The application of automatic computers to courses in methods of analysis, however, has not been clearly defined.

This paper gives a number of specific examples of the utilization of computers in engineering analysis. Foremost among these examples are two categories of computer utilization: 1) The application of computers to aid the student in the visualization of dynamic or mathematical phenomena; and 2) The opening up of new approaches to the explanation of system behavior — approaches which are out of reach of conventional analytical methods.

Analog Simulation of Particle Trajectories in Fluid Flow

Vance D. Norum
Space-General Corporation, Glendale, Calif.
Marvin Adelberg and Robert L. Farrenkopf
Space Technology Laboratories, Inc., Redondo Beach, Calif.

This paper presents a detailed account of the analog simulation of particle trajectories in a two-dimensional fluid flow field governed by Laplace's equation. A conductive surface is used as a direct analog of the two-dimensional fluid flow field in conjunction with an electronic analog computer to determine the trajectories of particles in the presence of fluid flow. Emphasis is placed on the concepts of accuracy of the particle trajectories as well as error criteria by which trajectory accuracy can be judged; and on the sources of error inherent in their determination.

A detailed error analysis is presented in which a suitable error model is derived and certain inaccuracies in the computing equipment are assumed in order to predict their effect on the particle trajectories. An example is presented to illustrate the types and magnitudes of errors that exist in a typical problem. The analog simulation is also used to obtain trajectories in a potential flow field distorted by the presence of a cylinder and the results are then compared to a similar case obtained by other authors using a different approach. These results were comparable, with suitable explanations for the difference.

The Application of Finite Fourier Transforms to Analog Computer Simulations

Eric Liban
Grumman Aircraft Engineering Corp., Bethpage, L. I., N. Y.

An analog computer technique for the solution of certain classes of boundary value problems of partial differential equation based on Finite Fourier Transforms is presented, which requires considerably less computer components than conventional finite difference methods. The derivation of the Finite Fourier Transform method is briefly stated and then applied to analog computer simulations of heat transfer equations with linear and nonlinear boundary conditions.

Analog Simulation of the Re-Entry of a Ballistic Missile Warhead and Multiple Decoys

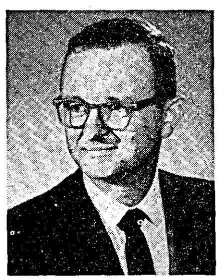
L. E. Fogarty and R. M. Howe
University of Michigan, Ann Arbor, Mich.

The basic problem considered here is the computation of the re-entry trajectory of a single ballistic missile warhead as well as the trajectories of a number of decoys which originate from the warhead trajectory. Suitable three-dimensional equations of motion are presented for a re-entry vehicle with arbitrary drag coefficient, mass, and area, and the analog computer circuit for solving these equations in real time is given. Then a method of using several such circuits to compute simultaneously the trajectories of multiple targets with variations in all three initial velocity components as well as variations in ballistic coefficient is presented.

Thursday, May 3, 9 a.m. to 12 noon, Venetian Room

SESSION H

Information Retrieval



Chairman:
JACK GOLDBERG
Stanford Research Institute
Menlo Park, Calif.

Panelists:
Charles P. Bourne, Stanford Research Institute, Menlo Park, Calif.
R. K. Wakerling, Lawrence Radiation Laboratory, University of California, Berkeley, Calif.

Two basic tasks in an information retrieval system presently requiring human judgment are the establishment of the indexing categories and the indexing of incoming items. There have been numerous suggestions for the mechanization of the latter task, using semantic or statistical analysis. One of the papers at this session will describe a statistical method for establishing the categories themselves, by analysis of the text of a representative body of items. The method might also be useful in mechanizing item indexing in a so-called probabilistic indexing and retrieval system.

Machine retrieval has been proposed for more than just library service. A second paper discusses the possibilities of a mechanized retrieval system at the center of a very complicated technical and human organization — the hospital. The paper illustrates the complexity of the problem, and the diversity of techniques which the system designer must employ.

The Construction of an Empirically Based Mathematically Derived Classification System

Harold Borko
System Development Corp., Santa Monica, Calif.

This study describes a method for developing an empirically based, computer derived classification system. Six hundred and eighteen psychological abstracts were coded in machine language for computer processing. The total text consisted of approximately 50,000 words of which nearly 6,800 were unique words. The computer program arranged these words in order of frequency of occurence. From the list of words which occurred 20 or more times, excluding syntactical terms such as *and, but, of,* etc., the investigator selected 90 words for use as index terms. These were arranged in a data matrix with the terms on the horizontal and the document number on the vertical axis. The cells contained the number of times the term was used in the document. Based on these data, a correlation matrix 90x90 in size, was computed which showed the relationship of each term to every other term. The matrix was factor analyzed and the first 10 eigenvectors were selected as factors. These were rotated for meaning and interpreted as major categories in a classification system. These factors were compared with, and shown to be compatible but not identical to, the classification system used by the American Psychological Association. The results demonstrate the feasibility of an empirically derived classification system and establish the value of factor analysis as a technique in language data processing.

The Storage and Retrieval of Physiological and Medical Data in a Modern Hospital

Paul C. Tiffany
Aerospace Corporation, El Segundo, Calif.

As an introduction, this paper considers some of the problems of data handling in a modern hospital. Next, the needs of the users of the data are considered. The principal area of interest is directed toward the hospital function which deals with the storage and retrieval of the clinical record *after* the patient's hospitalization. An estimation is made of the large amounts of terms used in medicine, and of two currently employed schemes for the indexing of diseases and operations. A description is made of a storage and retrieval system which allows the medical researcher to examine and browse through clinical records or abstracts of the records. The paper concludes with observations on the need for applied research and system development to acquire pilot systems for the storage and retrieval of physiological and medical data.

Thursday, May 3, 9 a.m. to 12 noon, Gold Room

SESSION I

Programming and Coding — Part 1

Chairman:
BERNARD A. GALLER
Computing Center
University of Michigan

Panelists:
Richard W. Hamming, Bell Telephone Labs, Murray Hill, N. J.
Edwin L. Jacks, Data Processing Section, General Motors, Inc., Detroit, Mich.
Alan J. Perlis, Computation Center, Carnegie Tech, Pittsburgh, Pa.
Francis V. Wagner, North American Aviation Company, Los Angeles, Calif.

The most striking feature about programming today is the variety of problems on which work is being done. We normally think of activity in programming as being concerned with sub-routines, translators, or system development, but as we shall see in the papers presented here, there are other areas under active investigation.

Two of the papers are concerned with new developments in the languages which we use in expressing algorithms. The very existence of these papers testifies that the topics which concern them must inevitably be provided for in computing languages. Two of the papers deal with new requirements on operating systems. As problems become more complex, we find that we must consider the implications of dynamic storage allocation, and these two papers are pointing up some of the different approaches to the problem.

The fifth paper in this session is also concerned with the complexity of future problems, but from a different point of view. Here we need to examine the methods used to determine when a program is working correctly. The trend toward putting the burden more squarely on the "shoulders" of the computer continues, and, of course, it must.

Fact Compiler Segmentation

Martin N. Greenfield

Minneapolis-Honeywell EDP Division, Wellesley Hills, Mass.

The manner in which the Fact Compiler handles segmentation of programs is described. Programs are divided into many interdependent segments in order to optimize the use of core storage. For instance, the internal storage required to handle a tape file (buffers, labels, controls) would be one segment. This segment would be operated upon by other processing segments. Each of the segments may be activated or released independently as required. Each of the segments is relocated at execution time. Segments in memory may be subsequently moved by the monitor in order to fit additional segments in core. The monitor has the ability to organize the required rearrangement. A hardware error detection feature is used to make the currently operating segments sensitive to the absence of a segment about to be addressed. This provides an efficient linkage to the monitor enabling it to activate the segment.

A General Test Data Generator for Cobol

Lt. Richard L. Sauder

Wright-Patterson Air Force Base, Ohio

Program checkout procedures are often hampered by the nonavailability of adequate test data. To reduce this problem, a Test Data Generator is currently being developed to operate in conjunction with the Cobol Compiler implemented by the Air Force Logistics Command. The system not only builds data items conforming to descriptions given in the Data Division of the associated Cobol Source Program but also inserts in these items necessary data relationships and requirements to test various branches of the Cobol object program. The generator is labelled "general" inasmuch as the method of expressing these data requirements is designed to be as hardware independent as the Cobol compiler employed to build the program being tested. This paper discusses both the utilization and the method of operation of the Data Generator.

Data Structures that Generalize Rectangular Arrays

Samuel A. Hoffman

Kettelle & Wagner, Paoli, Pa.

A class of data structures, useful in data processing, is defined. These are called generalized structures. A formal method of describing a generalized structure is given. It is shown how a compiler program, once given such a description or descriptor, can allocate contiguous storage and determine the appropriate form of the storage mapping function which will relate suitably referenced positions in the structure with positions in the linear storage. The suitable referencing of data in the structure is accomplished by reference expressions; these are defined and it is shown how, at run time, they are operated upon by the storage mapping function.

The class of structures, the descriptors, the form of the storage mapping function and the reference expressions are all shown to be direct generalizations of the corresponding considerations for n-dimensional rectangular arrays.

Finally, an Algol program for the Burroughs 220 computer is briefly described. The program simulates the functions that a compiler, upon receiving a descriptor, would perform in forming the storage mapping function, and the processing that would be carried out at run time when a reference expression is presented.

Thursday, May 3, 2 p.m. to 5 p.m., Gold Room

SESSION I

Programming and Coding — Part 2

Chairman: Same as Part 1
Panelists: Same as Part 1

An Experimental Time-Sharing System

Fernando J. Corbato

Massachusetts Institute of Technology Computation Center, Cambridge, Mass.

Time-sharing a digital computer is subject to two common interpretations. One can mean using different parts of the hardare at the same time for different tasks, or one can mean several persons making use of the computer at the same time. The first meaning, often called multiprogramming, is oriented towards hardware efficiency in the sense of attempting to attain complete utilization of all components. The second meaning of time-sharing, which is meant here, is primarily concerned with the efficiency of persons trying to use a computer. Computer efficiency must still be considered but only in the perspective of the total system utility.

The motivation for time-shared computer usage arises out of the slow man-computer interaction rate possible with the bigger, more-advanced computers. This rate has changed little (and become worse in some cases) in the last decade of widespread computer use. The desired performance of a time-shared computer will be discussed as well as specific hardware, programming and usage problems. The operational characteristics of an experimental time-sharing programming system prepared for an IBM 7090 will be described. Consideration will be given to the design compromises and to the future avenues of improvement.

A Programming Language

Kenneth E. Iverson

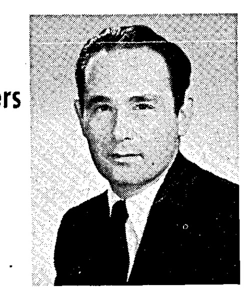
Thomas J. Watson Research Center, IBM Corporation, Yorktown Heights, N. Y.

The paper describes a succinct problem-oriented programming language. The language is broad in scope, having been developed for, and applied effectively in, such diverse areas as microprogramming, switching theory, operations research, information retrieval, sorting theory, structure of compilers, search procedures, and language translation. The language permits a high degree of useful formalism. It relies heavily on a systematic extension of a small set of basic operations to vectors, matrices, and trees, and on a family of flexible selection operations controlled by logical vectors. Illustrations will be drawn from a variety of applications.

Thursday, May 3, 2 p.m. to 5 p.m., Venetian Room

SESSION J

World Peace and Role of Computers



Chairman:
LOUIS FEIN
Consultant
Palo Alto, California

Panel Discussion

"Peace and the Role of Computers" defines the theme of this panel discussion by experts in the area of sociological and political research.

Replacing man with computers for making humanistic decisions is a novel and intriguing area which has capabilities and limitations that are largely unknown. The objectives of this discussion will be to explore ways in which computers can help peace gamers and other peace researchers in performing their tasks and solving their problems; and also bring to light what measures can be taken by professional computer people to further this application of machine to man's problems.

Subjects to be discussed are:
(1) Identifying necessary and sufficient conditions (economic, political, sociological, psychological, cultural, military, religious, moral, ethical, ideological, legal and semantic) for preventing major international conflicts—conflicts for whose resolution nations seriously consider all-out nuclear war as an acceptable instrument; (2) generating alternative models of society whose most important property is that they meet these necessary and sufficient conditions, (3) generating alternative routes of getting from our present world condition to a no-major-conflict condition of society.

In the event of conflict, peace research concentrates on (4) generating alternative non-destructive conflict-resolution policies and strategies, and (5) generating detailed ways of implementing these policies in practice.

Papers will be integrated with a continuity of subject matter from paper to paper.

Political scientists, behavioral scientists and computer scientists will explore some of the general problem areas of peace research and some of those specific classes of problems — if any — amenable to solution with the aid of computers. Finally, the credibility of computer-generated recommendations will be discussed.

Peace research appears to deal with five main problem areas: (1) Identifying necessary and sufficient conditions (economic, political, sociologial, psychological, cultural, military, religious, moral, ethical, ideological, legal and semantic) for preventing major international conflicts — conflicts for whose resolution nations seriously consider all-out nuclear war as an acceptable instrument; (2) generating alternative models of society whose most important property is that they meet these necessary and sufficient conditions; (3) generating alternative routes of getting from our present world condition to a condition of society with no major conflicts.

In the event of conflict, the research would concentrate on (1) generating alternative non-destructive strategies and policies to resolve conflicts, and (2) generating detailed ways of implementing these policies in practice.

Papers will be integrated with a continuity of subject matter from paper to paper. The format and content of the session may be considered as a very small scale model of the whole *process* of analyzing important sociological problems and solving them with the aid of computers.

Thursday, May 3, 2 p.m. to 5 p.m., Peacock Court (Mark Hopkins Hotel)

SESSION K

DDA and Hybrid Computation

Chairman:
HAROLD K. SKRAMSTAD
Naval Ordnance Laboratory
Corona, California

Panelists:
Robert M. Barnett, Ames Research Center, Moffet Field, Calif.
W. N. McLean, North American Aviation, Los Angeles, Calif.
Fred Shaver, National Aeronautics and Space Administration, Marshall Space Flight Center, Huntsville, Ala.

The Digital Differential Analyzer or DDA is a special-purpose digital computer of the incremental type which has the ability to solve differential equation problems with high efficiency. Programmed in the manner of analog computers, but free of analog limitations on precision, they are being increasingly used in real-time simulation and control, due primarily to the order of magnitude increases in speed attainable in recent years.

The first paper 'Design of a One-Megacycle Iteration Rate DDA" describes a new DDA of exceptionally high speed. The second paper "DDA Error Analysis Using Sampled Data Techniques" is a thorough analytical study of the errors produced in DDA's in which a conceptually simple error theory is evolved.

The third paper "Hybrid Techniques for Optimization Problems" describes a hybrid technique, combining analog and digital hardware, for minimizing a function dependent on the solution of a set of differential equations, by means of a systematic search procedure in parameter space.

Design of a One-Megacycle Iteration Rate DDA

R. E. Bradley, Design Engineer
J. F. Genna, Project Engineer
Hazeltine Technical Development Center, Inc., Indianapolis, Ind.

This paper discusses the special design features of a digital differential analyzer (DDA) which operates at a rate of one million iterations per second. SPEDAC (Solid-state Parallel Expandable Differential Analyzer Computer) features paralel organization of the integrators, serial-parallel organization of the integrators, serial-parallel arithmetic within the iteration cycle, 26-bit word length, and the integral inclusion of a multi-function digital function generator. The computer is programmed in analog computer fashion by means of plug board interconnection of the integrators.

To achieve a one-megacycle clock rate, the arithmetic circuits operate at a six-megacycle clock rate. Trapezoidal integration is performed. Initial conditions and function generator breakpoints and slopes are stored as parallel words in a multiplane magnetic core memory. The use of a parallel memory is exploited to permit direct parallel communication and hybrid operation with external large-scale general-purpose digital computers.

DDA Error Analysis Using Sampled Data Techniques

Don J. Nelson
University of Nebraska, Department of Engineering, Lincoln, Neb.

The Z or W-Transforms may be combined with matrix techniques to analyze errors in digital differential analyzers. This analysis demonstrates how errors in the solution of linear differential equations with constant coefficients can be simply determined and how solutions to these equations can be developed, the accuracy of which is limited only by round-off.

Hybrid Techniques Applied to Optimization Problems

Hans S. Witsenhausen
Electronic Associates, Inc., Princeton, N. J.

A hybrid system is described consisting of a general-purpose analog computer and a specially designed digital expansion system (DES). One of the functions of this expansion is to act as an intelligent operator of the analog high-speed computing capability. To this end, the expansion contains logic building blocks (essentially flip-flops and gates) interconnected on a patch-panel. Switching commands are transmitted from the DES to analog gates, memory units and mode control. Comparators transmit quantized information from the analog to the DES.

Application of this simplest capability of the hybrid approach is illustrated for the optimization problem, stated as follows:

A function dependent on the solution of a set of differential and/or algebraic equations containing adjustable parameters is to be minimized by systematic search procedures in parameter space. Among the applications are model building, process optimization and matching of boundary conditions. One possible procedure has been selected for illustration and its hybrid implementation is carried out for the general n-parameter case. Exploratory runs determine approximate partial derivatives from which a quantized direction is determined. Steps are taken in this direction until lack of improvement forces a redetermination of partials. The techniques of programming the DES and the hybrid interconnections are emphasized. ■

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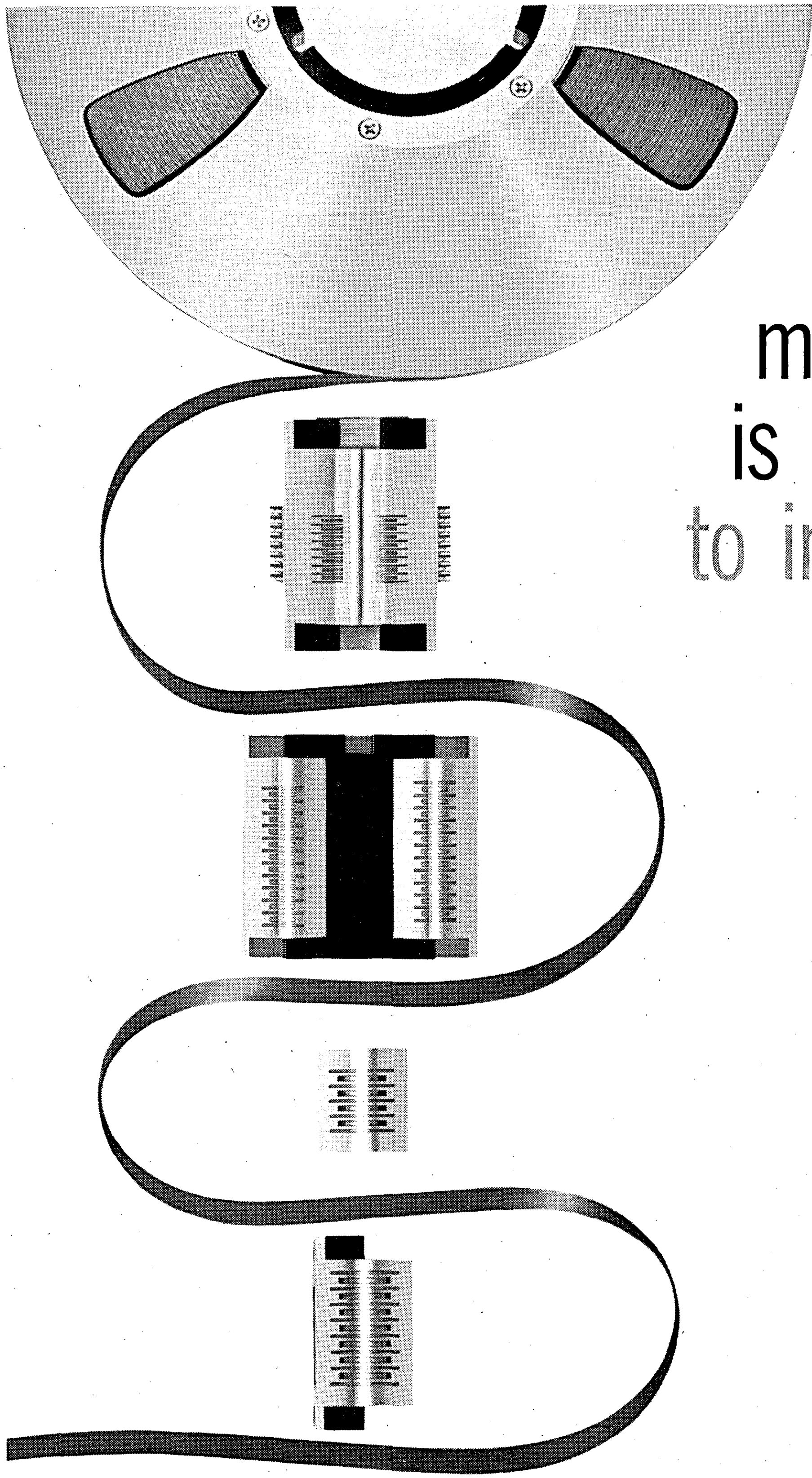

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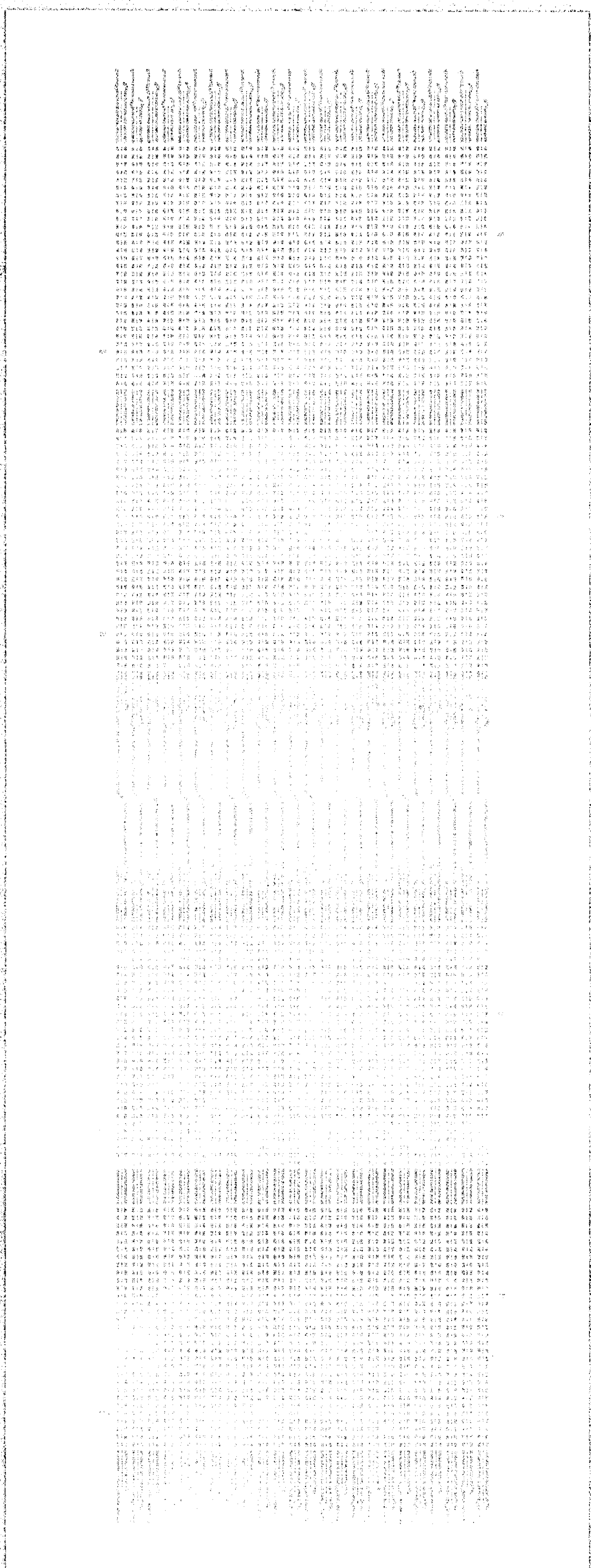

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3072 bit thin film memory plane

Burroughs' new high density thin film plane is the [illegible] memory device commercially available. This [illegible] plane operates to 5 [illegible] and is priced at under [illegible] per bit, making it ideal for the [illegible] memory applications. With [illegible] experience in manufacturing and marketing thin film memory planes, Burroughs once again leads the way in advanced memory techniques. Write for complete technical data on the new high density thin film plane, [illegible]

Burroughs Corporation

NEWS BRIEFS

CALL FOR INTERNATIONAL GLOSSARY STANDARDS

Individuals or organizations interested in submitting draft proposals for an international glossary standard on computers and information processing should contact J. F. Traub, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

Proposals for the glossary standard will be considered at the fall 1962 meeting of the TC-97 committee of the International Standards Organization. The glossary working group of TC-97 is WG-A, which is chaired by the Netherlands.

JOHNSON TO CHAIR 1963 SJCC

Dr. E. Calvin Johnson, head of Bendix Laboratories Computer Development Department, has been named chairman of the 1963 Spring Joint Computer Conference, to be held in Detroit.

Dr. Johnson joined the Research Laboratories Division of Bendix in 1951, where he has participated in a number of study and development programs involving special purpose analog and digital computers.

A member of the ACM, IRE, and AIEE, he organized the Detroit chapter of the IRE Professional Group on Electronic Computers and is currently on the national administrative committee.

14 UNIVERSITIES ADOPT U-M EXECUTIVE SYSTEM

Details of the U-M executive system, developed by the University of Michigan's Computer Center, were presented to computing center staff members from fourteen universities at a recent two-day meeting at Ann Arbor. The University representatives will implement the system at their respective centers.

The system, it is claimed, allows dp equipment to be used directly on problem solving almost 70 percent of the time. Most other systems, says Dr. Bernard A. Galler, acting director of the U-M Center, achieve only a 35-40 percent computation rate.

For scheduling computer time, the system supervises the necessary I/O steps. The problem, stated on punched cards in one of two languages—FORTRAN or MAD—is translated into machine language and stored in memory prior to actual computation. In addition to the two languages, the system includes the UMAP assembly program.

Attending the meeting were representatives of Michigan State; MIT; Yale; Illinois; Northwestern; Ohio State; Columbia; Purdue; Florida state; UCLA; NYU; Indiana; Chicago; and Texas A & M.

COMPUTER DYNAMICS WINS OVER C-E-I-R SUIT

The suit filed by C-E-I-R, Inc., to enjoin the Computer Dynamics Corp. from seeking to do business with C-E-I-R's former or prospective clients was dismissed in Montgomery County (Md.) Circuit Court recently.

C-E-I-R has appealed the decision to the Maryland Court of Appeals. The appeal may be argued within the next sixty days.

In ruling on the motion to dismiss, filed by attorneys for Computer Dynamics after a week of testimony by C-E-I-R, Judge Kathryn L. Shook stated that the former employees of C-E-I-R who formed the defendant company, "took no knowledge with them that was the employer's property, nor secret methods or formula," and that C-E-I-R had "no proprietary rights in business from the United States Government."

4,000 EXPECTED AT NMAA CONFERENCE, JUNE 19-22

"Key to Efficiency" has been set as the theme for the 11th Annual International Conference and Business Exposition, sponsored by the National Machine Accountants Association. To be held at New York City's Hotel Statler-Hilton, June 19-22, an attendance of more than 4,000 is expected.

Features of the conference include 30 seminars on dp, covering six subject areas; "Datathon," a ten-hour, closed-circuit TV program; and a President's Forum, comprised of chief executives of leading dp manufacturers.

Current plans are to conduct each of the thirty seminars twice, so if there is a conflict on two seminars being held concurrently, one can be attended later in the program. Fifteen seminars are planned for each morning and each afternoon, June 20 an 21.

The Datathon program will include a Data Processing Panel from specialized areas such as information systems, optical scanning, information retrieval, scheduling, etc. Also to be featured are interviews with persons prominent in dp, seminar speakers, exhibitors and conference attendees.

Topic of the President's Forum will be: "The Direction of Data Processing and its Relationship to Automation." Scheduled to participate are K. T. Bement, Burroughs; R. E. Pfenning, GE; O. M. Scott, IBM; W. W. Finke, Honeywell; R. G. Chollar, NCR; T. A. Smith, RCA; D. L. Bibby, RemRand. Moderating the program will be Walter Cronkite, of CBS.

The Conference's keynote speaker will be Dr. Kenneth McFarland, educational consultant, General Motors. Governor Nelson Rockefeller will officially open the Conference with a welcoming address.

ACM ISSUES CALL FOR PAPERS

The Association for Computing Machinery has issued a Call for Papers, which will be read at the 1962 ACM National Conference, September 4-7 at the Hotel Syracuse and the War Memorial, Syracuse, N. Y.

The Conference will include contributed papers in the following areas: Scientific Information Processing; Automatic Programming and Computer Language; Business Information Processing; Information Retrieval; Language Translation; Education; Real Time Information Processing; Social Aspects and Philosophies.

In order to be considered, an 800-1000 word illustrated summary and a 35 word abstract (both in quadruplicate) should be sent on or before May 1, 1962, to Robert W. Beckwith, 7614 Hunt Lane, Fayetteville, N. Y.

General chairman of the Conference Committee is Robert S. Jones (Sylvania); other members of the committee are: Joseph C. Batz (GE), vice chairman; Eleanor W. Kelsey (Sperry-Rand), secretary; Robert W. Beckwith (GE) and John P. Menard (Syracuse Univ.), technical program; Bernard G. Flanagan (Merchants National Bank & Trust Co.), treasurer; James A. Iverson (GE), publicity; Joseph Banas (Baldwinsville School System), exhibits; William Warmuth and Elizabeth G. Hill (IBM), arrangements-facilities; and Lewis Winner (consultant), conference-exhibit consultant.

L.A. SCHOOL SYSTEM ORDERS B-5000

A Burroughs B5000 has been ordered by the Los Angeles City School System, with delivery scheduled for early 1963. The installation will include 32K words of drum memory, with an additional 4K of core memory, one I/O channel, four mag tape units, card reader, punch, and line printer.

Some 46,000 employees are on the school system's payroll, involving 54 different types of payroll. Over 650 job classifications are included, plus three retirement classifications and 16 types of voluntary payroll deductions.

Utilization of the B-5000 will reduce computer operations from three shifts to one, allowing the system to be used for increased statistical analysis and expansion of general accounting and budgetary control applications.

CIRCLE 100 ON READER CARD

MIT COMPUTER LECTURES IN BOOK FORM

The M.I.T. lecture series on "Management and the Computer of the Future" has been published by John Wiley and Sons and the M.I.T. Press in a hardbound format.

Among the topics discussed were: "Scientists and Decision Making," C. P. Snow; "Managerial Decision Making," J. W. Forrester; "Simulation of Human Thinking," H. A. Simon; "The Computer in the University," A. J. Perlis; "Time-Sharing Computer Systems," J. McCarthy; "A New Concept in Programming," G. W. Brown; "What Computers Should Be Doing," J. R. Pierce, and "A Library for 2000 A. D.," J. G. Kemeny.

The discussions were held at M.I.T. last year as part of the school's 100th anniversary. Editor of the book is Martin Greenberger, of the School of Industrial Management.

CIRCLE 101 ON READER CARD

● Control Data Corporation's earnings for the six-month period ending December 31, 1961, totaled $17,308,142, as compared with $8,543,126 for the same period of the previous year. Net earnings came to $636,990; in 1960, the figure was $503,722. Per share earnings on common stock was 16¢.

● A Honeywell 400 will be used by the Commission on Professional and Hospital Activity, Ann Arbor, Michigan, to analyze the clinical records of hospital patients throughout the U. S. and Canada.

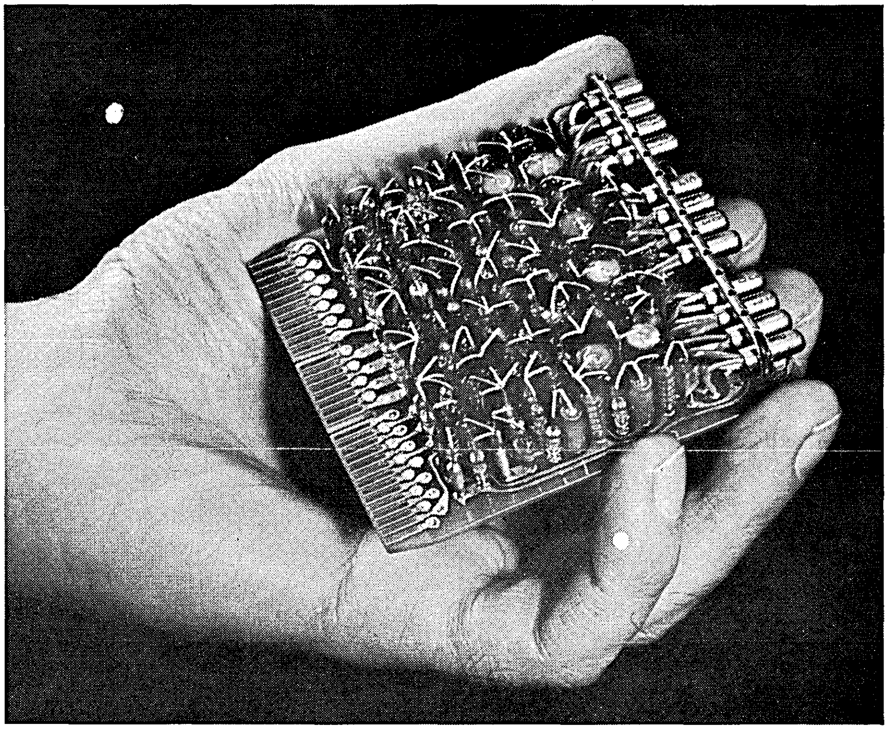
CIRCLE 102 ON READER CARD

● The National Science Foundation has awarded a $46,000 grant to the University of Michigan for research on "Theory of Automata." The project, under the direction of Prof. Arthur W. Burks, proposes to define broad mathematical classes of computing devices, sort out those automata that could be constructed into actual computers, and will explore ways in which the machines can be built.

FOR GENERAL ELECTRIC: CIRCLE 37 ON READER CARD →

IMAGINATIVE PACKAGING

Up to 247 standard parts on a 3-inch by 3-inch card with standard techniques



Electronic packaging engineers are perennially straight-jacketed with a multitude of system and functional constraints and then expected to enclose the several million parts of a complex electronic system into neat, logical, reliable, compact, efficient, economical, and readily producible and maintainable packages.

Litton packaging engineers drew just such an assignment when they were required to design packaging for a tactical digital data system to be installed in a carrier-based airborne early warning and control aircraft.

The constraints were: use standard parts; use standard techniques; achieve maximum producibility; confine system to a lesser volume of space than normally considered practicable; maintain flexibility required of a developmental system; and achieve better reliability than specified for airborne electronics.

Despite these stringent constraints, Litton packaging engineers successfully met all requirements. Most significantly, their efforts resulted in containing the system in half the weight and a quarter of the space of comparable systems.

Typical of the way in which packaging problems were resolved was the manner in which card-mounted digital circuits were handled. First, an extensive study was made of parts density, card space, and interconnections. The over 2000 cards in the system were composed of 120 types. 1900 of these cards (covering all 120 types) were designed to conform to a single standard grid pattern.

A square card (3″ x 3″) was selected for greatest loading efficiency. By edge-mounting the parts (standing them on end), densities as high as 247 parts per card were attained. Parts were distributed according to a technique that afforded the highest possible volumetric efficiency as well as optimum pin efficiency. On each card, circuits requiring many input/output leads were combined with those using only a few. Instead of the conventional 4 flip-flops per card, for example, 3 flip-flops and some logic gating were placed on a single card to avoid wasting leads. Moreover, several parts converging into a common connection were so placed that only a single lead was used. Parallel circuit paths were provided both on the card and through the connector to insure reliability.

By these and other techniques, packaging of extremely high density and reliability was attained. Analog circuits, including gear trains and servos, were mounted on the same type of cards as the digital circuits to make possible one standard card design and tooling.

Why talk about past engineering successes? With military and proprietary restrictions as they are, it's difficult to do otherwise. The point is, this was, and still is, pretty solid package engineering. Litton's new programs offer a host of extremely challenging problems that can be solved only through imagination-stretching, advanced electronic engineering. If such a climate appeals to you, write Harry D. Laur, Litton Systems, Inc., Data Systems Division, 6700 Eton Avenue, Canoga Park, California; or telephone DIamond 6-4040.

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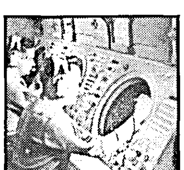

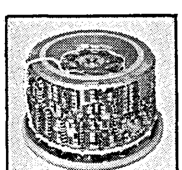

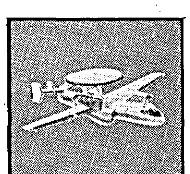

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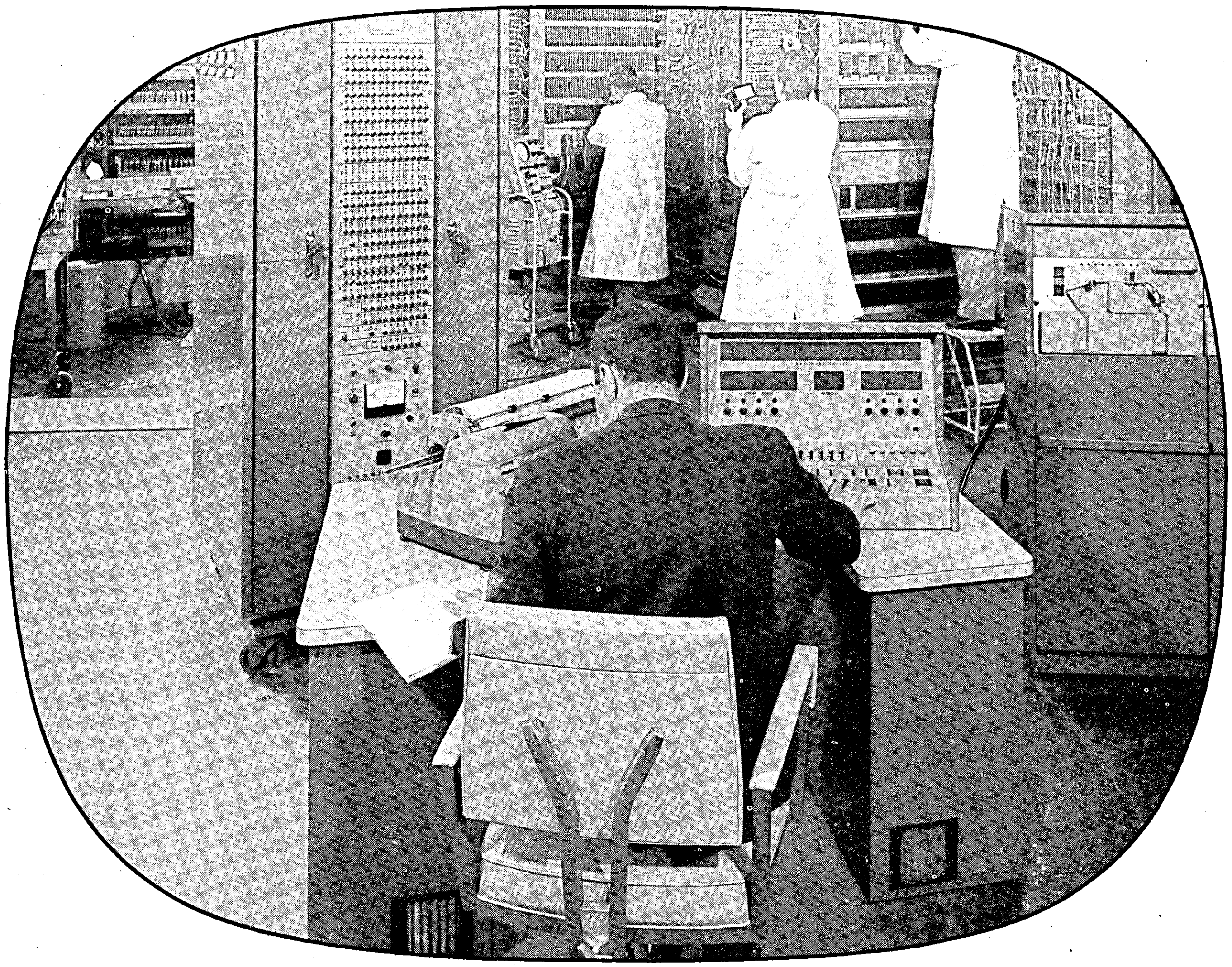

General Mills Computers to Process Data from NASA's Orbiting Astronomical Observatory

When the National Aeronautics and Space Administration launches its first OAO satellite late in 1963, General Mills AD/ECS-37 computers will perform data reduction and processing of information telemetered from the satellite. Several of these computers are shown above during "production-line" checkout. The first such computer has been delivered to the Goddard Space Flight Center at Greenbelt, Maryland. Additional computers, now being completed, will be installed at ground stations in NASA's minitrack network.

The AD/ECS-37 is a solid state, parallel, general-purpose digital computer system. It can be adapted readily to fit specific applications. Low cost "customization" has been made possible by the use of plug-in, printed circuit instruction cards. It has a 36-bit (plus sign) word length and utilizes a 4,096 word random access magnetic core memory (expandable to 8,192 words). The computing system has a simultaneous input-output-compute capability and can be used for scientific and engineering calculations, process control, or direct data handling and processing. External air conditioning is not required. **Write for the new booklet, AD/ECS Digital Computer Systems.**

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CIRCLE 38 ON READER CARD

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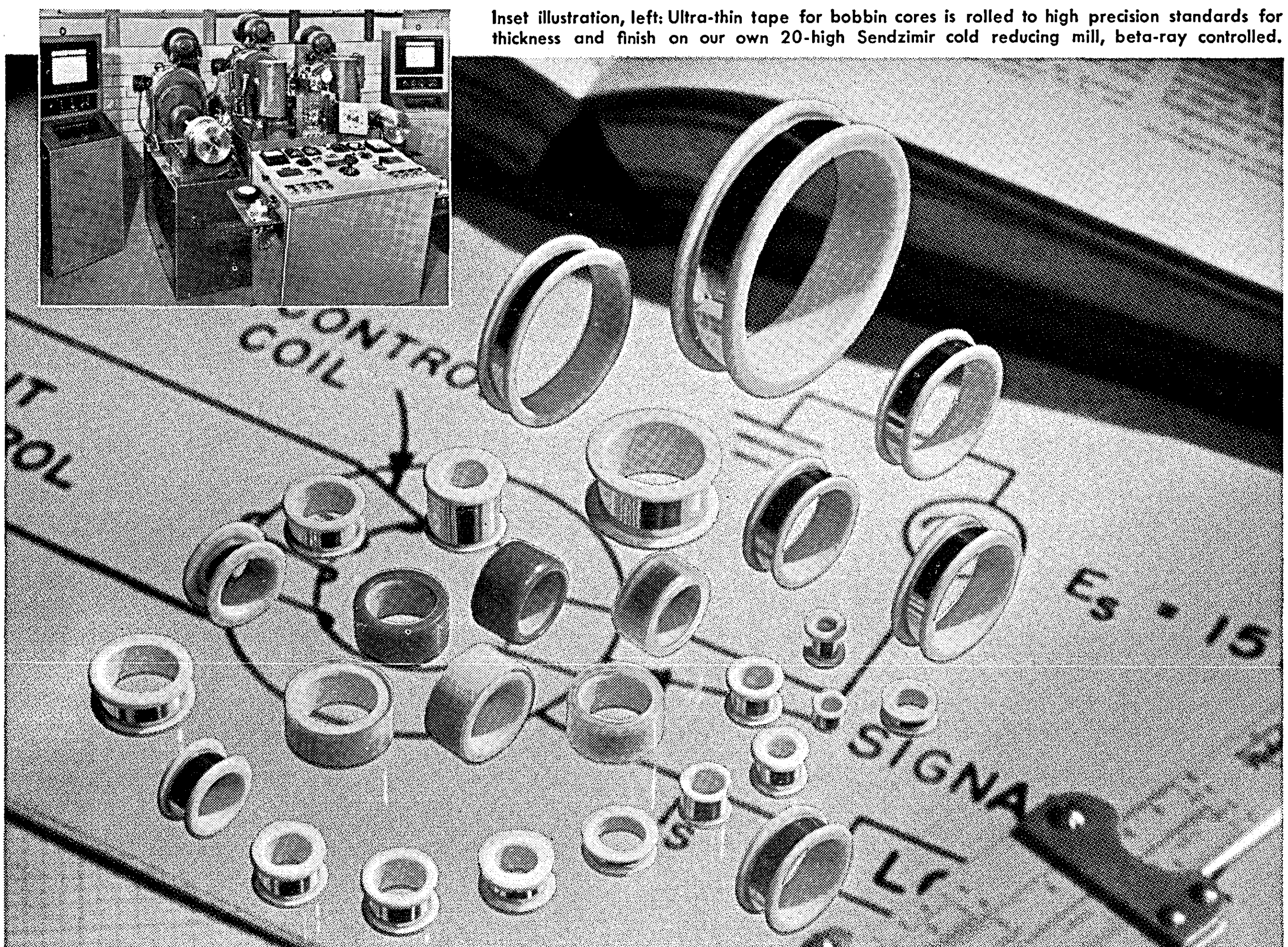
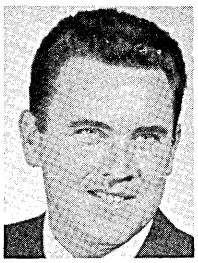


CIRCLE 39 ON READER CARD

ALGOL vs. FORTRAN

a defense of the former

by JAMES T. McMAHON, the Lamellar Corp. of America, Thousand Oaks, Calif.



Programming languages are well established as a tool in the use of electronic digital computers. Among the programming languages considered to be most useful are those which may be described as "machine-independent" and "problem-oriented." The first phrase implies that the programming language does not vary with the computer on which the problem is to be done. The second phrase implies that the only effort required of a human programmer is to state the problem in the programming language.

FORTRAN and ALGOL are in the forefront of those programming languages commonly described by the above terms. It is probably safe to say that, today, more computer programs are written in FORTRAN than in any other programming language.

Because of this, the use of FORTRAN is well entrenched. Programmers working in FORTRAN are many, and their work forms voluminous parts of the program library of many large computing laboratories.

The current entrenchment of FORTRAN tends to insure its continuing use, whether this continuation is otherwise logically and economically defensible. One objection most commonly heard against changing from FORTRAN to some other language is the "investment" in FORTRAN which cannot be thrown away.

Yet there is not one FORTRAN. There are a dozen or so FORTRANS. The difference in FORTRAN versions, according to McCracken in his most recent book[1], "... are in two categories: minor variations in details and fundamental differences in scope." In short, FORTRAN is not machine-independent.

That this might be so is clear from the fact that FORTRAN has no rigid syntactical definition and was, from the beginning, written without the benefit of one.

In comparison to this, ALGOL began with a rigid syntactical definition. It is in no sense machine-oriented. In fact, one may write problem statements in ALGOL without regard to the machine on which they are to be run, or whether they are to be run on any machine.

The development of ALGOL, well documented in such publications as *The Communications of the Association for Computing Machinery,* clearly shows the intent to make ALGOL a problem statement language. No other primary intent, in fact, was claimed for it.

Comparison is sometimes made between the historic versions of ALGOL (ALGOL '60, and the International Algebraic Language – sometimes called ALGOL '58) as basis for the comment, "There are several versions of ALGOL too!" There is an important difference, however. Each of the subsequent ALGOL developments is defined and preceded by a rigid syntactical statement. The various FORTRANS, on the other hand, have stemmed from hasty application to a new machine model.

The crux of the matter lies in ALGOL being a problem statement language. Every FORTRAN is a machine-oriented macro-language.

Criticisms of ALGOL which ignore this fact frequently are analogous to the following ridiculous conversation:

Q. "What do you think of the English language?"

A. "It will never replace the typewriter."

ALGOL is not a computing machine, nor is it, essentially, a computing machine language. It is a problem statement language whose structure is particularly well-suited for translation by existing computers. To compare ALGOL with a FORTRAN version aimed at and used on a particular computer makes as much sense as comparing rosebushes and pigs. There is no FORTRAN that is not defined for use on a particular digital computer.

Short examination of ALGOL in comparison to any of the FORTRAN versions will serve to convince a programmer or a mathematician of the following facts:

1. ALGOL is a much more powerful and general language than FORTRAN. It allows the user to write much more comprehensive problems in source language. There is no need to descend into lower-level languages or to side-track into ALGOL-type extensions at source language level.

2. ALGOL is much freer of restrictions and exceptions than FORTRAN. The effort required is less to master an ALGOL subset with the same capability as FORTRAN.

3. ALGOL offers better annotation capabilities. It permits the user to include self-explanatory comments and to introduce such annotation directly into sub-program parameter calls.

It is unfortunate but true that ALGOL has received a "bad press." DATAMATION (October, 1961) in reporting on the annual RAND symposium listed a number of loud objections. Most of the more frequently heard objections aimed at ALGOL are found in this report. Among them is the charge that the existing descriptions of ALGOL are "nearly impossible" to read. There is, unfortunately, some truth to this when one considers the language in which the full syntactical definitions are couched. In using a problem statement language, however, one does not continually refer to the full syntactical definitions, just as one does not look up every word in the dictionary when writing English. The full-blown mathematical definitions of high-school algebra can fill many books. Yet most of us use algebra frequently in a pick-and-shovel fashion without ever referring to the base of theory underlying it.

Consider the remarks of Robert W. Bemer[2] of the International Business Machines Corporation: "... ALGOL is a far superior language to any of its predecessors." In describing his work with various languages, Bemer said, "I have enough faith in the eventual future of ALGOL to have caused a program to be constructed which converts from FORTRAN source language into a rather stupid ALGOL. I have been asked many times why we did not make it translate from ALGOL to FORTRAN so that the existing processors could be utilized. The answer has always been that we wish to obsolete FORTRAN and scrap it, not perpetuate it. Its purpose has been served."

Bemer's remarks serve to point up two other matters. It is worthy of note that his program translated from FORTRAN into "rather stupid" ALGOL. The indication is, clearly, that ALGOL is a more comprehensive language than FORTRAN, so that a FORTRAN statement written in ALGOL appears rather like pidgin English. This greater comprehensiveness of ALGOL is the basis of another criticism leveled against it by those who say ALGOL is too complex, and hence, difficult to teach and learn. The facts are, as Bemer's program illustrates, that one need not know and use all of ALGOL to make constructive use of it, just as one need not memorize the dictionary to write sensible English. However, for those who wish to apply its full repertoire, ALGOL is a statement language of considerably more power than FORTRAN.

Bemer also did not wish to translate from ALGOL into FORTRAN. This is understandable for several reasons. In the first place, it would have been a near-impossible job to translate the broad generality of ALGOL into FORTRAN with its many restrictions. The resulting translation would result in a vastly expanded program. Such a translation would be highly impractical. The impracticality gets worse when one looks at the implementation used in FORTRAN systems. Existing machine versions of FORTRAN, without exception, make use of yet another intermediate language level intervening between the FORTRAN statement and the machine language statement. This is frequently defended on the basis that it is "essential" to the debugging of programs. Yet the facts are that many FORTRAN programmers doing successful work daily, and with output as high as other programmers, know no other problem statement language than FORTRAN, and could not debug in an intermediate language, nor in a machine language, even if they wished to do so.

Had Bemer been able to translate ALGOL to FORTRAN to the various levels of intermediate language (FAP, etc.) the total process would, without doubt, have been too ponderous for any sensible use.

Machine implementations of ALGOL are in daily use. One of these is the Burroughs Algebraic Compiler for the 220. Customers who use this programming system keep their problem documentation in a single language level. They do not have various statements, card decks, print-outs, and other such material for a single problem. There is no question of fiddling with the program at one level and failing to update the various documents at all the other levels.

Users also find that ALGOL is a language with ample notational power. Its offers full capability for the initial statement of computational algorithms.

They are not penalized by slow compilation speeds. Initial compiling and subsequent recompilings for check-out or program maintenance proceed directly from the problem statement to machine language. This compiler readily translated at rates from 400 to 500 instructions per minute. It is clearly limited by the internal speed of the 220. Yet the 220 is not a "slow" machine compared to many of the machines which translate FORTRAN statements at equivalent or lesser rates.

Why this difference? The answer rests between the fact that ALGOL has better "translation" characteristics than FORTRAN and in the manner in which a programming system was designed and built up using a representation of ALGOL as the language structure. The programmer can safely imagine its language is the machine language of a hypothetical system. It was built from the ground up with no constraints imposed by previous systems work. It was designed to compile rapidly. This is not because the designers had a fetish about rapid compilation, but rather because they recognized that rapid compiling provided a keystone about which to build their system. This is so because their rapid compilation techniques made the twin concepts of intrinsic symbolic debugging aids and single-language-level documentation practical. The result is a translator for the 220 compacted into 3200 word locations. Since this is a one pass compiler it clearly does not make use of magnetic tape for all of the purposes that most other programming systems do. It does not use tape to store and recall "approximations" to the final language. It makes use of no intermediate languages, but translates directly from ALGOL to machine language.

This latter comparison should stand as an effective answer to those critics who persist in comparing the ALGOL concept with a machine implementation of FORTRAN on economic grounds, and who come up with the answer, "It will never replace the typewriter." As a matter of fact, there exists a machine implementation of ALGOL demonstrating efficiency many times that of any existing FORTRAN implementation.

What of the object code produced by this machine implementation of ALGOL? Comparison of like problems, with due regard to internal machine speeds and organization, indicates that the object code produced by the 220 compiler is at least as efficient as that produced by any FORTRAN compiler.

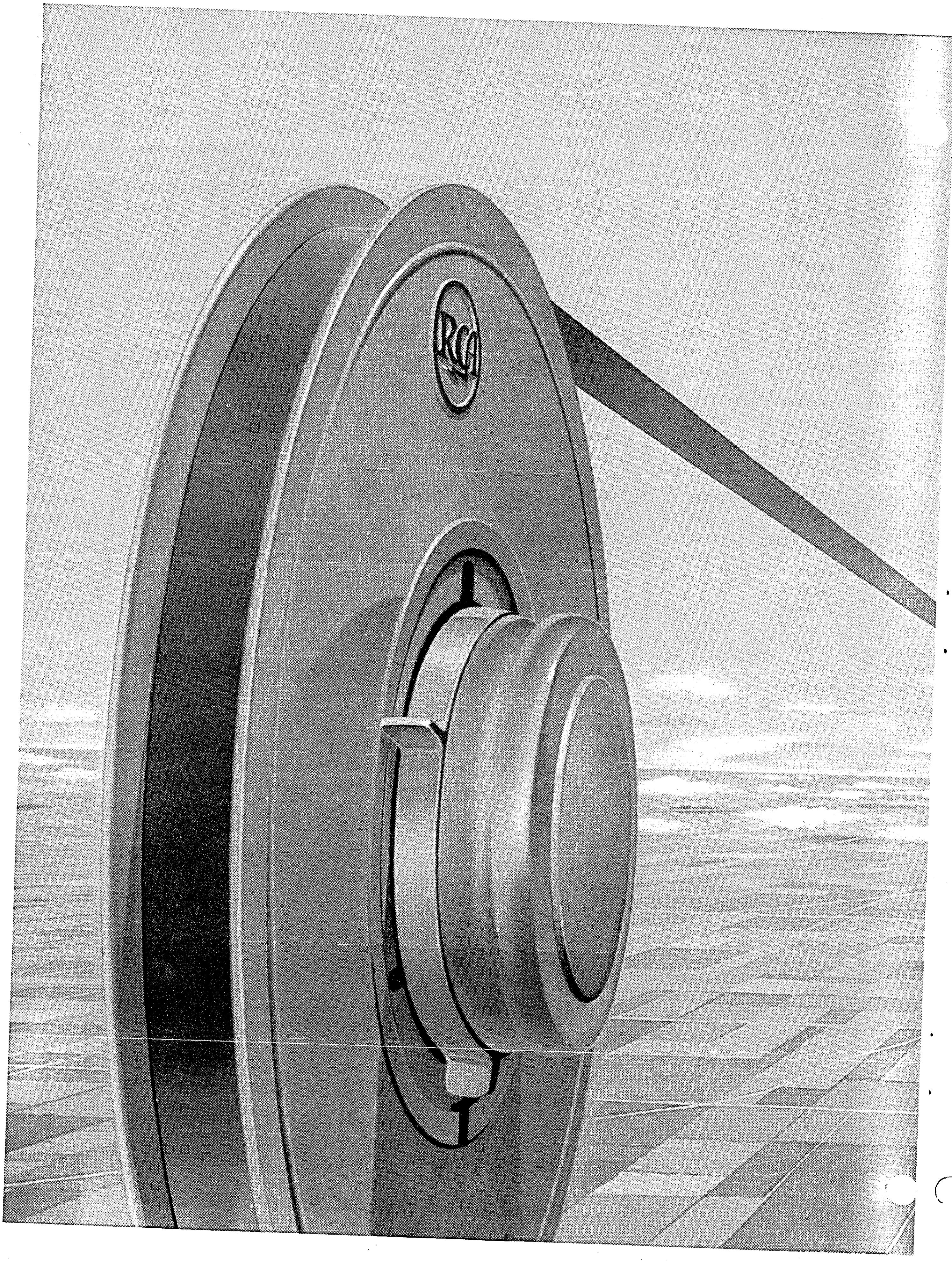
For these reasons, Burroughs Corporation will offer ALGOL in machine implementation with the B5000. The compilation will proceed directly from the ALGOL statement to machine language. By merely comparing internal speeds of the 220 and the B5000, one can come to the conservative conclusion that the B5000 may compile at rates comparable to 4000 to 5000 single address instructions per minute.

The B5000 is designed to provide effective processing of the object code types produced by automatic programming systems, and the ALGOL programming system is encoded in its own language. Its machine language representation has the object code characteristics of other codes translated by this system.

Thus, in comparing existing ALGOL implementation to FORTRAN, the balance is again in favor of ALGOL. It would seem that Mr. Bemer is correct, and that ALGOL is, indeed, "... a far superior language to any of its predecessors." ■

NOTES

1. McCracken, Daniel D., "A Guide to FORTRAN Programming," John Wiley & Sons, Inc., New York, 1961.
2. Bemer, R. W., "Survey of Modern Programming Techniques," *The Computer Bulletin,* March, 1961 The British Computer Society.


RCA

NORTH ELECTRIC

VISIONEERING ACHIEVEMENT
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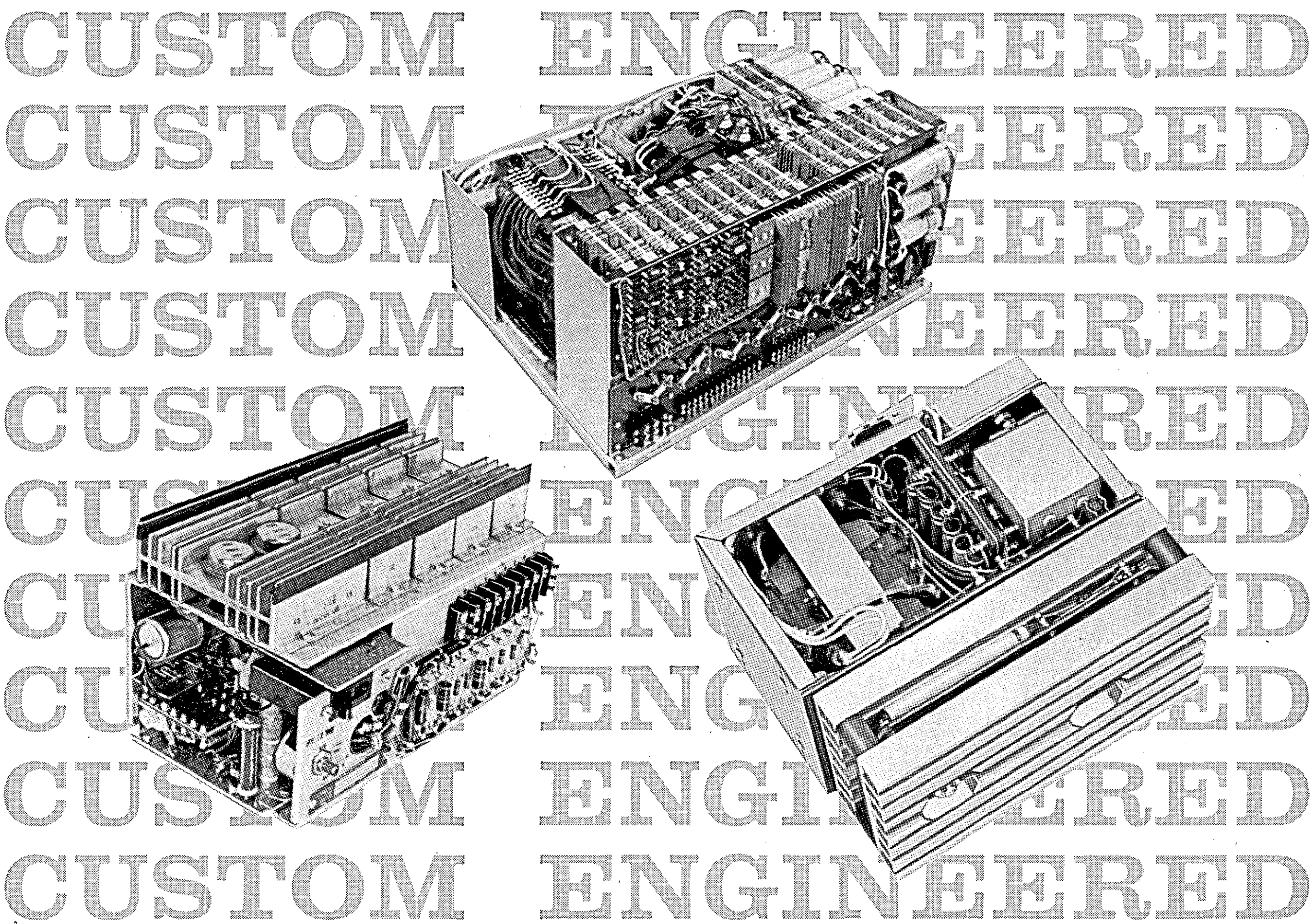

POWER SUPPLY SYSTEMS

...an expression of basic philosophy at Power Equipment Company

Leading manufacturers of computer, communications and automatic control systems have discovered it is more economical to order reliable PECO power supplies custom engineered to their rigid requirements than to modify off-the-shelf catalog units.

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PECO development, prototype and production facilities since 1935 have been devoted exclusively to the manufacture of power supplies for commercial, industrial and military systems applications. Today, PECO is the largest custom manufacturer of power supplies in the country.

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NORTH ELECTRIC
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CIRCLE 42 ON READER CARD

BOOK capsules

INFORMATION PROCESSING LANGUAGE-V MANUAL, edited by Allen Newell, 1961, The RAND Corp., dist. by Prentice-Hall, Inc., Englewood Cliffs, N. J., 244 pp., $6.00.

This manual sets forth the principles of heuristic programming and the simulation of cognitive processes, which led to the development of IPL-V. Divided into two sections, the first presents an introduction and a simplified description of the language, while the second enumerates the complete rules for coding in IPL-V. Both sections were originally RAND Corp. papers.

PRINCIPLES OF NEURODYNAMICS: Perceptrons and the Theory of Brain Mechanisms, by Frank Rosenblatt, 1962, Spartan Books, 6411 Chillum Place N.W., Washington 12, D. C., 636 pp., $6.50.

This work was originally published as a technical report for distribution by the Information Systems Branch of the Office of Naval Research and Cornell Aeronautical Laboratory, Inc. The report sets forth the principles, motivation, and accomplishments of Perceptron Theory in their entirety. It also provides a self-sufficient text for those interested in a serious study of neuro-dynamics.

PROGRAMMING AND CODING FOR AUTOMATIC DIGITAL COMPUTERS, by George W. Evans, II, and Clay L. Perry, 1961, McGraw-Hill Book Co., Inc., 330 W. 42nd St., New York 36, N. Y., 250 pp., $9.50.

This volume describes the techniques and methods for efficient programming. In a step-by-step format, the text develops logically the computer's instructions, and how to utilize programming and coding techniques. Topics include Boolean algebra, derivation of numerical representations, flow diagramming, debugging programs, and record-keeping.

ADVANCES IN COMPUTERS, VOLUME 2, edited by Franz L. Alt, 1961, Academic Press Inc., 111 Fifth Avenue, New York 3, N. Y., 434 pp., $14.

This four-part volume encompasses: A Survey of Numerical Methods for Parabolic Differential Equations; Advances in Orthonormalizing Computation; Microelectronics Using Electron-Beam-Activated Machining Techniques; Recent Developments in Linear Programming, and The Theory of Automata, a Survey.

MANAGEMENT GAMES, A NEW TECHNIQUE FOR EXECUTIVE DEVELOPMENT, by Joel M. Kibbee, Clifford J. Craft, and Burt Nanus, 1961, Reinhold Publishing Corp., 430 Park Ave., New York 22, N. Y., 348 pp., $10.

This text surveys aspects of the design and utilization of general business games. Information is included on games programmed for computers, and on developing a game to any situation. Several studies of actual case histories stress problems encountered in building the model, obtaining top management support, integrating simulations into training programs, and evaluating results.

HANDBOOK OF AUTOMATION, COMPUTATION, AND CONTROL, VOLUME 3, edited by Eugene M. Grabbe, Simon Ramo, and Dean E. Wooldridge, 1961, John Wiley & Sons, Inc., 440 Park Ave. S., New York 16, N. Y., 1,128 pp., $19.75.

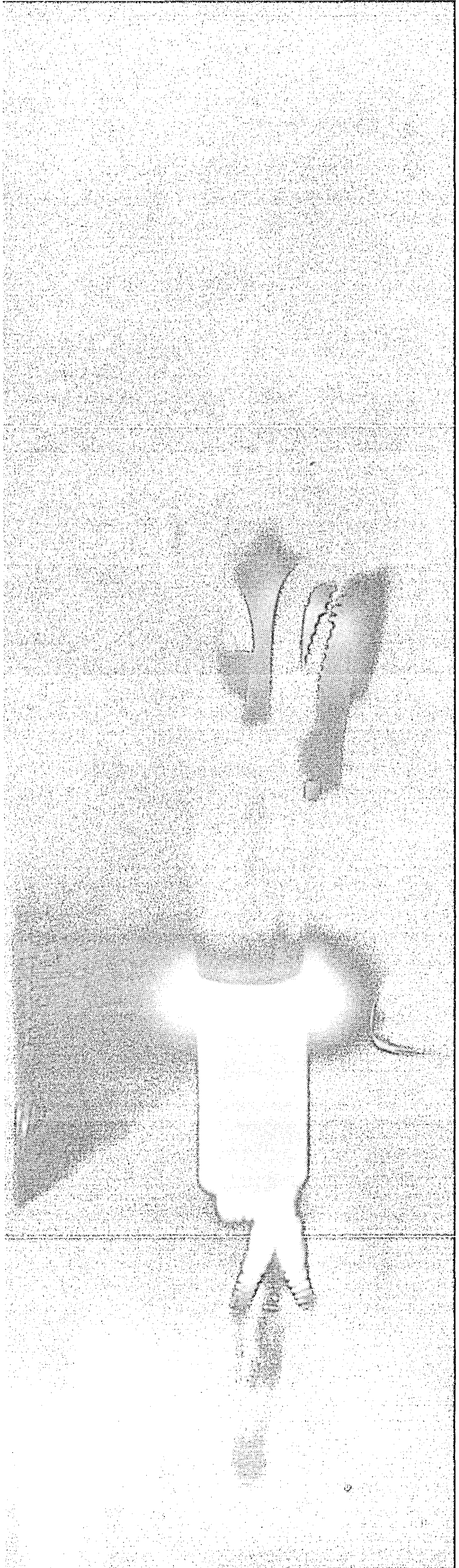
This volume, third in a series on systems engineering, treats engineering design, and presents significant examples of application. Also covered is applied feedback and instrumentation in process control, and stresses theory in presenting basic material on components.

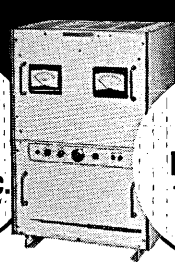
COMPUTER PROGRAMMING HANDBOOK: A GUIDE FOR BEGINNERS, by Robert Nathan and Elizabeth Hanes, 1961, Prentice-Hall, Inc., Englewood Cliffs, N. J., 214 pp., $7.65.

This textbook examines the programming of four different systems, the IBM 650 and 704, Burroughs 220, and UNIVAC 1103A. Each of the four is considered separately so that any one may be studied independently of the others, if desired. Examples, problems, and a summary list of pertinent commands used for each computer are presented at the end of each chapter when appropriate.

AUTOMATIC DATA PROCESSING SEMINAR FOR FEDERAL EXECUTIVES, edited by B. Ralph Stauber, 1961, The Graduate School, U. S. Department of Agriculture, Washington 25, D. C., 240 pp., $4.50.

This collection of papers was originally presented in a series of seminars for government officials. Included are reports on systems equipment, programming, analysis and design, implementation and operation, and the future of dp systems.





large-scale system announced by Honeywell

THE 1800 SERIES

A two microsecond main frame and a floating point unit reported by the manufacturer to be in the nanosecond range comprise Honeywell's 1800 series, designed for large-scale business and scientific applications and announced last month.

The central processor (model 1801) is said to have an internal operating speed of more than 120K three-address ops/sec. The floating point unit (model 1801B) achieves its asserted nanosecond speed when used with the 1801 central processor, and makes extensive use of tunnel diodes in its design.

The 1801, with a basic memory of 8K 48 bit words, rents for $19,150 monthly. Additional memories of up to 32K words rent for $3,200 each, per 8K words. The floating point unit will rent for $4,300 monthly. Sales price for the central processor is $919,200; $153,600 for each additional 8K words. Cost of the floating point unit is $206,400.

Delivery time for Honeywell 1800 series equipment will be 15 months after placement of orders.

1800 series equipment includes parallel processing and automatic error correction and detection. Peripheral devices in use with the Honeywell 800 can also be used with the 1800, it was pointed out.

Additionally, 800 software is compatible with 1800 equipment. Prospective users of 1800 series equipment will be able to check out their programs on Honeywell 800 configurations prior to delivery of the 1800.

The H-800 software package includes FACT, ARGUS, COBOL and FORTRAN. ■

NEW FIRMS
& mergers in DP

■ Informatics, Inc., is a new southern California consulting firm headed by Dr. Walter F. Bauer, formerly of TRW Computers Inc. Other principals in the firm include Werner Frank and Richard Hill, also of TRW.

Informatics will concentrate on programming and systems in data processing specializing in on-line systems and military systems. The firm is a subsidiary of Data Products, Inc. (see below)

CIRCLE 110 ON READER CARD

■ Data Products, Inc., is a new Los Angeles firm specializing in peripheral equipment for edp systems. The firm is headed by Irwin Tomash, formerly of Ampex, and was formed as a subsidiary of Telex, Inc. Data Products will offer a disc file and 300-line-a-minute printer as their first step in the development of a more complete product line. Other executives of the company include Raymond Stuart-Williams, Russell C. DuBois, William N. Nozena, Graham Tyson and Byron Smith.

CIRCLE 111 ON READER CARD

■ Digital Science Consultants is a new firm recently established in Encino, California. Lowell D. Amdahl, formerly head of the Military Computer Section, Digital Computer Department, Thompson Ramo-Wooldridge, was named president.

CIRCLE 112 ON READER CARD

■ Automated Procedures Corp., New York City, has acquired Automation Business Machine Service, Los Angeles. The new west coast subsidiary, to be called A.D.P. Sales & Service Corp., was obtained through an exchange of stock. The firm plans to set up or purchase dp centers in San Francisco, Seattle, Dallas, St. Louis, Chicago, Boston and Atlanta during 1962 and 1963.

CIRCLE 113 ON READER CARD

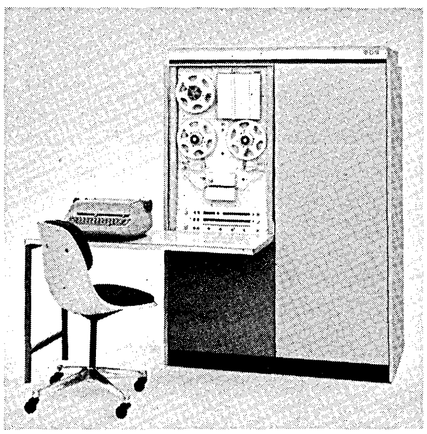
■ Benson-Lehner Corp., Santa Monica, Calif., has formed a Data Services Division. O. E. (Gene) Nemitz, formerly chief of data engineering for Douglas Aircraft's Missile and Space Division, was named to head the new division.

CIRCLE 114 ON READER CARD

A New Generation of Low Cost Computers

SDS 900 Series of high-speed, solid state, general-purpose digital computers are in production. First deliveries will be made in autumn. Designed with the user in mind, they are single address, random access core memory machines, intended for general-purpose scientific computation and special-purpose systems integration. Programming is simplified. Input/output is buffered and high speed. Computation rates are comparable to that of large-scale computers. SDS 900 Series computers are *symbolically homogeneous*—the programs from either machine can be run on the other. They are unusually reliable, with ferrite core memories, all-silicon semiconductors, and circuitry based on worst case analysis. Compare the following characteristics:

$89,000—Model 920



The 920 is an extremely fast, general purpose computer for scientific use. Its command structure includes built-in Floating Point and Multi-Precision instructions. In speed, characteristics, and working flexibility, it surpasses larger, more costly first generation solid state machines. When carefully compared on all of its operating parameters, the 920 clearly offers more general purpose scientific computing-per-dollar than currently available machines.

Memory & Speed The 920's basic core memory of 4,096 words is expandable to 16,384 words. Typical execution times for 24-bit operands, *including both memory access and indexing,* are: Add . . . 16 μsec. Multiply . . . 128 μsec. Floating point operations (24-bit mantissa plus 9-bit exponent) —Add . . . 192 μsec., Multiply . . . 280 μsec.; (39-bit mantissa plus 9-bit exponent)—Add . . . 368 μsec., Multiply . . . 560 μsec.

Standard Equipment All SDS 920 computers are delivered complete with 300 character/second paper tape reader, 60 character/second paper tape punch, input/output typewriter, and manual control and display of all registers. SDS magnetic tape units, converters, and other I/O devices are available as optional equipment.

Common Characteristics

Memory Characteristics

SDS 900 Series computer words contain 24 binary bits. An additional parity bit allows parity checking of all memory and input/output operations. Special logic makes memory non-volatile with power failure.

Input/Output Characteristics

SDS computers incorporate five separate input/output systems. One of these, a buffered input/output, allows data transfer at rates in excess of 120,000 characters/second. A priority interrupt system provides two standard plus 1024 optional channels. In addition to standard input/output devices, all SDS computers communicate directly with: IBM-compatible magnetic tape units, A-D converters, IBM 7090 computers, other SDS machines, and an unlimited range of additional input/output devices.

Programming Characteristics

SDS single address instructions include both an Index Register and an Indirect Address bit. *Programmed Operator* instructions, an exclusive SDS feature, permit complete interchangeability of 910 and 920 programs. FORTRAN II with magnetic tape statements and a symbolic assembler are included in a complete SDS 900 series software package.

Write today for new SDS 900 Series Brochure

SDS
SCIENTIFIC DATA SYSTEMS

1542 FIFTEENTH ST., SANTA MONICA, CALIF.

$41,000—Model 910

The 910 is the first random access, buffered input/output digital computer to be priced below $90,000. Although designed primarily for systems use, its high speed, working flexibility, and excellent performance allow it to be used as an extremely low cost general purpose machine. The 910 operates directly, without special coupling, with all types of input/output devices, including magnetic tape units, A-D converters, automatic typewriters and line printers.

Memory & Speed The 910's basic core memory of 2,048 words is expandable to 16,384 words. Typical execution times for 24-bit operands, *including both memory access and indexing,* are: Add . . . 16 μsec. Multiply . . . 248 μsec. Floating Point operations (24-bit mantissa plus 9-bit exponent) Add . . . 640 μsec., Multiply . . . 656 μsec.; (39-bit mantissa plus 9-bit exponent)—Add . . . 1,984 μsec., Multiply . . . 2,040 μsec.

Standard Equipment All SDS 910 computers are delivered complete with a 300 character/second paper tape reader and manual control and display of all registers. SDS magnetic tape units, converters, 60 character/second paper tape punch, automatic typewriter, and other I/O devices are available as optional equipment.

a special purpose configuration from Bendix

THE G-21

Development of a large-scale special purpose computer system with parallel processing capabilities has been announced by Bendix Computer Division. Designated the G-21, the system is designed for special military control system applications requiring the processing of large amounts of data on an on-line, real-time basis.

A total memory of 81K can be attained through the use of three linked G-20 central processor units, with 57K random access common core memory, plus an additional 8K words of memory reserved for each processor.

Price of a minimum G-21 system is pegged at more than one megabuck, and includes two central processing units, one data communicator, three memory units, one high-speed line printer, and three mag tape units. Approximate delivery date will be 18 months from receipt of order.

Three segments of the same problem or three separate problems may be handled simultaneously with the three central processor unit configuration. Transfer of data between systems will be possible through completely buffered communications lines under the control of independent I/O processors.

Features of the system include an executive control program, with a "fail-safe" provision. If one of the processors should fail, the remaining processors will automatically adjust and hold lower-priority problems until time is available.

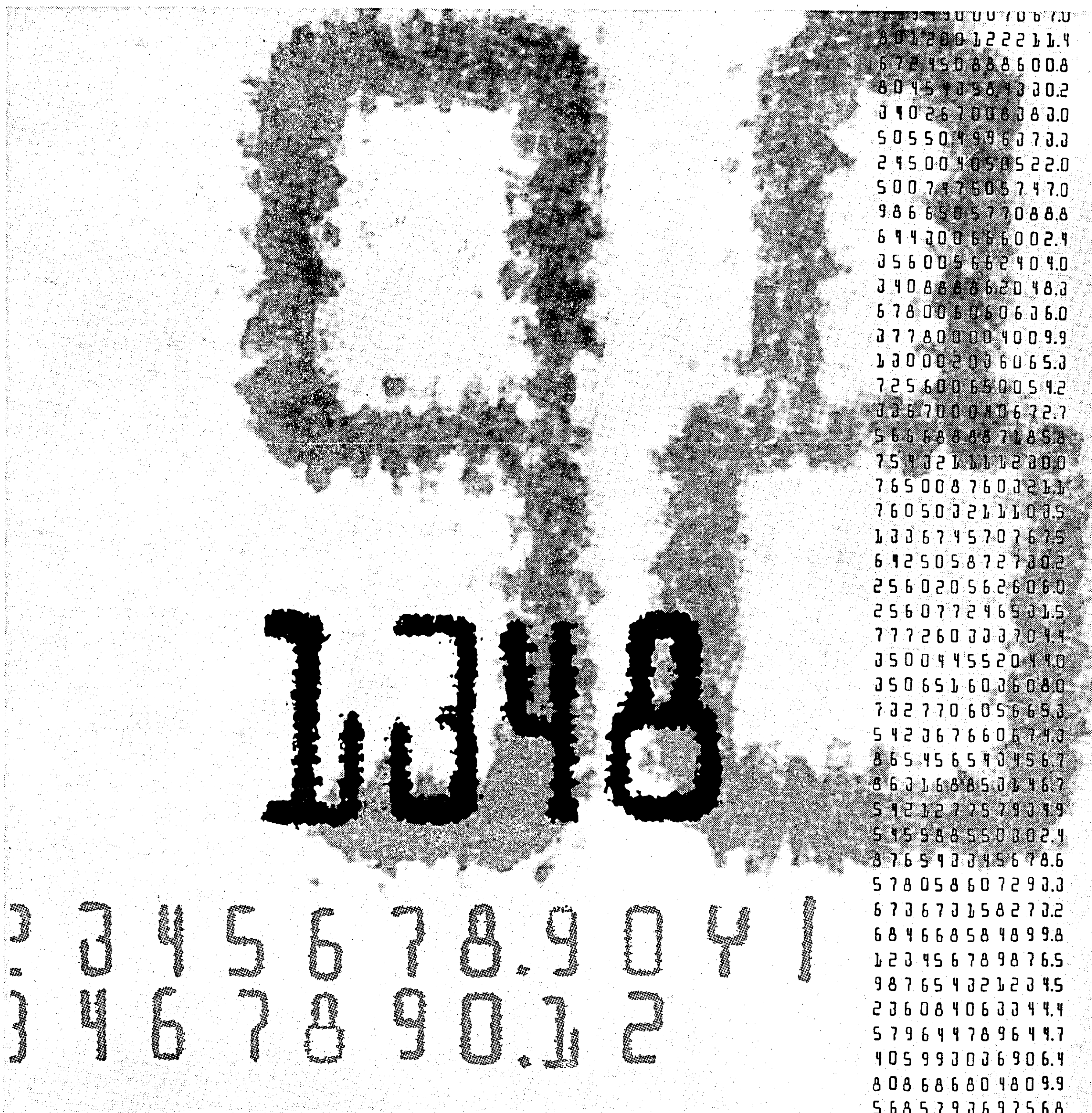
Programming packages for the G-21 will include many of the compilers, assemblers, routines and sub-routines developed for the G-20. Field tests of G-21 components in use at G-20 installations show an availability record of better than 99% of the central processor units.

Also announced recently was the creation of a military computer products group. The group, according to Bendix Computer Division's Charles M. Edwards, will specialize in R & D, production, and sales of special-purpose edp systems.

Robert A. Sweet will direct the marketing effort of the group, and Dr. D. C. Evans will be responsible for military engineering. Reporting to him will be Harvey E. Rennacker, manager of military product development, and V. P. Magnuson, manager, military R & E. ■

NEXT MONTH IN DATAMATION

An on-the-scene report from the Rome conference on symbollic languages will be one of the special features in **Datamation's** May number. Also on tap is a well-timed Grosch inspection of computing outside U.S. environs, and from our tape deck, some frank, on-the-record comments by Honeywell president Walter Finke. Other features will include a leasing survey; a report on traffic control by computer; a statistical round-up of hardware at the university, and a description of exceptional progress in teaching programming at the high school level.



Data processing design problem:

FOOLPROOF FIGURES

Thanks to the figures above, designed by the NCR Electronics Division, computer systems can now read "on sight" the printed output of cash registers and business machines. As a result, data processing systems have a key to greater speed, efficiency and economy.

A unique double code within the figures eliminates the problem of incorrect readings. This code, by making the characters self-checking, also permits important reductions in the cost and complexity of the reading equipment. Even though ink splotches, skew and weak print conspire constantly to "fool" the system, infallible recognition is now possible with relatively simple equipment—at laboratory speeds to 11,000 characters per second!

CAREERS NOW OPEN IN THESE AREAS:

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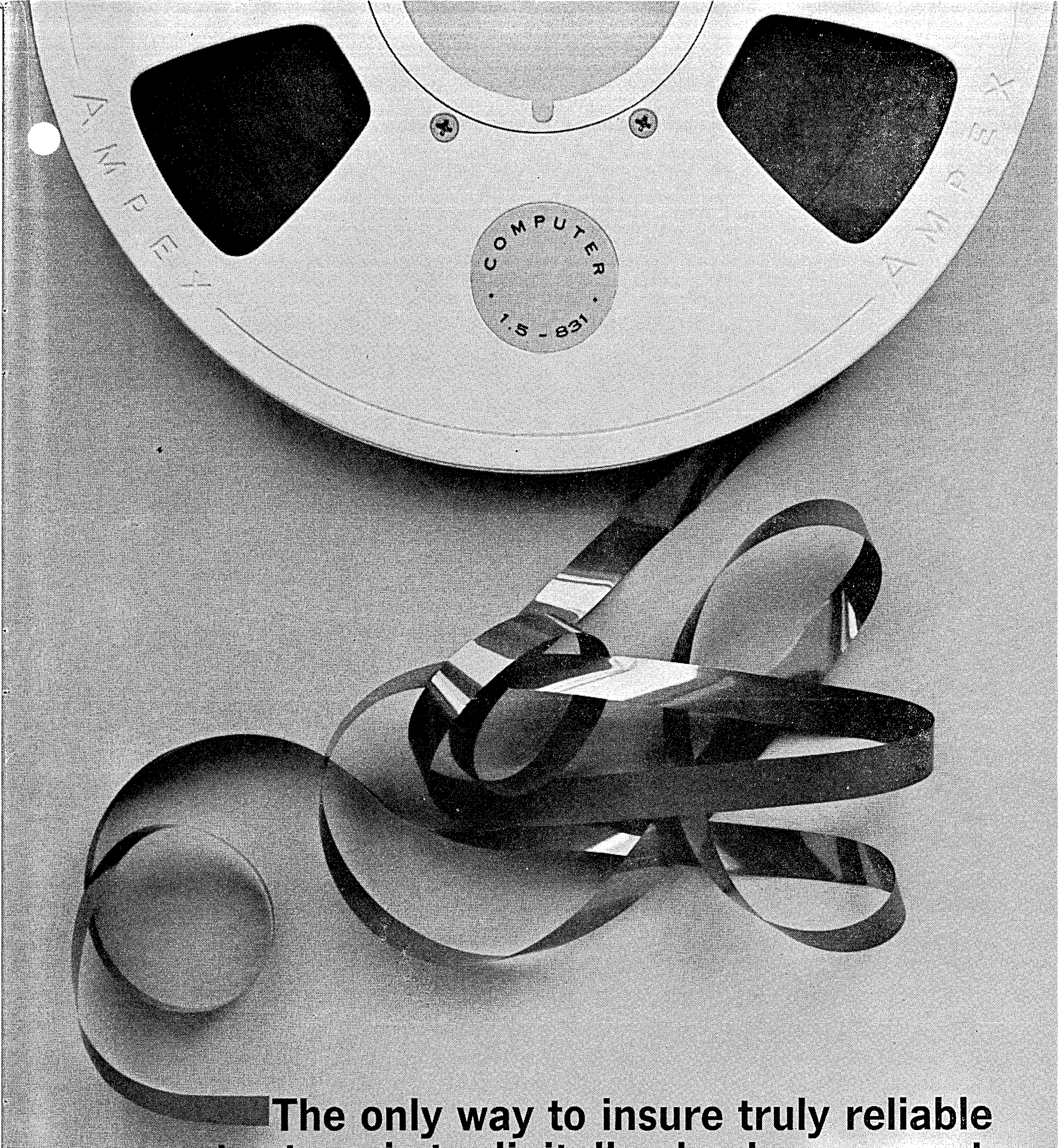
Please send resume to Norval E. Powell, Director of Industrial Relations. Interviews may be arranged for the Spring Joint Computer Conference in San Francisco, May 1-3.

NCR

The National Cash Register Company
ELECTRONICS DIVISION
1401 E. El Segundo Blvd., Hawthorne (Los Angeles), Calif./Phone PL 7-1811

CIRCLE 306 ON READER CARD



The only way to insure truly reliable computer tape is to digitally check <u>every</u> reel.

And Ampex does just that.

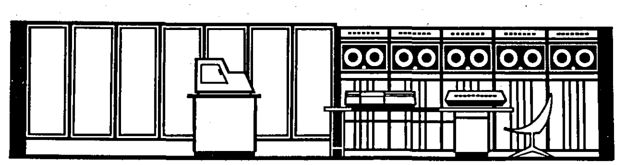
Ampex computer tape performs better. Provides better protection against dropout. The reason: it's truly clean. What do we mean — truly clean? Simply this: Ampex computer tape is completely free of any extraneous material. For it is produced in a controlled atmosphere. Then a special cleaning process removes all matter that might cause even a temporary dropout. Finally, before the tape leaves the plant, it is digitally checked from end to end. Each reel is tested according to the bit packing density at which it will be used by the customer. That way, we are sure it will perform perfectly. What's more, Ampex computer tape stays cleaner, longer. An exclusive Ferro-Sheen process — plus an improved binder system — keeps the surface smooth and thus reduces headwear and oxide build-up. Therefore, your system stays cleaner, too. Ampex computer tape is compatible with leading computer systems. Why not try it in yours? Ampex Corporation, Magnetic Tape Division, 934 Charter Street, Redwood City, California.

AMPEX

CIRCLE 53 ON READER CARD

Meet our new heavyweight

Here's the newest entry in our line-up of computers: the Honeywell 1800 Series. The 1800 is a heavyweight champ from the word go. It has the speed, capacity and capability to handle the very biggest business, scientific or real-time applications. If you're familiar with the Honeywell 400 and 800 computers, you're already aware of many of the advantages of the 1800. Some of these are: Parallel Processing, Orthotronic Control, FACT, vacuum-actuated tape units, control memory, Polyphase and Cascade sort techniques, and COP. This heritage is important. But so are the many new features. Especially if you have a big job in mind. Here, then, are the highlights of the new Honeywell 1800:



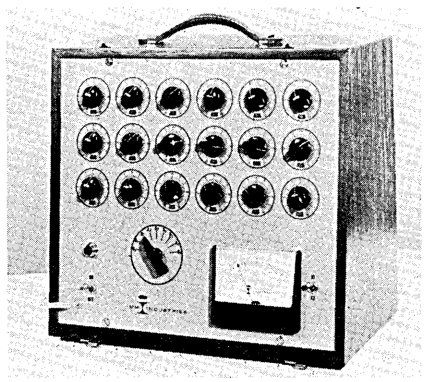

Computape, you never change a bit.
Penelope, you're exactly right. One can't change a bit if one expects to run around with computers all day. That's why I'm guaranteed to deliver *556 or* 800 bits per inch with no dropouts in severest computer applications.

NEW PRODUCTS

card reader and translator
The 401A card reader and 401B translator make it possible to gather information from distant stations directly from punched cards and transmit them via the Data-Phone service to a central data processing area. Up to 51 columns of prepunched information can be read and transmitted from a single card. THE STANDARD REGISTER CO., Dayton 1, Ohio. For information:
CIRCLE 200 ON READER CARD

language converter
This new data processing system was designed to accept both strip chart and microfilm data and to convert this automatically into various digital forms. The system is composed of a data scanner, a microfilm projector, an IBM card punch, a paper tape punch, an automatic typewriter, and a solenoid-operated adding machine, and operates at speeds up to 50 points per minute. RESEARCH CALCULATIONS, 200 Boylston St., Chestnut Hill 67, Mass. For information:
CIRCLE 202 ON READER CARD

fourier analysis computer
A Fourier analysis can be performed on this analog computer in three minutes, giving the DC offset and magnitude of the first, second, third and fourth harmonics of any waveform that can be plotted. IMM INDUSTRIES, SYSTEMS DIV., 14761 Califa, Van Nuys, Calif. For information:
CIRCLE 203 ON READER CARD



card correction
A correction key which is available for the model 24 card punch and the model 26 printing card punch enables keypunch operators to correct most punching errors by ejecting the erroneously punched card reproducing the next card to the exact point where the error occurred. IBM CORP., DP DIV., 112 E. Post Rd., White Plains, N. Y. For information:
CIRCLE 204 ON READER CARD

keyboard converter
This new octal to binary keyboard converter features an entry bar which automatically clears any previously depressed button as the information

NEW PRODUCTS . . .

is entered into the system. The keyboard provides input by octal or decimal pushbuttons and output by binary-coded contact closures. COMPUTER CONTROL CO., INC., 2251 Barry Ave., Los Angeles 64, Calif. For information:

CIRCLE 205 ON READER CARD

tape unit checkout

This tape preparation unit (TPU) has been developed for use with the Polaris missile checkout system and is capable of preparing program tapes for general and special purpose computers, automatic machining equipment, process control systems and production test equipment. The TPU can readout and verify tapes simultaneously, make corrections, modifications, and can change codes by selection of a proper patchboard. CHALCO ENGINEERING CORP., 15126 S. Broadway, Gardena, Calif. For information:

CIRCLE 206 ON READER CARD

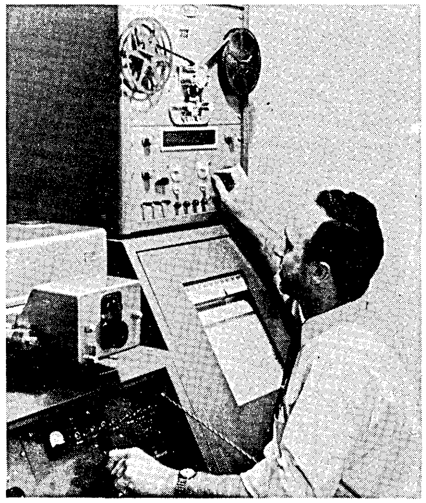
phone line analyzer

The PDA-241 phase distortion analyzer has been designed to aid in the wider use of telephone lines for digital data transmission. Phone lines and other voice communications media can be equalized for transmission of data in less than 15 minutes using the analyzer. In addition, it is compatible with any phase-type or amplitude-type commercial or military transmission system. THE HALLICRAFTERS CO., 4401 W. 5th Ave., Chicago 24, Ill. For information:

CIRCLE 207 ON READER CARD

spectrophotometer

This spectrophotometer computer is a new solid-state analog device which exposes a sample of material to a controlled light beam and yields information on the light transmission



NEW PRODUCTS . . .

and reflection of the sample. The unit takes these readings, compares data with calibration information in magnetic tape memory and produces a curve on a chart recorder. The complete unit sells for approximately $16,000. HOFFMAN ELECTRONICS CORP., 3761 S. Hill St., Los Angeles 7, Calif. For information:
CIRCLE 208 ON READER CARD

computer diode modules

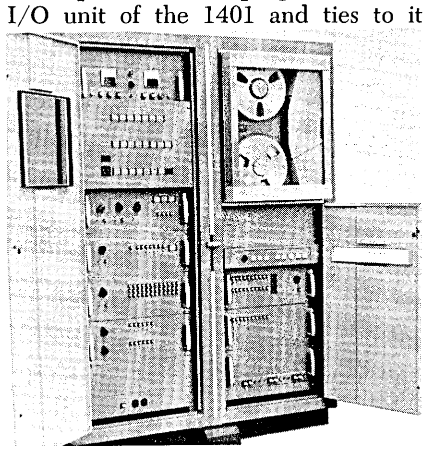
A new line of computer diode modules are available in a variety of circuit configurations and can be supplied using any miniature glass germanium diode and many of the miniature glass silicon diodes. The diode module case features the ability to automatically space itself the proper distance away from the circuit board by means of small spacers molded between the leads. NATIONAL TRANSISTOR MFG., INC., 500 Broadway, Lawrence, Mass. For information:
CIRCLE 209 ON READER CARD

magnetic head

This new high temperature magnetic head for tape recording and reading can be gapped to 40 microinches and remain stable to 200°F. Tests have shown a frequency response differential of ±2 db between outputs at and up to 200°F. with packing densities of 3300 cycles per inch. The head can be used for both digital and analog applications. MAGNE-HEAD DIV., GENERAL INSTRUMENT CORP., 3216 W. El Segundo Blvd., Hawthorne, Calif. For information:
CIRCLE 210 ON READER CARD

tape adapter

The 754 magnetic tape adapter unit provides 1401 users with read/write capability from GE/ERMA or GE 210 to IBM format or vice-versa. The 754 operates as a program control I/O unit of the 1401 and ties to it



in place of one 729 tape unit. The adapter is priced at $85,000. ELECTRONIC ENGINEERING CO. OF CALIF., DP SECTION, Box 58, Santa Ana, Calif. For information:

CIRCLE 211 ON READER CARD

recording computer system

This recording computer system can perform analog computing functions while recording process variables and /or computed values. A rotary pickoff transformer which performs multiplication, square root extraction, division, summing and ratio functions, is the key component of the system. DEVAR KINETICS DIV., CONSOLIDATED ELECTRODYNAMICS CORP., 494 Glenbrook Rd., Glenbrook, Conn. For information:

CIRCLE 212 ON READER CARD

data recording

The DL-210 Local Data Recording Assembly has been designed for applications where central data collection is not feasible. The assembly is comprised of an input station which can receive up to 80 digits of prepunched IBM card data, a control and power supply module, and a paper tape punch. DATEX CORP., P.O. Box 667, Monrovia, Calif. For information:

CIRCLE 213 ON READER CARD

large screen oscilloscope

The model LS 421 large screen sampling oscilloscope provides a full screen of 9"x12" and features a random sampling method which permits the scope to be used as an x-y plotter for events varying at a DC rate or as high as 5 mc. ITT, INDUSTRIAL PRODUCTS DIV., 15191 Bledsoe St., San Fernando, Calif. For information:

CIRCLE 214 ON READER CARD

typewriter transmitter/receiver

The TTR-200 typewriter-transmitter/receiver has been designed for computer I/O, off-line data preparation, communication transmitting and receiving, x-y plotting, inquiry and reply in data processing and information retrieval systems and also can be used as a data logger for process control, data collection and checkout systems. The TTR-200 prints at the rate of 15 characters per second. INVAC CORP., 14 Huron Dr., Natick, Mass. For information:

CIRCLE 215 ON READER CARD

plug-in modules

Two new digital circuit plug-in modules allow data transmission via cable

over distances to 1000 feet. The transmitter, model DT100, incorporates three independent circuits for simultaneous transmission of three channels of information. The model DR 100 receiver also has three circuits and provides TRUE (set) and FALSE (reset) outputs in addition to an auxiliary reset input. PACKARD BELL COMPUTER, 1905 Armacost Ave., Los Angeles 25, Calif. For information:

CIRCLE 216 ON READER CARD

magnetostrictive delay line

Type 174 is a magnetically-shielded, magnetostrictive delay line which provides a delay length of 10 milliseconds and operates at 655 KC/S pulse repetition rate with return-to-zero. DEL-TIME, INC., 608 Fayette Ave., Mamaroneck, N. Y. For information:

CIRCLE 217 ON READER CARD

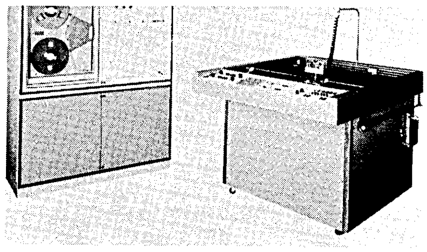
tape terminals

New paper tape terminals for the Dial-o-verter system allows transmission of data at 1,000 words per minute over telephone lines. Terminals feature initial line checking and photo-electric reading and can handle 5, 6, 7, or 8-level tape. Model D507S transmitter rents for $155 per month and model D570R receiver rents for $190 monthly. DIGITRONICS CORP., Albertson, N.Y. For information:

CIRCLE 218 ON READER CARD

automatic plotting

Model 1155B Electroplotter J and Magnetic Tape Converter System provides automatic plotting of points, symbols, digits, and draws line graphs



from digital data recorded on magnetic tape or punched cards. Points can be plotted at rates up to 300 per minute to an accuracy of ±0.05% of full-scale or ±0.015″. BENSON-LEHNER CORP., DATA PRODUCTS DIV., 1860 Franklin St., Santa Monica, Calif. For information:

CIRCLE 219 ON READER CARD

removable panel

A removable panel for TR-10 general purpose analog computers permits problems to be programmed in advance, and allows the operator to keep the computer in almost continuous operation by pre-programming a variety of problems. Upon solution of one, the panel can be removed and another with a different problem installed in its place in less than one minute. ELECTRONIC ASSOC., INC., Long Branch, N.J. For information:

CIRCLE 220 ON READER CARD

3 and 5 amp rated rectifiers

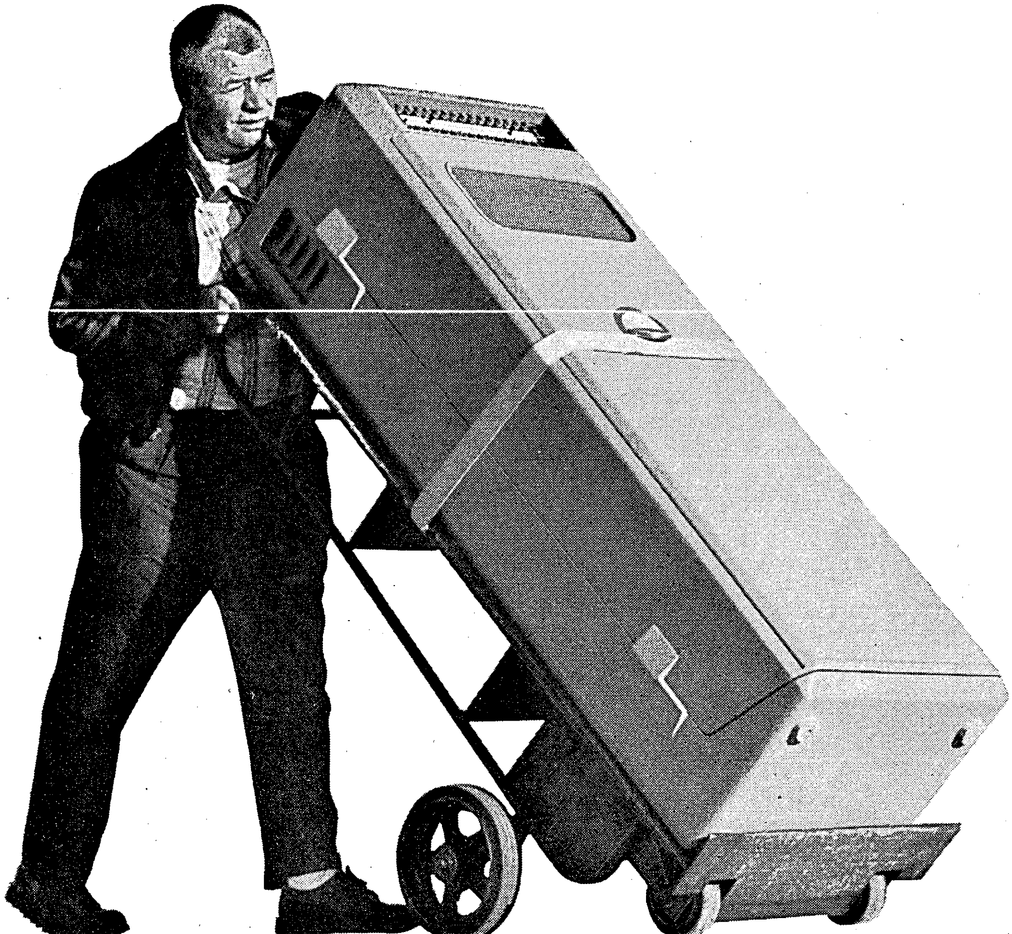
Two new series of silicon controlled rectifiers provide switching on applications such as computer circuitry and servo-mechanisms. Types 3RC5A-3RC40A are three ampere rated, have a PRV range from 25-400 volts. The five ampere rated series are designated 5RC2A-5RC40A. INTERNATIONAL RECTIFIER CORP., 233 Kansas St., El Segundo, Calif. For information:

CIRCLE 221 ON READER CARD

delay lines

The 6053 has been designed to provide a package to accommodate the frequent requirement for magnetostriction delay lines with large numbers of preset taps. FERRANTI ELECTRIC INC., DIV., Industrial Park No. 1, Plainview, Long Island, N. Y. For information:

CIRCLE 222 ON READER CARD



people IN DATAMATION

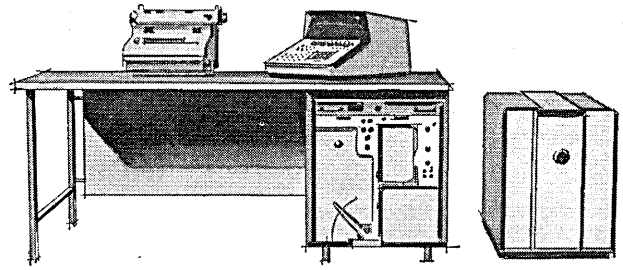
■ At TRW Computers, Dr. Walter F. Bauer, manager of information systems; Richard Hill, head, programming systems and services section, and Werner Frank, head, display application section, resigned last month to form their own company (see New Firms in *Datamation*). Replacing Dr. Bauer will be Randy Porter.

■ Donald T. Spaulding has been named president of IBM's Federal Systems Division in Rockville, Md. Prior to his new appointment, Spaulding was group director of the product line. He will succeed Charles Benton, Jr., who has been promoted to the position of executive assistant to the company's vice president and group executive for the Data Processing and Federal Systems divisions.

■ James A. Cunningham has been appointed Chief of the Computer Technology Section of Data Processing Systems at the National Bureau of Standards, where he will be responsible for the data acquisition system (AMOS IV) and the investigation of semiconductor devices for computer application as well as the design of automatic measuring equipments and data logging devices. Since 1950, Cunningham has been working in digital technology areas of the NBS.

■ Harold L. Leone has joined Computer Science Corp. as a process control specialist. Formerly, Leone was manager of the Applied Programming Operation, Process Computer Section of the General Electric Computer Division in Phoenix, Ariz.

■ Meade C. Camp has been appointed to the new position of manager, Marketing Systems Service, Electronic Data Processing, Radio Corporation of America. He will be responsible for four principal RCA edp activities: methods, training and education, product information, and the RCA Data Systems Center, Cherry Hill, N. J. Prior to his appointment, he was manager, Market Planning, RCA EDP.



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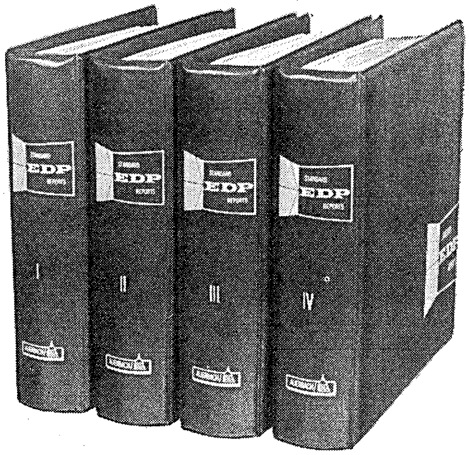

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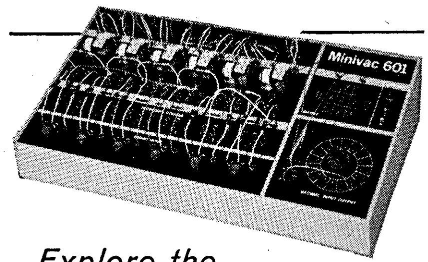

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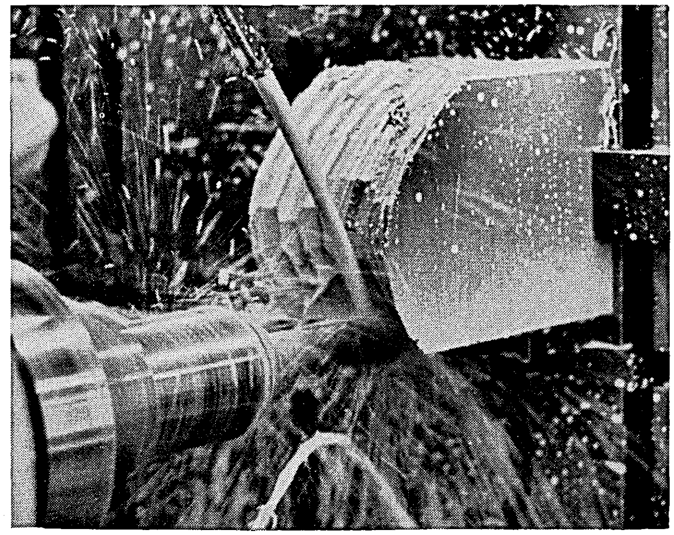
CIRCLE 66 ON READER CARD

IBM asks basic questions in computer software

How much work can computers do?

These IBM programmers are describing a machine part in AUTOPROMT, a programming language developed in cooperation with the United Aircraft Corporation.



Following orders generated by an IBM computer from an AUTOPROMT program, this numerically controlled milling machine is shaping a section of a hyperbolic paraboloid.

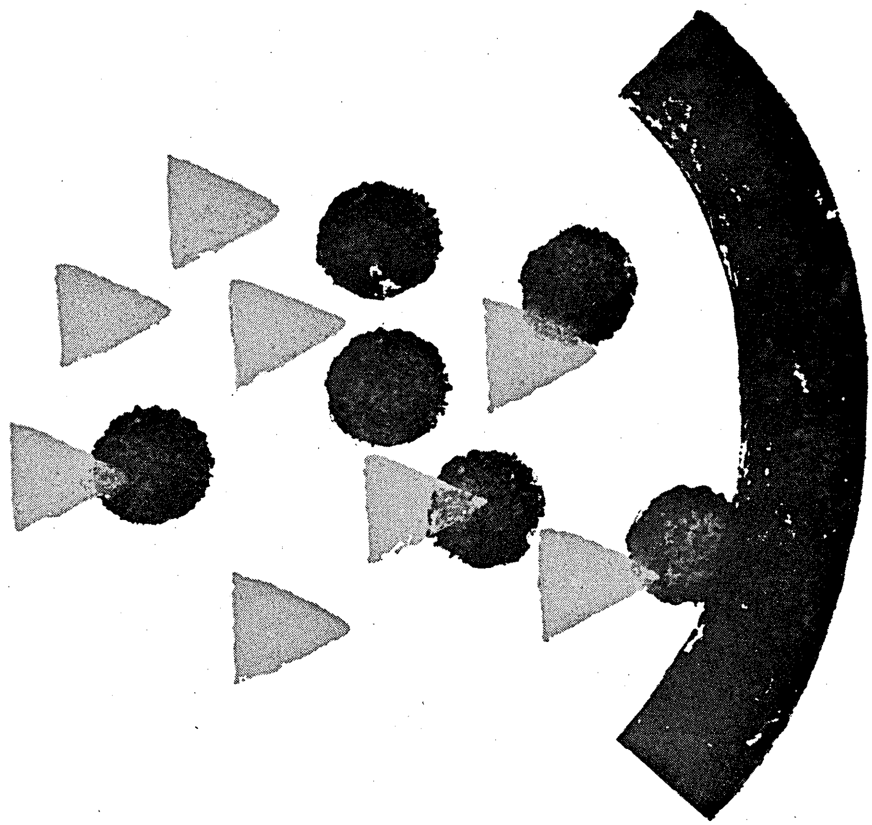
Men use words to symbolize ideas. Computers use a vastly different kind of language. Present computer logic requires instruction in language so rudimentary that each year millions of words of programming are devoted to basically repetitive procedures. Unless ways are found to economize on this instruction, the usefulness of computers may be limited by the shortage of trained personnel to put them to work.

IBM programmers are simplifying communication with computers. Through careful selection and ordering of references to machine structure, they have developed programming systems that transfer a large part of the repetitive work in programming to the computer itself. These systems permit programmers to express their instructions in language resembling English. They also make different machines "look alike" so that programmers can state their problems with as little difficulty as possible. In addition, IBM programmers are experimenting with systems which use the computer's own capacity to construct new programming systems, such as assemblers or compilers.

Programming systems can extend beyond the level of handling machine references automatically to include applications. AUTOPROMT, IBM's system for numerical control of machine tools, is a codification of machine shop language and practice which enables a computer to determine machining instructions from a description of the part's surfaces. The computer generates the sequence of machine tool paths required to produce the part. IBM has also developed information retrieval systems which reduce the burden of indexing, abstracting or disseminating technical information. One experimental system reduces an article to an abstract by statistically determining the most significant sentences in the article.

Eventually, programming systems may grow beyond boundaries of individual disciplines to include general information on the nature of the physical world. Such systems would be supported by information retrieval systems and inference systems capable of seeing logical consequences of retrieved information. They would allow men who direct computers to focus their attention on creative aspects of future problems. By making systems like these possible, IBM programmers and mathematicians are playing a leading role in applying the computer to ever-widening areas of human knowledge.

If you have been searching for an opportunity to make important contributions in software development, manufacturing research, optics, solid state physics, computer systems development or any of the other fields in which IBM scientists and engineers are finding answers to basic questions, please contact us. Write to Manager of Professional Employment, IBM Corp., Department 701Q, 590 Madison Ave., New York 22, New York, IBM is an Equal Opportunity Employer.



Said Michael Faraday: *"The amounts of different substances deposited or dissolved by the same quantity of electricity, are proportional to their chemical equivalent weights."*

Increasing requirements for pure, very thin films—especially those of ferro-magnetic elements and alloys—have become critical. To break this bottleneck, one production method under investigation is a chemical process from an aqueous solution—using metallic salts and a reducing agent.

Scientists at Lockheed Missiles & Space Company have conducted some highly successful experiments, in which extremely pure and thin ferro-magnetic film was deposited on such material as glass and plastics.

Thin film deposition is but one of many phenomena now being investigated at Lockheed Missiles & Space Company in Sunnyvale and Palo Alto, California, on the beautiful San Francisco Peninsula. Engineers and scientists of outstanding talent and ability naturally gravitate to Lockheed. For here they can pursue their special fields of interest in an ideal environment.

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COBOL MANUAL: Describes COBOL programming for the Burroughs B 5000. Defines B 5000 extensions to COBOL such as SORT, MERGE, use of relational symbols, and ADD and SUBTRACT CORRESPONDING. Lists COBOL electives implemented for the B 5000. Includes reserved word lists and sample problem. MGR., SALES TECH. SERVICES, BURROUGHS CORP., 6071 2nd Avenue, Detroit, Michigan. For copy:
CIRCLE 130 ON READER CARD

SPECIAL PURPOSE PROGRAM: Bulletin 1001 describes various computer programs in the fields of aerodynamics, propulsion, acoustics and structural dynamics. GENERAL APPLIED SCIENCE LABORATORIES, Merrick and Stewart Avenues, Westbury, L.I. For copy:
CIRCLE 131 ON READER CARD

COMPUTER DEPT. ACCESSORIES: A 14-page booklet describes reel storage equipment, cabinets, tape reel trucks, chairs, and other accessories for the computer department. Specifications are also listed. WRIGHT LINE, 160 Gold Star Blvd., Worcester 6, Mass. For copy:
CIRCLE 132 ON READER CARD

SILICON MODULES: A 16-page brochure contains description and specs for a new line of all-silicon semiconductor digital logic modules. SCIENTIFIC DATA SYSTEMS, 1542 Fifteenth St., Santa Monica, California. For copy:
CIRCLE 133 ON READER CARD

CONVERSION SERVICE: This four-page brochure gives information on a new computer tape conversion service which converts magnetic computer tapes made on one type of computer to a tape ready for direct input into another machine. A chart on data formats for conversion is included as are discussions on conversion equipment, data checking, conversion time and charges. ELECTRONIC ENGINEERING CO. OF CALIF., Box 58, Santa Ana, Calif. For copy:
CIRCLE 134 ON READER CARD

G-21 SYSTEM: This 7-page booklet describes the hardware, programming and applications of the G-21. Reliability factors as well as the philosophy of the G-21 are also included. BENDIX CORP., COMPUTER DIV., 5630 Arbor Vitae St., Los Angeles 45, Calif. For copy:
CIRCLE 135 ON READER CARD

DOCUMENTATION & INFORMATION RETRIEVAL: This selected bibliography lists nearly 100 books, articles, papers

NEW LITERATURE . . .

and special reports on this subject. CENTER FOR DOCUMENTATION & COMMUNICATION RESEARCH, SCHOOL OF LIBRARY SCIENCE, WESTERN RESERVE UNIVERSITY, Cleveland 6, Ohio. For copy:
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PERT PLANNING AND CONTROL: This booklet outlines the basic concepts of the PERT method for planning and controlling business or scientific projects by computer. RCA, 30 Rockefeller Plaza, New York 20, N. Y. For copy:
CIRCLE 137 ON READER CARD

DIGITAL TRANSDUCERS: This pamphlet includes a definition of digital transducers, explains the trend toward digital control, notes how to use transducers and describes them. Appropriate diagrams are also included. DIGINAMICS CORP., 2525 E. Franklin Ave., Minneapolis 6, Minn. For copy:
CIRCLE 138 ON READER CARD

EDP REPORTS: These three booklets highlight a new set of loose-leaf books which comprise the Standard EDP Reports. Subjects covered include computer systems reports, comparison charts, selection procedure reports, directories and special reports. THE BUREAU OF NATIONAL AFFAIRS, INC., 1231 24th St., N. W., Washington 7, D.C. For copy:
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STANDARD REGISTER FORMS: This folder includes six specification sheets prepared from the findings of a series of tests which determined the range of form construction sizes, papers, fasteners, etc. for use with various edp printers. THE STANDARD REGISTER CO., Dayton 1, Ohio. For copy:
CIRCLE 140 ON READER CARD

COMPUTER APPLICATION SERVICES: This brochure outlines typical projects in which this computer application department has participated and outlines its activities and services. GENERAL KINETICS INC., 2611 Shirlington Rd., Arlington 6, Va. For copy:
CIRCLE 141 ON READER CARD

TIME-DIVISION MULTIPLEX: The theory and application of time-division multiplex (TDM) to remote control, supervisory systems, and data transmission is discussed in this pamphlet. MOORE ASSOC., INC., 893 American St., San Carlos, Calif. For copy:
CIRCLE 142 ON READER CARD

DERIVING

majority logic

NETWORKS

FUND THM:

$f(X,Y,Z) \equiv (X\#Y\#f_{x\bar{y}})\#(\bar{X}\#\bar{Y}\#f_{x\bar{y}})\#f_{xy}$

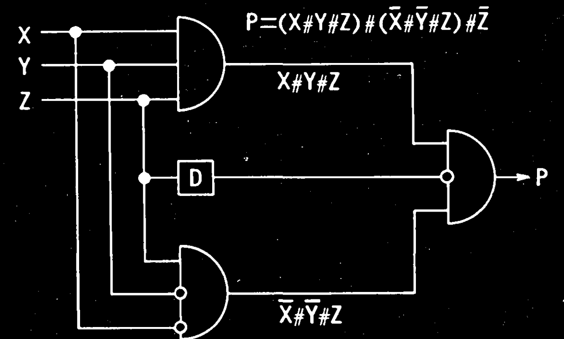
DEFINITIONS:

$X\#Y\#Z \equiv \mathrm{Maj}(X,Y,Z);\ f_{xy} \equiv f(X,X,Z);\ f_{x\bar{y}} \equiv f(X,\bar{X},Z)$

DERIVATION:

Let $f(X,Y,Z)$ be even-parity function P.
Then $f_{xy} \equiv \bar{Z}$ and $f_{x\bar{y}} \equiv Z$ so

$P=(X\#Y\#Z)\#(\bar{X}\#\bar{Y}\#Z)\#\bar{Z}$



The fundamental theorem of majority-decision logic, a typical product of Univac's Mathematics and Logic Research Department, has practical as well as theoretical interest. The even-parity checker derived above from the fundamental theorem can be treed to determine the parity of 3^n bits in $2n$ logic levels using only $\frac{3}{2}(3^n - 1)$ three-input majority gates.

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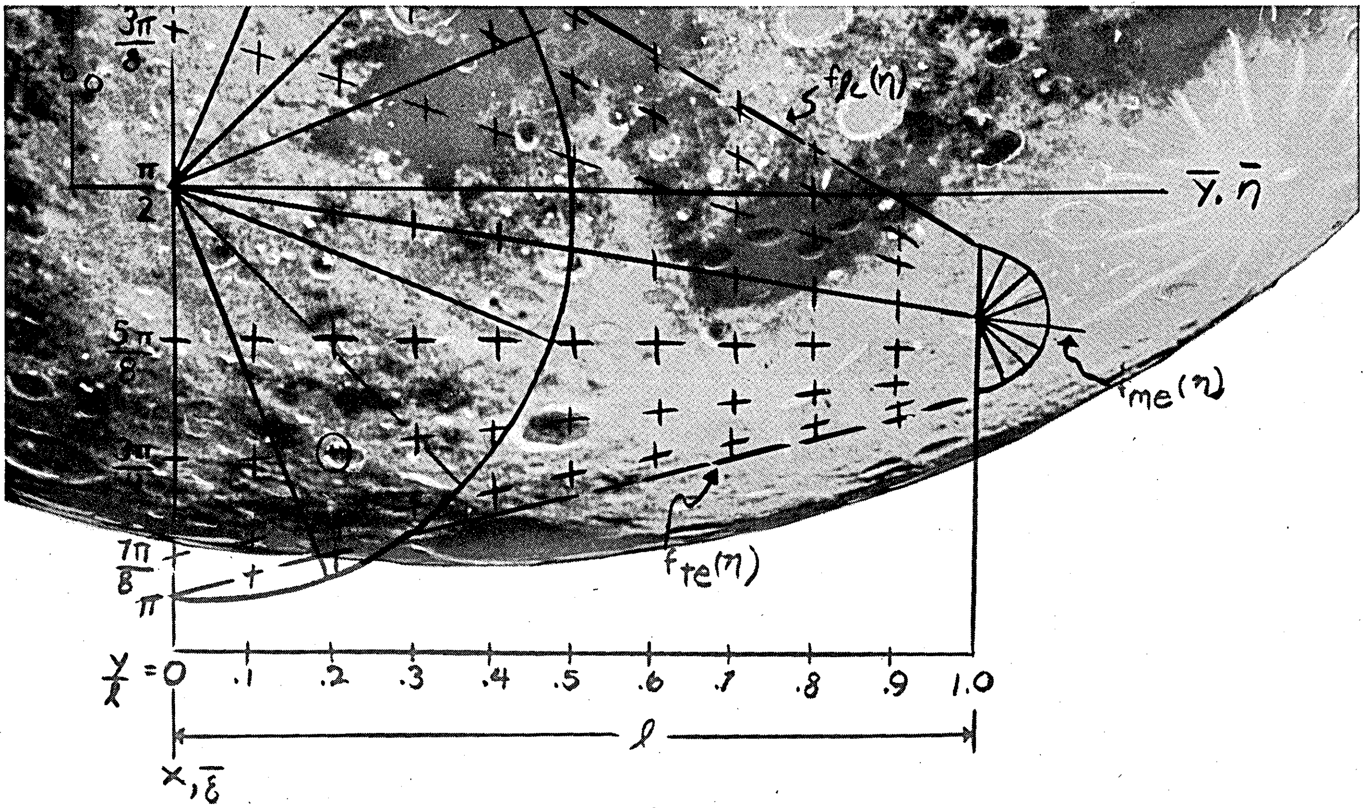

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...Determination of fuel reserve which must be carried aboard a rendezvous vehicle to achieve coplanar orbit.

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...Establishment of continuous flow inventory control systems for all materials and components of specific vehicles.

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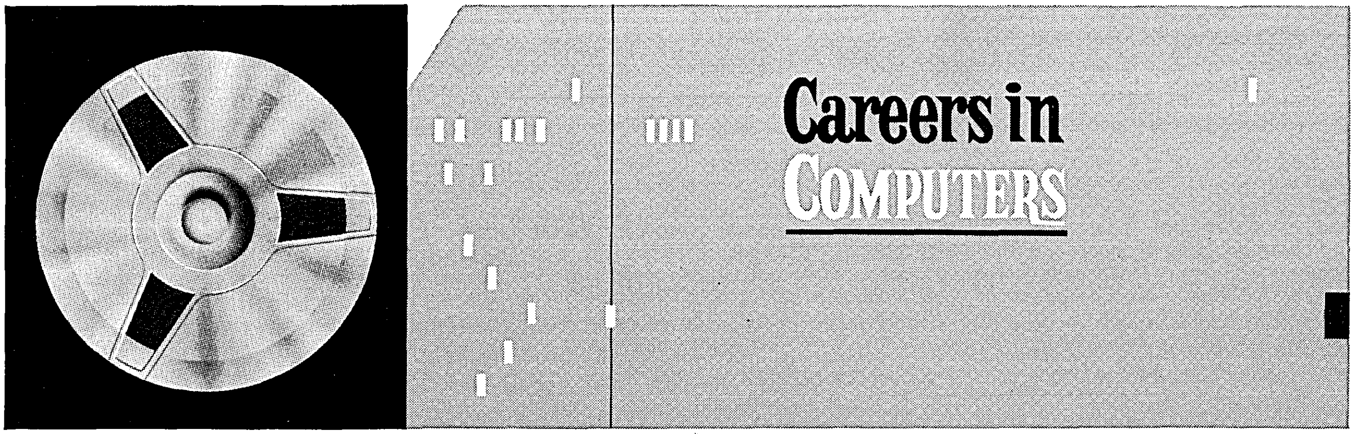

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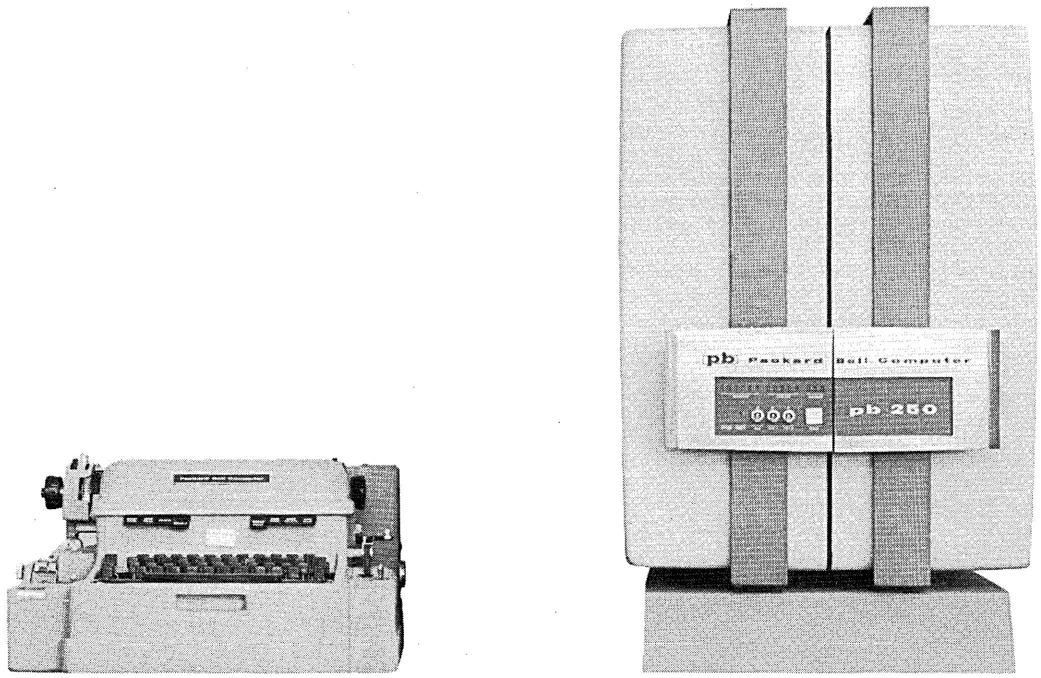

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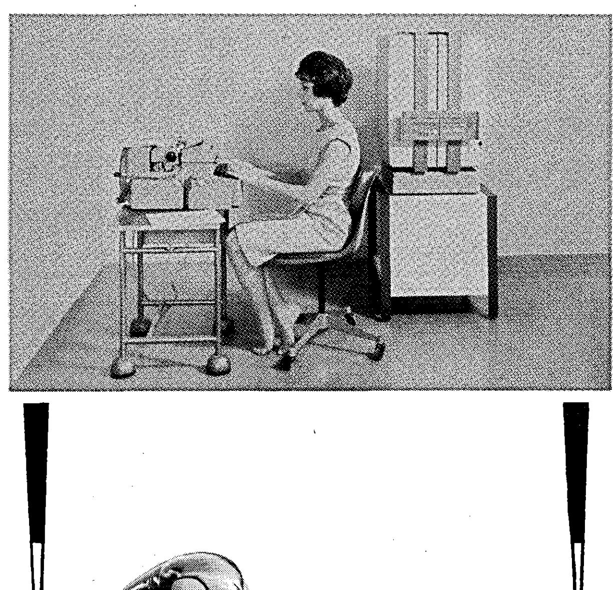

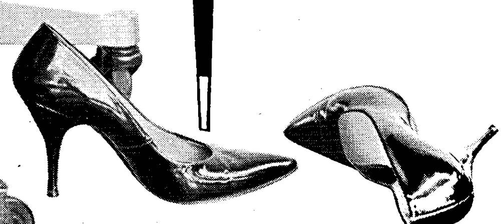

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