

EDN[®]

Low-bias-current op amps	pg 55
Memory cards	pg 67
Capture fast transients with single-shot recorders	pg 121
Feedback models simplify op-amp analysis	pg 139

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



Special Report:
Special-feature SRAMs
unlock CPU capabilities
pg 104

The background image shows a large, circular microchip die with a grid of circuitry. A smaller, square CPU chip is mounted on top of the die. The CPU chip has a circular hole in the center and is labeled 'CPU' and 'STATIC RAM'. The CPU chip is also labeled with the Motorola logo and 'D2266'. The die is shown in a perspective view, with the top edge of the die visible.



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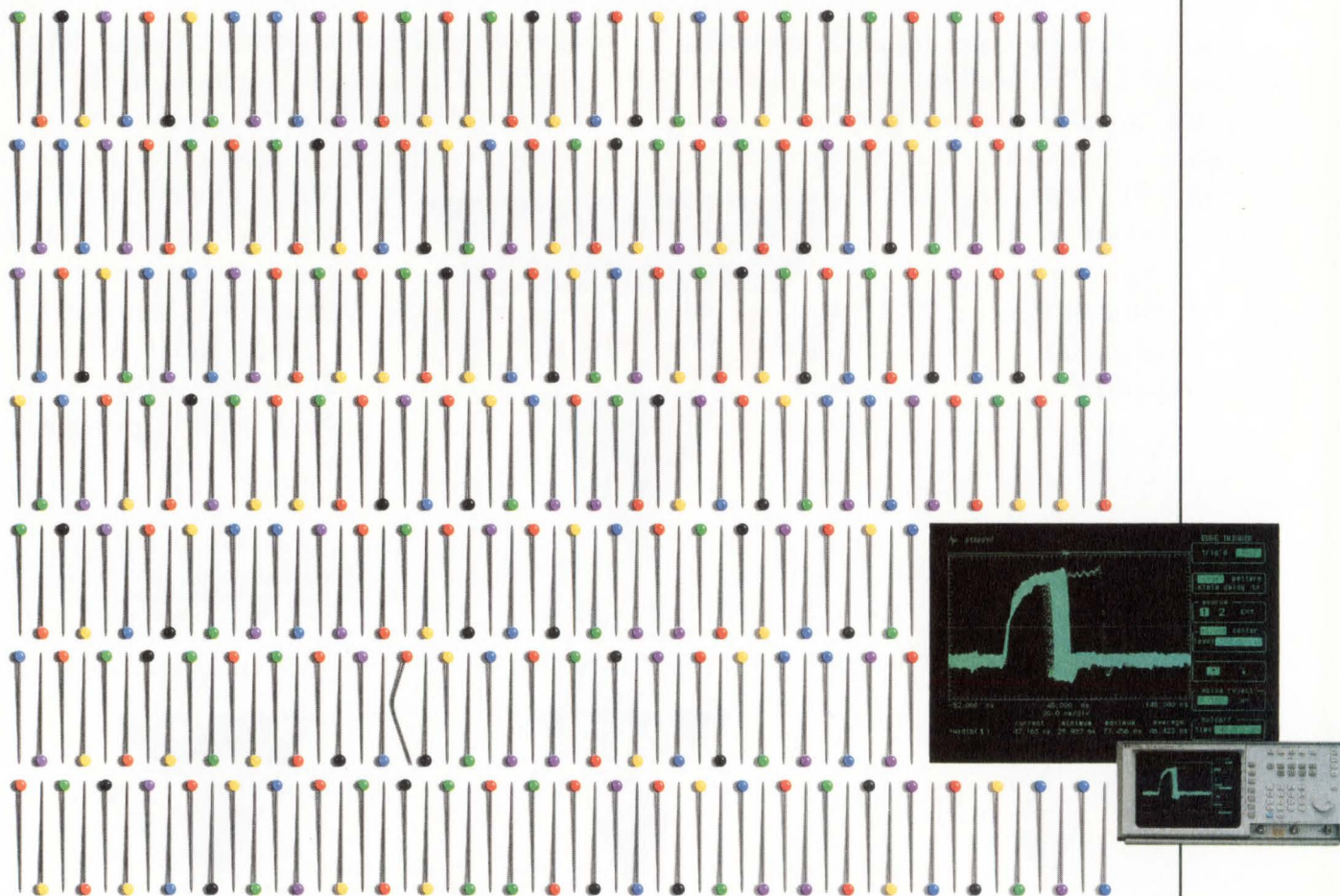
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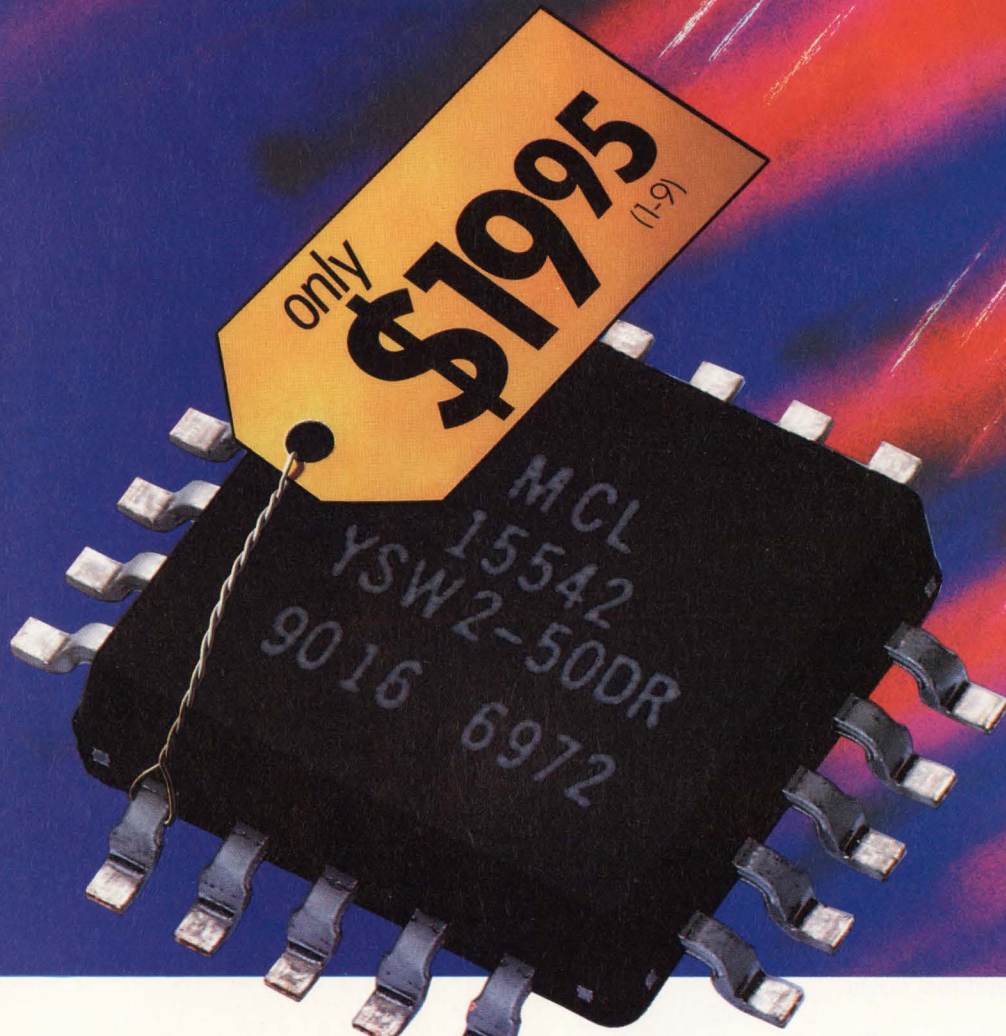
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SPECIFICATIONS

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ZYSW-2-50DR			
Insertion loss, typ (dB)	0.9	1.3	1.4
Isolation, typ (dB)*	50	40	28
1dB compression, typ (dBm @ in port)	20	20	24
RF input, max dBm (no damage)	22	22	26
VSWR (on), typ	_____	1.4	_____
Video breakthrough to RF, typ (mV p-p)	_____	30	_____
Rise/Fall time, max (nsec)	_____	3.0	_____

PRICE YSW-2-50DR \$19.95 (1-9)
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*typ isolation at 5MHz is 80dB and decreases 5dB/octave from 5-1000 MHz

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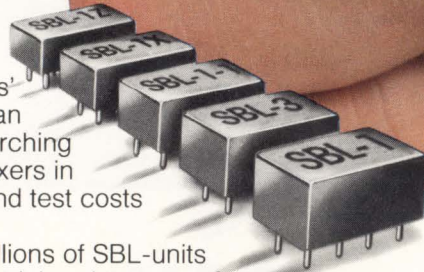
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Model	Frequency (MHz)	Conv. Loss (dB)	Isolation (dB)		LO Level (dBm)	Price, \$ ea. (10 qty)
			L-R	L-I		
SBL-1	1-500	5.5	45	40	+7	4.50
• SBL-1X	10-1000	6.0	40	40	+7	6.25
SBL-1Z	10-1000	6.5	35	25	+7	7.25
SBL-1-1	0.1-400	5.5	35	40	+7	7.25
SBL-3	0.025-200	5.5	45	40	+7	7.25
• SBL-11	5-2000	7.0	35	30	+7	18.75
SBL-1LH	2-500	5.8	68	45	+10	5.50
SBL-1-1LH	0.2-400	5.2	64	52	+10	8.25
• SBL-1XLH	10-1000	6.0	40	55	+10	7.25
SBL-2LH	5-1000	5.9	61	54	+10	8.25
SBL-3LH	0.07-250	4.9	60	53	+10	8.25
• SBL-11LH	5-2000	7.0	45	30	+10	19.75
SBL-1MH	1-500	5.5	45	40	+13	9.80
SBL-1ZMH	2-1100	6.5	40	25	+13	11.70

• IF not DC coupled

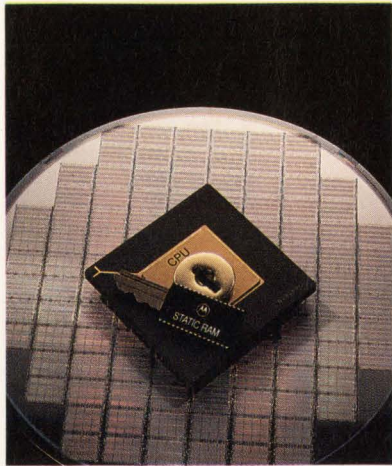
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On the cover: Incorporating glue-logic and system functions on-chip, innovative SRAM architectures hold the key to CPUs' potential speed. See our Special Report on pg 104. (Photo courtesy Motorola)

SPECIAL REPORT

Special-feature SRAMs

104

Each successive SRAM generation must be faster, denser, and wider to keep pace with the latest CPU speeds and architectures. Innovative SRAM architectures are often the means by which memory subsystems stay in the running with today's μ Ps.—*John Gallant, Associate Editor*

DESIGN FEATURES

Build a single-shot recorder to catch fast transients

121

By using an A/D converter with a high input bandwidth and oversampling at a 10:1 ratio, you can digitize and analyze fast transients without using an expensive storage scope.—*Ken Deevy, Dan Sheehan, and Mike Byrne, Analog Devices Inc*

Feedback models reduce op-amp circuits to voltage dividers

139

By extending an op amp's limited feedback model you can create a generalized model that reduces op-amp circuit analysis to determining voltage-divider ratios.—*Jerald Graeme, Burr-Brown Corp*

TECHNOLOGY UPDATES

Low-bias-current op amps: Femtoamperes fuel multifarious functions

55

Op amps with miniscule input bias currents reside in a diversity of measuring instruments. In application, the main problem is channeling all, and only, sensor current to the op amp's input.—*Brian Kerridge, European Editor*

Credit-card-sized memories: Small memories take on broader applications

67

Robust, credit-card-sized memory cards let you carry around—and control access to—a pocketful of nonvolatile data or programs. Backed by new introductions and new standards, these memories may become more popular.—*Charles H Small, Senior Editor*

Continued on page 7

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EDITORS' CHOICE

Compact, fast-sampling, 500-MHz scopes 77

PRODUCT UPDATES

60M-flops, floating-point DSP chip 80
MS Windows math software 84
Data-acquisition software 88

EDITORIAL

CAE-software buyers beware. What you see may not be what you get. 49

NEW PRODUCTS

Integrated Circuits 183
Computers & Peripherals 199
Components & Power Supplies 207
Test & Measurement Instruments 221
CAE & Software Development Tools 238

DEPARTMENTS

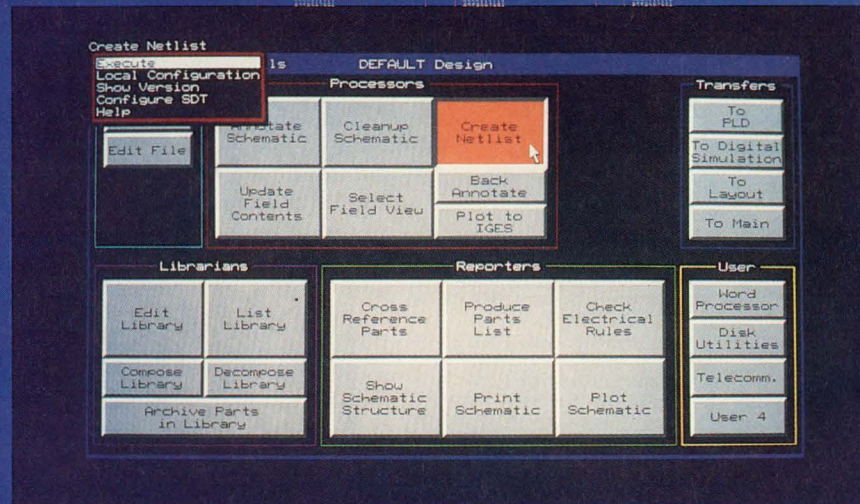
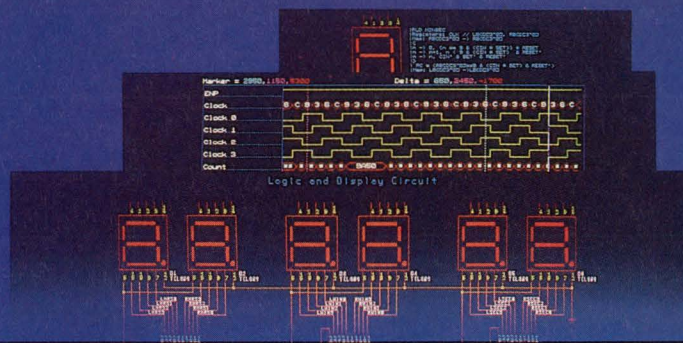
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Signals & Noise 31
Ask EDN 39
Calendar 40
Leadtime Index 98
Design Ideas 161
Literature 245
Career Opportunities 260
Business/Corporate Staff 266
EDN's International Advertisers Index 269

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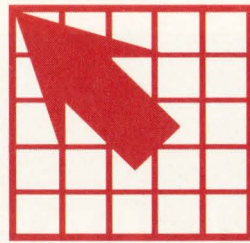
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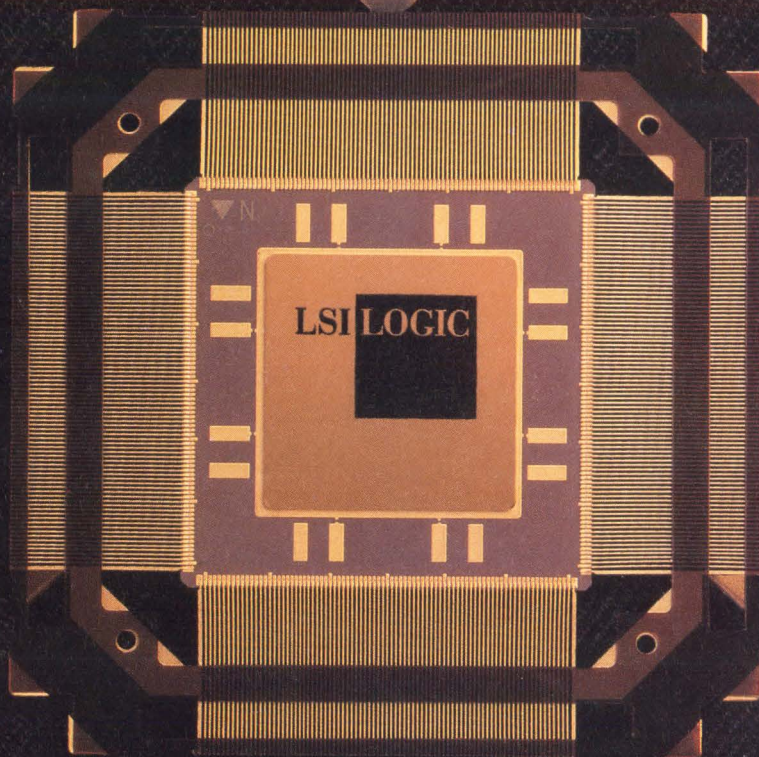
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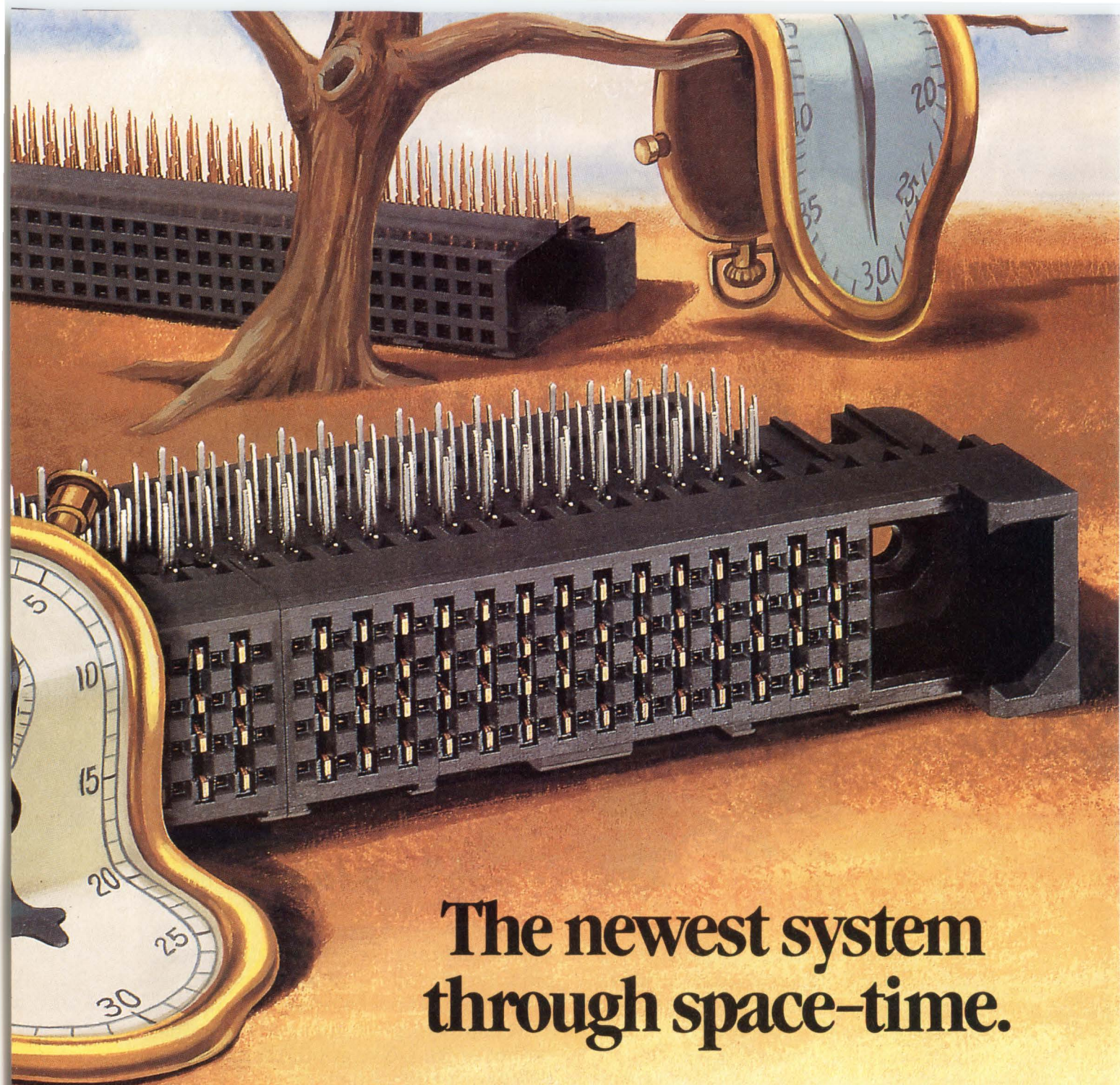
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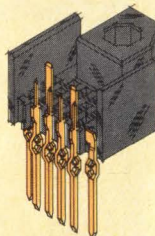
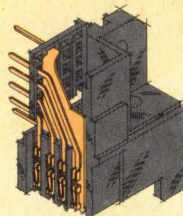
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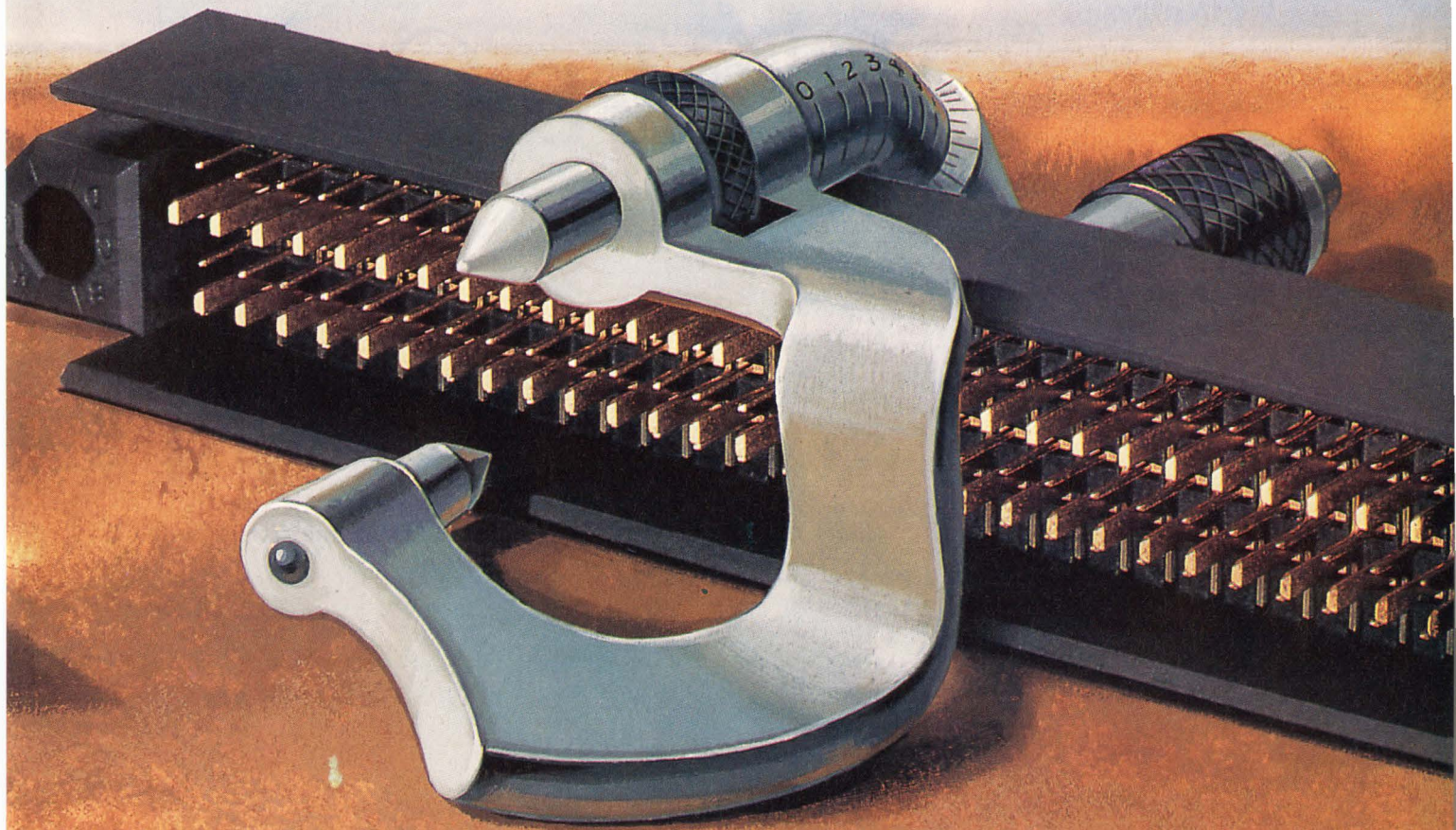
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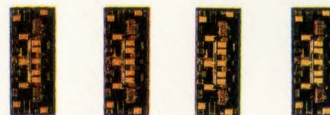
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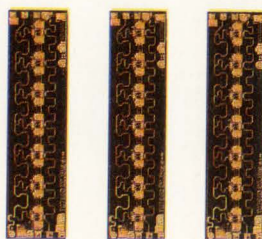
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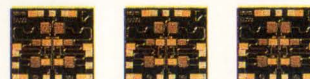
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NEWS BREAKS

EDITED BY SUSAN ROSE

WINDOWS OPENS ON CIRCUIT SIMULATOR, FRAMEWORK CLOSES

Although Microsim's Schematics uses Windows 3.0 on 80x86-based personal computers, the schematic-capture software isn't using Windows as a framework that would let you interface to third-party Spice simulators. Instead, Windows compatibility gives you multitasking capability and a familiar look and feel. The schematic-capture tool is coupled only to the vendor's PSpice simulator and Probe output analyzer/viewer (although both run in Windows, neither PSpice or Probe is a Windows 3.0 application, yet). This coupling lets you run simulations from within the schematic application—the software automatically calls a netlister to generate your Spice input file before the simulation starts. The schematic-capture program includes libraries containing more than 5000 analog and digital parts models. Features such as auto-incrementing of names and labels, auto-step and repeat, an electrical-rule checker, and a symbol editor are also part of the schematics package. The software also runs on Sun workstations as an Openwindows application. Through September, the software costs \$1250 for an IBM-PC and \$4150 for a SPARCstation. Microsim Corp, Irvine, CA, (800) 245-3022, FAX (714) 455-0554.—Michael C Markowitz

3V CMOS STANDARD-CELL LIBRARY CONSERVES BATTERY POWER

The 3V operation of AT&T Microelectronic's 0.9- μ m CMOS library reduces power, heat, and packaging costs. The library includes basic cells, memory elements, and high-level macrocells. The memory-cell list includes synchronous and asynchronous static RAM, a register file, a dynamic shift register, and ROM and FIFO memory. The following high-level macros are also available: DMA controller, UART, 8-bit microcontroller, programmable timer, interrupt controller, memory mapper, and real-time clock. A major tradeoff in moving to a lower-voltage library is lower transistor gain, which slows switching speeds. The library includes higher-power cells to use in speed-critical paths. You can develop ASICs with this library using the company's own Unix-based design tools. By the third quarter of 1991, you'll also be able to use tools from other major CAD vendors, including Cadence Design Systems (San Jose, CA), Synopsys (Mountain View, CA), Mentor Graphics (Beaverton, OR), and Viewlogic (Marlboro, MA). AT&T Microelectronics, Allentown, PA, (800) 372-2447 ext 804; in Canada, (800) 553-2448 ext 804, FAX (215) 778-4106.—Anne Watson Swager

SEMICUSTOM, SINGLE-BOARD COMPUTERS OFFER FLEXIBILITY

Ziatech's Application-Specific Automation Processor is an option if you can't find the right off-the-shelf single-board computer (SBC) for your embedded control application. You can select among a list of core modules, peripheral I/O modules, and custom I/O modules for the board, instead of investing the time and money to develop a custom SBC. Because 90% of the board comprises modules from previously tested and proven designs, the risk associated with a new design is minimized. The board is designed around the STD Bus form factor and uses a 16-MHz NEC V53 μ P for 80286 performance and code compatibility. You select the RAM, PROM, Flash EPROM, counters, timers, DMA channels, peripheral I/O modules, and other features you'll need. The initial contract for development and delivery of 25 boards is \$45,000. Delivery is 12 weeks, but prototyping cards let you begin software development before you have the first boards. The semicustom product is aimed at users requiring a minimum of 500 SBCs per year. Typical costs are \$500 to \$800 per board. Ziatech Corp, San Luis Obispo, CA, (805) 541-0488, FAX (805) 541-5088.—Doug Conner

NEWS BREAKS

FLAT-TENSION MASK TECHNOLOGY ADVANCES TO 17-IN. CRTS

Zenith Electronics Corp demonstrated 17-in. and 20-in. prototype versions of its flat-tension mask (FTM) CRT at the Society for Information Display Symposium held last month in Anaheim, CA. The 17-in. display was not just larger than the company's existing 15-in. FTM CRT display; the new display adds multifrequency operation and better maximum resolution—1024×768 pixels. The 17-in. tube retains the flat screen inherent with FTM technology. Other FTM CRT advantages include the lack of purity loss caused by electron-beam heating of the shadow mask; added ruggedness because the shadow-mask supports are bonded directly to the CRT's faceplate; better luminous efficiency because the shadow mask and screen are more precisely aligned; and greatly diminished glare because of the antireflection coating on the front of the CRT's flat face and the antiglare treatment applied to the screen's inner surface.

The company plans to ship production versions of the 17-in. display to OEM customers in November. Evaluation units will be available by early autumn. The company expects the retail price for multifrequency, 17-in. FTM CRTs to start below \$2000. In addition, you can order custom single-frequency versions with resolutions to 1280×1024 pixels for workstation applications. The company does not sell the displays directly to end users. Zenith Electronics Corp, Glenview, IL, (708) 391-8181, FAX (708) 391-7253.—Steven H Leibson

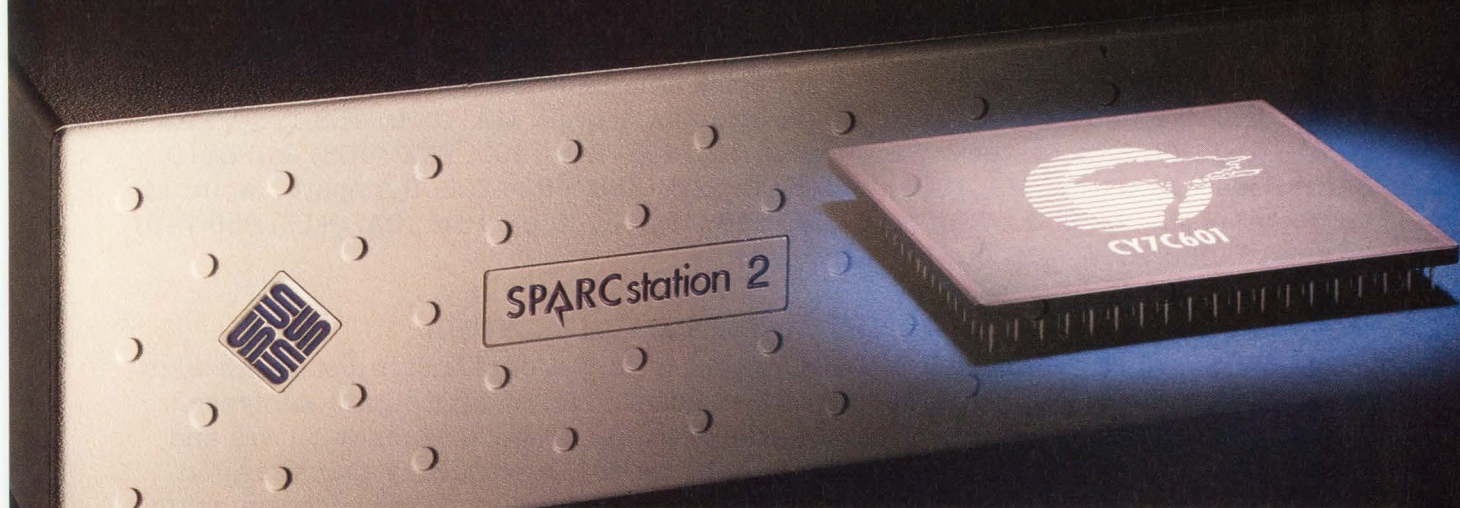
COMPUTING HARDWARE SHUNS VON NEUMANN

The CHS2×4 from Algotronix is an application-specific computer that operates by configuring hardware to a computational task. An IBM PC or compatible plug-in card houses the computer, and data flows via the IBM PC/AT bus or a rear panel I/O connector. You can program the computer to make dedicated datapaths, or map algorithms directly into the hardware. The technique relies upon the company's CAL1024 32×32-cell, CMOS field-programmable gate array (FPGA). Using on-chip static RAM (SRAM), you can program each cell of the FPGA to behave as any function of two boolean variables, or as a D-type latch with a 100-MHz toggle rate. You can program a 32×32 array in 70 μsec. Each computer employs nine FPGAs; eight form an array of 64×128 cells, and one performs house-keeping tasks. The computer also contains 2M bytes of SRAM for local data storage in pipelined computations. You can connect two of the computers to expand their array 128×128 cells, with 4M bytes of SRAM. Software support includes a symbolic editor for design work, an assembler and loader for array programming, and a C library for support functions including dynamic reconfiguration. The £4900 evaluation kit available now includes the IBM PC plug-in card and software. Algotronix Ltd, Edinburgh, UK, (31) 668-1550, FAX (31) 662-4678.—Brian Kerridge

NONVOLATILE STATIC RAM OFFERS 35-NSEC ACCESS

Benchmark Microelectronics's 32k×8-bit battery-backed nonvolatile static RAM (SRAM) has a 35-nsec access time. Two versions are available: The bq4011H has a 5% power-supply tolerance and the bq4011HY has a 10% tolerance. Both devices come in 600-mil DIP modules that are socket-compatible with standard SRAM, EPROM, and EEPROM memories. The modules include the SRAM, power monitoring and control circuitry, and a lithium battery. The modules are UL recognized. The devices cost \$60.30 (100) for the 35-nsec version; \$53.10 for a 45-nsec version. Benchmark Microelectronics Inc, Carrollton, TX, (214) 407-0011, FAX (214) 407-9845, contact John Landau.—Richard A Quinnell

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NEWS BREAKS

VHDL AND HARDWARE-ACCELERATOR MARRIAGES EASE USE

Coming on the heels of Cadence Design System's entry in the hardware accelerator business with its XLP simulation accelerator (EDN, May 23, 1991), rival accelerator producers Ikos Systems and Zycad have teamed up with Racal-Redac and Synopsys, respectively, to make their hardware tools easier to use.

Ikos Systems will deliver a VHDL hardware accelerator before the end of the year. Since hardware accelerators can only accelerate structural (gate-level) simulations, the hardware will rely on Racal-Redac's Silcsyn logic-synthesis software to generate a structural representation from your behavioral description. Nonsynthesizable parts of your description must run in a software simulator that the company is developing, but hasn't yet announced. The claimed capacity of the \$59,500 hardware accelerator exceeds 100,000 lines of synthesizable VHDL source.

Synopsys and Zycad have teamed up to integrate the former's \$24,000 VHDL simulation tools—acquired from Zycad last year—with the latter's XP fault and logic accelerators (from \$55,000). The tools don't perform any logic synthesis, but partition your behavioral models into the software simulator and structural models into the hardware simulator. Cadence Design Systems, Lowell, MA, (508) 458-1900, FAX (508) 441-1109. Ikos Systems, Sunnyvale, CA, (408) 245-1900, FAX (408) 245-6219. Racal-Redac, Littleton, MA, (508) 692-4900, FAX (508) 692-4725. Synopsys, Mountain View, CA, (415) 962-5000, FAX (415) 965-8637. Zycad, Menlo Park, CA, (415) 688-7451, FAX (415) 688-7550.—Michael C Markowitz

USE YOUR MAC AS A LOW-COST SPECTRUM ANALYZER

The \$495 Audio-Frequency Fourier Analyzer from National Instruments can turn your Apple Macintosh II computer into a 2-channel, dual-display signal analyzer. You can use the software for measuring the response of low-frequency filters and networks, or to measure the magnitude and phase of low-frequency transmission signals. The software gives you real-time display of the time, power spectrum, magnitude/phase spectrum, correlation function, impulse response, transfer function, and coherence function of incoming signals. At sample rates reaching 48k samples/sec, the program's accuracy specs indicate 426 lines of resolution with a broadband dynamic range of 93 dB and bandwidth from dc to 20 kHz. Frequency accuracy is 0.01% and frequency resolution approaches 0.013 Hz per line. If your Mac lacks the hardware to perform stand-alone signal analysis, you can buy the software bundled with a runtime version of LabView-2, an NB-DSP2300 board, an NB-A2100 board, and a 3-board RTSI cable for \$7495. National Instruments, Austin, TX, (512) 794-0100, FAX (512) 794-8411, contact David Koenig.—J D Mosley

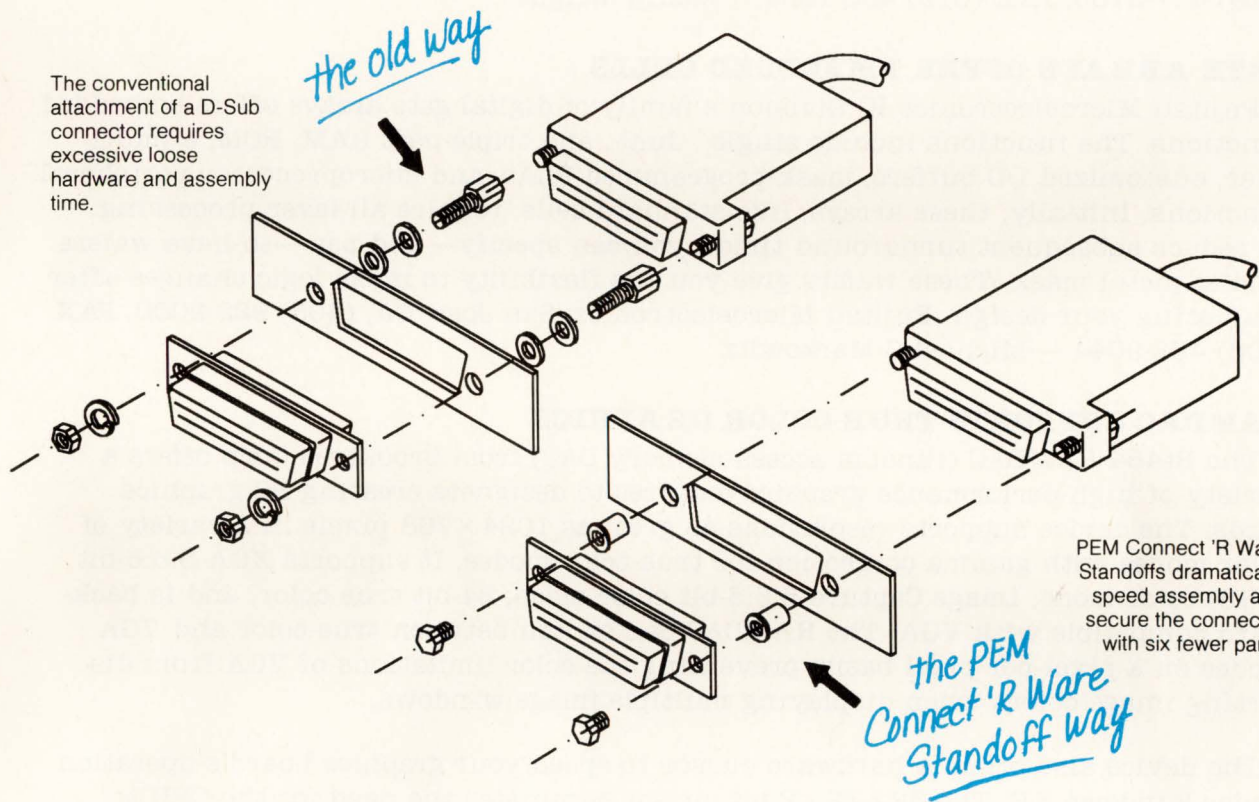
LOW-POWER, 10-BIT ADC SAMPLES AT 40M SAMPLES/SEC

The SPT7814 from Signal Processing Technologies combines a 10-bit ADC with an on-chip track-and-hold circuit, samples at 40M samples/sec, and requires no additional components to operate. At 40 MHz, the device draws 1.3W from its 5V and -5.2V power supplies (a relatively small amount of power for a converter this fast). The device's analog input has an input capacitance of 5 pF, which reduces the drive requirements on front-end circuits. The \$109 (100) converter has ECL outputs. A companion device, the \$79 (100) SPT7810, has similar features but samples at 20M samples/sec max. Signal Processing Technologies, Colorado Springs, CO, (719) 540-3900, FAX (719) 540-3970.—Steven H Leibson

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NEWS BREAKS

TOOL AUTOMATES GRAPHICAL-USER-INTERFACE DEVELOPMENT

Telesoft's Teleuse 2.0 development tool lets developers create OSF/Motif-based application programs without writing the user-interface code. Users paint the screens needed for the application, and the software tool generates the C-language code that performs the user-interface function. The tool can also output code that is compatible with the Open Software Foundation's user-interface language. Other features include support for OSF/Motif version 1.1, support for the X-Window standard version X11R4, and a porting kit that lets you execute software developed with the tool on any OSF/Motif-based system. The software tool will be available in July for \$7500 on SPARC, IBM RISC System/6000, and DECstation systems. Telesoft, San Diego, CA, (619) 457-2700, FAX (619) 452-1334.—Maury Wright

GATE ARRAYS OFFER EMBEDDED CELLS

Fujitsu Microelectronics IC Division's family of digital gate arrays offers embedded functions. The functions include single-, dual-, and triple-port RAM, ROM, a multiplier, customized I/O buffers, mask-programmed PLAs, and microprocessor peripheral functions. Initially, these arrays, like standard cells, require all-layer processing. To reduce subsequent turnaround times, you can specify—and pay—to have wafers held at metal mask. These wafers give you the flexibility to make logic changes after evaluating your design. Fujitsu Microelectronics, San Jose, CA, (408) 922-9000, FAX (408) 432-9044.—Michael C Markowitz

RAMDAC SUPPORTS TRUE-COLOR GRAPHICS

The Bt484 RAMDAC (random-access-memory DAC) from Brooktree Corp offers a variety of high-performance graphics features to designers creating PC graphics cards. The device supports resolutions as great as 1024 × 768 pixels in a variety of color modes with gamma correction for true-color modes. It supports XGA 5:6:5-bit (RGB) color mode, Image Capture 5:5:5-bit color mode, 24-bit true color, and is backward compatible with VGA. The RAMDAC can switch between true-color and VGA modes on a pixel-per-pixel basis, preventing the color limitations of VGA from distorting image colors when displaying multiple image windows.

The device also offers a hardware cursor to speed your graphics board's operation under Windows 3.0. The 32 × 32 × 2-bit cursor eliminates the need for the CPU to write a cursor into video memory; the RAMDAC superimposes its cursor wherever you specify, without disturbing the underlying image. Other device features include separate pixel ports for VGA (8-bit) and true-color (32-bit) data and a built-in shift clock to simplify your Video RAM interface. The device comes in 75- and 85-MHz speed grades and is sampling now. Volume production will begin in October; priced from \$29. Brooktree Corp, San Diego, CA, (619) 452-7580, FAX (619) 452-1249.

—Richard A Quinnell

1-GATE ICS PUT THE LOGIC YOU WANT WHERE YOU WANT IT

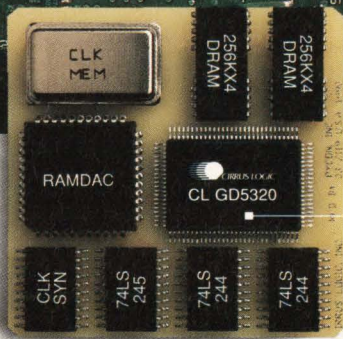
Each member of the TC7SXX family of logic devices from Toshiba places one logic gate in a 5-pin SOT-23MOD package measuring 2.9 × 2.8 × 1.1 mm. The 16-member family includes all of the basic logic functions and their logical complements, an analog switch, and a Schmitt-trigger gate. Example pricing includes the \$0.16 TC4S71F OR gate and the \$0.20 (25,000) TC7S00F NAND gate. Toshiba America Electronic Components, Irvine, CA, (714) 455-2000, FAX (714) 859-3963.

—Steven H Leibson

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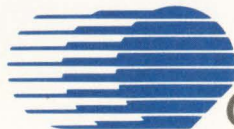
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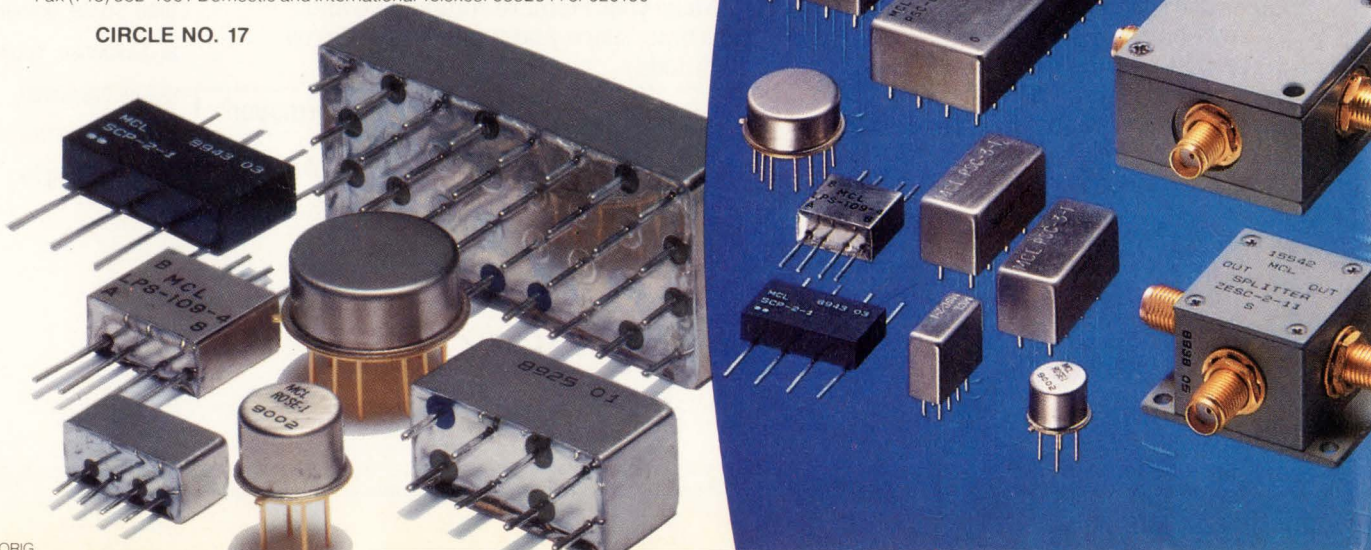
For detailed specs and performance data, refer to the MicroWaves Product Directory, EEM or Mini-Circuits RF/IF Signal Processing Handbook, Vol. II. Or contact us for our free 68-page RF/IF Signal Processing Guide.

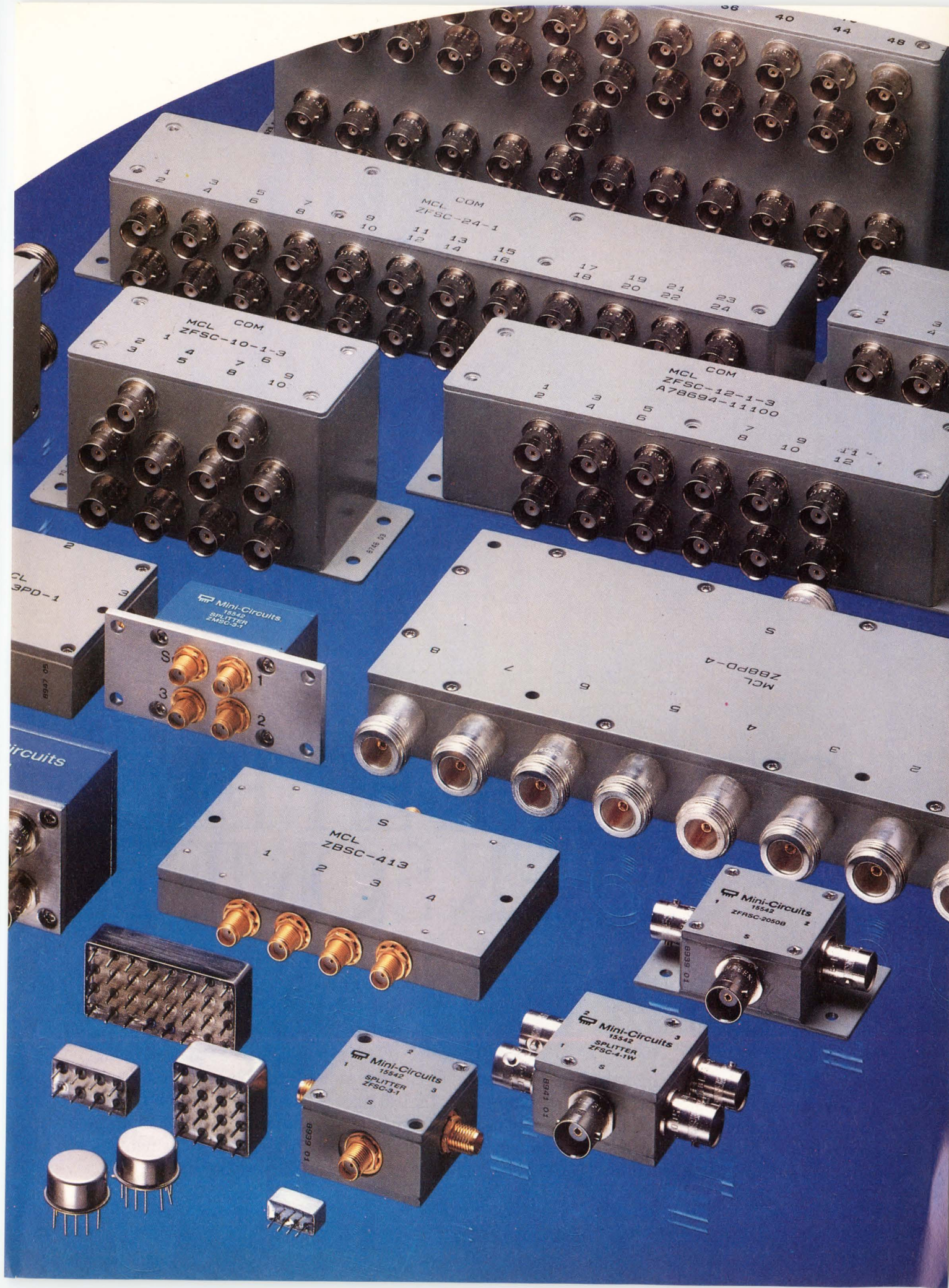
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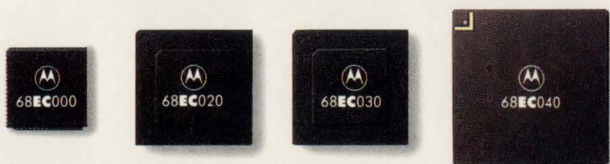
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OTHER 32-BIT EMBE OFFER SOMETHI




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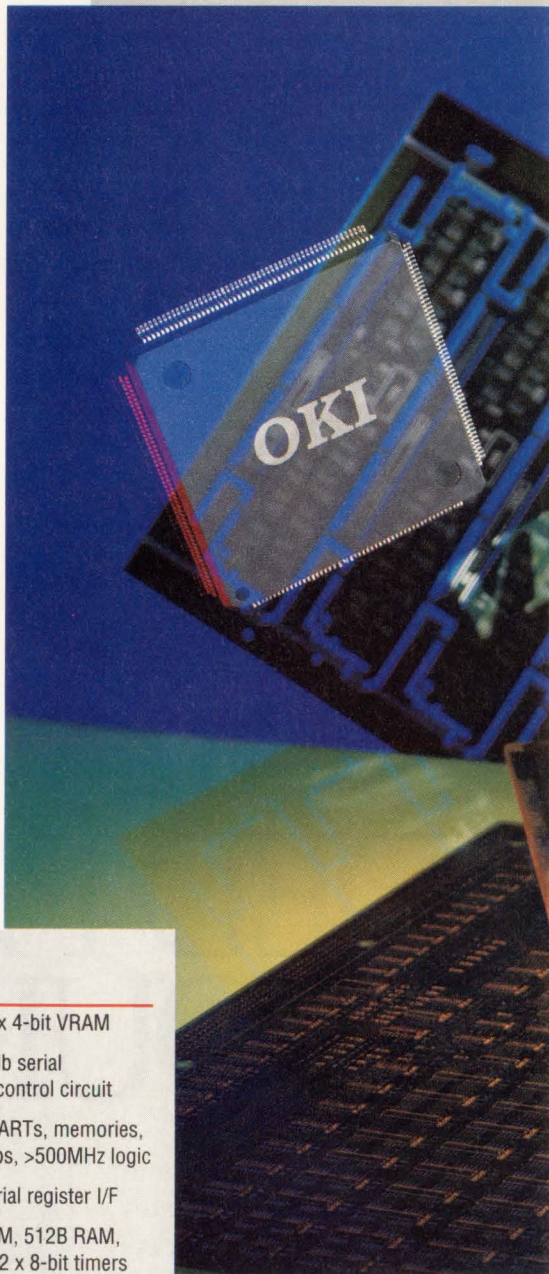
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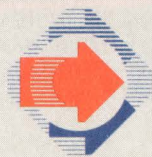
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	C P U	O S C	M R A M	D M A				
Z84C01	✓	✓						✓
Z84C50	✓	✓			✓			✓
Z84C90	✓	✓		✓				✓
Z80180	✓	✓	✓	✓	✓	✓		✓
Z80280	✓	✓	✓	✓	✓	✓		✓
Z84013/C13	✓	✓			✓			✓
Z84015/C15	✓	✓			✓			✓
Z84011/C11	✓	✓			✓	✓	✓	✓
Z80181	✓	✓			✓	✓	✓	✓

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SIGNALS & NOISE

Reader responds to Editor's Note about Apple

In his Editor's Note to the letter from J Thomas Baylor (EDN, March 14, 1991, pg 26), Jon Titus said that he would have been more impressed if Apple had made a commitment to an open bus. Apple has had the Nubus in their bigger machines since 1987, even before IBM switched to Micro Channel (a proprietary bus).

Apple has always encouraged companies to develop or port engineering and scientific applications to the Mac. I wonder why only a few companies do so. In our company, we use Macs only. We refuse to use MS-DOS-based software. If a semiconductor supplier cannot offer us a way to do development for their chips (PALs, μ Ps, and such stuff) on a Mac, we refuse to use their chips.

*Guido Körber
Applied Technologies
Berlin, Germany*

(Ed Note: Which side of the Wall were you on?)

Group offers outlet for budding experimenters

In Jon Titus's editorial, "Where are the experimenters?" (EDN, February 4, 1991, pg 29), he laments the small number of engineers who help youngsters discover "a love for the technology and a deep enthusiasm for new possibilities." Now that President Bush plans to recruit 100,000 volunteer engineers to assist teachers through the new Engineers in Education program, perhaps more engineers will work with youth. The American Radio Relay League, a nonprofit national organization for amateur radio operators assists professionals who want to take amateur radio to school—in particular, through the Shuttle Amateur Radio Experiment where students talk to orbiting astronauts via ham radio.

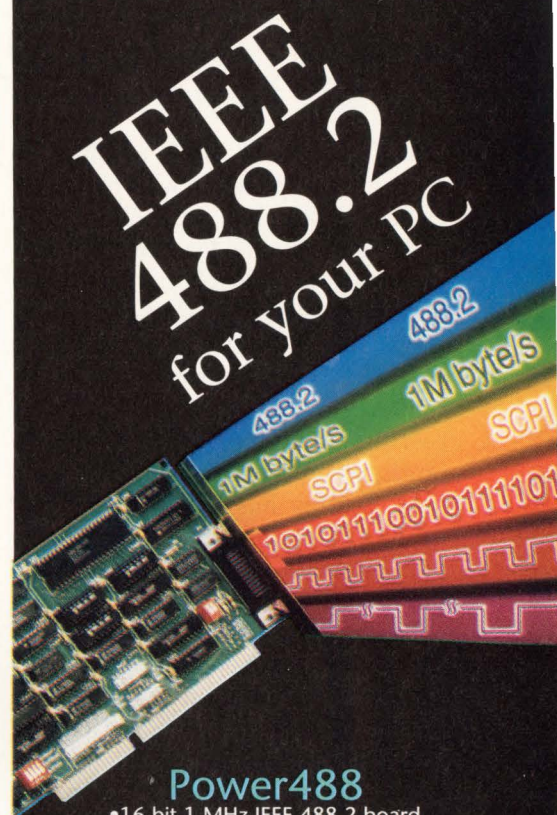
We also work with the IEEE, which sponsors a program for engineers called Amateur Radio in the Classroom. The professionals we've assisted report that students who get their hands on the radios and talk, rather than just listen, do get excited, even with cellular phones around. According to some teachers, the Federal Communications Commission's new entry-level amateur radio license, which doesn't require a Morse code test, has sparked the interest of students whose enthusiasm for ham radio was dampened by having to tackle Morse code. Anyone interested in taking amateur radio to school or in getting a license can contact ARRL, Dept EADN, 225 Main St, Newington, CT 06111, phone (203) 666-1541, or FAX (203) 665-7541.

*Rosalie White
Call Sign WA1STO
Educational Activities Manager
American Radio Relay League Inc
Newington, CT*



Simulation limitations hamper testing of Aegis

In response to Jon Titus's editorial "Smart weapons, smart lessons"



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Driver488 3.0

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CIRCLE NO. 23

SIGNALS & NOISE

(EDN, March 14, 1991, pg 35), I'm an engineer/manager who has been closely associated with the Aegis and 3-T programs for more than 25 years (15 years as a Navy engineering-duty officer and 10 years as the Aegis prime contractor, RCA/GE). I believe a fair appraisal will show that Aegis testing has exceeded the testing of any prior Navy AAW (antiaircraft warfare) missile system. Testing has been constrained primarily by the Navy's inability to fully simulate realistic battle conditions.

Recognizing the constraint very early, the original prime contractor, Wayne Meyer, fought hard for the necessary annual appropriations to improve the Navy's ability to test Aegis directly at high-threat levels. The Aegis program [director] funded the development and fielding of improvements in electronic

countermeasure jamming, chaff, targets, and range-control upgrades.

Meyer also established and funded a full-time "Old Crow" team of critics and adversaries for the early identification of soft spots in the design, as well as optimum tactics and techniques to use against Aegis. The present situation is that the Navy doesn't yet have the testing ability to fully stress the Aegis ships.

Safety considerations also impose constraints on staging a wartime environment against Aegis ships. Nearby populated areas, civilian aircraft, line-of-sight communications, and telemetry prevent a full spectrum of attack scenarios.

Has Aegis been tested under realistic conditions? Yes, to the best of the Navy's ability. Has it been fully stressed? No, it has not, but

not because of any contrived plan or bogus conditions.

*Robert C Beers, Manager
AAW Development Programs
GE Aerospace
Moorestown, NJ*

First, "number facts," then calculators

In answer to Jon Titus's editorial about teaching math (EDN, April 11, 1991, pg 41), I agree in part, wholeheartedly, but I was also married to an elementary-school teacher for many years. I learned from her a little about teaching math in the lower grades. At that level, a calculator would be an unmitigated disaster. The "number facts" must be learned so that they are second nature.

My wife had a cartoon showing a little boy at the blackboard, pout-

When customers
ask how I got so many
connectors
delivered so fast,
I tell them I have
connections.

- Ken Talentino
Multi-National
Account Executive

SIGNALS & NOISE

ing, with his arms folded. On the board was a problem like 657×149 . The teachers says, "Because calculator batteries go dead, that's why." I was once that little boy.

When I was nine years old or so, a neighbor who was an engineer died. I inherited his slide rule. No one in my house knew how to run it. I used to stare at it by the hour as I slid it back and forth. Once, by accident, I aligned the 1 with a 2, and noticed that at the other 2 was 4, and at the 3 was 6. I was hooked. I had a machine to do arithmetic. I refused to learn to multiply. Only after threats and promises would I learn my tables.

Log-log slide rule or scientific calculator, the device is essential to free the mind to explore math. Once children have learned the basics of arithmetic, their minds should be allowed to soar by using calcula-

tors to take the drudgery out of it.
Will Cochran
Chemagnetics Inc
Otsuka Electronics
Fort Collins, CO

Milli—not mega

In the Test & Measurement Instruments section of New Products (EDN, April 11, 1991, pg 176), EDN ran an item about the SR760 FFT spectrum analyzer from Stanford Research Systems. We erroneously described the \$4350 instrument as covering a much wider frequency range than FFT analyzers cover. The product works with signals from 191 *milli*Hertz (not MHz) to 100 kHz. Stanford Research Systems Inc is located at 1290D Reamwood Ave, Sunnyvale, CA 94089. Phone (408) 744-9040. FAX (408) 744-9049. TLX 706891.

IT'S EASY TO HAVE YOUR SAY

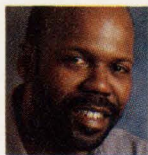
EDN's Signals & Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. You can use one of several easy ways to reach us. First, there's always the mail. Send your letters to Signals & Noise Editor, EDN Magazine, 275 Washington St, Newton, MA 02158. Or, send us a message via MCI mail at EDNBOS. Finally, EDN's bulletin-board system is ready for use—and it's free (except for the phone call). You can reach us at (617) 558-4241 and leave a letter in the EDITORS Special Interest Group. You'll need a 2400-bps or less modem and a communications program that is set for eight data bits, no parity, and one stop bit, or 1200/2400, 8N1 in shorthand.

EDN

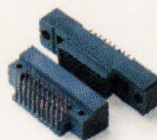


Our multi-national customers see Ken Talentino as their link to a wide spectrum of connector products. But

they don't see all



the people he relies upon for on-time



delivery and zero defects. There's

Chris testing ribbon cable assemblies. Tami quoting environmental connectors.



Cathy

watching over filter

connectors. And



Bernie who markets



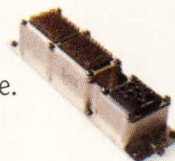
RF connectors. While Bill designs overmolded cable

assemblies. These are just some of the key connections that make Amphenol a world class manufacturer,



and

second to none when it comes to customer service.



Amphenol
an L.P.P. company
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Spectra Strip/TTD (800) 745-1000

AIPC (607) 754-4444

Bendix (607) 563-5011

Fiber Optics (708) 810-5800

CIRCLE NO. 22

Does it meet Six Sigma

Can it do true

mixed-mode

testing?

What tools have been developed?

Before the A500 started testing Motorola's mixed-



"Motorola has adopted a Six Sigma initiative which focuses attention on approaching zero-defect performance in everything we do, including our test systems. Our purchase of

the Teradyne A500 test system supports our Six Sigma initiative and our competitive leadership challenge."

Director of Marketing


Motorola knows you can't have a Six Sigma process unless you can test to Six Sigma standards. That's why Motorola's MOS Digital-Analog Integrated Circuits Division chose the Teradyne A500 Analog VLSI Test System. Because, in addition to proving the A500 could handle the

complex technical requirements of Motorola's advanced ISDN interfaces, we also demonstrated that we could perform to Motorola's stringent quality levels.

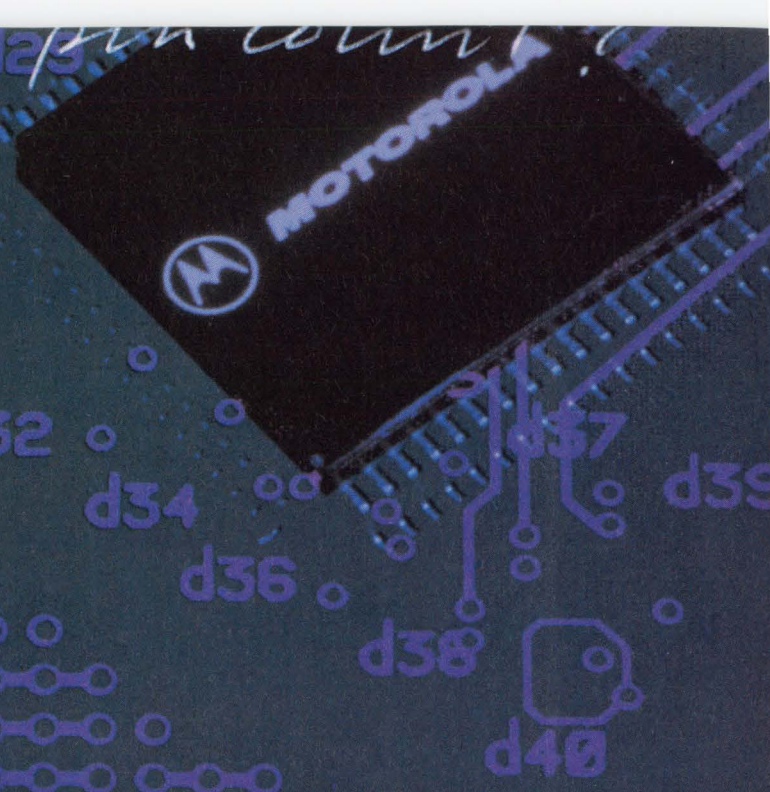
"Can it do scan testing? Digitize high-frequency waveforms? Do true mixed-mode testing? Does it have a flexible architecture? Can you give us the support for a Six Sigma process? Applications expertise? Complete documentation? The right tools? In each case, Teradyne answered yes."

Manager, Advanced Test Technology

IMAGE is a trademark of Teradyne, Inc.

Motorola and  are registered trademarks of Motorola, Inc.

standards?



CAN IT DIGITIZE HIGH-FREQUENCY WAVEFORM

signal technology, Teradyne had to pass a few tests.

With the A500, Motorola had the ability to digitize waveforms at 20 MHz, plus the high pin count necessary to guarantee that their ISDN U-Interface worked the way it was supposed to.

Best of all, the A500's full tester simulation and powerful IMAGE™ software provided the design flexibility and rapid debugging Motorola needed to deliver defect-free parts on time.

"The A500 gave us the resources we needed, in one place, to be able to have a functioning test program very quickly – at least two to three times faster than any other test system. This type of support is just what we need to get our complex circuits, such as the U-Interface transceiver, to the marketplace ahead of the competition."

Operations Manager

To Motorola, delivering Six Sigma quality is not just a promise. It's a way of doing business. And it's a test that must be passed by suppliers as well.

To see how our A500 family of test systems can help you deliver quality, call Beth Sulak at (617) 482-2700, ext. 2746.

Or call your nearest Teradyne sales office, or write: Teradyne, Inc., 321 Harrison Ave., Boston, MA 02118.

TERADYNE

FILTERS



dc to 3GHz from \$1145

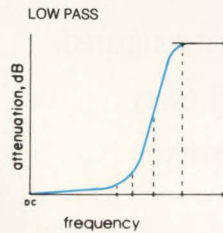
lowpass, highpass, bandpass, narrowband IF

- less than 1dB insertion loss • greater than 40dB stopband rejection
- 5-section, 30dB/octave rolloff • VSWR less than 1.7 (typ) • meets MIL-STD-202 tests
- rugged hermetically-sealed pin models • BNC, Type N; SMA available
- surface-mount • over 100 off-the-shelf models • immediate delivery



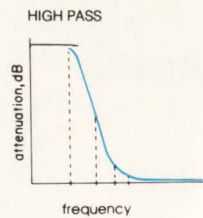
low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB)		STOP BAND, MHz (loss >20dB) (loss >40dB)			VSWR		PRICE \$ Qty. (1-9)
	Min.	Nom.	Max.	Max.	Min.	pass-band typ.	stop-band typ.	
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45



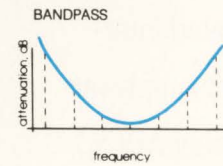
high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB)		fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss >20dB) (loss >40dB)		VSWR		PRICE \$ Qty. (1-9)
	Min.	Min.		Min.	Min.	pass-band typ.	stop-band typ.	
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95



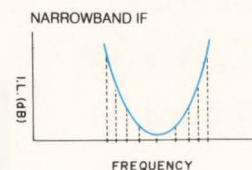
bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB)		STOP BAND, MHz (loss > 10 dB) (loss > 20 dB)				VSWR 1.3:1 typ. total band MHz	PRICE \$ Qty. (1-9)
		Max. F1	Min. F2	Min. F3	Max. F4	Min. F5	Max. F6		
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95



narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. >20dB		STOP BAND, MHz I.L. >35dB		PASS-BAND VSWR Max.	PRICE \$ Qty. (1-9)
			F5	F6	F7	F8-F9		
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95



CIRCLE NO. 26

Mini-Circuits

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Since other 12-bit ADCs need four times the space to go half as fast at twice the price, we use the term 'competition' lightly.



Maybe we are being a little boastful when we say that compared

to the AD671, every

other 12-bit monolithic A/D converter is a lightweight. But see if you don't agree.

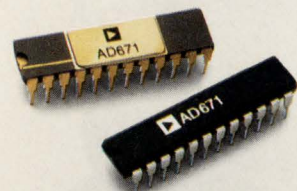
The AD671 comes in a 24-pin skinny DIP package. (Other A/D converters are in double- and triple-wide DIPs, taking up to four times as much space on your board.)

The AD671 has a true conversion time of 500 ns. (Making it twice as fast as the nearest 'competitor'.)

The AD671 costs only \$65. (You can expect to pay at least double that amount for any other 'comparable' ADC.)

And the AD671 doesn't have calibration cycles, complicated interfaces, or specs that can't hold up over temperature and power supply variations. (But if you like these things, you can get them with other ADCs.)

To find out more about the A/D converter that has more weight behind it, get a data sheet on the AD671 by contacting Analog Devices at 1-800-262-5643. Or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.



AD671 500 ns A/D CONVERTER.

The AD671 is the fastest 12-bit monolithic A/D converter, converting in under 500 ns while consuming less than 500 mW. It accepts standard input signals of 0 to +10 V, 0 to +5 V or ± 5 V, and it outputs data in offset/straight binary or two's complement format. The AD671 offers the right combination of speed and resolution for imaging applications using charge coupled devices, infrared detectors or photomultiplier tubes, while its accuracy is ideal for multichannel data acquisition systems and communications systems.

 **ANALOG
DEVICES**

ASK EDN

EDITED BY JULIE ANNE SCHOFIELD

Source of alternate sources

More than half the letters Ask EDN receives are from engineers looking for alternate sources or sources of obsolete parts. *The 1991 DATA Digest Alternate Sources and Replacements Library* contains alternate-source information for more than 688,000 devices, including ICs and discrete semiconductor devices. The library also includes more than 173,000 discrete-semiconductor suggested replacements. Parts from more than 500 manufacturers are represented. The 3-volume set costs \$295.

DATA Business Publishing
Box 6510
Englewood, CA 80155.

Also, the following company has picked up some obsolete RCA consumer parts:

Thomson Consumer Electronics
200 Clements Bridge Rd
Deptford, NJ 08096.

Few high-temperature-component sources found

We are looking for components to operate at 200 and 250°C: op amps, voltage regulators, transistors (similar to 2N2907 and 2N2222), diodes, resistors, capacitors, transient suppressors, miniature EMI filters, and analog ASICs or hybrid microcircuits.

Donald Weinstein
Kulite Semiconductor Products Inc
Leonia, NJ

We first turned to National Semiconductor's Bob Pease with this question. He says that he is not aware of any parts specified at these temperatures, but says the LM12 150W op amp will work at temperatures as high as 250°C.

Contacts at Harris Semiconductor (Melbourne, FL) say the company used to have a line of components specified for high-temperature opera-

tions but discontinued the line when the oil industry in the United States fell apart. Harris still has some products, including op amps, that operate at 200 and 250°C, but there are no guarantees.

Several companies, including Silicon General (Garden Grove, CA), are working on a radiation-hardened process that produces parts that can operate at 300°C. The technology is called silicon on insulator, or SOI. In six months to a year, Silicon General plans to introduce a 5V power regulator and a PWM control chip made using SOI processes. If any readers can shed more light on the SOI process, Ask EDN would like to hear from you.

We were much more successful finding sources of high-temperature resistors and capacitors. Caddock Electronics makes high-precision, high-voltage, and metal-film resistors that operate at temperatures as high as 275°C. Dale Electronics makes high-voltage, metal-film, metal-oxide, and wire-wound resistors that operate at both 200 and 250°C. Component Research Co Inc makes teflon-film capacitors that operate at 200°C.

Caddock Electronics
1717 Chicago Ave
Riverside, CA 92507
(714) 788-1700
FAX (714) 369-1151

Dale Electronics
Box 74
Norfolk, NE 68702
(402) 371-0080
FAX (402) 644-4206

Component Research Co Inc
1655 26th St
Santa Monica, CA 90404
(213) 829-3615
FAX (213) 829-9584

Reader seeks gold replacement

I have an application that uses an elastomeric (zebra) strip connector from an LCD to a pc board, which

we gold-plate to ensure a quality connection from the connector to the board.

I am currently investigating alternatives to gold plating for this application. I am looking into the use of lubricants, fluids, or other chemicals in conjunction with an elastomeric connector to provide the same quality connection between the elastomeric strip and the pc board that gold provides.

Any information, pro or con, about the method we currently use, methods involving lubricants, or any other successful zebra-to-pc-board mating methods would be useful to my investigation.

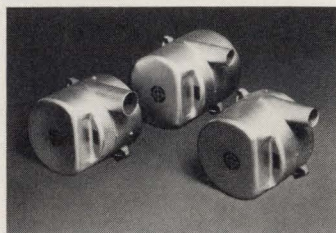
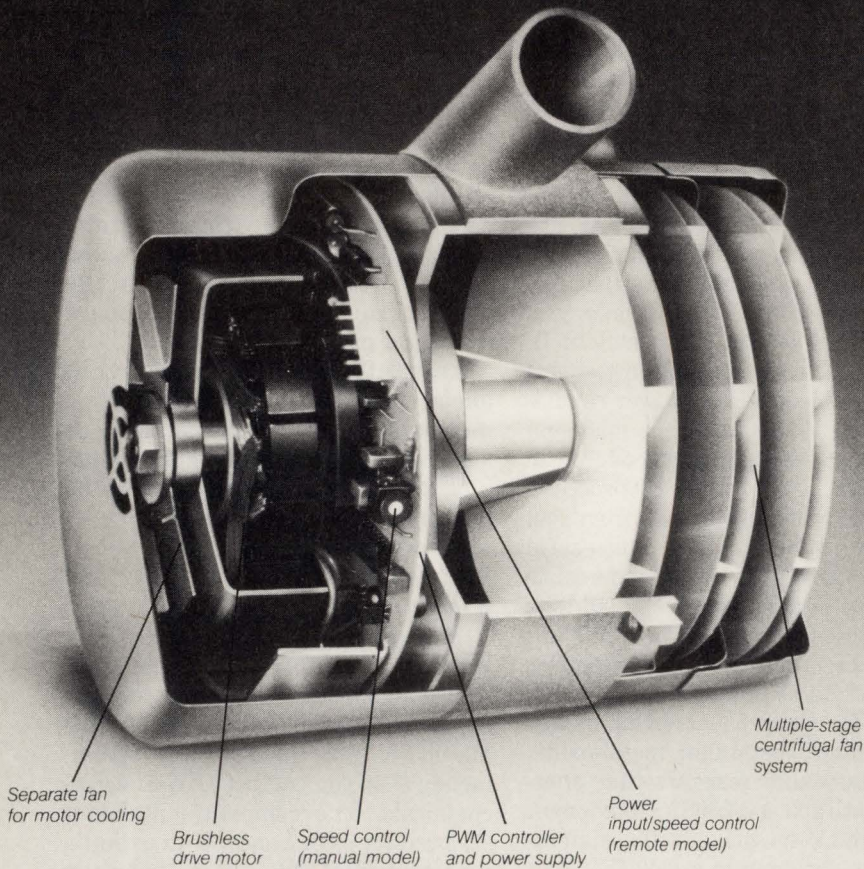
Marty Gappa
Watlow Controls
Winona, MN

Executive Editor Steve Leibson, whose Technology Update on contact-enhancing chemicals appeared in the March 14, 1991, issue of EDN, recommends that you contact D W Electrochemicals. The company's Stabilant 22 product is a concentrated liquid polymer that fills gaps between mated contacts and conducts current under an applied electric field. The product will probably do just the job you need, but you should ask the company about your specific application. Stabilant 22 could possibly work even better than gold plating because it fills in the gaps between the connector contacts and isolates the joint from the atmosphere.

D W Electrochemicals Ltd
9005 Leslie St, Unit 106
Richmond Hill,
ON, L4B 1G7 Canada
(416) 889-1522

Ask EDN solves nagging design problems and answers difficult questions. Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS. Or send us a letter on EDN's bulletin-board system at (617) 558-4241; leave a letter in the ask_edn Special Interest Group.

High performance blowers provide variable air flow from 120 VAC input



Compact units feature brushless dc motors with integral controller and variable speed capability

These new Wind-jammer® blowers combine electronics, motor, and fan system in a compact, cost-effective package. An exclusive Lamb Electric design, they were developed for demanding, limited space applications such as business machines, medical equipment and materials handling applications.

Just 5.7" in diameter, the blowers have 1-, 2-, or 3-stage fans for performance from 75" H₂O vacuum at 0 CFM to 125 CFM at 0" H₂O. With one version, a 0 to 10 VDC signal from a sensor or other device will control motor speed and adjust air perform-

ance from 0 to 100%. Or, a second model provides manual speed control by means of a potentiometer located in the blower housing.

These blowers also feature low noise performance and are UL/CSA component recognized. AMETEK, Lamb Electric Division, 627 Lake Street, Kent, OH 44240. Tel: 216-673-3451. Fax: 216-673-8994. In Europe, Friedrichstrasse 24, 6200 Wiesbaden, Germany. Tel: 611-370031. Fax: 611-370033.

AMETEK
LAMB ELECTRIC DIVISION

CALENDAR

CFC Alternatives Conference, Burlingame, CA. Angela Hoyte, Miller Freeman Expositions, 600 Harrison St, San Francisco, CA 94107. (415) 905-2354. FAX (415) 905-2239. June 24 to 26.

Test Engineering Conference, Atlanta, GA. Miller Freeman Expositions, Test Engineering Conference, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. June 24 to 27.

VXIbus User Group Meeting, Atlanta, GA. Matt Jacobs, National Instruments, 6504 Bridge Point Pkwy, Austin, TX 78730. (512) 338-9119. FAX (512) 794-5569. June 27.


International Conference and Exhibits on Failure Analysis, Montreal, Quebec, Canada. ASM International, Materials Park, OH 44073. (216) 338-1733. FAX (216) 338-4634. July 8 to 11.

Ionospheric Radio Propagation for System Planners (short course), Washington, DC. George Washington University Continuing Education, School of Engineering & Applied Science, Washington, DC 20052. (800) 424-9773; in DC, (202) 994-6106. FAX (202) 872-0645. July 8 to 11.




International Conference on Industrial and Applied Mathematics, Washington, DC. ICIAM Conference Manager, SIAM, 3600 University City Science Center, Philadelphia, PA 19104. (800) 447-7426; outside US, (215) 382-9800. FAX (215) 386-7999. July 8 to 12.

Engineering Workstations Conference, Boston, MA. EWC, Box 3275, Santa Monica, CA 90403. (213) 450-0500. FAX (213) 450-0132. July 9 to 11.

Programming with the AWK Language (short course), Seattle, WA. Specialized Systems Consultants



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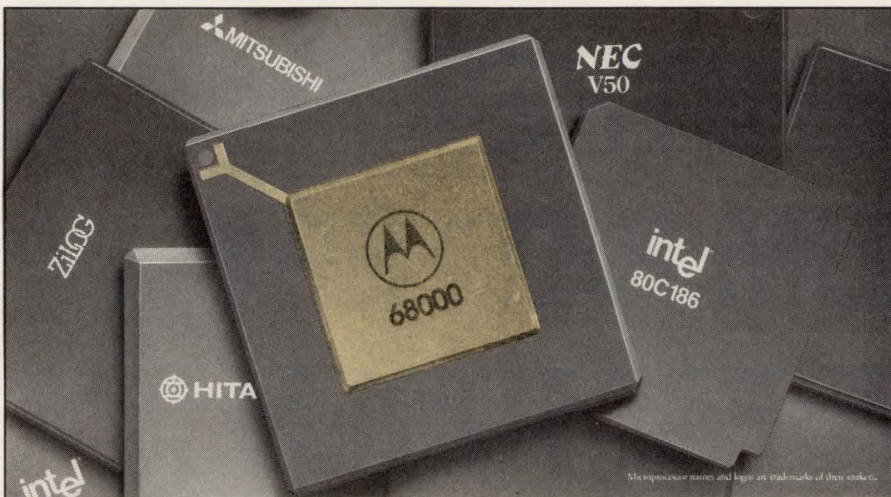
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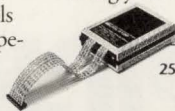
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Inc, Box 55549, Seattle, WA 98155.
(206) 527-3385. FAX (206) 527-2806.
July 11 to 12.

International Conference of Women Engineers and Scientists, Warwick, UK. Conference Services, ICWES9, 55 New Cavendish St, London W1M 7RE, UK. (071) 486-0531. FAX (071) 935-7559. July 14 to 20.

Ion Beam Processing: Techniques and Applications (short course), Cambridge, MA. MIT Summer Session Office, Massachusetts Institute of Technology, Room E19-356, Cambridge, MA 02139. (617) 253-2101. FAX (617) 258-6177. July 15 to 19.

Plastics Failure Analysis: Prevention and Testing Seminar, Denver, CO. Director of Educational Services, L J Broutman & Associates, 3424 S State St, Chicago, IL 60616. (312) 842-4100. FAX (312) 842-3583. July 18 to 19.

CMOS/BiCMOS: Process Integration and Engineering (short course), Troy, NY. Office of Continuing Education, Rensselaer Polytechnic Institute, Troy, NY 12180. (518) 276-8351. FAX (518) 276-8026. July 22 to 26.

Real-Time Structured Analysis & Design (short course), Los Angeles, CA. Learning Tree International, Box 45028, Los Angeles, CA 90045. (213) 417-9700. FAX (213) 337-7568. July 23 to 26.

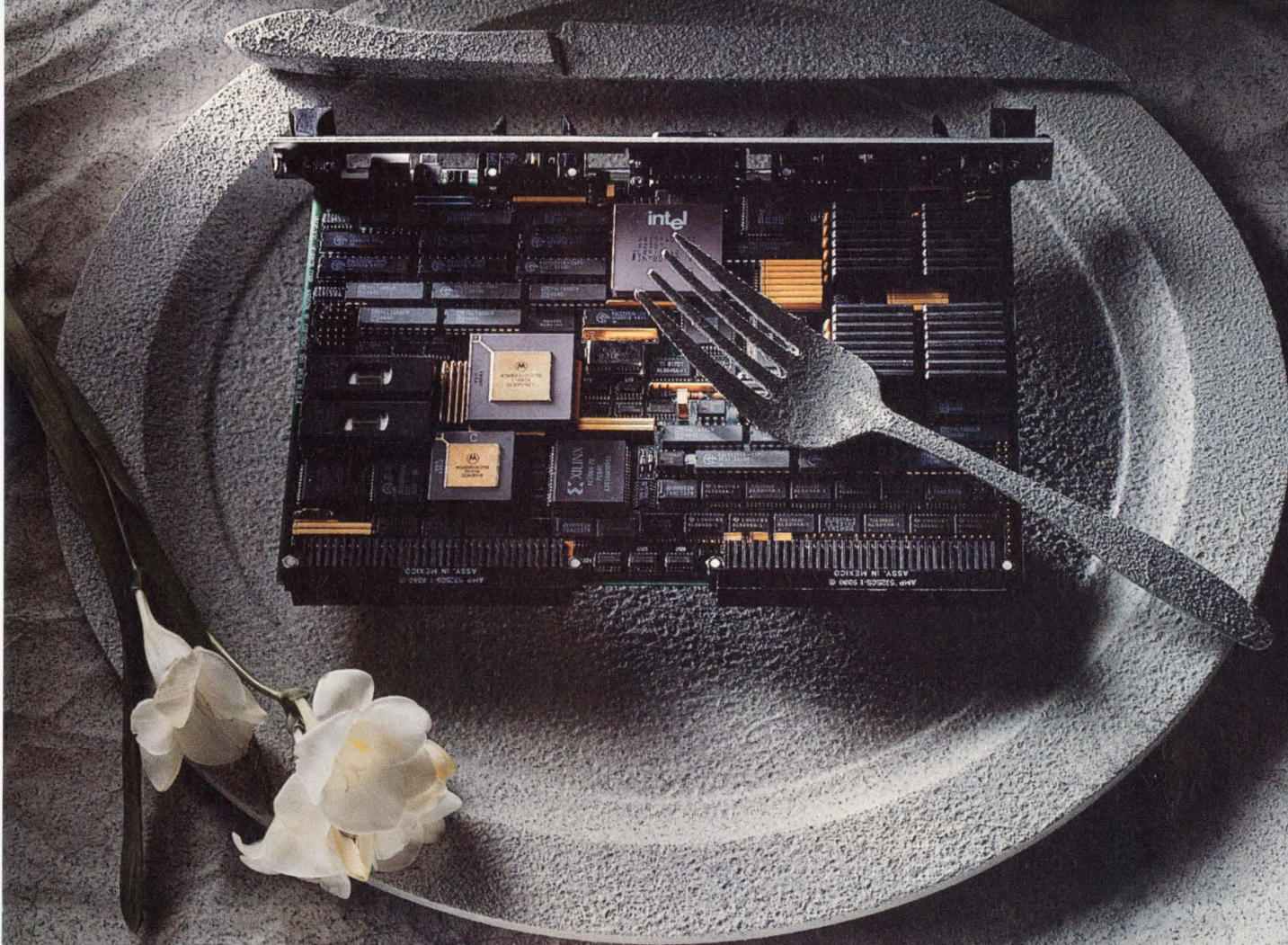
Siggraph Conference, Las Vegas, NV. Smith Buckland, Siggraph 91, 401 N Michigan Ave, Chicago, IL 60611. (312) 644-6610. FAX (312) 321-6876. July 28 to August 2.

Basic IC Technology Seminar, Sunnyvale, CA. ICE Corp, 15022 N 75th St, Scottsdale, AZ 85260. (602) 998-9780. FAX (602) 948-1925. August 6.

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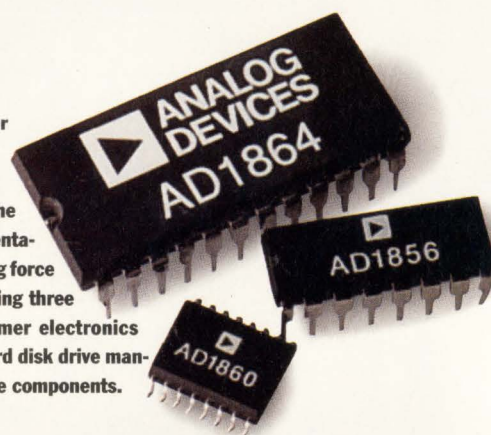
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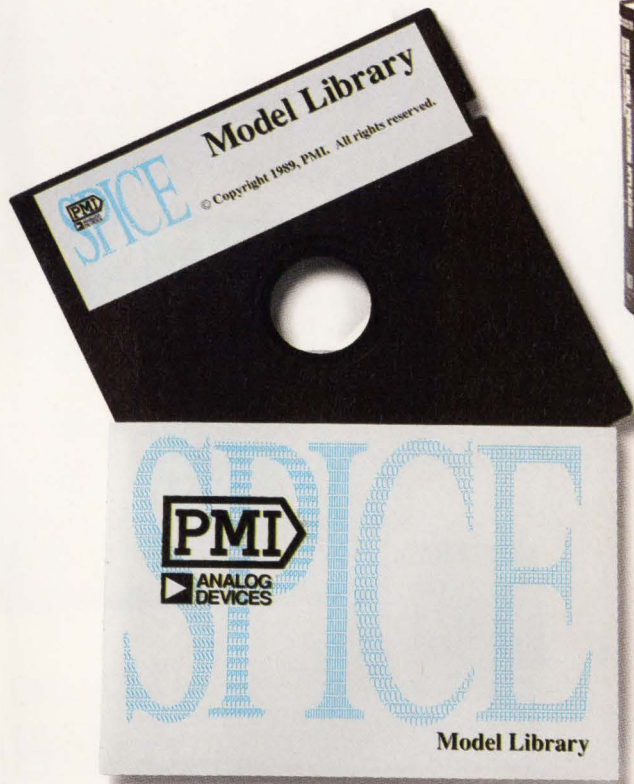


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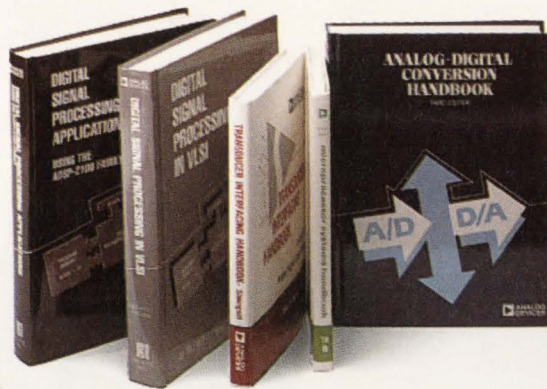
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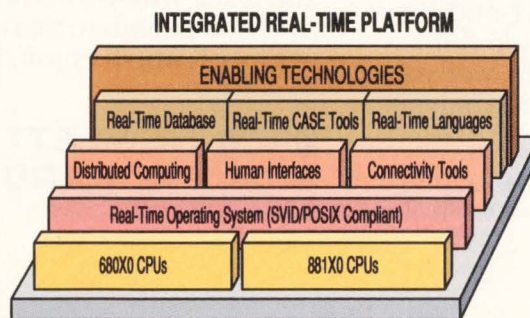
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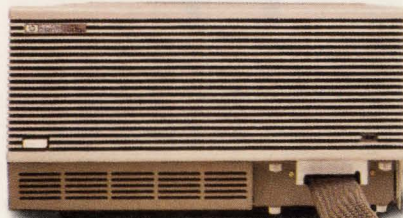
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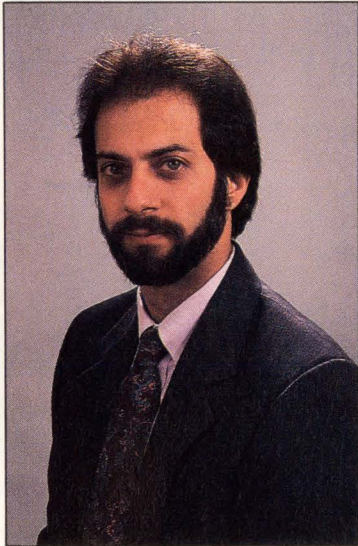
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EDITORIAL

The devil, you say?



This is the time of year when companies rush to put the finishing touches on CAE software and systems so that they can announce and show the products at the annual Design Automation Conference. Before you get swept away by all the new-product announcements, consider the fate of Fred.

Fred was a CAE software vendor for six years before the stress of staying ahead of his competitors took its toll. Fred had a stroke and passed away. Since Fred was mostly fair, honest, and responsible during his stay among the mortals, he went to Heaven. Saint Peter met him at the Pearly Gates and welcomed him with open arms. The angel gave Fred a tour and introduced him around. Being a smart businessman who makes decisions only after carefully evaluating all his options, Fred wasn't so sure that Heaven was all it was promoted to be.

"I'm sure Heaven is terrific," Fred said. "But before I agree to stay I have to check out the alternatives."

"You're wise to consider your options," Saint Peter replied. "I warn you, though, once you tell me your choice, you cannot change your mind."

Fred agreed, and the angel put him on the elevator to Hell. After a few minutes, the elevator slowed and then stopped. The door opened. There, waiting to greet Fred, was Satan dressed in a natty tuxedo and fluorescent green sunglasses. All around people were frolicking and making merry. The sounds of happiness and merriment were consuming. Fred was awe struck. "This is the place for me," he exclaimed. "I've got to go back and tell Saint Peter I'm staying here. I'll be right back."

Fred pushed the elevator's Heaven button. When he got there and told Saint Peter his choice, the angel was disappointed and reminded Fred of the finality of his decision. But Fred was confident he'd made the right choice. He said goodbye, got in the elevator, and pushed the button for Hell. As the elevator descended, Fred felt warmer and warmer. Soon Fred was so warm that he had to remove his shirt and tie. As the sweat dripped from his body, the elevator door opened. Satan, now dressed in flaming red, stood before him, pointed his trident, and ordered Fred from the car. Spine-chilling screams filled the air. Fred was frightened, but found the courage to ask what happened to all the happy people he'd seen just a few minutes ago.

"Ah," replied Satan, "That was just the demo."



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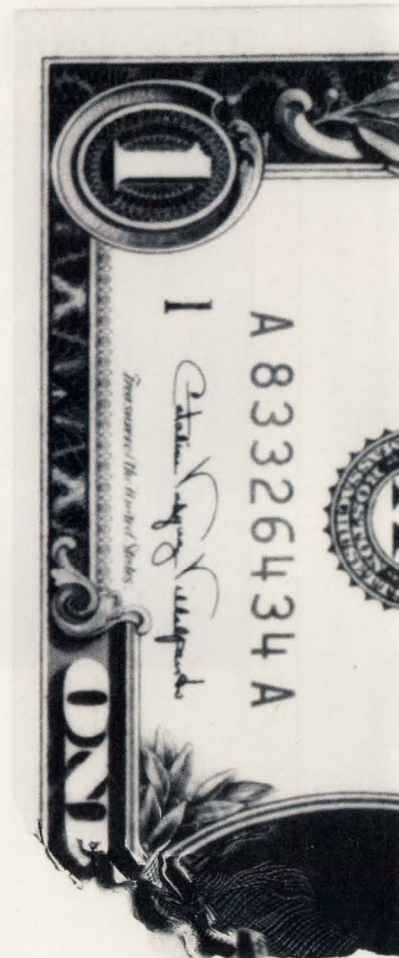
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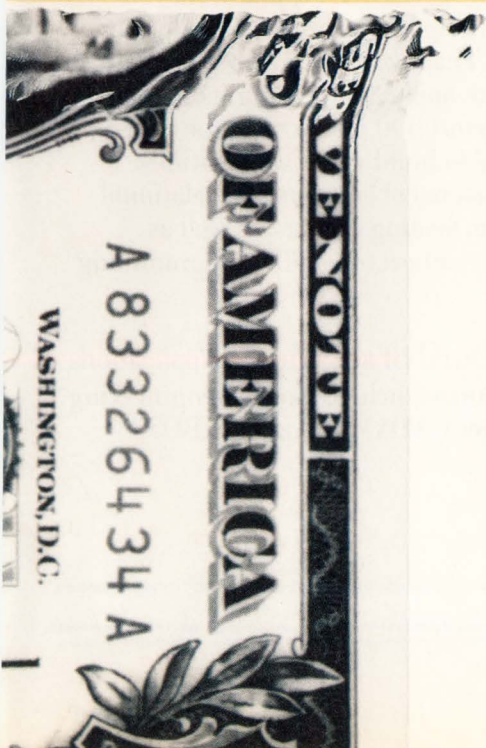
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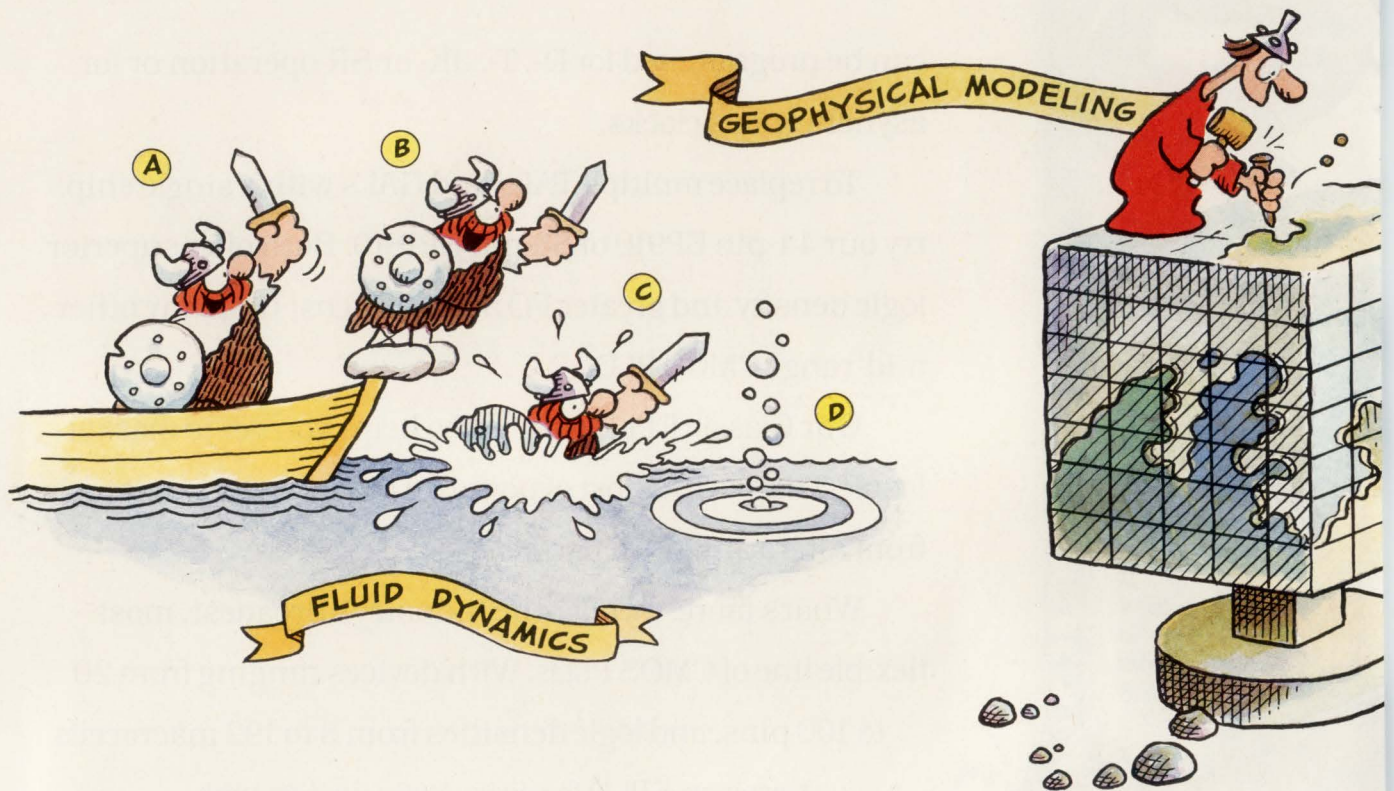
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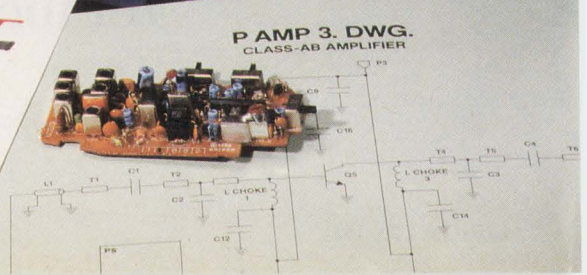
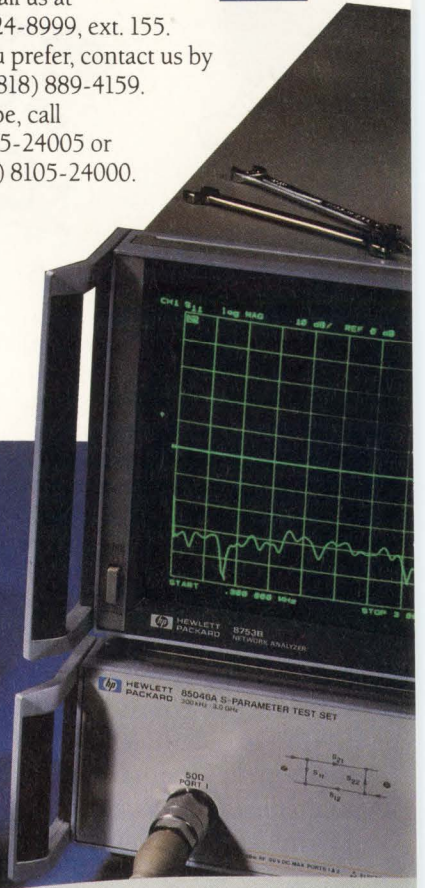
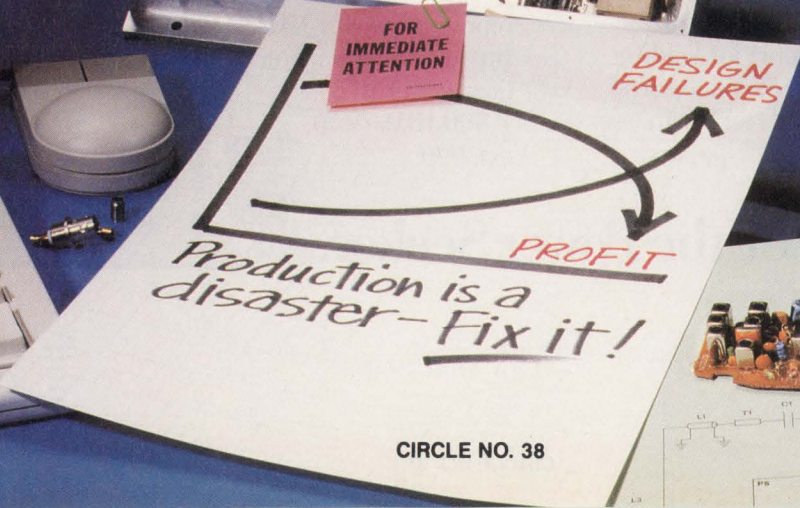
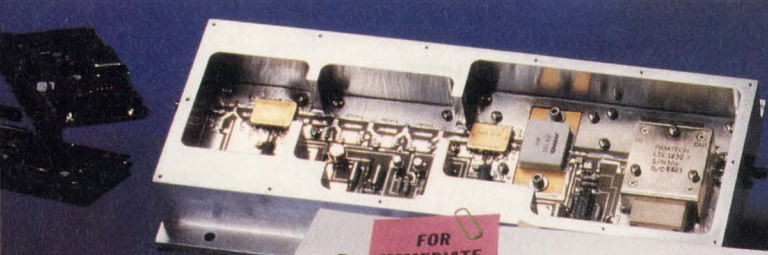
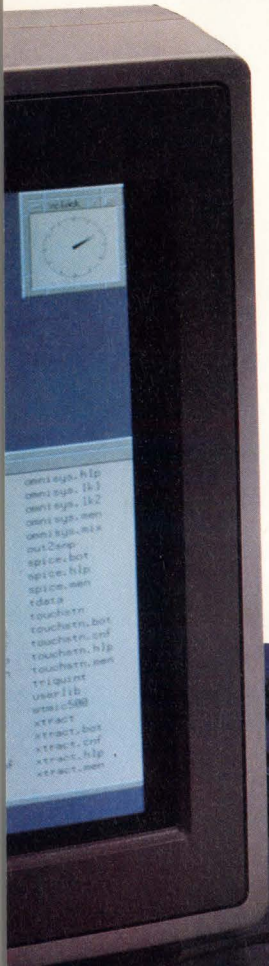
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*Brian Kerridge,
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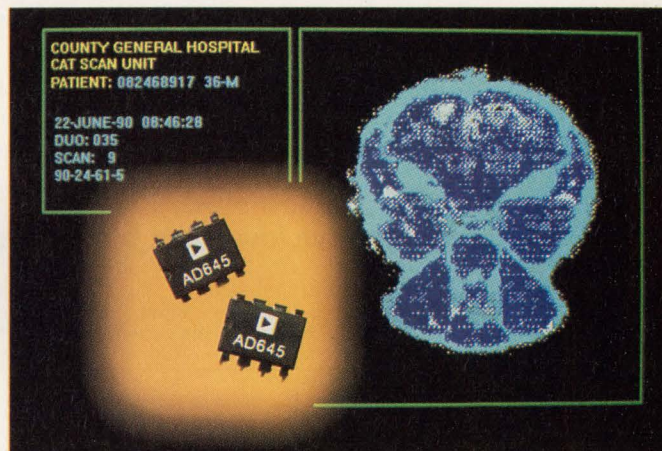
It doesn't take much to believe that amperes are flowing when you feel a component's warmth, or witness an occasional spark. But transport your mind to the femtoampere (10^{-15} A) level, and it takes a lot more effort to imagine anything useful trickling along the wires.

Nonetheless, current at this level is lifeblood to the input of electrometer-grade op amps. Electrometer-grade loosely describes that narrow class of op amps with input bias-currents (I_B) in the subpicoampere region. A narrow class it may be, but without these op amps, amplifiers capable of sensing teraohm source-resistance transducers, integrators with a 24-hour time-constant, sample-and-hold amplifiers with 100 μ V/sec drop, and log amplifiers with 180-dB dynamic range, would be harder, if not impossible, to produce.

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As is often the case, the design of an op amp's input stage determines its key characteristics. In general, for optimum low-level performance, a bipolar-transis-

tor input stage is the best compromise. But where importance of I_B is paramount, junction FETs (JFETs) or MOSFETs are the op amp designer's automatic choice for input component. Compared with a bipolar transistor, an FET's higher-input offset voltage (V_{IO}), V_{IO} TC, and doubling of I_B for every 10°C temperature rise is part of the penalty of focusing solely on I_B .



This CAT (computerized axial tomography) brain scanner uses Analog Devices' AD645 1.5-pA I_B op amp.

Even so, FET gate input-current depends upon the geometry and the fabrication process, and designers must still make adjustments to reach subpicoampere levels. Many common CMOS input-stage op amps have picoampere I_B at room temperature and below. But over an operating temperature range as high as 70°C ambient, I_B enters the low nanoampere region, rendering the op amp useless for sensing even 1-G Ω source resistance sensors. **Table 1** shows the few op amps with I_B no higher than 100 pA at 85°C. Compare prices

TECHNOLOGY UPDATE

Low-bias-current op amps

carefully, because figures assume lower-cost plastic packages where available. Some vendors insist upon metal packages, claiming that they offer screening advantages and more consistent performance in the long run.

While I_B is the principal concern for the range of applications mentioned, as always, other parameters play a secondary role. **Table 1** also shows input offset voltage V_{IO} , V_{IO} TC, and open-loop gain.

Choose FETs, JFETs, or MOSFETs

Both MOSFET and JFET input stages achieve low-level input current, but there are trade-offs with parameters other than I_B . MOSFETs can have the lowest input current, but generally show worse input voltage characteristics. MOSFETs are also more susceptible to transient damage without good protection, but protection

components induce more input leakage. Better process control with JFETs gives a significant edge to V_{IO} , and its associated TC and noise figure. But this outcome doesn't mean all vendors automatically offer JFET inputs. A glance at **Table 1** shows that approximately half of the vendors stick with MOSFETs. If you look further, you'll see as much as 10:1 difference in V_{IO} between JFET and MOSFET types. But note this ratio also tracks into the price column.

Whatever the choice of input FET type, op amp designers follow certain basic design principles. First, the smaller the dimensions of the FET, the lower the gate current. However, by indiscriminately reducing FET geometry, you eventually lose control of the voltage-match characteristics of the input pair, giving rise to high V_{IO} , and poor voltage noise performance.

Clearly, a balance between voltage and current objectives achieves optimal results.

In this fine balancing, no amount of fiddling with geometry and process alters the significant TC of an FET's gate current. Gate current approximately doubles for every 10°C rise in ambient. The only way to ensure an acceptable input current at 85°C is to design for a low femtoampere figure at room temperature.

Second, to maintain low-gate current across the operating range of variable input and power supply voltages, a cascode (or bootstrapped), input-stage circuit is mandatory. Effectively, this means internal power rails to the input stage float and track with the op amp's input signal. The result is a minute change in input characteristics with varying input signal or external power supply, yielding common-

Table 1—Representative low-input bias-current op amps

Vendor	Model	Input type	Input bias-current (fA)	Input bias-current at 85°C (pA)	Input offset-voltage (mV)	Input offset-voltage vs temperature ($\mu\text{V}/^\circ\text{C}$)	Open-loop gain with 2-k Ω load (dB min)	Small-signal gain-bandwidth product (MHz typ)
Analog Devices	AD515AL	JFET ¹	75.0	4.8	1.0	25.0	148	1.0
	AD546K	JFET	500.0	74.0	1.0	20.0 typ	100	1.0
	AD549L	JFET	60.0	9.0	0.5	10.0	100	0.7
	AD645K	JFET	1.5 pA	96.0	0.25	5.0	120	2.0
Burr-Brown	OPA111B	JFET	1.0 pA	130.0	0.25	1.0	120	2.0
	OPA128L	JFET	75.0	3.3	0.5	5.0	110	1.0
	OPA602C	JFET	1.0 pA	100.0	0.25	2.0	92	6.5
Harris	CA5420A	MOSFET	1.0 pA	15.0	5.0	Not specified	80	0.5
National Semiconductor	LMC662AI	MOSFET	40.0	4.0	3.0	1.3 typ	105	1.4
	LMC6041AI	MOSFET	2.0 typ	4.0	3.0	1.3 typ	100	75 kHz
Precision Monolithics	OP-80E	MOSFET	250.0	15.0	1.5	Not specified	100	300 kHz
Teledyne Components	1346	JFET	1.0 pA	30.0	3.0	5.0 typ	106	2.0
	1702	Varactor	5.0	2.0 fA/°D	5.0	30.0	100	350 Hz

Notes: 1. JFET = junction FET

2. Maximum specifications at 25°C, $\pm 15\text{V}$ supply shown unless otherwise stated.

3. Prices shown in order of availability, plastic, or metal.

TECHNOLOGY UPDATE

mode input-impedance figures of approximately 1000 teraohms ($10^{12}\Omega$), in parallel with less than 1 pF.

Common IC fabrication processes, called junction isolated, result by default in a reverse-bias diode that appears between individual components and the IC substrate. For normal ICs, this large parasitic diode junction causes no ill effect. For low I_B op amps however, the reverse leakage through the diode is significant.

Burr-Brown uses a dielectric isolation step in the fabrication process of its JFET input op amps, which eliminates the diode. According to Bruce Trump, Burr-Brown's op-amp product specialist, all of the company's low I_B op amps have dielectric isolation. Eliminating the diode-leakage element from the op amp's input current lets larger FET geometry yield voltage-characteristic improvements.



This PIN photodiode amplifier is one application for Burr-Brown's 75-fA I_B and 500- μ V V_{IO} OPA128. Using an HP 5082-4204 photodiode sensor and a feedback resistor of 10 G Ω , the circuit's V_{OUT} is 5V/nW.

Analog Devices uses a conventional junction-isolation process, but deals with leakage in the parasitic diode by using a pair of JFETs, each with two electrically isolated gates: The top gate handles the input from the outside world, while the back gate receives its drive from an internal bias network. The input current to the back gate contains the leakage-current element

of the parasitic diode, leaving the top gate with only its own input current. According to Jay Cormier, Product Marketing Manager with Analog Devices, the potential of the input FET's top and back gate track to within 30 mV over the operating supply voltage and temperature range. A second geometrically matched pair of dual-gate FETs model the operating point of the input FETs and develop a drive to bias the input-stage back gates. A further drop in I_B results from a top-gate junction area reduction to around 2000 μm^2 , in comparison with the back-gate area of more than 30,000 μm^2 .

Varactors win the day

While admiring process antics that achieve these unbelievably low currents, don't overlook what a bit of slightly older technology can do.

Teledyne's 1702 module op amp includes an example of a varactor-bridge-input stage for the ultimate in low I_B —5 fA at 25°C, with a TC of 2 fA/°C. This I_B effectively results from the leakage current of two reverse-bias diodes—the input varactor pair. The varactors form two arms of an ac capacitance bridge running at approximately 100 kHz. The input signal to the op amp causes a change in capacitance of one varactor diode, which unbalances the bridge. The conse-

Package	Comments ²	Price ³ (100s)
TO-99	Noise 4 μ V p-p typ 0.1 to 10 Hz	\$20
8-pin plastic DIP	Noise 4 μ V p-p typ 0.1 to 10 Hz, supply current 0.7 mA max	\$4.50
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TO-99	Noise 2.5 μ V p-p max 0.1 to 10 Hz	\$13.30
TO-99	Noise 4 μ V p-p typ 0.1 to 10 Hz	\$16.55
TO-99	Slew-rate 35V/ μ sec	\$9.85
TO-5, 8-pin plastic DIP	Single supply voltage 5V, or down to \pm 1V; supply current 0.55 mA max	\$3.37
8-pin plastic DIP, and small outline	Only dual op amp available, single supply voltage 5 to 15V	\$1.20
8-pin plastic DIP, and small outline	Single supply voltage 5 to 15V	\$1
TO-99	Supply voltage \pm 8V max, supply current 0.325 mA max at \pm 5V	\$7.20
TO-99		\$12
Module 1.125 x 1.125 x 0.5 in	1702-01 version has 10 μ V/°C TC	\$309 (10 off)

TECHNOLOGY UPDATE

Low-bias-current op amps

quent change in ac level from the bridge drives an ac amplifier, followed by a demodulator and dc amplifier to produce the op amp's output signal. Compared with monolithic op amps, the module's design is complex and the gain-bandwidth product is only 350 Hz. But with a key specification an order of magnitude up on its nearest rival, there is plenty of life in this product, even at \$309.

According to Jim Fleming, Teledyne's Applications Manager, the product appeals mainly to medical researchers, hospitals, and medical instrumentation manufacturers. There is also a growing military interest with infra-red search-and-track system integrators for use in test and calibration of circuits using monolithic, low- I_B op amps. Fleming points out that varactor inputs are particularly resistant to input overload abuse. The 1702 withstands inputs of $\pm 200V$ common-mode max, and 100V differential-mode typ.

By far the greatest problem designing with low- I_B op amps is ensuring that the op amp's input femtoamperes flow from the signal sensor and not from undefined sources elsewhere in the circuit. Without some very basic precautions, materials that you accept as insulators in normal circuits appear "leaky" to sensor- and op-amp-input impedances in the teraohm range. For example, a 15V power rail leaking through a 100-G Ω insulator results in 150 fA; you can see how easily stray leakage can swamp input bias current. By the same token, bear in mind settling time requirements, when just 1 pF with the same 100 G Ω results in a 0.1-sec time constant.

Keithley Instruments Inc publishes a booklet (Ref 1) that, although out of date in a few areas, still contains a wealth of useful in-

formation on principles and techniques in making low level measurements. Bob Erdman, Director of New Business Development at Keithley and a veteran designer of femtoampere-level circuitry, offers advice to novice engineers: In the low current world, you must adopt a mode of thinking whereby you look at everything as a current source and forget that there is any such thing as an insulator. You must model every material item in your design as a resistor, capacitor, and current source in parallel. This includes your pc-board, sockets, and standoffs. Using an electrometer, you can characterize all these components.

You must conduct measurements with your circuit under a good grounded shield at all times. A good shield means a light-tight box (many components, such as diodes, are photo-sensitive). If you have a 1/16-in. hole in the shield to bring out wires, then waving your arms around will cause the circuit to re-

spond. You must clamp and shield the lead out.

Regarding pc-board material, Erdman considers normal glass epoxy adequate for currents in the 1- to 10-pA range. Below that figure, Teflon clover-leaf standoffs are good down to 10 fA. If you need to deal with even lower currents, say 10 attoamperes ($10^{-17}A$), then you must consider sapphire standoffs.

Of all the problems, Erdman emphasizes effects that result from stress to materials. Teflon, in particular, generates current when stressed. For example, if you build a taught connection to a Teflon standoff into your circuit, don't be surprised if it generates 100 fA.

Low impedance diverts strays

The technique of guarding overcomes the main problem of channeling current from sensor to op amp, while deflecting all other sources of current. The method requires a low-impedance voltage source that faithfully tracks the magnitude of

For more information . . .

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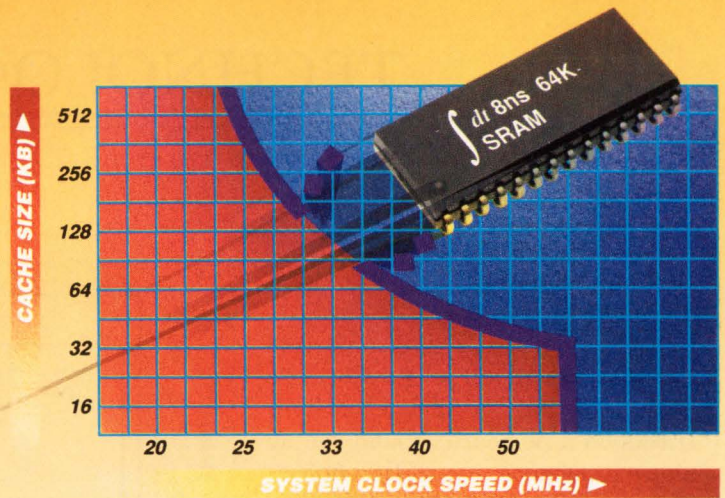
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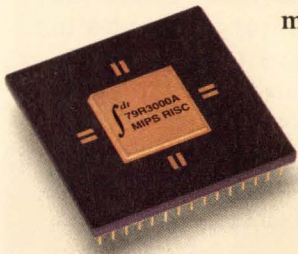
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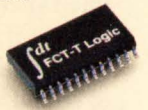
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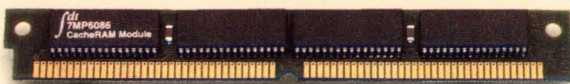
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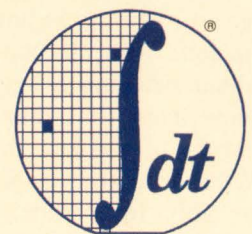
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Low-bias-current op amps

the input-signal voltage. This voltage source drives a conducting barrier that physically surrounds the input signal at all points along its path. The barrier may consist of tracks on a pc-board around the op amp's input pins, one of the screens of a coaxial or triaxial cable, or a metal enclosure. On the basis that with zero voltage between signal and guard, zero current flows into or out of the signal path. The guard barrier, being low impedance, also readily absorbs extraneous currents.

As well as reducing current-leakage effects, the guard minimizes the influence of stray capacitance on the signal path. Effectively, the low-impedance guard source, instead of the signal source, charges and discharges stray capacitances. A dramatic improvement in settling time arises, roughly in proportion to the ratio of signal source, to guard source impedance.

Other hazards exist that also confuse the femtoamperes in the op amp's input, which even perfect guarding cannot eliminate. These effects derive mainly from mechanical and electrochemical phenomena. Fig 1 shows a comparison of some of these phenomena and their magnitudes.

Movement of the sensor, measuring circuit, or the operator all cause minute changes in capacitance, which result in transient currents. Consequently, you must rigidly fix all parts of the measuring circuit.

Rigid cable for connecting sensors to circuits is not an appealing option. And, if you had thought about drawing a length of regular wire from that dusty reel in the corner of the lab, forget that too. Wire, insulated by low-cost plastic or polyvinyl chloride, is far too leaky for this application. PTFE (polytetrafluoroethylene)-insulated

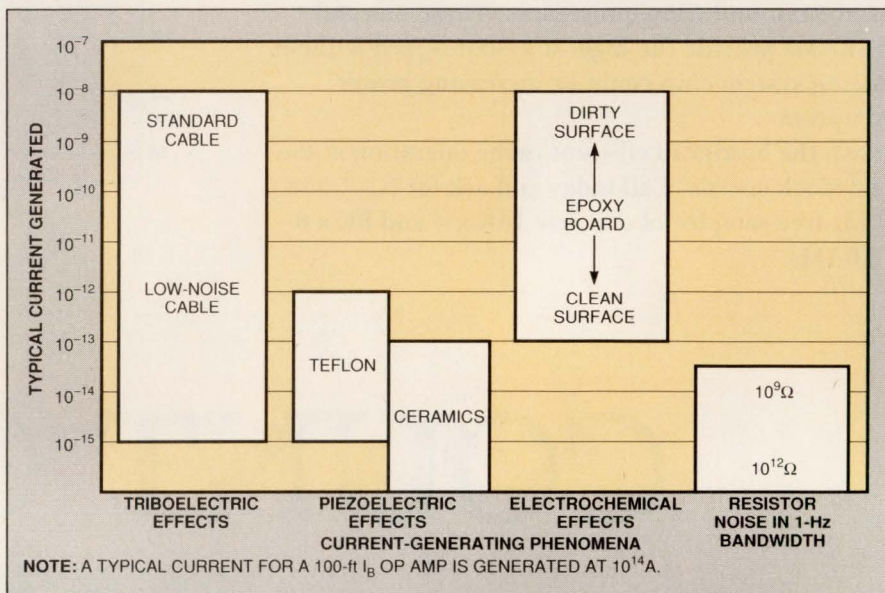


Fig 1—Various phenomena generate low-current levels. (Fig courtesy Keithley Instruments)

coaxial cable is preferable, but it should be an internally graphite-lubricated variety. The graphite lubrication in the outer braid reduces generation of charge as the cable flexes—a triboelectric effect.

Now having firmly bolted everything down, the next obstacle arises from microphones hidden in the measuring circuit. Vibration and shock to the insulation materials you have carefully chosen to protect the op amp's input current now produce error currents—a piezoelectric effect. Even favored Teflon insulators, ideal for lifting signals off the pc-board surface, become microphones at the femtoampere level. The only answer is to eliminate the origin of vibration.

You need to exercise equal care in the selection and handling of pc-boards used for the measurement circuitry. Even if you decide upon PTFE material as an improvement over conventional glass-epoxy, cleanliness of the board is a critical factor. Remnants of manufacturing chemicals not only open a leakage path, but also develop tiny voltaic cells sufficient to drive up to 100 fA.

Where guard tracks run on the pc-board, and where a conformal coating of solder resist covers the board's surface, it is a good idea to expose the guard to air. This arrangement ensures that the guard barrier remains effective even in the presence of surface contaminants and humidity. **EDN**

Reference

1. Keithley Instruments Inc, "Low level measurements," 1984.

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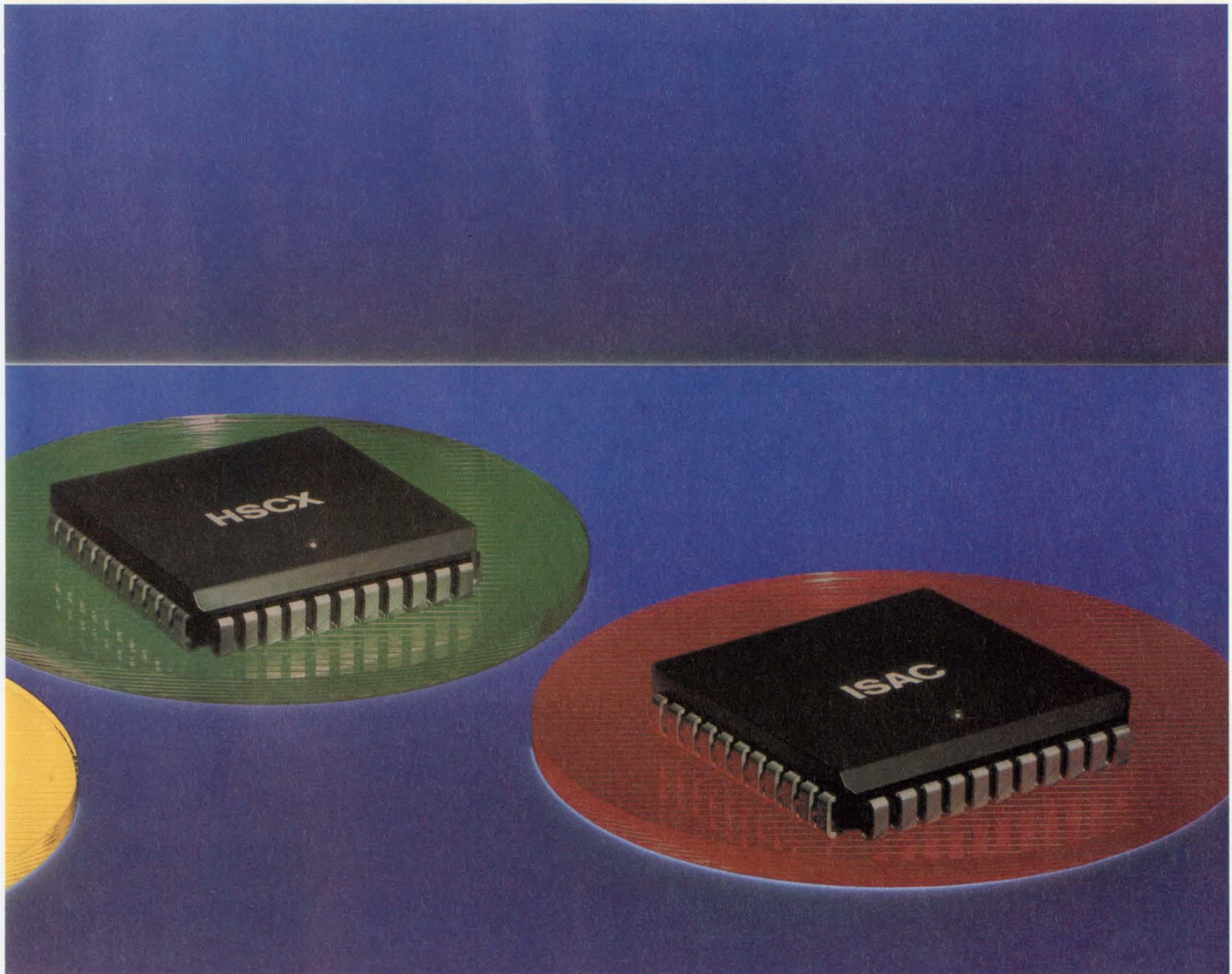
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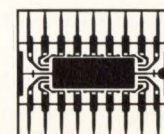
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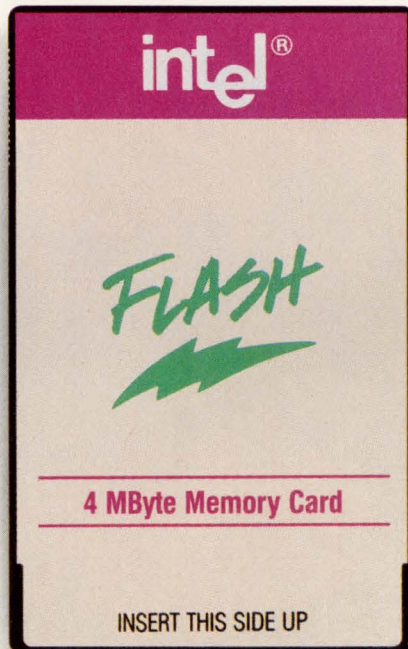
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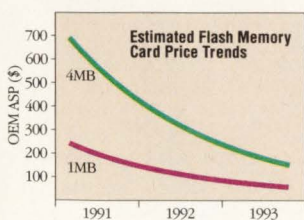
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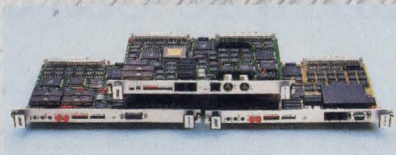
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*Charles H Small,
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The idea of credit-card-sized memory cards isn't really new. But two trends are spreading the idea out from niche applications toward widespread use. First, the ICs such memories use—both volatile and non-volatile—continue to increase capacity, consume less power, and drop in price. For example, Sharp has a 32M-bit masked ROM chip under development that will go into credit-card-sized memories nicely. Second, laptop computers promise to be a significant, high-volume application for these memories as a replacement for floppy disks.

Recently, a group of laptop-computer makers, memory-device vendors, and IC houses formed an association called the PC Memory Card International Association (PCMCIA). This group has endorsed a Japanese industry standard for use in laptop computers. Therefore, certain credit-card-sized memories and their supporting hardware and software will become an inexpensive design element that engineers can incorporate into a host of future products.

Not the only game in town

Note that other manufacturers already have non-PCMCIA credit-card-sized memories available for niche applications. For example, Dallas Semiconductor designed such a memory for security applications. The company rates its memories for 50,000 insertions and withdrawals—far more than the PCMCIA-spec cards can withstand. These memories have only five contact pins. The company forms the contact pins from an extra-thick layer of a proprietary alloy.

Mitsui offers credit-card-sized memories that have no contacts whatsoever. They feature serial access at 500k bps and come in 8k, 32k, or 128k bytes of battery-backed or CMOS RAM. Prices start at \$50.

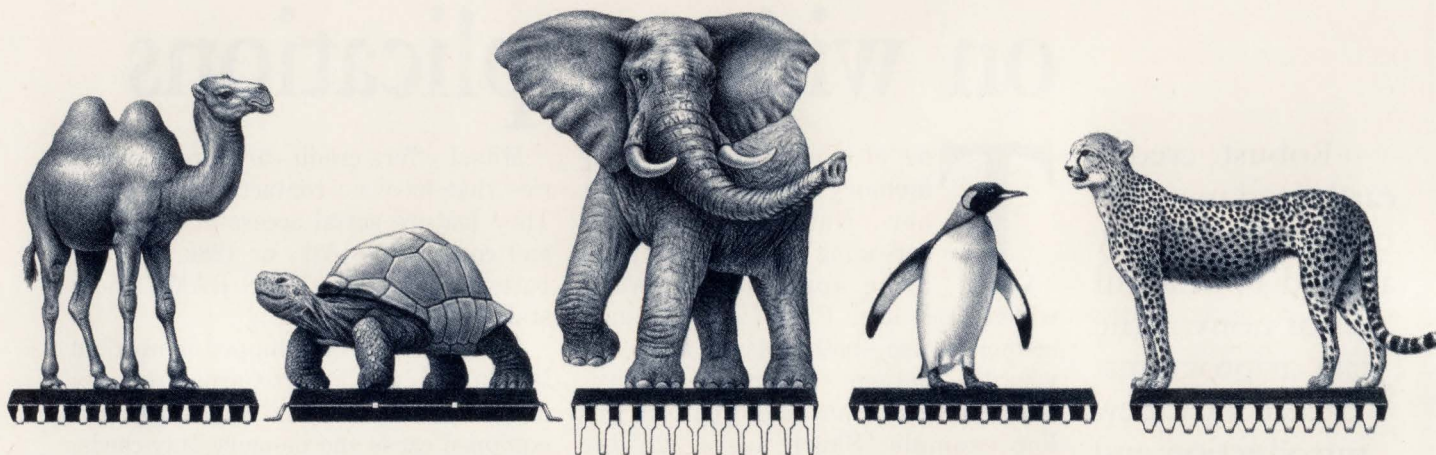
Schlumberger has shipped more than 50,000,000 of its Smart Cards primarily in Europe. This series includes both μ P-equipped cards and memory-only cards. Most of the company's credit-card-sized memory cards hold only a few hundred bytes—a small multiple of the data that a magnetic-stripe card holds. Similarly, Datakey has security-oriented credit-card-sized memories that extend its line of electronic keys.

If present trends continue, expect



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1-Meg SRAM

Model	Speed (ns)	Packaging	Data Retention Current	Special Features	Availability
128Kx8 -- CXK581000P	100/120	DIP 600mil	L/LL	B/X	Now
-- CXK581000M	100/120	SOP 525mil	L/LL	B/X	Now
-- CXK581100TM	100/120	TSOP (normal)	L/LL	B/X	Now
-- CXK581100YM	100/120	TSOP (reverse)	L/LL	B/X	Now
-- CXK581001P	70/85	DIP 600mil	L/LL		Now
-- CXK581001M	70/85	SOP 525mil	L/LL		Now
-- CXK581020SP	35/45/55	SDIP 400mil			Now
-- CXK581020J	35/45/55	SOJ 400mil			Now
128Kx9 -- CXK77910J	17/20	SOJ 400mil		Sync ASM	3/Q '91
256Kx4 -- CXK541000J	25/30/35	SOJ 400mil			3/Q '91

L = Low LL = Low,Low B = 3 Volt X = Extended Temperature

SONY

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TECHNOLOGY UPDATE

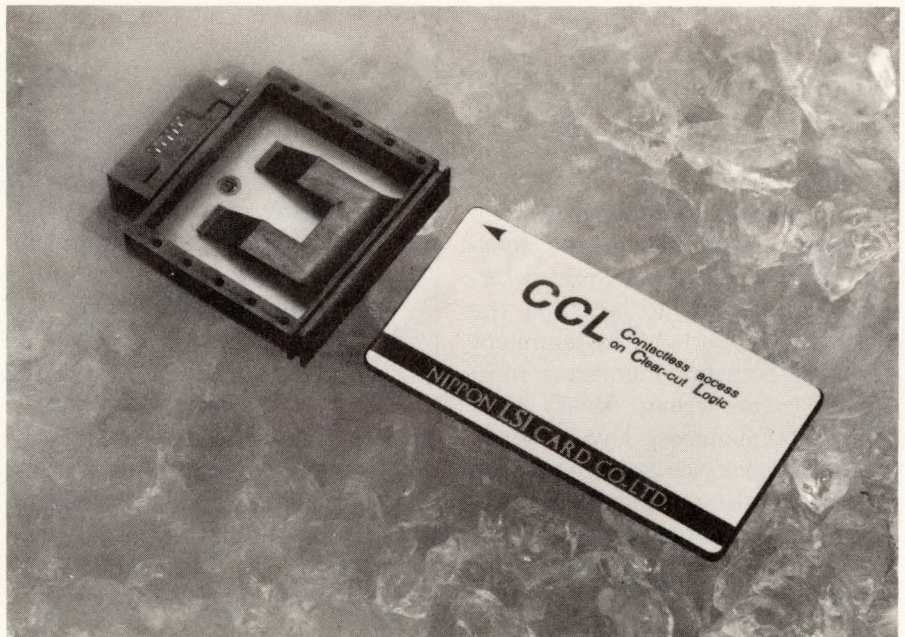
Credit-card-sized memories

several industry-standard credit-card-sized memories to serve most applications. And, expect a gaggle of specialized devices for niche applications, such as security and ID cards.

Sticker shock

Right now, as is common for recently introduced electronics, the higher-capacity cards have prices that are orders of magnitude higher than the cost of their constituent parts. For example, Sharp's RAM ICs used in these memories sell for \$1/Mbit. Expect credit-card-sized memory prices to drop rapidly.

Mitsubishi has PCMCIA static RAM (SRAM) versions of these memories ranging from 128k bytes to 2M bytes. They also have dynamic RAMs (DRAMs) ranging from 512k bytes to 3M bytes, EEPROMs ranging from 8k bytes to 192k bytes, one-time programmable ROMs ranging from 128k bytes to 2M bytes, and masked ROMs ranging from 512k bytes to 8M bytes. Prices start at \$80 for



Although all other credit-card-sized memories have some number of contact pins, the Mitsui (Nippon) LSI card has no contacts.

128k bytes, \$121 for 256k bytes, \$208 for 512k bytes, \$613 for 1M byte, and \$1163 for 2M bytes.

Shigma (Fujisoku of Japan) has a 1M-byte PCMCIA SRAM credit-card-sized memory that costs \$100

(1000). Intel, on the other hand, advocates credit-card-sized memories bearing flash memories. Intel cards have a 250-nsec access time and block-erase times of one or two seconds. The 1M-byte cards cost \$298

For more information . . .

For more information on credit-card memories, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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TECHNOLOGY UPDATE

Credit-card-sized memories

(1000), and the 4M-byte cards cost \$1198 (1000). Intel also has a flash-memory developer's kit for \$500. Databook can supply PCMCIA "disk drives" ranging from \$89 to \$399.

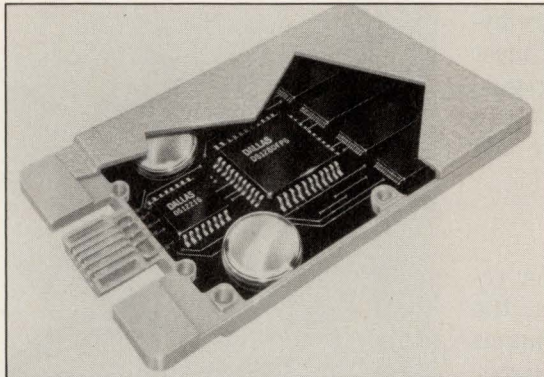
Credit-card-sized memories will supplant rotating memories in some applications. But don't count rotating memories out just yet. Like the glass CRT, reports of the imminent death of rotating memories have proven to be wrong. Every time solid-state memories have made a jump in capacity or executed a drop in price, rotating memories have responded with a doubling in capacity and a halving in size. Credit-card-sized memories will have their biggest impact in applications that rotating memories cannot serve, rather than driving rotating memories from their own turf.

Application areas

Credit-card-sized memories are also more expensive than rotating memories, and therefore not appropriate for all removable-memory applications. Right now, these memories have two possible applications: industrial and commercial.

Credit-card-sized memories are good in industrial applications because they are solid state, and therefore much more rugged and reliable than rotating memories. You could, for example, design credit-card-sized memories into vehicular, factory-floor, and high-reliability medical applications.

For commercial applications the small size and low power consumption of credit-card-sized memories predominate. Consider laptop computers, for example. Low-power components need only a small battery. A smaller battery, in turn, permits a smaller, lighter computer. In addition to laptops, these memories should also prove useful for inventory loggers, calculators, and other small, computerized



Able to withstand 50,000 insertions and withdrawals, Dallas Semiconductor's proprietary 500k-byte, nonvolatile-RAM Cybercard has five pins, compared to more than 60 for most other credit-card-sized memories.

implements. Indeed, the highest-volume existent application for PCMCIA cards is for Sharp's Wizard series of pocket-sized business computers.

Other than roughly similar outlines, the available and proposed credit-card-sized memories have little in common. They differ in the IC technology they employ, in their pinouts and other physical characteristics, and in their software structures.

Even within a given standard, variations exist. The PCMCIA standard is an umbrella that allows two card thicknesses: regular and pregnant. Pregnant cards contain UV-erasable PROMs and have a removable window cover so that you can erase the EPROMs. The standard also allows all common nonvolatile memory technologies: battery-backed RAM, ROM, EPROM, EEPROM, and flash EEPROM. Each of these technologies mandate significantly different access times and methods for writing and erasing memory contents.

The PCMCIA standard further allows a variety of data formats. All these allowable, noncompatible variations arise from the fact that the PCMCIA members have differing requirements and also because some have existing formats and technologies that they do not care to change.

Applications can use the credit-card-sized memory in three ways.

One approach replaces a floppy disk with a credit-card-sized memory. This approach entails all the software overhead of a file-management system, such as device drivers.

Another approach is to simply use the credit-card-sized memory as a repository, or log, of raw data. This approach requires only simple read/write routines. Third, you can run programs directly out of credit-card-sized memory space. This approach offers flexibility to simple factory-floor computers, such as industrial versions of the IBM PC, which now tend to have "hard-wired" software dedicated to a single program.

Beyond the straightforward, common-sense application for these memories, the cards' designers may have done, as engineers often do, something very important while trying to do something else. Running programs directly out of credit-card-sized memory space offers a solution to the problem of software piracy by thwarting the threat that centralized data bases pose to our civil liberties. Butressed by appropriate new privacy laws, credit-card-sized memories could easily allow individual citizens to centralize and control others' access to private data. **EDN**

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packaging and offer user programmable features such as resolution, bandwidth (to 1060Hz), and analog velocity output scaling. It accomplishes full programmability, and power supply decoupling with only seven external passive components. Resolution programming allows selection of 10,12,14, or 16 bits, with accuracies to 2.3 minutes. This feature combines the high tracking rate of a 10 bit converter (up to 2300 rps) with the precision and low-speed velocity resolution of a 16 bit converter in one package.

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Individual models are as follows: The RDC-19220 is in a 40 pin DIP package with differential inputs and ± 5V power supplies; The RDC-19221 is in a 28 pin DIP package with single-ended inputs and ± 5V power supplies; The RDC-19222 is in a 44 pin PLCC package with differential inputs and +5V or ± 5V power supplies; The RDC-19223 is in a 40 pin DIP package with single-ended inputs and +5V or ± 5V power supplies.

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For additional information, contact Mike Johnson at 1-800-DDC-1772, ext. 384. □

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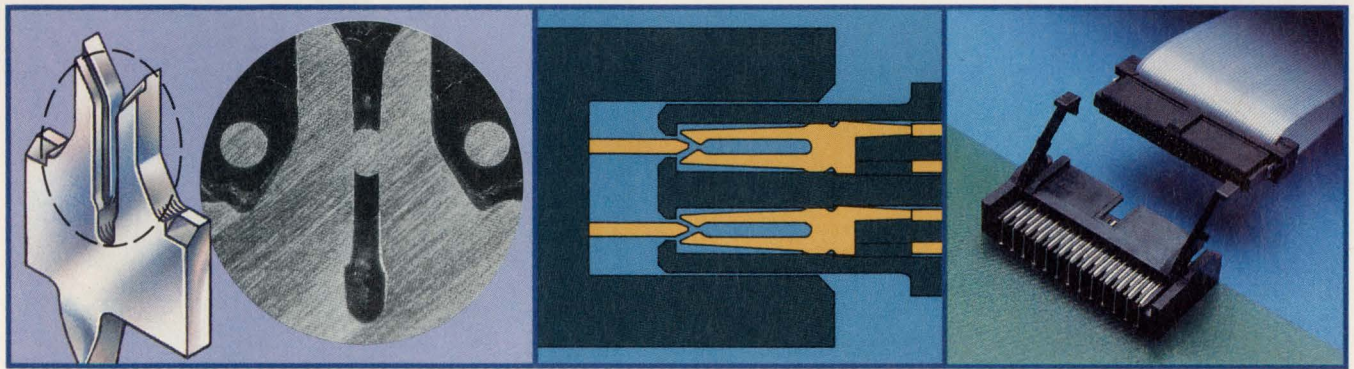
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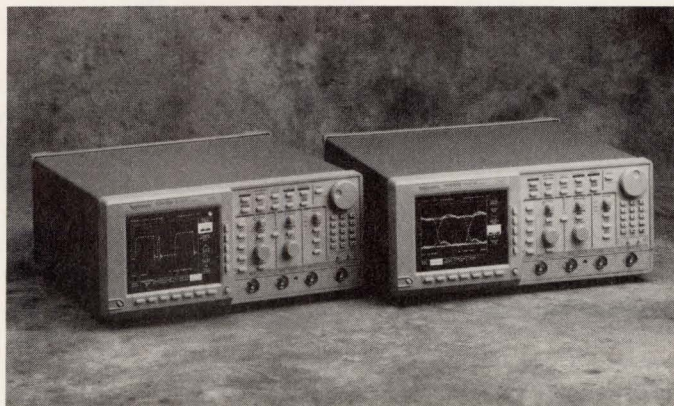
Compact, fast-sampling, 500-MHz scopes talk to users in words and pictures

You might say that Tektronix intends its TDS series of compact, high-speed-sampling, 500-MHz-bandwidth digital storage scopes to do for the instrument manufacturer what the K car (or maybe the minivan) did for Chrysler Corp. If you look at the scopes' combination of features and specs, you can legitimately call these products revolutionary—even

though, with one possible exception, no single feature is a first. Considering their high performance and middle-of-the-road pricing, the scopes offer a good value. (A 2-channel unit costs \$9490; a 4-channel unit costs \$13,900. Delivery takes six weeks ARO.)

The one feature that probably is unique in the 500-MHz DSOs is the 10- μ V resolution. This spec requires a little explanation. These scopes have 8-bit ADCs. (Data on effective bits vs frequency is not yet available.) You can obtain the extreme resolution only if the scopes are placing no more than 1M sample/sec in their waveform memories. In this case, real-time DSP (using the proprietary Tri-Star μ P also used in the vendor's much higher priced DSA 601/602) increases the scopes' resolution to 12 bits and allows vertical-scale expansion.

The scopes achieve the resolution enhancement by sampling at high rates and creating a short-term average in real time. Only the average goes into waveform memory, so av-



An unusual, yet intuitive user interface based on both text and graphics distinguishes Tektronix's TDS series of digital scopes.

eraging exacts no penalty in memory depth; at maximum sensitivity, it lets you clearly see 10- μ V signals.

Such high sensitivity is of interest mainly to people doing low-level analog design. Other features will interest a wider audience. The triggering is much like that on logic analyzers, allowing very complex sets of conditions to trigger a sweep. You can trigger on logical combinations of inputs, logical combinations qualified by a clock, undersized (runt) pulses, pulses whose width exceeds a minimum you set, and much more. The scopes perform waveform math and make 22 pre-programmed measurements. As you would expect, the scopes produce hard copy on graphics-capable printers, and they connect to computers and measurement systems via an IEEE-488.2 interface.

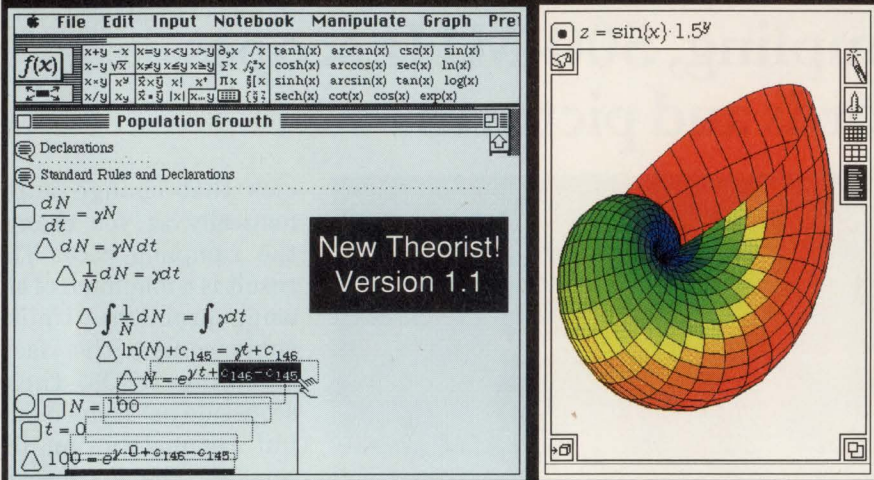
The fast DSP chip provides the quick response (also called "analog feel") of the company's DSA units. Lowpass input filters (which the company says lack sufficient attenuation to qualify them as true antialiasing filters) have corner frequen-

cies that change automatically as you change the sampling rate. The result is a minimum of aliasing problems. Unlike some competitive fast-sampling DSOs, these scopes do not include output reconstruction filters. At the expense of bandwidth, such filters improve repeatability in displays of single-shot pulse edges.

The standard memory depth is 15k samples/channel. An option (\$1500 on the 2-channel unit; \$1950 on the 4-channel unit) increases the memory depth to 50k samples/channel. These products indicate an industry trend toward deep memory in wide-band scopes. A competitor has been offering 50k-sample waveform memory in such scopes for several years.

You probably noted that the description of the units as high-speed sampling scopes failed to mention a maximum sampling rate. The reason for the omission is the complexity of the spec. These scopes can increase their single-shot sampling rate on one channel by interleaving samples from an ADC they borrow from an unused channel. Some of the vendor's other high-performance scopes also operate this way. Each ADC converts at a maximum speed of 250M samples/sec. Hence with one channel active, the 2-channel unit can take 500M samples/sec, and the 4-channel unit can take 1G sample/sec. When you view repetitive waveforms, the effective sampling rates are much higher.

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Another unusual feature is the user interface; its operation appears to be highly intuitive. A complete set of rotary controls is available, but you use only one set for all the vertical channels—even on the 4-channel unit. (The 2-channel unit will display two live waveforms and two computed waveforms.) Push-buttons let you select which channel you are controlling. The monochrome CRT uses high-resolution raster technology and displays white on black.

There are rows of buttons along the right-hand and lower edges of the CRT. Often, making a menu choice involves pushing a button from each group, but there is no further nesting of menus. A combination of words and pictures describes many of the menu selections. Whenever icons appear, words always accompany them.

At the right side of the front panel, a calculator-sized numeric keypad permits quick entry of numeric values—for example, large offsets on the X and Y axes. If you don't know what numbers to enter, as is often the case, you can adjust the large rotary control just above the keypad until you reach the value you need.

Internally, most of the scope is on one densely packed pc board, on which are surface-mounted proprietary chips, multichip modules that contain other proprietary chips, and discrete components. Battery-backed CMOS RAM stores all trim values. A high-resolution DAC converts the stored values and sends the analog levels to S/H circuits. No mechanical adjustments at all are necessary for potentiometers or trimmer caps. The company claims that although trimming with multiple DACs of equivalent resolution would have done away with the S/H circuits, such a design approach would have been much more expensive.—**Dan Strassberg**

Tektronix Inc, Box 19638, Portland, OR 97219. Phone (800) 426-2200.

Circle No. 730

Actual size

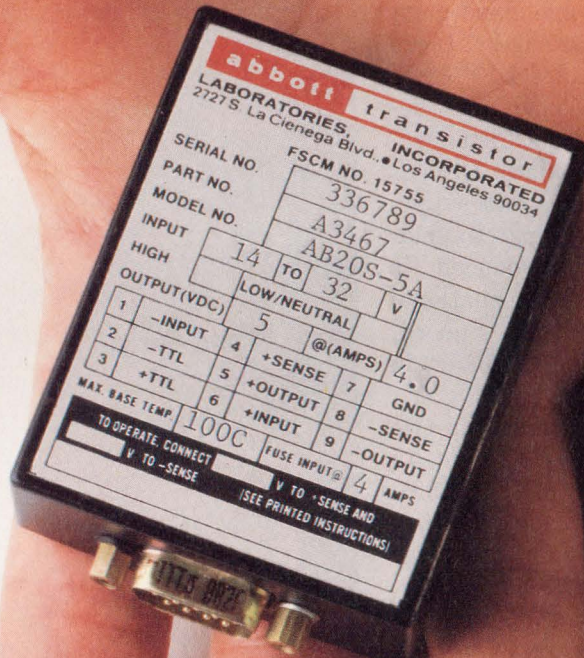
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Floating-point DSP chip runs at 60M flops and addresses 4G words of data memory

There's little left to debate on the merits of floating- and fixed-point math DSP operations. Today there are many floating-point DSP chips that compete with fixed-point devices on price and performance. Now you can add Analog Devices to the list of companies that supply floating-point DSP chips. In mid-May, the company introduced its ADSP-21020 at the International Conference on Acoustics, Speech, and Signal Processing (ICASSP) in Toronto.

The DSP chip is available in two speed grades that operate at 15 MHz (\$195) or 20 MHz (\$265). Prices are for single chips. The 15-MHz chip's floating-point processor operates at a peak rate of 45M flops, and the 20-MHz part operates at 60M flops. The company expects to supply a 25-MHz version of the chip late in 1991. The floating-point processor operates with both 32- and 40-bit floating-point values in the standard IEEE numeric format. The chip also operates on 32-bit fixed-point values, and it can accumulate a result with as many as 80 bits. Because the DSP chip furnishes an ALU and a multiplier that are independent of one another, the chip can simultaneously execute an addition and a multiplication operation—both of which are key to DSP operations. In comparison with other DSP chips, the 20-MHz version of the chip performs a 1024-point complex fast-Fourier transform (FFT) in 0.96 msec.

The company also uses a formula to compute the performance of the ADSP-21020 relative to a Texas Instruments TMS320C30-40 DSP chip. The relative "C30-equivalent" spec is given as "80 C30 MFLOPS" for a 1024-point complex FFT run



A processor and memory architecture crafted for use with high-level languages let C and Numerical-C compilers produce clean and efficient code for DSP operations in the ADSP-21020 chip.

on each DSP chip. We urge caution in applying such benchmarks. After all, the performance of a variety of chips running FFT benchmark programs may not be applicable to all possible DSP tasks. In the end, how a given DSP chip operates depends to a great extent on your application, on the limits of your hardware and software, and on your development tools.

The ADSP-21020 employs a modified Harvard architecture in which the data memory stores data, and the program memory stores both instructions and data. Thus the chip can fetch information from its data memory, information from its program memory, and an instruction from its internal cache, all within a single cycle. Because circular buffers are frequently used in

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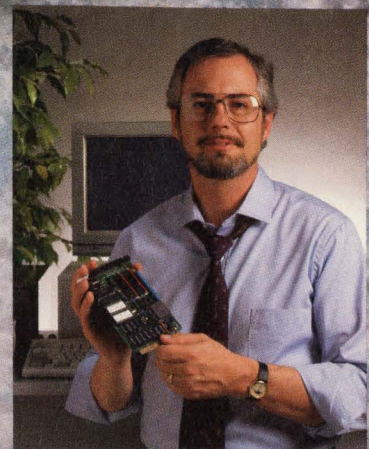
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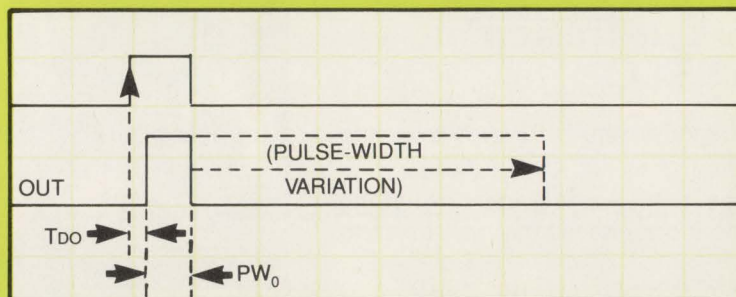
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DSP operations such as filtering and running FFTs, the chip lets you implement circular buffers in its external memory. The device handles buffer-address wraparound—the point when the buffer pointer reaches its maximum value and must be reset to the buffer's starting address. Circular buffers aren't constrained to specific places in memory, but can start at any address and can be any length.

The chip's program memory can contain as many as 16M words (16 bits per word), and its data memory can contain as many as 4G words. For execution at a 20-MHz clock frequency, you'll need DRAMs (dynamic RAMs) with 35-nsec access times for zero-wait-state operation of the processor. Wait states are programmable, and the chip supports page-mode DRAM addressing.

Besides the chip, the company supplies a variety of development hardware and software—as do third-party suppliers. The assembler, linker, and assembler package are available for \$995. The programs run on an IBM-compatible PC. For \$500 you can buy a development board that communicates with a host computer over serial I/O lines. The company is also supporting a superset of ANSI C, called Numerical C, which will offer additional vector and matrix operations as part of its language.

—Jon Titus

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Math software runs under MS Windows, handles symbolic math, and accesses handbooks

In many ways the mathematical software package, Mathcad V3.0, is a totally new product. It runs under MS Windows V3.0 and incorporates several features intended to further increase the software's usefulness.

The product's most noticeable feature is its "live-document" interface. Underlying that interface is the premise that engineers and scientists don't want to spend lots of time becoming experts on using the tools they employ to solve problems; they just want to get on with the problem solving.

Much of the other mathematical software targeted at the engineering and scientific communities requires you to study and practice extensively before you become competent enough to apply it successfully. On the other hand, spreadsheets, which are quite popular among engineers, let you get into problem solving quickly enough, but in significant ways are poorly suited to technical work. For example, once you've entered an equation into a spreadsheet, you are hard pressed to recognize it as the equation you know and love (or, perhaps, hate). Using Mathcad, the equations on the screen look the way you're used to seeing them.

You enter your problems in a free-form document in which you can place text and equations. If the solution of a problem is best described in the form of a 2-D or 3-D graph, the software can plot the graph and insert it in the document. If you define a variable at one point

and use it in equations elsewhere, as soon as you change the variable definition you can see the effect of the change throughout the document.

The new MS Windows-based version adds further embellishments. Although different users may argue about which of these added features is the most important, many users are likely to agree that the new version's ability to handle symbolic math is at the top of the list.

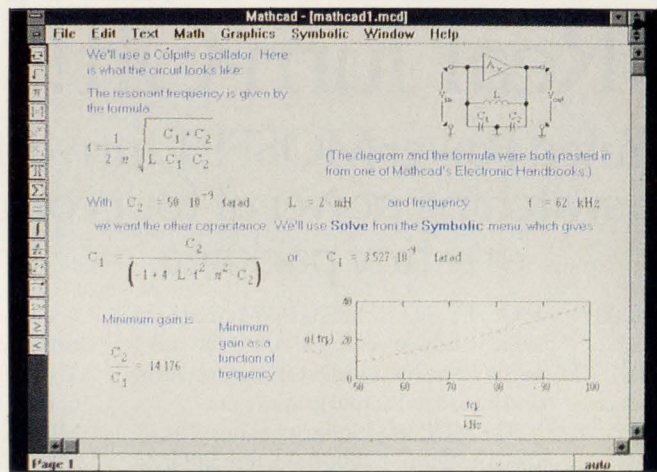
When categorizing mathematical software, the customary approach

Software's (Waterloo, ON Canada) Maple. Mathsoft has signed an agreement with Waterloo Maple to permit the use of Maple routines in Mathcad V3.0.

You don't get all of Maple in Mathcad, but what you do get should satisfy a large group of users' symbolic-solution needs. Although the symbolic solver springs to life at the touch of a mouse button, the integration of the numeric and symbolic capabilities is not totally seamless; you have to shift gears mentally when you change

modes. Mathcad's designers claim that in their testing with users, attempts to force a seamless transition proved more confusing than helpful.

Another major feature of V3.0 is the on-line handbooks. The first of these contains such items as conversion factors and physical constants—for example, the densities of common solids and liquids. Future handbooks will contain much more data and will take advantage



Electronic handbooks in Mathcad V3.0 give you on-line access to a reference library of technical information.

is to divide the packages into numeric and symbolic solvers. Numeric solvers can determine the roots of equations if you supply them with values for all the independent variables. They can even calculate families of solutions over a range of independent-variable values. What they can't do is express answers as equations that contain the independent variables in literal form. To perform the last function, you need a symbolic solver. One of the best known and most respected symbolic solvers is Waterloo Maple

of Windows' hypertext capabilities to permit access to photographic images as well as the numbers, text, line drawings, and graphs of the initial handbook.

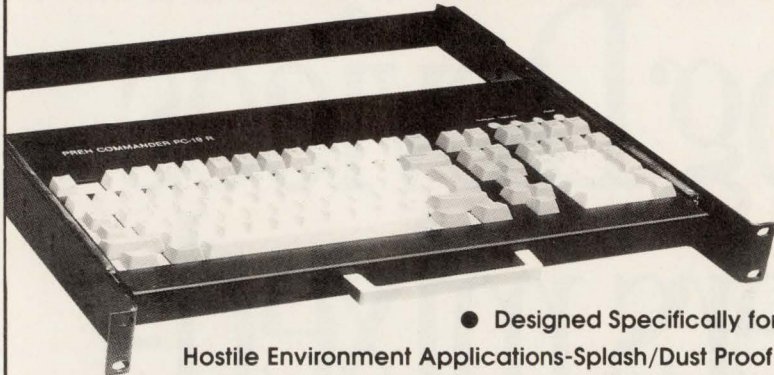
The third significant addition is the package's desktop-publishing capability. (Earlier versions produced documents that looked like the output of a scientific word processor.) The company is quick to point out that the new version is not a desktop publishing program. Anyone who buys it as such will quickly become frustrated by the

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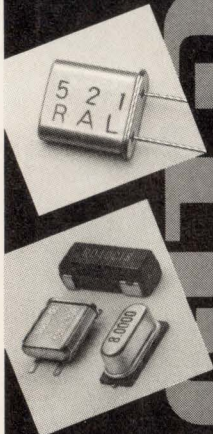
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absence of such features as indexing and footnoting. However, there are enough desktop-publishing features to permit engineers to turn out very attractive reports.

Enough questions have been asked about the operating speed of MS Windows-based products to warrant inquiries about speed each time a Windows-based productivity tool makes it debut. If you run V3.0 and its predecessor on equivalent hardware, and you time the operations, some will be faster and others will be slower. Overall, though, your impression of the new version is likely to be that it is faster, because the operations you focus on, such as graph plotting, are faster.

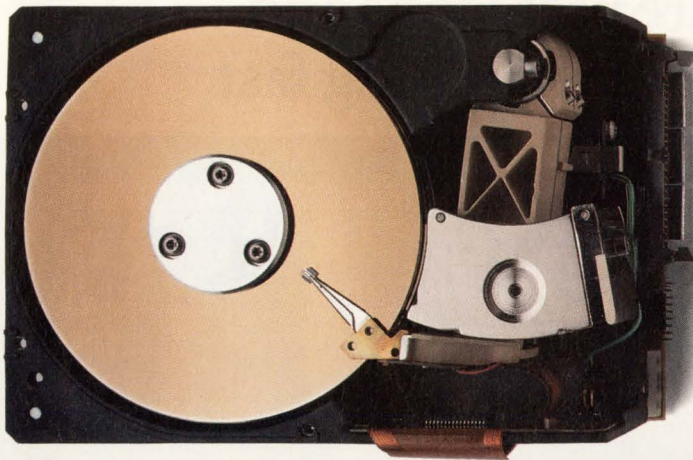
V3.0's added capabilities exact a price in system requirements. Although the new version does not require all of the following hardware, the company does recommend it, and you'll need most of it to run Windows 3.0 acceptably. The items consist of an 80386SX-based PC with 4M bytes of RAM; a display that conforms to the IBM enhanced-graphics-adaptor or video-graphics-array standards (monochrome will do); a numeric coprocessor; a mouse; and a hard disk with 6M to 7M bytes of free space.

The new version can read files created with earlier versions, but these versions cannot load documents produced by V3.0. For users whose hardware does not support V3.0, the company will continue to supply the prior version, V2.5 as well as a version for the Apple Macintosh. Both IBM versions list for \$495; an upgrade from V2.5 to V3.0 costs \$149 (\$99 until June 30, 1991).—**Dan Strassberg**

Mathsoft Inc, 201 Broadway, Cambridge, MA 02139. Phone (617) 577-1017. FAX (617) 577-8829.

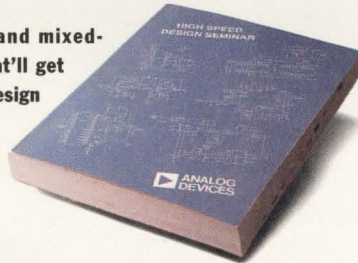
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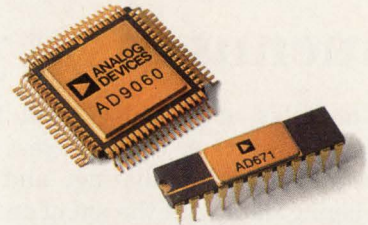


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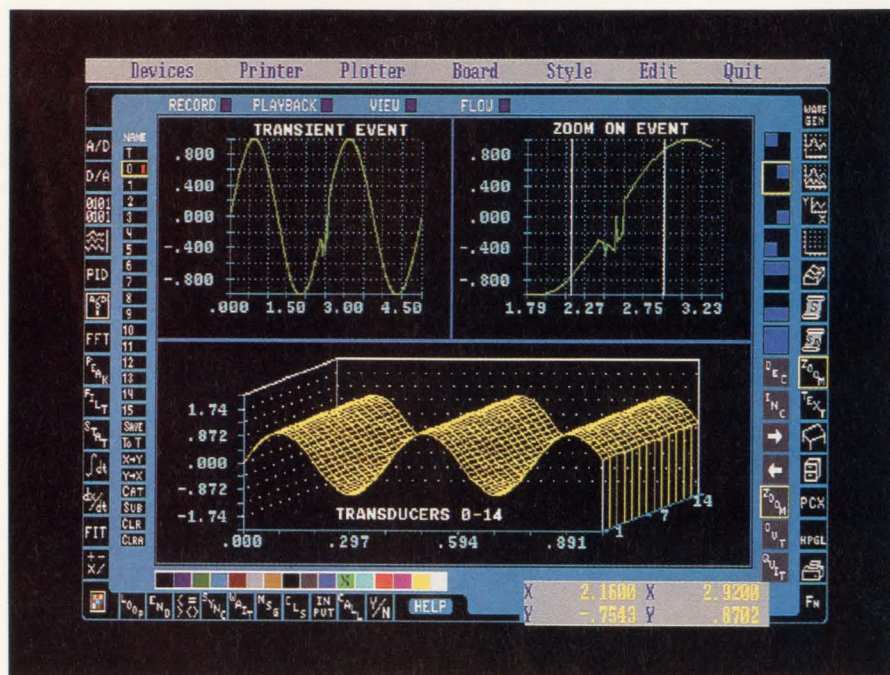
Data-acquisition software uses icons and menus to get your job up and running fast

The folks at Keithley/Asyst Software aver that with Easyst LX, acquiring, manipulating, and displaying data with the aid of an IBM PC or compatible will never be the same. A demonstration of the software suggests that they aren't exaggerating.

If you're skeptical about icons and scoff at packages that base their human interfaces on scores of the tiny pictures, you may be inclined to poke fun at this software. But before you laugh too loudly, take a closer look. The designers of this software have blended images with words in a way that leads you to your objective with a minimum of pain. Each time you position the mouse on an icon, the name of the function it represents appears at the lower-right corner of the screen. If you click a mouse button, a longer description of the function appears in the center of the screen.

You select all of the program's functions by clicking on icons. The icons appear in several columns along the sides of the screen and in a row across the bottom. Except in the runtime mode described below, all of the icons are visible all of the time. The center of the screen is available for displaying data and messages and for displaying and editing procedures you create. The package has extensive graphing capabilities. It can create 2D- and 3-D graphs of several types from acquired data. Its data-manipulation functions include FFTs.

Although the software runs in an interactive mode, you can also use it to generate programs that mechanize complex or repetitive procedures. Several packages that do away with conventional text-based



This waterfall plot allows users of Keithley/Asyst's Easyst LX software to compare data captured by using several channels of an IBM PC-based data-acquisition board.

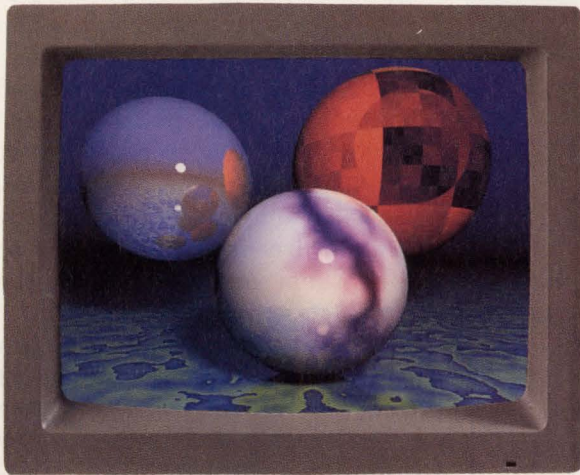
programming replace it with a process of connecting icons to form block diagrams on the screen. This package frees you from the need to create such diagrams. It automates program generation by recording keystrokes and mouse clicks. However, unlike most programs that record keystrokes, the package doesn't reproduce procedures by simply playing back what you typed in. Instead, the software generates an ASCII file from the keystrokes and then compiles the file.

A benefit of this approach is that, unlike strings of keystrokes, the ASCII files are easily readable; they contain mnemonic versions of the commands. The program lets you read the files in three ways. The View function displays a short version; the only editing available in View is deletion of commands. The Edit function displays a version

of the file in which all commands are fully expanded to show arguments. In Edit, you can make any changes you like. You can also view the file as a flowchart. Even if you don't think in flowchart terms, seeing your procedure displayed in this graphical form can simplify debugging. Moreover, the flowcharts provide reassuring evidence to non-programmers that, even without training, they can write programs.

In addition to its interactive and normal-execution modes, the package has a runtime procedure-execution mode. In this mode, a user need not even be aware of the package's presence. (You can set up the runtime mode to make all of the package's usual menus and prompts disappear.) Currently, however, there is no separate runtime-only version of the package. To invoke the runtime mode, the entire pack-

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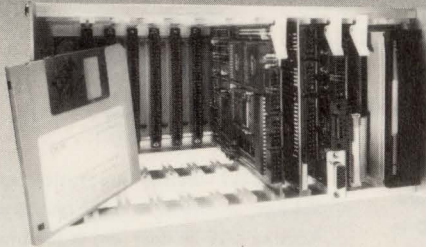
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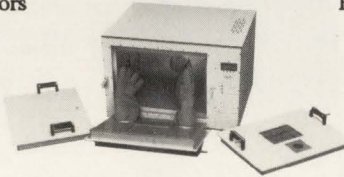
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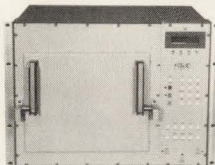


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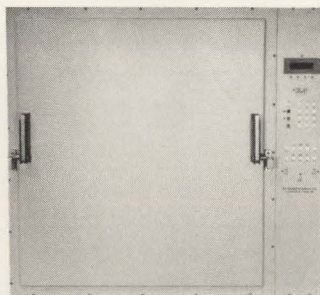


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UPDATE

age must be installed on a user's PC.

Asyst Software has long been an advocate of standardizing the command structure of IBM PC-based data-acquisition boards. So far, the results of the standardization effort have been mixed. But a notable result is a manual that describes how to write drivers for the boards to make them compatible with the firm's data-acquisition software.

Because the package complies with all of the company's rules of its older software, it can use the large library of drivers already written for the firm's older software. Thus, the LX version is compatible with scores of boards. Moreover, the package can import ASCII data files, so you can use it to process and display data acquired elsewhere. It can also import graphic files in .PCX format. This capability can let you display a picture of a pc board on which a technician is to make measurements. On the picture, you can indicate where the technician is supposed to place the test probes, and you can superimpose the measurement results at those points.

Easyst LX even runs on IBM PC-compatible computers whose CPU chip is an 8088. Main memory of 640k bytes and expanded memory (or extended memory configured as expanded memory) of 1M bytes is required, as is a mouse, a numeric coprocessor, and a display that supports the IBM EGA or VGA standards. Monochrome displays must allow the use of a gray scale to represent colors. The package is available now. In single quantities, it costs \$1295. Owners of the original version of Easyst can upgrade for \$530.—**Dan Strassberg**

Keithley/Asyst Software, 100 Corporate Woods, Rochester, NY 14623. Phone (800) 348-0033; in NY, (716) 272-0070. FAX (716) 272-0073.

Circle No. 731

EDN June 20, 1991

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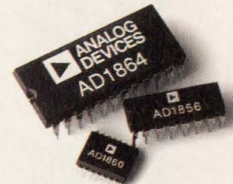
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We're far from your local component boutique. Over half of our \$540 million in revenues comes from international sales. And with manufacturing and stocking facilities on just about every continent, getting products to you quickly is a snap. Plus multiple manufacturing facilities allow us to take advantage of the right talent and processes for the job at hand.



With billions of dollars in annual sales at stake, the video game market is anything but child's play. One leader in this market found that with our DSP they could create more realistic and interactive games. As a result, they're driving away with a bigger share of the market.

Today, Analog Devices offers more cost-effective solutions to your high-performance mixed-signal needs than anyone else. Solutions that are surprisingly affordable, whether they're available off the shelf or developed for a specific application. To find out more about how we can help you develop products more efficiently, or for a free copy of our recent Mixed-Signal Technology white paper, call us at 1-800-262-5643.



SOUNDPORT DACs—We've made these DACs cost-efficient by making them complete with output amplifier, reference and digital logic interface. Perfect for high-fidelity digital audio and multi-media applications, these mixed-signal ICs achieve SNRs as high as 108 dB and THDs as low as 0.0025%.

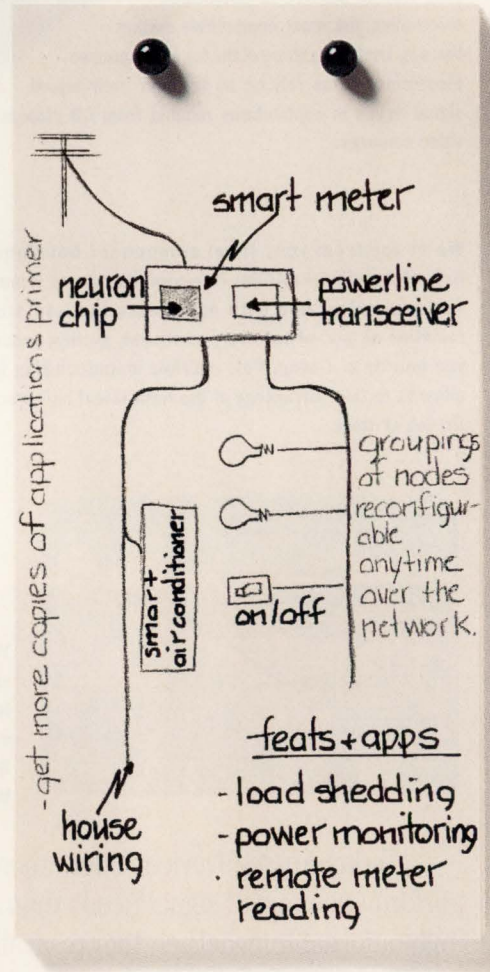
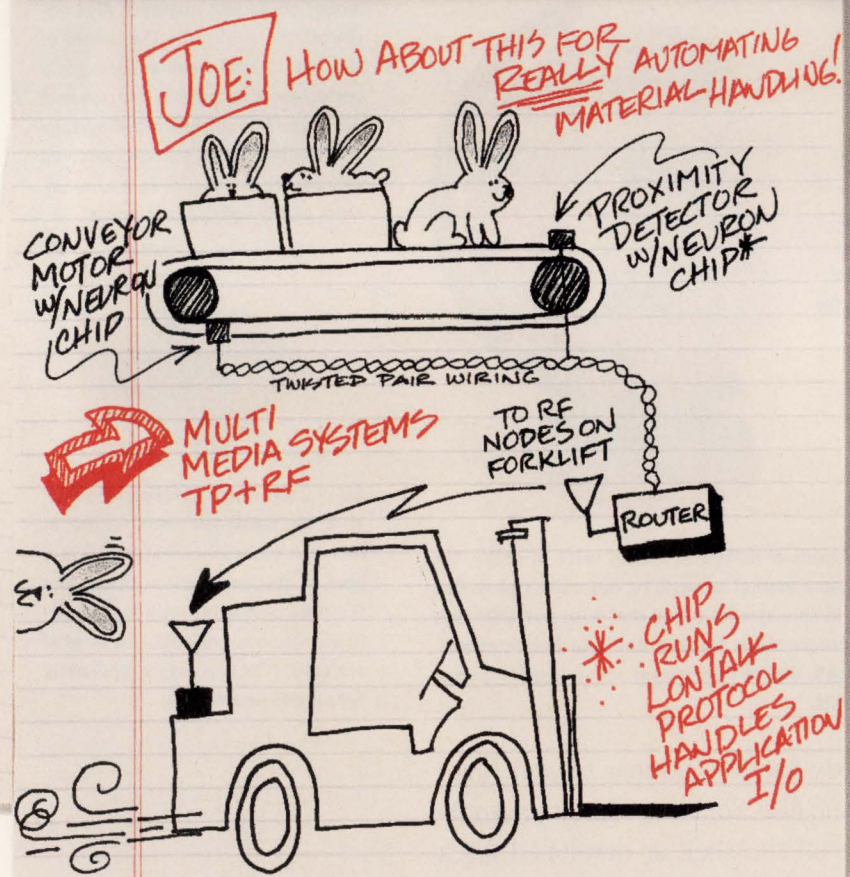
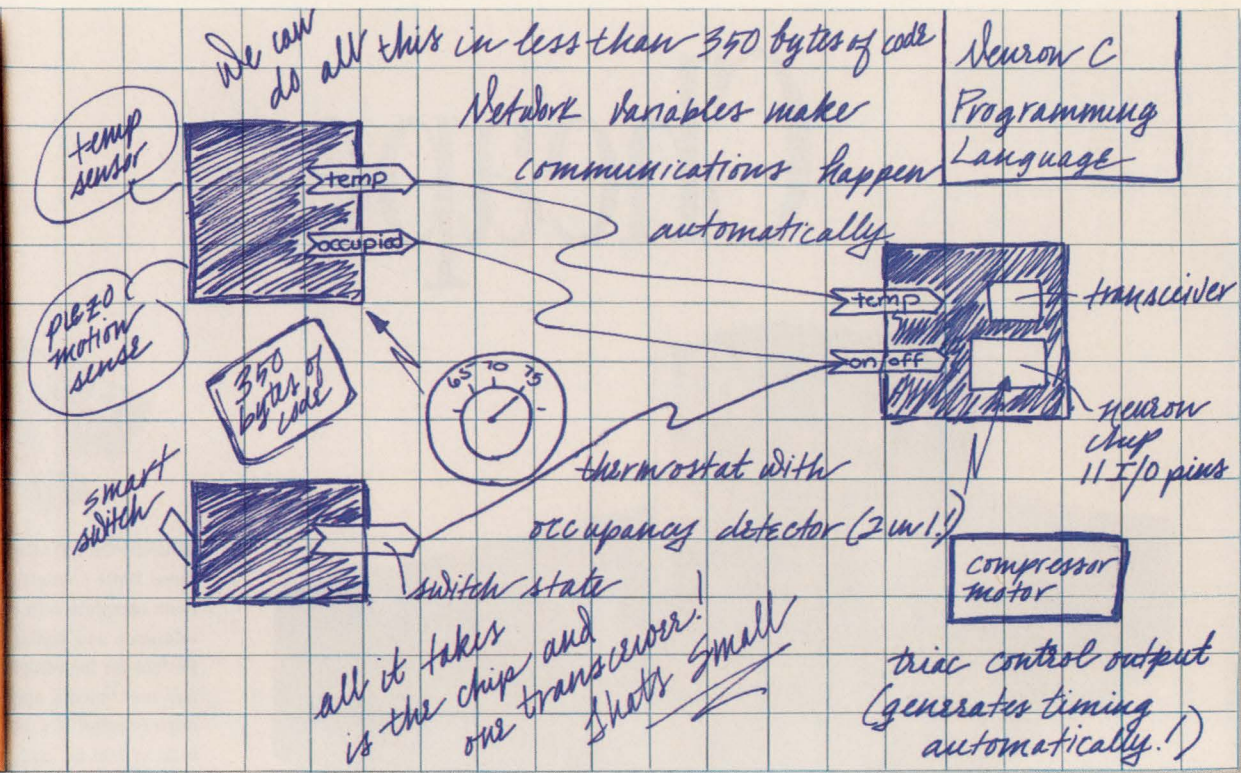


AD712—If you're working in professional audio and compact disc applications, you'll like the sound of this—an IC that combines two high-performance op amps in one compact package. You get low offset voltage and low input bias currents coupled with superb transient response, ambience, clarity and dynamic range.



ADSP-2105—High performance DSP at an incredibly low price. So low, in fact, you can now consider DSP in a host of new applications. And since it's pin-compatible with the ADSP-2101, and code-compatible with all of our other DSP processors, upgrading is easy and inexpensive.





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- 3 CPUS
- RAM, EPROM (ROM)
- COMM & I/O

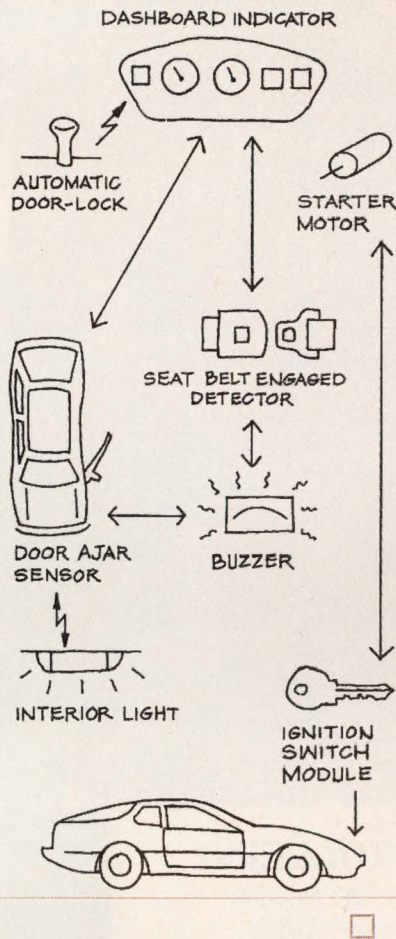
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ARIZONA	Phoenix	June 25
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	Los Angeles	Sept. 25
	Sacramento	Sept. 11
	Santa Clara	Sept. 12
	Woodland Hills	Sept. 10
COLORADO	Denver	June 26
CONNECTICUT	Stamford	June 18
FLORIDA	Ft. Lauderdale	April 9
	Orlando	April 10
GEORGIA	Atlanta	April 11
INDIANA	Indianapolis	June 5
ILLINOIS	Chicago	Sept. 20
MARYLAND	Baltimore	April 2
MASSACHUSETTS	Boston	April 3
	Boston	Sept. 19
MICHIGAN	Detroit	March 28
MISSOURI	Kansas City	March 26
	St. Louis	June 6
NEW HAMPSHIRE	Manchester	May 7
NEW JERSEY	Fairfield	June 12
NEW YORK	Albany	June 19
	Long Island	April 4
	Rochester	June 11
	Tarrytown	May 9
NORTH CAROLINA	Raleigh	Oct. 2
OHIO	Cleveland	March 27
	Dayton	June 4
OREGON	Portland	April 16
PENNSYLVANIA	Philadelphia	May 8
	Pittsburgh	June 20
TEXAS	Austin	Sept. 24
	Dallas/Ft. Worth	May 1
	Houston	April 30
VIRGINIA	Tysons Corner	June 13
WASHINGTON	Seattle	April 17
UTAH	Salt Lake City	June 27
CANADA	Montreal	April 24
	Ottawa	April 23
	Toronto	April 25
	Vancouver	April 18
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	Milan	May 28
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VM40	68040	20	50	4/8/16/32/DRAM	Ext.	1	●	2	EEPROM LXB	5-8	-40 to +85
VM20	68020/68882	4	16/25	1/2/4/8 DRAM	Ext.	2	●	2		4-6	-55 to +125
VMPM 68KD	68030/68882	6	16/25	0.5-3 SRAM	Ext. or Battery	0.5	●	2		10-12	-55 to +125
VMPM 68KC-2	68020/68882	4	12/16/25	0.5-3 SRAM	Ext. or Battery	0.5	●	2		9-11	-55 to +125
VSBC-1	68HC000	1	12/16	0.1-1 SRAM	Ext. or Battery	0.5	●	2	SCSI	4	-40 to +85
VSBC-2	68HC000	1	16	0.1-1 SRAM	Ext. or Battery	1	●	6		2	-55 to +125
VSBC-3	68HC000	1	16	0.1-1 SRAM	Ext. or Battery	1	●	4	20x TTL	3	-55 to +125

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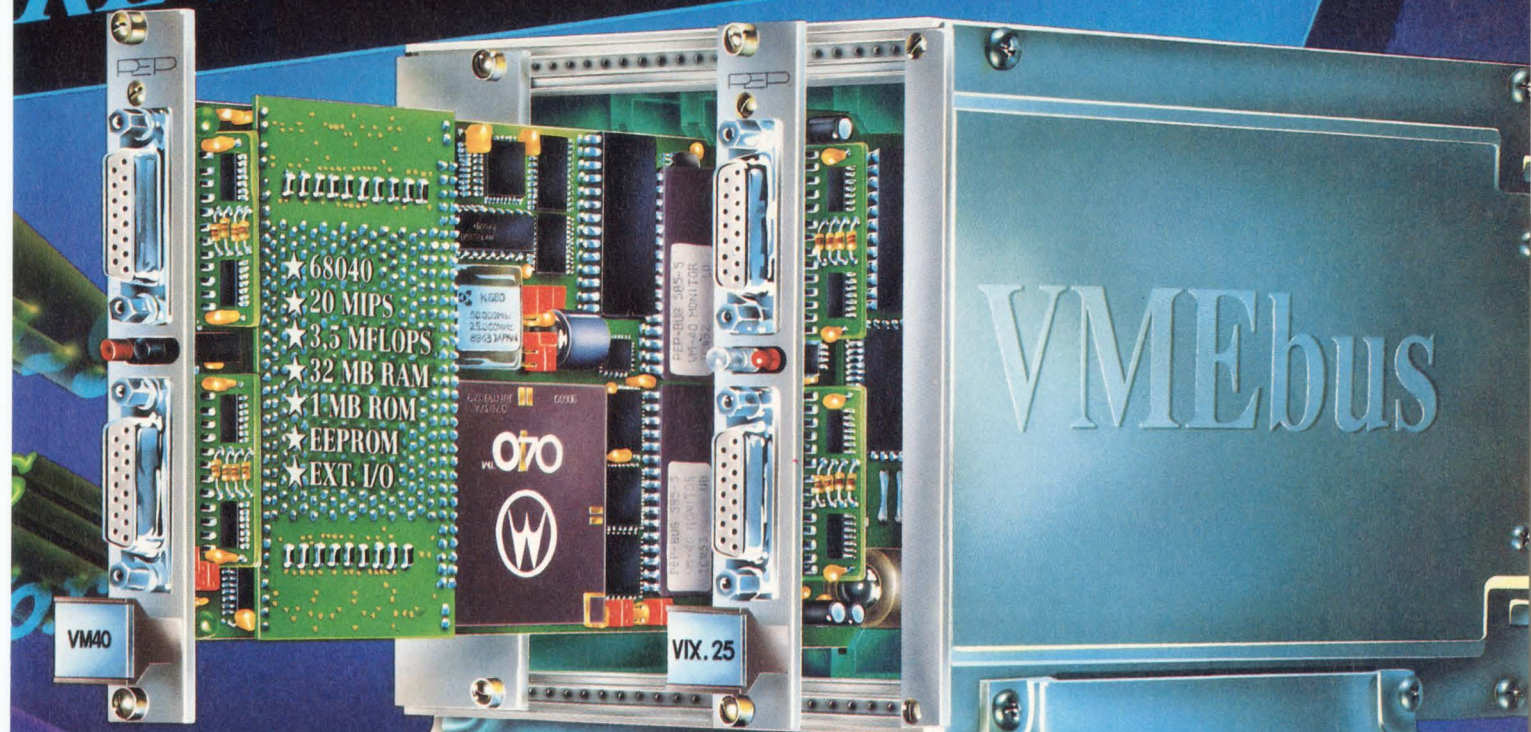
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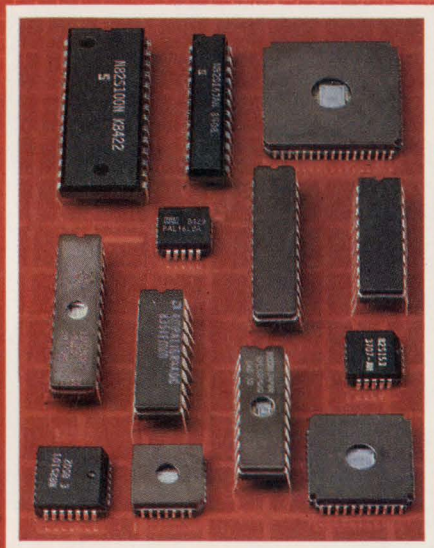
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ZL30A

Power in design Speed in production



Stag's ZL30A offers total PLD programming support

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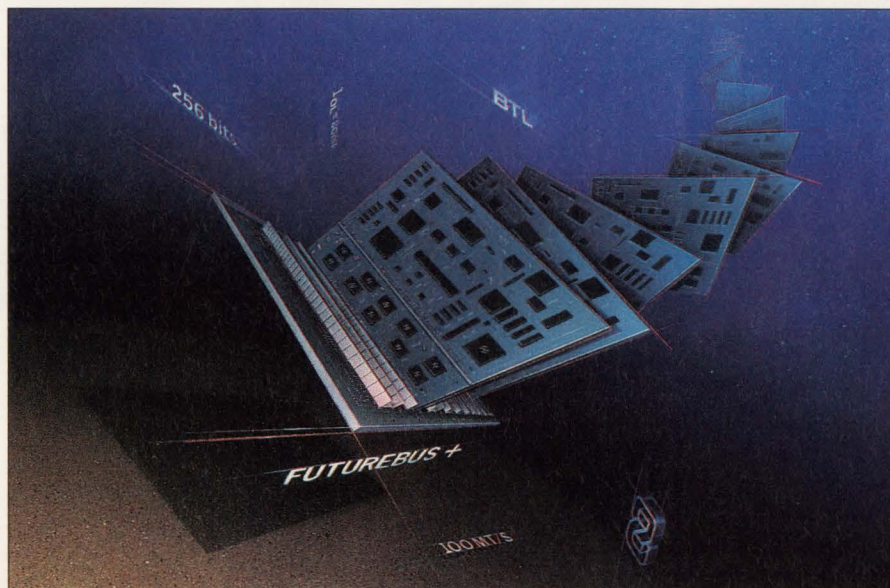
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National has long been the industry leader in BTL and mixed analog + digital technology. Now we've drawn on that heritage to make the most highly integrated Futurebus + ICs available today. We've also put together a full range of development tools to help you put that chipset to work. And the entire package is available now.

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With our new chipset, Futurebus + gives you more bandwidth for your money, making it—for the first time—fully cost-competitive with VME and Multibus®. In addition to an Arbitration Controller, our chip-set contains four advanced BTL devices: two 9-bit Data Transceivers (latched and unlatched), a Handshake Transceiver, and an Arbitration Transceiver.

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- Glitch filters (to eliminate wire OR-ing effects)
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Providing a broad range of development tools.

Start with our Designer's Handbook, with a slave-memory-board application note, product data sheets, and application notes on BTL design technology. Other tools include wire-wrap

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LEADTIME INDEX

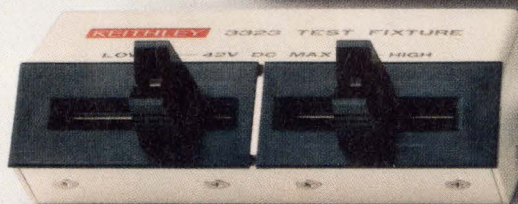
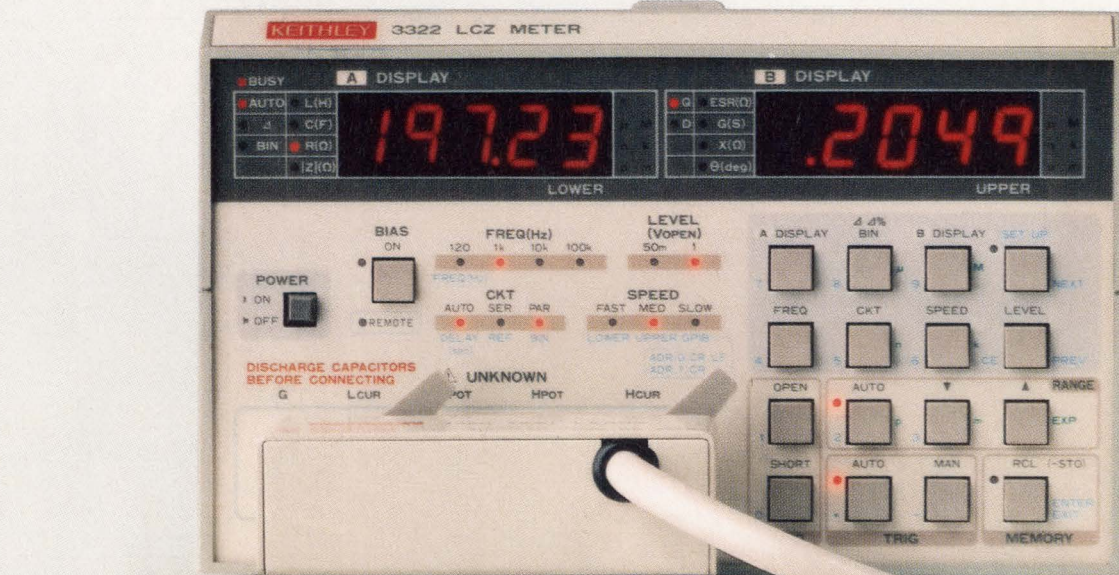
Percentage of respondents

ITEM	Percentage of respondents						Average (weeks)	
	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Last month's average (weeks)	Average (weeks)
TRANSFORMERS								
Toroidal	0	45	28	27	0	0	7.7	8.2
Pot-Core	0	27	36	27	10	0	10.4	6.4
Laminate (power)	0	25	42	25	8	0	10.0	6.5
CONNECTORS								
Military panel	0	40	20	40	0	0	8.9	7.9
Flat/Cable	15	46	39	0	0	0	4.4	4.9
Multi-pin circular	0	45	36	19	0	0	7.1	7.4
PC (2-piece)	9	46	45	0	0	0	4.9	4.7
RF/Coaxial	0	50	40	10	0	0	6.2	6.6
Socket	22	39	39	0	0	0	4.2	4.3
Terminal blocks	12	41	41	6	0	0	5.4	7.0
Edge card	8	53	31	8	0	0	5.3	4.9
D-Subminiature	7	43	50	0	0	0	5.2	6.6
Rack & panel	0	33	50	17	0	0	7.6	6.3
Power	0	60	40	0	0	0	4.9	6.3
PRINTED CIRCUIT BOARDS								
Single sided	0	71	29	0	0	0	4.4	4.0
Double sided	0	66	29	5	0	0	5.0	3.8
Multi-layer	0	53	40	7	0	0	5.8	4.2
Prototype	13	74	13	0	0	0	3.2	2.9
RESISTORS								
Carbon film	40	30	30	0	0	0	3.2	3.5
Carbon composite	19	50	25	6	0	0	4.4	5.5
Metal film	32	42	26	0	0	0	3.3	4.2
Metal oxide	24	41	35	0	0	0	4.0	6.4
Wirewound	0	40	50	10	0	0	6.7	7.1
Potentiometers	21	47	26	6	0	0	4.4	5.2
Networks	13	49	38	0	0	0	4.5	4.3
FUSES								
	55	18	27	0	0	0	2.6	4.1
SWITCHES								
Pushbutton	11	55	28	6	0	0	4.8	4.1
Rotary	0	42	33	25	0	0	7.7	7.0
Rocker	8	42	33	17	0	0	6.5	6.0
Thumbwheel	0	45	36	19	0	0	7.1	8.9
Snap action	8	33	50	9	0	0	6.3	6.8
Momentary	0	50	40	10	0	0	6.2	4.1
Dual-in-line	0	64	27	9	0	0	5.4	6.7
WIRE AND CABLE								
Coaxial	25	33	33	9	0	0	5.0	5.8
Flat ribbon	60	13	27	0	0	0	2.5	4.7
Multiconductor	47	13	27	13	0	0	4.5	4.9
Hookup	79	14	7	0	0	0	0.9	1.8
Wirewrap	38	37	25	0	0	0	3.1	2.8
Power cords	28	33	33	6	0	0	4.5	6.0
POWER SUPPLIES								
Switcher	0	19	45	36	0	0	9.7	13.3
Linear	0	18	36	36	10	0	11.5	9.4
CIRCUIT BREAKERS								
	27	27	36	10	0	0	5.2	6.4
HEAT SINKS								
	36	45	19	0	0	0	2.8	4.0
BATTERIES								
Lithium coin cells	43	43	14	0	0	0	2.4	4.3
9V alkaline	60	20	20	0	0	0	2.1	1.1
Real-time clock back-up	0	75	25	0	0	0	4.2	2.9
RELAYS								
General purpose	20	40	20	20	0	0	5.8	5.2
PC board	8	46	8	38	0	0	7.9	5.7

ITEM	Percentage of respondents						Average (weeks)	
	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Last month's average (weeks)	Average (weeks)
Dry reed	0	33	50	17	0	0	7.6	6.3
Mercury	0	50	0	50	0	0	9.2	5.4
Solid state	13	25	0	62	0	0	10.3	5.4
DISCRETE SEMICONDUCTORS								
Diode	36	19	27	18	0	0	5.5	4.5
Zener	39	28	22	11	0	0	4.3	4.4
Thyristor	25	31	25	19	0	0	5.8	6.0
Small signal transistor	27	20	33	20	0	0	6.3	4.2
MOSFET	10	30	10	50	0	0	9.4	8.2
Power, bipolar	18	28	27	27	0	0	7.1	5.4
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	20	40	20	20	0	0	5.8	9.4
CMOS	17	38	28	17	0	0	6.0	7.9
TTL	29	35	29	7	0	0	4.4	5.7
LS	20	40	33	7	0	0	4.9	5.1
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	8	50	33	9	0	0	5.5	3.9
OP amplifier	13	40	33	14	0	0	6.0	5.5
Voltage regulator	13	40	40	7	0	0	5.4	4.2
MEMORY CIRCUITS								
DRAM 16K	0	40	20	40	0	0	8.9	15.5
DRAM 64K	0	42	29	29	0	0	8.0	7.1
DRAM 256K	0	37	25	38	0	0	8.9	4.2
DRAM 1M-bit	11	33	33	23	0	0	7.1	4.6
SRAM 4K x 4	0	40	40	20	0	0	7.4	7.9
SRAM 8K x 8	0	50	30	20	0	0	6.9	7.6
SRAM 2K x 8	0	44	33	23	0	0	7.5	9.8
ROM/PROM	0	33	17	50	0	0	10.1	7.3
EPROM 64K	11	33	33	23	0	0	7.1	5.8
EPROM 256K	0	45	28	27	0	0	7.7	7.4
EPROM 1M-bit	0	43	0	57	0	0	10.1	9.2
EEPROM 16K	0	33	44	23	0	0	8.0	11.7
EEPROM 64K	0	29	42	29	0	0	8.7	11.7
DISPLAYS								
Panel meters	17	33	17	33	0	0	7.4	7.9
Fluorescent	0	0	40	60	0	0	12.5	15.5
CRT 12-in. mono	33	0	0	67	0	0	10.3	7.7
LED	38	31	8	23	0	0	5.1	5.6
Liquid crystal	0	25	25	50	0	0	10.4	12.5
MICROPROCESSOR ICs								
8-bit	9	36	28	27	0	0	7.5	7.5
16-bit	0	42	25	33	0	0	8.3	8.7
32-bit	0	40	20	40	0	0	8.9	8.7
FUNCTION PACKAGES								
Amplifier	0	29	57	14	0	0	7.5	7.8
Converter, A/D	0	30	30	40	0	0	9.4	10.3
Converter, D/A	0	33	23	44	0	0	9.6	11.6
LINE FILTERS								
	25	13	37	25	0	0	7.2	9.2
CAPACITORS								
Ceramic monolithic	32	23	31	14	0	0	5.3	3.6
Ceramic disc	37	26	26	11	0	0	4.5	4.3
Film	40	20	33	7	0	0	4.3	6.4
Aluminum electrolytic	25	25	25	25	0	0	6.6	5.2
Tantalum	24	24	47	5	0	0	5.2	6.8
INDUCTORS								
	0	27	53	20	0	0	8.1	8.0

Source: Electronics Purchasing Magazine's survey of buyers.

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KEITHLEY INSTRUMENTS

Remember when...
There were no lights in Wrigley Field?
Eight megabytes of RAM was only \$320,000?

Take a stroll with NEC



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down Memory Lane.

- 1893** Grover Cleveland sworn in as president. William Wrigley, Jr. introduces Juicy Fruit and Spearmint gum at 5¢ a pack, its price for the next 78 years.
- 1916** Wrigley buys Chicago Cubs.
- 1971** Wrigley's son Philip grudgingly increases price of gum to 7¢ a pack.
- 1975** Chewing gum is 15¢ a pack. Eight megabytes of RAM is \$320,000. 1K DRAMs are \$5.
- 1985** NEC introduces made-in-America 256K DRAMs.
- 1988** Lights go on in Wrigley Field (8/8/88). NEC 1-megabyte SIMMs retail for \$400. Chewing gum is a quarter.
- 1989** NEC ships 4-megabit DRAMs in high volume.
- 1990** NEC 1-megabyte memory modules (SIMMs) begin the year at less than \$100. George Bush throws out first ball. NEC samples 60-nanosecond 4-megabit DRAMs in 300-mil SOJ packages.
- 1993** U.S. president sworn in. NEC ships 16-megabit DRAMs from its Roseville, California, submicron line. Cubs win World Series.



If the price of chewing gum had dropped as fast as memory prices, you could buy 667 packs for a quarter.

For the latest information on NEC SIMMs and 4-megabit DRAMs in 300-mil SOJ packages, remember to call NEC.

Special-feature SRAMs

John Gallant, Associate Editor

Maintaining zero-wait-state memory performance for 33- and 40-MHz μ Ps can exceed a system designer's pain threshold. At such high speeds, designs employing standard static RAMs (SRAMs) and external glue logic suffer from interface problems. Time delays caused by latch propagation, package-lead inductance, pin capacitance, and pc-board trace lengths can force designers to use very expensive, fast-access SRAM to make up for lost time. The added burden of timing skews and uncertainties associated with the logic transition of control signals may bring a designer to conclude that, based on worst-case timing analysis, problems associated with zero-wait-state performance are insurmountable.

Fortunately, SRAM vendors are aware of the system designer's plight. Although vendors are constantly pushing the leading edge of IC lithography to produce faster, bigger, and wider SRAM cells, they are also implementing key architectural innovations to ease SRAM chip interface problems. SRAM vendors are incorporating glue-logic and system functions into SRAM architectures to take some of the heat off systems designers.

One notable architectural innovation combatting time delays is the absorption of address and data latches onto the SRAM chip. For example, modern CISC and RISC CPUs require an address latch between the CPU and the system's cache data RAM.

Most 16-MHz and 20-MHz designs employ a fast external 373-type transparent latch, which has an enable-to-latch delay of 5 to 10 nsec. However, a 33-MHz 80386 μ P, which performs a nonpipelined read in 60 nsec,

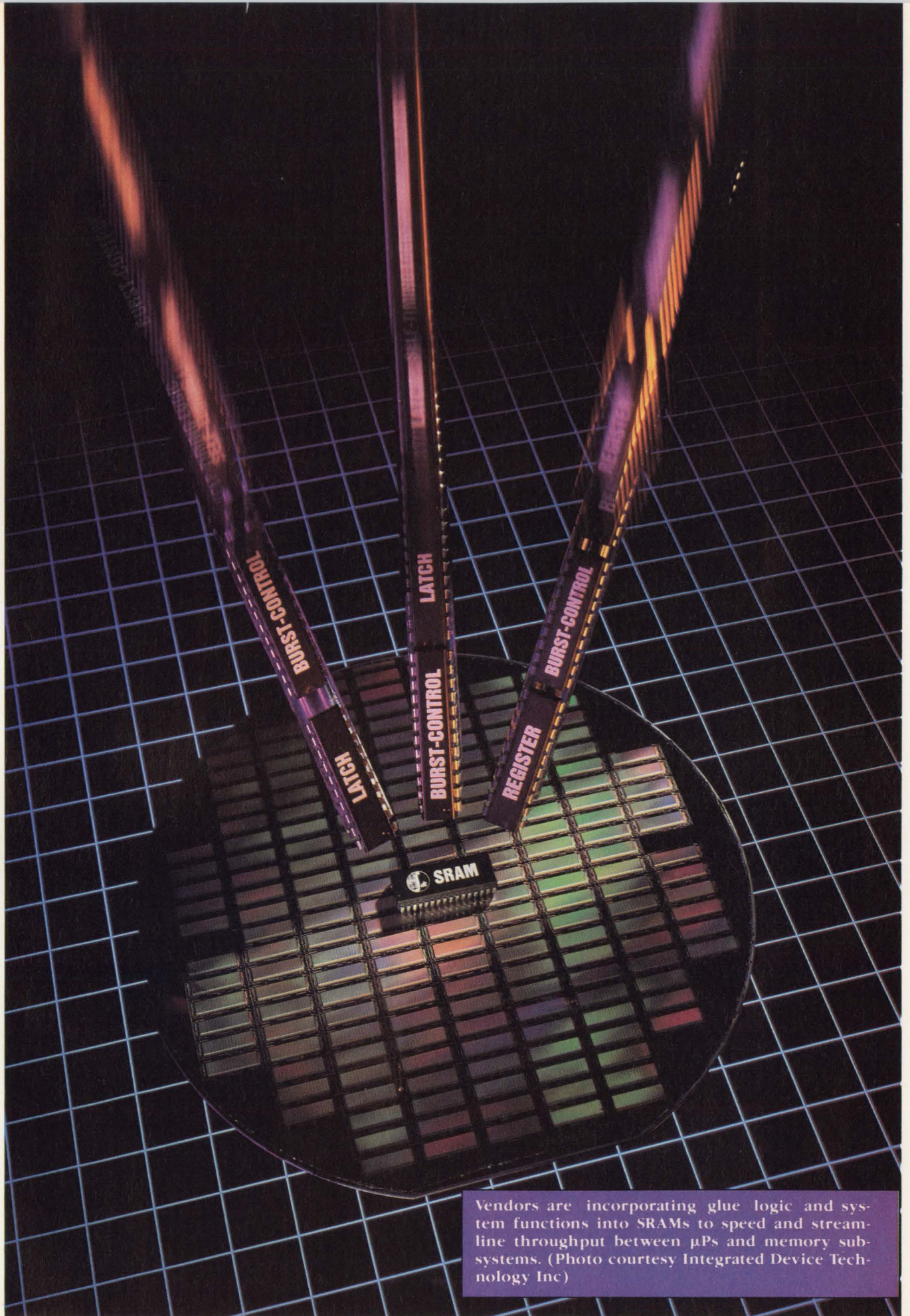
requires a fast-access SRAM for a cache data RAM. The search time for a tag-RAM match, before the cache controller enables the latch, is typically 20 nsec for Intel's 82385 cache controller, and the read setup time for the 80386 is 5 nsec. Therefore, the latch's enable time plus the RAM's access time must be less than 35 nsec. Additional circuit time delays and timing skews force the designer to use an SRAM that has a 20-nsec access time when employing an external latch.

The AT&T and Cypress 7C183 and 7C184 SRAMs absorb the transparent address latch onto the chip. Consequently, the latch-enable times are reduced to 1 to 2 nsec. Because the SRAMs match the timing requirements of

Intel's 82385 controller, they have read and write cycle times as low as 25 nsec. The 25-nsec latch-enable/RAM-access time yields an adequate margin for a 33-MHz design. Micron Technologies' MT56C0816 and Quality Semiconductor's QS88xx SRAMs contain on-chip transparent address latches optimized for use with the 82385 cache controller and the 80386 μ P. Both CMOS families of SRAMs have members that can work with 25-, 33-, and 40-MHz designs.

You can organize the memory cells for these CMOS

Each successive SRAM generation must be faster, denser, and wider to keep pace with the latest CPU speeds and architectures. But when SRAMs seem to be losing ground, innovative SRAM architectures are often the means by which memory subsystems stay in the running with today's μ Ps.



Vendors are incorporating glue logic and system functions into SRAMs to speed and streamline throughput between μ Ps and memory subsystems. (Photo courtesy Integrated Device Technology Inc)

Standard 16- and 20-MHz-style designs that employ traditional SRAMs and external glue logic cause interface problems at higher frequencies.

SRAMs as two, 2-way set-associative blocks of $4k \times 16$ -bit or one direct-mapped $8k \times 16$ -bit block. The memory arrays in two versions of the QS88xx family can accommodate a CPU parity bit. The MT56C0816 has two independent output-enable pins that tie to the \overline{COEA} and \overline{COEB} pins on the 82385. The output-enable time is 8 nsec—sufficient time to select the data from the correct associative block in a 33-MHz design.

Intel's 82395DX smart cache controller not only integrates address latches along with the data SRAM, the

single chip includes the tag RAM and the cache-management logic. The complete first-level cache subsystem ties directly to the local address, data, and control buses on the 80386 μ P. The chip has either 16, 32, or 64k bytes of data SRAM organized into 4-way set-associative blocks. The chip is available for 20-, 25-, and 33-MHz designs. Intel also offers the 82395SX smart cache controller with 8k bytes of data SRAM that ties directly to the 80386SX μ P.

Some μ Ps, such as Motorola's 68030 and 68040, can

Table 1—Special-feature SRAMs

Company	Part	Organization	Access time (nsec)	Package	Power	Price	Comments
AT&T	C183	dual $4k \times 16$ -bit or $8k \times 16$ -bit	25, 35, 45	48-pin DIP; 52-pin LCC	700 mW at 45 nsec	\$22 (PDIP) (25 nsec)	Transparent address latches; 80386 and 82385 compatible.
	C157	$16k \times 16$ -bit	20, 24, 33	52-pin PLCC	1.25W at 33 nsec	\$77 (PLCC) (20 nsec)	Clocked registers for address and data; dual-registered write enables; self-timed write; SPARC CY7C600 compatible.
Cypress Semiconductor	100E492	$2k \times 9$ bit	6	64-pin ceramic flat pack	2.0W	>\$100 (100)	Available 4th quarter 1991; BiCMOS with 100K and 101K ECL I/O; clocked registers for address and data; data and address parity flags; self-timed write.
	7B160	$16k \times 4$ bit	8	28-pin PDIP PLCC	700 mW	\$50.45 (100)	BiCMOS with TTL I/O; 4 chip enables eliminate bank decode logic; self-timed write.
IDT Inc	71321	$2k \times 8$ bit	20, 25, 30, 35, 45, 55	52-pin PLCC	325 mW	\$16.25 (100) (55 nsec)	Dual ports; interrupt logic; master busy logic.
	7052	$2k \times 8$ bit	25, 30, 35, 45	108-pin PGA 132-pin PQFP	750 mW	\$55.80 (100) (44 nsec)	Four ports.
	71322	$2k \times 8$ bit	35, 45, 55	48-pin DIP 52-pin PLCC	500 mW	\$19.80 (100) (55 nsec)	Dual ports; semaphore logic.
Micron Technology Inc	58C1616	$16k \times 16$ bit	15, 17, 20, 25	52-pin PLCC & PQFP	1.1W	\$35 (100) (15 nsec)	Clocked address registers; transparent data-in latches; dual write-enable lines; 6-nsec output-enable line; dual chip-select lines; optional 3.3V output buffers; upper and lower byte-select lines.
	56C2818	dual $4k \times 18$ bit or $8k \times 18$ bits	24, 28	52-pin PLCC & PQFP	1.1W	\$17 (100) (24 nsec)	Transparent address and data-in latches; 80486 and 82485 compatible; 8-nsec output enable; dual chip-select lines; upper and lower byte-select lines; automatic write-cycle completion.
	56C0816	dual $4k \times 16$ bit or $8k \times 16$ bits	20, 25, 35	52-pin PLCC & PQFP	1.1W	\$15 (100) (20 nsec)	Transparent address latch; 80386 and 82385 compatible; dual chip-select lines; upper and lower byte-select lines; 8-nsec output-enable time.
Mosel	76500	64×16 bit	20	52-pin PLCC	400 mW	\$32 (1000)	Dual-port bidirectional FIFO; i80355 BMIC compatible; parity generator and checker; full, empty, and half-full flags; 8-bit or 16-bit asynchronous inputs and outputs.
	443	$16k \times 9$ bit dual port	8	64-pin plastic flat pack	250 mW	\$16 (1000)	128-bit data path; part of the simulcache chipset for 33-MHz 80386 and 80486 designs; supports 486 burst reads and writes; dual ports.

Special-feature SRAMs

communicate with external memory synchronously. Synchronous communication requires the μ P to maintain valid bits on the address, data, and control buses during the rising edge of the system clock. System designs for 16- to 20-MHz operation employ 374-type D flip-flops to store bits on the local buses using the system clock. For synchronous 33-MHz and faster frequency designs, SRAM vendors have moved 374-type D flip-flop registers onto the RAM chip. These synchronous SRAMs use the system clock to store the address

and control inputs in the on-chip registers. Synchronous storage permits the μ P to communicate with the SRAM in a pipelined mode. For example, during a burst fill, the SRAM stores the $N + 1$ th address, chip select, and write-enable lines on a system-clock edge while returning the N th data word to the μ P on the same clock edge.

By synchronously storing the address, chip select, and write-enable lines on-chip, the synchronous SRAM also can generate the write pulse to the RAM array

Company	Part	Organization	Access time (nsec)	Package	Power	Price	Comments
Motorola Inc	62990	16k x 16 bit	17, 20, 25	52-pin PLCC	2.0W	\$33.75 (1000) (20 nsec)	Clocked address registers; transparent data latches; dual chip-select lines; upper and lower byte-select lines; optional 3.3V output buffers; self-timed write.
	62940	32k x 9 bit	14, 19, 24	44-pin PLCC	1.2W	\$40 (1000) (19 nsec)	68040 compatible; 2-bit binary burst-mode counter; clocked address registers; transparent data latch; self-timed write; optional 3.3V output buffers.
	62486	32k x 9 bit	14, 19, 24	44-pin PLCC	1.2W	\$40 (1000) (19 nsec)	80486 compatible; 2-bit binary burst-mode counter; clocked address registers; transparent data latch; self-timed write; optional 3.3V output buffers.
	62980	64k x 4 bit	15, 20	28-pin PSQJ	1.0W	\$31.85 (1000) (20 nsec)	Clocked address registers; asynchronous late-write abort, which can prematurely halt a burst write; optional 3.3V output buffers; self-timed write.
	62995	16k x 16 bit	17, 20, 25	52-pin PLCC	2.0W	\$31.25 (1000) (20 nsec)	MIPS R3000 compatible; asynchronous late-write abort; optional 3.3V output buffers; clocked address registers; upper and lower byte-select lines.
Quality Semiconductor Inc	8819	dual 4k x 18 bits	20, 25, 35	52-pin PLCC	1.0W	\$22 (100) (20 nsec)	Production quantities available 4th quarter 1991; 80386 and 82385 compatible; dual 8-nsec output-enable lines; dual chip-select lines; transparent address latches; upper and lower byte-select lines.
	8818	dual 4k x 18 bits	20, 25, 35	52-pin PLCC	1.0W	\$22 (100) (20 nsec)	Production quantities available 4th quarter 1991; identical to the 8819 except address A12 isn't latched. An unlatched A12 provides fast odd or even word access.
	8811	8k x 18 bits	20, 25, 35	52-pin PLCC	1.0W	\$25 (100) (25 nsec)	Production quantities available 4th quarter 1991; 80486 compatible; asynchronous address latch; 8-nsec output enable; upper and lower byte-select lines; 2-bit binary burst-mode counter.
Silicon Connections Corp	4109	8k x 9 bits	5	64-pin ceramic QFP	3.0W	\$2.57 (1000)	Samples available 4th quarter 1991; clocked address and data registers; tag RAM produces a match in 1.5 nsec; flash clear of the valid bit; BiCMOS with ECL I/O; self-timed write; address and data-parity flags.
	5204	256k x 4 bits	10, 12	32-pin ceramic flat pack	1.5W	\$3.30 (1000)	Samples available 4th quarter 1991; BiCMOS with 100K ECL I/O; balanced read and write cycle times.

For synchronous 33-MHz and faster frequency designs, SRAM vendors move 374-type D flip-flop registers onto the RAM chip.

onboard the chip—a technique known as “self-timed write.” An on-chip register has more controlled write-pulse setup time (measured from the rising clock edge to the falling write-pulse edge) and write-pulse hold time (measured from the rising edge of the write pulse to the next rising clock edge) than an off-chip register (Fig 1). Therefore, SRAM designers can generate a wider on-chip write pulse and thereby employ a slower, less expensive RAM array to achieve the system write-cycle time.

Micron Technologies' MT58C1616 and Motorola's MCM62990 SRAMs have typical synchronous SRAM architectures. Besides their synchronous registers and self-timing features, these devices have asynchronous input-data latches that simplify timing during write cycles. They also have dual write-enable lines that permit individual byte writes. Dual chip-select lines, which eliminate the need for chip-select decoders when using the SRAMs in a dual-bank arrangement, are another feature of both chips.

Both CMOS chips have an option for either 5V or 3.3V power supplies for the output buffers; therefore, they are compatible with future high-speed μ Ps that may use 3.3V power supplies. Micron also offers their cache data SRAMs in a 53-pin plastic quad flat pack (PQFP) that is 40% smaller than industry-standard 52-pin plastic leadless chip carriers. The PQFP has an

outside dimension of 14.3 mm. The smaller footprint not only occupies a smaller board space, it also reduces board trace lengths, cutting time delays and crosstalk.

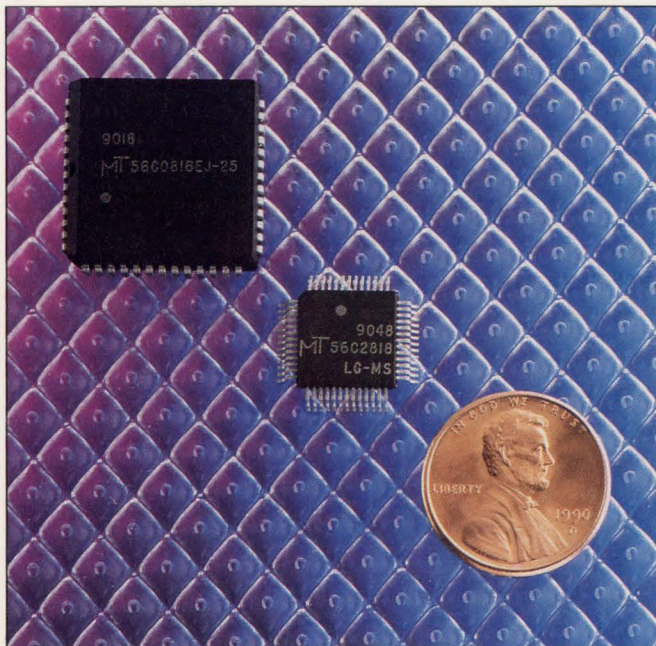
On-chip cache avoids bottlenecks

When a μ P sequentially reads and writes data to an external memory device, the μ P runs into a fundamental limitation known as the “Von Neumann bottleneck.” No matter how fast the μ P can clock data internally, the rate at which information can be piped in and out of external memory limits the chip's processing speed. Therefore, recent μ Ps place a complete first-level cache subsystem on the processor chip to profit from on-chip parallel processing. Motorola's 68040 integrates independent 4k-byte instruction and cache data SRAMs, independent memory management units (MMU) and cache controllers, a bus controller, and an execution unit on a single chip. Intel's i486 integrates an 8k-byte cache SRAM for storing code and instructions, a cache controller, an MMU, a bus controller, and an execution unit.

Although the densities of the cache RAMs in both the 68040 and i486 are sufficient to achieve better than 90% hit rates, occasionally a miss occurs and the cache controller must fetch the data from an external secondary cache. Both of these μ Ps have burst modes for accessing a line from external memory. During a burst line refill or push, the first access requires two clock cycles. Succeeding accesses require one clock cycle. Burst SRAMs assist the system designer in designing a secondary cache subsystem to handle the one-clock-cycle access timing constraints in a high-speed design.

Motorola's MCM62940 32k \times 9-bit synchronous burst SRAM is designed as a secondary cache to handle the 68040's burst mode. The 68040 can initiate a 16-byte line refill or push to the secondary cache using a single instruction—MOVE16. The burst SRAM integrates synchronous registers, which store address and control signals using the system clock, and an on-chip, 2-bit binary counter, which operates similar to the address counter in nibble-mode dynamic RAMs (DRAMs). The burst counter imitates the burst address sequence from the μ P, but only stores every fourth address in the sequence. The binary counter generates the intervening addresses. Because the chip internally generates successive addresses to the array, the architecture eases external timing constraints. The 62940's 9-bit organization accommodates the 68040's parity bits.

Intel's i486 also initiates a burst mode to refill or push a 16-byte line to an external secondary cache whenever there is a miss in its on-chip internal cache.



Small footprints reduce board space and consequently time delays and crosstalk because trace lengths are shorter. Micron Technologies' plastic quad flat pack has an outside dimension of 14.3 mm.

Special-feature SRAMs

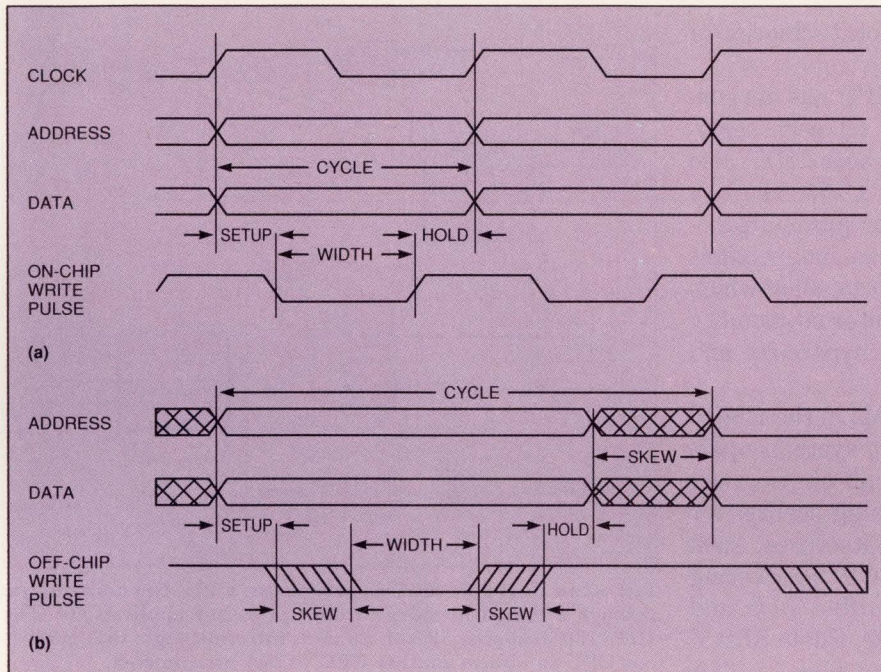


Fig 1—Synchronous SRAMs (a) generate an on-chip write pulse that occupies a smaller percentage of the system write-cycle period. The on-chip, self-timed write pulse eliminates timing skews associated with an off-chip write pulse (b), which either slow the system write cycle or force the use of a fast-access SRAM array.

Motorola's MCM62486 32k × 9-bit and Quality Semiconductor's QS881 8k × 18-bit burst RAMs contain 2-bit counters that imitate four successive addresses in the burst sequence of the i486 to alleviate off-chip timing burdens. Both devices operate in 33- and 40-MHz designs, and their 9-bit organization accommodates the parity bits of the i486.

Mosel's Simulcache is a chip set for use as a secondary cache in a 33-MHz i486 design. The set consists of the MS441 cache controller and the MS443 intelligent dual-port SRAMs. By providing dual-port access, the MS443 isolates the μ P from the system data bus. The dual-port SRAM provides 8-nsec, simultaneous access to the CPU and the main memory during burst reads and writes. In addition, the 16k × 9-bit SRAM has an internal 128-bit data path that permits the chip to move large chunks of data into, out of, and around the memory quickly. Therefore, the chip can absorb transactions from the main memory and reorder the data to meet the needs of the CPU.

Multiports assist multiprocessors

Architectural developments in high-speed, dual-port SRAMs allow two CPUs to communicate with each other by passing data through a common memory. The basic dual-port architecture is a variation on the traditional single-port SRAM, which has one read and write control circuit for a single address and data bus. The dual-port memory has two sets of address, data, and

read/write control signals, each of which access a single on-chip memory array. Each set of controls can independently and simultaneously access any word in the array, even when both ports are accessing the same location at the same time.

Multitasking processors must signal each other when requesting a task or indicating a task's completion. Interrupts are a common signaling mechanism. IDT's 25-nsec IDT71321 is a dual-port SRAM containing logic that allows one CPU to interrupt the other. A CPU simply writes to a specific address port to activate the interrupt to the other CPU. The IDT71322 dual-port SRAM contains semaphore logic that provides a set



SRAM architectures are married to the design of a specific processor. Motorola's MCM56824 is an 8k × 24-bit SRAM that has dual chip enables and output enables that conform to the time requirements of the DSP56001 DSP chip.

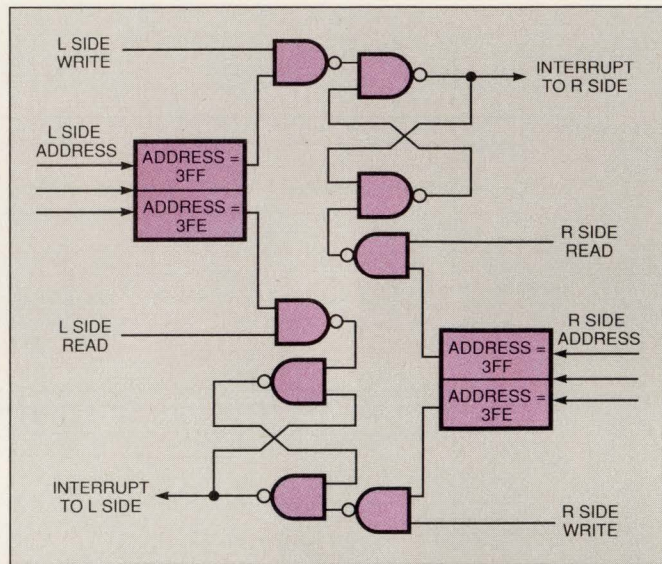
Special-feature SRAMs

of flags that software can use to allocate blocks of memory for one of the CPUs to use.

You use each flag to indicate which CPU has permission to use a specified block. You can set each semaphore flag to either CPU, but not to both. IDT also offers 4-port SRAMs, which let four CPUs share a common memory for multiprocessing or parallel processing. The IDT7052 4-port SRAM has independent address, data, and read/write control ports, all of which have independent access to the chip's internal memory array. The 4-port structure facilitates hypercube and cluster configurations.

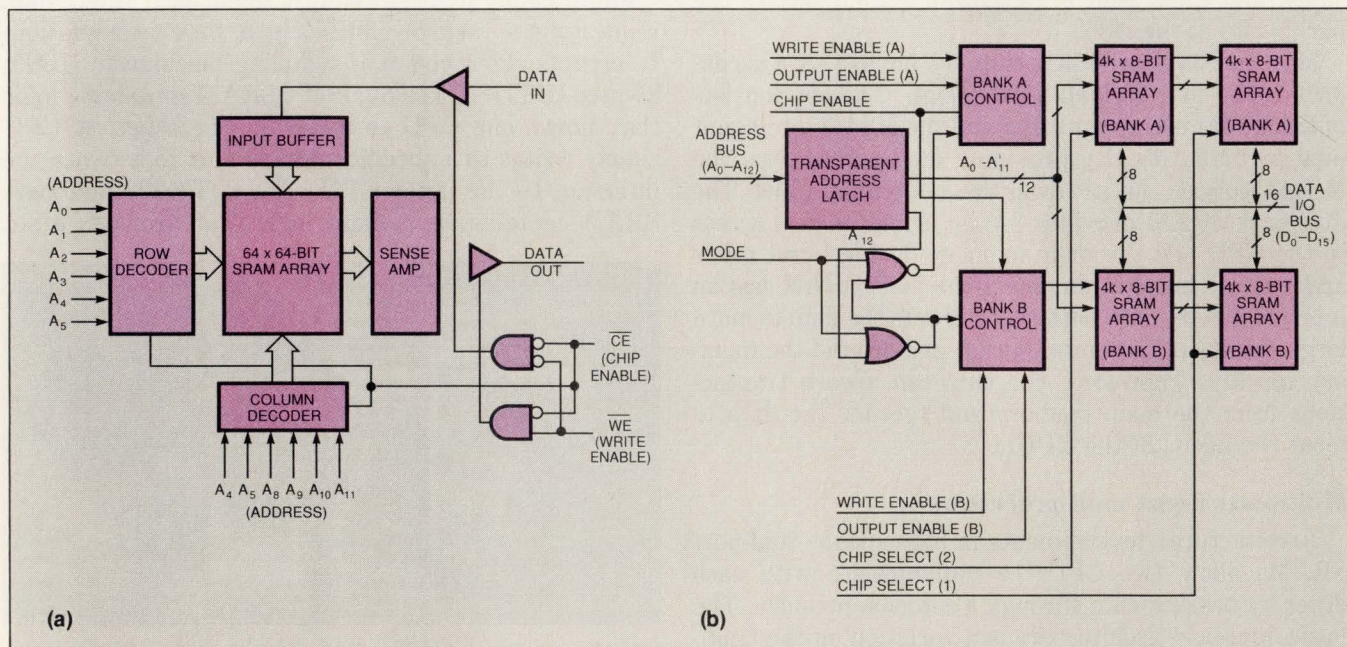
Architectural enhancements to SRAMs in the CMOS families are paving the path for memory systems operating as fast as 50 MHz. But CPUs aren't obeying any 50-MHz speed limit. Vendors are obtaining licenses for implementing some popular CPU architectures, such as the MIPS 3000, using GaAs to send CPUs rocketing ahead. These CPUs have ECL-compatible I/Os and will operate in the 60- to 100-MHz range. Some SRAM vendors are on top of the situation and plan to offer BiCMOS SRAMs that will have ECL I/Os and be able to interface with these CPUs.

Cypress has acquired the rights to manufacture National Semiconductor's 2k x 9-bit and 8k x 9-bit ECL SRAMs using a 0.8- μ m BiCMOS process. The 6-nsec CY100E492 is a synchronous, self-timed SRAM that

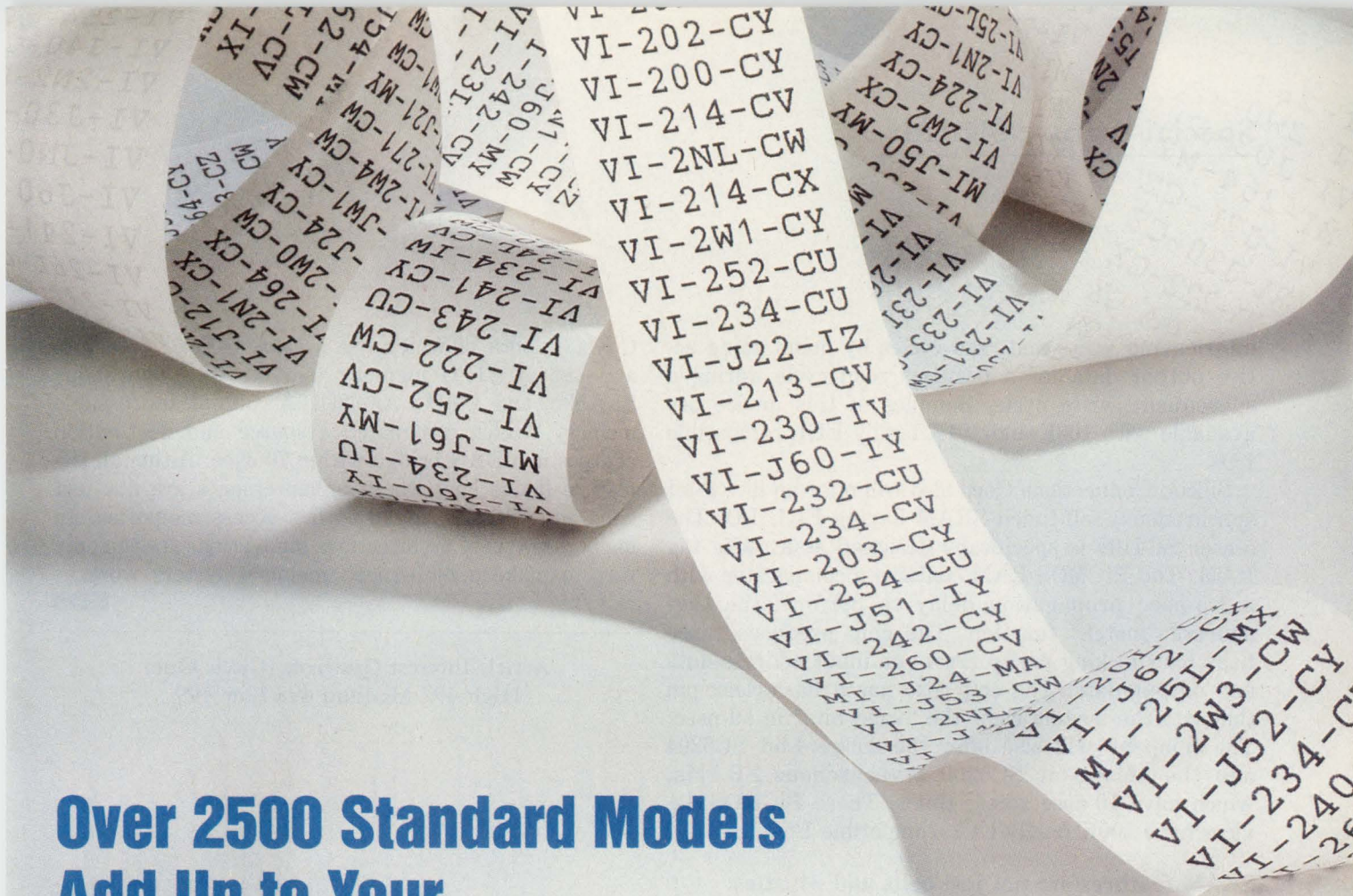


Fast access dual-port SRAMs permit two CPUs to communicate through a shared memory in multiprocessor applications. The IDT7130 dual-port SRAM contains interrupt logic that permits one CPU to inform another CPU of task assignments.

employs on-chip registers on its input and output lines. A single clock stores the data in the input registers, and the output registers are self timed. The chip produces a flag for checking the parity of both the address and the data. A hidden write-cycle mode simplifies



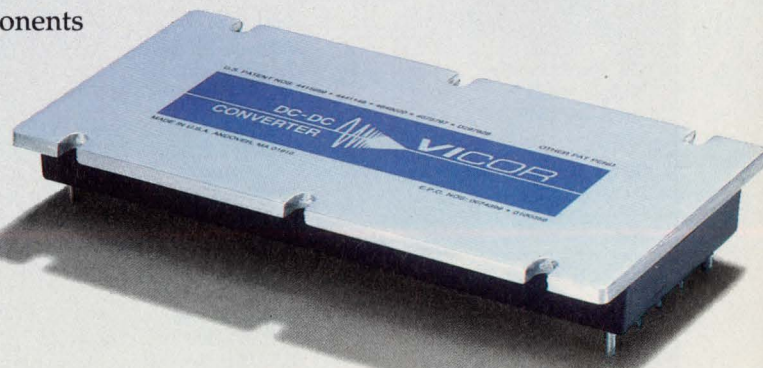
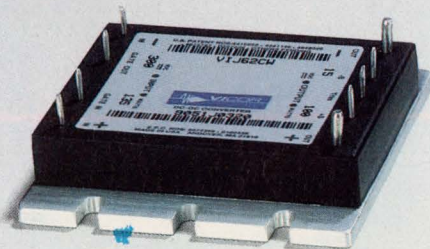
Modifications to the traditional SRAM architecture (a) simplify interfaces. Quality Semiconductor's QS8816 cache data SRAM (b) for 80386 systems has transparent address latches, dual chip selects to eliminate bank decoders, separate write enables for each memory bank, and dual 8-nsec output enables for gating data onto the bus.



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interleaving write and read cycles by maintaining active output data for a previous read cycle during a subsequent write cycle. Samples of this device are available with 100K and 101K family ECL-compatible I/Os.

Silicon Connections Corp also will offer an 8k×9-bit synchronous, self-timed SRAM having ECL I/O. The 5-nsec SC4109 is specifically designed as a cache tag RAM. The BiCMOS RAM contains a comparator with a 1.5-nsec propagation delay to perform the tag-address "match" function. The chip produces three flags for checking parity errors on input address data and output data. The chip also has a flash-clear pin that lets the system clear the "valid bits" in 50 nsec. The company will also offer the 256k×4-bit SC5204 and the 1M×1-bit SC5200 asynchronous SRAMs, which have 10-nsec access times. These BiCMOS devices have 100K family ECL-compatible I/Os.

SRAM features are not just bells and whistles

The complete list of features that vendors are incorporating into the basic SRAM architecture to improve system performance is too long for a single article. The list should include IDT's SyncFIFO and Cypress'

CYC451, both of which use a clock to load data into and out of FIFO memory (similar to synchronous SRAMs), and AMD's Am99C10A content-addressable memory, which can match a source and destination address in a LAN bridge within 70 nsec. Although the feature list is long, these enhancements are not just bells and whistles added to fast-access memories. In many cases these architectural innovations are the only way to make a high-speed memory system work.

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Manufacturers of special-feature SRAMs

For more information on the special-feature SRAMs such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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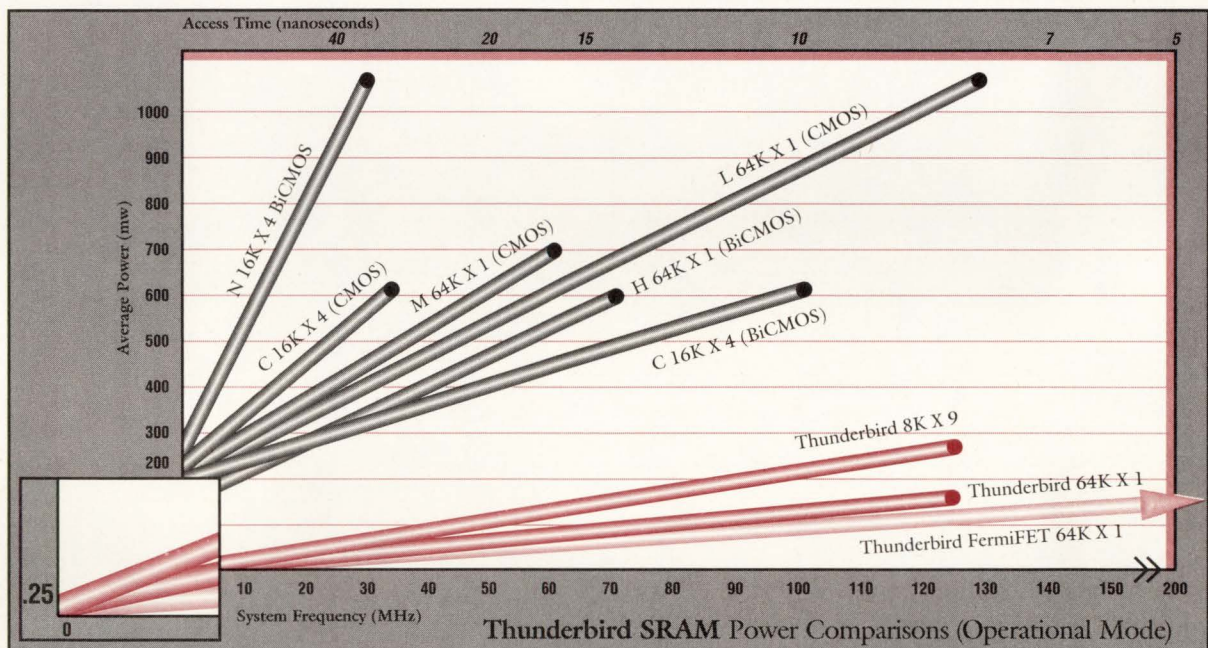
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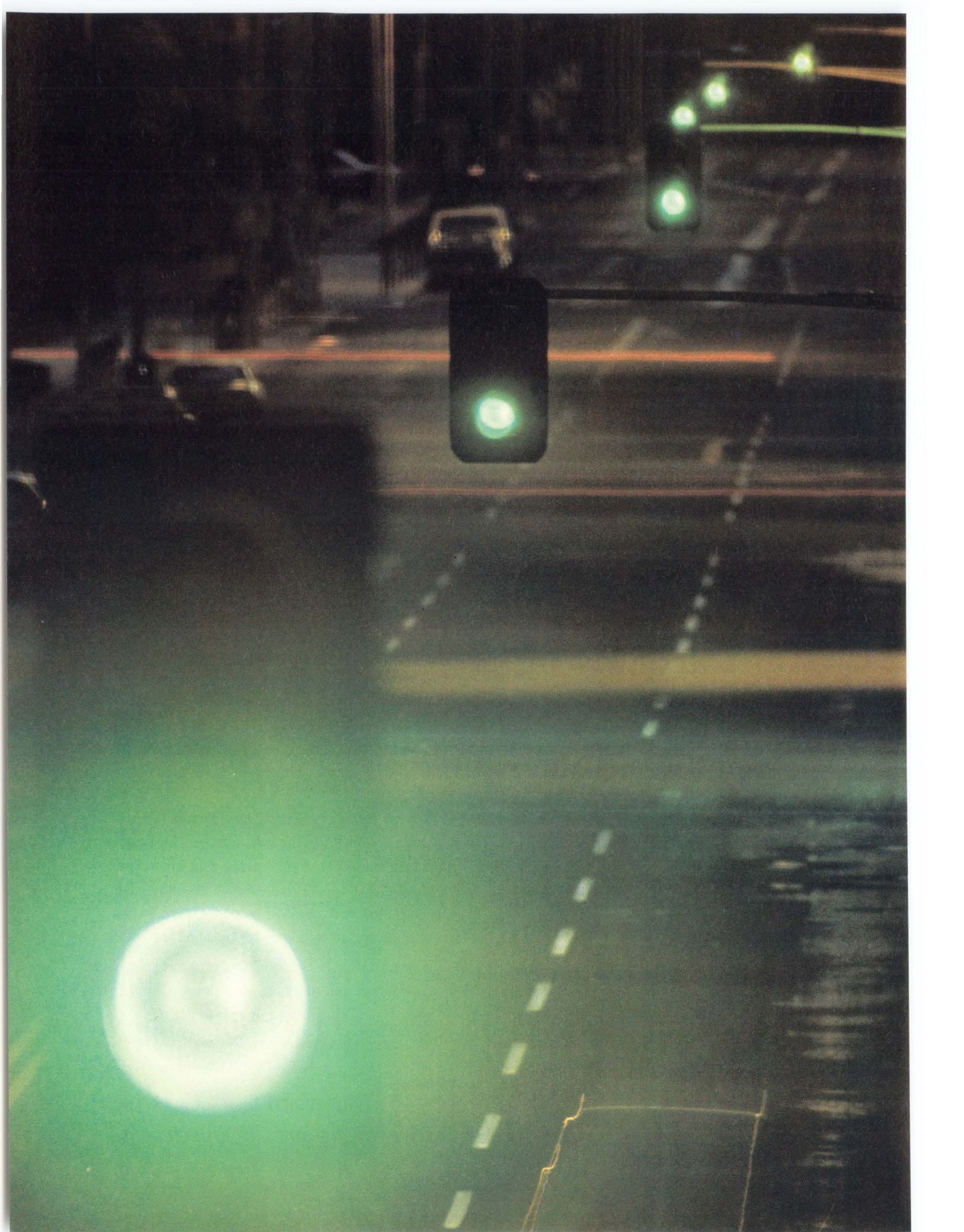
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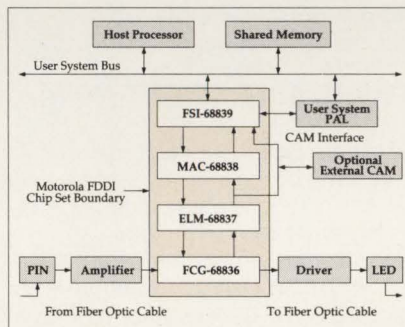
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Innovative analog circuits from Texas Instruments add a new edge to Digital Equipment's proven market winners. They can do the same for you.



The goal Digital Equipment Corporation set was clear: Strengthen its position as the leading supplier of Ethernet-based local area network products. Achieving the goal has been spurred by the use of Advanced Linear circuits from Texas Instruments.

These leadership ICs meet growing industry demand for linear circuits that can improve overall system performance and reliability, reduce costs and speed design cycles.

These were precisely the advantages Digital's designers needed.

Expertise and teamwork carry the day

For many years, Digital has used a wide variety of TI linear circuits — from op amps to mixed-signal devices — and values our analog viewpoint toward system design.

As Digital defined the requirements to meet its market goal, the decades-long relationship entered a new era of even more intense cooperation. With Digital handling system-level design and TI applying its linear expertise, the two teams fully utilized our LinASIC™ design methodology to create a series of mixed-signal Ethercell™ functions. They are the basis for the advanced linear devices Digital requires.

The design flow was aided by our

Boston-area Regional Technology Center that provides access to LinASIC development tools and by the extensive use of EDIF to exchange information.

Enhancing Digital's competitive edge

To date, close teamwork has produced components that can enhance Digital's ability to respond quickly to market demands for feature-rich but lower cost Ethernet and communications products:

- A dual driver and dual receiver IC that minimizes the number of components required for the Attachment Unit Interface (AUI) function in an Ethernet network.

“Utilizing TI’s LinASIC mixed-signal design methodology allows us to design cost-effective solutions with aggressive time-to-market goals.”

— Nick Ilyadis, Product Engineer
Telecommunications and Networks Group
Digital Equipment Corporation



- An octal receiver created to solve system-level cross-talk noise problems in RS-232, -485 and -423 applications. This full-custom device, fabricated in TI’s Advanced LinCMOS™ process, is designed to meet EIA and CCITT specs.
- A device that will be a complete AUI multiport concentrator on a chip. Fabricated in our LinBiCMOS™ process, it will replace a 6-inch by 12-inch circuit board that incorporates nine discrete ports, logic devices and analog circuitry. The new device will tie any combination of as many as eight units into Ethernet.

- A single-channel 10BASE-T twisted pair interface chip that includes internal precompensation and full duplex operation. Also fabricated in our LinBiCMOS process, this IC cuts component count and improves data transmission.

The Ethercell devices developed by Digital and TI will be incorporated into our existing LinASIC cell library.

Extensive mixed-signal capabilities

As Digital recognizes, few in the industry can match our experience in analog design and digital design. This expertise enables us to effectively combine high-performance

analog functions with leadership digital functions. The resulting mixed-signal devices typify our capabilities to design and develop the Advanced Linear circuits our customers need.

Let us help you meet your challenge

We are ready to provide information and assistance, as well as access to the hardware and software development tools you need, to help extend the boundaries of your system performance.

Our service circles the globe, and our worldwide manufacturing capability can support your production schedules wherever you are.

TI's analog viewpoint: From process technologies come Advanced Linear ICs.

TI's LinASIC mixed-signal methodology —

A cell-based design methodology allowing the combination of high-performance analog and digital functions on the same chip. This mixed-signal capability is used for many of our catalog products and for custom/semicustom solutions. It is supported by large cell libraries, design-automation tools and these TI Advanced Linear wafer process technologies:

LinBiCMOS — Combines Advanced LinCMOS, digital ASIC CMOS and up to 30-V bipolar technologies to allow the integration of digital and analog standard cells and handcrafted analog components on a monolithic chip.

LinEPIC™ — One-micron CMOS double-level metal, double-level polysilicon technology that adds highly integrated, high-speed analog to the high-performance digital EPIC™ process.

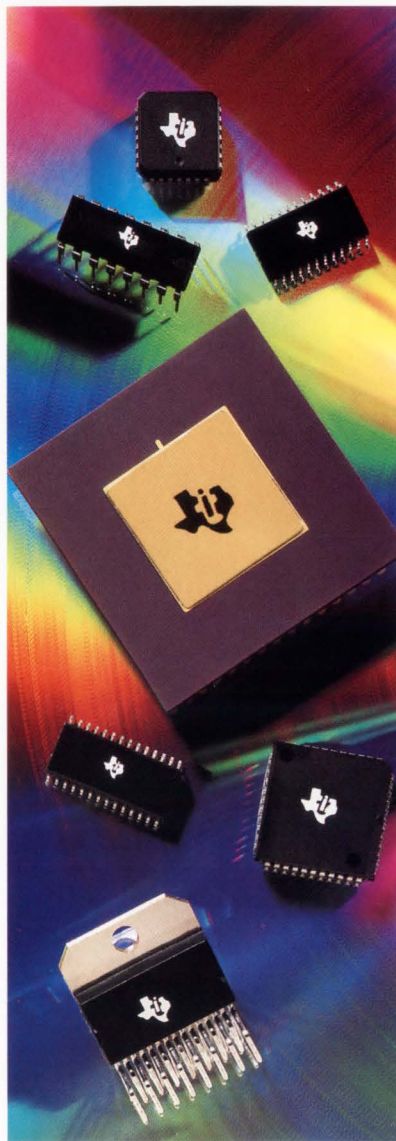
Advanced LinCMOS — An N-well, silicon-gate, double-level polysilicon process featuring improved resistor and capacitor structures and having three-micron minimum feature sizes.

Power BIDFET™ — Merges standard linear bipolar, CMOS and DMOS processes and allows integration of digital control circuitry and high-power outputs on one chip. Primarily used for circuits handling more than 100 V at currents up to 10 A.

Multi-EPI Bipolar — A very cost-effective technology that utilizes multiple epitaxial layers instead of multiple diffusion steps to reduce mask steps by more than 30%. Used to produce intelligent power devices that can handle loads as high as 20 A and voltages in excess of 100 V.

Excalibur — A true, single-level poly, single-level metal, junction-isolated, complementary bipolar process developed for high-speed, high-precision analog circuits providing stable op amp performance.

For more information on our Advanced Linear process technologies and the products they are producing, call 1-800-336-5236, ext. 3425.



TI's LinASIC methodology and Advanced Linear process technologies are enhancing these product families

Data Transmission — This family meets the needs of most industry-standard interfaces (EIA, IEEE, ANSI) and ranges from drivers/receivers/transceivers to fully integrated controller/transceivers.

Data Acquisition — The family ranges from stand-alone A/Ds and D/As to complete data conversion subsystems on a chip; from general-purpose functions to highly integrated digital signal processor and graphics signal processor analog interface circuits. Other specialized family members include telecom and speech synthesis functions.

Intelligent Power — These devices combine high-voltage and/or high-current switches with the analog and digital circuitry required to perform interface, control, protection and diagnostic functions in microcontroller-based systems.

Operational Amplifiers — A family of op amps and comparators ranging from standard bipolar to leadership high-performance CMOS and Excalibur complementary-bipolar devices, meeting needs ranging from low power and/or low noise to high speed and/or high precision.

Custom/semicustom Functions — In modifying existing products to fit your needs or in defining your own unique functions, our LinASIC methodology allows access to existing analog cells used in the development of our catalog products and compatibility with our digital cell libraries.

Build a single-shot recorder to catch fast transients

Capturing fast transients places special requirements on filters, track/hold amplifiers, and A/D converters. By using an A/D converter with a high input bandwidth and oversampling at a 10:1 ratio, you can digitize and then analyze transients without using an expensive analog or digital storage scope.

Ken Deevy, Dan Sheehan, and Mike Byrne,
Analog Devices Inc

Don't tie up expensive equipment trying to capture transients that occur infrequently. If you build a low-cost transient recorder or event sampler, you can dedicate it to capturing single-shot events. Typical applications for transient recorders include monitoring power-lines transients, evaluating power supplies, and capturing pressure and vacuum-line transients in medical equipment.

To build a transient recorder or burst-mode event sampler, you need a high-speed A/D converter, a wide-band track/hold amplifier, and an antialiasing filter. The A/D converter must have a sampling rate of at least twice the bandwidth to satisfy the Nyquist criterion. In practice, you should oversample the input signal. At $2\times$ oversampling (a sampling frequency of

twice the input bandwidth), you'll need to use a filter with an infinite roll-off rate to avoid aliasing effects. At $3\times$ oversampling, the roll-off requirement drops to 50 dB/octave in an 8-bit system. With an oversampling ratio of 10:1, the filter roll-off need be only about 16 dB/octave. (See **box**, "Oversampling reduces antialiasing requirements.")

High-speed sampling A/D converter chips routinely include track/hold amplifiers on the same chip. The AD7821 is an example of this trend. It combines a 100-kHz track/hold amplifier with a 1M-sample/sec 8-bit A/D converter. Because the A/D conversion rate is 10 times the input bandwidth, you don't have to design a complex antialiasing filter. In fact, if the input signal exhibits only a low-power spectral content at and above 500 kHz, you can eliminate the filter altogether.

The AD7821 uses a half-flash conversion technique to perform an 8-bit conversion in 660 nsec. A requirement of a 350-nsec signal-acquisition period between conversions results in a maximum acquisition rate of 1M samples/sec. You can operate the A/D converter with a single or dual supply for either unipolar or bipolar inputs.

Capture single-shot waveforms

One of the difficulties in capturing single-shot events is the speed at which the transient recorder circuit responds once the input signal has crossed a predetermined trigger point. If the recorder circuit responds too slowly, it can miss fast transients altogether.

To build a transient recorder or burst-mode event sampler you need a high-speed A/D converter, a wideband track/hold amplifier, and an antialiasing filter.

Therefore, to accurately capture fast events, you need a high-speed A/D converter and a wide-bandwidth track/hold amplifier. For example, an 8-bit A/D converter that has a 1- μ sec conversion time can capture 1- μ sec transients only if it's not preceded by a track/hold amplifier. If you match this A/D converter with a track/hold amplifier that has a 100-kHz bandwidth, the ADC can recover 6- μ sec-wide 5V transients.

To simplify fault detection or take corrective measures, you need a transient recorder that can grab pretransient information. You can use this pretransient data to learn timing relationships between the tran-

sient and another waveform. Additionally, your recorder should be able to react to both positive and negative transients.

Another important criterion for transient recorders is cost. Although you could use a digital storage oscilloscope (DSO) to capture frequently occurring or very fast transients, dedicating a DSO to capturing random events would be an expensive proposition.

Transient recorder

A block diagram of a transient recorder (Fig 1) shows the minimum hardware you'll need to build a high-speed transient recorder with playback. For sim-

Oversampling reduces antialiasing requirements

In the spectrum of a periodically sampled waveform, the spectrum of the (unsampled) input-signal repeats around harmonics of the sampling frequency. Any frequency contained in the input signal is repeated above and below each harmonic of the sampling frequency. Therefore, in the spectrum of the sampled signal, the band between 0 and f_{IN} (the input spectrum), appears—among other places—between $f_S - f_{IN}$ and f_S , where f_S is the sampling frequency. Though you may be under the impression that the input-signal bandwidth is 100 kHz, if the sampling frequency is 1M sample/sec, a signal at 991 kHz in the input spectrum would appear as a 9-kHz "alias" component in the sampled signal's spectrum.

The purpose of an antialiasing filter is to remove or at least attenuate any noise or spurious signals that could be aliased back into the bandwidth of interest.

Fig A shows the frequency response of an antialiasing filter for a generalized A/D converter. You determine the filter roll-off by

drawing a straight line between the highest signal frequency of interest, f_{IN} , and the stopband attenuation frequency, $f_S - f_{IN}$. As the ratio of f_S to f_{IN} increases (that is, as the oversampling ratio increases) the slope of the line decreases.

In an 8-bit system, an ideal

ADC's signal-to-noise ratio (S/N) is slightly greater than 256:1 or 48 dB. To avoid having noise limit the system performance, the ratio of the input signal to noise should exceed the approximately 48-dB limit imposed by the ADC. Here, the signal is the peak-to-peak value of the signal within

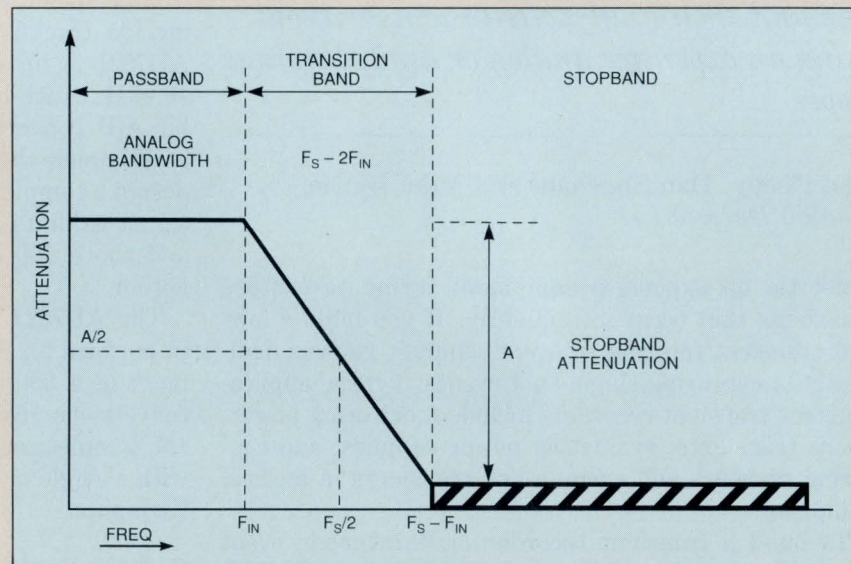


Fig A—The antialiasing filter that precedes the transient recorder's ADC can be simple or complex depending on the degree of oversampling. When the sampling frequency is 10 \times the highest frequency of interest, the filter has 3 octaves to roll in its attenuation. A simple 3-pole filter has 18 dB/octave roll-off. An 8-bit ADC needs slightly more than 48 dB of attenuation. Hence, a 3-pole filter is usually sufficient for 8-bit resolution.

plicity, the design uses a clock with an even mark/space ratio. The clock's 50% duty cycle limits the acquisition rate to 660k samples/sec rather than the A/D converter's 1-M sample/sec maximum rate. (This simplification reduces the oversampling ratio to 6.6:1.) A memory chip stores the digitized data for later playback on an X-Y plotter or oscilloscope via a dual 12-bit D/A converter and a quad op-amp. One half of the samples are pretransient information; the other half are transient data.

A more detailed schematic (Fig 2) shows that two counters, IC₁ and IC₂, control where the circuit stores pretransient and transient data. The counters also

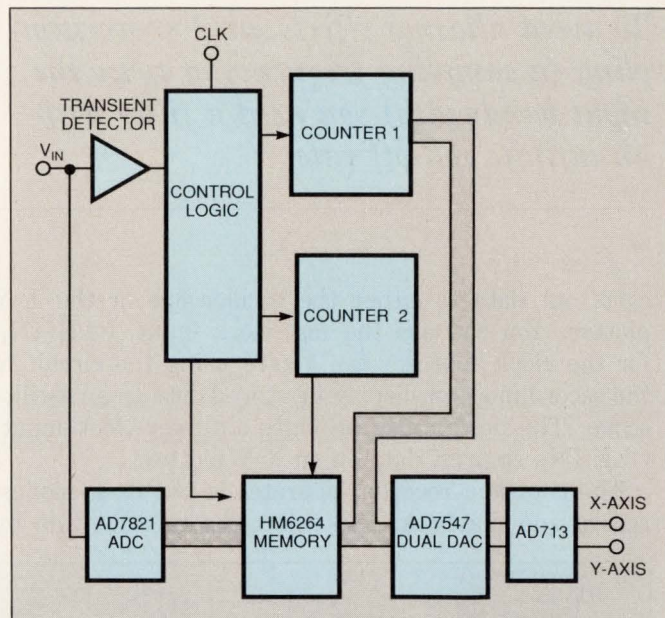


Fig 1—If you think of a transient recorder as merely an ADC, look again. This recorder contains several purely digital blocks as well as the DAC that drives the display.

the band of interest, and the noise is the square root of the sum of the squares of the amplitudes of all of the frequency components outside that band. The attenuation required on signals outside the band of interest depends on the application and the expected magnitude of the out-of-band signals. In most cases, the magnitude of these signals is much lower than that of the desired signal.

Usually, 8-bit systems require 50 dB of attenuation for signals that can be aliased into the band of interest. Even if 50 dB is not the desired number, the following calculations show the kind of reduction in antialiasing filter requirements brought about by oversampling. With $2 \times$ oversampling, (that is with $f_s = 2 \cdot f_{IN}$), f_s and f_{IN} are at the same point and the filter has to have infinite roll-off to attenuate signals at $f_s - f_{IN}$. With $f_s = 3 \cdot f_{IN}$ ($3 \times$ oversampling), the filter's attenuation must drop from 0 dB at f_{IN} to 50 dB at $2 \cdot f_{IN}$. In other words, the slope of the attenuation vs frequency curve must be 50 dB/

octave; the filter (if it has a Butterworth characteristic) must have more than eight poles.

With $10 \times$ oversampling, there are three octaves for the attenuation to drop from 0 to 50 dB. The required slope is a little more than 16 dB/octave; a 3-pole Butterworth filter will do the job.

The above analysis of the antialiasing filter holds true regardless of the type of ADC that follows the filter. No matter what the conversion technique, oversampling reduces the antialiasing filter requirements. Oversampling also reduces the ADC noise because it spreads the quantization noise over a wider bandwidth. Oversampling has recently gained considerable popularity in connection with sigma-delta ADCs. In the case of these converters, the advantages of oversampling are much greater than with successive-approximation or flash ADCs because noise shaping produces dramatic improvements in noise performance as the oversampling ratio increases.

The relationship between an-

tialiasing-filter performance and oversampling is, however, exactly the same for an oversampled sigma-delta modulator as for a half-flash or a successive-approximation ADC. A sigma-delta ADC and a half-flash ADC with the same oversampling ratio place the same requirements on the antialiasing filter.

The disadvantage of the sigma-delta process for transient recording is the pipelining or averaging technique inherent in sigma-delta converters. Because of the pipelining, a step change requires a significant time (the settling time of the ADC's digital filter) to ripple through to the output. Therefore, there is a delay before a sigma-delta converter produces an output that represents an input change. Between the time the input changes and the sigma-delta converter's output reflects the change, the ADC's output does not accurately represent the converter's input. Such performance is not appropriate for transient recorders of the type discussed here.

To avoid aliasing effects, at $2 \times$ oversampling (a sampling frequency of twice the input bandwidth) you need a filter with an infinite roll-off rate.

clock out data to either the oscilloscope or the X-Y plotter. You can use the fast clock input, CLK IN₁, for the clock source when you're using the circuit in the record mode or displaying stored data on an oscilloscope. The design also provides a slower clock input, CLK IN₂, to print data on an X-Y plotter.

The transient recorder operates in two basic modes: record and playback. You select the record mode by

placing switch S₁ in the record position. (IC_{18A} and IC_{18B} provide debouncing for this switch.) Having the MODE output of IC_{13D} low makes one input of both IC_{15D} and IC_{14D} low. Hence the clock inputs of IC_{9A} and IC_{9B} (pins 10 and 2, respectively) are disabled, ensuring that the $1\bar{Q}$ and $2\bar{Q}$ outputs of IC_{9A} and IC_{9B} are high. Besides disabling the chip-select inputs of the D/A converter, \overline{CSA} and \overline{CSB} , the circuit disables the output-

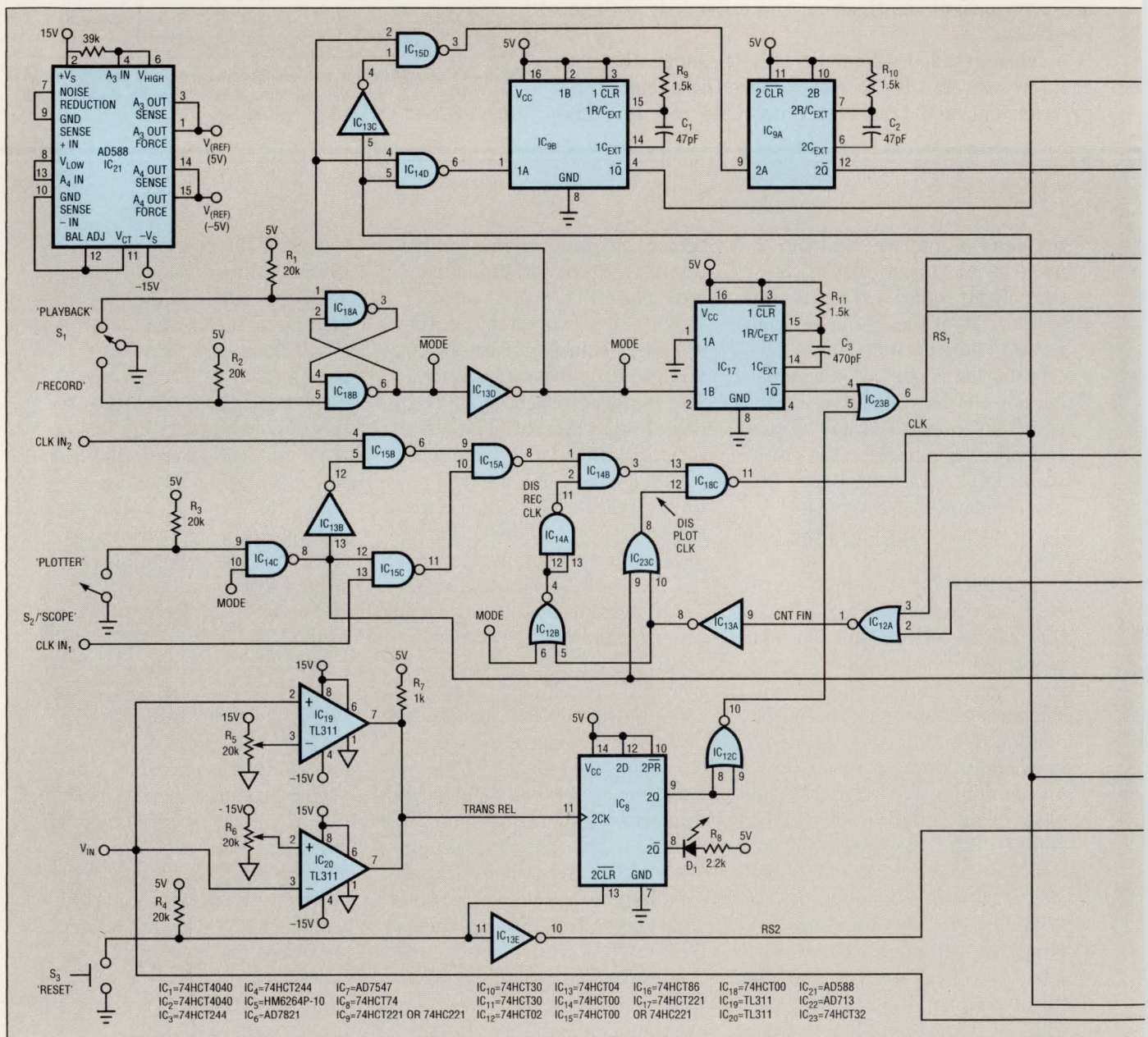


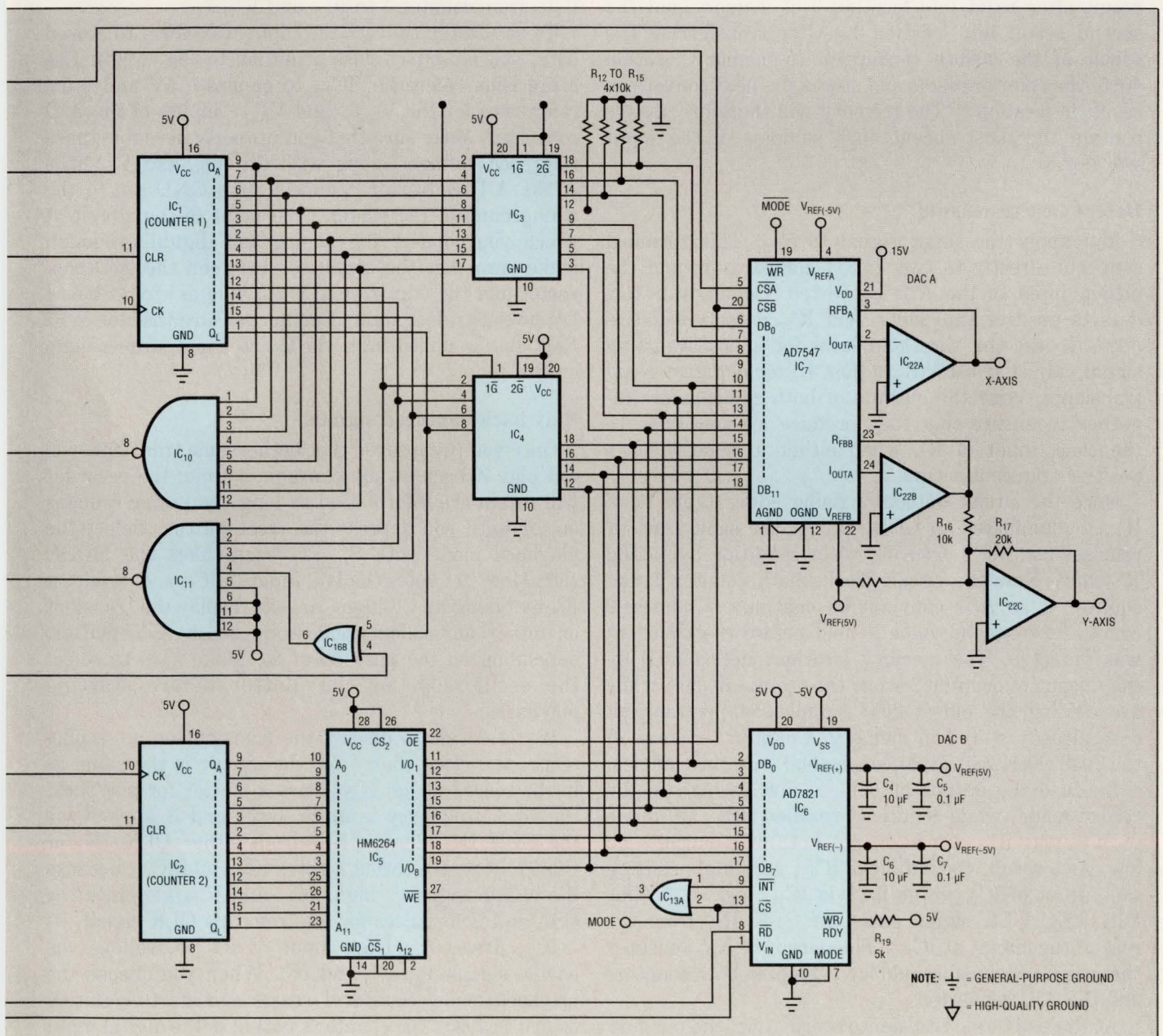
Fig 2—At the component level, the basic transient recorder is a circuit of moderate complexity, requiring 23 ICs.

enable signals of IC₃, IC₄, and IC₅ (the HM6264 memory chip), ensuring that the playback portion of the transient recorder is turned off.

CLK IN₁ serves as the clock source for the counters via IC_{14C}, IC_{-13B}, IC_{15B}, and IC_{15C}. While the MODE signal is low, CLK is the clock input for both counters and provides the \overline{RD} (convert) signal for the A/D converter, IC₆. At the same time, IC₆'s \overline{CS} input is active,

ensuring that the device is selected. After a reset from S₃ initializes the circuit, counter 2 begins counting. IC₁₇ and IC_{23B} hold the reset (CLR) input of counter 1 high from power-up and keep counter 1 in a reset condition until the circuit detects a transient.

You configure the A/D converter by tying its MODE input (pin 7) to GND. (Note that the MODE pin of the AD7821 shown bears no relation to the signal labeled



With an oversampling ratio of 10:1, the filter roll-off need be only about 16 dB/octave.

MODE in the circuit diagram.) When the CLK signal toggles its \overline{RD} input, the A/D converter executes continuous conversions of the input signal, V_{IN} . Counter 2 provides the memory addresses for the A/D conversion results. Data transfers from the digital outputs of IC₆ to IC₅ employ the \overline{INT} output of IC₆ to drive the \overline{WE} input of IC₅.

The circuit automatically loads the first conversion result after reset into location 0 of memory and the second result into location 1. After transferring the result of the 4096th conversion to memory location 4095, the counter resets and stores the next conversion result in location 0. The memory will therefore always contain the most recent 4096 samples of the input waveform.

Detect fast transients

You apply the input signal to V_{IN} . This terminal connects directly to two TL311 comparators and the analog input of the A/D converter. Comparator IC₁₉ detects positive transients, and IC₂₀ detects negative ones. To set the threshold level for a positive-going signal, adjust resistor R_5 ; adjust R_6 for negative-going transients. Wire the outputs of both comparators together to ensure that they produce a rising edge to the clock input of IC₈ when either a negative or a positive transient occurs.

Once the circuit detects a rising edge at pin 11 of IC₈, it illuminates an LED, D₁. At the same time, it releases counter 1 from its reset condition by taking RS_1 low. Now the circuit clocks both counter 1 and counter 2 as A/D conversions continue. Counter 2 counts up from the value it held before the transient was detected. The memory locations determined by the output of counter 2 store the transient data while overwriting the oldest 2048 samples of pretransient data already stored in memory. Counter 1 counts off the 2048 clock states that correspond with the samples.

Because the output of IC_{16B} is always high in the record mode, when counter 1 reaches 2047, all inputs to IC₁₀ and IC₁₁ are high and both IC's outputs go low. As a result, the output of IC_{12A} goes high, causing the output of IC_{14A} to go low via IC_{13A} and IC_{12B}. This DIS REC CLK signal gates off CLK IN₁ from the rest of the circuit at IC_{14B}. The output of IC_{18C} ensures that the CLK signal is held low, stopping both counters and the A/D converter.

At the end of the transient-record cycle, the memory will contain 4096 samples of the input waveform. One half of these samples are transient data, the other half

represent pretransient information. Whatever value is in counter 2 will be the last memory location for the transient data. The next memory location will hold the first of the 2048 words of pretransient data. Now when you start the playback mode, the first output from the counter will correspond to the memory location of the first pretransient sample. (To alter the ratio of transient to pretransient samples, simply alter the connections from counter 1 to IC₁₀ and IC₁₁.)

To accurately convert the input waveform to stored data, you must pay close attention to the circuit. Use a precision reference, IC₂₁, to generate 5V and -5V references for the V_{REF+} and V_{REF-} inputs of the A/D converter. Make sure that you properly decouple these reference voltages along with the V_{DD} and V_{SS} lines of the A/D converter. Connect IC₆'s GND pin to the star ground of the system (the point in the circuit at which you connect the analog and digital grounds). Make sure that the conductor between the A/D converter and the star ground is as wide as circuit-board layout constraints allow. Further, ensure that the \overline{WR}/RDY line is pulled high via R_{19} to avoid noise pickup on this pin.

Play back captured signals

Once you've captured that bothersome transient, you can play it back at any convenient time; the recorder will retain the information as long the power remains on, or until you depress the reset button. Select the playback mode with S_1 . Playback takes the MODE signal low, activates the \overline{WR} input to IC₇, and deselects IC₆ by taking its \overline{CS} high. You can display the transient on either an analog oscilloscope or an X-Y plotter, depending on the position of S_2 . Make sure to select the oscilloscope or the plotter before starting playback.

If you decide to display the transient on an oscilloscope, the clock source for the circuit is the same as in the record mode. If you use a plotter for playback, the clock frequency is much lower and is applied via the CLK IN₂ input. CLK (from either CLK IN₁ or CLK IN₂) passes through gates IC_{15D} and IC_{14D} because the MODE signal is high. IC_{9A} and IC_{9B} generate the \overline{CSA} and \overline{CSB} pulses for IC₇ from this CLK signal.

IC_{9A} drives the \overline{CSA} input of IC₇ as well as the enable signals for IC₃ and IC₄. When you choose the playback mode, counter 1 resets and starts counting from 0 to 4095. The counter's output is the digital input code to DAC A of IC₇. This DAC drives the X axis of either the oscilloscope or the plotter. DAC A produces

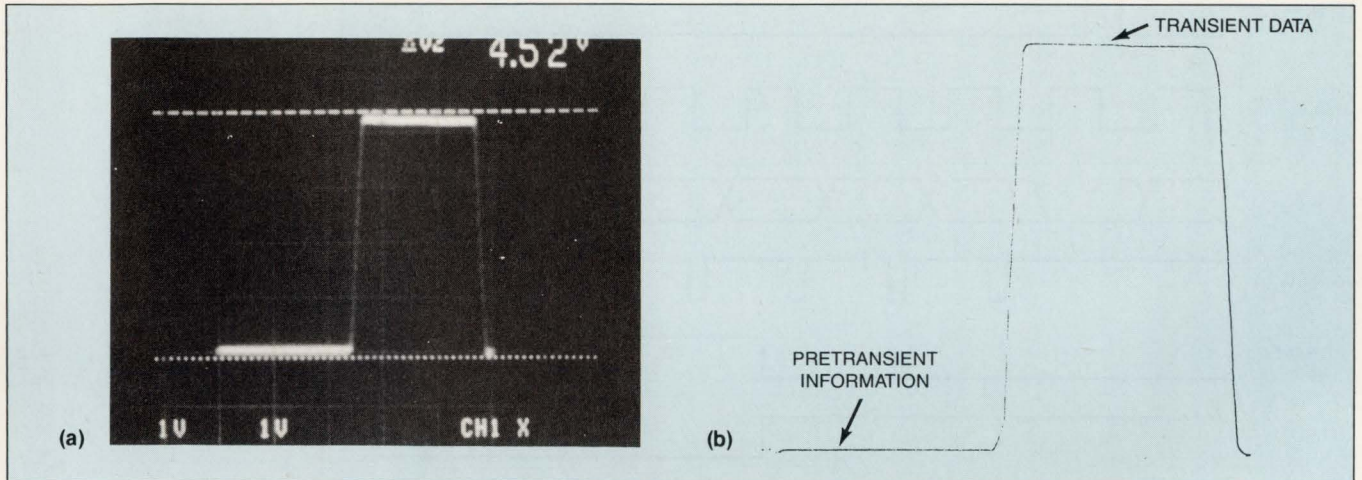


Fig 3—The recorder can display captured data on a scope, **a**, or on an X-Y pen plotter, **b**. The first half of each display shows data acquired before the triggering event.

a unipolar output range from 0 to 5V, with a resolution of 4096 steps.

The output of IC_{9B} drives the $\overline{\text{CSB}}$ input of IC₇ and also sets the logic level on IC₅'s output-enable line, $\overline{\text{OE}}$. This action latches the data from memory into DAC B, which drives the Y axis of the oscilloscope or plotter. By using dual supplies, you can set DAC B for a bipolar output range to reconstruct both positive and negative transients.

Counter 2 starts its count from the point at which it stopped at the end of the record mode; the first memory output word to IC₇ is the oldest sample in memory. The scan will then proceed through the 2048 samples of pretransient information and the 2048 samples of transient information. The output of each sample from memory to the Y axis, via DAC B, corresponds to the output of a count value from counter 1 to the X axis via DAC A. In this way, the circuit reconstructs the pretransient and transient waveforms.

For oscilloscope display of waveforms, place S₂ in the scope position. Doing so locks out CLK IN₂ from the rest of the circuit but allows CLK IN₁ to operate as clock signal for the circuit. Unlike the plotter display option, where counter 1 runs through once and then stops, CLK runs continuously. CNT FIN does go high when counter 1 reaches a count of 4095, but because the output of IC_{14C} is high, the DIS PLOT CLK signal does not go low. You can see the typical oscilloscope waveform display in Fig 3(a).

You display the stored waveform on an X-Y plotter by placing S₂ in the plotter position. Doing so locks

out the CLK IN₁ input from the rest of the circuit and permits CLK IN₂ to generate the clock signal for the circuit. IC_{16B}, IC₁₀, IC₁₁, and IC_{12A} function in a manner similar to the record mode to generate a high CNT FIN signal. But this time, IC₁₀ and IC₁₁ go low when counter 1 reaches a count of 4095. IC_{13A} goes low, and, because the output of IC_{14C} is already low, the DIS PLOT CLK signal goes low, turning off CLK IN₂ at IC_{18C} and holding the CLK signal high. Fig 3(b) shows a captured transient displayed using a plotter as the display method.

Record-mode timing and clock waveforms

The timing diagrams in Fig 4 show the logic relationships for the record mode. The MODE signal (not shown) is low and the DIS REC CLK signal is high. The RS₂ signal goes high when the recorder receives a reset command via S₃ resetting counter 2. The next falling edge of the CLK signal clocks out an address for IC₅ from counter 2. A conversion is also initiated on this falling CLK edge, and, within 700 nsec, the $\overline{\text{INT}}$ signal of IC₆ goes low, activating the $\overline{\text{WE}}$ input of IC₅. The rising edge of CLK resets the $\overline{\text{INT}}$ line 50 nsec later.

When the circuit detects a transient, the TRANS REC signal goes high, causing the RS₁ line to go low and releasing counter 1 from its reset state. The next falling edge of CLK clocks out the outputs from counter 1. When the count output from counter 1 reaches 2047, the CNT FIN signal goes high and causes the DIS REC CLK signal to go low, shutting off the CLK signal.

To accurately capture fast events, you need a high-speed A/D converter and a wide-bandwidth track/hold amplifier.

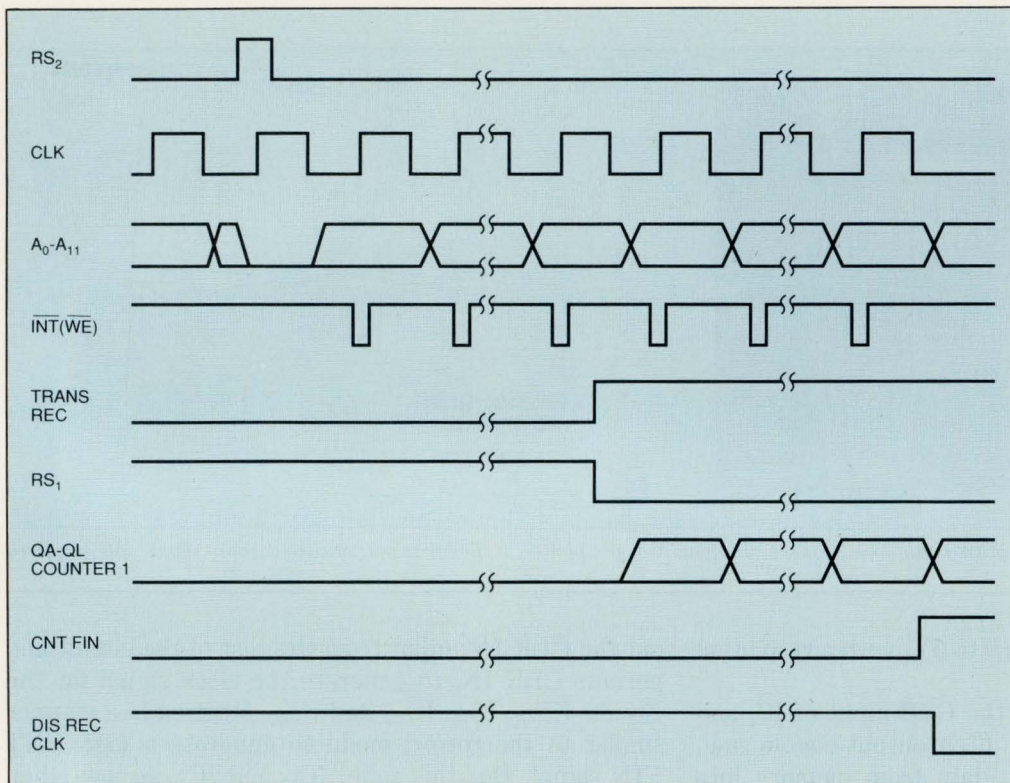


Fig 4—The timing relationships in the record mode show that recording starts on the first falling clock edge after the reset line goes high.

In the record mode in the waveforms shown, the 50/50 mark/space ratio of the CLK signal limits the clock frequency to 660 kHz. You need a CLK-low time of 750 nsec for the A/D converter to perform its conversion correctly and latch the data into IC₅. However, the CLK-high time can be as short as 350 nsec, the time required between conversions by the AD7821. Therefore, if the input to CLK IN₁ has a low time of 750 nsec and a high time of 350 nsec, the circuit can make one conversion every 1100 nsec—equivalent to approximately 900k samples/sec.

Playback to a scope

During playback to an oscilloscope, (Fig 5(a)), the MODE signal, the \overline{WE} input of IC₅, and the DIS REC CLK signal are high. When you place S₁ in the playback mode, RS₁ goes high, resetting counter 1. The CLK signal generates a \overline{CSA} signal for IC₇ on its rising edge and a \overline{CSB} signal on its falling edge. The falling edge of the CLK signal clocks data from counter 1, and the rising edge of \overline{CSA} updates the X axis. The falling edge of \overline{OE} outputs stored data from memory, and the rising edge of \overline{CSB} updates the Y axis. The CLK signal runs continuously when the circuit is in the scope-playback mode.

The timing diagram of Fig 5(b) shows operation of

the circuit for playback on a plotter. Once again, MODE, the \overline{WE} input of IC₅, and the DIS REC CLK signals are high. The circuit generates \overline{CSA} and \overline{CSB} to update the X and Y axes. Compared with scope playback, the difference in the circuit's operation is that when the output count from counter 1 reaches 4095 and the CNT FIN signal goes high, the DIS PLOT CLK signal goes low, forcing the CLK signal into a high state.

Burst-mode event sampling places requirements on an A/D converter similar to those for transient recording. In burst-mode sampling, the recorder looks at the input waveform infrequently, but when it does, it must acquire a large number of samples in a short time. With slower microprocessors or microcontrollers, you'll find that because of instruction- and bus-timing constraints, you can't achieve anything like the A/D converter's maximum throughput.

You can overcome timing limitations in a burst-mode sampler by using a DMA controller to initiate A/D conversions and transfer conversion data to memory. Doing so lets you run the A/D converter at or near its maximum sample rate, permitting high oversampling ratios and the acquisition of short transients.

Building a burst-mode sampler is a simple matter with the popular 8052 microcontroller (Fig 6). Al-

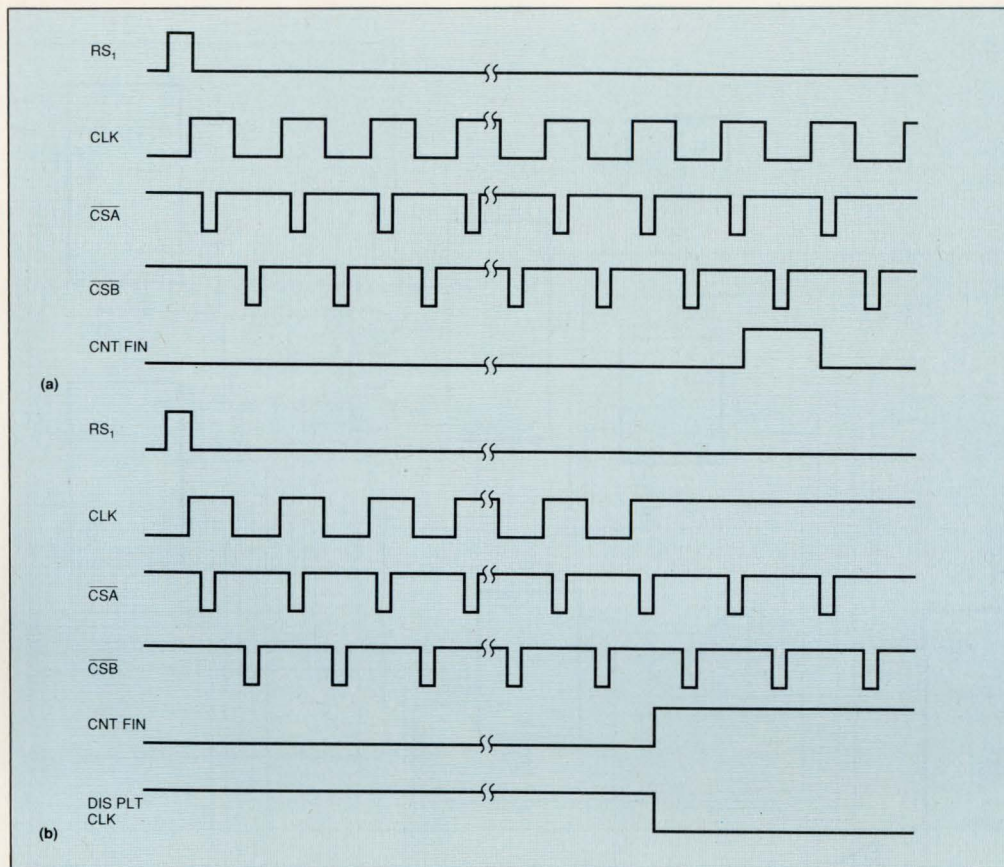


Fig 5—The timing for waveform playback is almost the same in the scope mode (a) as in the plotter mode (b). The difference is that the scope playback runs continuously, whereas the circuit produces a plotter output only once.

though the 8052 does not support hardware DMA, it does support what is termed “fake DMA.” However, expect the response time to DMA requests to be much slower than what is possible with microcontrollers that support genuine DMA.

The HM6264P memory chip, IC₃, stores the control program for IC₁. The first part of the control program is the initialization routine. This routine (Listing 1) sets up the sense of the DACK0 line of the 8237, IC₂, to be active high. It also loads the starting data address into IC₂ for the first conversion results. IC₁ initializes the counting register to control the number of conversions before IC₂ returns control to IC₁. The program must also set up IC₁ for “fake DMA.”

Once you’ve run the initialization program, IC₂ is ready to take control when requested to do so. Although IC₂ has four interrupt-request lines, this circuit uses only one, DREQ0. An external command signal drives this interrupt line high, telling IC₂ to take control of the circuit and start the A/D converter sampling the input waveform.

After IC₂ receives the DREQ0 request (Fig 7), its HRQ line goes high and feeds IC_{14C}, which takes the INT0 line of IC₁ low. IC₁ responds to this “fake DMA” request by bringing its P1.6 line low and the output of IC_{14A} high, selecting inputs of IC₇, IC₈, IC₉, and IC₁₀. When the output of IC_{14A} goes high, it shuts off IC₁’s address and data lines from the rest of the circuit and deselects the output’s address decoder, IC₁₃. The inverted P1.6 line also feeds the HLDA input of IC₂, acknowledging IC₂’s request for control. IC₂ then takes

control of the address and data bus and the sampling of the input waveform.

To reduce pin count, IC₂ multiplexes the eight higher-order address bits on the data lines. You need an external device to latch these address bits. The address strobe signal, ADSTB, takes AEN high and switches the \overline{OC} line of IC₆ low. ADSTB drives the C input of IC₆ to latch the higher address lines to the outputs of IC₆. The inverted AEN line also drives one input of IC_{16D}. The decoded output, Y₀, of IC₁₃ controls the other input of this gate. Therefore, either a high on AEN or a low on the decoder output selects IC₃. You need this control logic because both IC₂ and IC₁ must be able to access IC₃.

The DACK0 line goes high at about the same time that ADSTB latches the address and drives one input of IC_{15A}. IC_{15A} and IC_{15B} ensure that the \overline{CS} line of IC₄ goes low only when an input/output read operation of IC₂ occurs. IC_{15C} provides the correct polarity for the \overline{RD} input and equalizes the delay paths for the \overline{CS} and \overline{RD} lines, ensuring that the circuit obeys the \overline{CS} -to- \overline{RD} setup time.

Once IC₄ receives a \overline{CS} signal, it acknowledges receipt of the signal by bringing its RDY line low, placing the controller, IC₂, into a wait state for as long as its READY input is low. When the device completes a conversion, the RDY line goes high, releasing IC₂ from its wait state. Because IC₄’s RDY output is an open-drain output, you need to install an external pullup resistor, R₂.

When the circuit releases IC₂ from its wait state,

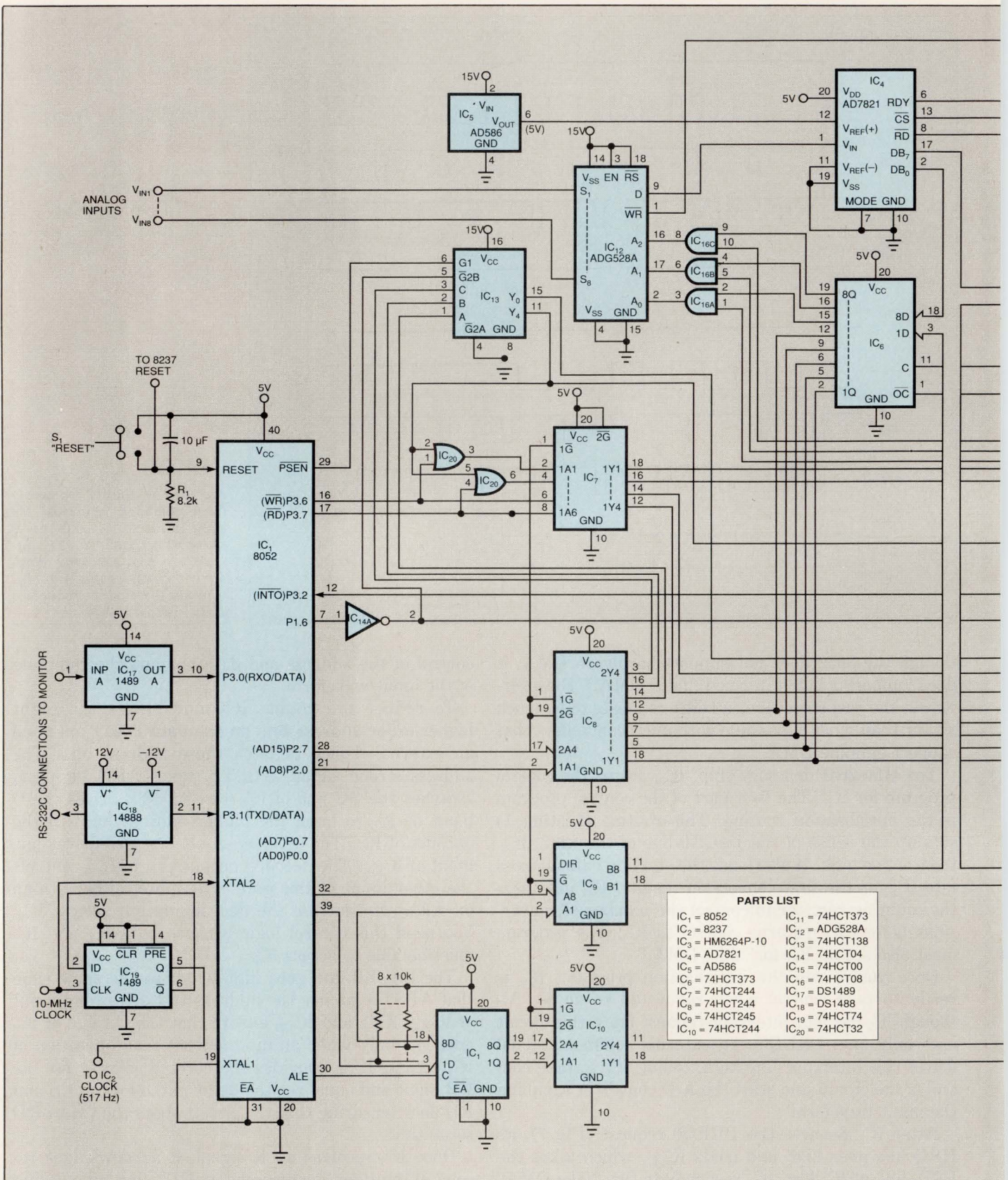
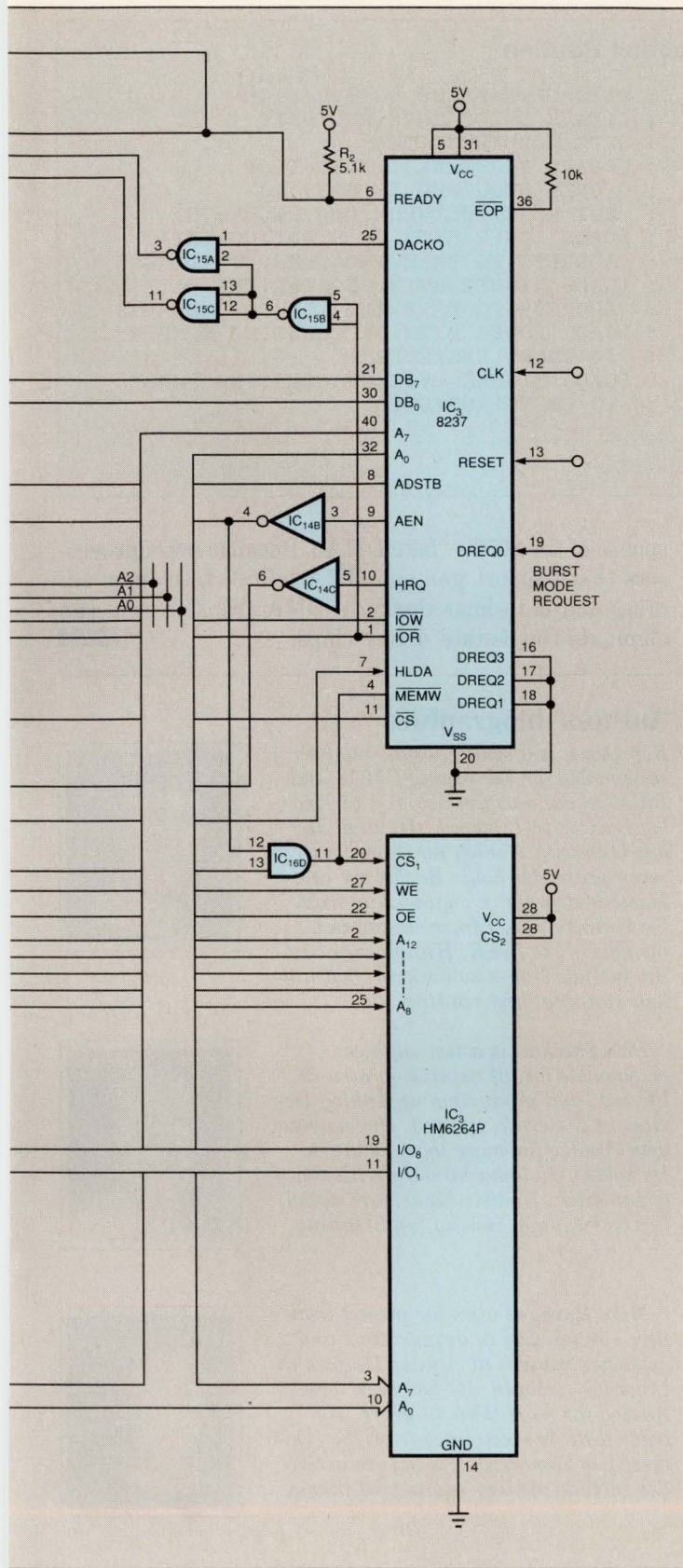


Fig 6—A burst-mode sampler using an 8052 microcontroller is roughly equal in complexity to the transient recorder shown earlier.

data from IC₄ is valid. The address lines of IC₂ determine where data loads into memory. IC₂ performs all of these operations automatically because a memory write accompanies each input/output read. Depending on the value loaded into the counting register, IC₂

will continue to issue read commands to IC₄ until the circuit completes the required number of conversions. IC₂ automatically increments the memory address after every write operation.

The multiplexer, IC₁₂, accommodates eight input



channels. The three upper and three lowest address lines of IC₂, gated through IC_{16A}, IC_{16B}, and IC_{16C}, select the input channel. If the three upper address lines are set to all 1s, IC₄ will convert each channel in sequence, and the conversion results will be stored in

consecutive memory locations. For example, if the first conversion takes place on the channel-1 input voltage, V_{IN1}, and the result is stored in location M of IC₃, the next conversion will take place on V_{IN2}, and the result will be stored in location M + 1. If the three uppermost address bits are set to 011, the circuit will sequence through channels 1 to 4 only.

Ready or not

The RDY line of IC₄ drives the \overline{WR} input of IC₁₂, loading the address for the next channel to be converted into the multiplexer. When you have only one input channel to convert, you can use an alternate design: Remove IC_{16A}, IC_{16B}, and IC_{16C}, and drive the A0, A1, and A2 inputs of IC₁₂ directly from the three uppermost address lines. Using this scheme, the program chooses the input channel.

IC₁ selects the device it talks to using a 1-of-8 address decoder, IC₁₃. The outputs of IC₁₃ provide signals for IC₁₂'s \overline{WR} line, IC₃'s \overline{CS} input, and IC₂'s \overline{CS} input. One of the outputs also gates the P3.7 (\overline{RD}) and the P3.6 (\overline{WR}) outputs from IC₁ to drive the \overline{IOW} and \overline{IOR} inputs of IC₂. The upper three address lines of IC₁ select the required device. The lower address lines are multiplexed with the data lines in a manner similar to the way IC₂'s address and data lines are multiplexed. IC₁₁ demultiplexes the lower eight address lines. IC₁'s ALE signal latches these address lines. The 3-state buffers, IC₇, IC₈, and IC₁₀, isolate IC₁ outputs from the address bus when IC₂ takes control. You must use these buffers because IC₁ can't place its address and data buses into a high-impedance state when IC₂ takes control of the circuit. IC₉ also acts as a buffer but is bidirectional because IC₁ must read data from and write data to memory.

IC₁ uses a 10-MHz input-clock frequency. A 74HCT74 counter (IC₁₉) divides down this clock to form the clock input to IC₂. The standard 8237 operates from a 3-MHz maximum clock frequency, so you can divide the 10-MHz clock by 4 to provide IC₂'s clock. You'll have a resultant acquisition rate of 608k samples/sec. A faster version of the 8237, the 8237-5, operates from a 5-MHz input clock, allowing you to divide the clock frequency by 2 and enabling the circuit to take 812k samples/sec. If you were to use IC₁ on its own to control the sampling of the input waveform, the best acquisition rate you could obtain would be approximately 100k samples/sec.

The entire circuit operates from 15V and 5V sup-

Listing 1—Initialization Routine

10	XBY(8008H) = 80H	: SETS DACK SENSE ACTIVE HIGH
20	XBY(800FH) = 0EH	: CLEARS DREQ0 MASK REGISTER
30	XBY(800BH) = 94H	: SETS MODE REGISTER
40	XBY(800CH) = 00H	: CLEARS FIRST/LAST FLIP-FLOP
		: (ONLY REQUIRED IF 8237 IS
		: NOT RESET BETWEEN DMA REQUESTS)
50	XBY(8000H) = 00H	: LOADS LOWER BYTE OF STARTING DATA
		: ADDRESS TO BASE AND CURRENT ADDRESS
60	XBY(8000H) = 08H	: LOADS HIGHER BYTE OF STARTING DATA
		: ADDRESS TO BASE AND CURRENT ADDRESS
70	XBY(8001H) = 00H	: LOADS LOWER BYTE OF COUNTING NUMBER
		: TO COUNT REGISTER
80	XBY(8001H) = 02H	: LOADS HIGHER BYTE OF COUNTING NUMBER
		: TO COUNT REGISTER
90	DBY(38) = DBY(38).OR.02H	
100	IE = IE.OR.81H	
110	GOTO 10	

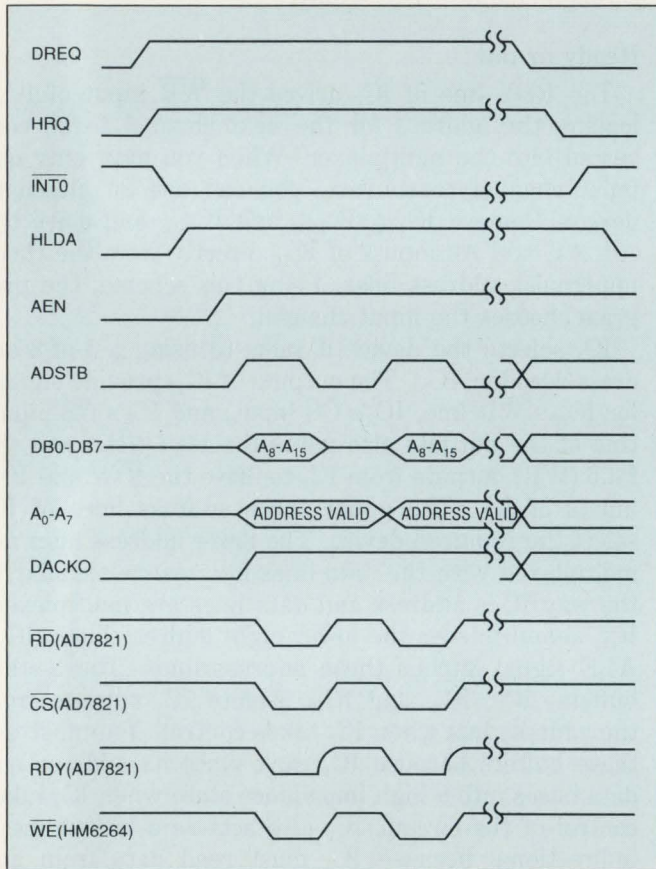


Fig 7—Although the 8052 does not support true DMA, you can create a “fake DMA” mode, which, though not as fast as real DMA, lets you transfer blocks of data directly to memory.

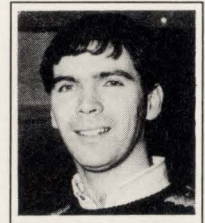
plies. If there isn't a 5V supply in your system, you can add a regulator to generate 5V. In addition, plan to use a precision 5V reference (IC₅) for the A/D converter, allowing an input range of 0 to 5V. To obtain accurate conversion results, you must obey the same guidelines regarding decoupling and grounding as apply to the transient-recorder circuit.

You can use the same design (Fig 6) with slow- and medium-speed microprocessors that support DMA requests. With these microprocessors, you'll find the DMA response time will be much faster than the re-

sponse of the 8052's “fake DMA.” Because microprocessors that support genuine DMA will 3-state their address and data lines during a DMA transfer, you can eliminate the 3-state driver chips. **EDN**

Authors' biographies

Ken Deevy is a senior design engineer responsible for developing CMOS and BiCMOS data-acquisition ICs at Analog Devices in Limerick, Ireland. He has been with Analog for more than seven years. He holds Bachelors' and Masters' degrees in engineering from the University of Limerick and is a member of the IEEE. His leisure activities include 5-on-a-side soccer, badminton, running, and reading.



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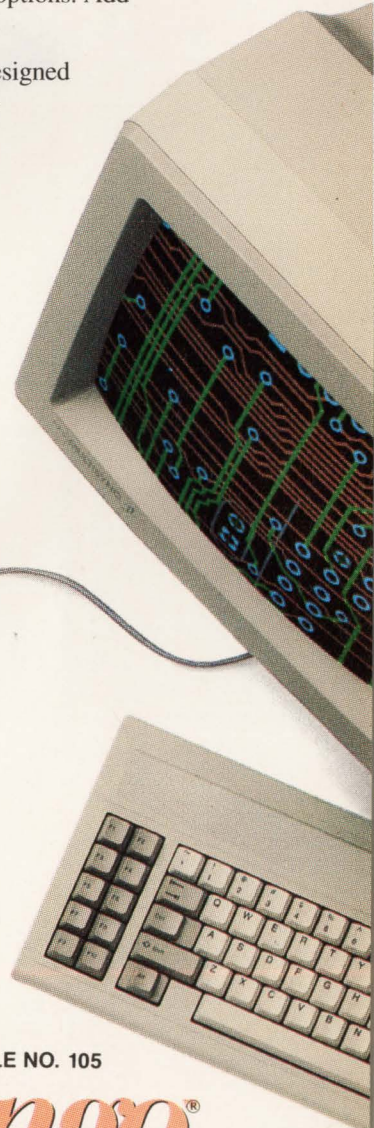
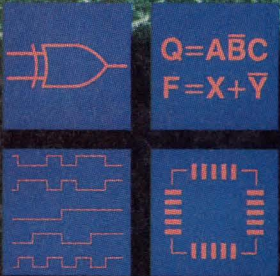
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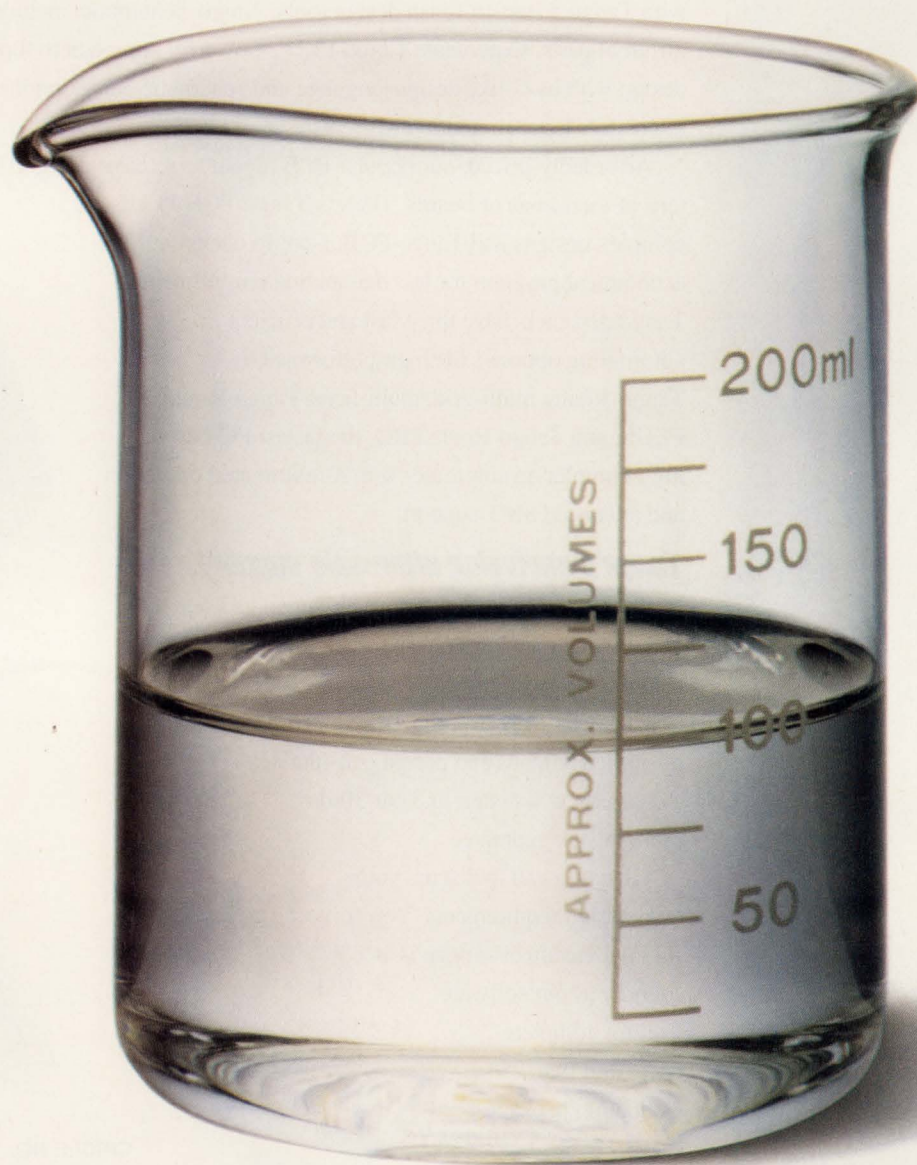
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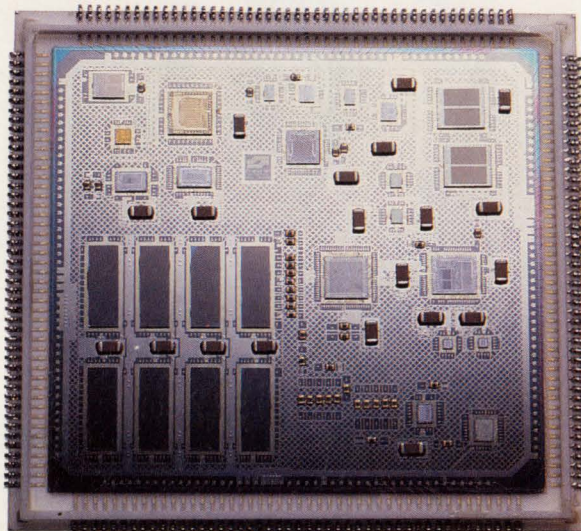
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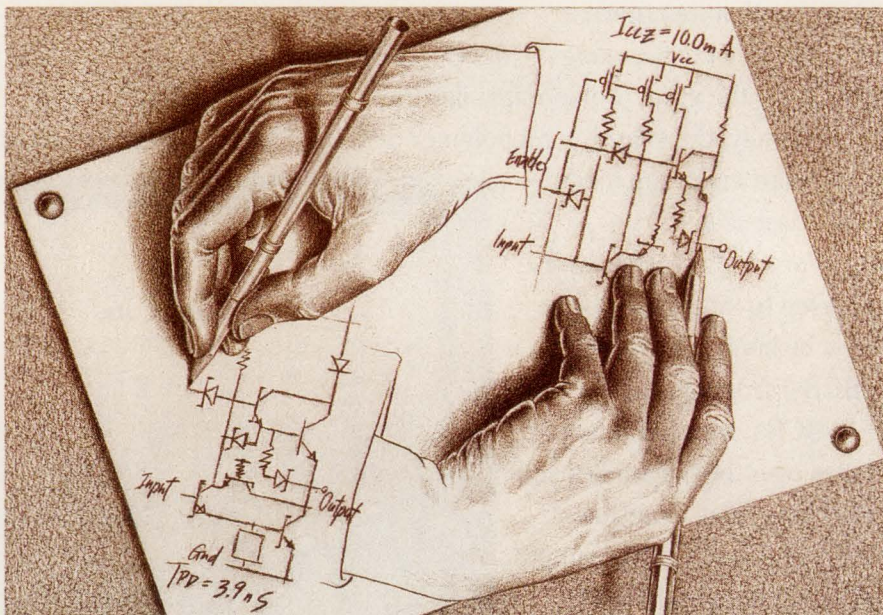
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	t_{PHL}	1.0	3.9	1.0	4.8	2.3	7.0
74BCT240	t_{PLH}	0.5	5.6	3.0	7.0	3.0	7.7
	t_{PHL}	0.4	4.0	1.5	6.5	1.5	5.0

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Feedback models reduce op-amp circuits to voltage dividers

An op amp's feedback factor defines a range of performance characteristics. Unfortunately, this factor is unknown for most op-amp applications because of a limited feedback model. By extending this model you can create a generalized feedback model that reduces op-amp circuit analysis to determining voltage-divider ratios.

Jerald Graeme, *Burr-Brown Corp*

The feedback factor of an op-amp circuit defines that circuit's performance more than any other parameter. The feedback factor sets the gain of the op amp's input-referred errors. These errors include offset voltage, noise, and the error signals generated by limited open-loop gain, common-mode rejection, and power-supply rejection. In addition, a circuit's feedback factor determines bandwidth and frequency stability. Yet this powerful performance indicator remains unknown for most op-amp applications. Except for the basic noninverting op-amp connection, the classic feedback model does not predict the feedback factors of op-amp circuits.

In the noninverting case, the closed-loop gain relates directly to the feedback factor; the application gain

itself determines the output errors and bandwidth. However, the relationship between the gain and feedback factor does not extend to other op-amp configurations. In other configurations, several conditions make the gain-feedback relationship unclear. The input and output signals of inverting op-amp connections, for example, combine on the feedback network to conceal the feedback factor. Other applications have both positive and negative feedback, which results in more than one feedback factor. In still other applications, bootstrap feedback adds another variable that the classic feedback model does not take into account. Without knowing the feedback factor, you must perform laborious calculations to determine these circuits' performance.

You can, however, extend the convenience of a feedback factor to these other circuits by modifying the classic op-amp feedback model. Specific connection examples can demonstrate the possible variations to this model. These variations are limited in number by the two inputs of an op amp; you can connect the input and feedback signals of an op amp in only a few ways. The examples in **Figs 1 through 11** demonstrate modeling principles that will let you create a feedback model for any op-amp configuration. The final example is a universal op-amp feedback model that has standardized performance equations.

For the noninverting op-amp configuration, a direct relationship between the closed-loop gain and the feedback factor simplifies analyzing circuit performance.

The feedback factor of an op amp defines the circuit performance more than any other parameter.

Fig 1 shows this configuration as a voltage amplifier. This noninverting circuit provides the familiar, ideal closed-loop gain (A_{CLI}): $A_{CLI} = (R_1 + R_2)/R_1$. This gain amplifies both the input signal (e_i) and the differential input errors (e_{ID}) of the op amp. Multiplying the input-referred amplifier errors by A_{CLI} yields the resulting output errors.

As you can see in the Fig 1 model, the mechanism relating both the input and output errors is the feedback factor. This model represents the noninverting op-amp connection by an amplifier with differential-input-error signal e_{ID} and feedback factor β . This feedback factor defines the portion of the output signal (e_o) that feeds back to the amplifier input. Writing a loop equation for this model shows that $e_o = (1/\beta)(e_i - e_{ID})$. Thus, the feedback model shows that $1/\beta$ —rather than A_{CLI} —amplifies e_i and e_{ID} .

To resolve this amplification difference, define the noninverting amplifier's feedback factor. The feedback factor is the fraction of the amplifier's output that feeds back to its input. In Fig 1, the voltage-divider action of the feedback resistors sets the fraction of e_o fed back to the op-amp input: $\beta e_o = e_o R_1 / (R_1 + R_2)$.

This relationship defines β as the voltage-divider ratio of the feedback network. Comparing this result with the A_{CLI} expression shows that $A_{CLI} = 1/\beta$ for the noninverting op-amp configuration. Thus, the circuit and model are in agreement for the input-to-output transmission of amplifier errors.

The types of amplifier errors this model takes into

account are numerous because e_{ID} includes errors related to several amplifier characteristics. Each of these characteristics produces an input-referred error source for the op amp. The following formula represents error sources related to op-amp input-offset voltage (V_{OS}), input-noise voltage (e_N), open-loop gain (A), common-mode rejection ratio (CMRR), and power-supply rejection ratio (PSSR). The last three error terms include circuit signals: the output voltage (e_o), the common-mode voltage (e_{ICM}), and the change in power-supply voltage (δV_S):

$$e_{ID} = V_{OS} + e_N + (e_o/A) + (e_{ICM}/CMRR) + (\delta V_S/PSRR).$$

To find the amplifier output errors each of these terms creates, multiply each term by the $1/\beta$ factor of the application circuit. Some familiar error terms result from this multiplication. The output error due to the finite open-loop gain becomes $e_o/A\beta$, which shows that the output signal is diminished by a fraction equal to the reciprocal of loop gain $A\beta$. The decline of open-loop-gain A with frequency makes this output error rise, thus shaping the closed-loop frequency response of the circuit. The output-noise error term is e_N/β , leading to the term "noise gain" for $1/\beta$. This description of $1/\beta$ is accurate only under certain bandwidth limits. For both the loop-gain and noise errors, greater insight into circuit performance results from frequency-response analysis.

For the noninverting circuit in Fig 1, the multiplier

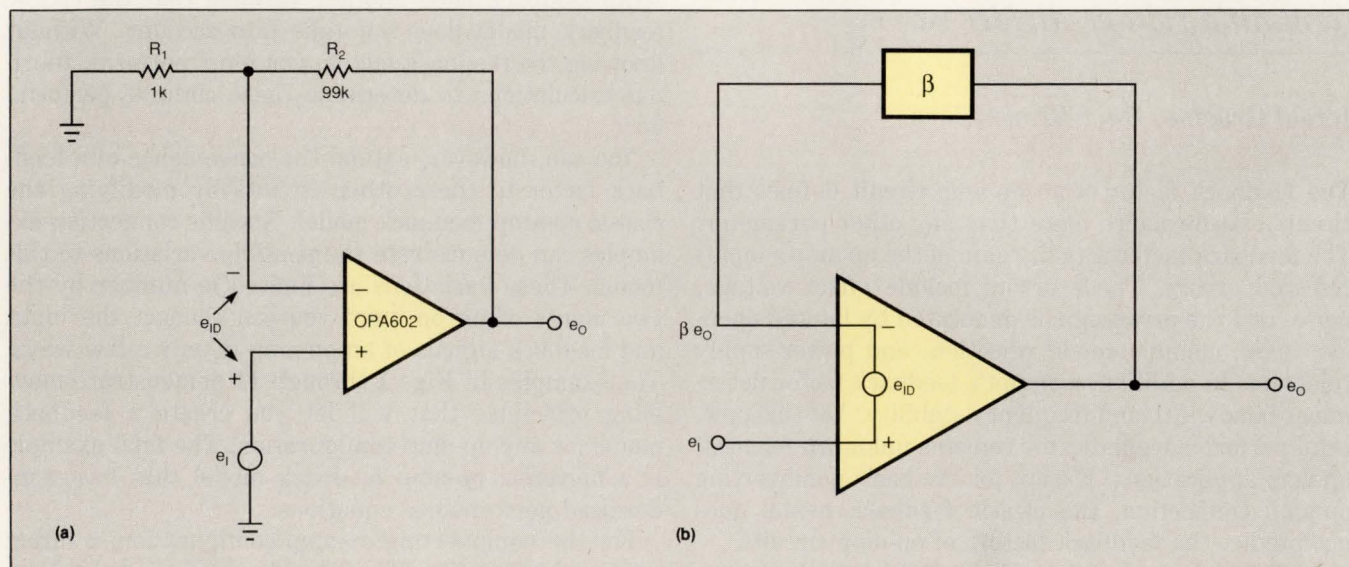


Fig 1— Op-amp input errors of the circuit schematic (a) are amplified by the reciprocal of the feedback factor, $1/\beta$, in the model (b).

that relates the input and output errors conveniently equals A_{CL} . Other op-amp configurations do not share this convenience. For these configurations, you must determine the $1/\beta$ factor independently of the ideal closed-loop gain. Once you determine this factor, the error-analysis process is the same as that of the Fig 1 circuit.

For these more-complex op-amp configurations, you need to use feedback modeling to determine the feedback factor. This modeling also yields frequency-response and frequency-stability information. To demonstrate modeling, consider the familiar noninverting circuit in Fig 2. This noninverting configuration highlights the voltage-divider action of the feedback network. For more general use, the network has impedances Z_1 and Z_2 rather than the resistors in Fig 1. As before, the network's divider action controls the fraction of the amplifier output fed back to the amplifier input. The Fig 2 circuit reduces input-error-signal e_{ID} to the value of the open-loop gain error, e_o/A . This reduction is due to the fact that the feedback modeling focuses only on gain and related frequency characteristics. Nevertheless, the one input-referred error is sufficient to define the feedback factor for use with the previous multi-error analysis.

Fig 2 also shows the feedback model for the noninverting op-amp connection. This classic feedback model, initially developed by Black (Ref 1), is generally proposed for op-amp circuits. However, this model ap-

plies only to the noninverting case and needs modification for other configurations. The model represents amplifier gain by gain-block A. A summation block, Σ , drives the inputs of the gain block. The summation block's inputs are input-signal e_i and feedback-signal βe_o . The feedback signal flows through feedback-attenuator block β . The summation block applies different polarities to the two signals, as the + and - signs indicate. These polarities correspond to the amplifier-input polarities of the actual circuit.

You can demonstrate the validity of the model by comparing the closed-loop-gain (A_{CL}) responses for the model and the circuit. For the model, the output signal is $e_o = A(e_i - \beta e_o)$. Solving this equation for e_o/e_i defines the modeled transfer response of the noninverting circuit as

$$A_{CL} = e_o/e_i = A/(1 + A\beta).$$

For the actual circuit of Fig 2, the transfer response of a noninverting amplifier is

$$A_{CL} = \frac{e_o}{e_i} = \frac{A}{1 + \frac{AZ_1}{Z_1 + Z_2}}.$$

Comparing the terms in the last two equations shows that the feedback factor is $\beta = Z_1/(Z_1 + Z_2)$.

The preceding analysis confirms the accuracy of the

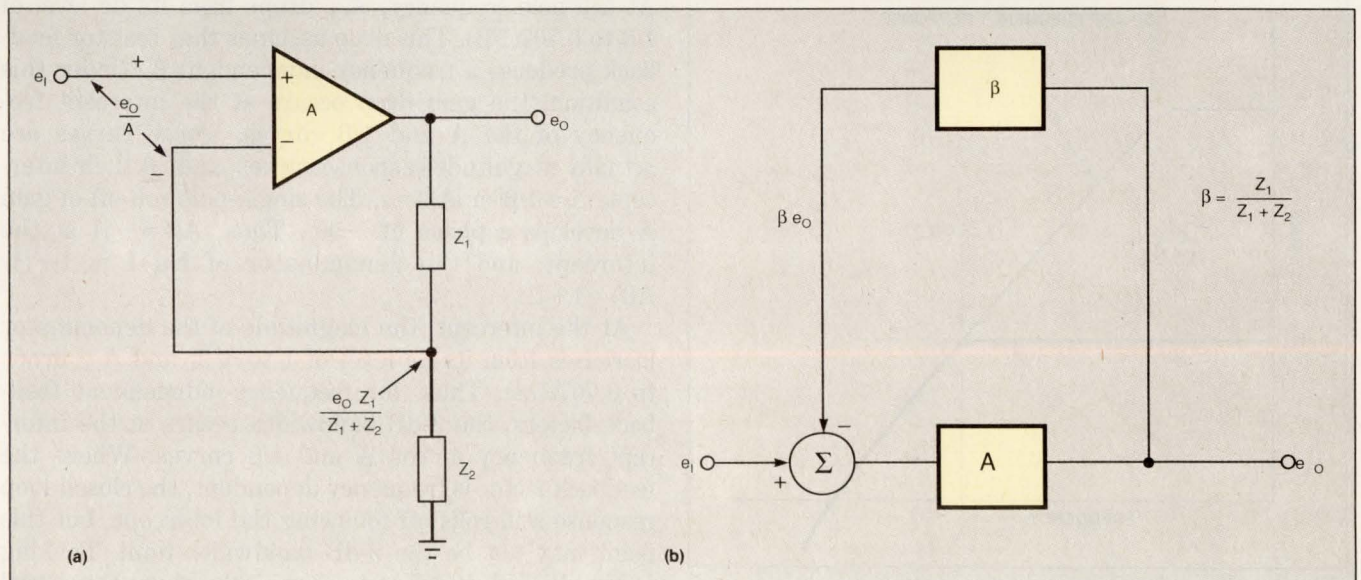


Fig 2—A comparison of circuit (a) and model (b) responses shows that the classic feedback model predicts op-amp performance in noninverting connections.

Except for the basic noninverting case, the classic feedback model does not predict the feedback factor of op-amp circuits.

Fig 2 model and provides the basis for determining the frequency response and stability of the circuit. This added performance information is based on the feedback factor and is not specific to the noninverting case. Using feedback modeling, you can derive the frequency characteristics of an op-amp circuit by analyzing the model's closed-loop-response equation (Ref 2). For the noninverting case, you can rewrite this equation as

$$A_{CL} = \frac{1/\beta}{1 + 1/A\beta} \quad (1)$$

Other op-amp configurations have different closed-loop-response equations, but these equations always have the same $1 + 1/A\beta$ denominator. This common denominator is central to the bandwidth and stability characteristics that hold for all op-amp configurations.

The frequency response of the Fig 2 circuit begins with the value of the ideal closed-loop gain (A_{CLI}) at dc. Because the op-amp open-loop gain (A) is very high at dc, the previous closed-loop-response equation simplifies to the ideal gain of the noninverting circuit: $A_{CLI} = 1/\beta$. At higher frequencies, the op-amp open-loop gain declines, causing the closed-loop gain to drop from the ideal value. This drop produces the circuit's bandwidth limit, as shown in Fig 3, which is a plot of the

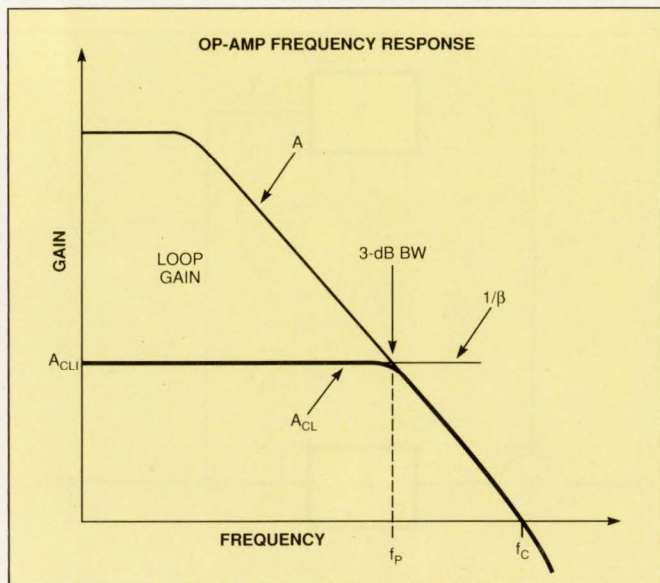


Fig 3—The feedback factor indicates op-amp bandwidth and stability through the relationship between the $1/\beta$ curve and the open-loop-gain curve, A .

op amp's closed-loop response, its open-loop gain, and the reciprocal of the feedback factor. All three variables of the original closed-loop-response equation are plotted on the same graph. The manner in which these variables interact in Fig 3 provides visual insight into bandwidth and frequency-stability limits.

The circuit-loop gain, $A\beta$, represents the amplifier gain resource available to maintain the ideal closed-loop response. In Fig 3, the separation between the A and $1/\beta$ curves represents the loop gain. Because of the logarithmic scale of response plots, this separation equals $\log(A) - \log(1/\beta)$, which equals $\log(A\beta)$. Thus, at any given frequency, loop-gain $A\beta$ is the vertical distance between the A and $1/\beta$ curves. Where the loop gain can no longer match the feedback demand, the closed-loop curve drops from the ideal A_{CLI} . The A and $1/\beta$ curves graphically define this point. The $1/\beta$ curve represents the feedback demand, and ideal closed-loop requirements are met as long as $1/\beta$ is below the open-loop-gain curve. Where this condition is no longer true, the actual response drops and follows the amplifier open-loop response downward. The rate of descent for the roll-off is -20 dB/decade for most op amps, a slope that is characteristic of a single-pole response. The heavier curve in Fig 3 represents the resulting closed-loop gain, A_{CL} .

The location of pole f_p in the A_{CL} response roll-off determines the closed-loop bandwidth of the circuit. At the pole frequency, A_{CL} drops from its dc level of $1/\beta$ to $0.707(1/\beta)$. This drop assumes that resistor feedback produces a frequency-independent β . Under this condition, the gain drop occurs at the intercept frequency of the A and $1/\beta$ curves. These curves are actually magnitude response curves, and, at their intercept, $|A| = 1/|\beta|$ or $|A\beta| = 1$. The single-pole roll-off of gain A develops a phase of -90° . Thus, $A\beta = -j1$ at the intercept, and the denominator of Eq 1 is $1 + (1/A\beta) = 1 + j1$.

At the intercept, the magnitude of the denominator increases from its dc level of 1 to $\sqrt{2}$, and A_{CL} drops to $0.707(1/\beta)$. Thus, for frequency-independent feedback factors, the 3-dB bandwidth occurs at the intercept frequency of the A and $1/\beta$ curves. Where the feedback factor is frequency dependent, the closed-loop response still rolls off following the intercept, but this point may not be the 3-dB bandwidth limit. Peaking in the closed-loop response curve may move the actual 3-dB point away from the intercept frequency.

For more-common op-amp applications, the feedback

factor is constant, and a simple equation defines the 3-dB bandwidth. The open-loop response of most op amps has a single-pole roll-off. Virtually all intercepts of the A and $1/\beta$ curves occur in this single-pole range. In this range, the gain magnitude is $A = f_c/f$, where f_c is the unity-gain crossover frequency of the amplifier. At the intercept, $f = f_p$, and $A = 1/\beta = f_c/f_p$. Solving for f_p , the 3-dB bandwidth (BW) for most op-amp applications is $BW = f_p = \beta f_c$.

This result holds for all op-amp applications having frequency-independent β s and a single-pole op-amp roll-off. In other cases, you find the 3-dB response limit by considering the added phase shift caused by the increased amplifier roll-off or by a frequency-dependent feedback factor.

Knowing the A_{CL} frequency response, you can refine the simple analysis of **Fig 1** so you can apply it to broader frequency ranges. The previous analysis showed that input-referred errors of op amps transfer to the amplifier output through a gain of $A_{CLI} = 1/\beta$. However, both A_{CLI} and $1/\beta$ are independent of the amplifier's high-frequency limitation. The **Fig 1** analysis is valid only when the op amp has sufficient gain to support the feedback demand. The 3-dB bandwidth marks a response roll-off that reduces amplification of both the signal and the error. Thus, op-amp error signals receive a gain of $A_{CLI} = 1/\beta$ only to the frequency where $BW = \beta f_c$. Beyond this limit, the gain available to error signals rolls off and follows the op-amp open-loop response in **Fig 3**.

This roll-off produces the difference between $1/\beta$ and the noise gain. The noise gain follows the roll-off **Fig 3** describes even though the $1/\beta$ curve continues uninterrupted. The denominator of the A_{CL} equation (**Eq 1**) expresses this roll-off. The closed-loop error gain, A_{CLE} , is

$$A_{CLE} = \frac{1/\beta}{1 + 1/A\beta} \quad (2)$$

This error gain is frequency dependent. Higher-frequency noise and CMRR and PSRR errors receive diminishing gain. Note that A_{CLE} depends on only the variables β and A . Any feedback model with β and A blocks configured as in **Fig 2** yields the same expression for A_{CLE} . This model configuration and the A_{CLE} result apply to all op-amp configurations.

Using response plots like **Fig 3**, you can evaluate

the frequency stability of an op-amp circuit from the curve slopes. The slopes of the A and $1/\beta$ curves at their intercept indicate phase shift for a critical feedback condition. At this intercept, $|A\beta| = 1$; a loop phase shift of 180° makes $A\beta = -1$. Then, the $1 + (1/A\beta)$ denominator of **Eq 1** is zero, and A_{CL} is infinite. With infinite gain, a circuit can support an output signal in the absence of an input signal, meaning the circuit can oscillate. To prevent oscillation, you must keep the phase of $A\beta$ below 180° . To prevent response ringing, you must further limit this phase to 135° or less.

You determine the loop phase shift by relating phase shifts to the slopes of the gain magnitude and $1/\beta$ curves. The relationship between the response slope and the phase shift is based on the effects of response poles and zeros. A pole creates a -20 -dB/decade response roll-off and -90° of phase shift; a zero produces the same effects but with opposite polarities. Additional poles and zeros add response slopes and phase shifts in increments of the same magnitudes. The slope and phase correlation is an accurate approximation when the critical intercept is well separated from response-break frequencies. When the intercept is less than one decade from a response break, you have to use a more detailed phase analysis (**Ref 2**). Even in these cases, the response slopes provide insight into probable stability behavior.

Relying on the slope and phase correlation, you determine the feedback phase shift from the gain magnitude and $1/\beta$ curves. The intercept point in **Fig 3** occurs after the amplifier's first pole develops the 90° phase shift but well before the second pole has any effect. At the intercept, the gain-magnitude curve has a slope of -20 dB/decade, and the $1/\beta$ curve has zero slope for a net 90° feedback phase shift. The result leaves a phase margin of 90° from the 180° needed to cause oscillation. The zero slope of the $1/\beta$ curve in **Fig 3** is characteristic of voltage-amplifier op-amp applications. In these applications, resistors form the feedback network. In other applications, capacitors are often part of this network and effect a nonzero $1/\beta$ slope.

Inverting configuration extends model

You can define the feedback factor and closed-loop gain for less obvious op-amp configurations by extending feedback modeling. The following examples demonstrate modifications of the **Fig 2** basic feedback model that you need for alternate signal and feedback connections. In each case, the A_{CL} transfer-function

The input and output signals of inverting op-amp connections combine on the feedback network to obscure the feedback factor.

has a denominator of $1 + (1/A\beta)$, and **Eq 2** describes the error-signal gain.

The first example is the simple inverting op amp (**Fig 4**). This circuit interchanges the ground and e_1 connections of **Fig 2**. This modification complicates determining the feedback factor for both the circuit and the model because the fraction of the amplifier output fed back to the input is not immediately obvious. The inverting input of the op amp is held near zero voltage by the inherent operation of an inverting circuit. This action results because the voltage at the inverting input receives counteracting signals from e_0 and e_1 .

The signals the op amp receives result from the voltage-divider action of the feedback network; e_0 and e_1

drive the divider at opposite ends. Superposition of these divider actions shows that the signal at the amplifier's inverting input or summing junction (e_{SJ}) is

$$e_{SJ} = \frac{e_0 Z_1}{Z_1 + Z_2} + \frac{e_1 Z_2}{Z_1 + Z_2}$$

The first term of this equation shows that $Z_1/(Z_1 + Z_2)$ remains the fraction of the output fed back to this input. Thus, for op-amp feedback networks, the feedback factor is the voltage-divider ratio of the network, regardless of the signals present in the actual circuit.

Analyzing **Fig 4** with the feedback model requires you to adjust for the input-signal connection. The classic feedback model of **Fig 2** shows e_1 driving a noninverting or positive input at the summation point. This arrangement corresponds to the signal connection at the amplifier's noninverting input. However, in **Fig 4**, e_1 is coupled to the amplifier's inverting input rather than its noninverting input. **Fig 4** accommodates this difference by changing the sign of the corresponding summation input. In op-amp feedback modeling, assign all summation inputs the same polarities as the corresponding amplifier inputs.

Also, the **Fig 2** model shows e_1 connected directly to the summation point in accordance with the direct connection of the circuit. **Fig 4**, however, shows e_1 connected to the feedback network rather than directly to the amplifier input. This network attenuates the amplifier input as the equation for e_{SJ} reflects. To include this attenuation in the feedback model, **Fig 4** adds feed-forward factor α . This feed-forward factor is the fraction of the input signal fed forward to the amplifier input. As with the feedback factor, a voltage-divider ratio of the feedback network defines the feed-forward factor. For α , the divider ratio is taken from the opposite end of the feedback network. For **Fig 4**, $\alpha = Z_2/(Z_1 + Z_2)$. In practice, every input signal connection to a feedback model has a corresponding α . For direct signal connections to amplifier inputs, α is unity.

Extended model simplifies inverter analysis

Using these model adjustments, you can extend feedback analysis to predicting the performance of inverting circuits. The feedback model of **Fig 4** sums the input and feedback signals for $e_0 = A(-\alpha e_1 - \beta e_0)$. Solving this equation for e_0/e_1 yields the model response. **Fig 4** compares the model with the corresponding circuit. Comparing terms confirms the defined values of

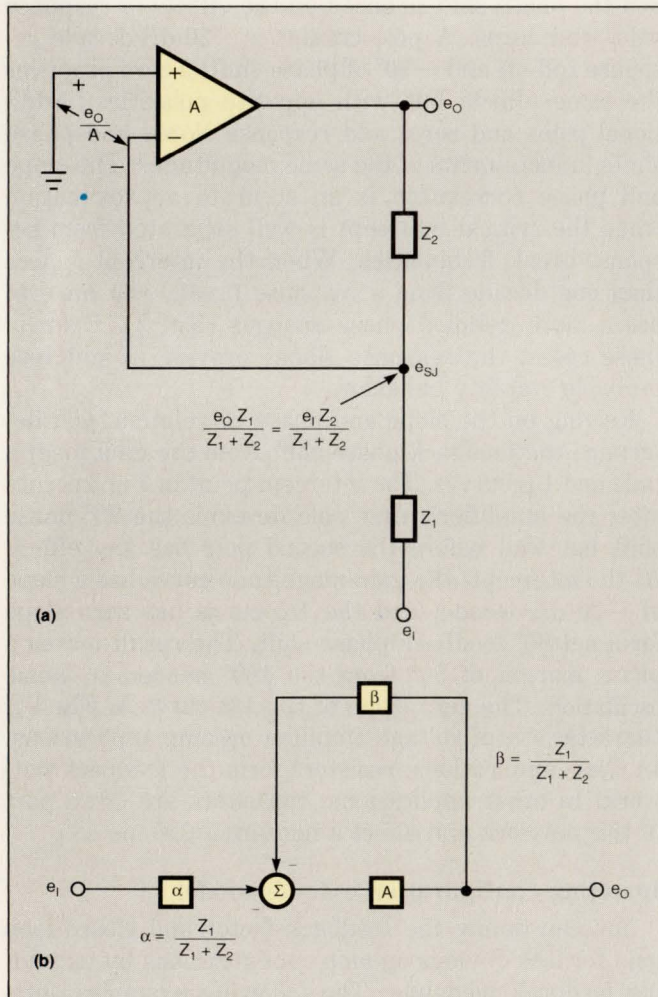


Fig 4—Inverting op-amp circuits (a) require model modifications (b) for an input signal that is attenuated and delivered to the opposite amplifier input.

α and β . Rewriting the model result shows that the closed-loop gain of the generalized inverting circuit is

$$A_{CL} = \frac{-\alpha/\beta}{1+1/A\beta} \quad (3)$$

When the loop-gain $A\beta$ is large, the equation reduces to the ideal closed-loop gain of $A_{CLI} = -\alpha/\beta = -Z_2/Z_1$.

The magnitude of this closed-loop gain is lower than the $(Z_1 + Z_2)/Z_1$ of the noninverting case, but the bandwidth is not correspondingly higher. This relationship results from the fact that the feedback factor—not the closed-loop gain—controls the bandwidth. The two circuits have the same feedback factor even though their gain magnitudes are different. As a result, the gain-bandwidth product drops when the circuit changes from the noninverting to the inverting configuration.

To quantify bandwidth for the inverting case, the previous noninverting analysis transfers directly. This transfer results from the standard form of the response equations. The noninverting bandwidth was derived from the denominator of the A_{CL} response (Eq 1). That same $1 + (1/A\beta)$ denominator applies to the inverting case as Eq 3 shows. In both cases, the A_{CLI} numerator reflects the ideal closed-loop gain. As in Fig 2, the bandwidth for the inverting op-amp connection is βf_C , even though the closed-loop gain has decreased.

This βf_C relationship extends to all other op-amp configurations as well. You can write the transfer response of any negative-feedback system in a form that includes the $1 + (1/A\beta)$ denominator. In this form, the numerator of the response equation reflects the ideal closed-loop gain. This gain describes the transfer response when $A\beta \gg 1$, thus making the denominator essentially unity. The standard equation for the generalized transfer response for any op-amp configuration is

$$A_{CL} = \frac{A_{CLI}}{1+1/A\beta}$$

Feedback modeling can reduce the transfer response of any op-amp connection to this generalized form. The conclusions you draw from this standard equation translate to all op-amp connections. Rederiving the characteristics of each individual configuration is unnecessary. The only variable factor is ideal-gain A_{CLI} , which you express in terms of α and β combinations that are unique to a given configuration. For a given configuration, you can find A_{CLI} by writing the re-

sponse of the feedback model in the standard form.

You can also express the op-amp input-error gain, A_{CLE} , in a generalized form. In this case, there are no differences between the equations for different amplifier configurations. For Fig 4, this gain is the gain of error-signal e_O/A . This gain also affects the other input-referred error signals of e_{ID} . For the Fig 4 circuit, you can find A_{CLE} by using superposition and a test signal. Setting e_I to zero, you add a second error signal, such as noise (e_N), to the e_O/A error signal. This procedure has the same effect as adding an e_N generator in series with the amplifier's noninverting input. The gain of this configuration amplifies such a signal, and

$$A_{CLE} = \frac{1/\beta}{1+1/A\beta} \quad (4)$$

Thus, A_{CLE} for the inverting configuration is the same as that of the noninverting case. Further examples show this equation to be true for all configurations. Op-amp input-referred error signals are amplified by $1/\beta$ up to the response roll-off the $1 + 1/(A\beta)$ denominator creates. From the Fig 3 discussion, this roll-off starts with the closed-loop bandwidth of the amplifier. Beyond this bandwidth limit, A_{CLE} follows the op amp's open-loop response.

Multiple paths extend possibilities

Other variations of op-amp configurations result from dual feedback paths or dual input-signal connections. Fig 5 shows a configuration with feedback to both amplifier's inputs. A voltage-follower connection provides unity feedback to the inverting input, and a feedback network supplies positive feedback to the noninverting input. Normally, positive feedback degrades circuit stability, but, in the Fig 5 example, the opposite is true. Positive feedback is useful when a greater negative feedback makes the overall circuit feedback negative. The combined feedback effects determine circuit operation, as feedback modeling illustrates.

The purpose of the dual feedback is to achieve voltage-follower operation with an op amp that is not phase compensated for unity-gain stability. Normally, a voltage follower must have unity-gain stability because of the follower's unity feedback. However, some op amps lack this stability because of reduced internal phase compensation. Numerous op amps offer different degrees of phase compensation. Often, one product ver-

You can extend the feedback-factor convenience to all op-amp circuit configurations through feedback modeling.

sion will have unity-gain stability but will also have a far slower slew rate than a lesser compensated version. The slew rate of the OPA37 in Fig 5 is 12V/ μ sec, and the device's phase compensation is set for gains of five or greater. A companion product, the OPA27, has unity-gain phase compensation, but its greater compensation reduces the slew rate to 2V/ μ sec. Typically, the devices' slew rates differ by a factor approximately equal to the minimum gain of the lesser compensated version.

Modifying the circuit's feedback factor makes the higher slew rate available to the voltage follower. The modification reduces the feedback factor without altering the closed-loop gain, which removes the requirement for unity-gain phase compensation. The frequency stability of an op-amp configuration depends on the phase shift at the intercept of the A and 1/ β curves. Fig 5 shows these curves for the reduced phase compensation and added positive feedback of the example. Because of the reduced compensation, the open-loop-gain curve A exhibits two response poles above the unity-gain axis. As a result, the slope of this curve is -40 dB/decade when the curve reaches unity gain.

This slope corresponds to 180° of phase shift and indicates oscillation for a 1/ β intercept at unity gain. Normally, this intercept would result with a voltage follower where 1/ β = 1. However, the positive feedback of the Fig 5 circuit reduces the net feedback factor to raise the 1/ β curve. The raised curve places the inter-

cept in a region of reduced open-loop-gain slope and ensures frequency stability.

Raising the 1/ β curve also moves the intercept back in frequency, which reduces the closed-loop bandwidth. In practice, this bandwidth reduction is the same as that produced by using the unity-gain compensated version of the amplifier as a conventional voltage follower. In that case, the added internal phase compensation reduces the bandwidth. To get the greatest bandwidth from the circuit in Fig 5, set the intercept at the level of the amplifier's minimum rated gain. This intercept condition results in 1/ β = A_{MIN} , where A_{MIN} is the minimum stable gain the manufacturer specifies for the amplifier.

To permit this feedback setting, you must determine the value of β for Fig 5. Once again, the feedback-factor definition and the basic feedback model fail in this task. Determining the fraction of the output fed back to the input is complicated by the dual feedback paths. The classic feedback model of Fig 2 offers no help because it represents only one feedback path. Fig 6 extends the Fig 2 model to the dual-feedback circuit of Fig 5 by incorporating two adjustments. First, the model adds feed-forward factor α in series with the signal input, following the process described for Fig 4. However, the model couples e_1 to the positive inputs on the amplifier and summation elements.

The second model change is the addition of the β_+ feedback path, which connects to a positive input on

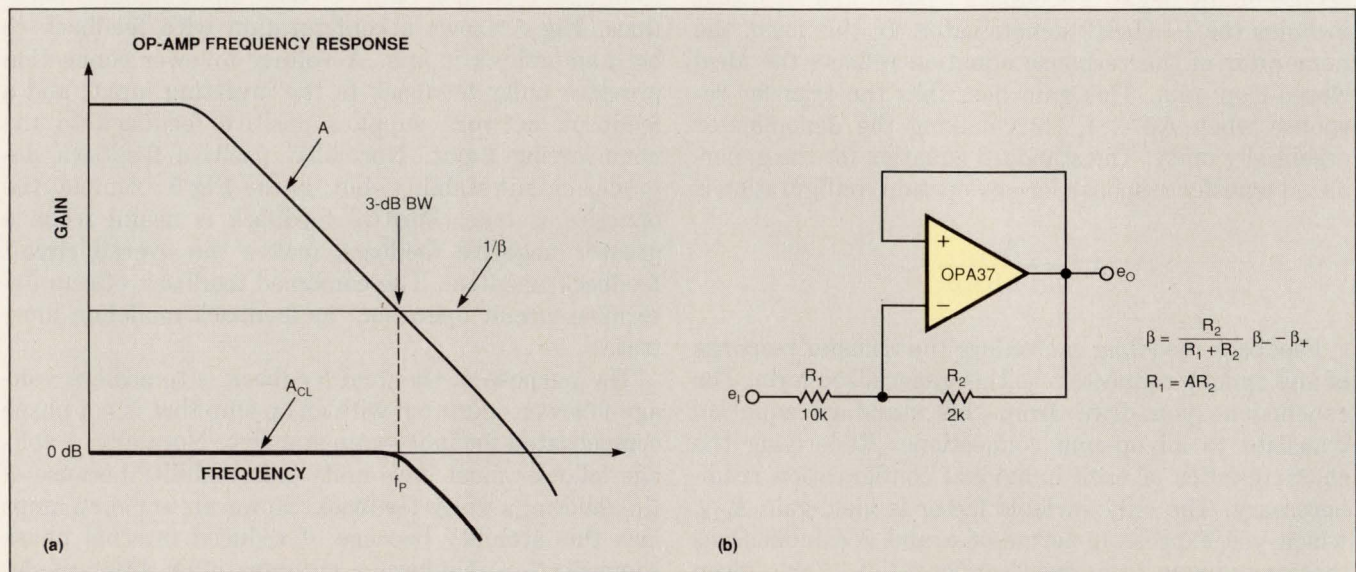


Fig 5—Feedback to both op-amp inputs separates the 1/ β and closed-loop-gain curves (a) for this high-slew-rate voltage follower (b).

the summation element. The summation polarity then matches that of the amplifier input the β_+ feedback-path affects. Feedback through β_- remains connected to a negative summation input, and the two feedback polarities reflect the differential nature of the amplifier. The differential inputs of an op amp cause the amplifier to respond to the difference between the signals at the two amplifier inputs. Thus, the amplifier subtracts the two feedback signals when the signals

are connected to opposite amplifier inputs. The model repeats this subtraction by using opposite signs for feedback inputs to the summation element.

Dual feedback subtracts feedback factors

The differential inputs' subtraction results in a net feedback factor that is the difference between the positive and negative feedback factors. Analyzing the circuit and model results in the response equations in Fig 6. The response denominator is of the standard form $1 + (1/A\beta)$ when the net circuit feedback factor is $\beta = \beta_- - \beta_+$. Then, the equations confirm the Fig 6 model to the amplifier configuration, and

$$A_{CL} = \frac{\alpha/\beta}{1 + 1/A\beta} = \frac{A_{CLI}}{1 + 1/A\beta}$$

$$\beta = \beta_- - \beta_+$$

Note that, because the net feedback is negative, the net feedback factor is $\beta_- - \beta_+$ rather than $\beta_+ - \beta_-$.

To determine the ideal gain, $A_{CLI} = \alpha/\beta$, express the α and β factors in terms of circuit elements. Although the equations for Fig 6 define these factors, depending on detailed equations is no longer necessary. Once the equations confirm the model, you do not need them to repeatedly analyze a given configuration. The A_{CL} expression of the model defines A_{CLI} in terms of factors you can determine by inspection. You determine the feedback and feed-forward factors from the associated voltage-divider ratios. The ratio is unity for the direct output-to-input connection of the Fig 6 β_- feedback. However, the Fig 6 model also holds for other cases in which a feedback network sets β_- .

For the specific circuit of Fig 6, the result is the desired voltage-follower response; however, the circuit amplifies any errors. Reading the individual factors from the Fig 6 circuit and subtracting the two β factors gives

$$\alpha = \beta = \frac{Z_2}{Z_1 + Z_2}$$

Thus, $A_{CLI} = \alpha/\beta = 1$ for the desired voltage-follower response. However, with $\beta < 1$, the input errors of the amplifier are amplified by $1/\beta > 1$. Given the β selection for Fig 5, $1/\beta = A_{MIN}$. Then, the input errors are amplified by approximately the same factor that slew rate is improved. For the specific components of Fig 5, the input errors are amplified by a factor of five, and the slew rate improves by a factor of six. The error-signal

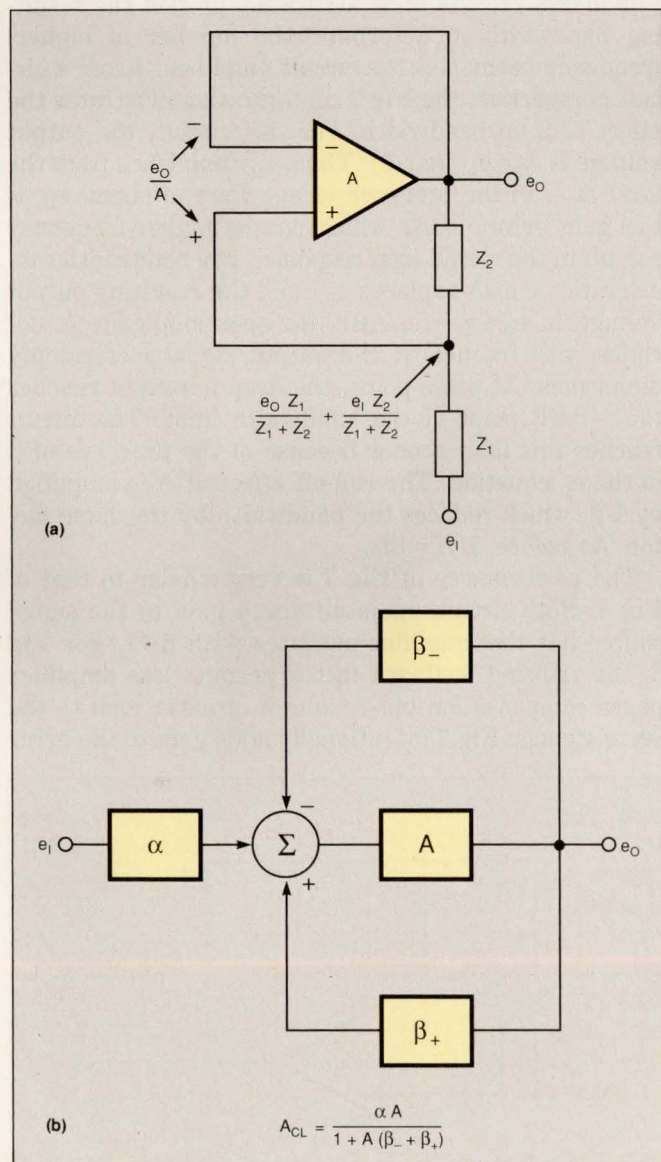


Fig 6—The dual feedback of the circuit in a results in a model with feedback factor, β , which is equal to the difference between the negative and positive feedback factors (b).

With feedback modeling, you can simplify op-amp circuit analysis to the determination of voltage-divider ratios.

gain rolls off in accordance with the amplifier open-loop response, as the equation for A_{CLE} (Eq 4) shows. You can remove the increased error gain for the input offset voltage by using a capacitor in series with R_2 in Fig 5.

The reduced input impedance of the Fig 5 circuit also increases the error. However, this effect is less than you would first expect. At first, the input impedance of the circuit appears greatly reduced because the input signal drives a feedback network. Normally a voltage follower presents the very high impedance of an op-amp input to the signal source. When driving the feedback network in an inverting circuit, the input signal sees the impedance of the input resistor. This great difference in input impedance would also result for Fig 5 except for the bootstrap action of the positive feedback. The follower action of the circuit keeps both ends of the feedback network at almost the same signal level. The only signal appearing on Z_2 in Fig 6 is the small e_o/A . Thus, the feedback network draws very little current from the signal source. The resulting input impedance is $R_1 = AZ_2$.

Dual inputs expand options

Still other op-amp configurations couple input signals to both inputs of the amplifier. For these configurations, modify the feedback model on the input rather than the feedback side. The input signals coupled to the op amp may be from the same signal source or from separate sources. In the simplest case, the same signal source supplies both op-amp inputs, serving to illustrate input modifications for the model.

Fig 7 shows the dual-coupling of a signal source to the two op-amp inputs. This circuit selectively amplifies the op amp's input-error signal for greatly improved resolution of error measurement. Distortion measurement is a prime beneficiary of this selective gain. Input-error-signal e_{ID} appears across R_1 and develops a feedback current of e_{ID}/R_1 . This current also flows through R_2 and develops an amplified replica of e_{ID} at the op-amp output. The resulting error-signal gain is $(R_1 + R_2)/R_1$. This gain equals $1/\beta$ as you can see by reading β from the voltage-divider ratio of the feedback network.

The amplification excludes test-signal e_1 because this signal does not appear across R_1 . The circuit bootstraps R_1 on top of e_1 ; the resistor supports only the amplifier-input-error signal. Signal e_1 shifts the op-amp input voltages without developing a voltage across R_2 . With no related signal on R_2 , the op-amp output follows e_1 . Thus, signal e_1 receives only unity gain from the circuit,

and the amplifier error signal receives a gain of $1/\beta$. Because of this selective amplification, the amplified error signal is far more prominent at the amplifier output. The selective gain reduces the dynamic-range requirements for the error measurement. In addition, the unity gain presented to e_1 lets this signal span the full voltage range of the op-amp input without causing output saturation.

However, this selective gain also reduces the feedback factor, resulting in bandwidth reduction. Distortion measurements must accurately predict the resulting bandwidth to determine the number of higher-frequency harmonics the circuit amplifies. From a circuit perspective, the Fig 7 configuration illustrates the effect of β on bandwidth. For this circuit, the output voltage is $e_o = e_1 - (e_{ID}/\beta)$. Thus, e_o diminishes from the level of e_1 in the presence of e_{ID} . Part of signal e_{ID} is the gain error, e_o/A , which causes higher-frequency roll-off in the closed-loop response. For bandwidth considerations, e_o/A replaces e_{ID} , and the resulting output voltage is $e_o = e_1 - (e_o/A\beta)$. As open-loop-gain A declines with frequency, the output signal increasingly diminishes. At some point, the drop in output reaches the -3 -dB point of the bandwidth limit. The circuit reaches this limit sooner because of the presence of β in the e_o equation. The roll-off effect of A is amplified by $1/\beta$, which reduces the bandwidth by the same factor. As before, $BW = \beta f_c$.

The performance of Fig 7 is very similar to that of Fig 5. Both circuits maintain unity gain to the signal source but the amplifier operates with $\beta < 1$. For Fig 5, the reduced feedback factor permits less amplifier phase compensation but results in greater gain to the error signals. Fig 7 intentionally adds gain to the error

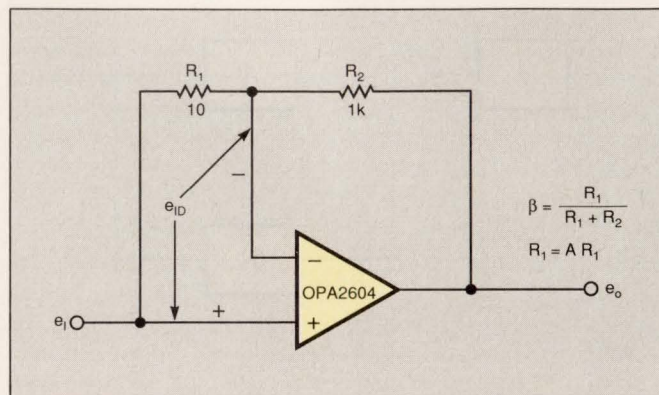
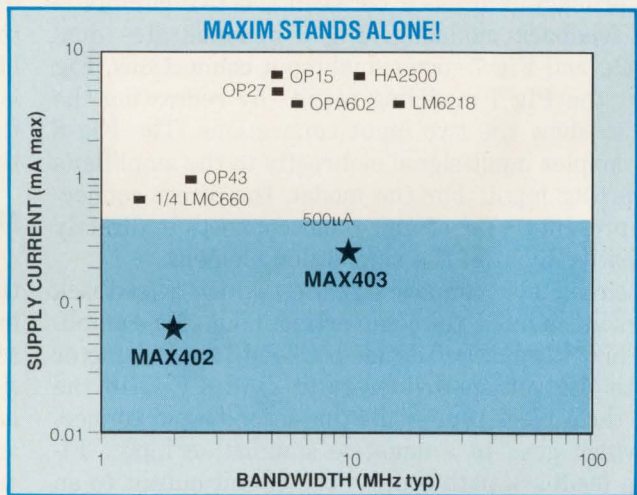


Fig 7—This circuit results in input signal coupling to both of the op-amp inputs when R_1 is boot-strapped to selectively amplify the error signal, e_{ID} .

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Using information based on the feedback factor, you can determine the frequency response and stability of an amplifier as well as its gain.

signal for measurement applications. The only difference between the two circuits lies in their applications. In practice, the circuits realize the same results through different configurations. From an applications standpoint, the two circuits are interchangeable.

The primary difference between the two circuits is in the feedback modeling. Fig 5 demonstrates dual feedback, and Fig 7 shows dual input connections. Fig 8 shows the Fig 7 modeling results by redrawing the circuit to show the two input connections. The Fig 8 circuit couples input-signal e_i directly to the amplifier's noninverting input. For the model, the direct connection represents an α of unity and connects e_i directly to a positive input of the summation element.

The circuit also couples signal e_i , which a feedback network attenuates, to the inverting input of the amplifier. This attenuation defines a feed-forward factor equal to the voltage-divider ratio $Z_2/(Z_1 + Z_2)$. In the model, the α block represents this second input connection, which goes to a negative summation input. Finally, a feedback path couples the circuit output to an amplifier input. In this path, the attenuation of the feedback network is $Z_1/(Z_1 + Z_2)$, which is the feedback factor. This feedback path connects to another negative summation input in the model, which corresponds to the inverting amplifier input connection of the circuit.

Analyzing the completed model produces a transfer response of the expected form:

$$A_{CL} = \frac{(1-\alpha)\beta}{1+1/A\beta} = \frac{A_{CLI}}{1+1/A\beta}$$

The denominator of this equation is the $1+(1/A\beta)$ result common to all of the previous results. Thus, bandwidth and stability conclusions previously drawn from this denominator also apply to the equations for Figs 7 and 8. The closed-loop bandwidth is βf_c , and frequency stability conditions relate to the intercept of the A and $1/\beta$ curves of Fig 3. The expression for the ideal closed-loop gain for the Fig 7 and Fig 8 circuits is the numerator of the equation, $(1-\alpha)\beta$. Substituting the expressions for α and β in this expression shows that $A_{CLI} = 1$.

Modeling extends simplicity

You can readily extend the modeling principles of the preceding examples to any op-amp application. Using this approach, the final circuit analysis reduces to a single loop equation. Moreover, feedback modeling simultaneously defines many circuit-performance characteristics while avoiding the more complex response analysis of the circuit. You analyze the actual circuit only when questions arise about the validity of the feedback model. The three steps of feedback analysis are drawing the model, determining the α and β factors, and finding the transfer response.

Drawing the model centers on the op amp's differential inputs. Feedback or input-signal connections to the op amp's inverting input are drawn as connections to negative inputs on the model summation element. Connections to the op amp's noninverting input are drawn as connections to positive summation inputs. An α or β attenuator accompanies each of these input and feed-

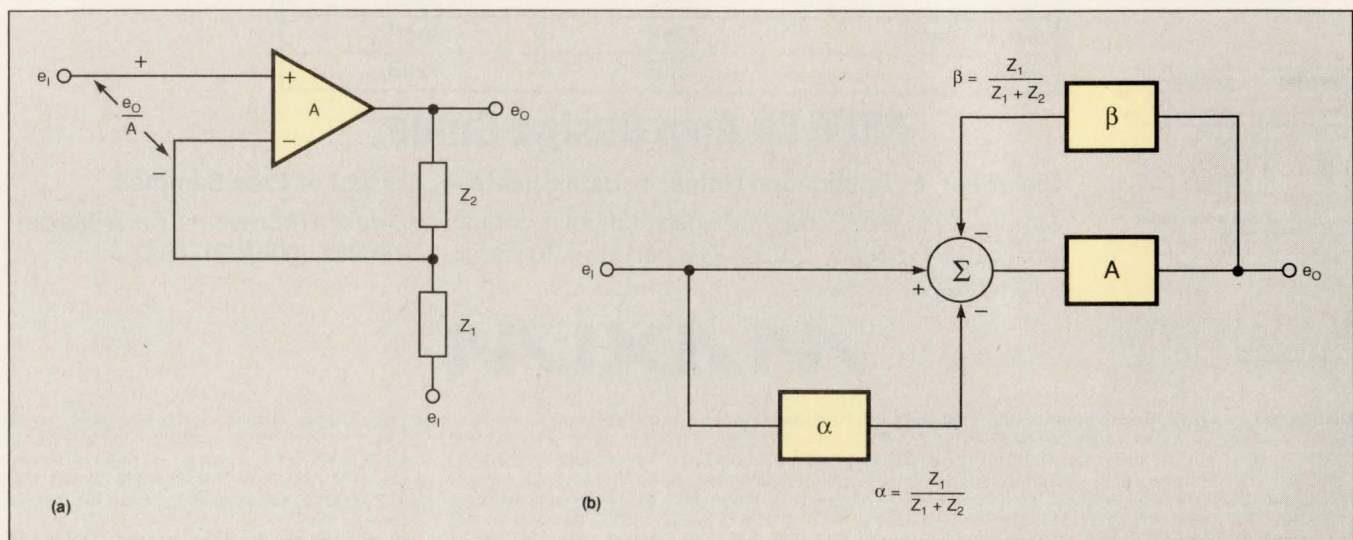


Fig 8—The direct and attenuated input connections of the circuit in a couple to opposite-polarity inputs of the feedback model (b).

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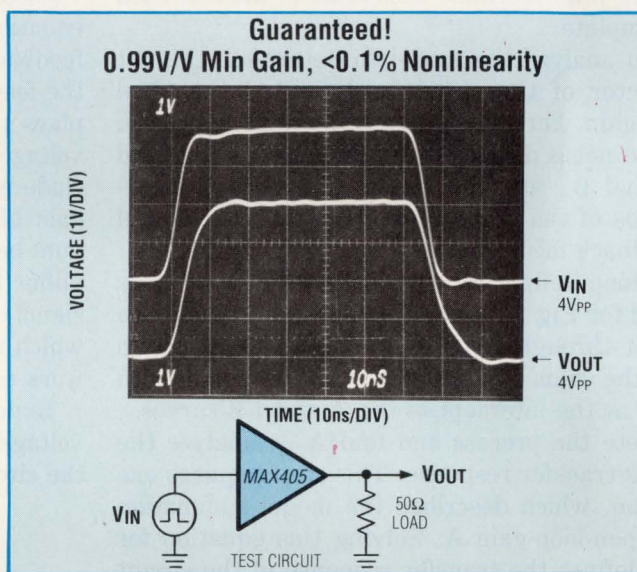
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The generalized feedback model covers each of the four possible input and feedback connections to the two op-amp inputs.

back connections. With just these polarity and attenuator guidelines, you draw the model itself. From the feedback networks, you find the individual α and β terms as voltage-divider ratios. Feedback and feed-forward signals drive a given network from opposite ends, resulting in different divider ratios. You find the two corresponding ratios by using superpositioning to separate the effects of the feedback and feed-forward signals. Once you determine these ratios, the feedback model is complete.

Next, you analyze the model to determine the net feedback-factor of the circuit and to find the ideal closed-loop gain. For most op-amp configurations, you can read the net β directly from the circuit. You read the individual β_- and β_+ factors from the voltage-divider ratios of the feedback networks. You can find the net feedback factor of the circuit from $\beta = \beta_- - \beta_+$. This step alone defines numerous performance errors as described for Fig 1. You can also find the bandwidth at this point through $BW = \beta f_c$. Where β varies with frequency, the value of beta used to find the bandwidth is the value at the intercept of the A and $1/\beta$ curves.

To complete the process and find A_{CLI} , analyze the model for its transfer response. This step requires one loop equation, which describes the model summation times the open-loop-gain A. Solving this equation for $A_{CL} = e_o/e_i$ defines the transfer response of the circuit in terms of A and the α and β factors. You then manipulate this result to arrange it in a standard form. The denominator of the A_{CL} result always reduces to the form $1 + (1/A\beta)$, and the resulting numerator is the ideal closed-loop gain, A_{CLI} . This standard-form requirement helps you detect analysis and modeling errors.

Complex circuit yields to modeling

To illustrate feedback analysis, consider the voltage-controlled current source of Fig 9 (Ref 3). Because of positive feedback, this op-amp connection produces an output current that is independent of the load voltage. The voltage load R_L develops acts as an input signal to the op amp's noninverting input. The amplification of this signal adjusts the op amp's output voltage by an amount that accommodates the load voltage. The added output voltage supplies a correction current through the positive feedback network R_2/n and R_2 form. This current accurately compensates the effect of the load voltage as long as you establish the illustrated 1:1/n resistor ratios.

The Fig 9 circuit is well known, but its performance

characteristics are not obvious. The circuit structure offers little insight into its bandwidth and the effects of input error signals. The voltage swing at the amplifier's output due to input and load voltages is not apparent. Furthermore, the circuit's positive feedback raises the question of frequency stability. Straightforward analysis of all these performance characteristics is a formidable task.

Feedback modeling reduces the task to one loop equation through the information you derive from the feedback factor and closed-loop response. Fig 10 shows the feedback-analysis circuit of Fig 9. This format displays positive and negative feedback factors through voltage dividers. To model the Fig 10 circuit, you include positive and negative feedback paths around the gain block. These paths meet summation-element inputs bearing the same signs as the corresponding amplifier inputs in the circuit. The model couples input-signal e_i to the summation element through an α block, which represents the attenuation of the feedback network e_i drives.

To define the α and β terms, take the corresponding voltage-divider ratios from the circuit diagram. For the circuit of Fig 10,

$$\alpha = \frac{1}{1+n}, \beta_- = \frac{n}{1+n}, \beta_+ = \frac{nR_1}{R_2 + (1+n)R_L}$$

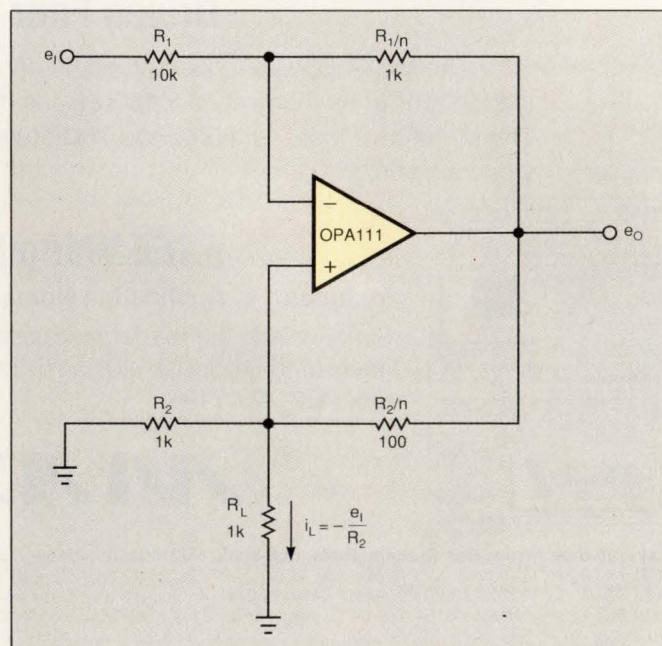


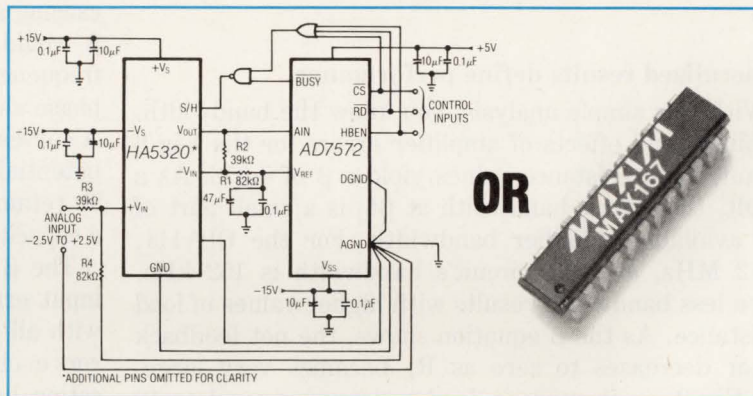
Fig 9—A complex feedback structure confuses calculation of circuit performance for this well-known current source.

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Using feedback modeling, you can derive the frequency characteristics of an op-amp circuit by analyzing the model's closed-loop response equation.

You find the net circuit feedback factor from

$$\beta = \frac{R_2}{R_2 + (1+n)R_L} \beta_-$$

Generalized results define performance

With this simple analysis, you know the bandwidth, stability, and effects of amplifier errors for the Fig 9 circuit. The resistance values yield a β of 0.076. As a result, the circuit bandwidth at βf_c is a small part of the available amplifier bandwidth. For the OPA111, $f_c = 2$ MHz, and the circuit's bandwidth is 152 kHz. Even less bandwidth results with higher values of load resistance. As the β equation shows, the net feedback factor decreases to zero as R_L becomes very large. For Fig 9, an increase in load resistance from 1 to 10 k Ω reduces the circuit bandwidth from 152 to 16 kHz. Normally, the values of R_1 and R_1/n would suggest a low-gain circuit for which the bandwidth would approach that of f_c . However, an almost equal β_+ counteracts the near-unity β_- , and the resulting feedback demand for amplifier gain is high.

The frequency-stability information revealed by the β equation is twofold. First, the equation shows that β is always a positive value, indicating that negative feedback prevails regardless of the load resistance. Otherwise, the positive feedback could have dominated the circuit to cause latching or oscillation. The β equa-

tion provides further stability information through graphical analysis. Oscillation can still result if R_L is an inductive load, such as that of a motor. In this case, the load impedance rises with increasing frequency, causing a corresponding decrease in β . This decreasing β would cause the $1/\beta$ curve of Fig 3 to rise with frequency. The increased $1/\beta$ slope signifies greater phase shift in the loop at the intercept of the $1/\beta$ and A curves. This increased feedback phase shift signifies potential response ringing or even circuit oscillation. To retain stability in these cases, bypass the load with a capacitor.

The β equations also show the effects of amplifier input errors on the Fig 9 circuit output current. As with all op-amp configurations, the input-referred errors e_{ID} includes are first amplified by $1/\beta$. This amplification determines the error effects at the op amp's output. From this output, the positive feedback network feeds back the errors through an attenuation factor of β_+ . This attenuated signal is across load R_L and develops an output error current of $(\beta_+/\beta)(e_{ID}/R_L)$. Typically, β_+/β is large, and the effects of e_{ID} are amplified in the load current. For the components of Fig 9, $\beta_+/\beta = 11$, which is the gain the circuit applies to the errors of e_{ID} before those errors appear across R_L .

Continuing the model analysis yields the Fig 9 transfer response. You derive the current-output response from the input-to-output voltage response, e_o/e_i . Using

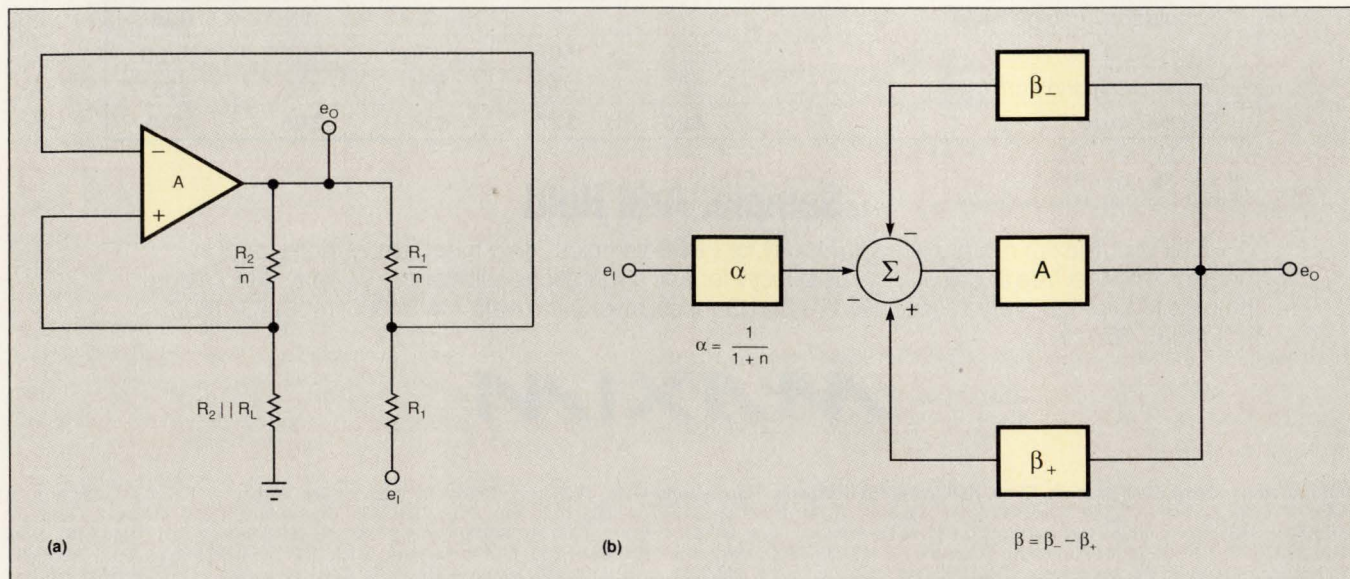


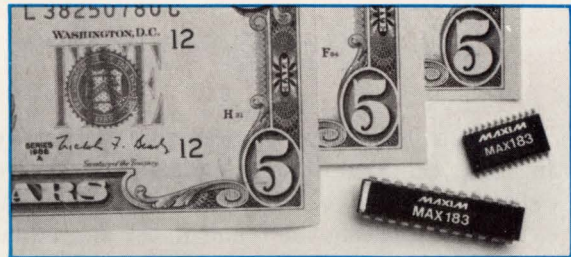
Fig 10—Translating the Fig 9 circuit into a feedback-analysis circuit (a) and then a feedback model (b) simplifies analysis and extends performance insight through standardized feedback results.

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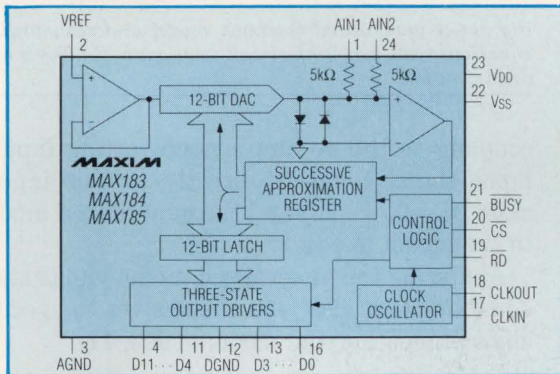
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Frequency plots let you evaluate the frequency stability of an op-amp circuit from the A and 1/β curve slopes.

the Fig 10 model, you find e_o/e_i from a single loop equation that you then reduce to standard form. From the model, $e_o = A(-\alpha_- e_i - \beta_- e_o + \beta_+ e_o)$. Solve this expression for $A_{CL} = e_o/e_i$ and manipulate the result to develop the standard denominator of $1 + (1/A\beta)$. For Fig 10,

$$A_{CL} = \frac{e_o}{e_i} = \frac{-\alpha/\beta}{1 + 1/A\beta}$$

You then translate this result to a current output by first noting that the load voltage equals the positive feedback signal, or $e_L = \beta_+ e_o = i_L R_L$. Solving this equation for e_o and substituting the result in the A_{CL} equation yields a Fig 9 response of

$$\frac{i_L}{e_i} = \frac{-1/R_2}{1 + 1/A\beta}$$

Generalized model covers all

Drawing and analyzing feedback models adds insight to op-amp circuit operation and works with any op-amp application. However, op-amp circuit analysis is even simpler with a generalized feedback model and standard response equations. These standardized results avoid even the single loop equation of the model analysis and hold for all practical applications. Op-amp circuit analysis then reduces to finding voltage-divider ratios, which you can generally determine by inspection.

The feedback model of Fig 11 represents all possible op-amp circuit configurations. This model includes input and feedback connections to both the positive and negative summation inputs. The separation between the possible and the practical excludes op-amp configurations that have no end value.

The Fig 11 model represents each of the four possible input and feedback connections to the two op-amp inputs. Most op-amp configurations do not use all of these connections. In these cases, you set the associated α or β terms to zero. Similarly, many op-amp applications have direct input or feedback connections to the op-amp inputs. In these cases, a network does not attenuate the related signals, and you set the associated α and β terms to unity. For example, the Fig 10 circuit has no input-signal coupling to the op amp's noninverting input. This lack of input-signal coupling sets α_+ to zero, and the Fig 11 model reduces to the model in Fig 10. Similarly, the Fig 8 circuit has no feedback

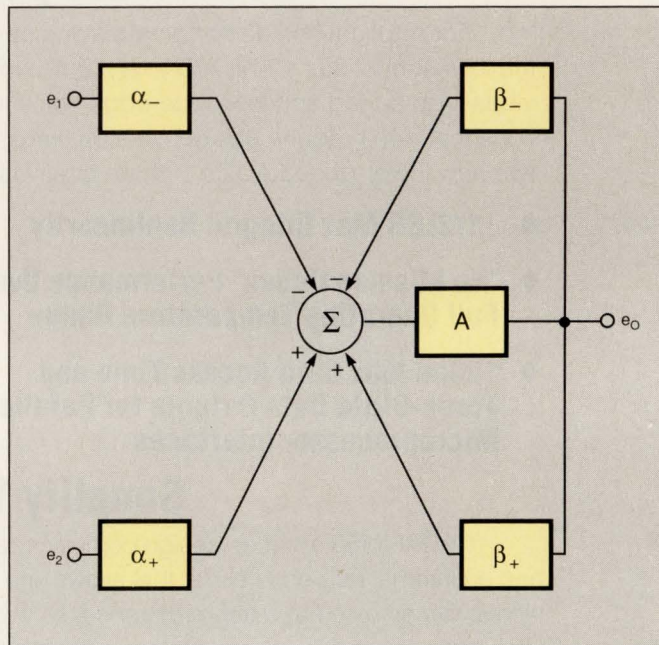


Fig 11—A generalized feedback model and standardized response equations reduce op-amp circuit analysis to finding α and β voltage-divider ratios.

coupling to the op amp's noninverting input, and the input signal connects directly to this input. In this case, $\beta_+ = 0$, $\alpha_+ = 1$, and the generalized model reduces to the model in Fig 8.

Analyzing the generalized model yields standardized equations that also lend themselves to specific op-amp applications. For the model of Fig 11,

$$A_{CL} = \frac{e_o}{e_i} = \frac{\alpha/\beta}{1 + 1/A\beta} = \frac{A_{CLI}}{1 + 1/A\beta} \quad (5)$$

$$\beta = \beta_- - \beta_+$$

This analysis immediately communicates three results common to all op-amp configurations. First, the net feedback factor of the circuit is $\beta = \beta_- - \beta_+$. In all cases, the differential inputs of the op amp subtract one feedback signal from the other. Next, the denominator of the A_{CL} equation is the familiar $1 + (1/A\beta)$. Thus, the bandwidth and frequency-stability conclusions drawn using this denominator still apply. As in Fig 3, the intercept of the $1/\beta$ and A curves sets the Fig 11 bandwidth $BW = \beta f_C$. Frequency stability relates to the curve slopes at this intercept, as also described for Fig 3. Finally, the numerators of Eq 5 show that the ideal closed-loop gain is $A_{CLI} = \alpha/\beta$ regardless of the op-amp configuration. Because of the denominator form of Eq

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5, A_{CL} reduces to the numerator term when loop-gain $A\beta$ is large. A large $A\beta$ again denotes the ideal region of operation.

Two variables in the generalized A_{CL} equation are defined differently for different op-amp configurations. This flexibility permits one standard response equation for all configurations. In the A_{CL} equation, both α and e_1 depend on the input connections of the specific circuit. The varied participation of the modeled α_- and α_+ determine feed-forward factor α . One or the other of these α terms applies to most op-amp connections; other connections involve both terms. Input signal connections dictate the relevant α terms. α_- attenuates signals connected to the e_1 terminal of the model; the signals then go to a negative summation input. For signals at the e_2 input, α_+ is the attenuator, and the summation input has a positive polarity.

The input signal, e_1 , in the standard equation accommodates this α variability; the modeled input signals are e_1 and e_2 . This generalized e_1 signal permits various combinations of signals e_1 and e_2 . You can model the input signal connections using one equation for inverting, noninverting, differential, and common-mode cases. For each of these cases, a corresponding α term results as summarized in the following table:

Cases	e_1	α
Inverting	e_1	$-\alpha_-$
Noninverting	e_2	α_+
Differential	$e_2 - e_1$	$\alpha_+ = \alpha_-$
Common mode	$e_1 = e_2$	$\alpha_+ - \alpha_-$

Examining this table shows agreement with previous modeling results. From the table, an inverting input connection of e_1 couples through α_- to a negative input. Hence, the table's α term and polarity. This is the input case for Fig 10, which has a $-\alpha = -\alpha_-$ term in the response equation's numerator. For Fig 6, the input signal couples to a noninverting amplifier input for a $\alpha = \alpha_+$ term in the numerator of Eq 5. Similarly, Fig 8 shows a common-mode input case, and the resulting response numerator has a factor of $1 - \alpha$, which is $\alpha_+ - \alpha_-$. For the differential-input case, the table shows that Eq 5 accepts $e_1 = e_2 - e_1$ for $\alpha = \alpha_+ = \alpha_-$.

One additional standard equation applies when using the generalized model. The equation for error-signal gain is

$$A_{CLE} = \frac{1/\beta}{1 + 1/A\beta}$$

For the model, consider an input error source, $-e_{ID}$, directly coupled to a positive summation input. This addition indicates that the amplifier input errors are in series with the input circuit. With the e_{ID} source connected to the model, analysis shows that Fig 11 amplifies input-referred errors by the same gain described earlier.

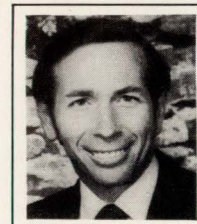
EDN

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Author's biography

Jerald Graeme has been with Burr-Brown for 25 years and is the manager of instrumentation components design. Jerry has developed numerous linear ICs including op amps, instrumentation amplifiers, analog multipliers, V/F converters, and D/A converters. He has a BSEE from the University of Arizona, and a MSEE from Stanford University. In his leisure time, he enjoys scuba diving, photography, and woodworking.



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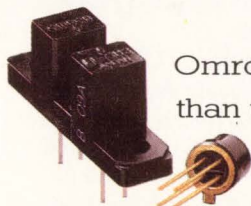
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SOFTWARE PROGRAMMABLE FEATURES			
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CIRCLE NO. 113



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DESIGN IDEAS

EDITED BY ANNE WATSON SWAGER

Diode sensor compensates laser

Gheorghe Stoenescu and Neculai Grosu
Institute of Atomic Physics, Bucharest, Romania

Laser-receiver circuits must bias their avalanche photodiodes (APD) to achieve optimal gain. Unfortunately, an APD's gain is dependent on the operating temperature. The circuit in Fig 1 controls the operating voltage of an APD over a large temperatures range to maintain the gain at the optimal value. The circuit uses D_1 as a temperature sensor thermally matched with the APD.

A voltage regulator, IC_1 , supplies the necessary reference voltage to the circuit. IC_{2A} and Q_1 bias D_1 at a constant current. IC_{2B} , IC_{2C} , IC_{3A} , IC_{3B} , and IC_{3C} amplify D_1 's varying voltage and set Q_2 to the optimal gain corresponding value. Potentiometer R_1 controls

the amplification over a range of 5 to 15. R_2 controls the voltage level, which corresponds to the optimal gain of the APD at 22°C (the temperature is specific to the type of APD).

Fig 1 was tested with an RCA C 30954E APD. The tests covered the -40 to +70°C temperature range and used a semiconductor laser. The laser radiation was transmuted on the APD's active surface in the climatic room via an optical-fiber cable. The gain varied by at most ± 0.2 dB over the entire temperature range. EDN BBS /DL SIG #974

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To Vote For This Design, Circle No. 746

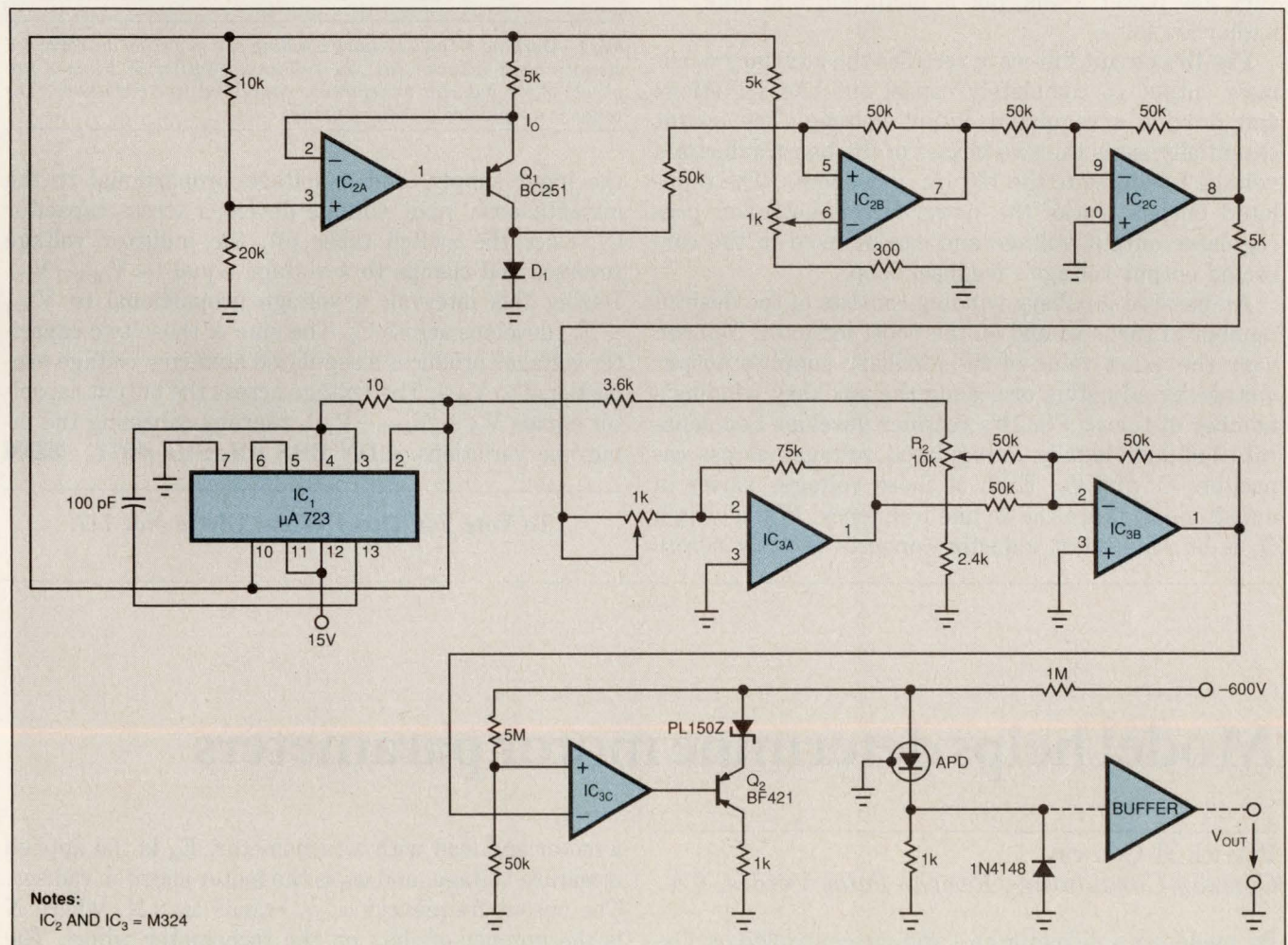


Fig 1—This circuit controls the operating voltage of an avalanche photodiode over a wide range of temperatures by using D_1 as a temperature sensor.

Auxiliary supply tracks power factor

Bill Andreycak
Unitrode Integrated Circuits Corp,
Merrimack, NH

Most power-factor-correction circuits use a boost converter to generate a regulated dc output voltage from the ac line input while forcing the load to draw sinusoidal current, thereby maximizing the power factor. Typically, these circuits use an additional winding on the boost inductor (Fig 1a) to supply power to the control circuit. Unfortunately, the voltage across the inductor varies with the line voltage during both the charging and discharging period. A crude arrangement that uses a limiting resistor to feed a storage capacitor in parallel with a zener diode works well enough at very low power levels, but is inefficient and bulky at higher levels.

Fig 1b's circuit full-wave rectifies the auxiliary winding's output to completely cancel out line variations and provide a regulated output voltage. The circuit essentially sums the two phases of the boost inductor's voltage to eliminate the 120-Hz components. The regulated output tracks the power-factor-controlled pre-regulator output voltage and can be used in the corrected output voltage's feedback loop.

An isolated auxiliary winding consists of the desired number of turns wound on the boost inductor. You can vary the exact value of the auxiliary supply's output voltage by adjusting or scaling the auxiliary winding's number of turns. Fig 1b's rectifier develops two separate but individually unregulated voltages across capacitors C_1 and C_2 . Each of these voltages varies in amplitude at twice the ac line frequency. When switch Q_1 is on, the boost inductor connects directly across

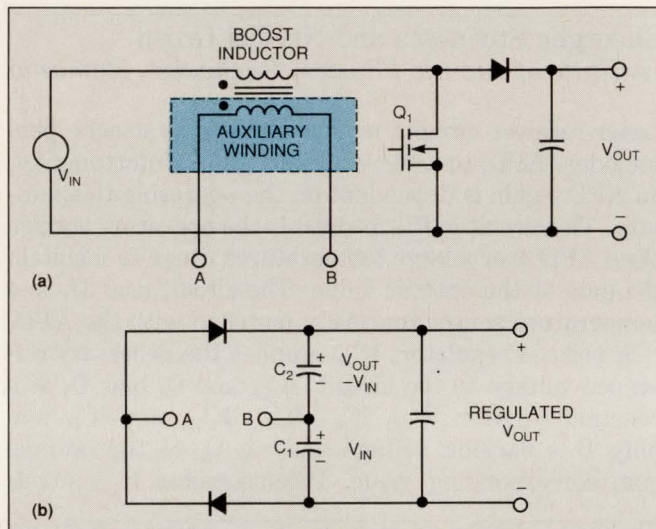


Fig 1—Working off an auxiliary winding of a power-factor-corrected circuit's boost inductor (a), the full-wave rectifier in b sums two phases of the inductor waveform to cancel out line variations. The result is a regulated auxiliary output.

the input supply, and a voltage proportional to the instantaneous input voltage develops across capacitor C_1 . Once the switch turns off, the inductor voltage reverses and clamps to a voltage equal to $V_{OUT} - V_{IN}$. During this interval, a voltage proportional to $V_{OUT} - V_{IN}$ develops across C_2 . The sum of these two capacitor voltages produces a regulated auxiliary voltage proportional to V_{OUT} . The voltage across the output capacitor equals $V_{IN} + (V_{OUT} - V_{IN})$, thereby canceling the input-line variations. EDN BBS /DL_SIG #971 EDN

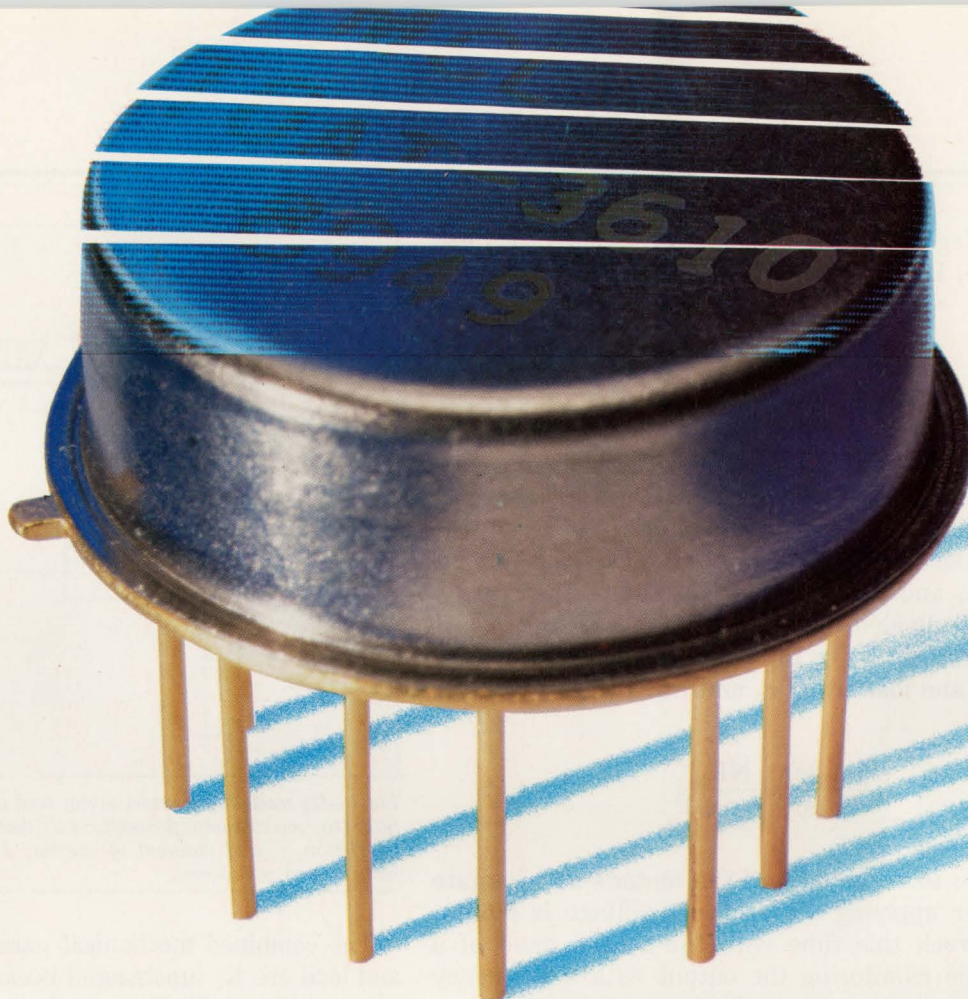
To Vote For This Design, Circle No. 747

Model helps determine motor parameters

Patrick H Conway
Conway Consultants, Rancho Palos Verdes, CA

By modeling a dc motor as a voltage-controlled oscillator, you can determine a servo motor's parameters for your particular load conditions. Fig 1a is a diagram of

a motor and load with a tachometer. E_A is the applied armature voltage, and ω_M is the motor speed in rad/sec. The output frequency, ω_{OUT} , equals $\omega_M \times N$, where N is the number of slots on the tachometer wheel. The standard motor terms are the torque constant, K_T ; the moment of inertia, J ; and the viscous-friction coefficient,



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1.5	0.32	3.0	0.4	9.0	0.6	15.0	0.6
2.0	0.2	4.0	0.3	10.0	0.3	20.0	0.4
2.5	0.32	5.0	0.5	13.0	0.6	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	30.0	0.7
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DESIGN IDEAS

cient, f . Neglecting the armature resistance, R_A , and inductance, L_A , the motor's transfer function is

$$\frac{\omega_{OUT}(s)}{E_A(s)} = \frac{NK_T f}{J s + 1}$$

Because the steady-state speed is proportional to the applied voltage, and the step response is exponential—one pole in the transfer function—you can use a VCO with a lowpass filter at its input to represent the motor and load (Fig 1b.) Time constant τ_M equals $R \times C$ in seconds, and gain constant K_M equals the steady-state speed divided by E_A in units of rad/sec/V. N is identical to that of Fig 1a. Thus, you can characterize the motor and load using τ_M and K_M . Fig 1b's transfer function is

$$\frac{\omega_{OUT}(s)}{E_A(s)} = \frac{NK_M}{\tau_M s + 1}$$

The time to reach 50% of the motor's steady-state speed after applying a step input voltage is $0.69\tau_M$. You can track this time with the second hand of a watch while monitoring the output with a frequency counter. For a motor speed of 3600 rpm and a tachometer with 400 slots, ω equals 150.8k rad/sec (24 kHz). The coefficients of corresponding terms in the two transfer functions are related as follows: $K_T/f = K_M$ in rad/sec/V, and $J/f = \tau_M$ in seconds.

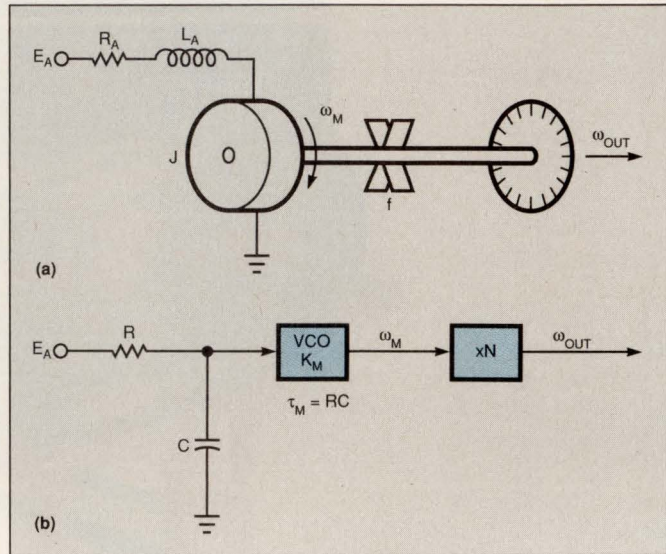


Fig 1—By modeling a servo motor and load (a) as a VCO and RC filter (b), you can solve for coefficients that let you derive a coefficient of friction, f , and moment of inertia, J , that correspond to your motor's load conditions.

The combined mechanical parameters of the motor and load are K_T (unchanged because the load does not influence it), $f = K_T/K_M$, and $J = f \times \tau_M$.

EDN BBS /DI_SIG #973

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To Vote For This Design, Circle No. 748

Spice model aids loop-gain analysis

Henry Yiu

Perkin Elmer Corp, Pomona, CA

To plot the gain-phase relationships of a closed-loop feedback network using Spice, you must break the loop and inject an input signal. When you open the loop, proper dc bias is difficult to maintain because the open-loop dc gain is usually very high. Accounting for the opened loop's input and output impedances is also difficult. For instance, the input capacitance of an op amp could be in a separate library file that is inaccessible to the user. Models that approximate forward- and reverse-loop gain let you maintain the proper dc bias when the loop is open.

Fig 1 shows the general ac model for any 2-port open-loop network. The parameters E , F , R , and Y can be any functions of the complex frequency, S . The correct way to calculate the loop gain is to close the

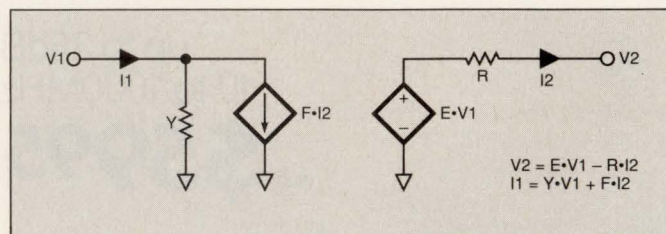


Fig 1—This general ac model for a 2-port open-loop network contains parameters E , F , R , and Y , which can be any function of the complex frequency, S .

loop by making $V1 = V2$ and $I1 = I2$ and then open the loop at the dependent sources.

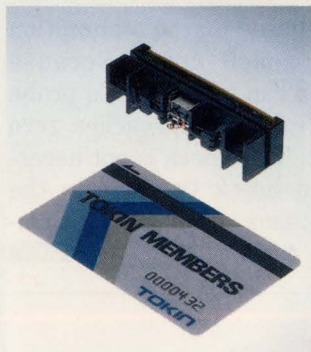
The forward-loop gain, FLG, is the voltage gain from the dependent voltage source around the loop and back:

$$FLG = E \cdot \frac{1-F}{1+RY-F}$$

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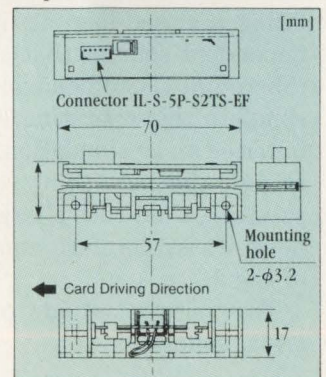
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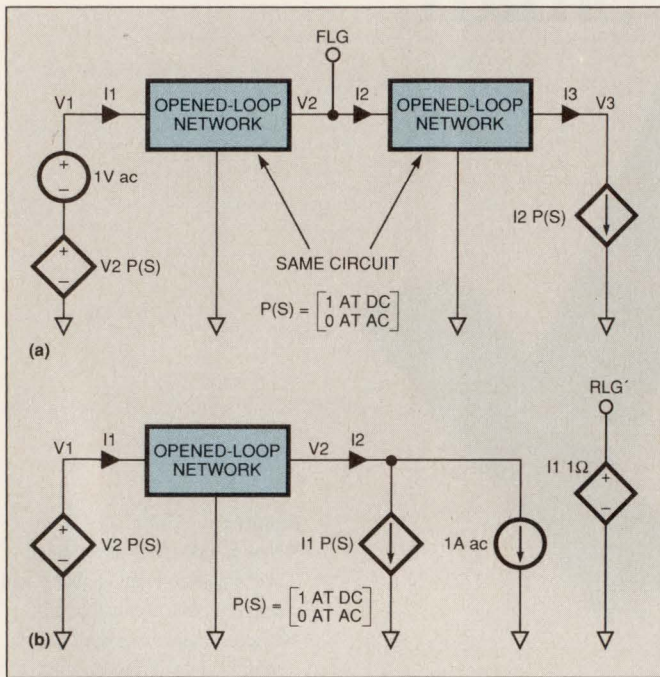


Fig 2—These PSpice models approximate the forward-loop gain, FLG (a), and the reverse-loop gain, RLG (b).

Likewise, the reverse-loop gain, RLG, is the current gain from the dependent current source around the loop and back:

$$RLG = F \cdot \frac{1-E}{1+RY-E}$$

Depending on where you break the loop, E, F, R, and Y vary, but FLG and RLG stay constant.

Fig 2 shows Spice models that approximate FLG and RLG. The models maintain proper dc bias by simulating a closed-loop dc operating condition and using dependent sources that are active only at dc. PSpice's (MicroSim Corp) behavioral modeling features let you simulate this operating condition. When the program initiates an ac simulation, all circuit elements linearize around the bias point so that the output will never saturate, even with a large loop gain. The ac open-loop network is therefore equivalent to the general model of Fig 1.

The voltage outputs of the FLG and RLG models are as follows:

$$FLG' = E \cdot \frac{1}{1+RY}$$

$$RLG' = F.$$

Listing 1 (which you can also obtain from the EDN BBS's DI Special Interest Group (617-558-4241,300/1200/2400,8,N,1—from main menu, enter (s)ig,

Listing 1—PSpice models for loop-gain analysis

```
* LOOP GAIN TESTING MODEL
*
.AC DEC 10 0.1 100K
.PRINT AC V([FLG]) VP([FLG])
.PRINT AC V([RLG]) VP([RLG])
.PROBE
XF      [FLG]  FLG
XR      [RLG]  RLG
*
.SUBCKT FLG      [FLG]      ; Forward Loop-gain Testing Model
VIN     19      0          AC      1.0
RS9     19      0          1000G
EBIAS   11      0          FREQ {V(2)} = (0,0,0) (1E-50,-1E4,0)
EHP     12      11         FREQ {V(19)} = (0,-1E4,0) (1E-50,0,0)
RS1     12      0          1000G
VM1     12      1          DC      0
X1      11      2          OLN
VM2     2       [FLG]     DC      0
X2      [FLG]  3          OLN
VM3     3       13         DC      0
GBIAS   13      0          FREQ {I(VM2)} = (0,0,0) (1E-50,-1E4,0)
.ENDS   FLG
*
.SUBCKT RLG      [RLG]     ; Reverse Loop-gain Testing Model
VIN     19      0          AC      1.0
RS9     19      0          1000G
EBIAS   11      0          FREQ {V(2)} = (0,0,0) (1E-50,-1E4,0)
RS1     11      0          1000G
VM1     11      1          DC      0
X1      11      2          OLN
VM2     2       12         DC      0
GBIAS   12      0          FREQ {I(VM1)} = (0,0,0) (1E-50,-1E4,0)
GHP     12      0          FREQ {V(19)} = (0,-1E4,0) (1E-50,0,0)
HOUT    [RLG]  0          VM1   1.0
RS2     [RLG]  0          1000G
.ENDS   RLG
*
* Opened-Loop Network (OLN) to be tested for loop-gain
.SUBCKT OLN      1       2       ; 1 = loop input, 2 = loop output
VDC     5       0          DC      2.0
RY      1       5          IMEG
F       1       5          VMO    0.001
E       3       5          1       5          -1000.0
R       3       4          10K
VMO     4       2          DC      0
.ENDS   OLN
*
.END
```

(</di_sig>, rk972)) contains the PSpice code for these models. To use the models, make the open-loop network under test into a subcircuit named OLN, which you then run as a PSpice model. If $|RLG'| = |F| \ll 1$, then FLG' closely approximates the loop-gain term, FLG. Otherwise, break the loop at a different point and run the analysis again.

Note that these models are based on the assumption that $|1+RY|$ does not approach zero. Because $1+RY = V3/V2^2$ in Fig 2a, you can use PSpice's probe feature to verify that $|1+RY|$ never approaches zero over all frequencies of interest. This check is not necessary unless, for example, you break the loop in the middle of a tuned LC network or a resonant transmission line. EDN BBS /DI_SIG #972 **EDN**

Reference

1. Caldwell, David J, "Minimize loading errors in loop-gain measurements," EDN, May 24, 1990, pg 165.

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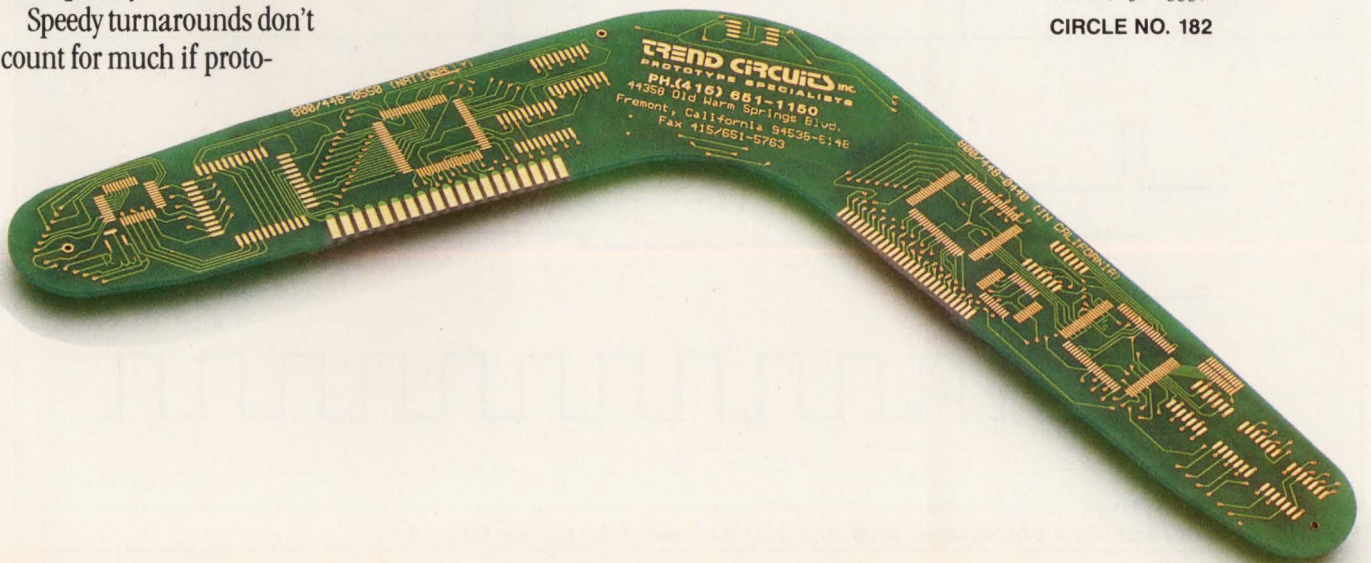
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CIRCLE NO. 182



Low-battery detector polls threshold

Yongping Xia

Department of Electrical and Computer Engineering, West Virginia University, Morgantown, WV

The battery low-voltage detector in Fig 1 uses a CD4093 Schmitt trigger, a capacitor that acts as a 1-bit dynamic RAM. The circuit conserves power by using a periodic test method. IC_{1A}, C₁, R₁, R₂, and D₁ generate a narrow, positive pulse at point A. The duty cycle of this pulsed signal depends on the ratio between R₁ and R₂. When the signal at A is high, the voltage at this point almost equals that of the power supply because IC_{1A} is a CMOS device.

D₂, R₄, and R₅ regulate and divide the signal at A. Thus, the input of IC_{1B} is independent of the power supply. Because the threshold voltage of the Schmitt

trigger depends on the power supply, the threshold voltage will drop if the power-supply voltage drops. When the threshold voltage is lower than the input voltage, IC_{1B} will go low, and IC_{1C}'s output will go high. Otherwise, IC_{1C} will always be low.

Capacitor C₂ stores the results of the periodic test. The time constant C₂ and R₆ set is 1 sec, and the test period is approximately 0.1 sec, so point B holds the test result between successive tests. When point B is high, which implies that the battery is low, IC_{1D}, C₃, and R₇ generate a square waveform, which lights D₃. You can adjust the detected voltage level by adjusting R₄. You can test different battery voltages by changing the voltage level of D₂. EDN BBS /DL_SIG #975 EDN

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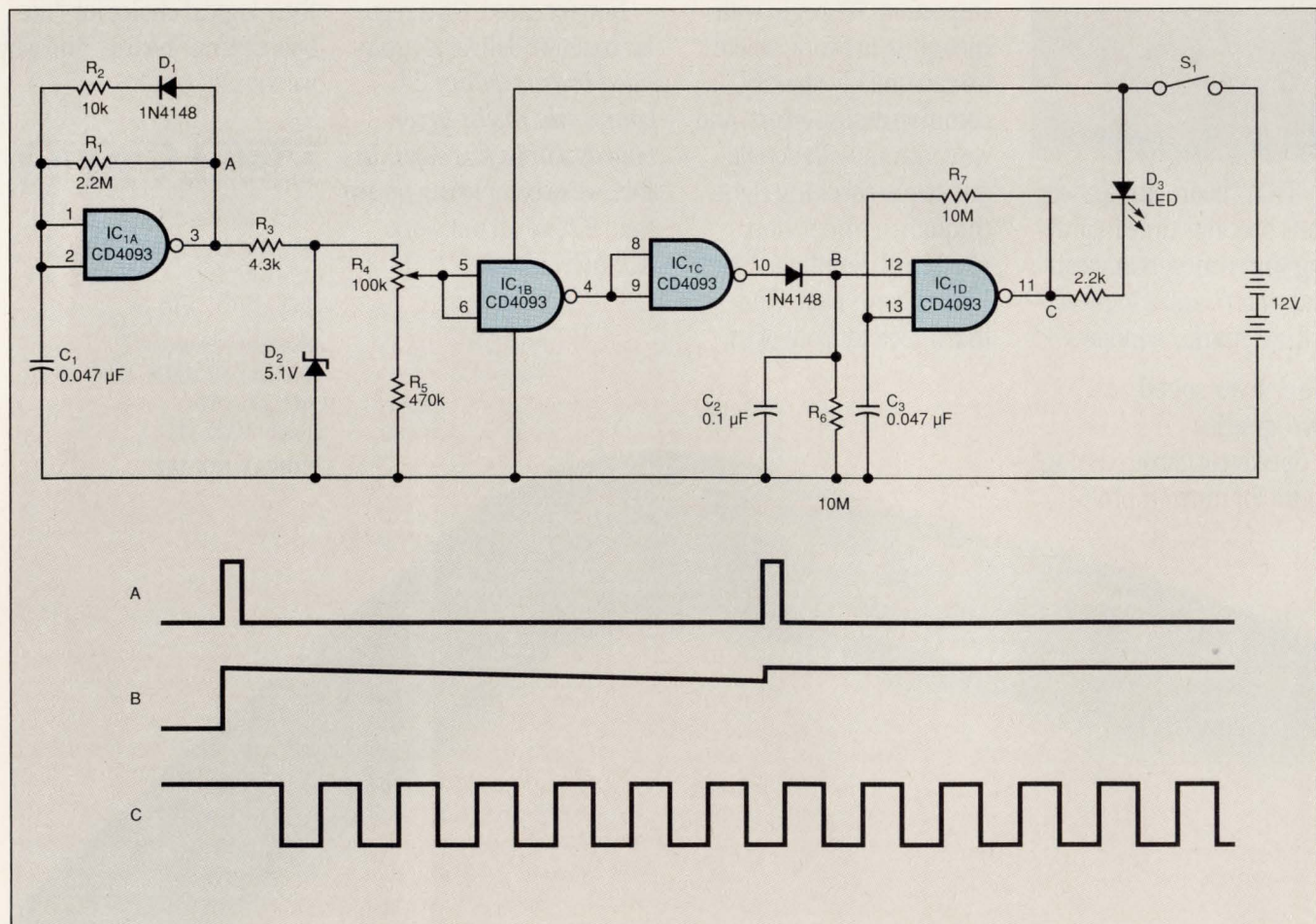
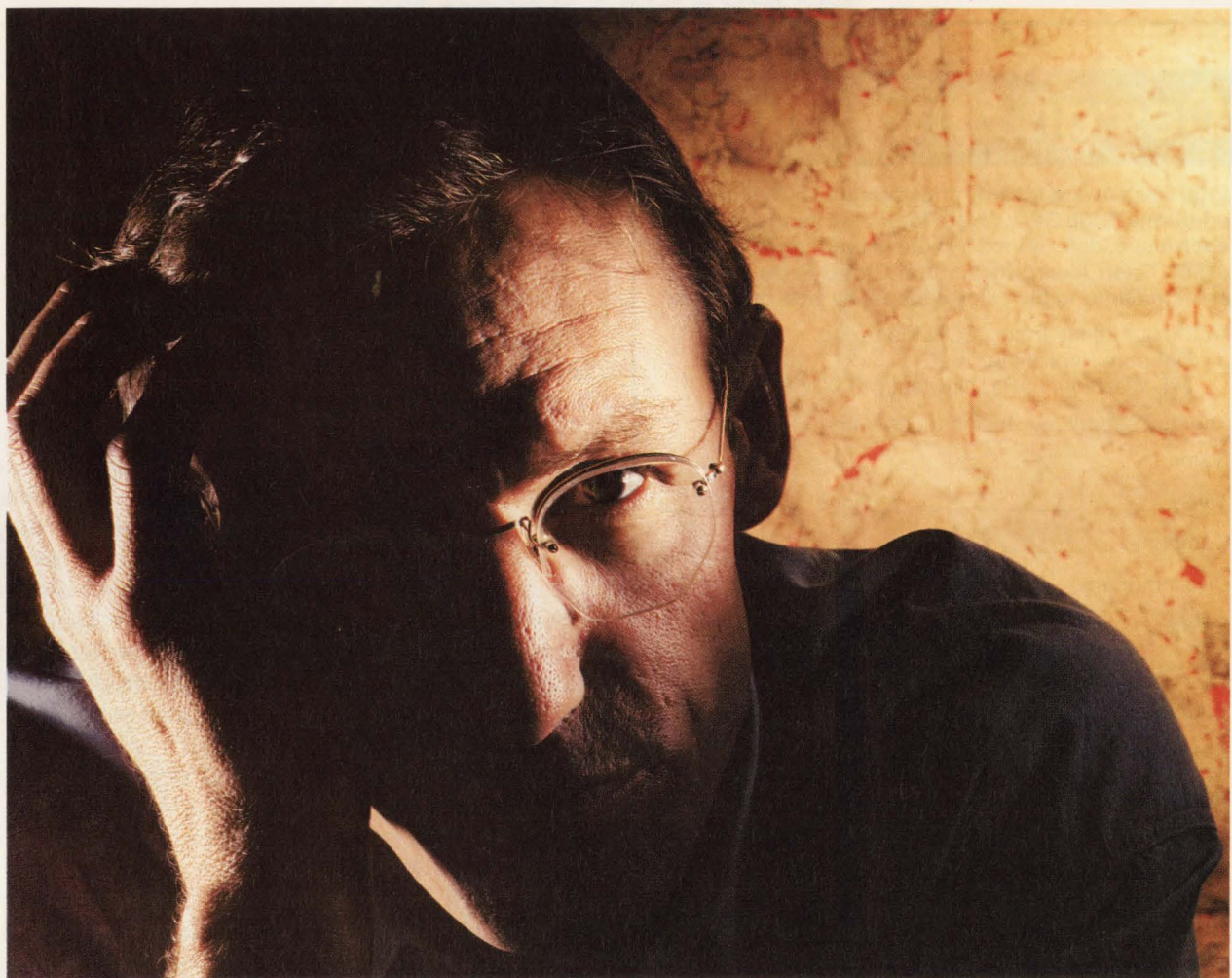


Fig 1—Capacitor C₂ acts like a 1-bit dynamic RAM by storing the result of this periodic battery tester.



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ISSUE WINNER

The winning Design Idea for the March 14, 1991 issue is entitled "One coax cable carries video and power," submitted by Jeff Kirsten and Charlie Allen of Maxim Integrated Products (Sunnyvale, CA).

The winning Design Idea for the March 28, 1991 issue is entitled "Pulse generator wrings out scopes," submitted by Jim Williams of Linear Technology Corp (Milpitas, CA).

FEEDBACK AND AMPLIFICATION

Suggestion invokes tradeoffs

Thanks to Larry K Baxter for his comments on the Design Idea "S/H circuit multiplexes op amp" in EDN's Feedback and Amplification column of February 18, 1991. He suggests moving R_1 outside the feedback loop to ensure stability in the op amp (although EDN published his wording as "... should be inside the feedback loop...") However, stability wasn't an issue for the op amp tested, an old 8007 from Intersil. Placing the resistor as Mr Baxter recommends eliminates a potentially destabilizing phase shift but lengthens the acquisition time by increasing the capacitor-charging resistance. Readers who use other op amps may want to consider this tradeoff of stability vs acquisition time.

As to the left-hand analog switch, we haven't converged on a clarification because that switch is drawn differently in all four schematics: the original author's (a Maxim employee) version, my edited version, EDN's published version (which doesn't work), and Mr Baxter's version. The pole of that switch must connect to the op amp. It connects to V_{IN} in EDN's October 1, 1990, original version, which disconnects the op amp in hold mode. Mr Baxter's switch doesn't identify the pole, though he may not have drawn it that way. In any case, we all agree that analog switches exhibit less leakage and capacitance on switched nodes than on the common node.

Engineers and magazine art departments could reduce such confusion by adhering to standard IEEE or EIA-approved symbols for electronic components.

Tarlton Fleming, Technical Editor

Maxim Integrated Products

120 San Gabriel Dr

Sunnyvale, CA 94086

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Schematic Corrections

Please note two schematic errors that crept into the March 14, 1991, Design Idea "One coax cable carries video and power" by Jeff Kirsten and Charlie Allen. In Fig 2, Q_2 should be a 2N3904, not a 2N3906. In Fig 3, the ground symbol at IC_2 should be a triangle to indicate a power-supply ground.

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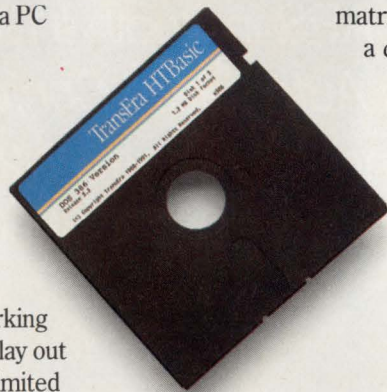
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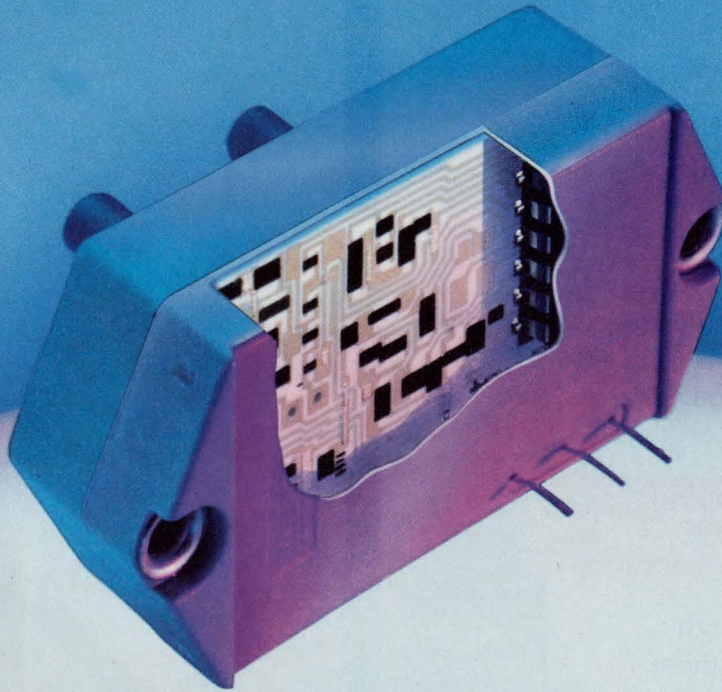


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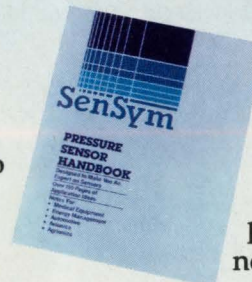
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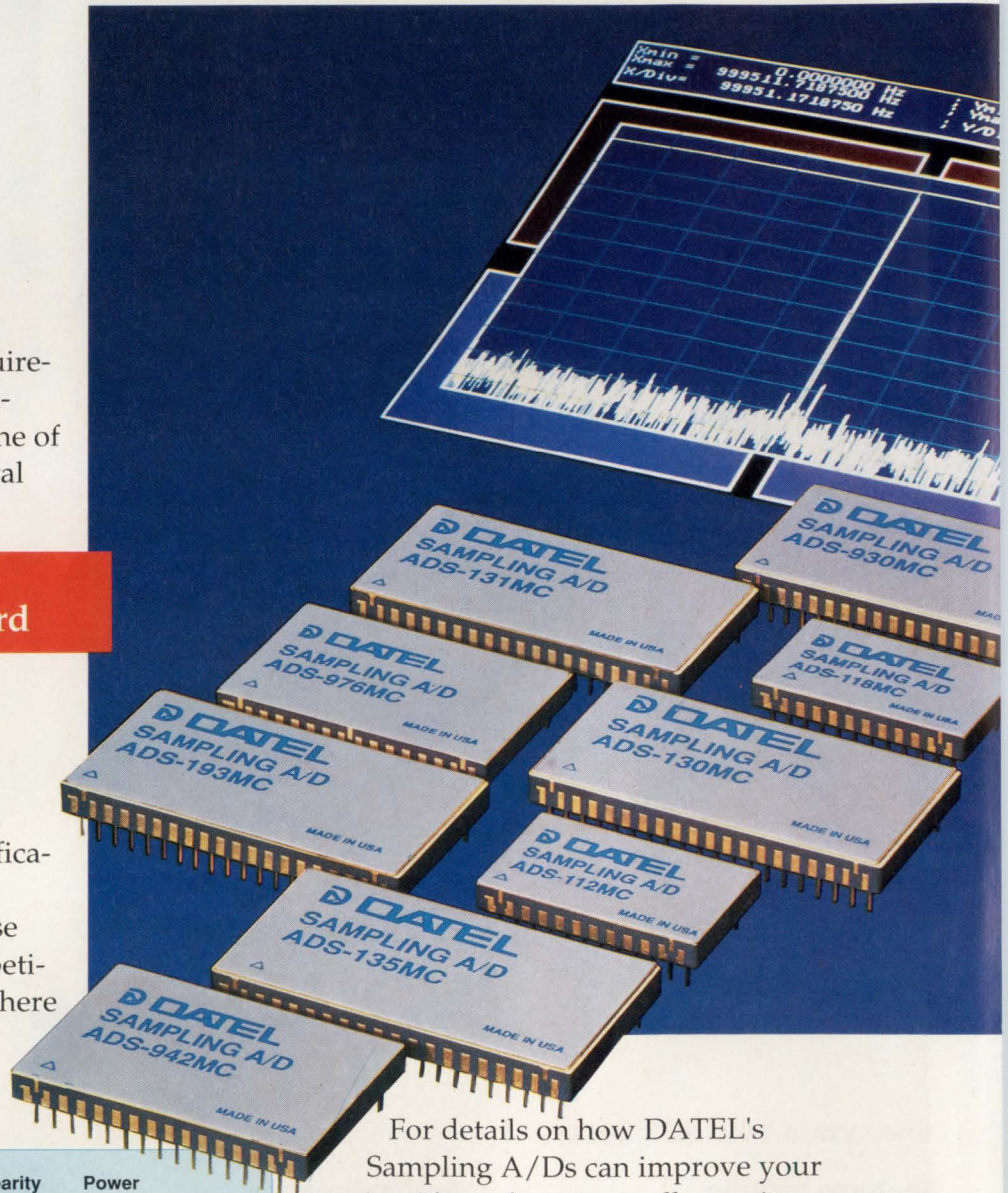
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ADS-132	12	2.0	±1/2	2.9	32-PIN
ADS-118	12	5.0	±3/4	2.3	24-PIN
ADS-131	12	5.0	±3/4	3.8	40-PIN
ADS-130	12	10.0	±3/4	4.0	40-PIN
ADS-924	14	0.300	±1	1.3	24-PIN
ADS-928	14	0.500	±1/2	2.9	32-PIN
ADS-941	14	1.0	±3/4	3.1	32-PIN
ADS-942	14	2.0	±3/4	3.2	32-PIN
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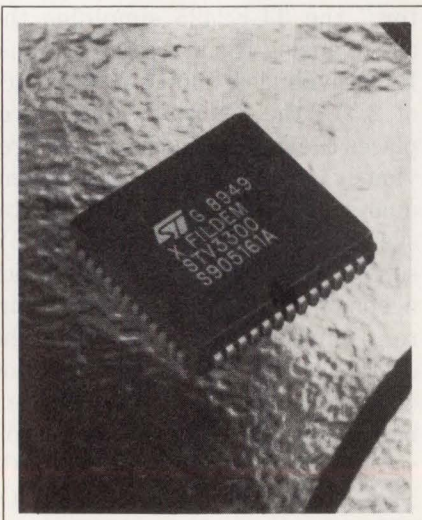
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verse-battery protection, a feature that prevents the regulator from acting as a short circuit when the battery terminals are reversed. The LP2952 is available in 14-pin DIPs and 16-pin SO packages. The LP2963 is available in 16-pin DIP

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National Semiconductor, Box 58090, Santa Clara, CA 95052. Phone (408) 721-7509. TWX 910-339-9240. **Circle No. 351**



Video Conversion Chip

- Meets CCIR 601 standard
- Converts signals from YUV to RGB

Designed for use in the video-restitution stage of a digital image-processing system, the STV3300

chip converts YUV (luminance/chrominance) signals to RGB (red, green, blue) signals in accordance with CCIR 601 recommendations. A filter block provides 2 \times oversampling, which helps to eliminate noisy signals in digital receiver applications. Four selectable filters are available for chrominance signals, and one fixed filter is available for the luminance signal. Input data is in the 4:2:2 format defined by CCIR 601 and is fed through two 8-bit buses at 13.5 MHz max for the luminance and 6.75 MHz for the chrominance samples. RGB output data is on three 8-bit buses at 27 MHz max. The STV3300 comes in a 52-pin plastic leaded chip carrier. \$18.20 (1000).

SGS-Thomson, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. FAX (602) 867-6290.

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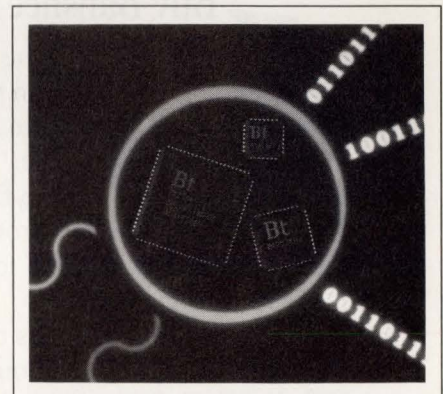


Image Digitizers

- Accelerate video-capture rate
- Provide high-resolution output

Featuring video-capture rates to 30M samples/sec, a trio of image digitizers can digitize NTSC video signals at 8 times the subcarrier frequency. This capability simplifies the design requirements of antialiasing filters. The three parts are the Bt218 8-bit flash converter, the

INTEGRATED CIRCUITS

Bt252 single-channel image digitizer, and the Bt254 3-channel image digitizer with color output format. The Bt218 contains 256 high-speed parallel comparators to digitize analog-input signals. An input range of 0.714 to 1.2V allows direct digitization of NTSC and CCIR video signals. The Bt252 for

monochrome video signals contains an 8-bit flash A/D converter that supports four analog video outputs. A 256 × 8-bit RAM look-up table enables real-time image manipulation prior to data storage. The Bt254 contains three 8-bit video A/D converters, supports two separate 3-channel video-output ports, and

generates 8, 15, or 24 bits of color information for each pixel. The Bt218 is available in a 24-pin DIP or a 28-pin plastic leaded chip carrier (PLCC); the Bt252 and Bt254 come in 44-pin PLCCs. Bt218, \$10; Bt252, \$33; Bt254, \$40 (100).

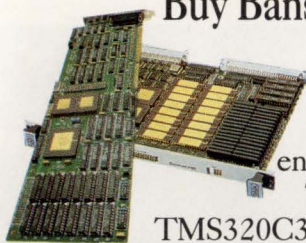
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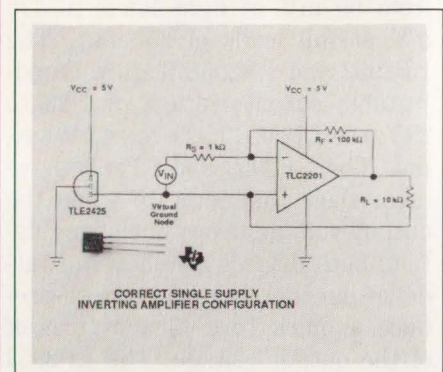
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Text continued on pg 188

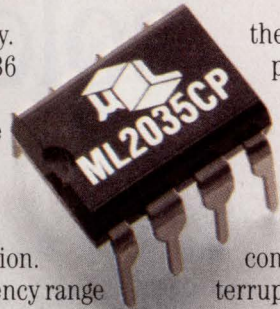
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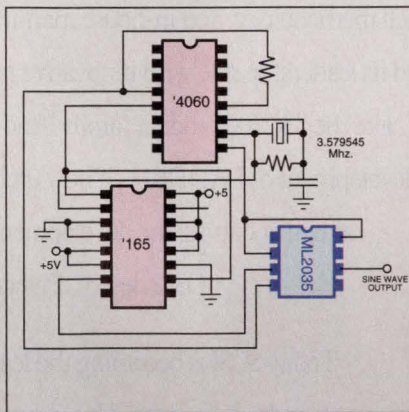


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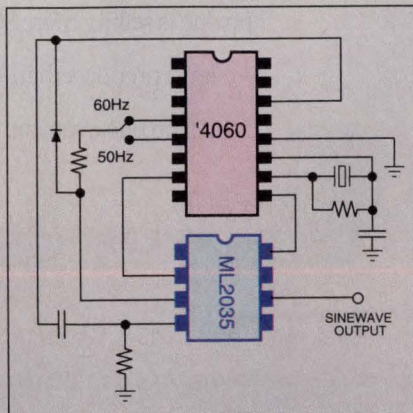
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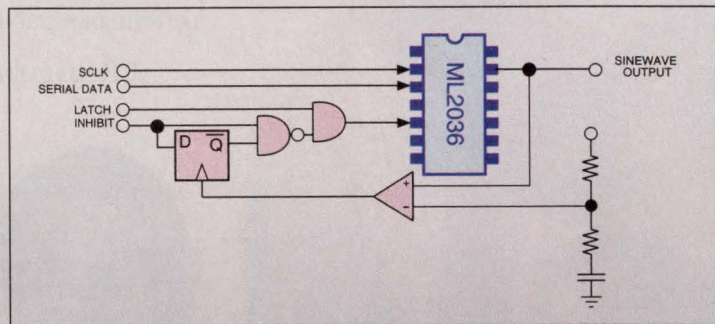
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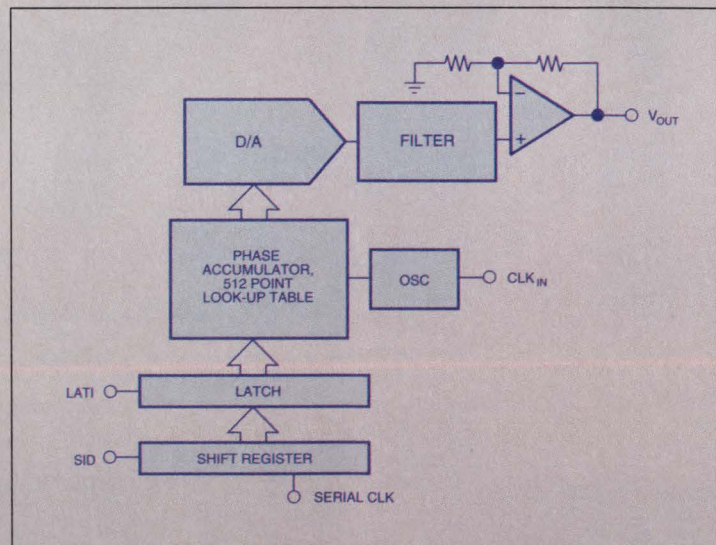
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ML2035 Block Diagram

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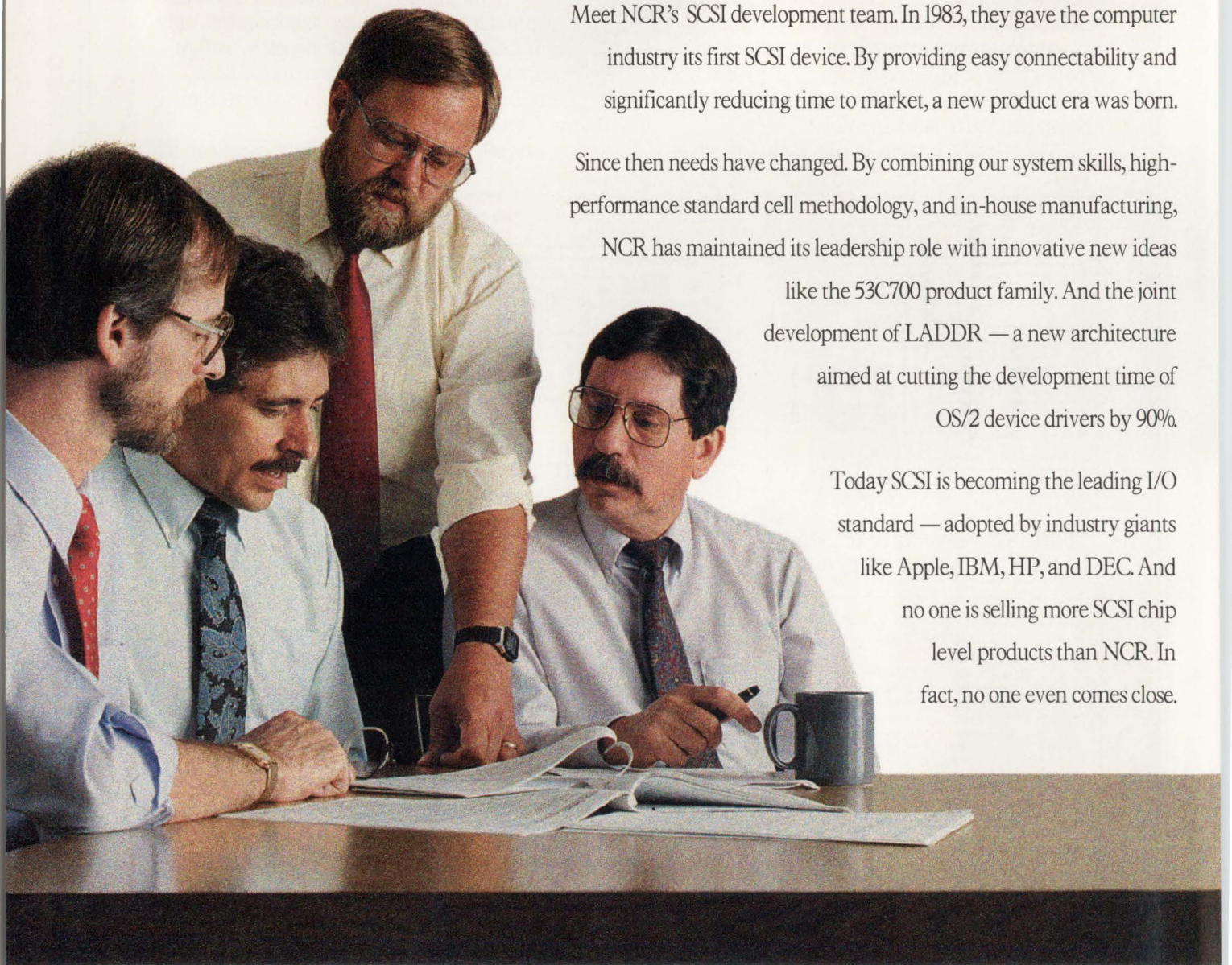
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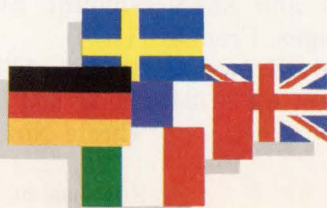
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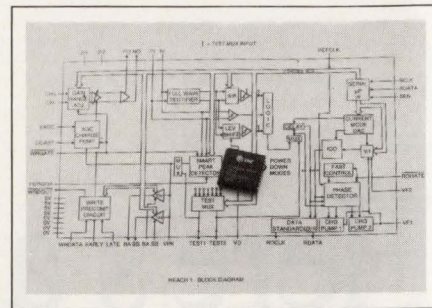
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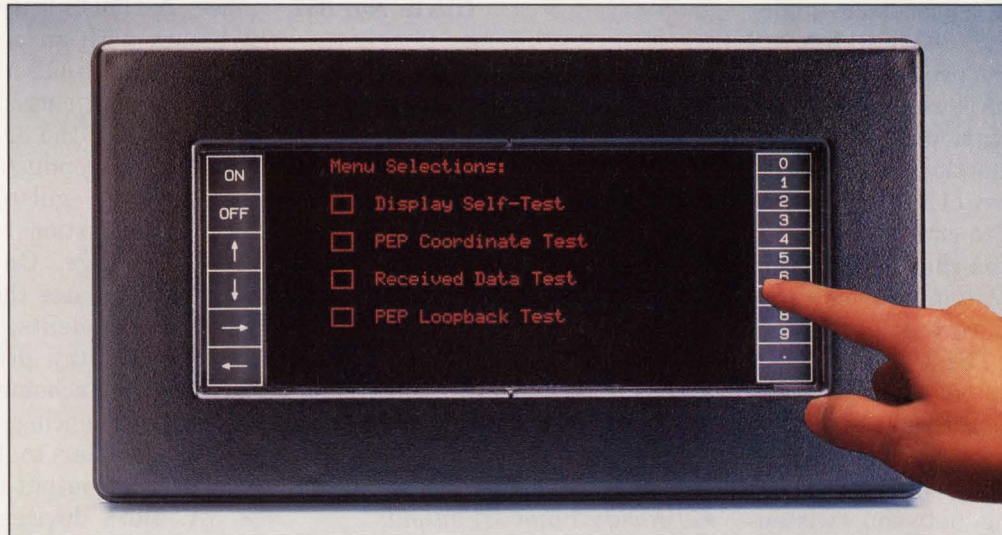
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- Compact flat panel is only 3" deep—fits where CRTs can't
- Battery backed canned message RAM reduces host memory overhead

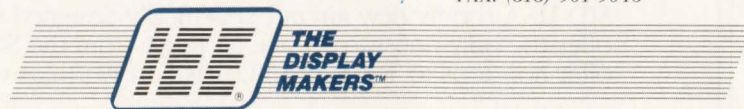
Display Features

- 240×120 accessible dots form a 12 line by 40 character display, using a nominal 5×7 dot matrix character
- 96-character U.S. ASCII character set in regular height-width, double height, double width, double height-width; all in regular and reverse video
- 96-character ISA Graphics character set
- 14.10×7.85×3.00" (W×H×D)

Operation

- Requires only +5.0VDC TTL supply and an unregulated 11-29VDC panel supply
- Serial I/O RS-232-C (with CTS and DTR) and RS-422 interfaces at 1200 or 9600 baud
- ANSI-standard VT100 compatible control codes

*Industrial Electronic Engineers, Inc.
Industrial Products Division
7740 Lemona Avenue
Van Nuys, CA 91409-9234
Tel.: (818) 787-0311, ext. 418
FAX: (818) 901-9046*



Circle No. 3 For Immediate Response

Circle No. 4 For Future Reference

10 Base-T Transceiver

- Implements IEEE-802.3 standard
- Includes polarity detection

The NE86C92 transceiver implements the IEEE-802.3 10 Base-T standard, which specifies a 10M-bit/sec Ethernet LAN using unshielded twisted-pair wiring. Among the transceiver's functions are polarity detection/correction, a smart squelch circuit, a crystal-controlled oscillator, and on-chip LED drivers for status indication (transmit, receive, polarity reversal, collision, and jabbing). The transceiver allows automatic selection between the 10 Base-T transceiver and the AUI (attachment unit interface). The AUI lets you change jumpers when switching between twisted-pair wiring and a remote medium-access unit, without removing the interface card. The transceiver has a typical current drain of 20 mA

without traffic and 65 mA with heavy traffic. \$12 (100).

Signetics, Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000.

Circle No. 357



Three-Phase Motor Drivers

- For 12V disk-drive spindle motors
- Provide 3 and 4A outputs

The A8922 and A8925 motor drivers provide control and drive for 3-phase brushless dc motors in cartridge-tape and hard-disk drives,

respectively. The 8925, which drives 12V spindle motors, has an output-current rating of 4A to accommodate faster up-to-speed times. A DMOS sense-FET output structure with an on-resistance of just 0.25Ω extends the head room at high output currents. To control spindle speed, the 8925 employs an on-chip transconductance amplifier that linearly regulates output current in proportion to an external control voltage. On-chip current sensing eliminates the need for external components, and internal control circuitry provides brake, disable, and tachometer functions, and the sequencing of the output drivers. Similar to the 8925, the 8922 has an output-current rating of 3A. Both devices accept Hall-effect inputs for motor commutation. The 8925 and the 8922 come in 44-lead and 28-pin plastic leaded chip carriers, respectively. 8925

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INTEGRATED CIRCUITS

unit, \$8; 8922 unit, \$7.50 (1000).

Allegro Microsystems, Box 15036, Worcester, MA 01615. Phone (508) 853-5000. FAX (508) 853-5049. **Circle No. 358**

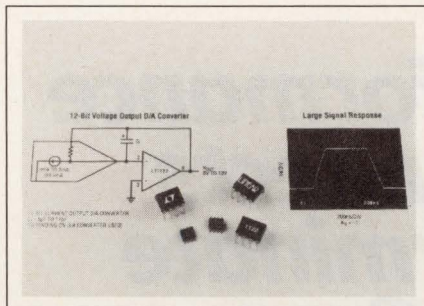
Variable Gain Block

- Gain-control range is 50 dB
- Small-signal bandwidth is 200 MHz

Used as an analog building block, the EL2082 2-quadrant multiplier provides 50 dB of variable gain control. The device operates in current mode rather than voltage mode, thus reducing input impedance and increasing output impedance. Targeted at high-frequency applications, the device features a small-signal bandwidth of 200 MHz and a large-signal bandwidth of 150 MHz. The device operates from ± 5 to ± 15 V supplies. When used with an external op amp, the multiplier's

differential gain is 0.05%, and differential phase is 0.025° . In the disable mode, the device has 80 dB of isolation at 10 MHz. The EL2082 is available in 8-pin DIPs and SOIC packages. \$5.95 (100).

Elantec Inc, 1996 Tarob Ct, Milpitas, CA 95036. Phone (408) 945-1323. **Circle No. 359**



Fast-Settling Op Amp

- Settles to 1 mV in 340 nsec
- Slew rate is 80V/ μ sec

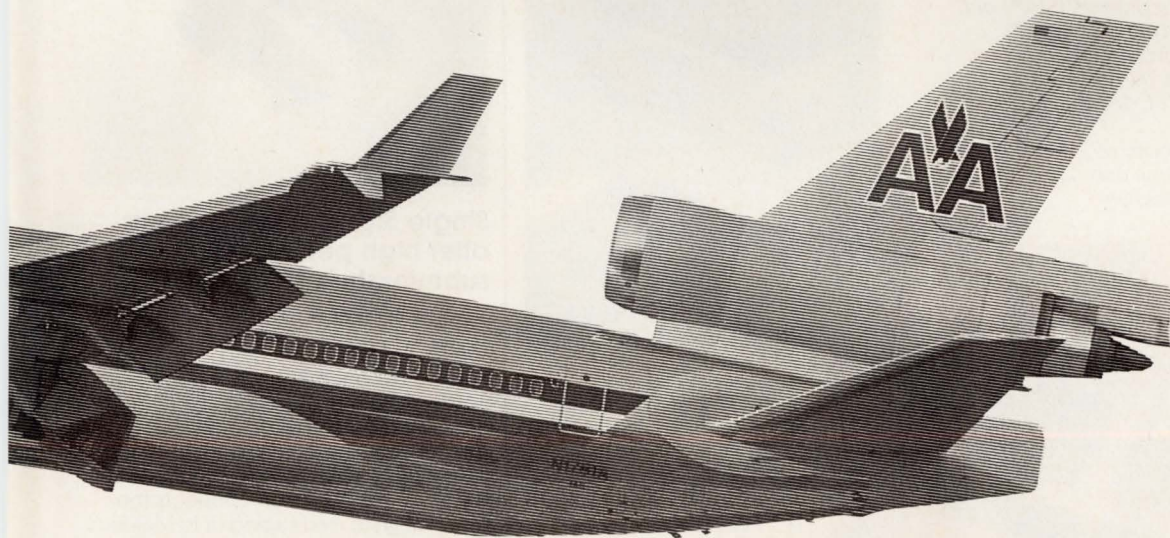
The LT1122 op amp features a typi-

cal settling time of 340 nsec and a guaranteed maximum settling time of 540 nsec, 100% tested to 1 mV at the sum node with a 10V input step. The op amp also features a typical slew rate of 80V/ μ sec (60V/ μ sec min). Internally compensated for unity-gain stability, the op amp has a small-signal bandwidth of 14 MHz and a large-signal (20V p-p) bandwidth of 1.2 MHz. Total harmonic distortion is only 0.001%. The JFET input op amp also features high precision. Input offset voltage is 600 μ V, input-bias current is 75 pA, and input-offset current is 40 pA, all 100%-tested maximum values. The op amp is available in 8-pin SO packages, and in plastic and hermetic DIPs. \$2.50 (100).

Linear Technology, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (800) 637-5545; in CA, (408) 432-1900. FAX (408) 434-0507.

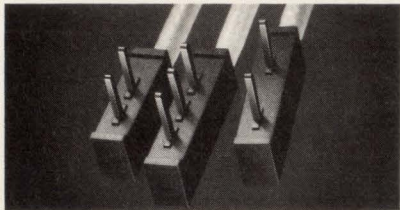
Circle No. 360

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award-winning International Flagship Service®. In fact, the only change you'll see is in the plane we're flying. ♦ We invite you to experience the MD-11 for yourself. For information or reservations, call your Travel Agent or American Airlines at 1-800-624-6262.

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Low Profile PCB Solderable Interconnects

- Solders to the PC Board
- Impedance matched

Meritec's low profile, impedance matched PCB Solderable Interconnects

solder directly to the PC Board for a permanent connection. Pin lengths of .110" and .160" are available for different board thicknesses. The connectors feature precision, high strength molded terminations for reliability in critical applications. Available in 1x2 and 1x3 configurations, the connectors are side-to-side stackable and feature heights as low as .150" from the PC Board, making them ideal for dense package applications. Meritec PCB Solderable Interconnects can be terminated to a variety of different cable types.

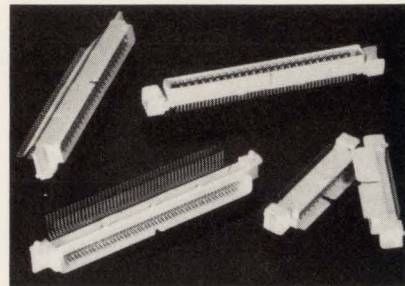
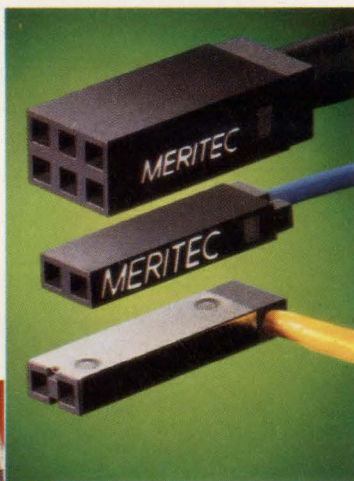
Circle No. 168

High-Performance Interconnects That Terminate High Cost.

Meritec has terminated the high cost of high performance interconnects for fast logic applications. We produce a full line of cable assemblies for applications in the 3ns to sub nanosecond range—engineered to match your requirements for controlled impedance and propagation rate while minimizing crosstalk. We deliver assemblies of unparalleled quality. On time. At a very reasonable price.

Our complete line includes Single Signal Interconnects (SSI™), Shielded Performance Interconnects (SPI™) and Multi Signal Interconnects (MSI™), terminated to a diversity of controlled impedance cables, including coax, twin coax, FEP, PTFE and our Flatex™ textile cable.

Call Meritec today at 216-354-3148 for more information and a free copy of our capabilities brochure.

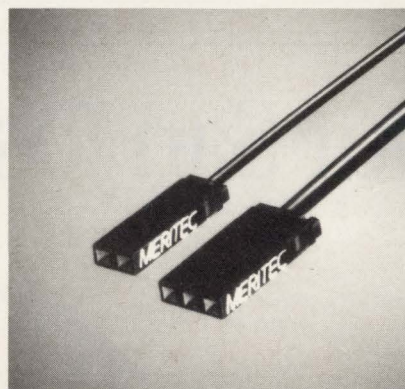


.050" Pitch Hermaphroditic Connectors eliminate the need for separate male and female parts

- Feature .050" centers
- 50Ω impedance matched

Meritec introduces a new concept in board-to-board interconnects – CP50™ Hermaphroditic Connectors. Each mating half is identical in configuration, eliminating the need for separate male and female parts. Close pitch .050" centers minimize board space requirements. The 50Ω impedance matched connectors feature precision, high strength molded terminations for reliability in critical applications and are designed to meet IR or vapor phase reflow requirements. Contact tails come in SMT and through hole configurations, straight and right angle.

Circle No. 168

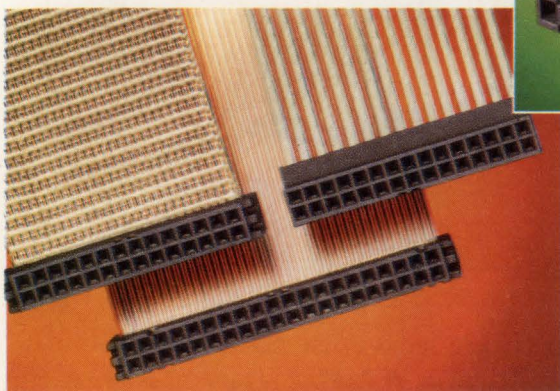


Single Signal Interconnects offer high performance in a subminiature package

- Controlled impedance
- Low crosstalk

Meritec's economical 1x2 and 1x3 Single Signal Interconnects (SSI™) are engineered to match application requirements for controlled impedance and propagation rate while minimizing crosstalk. A spring latch connects the termination to the housing or to Meritec's Single Signal Carrier Systems (SSC™), which allow group interfacing with single, dual or triple row headers. Precision, high strength molded terminations provide reliability in critical applications. Boxed contacts with thermo resistance welding provides the ultimate in electrical continuity.

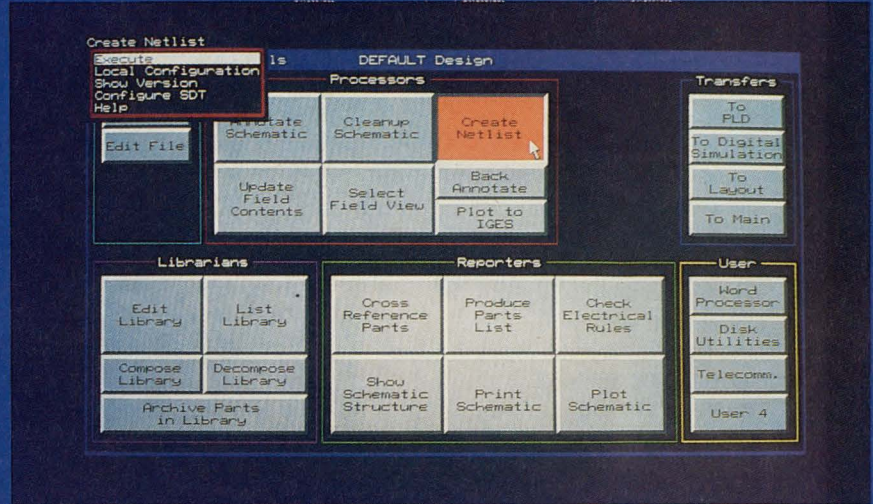
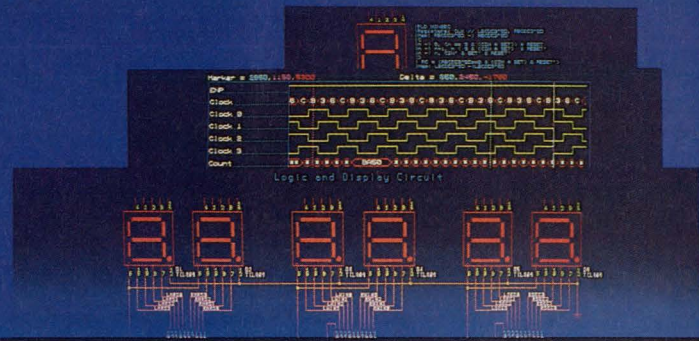
Circle No. 168



1359 West Jackson Street
P.O. Box 8003
Painesville, Ohio 44077
216-354-3148
FAX: 216-354-0509

CIRCLE NO. 168

OrCAD presents Release IV



The limits are gone

OrCAD has introduced the greatest product upgrade in its history. Memory limits, design restrictions, even boundaries between products are all disappearing.

For years, OrCAD's competitors have been playing a game of catch-up. With the introduction of Release IV, the race is over. No one will match our price/performance ratio on these features:

- Schematic Parts Library has been increased to over 20,000 unique library parts
- Digital Simulation process has been speeded up by an order of magnitude
- Printed Circuit Board Layout package offers autoplacement and autorouting at no extra charge
- Expanded memory capabilities

Best of all, OrCAD introduces ESP

ESP is a graphical environment designed specifically for the electronic designer. Software tools appropriate for different stages in the design process are now linked together to form a seamless flow of information. This easy-to-use framework relieves the designer of time consuming tasks and the inconvenience of moving from one tool set to another. You can now spend more time productively designing.

For more information . . .

You need to know more about Release IV and all of the benefits OrCAD has to offer. Call the telephone number below and we'll send you a free demonstration disk.



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For more information, call (503) 690-9881

or write to OrCAD Sales Department, 3175 N.W. Alcock Drive, Hillsboro, Oregon, 97124

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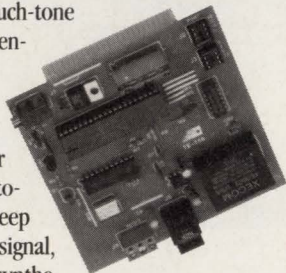
Data Acquisition & Control

NEW

TE-158 Telephone Control Card:

Take total control over your telephone communication. Direct telephone line interface gives you control over line connect/disconnect, touch-tone decoding and encoding, and detects call progress. Set your computer to dial out automatically, to keep trying if busy signal, control voice synthesizer, tape recorder with complete in/out capability. FCC approved.

TE-158: \$190.00



Relay Card:

8 individually controlled industrial relays. 3A at 120VAC, SPST.

RE-140: \$142

8 Bit A to D:

8 Analog inputs. 0-5.1V. 20mV steps. 7500 readings/sec.

AD-142: \$142

Temperature Sensor:

Range 0-200°F. 10mV/°. 2° Resolution with AD-142.

TS-111: \$12

Digital Input:

8 opto-isolated inputs. Read voltage presence or switch closures.

IN-141: \$65

Latched Digital Input:

8 opto-isolated inputs. Each input individually latched to catch switch closures and alarm loops.

LI-157: \$85

Smart Quad Stepper Controller:

On board micro-processor controls four motors simultaneously. Uses simple commands like "MOVE ARM 10.2 (INCHES) LEFT". Set position, ramping, speed, units... Many inputs for limit switches etc. Stepper motors available.

SC-149: \$299

Odin Software:

PC compatible. Control relays from analog inputs or time schedules. Logging. Runs in background.

OS-189: \$129

Reed Relay Card:

8 reed relays (20mA at 60VDC, SPST).

RE-156: \$109

Digital Output Driver:

8 outputs: 250mA at 12V. For relays, solenoids, stepper motors, lamps.

ST-143: \$78



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Touch Tone Decoder:

Converts tones to unique values.

PH-145: \$87

A-Bus Prototyping card:

PR-152: \$16

Motherboard:

Holds up to 5 A-Bus cards. **MB-120: \$108**

Counter Timer:

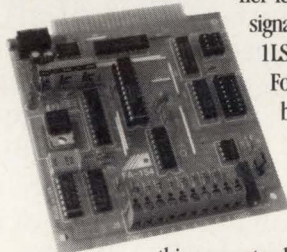
Three 16 bit counters/timers. Count pulses, measure frequency.

CT-150: \$132

NEW

FA-154 High Speed 12 Bit A/D Converter:

Blinding speed at low cost! Convert at 10 μ s. Eight input channels accepting 0-5V signals. Special onboard variable gain amplifier lets you read signals less than 1LSB (1.2mV).



For value combined with speed in data acquisition and signal processing,

this converter leads the pack!

FA-154: \$179.00

12 Bit A to D:

Range: $\pm 4V$. On-board amp. 1mV resolution. Conversion time 130ms. 1 channel; expand with RE-156 or MX-155

AN-146: \$153

32 Channel Multiplexer:

Switches up to 32 channels to a single common.

MX-155: \$83

Clock with Alarm:

Powerful clock/calendar. Battery backup. **CL-144: \$98**

These products work with IBM PC, Apple II, Commodore and Tandy, etc. Our serial interfaces let you use any computer with an RS-232 port.

A-Bus Adapters:

IBM PC/XT/AT & compatibles.

AR-133: \$69

Serial Adapter:

Connect A-Bus systems to any RS-232 port. **SA-129: \$149**

MicroChannel Adapter:

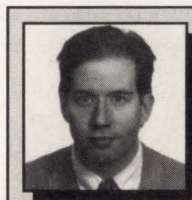
Parallel Adapters also available for Apple II, Commodore 64, 128, TRS-80.

AR-170: \$93

Serial Processor:

Built in BASIC for off-line monitoring, logging, decision making.

SP-127: \$189



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Kevin Tschudi Engineer, Alpha Products

24 line TTL I/O:

Connect 24 signals, TTL 0/5V levels or switches. (8255A)

DG-148: \$72

D/A converter:

4 Channel 8 Bit D/A converter with output amplifiers.

DA-147: \$149

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NEW PRODUCTS

COMPUTERS & PERIPHERALS

Noninterlaced Monitor

- Has a 248 × 186-mm viewing area
- Has a flicker-free refresh rate

The ViewSonic 6 is a true 1024 × 768 noninterlaced 14-in. ultra-VGA color monitor with a 248 × 186-mm display area. A multisynchronous unit, it automatically adjusts to horizontal scanning frequencies of 30 to 50 kHz and vertical frequencies ranging from 50 to 90 Hz. In the 800 × 600 pixel mode, the monitor has a 72-Hz (VESA (Video Electronics Standards Association) standard) flicker-free refresh rate and a 0.28-mm dot pitch. All access controls, including the presetting and auto-sizing functions, are located directly under the screen, making it convenient to switch between different screen modes. Controls include vertical and horizontal sizing, brightness, contrast, and centering. The monitor also has a tilt-and-swivel base. Operating in any IBM or compatible; MAC II; or Sony C1304 environment, the



unit supports graphics standards including ultra-VGA, 8514/A, super-VGA, and VGA. \$699.

Viewsonic, 12130 Mora Dr, Santa Fe Springs, CA 90670. Phone (213) 946-0711. **Circle No. 361**

Data-Storage Units

- Designed for the DSSI bus
- Interface with SCSI peripherals

This family of products is designed for the DSSI bus and offers MicroVAX 3XXX and VAX 4000 users the performance and capacity advantages of SCSI peripheral devices. The family includes three products—the DM/3000 and DM/4000 drive module kits, and the DH01 host adapter. The DM/3000 is designed to be mounted internally in the MicroVAX 3300 and 3400. It consists of a 5¼-in. drive integrated with the company's MD30 bridge controller, mounting hardware, and cables. The DM/4000 is available for the VAX 4000 and includes all the components of the DM/3000 plus an operator's panel. Both kits are available in 700M-, 1200M-, and 1600M-

bit capacities. The DH01 is a Q-bus-to-DSSI host adapter for the MicroVAX, which has no DSSI port. It will function with either of the DM drive kits or with a DEC ISE. DM/3000, \$6795 to \$8895; DM/4000, \$7095 to \$9195; DH01, \$2295 to \$2495.

Emulex Corp., Box 6725, Costa Mesa, CA 92626. Phone (714) 662-5600. **Circle No. 362**

Laptop Modem

- Designed for the laptop market
- Requires no electrical outlet

Pocket Edition 2400 is a 3-oz., 3-in.-long modem designed specifically for the business traveler and the laptop market. It requires no electrical outlet, battery pack, or serial-port adapter to connect to a laptop or portable computer

—it runs off the power supplied through the telephone line. The unit comes packaged with cables, Smartcom EZ communications software, and a carrying case. The modem is compatible with 2400-, 1200-, and 300-bps communications. The unit will also send faxes when used in conjunction with an information service like those offered by AT&T, MCI, US Sprint, CompuServe, or Genie. Smartcom EZ provides easy-to-follow menus and phone-book entries to store frequently called numbers. Keyboard macros, extensive on-line help screens, and Autotype, which enables users to transfer text files, are other features of Smartcom EZ. \$179.

Hayes Microcomputer Products Inc., Box 105203, Norcross, GA 30348. Phone (404) 441-1617.

Circle No. 363

Keypad Encoder

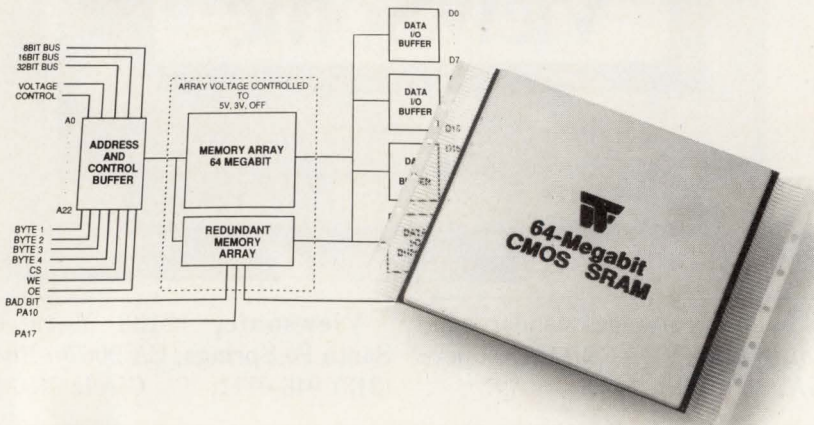
- Is user configurable
 - Designed for IBM compatibles
- The USE144 user-programmable keypad encoder is designed for use with IBM PC/XTs or PC/ATs, compatible computers, or RS-232C devices. The unit is software configurable; both the keypad layout and

keycode values can be changed by the user at any time. Interface type, baud rate, typematic period, and typematic delay are also software configurable. Using a utility program (Usecon), you can program all parameters. Usecon is menu driven and provides utility functions. The 144 works with matrix

keypads and accommodates practically any pinout of rows and columns total 144 keys max. The encoder comes with two standard connectors—a right-angle header for the keypad and a straight header for all interface signals. The encoder operates from a 5V supply to provide true RS-232C compatibility. \$145.

VG Controls Inc, 34 Jenkins Rd, Hewitt, NJ 07421. Phone (201) 853-4600. **Circle No. 364**

64-MEGABIT CMOS SRAMs



Big Memory, Small Package!!

Here's 64-Megabits of CMOS SRAM memory we've just packed into a 120-pin 3" x 3.5" x 0.32" ceramic flatpack. Just right for designs that need a lot of memory, space is scarce, and temperature is a factor.

Look at these key features.

- User Configurable to:
 - 8-Meg x 8,
 - 4-Meg x 16, or
 - 2-Meg x 32
- 150ns Read/Write Time, Max.
- Low Power
 - 5 Volt Operation
 - 120mA Operating Current
 - 1mA Data Retention Current
- Internal Memory Redundancy Correction Mode
- Temperature Ranges
 - Military: -55°C to +125°C
 - Industrial: -40°C to +85°C

- Screening and Burn In to Military Standards Are Available Options

If that's not enough memory, these modules can be combined to get you into the Gigabit range and beyond.

And, if you're after non-volatile memory, we have that too. We have an 8-Megabit Flash PROM in a 34-pin package, and we're working on a new 128-Megabit Flash PROM in a 3" x 3.5" flatpack. We also have a large selection of SRAMs and EEPROMs to fit almost every memory size and package requirement.

More? Yes, much more. We're designing memory systems in the terabit regions, and if you're looking for a complex single-package system, a supercomputer array, or a totally defined multi-package management information system, give us a call. Your imagination or ours, we'll make it happen.



White Technology, Inc.

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CIRCLE NO. 132

20-in. Monitor

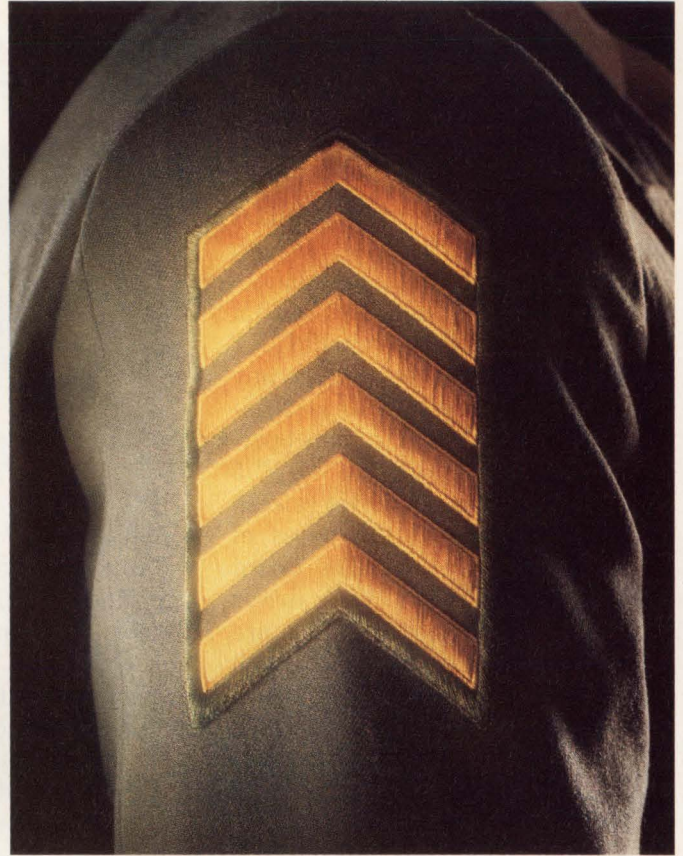
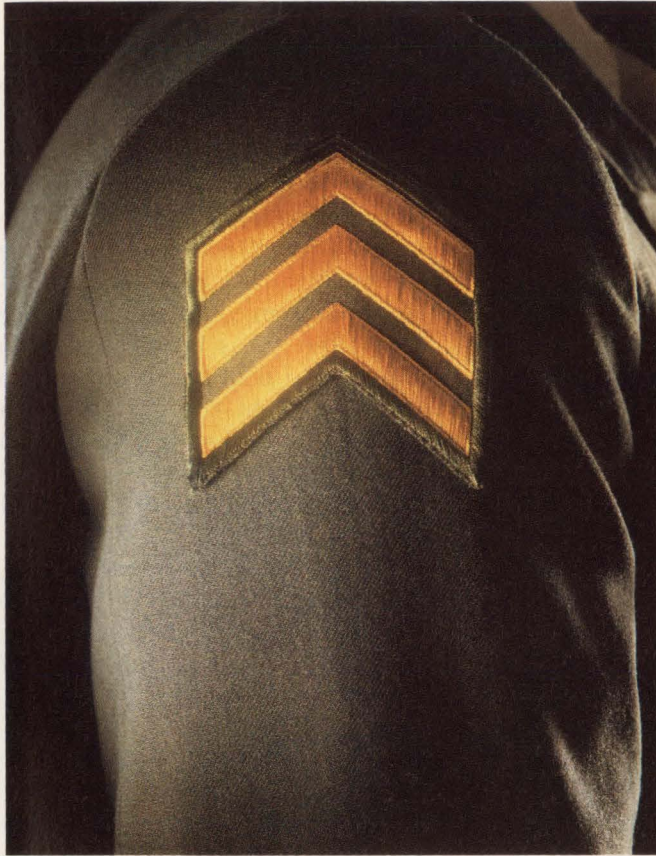
- Fully IBM compatible
- Designed for high resolution applications

The Spectrum Autosync multi-frequency monitor was designed to meet the most demanding high-resolution graphics and text requirements. It features a 20-in. dark tube to optimize picture quality in a wide range of applications including CAD/CAM/CAE, 3-D imaging, window applications medical, and desktop publishing. The unit is housed in a 56-lb plastic cabinet, which locates all controls at the user's fingertips. The unit is fully compatible with all IBM PC/XT, PC/AT, and PS/2 graphics including PGA, VGA, extended VGA, 1024 x 768, and 1280 x 1024 formats. The unit automatically adjusts picture size from horizontal frequencies of 29 to 66 kHz and vertical frequencies of 40 to 120 Hz. The unit comes with a universal-input power supply. \$3195.

Aydin Controls, 414 Commerce Dr, Fort Washington, PA 19034. Phone (215) 542-7800. FAX (215) 542-8447. **Circle No. 365**

Controller Board

- Enhances VGA monitor resolution
 - Includes an antialiasing feature
- The MicroVGA 452 video controller board provides a resolution of 1536 x 1280 with a palette of 742,813




Now, up to twice the power of a standard battery.

Gates introduces two new rechargeables that are commanding everyone's attention: Nickel-Metal Hydride and ULTRAMAX™ Nickel-Cadmium batteries.

Ni-MH offers up to 100% more capacity than a standard Ni-Cd battery, while our ULTRAMAX line offers up to 70% more capacity.

And, with this power increase comes unequaled design flexibility, such as longer run time, additional features, or downsizing without having to sacrifice performance. Contact your nearest sales engineer by calling 1-800-67-POWER.

And see why no battery ranks higher. 

COMPUTERS & PERIPHERALS

colors on a standard 640 × 480 VGA monitor. An antialiasing feature reduces stair-stepping and provides users with straight lines, smooth circles and arcs, and near photo-realistic images. The board is IBM PC/AT-compatible; with its' PC/XT form-factor, it can be used in any size PC enclosure in 16-bit expansion bus slots for applications operating at speeds ranging to 12.5 MHz. The unit has a 60-Hz refresh rate and includes 512k bytes of video RAM on board. The board comes with an Ultra VGA driver for Autodesk applications that use the ADI 4.0 display list driver, such as AutoCAD, Autoshade, and Autosketch. There's also an Ultra VGA driver for Microsoft Windows 3.0. \$395.

Monolithic Systems Corp, 7050 S Tucson Way, Englewood, CA 80112. Phone (303) 790-7400. FAX (4303) 790-7118. **Circle No. 366**



Tape Drive

- Provides 2G-byte storage
- Supports all SCSI commands

The Model 7200 digital audio-tape drive is a 3 1/2-in. form factor unit which provides 2G bytes of data storage on a single cassette without using data compression. Using a 2:1 data-compression ratio, the unit has a 4G byte storage capacity. Fully DDS compatible, the unit supports all standard SCSI commands and features a fast search mode that locates files

within 20 sec. The drive includes a head cleaner that automatically activates a loaded cassette. The drive design allows users to employ the company's EEPROM technology to custom-configure the device even after it has been installed in a system. Updates can be sent to the drive from the system via a SCSI bus, or they can be loaded directly into the drive from a digital audio-tape cassette. \$1200 (OEM qty).

Wangtek Inc, 41 Moreland Rd, Simi Valley, CA 93065. Phone (805) 583-5255. FAX (805) 583-8249.

Circle No. 367

PC/AT Extender Card

- Provides protective buffering
- Controlled by users' test program

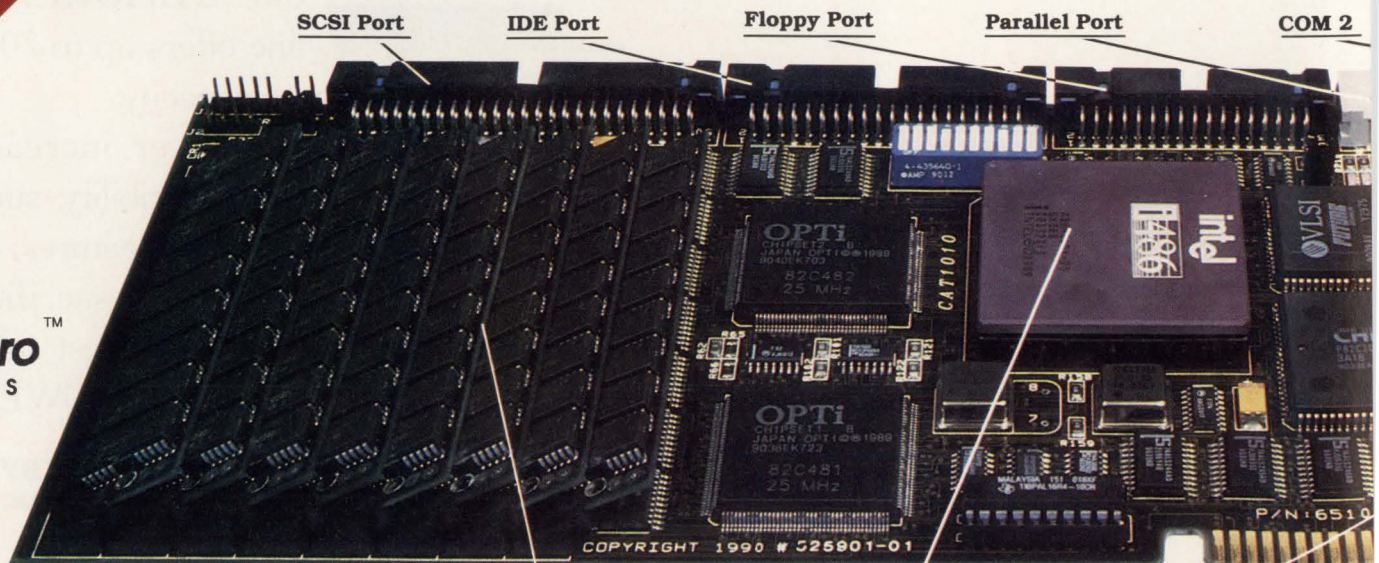
The IBM PC/AT-EXT AT-compatible extender card provides a buffer for the computer circuits and other

Inquire about
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About The DTI 25/33MHz '486'



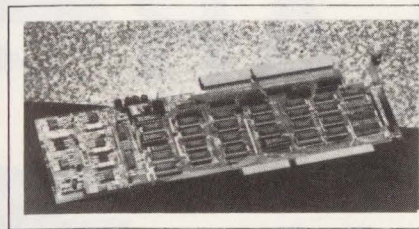
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RAM On-board**

**High Performance Intel
80486 33MHz**

**Industry Standard
Custom BIOS**



cards. It allows the card under test to be removed or inserted without powering down the PC or affecting the PC's operation. Card control takes place either manually with on-card switches or by instructions from the users' test program. You insert the card to be tested in the connector on top of the extender and run your test program or turn the extender card's power. In either case, the card will sequence power and ground signals on and off in a nondisruptive manner. A 2-color LED indicates when power is applied to the card under test. Any current overload or voltage short circuit shuts off power to the

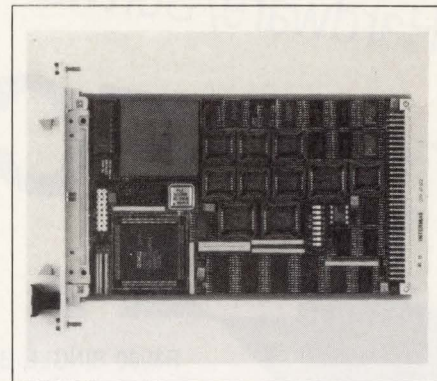
card. The card works in all IBM PC/ATs and compatible computers. \$495.

ICS Electronics Corp, 744S Hillview Dr, Milpitas, CA 95035. Phone (408) 263-5500. FAX (408) 263-5896. **Circle No. 368**

Interface Board

- Provides intelligent SCSI and Ethernet interfaces
- Works in 3U and 6U VMEbus systems

The MZ 8554 multifunction peripheral board that provides intelligent Ethernet and SCSI interfaces. A single-height (3U) design, the board is designed to work in both 3U and 6U VMEbus systems. The unit is supported by Unix and other leading operating systems. The unit provides a SCSI interface based on the NCR 53C700 SCSI I/O processor and an Ethernet interface based on the Intel 82596 Ethernet copro-

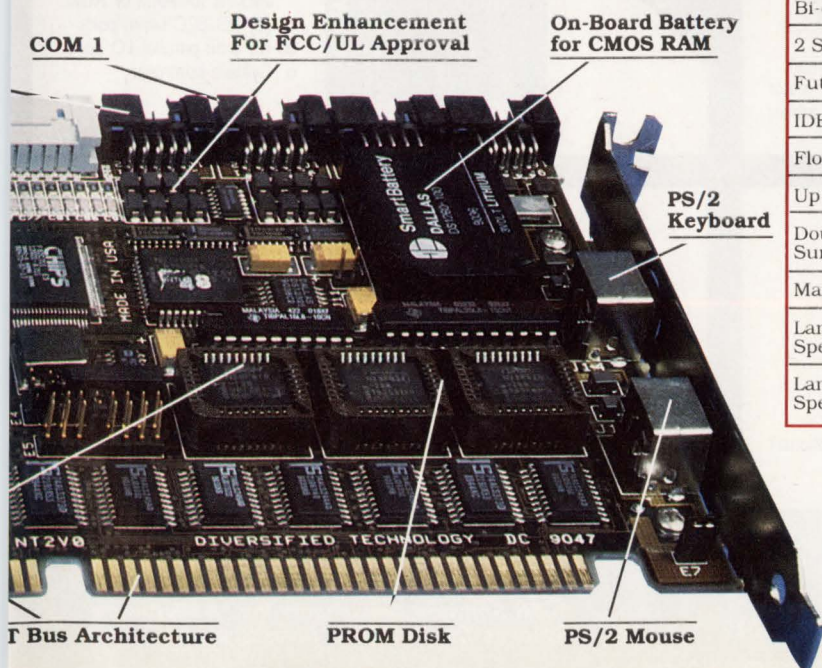


cessor. Both of the interfaces provide direct memory access to 128k bytes of onboard buffer memory. Both interfaces can execute command sequences independent of the host processor. Software included with the boards provides support for Unix system V release 4 and real-time operating systems such as Microware's OS-9. \$995.

Mizar Inc, 1419 Dunn Dr, Carrollton, TX 75006. Phone (214) 446-2664. **Circle No. 369**

REAL FACTS!

Single Board Computer



COMPARE FUNCTION	DTI CAT1010 486	Competitor 1 486	Competitor 2 486
25, 33MHz CPU- Shipping Now!	✓		25MHz Only 7-8 Wks Del.
Up to 32M RAM Onboard	✓		
Noise Reduction Circuitry For FCC Class B	✓		
PS/2 Mouse Support	✓		
PS/2 Keyboard Support	✓		
On-Board Battery Real Time Clock	✓		✓
Bi-directional PS/2 Printer Port	✓		
2 Serial Ports - Up to 115K Baud	✓		
Future Domain SCSI	✓		
IDE Interface	✓		
Floppy Interface	✓		
Up to 512Kb User PROM Disk	✓		
Double Sided Surface Mount Technology	✓		
Manufactured In-House(U.S.A.)	✓		
Landmark V1.14 Speed at 25MHz	114.1		84
Landmark V1.14 Speed at 33MHz	150.9		

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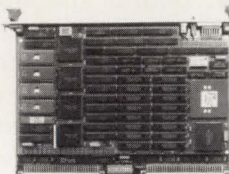
U.S.A. - (601) 856-4121 Fax (601) 856-2888
Outside U.S.A. - (201) 891-8718 Fax (201) 891-9629

OMNIBYTE'S
Hardware/Software

VME SPECTACULAR

OB/ACP-VR3000™

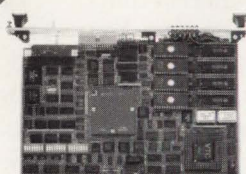
R3000 SINGLE BOARD COMPUTER



- o 25MHz MIPS R3000 CPU
- o 25MHz R3010 FPC
- o (4) 25MHz R3020 write buffers
- o 128KB (or 32KB) I cache
- o 128KB (or 32KB) D cache
- o 4, 8, 16, or 32MB DRAM
- o (1) RS232C serial port
- o (4) 28-pin EPROM sockets

OB68K/VME40™

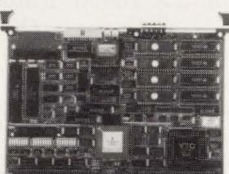
SINGLE BOARD COMPUTER



- o 68040 25-33MHz CPU
- o (8) 28-pin SRAM sockets (up to 256KB)
- o (8) 32-pin ROM sockets (up to 8MB)
- o (2) RS232C serial ports
- o (16) lines of parallel I/O
- o (1) OMNIMODULE socket
- o VICO68 VME Controller

OB68K/VME20™

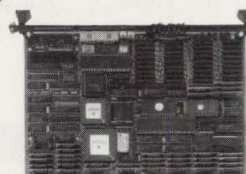
SINGLE BOARD COMPUTER



- o 68020 16.66-33MHz CPU
- o (8) 28-pin SRAM sockets (up to 256KB)
- o (8) 32-pin ROM sockets (up to 8MB)
- o (2) RS232C serial ports
- o (16) lines of parallel I/O
- o (1) OMNIMODULE socket
- o VICO68 VME Controller

OB68K/VSBC20™

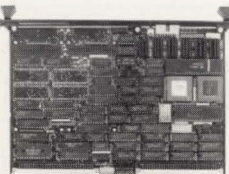
SINGLE BOARD COMPUTER



- o 68020 16-33MHz, CPU
- o 1 - 4MB DRAM
- o 68882 (optional)
- o (2) 32-pin ROM sockets
- o (2) RS232C serial ports
- o (2) 8-bit parallel ports
- o (1) OMNIMODULE socket for a wide variety of I/O
- o 4 level bus arbiter (opt.)

OB68K/VSBC1™

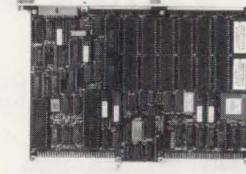
SINGLE BOARD COMPUTER



- o 68000 12.5-16MHz CPU
- o 512KB DRAM
- o (4) 28-pin ROM sockets
- o (3) 16-bit counter/timers
- o (2) OMNIMODULE I/O sockets
- o DMA controller (optional)
- o Optional interrupt generator
- o Optional 4 level bus arbiter

OB68K/VME1™

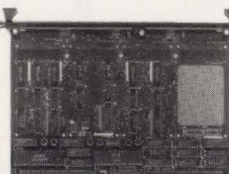
SINGLE BOARD COMPUTER



- o 68000 12.5-16MHz CPU
- o (8) pairs of 28-pin sockets for RAM or ROM
- o (2) RS232C serial ports
- o (2) 8-bit parallel I/O ports
- o System controller

OB68K/VIO™

UNIVERSAL I/O BOARD



- o (4) OMNIMODULE I/O sockets for a wide variety of I/O (i.e. 8 serial ports, 80 parallel lines)
- o One (1) interrupt per OMNIMODULE (2 optional)

AVAILABLE SOFTWARE

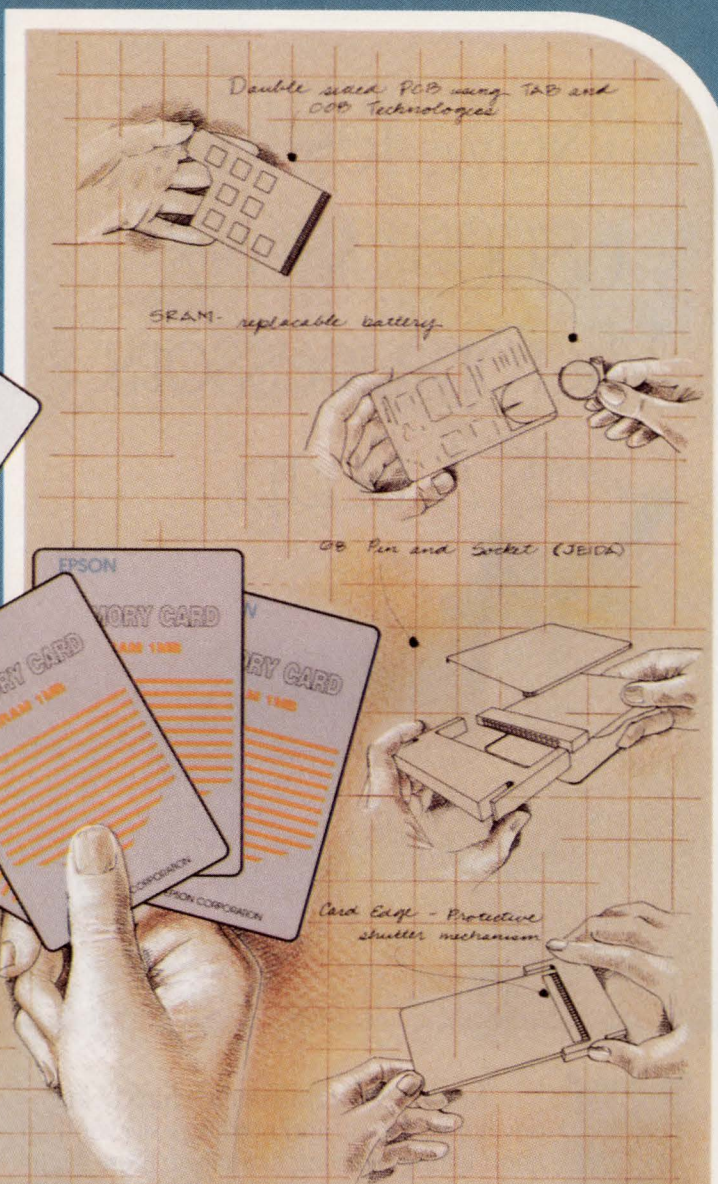
	680x0	R3000
Monitor	VERSAbug/020 bug ¹	SPPe ²
Debugger	FreeForm ³	SPPe
Cross Compiler	CrossCodeC ³	IDT/c ⁴
Real Time Monitor	C EXECUTIVE ⁵	C EXECUTIVE ⁵
Real Time O.S.	Industrial OS-9 ⁶	VxWorks ⁷
Full O.S.	Professional OS-9 ⁶	RISC/os ²

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EPSON® IC MEMORY CARDS



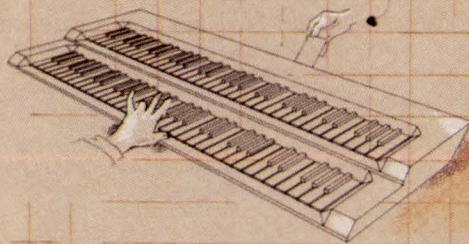
JEIDA/PCMCIA

SRAM	64kB to 2M
OTP EPROM	64kB to 2M
Flash EEPROM	64kB to 1M
Mask ROM	256kB to 8M
EEPROM	16kB to 32kB

Storage and Software

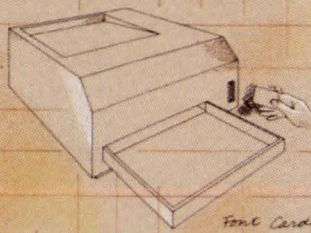
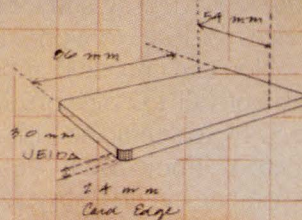


Musical Sound Cards

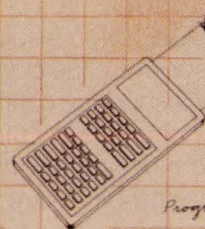


CARD EDGE

SRAM	8kB to 1M
OTP EPROM	32kB to 1M
Flash EEPROM	128kB to 1M
Mask ROM	128kB to 4M
EEPROM	8kB to 32kB



Font Cards



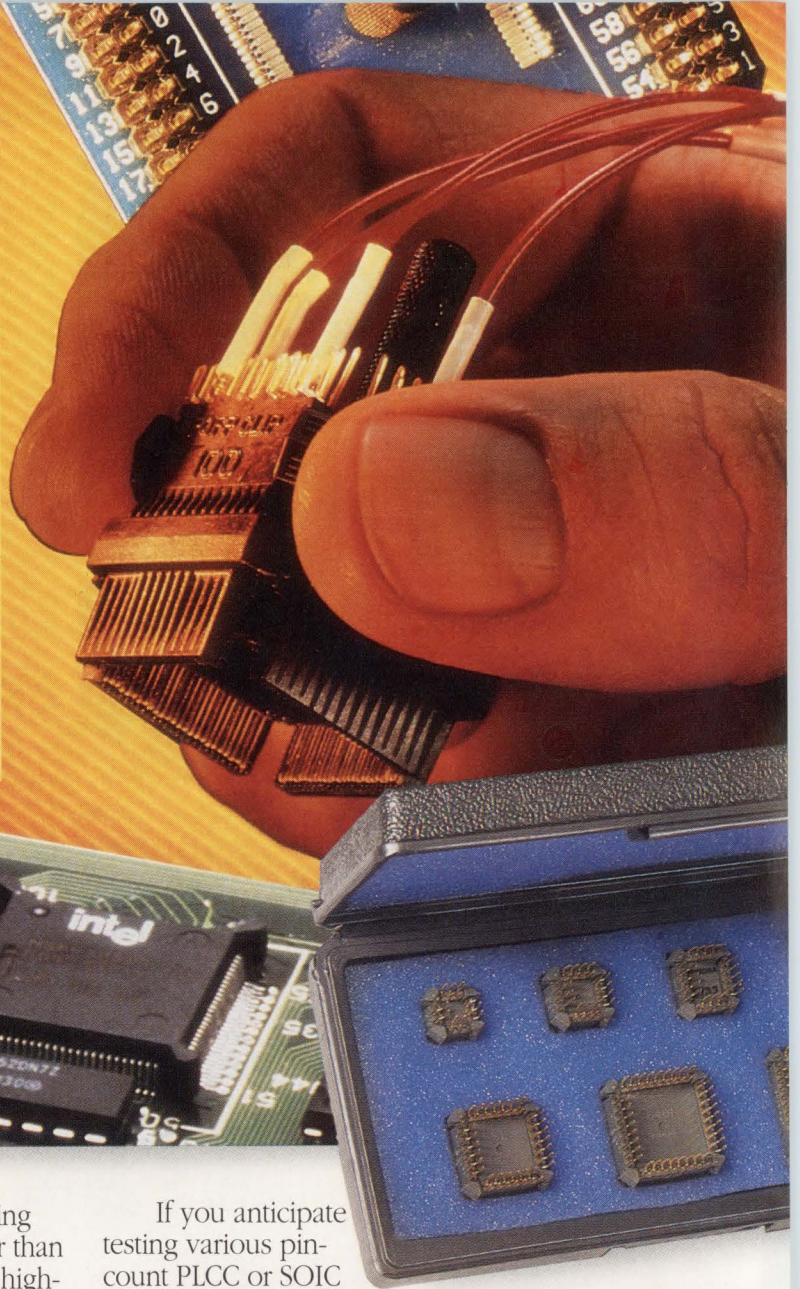
Programs and memory

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Now, Testing 68000/386SX Microprocessors Is A Snap.



Nothing's faster than the chips being developed today, and nothing's slower than hand wiring or trying to analyze these high-density, surface mounted quad flat pack (QFP) devices for test. No worry, Pomona has the answer.

You can choose Pomona's 5711 SMT Test Clip to grab onto all 132 pins of a Motorola 68020 or 68030, or the 5713, to simultaneously access all 100 pins of an Intel 80386SX. Immediately, your interface with logic analyzers, on-line circuit test systems, or lab instruments will be faster, easier, and reliable. A locking mechanism firmly holds the glass-filled, Nylon insulated clip onto the device, making positive contact with each of the IC's gull-wing leads via specially configured, gold-plated, beryllium copper pins. Above, multi-rows of gold-plated phosphor-bronze pins provide an easy-to-access pattern. Suddenly, interface problems are solved.

If you anticipate testing various pin-count PLCC or SOIC devices, Pomona's Test Clip Kits will make testing faster too. And, to make the interface between your test clip and logic analyzer sockets or emulator pods easier, Pomona's Flying Leads are available in low-cost packs, or supplied with the 5711 and 5713 Test Clips as kits. Of course, all of Pomona's other SMT test accessories are ready to make your IC testing faster and less expensive.

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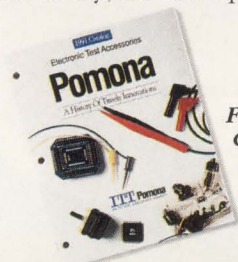
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5515A PLCC Clip Kit
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Adapters from 20-84 pins.

Color-coded Flying Leads simplify interconnections between PLCC or SOIC test clip and logic analyzer sockets or emulator pods; 3 inches long, with female socket one end to .79 dia. pin.
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NEW PRODUCTS

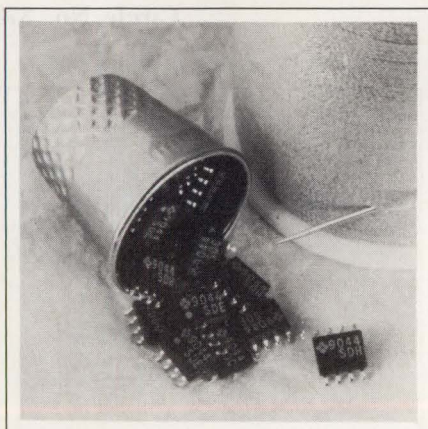
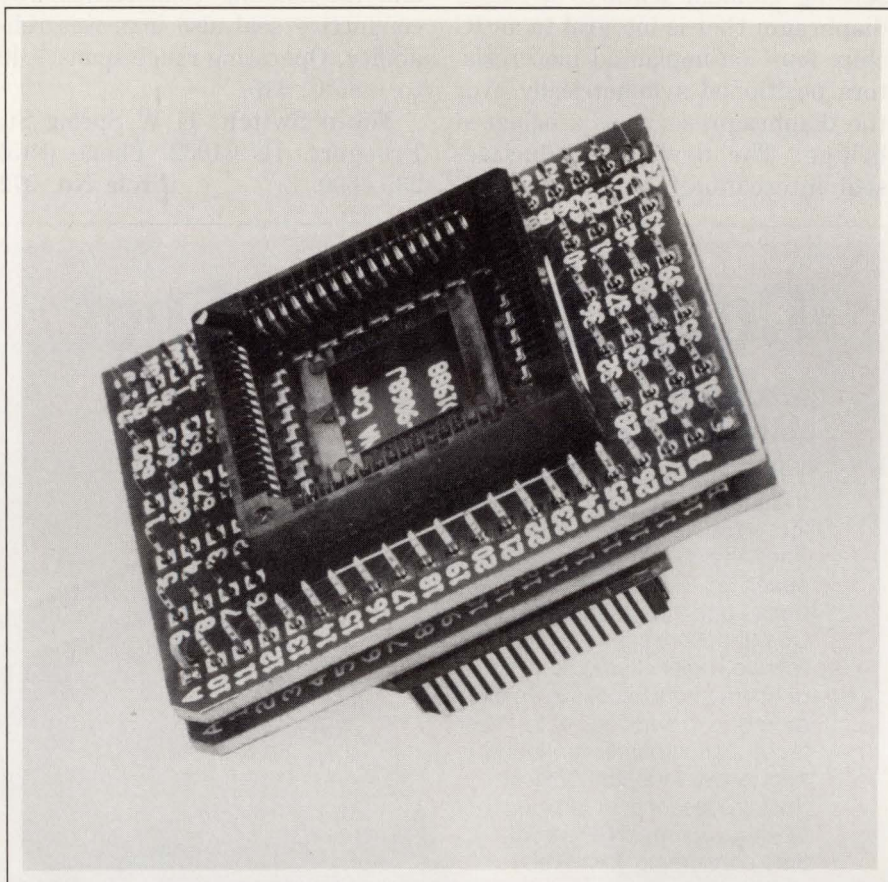
COMPONENTS & POWER SUPPLIES

Test Adapter

- Tests plastic-leaded-chip-carrier components
- Provides numbered test points

The ANC-4068 provides designers with a method to test and monitor socketed plastic-leaded-chip-carrier (PLCC) components. Numbered test points are provided for scope and meter lead attachment. Modular in construction, the test adapter is easily reconfigured to accommodate PGA (pin-grid-array) or LCC devices by plugging in optional component socket cards. You can also stack the component cards to debug and test multiple levels of PLDs. The base-unit ANC-4068 provides two PLCC stacking levels, and it can be installed in either PGA or PLCC sockets with the mating plugs included. The adapter is also available in 52- and 84-pin versions. \$154; optional adapters, \$49.

Antona Corp., 1643½ Westwood Blvd, West Los Angeles, CA 90024. Phone (213) 473-8995. FAX (213) 473-7112. **Circle No. 370**



Diode Arrays

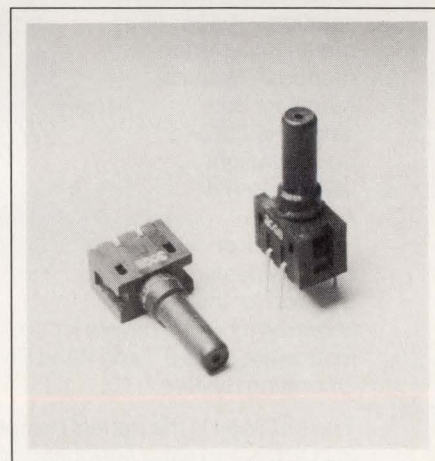
- Are surface mountable
- Feature four diodes in a single package

Available in unidirectional and bidirectional versions, SMDA Series diode arrays are housed in 8-pin surface-mountable TO-8 packages.

Based on Transzorb technology, each unit consists of four independent diodes. Each device protects against power peaks ranging to 300W, has a 5A forward-surge rating, and operates over a range of -55 to +150°C. You can use the board-mountable units to protect all I/O ports and power bus lines. The devices are available for data lines and bus lines rated at 5, 12, 15, and 24V. Housed in molded-unit packages, the diode arrays feature a gull-wing-lead configuration. The low-profile packages are designed to minimize inductance. Unidirectional models, \$2.95; bidirectional models, \$3.05 (1000).

General Semiconductor Industries Inc., 2001 W 10th Pl, Tempe, AZ 85281. Phone (602) 968-3101.

Circle No. 371



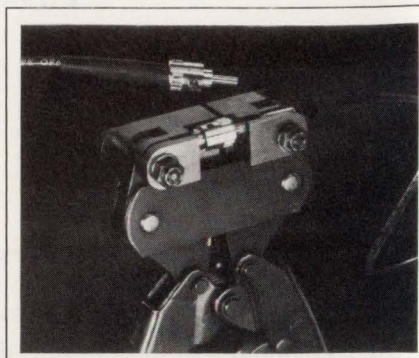
Miniature Pressure Sensors

- Provide wet-wet sensing for added versatility
 - Have 1- to 30-psi range
- Series 24PC pressure sensors provide wet-wet sensing capability.

The line includes units that offer from 0 to 1 psi to 0 to 30 psi. A sensing element features a silicon diaphragm that is integral to an IC chip; four ion-implanted piezoresistors positioned symmetrically over the diaphragm serve as a balanced bridge. The devices' conductive-seal interconnect system cuts as-

sembly time and saves overall production costs by eliminating wire- and tab-bonding connections. The conductive seal also improves reliability. Operating range spans -40 to +85°C. \$15.

Micro Switch, 11 W Spring St, Freeport, IL 61032. Phone (815) 235-6600. **Circle No. 372**



Fiber-Optic Connector

- Has crimp termination
- Has 1-dB insertion loss

The Lighterimp ST-Style fiber-optic connector can be terminated to optical fibers using a straightforward crimping technology—no epoxy, oven, or ultraviolet curing is required. A key feature of the unit is an innovative fiber-retention system. This system, combined with simple hand tools, allows a fiber to be terminated within 2 minutes. The 2.5-mm bayonet connector has a 1-dB max insertion loss and a lifetime specification of 500 cycles. Operating range spans -20 to +60°C. \$6 to \$7.

AMP Inc, Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752; in PA, (717) 564-0100.

Circle No. 373

Compact SCSI / Enet

Mizar's new MZ 8554 packs maximum I/O into minimum VME space.

The newest addition to Mizar's expanding line of 3U VMEbus boards is the perfect solution for your system I/O needs. The MZ 8554 provides intelligent, high speed SCSI and Ethernet interfaces based upon the latest IC technology. Designed for superior system performance, both interfaces provide direct memory access to on-board memory. In addition, both interfaces can execute command sequences independently of host processor intervention, freeing your main CPU from time consuming low-level protocol handling.

The economical alternative to expensive two board solutions, the MZ 8554 meets high-performance I/O requirements for both single-height and double-height VME systems. And, the MZ 8554's price can't be beaten! Support for the MZ 8554 includes drivers for both Microware's OS-9™ and Wind River Systems' VxWorks™ Real-Time Operating System.

The MZ 8554 is the perfect complement to Mizar's extensive line of 3U CPU's and other peripheral boards. To find out why more and more engineers are turning to VME boards from Mizar, call today.

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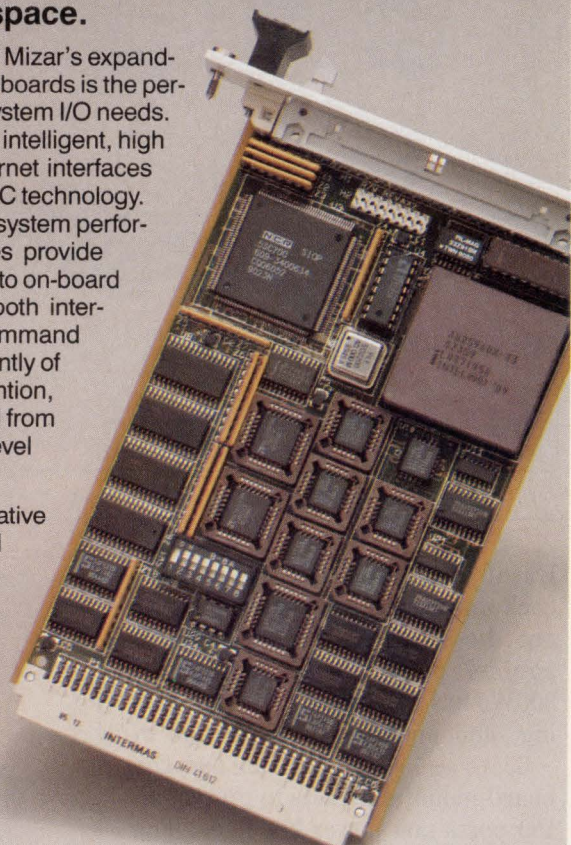
1-800-635-0200.

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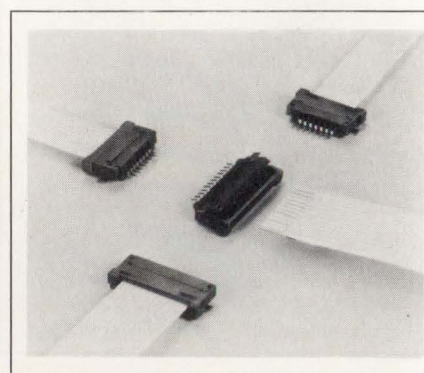
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MIZAR

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(214) 446-2664



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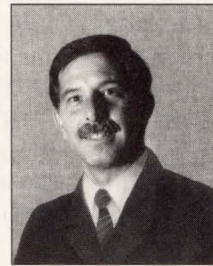
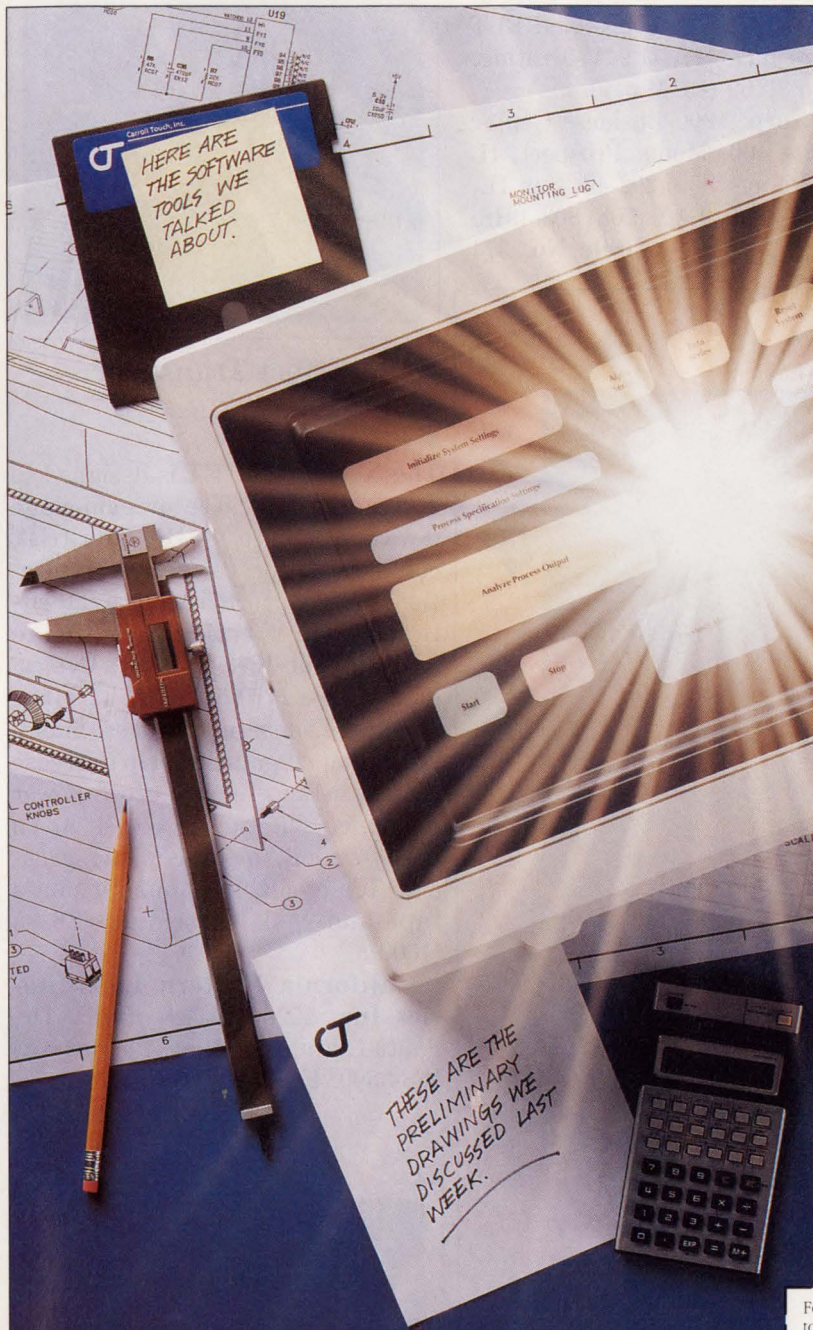


Snap-Lock ZIF Cable Connectors

- Provide ZIF connection
- Are surface mountable

Type FPZ miniature flex/flat cable connectors feature a hinged snap-lock cover that provides a zero-

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 Hewlett-Packard Company

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"Carroll Touch people really approach our projects as a team project."

"Working with Carroll Touch people is great because everybody is part of the team – which helps us create a very successful product. Their willingness to go that extra step makes our job much easier.

"In developing a recent functional spec for a touch frame, Carroll Touch engineers worked closely with us in making sure that the assemblies would survive electrostatic discharge.

"We held design reviews of the various approaches and all of our recommendations were considered very sincerely by Carroll Touch. Comments were intelligently relayed back to us and everything we asked for was delivered in the specified time."

For more information on how Carroll Touch can help you create success with your touch technology applications, call 512/244-3500, or simply mail your business card with this coupon to Carroll Touch, P.O. Box 1309, Round Rock, Texas 78680.

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Company Name _____

Address _____

City _____ State _____ Zip _____

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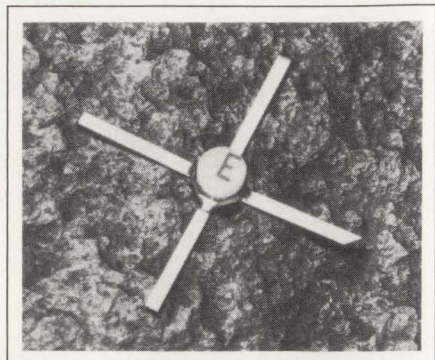
Carroll Touch
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 EDN 062091

insertion-force connection. The surface-mountable units have a 1-mm pitch and a closed height of 2.9 mm. The right-angle connectors accommodate from 7 to 25 circuits and are available on embossed tape for compatibility with auto-insertion equipment. Connector contacts are phosphor bronze with a tin plating.

The contacts are rated for 0.5A at 50V ac or dc. The glass-filled PBT housings have a UL 94V-0 rating. \$0.40 to \$0.60 (OEM qty).

JST Corp, 1200 Business Center Dr, Suite 400, Mount Prospect, IL 60056. Phone (800) 292-4243; in IL, (708) 803-3300. FAX (708) 803-4918.

Circle No. 374



Field-Effect Transistor

- Operates to 13 GHz
- Has 9.5-dB gain

The NE42184A FET is designed to serve as a low-noise or gain-stage device for 0.5- to 13-GHz industrial, commercial, or consumer applications. Key performance characteristics include a typical noise figure of 1.2 dB at 12 GHz and a typical gain figure of 9.5 dB at 12 GHz. The FET design features mushroom-shaped gates to help decrease gate resistance and improve power handling. The device comes in an epoxy-sealed, metal-ceramic package. It's available in quantity on a tape-and-reel cartridge. \$6.85 (1000).

California Eastern Laboratories Inc, 4590 Patrick Henry Dr, Santa Clara, CA 95054. Phone (408) 988-3500. FAX (408) 988-0279.

Circle No. 375



Digital Attenuator

- Operates to 4 GHz
- Has 32-dB max attenuation

The Model DAS-124 attenuator operates over a frequency range of 1 to 4 GHz and can switch as many as 4 bits. Bit attenuation figures

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CIRCLE NO. 143

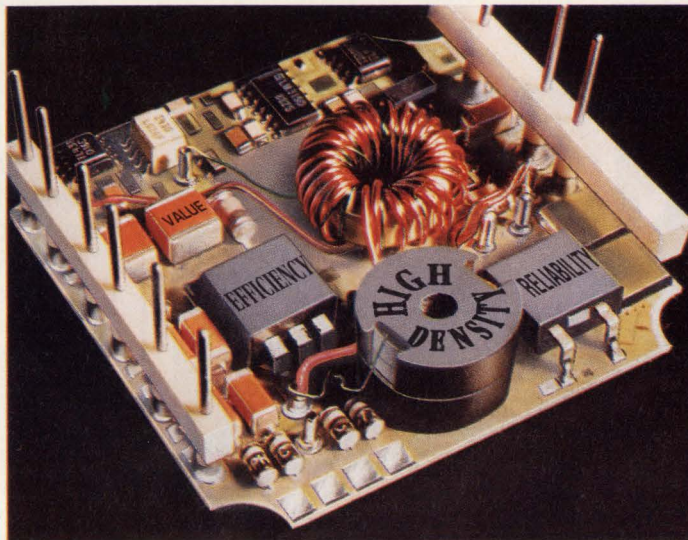
WHEN WE DESIGNED OUR NEW NFC SERIES DC/DC CONVERTERS, WE INCLUDED EVERYTHING. EXCEPT COMPROMISE.

Designed to fulfill the needs of the nineties, our new NFC family of power converters are more compact, consistent and cost effective than competitive products.

For example, the NFC40 packs over 16 watts per cubic inch — 5 times more than similar converters. Plus up to three outputs with various user interface functions. The cooling baseplate makes heat-sinking easy. And its small footprint and low profile are ideal for space critical applications in telecom and data communications.

But more power and features per inch weren't the only goals we set for ourselves. We built in more reliability too. Most models

are built on a rugged thick film hybrid substrate in an automated assembly process so highly con-



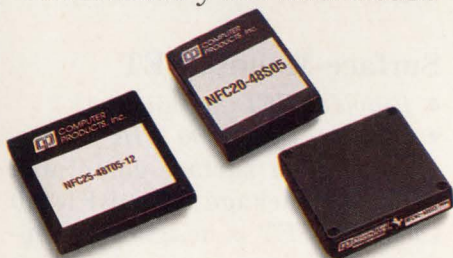
trolled and repeatable, you get consistent quality and reliability whether you order ten or ten thousand. And lower costs too!

The NFC family's high efficiency allows them to withstand hot ambient temperatures. Their wide input voltage range lets you operate from a poorly regulated 24V or 48V power source, or

even from a battery as it discharges.

Best of all, the NFC series is a winner in value too. Because in addition to more power density and reliability, we also included many useful features. Like a choice of single or multiple user-adjustable outputs. Or converter inhibiting with a simple TTL signal.

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NFC25 25W triple output.
Density: 6W/cubic inch.
Wide range input.
Output voltage adjust, TTL inhibit.

NFC20 20W single and double output.
Density: 14W/cubic inch.
Wide range input.
Hybrid technology.
Output voltage adjust, TTL inhibit.

NFC15 15W single and double output.
Density: 10W/cubic inch.
Wide range input.
Hybrid technology.
Output voltage adjust, TTL inhibit.

3797 Spinnaker Court, Fremont, California 94538 Phone: 415-657-6700, FAX: 415-683-6400

range from 0.5 dB min to 32 dB max. The unit uses advanced CMOS-TTL-compatible drivers that provide switching speeds of 100 nsec max. The miniature all-ceramic (including lid cover) surface-mount package is microstrip compatible and features solderable or wire-bondable transmission line

and logic input connections. Additional attenuator models provide a 6-bit switching capability but have a reduced operating frequency range. 4-bit model, \$400.

KDI/Triangle Electronics, 60 S Jefferson Rd, Whippany, NJ 07981. Phone (201) 887-8100.

Circle No. 376

Bilevel LED Arrays

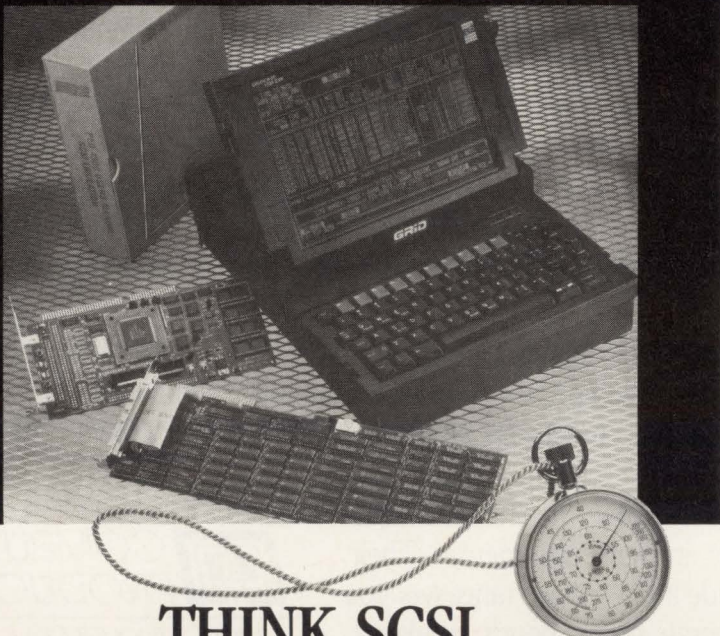
- Available with red, yellow, and green LEDs
- Available in a number of versions

Available with red, yellow, or green LEDs, Series 552 and 553 bilevel arrays are designed for high-density pc-board applications. The 552 models feature T-1³/₄-sized LEDs, and the 553 models offer T-1-sized LEDs. The 552 Series units are available in standard-efficiency, high-efficiency, super-bright, and super-efficiency versions. A bicolor (red/green) LED and units with integral resistors are also available in the series. The 553 Series includes three versions—standard efficiency without resistor, a super-efficient unit for 2-mA operation, and a 5V unit, which includes a built-in resistor. Operating range spans -20 to +100°C and -55 to +100°C for 552 and 553 Series devices, respectively. Series 552, from \$1.11; Series 553, from \$1.16 (1000). Delivery, stock to eight weeks ARO.

Dialight Corp, 1913 Atlantic Ave, Manasquan, NJ 08736. Phone (908) 528-8932. FAX (908) 223-8788.

Circle No. 377

THINK FAST.



THINK SCSI.

Think SCSI analyzer. Technology moves fast; that includes the speed of peripheral devices using SCSI bus architecture. Not to worry. Pacific Electro Data has the tools to detect the errors and bugs that **WILL** pop up on the SCSI bus.

Speaking of fast, our analyzer systems can continuously capture data at rates of more than 10MB/sec with a timing resolution of 40 Nsec.

News flash... Pacific Electro Data just added a powerful SCSI emulation system to their rapidly growing analyzer product line. Working in conjunction with their existing systems, it's easy to emulate target and initiator devices.

That includes the CPU, drives and other

peripherals. This integrated emulation can synchronously transfer data at burst rates up to 10MB/sec. That's fast.

Another news flash... The PED analyzer and emulation systems are now offered completely installed in either the top-ranking **Grid™** computer or other portable systems. The **Grid 386** laptop comes with a 40MB HDD, 72-key keyboard, rugged magnesium case and either a blue backlit or a gas plasma display.

Maybe you don't need fast... take a few days off and check out the bugs and errors on the SCSI. Or go F-A-S-T and call Pacific Electro Data to learn about

their fast SCSI portable analyzer and emulator systems.



14 Hughes, Ste. B205, Irvine, CA 92718

Tel: (714) 770-3244 ■ 1-800-676-2468 ■ Fax: (714) 770-7281

Surface-Mount JFET

- Provides RFI immunity
- Operates in the 900-MHz range

Housed in a surface-mountable SOT-143 package, the BFR200 Channel JFET is designed to suppress RFI in sensitive detection equipment. By integrating two resistors and two MOS capacitors onto a single silicon chip, the unit adds a lowpass filter to the input stages of this sensitive equipment and suppresses RFI signals in the 450- to 900-MHz cellular radio range. The JFET eliminates the need for additional passive components. The device is designed primarily to prevent the generation of false events in IR detectors, burglar alarms, electret microphones,

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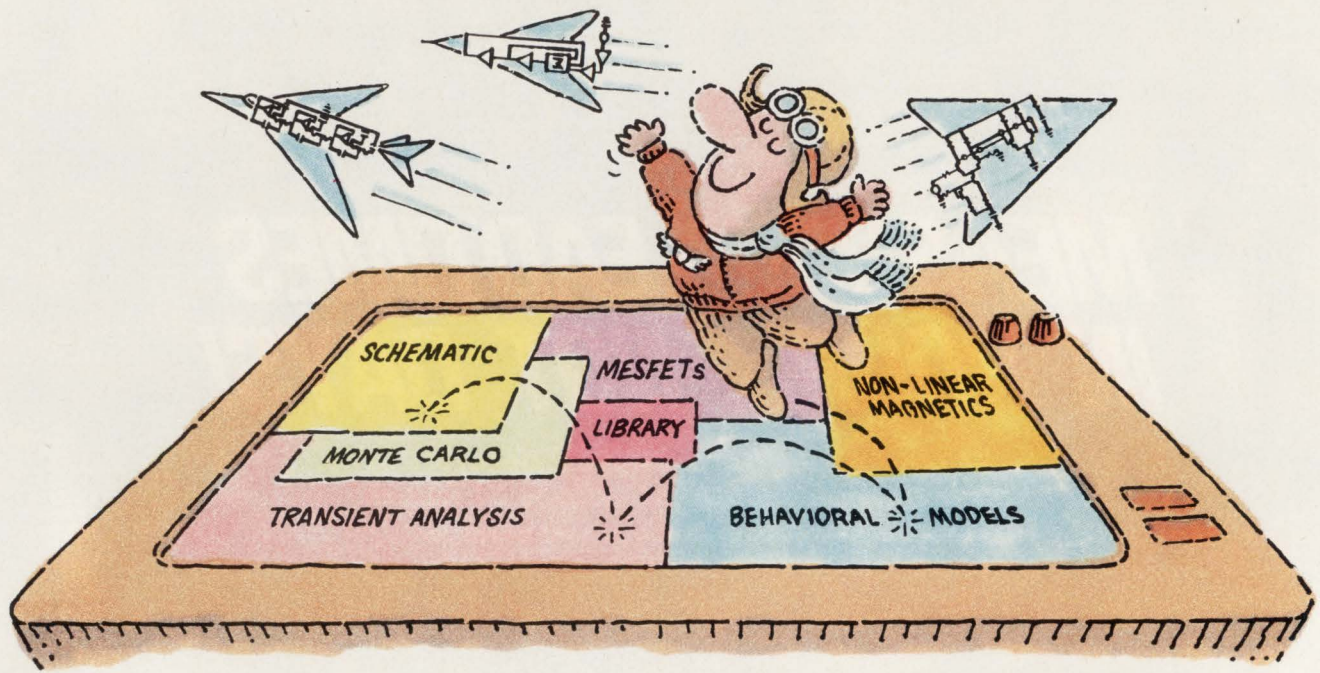
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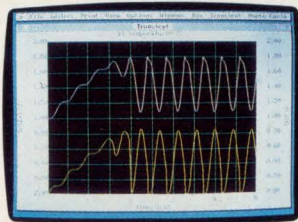
THE NEW MICRO-CAP III.TM SO YOU CAN TEST-FLY EVEN MORE MODELS.

It wasn't easy. But we did it. Made the long-time best-selling IBM® PC-based interactive CAE tool even better.

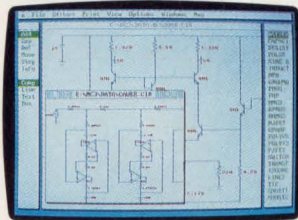
Take modeling power. We've significantly expanded math expression capabilities to permit comprehensive analog behavioral modeling. And, beyond Gummel Poon BJT and Level 3 MOS, you're now ready for nonlinear magnetics modeling. Even MESFET modeling.

Analysis and simulation is faster, too. Because the program's now in "C" and assembly language. That also means more capacity — for simulating even larger circuits.

As always, count on fast circuit creation, thanks to window-based operation and a schematic editor. Rapid, right-from-schematics analysis — AC, DC, fourier and transient — via SPICE-like routines. The ability to combine digital/analog circuit simulations using integrated switch



Transient analysis



Schematic editor



Monte Carlo analysis

models and parameterized macros. And stepped component values that streamline multiple-plot generation.

And don't forget MICRO-CAP III's extended routine list — from impedance, Nyquist diagrams and BH plots to Monte Carlo for statistical analysis of production yield. The algebraic formula parsers for plotting virtually any function. The support for Hercules, CGA, MCGA, EGA and VGA displays. Output for plotters and laser printers.

Cost? Still only \$1495. Evaluation versions still only \$150. Brochure and demo disk still free for the asking. Call or write for yours today. And see how easily you can get ideas up and flying.

spectrum

1021 S. Wolfe Road
Sunnyvale, CA 94086
(408) 738-4387

COMPONENTS & POWER SUPPLIES

smoke detectors, and radiation detectors. It has a low leakage current of 2 pA typ. Two antiparallel diodes connected to its gate make the JFET very compatible for use in source-follower circuits. \$0.40 (10,000). Delivery, stock to eight weeks ARO.

Philips Components, 2001 W Blue Heron Blvd, Riviera Beach, FL 33404. Phone (800) 447-3762.

Circle No. 378

Bypass Boards

- Provide simple jumpering
- Maintain system airflow

These bypass boards provide a simple solution to the problem of filling empty or spare slots in a VXIbus system. The units electrically pass through the Busgrant and IACK daisy-chained signals to other boards in the system. Air baffles provided on the board surface maintain the integrity of the air-flow system. On each model, a front panel, complete with ejectors, is attached to an aluminum substrate that doubles as an RFI barrier. A specially configured male DIN connector provides the bypass path for the signals. The boards are available in A, B, C, and D sizes as specified in the VXIbus standard. C-size board, \$44.63 (100).

Dawn VME Products, 47073 Warm Springs Blvd, Fremont, CA 94539. Phone (415) 657-4444. FAX (415) 657-3274. Circle No. 379

1500W Power Supply

- Has 0.99 power factor
- Meets IEC-555-2 specification

The SPF4 supply provides as much as 1500W of power and features a 0.99 power factor. It meets all international safety and EMI requirements including the IEC-555-2 specification for input-current harmonic content. The supply also features a universal 85 to 264V ac input, and it can be configured to provide as many as 12 outputs.

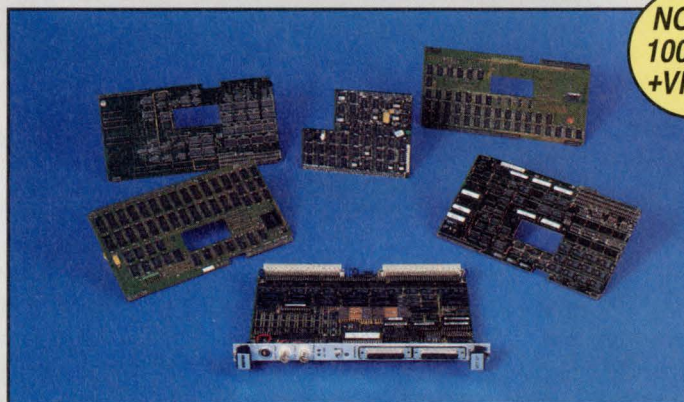
A selection of 38 fully regulated single- and multiple-output modules is available in voltages of 2 to 48V and power ratings of 240 to 1250W. Parallel operation with true current sharing is standard on all single-output modules. A steel 5×8×11-in. package, which is by a ball-bearing fan, fully encloses

the power supply. \$1091 (OEM qty).

Power-One Inc, 740 Calle Plano, Camarillo, CA 93010. Phone (800) 678-9445; in CA, (805) 987-8741. TWX 910-336-1297.

Circle No. 380

The Ultimate VMEbus Tool Set

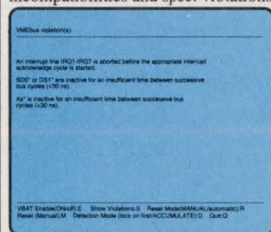


Based on the VBT-321 Advanced VMEbus Analyzer, VMETRO's Modular VMEbus Analyzer System offers piggyback modules for all kinds of VMEbus development, verification and tuning purposes.

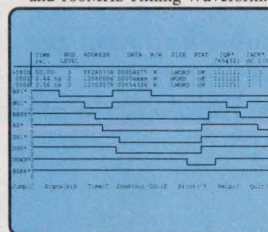
VMETRO's Modular VMEbus Analyzer System gives you unrivalled measurement capability in a single VMEbus slot. Pick the right piggyback module to the VBT-321 VMEbus Analyzer and obtain:

- * VMEbus Anomaly Trigger
- * VSB State Analysis
- * VME Cycle Generator
- * 100MHz VME Timing Analysis
- * P2 General Purpose Analysis
- * 256K Trace w/SCSI dump

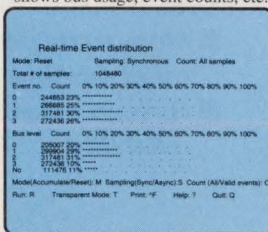
VMEbus Anomaly Trigger reveals incompatibilities and spec. violations.



Combined VMEbus State trace and 100MHz Timing Waveform.



Real-time VMEbus histograms shows bus usage, event counts, etc.



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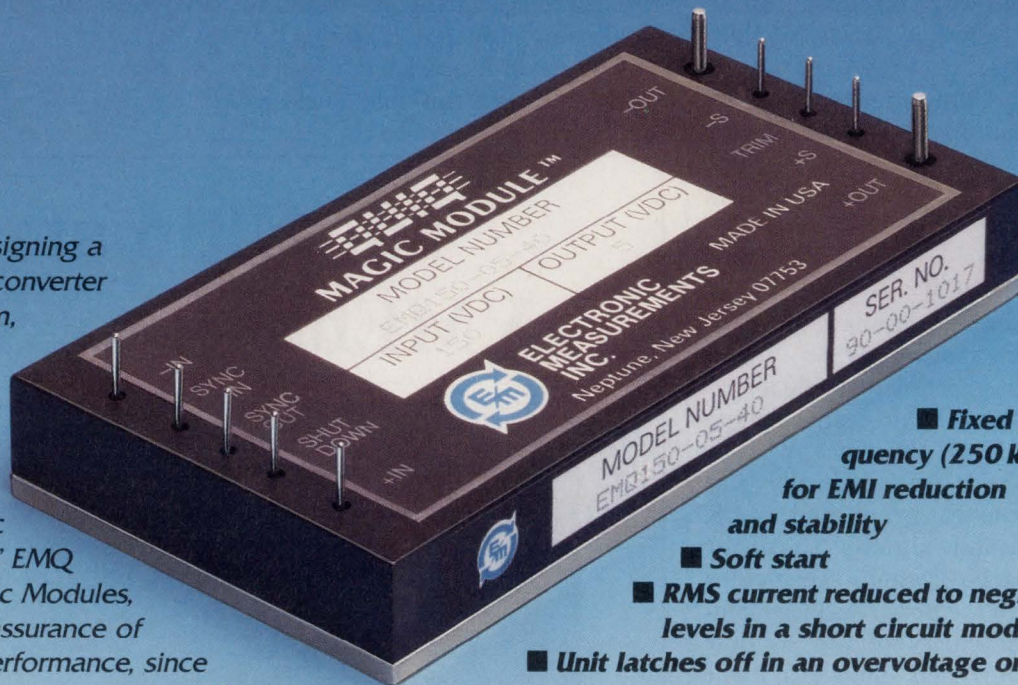
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When designing a DC/DC converter into your system, you want the assurance that a surprise is not going to pop up. With Electronic Measurements' EMQ Series of Magic Modules, you have the assurance of dependable performance, since the design incorporates proven fixed frequency, forward converter technology with current mode control and a nominal frequency of 250 kHz. Another good reason to choose the Magic Module is size. The EMQ Series also offers the highest power rating for any self-contained 5-V output, high density, board mounted unit available.

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- **Forward converter topology for proven reliability**



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- **Unit latches off in an overvoltage or over temperature condition**
- **Operates in the N+1 Mode for system redundancy**
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- **Thermal characteristics allow for PC board mount with only natural convection up to 50 watts**

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THE MAGIC MODULE brochure is yours for the asking. If you need information immediately, call TOLL FREE 1-800-631-4298 (In NJ, HI, AL and Canada 908-922-9300).



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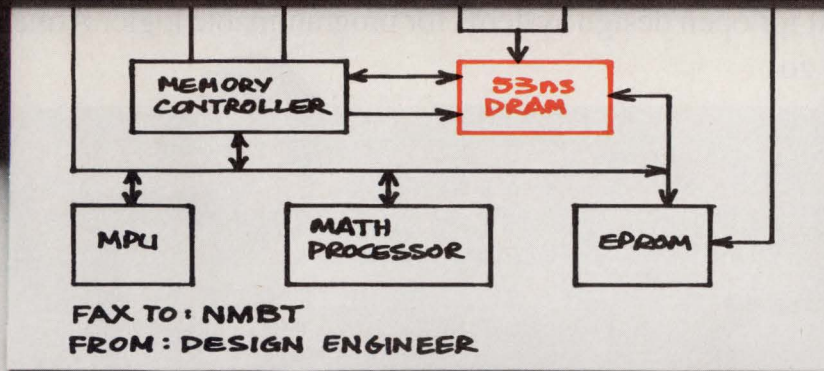
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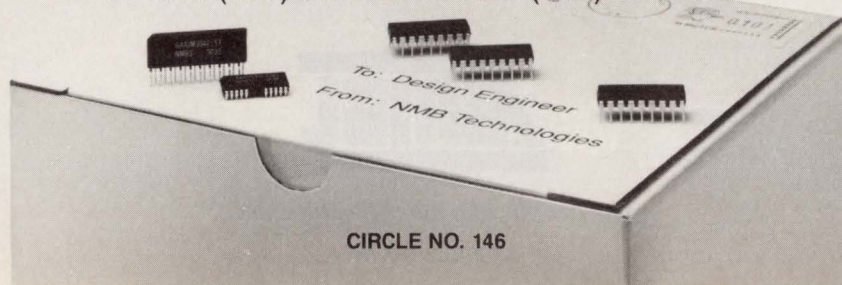
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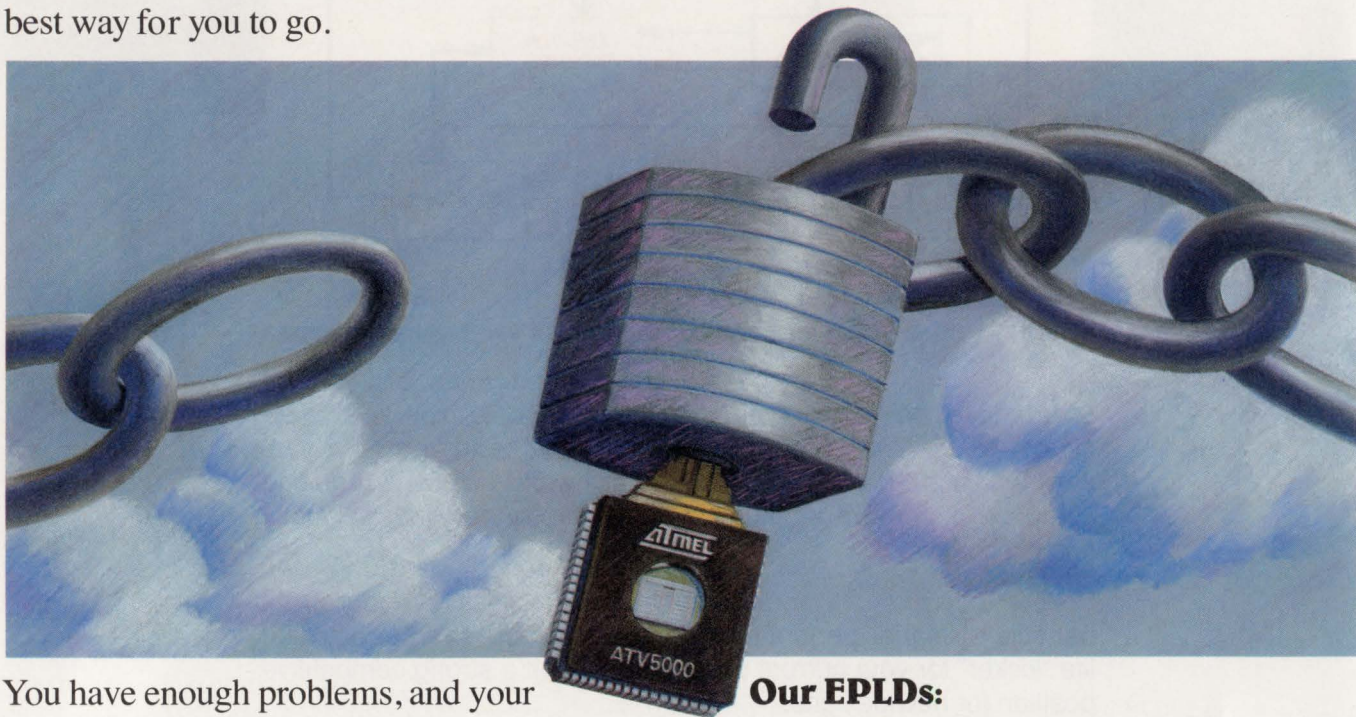
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Device	Gate Count	System Frequency	Pins	Availability
AT22V10	500	80MHz	24	NOW
ATV750	750	55MHz	24	NOW
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ATV5000	5000	50MHz	68	NOW

So, if you want programmable logic that meets the spec no matter what your application, call Atmel, the people who think that open design systems are the only way to go.

DECLARE YOUR INDEPENDENCE!



The people who make the difference.

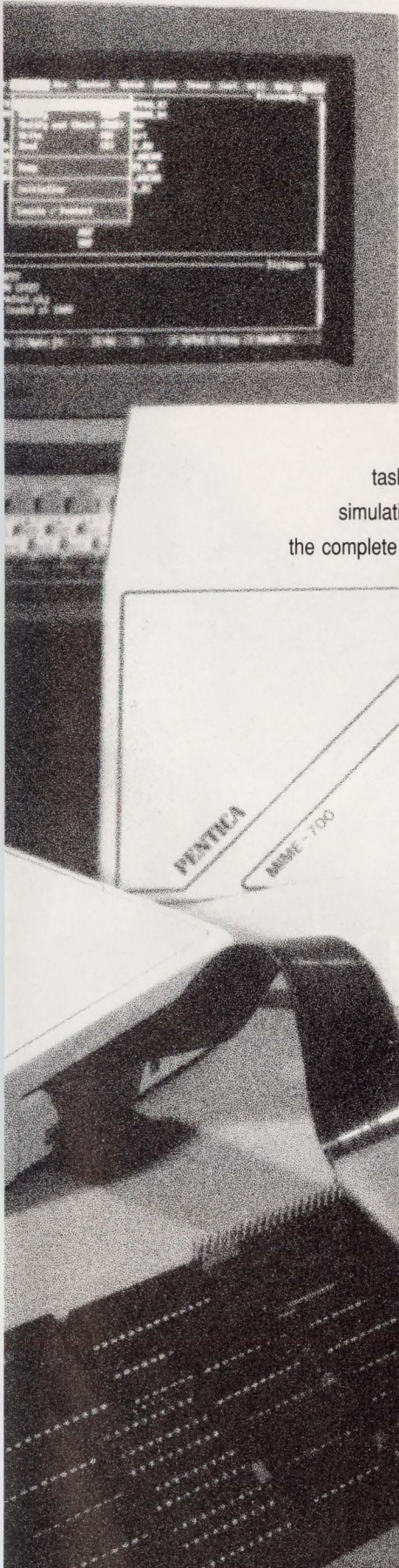
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CIRCLE NO. 147

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Tel. (408) 441-0311
FAX (408) 436-4200

EDN June 20, 1991



Development Puzzles Solved by Pentica

(Part One of a Design Dictionary)

Trace Buffer n. Digital memory part of in-circuit emulator. Used to store a sequence of microprocessor addresses, data and status for post execution analysis.

The Puzzle: You have developed a complex real time system with interrupt driven multi-tasking software. Each of the software tasks has been debugged. No problems show up under simulation. The hardware designer, insisting his part works great, has gone on vacation. However, the complete system crashes after anything between 10 minutes and 3 hours.

The Solution: Use an ICE with a trace buffer large enough to capture the events which lead to the crash. Complex and sequential triggering of the trace may be required to stop tracing events which occur after the crash--an 8k word trace buffer could overflow in under 2ms. Pre-filtering of trace cycles can be used to extend the capture time. The ability to re-trigger the trace allows critical areas to be traced and then disregarded if the crash does not happen. Comprehensive search facilities are needed to analyse large amounts of data.


Pentica's MIME-700 in-circuit emulator offers these features and more, while Pentica prides itself on its superior technical service and support. Write or phone and let's start solving your next development puzzle!

PENTICA IN-CIRCUIT EMULATORS

We love to solve puzzles!

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Wokingham, Berkshire
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(0734) 792101
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Cambridge, MA 02139
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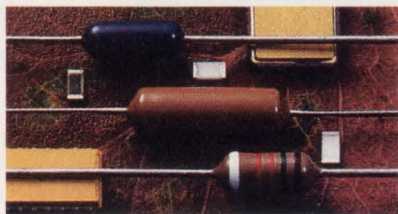
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NEW PRODUCTS

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Magnetics Tester

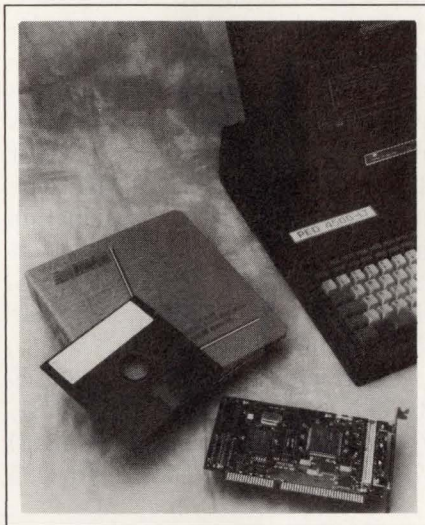
- Measures turns and turns ratio
- Checks for open and shorted coils and improper air gaps

The 2000 Coil Test and Magnetics Design system is a benchtop instrument that, among other things, measures transformer turns ratios and numbers of turns in coil and transformer windings. It also checks for open coils, shorted turns, and improper air gaps. Measured values appear on a large LCD. The unit measures turns ratios with $\pm 0.1\%$ accuracy. The system's general-purpose application block is suited to testing a variety of mag-



netic devices. Custom application blocks offer further flexibility. \$3350.

Influx Corp., 106 Billings St., Sharon, MA 02067. Phone (617) 784-5606. **Circle No. 381**



SCSI Bus Emulator

- Runs on IBM PC/ATs and compatible computers
- Emulates host CPU or peripheral devices

Emulating either a host CPU or a peripheral device, the PED-4500 SCSI bus emulator lets you debug SCSI systems operating asynchronously to 5M bytes/sec or synchronously to 6.25M bytes/sec. The emulator supports the SCSI II standard in the host and target modes. A target-description library contains information on target devices.

You can create custom libraries that include unique commands, messages, and data structures. Debugging occurs either interactively or under program control. \$1295 to \$1995.

Pacific Electro Data, 14 Hughes, Suite B205, Irvine, CA 92718. Phone (800) 676-2468; in CA, (714) 770-3244. FAX (714) 770-7281.

Circle No. 382

SCSI Disk-Drive Tester

- Evaluates single-ended drives per ANSI SCSI-1 and -2
- Sends results either to printer or 3 1/2-in. disk

The portable PR4050 SCSI disk-drive tester evaluates single-ended hard disks that conform to the ANSI SCSI-1 and -2 definitions. The tester sends results to a printer via a parallel port or can store them on an IBM PC-compatible 3 1/2-in. floppy disk. The unit incorporates an editor with which you can create command-descriptor blocks and custom test routines. The command blocks and routines reside in 64k bytes of nonvolatile RAM; you can also transfer them to a floppy disk.



The unit, which includes an RS-232C interface, can supply power to the drive under test. \$12,850.

Pioneer Research, 1745 Berkeley St., Santa Monica, CA 90404. Phone (800) 223-1745; in CA, (800) 848-1745. FAX (213) 453-3929.

Circle No. 383

SCSI Bus Analyzer/Emulator

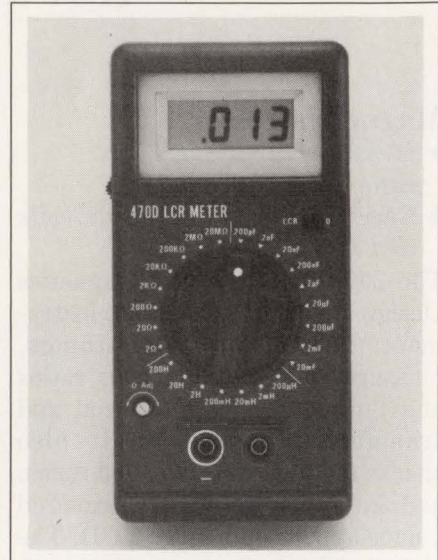
- Supports SCSI-1 and -2
 - Traces bus activity to 10 MHz
- The 202/F SCSI bus analyzer/emulator supports the SCSI-1 and -2 standards. It can trace bus activity at speeds to 10 MHz. The unit, which works with an external terminal or PC, provides a 128k-frame trace memory with 40-nsec time-



stamp resolution and recording of four request-acknowledge edges per bus transaction. It can test both initiators and targets. \$6950 to \$11,800.

Ancot Corp, 115 Constitution Dr, Menlo Park, CA 94025. Phone (415) 322-5322. FAX (415) 322-0455.

Circle No. 384



Handheld LCR Meter

- Resolves 2000 counts
- Measures 20,000 μF , 200H, and 20 M Ω

The 470D handheld, battery-powered, 3½-digit meter measures inductance, capacitance, and resistance. It provides seven L ranges from 200 μH to 200H; nine C ranges from 200 pF to 20,000 μF , and eight R ranges from 2 Ω to 20 M Ω . The unit also measures the dissipation factor (D) of capacitors. It tests at 120 Hz and 1 kHz. The vendor supplies probes for surface-mountable components. \$249.

American Reliance Inc, 9952 E Baldwin Pl, El Monte, CA 91731. Phone (818) 575-5110. FAX (818) 575-0801. Circle No. 385


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- Superior pulse transformer technology applied to advanced telecom magnetics.
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ISDN S-Interface transformers comply with CCITT L.430. UL recognized. BABT approved. Single or dual packages.

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Emulator For i960 μP s

- Supports the i960SA and SB
- Emulates at speeds to 16 MHz

The ICE-960SB in-circuit emulator supports the vendor's i960 SA and i960 SB processors at speeds to 16 MHz. The IBM PC-hosted unit has a color interface. It lets you set breakpoints on execution addresses, instruction types, bus read or write accesses, and data values. The emulator also lets you monitor and rapidly update program variables. The trace buffer holds 1024 frames. Communication between

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- Universal Programmer supports virtually all devices on the market and features: True Self Calibration/Diagnostics, Programmable Current Generator, Part Insertion Sensing, Continuity Test, True State Machine Testing, Handler Interface; Adapters for Gang, PLCC, etc...



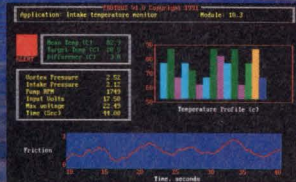
PROGRAMMER



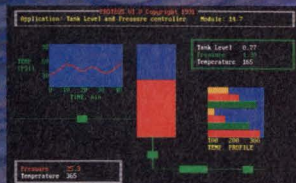
ALGORITHM DEVELOPMENT



DATA LOGGER



CONTROLLER



POWER SUPPLY

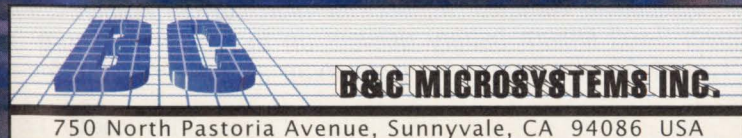


TESTER



from \$995

[Basic Unit with Programming Adapter supporting up to 40 pin devices; Detachable computer shown in photo not included.]



(408) 730-5511
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CIRCLE NO. 150

DISTRIBUTORS WANTED

the emulator and host can be via Ethernet, RS-232C or RS-432. The software lets you customize the command set. With a change in the pod and software, the unit supports the i960 KB. \$16,495.

Intel Corp, Box 58065, Santa Clara, CA 95052. Phone (800) 874-6825; in CA, (602) 554-2388. FAX (503) 696-4633. **Circle No. 386**

800M-Sample/Sec Logic Oscilloscope

- Resolves repetitive events to 50 psec
- Uses same probes for logic analysis and waveform viewing

The 16482 high-speed probe works with the vendor's Model 1600 logic oscilloscope. The instrument, a logic timing analyzer expandable to 160 channels, displays analog waveforms instead of the usual binary data. The probe, a small box with

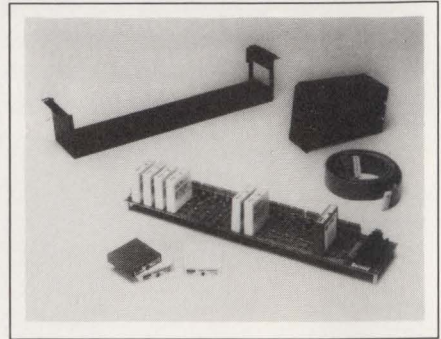
two probe tips, connects to one of the scope's 8-channel input groups. The probe samples single-shot data on two channels at 800M samples/sec or on four channels at 400M samples/sec. You can use more probes to capture additional high-speed signals. With repetitive signals, the scope's effective timing resolution becomes 50 psec and its vertical resolution also improves. Bandwidth for all signals is 350 MHz. \$750. Delivery, 45 days ARO.

Outlook Technology Inc, 200 E Hacienda Ave, Campbell, CA 95008. Phone (408) 374-2990. TLX 350479. **Circle No. 387**

Analog Signal Conditioners

- Offer 1500V continuous common-mode isolation
- Inputs withstand 240V ac

The PCI-5B line of analog signal-



conditioning modules conforms to a de facto industry standard. The family consists of 29 products. The conditioners, which are encapsulated in hard epoxy, are physically interchangeable with one another and plug into panels that accommodate multiple units. The modules accept inputs from such sources as 4- to 20-mA current loops, resistance-temperature detectors, and thermocouples. The thermocouple conditioners provide linearization and cold-junction compensation. In-



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TEST & MEASUREMENT INSTRUMENTS

put-to-output ohmic isolation withstands 1500V continuously. Inputs withstand 240V ac. From \$150.

Intelligent Instrumentation/Burr-Brown, 1141 W Grant Rd, MS 131, Tucson, AZ 85705. Phone (602) 623-9801. FAX (602) 623-8965.

Circle No. 388

Capacitance Meter

- Measures at 1 MHz
- Provides $\pm 100V$ programmable bias

The Model 7200 capacitance meter measures capacitance at 1 MHz in the presence of parallel loss. The instrument computes and displays parallel resistance, dissipation, quality factor (Q), equivalent series resistance, and equivalent series capacitance, as well as the difference (in percentage or pF) of a measured capacitance from a preselected value. The unit measures capaci-

tance from 0 to 2000 pF and conductance from 0 to 2000 μS . You can program the test levels from 15 to 100 mV. An optional internal supply produces bias voltages in the $\pm 100V$ range. The unit, which you can control via the IEEE-488 bus, will display these voltages or external bias levels in the $\pm 200V$ range. \$4795. Delivery, four to six weeks ARO.

Boonton Electronics Corp, 791 Route 10, Randolph, NJ 07896. Phone (201) 584-1077.

Circle No. 389

Remote Diagnostic Software

- Uses digital scopes and phone lines
- Runs on an IBM PC at central repair depot

PM 9372 Telegnostics software permits remote troubleshooting and

fault diagnosis on complex electronic equipment. The software uses a digital storage oscilloscope (DSO) at a remote site linked by telephone lines to an IBM PC at a central repair depot. The software sends setups and reference waveforms to the remote scope and downloads captured waveforms for display on a second DSO—this one at the repair depot. Messages can be transmitted to a technician at the remote site and displayed on the screen of his DSO. The software supports the vendors' DSOs that have RS-232C ports. \$200.

John Fluke Mfg Co Inc, Box 9090, Everett, WA 98206. Phone (800) 443-5853; in WA, (206) 356-5671.

Circle No. 390

Philips Test and Measurement, Bldg TQIII-4, 5600 MD, Eindhoven, The Netherlands. Phone local office.

Circle No. 391



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CIRCLE NO. 155

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Futaba is the leading global supplier of vacuum fluorescent displays and modules. We have the capability, technology, and market knowledge to provide you with the most cost effective display system tailored to your specific application.

Futaba's high brightness fluorescent display products range from simple numeric and dot matrix displays to large multi-color graphic panels.

TECHNICAL SUPPORT

Futaba engineers have a broad range of application experience including automotive, point of sale, appliance, medical, and instrumentation products. They are ready to assist you in optimizing your display system design.

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Futaba's state-of-the-art SMD manufacturing facility in Schaumburg, Illinois provides local service, JIT delivery, and reinforces its commitment to supply the North American market.

QUALITY

Futaba's number one commitment is supplying products having the highest level of quality. Quality begins with the initial design and is controlled throughout the manufacturing process by using SPC and having well trained and motivated employees.

Futaba is dedicated to the principal of continuous improvement and always strives to provide the highest level of customer satisfaction.

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Electronic Instrument Panel to J.I. CASE Tractors.



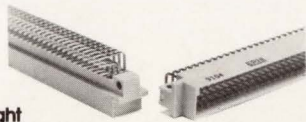
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Appliance Control Display.



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FAX 708-884-1635
CIRCLE NO. 153

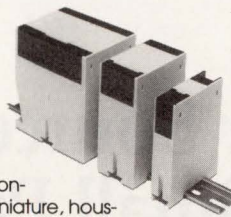


Right Angle Pressfit

Cost-efficient ERNI Press pressfit connectors for the Eurocard sub-assembly:

- Type B & C male versions and Type Q & R female versions
- Universal press-in technique for thru hole or SMT board designs
- Gas tight connection withstands corrosion and vibration

ERNI



LDG Miniature Housing Enclosures

Multi-use, non-metallic, miniature, housing enclosures:

- Internal PCB mount terminal blocks
- Multiple connecting options (from 12 up to 70)
- DIN-rail mountable

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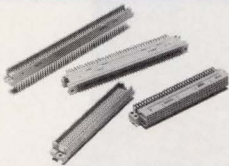


Application Specific DIN Connectors

PCB process compatibility and application specific options from ERNI:

- SMT DIN Connectors
- PCB hold-down clips
- Variable pin lengths for early-make-late-break connections for "Zap-proofing"

ERNI



Extended DIN High I/O Connectors

Extended DIN connectors including 120, 128, and 150 positions:

- Cost-efficient inverse (reverse) style two-piece DIN connectors
- 3 row (120 & 150) or 4 row (128) versions
- Solder, wirewrap, & pressfit options

ERNI



PCB Edgecard Connectors

ERNI Edgecard connectors featuring the latest configurations and options:

- Connectors for every bus type like STD, Multi(+ S-100), Q, Apple II, XT & AT, Microchannel, and more
- Complete range of high-density .050" types
- Extensive options in contact style, type of termination, mounting, and plating

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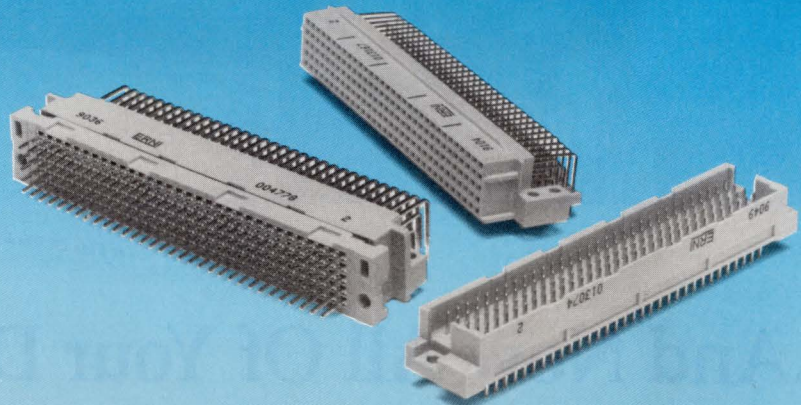
.050" SMC

Introducing ERNI's .050" SMC two-piece high-density connector system:

- Perpendicular (daughter to mother board), stacking (parallel or mezzanine), and side-to-side (edge-to-edge) mating configurations
- Anti-twist contact design assures longer life and reliability
- Built-in keying plug cavity for easy plug installation

ERNI

IN THE SPACE OF THIS 7"x10" AD YOU COULD MAKE 4,640 CONNECTIONS.



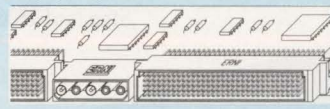
Introducing The New High-Density 160 Connector From ERNI.

An interesting addition to DIN 41612, the new Type E and TE 160 pin connectors meet today's design needs for high-density connectors. So pack it in: 160 connections in an array of 5 rows of 32 contacts in 3.740" x .618" — Type E 160 external dimensions (Yes, 29 connectors could physically fit in this ad space!).

Spec it where miniaturization requires more contacts in less space. Take advantage of its flexibility through either standard (E) or inverse (TE) styles. Choose your connections: dip solder, wire wrap, or compliant press-fit. More choices: 3 quality grades with either gold- or tin-plated termination areas — providing design options to withstand up to 500 mat-

ing cycles. Add in ERNI's Eurocard Center connector and you have a multifunctional signal + coax + power + fiber optic system or 362 signal connections all possible on a double Eurocard. The selections list seems endless when you include backplane shrouds, coding strips, pressfit tooling, and more.

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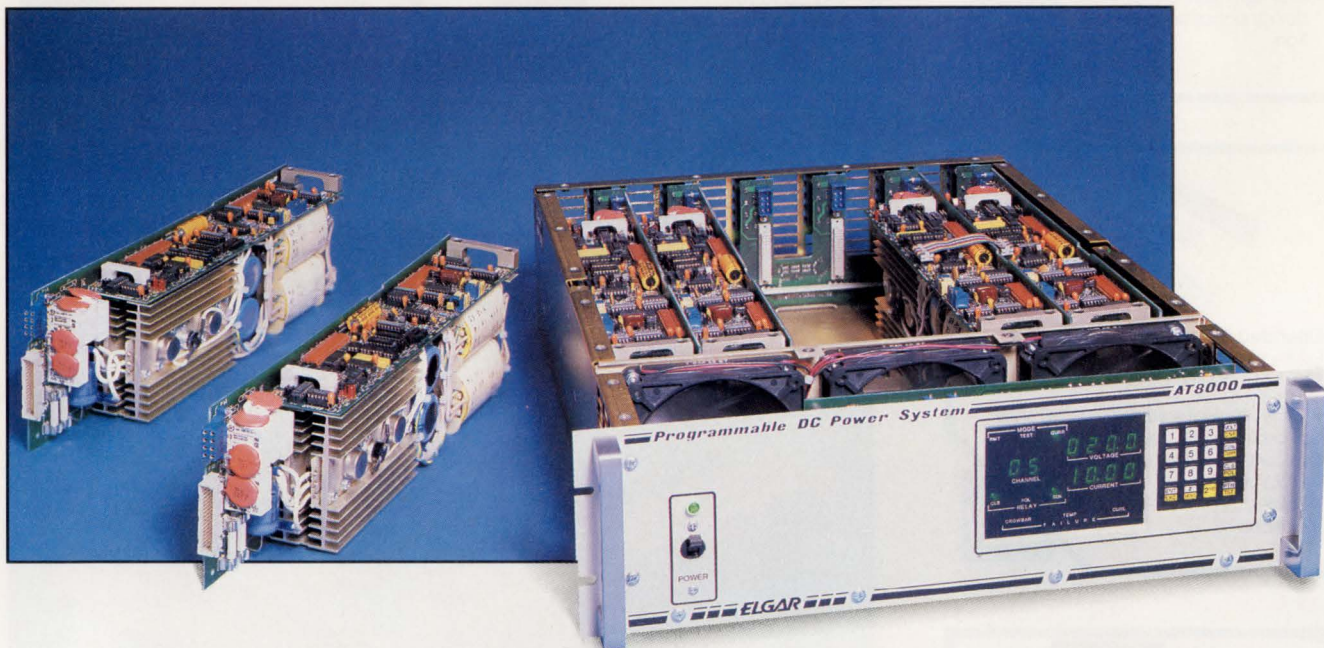
160 pins + Eurocard Center connectors = Increased I/O with power, coax, &/or fiberoptics

So get with ERNI and get to know more about us and about all the possibilities and advantages of the 160 series. Phone or write to: ERNI Components;

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Phone (804) 794-6367;
FAX (804) 379-2109.

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Introducing Programmable DC Loads

The new AT8000A Programmable Loads are based on the new "instrument on a card" technology that became so popular with our AT8000 Power Sources. The AT8000A can house up to six 300W loads in one 5¼ inch drawer. By paralleling modules, you can increase the load of any single channel up to 1800W. And by adding expansion chassis, you can increase the system up to 16 channels!

Now You Can Meet Virtually Any ATE DC Source or Load Requirement

You'll appreciate the fact that the Elgar DC Loads and Power Sources can be used in any combination in the same AT8000A chassis. Plus, the option of Built-In Test (BIT) allows you to perform self testing and measurement of system parameters through the bus. The AT8000A can also include an embedded TMA and accept CIIL commands per MATE Interface Standard 28067633.

Elgar Power Is Preferred the World Over.

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For more information about how the AT8000A Power Sources and Loads can help you solve your ATE testing needs, call:

1 (800) 73-ELGAR

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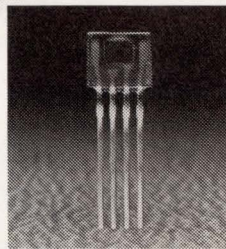


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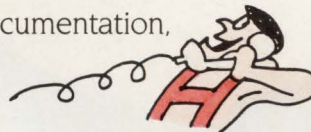
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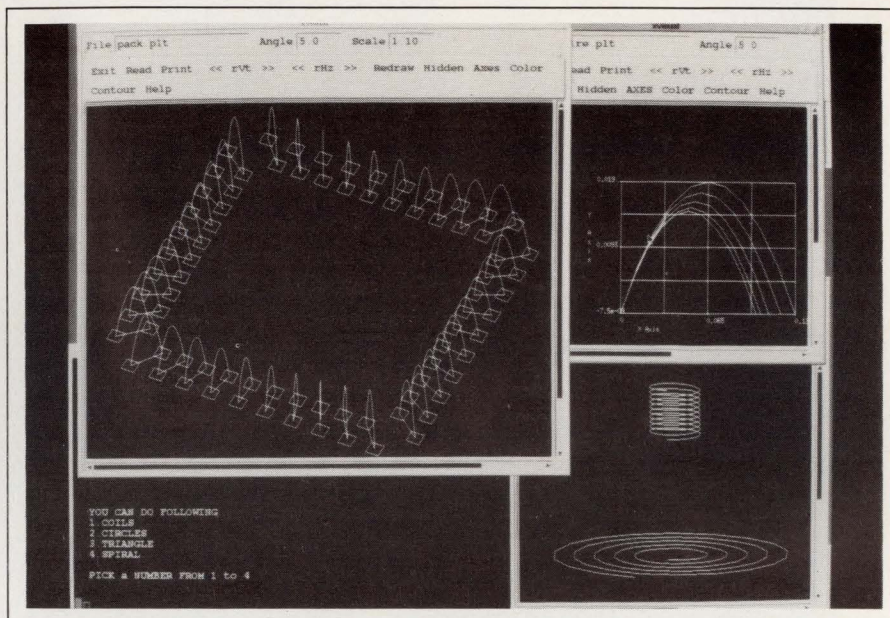
NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

Self- and Mutual-Inductance Simulator

- Calculates inductance in non-magnetic media
- Handles IC package leads, bond-wires, and all coil types

Henry is a 3-D inductance simulator that calculates self and mutual inductance of complex structures in nonmagnetic media. The program uses the complete mathematical definitions of inductance and mutual inductance, which are based on the energy stored or shared between magnetic circuits. Use of these definitions removes any limitations imposed by nonmagnetic media. Typical applications are for the calculation of inductances in IC package leads, ground planes, vias, traces, and any kind of coils. The simulator does not require a ground-plane structure in order to calculate the solution. The program runs on Sun-



3, Sun-4, and Sun SPARCstation computers under SunOS, or on Mips workstations under Unix. From \$40,000.

OEA International Inc, 3235 Kifer Rd, Suite 300, Santa Clara, CA 95051. Phone (408) 738-5972.

Circle No. 392

C Functions For Geometric Computations And Display

- Geometric computations include NURBs
- Compatible with AutoCAD

Development System Release 10 CAD/CAM Developer's Kit/2D is a library of C functions for geometric computations, display, and DXF data exchange. Geometric computation functions include construction, rotation, scaling, mirroring, intersection and trimming of lines, and NURBs (Non-Uniform Rational B-Splines). The display functions allow you to set up one or more viewports and to pan or zoom; these functions are adaptable to popular graphics libraries. The DXF data-exchange functions allow you to read and write ASCII and binary files, and are compatible with all AutoCAD release 10 entity-types. The CAD/CAM Developer's Kit/2D is a subset of the vendor's full 3-D Developer's Kit, and you can up-

grade to the 3-D version at any time. The personal edition, for in-house use only, \$399; upgrade to 3-D edition, \$600, professional edition upgrade, which provides royalty-free distribution rights, \$500.

Building Block Software Inc, Box 1373, Somerville, MA 02144. Phone (617) 628-5217.

Circle No. 393

Simulation Model Bank

- Includes both architectural and structural models
- Compatible with Zycad's hardware simulation accelerator

The Model Bank service is founded on joint agreements with leading manufacturers to market both architectural and structural simulation models of microprocessors and logic modules. The structural models are based on existing hardware and allow users to construct simulation models of complete systems

and subsystems for use in prefabrication verification. The architectural models, such as those of the Mips R3000, R3010, and R4000 devices, allow you to design systems with processors that are not yet available in silicon. All of the models are compatible with Zycad's hardware simulation accelerator, and yield better accuracy than suboptimum techniques such as behavioral model or in-circuit emulation. Subscription to Model Bank, from \$5000.

Protocol, 500 International Dr, Mount Olive, NJ 07828. Phone (201) 347-7900. FAX (201) 347-8525.

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Design Aid For Filters

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- Active version 2.07 is a software package for the analysis and design



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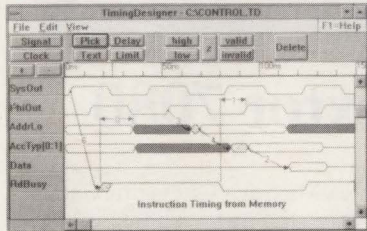
¹6801,6301, 68HC11, 6809, 68000/10,68020/30/40, 68332,32000 • ²MSDOS, MAC-MPW, VAX VMS/ULTRIX, DECSTATION, IBM RS6000, SUN3, SUN4, APOLLO, 386 UNIX SYSTEM V
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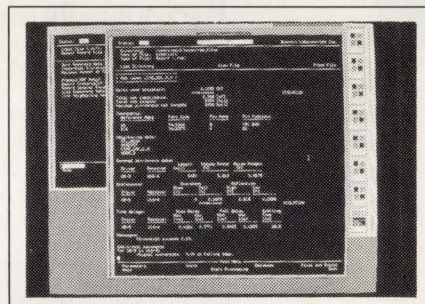
CIRCLE NO. 165

EDN June 20, 1991

CAE & SOFTWARE

of active filters that runs on IBM PCs and compatibles. You can design Butterworth, Chebyshev, Bessel, Real-Pole, Gaussian, Linear-Phase, or Elliptic filters. You can define a filter by its polynomial transfer function, by its poles and zeros, or by its gain. Conversely, for a filter that you've already designed, based on a specific topology and populated with specified component values, the software will display the ideal characteristics, along with Monte Carlo sweeps of the filter's performance. You can now output hard copy of Hercules, CGA, and EGA graphics directly to dot-matrix and laser printers. When you're building a filter with standard-value components that significantly shift the passband/stopband borders away from the design center, a "best combination" feature allows you to change some of these values in such a way as to approach the design center more closely. \$745.

Tatum Labs Inc., 3917 Research Park Dr, Suite B-1, Ann Arbor, MI 48108. Phone (313) 663-8810. FAX (313) 663-3640. **Circle No. 395**



Simulation Tool For Crosstalk Effects

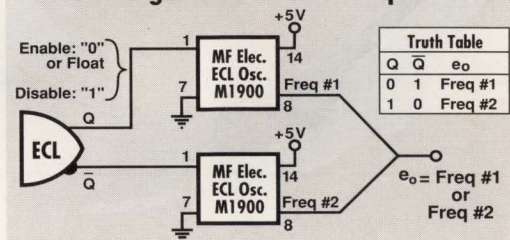
- Reports time delays and functional violations
 - Analyzes crosstalk between nets
- Boardscan version 2.0 is a pc-board screener that calculates both transmission-line signal integrity and crosstalk effects. Input to the screener takes place through an interface file, which is integrated with EDA (electronic design auto-

ECL Oscillators In Standard D.I.P. Are The Industry Standard From 10 to 325 MHz

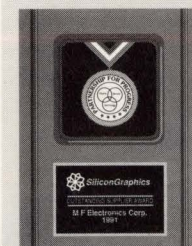


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Enable/Disable Application; How to get one of two frequencies



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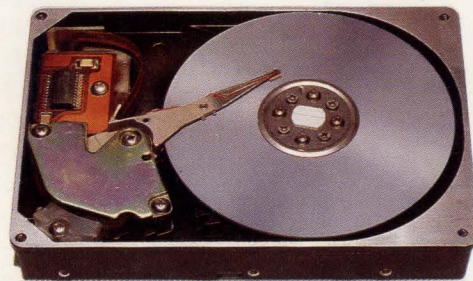
from SiliconGraphics.

CIRCLE NO. 164

MF ELECTRONICS CORP.

10 Commerce Drive
New Rochelle, NY 10801
(914) 576-6570 Fax: (914) 576-6204

Specs for Hard Drivers.



Maxtor 7080

Simplicity of design makes Maxtor's Cheyenne Series inch-high 80MB 7080 disk drive the most reliable in its class. Compare Maxtor's four-head, two-platter design to Seagate's six-head, three-platter design. Fewer moving parts make Maxtor's drives inherently more dependable.

Power consumption is a very low 2.8 watts, making it one of the lowest in the 80MB class. The 7080 is also Novell Labs certified, and is available with either SCSI or AT interface, giving you flexibility for a winning system.

Exceptionally fast 17ms seek time and 32K cache buffer in the new generation inch-high form factor give Maxtor faster data throughput than the competition.

Call and ask about our entire Cheyenne family of disk drives with capacities from 40MB to 130MB. Don't fall for the off-the-wall claims. Give us a shot and we'll prove Maxtor specs can't be matched. **Call your nearest Authorized Maxtor Distributor.**

3.5-inch Disk Drive Spec.	Maxtor 7080A	Seagate 1102A
Seek Time	17 Msec.	19 Msec.
Standard Buffer Size	32K	8K
Form Factor	3.5" x 1"	3.5" x 1.6"
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Circle No. 396

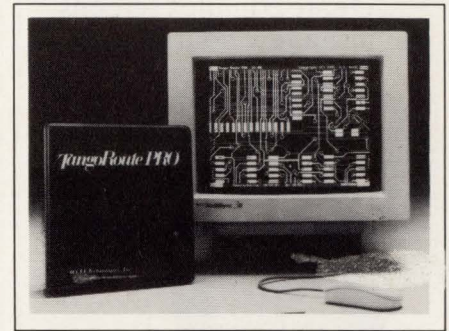
Test-Vector Generator For Timing Simulator

- Converts waveforms to various PLD Test Vector formats
- Lets you customize test-vector formats

Test Vector Generator is a tool for use with the vendor's dV/dt Timing Diagram Accelerator; it lets you convert waveforms generated with dV/dt to various PLD test-vector formats or test vectors into dV/dt waveforms. The program currently supports the following PLD formats: Abel (Data I/O Corp), MacAbel (Capilano), TangoPLD (Accel), OrCAD/PLD (OrCAD Corp), Palasm (Advanced Micro Devices), and Schema PLD (Omation). The test-vector-generator manual provides the necessary file specifications for customizing test-vector format outputs. Test Vector Generator, \$495; dV/dt, from \$695; combined dV/dt with Test Vector Generator, \$995; upgrade for registered users of dV/dt, \$195.

Doctor Design, 5415 Oberlin Dr, San Diego, CA 92121. Phone (619) 457-4545.

Circle No. 397



Enhanced Autorouter

- New Reconstruct algorithm replaces ripup-and-retry
- Multiple passes handle SMDs and wide traces

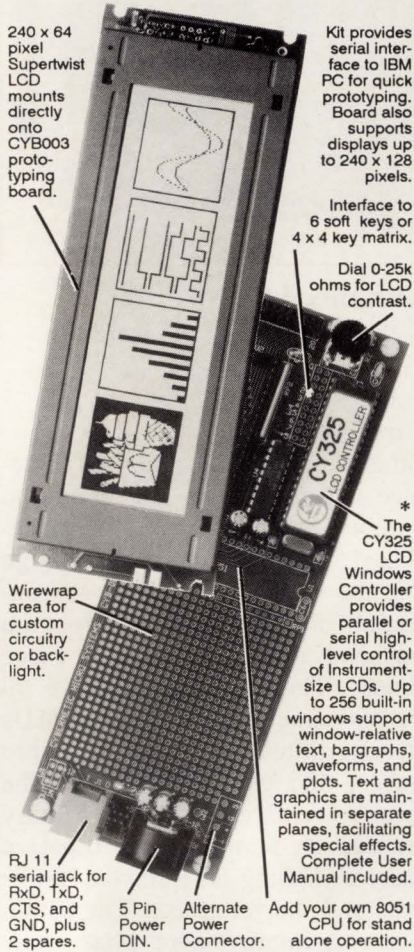
Tango-Route Pro is a high-performance autorouter for IBM PCs and compatibles. The vendor has replaced older ripup-and-retry algorithms with a much faster "reconstruct" algorithm. The program performs multiple passes in three phases. The constructive phase includes special passes for SMDs (storage-module drives), wide traces, and memory routing. The remove-and-replace phase may include as many as 10 iterative passes, yielding fewer layers, fewer vias, and shorter traces. The manufacturing-improvement phase may have as many as 10 manufacturing passes and one final manufacturing pass. The program runs under the vendor's Accel Productivity Interface, a Windows-like, menu-driven interface that helps both the novice and the professional designer. All routing options are selected from menus and dialog boxes; prompts and on-line help provide cues to proper operation at each phase. The program supports both uniform and nonuniform routing grids, allowing virtually any board density and any combination of design rules and pad sizes. Tango-Route Pro interfaces to Tang-PCB and Tango-PCB Plus layout tools. \$5500.

Accel Technologies Inc, 6825 Flanders Dr, San Diego, CA 92121. Phone (619) 554-1000. FAX (619) 554-1019.

Circle No. 398

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Tel: 415-726-3000 • Fax: 415-726-3003

CAE & SOFTWARE

Schematic-Capture Tool

- Compiler increases design size
- Manager controls data flow

Schema III version 3.3 is a schematic-capture tool that runs on IBM PCs and compatibles. New features include an incremental compiling postprocessor, which reduces compilation time and makes disk space the only limitation on design size; full network compatibility; and the Schema Integrated System Manager (SISM), which controls the flow of data through schematic capture, simulation, PLD design, and pc-board layout. It also has new parts-creation routines, parts label-swapping routines, and drawing editor commands. A switch lets you toggle in and out of high-resolution VGA mode. \$495.

Omaton Inc., 801 Presidential Dr, Richardson, TX 75081. Phone (800) 553-9119; in TX, (214) 231-5167. **Circle No. 399**

Virtual-Memory Spice

- Runs 10,000-transistor circuits
- Processor reads Spice output files

RSpice is a virtual-memory version of Spice release 2g6 for use on 80386- and 80486-based PCs. The program determines the amount of extended memory available; as the program runs, if the simulation requires more memory than is available, the program begins swapping to disk and completes the simulation. With as little as 1M byte of extended memory, the program handles circuits with as many as 10,000 transistors. The RGraph graphical postprocessor can read a standard Spice output file from RSpice or any Spice-like simulator, as well as ASCII data files. This program directs hard copy of an RSpice screen plot to HP laser printers. RSpice and RGraph together, \$295; free demo disk available.

RCG Research Inc., Box 509009, Indianapolis, IN 46250. Phone (800) 442-8272; in IN, (317) 877-2244.

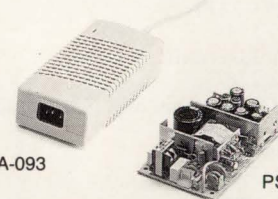
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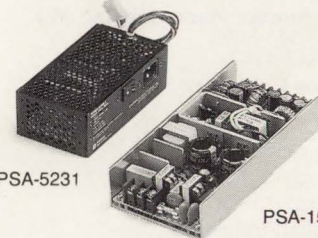
PSA-4031

FOR NOTEBOOK PC

WATTS	MODEL	O/P1	O/P2	O/P3	O/P4	DIMENSION
30W	PSA-093	9.5V/3A				149 x 75 x 45H
	PSA-161	16.5V/1.8A				
	PSA-181	18V/1.65A				
	(7 MODELS)					
40W	PSA-4641	18V/1.4A. CHARGER 1A				166 x 80 x 45
	(3 MODEL)					
50W	PSA-124	12V/4.2				166 x 80 x 54
	PSA-242	24V/2.2A				
	(7 MODELS)					

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	PSA-4005	5V/6A				
	(8 MODELS)					
50W	PSA-5031	5V/5A.	12V/2.5A	-12V/0.5A		160 x 100 x 45
	(3 MODELS)					



PSA-5231

PSA-1500U

WATTS	MODEL	O/P1	O/P2	O/P3	O/P4	DIMENSION
50W	PSA-5231	5V/4A.	12V/2A	-12V/0.5A		144 x 80 x 48

WATTS	MODEL	O/P1	O/P2	O/P3	O/P4	DIMENSION
150W	PSA-1500U	5V/15A	-5V/1A	12V/1A	12V/5A	198 x 97 x 38
	PSA-1503U	5V/30A				
	PSA-1509U	5V/15A	-5V/1A.	-12V/1A	12V/5A	
	(10 MODELS)					
200W	PSA-2041U	5V/25A	-5V/2.5A	-12V/2.5A	12V/5A	203 x 114 x 51
	(3 MODELS)					

SAFETY:

- * ALL APPROVED BY UL/CSA/TUV (PSA-2041 IS IN PROCESS)
- * PSA-40XX AND PSA-50XX APPROVED BY UL/CSA/TUV/VDE



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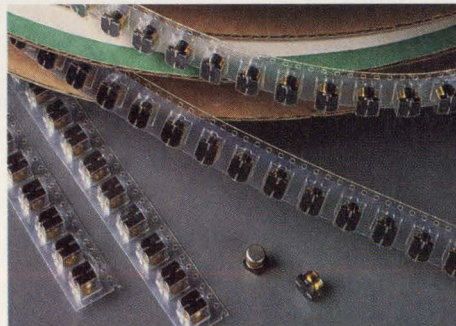
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UZ	5,000 hr. life/6mm ht./4~50V -55~+105°C/0.1~200 μF
WX	2,000 hr. life/5.5mm max. ht. -40~85°C/0.1~220, μF/4~50V
UT	2,000 hr. life/6mm ht. -55~105°C/0.1~100, μF/4~50V
UP	1,000 hr./6mm ht./Non-polarized -40~+105°C/0.1~47 μF 6.3~50V
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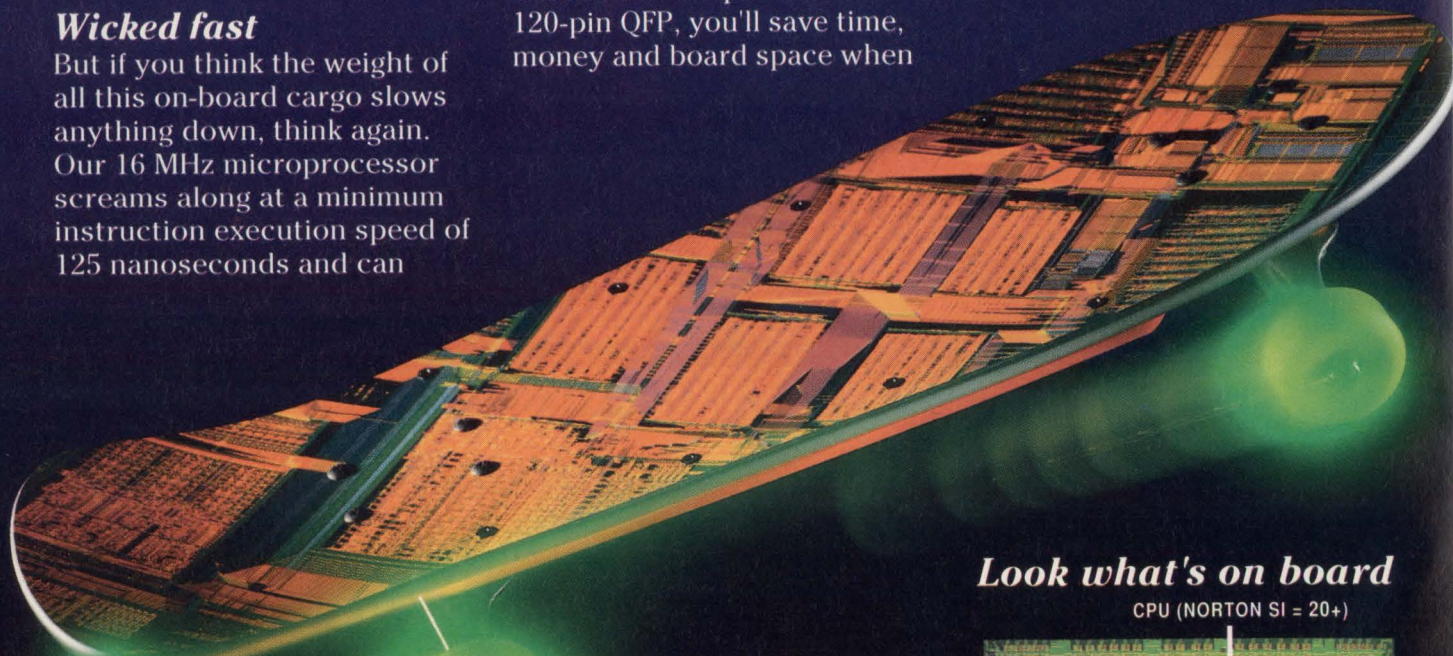
And since you want a ride that's smooth as well as a fast, we offer you the development tools you need. And whether you choose the 132-pin PGA or 120-pin QFP, you'll save time, money and board space when

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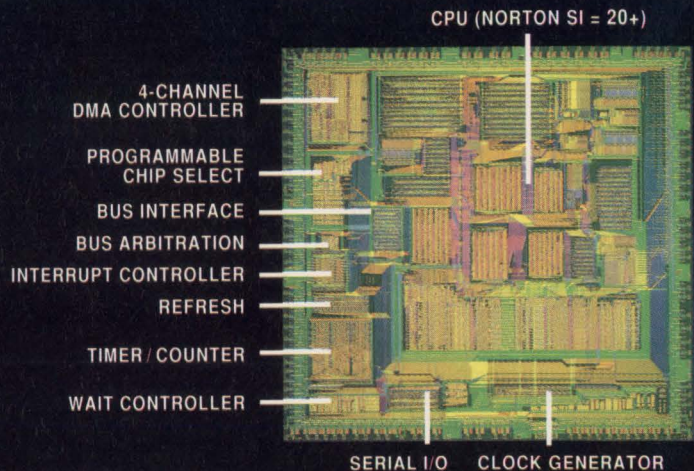
Free Data Book

For your free copy of NEC's 16-bit V-Series Microprocessor Data Book, call 1-800-632-3531. Ask for Info Pack #100.

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P.O. Box 7241
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1-800-632-3531/1-415-965-6158



Look what's on board

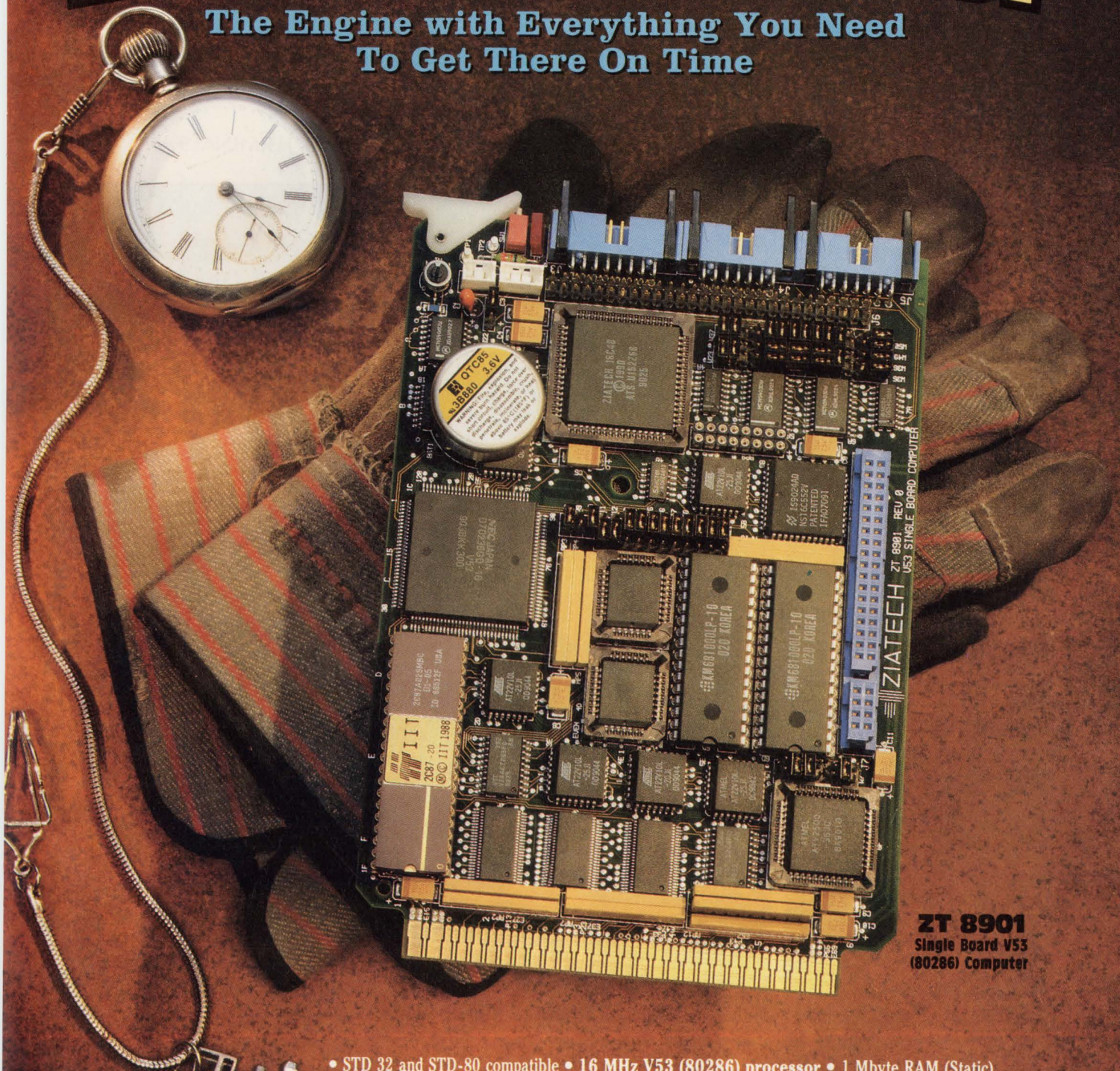


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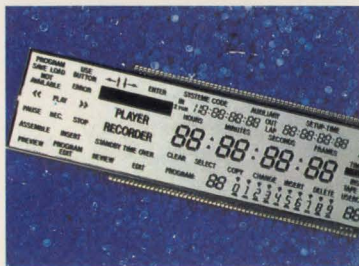
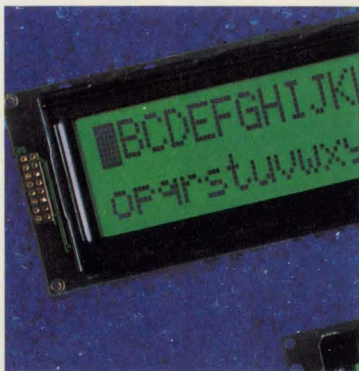
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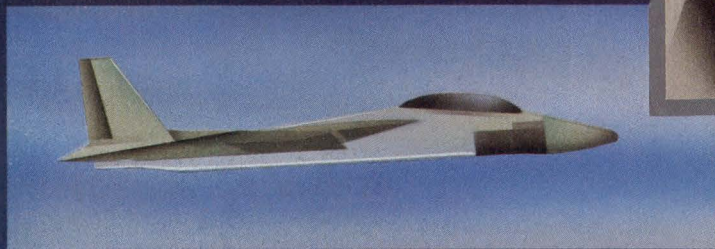
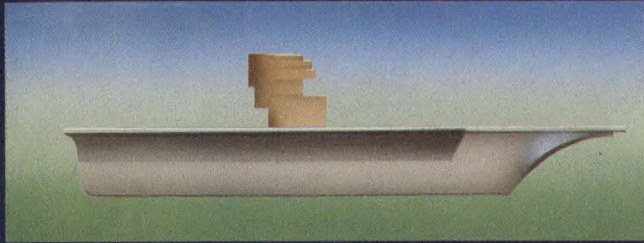
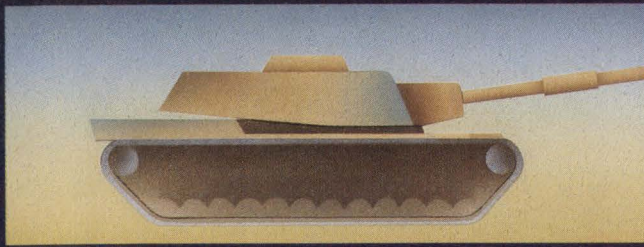
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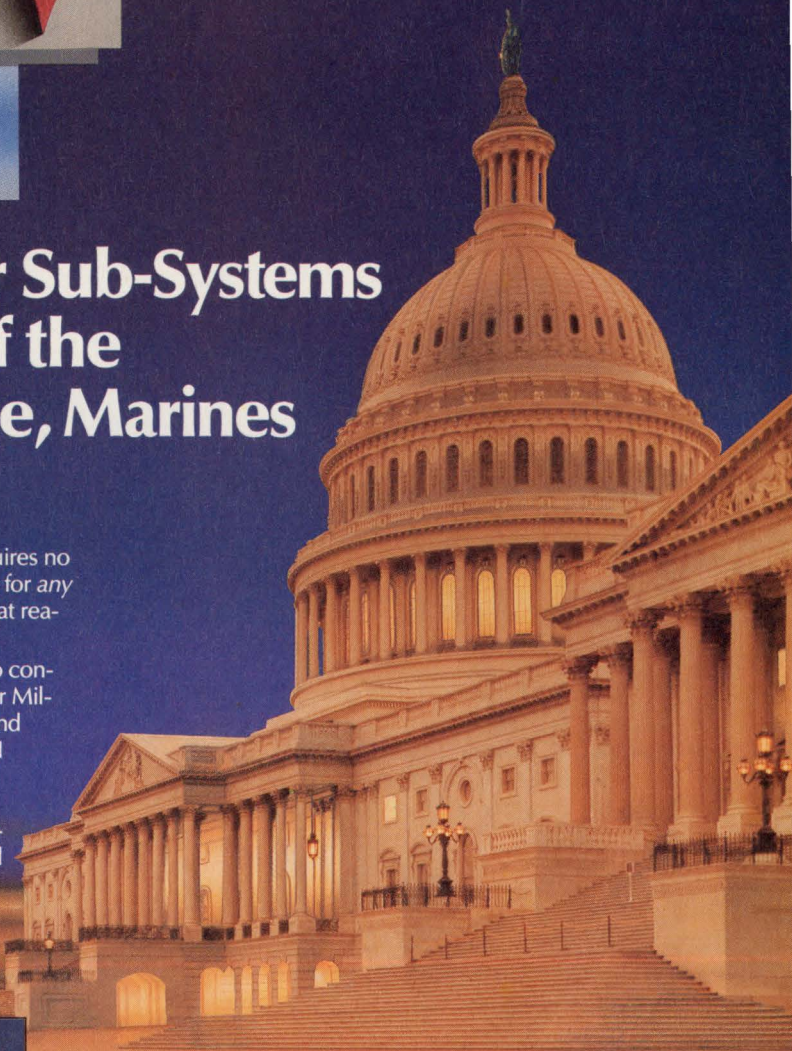


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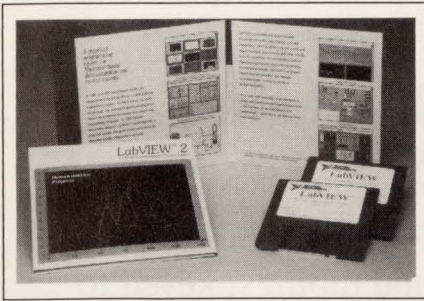
GSA Schedule GS00K89AGS6289

KMS Advanced Products, Inc.

700 KMS Place, Ann Arbor MI 48106-1868

CIRCLE NO. 160

LITERATURE



Labview 2 Demo, Video, And Directory

Three literature choices are available for Labview 2. The 30-minute demonstration disk shows how to develop virtual instruments for data acquisition and provides instrument control applications. The demo requires a Macintosh with 2M bytes of RAM, 2M bytes of available hard-disk space, and a 13-in. monitor. In the 6-minute video tape, *Applications*, users of industrial, laboratory, and educational applications describe how they use the Labview 2 graphical programming software. The video comes in VHS or PAL formats. *Solutions*, a directory of consultant services and products, provides a desktop reference guide to programming or application consultant services in a particular field.

National Instruments Corp., 6504 Bridge Point Pkwy, Austin, TX 78730. **Circle No. 401**

Three Software-Specific Journals

Inside Turbo C++, a 16-pg monthly journal, offers programmers information about polymorphism, inheritance, debugging object hierarchies, and third-party object class libraries. This periodical demonstrates proven techniques with actual examples and code samples that you can download from the vendor's on-line information system. *The DOS Authority* provides tips and techniques for consultants, programmers, and MIS managers. Topics include configuring tips and techniques; in-depth explanations of

documented—and undocumented—DOS commands; a behind-the-scenes look at DOS internal devices; and debug scripts or GWBasic routines that create tools and utilities for enhancing DOS. The third journal, *Inside QuickBasic* provides information about using DOS and BIOS calls, optimizing QuickBasic programs for size and speed, creating intuitive user interfaces, and communicating with serial and parallel devices. 1-year subscriptions: *Inside Turbo++*, \$79; *The DOS Authority*, \$99; *Inside QuickBasic*, \$59.

The Cobb Group, 9420 Bunsen Pkwy, Suite 300, Louisville, KY 40220. **Circle No. 402**

Paper Compares Throughput Of Counters

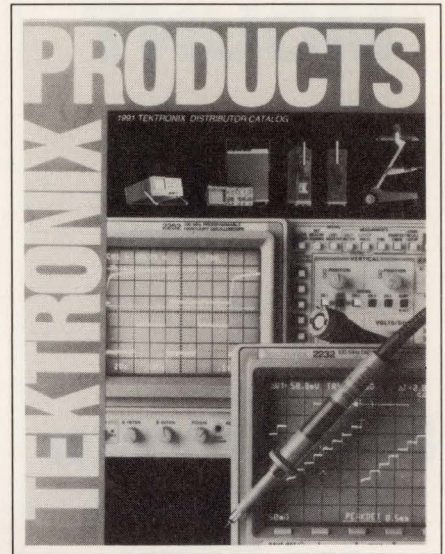
The 4-pg paper, *Optimizing Throughput with HP VXI*, compares the throughput of the HP E1420A VXI universal counter with that of a message-based VXI counter and an HP-IB equivalent of the HP E1420A. A second comparison shows the time savings achieved by using register-based devices. The paper discusses SCPI (Standard Commands for Programmable Instruments), register-based devices, continuous acquisition, and programming of register-based devices and controllers.

Hewlett-Packard, 19310 Pruneridge Ave, Cupertino, CA 95014.

Circle No. 403

Analog And Digital Storage Scopes Cataloged

The 1991 Distributor Products Catalog from Tektronix provides specifications and descriptions of 13 analog and digital-storage oscilloscopes. It also features low-cost bench instruments, including frequency counters, DMMs, and function generators. The 24-pg catalog has selection tables for choosing replacement and accessory probes for



oscilloscopes.

RAG Electronics Inc., 21418 Parthenia St, Canoga Park, CA 91304. **Circle No. 404**



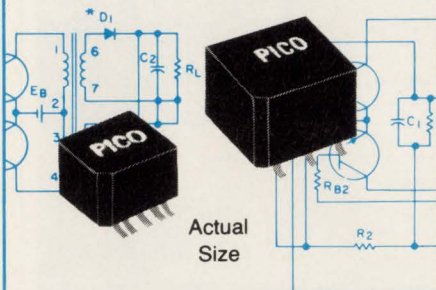
Manual Helps You With Layouts

You can use this technical manual to lay out ASICs. It contains data about each semicustom ASIC, packaging selections, tips on good layout practice, and step-by-step instructions for doing both manual and computer-aided layouts.

Cherry Semiconductor Corp., 2000 South County Trail, East Greenwich, RI 02818.

Circle No. 405

ULTRA-MINIATURE SURFACE MOUNT



DC-DC Converter Transformers and Power Inductors

These units have gull wing construction which is compatible with tube fed automatic placement equipment or pick and place manufacturing techniques. Transformers can be used for self-saturating or linear switching applications. The Inductors are ideal for noise, spike and power filtering applications in Power Supplies, DC-DC Converters and Switching Regulators.

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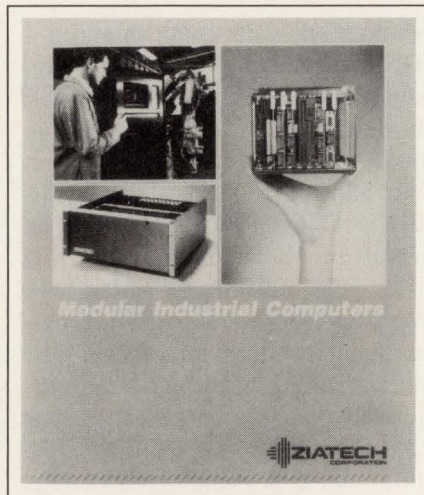
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CIRCLE NO. 178

LITERATURE



Brochure Features Modular Computers

Modular Industrial Computers presents the features and specifications of the vendor's integrated, industrial computers. The 14-pg brochure describes computers for compact, embedded applications, computers for rack-mount applications, and computers for factory applications that require a user interface and NEMA 4/12 specifications.

Ziatech Corp, 3433 Roberto Ct,
San Luis Obispo, CA 93401.

Circle No. 406

Questions And Answers For IEEE-488 systems

Application Note #6, *Troubleshooting IEEE 488 Systems and Software*, is a compilation of frequently asked IEEE system-integration questions in a question-and-answer format. As indicated in the title, the note covers both hardware and software topics. A short IEEE-488 tutorial presents terminology and general operation.

IOtech Inc, 25971 Cannon Rd,
Cleveland, OH 44146.

Circle No. 407

Pamphlet Describes Voltage Suppressors

The 12-pg brochure, *Transient Voltage Suppressors: an Overview of Silicon TVS Devices*, features de-

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The New Ideas Brochure describes and illustrates recent automotive technologies covering moisture sealing, insulating, interconnects with precision overmolding, flexible magnet material and powder and liquid resins. To obtain a copy, contact a 3M Automotive Trades sales representative, or call 1-800-233-3636.



New Ideas Brochure describes dozens of technologies for solving present and future on-vehicle problems.

3M Electrical Specialties Division

Automotive OEM, A130-3N-48

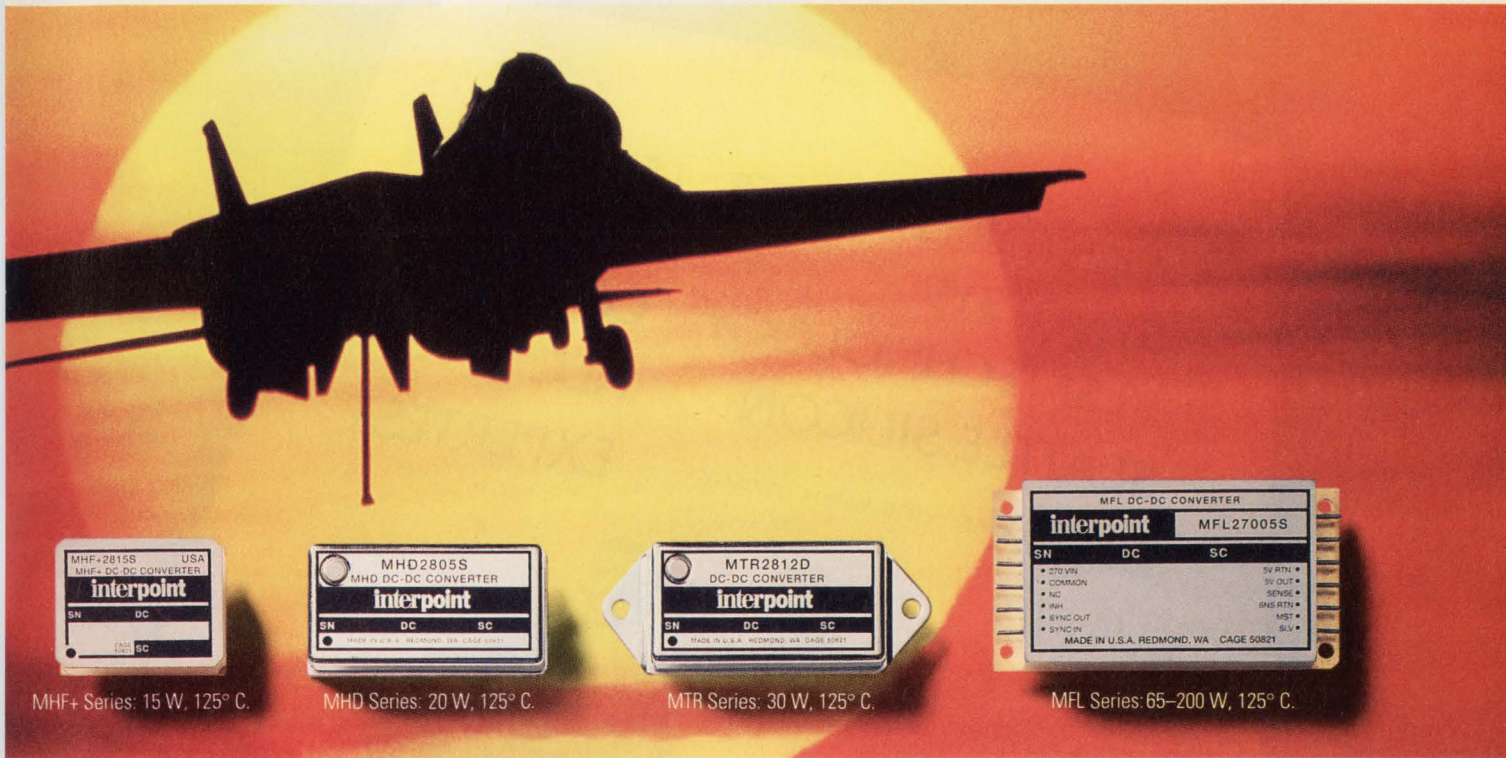
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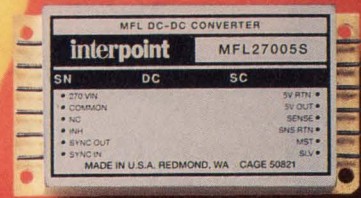
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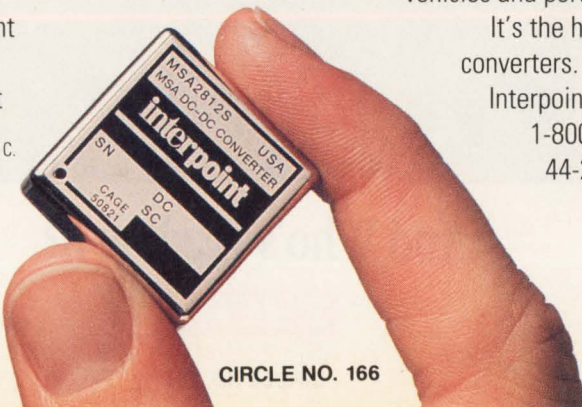
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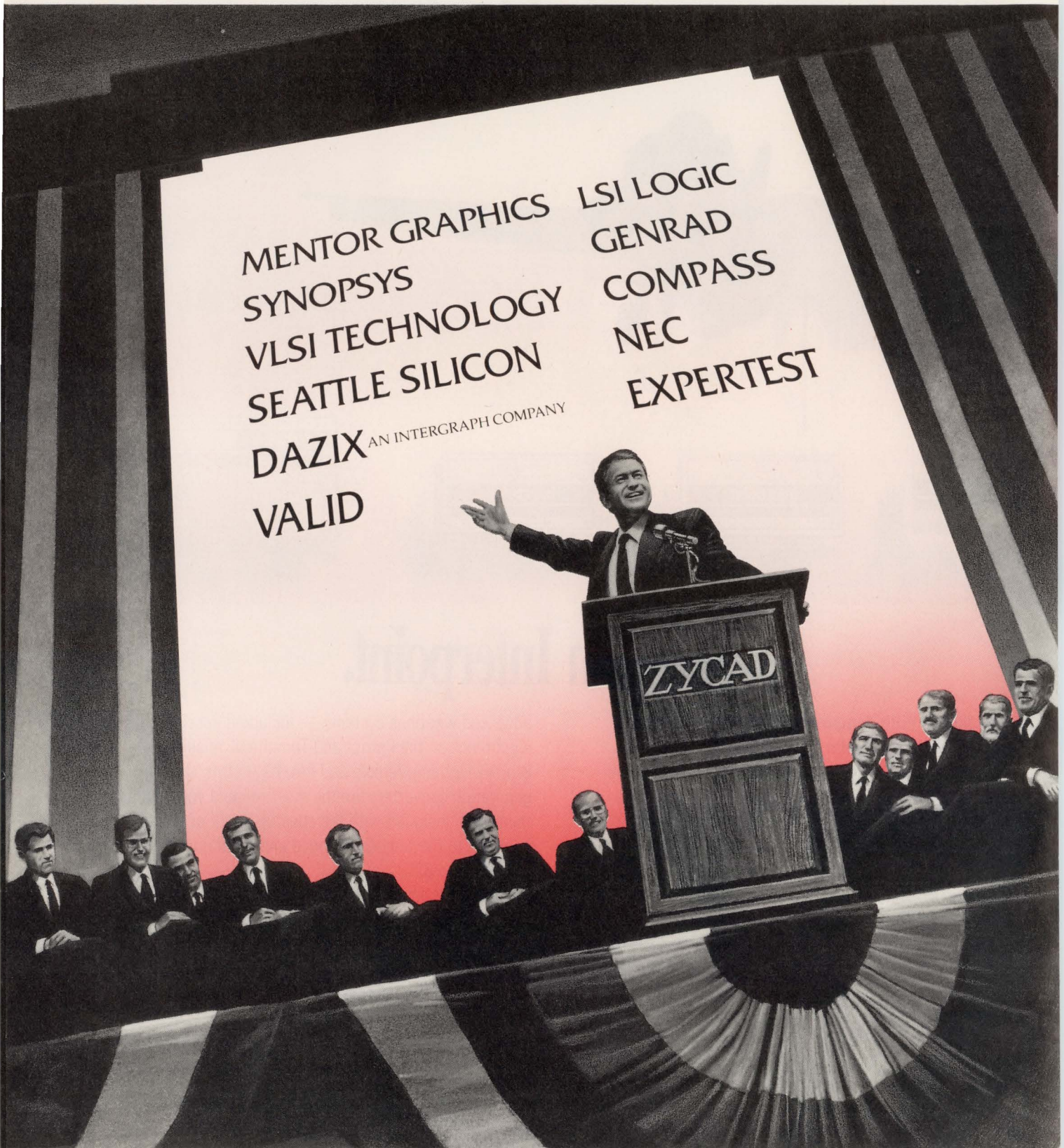
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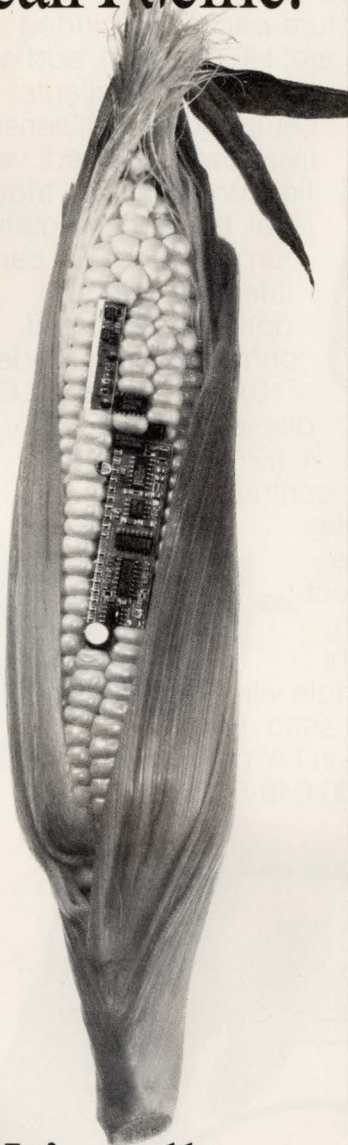
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EDN June 20, 1991

LITERATURE

sign notes, applications, and selection guidelines for circuit protection. A reference guide highlights TAZ (transient absorption zener) products for military and industrial applications. The booklet complements the company's TAZ kits.

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SAW Coupled-Resonator-Filter Applications

The application note AN23, *Capabilities and Applications of SAW Coupled-Resonator (CR) Filters*, covers the theory of CR filter operations and its practical and theoretical performance limits. The note also provides specifications of a SAW CR filter, a comparison of SAW CR filters with other RF filters, and a review of the filter's applications.

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Publication Of DSP Series

This catalog of the 1991 Prentice Hall Signal Processing Series lists texts and reference books on developments in digital signal processing. Three 1991 editions have been published: *Underwater Acoustic System Analysis 2/E*; *Advances in Spectrum Analysis and Array*; and *Digital Signal Analysis 2/E*. Other areas covered include digital image restoration, FFT, digital image processing, adaptive filters, multi-rate DSP, acoustic waves, and advanced topics in signal processing. The catalog contains blurbs about each book and provides two indices—one under author/title and the other under title/author.

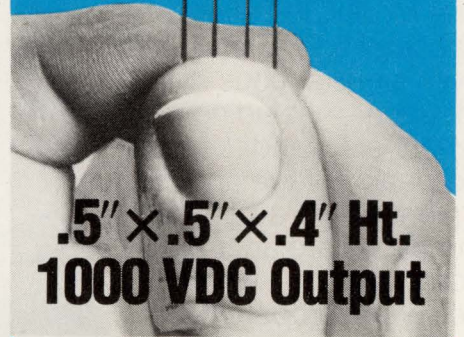
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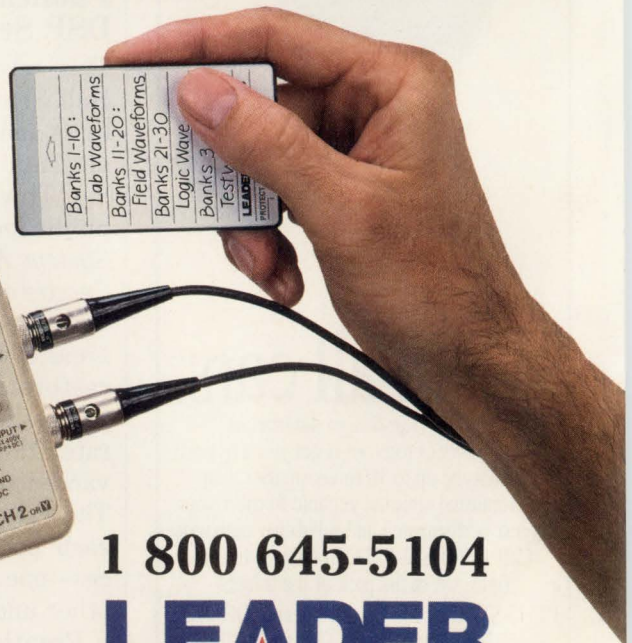
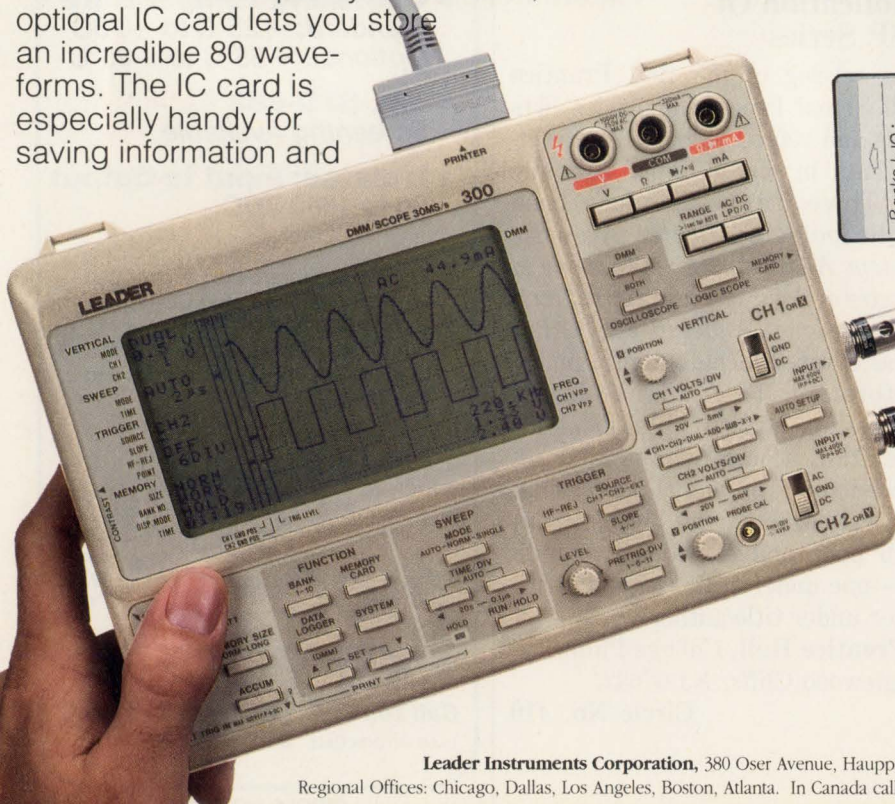
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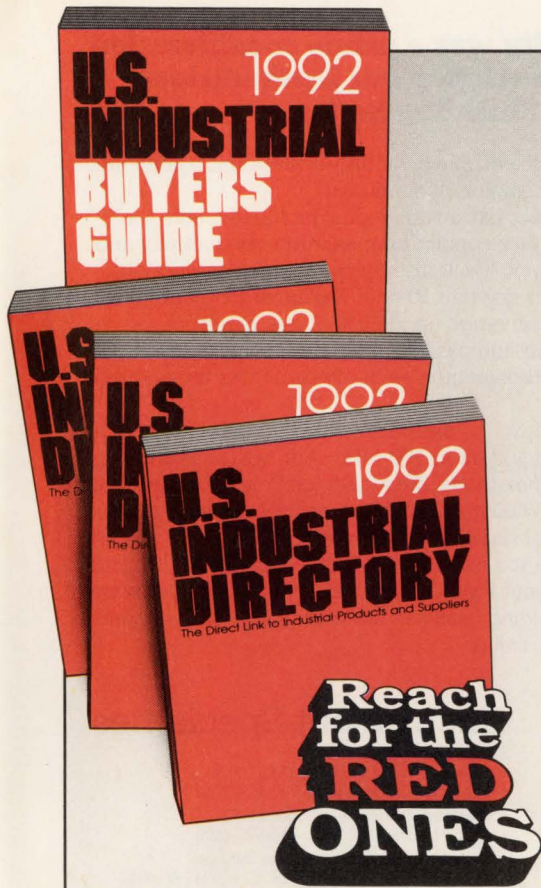
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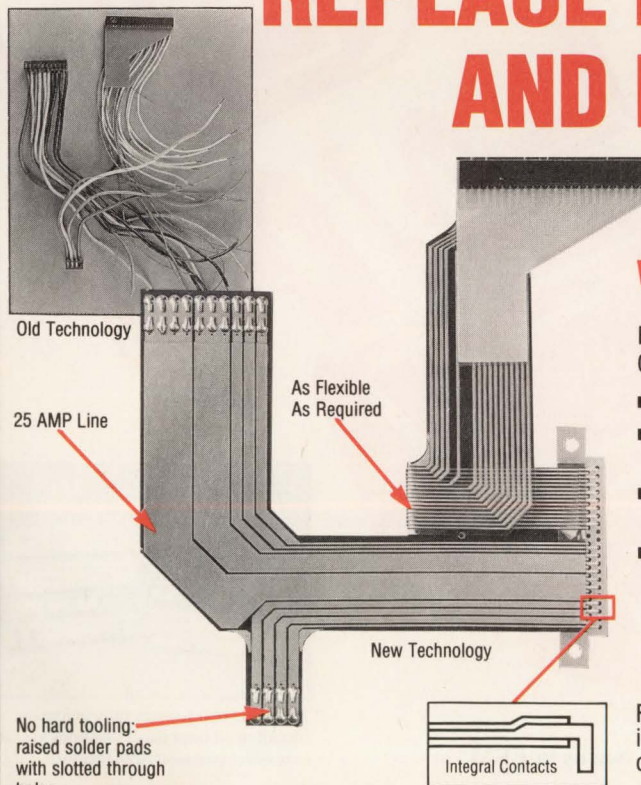
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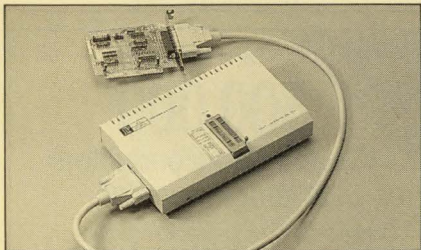


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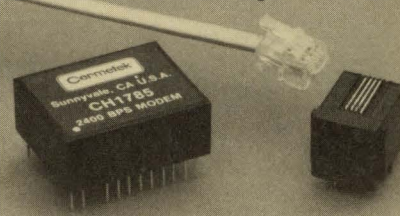


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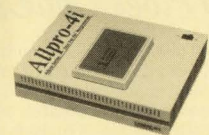


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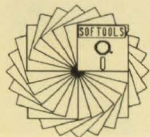
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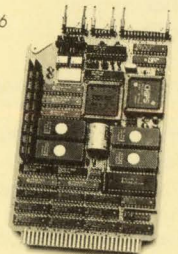
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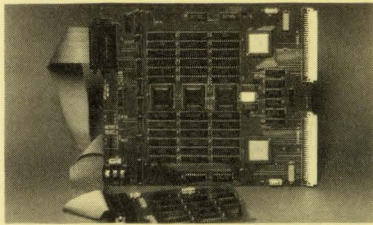
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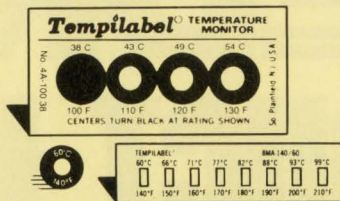
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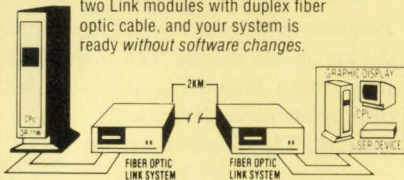
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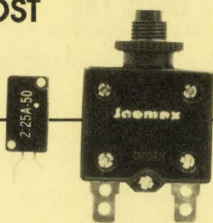
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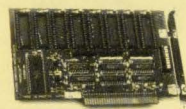
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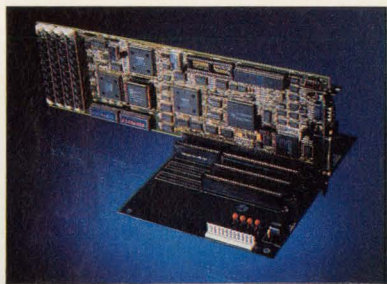
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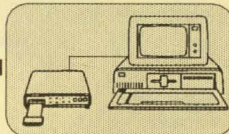
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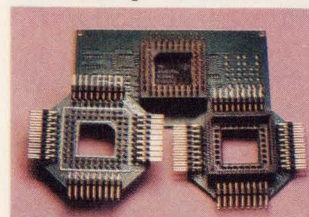
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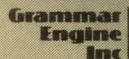
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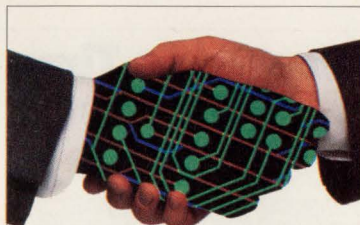
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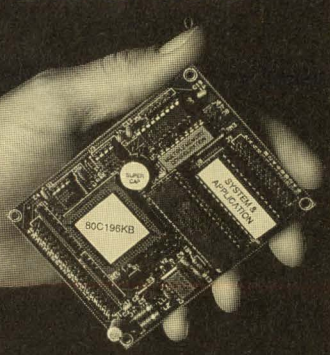


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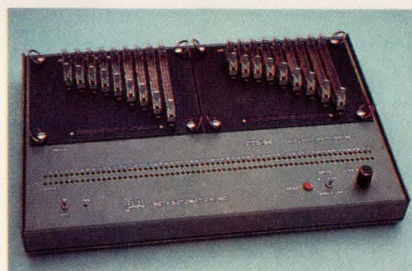


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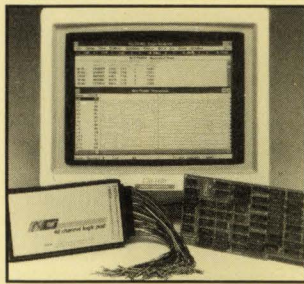
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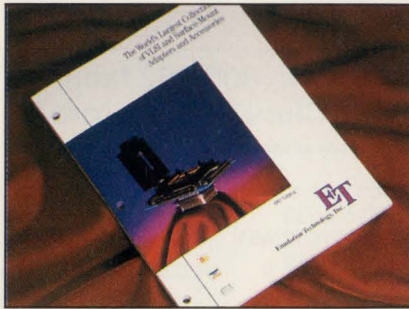
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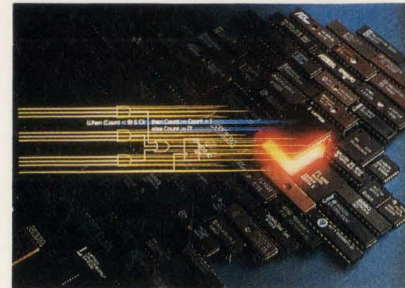
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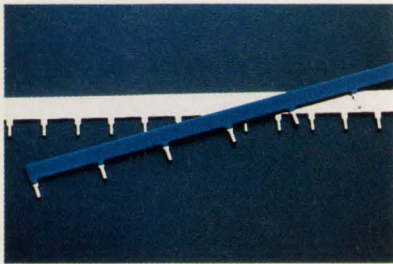
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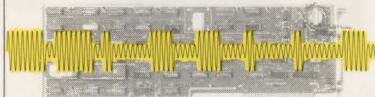
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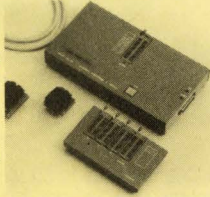
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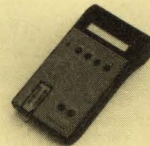
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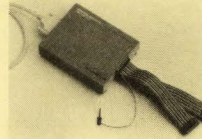
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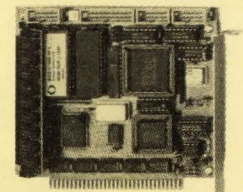
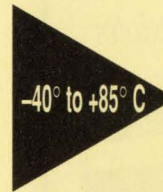
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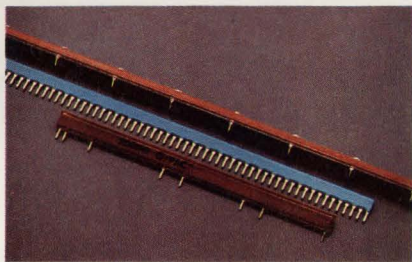


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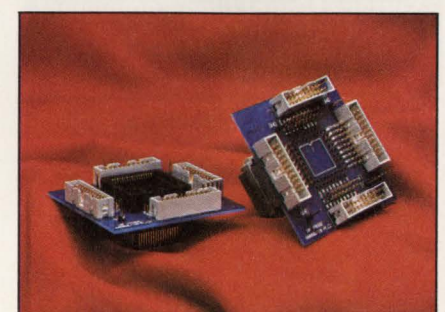
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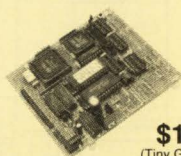
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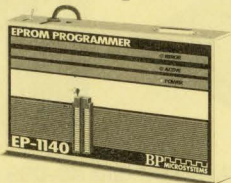
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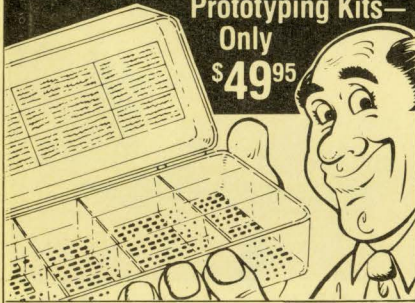
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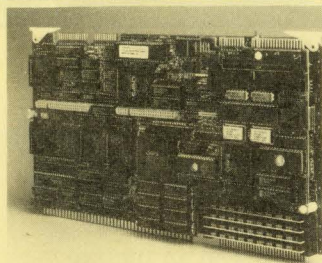


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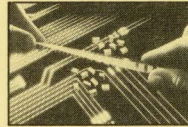
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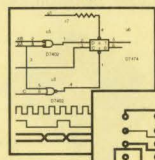
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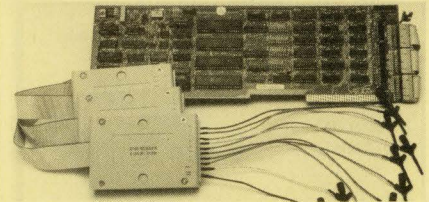
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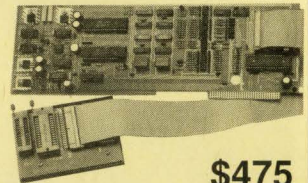
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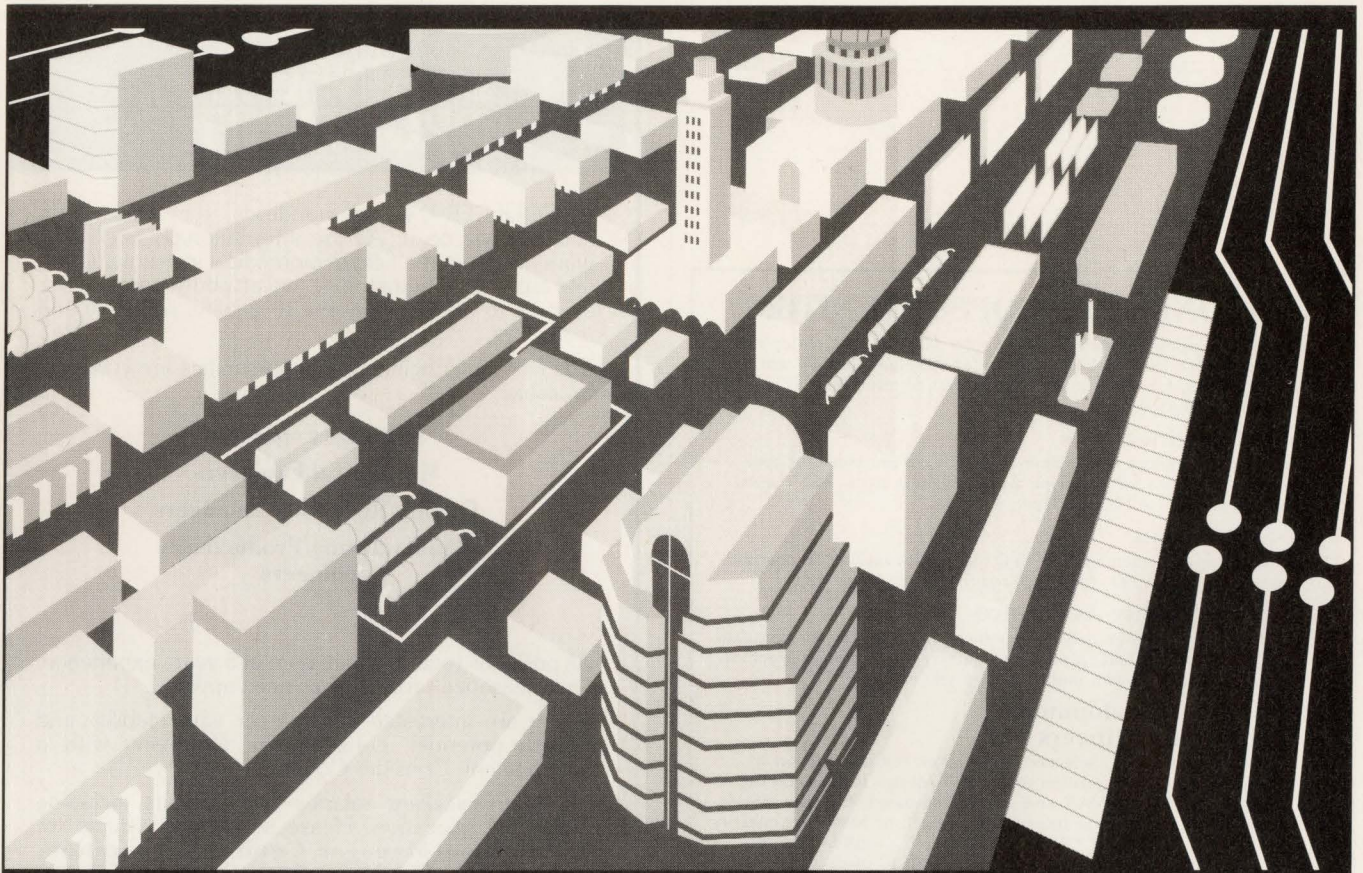
Issue	Issue Date	Ad Deadline	Editorial Emphasis
Magazine Edition	July 18	June 26	Product Showcase—Volume II • Test & Measurement, Computer Peripherals • Components, CAE/ASICs •
News Edition	July 25	July 5	ICs & Semiconductors, Peripherals**, Regional Profile: Massachusetts**
Magazine Edition	Aug. 5	July 11	CAE • ASICs, Test & Measurement • Computers & Peripherals • Technical Article Database
News Edition	Aug. 8	July 19	CAE, Datacom**
Magazine Edition	Aug. 19	July 25	Military Electronics Special Issue, Image Processing • Ultra High Speed ICs/ASICs • Computer Peripherals, Software •
News Edition	Aug. 22	Aug. 2	Peripherals/Components, Test & Measurement**, Regional Profile: Idaho, Colorado, Utah**
Magazine Edition	Sept. 2	Aug. 8	ASICs Special Issue, Semicustom ICs • CAE, Packaging • ICs & Semiconductors Data Converters
News Edition	Sept. 5	Aug. 16	Military Electronics Special Issue, Computer Architectures, Defense Electronics**
Magazine Edition	Sept. 16	Aug. 21	DSP/Microprocessors, ICs & Semiconductors, CAE/ASICs, Environmental Engineering • Software
News Edition	Sept. 19	Aug. 29	RISC/ICs, Computers**, Regional Profile: Florida**
Magazine Edition	Oct. 1	Sept. 5	Computers & Peripherals/Networks, DSP Chip Directory • ICs & Semiconductors/Memory Technology, Instrumentation
News Edition	Oct. 3	Sept. 13	ICs & Semiconductors, Multimedia**
Magazine Edition	Oct. 10	Sept. 19	Test & Measurement Special Issue, Oscilloscopes, VXI Board Directory • CAE/ASICs, Sensors & Transducers •
News Edition	Oct. 17	Sept. 27	ATE/Board & IC Testing, Artificial Intelligence**, Regional Profile: New Mexico & Arizona**
Magazine Edition	Oct. 24	Oct. 3	Telecommunications ICs, Graphics & Video Circuits, Computers & Peripherals, Software, Wescon Preview Issue
Magazine Edition	Nov. 7	Oct. 17	High Performance DSPs • CAE/ASICs, Computers & Peripherals/Communications, Software, Wescon Show Issue
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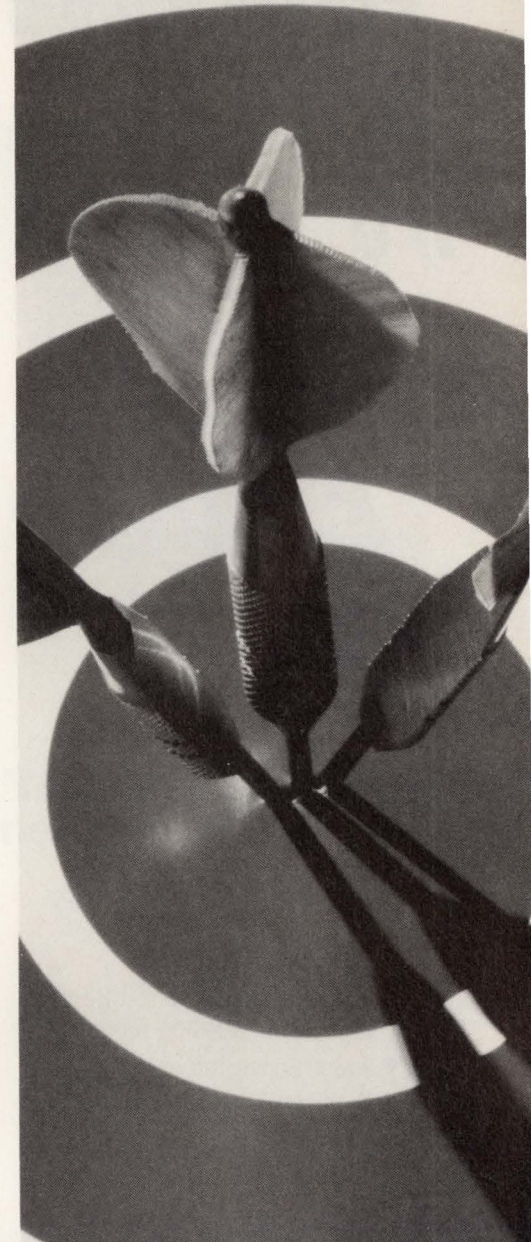
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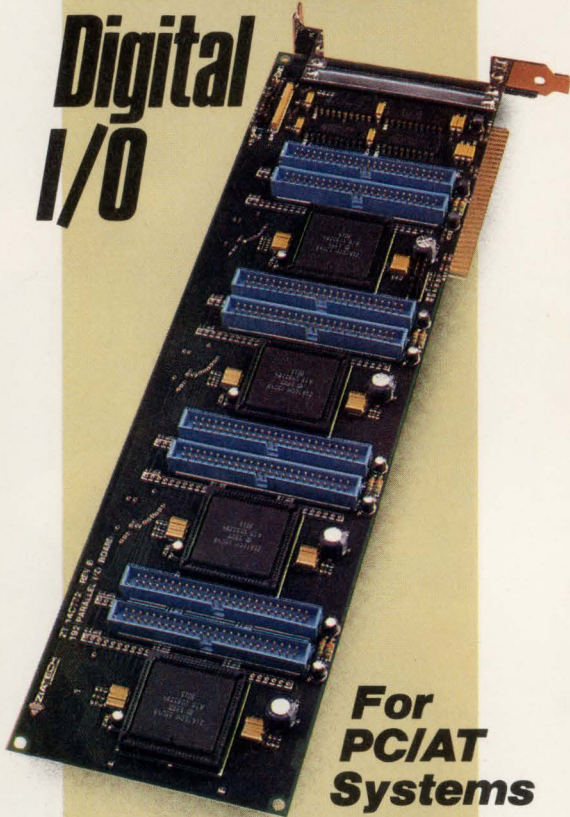
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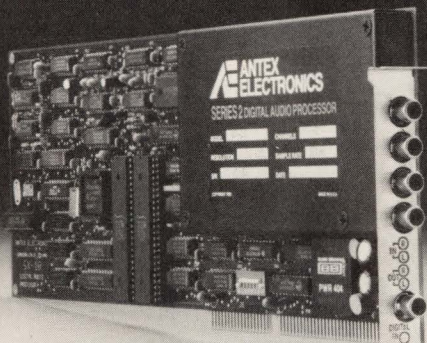
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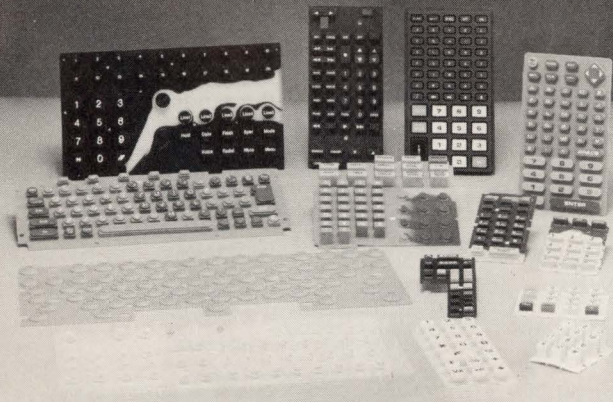
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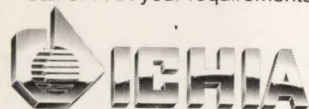


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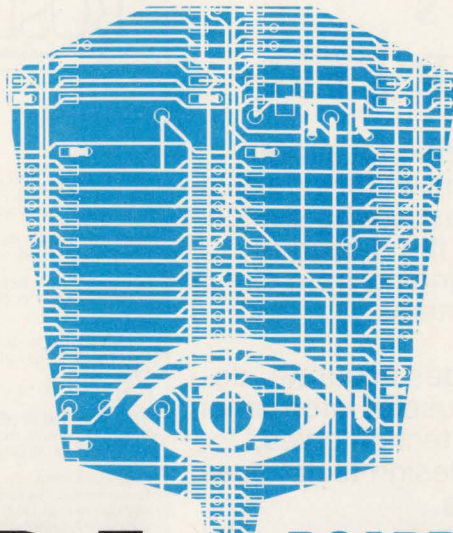


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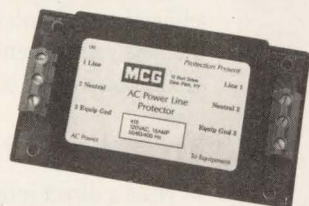
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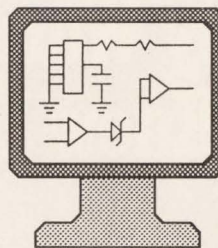
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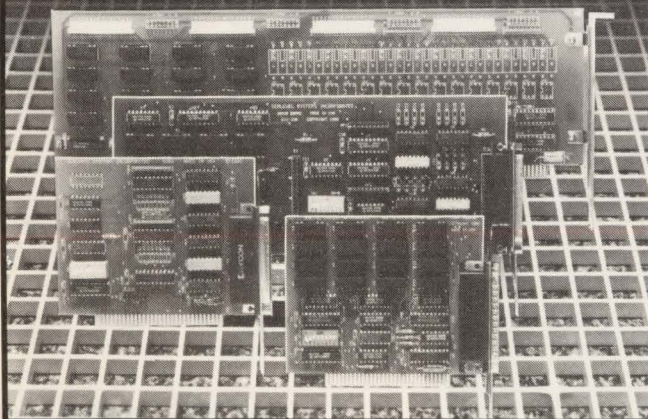
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Abbott Electronics	79	Instrument Specialties Co Inc	252	Planar	255
ACCEL Technologies Inc	133	Intergraph	232	Power Convertibles	264
Advanced Circuit Technology	251	Intel	64-65, 72-73	Preh Electric	36
Alpha Products	194	Interphase Corp	116	Prescience	78
Altera Corp	50-51	Interpoint	247	Pulse Engineering	222
American Airlines	190-191	Introl Corp	234	Quantic Lab	265
American Switch	230	IOtech Inc	31	Radstone Technology	243
Ametek	40	Ironwood Electronics Inc	255	Raltron	86
AMP	14-15	ITT Pomona Electronics	206	Rogers Corp	256, 257
Amphenol	32-33	Joemex Electrics America	254	Rolyn Optics Co	254
Analog Devices Inc	38, 44-45, 85, 87, 89, 91, 259	Keithley Instruments	99-101	SBE	66
Antex Electronics	265	Kikusui	252	Sealevel Systems	267
Atlanta Signal Processors, Inc	184	Kinemetrics/Truetime	256	Sextant Avionique	28
Atmel Inc	219	KMS Advanced Products	244	Siemens Munich	62-63
Avocet Systems Inc	210	Lattice Semiconductor Corp	6	Signal Transformer Co Inc	C4
Bayer AG	157	Laube Technology	267	Signum Systems	255
B&C Microsystems	223	Leader Instruments Corp	250	Silicon Systems	61
Beta Automation	255	Leap Electronic Co.	253	Single Board Solutions	258
BNK	254	Linear Technology Corp	160	Softaid Inc	256
BP Microsystems	258	Link Computer Graphics Inc	258	Softools	253
Burr-Brown Corp	268	Littelfuse Inc	258	Sony	68
Cahners CAPS	179	Logical Devices Inc	C2, 253	Sophia Systems Inc.	29
Capilano Computer Systems Inc	256	LSI Logic Corp	12-13	Spectrum Software	214
Capital Equipment Corp	82	3M Electrical Specialties Div	246	Stag Microsystems Inc	96
Carroll Touch Inc	209	Macrolink Inc	254	Sun Systems	90
Cermetek	253	Masstek	255	Synsem	181
Chronology	235	Maxim Integrated Products	149, 151, 153, 155	TEAC Corp	261
Cirrus Logic	23	MCG Electronics Inc	267	Teltone	257
Communications Specialties Inc	253	MCSI	254	Tempil Div, Big Three	254
Communication Specialists	258	Maxtor	236, 237	Tempustech, Inc	255
Computer Products Inc	211	Mental Automation	258	Teradyne Inc	34-35
Cubit/Proteus Industries Inc	81	Meritex	192	Texas Instruments Inc	117-120
Cybernetic Micro Systems	238	MetaLink	255, 257	Thomas and Betts Corp	74-75
Cypress Semiconductor	19	MF Electronics	235	Thunderbird Technologies	113
Dale Electronics Inc	1, 220	Micro Linear	185	Tokin America	165
Data Delay Devices	82	Micromint	263	Toshiba America Electronic Components	171-178
Data I/O Corp	256	Micro/Sys	253	Transera	180
Datel	182	Mini-Circuits Laboratories	3, 4, 24-25, 36-37, 163	Trend Circuits	167
Deltron Inc	227-230	Mizar Inc	208	Tribal Microsystems	257
Design Computation Inc.	254	Molex Inc	270	Universal Data Systems	C3
Dexter Magnetics	42	Motorola	146-147	US Industrial Distribution	251
DigiKey	213	Motorola Semiconductor Products Inc	26-27, 83, 114-115	Vesta Technology Inc	255
Digital Equipment Corp	10-11	Murata Erie America Inc	157	Vicor Corp*	111
Diversified Technology	202-203	Murrietta Circuits	267	Vishay Electronics Components	1
Dow Chemical USA	134-135	National Semiconductor Corp	97, 136, 137-138	VL Electronics	242
Duracell	224-225	NEC Corp	102-103	VMETRO Inc	215
Eagle Picher	41	NCI	256	Westcor	76
Echelon	92-93	NCR Corp	186-187	White Technology	200
EEsof	54	NEC Electronics Inc	240	WinSystems Inc	90
Electronic Measurements Inc	216	Nichicon Corp	239	Zax Corp	42
Elgar	228	NMB Technologies	217	Z-World Engineering	257
Emulation Technology	256, 257	Octagon Systems	257	Ziatech Corp	241, 264
Epson America Inc	205	OKI Semiconductor	28-29	Zilog Inc	30
ERNI Components	227	Omnibyte Corp	204	Zycad	248
Futaba Corp of America	226	Omron Electronics Inc	159		
Gates Energy Products Inc	201	OrCAD Systems Corp	8-9, 193		
GCOM Inc	257	Orion Instruments	169		
Glassman High Voltage Inc	231	Pacific Electro Data Inc	212		
Grammar Engine Inc	255	Pacific Hybrid Microelectronics	249		
Hamamatsu Corp	229	Penn Eng & Mfg Corp	21		
Heurikon Corp	43	Pentica Systems	218		
Hewlett-Packard Co	2, 16, 48	PEP Modular Computers	94-95		
IBM Corp	52-53	Phihong Enterprise Co Ltd	238		
ICHIA North America	265	Pico	246, 249		
IDT	59	Pioneer Magnetics	188		
IEE	189				
ILC Data Device Corp	71				
Incredible Tech	258				

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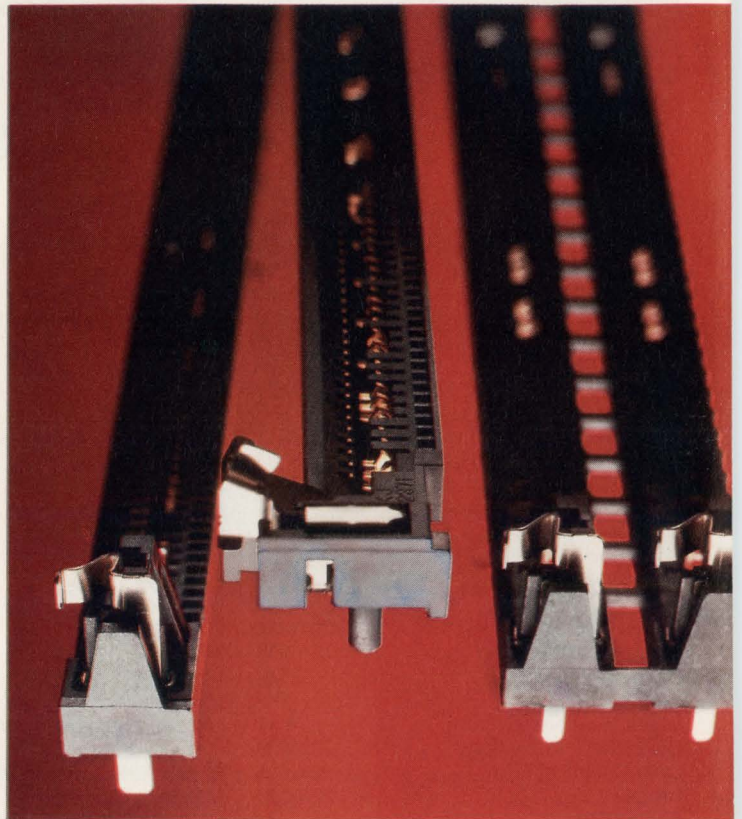
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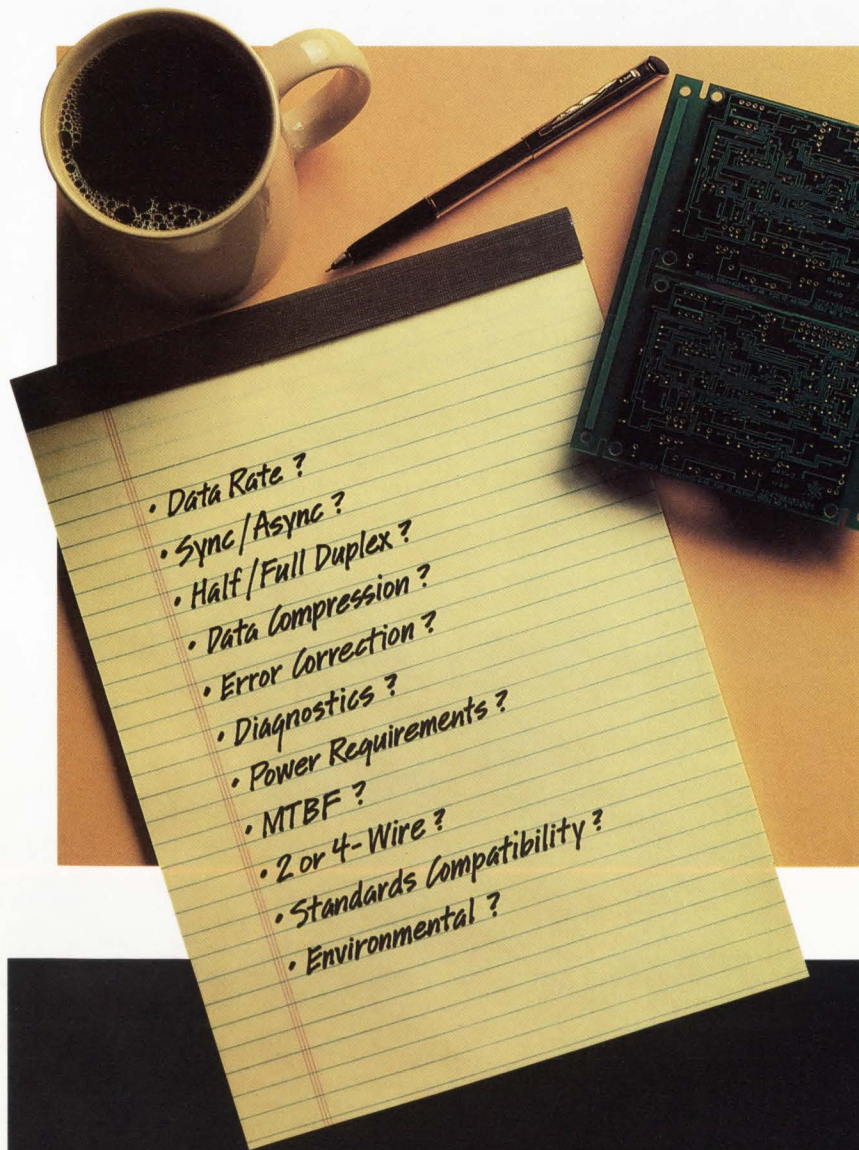
Made with high temperature-resistant liquid crystal polymer housings, SIMM sockets come in .050" and .100" pitch, and are available in a broad range of configurations: single and dual row, verticals, low profiles, and right angle. Call today for more information.



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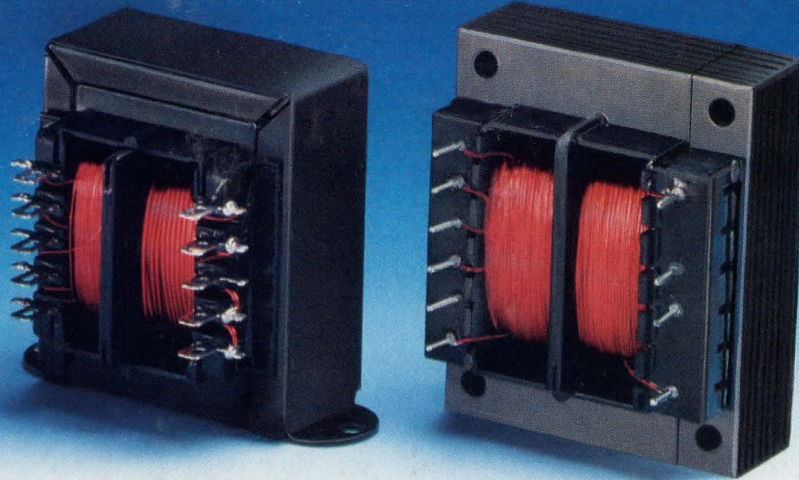
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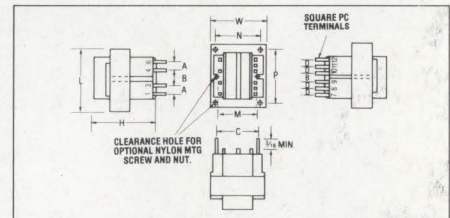
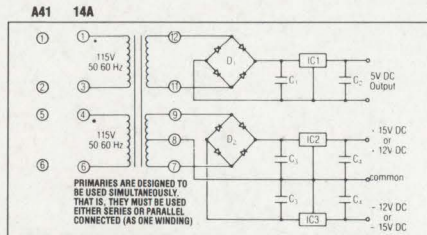
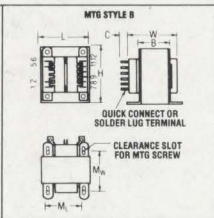
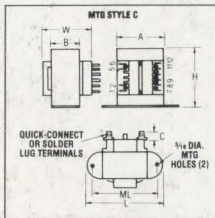
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PART NUMBER PRIMARY 50/60 Hz	DC OUTPUT		VA	PRICE
	Regulator 1	Regulator 2		
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A41-25-515	5V @ 1.25A	± 15 V @ 130MA	25	16.25
A41-43-512	5V @ 2A	± 12 V @ 300MA	43	20.75
A41-43-515	5V @ 2A	± 15 V @ 250MA	43	20.25
A41-80-512	5V @ 3.5A	± 12 V @ 600MA	80	28.50
A41-80-515	5V @ 3.5A	± 15 V @ 500MA	80	28.50

PART NUMBER PRIMARY 50/60 Hz	DC OUTPUT		VA	PRICE
	Regulator 1	Regulator 2		
115/230V				
14A-20-512	5V @ 750MA	± 12 V @ 200MA	20	15.00
14A-20-515	5V @ 750MA	± 15 V @ 175MA	20	15.00
14A-30-512	5V @ 1.25A	± 12 V @ 250MA	30	17.75
14A-30-515	5V @ 1.25A	± 15 V @ 200MA	30	17.25
14A-56-512	5V @ 3A	± 12 V @ 300MA	56	21.00
14A-56-515	5V @ 3A	± 15 V @ 250MA	56	21.00



VA	Dimensions						Terminals	Mtg. Style	Mtg. ML	Mtg. MW	Mtg. Screw	Lbs.
	L	W	H	A	B	C						
25	2 ¹³ / ₁₆	1 ⁷ / ₈	2 ⁵ / ₁₆	2	1 ¹ / ₈	3 ¹ / ₈	3 ¹ / ₁₆ (.187)	C	2 ¹ / ₈	-	#6	1.25
43	3 ¹ / ₈	2 ¹ / ₁₆	2 ¹ / ₁₆	2 ¹ / ₄	1 ¹ / ₈	3 ¹ / ₈	3 ¹ / ₁₆ (.187)	C	2 ¹ / ₁₆	-	#6	1.6
80	2 ¹ / ₂	2 ³ / ₈	3	-	1 ³ / ₈	3 ¹ / ₈	3 ¹ / ₁₆ (.187)	B	2	2 ¹ / ₁₆	#6	2.8

VA	Dimensions								Pin Dimensions	Mtg.			Mtg. Screw	Quantity	Lbs.
	L	W	H	A	B	C	D	M		N	P	Size			
20.0	2 ¹ / ₄	1 ³ / ₈	1 ¹ / ₈	.400	.400	1.460	.200	0.038SQ	1 ¹ / ₂	-	-	#4	2	0.90	
30.0	2 ³ / ₈	2 ¹ / ₁₆	1 ¹ / ₈	.550	.275	1.680	.275	0.045SQ	-	1 ¹ / ₄	2 ³ / ₁₆	#6	4	1.15	
56.0	3	2 ¹ / ₂	1 ¹ / ₁₆	.600	.300	1.900	.300	0.045SQ	-	2	2 ¹ / ₂	#6	4	1.70	

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