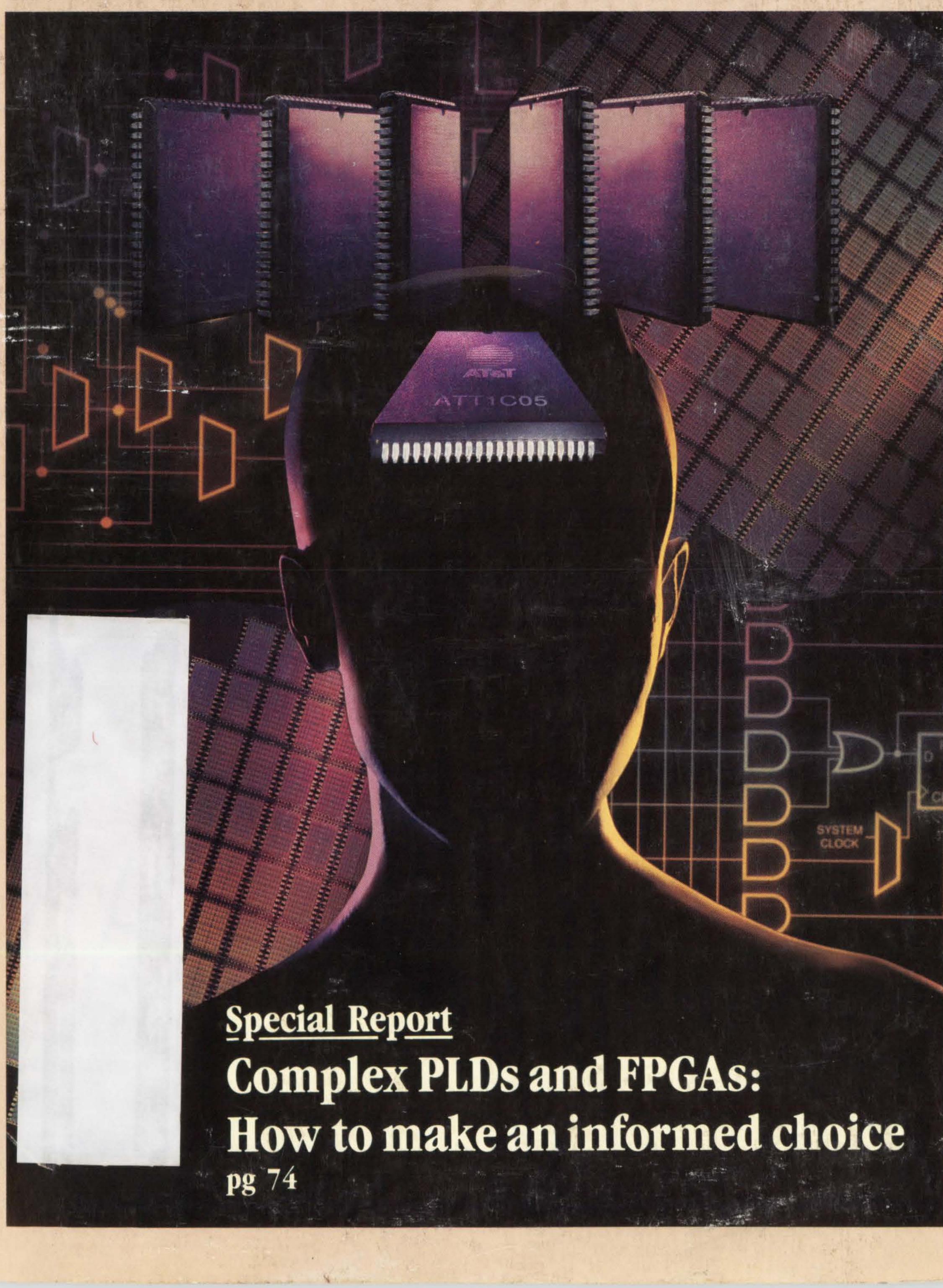
EDN

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

A CAHNERS PUBLICATION

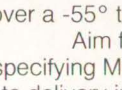
September 17, 1992



Special Report

Complex PLDs and FPGAs: How to make an informed choice

pg 74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up to 1900MHz from $6[25]

Now available, a large variety of tiny, ultra-rel high performance mixers to handle your applications from extra wideband, high isolation, low two-tone third-order IM, to very low +3dBm LO power.

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5-YR. GUARANTEE *

with extra long life due to unique HP monolithic diode construction, 300°C high temp. storage, 1000 cycles thermal shock, vibration, acceleration, and mechanical shock exceeding MIL requirements.

SPECIFICATIONS: all spec limits are 4.5 σ from mean

Model	Freq. Range LO. RF	(MHz) IF	LO Level (dBm)	Conv. Loss Mean ($\bar{X}$) mid-band (dB)	L-R Isol. Mean ($\bar{X}$) mid-band (dB)	Price $ (1-9)
LRMS-2L	800-1000	DC-200	+3	6.6	24	6.95
LRMS-1	0.5-500	DC-500	+7	6.4	45	6.25
LRMS-1W	2.0-750	DC-750	+7	5.8	45	6.75
LRMS-2	5-1000	DC-1000	+7	6.8	38	6.95
LRMS-2D	5-1000	DC-1000	+7	6.8	40	7.25
LRMS-2U	10-1000	10-1000	+7	6.5	46	11.45
LRMS-5	5-1500	DC-1000	+7	6.0	41	13.95
LRMS-11A	1400-1900	40-500	+7	7.0	25	16.95
LRMS-1LH	2.0-500	DC-500	+10	5.8	47	7.95
LRMS-2LH	5-1000	DC-1000	+10	6.6	40	8.95
LRMS-5LH	10-1500	DC-900	+10	5.4	38	14.95
LRMS-1MH	2.0-500	DC-500	+13	5.7	44	8.95
LRMS-2MH	5-1000	DC-1000	+13	6.6	44	9.95
LRMS-5MH	10-1500	DC-900	+13	5.8	46	15.95
LRMS-1H	2.0-500	DC-500	+17	6.3	44	10.95
LRMS-2H	5-1000	DC-900	+17	7.2	36	11.95
LRMS-2UH	10-1000	10-750	+17	7.1	38	14.45
LRMS-5H	10-1500	DC-900	+17	7.2	45	17.95

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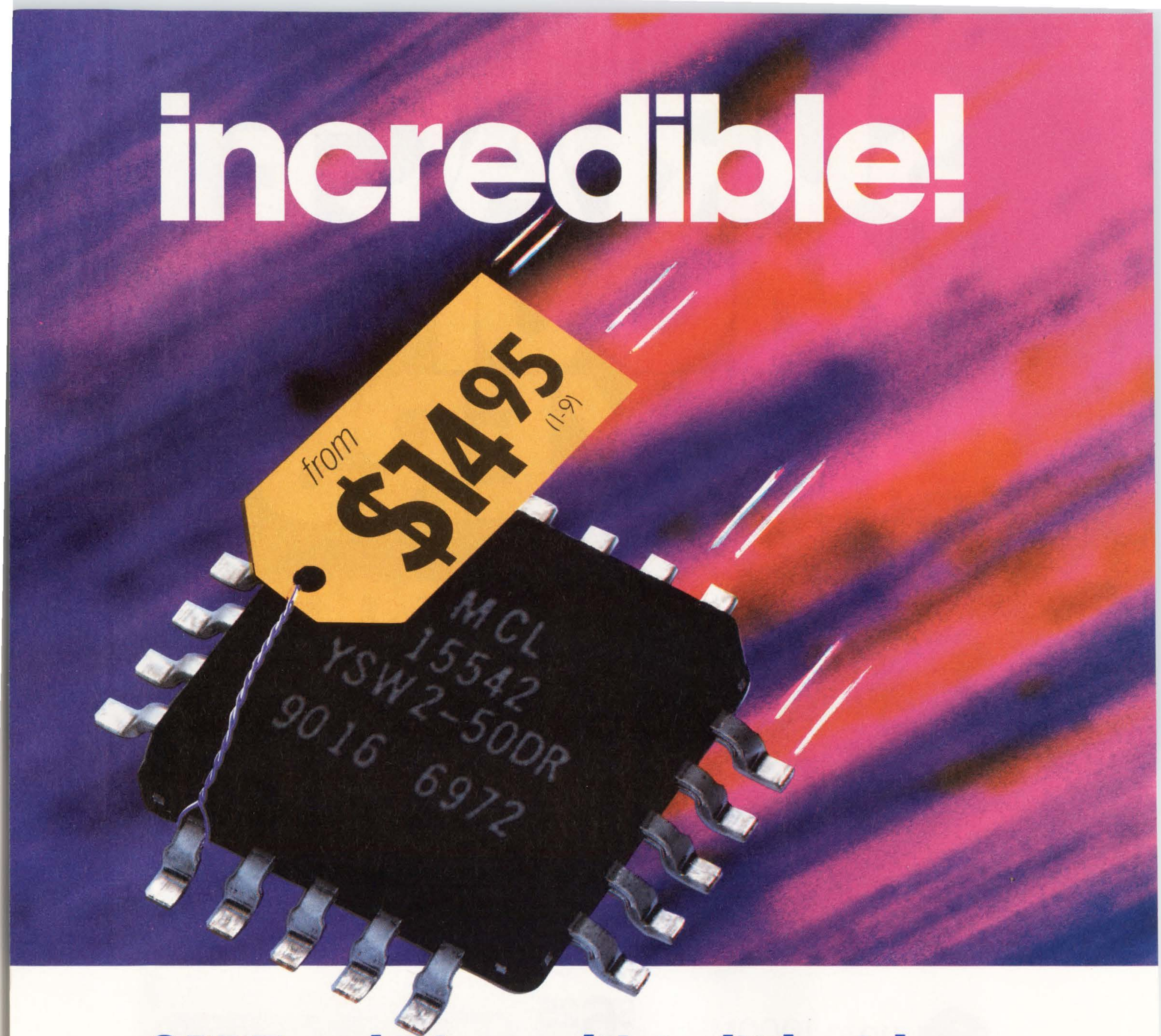

SPDT switches with built-in driver

ABSORPTIVE or REFLECTIVE dc to 5GHz

Truly incredible...superfast 3nsec GaAs SPDT reflective or absorptive switches with built-in driver, available in pc plug-in or SMA connector models, from only $14.95. So why bother designing and building a driver interface to further complicate your subsystem and take added space when you can specify Mini-Circuits' latest innovative integrated components?

Check the outstanding performance of these units...high isolation, excellent return loss (even in the "off" state for absorptive models) and 3-sigma guaranteed unit-to-unit repeatability for insertion loss. These rugged devices operate over a -55° to +100°C span. Plug-in models are housed in a tiny plastic case and are available in tape-and-reel format (1500 units max, 24mm). All models are available for immediate delivery with a one-year guarantee.

SPECIFICATIONS (typ)	Absorptive SPDT YSWA-2-50DR ZYSWA-2-50DR			Reflective SPDT YSW-2-50DR ZYSW-2-50DR		
Frequency (MHz)	dc-500	500-2000	2000-5000	dc-500	500-2000	2000-5000
Ins. Loss (dB)	1.1	1.4	1.9	0.9	1.3	1.4
Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	—	20	—	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
Sw. Spd. (nsec)	3	3	3	3	3	3
Price, $ (1-9 qty)	YSWA-2-50DR (pin) 23.95 ZYSWA-2-50DR (SMA) 69.95			YSW-2-50DR (pin) $14.95 ZYSW-2-50DR (SMA) 59.95		

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CIRCLE NO. 16

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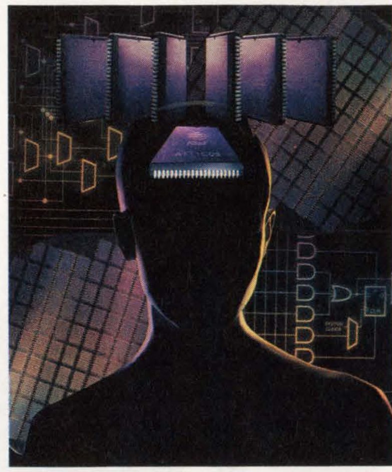
EDN
MAGAZINE EDITION

September 17, 1992 VOLUME 37, NUMBER 19

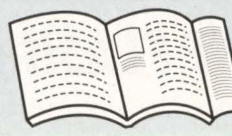
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE



On the cover: Making informed choices about the many types of complex PLDs and FPGAs means sifting carefully through your design criteria. Among the things to consider is your choice of hardware architecture and what design methodologies you will use. (Photo courtesy of AT&T; photography by Clayton J Price; concept by Bessen Tully & Lee) . . . . PAGE 74

Foldout Contents

Turn to the last information-retrieval service card in the back of this magazine and you'll find a foldout table of contents. Now, instead of flipping back and forth from this table of contents to the articles you want to read, you can have the convenient foldout open at all times while you're reading EDN. Use the foldout contents to mark off articles you'd like your colleagues to read or to remind yourself to copy stories for your files.



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EDN
MAGAZINE EDITION

September 17, 1992

Continued from page 5

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PROCESSOR UPDATES

DESIGN IDEAS

NEW PRODUCTS

DEPARTMENTS

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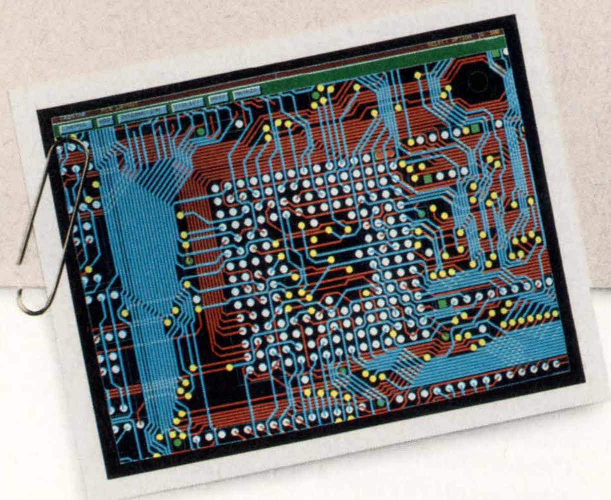

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CIRCLE NO. 17

A summary and analysis of articles in this issue

If you're designing wireless communications systems, you not only have to be an expert, you need help too. Communications is a hot area, and we're seeing an increasing demand for engineers with experience designing wireless products. Today, those products go beyond cellular phones, from mundane garage-door openers to wireless office networks. Doug Conner takes a look at **CAE tools that let designers simulate wireless systems** from the beginning to the end of the system. Unfortunately, vendors differ on how they define beginning and end. Some tools help you design modulators and demodulators, and others easily handle the RF front ends of communications systems.

Specifically, Doug's report looks at how you can use simulation tools to observe the effects of small changes in wireless systems. These are often tough problems to discover and solve. Doug says that engineers facing the challenge of designing sensitive wireless communications systems often don't know what tools are available.

Engineers can use assistance, too, when trying to decide which type of complex programmable logic device (PLD) or field-programmable gate array (FPGA) to use. Anne Swager's Special Report gives you a brief tutorial about what's available and **how to approach complex-PLD and FPGA design problems.** Anne says that most designers are used to working with simple PLDs. However, the complex PLDs and FPGAs present new problems and require new ways of thinking. FPGAs are blocks of logic functions, but PLDs remain structured sets of sum-of-product blocks. It's not as easy as it might seem to go from one to the other.

Anne Swager takes a close look at the differences between designing with FPGAs and complex PLDs.

Doug Conner's Technology Update covers CAE tools for wireless systems.

Anne's report tells you how to compare and select products. She also tells you about the design methods you can choose.

David Shear completes this issue's line-up with our annual **Digital Signal Processor Chip Directory**. David has dug deeply through mounds of DSP-chip information to bring you the latest compilation of chip specs, facts, and figures.

Jon Titus
Editorial Director

Soon, Eight Hours Of Portable Computing Will Be...

(actual size)

AMD Introduces The World's First 386 Microprocessor With 3-Volt Technology.

Two standard dry-cell batteries. There's really nothing special about them. Aside from the fact that they can run a powerful, portable 386 computer for a full eight hours. Provided, of course, that portable is built around a low-voltage Am386™ microprocessor.

The 25MHz DXLV and the 25MHz SXLV are available in PQFP packaging.

Thanks to the low-voltage Am386 microprocessors, laptop, palmtop and notebook computer designs will become smaller, lighter, and more powerful than ever before.

With battery life of up to eight hours or more. That's a full day's worth of 386 performance—the per-

urs Of Portable Look Like This.

formance you need to run sophisticated applications like Windows™ 3.0.

And rest assured, the low-voltage Am386 microprocessors are proven compatible and comply fully with JEDEC standards for low-power, 3-volt computing. We can even supply you with the 3-volt EPROMs your systems will need. Other 3-volt system logic is also readily available.

For more information on the low-voltage Am386 microprocessors call AMD today at **1-800-222-9323**. You'll never look at dry-cell batteries the same way again.

Advanced Micro Devices

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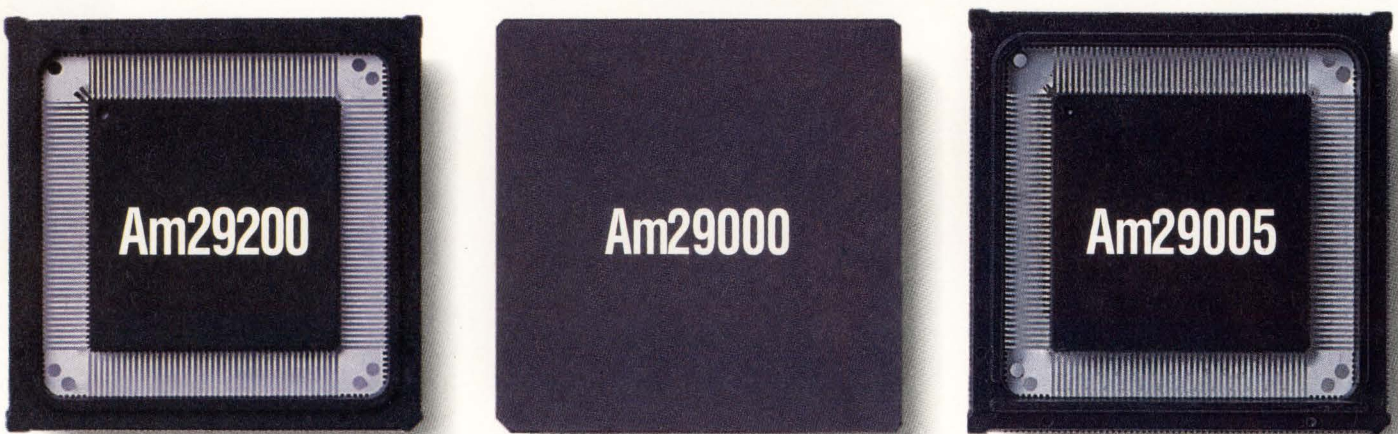
CIRCLE NO. 21

Put These G
And Take So



Whatever you're working on, please stop. You deserve to take some time off. And with any member of the AMD 29K™ Family of embedded RISC processors, you can take several months off your design cycle.

That's because 29K processors' simple, highly integrated designs will knock time-consuming steps off your schedule. Take the inexpensive, new Am29200™ microcontroller. With many features like I/O controls and serial ports included on-chip, it's the easiest to use embedded processor available. Adding memory requires no interface circuitry. It's as simple as playing "Connect the dots."

Memory interface throughout the rest of the family is fast and easy too. Each processor in the 29K Family integrates easily with low-cost PLDs or simple glue logic to minimize your circuitry needs.

You'll also save valuable time when you're expanding your product line. The entire 29K family is binary compatible. So you just deter-

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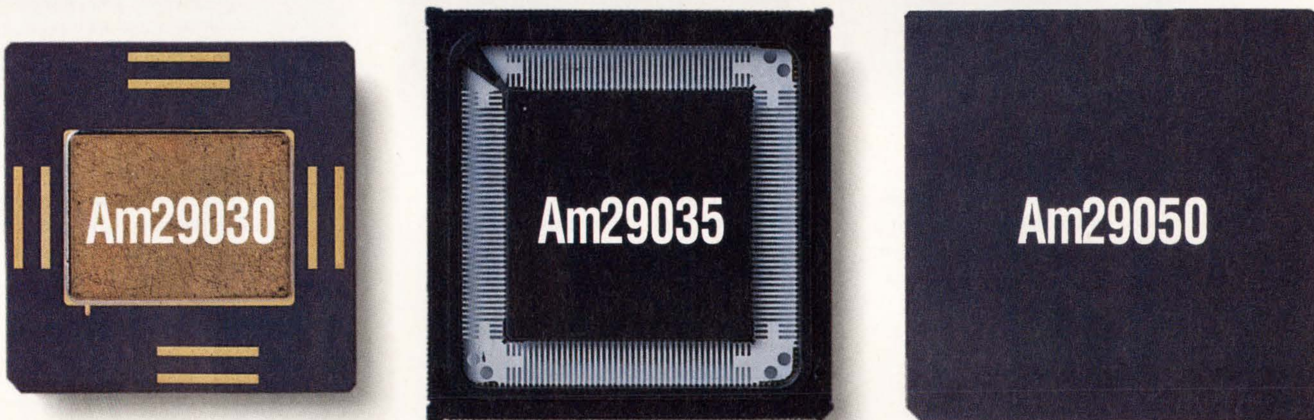
me Time Off.



mine the performance you need and select the appropriate chip—from the Am29200 to the high-end Am29050™ processor. There's no need to recompile your applications' software as you scale up or down the performance ladder.

And thanks to the 29K's RISC architecture, you can use inexpensive memory devices to lower your system costs and still deliver the high performance your customers demand.

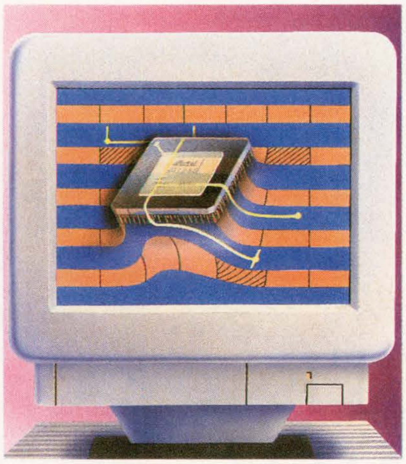
For more information on the 29K embedded RISC family call today at **1-800-292-9263 Ext. 3.** Then kick back and watch the AMD guys go to work.

Advanced Micro Devices

901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088.

CIRCLE NO. 22

PGA Market Leader, Thoughts About Who's #1.



Designing Made Simple.

Actel devices' plentiful routing resources give you 85% gate utilization using 100% automatic placement and routing, letting you place and route a 4,000-gate design in our A1240 chip in only 30 minutes.

Greater Capacity.

With 8,000 gate-array equivalent gates, the A1280 has led the industry in capacity for over 2 years. And it's still the only high-density, high-performance FPGA available in volume production.

Catch Our Next Act.

We're building on this FPGA technology to set new performance levels with our upcoming ACT 3 FPGAs. Whichever ACT you catch, you'll get a long-term partner and the best performance in town.

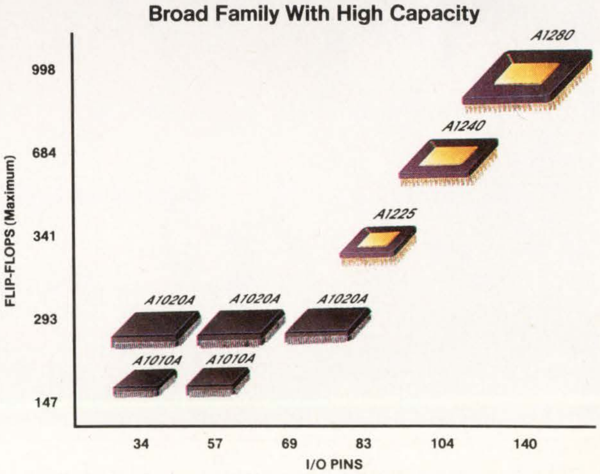
much quicker time-to-market and complete control of the design process, as well as competitive FPGA prices. Which saves you both money *and* time.

The FPGA Design Guide

And #1 in service and support. Customers can call our technical hotline and talk to a real person—not voicemail. Or customers can use our automatic Action FACTS system to fax themselves quick answers to their application questions.

We're building on our experience to bring you the most advanced products for any application, and we're committed to establishing a quality, long-term partnership with you for your future success.

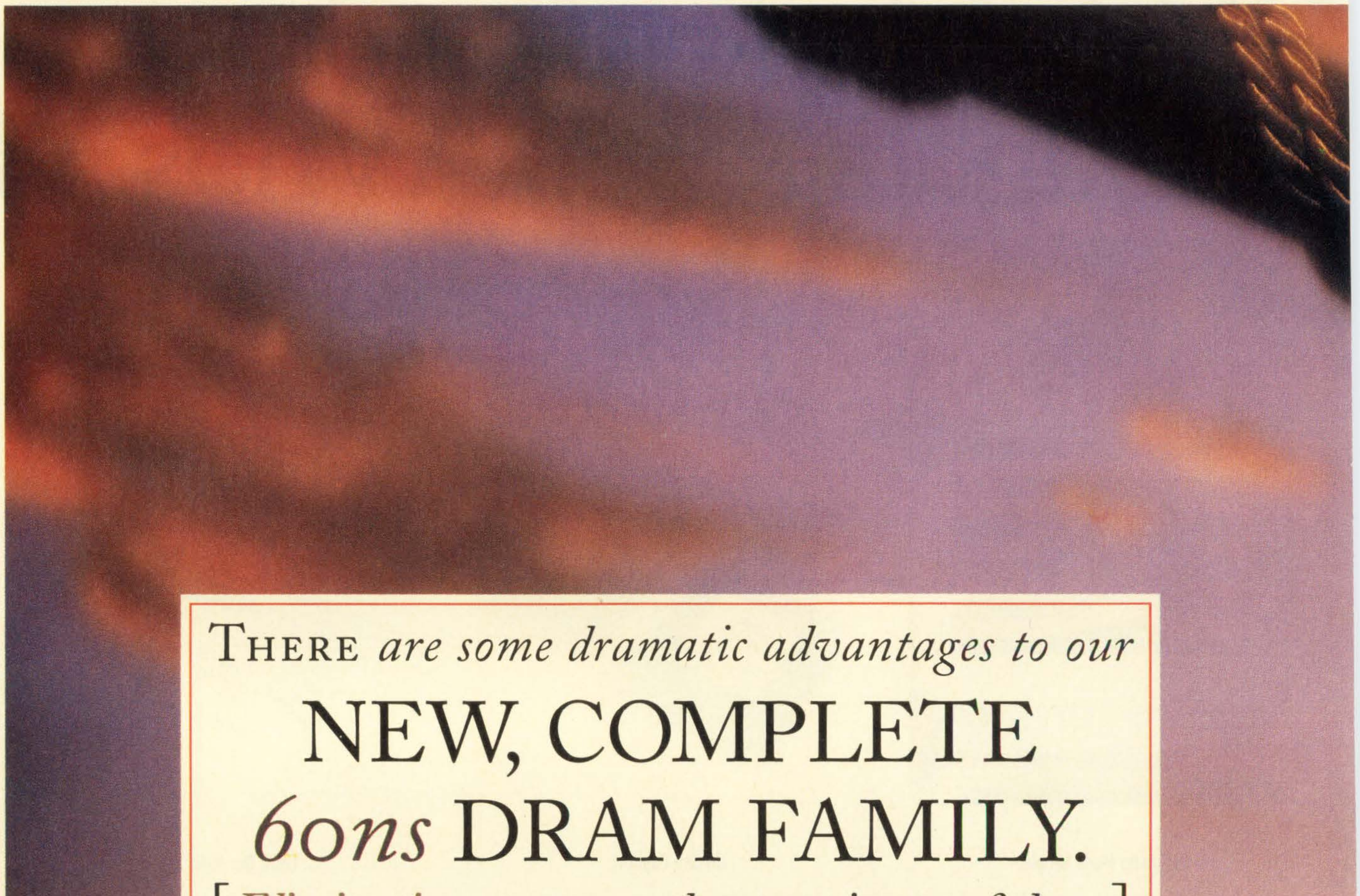
Call **1-800-228-3532** for more information on our powerful family of FPGAs. And discover how far the real industry leader can take you.



Actel

Risk-Free Logic Integration

CIRCLE NO. 23

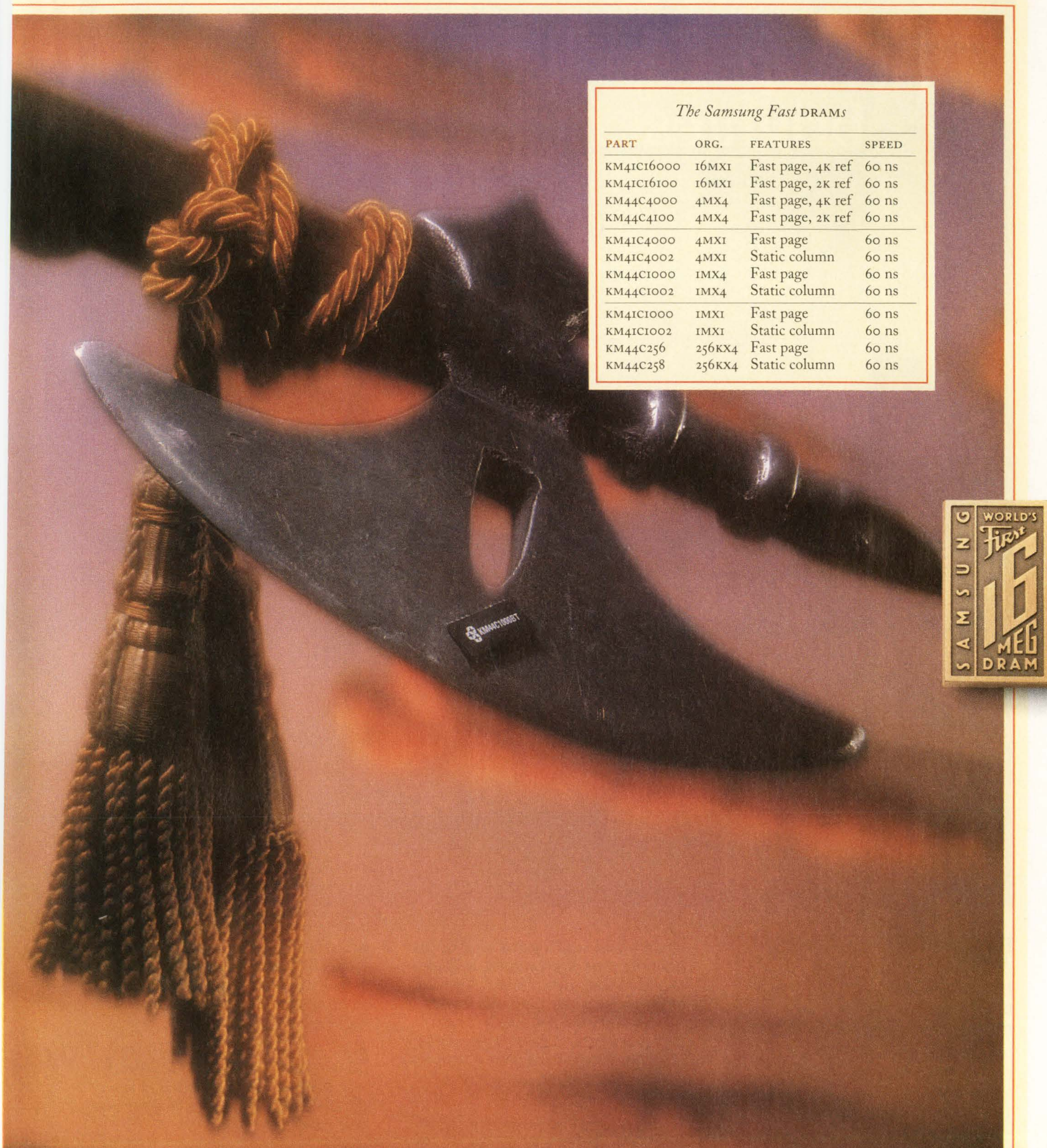


At Samsung, we're not content to have brought the world its first 16-meg DRAM.

We're extending the gains we've made in this important segment of technology, by introducing a complete family of DRAMs at the highest speeds in use—60 nanoseconds.

These are speeds that will let designers of many 386 systems eliminate SRAM cache altogether. And for many high-end graphics OEMs, it will be possible to eliminate VRAMs.

Of course, one result of those things will be that you'll be able to lower the axe, so to speak, on unwanted costs.



The Samsung Fast DRAMs

PART	ORG.	FEATURES	SPEED
KM41C16000	16MX1	Fast page, 4K ref	60 ns
KM41C16100	16MX1	Fast page, 2K ref	60 ns
KM44C4000	4MX4	Fast page, 4K ref	60 ns
KM44C4100	4MX4	Fast page, 2K ref	60 ns
KM41C4000	4MX1	Fast page	60 ns
KM41C4002	4MX1	Static column	60 ns
KM44C1000	1MX4	Fast page	60 ns
KM44C1002	1MX4	Static column	60 ns
KM41C1000	1MX1	Fast page	60 ns
KM41C1002	1MX1	Static column	60 ns
KM44C256	256KX4	Fast page	60 ns
KM44C258	256KX4	Static column	60 ns

But the advantages don't end there. Reduced parts count will mean greater reliability, lower power consumption, and reduced assembly costs.

We offer the fast DRAM in 1Mb, 4Mb, and even 16Mb densities. Which not only puts us on the cutting edge. But will do the same for you.

For more information, please call 1-800-446-2760 or 1-408-954-7229 today. Or write to DRAM Marketing, Samsung Semiconductor Inc., 3655 No. First St., San Jose, CA 95135.

SAMSUNG

A *Generation* AHEAD.

EDITED BY SUSAN ROSE

Analog ASIC gives choice of design basis

Designers of digital ASICs have long had a choice between gate-array, standard-cell, and full-custom designs, each offering a different tradeoff between circuit density and ease-of-design. Raytheon's Semiconductor Division is now giving analog designers a similar choice by adding a standard-cell library to its RPA160 BiCMOS analog tile-array family. Because the tile array and standard cells share the same process, designers can take advantage of the quick turnaround for the array, then migrate their design to standard cells as production levels warrant.

The npn and pnp transistors of the base process have a toggle frequency (f_t) of 4 and 1.5 GHz and a breakdown voltage of 13V. The resulting cells are also fast and include a 500-MHz buffer, a 70-MHz 8-bit DAC, and a 30-MHz ADC. The standard-cell library also includes digital cells, offering both CMOS and ECL logic. The company has CAD software for both PC and workstation platforms for the array and standard-cell library or will handle your design as a turnkey operation. NRE charges for standard-cell designs begin at $40,000, with prototype delivery in eight weeks. Raytheon Co, Mountain View, CA, (415) 968-9211, FAX (415) 969-8556.

Scalable processor board suits STD 32 Bus

Designs requiring high processing power for industrial applications can take advantage of Ziatech's ZT8911 Scalable Processor Board. The processor board accommodates performance options ranging from a 25-MHz 486SX to a 66-MHz 486DX2. In addition, the replaceable CPU module will also accommodate Intel's next-generation CPU when it becomes available. The board uses the 32-bit capability of the STD 32 Bus with data-transfer rates up to 32 Mbytes/sec.

The scalable processor board can function as the permanent master in multiprocessor systems, providing the bus-arbitration function for as many as six temporary masters in an STD 32 Star system. The board provides two interrupt controllers, two DMA controllers, two serial ports, a printer port, a real-time clock, an optional 64-kbyte second-level cache, and as much as 16 Mbytes of RAM. The processor board also has features for industrial applications such as watchdog timers, ac power-fail detect circuitry, timer/counters, and 24 lines of general-purpose digital I/O. The board occupies two card slots on the backplane. Single-unit price is $3500. Ziatech, San Luis Obispo, CA, (805) 541-0488, FAX (805) 541-5088.

120-MHz frequency generator costs $495

Four independent phase-locked-loop frequency sources on the GT310 let you generate frequencies from 360 kHz to 120 MHz. In addition, one of the four channels includes synthesis down to 0.0024 Hz, generating counted bursts, and precision pulse widths. All channels drive a 50Ω load with TTL-compatible levels. Frequency step size is less than 0.8% of output frequency. The PC/AT plug-in board comes with software for a virtual front panel, drivers, and library functions for Microsoft C or QuickBasic. Guide Technology, San Jose, CA, (408) 246-9905.

Add a solder mask to multilayer pc-board prototypes

When you need a prototype pc board fast, you can use a variety of pc-board prototyping systems to put one in your hands in less than one day. Unfortunately, you often have to give up important features you take for granted in a production pc board, such as multilayer designs with solder masks. Direct Imaging has now added dry-film solder-mask capability to their multilayer prototyping system, letting you create pc boards with solder masks that are as big as 11 × 14 in. and have 12 layers. The solder mask reduces bridging and electrical shorts when the pc board is soldered and provides an environmental barrier. The System Two Soldermask Station is $2995. Complete multilayer prototyping systems including the solder-mask station are less than $50,000. Direct Imaging, West Lebanon, NH, (603) 298-8383, FAX (603) 298-5257.

Software tests embedded systems

Texas Instruments' Scan Engine is a testability software package currently under development. The package will provide scan-based testing in embedded systems, eliminating external field-service test equipment. The software eliminates the test equipment because it can test anything that initiates and executes with boundary scan, such as built-in self-test, interconnect, functional, device, or logic cluster testing.

The software lets you embed GO/NO GO tests and

Text continued on pg 20

Text continued from pg 19

logging capabilities for batch test programs. The package is portable ANSI C source code that reads serial scan vectors from memory and applies those vectors to the unit under test with the end-user application. Designers receive the source code for the software so they can compile it on their target μP or μC. The source code is used for test application and response retrieval, response logging options, and portability to the embedded environment. User-definable parameters, such as the memory location of the test data, let you customize the test application to the target system. The licensed list price for the software package is $12,000. The company will charge a nominal royalty fee per unit shipped. Texas Instruments, Semiconductor Group, Dallas, TX, (214) 995-6611, ext 3990.

Data converter adds serial link for remote sensing

Many remote-sensing applications use an A/D converter at the sensor end and report data back to the host over a serial link. Now a single IC can handle all of those tasks. The ML2223 combines an A/D converter, S/H circuit, voltage reference, RS-232C UART, and baud-rate generator into one 16-pin plastic DIP. The device's base A/D converter uses a self-calibrating algorithmic successive-approximation technique to provide 12 data bits with one sign bit for an input-voltage range of −5 to +5V. The device can provide data on command with a conversion time of 45.6 μsec, or send a continuous stream of data over the serial link. The UART will handle RS-232C data rates as great as 19.2 kbps and RS-422 data at rates of 200 kbps. Samples are available for $14.50 (1000), with full production scheduled for September. Contact Micro Linear, San Jose, CA, (408) 433-5200.

Port graphics applications to Sun platforms

If you want to port Silicon Graphics (SGI) applications to a Sun SPARCstation, you can use a $900 software package called Nth Portable GL to accomplish the task within a few days, instead of the months the job might otherwise require. The program provides such high porting speeds because it supports almost all of the 478 SIG Iris GL V4.0 calls and provides a font manager and mixed-window-ing functions. The program uses Sun's native XGL graphics protocol, so the ported application will work with every Sun graphics board. Nth Graphics, Austin, TX, (512) 832-1944, FAX (512) 832-5954.

Engineers work for education

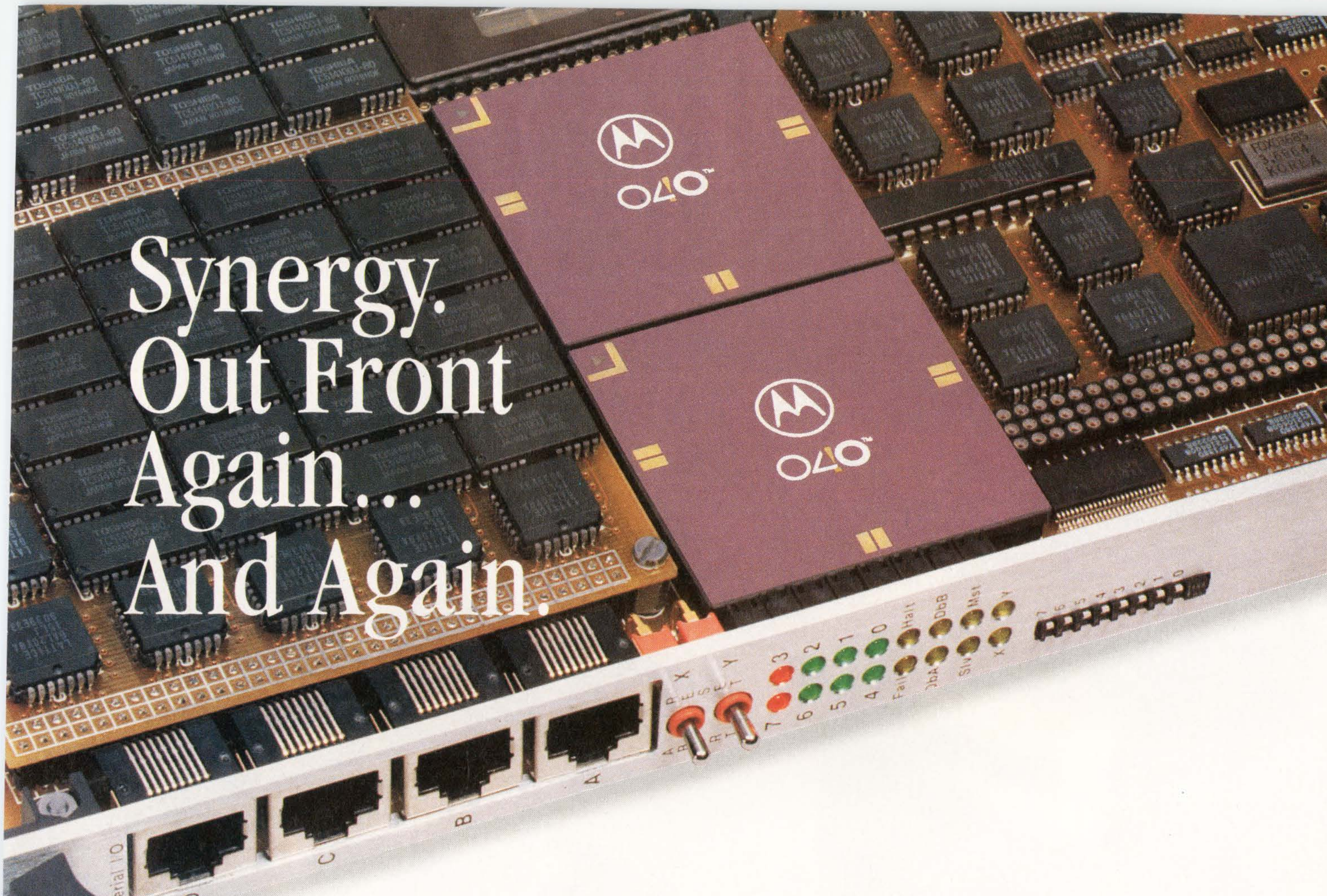
The steady decline in mathematics and science achievement of elementary and secondary students has made it increasingly difficult for American corporations to compete in the world marketplace. To change this trend, engineering professionals are taking to the schools. Engineers for Education is a nonprofit association of 45 engineering professional societies with the objective of recruiting 100,000 engineers as volunteers to improve math and science education in elementary and secondary schools throughout the US. Volunteers will serve as an additional resource for schools' math and science teachers—enhancing the caliber of education for our students. The group is establishing local coalitions that will work closely with individual schools and school boards to ensure that the programs respond effectively to the schools' needs.

The group offers many of programs through which engineers can volunteer. Activities depend on the interests and abilities of the volunteer and the needs and desires of the principal and teachers in each local school. Specific assignments are mutually agreed to by all parties. Typical activities include conducting classroom demonstrations and presentations, participating in career days, sponsoring or leading science and technology clubs, arranging field trips, providing mentorship, tutoring individual students, and more.

Volunteers can choose from a variety of programs that cater to specific age groups. For fourth through sixth graders, the group sponsors three programs: "A World in Motion" is a partnership of professional engineers assisting elementary school teachers in motivating students and bringing excitement and relevance to physical science and mathematics. "MAS" is a collaborative program designed to increase interest and achievement in math and science. It was originally used in communities along the Texas-Mexico border but is being expanded nationally. "SKILL" is an after-school and summer program designed to stimulate interest and encourage children. SKILL volunteers work closely with members of the National Action Council for Minorities in Engineering Inc.

Patterned after after-school sports, "Mathcounts" is designed for seventh- and eighth-grade students. "Mathcounts" combines a "coaching" component at the school level with a series of competitions at local, state, and national levels. For high-school students (grades 9 to 12), volunteers can work for "TEAMS." TEAMS gives students a chance to apply what they learn in math and science classes to real work situations in a national competition. Finally, "Science by Mail" teams up volunteer scientists with children as pen pals.

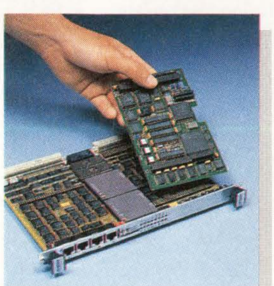
For more information about these programs or Engineers for Education, call the EFE hotline at (800) 489-0348. For more information on "Science by Mail," call (617) 589-0437. Engineers for Education, 39 Old Ridgebury Rd, Danbury, CT 06817.



The New Dual '040 VME SBC: Faster, More Efficient and Lower Cost Than Any Multi-board Solution

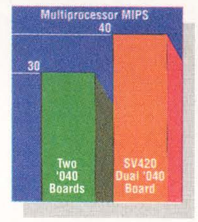
Get on-board multiprocessing and an astounding **40 MIPS** throughput, when you power your system with Synergy's new SV420 single-slot SBC. The SV420's dual-CPU design means you'll need fewer boards in your VME chassis, with no VMEbus bandwidth bottlenecks between the '040s, and system-wide cost saving of more than 40%.

And even if you don't need multiprocessing right now, the SV420 still puts you out front. Use the second '040 as a super-smart DMA controller. When combined with the SV420's **66 MByte/sec** VME64® circuitry, nothing communicates faster over the VMEbus.



Over a dozen smart, powerful I/O modules fit Synergy's '020, '030, '040 and Dual '040 SBC's.

Add even more on-board power by selecting from Synergy's big list of high-performance, intelligent plug-on I/O modules – such as our latest Super-VSB module offering 40+ MB/sec over the VSB bus. Or choose another module, from a T1/E1 controller to a super-fast graphics engine, that plugs onto any Synergy SBC.



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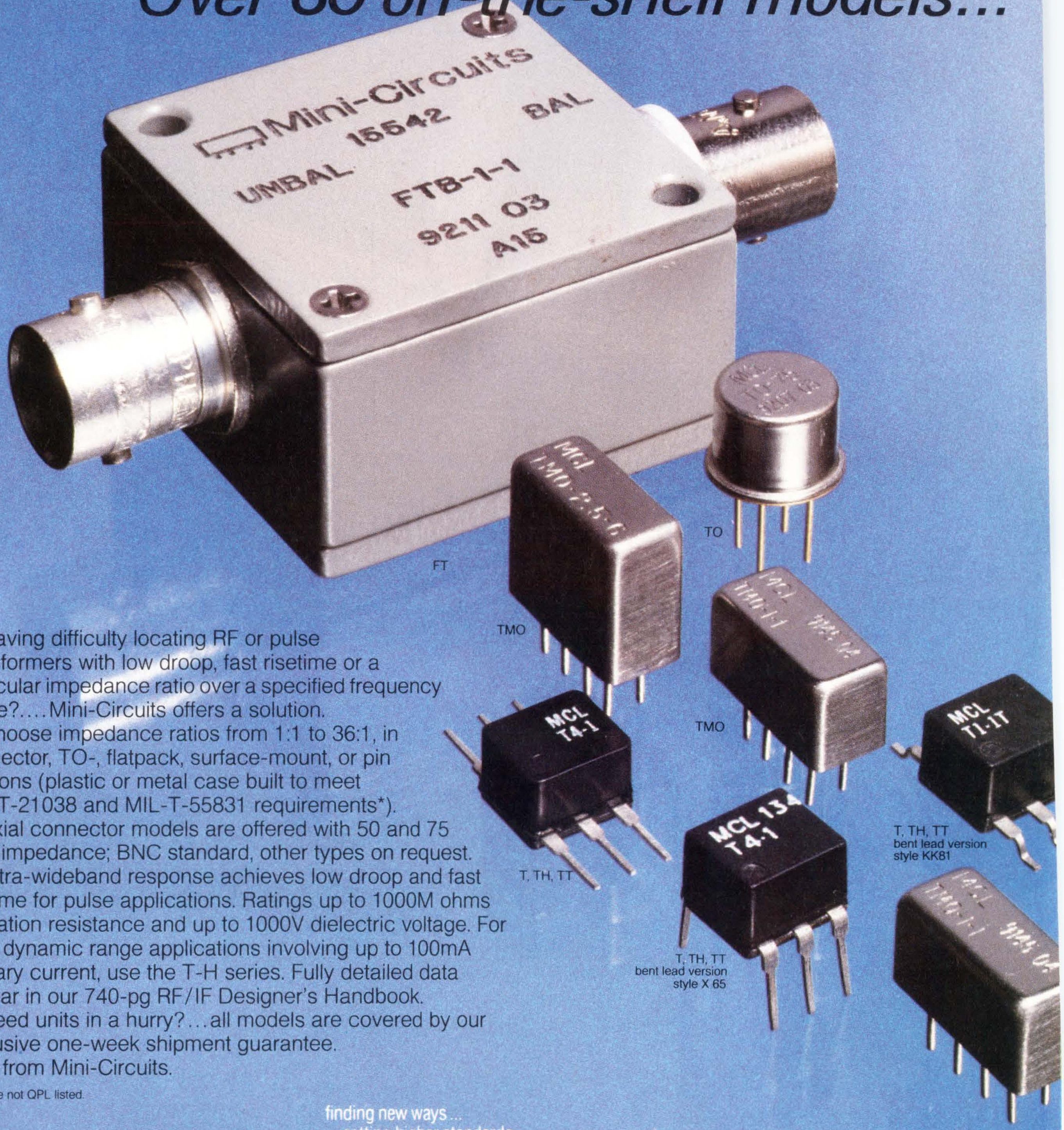

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FORMERS

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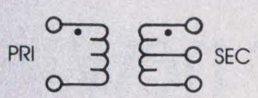
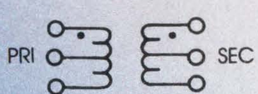
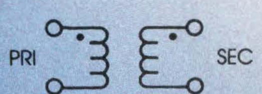
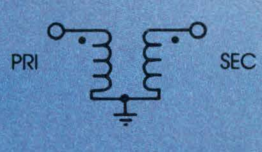
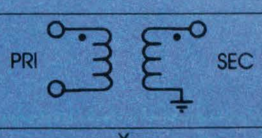
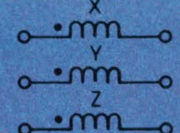
Config.		MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	2dB MHz	1dB MHz	PRICE $ Qty. (1-9)
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
		T1-6T	1	.015-300	.015-300	.021-150	.03-50	6.95
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	.2-350	.2-350	.35-300	2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
		T8-1T	8	0.3-140	0.3-140	0.7-90	1-60	7.95
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
	TMO	TMO1-1T	1	.05-200	.05-200	.08-150	.2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	8.45
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
		TT1.5-1	1.5	.075-500	.075-500	.2-100	1-50	5.95
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
	TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
		T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65
		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
		T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
		T36-1	36	.03-20	.03-20	.05-10	.1-5	6.95
	TO	TO-75	1	10-500	—	10-500	40-250	6.95
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
		T9-1H	9	2-90	2-90	3-75	6-50	6.45
		T16-1H	16	7-85	7-85	10-65	15-40	6.45
	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
		TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-8	8.45
		†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
		†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
		TMO16-1	16	.3-120	.3-120	.7-80	5-20	7.95
D 	T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
		T3-1	3	.5-800	.5-800	2-400	—	4.45
		T4-2	4	.2-600	.2-600	.5-500	2-250	3.95
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
	TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
		TMO3-1	3	.5-800	.5-800	2-400	—	8.45
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95
E 	FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
		■FTB-1-75	1	.5-500	.5-500	5-300	10-100	36.95
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95
		T2-613.1						

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0.5 dB over entire frequency range

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TMO, case A 11, + case B 13 FT, FTB, case H 16
NEW TC SURFACE MOUNT MODELS from 1 MHz to 1500 MHz

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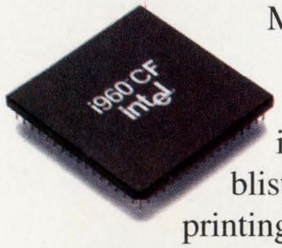
We've just tested the performance of our new i960 CF processor.



Make no mistake. This is no middle-of-the-road processor. It's our new superscalar i960™ CF chip. And it delivers blistering speed to your high-end printing, imaging, communications and networking applications. Simply put, it outruns every 32-bit embedded processor on the market—and we have over 25 benchmarks to prove it.

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The MACH™ Family From AMD: The Fastest, Most Predictable High Density PLDs Available Today.

Oops! You're a couple of nanoseconds shy this time, and it's going to hurt. Perhaps next time you'll choose a more predictable vehicle. And the most predictable high speed, high-density PLDs available are the MACH family from AMD.

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Model Number	Equiv. Gates	Macro Cells	Max. Delay	System Speed	I/O Pins	Hard-Wired Option
MACH 110	900	32	12ns	66.7 MHz	44	MASC 110
MACH 210	1800	64	12ns	66.7 MHz	44	MASC 210
MACH 120	1200	48	15ns	50 MHz	68	MASC 120
MACH 220	2400	96	15ns	50 MHz	68	MASC 220
MACH 130	1800	64	15ns	50 MHz	84	MASC 130
MACH 230	3600	128	15ns	50 MHz	84	MASC 230

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We listen

We're pleased to listen to what readers tell us. Even when we may not like what you have to say, we listen to your comments, criticisms, and ideas. We appreciate your writing, phoning, and keeping in touch. Even if you simply print a quick note on a bingo card, we read it.

As part of our continuing program to improve EDN, we've been listening closely to what you have been telling us about your needs for information. You've said many times that products and technology are important, followed by information about career planning, education, and professional issues. So, starting in October, you'll see more of an emphasis on those topics in our companion tabloid edition. Also, to dispel any confusion, both our magazine and our tabloid will simply carry the EDN logo, but you'll see the subheading, "Products & Careers" on the tabloid. What you'll see and read isn't a radical shift for us or for you—we've been covering products, technology, and careers since we started tabloid editions several years ago.

You'll also see a new emphasis on direct communications between you and our editors. We'll routinely ask your opinions on pressing technical and professional issues. We'll also ask you to tell us which products you like and which ones you don't. And we'll want to know which companies you would like to work for and which ones you wouldn't. You'll see your responses in articles that feature poll results and comments from many readers. Numerous articles will ask for reader feedback. In addition to your opinions, EDN Products & Careers will bring you the faces and the stories of your colleagues in engineering and management.

Besides our regular and new career information we'll also run product-preference polls that let you tell us what you think about products. We'll publish the results with no holds barred. If you and your colleagues pan a product, we'll let you know. All too often, publications become cheering sections for advertisers. Not in EDN. To help you find the products you need, we've aligned the product classifications we use in EDN Magazine and in our sister Products & Careers tabloid.

Reading any publication should be interesting and enjoyable. We're adding several new columnists, and you'll get their biased and unbiased opinions on everything from the latest products and technologies, to the best engineering bookstores, to the neatest high-tech hangouts, museums, and other places you want to know about. Columns will cover technical topics from analog circuit design to power-supply design, too. Also, if you've got a puzzle that will stump your colleagues, send it in.

We're pleased that you've been telling us what you think of EDN. I'm sure you'll be pleased with the Products & Careers tabloid edition of EDN you'll receive in October. After you read a few issues of EDN Products & Careers, let us know what you think. We'll be listening.

Jon Titus
Editor

Jesse H. Neal
Editorial Achievement Awards
1990 Certificate, Best Editorial
1990 Certificate, Best Series
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

American Society of Business Press Editors Award
1991, 1990, 1988, 1983, 1981

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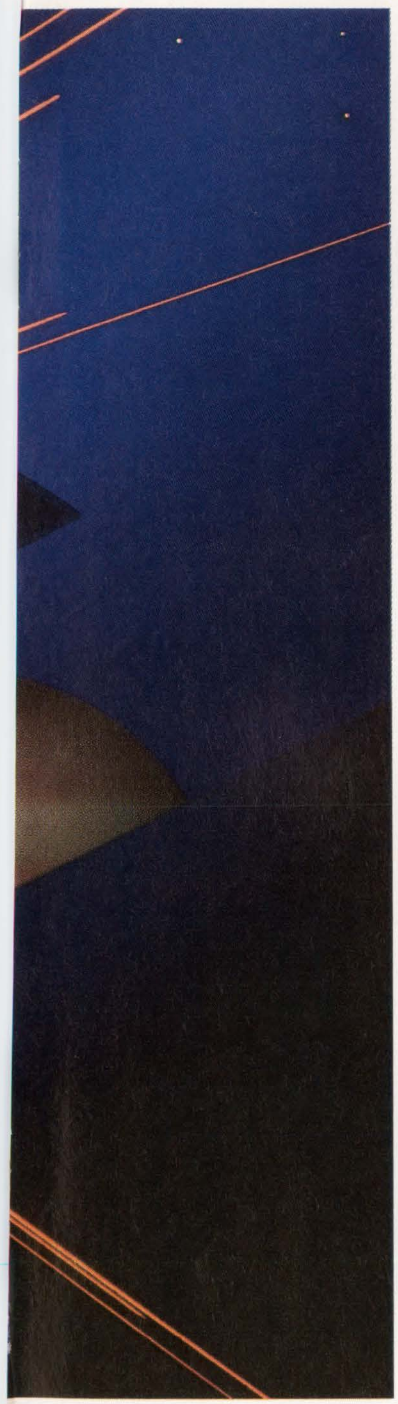
worldwide acceptance of LANs. In fact, well over 13 million Ethernet adapter cards have been designed using National's silicon — more than all other suppliers combined. National's ST-NIC™ was the first single-chip **10BASE-T** controller to put 10Mbps Ethernet on standard unshielded twisted pair wire. And our newest 16- and 32-bit solutions are making the first "Network Ready" PCs, MACs and peripherals a reality. National is also developing solutions to simplify the role of **NETWORK MANAGEMENT.** Our Product of the Year Award-winning RIC™ + SONIC™ chipset is the first to fully support the IEEE 802.3 mandatory and optional repeater management requirements. We're



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		20ns	x1, x4
	4M	20ns	x1, x4, x8
☐ DRAM	4M	60ns	x1, x4
		70ns	x8, x9, x16, x18
	16M	60ns	x1, x4
☐ VRAM	2M	70ns	x8
☐ SRAM	256K	55ns	x8
	1M	70ns	x8

NEC is the front-runner in memory design because we give you more speed and more choice, including low-voltage and thin-package options. For memories fast enough to keep pace with the future, call NEC today.

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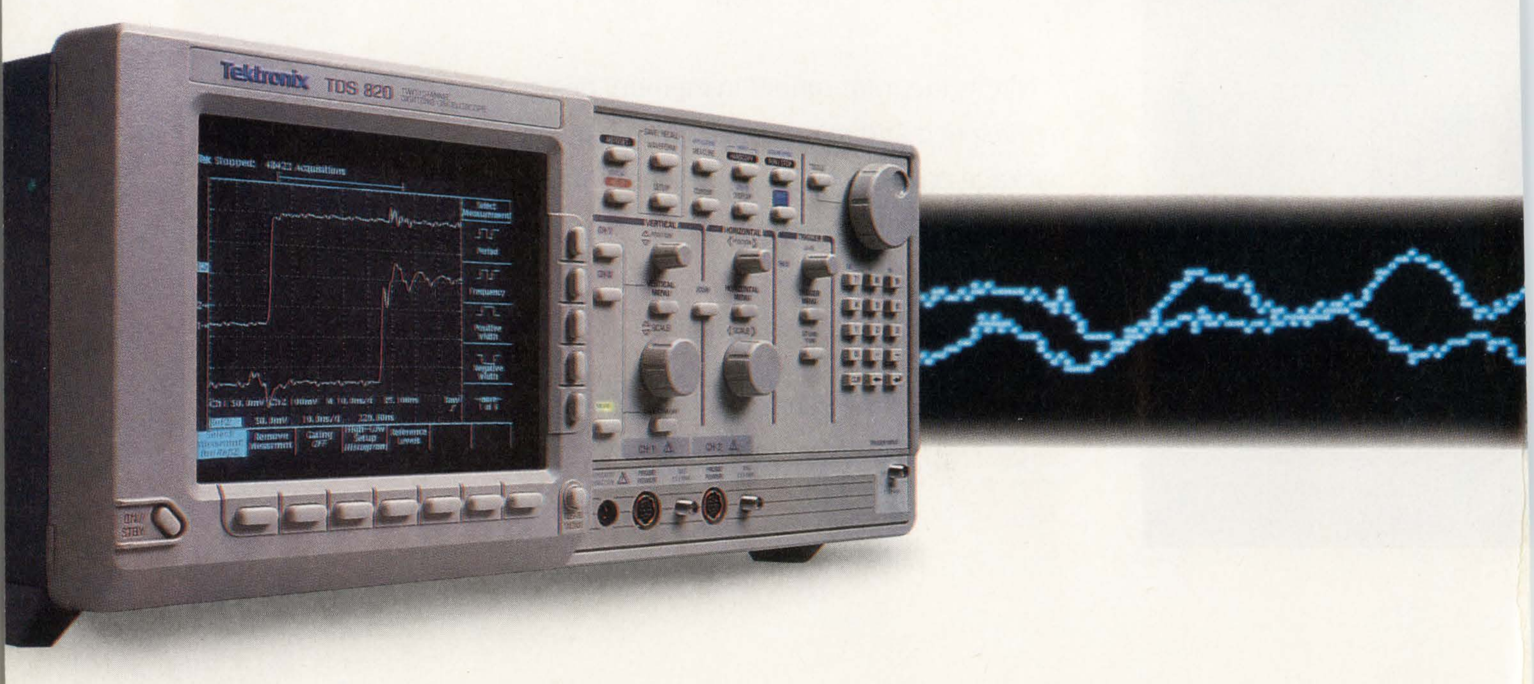

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With Four Times The Performance Of The Competition, Nobody Else In The Field Is Even In The Running.

Our innovative controllers keep you on the fast track of communications.

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2- and 8-Channel Controllers

The ESCC8 also supports a wide range of protocol options—including X.25 LAPB, ISDN, LAPD, HDLC, SDLC, and both ASYNC and BISYNC—plus easy adaptability to either Intel® or Motorola® microprocessors through the use of a 16-bit data bus interface. For fast, reliable and accurate multi-protocolling.

A New Breed Of Performance ICs.

With 16- or 32-bit CRC handling and 28 programmable universal I/Os, the ESCC8 gives you superior performance in a communications controller. And only the ESCC8 offers a collision detect resolution scheme which provides multiple masters on one bus to prioritize data instructions, plus 64-byte FIFOs per channel for increased storage capabilities.

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For an ESCC8/ESCC2 evaluation kit, or more information on our full line of innovative communications ICs, call **800-456-9229.** And put yourself on the fast track of communications.

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CIRCLE NO. 34

CAE TOOLS FOR WIRELESS SYSTEMS

System simulators meet wireless challenges

DOUG CONNER, Technical Editor

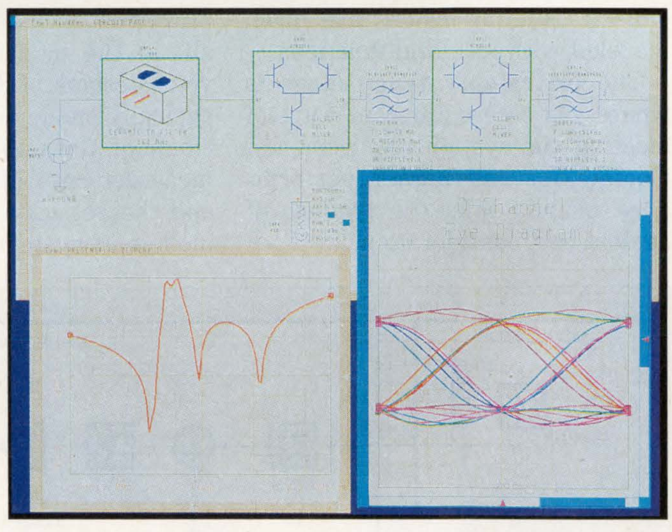
Designers of wireless RF and microwave systems can turn to specialized software tools to help them simulate complex systems efficiently.

Simulating wireless systems requires tools that have the flexibility to simulate systems at a rough block-diagram level, yet can also integrate the results of circuit-level simulations. Furthermore, to be useful, a system simulation must run quickly.

Wireless systems are often complex. The complexity stems not just from the demands of high-frequency analog design of transmitters and receivers. Their complexity is due in part to the fact that wireless systems operate within the RF-to-microwave frequency range where there is great pressure from industry and the government to make efficient use of scarce spectrum. The need to preserve spectrum encourages the use of ever more complex communication techniques to squeeze as many channels as possible into a given bandwidth.

Wireless-system designers also face challenges common to other electronic products. Many wireless systems require portability. The lighter, smaller, and less power consuming, the better. Long battery life is important, but even if great strides are made in the energy density of batteries, most portable systems must remain low-power to minimize the exposure of humans to RF and microwave energy. Efficiency is key. Even if you have a wireless LAN that can plug into the wall for power, you want an efficient system to minimize the RF energy in your office.

The unknown environment between transmitter and receiver adds additional difficulties to wireless systems. You don't need someone actively trying to jam your transmissions, a consideration in military applications, to have transmission problems. Multipath signals caused by reflections from terrain or buildings can impair the signal and degrade system performance. You can evaluate the effects of these transmission problems using simulation with appropriate models for the signal impairments.



A 900-MHz CT1 digital cordless telephone simulated with the Hewlett-Packard RF Design System shows the receiver's frequency response from 100 to 2200 MHz and an eye diagram of the demodulated performance.

To design a wireless system that meets a specification, you need to look at all the function blocks working together to really know if you've designed a suitable system. You can't just throw together a simple prototype for RF and microwave work as you might with low-speed analog or digital designs. Simulation or an expensive prototype are your two choices.

If you choose to enlist the aid of simulation during the design process, then you need to focus on the three fundamentals of simulation—models, stimulus, and measurements.

The right model for the job

When you first start a design and are working at the proposal or preliminary-design stage, you may not have specific hardware and detailed models available. You'll often be designing and simulating with generic building blocks for amplifiers, mixers, filters, and whatever function blocks your system requires. These generic building blocks are often modeled with idealized functions.

The preliminary-design stage is where you assess different ways of meeting the system requirements. Complexity and higher performance usually must be traded off against cost considerations.

As the system design begins to stabilize, you want more detailed information out of the simulation, which means you need to start using more refined models. At this point in the design you may still be using functional blocks, but you are modeling the nonideal aspects of those blocks more accurately. Eventually, you may start simulating the system with specific components at the circuit level. If the simulator you are using provides a way to mix high-level functional blocks with circuit-level simulation, you'll be able to make the transition smoothly.

Simulation results are very dependent on how well the models represent the real circuit. With any simulator you'll hope to obtain a library that includes most, or ideally all, of the models you'll need for your designs. Library models are typically made up from combinations of data-sheet information, measurements of actual products, and theoretically derived data. For models of system blocks or circuit elements that aren't available in a library, you'll have to create the models or obtain them from a company that provides that service.

You can often create components models from data-sheet information, as long as the simulator can use models based on S-parameter data or other readily available data. Another way to create models is to characterize the circuit element with a network analyzer or other test instruments to obtain the necessary data.

Special function blocks that let you easily simulate some of the more complex modulation and demodulation techniques can save you considerable time. For example, function blocks that perform the π/4 DQPSK (differential quadrature phase shift keying) modulation and demodulation will make it easier to create a simulation of a system using that communication technique than having to create your own function blocks. The trend toward ever more complex communication standards will make the

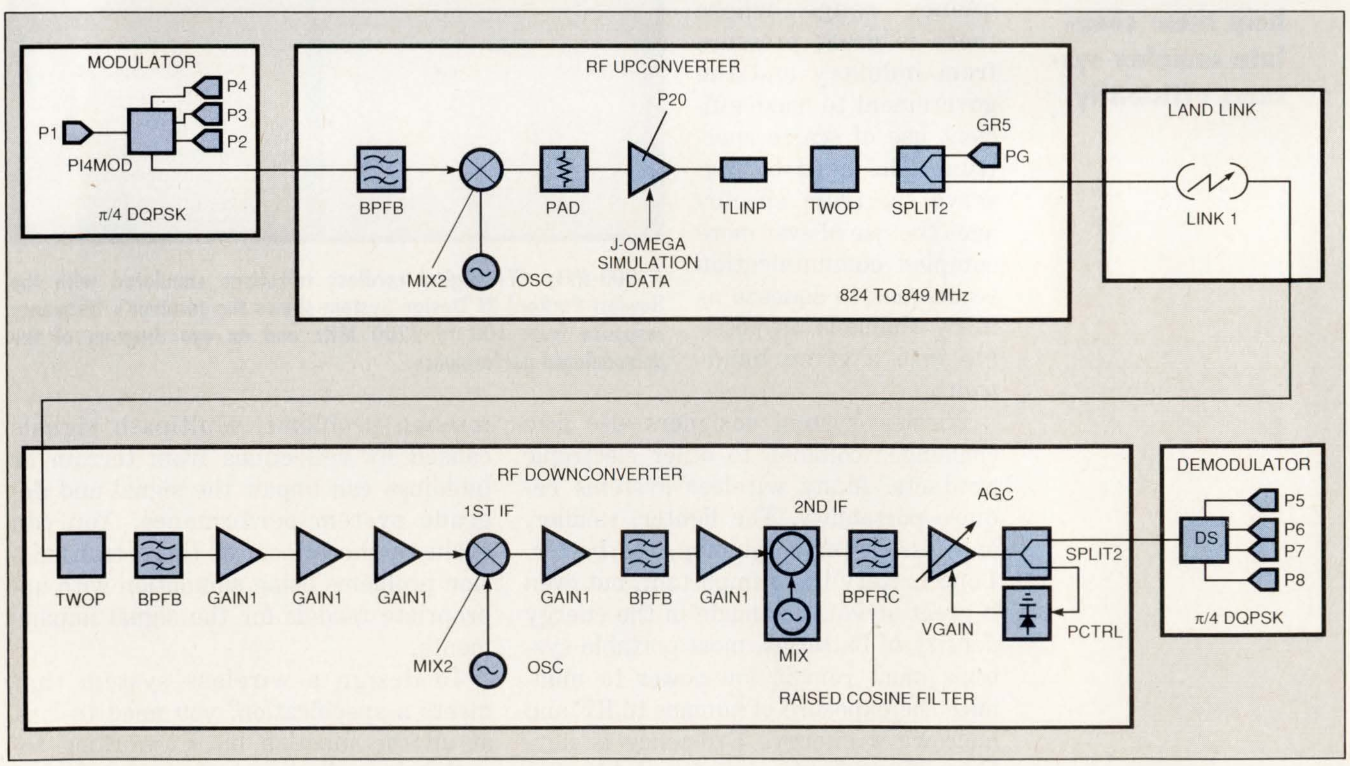


Fig 1—The block diagram shows the IS-54 digital cellular communication system simulated using EEsof's Omnisys simulator.

availability of these specialized modulation and demodulation function blocks even more of an asset.

As your simulation models become more detailed, especially if you start simulating part or all of a design at the circuit-level, simulation times will increase. Different types of simulators not only provide different results, they also vary in the time required to simulate a given circuit.

Linear simulators typically run the fastest. Linear simulation is useful for some parts of systems, but it isn't adequate for general-purpose system simulation. The major drawbacks to linear simulation are the inability to simulate systems through frequency translation devices such as mixers, and the obvious lack of nonlinear results.

Time-domain simulation methods, such as Spice, can provide nonlinear analysis and can also simulate system transients. Some versions of Spice have extensions to better suit them to RF and microwave applications, especially for circuit-level simulations. Simulating a 1-GHz signal requires extremely small (subnanosecond) time increments in the simulation, yet the modulating signal may be in the tens of kilohertz. To simulate the signal for several milliseconds will take many thousands of time increments, making simulation relatively slow.

Spice analyzes all circuit elements in the time domain, whether they

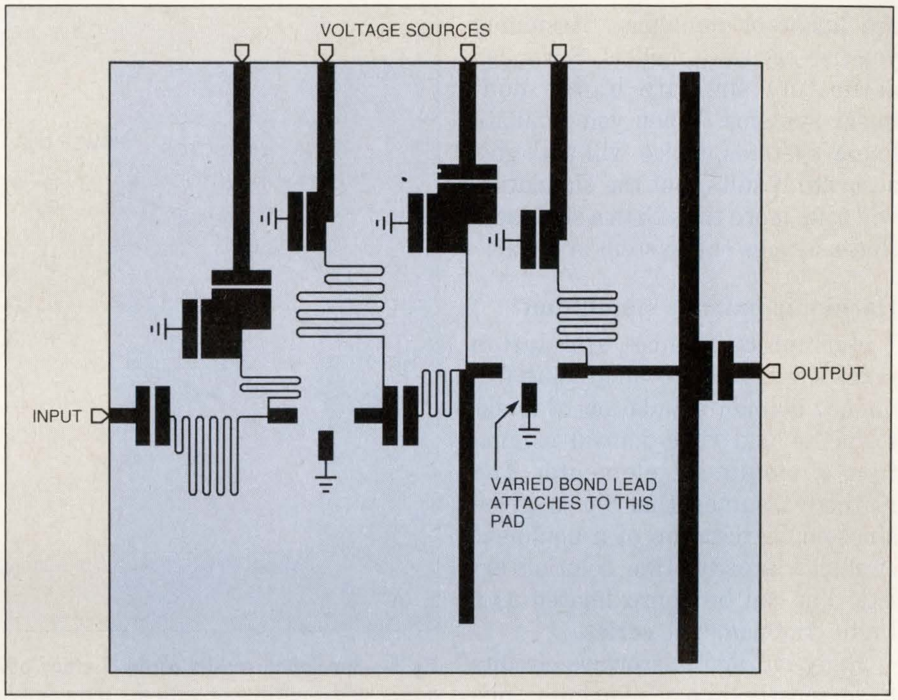


Fig 3—The figure shows the layout of the substrate for the 2-stage power amplifier. Ground symbols are shown for those elements that have vias to the ground plane.

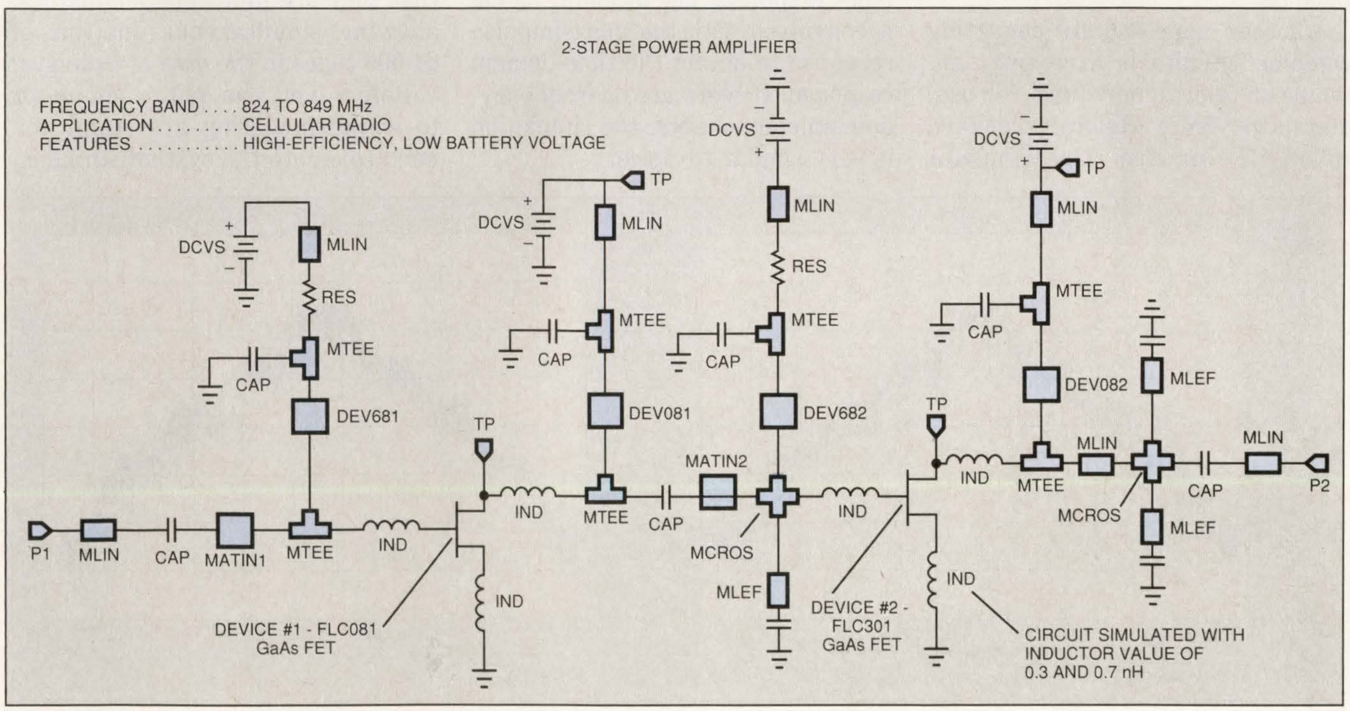


Fig 2—The schematic shows the 2-stage power amplifier module used in the RF upconverter. The inductor indicated is varied in the simulation to determine the effect of changing the bond lead length.

are linear or nonlinear. Assuming you use accurate models, Spice can accurately simulate highly nonlinear systems. When you simulate linear systems, Spice will also give accurate results, but the simulation will take more time than a simulator that assumes the system is linear.

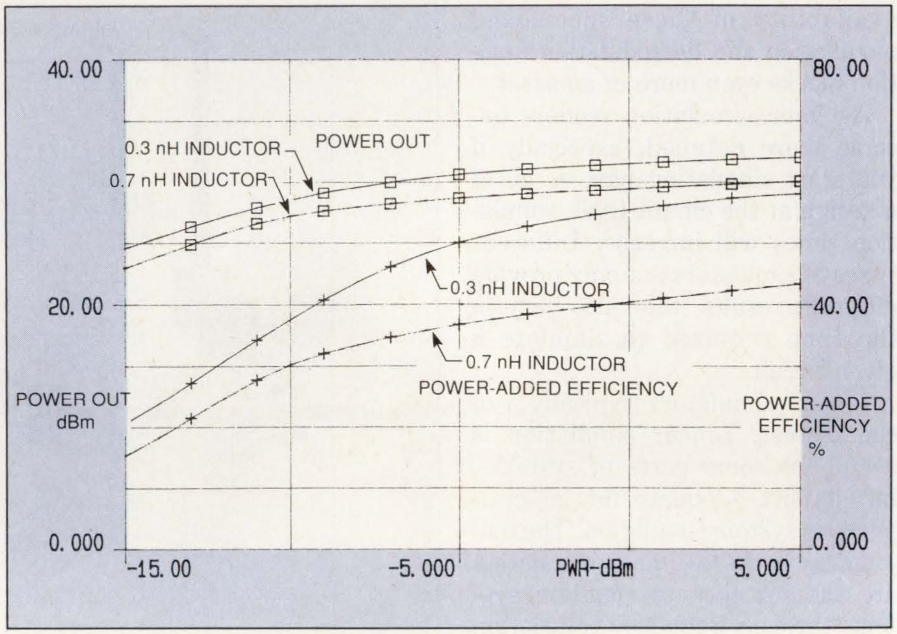


Fig 4—Simulation results of the 2-stage power amplifier show the reduction in gain and power added efficiency with the increased inductance.

Harmonic-balance simulation

Harmonic-balance simulation takes the middle ground, using frequency-domain simulation of linear elements and time-domain simulation of nonlinear elements. The method assumes that for a given sinusoidal excitation of a nonlinear circuit, a steady-state solution exists that can be approximated as a finite trigonometric series.

Many RF and microwave circuits have mostly linear elements, primarily passive components, and only a few nonlinear components such as diodes and transistors. If the steady-state response to a sinusoidal input is what you need, then these mildly nonlinear systems can be simulated accurately and much faster than Spice using harmonic balance.

Another approach to simulating complex circuits is a recently announced (December 1992 release) simulator from Hewlett-Packard called HP Impulse. The simulator incorporates frequency-domain components into a time-domain simulator using a technique that the company calls dynamic convolution. Dynamic convolution converts the frequency response of each frequency-domain component into a finite-impulse response. The incoming signal is convolved with the finite-impulse response to obtain the time-domain response. If there are no frequency-domain components, the simulation is very similar to Spice.

System simulators such as Omnisys from EEsof and Success from Compact operate in the frequency domain. Such simulators cannot simulate system transients, although they can simulate nonlinear elements. Also important is the fact that they are multitone simulators, allowing simultaneous analysis of 64,000 tones in the case of Omnisys.

Before you can put a simulator to work simulating a system, you need to create the system stimulus.

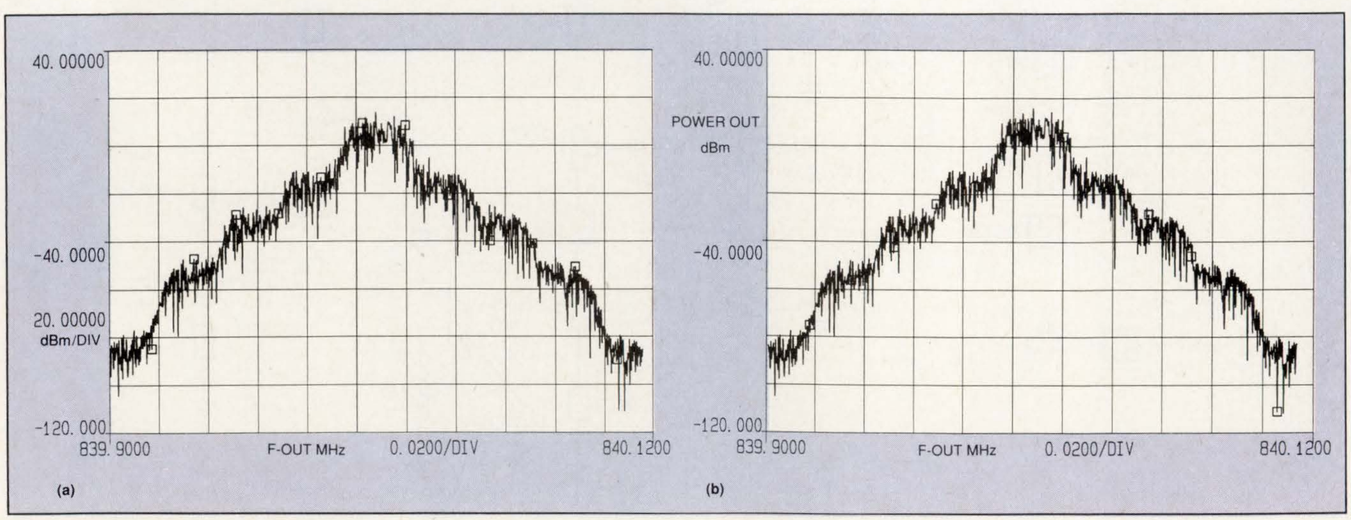


Fig 5—(a) shows the upconverted and amplified spectrum for the circuit with 0.3 nH of inductance and (b) shows the same plot for the circuit with 0.7 nH of inductance.

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CAE TOOLS FOR WIRELESS SYSTEMS

Depending on the type of system you are simulating and where you choose to make the system boundaries, you may be using analog or digital inputs. For digital data transmission, you'll often use pseudorandom bit sequences.

The objective of any simulation is to see how the system performs. You can evaluate system performance easiest if you can get output data in a format that is most useful for you. Standard plots such as power vs frequency, voltage vs time, or frequency vs time are commonly available. Eye and constellation diagrams are information that you may have available from test equipment and may also be valuable during simulation too.

For digital transmissions, the bit-error rate may be the most informative overall measure of a system's performance. If the bit-error rate is poor, you'll need other information to diagnose where the problem lies in the system. Budget analysis methods that look at the contribution of each component or system block and compare them to the total are helpful.

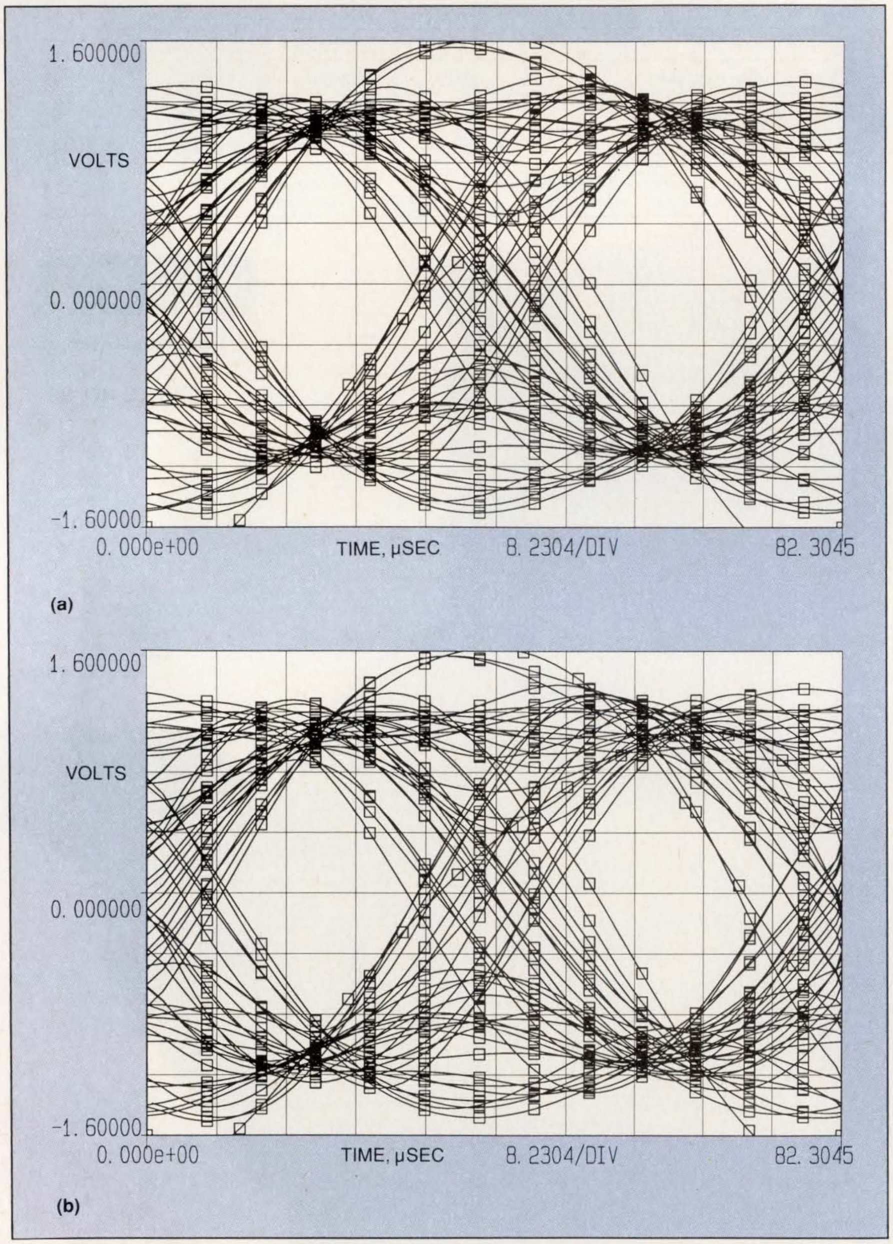

Fig 6—(a) shows the eye diagram of the demodulated signal for the circuit with 0.3 nH of inductance. (b) shows the same plot for the circuit with 0.7 nH of inductance.

DSP methods are having a large impact on wireless communication systems too. Methods that attempt to extract data from a noisy background may be treated as a post processing function on some simulators without DSP function blocks. For these simulators, it's up to you to develop the DSP software algorithm. A more direct approach is to use a simulator that is capable of simulating wireless systems and has DSP function blocks in the simulator.

For example, the Signal Processing Worksystem from Comdisco provides more than 500 system blocks, including many for DSP functions that let you simulate wireless systems. Although the software is capable of simulating complete wireless systems with extensive DSP ability, it concentrates on the baseband signal, the lower frequency signal before modulation, and the lower frequency signal after the demodulation. If you want to simulate the analog details of an RF system between the modulator and demodulator, you'll typically need additional simulation tools, perhaps a circuit-level simulator.

Optimizing for manufacturing

After you've created a satisfactory system design, you can get more utility out of a system simulator that helps you look at manufacturing optimization and yield. By simulating typical component variations, often using Monte Carlo simulation runs, you can see how component variations will affect your design.

Manufacturing optimization methods, such as design centering, help you make sure to choose the

correct nominal component value to achieve the best system performance with component variation. When trying to minimize the cost of a system while achieving some minimum performance level for all systems, manufacturing optimization methods help you know which components to spend money on for tighter tolerances and when you can save money on loose tolerance components.

Simulating designs

An example best demonstrates the value of a system simulation tool for a wireless system. The example shown here is a cellular radio using the IS-54 digital cellular communication standard for North America. The system uses the $\pi/4$ DQPSK modulation technique to transmit data at 48.6 kbps. Radio systems designed to this standard are just now starting to appear.

The simulation uses EEsof's Omnisys system simulator for everything except the power amplifier in the upconverter section is modeled using the company's $29,000 J-Omega RF circuit-level simulator. **Fig 1** shows the block diagram of the system. The system simulator is used in this example as a way to examine how a circuit-level design change in a power amplifier module affects the whole system.

The 2-stage power-amplifier schematic is shown in **Fig 2** and layout of the power-amplifier module is shown in **Fig 3**. The layout shows schematic ground symbols for those elements that have vias to the ground plane. Two simulation runs look at the effect of changing the bond-lead inductance on the source leg of the output-stage GaAs FET.

Table 1—System-level simulators for wireless systems

Manufacturer	Product	Compatible computer systems	Price	Notes
Comdisco Systems	SPW (Software Processing Worksystem)	HP, DEC, Sun workstations	$25,000	Optional software generates DSP code or VHDL netlist for synthesis of DSP functions. Optional network and protocol simulator.
Compact Software	Success	PCs under Windows or OS-2	$8000 to $10,500	The company also offers circuit-level simulators.
EEsof Inc	Omnisys	Unix-based workstations from HP, DEC, Sun, IBM. PCs under OS-2.	$25,000 (US typical system price)	Unix-based X-Window interface. The company also offers circuit-level simulators.
Hewlett-Packard	Microwave Design System	Workstations from HP, DEC, Sun, IBM. 386/486 PCs.	$31,000	A circuit-level simulator that uses system-level function blocks for system simulation.
	RF Design System	Workstations from HP, DEC, Sun, IBM. 386/486 PCs.	$28,093	A circuit-level simulator that uses system level function blocks for system simulation. Available in December 1992.
Tesoft Inc	TESLA	PCs	$695	

Note: VHDL = VHSIC Hardware Description Language.

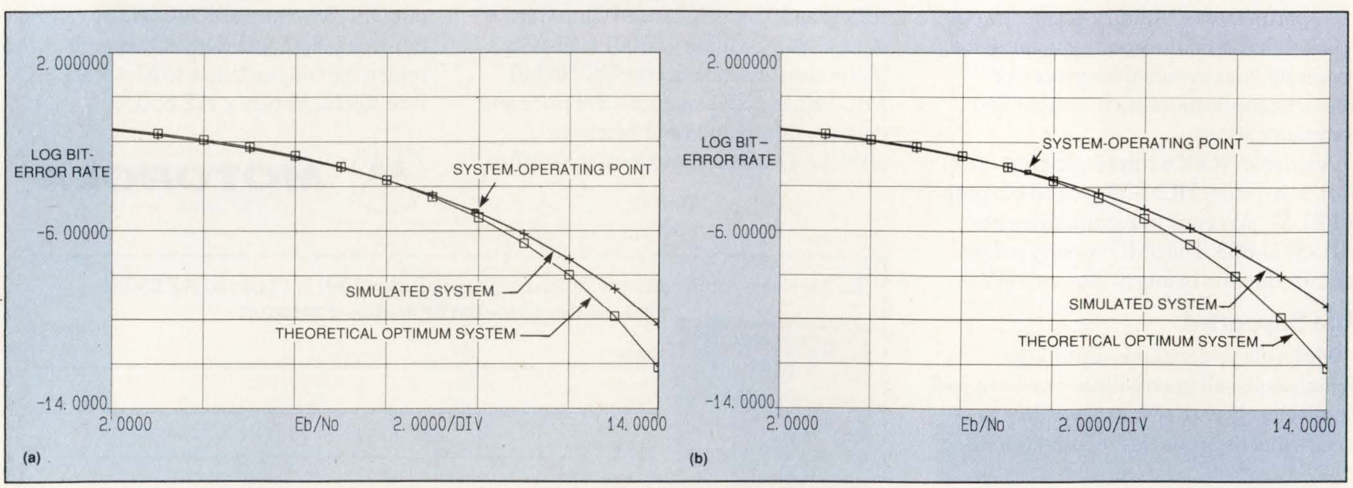

Fig 7—(a) shows the change in bit error rate as a function of the energy per bit per noise output density for the circuit with 0.3 nH of inductance. (b) shows the same plot for the circuit with 0.7-nH of inductance. Note how the system operating point has moved between the two plots, indicating a much higher bit error rate for the 0.7-nH inductance case.

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Simulating the system with a bond-wire inductance from 0.3 to 0.7 nH is equivalent to a bond-wire length of 12 to 28 mils. A circuit-level simulation of just the 2-stage power amplifier provides the data in **Fig 4**.

You can see by comparing the two curves that the output power of the amplifier for a −5-dBm input changes from approximately 31 to 28 dBm with the increased inductance. The power-added efficiency (a ratio of the power out to the dc and RF power in) drops from about 50% at −5-dBm input power to about 37% with the added inductance. The power efficiency reduction is particularly significant for portable handheld units where battery life is important.

The data from the above circuit-level simulation is imported into the system-level simulation using a power-dependent S parameter file. Now you can use the full system-level simulation to evaluate how the power-amplifier change affects the performance of the full system.

The power vs frequency plots in **Figs 5a** and **5b** show a small change. The eye diagrams in **Figs 6a** and **6b** show only a small closing of the eye. The qualitative measurements shown in **Figs 5** and **6** might lead you to believe that the system performance has not been significantly altered by the increased inductance.

The bit-error rate tells a different story. **Figs 7a** and **7b** show the change in bit-error rate as a function of the energy per bit per noise output density. The curves marked with the small squares show the theoretical system performance, and the curves marked with the plus signs show the performance of the simulated system.

Although the inductance variation causes only a small divergence at high levels of Eb/No, the system's bit-error rate is significantly affected by the change in operating point. The change in the system's operating point is caused by the lower gain of the amplifier reducing the energy-per-bit value. The bit-error rate of the system changes from approximately one error in 100,000 bits to one error in 3000 bits. EDN

Acknowledgment

I'd like to thank Tim Hopple of EEsof for providing the simulation of the IS-54 digital cellular system.

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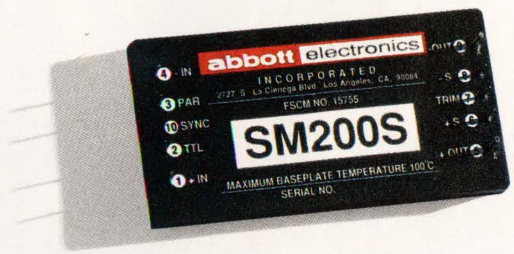

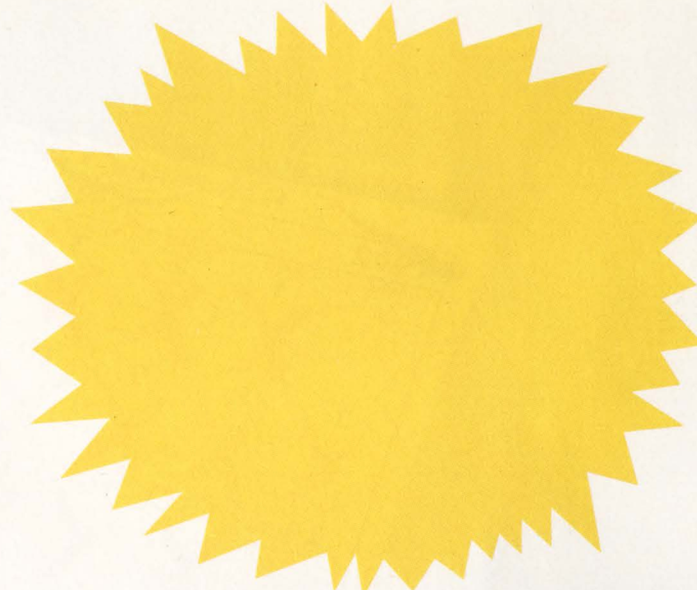

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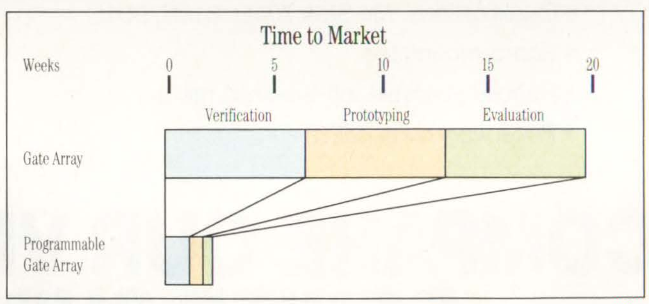

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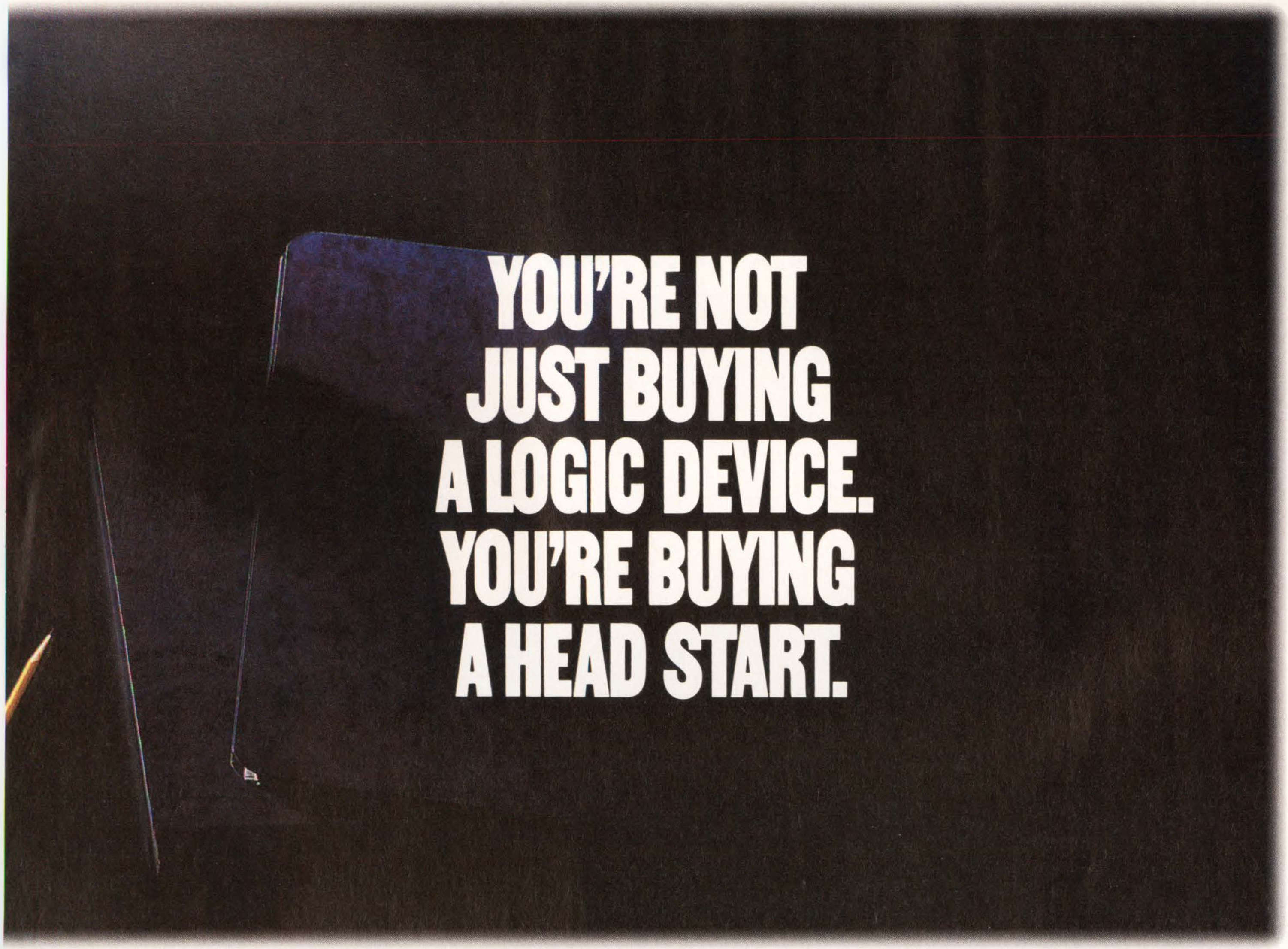

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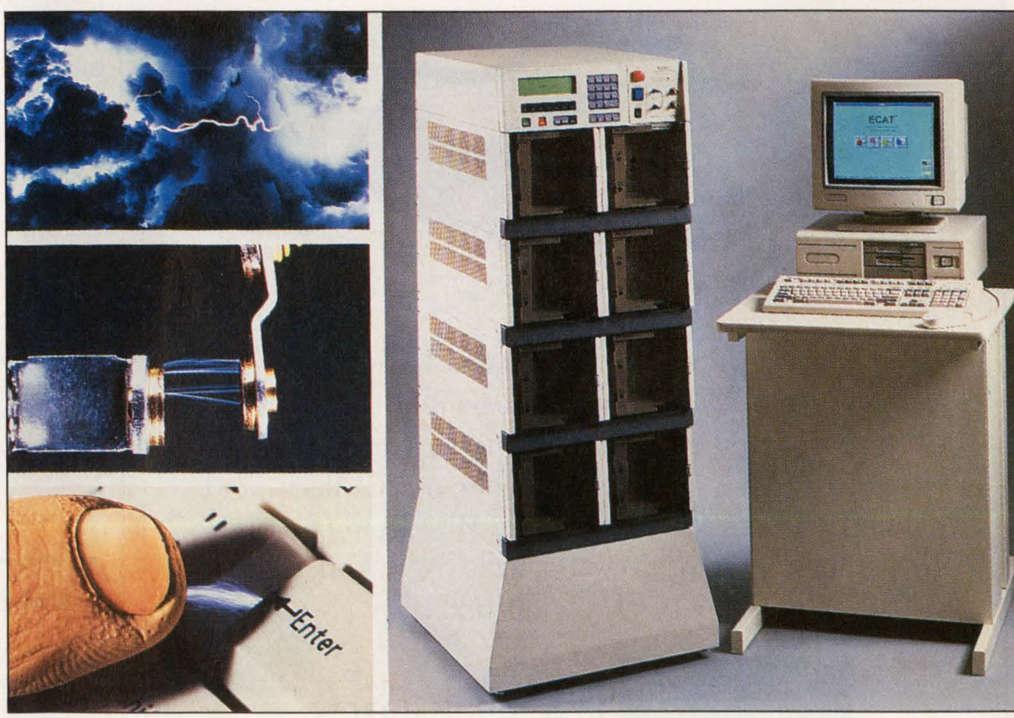
An irony of electronics is that, despite binary signals' high noise immunity, common types of electromagnetic interference (EMI) are more likely to cause malfunctions in modern digital products than in older analog gear. A group of threats—electrostatic discharge (ESD), electrical fast transients (EFTs), surges, and power-line disturbances—can create problems for which neither the true causes nor the remedies are obvious. Keytek's ECAT systems (for expert computer-aided test) not only simulate these threats but include optically coupled data-acquisition modules to accurately monitor signals within equipment *while* you apply the threats. Combining simulation and monitoring facilitates finding the causes of failures and fixing them.

If you think that manufacturers of products such as process-control, communications, and military equipment are the only ones concerned with EMI susceptibility, you're wrong. Concern is growing even among manufacturers of consumer products. The International Electrotechnical Commission (IEC) has promulgated a series of test standards (IEC 801-2, -4, and -5), and the European Community (EC) is getting ready to require that several types of products sold in Europe comply with them. In the US, at least one large retail chain requires manufacturers of products sold under its name to certify that the products meet the US equivalents of these standards.

One reason for the great emphasis on EMI immunity is the growing pervasiveness of digital technology; microprocessors have found their way even into such commonplace items as vacuum cleaners. Most digital systems contain circuits that respond to fast edges, which are among the most prevalent of EMI threats; analog equipment rarely had enough bandwidth to respond—some of these edges are as short as a few tens or hundreds of psec. Although some EMI-induced failures are relatively benign (you can correct them by turning the equipment off and then on again), some necessitate costly repairs, and others are life threatening.

Many of the threats are truly massive—kilovolt-level transients, for example. Because the ECAT systems' µP-based Fibersense data-acquisition modules let you monitor both digital and analog signals (including low-level signals) within your product in the presence of disturbances produced by the systems' simulation modules, you can learn exactly what circuits or subsystems malfunction and quickly devise remedies. Heretofore, the only alternatives were tedious series of experiments, which, with luck, would lead you to deduce the problem.

The systems' simulation modules fall into four categories: the E200 series for ESD, the E400 series for EFT, the E500 series for surges, and the EP series for power-line disturbances (the vendor uses the trademark PQF, for power-quality



Electromagnetic interference from sparks, as from a finger to a keyboard (top left), from the opening and arcing of an ac-line contactor (center left), or from lightning—even when it jumps between two clouds and doesn't strike the earth (bottom left)—can play havoc with your equipment. The ECAT system (right) simulates all of these threats and enables you to find out exactly why your product fails.

faults). Of these, ESD, usually from sparks to the chassis of the equipment under test, is best understood. EFT refers to very fast or very-high-frequency transients, normally of relatively low energy, coupled onto signal or power lines from power switching. Surges, which originate in lightning or power switching, are somewhat slower but have much higher energy (currents can be as high as several kA). They most often appear on power lines but can sometimes couple into signal lines. PQFs are dropouts, dips, and other anomalies on the ac line, usually lasting for several cycles.

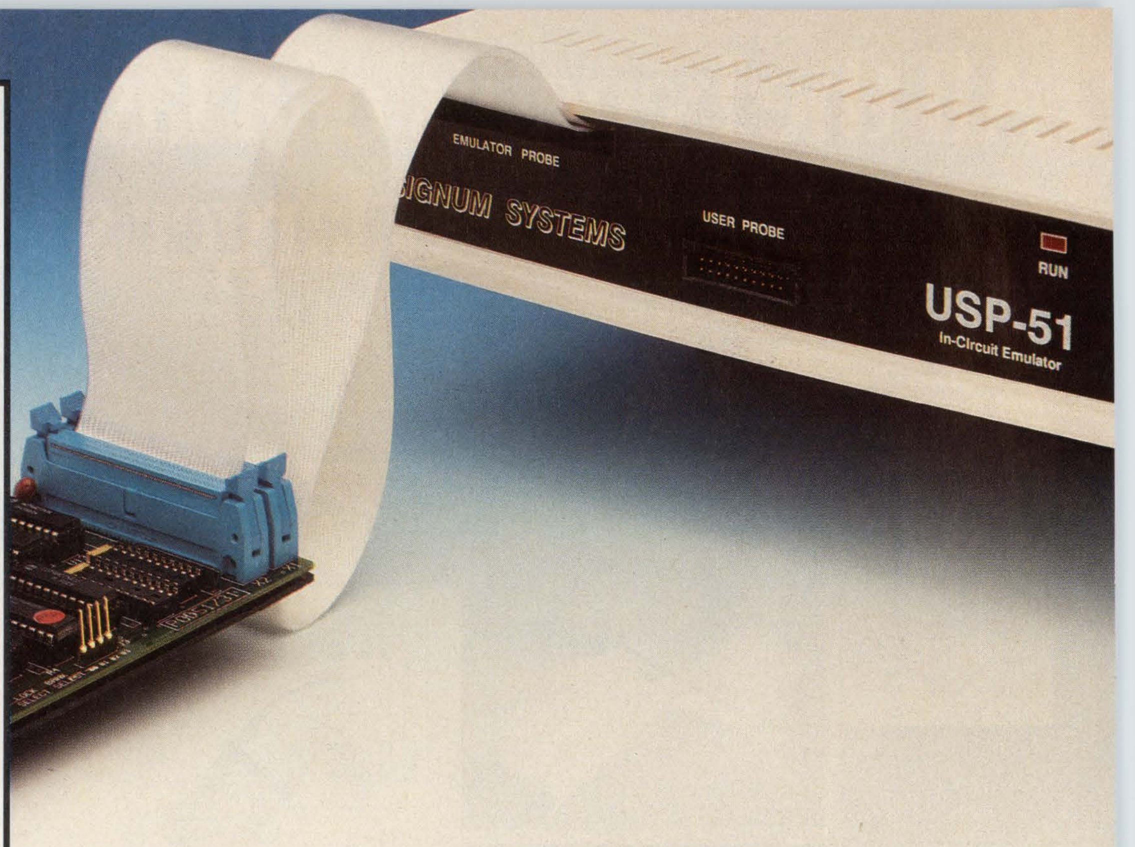
ECAT systems consist of a controller and one or more simulator modules either in a free-standing arrangement or, in larger configurations, in a 19-in. equipment rack. You can upgrade a system's capabilities at any time by adding modules. Adding modules requires no change to the existing ones. The µP-based controller's keypad and 8-line × 40-character LCD let you completely control the system without a host computer. However, MS-Windows-based software allows remote control of all system functions from a host PC. Pricing begins at $22,630. A system with EFT, surge, and PQF simulators costs $67,170. Shipments have already begun.—**Dan Strassberg**

Keytek Instrument Corp, 260 Fordham Rd, Wilmington, MA 01887. Phone (508) 658-0880. FAX (508) 657-4803. TLX 951389.

Circle No. 700

What's Coming Up In EDN

Beginning in the October 1 issue, EDN Magazine will show you how to "Design It Right." In this four-part series, we'll relate the do's and don't's that are essential to good product design. Many of these techniques may work for you!



Universal 8051/52 Family	
Intel 8031	32 MHz
Intel 8032	24 MHz
Intel 80C31	32 MHz
Intel 80C32	24 MHz
Intel 80C51FA	16 MHz
Intel 80C152	16 MHz
Intel 8048/49/50	11 MHz
AMD/Siemens 80515	16 MHz
AMD/Siemens 80535	16 MHz
AMD/Siemens 80C535	16 MHz
Siemens 80537	16 MHz
Siemens 80C537	12 MHz
Siemens 80C517	16 MHz
Signetics/Philips 80C451	16 MHz
Signetics/Philips 83C451	16 MHz
Signetics/Philips 87C451	16 MHz
Signetics/Philips 80C552	16 MHz
Signetics/Philips 8XC552	16 MHz
Signetics/Philips 83C751	16 MHz
Signetics/Philips 87C751	16 MHz
AMD 80C321	16 MHz
AMD 80C325	16 MHz
AMD 80C525	16 MHz
AMD 87C525	16 MHz
Intel 8096/196 (KB, KC, KR, KQ, JR, JQ)	
8096/80196	16 MHz
8098/80198	12 MHz
Zilog Z8. Super-8	
Z8	20 MHz
86C94	30 MHz
Super-8	20 MHz
Texas Instruments DSP's	
320C10/15	33 MHz
320C16	35 MHz
320C17	20 MHz

Let's talk real 8051 8096/196 in-circuit emulation. . . . and DSP's too!

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* System capable of 32 MHz; actual emulation speeds limited by currrent device speeds.

CIRCLE NO. 44

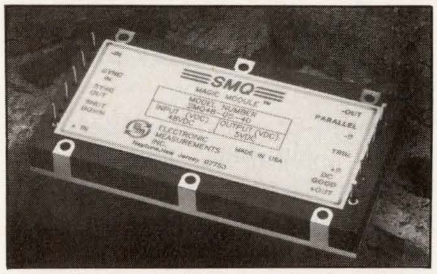
Modular dc/dc converters develop 3.3 to 48V outputs

SMQ Series high-density dc/dc converters reflect the industry's most popular mounting, dimensional, pinout, and cooling specifications. More than 100 models are available with inputs ranging from 12 to 300V and outputs covering a 3.3 to 48V range. Special versions with 1.2V outputs are available for applications such as backplane termination. Output power capability ranges from 75 to 230W—equivalent to a power density of 40W/in.^{3}

The SMQ converters operate at a fixed frequency between 250 and 300 kHz—a range where low equivalent-series resistance, high-temperature electrolytic capacitors provide low ripple and six times more capacitance than typically found in many competitive units. As a result, SMQ converters have a guaranteed transient response—a characteristic always expected of high-performance, higher-power computer or telecommunications supplies.

Responding to market trends toward fault-tolerant (redundant mode) applications, SMQ converters have single-wire paralleling. To help in fault isolation, they also have a dc-good signal as a standard feature. This feature is almost always found in more expensive, higher-power, off-line power supplies.

The units in the SMQ line rely on a time-proven PWM forward converter with current-mode control. Using a 2-transistor forward converter lessens MOSFET capacitance losses and helps make the power section bullet-proof in terms of susceptibility to overvoltage damage. Limiting the operating frequency to 300 kHz sharply reduces capacitance-related losses, which inherently occur at 750 kHz or higher.



Housed in an industry-standard package, SMQ dc/dc converters feature a 230W output capability. They are available with outputs of 3.3 to 48V and incorporate single-wire paralleling and protection against overvoltage, overcurrent, and overtemperature conditions.

One area of performance often cited by users relates to the differential and common-mode noise that often appears at the output as spike noise. This noise is caused by the power semiconductor switching transitions. In the SMQ converters, a proprietary noise filtering technique significantly reduces this noise.

All SMQ converters incorporate overvoltage, overtemperature, and overcurrent protection along with remote shutdown, option synchronization, and a standard on-status signal to indicate proper drive-chip operation. A preset turn-on delay lets the converters drive incandescent or highly capacitive loads without going into an overcurrent mode—a definite problem with fast turn-on converter designs.

SMQ converters are housed in a 2.4×4.6×0.5-in. encapsulated package, which is compatible with either surface-mount or through-hole assembly operations. The units use planar magnetics and can deliver a 230W output at an 85°C baseplate temperature. $125 to $250. Delivery, six to eight weeks ARO.

—Tom Ormond

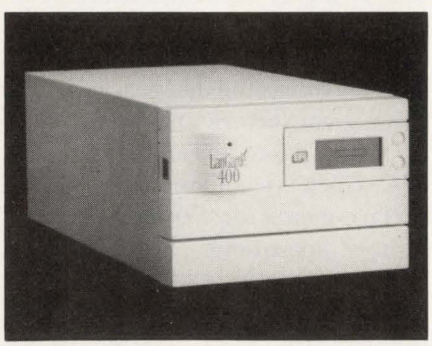
Electronic Measurements Inc, 405 Essex Rd, Neptune, NJ 07753. Phone (908) 922-9300. FAX (908) 922-9334. **Circle No. 733**

Intelligent supplies have power-out warning

Targeted at local-area-network (LAN) applications, Langarde uninterruptible power supplies (UPSs) are available in 400-, 600-, 900-, and 1250-VA models. The smart units feature power-outage warning, advance battery-condition monitoring, and orderly network shutdown. The units also incorporate batteries that the user can replace in 60 sec.

Langarde systems meet the UL1778 rating as a UPS and UL1449 as a transient-voltage surge-suppression device. Suppression circuitry tracks the ac sine wave and provides an effective clamping barrier of less than 50V. The units operate as a line-interactive UPS with a response time that provides 15 minutes of sine-wave output power when connected to a 386 workstation. A boost feature eliminates battery discharge during brownouts.

During a power outage, the Langarde UPS uses the company's Nettrax software interface to automatically notify the LAN administrator of the outage. If no one shuts the network down, the UPS automatically saves files and shuts down any connected equipment. Langarde network power-management software is compatible with windows and supports all major LAN operating systems.



Targeted at LAN applications, the Langarde UPS line features power-outage warning, advance battery-condition monitoring, and orderly network shutdown. Removable front panels let you locate the units out of the way while keeping the monitoring display and control functions within easy reach.

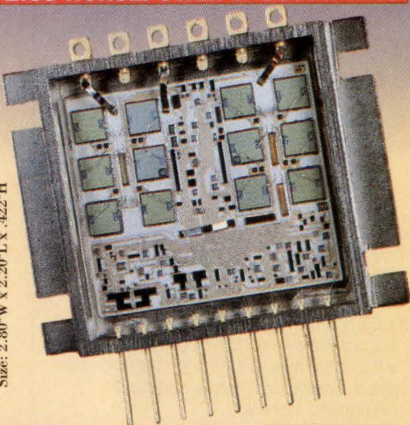
Power-monitoring features include a surge counter and power-disturbance snapshot, which captures power disturbances. Also included is the Mousetrax remote system—a peripheral for control and monitoring of ac power and UPS functions. This system continuously monitors all critical functions—UPS load and temperature, battery condition, charge and uptime, outlet ground and polarity, and surge monitoring. These features can often eliminate the need for expensive power monitoring equipment.

Communication between the Langarde UPS and the workstation happens over the network media or by daisy-chaining the units through the serial port, which effectively creates a local UPS network. This serial network lets the network administrator monitor LAN components, such as file servers and workstations, and equipment that is off the LAN, such as a PBX.

While Langarde is primarily designed for LAN applications, it can also back up single computers. The removable remote front panel lets you place the UPS out of the way while still keeping the monitoring display and control switches within easy reach. $499.95 for the 400-VA version.—**Tom Ormond**

EFI Electronics Corp, 2415 S 2300 W, Salt Lake City, UT 84119. Phone (800) 877-1174. FAX (801) 977-0200.

Circle No. 734



NEWS

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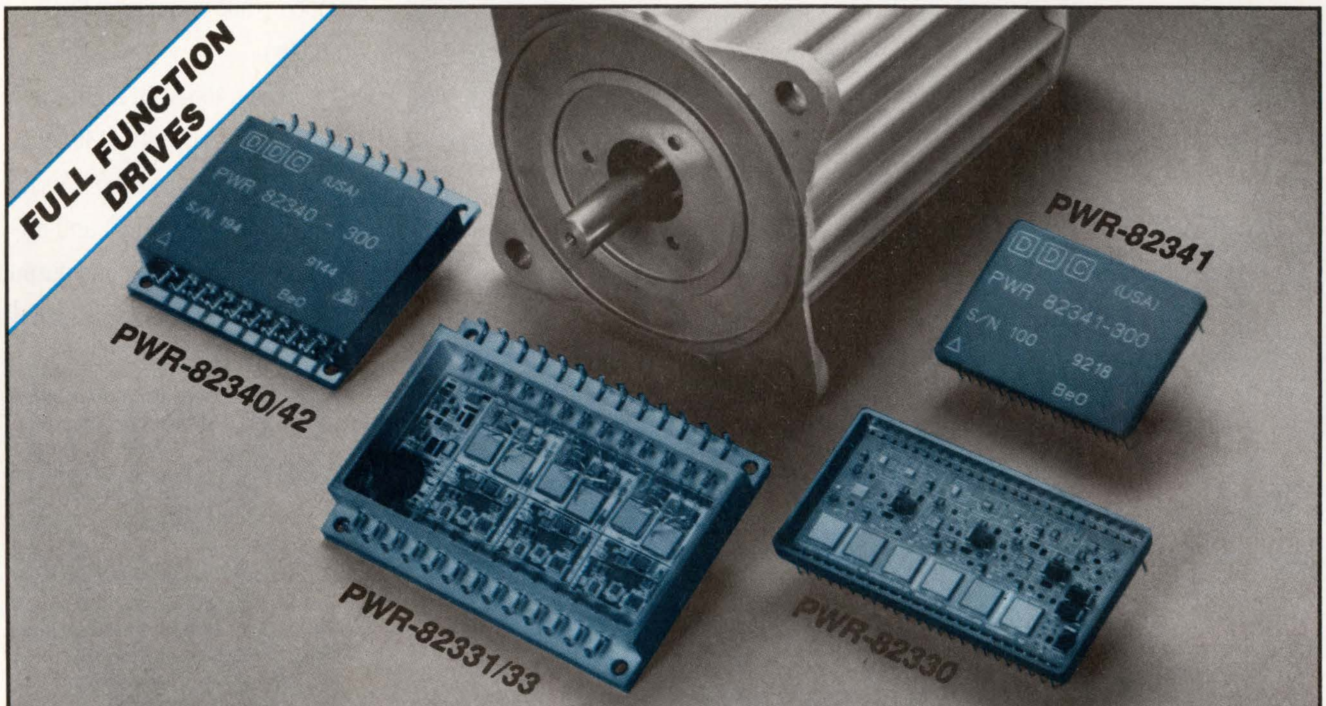

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Our 3-phase drives begin with the 250W PWR-82330, which is designed to operate from a 28V MIL-STD-704 power bus and can deliver 5 amps to the load. This high-efficiency MOSFET drive has a self-contained charge pump, complete gate drive including cross-conduction lock out, and operates from either 5 to 15V input logic signals. Housed in a 50-pin PCB mount package, requiring 3.6 square inches of board space, the PWR-82330 measures only 1.4"W x 2.6"L x 0.25"H.

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Then you need to further upgrade your system to 270V. No problem, use the 10.5kW PWR-82333, 270V drive with an IGBT output stage. This drive is a pin-for-pin, form fit function, high voltage replacement of our PWR-82331. Both drives are available in a 2.1"W x 3.0"L x 0.39"H package and operate from -55°C to +125°C case temperature.

Additionally we offer complementary 2-phase drives with both high and low voltage capability.

Give Bob Fryer a call at 516-567-5600, ext. 7390 (toll free outside N.Y. 1-800-DDC-1772 ext. 7390) to receive more information and become a member of the family. ❑

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CIRCLE NO. 47

16-MHz RISC μP strips down for action

RISC μPs are making it big in the embedded-systems world, especially in printers, X-terminals, and communications gear. In these arenas the push is on for cheaper, minimal RISCs (reduced-instruction-set computers). AMD's newest member of the 29K family, the 29205, aims to please. A stripped-down 29200, the 29205 delivers four native MIPS sustained, on a 16-bit data bus.

The 29200 was designed specifically for printer-type applications. It interfaces to video RAM, produces printer-control signals, and provides a range of peripheral interfaces. The 29205 trims away the overhead for low-cost, down-in-the-dirt applications. The external memory bus is trimmed from 24-bit address and 32-bit data lines, to 22-bit address and 16-bit data lines. Video-RAM support is dropped, as well as burst-mode ROM accesses. ROM chip selects have been trimmed back, and the chip can use only 8- and 16-bit peripherals. These reductions decrease pin count from 168 to 100 pins.

The 29205 has one programmable 8-bit I/O port; you can program the 8 bits to act as external interrupts for control applications. The chip also handles DMA transfers between on-chip (1 channel) or off-chip peripherals (1 channel) and dynamic RAM (DRAM) memory. DMA offloads prevent the CPU from obtaining and moving data to memory.

The 29K family members were originally desktop RISC processors, but missed their market window. The chips were initially structured for Unix, so they have a supervisor and user mode, which is useful for real-time applications and interrupt handling. In addition, the CPUs contain 192 registers, many of which are available for application tasks. The large number of registers helps keep the top of the user stack on chip and provides fast, local storage for processing data.

The original chip also had a branch-target cache, which cached the target addresses of branches to speed up the next iteration of loops. To cut costs, this cache was left out of the 29200 and 29205 μPs. Later 29K family chips added a 4-kbyte on-chip cache.

One of the most respected features of the 29K family is its simple memory interface, which lets the CPU run with standard, fast DRAM, rather than requiring an on-chip or supplemental cache memory. The 29200, and now the 29205, have simplified the 29K memory interface further with an on-chip memory controller that eliminates memory glue logic. The 29205 uses as much as four banks of DRAM, and the ROM controller uses as much as four banks of ROM or static memory with programmable-access characteristics. You can stretch memory-access times by asserting the chip's wait* pin.

The 29205 is code compatible with the 29K family and has a range of development software and tools for the 29K RISC CPU. For evaluating the 29205, AMD supplies the SA29205 demonstration board. The 29205 includes a 16.7-MHz 29205, 512 kbytes of 16-bit-wide DRAM, 1 Mbyte of one-time-programmable logic, 16-bit-wide EPROM, an RS-232C serial interface, and an expansion connector. The board links to a PC host and can be controlled via a ROM monitor, MiniMon29K, in EPROM.—**Ray Weiss**

AMD, 5204 E Ben White Blvd, Austin, TX 78741. Phone (512) 385-8542. **Circle No. 688**

AMD 29205 RISC embedded processor

- 16-MHz, 32-bit CPU
- 192 registers
- 117 instructions with mainly 2-cycle execution (two 16-bit accesses for instruction words)
- No full MPY/DIV instructions done in software
- 4M native MIPS sustained 50% of 29200
- 4-stage, pipelined RISC
- Load/store multiple register instructions for speed
- External memory bus, Harvard architecture with separate 22-bit address and 8-/16-bit data lines
- ROM (8-bit), DRAM (16-bit) controller with DRAM page-mode support
- 2-channel DMA controller
- 8-bit I/O port
- 2 external interrupts, also I/O pins programmable as external interrupts
- UART, bidirectional parallel-port video interface for imaging applications
- Interrupt controller, timer
- 2-port peripheral interface adapter
- In 100-pin PQFP, $38.25 (1000)

8-bit μC drives closed-caption TV

The clock is counting down: By mid-1993, all new TVs (13 in. or larger) must handle closed captions. Motorola's 8-bit 68HC05CC1 will supply a complete TV microcontroller (μC) for TV control, on-screen display (OSD), and closed-caption applications. It makes today's expensive decoder boxes obsolete.

The 68HC05CC1 is pin and function compatible with the 68HC05T2, which many engineers now use for TV and display control. Using the 68HC05CC1, engineers can upgrade to closed-caption processing with a minimum of hardware design. The chip replaces the older chip with only a few wiring modifications. It handles closed-caption processing with up to 34 characters/line and can fill the full screen or present a smaller number of lines that are scrolled or popped up.

Providing closed-caption TV

services requires a controller to monitor the video output to the display. The controller detects line 21 of the TV display, which carries the TV-programmer's closed-caption instructions. These instructions are pulled off the transmitted line and used to direct the closed-caption controller in building and transmitting the captions. The 68HC05CC1 Data Slicer peripheral monitors the signal and pulls off the closed-caption directives, which are then stored in RAM for processing. The slicer (and OSD) trigger off of the horizontal and vertical sync signals: All timing is related to the signals.

A Data Slicer interrupt signals the CPU when it receives a new set of caption directives. Software then sets up the Output Screen Device to put characters at a given scan line. The chip compares the current screen line to the event line. When a match occurs, the characters are scanned and output to the RGB signals. A blanking signal, FBKG, blanks the incoming video, eliminating interference with the character pixel stream.

The closed-caption display characters are defined by the OSD character ROM. Users can program it for special character sets. The ROM defines 128 display characters. Each character is 9 bits wide and up to 13 pixels high.

The chip is built on a simple accumulator-based architecture with a single index register, the 68HC05, which serves as a base for more than 130 variations, many of them application-specific CPUs. The 68HC05 is also popular as a low-end 8-bit μC for replacing control logic and tackling simple control problems.—**Ray Weiss**

Motorola Inc, 6501 William Cannon Dr W, Austin, TX 78735. Phone (512) 891-2000. **Circle No. 689**

Motorola 68HC05CC1 closed-caption μC

- 8-MHz clock, 4-MHz bus cycle
- Accumulator-based architecture with accumulator, index register, and stack pointer
- 16-bit program counter
- 16-kbyte ROM
- 544-byte RAM
- 32-kbyte memory address space for RAM, ROM, vectors, I/O
- 1664 × 9-bit character ROM
- 8-bit pulse accumulator
- Watchdog-timer option
- 8-channel, 6-bit PWM (DAC)
- 1-channel restive ladder A/D converter
- Serial I/O port with I^2C master capability
- Video display outputs (RGB and a signal for blanking video) closed-caption video generator
- Clocks video data in to 28 MHz generated by an internal PLL
- 15 I/O pins
- 45-pin shrink DIP, 40-pin DIP
- Less than $7 (50,000)

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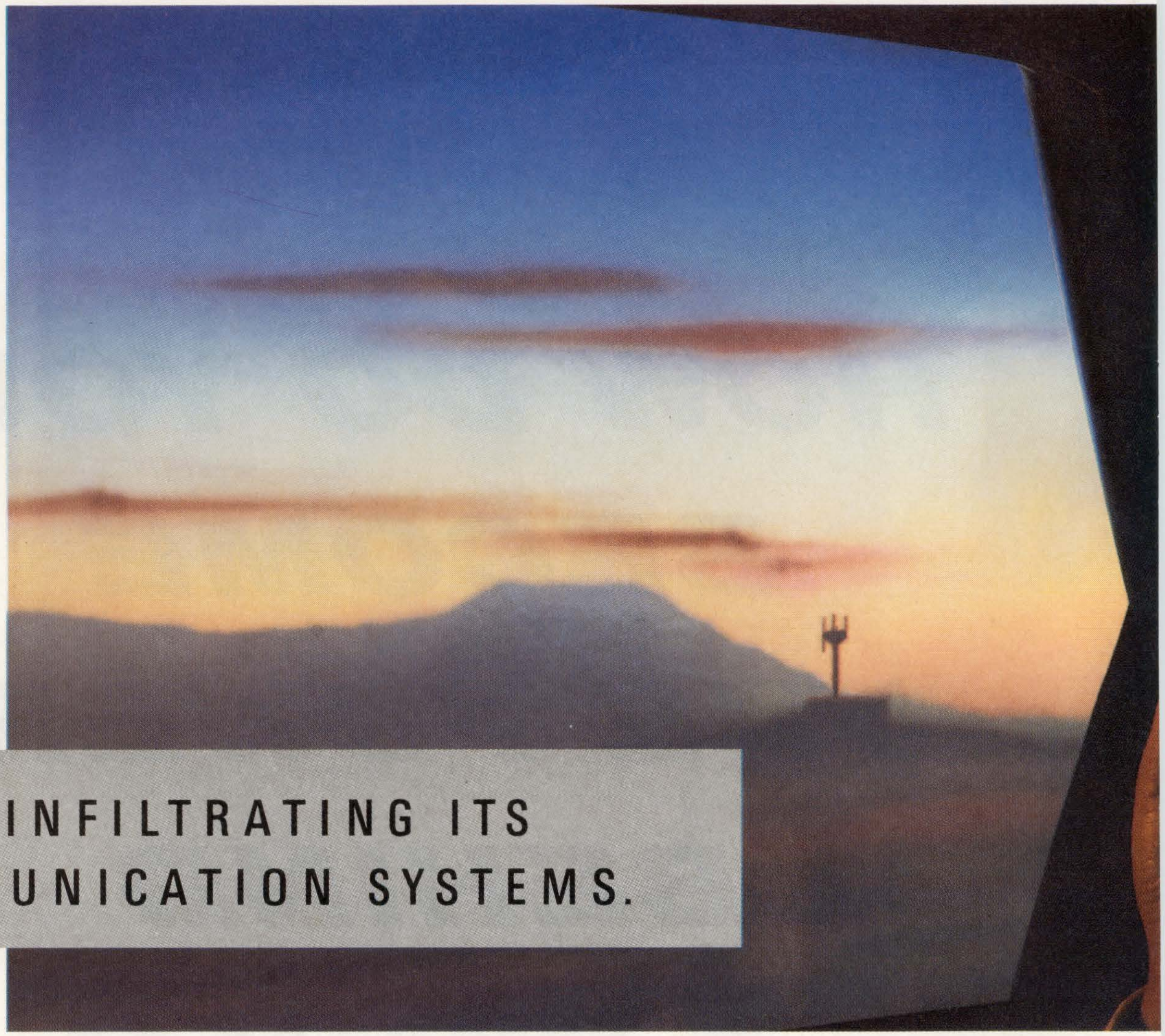

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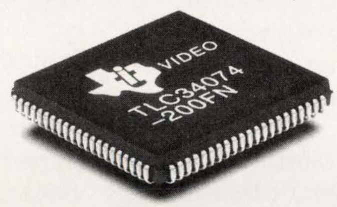
CIRCLE NO. 49

How do you get 1600 x 1280 resolution in an X-terminal design right away?

Use TI's TLC34074 Video Interface.



It's the first 200-MHz video interface optimized for X terminals, enabling 1600 x 1280 resolution at a 72-Hz refresh rate. And it's in distributor stocks now.

The TLC34074 from Texas Instruments integrates a complete grey-scale graphics system back-end onto a single chip, eliminating up to 30 components.

Best yet, it is pin compatible with TI's full-featured TLC34076 palette that supports monochrome to 16- and 24-bit-per-pixel true color. Which allows you to make system cost/performance trade-offs while maintaining a common architecture.

Multiple Speed/Price Options

TLC34074

Designed specifically for B&W/grey-scale applications

Resolution	Refresh Rate	Price (1,000s)	Speed
1600 x 1280	@ 72 Hz	$34	200 MHz
1600 x 1280	@ 60 Hz	22	170 MHz
1280 x 1024	@ 72 Hz	12	135 MHz

TLC34076

True color for X terminals, high-end PCs and workstations

Resolution	Refresh Rate	Price (1,000s)	Speed
1280 x 1024	@ 72 Hz	$45	135 MHz
1280 x 1024	@ 60 Hz	30	110 MHz
1024 x 768	@ 72 Hz	18	85 MHz

More advantages

- Both devices are compatible with virtually any video controller architecture: CISC and RISC microcontrollers, including TI's TMS340 graphics coprocessors, as well as hard-wired controllers.
- Handles Big- or Little-Endian formats with no hardware modifications.
- Direct interface to VRAM and controller.

TEXAS INSTRUMENTS

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CHOOSING COMPLEX

Design methodology, performance, and software tools should all influence you as you seek the right high-density PLD. But first you have to know the foundations of complex PLD and FPGA architectures.

Anne Watson Swager, Technical Editor

Complex PLDs and FPGAs are proliferating, and so are the software tools necessary to work with them. In fact, the task of choosing from such a vast array of high-density programmable logic devices (PLDs) is enough to overwhelm unsuspecting newcomers. However, an overview of the hardware architectures, design methodologies, and other important criteria can help you on your way to choosing the right device for your design.

Not only is there currently a wide assortment of architectures to choose from—both complex PLDs and field-programmable gate arrays (FPGAs)—but the list of such architectures keeps growing. Within the last year, at least three start-ups—Concurrent Logic, Crosspoint Solutions, and Quicklogic—started shipping their FPGAs. AT&T Microelectronics, which currently second-sources a number of FPGA market leader Xilinx's devices, announced a proprietary architecture that will be in full production by the beginning of 1993. Cypress Semiconductor recently announced an agreement with Quicklogic that will potentially lead to wider availability and expanded capability of the latter company's architecture. Motorola (Phoenix, AZ) has announced its intention to enter the FPGA market and, at the time of this article's writing, is close to making its specific plans public. And even Harris Semiconductor (Melbourne, FL) is getting into the FPGA act through an agreement with Xilinx to produce a radiation-hardened version of one of their FPGAs.

Just as there are multiple architectures, so there are myriad software tools, from both IC vendors and third-party vendors, that embody various design-entry approaches, from schematic capture, to Boolean entry, to waveform entry, to hardware-description languages. CAE vendors have been extremely busy introducing all manner of software tools such as retargeters, which take a design intended for one architecture and transform it for another, and device fitters, which take compiled designs and map them to a specific part.

Taking it all in

Absorbing all of the product and tool information necessary to make an informed choice (**Fig 1**) could possibly require more time than an entire design project. Becoming familiar with these devices' architectures is a critical first step. When you start learning about these devices, it is simplest to divide high-density programmable logic into two main camps: com-

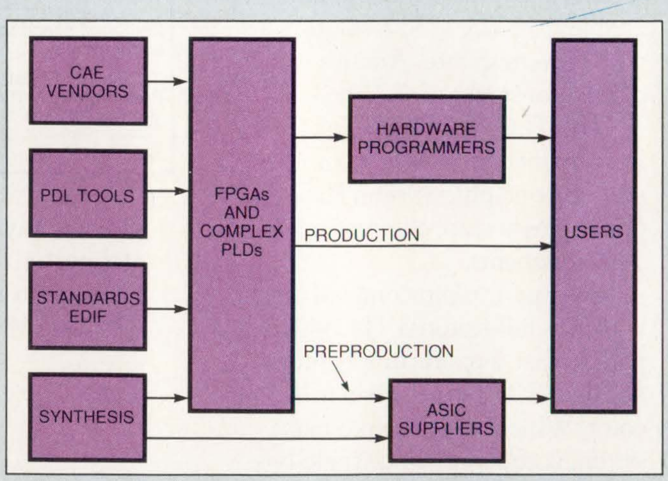
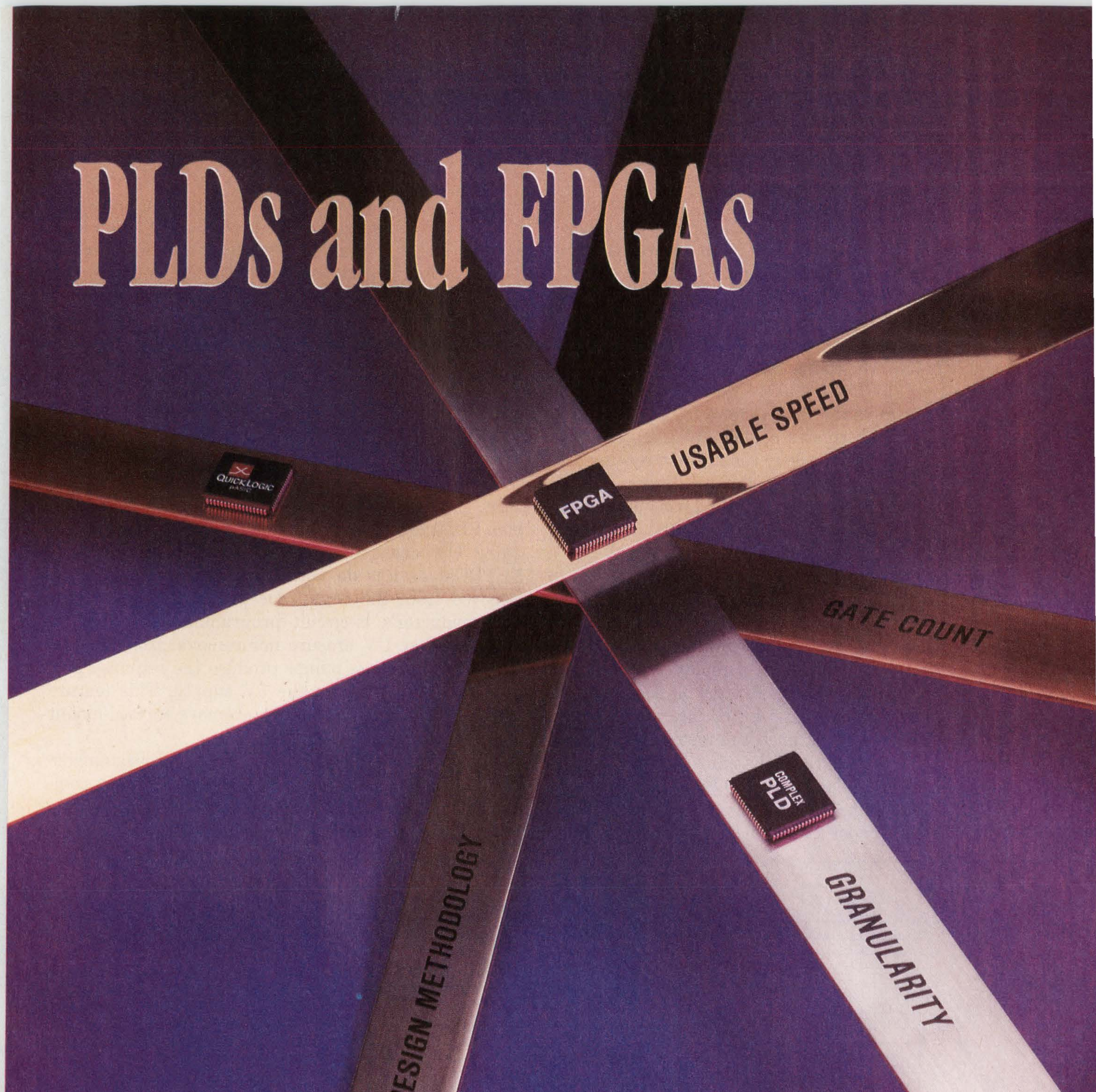


Fig 1—FPGAs and complex PLDs don't exist in a vacuum. Learning about the devices themselves is an important first step, but so is becoming familiar with their dependence on design software, programming hardware, and in some cases, ASIC conversion processes. (Diagram courtesy Actel Corp)

PLDs and FPGAs



The capabilities of computer PLDs and FPGAs do intersect, but different structures mean one or the other may perform a function faster or more predictably. (Photo courtesy Quicklogic Corp)

plex PLDs and FPGAs. Both complex PLDs and FPGAs help you achieve the same goal, that is, to absorb large amounts of standard logic into one device. Using one or the other—or both—for your design requires understanding the strengths of each.

Complex PLDs are essentially large collections of PAL-like structures on one chip. In other words, a complex PLD is a large collection of sum-of-products arrays (**Fig 2a**). The connections between logic and I/O cells are typically fixed, and the devices feature a centralized programmable interconnect. This setup is sometimes referred to as a segmented-array architecture. These devices' relatively constrained routing provides them with one of their main advantages: predictable timing. With some exceptions in terms of architectural features, all complex PLDs share the same basic logic structure.

This last statement absolutely doesn't apply to FPGAs. Grouping diverse devices under the term *field-programmable gate array* makes FPGAs sound as if they all exhibit gate-array-like characteristics. In fact, they are distinguishable from complex PLDs simply because they comprise arrays of logic blocks connected by rows and columns of distributed interconnect lines (**Fig 2b**), which is sometimes referred to as a channeled-array architecture. Any more specific resemblance to each other ends there. Only one FPGA manufacturer's architecture closely resembles a gate array.

Each FPGA vendor's logic blocks and each product family from one vendor contains a different collection of logic and different levels of logic functionality. FPGAs have no predetermined coupling between logic and I/O blocks, although some devices do have a few dedicated inputs such as clock-drive inputs. These devices' unrestricted routing structure provides them with one main advantage: flexibility.

Reprogrammable vs one-time-programmable parts

Complex PLDs and FPGAs use different fabrication and interconnect technology. Most complex PLDs are CMOS-EPROM based or EEPROM based, and the PROM memory bit switches a transistor that controls the configuration pattern of the logic. Thus, no hard-wired physical link exists, and most off-the-shelf complex PLDs are reprogrammable. EPROM versions require UV erasure prior to reprogramming, but EEPROM devices do not, although both have to be removed from the circuit for programming. Lattice Semiconductor's in-circuit programmable device requires neither UV erasure nor removal from the circuit. On-chip charge pumps produce the required programming voltage from the 5V supply. This feature is particularly useful for hard-to-remove surface-mount packages.

Although complex PLDs start out reprogrammable in some form, once a design is established, many companies offer conversions to one-time-programmable versions. Altera offers a third step called MPLD, or

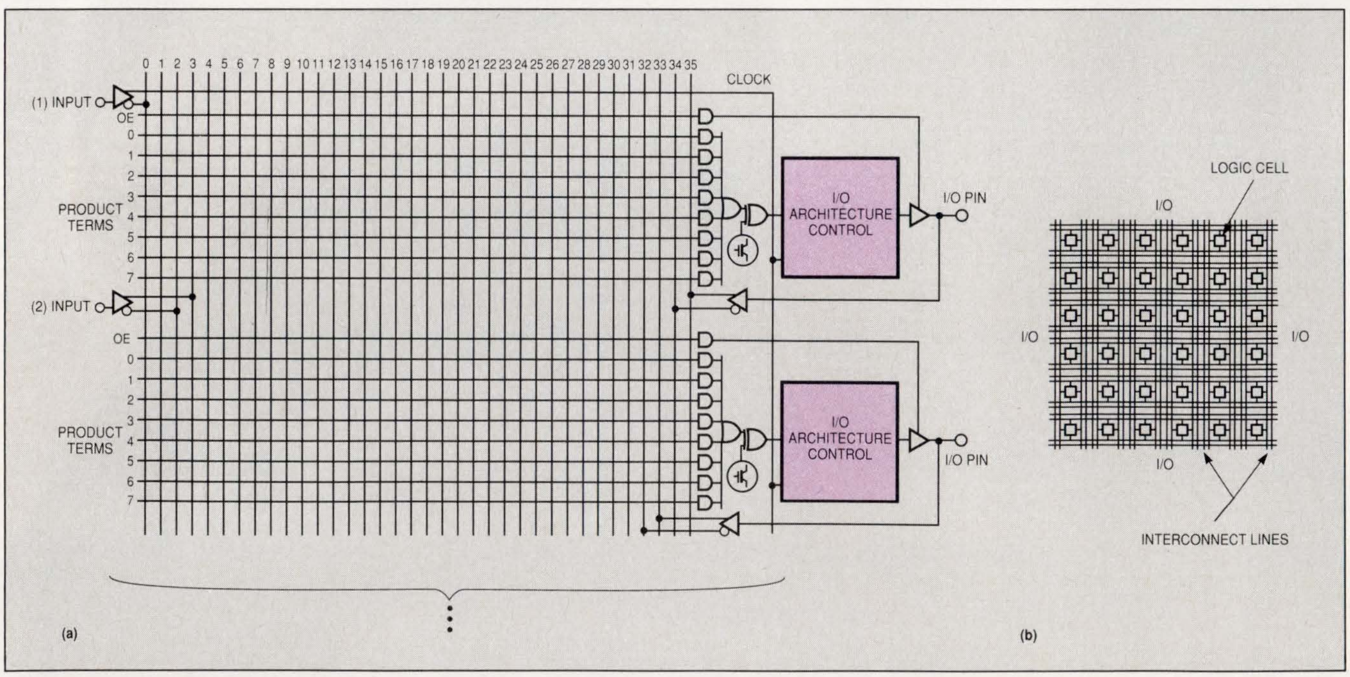


Fig 2—Complex PLDs (a) are large collections of sum-of-products arrays, whereas FPGAs (b) feature an array of identical logic cells connected by rows and columns of interconnect. Not all FPGAs are symmetrical like the array in (b), and internal logic cells and routing structures vary from device to device.

"mask-programmable logic device." These one-time- and mask-programmable versions offer significant price savings.

FPGAs are available in both reprogrammable and one-time-programmable technologies, static RAM and antifuse, respectively. SRAM-based FPGAs, pioneered by Xilinx, and now manufactured by Algotronix, AT&T Microelectronics, and Concurrent Logic, use a memory bit to program connections open or closed on power up. Thus, SRAM-based FPGAs are reprogrammable and volatile. Like some complex PLD vendors, Xilinx also offers a conversion to a one-time programmable device, which the company calls "hardwire." In antifuse FPGAs, pioneered by Actel, and now manufactured by Crosspoint Solutions, Quicklogic, and Texas Instruments (second source to Actel), the high programming voltage establishes a hard-wired physical link. Thus, antifuse FPGAs are one-time programmable.

Basic architectural and technology differences are just two aspects that distinguish complex PLDs from FPGAs. One of the biggest differences between complex PLDs and FPGAs is the design methodology necessary to implement logic functions in each device. Depending on your design perspective, you may have to make some adjustments. If you have experience designing with 7400 series devices, the jump to FPGAs won't be difficult. In fact, Doug Conner, in his hands-on projects (**Refs 1** and **2**), found it to be quite easy. And if you're currently a PAL designer, designing with complex PLDs won't take much of a change in your way of designing and implementing standard logic functions.

However, the jump from PLD design to FPGA design will require some adjustments. FPGAs are very flexible devices, and designing with them involves making tradeoffs. Whereas a complex PLD data sheet can closely predict the final speed of the design, the timing of an FPGA is not at all deterministic. How much of the FPGA a logic design utilizes influences the final speed of that logic. For example, a recent EDN Design Idea (**Ref** 3) shows how you can trade off modules for speed when using FPGAs. This Design Idea shows that using the fewest modules requires the

Benchmarking group grapples with performance comparisons

All vendors of complex PLDs and FPGAs have until now used their own unique ways of quoting system performance for particular designs implemented in their devices. Each of these performance predictions is a type of one-company benchmark—each company uses a different logic implementation to arrive at their performance numbers.

This situation is changing. The Prep Corp (San Jose, CA, (408) 356-2169)—PREP stands for programmable electronics performance—consists of a consortium of IC and software vendors trying to establish a viable benchmarking method. This method should help users make apples-to-apples comparisons of the speed and logical capacities of larger programmable logic devices, namely complex PLDs and FPGAs.

Prep has two essential goals: to help introduce the architecture of different PLDs to users so that they may better understand the factors involved in selecting among them, and to allow experienced users to more quickly evaluate different architectures with respect to a specific design.

The suite of benchmarks includes a set of circuits implemented according to a prescribed methodology for measuring and reporting the capacity and timing measurements. Vendors will measure device capacity by using a "repeat and fill" scheme, whereby they will repeat the particular benchmark circuit as many times as possible, then fill the leftover logic space with filler circuits. Vendors will measure the maximum operating speed of a benchmark circuit by reporting the worst case delay of the circuit's slowest path.

The repeat-and-fill methodology is one of many that the group could have chosen for the benchmarking process. Although the vendors will be at least using the same implementation and measuring procedures to compare the devices, keep in mind that few real designs contain repeated units of the same logic circuits. Thus, it's not wise to use these benchmarks to predict the over all speed of a design that contains a variety of circuits. Clearly, the ultimate benchmark is your circuit implemented in each architecture.

The first suite of benchmarks will include the following circuits: data path, timer/counter, state machine, large state machine, arithmetic circuit, 16-bit accumulator, 16-bit counter, and memory mapper. The small filler circuit is a combination of commonly found logic elements such as 4-bit counters, 4:1 multiplexers, 4:2 encoders, and 4-bit accumulators.

By the time of this article's printing, vendors should be very close to—if not done with—final verification of the benchmarks. Then, final Prep-approved data for each vendor's circuits should be published by the end of the year.

largest number of logic levels, thus incurring the worst-case delay. The idea presents alternative designs that use fewer logic levels and decrease propagation delays at the expense of the module count.

Also, the speed of an FPGA depends on the interconnections between logic blocks and, thus, on the layout of the device. Each design, even each iteration of the same design, can use very different routing paths, the length and resulting impedance of which will heavily impact the speed of a final design. A smaller design can have a more efficient layout leading to more efficient routing and faster performance. A denser design places more constraints on layout and routing, leading to possibly slower performance.

The worst-case scenario that can occur with either complex PLDs or FPGAs is when so much logic space in the IC is occupied that there aren't enough routing resources to allow the necessary interconnections. This problem arises most often when I/O pins are fixed early in the design process.

You can use an FPGA's density-vs-speed flexibility to your advantage, but don't expect to predict how fast or slow an FPGA design will run at the outset. Also, routing efficiency—and therefore the IC's final performance—depends not only on how much of the FPGA a design utilizes, but also on the quality of the place-and-route software. Determining that final performance requires post-layout simulation. Having to use and rely so heavily on these software tools is quite different from working with complex PLDs.

Because there isn't one standard FPGA architecture, studying and understanding each architecture is important for designing optimum circuits with that architecture. In some cases, you'll need to learn more efficient ways of implementing certain logic functions such as state machines. Because few internal connections exist within an FPGA, implementing a design takes two steps: partitioning the logic within the logic-cell structure of the FPGA and connecting the various blocks together using the device's routing resources.

Predictable vs unpredictable performance

Vendors of complex PLDs and FPGAs claim their devices can run at high speeds. However, their numbers are very difficult to judge and compare. One thing that you can bank on however, is that complex PLDs are usually a better choice for designs that have very tight speed requirements, simply because of their deterministic timing. This is not to say that the complex PLD will be the fastest implementation of a design, but simply that the final speed will be fairly predictable at the beginning of the design cycle. Creative FPGA design can result in very fast logic, but it can also require time-consuming attention to placement and routing details of internal logic blocks.

When it comes to implementing circuit applications, complex PLDs and FPGAs each have their strong points. However, each new architecture that debuts modifies those points somewhat. The parts themselves are changing to address some of the deficiencies of previous architectures (as the gray area in **Fig 3** indicates). For example, Xilinx has improved the FPGA decoding situation in its XC4000 family by providing dedicated wide-decoding logic, which is directly coupled to input pins. Also, Quicklogic claims that its architecture is particularly suited to high-speed state machines. Complex-PLD vendors are adding more registers and I/O to their larger devices.

Still, for some applications, the choice between a complex PLD and an FPGA is fairly clear cut (as on the axes in **Fig 3**). Generally, complex PLDs excel at implementing large amounts of combinatorial logic, and

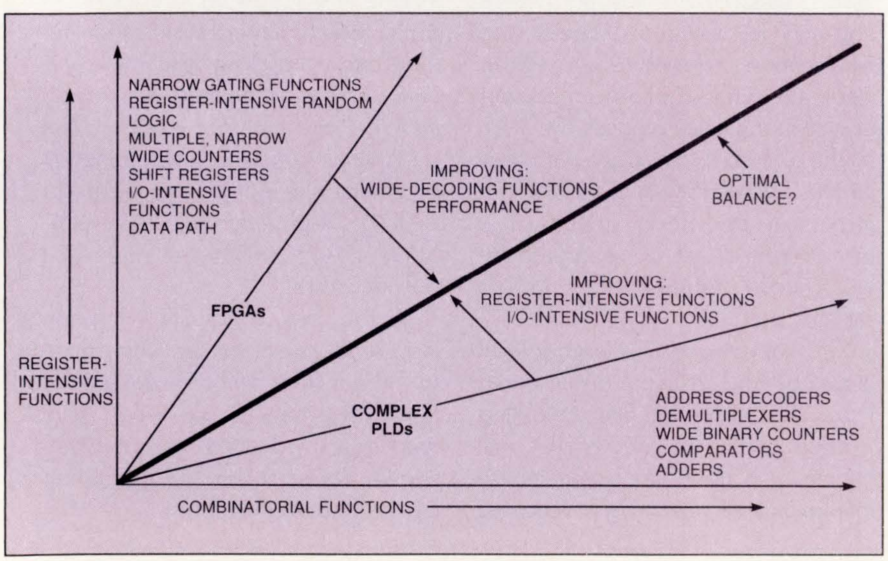


Fig 3—Complex PLDs excel at combinatorial functions. FPGAs excel at register-intensive functions. However, there is some gray area between the two. The parts themselves are improving, and techniques exist to implement logic functions in both device types. (Courtesy Advanced Micro Devices)

FPGAs excel at designs that require large numbers of registers. For example, implementing a large state machine or an extremely wide input decoder in an FPGA wouldn't make much sense because complex PLDs have a wide sum-of-products structure and are perfectly suited to that purpose. Likewise, implementing a design that requires many flip-flops, a register file or common-access memory for example, in a complex PLD wouldn't make much sense because FPGAs contain many more flip-flops than complex PLDs do.

These tradeoffs may be clear cut for a single logic circuit. However, if a design involves a variety of logic structures—if the state machine is only one quarter of the design, for example—the choice between complex PLDs and FPGAs isn't black and white. During the initial design-partitioning phase, you may discover that part of the design works well in a complex PLD and part in an FPGA.

If you must fit a variety of logic types into one device, you can implement the same logic function in both devices as long as you use the right structure for each. Techniques do exist to efficiently implement traditional register-intensive and combinatorial-intensive functions in both complex PLDs and FPGAs.

Techniques fit designs into FPGAs

State machines (**Fig 4a**) and binary counters are two examples that require different implementations to get optimum performance from the complex PLDs and FPGAs. Because of their wide decoding ability, complex PLDs are well suited for maximally encoded state machines, that is, state machines in which a minimal set of variables defines each state (**Fig 4b**). A 4-bit counter is one example of such a state machine—4 bits define a total of 16 states.

However, implementing a maximally encoded state machine in an FPGA is not a good use of the FPGA's narrow decoding, register-rich architecture. A better approach is to use the state-per-bit or one-hot method (**Fig 4c**), first proposed by FPGA consulting firm Highgate Design (Saratoga, CA). In this method, the state of a single, or "hot," register determines the current state. A state machine with 16 states thus requires 16 flip-flops. The input and a small amount of decode logic determine the next state. This approach usually requires fewer logic levels between clock edges than binary encoding and ultimately produces faster FPGA operation. One penalty of this approach is apparent if two registers become active at one time. The design may need extra logic to decode and then prevent such illegal states.

Likewise, implementing a classic binary counter in a complex PLD makes sense. Conventional binary counters use wide fan-in logic to generate high-end carry signals. An FPGA's limited fan-in makes this particular implementation cumbersome. A much simpler structure, the linear-feedback-shift-register (LFSR) counter **(Fig 5)**, sacrifices the binary count sequence but achieves high speed with very simple logic using an FPGA. The counting sequence is the

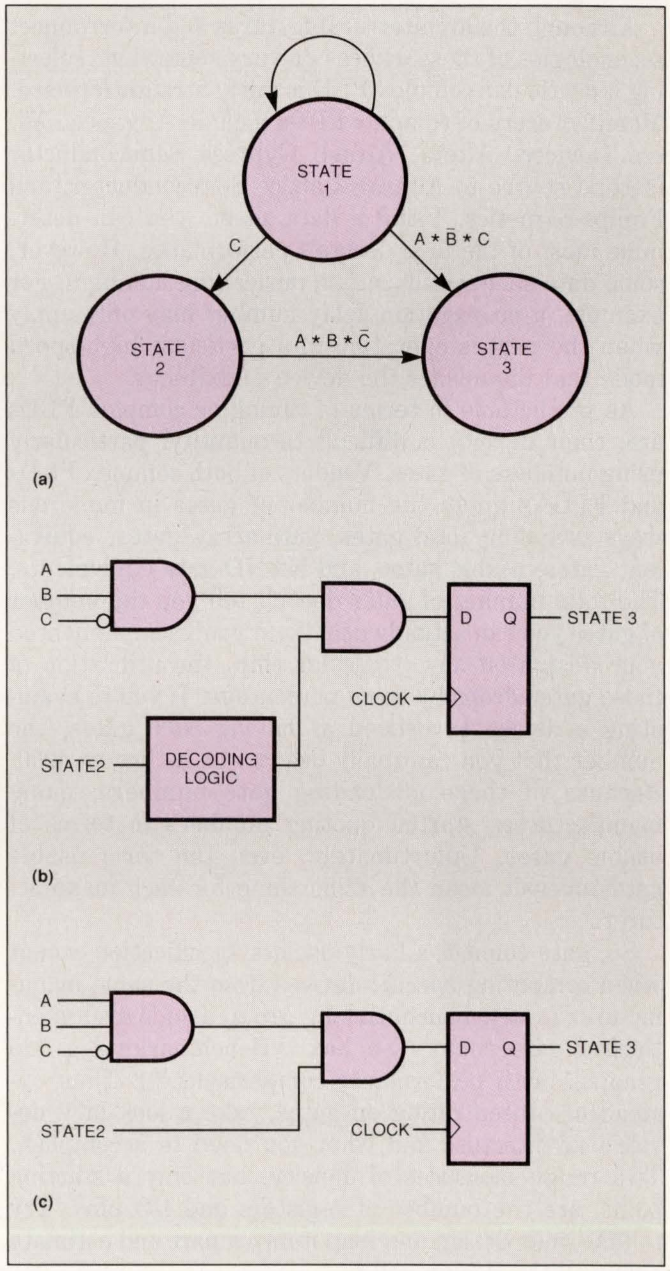


Fig 4—This very simple state machine (a) reveals the problem of implementing a maximally encoded state machine (b) in an FPGA. The decoding logic required is a waste of the FPGA's architecture. As the state machine grows in complexity, many such decoding blocks would be necessary. However, using the one-hot method (c) in which one and only one register's output (the "hot" one) determines the current state, does away with the decoding blocks entirely.

major difference between a binary counter and an LFSR counter. The counting sequence of an LFSR counter is not binary and is essentially pseudorandom. Whereas a binary counter can count to 2^N states, an LFSR counter can count to $2^N - 1$ states.

Getting down to the specifications

Although the architectural features and interconnect technologies of these devices do vary somewhat, selecting a particular complex PLD is fairly straightforward. Manufacturers of complex PLDs include Advanced Micro Devices, Altera, Atmel, Cypress Semiconductor (second source to Altera), Lattice Semiconductor, and Philips-Signetics. Using a data sheet, you can determine most of the final design's performance. However, some data sheets still contain misleading numbers. For example, a propagation-delay number may only apply when the part is operating in a particular high-speed mode that diminishes the device's flexibility.

As predictable in terms of timing as complex PLDs are, their density is difficult to quantify, particularly using numbers of gates. Vendors of both complex PLDs and FPGAs quote the number of gates in numerous ways including total gates, gate-array gates, equivalent gates, usable gates, and NAND-gate equivalents. The total number of gates doesn't tell you the number of gates you can actually use. Once you've implemented your design on any particular chip, the utilization of those gates drops by some percentage. If you're evaluating a device advertised as having 8000 gates, the number that you can really use can be as low as 4000. Because of these misleading gate numbers, many manufacturers started quoting numbers in terms of usable gates. Unfortunately, even the term usable gates doesn't mean the same thing for each manufacturer.

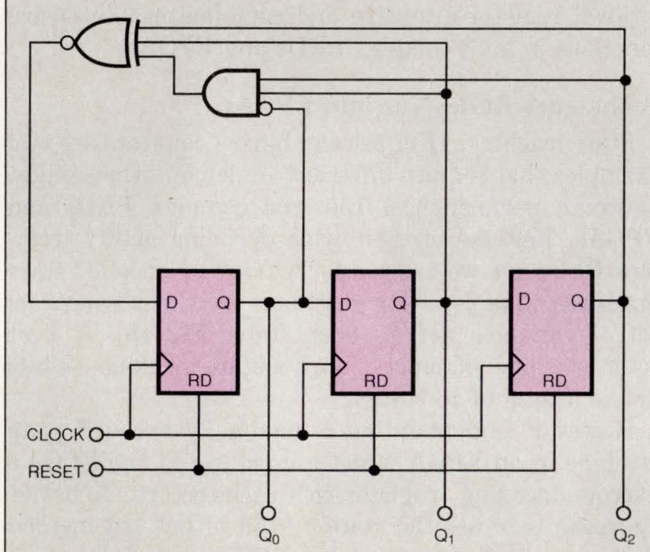
So, gate count is a fairly useless specification except when comparing specific devices from the same manufacturer (a new benchmarking group avoids even mentioning gate count (see **box**, "Benchmarking group grapples with performance comparisons.")). Thus, instead of concentrating on gates, take a look at a device's architecture and what you need to accomplish. Two rough measures of density, but only a starting point, are the number of registers and I/O pins. Try to take your design and map it into a part and estimate how well the design will fit.

One approach is to estimate what your design would take in standard logic. Then, look those devices up in the vendor's library and note the logic-block count for implementing that function. Adding up all the logic blocks necessary will give you a rough estimate that will allow you to decide between a 2000-gate device and a 4000-gate device.

The first thing to recognize when choosing an FPGA is that each vendor's devices exhibit fundamental architectural differences. These differences manifest themselves in both the individual logic blocks and the routing structure of the devices. Designers of the first FPGAs focused most of their attention on the structure of the logic blocks themselves, only to discover that the lack or abundance of routing channels can make or break the final design. Thus, the latest FPGA designs, from market leaders and recent start-ups, pay close attention to both.

The structure of FPGA logic cells ranges from extremely fine granularity to coarse granularity (**Fig 6**). Granularity is the amount of logic contained in one logic block. A fine-grained architecture, such as **Fig 6a**, is one that has very simple, basic blocks, even down to the transistor level. A coarsely grained architecture, such as (**Fig 6b**), has logic blocks of high complexity containing a number of digital logic functions.

Other than having to sort through architectural details, the most frustrating part of choosing one FPGA



STATE TABLE

Q_0	Q_1	Q_2
0	0	0
1	0	0
1	1	0
0	1	1
0	0	1

Fig 5—Implementing conventional binary counters in FPGAs isn't optimum because these counters use wide fan-in logic to generate high-end carry signals. A linear-feedback-shift-register counter, such as this 3-bit, modulo-five counter, is a more efficient implementation for an FPGA. Note from the state table that the counter skips some states and the counting sequence is a nonbinary, pseudorandom pattern. (Courtesy Xilinx application notes)

over another is that so very little data about the final density and speed is predictable from the outset. Whereas propagation delays of complex PLDs give you a good idea of your final design's performance, delays of the individual blocks within an FPGA are meaningless. The overall speed of an FPGA is determined both by the details of the internal blocks and the interconnect delays of the final utilized chip.

Every FPGA manufacturer's data sheets state things a little differently and with different underlying assumptions. Although the toggle rates of individual flip-flops inside each logic block tell you the speed possible from that block, there is no way to extrapolate system performance from that number due to the influence of the final routing paths.

Fortunately, more companies are now quoting attainable system-clock rates, but these numbers can also be highly misleading. Because of the speed/density tradeoff inherent to FPGAs, the speed the company was able to achieve for its example depends on the placement, routing, and implementation of the logic. You may see an advertisement for an 80-MHz 16-bit counter, but it's very possible that to achieve that performance, the FPGA requires expert hand routing and contains no logic other than that lonely 16-bit counter. That same counter combined with other logic may run at only 25 MHz.

Propagation delay is another potentially misleading specification. Because of the structure of a complex PLD, propagation delay is a quite meaningful measure of ultimate system speed. However, because of the structure of an FPGA, you can't use one logic cell's propagation delay to predict the timing of the overall design.

Fortunately, help may be on the way in the form of

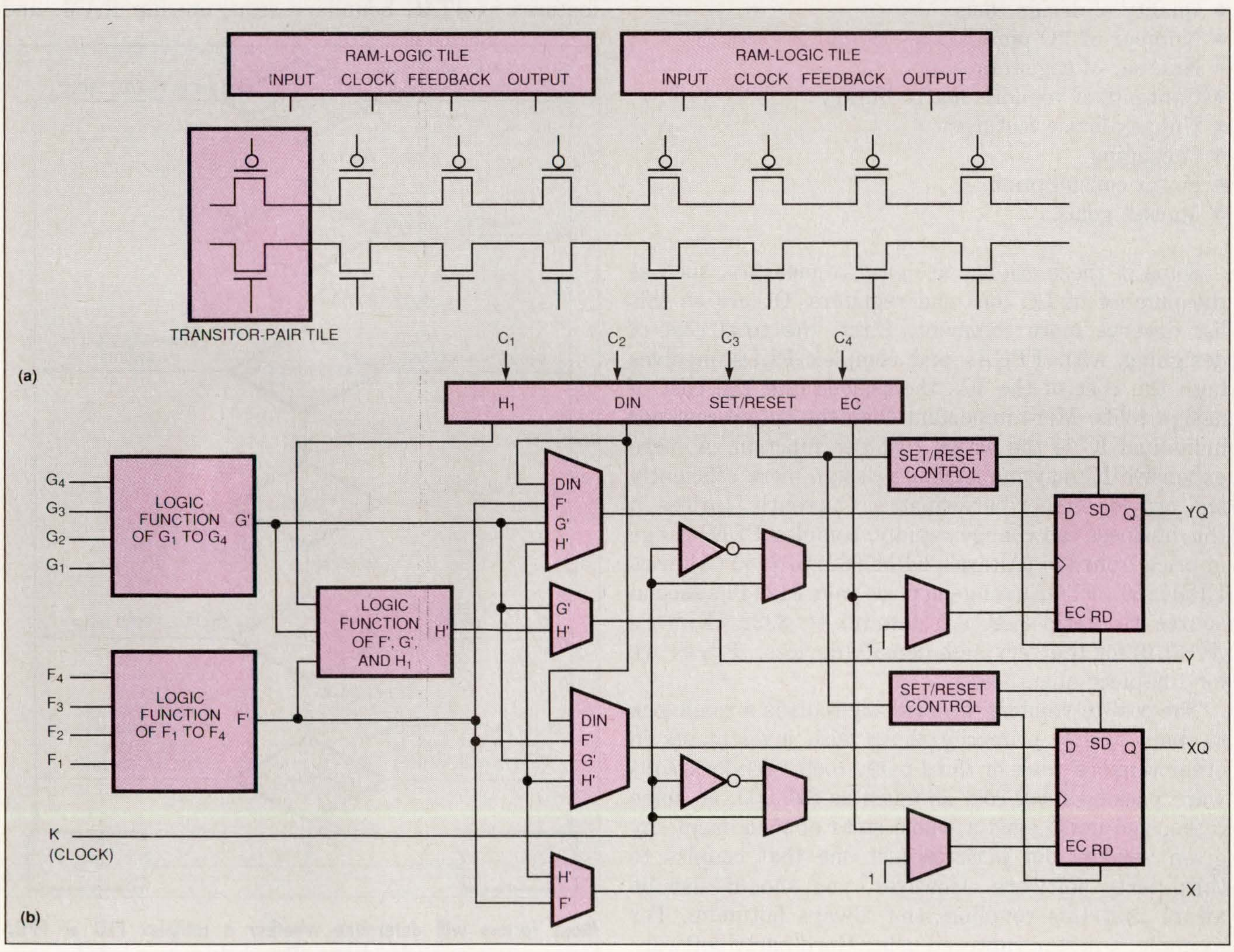


Fig 6—An FPGA's granularity can range from fine to coarse, respectively referring to the simplicity or complexity of the internal logic cell's structure. Crosspoint Solutions' devices and Xilinx's 4000 series represent the two ends of the granularity spectrum. Of all the available FPGAs, Crosspoint's devices, which connect transistor-pair and RAM-logic tiles to form macrocells, most closely resemble gate arrays.

benchmarks that have a common methodology and implementation. Both complex-PLD and FPGA vendors are cooperating to produce useful benchmarks that showcase the performance of each architecture under similar implementation conditions (see **box**, "Benchmarking group grapples with performance comparisons").

Consider all criteria

Architectural differences, interconnect technologies, and design methodologies inherent in complex PLDs and FPGAs are important factors governing the choice of these devices. Many other criteria will ultimately determine the wisdom of the final choice. These criteria include (but aren't limited to) the following:

- Cost of devices *and* design tools
- Quality of design tools
- Number of I/O pins
- Number of registers
- Contents of vendor's macro library
- Unique device features
- Packaging
- Power consumption
- Market goals.

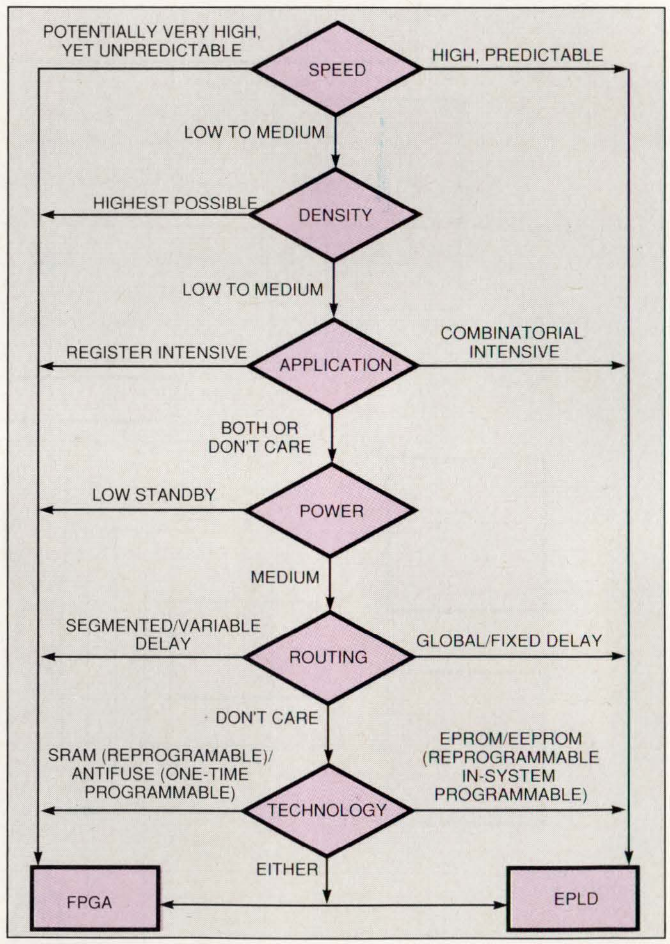
Some of these criteria are easy to measure, such as the number of I/O pins and registers. Others on this list deserve more comment. First, the total cost of designing with FPGAs and complex PLDs involves both the cost of the ICs themselves *and* the cost of design tools. More important than the actual cost per individual IC is the actual cost per function. A more expensive IC may implement a design more efficiently and provide higher performance. Currently, (prices in this business can change rapidly) complex PLDs range in price from $15 (Altera's EPM7032) to $400 (Altera's EPM7256). FPGAs range in price from $12 (TI's second source to Actel's ACT 1 family) to $922 (Xilinx's XC4010) for the very high density devices. (Prices are for 100-piece quantities.)

The cost of vendors' proprietary tools is a roadblock to many users, primarily those with investments in other vendors' tools or third-party tools. Vendors' software packages can cost as much as $10,000. In some cases, you don't need a whole suite of tools from any given vendor, but perhaps just one that couples to third-party software. However, you should also be aware that this coupling isn't always optimum. For example, a design captured using third-party software may not run successfully on the vendor's compiler. You may get only a cryptic error message that says something's not right. So, though buying proprietary tools may seem excessive, you may run into some time lags when using coupled software. On the flip side, third-party software can sometimes be better than proprietary tools at performing certain tasks.

Ultimately, judging the efficiency of the software tools isn't easy. One question that may help you judge is to ask vendors if hand routing will be necessary to produce an optimal design.

The completeness of a vendor's macro library—a library of expert-crafted logic functions—can also be a selling point for a particular complex PLD or FPGA. Every vendor supports some type of library. However, not all libraries contain exact equivalents to 7400 series standard logic but, instead, contain vendor-specific functions. Such a library makes retargeting and converting to a gate-array difficult.

Special features of FPGAs may influence your choice of devices. Some of the newest FPGAs include such features as JTAG boundary scan, on-chip RAM, and



Many factors will determine whether a complex PLD or FPGA better suits a particular design. This decision tree includes some basic criteria to consider when choosing between the two types. This tree makes the decision look straightforward, but most complex designs will involve compromises between the two devices' strong points.

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fast carry logic. If package style is important, be aware that, for example, not all complex PLDs and FPGAs come in surface-mount packages.

Delving into small details too quickly can obscure some other information that you'll have to digest to choose the right complex PLD or FPGA. Backing away from the design details and considering overall market goals will also help narrow down the decision.

Most users may start out thinking that their product will sell millions and they'll end up converting to a gate array (**Ref** 4). However, according to the vendors and users interviewed for this article, it seems that many FPGAs or complex PLDs find permanent homes in the end product. Still, your estimated production volume will have great bearing on the device you choose, whether it's because of the specific device cost of the FPGA or because you're looking for an architecture amenable to gate-array conversion.

Another product development issue to consider is prototyping time. If it's necessary to turn out prototypes quickly, the design-compiling time and device-programming time may be huge factors in your product's success. And even though the programming time may not seem critical during development, it may turn out to be crucial to the manufacturing department. Depending on the design platform, PLDs can take minutes to compile, whereas very dense FPGAs can take hours.

Considering all facets of complex PLDs and FPGAs—from the design methodology to market goals—is indeed daunting to the new user, but these devices are too useful to ignore. Although you won't find any easy answers when it comes to choosing high-density programmable logic, the rewards of density, flexibility, and user configurability are worth the effort. EDN

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Article Interest Quotient (Circle One)
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Manufacturers of complex PLDs and FPGAs

For more information on complex PLDs and FPGAs such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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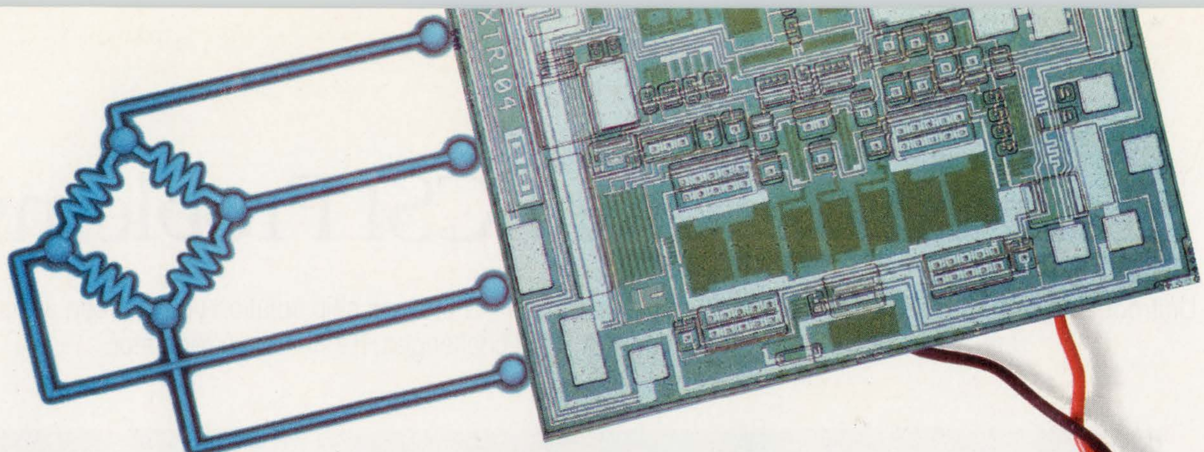
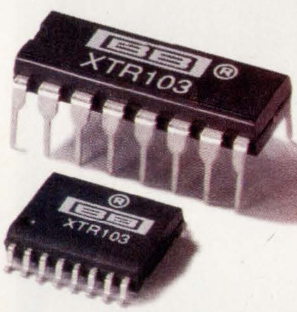


4-20mA Transmitters for RTDs & Bridges



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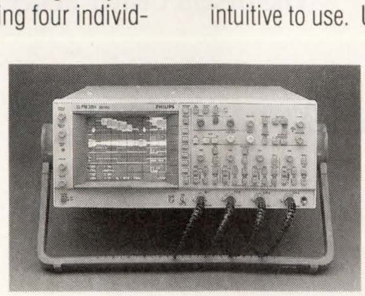

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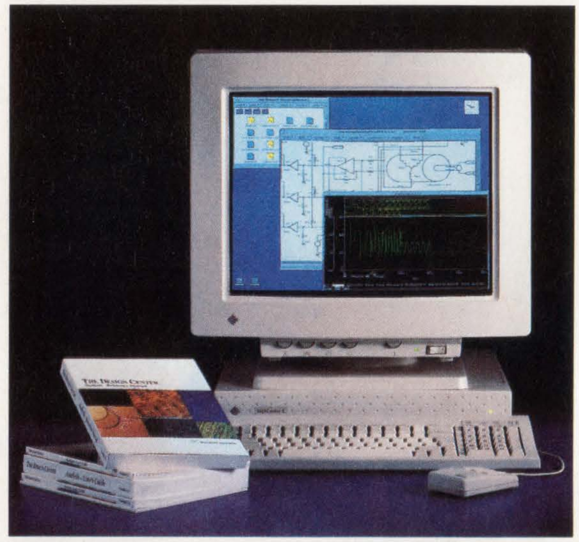

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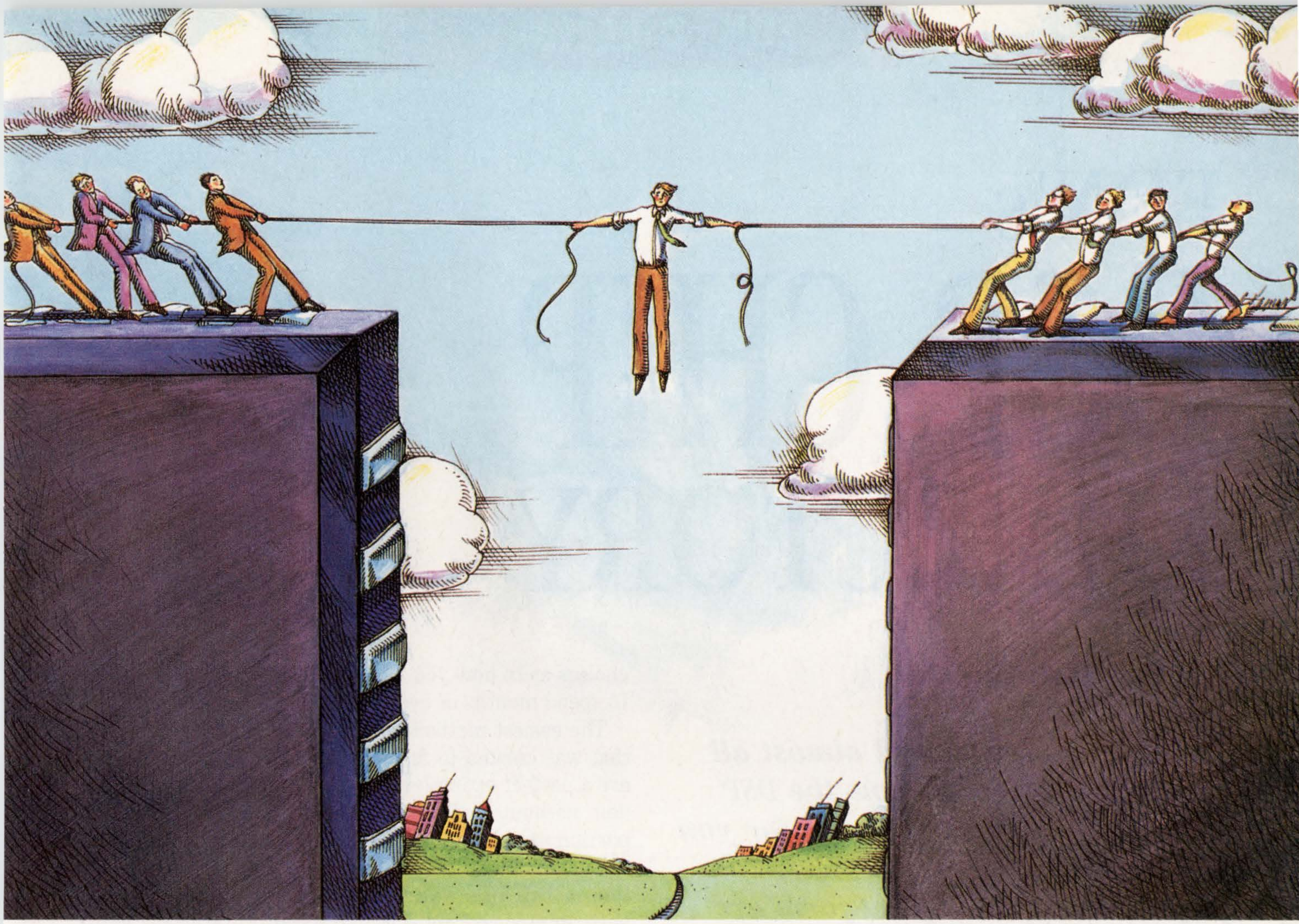

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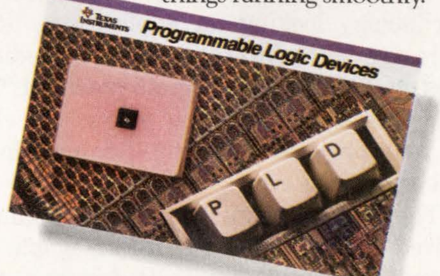

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CIRCLE NO. 56

EDN's DSP-CHIP DIRECTORY

David Shear, Technical Editor

DSP chips have touched almost all areas of electronics. Now the DSP industry is making it easier for you to use these powerful devices. Complete systems in chip-set form are now available, as are good tools to develop DSP applications.

The DSP industry is expanding into an ever increasing number of applications. DSP chips have invaded disk drives, cellular telephones, modems, radios, medical instruments, appliances, automobiles, and a number of other products. DSP is well beyond a strange new technology looking for applications. It is a maturing industry with chip sales alone exceeding a billion dollars in 1991. The expected growth is more than 30% per year for the next few years. The chances that one of your projects will benefit from using these devices is better than ever.

The biggest obstacle to many engineers is the perceived difficulty of using DSP. It would be very difficult if you just grabbed a DSP chip and a data book and tried to use it. That is what you would have had to do a few years ago. But the DSP industry has not been just sitting around. Many vendors are working hard to make DSP easier to use. You have many choices as to how you will use DSP. It is not necessary to spend months or even years becoming a DSP expert.

The easiest method of using DSP is to buy a chip set that was created to fit a market niche. Modem chip sets are a perfect example. You can create a high-speed modem without really concerning yourself with the DSP portion of the system. For example, AT&T has a chip set for 9600-baud and above modems. In this application, a DSP16A works as a data pump in conjunction with an analog front end and a digital interface chip.

Motorola is working with many vendors to be able to license niche-application code directly. The company wants to be a one stop shop for DSP. You will be able to buy the DSP chip and the software from the same vendor. But if you wish, you can negotiate directly with the algorithm developer.

The DSP chip manufacturers aren't the only ones providing chip sets with software and hardware support. DSP Group Inc (San Jose, CA) is an example of a company that is providing niche market chip sets. They use custom versions of TI's fixed-point DSP chips to implement a variety of functions. For example, they provide a chip set for digital answering machines. You don't have to be aware that there is a DSP chip in the chip set. You just tell it what you want done and the chip set does it.

Analog Devices is attempting to create an open standard for DSP called Signal Computing. This unites a general-purpose DSP with third-party software so that you can gather the DSP functions you need. Independent Algorithm Vendors (IAVs) create the code that runs on the DSP, which you can license. With the open nature of Signal Computing, each IAV can make its algorithms work on a variety of DSP chips. In many cases you will be able to select the hardware you need and get the DSP portion off the shelf.

It is too early to tell if Signal Computing will become the standard Analog Devices hopes it will. It will certainly make your job considerably easier if it does. With such a standard, as new DSP chips emerge, you will be able to transfer much of your design to the latest DSP. Since many products are expected to double in performance every 18 months, it would be nice to know that you didn't have to reinvent the wheel each time you had to design a new product.

Even without a standard, there are a number of vendors who sell algorithms. They will sell you a complete program for your needs or a partial program that contains all of the DSP code. Before you take on code development, check with the DSP chip manufacturer and see if they have or know of existing code. Each of the major DSP vendors has a very complete list of third-party vendors that can help you out.

TI has had a long tradition of offering tremendous support. They have an incredible amount of free DSP code on their bulletin board and in application manuals (call vendors for BBS numbers). Since the TI chips are the most popular DSP chips, more code has been writ-

The future looks bright for the DSP market

According to Will Strauss, President of Forward Concepts Co (Tempe, AZ), the total DSP-chip market was worth more than a billion dollars in 1991. This is divided into general-purpose, function- and algorithm-specific, building-block, and μP/μC DSP chips. The general-purpose DSP chips make up 36%, or $395 million, of the total market (**Fig A**).

Strauss expects the total DSP market to grow 29% next year, with the general-purpose DSP-chip market growing 39% in 1992. This growth is expected to continue for many years. There are so many applications and so much growth that there is room in the market place for many different products.

TI is still way out in front with 57% of the market (**Fig B**). Many large-volume applications are beginning to hit production. The largest market is modems, followed by disk drives and then by speech and audio applications. Digital cellular phones are coming on strong and will be one of the top applications soon.

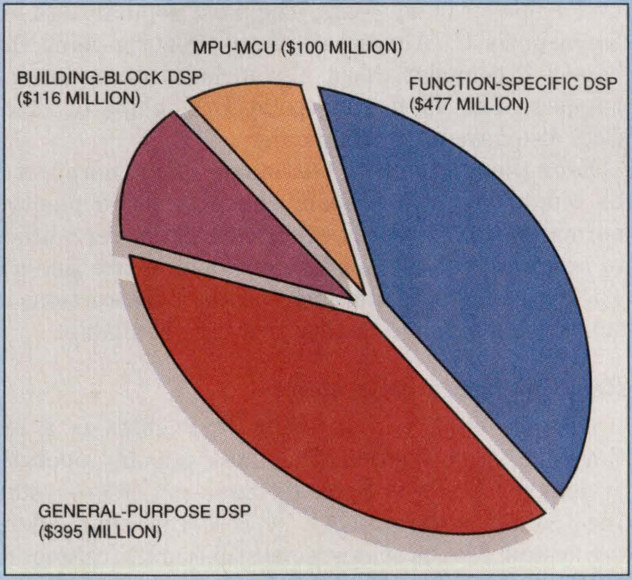


Fig A—This chart shows the total DSP market for 1991. (source Forward Concepts)

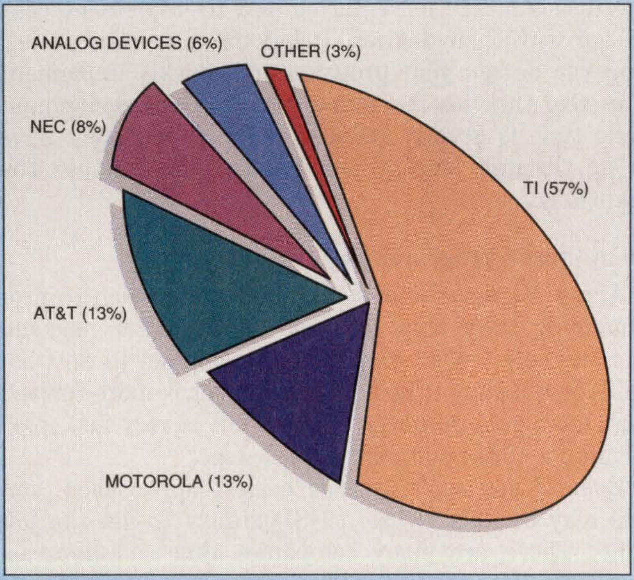


Fig B—This chart shows the general-purpose DSP market for 1991. (source Forward Concepts)

ten for them then any others. Many of the DSP text books you can use to get up to speed in using DSP have examples written for the TI chips.

Block-level programming

If you have to create your own algorithms, you may consider using a block-diagram type of programming system. Comdisco, Mentor, and Star Semiconductor have systems that let you create your program with block diagrams and then let the system implement it. Comdisco and Mentor have the ability to simulate the design and then implement it in a variety of ways.

Each of these systems has a library of blocks you can choose from. You use a graphical method to draw a signal-flow diagram to implement your algorithm. You can also create your own blocks to expand on the existing blocks.

Once the design is completed, you can simulate it and modify it to tune it to your application. After proving your concept, the system can automatically generate code for general-purpose DSP chips. You can implement your DSP system on an FPGA or other ASIC, or you can synthesize a custom IC.

Star Semiconductor uses a different approach. You enter the design in a similar manner but skip the simulation step because you can run the code directly on the SPROC-1000. The company's block-diagram programming tools work only with their chips. This has the disadvantage of requiring you to implement your design with their devices. It has the advantage of letting you design your program and quickly implement it in real time on the actual device. The development cycle time is greatly reduced because you don't have to go through lengthy simulations; you can use the real thing.

Menu-based programming

Array Microsystems has a similar approach to programming their chip set. The ArraysoFFT package lets you select what you want the chip set to do from pull-down menus (**Fig 1**). This chip set is more limited than most general-purpose DSPs but is very fast, performing a 1024-point FFT in 131 μsec.

Even if you can't use the easiest approaches, you still may be able to use a DSP library to get the job done. There are many companies that sell libraries that have standard algorithms in either source code or object code. Sonitech International Inc (Wellesley, MA) is an example of a company that sells DSP libraries as well as board-level DSP products and also licenses code for many of the popular algorithms.

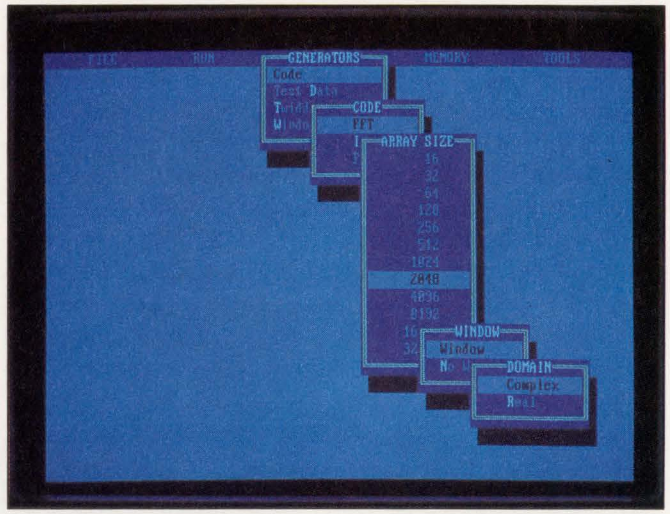


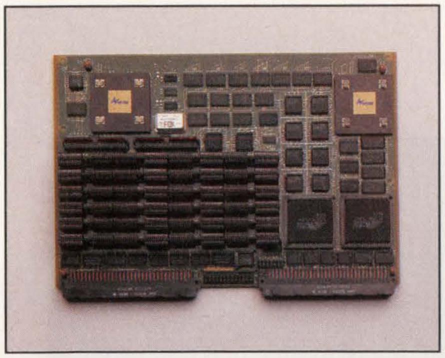
Fig 1—You can select what you want the a66 chip set from Array Microsystems to do by using pull-down menus. The ArraysoFFT package will then create the code.

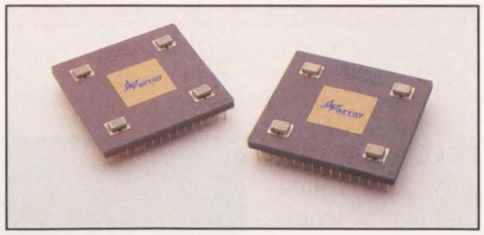
There is more to most DSP projects than just the creation of code to run algorithms. You will often have to write a large portion of the code to take care of system functions such as controlling indicators, communicating, interfacing with an operator, or controlling a few lines here and there. High-level languages and operating systems have been available for DSP chips for many years. The most popular high-level language is C. Almost all of the floating-point chips have a C compiler. Most also include source-level debuggers. The TI floating-point DSP chips (C3X and C40) also have an Ada compiler.

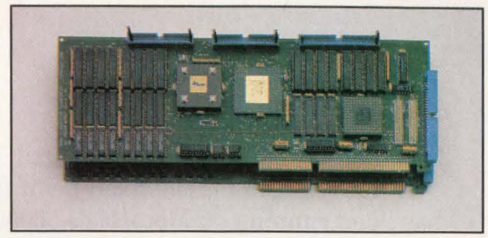
Even though the DSP portion of code generation can be tough, you will probably have to write plenty of normal μP-type code. The first DSP chips were difficult to program, but the more recent devices are fine μPs. Their architectures and many of their instructions are similar to a μP, and quality tools are available.

Real-time operating systems

Another major aid to using DSP chips is a real-time operating system. The most popular operating system for DSPs is Spox by Spectron Microsystems Inc (Santa Barbara, CA). It is a real-time operating system that provides a real-time multitasking kernel and modules for memory management, stream I/O, DSP math functions, and a C library. The company has just added a debug feature and multiprocessing support. Spox runs on Analog Devices'







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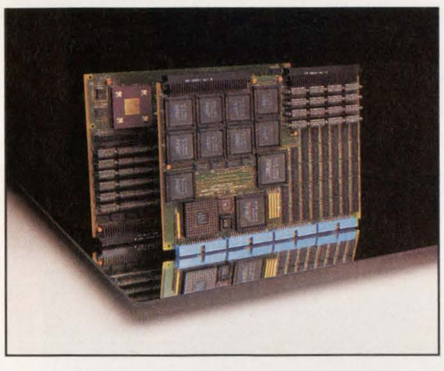

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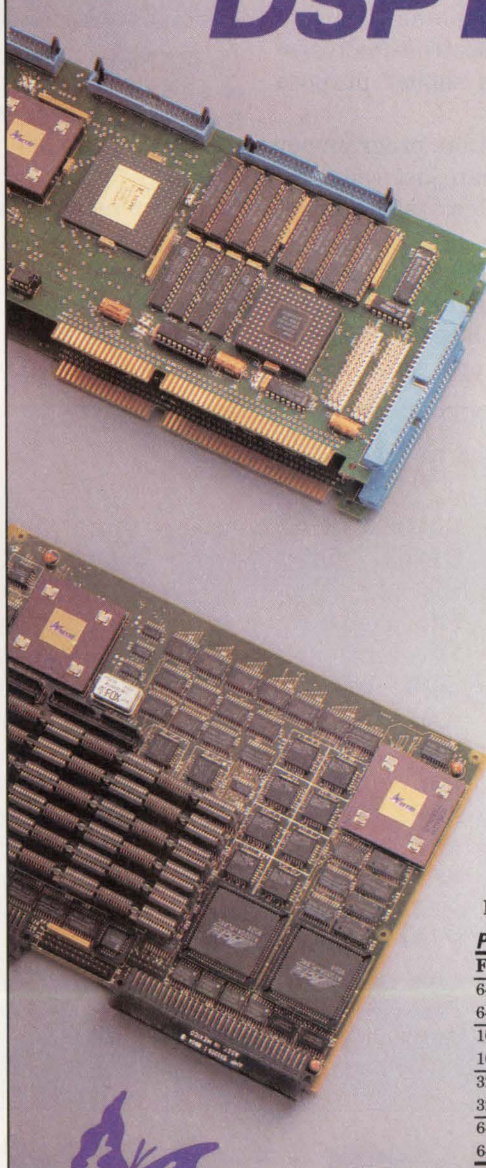

PC-AT DSP

1K FFT/126µs

DSP engine for the 16-bit PC-AT Industry Standard Architecture (ISA) bus

Performance Benchmarks

FFT size	a66550/32K @25MHz
64 Real	7.2 µs
64 Complex	10.9 µs
1024 Real	125.9 µs
1024 Complex	209.9 µs
32K Real	5.90 ms
32K Complex	10.49 ms
64K Real	15.73 ms
64K Complex	N/A

VME DSP

1K FFT/79.6µs

DSP engine for industry-standard VMEbus

Performance Benchmarks

FFT size	a66540A @40MHz	a66540A Cascade Sys.
64 Real	5.1 µs	2.9 µs
64 Complex	5.0 µs	3.7 µs
1024 Real	79.6 µs	29.6 µs
1024 Complex	132.7 µs	59.1 µs
32K Real	3.69 ms	0.91 ms
32K Complex	6.56 ms	1.82 ms
64K Real	7.37 ms	1.82 ms
64K Complex	13.11 ms	3.64 ms

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21000 family, Motorola's 96002, and TI's C3X and C40.

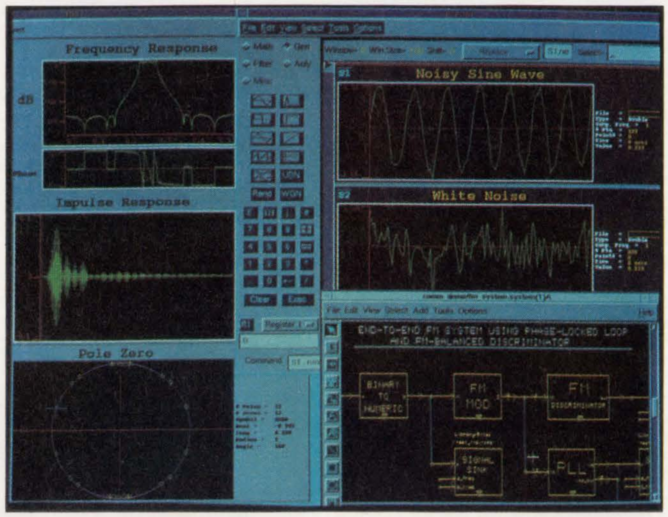
A new version for the fixed-point family, MicroSpox, has been running on Motorola's 56000 and is now available for Analog Device's ADSP2100 family and TI's TMS320C2X and TMS320C5X family. MicroSpox contains only the multitasking kernel, I/O, and memory management.

Motorola's 56000 also runs VRTX from Ready Systems, a real-time operating system that runs on virtually all major μPs. National Semiconductor is planning to have a real-time operating system for the 32SF640 available by the end of the year.

AT&T and Spectron Microsystems both have software interfaces between the DSP chip and the end-user application. VCOS from AT&T is an operating system that implements the DSP3210 on the mother board of a PC or workstation. OSPA from Spectron Microsystems works with Spox and serves a similar purpose with other DSP chips.

Both products isolate the application programmer from the algorithm developer. You can just call DSP functions and let the operating system take care of everything else.

In almost all projects you will have to write some portions of the code in assembly language. In some projects you may have to write all of the code in assembly language. Often the DSP portion must be optimized by programming in assembly language. Writing assembly code for DSP chips is often like writing code for your favorite μP. Many DSP chips are capable μPs. It is difficult to generate assembly code that takes advantage of all of the parallel features of the DSP chips. Unfortunately, this is usually the code that



The DSP Framework provides an environment to enter your design as a block diagram, analyze its performance, and then implement the design on an FPGA, ASIC, custom chip, or general-purpose DSP chip.

Key to abbreviations used in block diagrams

AB—combined program-and-data address bus
ACC—accumulator
ADC/DAC—analog to digital and digital to analog converter
ADDR GEN—address generator
ALU—arithmetic logic unit
BIT MANIP—bit manipulation
BS—barrel shifter
CDB—control data bus
CM—cache memory
CPUB—CPU bus
DAB—data address bus
DB—combined program-and-data data bus
DDB—data data bus
DM—memory for data only
DMAAB—DMA address bus
DMADB—DMA data bus
DMAC—direct memory access controller
FX—fixed-point
FP—floating-point
GDB—global data bus
HOST INTER—host interface
IDB—instruction data bus
INT—external interrupt
MAC—multiplier accumulator
MULT—multiplier
PAB—program address bus
PDB—program data bus
P/DM—program and data memory
PIO—parallel I/O
PM—memory for program only
PPCP—parallel processor communication port
PRAB—peripheral address bus
PRDB—peripheral data bus
REG—register
REGB—register bus
SIO—serial I/O
TIM—timer
XAB—external address bus
XDB—external data bus
XDAB—external data address bus
XDDB—external data data bus
XIOAB—external I/O address bus
XIODB—external I/O data bus
***XPAB**—external program address bus
XPDB—external program data bus

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CIRCLE NO. 58

has to be optimized for speed.

But vendors do not leave you on your own to create assembly-language programs. There is a considerable amount of free DSP code. You can find it on computer bulletin boards operated by the DSP vendors. Or, you can get it out of some of the excellent application manuals that are available. By looking at this code, you can quickly get up to speed on using assembly language. You may even be able to modify some existing code to get what you want.

Almost all of the DSP manufacturers have developed evaluation packages that include an evaluation board and enough software tools to give you a feel for what the chip can offer, what their support is like, and how well their tools work (**Ref 1**). Spending a couple of bucks and a few days can give you the confidence to make informed choices about which part to use.

Index to DSP μPs included in this directory

Supplier	Device	Type	Page
Analog Devices	ADSP-2100 family	16-bit fixed-point	100
Analog Devices	ADSP-21020	32-bit floating-point	121
Array Microsystems	a66 chip set	16-bit fixed-point	136
AT&T	DSP16 family	16-bit fixed-point	101
AT&T	DSP32C/3210	32-bit floating-point	122
Motorola	DSP56156	16-bit fixed-point	102
Motorola	DSP56001/2	24-bit fixed-point	103
Motorola	DSP96002	32-bit floating-point	125
National	NS32SF640	32-bit fixed-point	104
NEC	77C25	16-bit fixed-point	105
NEC	77016	16-bit fixed-point	106
NEC	77220	24-bit fixed-point	109
NEC	77240	32-bit floating-point	132
SGS-Thomson	ST18 family	16-bit fixed-point	110
Sharp Electronics	LH9124/9320 chip set	24-bit fixed-point	141
Star Semiconductor	SROC-1000	24-bit fixed-point	113
Texas Instruments	320C1X	16-bit fixed-point	114
Texas Instruments	320C2X/5X	16-bit fixed-point	117
Texas Instruments	320C3X	32-bit floating-point	135
Texas Instruments	320C40	32-bit floating-point	126
Zilog	Z89C00	16-bit fixed-point	118
Zoran	34325	32-bit floating-point	129

Another trend that will make your job easier is custom DSP chips. You can take a DSP core and surround it by the memory and peripherals you need. So far, this approach is only viable for very-high-volume applications. All DSP chip makers are migrating their chips into a core that lets you surround the basic chip with the peripherals you need. At present TI sells between 10 and 20% of their products as custom devices based on their fixed-point core. Within a few years, custom devices are expected to grow to 50% of production. As the volume grows, it will become cheaper to get the DSP chip you need, and lower-volume applications will be able to take advantage of it.

You should also keep an eye on μPs and microcontrollers (μCs) because many are gaining some DSP capability. You will continue to see multipliers and other DSP elements sprout on these chips. But just sticking a multiplier on a chip doesn't mean that it can perform DSP functions. Many of the devices that have limited DSP capability are designed for a particular application. Your algorithm may or may not be enhanced by the added circuitry.

An example of DSP growth on a μC is Motorola's 68HC16. It is a 16-bit device that can perform a multiply and accumulate in 720 nsec. In terms of traditional DSP, this is not very fast. But for the applications it was designed for, it works very well. This chip was designed for disk-drive applications but is useful elsewhere.

Motorola admits that the device is not fast but points out that many applications can't afford, and don't need, full general-purpose DSP capability. When reviewing requirements with potential customers, Motorola blocks out a combined μC and DSP including memory for both devices. Everyone gets excited until the cost is discussed. All of that silicon costs a lot of money.

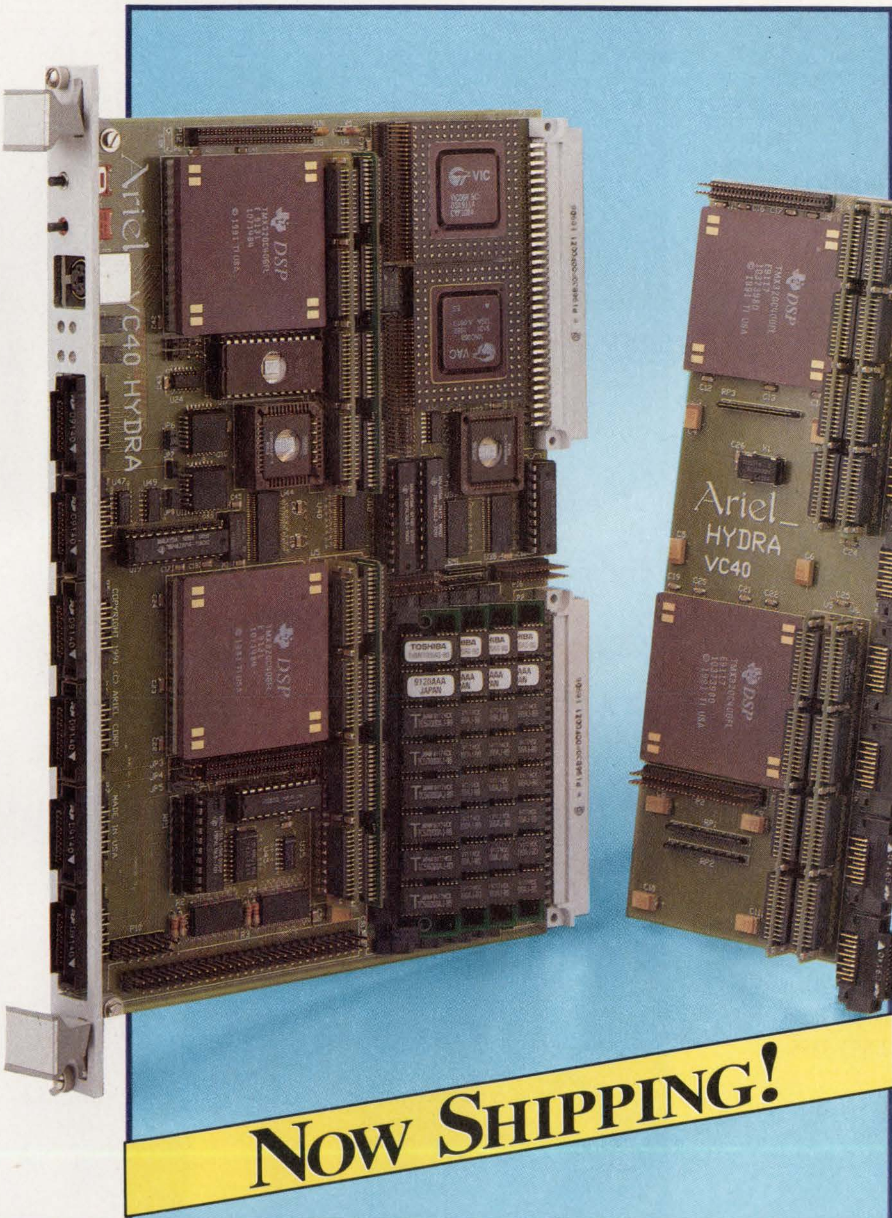
By adding incremental DSP capability, an incremental cost is incurred. By knowing your algorithm and knowing how to get by with only the capabilities you really need, you can reduce the cost of the μC chip.

National is approaching the problem in a similar manner to Motorola. Almost all of their μP products have some DSP capability on the chip. Each version is intended for a niche market, from digital answering machines, to modems, to faxes, to printers, to combined office equipment that does all of these functions. Each chip has a different amount of DSP based on the needs of the algorithm in the application.

Zilog has looked at the problem and decided to create its own DSP chip (Z89C00) and integrate it onto a Z8 μC. The μC and the DSP chip each have their own

Ariel V-C40 Hydra Breaks the BOPS Barrier

1.1 billion operations per second sets the record for 6U VMEbus coprocessor cards



Only Ariel's Hydra combines four TI TMS320C40 DSPs to deliver twice the processing speed and four times the I/O bandwidth of any 6U VMEbus coprocessor card. It's the only choice for the most compute-intensive multiprocessor applications.

The V-C40 packs up to 64 Mbytes of DRAM as well as up to 5 Mbytes of SRAM in eight banks—two per processor. Each DSP has direct access to memory via dual 32-bit memory buses, as well as six parallel I/O ports and a high-speed six-channel programmable DMA controller. All six channels can transfer data simultaneously without interrupting program execution.

Hydra also includes a 24-bit parallel ADbus that lets you access a wide range of high-speed data acquisition cards. Development support includes an ANSI C compiler and the first PC-based XDS510 in-circuit emulator to support parallel processing. And of course, with Ariel's legendary technical support, you'll never work alone.

To learn more about the V-C40 Hydra, or any of Ariel's DSP products for ISA/EISA, VMEbus, SBus, Hewlett-Packard, NeXT, or Macintosh computers, send us a fax, leave us a message on the BBS or E-mail, or just give us a call.

Distributed in: **France**, REA Informatique, tel: 1 49 65 25 50, fax: 1 49 65 25 69; **Israel**, Militram Futuristic Technology Ltd., tel: 52-545685, fax: 52-574383; **Italy**, International Trading Device SRL, tel: 02-749 0749, fax: 02-761 0407; **Japan**, Marubun Corp., tel: 033-639 9816, fax: 033-661 7433; **South Korea**, Seoil Enterprise, 3030, 21-Dong, Sunin Electronics Bldg., 16-1, 2-Ku, Hankang-Ro, Yeoungsan-Ku, Seoul, tel: 2-704 1392, fax: 2-703 8090; **United Kingdom**, Data Beta, Unit 7, Chiltern Enterprise Centre, Theale, Berks RG7 4AA, tel: 44-0734 303631, fax: 44-734 323617.

Ariel_

The DSP Authority

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CIRCLE NO. 59

memory and communicate to each other via a set of common registers. The combined chip is intended for modem and fax applications. In these applications, the requirements of the DSP portion of the code are compute intensive enough to warrant more capable DSP hardware on the same chip. But even this chip is limited in order to keep the cost down. It doesn't have a barrel shifter or zero overhead looping, it only has a 24-bit accumulator, and it lacks a few more features of other DSP chips. But you don't always need all of the functions of a general-purpose DSP chip. By leaving some things off the chip, it costs a lot less.

It is also possible to let the DSP chip absorb the μC functions. In many applications a μC will run much less than 1 MIPS. When a DSP chip is runs at 20 MIPS, it usually has plenty of power to spend some time on the functions normally taken care of by a μC.

Some DSP applications need as much power as possible. In these cases, like video compression, the DSP chip will usually be doing just DSP functions. But many other applications leave the DSP chip idle some of the time. With the increasingly capable tools, you should be able to bring the control functions into the DSP chip.

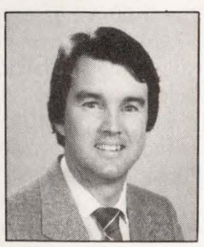
All of these methods have varying degrees of difficulty and flexibility. It is sometimes dangerous to adopt a new technology and expensive to acquire the expertise. There are many companies that are doing their best to reduce the danger and cost. But the most dangerous approach is to ignore DSP all together. You can be assured that your competition isn't ignoring it. It has been proven that DSP can bring immense performance and functionality gains to a product. EDN

Reference

1. Leibson, Steve, "Learn to use DSP chips with a minimum of pain," *EDN*, June 4, 1992, pg 45.

Author's biography

David Shear is one of EDN's technical editors. He can be reached at (503) 754-9310.



Article Interest Quotient (Circle One)
High 473 Medium 474 Low 475

ADSP-2100 FAMILY

16-BIT FIXED-POINT CMOS DSP μP

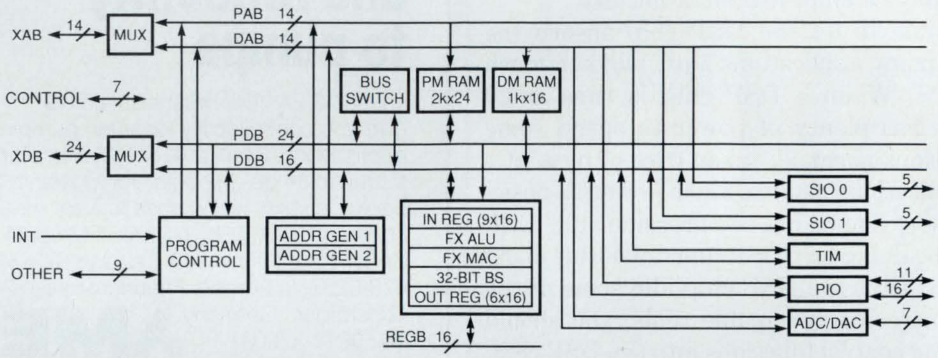
AVAILABILITY: All units are in production now.

COST: ADSP-2100 $45 (1000); -2101, $36 (1000); -2102, $34 (min 5000); -2105, $9.90 (1); -2106, 11.39 (min 25,000); -2111, $48 (1000); -2112, $46 (min 5000); -21msp50, $57 (1000); -21msp51, $40 (min 25000).

SECOND SOURCE: None.

Analog Devices Inc
Box 9106
Norwood, MA 02062
(617) 461-3881
Circle No. 669

DESCRIPTION: The ADSP2100 family offers a variety of options, ranging from the 2100, without any on-chip memory and a Harvard architecture brought off-chip, to the 21msp51, with program and data ROM and data RAM and peripherals, including an ADC, DAC, and host-interface port, on chip. The data memory has a 16-bit width, but the program memory has a 24-bit-word width to control the parallel operations. Low voltage versions are now sampling.



FEATURES: 60-, 77-, 80-, 100-, 125-, and 167-nsec cycle-time versions.

Separate on-chip program and data buses.

On-chip memory: The 2100/A has no on-chip memory. The 2101 has a 2k × 24-bit program RAM and a 1k × 16-bit data RAM. The 2102 has a 2k × 24-bit program ROM or RAM and a 1k × 16-bit data RAM. The 2105 has a 1k × 24-bit program RAM and a 512 × 16-bit data RAM. The 2106 has a 1k × 24-bit program ROM or RAM and a 512 × 16-bit data RAM. The 2111 and 21msp50 have a 2k × 24-bit program RAM and a 1k × 16-bit data RAM. The 2112 has a 2k × 24-bit program ROM or RAM and a 1k × 16-bit data RAM. The 21msp51 has a 2k × 24-bit program RAM, 2k × 24-bit program ROM, and a 1k × 16-bit data RAM.

Separate program and data buses brought off the chip only on the 2100/A.

All other parts combine program and data buses off the chip.

Off-chip memory capacity: The 2100/A has 32k × 24-bit program and 16k × 16-bit data memory capacities. All the others have 16k × 24-bit program and 16k × 16-bit data memory capacities.

Boot memory controller loads program from external byte-wide EPROM (except 2100/A).

On-chip peripherals: The 2100/A has no on-chip peripherals. The 2101 and 2102 have two serial I/O ports and a timer; the 2105 has one serial I/O port and a timer. The 2111/2 have two serial I/O ports, a timer, and a host interface port. The 21msp50 has two serial I/O ports, a parallel I/O port, a timer, and a 16-bit ADC/DAC (linear codec).

Multiplier/accumulator accepts 16-bit fixed-point input and creates 32-bit fixed-point results within a 40-bit accumulator. 16-bit ALU. 32-bit bidirectional barrel shifter. 40-bit accumulator.

Multiplier/accumulator, ALU, and shifter are separate blocks connected by the 16-bit R-bus and the data bus.

Zero-overhead looping.

Only the 2100/A has a 16 × 24-bit on-chip cache.

Direct, indirect, immediate, circular, and bit-reversal addressing modes.

Two address generators.

No on-chip DMA. Serial port and codecs have auto buffer, which transparently transfers data to and from memory.

16-level hardware stack. Status stack limits interrupts to four levels of nesting on the 2100/A, seven levels on the others.

Four external interrupts on the 2100/A; three external interrupts on others.

The 2100/A has only hardware wait states. Others have only software-programmable wait states.

No on-chip emulation port.

Only the 21msp50 has power-down mode to CMOS standby levels. The 2101, 2105, 2106, 2111, and 2112 have an idle mode, which lowers power until an interrupt is detected.

Packaging: 2100/A, 100-pin PQFP and 100-pin PGA. 2101/2, 68-pin PGA and 68-pin PLCC. 2105/6, 68-pin PLCC. 2111, 100-pin PQFP and 100-pin PGA. 21msp50/1, 100- and 132-pin PQFPs, 144-pin PGA.

SUPPORT

HARDWARE

Full featured in-circuit emulator.
Low-cost in-circuit emulator board.
Demo board.
Evaluation packages.
Third-party support: Contact Analog Devices for a list of third-party vendors.

SOFTWARE

C compiler. Simulator.
Macroassembler/linker.
Application libraries.
Upcoming Numerical C.

16-BIT FIXED-POINT CMOS DSP µP

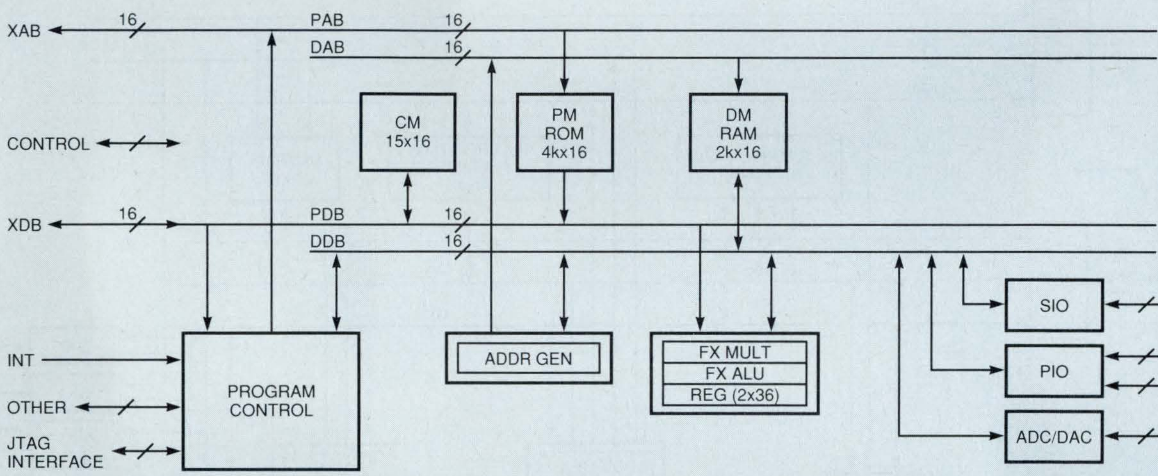
AVAILABILITY: The DSP16A, DSP16C, DSP1610, and DSP1616 are in production.

COST: DSP16A, $22.60; DSP1610, $91; DSP1616, $35.70 (1000).

SECOND SOURCE: None.

AT&T Microelectronics
Dept 52AL040420
555 Union Blvd
Allentown, PA 18103
(800) 372-2447, ext. 796;
in Canada, (800) 553-2448, ext. 796
Circle No. 670

DESCRIPTION: The members of the DSP16 family have long been the fastest fixed-point DSP chips. The DSP16A has a 25-nsec cycle time. The DSP16A and DSP16C also have the largest on-chip program memory at 12k×16 bits. Many applications that would require external ROMs with other DSP chips can fit within the DSP16 family's on-chip memory. The DSP16C has an ADC and a DAC on chip. The DSP16C also has a 4-pin JTAG interface, which assists in testing tightly packed boards. A 3.3V version of the DSP16A is available. The DSP1610/1616 are enhanced versions intended for digital cellular telephone use.



FEATURES: 25-, 33-, and 55-nsec cycle-time versions. The DSP16C has 25-, 28-, 33-, and 38-nsec cycle-time versions.
Separate on-chip program and data buses.
On-chip memory: The DSP16A and -16C have a 12k×16-bit program ROM and a 2k×16-bit data RAM. The DSP1610 has a 512×16-bit boot ROM and an 8k×16-bit dual-port RAM. The DSP1616 has a 12k×16-bit ROM and a 2k×16-bit dual-port RAM.
The program ROM on the DSP16A and -16C can be replaced or augmented with as much as 64k words of external memory.
The DSP1610/1616 can access two external 64k address spaces
Parallel and serial I/O port.
The DSP16C has an on-chip codec.
The DSP1610/1616 each have an on-chip timer.
The multiplier accepts 16-bit fixed-point data and creates 32-bit fixed-point results within a 36-bit accumulator.
32-bit ALU.
Only the DSP1610/1616 have a 36-bit barrel shifter and bit-manipulation instructions.
Two 36-bit accumulators.
Zero-overhead cache looping as many as 127 times.
15-word instruction cache.
Immediate, register-indirect, and circular addressing modes.
No on-chip DMA.
Single-level hardware stack is software expandable into main memory.
One external interrupt.
DSP1610 has hardware and software wait states. DSP1616 has software wait states.
DSP1610/1616 have on-chip emulation port.
The DSP16A, -16C, 1610, and 1616 have power-down mode.
The DSP1616 will run from 3.3 to 5V.
Packaging: DSP16A, 84-pin PLCC or 84-pin PQFP. DSP16C, 100-pin PQFP. DSP1610, 132-pin PQFP. DSP1616, 100-pin PQFP or SQFP.

SUPPORT

HARDWARE

Development system with in-circuit emulation.
Evaluation board that plugs into a PC.

SOFTWARE

Assembler/linker.
Simulator.
Application library.
Third-party support includes filter-design packages. Contact AT&T for a list of third-party vendors.

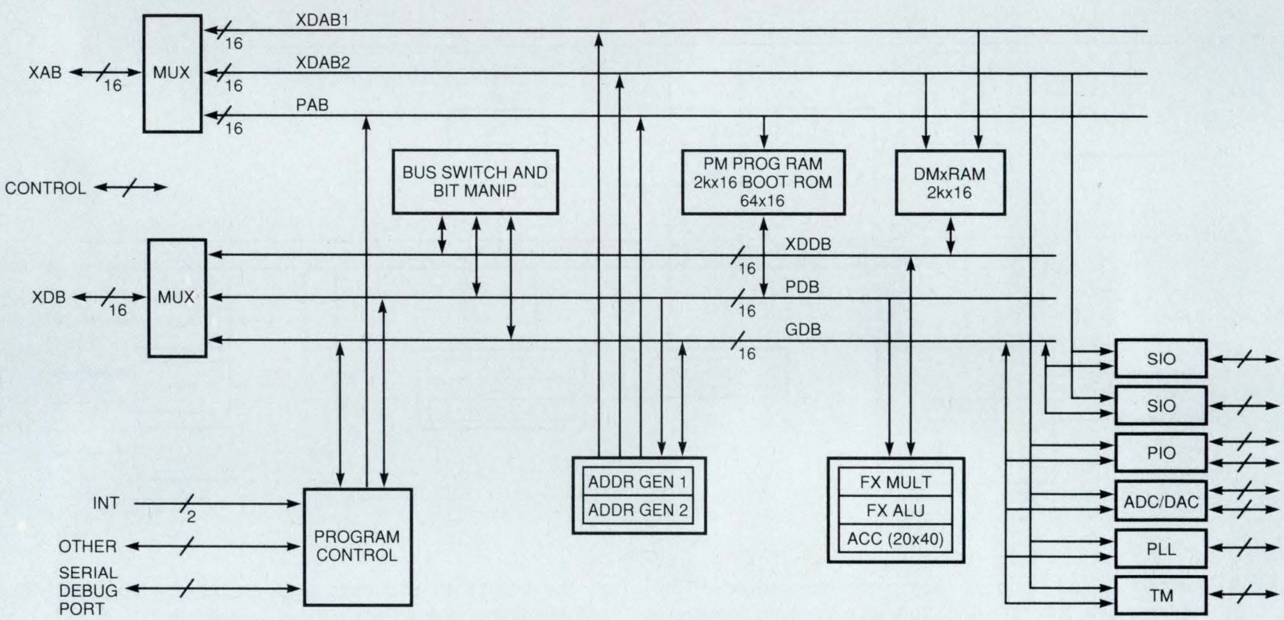
DSP56156

16-BIT FIXED-POINT CMOS DSP μP

AVAILABILITY: Now.
COST: DSP56156—40 MHz, $72 (1), $50 (1000); 60 MHz, $108 (1), $75 (1000).
SECOND SOURCE: None.

Motorola Inc
Microprocessor Products Group
6501 William Cannon Dr
Austin, TX 78735
(512) 891-2030
FAX (512) 891-3874
Circle No. 671

DESCRIPTION: The 56156 is a 16-bit subset version of the 56001. It is intended for cellular telephone and other communication applications. It has a built-in codec and phased-locked loop. Development tools are similar to the 56001 and the 96002.



FEATURES: 33- and 50-nsec cycle-time versions.
Three address buses and three data buses.
On-chip memory includes a 2k×16-bit program RAM and a 2k×16-bit data RAM.
ROM-based version (DSP56156ROM) contains a 12k×16-bit program ROM.
Separate external program and data memory spaces. Each can address 64k×16-bit locations.
Can load program from external EPROM.
Asynchronous and synchronous serial I/O ports.
Parallel port can interface with a host μP.
Has on-chip phase-locked loop (PLL).
On-chip sigma-delta voice band codec.
Multiplier accepts 16-bit data and returns 40-bit results to 40-bit accumulator.
ALU performs arithmetic operations on 40-bit data and logical operations on 16-bit data.
No barrel shifter.
Two 40-bit accumulators.
Zero-overhead looping.
Immediate, direct, indirect, circular, and bit-reversed addressing modes.
No DMA support.
Two external vectored interrupts.
Has on-chip emulation.
Low-power mode.
Packaged in a 112-pin ceramic quad flatpack.

HARDWARE — SUPPORT — SOFTWARE

Hardware:
Application development system includes in-circuit emulator.
Contact Motorola for a list of third-party vendors.

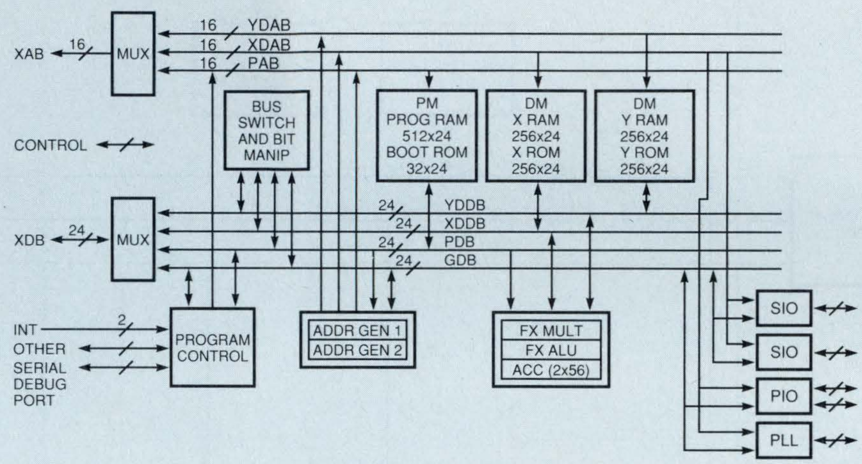
Software:
Macro cross assembler.
Linker.
Application development board.

24-BIT FIXED-POINT CMOS DSP μP

AVAILABILITY: Now.
COST: DSP56001: 27 MHz, $33 (1), $27 (1000); 33 MHz, $40 (1), $33 (1000). DSP56002: 40 MHz, $55 (1), $43 (1000).
SECOND SOURCE: None.

Motorola Inc
Microprocessor Products Group
6501 William Cannon Dr
Austin, TX 78735
(512) 891-2030
FAX (512) 891-3874
Circle No. 672

DESCRIPTION: The 56001 provides one 24-bit data word and two 56-bit accumulators. This extended precision lets the chip process 16-bit data more easily than the 16-bit machines can. A 24-bit-word width eases scaling, and the 56-bit accumulators prevent overflow. The 24-bit data width suits digital audio applications. The 56002 is a high-speed, low-power, low-voltage version of the 56001 that is 100% software compatible, and includes a PLL and on-chip emulation.



FEATURES: DSP56001 60- and 74-nsec cycle-time versions. DSP56002 50-nsec cycle-time.
Three address buses and four data buses.
Separate address buses for program ROM and the two data RAMs.
Separate data buses for program ROM, the two data RAMs, and global data.
On-chip memory includes a 512×24-bit program RAM, a 32×24-bit boot ROM, dual 256×24-bit data RAMs, and dual 256×24-bit data ROMs.
ROM-based version (56000) available.
Three separate memory spaces (X, Y, and P). Each can address 64k×24-bit locations.
Can load program from external EPROM.
Asynchronous 8-bit serial I/O port.
Synchronous 8- to 24-bit serial interface.
Parallel port can interface with a host μP.
56002 has on-chip PLL.
Multiplier accepts 24-bit data and returns 48-bit results to 56-bit accumulator.
ALU performs arithmetic operations on 56-bit data and logical operations on 24-bit data.
No barrel shifter.
Two 56-bit accumulators.
Zero-overhead looping.
Immediate, direct, indirect, circular, and bit-reversed addressing modes.
Two address generators.
No DMA support.
System stack is 15 levels deep but can be read by program to extend stack into main memory.
Two external vectored interrupts on 56001, three on 56002.
Hardware and software-programmable wait states.
Only the 56002 has on-chip emulation.
Low-power mode.
Low-voltage version of 56002 by fourth quarter 1992.
56001 is packaged in a 132-pin ceramic quad flatpack or 88-pin PGA. 56002 is packaged in a 132-pin PGA or PQFP.

SUPPORT

HARDWARE

Application development system includes in-circuit emulator.
Contact Motorola for a list of third-party vendors.

SOFTWARE

C compiler.
GNU C compiler and source-level debugger.
Macro cross assembler.
Linker/librarian.
Simulator.
Code translator from TMS320C10 to 56001.
Third-party support includes filter-design software, and VRTX32/DSP56001 and Spox real-time operating systems.

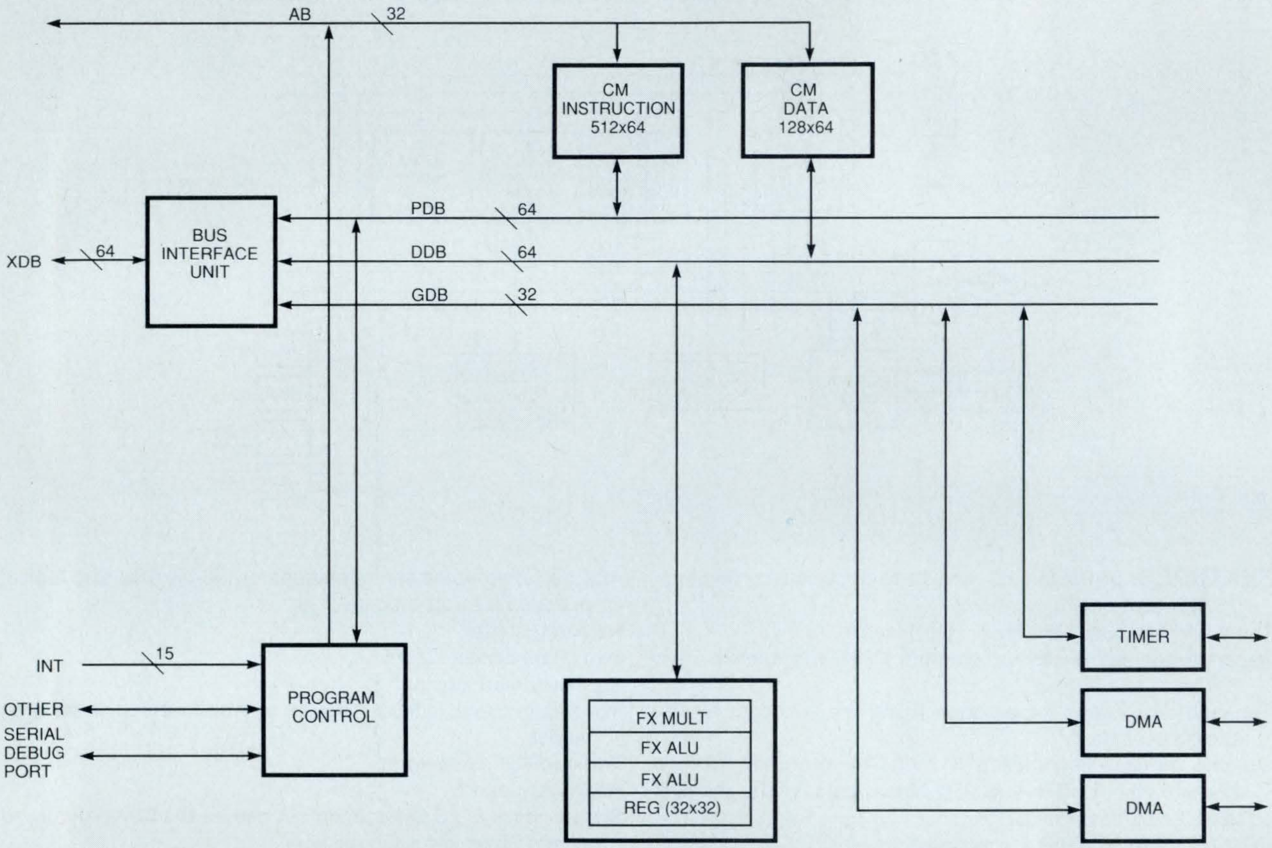
NS32SF640

32-BIT FIXED-POINT CMOS DSP μP

AVAILABILITY: Available now.
COST: NS32SF640-25/50, $195 (10,000).
SECOND SOURCE: None.

National Semiconductor Inc
2900 Semiconductor Dr
M/S 16-320
Santa Clara, CA 95052
(408) 721-2636

DESCRIPTION: Called Swordfish by National, the 32SF640 has a 64-bit data bus but operates on 32-bit data. The 32SF641 is identical except that it includes a floating-point unit. A highly pipelined architecture lets the device perform more than one operation per cycle. It is more of a RISC μP than a DSP, but the 20-nsec multiplier lets it perform many DSP functions.



FEATURES: 20-, 25-, and 31-nsec cycle-time versions.
- One 32-bit address bus, two 64-bit data buses, and one 32-bit I/O data bus on chip.
- Separate data buses for program and data.
- No on-chip memory.
- 4G words of external address space.
- Two 32-bit ALUs.
- IEEE-754 32-bit and 64-bit floating-point unit on the 32SF641.
- Multiplier accepts 16- or 32-bit fixed-point data and returns 32-bit results.
- 512×64-bit instruction cache.
- 128×64-bit data cache.
- No barrel shifter.
- Thirty-two 32-bit register-based accumulators.
- DMA is supported via two DMA controllers.
- The stack is maintained in main memory.
- 15 external vectored interrupts.
- Hardware wait states.
- Serial debug port for in-circuit debugging.
- Packaged in a 223-pin PGA.

SUPPORT

HARDWARE

Hardware evaluation system includes development board.
In-circuit emulator by the end of 1992.

SOFTWARE

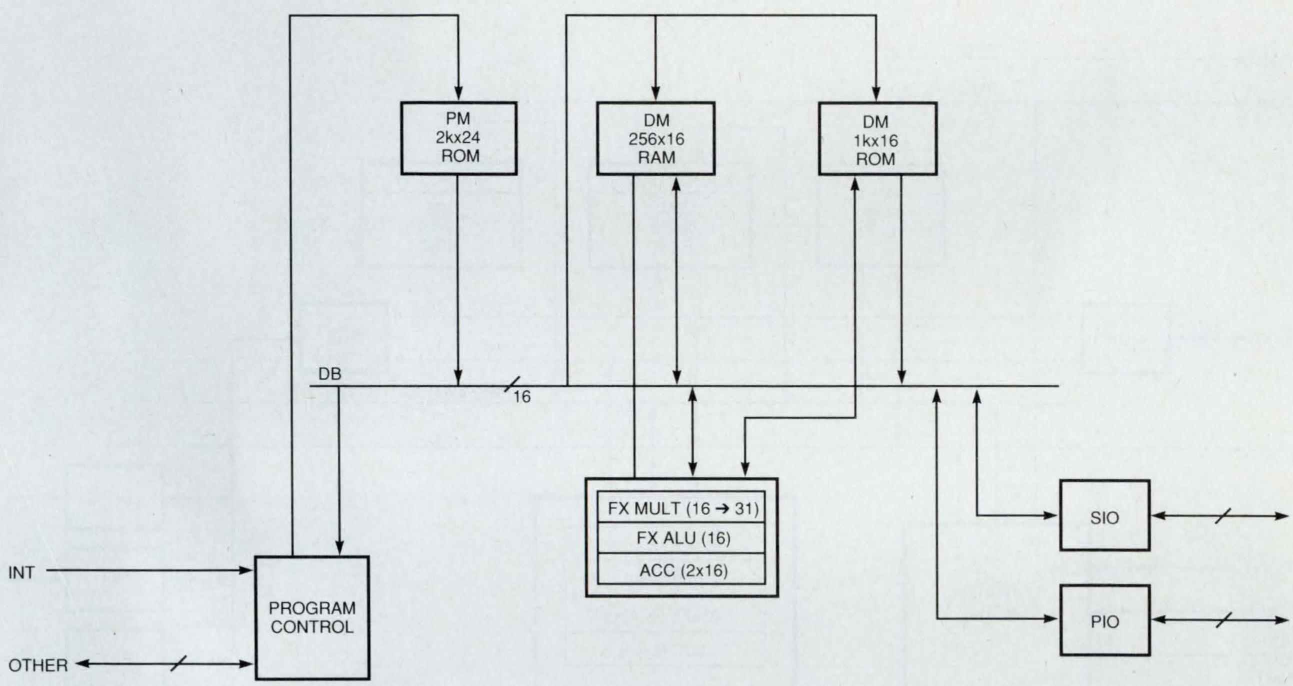
GNX tool set includes C compiler, Assembler, Source-level debugger, Profiler.
PXROS real-time operating system due by the end of 1992.

16-BIT FIXED-POINT DSP μP

AVAILABILITY: The 77C25 is available now.
COST: The 77C25 costs $9 (5000); the 77P25 costs $45 (1000).
SECOND SOURCE: Oki Semiconductor (Sunnyvale, CA) also makes the 7720.

NEC Electronics
401 Ellis St
Mountain View, CA 94039
(800) 632-3531; (415) 965-6158
FAX (800) 729-9288; (415) 965-6130
Circle No. 673

DESCRIPTION: The 77C25 is an upgrade of the 7720, which was one of the first successful DSP chips. The basic architecture is out of date, and its memory can't be expanded off chip. The manufacturer says there is still interest in new 77C25 designs because of the chip's low cost. The 77P25 is an EPROM version of the 77C25.



FEATURES: 100- and 122-nsec cycle time.
Single address bus only for program memory.
Pointers address data memory.
Single data bus for both program and data.
On-chip memory: The 77C25 has a 2k × 24-bit program ROM, a 256 × 16-bit data RAM, and a 1k × 16-bit data ROM. The 77P25 has the same memory as the 77C25 but replaces ROM with EPROM.
No external memory expansion.
One 8-bit serial I/O port.
Parallel I/O port.
Multiplier accepts 16-bit fixed-point data and produces 31-bit fixed-point results within two 16-bit accumulators.
16-bit ALU.
No barrel shifter.
Two 16-bit accumulators.
No zero-overhead looping.
No address generators.
No on-chip DMA controller.
4-level stack stores the program counter during subroutines and interrupts and is not expandable.
Single external interrupt.
No wait states.
No on-chip emulation port.
No low-power mode.
Packaged in 28-pin DIP, 28-pin PLCC, 44-pin PLCC, and 32-pin SOP.

SUPPORT

HARDWARE

Evaluation kit for application development also functions as an in-circuit emulator.

SOFTWARE

Assembler/linker.
Third-party simulator available.

μPD77016

16-BIT FIXED-POINT CMOS DSP μP

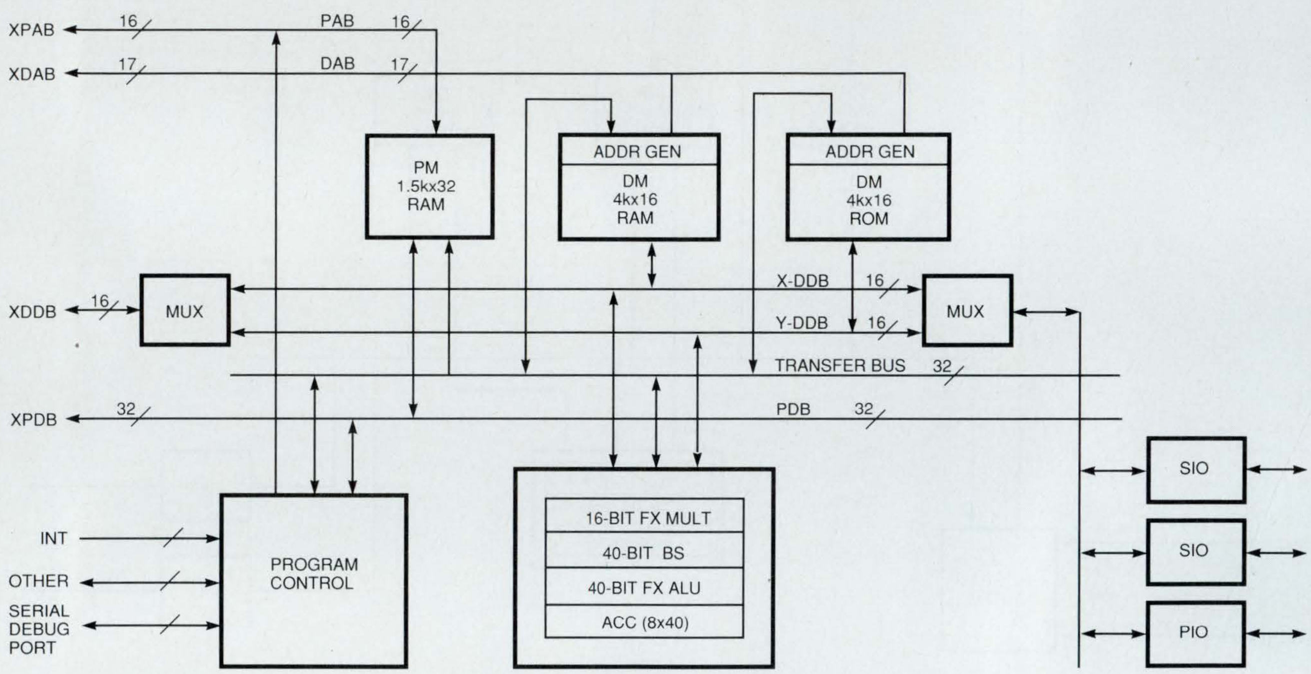
AVAILABILITY: Engineering samples, fourth quarter 1992. In production first half of 1993.

COST: 77016, 33 MHz, $55 (1000).

SECOND SOURCE: None.

NEC Electronics
401 Ellis St
Mountain View, CA 94039
(415) 965-6620
FAX (800) 729-9288
Circle No. 674

DESCRIPTION: This DSP is optimized for digital cellular phones and high-speed data/FAX modem applications. It has a Harvard architecture that is maintained off chip and a large amount of on-chip memory. The serial debug port allows for low-cost in-circuit emulation.



FEATURES: 30- and 50-nsec cycle-time versions.

Separate program and data buses maintained off chip.

Three internal data buses.

On-chip memory includes a 1.5k × 32-bit program RAM, a 4k × 16-bit data RAM, and a 4k × 16-bit data ROM.

Off-chip memory can be expanded to 64k × 32-bit program memory and 128k × 16-bit data memory.

Two serial I/O ports.

Parallel I/O port can be used as host μP interface.

Four general-purpose parallel I/O ports.

Multiplier accepts 16-bit fixed-point data and creates 40-bit fixed-point results within a 40-bit accumulator.

40-bit ALU.

40-bit barrel shifter.

Eight 40-bit accumulators.

Two address ALUs with circular buffering and bit-reversal addressing support.

On-chip DMA.

Zero-overhead looping.

12 interrupts (4 external/8 internal)

Wait-state control on both external buses.

On-chip emulation port.

Low-power mode.

Packaged in a 160-pin PQFP.

HARDWARE — SUPPORT — SOFTWARE

Hardware: Hardware emulator works with on-chip emulation port and runs on IBM PC.

Software:
Assembler/linker.
Simulator.
C compiler planned.

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EPOCH

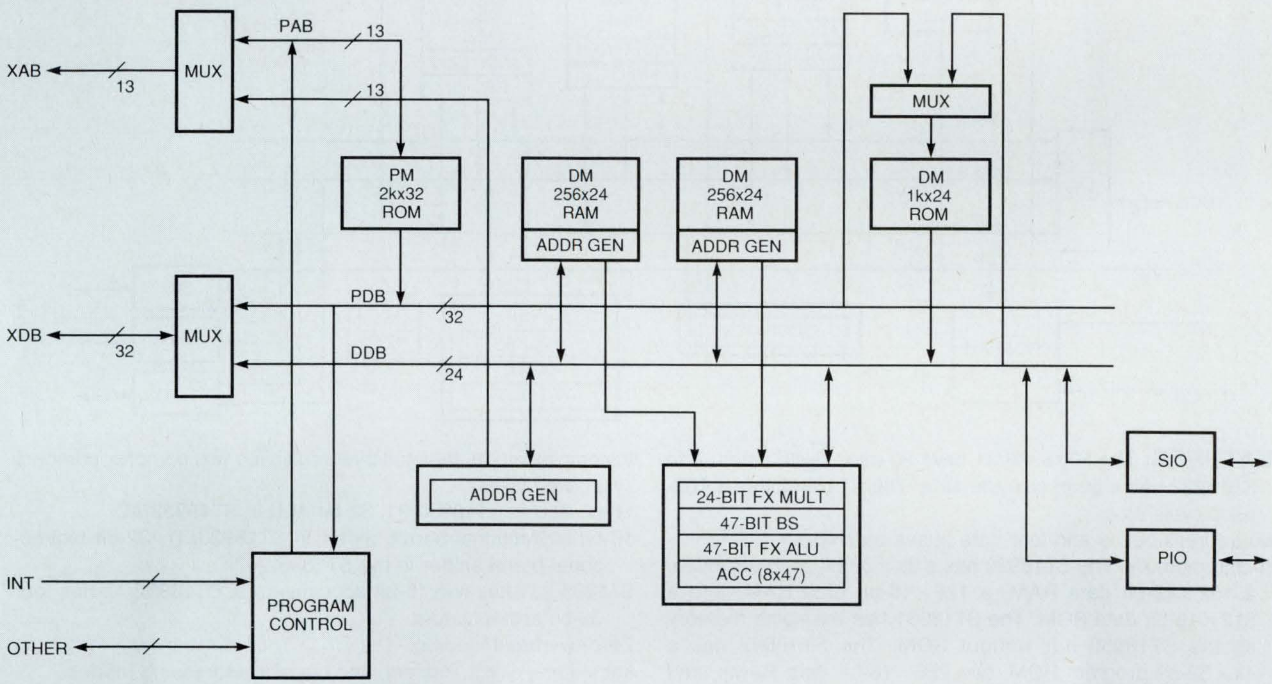
 CIRCLE NO. 64

24-BIT FIXED-POINT CMOS DSP μP

AVAILABILITY: 100- and 122-nsec versions available now.
COST: $30 (5000).
SECOND SOURCE: None.

NEC Electronics
401 Ellis St
Mountain View, CA 94039
(800) 632-3531; (415) 965-6158
FAX (800) 729-9288; (415) 965-6130
Circle No. 675

DESCRIPTION: The 77220 is a scaled-down version of the 32-bit floating-point 77230. The chip size and pin count are reduced by using 24-bit data and removing the floating-point exponent hardware. The 24-bit-word width suits the digital audio market. The instruction set is a subset of the 77230 and is source-code compatible with the floating-point device. The vendor says the 77220's architecture is optimized for adaptive filter applications. The 77P220R EPROM version and the 77P220L one-time-programmable version are for prototyping and low-volume applications.



FEATURES: 100- and 122-nsec cycle-time versions.
Separate on-chip program and data buses.
On-chip memory includes a 2k × 32-bit program ROM, dual 256 × 24-bit data RAMs, and a 1k × 24-bit data ROM.
Off-chip memory can be expanded to 8k × 32-bit program memory and 8k × 24-bit data memory.
One serial I/O port.
Parallel I/O port can be used as host μP interface.
Multiplier accepts 24-bit fixed-point data and creates 47-bit fixed-point results within a 47-bit accumulator.
47-bit ALU.
47-bit bidirectional barrel shifter.
Eight 47-bit accumulators.
Direct, indirect, immediate, circular, and bit-reversal addressing modes.
Three address generators.
No on-chip DMA.
Hardware stack is eight levels deep and is not expandable.
Two external interrupts.
No supported wait states.
No on-chip emulation port.
No low-power mode.
Packaged in a 68-pin PGA or 68-pin PLCC.

HARDWARE — SUPPORT — SOFTWARE

Hardware:
Evaluation kit and IBM PC-based evaluation board.

Software:
Assembler/linker.
Simulator.
C compiler.

ST18930/31/32/42

16-BIT FIXED-POINT CMOS DSP μP

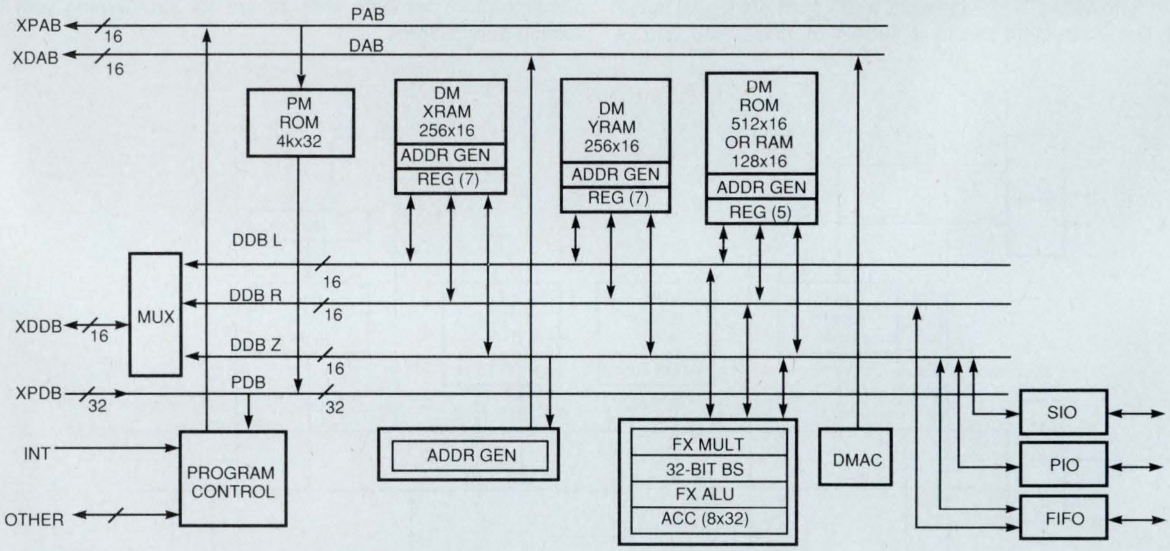
AVAILABILITY: Now.

COST: ST18930, $15 (10,000); ST18931, $75 (100); ST18942, $35 (10,000); ST18R942, $80 (100). The ST18932 is only available for ASIC designs.

SECOND SOURCE: None.

SGS-Thomson Microelectronics
1000 E Bell Rd
Phoenix, AZ 85022
(602) 867-6340
Circle No. 676

DESCRIPTION: The ST18 family consists of four devices. The ST18930 and -31 are CMOS versions of the NMOS original with a few enhancements and twice the speed. The ST18932 is a core for use in custom DSP μPs. The CMOS ST18942 offers further enhancements in its arithmetic capabilities, addressing modes, and I/O functions. All family members can operate on complex and double-precision data. The ST18932/42 have a 32-bit ALU and 16-bit data buses.



FEATURES: The ST18930/31 have 80-nsec cycle times. The ST18932 has a 50-nsec cycle time. The ST18942 has a 100-nsec cycle time.

Two address buses and four data buses on chip.

On-chip memory: The ST18930 has a 3k × 32-bit program ROM, a 192 × 16-bit data RAM, a 128 × 16-bit data RAM, and a 512 × 16-bit data ROM. The ST18931 has the same memory as the ST18930 but without ROM. The ST18942 has a 4k × 32-bit program ROM, two 256 × 16-bit data RAMs, and a 512 × 16-bit data ROM. The ST18R942 is a ROMless version of the ST18942 and has two 256 × 16-and one 128 × 16-bit data RAMs.

64k × 32-bit external program memory (except ST18930).

ST18930/31 4k × 16-bit external data memory space. ST18932 8k × 16-bit external data memory. ST18942 and ST18R942 64k × 16-bit external memory.

Only the ST18942 has both a serial I/O port and a parallel I/O port.

ST18932/42 multiplier accepts 16-bit fixed-point data and returns 32-bit fixed-point results to a 32-bit accumulator. The ST18930/31 returns 16-bit results.

In complex mode, the multiplier multiplies two complex numbers in two cycles.

16-bit ALU in ST18930/31. 32-bit ALU in ST18932/42.

16-bit bidirectional barrel shifter in ST18930/31. 32-bit bidirectional barrel shifter in the ST18932/42.

ST18930/31 has two 16-bit accumulators. ST18932/42 has four 32-bit accumulators.

Zero-overhead looping.

Immediate, direct, indirect, and circular addressing modes.

The ST18942 has on-chip DMA.

ST18930/31 has 1-, ST18932 has 2-, and ST18942 has 8-level hardware stack for interrupts and subroutines. All can be expanded into main memory with software.

Three external interrupts on the ST18930/31 and eight on the ST18932/42.

Hardware and software-programmable wait states.

Only the ST18932 has an on-chip emulation port.

Low-power mode.

Packaging: ST18930, 48-pin DIP, and 52-pin PLCC. ST18931, 124-pin PGA. ST18942, 160-pin PQFP. ST18R942, 160-pin PQFP and 144-pin PGA.

HARDWARE — SUPPORT — SOFTWARE

Hardware development system provides in-circuit emulation of as many as three DSP chips in real time.

Stand-alone emulator board connects to an IBM PC.

EPROM module. A ROMless version with EPROMs on a small board that plugs into a ROM-version socket.

Macroassembler/linker.

Simulator.

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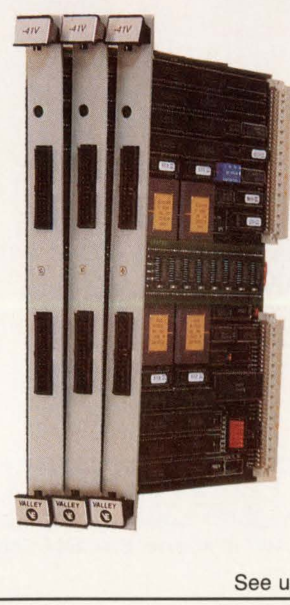

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CIRCLE NO. 53

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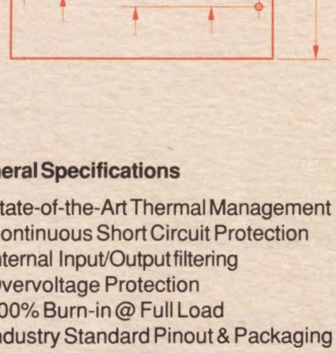

10 Watt

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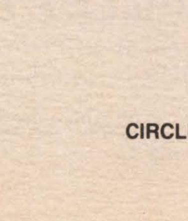
- V_{OUT}: 5, 12, 15, ±12, ±15



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CIRCLE NO. 68

24-BIT FIXED-POINT CMOS DSP μP

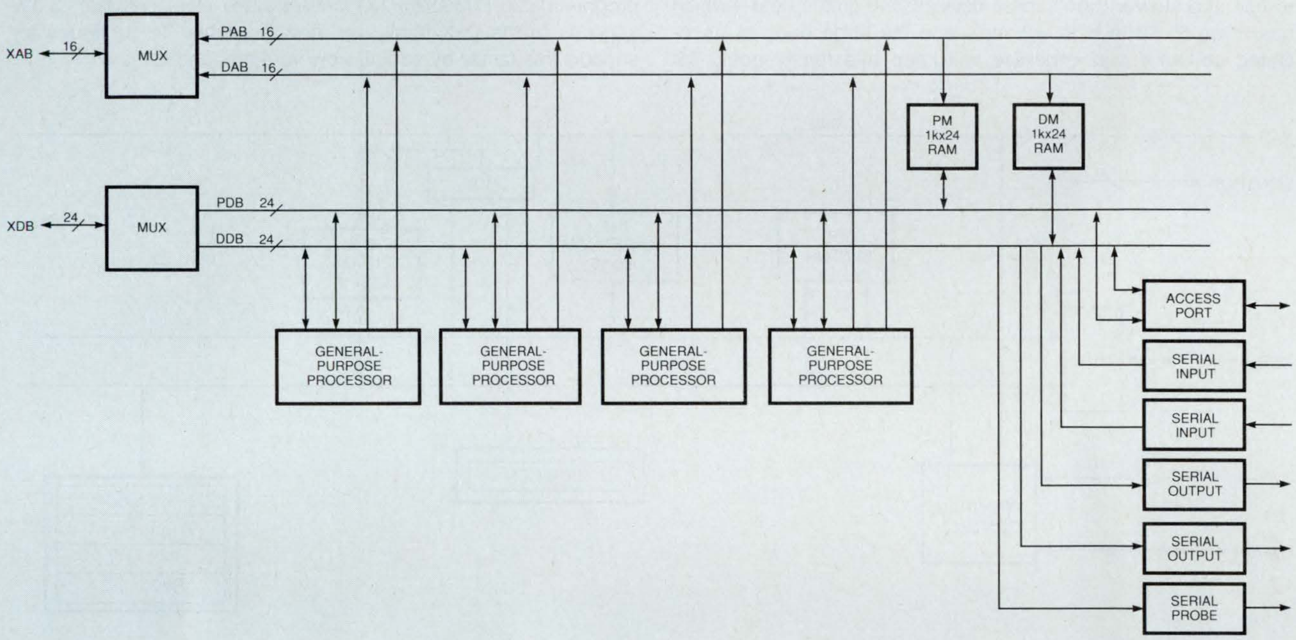
AVAILABILITY: Now.

COST: 50-MHz SPROC-1400 (four processors on chip), $70 (1000). By mid 1993, the SPROC-1000 (one processor) will cost $15 and the SPROC-1400 will cost $50.

SECOND SOURCE: None.

Star Semiconductor Corp
25 Independence Blvd
Warren, NJ 07059
(908) 647-9400
FAX (908) 647-4755
Circle No. 677

DESCRIPTION: The SPROC family has one, two, or four general-purpose processors on the chip. Programs are generated with signal flow diagrams, which are converted into code for the processors. Automatic partitioning of the code isolates you from the complexities of multiprocessing. You can very quickly create a system and see the results in real time. A probe port lets you see what the signal looks like anywhere in the block diagram.



FEATURES: 20-, 40-, and 50-MHz versions.
One to four general-purpose processors share common program and data memory.
Multiported data memory lets each processor access memory each cycle.
Separate instruction and data bus on chip.
Can access external memory via parallel port.
Serial data flow into and out of chip is controlled by Data Flow Managers with no impact on performance.
24-bit multiply with 56-bit accumulation.
Two serial input ports and two serial output ports.
Serial ports configurable for 8-, 12-, 16-, or 24-bit data.
Initialized by μP or external 8-bit EPROM.
Access port for development and debugging.
Probe port allows view of data at any point in the program. Output to DAC board allows real-time view on oscilloscope,
Parallel port transfers data to an external controller, peripheral, or memory.
Parallel port has hardware and software wait states.
Packaged in a 132-pin PGA.

SUPPORT

HARDWARE

An interface box and an evaluation board are included with the SPROClab.

SOFTWARE

SPROClab graphical development system. Includes signal flow editor, function block library, filter design tool, compiler, loading, and debugging tools.

TMS320C1X

16-BIT FIXED-POINT CMOS DSP µP

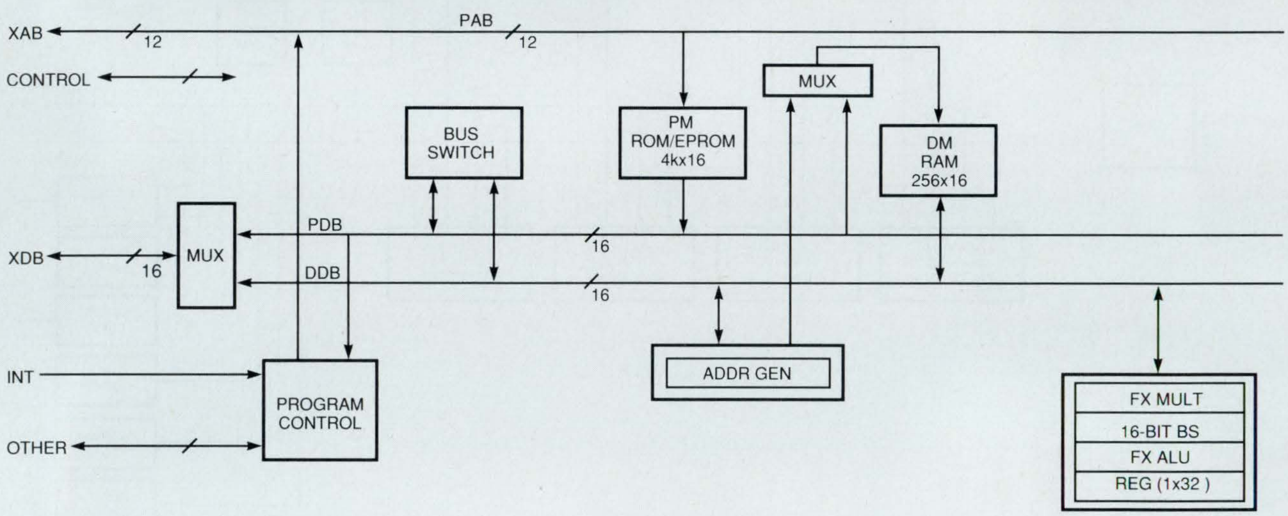
AVAILABILITY: The C10, C15, C16, C17, E14, E15, E17, P15, P17, P14, LC15 (3.3V), LC16 (3.3V), and LC17 (3.3V) are available now. The C14 will be available in the third quarter of 1992.

COST: C10 (20 MHz), $4.90; C14, $10; E14, $45; P14, $22; C15 (20 MHz), $7; E15 (20 MHz), $36; P15, $17; C16, $8.40; E17, $39; P17, $19 (C10, quantity 1; all others, quantity 1000).

SECOND SOURCE: Microchip Technology (Chandler, AZ) second-sources the C10, C14, and E14. No second source for other parts.

Texas Instruments Inc
Semiconductor Group
Box 809066
Dallas, TX 75380
(214) 995-6611, ext 3990
Circle No. 678

DESCRIPTION: This first generation of the vendor's DSP family was introduced in 1982. Although this family is difficult to use and slower than similar devices, the chip's cost—which has fallen to $3 in high volume—and the large body of associated software and expertise will keep this family going for some time. Newer family members have additional memory and peripheral options. EPROM (TMS320E1X) and one-time-programmable (TMS320P1X) versions are also available. 3.3V versions of the C1X family are now available. TI continues to support this family by adding new versions and tools.



FEATURES: 114-, 160-, 200-, and 280-nsec cycle-time versions. Separate on-chip program and data buses.

On-chip memory: The C10 has a 1.5k × 16-bit program ROM and a 144 × 16-bit data RAM. The C14, C15, and C17 have a 4k × 16-bit program ROM and a 256 × 16-bit data RAM. The E14, E15, and E17 have a 4k × 16-bit program EPROM and a 256 × 16-bit data RAM. The C16 has an 8k × 16-bit program ROM and a 256 × 16-bit data RAM. P1X versions are one-time programmable.

Program and data buses are combined off chip.

4k × 16-bit total external memory except the C16, which has 64k × 16-bit external memory, and the C17, which has no external memory.

On-chip peripherals: The C10, C15, and C16 have parallel I/O. The C14 has serial and parallel I/O. The C17 has two serial I/O ports, parallel I/O, and a compander.

Multiplier accepts 16-bit fixed-point data and creates 32-bit fixed-point results within a 32-bit accumulator.

32-bit ALU.

16-bit left barrel shifter.

Single 32-bit accumulator.

No zero-overhead looping.

No DMA.

4-level hardware stack except the C16, which has an 8-level hardware stack.

Single external interrupt.

No wait states.

No on-chip emulation.

LC1X devices operate at 3.3V.

Packaging: C10, 40-pin DIP or 44-pin PLCC. C14, 68-pin PLCC. C15, 40-pin DIP or 44-pin PLCC. C16, 64-pin QFP. C17, 40-pin DIP or 44-pin PLCC.

SUPPORT

HARDWARE

In-circuit emulator.

Evaluation module.

Software development system.

Many third-party support tools. Contact manufacturer for a list of third-party vendors.

SOFTWARE

Assembler/linker.

Simulator.

Application library.

Many third-party support tools.

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CIRCLE NO. 69

16-BIT FIXED-POINT CMOS DSP μP

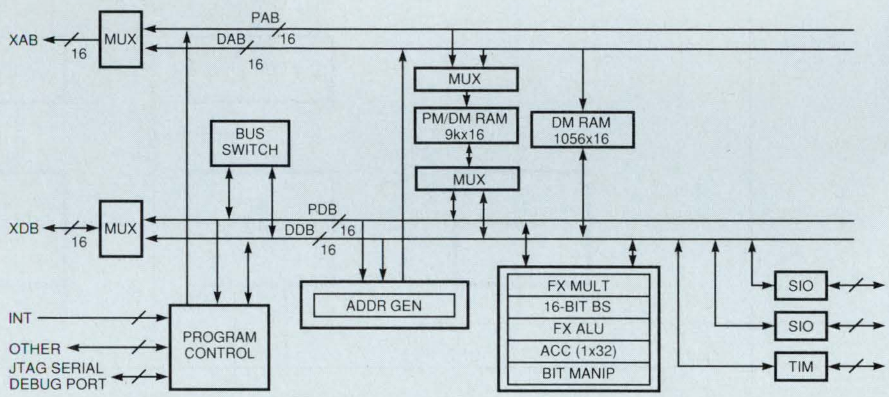
AVAILABILITY: The C25, C26, E25, C50, and C51 are available now. The C28 is sampling now and will be in production in the first quarter of 1993. The C53 is sampling now and will be in production in the fourth quarter of 1992.

COST: C25 (33 MHz), $13; C25 (40 MHz), $13.50; E25, $67; C26, $15; C50, $106; C51, $33; C53, $50 (C25 quantity 1, all others, quantity 1000).

SECOND SOURCE: None.

Texas Instruments Inc
Semiconductor Group
Box 809066
Dallas, TX 75380
(214) 995-6611, ext 3990
Circle No. 679

DESCRIPTION: These chips make up the second and third generation of the vendor's fixed-point DSP family. They offer higher performance than the first-generation chips and are easier to use. For many applications, the C25's price has fallen to a point where the chip is replacing the C1X. The C5X parts are enhancements to the C25. They use the same basic core architecture as the C25 but have double the performance level, additional on-chip peripherals, and expanded memory. New family members include the C28 (which expands memory and adds a power down mode to the C25) and the C53 (which expands memory to the C5X).



FEATURES: The C2X chips come in 78-, 98-, and 125-nsec cycle-time versions. The C5X chips come in 35- and 50-nsec cycle-time versions.

On-chip memory: The C25 has a 4k × 16-bit program ROM and a 544 × 16-bit data RAM. The C26 has a 1.5k × 16-bit program RAM with boot ROM to load programs from external memory and a 544 × 16-bit data RAM. The C28 has an 8k × 16-bit program ROM and 544 × 16-bit data RAM. The C50 has a 9k × 16-bit program/data RAM and a 1056 × 16-bit dual-access RAM. The C51 has an 8k × 16-bit program ROM, a 1k × 16-bit program/data RAM, and a 1056 × 16-bit dual-access RAM. The C53 has an 16k × 16-bit program ROM, a 3k × 16-bit program/data RAM, and a 1k × 16-bit dual access RAM.

Program and data memory are combined off chip.

The C2X and C5X can address 64k × 16-bit program and 64k × 16-bit data memory.

The C25 and C26 have one serial port each. The C5X has two serial ports.

Multiplier accepts 16-bit fixed-point data and creates 32-bit fixed-point results within a 32-bit accumulator.

32-bit ALU.

The C5X has a separate 16-bit parallel logic unit for manipulating bits without affecting the contents of the accumulator.

16-bit left barrel shifter.

Single 32-bit accumulator.

Next-instruction-repeat looping. Only the C5X has zero-overhead block looping.

Immediate, direct, indirect, and bit-reversal addressing modes. C5X also has circular addressing.

No DMA.

8-level expandable hardware stack.

C5X has a 1-level-deep shadow RAM, which stores some registers.

C2X has three external interrupts; C5X has five.

Hardware wait states. C5X also has software-programmable wait states.

The C5X has an on-chip emulation port.

The C2X is source-code compatible with the C5X.

The C5X has a JTAG interface.

The C25 and C26 have an idle mode. The C28 and the C5X have a power-down mode.

Packaging: C25 and C26, 68-pin PGA or PLCC. C28, 80-pin QFP. C50, C51, and C53, 132-pin QFP.

HARDWARE — SUPPORT — SOFTWARE

Hardware

Both the C2X and C5X have an in-circuit emulator, a software-development board for the IBM PC, evaluation boards.

Many third-party support tools. Contact manufacturer for a list of third-party vendors.

Software

C compiler.

Source-level debugger.

Assembler/linker.

Simulator.

Application library.

Many third-party support tools.

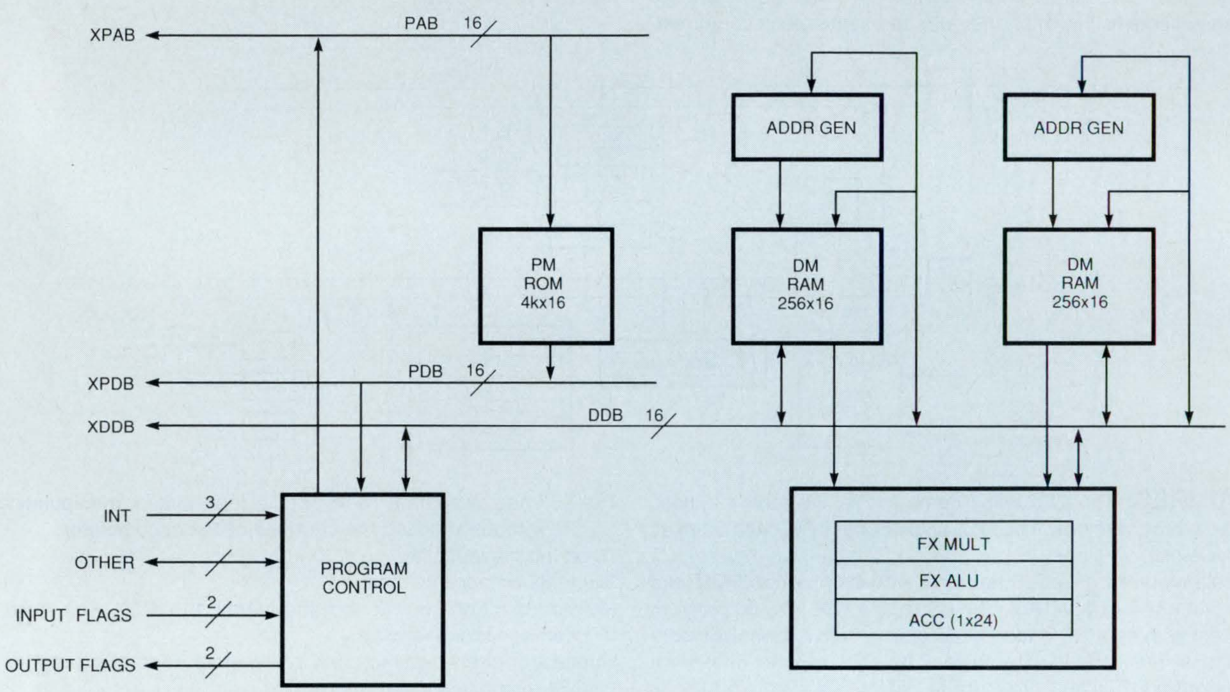
Z89C00

16-BIT FIXED-POINT CMOS DSP μP

AVAILABILITY: Now
COST: Z89C00, $15 (100), $5 (25,000).
SECOND SOURCE: None.

Zilog Inc
210 E Hacienda Ave
Campbell, CA 95008
(408) 370-8000
FAX (408) 370-8056
Circle No. 680

DESCRIPTION: Zilog created the Z89C00 to let them provide system-level μCs with on-chip DSP capability. They consider the Z89C00 to be a competitive DSP chip and are supporting it as a stand-alone device. In 1993 they will introduce an enhanced version that will be code compatible with the Z89C00. The device is made with a process that can be made to operate at 3V.



FEATURES: 100-nsec cycle time.
On-chip memory: 4k × 16-bit program ROM and dual 256 × 16-bit data RAM.
64k × 16-bit off-chip program ROM.
Can access external memory via eight 16-bit memory locations. Intended to interface to FIFO, DMA controller, or μC.
16-bit parallel I/O, two output flags, and two input flags.
Multiplier accepts 16-bit fixed-point data and creates 32-bit fixed-point result, but only the top 24-bits are usable.
24-bit ALU.
No barrel shifter.
Single 24-bit accumulator.
No zero-overhead looping.
8 address registers. Circular buffering supported.
No on-chip cache.
No DMA.
6-level hardware stack.
3 external interrupts.
Hardware wait states.
Power down via external pin.
No on-chip emulation.
Packaging: 68-pin PLCC.

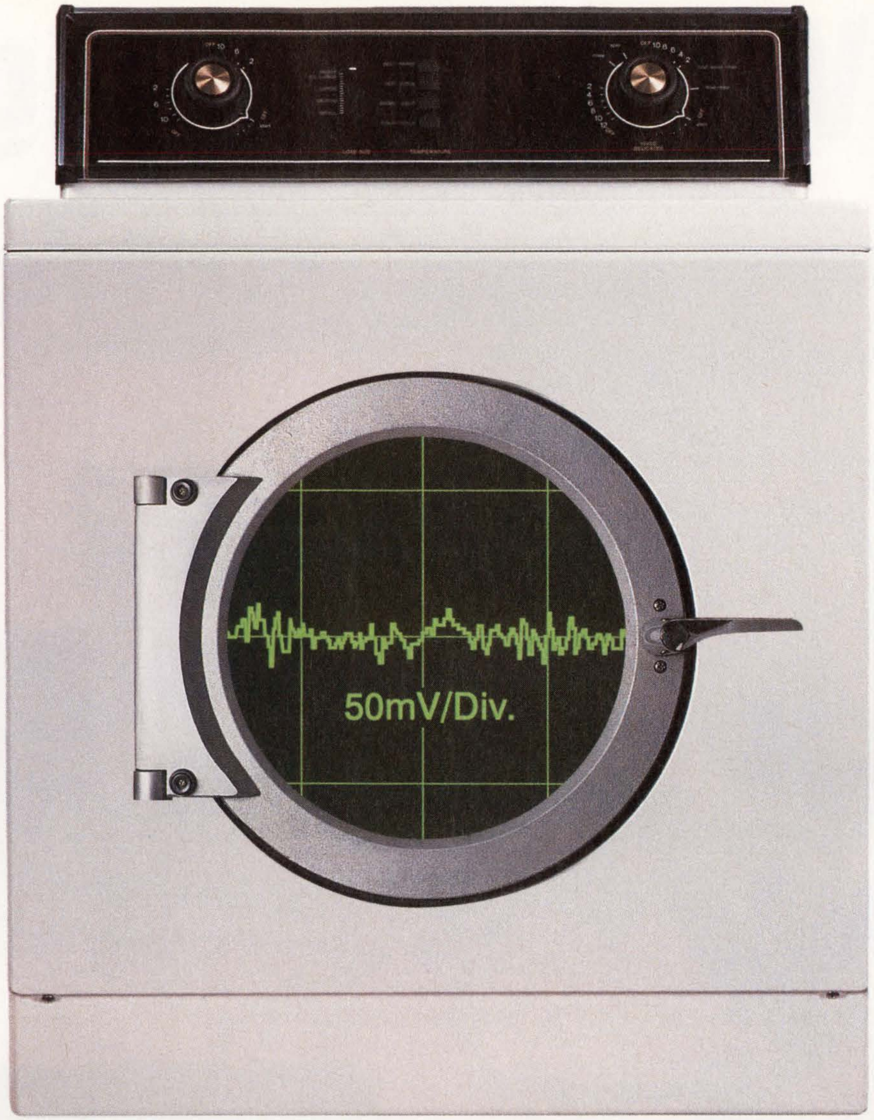
SUPPORT

HARDWARE

In-circuit emulator.
Evaluation board.

SOFTWARE

Assembler/linker.
Simulator.
C compiler.
Source-level debugger.
Application library.
TMS320 to Z89C00 assembly code translator.



EMS II High Power Switchers. You've never seen power this clean.

The new EMS II Series Switch Mode DC Power Supplies give you clean power, every time...with no glitches, spikes or headaches. In fact, they handle the highest load of power per cubic inch in the industry. Here are some more features to make your decision easier:

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ELECTRONIC MEASUREMENTS, INC.
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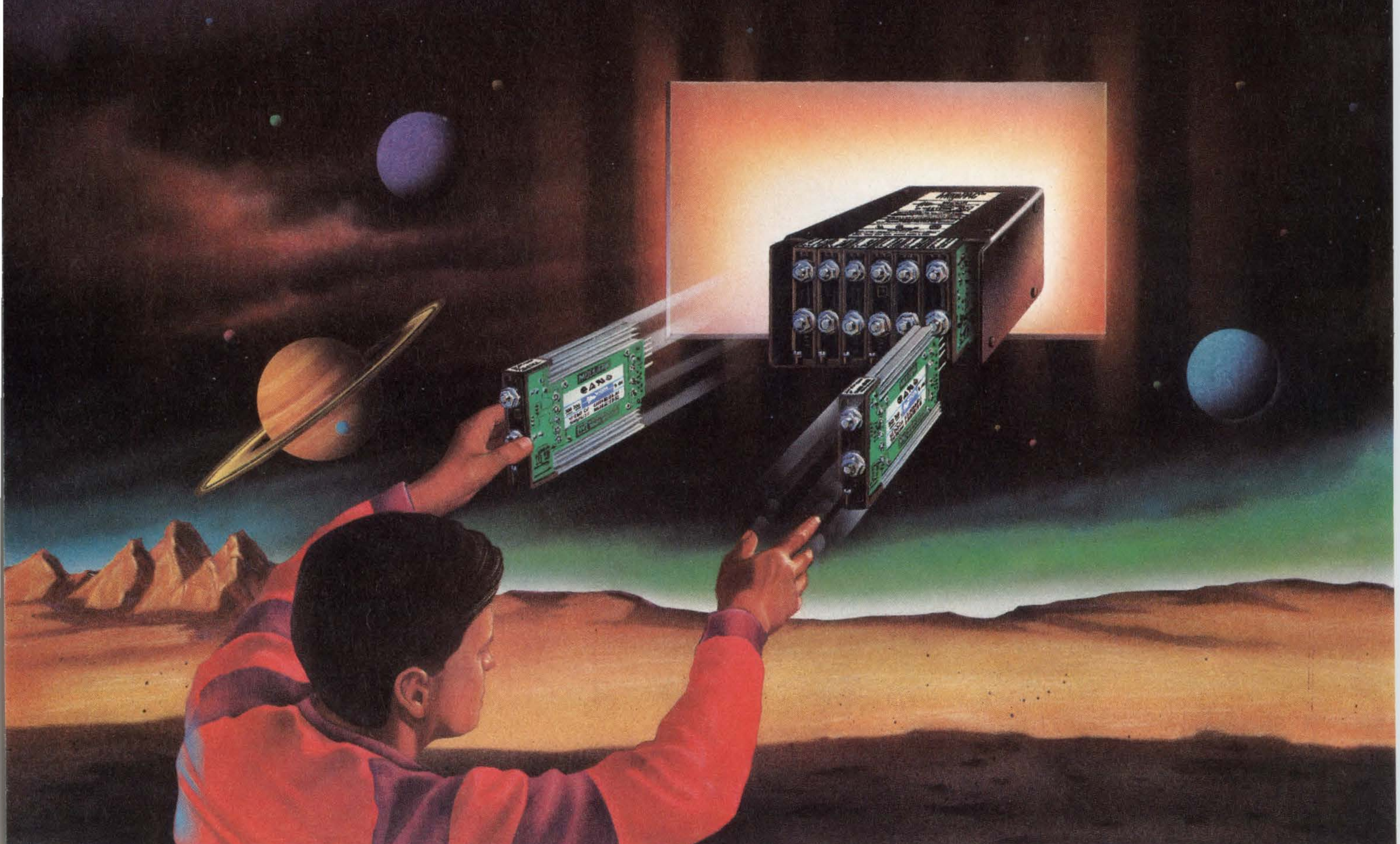
CIRCLE NO. 70

POWER To Configure



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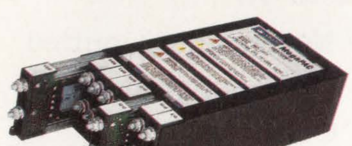
Power: Up to 1200 Watts
Input: 110/220 VAC, strappable; 300 VDC
Outputs: 1 to 8 isolated and fully regulated, 2 to 95 VDC
Size: 11.8"L x 6.0"W x 3.4"H



Plug into *instant power supply configurability* with the new MegaPAC switcher from our Westcor division. MegaPAC outputs can be configured in virtually an infinite number of voltage and power combinations using up to 8 slide-in **ModuPAC™** assemblies. Want to change a voltage or power level at your factory or at a customer site? No problem. . .shut down input power, slide out the ModuPAC you want to replace and slide in the new one. It's that simple.

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Call VICOR EXPRESS (800) 735-6200 for information and be sure to ask for a MegaPAC data sheet. Or call WESTCOR (division of Vicor) at (408) 395-7050. Fax us at (508) 475-6715 or (408) 395-1518.

VICOR

VICOR Corporation
23 Frontage Road, Andover, MA 01810

Component Solutions For Your Power System

CIRCLE NO. 71

32/40-BIT FLOATING-POINT CMOS DSP µP

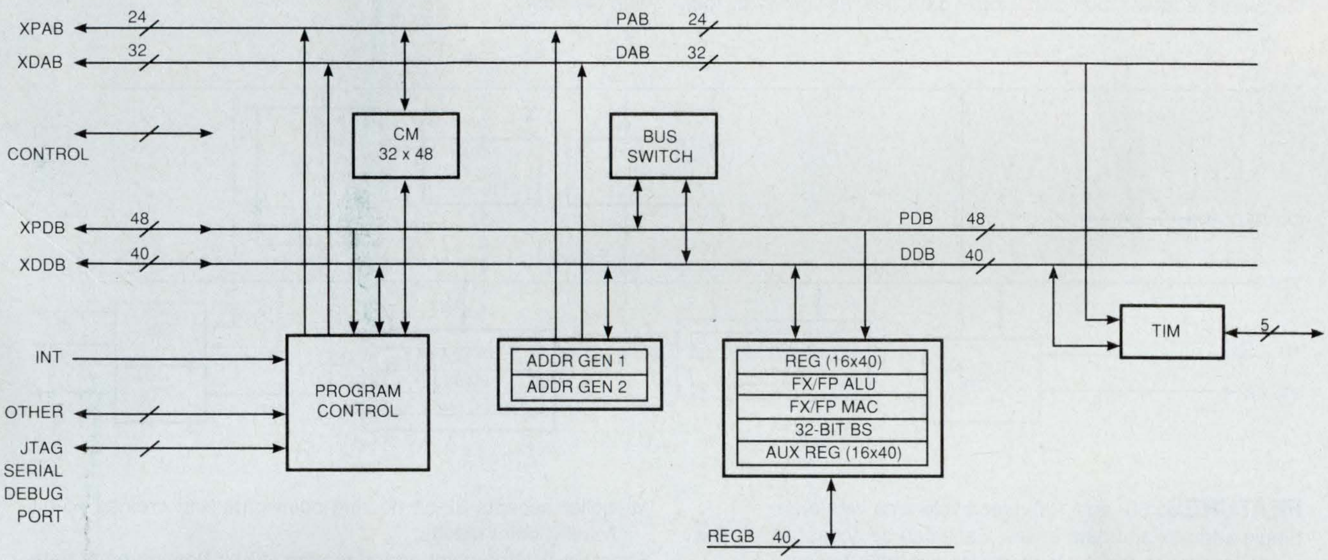
AVAILABILITY: The ADSP-21020 and ADSP-21010 are now in production.

COST: ADSP-21020, 33-MHz, $220 (1000); ADSP-21020, 20-MHz, $176 (1000); ADSP-21010, 12.5-MHz, $49.90 (100).

SECOND SOURCE: None.

Analog Devices Inc
Box 9106
Norwood, MA 02062
(617) 461-3881
Circle No. 681

DESCRIPTION: This family has an off-chip Harvard architecture and is similar to the fixed-point 2100 family. On-chip emulation is supported via a JTAG port. The device conforms to the IEEE-754 floating-point standard. It has an algebraic-like assembly language along with high-level-languange support. The ADSP-21010 is a new lower-cost addition to the family. It lacks only the 40-bit floating-point support.



FEATURES: 21020 has 30-, 40-, and 50-nsec cycle-time versions. 21010 has 80-nsec cycle time.
One 32-bit and one 24-bit address bus.
One 40-bit and one 48-bit data bus.
Seven 40-bit additional buses in the CPU.
Separate program, and data buses (off-chip Harvard Architecture).
4G × 40-bit external data memory and 16M × 48-bit external program memory.
One 32-bit timer.
IEEE-754 32-bit and 40-bit floating point format. 21010 supports only 32-bit format.
Multiplier accepts 32 and 40-bit floating-point data and returns 32 or 40-bit results. 32-bit fixed-point operands produce 64-bit fixed-point products. The multiplier also incorporates dual 80-bit fixed-point accumulators.
ALU accepts 32 and 40-bit floating-point data and returns 32 or 40-bit results. 32-bit fixed-point operands produce 32-bit results.
Parallel multiplier and ALU operate in single cycle.
32-bit bidirectional barrel shifter (64-bit result).
32 40-bit register-based accumulators.
Zero overhead looping.
32 × 48-bit instruction cache.
Cache optimizes performance by selecting only 3-bus-operation instructions for storage in cache. Cache can be frozen to keep often-used instructions in cache.
Register, direct, indirect, immediate, relative, circular-buffer, and bit-reversed addressing modes. Two independent address generators.
The hardware stack is 20 deep and can be expanded into main memory.
Four external vectored interrupts.
Four bidirectional I/O flags.
Hardware- and software-programmable wait states.
JTAG support of in-circuit emulation.
IDLE state for low-power mode.
Packaging: 223-pin ceramic PGA and 304-pin PQFP.

SUPPORT

HARDWARE

Full-speed in-circuit emulator.
Demo board for IBM PC.
Evaluation package.
Third-party support: Contact Analog Devices for a list of third-party vendors.

SOFTWARE

Optimizing ANSI C and Numerical C compilers.
Source-level debugger for ANSI C/Numerical C.
Simulator, Assembler, Linker, PROM Splitter.
Application libraries.
Third-party support includes real-time multitasking operating system (SPOX), filter design packages with code generation, block-level algorithm development package.

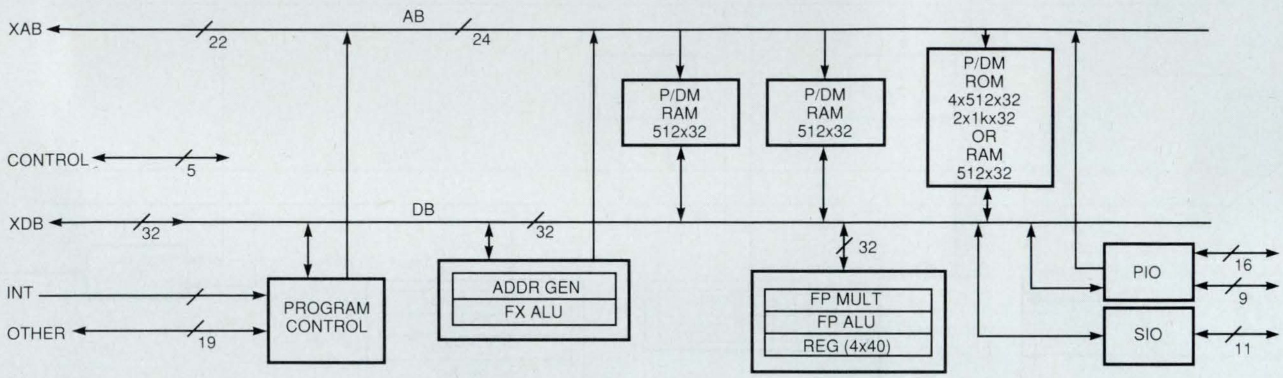
DSP32C/3210

32-BIT FLOATING-POINT CMOS DSP μP

AVAILABILITY: The DSP32C and DSP3210 are available now.
COST: DSP32C, $70 (1000); DSP3210, $50 (100,000).
SECOND SOURCE: None.

AT&T Microelectronics
Dept 52AL300240
555 Union Blvd
Allentown, PA 18103
(800) 372-2447, ext 796;
in Canada, (800) 553-2448, ext 796
Circle No. 682

DESCRIPTION: The DSP32C has one of the simplest architectures of the 32-bit floating-point DSP chips. It uses a single 4M-word linear memory space instead of the separate program and data memory common in other DSP chips. You can access the single address bus and single data bus as many as four times per cycle. You can access each internal memory as many as two times per cycle. The DSP3210, along with the VCOS operating system, is intended for use on the mother board of personal computers and workstations where it shares memory with the host.



FEATURES: 80- and 100-nsec cycle-time versions.

Single address and data buses. Each can be accessed as many as four times per cycle to imitate separate buses.

DSP32C has three on-chip 512×32-bit RAMs. Optional ROM-based DSP32C replaces one RAM with a 4k×32-bit ROM. DSP3210 has two 1k×32-bit RAMs and a 256×32-bit boot ROM.

The DSP32C can address as much as 4M×32-bits of external memory. The DSP3210 can address 4G bytes of external memory.

All memory is a general resource; both program and data can exist anywhere.

Data addressable as 8-, 16-, or 32-bit words.

DSP3210 can load program from external EPROM.

The DSP32C has on-chip serial and parallel I/O. The DSP3210 has serial I/O, timer, DMA controller, and a 32-bit bus interface that is compatible with Motorola and Intel μPs.

The serial I/O is a double-buffered port that allows concurrent input and output of 8-, 16-, 24-, or 32-bit data widths.

The DSP32C has an 8- or 16-bit parallel I/O port that an external μP can control.

Proprietary 32-bit floating-point format.

Single-cycle conversion to/from nonstandard DSP32 floating-point format from/to IEEE-754 floating-point format.

Multiplier accepts 32-bit floating-point data and creates 45-bit floating-point results.

Separate floating-point adder accepts 40-bit floating-point data and creates 40-bit floating-point results.

Fixed-point ALU accepts 16- or 24-bit data.

Does not have a barrel shifter.

Four 40-bit accumulators.

Zero-overhead looping. As many as 2048 repeats of a block with a maximum size of 32 words.

Immediate, memory-direct, register-direct, register-indirect, and bit-reversal addressing modes.

You can use the DMA with both the serial I/O and the parallel I/O.

No hardware stack.

1-level-deep shadow RAM of some registers.

Two external interrupts.

Hardware wait states. DSP3210 has software-programmable wait states.

No on-chip emulation port.

Only the DSP3210 has a low-power mode.

DSP32C packaged in a 164-pin PQFP, 133-pin PGA, or 68-pin PLCC (μC version, no external memory).

SUPPORT

HARDWARE

In-circuit emulator.

IBM PC-based development board.

VME bus-based development board.

Many third-party support tools, including the HP64773 in-circuit emulator from Hewlett-Packard. Contact AT&T for a list of third-party vendors.

SOFTWARE

Optimizing C compiler.

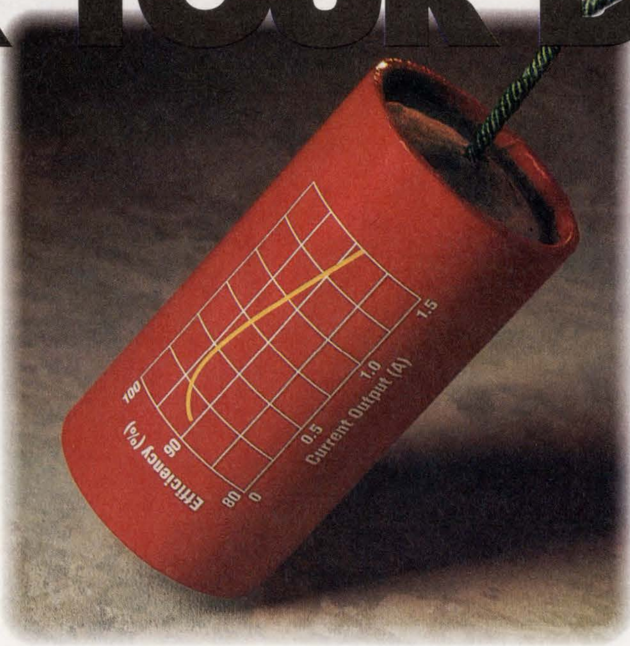
Assembler/linker.

Simulator.

VCOS operating system and multimedia modules.

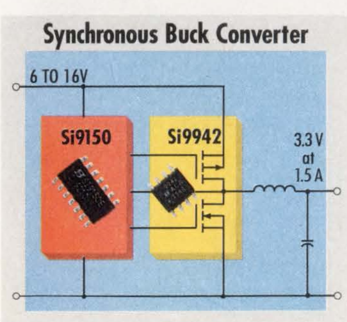
What do designers of notebook computers and other battery-powered systems get with Siliconix' new power conversion chip set?

MORE BANG FOR YOUR BUCK.



That means higher power conversion efficiency, smaller system size, both 3.3-V and 5-V compatibility and longer battery life. DC/DC conversion at 94% measured efficiency.

This high-efficiency produced by our new power conversion chip set, the Si9150DY Sychrononous Buck Converter and the Si9942DY LITTLE FOOT™MOSFET allows your DC/DC converter to run cooler and adds about 10% to battery life during normal operation. And in sleep mode it only consumes 100 μA, to extend battery life by 1000%.



The smallest and simplest high-efficiency solution available.

The controller, in a tiny SO-14 package, is highly integrated and requires few external parts. Team it with our LITTLE FOOT SO-8 to achieve the most compact converter design possible. Our Si9150 design manual includes complete instructions for building your DC/DC converter. The bottom line result… your product gets to market faster!

Operating voltage options.

Many "next-generation" designs are employing lower, and sometimes multiple operating voltages. That's why our Si9150DY/Si9942DY buck converter takes unregulated battery voltage and converts it into 5.0 V or 3.3 V.

Get more bang for your buck converter!

For OEM quantities, prices of this 94% efficient power conversion chip set can be yours for less than $3.00.

More power efficiency, more compact design, and more voltage options are as close as your local Siliconix sales office. Or call toll-free hot line now! **(0635) 30905, ext. 970.** Ask for the "More Bang for your Buck" Design Manual.

Siliconix

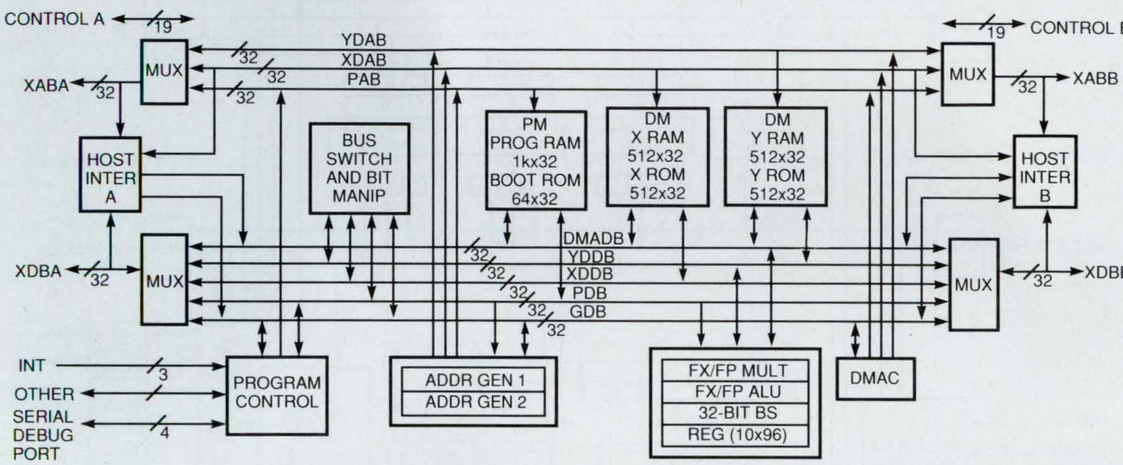
Weir House, Overbridge Square, Hambridge Lane, Newbury, Berks RG14 5UX

32-BIT FLOATING-POINT CMOS DSP μP

AVAILABILITY: Available now.
COST: 96002 (33 MHz) costs $368; 96002 (40 MHz) costs $441.
SECOND SOURCE: None.

Motorola Inc
Microprocessor Products Group
6501 William Cannon Dr
Austin, TX 78735
(512) 891-2030
FAX (512) 891-0400
Circle No. 693

DESCRIPTION: The 96002 is an architectural superset of the fixed-point 56001. The 96002 continues Motorola's emphasis on precision. The 96-bit accumulators will support future double-precision parts. The 32-bit floating-point device conforms to the IEEE-754 floating-point standard. The dual 32-bit external buses support glueless multi-96002 systems. The external buses can access external memory and peripherals or communicate with a host μP.



FEATURES: 50-, 60-, and 74-nsec cycle-time versions.

Three 32-bit address buses and five 32-bit data buses on chip.

Separate address buses for program and the two on-chip RAMs.

Separate data buses for program, the two on-chip RAMs, global data, and DMA.

On-chip memory includes a 1k×32-bit program RAM, a 64×32-bit boot ROM, dual 512×32-bit data RAMs, and dual 512×32-bit data ROMs.

On-chip boot ROM loads program from external byte-wide EPROM.

Revised version will let the internal 1k×32-bit program RAM function like an instruction cache.

Two complete 32-bit external expansion ports for memory and I/O.

Three separate memory spaces (X, Y, and P). Each can address 4G words.

Each memory space is divided into eight 0.5G-word areas. Each can be programmed to either the A or B expansion ports.

Two host interfaces allow interface to μP or other 96002s. No other on-chip peripherals.

IEEE-754 32-bit floating-point format.

Multiplier accepts 32-bit floating-point data and returns 44-bit results. Multiplier accepts 32-bit integer data and returns 64-bit results.

32-bit bidirectional barrel shifter.

Ten 96-bit or thirty 32-bit register-based accumulators.

Zero-overhead looping.

Immediate, direct, indirect, circular, and bit-reversal addressing modes.

Two address ALUs.

Supports DMA. Uses its own internal bus and doesn't cycle-steal. Can use all of the addressing modes, including bit-reversal, with the DMA controller.

The stack is 15 levels deep, expandable into main memory.

Three external vectored interrupts.

Hardware and software-programmable wait states.

Serial debug port for in-circuit debugging.

Low-power mode.

Packaged in a 223-pin PGA.

HARDWARE — SUPPORT — SOFTWARE

Hardware evaluation system includes in-circuit emulator.

Some third-party hardware products are available. Contact Motorola for a list of third-party vendors.

Optimizing C compiler.

Assembler/linker.

Simulator.

Application library.

GNU C compiler and source-level debugger.

Third-party support includes optimizing C compiler, block-level diagramming language, filter-design software, and real-time operating system (SPOX).

32-BIT FLOATING-POINT CMOS PARALLEL DSP µP

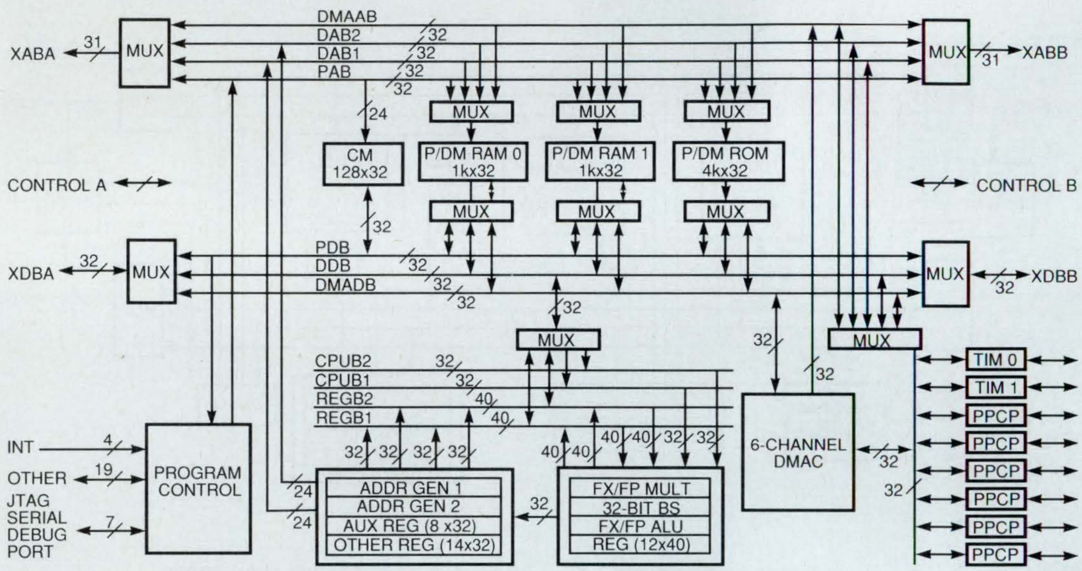
AVAILABILITY: Preproduction available now. Production quantities in fourth quarter of 1992.

COST: Pre-production $390 (100). Production $250 (5000).

SECOND SOURCE: None.

Texas Instruments Inc
Semiconductor Group, SC-9026
Box 809066
Dallas, TX 75380
(800) 336-5236, ext 700
Circle No. 685

DESCRIPTION: This device was designed for applications that require the performance of parallel processing. It is upward compatible with the C30 but adds six 32-bit FIFO dual-buffered communication ports, two complete 32-bit external buses, an analysis module that supports multiprocessor debugging via a JTAG interface, and a 4G-word address space. The chip also features single-cycle conversion to/from the IEEE floating-point standard and a cycle time of 40 nsec. Each communication port can transfer data to/from another C40 at 20 Mbytes/sec without any external logic.



FEATURES: 40- and 50-nsec cycle time.

Four 32-bit address buses and three 32-bit data buses.

Two 32-bit and two 40-bit additional buses in the CPU.

Separate program, data, and DMA buses.

Each internal RAM and ROM allows two accesses per cycle.

Any of the separate memories can be used for program or data.

Two on-chip 1k × 32-bit RAMs and a 4k × 32-bit ROM.

Dual 32-bit external buses. Each has a 31-bit address, so the 4G-word memory is equally divided between the two buses.

Six independent 32-bit communication ports for glueless communications between C40s. Separate 8 × 32-bit FIFOs for input and output buffering.

No on-chip serial ports. Two 32-bit timers.

Proprietary 2's complement 32-bit floating-point format.

Single-cycle conversion to/from the IEEE-754 32-bit format.

Multiplier accepts 32-bit floating-point data and returns 40-bit floating-point data. 24-bit integers result in 32-bit fixed-point results.

ALU operates on 40-bit floating-point and 32-bit fixed-point data.

Parallel multiplier and ALU operations in a single cycle.

32-bit bidirectional barrel shifter.

Twelve 40-bit register-based accumulators.

Single-instruction and zero-overhead block looping.

128 × 32-bit instruction cache.

You can disable cache when it's not needed and freeze it to keep an often-used portion of code available in the cache.

Register, direct, indirect, immediate, relative, circular, and bit-reversed addressing modes. Two address ALUs.

6-channel DMA controller for concurrent I/O and CPU operation.

Transmitting DMA can control the operation of the receiving DMA, so setup for DMA transfer will not affect CPU.

Hardware pointer to software stack.

Four external vectored interrupts.

Hardware- and software-programmable wait states.

JTAG-based debug port controls the analysis module, which functions as an in-circuit emulator. Multiple C40s can be debugged via JTAG interface.

Packaged in a 325-pin ceramic PGA.

HARDWARE — SUPPORT — SOFTWARE

Hardware

Development system includes in-circuit emulation via JTAG interface.

4-processor host-independent evaluation board.

Third-party support. Contact TI for a list of vendors.

Software

Optimizing ANSI C compiler with parallel-processing runtime support.

Source-level debugger. Assembler/linker. Simulator.

Application library.

Third-party support includes SPOX, Helios, 3L, parallel C and Ada operating systems and languages.

32-BIT FLOATING-POINT CMOS DSP μP

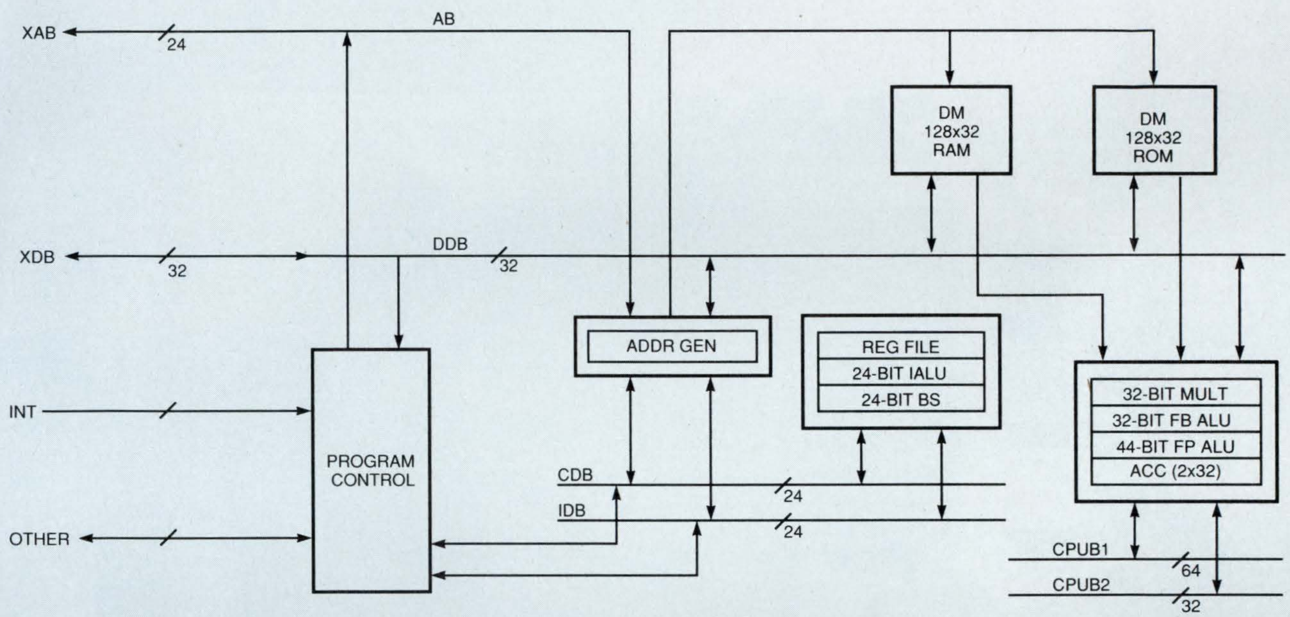
AVAILABILITY: Now.

COST: The 34325 (25 MHz) costs $137; the 34325 (20 MHz) costs $124 (10,000).

SECOND SOURCE: None.

Zoran Corp
1705 Wyatt Dr
Santa Clara, CA 95054
(408) 986-1314
FAX (408) 986-1240
Circle No. 688

DESCRIPTION: The ZR34325 is a vector-signal processor, which is a DSP chip that operates on complex data and large blocks of data with single high-level instructions. The instruction set includes a single instruction to calculate an FFT, FIR filter, IIR filter, and other complex functions. The highly specialized architecture is optimized to perform these functions quickly. The architecture also eases programming because the programmer doesn't have to write code for complex DSP functions. The 32-bit floating-point data conforms to the IEEE-754 standard.



FEATURES: 80- and 100-nsec cycle-time versions.
Single address and data bus.
Vector instructions generally take longer to execute than to fetch, so little speed penalty is incurred with this simple bus architecture.
High-level instructions, such as those to calculate FFTs and FIR and IIR filters, simplify programming.
256 × 32-bit coefficient dual-port ROM and 128 × 32-bit dual-port RAM on chip.
No on-chip program memory.
Internal memory can be directly accessed by external device.
16M × 32-bit memory space.
No on-chip peripherals.
IEEE-754 32-bit floating-point format.
Multiplier accepts 32-bit floating-point data and creates 44-bit results.
Three ALUs: two floating point and one integer. 32-bit floating-point data can be added to 32 bits with one ALU and to 44 bits with the other.
24-bit bidirectional barrel shifter.
Two 32-bit accumulators.
No zero-overhead looping.
Direct, indirect, register, immediate, circular, and bit-reversed addressing modes.
Address generators for internal RAM and ROM.
On-chip DMA.
Slave mode opens chip to external access.
Hardware stack maintained in main memory.
Single external interrupt.
Hardware wait states.
No on-chip emulation port.
No low-power mode.
Packaged in an 84-pin PGA or 84-pin MQFP.

SUPPORT

HARDWARE

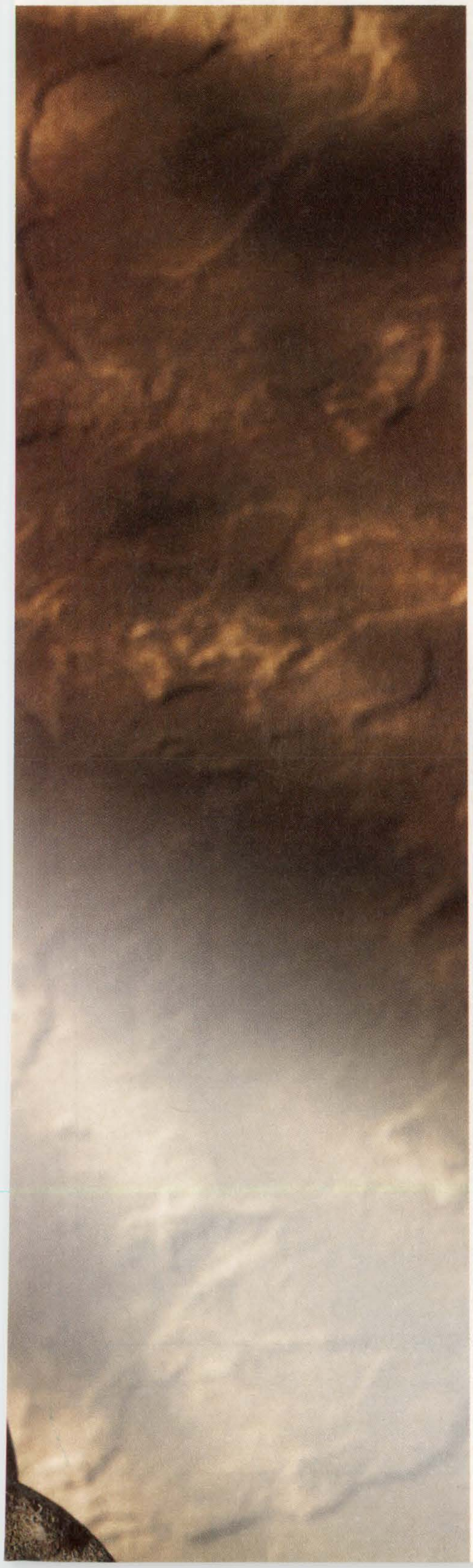
Hardware-development-system board.
VME bus-based product for development.
Third-party hardware available.

SOFTWARE

Assembler/linker/simulator (MS-DOS and VAX/VMS).
Application library (MS-DOS and VAX/VMS).
PSS ADA Compiler for VAX/VMS.

When systems demand extra
can shape a TMS320 to your

-special DSPs, we needs.



Choosing the right DSP for your application is vital to your marketplace success. Only TI has the customizable capability and broad TMS320 family to help you get what you need.

What you want is what you get
With our unique customizable digital signal processing (cDSP) capability, you can achieve the integration and product differentiation you want. You can choose system peripheral functions (A/D, D/A, serial ports, timers, phase comparators and oscillators), add interface logic and then integrate them all directly on proven TMS320 DSP chips. You can even change the mix of on-chip memory and peripherals. Yet device development cycles are shorter and costs are lower than with full-custom gate-level approaches.

Over the past five years, this innovative TI technology has created winning solutions for hundreds of high-volume market leaders.

Broad TMS320 family
Our more than 30 standard DSP solutions can meet the majority of your price/performance needs.

You can choose from our 16-bit fixed-point DSPs that start at $3 or from our 32-bit floating-point devices beginning at $25. There are family members delivering 50-MFLOPS performance, EPROM and OTP DSPs and those optimized for specific applications, plus military versions.

When you want super-processing power, our parallel-processing TMS320C40 DSP allows direct processor-to-processor communications to achieve the MOPS, MBPS, MIPS and MFLOPS your design requires.

World-class support
To speed you to market faster, you can talk with TMS320 specialists, attend hands-on workshops, read over 2,000 pages of applications notes and contact more than 100 third parties and consultants.

The development environment you will use is the same as that for general-purpose microprocessors whether you are working with a standard TMS320 or a cDSP. It includes high-level-language optimizing compilers, multitasking operating systems and realtime emulation.

To make your DSP match, call 1-800-336-5236, ext. 3538
You will receive information on our cDSP capability, the complete TMS320 family of devices and our world-class support. What's more, we'll send you "Designing with DSPs is Easy" – an interactive disk that gives you a personal look at TMS320 support and the TMS320 Programmer's Interface.

TEXAS INSTRUMENTS

CIRCLE NO. 75

08-12111

µPD77240

32-BIT FLOATING-POINT CMOS DSP µP

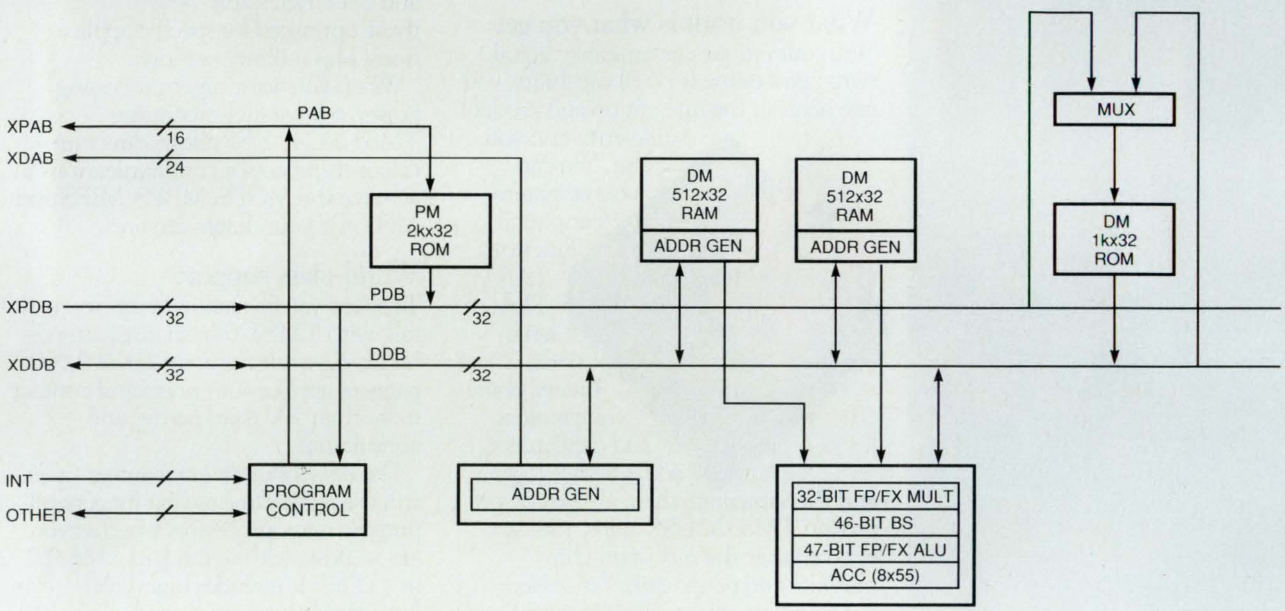
AVAILABILITY: The 132-pin PGA is available now. The PQFP will be available in 1992.

COST: $75 (1000).

SECOND SOURCE: None.

NEC Electronics
401 Ellis St
Mountain View, CA 94039
(800) 632-3531; (415) 965-6158
(800) 729-9288; (415) 965-6130
Circle No. 683

DESCRIPTION: The 77240 is a 32-bit CMOS floating-point DSP chip. The internal instruction and data ROM are preprogrammed with math matrix routines. It has two external buses: one for data addressing up to 16M×32 bits, and the other for instruction addressing up to 64k×32 bits. The vendor says the architecture suits adaptive filter applications.



FEATURES: 90-nsec cycle time.
Separate on-chip program and data buses.
On-chip memory: 2k×32-bit program ROM (preprogrammed), dual 512×32-bit data RAMs, and a 1k×32-bit data ROM (preprogrammed).
External memory expansion: 64k×32-bit program memory and 16M×32-bit data memory.
Separate external program and data buses.
The 77240 has no on-chip peripherals.
Proprietary 32-bit floating-point format.
Multiplier accepts 32-bit floating-point data and creates 55-bit floating-point results.
Multiplier accepts 24-bit fixed-point data and creates 47-bit fixed-point results.
47-bit ALU.
47-bit bidirectional barrel shifter.
Eight 55-bit register-based accumulators.
Direct, indirect, immediate, circular, and bit-reversal addressing modes.
Three address ALUs.
No on-chip DMA.
The stack is eight levels deep and is not expandable.
Two external interrupts.
No wait states.
No on-chip emulation port.
No low-power mode.
Packaging: 132-pin PGA.

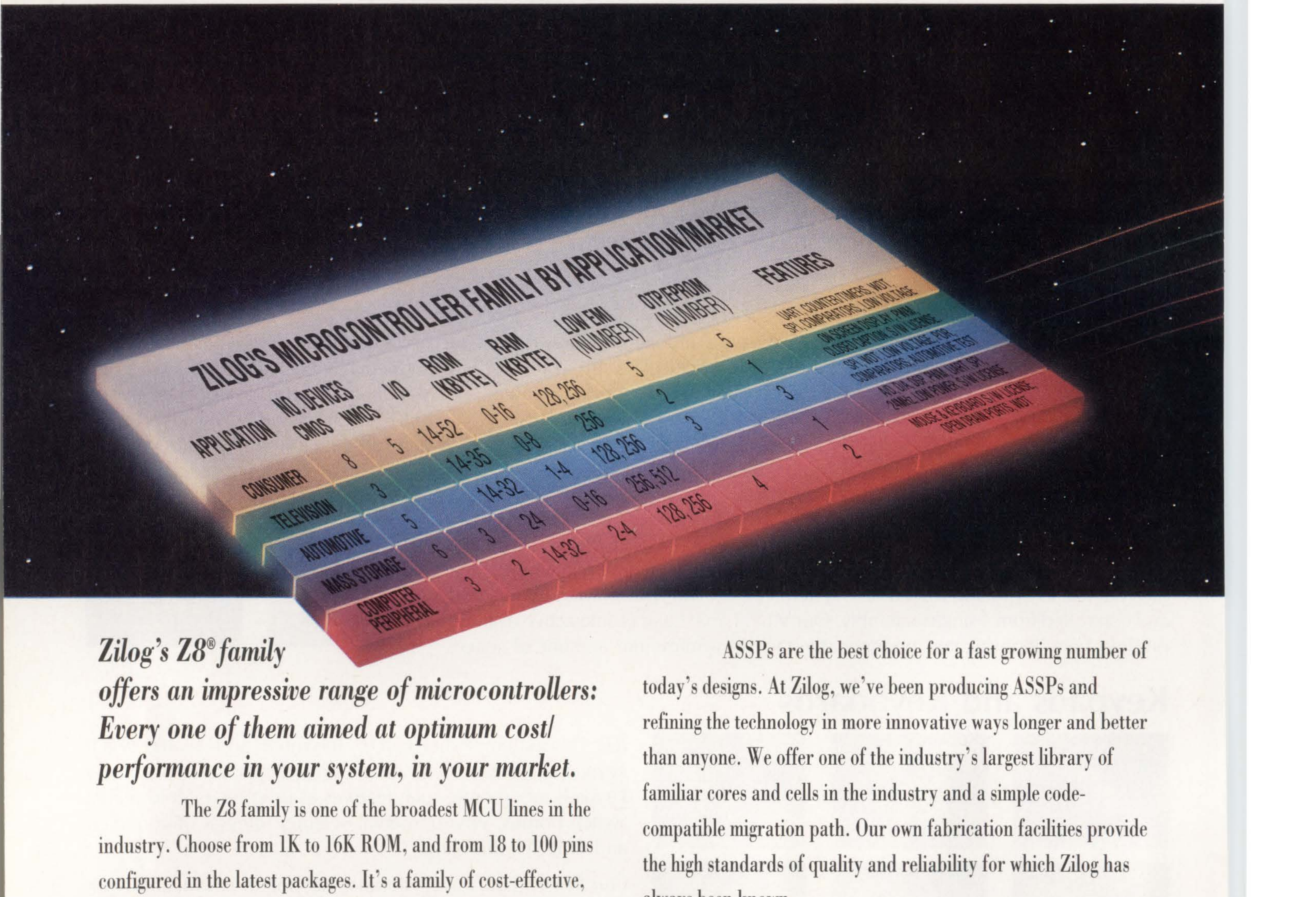
HARDWARE — SUPPORT — SOFTWARE

Hardware: Evaluation kit, which includes an in-circuit emulator.

Software: Assembler/linker and simulator.
C compiler.

Zilog Microcontrollers

More Choices. On Target.



Zilog's Z8® family offers an impressive range of microcontrollers: Every one of them aimed at optimum cost/performance in your system, in your market.

The Z8 family is one of the broadest MCU lines in the industry. Choose from 1K to 16K ROM, and from 18 to 100 pins configured in the latest packages. It's a family of cost-effective, high-performance 8- to 16-bit microcontrollers . . . precisely targeted for particular applications in specific markets, such as mass storage, auto, computer peripherals, speech processing, and general purpose embedded control.

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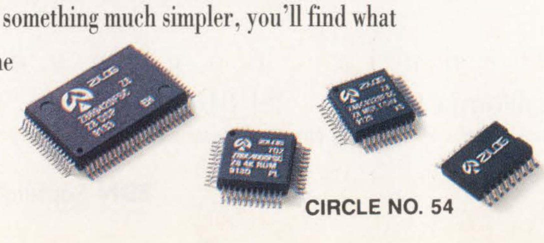

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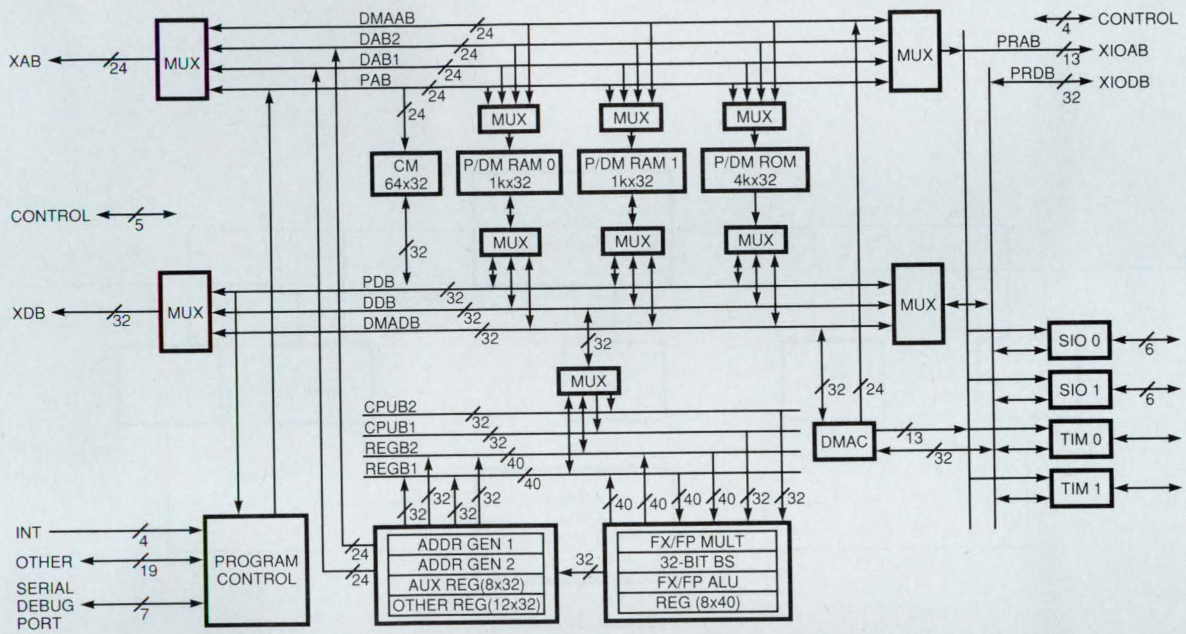
CIRCLE NO. 54

32-BIT FLOATING-POINT CMOS DSP μP

AVAILABILITY: The C30 (27, 33, and 40 MHz) and the C31 (27, 33, and 40 MHz) are available now.
COST: C30, $158; C30-27, $137; C30-40, $200; C31, $56; C31-27, $55; C31-40, $67 (1000).
SECOND SOURCE: None.

Texas Instruments Inc
Semiconductor Group
Box 809066
Dallas, TX 75380
(214) 995-6611, ext 3990
Circle No. 684

DESCRIPTION: This device was the first floating-point member of the vendor's TMS320 family. It is not code compatible with the fixed-point chips. The C30 is available in a slower, lower-cost version called the C30-27. The C31 is object-code compatible with the C30 and C30-27 but has only one serial port, one parallel port, and one timer. This feature reduction reduces the chip size and pin count, which lets TI offer a floating-point DSP for $35 in high volume.



FEATURES: 50-, 60-, and 74-nsec cycle-time versions.
Four 24-bit address buses and three 32-bit data buses.
Two 32-bit and two 40-bit additional buses in the CPU.
Separate program, data, and DMA buses.
Each internal RAM and ROM allows two accesses per cycle.
Any of the separate memories can be used for program or data.
Two on-chip 1k × 32-bit RAMs and an on-chip 4k × 32-bit ROM.
24-bit external memory-address bus provides 16M × 32-bit total address space.
13-bit external-I/O address bus provides 8k × 32-bit I/O ports, which are mapped into the 16-Mbyte address space.
Two 8-, 16-, 24-, and 32-bit serial I/O ports. Two 32-bit timers.
Proprietary 2's complement 32-bit floating-point format.
Multiplier accepts 32-bit floating-point data and returns 40-bit floating-point result. 24-bit integers result in 32-bit fixed-point results.
ALU operates on 40-bit floating-point and 32-bit fixed-point data.
Parallel multiplier and ALU operations in a single cycle.
32-bit bidirectional barrel shifter.
Eight 40-bit register-based accumulators.
Single-instruction and zero-overhead block looping.
64 × 32-bit instruction cache.
Cache can be disabled when not needed and frozen to keep an often used portion of code available in the cache.
Register, direct, indirect, immediate, relative, circular, and bit-reversed addressing modes. Two address ALUs.
DMA controller allows concurrent I/O and CPU operation.
Hardware pointer to software stack.
Four external vectored interrupts.
Hardware- and software-programmable wait states.
Serial debug port can provide in-circuit emulation.
Packaging: C30, 180-pin PGA. C30-27, 180-pin PGA. C31, 132-pin QFP.

HARDWARE — SUPPORT — SOFTWARE

Full-speed in-circuit emulator for IBM PC and Sun workstations.
Evaluation module plugs into an IBM PC.
Significant third-party support. Contact manufacturer for a list of third-party vendors. Hewlett-Packard has a version of the HP64700 in-circuit emulator for the C30.

Optimizing ANSI C compiler. Source-level debugger and code profiler. (PC or Sun).
Assembler/linker. Simulator. (PC or Sun).
Application library.
Third-party support includes real-time multitasking operating system (SPOX), Ada compiler, filter-design packages, and block-level diagramming language.

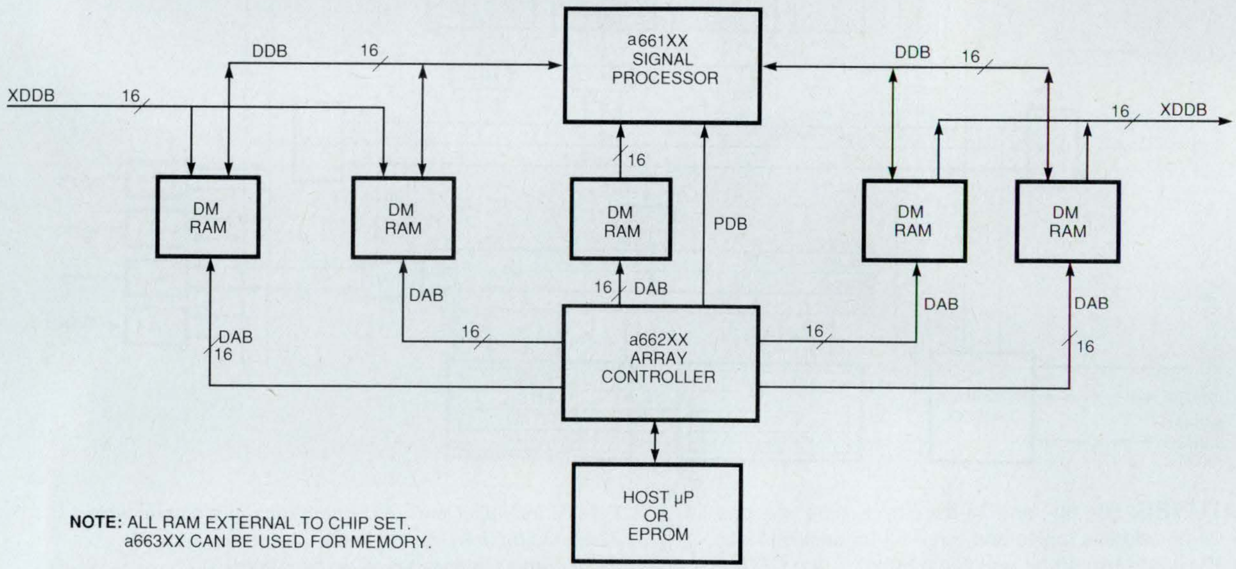
a66 FAMILY

16-bit FIXED-POINT DSP CHIP SET

AVAILABILITY: Now.
COST: a66111, 40-MHz, $700; a66211, 40-MHz, $680; a66311, 40-MHz, $520 (1).
SECOND SOURCE: None.

Array Microsystems Inc
1420 Quail Lake Loop
Colorado Springs, CO 80906
(719) 540-7999
FAX (719) 540-7950
Circle No. 686

DESCRIPTION: The a661XX combines arrays of adders, multipliers, and ALUs for high-performance DSP applications. The a662XX provides system control and five address generators for FFT applications. The a663XX is a reconfigurable memory array that can be used with the family to reduce chip count. A 1024-point complex FFT can be calculated in 131 μsec. DSP operations are controlled by high-level DSP instructions.



NOTE: ALL RAM EXTERNAL TO CHIP SET.
a663XX CAN BE USED FOR MEMORY.

FEATURES: 30- and 40-MHz versions.

Internal block floating-point maintained by a661XX.
16 high-level instructions execute FFT and general-purpose operations.
a662XX has 32-word instruction store for DSP programs.
Unlimited program size via external memory.
Directly supports up to 64k-point complex or 128k-point real data frames.
Simultaneously generates up to five 16-bit addresses to control memory array.
Program can be initialized by host μP or automatically booted from ROM.
a663XX contains 64k-bit of configurable static RAM.
One a66111, one a66211, and three a66311 chips create a complete 1024-point double-buffered FFT engine.
Multichip-module version being developed.
MIL-883 versions available.
Packaging: 144-pin PGA.

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HARDWARE

VME and pc boards available.

SOFTWARE

Software development environment includes code generator, assembler, and graphical interface.

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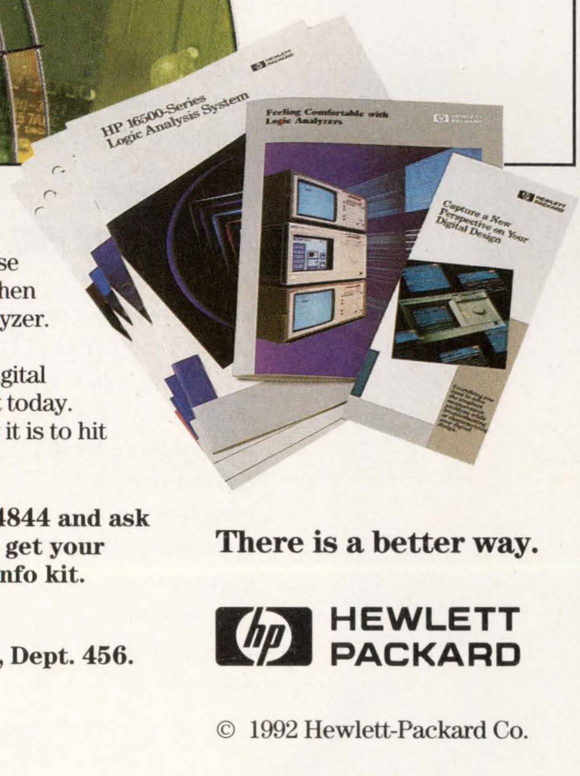

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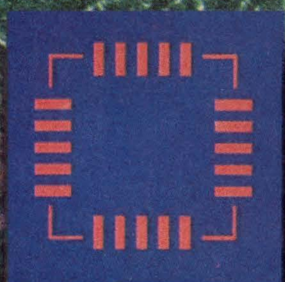

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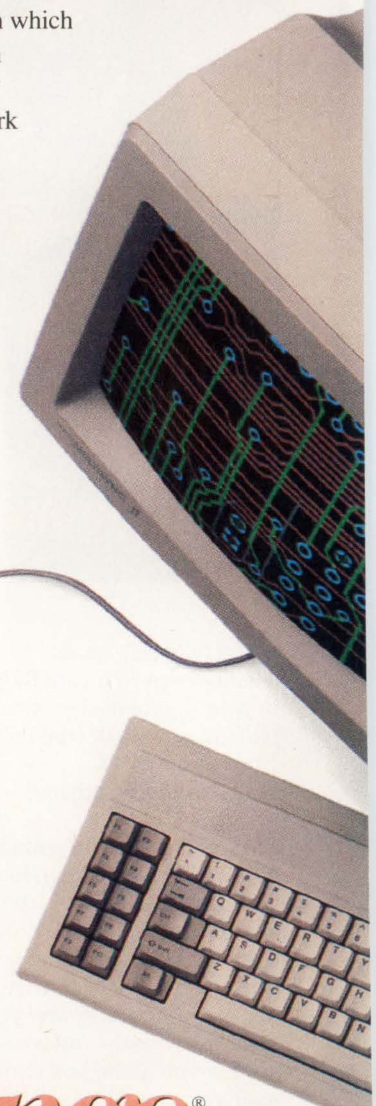
Tango-Route PRO has a unique "reconstruct" algorithm which iterates to 100% completion up to five times faster than comparable PC-based "rip-up and retry" or "push and shove" PC-based autorouters. Its automated options work like an "expert system" selecting the optimum routing configuration right out of the box for best results in the shortest time. Intelligent algorithms produce boards with fewer vias and shorter trace length to ensure high yields, lower fab cost and enhance board aesthetics. Uniform-, non-uniform- and off-grid routing offer performance equal to or better than "gridless routers." The program fully supports the 32-bit power of 386/486 computers, virtual memory and all current PCB technologies including advanced SMD. And you'll drive Tango-Route PRO with the easy-to-use, Windows™-like Tango interface.



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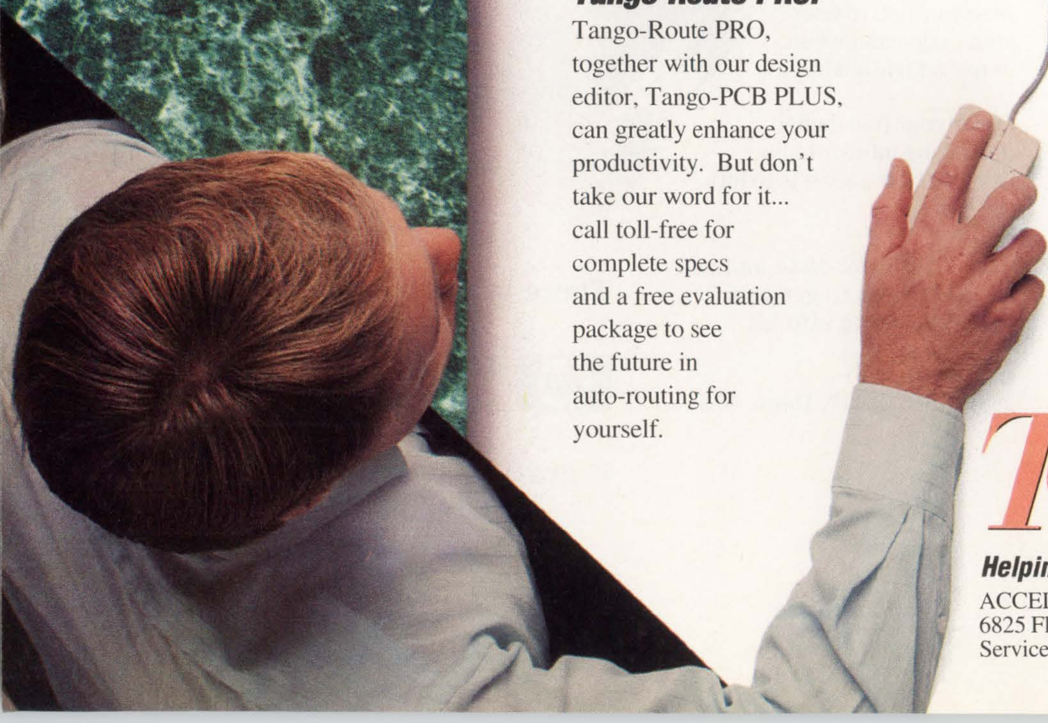

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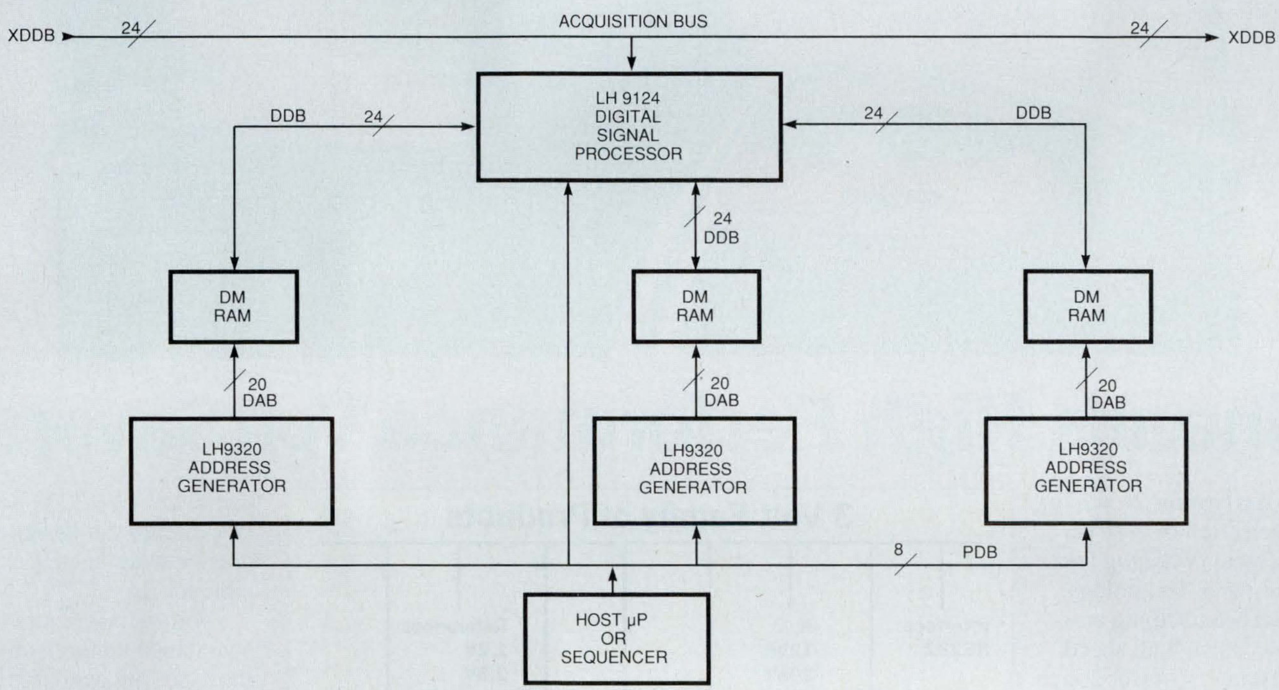
CIRCLE NO. 81

24-bit FIXED-POINT DSP CHIP SET

AVAILABILITY: Now.
COST: LH9124, $1200; LH9320, $260 (100).
SECOND SOURCE: None.

Sharp Electronics Corp
5700 NW Pacific Rim Blvd, Suite 20
Camas, WA 98607
(206) 834-2500
FAX (206) 834-8903
Circle No. 687

DESCRIPTION: The LH9124 is optimized for block-oriented algorithms and array processing. It is microcoded to perform standard DSP functions in time domain or frequency domain. The LH9320 is an address generator with many patterns to support DSP algorithms. High-level DSP commands simplify software generation. A 1024-point complex FFT can be performed in 81 μsec.



FEATURES: 33- and 40-MHz versions.
LH9124 maintains internal block floating-point.
26 high-level instructions execute FFT and general-purpose operations.
Multiple units can be paralleled or cascaded for higher performance.
Data width can be 8- to 24-bit real or complex.
No on-chip memory.
Packaging: LH9124, 262-pin PGA; LH9320, 68-pin PLCC.

SUPPORT

HARDWARE

System-validation card for each chip.
Evaluation module.

SOFTWARE

PC-based real-time simulator.
Object-oriented high-level-language development system.

CMOS switches develop negative voltage

Ľubomír Gálfy, Ústav Automatizácie a Komunikácie, Severná, Československo

The simple negative-voltage converter in **Fig 1** works over an input range of 3 to 9V with an internal resistance ranging from 2000 to 400Ω (depending on input voltage and output loading). The converter's negative output is nearly equal in magnitude to the input voltage.

Resistor R_1, capacitor C_1, and switches IC_{1A} and IC_{1B}, functioning as inverters, form an RC oscillator. Switches IC_{1B} and IC_{1C} alternately charge C_2 from V_{IN} and discharge C_2 into C_3.

If you use a 74HC4053 instead of a CD4053, the circuit will have a lower internal resistance, but function only over a V_{IN} range of 2 to 5V. If the negative output is greater in magnitude than the input, the circuit can feed energy back from output to input.

EDN BBS /DI_SIG #1184 EDN

To Vote For This Design, Circle No. 748

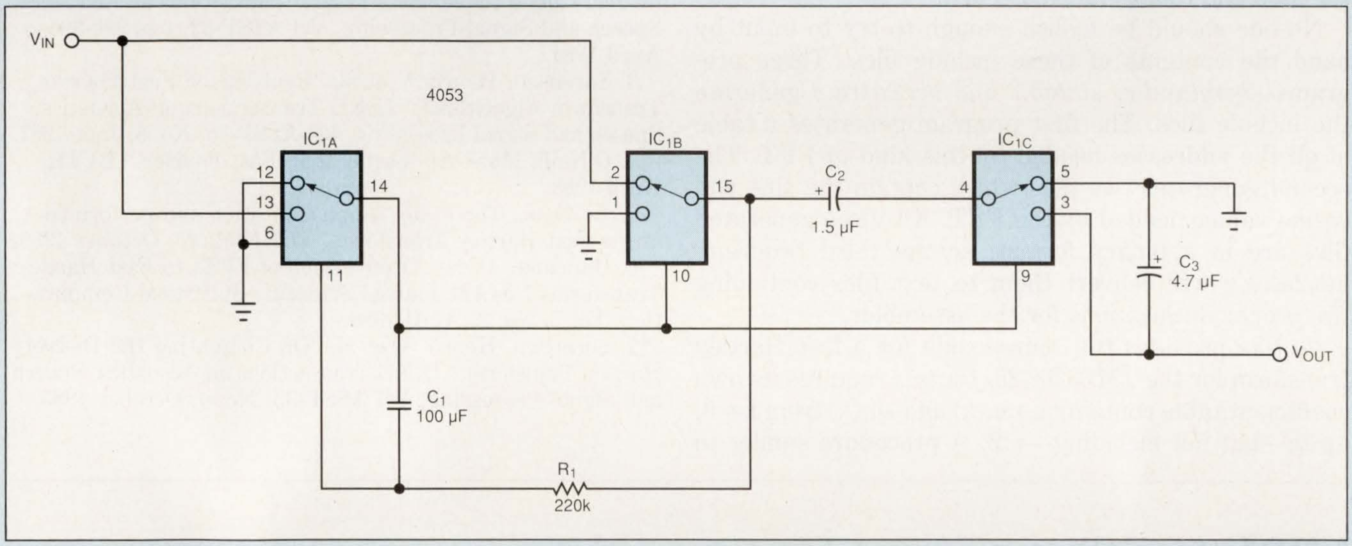


Fig 1—Cleverly using analog switches as inverters in an RC oscillator, this circuit will produce a negative output nearly equal in magnitude to its supply voltage.

Hartley transform beats FFT for DSP µPs

Vladimir Bochev, Université De Nancy, Nancy, France

Bergland's well-known algorithm for the FFT (**Ref 1**) has drawbacks in light of modern DSP µPs. His algorithm decreases the memory requirements and the number of operations of a bit-reverse FFT by a half. But Bergland's FFT has a much more complicated addressing scheme compared with the simple bit-reverse for the complex FFT.

The Hartley transform is a real transform for a real signal. Furthermore, the inverse-transform algorithm is exactly the same as the forward transform. The overspeculated fast Hartley transform (**Refs 4** and **5**) better suits DSP µPs such as the TMS320C25. The fast Hartley transform is not faster than real valued FFTs and requires the same storage. It requires even a few more operations (**Refs 6** and **7**) to obtain a meaningful frequency spectrum. But the fast Hartley transform *is* faster than complex FFTs and requires less storage.

Its real-valued nature and the low memory requirements along with easy address generation makes the fast Hartley transform the algorithm of choice for frequency analysis of real-time signals on DSP microprocessors.

The listings are much too long to be printed here. But you can find source code and examples that you can run of both the Bergland FFT and Hartley transforms, along with some handy utilities, posted on the EDN BBS. After obtaining the files, you can call the program *fft_real*, written in 80x86 assembly language, directly from a C program running on your PC. *fft_real* is very easy to understand—especially the section on the butterfly computations. To simplify generating addresses for the data and coefficient array, all addresses are precomputed and stored in an include file, as are the sine and cosine values needed.

No one should be foolish enough to try to input by hand the contents of these include files. Three programs—*bergland.c*, *sintab.c* and *hex2asca.c* generate the include files. The first program generates a table of all the addresses needed by this kind of FFT. The second generates two files which contain the sine and cosine values needed by the FFT. All three generated files are in a binary format, so the third program, hex2asca.c will convert them to text files containing the proper declarations for the assembler.

fht.tms provides the source code for a fast Hartley transform for the TMS320C25. *fht.tms* requires its own coefficient table containing tan(x) and sin(x) from x = 0, up to—but not including—π/2. A procedure similar to *sintab* for the Bergland FFT will generate the table in for the fast Hartley transform. To make an include file you'll need to slightly modify *hex2asca.c* to emit, for example, DATA statements instead of "dw", and also the proper "hex" header and not suffix "h".
EDN BBS /DI_SIG #1183

To Vote For This Design, Circle No. 749

References

1. Bergland, Glen D, "A Fast Fourier Transform Algorithm for Real Valued Series," Communications of the ACM, Vol 11, No. 10, Oct 1968.
2. Martens, J B, "Discrete Fourier Transform Algorithms for real valued sequences," IEEE Transactions on Acoustics, Speech and Signal Processing, Vol ASSP-32, pgs 390-396, April 1984.
3. Sorensen, Henrik V et al, "Real-Valued Fast Fourier Transform Algorithms," IEEE Transactions on Acoustics, Speech and Signal Processing, Vol ASSP-35, No. 6, June 1987.
4. O'Neill, Mark A, "Faster than Fast Fourier," BYTE, April 1988.
5. Le Ngoc, Tho et al, "Implementation and performance of the Fast Hartley Transform," IEEE Micro, October 1989.
6. Buneman, Oscar, "Conversion of FFTs to Fast Hartley Transforms," SIAM Journal Scientific Statistical Computation, Vol 7, No. 2, April 1986.
7. Sorensen, Henrik V et al, "On Computing the Discrete Hartley Transform," IEEE Transactions on Acoustics, Speech and Signal Processing, Vol ASSP-33, No. 4, October 1985.

VHDL "wait" statement inserts registers

Steve Carlson, Synopsys Inc, Mountain View, CA

The circuit in **Fig 1** illustrates how a logic synthesizer interprets the VHDL (VHSIC hardware-description-language) *wait* statement (**Listing 1**). In the **Listing**, the *wait* keyword tells the logic synthesizer to store certain logic values. The synthesizer then inserts registers where required. **EDN BBS /DI_SIG #1181**

To Vote For This Design, Circle No. 750

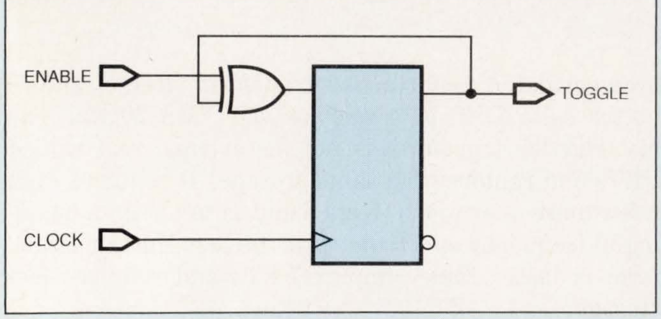
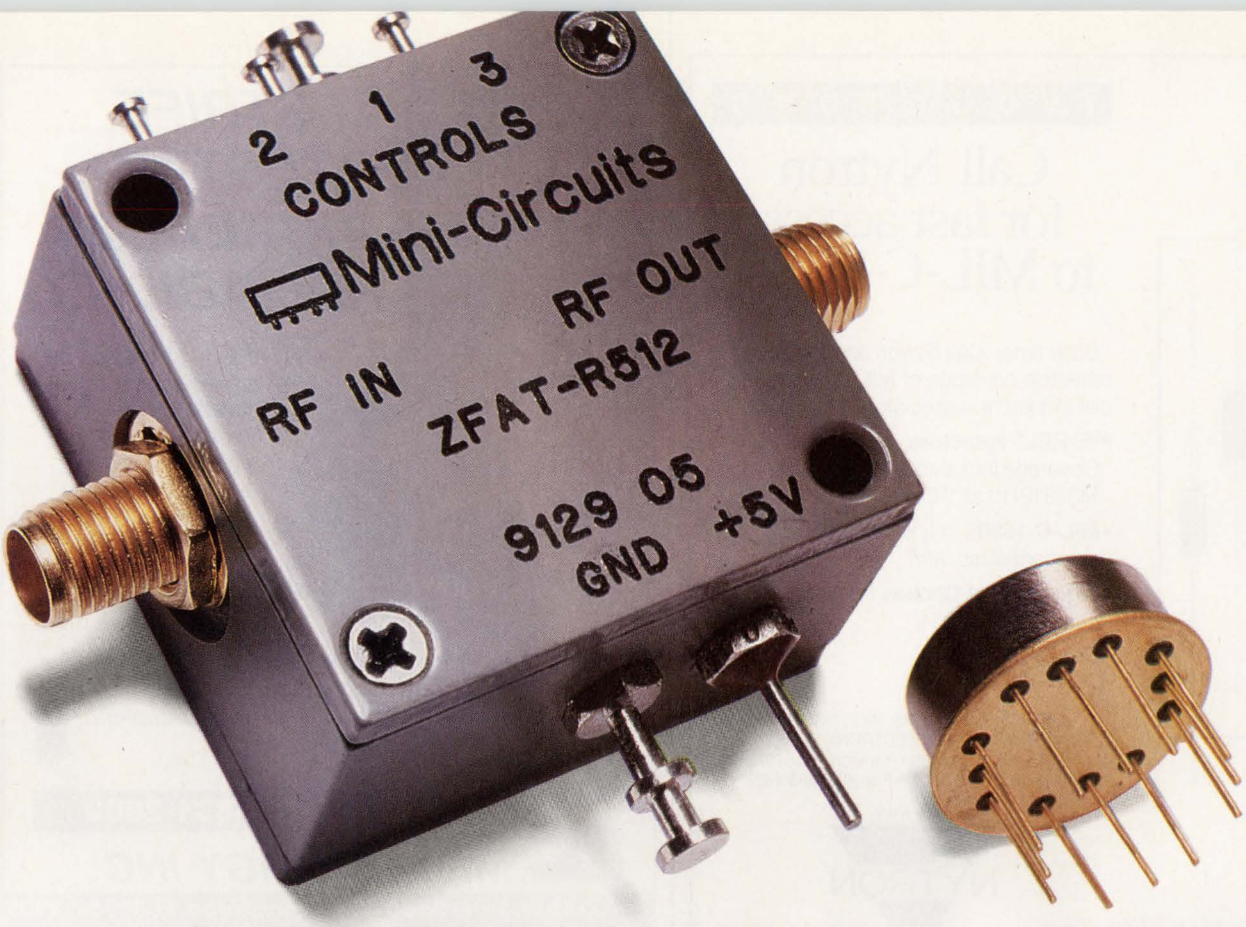


Fig 1—A logic synthesizer will generate a register like this one in response to a VHDL wait statement in the listing.

Listing 1—VHDL wait example

```
entity VHDL is
    port(
      ENABLE : in  BIT;
      CLOCK  : in  BIT;
      TOGGLE : buffer BIT
    );
end VHDL;

architecture VHDL_1 of VHDL is
begin
  process begin
    wait until not CLOCK'stable and CLOCK = '1';
    if (ENABLE = '1') then
      TOGGLE <= not TOGGLE;
    end if;
  end process;
end VHDL_1;
```



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1.0	**0.2**	**2.0**	**0.2**	**6.0**	**0.3**	**8.0**	**0.3**	**10.0**	**0.3**
1.5	0.32	3.0	0.4	9.0	0.6	12.0	0.6	15.0	0.6
2.0	**0.2**	**4.0**	**0.3**	**10.0**	**0.3**	**16.0**	**0.5**	**20.0**	**0.4**
2.5	0.32	5.0	0.5	13.0	0.6	20.0	0.8	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	24.0	0.8	30.0	0.7
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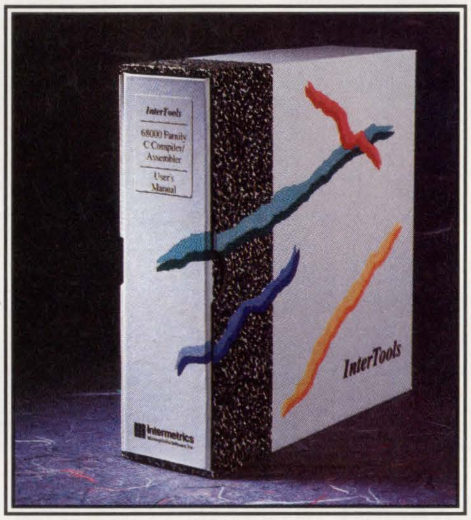

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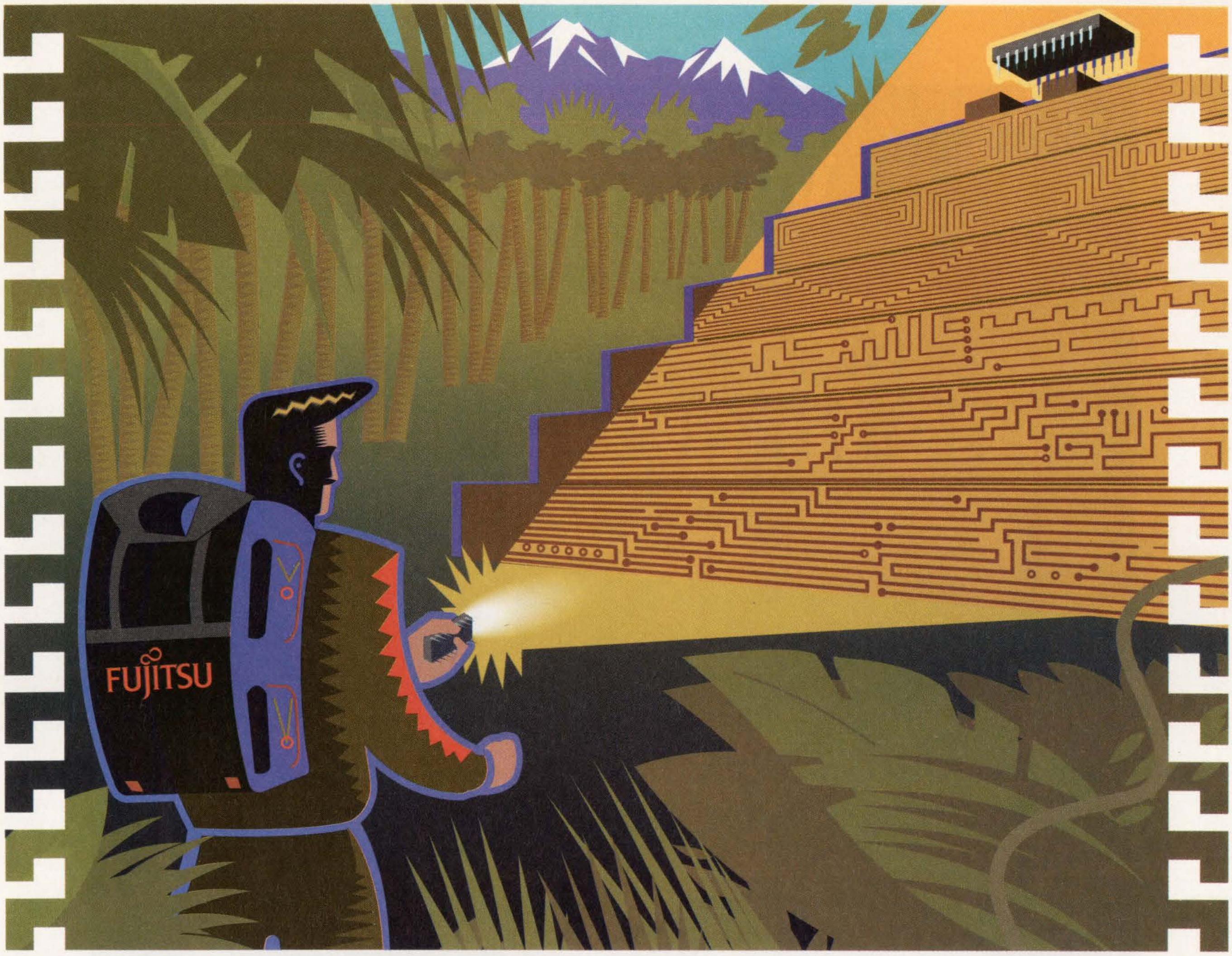
CIRCLE NO. 89



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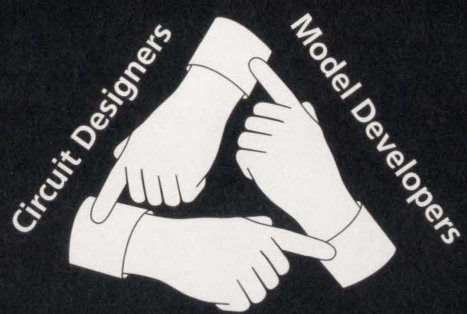
FUJITSU MIKROELEKTRONIK GmbH (Dreieich-Buschlag, Germany) Ph: 06103-6900 Fax: 06103-690122.

CIRCLE NO. 90

When the chips are down, the finger pointing starts.



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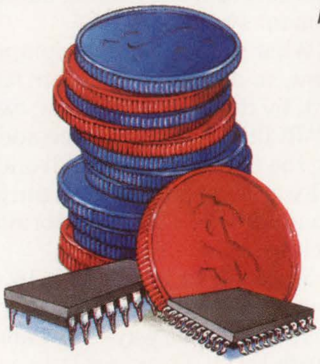

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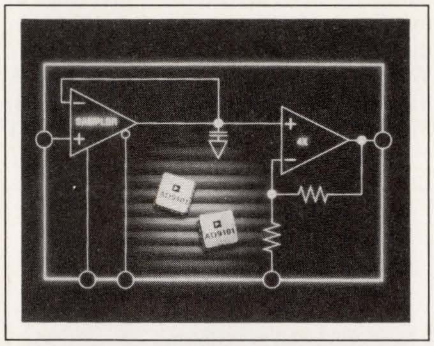
CIRCLE NO. 91

SPARC peripheral chip set. The SPARCset 7-chip chip set lets you build Mbus modules ranging from a single processor, 33-MHz CYM6001 SPARC-set module to a dual-processor 66.7-MHz CYM6226 hyperSPARC module. The CY7C617 is a graphics controller that interfaces directly to the Mbus. The CY7C616 and CY7C618 provide an Mbus to SBus interface. The CY7C613 is a memory controller, and the CY7C604/5 is a cache controller/memory-management unit. The CY7C614 and CY7C615 are I/O controllers. Chip set, $250 (100). **Cypress Semiconductor,** 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600.

Circle No. 365

QPSK modulator. The HPMX-2002 is a monolithic quadrature-phase-shift-keyed (QPSK) modulator and dual-conversion unit. It modulates signals in the 40- to 300-MHz frequency range and transmits RF data at frequencies as high as 2 GHz. The I and Q bandwidths are greater than 10 MHz, and the output power is −11 dBm. The 20-pin plastic chip consumes 60 mW when operating from 5V and 50 μW in standby mode. $8.75. **Hewlett-Packard Co,** Box 58059, Santa Clara, CA 95052. Phone (800) 752-0900. **Circle No. 366**



Sampling amplifier. The AD901 Sampling amplifier consists of a track and hold amplifier driving a positive gain op amp with a gain of 4 in a 20-pin SOIC or ceramic LCC package. Acquisition time to 0.4% of amplitude is 5 nsec, and 0.01% of amplitude is 11 nsec. The rms noise when the amplifier is tracking the input is 3.3 nV/$\sqrt{\text{Hz}}$. The harmonic distortion during hold mode is −75 dB below full scale for a 50M-sample/sec sampling rate and a 23-MHz input sine wave. $33 (100). **Analog Devices Inc,** Computer Labs Div, 7910 Triad Center Dr, Greensboro, NC 27409. Phone (919) 668-9511. FAX (617) 821-4273. **Circle No. 367**

Windows accelerator. The HT216-32 Windows Express is a local-bus VGA controller. It accelerates Windows applications for 486 and 386 μPs. The controller is register compatible with the IBM VGA standard and operates at CPU clock speeds from 16 to 40 MHz. Hardware in the controller assists the CPU in controlling Windows operations. $25 (1000). **Headland Technology,** 46221 Landing Pkwy, Fremont, CA 94538. Phone (510) 623-7857.

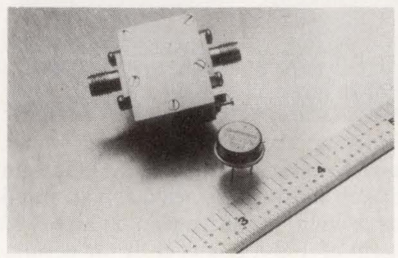
Circle No. 368

FIFO memories. The QS7201 and QS7202 asynchronous FIFO memories have 12-nsec access times and 512k × 9-bit and 1k × 9-bit densities, respectively. The asynchronous QS7203 and QS7204 FIFO memories have 10-nsec access times and 2k × 9-bit and 4k × 9-bit densities, respectively. The syn-

chronous QS7223 and QS7224 FIFO memories operate with 66-MHz clocks and have 2k × 9-bit and 4k × 9-bit densities, respectively. $30.15 to $98.50. **Quality Semiconductor,** 851 Martin Ave, Santa Clara, CA 95050. Phone (408) 450-8000. FAX (408) 496-0591.
Circle No. 369

Board-history recorder. The Scope Diary TMS29F816 JTAG-compatible chip maintains the operational history of a PC board. It stores serial and model numbers, calibration constants, engineering revisions, elapsed operation time, repair history, and power-down status log. In addition, the chip has one-time write protection, 16 kbits of memory, and nonvolatile storage. $15 (1000). **Texas Instruments Inc,** Semiconductor Group, Box 809066, Dallas, TX 75380. Phone (214) 995-6611, ext 3990.
Circle No. 370

GaAs products. This family of prescalers and gain-block amplifiers are the company's first commercial GaAs products. The divide-by-4, -8, and -32 prescalers operate from a −5.2 to −6V supply and from dc to 14 GHz. The gain-block amplifiers provide 10 or 20 dB of gain from dc to 10 GHz. The amplifiers operate from a 4 to 7V supply and consume 200 mW. Divide-by-8 prescaler in die form, $14.95; 10-GHz gain block in die form, $9.95. **Rockwell/MTC,** 2427 W Hillcrest Dr, Newbury Park, CA 91320. Phone (805) 375-1237. FAX (805) 375-1268. **Circle No. 371**



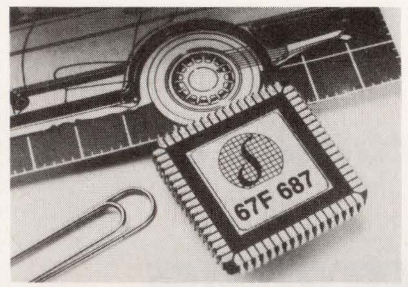
10- to 1500-MHz amplifier. The UTO-1576 RF amplifier provides 10.5 dB of gain from 10 to 1500 MHz. It comes in a T0-8 package and exhibits 50 dB of reverse isolation. Other features include 0.5-dB gain flatness, 5-dB noise figure, and a 1-dB gain compression point of 9 dBm. The amplifier operates from −55 to +85°C. $120. **Hewlett-Packard Co,** Box 58059, Santa Clara, CA 95052. Phone (800) 752-0900.
Circle No. 372

4M-bit video RAM. This video RAM includes reading and writing of bits to split registers, 4 × 4 × 4 block writes for fast area-fills, and CAS-before-RAS refresh. The chip integrates a 256k × 16-bit dynamic RAM with a 256-bit serial-access memory. One version has a 70-nsec row-enable access time and a 20-nsec serial-data access time. Another version has an 80-nsec row-enable access time and a 25-nsec serial-data access time. From $70. **Texas Instruments Inc,** Semiconductor Group, Box 809066. Dallas, TX 75380. Phone in US and Canada, (800) 336-5236, ext 3990; (214) 995-6611, ext 3990. **Circle No. 373**

3V 22V10 PLDs. The AT22LV10 and AT22LV10L are 3V versions of the industry-standard 22V10 PLD. Both chips operate from 3 to 5.5V. Propagation delay for both devices is 20 nsec. The AT22V10 draws 40 mA of standby current, and the AT22V10L draws 4 mA from a 3.6V supply. Packaged in plastic DIPs, AT22LV10, $8.40; AT22LV10L, $6.60 (100). **Atmel Corp,** 2125 O'Nel Dr, San Jose, CA 95131. Phone (408) 441-0311. **Circle No. 374**

386DX ISA bus controller. The VL82C380 is an ISA bus controller chip with on-chip cache. Its cache controller employs a look-aside, write-back architecture. The chip controls 1- or 2-bank cache RAMs and maintains coherency during DMA and master-mode cycles to eliminate flushing and invalidating operations. The memory controller can access as much as 64 Mbytes of main memory. Approximately $20 (OEM qty). **VLSI Technology Inc,** SC386, 200 Parkside Dr, San Fernando, CA 91340. Phone (602) 752-6212. FAX (602) 752-6000. **Circle No. 375**

Quad video buffers. The Si584 monolithic quad video buffers have a 200-MHz bandwidth and an output drive-current capacity of ±20 mA. The unity-gain buffers don't require any external components, and the differential gain and phase errors are 0.8% and 0.1°, respectively. The chip comes in a 14-pin DIP or SO-14 package. $10.15 (1000). **Siliconix Inc,** 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (800) 554-4454, ext 1900; (408) 988-8000. **Circle No. 376**

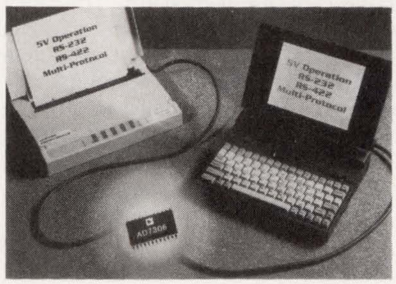


Combustion-engine peripheral. The 67F687 controls the spark and fuel control systems in 4-, 6-, or 8-cylinder engines. Because the chip generates fewer interupts than other engine peripheral ICs, you can use simple, inexpensive μPs. On-chip features include sensor conditioning and output predrivers. A digital phase-locked-loop circuit tracks engine position using two sensor inputs. $3.50 to $15. **Silicon Systems,** 14351 Myford Rd, Tustin, CA 92680. Phone (714) 573-6200. FAX (714) 573-6914. **Circle No. 377**

Audio chip sets. The Aria family consists of three chip sets for synthesizing music on a computer. The ST8000 emulates Creative Lab's Sound Blaster board and has a joystick port, a MIDI port, a Rowland MPU-401 port, and digital recording and playback. The ST8001 and ST8002 offer the same features and have a 512-kbyte and 1-Mbyte sound library, respectively. $30 to $60 (10,000). **Sierra Semiconductor,** 2075 N Capitol Ave, San Jose, CA 95132. Phone (408) 263-9300. FAX (408) 263-3337. TLX 384467. **Circle No. 378**

Power op amps. The single OMA541 and dual OMA2541 power operational amplifiers operate from ±40V power supplies and deliver 5A of continuous output current. The OMA501 delivers ±10A and is stable in a unity-gain configuration. OM501AK, $76.90; OMA2541SK, $106.70 (100). **Omnirel Corp,** 205 Crawford St, Leominster, MA 01453. Phone (508) 534-5776. FAX (508) 537-4246. **Circle No. 379**

Single-supply communications transceivers. The AD7306 combines two RS-232C and an RS-422 driver with an RS-232C and configurable RS-232C or RS-422 receiver in a 24-pin SOIC package. The chip operates from a single 5V supply and internally generates ±10V for the transceivers. A charge-pump voltage converter operates with an external nonpolarized 0.1-μF capacitor. **Analog Devices Inc,** 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428. FAX (617) 821-4273. **Circle No. 380**



Real-time clock. The DS1587 serialized real-time clock is a timekeeper that can switch on a DOS-compatible computer to perform a scheduled task. It has a permanent 64-bit serial number to identify the computer. Besides the standard real-time clock registers and 50 bytes of user nonvolatile static RAM, the chip provides an additional 60 bytes of nonvolatile staticRAM. $15.50 **Dallas Semiconductor,** 4401 S Beltwood Pkwy, Dallas, TX 75244. Phone (214) 450-0448. FAX (214) 450-0470. **Circle No. 381**

ISDN buck regulator. The PWR-SMP402 dc/dc converter for nonisolated ISDN (Integrated Services Digital Network) power-supply applications. The device accepts 20 to 72V dc inputs and generates a 5V supply line using a buck regulator. The IC meets ISDN specifications for T1 telecommunications requiring output power greater than 1W. A MOSFET power switch operates from 50 to 500 kHz. $2.30 (1000). **Power Integrations Inc,** 411 Clyde Ave, Mountain View, CA 94043. Phone (415) 960-3572. **Circle No. 382**

Wireless communications chips. The PMB2200 transmit modulator and PMB2400 receive demodulator comply with the Cellular Telecommunication Industry Association-endorsed IS-54 standard and the Groupe Speciale Mobile standard for digital wireless communications systems. The PMB2200 converts baseband signals to RF carrier frequencies between 700 MHz and 1 GHz. The PMB2400 converts the RF carrier to baseband signals, using dual-stage heterodyne receivers. $7.85 each (1000). **Siemans Components Inc,** Integrated Circuit Div, 2192 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 980-4500. **Circle No. 383**

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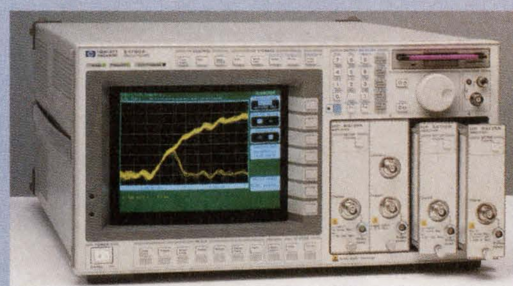

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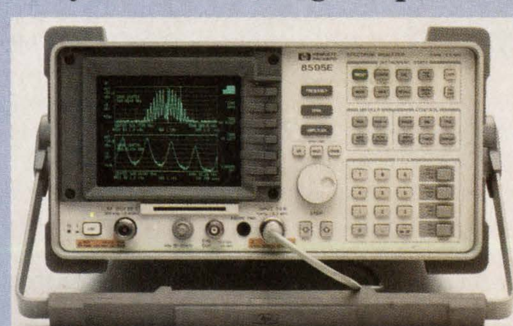

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CIRCLE NO. 95

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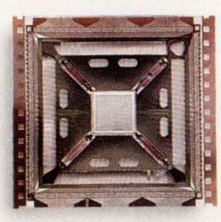

Whether you're designing your next gate array, or your first, you've got to think about system power requirements. Your very next thought should be: **Mitsubishi Gate Arrays.**

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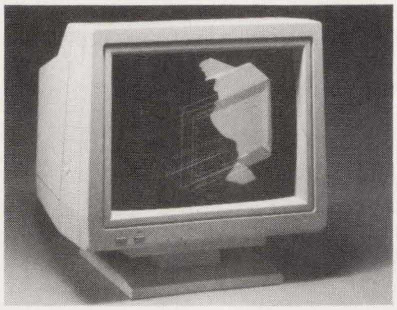
MITSUBISHI
ELECTRONIC DEVICE GROUP
CIRCLE NO. 96

Computers & Peripherals

IDE module. The Portfolio is a 13-port multifunction IDE (integrated-drive-electronics) interface module for serial, parallel, floppy, and game-port functions. Using this unit you can connect a laser printer, a dot-matrix printer, as many as four 1.2- or 1.44-Mbyte floppy-disk drives, two IDE drives, a tape-back-up unit, a serial mouse, a modem, and a joystick. $79. **Quadtrek Corp,** 6034 W Courtyard Dr, Suite 305-74, Austin, TX 78730. Phone (512) 338-2125. FAX (512) 338-2127. **Circle No. 384**

Multiprocessor application accelerators. The Skybolt-mp Shamrock offers processing speeds as high as 1.28 Gflops in a 9U VME slot, and the Skybolt Shamrock offers processing speeds as high as 320 Mflops in a 6U VME slot. The accelerators feature a modular design with an Intel i960 processor controlling several Intel i860 processors. The 6U Skybolt Shamrock, from $27,450; 9U Skybolt-mp Shamrock, from $32,350. **Sky Computers Inc,** 27 Industrial Ave, Chelmsford, MA 01824. Phone (508) 250-1920. FAX (508) 250-0036. **Circle No. 385**



Multifrequency monitor. The Spectrum Autosync monitor has a 20-in. dark tube and is compatible with PGA, VGA, extended VGA, 1024×768-pixel and 1280×1024-pixel formats. The monitor automatically adjusts picture size from horizontal frequencies of 29 to 66 kHz and vertical frequencies of 40 to 120 Hz. $3195. **Aydin Controls,** 414 Commerce Dr, Fort Washington, PA 19034. Phone (215) 542-7800. **Circle No. 386**

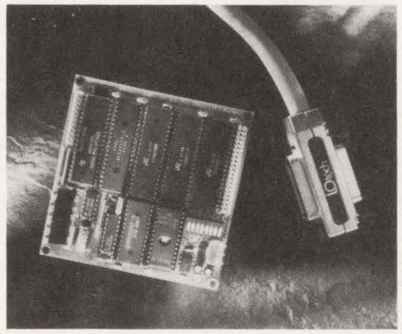
Super-VGA board. The VGAwonder XL24 displays 16.7 million colors in 640×480-pixel resolution or more than 32,000 colors in 800×600-pixel resolution. The board is available in 512 kbytes or 1 Mbyte and comes with drivers for Microstation, CADKey, OS/2 2.0, and Windows 3.X. $179. **ATI Technologies Inc,** 3761 Victoria Park Ave, Scarborough, ON M1W 3S2, Canada. Phone (416) 756-0718. FAX (416) 756-0720. TLX 06966640. **Circle No. 387**

Super-VGA graphics card. The SVGA Multiview/Micro Channel graphics card provides a 115-Hz refresh rate on the Micro Channel bus. The card and its software utilize Windows in 1024×768-pixel and 800×600-pixel resolutions and more than 16.7 million colors. $549. **Radius Inc,** 1710 Fortune Dr, San Jose, CA 95131. Phone (408) 434-1010. FAX (408) 434-0770. **Circle No. 388**

Solid-state power controllers. The SSP-21120 series solid-state power controllers operate as high as 80A at 28V dc. The controllers include a thermal memory that shortens trip times when repeated attempts are made to turn on the device into an overload condition. Using several devices in parallel yields higher current ratings. From $1295. Delivery, 60 to 90 days. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600, ext 7381. FAX (516) 567-7358. **Circle No. 389**

Minicartridge tape products. The three drives in the Tape250 series are QIC-80 tape drives that are able to read Irwin-formatted tapes and are based on the floppy-disk interface. The drives come with Central Point Backup software for DOS and Windows and data-compression software that allows the drives to store as much as 250 Mbytes. Insider, $299; Insider Half-Height, $349. Both drives fit into a standard 3½-in. bay. PC Powered drive, an external device, $499. **IOmega,** 1821 W 4000 S, Roy, UT 84067. Phone (800) 456-5522. FAX (801) 778-3450. **Circle No. 390**

32-I/O line interface board. The Digital 488/32/OEM 4×4-in. 32-I/O line interface board enables data transfers between the IEEE-488 bus and devices



equipped with 8-, 16-, or 32-bit-wide digital ports. The 32 TTL-level lines are programmable in 8-bit groups as either inputs or outputs. $495. **IOtech,** 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. FAX (216) 439-4093. **Circle No. 391**

Memory cards. For pen-based and palmtop systems, the SmartRAM memory-card family combines flash and static-RAM (SRAM) memory and includes a built-in controller and battery backup circuitry. The PCMCIA-standard cards have average read-access and write-cycle times of 150 nsec each. The cards, which weigh 35g, allow data-write cycles at 5V and incorporate 256 kbytes of SRAM and 768 kbytes of flash memory for a total of 1 Mbyte. $160 (100). **Smart Modular Technologies,** 45531 Northport Loop W, Bldg 3B, Fremont, CA 94538. Phone (510) 623-1231. FAX (510) 623-1434. **Circle No. 392**

Ruggedized VMEbus module. The CPUC32 is a cost-reduced version of a militarized single-board computer for the VMEbus. The board is based on the 68030 processor and has as much as 4 Mbytes of battery-backed static RAM. Operating systems include OS-9 and VxWorks. $5000. **Alphi Technology Corp,** 6202 S Maple Ave #128, Tempe, AZ 85283. Phone (602) 838-2428. FAX (602) 838-4477. **Circle No. 393**

Memory-card drives. These open-frame memory-card drives are compatible with JEIDA 4.0 and PCMCIA memory cards. The drives accept 512-kbyte to yet-to-be-released 64-Mbyte memory cards. Both drives are the

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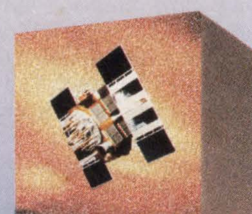


CIRCLE NO. 99

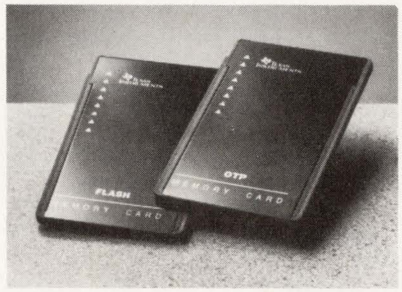
same size as a standard 3.5-in. floppy-disk drive. The MCRW-B has an RS-232C port; the SCSI version is the MCdisk-1. $495. **Gespac Inc,** 50 W Hoover Ave, Mesa, AZ 85210. Phone (602) 962-5559. FAX (602) 962-5750. **Circle No. 394**

HC11 CPU module. The 68HC11 includes a 68HC811E2FN 8-bit microcontroller, 2-Mbyte flash EPROM, 32-kbyte nonvolatile RAM, 2-kbyte EEPROM, 8-channel 8-bit A/D converter, a real-time clock calendar, RS-232C and RS-485 ports, 16-bit timer, open-architecture 64/96 DIN expansion bus, and C and assembler routines. The module comes with 24-hour BBS support. $287. **Ackerman Computer Sciences,** 4276 Lago Way, Sarasota, FL 34241. Phone (813) 377-5775. **Circle No. 395**

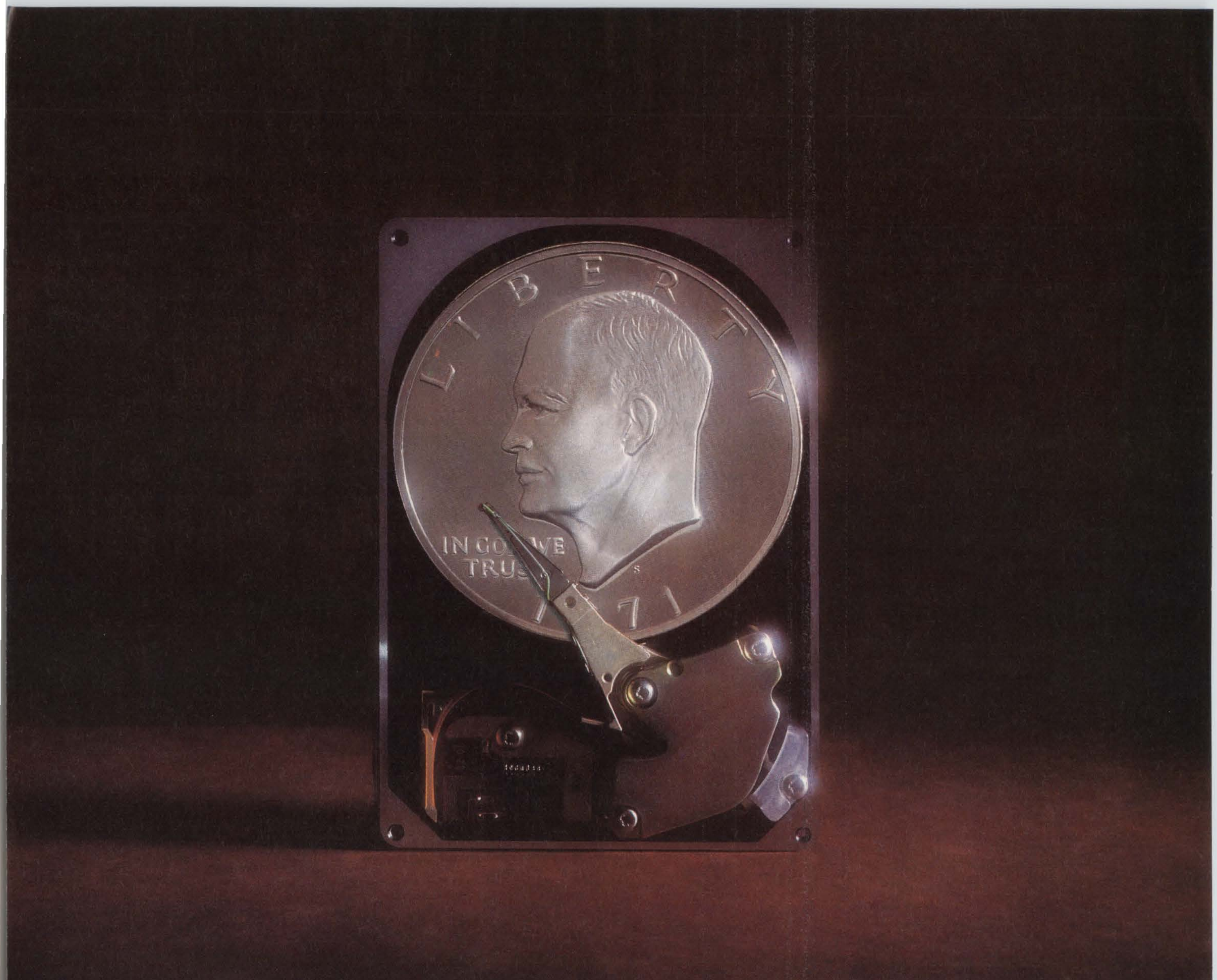
I/O-module interface cards. The PSR00 and MSR01 Power I/O Module interface cards are compatible with Opto22, Gordos, Burr-Brown, and Potter and Brumfield. The PSR00 is for ISA- or EISA-style computers, and the MSR01 is for Wintek 6800- and 6809-based computer systems. As many as 24 I/O channels may be used as inputs or outputs in any combination. PSR00, $159; MSR01, $125. **Wintek Corp,** 1801 South St, Lafayette, IN 47904. Phone (800) 742-6809; (317) 448-1903. FAX (317) 448-4823. **Circle No. 396**

Networked microcontroller. Based on the Motorola MC68HC11F1 chip, the GCB11 is an 8-bit, networked microcontroller hardware-and-software package for distributed-control applications. The 3×4-in. board includes 32 kbytes of static RAM and 32 kbytes of ROM. The package comes with a set of development tools and network and application libraries. $179. **Coactive Aesthetics,** Box 425967, San Francisco, CA 94142. Phone (415) 626-5152. **Circle No. 397**

High-speed development platform. The DPS-1 Rev C is an SBus development platform for prototyping hardware and software. The development platform allows the designer to adapt new hardware or convert existing systems to the SBus. The kit uses LSI-Logic's L64853A DMA Plus controller. $1095. **Dawn VME Products,** 47073 Warm Springs Blvd, Fremont, CA 94539. Phone (800) 258-3296; (510) 657-4444. FAX (510) 657-3274. **Circle No. 398**



OTP and flash memory cards. The company's one-time-programmable (OTP) and flash memory cards follow PCMCIA standards and come with 256 kbytes to 1 Mbyte. Flash cards are available in 2-Mbyte density. OTP cards, $72 to $180; flash cards, $117 to $521. **Texas Instruments Inc,** Semiconductor Group SC-92044, Box 809066, Dallas, TX 75380. Phone in US and Canada, (800) 336-5236, ext 3990; elsewhere, (213) 995-6611, ext 3990. **Circle No. 399**



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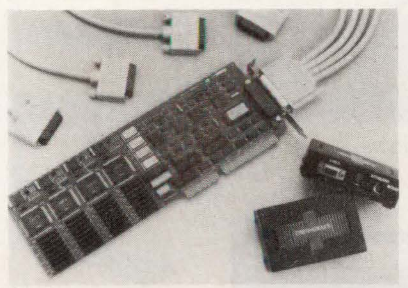
CIRCLE NO. 101

Magneto-optical drive. A 3.5-in. rewritable optical disk drive, the RF-3000 provides as much as 128 Mbytes of storage and is compatible with ISO/ANSI-standard 3½-in. magneto-optical disks. The drive has an average seek time of 38 μsec and transfer rates of 640 kbytes/sec. The drive is controlled through a SCSI bus, and two drives can be daisy-chained together. $2195; internal model, $1995. **Plasmon Data Systems Inc,** 1654 Centre Pointe Dr, Milpitas, CA 95035. Phone (800) 445-9400; (408) 956-9400. FAX (408) 956-9444. **Circle No. 400**

Keyboard network station. The 386SX-25-IDE Keyboard Network Station includes an IDE hard-disk drive in either 40, 80, 100, or 200 Mbytes. The pc within a keyboard has a standard 101/102 keyboard, 1 Mbyte of RAM (expandable to 16 Mbytes), a Super-VGA adapter, a 3½-in. floppy-disk drive, one parallel and two serial ports, and a 16-bit expansion slot. $1095. **Advanced Interlink Corp,** 15181 Springdale St, Huntington Beach, CA 92649. Phone (714) 894-1675. FAX (714) 893-1546. **Circle No. 401**



Multiple-VGA adapter kit. The Theo+Grafx Multi VGA Adapter Kit allows you to connect as many as four VGA monitors to one 386 or 486 host PC running DOS. The kit comprises the TG/4 multiuser video graphics adapter, software drivers, controller boxes, and cables. Kit for four users, $1895. **Theos Software Corp,** 1777 Botelho Dr, Suite 360, Walnut Creek, CA 94596. Phone (510) 935-1118. FAX (510) 935-1177. **Circle No. 402**

Multipurpose video boards. The Tango and Mambo boards for MS-DOS computers integrate multiple sources required for networked digital multimedia. Each board includes video display drivers, Ethernet drivers and interfaces, digital audio and video interfaces, and audio recording and playback capabilities. Tango, for standard monitors, $1895; Mambo, for portable computers with LCD screens, $1495. **Mediashare Corp,** 2035 Corte Del Nogal, Carlsbad, CA 92009. Phone (619) 931-7171. FAX (619) 431-5752. **Circle No. 403**

SBus board with SCSI interface. The TMS320C30 SBus board is based on the TI 33-MHz floating-point digital signal processor. The board has as much as 512k words of static RAM, dual-port RAM, analog-to-digital options, high-speed digital I/O from a disk at 2 Mbytes/sec, and a SCSI interface. $4795; with TI's Sun-4-based assembler/linker/C compiler, SMON30 debug monitor, C interface library, and SunOS device drivers, $9795. **Spectrum Signal Processing Inc,** 8525 Baxter Pl, 100 Production Ct, Burnaby, BC V5A 4V7, Canada. Phone (604) 421-5422. FAX (604) 421-1764. **Circle No. 404**

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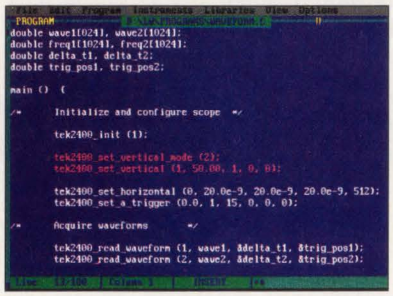

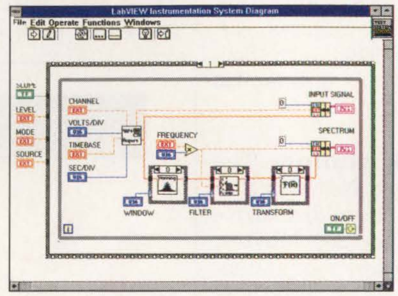

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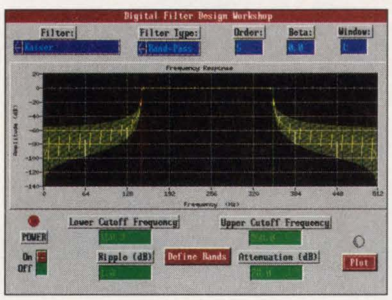

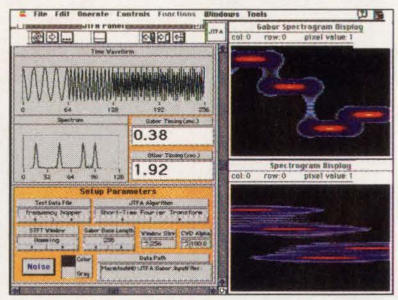

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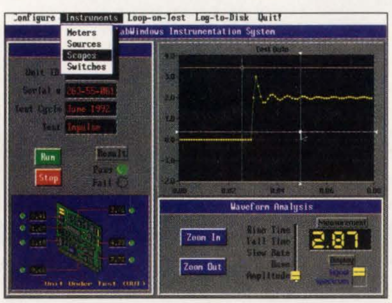

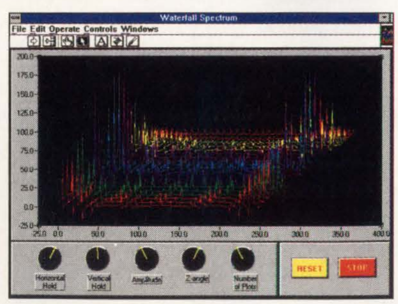

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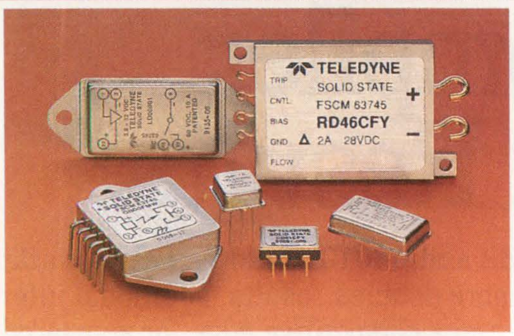

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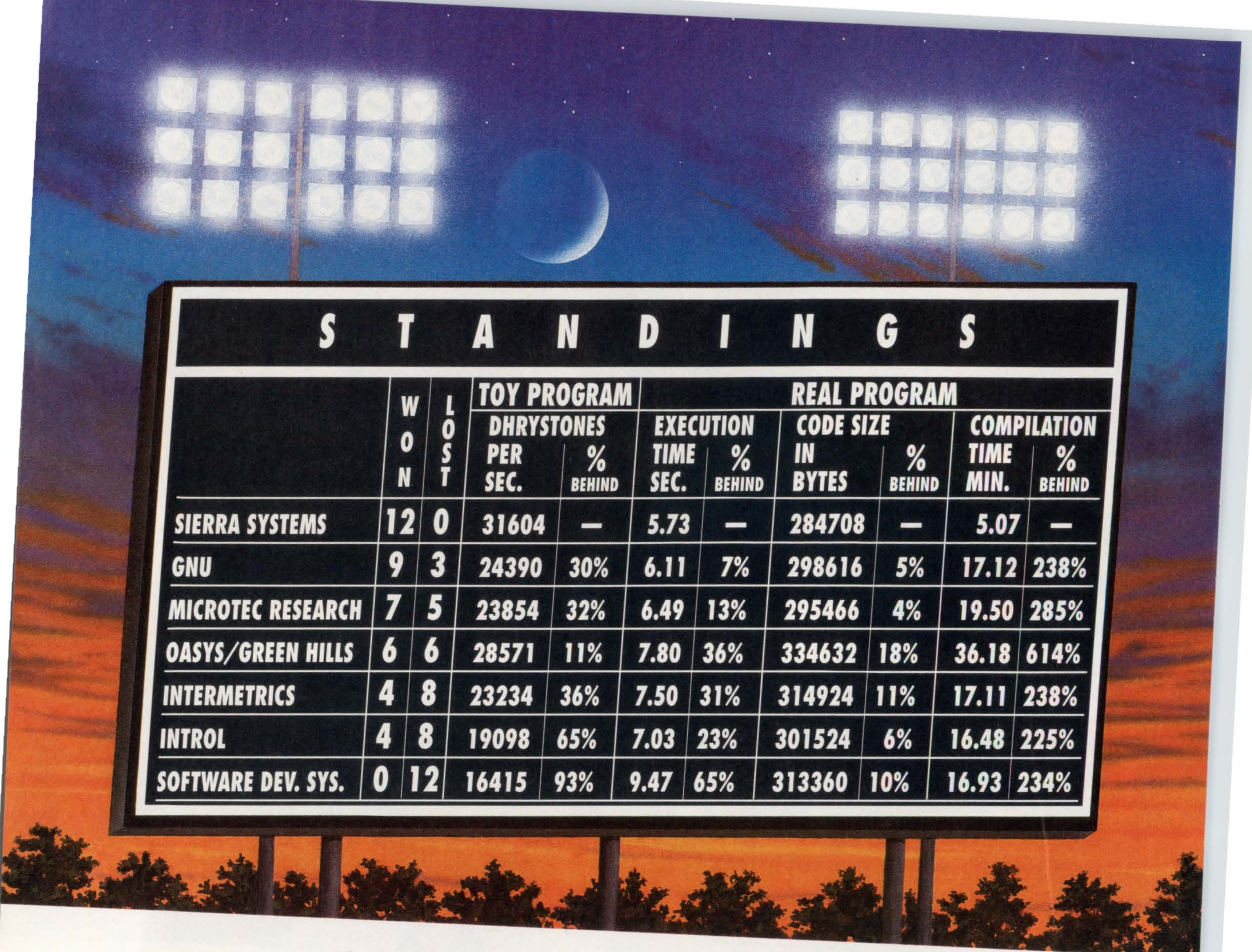
See EEM Volume B, Pages 1608-1612

CIRCLE NO. 104



STANDINGS

	WON	LOST	TOY PROGRAM: DHRYSTONES PER SEC.	% BEHIND	REAL PROGRAM: EXECUTION TIME SEC.	% BEHIND	CODE SIZE IN BYTES	% BEHIND	COMPILATION TIME MIN.	% BEHIND
SIERRA SYSTEMS	12	0	31604	—	5.73	—	284708	—	5.07	—
GNU	9	3	24390	30%	6.11	7%	298616	5%	17.12	238%
MICROTEC RESEARCH	7	5	23854	32%	6.49	13%	295466	4%	19.50	285%
OASYS/GREEN HILLS	6	6	28571	11%	7.80	36%	334632	18%	36.18	614%
INTERMETRICS	4	8	23234	36%	7.50	31%	314924	11%	17.11	238%
INTROL	4	8	19098	65%	7.03	23%	301524	6%	16.48	225%
SOFTWARE DEV. SYS.	0	12	16415	93%	9.47	65%	313360	10%	16.93	234%

68000 Compiler Benchmark Results.

Sierra Systems undefeated on the 68040. Two benchmarks were selected, Dhrystone 2.1 (the Toy program) and the Sierra Systems production C compiler (the Real program). The compiler was selected because both its size and complexity are representative of real-world applications.

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Won/Lost Record: For each benchmark, the compilers' run-time performances were compared to each other with wins and losses totalled in round-robin fashion. (See Dhrystones and Execution Time columns on scoreboard.)
Compilers: GNU 2.0, Intermetrics 8.0, Introl 3.06, Microtec Research 4.2d, Oasys/Green Hills 1.8.5Rc, Sierra Systems 3.0, Software Development Systems 5.1.
Hosts: 33 MHz 386 Zeos PC and Sun SPARCstation IPC. All compilers were run on the PC, except for GNU and Oasys/Green Hills, which were run on the Sun. Running the Sierra Systems compiler on both host systems allowed the Sun times to be scaled to PC time for the scoreboard.
Target: Motorola VME167, 25 MHz 68040 with caches enabled.

SierraSystems

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CIRCLE NO. 108

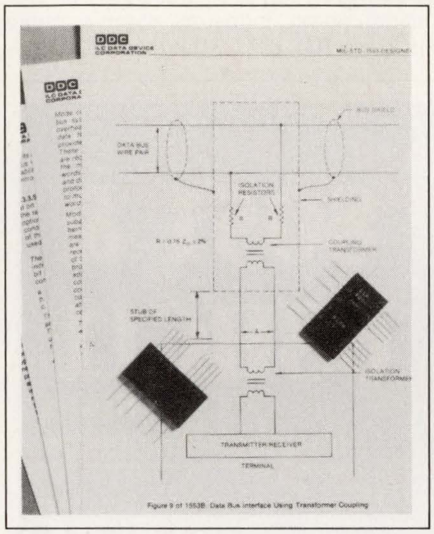
Surface-mount socket. This 100-position development socket is a surface-mountable component with essentially the same pc-board footprint as the quad flatpack (QFP) device. In this way, you can prototype a pc board using the socket and then transfer to production using bare QFPs, without board layout changes. $35. **Altera Corp,** 2610 Orchard Pkwy, San Jose, CA 95134. Phone (408) 984-2800. **Circle No. 413**

Interface converter. Model 285 RS-232C to RS-422/RS-485 interface converter can be configured in five user-selectable modes. This flexibility allows support of any master-slave configuration found in industrial applications. Other features include a DTE/DCE switch, TD and RD LEDs, and a programmable terminating resistor. $148. **Telebyte Technology Inc,** 270 E Pulaski Rd, Greenlawn, NY 11740. Phone (800) 835-3298; (516) 423-3232. FAX (516) 385-8184. **Circle No. 414**

Optical modules. The Astrotec 1238 transmitter operates at rates of 1200 Mbps. The 1318 receiver provides conversion for data rates of 20 to 1500 Mbps. The receiver's dynamic range measures 26 dBm. Both units are housed in 20-pin DIPs compatible with SONET standard packages. Model 1238, $1295; 1318, $1000. Delivery, 12 weeks ARO. **AT&T Microelectronics,** 555 Union Blvd, Dept 520404200, Allentown, PA 18103. Phone (800) 372-2447, ext 843; in Canada, (800) 553-2448, ext 843; (908) 771-2826. **Circle No. 415**

Sensing resistors. PMA-Cu and PMB-Cu 4-terminal resistors are rated for 1 and 2.5W, respectively. Designed for Kelvin measurements, the units are available with values as low as 0.001Ω. Construction features Manganin alloy foil banded to copper substrates for good thermal performance and accuracy to 0.5%. From $1.50 (10,000). Delivery, stock to eight weeks ARO. **Isotek Corp,** 566 Wilbur Ave, Swansea, MA 02777. Phone (508) 673-2900. FAX (508) 676-0885. **Circle No. 416**

Power supplies. PU110 Series supplies are available in single- (5V/22A, 12V/9A, 15V/7.5A, and 24V/4.5A) and multiple-output (combinations of 5V/10A, 12V/5A, 24V/1A, −5V/1A, and −12V/1A) models. Features include EMI filter, power-fail signal, overvoltage protection, and short-circuit protection. Efficiency equals 65%. $115; less than $60 (OEM qty). **International Power Sources Inc,** 200 Butterfield Dr, Ashland, MA 01721. Phone (508) 881-7434. FAX (508) 879-8669. TWX 510-100-3630. **Circle No. 417**



Low-profile transformers. DLP Series transformers have a 0.13-in.-high profile and are designed for MIL-STD-1553A or B serial-data-bus systems. The line includes 14 models that feature frequently used turns ratios. They are available with either straight tin-plated flatpack leads or tin-plated gull-wing leads for surface-mount packages. All units have center-tapped primaries and multitapped secondaries. $125. Delivery, 12 weeks ARO. **Beta Transformer Technology Corp,** 40 Orville Dr, Bohemia, NY 11716. Phone (516) 244-7393. FAX (516) 244-8893. **Circle No. 418**

LEDs. These multichip lamps have a warm white output. The units are available in T-1-¾ and T-3-¼ models with voltage ratings ranging from 5 to 120V ac and dc. Available bases range from midget flanged to miniature screw and include wedge, bi-pin, bayonet, and all telephone-style slide bases. Life ratings equal 100,000 hours. From $4.99. Delivery, stock to 75 days ARO. **Lamp Technology,** 1645 Sycamore Ave, Bohemia, NY 11716. Phone (516) 567-1800. FAX (516) 567-1806. **Circle No. 419**

Connector. The DLM6 360 ZIF connector has 360 contacts and features an aluminum housing that provides EMI/RFI shielding. Lifetime equals 10,000 mating/unmating cycles. The gold over beryllium copper contacts, rated for 5A/1200V ac, are available in either a crimp snap-in version or 0.025-in. square posts for pc-board and wire-wrapping applications. Less than $150 (OEM qty) for a plug-receptacle pair. Delivery, 12 weeks ARO. **ITT Cannon,** 1851 Deere Ave, Santa Ana, CA 92705. Phone (714) 757-8257. **Circle No. 420**

Trimmer capacitors. Series 47000 trimmers are designed for RF and microwave applications. The units are supplied with either a removable cap or a poke-seal. The poke-seal replaces the traditional O-ring design. Voltage rating equals 500V and Qs measure 2500 min at 250 MHz. Operating range spans −65 to +125°C. $6 (1000). Delivery, six to eight weeks ARO. **Johanson Manufacturing Corp,** Rockaway Valley Rd, Boonton, NJ 07005. Phone (201) 334-2676. TXW 710-987-8367. **Circle No. 421**

Power supplies. The modular construction of the SPR5 Series 2000W power supply allows for as many as 15 outputs with an ac input and 9 outputs with a 48V dc input. The units are certified to UL1950 and IEC950 and feature fan cooling. Available options include battery backup, output paralleling with current sharing, and VME/VXI-compatible signals. $1150 (100) for a 3-output model. **Power One,** 740 Calle Plano, Camarillo, CA 93010. Phone outside CA, (800) 235-5943; in CA, (800) 421-3439; (805) 987-8741. TWX 910-336-1297. **Circle No. 422**

Relays. Designed for switching capacitive loads, this line of relays includes 15 models capable of isolating as much as 65,000V dc and switching currents as high as 1500A at speeds of 500 nsec. The relays are sealed so there's no contact oxidation. In addition, the sealed units are compatible with applications involving explosive atmospheres. From $105 (100). **Kilovac Corp,** Box 4422, Santa Barbara, CA 93140. Phone (800) 253-4560; (805) 684-4560. FAX (805) 684-9679. **Circle No. 423**

Connector. The NE-1 is a metal-on-elastomer connector, which features more than 200 conductors per inch. With a 0.6-mm electrode, the unit can carry 100 mA/mm^2. With 0.25-mm-wide gold-plated electrodes, contact resistance measures less than 50 mΩ. The connectors are available in lengths ranging to 250 mm. $1 per linear in. (1000). **Shin-Etsu Polymer America Inc,** 34135 Seventh St, Union City, CA 94587. Phone (510) 475-9000. FAX (510) 475-0613. **Circle No. 424**

Edge connectors. Designed specifically for AT- and XT-compatible computers, Lyte Series connectors feature a double row of solder tails on 0.2-in. centers. Contact positions are 18/36+31/62, 31/62, and 18/36. The units meet the performance criteria of MIL-C-21097 and operate over a −55 to +105°C range. $0.24 to $1. **Cinch Connectors,** 1500 Morse Ave, Elk Grove Village, IL 60007. Phone (708) 981-6000, ext 6043. **Circle No. 425**

Inductors. Series 2512 molded surface-mount power inductors cover a range of 1 to 100 μH. Standard tolerance equals 10%. Maximum current ratings range from 260 to 1640 mA. The solder-coated copper terminations are compatible with all soldering operations. $0.599 (1000). Delivery, four to six weeks ARO. **American Precision Industries,** 270 Quaker Rd, East Aurora, NY 14052. Phone (716) 652-3600. FAX (716) 652-4814. **Circle No. 426**

LED lamps. SLR Series LEDs have a 10,000-hour operating life. Model SLR-56 is a T-1-¾ lamp with an illumination of 6.3 to 10 mcd. Models SLR-37 and SLR-34 are T-1 devices with luminous intensities of 10 to 16 mcd. All units are available in red, red-orange, yellow, yellow-green, and green. From $0.07 (1000). Delivery, eight weeks ARO. **ROHM Corp,** 3034 Owen Dr, Antioch, TN 37013. Phone (615) 641-2020, ext 131. FAX (615) 641-2022. **Circle No. 427**

Headers. TMT Series surface-mount units are available with either single or double rows of contacts on 0.05-in. centers. Lead coplanarity measures 0.006 in., and the plastic housings can withstand infrared and vapor-phase soldering processes where temperatures do not exceed 230°C for 60 sec and 260°C for 10 sec. From $0.038 per pin. **Samtec Inc,** Box 1147, New Albany, IN 47151. Phone (800) 726-8329; (812) 944-6733. FAX (812) 948-5047. TLX 333918. **Circle No. 428**

Pin monitors. The PLeCMO-84-ZL/A takes the place of 84-pin plastic leaded chip carriers (PLCCs) in a target socket. The hinged ZIF lid accepts PLCCs as well as J-bend and ceramic LCCs. The lid is rated for 10,000 insertions min. It accepts 50-mil pitch devices. The unit terminates in a male PLCC plug. $221. **EDI Corp,** Box 366, Patterson, CA 95363. Phone (209) 892-3270. **Circle No. 429**

Inductors. RL-3745 and RL-3750 devices are low-power inductors available in values ranging from 150 to 1000 μH. Current ratings range from 0.5 to 1.7A. The devices are available in packages for vertical mounting with a pc-board footprint of 0.5×0.7 in. or in low-profile packages with a mounted height of 0.45 in. $0.99 (1000). Delivery, stock to eight weeks ARO. **Renco Electronics Inc,** 60 Jefryn Blvd E, Deer Park, NY 11729. Phone (516) 586-5566. **Circle No. 430**

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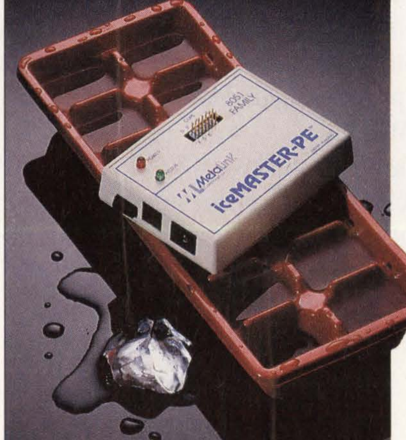

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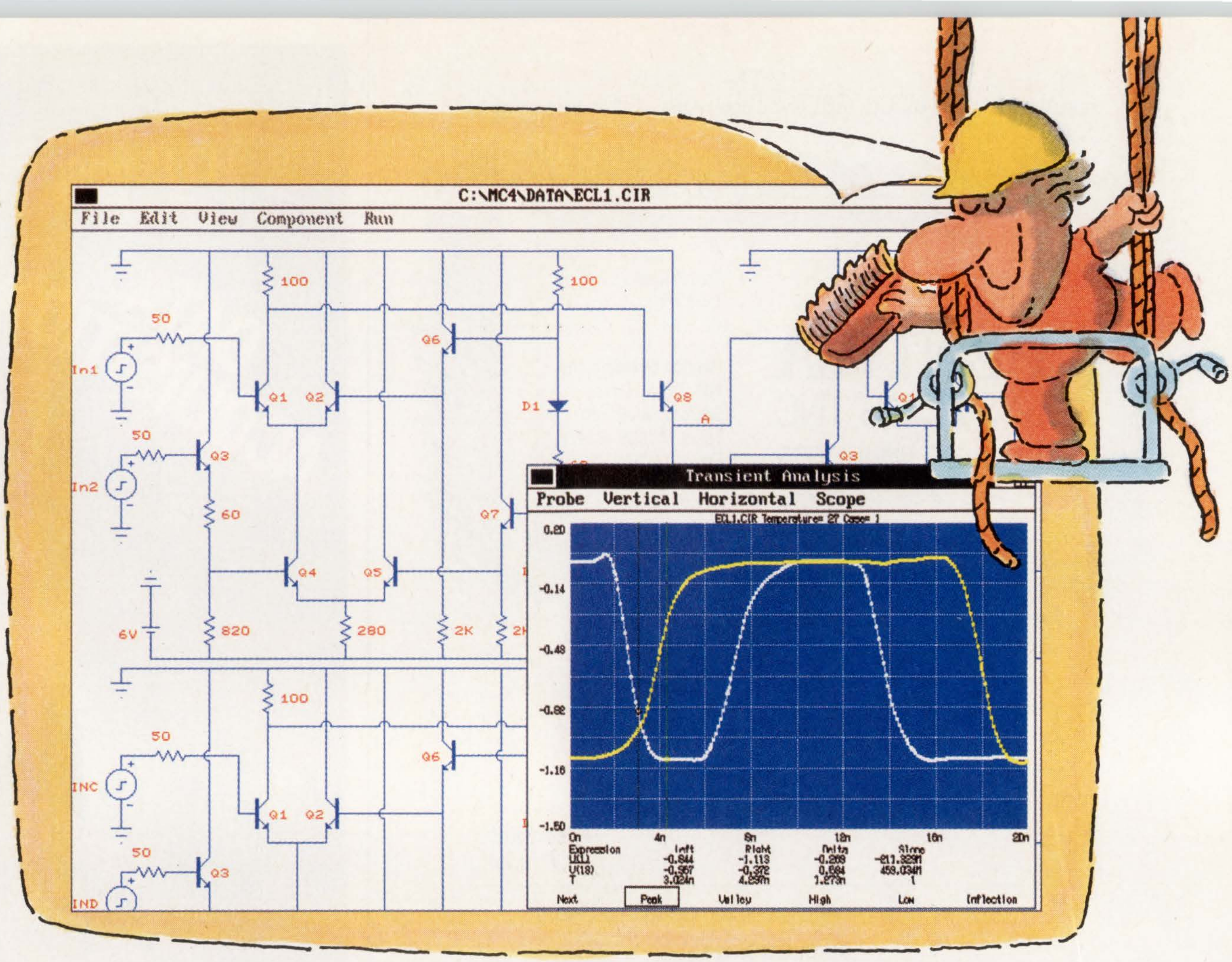

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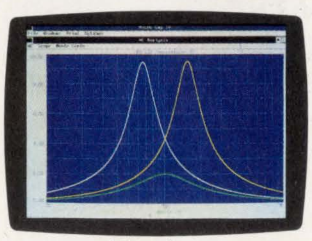
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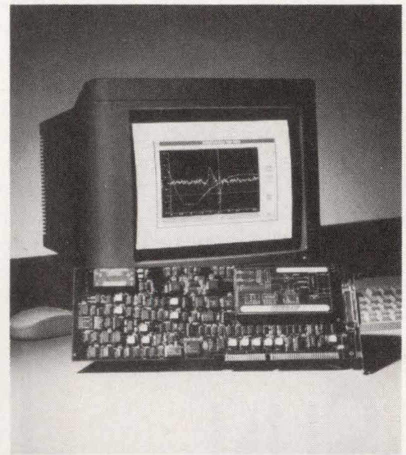
Philips Test and Measurement, Building TQIII-4, 5600 MD Eindhoven, The Netherlands. Phone local office.
Circle No. 406

8-channel, 250k-sample/sec, simultaneous S/H ADC board for ISA bus. The DT2833 has eight differential inputs. It can simultaneously sample all of its input signals and then convert them with 12-bit resolution at 250k sam-

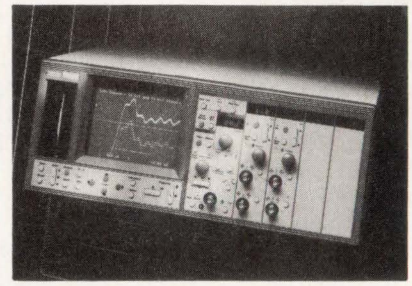


ples/sec. The board includes patented circuits that correct for offset on any channel. It also includes a pair of 12-bit D/A converters, eight lines of digital I/O, and two counter timers. The vendor supplies an MS-Windows data-acquisition library for its Global Lab software at no cost with the board. The library costs $95 if purchased separately. You save $1000 if, when you buy the board, you also buy Global Lab, its signal-processing library, and printing module. $2595. **Data Translation Inc,** 100 Locke Dr, Marlborough, MA 01752. Phone (508) 481-3700. FAX (508) 481-8620. TLX 951646. **Circle No. 407**

WAN protocol analyzer. The 4959A is intended for installation and maintenance testing of wide-area networks (WANs). It has an expansion slot that you can use to adapt it to testing of high-speed networks, such as 2-Mbps SMDS (switched-multimegabit data service) and frame-relay networks. The unit also runs MS-DOS application software on an 80386SX µP with as much as 8 Mbytes of RAM. $10,995; remote troubleshooting software, $990. **Hewlett-Packard Co,** Box 58059, MS 51L-SJ, Santa Clara, CA 95051. Phone (800) 452-4844. **Circle No. 408**

Transformer tester. The AT3500 mounts on a bench top; it measures transformer turns ratios, mutual inductance, leakage inductance, magnetizing current, winding resistance, open-circuit voltage, and interwinding capacitance. It also measures line-frequency breakdown voltage between windings and from the windings to the core. You can vary the ramp and dwell times in breakdown tests. The unit can make most measurements at frequencies from 10 Hz to 1 MHz. It measures magnetizing current to 2.5 kHz. The tester operates in stand-alone mode or coupled to a PC. $49,000. **Voltech Inc,** 200 Butterfield Dr, Ashland, MA 01721. Phone (508) 881-7329. **Circle No. 409**

8/16-channel, 12-bit, 100k-sample/sec ADC boards for ISA bus. The DAS-1400 series includes two units, each with four programmable gains (1, 2, 4, and 8 or 1, 10, 100, and 500). A 3-channel programmable timer and several counters in the boards' ASIC provide flexible triggering. A burst mode mimics simultaneous S/H operation for slowly changing signals. The boards include eight digital-I/O channels. The vendor supplies drivers for several versions of Basic and a terminate-and-stay-resident application that lets you pop a control panel onto the screen. A $99 software option includes drivers callable from programs in additional languages and file I/O drivers for all languages. $699. **Keithley Metrabyte,** 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. FAX (508) 880-0179. **Circle No. 410**



Deep-memory DSOs. The Pro 32 (2 channels, 12 bits, 20M samples/sec), Pro 42 (4 channels, 12 bits, 20M samples/sec), Pro 34 (2 channels, 14 bits, 5M samples/sec), and Pro 44 (4 channels, 14 bits, 5M samples/sec) are modular units that can have memory, which can store 4M samples. The Pro 92 includes both the 12-bit digitizer of the Pro 32 and 42 units and an 8-bit, 200M-sample/sec ADC. $11,490 to $29,990. **Nicolet Measurement Instruments,** 5225 Verona Rd, Madison, WI 53711. Phone (800) 356-8088; (608) 271-3333. FAX (608) 273-5061. **Circle No. 411**

Universal IC programmer. By using "job disks," production personnel can quickly set up the Allpro-88XR to program specific devices for specific applications. The job disk (a floppy disk) contains data and programming algorithms as well as command sequences that you would normally enter from the keypad or a host PC. The 88-pin programmer has a DAC-per-pin architecture and handles devices packaged in DIPs and plastic leaded chip carriers. It operates in stand-alone and PC-hosted modes and includes a floppy-disk drive, an LCD, and a keypad. A 40-Mbyte hard drive is optional. You can use either a parallel or a serial (57.6-kbps) interface to link the programmer to a PC. The software runs under MS Windows. $9995. **Logical Devices Inc,** 1201 NW 65th Pl, Fort Lauderdale, FL 33309. Phone (305) 974-0967. FAX (305) 974-8531. **Circle No. 412**

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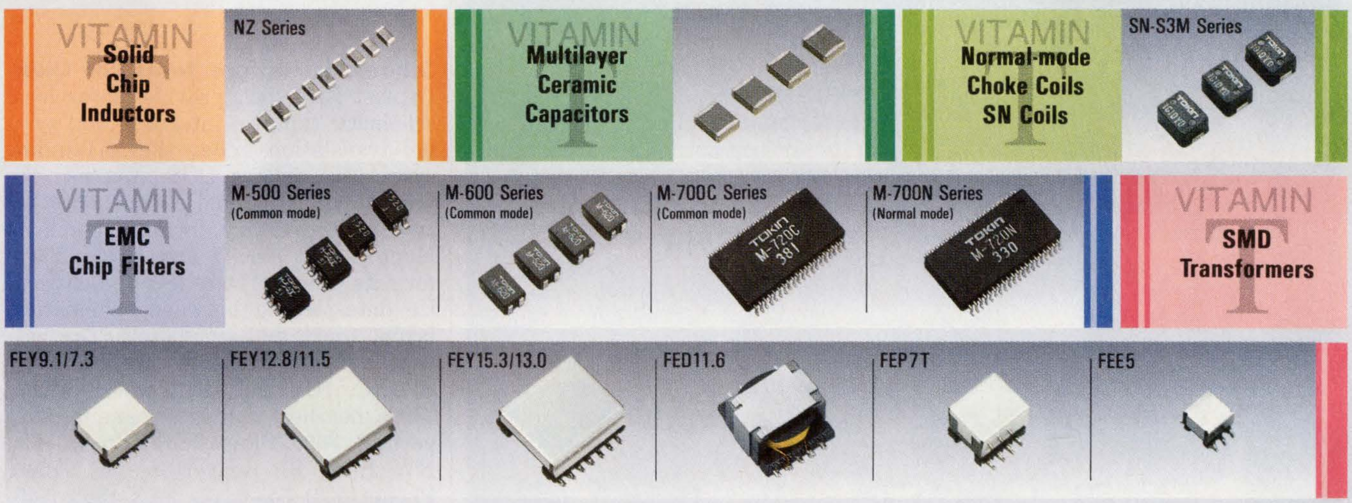

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CIRCLE NO. 111

Development tools. A set of integrated development tools for the Motorola CPU32 family of microcontrollers includes the Validate/XEL debugger interface and language tools, instruction-set simulator, Codetap, emulator, and support services. The tools run on PCs, Sun SPARCstations, and DECstations. Each tool priced separately, $2000 to $15,000. **Applied Microsystems Inc,** Box 97002, Redmond, WA 98073. Phone (206) 882-2000. **Circle No. 351**

VHDL source-code libraries. The VHDL Source Model Libraries consist of a Small Scale Integration (SSI) Library with more than 600 standard logic parts and a Memory Library with more than 1200 commonly used memory devices including static RAMs, dynamic RAMs, and EPROMs. Both libraries comply with VHDL (VHSIC Hardware Description Language) IEEE-1076 and run in Mentor System 1076, Cadence VHDL-XL, Viewlogic Viewsim, Synopsys VHDL System Simulator, and Vantage Spreadsheet. Site licenses for Memory Library, from $18,000; for SSI Library, from $12,000. **Logic Modeling Corp,** 1520 McCandless Dr, Milpitas, CA 95035. Phone (408) 957-5200. FAX (408) 945-9181. **Circle No. 352**

Nonlinear curve-fitting software. Peakfit 3 is an update to the company's chromatography/spectroscopy-analysis software package for PCs. The analysis techniques use nonlinear curve fitting to reduce noise and separate and characterize unresolved peaks in overlapping peak data. You can observe and control the nonlinear fitting process graphically on screen. $595. **Jandel Scientific,** 2591 Kerner Blvd, San Rafael, CA 94901. Phone (800) 874-1888; (415) 453-6700. FAX (415) 453-7769. **Circle No. 353**

Schematic-capture tools for Unix. Capfast EDA tools provide hierarchical schematic capture, interface, and symbol translation under the X-Window system as well as DOS. You use the tools to translate and extract data between proprietary formats, such as Mentor, and ASCII and EDIF 2 0 0 formats. The software lets you customize data-passing between schematics, layout tools, and simulators. The network version runs under Unix on Sun/SPARC, HP, and DEC workstations. $4995 per host computer; annual support fee, $600. **Phase Three Logic,** 1600 NW 167th Pl, Beaverton, OR 97006. Phone (503) 645-0313. FAX (503) 645-0207. **Circle No. 354**

Internal and boundary-scan test translation. With software called TSSI version 5.0 you do scan test using existing testers and without dedicated scan-test hardware. The Waveform Database portion of the software stores, edits, manages, and augments test data produced by CAE tools such as those from Cadence, Synopsys, and Texas Instruments. The software combines scan and primary input and output values with timing information, tester protocols data on shift chain order and produces programs that are tester ready. From $10,000. **TSSI,** 8205 SW Creekside Pl, Beaverton, OR 97005. Phone (503) 643-9281. FAX (503) 646-4954.

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Synthesis tools. The suite of synthesis tools called Dazix Synergy Synthesis assists with the design of ASICs. The software provides Archsyn for behavioral synthesis of VHDL, Verilog, and C HDLs (hardware-description languages), $15,000; Macrosyn for datapath synthesis, $10,000; Logsyn for timing-driven logic synthesis and optimization, $30,000; Testsyn for test synthesis and automatic test-pattern generation, $25,000; and Libsyn for building synthesis models, $10,000. **Dazix,** 1 Madison Industrial Park, Huntsville, AL 35894. Phone (205) 730-2000. FAX (205) 730-8344.

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DSP source-code interface. Using any one of more than 35 plug-in DSP boards, Hypersignal-Macro lets you create and add DSP algorithm and product code. The DSP Source Code Interface available for a variety of popular DSP chips, contains a library of math and DSP routines. The interface allows transfer of data, such as data recording, instrumentation, measurement, and simulation acceleration, between the DSP chip and the software. Hypersignal-Macro software, $989; DSP Source Code Interface, $795. **Signalogic,** 9704 Skillman, #111, Dallas, TX 75243. Phone (214) 343-0069. FAX (214) 343-0163.

Circle No. 357

Numeric compiler. Adding to the High Tech Basic product line, the HTBasic DOS 386/486 Numeric Compiler focuses on the subroutines, which often require the greatest amount of time to execute. The compiler lets you produce numeric-intensive subprograms without requiring additional programming skills. The company claims that much of the PC-based Rocky Mountain Basic code will run at speeds comparable to the fastest HP Basic workstations. $1325. Upgrade for current HTBasic users, $450. **Transera Corp,** 3707 North Canyon Rd, Provo, UT 84604. Phone (801) 224-6550. FAX (801) 224-0355. TLX 296438.

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Behavioral model synthesis. Analog Model Synthesis for the company's Saber simulator eliminates the use of equations or modeling code to create behavioral models. Instead, it uses graphical data from previous simulations or laboratory instrument readings and automatically transforms them into behavioral models. $2000. **Analogy Inc,** 9205 SW Gemini Dr, Beaverton, OR 97075. Phone (503) 626-9700. FAX (503) 643-3361.

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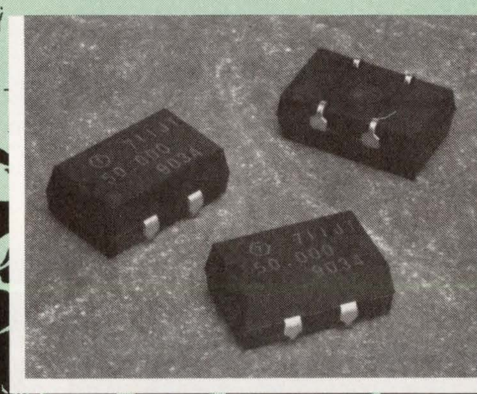
Multidescription design-capture tools. Design Expressions, a suite of multidescription design-capture tools, lets you define functionality at any level of abstraction by a variety of familiar graphical and textual methods. It includes gate-level designs with schematic capture, register transfer level with state machines, graphical state diagrams, truth tables, and Boolean equations; behavior, structural and data-flow designs with VHDL syntax-



directed editor; and analog behavioral-level designs. $15,000. **Dazix,** 1 Madison Industrial Park, Huntsville, AL 35894. Phone (205) 730-2000. FAX (205) 730-8344. **Circle No. 360**

ROM development kit. C-thru-ROM version 2.00 is a development kit to build stand-alone programs that run from ROM on Intel's 80x86 or NEC's

V-Series CPUs. It works with Microsoft C7 or C++, Borland C++, and the manufacturer's ROMview debugger. The ROMView debugging tool lets you start remote debugging on a stand-alone target system without tying up target-system serial ports or RAM. ROMview works with Borland's Turbo Debugger or the company's RDEB debugger. C-thru-ROM, $495; ROMview, $395. **Datalight,** 307 N Olympic Ave, Suite 201, Arlington, WA 98223. Phone (800) 221-6630; (206) 435-8086. FAX (206) 435-0253. **Circle No. 361**

Engineering-change-order software. Sherpa/View lets you view and comment on documents electronically, eliminating serial, paper-based approval processes. The product is integrated in Sherpa/PIMS, the company's information-management system, which eliminates the need for CAD seats for simply viewing documents; you can view data and make annotations from a 386-based PC on the network. Single copy, $745 to $1445. **Sherpa Corp,** 611 River Oaks Pkwy, San Jose, CA 95134. Phone (408) 433-0455. FAX (408) 943-9507. **Circle No. 362**

Real-time operating system. OS-9000 version 1.3 allows real-time data-acquisition and control tasks to be combined with DOS supervisory or postprocessing programs. The package includes VPC (Virtual PC), a DOS emulation program that runs DOS and Windows programs under OS-9000. The module emulates the DOS BIOS from OS-9000 RAM and transfers data between the two operating systems. $995. **Microware Systems Corp,** 1900 NW 114th St, Des Moines, IA 50325. Phone (800) 475-9000; (515) 224-1929. FAX (515) 224-1352. TWX 910-520-2535. **Circle No. 363**

Test system for ICs. The Analytical Probestation is an integrated system for CAD-driven probing and testing of complex integrated circuits. The system combines accurate probing and automated layout integration for verification, characterization, and failure analysis. The integrated system eliminates the need to assemble lab components from various sources. XL/ATS configuration, $400,000. **Integrated Measurement Systems Inc,** 9525 SW Gemini Dr, Beaverton, OR 97005. Phone (503) 626-7117. FAX (503) 644-6969. **Circle No. 364**

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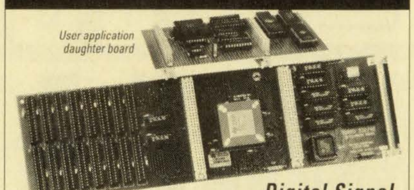

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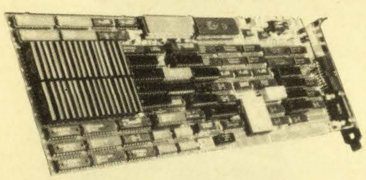

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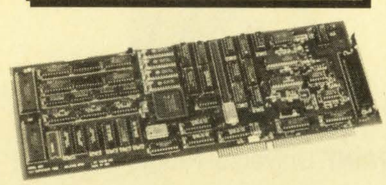

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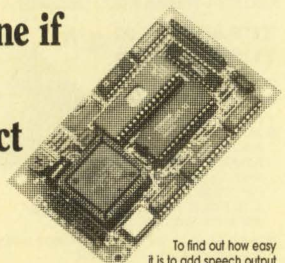

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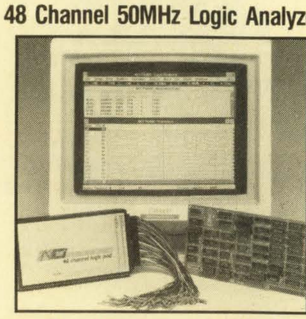

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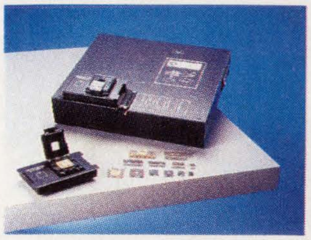

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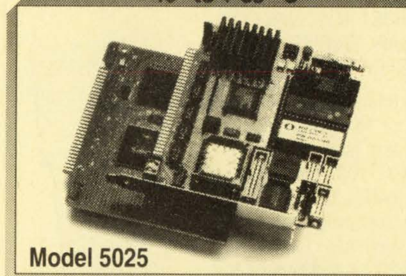

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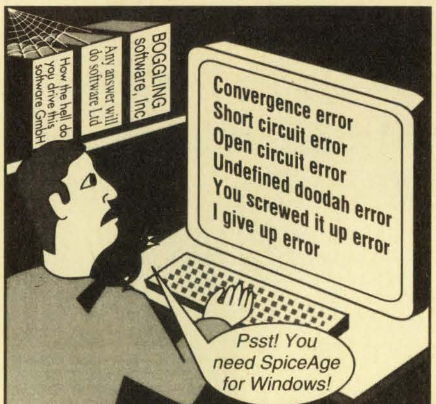

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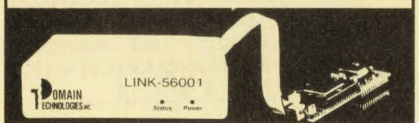

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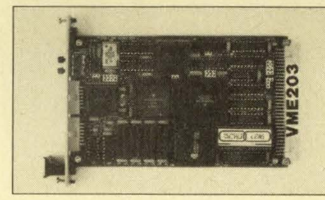

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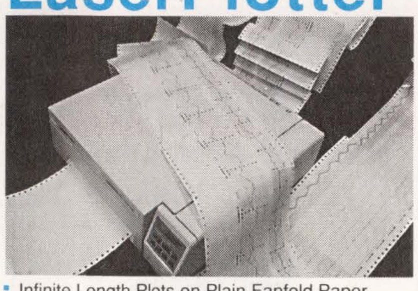

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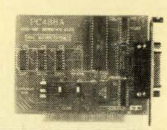

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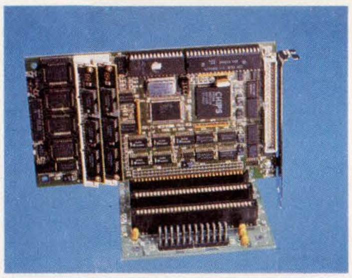

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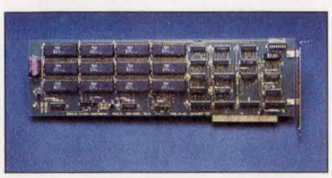

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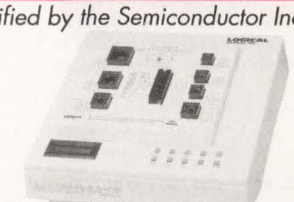

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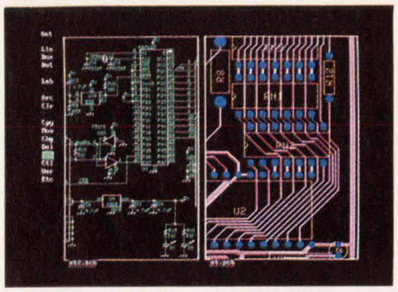

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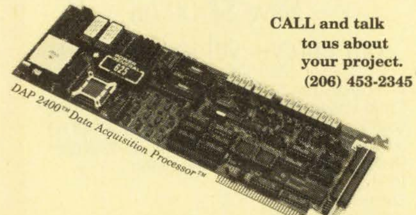

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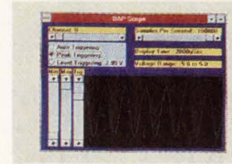

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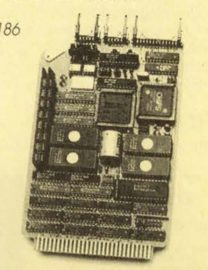

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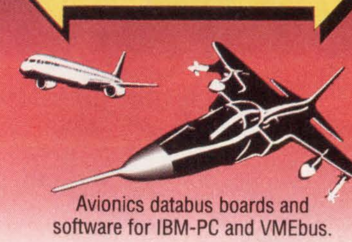

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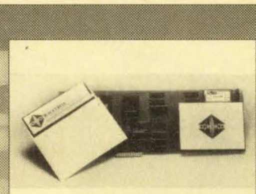

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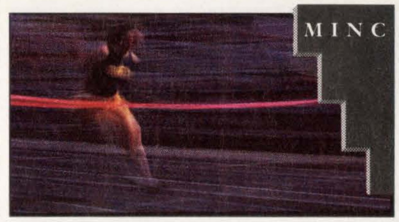

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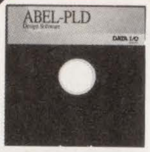

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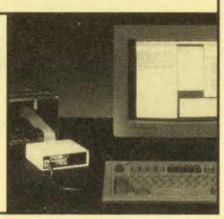

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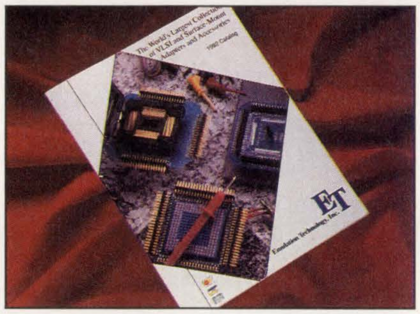

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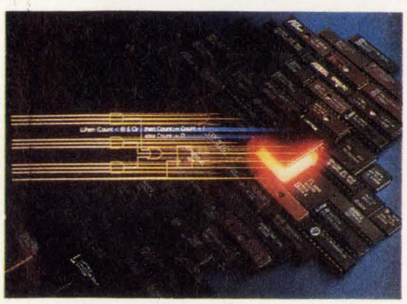

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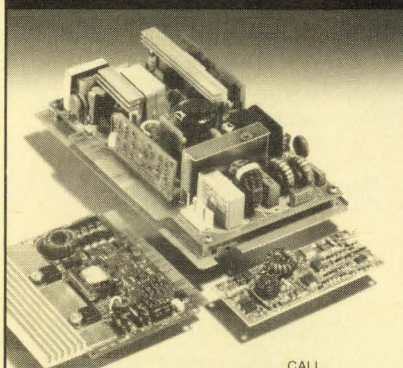

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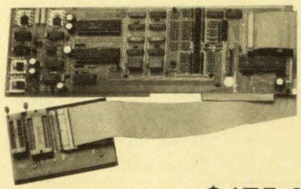

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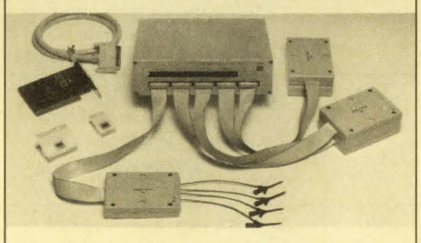

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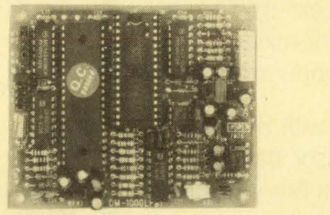

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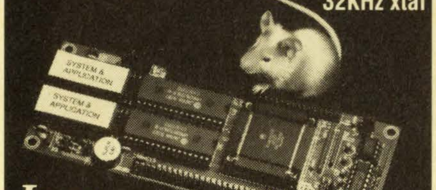

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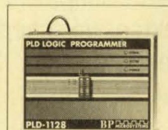

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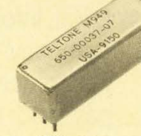

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1992 Recruitment Editorial Calendar

Issue	Issue Date	Ad Deadline	Editorial Emphasis
News Edition	Oct. 8	Sept. 24	CAE • PC/Workstation Design • Engineering Management Special Series
Magazine Edition	Oct. 15	Sept. 24	Disk Drives • Portable-Computer Design • Switching Power Supplies • Design it Right Series—Part II
News Edition	Oct. 22	Oct. 8	Data Storage Technology Communications Technology Regional Profile: Michigan, Illinois, Missouri
Magazine Edition	Oct. 29	Oct. 8	ELECTRONICA SHOW ISSUE • Object-oriented Programming • Chipsets for PCs Design it Right Series—Part III Wescon Preview Issue
News Edition	Nov. 5	Oct. 22	COMDEX/WESCON SPECIAL ISSUE • Special Supplement: Design for Portability • Microprocessors • Wescon/Comdex Hot Products • CAE Software • Diversity Special Series
Magazine Edition	Nov. 12	Oct. 22	COMDEX/WESCON SPECIAL ISSUE • Integrated Circuits • Test & Measurement • Design it Right Series—Part IV
WESCON '92 SHOWGUIDE & PRODUCT SPOTLIGHT		Oct. 9	A free page available to all advertisers running a full page in 2 out of 3 Wescon issues.
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Magazine Edition	Nov. 26	Nov. 5	19th Annual Microprocessor Directory • ASICs • Sensors • EDN's "Innovation Crusade"—Winners Coverage
News Edition	Dec. 3	Nov. 19	ICs & Portable Computers • Power Sources • Laptops/Portables • Low-power Design • Regional Profile: Massachusetts, New Hampshire
Magazine Edition	Dec. 10	Nov. 19	INTERNATIONAL PRODUCT SHOWCASE—Vol. I • Power Sources • ICs & Semiconductors • Software • Hardware & Interconnect
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Date Available	I Will Travel		
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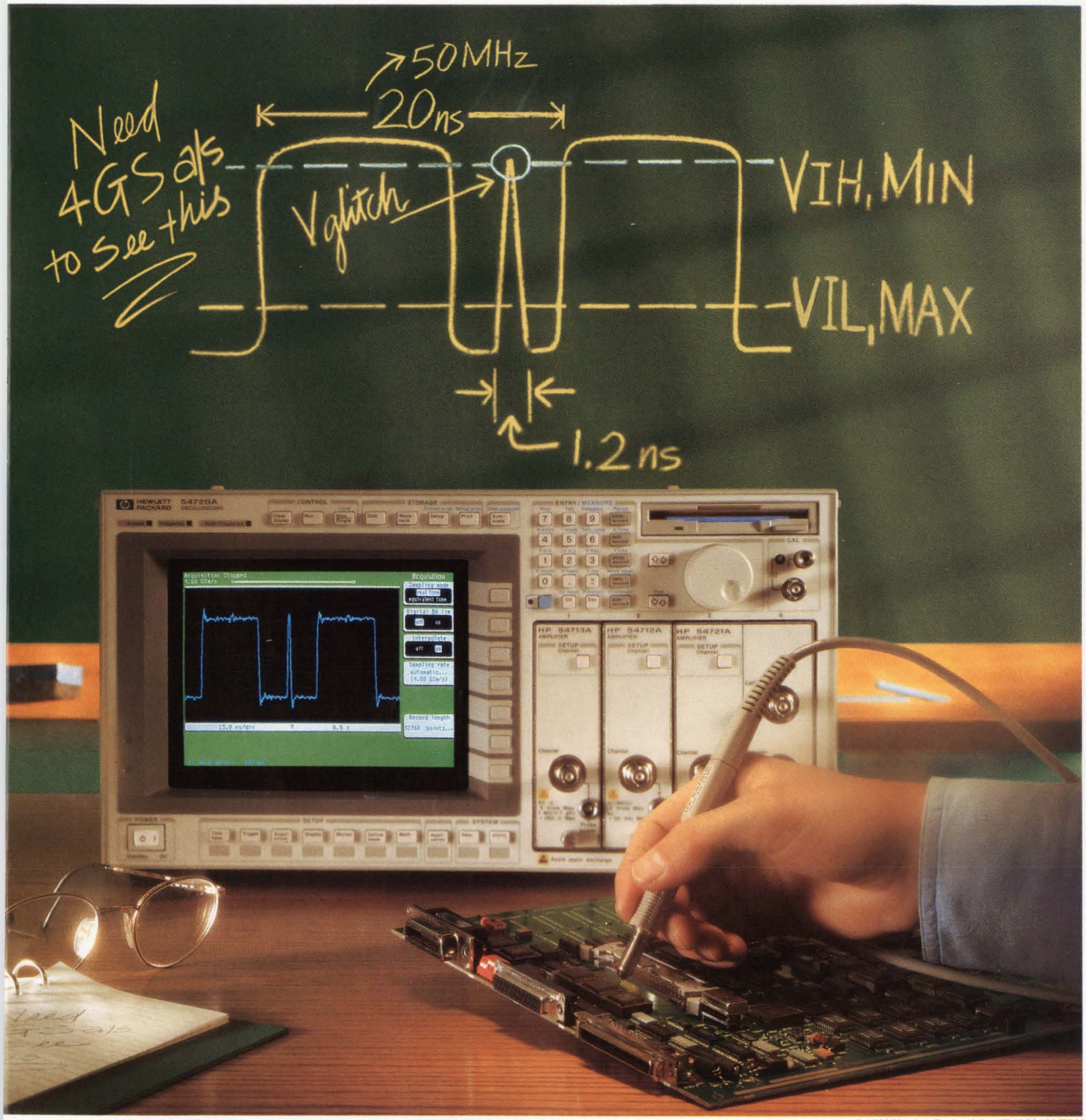

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