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ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

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A CAHNERS PUBLICATION

November 12, 1992

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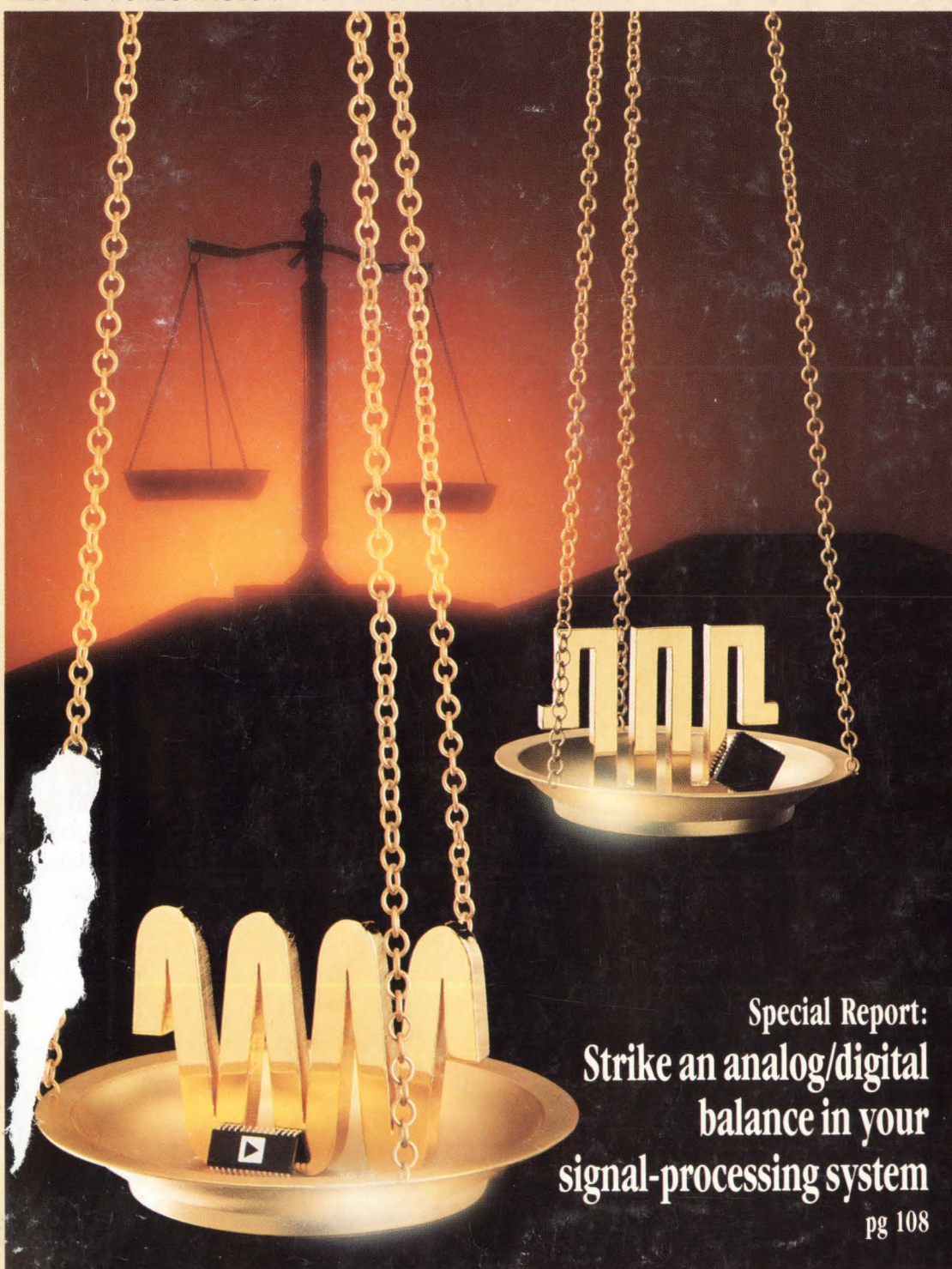
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Special Report:
**Strike an analog/digital
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pg 108

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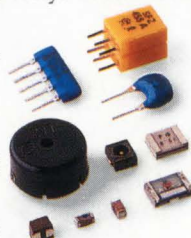
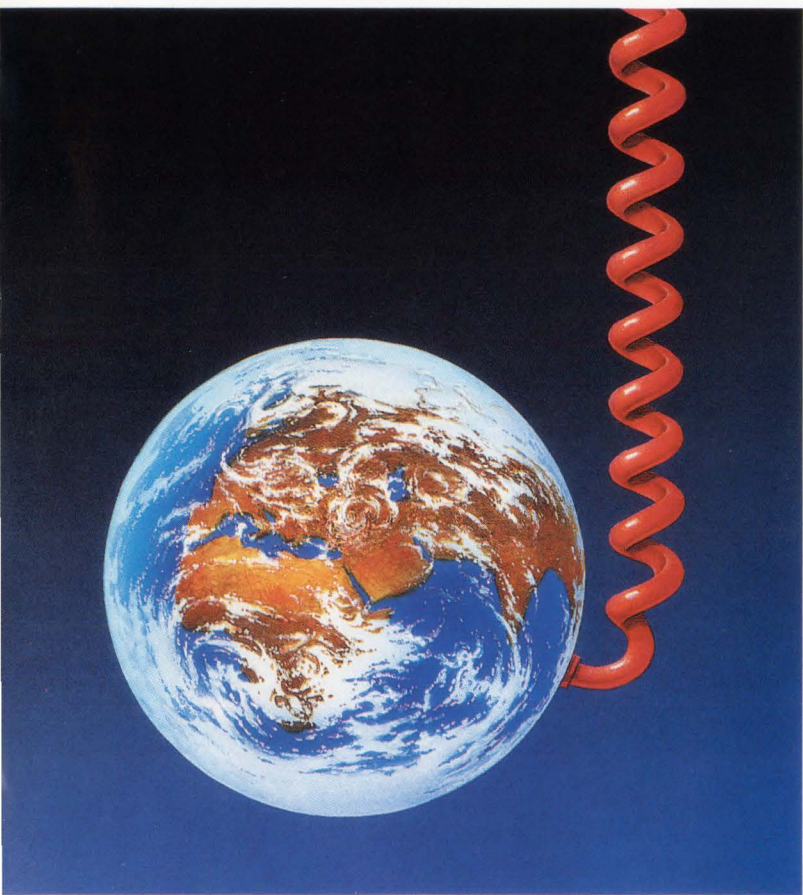
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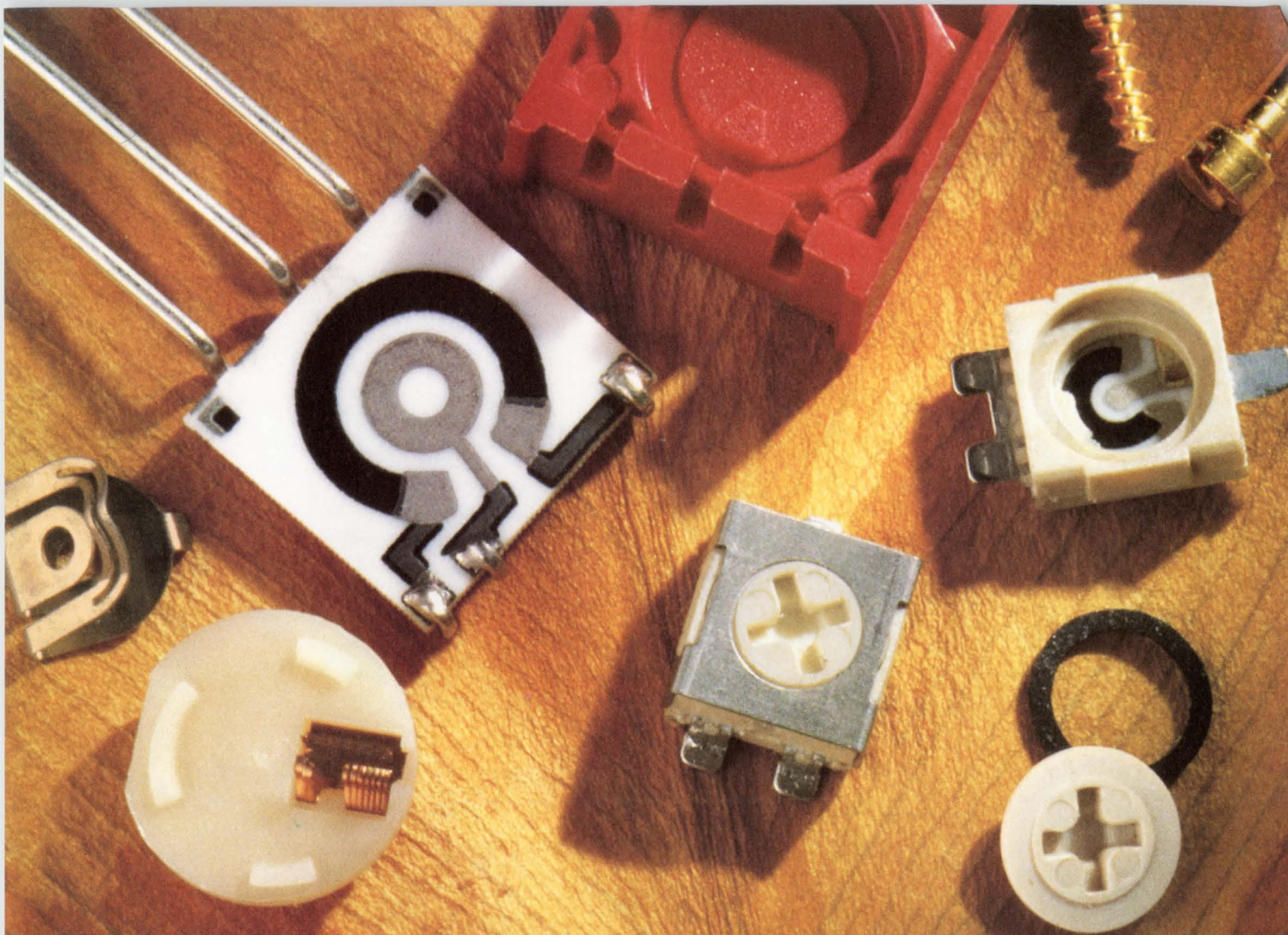


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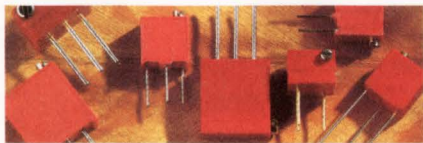
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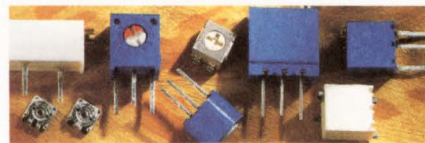
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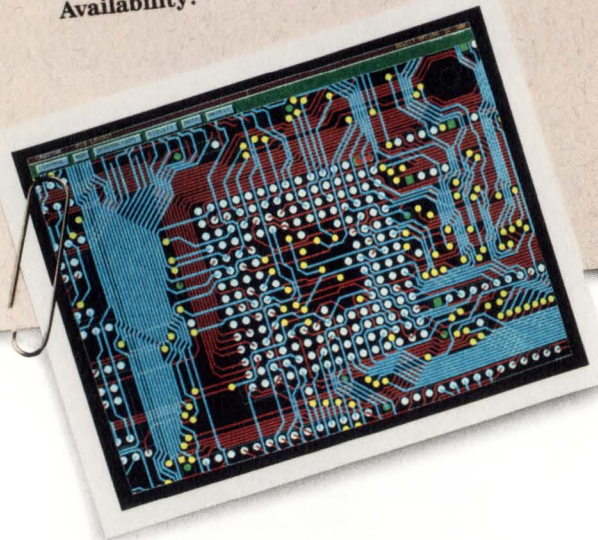
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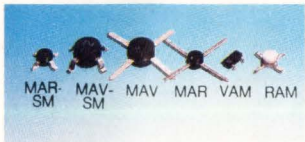
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	1.04	1.40	1.50	1.60	1.34	1.80	1.75	2.15	
	MAV-1	+MAV-2	+MAV-3	MAV-4					
	1.15	1.45	1.55	1.65					
CERAMIC SURFACE-MOUNT	RAM-1	RAM-2	RAM-3	RAM-4	RAM-6	RAM-7	RAM-8		
	4.95	4.95	4.95	4.95	4.95	4.95	4.95		
PLASTIC FLAT-PACK	MAV-1	+MAV-2	+MAV-3	MAV-4				MAV-11	
	1.10	1.40	1.50	1.60				2.10	
	MAR-1	MAR-2	MAR-3	MAR-4	MAR-6	MAR-7	MAR-8		
	0.99	1.35	1.45	1.55	1.29	1.75	1.70		
Freq. MHz, DC to	1000	2000	2000	1000	2000	2000	1000	1000	
Gain, dB at 100MHz	18.5	12.5	12.5	8.3	20	13.5	32.5	12.7	
Output Pwr. +dBm	1.5	4.5	10.0	12.5	2.0	5.5	12.5	17.5	
NF, dB	5.5	6.5	6.0	6.5	3.0	5.0	3.3	3.6	

Notes: + Frequency range DC-1500MHz ++ Gain 1/2 dB less than shown

designer's amplifier kits

DAK-2: 5 of each MAR-model (35 pcs), only \$59.95

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DAK-3: 3 of each MAR, MAR-SM, MAV-11, MAV-11SM (48 pcs) \$74.95

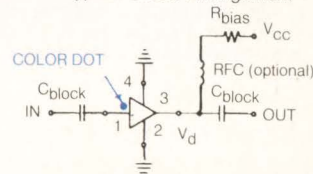
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80 x 50	1000, 2200, 4700, 6800, 10,000 pf
120 x 60	.022, .047, .068, .1µf

Typical Circuit Arrangement



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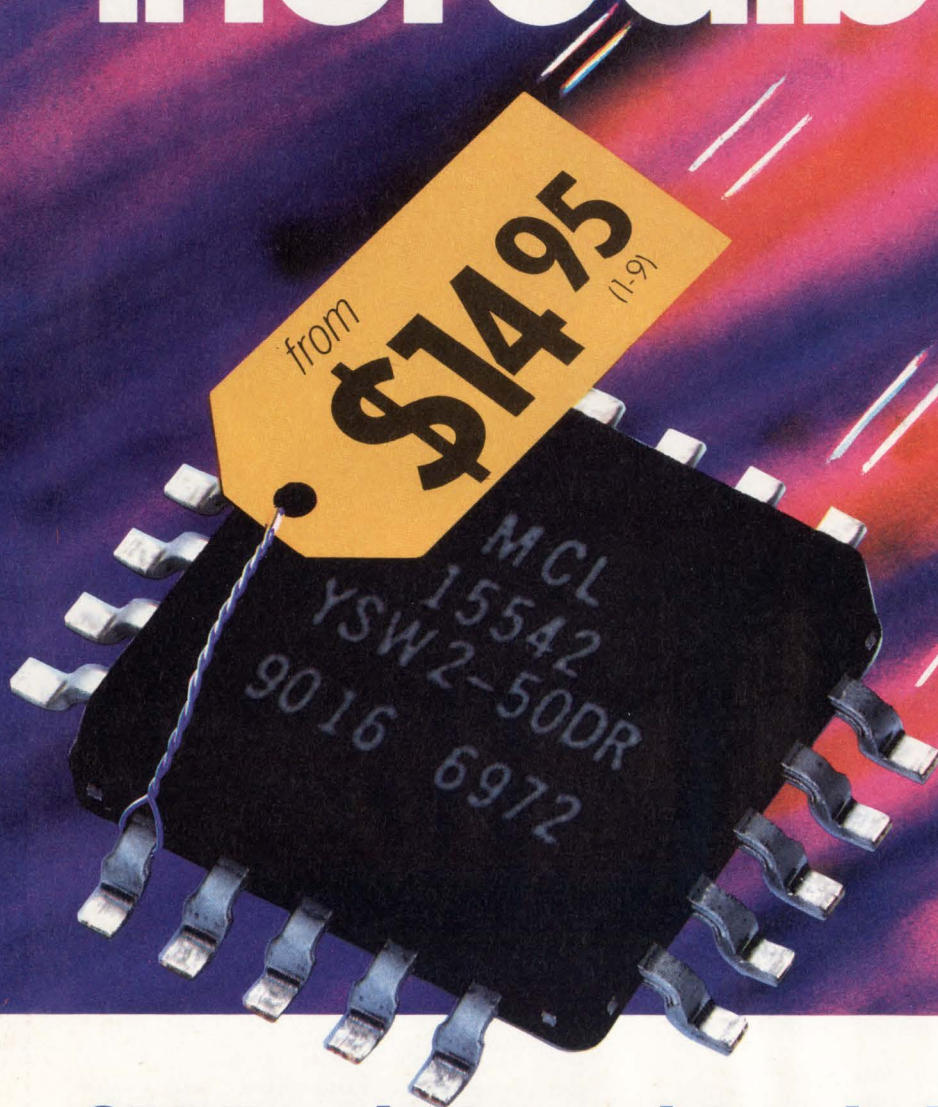
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SPECIFICATIONS (typ)

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	YSWA-2-50DR	ZYSA-2-50DR	ZYSWA-2-50DR	YSW-2-50DR	ZYSW-2-50DR	ZYSW-2-50DR
Frequency (MHz)	dc-500	500-2000	2000-5000	dc-500	500-2000	2000-5000
Ins. Loss (dB)	1.1	1.4	1.9	0.9	1.3	1.4
Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	—	20	—	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
Sw. Spd. (nsec)	3	3	3	3	3	3
Price, \$ (1-9 qty)	YSWA-2-50DR (pin) 23.95 ZYSWA-2-50DR (SMA) 69.95			YSW-2-50DR (pin) \$14.95 ZYSW-2-50DR (SMA) 59.95		



On the cover: Both types of signal processing—*analog and digital*—have their own advantages. You've got to weigh the tradeoffs between the two before selecting the best components for your signal-processing system. (Photo courtesy Analog Devices.) Our Special Report begins on **PAGE 108**

Foldout Contents

Turn to the last information-retrieval service card in the back of this magazine and you'll find a foldout table of contents. Now, instead of flipping back and forth from this table of contents to the articles you want to read, you can have the convenient foldout open at all times while you're reading EDN. Use the foldout contents to mark off articles you'd like your colleagues to read or to remind yourself to copy stories for your files.



ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

Signal processing

SPECIAL REPORT

Designing an optimum signal-processing system means choosing components, both analog and digital, based on their relative strengths.—*Anne Watson Swager, Technical Editor*

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Design It Right—Part IV

DESIGN FEATURES

This final part covers how to increase effectiveness by bringing in outside help.—*Dan Strassberg, Senior Technical Editor*

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Wescon/92 show preview & products

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Rigorous testing of SCSI disk drives and arrays ensures peak performance

Thorough testing can distinguish your SCSI disk drive or array from your competitors' by ensuring that your product meets its performance, reliability, and data-availability goals.—*Herbert W Silverman, Peer Protocols Inc*

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You can obtain boundary scan's benefits despite use of some nonscan ICs

Boundary scan simplifies testing of digital subassemblies and pc boards. Some people think that serious use of the technique must wait until scannable versions of all ICs become available. You don't need to.

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—*Jon Turino, Logical Solutions Technology Inc*

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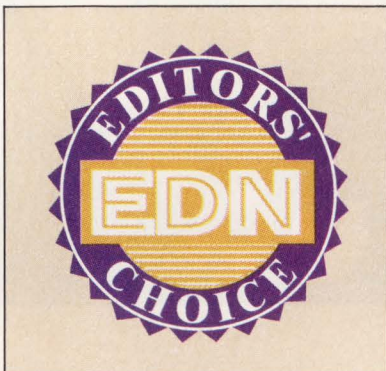
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EDN's editors have selected VLSI Technology's antifuse technology as this issue's Editors' Choice. . . . PAGE 75

DESIGN FEATURES

Common Access Method simplifies development of SCSI device drivers

The Common Access Method (CAM) drastically reduces the effort you need to expend when developing device drivers for SCSI peripherals. CAM lets you develop a single device driver for SCSI pc boards that adhere to the CAM standard.—*Chris Borgers and Dave O'Shea, Future Domain Corp*

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Architectural choices provide the key to reliable fixed-point filters

Fixed-point DSP μ Ps offer significant cost-performance advantages over their floating-point counterparts when creating digital filters. Unfortunately, fixed-point filters can yield poor performance if improperly implemented. Selecting the right architecture is the key to successful designs.—*Fred J Taylor, University of Florida; Glenn S Zelniker, Monica A B Murphy, Henry A Gancedo, The Athena Group Inc*

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TECHNOLOGY UPDATES

Comdex/Fall '92 targets technology for multimedia and connectivity

Two thousand exhibitors and 130,000 attendees will converge in Las Vegas for this bigger-than-ever annual gathering of the computerized faithful.—*J D Mosley, Technical Editor*

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- Live-insertion module allows board "hot swap" 76
- Multimedia hardware/software combo for PCs 78

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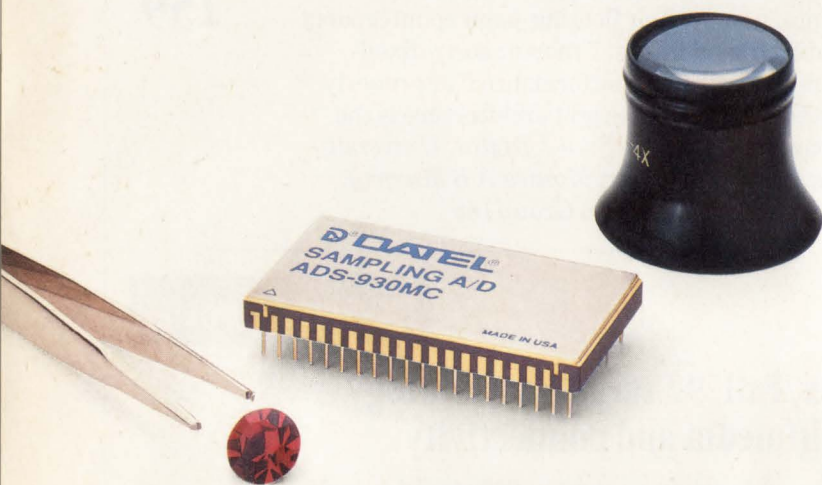
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Clock-buffer IC prevents skew-ups in P5 PC designs 82

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EDITORIAL

Take your tools

Each of us has special talents and abilities that can serve us well, but you've got to share them to enjoy them.—*Jon Titus, Editor*

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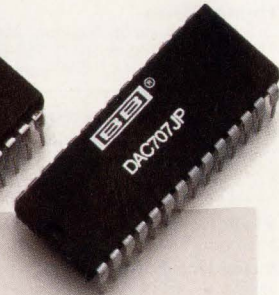
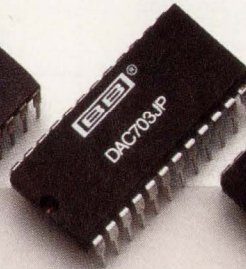
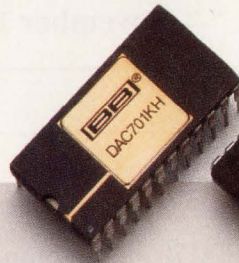
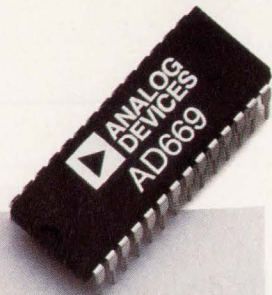
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Introducing the AD669, the first complete 16-bit monolithic DAC.



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Bipolar Offset	±15mV	N/A	±20mV	±20mV
Double-buffered Latches	Yes	No	No	Yes
Monolithic	Yes	Yes	Yes	No
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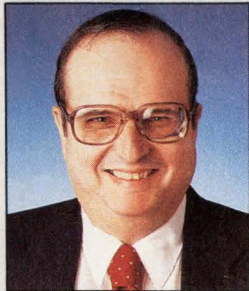
INSIDE EDN

A summary and analysis of articles in this issue

Dan Strassberg wraps up his 4-part Design It Right series with a look at strategic partnerships. Two stories in this segment relate what happened when companies designing with custom ICs brought in outside help. Today, Dan says, it's a rare occurrence when a product that uses custom ICs doesn't rely on another company or division. For this article, Dan also interviewed industry legend Bernie Gordon to get a behind-the-scenes look at how his company—Analogic—aggressively pursues the partnering concept.

manufacturers of electronic components, ICs and semiconductors, test and measurement equipment, and design automation products. Turn to our show coverage for a preview of some of the more significant products that will be on display. Gary Legg also gives you a run-down of the 40 technical sessions that will run concurrently with the exhibits.

Those interested in recent developments in anything computer related might want to check out J D Mosley's overview of the Comdex show. Technical sessions will be



Dan Strassberg



Anne Swager



J D Mosley

The subject of signal processing gets an in-depth treatment in our cover story by Anne Swager. DSP is making major inroads in what used to be a traditional analog stronghold. But because most signal-processing systems rely on both analog and digital components, you need a firm foundation in the strengths and weaknesses of each type of device before you start designing. Anne discusses the trade-offs, updates you on the innovative improvements in traditional analog-processing ICs, and gives a glimpse of the novel signal-processing approaches used by two pioneering start-up companies.

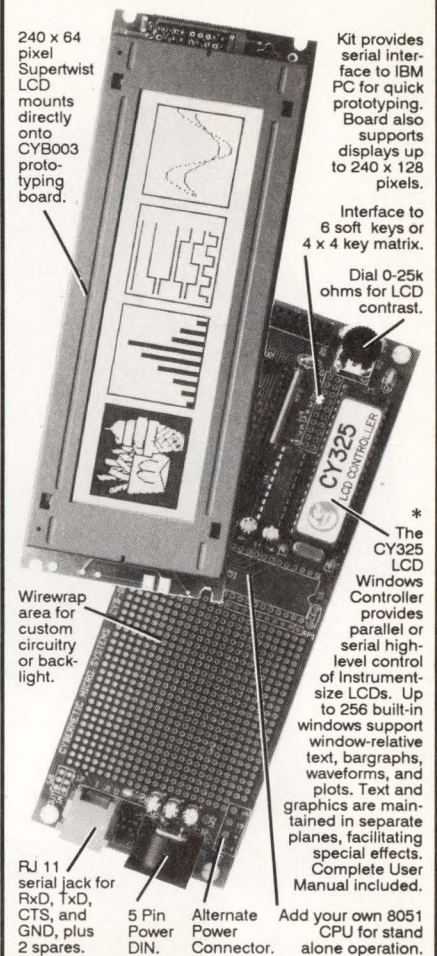
We call this issue our "show issue." What that means to you is products, products, and more products. Wescon, which will be held in Anaheim, CA on November 17 to 19, is expected to house 1250

dedicated to network computing, multimedia, imaging applications, and OEM business issues. And 2000 exhibitors will bring their wares to the Las Vegas sites, with 350 exhibitors alone displaying multimedia systems and products. For those of you who have been disappointed in not being able to attend both the Wescon and Comdex shows because of their overlapping schedules, take heart: J D points out that Wescon will take place in September, starting next year.

Joan Morrow Lynch
Managing Editor

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CIRCLE NO. 7



Increased 386 Perform

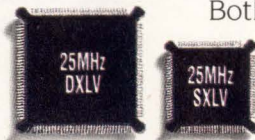
AMD's 3-Volt 386 Microprocessors Deliver The Longest Battery Life For Portable Computing.

The power struggle continues. While you can get a 386 microprocessor that goes fast, you'll still burn through a battery charge in a hurry. Low-voltage 386 CPUs from AMD are the answer—the Am386™SXLV and Am386DXLV microprocessors.

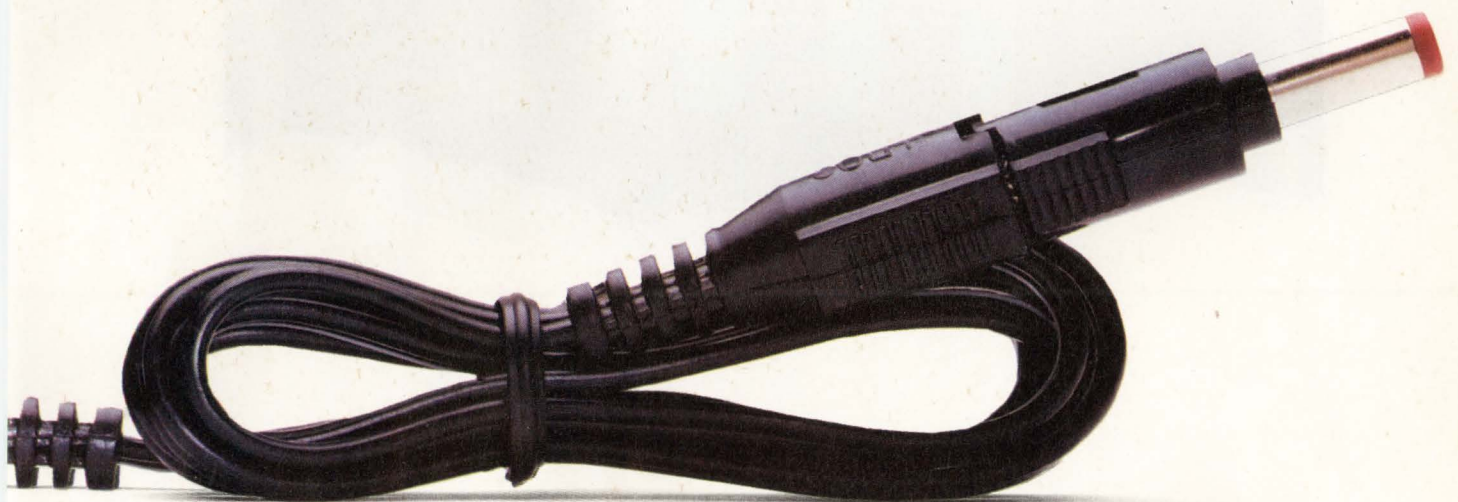
Here are two CPUs made not only to go fast, but to go the distance with portable computer users. Unlike common power-hungry 386s, these low-voltage CPUs

run on 3 volts. And they automatically slip into a static "sleep" mode to save power whenever the processor is idle. So users depend less on recharge units—and get the longest operational battery life.

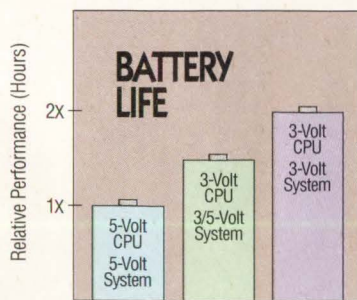
Both Am386 CPUs were designed to fit as comfortably in your budget as they do your portable computers. But you won't compromise on performance because the Am386SXLV and Am386DXLV 3-volt microprocessors both run at 25MHz. So



The 25MHz DXLV and the 25MHz SXLV are available in PQFP packaging.



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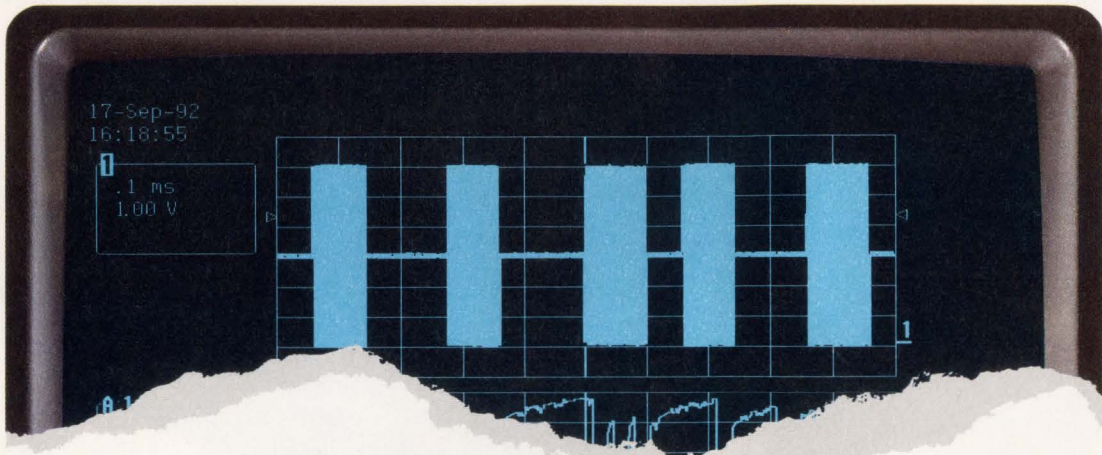


Advanced Micro Devices

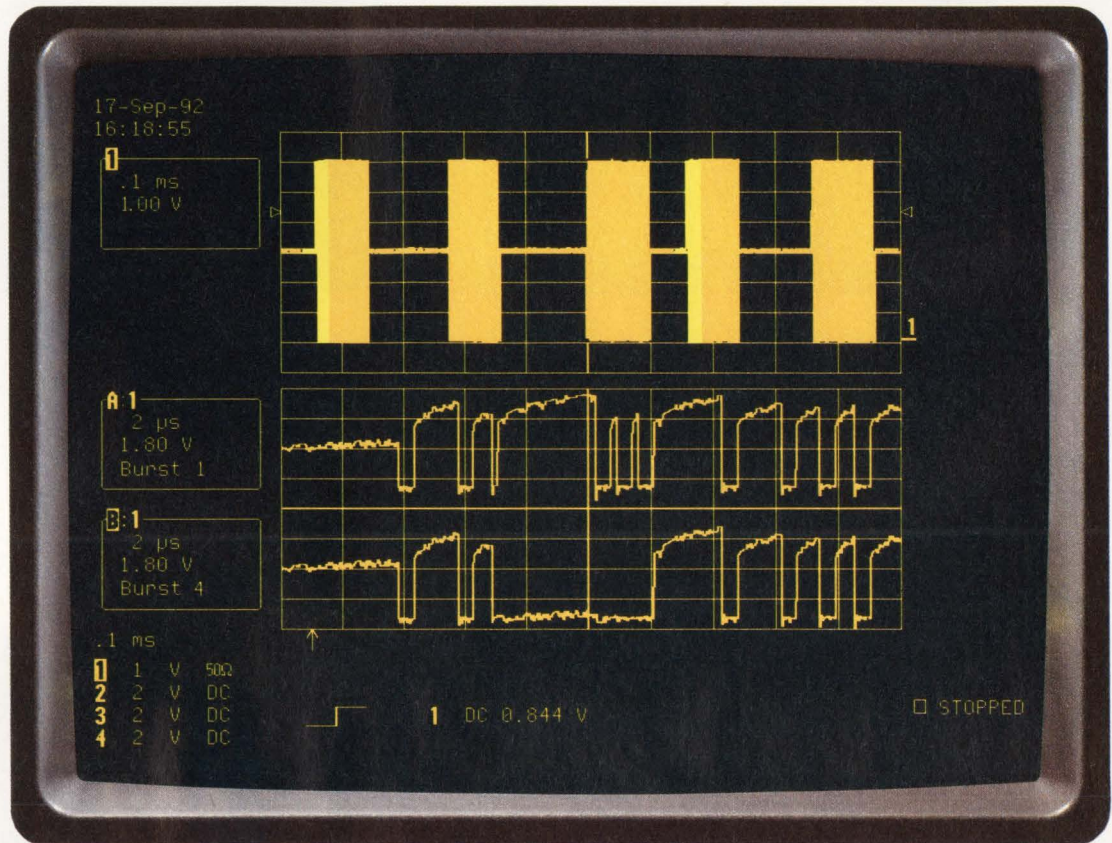
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KM41V4000BLL	4Mx1	SELF REFRESH	70 ns
KM44V1000BL	1Mx4	LOW POWER	70 ns
KM44V1000BLL	1Mx4	SELF REFRESH	70 ns
KM416V1000AL	1Mx16	LOW POWER	70 ns
KM416V1000ALL	1Mx16	SELF REFRESH	70 ns
KM48V2000AL	2Mx8	LOW POWER	70 ns
KM48V2000ALL	2Mx8	SELF REFRESH	70 ns

Fast page mode on all



the 16-meg in speeds up to 70 nanoseconds. Which seems all the more remarkable when you consider that reduced voltage generally tends to *decrease* performance.

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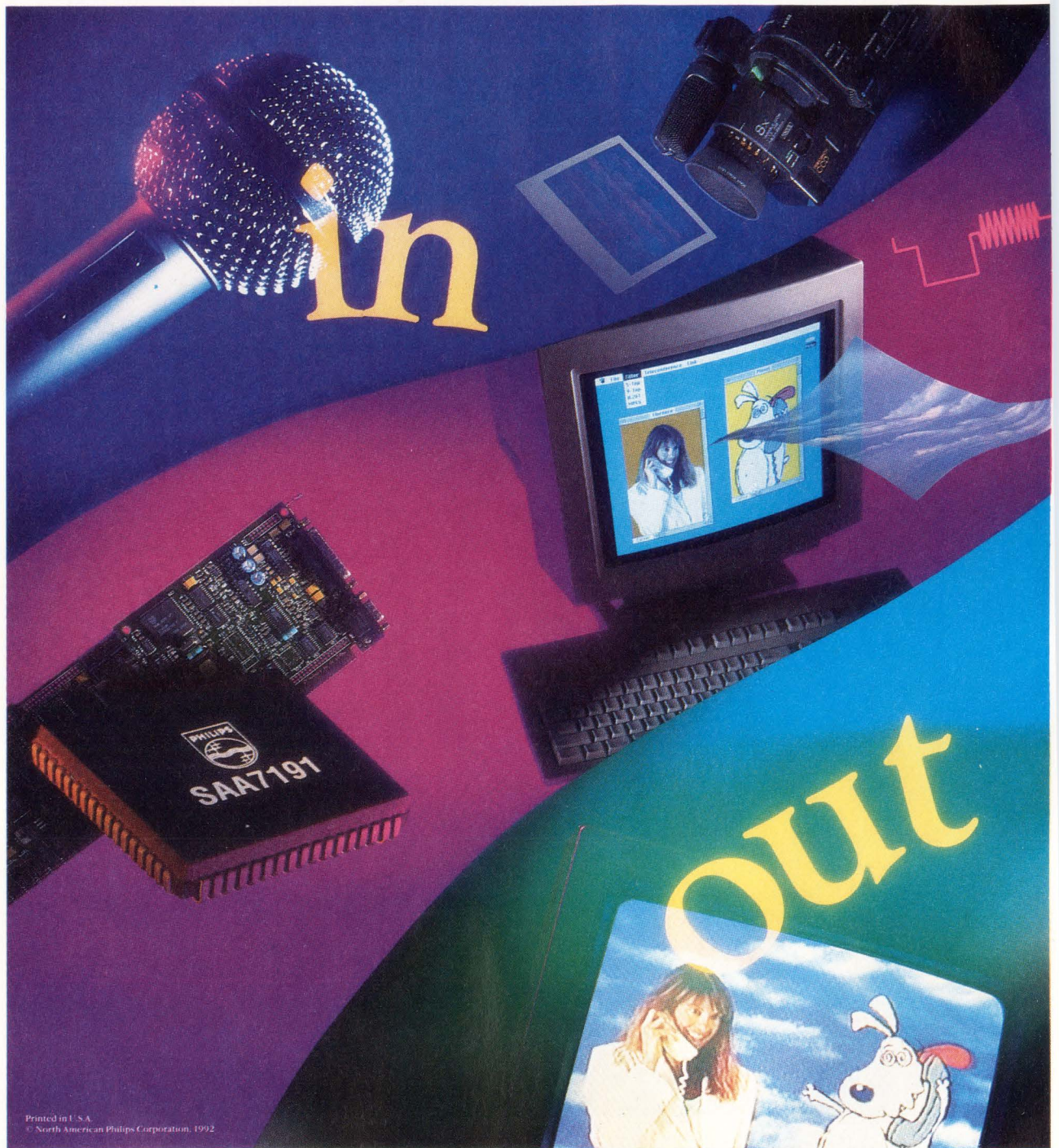
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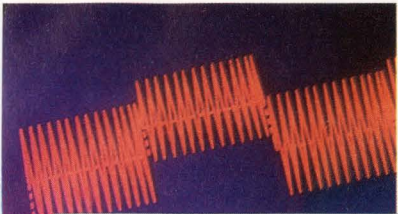


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		TDA8425 Audio Control	TDA7052A 1W Power Amp w/ Volume Control
		TDA1215 Digital Audio Input Output	TDA1519 2 x 10W Power Amp
Video	TDA8708 Video A/D with Clamp and AGC	SAA7192A Digital Color Space Converter	SAA9065 Video Triple D/A with features
	SAA9051 7-Bit Digital Color Decoder	SAA7186 Digital Video Scaler	SAA7199B Digital Video Color Encoder
	SAA7151B 8-Bit Digital Color Decoder		SAA7169 Video Triple 9-Bit D/A
	SAA7191B 8-Bit Digital Color Decoder		TDA8702 Video 8-Bit D/A

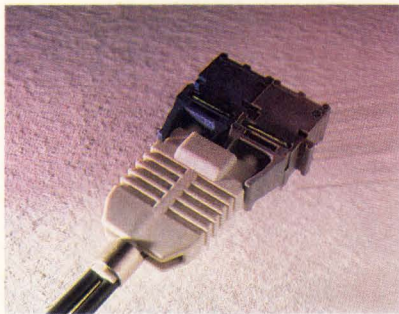
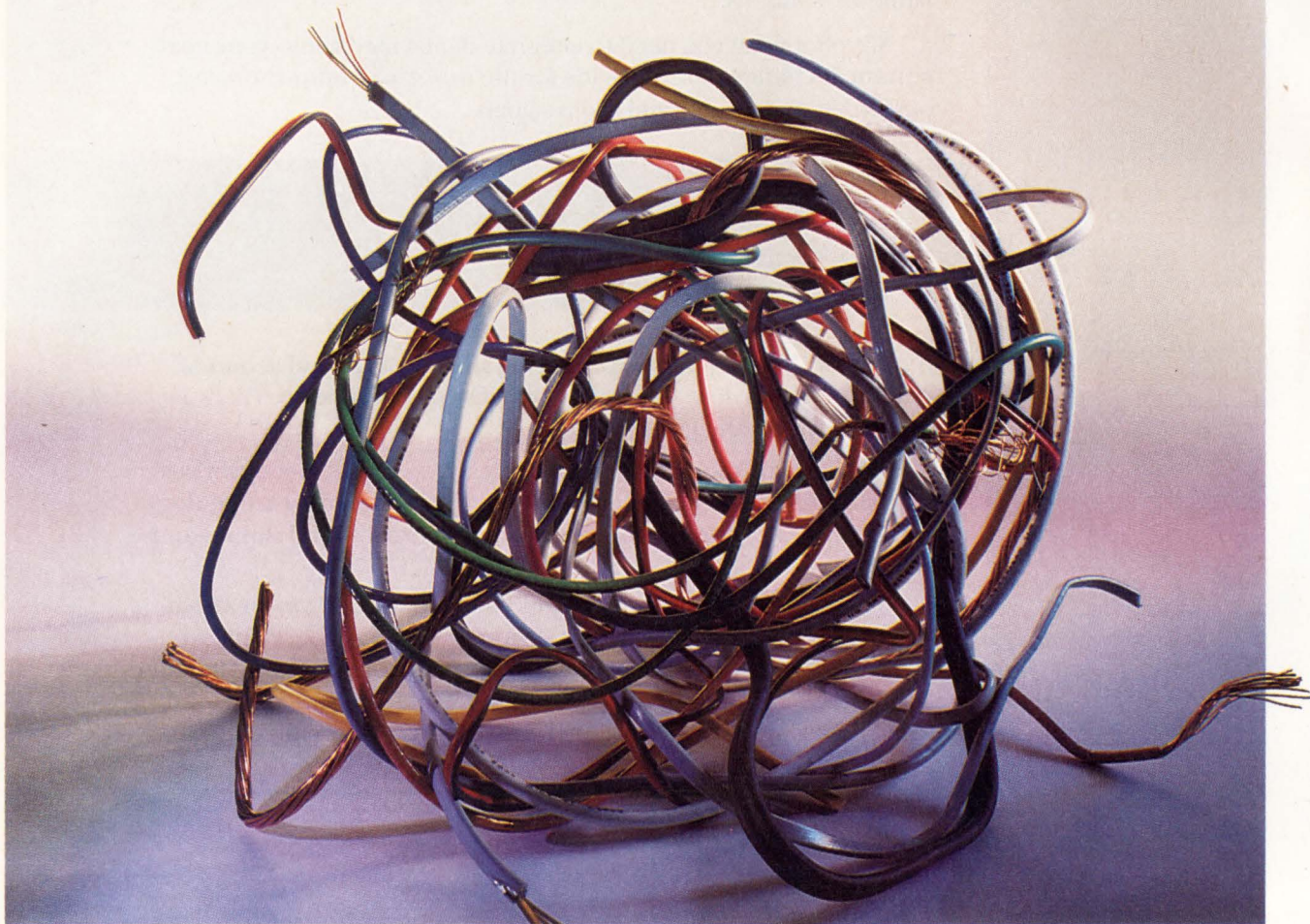
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Speedy FPGAs suit 50- to 60-MHz systems

Xilinx doubled the maximum speed of its XC3000 family of field-programmable gate arrays (FPGAs) to create the XC3100 logic family. The substantial speed increase was made possible by changing from a 1.0- to a 0.8- μ m process and optimizing the internal circuit design. The significance of this speed improvement is that the new FPGAs have sufficient speed to operate in systems with 50- to 60-MHz clock rates.

Because the family is functionally identical to the previous logic family, you can upgrade synchronous designs by just dropping in the new part and raising the clock rate. Designers already familiar with the older family can use the new parts without having to learn a new architecture or new tools.

A typical 3-logic-level circuit can perform the operations of an 8-bit magnitude compare or a 16-bit add in 17.4 nsec; a maximum clock rate of 57.5 MHz. A 1-of-8 decoder function equivalent to a 74138 takes 13.6 nsec. For an 8-bit register, the setup time is 4.3 nsec, and the clock-to-output time is 8.8 nsec. Simple logic functions can operate in excess of 100 MHz.

The five members of the XC3100 family range from 1300 to 5000 usable gates and are available now. Pricing for the highest speed parts with 2.7-nsec internal block delays range from \$31.15 for the 1300-gate XC3120-3 to \$162.65 (100) for the 5000-gate XC3190-3. Xilinx Inc, San Jose, CA, (408) 559-7778, FAX (408) 559-7114.—by Doug Conner

One-stop shopping for component information

Lack of symbols and models often presents a stumbling block to realizing productivity gains from electronic-design automation (EDA) tools. The first step in developing symbols and models is transferring component information from semiconductor manufacturers to EDA vendors for packaging and forwarding to

electronic designers. That flow of information now is often stymied by an 18-month lead-time for printing databooks. Both EDA vendors and their customers must often re-key information from hardcopy sources to develop project libraries.

R R Donnelley & Sons has formed a unit called Viewpoint Information Systems that will supply comprehensive component information in electronic form to product designers. Mentor Graphics Corp has signed on as the first EDA vendor to dis-

tribute the service. The information will include both standard data sheets in electronic form and machine-readable data of three types: CAE logical data, CAD physical data, and parametric data. Now supplied on magnetic tape, component data will be available from customer-sited servers during the first quarter of 1993. The company plans to institute a quarterly service during 1993 that will update information on customer servers by CD-ROM. The information service's products will be available from design-automation tool vendors. Pricing will start at \$300 for data on one component and scale up depending on level of service and usage. Viewpoint Information Systems Inc, Waltham, MA, (617) 466-9100.

—by John C Napier

Serial EEPROMs keep running below 2V

Even as your batteries are delivering the last of their energy, the 93AAxx series of serial EEPROMs from Microchip Technology will continue to operate normally. The devices can read and write data with a supply voltage as low as 1.8V, which corresponds to two series-connected batteries at the end of their usable life. Normal operation includes 1 million read/write cycles per cell, self-timed erase and write commands, and >40-year data retention. The de-

vices come in three sizes: the 93AA46 has 1kbit, the 93AA56 has 2kbits, and the 93AA66 has 4kbits. You can program them to operate with $\times 8$ or $\times 16$ organization. The devices come in 8-pin plastic DIPs or SOICs and have a 3-wire serial interface and chip-select, and device-status signals. Prices range from \$1.35 to \$2.78 (100). Microchip Technology, Chandler, AZ, (602) 786-7200, FAX (602) 899-9210.

—by Richard A Quinnell

ADC families feature serial-I/O interface

National Semiconductor has introduced four ADC families that offer serial-I/O capability, low-power operation, and software configurability. These attributes are especially useful in remote-sensing applications where the ADC is located near the sensor. By having a serial-I/O interface, cabling and isolation networks are simplified. All of the devices have onboard multiplexers with 2, 4, or 8 channels, have software and hardware power-down controls, and come in DIPs and small-outline packages. Most devices operate on a single 5V supply. The ADC1083x family, however, uses $\pm 5V$.

Two families, the ADC-1073x and ADC1083x, provide a 10-bit-plus-sign resolution of either single-ended or differential signals, and offer a conversion

Text continued page 22

Don't be limited by an FPGA's logic capacity

NeoCAD's Prism software tool provides automatic post-mapped partitioning of logic into multiple field-programmable gate arrays (FPGAs). You can create an entire design without regard to whether it will fit in a single FPGA. The software maps the design into the logic blocks that are native to the particular FPGA you are using. After mapping the design into the logic blocks, you enter timing requirements for clock rates and maximum point-to-point delays. The software then determines the fastest overall partitioning for your design.

The importance of postmapped partitioning is that pre-mapped partitioning cannot take into account actual component delays because they are unknown until the design has been mapped into the FPGA's logic blocks. Pre-mapped partitioning also cannot accurately predict routing requirements.

The software is useful for board-level designers who require multiple FPGAs to implement their design, and designers who are using multiple FPGAs for system-level ASIC verification. The first release of Prism works with the Xilinx 3000 FPGA family and is available now for \$6000. The software operates within NeoCAD's FPGA Foundry environment (\$13,000). NeoCAD, Boulder, CO, (303) 442-9121, FAX (303) 442-9124. —by Doug Conner

Text continued from page 21

speed of 5 μ sec. They draw a maximum power of 37 and 59 mW, respectively. Prices begin at \$5.60 (1000). The ADC1203x and ADC12H03x families have a 12-bit-plus-sign resolution and offer a number of programmable characteristics. You can select a device's speed, resolution, and output data format under software control. The devices are self-calibrating, adjusting linearity, zero, and full-scale errors within 1 LSB. The H-series parts convert as fast as 8.6 μ sec, the others as fast as 5.5 μ sec. Prices begin at \$11.16 (1000). National Semiconductor, Santa Clara, CA, (408) 721-5000.

—by Richard A Quinnell

3.3V SRAMs offer 20-nsec speed

Joining the ranks of 3.3V-memory suppliers, Integrated Device Technology (IDT) has introduced a 32k \times 8-bit static RAM (SRAM). The introduction is part of an industry-wide move toward low-voltage ICs that is occurring in two waves. The first-wave parts were often recharacterized 5V parts that sacrificed speed to obtain a lower operating voltage. The second-wave parts use new design and processing techniques to recover that lost speed. The IDT SRAM is part of that second wave.

The device (IDT-

713256SL) operates at 3.3V \pm 10% and meets the I/O specifications of the JEDEC linear-variable TTL standard. It draws a maximum of 500 μ A in standby mode, helping conserve power in battery-operated systems. It will also retain its data with a supply voltage as low as 2V for further power conservation. The device's access time is 20 nsec, with 25- and 30-nsec speed grades available. In 28-pin SOJ packages, prices start at \$8.50 (1000). IDT, Santa Clara, CA, (408) 727-6116, FAX (408) 492-8674.

—by Richard A Quinnell

Windows offered for consumer-level embedded applications

Microsoft is unleashing Windows on consumer-level embedded applications with a product called Modular Windows. The software is based on the company's Windows 3.1 operating-system shell and the underlying DOS operating system. The software runs on 80386-based systems and requires 1 Mbyte each of ROM and RAM. You can use PC-based Windows software development tools to create Modular Windows applications. The only extra software you'll need to create applications is a \$99 software-development kit.

To create a modular operating environment for specific applications, the company threw out many of

the more general-purpose Windows 3.1 features, such as multiple windowing, printer drivers, and the program manager. The intent was to create a runtime environment that provides device independence for consumer applications. Just as Windows 3.1 makes display and printer variations invisible to the application program, Modular Windows provides a consistent application programming interface for various I/O devices such as a TV screen, keyboard, and joystick.

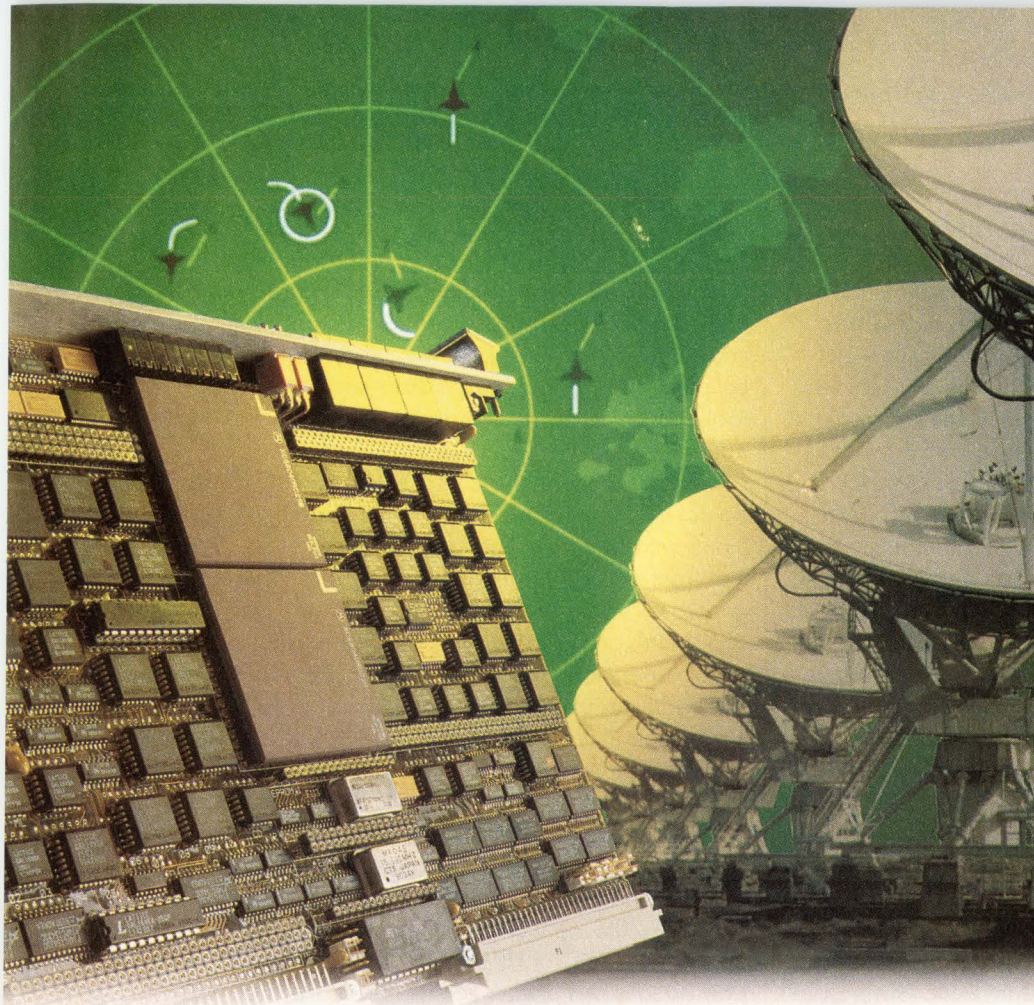
Because the software is intended for high-volume consumer applications, the company will negotiate licenses for Modular Windows on a company-by-company basis. You can purchase a license outright, but the company will also consider royalties on a per-unit and a per-use basis where applicable. Microsoft Corp, Redmond, WA, (206) 882-8080, FAX (206) 936-7329.

—by Steven H Leibson

Programming boosts FPGA speed

Crosspoint Solutions has increased the speed rating on its \$236 (100) (ceramic pin-grid-array version) CP20420 FPGA (field-programmable-gate-array) family without revising its design or processes. Instead, they have developed a programming algorithm that interacts with the FPGA to optimize the on-resistance of each anti-

Text continued page 24



*"Synergy's
dual '040
outperformed all
other boards
I've evaluated in
the last five
years."*

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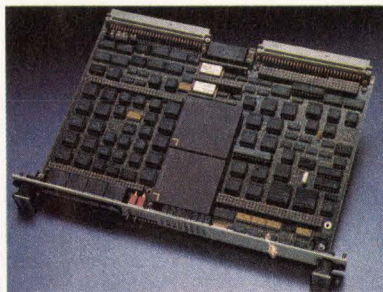
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The Problem:

To get the needed horsepower, sixteen 68040 CPU boards were required. However, with this many boards, VMEbus bandwidth limits would severely degrade system performance making the project unfeasible.

The Solution:

Synergy's V420 dual 68040 SBC. After evaluating several products, KOR Electronics selected eight V420s which could deliver 320 MIPS without VMEbus bandwidth degradation.



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we meet our project
performance goals,
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reduce our costs
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In Synergy, KOR also found a design partner with strong integration expertise and dependable customer support.

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fuse automatically. Programming their FPGA with the new algorithm provides a 30% speed boost for their parts.

By controlling the on-resistance, Crosspoint controls its FPGA's propagation delays. The RC time constant of the antifuse resistance and the load capacitance determines those delays. A tight control on resistance translates in a smaller worst-case timing specification. That effect gets compounded when you consider the cumulative effect of using worst-case timing for each segment of a critical signal. Crosspoint Solutions, Santa Clara, CA, (408) 988-1384, FAX (408) 980-9594.

—by Richard A Quinnell

High-performance disk drives make debut

Two new SCSI-2 disk drives from Digital Equipment Corp provide extremely high data capacity, extremely fast access and transfers, and special features for ensuring data integrity. The 5¼-in. DSP5350 has 3.5 Gbytes of formatted capacity; the 3½-in. DSP3160 has 1.6 Gbytes. The drives come from DEC's OEM Disk Business group, which the company formed last year.

Both drives feature an embedded servo controller, four headers per sector, 264-bit Reed Solomon error-correction code (ECC), and end-to-end er-

ror-detection code (EDC). Average latency is 5.6 msec for both drives; average seek time is 11.5 msec for the 3.5-Gbyte drive and less than 10 msec for the 1.6-Gbyte version. Each drive has a 512-kbyte cache in an implementation that DEC claims is unusually effective at increasing performance and for which the company has applied for patents. Media transfer rates are as high as 5.5 Mbytes/sec for the larger drive and 4.9 Mbytes/sec for the smaller one. Host transfer rates as high as 20 Mbytes/sec are possible.

Mass production of the drives will begin in January; evaluation units are available now. Single-unit price of the 3.5-Gbyte drive is \$3495; the 1.6-Gbyte drive is \$1995. Digital Equipment Corp, Shrewsbury, MA, (508) 841-3111.—by Gary Legg

OEMs can get free IEEE-488 support

IOtech Inc's 488 Club is a free support service for OEM application engineers that provides literature and other information on the IEEE-488 test standard. Members can obtain free loaners of the company's products and can perform beta tests on the company's new products. For more membership information, contact Leo Nurmi. IOtech Inc, 25971 Cannon Rd, Cleveland, OH 44146, (216) 439-4091, FAX (216) 439-4093. —by Susan Rose

Tool automates design-for-test

Mentor Graphic's Flexitest and Fastscan are synthesis tools that give digital-chip designers predictable fault coverage in a fully integrated, top-down design environment when coupled with the company's front-end design tools. Both tools also function as stand-alone automatic-test-pattern-generation (ATPG) products.

Flexitest works on ASIC and full-custom IC designs that do not already include full-scan methodology. When combined with Mentor's Autologic synthesis tools or Idea Station front-end design tools, the software automatically generates test patterns for high coverage of faults for sequential, partial-scan, and full-scan designs with minimal user intervention. The software also lets you use a constraint-driven, partial-scan approach.

Fastscan is a comprehensive ATPG tool for full-scan designs. The software generates test vectors for chips in the 100,000-gate range in less than one hour on a SPARCstation and works on designs with as many as 1 million gates. The software generates 99.9% test coverage, gives self-test analysis, and compresses test vector sets by 50 to 70%, reducing test time. The two tools are available immediately for HP Series 400 and 700 and Sun SPARC workstations. A network license costs less than \$100,000. Mentor Graphics Corp, Wilsonville, OR, (503) 685-7000.

The Test-intelligent Design Series from Cadence Design Systems combines optimizing and synthesizing test with synthesizing logic. Because the tool uses functional logic elements as part of the scan circuitry, it gives you full-scan design without significant area or performance penalties. The software consists of three modules: the Test Synthesizer (\$30,000—also requires HDL/VHDL Synthesizer and Optimizer); the Test Generator (\$50,000); and the Test Simulator (\$45,000). You can also buy the three tools bundled with logic synthesis and the Composer design composition and debug environment for \$175,000.

The Test Synthesizer pattern-generation and fault-simulation tools share a common simulation engine and fault dictionary. For example, you can mix functional and scan vectors. The software uses a rules-based approach, synthesizing and optimizing test constructs (such as redundancy removal, scan-chain distribution, and scan-chain order) in conjunction with logic synthesis. The Test Generator is a combinatorial scan-based automatic-test-pattern-generation (ATPG) tool that accepts the optimized netlist from synthesis and generates up to 100% fault coverage. The Test Simulator generates a testability report combining the coverage generated by the ATPG tool with coverage obtained from design-verification vectors.

The tools run on several Unix-based workstations. Limited production on the three tools begins by the end of 1992 with full production shipment in the first quarter of 1993. Cadence Design Systems Inc, San Jose, CA, (408) 943-1234, FAX (408) 943-0513.—by John C Napier

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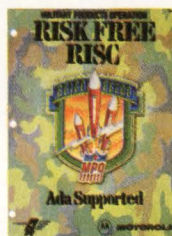
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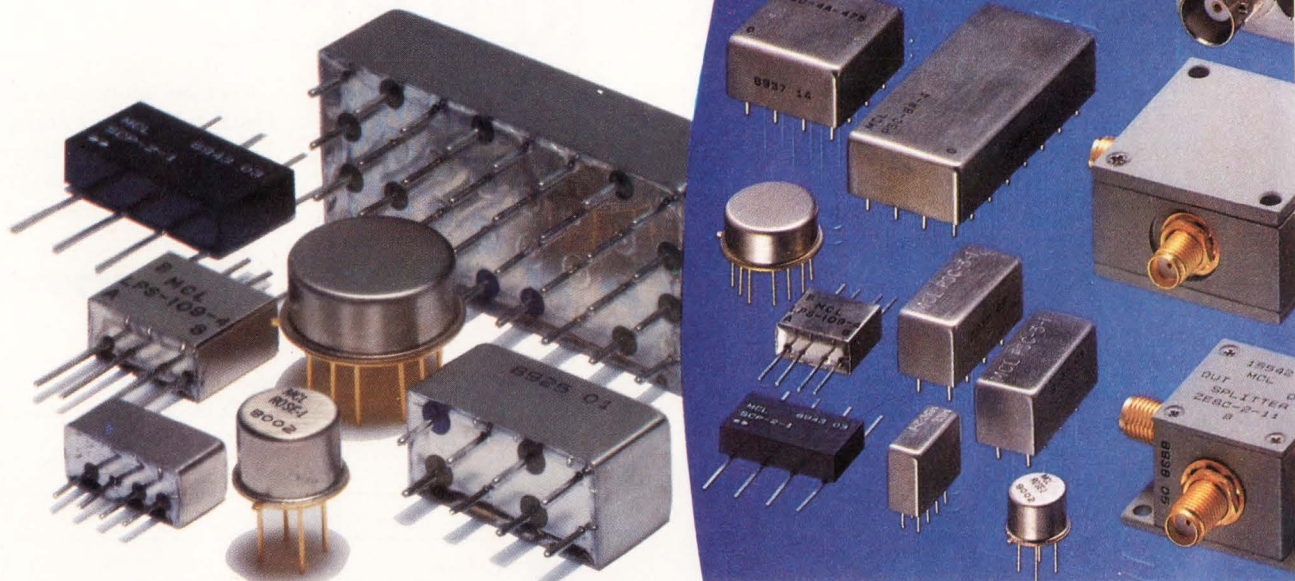
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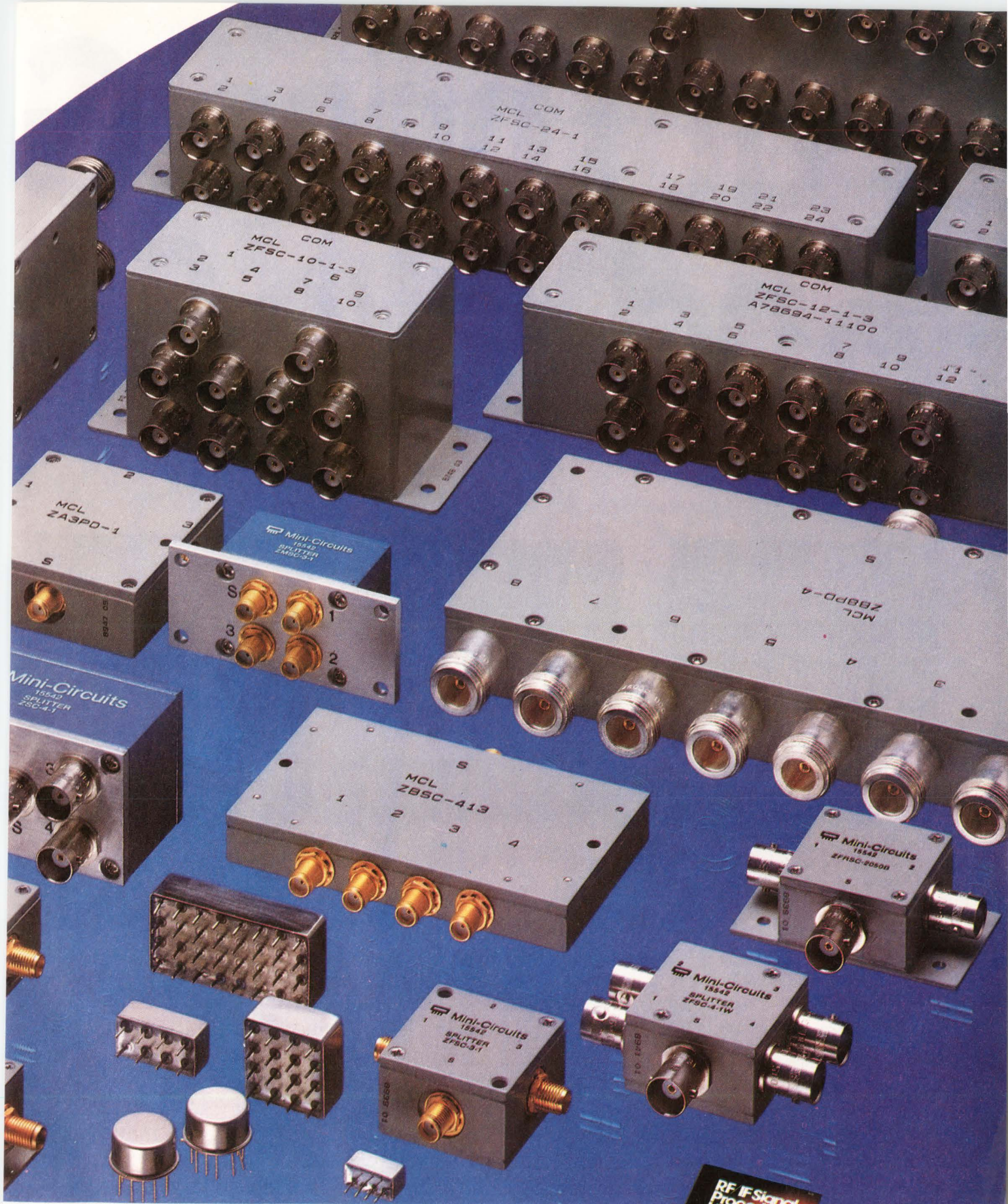
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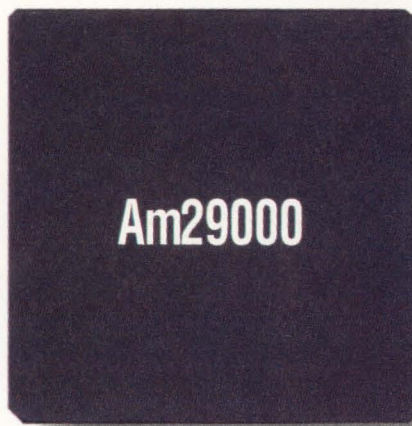


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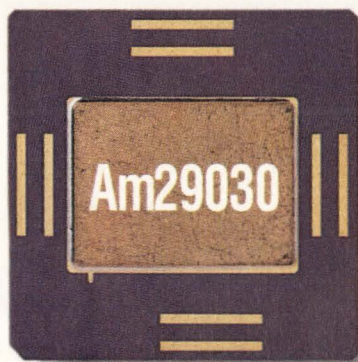
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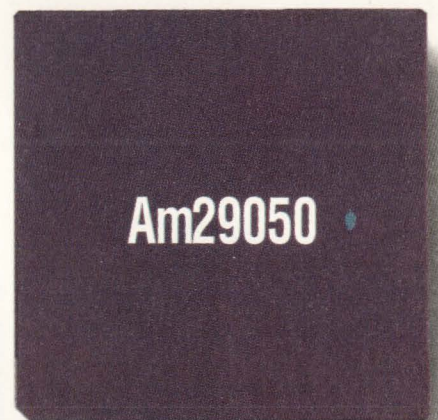
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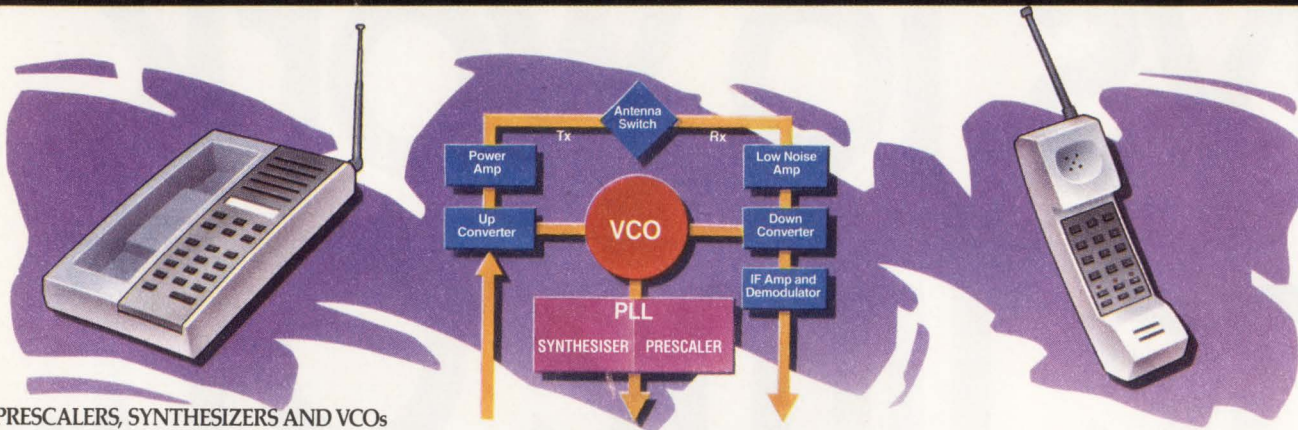
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Motorola Logic



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meet the needs of most designs. In addition, capabilities have been established that enable very quick turnaround for a customized option for those applications not covered in the existing portfolio.

Motorola is expanding the current RF portfolio to include integrated single chip synthesizers. The MC12202 and MC12207 synthesizers provide significant savings in power dissipation, which makes them ideal for hand-held, battery-

operated applications. With Vcc voltage range of 2.7V to 5.5V and currents of 5.0 and 6.5mA, respectively, these devices represent state-of-the-art in one-chip synthesizer design.

Of course, the world of RF does not depend on synthesizers alone. Motorola's current and future efforts include integrated communication VCOs, as well as higher levels of integration for the transmit and receive sections of various wireless applications. A.



HIGH-SPEED SERIAL DATA TRANSMISSION TO KEEP COMMUNICATION CHANNELS OPEN

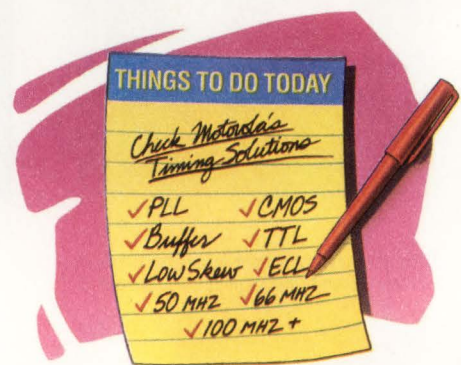
As microprocessor clock rates increase, the job of transferring inter-system data becomes more difficult. So that designers can take full advantage of state-of-the-art processing speeds, data transfer rates must keep pace with rising clock rates. To address these data rate issues for multiprocessor communication, high speed peripheral data transfers and high speed LAN connections, several serial communications standards are currently under development, including Serial Hippi, Fiber Channel, SCI, ATM and proprietary designs. All require high speed serialization and clock recovery ICs. To meet those needs we're applying our experience in high-speed ECL design to the state-of-the-art bipolar processes within Motorola to provide high speed, low power, cost-effective solutions for high speed serial interface applications. Watch for developments. D.



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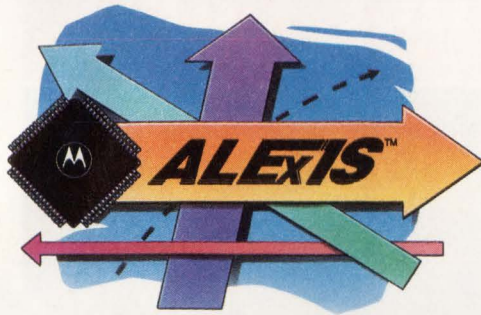
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LOW-SKEW CLOCK DRIVERS FOR PRECISION CONTROL & TIMING OF HIGH SPEED RISC AND CISC DESIGNS

With frequencies routinely hitting 33MHz and nearing 40, 50 and 66MHz and higher in today's CISC and RISC microprocessor systems, well controlled and precise clock signals are a must for a synchronous system. Many microprocessors also require input clock duty cycles close to 50%. Such stringent timing requirements dictate the need for specially designed, low skew clock distribution circuits. Offering a family of CMOS, TTL and ECL clock drivers featuring everything from simple buffers to integrated phase-locked loop devices, Motorola has a solution for every clock driver need—be they low-end 1.5nS skew or high-end 50pS skew devices. F.

Technology Review



BICMOS INTERFACE LOGIC IC MEETS HIGH-SPEED SYSTEM DEMANDS

In response to the performance demands of today's high-speed systems, Motorola offers ALEXIS™ (Advanced Low Power Expandable Interface Solutions), a new family of low-power, high-speed bus interface circuits fabricated with a fully integrated, state-of-the-art BiCMOS process technology designed to yield performance improvements in all applications. Available in buffers, transceivers, latches, registers, parity bus buffers, transceivers and other functions, ALEXIS™ gives circuit designers the freedom to use almost any combination of MOS and bipolar transistors throughout the design. Planned device types include 5V, 5V to 3.3V translators, pure 3.3V and Boundary Scan. **B.**



DYNAMIC BUS SIZER ALLOWS EASY COMMUNICATION TO 8, 16 or 32-BIT PERIPHERALS

Motorola's MC68150 Dynamic Bus Sizer is designed to enhance the 32-bit MC68040/MC68LC040/MC68EC040 bus capabilities allowing communication bi-directionally with 32-, 16- or 8-bit peripherals and memories. It dynamically recognizes the size of the selected peripheral/memory, and then reads or writes the appropriate data to or from that location. Systems using the 68030, which has bus sizing features built in, can now be easily upgraded to the 68040 by incorporating the MC68150. The MC68150 can also be used to separate "fast and slow" buses which would reduce loading on the data bus. The MC68150 is available in a 68-pin PLCC package. **G.**



HIGH-PERFORMANCE GLUE FOR HIGH-PERFORMANCE SYSTEMS

Motorola's ECLinPS Lite™ is an ECL family of single, essential logical primitives—gates, muxes, flops, translators, etc.—housed in a space efficient, cost effective standard 8-lead SOIC. Gates switch in 275ps, edges skew in 225ps, and flops toggle at over 2 GHz, providing designers with the performance necessary for very high speed designs. Superior AC specifications, tight skews and superior isolation combined with a small package size provide ideal solutions for pin cards and other applications that require density, but not at the expense of signal integrity.

For applications requiring a step up in integration without a step down in performance, we offer our standard ECLinPS™ family. Packaged in 28-lead PLCCs, it provides a wide selection of SSI and MSI functions with performance levels well suited to 500MHz-1.0GHz designs. In addition to higher speed performance, the ECLinPS™ family provides significant reduction in power over competing ECL logic families. And because ECLinPS™ is a standard logic family, they are always on the shelf and ready to order.



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Sometimes, a standard family just doesn't quite meet your needs; performance may be right on target but functionality doesn't quite match. For that we offer the ECL300™ LogicArray, which provides ECL functions with performance that rivals that of the ECLinPS™ family, and functionality that is customized to your precise needs. All you have to do is provide us with a block diagram—we'll quickly deliver to you a design prototype.

Even in the highest performance systems there are times when the world slows down to TTL technologies. Motorola offers several devices to interface your high speed ECL portions to the lowest speed TTL sections of your design. Wide high drive buffers are available to drive banks of DRAMs or differential ECL and PECL translating devices for sending those TTL signals across the backplane. And when board space is an issue, ECLinPS Lite™ translators are the answer. **C.**

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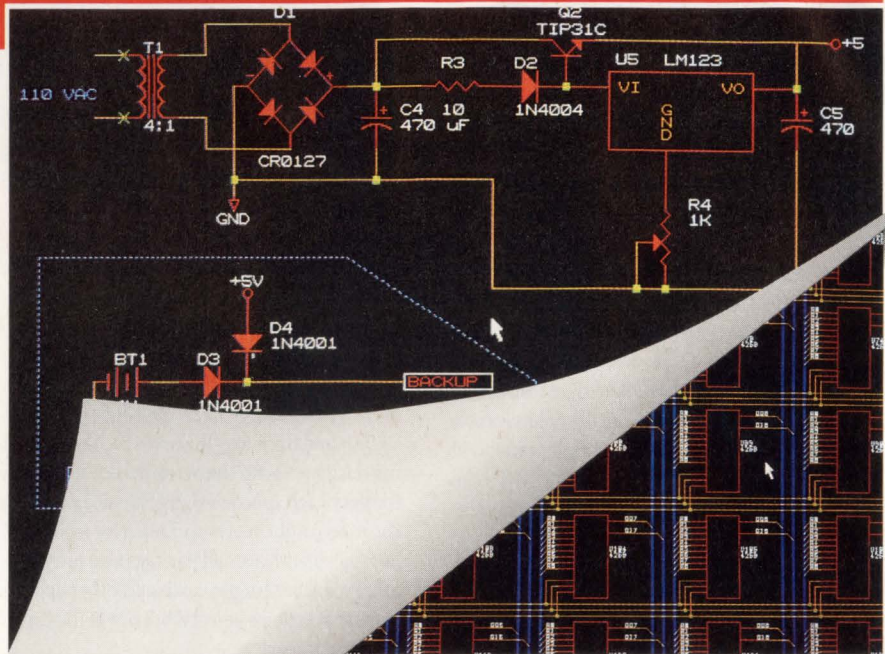
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Preventing aliasing

With reference to Anne Watson Swager's interesting and useful article, "Design software links active-filter performance with real devices" (EDN, April 9, 1992, pg 45), I would like to offer one small, but crucial, correction. On pg 48, she states, "Putting a simple RC filter at the *output* of a switched-capacitor filter is sufficient to remove any clock-feedthrough artifacts and prevent aliasing." This is only half true. It will reduce clock feedthrough; it will not prevent aliasing. The only way to accomplish the latter is to make certain the *input* signal contains no frequency components near the clock frequency. In other words, put an antialiasing filter on the input.

Having performed a number of designs using National's MF-10 and similar parts, I have had ample opportunity to observe the dramatic, and irreversible, effects of aliasing. Once this happens within a sampled data system, further filtering is a lot like locking the barn door, etc However, because the clock frequency and corner frequency are related by either a nominal 50:1 or 100:1 ratio, it is not difficult to control the problem with a simple RC network at the input to the switched-capacitor device.

*Thomas I Kirkpatrick
EE Dept Manager
Schilling Development Inc
Davis, CA*

Reader describes "trial by delivery"

After reading Julie Anne Schofield's editorial on the apparent lack of interest of big component companies in making small quantities of components available to engineers (EDN, March 16, 1992, pg 33), I'm reminded of another situation I constantly find myself in.

We bid on many projects in a short period of time. To bid accu-

ately on these projects, it's necessary to obtain current price and delivery on components that were quoted on days earlier. Delivery is more important than cost in many instances. The components that were in stock when an RFQ (request for quotation) was submitted to a distributor a few weeks earlier, may have been sold as soon as a few minutes later, requiring the distributor to go to the factory for delivery.

Delivery may now be unacceptable to meet our required delivery date to our customer. It would appear that many of the distributors of electronic components only want to process RFQs for pending orders, and in many instances, ignore the RFQs that have been submitted, viewing them as a nuisance. When contacted regarding their lack of response, the reply in many cases has been, in essence, when are we going to get an order for the last RFQ we bid on?

Small quantities also add to this dilemma. If we have to deal with distributors who are reluctant to supply small quantities, we are forced to find someone else who will.

I understand the predicament the distributors are in. Many have reduced work forces due to economic reasons and need to use these resources wisely to generate income. On the other hand, if our company doesn't bid on RFQs sent to us, we will never have any customers.

The only parties in this vicious circle who have the power to correct this problem are obviously the distributors. After working hard to make our business grow despite the attitudes of the distributors, we will remember the ones who were there for us when we were small.

*Daniel R Mattis
Product Development Engineer
Valtronics Engineering &
Manufacturing Inc
Glendale, AZ*

A national health-care system is workable

Characterizing a national health-care administration as a control system to argue against the implementation of one does a disservice to everyone. Mike Harris's argument (EDN, May 21, 1992, pg 29) states that it would be impossible to write state equations for such a system, (and, therefore, such a scheme should be rejected). He ignores the argument that the present system of health-care delivery is the same type of system with different inputs and feedback paths.

For the average American, our system of health care works badly now, judged by objective results compared with results elsewhere where national health plans are in effect. Federally administered health-care systems in many of the Western nations produce greater average longevity, lower infant-mortality rates, and a higher standard of minimum health care, and they cost less than does free-enterprise medicine in this country. The average citizen of Canada or France or Sweden lives longer than we do, and their children are more likely to grow up. Unless, of course, your employer buys comprehensive health insurance for you. Then you live longer than the average [US citizen] and your children are more likely to survive.

We have a 2-tier society here in the USA in that two-thirds of us receive first-world medicine and the remainder get second- or third-world care.

President Reagan did a disservice by propagandizing against government and persuading many citizens that government is bad. Governmental administration is necessary to regulate and provide essential services.

*Robert E Elcox, Engineer
Active Systems
Afton, VA*

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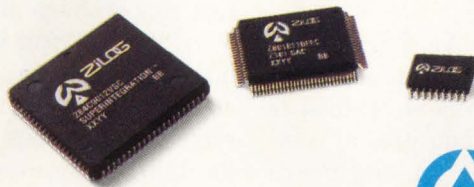
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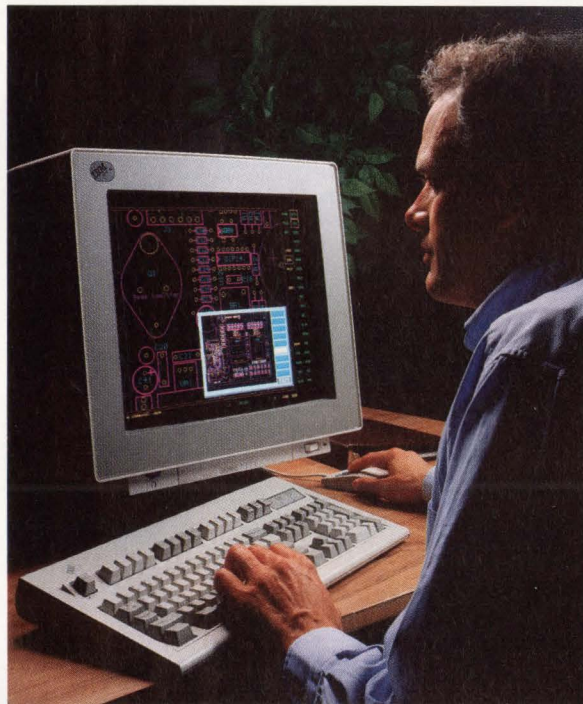
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When the chips are down, the finger pointing starts.

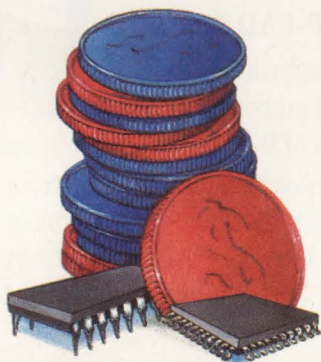


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Reader's curiosity piqued by oscilloscope constant

It is not unusual to see oscilloscope literature stating that the rise-time-bandwidth product equals 350. Thus, knowing the oscilloscope bandwidth in megahertz, one can determine the rise time in nanoseconds and vice versa.

I would appreciate knowing how the 350 constant is derived in this oscilloscope rise-time-bandwidth equation.

*Denis Harrington
Tegspec
Cape Canaveral, FL*

John Rettig of Tektronix (Beaverton, OR) responds: The relationship between bandwidth and rise time is derived from the response of a single-pole RC circuit. The 3-dB bandwidth of a single-pole RC circuit is

$$\text{bandwidth} = 1/(2\pi RC). \quad \text{Eq 1}$$

The voltage vs time relationship is

$$V_{\text{OUT}} = V_{\text{IN}}(1 - e^{-t/RC}). \quad \text{Eq 2}$$

Solving for the 10 to 90% rise time (t_R) in Eq 2 yields $t_R = 2.2RC$. Substituting the result into Eq 1 yields

$$\text{bandwidth} = 0.35/t_R.$$

This relationship assumes that a single-pole RC circuit dominates the system's response; the equation becomes a poorer approximation as the circuit's response moves away from the single-pole situation. For example, the relationship is not a good approximation for an underdamped system with more than 4% overshoot.

Motorola freeware available via computer bulletin board

In the July 6, 1992, European edition of EDN Magazine, the story on fuzzy logic mentioned that freeware was available for downloading from the Motorola computer bulletin board. The phone number was the only additional bit of information about this service. Could you provide more information about the Motorola BBS and how to use it?

*Manuel Vaz Guedes
DEEC
Porto, Portugal*

First, you need a computer, a modem, and a reliable communications program. To access Motorola's DSP computer bulletin board, phone (512) 440-3771 (or (512) 440-3772 if you have a V.22 modem) using modem settings 8,N,1. Once your computer connects, just follow the menu choices.

Most computer bulletin boards run on PCs or Macintoshes, but Motorola uses a rare program that runs under Unix on a VMEbus system. This program has a rather difficult user interface, so be patient.

"Why was my company left out?"

In your May 7, 1992, column, Mr Yves Ephraim of Cable and Wireless, Antigua, West Indies, asked where he could purchase a C compiler that produces Z80 code. Our firm designs and produces such compilers.

Why weren't we included in your response to this inquiry?

*John Dalton
Executive Vice President
2500ADSoftware Inc
Buena Vista, CO*

In our response, we said that the companies that offer C compilers for the Z80 include all the cross-compiler companies, which are too numerous to list in an Ask EDN column. We decided to include three companies as examples to give readers a starting point.

However, we can't always print the names of all the companies that make, for example, a hard-to-find product because we don't have the resources to do an exhaustive search. That's where readers come in. They've identified many companies—both large and small, advertisers and nonadvertisers—that offer just the device or service a reader was looking for.

For the record, 2500ADSoftware's C compiler for the Z80 comes with an assembler, linker, librarian, and simulator/debugger. The compiler costs \$700 for 16-bit systems running MS-DOS and \$650 for 32-bit DOS systems. You can contact the company at

2500ADSoftware Inc
1 2500AD Pkwy
109 Brookdale Ave
Buena Vista, CA 91211
(800) 843-8144; (719) 395-8683
FAX (719) 395-8206.

Readers comb libraries, find manuals

In the June 4, 1992, Ask EDN, we printed a letter from Robert E Bober, who was looking for a manual for the Intel Prompt 48—a box for programming and emulating the MCS 48 family of microcontrollers. We'd like to thank the two readers that found schematics, manuals, and various other reference goodies for the Intel Prompt 48. The first reader is Chip Calton of Tracor Aerospace Inc (Austin, TX); the second works in Washington, DC, but prefers to remain anonymous. If anyone else wants copies of this material, drop Ask EDN a line.

Keep warm at night with a vacuum-tube radio

I have a comment to pass on to your Alaskan reader, Pierre Lonewolf, who was looking for a good AM radio (July 6, 1992, Ask EDN). I have used a number of good communications receivers, but the best AM radio I have ever seen is my old Zenith S-17366 tube type, circa 1950.

I lived in Nashua, New Hampshire, as a kid and did AM dxing (long-distance listening). My log extends to some 300-plus stations including WBAP in Fort Worth and WGN in Chicago. I could also peg some Mexican and Canadian stations, as well as some skip from Deutsche Welle and Britain. As a bonus, if you pull off the back cover, tube radios provide light and heat for those long, dark Alaskan nights.

*Rick Desmarais
Project Manager
Teletrol Systems Inc
Manchester, NH*

Ask EDN solves nagging design problems and answers difficult questions. Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS. Or send us a letter on EDN's bulletin-board system at (617) 558-4241: From the Main System Menu, enter SS/ASK_EDN and select W to write us a letter.

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Our hard drive solution features the first all-CMOS read channel ICs, fabricated with AT&T's advanced, low-power 0.9 μm drawn mixed-mode CMOS process.

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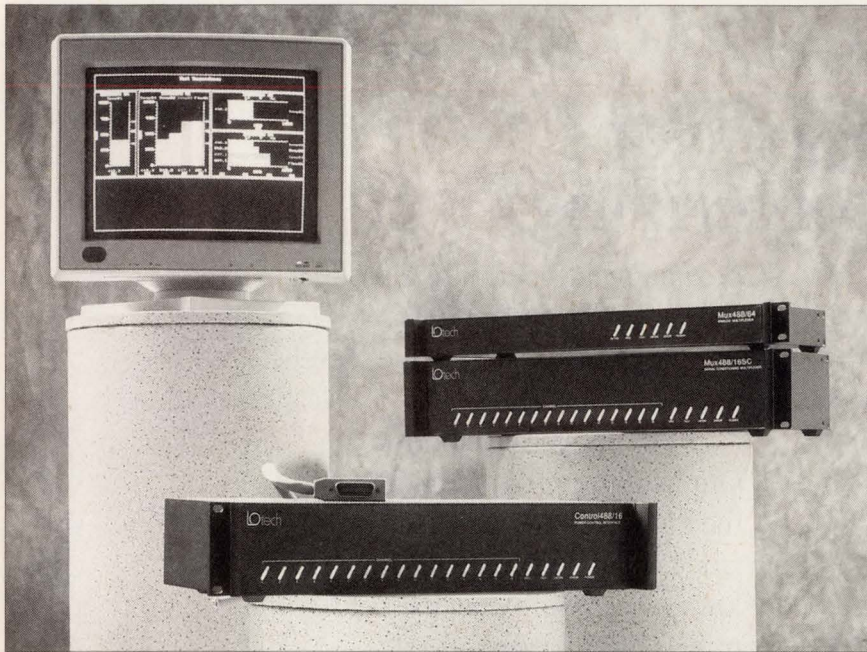
The chip set is supported by evaluation kits, which provide both a hardware and a software platform on which to build a prototype disk drive, as well as a fast means of evaluating the devices.

To get the evaluation kit, along with complete technical information on AT&T's 3-chip disk drive solution, just give AT&T Microelectronics a call at 1 800 372-2447, ext. 908.



AT&T
Microelectronics

New Switch Family for IEEE 488, RS-232, and PC-based Systems



Iotech's new switch family provides switching for a wide variety of signals

Iotech's new family of programmable switches accommodates a wide range of signals, from low-level thermocouple signals to 280 VAC signals. These products can be used as stand-alone programmable switches or as multiplexing front-ends to DVMs, data loggers, PC plug-in A/D converter boards, and Iotech's own ADC488 series of A/D converters.

These new switches offer three means of computer control, making them useful for a variety of applications. They are available with IEEE 488 and RS-232 interfaces, and with a parallel 8-bit digital interface for control directly from a PC's parallel port or from any digital I/O port.

High Channel Capacity. For applications that involve switching signals up to $\pm 10V$, the Mux488/64 can switch up to 64 inputs for output to an A/D converter. For applications requiring greater switching capacity, multiple units can be connected in a master-slave configuration, providing switching for as many as 1024 channels. The Mux488/64 also features a time-base and trigger source that enables it to automatically scan selected groups of signals at rates up to 4 kHz, and trigger an A/D converter after each signal is switched.

Signal Conditioning. For applications that involve thermocouples, RTDs, strain gages, or other low-level signals, the Mux488/16SC provides up to 16 input channels, each of which is isolated by 500V from

the other channels and from the IEEE 488 bus. Each input is converted into a 0 to 5V linearized and compensated output for switching to an external A/D converter. The Mux488/16SC can concurrently output converted signals from all 16 channels or can multiplex them for output on 1, 2, or 4 channels. Multiple units can be connected in a master-slave configuration to switch as many as 256 channels. The Mux488/16SC offers a screw-terminal block that accepts transducer wires and has cold-junction sensors for thermocouple measurements.

High Voltage Switching. For high-voltage or high-current switching applications, the Control488/16 accommodates a wide range of user-configurable switches. Each of the Control488/16's switches is isolated by 500V from the other switches and from the IEEE 488 bus, and can accommodate DC and AC voltages up to 280V RMS, and DC and AC currents up to 3A. The Control488/16 provides two terminals for each switch and a convenient quick-disconnect, screw-terminal rear panel board with built-in strain relief.

Pricing. The Mux488/64, Mux488/16SC, and Control488/16 are all available from stock and are priced from \$595 to \$1,195. Transducer-conversion modules are extra. **For more information, call Iotech at (216) 439-4091, or fax your request to (216) 439-4093.**

CIRCLE NO. 85

Electrical Contacts in Product Design (short course), Madison, WI. University of Wisconsin, Madison, Engineering Registration, Wisconsin Center, 702 Langdon St, Madison, WI 53706. Phone (800) 462-0876; (608) 262-1299. FAX (608) 263-3160. November 16 to 18.

International Security Systems Symposium and Exhibition, Washington, DC. ISSS Expo 92, EJ Krause & Associates, 7315 Wisconsin Ave, Bethesda, MD 20814. Phone (301) 986-7800, ext 24. FAX (301) 986-4538. November 16 to 18.

Reliability: A Practical Approach (short course), San Diego, CA. Continuing Engineering Education Program, The George Washington University, Washington, DC 20052. Phone (800) 424-9773; (202) 994-2337. FAX (202) 872-0645. November 16 to 19.

Comdex/Fall '92, Las Vegas, NV. The Interface Group, 300 First Ave, Needham, MA 02194. Phone (617) 449-6600. FAX (617) 444-4806. TLX 174273. November 16 to 20.

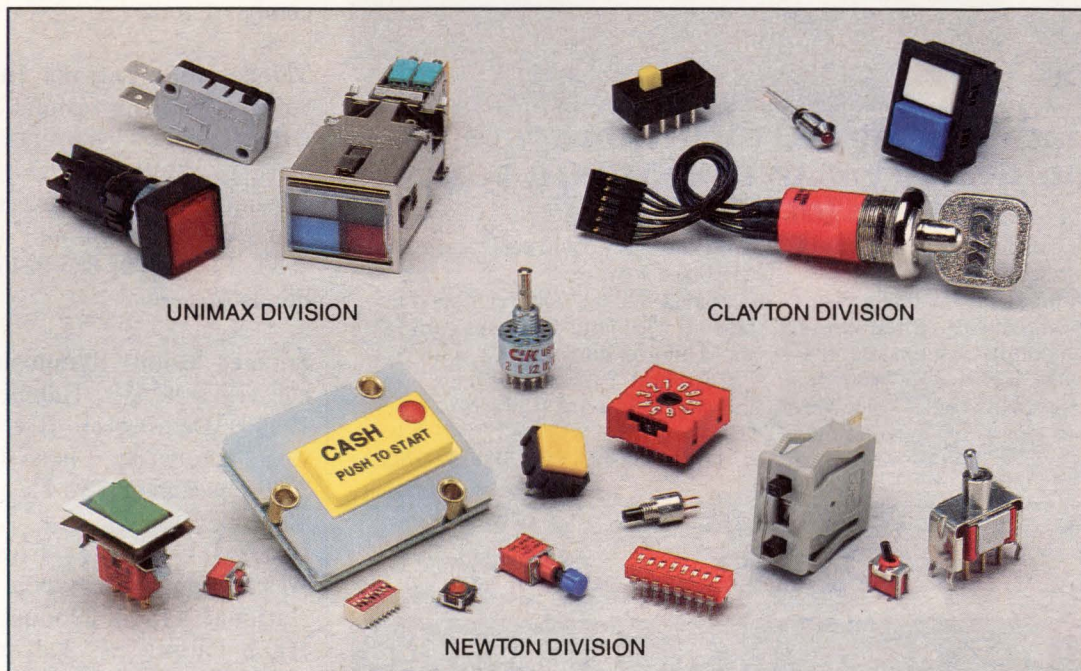
Electrosafe 1992: European Conference on Electrical Safety in the Workplace, Luxembourg. IEE Conference Services, Savoy Pl, London WC2R OBL, UK. FAX (071) 497-3633. November 17 to 18.

International Conference on Metering Apparatus and Tariffs for Electricity Supply, Glasgow, Scotland. Secretariat, Conference Services, IEE, Savoy Pl, London WC2R OBL, UK. Phone (071) 240-1871, ext 222. FAX (071) 240-7735. TLX 261176. November 17 to 19.

Asian Test Symposium, Hiroshima, Japan. Camie deHollan, LTX Corp, LTX Park at University Ave, Westwood, MA 02090. Phone (617) 461-1000. FAX (617) 461-0993. November 26 to 27.

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Flat Information Displays Conference, Exhibition, and Tutorial, Santa Clara, CA. Information Associates, 1259 El Camino Real #231, Menlo Park, CA 94025. Phone (415) 322-0247. FAX (415) 322-0469. December 1 to 3.

Telecommunications Infrastructure Planning (short course), Orlando, FL. Conferences and Institutes, 208 Van Doren Hall, Washington State University, Pullman, WA 99164. Phone (509) 335-3530. FAX (509) 335-0945. December 1 to 3.

Surface Mount Symposium, various cities in US. Hamilton/Avnet, 10950 Washington Blvd, Culver City, CA 90232. Phone (310) 558-2000. December 7 to 11.

Federal Computer Conference, Washington, DC. Sylvia Griffiths, National Trade Productions Inc, 313 S Patrick St, Alexandria, VA 22314. Phone (800) 638-8510; (703) 683-8500. December 8 to 10.

ACM SIGSOFT Symposium on Software Development Environments, Washington, DC. Ian Thomas, Software Design & Analysis, 444 Castro St, Suite 400, Mountain View, CA 94041. Phone (414) 694-1464. December 9 to 11.

IEEE International Electronic Devices Meeting, San Francisco, CA. Melissa Widerkehr, IEDM, Suite 610, 1545 18th St NW, Washington, DC 20036. Phone (202) 986-1137. FAX (202) 986-1139. December 13 to 16.

Troubleshooting & Maintaining the IBM PC, XT, AT, PS/2 & Compatibles (short course), Seattle, WA. Data-Tech Institute, Box 2429, Clifton, NJ 07015. Phone (201) 478-5400. FAX (201) 478-3344. December 14 to 15.

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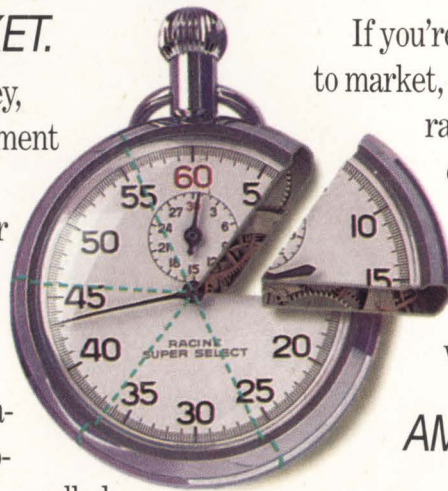
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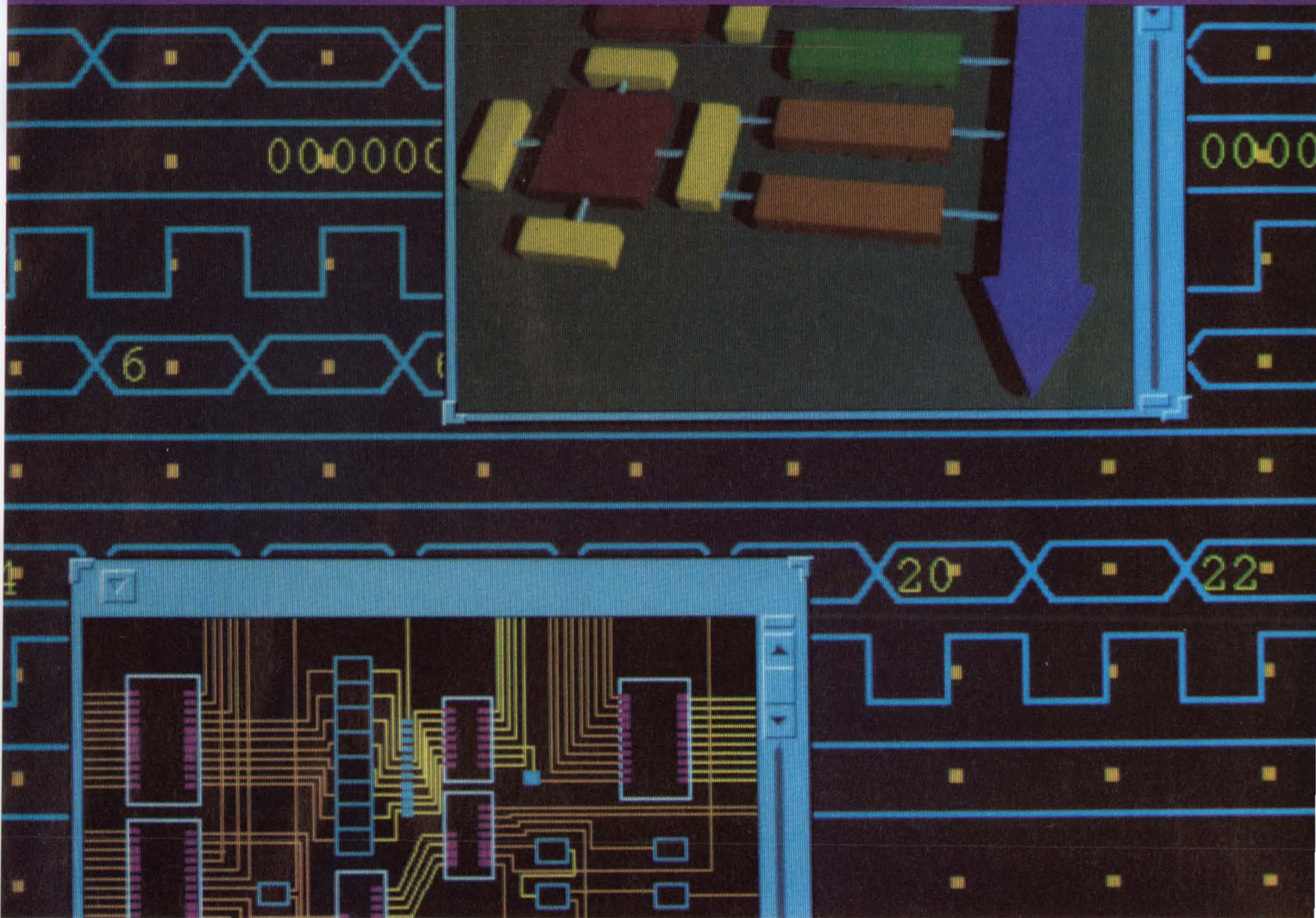
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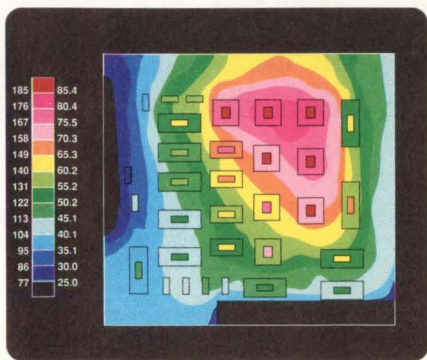
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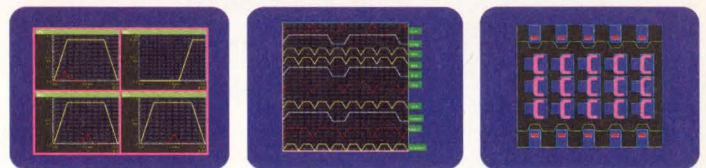
schematic or logic diagram all the way to a valid software first article.

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Placement optimization uses thermal analysis, along with electrical, power, and manufacturing considerations.

(Courtesy of BETAsoft, Dynamic Soft Analysis Inc., Pittsburgh, PA.)



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analog transient noise effects, system impedance, and transmission line layout rules.

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Look to AMP for the help you need to meet tight production schedules and narrow market windows, and the resources you want to move into next-genera-

Complete system architectures include packaging systems, power supplies, and I/O. Developed and manufactured to your requirements.

tion technologies. Our knowledge base in fast boards, high-speed cable assemblies, surface mount technology, and related subjects can simplify the transition to faster logic and smaller form factors.

Custom high-performance cable assemblies represent value-added capabilities in advanced design technologies.

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Your program, and your problems, are unique. Your program is yours alone, but your problems don't have to be. We can help in any of the areas we've listed here.

Or let us put it all together for you, and move you from start to finish. Our specialists can bring our services to you anywhere in the world, and coordinate the AMP resources you need to bring your idea into production. Cost-effectively. And on time.

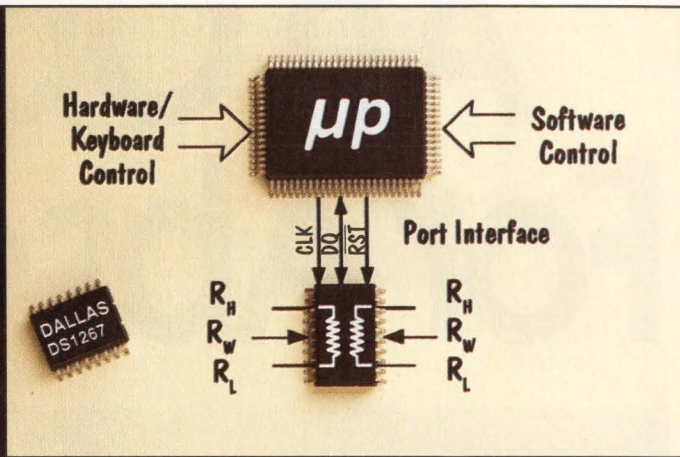
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Manual vs. Automatic



The Potentiometer for Remote Control

So you need to **change** your potentiometer's setting. You know the options with **mechanical** pots. You can fiddle with dials endlessly, or you can **take apart** the system and try to get at the pot with your oversized hands and **that** little munchkin screwdriver.

We've Eliminated the Mechanics

Dallas Semiconductor's digital potentiometers, unlike their mechanical counterparts, can be set remotely. No dials. No screwdrivers. **Resistance** is changed with digital signals using software. So **equipment** can be adjusted in the field without ever opening the enclosure. Which is mighty important when you've got pots in some tight **places** where you may not want to put your hands. Like under **the hood** of your car at 105°C. Or inside test equipment that **measures** the presence of toxic gasses.

Exactitude

Our digital pots **contain** two independent 256-position pots. You write two 8-bit words **through** a serial port to an on-chip register. That number is **stored** in a read/write memory and the setting is read electronically. **So it** is exactly what you want it to be.

Change Settings Fast

Chances are if your **system** has one pot, it has a bunch. Even if you can find them all, **changing** them within a reasonable amount of time is a losing **proposition**. Dallas Semiconductor's digital pots can be **ganged** together to create arrays that can be addressed as one device with **no external** logic or components. Updating system parameters and **making** calibrations takes less than a second—even if you've got **20** pots to update.

No Noise

We spec'd our potentiometers quieter than -120 dB — about the noise of a **thermal** transistor. Because all electronics **remain** on the card, you don't have to run wires out to dials **on** the surface of the equipment, which eliminates **that** source of noise.

In addition, our digital pots don't have to stop at every setting along the way — they can hop directly to the resistance you choose. Once the setting has been made, there is no activity in the chip to cause noise.

And all these features come in a package that is surface-mountable.

MEET THE FAMILY

Two Pots in One Package

The DS1267 Dual Digital Potentiometer helps you minimize board space consumption by offering two pots in a single package. The pots can be used separately or tied together and addressed as one 512-position pot.



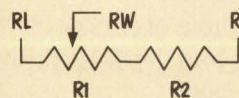
Pots Plus Op Amps



The DS1667 Dual Digital Potentiometer Plus Op Amps adds two op amps to create a variety of gain stages. The op amps contain both inverting and non-inverting inputs, and can be used independently of the resistors.

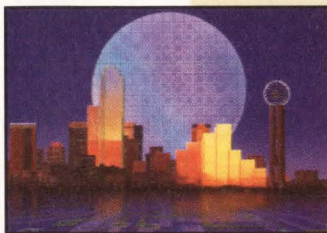
Audio Resistor

For audio and logarithmic applications, the DS1666 Audio Digital Resistor is a 128-position audio taper potentiometer with two degrees of resolution in one package. With digital audio control, sound cards for personal computers can control frequency



amplification from a screen. Studio recording equipment settings can be set by, stored in, and recalled by a computer, so you don't have to remember the positions of 40 slider pots.

So give your wrist a rest. And give us a call.



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Model Number	Equiv. Gates	Macro Cells	Max. Delay	System Speed	I/O Pins	Hard-Wired Option
MACH 110	900	32	12ns	66.7 MHz	44	MASC 110
MACH 210	1800	64	12ns	66.7 MHz	44	MASC 210
MACH 120	1200	48	15ns	50 MHz	68	MASC 120
MACH 220	2400	96	15ns	50 MHz	68	MASC 220
MACH 130	1800	64	15ns	50 MHz	84	MASC 130
MACH 230	3600	128	15ns	50 MHz	84	MASC 230

*In applications with a full 16 product terms. Every MACH part is specified using real-life conditions with all outputs switching.

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Take your tools



On the last weekend in August, my son Chris left home to start college. Before he went, I made sure he had a small toolbox, which included screwdrivers, pliers, cutters, nut drivers, and a hammer. I added a soldering iron and some solder just for fun. Most of his friends were kidding him about the toolbox his Dad was making him take to college. They were worrying about taking their stereo equipment or their new clothes. Tools? Why would you need tools? Chris took the kidding as good fun, but he, too, had doubts about carrying tools to college.

As it turns out, the tools have spent a lot of time being used around the dormitory. Kids have needed desks screwed back together, shelves adjusted, computer cables tightened, bikes repaired, and stereo gear reconnected. The tools were a good investment after all. Chris has met everyone on his dorm floor. After only a day or two, he had people stopping by to chat, and he felt comfortable stopping in to visit with newcomers who had borrowed his tools. The tools were great ice-breakers and very practical. Now there are no jokes about the toolbox, and everyone knows where to find it—and Chris.

We all have tools, and they're not always socket wrenches or screwdrivers. We all have professional skills, but we may also have the ability to play the piano or do card tricks. Some of our skills are practical, while others are just for fun. For the moment, set aside your professional talents and training. The point is that many of your avocational skills or talents give you opportunities to get to know other people, to break

the ice at meetings, to develop relationships, and to have a richer life. In some cases, they can mean the difference between getting into a new job and not.

I used to poke fun at an advertisement for piano lessons that said, "They laughed at me when I sat down to play the piano." The implication was that this poor guy couldn't play and was about to make a fool of himself. But, he had taken music lessons and was about to attract a crowd of listeners. After taking lessons, he had something fun and interesting to offer—something the other people didn't.

As engineers, scientists, and technical people, we often take abuse for being reclusive, introverted, and uninteresting. Nothing could be further from the truth. Most of the technical people I know have interesting sets of talents that they can and do use often. Some of these people raise cats, do landscaping, play bridge, sail boats, cook gourmet meals, go deep-sea fishing, serve in volunteer organizations, and play musical instruments. Some of them enjoy technical hobbies such as photography, repairing old cars, astronomy, and ham radio. In almost all cases, these people aren't solitary enthusiasts. They share their interests and enthusiasm with others, and in doing so they get acquainted with new people and open new friendships.

The key to having talents is sharing them with others, either to help others or just for enjoyment. A long time ago, someone said, "Don't hide your light under a basket. Let your talents shine through." The results might surprise you.

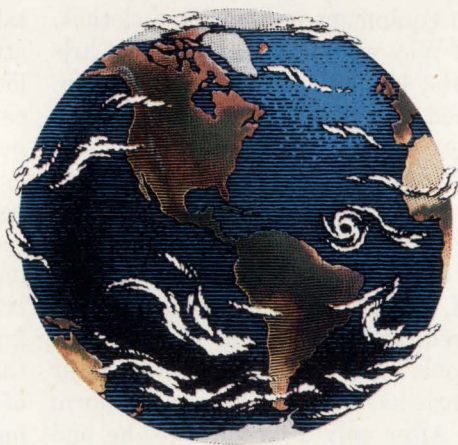


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Jon Titus
Editor

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Comdex/Fall '92 targets technology for multimedia and connectivity

J D MOSLEY, Technical Editor

Two thousand exhibitors and 130,000 attendees will converge in Las Vegas for this bigger-than-ever annual gathering of the computerized faithful.

Harboring more than 2.1 million square feet of exhibit space (at the Las Vegas Convention Center, Sands Expo and Convention Center, Las Vegas Hilton, Bally's Casino, Riviera Hotel, and the Tropicana Hotel), Comdex/Fall '92 will offer five days of computer-based demonstrations and displays in 11,800 booth spaces. The show caters to an international assortment of system integrators, hardware and software vendors, resellers, distributors, corporate decision-makers, and volume buyers. The list of exhibitors is a virtual *Who's Who* among computer manufacturers,

software developers, and peripheral suppliers.

Scheduled for the week before Thanksgiving (Monday, November 16 to Thursday, November 19), Comdex once again overlaps Wescon's show dates. Fortunately for those whose business requires coverage of both shows, nearly two months will separate these exhibitions in 1993, when Wescon moves to September.

Technologies on display

This year, Comdex presents four technology showcases dedicated to network computing, multimedia, imaging applications, and OEM business issues. The showcase exhibit areas include multimedia at Bally's Casino Resort and network computing at the Las Vegas Convention Center and South Annex. New for 1992 are the showcases for OEM business products and for imaging, both located in the Tropicana Hotel.

Three hours of presentations will kick off Comdex/Fall '92 on Monday morning. At 9 am, Philippe Kahn, CEO of Borland International, will deliver the keynote address entitled "Putting the personal back into personal computers." This presentation will introduce ways to integrate dissimilar systems in order to share strategic data, enhance group communication, and create customized applications.

At 10:30 am, the Comdex plenary session will examine the increasing pace of change throughout the computer industry. Dubbed *The Comdex Crystal Ball: Pushing the Envelope*, this session will examine the increasing change of pace in the computer industry as products and users redefine both computers and



Each year, Comdex draws thousands of computer-industry professionals to its show floors to examine emerging products and trends in the industry.

Table 1—Comdex/Fall '92 technical conferences and courses schedule

		Corporate Computing Program	Connectivity Program	New Media Program	Channel Program
Monday November 16	9 to 10 am	Comdex Keynote			
	10:30 am to noon	Comdex Plenary—The Comdex Crystal Ball: Pushing the Envelope			
	12:30 to 1:30 pm	Operating Platform Directions			
	2 to 3:30 pm	Aligning technology and corporate goals Operating-system directions Product suites or sweet products	Connectivity Plenary	New Media Plenary	
	4 to 5:30 pm	Re-engineering: Changing the flow of work The GUI wars Power platforms	Client/Server directions Embedded mail (Beyond E-Mail) Network management Open systems and the user	The basics of multimedia technology The multimedia platforms The impact and effects of consumer technologies	
Tuesday November 17	9 to 10:30 am	Complex data: Managing what counts Does rightsizing mean downsizing? Next-generation technologies	Distributing data The technologies of performance Unix and open systems Directions in mobile computing	Multimedia in action I: Business and sales communications The ABCs of multimedia production PC TV and TV PC: Who will define the standards? Introduction to imaging technology Imaging and databases	Redefining the value quotient The coming of consumer computing technologies OEMs as partners
	11 to 12:30 pm	What is a user interface? Technical support of complexity The technologies of pen computing	Front-line customer systems High-volume network applications Connecting the occasional user Mobile computing case 1: The mobile professional	Multimedia in action II: Training in the workplace The authoring environment Video-game technologies Justifying the value of imaging technology Imaging on the network	
	1 to 2 pm	Platform Directions			
	2:30 to 3:30 pm	CEO Perspective			
Wednesday November 18	9 to 10:30 am	The outsourcing alternative Building with objects Integrating mobile users	Building the enterprise network Migrating to open systems Mobile computing case 2: Routes to success The technologies of mobility	Multimedia in action III: Education—an update PC video production: Authoring and production systems Delivering technology to the home Identifying an imaging application Input and imaging	Getting products to market: The changing channel Selling PCs in a commodity market Value-added OEM technology
	11 to 12:30 pm	Object-oriented systems in the corporation Real-life product evaluations Desktop development tools	Network servers The future of open systems Mobile computing case 3: In the warehouse The mobile user	PC video applications: Conferencing and communications Designing for cost-effective configurations Platform perspectives Cases in desktop imaging Supporting imaging with your current systems	
	1 to 2 pm	Platform Directions			
	2:30 to 3:30 pm	CEO Perspective			
Thursday November 19	9 to 10:30 am	Object-oriented vs relational databases New-age capacity planning The integrated desktop	Network backbones OSI and/or TCP/IP Wireless electronic mail: Mobile's killer application? Connecting anytime, anyplace	Emerging applications and new directions Electronic media Evaluating your implementation options The major issues in imaging	Selling the hot technologies The right product at the right price The art of successful sourcing
	11 to 12:30 pm	Middleware Document engineering and management Desktop SQL programming	Is frame relay the next step? Cross-platform connectivity Managing the mobile network Cellular's "open standard" for mobile data	Document-management reality Imaging—today and tomorrow	

Comdex/Fall '92

computing. By attending this plenary, you'll learn about emerging technologies and what they mean to the computer industry and its customers.

Following the Comdex plenary at 12:30 pm, and recurring on Tuesday and Wednesday at 1 pm, is a new session called Platform Directions. During each of these sessions, senior executives from IBM, Microsoft, and Unix System Laboratories will discuss their operating platform strategies and future directions.

Choose your subject

Simultaneously scheduled from 2 to 3:30 pm are the connectivity plenary and the new media plenary. For those interested in the technologies that connect customers, suppliers, the factory floor, and staff into an integrated business solution, you'll want to attend the plenary entitled "The connected busi-

ness: Directions for the 1990's." The discussions will relate how hardware, software, communications and business needs are converging on a window of applications opportunity and reshaping the art of doing business in the 1990s.

Attendees involved in the areas of multimedia, imaging, and consumer technologies should attend the New Media plenary. Referred to as "The digital revolution," this panel will introduce the new cross-industry and cross-technology alliances that are forming among the computer, consumer electronics, communication, and entertainment industries. Offering a vision of evolving multimedia technologies, this session will consider how the *new media* will change the way people work, educate, train, and entertain themselves by the end of the decade.

CEO perspectives close each pro-

gram at 2:30 pm on Tuesday and Wednesday. Brought back to Comdex by popular demand, these panels assemble leading CEOs who will discuss their views and visions of computing in the '90s.

Beyond these general sessions, the conference consists of four distinct programs covering corporate computing, connectivity, new media, and channels. **Table 1** presents the complete conference schedule and specific presentation topics.

The corporate computing program's theme is "Turning technology into reality." Focusing on business strategies, enabling technologies, and implementation processes, this program will analyze the synergies that provide direction and structure for corporate technical managers.

The connectivity program focuses on "Making the connection." Network computing topics will follow

International Program airs global technology concerns

Sunday, November 15, spotlights the International Program—a distinct block of three single-day conferences. Scheduled from 9 am to 4:30 pm in the Sands Hotel, these three conferences examine business opportunities in Asia, Latin America, and international markets.

Topics included in the presentation of business opportunities in Asia involve understanding Asia's market, how to do business in Asia, hardware and software companies' need for alliances in Asia, marketing in Asia, copyright, and the role of trade boards. Presented by the Southeast Asia Information Technology Organization (SITO) and sponsored by *Asia Computer Weekly*, this conference will include case studies to help create a framework for potential marketing partnerships with Asian producers. As one of the world's largest producers of computer products, Southeast Asia also represents one of the largest markets for computer products and services. Lunch and a cocktail reception are included.

The international marketing forum is sponsored by the Software Publishers Association. Spotlighting northern, southern, and eastern Europe, Latin America, Japan, and a variety of English-speaking markets, this conference examines selected market opportunities

around the globe. Revenue from overseas markets now represents a significant contribution to the bottom line of computer product companies. Accordingly, access to the international marketplace is a critical component for future business plans. Designed for software and hardware marketing professionals, this conference also includes lunch and a cocktail reception.

Latin America is rapidly becoming one of the world's most open markets. Attendees at the Comdex Latin America conference will hear presentations on product and policy trends and projections, exporting and marketing, and identifying the products most in demand. Another discussion will cover methods for successful distribution, partnering, and sourcing. Conference presenters will offer particular insights into the Brazilian and Mexican markets.

To participate in the International Program, you will have to pay an additional \$195 fee for each conference program you decide to attend. The \$450 comprehensive program fee you can pay to participate in the connectivity, corporate computing, new media, and channel programs will not provide admission to any of the international conferences.

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an applied-technology track and an implementation track to lead participants through the intricacies of embedded electronic-mail, distributing data, network management, and the art of building an enterprise network. Open systems topics will examine the issues surrounding interoperability and cross-platform connectivity. The mobile computing sessions will look at case studies that use wireless electronic mail and digital/cellular technologies to create a virtual office for mobile professionals.

Hear the big picture

The new-media program examines multimedia and imaging within tracks that encompass business applications, applied technologies, and planning. The consumer technologies topics contemplate merging markets and technologies, and con-

sider the task of reaching the consumer. With more than 46,000 Comdex/Fall '91 attendees indicating a high interest in multimedia systems and products, this year's conference has responded to that interest with this 30-session conference program. More than 350 companies will exhibit multimedia systems and products this year.

Finally, the channel program will consider how the computer industry is conducting business. Focusing on the sale and purchase of products and the development of partnerships and relationships, this program examines mass merchandising, OEM business, and getting products to market.

During the course of the conference, you can depend upon complimentary shuttle bus service between the various convention sites. Nineteen hotels will also have shut-

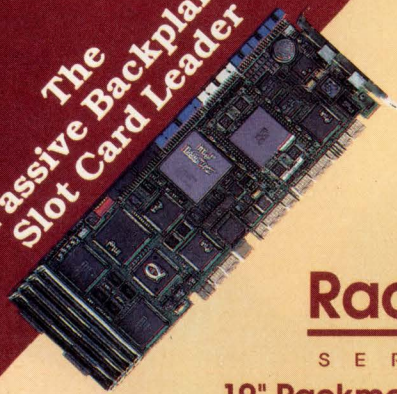
tle service for the convenience of registered show attendees.

The Comdex exhibit areas will open Monday, November 16 at 10:30 am in the Las Vegas Convention Center (LVCC) and at 9 am in Sands Expo Center and other exhibit locations. Tuesday through Friday, the LVCC exhibit hall will open at 10 am. Other exhibit areas will open at 8:30 am. Preregistered attendees can pick up their badges as early as 1 pm on Sunday, November 15, at the LVCC registration area. **EDN**

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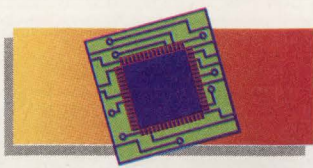
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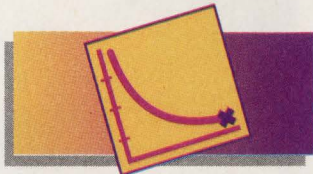
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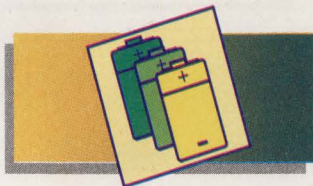
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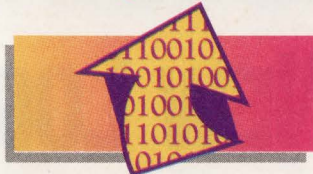
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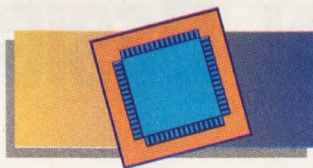
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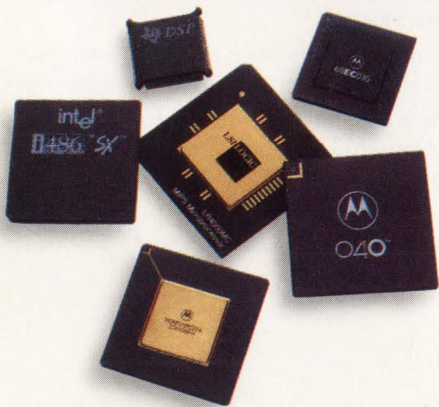
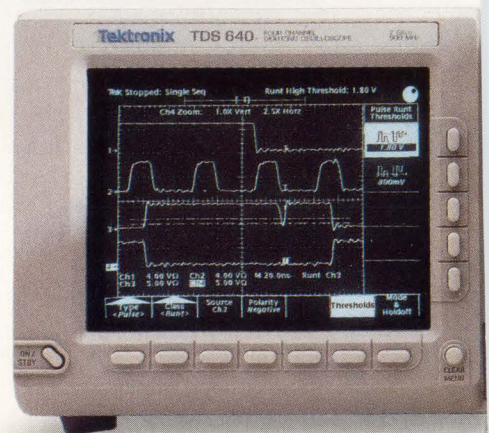
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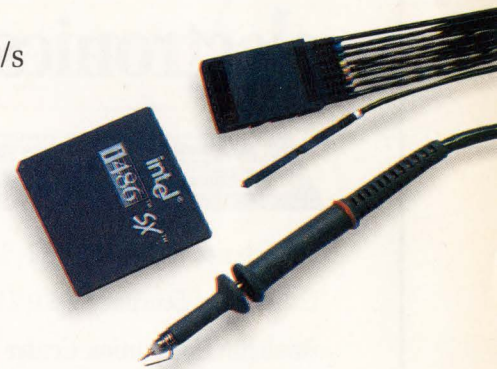


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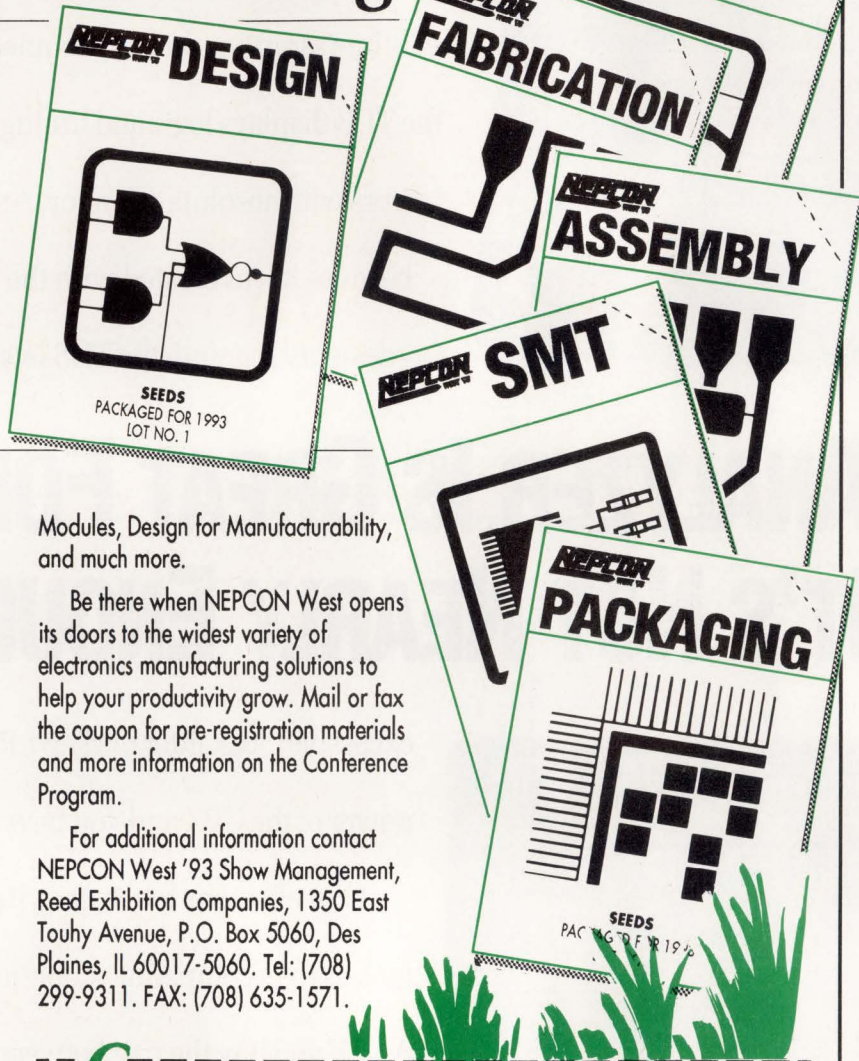
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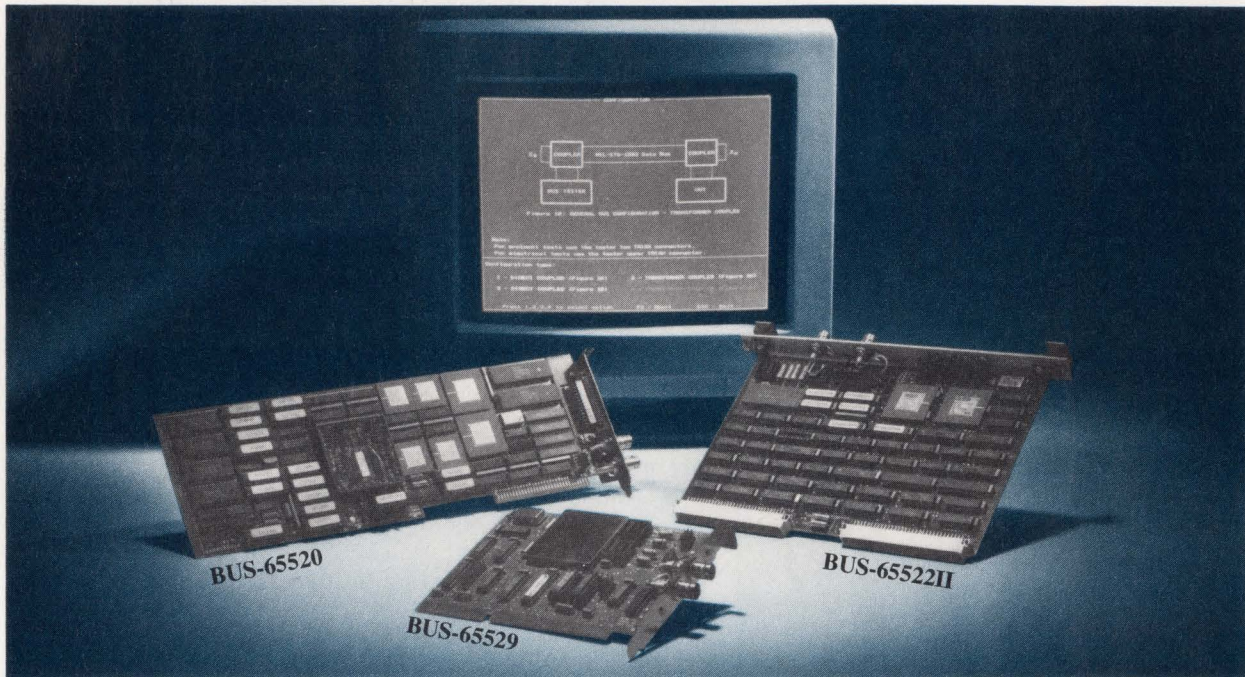
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The **BUS-65520** is a complete 1553 solution. It consists of a full-size IBM-PC MIL-STD-1553B (BUS-65517II "IDEA") interface card, menu software, "C" and Pascal library software, and Validation and Production Test Plan software packages. The BUS-65517II card can simultaneously emulate a Bus Controller(BC), Bus Monitor(MT), and up to 31 Remote Terminals(RTs). The "C" and Pascal Library software allows you to write customized application software. The Production and Validation Test Plan software packages allow you to test a RT in accordance with SAE document AS4112 and section 100 of MIL-HDBK-1553. □

The **BUS-65529** is a 16-bit, half-size IBM PC/AT® MIL-STD-1553 board, which can be a Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT). The board complies with MIL-STD-1553B protocol and has dual redundant bus capabilities. The BUS-65529 is memory mapped, allowing the programmer to write software in any language. All register, memory locations, and bit maps are fully documented for user accessibility. □

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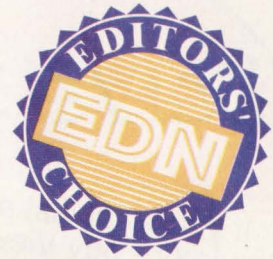
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The **BUS-65522II** VME/VXIbus MIL-STD-1553 board emulates either a MIL-STD-1553 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT). The board is packaged on one double Eurocard-size printed circuit card. Additional features include an on-line built-in loop test, Time Tag counter, software programmable base memory address and RT address. The BUS-65522II supports all dual redundant mode codes and message formats. Its full compliance with MIL-STD-1553B makes it an excellent choice for real-time applications.

For further information, please contact Fabio Stanzini at (516) 567-5600, extension 7206. □

DDC
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ASIC family adds antifuse field programmability to library

VLSI Technology helped develop the amorphous-silicon antifuse technology used in Quicklogic's FPGAs. Now the ASIC vendor has added that technology to its own product line.

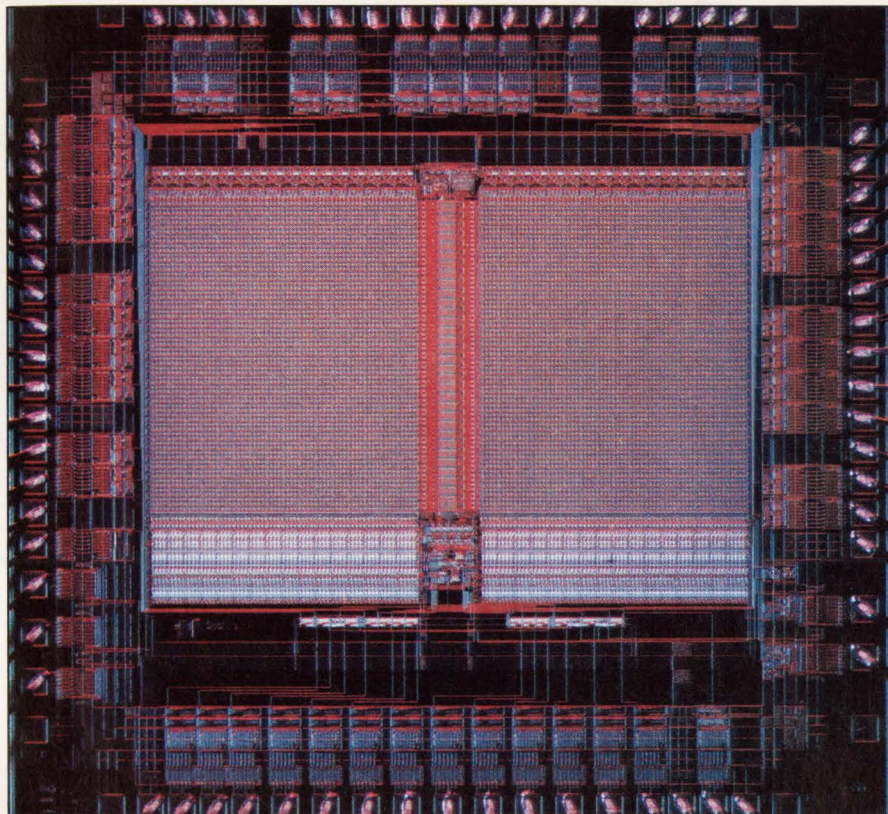
The antifuse starts as a high-resistance ($>2500\text{-M}\Omega$) link between metal layers. It has approximately the same drawn dimension as a standard via. Applying a programming voltage across the link restructures the amorphous silicon, lowering its resistance to $<100\Omega$ and creating a via on demand.

One advantage the antifuse technology provides ASIC designers is that it only affects the space between metal layers; no compromises with the transistor process technology are necessary. Further, the antifuse's density is limited only by metal pitch, so it scales without affecting process shrinks.

The principal advantage, however, is that you can finish customizing your design after the ASIC has been delivered. Designs involving data encryption, for example, can program each ASIC with a unique key. You can also add serial numbers, create selectable design options, or embed microcode to make your design adaptable to changing market requirements.

VLSI has incorporated the antifuse technology by creating programmable system-function blocks for its $1\text{-}\mu\text{m}$ design library. Only one block is presently available, a field-programmable ROM. It comes in $512 \times 1\text{-bit}$ and $512 \times 32\text{-bit}$ arrays with readback-security cells you can program to hide your design from prying eyes.

Future blocks will include PLD and FPGA structures, so you can get your ASIC into production and



Structures like this $512 \times 32\text{-bit}$ ROM are the first in a series of field-programmable logic blocks now available in VLSI Technology's $1\text{-}\mu\text{m}$ ASIC library.

still have the ability to make last-minute logic changes. You can also create custom blocks that, for example, let you select resistor or capacitor banks to tune oscillators and filters.

Programming a custom IC can be a challenge. To meet this challenge, VLSI has adopted a mother-/daughter-board approach. VLSI's standard mother board contains all of the computer interfaces, self-test hardware, and programming details. Custom daughter boards plug into the mother board and provide the physical interface for your specific pinout and package type. You can do the programming at wafer sort or at the customer site.

The premium you pay for this

programmability is slight. Specific dollar figures vary with your design's size and complexity, but you can expect the die costs for a 2-metal-layer programmable ASIC to be comparable to a standard 3-metal-layer design. As for I/O-pin overhead, you only need two dedicated pins for the programming command and voltage. All other programming signals are multiplexed onto your other I/O pins. The programmable blocks can be as much as 20% of the die area.

—Richard A Quinell

VLSI Technology Inc, Inquiries
Dept 134—Code PROFSB, 200
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CIRCLE NO. 207

76 • EDN November 12, 1992

Live-insertion module allows board "hot swap"

The HS-1 live-insertion module lets you insert or remove a VME board from a VME system that is powered up and running. The 60-mm-deep module fits between a VME board and the VME backplane. Circuitry within the module electrically isolates the board from the backplane during power-up and -down sequences and when power is off.

When VME rack power comes on, the HS-1 module checks its own board slot to see if a board is plugged in. If a board is present, the module applies power to it; if not, it merely links daisy-chain signals so that these signals get passed down the VMEbus to the next slot.

To remove a board from an active system, you must first press a switch that connects to the module. This starts an isolation process in which the module requests the bus (to ensure that the sequence doesn't interrupt a bus operation), isolates the board, releases the bus, and powers down the affected slot.

To insert a board, no special ac-

tion is necessary. The HS-1 senses the inserted board, starts a power-up sequence, and connects the board to the bus. The module uses the bus for less than 400 nsec during either an insertion or a removal sequence.

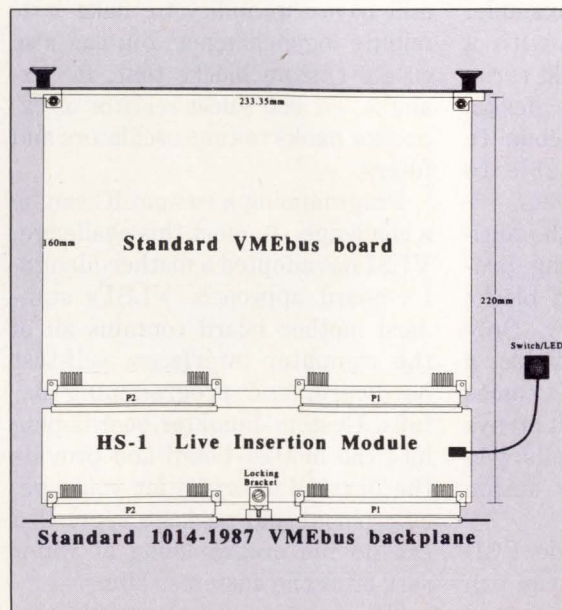
To avoid degrading system performance, the module uses special devices that switch bidirectional VME signals in less than a nanosecond. For single-direction signals, it uses normal TTL 3-state buffers.

During the power-up and -down sequences that accompany board insertion or removal, the module ramps the 5, 12, and -12V power rails to the VME board. This action prevents the main VME rack power supplies from generating glitches as a result of large, rapid changes in output currents. The HS-1 costs \$975; delivery is 45 days ARO.

—Gary Legg

Radstone Technology, 20 Craig Rd, Montvale, NJ 07645. Phone (800) 368-2738; (201) 391-2700. FAX (201) 391-2899.

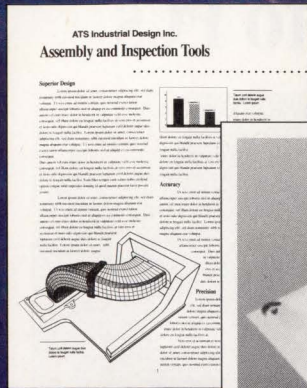
Circle No. 397



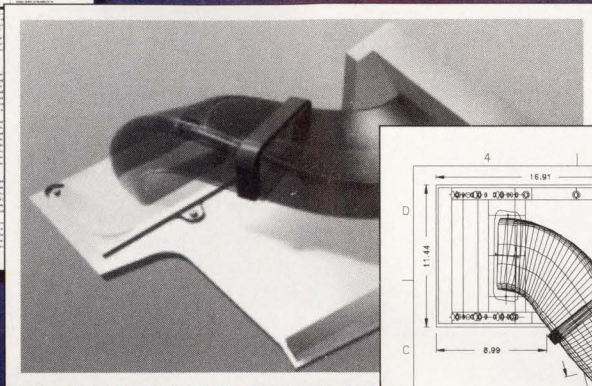
The HS-1 live-insertion module fits between a VME board and a VME backplane, letting you insert and remove the board while power is on.

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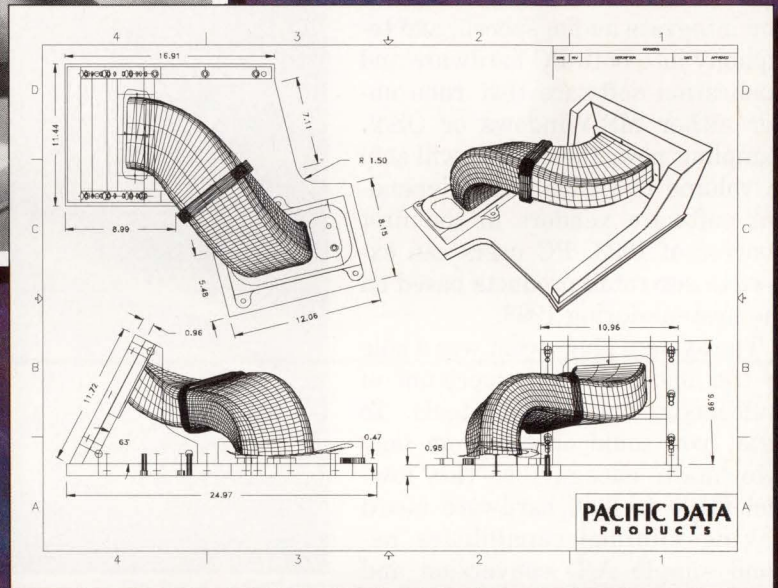
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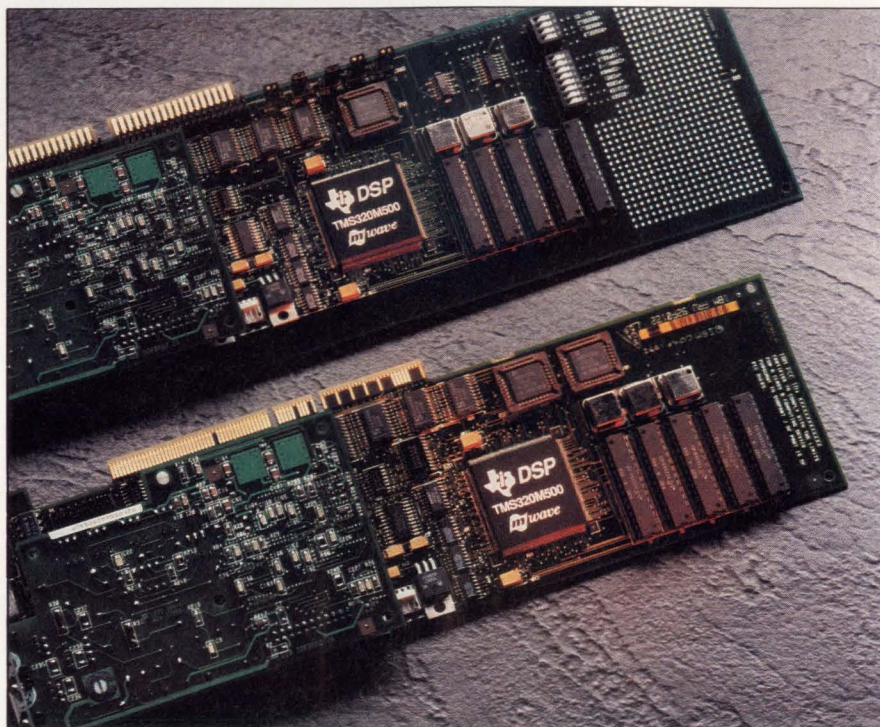
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Hardware/software combo brings low-cost, advanced multimedia to PCs

The alliance that IBM, Texas Instruments, and Intermetrics formed last March is bearing its first fruit: the Mwave Multimedia System from TI. The system lets you integrate audio, speech, and telephony into both PC hardware and application software that runs under either MS-Windows or OS/2. Sampling now, the system will ship in volume to OEMs and independent software vendors in the first quarter of 1993. PC users can expect to see retail products based on the system during 1993.

The system plugs what was a hole in the middle of the spectrum of multimedia development tools. To date, you could choose from only two main categories: the low-end (\$100 to 300) hardware board having minimal capabilities beyond simple A/D conversion and minimal support software, or the high-performance DSP board costing thousands of dollars but again having little software that targets mainstream applications development. The Mwave system offers substantial hardware and software resources at a moderate price.

The software/hardware combination lets you start a product line with OEM entry prices as low as \$100 and expand it to encompass a range of multimedia features at higher prices. For a planned price of \$995 in early 1993, you will get a developers kit that includes an evaluation module and comprehensive systems software. The combination lets you work either on the surface or in depth with both Windows and DSP tasking. The software includes a DSP OS and a manager/supervisory component that coordinates the DSP chip with the



The Texas Instruments Mwave Multimedia System includes a Software Developers Kit and hardware-evaluation module. Versions will support the ISA and Micro Channel Architecture PC bus standards.

host processor. TI will coordinate and resell device drivers for 3rd-party hardware and provide development kits for device drivers as well (second quarter 1993).

The hardware includes a developer's board with a custom, 17-MIPS DSP chip, called the TMS320M500. The DSP μ P includes on-chip interfaces for phone, voice, CD stereo, MIDI, PC modem (UART), audio control, and DMA access to the PC bus (ISA or Micro Channel Architecture). The interfaces give you multiple serial DMA channels (one per peripheral type) that impose no overhead on either the host processor or the DSP μ P.

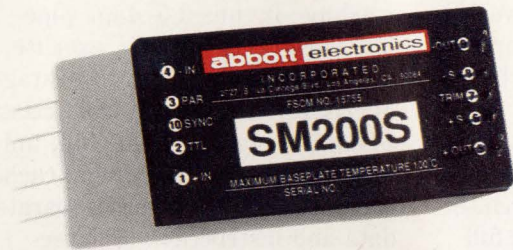
The software includes a Software Developers Kit (SDK) and system software. The SDK includes Win-

dows or OS/2 device drivers for audio, fax, data-modem, and telephone-answering-machine capabilities with speakerphone and handset I/O. The audio drivers perform music synthesis, audio compression, text-to-speech conversion, and sound-effects processing. The system software includes both the embedded Mwave OS, which runs concurrent multimedia tasks on the DSP, and a Manager component that mediates between the Mwave OS and MS-Windows and ensures timely task completion.

—John C Napier

Texas Instruments Inc, SC-92079, Box 809066, Dallas, TX 75380. Phone (214) 995-6611, ext 3990.

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CIRCLE NO. 65

EDN November 12, 1992 • 79

\$179 buys a single-chip, 50-MHz desktop SPARC CPU

Next-generation, 32-bit SPARC RISC is more than just high-throughput, super-scalar SuperSPARCs or hyper-SPARCs (EDN, June 4, 1992, pgs 89 to 94). It also includes high-integration, minimal SPARC μ Ps that target mid- to low-end computing. Texas Instruments' MicroSPARC is the first of these integrated SPARCs. Running at 50 MHz, with two on-chip caches, it delivers first-generation execution speeds (see **table**).

MicroSPARC represents a new direction in SPARC design, which has been growing in complexity and size. Unlike the current generation of desktop SPARCs, the MicroSPARC targets low-chip-count designs. It integrates a dynamic-RAM (DRAM) refresh and addressing controller and a 5-slot SBus controller on chip. You can cobble together a single-board SPARC system with five SBus slots, up to 128 Mbytes of memory with a MicroSPARC, eight memory SIMMs, a boot PROM, and four signal-buffer chips. Also needed are two NCR SBus peripheral chips, the NCR 89C100 and the NCR 89C105, which provide the SBus master I/O (DMA

controller, parallel port, Ethernet, and SCSI) and the SBus slave I/O (counter/timers and serial ports, as well as interrupt, mouse/keyboard, and floppy controllers).

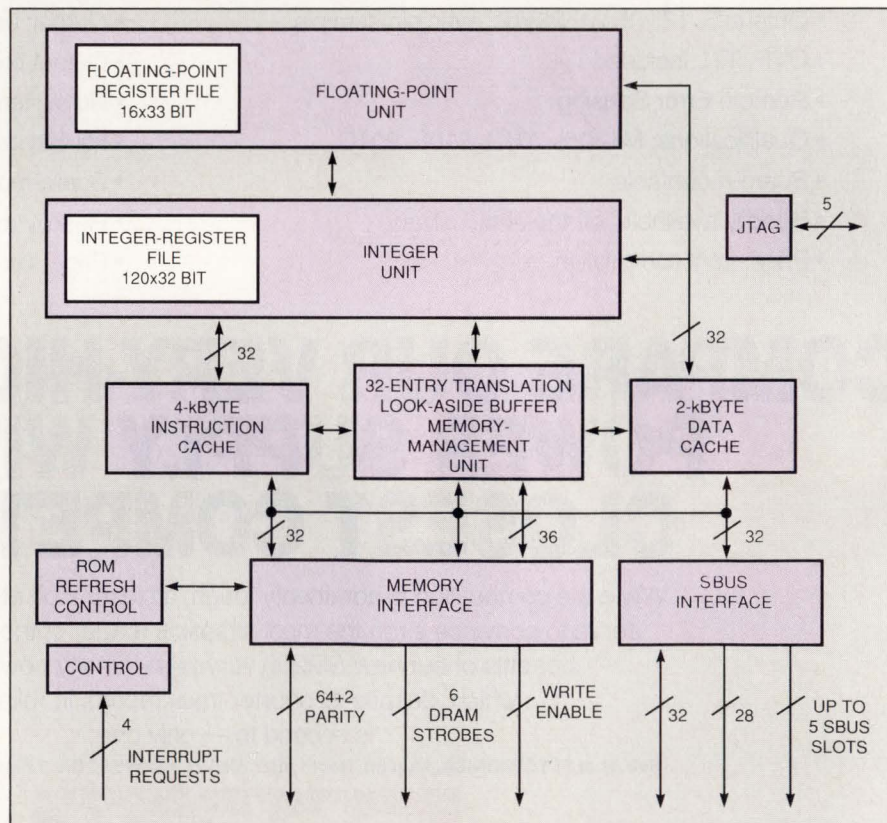
Developed by Sun and TI, MicroSPARC implements the SPARC version 8 Instruction Set Architecture (ISA), which includes a full hardware multiply instruction. MicroSPARC is a classic RISC CPU with 108 instructions, limited addressing modes, and a load/store architecture. A SPARC, the TI processor has a large register file of 120 32-bit registers, which are organized into a set of overlapping register windows and eight global registers. The chip includes a floating-point unit with its own 32 32-bit floating point registers.

MicroSPARC is a single-issue machine; it runs a 5-stage pipeline with fetch, decode, execute, cache access, and writeback stages. MicroSPARC deviates from classic SPARC design with off-chip, unified caches and two on-chip caches organized in a Harvard (separate data and instruction) architecture. Both the 4-kbyte-instruction and 2-kbyte-data caches are 32 bits wide and direct-mapped, with a 32-byte cache line size. The data cache provides a write-through, no write-allocate protocol (cache writes are passed through to memory). A double word buffer holds writes, permitting execution to continue.

To speed execution, MicroSPARC has a 64-bit-wide memory

TI MicroSPARC TMS390S10 μ P

- 50-MHz 32-bit SPARC, 120 registers with 7 registers windows
- On-chip 64-bit FPU, 32 32-bit registers
- 22.8 SPECint92; 17.8 SPECfp92
- 800,000 transistors
- 5-stage pipeline
- 4-kbyte instruction cache
- 2-kbyte data cache
- 27-bit unified address space
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MicroSPARC integrates a 50-MHz SPARC CPU with a DRAM and SBus controller and on-chip instruction and data caches. It directly drives up to 128 Mbytes of DRAM and five SBus slots.

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3.3 \longleftrightarrow **5.0V**

10 Bit

5.0V P4C218 Cache RAM

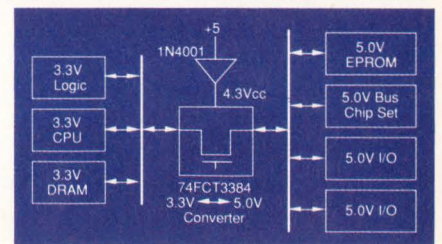
With wide-word, on-chip address latch, high and low byte controls, low standby power, 13ns access time including delay through the on-chip latch, Performance Semiconductor offers you a versatile, low part count solution for 40MHz primary and 66MHz secondary caches. For use with multiplexed address-data buses, or as general-purpose static RAM with iX86, MIPS R3000A, and R4000 processors. The P4C218 is available *NOW* in standard JEDEC 52-pin PLCCs.

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For mixed supply systems, Performance Semiconductor now offers the P74FCT3384, a zero delay, 3.3V to 5.0V bidirectional translator that provides a set of ten high-speed CMOS/TTL-compatible switches which allow interfacing of 3.3V and/or 5.0V components within an application without adding propagation delay or ground bounce noise. Performance's FCT3384 is supplied in surface mount SOIC, PDIP, and the super tiny SSOP150 for notebook or palm top applications.



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bus. With a 60-nsec DRAM, reads take only one cycle and writes take two. Error-detecting parity is carried in the system, but to keep costs down, MicroSPARC implements a single parity bit for each 32-bit word, adding 2 bits to the bus. The chip has a 27-bit address space with up to 128 Mbytes of memory in eight SIMMs, which is organized into four banks (two CAS and four RAS strobes, and 22 bits of row/column addresses).—**Ray Weiss**

Texas Instruments, Semiconductor Group (SC-92093), Box 809066, Dallas, TX 75380. Phone (214) 995-6611, ext 3990. Circle No. 383

Clock-buffer IC prevents skew-ups in P5 PC designs

Although Intel hasn't released its long-awaited successor to the 80486 (code-named the P5), the industry is already preparing for its arrival by introducing support devices. The GA1086 from TriQuint Semiconductor is one such device, offering low-skew clock buffering.

Adequate clock distribution is key to the success of any high-speed design. One of the most important parameters to control in your clock distribution tree is clock-to-clock skew for the various branches. Too much skew and the subsystems hanging on those branches will fail to meet each other's setup or hold requirements.

The GA1086 solves the skew problem by locking an internal 400-MHz phase-locked loop (PLL) to the P5's 66-MHz system clock. The incoming clock can have a pulse width as low as 3.8 nsec. The output clocks will be symmetrical, with nine of them at 66 MHz and one at 33 MHz.

Each of the 10 clock output signals derives from the PLL signal through a divider chain. You can

feed one of the signals back as a reference for comparison with the system clock, resulting in an effective propagation delay of ± 500 psec for the clock signals.

Several of the device's important features don't show up in the timing specs. For example, the device is packaged in a metal quad flatpack (MQUAD). This package style has a metal plate built in, which serves as a heat spreader. As a result, the device operates over its 0 to 70°C ambient temperature range without needing a heat sink or more than convection cooling.

The device also incorporates a test mode that can help to debug your design. In the test mode, the input clock bypasses the PLL and divide logic, passing straight to the output buffers. Thus, you can single-step or gate your system's clock or run at any frequency you need for test purposes.

TriQuint offers a less expensive version, the GA1086E (\$22.73), for those with looser system requirements. The principal difference is

TriQuint GA1086 clock-buffer IC

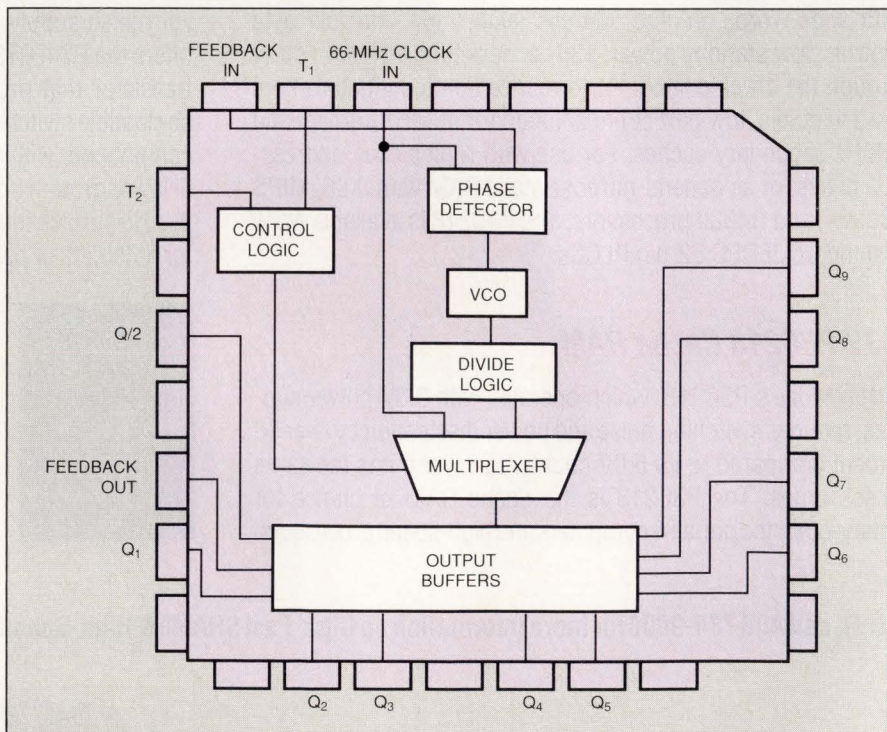
- 66-MHz $\pm 5\%$ input clock
- 500- μ sec (max) PLL capture time
- 250-psec (max) clock-to-clock skew
- 75-psec (typ) edge jitter
- 30-mA, TTL output drive
- In 28-pin J-lead MQUAD package, \$26.79 (1000)

the effective clock-to-output signal delay. The GA1086E has a delay of 1 nsec instead of 500 psec.

The device will tolerate either series or parallel termination, but TriQuint recommends parallel termination for best performance where the excess power dissipation in the termination network is not of concern. The device's data sheet includes examples of both termination types, as well as suggestions for clock trees with more than 10 branches.

—**Richard A Quinnell**

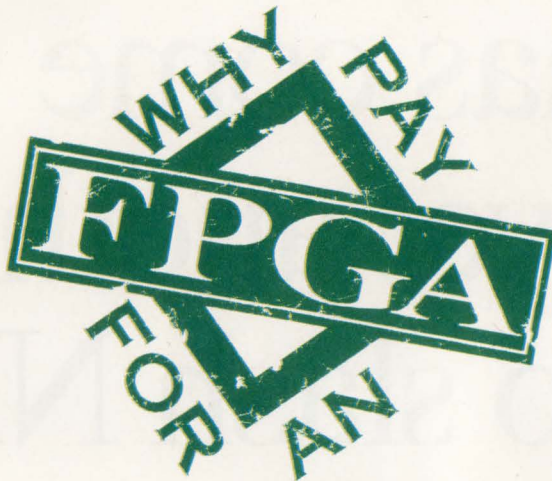
TriQuint Semiconductor Inc, 2300 Owen St, Santa Clara, CA 95054. Phone (408) 982-0900. FAX (408) 982-0222. Circle No. 384



By locking a high-frequency PLL to the incoming clock signal, the GA1086 produces 10 copies of the clock with less than 250 psec between them.

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Packages	44 PLCC	84 PLCC	100 PQFP	144 PQFP	160 PQFP
	28 PLCC	68 PLCC	84 PLCC	100 PQFP	144 PQFP
PLCC	20 SOIC	44 PLCC	68 PLCC	84 PLCC	100 PQFP
PQFP	16 SOIC	28 PLCC	44 PLCC	68 PLCC	84 PLCC
SOIC				44 PLCC	68 PLCC
					44 PLCC

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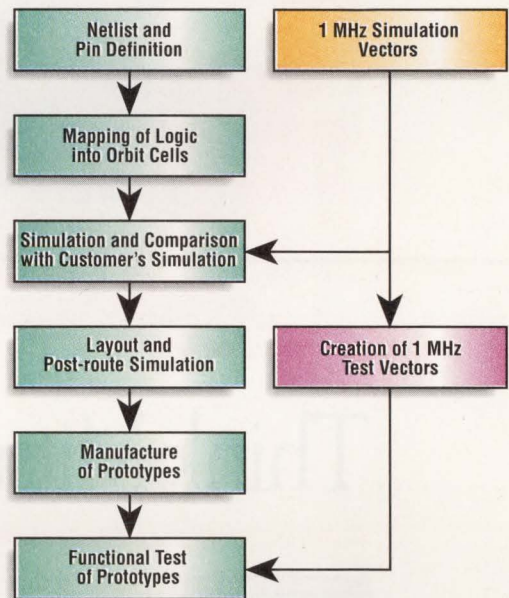


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Here's what we need to get started:

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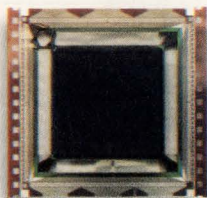
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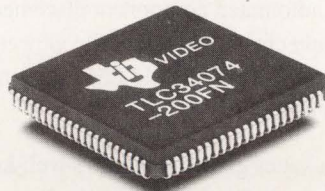
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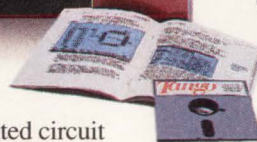
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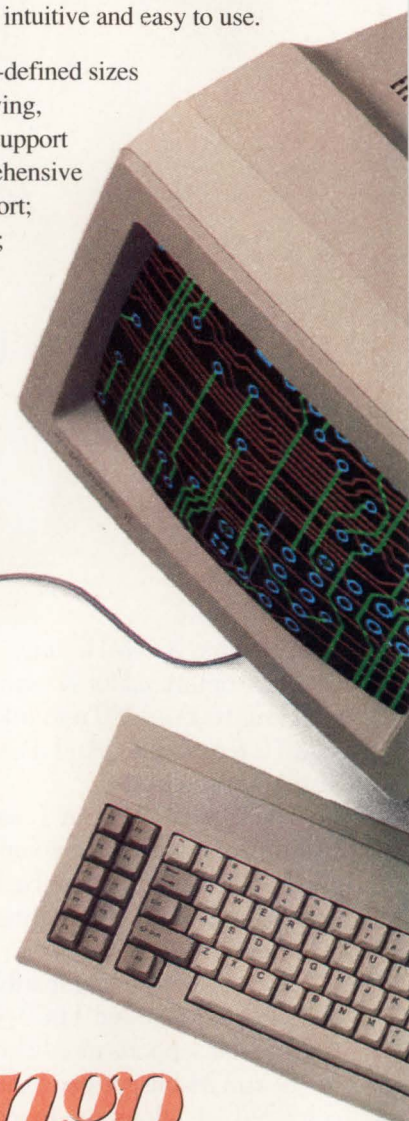
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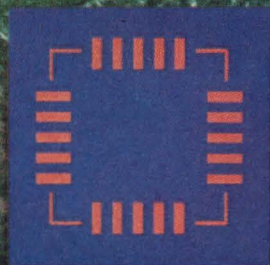


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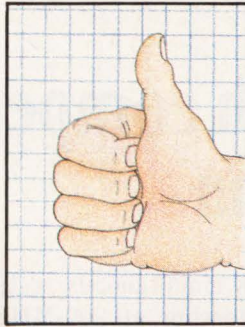
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PART 4

Increasing your effectiveness by bringing in outside help

Dan Strassberg, Senior Technical Editor

This final part of Design It Right is about an increasingly popular way of maximizing your development funds' impact—having another organization perform some or all of your new-product development work. Almost every product that uses custom ICs relies heavily on the effort of another company or division. But such strategic partners are by no means limited to manufacturers of custom ICs; electronics firms started forming strategic partnerships long before custom chips existed.

Two of the stories in Part IV are about products based on custom ICs. One product

family, Teradyne Inc's J990 series of memory-test systems, uses 11 custom chips from three vendors. The other, Hewlett-Packard's 16550A, a plug-in for a modular logic-analysis system, uses two custom devices manufactured by other HP divisions. If you work for a multidivisional company, you know that buying a key component from a sister division can

sometimes require more skill than dealing with a separate company. HP's story tells of a successful relationship between divisions.

Lastly, this part discusses Analogic Corp, a company that pioneered in forming strategic partnerships with other firms. Analogic is not a manufacturer of semiconductors. It engineers and manufactures a variety of high-tech assembled products. Despite Analogic's large number of strategic partners, hardly anybody is aware of how many products the firm designs and builds.

Teradyne Inc.—J990-series memory-IC test systems

Attributes of a tough competitor: audacity and stamina

If a company is a reflection of the person at the top, then Teradyne Inc, the Boston-based manufacturer of automatic test equipment (ATE), CAE tools, and interconnection products (annual sales >\$500 million; ~4300 employees), certainly mirrors the personality of its co-founder, Chairman, and CEO. For three decades, Alex d'Arbeloff has been synonymous with ATE, the industry he helped to found. Sometimes wrongly described as humorless, d'Arbeloff is serious and plainly intense. His single-mindedness and dogged determination do much to explain why Teradyne continues to be a leader in ATE, even though some of its competitors are floundering.

Such fortitude may be common enough among the Japanese companies that have successfully penetrated American markets, but it is rare—if not unique—among American electronics firms. Nevertheless, for those of stout heart whose companies' pockets are deep, persistence appears to lie at the core of successful competition with the Japanese. Teradyne's tradition of tenacity, backed by its belief that being a successful competitor requires great resolve, set the stage for an especially bold move: a heavy investment in developing a new line of systems for production testing of memory chips. The J990 family goes head-to-head with made-in-Japan test systems in a market dominated by Japanese customers.

The new testers offer such capa-

bilities as simultaneous testing of 64 ICs, testing at 200-MHz, the ability to handle chips with a variety of architectures from 1 to 18 bits wide, and the ability to accommodate devices and assemblies that store as much as 4 Gbits. Despite the array of features, cost per test site is about half that of earlier memory testers. Teradyne hopes to sell several hundred of the systems, which carry price tags that start at about \$700,000.

As you might expect, the new product line, which the firm's Semiconductor Test Division (STD) in Agoura Hills, CA first shipped only

this past winter, has yet to capture the lion's share of the memory-chip-tester business. The series has, however, racked up some impressive wins over competition, including at least one win over an Asian ATE firm at an IC company in Asia. You can bet that Teradyne will continue to battle and innovate in memory-test as well as in other areas of semiconductor test. (STD, with about 475 employees, is just one of the Teradyne divisions in the IC-tester business. The other, the Industrial/Consumer Division (ICD) in Boston, makes testers for analog and mixed-signal chips.)



Automatic test systems for ICs are among the largest electronic systems sold today as standard products. In appearance, though not in performance, the memory-IC testers in Teradyne's J990 series are typical of the genre. The systems' 11 custom ICs provide evidence of the testers' state-of-the-art technology.

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Leave nothing to chance

Not all of Teradyne's do's and don'ts apply to custom ICs. Some are specific to such parts; some apply to custom ICs and to assemblies that might either be purchased or built in house; others relate to different facets of the design process and to the interface between design and manufacturing.



From the outset, put a lot of effort into selecting suppliers of unique parts, especially suppliers of custom ICs.



Involve senior engineering, operations, and purchasing people in qualifying vendors.



Don't pick "delicate" vendors—ones who lack either the resources or the commitment to work with you to resolve problems in a timely manner.



Be sure you understand how suppliers plan to test an item and how they will ensure its quality. Misunderstandings in this area have the highest potential for causing problems between your suppliers and your company.



Remember that nothing about a custom component's specification is obvious; spell out your requirements. For example, suppose an IC's switching delay changes as a function of its junction temperature, which depends on the ambient temperature and power dissipation. If you need some maximum switching delay at the worst-case junction temperature, make sure that the test protocol guarantees it. (If you can't run tests at the worst-case temperature, you should run them with modified limits under conditions that are practical.) In this example, if you

fail to make your requirements clear, the vendor is likely to test the parts under irrelevant conditions, and there is a good chance that you will be unable to use a large percentage of the parts you receive.



Ensure that each design meets manufacturability rules by conducting design and manufacturability reviews early in the development cycle.



Check out new manufacturing processes before you decide to use them. Teradyne uses what it calls PETs (process-evaluation tools) for this purpose. For example, to determine the yield of a new soldering process and to reveal inherent weaknesses in the process, STD manufacturing designed a special pc board, which it then tortured and tested extensively.



Nurture the relationship between design and manufacturing. STD's manufacturing engineering group made major contributions to the J990 series from the outset. In fact, manufacturing contributions were so great that Teradyne was reluctant to divulge what percentage of the total J990 design effort represented design labor and what percentage represented manufacturing labor.



Establish cost targets as part of your initial product definition. Design to those targets and use them to continually monitor your performance.



Don't start the development until hardware and software design, marketing, and manufacturing management have all agreed on the product definition.



Listen not only to what the customer says, but to what he or she *means*. Customers will tell you about today's problem; you have to understand the underlying need. By the time you deliver your product, the customer will probably have solved the immediate problem, but the underlying need may well persist. If your product addresses a real need, you should be able to sell it; if it merely addresses a symptom the customer has already dealt with, you have little basis for a sale.



Don't assume that information will just naturally flow between people who happen to sit near each other.



Put information-transfer mechanisms in place and work on continually improving them. In Teradyne's case, in addition to the IC design manual, these mechanisms include in-house newsletters to which design and manufacturing people are encouraged to contribute. Teradyne's engineering community is large enough that contributors receive genuine recognition from peers. Most find the recognition so gratifying that they become repeat contributors, even though contributing requires work beyond their regular assignments.



Don't take the claims of CAE tool vendors at face value. Conduct your own evaluations before you decide that a particular tool set is the right one for a specific job. Note that Teradyne makes this suggestion even though some of its divisions supply CAE tools.



Don't assume that you can use the current generation of tools to design the next generation of products.

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Teradyne may be audacious, but it isn't stupid, so eight of the J990's custom ICs are ones that the company first used in a tester family it introduced about a year earlier: the J971 series of high-speed VLSI-IC test systems. ICD's testers also use some of these chips. During the J971 development, plans for the J990 series had gone beyond the formative stages, so the J971 team was able to consider the needs of the J990 as well. However, as STD Engineering Manager, George Conner puts it, "even if we hadn't been planning to develop new memory testers, the custom chips would have been nearly the same." The architecture of VLSI testers is more general than that of memory testers, so, from a technical standpoint, it made sense to develop the VLSI tester first.

Of course, Teradyne also had marketing reasons for designing a new VLSI tester before designing a new memory tester. Among the reasons: for memory-chip families in current production, IC makers were locked into ATE choices they had made earlier. New generations of memory chips and new decisions about ATE still lay down the road. Indeed, even after the J990 announcement, the worldwide recession delayed many customers' decisions on new memory ATE longer than Teradyne would have liked.

The J990 series uses 11 custom ICs of several types from three vendors. Teradyne has learned a lot about what to do and what not to do in custom-chip developments—so much, that it has written a book, *The IC Design Manual*. But no, you can't get a copy; the contents are

proprietary. The company considers its knowledge in this field to be a weapon in the arsenal it can turn on competitors. Nevertheless, the firm agreed to let EDN readers in on a few of its findings. They appear in the accompanying do's and don'ts **box**. Because several divisions design custom chips for their products, the book is a safeguard against a division repeating errors that another division learned from at great pain.

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Sue Hudson

Circle No. 315

Hewlett-Packard, Colorado Springs—16550A

A conservative approach can yield a state-of-the-art product

The 16550A is a 102-channel plug-in for Hewlett-Packard's popular 16500 series of logic-analysis systems. The board uses custom ICs of two types: a very-large-scale integrated CMOS chip and a much smaller bipolar chip that contains, mainly, high-speed comparators. According to HP, if you accept the number of transistors on a chip as an index of the IC's complexity, the CMOS chip, with roughly 1.2 million transistors, is about as complex as an i486 μ P.

HP calls the CMOS IC a logic analyzer on a chip. It is the second such device that the Colorado Springs Division has designed. (In

addition to logic analyzers, the division manufactures HP's digital scopes and in-circuit emulators.) The first logic analyzer on a chip appeared in 1987 in plug-ins for the 16500 and is also the heart of HP's 1650 series of portable logic analyzers. Shortly after releasing the 16550A, HP announced a new family of portable analyzers, the 1660 series, based—like the 16550A—on the 1.2-million-transistor chip.

There is no question that the original analyzer on a chip had a major and lasting impact on logic analyzers. It significantly lowered the price of performance that appealed to a broad cross section of

users. Although that performance still has wide appeal, increases in μ P clock rates and word lengths have driven analyzer users to seek even greater performance. Thanks to the second-generation chip, the 16550A and the 1660 series deliver this performance.

By the most conservative measures, the new analyzer chip is 2.5 \times as fast as its predecessor; it also provides 4 \times the memory and over twice as many channels. The first-generation (NMOS) chip has 16 channels and performs timing analysis at 100 MHz and state analysis at 35 MHz. Its memory depth is 1024 bits. The new chip

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has 34 channels. It performs timing analysis at 500 MHz on half the channels or 250 MHz on all. (Using transitional timing cuts the timing speeds in half; using glitch detection limits timing analysis to 125 MHz.) The state analysis speed is 100 MHz. The memory depth is 4k samples/channel. When you use half the channels, the memory depth doubles.

It had to be right

Because the new analyzer chip was to be the heart of a bread-and-butter product line, it had to be

right in many ways. Both its performance and its cost had to be right. It had to be an item that the IC foundry could produce in quantity with good yields, and, when installed in an instrument, it had to perform reliably for years. Colorado Springs' experience with the older analyzer chip was an asset; lessons learned on the first development stood the 16550A team in good stead. But because of the much greater complexity of the new IC, the development was scarcely a piece of cake.

You might assume that because the foundry was another HP division (in Fort Collins, CO, over 100 miles away), Colorado Springs' problem was significantly more manageable than yours might be if you were to work with an independent foundry to develop a custom IC. On the other hand, if yours is a multidivisional company and you buy portions of your product from another division that is also a profit center (as HP's Fort Collins foundry is), you know that relations among divisions can come unglued

Make sure that everyone gets the message



Establish a "message" for your product very early in the program. This message is a succinct statement of the product's major objectives—in marketing terms, the product positioning.



Make sure that all team members have the message fixed firmly in their minds.



Don't change the message once you've decided on it and have started to communicate it. If you fail to send the message or if you send mixed or changing messages, confusion will result; everyone will develop a different mental image of the message. Because of lack of direction, people you must depend on for support will act in ways that seem counterproductive. You are responsible for making sure that everyone has the same clear message—yours.



At the appropriate times, send the product message to everyone who needs to know. As the project progresses, the group that needs to know will expand to include sales engineers

and customers. Failure to send the message to this larger group at the appropriate times will create the same kinds of problems as sending mixed or changing messages.



Decide early on which few performance features are essential in a product consistent with the chosen message.



Be quite ruthless about rejecting features inconsistent with the message. Team members and others will subtly test your resolve by suggesting non-essential features. Your actions must be consistent with your message.



Construct a detailed schedule early in the project.



Encourage team members to be realistic in scheduling tasks. Although excessive optimism is more common than pessimism, you'll encounter both and you should reject both.



Relegate work on non-essential but "nice" features to the back end of your schedule. If you have time, you may be able to include some of these features, but making it clear that

their priority is low will keep you from missing key dates because team members were working on nonessential features.



Base your selection of an IC process on availability of suitable tools and support.



Don't let promises of raw performance entice you to select a newer but less well-developed IC process.



Insist that the hardware designers thoroughly consider the implications of their decisions on the system software. Although the software people will probably be able to design around unfortunate hardware arrangements, doing so can take time. Often, implementing a more appropriate hardware design will be no more difficult, time consuming, or expensive and will save considerable software development effort.



Don't wait until first silicon is available to work on the test process for a new IC. HP learned that lesson during the development of its first-generation NMOS analyzer chip. Only a memory test was available when first silicon arrived. The inability to test most of the chip delayed the program.

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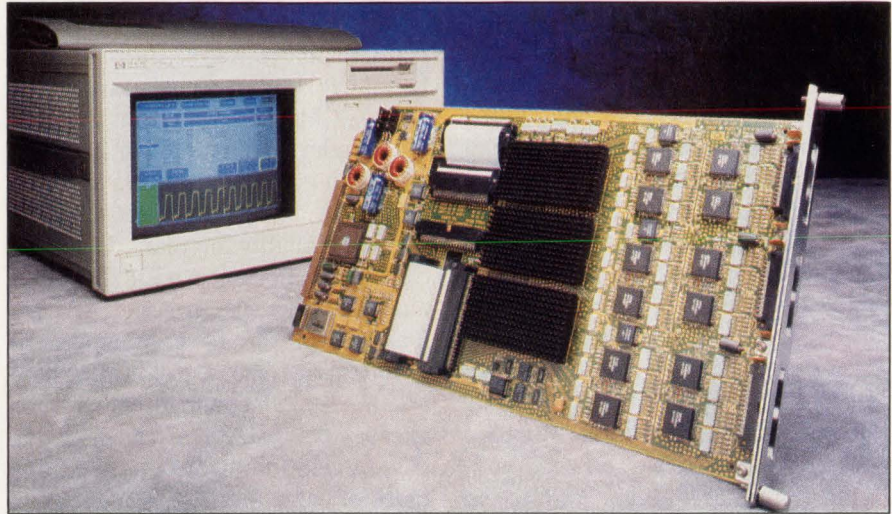
all too easily; too often, everyone involved in such a venture feels ill used. The successful relationship between the two HP divisions didn't just happen.

When a company (or, in this case, a division) works with another organization to produce a custom chip, the form of the partnership can vary widely. In the case of the logic-analyzer chip, the complete logic design and layout came from Colorado Springs. However, the designers didn't create the design in a vacuum and then send a set of workstation tapes to Fort Collins so chips could be fabricated. There was a high degree of cooperation in every phase. Before any real work began, the two divisions reached agreement on a number of key points and documented their agreement. (In essence, they drew up a contract.)

No new processes

One of the guidelines was that the chip was to be fabricated using an existing IC process with no adjustments to process parameters. Even though the IC would operate at very high speeds, Colorado Springs opted *not* to use the latest process. Instead, an older process was selected. Not only did this choice remove some uncertainty, it also allowed the designers to use a more mature set of design tools. The last thing the team wanted was to become embroiled in simultaneously developing a critical, high-performance chip *and* a set of tools. In the end, the existing IC process proved entirely adequate; there was never a need to reconsider the choice of a process.

One area involved especially close cooperation: testing the IC. Although Colorado Springs was responsible for the chip design and layout, Fort Collins has the HP 82000 IC evaluation systems that run the tests, so testing became Fort Collins' responsibility. Colo-



The custom CMOS logic-analyzer chips reside beneath the heat sinks on the 16550A board, shown here in front of the 16500A. (The 102-channel 16550A uses three of the 34-channel chips.) HP found that it could have used smaller heat sinks, but decided to retain the large ones because they lower the ICs' junction temperatures and increase the devices' reliability.

rado Springs had simulated the IC during the design phase; obtaining a first-pass set of functional test vectors merely entailed throwing a few software switches and translating the simulation vectors.

That was not the end of the test-process development, though. Having vectors ready for testing the first silicon was important to keeping the program on schedule. But as you might expect with a chip this big, fast, and complex, a lot more work was needed before chip approval; still more work had to go on before Fort Collins concluded that the test process worked in production. Back in Colorado Springs, the team had assembled a prototype 16550A into which it could plug the first packaged devices as soon as they arrived.

Clearly, showing that a chip works in its intended application is a big step—a much more satisfying one than running a simulation successfully or running functional vectors on the chip in a tester. Nevertheless, it is important not to let emotion rule the day. Management may be breathing down your neck, looking for an indication that the

custom chip is good. With such pressure, when you first see the prototype work, your temptation may be to break out the champagne. Instead, you should methodically complete your test protocol, as the 16500A team did. Otherwise, you may not discover subtle faults that, if they go undetected, could cause major problems later.

One possible and very serious problem that can result from too much optimism too soon is failure to recognize the need to go through another round of IC mask changes. From a cost and schedule viewpoint, such changes are bad enough. (The effect on the product in the marketplace can be fatal.) But from a personal standpoint, having to go through such changes after you've declared them unnecessary can bring a rapid end to your career.

Fortunately, the 16550A project encountered no such problems. It kept very close to its schedule. Ed Davis, who managed the program, attributes this success to attention to detail. One example was the way he learned to calibrate team members' estimates of how long tasks would take. He compared the actual

times with the forecasts and developed a "fudge factor" for each team member. He updated the fudge factors with the completion of each new task, and applied them to subsequent forecasts.

One place where Davis feels that he and the team could have done better was in predicting the effect

of hardware implementation details on the system firmware. He thinks that the software engineering job would have been simpler if, before committing to fabrication of the first silicon, the team had spent more time considering what its hardware decisions implied about the microcode. Had the team taken

this time early on, the software engineering job would have been simplified enough that the project could have been completed sooner.

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Analogic Corp—Strategic partnerships

A partner you can trust and work with can be a big asset

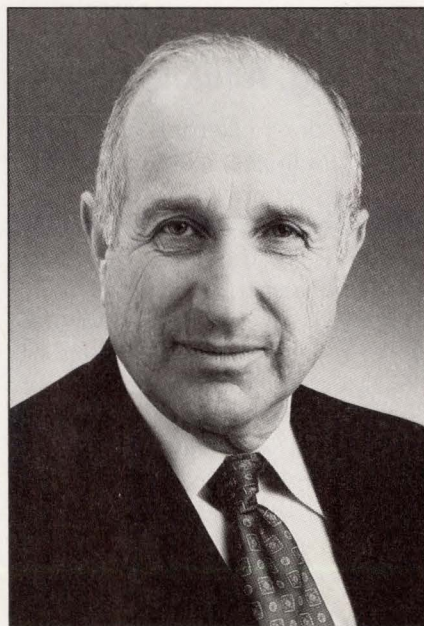
Time was, if you worked for a company of any size and you designed a product that used a sole-sourced component, you were destined to have to defend your decision in front of management, and, very likely, to redesign the product using components several sources.

You've probably heard the arguments against sole sourcing: Sole-sourced parts take away the purchasing department's leverage in negotiating the best price. (Though hardly anyone ever says so, sole-sourced parts actually do away with much of the purchasing department's reason for existence.) If you use a sole-sourced part, how will your company be able to continue delivering the product you designed if the part supplier goes out of business or discontinues the part?

Although many companies still insist on using multiple-sourced parts, the rule is far less universal than it once was. In many firms, the insistence on multiple sources has given way to something close to the exact opposite: the strategic partnership.

In the context of this discussion, a strategic partnership is an ar-

angement between two companies in which one provides a significant portion of the other's product. Although the exact roles of the partners vary greatly from deal to deal,



Analogic Corp's founder, chairman, and CEO, Bernard Gordon, has built his company on partnering with OEMs. For these companies, Analogic designs and builds custom instrumentation and signal-processing equipment. The firm also builds several lines of standard products.

in this type of partnership, you generally are not contracting with another firm to have it build something that you designed; you are turning over responsibility to your partner to design and manufacture a major part of a product or an entire product.

To learn more about such partnerships, EDN visited a company that pioneered in working as a partner with other firms. Although it does sell proprietary products under its own name, Analogic Corp of Peabody, MA, a firm with approximately 1200 employees worldwide and annual sales of about \$140 million, probably has more experience than any other company in the development and quantity manufacture of custom products for control, data-acquisition, image processing, and signal processing. These products go into commercial, industrial, medical, and military applications.

The units' primary content is electronic, but some also include electromechanical items, such as printers. They range from instruments for which the final purchaser might pay a few thousand dollars to major subsystems which, if sold

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separately, would command as much as a quarter million dollars. When Analogic's partners resell the firm's products to customers of their own, the prices they receive usually are between three and five times what they paid Analogic. Consequently, in over 20 years of existence, Analogic has delivered many billions of dollars worth of equipment that hardly anyone knows it designed and built.

Bernard Gordon, Analogic's founder, chairman, and CEO, is, beyond question, a legend in our industry. The holder of nearly 100 US and foreign patents, Gordon has made a substantial fortune for himself and for more than a few of his employees. At the root of this success are two major strategies: focusing his company's work on the most difficult areas of electronic technology and choosing to build the firm's core businesses around strategic partnerships.

This mode of operation continually places stringent demands on Gordon himself and on Analogic personnel. Yet, despite (or maybe because of) this highly charged atmosphere, Analogic has always been able to attract and retain some of the brightest and most resourceful technical minds in the business.

Gordon doesn't like the term "engineering manager;" to him, it connotes business-school types who have little if any appreciation for the technology—technology to which he's devoted his life. He prefers "project engineer" (or chief engineer). A chief engineer is someone who spends the majority of his time doing engineering, but who may do a little managing when the situation requires it. Despite his other titles, Gordon still unabashedly assumes the function of project engineer in programs that involve his company's major partners.

As a project engineer in the com-

pany where you work, you can play a crucial role in developing a strategic partnership with a firm like Analogic. That role is likely to involve obtaining proposals and evaluating competitive bids. But, unlike Gordon in his dual role of project engineer and CEO, you aren't likely to have the final say. Ultimately, someone further up the corporate ladder, a general manager or your company's president, will be the one who commits your firm to the partnership. Regardless of how you feel about a potential partner, no strategic partnership will go very far without good chemistry between the people at the top in both companies.

As in successful partnerships of all kinds—living with someone . . . marrying someone—successful strategic partnerships are built on trust. In an atmosphere of trust, when somebody makes a mistake, the discussion doesn't focus on plac-

The do's and don'ts of partnering, Analogic style

From Gordon's and Analogic's viewpoint, the most important thing you can do when dealing with a potential strategic partner and in working with a partner once the two firms have struck a deal, is:



Put your personal pride behind you and focus on your company's needs. As an engineer, you've been trained to solve problems. It's only natural that you have ideas about how to design the product your company is thinking of having a partner design and build; you may even regard the idea of bringing in a partner as a personal affront. Although you should . . .



feel free to express your ideas, . . .



don't enter the discussions with the expectation that your partner is simply going to execute what you've proposed. If you do, you set up yourself, and your partner, to fail.



Listen to your partner . . . listen well. Successful partnerships require that both partners be good listeners.



Tell your partner *what* you need accomplished, *not* how to accomplish it.



Don't impose too many constraints. Constraints can prevent your partner from taking advantage of its strengths in certain types of design or manufacturing.

Gordon points with pride to how,

by listening to its Japanese partners, Analogic upgraded its state-of-the-art pc-board manufacturing facilities not just to meet, but to exceed Japanese quality standards. Moreover, the company has achieved these quality levels while maintaining a very favorable cost structure. Unlike many suppliers of high-quality boards, Analogic produces a large number of different board types *and* builds more than a million boards each year.



Look for a partner familiar with the technologies that form the basis of your product.



To the partnership, you should expect to contribute a knowledge of your customers and their applications, and an understanding of how your product is sold.

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DESIGN IT RIGHT

INCREASE YOUR EFFECTIVENESS

ing blame; it moves quickly to how best to go forward.

For example, Gordon recalls an incident when, after a hard-fought shoot-out with competition, he won an order for 2000 data-acquisition units. Shortly after delivering them, he discovered that 30 units had failed at the customer's sites. Without waiting for the customer to ask him to do anything, Gordon decided to recall and rework all of the units; the immediate impact on Analogic was a \$1-million charge. A supplier of optoisolators had, without notice, changed its manufacturing process, causing a reduction in the component's breakdown voltage. From Gordon's viewpoint, the million-dollar charge was something he had to incur to live up to the trust the customer had shown by placing the order with Analogic.

If this discussion has aroused your interest in Analogic as a partner, you should understand that the firm looks for partners who, over the production life of a product—typically about five years—will buy

an aggregate of roughly \$5 million worth (or more) at Analogic's prices. To Analogic's partners, that translates to between \$15 million and \$25 million in sales to their customers; an average of \$3 million to \$5 million annually. Of course, no such minimums apply to orders for Analogic's standard products.

Analogic makes its money from manufacturing and selling products to its partners. When the firm anticipates that a partner will purchase a custom product at a \$1-million annual rate, Gordon expects to invest \$250,000 on the initial development and another \$250,000 on continuing engineering and enhancements over five years.

If \$250,000 (your partner's \$250,000, at that) strikes you as a rather small sum for developing a product that will bring your company perhaps \$20 million in revenue, Gordon says he really believes that Analogic's engineers are about 3× as productive as the average in the industry. The productivity measure is revenues from product

sales to end users divided by the cost of development.

Gordon attributes the high productivity to Analogic's operational style—built not around managers, but around working project engineers. He feels that most companies are overburdened with paperwork and that they turn their most creative engineers into managers, who at best turn out to be mediocre at managing and also become unproductive as engineers. At Analogic, chief engineers spend most of their time engineering rather than managing. Thus, the company's most creative people are also its most productive.

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Where to from here? You decide.

The four parts of Design It Right have included over 100 do's and don'ts—techniques that the companies we've covered use to ensure that their product-development programs are successful. By "successful," the companies mean well received by customers, reliable, and profitable.

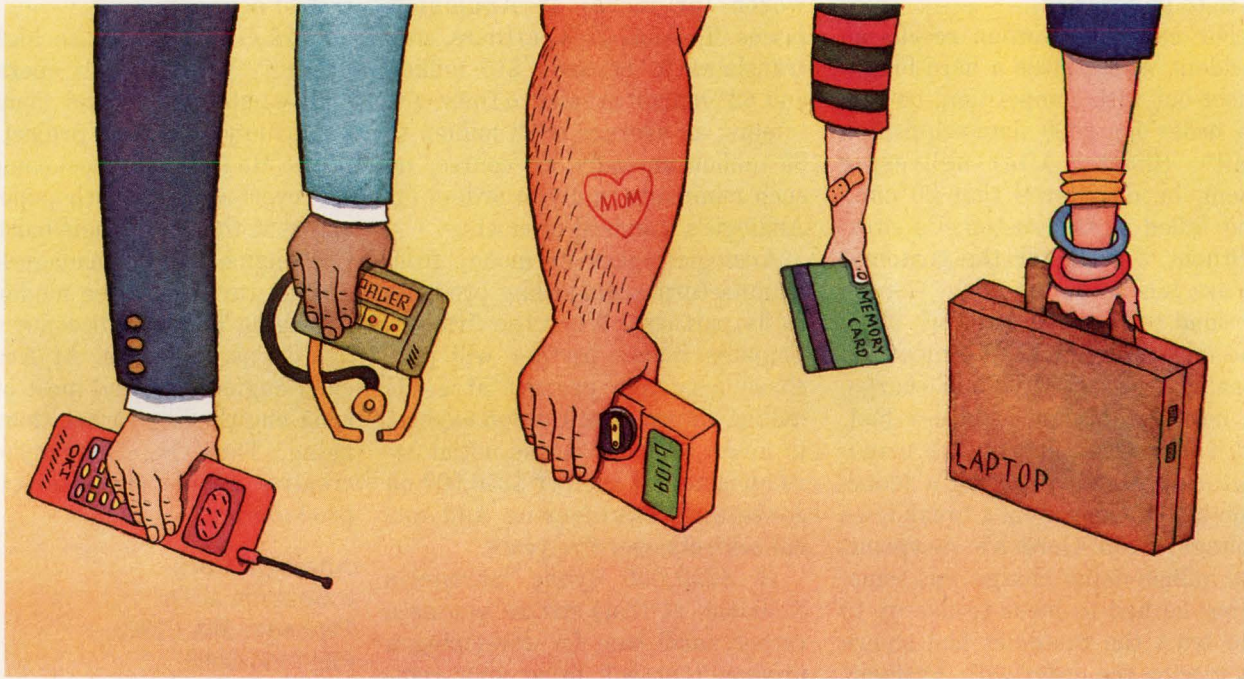
As we promised at the outset, there is less than total agreement among these companies on what works and what doesn't. For example, Quantum Corp relies on what it calls a "bump" environment (EDN, October 15, 1992, pg 97) to encourage communication among members of a project team, whereas Teradyne (in this issue) says that you can't rely on people to communicate just because they sit close to each other. So, as we said in Part I, you've got to evaluate which of the series' do's and don'ts are worth trying in your own company or division.

One area where the companies agree unanimously, is that designing a successful product requires looking at the customer's problem from the customer's view-

point. If this statement sounds like a sweeping generalization that nobody of sound mind could possibly disagree with, look around at the products you use every day and ask how many of them really succeed in addressing your needs. (If you look at products made by companies other than your own, you'll probably be able to answer more objectively.) Once you've convinced yourself that other companies often fail to follow this totally obvious advice, maybe you'll be willing to concede that your own products could do a better job of addressing customer needs.

When you've completed that exercise, go back over the do's and don'ts presented in the four parts of Design It Right and take a second look to see how many of the ones that you first dismissed as obvious might also be worth serious consideration. The do's and don'ts really represent a gold mine of ideas. However, the hard part—deciding which ideas can work for you, and actually making them work—has to be your responsibility.

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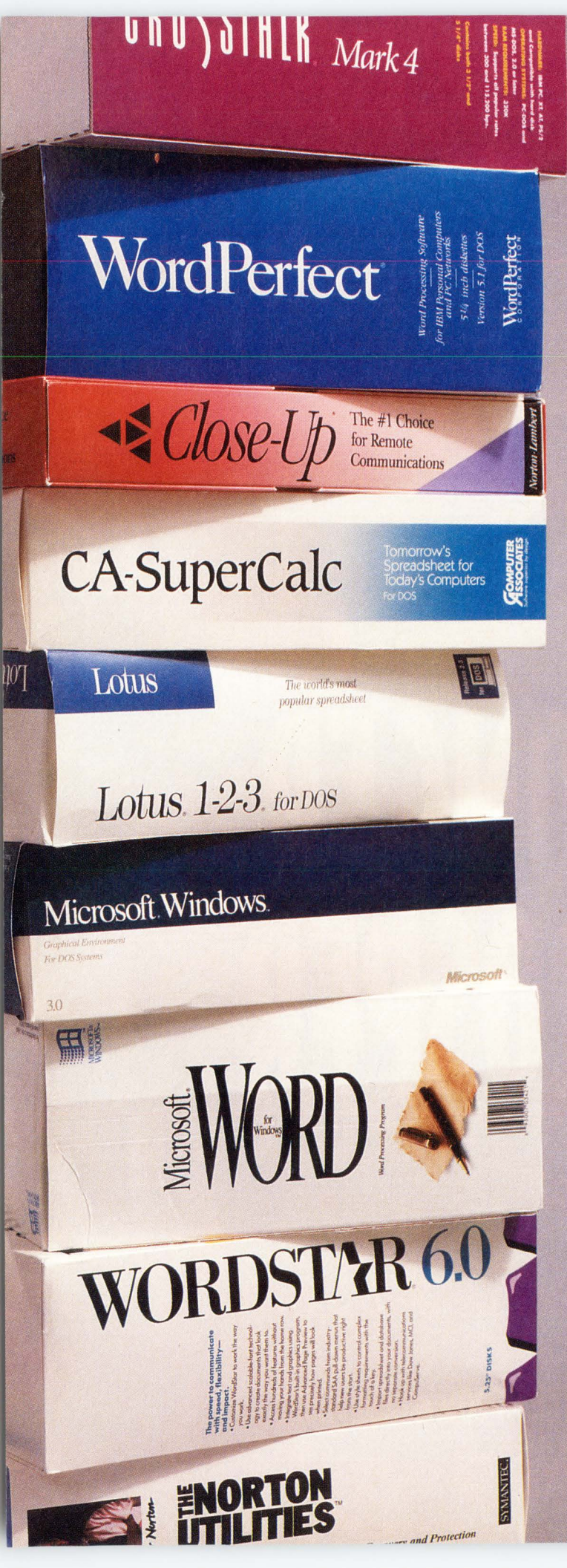
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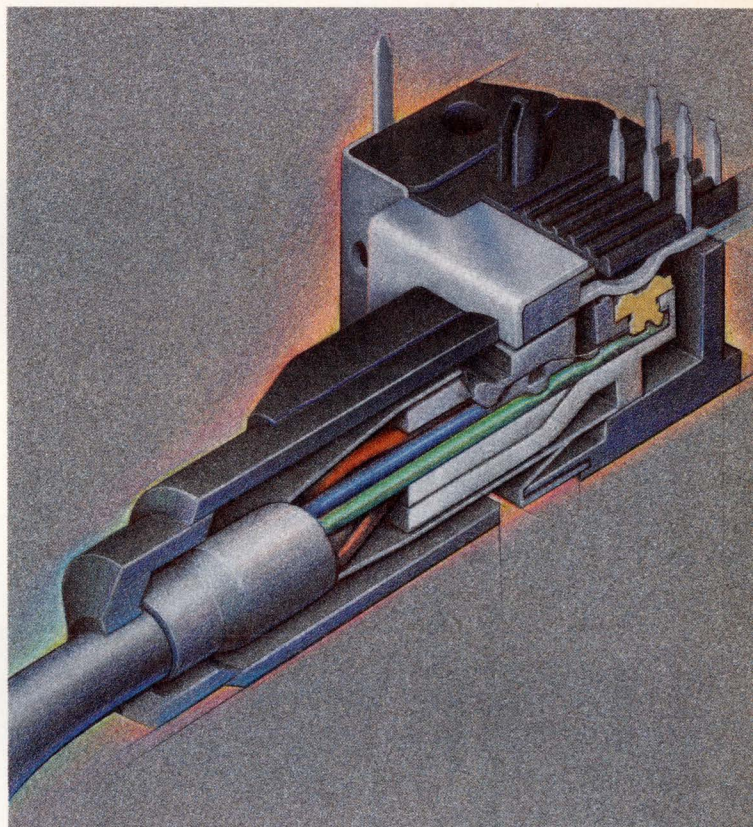
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CIRCLE NO. 77

Signal processing

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Designing an optimum signal-processing system means choosing components, both analog and digital, based on their relative strengths. Traditional—but not necessarily archaic— analog components can speed up systems and reduce complexity.

Anne Watson Swager, Technical Editor

Although it may seem that DSP is supplanting many traditional analog functions, very few signal-processing systems are purely digital or purely analog. Some analog preprocessing is almost always necessary, whether to amplify, buffer, or modify the signal prior to A/D conversion. The system designer's job is to determine which processing tasks analog and digital components perform most effectively. Using some traditional analog ICs to preprocess signals prior to A/D conversion can relieve the DSP μ P's processing burden, reduce system complexity, and ultimately produce a more efficient system. In addition to these ICs, novel signal-processing approaches present even

more design possibilities (see **box**, "Signal processors defy analog and digital stereotypes").

You shouldn't view traditional analog-processing ICs such as multipliers, logarithmic amplifiers, and RMS-to-dc converters as esoteric oddities. Although the circuit applications and the general functions of these ICs haven't changed much in recent years, these devices are by no means dead in the water. According to Barrie Gilbert, a well-known designer of many such circuits for Analog Devices, the latest versions of these devices are no longer academic curiosities and involve new concepts more aligned with today's applications. New designs with lower prices,

Take a new look at traditional analog-processing ICs—asking them to preprocess signals before A/D conversion will produce a more efficient system. (Photo courtesy Harris Semiconductor)

Signal processing

lower power, and high-speed performance make these components cost-, space-, and performance-effective for certain signal-processing applications.

A look at some of the tradeoffs between analog and digital signal processing puts these devices' usefulness into better perspective. Many criteria determine whether an analog or digital approach is best. These criteria may establish whether you design an all-analog processing system or, if you'll be using DSP, where in the signal-processing chain you digitize the signal.

Ultimately, both types of processing have their own unique advantages. As Michael Sedayao, applications engineer at Elantec, puts it, "Analog is the best *presentation* technology—you can't easily interface with 1's and 0's directly—while

digital is the best *processing* technology." You could amend this quote to say that digital is the best *postprocessing* technology. There still is an incredible need for analog preprocessing, such as amplification, level shifting, and dynamic-range reduction, prior to A/D conversion and digital processing.

High speed belongs to analog

Many performance and application features highlight the advantages of analog and digital processing. High speed is clearly analog processing's forte, with high speed in this case defined for any real-time, continuous signals sufficiently greater than 1 MHz. The speed limitations of digital processing lie in both the A/D converter and the DSP μ P. Measuring an ac signal requires an A/D converter that's fast enough to convert that signal. If a

fast enough converter doesn't exist, you can preprocess the data—depending on the application—with analog components, such as RMS-to-dc converters, and then digitize the resultant signal with a slower converter.

The converter's speed may not even be the problem. Many converters can digitize signals at sampling rates much higher than 2M samples/sec (enough to satisfy the Nyquist criterion for a 1-MHz signal), but no current DSP μ P has the speed or power to process continuous data at such speeds. Most of these high-speed converters operate in a burst mode, supplying high-speed data to the processor in small packets. DSP μ Ps can process bursts of high-speed data intended for repetitive measurements. The emphasis on speed of all analog manufacturers has become clearly

Signal processors defy analog and digital stereotypes

Start-up companies are pioneering several innovative approaches to signal processing. Two very different systems, one analog and one digital, are Comlinear Corp's Acoustic Charge Transport (ACT) technology and Star Semiconductor's Sproc processor and accompanying design tools.

Comlinear uses very-high-speed GaAs hardware and surface-acoustic-wave (SAW) technology to implement a variety of high-speed functions. The basic ACT device is essentially a transport channel that functions as a wideband tapped delay line. Such delay lines form the basis for a variety of signal-processing devices, including transversal (FIR) filters.

ACT technology (originally developed by Electronic Solutions Inc of Urbana, IL, which merged with Comlinear earlier this year) promises to deliver computational power of over 45 billion multiply-accumulates per second, high-megahertz sampling rates, programmability, compact size, no required A/D and D/A conversion (the technology is 100% analog), and low power (systems on the order of a few watts).

Proposed applications include pulse equalization and high-speed clock recovery for disk-drive read channels and adaptive filtering for digital audio broadcast. The first ACT-based part, due for introduction next month,

is a 127-tap programmable transversal filter with a sampling rate of 360 MHz. The 40-pin-DIP device will cost approximately \$750 (100).

The second, purely digital, processing technique uses a novel multiprocessing architecture: a central processor surrounded by memory. Not only is the Sproc processor architecture itself different from that of other DSP μ Ps, but Star Semiconductor's development tools don't require designers to become DSP programming and architecture experts. A cell library of high-level system blocks includes digital and analog functions. Any analog systems-level designer who starts with a block diagram of systems can implement that same function, given some performance exceptions, using the Sproc μ P.

The company recently announced a 50-MHz version of the Sproc 1400 processor (\$74 (1000)) and added more than 140 analog-and digital-processing functions in the cell library for its Sproclab development system (\$8950). The library includes a variety of cells, including peak detectors, filters, logic functions, mathematical operators, and signal generators. It also includes signal-conditioning blocks such as amplifiers, rectifiers, phase-locked loops, signal generators, and an AGC circuit.

evident: In addition to the processing ICs discussed here, low-cost, very-high-speed op amps are now abundant (Ref 1).

Analog suits fixed function

Analog processing is best for fixed, dedicated functions; DSP is clearly the choice for tasks that re-

quire programming or a complete change of processing algorithm—analogue to a complete change of circuit topology—on the fly. Analog processing does allow some degree of flexibility (using digitally programmable analog filters is one example), but this flexibility is limited to functions that you can implement

within a given circuit's basic topology. Digitally implementing control loops and servo mechanisms allows you to modify the control-loop algorithm easily.

Digital processing has a slight leg up on analog signal processing when it comes to precision. Analog precision is limited by gain errors, offset voltage, temperature drifts, nonlinearities, and instability. Filters and other analog functions implemented digitally don't suffer from such effects. However, in any digital-processing system, you can't ignore the errors incurred by A/D conversion. Every A/D converter has front-end signal conditioning, which can compromise the precision of any digital processor. Also, every A/D converter has a reference, and that reference is itself an analog component subject to drift.

Dealing with wide dynamic range

Wide-dynamic-range signals, including quite small signals, can be somewhat easier to deal with in the analog realm. For example, logarithmic amplifiers can effectively reduce the dynamic range of a signal prior to digital processing. Without such signal reduction, say for signals with ranges greater than 80 dB, the processing power and time necessary to deal with large numbers of bits becomes excessive.

A drawback to analog-processing components is that they can require trimming and adjusting, both of which are costly manufacturing activities. Many analog components designed to reduce the necessity for trimming are available in a variety of performance grades. However, the higher-performance grades can cost two to three times more than the lowest grade.

A subtle advantage of analog over digital is overload and noise recovery. Digital systems may need some sort of system reset after a noise spike on the input or power supplies, but analog components

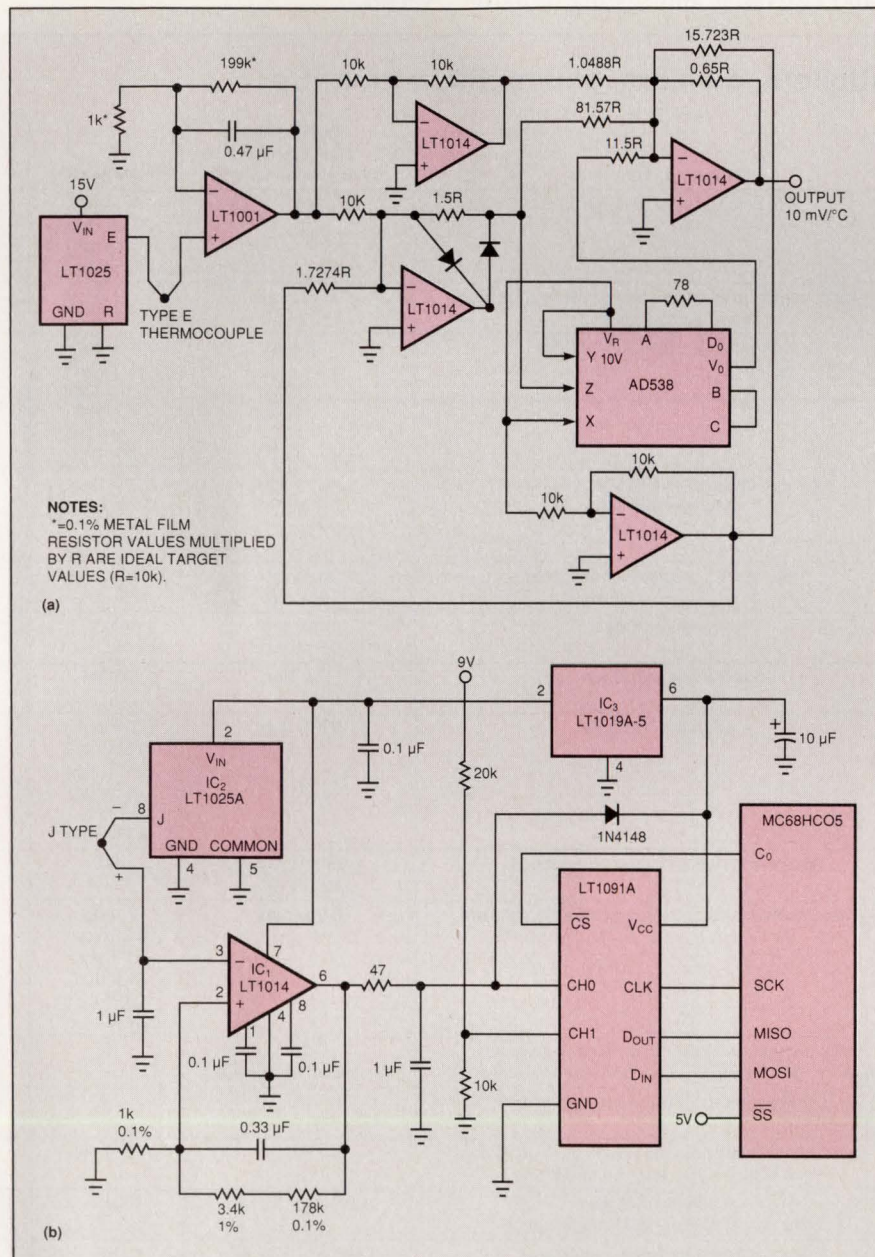


Fig 1—Two approaches to transducer linearization highlight the tradeoffs between analog and digital processing. Analog systems (a) can require trimming and expensive precision components, whereas digital systems (b) require some coding. Even the digital approach requires a surprising amount of attention to analog detail. (Courtesy Linear Technology Corp)

Signal processing

can recover more quickly from these events, assuming the components have sufficient input protection. Yet another subtle tradeoff is that analog processing gives you a choice: you can use a continuous-time or sampled-data technique. Digital is by definition only a sampled-data technique.

Other analog- and digital-processing design considerations, such as

reliability, size, space, power, and design time, depend entirely on the signals being processed. For high frequencies, analog components require less power than high-speed A/D converters. At low frequencies, the power required may be about the same. Design time between the two processing types isn't clear cut. Analog design can require hours for hand tweaking and testing of hard-

ware circuits. DSP, on the other hand, can require hours for writing and debugging software.

Comparing costs between analog and digital processing also depends on the input signal. In addition to the cost of the DSP μ P, you can't forget to consider the cost of front-end signal conditioning, such as the antialiasing filter and A/D converter.

Table 1—Representative multipliers, dividers, and multifunction ICs

Company	Part number	General description	Total error (% of full scale unless otherwise specified)	Nonlinearity
Analog Devices	AD534JH	Precision, 4-quadrant multiplier	$\pm 1\%$	Y input: 0.2% typ X input: 0.4% typ
	AD538AD	Analog computational unit that multiplies, divides, and takes exponents	$\pm 1\%$ of reading $\pm 500 \mu\text{V}$	NS
	AD633J	Low-cost, 4-quadrant multiplier	2% max	Y input: 0.1% typ 0.4% max X input: 0.4% typ 1% max
	AD734AN	High-accuracy, low-distortion, 4-quadrant multiplier/divider	0.1% typ 0.4% max	Y input: 0.025% typ X input: 0.05% typ
	AD834J	High-speed, 4-quadrant multiplier	0.5% typ 2% max	0.5% typ 1% max
Burr-Brown	DIV100JP	2-quadrant divider	0.3% typ 0.5% max	NS
	MPY100BM	4-quadrant multiplier/divider	1% max	0.08%
	MPY534KH	4-quadrant multiplier	0.5% max	Y input: 0.01% typ 0.1% max X input: 0.2% typ 0.3% max
	MPY600AP	Wide-bandwidth, 4-quadrant multiplier	$\pm 25 \text{ mV}$ (V_{OUT}) $\pm 88 \mu\text{A}$ (I_{OUT})	NS
	MPY634BM	Wide-bandwidth, precision 4-quadrant multiplier	0.5% max	Y input: 0.01% typ 0.1% max X input: 0.2% typ 0.3% max
	4302	Multifunction converter that multiplies, divides, squares, exponentiates, and performs trig functions	0.25% (multiplier and divider)	NS
Elantec	EL2082C	Current-mode, 2-quadrant multiplier	NS	NS
Exar	XR-2208CP/2228CP	Operational multipliers that combine 4-quadrant multipliers with a buffer and op amp	NS	1.0% max
Harris Semiconductor	HA-2546/7	2-quadrant multipliers (2546 has V output, 2547 has I output)	1.6% typ, 3% max	NS
	HA-2556/7	4-quadrant wideband multipliers (2556 has V output, 2557 has I output)	1.5% typ, 3% max	NS
Raytheon	RC4200	4-quadrant multiplier	2% max	0.1% max

Note:
NS=Not Specified

collector current and the base-emitter voltage.

A typical multiplier based around the Gilbert cell, such as the industry-standard 4-quadrant AD534 and MPY534, contains the following sections (Fig 3): a set of voltage-to-current converters for the X and Y inputs; a multiplying cell, which includes a set of matched current sources; a reference; and a differential amplifier. The converters produce linearly related currents from the X and Y voltage inputs. The multiplying cell produces two currents whose difference is proportional to the product of the input voltages. The amplifier converts this current difference to a single-ended output voltage. The AD534 also has a Z input, which allows you to add another signal to the output.

Many of the other multipliers in Table 1, including those from Burr-Brown and Harris Semiconductor, use the Gilbert-cell technique for multiplication. However, not all of the multipliers or devices in the table are made from this transduc-

tance mold. For example, Burr-Brown's 4302 and the AD538 implement the following transfer function using a log-antilog technique (the part multiplies and divides by subtracting and adding logs):

$$V_{OUT} = (V_Z/V_X)^m.$$

Elantec's EL2180 is also quite a bit different from the Gilbert-cell-based amplifier. This 2-quadrant device is a building block for gain-control circuits. Whereas the Gilbert-cell-type multipliers are voltage-in, voltage-out devices (they do work with current internally), the EL2180 has a current input and a current output. In most circuit applications, you would add an input resistor and an op amp to implement a specific function.

Spec includes feedthrough, offset

The total-error specification of any multiplier is the maximum difference between the multiplier's actual and ideal output values for any pair of dc input voltages within the

multiplier input range. Static error terms, such as input and output offsets, scale factor, feedthrough, and nonlinearity, add errors to the total error specification of the device.

Although total error is an all-encompassing specification, the individual error terms can be important for certain applications. As already mentioned, feedthrough is clearly important for those applications in which the output has to go to zero. Likewise, output offset is also important for these same applications if they are dc-coupled.

Nonlinearity is the maximum deviation of the output voltage from a straight-line transfer function. As you can see from the nonlinearity numbers in Table 1, the specifications for the X and Y inputs can be quite different for transconductance-based multipliers. These differences stem from the circuit topology of the translinear cell.

More than the name implies

Classifying the applications for multipliers is about as easy as classifying the uses for an op amp. Although some applications do call for multipliers to perform straightforward multiplication of two signals, multipliers are also useful for controlling voltage or gain, as either voltage-controlled amplifiers or gain-controlled amplifiers. Numerous multiplier data sheets and application notes give example circuits (Fig 4.)

Log amps compress signals

Another type of analog computational component is the logarithmic amplifier, or log amp for short. Log amps can be confusing (see Ref 6 for a clear and current discussion of log amps), and the confusion starts with their name. Log amps are not *amplifiers* in the usual sense of the word, because they are inherently nonlinear components.

Log amps are useful whenever you need to monitor a signal, control a signal, or compress a signal of large

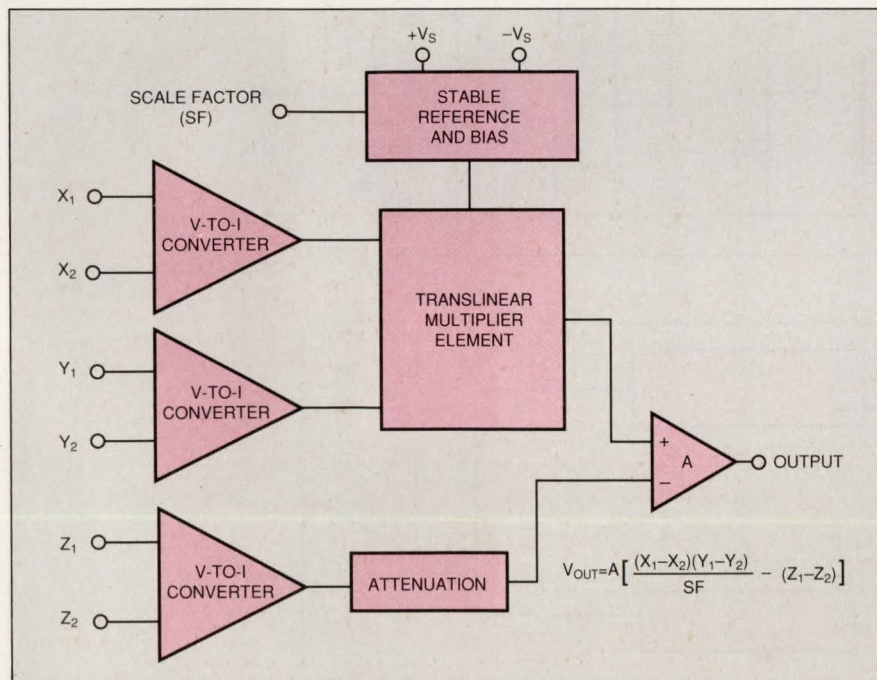


Fig 3—A typical 4-quadrant multiplier based on the Gilbert cell, such as the industry-standard '534, contains the following sections: a set of voltage-to-current converters for the X and Y inputs; a multiplying cell, which includes a set of matched current sources; a reference; and a differential amplifier.

Signal processing

dynamic range—of say 50 to 100 dB—to some smaller range. Log amps perform compression without any other controlling elements, such as AGC loops. Inserting a log amp in front of an 8-bit A/D converter can enable that converter to handle signals with large dynamic range, such as 16 bits or 96 dB.

Log amps fit into three basic categories (Ref 6): translinear, baseband, and demodulating. Most early

log amps were designed around the translinear principle discussed earlier. Burr-Brown's LOG100JP (\$36.05) computes the logarithm of an input signal by using the natural logarithm characteristics of the pn junction of a diode or transistor. This log amp features an input dynamic range of 6 decades and a 0.37% maximum total error over 5 decades.

The main liability of translinear-

based log amps is low bandwidth. Not only is their bandwidth fairly low, but it changes with input signal level (actually a problem for a number of nonlinear circuits). For example, as the input currents of the LOG-100JP decrease from 1 mA to 1 nA, the bandwidth decreases from 45 to 0.11 kHz. Thus, this type of log amp is useful primarily for low-frequency instrumentation applications.

Baseband and demodulating log

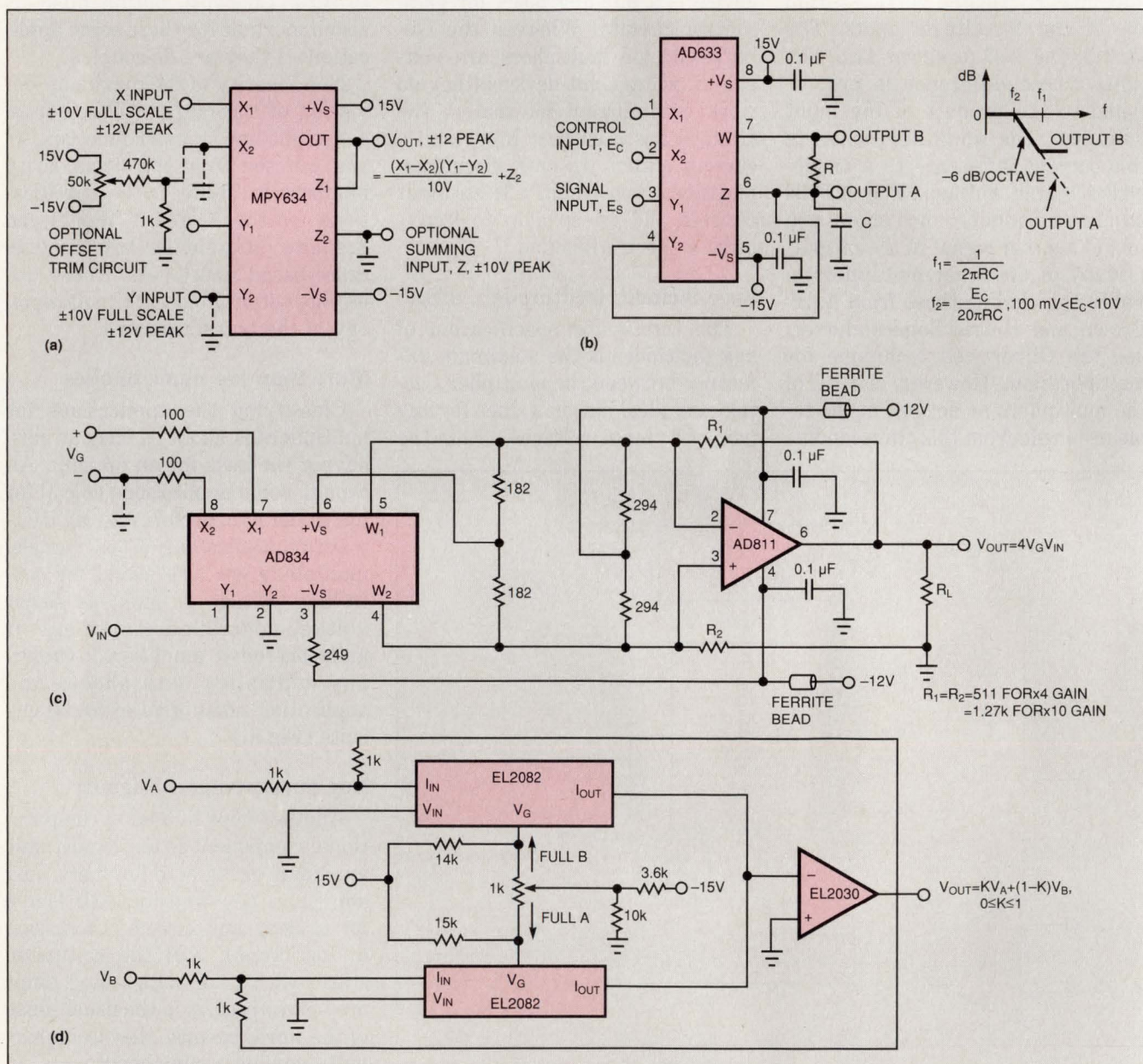
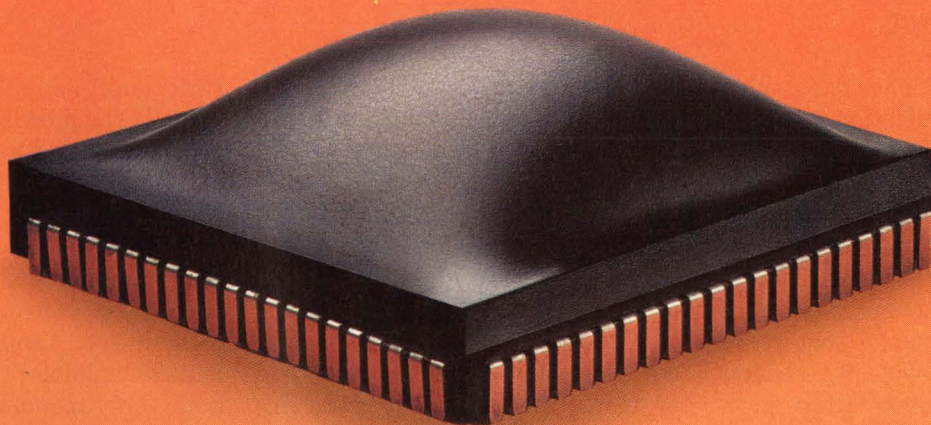


Fig 4—Multipliers comprise the basis of a number of application circuits. While you can certainly use multipliers to perform straightforward analog multiplication (a), multipliers can also implement voltage-controlled filters (b), 90-MHz voltage-controlled amplifiers (c), and linearized gain controllers/faders (d). (Courtesy Burr-Brown Corp, Analog Devices Inc, and Elantec Inc)



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Signal processing

amps have much higher bandwidths and suit communications applications. Baseband log amps produce a logarithmic output of the instantaneous value of some rapidly changing input. Demodulating log amps accept modulated, sinusoidal input signals and, using rectifiers, produce a quasi-dc signal that corresponds to the envelope of that input signal. Both achieve their high-bandwidth properties using a progressive-compression technique. This technique uses a chain of cascaded amplifiers, each having moderately low gain. Because each stage handles only a little of the overall log amps' gain, the bandwidth of each stage can be very high, leading to an overall response with high bandwidth.

Analog Devices' AD640 (\$29.95 (100)) and new AD606 (\$20 (100)) are demodulating log amps based on this technique and feature bandwidths of 120 MHz and 50 MHz, respectively. The AD606, introduced in September, features an 80-dB range, operates from one 5V supply, and requires 65 mW. The company designed the part primarily for digital-mobile-radio systems

to help measure the received RF power in handsets and base stations. However, the part is still fairly general purpose and will perform as a baseband log amp. You can use the part at audio frequencies by using some external capacitors.

RMS-to-dc converters do exactly as their name implies. Using one of three methods—thermal, implicit, or explicit—they convert the RMS level (power) of a waveform to a dc value. Just as with multipliers, RMS-to-dc converters have a variety of error sources. The important specifications for RMS-to-dc conversion are accuracy, crest-factor range, bandwidth, and dynamic range. The crest factor of any waveform is the ratio of its peak value to its RMS values. RMS converters have the same Achilles heel as translinear op amps; namely, bandwidth is a function of input amplitude.

The mathematical definition of RMS voltage is

$$V_{\text{RMS}} = \sqrt{V_{\text{IN}}^2}$$

Practically speaking, the RMS value is the amount of dc signal required to produce an equivalent amount of heat in the same load. Thus, the thermal method is the most conceptually basic. However, the implementation of a thermal RMS-to-dc converter is far from elementary. Linear Technology's LT1088 building block (\$13.95 (100)) is the only monolithic IC that uses the thermal technique. This part's fabrication technology is unusual because of the requirement of the die attach's thermal resistance. Making this resistance very high minimizes other internal mismatches within the IC. Thus, the company uses air-impregnated polymer as the die attach, which shows up as bubbles in a side-on die photo.

The thermal-conversion technique's main advantage is wide bandwidth. The LT1088 is not a stand-alone part, but when combined with a few amplifiers and passive components, it can achieve accuracy of 1 and 2% of full scale for signals from dc to 50 and 100 MHz, respectively, and handle crest factors of 50:1.

Manufacturers of signal-processing ICs

For more information on the signal-processing methods and components such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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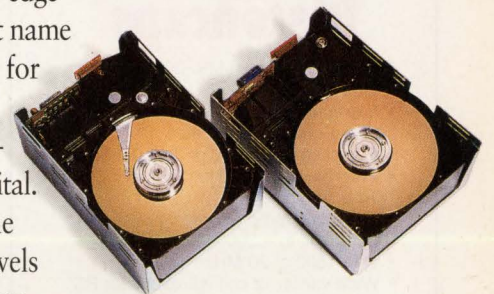
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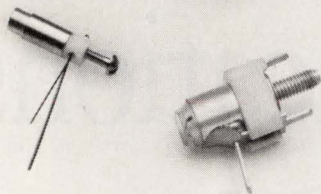
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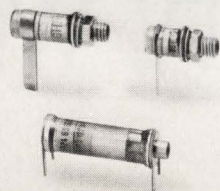
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Signal processing

Implicit and explicit conversion techniques either indirectly or directly perform the actual functions of the above equation: squaring, averaging, and square rooting. Because multipliers perform squaring functions, you can use multiplier/divider ICs to design RMS-to-dc converters. In fact, you'll find a number of RMS-to-dc conversion circuits in the application notes that accompany multiplier data sheets.

The AD736 and AD737 (starting at \$3.97 (100)) are Analog Devices' latest converters that can compute the *true* RMS value, the average rectified value, and the absolute value of a variety of input waveforms. The word *true* implies that these converters can accurately measure not only pure sine waves but other waveforms, including square waves, pulse trains, distorted sine waves, and noise. The converters require at most one external capacitor to perform these computations. These devices are suitable for portable instruments—most notably multimeters—because they feature power-supply current under 200 μ A and can operate with power-supply spans as low as 6V. For their rated accuracy of ± 0.5 mV, $\pm 0.5\%$ of reading, the converters handle input signals from dc to 1 kHz and handle signal crest factors up to 5.

Multipliers (and their relatives), log amps, and RMS-to-dc converters are just three types of special-function analog components. Many other specialized devices, such as dedicated voltage-controlled amplifiers (Analog Devices, Burr-Brown, and Comlinear,) voltage-to-frequency converters (Burr-Brown,) trigonometric-function converters (Analog Devices), and integrating devices (Burr-Brown), exist. Keeping an eye on the continuing developments of these ICs and perusing through what you might think are

obscure additions to analog-component data books may provide you with some surprising signal-processing circuits. **EDN**

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Acknowledgment

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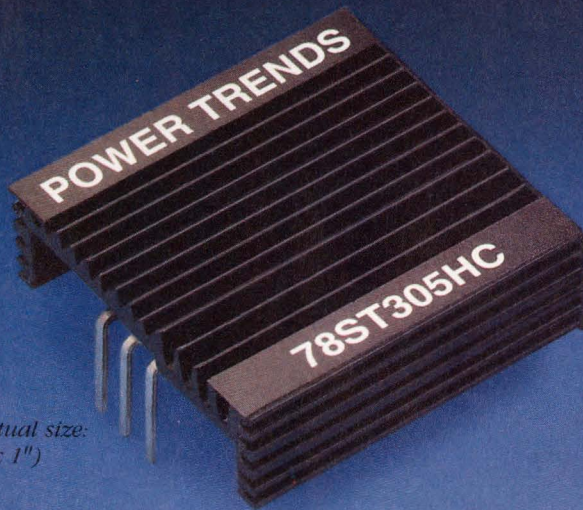
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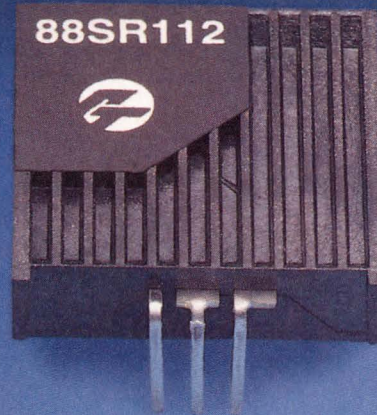
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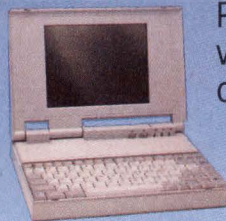
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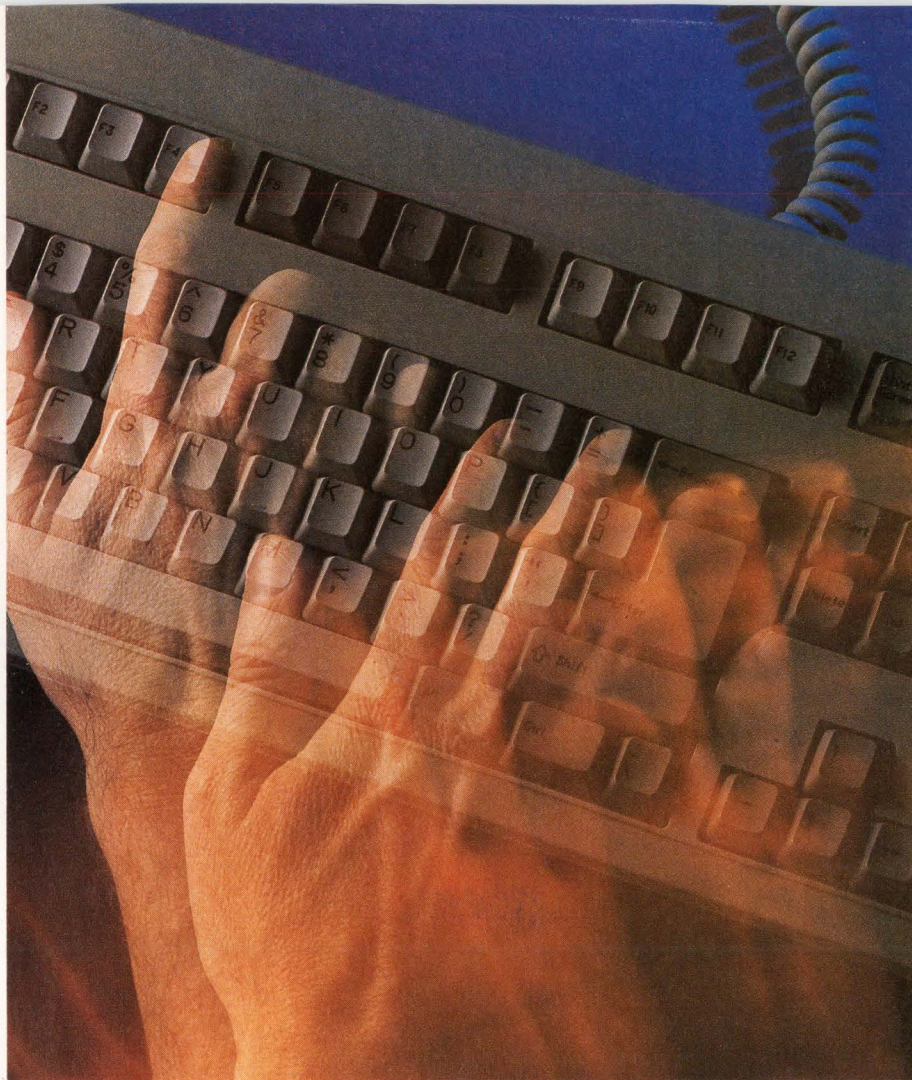


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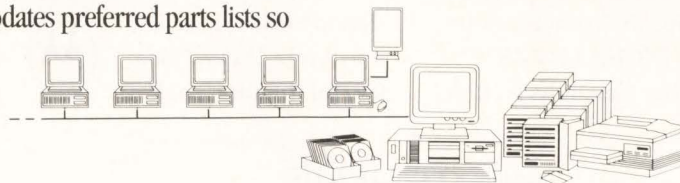


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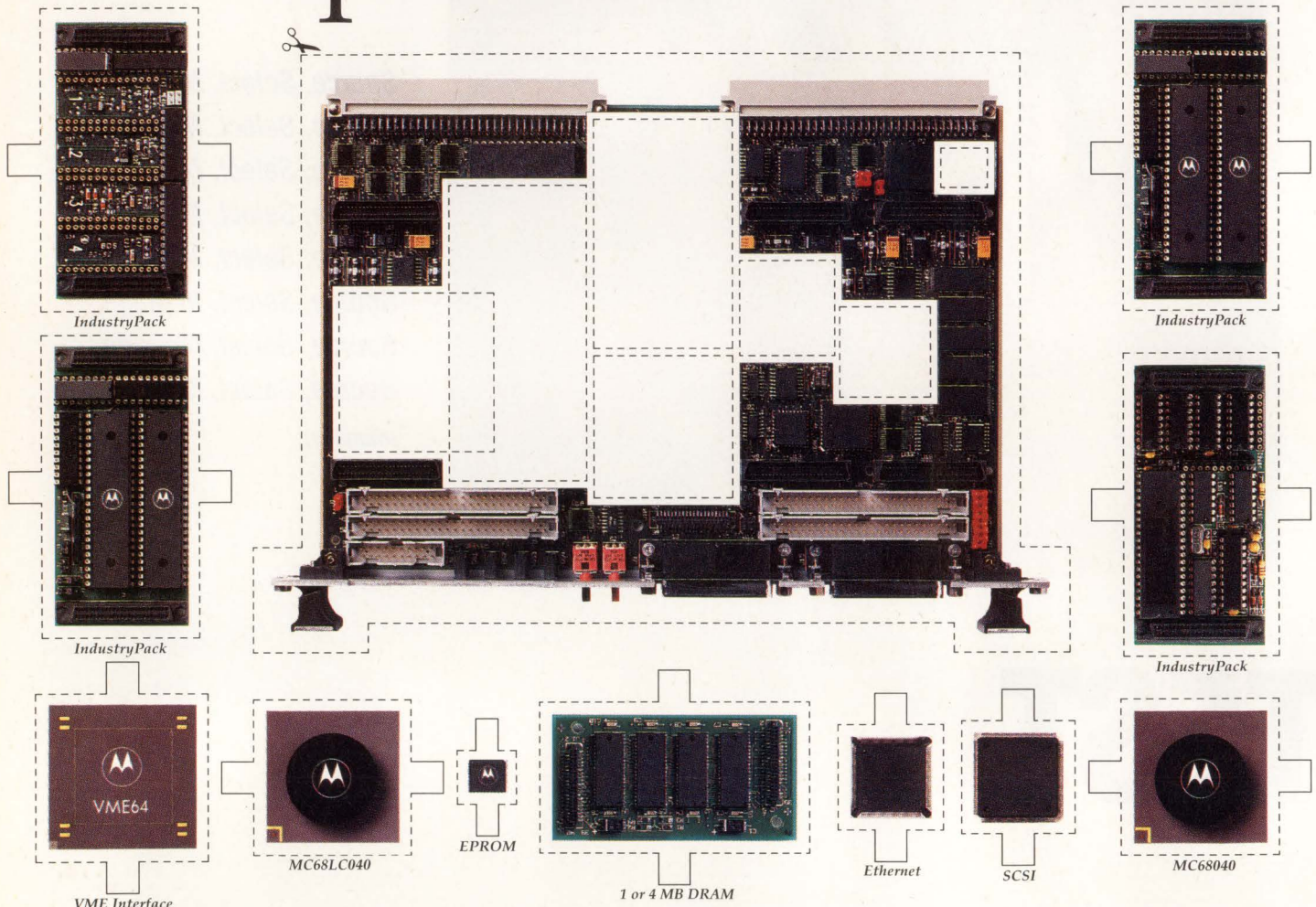
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GARY LEGG, Senior Technical Editor

Wescon/92's short courses and technical sessions let you concentrate on one technology and branch out to others.

Five separate electronics conventions, each one specializing in a single technology area, are on tap at this year's Wescon. The annual show will be held in Anaheim, CA, from Tuesday, November 17, to Thursday, November 19. The convention will feature product exhibits and technical sessions in electronic components, ICs and semiconductors, test and measurement, design automation, and electronic production, as well as several short courses.

Exhibits and technical sessions for the five shows are under one roof at the Anaheim Convention Center, and a single ticket provides access to all. Short courses for technical and personal development, which start on Monday, November 16, will be held in the Anaheim Hilton Hotel.

Several special events will reflect Wescon's theme, the business of change in the electronics industry. In the keynote address, Hughes Aircraft Co Chairman and Chief Executive Officer C Michael Armstrong will discuss technology transfer from military to commercial markets. Armstrong will speak in the Anaheim Convention Center on Tuesday, November 17, at 11 am.

Throughout the show, officials of Wescon and the US Department of Commerce (DoC) will conduct activities that promote international business opportuni-

ties between manufacturers and buyers of electronic products and services. Additional events will include a post-election economic forecast (Wednesday at 2 pm) and sessions on advanced technologies (Tuesday through Thursday).

The sessions on advanced technologies augment five other session tracks, one for each of the "mini" Wescon conventions. The separate shows are:

- IC Expo—for manufacturers of ICs and semiconductors
- Computools—addressing computer tools for engineers
- EC World—covering passive electronic components, packaging, and interconnect
- ITM—International Test and Measurement
- EPEX—Electronic Production Expo.

All together, the six technical-session tracks encompass about 40 individual sessions (**Table 1**).

Most of the Wescon short courses cover technologies that are in rapid transition (**Table 2**). Fuzzy logic, neural networks, object-oriented software engineering, surface-mount technology, biomedical engineering, and fiber optics are some of the key topics.

There are also career-oriented courses, including "High technology corporate dynamics for women engineers" and, perhaps wryly pertinent to the existing US economy, "How we all found jobs." Short courses last either a day or half a day.

Wescon's theme of change in the electronics business will be highlighted by emphasis on global markets and international alliances. Show manager Jane Cook pre-

Table 1—Technical-session schedule

		IC EXPO	Computools	Advanced Technologies	EC World	ITM	EPEX
Tuesday	9 am to 11 am	IC-1 High-performance clock networks	CO-1 Network performance management	AD-1 Outlook 2000	EC-1 Practical advanced technology application for electronic packaging	IT-1 Bus-based instrumentation and the SCPI standard	EP-1 International issues
	12:30 pm to 2:30 pm	IC-2 High-performance logic in the 90s		AD-2 Applications for fuzzy logic	EC-2 Are multichip modules (MCMs) for real?	IT-2 Test strategy innovations for the 90s—tutorial	
	3 pm to 5 pm	IC-3 Cache technology today: from notebook to 67-MHz file servers		AD-3 Emerging technologies—where is the automotive industry heading?—panel	EC-3 Microprocessors in embedded control applications	IT-3 Insight into applications of IEEE 1149 test standard	EP-2 SMT/FPT processing
Wednesday	9:30 am to 11:30 am	IC-4 FPGA/EPLD architectures	CO-2 EDA and design technology for high-complexity ASIC-based systems	AD-4 <i>EE Times</i> emerging technologies	EC-4 Flat-panel display technology	IT-4 ASIC test: prototyping emulation and verification	EP-3 Process improvement: six-sigma and beyond
	12:30 pm to 2:30 pm	IC-5 IC design advances for portable systems	CO-3 Design automation for very-large-ASIC design	AD-5 The reality of virtual reality—I	EC-5 High-performance batteries I: portable applications	IT-5 Integrated-circuit test and emulation	
	3 pm to 5 pm	IC-6 BiCMOS goes mainstream	CO-4 FPGA tools	AD-6 The reality of virtual reality—II (hands-on workshop)	EC-6 High-performance batteries II: design issues and high-power applications	IT-6 Instrumentation and measurement technology—the decision to test	EP-4 The impact of the "American with disabilities act" on engineering and manufacturing
Thursday	9:30 am to 11:30 am	IC-7 DRAM architecture for high-speed data transfer	CO-5 EDA component libraries—future directions—panel	AD-7 Digital video technology			EP-5 Environmentally conscious manufacturing I: alternative materials and processes
	12:30 pm to 2:30 pm	IC-8 Innovations in specialty memories		AD-8 Electronic applications of high-temperature superconductors			EP-6 Environmentally conscious manufacturing II: process waste reduction, recovery, and recycling

Table 2—Short-course schedule

Monday November 16	SC1 9 am to 1 pm Design-oriented analysis methods: a survival course	SC2 9 am to 12:30 pm High-technology corporate dynamics for women engineers	SC3 9 am to 5 pm Technical career management	SC4 9 am to 3 pm How we all found jobs	SC5 9 am to 5 pm Design for testability
Tuesday November 17	SC6 9 am to 5 pm Total quality and R&D in the 90s (Parts 1 and 2) Part 1: Total quality in the DoD environment Part 2: Weapons-systems acquisitions update	SC7 9 am to 5 pm The Demeter method for object-oriented software development	SC8 9 am to 1 pm Biomedical engineering: where the engineering disciplines are needed and what is occurring in this exploding field	SC9 9 am to 5 pm Faster new-product development	
Wednesday November 18	SC10 9 am to 5 pm Concurrent systems architecting and engineering	SC11 9 am to 5 pm Surface-mount and fine-pitch technologies	SC12 9 am to 5 pm Introduction to neural networks and fuzzy information-processing systems	SC13 9 am to 1 pm Electronic cooling	
Thursday November 19	SC14 9 am to 5 pm An introduction to fiber-optics systems design	SC15 9 am to 5 pm Use of Spice power for modern analog simulation	SC16 9 am to 1 pm A management briefing on CASE		

What Wescon/92 attendees need to know

Here's the basic information you'll need if you attend Wescon/92:

Exhibits: Anaheim Convention Center from 9 am to 5 pm Tuesday, November 17, and Wednesday, November 18; 9 am to 4 pm Thursday, November 19.

Technical sessions: Anaheim Convention Center from 9 am to 5 pm Tuesday, November 17, and Wednesday, November 18; 9 am to 2:30 pm Thursday, November 19.

Short courses: Anaheim Hilton Hotel, full-day (9 am to 5 pm) and part-day short courses Monday, November 16, to Thursday, November 19.

Fees: Regular admission free to qualified preregistrants, \$10 at the door. Covers all exhibits and technical sessions. Short-course tuition is \$40 to \$250 per course for advance registration, \$50 to \$300 at the door. Advance registration is advised.

Parking: 2000 to 3000 spots at Anaheim Convention Center for \$5 a day, additional parking at Hilton and Marriott hotels for \$7 a day.

Transportation: Shuttle buses between the convention center and several nearby hotels.

For more information: Phone (800) 877-2668 or FAX (310) 641-5117.

dicts that 15 to 18% of this year's Wescon attendees will be foreigners, up from 12% last year. Cook expects 18 to 20% of exhibitors will be foreign companies, many of them supported by their governments and trade agencies.

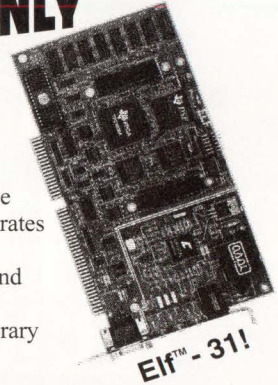
Capitalizing on Wescon's international mix, the show's organizers are assisting the DoC with its Foreign Buyer Program. In that program, DoC officials work with US embassies and consulates to match foreign buyers with US companies. Wescon representatives work with DoC officials, foreign trade representatives, and show attendees to set up consultations.

Wescon officials expect more than 1250 exhibitors at the show and predict attendance of 45,000. **EDN**

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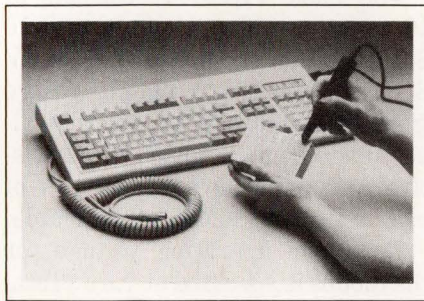
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The G80-1600 also includes separate cursor and numeric keypads, synchronous-data format, mode-selection switch located under the keyboard, and international availability in a variety of languages. \$289.

Cherry Electrical Products, 3600 Sunset Ave, Waukegan, IL 60087. Phone (708) 360-3599. Booth 2157. Circle No. 402

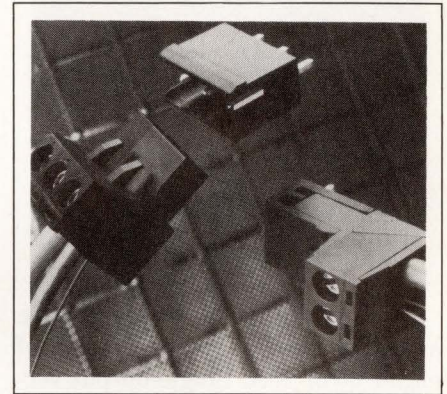
Disk set

This custom CD-ROM (compact-disk read-only-memory) set will contain Philips/Signetics ICs and discrete semiconductor components, unabridged scanned databooks including errata sheets, specifications, and application notes. The disk set contains a subset of the CAPS (computer-aided-product-selection) semiconductor database including part numbers of Philips/Signetics competing manufacturers. The database will be parametrically searchable, letting users cross-reference competing part numbers.

CAPS is a networkable component-selection management system that lets engineers select the best components available for a new design. It lets you identify equivalent devices and alternative sources, find MIL-spec parts, and ensure that a specified part is still in production; it also lets you look up obsolete components and identify equivalent replacements. CAPS provides query-driven access to more than 1.5 million components and hundreds of thousands of manufacturers' data sheets, techni-

cal specifications, and applications data.

Cahners Technical Information Service, 275 Washington St, Newton, MA 02158. Phone (617) 558-4999. FAX (617) 630-2168. Booth 2240. Circle No. 403



Terminal blocks

Series 86 and 87 Eurostyle terminal blocks are 2-piece plug and header systems that are polarized with the industry-standard scalloped design. The units are interchangeable and intermateable with competitive pluggable terminal blocks.

The plug in the Eurostyle system features rising cage pressure clamps that hold wires with a positive grip. The clamp compresses the wires uniformly at any location in the cage. Wire-size capability ranges from #12 to #30 AWG.

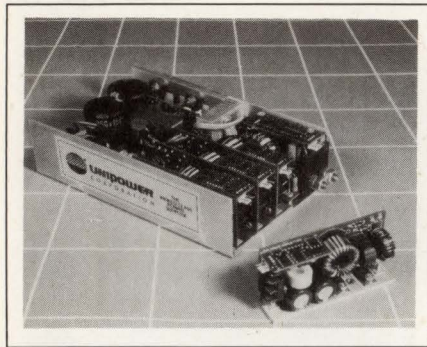
The terminal blocks are available in sizes of 2 to 12 positions. Terminal spacings equal 0.2 in. and 5 mm for Series 86 and 87 terminal blocks, respectively. The blocks conform to VDE specifications; UL and CSA approvals are pending. \$0.44 (250) per mated line.

Beau Interconnect Systems, Box 10, Laconia, NH 03247. Phone (603) 524-5243. Booth 1490. Circle No. 404

Power supplies

Uniflex Series 500W open-frame switching supplies are made up from three output modules. These

modules have wide adjustment ranges that span nominal voltages of 2 to 6V, 5 to 15V, and 15 to 36V. The modules also feature independent overvoltage and overcurrent protection.



Multioutput Uniflex supplies are available with 5V main outputs of either 60 or 70A. Single-output versions have 2-, 3.3-, 5-, 12-, 15-, and 48V outputs. Line and load regulation equals 0.1% and ripple and noise measure 1%.

Standard supply features include remote sense on all outputs, current share, power-good signal, remote inhibit, jumper-selectable 115/230V ac input, power limit, thermal shutdown, and Class A EMI input filter. Options include a universal input, Class B EMI filter, and rear- or top-mounted dc fan. \$480 to \$690. Delivery, stock to six weeks ARO.

Unipower Corp, 2981 Gateway Dr, Pompano Beach, FL 33069. Phone (305) 974-2442. FAX (305) 971-1837. Booth 2542. Circle No. 405

Function generator

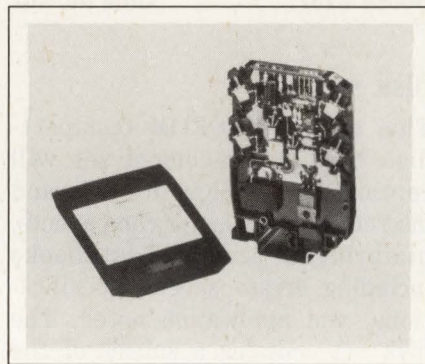
Model 2003-485 has dc to 1.6-MHz frequency range with five selectable waveforms and six operational modes. Frequency stability is guaranteed at ± 10 ppm with 10 digits of resolution. Output waveforms include sine, square, triangle, and ramp. Functions include full internal sweep capabilities programmable for linear or log mode across the entire frequency range. The digitally controlled output is 20-mV

p-p into an open circuit or 10 mV into a 50 Ω load.

The computer interface on the 2003-485 lets you set and retrieve all generator modes and parameters from a PC or any computer equipped with an RS-485 serial port. The interface accommodates as many as 32 devices on a single bus in a daisy-chain fashion.

The generator has facilities for stand-alone operation. The unit has a 32-character LCD with a keypad and rotary tuning knobs for selecting functions. \$750.

Global Specialties, 70 Fulton Terrace, New Haven, CT 06512. Phone (203) 624-3103. FAX (203) 468-0060. Booth 2656. Circle No. 406



Electromechanical relay

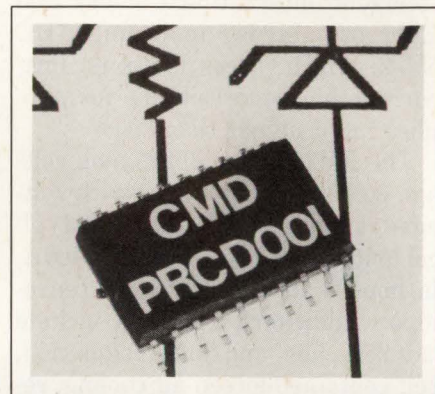
Long Life electromechanical relays (EMRs) are rated for 20 million full-load operations even with inductive loads—200 times longer than a typical EMR. The relays owe their extended life to a patented fabrication technique that prevents contact failure.

The family includes two models that operate with a 24-V dc input and feature 5A contacts. The ORA and ORC can switch loads as high as 1250-VA ac and 300W dc, respectively. The I/O isolation for both models equals 3 kV, and operating range spans -20 to +52°C for the ORC and -20 to +58°C for the ORA.

Long Life relays are 9 mm wide, allowing DIN rail mounting of 33

relays per foot. Both models feature an LED status indicator. \$39.

Entrelec, 1950 Hurd Dr, Irving, TX 75038. Phone (800) 431-2308. Booth 1778. Circle No. 407



Surface-mount networks

PRCD001 Series surface-mount resistor-capacitor-diode networks are fabricated using a blend of thin-film and semiconductor technology. The devices are highly stable, have low-noise characteristics, and suit use in high-speed logic termination and EMI/RFI-filtering applications.

The basic PRCD001 consists of 16 resistors, 16 capacitors, and 16 Schottky diodes housed in a 20-pin SOIC. Resistance values range from 10 to 150 Ω and capacitor values range from 25 to 250 pF. Resistive and capacitive tolerances of ± 5 , ± 10 , and $\pm 20\%$ are available.

Maximum operating voltage for the diodes is specified at 7.5V. Total package power dissipation equals 140 mW. The package uses four ground pins to minimize lead inductance. \$5 (10,000). Delivery, eight weeks ARO.

California Micro Devices Corp, 215 Topaz St, Milpitas, CA 95035. Phone (408) 263-3214. FAX (408) 263-7846. Booth 2085. Circle No. 408

Pushbutton switch

Series 644-2100 switches accommodate four T-1 subminiature flange-base lamps or LEDs. The switches

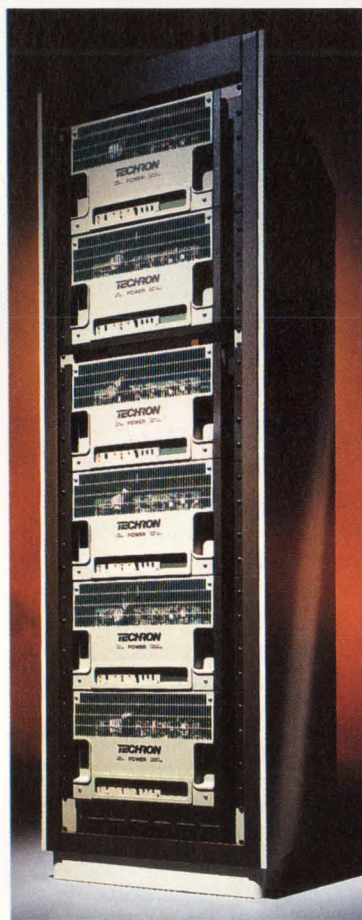
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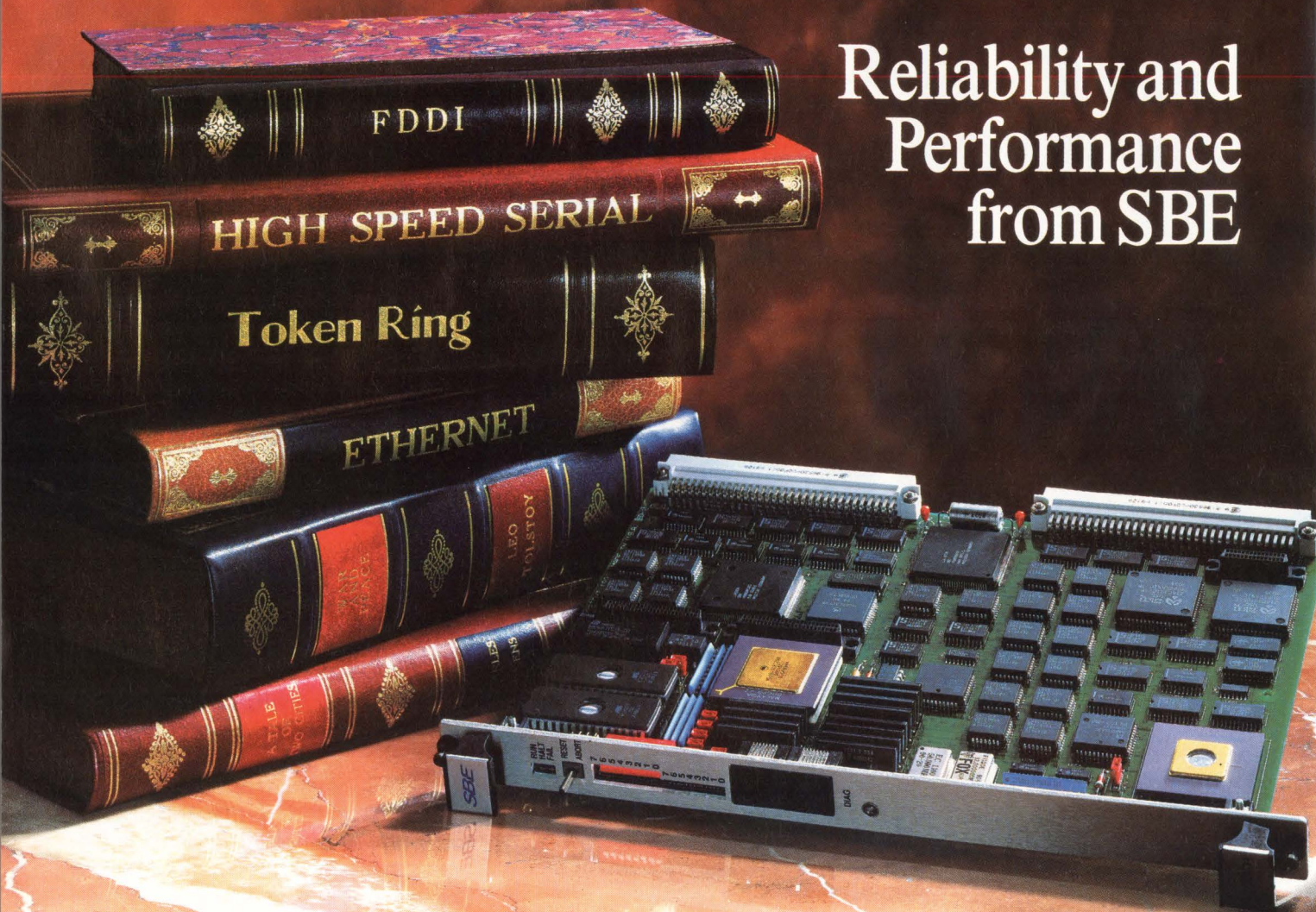
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SBE, Inc., 2400 Bisso Lane, Concord CA 94520

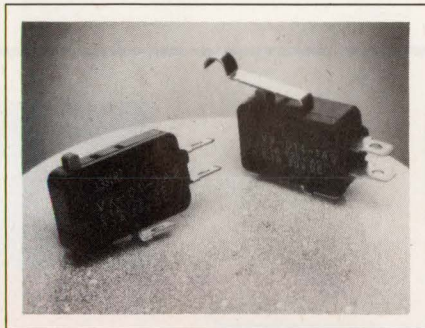
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Communications &
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are available with spst or dpdt switching functions; contacts are rated for 30V dc or 115V ac at 2A resistive or 0.5A inductive.

The 644-2100 switch mounts in a 0.698-in. square panel opening using a case that slides on from behind the panel and attaches to the switch with a locking arm. The locking arm is tightened with a screw located beneath the lens. Hidden and split legends are available and matching indicators and push-to-test indicators are available for front-panel display consistency. The switch has a 2-lb operating pressure and is designed to meet MIL-5-22885 requirements. \$40 (100).

Electro-Mech Components Inc,
1826 N Floradale Ave, South El Monte, CA 91733. Phone (818) 442-7180. FAX (818) 350-8070. Booth 2587.

Circle No. 409



Switches

VX Series snap-action switches feature a low 15 to 50g operating force—important for quick-response switching in vending machines, appliances, arcades, and other consumer and commercial applications. The spdt devices are available in 5 and 0.1A versions.

The 5A (Model VX-5) and 0.1A (Model VX-01) devices have a lifetime specification of 500,000 and 1,000,000 operations, respectively. Operating speeds range from 0.1 mm to 1 mm/sec. Operating frequency equals 60 actuations per minute and operating range spans -25 to +80°C.

Contacts for the 5A versions are rated to handle 250V ac or dc; the 0.1A models will handle 125V ac or 30V dc. Both models carry UL and CSA ratings. \$0.79 (1000). Delivery, 10 to 12 weeks ARO.

Omron Electronics Inc, 1 E Commerce Dr, Schaumburg, IL 60173. Phone (800) 826-6766. FAX (708) 843-7787. Booth 1134.

Circle No. 410



DC/DC converters

These triple-output 30W converters operate on inputs of 10 to 20V, 18 to 36V, or 36 to 72V and provide two independent, synchronized output sections. Each of the single- and dual-output sections are completely isolated from each other and independently regulated. Total output accuracy equals 2%.

Efficiency for the converters equals 85%. I/O isolation meets the UL 1459 mandated value of 1544V dc. The units operate over a -40 to +85°C range. A convenient on-off control pin is provided for portable applications. The converters are housed in a 6-side shielded case that measures 2.58 x 3.01 x 0.83 in. \$98 (100).

Calex Mfg Co Inc, 2401 Stanwell Dr, Concord, CA 94520. Phone (800) 542-3355. FAX (510) 687-3333. Booth 1391.

Circle No. 411

Spectrum analyzer

Model P-7802 spectrum analyzer determines RF signal frequency and levels generated by sources from 1 to 1000 MHz. It features a ±1% accuracy and 1-MHz reso-

lution for center frequency display.

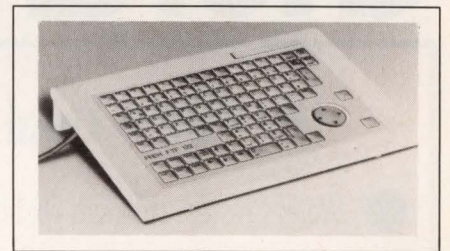
The analyzer features a 0.1 to 100 MHz 10-step scanning band at 3 dB per band. Scanning band accuracy equals ±6% below 100-MHz center frequency and ±10% above 100 MHz. Amplitude measuring range is rated at 15 to 129 dBμ. CRT amplitude is 15 to 80 dBμ and you can set panel switches from 80 to 129 dBμ. The CRT readout has a megahertz- and kilohertz-bandwidth display. \$3500.

Protek, Box 59, Norwood, NJ 07648. Phone (201) 767-7242. FAX (201) 767-7343. Booth 2650

Circle No. 412

Sealed keyboard

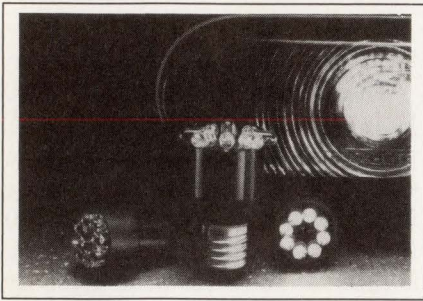
The FTF122 sealed keyboard features a built-in mouse device and is waterproof and dustproof enough to meet the European IP 65 rating. The electronics are encapsulated and the unit is available in either height-adjustable housing or as a stand-alone unit for custom installations. Both versions work with IBM PC/XT, PC/AT, PS/2, or compatible systems and they run Windows software.



The keyboard features color-coded function keys and tactile feedback for easy operator use. The English version is standard and is available from stock. Foreign versions are optional on a special-order basis. A standard-programmer software disk that lets users completely reprogram the keyboard is available. \$325.

Preh Electronic Industries Inc, 470 E Main St, Lake Zurich, IL 60047. Phone (708) 438-4000. Booth 1384.

Circle No. 413



LED bulbs

S600, B600, and DB600 Series of solid-state 15-mm LED clusters can replace standard incandescent bulbs in many applications. When configured in clusters of 9 to 40 red LEDs, the units are suited for tail-light, side-marker, and warning-light replacements in transportation applications, and they are direct replacements for red-orange incandescent bulbs in military applications.

The 15-mm S600 LEDs feature a screw-type base and the B600 and

DB600 LEDs are packaged in a bayonet-type base. All units are available in multichip 9- to 40-LED clusters in direct-mount, single- or double-contact, or double-contact-index versions. The LEDs are available in high-efficiency, super-bright, and infrared versions or with a built-in resistor for direct 5 to 130V ac operation. From \$12.50 to \$15 (1000). Delivery, stock to six weeks ARO.

Ledtronics Inc, 4009 Pacific Coast Hwy, Torrance, CA 90505. Phone (310) 549-9995. FAX (310) 549-4820. Booth 1336.

Circle No. 529

Trimmer capacitors

Series 47000 Giga-Trim devices are extremely small multiturn trimmers designed for tuning RF and microwave circuits. The line has been value-engineered to provide a

component for cost-conscious commercial applications.

As an example, the traditional sapphire dielectric has been replaced by ceramic without a significant change in Q or performance range. The units also feature a patented self-locking constant torque-tuning mechanism.

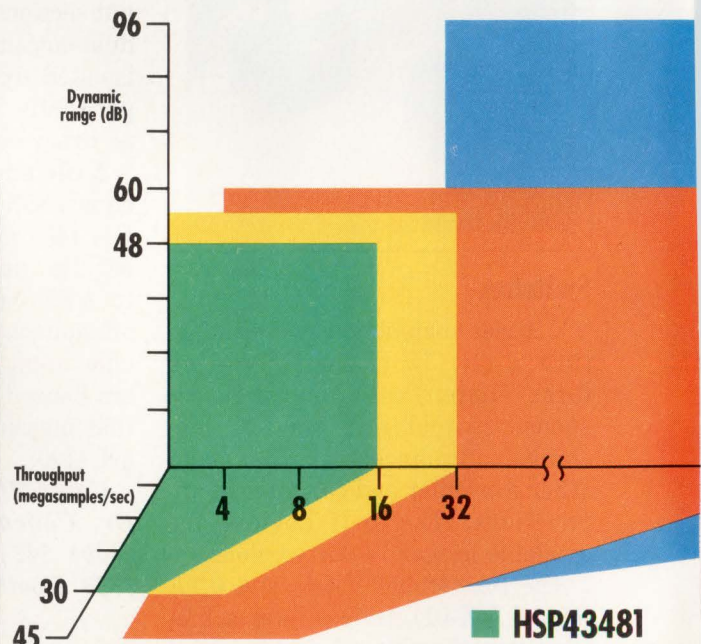
Selected mounting styles are available on tape-and-reel for surface-mount applications. The 47000 Series capacitors are supplied with either a removable cap or a poke-seal. The poke-seal replaces the O-ring design and provides greater reliability. The units have a 500V voltage rating, Qs of greater than 2500 at 250 MHz, and operate over a -65 to +125°C range. \$6 (1000). Delivery, six to eight weeks ARO.

Johanson Manufacturing Corp, Rockaway Valley Rd, Boonton, NJ 07005. Phone (201) 334-2676. Booth 1255. Circle No. 530

CHOICE FIRS

HSP43168 Dual FIR Filter

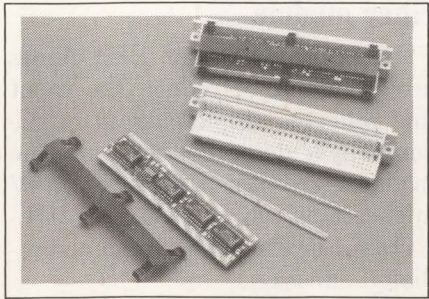
- World's fastest standard FIR filter at 45 MHz
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Nobody gives you more choices in programmable FIR filters than Harris. From the

45 megasamples per second throughput of our HSP43168, to the 512,000-equivalent-tap

precision of our HSP43220, Harris has a FIR filter that meets your digital filtering needs.



Connector

The Active Eurocard Connector is a pc board-to-backplane connection system that lets you mount a daughter card having active circuits on the connector. The right-angle connector attaches to the pc board via 126 solder tail pins on a 0.1-in. pitch. The VMEbus- and Multibus II-compatible connector mates with all standard Type C Eurocard DIN backplane connectors having 96 pins on three rows.

By incorporating active devices on the connector, you can shorten

the signal path from an IC to the backplane. The shorter distance can improve signal integrity and reduce bus loading effects caused by distributed capacitance and inductance. The active connector also frees up board space for other components, which is helpful for dense board designs.

The connector housing can withstand infrared and vapor phase soldering processes. The connectors two metal-on-elastomer strips fit into housing grooves to connect the daughter card to the connector. The card can hold customer-supplied ICs or devices the company supplies. The connector's phosphor-bronze contacts have a minimum of 30 μ in. of gold plating. \$14 to \$15 excluding active devices (OEM).

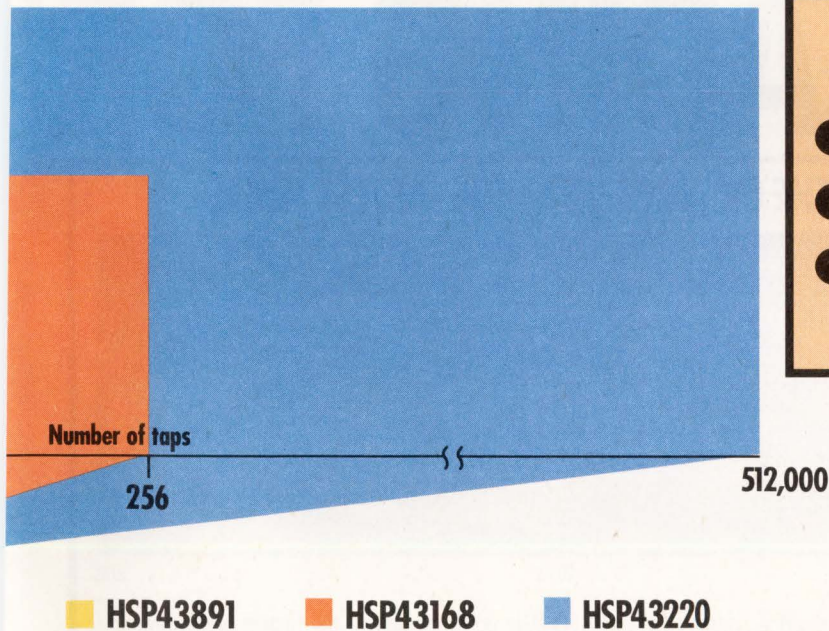
AMP Inc, Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752. Booth 1043.

Circle No. 531

Panel meter

A-3000 Series DPMs can measure 12 different electrical or physical parameters and provide several types of outputs. The design consists of a basic DPM chassis, which incorporates the digital display (3 $\frac{1}{2}$ digit), operational circuitry, and power supply. Into this basic chassis, users can plug input circuit modules to characterize the instrument for any of the following roles—voltage or current meter, ac average voltage or current meter, ac true-rms voltage or current meter, frequency meter, thermocouple monitor, ohmmeter, resistance-temperature detector, process monitor, or strain gauge.

Several ranges are available for each measured parameter. The complete set of input modules has 54 different range options. Common specifications include a 15/sec conversion rate, leading zero suppression,



HSP43220 Decimating Digital Filter

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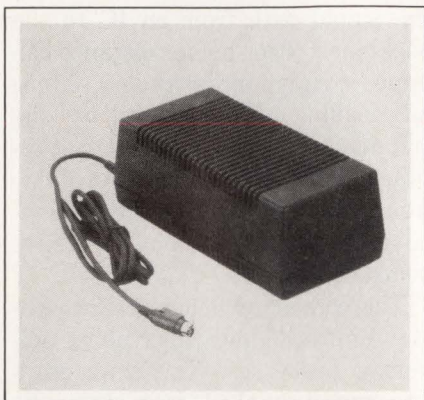
and decimal point adjustable to any digit position. \$141 for the basic chassis; \$44 to \$154 for modules.

Selco Products Co, 7580 Stage Rd, Buena Park, CA 90621. Phone (714) 521-8673. FAX (714) 739-1507. Booth 2660. Circle No. 532

Power supplies

The SWA Series of external power supplies includes 15-, 20-, and 30W wall plug-in and 40- and 60W cord-to-cord units. The cord-to-cord models have a universal input of 90 to 264V ac; plug-in units are available with inputs of 90- to 132- and 198- to 264V ac.

All models offer outputs of 5 to 17.5V dc and deliver as much as 4A. All units feature overload protection with automatic reset. Typical operating efficiency equals 65 to 70% and ripple and noise range from 100 to 200 mV p-p.



Built-in EMI circuitry meets FCC part 15J Class B and VDE 0871 Class B emission levels. All models have been certified to meet the safety requirements of UL, CSA, VDE, and MITI. From \$39 and \$78 for the plug-in and cord-to-cord models, respectively.

Tamura Corp of America, 1150 Dominguez St, Carson, CA 90746. Phone (213) 638-1790. FAX (213) 638-9956. Booth 3478. Circle No. 533

Filter module

FMD/FME-461 Series EMI filters are designed to reduce the input line reflected ripple current of the company's dc/dc converters. The modules are aimed at 28 or 270V applications, which must meet MIL-STD-461 levels of conducted and radiated emissions.

When combined with the company's converters, the filters reduce input ripple current by 30 dB at 500 kHz and by more than 50 dB from 1 to 50 MHz. All filters in the line protect against spikes as high as $\pm 600V$ (50Ω source impedance) for as long as 10 μ sec. The 28V parts will pass 100V transients without being damaged. The 270V parts will pass on $\pm 500V$ transients without being damaged.

The FMD/FME filters are rated for inputs of 16 to 40V dc and 160 to 270V dc. All modules operate over the full -55 to $+125^\circ C$ mili-

SPEED READING FOR

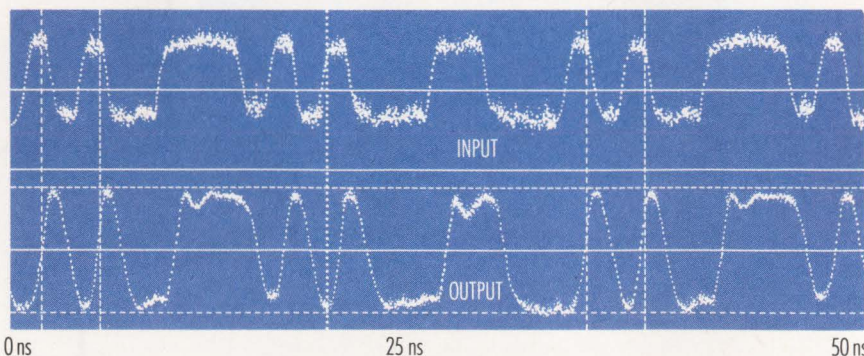
No one does megahertz so megafast. Because Harris monolithic devices give you -3 dB bandwidths up to 850 MHz. Plus excellent gain flatness of 0.14 dB to 100 MHz.

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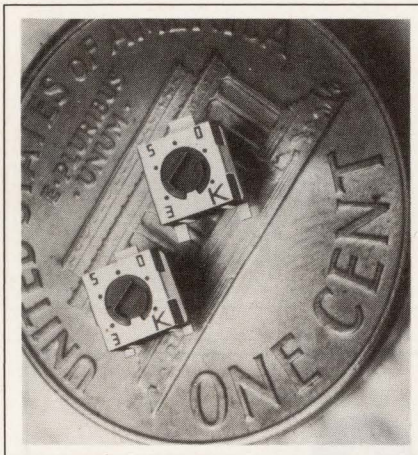
tary operating range. The units are housed in metal hermetic side-leaded packages. The 28V models are also available in down-leaded packages. From \$250 (100).

Interpoint Corp., Box 97005, Redmond, WA 98073. Phone (206) 882-3100. FAX (206) 869-7402. Booth 3180. Circle No. 534

Resistive trimmers

The microminiature, surface-mountable trimming potentiometers in the G3 Series measure 3.4×3.2 mm and have an above-board profile of 2 mm. Resistance values for the trimmers range from 100Ω to $1\text{ M}\Omega$. Standard tolerance equals $+20\%$.

The trimmers in the G3 Series are available in two mounting styles. The A version features J-lead terminations while the B version has gull-wing terminations. All units are rated for 125 mW at 70°C , and



they have a -55 to $+125^\circ\text{C}$ operating range. The trimming potentiometers are sealed to withstand soldering and immersion processes per MIL-R-22097. \$1.50 (1000). Delivery, six to eight weeks ARO.

Tocos America, 565 W Golf Rd, Arlington Heights, IL 60005. Phone (708) 364-7277. FAX (708) 364-7317. Booth 1636. Circle No. 535

Power supplies

The MPS Series of $N+1$ redundancy power supplies includes four 350W models. All units feature a zero-wire power-sharing system. The system uses a nondissipative droop regulator that automatically shares output power and ensures glitch-free operation. Because there is no third-wire connection, and no master or slave units in the configuration, zero-wire paralleling is truly redundant.

The units in the MPS line feature three or four outputs. The main output delivers 5V at 50A. The second provides 12V at 8A, and the third output delivers -12V at 4A. The fourth output can be -5.2V at 2A, 12V at 2A, or 24V at 1.5A. Outputs two and three are fully regulated using the company's exclusive Magna-Flux switching magnetic amplifier post regulators. Output four uses a 3-terminal linear regulator. \$366 (100).

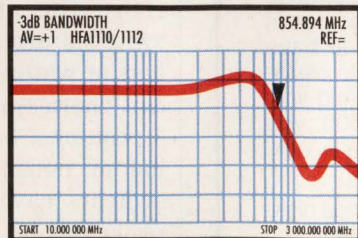
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Product: HFA5250 Pin Driver
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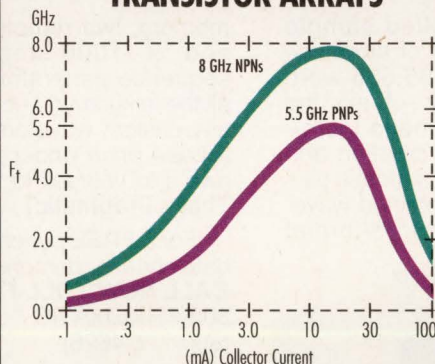
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Our HFA1110/1112 buffer amps offer wide bandwidth and gain flatness of 0.14 dB to 100 MHz.

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Selectable gain	unity	$+2, \pm 1$
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Pinout	Std. buffer	Std. op amp
Price (100s)	\$5.95	\$5.95

TRANSISTOR ARRAYS



For extremely fast NPNs and PNP's on a single die, Harris transistor arrays are available as high-performance analog cells, enabling you to design your own differential amps, S/H s, comparators, mixers and more.

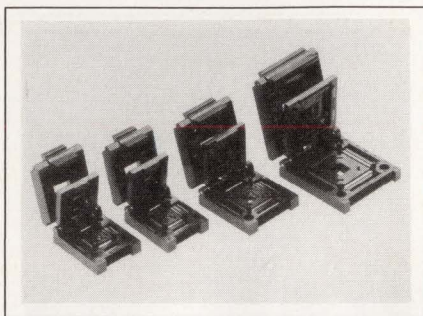
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Delivery, four to six weeks ARO.
**Todd Products Corp, 50 Emjay
 Blvd, Brentwood, NY 11717.
 Phone (516) 231-3366. FAX (516)
 231-3473. Booth 2278. Circle No. 536**



IC Sockets

The QP1 Series of small outline sockets are designed for 0.5-mm

pitch plastic-, thin-, and metric-quad flatpacks. The sockets are suited for high-density test and burn-in service. The line includes units for packages with 80, 100, 144, and 208 pins.

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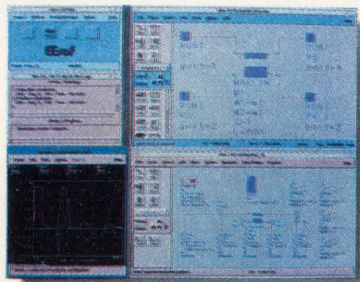
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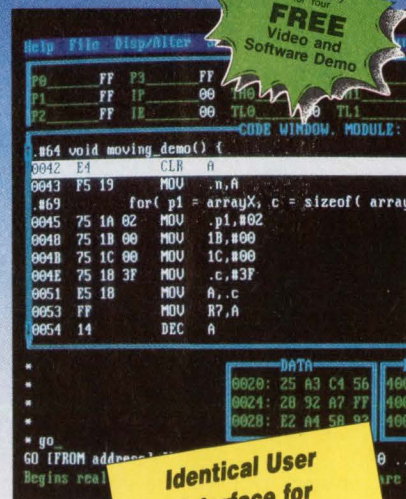
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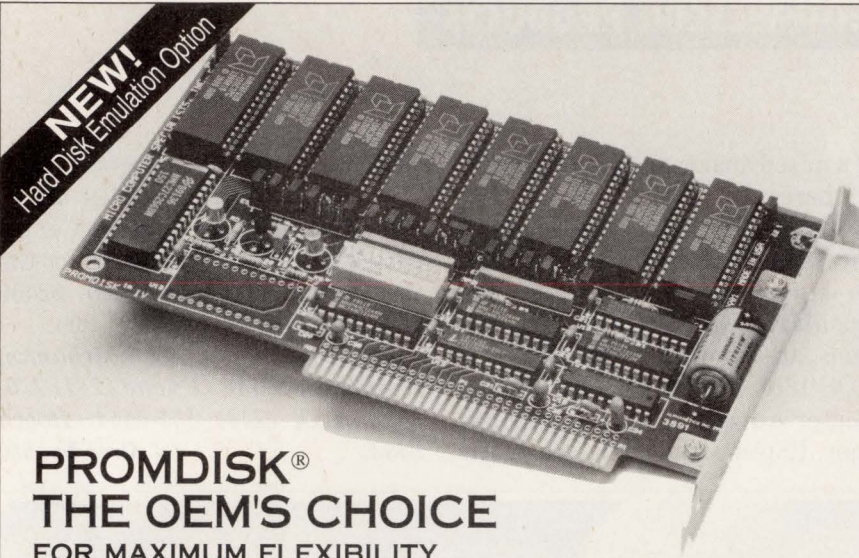


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CIRCLE NO. 185

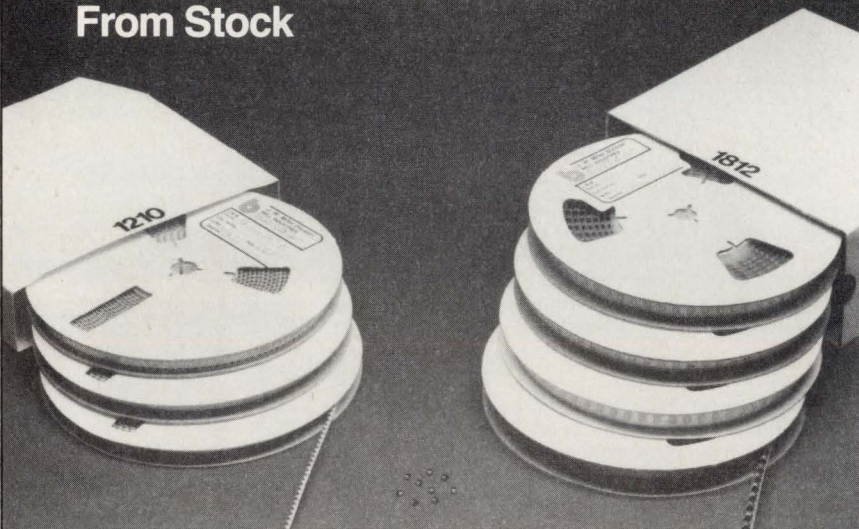
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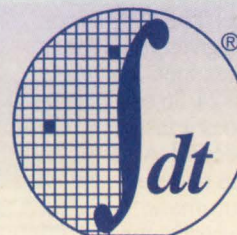
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*Specs are for '244 device

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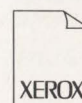


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CIRCLE NO. 96

Rigorous testing of SCSI disk drives and arrays ensures peak performance

Herbert W Silverman, Peer Protocols Inc

Thorough testing can distinguish your SCSI disk drive or array from your competitors' by ensuring that your product meets its performance, reliability, and data-availability goals.

The enormous complexity of creating disk subsystems using disk-array technology and SCSI-2 command-queuing facilities challenges the designer, the test engineer, and the SCSI test-equipment manufacturer. Despite this complexity, you can overcome the potential pitfalls and assure that your design meets its objectives if you include thorough performance testing throughout the product's life cycle: from initial concept to field support.

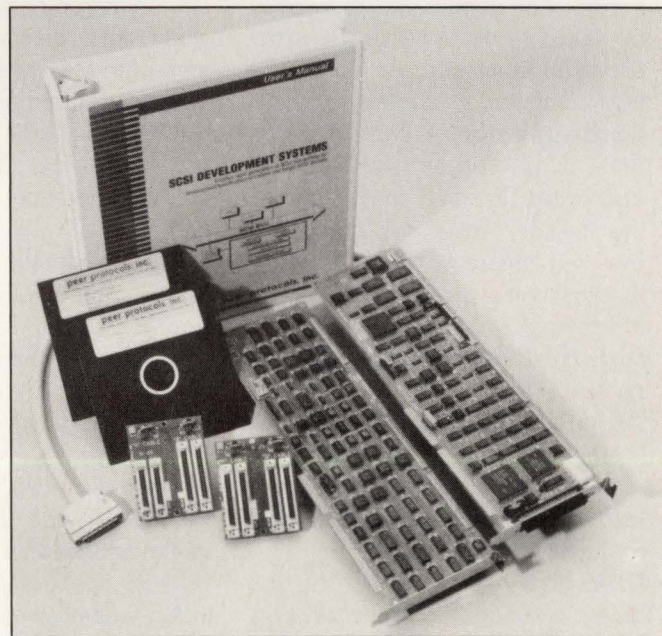
The major phases in a product life cycle are development, manufacturing, distribution, and field support. All of these phases require some sort of test technology, but the development phase is the most demanding. Test methods and equipment that meet all development-phase test requirements can usually support the needs of the other phases, with two restrictions:

First, development-phase tests and tests used during other phases should be compatible in all ways and should allow the transfer of hardware and software from one phase to another.

Second, a test's ease-of-use is always important and becomes increasingly so as you move from development through manufacturing, distribution, and support.

However, as you move through the product's life cycle, emphasis shifts from the ease of creating tests to the ease of running the tests and interpreting the results.

Development testing of a complex disk drive or disk-array subsystem can take almost as long as the rest of the development effort and often consumes one-third of the development resources.



SCSI disk test adapters such as this Model 7000 from Peer Protocols Inc can help you extract peak performance from new disk-drive and -array designs.

SCSI disk testing

Usually, disk-drive and disk-array development breaks down into seven stages:

1. Measure existing systems to determine where performance can be improved. The product life cycle starts with performance measurements of existing system operations to identify the system bottlenecks. These tests should help you determine whether a queuing device or other architectural changes can help overall system performance. Typical measurements at this stage include the disk-command-arrival rate, the LBA (logical block address) distribution, and the block size. For SCSI-based systems, a passive bus monitor can help make these measurements.

2. Develop queuing algorithms and other strategies to overcome the system bottlenecks you identified in stage 1. Use the insight you've gained from measurements of existing systems plus the benefits of new technologies to improve on existing designs. Define cache size and caching strategy, group size, and striping strategy (logical/physical disk arrangement and stripe depth) to take best advantage of your system's data-block transfer size and performance requirements.

Trading off data availability, performance, transaction rate, and transfer size is a very complex task. In fact, you may not find one optimal solution. Some disk

arrays use a "redundancy group" in which each member of the array's storage group optimizes a different set of parameters. For example, one storage unit may optimize performance at the expense of data availability. Several redundancy groups may be present in one disk array for access through different SCSI LUNs (logical unit numbers).

3. Simulate or model the new design. You may need to use device simulations or system models including individual component parameters and the interaction characteristics of these components in larger systems such as disk arrays.

4. Build the queuing system, disk array, or disk drive. You may need feasibility implementations or breadboards because modelling an entire system is very complicated. Simple simulation models may not reveal all the aspects of system operation.

5. Test individual units. Implementing a disk array subsystem requires many person years of engineering effort. Software internals in some data-storage products require several hundred thousand lines of C code operating within the environment of a real-time control system. Often, you need multiple microprocessors to meet performance, reliability, and data-integrity requirements. You can minimize the inevitable system

Glossary

Command queuing—A SCSI-2 facility that permits the disk array or disk drive to optimize the processing of commands issued by the host computer.

Cache memory—RAM in a disk drive or disk array used to buffer operations. In some configurations, this memory holds disk data, thus avoiding physical disk accesses if the host computer requests data already held in the cache.

Deferred write—In this mode of cache operation, the host computer transfers data to the cache and can immediately proceed with subsequent operations. The disk or disk array later writes the cached data to the physical media.

Disk array—A collection of disk drives arranged to optimize performance, data availability, and data reliability.

Phase—an element of the SCSI

protocol that defines the SCSI bus state during a command. Phases include data, command, status, and message. Message phases perform flow control and error recovery between the initiator and the target.

Initiator—The device that starts a SCSI operation. Usually the host computer.

I/Os—Input/output operations.

LBA—Logical block address. An addressing unit for SCSI devices. The host computer views a SCSI disk as a contiguous range of LBA numbers starting from 0, with an upper value that is the logical capacity of the disk or disk array.

LUN—Logical Unit Number. A method to split up a SCSI device's address space. LUNs may operate independently within a SCSI device.

RAID—Redundant array of independent disks.

SCSI—Small computer system in-

terface. An industry-standard bus to interconnect computers and peripherals. SCSI-2 is the second and current version of the SCSI standard.

SCSI exerciser—A test instrument that simulates a host computer or target device. It has the ability to emit SCSI commands and illogical SCSI phases, as well as insert error conditions that a real SCSI device cannot normally produce.

Stripe depth—The amount of contiguous storage on each element of a disk array as the data is spread across parallel drives.

Target—The SCSI device that responds to an initiator's request. Usually the disk or disk array.

Transfer length (or request size)—the amount of data (usually the number of LBAs) requested in a specific command from the host computer.

problems associated with this tremendous software complexity through the judicious placement of internal test points that help you test individual system components as you integrate them.

6. Test the system. Once the components have been integrated, perform "black box" testing to ensure that the product meets its functional specifications with respect to SCSI command compliance, performance, data integrity, and the user interface.

System testing is complicated by the many combinations and permutations of host, drive, partitioning, and RAID levels. It is impractical to exhaustively test all of these possibilities, so the key to a successful system test plan is the selection of configurations that will stress boundary conditions and design weaknesses. Use knowledge of the design to judiciously choose test points and conditions.

Run performance and stress tests on the system in several simulated environments and selected configurations. Host systems generally cannot push storage subsystems to their limits, so stress testing usually calls for test equipment specifically designed for high-performance SCSI command generation and monitoring in addition to the end-user systems running benchmarks and application programs.

7. Measure system performance in a live environment. During this final development stage, test your design to see whether the system meets overall system requirements and determine if it is, in fact, a useful product. Tune if necessary.

Architectural design and modelling

Mathematical models, not tests, drive design concepts for storage subsystems. These models include queuing models, statistical models, and parametric

models of the system (disk drive or disk array). Combinations of disk drives and bus configurations provide a vast number of modelling opportunities, making it nearly impossible to completely model all of the factors governing the operation of a complex disk array. You can develop partial mathematical models and simulations to help design the system, but the combined use of hardware models, system emulations, and disk-drive emulations often provides a more attractive alternative. Hardware emulation lets you construct a system and then tune your design based on a combination of observed and simulated behavior.

As Fig 1 shows, disk drives in a prototype disk array may be physical disk drives, simulation models, or drive emulations. A SCSI test adapter running in target mode can emulate a disk drive. The test adapter appears as a disk to the host or disk array. Using a SCSI test adapter in this manner lets you modify drive behavior under operator or program control. This approach lets you introduce drive errors and bus errors in a controlled manner to thoroughly test error paths.

Although the use of drive emulations provides significant benefit in measuring the functional characteristics of the host or disk array, drive emulators have their limitations. For example, PC-based SCSI test adapters may use a DOS file for the emulated disk drive's storage, but that approach incurs a speed penalty. Conversely, if the test adapter uses on-board RAM to emulate disk storage, its emulation speed may be adequate, but data storage space will be limited.

The ideal SCSI disk-drive emulation uses a known data pattern throughout the drive so that the test system can reconstruct a comparison pattern without having to access a data file. However, this approach is not always practical when emulating disk arrays

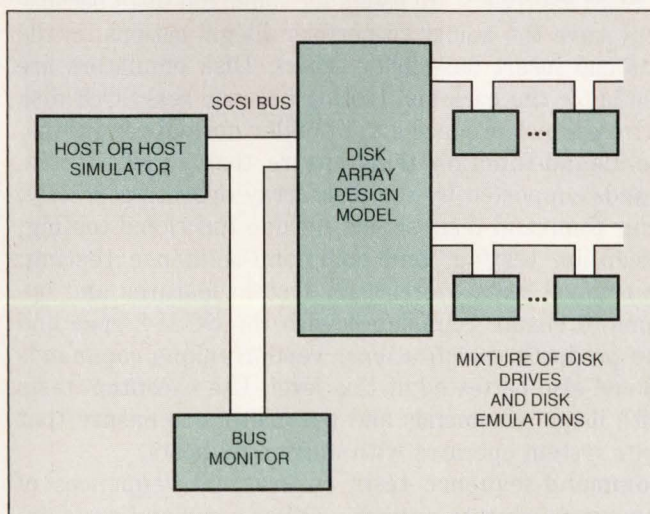


Fig 1—Hardware modelling of a disk array lets you tune your design before building a complete prototype.

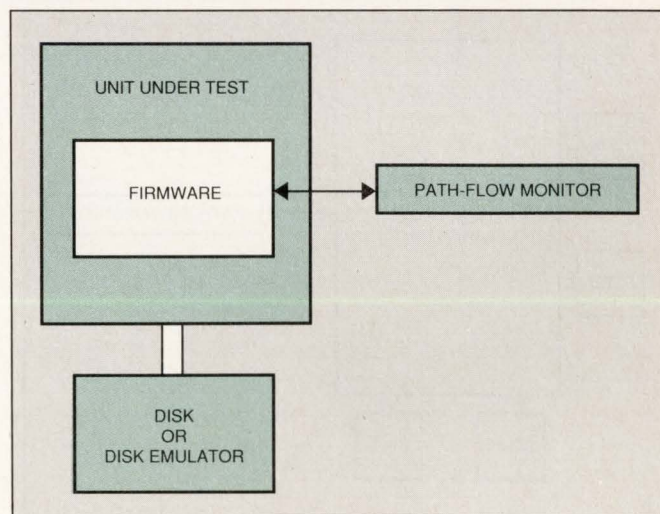


Fig 2—Unit testing saves you time during the integration phase of development.

SCSI disk testing

because the array controller may insert additional information into each data block. This control information must be retrieved intact from the emulated media.

Using test equipment to help model the disk array lets you construct a system and operate it while still defining system goals, operating parameters, and architecture. Tuning the system at this stage could prevent a major overhaul of the system architecture should the original design fail to meet objectives.

Unit testing

Perform unit tests on the individual disk-array components as they near completion (Fig 2). Testing of these components (caching logic, data reconstruction logic, etc) individually will reduce overall system-integration time. Component testing (hardware and firmware) should exercise all major subsystems to their parametric limits. To fully exercise all input parameter ranges, you may need to use simulation test stubs around individual code modules. Test stubs are often easier to vary than the modules or hardware they replace.

You may also need aids such as path-flow monitors to ensure that testing has exercised all paths within a software module. Path-flow monitors (sometimes called performance analyzers) track a processor's program counter and show you the portions of your code that have executed. Fig 3 shows a simplified hardware/firmware component-test environment that uses a path-flow monitor.

Unit testing presumes that completely testing an individual module's input combinations is easier than for the complete product. At the very least, testing at this level must prove that all of the modules will operate over the entire range of every input parameter

and with all combinations of range extremes. For example, unit tests should prove that the largest block size will work with the smallest cache size, and vice versa. It may be easier to construct test stubs than to create physical systems with the necessary variations. You can then independently control all stub parameters for tests. As you integrate more of the disk array's components into a system, testing should continue to prove that the individual elements will operate for all possible values and all combinations of extremes.

System testing

System tests treat the disk array as a "black box" and place it in a simulated end-user environment with selected parametric variations. (It is usually impossible to vary every parameter within the product specification during system tests). System tests include:

SCSI protocol tests that verify your design's compliance with the SCSI message system—the functions within the SCSI protocol that control data flow across the bus. Protocol compliance is a major source of difficulties for many SCSI designs. A disk array's "front end" (the host-side interface) and "back end" (the drive-side interfaces) require exhaustive protocol testing. Use a selected subset of SCSI commands to test the SCSI-identify, resource-negotiation, command-queuing, and error-recovery (including contingent-allegiance) messages.

In well-behaved systems, protocol errors do not occur very often. However, testing for SCSI protocol errors is important because if they do occur in the field and the system fails, it may be impossible to determine the cause of the failure. It may therefore be impossible for you to duplicate and fix such field failures.

SCSI exercisers are useful for command tests because they have the ability to perform illegal actions on the bus and insert bus-parity errors. Disk emulators are useful for the back-end testing because real SCSI disk drives do not produce errors under normal conditions.

Command-function tests ensure that all SCSI commands supported by the disk array operate correctly. Your command tests should include functional testing, exception testing, and command-sequence testing. Functional tests exercise all system features and options to ensure compliance with the SCSI-2 spec and the product's specifications. Vendor-unique commands should also be tested at this level. Use exception tests with illegal commands and parameters to ensure that your system operates with unfriendly hosts.

Command-sequence tests ensure that sequences of commands operate properly. Other command tests operate on individual commands and all of their parameter variants. Command-sequence tests ensure that

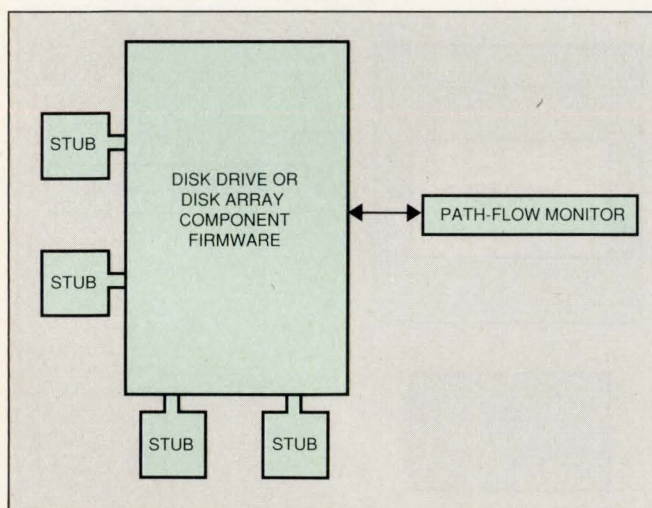


Fig 3—A path-flow monitor ensures that you have exercised all paths in your code.

data-spanning commands operate properly. Contingent-allegiance support, reserve-and-release support, and the effects of mode-select parameter modification should also be tested at this point.

Cache-function tests exercise the storage subsystem's cache. These tests should change buffer-full and buffer-empty ratios and check to see that the design still meets performance goals. They should measure reconnect timing with a single initiator while varying block size and transfer size with respect to stripe size. The tests also check timing using multiple initiators with each initiator using a different buffer-full ratio. The tests should vary cache-segment, block, and transfer sizes with one or more initiators.

Cache-function tests should also include delayed-write tests that read a recently written block before the subsystem transfers the data from the cache to the media. The block that's read should match the just-written block, not the data block residing on the physical media. This test ensures that you always get the latest version of the data from the disk drive or array.

Queued-command sequence tests ensure that queued commands are executed in the proper order for sequences of writes and reads and mixtures of tagged-queue, head-of-queue, and simple-queue SCSI-2 command options. For example, these tests should verify that writes preceding reads in a queue do not corrupt data. This problem could occur if the disk array were to erroneously select and execute the read command before the write command.

The test equipment used for command tests must be able to emit all SCSI-2 and your vendor-unique

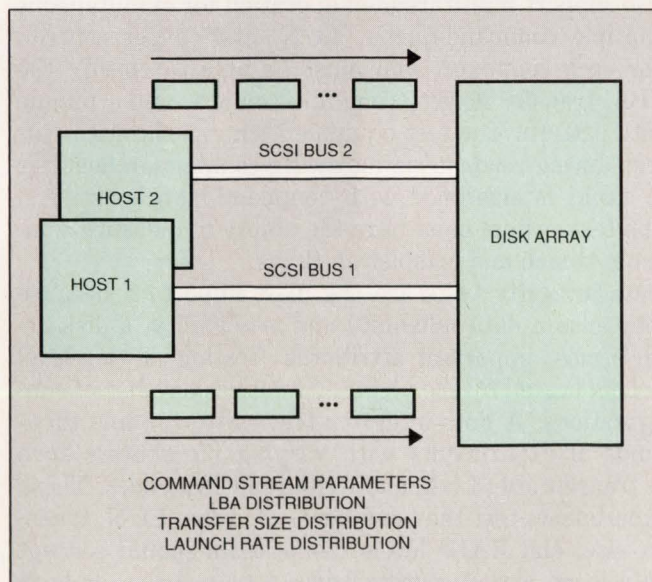


Fig 4—In a command-launch stress test, one or more computers emit commands using varied logical block addresses, transfer sizes, and intercommand timing.

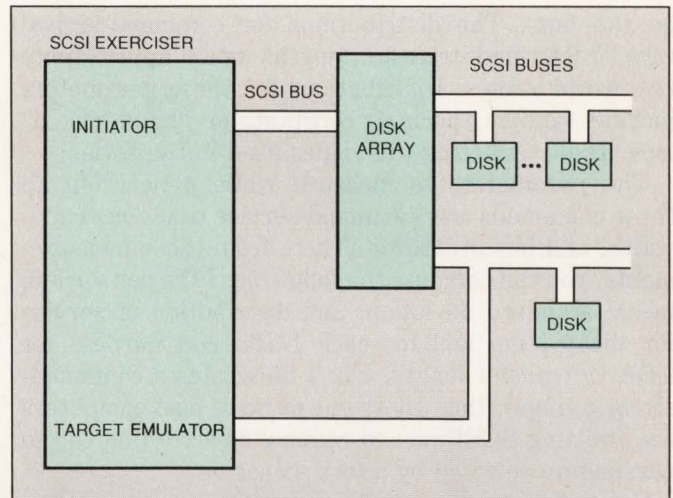


Fig 5—One SCSI test adapter can exercise both the "front end" (host side) and "back end" (drive side) SCSI buses.

commands. It must be able to generate and respond to all of the SCSI messages including command-queuing messages and must ensure that the device being tested obeys the SCSI contingent allegiance and extended contingent allegiance rules resulting from drive errors.

Because disk drives or arrays with caching and buffering are very complex, you must test cache and buffer boundary conditions with varying block sizes to make sure that buffer pointers never become garbled. To accomplish this type of testing, each write command must have a unique data pattern that can be verified by subsequent reads. Test systems usually verify data blocks with low-overhead hardware to maintain heavy data-transfer loading on the disk or array under test.

Performance and stress tests exercise the disk drive or array to measure a number of valuable performance parameters such as various kinds of overhead, bandwidth, throughput, and response time under varied load conditions. In addition, these tests introduce error conditions on both the host side and drive side while stressing the I/O rate to measure the error-recovery and data-reconstruction effectiveness under load. Performance and stress tests also reveal the error recovery's effect on performance. Other parameters measured by these tests include throughput (measured in I/Os per second) and fairness with respect to queued I/O under varying load and command mix.

You should define several "test scenarios" or specific experiments for your performance and stress tests by varying the following parameters: command-launch rate and distribution, LBA distribution, transfer-length distribution, number of I/Os, percent of reads vs writes, the number of LUNs, and the number of targets (which determines the effects of other traffic

SCSI disk testing

on the bus). The distributions for command-arrival rate, LBA, and transfer lengths must approximate real-world values. Distributions for these parameters include random, normal, constant, or "hand-picked" (specifically selecting the values used in the series).

The parameters to measure while generating all these commands are: command-service time, bus bandwidth, and bus utilization. Then, from these measurements, you can compute the following: I/O's per second; mean, standard deviation, and distribution of service for the system and for each LUN; and fairness for LBA vs transfer length. Fig 4 illustrates a command-stress configuration where one or more host computers are emitting SCSI-queued commands according to the parameters selected by a test scenario.

Some disk-drive or -array capacities are larger than the volume sizes supported by the host's operating system. The SCSI spec defines a logical unit number (LUN) to expand the address space of the drive in these cases. A host can access LUNs independently in a multithreaded fashion; therefore, LUNs must be tested in the same manner. Further, disk drives and arrays must co-exist on the SCSI bus with other disk or tape devices, and you may need to test such configurations. SCSI target devices can misbehave in a multi-target system, particularly when bus errors are introduced.

For disk-array drive-side testing, you need a disk emulator to inject drive-side anomalies during heavy loads. You also need a method to coordinate host- and drive-side processing to inject errors at desired points. Test equipment for performance and stress tests must let programmable command-arrival rates maintain full

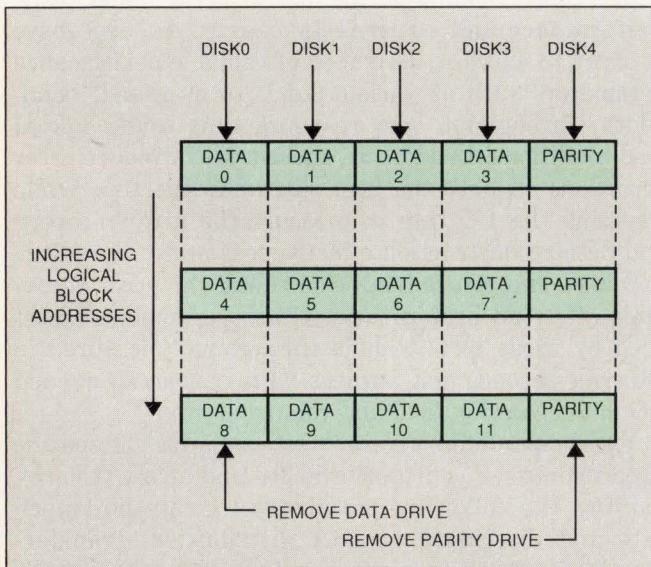


Fig 6—Data-integrity tests that turn drives on and off probe an array's ability to function if a data or parity drive fails.

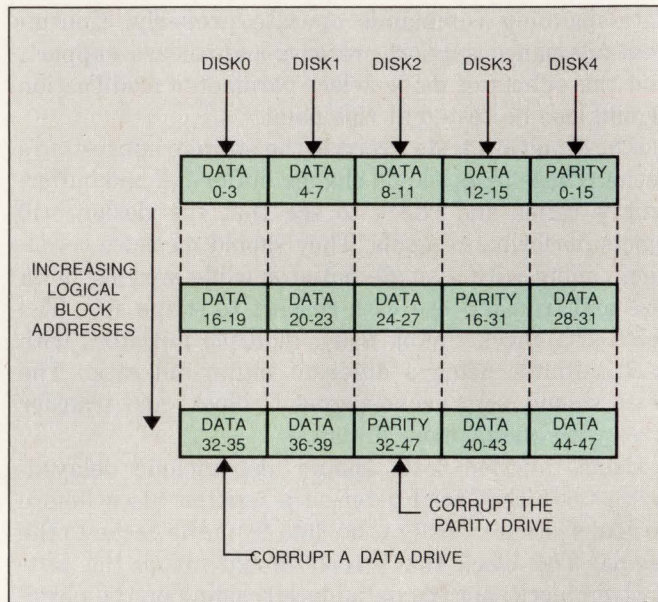


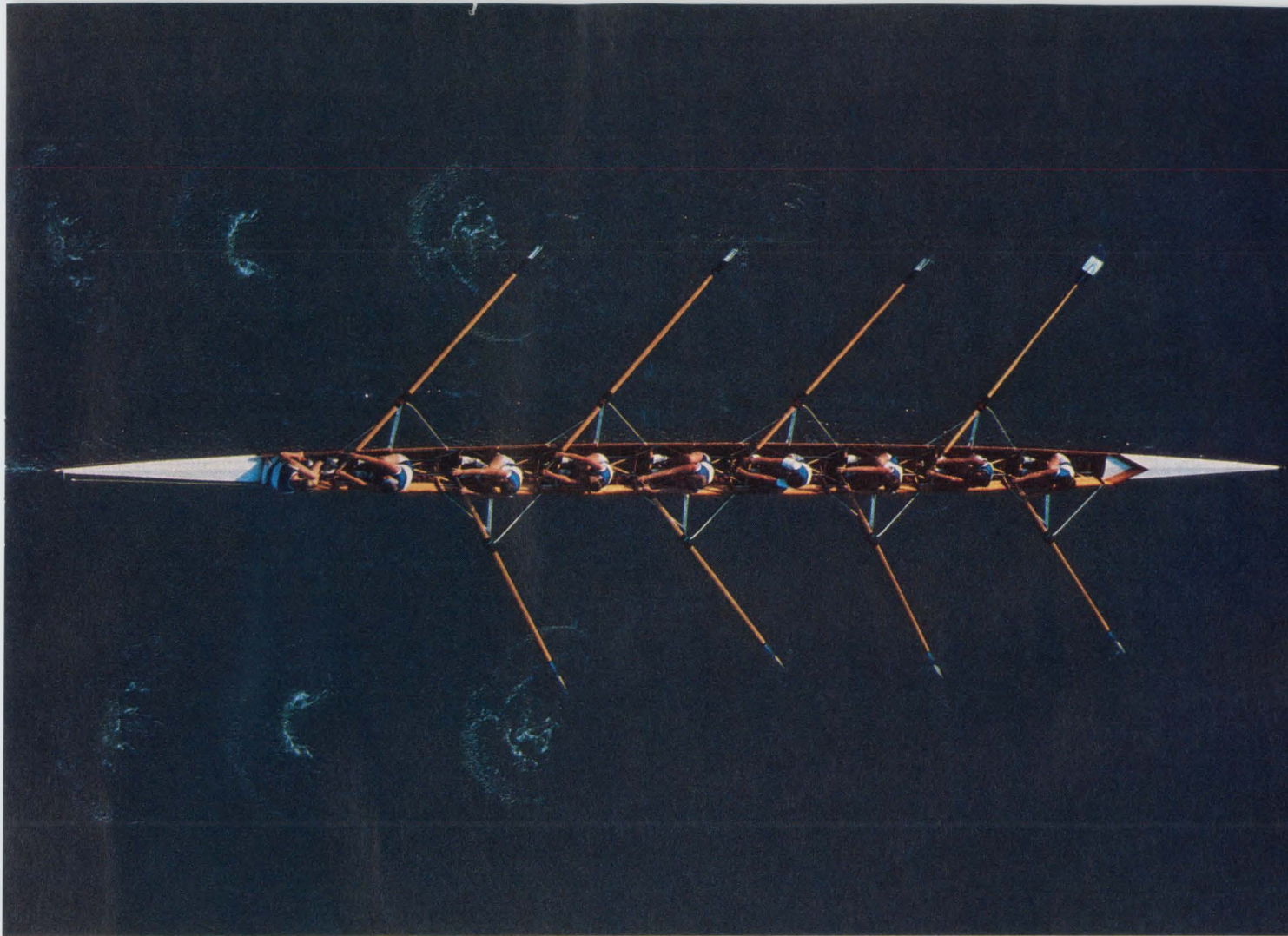
Fig 7—Data integrity tests that corrupt specific logical block addresses can identify redundancy problems with RAID Level 5 disk arrays.

queues. The equipment must also support a range of SCSI-2 bus-width and cabling options. The test system must be configurable to support various combinations of initiator and target configurations, and the system must be flexible and easy to use so that test engineers can generate test procedures efficiently.

The test system must support many device configurations and be able to control command launch rates according to your test scenario. Test equipment must also support multithreaded operation for simultaneous multiple command-queue, LUN, and target control. For each command, you must be able to specify the LBA, transfer length, time until launch, and a unique data pattern. The test equipment checks the data pattern during reads using hardware comparison facilities to avoid interference with command-launch activity. The test system must have the ability to measure command launch and completion times.

Data-integrity tests are the most important because they ensure data reliability and availability, a disk array's most important attributes. Testing at this level is complicated by the virtually limitless number of configurations. A data-integrity test suite contains thousands of experiments with varying parameters such as transfer size, LBA, and write/read sequences. These experiments test the boundaries of cache, LUN, transfer size, and RAID levels. Some tests should corrupt data in an array's parity drive, a data drive, or both drive types at the same time to test the array's response to such errors.

The data-integrity test suite should also include sev-



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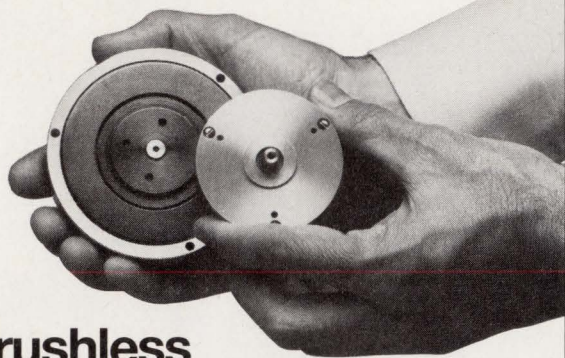
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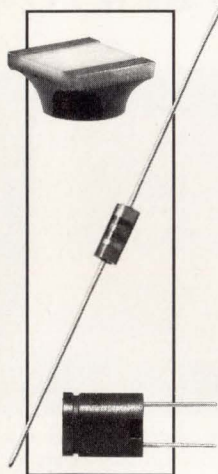
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eral tests in which two test adapters—a host simulator and a disk emulator—coordinate the timing of simulated disk errors with stressful command loading from the host. **Fig 5** illustrates this test configuration. The same configuration is useful for performance and stress testing.

Fig 6 shows a RAID Level 3 disk-array configuration with a dedicated parity drive. In this example, a block read of LBAs 0 through 3 will exhibit higher performance because independent SCSI buses access all four disk drives in parallel.

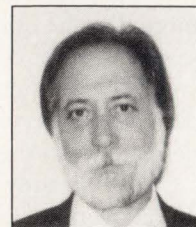
The stripe depth (sometimes called the "chunk size") is the number of contiguous blocks accessible on each logical disk. **Fig 6** shows a stripe depth of 1. Disk arrays can vary the stripe depth as a function of user-request size to meet specific performance goals; usually, the stripe depth and the request size are equal. **Fig 7** shows a RAID Level 5 disk array with a stripe depth of 4. Each drive in this example stores four contiguous blocks.

Data-integrity tests should use data transfers that span data disks using multiple stripe depths ranging from 1-block transfers to transfers of many thousands of blocks. Subsequent tests should cause data corruption to check the array's ability to recover data. Other tests should disable an entire drive to check for proper drive reconstruction while new transactions are being processed.

Configuration-limit tests apply data-integrity tests to different disk-array configurations. The tests execute on a selected set of disk-array configurations by varying the number of back-end disk drives, back-end SCSI ports, and front-end host initiators. As each configuration takes many hours of test time to execute, selecting the configuration set to run these tests against becomes a significant part of test design. **EDN**

Author's biography

Herbert W Silverman founded Peer Protocols Inc (Newport Beach, CA) in 1986 to create SCSI testing tools. He holds a BSEE and MSEE from Northeastern University (Boston, MA).

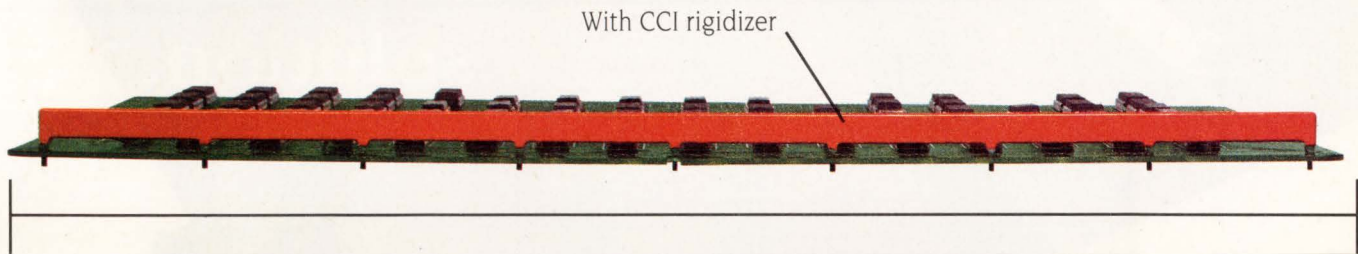


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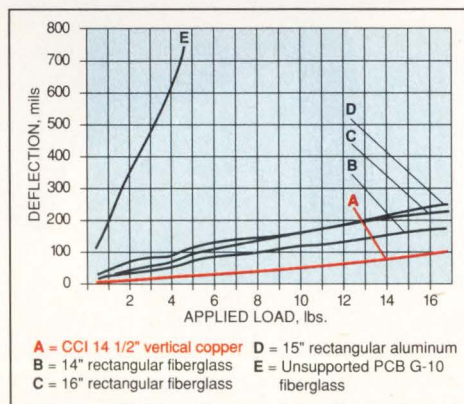


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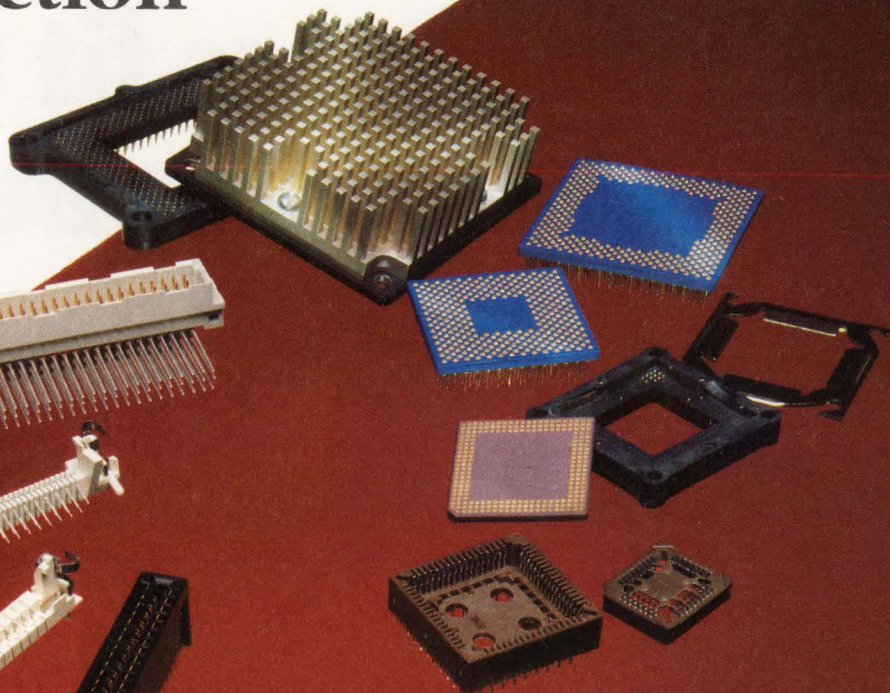
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Architectural choices provide the key to reliable fixed-point filters

Fred J Taylor, University of Florida; Glenn S Zelniker,
Monica A B Murphy, Henry A Gancedo, The Athena Group Inc

Fixed-point DSP μ Ps offer significant cost-performance advantages over their floating-point counterparts when creating digital filters. Unfortunately, fixed-point filters can yield poor performance if improperly implemented. Selecting the right architecture is the key to successful designs.

DSP μ Ps can yield reliable, high-precision, and cost-effective digital replacements for analog filters. They can also implement programmable and adaptive filters that are difficult to develop using analog components. Because they have a finite word length, however, digital filters suffer from errors introduced by rounding, truncating, or arithmetic overflow that occur at the register level. You can reduce these problems by using floating-point DSP μ Ps, but fixed-point filters have the advantages of increased filter bandwidth and lowered system cost, power consumption, and board area. The key to success is choosing the proper fixed-point architecture.

Digital filters are generally classified as being either finite impulse-response (FIR) or infinite impulse-response (IIR) filters. FIR filters, which are purely feed-forward networks, are free from instability problems, have a simple structure, and can be easily protected from severe finite-word-length effects. How-

ever, to meet even the most basic specifications, FIR filters need to be of a high order. High-order filters can become arithmetic-intensive, with an attendant reduction in bandwidth. In comparison, IIR filters can generally meet a set of specifications with a much lower-order design, making them the most preferred choice. An IIR filter, however, is both a feed-forward and a feedback network. The feedback structure gives rise to stability problems and recirculates finite-word-length errors.

Designing the IIR filter

The IIR filter design process consists of three general steps, with a fourth required for fixed-point implementation. You should verify and test your design after each step. The steps are:

1. Specify the design requirements in terms of attenuation (gains) and frequency ranges.
2. Generate the filter transfer function or model,

$$H(z) = \frac{\sum_{i=0}^{n-1} a_i z^{-i}}{\sum_{i=0}^{n-1} b_i z^{-i}}$$

3. Select and evaluate the filter architecture, such as Cascade, Direct II, Lattice-ladder, etc.
4. Convert the design into a scaled fixed-point filter that maximizes precision without introducing arithmetic overflow errors.

Once you have established the desired response of the target filter (Step 1), you have several ways of

FIXED-POINT DIGITAL FILTERS

generating the filter model. You can choose either a classic approach, such as Butterworth, Chebyshev, or Elliptic filters, or a user-defined approach. You can also shift between models, as diagrammed in Fig 1.

The classic IIR filter design models are legacies of the earlier radio-engineering era. They appear in most filter-design handbooks (Refs 1 and 2) and a number of DSP software packages can implement them (Ref 3). If you choose to use a classical filter model, you can make your selection based on which filter attribute is most important in your application. Table 1 gives some guidelines for choosing classical filters. Elliptic is the most popular IIR form because it has the lowest order for a given performance level. A lower filter order translates directly into increased speed (that is, fewer multiply-accumulates) for a processor-based design. If speed is not the principle design limitation, then the other types of filters can offer advantages.

If you choose to create a user-defined filter, there are two commonly accepted means of converting an analog filter, specified in the s-plane as a transfer function $H(s)$, into a discrete or digital filter, given in the z-plane as $H(z)$. You use either the standard z-transform or the bilinear z-transform. Both processes are also well-documented in handbooks and are available in some DSP software packages.

Architecture, the forgotten step

After you have completed Step 2, you'll have only a transfer function, $H(z)$. This is sufficient information to implement a digital filter in software using the difference equation

$$y(n) = \sum_{i=0}^{n-1} a_i u(n-i) + \sum_{j=1}^{n-1} b_j y(n-j),$$

relating output samples $y(n)$ to input samples $u(n)$. However, this would produce an awkward implementation in DSP hardware because it requires approximately $2n$ shift registers to store the necessary series of values $\{u(n)\}$ and $\{y(n)\}$. The simplest, or canonic, architectures (the arrangement of multipliers, adders, and shift registers that implement the transfer function) require only n shift registers. Table 2 summarizes

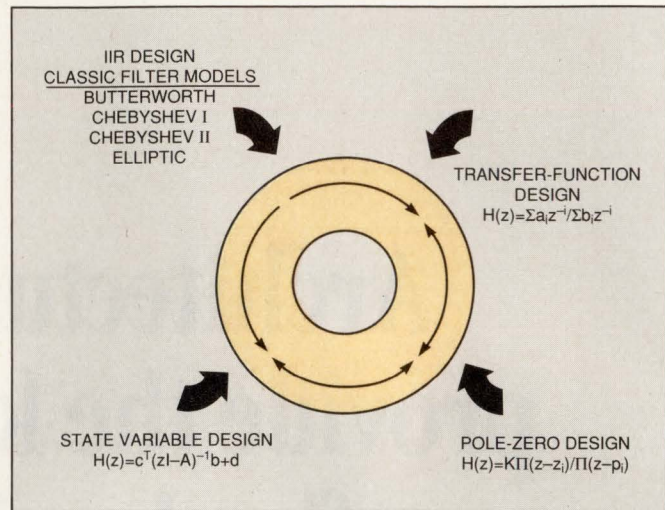


Fig 1—You can implement an IIR filter design using a classical filter model or one of several user-defined models, as well as shift between model descriptions.

some of the commonly used canonic architectures and their relative merits. These are general guidelines, however, and must be verified on a case-by-case basis. The guidelines assume a classic tradeoff between round-off-error sensitivity (precision) and filter complexity (throughput).

Some architectures are less susceptible to fixed-point errors than others. For simple fixed-point implementations, the Cascade architecture is the most commonly used. However, Cascade filters have a higher finite-wordlength error sensitivity than some of the others. Yet, even though the rules for converting a transfer function to an architecture are published, most software packages utilize only the simple Cascade architecture at the exclusion of more sophisticated fixed-point architectures, or offer no conversion algorithms at all. The reason for this lack appears to be the greater level of mathematics capability required to be able to design and analyze advanced architectures.

Among the other architectures, Direct-II filters require the fewest number of multiply-accumulates to implement, and therefore have the highest potential bandwidth. If you were working with floating-point processing, where round-off errors are not typically a problem, the high bandwidth of a Direct-II filter would

Table 1—Attributes of classical IIR filters

Attribute	Best IIR	Worst IIR
Filter Order	Elliptic	Butterworth
Flat Passband	Butterworth, Chebyshev II	Elliptic, Chebyshev I
Flat Stopband	Chebyshev I	Chebyshev II

Table 2—Relative merits of canonical filter architectures

Architecture	Advantage	Disadvantage
Cascade	Good fixed-point performance	Few
Direct-II	Fastest (highest bandwidth)	High round-off error sensitivity
Parallel	Fault tolerant	Higher round-off error sensitivity
Normal	Low coefficient error sensitivity	Increased complexity
Lattice-Ladder	Orthogonal outputs	Complex
Wave	Lowest round-off error sensitivity	High complexity

make it the natural choice. However, for a very high-order IIR ($n > 12$), the filter coefficients may need to span a 20- to 30-bit dynamic range. In such cases, even 32-bit floating-point DSP μ Ps have insufficient resolution to guarantee acceptable performance. The situation for fixed-point Direct II is worse—even low-order Direct-II filters can suffer from catastrophic fixed-point errors.

Clearly, to choose the best architecture for your fixed-point design, you must understand and analyze the sources and effects of finite-wordlength errors. Fixed-point arithmetic gives rise to a host of nonlinear effects caused by finite wordlength. The effects stem from two sources, coefficient roundoff and arithmetic errors.

Coefficient-round-off errors come about when you first create the fixed-point implementation of a transfer function by rounding the transfer function's coefficients. The difference equation becomes

$$y(n) = \sum_{i=0}^{n-1} (a_i)_Q u(n-i) + \sum_{j=1}^{n-1} (b_j)_Q y(n-j),$$

where x_Q is the rounded value of x . Coefficient round-off can alter the shape of the filter's time and frequency responses from the ideal. It can also change the filter's pole and zero locations causing, in extreme cases, instability. If the word width is properly utilized, however, modern fixed-point DSP μ Ps generally provide sufficient precision to control coefficient-round-off errors for low-order IIR filters.

You can also reduce coefficient-round-off errors by properly pairing poles and zeros into first- and second-order filter sections. You can factor all transfer functions $H(z)$ having real coefficients $\{a_i\}$ and $\{b_j\}$ into real and complex-conjugate roots. You use the real roots to create first-order filter sections and combine complex-conjugate pole and zero pairs to create second-order filter sections, all having real coefficients. These first- and second-order sections are the fundamental building blocks of a digital filter having cascade sections. As a rule-of-thumb, you reduce the coefficient round-off errors by pairing the poles and zeros that are the closest together based of their Euclidian distance, or proximity, in the z -plane.

The second error source is arithmetic. An n -bit fixed-

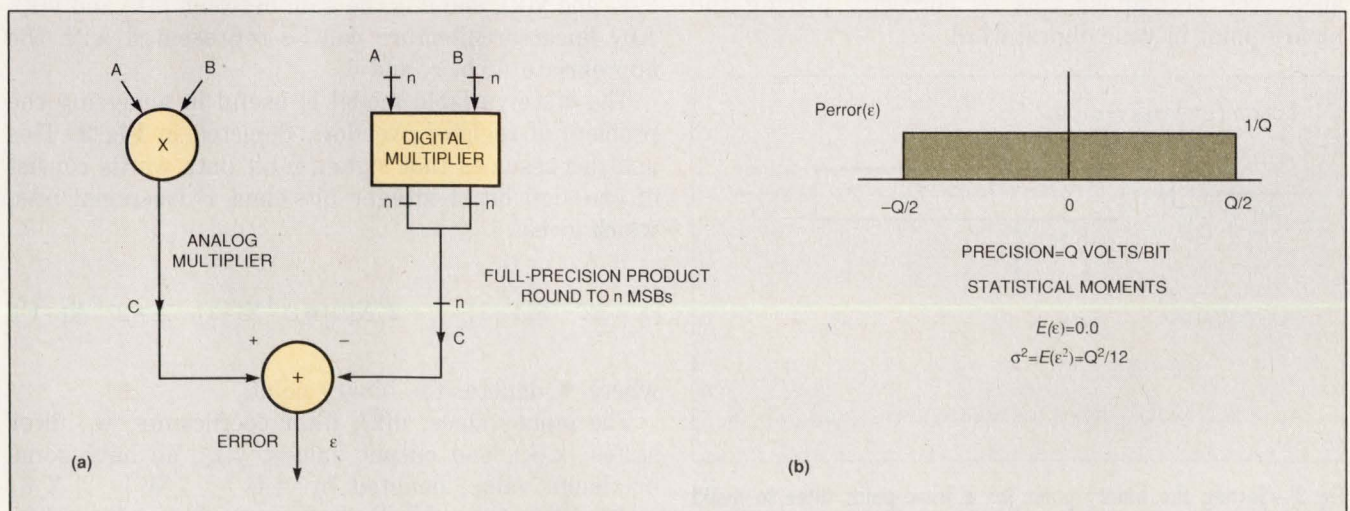


Fig 2—Arithmetic round-off error in digital filters comes about when a full-precision product gets truncated (a) by a multiplier. The resulting error can be statistically analyzed and is typically expressed (b) as a uniform probability distribution.

FIXED-POINT DIGITAL FILTERS

point arithmetic unit will accept two n-bit operands and produce a precision product, which it then rounds to an n-bit result. This produces an error, ϵ , as shown in Fig 2a. Such errors, unfortunately, recirculate within the IIR filter's feedback structure and have a cumulative debilitating effect on the system's output data. Therefore, arithmetic errors are not simply additive, but are defined by a transfer function from the error source (that is, multiplier) to the output, which you must derive for each noise source.

You can analyze the effects of this error type statistically, as shown in Fig 2b. The value Q , called the quantization step size, has units of volts/bit. If a signed analog signal having a range of $\pm V$ volts is subdivided into 2^n distinct (digital) values, then $Q = V/2^{n-1}$ volts/bit. A frequently used model for the quantization-error probability density function is a uniform distribution over the range $(-[Q/2], [Q/2])$. The mean of this distribution is zero and its variance is $Q^2/12$. Each multiplier contributes round-off error power to the output, an amount $\sigma_i^2 = G_i(Q^2/12)$. The value G_i is the noise power gain, or simply noise gain, from the i -th multiplier to the output. The noise power reaching the output is the sum of all contributions.

Arithmetic errors are also characterized by nonlinear effects. The most severe form is register overflow, or saturation. If it should occur, large sample-by-sample errors can result. Recognizing this as a potential problem, most DSP μ Ps incorporate saturating arithmetic, which clamps the multiply-accumulate result to its minimal or maximal value upon detecting an overflow. While not eliminating the problems caused by register overflow, this feature reduces the effects. Even so, ensuring that such overflow will not occur in your fixed-point IIR filter is critical to the filter's performance. You accomplish this by correctly placing the binary point in your digital word.

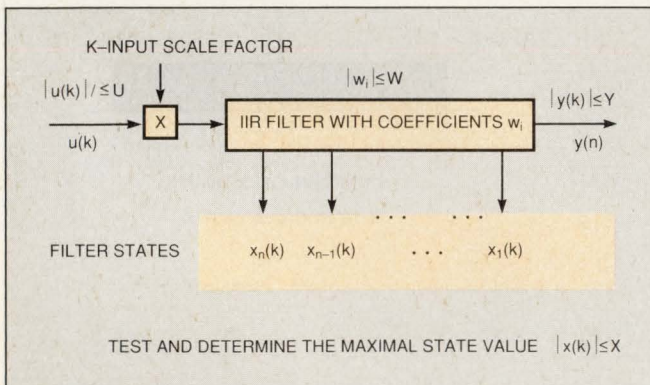


Fig 3—Setting the binary point for a fixed-point filter to avoid overflow errors requires that you find out how large the numbers will get. The inputs, outputs, coefficients, and internal register values all have upper limits that you must find.

Calculating the noise gain (G_i) for arithmetic errors and determining the correct decimal placement to avoid overflow can be formidable problems when dealing with an arbitrary architecture. The most efficient bridge between architecture and noise-gain analysis stems from state-variable techniques like those used in circuit analysis. The techniques simplify the analysis of both noise gain and register overflow. Unlike the other possible transfer-function descriptions, the state-variable paradigm describes the behavior of an IIR filter at the shift-register level as well as relating the output to the input.

State-variables simplify analysis

In the state-variable schema, the transfer function for an n -th-order IIR filter is given by

$$H(z) = \mathbf{c}^T (z\tilde{\mathbf{I}} - \tilde{\mathbf{A}})^{-1} \mathbf{b} + d,$$

where d is a scalar, \mathbf{b} and \mathbf{c} are n -dimensional vectors, $\tilde{\mathbf{A}}$ is an $n \times n$ matrix, and $\tilde{\mathbf{I}}$ is the identity matrix. From this transfer function comes the state model

$$\mathbf{x}(k+1) = \tilde{\mathbf{A}}\mathbf{x}(k) + \mathbf{b}u(k),$$

which has a filter-output value given by

$$y(k) = \mathbf{c}^T \mathbf{x}(k) + du(k),$$

with $u(k)$ and $y(k)$ being the scalar input and output values for sample k and \mathbf{x} being the vector comprising the contents, or state, of the filter's n shift registers for sample k . The element a_{ij} defines the gain between state $x_j(k)$ and state $x_j(k+1)$, b_j is the path gain between $u(k)$ and $x_j(k+1)$, c_j is the path gain between $x_j(k)$ and $y(k)$, and d is the gain between $u(k)$ and $y(k)$. Any linear architecture can be represented with the appropriate $\tilde{\mathbf{A}}$, \mathbf{b} , \mathbf{c} , and d .

The state-variable model is useful in analyzing the problem of register overflow, depicted in Fig 3. This analysis assumes that signed n -bit data words consist of one sign bit, I integer bits, and F fractional bits, which gives:

$$x = \pm 2^{I-1} X(I-1) + \dots + 2^0 X(0) \blacklozenge 2^{-1} X(-1) + \dots + 2^{-F} X(-F),$$

where \blacklozenge denotes the binary point.

The input values, $u(k)$, filter coefficients, w_i , filter states, $x_n(k)$, and output values, $y(k)$, all have some maximum value, denoted by $|U|$, $|W|$, $|X|$, and $|Y|$. Assuming that the scale factor $K=1$, the problem of implementing an overflow-free filter is one of determining where to set the binary point so that

Table 3—Definition of register norms (bounds)

Norm	Definition	Input assumption	Worse-case input
l_f (frequency domain)	$\ h_k\ _f = \max_{\omega} H_k(e^{j\omega}) $	$u(k) = \cos(\omega_0 k + \phi)$	Sinusoidal
l_1 (time-domain)	$\ h_k\ _1 = \sum_n h_k(n) $	$ u(n) \leq 1$	Bounded by unity
l_2 (time-domain)	$\ h_k\ _2 = \left(\sum_n h_k(n) ^2 \right)^{1/2}$	$\sum_n u(n) ^2 \leq 1$	Finite energy

$2^I > M = \max(|U|, |W|, |X|, |Y|)$. Therefore, the design of a fixed-point digital filter requires that a compromise be made between the dynamic range requirement ($I > \log_2(M)$ in bits) and precision ($F = (N - I - 1)$ in bits). The key to making this compromise wisely is compute a meaningful dynamic-range bound, M .

Norms set computing bounds

From the state-variable model you can easily determine the impulse response from the input to the k -th state, x_k , with the response denoted by the sequence $h_k = \{h_k(n)\}$. You may define three useful bounds, or norms, from this sequence, each bound corresponding to a particular class of input signal. For sinusoidal signals, use the l_f norm. For aperiodic signals, use the l_1 norm, and for finite-energy signals, use the l_2 norm. **Table 3** summarizes these norms.

These norms are useful in determining the bounds for the register states. If the input signal satisfies the l_1 constraint, then the shift-register content at the k -th state is bounded by $\|h_k\|_1$. The same relationship holds for the l_2 and l_f norms. Which norm you choose

depends on the filter's application and the properties of the signal to be filtered.

The relationship between the norms is

$$\|X\|_2 \leq \|X\|_f \leq \|X\|_1.$$

You can compute the l_2 bound directly from the state-variable description, but the bound is optimistic in that it may be too small to hold true for a real-world input signal. The l_1 time-domain bound is best, but is difficult to compute in closed form. However, if you can approximate the impulse response with a sufficiently long finite sum (that is, if the tail of the response is negligible), then you can experimentally determine the l_1 bound. You can use an FFT to approximate the l_f frequency-domain bound, which presumes that the worst-case input signal is sinusoidal. All these calculations presume that each of the filter's shift registers is accessible for analysis; in the case of a state-variable model, they are.

As an illustration of computing the norms, consider the two finite-duration time series $x_1 = \exp(-0.9n)$, and $x_2 = \exp(-0.9n)\cos(2\pi n/8)$, $n \in [1, 15]$. You can compute

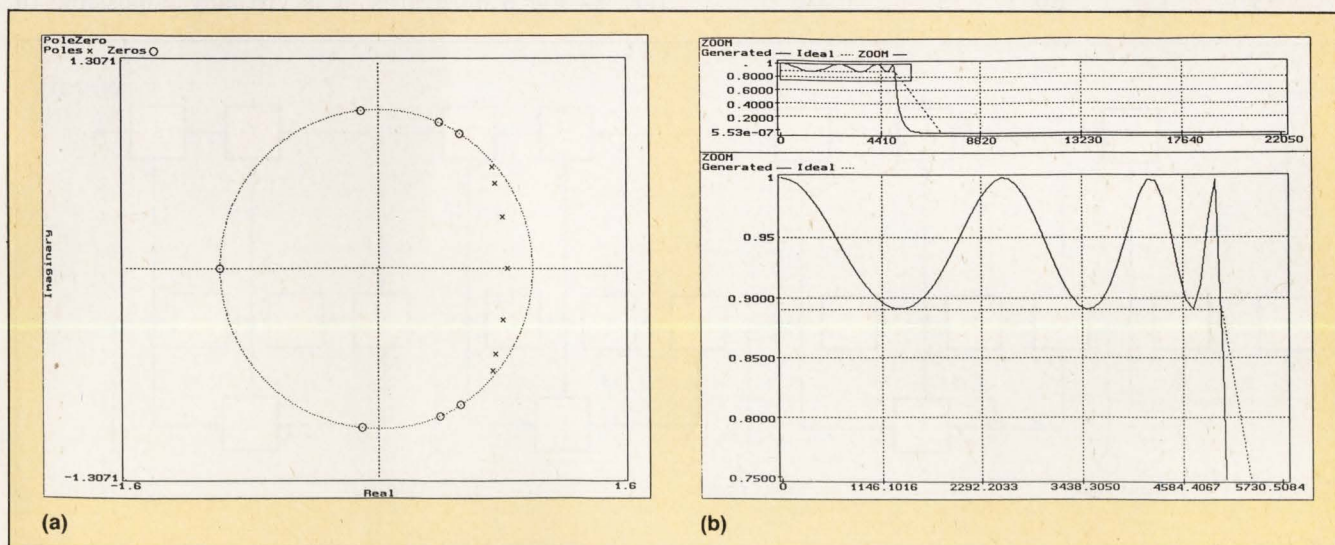


Fig 4—A sample Elliptic filter has the pole-zero map given in (a) with the frequency response shown in (b). Many different architectures will produce these same filter characteristics, but their internal behaviors will vary considerably.

FIXED-POINT DIGITAL FILTERS

the l_1 and l_2 norms directly from their definitions. You compute the l_1 norm by zero-padding the finite-duration time series, taking the FFT, and then finding the maximum magnitude. The results are ordered in agreement with theory,

$$\|x_1\|_2 = 1.09455 \leq \|x_1\|_f = 1.68512 \leq \|x_1\|_1 = 1.68512$$

and

$$\|x_2\|_2 = 1.04198 \leq \|x_2\|_f = 1.28547 \leq \|x_2\|_1 = 1.37251.$$

Using the state-variable description, then, lets you determine the optimal setting for the binary point and predict the noise performance of a given filter architecture. For example, consider a seventh-order Elliptic filter with the following attributes: sampling frequency = 44.1 kHz, passband from dc to 5 kHz with unity gain and flatness ± 1 dB, and stopband from 7 to 22.05 kHz (the Nyquist frequency) with at least 80-dB attenuation.

The filter's transfer function is:

$$H_{(z)} = 0.0007266 \sum_{i=0}^{n-1} a_i z^{-i} / \sum_{i=0}^{n-1} b_i z^{-i},$$

where

i	ai	bi
0	1.0	1.0
1	0.636	5.456
2	1.808	13.545
3	0.349	19.679
4	0.349	17.999
5	1.808	10.346
6	0.636	3.460
7	1.0	0.520

Table 4—Comparison of architectures for sample Elliptic filter

Architecture	W	X_{l_2}	X_{l_1}	X_{l_1}	σ_{Noise} (in bits)
Cascade	≤ 2	≤ 0.232	≤ 0.531	≤ 1.344	-9.8
Direct-II	≤ 21	≤ 0.191	≤ 0.888	≤ 1.430	-10.7
Normal (cascade)	≤ 9	≤ 0.232	≤ 0.532	≤ 1.344	-11.2
Wave	≤ 57	≤ 0.374	≤ 1.875	≤ 2.977	-7.4
Lattice-Ladder	≤ 19	≤ 0.191	≤ 0.888	≤ 1.430	-9.7

Fig 4 shows the filter's zero-pole distribution and its magnitude-frequency response. Using the state-variable description together with DSP design tools, you can calculate the coefficient bound, W, and the three dynamic range bounds for a variety of architectures. You can also calculate the round-off-error noise power, σ , to predict how many bits of fractional precision each architecture will lose. In this example, with results shown in **Table 4**, the Cascade architecture provides the greatest fractional precision after subtracting the effects of noise. The Wave architecture has a smaller noise power, but, for a given word length, has fewer fractional bits to begin with because of its coefficient bound.

Fig 5 shows the Cascade architecture. Notice that the filter comprises three second-order sections and one first-order section. Notice, too, that you need to analyze only states x_0 , x_2 , x_4 , and x_6 because the remaining states contain the same information, although delayed. Fig 6 shows the frequency responses for both a Cascade and a Wave floating-point implementation, measured at the filters' outputs and at each shift register. As Fig 6 illustrates, it is virtually impossible to

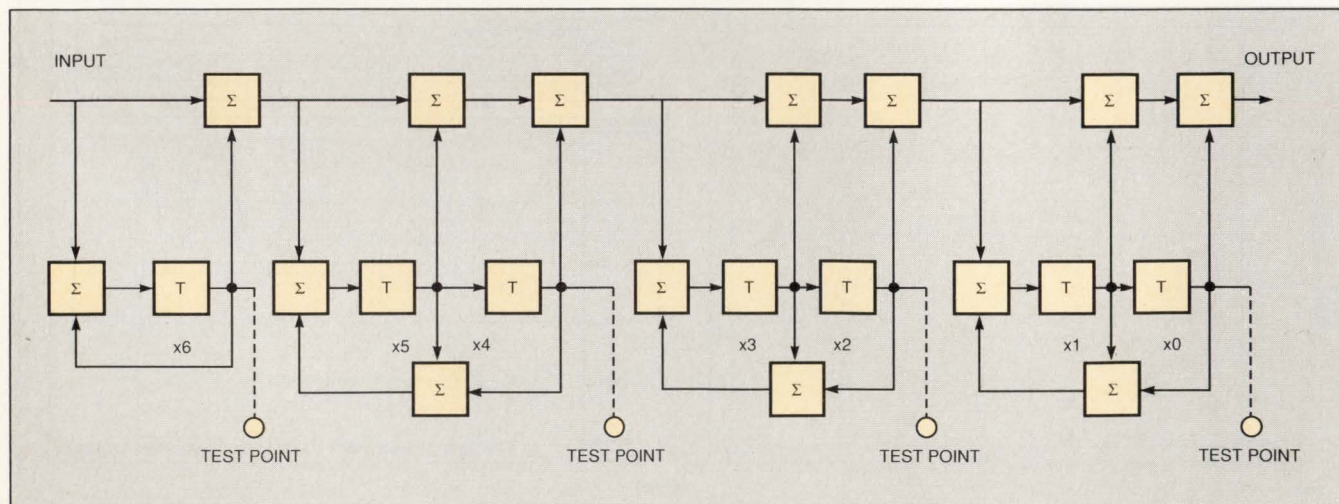


Fig 5—The cascade representation of the sample filter shows the filter's internal states, x_i . If you want to fully test this filter, you'll need the test points indicated so that you can monitor the filter's behavior at the register level.

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predict the internal behavior of filters based only on their input and output measurements. You must be able to explore the internal details to develop a successful design.

The l_1 norm for all the internal states of the Cascade filter is, according to **Table 4**, at most 1.344. This means that if the input signal is bounded by unity for all n , then state x_6 , for example, should never exceed 1.344. **Fig 7b** shows the results of a computation of the l_1 norm for state x_6 assuming a unit impulse. By analogy to a matched filter, it is relatively easy to see that the state will eventually approach the l_1 norm if the input signal is the sign-reversed impulse response from the

input to state x_6 , namely $u(n) = -\text{sign}(h_6(-n)) = \pm 1$. Generally, the worst-case time series will be an aperiodic sequence.

Set word format to avoid overflow

Fig 7a shows the impulse response for state x_6 and **Fig 7b** shows the l_1 norm. As predicted in **Table 4**, the norm is bounded by 1.344. **Table 4** also reports that the largest filter coefficient is <2 . The input and output values are bounded by unity, so the dynamic range bound $m = \max(|U|, |W|, |X|, |Y|) < 2$. This condition requires that the word format used in a DSP processor have at least one integer bit ($I = 1$).

To verify this word-format choice, we calculated the filter's state-6 output using the input sequence shown

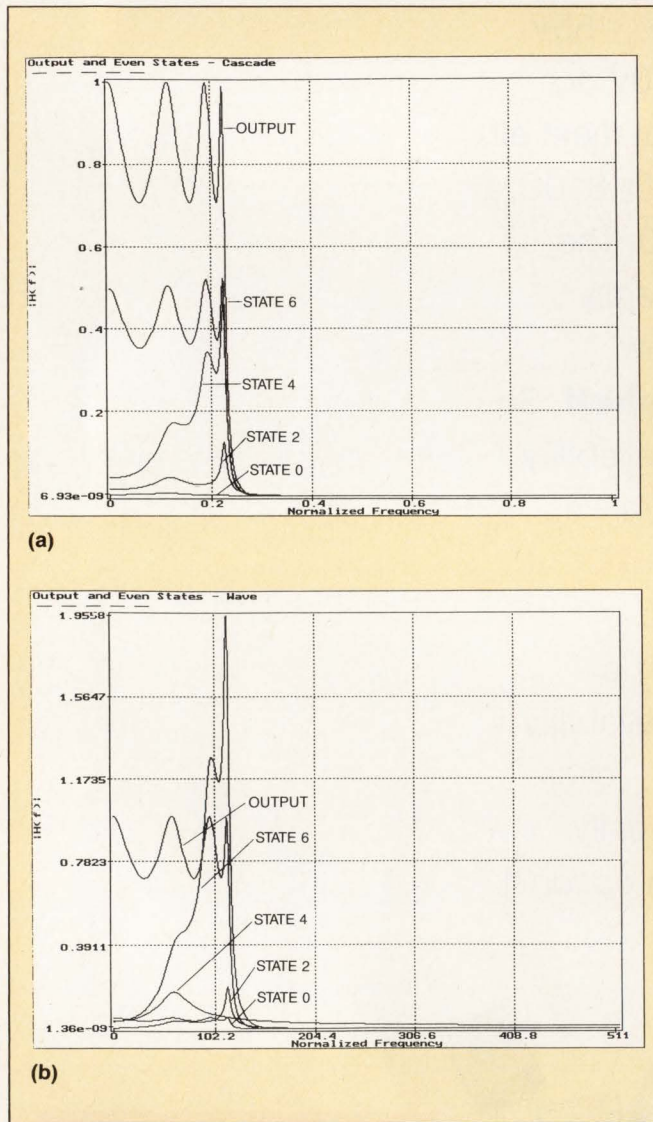


Fig 6—Both a Cascade (a) and a Wave (b) architecture produce the same filter output, but their internal behavior differs widely. Registers in the Wave architecture need extra integer bits in their fixed-point data words to avoid register overflow.

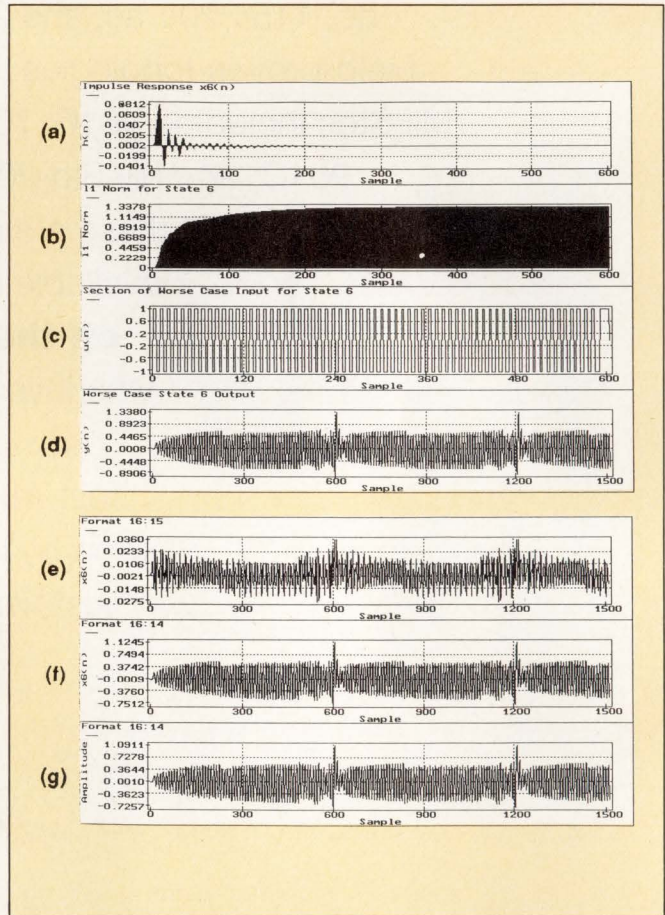


Fig 7—If you drive the sample filter with its worst-case input signal(c), derived from one register's impulse response (a), you can test the predictions made by the various norms. The norm for the filter's state 6 (b) predicts an upper limit adhered to in a floating-point filter design (d). A 16-bit fixed-point filter design having no integer bits shows distortion (e) due to overflow errors. By providing one integer bit, the output (f) more closely matches the floating-point result (d). Adding a second integer bit has little effect (g), except to lose accuracy.



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in Fig 7c. The output for a floating-point implementation appears in Fig 7d as a reference. Figs 7e, 7f, and 7g show the results obtained for a 16-bit fixed-point filter using word formats having 1 sign bit and 15, 14, or 13 fractional bits (abbreviated (16,15), (16,14), and (16,13)). As Fig 7e shows, the (16,15) format results in distortion due to run-time register overflow. The distortion occurs even though the processor used saturation arithmetic to suppress most of the undesirable effects. Fig 7f, showing the (16,14) response, shows good agreement with the floating-point response; the filter was free of run-time overflows, as expected. Note, however, that the maximal output value decreased from 1.33 to 1.12 due to finite word-length effects. The output value could as easily have increased by as much. Fig 7g shows that the (16,13) response is also overflow-free but is, in general, less precise than the (16,14) filter.

The state-variable approach, then, is a powerful tool for designing successful IIR filters using fixed-point DSP processors. By examining the internal behavior of a candidate filter architecture and selecting the appropriate word format, you can choose the architecture that best meets your system's speed and precision tradeoffs.

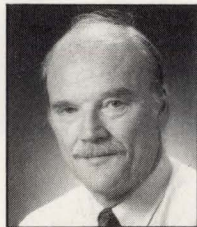
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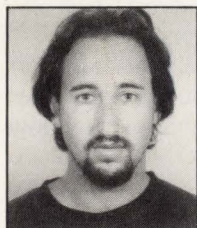
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Authors' biographies

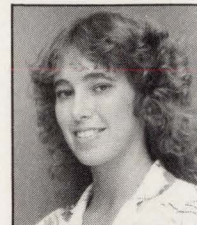
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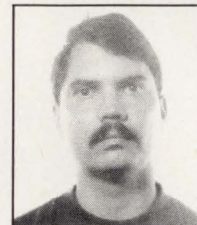
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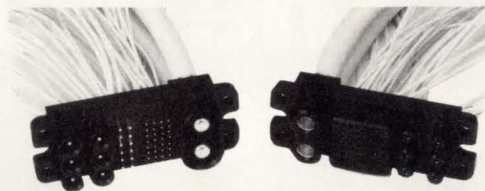
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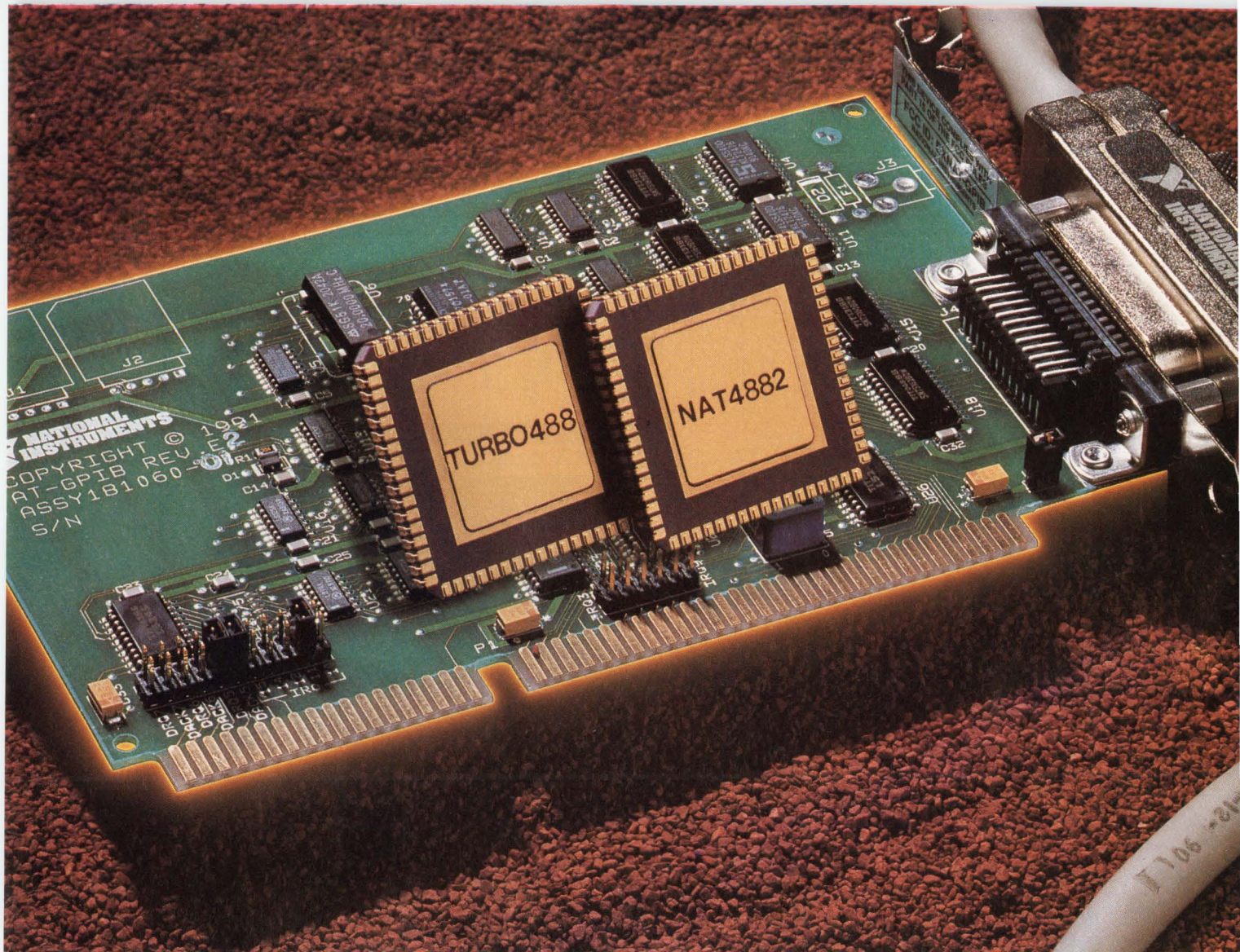


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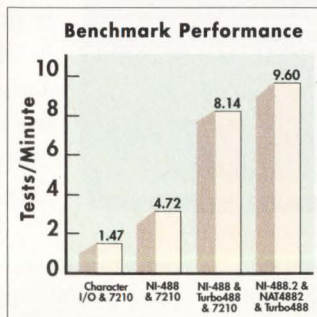
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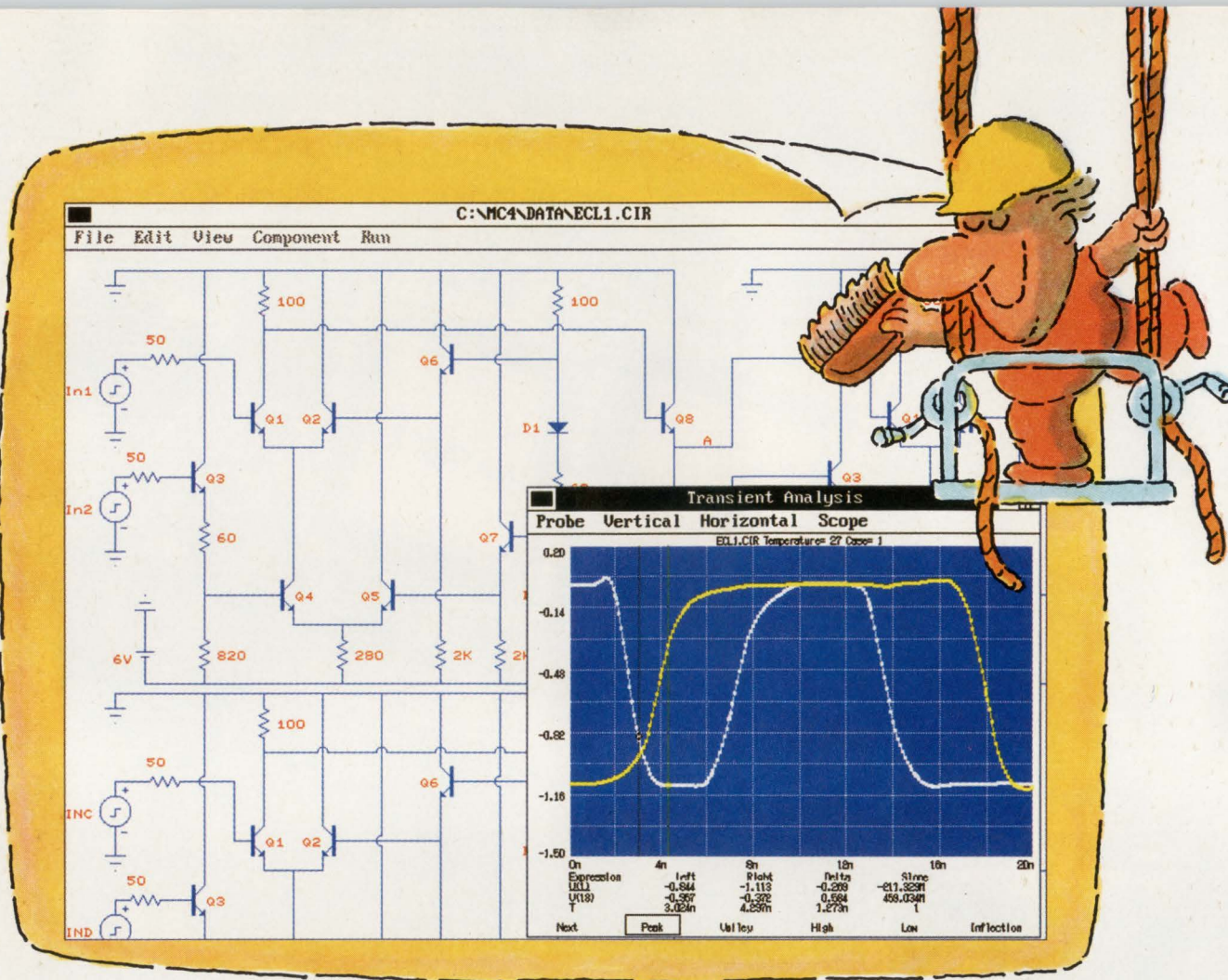
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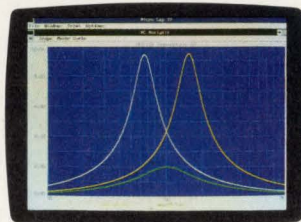


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You can obtain boundary scan's benefits despite use of some nonscan ICs

Jon Turino, Logical Solutions Technology Inc

Although boundary scan can simplify testing of digital subassemblies and pc boards, some people think that serious use of the technique must wait until scannable versions of all ICs become available. But you need not wait; you can realize many boundary-scan benefits in designs that mix nonscannable and scannable devices.

The approval of IEEE standard 1149.1 for a test-access port (TAP) and a boundary-scan architecture will eventually let semiconductor manufacturers supply standard ICs that provide "testability on a chip." Although some chips that conform to IEEE-1149.1 are already on the market, several years will pass before boundary-scan structures appear in all ICs that can benefit from them.

Using boundary scan to design for testability will become much more common as designers increase their systems' performance by using packaging techniques such as fine-pitch technology (FPT), tape-automated bonding (TAB), and multichip modules (MCMs). Although these techniques improve performance, they reduce the subassemblies' test-probe accessibility. The objective of boundary scan is to allow testing for the usual range of manufacturing-induced defects despite limited probe access.

With boundary scan, electrical access to subassembly nodes replaces physical access. Fig 1 shows a block diagram of a boundary-scan chip. Only four pin connections provide electrical access for controlling and observing all of the chip's nodes (and any built-in self-test

features). The four connections are for the test-data-input (TDI), test-mode-select (TMS), test-data-out (TDO), and test-clock (TCK) lines. These lines connect to the TAP controller, an on-chip finite state machine required by the standard.

Test interface comprises four connections

If all of the ICs on a board or subassembly support boundary scan, you can test the entire assembly through the same four external connections. To create the required configuration,

- connect the first chip's TDI to the external interface
- daisy-chain each chip's TDO to the next chip's TDI
- connect the last chip's TDO to the external interface
- connect all of the TMSs together and all of the TCKs together, then connect the TMS and TCK buses to the external interface.

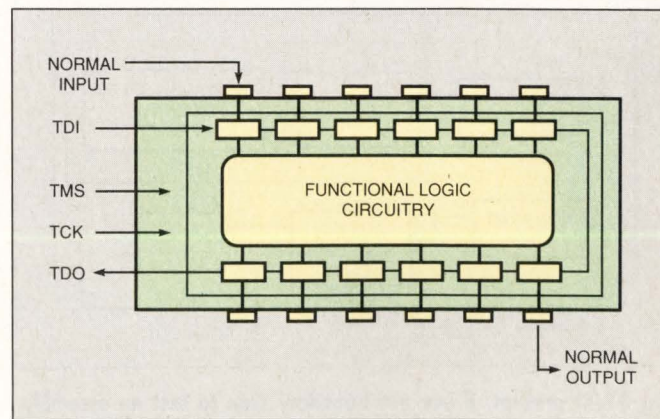


Fig 1—An IC that incorporates IEEE-1149.1 boundary-scan capabilities has four extra pins that control access to the testability features.

BOUNDARY-SCAN TESTING

The TMS and TCK lines clock data into each device's TAP. The TMS line carries chip-state data that tell the TAP controller to tell its device which mode to assume. The TDI line, aided by TCK, transmits the actual instructions and data.

The information that the TDI line sends to each chip can go to the boundary-scan registers, the bypass registers, or any other registers in the device that the TAP can access. The noninverting TDO line allows reading the contents of the instruction, boundary-scan, bypass, and identification registers (if any), as well as certain internal registers. Refs 1 and 2 contain more complete information on how boundary-scan-equipped devices operate.

Until all, or at least most, devices include boundary scan, the situation illustrated in Fig 2 will arise. In this example, the mixture of scannable and nescannable parts results in incomplete fault coverage and can cause device-to-device protocol differences that complicate communication.

Vendors of traditional in-circuit and combinational board testers, as well as boundary-scan proponents, are therefore recommending interim solutions that mix boundary scan with traditional mechanical probing. The idea is that over time, because of the increased use of boundary scan, the number of nodes requiring mechanical probing will decrease faster than it must increase as a result of greater circuit complexity. Therefore, critical nodes that are inaccessible via the boundary-scan path (or other electrical-testability path) will continue to be accessible via mechanical probing.

In some cases, boundary-scan devices can enable the testing of external logic not directly in the scan path. Fig 3 illustrates this capability. To use this approach,

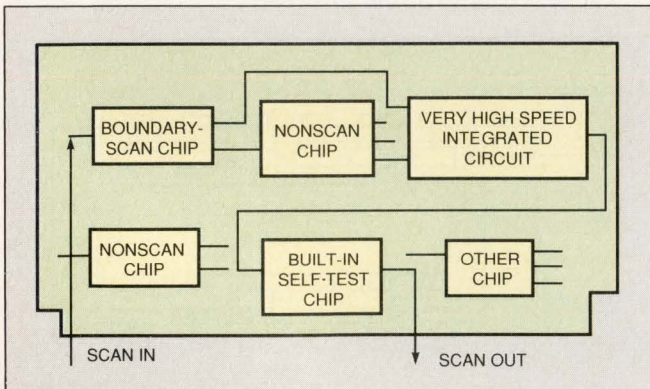


Fig 2—At present, if you use boundary scan to test an assembly, you will almost certainly have to mix scannable and nescannable parts. If you don't combine them carefully, the result can be incomplete fault coverage and communication complicated by device-to-device protocol differences.

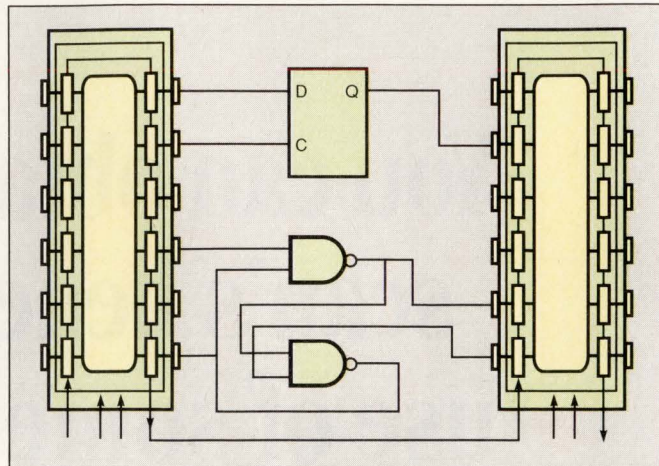


Fig 3—In some cases, boundary-scan devices can enable the testing of external logic not directly in the scan path.

you must convert the external-logic test patterns from parallel to serial, apply them through the scan path, capture the resulting external-logic states, scan them out, convert them back to parallel form, and verify them. Although this approach can be practical for small clusters of fairly simple nescan circuits, it is not very practical when the external circuits include processors, 10,000-gate ASICs, or other very complex logic.

The objectives of boundary scan, however, focus more on detecting what are called "structural defects" in an assembly than on retesting a chip's logic functions after the chip is attached to a board. Thus, there are ways to use boundary-scannable devices to apply and observe fairly simple patterns at the nodes of nescannable devices. With this approach, you can detect "stuck-at-0" or "stuck-at-1" faults caused by open circuits and solder shorts, as well as faults caused by wrong, incorrectly installed, or dead components.

When you add circuits or connections to a device or board to improve its testability, you can impair its performance, its reliability, or both. Boundary scan uses extra silicon for the TAP controller and the boundary-scan cells. Depending on the complexity of the normal functional (or "core") logic, this overhead can range from 30% (for simple devices) to as little as 3 to 5% (for complex devices). The extra silicon is fairly cheap, however, and should not affect reliability significantly.

The biggest complaint regarding boundary scan is the addition of two extra gate delays—one at each chip input and output. However, even if these gate delays degrade the product performance to an unacceptable degree, you can still add boundary-scan-equipped devices as shown in Fig 4. If you can control the 3-state or output-enable lines of the processor, ROM, and

RAM, this approach lets you use the boundary scan devices (labeled 8245) to see if the chips are "alive" and to check the integrity of the bus lines that connect to all of the ICs.

Bypass register speeds testing

The need to achieve acceptable testing speeds helps to explain why IEEE-1149.1 includes a bypass register. Using the register reduces a device's effective word length to one bit or two (depending on the implementation). You can set most of the devices in a boundary-scan path into the bypass mode and supply full-length clocking or data sequences only to chips that perform operations in a particular test.

Another way of shortening individual scan sequences is to multiplex the scan chains (Fig 5). You can think of scan-chain multiplexing as partitioning of the scan chain to permit scanning individual sections of the circuit under test. Of course, the total number of test vectors will still equal the total number of scan cells times the number of test vectors per scan chain (plus a few additional vectors to select a particular scan chain). Where performance restrictions do not preclude it, the ideal approach is to replace single-function parts with parts that include boundary-scan features. These parts let you partition, control, and observe your circuit, hence they let the circuit meet all of the criteria for testability. Fig 6 demonstrates this approach.

Performing structural and performance tests of subassemblies and systems built from mixing scannable and non-scannable ICs that are likely to exist for at least the next few years will require dedicated testability circuits that can interface to scannable and non-scannable chips. One approach is to replace single-function logic circuits with circuits that have both functional

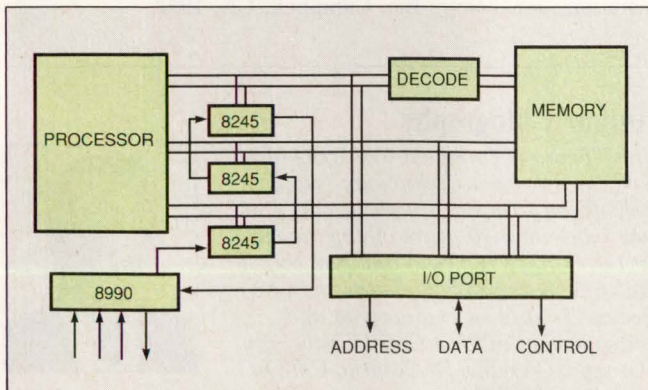


Fig 4—The biggest complaint regarding boundary scan is the addition of two extra gate delays—one at each chip input and output. However, even if these gate delays degrade the product performance to an unacceptable degree, you can still add boundary-scan-equipped devices.

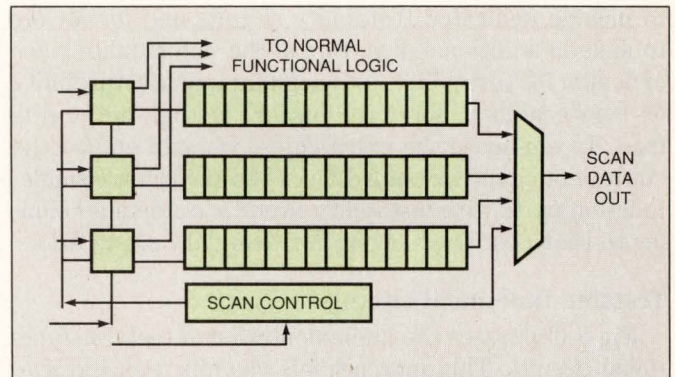


Fig 5—You can think of scan-chain multiplexing as partitioning of the scan chain to permit scanning individual sections of the circuit under test.

and protocol-independent test interfaces. Fig 7 illustrates the addition of dedicated control and observation circuits to a design. These circuits provide coupling from the I/O lines of a subassembly's testability bus to virtually any device on the board or module. The coupling is transparent to CAE tools, automatic test equipment, and built-in test resources.

The approach illustrated in Fig 7 has several advantages. First, you can partition the scan chains to improve fault-isolation resolution. Next, by using the testability bus (also called T-bus) to select the target device's address, design verification and test resources can use their own protocols to communicate with target devices. Third, because the test circuits are not in series with the functional circuits, there are no performance penalties. Fourth, by including real-time-addressable serial and direct-access ports, the control and observation circuits can test themselves fully.

The drawback of this approach is the need for boards

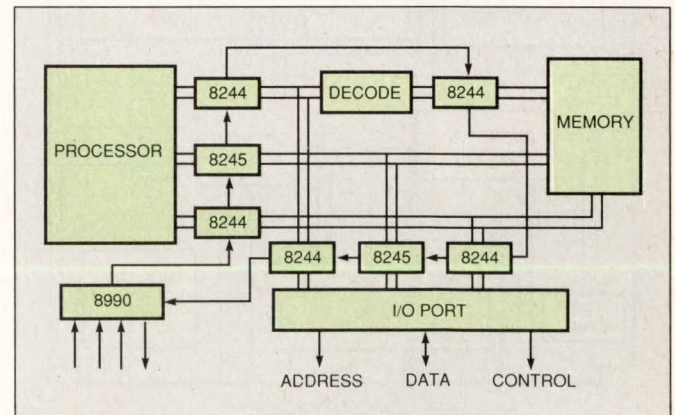


Fig 6—Where performance restrictions do not preclude it, the ideal approach is to replace single-function parts with parts that include boundary-scan features. These parts let you partition, control, and observe your circuit.

BOUNDARY-SCAN TESTING

to include dedicated testability circuits and for MCMs to include additional dice. One of the unfortunate rules of design for testability (or design for manufacturability or serviceability, for that matter) is that nothing is free. To eliminate the extra chips, you can embed the equivalent circuits in an ASIC, or you can replace single-function parts with testability circuits in a manner similar to that described earlier for boundary-scan parts.

Testable functional circuits

Fig 8 illustrates the implementation of testable functional circuits. This approach lets you mix scan and non-scan devices on boards and in MCMs without seriously affecting circuit performance or using many extra parts.

Boundary scan, although certainly a welcome member of the IEEE-1149.x family of approved and proposed standards and a valuable testability tool, is not a panacea for all of the world's testing problems. Moreover, until all devices are both scannable and all-digital, the need for new ways to design for testability will continue.

Vendors of in-circuit and combinational automatic-test equipment have already embraced boundary scan to provide "virtual nails" or "silicon nails" in place of real nails (that is, spring-contact probes) in "bed-of-nails" test fixtures. Nevertheless, as long as circuits consist of a mixture of scan and nonscan ICs, test methods must accommodate both device types.

Moreover, although a mixture of virtual and real nails may solve most SMT and FPT testability problems, solving MCM testability problems requires a combination of testability circuits—including boundary-scan circuits—on the chips within MCMs and on the MCM

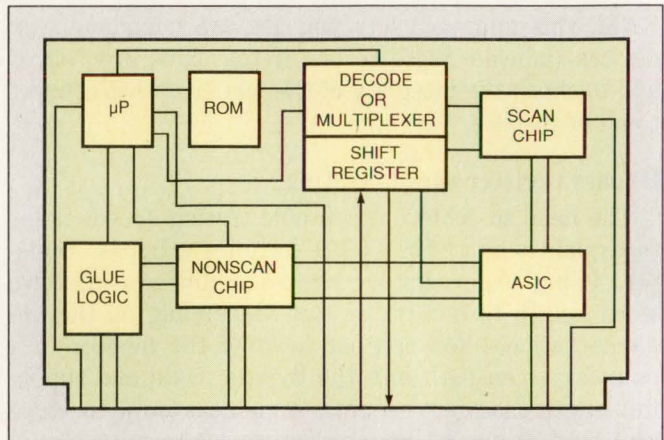


Fig 8—Testable functional circuits let you mix scan and nonscan devices on boards and in MCMs without seriously affecting circuit performance or using many extra parts. Note that this is an IEEE-1149 testability bus.

substrates. Resolving these real testability problems will shorten the time needed for design verification, for logic and fault simulation, and for test generation. Dealing with testability issues will also reduce test and troubleshooting costs in the factory and in the field. EDN

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Author's biography

Jon Turino is President and CEO of Logical Solutions Technology Inc, a consulting firm in Campbell, CA. Jon has more than 20 years of experience in the engineering field and has been a full-time consultant for more than 12 years. He studied engineering and management at West Coast University (Orange, CA) and El Camino College (Via Torrance, CA).

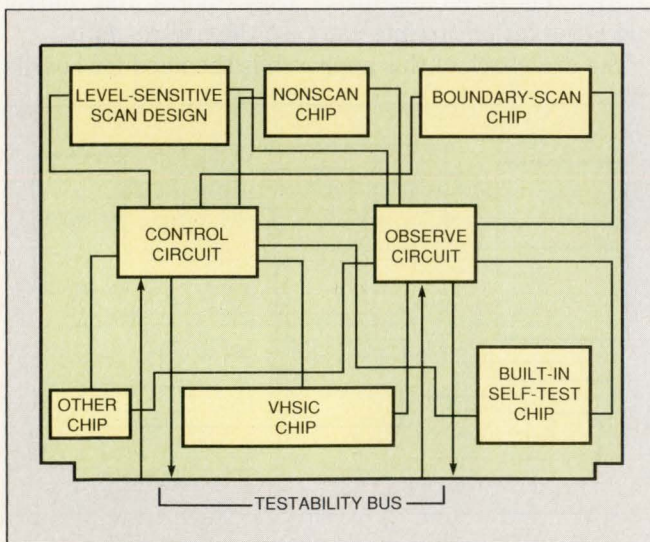
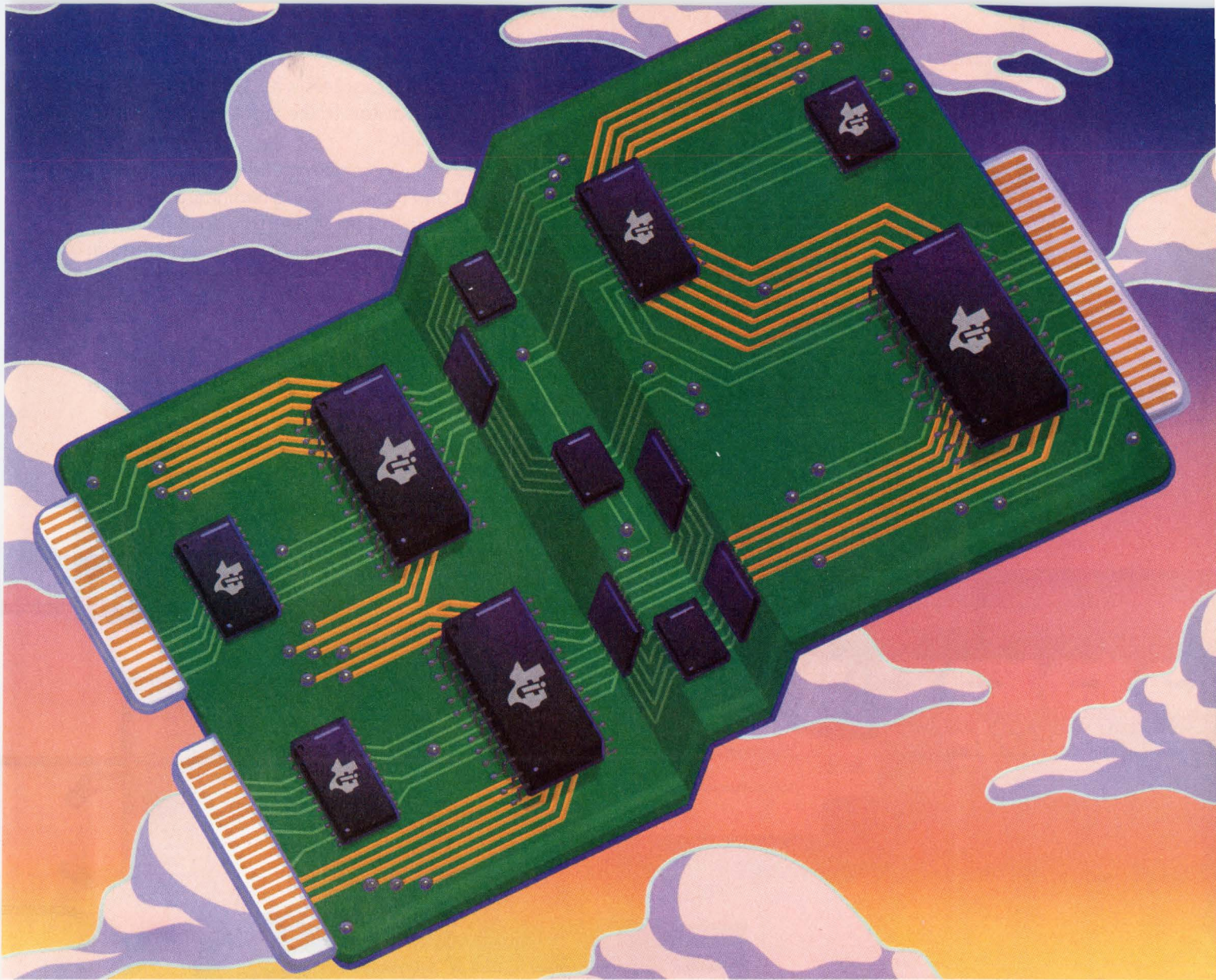


Fig 7—Dedicated control and observation circuits provide coupling from the I/O lines of a subassembly's testability bus to virtually any device on the board or module.

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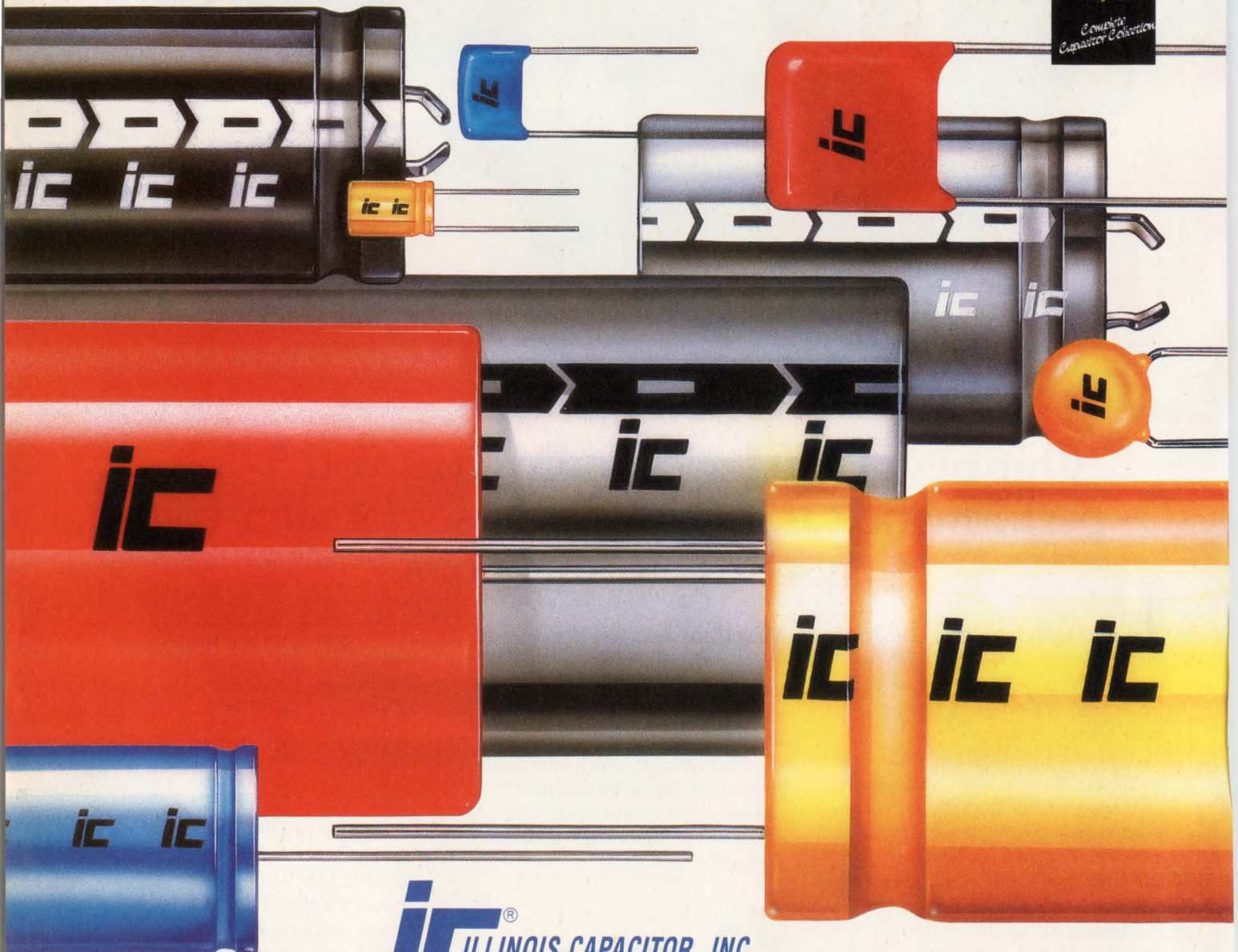
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Common Access Method simplifies development of SCSI device drivers

Chris Borgers and Dave O'Shea, Future Domain Corp

The Common Access Method (CAM) drastically reduces the effort you need to expend when developing device drivers for SCSI peripherals. CAM lets you develop a single device driver for SCSI pc boards that adhere to the CAM standard. Using CAM, applications programs can access SCSI pc boards and peripherals in a consistent manner despite hardware differences.

Writing device drivers for SCSI peripherals is a demanding job: You have to write a driver for every existing SCSI host pc board; you must be an expert on the operation of a SCSI pc board's hardware and the lowest levels of the SCSI protocol; and you must ensure that multiple SCSI drivers don't attempt to control host SCSI board directly. These demands have inspired a new approach for writing SCSI device drivers: the Common Access Method, or CAM. CAM simplifies writing SCSI device drivers in three ways. It provides a software interface that lets SCSI peripherals share the SCSI pc board, conceals the hardware details of the pc board, and insulates the driver developer from the low-level details of the SCSI protocol.

Device drivers fill the gap between an operating system's I/O interface and some type of hardware interface. In the case of SCSI peripheral drivers, the hardware is a SCSI pc board and a SCSI peripheral. Bridg-

ing this interface gap has been problematic. First, each time a designer introduced a new SCSI pc board, he or she had to develop a new driver because SCSI pc boards usually have diverse interfaces. In well-structured code, developing drivers was laborious at best. In poorly structured code, the result was a completely new device driver for each SCSI pc board.

A second problem device-driver developers sometimes face is lack of expertise about the operation of the SCSI pc board's hardware and lack of knowledge about the lowest levels of the SCSI protocol. A programmer had to expend considerable effort programming the host's SCSI pc board instead of concentrating on programming the SCSI device.

A final problem in developing SCSI peripheral drivers occurs when multiple SCSI drivers try to control SCSI pc-board hardware directly. Schemes employing two independent drivers making use of the same SCSI pc board are destined to fail. This danger is especially real in a multiprocessing environment such as Unix. This multidriver-contention problem arises when the operating system treats the I/O devices in a traditional manner, as though they were attached to a dedicated controller board (Fig 1). In contrast, under SCSI, the pc board functions simultaneously as a controller board for many different types of peripherals (Fig 2).

To employ CAM for device-driver development, you must understand the services CAM provides and which data structures you need to use these services. This article presents the CAM services in the order a programmer typically follows when implementing a device driver. The CAM data structures themselves are in a file posted on the EDN bulletin-board system. C-language typedef types will frequently appear in the



The software listings in this article are available on EDN's computer bulletin-board system (BBS). Phone (617) 558-4241 with modem settings 300/1200/2400/9600 8,N,1. Access /freeware SIG and specify (r)ead option followed by (k)eyword search for "MS490".

COMMON ACCESS METHOD

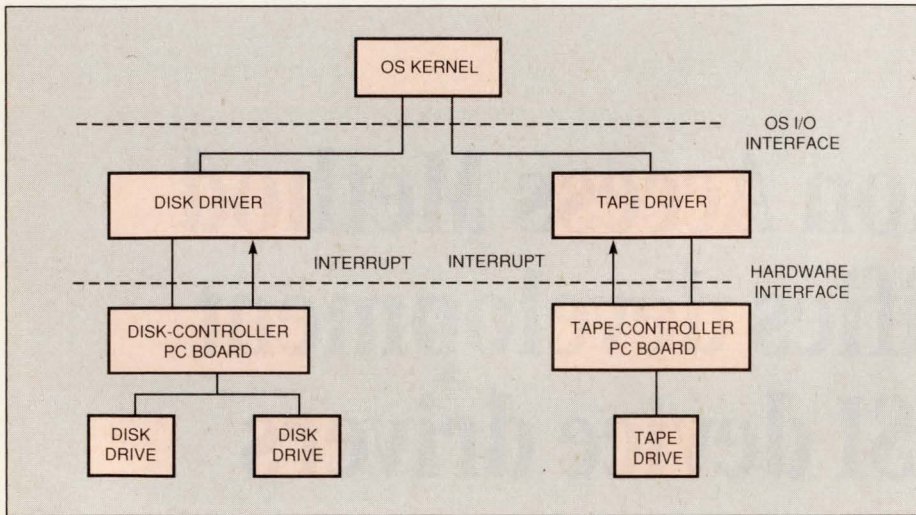


Fig 1—Unlike SCSI systems, older systems have a separate controller board for each type of peripheral device. These older systems can get by with a separate software device driver for each controller board.

examples without definitions. Generally, you can find definitions of these mystery types in the C header file in the **BBS listing**. **Table 1** outlines the major CAM services.

The CAM specification defines data structures independent of programming language. The following examples will use Future Domain Corp's realization of the CAM specification, called Future/CAM. Future/CAM is a C implementation of the CAM specification. All CAM-compliant implementations operate with each other because CAM is a low-level, language-independent specification. To obtain copies of the SCSI-2 and CAM specifications, see **box**, "Getting started."

To use a CAM service, you must fill in a data structure called a CAM control block (CCB) and pass the data structure a pointer to the CAM entry point for

execution. Most operating systems employ a stack-based procedure call to access SCSI hardware such as SCSI. However, MS-DOS uses a different approach. DOS requires you to put the pointer into a μ P register, instead of on the stack, and to issue a software trap (using the Intel 80X86 INT instruction) instead of a procedure call. Whichever method a particular operating system uses, the result is the same: The CAM-compliant device driver gets control of the CPU and accesses the parameters in the CCB.

This example uses a C function:

```
void xpt_action(scsi_header_t * ccb);
```

This function would start a CAM service request and corresponds to a directive from an operating system's drivers to the CAM interface in **Fig 3**. Because you utilize all CAM service requests by setting up a CAM Control Block (CCB), the service request itself is called a CCB request.

Locating CAM services

To use CAM, the host computer must first determine if it is present and locate its entry point. The operations associated with getting the entry point are different for DOS, Unix, OS/2, and Novell Netware. Rather than go into details of each operating system, this discussion settles on Unix 386. Under Unix 386, the CAM entry point is an external C function declared as *xpt_action* above.

SCSI device drivers use three CAM services most frequently: path inquiry, get device type, and execute SCSI I/O. The examples will enumerate these services as FC_PATH_INQUIRY, FC_GET_DEVICE_TYPE, and FC_EXECUTE_SCSI_CMD.

The path-inquiry request determines how many SCSI bus channels are present and how to address

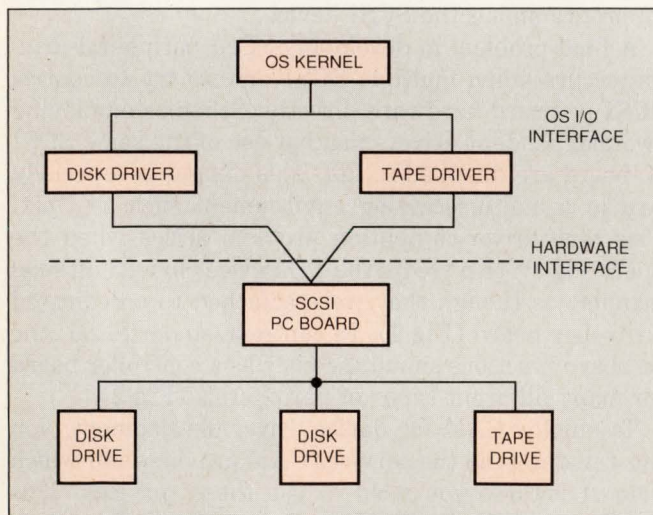


Fig 2—A single channel of a SCSI pc board can handle as many as seven disparate devices, so old-fashioned device drivers can collide disastrously when they try to work through a single SCSI pc board.

Table 1—Major CAM services

Execute SCSI I/O	Transmitting a SCSI command to a SCSI peripheral and transferring any data associated with the command.
Get device type	Obtaining the SCSI-2 Device type for a specific device without performing a SCSI inquiry command.
Path inquiry	Obtaining specific information about a SCSI bus and about how many SCSI buses are in the CAM system.
Abort SCSI command	Aborting an outstanding CAM command request.
Reset SCSI device	Much like an Abort SCSI command, except that it sends the SCSI BUS DEVICE RESET message instead of the SCSI abort message. The abort service does not always end up aborting the CAM request. However, the Reset SCSI Device request always sends the Bus Device Reset message.
Asynchronous callback	Events that are asynchronous in nature can be monitored by a client device driver using this service. Examples of such events are SCSI buses being registered and unregistered in a dynamic fashion (such as under the Novell Netware 386 operating system) or SCSI resets performed by another initiator.
Release SIM queue	Unfreezing the CAM module after certain error handling conditions take place. This service is used only when extensive control is needed over command execution for devices that require complicated error-recovery actions.
Reset SCSI bus	CAM provides this function because there are few situations in the SCSI protocol that require resetting the SCSI bus to resolve the situation. Most of these situations never occur in real-world drivers, and a SCSI driver should never resort to resetting the SCSI bus.

these channels under CAM. The get-device-type request narrows the number of devices for which a device driver must obtain detailed information. For instance, if you're writing a tape driver, you would use this command to find all the tape drives in the system. If you were developing a tape driver that would work only for some particular brand of tape drive, you could use a get-device-type request to find all the tape units and then send a path-inquiry command to the tape units to identify the vendor, model, and even serial number of each unit.

The execute SCSI I/O request is the function device-driver developers use most frequently. The function

lets the driver developer fill in a data structure with SCSI-command information and then call CAM to carry out the SCSI command. Drivers developed for multi-tasking, interrupt-driven operating systems would use CAM's asynchronous-callback mechanism or asynchronous-even-notification capability, which is a critical part of the SCSI CAM specification. Asynchronous even notification is a fancy name for a device driver's interrupt-handling routine. The CAM driver calls this routine when a CAM request completes.

The path-inquiry service lets the calling program obtain information about a SCSI device and the SCSI pc board it hooks to. This information includes the

Getting started

The documents essential for developing a SCSI driver are the ANSI draft SCSI-2 document X3.131-199x and the ANSI CAM document X3T9.2/90-186. The SCSI-2 draft defines the peripheral command sets that programmers use to talk to SCSI peripherals. The CAM document presents an overview of CAM. It specifies data structures in a binary format of bits and bytes rather than in the compatible C-

data-structure format, which Future/CAM uses.

A handy reference book to have nearby is the *SCSI Bench Reference*. The book is a shorthand reference of much of the information found in the SCSI-2 document. It contains general information and specifics for disk- and tape-drive peripherals.

The CAM and SCSI documents, \$25 and \$60, respectively, are available from

Global Engineering Documents
2805 McGaw Ave
Irvine, CA 92714
(714) 261-1455
(800) 854-7179.

The *SCSI Bench Reference*, \$195, is available from

ENDL Publications
14426 Black Walnut Ct
Saratoga, CA 95070
(408) 867-6630.

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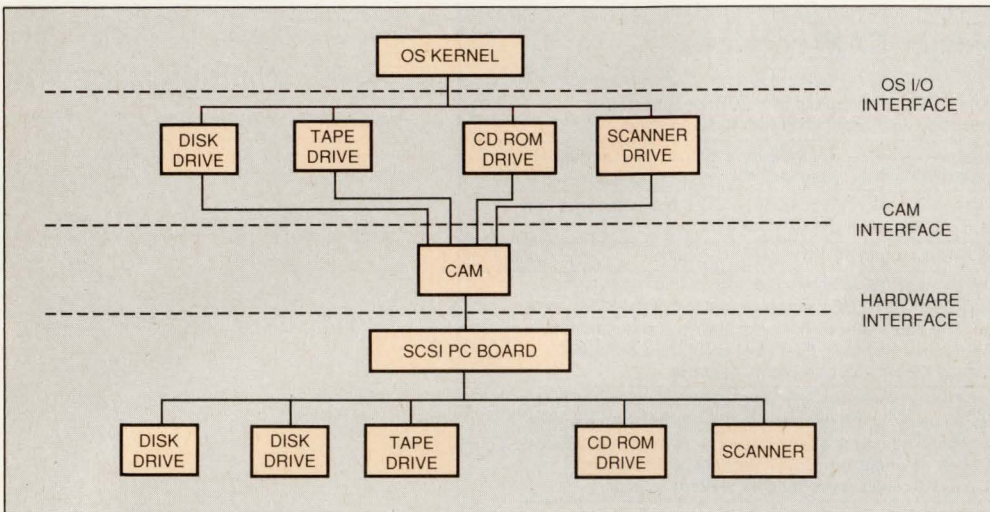


Fig 3—The Common Access Method (CAM) coordinates interchanges between an operating system's many device drivers (which must meet CAM's standards) and their respective peripherals in a uniform manner and eliminates contention for the SCSI host pc board.

CAM revision, the capabilities of the host's SCSI pc board, the vendor of the SCSI interface module, the vendor of the SCSI board, and the SCSI ID of the pc board for that SCSI bus. The path-inquiry command also can find out how many SCSI bus channels are present in the CAM subsystem. This service lets a device driver identify how many SCSI boards are installed, what their capabilities are, how many SCSI buses they support, and who makes the boards.

The following fragment of C code shows how to use the path-inquiry service to obtain the highest path ID in a system:

```
path_inquiry_t pi;
pi.pi_ccb_addr = &pi;
pi.total_length = sizeof(pi);
pi.function_code = FC_PATH_INQUIRY;
pi.pi_flags = 0;
pi.pi_path_id = 0xFF; /* 0xFF is the XPT's reserved PATH address*/
xpt_action((scsi_header_t *) &pi);
```

On most operating systems, the SCSI pc boards will have path IDs starting at 0. This assumption makes coding an initialization routine easy, but it is not always true of all the operating systems that work with CAM. However, assume that this assumption holds true for Unix 386.

Upon return from this call, the only valid field in the CCB will be *pi_adapters_found*. It will contain the last SCSI pc board's path ID or FF_{HEX} if it found no SCSI pc boards.

Once you determine the number of valid paths, you can query each path with a path inquiry:

```
path_inquiry_t pi;
pi.pi_ccb_addr = &pi;
pi.total_length = sizeof(pi);
pi.function_code = FC_PATH_INQUIRY;
pi.pi_flags = 0;
pi.pi_path_id = 0x00; /* Check out path id 0 */
xpt_action((scsi_header_t *) &pi);
```

When you combine several path inquiries, the basic startup code might look like the code in Listing 1.

Identifying device types

Once a device driver identifies which path IDs are valid, it will want to find out which SCSI devices are attached to each SCSI pc board. There are several ways to do this. One technique is first using the FC_GET_DEVICE_TYPE service and then transmitting SCSI inquiry commands via the FC_EXECUTE_SCSI_CMD service. The strategy is to use the FC_GET_DEVICE_TYPE service to limit the number of devices that must receive the inquiry com-

Listing 1

```
typedef struct adapter_t
{
    path_id;
    /* Other fields: (This is an example)
    } adapter_t;

path_inquiry_t pi; /* Path Inquiry CCB data structure */
int highest_id; /* Highest ID for an installed bus */
int id; /* Id to loop through possible path IDs */
adapter_t adapters[10]; /* adapter_t is for example only */
int ad_cnt; /* Number of adapters we have found */

pi.pi_ccb_addr = &pi;
pi.total_length = sizeof(pi);
pi.function_code = FC_PATH_INQUIRY;
pi.pi_flags = 0;
pi.pi_path_id = 0xFF; /* 0xFF is the XPT's reserved PATH address */
xpt_action((scsi_header_t *) &pi);

if (pi.pi_cam_status != CS_COMPLETED) /* Bad status from XPT, bail */
    abort();

highest_id = pi.pi_adapters_present; /* Get highest path id */

/* Search through path ID's from 0 to highest in use. The path ids
 * may not all be valid. Some ID's may have gone invalid because a
 * dynamic SCSI Interface Module (SIM), has deregistered a previously
 * registered id. NOTE: On systems that do not support dynamic
 * registration and deregistration of SCSI buses, then all of the
 * ID's from 0 to highest_id will be valid.
 * The later assumption is frequently applied in systems such as
 * DOS, UNIX, and OS/2, because these operating systems do not allow
 * device drivers to "unload".
 */

for (ad_cnt=0, id=0; id <= highest_id; id++)
{
    pi.pi_path_id = id;
    xpt_action((scsi_header_t *) &pi);
    if (pi.pi_cam_status == CS_COMPLETED)
        adapters[ad_cnt++].path_id = id;
}
}
```


mand. Once FC_GET_DEVICE_TYPE narrows the field of interesting devices, then a SCSI inquiry command can obtain specific information about each device.

To illustrate the technique, consider the case of a floppy-disk drive's device driver. Such a driver can use the FC_GET_DEVICE_TYPE service to identify the ID and LUN (logical unit number) addresses of all the disk-device peripherals in the system. For each of the identified TARGET/LUN combinations, an inquiry command would then obtain additional information about the device. For instance, the command could check to see if the removable-media bit in the inquiry reply was set. If a device did not set this bit, a fixed-disk driver might then choose to ignore this device. Some driver developers might want to support a more limited set of devices by restricting their scope to a specific vendor or model of drive. This information can also be obtained from the SCSI inquiry command.

In fact, the inquiry command can obtain all of the identification information that a driver might want. So why complicate things using the FC_GET_DEVICE_TYPE command? The answer is simple: The command cuts down on the amount of traffic over the SCSI bus during initialization. For instance, imagine three SCSI drivers in a system, one for tape, one for disk, and one for CD-ROM devices. If each driver scanned the SCSI bus using inquiry commands to all target-ID/LUN combinations, the CAM software would have to wait 250 msec (recommended as device-selection timeout) before deciding that a given ID/LUN was not present. This wait could cause considerable initialization delays.

Listing 2 builds on the path-inquiry examples. It assumes that `ad_cnt` is already set and that the `path_id` field has been filled in for each SCSI pc board [`0 . . . ad_cnt`].

Executing a SCSI command

A SCSI driver's mission is threefold—convert an operating-system request into one or more SCSI requests, execute the requests on a SCSI device, and return a status report to the operating system. To succeed at this mission, the device driver must have a method of sending SCSI commands to a device and a way of determining if the command completed properly. If a command fails, a device driver usually wants to know why, so that it can report an error or retry the operation. The FC_EXECUTE_SCSI_CMD service fulfills these needs by letting the operating system know if a command was successful, and if not, why not. Because this service actually does SCSI commands, and because there are many ways to execute SCSI commands, this service has quite a few options, flags, and subfeatures. A typical device driver will use

Listing 2

```
#define MAX_TARGET 8
#define MAX_LUN 8

typedef struct adapter_t
{
    path_id;
    /* Other fields */
} adapter_t;

path_inquiry_t pi; /* Path Inquiry CCB data structure */
int target; /* Id to loop through possible path ids */
int lun; /* Working value for looping through LUN */
adapter_t adapters[10]; /* adapter_t is an example only */
int ad_cnt; /* Number of adapters we have found */
dev_type_t ccb; /* CCB for FC_GET_DEVICE_TYPE service */
scsi_ccb_t inquiry; /* CCC for FC_EXECUTE_SCSI, inquiry cmd */
uchar_t inquiry_data[40]; /* Data buffer for device inquiry info */

/* Initialize the FC_GET_DEVICE_TYPE ccb for use */
ccb.dt_total_length = sizeof(dev_type_t);
ccb.dt_function_code = FC_GET_DEVICE_TYPE;
ccb.dt_ccb_addr = &ccb;
ccb.dt_flags = 0;

/* Initialize the FC_EXECUTE_SCSI_CMD for use in sending an inquiry */
inquiry.sc_total_length = sizeof(scsi_ccb_t);
inquiry.sc_function_code = FC_EXECUTE_SCSI_CMD;
inquiry.sc_addr = &inquiry;
inquiry.sc_flags =
    S_FLG_READ|S_FLG_SIMQ_FRZ_DISABLE|S_FLG_NO_CALLBACK;
inquiry.sc_data = inquiry_data;
inquiry.sc_data_len = 0x20; /* 32 bytes of inquiry data to asked for */
inquiry.sc_cmdlen = 6; /* Inquiry command is 6 bytes long */
inquiry.sc_cmdbyte[0] = 0x12; /* Command function */
inquiry.sc_cmdbyte[1] = 0x00;
inquiry.sc_cmdbyte[2] = 0x00;
inquiry.sc_cmdbyte[3] = 0x00;
inquiry.sc_cmdbyte[4] = 0x20; /* Data length */
inquiry.sc_cmdbyte[5] = 0x00;

for (ad=0; ad < ad_cnt ; ad++)
{
    ccb.dt_path_id = adapters[ad].path_id;
    inquiry.sc_path_id = adapters[ad].path_id;

    for (target=0 ; target < MAX_TARGET ; target++)
    {
        ccb.dt_target = target;
        inquiry.sc_target = target;

        for (lun=0 ; lun < MAX_LUN ; lun++)
        {
            ccb.dt_lun = lun;
            inquiry.sc_lun = lun;

            xpt_action(&ccb); /* Use the FC_GET_DEVICE_TYPE service */
            if (ccb.dt_cam_status != CS_COMPLETED)
                continue;
            else if ((ccb.dt_device_type & DEVT_BITS) == DEVT_DISK)
            {
                /* We have found a disk */
                /* Check if its removable */
                inquiry.sc_cam_status = CS_IN_PROCESS;
                xpt_action(&inquiry);
                while (inquiry.sc_cam_status == CS_IN_PROCESS)
                {
                    /* Spin waiting for completion. This example
                     * spins because we do not want to put in OS
                     * specific operations into this general example.
                     * Normally, a programmer would use OS services to
                     * suspend process execution. Execution would be
                     * resumed via an OS specific means within a
                     * callback routine. In unix, sleep and wakeup
                     * would be used. In OS/2 block and run.....
                     * We just spin for simplicity of example.
                     */
                }
                /* Check inquiry information */
                ; /* Now we could check removable bit, vendor, model
                 * or any other inquiry information we wanted.
                */
            }
            else
                continue;
        }
    }
}
```

only a few of the possible features of the FC_EXECUTE_SCSI_CMD service.

The FC_EXECUTE_SCSI_CMD service uses a `scsi_ccb_t` type of data structure. This C structure has fields for the SCSI command descriptor block (CDB), pointers at input or output data areas, flags for customizing execution behavior, status fields for determining if execution was successful, and an asyn-

COMMON ACCESS METHOD

chronous callback field for identifying where to re-enter the device driver to post a status report about a command. The complete data structure is included in the BBS listing.

You can set up the CDB in one of two ways. The bytes of the CDB can be placed directly into an area in the command control block (CCB)—the `sc_cmd` field. Alternatively, the CCB can include a pointer that identifies the buffer containing the CDB. In C, the field is actually a union of a pointer and an array of unsigned characters (bytes). The `S_FLG_CDB_PTR` flag interprets the state of this union. A set flag means that the union contains a pointer; an unset flag means the union contains the actual CDB bytes.

If you treat the union as if it contains a pointer, then the `S_FLG_CDB_PTR_AT` flag defines the pointer's type as virtual or physical. Leaving this bit unset means the pointer is an operating-system virtual address; setting it means the pointer points to a physical address. Using a virtual address is almost always more convenient because most operating systems require that you use some sort of OS service to convert a virtual address into a physical one.

When the command bytes are put directly into the CCB, the CDB command settings will look like

```
scsi_ccb_t ccb;

ccb.sc_flags &= S_FLG_CDB_PTR;
ccb.sc_cmdbyte[0] = cmdbyte0;
ccb.sc_cmdbyte[1] = cmdbyte1;
...
ccb.sc_cmdbyte[n] = cmdbyteN;
ccb.sc_cmdlen = N;
```

When the pointer is used, the settings will look like

```
unsigned char CDB[12];
scsi_ccb_t ccb;

ccb.sc_flags |= S_FLG_CDB_PTR;
ccb.sc_flags &= S_FLG_CDB_PTR_AT;
ccb.sc_cmdptr = (saddr_t) CDB;
ccb.sc_cmdlen = N;
```

If you have extreme space constraints, you'll probably want to use the inline method. The inline method requires you to copy or build command bytes in place each time. By using the pointer method, you can build commands once when initializing the driver, merely setting a pointer each time you use the command.

A look at the data area

To illustrate how a driver fills in the data fields of an execute SCSI command's CCB, consider the case of a Unix 386 driver trying to perform a SCSI read command. This driver wants blocks of data from the disk put into a specific buffer in memory. Because all Unix kernel memory is continuously addressable at all times and because only a single buffer is available per

request, the following code is a good example of the most common and simplest memory description:

```
scsi_ccb_t ccb;

#define BUFFER_SIZE 0x1000L
uchar_t the_buffer[BUFFER_SIZE];

ccb.sc_flags &= S_FLG_DATA_PTR; /* Virtual address */
ccb.sc_flags &= S_FLG_DIRECTION; /* Clear direction flags */
ccb.sc_flags |= S_FLG_READ; /* Set Read direction */
ccb.sc_flags &= S_FLG_SCATTER_GATHER; /* Simple case */

ccb.sc_data = (saddr_t) the_buffer;
ccb.sc_dataalen = BUFFER_SIZE;
```

Some systems have far more complex memory-addressing problems, and the execute SCSI command CCB has flags and facilities to handle even the most complex situation. CAM supports "scatter-gather" operations and both physical and virtual memory addressing. Thus, CAM can handle both lists of memory locations and virtual memory that is not physically contiguous.

Setting the command addressing

Now that you know the fields that tell CAM which command bytes to send to a device and where in memory to get or put the data associated with the command, it's time to describe the addressing component of the CCB. CCB addressing data comprises three fields: the `sc_path_id` field, the `sc_target` field, and the `sc_lun` field. The `sc_path_id` field specifies the SCSI bus where the peripheral is connected. The `sc_target` field specifies the SCSI ID of the device on that bus; the `sc_lun` field specifies the logical unit number (LUN) of the device at that SCSI ID on the SCSI bus. Together these three fields completely specify a SCSI initiator target LUN connection, or I-T-L nexus. To send a request to a disk device attached to the second SCSI bus in the system (at SCSI ID 1, LUN 0), you would fill in the `sc_path_id`, `sc_target`, and `sc_lun` fields as follows:

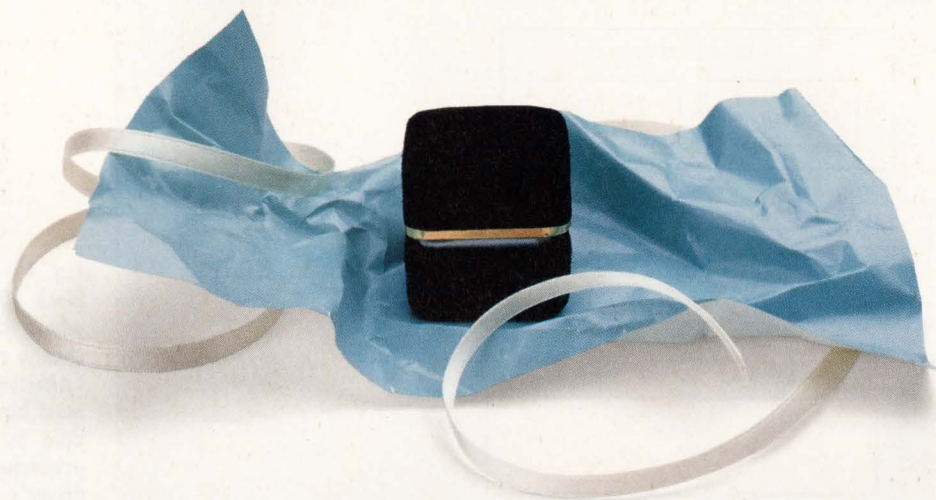
```
scsi_ccb_t ccb;

ccb.sc_path_id = 1; /* Path ID are zero based, 1=second bus */
ccb.sc_target = 1;
ccb.sc_lun = 0;
```

Getting status information

Three other fields play a critical role in determining the success or failure of a CAM command-execution request: the `sc_callback` field, the `sc_cam_status` field, and the `sc_scsi_status` field. The `sc_callback` field specifies the destination address for execution to jump to, using a call/return operation, at the end of a CAM request. This address points to a C-compatible function that behaves much like a standard device-driver interrupt handler (Fig 4). The CAM document refers to the destination address as a "callback" address because

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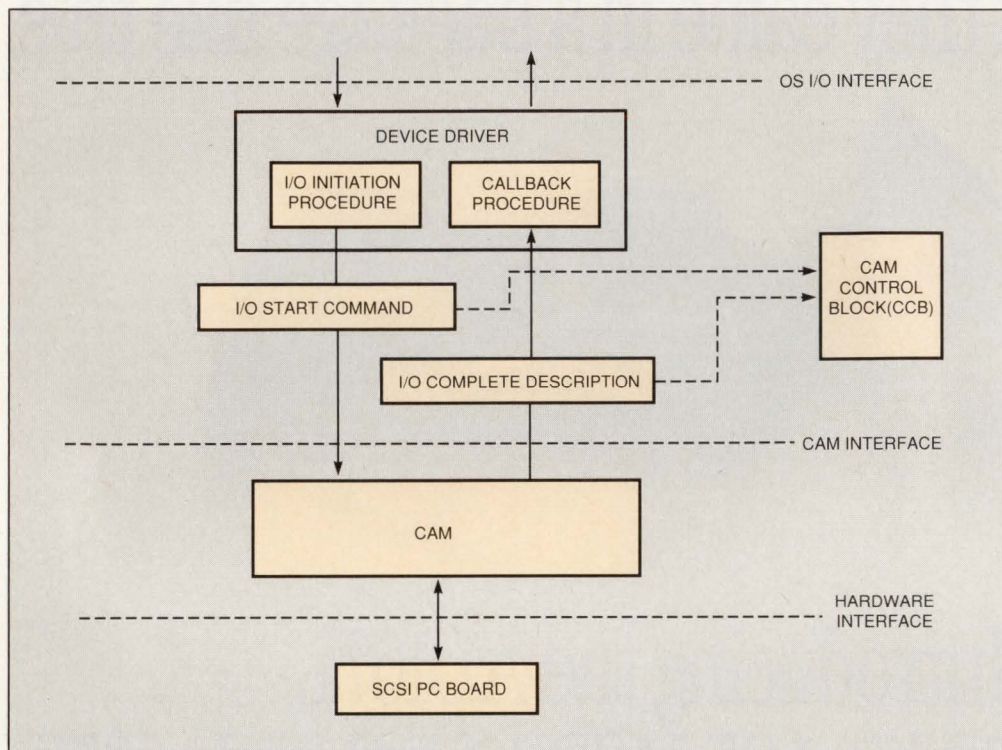


Fig 4—CAM's CAM control block (CCB) is the "mailbox" where drivers and CAM exchange messages. Note that a CAM-compliant device driver must have a "callback" procedure as well as an initiation procedure. CAM invokes a driver's callback procedure to transfer control from CAM back to the driver. The callback mechanism is a sophisticated analog of an interrupt handler and is needed for complex multitasking systems.

the address is the location where the SCSI peripheral driver will be called back by CAM at the completion of the CAM request. The field containing the entry point's location is therefore called `sc_callback`.

At the end of a CAM request, the driver extracts the contents of the `sc_callback` field and calls this address using C conventions. The driver makes the C call using a single argument—the original pointer to the CCB specified in the CAM service-request call. The following C code illustrates the callback semantics:

```
scsi_ccb_t * new_ccb_ptr;
scsi_ccb_t ccb_request;

scsi_ccb_t *
my_callback_routine(scsi_ccb_t * ccb)
{
    /* Do something */
    return (scsi_ccb_t *) 0;
}

ccb_request.sc_callback = my_callback_routine;
```

If CAM has been invoked as

```
xpt_action(&ccb_request);
```

when the CCB request specified by `ccb_request` finishes, CAM will make the following call:

```
new_ccb_ptr =
(*(ccb_request.sc_callback))(&ccb_request);
```

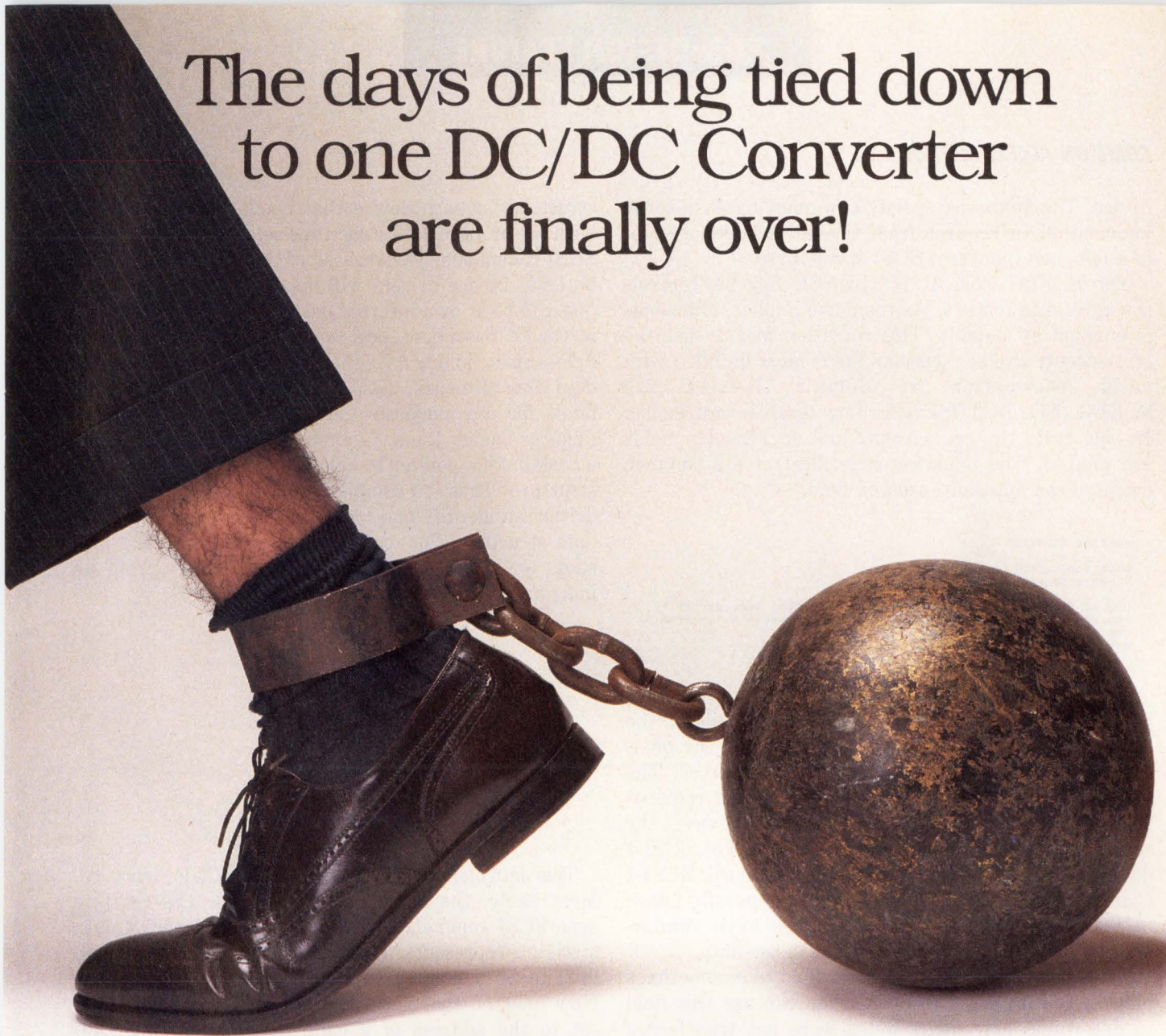
In other words, the callback function is called with the CCB address as its argument.

A SCSI peripheral driver will examine the fields of the posted CCB structure within the callback posting function. The peripheral driver examines the status fields of a completed CAM request within its callback function. Because the CAM service code passes the CCB pointer back to the driver as an argument to the callback function, the SCSI driver's callback function can determine which request has completed and examine all the CCB fields. The key fields to check are the `sc_cam_status` field and the `sc_scsi_status` field.

The `sc_cam_status` field contains the completion status of the CCB request. The `sc_scsi_status` field contains the SCSI status byte from the I-T-L nexus. These two fields often supply sufficient information for device-driver control logic and error-handling logic. However, additional status information is critical to some applications and error-recovery schemes. For these more complex cases, you can take advantage of CAM's autosense feature, which automatically generates SCSI request-sense commands and reports sense-byte information.

SCSI request-sense commands empower complex error-recovery schemes in SCSI device drivers. These request-sense commands are sent when a nonzero SCSI status is received from a SCSI target/LUN device. The results of the SCSI request-sense command—the sense bytes—are available in a data area the CCB specifies. The `sc_senseptr` and `sc_senselen` fields specify where the SCSI driver would like the CAM services to place the sense-byte information gathered from the

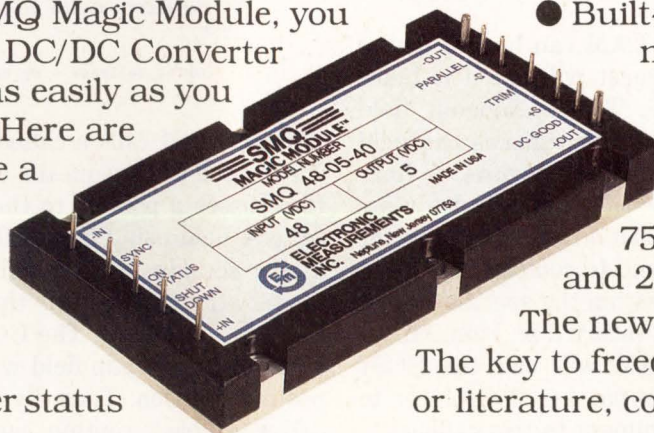
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device. The fields also specify how many bytes of sense information to request from the device upon receipt of a nongood (nonzero) SCSI status byte.

The `S_FLG_NO_AUTO_SENSE` flag bit controls the autosense feature. As the name implies, autosense is enabled by default. This condition means that the `sc_senseptr` and `sc_senselen` fields must be filled with valid information by default. Setting the `S_FLG_NO_AUTOSENSE` flag disables autosense. In this case, the `sc_senseptr` and `sc_senselen` fields are unused. The following code illustrates a common usage of the autosense-related fields:

```
#define SENSELEN 13
scsi_ccb_t ccb;
uchar_t sensebuf[SENSELEN];

ccb.sc_flags &= S_FLG_SENSE_PTR_AT; /* Virtual Addr Buffer */
ccb.sc_flags &= S_FLG_NO_AUTOSENSE; /* Auto sense is enabled */
ccb.sc_senseptr = sensebuf;
ccb.sc_senselen = SENSELEN;
```

The `S_FLG_SENSE_PTR_AT` flag bit modifies the `sc_senseptr` field. When the bit is unset, the `sc_senseptr` field is a virtual address; when the bit is set, the `sc_senseptr` field is a physical address. The format of the sense information follows the request-sense extended-sense format. For SCSI-2 devices, the sense-information format is standardized. For SCSI-1 devices, the sense information is less standard. SCSI-1 Common Command Set Level 2 disks generally follow SCSI-2 specifications. Other devices have vendor-specific information returned in the sense data.

The `sc_residual` field is another field that sometimes plays a role in error recovery. You can use this field to determine how many bytes were not transferred as specified by the `sc_dataalen` field. For instance, if `sc_dataalen` specifies a transfer of 400_{HEX} bytes, but only 100_{HEX} bytes transfer over the SCSI bus, then the `sc_residual` field would contain 300_{HEX} as its value. Frequently, the sense bytes provide this information in the `sc_residual` field.

In addition to data errors, CAM can handle device timeouts as well. A CCB request will fail if it takes longer than a specified time. The `sc_timeout` field specifies that time in seconds, which makes the field useful for device-driver hung-device timeouts. A finer granularity is not really needed for hung-device reactions. A value of -1 specifies that an unlimited amount of time is allowed for a command to complete.

If a CCB doesn't complete within the specified time, the request has failed and will return a `sc_cam_status` value of `CS_TIMEOUT`. CAM will call the SCSI driver's callback routine, again passing the pointer to the CCB instruction as an argument to this callback.

Device drivers often need to link related data structures. For instance, a device driver will have a control

structure for each device that needs to be associated with one or more data structures related to outstanding SCSI commands. The reverse of this situation can also be true. Device drivers will need to relate a CCB request to their own internal data structures. Two fields in the CCB—the `sc_pdp` field and the `sc_rmap_info` field—make linking a CCB and a device driver's private data structure easy. CAM clients can use both of these fields for any purpose: CAM does not examine the fields or modify them. Commonly, these fields provide a back-linking pointer to a device driver's internal data structure. Thus, on completion of a CAM request, the driver can identify and modify the appropriate private data structure. For example, the following code presents an arbitrary internal data structure from an imaginary device driver:

```
typedef struct my_internal_stuff_t
{
    int device_unit;
    int device_status;
    int device_color;
    int device_widget_on;
    int device_scsi_level;
    scsi_ccb_t * device_ccb_ptr;
} my_internal_stuff_t

scsi_ccb_t ccb;
my_internal_stuff_t device;

device.device_ccb_ptr = &ccb;
ccb.sc_pdp = &device;
```

This data structure has an associated CCB structure. Most likely, the device driver will use the CCB to send SCSI commands to the device the internal data structure represents. The driver set the CCB's `sc_pdp` field to be a pointer to the internal data structure. Now imagine that the CCB has its `sc_callback` field set to the address of a callback function, `my_callback_func`:

```
scsi_ccb_t *
my_callback_func(scsi_ccb_t * ccb)
{
    my_internal_stuff_t * my_stuff;
    my_stuff = (scsi_ccb_t *) ccb->sc_pdp;
    my_stuff->device_status = NOT_BUSY_ANYMORE;
}

ccb.sc_callback = my_callback_func;
```

When CAM calls a callback function to post the results of the CCB request's execution, the callback function passes a pointer to the CCB. You can access the `sc_pdp` field using this CCB pointer. The driver filled in the `sc_pdp` field was filled with a pointer to the device structure before the driver sent the CCB to CAM for execution. The CCB still has this unchanged value in the `sc_pdp` field when CAM calls the callback posting function. Thus, by using the `sc_pdp` field, the driver callback routine can access the internal data structures.

In the previous example, the callback routine uses



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the `sc_pda` pointer to reference a device's internal data structure and change the `device_status` field. A device driver could employ the `sc_pdp` field for any use, but an arrangement similar to this example is usually the most powerful use. Only the SCSI driver uses the `sc_rmap_info`, and it can use it for any purpose.

A word about status codes

A device driver needs to determine the completion status of a CCB request so it can plan additional requests. Generally, the driver needs more than simple success or failure information. CAM supplies two fields for determining a CCB structure's completion status: the `sc_scsi_status` field and the `sc_cam_status` field.

The `sc_scsi_status` field is a direct reflection of the SCSI-protocol status-information byte. The SCSI peripheral supplies this information to CAM, and CAM then passes it back to the SCSI peripheral. This field is present only in the execute SCSI I/O CAM service-request CCB because executed SCSI commands are the only means by which a peripheral generates such information. Services, such as the `FC_PATH_INQUIRY`, that do not generate a SCSI command consequently do not have such a field. The following is a list of SCSI status codes (with values in hexadecimal) from the ANSI SCSI-2 specification.

```
00h GOOD
02h CHECK CONDITION
04h CONDITION MET/GOOD
08h BUSY
10h INTERMEDIATE/GOOD
14h INTERMEDIATE/CONDITION MET/GOOD
18h RESERVATION CONFLICT
22h COMMAND TERMINATED
28h QUEUE FULL
```

GOOD means the command proceeded without incident. Any other status code indicates that there's a problem. The CHECK CONDITION code is returned for most errors. To determine the nature of the error, you can use CAM's autosense feature or explicitly send a SCSI Request Sense Information command to the device.

The CAM status field (`sc_cam_status`) contains general information about the success or failure of a CCB request. This field is present in all CCB request-packet formats. (All CAM services can fail for at least one reason.) In a properly debugged device driver using CAM, two CAM status values are most frequent: `CS_COMPLETED` and `CS_COMPLETED_IN_ERROR`. The `CS_COMPLETED` code comes back when CAM completes a request without incident. The `CS_COMPLETED_IN_ERROR` code is the most common "error" code that a device driver will see. For instance, if a SCSI device had a SCSI status of 2 (the CHECK_CONDITION status), the CAM status would be set to `CS_COMPLETED_IN_ERROR`. This error

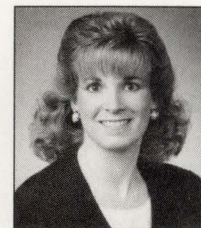
code returns because although the command completed, it did not complete without incident. If autosense is enabled, additional status information would be present in the `sc_senseptr` memory area.

The CAM status byte is divided into three regions. The high bit reflects whether autosense collected the sense information. The `40HEX` bit reflects whether an error in a CCB request froze the SCSI interface module (SIM) internal CCB request queue. CAM will never set the `40HEX` bit because CAM will never freeze the SIM's internal queue. Generally, the `80HEX` bit will be set if you enable autosense in the CAM flags and if a command completed with a non-GOOD SCSI status.

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Authors' biography

Chris Borgers is software marketing manager at Future Domain Corp (Irvine, CA). She is responsible for operating-system and third-party-development support. She helped develop Future/CAM and is a member of the AEA and ANSI SCSI committee. Chris holds a BS degree in information and computer science from the University of California at Irvine. In her spare time, she enjoys snow skiing, horseback riding, reading, and walking the beach.



Dave O'Shea, coauthor of this article, has left Future Domain.

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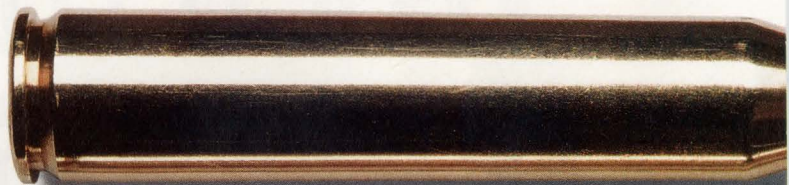
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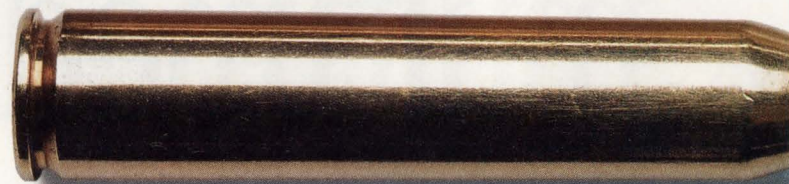
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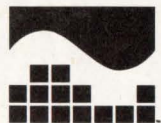


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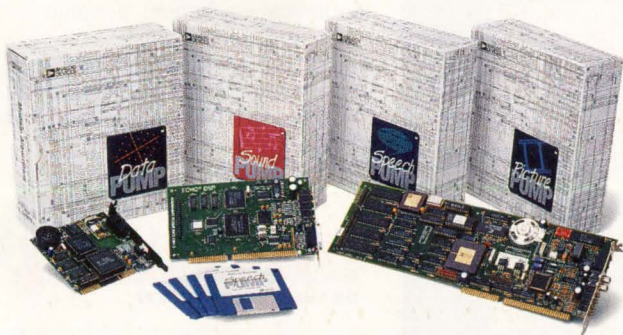
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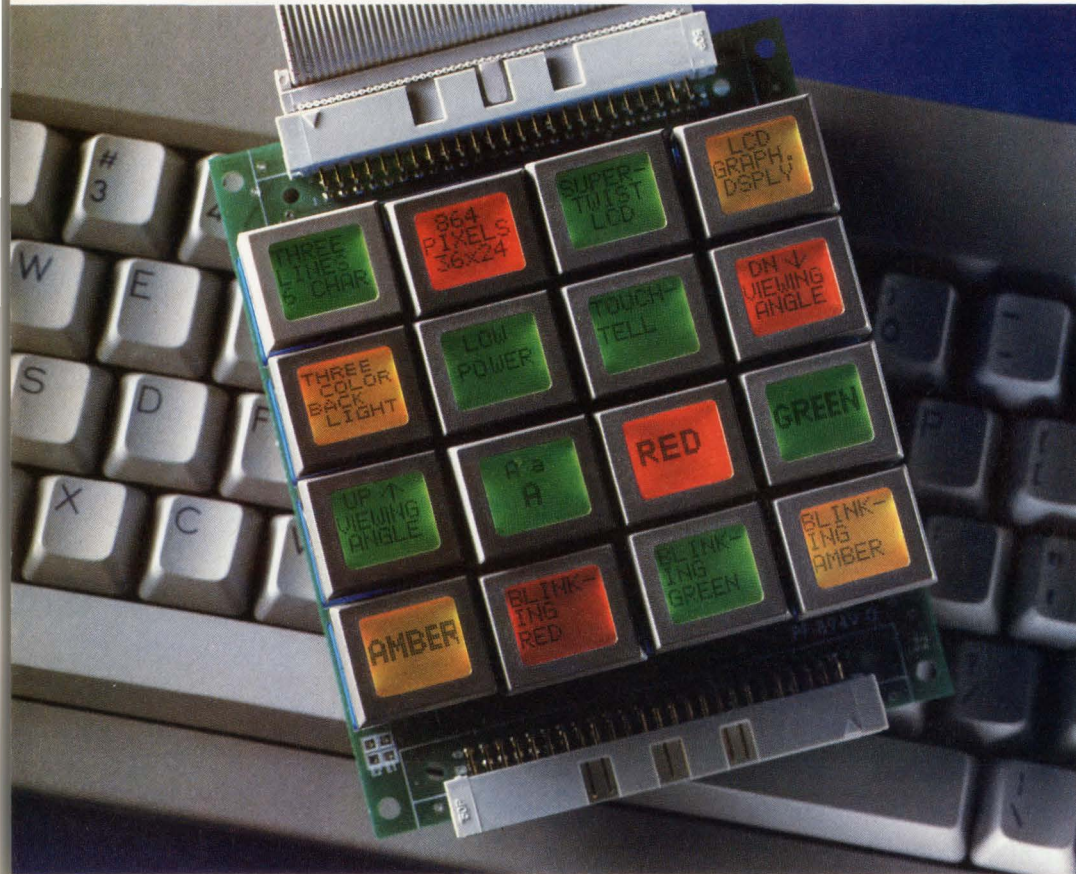
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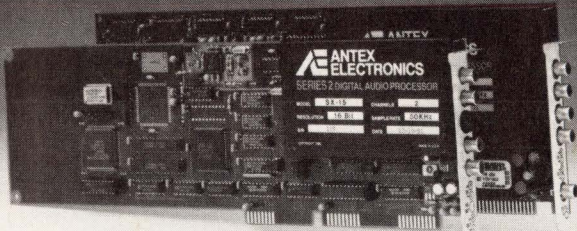
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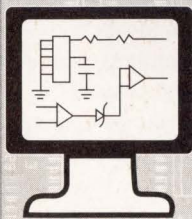


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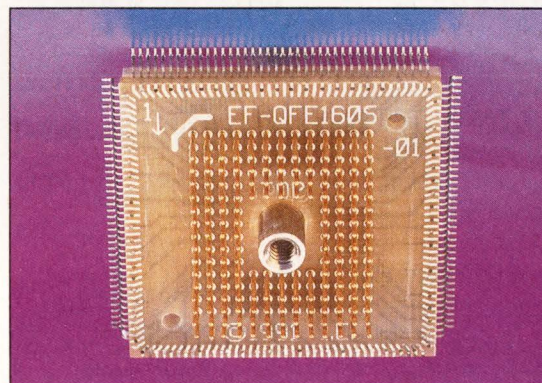
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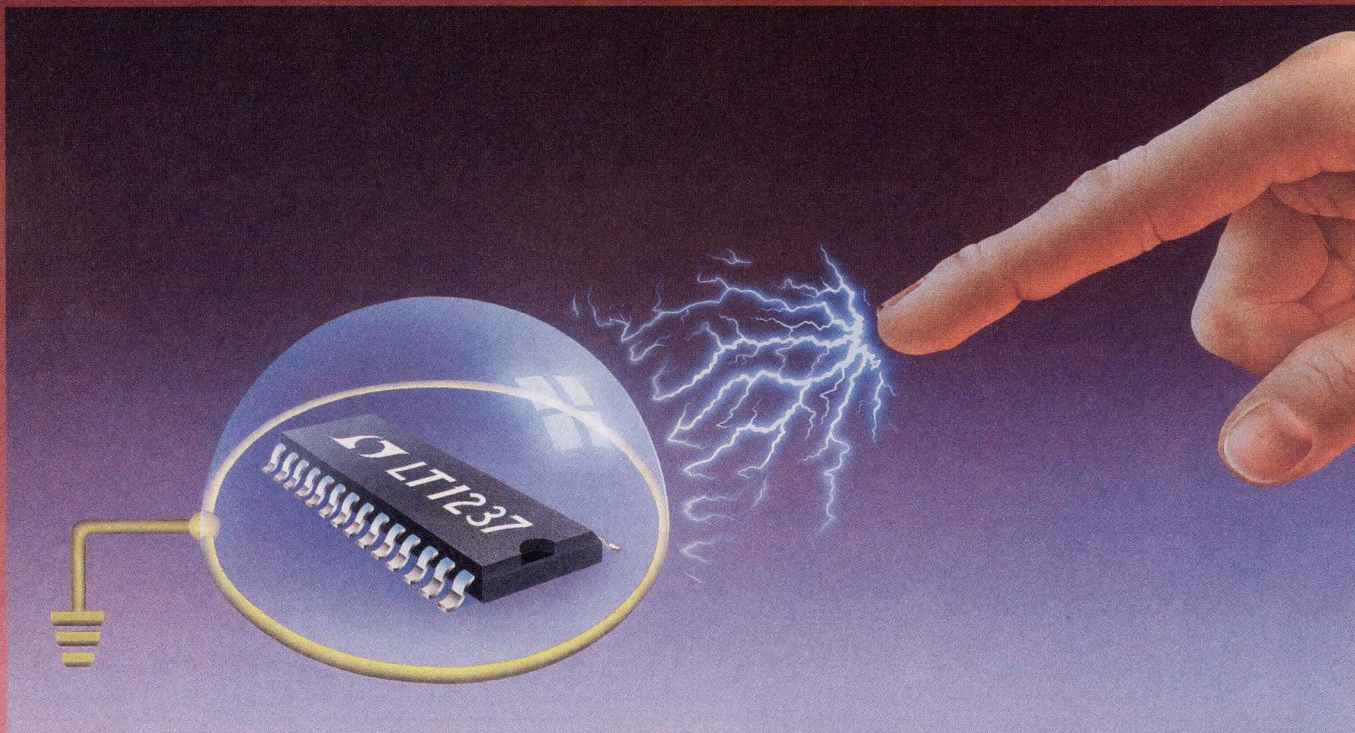
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Logic Interface	5V	5V	3V	3V
3V Operation				X
Driver Disable	X	X	X	X
Receiver Active In Shutdown		X	X	X
Baud Rate	120k	120k	120k	120k

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VCO Spice model is voltage programmable

Donald B Herbert, Consultant, Lomita, CA



The VCO model in Fig 1 is compatible with any commercial or public-domain edition of Spice2. Its primary application is phase-locked-loop simulation in the time domain. The model uses variable damping to stabilize effectively the amplitude of the oscillation over a broad range of frequencies and solution time-step sizes. The model is also voltage programmable. You set three VCO parameters—oscillation frequency (f_o), frequency sensitivity or rate of change in frequency with respect to the input voltage (KS), and oscillation amplitude (A)—external to the model using applied dc voltages. Hence, you don't have to alter the model's internal element values for every application.

The model uses 1-G Ω resistors to satisfy the Spice2 requirement for a minimum of two elements connected to every node or a dc path from a node to ground. Listing 1 contains the Spice2 coding, which you can also download via the EDN BBS. The model's name is VPVCO, and internal nodes 1 through 6 defined on the .SUBCKT line connect the model into an overall simulation. You would connect this subcircuit to another simulation using a statement such as

XVCO 1 2 3 4 5 6 VPVCO.

Node 1 is the VCO input. Node 2 is the output. Node 3 lets you set an initial condition, if necessary. Nodes 4, 5, and 6 let you set the VCO parameters of f_o , A,

Listing 1—Spice2 VCO model

```
.SUBCKT VPVCO 1 2 3 4 5 6
* INPUT OUTPUT XDOT/OMEGA KS A fo
* VOLTAGE-PROGRAMMABLE VCO MODEL
* VOLTAGE ANALOG PARAMETERS:
* KS IS FREQUENCY SENSITIVITY IN KILOHERTZ/VOLT
* A IS AMPLITUDE OF OSCILLATION IN VOLTS
* fo IS OSCILLATION FREQUENCY IN KILOHERTZ WHEN INPUT IS ZERO
RIN 1 0 1G
R45 4 5 1G
R6 6 0 1G
**IMPLEMENT VOLTAGE CONTROLLED FREQUENCY TERMS FOR INTEGRATOR #1
G1A 0 3 POLY(3) 7 0 1 0 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
G1B 0 3 POLY(2) 7 0 6 0 0 0 0 0 0 1
R1 3 0 1G .159154943M
**IMPLEMENT VOLTAGE CONTROLLED FREQUENCY TERMS FOR INTEGRATOR #2
G2A 0 8 POLY(3) 3 0 1 0 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
G2B 0 8 POLY(2) 3 0 6 0 0 0 0 0 0 1
R2 8 0 1G .159154943M
**IMPLEMENT FIRST INTEGRAND WITH VARIABLE DAMPING TERM
EXDD 7 0 POLY(3) 3 0 8 0 5 0
+ 0 0 -1.0 0 0 0 0 0 0 0 -0.1 0 0 -0.1 0 0 1
* - - P2 - - - - - P10 - - - P13 - P15
R7 7 0 1G
**OUTPUT BUFFER STAGE
REO 2 0 1G
EO 2 0 8 0 1
**START-UP CIRCUITRY
VSTART 9 0 PULSE (1 0)
R9 9 0 1G
* SET INITIAL AMPLITUDE TO V(5) VOLTAGE
EIC 10 0 POLY(2) 9 0 5 0 0 0 0 0 0 -1
.ENDS VPVCO
```

and KS using dc voltages. Thus, V(4), V(5), and V(6) are voltage analogs of the respective VCO parameters.

The model uses two integrator circuits. The first integrator computes $V(3) = A \cos(\omega t)$; the second integrator computes $V(8) = A \sin(\omega t)$. In these circuits, the current each pair of transconductance sources (G1A, G1B and G2A, G2B) develops is equal to each integrator input voltage times a gain of $f_o + KS \cdot V_{in}$. This current

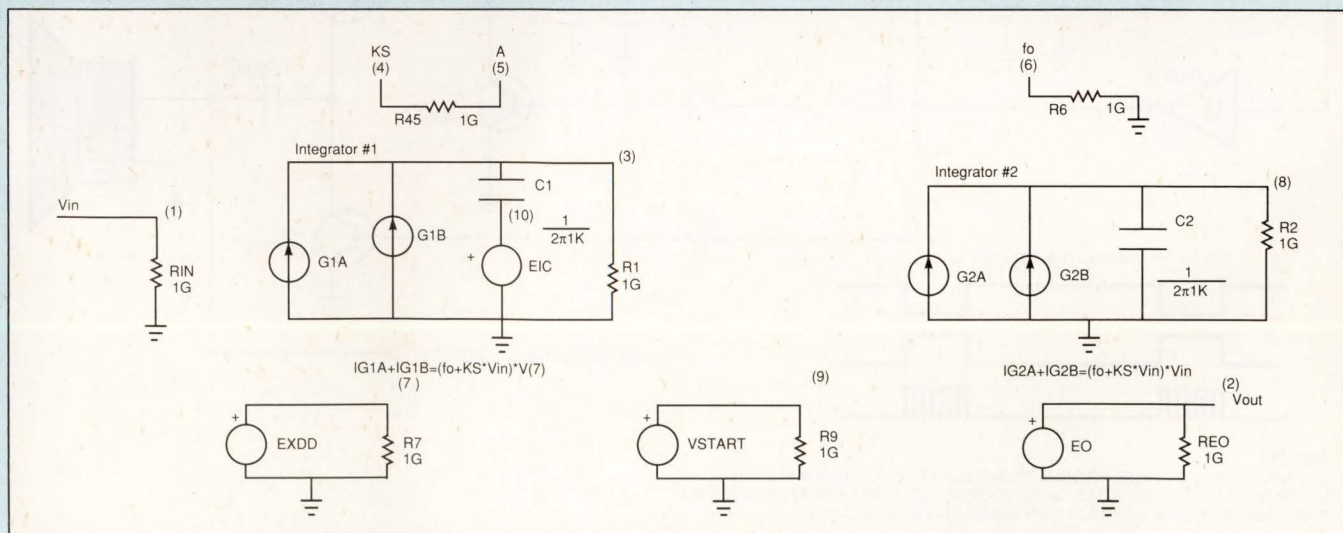


Fig 1—The equivalent circuit of the VCO model includes two integrators and two voltage sources. One of the voltage sources implements a variable damping term (EXDD).

pumps into capacitors C1 and C2, each of which has a value of $1/(2\pi 1K)F$. Thus, the voltage that develops across each capacitor equals the integral of the input voltage times ω , where $\omega = 2\pi(f_0 + KS*Vin)1K$.

The model also uses two voltage-controlled voltage sources. Source EXDD implements the variable damping term that stabilizes the amplitude of oscillation, and source EO provides output buffering.

Finally, source EIC automatically starts the VCO by implementing the product of V(5) and V(9), which sets the voltage on C1 to parameter A at time zero.

The independent source VSTART develops V(9). VSTART is defined to be unity at time zero and zero at the time equal to the first solution time step. However, if you specify initial conditions using the UIC option of the .TRAN statement, you should set V(3) to the A value with a .IC statement.

EDN BBS / DL_SIG #1189

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To Vote For This Design, Circle No. 394

Driver isolates itself from transducer

Lance M Towers, Towers Engineering Services, Huntington Beach, CA

Ultrasonic transducers are part of a variety of circuits such as motion detectors and range finders. One design practice is to operate the transducers as matched pairs of one transmitter and one receiver. Fig 1 presents an alternative design practice in which a single transducer acts as a transceiver.

To maximize the efficiency of an ultrasonic-transceiver design, the low output impedance of the driver must not load the transducer when the device is in the receiving mode. This low-impedance load would dampen the transducer's performance. As a result, isolating the transducer from the driver during the receive-

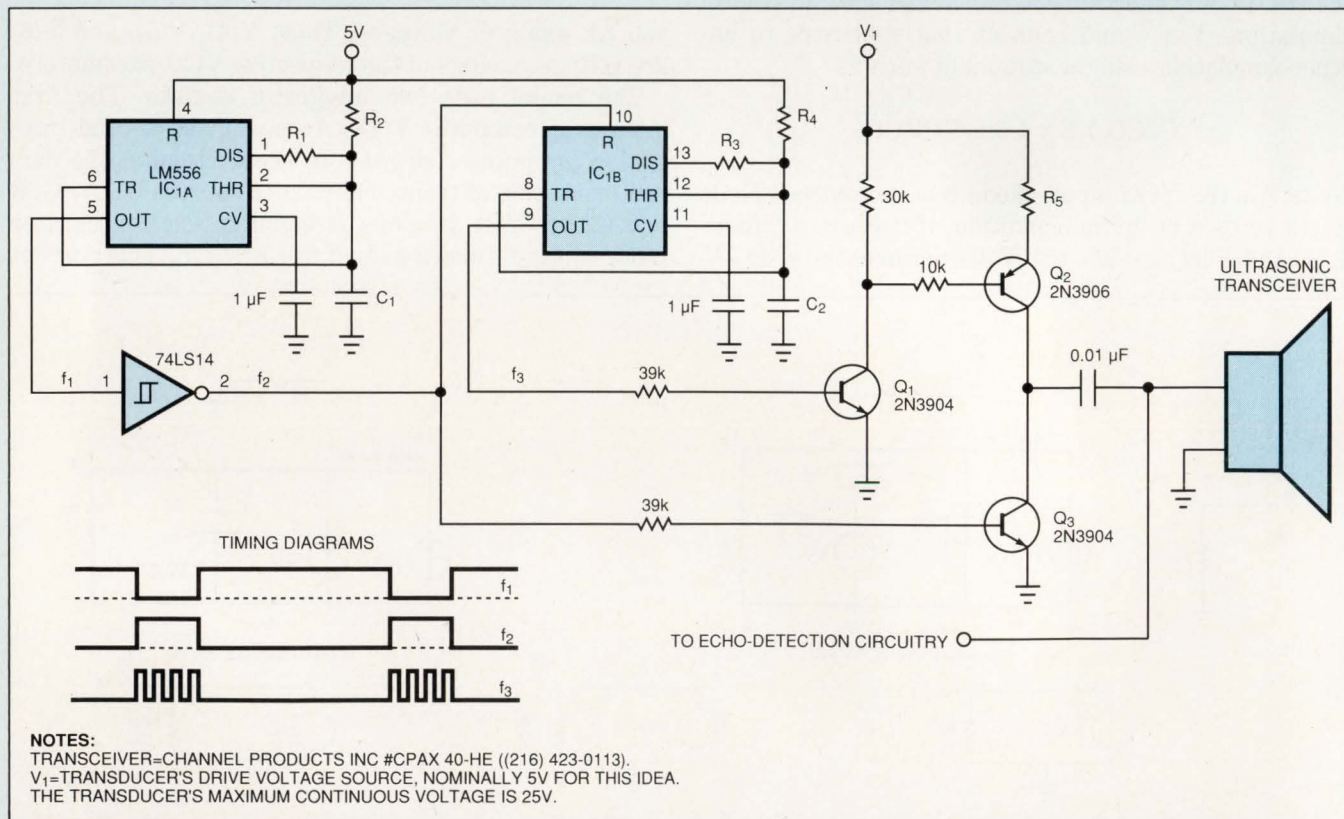
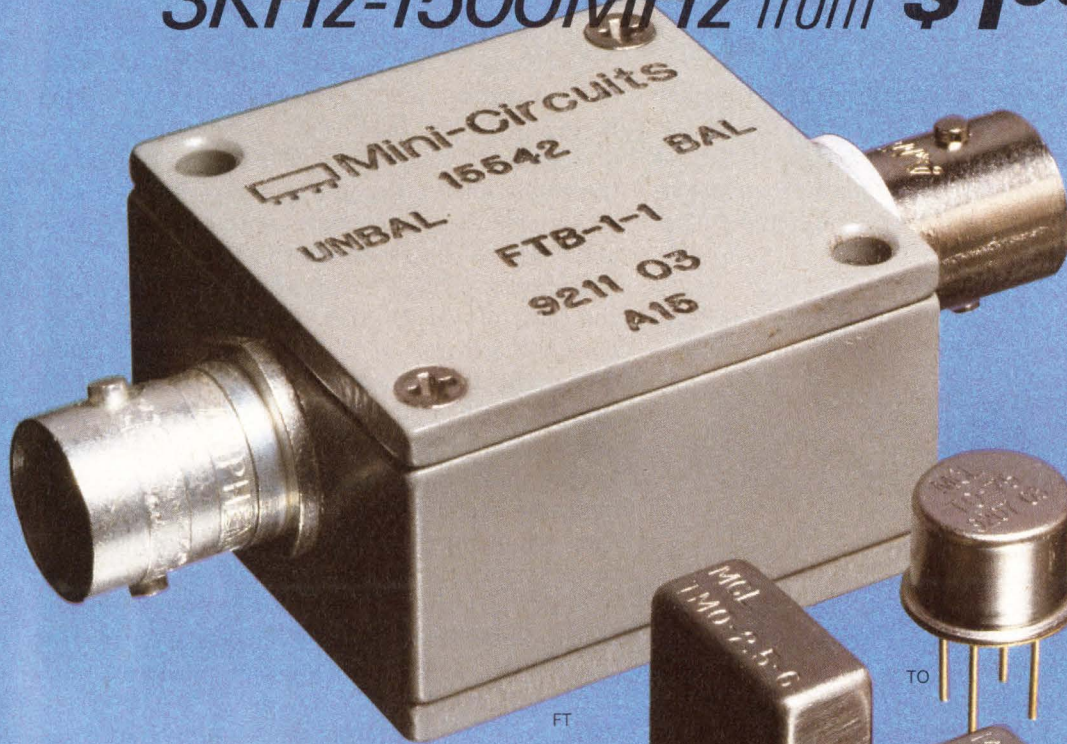


Fig 1—During the transducer's receiving mode, the reverse bias on the base-emitter junctions of Q₂ and Q₃ isolates the driver from the transducer.

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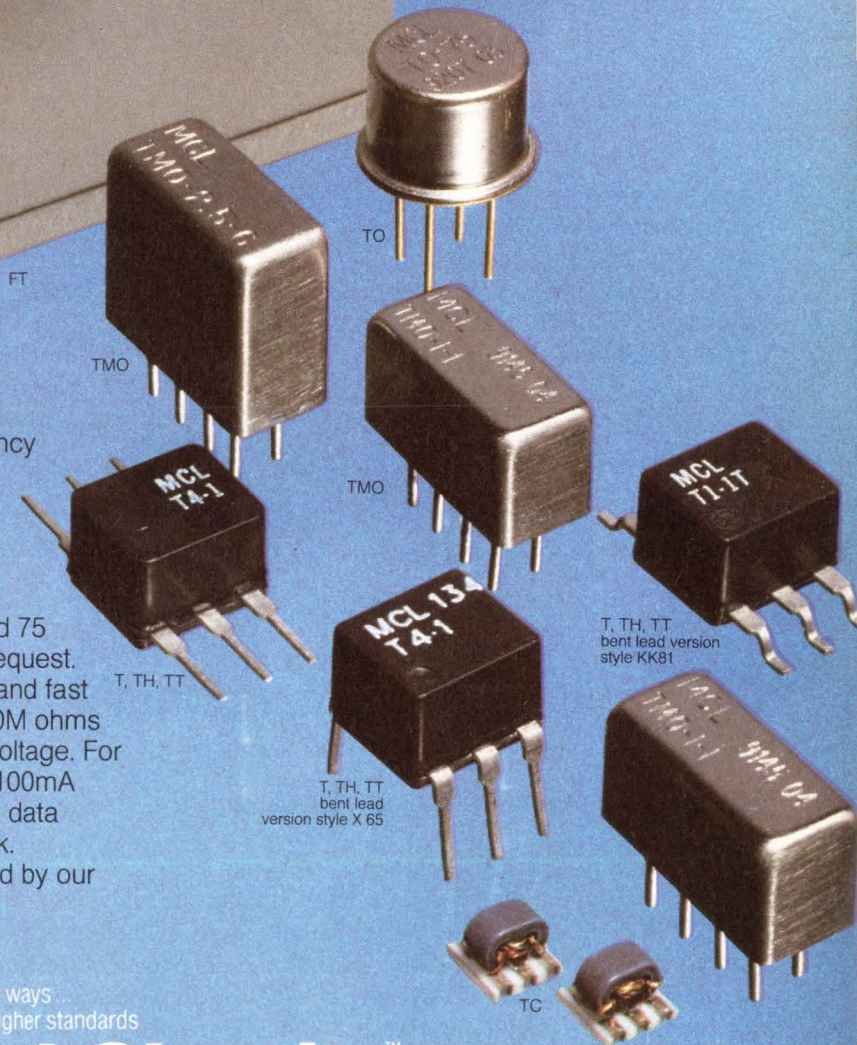
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ing mode is necessary so the transducer sees only the higher input impedance of the receiving amplifier. Circuits can achieve this isolation by using relays, solid-state switches, or the design's inherent ability to achieve isolation. **Fig 1's** circuit has an inherent ability to isolate itself from the transducer during the receiving mode.

The LM556 dual timer, IC₁, creates the transmission's periodic pulse train. The first timer in the device, IC_{1A}, creates the transmission and receiving durations (see f_1 of the timing diagram). The following equations determine f_1 ; t_1 and t_2 are output time high and output time low, respectively.

$$f = \frac{1}{t_1 + t_2} \quad (1)$$

$$\text{duty cycle} = \frac{R_1}{R_2 + 2R_1}$$

$$t_1 = 0.693(R_1 + R_2)C_1$$

$$t_2 = 0.693 R_1 C_1.$$

Because the IC_{1A}'s minimum duty cycle is 50%, the circuit inverts the output (f_1) to obtain the desired duty cycle (see f_2 of the timing diagram).

The second timer, IC_{1B}, generates the resonant frequency of the ultrasonic transducer according to **Eq 1** and the following two equations:

$$t_1 = 0.693 R_4 C_2$$

$$t_2 = \left(\frac{R_3 R_4}{R_3 + R_4} \right) C_2 \ln \left(\frac{R_4 - 2R_3}{2R_4 - R_3} \right).$$

Signal f_2 controls the IC_{1A}'s reset pin. When the reset is low, the timer's output is correspondingly low. When the reset is high, the timer oscillates. This timer configuration produces a signal that contains a periodic high-frequency burst (see f_3 of the timing diagram).

Signals f_2 and f_3 control the operation of Q₃ and Q₁, respectively. When f_2 is high (transmission mode), the base-to-emitter junction of Q₃ is forward-biased. This state lets current flow from the collector to the emitter and creates the ground path for Q₂. When f_2 is low (receiving mode), the junction is reverse-biased. This condition cuts off the collector-to-emitter current flow and removes the ground path of Q₂.

Q₁ inverts f_3 and changes the signal's amplitude to the level of V₁. As the collector of Q₁ oscillates, so does the collector of Q₂. The output of Q₂'s collector drives the transducer. R₅ limits the driver's source current. During the transducer's receiving mode, f_3 is low, which reverse-biases the base-emitter junction of Q₁ and pulls the base of Q₂ high. If the base of Q₂ is high, the base-emitter junction of Q₂ is reverse-biased, thus removing the driver's low-impedance dc path to the transducer.

In short, during the transmission mode, Q₃ is in saturation, and the collector of Q₂ oscillates in sync with the output of IC_{1B}. During the receiving mode, the base-emitter junctions of Q₂ and Q₃ are reverse-biased, which effectively removes the low-impedance dc source and the ground path of the driver to the transducer. Matching the impedance between the transducer and the receiving amplifier results in maximum efficiency.

EDN BBS /DI_SIG #1187

EDN

To Vote For This Design, Circle No. 395

Data pipeline has programmable depth

Valentin Jordanov, University of Michigan, Ann Arbor, MI



In some fast DSP systems, delaying the data leaving the digitizer for a fixed amount of time is necessary. The delay usually equals the number of clock cycles necessary to shift the data from the input to the output of the delay device. In applications such as peak detection that use a moving average filter, the ideal data-delay circuit is both fast and programmable. The data pipeline in **Fig 1** has a digitally programmable depth and can shift 8-bit data words at 66 MHz.

The circuit consists of a synchronous FIFO register, IC₁, and a control circuit implemented in a PLD, IC₂. **Listing 1**, which you can also download via the EDN BBS, is the proLogic compiler source code that configures the EP630 (IC₂) for this application. The synchronous FIFO register operates in single-clock mode; that is, RCLK and WCLK connect to a common clock signal, CLK. The low-to-high transition of CLK shifts data in and out of IC₁. When RESET is low, the FIFO register resets. When RESET is low and CLK goes

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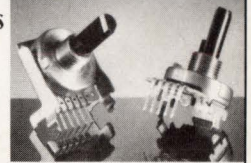


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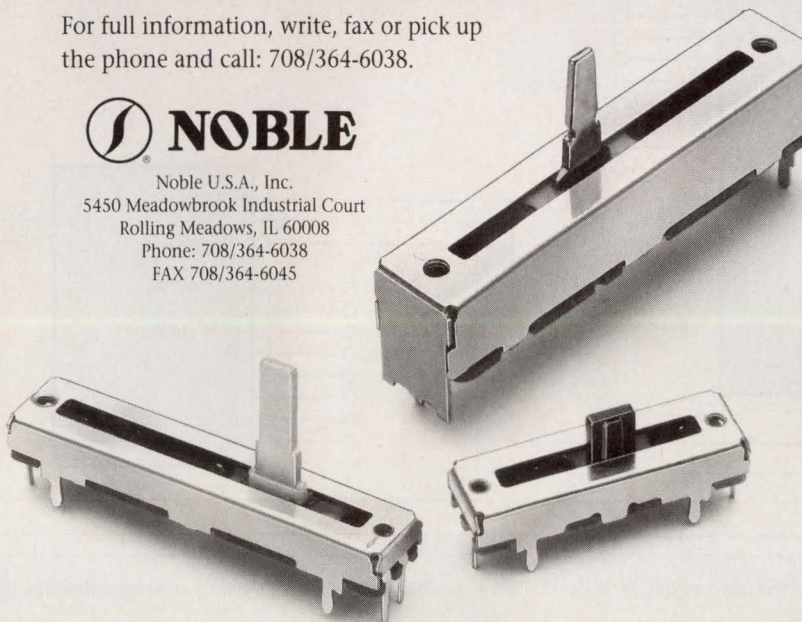
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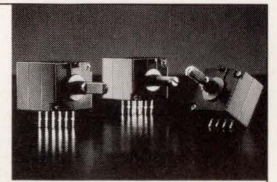
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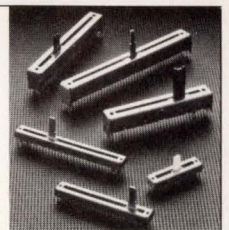
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high, IC₂ loads the digital code, or DEPTH CODE, present at the P₀ through P₇ inputs into an 8-bit down counter. At this time, IC₂ also sets the read- and write-enable signals (REN and WEN, respectively) to an

inactive high state. When RESET is high, the data at IC₂'s inputs doesn't affect the content of the counter.

The first rising edge of CLK following the RESET transition to high causes the signal WAIT to go low (refer to Listing 1). As a result, the next low-to-high CLK transition sets WEN low. Thus, one clock-cycle delay exists between RESET and the WEN, which ensures that the FIFO register operates properly. When WEN is low, the FIFO write operation is enabled, and the counter begins its countdown. The counter's content decreases by one at every low-to-high CLK transition until it reaches the state 01H. Upon reaching this state, the signal REN goes low, which initiates a FIFO read operation. The low states on REN and WEN do not change until the next active reset.

The pipeline's depth is equal to the number of clock cycles elapsed between the high-to-low transitions of WEN and REN. Due to the latency timing of IC₁ at the empty boundary condition, the minimum programmable depth is three data words. This depth corresponds to P₀ through P₇ codes equal to 01H, 02H, or 03H. Input codes equal to 00H set the delay between WEN and REN to 256 cycles. All other hexadecimal values of DEPTH CODE represent the hexadecimal number of the pipeline depth.

EDN BBS /DI_SIG #1190

EDN

To Vote For This Design, Circle No. 396

Listing 1—proLogic compiler source code for data-delay circuit

```

title ( Device: EP630
        Application: Data Pipeline with Programmable Depth
                  ID772200 control circuit
        Author: Valentin Jordanov
                University of Michigan
)

include p630; /* the device description header */
include p630.typ; /* the type header */
include cntnr; /* the -- (countdown) operator */
include xor; /* the % (exclusive or) operator */

define count = (q\7..0); /* counter */
define pdata = (p\7..0); /* parallel data P0..P7 */
define ce = !wait.q & ren.q; /* count enable */
define cnt01 = !q7.q & !q6.q & !q5.q /* counter = 01, active HIGH */
             & !q4.q & !q3.q & !q2.q
             & !q1.q & q0.q;

NOTF count @ (3..5,20..18,16,15); /* T-flip-flop, outputs disabled */
TOTF ren @ 17; /* T-type flip-flop, pin17 */
NORF wen @ 21; /* D-type flip-flop, pin21 */
NORF wait @ 22; /* D-flip-flop, output disabled */
INP pdata @ (2,6..11,14); /* P0..P7, pin2:MSB, pin14:LSB */
INP reset @ 23; /* RESET input, pin23 */

wait.d = !reset; /* wait state */

wen.d = !reset /* FIFO write enable, active LOW */
      | wait.q; /* wait one cycle after reset */

ren.t = !wait.q & cnt01 & ren.q /* FIFO read enable, active LOW */
      | !reset & !ren.q /* delay after wen = LOW until */
      | wait.q & !ren.q; /* counter = 01 */

if (ce = 1) /* if count enable */
  -count.t; /* countdown */
else /* otherwise do nothing or */
  count.t = !reset /* if reset = LOW, load */
            & (pdata % count.q); /* P0..P7 into the counter */

turbo_bit = programmed; /* set turbo mode */
    
```

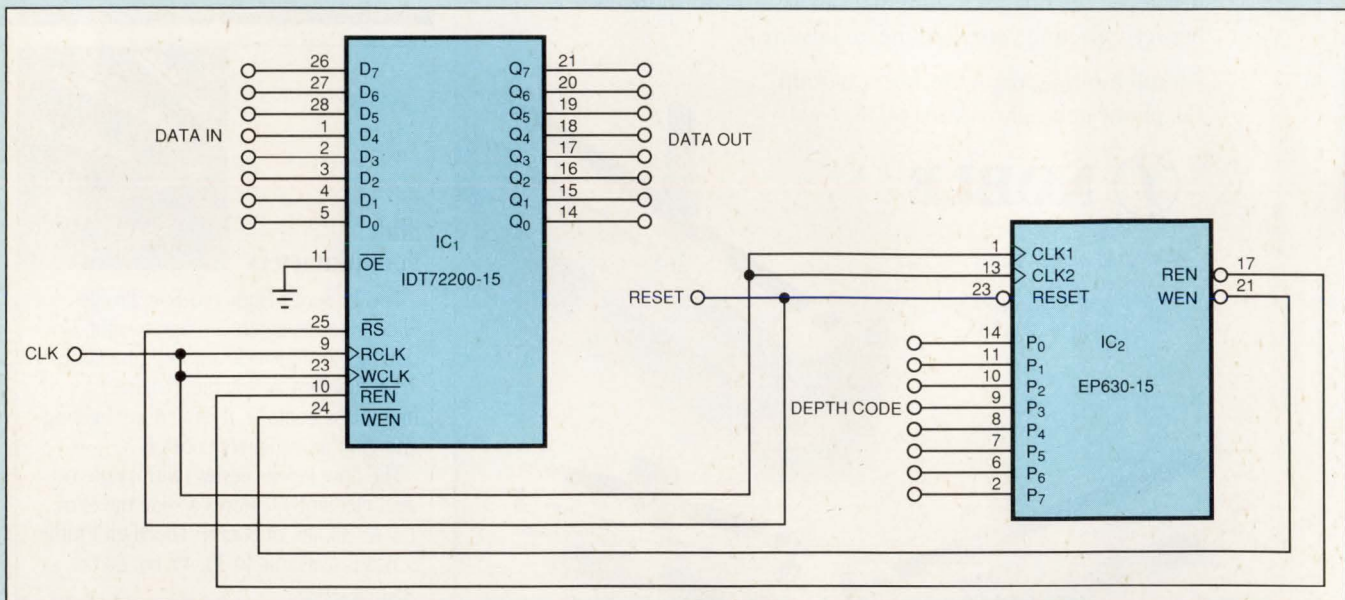


Fig 1—A FIFO register (IC₁) and a control circuit implemented in IC₂'s PLD form a data-delay circuit having a programmable depth and a 66-MHz maximum 8-bit-word shift frequency.

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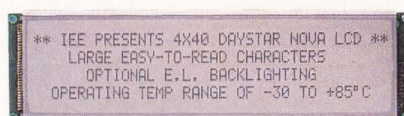


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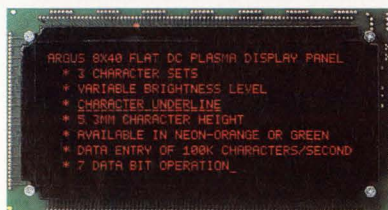
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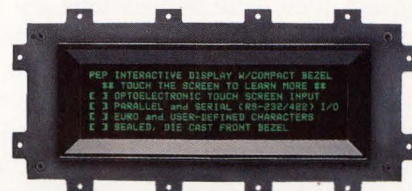
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Reader further eases Sallen-Key filter design

Michael Wyatt, in his Design Idea #1075 "Active filter makes component selection easier," EDN January 20, 1992, pg 136, adds a second op amp to the classic Sallen-Key active lowpass filter, to achieve "greater freedom in component selection." This looks like a useful tool for a circuit designer. However, the increase in freedom is not nearly as great as is implied by this Design Idea. The implications are that, for the classic circuit, the designer is stuck with choosing between the equal-resistor approach and the equal-capacitor approach, and that to get a damping factor less than one, he must choose the equal-resistor approach, and then live with the problem that the calculated capacitances probably won't be close enough to stock values.

A method of obtaining damping factors less than unity in the original Sallen-Key circuit, while achieving the resolution provided by stock resistor values, is to assign standard capacitances such that C_2/C_1 is equal to, or less than, ζ^2 (where ζ is the damping factor), and then calculate resistances.

Referring to the standard Sallen-Key filter (Fig 1a in the Design Idea), a "cookbook" design procedure is

1. Assign ζ . Is the design a complete Butterworth filter, a Bessel filter, or a pole-pair of a larger Butterworth filter, etc?

2. Determine ω_0/ω_c . ω_0 is the undamped natural frequency and ω_c is the cutoff frequency. For your design, this cutoff frequency might be where the response is down 3 dB, or 5%, or some other amount. In any case, this point on the plot of gain magnitude vs frequency, for the pole-pair that exhibits the previously determined ζ , yields numbers, which enable you to calculate ω_0/ω_c .

3. Calculate ω_0 . $\omega_0 = (\omega_0/\omega_c)\omega_c$.

4. Assign C_1 . This is the larger of the two capacitances.

5. Calculate maximum allowable C_2 . $C_2 = C_1\zeta^2$. Assign C_2 .

6. Calculate R_1 . $R_1 = (\zeta + (\zeta^2 - C_1/C_2)^{1/2})/C_2\omega_0$. Assign R_1 .

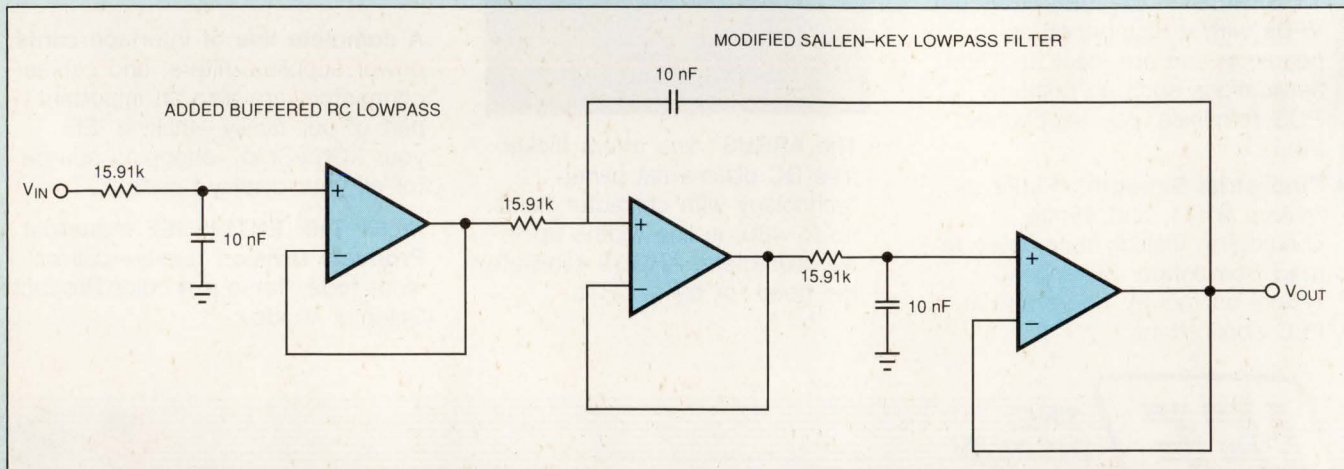
7. Calculate R_2 . $R_2 = 1/(R_1C_1C_2(\omega_0)^2)$. Assign R_2 .

8. Review the component values. Decide whether to iterate steps 4 through 8.

*Keith Timothy
2503 Villa Vista Way
Orange, CA 92667
(714) 998-3135*

I would like to thank Mr Keith Timothy for his comments and suggestions. His approach to the component-value selection by selecting a capacitor ratio less than or equal to the damping ration squared, then computing the resistor values is a valid approach and should yield practical component values. However, this approach may not lead to the equal-capacitor design as mentioned in my Design Idea. As an example, using Mr Timothy's approach to design the second-order Butterworth filter in my Design Idea yields component values of $C_1 = 0.01 \mu\text{F}$, $C_2 = 0.0047 \mu\text{F}$, $R_1 = 29.81 \text{ k}\Omega$, and $R_2 = 18.08 \text{ k}\Omega$.

The component values from my modified Sallen-Key approach are $C_1 = C_2 = 0.01 \mu\text{F}$, $R_1 = 11.25 \text{ k}\Omega$, and $R_2 = 22.50 \text{ k}\Omega$. An additional benefit of my modified Sallen-Key approach is that the filter's performance is



Adding a buffered lowpass filter to a modified Sallen-Key filter yields a third-order Butterworth filter whose resistors' and capacitors' values are equal, respectively.

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ISSUE WINNER

The winning Design Idea for the April 9, 1992, issue is entitled "Transducers form proximity detector," submitted by Maxim Integrated Products (Sunnyvale, CA).

ISSUE WINNER

The winning Design Idea for the April 23, 1992, issue is entitled "Paralleled amplifiers drive loads quietly," submitted by Moshe Gerstenhaber and Mark Murphy of Analog Devices Semiconductor (Wilmington, MA).

less sensitive to component variations than the original Sallen-Key approach.

An interesting adaptation of the modified Sallen-Key filter involves preceding the filter with a simple, buffered, RC lowpass filter section (Fig 1). A third-order Butterworth lowpass (or highpass, by interchanging Rs and Cs) filter results if all the resistor values are equal and all the capacitor values are equal. The -3-dB corner frequency of the third-order Butterworth filter is simply $1/(2\pi RC)$.

*Michael A Wyatt
MS 931-4
SSO Honeywell Inc
Clearwater, FL 34624
(803) 539-5653*

A letter from the front

Thank you very much for your letter and FAX. Unfortunately, there is brutal civil war between Serbs against Muslims and Croats here in Bosnia and Herzegovina. We hope that tremendous efforts to make stable peace will end successfully. If not, we're afraid that the European peace might be seriously jeopardized!

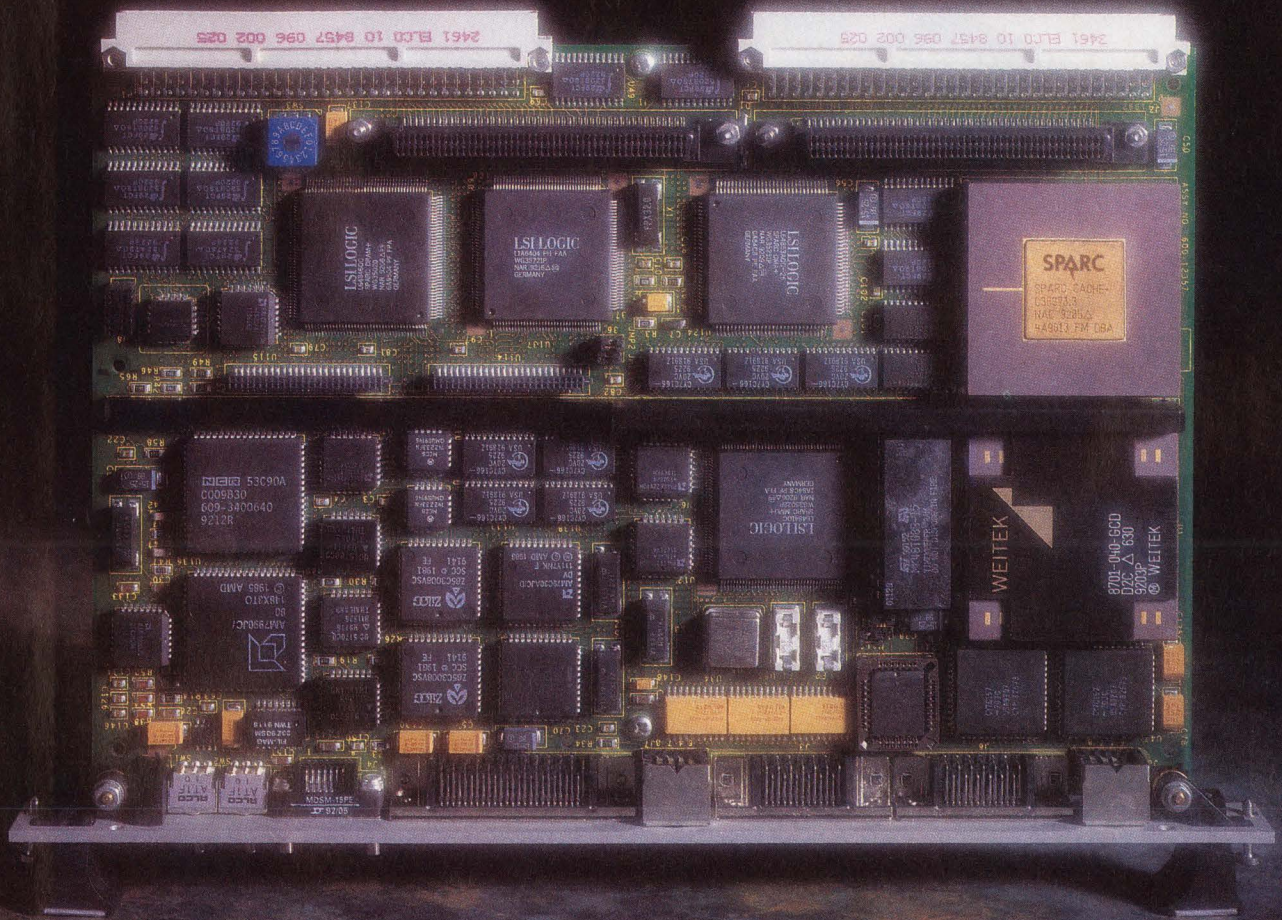
If you decide to publish our Design Idea, we will be satisfied if you can publish it under our names with name of our facility and city only (without the name of the country!).

Names withheld

How to use our bulletin board



This icon identifies those Design Ideas that have computer-readable material posted on EDN's bulletin-board system (BBS). Call our free BBS at (617) 558-4241 (300/1200/2400/9600 8,N,1). Not every Design Idea has downloadable material, but each one does have a BBS number printed at the end of it. Once you get into the system, you can use that number to find more information on a particular idea. If you'd like to comment on any Design Idea, include the number in the subject field of your message.



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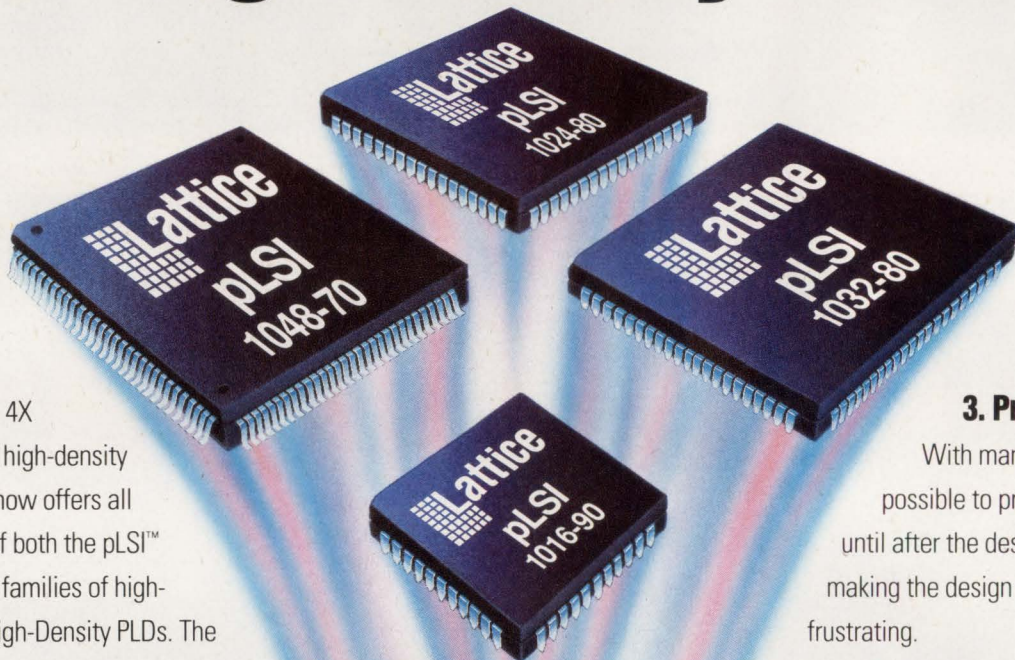
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To achieve a 4X improvement in high-density design, Lattice now offers all four members of both the pLSI™ and the ispLSI™ families of high-performance, High-Density PLDs. The pLSI 1016, 1024, 1032, and 1048 are now available along with their in-system programmable versions in the ispLSI family.

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Circle #40 For Literature

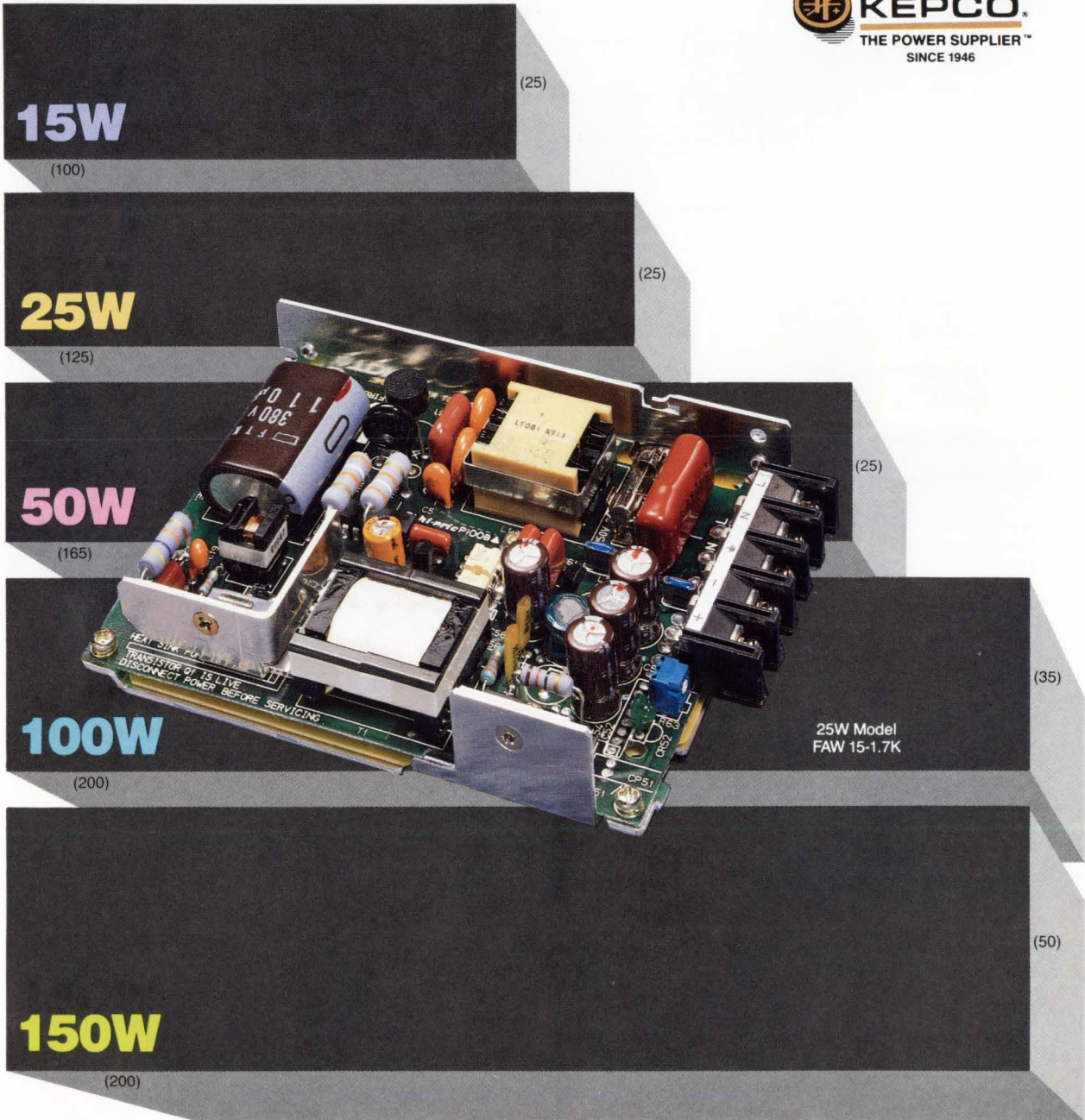
SLIM SWITCHERS

UNIVERSAL INPUT 85-264V a-c

Kepeco's low-profile solutions to your d-c power needs

Surface mount technology combined with advanced magnetics provide quality industrial-grade d-c power in slim packages

All 95mm wide.



15W

(100)

(25)

25W

(125)

(25)

50W

(165)

(25)

100W

(200)

(35)

25W Model
FAW 15-1.7K

150W

(200)

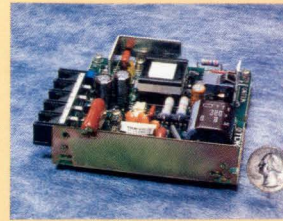
(50)

FAW INPUT CHARACTERISTICS

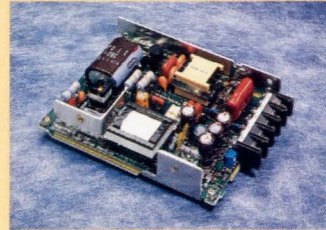
SPECIFICATION		RATING					CONDITION
		All Models					
a-c voltage	nom	120/240V a-c					Single phase
	range	85-264V a-c					
d-c voltage	range	105-370V d-c					Polarity insensitive
Brown-out voltage	min	80V a-c/97V d-c					Ripple, stabilization increase
Frequency	nom	50-60Hz					Single phase
	range	47-440Hz ⁽¹⁾					
EMI		FCC 20780 and VDE 0871					Conducted Class B
Soft-start circuit		Thermistor limiter					
Leakage current	max	0.5 mA UL method					120V a-c 50-60Hz
	max	0.75 mA VDE method					240V a-c 50-60Hz
Startup time	max	500 msec ⁽²⁾					From turn on until d-c output reaches nominal
Holdup time	typ	20 msec					120V a-c
	min	15 msec					100V a-c
Power OK		Green LED plus logic					(See figure 1)
INPUT CURRENT							
(Amperes)		15W	25W	50W	100W	150W	
a-c current	typ	0.3	0.55	1.0	2.0	3.0	120V a-c rms
	max	0.4	0.70	1.2	2.4	3.5	
	typ	0.2	0.35	0.5	1.0	1.5	240V a-c rms
	max	0.3	0.45	0.7	1.4	1.7	
Fuse value		2.0	2.5	3.0	5.0	6.3	250V type 5x20mm
Initial turn-on surge, first half cycle		22	43	45	45	45	120V a-c rms
		34	85	90	90	90	240V a-c rms
Efficiency	typ %	70	70	76	76	76	Max load, nominal input
Circuit type		A	A	B	B	B	
A = Flyback B = Forward converter							
Switching frequency	typ	120KHz					Nominal load

(1) At 440Hz the leakage current exceeds the UL safety specification

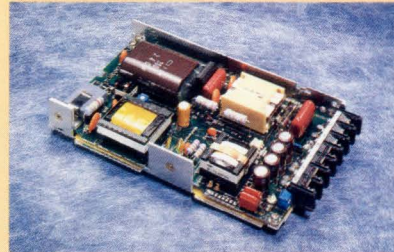
(2) 900 msec for 100W and 150W models



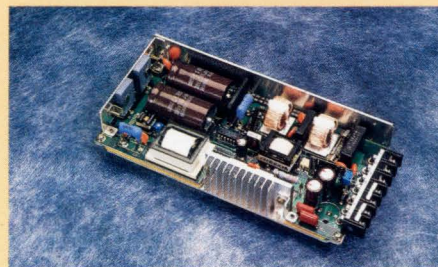
15 Watt model



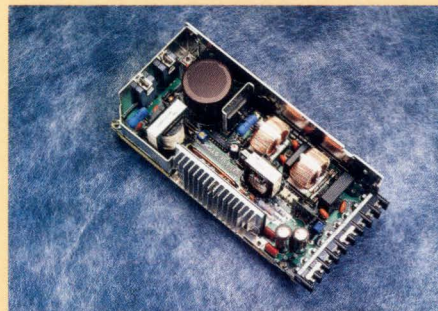
25 Watt model



50 Watt model



100 Watt model



150 Watt model

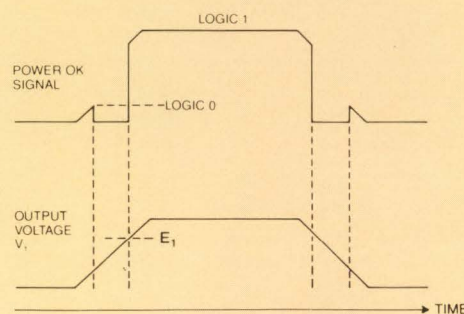
FAW OUTPUT CHARACTERISTICS

SPECIFICATION		RATING		CONDITION
Source effect	typ	1.0%		85 - 132 or 170-264V a-c
	max	2.0%		
Load effect	typ	1.0%		10% to 100% load
	max	2.0%		
Temperature effect	typ	1.0%		Nominal input, rated load
	max	2.0%		
Combined effect	typ	2.0% ⁽¹⁾		Source, load and temperature
	max	4.0%		
Time effect (drift)	typ	0.1%		0.5 - 8.5 hr, max load 25°C
	max	0.5%		
Recovery characteristic	excursion	<4%		Step load 50-100%, rise time >50µs
	recovery	2ms		

(1) FAW 15W and 25W : 2.6%

FIG. 1: POWER OK SIGNAL RELATED TO OUTPUT

	5V model	12V model	15V model	24V model	28V model	48V model
E ₁ (min)	4.5V	9.5V	12V	19V	22V	40V
Logic 1 (min)	2.5V	5V	6V	9V	11V	20V
Logic 1 (max)	< OUTPUT VOLTAGE					



Series FAW wide range input (85-264V a-c) accommodates mains power everywhere without selector. UL listed, CSA certified and approved by TÜV. Onboard VDE 0871 level B EMI filter. Power OK logic. Optional metal enclosure.

TEAR ON DOTTED LINE TO REMOVE AND SAVE.

FEATURES:

- **Power-OK LED:** green.
- **Power-OK logic:** open collector.
- **a-c input 85-264V;**
d-c input 105-370V.
- **Operating frequency:** 120-130KHz.
- **Soft-start circuit:** limits a-c turn-on surge.
- **Adjustable voltage:** internal trimmer.
- **Holding time:** output is sustained by internally stored energy for 20ms typical, 15ms minimum.
- **Built-in EMI filter:** attenuates the conducted noise below the requirements of both FCC 20780 and VDE 0871 for Class B computing devices. Optional perforated metal covers attenuate radiated noise and provide protection.
- **Safety:** FAW are recognized by UL, certified by CSA and approved by TÜV Rheinland.
- **Connections:** input and output screw terminal barrier strip.
- **Remote error sensing:** the 50, 100 and 150W FAW provide separate remote error sense terminals: 0.25V drop/wire.
- **Optional Steel Enclosures:**

Size	15W	25W	50W	100W	150W
Model	CA 24	CA 25	CA 26	CA 27	CA 28

15W

25W

50W

100W

150W

FAW MODEL TABLE						
15 WATT MODELS						
MODEL	OUTPUT VOLTS	ADJUSTMENT RANGE	OUTPUT CURRENT AMPS, 0-50°C	SW RIPPLE mV		NOISE (spike) mV max
				typ	max	
FAW 5-3K	5	4.5- 5.5	0-3.0	15	30	<120
FAW 12-1.3K	12	10.8-13.2	0-1.3	10	30	<190
FAW 15-1K	15	13.5-16.5	0-1.0	10	30	<220
FAW 24-0.7K	24	21.6-26.4	0-0.7	20	50	<310
25 WATT MODELS						
FAW 5-5K	5	4.5- 5.5	0-5.0	31	62	<120
FAW 12-2.1K	12	10.8-13.2	0-2.1	32	65	<190
FAW 15-1.7K	15	13.5-16.5	0-1.7	42	85	<220
FAW 24-1.1K	24	21.6-26.4	0-1.1	57	115	<310
50 WATT MODELS						
FAW 5-10K	5	4.5- 5.5	0-10.0	30	60	<120
FAW 12-4.2K	12	10.8-13.2	0-4.2	35	70	<190
FAW 15-3.4	15	13.5-16.5	0-3.4	45	90	<220
FAW 24-2.1K	24	21.6-26.4	0-2.1	50	100	<310
100 WATT MODELS						
FAW 5-20K	5	4.5- 5.5	0-20	30	60	<120
FAW 12-8.3K	12	10.8-13.2	0-8.3	35	70	<190
FAW 15-6.6K	15	13.5-16.5	0-6.6	45	90	<220
FAW 24-4.2K	24	21.6-26.5	0-4.2	50	100	<310
FAW 28-3.5K	28	25.2-30.8	0-3.5	60	120	<330
FAW 48-2K	48	43.2-52.8	0-2	80	160	<530
150 WATT MODELS						
FAW 5-30K	5	4.5- 5.5	0-30	30	60	<120
FAW 12-12K	12	10.8-13.2	0-12	35	70	<190
FAW 15-10K	15	13.5-16.5	0-10	45	90	<220
FAW 24-6K	24	21.6-26.4	0-6	50	100	<310
FAW 28-5K	28	25.2-30.8	0-5	60	120	<330
FAW 48-2.8K	48	43.2-52.8	0-2.8	80	160	<530


UL RECOGNIZED


CSA CERTIFIED


TÜV APPROVED


This KEPCO product is backed by a firm 1-YEAR WARRANTY

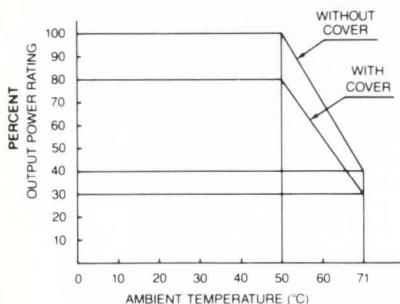


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Series FAW wide range input (85-264V a-c) accommodates mains power everywhere without selector. UL listed, CSA certified and approved by TÜV. Onboard VDE 0871 level B EMI filter. Power OK logic. Optional metal enclosure.

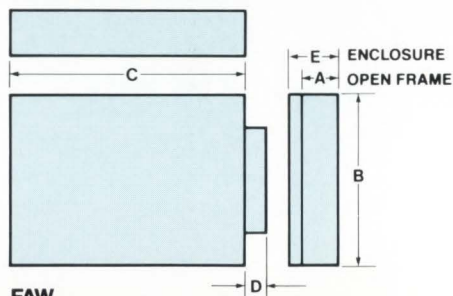
FAW GENERAL SPECIFICATIONS		
SPECIFICATIONS	RATING/DESCRIPTION	CONDITION
Temperature	0 - 71°C (See figure 2)	Operating
	- 40°C to + 85°C	Storage
Humidity	95% RH	Non condensing: operating & storage
Shock	20g, 3 axes (11 msec ± 5 msec pulse duration)	Non operating, 3 shocks each axis
Vibration	5-10Hz: 10mm amplitude 3 axes	Non operating 1 hour each axis
	10 - 55Hz: 2g, 3 axes	
Isolation	Output to case 500V d-c, 100MΩ	25°C, 65%RH
Enclosure	Optional metal	
Type of Construction	PC card, L-chassis	
Cooling	Convection	
Withstand Voltage 15W, 25W, 50W	Input to output	25°C, 65%RH, Y cap removed
	Input to case	
Withstand Voltage 100W, 150W	Input to output	
	Input to case	
Safety: 15W, 25W, 50W	UL 478, CSA EB 1402B, VDE 0806, IEC 380	
Safety: 100W, 150W	UL 1950, CSA EB 1402B, IEC 950	

FIG. 2: OUTPUT POWER VS AMBIENT TEMPERATURE



OUTLINE DIMENSIONAL DRAWINGS

Dimensions in light face type are in inches, dimensions in bold face type are in millimeters.



FAW

MODEL	A ⁽²⁾	B	C	Barrier Strip Protrusion D	E ⁽¹⁾
15 WATTS	0.98	3.74	3.94	0.59	1.18
	25	95	100	15	30
25 WATTS	0.98	3.74	4.92	0.59	1.18
	25	95	125	15	30
50 WATTS	0.98	3.74	6.50	0.59	1.22
	25	95	165	15	31
100 WATTS	1.38	3.74	7.87	0.59	1.50
	35	95	200	15	38
150 WATTS	1.97	3.74	7.87	0.59	2.09
	50	95	200	15	53

(1) With cover (optional) (2) Open frame

Tolerances:
0.04" (1.0 mm) unless otherwise noted

Mounting:
4-40 tapped holes — (2) side;
maximum screw penetration 0.2 (5 mm)

OPEN FRAME DIMENSIONS (HWD)

- 15W:** inches — 0.98 x 3.74 x 3.94
mm — 25 x 95 x 100
- 25W:** inches — 0.98 x 3.74 x 4.92
mm — 25 x 95 x 125
- 50W:** inches — 0.98 x 3.74 x 6.50
mm — 25 x 95 x 165
- 100W:** inches — 1.38 x 3.74 x 7.87
mm — 35 x 95 x 200
- 150W:** inches — 1.97 x 3.74 x 7.87
mm — 50 x 95 x 200

CASED DIMENSIONS (HWD)

- 15W case (CA24):**
inches — 1.18 x 3.74 x 3.94
mm — 30 x 95 x 100
- 25W case (CA25):**
inches — 1.18 x 3.74 x 4.92
mm — 30 x 95 x 125
- 50W case (CA26):**
inches — 1.22 x 3.74 x 6.50
mm — 31 x 95 x 165
- 100W case (CA27):**
inches — 1.50 x 3.74 x 7.87
mm — 38 x 95 x 200
- 150W case (CA28):**
inches — 2.09 x 3.74 x 7.87
mm — 53 x 95 x 200

NET WEIGHT:

- 15W:** 9.52 oz, 270 gm
- 25W:** 10.60 oz, 300 gm
- 50W:** 15.90 oz, 400 gm
- 100W:** 2.6 lbs, 1.2 kg
- 150W:** 3.3 lbs, 1.5 kg

15W

25W

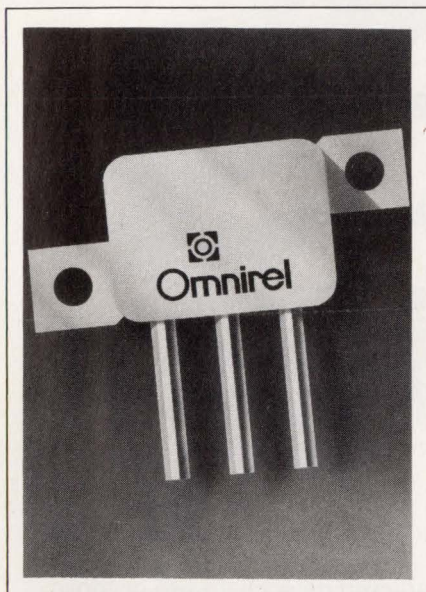
50W

100W

150W



Integrated Circuits



Power MOSFETs. The OM11N60 and OM11N55 are power MOSFETs rated at 600 and 550V, respectively. Current rating is 11A, and the on-resistance is as low as 0.42Ω. The devices come in TO-254 hermetically sealed metal packages with either side or top tabs. The

devices are available with hi-rel screening. OM11N55AA, \$47.50 (100). **Omni-rel Corp**, 205 Crawford St, Leominster, MA 01453. Phone (508) 534-5776. FAX (508) 537-4246. **Circle No. 414**

Dual-in-line power devices. This chip family in plastic DIPs suits power-switching applications. The Power+ Logic devices employ the company's mixed-signal process. The methodology, called Prism, permits microcontrollers (μCs), analog circuits, and power devices to be integrated on a single chip. Chips include the TPIC6259 8-bit addressable latch; the TPIC6273 Octal D-type flip-flop; and the TPIC6595 8-bit shift register. \$1.60 (1000). **Texas Instruments Inc**, Semiconductor Group (SC-92074), Box 809066, Dallas, TX 75380. Phone (214) 995-6611, ext 3990. **Circle No. 415**

Optoisolated power MOSFETs. The TC4803/4804 are optoisolated power MOSFET drivers. The drivers provide 2500V rms of isolation from input to output, and they can drive MOSFET gate

capacitance of 1000 pF to 15V in 45 μsec. Peak current drive is 2A, and they can sink 0.8A. Operating voltage ranges from 10 to 18V. The drivers convert a 5V logic level to an 18V level in 140 nsec. \$1.82 (1000). **Teledyne Components**, 1300 Terra Belle Ave, Mountain View, CA 94039. Phone (415) 968-9241. **Circle No. 416**

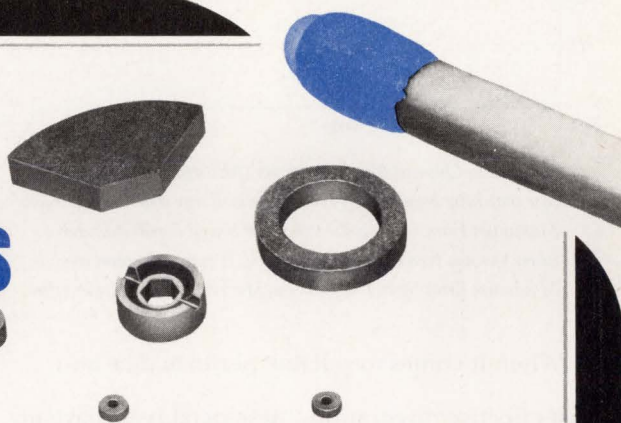
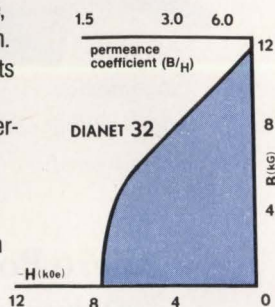
UV PROMs. This UV PROM family features an address access time (t_{AA}) of 25 nsec and a chip select-to-output time (t_{CS}) of 12 nsec. The fast select time permits the chips to operate with 50-MHz DSP chips. The family includes the 8k×8-bit WS57C49C; 4k×8-bit WS57C43C; 2k×8-bit WS57C191C; and 2k×8-bit WS57C291C. From \$9.30 to \$18.05 for CERDIPs; plastic OTPs, from \$5.60 to \$14.75. **WSI**, 47280 Kato Rd, Fremont, CA 94538. Phone (510) 656-5400. FAX (510) 657-5916. **Circle No. 417**

Instrumentation amplifier. The INA131 has a fixed gain of 100. A 3-op-amp design distributes the gain be-

Imagine what you could do with Samarium MGOe 32 Magnets

Another industry first from EPSON

Smaller, thinner, stronger than any other magnets... because they need no bulky anti-corrosion coating... EPSON's new DIANET® 32 Sintered Samarium Cobalt Magnets offer a step forward in mini-magnet design. And the same size/strength advantages benefit larger designs too. You can specify DIANET Series anisotropic magnets with axial or transverse orientation in virtually any size, shape, or thickness you design. EPSON DIANET Series magnets have a very narrow range of deviation in magnetic characteristics and high dimensional accuracy. The high coercive force bH_c is nearly equal to B_r to minimize the influence from external magnetic fields.



DIANET® Series Anisotropic Sintered Samarium Cobalt Magnets

	BHmax MGOe	Br (KG)	bHc (KOe)	iHc
DM-32	28 to 32	11.0 to 11.6	5.5 to 9.5	>6.00
DM-30	26 to 30	10.6 to 11.3	6.0 to 10.0	>7.00
DM-28	27 to 29	10.5 to 11.0	5.0 to 7.0	>5.00
DM-26	25 to 27	10.1 to 10.6	5.0 to 7.0	>5.00
DM-24	23 to 25	9.7 to 10.2	6.0 to 8.0	>6.00
DM-22	21 to 23	9.2 to 9.7	8.0 to 9.2	>8.00
DM-20	19 to 21	8.7 to 9.2	8.5 to 9.2	>8.50
DM-18	17 to 19	8.2 to 8.7	8.0 to 8.7	>8.75
DM-16	15 to 17	7.7 to 8.2	7.5 to 8.2	>9.00

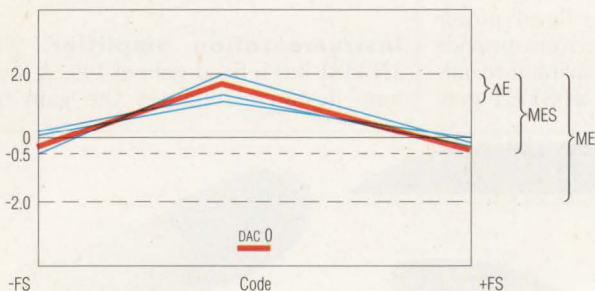
For information, call our Representative

EPSON® EPSON AMERICA, INC.
International Magnaproducts, Inc.

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Eight DACs, one tweak

Calibrating the outputs of a high-precision multiple DAC has never been easier. The MP7610 and MP7611 are the first 14-bit octal DACs to offer matched channel-to-channel performance within 2 LSB across all codes. Make a single V_{REF} adjustment for minimum total error on one channel, and the total error for all eight DACs meets spec. **It's like having one DAC with eight outputs.**

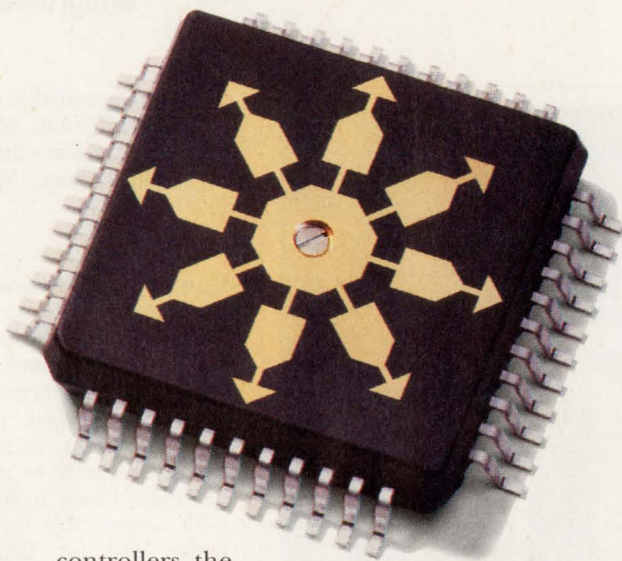


Channel-to-Channel Maximum Error (ΔE) represents the worst-case matching between any two channels at any code. All Channels Maximum Error (ME) is the total error bound for all channels when V_{REF} has been adjusted to give DAC 0 minimum total error. Maximum Error Span (MES) is the Maximum Error minus offset.

When it comes to reliable performance and cost-effective integration, these octal DACs have no match. The MP7610 combines eight 14-bit DACs with output op-amps and a 3-wire serial data interface in a 28-pin PDIP or SOIC package. The MP7611 offers identical DAC performance, with a double-buffered 14-bit parallel digital address and data port, housed in either a 44-pin PQFP or PGA.

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MP7610 and MP7611 satisfy virtually any multi-DAC application. You can even daisy chain two or more MP7610s using the Serial Data Out pin.

For more information about the MP7610 family of 12- and 14-bit octal DACs, call 1-800-765-5350.

If you call now you'll receive a Design Guide, including an application note, data sheets, and a request card for samples. A complete data book of Micro Power Systems' analog and digital data conversion products is also available.

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- output settling $< 30\mu s$
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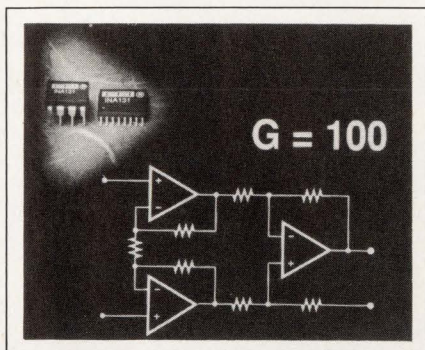


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EDN-NEW PRODUCTS

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tween the input ($\times 20$) and the output ($\times 5$) stages, which increases the bandwidth and improves the common-mode range. Laser-trimmed resistors provide a gain accuracy of 0.024%, a gain drift of 10 ppm/ $^{\circ}\text{C}$ (max), a voltage offset of 50 μV , and a voltage drift of 0.25 $\mu\text{V}/^{\circ}\text{C}$ (max) \$3.25 (1000). **Burr-Brown Corp.**, Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; (602) 746-1111. FAX (602) 889-1510. **Circle No. 418**

10.5-nsec cache RAM. The IDT-71B589 is BiCMOS cache RAM for 50-MHz i486 and 67-MHz Intel P5 systems. The chip has a 32k \times 9-bit organization and features a 10.5-nsec clock-to-data access time, which permits zero-wait-state operations. The chip integrates self-timed write operation and has an on-chip burst counter to ease timing issues. In addition, the chip has a 0.5-nsec address setup time and a 5-nsec output enable time. \$54.90 (1000). **Integrated Device Technology Inc.**, 3236 Scott Blvd, Box 58015, Santa Clara, CA 95052. Phone (408) 727-6116. FAX (408) 492-8674. **Circle No. 419**

High-voltage switch-mode ICs. The HV9100, HV9101, and HV9102 are BiCMOS switch-mode power-supply ICs. The chips feature clock speeds as fast as 1 MHz. The HV9100 and HV9101 accept input voltages from 10 to 70V dc, and their output switch has a 150V and 5 Ω rating. The HV9102 accepts input voltages from 10 to 120V dc, and its output switch has a 200V and 7 Ω rating. \$3.15 to \$3.58 (1000). **Supertex Inc.**, 1350 Bordeaux Dr, Sunnyvale, CA 94089. Phone (408) 744-0100. FAX (408) 734-5247. **Circle No. 420**

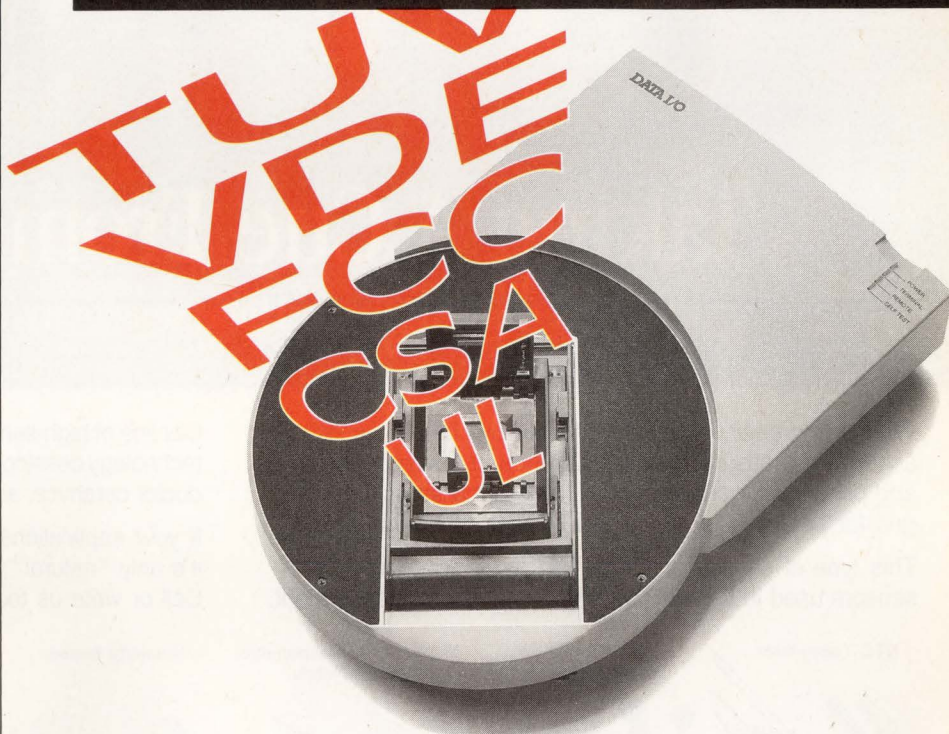
Data-acquisition system. The MN7450 and MN7451 are self-calibrating data-acquisition systems. They have an 8-channel input multiplexer, software-programmable gain amplifier, and

a 16-bit A/D converter that samples as fast as 47 kHz. The MN7450 has 0 to 5V or $\pm 5\text{V}$ input ranges, and the MN7451 has 0 to 10V or $\pm 10\text{V}$. \$350 (100). **Micro Networks**, 324 Clark St, Worcester, MA 01606. Phone (508) 852-5400. FAX (508) 853-8296. **Circle No. 421**

Military telecomm devices. The 145152-2 is a PLL frequency synthesizer. The chip features a reference os-

cillator, a 10-bit programmable divide-by-N counter, and a 6-bit programmable divide-by-A counter. You program the counters via a 12-bit parallel port. The 145406 chip combines three drivers and three receivers for EIA-232 and V.28 communications. Both chips meet MIL-STD-883 specifications. 145152-2, \$34.45; 145406, \$15.65. **Motorola Inc.**, EL376, 2100 E Elliot Rd, Tempe, AZ 85284. Phone (602) 897-3782. FAX (602) 897-4034. **Circle No. 422**

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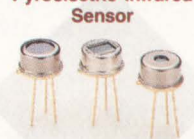
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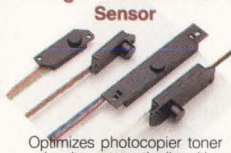
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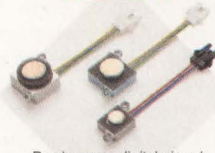
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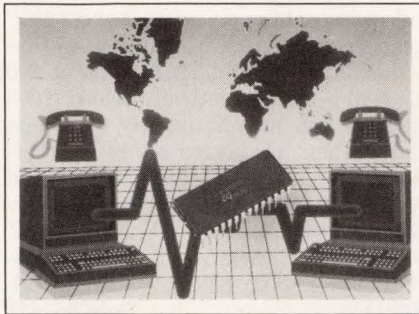


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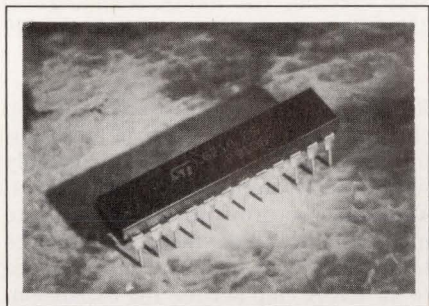


a conventional dynamic-RAM array and a serial-access memory array on a single chip. KM424C257, \$8.50; KM428C128, \$9.25 (100). **Samsung Semiconductor**, 3725 N First St, San Jose, CA 95134. Phone (800) 446-2760; (408) 954-7000.

Circle No. 426

High-power op amp. The OPA502 delivers 10A operating from ± 10 to $\pm 45V$ power supplies. The op amp has a 20-

Graphics coprocessor chip. The GUI Ultra accelerates graphical-user-interface (GUI) software such as Windows, OS/2, and X-Window software. The coprocessor comes as a chip set, which includes an IBM-compatible XGA RAMDAC and a clock generator or as a stand-alone unit. The chip interfaces with dynamic RAM and a 32-bit local bus; it produces 24-bit color for 800×600 pixels and 16-bit color for 1024×768 pixels. \$35 (1000). **Avance Logic Inc**, 4670 Fremont Blvd, Suite 105, Fremont, CA 94538. Phone (510) 226-9555. **Circle No. 424**



Stepper motor controller. The single-chip L6219 contains all of the circuitry to control and drive a 2-phase bipolar stepper motor. The chip contains two power bridge stages capable of supplying 750 mA. You can program the output current in four levels, which permits full- and half-step operations. An external D/A converter connected to the reference voltage input can micro-step the motor. \$2.60 (1000). **SGS-Thomson Microelectronics**, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. **Circle No. 425**

1-Mbit VRAMs. Two 1-Mbit video RAMs (VRAMs) have access times as fast as 60 nsec. The KM424C257 and KM428C128 VRAMs have $256k \times 4$ -bit and $128k \times 8$ -bit organizations, respectively. Both dual-port VRAMs offer flash-write, block-write, and split-register features. The VRAMs combine

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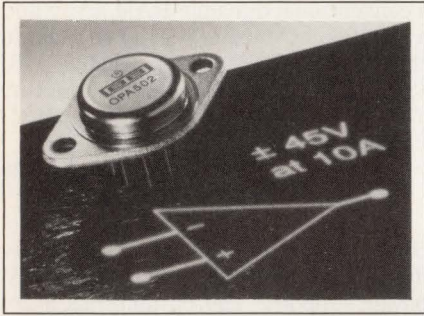
DATA I/O

CIRCLE NO. 132

EDN November 12, 1992 • 217

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mA quiescent supply current and a 10V/ μ sec slew rate. A FET input stage has a maximum input bias current of 200 pA. An 8-pin hermetically sealed TO-3 package can mount directly to a heat sink without insulating hardware. Versions operate from -40°C to $+85^{\circ}\text{C}$ and -55°C to $+125^{\circ}\text{C}$. \$37.95 (100). **Burr-Brown Corp.**, Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; (602) 746-1111. FAX (602) 889-1510. TWX 910-952-1111. **Circle No. 427**

Histogram IC. The HSP48410 generates a histogram of input gray levels. A 1024×24 -bit array accumulates 1024 gray levels having 10-bit resolution. The chip calculates the number of occurrences for each gray level. In addition, the chip can generate and store cumulative distribution functions for use in histogram equalization. The 33-MHz version, \$52.01; the 40-MHz version, \$59.81 (1000). **Harris Semiconductor Corp.**, Box 883, Melbourne, FL 32901. Phone (800) 442-7747, ext 1040; (407) 724-3704. **Circle No. 428**

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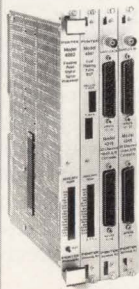
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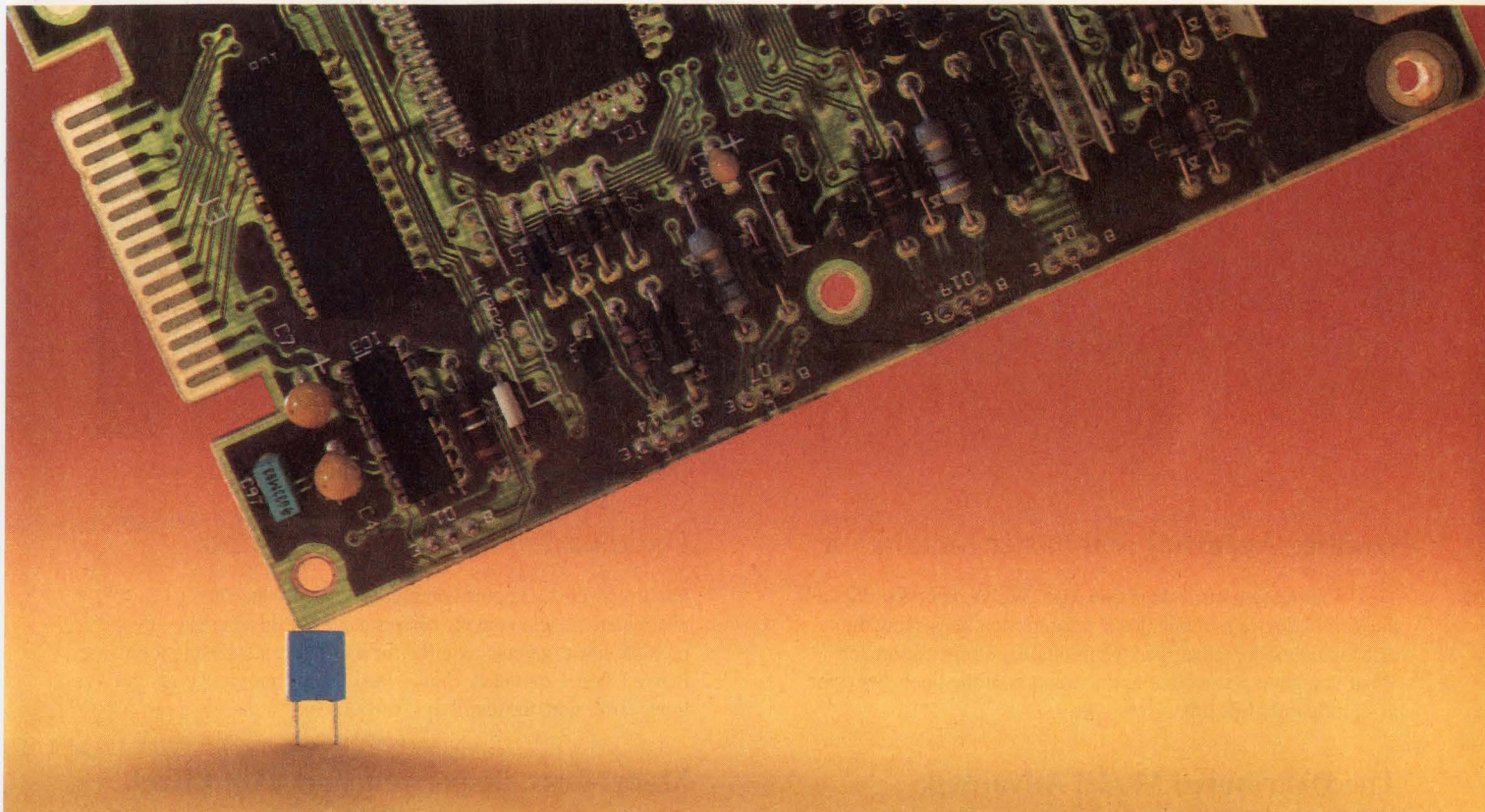


8-bit microcontroller. The TMP-68C711J6 has 16 kbytes of EPROM or OTPROM (one-time-programmable ROM). It operates as fast as 16.8 MHz, and its static design permits clock rates as low as dc. The chip contains 256 bytes of bootstrap ROM and 512 kbytes of static RAM. Other features include seven 54-bit I/O ports, a 16-bit timer, and a COP (computer-operating-properly) watchdog system. OTPROM version, \$25 (100). **Toshiba America Electronic Components Inc.**, 9775 Toledo Way, Irvine, CA 92718. Phone (714) 455-2000. **Circle No. 429**

R4000 peripheral chip set. A 3-chip chip set provides peripheral functions for a 50-MHz Mips R4000 μ P to comply with ARCSys 100 specifications. The chip set provides an interface to main memory and video, an interface to an i386 local bus, and an interface to an EISA chip set for I/O expansion. The set consists of two data-path chips, the TC85R4220F, and an address controller, the TC85R4230F. Chip set, \$250. **Toshiba America Electronic Components Inc.**, 9775 Toledo Way, Irvine, CA 92718. Phone (714) 455-2000. **Circle No. 430**

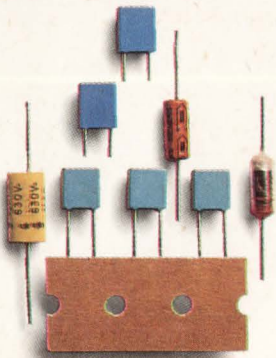
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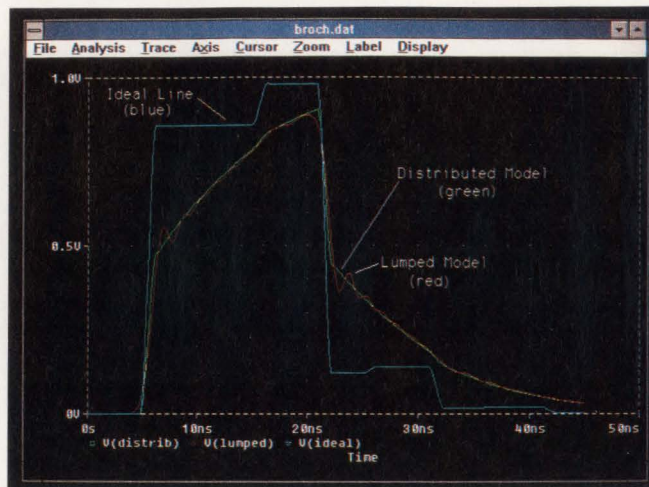
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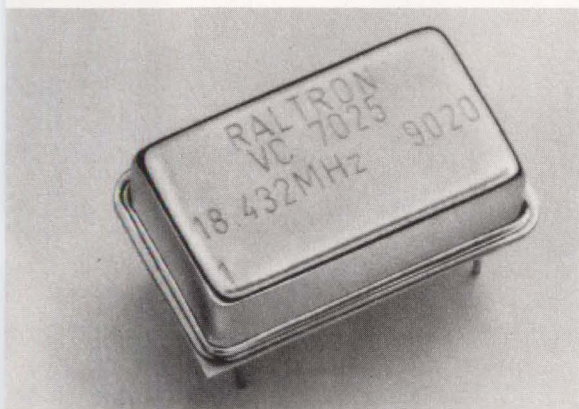
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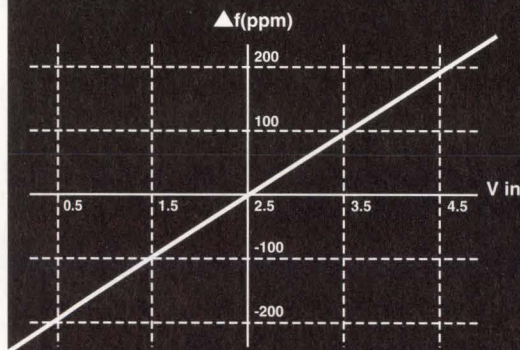
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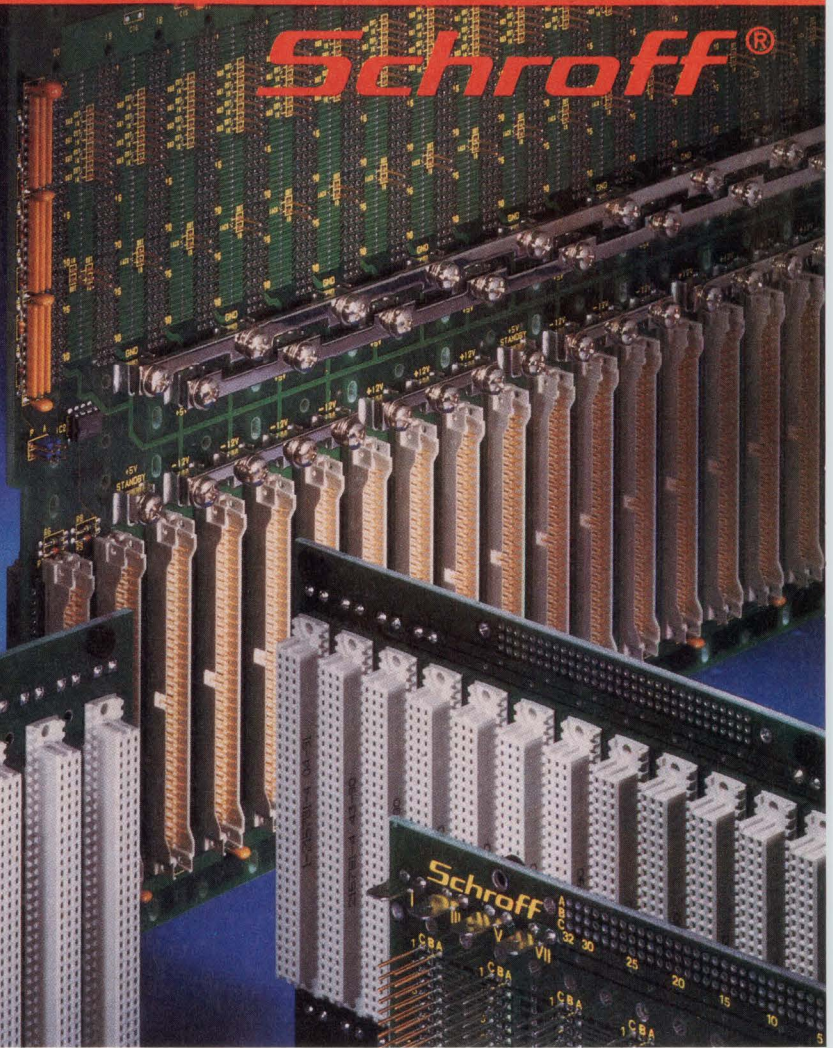


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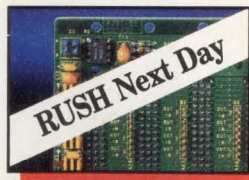
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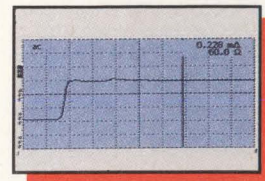
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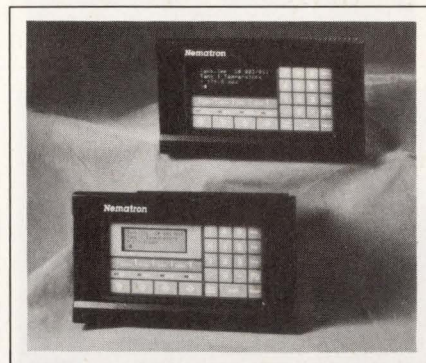
Computers & Peripherals

32-bit processor card. The ZT 8911 board operates at 32 bits across the STD 32 backplane. Its CPU module is replaceable, thus accommodating processor options. The board can serve in a single-processor system or as the primary processor in a multiprocessing system. \$3350. **Ziatech Corp**, 3433 Roberto Ct, San Luis Obispo, CA 93401. Phone (805) 541-0488. FAX (805) 541-5088. **Circle No. 432**

486-based PC/104 module. The Coremodule/486 puts a 25-MHz Cx-486SLC processor in a palm-sized PC/104 module. The stackable module contains all key functions of a full 486-based PC/AT. Special features include an on-board 1-Mbyte solid-state disk, a watchdog timer, and power-monitor functions. \$995 (100). **Ampro Computers Inc**, 990 Almanor Ave, Sunnyvale, CA 94086. Phone (408) 522-2100. FAX (408) 720-1305. **Circle No. 433**

DSP board for VME. The IXD7132 performs DSP operations on VME systems. Features include configurable in-

terrupts, multiple timers, board synchronization, and a master/slave VME interface that supports DMA and block transfers. The board calculates a 1024-point complex FFT in 0.77 msec. Less than \$5000 (OEM qty). **Ixthos Inc**, 12210 Plum Orchard Dr, Silver Spring, MD 20904. Phone (301) 572-6700. **Circle No. 434**



VME board for software engineers. The Aries VME board has dual 68030 processors to facilitate software development. Task segmentation between the processors simplifies programming.

The secondary processor can function either as an I/O processor or as a 32-bit DMA controller. \$2995 (1); \$2396 (100). **Omnibyte Corp**, 245 W Roosevelt Rd, West Chicago, IL 60185. Phone (708) 231-6880. FAX (708) 231-7042. **Circle No. 435**

PC bus board. The AVmux independently switches four video and four stereo audio inputs to one video and one audio output. You can use multiple cards to control more than four sources, and you can control audio levels to obtain fade-in/fade-out and similar effects. Vertical-interval switching is also user selectable, a feature that provides seamless cuts between video sources that are in sync. \$299. **New England Technology Group Inc**, 1 Kendall Square, Building 700, Cambridge, MA 02139. Phone (617) 494-1151. FAX (617) 494-0998. **Circle No. 436**

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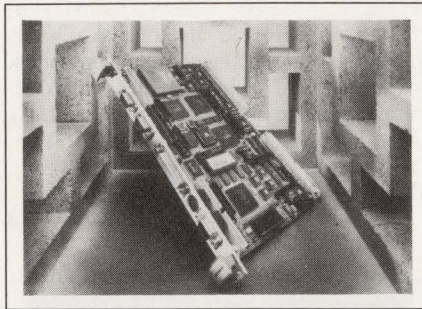
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tures Openboot firmware, which allows dynamic configuration of the computing environment and is in the process of being standardized by the IEEE. The board is available with as much as 64 Mbytes of dynamic RAM. \$7995 to \$12,490, depending on amount of memory. **Force Computers Inc.**, 3165 Winchester Blvd, Campbell, CA 95008. Phone in US and Canada, (800) 237-8863; (408) 370-6300; elsewhere, (49 89) 608140. FAX (408) 374-1146. **Circle No. 437**



486-based VME processor board. The VSCIM486, a 486-based PC/AT-compatible VME processor board, runs DOS, Unix, or any PC real-time operating system from ROM. In addition to a full VMEbus interface, the board includes ports to the SCIM mezzanine bus and STEbus. Its Peak-DM chip set from Chips & Technologies provides full compatibility with AT computers. From \$2900. **Arcom Control Systems Inc.**, 13510 S Oak St, Kansas City, MO 64145. Phone (816) 941-7025. FAX (816) 941-0343. **Circle No. 438**

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FDDI network adapter. The V/FDDI 5211 Peregrine-II network adapter for VME64 systems can be configured as a single- or dual-attached station for FDDI networks. The adapter is based on Motorola's 68EC040 and FDDI (Fiber Distributed-Data Interface) chip set. Transfers occur at rates as high as 50 Mbytes/sec. Dual-attached version, \$5995; single-attached version, \$4695; twisted-pair single attachment, \$4195. **Interphase Corp.**, 13800 Senlac, Dallas, TX 75234. Phone (214) 919-9000. FAX (214) 919-9200. **Circle No. 439**

Graphics controller. For X-Window and Microsoft Windows environments, the single-board, 1280 x 1024 x 8-pixel X8 controller turns ISA/EISA-bus-compatible personal computers into workstations. The unit places no demands on the host processor; it partitions tasks between the graphics controller and the host. The unit transfers images in 250 msec and draws 132,000 vectors/sec on the display. \$2995. **Microfield Graphics Inc.**, 9825 SW Sunshine Ct, Beaverton, OR 97005. Phone (800) 334-4922; (503) 626-9393. FAX (503) 641-9333. **Circle No. 440**

386 board for STD and PC/104 buses. The MCM-SX386 board offers both stand-alone operation or expansion with the STD bus or the PC/104 bus. It integrates basic AT peripherals and operates at clock speeds as high as 33 MHz. The board has space for an on-board 440-kbyte, bootable ROM disk. From \$850. **Winsystems**, 715 Stadium Dr, Suite 100, Arlington, TX 76011. Phone (817) 274-7553. FAX (817) 548-1358. **Circle No. 441**

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Siemens 80C517/537	16 MHz
Signetics/Philips 8XC451	16 MHz
Signetics/Philips 8XC550	16 MHz
Signetics/Philips 8XC552	16 MHz
Signetics/Philips 8XC562	16 MHz
Signetics/Philips 8XC652	16 MHz
Signetics/Philips 8XC751	16 MHz
Signetics/Philips 8XC851	16 MHz
AMD 80C321	16 MHz
AMD 80C325/525	16 MHz
Oki/Matra 8XC154	16MHz

Intel 8085 10MHz

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80C194/198	12 MHz
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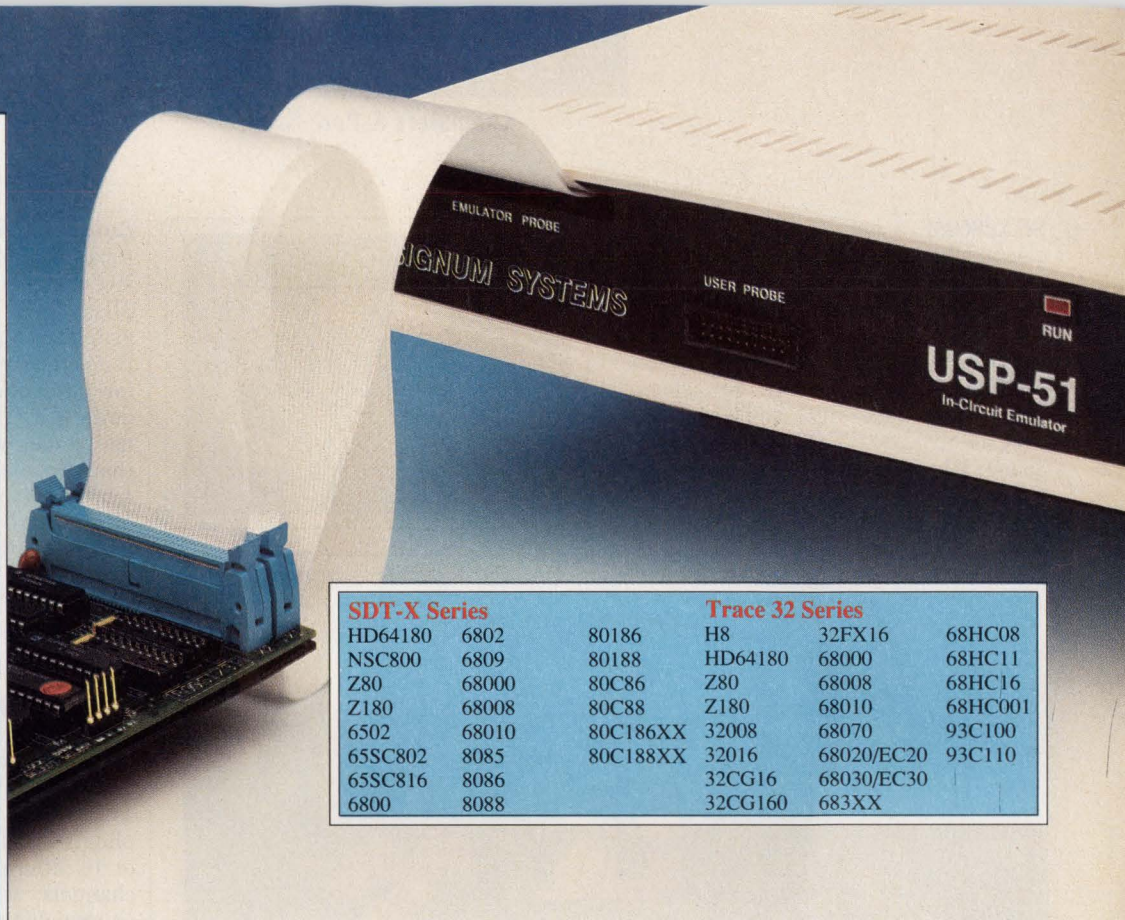
HPC Series	40 MHz
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Zilog Z8

Z8	20 MHz
Z86C95 (DSP)	24 MHz

Texas Instruments DSP's

320C10/15	33 MHz
320C16	35 MHz
320C17	20 MHz



SDT-X Series

HD64180	6802
NSC800	6809
Z80	68000
Z180	68008
6502	68010
65SC802	8085
65SC816	8086
6800	8088

Trace 32 Series

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80188	HD64180	68000	68HC11
80C86	Z80	68008	68HC16
80C88	Z180	68010	68HC001
80C186XX	32008	68070	93C100
80C188XX	32016	68020/EC20	93C110
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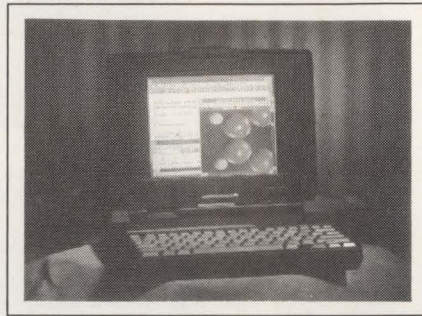
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SFX2800M, a non-Tempest version, is also available. Both tabletop models can communicate synchronously or asynchronously over a variety of data lines. The 2800M works with Group 2 and 3 CCITT standard protocols. Both models are plug compatible with government secure telephone units and encryption devices. SFX2800TE, \$8400; SFX2800M, \$5500. **Ricoh Corp.**, 5 Dedrick Pl, West Caldwell, NJ 07006. Phone (201) 882-2000. FAX (201) 882-2506. **Circle No. 442**



Color notebook computer. The Comtura 3/25c features a bright, 9-in. passive-matrix color VGA display and a 25-MHz 386SL processor. A proprietary graphics chip and software drivers help the computer deliver high performance for notebook computers running Windows 3.1. The computer weighs 6.7 lb and comes with a NiMH battery pack that provides 3 hours of operation on a 1-hour charge. Model 84/w with 84-Mbyte hard disk, \$2799; model 120/w with 120-Mbyte disk, \$3099. **Compaq Computer Corp.**, Box 692000, Houston, TX 77269. Phone (713) 370-0670.

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Military VME analog-input board.

The AIP-1 analog-input module features software-programmable gain, 1-channel conversion frequency as high as 50 kHz, and a programmable sampling rate. It provides 32 single-ended or 16 differential analog-input interface channels, with user-selectable bipolar or unipolar ranges. \$2955. Delivery, 30 to 45 days ARO. **Radstone Technology Corp.**, 20 Craig Rd, Montvale, NJ 07645. Phone (800) 368-2738; (201) 391-2700. FAX (201) 391-2899.

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The Designjet 600 offers three output quality levels—enhanced (addressable 600 dpi), final (300 dpi) and draft (addressable 300 dpi). Six interface cards provide a variety of connectivity options. In final mode, an E-size paper drawing takes less than 6 minutes. In enhanced mode, print time for the same size drawing is 12 minutes max. \$8495 and \$9995 for D- and E-size models, respectively. **Hewlett-Packard Co.**, Box 58059, MS511L-SJ, Santa Clara, CA 95051. Phone (800) 752-0900 or local sales office.

Circle No. 445

TV display for VGA.

The Model 721 Videomate allows any VGA-equipped computer to display standard TV programs without any software and without opening the computer. TV signals (from antenna, cable, VCR, or other source) and a PC's monitor signals go into the stand-alone unit; the PC can control, via another connection, whether the unit sends PC display output or TV to the computer's monitor. You can switch back and forth by pushing a button. \$325. **Telebyte Technology Inc.**, 270 E Pulaski Rd, Greenlawn, NY 11740. Phone (800) 535-3298; (516) 423-3232. FAX (516) 385-8184.

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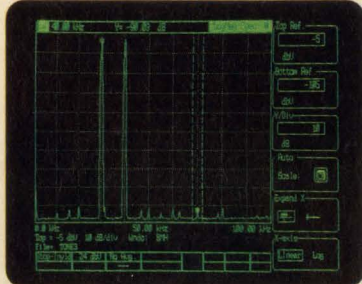
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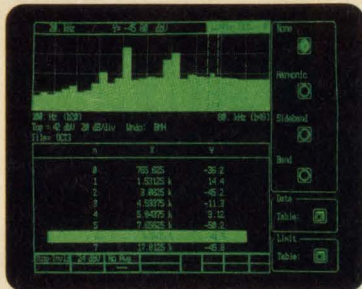
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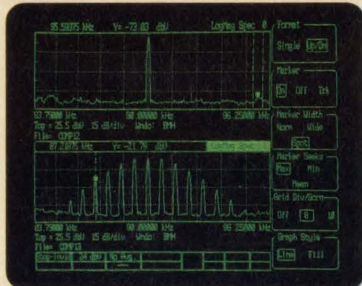
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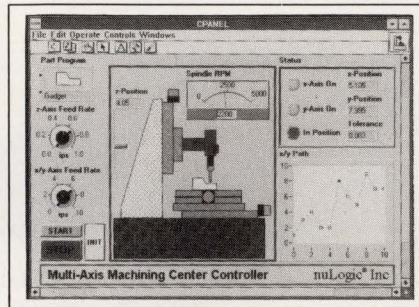
24 to 96-channel digital-I/O boards for 16-bit ISA bus. The PDIO-24, -48, -72, and -96 (priced at \$120, \$130, \$145, and \$160) let you mix input and output functions. The cards use 82C55A ICs, which operate in three I/O modes: basic, strobed, and bidirectional with handshaking. You configure the ports by writing to the boards' control registers; you transfer data using programmed I/O. The boards power up with all ports in a benign 0V state. **Analogic Corp.**, 8 Centennial Dr, Peabody, MA 01961. Phone (508) 977-3000. FAX (508) 532-6097. TLX 681-7144. **Circle No. 447**

Benchtop high-voltage ac/dc connection tester. The W 453 tests backplanes and cables for dielectric breakdown and continuity. You can choose breakdown test voltages as high as 1500V dc or 1000V ac and thresholds as high as 1 G Ω . Continuity-test current can be as high as 2A. The system tests as many as 2048 points and handles assemblies that include resistors, capacitors, diodes, and zeners. Guarding isolates parallel resistances, and Kelvin connections let you measure low resis-

tances. The system, which includes an MS-DOS PC, can generate its own programs from a known-good unit. It stores the programs on an 80-Mbyte hard disk or on a network file server. From \$40,000. **Weetech Inc.**, 1 Merchant St, Sharon, MA 02067. Phone (617) 784-1208. FAX (617) 784-1281.

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MS-Windows-based motion-control software. Motion Control Virtual Instruments (\$395) is a library that



works with National Instruments' new LabView for Windows package and with the vendor's PCStep 3-axis mo-

tion-control board (\$1095; \$1395 closed-loop). Included in the library are facilities for starting, stopping, and controlling position, velocity, and trajectory. **Nulogic Inc.**, 475 Hillside Ave, Needham, MA 02194. Phone (617) 444-7680. FAX (617) 444-2803. **Circle No. 449**

In-circuit emulators for H8/300 and H8/500 processor families. The Mime-700, hosted by an MS-DOS PC, provides real-time emulation at full clock speed for five processors in each of the two families. The in-circuit emulator supports target systems having as much as 16 Mbytes of memory; the resolution of memory overlays is 512 bytes. The unit provides a 32k x 128-bit trace buffer and an unlimited number of hardware breakpoints, including an execution-mode breakpoint. The emulator is compatible with several high-level-language compilers and debuggers. \$14,159; personality cards for specific processors, \$6230. Rental units are available. **Pentica Systems Inc.**, 19A Crosby Dr, Bedford, MA 01730. Phone (617) 275-4419. FAX (617) 275-6514.

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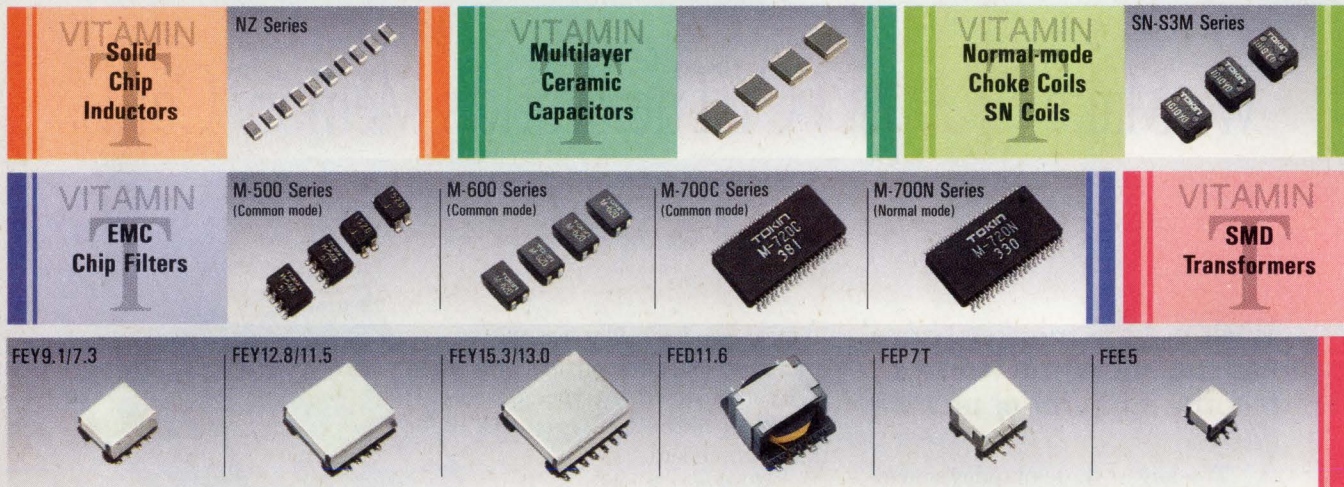


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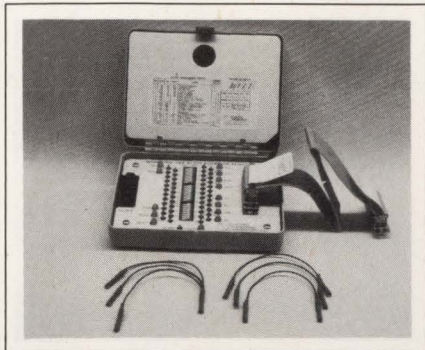
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\$995 3.1-MHz function synthesizer. The DS335 produces sine and square waves from 1 μ Hz to 3.1 MHz, ramp and triangular waves from 1 μ Hz to 10 kHz, and white noise from dc to 3.5 MHz. The unit's frequency resolution is 1 μ Hz. Sine-wave outputs' spurious responses are -65 dBc to 1 MHz; harmonic distortion is -70 dBc to 20 kHz. Square waves have a 15-nsec rise time (± 5 nsec) and <2% overshoot. The generators provide frequency-shift-keyed and swept outputs. Linear sweeps can cover the full frequency range; log sweeps can cover six decades. The time-base is accurate to 5 ppm from 20 to 30°C and ages at a rate of 5 ppm/year. **Stanford Research Systems**, 1290D Reamwood Ave, Sunnyvale, CA 94089. Phone (408) 744-9040. FAX (408) 744-9049. TLX 706891. **Circle No. 452**

Adapterless gang/set IC programmer. Without using adapters, the Multi-TRK-2000 Multiprogrammer programs devices in DIP, SIMM (single-in-line memory module), and surface-mount packages. It can program 16 μ Cs (microcontrollers) simultaneously. The programmer, which includes a keypad and an LCD to allow stand-alone operation and a floppy-disk drive for the device library, accommodates two TRKceels, each of which accepts eight devices. There are TRKceels for a variety of

packages. \$1995, not including cost of TRKceels. **Bytek Corp**, 543 NW 77th St, Boca Raton, FL 33487. Phone (407) 994-3520. FAX (407) 994-3615. **Circle No. 453**

Zero-wait-state in-circuit emulator for i486/486SX. The Mice-V-486 in-circuit emulator (ICE) uses SRAMs and high-speed buffers to support these processors at 33 MHz with no wait states in burst or nonburst modes. The

small probe size and the flexible cable connecting the probe to the pod permit using the emulator in tight spaces. In addition, the probe draws only 50 mA more from the target than the standard i486 does. The ICEs provide 1 Mbyte of overlay RAM and an 8k-frame trace buffer. \$29,500 (25 MHz); \$32,000 (33 MHz). **Microtek International**, 3300 NW 211th Terrace, Hillsboro, OR 97124. Phone (503) 645-7333. FAX (503) 629-8460. **Circle No. 454**

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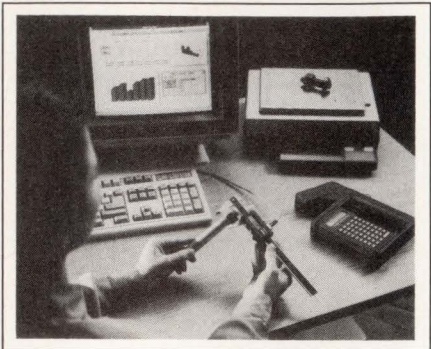
CIRCLE NO. 146

Die bonders. Series 6495 includes units for flip-chip bonding using silver-glass, thermoplastic, or epoxy die attachment processes on multichip modules, flexible or rigid pc boards, and very large hybrid substrates. The units accommodate dice that range in size from 250- μ m square to 1-in. square and substrates as large as 12-in. square. Dice can be selected from wafer packs, mounted wafers (to 8-in. diameter), or chip trays. A multicamera pattern-

recognition system is optional. \$49,550 to \$62,000. Delivery, 8 to 10 weeks ARO. **Kulicke and Soffa Industries Inc.**, 2101 Blair Mill Rd, Willow Grove, PA 19090. Phone (215) 784-6000. FAX (215) 659-7588. TLX 83-4268.

Circle No. 455

Software driver for RS-232C data-acquisition devices. Software Wedge feeds information entering a PC via its



RS-232C port into MS-DOS- and MS-Windows-based applications (spreadsheets and database managers, for example) as if you were typing it in yourself. Among the software's features are full bidirectional-communications support, date- and time-stamping, data parsing and filtering, and insertion of multiple-keystroke macros. DOS version, \$129; Windows version, \$199. **TAL Enterprises**, 2022 Wallace St, Philadelphia, PA 19130. Phone (800) 722-6004; (215) 763-2620. FAX (215) 763-9711.

Circle No. 456

Arbitrary-waveform generators with graphics interface. There are two generators in the 2000 Series: the \$7995 AFG2020 and the \$11,995 AWG2020. Both units use direct-digital function synthesis, reconstructing signals at a maximum rate of 250M-samples/sec with 12-bit resolution. The less expensive unit permits 1024-point waveform definitions and includes modulation and sweep-generation facilities. It also produces waveform sequences and multiple waveforms. The more expensive unit includes 1.8 Mbytes of memory and can store waveform definitions 256k-points long. This unit also accommodates a \$1000 DSP option that lets you define waveforms in either the frequency or the time domain. Delivery, six to eight weeks ARO. **Tektronix Inc**, Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200.

Circle No. 457

Arbitrary-waveform generators. The AWG5102 (\$3495), AFG5102 (\$3995), AWG5502 (\$4295), AFG5502 (\$4795), and AWG5105 (\$5995) are arbitrary waveform and function generators that produce fixed-frequency, digitally synthesized waveforms with 12-bit resolution. Units whose model designations contain the letter F also include analog swept-frequency (sine/square/triangle) generators. Units whose model designations have 1 as the second digit are



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CIRCLE NO. 148

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EDN November 12, 1992 • 233

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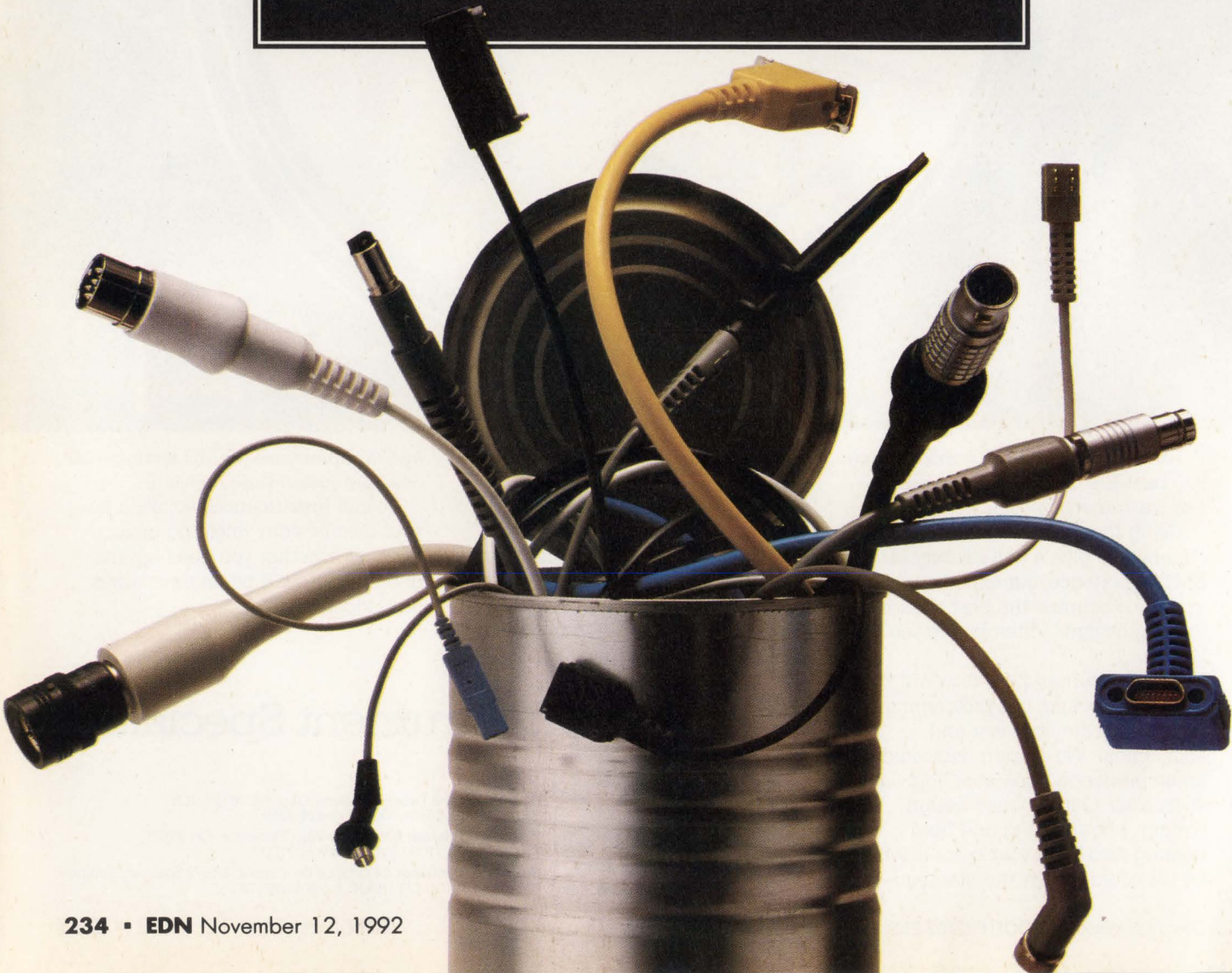


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CIRCLE NO. 149

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EDN-NEW PRODUCTS

Test & Measurement Instruments

plug-ins for the vendor's TM5000 modular-instrument system. Models whose designations contain 5 as the second digit are stand-alone units. The units whose model designations end in 2 operate to 20M samples/sec, conform to IEEE-488.1, and include a single channel with a 32k-point memory; the one whose model number ends in 5 operates to 50M-samples/sec, conforms to IEEE-488.2, and has two channels with 64k-point/channel memories. **Tektronix Inc**, Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200. **Circle No. 458**



ules directly accept frequency, resistance, dc and ac voltages, and thermocouple signals. The unit also has 12 digital I/O lines and a totalizer. \$3200 with 256-kbyte (~50,000 readings) memory card. **John Fluke Mfg Co Inc**, Box 9090, Everett, WA 98206. Phone (800) 443-5853. **Circle No. 461**

Philips Test and Measurement, Building TQIII-4, 5600MD Eindhoven, the Netherlands. Phone local office. **Circle No. 462**

Automated IC programmer. The Autosite Automated Programmer works with Exatron Corp's automated device handling systems. It accommodates ICs in DIP and PLCC packages having 20 to 84 pins. The programmer, a stand-alone unit with 2 Mbytes of RAM, programs memory and logic devices and microcontrollers. Device with 44 pins, \$11,840; device with 84 pins, \$16,840. **Data I/O Corp**, Box 97046, Redmond, WA 98073. Phone (800) 332-8246; (206) 881-6444. FAX (206) 881-6856. **Circle No. 459**

16-bit measurement module for semiconductor parameter test systems. The \$7500 DMM-16 works in the vendor's systems, operating as a differential voltmeter or as a driven current meter and increasing the sensitivity to 4 μ V and 2 pA. Because of its 140-dB CMRR, the unit introduces only 10 μ V of error with a common-mode voltage of 100V. The module also monitors high-transconductance transistors without oscillation. You can plug in the unit in place of an earlier 12-bit module; no modifications are necessary. **Reedholm Instruments Co**, 47810 Westinghouse Dr, Fremont, CA 94539. Phone (510) 490-5666. **Circle No. 460**

Portable data logger with removable, nonvolatile memory cards. The vendor calls the 20-channel 2635A a Data Bucket to denote that you can take it to a remote site, set it up to acquire data unattended, have it store as many as 400,000 readings on a plug-in credit-card-size memory card, retrieve the card for off-site data analysis, and leave the unit to acquire more data. Power can come from a 50- or 60-Hz ac line (90 to 264V) or from a dc source (9 to 16V). For locations that have communications lines, the logger includes a 38.4-kbps RS-232C port. Plug-in mod-

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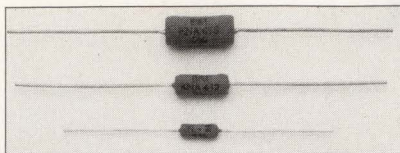
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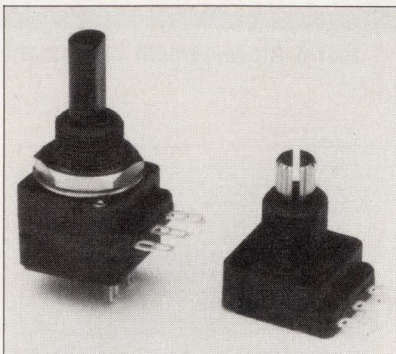
CIRCLE NO. 93



Wirewound Resistors

Silicone coated, all-welded construction, completely flameproof. Power ratings 3W to 15W over the ohmic range of 0R025 to 75K with a standard tolerance of 5%. Available in tape pack.

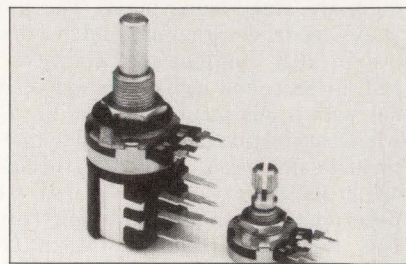
CIRCLE NO. 210



Modular Potentiometers

Completely insulated 16mm potentiometers are made of autoextinguishable plastic UL94 (VO). Modular design allows ganging up to 4 pots and a switch on the same metal or plastic shaft. Dust and solvent resistant.

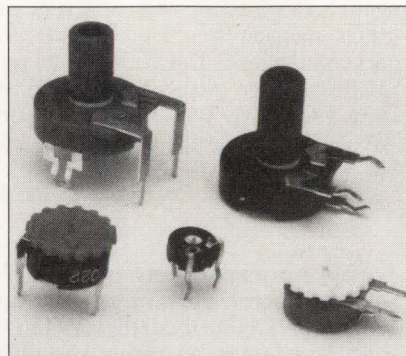
CIRCLE NO. 211



Control Potentiometers

Rotary control potentiometers available in 16mm and 21mm diameter versions. Both models are available with switches to satisfy virtually any design requirement.

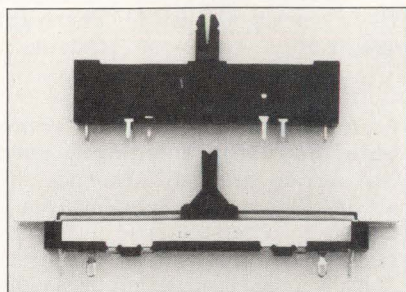
CIRCLE NO. 212



Trimmer Series

Our PT6 model is available in carbon. PT10 and PT15 models come in carbon and are also available in cermet. All trimmers are enclosed to protect against dust, cleaning solvents and water. Wide choice of mounting and adjustment options.

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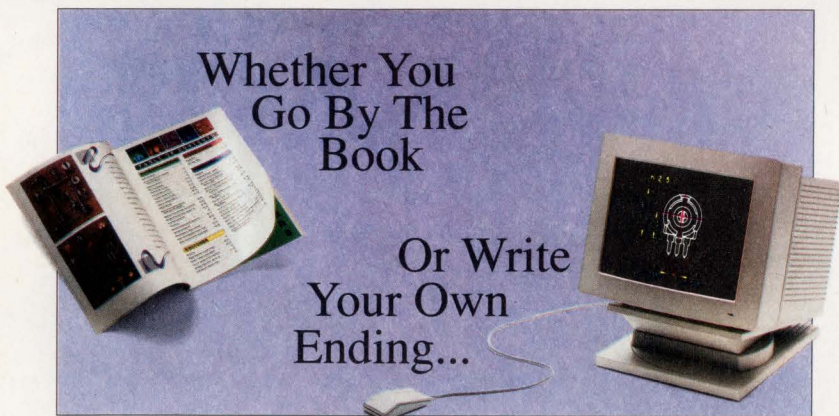
Slide Potentiometers

Featuring a linear adjustment, our slide potentiometers are available in 40mm and 60mm travels. Choose PC or panel mount in a variety of curves. Dust and solvent resistant.

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Or Write
Your Own
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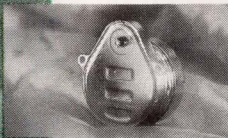
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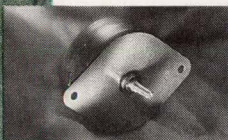


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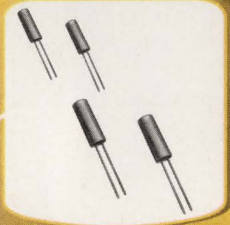
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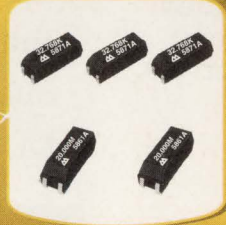
C-2

- LOW FREQUENCY TUNING FORK TYPE
- 32.768 KHz
- 20 KHz - 100 KHz

CA-301

- HIGH FREQUENCY AT - STRIP TYPE
- 4.0 MHz - 67.0 MHz

SMD



MC-405/6

- HEAT RESISTIVE C-2H INSIDE
- L10.4xW4.06xH3.56mm
- 20 KHz - 100 KHz

MA-505/6

- HEAT RESISTIVE CA-303 INSIDE
- L13.46xW5.08xH4.57mm
- 4.0 MHz - 67.0 MHz

MINIATURE SMD



MC-306

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- 32.768 KHz

MA-306

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- 17.7 MHz - 40.0 MHz

OSCILLATORS

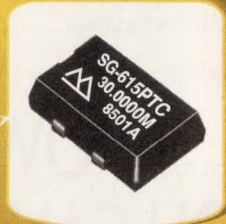
THRU-HOLE



SG-51/531

- COST EFFECTIVE AUTO INSERTABLE FULL SIZE (SG-51) AND HALF SIZE (SG-531) DIP'S
- CA-301 CRYSTAL INSIDE
- 1.025 MHz - 67.0 MHz

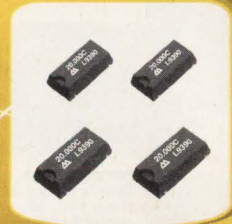
SMD



SG-615

- SURFACE MOUNTABLE
- HEAT RESISTIVE CA-303 INSIDE
- L14.0xW9.8xH4.7mm
- 1.025 MHz - 67.0 MHz

MINIATURE SMD



SG-636

- MINIATURE SURFACE MOUNT
- NEW AT - STRIP CRYSTAL TECHNOLOGY
- L10.3xW5.8xH2.8mm
- 2.20 MHz - 40.0 MHz

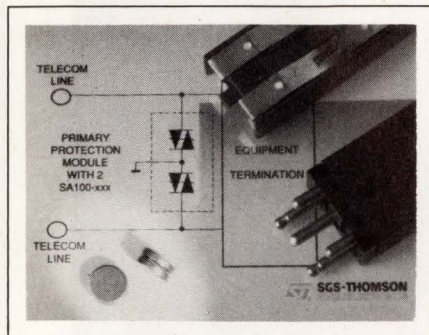
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Surge arresters. SA100 Series units provide crowbar protection with maximum surge currents as high as 100A. Key features include leakage current of 10 μ A max, breakover voltages of 350 or 400V max, and a maximum on-state voltage of 3.5V. Holding current equals 250 mA min. From \$0.92 (10,000). **SGS-Thomson Microelectronics**, 1000 E Bell Rd., Phoenix, AZ 85022. Phone (602) 867-6100. FAX (602) 867-6102. **Circle No. 562**

DIP switches. ESD Series devices are end stackable (as many as 12 packages), have standard pinouts on 0.1-in. centers, offer as many as 12 positions, and are available in red, blue, or black body colors. The surface-mount units are only 0.13 in. high. The spst contacts are rated for 25 mA at 24V dc switching; carry ratings are 100 mA at 50V dc. \$0.75 (10,000) for an 8-position unit. Delivery, eight weeks ARO. **Raltron Electronics Corp.**, 2315 NW 107th Ave., Miami, FL 33172. Phone (305) 593-6033. FAX (305) 594-3973. **Circle No. 563**

Electromechanical relays. LQ52 Series relays feature two Form C contacts and are housed in a 10-pin package that requires only 2 in.² of board space. Load ratings range to 1A, and lifetime measures 100 million operations. Input-power requirements range from 140 to 300 mW. Input voltage ratings of 3, 5, 6, 12, 24, and 48V dc are standard. Less

than \$2 (5000). Delivery, stock to eight weeks ARO. **CP Clare Corp.**, 3101 W Pratt Blvd., Chicago, IL 60645. Phone (312) 262-7700. FAX (312) 262-7819. **Circle No. 564**

Enclosures. The 8-24 Series VME enclosures feature a hinged top panel that contains the power supply in a swing-away assembly. The units can be configured with a removable I/O panel or with provisions for mounting as many as 12 Motorola-style transition boards. Available with as many as 21 slots, the units come with monolithic J1/J2 backplanes. Power supply ratings range to 750W. From \$2725. Delivery, four to six weeks ARO. **Hybricon Corp.**, 12 Willow Rd., Ayer, MA 01432. Phone (508) 772-5422. FAX (508) 772-2963. **Circle No. 565**

LED clusters. Series S600, B600, and DB600 15-mm LED clusters can replace standard incandescent bulbs. S600 units feature a screw-type base; the B and DB units are housed in bayonet-type bases. All are available in clusters of 9 to 40 LEDs in direct-mount, single- or double-contact, or double-contact index versions. From \$12.50 (1000). **LEDtronics Inc.**, 4009 Pacific Coast Hwy., Torrance, CA 90505. Phone (310) 549-9995. FAX (310) 549-4820. **Circle No. 566**

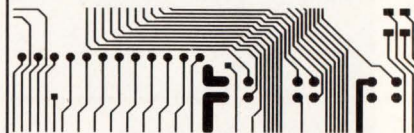
Resistors. LO Ω Series resistors are available in 3 and 5W packages that are compatible with automatic-insertion equipment. Both lines operate over a 25 to 200°C range and feature 11 standard resistance values ranging from 0.005 to 0.1 Ω . Tolerances go as low as 1%. Typical inductance is less than 0.02 μ H at 500 kHz. From \$0.34 (10,000). **IRC-Shallcross**, Box 1860, Boone, NC 28607. Phone (704) 264-8861. FAX (704) 262-1972. **Circle No. 567**

Connectors. Designed to terminate flat-ribbon cables, FM-6 connectors are available with as many as 40 positions. Impedance is either 60 or 75 Ω . Two plug designs allow stacking one above the other. \$14.50 (OEM qty). **Hirose Electric Inc.**, 2688 Westhills Ct., Simi Valley, CA 93065. Phone (805) 522-7958. FAX (805) 522-3217. **Circle No. 568**

Bar-graph display. The LL7164 Series 10-element bar-graph display is available with any combination of blank, red, green, and yellow LED



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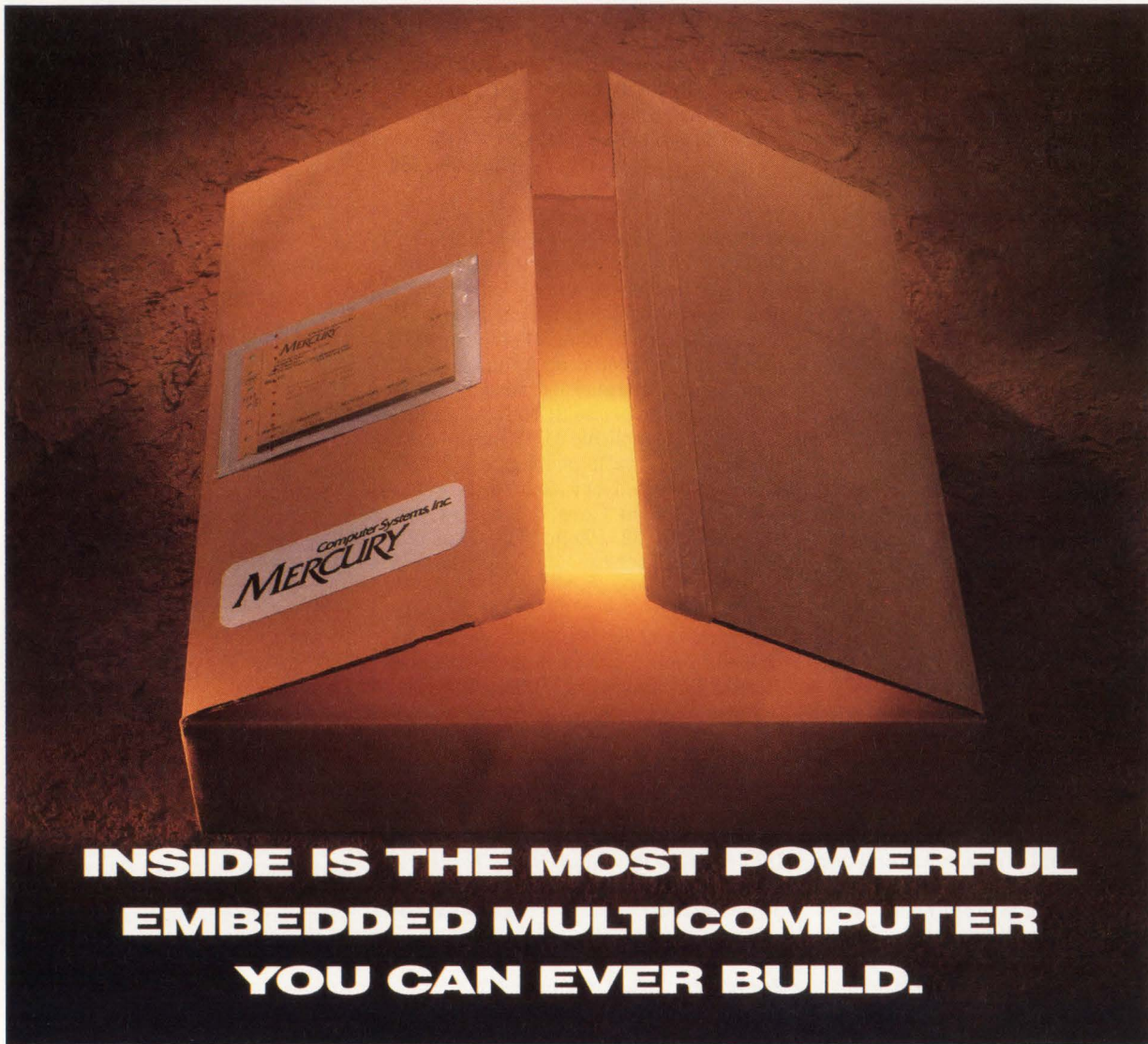
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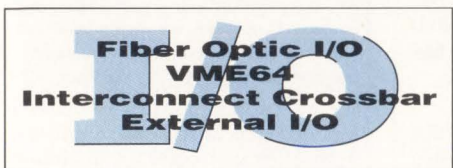
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CIRCLE NO. 155



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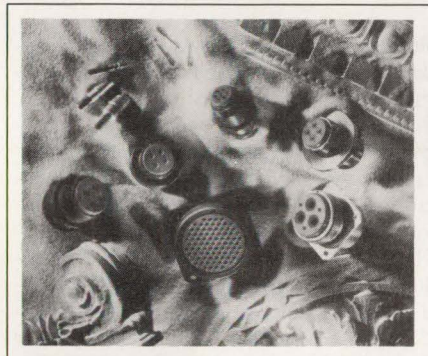
Components & Power Supplies

elements. The 20-pin unit fits standard 0.100×0.300-in. DIP layouts and may be socketed or wave soldered. \$1.85 (500). **IEE Inc**, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311, ext 418. FAX (818) 902-3723.

Circle No. 569

Power MOSFETs. The OM11N60 and OM11N55 are rated at 600V and 550V, respectively. $R_{DS(ON)}$ for both devices equals 0.42Ω. The devices come in a TO-254 hermetic isolated metal package in both side-tab and top-tab configurations. All devices are available in high-reliability screened versions. OM11N55AA, \$47.50 (100). **Omnirel Corp**, 205 Crawford St, Leominster, MA 01453. Phone (508) 534-5776. FAX (508) 537-4246.

Circle No. 570



Cylindrical connectors. CI Series connectors can accommodate both power and signal requirements. Offered in front- and rear-release styles, the line consists of 200 insert arrangements. The units are designed to meet the requirements of MIL-C-5015 and are offered in shell sizes 8 through 48. \$14 to \$120 (OEM qty). Delivery, 10 to 12 weeks ARO. **Cinch Connectors**, 1500 Morse Ave, Elk Grove Village, IL 60007. Phone (708) 981-6000.

Circle No. 571

Pressure sensors. SLP004D units offer differential and gauge pressure measurements of 0 to 4-in. water column full scale—approximately 0.15 psi. Operating from a 5V supply, the unit can develop a 50-mV full-scale output (FSO) with an accuracy (linearity and hysteresis) of 1% FSO max. The output voltage is ratiometric to the supply voltage, and the devices can operate with supply levels of 2 to 7.5V. \$29.75 (100). **Sensym Inc**, 1244 Reamwood Ave, Sunnyvale, CA 94089. Phone (800) 457-3679; (408) 744-1500.

Circle No. 572

DC/DC converter. The 4A5R3.3 converter has a 3.3V at 1A output with a ± 200 -mV output tolerance. It features I/O isolation and short-circuit protection. The unit is housed in a 1×2×0.375-in. package. \$24 (OEM qty). Delivery, six to eight weeks ARO. **Reliability Inc**, Box 218370, Houston, TX 77218. Phone (713) 492-0550. FAX (713) 492-0615.

Circle No. 573

Programmable supplies. The MST Series 200W supplies feature power-factor correction and meet IEC 555-2 specifications. Individual supplies are made up of a basic module that plugs into a rack enclosure holding as many as eight modules. Output ratings range from 0 to 6V at 20A to 0 to 150V at 1.2A. Individual modules can operate in an N+1 redundant mode. Module, \$1695; rack enclosure, \$895. Delivery, eight weeks ARO. **Keeco Inc**, 131-38 Sanford Ave, Flushing, NY 11352. Phone (718) 461-7000.

Circle No. 574

Chip adapter. The ANC-4044 adapter allows designers to test socketed 44-pin plastic-leaded-chip-carrier or PGA components. Numbered test points are provided for attachment of scope probe. Two LED status circuits on the adapter provide a visual indication for user-selected signals. \$122. **Antona Corp**, 1643½ Westwood Blvd, West Los Angeles, CA 90024. Phone (310) 473-8995. FAX (310) 473-7112.

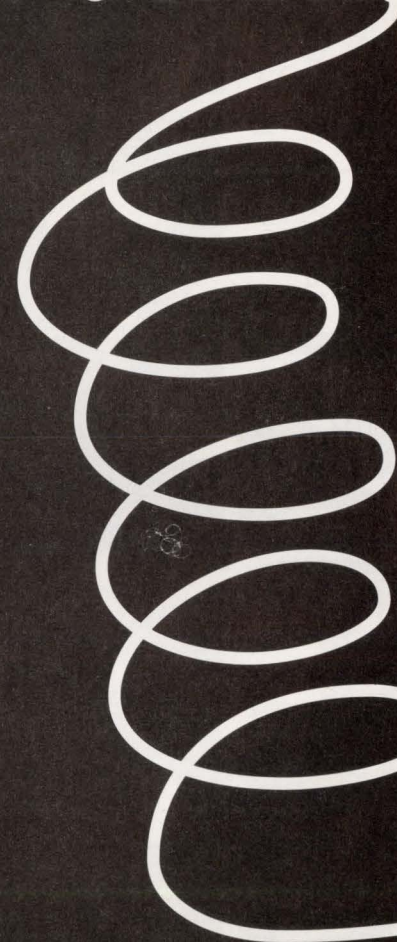
Circle No. 575

Surface-mount transformers. These dual devices are designed specifically for use in T1 and E1/CEPT high-speed digital telecomm interfaces operating at 1.544 or 2.048 Mbps. The units operate over a -40 to +85°C range. The devices are matched to the transceiver or line interface chips offered by eight leading manufacturers. The units are UL 1459 recognized and feature 1500V rms min isolation. \$4 (500). **Pulse Engineering**, 12220 World Trade Dr, San Diego, CA 92128. Phone (619) 674-8100. FAX (619) 674-8262.

Circle No. 576

DC/DC converters. The AB100S and AB200S 200W converters are designed to withstand the rigors of armored and ground mobile-system applications. They operate from inputs of 14 to 32V and develop outputs ranging from 5 to 28V. Operating range, with no derating, spans -55 to +100°C. Line and load regulation equals 0.1%, and effi-

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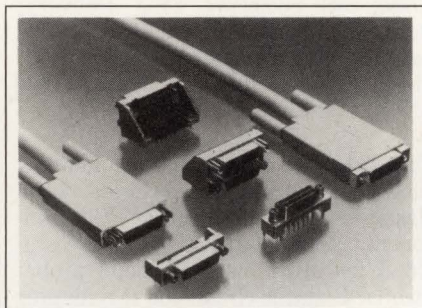
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EDN-NEW PRODUCTS

Components & Power Supplies

ciencies are in the 70 to 80% range. 100W version, from \$1775; 200W version, from \$2350. **Abbott Electronics Inc.**, 2727 S La Cienega Blvd, Los Angeles, CA 90034. Phone (213) 202-8820. FAX (213) 836-1027. **Circle No. 577**

Keyboard. The FTF keyboard features a built-in mouse and is housed in a waterproof and dustproof enclosure that meets the IP 65 rating. The keyboard is also available unboxed for custom applications. The unit features color-coded function keys and tactile feedback. The English-language version is standard, but optional foreign-language layouts are available. **Preh Electronic Industries Inc.**, 470 E Main St, Lake Zurich, IL 60047. Phone (708) 438-4000. **Circle No. 578**



Cable connectors. The Amplimite .050 Series of shielded 26-position connectors includes right-angle and stacked right-angle headers, a through-hole vertical pc-board receptacle, and a mating-cable plug connector that is preloaded with insulation displacement contacts. Housings and covers have a UL 94V-0 rating, and they are compatible with reflow solder processes. \$4 to \$10. **AMP Inc.**, Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752. **Circle No. 579**

Resistor network. The bused MNR-35 chip resistor network features eight resistive elements with two electrodes positioned in common on the network. The units are rated for 0.063W and are available with values of 0.1 to 100 k Ω . Maximum voltage rating varies with resistance values and ranges to 50V. \$0.12. Delivery, 10 weeks ARO. **Rohm Corp.**, 3034 Owen Dr, Antioch, TN 37013. Phone (615) 641-2020, ext 116. **Circle No. 580**

DC/DC converter. This 1W converter accepts a 5V input and develops a 12V regulated output. It features an enable function for programming and erasing

flash memories. The unit is TTL compatible and features short-circuit protection, 500V I/O isolation, and no derating to 71°C. The converter is available in SIP and DIP housings. \$8.50 (OEM qty). **Reliability Inc.**, Box 218370, Houston, TX 77218. Phone (713) 492-0550. FAX (713) 492-0615. **Circle No. 581**

Solid-state relay. The KD Series relay is housed in a hermetic package and features a power FET output with a rating of 5A at 60V dc. It is designed for use in MIL-STD-704 28V dc systems. The control circuit is optically isolated. Short-circuit and current-overload protection are available as options. \$94 (OEM qty). Delivery, stock to eight weeks ARO. **Teledyne Solid State**, 12525 Daphne Ave, Hawthorne, CA 90250. Phone (213) 777-0077. **Circle No. 582**

Display modules. Series 6800 LED display modules feature 1-in.-high characters in 1 \times 12 and 1 \times 20 formats. Available in red, green, yellow, or high-brightness red colors, the units are μ P controlled and have a bidirectional, 9600-baud, RS-232C serial interface. The on-board character generator provides ASCII, general European, Cyrillic, Katakana, and Hebrew character sets. 6800-01 1 \times 20 models, from \$233; 6800-02 1 \times 12 models, from \$165 (100). Delivery, four to six weeks ARO. **IEE Inc.**, 7740 Lemon Ave, Van Nuys, CA 91409. Phone (818) 787-0311, ext 418. **Circle No. 583**

Pressure monitor. The Infinity Pressure Standard is available with ranges of 15 to 6000 psig. The unit can be configured with outputs such as dual 4A Form C relays or BCD, analog output, RS-232C, or RS-485. Standard features include front-panel tare, peak and valley detection and memory, and 6-digit display for high resolution. From \$725. **Newport Electronics Inc.**, 2229 S Yale St, Santa Ana, CA 92704. Phone (800) 639-7678; (714) 540-4914. **Circle No. 584**

Quartz crystal. This initial version of the CX4 operates at 32.768 kHz and is designed for surface-mount applications. It has gold-flash or nickel tin-plated contact pads that are bumped for better termination. Standard frequency tolerances of ± 30 , ± 100 , and $\pm 10,000$ ppm are available. \$4.75 (10,000). Delivery, four to six weeks ARO. **Micro Crystal**, 702 W Algonquin Rd, Arlington Heights, IL 60005. Phone (708) 806-1485. **Circle No. 586**

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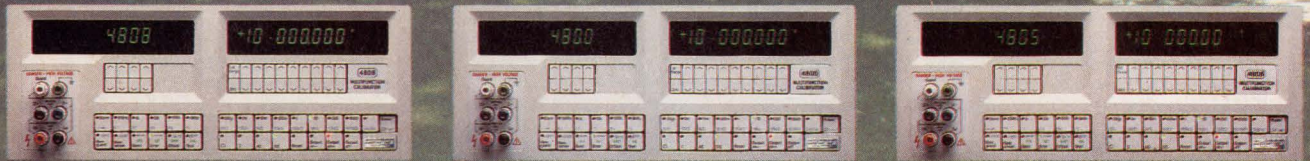
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Circle No. 159 For Literature

Circle No. 160 For Demo

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S T A N D I N G S

	W O N	L O S T	TOY PROGRAM		REAL PROGRAM					
			DHRYSTONES PER SEC.	% BEHIND	EXECUTION TIME SEC.	% BEHIND	CODE SIZE IN BYTES	% BEHIND	COMPILATION TIME MIN.	% BEHIND
SIERRA SYSTEMS	12	0	31604	—	5.73	—	284708	—	5.07	—
GNU	9	3	24390	30%	6.11	7%	298616	5%	17.12	238%
MICROTEC RESEARCH	7	5	23854	32%	6.49	13%	295466	4%	19.50	285%
OASYS/GREEN HILLS	6	6	28571	11%	7.80	36%	334632	18%	36.18	614%
INTERMETRICS	4	8	23234	36%	7.50	31%	314924	11%	17.11	238%
INTROL	4	8	19098	65%	7.03	23%	301524	6%	16.48	225%
SOFTWARE DEV. SYS.	0	12	16415	93%	9.47	65%	313360	10%	16.93	234%

68000 Compiler Benchmark Results.

Sierra Systems undefeated on the 68040. Two benchmarks were selected, Dhrystone 2.1 (the Toy program) and the Sierra Systems production C compiler (the Real program). The compiler was selected because both its size and complexity are representative of real-world applications.

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Won/Lost Record: For each benchmark, the compilers' run-time performances were compared to each other with wins and losses totalled in round-robin fashion. (See Dhrystones and Execution Time columns on scoreboard.)

Compilers: GNU 2.0, Intermetrics 8.0, Introl 3.06, Microtec Research 4.2d, Oasys/Green Hills 1.8.5Rc, Sierra Systems 3.0, Software Development Systems 5.1.

Hosts: 33 MHz 386 Zeos PC and Sun SPARCstation IPC. All compilers were run on the PC, except for GNU and Oasys/Green Hills, which were run on the Sun. Running the Sierra Systems compiler on both host systems allowed the Sun times to be scaled to PC time for the scoreboard.

Target: Motorola VME167, 25 MHz 68040 with caches enabled.

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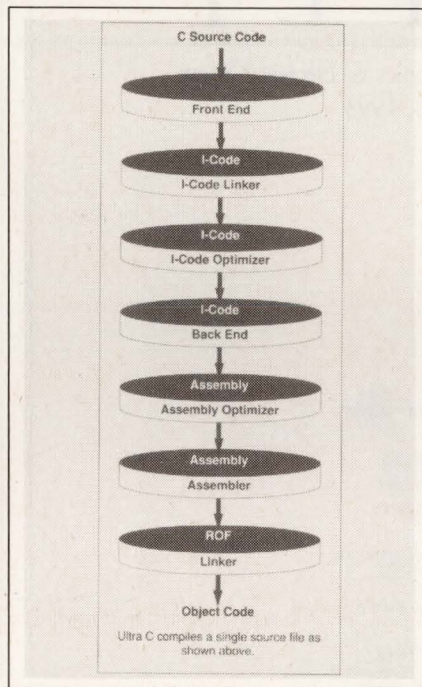
VHDL simulator for HP and IBM. In addition to Sun workstations and PCs, the V-System VHDL simulator runs on HP Series 700 and IBM RISC System/6000 workstations. The software gives full conformance to IEEE-1076 and interactive source-level debugging. A Structure View window also dynamically links seven other windows that give multiple views into a design, including a display of VHDL signals as waveforms. Floating license, \$9995. **Model Technology Inc.**, 15455 NW Greenbrier Pkwy, Suite 240, Beaverton, OR 97006. Phone (503) 690-6838. FAX (503) 690-2093. **Circle No. 544**

Re-engineering tools. Three reverse-engineering software environments (Tree4c, Tree4Fortran, and TreePascal) parse existing source code and display a program's structure chart. The tools also let you selectively reuse documentation, source code, test cases, and other data, as well as construct user-defined and filtered reuse libraries. The programs include tools for modeling, default editing, generation of makefiles, graphical viewpaths, configuration management, testing, problem report management, profiling, project communications, and report generation. For Sun workstations, \$1500 each. **+1 Software Engineering**, 2510-G Las Posas Rd, Suite 438, Camarillo, CA 93011. Phone (805) 389-1778. **Circle No. 545**

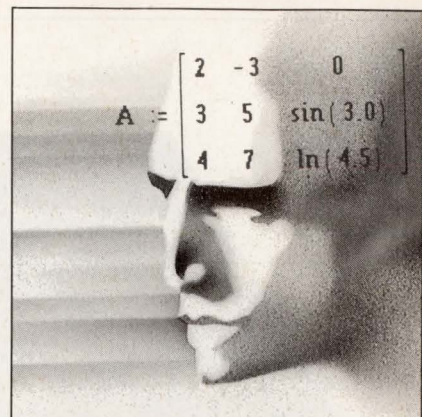
DOS scripting software. PC-Automate lets you create scripts that start programs, issue keystrokes, and perform operations when the computer is unattended. Once you create a script, you can execute it on request, from a menu, or at a scheduled time. When your needs go beyond keystroke recording and playback, you can use com-

mands for execution control, mathematics, file manipulation, string manipulation user input, retrieving date and time, screen access, and decision making. \$99. **Excellsoft Co.**, 1960 Eva Dr, Lansdale, PA 19446. Phone (215) 251-7097; (215) 699-4021. **Circle No. 546**

Cross-development tools for embedded systems. The Spectra development system includes the host-resident Target Manager and user-extensible ToolBuilder interface. The system uses the Xtrace protocol that allows multiple host-resident tools to communicate with a target system over a network or communications link. A multiuser debug model lets a work group coordinate its activities to share a number of targets. Sun/68000 versions, \$5000. **Ready Systems**, 470 Potrero Ave, Sunnyvale, CA 94086. Phone (408) 736-2600. FAX (408) 736-3400. **Circle No. 547**



C compiler for real-time systems. The Ultra C compiler includes all the I/O and systems calls for the maker's OS-9 and OS-9000 real-time operating systems and outputs machine code for Motorola 68xxx and Intel 80x86 processors. The compiler also optimizes code with your choice of maximum speed, minimum size, or a combination of the two, and it complies with the Plum Hall C Validation Suite and all ANSI requirements. The compiler will run on the target processor and any Motorola-



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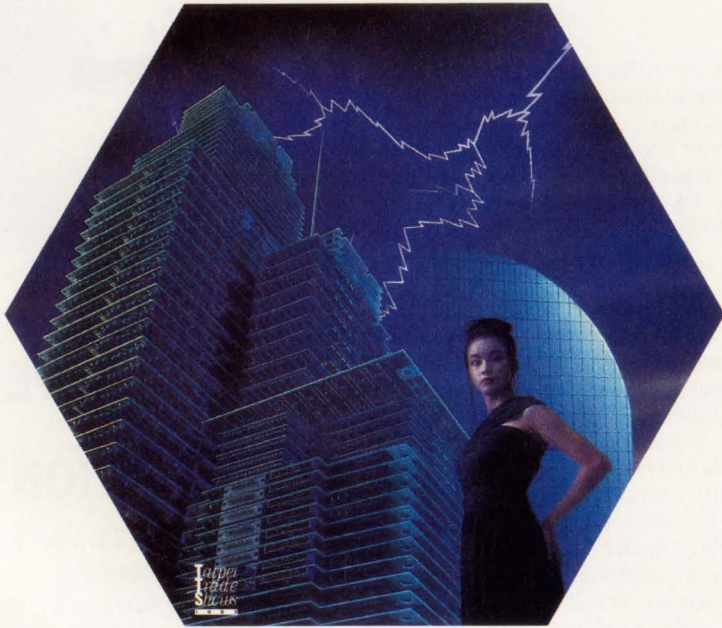
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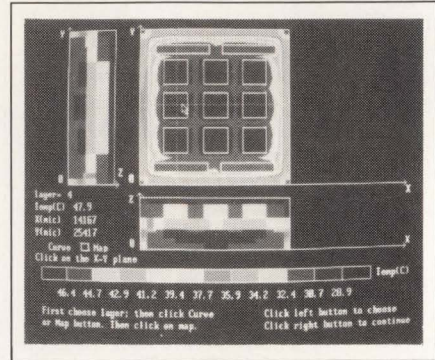
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or Intel-based personal computer or workstation. For 68000 systems, \$1250. **Microware Systems Corp**, 1900 NW 114th St, Des Moines, IA 50325. Phone (515) 224-1929. FAX (515) 224-1352.

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Thermal analysis software for components. Betasoft-C predicts thermal performance, evaluates thermal resistances and impedances, and provides packaging alternatives for components. Computation time for a typical MCM on a 16-MHz 386SX is approximately three minutes, and preparing a new component for analysis takes approximately 20 minutes (max) for a new user. Steady-state results appear in color graphics on three orthogonal planes at any point of interest. PC version, \$3995. **Dynamic Soft Analysis Inc**, 213 Guyasuta Rd, Pittsburgh, PA 15215. Phone (412) 781-3016. FAX (412) 781-3098.

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Real-time development tools for VME/Unix. VMEexec 2.2 standardizes network and system interfaces to a real-time kernel to allow reuse and porting of software between projects. This version adds a memory-management unit and Deltaguide, based on Motif, that facilitates creation of applications that represent data pictorially with dials, sliders, graphs, or other moving graphical shapes. \$5700. **Motorola Inc Computer Group**, 2900 S Diablo Way, Tempe, AZ 85282. Phone (408) 369-4480.

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2. Mail Subscriptions (Paid and/or Requested)	147,998	130,545
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D. Free distribution by mail, carrier, or other means samples, complimentary, and other free copies	2,088	2,163
E. Total Distribution (Sum of C & D)	150,086	132,708
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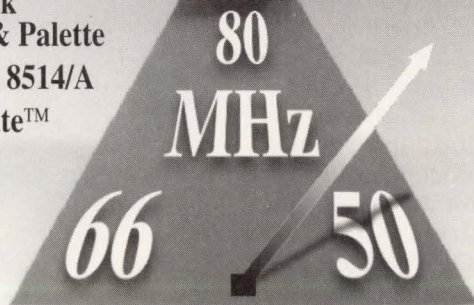
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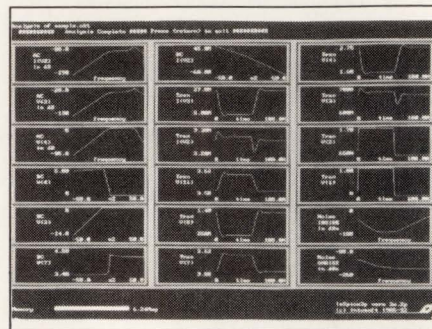
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Spice circuit simulator. IsSpice3 implements Berkeley Spice 3E.2 and performs ac, dc, transient, noise, distortion, Fourier, pole-zero, temperature, sensitivity, and mixed-mode analyses on circuits operating from dc through microwave frequencies. The program includes built-in models for a variety of passive and active components, additions to behavioral modeling capabilities, and an interactive user interface that displays waveforms as the simula-



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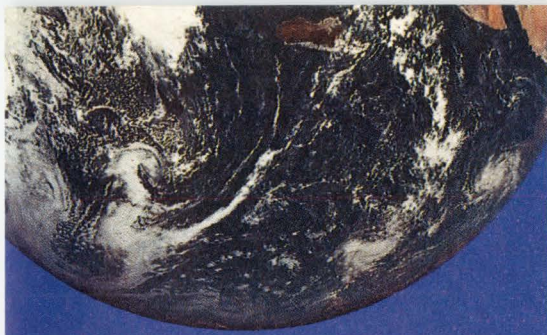
CIRCLE NO. 175

tion runs. The software gives input and output compatibility with Berkeley Spice 2G.6. \$695 **Intusoft**, 222 W Sixth St, Suite 1070, San Pedro, CA 90731. Phone (310) 833-0710. FAX (310) 833-9658. **Circle No. 552**

VHDL-source-code libraries. Source-model Libraries give you VHDL source code for 600 SSI parts and 1400 memory devices, including static RAMs, dynamic RAMs, PROMs, and EPROMs. The two libraries comply with IEEE-1076 and include error-checking and accurate timing behavior. The models include databook and other nonproprietary information, and they conform to a consistent format throughout the libraries. The libraries work with certain VHDL simulators from Mentor, Cadence, Viewlogic, Synopsys, Dazix, and Vantage. Site license for 20 or fewer users, \$18,000 for the Memory Library; \$12,000 for the SSI Library. **Logic Modeling Inc.**, 19500 NW Gibbs Dr, Beaverton, OR 97075. Phone (503) 690-6900. FAX (503) 690-6906. **Circle No. 553**

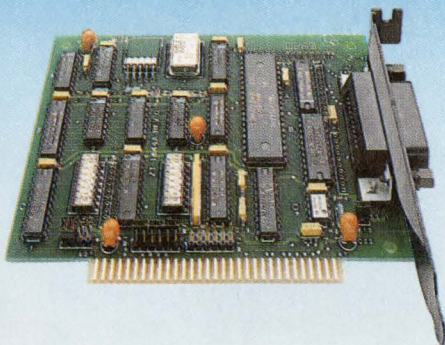
DSP development system. Hypersignal-Acoustic 3.31 is DSP development software for the acoustic/audio professional. Improvements with this release include additions to the real-time Spectrum Analyzer display: continuous display of the impulse response of the system under test, coherence function display, additional averaging methods, averaged phase delay, and output of waveforms on the DSP/acquisition-board D/A channels during operation to provide stimulus to the system under test. For DOS, \$1489. **Signalogic Inc.**, 9704 Skillman #111, Dallas, TX 75243. Phone (214) 343-0069. FAX (214) 343-0163. **Circle No. 554**

PC-based VHDL simulator. V-System/Windows 3.0 for the PC adds five windows for debugging of VHDL designs. The simulator complies with



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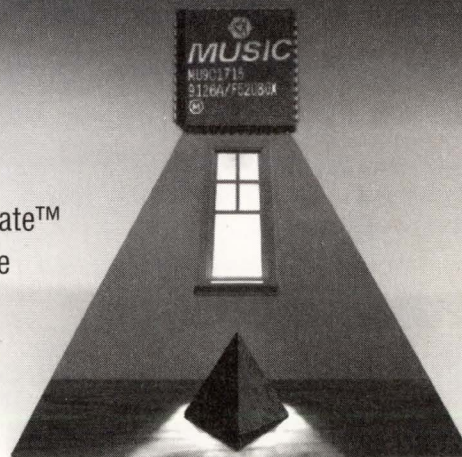
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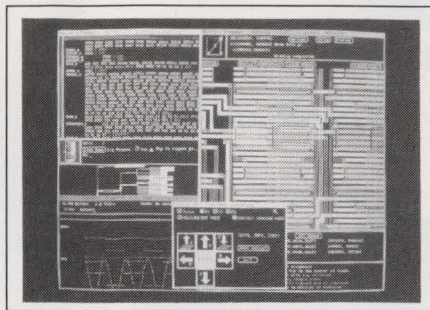


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IEEE-1076. The five windows include Structure View, Waveform Display, Signals, Variables, and Process. For MS-Windows 3.0 or 3.1, single copy, \$2495. Also available for DOS and Unix. **Model Technology Inc.**, 15455 NW Greenbrier Pkwy, Suite 240, Beaverton, OR 97006. Phone (503) 690-6838. FAX (503) 690-2093. **Circle No. 555**



System for silicon and CAE. Megalink/Megalab software and communications package connects post-silicon test and modification systems that work in Merlin's Framework. The system lets you find and work on a feature of interest; you can then pass its coordinates and other relevant data between instruments that perform tasks such as signal probing, circuit testing, visual, silicon modification by focused ion beam micromachining and microdeposition, hot-spot detection, communication, and documentation. The system requires Sun-3, Sun-4, or SPARCstation and network. \$85,000. **Knights Technology Inc.**, 3506 Bassett St, Santa Clara, CA 95054. Phone (408) 988-0600. FAX (408) 988-0663. **Circle No. 556**

Embedded DOS for STD32 bus and 80C186. The Embedded DOS Development System for the VL-186-1 80C186 CPU/SBC (single-board computer) is a real-time, multitasking operating system that is compatible with DOS 3.31 and runs on an STD32 bus target. The OS provides priority-based scheduling, round-robin scheduling, and non-preemptive scheduling, and it is fully re-entrant. You can access the kernel from C and assembly languages. The software boots from a ROM-disk and includes standard DOS hardware resources such as COM1, COM2, LPT1, and VGA. Software bundled with 16-MHz VL-186-1 CPU card, STD32 card cage with power supply, ZT-8980 VGA/keyboard card, \$2421. **Versallogic Corp.**, 3888 Stewart Rd, Eugene, OR 97402. Phone (800) 824-3163. FAX (503) 485-5712. **Circle No. 557**

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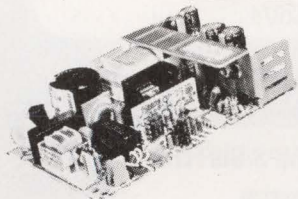


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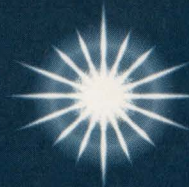
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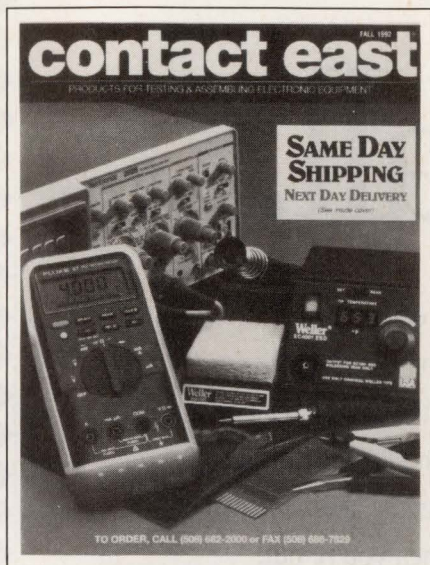
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Supplement of test equipment. This 48-pg supplement to the general catalog highlights test instruments and tools. It features products for testing, repairing, and assembling electronic equipment from brand-name manufacturers. The book covers programmable power supplies, spectrum analyzers, frequency counters, instrument carts, EPROM programmers, and ESD-safe ergonomic chairs. Other products include oscilloscopes, DMMs, ozone-safe cleaners, soldering/desoldering systems, state-protection products, tool kits, and workbenches. **Contact East Inc.**, 335 Willow St S, North Andover, MA 01845. Phone (508) 682-9844. FAX (508) 688-7829. **Circle No. 463**

Application note on convert pulses. AN7, *Modifying Start Convert Pulses Using Commercially Available Devices* explains various techniques for creating start convert pulses when using sampling ADCs. It reviews the impact of varying the width and repetition rate of the start convert pulse. The 4-pg note also explains how to create start convert pulses, using common D-type flip-flops on Series 123 multivibrators. Circuit diagrams, logic-function tables, and circuit descriptions help you in creating start convert pulses for data converters. **Datel Inc.**, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. FAX (508) 339-6356. **Circle No. 464**

Condensed catalog of fasteners. The *PEM Self-Clinching Fastener Guide* profiles a line of self-clinching and broaching fasteners. The guide gives an overview of fastener lines, including parts' designations, materials, and

thread sizes. It also describes the *Pem-serter* line of precision fastener-installation presses. **Penn Engineering & Manufacturing Corp.**, 5190 Old Easton Rd, Danboro, PA 18916. Phone (215) 766-8853. **Circle No. 465**

Catalog of hardware/software packages. This 60-pg catalog presents an expanded line of real-time PC-based hardware and software. It features AT/MCA CODAS (computer-based oscilloscope and data-acquisition system). The publication also features CODAS I/O modules, a software-development kit for ADSP-2101 DSP μ Ps, a 200 Series software-development kit for DOS and Windows, industrial-grade amplifiers, biomedical-grade amplifiers, and analysis software. **Dataq Instruments Inc.**, 150 Springside Dr, Suite B220, Akron, OH 44333. Phone (216) 668-1444. FAX (216) 666-5434. **Circle No. 466**

Threaded inserts cataloged. The 14-pg catalog presents a line of threaded inserts. It discusses SI ultrasonic, molded, and postmolded threaded inserts. The publication provides parts' designations, materials, thread sizes, and specifications. **Standard Insert**, 5190 Old Easton Rd, Danboro, PA 18916. Phone (800) 338-3502; (215) 766-0960. FAX (215) 766-0962. **Circle No. 467**



Booklet of coaxial connectors. This 8-pg catalog details 55 coaxial and twin-axial connectors for pc-board applications. It includes designs for board-to-board, board-to-panel, and board-to-cable assembly types used in 55 and 75 Ω applications. The publication features BNC, TNC, Mini-UHF, Twinax, SMA, SMB, SMC, SSMA, SSMB, and SSMC

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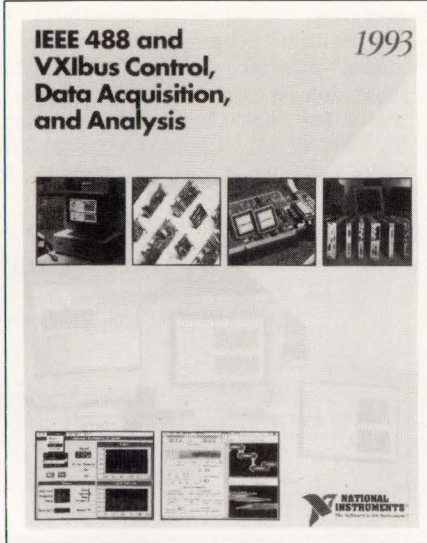
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connector series. Other products covered include coaxial contacts for D-Subminiature connectors and customer specials. **Amphenol Corp.**, RF/Microwave Operations, 1 Kennedy Ave, Danbury, CT 06810. Phone (203) 743-9272. FAX (203) 796-2032. TWX 710-456-0281. **Circle No. 468**



Measurement and instrumentation products. This 1993 catalog describes software and hardware for developing integrated measurement and instrumentation systems based on PC/XT, PC/AT, EISA, Macintosh, Sun, Hewlett-Packard, Digital Equipment Corp, and other computer companies. It discusses applications that require the measurement, monitoring, or control of physical phenomena. Applications include laboratory automation, automated test, process monitoring and control, factory automation, applied chemistry, educational instruction and research, medical research, and motion control. The 544-pg catalog is color-coded by section—Application Software, IEEE-488, Data Acquisition, VXI/MXI, and Training. The first four sections present tutorials with examples of IEEE-488.2, SCPI (standard commands for programmable instruments), plug-in data-acquisition systems, signal-conditioning accessories, DSP, VXI, and MXI. **National Instruments**, 6504 Bridge Point Pkwy, Austin, TX 78730. Phone in US and Canada, (800) 433-3488; (512) 794-0100. FAX (512) 794-8411. **Circle No. 469**

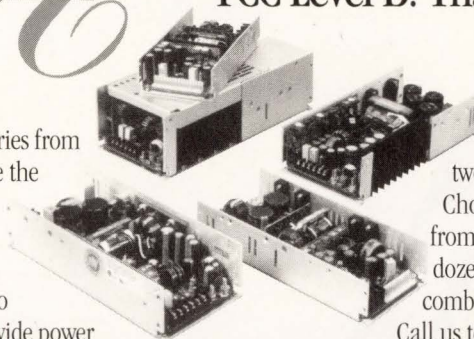
Interface and logic products cataloged. The 350-pg catalog entitled *Automation Interface and Logic Products* features advanced control devices in 12 product areas: switching amplifiers,

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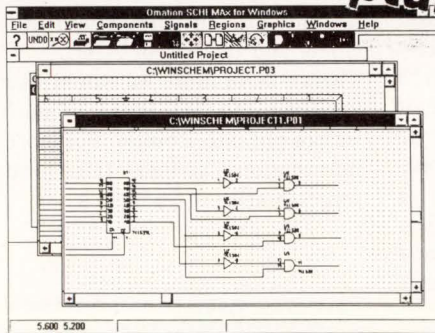
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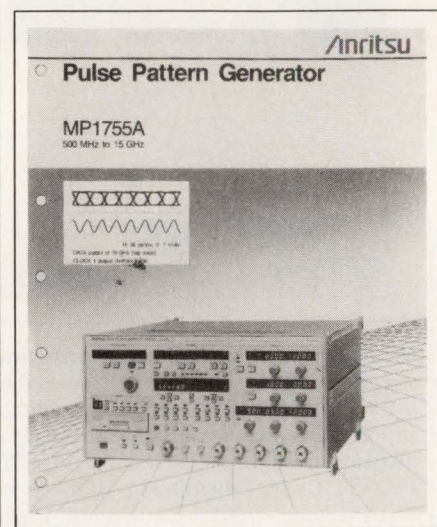
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Pamphlet on pulse-pattern generator. This 6-pg brochure deals with the MP1755A pulse-pattern generator. It contains graphs for the numerical relation between word length and number of words, between word length and step width, and the relationship between pages of the Word and Data mode. The photos help in understanding clock outputs and $1/2$ - and $1/4$ -speed output. The publication explains 512-kbit programmable patterns, complementary clock outputs, variable amplitudes and offsets, and multiplexer operation. **Anritsu Wiltron Sales Co.**, 685 Jarvis Dr, Morgan Hill, CA 95037. Phone (408) 776-8300. **Circle No. 559**

PCXI catalog. The PCXI catalog describes 486 EISA systems that conform to the PCXI (PC Bus Extended for Industry) Consortium EISA Passive Backplane Standard. It also provides a database of industrial EISA products and explains how to configure your PCXI system. **Rapid Systems**, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. **Circle No. 560**

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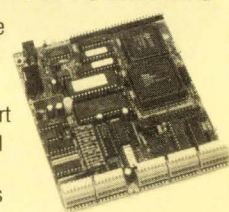
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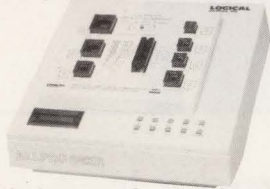
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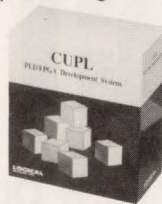
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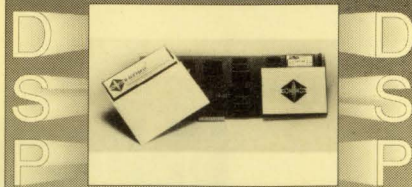


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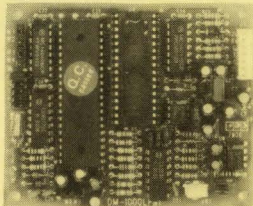
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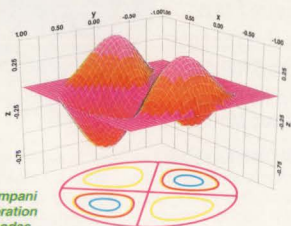
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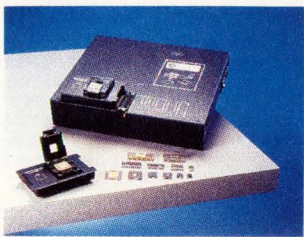
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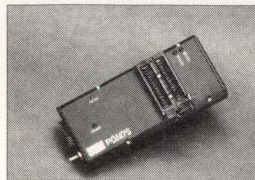
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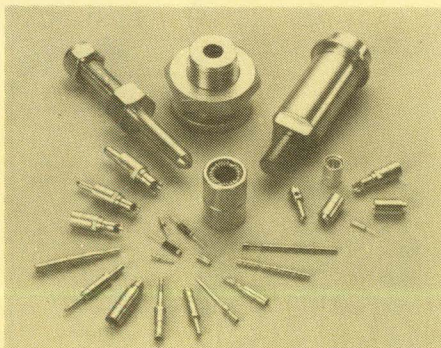
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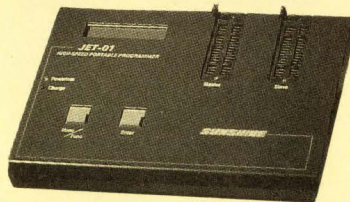
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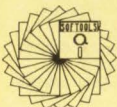
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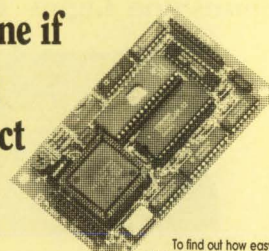
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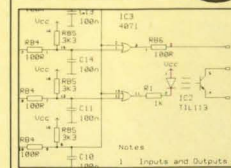
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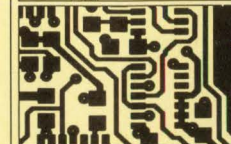
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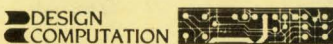
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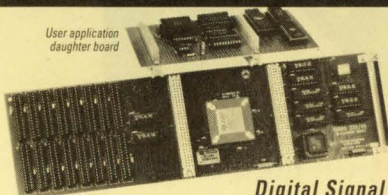


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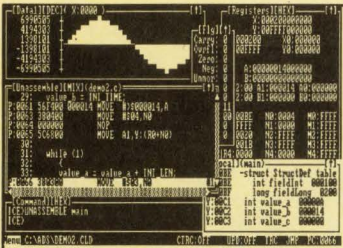
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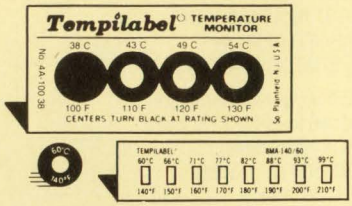
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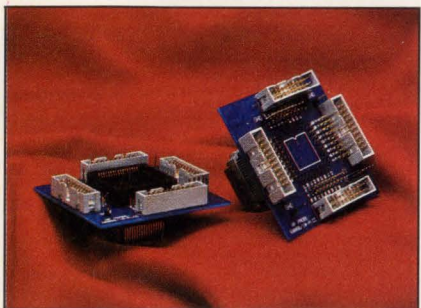


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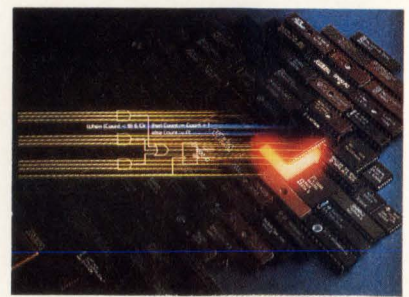
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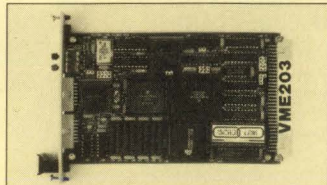
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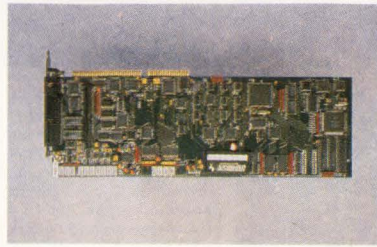
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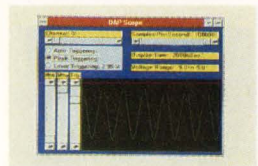
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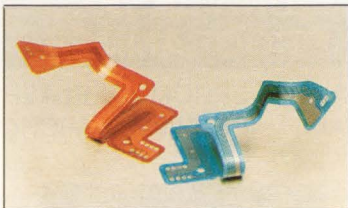


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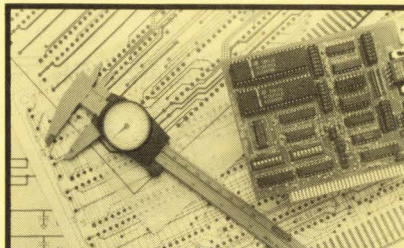


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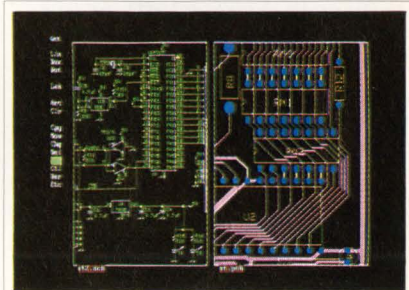
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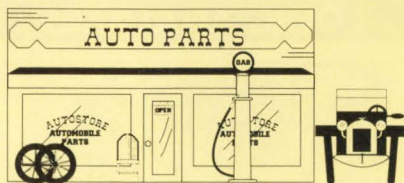
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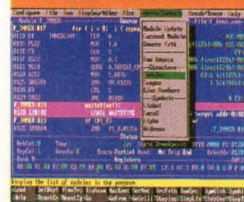
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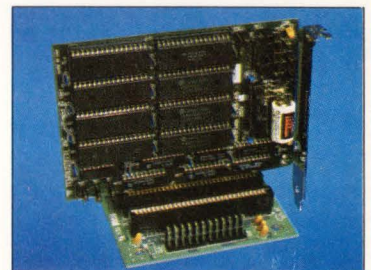
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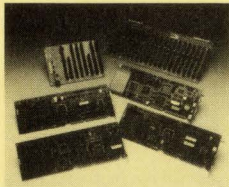
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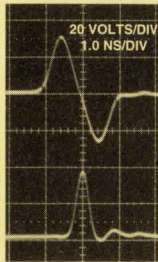
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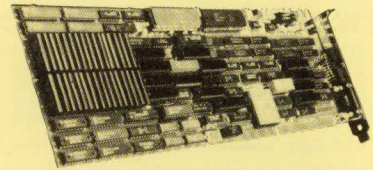
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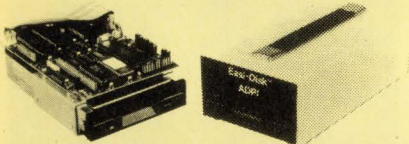
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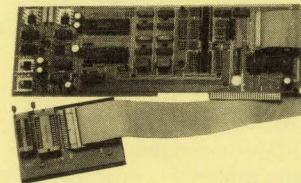
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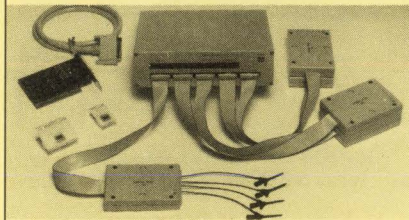


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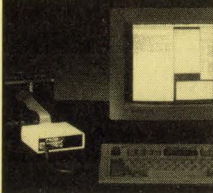
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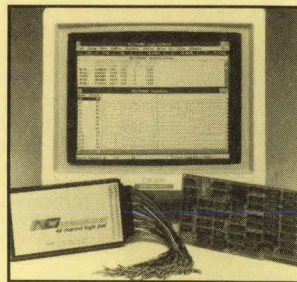


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- Modelling software evaluation and electrical characterization measurement techniques experience.

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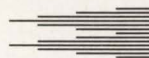
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- Litton Data Systems has achieved a well-respected position as one of the world's foremost developers and manufacturers of military command, control and communications (C³) systems. We are currently seeking qualified engineers to work on the THAAD project. A component of SDI, THAAD will defend large geographical areas from tactical ballistic missile threat.

Systems Engineers

- These positions require individuals with 5-15 years' experience in defining and documenting software and interface requirements using DOD-STD-2167A. Background in OOA/OOD, CASE tools, Ada and Army common hardware/software desired. Air Defense user experience a plus. Excellent communication skills and a technical degree (Master's preferred) also required.

Software Engineers

- These positions require individuals with 5-10 years' experience with Ada, real-time/C³ systems and modern software engineering methods. As part of a technical or implementation team, the successful candidates will perform detailed design, code, unit test and documentation. Additional duties include supporting inspections and reviews and assisting with software integration and test. BA/BS, or equivalent, in Computer Science or related field a must.

Systems Architecture Engineers

- These position require individuals with 5-15 years systems architecture experience with real-time systems. Experience with Unix system calls, Ada, and modern software engineering methods a must. Computer Science or equivalent degree required.
- Applicants selected will be subject to a security investigation and must meet eligibility requirements for access to classified information. U.S. citizenship required.

For immediate consideration, please forward your resume, including salary history to:
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This individual will define/design board-level products, develop technical product literature, provide technical analysis of competing products, and interface with key groups to support new and existing products. In addition to a strong background in PC graphics system hardware design and leadership capabilities, you will need a BSEE and 6-10 years engineering experience with VGA graphic system design. 2-3 years' management experience with multimedia, BIOS and customer support are a plus.

Sr. Applications Engineer

This successful candidate will work in a high energy, team environment and will need 5+ years of VGA graphic experience, a BSCS or BSEE and possess a solid understanding of both hardware/software; VGA adaptors, assembly, "C", BIOS and drivers. Excellent verbal and written communication skills are essential.

Sr. Software Engineer

Windows Display Driver

Successful candidate selected for this position will need a BS/MS in Computer Science, 4-5 years experience in assembly and "C" language, and a solid working knowledge with VGA programming. Experience with MS Windows SDK and DDK also required.

Sr. Logic Design Engineer

This technically proficient professional must be thoroughly familiar with various ASIC design methodologies, tools and processes. In addition, possess a solid background in ISA bus, CPU local bus, PC and computer graphic architecture. MSEE required. A good understanding of LCD technology, Verilog and HDL and System Programming background is an extra.

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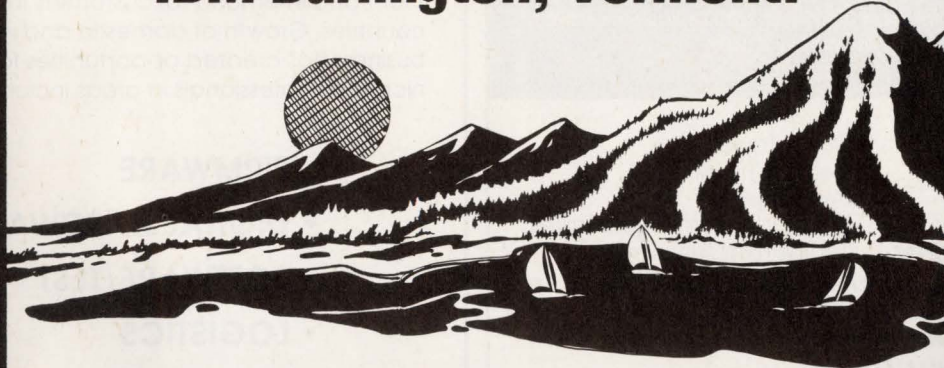


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One of the world's most advanced semiconductor operations is what you'll find at IBM's major development and manufacturing facility in Burlington, where continued business growth is matched by a superb living environment. We now have outstanding career opportunities for engineers with the specialized computer skills to make significant impact on RISC microprocessor development.

Logic Design

Responsible for definition, logic design and verification of high performance RISC microprocessors. To qualify, you must possess a BSEE or higher, with an emphasis on Computer Engineering, and be capable of carrying logic design through to physical chip design stage. Minimum of 3 years in logic/chip, CMOS and VLSI design required. RISC experience is key. Background in microprocessor and multiprocessor design desirable.

Circuit Design

Will design CMOS circuitry for RISC-based microprocessor functions. Includes custom SRAM cache design, complex logic dataflow circuitry, random logic, IO, clocking and other circuitry in custom microprocessor layouts. Requires BSEE or higher with emphasis on Computer Engineering or Circuit Design. Ability to design complex CMOS or Bi CMOS circuits and perform circuit analysis and verification is essential, along with minimum of 3 years circuit design experience in industry. CMOS, VLSI, digital circuit design is a prerequisite.

Physical Design

Responsible for CMOS VLSI chip physical design of RISC microprocessor in advanced CMOS technology. Includes using state-of-the-art CAD tools to perform chip layout, wiring and chip timing analysis. A BSEE or higher, with emphasis on Computer Engineering or Circuit Design, is essential, along with at least 3 years of physical design experience in industry. RISC and CMOS, VLSI design experience (chip layout/wiring) necessary. Background in microprocessor design desirable.

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Harris Corporation's RF Communications Division is a worldwide supplier of complete radio communications systems solutions to U.S. Government and international customers in over 100 countries. Growth of domestic and international business has created opportunities for Communications Professionals in areas including:

- FIRMWARE
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The positions require a BSEE/CE/ME/CS or equivalent and 5+ years' relevant experience; an MS is desirable. Some positions require ability to obtain U.S. Security Clearance. Multi-lingual skills are desirable.

For prompt consideration, please send resume in confidence to: HARRIS CORPORATION, RF Communications Group, HR Dept. EDN, 1680 University Avenue, Rochester, NY 14610. An Equal Opportunity Employer M/F/D/V.

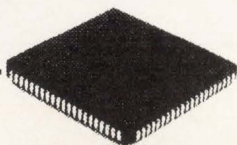


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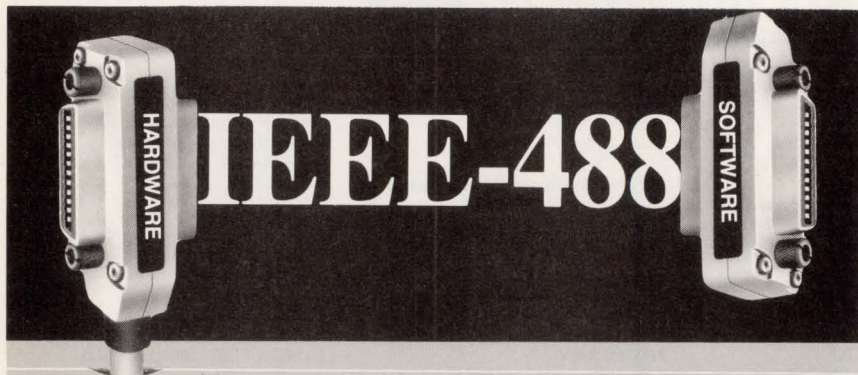
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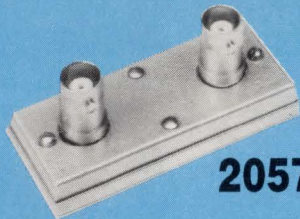
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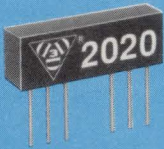
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- A/D—analog to digital
- AGC—automatic gain control
- ANSI—American National Standards Institute
- ASIC—application-specific integrated circuit
- ATE—automatic test equipment
- BBS—bulletin-board system
- CAE—computer-aided engineering
- CAM—Common Access Method
- CCB—CAM Command Block
- CDB—Command Descriptor Block (a CAM term)
- CD-ROM—compact-disk read-only memory
- CEO—chief executive officer
- CMOS—complementary metal-oxide semiconductor
- D/A—digital to analog
- DoD—Department of Defense
- DSP—digital signal processing
- FFT—fast Fourier transform
- FIR—finite-impulse-response
- FPT—fine-pitch technology
- IEEE-1149.1—the IEEE standard for boundary-scan testing
- IEEE—The Institute of Electrical and Electronics Engineers
- IF—intermediate frequency
- IIR—infinite-impulse-response
- I/O—input-output
- I-T-L—Initiator Target LUN (a CAM term)
- LBA—logical block address
- LUN—logical unit number (a CAM term)
- MCM—multichip module
- MS-DOS—Microsoft Disk Operating System
- NMOS—N-channel metal-oxide semiconductor operating system
- pc—printed circuit
- RAID—redundant array of independent disks
- rms—root-mean-square
- SAW—surface acoustic wave
- SCSI—Small Computer System Interface
- SIG—special interest group
- SIM—SCSI Interface Module (a CAM term)
- TAB—tape-automated bonding
- TAP—test-access port
- TCK—test clock, a signal on an IEEE-1149 TAP
- TDI—test-data input, a signal on an IEEE-1149 TAP
- TDO—test-data output, a signal on an IEEE-1149 TAP
- TMS—test-mode select, a signal on an IEEE-1149 TAP
- VLSI—very large-scale integration

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EDN-HANDS ON!

Product reviews from EDN's editors and readers

Magazine probes science and technology

In many of my editorials I've been promoting better science and math skills for young people. Unfortunately, there have been few sources of interesting and fun math and science information and activities for these young people. A subscription to the magazine *Science Probe!* may be just the gift for a young person you know with a budding or even a strong interest in scientific topics. After all, it's today's young people who will—hopefully—become scientists and engineers as many of us prepare to retire. Recent issues of *Science Probe!* have explored how to photograph ice crystals with polarized light, basic statistics, the Hubble space telescope, and experiments in horticulture. In my opinion, the magazine appeals to people age 12 and older.

Each 128-page issue of the quarterly magazine features articles about many areas of science, and it includes science projects and activities. The magazine covers electronic and computer projects, too. Although the magazine aims its editorial coverage at young scientists, the publication has many professional scientists, researchers, and engineers on its subscription lists.

The publication boasts of a top-notch line up of editors and contributors. Larry Steckler, the publisher, had a long history at *Radio-Electronics* magazine, and editor Forrest Mims III has been writing about science and electronics for as long as I can remember. Among the frequent contributors are William Barden Jr and Harry Helms, who both have many science and electronics articles to their credit.

The magazine is well organized, and it makes good use of color and typography to emphasize points and illustrate topics. Although the articles are meant for "amateur" scientists, the authors and editors don't

shy away from tackling difficult topics. In addition, illustrations often include spectrograms, 3-D diagrams, and schematic diagrams that present the right level of detail for readers. Illustrations enlighten rather than confuse. When an article calls for special products or equipment, you'll find sources listed within each article.

Most of us tend to think of engineering and science as professions that are dominated by males. Mims reports that the magazine has a large contingent of female subscribers and that most of the science-fair reports come from girls. That's an encouraging sign for those of us with female offspring or relatives who show interests in science and technology. The magazine portrays men and women and girls and boys equally, too.

If you know a young person who is interested, even mildly, in science, engineering and "technical things," I recommend *Science Probe!* highly.

—Jon Titus

A subscription costs \$9.95, post-paid. Postage to Canada costs an additional \$6.05, and postage to other countries costs \$7.50 per year. For subscriptions or other information, write to *Science Probe!*, 500-B Bi-County Blvd, Farmingdale, NY 11735. Phone (516) 293-0467. FAX (516) 293-3115.

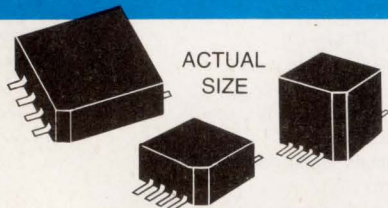
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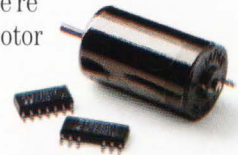
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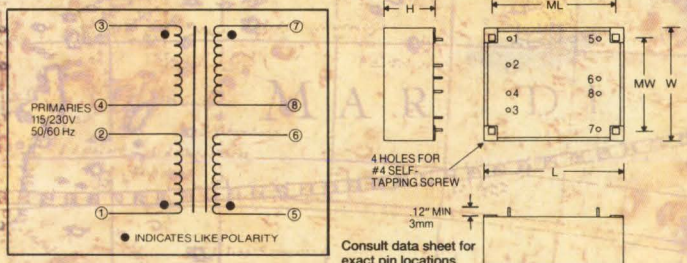
For more information on Signal's International Flathead Series, contact Signal Transformer, 500 Bayview Ave., Inwood, NY 11696.

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IF-2-16	2VA	16Vct. @ 125mA	8V @ 250mA	
IF-2-20	2VA	20Vct. @ 100mA	10V @ 200mA	
IF-2-24	2VA	24Vct. @ 85mA	12V @ 170mA	
IF-2-30	2VA	30Vct. @ 70mA	15V @ 140mA	
IF-2-34	2VA	34Vct. @ 60mA	17V @ 120mA	
IF-2-40	2VA	40Vct. @ 50mA	20V @ 100mA	
IF-2-56	2VA	56Vct. @ 40mA	28V @ 80mA	
IF-2-230	2VA	230Vct. @ 9mA	115V @ 18mA	
IF-10-10	10VA	10Vct. @ 1.00A	5V @ 2.00A	\$9.49
IF-10-12	10VA	12Vct. @ 835mA	6V @ 1.67A	
IF-10-16	10VA	16Vct. @ 625mA	8V @ 1.25A	
IF-10-20	10VA	20Vct. @ 500mA	10V @ 1.00A	
IF-10-24	10VA	24Vct. @ 420mA	12V @ 840mA	
IF-10-30	10VA	30Vct. @ 335mA	15V @ 670mA	
IF-10-34	10VA	34Vct. @ 300mA	17V @ 600mA	
IF-10-40	10VA	40Vct. @ 250mA	20V @ 500mA	
IF-10-56	10VA	56Vct. @ 180mA	28V @ 360mA	
IF-10-230	10VA	230Vct. @ 45mA	115V @ 90mA	
IF-30-10	30VA	10Vct. @ 3.00A	5V @ 6.00A	\$13.99
IF-30-12	30VA	12Vct. @ 2.50A	6V @ 5.00A	
IF-30-16	30VA	16Vct. @ 1.90A	8V @ 3.80A	
IF-30-20	30VA	20Vct. @ 1.50A	10V @ 3.00A	
IF-30-24	30VA	24Vct. @ 1.25A	12V @ 2.50A	
IF-30-30	30VA	30Vct. @ 1.00A	15V @ 2.00A	
IF-30-34	30VA	34Vct. @ 900mA	17V @ 1.80A	
IF-30-40	30VA	40Vct. @ 750mA	20V @ 1.50A	
IF-30-56	30VA	56Vct. @ 550mA	28V @ 1.10A	
IF-30-230	30VA	230Vct. @ 130mA	115V @ 260mA	



Size	L	W	H	ML	MW	WGT
2	2.09" 53.0mm	1.73" 44.0mm	0.69" 17.6mm	1.87" 47.5mm	1.48" 37.5mm	4.6oz 0.13kg
10	2.66" 67.6mm	2.24" 57.0mm	0.89" 22.6mm	2.46" 62.5mm	1.97" 50.0mm	10.3oz 0.29kg
30	2.68" 68.0mm	2.26" 57.5mm	1.39" 35.3mm	2.46" 62.5mm	1.97" 50.0mm	19.7oz 0.58kg

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