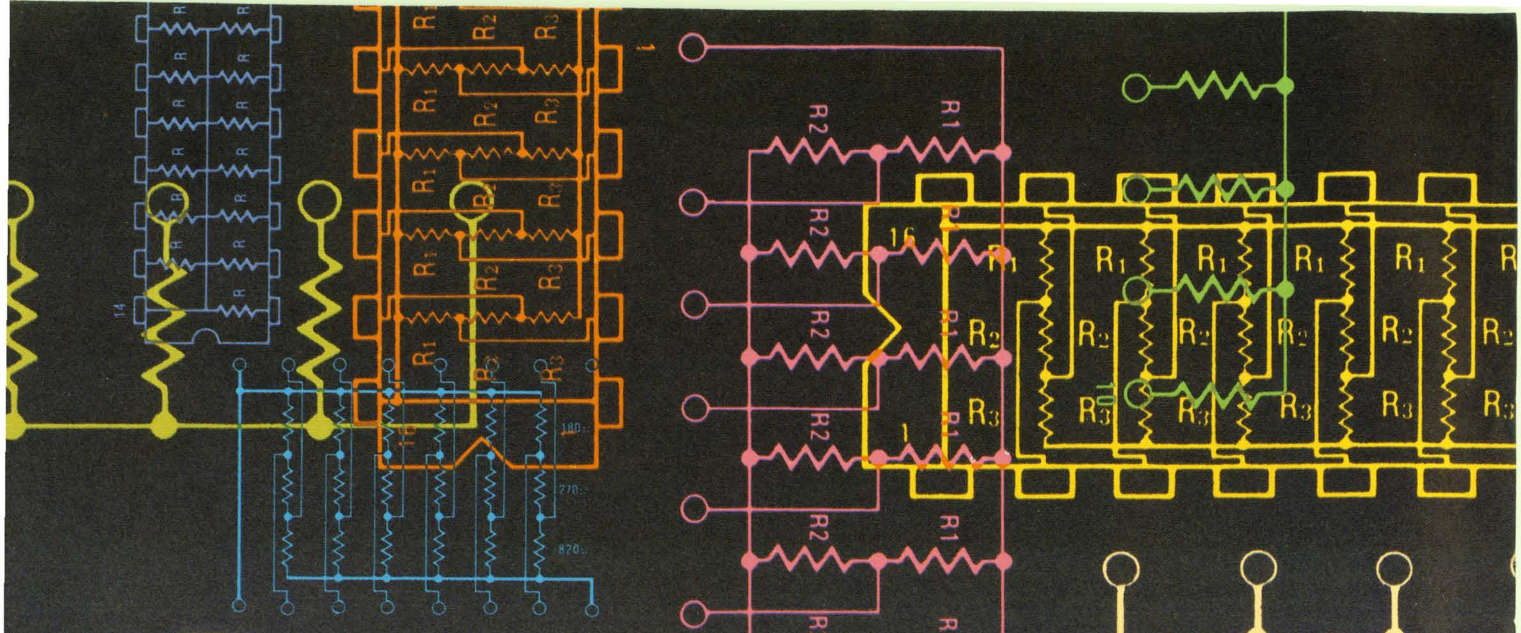
VOL. 25 NO. 21

# Electronic Design®

FOR ENGINEERS AND ENGINEERING MANAGERS

OCT. 11, 1977

**Selecting a processor** no longer requires wading through dozens of manuals. Electronic Design's μP Data Manual describes each processor's performance and the available hardware and software support. Also included are spec summary tables, discussions of spec pitfalls and a primer for the μP beginner. Start on page 54.



# Bourns resistor networks

## . . . for the "discreet" design engineer.

Sure, you've already made a smart decision, choosing networks over discrete resistors. After all, the cost per resistor in a network package can be 40% less; they require only 10-15% of the P.C. board space needed by discretes; and component count is reduced as much as 95% with resistor networks.

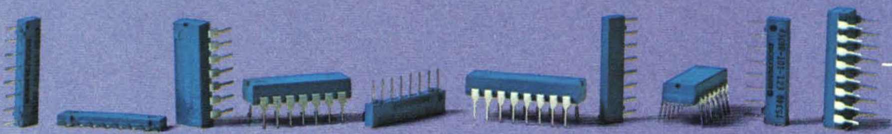
But, when choosing a network supplier, you should also consider these points:

1. Bourns has the broadest network product line in the industry — over 1000 part numbers in all. And our standard DIP circuits range from simple pull-up configurations to Thevinin-equivalent ECL terminators and memory interface circuits.
2. Bourns Krimp-Joint™ offers both a mechanical and electrical bond that lap or butt joint construction doesn't provide. The lead is crimped onto the network element and a high-temp, reflow-resistant solder is used to prevent failure during wave soldering and in circuit thermal cycling and vibration.
3. Bourns was the first manufacturer to offer a complete line of off-the-shelf, super low profile SIPs with demonstrated automatic insertion capability.

These are the facts. So, now you can be even more "discreet". We're sure you'll specify Bourns Resistor Networks — direct or through your local distributor.

Send today for our new 1977 Resistor Networks Catalog.

TRIMPOT PRODUCTS DIVISION, BOURNS, INC., 1200 Columbia Avenue, Riverside, CA 92507, Telephone 714 781-5415 — TWX 910 332-1252.



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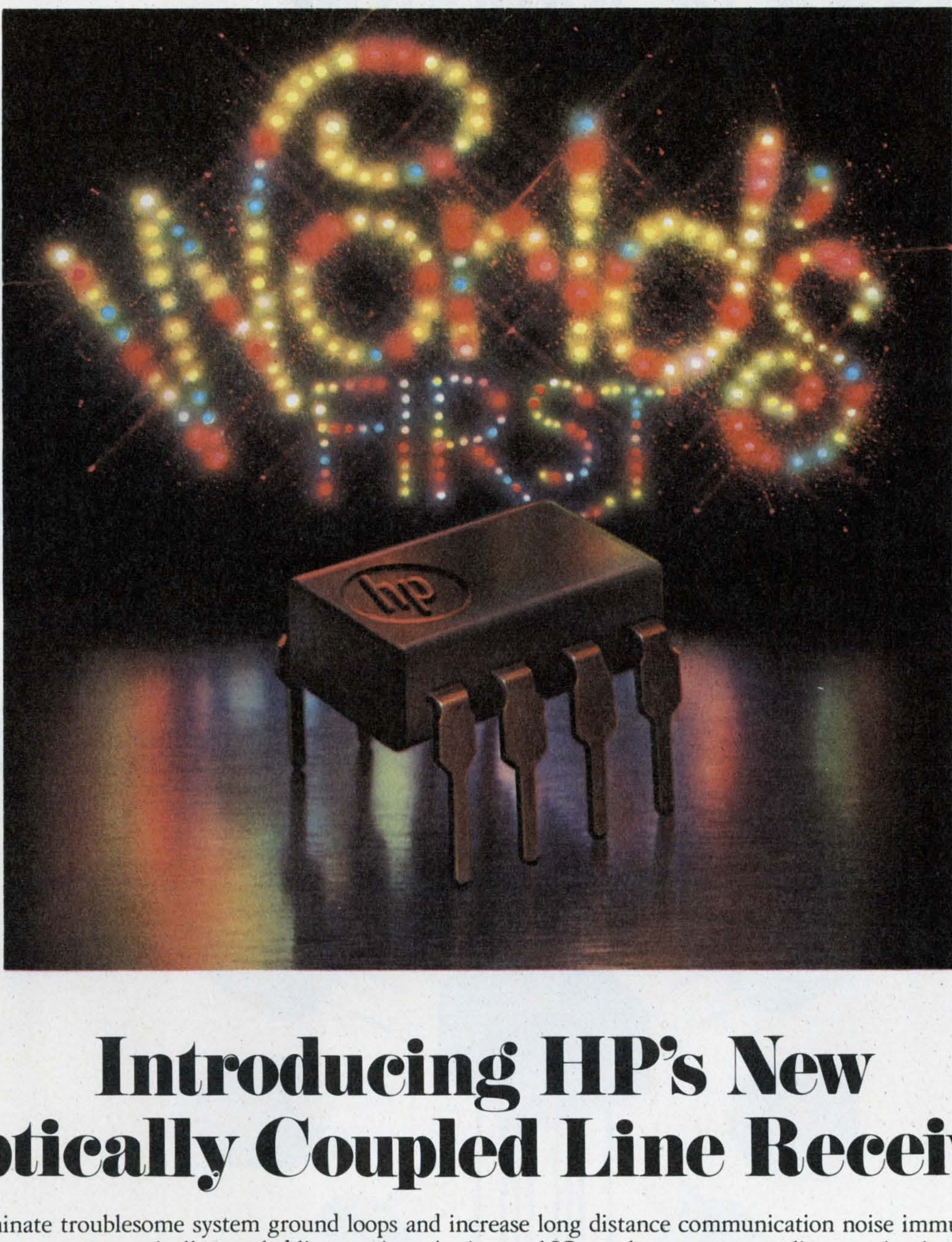
**For Immediate Application — Circle 130**
**For Future Application — Circle 230**

# SURPRISE!




## Introducing HP's New Optically Coupled Line Receiver

Eliminate troublesome system ground loops and increase long distance communication noise immunity with HP's new easy-to-use optically coupled line receiver. An internal IC regulator serves as a line termination and allows direct connection to transmission lines without any additional components.

Use of a high-speed, high-gain output photo IC permits data rates in excess of 10 Mbits/second. An internal shield provides excellent common mode rejection even at these high data rates.

The HCPL-2602 is designed for high-speed data transmission applications such as computer-peripheral interface, instrumentation, and simplex/multiplex data transmission.

Priced at $6.65* in quantities of 1000, the HCPL-2602 is in stock at any franchised distributor. In the U.S., contact Hall-Mark, Wilshire or the Wyle Distribution Group (Liberty-Elmar) for immediate delivery. In Canada, just call Zentronics, Ltd. *U.S. Domestic price only

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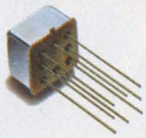
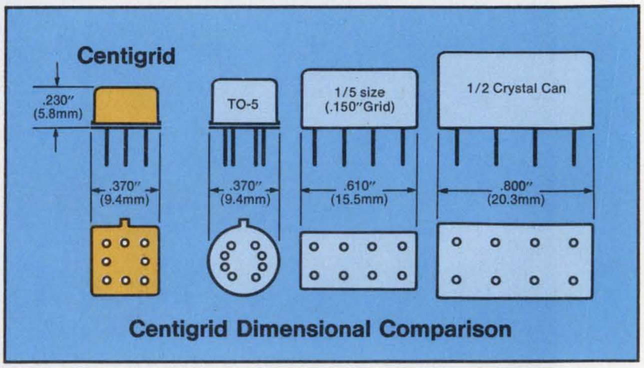
CIRCLE NUMBER 2

# TO-5 RELAY UPDATE

# The Relay of Tomorrow is here today: the Centigrid.



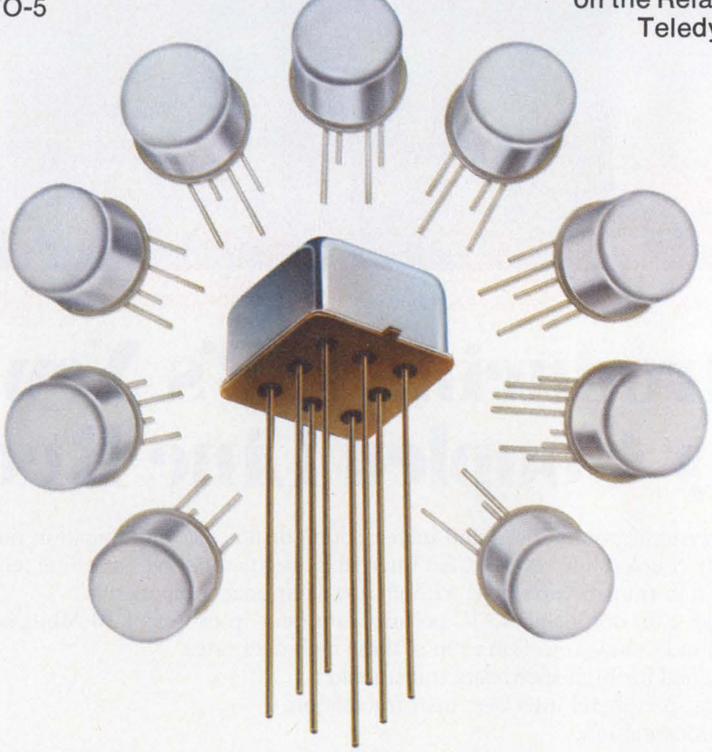



*Out of Teledyne's TO-5 relay technology has evolved the Centigrid® — the ultimate subminiature relay.* It combines the proven TO-5 relay design concept and internal construction into an even more compact package. Low profile height — just .230″ (5.84mm) — with terminals spaced on a .100″ (2.54mm) grid permitting direct pc board mounting without the need for lead spreading.

Add to this the same low coil power consumption as the TO-5 relay, with obvious thermal and power supply advantages. And for RF switching, the Centigrid's low inter-contact capacitance and contact circuit losses provide high isolation and low insertion loss up through UHF frequencies.

*To top it all off, the Centigrid is qualified to levels "L" and "M" of MIL-R-39016, including the internal diode suppressed versions.*

For complete specification data on the Relay of Tomorrow, contact Teledyne Relays, the technology leader in the relay industry.



## TELEDYNE RELAYS

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CIRCLE NUMBER 3

# Electronic Design® 21

VOL. 25 NO. 21

FOR ENGINEERS AND ENGINEERING MANAGERS

OCT. 11, 1977


## NEWS



## TECHNOLOGY



## PRODUCTS



## DEPARTMENTS



**Cover:** Photo by Art Director, Bill Kelly


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POSTMASTER: Please send form 3579 to ELECTRONIC DESIGN, P.O. Box 13803, Philadelphia, PA 19101.

# 8-bit DAC's that think otherwise.

# Across the desk

## Late WOM tester

We regret the delay in our publication of the April 1 announcement of the new Tektronix WOM tester. The system is intended for use with the Signuteks 9046 X N random-access write-only memory or equivalents. The system is unique in its testing neu devices (which enhance or deplete regardless of gate polarity).

The tester provides fast, clean pulses by use of Pushme-Pullyou Drivers. Quadra-state comparators allow flexibility in checking WOM outputs with only 12 clock phases.

The system uses TEKTEST IXX, Version 999.99, which is neither upward nor downward compatible with other test languages due to its unique language structure. Users can be freed of problems with hexadecimal, octal and other cumbersome languages, and revel in the simplicity of ones and zeros. No compilers, assemblers or translators are needed, so there is ample space for test programs.

The instruction set includes:

| | |
|---|---|
| BH | Branch and Hang |
| IIB | Ignore Inquiry and Branch |
| TDB | Transfer and Drop Bits |
| DO | Divide and Overflow |
| SRZ | Subtract and Reset to Zero |
| PI | Punch Invalid |
| SSJ | Select Stacker and Jump |
| FSRA | Forms Skip and Run Away |
| RASC | Read and Shred Card |
| SRSD | Seek Record and Scar Disc |
| BST | Backspace and Stretch Tape |
| RIRG | Read Inter-Record Gap |
| UER | Update and Erase Record |
| SPSW | Scramble Program Status Word |
| EIOC | Execute Invalid Op Code |
| EROS | Erase Read-Only Storage |
| PBC | Print and Break Chain |
| CM | Circulate Memory |
| MLR | Move and Lose Record |
| CRN | Convert to Roman Numberals |
| DMPK | Destroy Memory Protect Key |
| DC | Divide and Conquer |
| EIP | Execute Programmer Immediate |
| LCC | Load and Clear Core |
| HCF | Halt and Catch Fire |
| IDC | Initiate Destruct Command |

The address ports of the WOM are multiplexed with a negative frequency to achieve optimum resolution. The drain on the WOM is tested by monitoring a 5-gallon bucket.

Handlers are easily interfaced to this tester with only 500 signal lines. The system is capable of binning into two categories: one for NO-GO DIPs, the other for FAILED $I^2R$. If the $I^2R$ mode occurs, it's time to call the power-distribution agency to find out how many substations went "WOM" as they exceeded maximum dissipation.

Depending on configuration, this machine will sell competitively from $1.98 to something less than the national debt.

For more information **Circle 120**

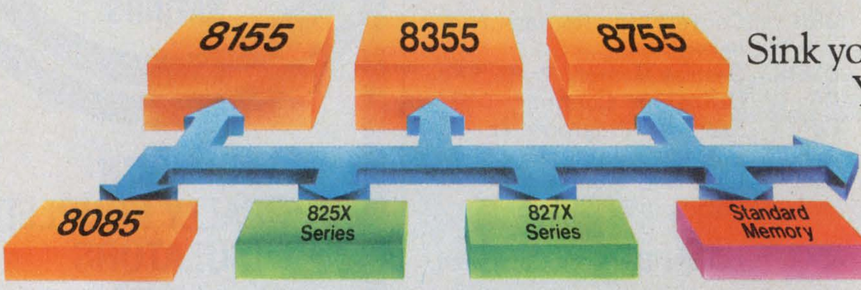
## More resolution

Peter Simmons, marketing manager of EMI Technology's Instrumentation Division, now reminds us that his firm, too, markets a 6-½-digit voltmeter. In our March 1 story on Guildline Instruments' 7-½-digit instrument (ED No. 5, p. 18), we said that the highest-resolution DVM available in the United States was the 6-½-digit Dana/Keithley 6900. The Model SM215 from EMI and the DM-1000 from Julie Research, New York, also resolve 6-½ digits.

*(continued on page 272)*

**Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Managing Editor, Electronic Design, 50 Essex St., Rochelle Park, NJ 07662. Try to keep letters under 200 words. Letters must be signed. Names will be withheld upon request.**

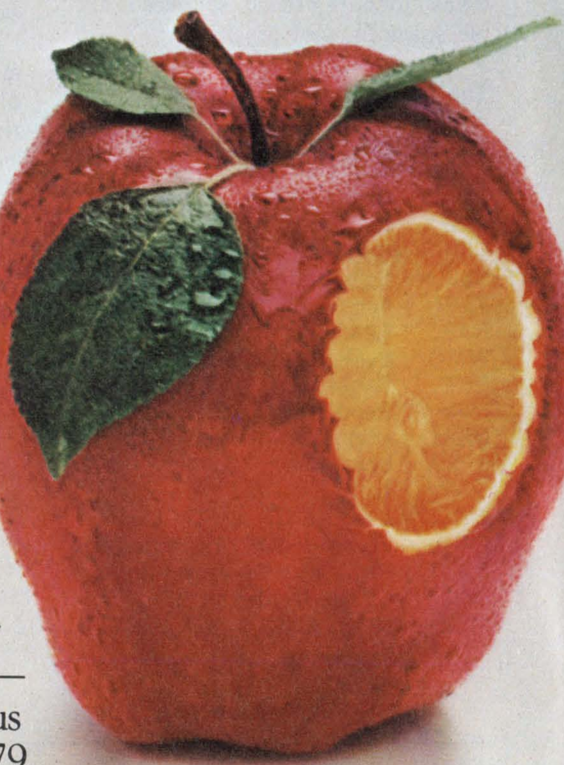
# Intel delivers the 8085, designers just




Sink your teeth into Intel's new 8085. You'll find it's the only microcomputer that combines the performance, economic advantages and total support it takes to be recognized as the new industry standard. So it's no surprise that there are already four announced sources for the 8085. In fact, the deeper you go, the better the 8085 gets.

The 8085, even more than the 8080 it succeeds, is a total design solution, not just a component. It delivers higher performance, for capabilities far beyond the 8080's. It has a higher level of integration, so you can design your products with fewer components, making them more competitive and more profitable. And to help you get those products to market quicker we've given the 8085 the industry's broadest base of system and development support.

Yet the 8085 is fully compatible with the 8080. So your investment in existing designs is protected, and implementing new designs is simplified by the wealth of 8080 software and peripherals at your disposal.



It all adds up to a design solution you won't be able to resist. That's true for a broad range of applications. The 8085 can be designed in as an economical stand-alone three-chip system using the 8085 CPU, the 8155 256-byte RAM with I/O and timer, and the 8755 2K-byte EPROM with I/O or its interchangeable 8355 ROM with I/O.

You can expand this basic system for larger applications using additional RAM, ROM, EPROM and Intel's complete family of first and second generation peripheral controllers, including our four new programmable peripheral controller chips—the 8271* Floppy Disc Controller, 8273* Synchronous Data Link Controller, 8275 CRT Controller and 8279 Keyboard/Display Interface. All these components including 8755 EPROM operate from a single +5V supply.

*Available 4th Quarter 1977

# the new microcomputer can't resist.

A multiplexed data/address bus permits integration of many auxiliary system functions—such as clock generation, system control and multiple interrupts—onto the 8085 chip while maintaining 8080 compatibility and the same 40-pin package. And forward-thinking engineers will realize that it is also a link to Intel's future generation microcomputer products.

No microcomputer can match the 8085 as a total design solution because no microcomputer can come close to the 8085's support base. Support for the 8085 includes the Intellec® microcomputer development system with resident PL/M, the high level programming language that can cut months off your software development time. Intellec is the only development system with ICE-85,™ providing in-*system* emulation for faster system development and debugging. Then there's application assistance, training classes and seminars worldwide. And a comprehensive development software library at your disposal.

The quickest way to get a taste of the 8085's power and versatility is with the SDK-85 System Design Kit. It's available now for only $250. You can order SDK-85 and all MCS-85™ components directly from your nearest Intel distributor: Almac/Stroum, Components Specialties, Cramer, Hamilton/Avnet, Harvey Electronics, Industrial Components, Pioneer, Sheridan, L.A. Varah, Wyle Liberty/Elmar or Zentronics.

Or, for more information on the 8085 and SDK-85, use the reader service card or write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051. Telephone: (408) 246-7501.

**MCS-85™ Microcomputer System Components Family**

**8085 CPU** with system bus control, system clock generator, serial I/O and 4-level interrupt control.
**8155/8156 RAM, I/O & Timer.** 256-byte static RAM, 22 I/O lines, 14-bit programmable interval timer/event counter.
**8355 ROM & I/O.** 2048-byte masked ROM, 16 I/O lines. Interchangeable with 8755.
**8755 Erasable PROM & I/O.** 2048-byte UV erasable and electrically reprogrammable EPROM. Interchangeable with 8355.

**Compatible MCS-80™/MCS-85™ Peripheral Components**

*General Purpose*
**8251 Programmable Communications Interface**
**8253 Programmable Interval Timer**
**8255 Programmable Peripheral Interface**
**8257 Programmable DMA Controller**
**8259 Programmable Interrupt Controller**
**8205 High Speed 1 out of 8 Binary Decoder**
**8212 8-bit Input/Output Port** (Latch/Buffer)
**8216/8226 4-bit Parallel Bidirectional Bus Driver**
*Dedicated Function*
**8271 Programmable Floppy Disk Controller**
**8273 SDLC Protocol Controller**
**8275 Programmable CRT Controller**
**8279 Programmable Keyboard/Display Interface**

**Performance Matched Standard Memory**

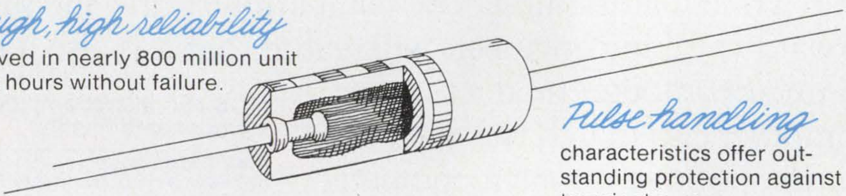
*Static RAM*
**2114** 1024x4-bit, 450 nsec, 18 pin
**2142** 1024x4-bit, 450 nsec, 20 pin
**8101A-4** 256x4-bit, 450 nsec, separate I/O
**8102A-4** 1024x1-bit, 450 nsec, separate I/O
**8111A-4** 256x4-bit, 450 nsec, common I/O
*ROM/EPROM*
**2716** 2048x8-bit Erasable PROM, 450 nsec
**2708** 1024x8-bit Erasable PROM, 450 nsec
**2316E** 2048x8-bit Masked ROM, 450 nsec
**8308** 1024x8-bit Masked ROM, 450 nsec

**intel® delivers.**

# When you're small you've got to be tough to last.

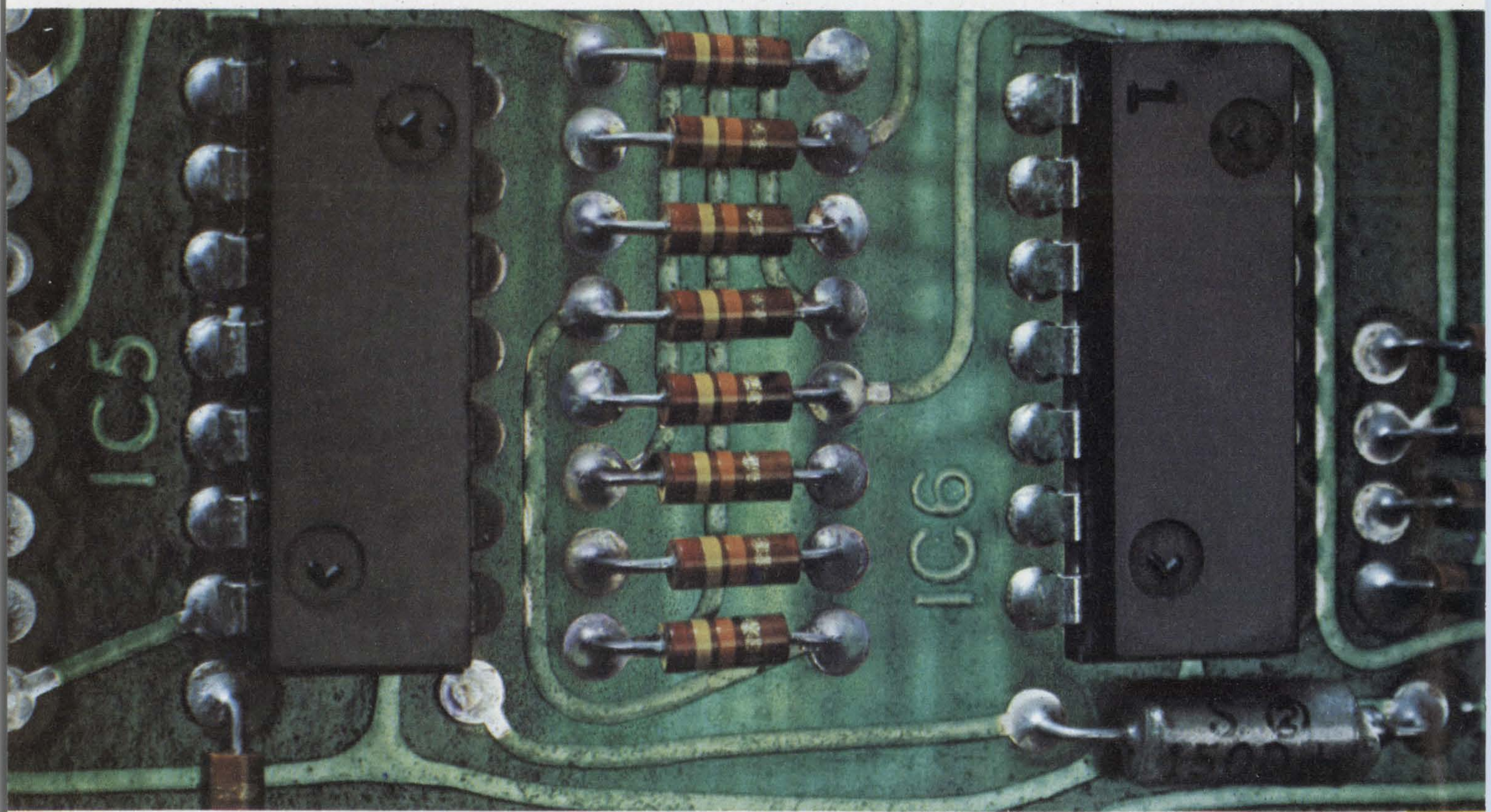
This rugged little ⅛-watt fixed resistor (.145 L x .062 D) is hard to beat in durability. It's the Type BB...part of a family that has passed nearly 800 million unit test hours without a single failure. It's small enough to be mounted on .300 by .100 hole centers, eight in the same space as one dual in-line package. It takes transient pulses that would knock out most any film resistor of similar dimensions. Performance is exceptionally consistent from one resistor to the next. We have the space-saving resistors you need. Our distributors have them when your need is now.

*Tough, high reliability*
Proved in nearly 800 million unit test hours without failure.



*Pulse handling*
characteristics offer outstanding protection against transient surges.

*Low TCR*
typically less than 200 PPM over normal operating temperature range of +15°C to +75°C.

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**CIRCLE NUMBER 7**

# Precision quad op amps.

# *Precision.*

## PMI's new OP-09 and OP-11 are pin-compatible with the un-precision quads now on the market.

The quad op amp has finally come of age. With the introduction of the OP-09 and OP-11, PMI has made it a truly workable reality. Consider:

## Low $V_{OS}$ and other goodies.

Since quads can't be nulled—there aren't enough pins available—the user is at the mercy of whatever input offset voltage ($V_{OS}$) he happens to get. PMI refined the manufacturing process to get $V_{OS}$ under control. We came up with the lowest $V_{OS}$ of any quad op amp made today.

At the same time, we gave the OP-09 and OP-11 the highest gain and the lowest drift of any quad op amp. We expanded bandwidth, reduced offset and supply current, and increased the slew rate. Here it is in black and white:

## OP-09/OP-11 Features

| | TYP. | MIN./MAX. |
|---|---|---|
| • **Low $V_{OS}$** | 0.30 mV | 0.5 mV MAX. |
| • **Low offset current** | 8.0 nA | 20 nA MAX. |
| • **Low supply current (Total for all 4)** | 3.5 mA | 6 mA MAX. |
| • **Voltage gain** | 250K | 100K MIN. |
| • **Slew rate** | 1.0 V/$\mu$S | 0.7 V/$\mu$S MIN. |
| • **Matched positive and negative slew rate for low distortion.** | | |
| • **Bandwidth** | | 2.0 MHz MIN. |

## We make them match.

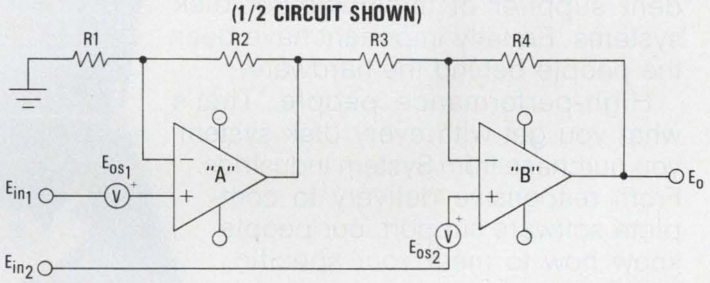
Another important advantage: we guarantee that all four op amps will match in terms of $V_{OS}$ and CMRR. Here's how we specify them:

## Matching Characteristics

| | | OP-09A/E OP-11A/E | | | OP-09B/F OP-11B/F | | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Units** |
| **Input Offset Voltage Match** | $\Delta V_{OS}$ | – | 0.5 | 0.75 | – | 0.8 | 2.0 | mV |
| **Common Mode Rejection** | $\Delta$CMRR | – | 1.0 | 20 | – | 1.0 | 20 | $\mu$V/V |
| **Ratio Match** | | 94 | 120 | – | 94 | 120 | – | dB |

**(Match exists between all four amplifiers)**

**DUAL INSTRUMENTATION AMPLIFIER 2 OP AMP DESIGN (1/2 CIRCUIT SHOWN)**




These matching dc characteristics should interest you. They reduce distortion, improve system performance, and simplify your design. But that's not all.

We've given all four op amps symmetrical positive and negative slew rates—an important thing to keep in mind for audio system design.

It's fair to say that the OP-09 and OP-11 are the most accurate, most advanced and the only **precision** quad op amps on the market. And they **are** on the market—available now, today.

Like to check one out? Be our guest. Just drop us a line on your company's stationery, telling us if you'd prefer an OP-09 (4136 pinout) or an OP-11 (148/4741 pinout). We'll be glad to send literature and a sample.

**Precision Monolithics Incorporated**
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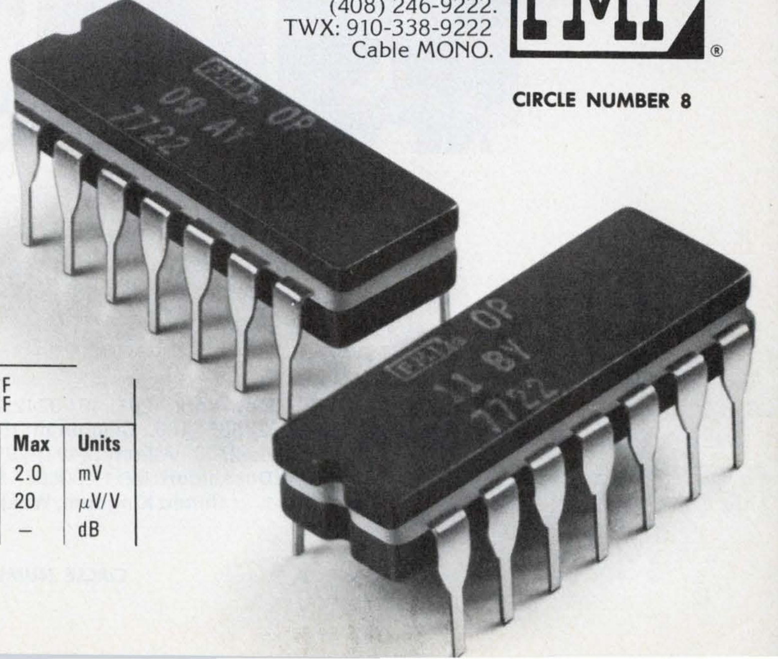
Cable MONO.

PMI®

**CIRCLE NUMBER 8**



# When you buy disk systems from us, you get a lot more than just high-performance hardware...

At System Industries, we take great pride in translating the latest disk storage technologies into high-performance hardware. But by itself, superior hardware would not have made us the world's largest independent supplier of minicomputer disk systems. Equally important have been the people behind the hardware.

High-performance people. That's what you get with every disk system you purchase from System Industries. From responsive delivery to complete software support, our people know how to meet your specific requirements.

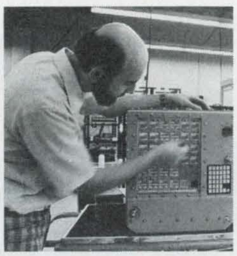
You can also add low price— the lowest in the industry for OEM-quantity purchases. Because we buy more disk drives than any other independent, we can afford to pass the savings on to our customers.

We believe the best business relationship is a mutually profitable one. That's why we're ready to help our customers become self-sufficient in handling their future disk storage needs. And that's why our customer base continues to grow rapidly.

We'd like to tell you more about our high-performance people and products by sending you "The Bit" — our quarterly newsletter. To receive your free copies, simply drop us a short note with your business card. Or phone your request to the System Industries sales/service office nearest you.

We make good disk drives work better, and we think you should know why.

# ...you get the support of high-performance people.

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CIRCLE NUMBER 9


CIRCLE NUMBER 11

# The new DAC standard. Analog Devices' complete 10-bit monolithic DAC.

# Less than a buck a bit.

You can pay at least twice as much for a 10-bit IC D/A converter and still not get the degree of accuracy and stability of our new AD561. Selling for less than $10, the AD561 sets a new standard of price and performance for the other guys to shoot for.

As for accuracy, the AD561 is guaranteed to ±½LSB max of 10-bits (or even ±¼LSB — and that's 11-bits). Monotonicity is guaranteed over the full operating temperature range. The excellent stability is made possible by a unique buried zener voltage reference and Analog Devices' proprietary thin film resistor process. And for settling time, there's nothing faster: less than 250ns for the worse case transition; that's fast enough to build a 5 $\mu$sec ADC. Current-to-voltage conversion with an op amp is direct and simple: trimmed application resistors mean no calibration trimmers are needed.

How did we achieve this breakthrough? With the industry's most advanced monolithic processing and our pioneering technique of laser wafer trimming. The kind of advances that have quickly pushed us to the top and made us the leading supplier of D/A and A/D converter components.

The AD561 joins another group of Analog Devices' pacesetters: a series of monolithic CMOS converters that also set new performance standards. At the same time they set a lot of microprocessor users free of analog interface problems. One is the 10-bit successive approximation AD7570 ADC. Another is the multiplying 10-bit DAC, AD7522, the only device that can be loaded in either parallel or serial modes.

And the AD561 joins the industry's 12-bit IC DAC standard, AD563.

Find out how you can cut in half the cost of your 10-bit IC D/A converters and still get true, 10-bit performance by writing for our data sheet. Contact Analog Devices, the real company in precision measurement and control.

**ANALOG DEVICES**

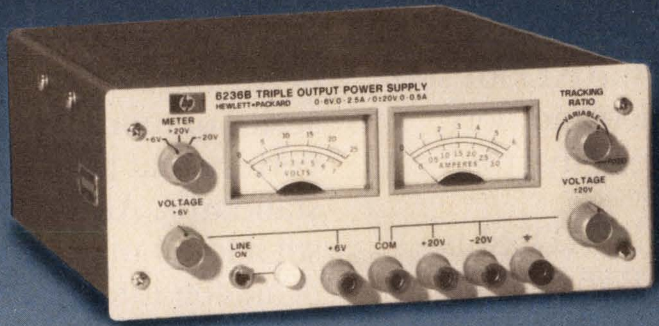
The real IC converter company.

**CIRCLE NUMBER 13**

Analog Devices, Inc., Box 280, Norwood, Massachusetts 02062 East Coast: (617) 329-4700, Midwest: (312) 894-3300, West Coast: (213) 595-1783, Texas: (214) 231-5094, Belgium: 031 38 27 07, Denmark: 02/84 58 00, England: 01/94 10 46 6, France: 686-77 60, Germany: 089/53 03 19, Japan: 03/26 36 82 6, Netherlands: 076 14 21 50, Switzerland: 022/319704 and representatives around the world.

# You Can Do More with HP Microprocessor Power Supplies...

# BECAUSE YOU GET TRIPLE OUTPUT!




## for the design stage...

of your microprocessor system, HP's compact, low cost lab power supplies offer more. For example, Models 6236B and 6237B offer three adjustable output voltages. Model 6236B covers 0 to 6V at up to 2.5A. Model 6237B is 0 to 18V at up to 1A. Both have plus and minus outputs of 0 to 20V that track within 1%, or you can switch to a variable tracking mode which allows the negative output to be separately set lower than the positive providing three different output voltages. There are no turn-on/off voltage transients so your circuit is protected against damage. Both models are designed to make development work with microprocessors easier.


## for the end product...

where you can feature a triple output OEM Modular Supply specifically designed for powering microprocessor systems. Model 62312D provides three isolated, independently adjustable outputs. The main output is rated at 4.75V to 5.25V at 3A. Two others each range from 4.75V at 0.38A to 12.6V at 0.6A. Other standard features to help optimize your microprocessor design include an internal AC line fuse, fixed foldback current limit, over voltage protection on the main 5V output, remote programming terminals for margin testing and much more. Write for complete details or contact your nearby HP field sales office.

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1507 Page Mill Road, Palo Alto, California 94304

For assistance call: Washington (301) 948-6370, Chicago (312) 255-9800, Atlanta (404) 434-4000, Los Angeles (213) 877-1282

21701

CIRCLE NUMBER 14

## Codec converts with ladder of Cs, not Rs

The first telecommunications coder-decoder set to use switched capacitors instead of resistors in a/d and d/a conversions can maintain accuracies of one in 8000. The codec also takes advantage of fundamental CMOS properties. Furthermore this accuracy is obtained without the need for laser trimming.

Slated to be second-sourced by Nitron, Cupertino, CA, this single-line, logarithmic companding codec from Siliconix, Santa Clara, CA, has already proved useful to telephone companies converting to digital networks. They set the codec's performance specifications to fit their needs for PCM voice transmission. Moreover, "because of the large-volume demands of the telephone industry, the designer who builds single-line codecs into his equipment can be assured of a wide choice of types, and low prices from many viable suppliers," comments Fred Glynn, a telecommunications consultant with the San Francisco Research Group.

But the Siliconix codec may find uses in other audio fields as well, since it crams into 8-bit words the same high signal-to-noise ratio and speech quality of a 13-bit conventional a/d.

Requiring no external components, the codec consists of two CMOS chips in 14-pin DIPs. The DF 331 coder chip accepts a voice waveform, band-limited by filters to 4 kHz, does a/d conversions at 8-kHz under control of an external sample clock, and outputs an 8-bit PCM word for each sample. The DF 332 decoder accepts 8-bit words, performs d/a conversions, and outputs the reconstructed analog wave shape via an on-chip sample-and-hold amplifier.

In standard telephone applications, the output bits of 24 DF 331s are interleaved (multiplexed digitally) to form a single 1.544-Mbit/s PCM bit stream. Digital multiplexing is accomplished by tying the open-drain outputs of all 24 coders to the same pull-up resistor, and sequencing the coders' sample clocks from separate taps of a shift register. The PCM bits are sent to the distant location, and distributed to 24 decoders.

Within the codec, logarithmically weighted groups of 256 identical 0.7-pF capacitors provide a 16-segment piecewise-linear transfer characteristic that assigns small quantizing steps to low-signal amplitudes and progressively larger steps to high-signal amplitudes.

Right now, the DF 331 and 332 follow the $\mu$-225 law, the standard companding characteristic in the United States. The European standard A-law will be incorporated into later codecs.

Siliconix is now shipping samples of the $\mu$-law codec, and plans to deliver in volume by year-end. Similar A-law codecs are scheduled for sampling by year-end and production in the first quarter of 1978. Both versions will be second-sourced by Nitron. Siliconix will provide masks, process information, and technical assistance to McDonnell Douglas division, which expects to be producing both $\mu$-law and A-law units in volume soon after Siliconix. Prices will be below $10.

### Small 3½-digit multimeter: the lowest-cost of the low

At $49.95, the PDM35 is not only the least expensive 3-1/2 digit multimeter but also half the price of the previous record holders. Measuring a scant 6 × 3 × 1-1/2 in., the Sinclair Radionics multimeter is styled much like the firm's handheld calculators.

Four ranges for ac and four ranges for dc voltage measurements are offered, as well as six direct-current ranges and five resistance ranges.

Part of the reason for the PDM35's very low price is that it has no circuitry to measure ac amperes, according to John T. Nicholls, head of Sinclair's instrument division. However, it does have LSI digital circuitry, discrete BiFet amplifiers instead of single-chip a/d converters, and thick-film resistance ladder networks—all of which help bring down the cost, while hiking reliability.

Until now, the lowest-priced 3-1/2-digit instruments went for just under $100 and came from, among other companies, B&K Precision, Chicago, and Sinclair, whose DM2 is priced at $99.

The PDM35 is the first in a new series of DMMs Sinclair plans to introduce over the next six months. On tap is a 4-1/2-digit multimeter with automatic range selection and a price tag of around $200.

The PDM35 operates either from throwaway 9-V batteries or from an optional ac adapter. Its rated accuracy is ±(1% of reading +1 count) on dc voltage and current ranges, ±(1% of reading +2 counts) on ac voltage ranges, and ±(1.5% of reading +1 count) on resistance ranges.

Resolution is 1 mV dc, 1 V ac, 1 nA dc, and 1 Ω. Polarity is selected automatically, and overrange (beyond 1999 counts) is indicated by horizontal bars on the most-significant digits and zeroes on the other digits.

Radionics has also introduced the first programmable calculator to use a single chip. Advanced mathematical and scientific capabilities are combined with a 36-step keyboard-entry program memory in a handheld unit about the size of a king-sized pack of cigarettes. At $29.95, the Cambridge Programmable can handle programmed calculations in math, finance and statistics, physics and engineering, and electronics, as detailed in a four-book, 294-program library ($9.95). Original programs can also be developed.

### Chip can interface micro with bus—all by itself

Making and using IEEE 488-compatible devices will soon be a lot easier.

A new chip can easily interface a microcomputer to the IEEE 488 bus without the expensive controllers currently used.

The 68488 from Motorola, Phoenix, AZ, is a semiconductor implementation of the talker/listener state diagram of the IEEE bus, and can be used alone as long as logic circuitry is available to control it. But a better way to use it, according to Motorola application engineer George Nelson, is to hook it up to a 6800 or 6802 microprocessor.

The 68488 provides a microprocessor with bus information when addressed. but if the chip recognizes that an address is not its own, it ignores the address and leaves the micro undisturbed. Otherwise, it informs the micro that it is being addressed and tells it to go into a talk or listen mode.

The mode selected depends on the 7-bit address code sent. Five bits are actually used to supply address information, while the other two are used to designate the mode.

The 68488 decodes these two additional bits and uses the information to control bidirectional transceivers, which handle the flow of data to and from the bus.

The 68488 can be programmed for a particular address by entering binary data via external switches connected to three-state logic devices. When a read signal comes from the micro, the three-state devices are enabled and the data presented by the switches are read into the chip. This address information will remain in the 68488 memory until it is changed or until power is removed from the device.

The first applications of the new 488 interface IC will probably come from Motorola. Current plans call for the chip to be included in an updated version of the company's 6800 evaluation board. The chip will also be used in an IEEE-compatible DVM board and an IEEE-compatible DMM board.

The 68488 is currently being sampled and will be available off the shelf in December. The price in 100 quantities will be $13.75.

## μP packs mini power but stays Z80-compatible

A 16-bit microprocessor, optimized for compiler-generated code, will be able to match a PDP-11/70 minicomputer's processing power. Not only that, but the Z8000, being developed by Zilog, Cupertino, CA, will be assembly-language compatible with the Z80 8-bit microprocessor.

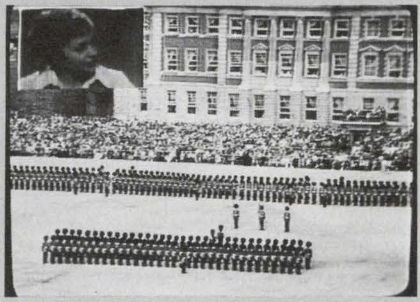
Programs that run on a Z80 will be able to run on the Z8000, providing the assembly code is available, states Ralph Ungerman, Vice President. A special translator program is being developed for code conversion.

The Z8000 will have an addressing range of millions of bytes—when used with a special auxiliary circuit. However, since it will be housed in a 40-pin DIP, the basic addressing range of the μP will be 65,536 words, assuming a 16-bit address bus.

But since the processor is designed to handle compiler generated code, the memory-expansion circuit will probably have to be used frequently. Compiler code tends to be quite lengthy and can easily require more memory than the basic addressing range can handle.

Instruction capabilities have not been fully defined as yet, but the shorter instructions are expected to execute in well under 1 μs. Typical high-level instructions will include hardware multiply and divide.

## Now you can watch two shows at once



The latest advance in remotely operated color television receivers is a second channel-monitoring capability, which is being offered in sets just introduced by Barco Electronics of Belgium.

Using charge-coupled devices, Barco engineers have been able to design a system that inserts a miniature image of the program presented on a second channel in the top left-hand corner of the program being viewed. A viewer simply presses the CCD mode switch on the remote control unit and then punches in the number of the second channel to be monitored.

Two receiver sections are used to produce the individual video signals. The second video signal is then read into two charge-coupled devices, which reduce the bandwidth from 5 MHz to 1.6 MHz. By reading the signal out of the CCD at a three-times-faster rate, the 5-MHz bandwidth is restored.

Read-in and read-out operations to the CCD are synchronized by the field and sync pulses of the main video signal. As a result, the two video signals can be combined and displayed as one on the TV screen.

Another development from Barco is what is touted as the world's first worldwide color television receiver. Called the Seagull, the receiver can receive all color systems, including PAL, PAL M, PAL N, SECAM H, SECAM V, NTSC 4.43 and NTSC 3.58. The set's power supply accommodates 220-V, 50-Hz and 110-V, 60-Hz power sources.

In the works is a version of the Seagull that will automatically examine an incoming TV signal and activate the appropriate decoding circuitry.

## Plastic insulation is safer than asbestos

A new low-cost, high-temperature plastic insulation eliminates the hazards of handling asbestos-coated wire when fabricating and assembling the wiring for high-volume applications like electrical appliances.

EXL-150, a tough, cross-linked polyolefin insulation developed by Prestolite Wire Co., Port Huron, MI, can not only be handled more easily, but it also resists abrasion better than asbestos and another high-temperature insulation, silicone. EXL-150 is easier to terminate and mark than asbestos, which is soft and easily damaged, and difficult to mark for identification.

Prestolite wire insulated by EXL-150 costs only slightly more than asbestos-coated conductors, which are the lowest cost, but less than silicone-insulated wire which costs one and a half times as much as asbestos.

EXL-150 is rated at 150 C by Underwriters' Laboratories. To attain this rating it has passed accelerated aging tests at 180 C for five days followed by 158 C for 90 days.

## Solar energy may power rendezvous with comet

Solar energy may be the ultimate source of fuel for a space ship that will rendezvous with Halley's comet in 1986. If NASA scientists have their way, solar energy will be used to produce electricity to power mercury-ion engines, which will provide the actual motive force for the spaceship.

Ion rocket engines and solar-sail systems had been investigated for several years. But the former was finally chosen to be the source of power for interplanetary shuttles used in the 1980s and beyond. The ion drive was chosen primarily because it is less risky to use and has greater growth potential, according to Dr. Kenneth L. Atkins of the Jet Propulsion Laboratory in Pasadena, CA, and head of the propulsion study team.

The ion-drive spacecraft will be ready for launching from the Space Shuttle in late 1981 or early 1982, but probably won't be used for any major application until the anticipated rendezvous with Halley's comet.

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Average Rectified Current @25°C:
25 & 10mA
Static Forward Voltage, 10mA @25°C:
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Reverse Recovery Time (Max.): 300ns
Case Size (Max.):
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Average Rectified Current @55°C in Oil: 200mA
Static Forward Voltage, 100mA @25°C: 12V
D.C. Blocking Voltage @25°C: 7500 & 10,000V
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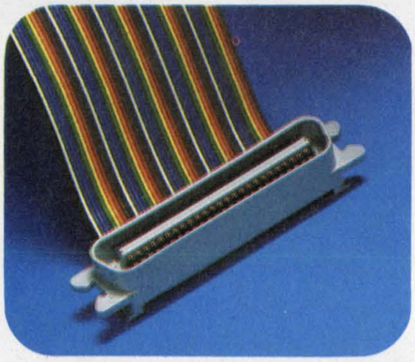
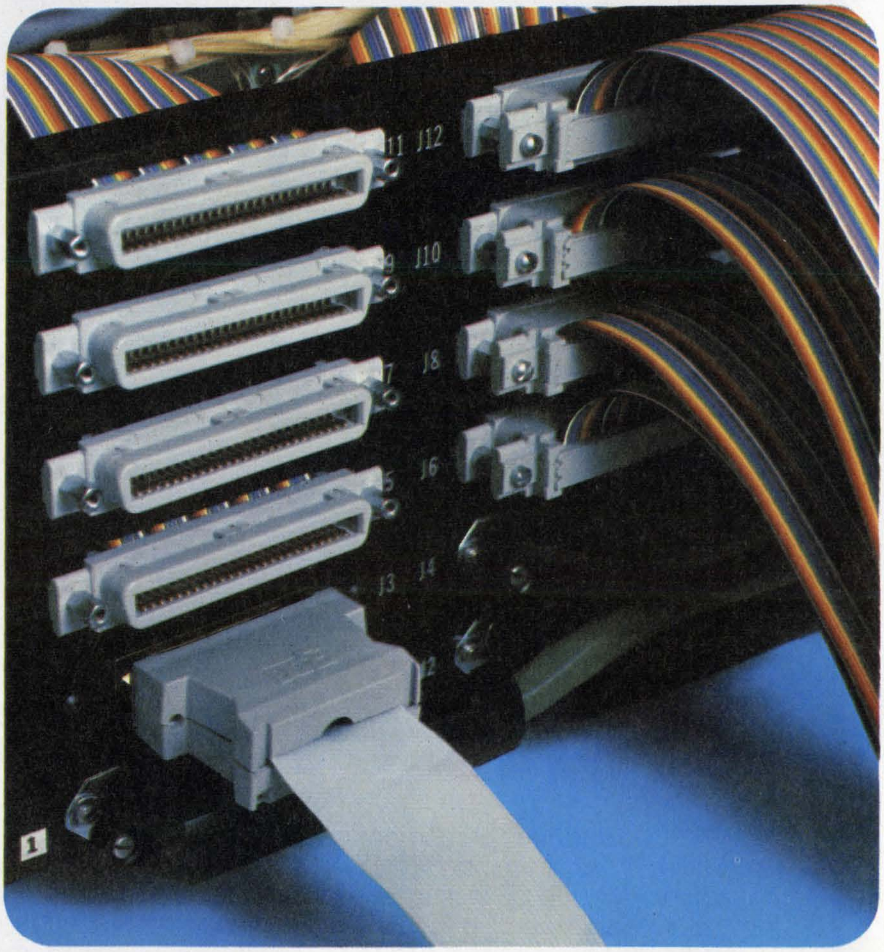
CIRCLE NUMBER 15

# Now you can mass terminate with ribbon connectors...



Here's another industry first from 3M that's good news for you: the Scotchflex brand Delta Ribbon Connector System for intra-system or I/O interconnections. In computer applications, in telecommunications, in any place or any way you want to use flat cable and ribbon connectors, this versatile system can do the job at sharply reduced assembly time and labor costs.

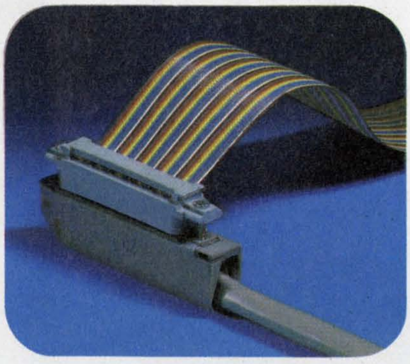


With Scotchflex Delta Ribbon Connectors, no stripping, soldering or other wire preparation is necessary. You can mass terminate a parallel-lay 50-conductor (25-pair) .0425″ center-spaced flat cable in less than 30 seconds with one step. That's about ten times faster than other available methods. And thanks to 3M's field-proven, gold-plated berylium copper U-contacts, all connections are reliably corrosion-resistant and gas-tight.

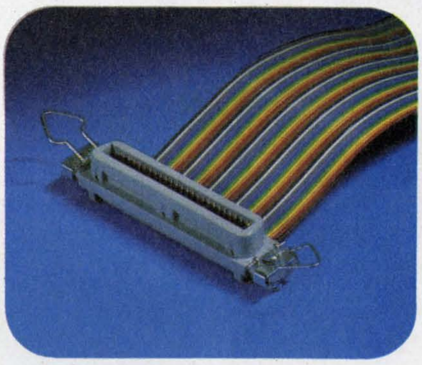
After termination, there are more savings. You can buss from point to point without disassembling or breaking existing cables. And there's no need to redesign or rework first generation components. This Scotchflex system mates perfectly with all standard miniature ribbon connectors.

# ...in 30 seconds or less!

There's no costly investment to make in equipment or training. All you need are two locator plates and the Scotchflex manual or pneumatic assembly press. You can start mass terminating assemblies quickly and economically. No special operator skills are required. Rejects and reworking are greatly minimized.



The Scotchflex Delta Ribbon system includes 50-position male and female connectors, plus appropriate bail mount, screw mount and jack screw kits, strain relief clips and dust covers. Color-coded flat cable is available in parallel-lay conductors #28 AWG stranded or #26 AWG solid.



Only 3M offers you so broad a range of flat cable and system components. A nationwide network of stocking distributors. Best off-the-shelf availability. Proven performance. And the unmatched experience of the people who pioneered mass terminations.

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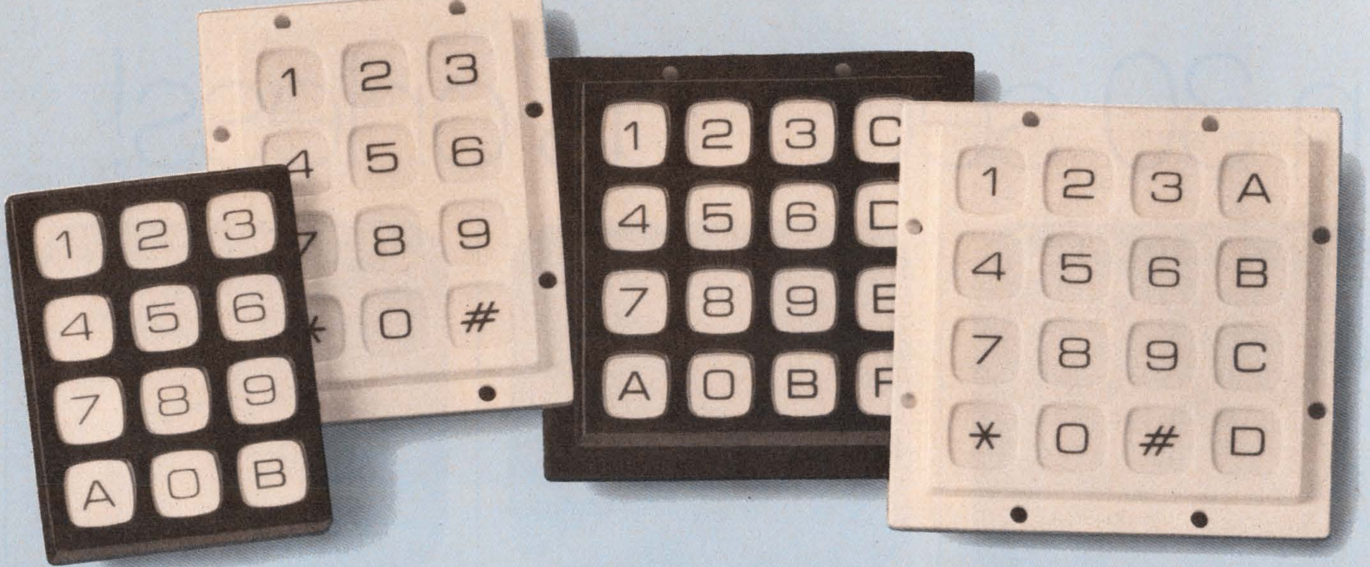
3M COMPANY

See our catalog in EEM, page 2256

CIRCLE NUMBER 18

# CENTRALAB MONOPANEL KEYBOARDS

# The TOUCH Switch System ...



# ...Now available from Centralab Distributors

You'll meet keyboard requirements faster, easier and at surprisingly low cost with MONOPANEL — Centralab's touch-sensitive keyboards. They help solve design problems, simplify and reduce cost in assembly and production and give your product a competitive edge in appearance, design and function. And now, 16 standard keyboards are in stock for immediate delivery from Centralab Distributors.

Don't confuse MONOPANEL with other keyboards. Even though they're priced about the same, MONOPANEL keyboards are superior in construction, reliability, quality and value. First of all, they're backed by Centralab's more than half-century of experience in switch manufacturing. They're 100% tested. They're tough — designed for long, trouble-free life; have no mechanical parts to wear out. And they've been proven in use. The basic Monopanel key switch has undergone more than 70,000,000 switching cycles without failure.

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For complete product and price information contact your Centralab Distributor. Or, for the name of your distributor, call Centralab Distributor Products, Milwaukee (414)228-2911.

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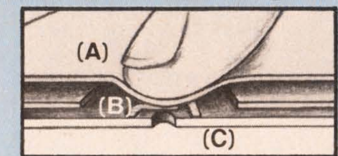


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MONOPANEL is a thin, light, flat, front panel subassembly with micro - motion touch switches already mounted and interconnected. Each MONOPANEL is a multilayer assembly containing **(A)** a flexible, tough, moisture proof polyester membrane with graphics and flexible conductors screened upon the rear surface; **(B)** a thin spacer with holes for each switch provides an .007" air-gap; **(C)** a circuit board with switch circuits on its face, joined by plated through-holes to interconnections on its back.

The basic switch closure is momentary, normally open. Light touch pressure (2 oz. typical) on the smooth, flexible front panel closes the contact. Releasing pressure allows the front panel membrane to return, opening the contact.

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CIRCLE NUMBER 19

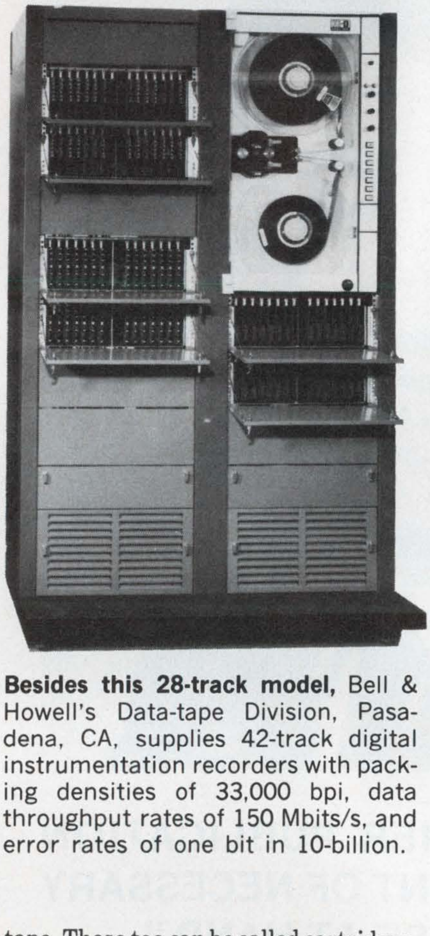
# Digital tape recording is denser, but standardization isn't standard

Digital recording on tape, whatever its width, is getting denser. And then some. Quarter-inch-wide tape in cartridges has shot up to 6400 bits per inch. Half-inch reel-to-reel drives are running at 6250 bpi and full-inch tape for instrumentation is packing 33,000 bpi and 42 tracks across the head. But while density increases, the near-term likelihood of standardization decreases, particularly for quarter-inch cartridges.

Just as the American National Standards Institute was about to come up with a standard format for 3M quarter-inch-tape cartridges, IBM's introduction of the 5100 desktop computer upset the apple cart. The 5100 uses the 3M tape cartridge, but not the ANSI-proposed standard data format. So the tape industry's elation at having the "Giant of Armonk" ratify its standard was simultaneously dampened by the knowledge that IBM data formats almost automatically become industry standards.

Two other firms have introduced "nonstandard" 6400-bpi 3M tape drives. For example, the Model 3400 drive announced by Data Electronics of Pasadena, CA, "is used almost exclusively for backing up Winchester disc drives," according to marketing manager Sam Thompson. The unit reads and writes data at 30 inches per second and moves tape for rewind or search at 90 ips. A similar device is the Loadstar 6400-bpi drive from Microdata, Irvine, CA.

(The term "cartridge" was introduced by 3M to differentiate its belt-driven unit from Philips' "cassette," which uses a pinch roller. They both shuttle a length of tape from one reel to the other. The 3M cartridge should not be confused with those transport schemes based on an endless loop of tape. These too can be called cartridges, as with Tri-Data's "Cartrifile" unit.)



**Besides this 28-track model,** Bell & Howell's Data-tape Division, Pasadena, CA, supplies 42-track digital instrumentation recorders with packing densities of 33,000 bpi, data throughput rates of 150 Mbits/s, and error rates of one bit in 10-billion.

### Half-inch goes full-cycle

Meanwhile, reel-to-reel half-inch tape drives are growing smarter and denser at the same time. Today, these tape drives, which used to run at 1600 bpi, can now run at 6250 bpi—and correct multiple-track errors without processor intervention. This involves adding an intelligent data formatter/checker at the front end.

For 6250-bpi recording, data are first accepted into the formatter's buffer memory, where partitioning and expanding take place, then divided into 4-byte subgroups and 8-byte full groups.

Each data byte gets a parity bit. Then an error checking and correction (ECC) byte is generated and imbedded in the data stream following each of the 4-byte subgroups. (The ECC is generated cyclically on the four associated data bytes plus parity.)

When reading, the formatter looks at an 8-byte full group and the two ECCs. Because of the mathematics involved, it can detect and correct both single and double-bit errors without the help of the processor.

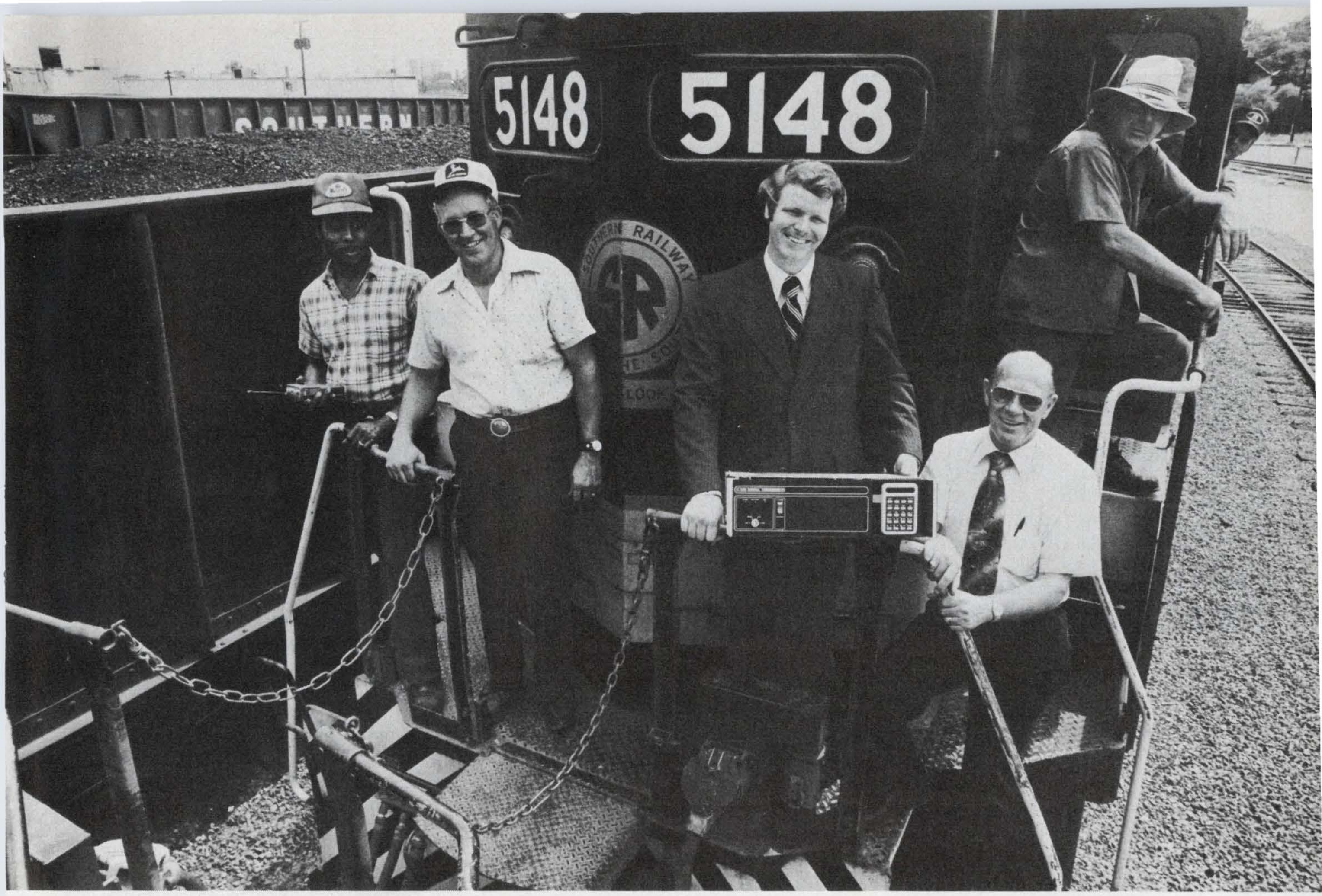
This technique, called "group-coded recording" (GCR), comes from IBM, so of course it is IBM-compatible. And, not too surprisingly, it has been accepted as an ANSI standard.

The half-inch drives' increase from 1600 bpi to 6250 bpi makes phase-encoded recording unsuitable. Instead, the earlier nonreturn-to-zero (NRZ) recording technique must be used. Phase-encoded recording uses either one or two flux reversals per bit time. At 6250 bpi, flux-reversal density resulting from normal data streams exceeds the maximum density of the tape (see box). Today's magnetic tape can only support about 9500 flux reversals per inch before the signal-to-noise ratio degrades to the point where the tape cannot be read without excessive errors.

Even though 6250-bpi tape drives use NRZ recording, they retain the benefit of self-clocking by coding the data so that no more than two consecutive ZEROs are allowed in the data stream. The "read" clock need only adjust to three frequencies that correspond to a stream of ONEs, alternating ONE-ZEROs or two ZEROs and a ONE.

Group-coded recording accommodates the consecutive-zero restriction and formats data so that multiple-track errors can be detected and corrected. This is a quantum jump over simple parity checking and other data integrity schemes that would demand the host processor's attention.

**Dick Hackmeister**
Western Editor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5148

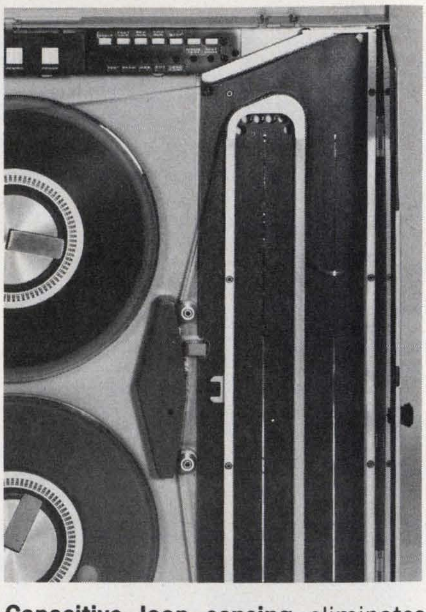
## Flux Reversals

Flux reversals are the key to digital recording, no matter which recording method is used. Bits (ONEs and ZEROs) are encoded with flux reversals on the tape as a function of the magnetic polarity (direction) of small, contiguous lengths of tape.

In earlier return-to-zero recording, a ONE was encoded as a period of flux reversal (opposite magnetization) against a background of all ZEROs. As the tape was moved across the fine coils of wire in the read head, flux reversals at the leading and trailing edges of the ONE would induce small voltages in the detector coils. One of these voltages would be amplified to a ONE.

Since with RZ recording the trailing edge of the flux-reversed segment was redundant, nonreturn-to-zero recording soon became popular. (Any flux reversal, in either direction, indicates a ONE; a ZERO manifests no indication.) But since there was no time reference, NRZ recording did not resolve the problem of dealing with a string of consecutive ZEROs—which Zero was which?

Phase-encoded recording solved the problem. At every bit time, at least one flux reversal occurs—one reversal indicates a ZERO, two reversals, indicate a ONE. The flux reversal is in one direction for a ZERO, another for a ONE. This scheme provides a self-clocking mechanism that can track a string of repetitive bits, no matter how long it is.



**Capacitive loop sensing** eliminates the "steps" that occur with photodiode sensing. A flexible, Mylar-backed conductive film is exposed to the back of the vacuum column (a thin vertical line). In this Model 9300, 125-ips, 6250-bpi tape drive from Kennedy, the magnetic tape, with atmospheric pressure on one side of the loop and a vacuum on the other, causes the conductive film to be deformed for a length equal to its position in the vacuum-buffer column. A servo control system responds to capacitance changes, which in turn indicate loop position.

Still, the 6250-bpi drives are not all that popular.

"The cost of developing a 6250-bpi tape drive is over $1-million," according to Steve Arnaudoff, marketing manager for Kennedy Tape Co., Altadena, CA. "And all that R&D would go out the window if semiconductor firms were to introduce LSI formatter chips." Meanwhile, all tape-drive eyes are on the Model 1900 6250-bpi GCR drive introduced by Storage Technology Corp. of Louisville, CO, at the NCC last June. If it is well received, a lot more 6250-bpi drives could hit the marketplace.

### New uses for 1-in. recorders

At the same time, full-inch digital instrumentation recorders, nudged forward by spaceborne and geophysical applications, now pack in up to 33,000 bpi and 42 tracks across the head. In one geophysical application, searching for oil, huge amounts of raw data need to be accumulated and burst into a host processor. Standard 1-in. instrumentation recorders exist with data-throughput rates up to 150 Mbits/s and error rates down to one bit in 10 billion—for an entire 2-mile reel of tape.

Data protocols and intelligent formatting are the key to these low error rates. The 1-in. recorders format the data somewhat like data-communications protocols—they use synchronizing words with particular bit patterns and differentiate them from raw data.

In Bell & Howell's high-density system, for example, a sync word consists of 10 repeated ONE-ZEROs followed by ZERO-ONEs. The double 00 line in the center is made unique, so it cannot be replicated by data because of parity differences.

At 33,000 bpi, each bit takes up a mere 30 microinches along the tape. Dynamic and static skew can be problems, so the Bell & Howell system uses the sync words to monitor and correct for it.

Because the short "data wavelengths" in the ferrite medium of data-recording tapes are substantially smaller than the thickness of Mylar backing, the problem of noise due to "print-through"—overlapping layers of tape magnetizing each other—is reduced to nil. Print-through is reduced even more because high-density systems do not saturate the ferrite medium as other technologies do. The B-H curve in the Bell & Howell system, for example, is driven to no more than 10% of saturation.

Supporting bursts of very high-speed data from a satellite or from an unmanned geological monitoring site, requires a high rate of data throughput. Under certain conditions, time is compressed by high-density systems a factor of 80:1 or more.

If 150 Mbits/s is too fast for a host computer, data can be down-translated by a factor of 64 or less.■■

## For more information . . .

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Erick Ringjob

Tri-Data, Inc.
800 Maude Ave.
Mountain View, CA 94043
(415) 969-3700
R. J. Hlava

# Spectrum analyzer on a chip? Analog CCD module comes close

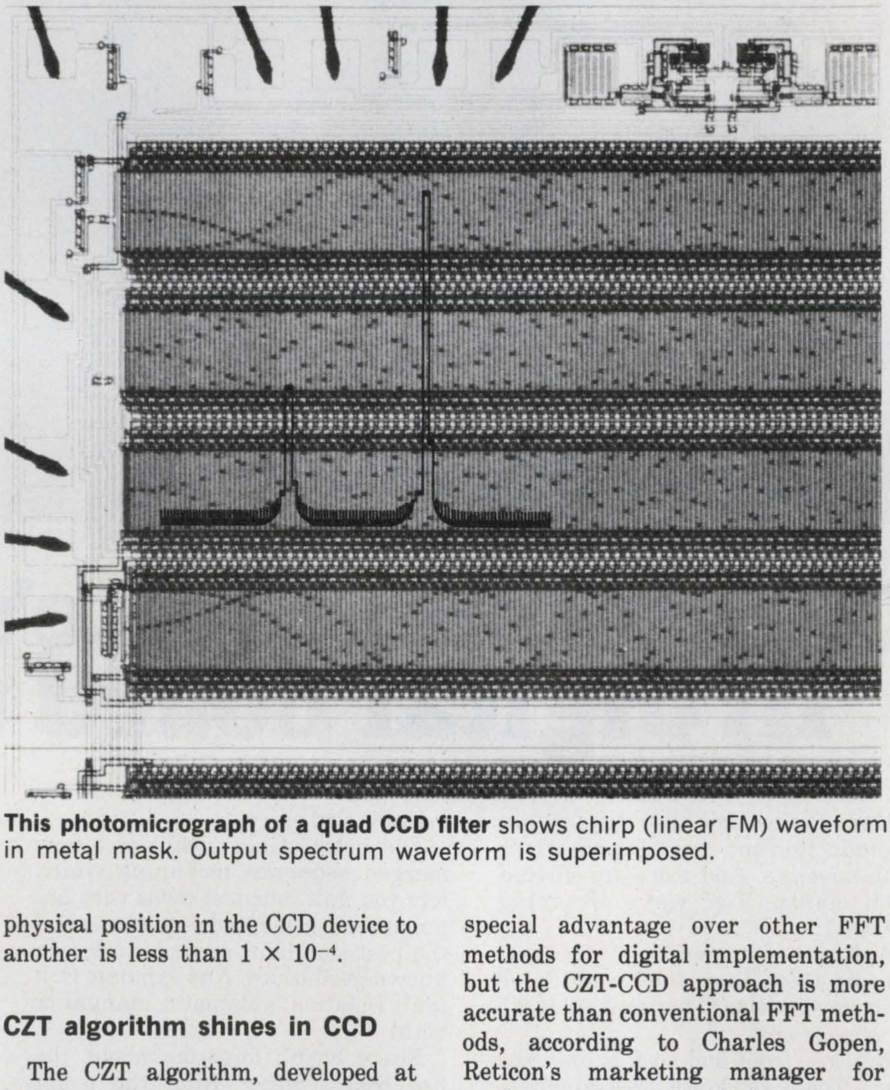
By computing Fourier spectra faster than a large-scale digital computer, a new analog CCD chip makes it practical to design spectrum analysis into bandwidth-compression and speech-recognition designs for commercial and consumer devices. So says John Rado, president of Reticon Corporation of Sunnyvale, CA. Reticon's Chirp Z-Transform (CZT) transversal filter chip, the R5601, is the first device available to the OEM that can compute Fourier transforms economically.

"Our CZT-CCD approach cuts size, weight, and power dramatically, perhaps in some cases by 50 to 1," Rado explains, pointing to a two-board spectrum analyzer module, built to demonstrate the use of the chirp chip. "This little module, taking up 80 square inches, gives you all the same answers as a digital Fourier analyzer that uses a dedicated minicomputer and half a rackful of other gear." And while the latter group takes only six microseconds per data point, Rado adds, the system costs $40,000. The Reticon modules work just as fast, but for around $800.

Performing many precise analog multiplications simultaneously in real time, the R5601 chip converts 512 time samples to 256 spectral lines. It does the convolution calculations for both discrete Fourier transforms (DFTs) and power spectral density plots (PSDs), starting from a sampled-data analog input with a dc-to-50-kHz bandwidth.

The chirp chip boasts a 70-dB dynamic range, peak-signal-to-rms noise, and can separate two adjacent-frequency signals that are 50 dB different in amplitude. Total harmonic distortion is less than 1%. Moreover, the average inefficiency of transferring the analog charge from one physical position in the CCD device to another is less than $1 \times 10^{-4}$.

**Dave Barnes**
Western Editor



**This photomicrograph of a quad CCD filter** shows chirp (linear FM) waveform in metal mask. Output spectrum waveform is superimposed.

### CZT algorithm shines in CCD

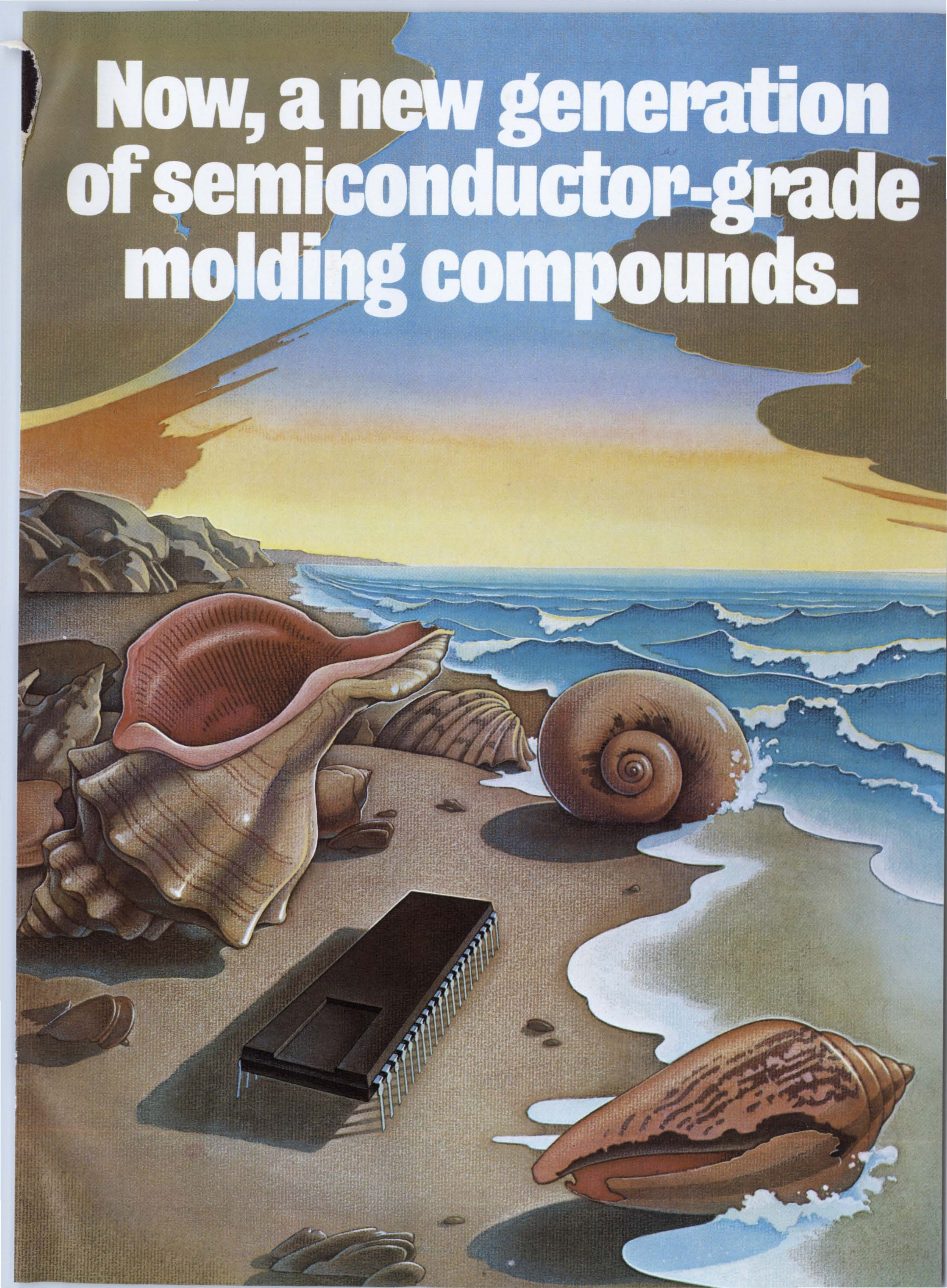
The CZT algorithm, developed at MIT in the late 1960s, is named for the chirp, a linear FM waveform that rapidly sweeps from low frequencies to high. The algorithm calls for premultiplying the signal by the chirp waveform, then circulating the product in the chirp filters, as shown in the block diagram. For PSD, the outputs of the filters are squared and summed. But for the actual Fourier coefficients for magnitude and phase, the outputs are postmultiplied by another chirp waveform.

The CZT algorithm alone has no special advantage over other FFT methods for digital implementation, but the CZT-CCD approach is more accurate than conventional FFT methods, according to Charles Gopen, Reticon's marketing manager for analog products. In digital Fourier analysis, the errors in calculation increase as the square-root of N, the number of samples, he explains. But most of the CZT-CCD errors are independent of N.

"At 512 points," says Gopen, "this system with its 9-bit tap-weight precision is more accurate over-all than a digital FFT system with 13 bits."

Multiplying DACs do the premultiplication, getting their chirp-

*(continued on page 34)*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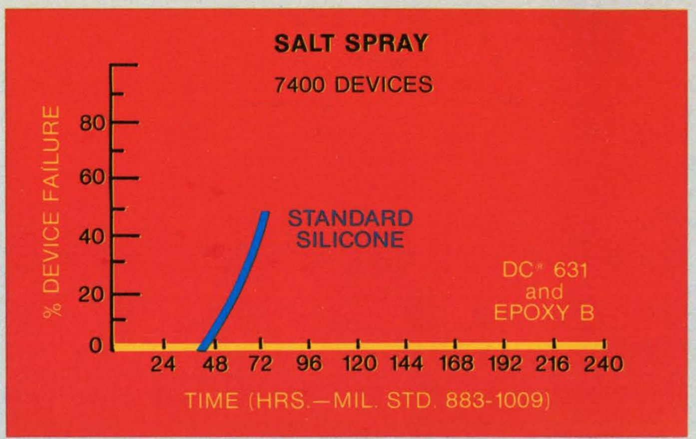


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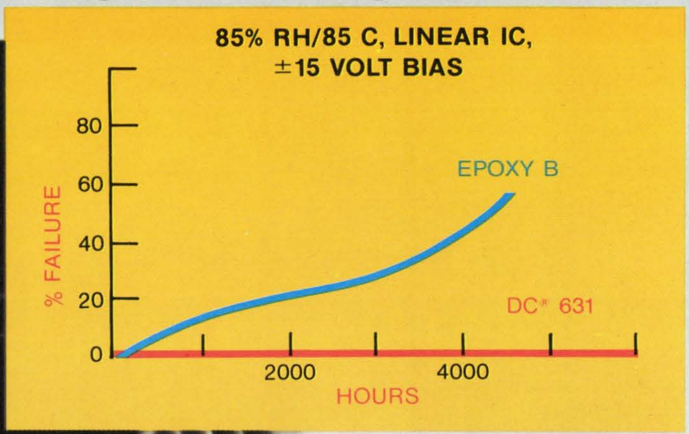


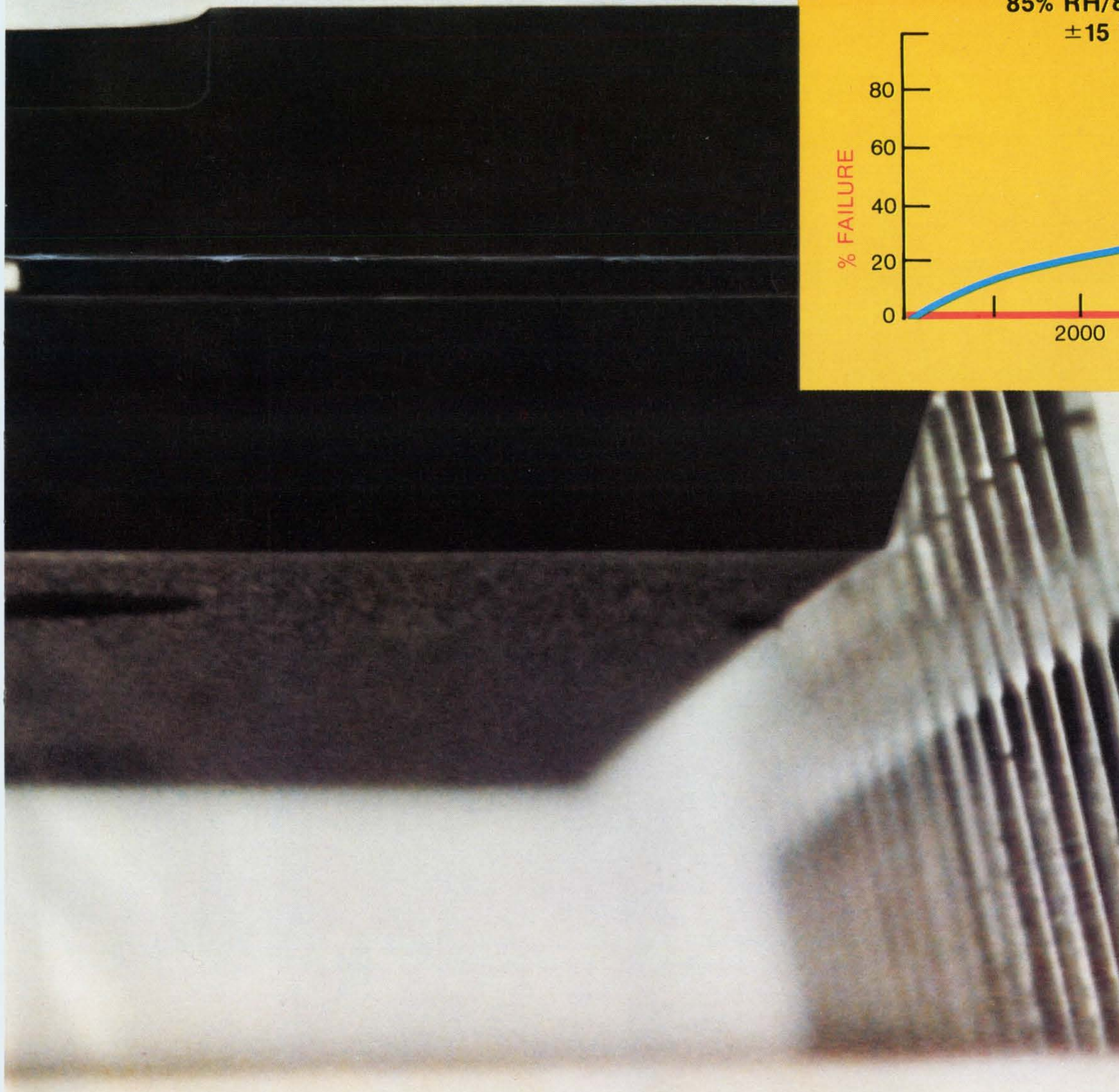

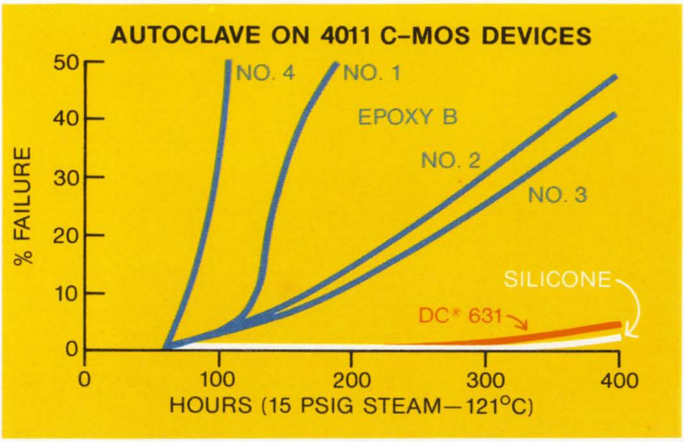


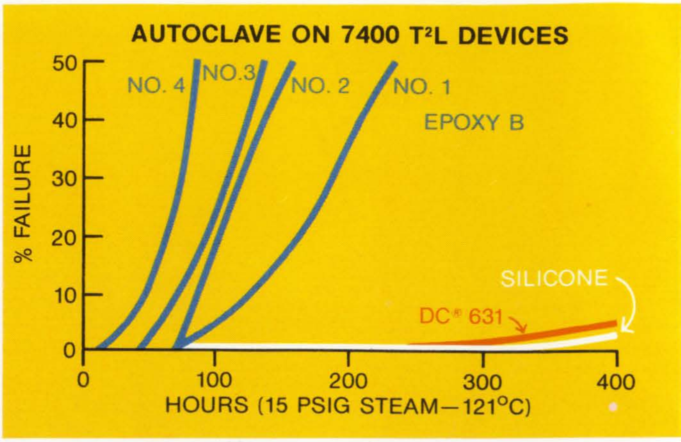


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CIRCLE NUMBER 24

(continued from page 32)

waveform values from ROM storage. All the pre and postprocessing circuits are available on the CZT prototype module.

Although the R5601 chip is designed for sampling rates from 500 Hz to 2 MHz, the CZT module is set up just for 100-kHz operation. Or it can be controlled by an external signal of up to 200 kHz.

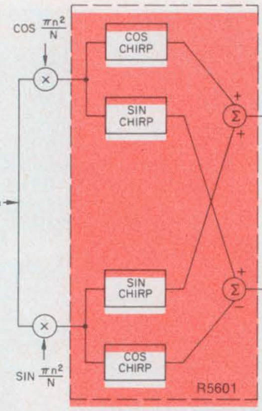
### Quad-channel chirp chip

The R5601 chip itself is a surface-channel CCD split-electrode filter, in which analog charge packets are shifted along by a four-phase clock. It is packaged in a standard 22-pin DIP, and requires standard MOS-level clocks.

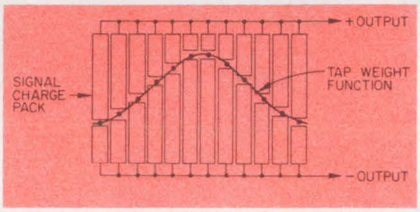
As with any CCD, digital or analog, mobile minority-charge carriers are stored in depletion regions under pulsed electrodes. The charges move in the direction dictated by the clocks, and the sampled signal moves down what amounts to an analog delay line.

Transversal filters, a fairly recent blossom in the CCD garden, are formed by splitting the pulsed electrodes. The location of the split is chosen to form capacitors whose size is correctly related to the tap-weight function. As the sampled analog signal moves down the line, each packet of charge introduces a current proportional to the product of its tap weight and its signal amplitude. The common connection between electrodes sums these currents, and the basic convolution calculation —summing many products—is accomplished.

Transversal filters can be made with some impressive specifications, such as




**A CZT (chirped-Z transform) algorithm** is implemented with external components in addition to the four transversal chirp filters of the R5601.




**This split-electrode structure** forms capacitors that hold the tap-weight function. Analog charges induce product currents that are summed and fed to differential amplifiers.

linear phase response, 1-MHz sampling rate, 100-dB/octave skirt steepness, and stopband rejection of 50 dB or more. For the CZT application, the tap-weight values are produced on the metal mask with an accuracy of ±8 bits, and the complex convolution is performed by multiplying the input samples by these chirp-related tap weights.

Two types of chirp chips are available, the R5601-1 with linear-chirped waveforms, and the R5601-2 with the same function multiplied by a Hanning window function. With the Hanning function, energy leakages into adjacent spectral lines are reduced. But this technique is used only in power spectral density applications, where phase information is not required. As a result, the 5601-1 can do either the total discrete Fourier transform or the PSD, while the 5601-2 can do only the PSD. Both devices, however, contain four 512-tap split-electrode transversal filters, with two sine chirps and two cosine chirps.

Each R5601 chip customer is required to buy at least one complete CZT module which requires only dc power to operate. The Reticon module is priced at $600 including documentation, but without the CCD device. Either type of R5601 chirp chip costs $675 in unit quantity, or $265 in quantities of 100 and up. The availability of modules and chips is immediate, for sample quantities.

As new as the CZT-CCD capabilities are in the OEM market, the product is not an untried, unprecedented design. Reticon has been active for several years in producing related devices.

But the direct forerunner of the R5601 was developed by Texas Instruments under U.S. Navy contract. Technical contributions came also from GE, RCA, Bell Labs, and MIT (see *IEEE Journal of Solid-State Circuits*, Vol. SC-11, No. 1, Feb., 1976, pp. 75-84.).

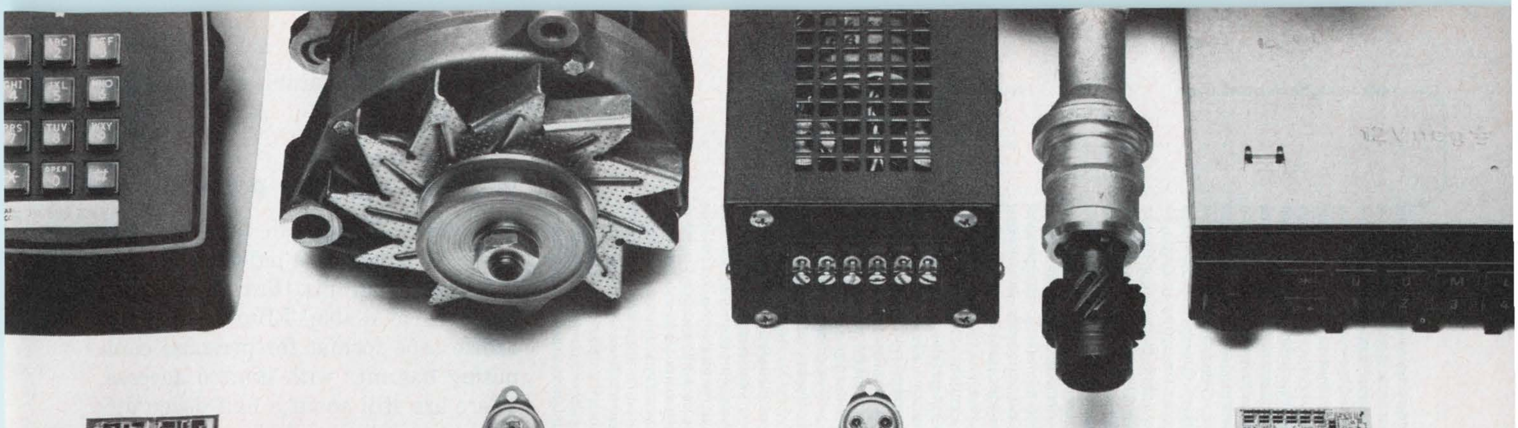
In addition, increasing the integration level of its CZT devices under Army and NASA contracts, TI has put the chirp multiplier DACs and clocks on a chip with its 500-point and 32-point CCD filters, and even includes the ROMs to feed the DACs on the 32 point chips. ■■

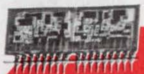
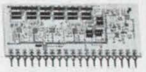
# Software distribution is a problem in personal computing—with solutions

With the ever increasing demand for computers by hobbyists and small businessmen, a problem that has been around for a long time but largely ignored is finally getting some attention—how to distribute software quickly and efficiently. Several solutions have been introduced, but so far the least expensive way is to enter data into a computer from a series of bars, which are somewhat similar to the codes found on supermarket products. The width of the bars varies to represent a one or a zero, and seven bars can be used to represent one ASCII-coded character.

Other techniques include
- Magnetic tape cassettes.
- Floppy discs.
- Floppy ROMs.
- Magnetic cards.
- Semiconductor ROMs.

Actually, the simplest way is to print a listing of the program and send it out.



HYBRID

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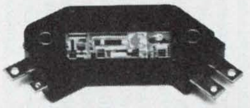

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CIRCLE NUMBER 25

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FRAME IDENTIFICATIONS

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44

**Computer programs** printed in a bar-code format can be entered directly from a printed page into a computer with the aid of a scanner from Micro-Scan. Sensitivity is so good, that even photocopies of the bar code can be read.

But it is also the most inconvenient. Someone has to sit by a terminal and type the program in—which can be very time-consuming and inefficient if the program is long, as most useful ones are.

Punched paper tape, which reduces entry time drastically, can be read on most computer systems. But paper tape is awkward to handle and easily damaged. Reproduction is a problem, too, because paper tapes can only be reproduced one at a time. So if large quantities are needed, it takes a while to prepare the tapes.

But the bar-scanner technique developed by Walter Banks, head of the computer communications network group at the University of Waterloo in Canada, combines the mass production and low cost of the printed page with the ease of inputting data directly into a computer. To read the bar code, a simple hand-held scanner is used to scan a line of code. The output of the scanner is a TTL-compatible serial signal that is then fed into any parallel port of any computer. The signal is fed to the computer in the most significant bit position so it looks like a sign bit. A test is performed to see if it is a one or zero. Additional software converts the data to alphanumeric information. Only 256 bytes of machine language code are required to handle the input and interpretation of data entered from the bar-code scanner.

Several companies are preparing entries into the bar-code scanner arena. One scanner, just introduced by Micro-Scan Associates of Natick, MA, sells for $97, which is an order of magnitude cheaper than any available optical scanners. The expensive optics normally used have been eliminated, explains Frederick L. Merkowitz, designer of the unit. All the scanning head consists of is a rectangular aperture placed in front of a Texas Instruments TIL 139 LED-phototransistor pair. The lenses generally seen in scanners aren't needed, Merkowitz notes, because the rectangular aperture makes it possible to integrate light over the whole bar, while units that use lenses only look at a small circular portion of the bar.

This difference in reading also enables the Micro-Scan unit to read photocopies as well. No other scanner available can do that, Merkowitz claims.

Although the Micro-Scan is not yet in wide use, Merkowitz notes that there are several promising applications pending. Right now, computer programs can be entered directly from a book or magazine article. One hobby magazine has already started printing programs in machine-readable, as well as human-readable, form.

Minicomputer manufacturers have expressed interest in using bar codes and scanners to patch already released software, Merkowitz goes on, or to use them even to distribute small software packages. They might also be used with scientific calculators to enter programs.

Data density per printed page is about the same as that for conventional program listings and input speed to a computer is comparable to that of paper tape.

## Magnetic tape has problems

Meanwhile, magnetic tape is widely used throughout the industry to store software programs. But there is no standard available. Efforts to standardize tape format for personal computing has met with limited success. There are still about a half dozen different recording techniques used.

Consumer-computer manufacturers like to use cassette tapes as a distribution medium because almost everyone has a reader—the conventional cassette recorder. The big problem for the software distributor, however is that cassettes are expensive and have to be produced one at a time. And for data-storage applications, high-quality tape and recording equipment are a must. In addition, several different recording formats must be provided to cover the whole market.

Floppy discs, which have become the darling of micro/mini users, have similar problems. They do have a much larger storage capacity, and are faster, but like cassettes, they have no standard. An IBM design is used by many manufacturers, but only for physical disc drives. Many IBM-compatible discs cannot be used on other IBM-compatible machines because the technique used for storing and retrieving data differs from unit to unit. And floppy discs are an expensive storage medium, typically $8 per disc.

## Floppy ROM debuts

Another approach to the mass distribution of software is a flexible vinyl record that can be bound into a magazine. Known as a floppy ROM, it combines the convenience of cassette tapes with the low cost of records.

As with cassettes, most people already have a reader for the floppy ROM, their conventional hi-fi system. The floppy ROM itself can be mass-pressed like conventional records and made for only about 10¢ apiece. They can store about 4 kbytes of data. Interfacing to a computer is done via cassette-interface electronics.

A variation on the floppy ROM is the conventional phonograph record. With this approach, longer recording times become available—which means that either longer programs or multiple programs can be recorded or, as is currently being done, one program can be recorded with several different record-


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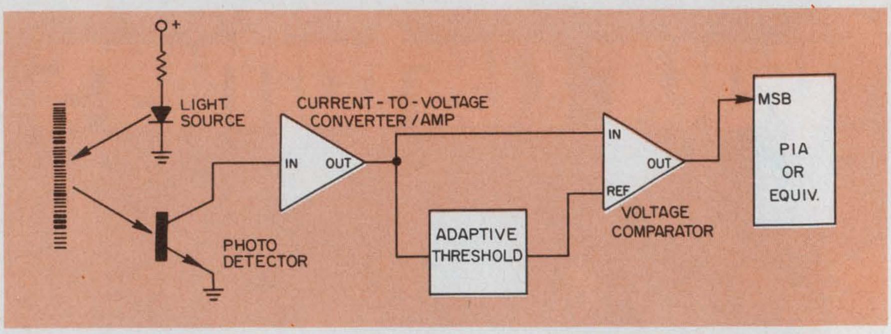



**Bar coded programs** are illuminated by a LED and sensed by a phototransistor. The pulse produced by the transistor is amplified and fed to a comparator. An adaptive threshold circuit that is used as a reference for the comparator helps eliminate noise. The output of the comparator then goes to a peripheral interface adapter (PIA) and then to the computer.

ing techniques so that it can interface with any of the cassette interface electronics currently available.

The latest medium to be introduced for the mass distribution of software is a card about the size of a credit card. The Kilobyte card is manufactured by Vertel Electronics. Although it is a magnetic-storage medium, it doesn't suffer from the high reproduction costs generally associated with magnetic storage. Cards can be produced in long strips and then cut up afterwards. They don't have to be recorded one at a time.

Each card contains four tracks of data that store 256 bytes, so that by passing it through a reader 4 times, it can yield 1024 bytes of data. This is equivalent to 30 to 50 lines of a conventional Basic language program.

### Firmware being offered

For large, sophisticated programs, the PROM is gaining in popularity as a distribution medium. Software that has been placed in hardware is known as firmware. While this concept has been around for a long time, only the recent low cost of semiconductor ROMs and PROMs has made it a feasible software-sharing technique.

A real-time operating system for the 6800 microprocessor is being offered as firmware by Microware in Des Moines, IA, and by AMI, a semiconductor manufacturer that produces the 6800.

Microware's RT-68 can easily be substituted into any system that uses Motorola's Mikbug ROM. The RT-68 has the same entry points as the Motorola device and is a real-time task scheduler that can handle 16 chores at one time.

### Computer-to-computer exchange

The most sophisticated way of distributing software is by a computer to computer exchange. This has been done by large computers for a long time via different data networks, and has now become feasible for small computers as well.

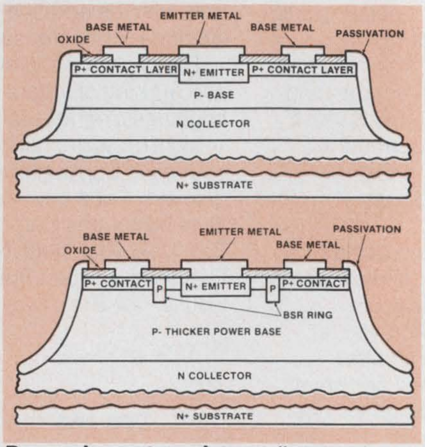
One way is to equip computers with a cassette-tape interface and have them talk to each other through these interfaces. Another way is simple frequency-shift keying over conventional communication lines, which makes it possible for computers all over the world to converse with each other and exchange software. ■■

# Power transistor process boosts performance

A new breed of power transistors offers the rugged safe-operating area generally associated with single-diffused-base transistors and the economy and complementary structures of epitaxial-base devices.

Announced by Motorola Semiconductor, Phoenix, AZ, the transistors are fabricated with what Motorola calls a power-base process. This technique reduces the crowding of current into destructive hot spots, according to Ralph Greenburg, Motorola's manager of power products. A base-spreading resistance ring is used to produce a uniform current flow in the relatively thick epitaxial base region.

Base-spreading resistance should not be confused with base or emitter-ballast resistors that have been used in the past, says Greenburg. In an npn device, the base-spreading resistance takes the form of a ring structure that surrounds the N+ emitter area in the center of the power-semi chip. This ring is fabricated by making an extra, deep P+ diffusion in the area surrounding the emitter.




**Power-base transistors** (bottom) are constructed very much like conventional epitaxial devices (top).

Some additional changes are required in the standard epitaxial-base process to produce the new power-base devices. The epitaxial-base region and the collector-base are thicker than usual. And, since the thicker bases result in a lower gain, the concentration of impurities in the emitter is changed to bring the gain back up.

Comparing the new power-base devices with those currently available, Greenburg notes that they yield performance similar to that of single-diffused devices but with a much smaller chip. For example, a single-diffused device fabricated on a 180 × 180-mil chip can be replaced by a power-base device whose chip is only 120 × 120 mil. Not only does this size reduction cut costs, but also the modified epitaxial-base process is an inherently less expensive process than single-diffused. ■■

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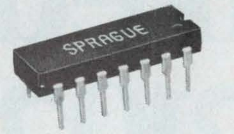
● Type UDN-2956A and UDN-2957A 14-lead DIP designs are customarily used for switching the ground side of telecommunications relays (usually −48V). Positive input and "enable" levels activate the output load.

● Series UDN-2980A 18-lead DIP devices are 8-channel source ICs for general applications, including MUXed LEDs (segment-driver/common-cathode; digit-driver/common-anode), lamps, relays, solenoids, motors, triacs, etc. An appropriate logic "1" on the input switches the output "on"; an input inverter buffers the high supply voltage from the logic circuitry. A prime application is the replacement of current-sinking ICs which may experience logic malfunctions associated with high ground currents (IR buildup) or ground noise.

● Type UDN-6118A and UDN-6128A 18-lead DIP devices are intended for vacuum fluorescent display interface. A positive input signal causes the driver outputs to switch high. Internal pull-down resistors minimize component count as well as reduce circuit cost.





| Application | Telecommunications Relays, PIN Diodes, & General-Purpose Power | | LEDs, Relays, Motors, Lamps, Triacs, Solenoids, & General-Purpose Power | | Vacuum Fluorescent Display Segment and Digit Driver | |
|---|---|---|---|---|---|---|
| Type Number | UDN-2956A | UDN-2957A | UDN-2981A/83A | UDN-2982A/84A | UDN-6118A | UDN-6128A |
| Sustaining Voltage | 80V | 80V | 50V (UDN-2981A)<br>80V (UDN-2983A) | 50V (UDN-2982A)<br>80V (UDN-2984A) | 85V | 85V |
| Source Current | 500mA | 500mA | 500mA | 500mA | 40mA | 40mA |
| No. of Drivers | 5 | 5 | 8 | 8 | 8 | 8 |
| Input | 6-15V | 5V | 5V | 6-15V | 5V | 6-15V |
| Engineering Bulletin | 29309 | | 29310 | | 29313 | |

*For application engineering assistance on these or other interface circuits, standard or custom, write or call George Tully or Paul Emerald, Semiconductor Division, Sprague Electric Company, 115 Northeast Cutoff, Worcester, Mass. 01606. Telephone 617/853-5000.*

*For Engineering Bulletins and a 'Quick Guide to Interface Circuits', write to: Technical Literature Service, Sprague Electric Company, 347 Marshall Street, North Adams, Mass. 01247.*

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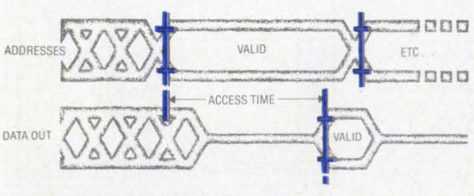
| **NO CLOCKS. NO TIMING STROBES.**   | ✓ | ✓ | No clocking needed for TI's fully static 4K RAMs. No edges. Just present an address to the selected device and data can be read at access time. That's it. |

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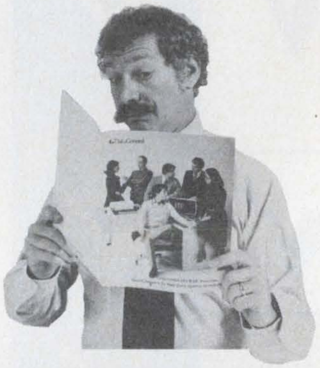

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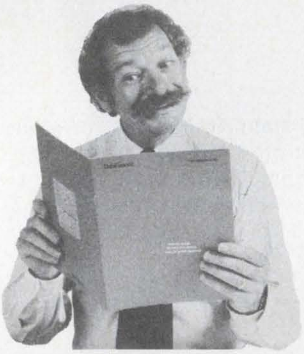

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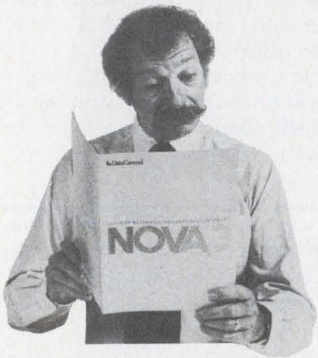


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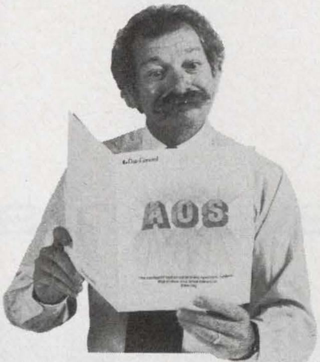


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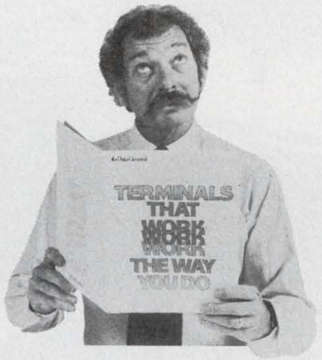


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# Washington report

## Space Shuttle instruments chosen

Five instruments have been chosen for the experimental payload of NASA's second orbital mission for the Space Shuttle. This flight, scheduled for 1979, will be the first with a predominantly scientific payload: The first mission will be devoted almost entirely to monitoring the performance of the spacecraft itself.

The instrument, an active radar of a type used in the Landsat earth-resources satellite program, is intended to operate in the microwave region of the spectrum. Landsat uses visible and near-infrared observations, and NASA considers active microwave sensors particularly valuable for mineral exploration and observations in areas usually covered by clouds. Another Landsat-type instrument, a multispectral IR radiometer, will test various combinations of near-IR bands not now used by Landsats.

Other instruments on the spacecraft will be used in experiments to measure the amount and circulation of carbon monoxide in the middle and upper troposphere; to find concentrations of chlorophyll in ocean water in an attempt to locate fish feeding grounds; and to examine the correlation between lightning and various types of severe storms. This last experiment will use a standard 16-mm movie camera rigged with a photocell to record lightning flashes as signals on a film sound track.

## Cruise missile price tag put at $3.2-billion

Cruise missiles needed to fill the gap in strategic defenses left by the cancellation of the B-1 bomber will cost $3.2-billion, the Pentagon now estimates. While the number of missiles needed has not been given, Navy Capt. Walter M. Locke, the Defense Department's cruise missile program manager, has estimated that the cruise missiles will cost up to $1-million each when inflation is taken into account.

Testifying recently before the House Armed Services Committee, Locke stated that $104.6-million in procurement funds will be needed for fiscal year 1978, which begins Oct. 1, and that another $142.5-million will be earmarked for procurement in fiscal year 1979. These funds are above and beyond the $218-million to be spent on cruise-missile development in fiscal 1978. According to Locke, the development funds will be used to prepare for the competitive flyoff in 1979 between Air Force and Navy Cruise missiles (ED No. 19, Sept. 13, 1977, p. 45) and to gear aircraft to accommodate cruise missiles.

## $1.2-billion AWACS offer to Iran goes to Congress

Congress is considering a $1.2-billion Defense Department proposal to sell an air defense system to Iran—seven E-3 Airborne Warning and Control System aircraft ($718.7-million) plus maintenance, training and spare parts ($510.2-million).

The offer had earlier been blocked by Congress on grounds that AWACS was more expensive than alternate systems and that selling the electronics-laden aircraft to Iran might cause top-secret cryptographic equipment to fall into the hands of the Soviet Union.

President Carter attempted to reassure Congress by promising that such sensitive equipment as the KG-40 encipherment system, the Joint Tactical Information Distribution System, signal-intelligence equipment, electronic counter-countermeasures and a security mode of identification of friend and foe (IFF) would not be included in the deal.

Meanwhile, the Pentagon sought to override objections that there was a better alternative to AWACS by doing a comparative study of AWACS vs both the Navy's E-2C airborne warning aircraft and a ground-based radar system known as Seek Sentry. According to the Pentagon Study team, AWACS would be available in six and a quarter years at a total cost of $2.25-billion, including 12 existing Westinghouse ADS-4 ground radars, while 21 E-2C aircraft and the same radars would cost $1.95-billion and take six and a half years. However, the E-2C is a smaller aircraft and would not have the speed, range or on-station time of AWACS.

## Air Force to develop anti-satellite weapons

The Air Force is launching a program to develop anti-satellite weapons to match recent Soviet experiments with hunter-killer satellites that were tested against Russia's own satellites. Although a 1958 treaty bans weapons in space, it does not forbid a nation from testing them against its own satellites.

The top-secret Air Force effort, known as the Satellite Defense Technology Program, will study launching projectiles from both spacecraft and aircraft against hostile satellites. Anti-satellite weapons, which would be developed for the North American Air Defense Command, would fire small, lightweight projectiles from satellites orbited by Atlas or Titan boosters.

The studies will also consider high-flying aircraft that can go into a steep climb and fire projectiles into space from pods mounted under their wings. An Air Force F-15 fighter recently demonstrated that it could climb to an altitude of 96,000 feet in less than three and a half minutes.

## NASA using IR to study air turbulence

A new round of tests to improve measurements of clear-air turbulence (CAT) through infrared radiometry techniques is due to begin in mid-October under a joint program of the National Aeronautics and Space Administration and the National Oceanic and Atmospheric Administration. The tests will try to determine how much IR readings are affected by the direction the turbulence is approached and which IR wavelengths indicate the duration and intensity of the turbulence most reliably.

Earlier NOAA tests had achieved an 81% reliability in detecting CAT ahead of an aircraft, and NASA plans to check those results with an IR radiometer mounted in a Lear Jet. The radiometer will read the fluctuation in water vapor associated with CAT. An accelerometer will measure turbulence actually encountered.

## Capital Capsules:

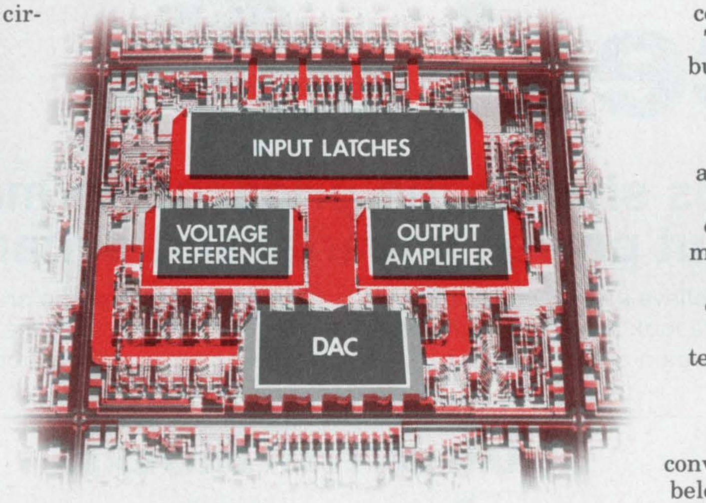
The Air Force has ordered full-scale development of the Precision Location Strike System, **an array of airborne sensors to pinpoint and attack enemy air-defense radars.** Lockheed Missiles & Space Co. was chosen as the prime contractor in June and awarded a $30-million contract, but actual payment was held up pending final approval. . .After a series of delays, the Sikorsky Aircraft Div. of United Technologies Corp. was chosen over the Boeing Vertol Div. to supply **the air frame for the Navy's Light Airborne Multi-Purpose System (LAMPS) Mark III anti-submarine-warfare helicopter.** At the same time, the Navy admitted that LAMPS prime contractor IBM had an 8% avionics "cost growth."

# New: The First Monolithic D/A Converter System.

**No one else can give you an 8-bit DAC with all peripheral functions on-chip. It's truly microprocessor-compatible and costs $6.95!**

Single-chip D/A converter circuits have been around a long time. But so have the design problems that go along with them when interfacing with microprocessors—selection of op amps, voltage reference, latches and the various other active components you've had to add to use them.

Now, for the first time, you can simplify your system design by using the Signetics 5018 Monolithic D/A Converter System. It combines, on a single chip, the converter circuit and all the required peripheral functions—a voltage reference, input latches, and an output amplifier. It costs, in quantities of 100 and up, only $6.95. That's one reason why it saves you money.




### Reduce Parts Count and Assembly Costs.

The 5018 is a system simplifier and cost reducer. You can forget about the costs associated with all those extra parts. Material control is simpler. Incoming test and inspection costs go down. Component handling and assembly expenses can be reduced as much as 75 percent.

### Ideal Architecture for Computer-Based Systems.

The 5018 has built-in latches and extremely low input loading (1/100 TTL load per line). These features make it a good choice for multiple-peripheral, bus-oriented microprocessor or computer-based systems. The low input loading lets you drive many converters from a single bus. The latches then permit the bus to service several peripherals at its maximum throughput rate.

Temperature stability is an added plus. The reference voltage can be adjusted for correct full-scale value with minimal temperature effects. Temperature-related inaccuracies are also minimized because the precision, low-temperature coefficient resistors are on the chip.

### Other Signetics DACs.

The 5018 is our newest D/A conversion product. The coupon below will help you learn more about it. If you'd like other data sheets on our other D/A converters listed below, be sure to check the appropriate boxes or call your nearest Signetics distributor.

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# RECEIVER APPLICATIONS:

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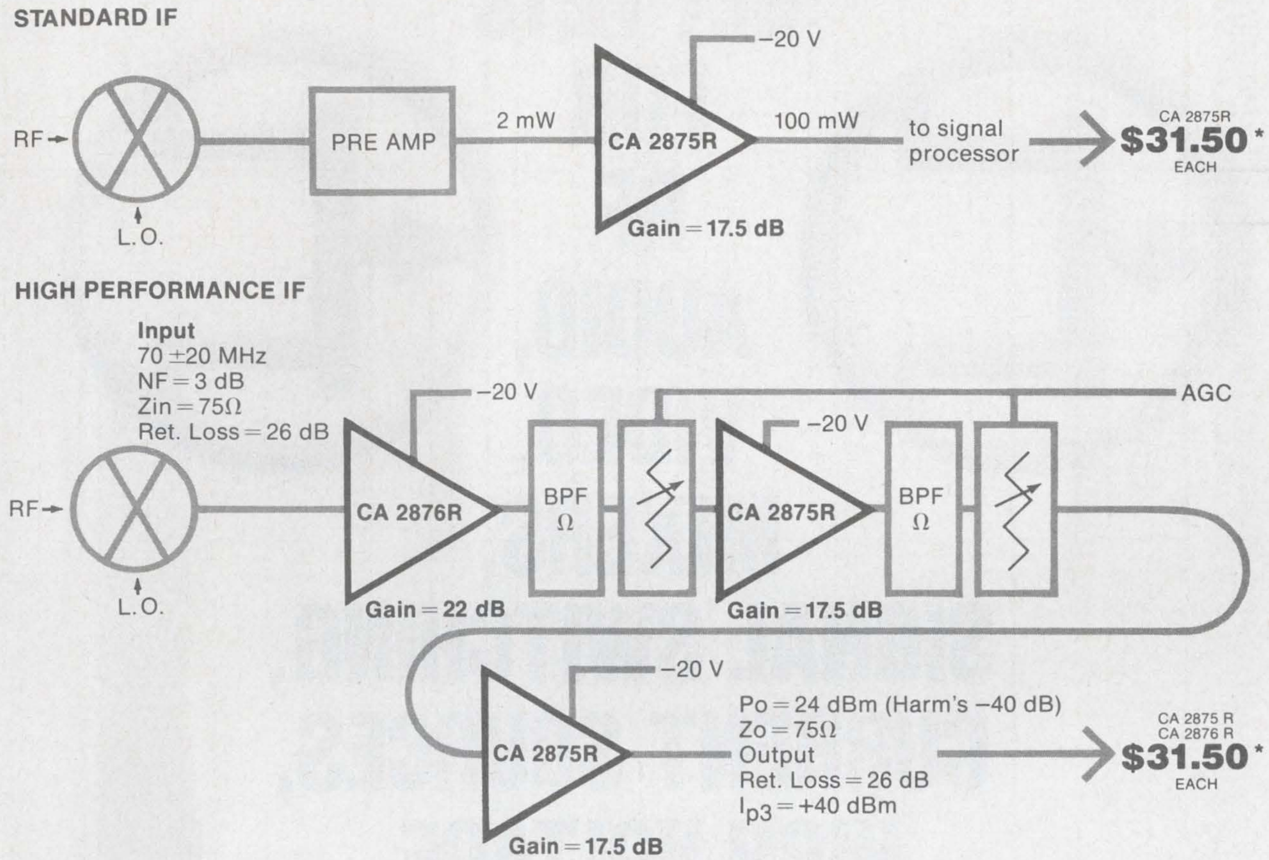
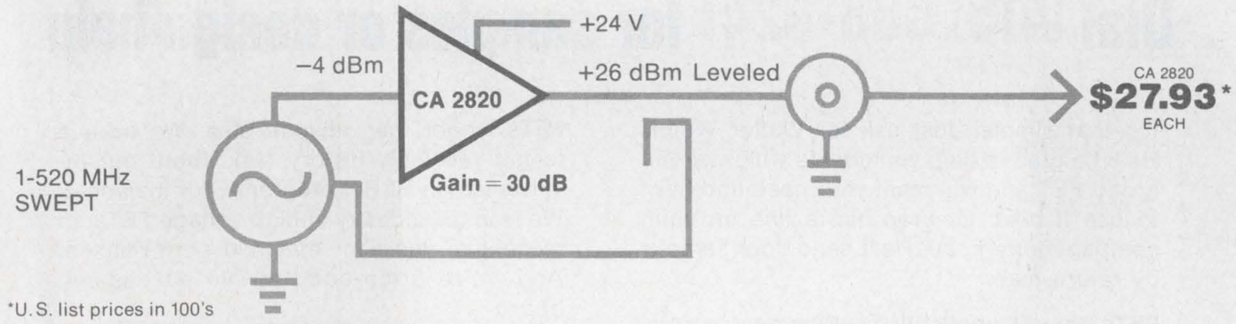



# INSTRUMENTATION APPLICATIONS:

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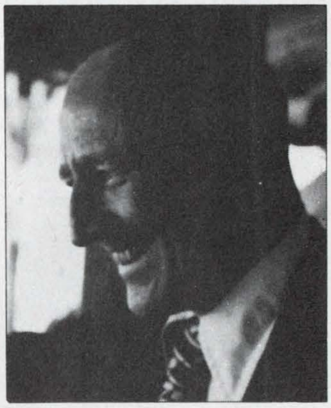
CIRCLE NUMBER 32

# The trademark



An attorney wrote the other day and insisted that I cease and desist from using his client's trademark as a generic term. Well, we're eager to protect people's trademarks, so we always capitalize the first letter. But in this case, I argued in my letter to the attorney, we didn't feel the word was a trademark, as it had seen widespread usage by other manufacturers and his client's leading competitor had been using it generically for years.

But I'm not a lawyer, I pointed out, so I would stop using the term until the squabble with his leading competitor was resolved. And it was.

The company whose lawyer had approached me —let's call it Company A—began legal action against the chief competitor—Company B. One day, one of the attorneys on Company B's side asked its president to sign some documents. When the president asked what it was all about, he was told, "This is in reference to Company A's suit against us." "Suit? What suit?" the president asked. And he was told—for the first time. "What!" he shouted. " 'Lead Arm' is going to sue us? That's ridiculous. That guy couldn't even throw a football straight when we were in school together. I'll take care of this right now."

So he telephoned "Lead Arm," Company A's president, and asked about the suit. The response went something like, "So you're still playing football without a helmet, 'Wrong Way.' What suit? What are you talking about?" And when "Wrong Way" told "Lead Arm" about the copyright-infringement litigation, "Lead Arm" said, "This is the first I've heard of it. That's absurd. I'll stop it right now." After an exchange of pleasantries and promises to buy lunch, "Lead Arm" called the head of his legal department and demanded, "Don't you guys have anything better to do with your time? Knock off this nonsense." And that was the end of the suit.

Well, it's nice to see a wrangle end amicably and sensibly. Perhaps it was fortunate, in this case, that the "contestants" were old college buddies. One wonders, though, how many other problems in management and engineering could be solved with a simpler, more direct approach. How many times do we tackle problems with a time-hallowed, absurd ritual? How often do we do things by formula, when some common sense and a departure from tradition would be simpler, less costly, and far more effective?

George Rostky

GEORGE ROSTKY
Editor-in-Chief

# The 8080A diagram

At this writing, National Semiconductor is offering 60 support products for its 8080A microprocessor. (Most are off the shelf; all are compatible with National's standard MICROBUS,™ and with microprocessors of the future.)

**Micro Bus**

## Digital I/O

| Part No. | Description |
|---|---|
| 8202 | Tri-State 8-Bit Bus Driver |
| 8203 | Tri-State 8-Bit Bus Driver (Inverting) |
| 82LS05 | 1 Out of 8 Binary Decoder |
| 83C06 | 8-Bit I/O Latch |
| 8208 | 8-Bit Bidirectional Bus Driver |
| 8212 | 8-Bit Input/Output Port |
| 8213 | Bidirectional 8-Bit I/O Port |
| 8216 | 4-Bit Bidirectional Bus Driver |
| 8226 | 4-Bit Bidirectional Bus Driver (Inverting) |

## Peripheral Control

| Part No. | Description |
|---|---|
| 8244* | 90-Key Keyboard Encoder |
| 8245 | 16-Key Keyboard Encoder |
| 8246 | 20-Key Keyboard Encoder |
| 8247* | 4-Digit Display Controller |
| 8248* | 6-Digit Display Controller |
| 8253* | Programmable Interval Timer |
| 8254 | Programmable Bit Addressable Interface |
| 8255 | Programmable Peripheral Interface |
| 8257* | Programmable DMA Controller |
| 8258* | Advanced Programmable DMA Controller |
| 8259* | Programmable Interrupt Controller |
| 8272* | Floppy Disk Formatter/Controller |
| 8276* | CRT Controller |
| 8285 | Character Generator |
| 8292 | 8-Bit A/D Convertor with 16-Channel Analog Mux |
| 8294 | 3-3/4-Digit DVM with Multiplexed BCD Outputs |
| 8298* | LLL 8080A "Basic" Interpreter Plus Hex Debugger |

# Intel couldn't run.

Intel offers only 29 support products.
Which leaves us with 31 more ways we can help you get the job done.
And that's kinda nice.

## 8080A Microprocessor

| Part No. | Description |
|---|---|
| 8224 | Clock Generator and Driver for the 8080A CPU |
| 8228 | System Controller and Bus Driver for the 8080A CPU |
| 8238 | System Controller and Bus Driver for the 8080A CPU |

## Communications

| Part No. | Description |
|---|---|
| 8250 | Asynchronous Communications Element |
| 8251 | Programmable Communications Interface |
| 8252* | Advanced Programmable Communications Interface |
| 8261* | Programmable Communications Subsystem |
| 8274* | Multi-Protocol Communications Controller-SDLC, ADCCP, Bisync, DDCMP |
| 8283* | Advanced SDLC, ADCCP Protocol Controller |

## Memory

| Part No. | Description |
|---|---|
| 8356 | 2048X8 ROM, 128X8 RAM I/O |
| 8154 | 128X8 Static RAM with 16-Bit I/O |
| 8364/ 8364E* | 8192X8 MOS Mask ROM (E is 2708 Compatible) |
| 8316A/E | 2048X8 MOS Mask ROM |
| 8332E | 4096X8 MOS Mask ROM (2708 Compatible) |
| 1702A | 256X8 EPROM |
| 8704 | 512X8 EPROM |
| 2708/8708 | 1024X8 EPROM |
| 8101A-4 | 256X4 Static RAM with Separate I/O |
| 8111A-4 | 256X4 Static RAM with Common I/O |
| 8102A | 1024X1 Static RAM |
| 74C920 | 256X4 CMOS Static RAM with Separate I/O |
| 74C921 | 256X4 CMOS Static RAM with Common I/O |
| 74C929 | 1024X1 CMOS Static RAM |
| 2114 | 1024X4 Static RAM |
| MM257 | 4096X1 Static RAM |
| DM87S296* | 512X8 Bipolar PROM |
| 5290 | 16K Dynamic RAM |
| 8316A/E | Mask ROM (2708 Compatible) |
| DM74S472* | 512X8 Bipolar PROM/20-Pin DIP |
| MM5204 | 512X8 EPROM |

*Available soon.

# Microprocessor Data Manual

This manual has four sections to help you evaluate the microprocessors, microcomputers and bit slices available from over 30 manufacturers.

The first section of the Data Manual deals with microprocessor specifications and some of the pitfalls you should avoid as you try to narrow the choice to a specific model. Included are summary tables of many device specifications as well as cross references by model number and an alternate-source directory.

The second section features a primer article intended for the microprocessor novice or for those who want a refresher. The primer reviews most microprocessor fundamentals and contains a glossary of commonly used microprocessor-related terms.

The third section contains a data page for each microprocessor or family of processors. Each page has a complete description of the processor, its family of support circuits with prices as of Aug. 1, 1977, a description of the architecture and a discussion of available software and the unit's instruction set.

The fourth section contains a Focus report on floppy-disc drives, the most popular bulk-storage device now in use with microprocessor-based equipment. Learning how to avoid specification pitfalls will be an important part of picking the best drive for your microcomputer system.

## Contents

# Microprocessor selection guide

Every microprocessor can do a job—but with its own language, architecture, support circuits and development aids. Knowing one particular microprocessor's language (instruction set) doesn't mean you can easily switch to another.

Selecting the best microprocessor, microcomputer or bit slice has become a nightmare. Once you've selected one, you face another bad dream—testing it. Because a $\mu$P is designed to be general-purpose, it can handle a virtually unlimited number of code combinations. Some manufacturers have calculated that, even when operating the processor at top speed, it would take over 10 years to check all code combinations.

To help sort out the various models, word sizes and performance ranges, ELECTRONIC DESIGN presents its Microprocessor Data Manual. In it you will find performance summaries of every available processor and summary tables to help you compare similar units. Also, to help you locate a processor by manufacturer or model number, we have included cross-reference tables and an alternate-source directory.

Three major classes of processor components are covered in this Manual:

1. **Microprocessor**—a general-purpose processor on one to three chips. It contains an arithmetic and logic unit (ALU), an address and data bus (sometimes multiplexed), a built-in instruction set, and the basic control logic.

2. **Microcomputer**—an all-in-one general-purpose processor that is similar to the microprocessor except that the chip contains the main control program in read-only memory (ROM) and possibly a clock oscillator, some input/output (I/O) capability, and some read-write random-access memory (RAM).

3. **Bit slice**—an enhanced subsection of the microprocessor's ALU. Besides the slice, which is available in two or four-bit sections, other circuits must be added to provide the basic control logic.

There are, of course, other classes of microprocessor components—dedicated controller chips that are either custom-designed or preprogrammed for specific applications. Calculator chips, floppy-disc controllers, microwave-oven controllers and many industrial process-control circuits are typical examples.

### Selection can start with data-word size

To start selecting, many companies recommend that you first decide on the word size and the type of instructions needed. Then you can determine the execution speed and I/O capability needed. Once these four basics are nailed down, you're free to look at price, power drain, technology and available support.

Instruction-compatible microprocessors are available in more than one technology to provide performance demanded by some applications. You can pick and choose from bipolar technology (ECL, $I^2L$, STTL or TTL) or MOS (CMOS, NMOS or PMOS).

If you plan to use an off-the-shelf processor, you can select data-word lengths of 1, 4, 8, 12 or 16 bits for microprocessor chips, 1, 4, 8 or 16 bits for microcomputer chips and 2 or 4 bits for bit slices. (An 8-bit ECL slice is expected next year from Fairchild.)

Performance summaries of the three processor types are provided in Tables 1, 2, and 3, respectively. While all performance specs have been normalized for easy comparison, you can still be misled by manufacturers if you don't read the fine print.

Computing speed is a case in point. Often, manufacturers use a basic cycle time or period—sometimes called a microcycle—to specify the instruction execution speed. But a microcycle is not necessarily the inverse of the clock frequency—it's often a multiple, possibly two or three times the clock frequency. Each instruction is then defined as requiring several microcycles for execution.

As a result, a three-microcycle instruction may actually require three, six or nine clock cycles. What's more, longer instructions such as multiply and divide can require tens or even hundreds of microcycles.

Clock speed can be misleading, too, if taken for a measure of processor speed. One microprocessor can perform basic operations—such as a register-to-register add—faster than another unit running at a higher clock because of variations in its internal architecture. In this instance a clock-rate spec is not very important.

Other speeds can give false indications of processor speed, including minimum instruction time, interrupt-response time, and addition time. Like cycle time and clock rate, these specs *don't* measure such important factors as the over-all time needed to perform critical routines in an application. Excluded, for instance, are the delays incurred when the processor must get data from memory. You can solve this dilemma by tailoring a program that compares the performance of several machines doing the same job.

Such a benchmark can help determine the power of the processor's instruction set, and circumvent another oft-abused spec—the number of instructions. Microprocessor comparisons based on this number abound, but don't make a choice based only on this number. Make sure you can use all the commands.

### Examine the instruction set carefully

A number won't tell you which instructions are put aside for data movement and manipulation, for decision and control and for input and output. Some microprocessors have many more I/O commands than

# Table 1. General-purpose microprocessors

| Manufacturer | Processor | Process technology | Word size (data/instruction) | Direct addressing range (words) | Number of basic instructions | Maximum clock frequency (MHz)/phases | Instruction time shortest/longest[2] (µs) | TTL compatible | BCD arithmetic | On-chip interrupts/levels | Number of internal general-purpose registers | Number of stack registers | On-chip clock | DMA capability | Specialized memory & I/O circuits avail. | Prototyping system avail. | Package size (pins) | Voltages required (V) | Assembly language development system | High-level languages | Time-sharing cross software | Comments | Circle number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Motorola | MC14500 | CMOS | 1/4 | 0 | 16 | 1/1 | 1/1 | Yes | No | Yes/1 | 1 | 0 | Yes | No | No[4] | No | 16 | 3 to 18 | No | No | No | Needs external program counter | 451 |
| Intel | 4004 | PMOS | 4/8 | 4k | 46 | 0.74/2 | 10.8/21.6 | No | Yes | Yes/1 | 16 | 3x12 | No | No | Yes | No | 16 | 15 | Yes | Yes | Yes | Superseded by 4040 | 452 |
| Intel | 4040 | PMOS | 4/8 | 8k | 60 | 0.74/2 | 10.8/21.6 | No | Yes | Yes/1 | 24 | 7x12 | No | No | Yes | Yes | 24 | 15 | Yes | Yes | Yes | General-purpose 4-bit µP | 453 |
| NEC Microcomputers | µPD541 | PMOS | 4/8 | 4k | 69 | 0.5/2 | 6.4/38.4 | Yes | Yes | Yes/8 | 4 | 8x12 | No | Yes | Yes | Yes | 42 | 5,−5 | Yes | No | No | Intended for electronic cash registers, etc. | 454 |
| Fairchild | 2 chip F8 | NMOS | 8/8 | 64k | 69 | 2/1 | 2/13 | Yes | Yes | Yes/1 | 64 | RAM | Yes | Yes | Yes | Yes | 40 | 5,12 | Yes | Yes | Yes | Usually used with program storage unit | 455 |
| General Instrument | 8000 | PMOS | 8/8 | 1k | 48 | 0.8/2 | 1.25/3.75 | No | Yes | Yes/1 | 48 | 0 | No | No | Yes | Yes | 40 | 5,−12 | No | Yes | Yes | Predecessor of F8 | 457 |
| Intel | 8008 | PMOS | 8/8 | 16k | 48 | 0.8/2 | 12.5/37.5 | No | Yes | Yes/1 | 6 | 7x14 | No | No | Yes | Yes | 18 | 5,−9 | Yes | Yes | Yes | Predecessor of 8080, still in wide use | 458 |
| Intel | 8080A | PMOS | 8/8 | 64k | 78 | 2.6/2 | 1.5/3.75 | Yes[3] | Yes | Yes/1 | 8 | RAM | No | Yes | Yes | Yes | 40 | 5,12,−5 | Yes | Yes | Yes | By and large, still the most popular | 459 |
| Intel | 8085 | NMOS | 8/8 | 64k | 80 | 3/1 | 1.3/5.85 | Yes | Yes | Yes/4 | 8 | RAM | Yes | Yes | Yes | Yes | 40 | 5 | Yes | Yes | Yes | 8080 code compatible, has built-in clock | 460 |
| MOS Technology | MCS-650X | NMOS | 8/8 | 64k | 56 | 4/1 | 0.5/3.5 | Yes | Yes | Yes/1 | 0 | RAM | Yes | No | Yes | Yes | 40 | 5 | Yes | Yes | Yes | Provides 13 addressing modes | 461 |
| MOS Technology | MCS-651X | NMOS | 8/8 | 64k | 56 | 4/2 | 0.5/3.5 | Yes | Yes | Yes/1 | 0 | RAM | No | No | Yes | Yes | 40 | 5 | Yes | Yes | Yes | Similar to 650X but needs 2φ clock | 462 |
| Motorola | M6800 | NMOS | 8/8 | 64k | 89 | 2/1 | 1/2.5 | Yes | Yes | Yes/1 | 0 | RAM | No | Yes | Yes | Yes | 40 | 5 | Yes | Yes | Yes | Available in new depletion-load version | 463 |
| Motorola | M6809 | NMOS | 8/8 | 64k | 100+ | 2/1 | 2/5 | Yes | Yes | Yes/1 | 0 | RAM | Yes | Yes | Yes | Yes | 40 | 5 | Yes | Yes | Yes | Enhanced 6800 command set | 464 |
| Motorola | M6802 | NMOS | 8/8 | 64k | 89 | 2/1 | 2/5 | Yes | Yes | Yes/1 | 0 | RAM | Yes | Yes | Yes | Yes | 40 | 5 | Yes | Yes | Yes | Has 128 x 8 on-chip RAM | 465 |
| National Semiconductor | SC/MP | PMOS NMOS | 8/8 | 64k | 46 | 4/1 | 5/10 | NMOS only | Yes | Yes/1 | 0 | RAM | Yes | Yes | No[4] | Yes | 40 | 5,−7 | Yes | Yes | Yes | Has handy daisy-chain capability | 466 |
| NEC Microcomputers | µPD 8080A | NMOS | 8/8 | 64k | 78 | 2/2 | 1.92/8.16 | Yes[3] | Yes | Yes/1 | 8 | RAM | No | Yes | Yes | Yes | 40 | 5,12,−5 | Yes | Yes | Yes | Pin compatible but does BCD subtraction | 467 |
| RCA | 1802 | CMOS | 8/8 | 64k | 91 | 6.4/1 | 2.5/3.75 | Yes | Yes | Yes/1 | 16 | RAM | Yes | Yes | Yes | Yes | 40 | 3 to 12 | Yes | Yes | Yes | Superseded two-chip version | 468 |
| RCA | 1803 | CMOS | 8/8 | 64k | 91 | 6.4/1 | 2.5/3.75 | Yes | Yes | Yes/1 | 16 | RAM | Yes | Yes | Yes | Yes | 28 | 3 to 12 | Yes | Yes | Yes | Trimmed down version of 1802 | 469 |
| Scientific Microsystems | SMS-300 | Bipolar | 8/8 | 8k+ | 8 | 10/1 | | Yes | No | No | | 0 | No | | Yes | | 50 | | No | Yes | Yes | Very specialized instruction set | 470 |
| Signetics | 2650 | NMOS | 8/8 | 32k | 75 | 1.2/1 | 4.8/9.6 | Yes | Yes | Yes/1 | 7 | 8x15 | No | Yes | Yes | Yes | 40 | 5 | Yes | Yes | Yes | Has two higher speed versions | 471 |
| Zilog | Z80 | NMOS | 8/8 | 64k | 150+ | 4/1 | 1/5.75 | Yes | Yes | Yes/1 | 14 | RAM | No | Yes | Yes | Yes | 40 | 5 | Yes | Yes | Yes | 8080 instructions are a subset | 472 |
| Intersil | 6100 | CMOS | 12/12 | 4k | 81 | 4/1 | 2.5/5.5 | Yes | No | Yes/1 | 0 | RAM | Yes | Yes | Yes | Yes | 40 | 4 to 11 | Yes | Yes | Yes | Emulates PDP-8 instruction set | 473 |
| Toshiba | T3190 | PMOS NMOS | 12/12 | 4k | 108 | 2.5/1 | 10/30 | Yes | No | Yes/8 | 8 | RAM | Yes | Yes | Yes | Yes | 36 | 5, −5 | Yes | Yes | Yes | Has multiply and divide inst. | 474 |
| Data General | mN601 | NMOS | 16/16 | 32k | 42 | 8.33/2 | 1.2/29.5 | Yes | No | Yes/1 | 4 | RAM | Yes | Yes | Yes | No | 40 | 5,10,14,−4.25 | Yes | Yes | Yes | Emulates NOVA instruction set | 475 |
| Fairchild | 9440 | I²L | 16/16 | 64k | 42 | 10/1 | | Yes | No | Yes/1 | 4 | RAM | Yes | Yes | No[4] | No | 40 | | No | No | No | Emulates NOVA instruction set | 476 |
| Ferranti | F100L | Bipolar | 16/16 | 32k | 28 | 20/1 | 1.19/5.75 | Yes | No | Yes/1 | 0 | RAM | No | Yes | Yes | Yes | 40 | 5 | Yes | Yes | Yes | Can do double word operations | 456 |
| General Instrument | CP1600 | NMOS | 16/16 | 64k | 87 | 4/2 | 1.6/4.8 | Yes | No | Yes/1 | 8 | RAM | No | Yes | Yes | Yes | 40 | 5,12,−3 | Yes | Yes | Yes | All internal registers can be accumulators | 477 |
| National Semiconductor | INS8900/PACE | NMOS/PMOS | 16/16 | 64k | 45 | 2/2 | 2.5/5 | No | Yes | Yes/6 | 4 | 10x16 | No | Yes | Yes | Yes | 40 | 5,8,−12 | Yes | Yes | Yes | Architecture intended for data handling | 478 |
| Panafacom | MN1610 | NMOS | 16/16 | 64k | 33 | 2/2 | 2/6 | Yes[3] | No | Yes/3 | 5 | RAM | No | Yes | Yes | No | 40 | 5,12,−3 | Yes | No | No | | 479 |
| Texas Instruments | TMS9980 | NMOS | 16/16[1] | 16k | 69 | 4/4 | 3.2/49.6 | Yes[3] | No | Yes/4 | 16 | RAM | Yes | Yes | Yes | No | 40 | 5,12,−5 | Yes | Yes | Yes | Small version of TMS 9900 | 480 |
| Texas Instruments | TMS/SBP9900 | NMOS I²L | 16/16 | 64k | 69 | 4/4 | 2/31 | Yes[3] | No | Yes/16 | 16 | RAM | No | Yes | Yes | No | 64 | 5,12,−5 | Yes | Yes | Yes | Emulates 990 mini instructions | 481 |
| Western Digital | WD-16 | NMOS | 16/16 | 64k | 116 | 3.3/4 | 2.1/780 | Yes | Yes | Yes/16 | 6 | RAM | No | Yes | Yes | Yes | 40 | 5,12,−5 | Yes | Yes | No | Very similar to DEC LSI-11 | 529 |

1. Has 8-bit external buses and 16-bit internal buses 2. With maximum clock 3. Except clock lines 4. Standard TTL or MOS circuits will suffice

others, and are thus tailored for a specific group of applications. Instructions that you want but are not included in the instruction set can be provided with programmed routines, although you'll probably sacrifice some speed to get the extra commands.

Examine a particular unit's programming manual carefully. The number of instructions claimed for a processor can increase from one page to another. Often, this increase stems from the different ways used to define instructions. Many instructions are available in different modes or operate on different bits of a data word. Each variation in the same basic instruction produces a different operation code—a different instruction.

For example, the programming manual for a Z80 microprocessor says there are 158 "different" instructions. But taking into account all the possible addressing modes and variations, the 158 instructions become 696 operation codes. (Just to go back to the testing problem, there are 696! possible combinations of instructions. Multiply each instruction by 1.5 $\mu$s—assuming a 4-MHz clock—and then figure out how many years you'll need for a full test.)

Common addressing modes include direct, immediate and indirect, but many processors offer other modes, such as register, page 0, register indirect, extended, implied and relative.

Often, the most flexible instruction sets are available in 16-bit processors, since the units closely resemble minicomputers in both performance and design. For example, some 16-bit processors offer multiply and divide instructions that execute in tens of microseconds. Eight-bit processors can be programmed to do the same calculation, but take milliseconds to do the job. In general, processors with the same word length offer similar performance.

### Analyze the $\mu$P's architecture

Chip vendors will tout the computer-like features of microprocessors every chance they get. These include the number and function of on-chip registers, the type and depth of the stack register, interrupt capability and the direct-memory-access feature. But when it comes to architecture, the chip vendors lose their voices to minicomputer manufacturers. They can't deliver as much performance.

The number of internal registers included in a processor is not really critical unless you are designing a minimal one or two-chip system. Essentially, the only register a processor needs is an accumulator. However, the accumulator must have access to memory, and an instruction set should permit immediate addressing and data manipulation between the memory and the accumulator. If indirect addressing is available, even special indexing registers can be imitated by using memory locations as registers.

The advantage of using on-chip registers instead of memory space is that the instructions are faster and the bits required are fewer. For example, not nearly as many bits are required to specify one of several predefined working registers as to specify a memory location. And since the registers are on-chip, access times are much shorter than for normal memory.

The type and flexibility—not just the quantity—of these on-chip registers is also important. Not every "general purpose" register can be incremented, tested for zero, decremented, or have other operations performed. Not every register can be used for program-loop control or counting or even indexed addressing, without some fancy programming tricks or excessive time delays.

Even the source and destination points for these registers must be examined. A processor should be able to load registers directly from memory—and memory from registers—without having the data first go into its accumulator.

Microprocessors are split about 50-50 between those that have on-chip subroutine stack registers and those that don't. The units without use memory as a subroutine stack, so they can handle an almost unlimited number of program subroutines. However, their chips must have a stack-pointer register, which must be set by one of the initialization instructions to point at the area of memory reserved for the stack. When the stack is on the processor chip, there is a limit to the number of subroutine levels that can be stored in the stack.

If an application involves asynchronous or unpredictable events, an interrupt capability on the processor is essential. Most units claim some form of interrupt capability, but only a few of the newer units can handle several levels of prioritized interrupt. Most of the processors announced in the last year can handle single-line, multilevel and vectored interrupts. And all their registers are automatically saved in the stack when an interrupt comes along; after the interrupt is serviced, the register contents are automatically restored.

When large amounts of data must be transferred back and forth between a $\mu$P's memory and peripherals, your processor should be able to withdraw itself from the loop and permit direct-memory accesses (DMAs). Most of the newer units can do that and even have one or two pins dedicated to a DMA-control function. A DMA transfer can often be five to ten times faster than transferring data through the processor itself for I/O applications.

### Decide on the number of I/O lines

Most microprocessors provide the means to control input/output operations via specialized circuits. Microcomputers, on the other hand, usually have some of the I/O capability built in. If your application requires a fixed number of input lines and a fixed number of output lines, one of the all-in-one chips could be the answer, since they offer as many as 32 I/O lines in a single package. However, when your I/O requirements are subject to change, one of the

# Table 2. All-in-one processors

| Company | Device | Process technology | Word size in bits (data/inst.) | On-chip RAM size | On-chip ROM/PROM size (words) | Off-chip memory expansion | Number of basic instructions | Maximum clock frequency (kHz) | On-chip clock | Instruction time (shortest/longest) μs | TTL compatible | BCD arithmetic | On-chip interrupts/levels | Subroutine nesting levels | General-purpose internal registers | Number of I/O lines | Additional special support circuits | Package size (DIP pins) | Voltages required (V) | Prototyping system avail. | Assembly language programming system | High-level language programming system | Time-sharing cross software | Comments | Circle number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| General Instrument | SBA | NMOS | 1/8 | 120×1 | 1024×8 | No | 8 | 800 | Yes | 1.25/1.25 | Yes | No | No | 16 | RAM | 31 | No | 40 | 5,12 | Yes | No | No | No | Will have expandable version | 482 |
| Essex International | SX-200 | PMOS | 4/8 | 64×4 | 1024×8 | Yes | 41 | 400 | Yes | 20/20 | No | Yes | Yes/1 | 1 | RAM | 16 | No | 28 | 10 to 20 | Yes | Yes | Yes | Yes | Has touch switch interface | 483 |
| ITT Semiconductor | 7150 | PMOS | ? | ? | N.A.[1] | ? | ? | 25 | Yes | ? | ? | ? | ? | ? | ? | 14 | Yes | 14/18/24 | −15 | No | No | No | No | Designed for washing machines | 484 |
| National Semi | MM57109 | PMOS | 4/8 | 5×32 | N.A. | Yes | 70 | 400 | No | 1220/1 S | Yes | Yes | Yes/1 | 4 | 1 | 11 | Yes | 28 | 9 | No | No | No | No | Has scientific calculation ability | 485 |
| | MM57140/57152 | PMOS | 4/8 | 55×4 | 630×8 | No | 35 | 280 | Yes | 16/16 | Opt. | Yes | 0 | 2 | 4 | 24 | No | 28 | 7.9 to 9.5 | Yes | Yes | No | Yes | Drives LEDs or fluorescents | 486 |
| | MM5799 | PMOS | 4/8 | 96×4 | 1536×8 | No | 35 | 400 | Yes | 10/20 | Opt. | Yes | 0 | 2 | 5 | 23 | Yes | 28 | 7.9 to 9.5 | Yes | Yes | No | Yes | Serial I/O and LED drive | 487 |
| | MM5781/82 | PMOS | 4/8 | 160×4 | 2048×8 | Yes | 35 | 400 | No | 10/20 | Opt. | Yes | 0 | 2 | 5 | 24 | Yes | 28 | 7.9 to 9.5 | Yes | Yes | No | Yes | Two chip set | 488 |
| NEC Microcomputers | μPD548 | PMOS | 4/10 | 96×4 | 1920×10 | Yes | 72 | 200 | No | 10/20 | Yes | Yes | Yes/2 | 4 | RAM | 35 | No | 42 | −10 | Yes | Yes | No | No | Can interface to keyboard | 489 |
| | μPD546 | PMOS | 4/8 | 96×4 | 2000×8 | No | 80 | 440 | No | 10/40 | Yes | Yes | Yes/1 | 3 | 6 | 35 | No | 42 | −10 | Yes | Yes | No | Yes | Has 6-bit programmable timer | 490 |
| | μPD547 | PMOS | 4/8 | 64×4 | 1000×8 | No | 58 | 440 | No | 10/40 | Yes | Yes | Yes/1 | 1 | RAM | 35 | No | 42 | −10 | Yes | Yes | No | Yes | Instructions are 546 subset | 491 |
| | μPD545 | PMOS | 4/8 | 32×4 | 640×8 | No | 58 | 440 | No | 10/40 | Yes | Yes | Yes/1 | 1 | RAM | 21 | No | 28 | −10 | Yes | Yes | No | Yes | Can handle high voltages | 492 |
| Panasonic | MN1400 | NMOS | 4/8 | 64×4 | 1024×8 | No | 75 | 300 | Yes | 10/20 | Yes | Yes | Yes/1 | 2 | RAM | 30 | No | 40 | 5 | No | Yes | Yes | Yes | Complete all-in-one controller | 532 |
| | MN1402 | NMOS | 4/8 | 32×4 | 768×8 | No | 57 | 300 | Yes | 10/20 | Yes | Yes | Yes/1 | 2 | RAM | 19 | No | 28 | 5 | No | Yes | Yes | Yes | Smaller I/O version of 1400 | 533 |
| | MN1498 | NMOS | 4/8 | 64×4 | N.A. | Yes | 68 | 300 | Yes | 10/20 | Yes | Yes | Yes/1 | 2 | RAM | 18 | No | 40 | 5 | No | Yes | Yes | Yes | Handles 1024 bytes of external memory | 534 |
| | MN1499 | NMOS | 4/8 | 64×4 | N.A. | Yes | 75 | 300 | Yes | 10/20 | Yes | Yes | Yes/1 | 2 | RAM | 31 | No | 64 | 5 | No | Yes | Yes | Yes | Handles 2048 bytes of external memory | 535 |
| Rockwell | PPS-4 | PMOS | 4/8 | 0 | 0 | Yes | 50 | 200/400 Two clocks | No | 5/15 | No | Yes | Yes/1 | 2 | 1 | 12+ | Yes | 42 | −17/+5,−12 | Yes | Yes | No | Yes | Combination ROM/RAM/I/O available | 493 |
| | PPS 4/2 | PMOS | 4/8 | 0 | 0 | Yes | 50 | 200/400 | Yes | 5/15 | No | Yes | No | 2 | 1 | 12+ | Yes | 42 | −17/+5,−12 | Yes | Yes | No | Yes | Same as PPS-4 but has internal clk | 494 |
| | PPS-4/1 MM77 | PMOS | 4/8 | 96×4 | 1344×8 | RAM only | 50 | 100/4 | Yes | 10/40 | Yes | Yes | Yes/1 | 2 | 2+RAM | 31 | Yes | 42 | −15/+5,−10 | Yes | Yes | No | Yes | I/O includes serial channel | 495 |
| | MM78 | PMOS | 4/8 | 128×4 | 2048×8 | RAM only | 50 | 100/4 | Yes | 10/40 | Yes | Yes | Yes/1 | 2 | 2+RAM | 31 | Yes | 42 | −15/+5,−10 | Yes | Yes | No | Yes | Software compatible with 77 | 496 |
| | MM76 | PMOS | 4/8 | 48×4 | 640×8 | RAM only | 50 | 100/4 | Yes | 10/40 | Yes | Yes | Yes/1 | 1 | 1+RAM | 31 | Yes | 42 | −15/+5,−10 | Yes | Yes | No | Yes | Primarily used for keyboard display | 497 |
| | MM76/C | PMOS | 4/8 | 48×4 | 640×8 | RAM only | 50 | 100/4 | Yes | 10/30 | Yes | Yes | Yes/1 | 1 | 1+RAM | 39 | Yes | 52 | −15/+5,−10 | Yes | Yes | No | Yes | Has high-speed counter | 498 |
| | MM76/D | PMOS | 4/8 | 48×4 | 640×8 | RAM only | 50 | 100/4 | Yes | 10/30 | Yes | Yes | Yes/1 | 1 | 1+RAM | 37 | Yes | 52 | −15/+5,−10 | Yes | Yes | No | Yes | Has a/d converter on chip | 499 |
| | MM76/E | PMOS | 4/8 | 48×4 | 1024×8 | RAM only | 50 | 100/4 | Yes | 10/30 | Yes | Yes | Yes/1 | 1 | 1+RAM | 31 | Yes | 42 | −15/+5,−10 | Yes | Yes | No | Yes | Larger ROM than MM76 | 500 |
| | MM76/L | PMOS | 4/8 | 48×4 | 640×8 | RAM only | 50 | 100/4 | Yes | 10/30 | Yes | Yes | Yes/1 | 1 | 1+RAM | 31 | Yes | 40 | 6 to 11 | Yes | Yes | No | Yes | Low voltage version of 76 | 501 |
| | MM75 | PMOS | 4/8 | 48×4 | 670×8 | RAM only | 50 | 100/4 | Yes | 10/40 | Yes | Yes | Yes/1 | 1 | 1+RAM | 22 | Yes | 28 | −15/+5,−10 | Yes | Yes | No | Yes | Reduced I/O version of 76 | 502 |
| Texas Instruments | TMS-1000 | PMOS/NMOS | 4/8 | 64×4 | 1024×8 | No | 43 | 400 | Yes | 15/15 | Yes | Yes | Yes/1 | 1 | 2 | 23/25 | Yes | 28/40 | 15 | Yes | Yes | Yes | Yes | Also a 35 V family and a low voltage family TMS 1070/1270 and TMS 1100/1300 | 503 |
| | TMS-1100 | PMOS/NMOS | 4/8 | 128×8 | 2048×8 | No | 40 | 400 | Yes | 15/15 | Yes | Yes | Yes/1 | 1 | 2 | 23/28 | Yes | 28/40 | 15 | Yes | Yes | Yes | Yes | Pin compatible with TMS-1000 | 504 |
| | TMS-1018 | PMOS | 4/8 | 64×4 | N.A. | No | 43 | 400 | Yes | 15/15 | Yes | Yes | No | N.A. | N.A. | 4 | No | 28 | 15 | Dedicated number cruncher | | | | | 505 |

| | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TMS-1022 | PMOS | 4/8 | 64×4 | 1024×4 | No | 43 | 400 | Yes | 15/15 | Yes | Yes | Yes/1 | 1 | 2 | N.A. | No | 28 | 15 | Dedicated CB PLL controller | | | | | 538 |
| | TMS-1117 | PMOS | 4/8 | 128×8 | N.A. | No | 43 | 400 | Yes | 15/15 | Yes | Yes | No | N.A. | N.A. | 19 | Yes | 28 | 15 | Dedicated controller for microwave ovens | | | | | 506 |
| | TMS-1121 | PMOS | 4/8 | 128×4 | 2048×8 | No | 42 | 400 | Yes | 15/15 | Yes | Yes | Yes/1 | RAM | RAM | N.A. | Yes | 40 | 15 | Dedicated multiappliance timer/controller | | | | | 539 |
| | TMS-1330 | PMOS | 4/8 | 128×4 | 2048×8 | No | 42 | 400 | Yes | 15/15 | Yes | Yes | Yes/1 | RAM | RAM | 31 | Yes | 40 | 15 | Yes | Yes | No | Yes | Has on chip 5-bit a/d converter | 540 |
| Toshiba | T3444 | NMOS | 4/8 | 16×8 | 256×24 | Yes | 3 | 800 | Yes | 3 | Yes | 3 | Yes/1 | 8 | RAM | 16 | No | 40 | 5 | Yes | Yes | Yes | Yes | Intended for dedicated controllers | 536 |
| | T3472 | NMOS | 4/8 | 16×4 | 256×24 | Yes | 67 | 1000 | Yes | 33/360 | Yes | Yes | Yes/2 | 8 | RAM | 16 | Yes | 42 | 5 | Yes | Yes | Yes | Yes | Designed for keyboard/display interfacing | 537 |
| Western Digital | 1872 | PMOS | 4/10 | 4×32 | 512×10 | No | 37 | 150 | Yes | 6.25/12.5 | Yes | Yes | Yes/1 | 1 | RAM | 27 | No | 40 | 12 | Yes | Yes | Yes | Yes | RAM holds BCD numbers | 507 |
| General Instrument | PIC-1650 | NMOS | 8/12 | 32×8 | 512×12 | Yes | 31 | 1000 | Yes | 4/8 | Yes | Yes | Yes/1 | 2 | RAM | 32 | No | 40 | 5 | Yes | Yes | Yes | Yes | Smaller I/O and larger ROMs avail | 509 |
| Intel | 8041/8741 | NMOS | 8/8 | 64×8 | 1024×8 | Yes | 90 | 6000 | Yes | 2.5/5 | Yes | Yes | Yes/1 | RAM | RAM | 18 | Yes | 40 | 5 | Yes | Yes | Yes | Yes | Both a ROM and EPROM version are available | 531 |
| | 8048/8748 | NMOS | 8/8 | 64×8 | 1024×8 | Yes | 96 | 6000 | Yes | 2.5/5 | Yes | Yes | Yes/1 | 8 | RAM | 27 | Yes | 40 | 5 | Yes | Yes | Yes | Yes | 8748 has UV PROM | 510 |
| Mostek 1 chip F-8 | 3870 | NMOS | 8/8 | 64×8 | 2048×8 | Yes | 70+ | 4000 | Yes | 1/6.5 | Yes | Yes | Yes/4 | RAM | RAM | 32 | Yes | 40 | 5 | Yes | Yes | Yes | Yes | Software compatible with F8 | 511 |
| Motorola | 6400 | NMOS | 8/8 | 32×8 | 1024×8 | Yes | ? | 8000 | Yes | ? | Yes | ? | ? | ? | RAM | ? | Yes | ? | 5 | Yes | 1978 | 1978 | 1978 | Intended for controller use | 512 |
| | 6801 | NMOS | 8/8 | ? | ? | Yes | ? | 2000 | ? | ? | Yes | ? | ? | ? | ? | ? | Yes | 40 | 5 | No | 1978 | 1978 | 1978 | Available 1978 | 513 |
| Rockwell | PPS-8 | PMOS | 8/8 | 0 | 0 | Yes | 100 | 256/4 | No | 4/12 | No | Yes | Yes/3 | 16 | 2 | 0+ | Yes | 42 | −17/+5,−12 | Yes | Yes | No | Yes | Combination RAM/ROM/I/O support | 514 |
| | PPS-8/2 | PMOS | 8/8 | 0 | 0 | Yes | 100 | 200/4 | No | 5/15 | No | Yes | Yes/3 | 16 | 2 | 0+ | Yes | 42 | −17/+5,−12 | Yes | Yes | No | Yes | I/O chip includes clock | 515 |
| Zilog | Z8 | NMOS | 8/8 | 96×8 | 2048×8 | Yes | ? | 4000 | Yes | 0.75/? | Yes | Yes | Yes/? | ? | RAM | 32 | Yes | 40 | 5 | 1978 | 1978 | 1978 | 1978 | Has two counter/timers | 516 |
| Texas Instruments | TMS 9940 | NMOS | 2 | 128×8 | 2048×8 | No | 68 | 5000 | Yes | 2/452 | Yes | Yes | Yes/4 | 64 | RAM | 16 | No | 40 | 5 | Yes | Yes | Yes | Yes | Two versions available, one has a 2 k EPROM, the other a 2 k ROM | 530 |

1 Not applicable ? Not available 2 Externally 8 bits, internally 16 bits 3 User defined

more general-purpose units would probably be better.

Ideally, when you pick a processor with I/O lines on the same chip, you'd like to be able to configure each line as you need it. With some processors, you can configure each line to act as either an input or an output. But many processors don't have this capability—and skimming the data sheet may not uncover this deficiency.

Often, the I/O lines are already dedicated—some fixed as outputs and the rest as inputs. And, even if they are programmable, they might be programmable only on a word basis. Individual lines cannot be set as input or output. Some all-in-one circuits can be expanded beyond their limited on-chip I/O capability, but by the time you add all the necessary expansion circuits, you'll be wishing that you had used a general-purpose chip instead.

While you're checking the capabilities of the I/O lines, check the capabilities of the I/O instructions. Processors with dedicated I/O lines usually have special instructions for manipulating bits, setting mask codes and even performing operations directly on the bits in the port. General-purpose processors usually don't have any I/O port lines, but there are many specially designed support circuits available to provide both serial and parallel I/O ports.

Serial I/O capability is available only on a few processor chips but if you need only one serial port along with some parallel I/O lines you should consider a processor with serial I/O to keep the chip count minimal. Controlling the serial port is done via the program so no extra hardware is needed, except for a buffer or level shifter.

For almost all processors, data sheets claim TTL compatibility—but don't expect most MOS processors to drive more than one normalized or low-power TTL load. Older processors can't even drive that much of a load without pull-up resistors or MOS-to-TTL level shifters and buffers.

Few microprocessor spec sheets deal with noise immunity—an important spec if your processor will be used in industrial environments. Comparing input levels for peripheral circuits with the address-output levels of a certain processor may reveal little or no protection against unwanted transients. If you don't have the needed noise immunity, you will quickly discover the need when you move the prototype from the lab bench to the factory floor.

However, some CMOS processors can provide noise immunity without much strain since the signal swings typically range from the supply to ground. Of course, you can get around the noise problem by using inexpensive level shifters and pull-up resistors, but they take up valuable board space and power.

## You can also roll your own processor

Now that bit-slice chips are available, you can design your own multichip processor. A bit-slice-based processor will be two to five times faster than NMOS

## Table 3. Bit-slice families

| Company | Series | Process technology | ALU part number | ALU word size (bits) | Number of ALU instructions | Can ALU do BCD arithmetic | Maximum ALU clock rate (MHz) | General-purpose registers in ALU | ALU package size (DIP pins) | Microprogram sequencer number | Number of address bits | Maximum sequencer clock rate (MHz) | Number of sequencer commands | Sequencer stack size | Sequence package size (DIP pins) | Are parts TTL compatible | Voltages required (V) | Prototyping system available | Development software available | Specialized support circuits available | Comments | Circle Number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Advanced Micro Devices | 2900 | STTL | 2901A | 4 | 16 | No | 10 | 16 | 40 | 2909/11 | 4 | 10 | 12 | 4×4 | 28/20 | Yes | 5 | Yes | Yes | Yes | Has widest number of second sources | 517 |
| | | STTL | 2903 | 4 | 25 | No | 10 | 16 | 48 | | | | | | | | | | | | ALU has nine more instructions than 2901, including multiply and divide. | 827 |
| Fairchild | Macrologic | STTL/ CMOS | 9405/34705 | 4 | 64 | No | 10 | 8 | 24 | 9406 | 4 | 10 | 4 | 16×4 | 24 | Yes | 5 | Yes | Yes | Yes | CMOS version (34705) operates at 2 MHz | 518 |
| | 100k 8-bit | ECL | ADIU | 8 | 27 | Yes | 20 | 1 | * | * | * | * | * | * | * | * | −4,5,−2 | 1978 | 1978 | 1978 | Only 8-bit slice | 519 |
| Intel | 3000 | STTL | 3002 | 2 | 40 | No | 10 | 11 | 28 | 3001 | 9 | 10+ | 11 | 0 | 40 | Yes | 5 | Yes | Yes | Yes | Only 2-bit ALU available | 520 |
| Monolithic Memories | 5700/6700 | STTL | 57/6701 | 4 | 32 | No | 5 | 16 | 40 | 6710 | 9 | 10+ | 8 | 0 | 40 | Yes | 5 | Yes | ? | No | Has double-addressing capability | 521 |
| Motorola | 10800 | ECL | 10800 | 4 | 100+ | Yes | 20 | 0 | 48 | 10801 | 4 | 20 | 16 | 4×4 | 48 | No | −2,−5.2 | Yes | Yes | Yes | Fastest bit slice available | 522 |
| National Semiconductor | IMP-4 | PMOS | 00A/520 | 4 | 8 | No | 5.714 | 20 | 24 | 4A/521 | 4 | 5.714 | 100+ | in ALU | 24 | Yes | +5,−12, | Yes | Yes | No | Need external register file | 523 |
| | IMP-8 | PMOS | 00A/520 | 4 | 8 | No | 5.714 | 20 | 24 | 8A/521 | 8 | 5.714 | 100+ | in ALU | 24 | Yes | +5,−12 | Yes | Yes | No | Uses IMP-4 ALUs with big ROM | 524 |
| | IMP-16 | PMOS | 00A/520 | 4 | 8 | No | 5.714 | 20 | 24 | 16A/521 | 16 | 5.714 | 100+ | in ALU | 24 | Yes | +5,−12 | Yes | Yes | No | Two development systems available | 525 |
| Texas Instruments | SBP-0400A | I²L | SBP 0400 | 4 | 512 | No | 5 | 10 | 40 | 74S482 | 4 | 20 | 64 | 4×4 | 20 | Yes | Current | Yes | No | No | Has pipeline register | 526 |
| | SBP-0401A | I²L | SBP 0401 | 4 | 512 | No | 5 | 10 | 40 | 74S482 | 4 | 20 | 64 | 4×4 | 20 | Yes | Current | Yes | No | No | Does not have pipeline register | 527 |
| | 74S481 | STTL | 74S481 | 4 | 24,780 | No | 10 | 0 | 48 | 74S482 | 4 | 20 | 64 | 4×4 | 20 | Yes | 5 | Yes | No | Yes | Very flexible instruction set | 528 |

*In definition stage

processors since just about every slice is bipolar and takes under 100 ns to execute an instruction. Right?

Wrong. The 100 ns refers to a microinstruction—not a complete instruction as in microprocessors.

In a microprocessor, microprograms tell the logic circuits in the chip how to route data and set up the ALU to perform an operation. In a bit slice, you must program these instructions into the microprogram memory. (The microprogram memory consists of a ROM array that is not part of the addressable RAM or major program space.)

Normally, a programmed bit-slice processor may require anywhere from 100 to 1024 words of microprogram memory to control all the operations. Each word, in turn, can consist of many bits since it can be used to control more than just the processor slice. It can also control peripherals, memories and other processor subfunctions. Depending on the application, a microprogram-control word can be from about 10 to 60 bits long.

The advantages of microprogramming your own processor versus buying a programmed chip include the ability to write your own macroinstructions and thus customize for your application.

With microprogramming, you don't need as much control hardware either—software does more of the peripheral control than with a macroprogrammed processor. This proves invaluable in applications requiring in excess of tens of thousands of units. Microprogramming also presents a good alternative when a system must be emulated or when critical short routines must be executed rapidly.

However, microprogramming does have a drawback. Since the programmer works very closely with the timing relationships of the machine itself and on a machine-language level (the 1's and 0's), developing a program is difficult. Each application requires a different microprogram, with a different instruction set, so designs cannot be transferred readily. Nor can software design aids, most of which are geared for a fixed instruction set, be used with a bit-slice processor's alterable macroinstruction set.

### What's happening

Even in the short interval since ELECTRONIC DESIGN presented its microprocessor roundup (ED No. 14, July 5, 1977, p. 26), new microprocessors and microcomputers have been introduced.

For example, Texas Instruments claims a first with its TMS9940—the first 16-bit microcomputer chip. It is instruction compatible with the other TMS9900 products except for four instructions. The development version puts a 2048-byte erasable PROM and the processor on the same chip, while the production version puts a mask-programmed ROM on the chip.

Drifting down to the low-end microcontrollers: Both Toshiba and Panasonic (Matsushita) have introduced 4-bit processors for dedicated-control applications. Toshiba offers the T3444 and 3472 processors for high-speed data handling and man/machine interfacing, respectively. Preprogrammed versions of the T3444 are available as floppy-disc controllers and cassette controllers.

Panasonic's MN1400 family consists of four models, each with a different amount of on-board memory and different features. The MN1499 is the prototyping unit and has provisions for external memory and 75 instructions.

The other newcomer is the 4-bit S2000 developed by American Microsystems. It is a display-oriented microcomputer with a 1 k × 8 on-chip ROM and drivers for either a LED or vacuum fluorescent display. Meanwhile, more details have finally come out about the 2903, an enhanced version of the 2901A bit slice from Advanced Micro Devices. The 2903 has nine additional instructions—unsigned multiply, two's complement multiply, increment by one or two, sign/magnitude two's complement, two's complement multiply correction, single length normalize, double length normalize and first divide op., two's complement divide, and two's complement divide, correction, and remainder. No other processor slice has multiplication or division routines.

Products that will appear in early 1978 include an 8-bit ECL processor slice currently being developed by Fairchild, the Z8 microcomputer from Zilog, and a 2-k × 8 version of the 8048 from Intel.

More details of the Zilog Z8 all-in-one microcomputer have been released since the product was brought to light in the ELECTRONIC DESIGN roundup. The 8-bit processor chip includes a 96-byte RAM, where each byte can act as an accumulator. Data can be transferred back and forth to any RAM word by the I/O ports or ALU. Although the Z8's instruction set has fewer basic instructions than the Z80, more variations are possible. So the number of op codes increases.

Of the 32 I/O lines on the Z8, 16 are set up to be individual-line programmable as input or output, eight lines are set to be byte-programmable as input, output or bidirectional, and eight can be divided into 4-bit sections, each of which can be either input, output or bidirectional lines. Software controls all the port I/O lines and the control commands can be either mask-programmed on the processor chip or stored in external memory.

External memory for the Z8 can be expanded so that the processor addresses both 65 kbytes of ROM and another 65 kbytes of RAM or ROM. The processor also has an on-chip prioritized interrupt structure that is software-controllable. Up to six interrupts can be handled without any support circuits.

The processor executes its instructions fairly fast —the shortest instruction can run in 0.75 $\mu$s and the longest in 1.9 $\mu$s.

Also on the Z8 chip are two software-controllable 8-bit counter/timers that can interrupt the processor. One timer has an 8-bit prescaler that is also software programmable so that large timing loops can be used.

Zilog is also readying the Z8000, an NMOS 16-bit microprocessor with the equivalent processing power of a minicomputer such as the 11/70 made by Digital Equipment Corp. (Maynard, MA). The Z8000 will have a RAM-addressing capability of millions of bytes (with the use of a special memory-expander chip) and have advanced instructions such as hardware multiply and divide.

The processor has been optimized to execute compiler-generated code, according to company officials. It can perform instructions in less than 1 $\mu$s (for the shortest instruction). Still, the processor instructions will be compatible with the assembly-level mnemonics already in use on the Z80. A translator program will also by available to transfer assembly-level Z80 programs into Z8000 op code.

Both the Z8 and Z8000 will not be available until 1978, with the Z8 scheduled for early 1978 and the Z8000 for late 1978.

This year has been a good one for alternate-source agreements. Even Intel has selected a few companies to whom it will provide masks for its 8048 and 8085 microprocessors. Monolithic Memories has finally found an alternate source—ITT—for its 5701/6701 bit slice just as it starts manufacturing the 2901A bit slice as an alternate source to AMD.

In the 4-bit area, Texas Instruments has quietly postponed its introduction of NMOS equivalents to its TMS-1000 family. But even more quietly, TI has announced a CMOS equivalent. The only 4-bit CMOS processor on the market, it should find a home in many portable and battery-operated items.

### Take a close look at some units

Most of this year's development activity has been in 8-bit microprocessors and microcomputers. The Mostek 3870 single-chip microcomputer is in a head-to-head confrontation with the Intel 8048. Both units have many of the same features, with the Mostek chip

# Processor alternate source directory

| Generic type number | Data word size (bits) | Technology | Original source | Alternate sources | Data manual page number |
|---|---|---|---|---|---|
| 1600, 1610 | 16 | NMOS | General Instrument | EM&M Semiconductor | 164 |
| 1650, 1655 | 8 | NMOS | General Instrument | EM&M Semiconductor | 106 |
| 1802, 1803 | 8 | CMOS | RCA | Hughes & Solid State Scientific | 130 |
| 1872 | 4 | PMOS | Western Digital | None | 116 |
| 2650 | 8 | NMOS | Signetics | Advanced Memory Systems National Semiconductor | 144 |
| 2900 | 4 | STTL | Advanced Micro Devices | Fairchild, Monolithic Memories, Motorola, National Semiconductor, Raytheon, Sescosem, Signetics | 180 |
| 3000 | 2 | STTL | Intel | Signetics | 176 |
| 3850 | 8 | NMOS | Fairchild | Mostek, Motorola | 132 |
| 3859 | 8 | NMOS | Fairchild | Discontinued | — |
| 3870 | 8 | NMOS | Mostek | Fairchild, Motorola | 110 |
| 4040/4004 | 4 | PMOS | Intel | National Semiconductor | 124 |
| 5701/6701 | 4 | STTL | Monolithic Memories | ITT Semiconductor | 182 |
| 6100 | 12 | CMOS | Intersil | Harris Semiconductor | 154 |
| 6400 | 8 | NMOS | Motorola | None | — |
| 65XX | 8 | NMOS | MOS Technology | Rockwell, Synertek | 138 |
| 6800, 68A00, 68B00 | 8 | NMOS | Motorola | American Microsystems, Fairchild, Fujitsu, Hitachi, Sescosem Thompson CSF | 140 |
| 6801 | 8 | NMOS | Motorola | None* | — |
| 6802 | 8 | NMOS | Motorola | None | 142 |
| 6809 | 8 | NMOS | Motorola | None* | 118 |
| 7150 | 4 | PMOS | ITT Semiconductor | None | |
| 8000 | 8 | PMOS | General Instrument | AEG, SGS-ATEs | 112 |
| 8008 | 8 | PMOS | Intel | None | 148 |
| 8035, 8048, 8748 | 8 | NMOS | Intel | Advanced Micro Devices, NEC and Signetics | 108 |
| 8041, 8741 | 8 | NMOS | Intel | None | 120 |
| 8080A | 8 | NMOS | Intel | Advanced Micro Devices, NEC, National Semiconductor, Signetics, Texas Instruments | 134 |
| 8085 | 8 | NMOS | Intel | Advanced Micro Devices, NEC | 136 |
| 8900 | 16 | PMOS | National Semiconductor | None | 166 |
| 9002 | 8 | NMOS | Electronic Arrays | Discontinued | — |
| 9080 | 8 | NMOS | Advanced Micro Devices | Actually an alternate source for 8080 | 134 |
| 9405, 34705 | 4 | STTL/CMOS | Fairchild (Macrologic) | Signetics | 178 |
| 9440 | 16 | $I^2L$ | Fairchild | None | 160 |

*This product is still in development

offering double the ROM capacity and the Intel device a larger instruction set.

Intel introduced the 8048 and 8085 processor families last year, with a flurry of industry firsts. A pin-compatible unit with the 8048, the 8748 has all the features of the 8048, but instead of containing 1024 bytes of mask-programmable ROM, the 8748 contains 1024 bytes of ultraviolet, erasable, programmable read-only memory. Not only is the PROM included on the chip, but the chip itself can operate from a single 5-V supply—another first.

Support for the 8048 and 8085 comes from a family of 8-bit auxiliary chips, including the 8155, a 256 × 8 static RAM with programmable 14-bit timer and 22 lines of programmable I/O—all on one chip. There's also the 8355/8755, a 2048 × 8 ROM with 16 lines of programmable I/O, or a 2048 × 8 UV EPROM with 16 lines of programmable I/O. Both the 8155 and 8355/8755 also help simplify the interface between Intel's other new processor, the 8085, and the outside world.

The 8085 is a souped-up 8080A with two more instructions, some new control lines, an on-chip clock oscillator, and a faster instruction-execution speed. However, to get the additional control capability while keeping the processor in its 40-pin package, something

| Generic type number | Data word size (bits) | Technology | Original source | Alternate sources | Data manual page number |
|---|---|---|---|---|---|
| 9900 | 16 | $I^2L$/NMOS | Texas Instruments | American Microsystems (NMOS version) | 170 |
| 9940 | 16 | NMOS | Texas Instruments | None* | 114 |
| 9980 | 16 | NMOS | Texas Instruments | None | 172 |
| 10800 | 4 | ECL | Motorola | None | 184 |
| 14500 | 1 | CMOS | Motorola | None | 122 |
| 8X300 | 8 | STTL | Signetics | None | 128 |
| 74S481 | 4 | STTL | Texas Instruments | None | 188 |
| 100 K | 8 | ECL | Fairchild | None* | 98 |
| COPS | 4 | PMOS | National Semiconductor | None | — |
| F8 | 8 | NMOS | Fairchild | See 3850 | 158 |
| F100L | 16 | Bipolar | Ferranti | None | 190 |
| IMP-4, 8, 16 | 4, 8, 16 | PMOS | National Semiconductor | Rockwell | |
| Macrologic | 4 | STTL/CMOS | Fairchild | See 9405, 34705 | — |
| MCP-1600/WD-16 | 16 | NMOS | Western Digital | None | 174 |
| Micromachine | 8 | NMOS | Fairchild | See 3859 | — |
| mN601 | 16 | NMOS | Data General | None | 162 |
| MN1400 | 4 | NMOS | Panasonic | None | 90 |
| MN1610 | 16 | NMOS | Panafacom | None | 168 |
| PACE | 16 | PMOS | National Semiconductor | Rockwell | |
| PPS-4 | 4 | PMOS | Rockwell | National Semiconductor | 126 |
| PPS-4/1 | 4 | PMOS | Rockwell | None | 104 |
| PPS-4/2 | 4 | PMOS | Rockwell | None | 126 |
| PPS-8 | 8 | PMOS | Rockwell | National Semiconductor | 152 |
| PPS-8/2 | 8 | PMOS | Rockwell | None | 152 |
| S2000 | 4 | NMOS | American Microsystems | None | 88 |
| SBA | 1 | NMOS | General Instrument | None | 84 |
| SBP0400A/ 0401A | 4 | $I^2L$ | Texas Instruments | None | 186 |
| SC/MP, SC/MPII | 8 | NMOS/PMOS | National Semiconductor | Rockwell, Signetics, Western Digital | 150 |
| SMS-300 | 8 | STTL | Scientific Microsystems | Signetics | — |
| SX200 | 4 | PMOS | Essex International | None | 96 |
| T3190 | 12 | PMOS, NMOS | Toshiba | None | 156 |
| T3444 | 4 | NMOS | Toshiba | None | 92 |
| T3472 | 4 | NMOS | Toshiba | None | 94 |
| TMS1000, 1100, 1200, 1300 | 4 | CMOS, NMOS or PMOS | Texas Instruments | Motorola for CMOS version | 86 |
| uCOM 42 | 4 | PMOS | NEC | None | 100 |
| uCOM 43, 44, 45 | 4 | PMOS | NEC | None | 102 |
| Z8 | 8 | NMOS | Zilog | None* | — |
| Z80 | 8 | NMOS | Zilog | Mostek, Sharp | 146 |

had to be forfeited.

So the 8080A's totally separate data and address buses had to go. The 8085 has the eight most-significant address bits brought out to their own pins, but the eight least-significant address bits are multiplexed on the eight data-bus lines. So that a complete system can be formed with only two chips, the 8355/8755 and the 8155 have internal address latches that can hold the first eight bits of the address.

The 8085 contains the equivalent of the bus controller and clock generator on its chip. All the 8080A's software is compatible with the 8085. The only changes you may have to make are in timing loops since the time will change with the higher clock frequency. The processor chips, of course, are not pin-compatible, so upgrading the system really means redesigning the circuit board. However, all chips in the 8085 can operate from a single 5-V supply.

Mostek's 3870 doesn't have any new specialized support circuits, but it is compatible with all the older F8 processor circuits and software. So popular is the 3870, in fact, that Fairchild, the original developer of the F8, has scratched plans to market its own one-chip microcomputer, the 3859. Instead it will alternate-source the 3870, currently the only 8-bit microcomputer with 2048 bytes of on-chip storage.

## Table 4. Directory of $\mu$Ps by vendor

| Manufacturer | Microprocessor model number |
|---|---|
| AEG | Series 8000* |
| Advanced Micro Devices | 2900, 8048*, 8080*, 8085* |
| Advanced Memory Systems (Intersil) | 2650* |
| American Microsystems | 6800*, 9900*, S2000 |
| Data General | mN601 (microNova) |
| EM&M Semi | CP1600*, 1610*, 1650*, 1655* |
| Essex International | SX200 |
| Fairchild | Macrologic (9405), 100K, 2900*, 3850(F8), 3870*, 6800*, 9440 |
| Ferranti | F100-L |
| Fujitsu | 6800* |
| General Instrument | CP1600, 1610, 1650, 1655, SBA |
| Harris Semiconductor | 6100* |
| Hitachi | 6800* |
| Hughes | 1802* |
| Intel | 3000, 4004/4040, 8008, 8048, 8080A, 8085 |
| Intersil | IM6100 |
| ITT | 1600*, 5701/6701*, 7150 |
| Monolithic Memories | 2900*, 5701/6701 |
| MOS Technology | 65XX |
| Mostek | 3850*, 3870, Z80* |
| Motorola | 2900*, 3850*, 3870*, 6400, 6800, 6801, 6802, 6809, 10800, 14500 |
| National Semiconductor | 2650*, 2900*, 4004/4040*, 8080A* COPS, IMP-4, 8, 16, INS8900, PACE, PPS-4*, PPS-8* |
| NEC | 8048*, 8080A*, uCOM 42, 43, 44, 45 |
| Panafacom | MN1610 |
| Panasonic | MN1400 |
| Philips | 8080A* |
| RCA | CDP1802 |
| Raytheon | 2900* |
| Rockwell | 65XX*, PPS 4, 4/1, 4/2, 8, 8/2, SC/MP II* |
| SGS-ATES | Series 8000* |
| Scientific Microsystems | SMS-300 |
| Sharp | Z80* |
| Siemens | 8080A* |
| Signetics | 8X300, 2650A, 2900*, 8048*, 8080A*, 8085*, 9405*, 34705*, SMS-300* |
| Solid State Scientific | 1802* |
| Synertek | 65XX* |
| Texas Instruments | 74S481, 8080A*, SBP-0400A/0401A, TMS-1000, TMS-9900, 9940, 9980 |
| Thomson CSF/Sescosem | 2900*, 6800* |
| Toshiba | T3190, T3444, T3472 |
| Western Digital | 1872, MCP1600/WD-16, SC/MP II* |
| Zilog | Z8, Z80, Z8000 |

*Alternate source product

Meanwhile, no 16-bit processor has captured a dominant market share. The biggest 16-bit trend is price reductions. General Instrument, for instance, recently introduced an $8 version (100 qty) of its CP1600 16-bit microprocessor. The low-cost 1610 is totally pin and software-compatible. Performance, however, was traded off for low cost—the 1610 operates at a 2-MHz maximum clock instead of 4 MHz, and comes in a plastic—not ceramic—40-pin DIP.

National Semiconductor has upgraded its PMOS 16-bit microprocessor, the PACE, with an NMOS equivalent, the INS8900, which performs better for the same price. (National, however, isn't pushing the PACE any more and rumors indicate it will be discontinued in the near future.)

Ferranti's bipolar 16-bit processor, the F100L, is not well known in the U.S. But with its rapid clock speed, it can provide high performance, and since it's a bipolar device, it can operate over the full military temperature range.

The only other 16-bit bipolar processor is the SBP9900 from TI. The SBP9900 and its NMOS equivalent, the TMS9900, as well as a "shrink" (16-bit internal data bus, 8-bit external) version, the TMS9980, are all software-compatible with each other and with TI's 990 series of minicomputers. Software-development costs for the 9900 can be kept down since the 990 minicomputers have an extensive program library.

The same is true for the mN601 (microNova) from Data General. The 16-bit mN601 is software-compatible with the company's Nova series of minicomputers, so it has a vast repertoire of applications software. Also available are all the peripheral devices and interface circuits already designed for the Nova minicomputers.

Fairchild has announced a bipolar ($I^3L$) 16-bit machine, the 9440, that emulates the Nova 1200 minicomputer-instruction set. However, due to patent-infringement lawsuits brought on by Data General (the developer of the Nova), the 9440 will not be available for a while.

Getting all the hardware together for a prototype system is probably the easier half of system design. The harder half is getting the software to control the system. Writing the code to control the microprocessor, microcomputer or bit slice can take about double the time you typically allot for it—and possibly cost as much as $100,000. However, the software cost can be amortized by the number of systems produced since it is a one-shot expense.

### Speed program development with design aids

Almost every manufacturer of a processor product —and several other manufacturers—offer some form of development system to help you develop both hardware and software for the processor. However, features vary considerably from one manufacturer's system to the next. Depending on the features each system offers, be prepared to spend anywhere from $6000 to $15,000 for a system that permits you to program only one manufacturer's processor.

Only one or two systems can program more than one manufacturer's processor—that capability will cost you about $25,000. But what do you get for the money? Typically you're buying a microcomputer with about 32 kwords of RAM, several kwords of ROM, a dual floppy-disc system, a CRT terminal and a printer, paper-tape reader/punch and possibly a PROM programmer. The floppy-disc memory and the ROMs contain most of the control programs needed to develop your own programs.

If you don't want to invest in major equipment such as a development system, you can use a computer (usually a large one) to develop your programs. But depending on how long it takes to develop your program, going this route could be more expensive in the long run.

Typical programs you would use during a program-development cycle include an assembler, editor and a compiler. There are also large programs written in Basic, variations of PL/1 and Fortran that are used first to develop programs in these higher-level languages, then to translate the instructions down to the actual operation code needed to control the processor. These languages, though, generate more code than is necessary. But that's the price you pay if you don't want to work in the assembly language of the processor itself.

An assembler is a program that translates assembly-language statements into machine code that your processor can execute. However, there are many types of assemblers, each with its idiosyncrasies.

Essentially, an assembler reads statements written in mnemonic or symbolic form and produces the op codes necessary to run the processor. Errors due to misuse of the assembly language can be detected by the better assemblers and pointed out before the code is programmed into the processor.

Most assemblers offered require two passes through the mnemonics to be assembled before they complete their job. Usually, on the first pass the assembler assigns addresses to all jump symbols and labels used in the program. On the second pass, all instructions are converted into binary, with all the correct jump locations inserted into the proper places.

More efficient assemblers require only one pass through the mnemonic listings to do the job completely, which cuts the time needed to obtain binary codes. Many of the assemblers also offer the convenience of transferring the binary codes directly to a paper tape or PROM, thus providing a permanent record of the program and putting it in a form easy for the processor to digest.

The more powerful assemblers often include another feature, called macro capability. This feature permits short, oft-used mnemonic routines to be represented by a new mnemonic that can then be substituted into the program under development. When the final program is assembled, the macroassembler automatically substitutes the proper code sequence.

Editor programs permit you to write programs in assembly language and to change them at will with simple commands. They are available either on time-sharing systems or on most of the purchasable development systems. With editors, you can add documentation; store, combine and retrieve programs; and deliver programs to paper tape or printers.

The coding process is usually completed with a loader. Usually stored in ROM, a loader transfers the binary programs from paper tape into RAM, from ROM into RAM or from some form of magnetic storage into the computer. A relocating loader automatically readjusts program addresses and loads the resulting instructions into the computer. Another feature some loaders offer is a linking capability, which lets you use routines with undefined labels. Missing label definitions are filled in as the program is loaded.

Compiler programs let you develop your program in a higher-level language. Since many programmers are familiar with languages such as Fortran or PL or Basic, this capability cuts development time. The biggest factors in deciding whether or not to use a high-level language are turnaround time and memory size. (Code generated by high-level languages can require about 20 to 50% more memory space than assembly-language-generated programs.)

In addition to the basic development aids, simulators, emulators and debuggers are usually mandatory to track down errors that might still remain in the code. For the same reason hardware emulators and in-circuit emulation are handy capabilities to have in a development system.

## Don't overlook the learning aids

Anyone interested in designing μP-based equipment is immediately confronted with a bewildering variety of evaluation kits, learning aids, design aids, teaching aids and programming aids. Because the μP market has grown so rapidly, there are no exact definitions for the aids.

"Aids" currently range from under $200 to well over $20,000 depending on the features. But one subgroup, from $100 to $900, permits just about anyone to get "hands on" experience with a particular processor.

Almost all the inexpensive microprocessor design aids are aimed at 8-bit devices—there are no 4-bit microprocessor or microcomputer design aids. There are, however, several inexpensive evaluation kits for the two-bit Series 3000 bit slice and the 2900 4-bit slice.

For the 8-bit processors, Intel offers several kits as well as preassembled boards for its 8080A and 8085. Motorola offers several kits for its 6800. National Semiconductor offers a kit and some boards for the SC/MP. RCA offers a designer's kit for its 1802. Intersil offers a learning system for its 6100. MOS Technology offers a system for its 6502. Both Fairchild and Mostek offer boards for the F8. Zilog offers a family of boards for the Z80. Signetics offers a board for the 2650 and another for its 8X300. American Microsystems offers several kits for the 6800. And the list of "offerings" keeps growing as more processors are developed.

Software for microprocessors can also be as confusing to select as design aids. Basically, software is available in resident and nonresident forms—and there are several hundred variations in each form. Resident software consists of programs written in the instructions of a specific microprocessor and ready to run on a system that uses that micro. Nonresident software consists of programs that run on one processor (typically, a minicomputer or larger processor) to help you develop the software of another processor (typically at $\mu$P).

Most microprocessor-development systems, which range from the $100 kit to the $20,000 work station, come with some form of resident software—if the system is designed to develop code for one type of microprocessor. Some development stations, though, don't have truly resident software. For example, the 8002 universal microprocessor development system from Tektronix (Beaverton, OR) uses the 2650 as the main controller, but it can also be used to develop code for the 8080A, 6800, Z80 and TMS9900 processors.

For less expensive systems, the software included is usually minimal and often stored in ROMs (sometimes referred to as firmware). The more expensive systems usually contain either a paper-tape reader or a floppy-disc drive to permit large programs to be entered and help you develop software.

Firmware on most of the smaller development systems usually consists of a monitor program that permits you to use either a TTY or CRT terminal with the board and write your programs in machine code. Such commands as examine a memory location, change its contents and examine the next location, start execution at a specific location, and establish breakpoints to allow selected program sections to be executed are available on most monitors.

However, if you want the convenience of working in assembly language, you'll have to use a fairly large development system, since most assembly-language programs require several thousand bytes of RAM. Extensive program-development systems are available from most processor vendors, but other alternatives are available from many companies. Futuredata Computer Corp. (formerly Microkit) in Santa Monica offers a flexible system that provides assembly-language capability for the 8080, Z80 and the 6800. Other companies offering systems include muPro (Cupertino, CA) and Wintek (Lafayette, IN). The muPro System 80, intended for 8080A users, not only lets you develop programs for the 8080A, but also contains an in-circuit emulator, a field-test system, and an 8080 microcomputer. The system uses a language developed by muPro called BSAL-80, a nonmnemonic language.

The Wintek systems use the 6800 and, since they are designed on a standard 44-pin circuit card (dual 22-pin), can be installed in a standard card rack.

Although not quite design aids, some of the newer microcomputer systems such as the PET made by Commodore (Palo Alto, CA) and the TRS-80 made by Radio Shack (Fort Worth, TX) come ready-to-use and let you write programs in Basic and load or store the programs on a magnetic-cassette transport. The 6502-based PET has an IEEE-488 interface bus, so it can figure in many instrumentation applications. What's more, the price for the processor with integral CRT, 12 k of ROM, 4 k of RAM, cassette deck and 70-key keyboard is only $595.

The Z80-based Radio Shack system also includes 4 k of RAM and 4 k of ROM, but has a separate video monitor, cassette deck and keyboard/CPU as well.

### Don't want hardware? Try time-sharing

The accessibility of large computers and time-sharing services has sparked the processor manufacturers to develop higher-level programs that can run on the large machines and be shared by hundreds of users at the same time. Programs are now available in machine language, forms of PL/1, Fortran and Cobol to permit you not only to develop programs in higher languages but also to get processor-compatible code when you're done.

Such programs are usually not as efficient as assembly-language programs. However, some time-sharing companies have helped reduce the inefficiencies by developing their own software for program development. For instance, the Boston Systems Office uses large minicomputers in its time-sharing network, and develops its own software in the minicomputers' assembly language. What this means is more efficient use of the computer's time and thus smaller time-sharing bills.

Some of the other larger companies that offer $\mu$P-development programs include National CSS (Norwalk, CT), General Electric Information Services (Bethesda, MD), First Data (Waltham, MA), United Computer Systems (Kansas City, MO) and Tymshare (Cupertino, CA). Each company's original programs will offer different features, so you must get each company's manual and compare features to make sure you get what you need.

A high-level system often lets you develop the program for your system before the hardware can be prototyped—sometimes even before a dollar is spent for hardware—since complete simulators and emulators are available for many processors. Cross-assemblers are commonly available in Fortran, versions of PL/1 and assembly language. Some assemblers even provide more than one machine-code format for absolute and relocatable code listings.

Compiler and integrator programs are available in PL/M, PL/W, PL/Z, MPL, Fortran, Cobol, Forth. And if that isn't enough alphabet soup, there are at least as many that have gone unnamed.

However, all isn't roses with time-sharing services —computer time is expensive. If you're concerned with CPU time, keep a careful watch over the use of a terminal with a time-shared computer. And CPU time isn't the only big expense. Storage space reserved, output time and communication links, and manpower will also cost you dearly.

Software costs can vary widely, depending on the design approach taken by the programmer. Some programmers can also keep the hardware cost down by transferring some of the hardware into software routines handled by the microcomputer. Often, the more functions you can assign to software, the more flexible the final system. Of course, you shouldn't burden the processor with so many little things that it can't do the job you originally wanted it for.

Software cost can get bothersome if you saddle capable programmers with a new and totally unfamiliar instruction set. The learning curve starts at the peak cost and must be given time to work its way back to average as the programmers become familiar with each processor's language. And with the approximately 40 languages that have appeared the last six years, it will take a while before they catch up.

When you start a microprocessor development program, don't just consider the circuit hardware and the programming language—look at the development system itself. One of the most overlooked items is some form of high-speed, hard-copy output device. Sure, the ASR-33 teletypewriter is the industry workhorse—but it's too slow for many program-development uses.

Say you've spent the day working on a program and you want to get a printout of your 2000-line program with all comment notes to check out. If you're using a 10 to 50 character-per-second printer, forget it. Assuming each line has about 50 characters and the printer chugs away at 10 cps, you'll have to wait about three hours for the listing. With a 50-cps printer the delay is less—only half an hour.

Does your system use a cassette, cartridge or disc-file system? Floppy-disc operating systems usually offer the fastest performance, but they're also the most expensive. But in a dual-disc system one disc holds main operating programs, while the other stores user programs. This method helps reduce access time, while providing a more flexible development system.

If there is an ideal development system, it hasn't been put on the market yet. Ideally, the basic hardware should include a universal CPU, a full complement of RAM and ROM-based bootstrap-loader programs, general-purpose interfaces for terminals, printers, disc drivers, PROM programmers, paper-tape readers/punches, etc., a CRT terminal with a few programmable keys and a high-speed printer capable of 50 to 100-cps hard-copy outputs. Of course, the floppy discs that come with the system should hold the development programs you'll need to write the software for your system. ■■

## Need more information?

Listed below are the original-source microprocessor manufacturers and most of the alternate source vendors. For additional companies consult ELECTRONIC DESIGN's Gold Book under IC, Central Processing Unit and Computers, Digital, Micro.

AEG, 6 Frankfurt 70, AEG Hochhaus, Federal Republic of Germany. **Circle No. 405**

Advanced Memory Systems, 1215 Hammerwood Rd., Sunnyvale, CA 94086. (408) 734-4330. **Circle No. 406**

Advanced Micro Devices, 901 Thompson Pl., Sunnyvale, CA 94086. (408) 732-2400. **Circle No. 407**

American Microsystems, 3800 Homestead Rd., Santa Clara, CA 95051. (408) 246-0330. **Circle No. 408**

Data General, Route 9, Southboro, MA 01772. (617) 485-9100. **Circle No. 409**

Electronic Memories & Magnetics, Semiconductor Div., 12621 Chadron Ave., Hawthorne, CA 90250. (213) 644-9881. **Circle No. 410**

Essex International, 564 Alpha Dr., Pittsburgh, PA 15238. (412) 963-9322. **Circle No. 411**

Fairchild, 1725 Technology Dr., San Jose, CA 95110. (408) 998-0123. (MOS) **Circle No. 412**

Fairchild Semiconductor, 464 Ellis St., Mountain View, CA 94042. (415) 962-3816. (Bipolar). **Circle No. 413**

Ferranti Ltd., Western Rd., Bracknell, Berkshire RG12 1RA, England. **Circle No. 414**

Fujitsu Ltd., 6-1, Marunouchi 2 Chome, Chiyoda-ku, Tokyo, Japan. **Circle No. 415**

General Instrument, 600 W. John St., Hicksville, NY 11802. (516) 733-3130. **Circle No. 416**

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901. (305) 727-5400. **Circle No. 417**

Hitachi, Ltd., Nippon Building, No. 6-2, 2-Chome, Ohtemachie, Chiyoda-ku, Tokyo 100, Japan. **Circle No. 418**

Hughes, Solid State Div., 2601 Campus Dr., Irvine, CA 92715. (714) 752-6396. **Circle No. 419**

ITT Semiconductor, 74 Commerce Way, Woburn, MA 01801. (617) 935-7910. **Circle No. 420**

Intel, 3065 Bowers Ave., Santa Clara, CA 95051. (408) 246-7501. **Circle No. 421**

Intersil, 10900 N. Tantau Ave., Cupertino, CA 95014. (408) 996-5000. **Circle No. 422**

MOS Technology, Valley Forge Corporate Center, 950 Rittenhouse Rd., Norristown, PA 19401. (215) 666-7950. **Circle No. 423**

Monolithic Memories, 1165 E. Arques Ave., Sunnyvale, CA 94086. (408) 739-3535. **Circle No. 424**

Mostek, 1215 W. Crosby Rd., Carrollton, TX 75006. (214) 242-0444. **Circle No. 425**

Motorola Semiconductor, 3501 Ed Bluestein Blvd., Austin, TX 78721. (512) 928-2600. (MOS) **Circle No. 426**

Motorola Semiconductor, 5005 E. McDowell Rd., Phoenix, AZ 85008. (602) 244-6900. (Bipolar). **Circle No. 427**

NEC Microcomputers, 5 Militia Dr., Lexington, MA 02173. (617) 862-6410. **Circle No. 428**

National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95050. (408) 737-5000. **Circle No. 429**

Panafacom Ltd., 2-10-16 Jiyuzaoka, Mezuro-ku Tokyo, Japan 152. **Circle No. 430**

Panasonic, 50 Meadowland Parkway, Secaucus, NJ 07094. (201) 348-7276. **Circle No. 431**

Philips Industries, Electronic Components and Materials Div., P.O. Box 523, Eindhoven, the Netherlands. **Circle No. 432**

RCA, Box 3200, Route 202, Somerville, NJ 08876. (201) 685-6423. **Circle No. 433**

Raytheon, 350 Ellis St., Mountain View, CA 94040. (415) 968-9211. **Circle No. 434**

Rockwell International, P.O. Box 3669, RCOI-Dept. 720, Anaheim, CA 92803. (714) 632-2321. **Circle No. 435**

SGS-ATES, Via C Olivetti 1/20041, Agrate Brianza, Italy. **Circle No. 436**

Scientific Microsystems, 520 Clyde St., Mountain View, CA 94043. (415) 964-5700. **Circle No. 437**

Sharp, 22-22 Nagaike-Cho, Abeno-ku, Osaka, 545, Japan. **Circle No. 438**

Siemens AG, Central Information Dept., Oskar-von-Miller Ring 18, D-8000 Munchen 2, Federal Republic of Germany. **Circle No. 439**

Signetics, 811 E. Arques Ave., Sunnyvale, CA 94086. (408) 739-7700. **Circle No. 440**

Solid State Scientific, Montgomeryville Industrial Park, Montgomeryville, PA 18936. (215) 855-8400. **Circle No. 441**

Synertek, 3050 Coronado Dr., Santa Clara, CA 95051. (408) 241-4300. **Circle No. 442**

Texas Instruments, 13500 North Central Expressway, M/S 308, Dallas, TX 75222. (214) 238-2011. **Circle No. 443**

Thomson-CSF, Sescosem, 101 Boulevard Murat, 75781 Paris Cedex 16, France. **Circle No. 444**

Toshiba Transistor Works, 1 Komukai Toshiba-cho, Kawasaki-shi Kanagana-ken, Japan. **Circle No. 445**

Western Digital, 3128 Red Hill Ave., Newport Beach, CA 92663. (714) 557-3550. **Circle No. 446**

Zilog Microcomputers, 10460 Bubb Rd., Cupertino, CA 95014. (408) 446-4666. **Circle No. 447**

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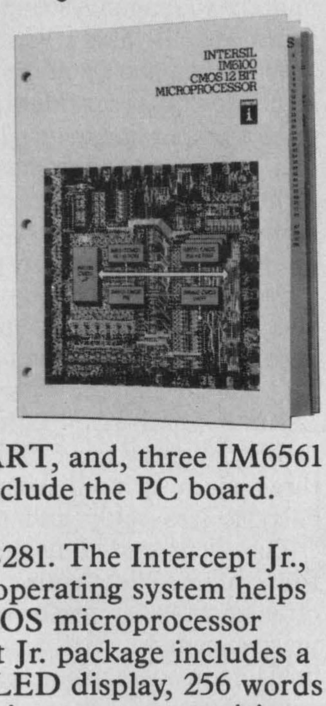


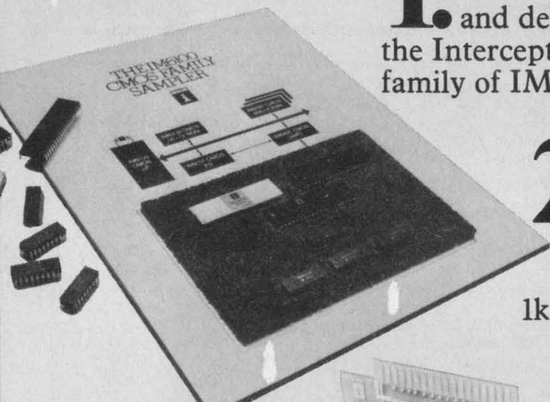


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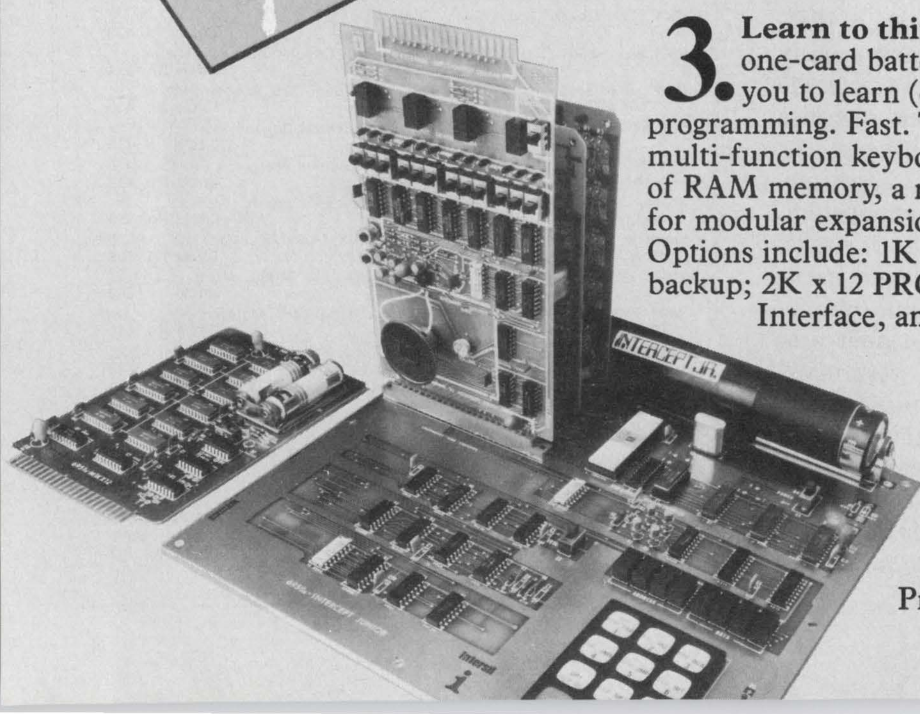


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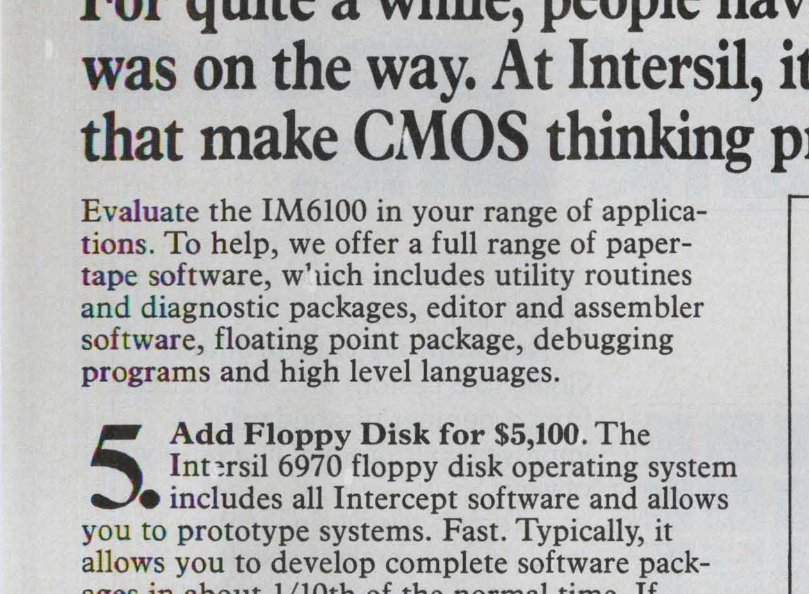


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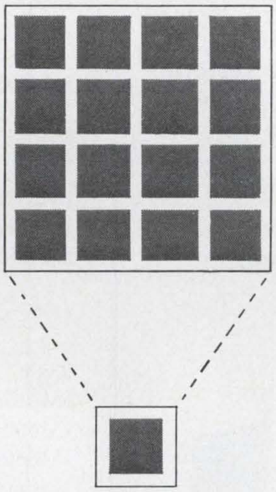

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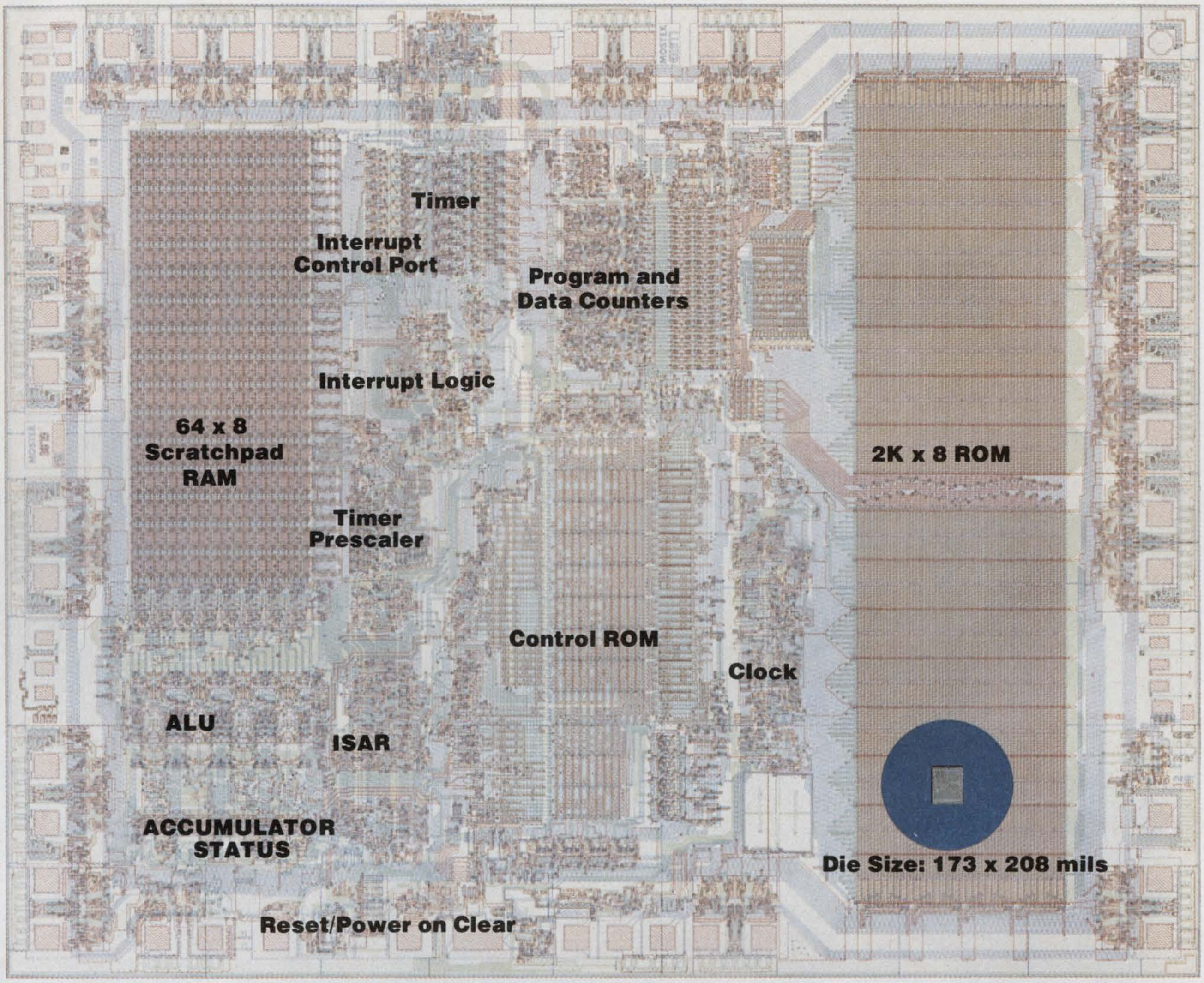


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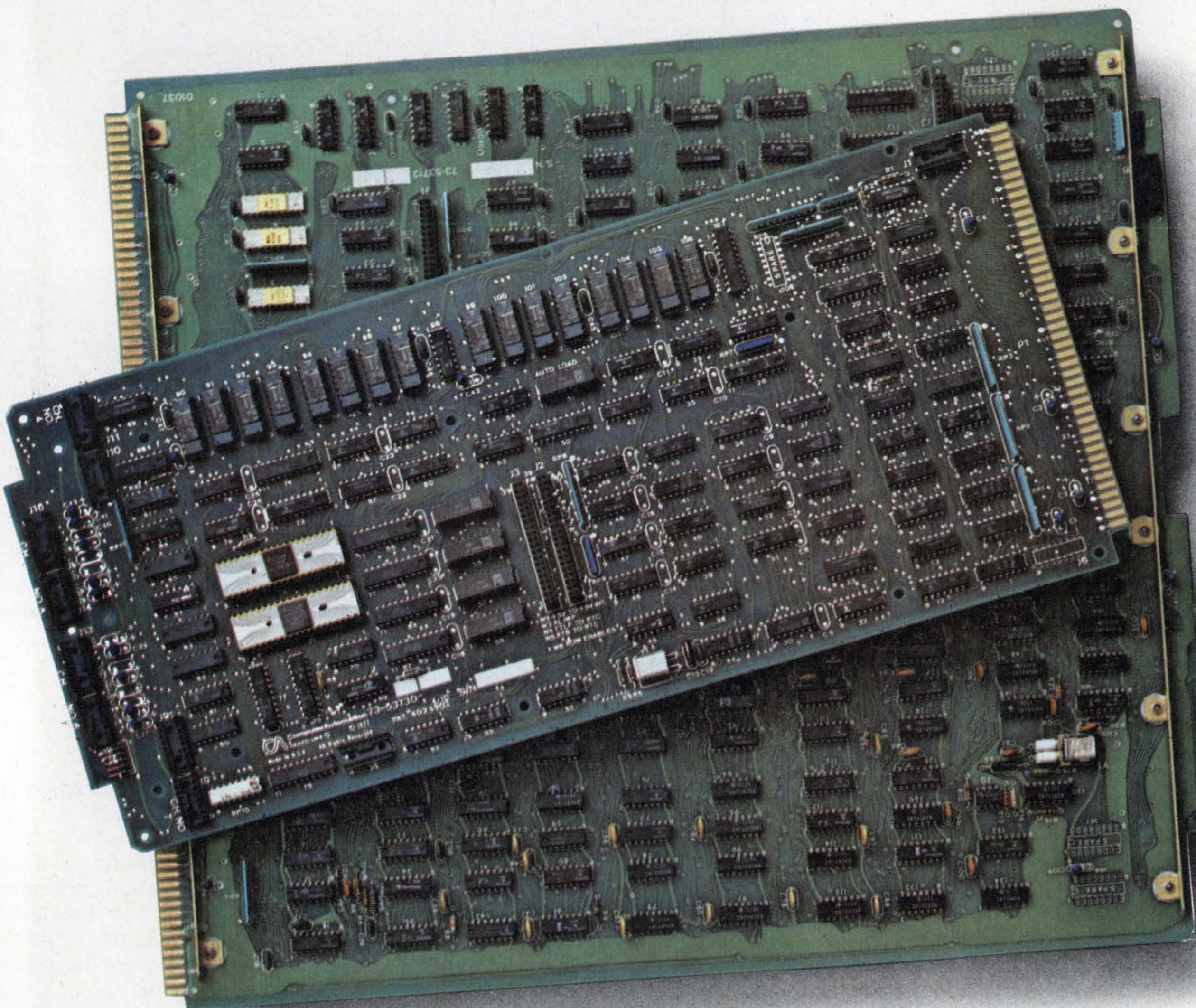

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# Learn microprocessor fundamentals.

## Even if you are familiar with $\mu$Ps, you may find this review of basic concepts useful and refreshing.

*As microprocessors ($\mu$Ps) become more and more acceptable as basic building blocks for all kinds of "intelligent" systems there is a tendency to assume that all engineers have a working knowledge of them. As a result, many $\mu$P articles that appear today—even many of the so-called "basics"—unexpectedly leave some readers in a dust cloud of vectored interrupts.*

*For those of you who missed the primer article about $\mu$P fundamentals that* ELECTRONIC DESIGN *ran back in 1975, the following article will introduce the basics. While no prior knowledge of $\mu$Ps is required, a little knowledge of computer programming and basic digital logic will help. A brief glossary of terms is included to summarize many of the buzz words.*

A microprocessor can be thought of as a box with three sets of signal lines coming out of it (Fig. 1):

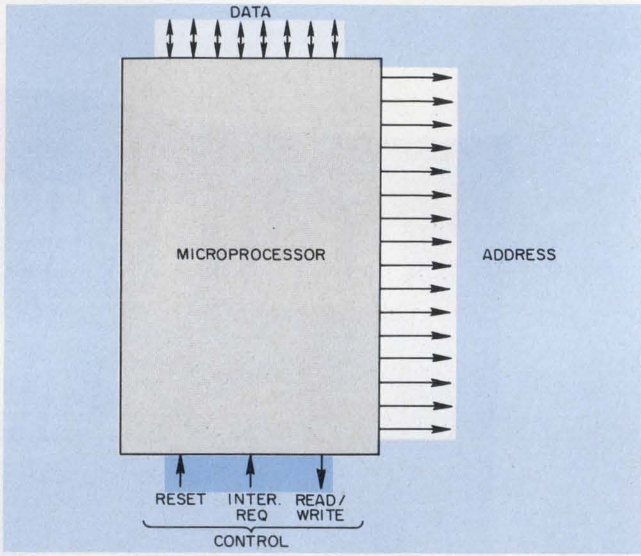
1. Address lines (often 16 of them), are all outputs and at any time may be at a logic 1 or 0, which indicates a binary number from 0 to 65,535 ("64 k").

2. "Data" lines (usually eight for an 8-bit $\mu$P) can act as inputs or outputs (bidirectional).

To find out what they are doing, look at

3. The control bus, whose most important segment is the read/write line. This output indicates whether the data lines are outputting (writing) or acting as inputs (reading).

At a given time, a $\mu$P will output an address between zero and 64 k, a read or write status, then will either output an 8-bit data word onto the data lines or accept data from the lines. The control bus also contains control lines for interrupts, resets, and other features, depending on the particular processor.




1. **A microprocessor, in its simplest form,** can be thought of as a black box with three sets of wires coming out of it.

### The memory is organized like this...

There are 64-k possible memory addresses, typically organized in groups of 8 bits (Fig. 2). A group of bits in parallel is called a "word," but the 8-bit word occurs so frequently that it has its own name—a byte.

Each byte of memory is accessed by the address lines. Until its individual address is called, it appears open-circuited. The byte being addressed is either pulled from the memory location onto the data lines or changed to match the byte of data on the data lines, depending on the status of the read/write line, shown in the block diagram of Fig. 3.

Rarely will all 64 kbytes of addressable memory be used. The capability is there, but only as much memory as is required by the application is ever used —sometimes less than 1024 bytes. Often in such systems, decoding is simplified by not using all 16 address bits.

To deal with large binary numbers, certain simplifications are extremely helpful. To this end, hexadecimal notation is often used (see box, p. 75).

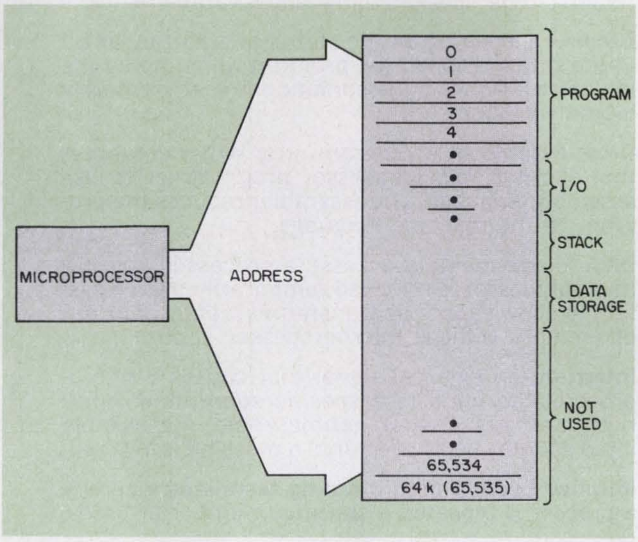
A microprocessor's memory is generally organized into blocks of addresses that serve specific areas:

1. Program.
2. Scratchpad and data storage.
3. The "stack."
4. Input/output (I/O) ports.

*The program* is a series of instructions to direct processing. Each instruction can contain one or more bytes. The first byte of a multibyte instruction provides the basic information, including the number of additional bytes in the instruction. Steps within an instruction proceed serially byte by byte. And unless otherwise indicated, a $\mu$P will "look" at the instructions sequentially, starting with a specific memory address and incrementing the address.

**Edward Gellender,** Consultant, 26 Middle Neck Rd., Roslyn, NY 11576.

In most cases, a μP reads only from the program section of memory since programs are often stored in read-only memories (ROMs). In developmental systems, however, more flexible program storage is usually required. To this end, read/write random-access memories (RAMs) should be used. However, this permits the original program to be stored on a magnetic cassette, so that it can be entered each time the power is turned on. This inconvenience is compensated by ability to change the program at will and rerecord it on the cassette. The corrected tape can be generated by one of several means—sometimes from a program already in the development systems, called a resident assembler, or from a "cross-assembler" program on a large computer. Or from a number of time-sharing services that have various cross-assemblers in their software arsenals. And simpler pad and pencil techniques can also be used quite successfully for short programs.




2. **Everything the microprocessor is hooked into** fits into the category of memory organized into specialized blocks.

An intermediate programming step is to use EPROMs (erasable programmable read-only memories), which can be erased with ultraviolet light. Once programmed, however, they can retain their information indefinitely. With μPs that serve to control routine operations, use of factory-programmed ROMs will minimize cost, but sacrifice flexibility.

### Examine a typical program sequence

Having come this far, consider a program sequence that illustrates a simple procedure. Suppose a byte of data were to be moved from one memory location to another. Assume that the address of the previous instruction is 0100 and that the contents of byte 24F1 are to be moved into 2407, neither address being in the program section of memory. Table 1 shows how it's done.

*Step 1.* The next consecutive address after 0100, 0101, is read. Its contents are 7A, which is interpreted as "Read data from the address given by the next two bytes."

*Step 2.* The least significant byte (F1) is read.

*Step 3.* The most significant byte (24) is read.

*Step 4.* The consecutive-address sequence on the

## Hex notation explained

Hexadecimal notation groups together four binary digits to form one digit representing a count from zero to 15. Obviously, some one-digit characters are needed to represent the decimal two-digit numbers from 10 to 15. The six letters, A through F, are used for this.

Hexadecimal notation is very convenient for microprocessors since it gives good counting densities and works very well with the multiples-of-four binary words usually encountered in a μP.

To understand the hexadecimal notation, take a number like 107. In binary notation, this becomes 1101011. Breaking this number into two groups of four digits, you get 0110 and 1011. The first of these is equal to 6, while the second one is 11. In hexadecimal notation, 107 becomes 6B.

Note that the highest memory address in a micro is hexadecimal FFFF.

To convert from decimal to hexadecimal, or vice versa, you must first convert the number into binary and then into hexadecimal as previously illustrated.

### Decimal conversion guide

| Decimal | Hex | Binary |
|---|---|---|
| 0 | 0 | 0000 |
| 1 | 1 | 0001 |
| 2 | 2 | 0010 |
| 3 | 3 | 0011 |
| 4 | 4 | 0100 |
| 5 | 5 | 0101 |
| 6 | 6 | 0110 |
| 7 | 7 | 0111 |
| 8 | 8 | 1000 |
| 9 | 9 | 1001 |
| 10 | A | 1010 |
| 11 | B | 1011 |
| 12 | C | 1100 |
| 13 | D | 1101 |
| 14 | E | 1110 |
| 15 | F | 1111 |

## Glossary of some microprocessor related terms

### Category I: Basics

**Bit:** a minimum logic element. A binary number of either 0 or 1.

**Word:** any group of bits indicating a single number or expression.

**Byte:** a word consisting of eight bits.

**Address:** a specific memory location that is called out by the program counter.

**Hex:** short for hexadecimal: numbers calculated to the base 16.

**Register:** a device that stores one word of data, and often consists of several flip-flops.

**RAM** (random-access memory): a data-storage device that can retain and produce on demand any data placed in it.

**ROM** (read-only memory): a device that has data permanently entered into it to be outputted on demand.

**PROM:** a programmable ROM in which a program is entered by the user before installation into equipment, as opposed to a factory-programmed ROM.

**EPROM:** A PROM that can be erased and reused indefinitely. Most EPROMs are erased under ultraviolet light and can be recognized by the clear cover over the silicon "chip."

**Decoder:** usually a device that detects a certain specific address on the address bus.

**Bus:** a group of wires that carry related binary signals, usually a word, as in a 16-wire address bus. A bus can be bidirectional, as in the case of a data bus.

### Category II: Parts of a microprocessor

**Accumulator:** a register in the microprocessor that operates on data. It is so-called because these registers were first used to accumulate totals.

**ALU** (arithmetic and logic unit): the circuitry that performs the manipulations on data held in the accumulator.

**I/O** (input/output): hardware that interfaces a microprocessor system with the outside world.

**Port:** a place through which inputs and outputs—either data or instructions—are channeled. A $\mu$P can have more than one port or can address many. Port size, though, is often specified in bits, ranging from 4 to 16 bits.

**Processor Status Word** (PSW): a word of readily available status information provided to indicate the result of specific operations.

**Program Counter:** two 8-bit registers used to generate the 16-bit address. The registers are called PCH and PCL and are used for the higher-order and lower-order bytes, respectively.

**R/W** (read/write): a control output of the microprocessor that indicates if data are being transferred from the microprocessor to memory, or vice versa.

**Scratchpad:** an area of the main memory set aside for short and often done calculations.

**Stack:** storage for data during subroutines or interrupts.

**Stack Pointer:** two 8-byte registers containing the address of the top (most recent end) of the stack.

### Category III: Programming

**Assembly Language:** a compromise between the user's thoughts and the numerical notation of the microprocessor. Assembly language is the closest technique to the actual numerical codes that still retains some speaking-language characteristics.

**Branch:** depending on the status of a particular bit in the status register, the program will jump by the indicated amount if the condition is met, or merely increment if not.

**Cross-Assembler:** a program on a larger computer that allows a microprocessor programmer to use assembly language. The assembler reduces the program to the machine language.

**DMA** (direct memory access): a process in which a microprocessor is removed temporarily from a system to allow data to be transferred rapidly in or out of memory without microprocessor control.

**Interrupt:** an external signal that causes a microprocessor to jump to a specific subroutine. Interrupts are maskable or nonmaskable. A maskable interrupt may be delayed until a mask bit is lowered.

**Iterative Loop:** a programming technique whereby a process is repeated a specified number of times.

**Jump:** a programming instruction that breaks the consecutive-instruction programming sequence and resumes elsewhere in the program.

**Machine Language:** Numerical coding, representing instructions, usually in the form of groups of bytes, used by the microprocessor.

**Peripheral:** a unit operated with a microprocessor system such as a keyboard or a printer.

**Program:** a set of sequential instructions that a computer follows.

**Subroutine:** a program within a program that performs a specific, often-used function.

**Vector:** a specific address loaded into a microprocessor's program counter to force the $\mu$P to start processing at a specific address.

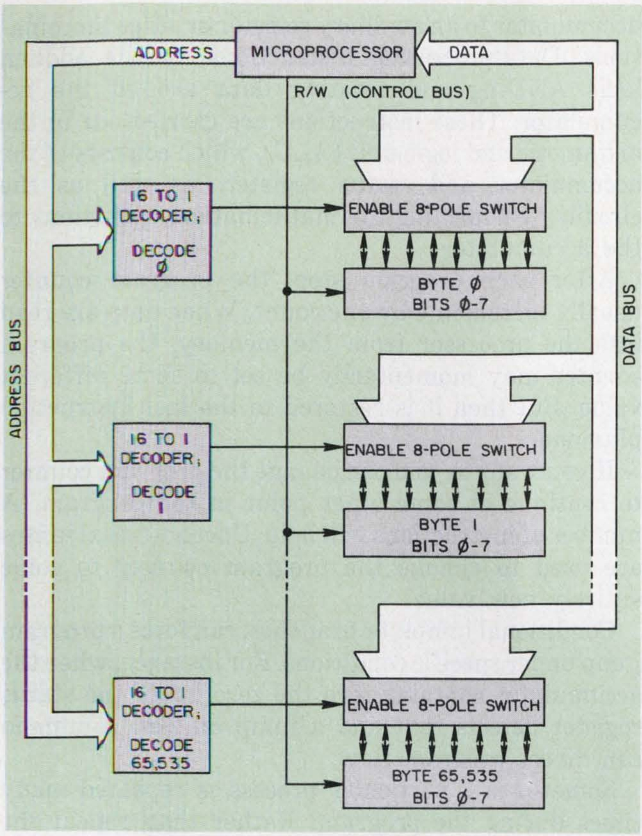
address bus is momentarily interrupted, and the contents of byte 24F1 are read. The contents are 7A — but now the 7A represents data, not an instruction as in Step 1.

*Step 5.* The consecutive-address count resumes at 0104. The next instruction, 4A, is interpreted as "Write the data stored in the processor into the address given by the next two bytes."

*Step 6.* The least significant byte (07) is read.

*Step 7.* The most significant byte (24) is read.

*Step 8.* The consecutive addresses are interrupted again, while 7A is placed into address 2407.




3. **Microprocessor-to-memory connection** via the buses can be thought of as shown above. Note that each 8-pole switch can be closed one pole at a time.

## A simple machine program

| Step no. | Address bus | Data lines | R/W |
|---|---|---|---|
| 1 | 0101 | 7A | R |
| 2 | 0102 | F1 | R |
| 3 | 0103 | 24 | R |
| 4 | 24F1 | 7A | R |
| 5 | 0104 | 4A | R |
| 6 | 0105 | 07 | R |
| 7 | 0106 | 24 | R |
| 8 | 2407 | 7A | W |
| 9 | 0107 | ... | |

*Step 9.* The consecutive addresses resume.

Note that the μP follows a rigid sequence to keep track of which bytes are instructions, which are data, which are addresses, and so on. Thus, the same byte (7A in the example) can be placed on the data lines at two different times and have two separate meanings.

Note also, that the least significant byte of an address is handled first, although it isn't crucial. Some processors do it this way while other processors do it the reverse. Just make sure to check which way it should be done when you start to program.

The *scratchpad and data storage* serve to store data temporarily. "Scratchpad memory" usually designates an area of memory used for many quick data transfers. It is the most frequently used memory segment. Some microprocessors have simplified instructions that can only be used in a certain small part of the memory (say, the first 256 bytes), where the most significant byte of the addresses is zero. The scratchpad is usually placed in such a location.

The data-storage area is similar to the scratchpad, except that just the usual processor instructions can be used. Thus data may be addressed slower than in the scratchpad area. Data storage is used for the bulk of the memory, and RAM is most often used for data storage.

The *stack* is a read/write block of memory used to "remember" the next consecutive address and associated data when the address lines are taken over by a sequence of nonconsecutive addresses, as in a subroutine. More will be said about the stack when subroutines are discussed.

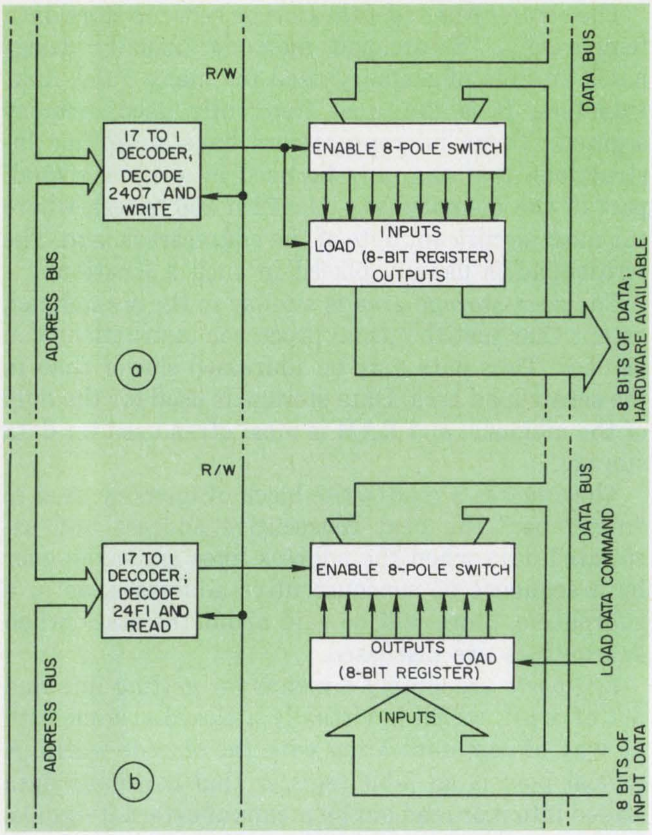
*I/O ports* are simply a means for getting into and out of a μP, which is virtually a closed system with no way of communicating with the outside world. A typical port is an 8-bit register that can have data loaded into it or read out by means of external signals. It also has an address decoder to detect when the μP is addressing it. At such a time, either the contents of the data bus are put into the register (output port) or the contents of the register are placed on the data bus (input port).

If, for the program sequence of Table 1, address 2407 does not go to a RAM but is decoded and used to load the contents of the data lines (7A) into a register, the data are accessible at the outputs of the register (an output port) until the register is supplied with new data. Thus the data stored in memory at address 24F1 and accessible only by programming are now available to the outside world via an output port (Fig. 4a). If such a register's address is called with the outputs connected to the data lines, the register would be an input port (Fig. 4b).

### What goes on inside?

So far the microprocessor has been treated as a "black box" that always knows which words to place on the address and data lines. Look inside to see how the μP figures out what to to.

The simplest μP consists of a program counter, a controller and an accumulator (Fig. 5a). The program counter often consists of two cascaded 8-bit counters —the low and high-byte registers (or the least and most significant bytes). When power is applied, the program counter is forced to a particular starting address that holds the first line of the program. The first line is then read into and interpreted by the controller. The program counter is then increased by one count unless that line has information that drastically modifies the counter.




4. **Output (a) and input (b) ports** provide the means for communicating with the outside world. In "a," address 2407 and a WRITE command load the data bus into a register. In "b," data are loaded into the register. Address 24F1 places them onto the data bus.

Any data read in or out via data lines are read to or from the accumulator, which is also an 8-bit register. All logic and math manipulations occur in the accumulator. For example, a word can be read from memory and added to one already in the accumulator. The result is stored in the place of data used to generate it.

Fig. 5b depicts a more complex microprocessor. Certain tests on the accumulator such as checking for zero, a positive result, a negative result, or something else, are often needed, and indicators are provided by bits in the status register. A carry bit for additions indicates sums in excess of the accumulator capacity. Another bit indicates when the accumulator holds all zeros. Certain program instructions require the instruction decoder to monitor those status bits and a few others.

A number of auxiliary registers can be provided for modifying the program counter, additional accumulators, or readily available scratchpad memories.

## Control the μP with a program

Having covered the basics, you are ready to learn about basic programming instructions to move and process data, and modify a program.

Data-move instructions transfer data from memory into the accumulator and vice versa, or from the accumulator to an auxiliary register or other combinations. Data-processing instructions include adding, logic ANDing and rotating data around the accumulator. Those instructions are carried out in the arithmetic and logic unit (ALU), which consists of the accumulator and status register, as well as the circuitry performing the mathematical operations to the accumulator.

After each program step, the program counter usually increments by one count. When data are read into the processor from the memory, the program counter may momentarily be set to some different value. But then it is restored to the last instruction plus one.

If you want to, you can change the program counter to continue at some other point in the program. A number of instructions will help. Unconditional jumps are used to change the program counter to some entirely new value.

Conditional jumps, or branches, can force a program jump under specific conditions. For instance, when the accumulator contains zero the zero bit of the status register detects that and a jump on zero command can divert program flow.

Sometimes a particular process is repeated many times during the program. Rather than repeat the program section each time, the program can call a subroutine (a subservient program) whenever it is needed. This particular process is written in a separate part of program memory, usually after the main program. Getting to the subroutine is similar to the unconditional jump. Bear in mind, however, that the present location of the program sequence must be memorized for the program to return to where it left off after completing the subroutine.

The stack is used for this purpose. It is an area of memory reserved primarily, but not exclusively, for program addresses. A stack pointer, which refers to addresses placed in the stack, is initialized to a desired value at the beginning of the program to the starting point of the block of memory locations reserved for the stack. When a subroutine is called, the contents of the program counter are incremented and placed in two bytes of the stack memory (16 address bits in two bytes). The stack pointer is lowered by two counts. At the end of the subroutine, the two bytes are read from the stack into the program counter to call the next consecutive instruction as if no change had taken place. Of course, the stack pointer is brought back up to keep the bookkeeping up-to-date.

But suppose the contents of the accumulator, status register or other registers are needed later and cannot be kept in their present locations while the subroutine is being executed. The first instructions in the subroutine may also load these contents onto the stack. The last instruction in the subroutine will have to restore these registers to their original status. The stack pointer, of course, will be changed accordingly.

Another alternative is for subroutines to call other subroutines to be performed, then return first to the original, or main subroutine, and finally to the main program. Calling subroutines within subroutines, or nesting, can continue indefinitely, as long as there is enough room in the stack. Each time an address is loaded onto the stack, the stack pointer is decremented by two bytes. The next address is then placed in the next two bytes, and the stack pointer is decremented again. Each time a return from subroutine is executed, the top address is taken from the stack and the stack pointer is incremented twice. When the main program is running again, the stack pointer will return to its initial value.

Sometimes, the program can be modified by data stored in a particular memory location. For instance, data stored in one place can indicate the address where some other data are to be sent. The programming steps described so far do not allow for this.

### Indirect addressing helps

Some sort of indirect addressing is included in a $\mu$P, to allow the data to provide some form of steering to the program. One technique is to place a byte of data into one byte of the program counter, and then have the $\mu$P read or write data between that composite address and the accumulator. At the end of that step, the old program counter contents (plus one) are reintroduced.

I/O ports are often used for data transfer into and out of the system. However, the $\mu$P must determine whether or not an input has occurred and data have been loaded into an input port.

One way to determine if data are present is to allow the processor program to test one bit of an input port periodically. If data are brought in, that bit can be set to 1 by external circuitry and reset to 0 via an output port after the data are entered. This approach is very slow, however, so a faster method is generally used.

The essence of the faster method is to provide a special input to a $\mu$P. It is called an interrupt input. During normal operation, the processor ignores all input ports. Should data be entered, an external signal is brought to the interrupt input, without going through the program.

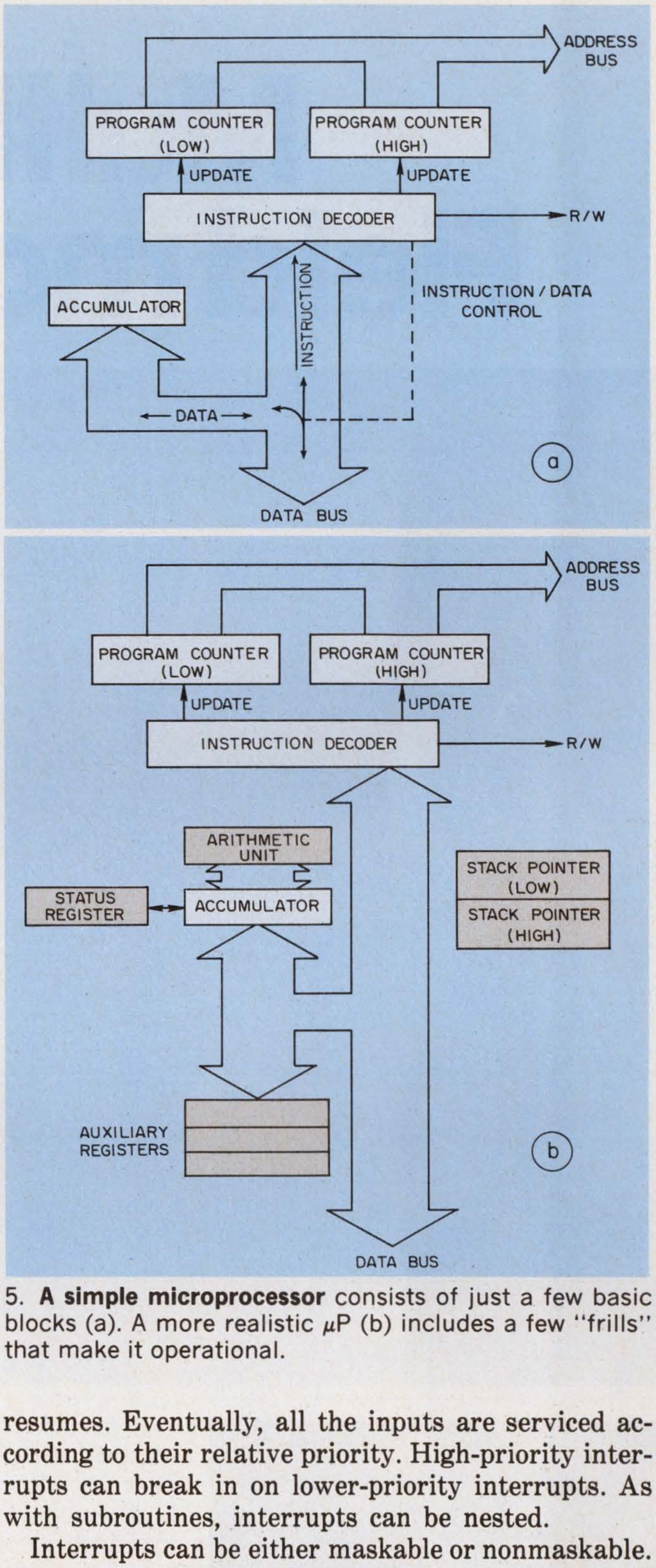
Once the instruction in progress is completed, the processor acts as if a "call subroutine" is being read. The program counter and status-register contents are placed on the stack and the program counter is forced (or vectored) to the address where a program servicing the interrupt begins. The interrupt is serviced and a return from interrupt, similar to a return from subroutine, restores the program counter and status registers to the initial values.

In general, when one of several inputs causes an interrupt, the interrupt program scans the inputs to determine which one has new information. The most time-critical input is scanned first, then successively less critical inputs.

When a high-priority input is completed, scanning resumes. Eventually, all the inputs are serviced according to their relative priority. High-priority interrupts can break in on lower-priority interrupts. As with subroutines, interrupts can be nested.

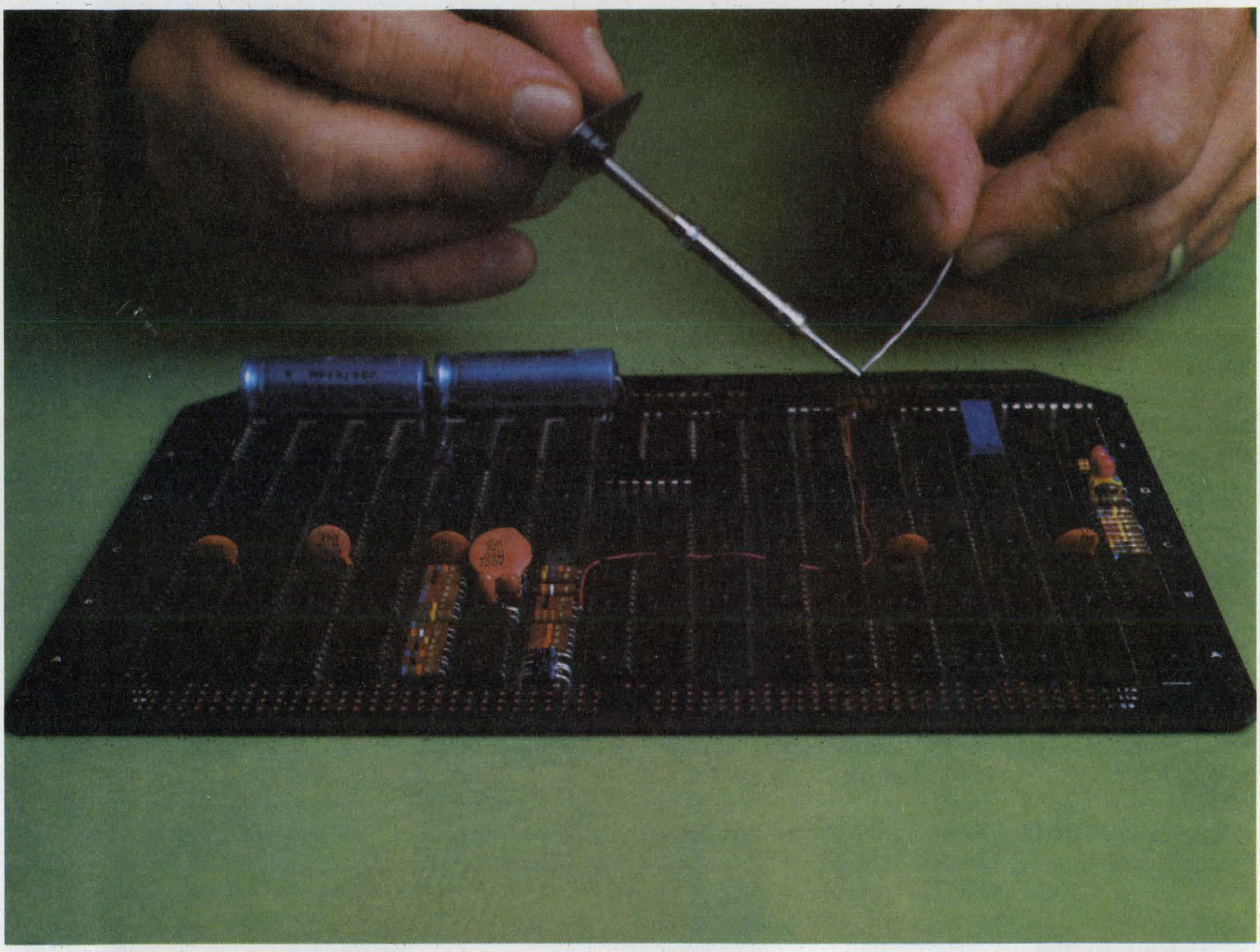
Interrupts can be either maskable or nonmaskable. A mask bit can delay servicing of an interrupt until the bit is lowered. Nonmaskable interrupts do not respond to a mask bit and are serviced immediately.

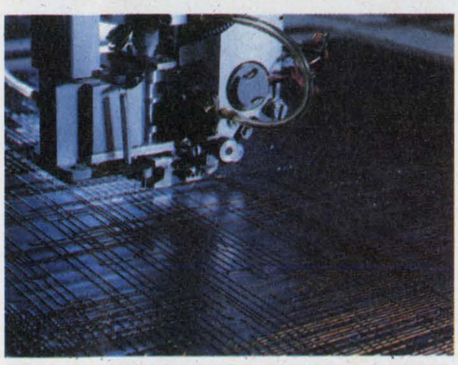
Sometimes, data or programs must be quickly loaded from memory into an external unit, or vice versa. These are jobs for direct memory access (DMA). DMA capability means that a $\mu$P can be effectively decoupled from the address, data, and read/write buses. An external device will control those lines to rapidly transfer blocks of data directly into memory, and bypass the $\mu$P.■■




5. **A simple microprocessor** consists of just a few basic blocks (a). A more realistic $\mu$P (b) includes a few "frills" that make it operational.

# Multiwire®: Field modifiable.





Of the many benefits offered by Multiwire, one of the most important is its simplicity of change and repair. Multiwire boards are normally easier to change after assembly or in the field than multilayer.

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Multilayer changes, of course, are an entirely different story. Corrections are difficult at best and frequently impossible. As one engineer familiar with multilayer puts it: "Corrections... are something of a disaster."

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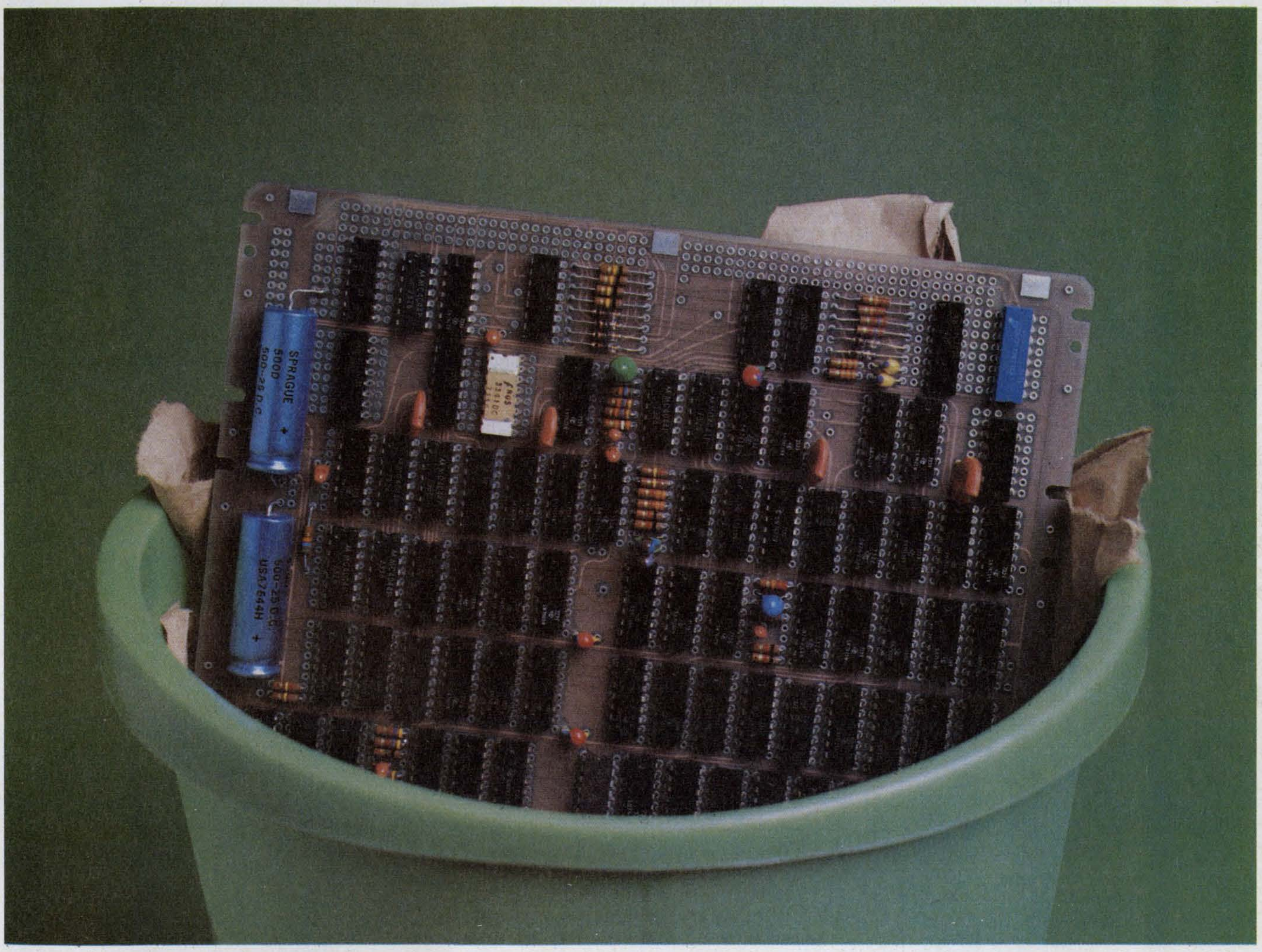

is simply unsoldered; the plated-through holes stand up just as well if not better than regular PC board holes. With multilayer, however, a soldering iron often lifts the land off the board, with many ensuing problems.

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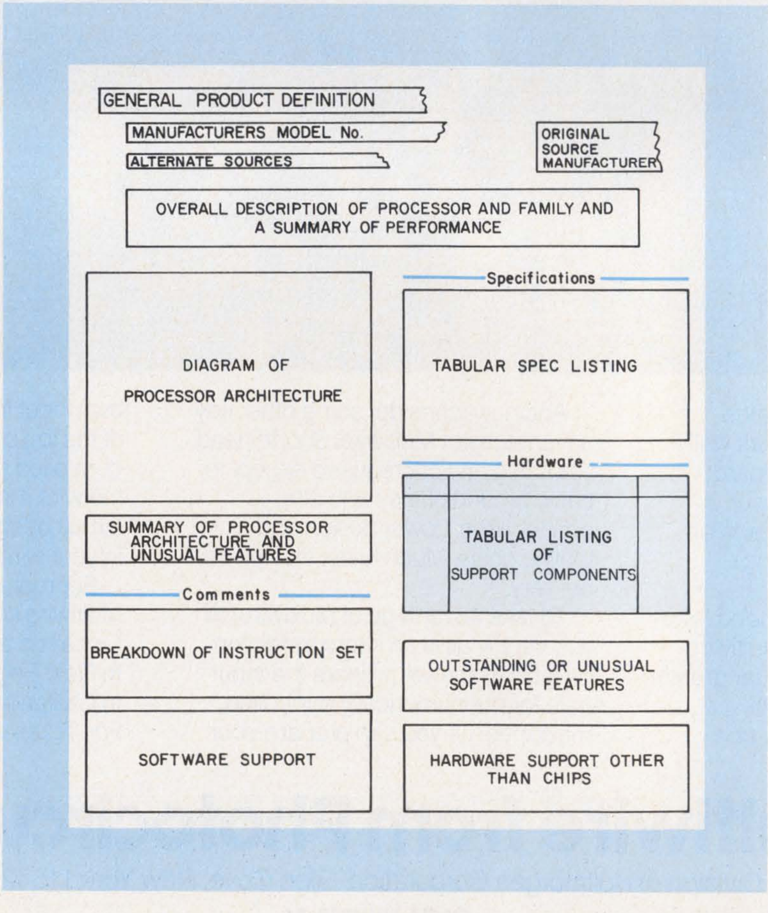
**CIRCLE NUMBER 36**

# Using the Microprocessor Data Manual

The Data Manual microprocessor data pages are organized first by processor data-word size, then by generic family, by technology and finally by original source manufacturer (within each generic family processors are listed alphabetically by original manufacturer). Generic families included in the manual are:



# Here's what's on a manual page



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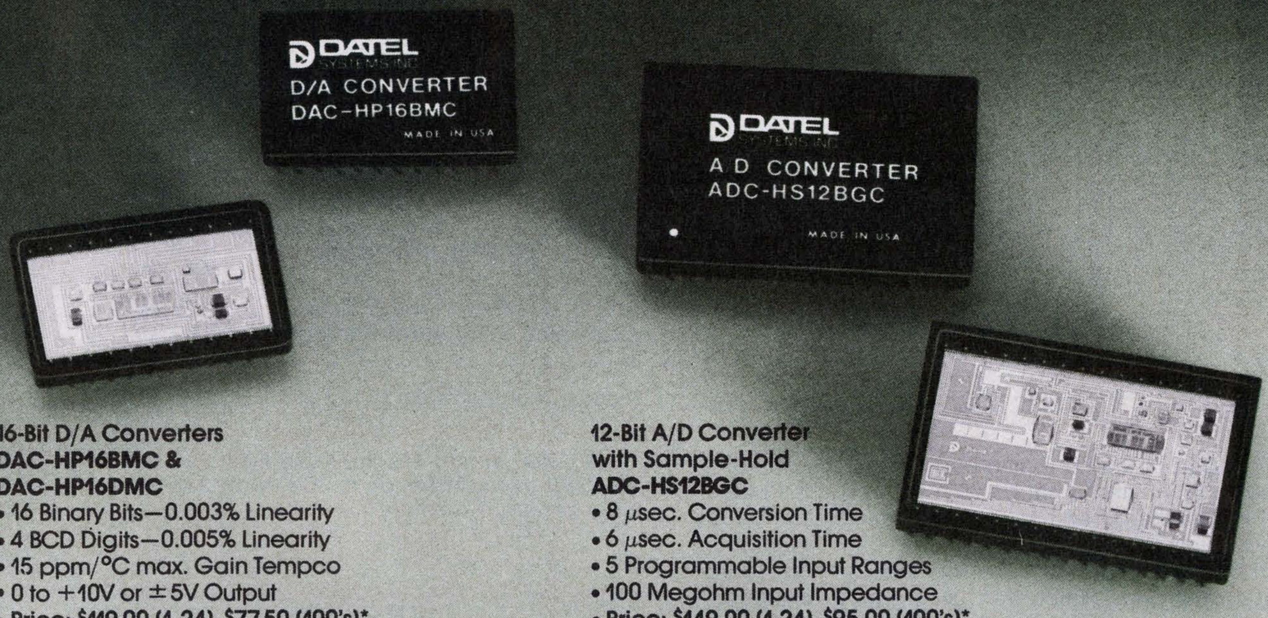


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CIRCLE NUMBER 37

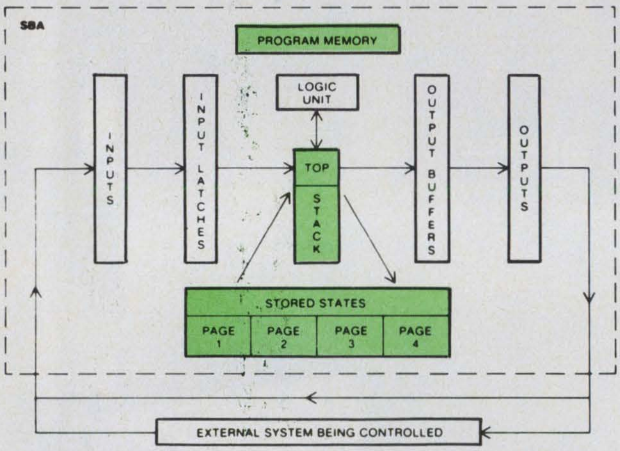
# 1-bit microcomputer, NMOS

## SBA (Sequential Boolean Analyzer)

**General Instrument Corp.**
**600 West John St.**
**Hicksville, NY 11802**
**(516) 733-3107**

Alternate sources: None.

A simple, low-cost single-bit processor, the SBA can directly evaluate a set of Boolean equations. Thirty programmable inputs and outputs as well as memory make the SBA a true 1-bit microcomputer. An n-channel, ion-implanted device, the SBA is designed for ease of use, in simple control applications.




The Sequential Boolean Analyzer consists of a program memory that holds a set of Boolean functions that define system operation as well as 30 input buffers that are latched at the start of the evaluation of Boolean equations, and four pages of 30 stored-state flip-flops which can be grouped to emulate counters and shift registers. Also included are a logic unit that can perform the logic functions and a stack that holds a set of Boolean values used to evaluate the input equation.

### Specifications

| | |
|---|---|
| Data word size: | 1 bit |
| Address bus size: | None* |
| Direct addressing range: | None* |
| Instruction word size: | 8 bits* |
| Number of basic instructions: | 24 |
| Shortest instruction/time (All): | 1.25 μs |
| Clock frequency (min/max): | 10 kHz/ 800 kHz |
| Clock phases/voltage swing: | Internal |
| Dedicated I/O control lines: | 30 |
| Package: | 40-pin DIP |
| Power requirements: | 12 V/? mA |
| | 5 V/? mA |

* No external address lines are available but the SBA can address up to 1023 words of on-chip program memory.

### Hardware

| Model | Description | Price |
|---|---|---|
| SBA | CPU | $4 (2500 qty) |
| SBA-1 | Same as SBA but uses external PROM/RAM | N/A |

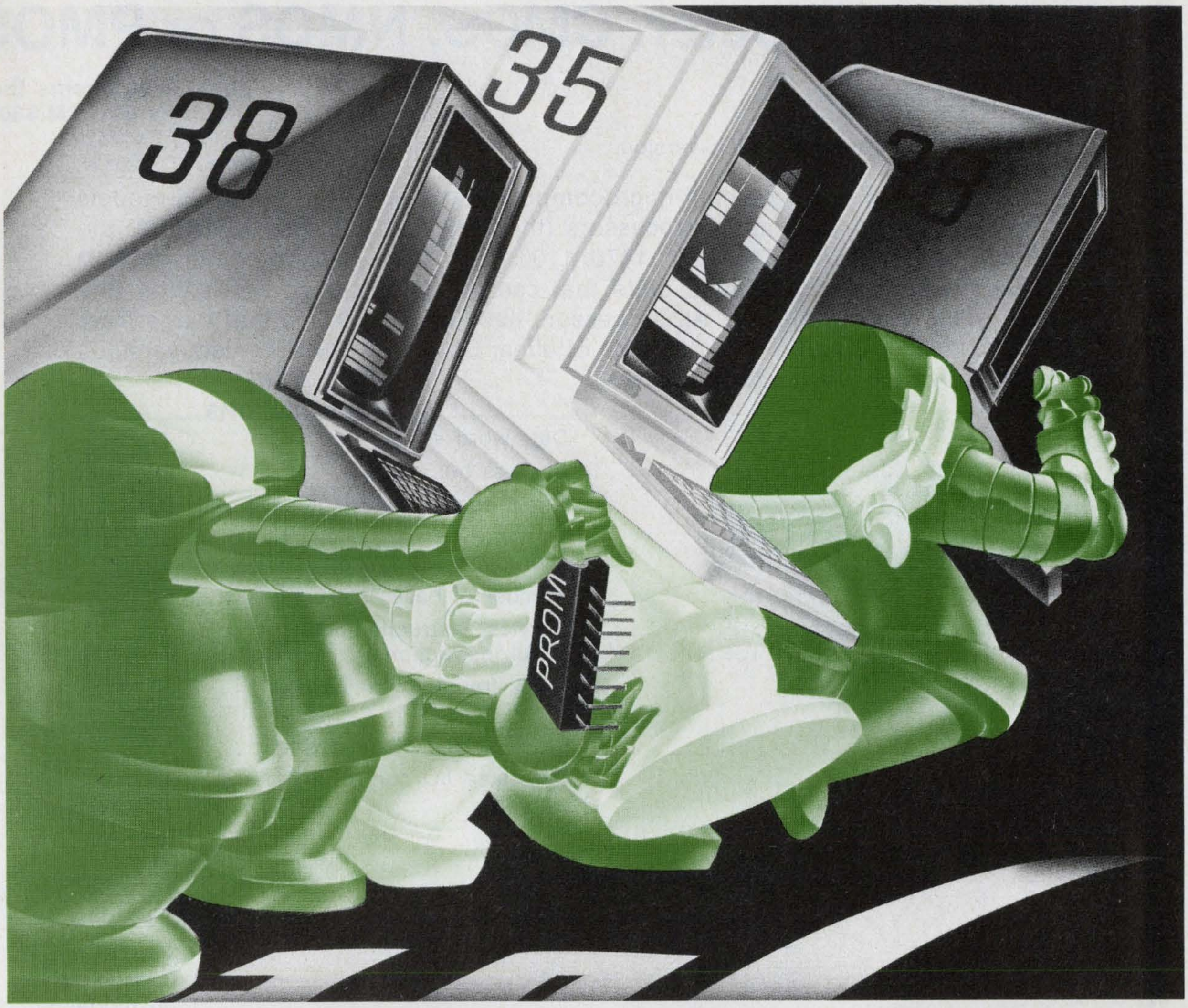
### Comments

**The results of Compare and Invert** instructions are stored in either the stack, memory or output. Inputs for logic operations are from the stack or memory, or from inputs. The stack is 16 x 1 bit and the state store is 120 x 1 bit. There are 24 basic instructions, all of which execute in the same amount of time. The processor is designed to process Boolean equations based on the status of the 30 I/O lines.

**An SBA Compiler** produces optimized codes from Boolean equation inputs, and an SBA simulator provides software simulation of the SBA.

**The programming for the SBA** is via Boolean expressions. An 8-bit word provides the instruction code, five bits of the code provide an address for the inputs, outputs or stored states and, if two of the 32 available addresses are reserved for addressless instructions, the remaining three bits of the code enable a total of 24 instructions to be made available. Most of the instructions are AND, NAND, OR, Ex-OR, and stack or I/O operations.

**Hardware support will be** the SBA-1, a version with external RAM or PROM for prototyping, otherwise there are no prototyping systems available.

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In addition to all the basic plays to control routine disc operations, the software system provides a resident monitor, a symbolic assembler, editor, debugger and utilities for systems generation, communications and copy operations. Device drivers are also provided for interfacing with CRT, communications adaptors and external peripherals. Discs provide memory storage and can be used in creating PROMs reflecting a user program. Final score: it's a winner!

Write or call Michael L. Squires for details and specifications, Information Products Division, Omron Electronics, Inc., 432 Toyama Drive, Sunnyvale, CA. 94086. (408) 734-8400.

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CIRCLE NUMBER 38

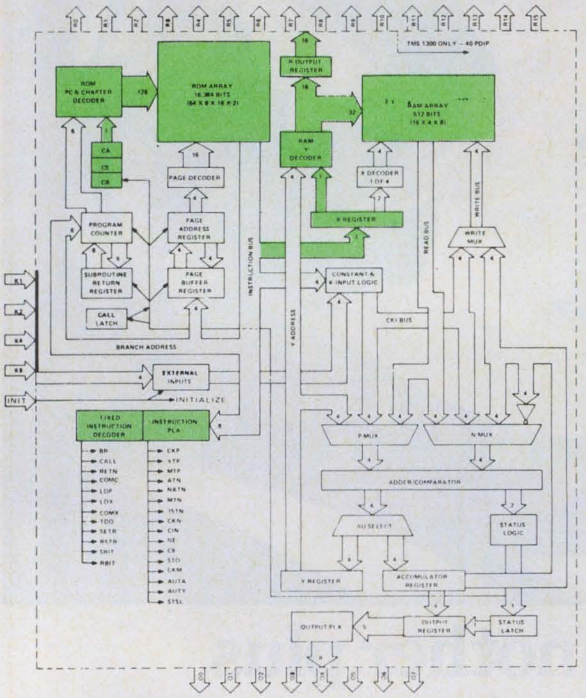
# 4-bit microcomputer, CMOS, NMOS or PMOS

## TMS1000 family

Alternate sources: Motorola for CMOS version.

**Texas Instruments Inc.**
**P.O. Box 5012, M/S308**
**Dallas, TX 75222**
**(214) 238-2011**

The TMS1000 family of single chip microcomputers is available in about 35 models —the unprogrammed evaluation processors (the TMS1099/SE1 and 1098/SE2), the general purpose family (the TMS1000, 1070, 1100, 1200, 1270, 1300 and other models) and some already preprogrammed units that can go right into an application (the TMS1018, 1022, 1117 and 1121). All processors have on-chip ROMs that range from 1024 × 8 to 2048 × 8 and on-board RAMs of either 64 × 4 or 128 × 4. Also, versions with up to 16 output lines can be had.



The architecture of all the TMS1000 products is very similar, with the main differences appearing in the size of the RAM and ROM and the number of I/O lines. All processors have an internal clock generator, but can accept a single-phase clock signal if timing must be generated externally. Just the single chip is needed to form a minimal working system.

### Comments

**The instruction set** contains a total of 54 commands that are divided into five basic groups: 12 register reference instructions, 27 arithmetic and logic operations, three bit-manipulation commands, five I/O instructions and seven memory addressing.

**Software support** for the TMS1000 family consists of an assembler, simulator, a high-level language compiler (TIML) and a variety of utility programs. There is no program library available.

**Special features of the software** include the wide variety of register and accumulator operations possible as well as the individual bit set, reset and test operations on the contents of a memory location.

**Hardware support** for the TMS1000 family starts with the 64-pin system evaluator chips that permit external RAM and ROM interfaces and prototype boards for the evaluation chips. Also available is the AMPL development system which permits assembly and simulation and will soon permit in-circuit emulation.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | Internal |
| Direct addressing range: | 2048 words, max |
| Instruction word size: | 8 bits |
| Number of basic instructions: | 54 |
| Shortest instruction/time (All instructions): | 6 μs min. |
| Clock frequency (min/max): | 50 kHz/1 MHz |
| Clock phase/voltage swing: | $1/V_{supply}$ |
| Dedicated I/O control lines: | 16 max. |
| Package: | 28 or 40-pin DIPS or 64-pin evaluator |
| Power requirements: | 3 to 35 V at 1 to 10 mA, depending on model |

### Hardware

| Model | Description | Price (5000 qty) |
|---|---|---|
| TMS1000 | 28-pin microcomputer | Under $4. |
| TMS1070 | 28-pin microcomputer | Under $4. |
| TMS1100 | 28-pin microcomputer | Under $4. |
| TMS1200 | 40-pin microcomputer | Under $4. |
| TMS1270 | 40-pin microcomputer | Under $4. |
| TMS1300 | 40-pin microcomputer | Under $4. |
| TMS1098/SE1 | 64-pin evaluator | N/A |
| TMS1099/SE2 | 64-pin evaluator | N/A |
| TMS1330 | Combo CPU, a/d converter and keyboard controller | $7. |
| TMS1024 | 4 x 4 I/O expander | Under $3. |
| TMS1025 | 4 x 7 I/O expander | Under $3. |
| TMS1976 | CPU to capacitive keyboard interface | Under $3. |

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H-2-6

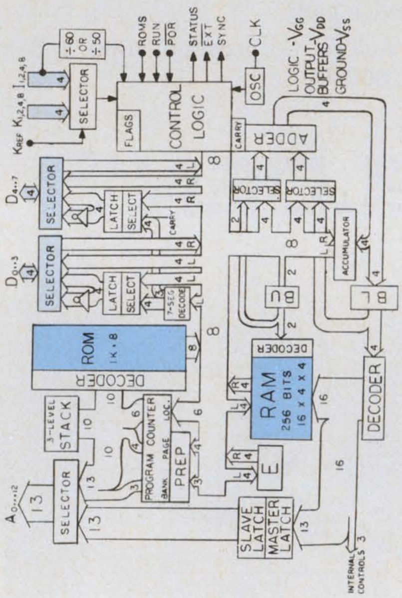
# 4-bit microcomputer, NMOS

## S2000

American Microsystems Inc.
3800 Homestead Rd.
Santa Clara, CA 95051
(408) 246-0330

Alternate sources: None.

A single-chip, 4-bit microcomputer built with silicon-gate, depletion-load NMOS technology, the S2000 includes, on-chip, a 1 k x 8-bit ROM, 64 x 4-bit RAM, 50/60-Hz timer and clock oscillator. Most of its 61 instructions are executed in 4 $\mu$s. Among 29 I/O lines are LED drivers (and a 7-segment display decoder), as well as a touch-control interface. The device operates from a 9-V supply and has power-on reset circuitry.




The architecture of the S2000 microcomputer includes I/O ports for almost every application—there are seven-segment display outputs, touch-control inputs, LED or vacuum-flourescent drivers (S2000A), a voltage comparator, a 64 × 4 RAM, a three-level stack and an on-chip clock oscillator. All lines are TTL compatible and the eight D lines also have three-state capability.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | 13 bits |
| Direct addressing range: | 8192 words |
| Instruction word size: | 8 bits |
| Number of basic instructions: | 61 |
| Shortest instruction/time (Most): | 4 $\mu$s |
| Longest instruction/time (Jump to subroutine): | 8 $\mu$s |
| Clock frequency (min/max): | Dc/1 MHz |
| Clock phases/voltage swing: | 1/internal |
| Dedicated I/O control lines: | 29 |
| Package: | 40-pin DIP |
| Power requirements: | 9 V/26 mA |

### Hardware

| Model | Description | Price |
|---|---|---|
| S2000 | 4-bit microcomputer | $3.50 (100-k qty) |
| | No special interface circuits are needed. | |

### Comments

**The instruction set** for the S2000 processor consists of 61 commands that are divided into the following groups: 14 ROM and RAM instructions, 13 conditional skip commands, 12 arithmetic and logic operations, 11 I/O directives and 11 register instructions.

**Software support** includes a text editor, assembler, real-time debugger, floppy-disc operating system, software simulator, macroprogram library, self-diagnostic programs and many applications oriented programs. All these programs are designed to run on the MDC, a microcomputer development center.

**Special features of the software** include the fact that all but two instructions execute in one machine cycle and that some instructions can do several jobs simultaneously. For instance, the XCD command exchanges the accumulator contents with a RAM location, decrements register BL, modifies register BU and does a conditional jump.

**Hardware support** consists of the MDC microcomputer development center, which includes a CRT terminal, a dual-floppy-disc system, the DEV-2000 real-time debug breadboard, printer and logic analyzer (40 channels × 1024 events). There is also a single-board S2000 evaluator that uses a UV EPROM memory to permit program testing.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Our new $\mu$p-based interface couplers will link virtually any programmable instrument to the IEEE 488 bus even though their input and output is not bus compatible.

**RS-232 TO BUS** Here's a new, inexpensive way to convert your teletype to a 488 bus printer. For about $900, the Model 4884 will provide a bi-directional data link between the parallel IEEE 488 bus and the RS-232 serial data path. And it's not limited to teletype. The 4884 will make any 20mA device such as printers and recorders bus-compatible.

**DVMs AND COUNTERS TO BUS** Building an ATE system? You may have a pool of older instruments, But the DVMs and counters aren't 488 compatible. For about $800 you can buy a Model 4881 that will take data from any DVM, counter, or other instrument and put it on the bus.

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**HOW ABOUT A BI-DIRECTIONAL COUPLER** For about $900, the 4884 combines capability and operational features of the 4881 and 4882 in one unit. It can be used to control or take data from a measuring device, accept program commands from the bus, pass the commands on to a DVM's control inputs, initiate readings and output data when addressed. You can even reduce it to "talk-only" or "listen-only" by setting the mode switches.

**AND THERE'S MORE TO THE FAIRCHILD LINE** Fairchild also offers other instruments. The 6600 takes paper tape input and interfaces to CRTs, modems or remote CPUs. The 1700 takes BCD output and interfaces with TTYs, CPUs modems and paper tape punches. Write: Fairchild Instrumentation, a unit of Fairchild Camera and Instrument Corp., 1725 Technology Drive, San Jose, CA 95110 Phone (408) 275-6600 or (408) 998-0123.

**FAIRCHILD**

**CIRCLE NUMBER 40**

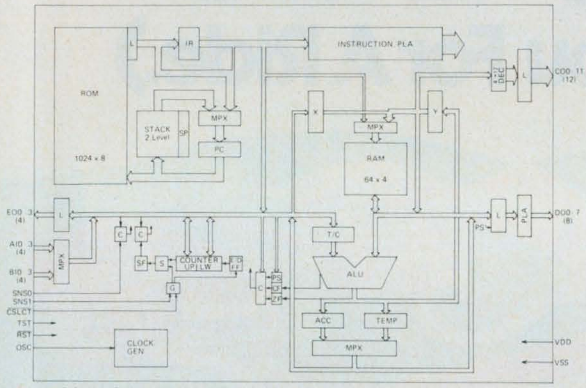
# 4-bit microcomputers, NMOS

## MN1400 series

**Panasonic Co.**
**50 Meadowland Parkway**
**Secaucus, NJ 07094**
**(201) 348-7276**

Alternate sources: None.

The MN1400 series of microcomputers consists of four models, each with different amounts of on-chip program memory. The "standard" model is the MN1400, with a 1k x 8 on-chip mask-programmed ROM and 75 instructions. A "shrink" version of the unit, dubbed the MN1402 offers 57 instructions and only a 768 x 8 program memory. Also available are two versions that have no on-chip memory. The MN1498 can address 1 k x 8 of external memory and offers 68 instructions. The largest processor is the MN1499, with an addressing capability of 2 k x 8 and 75 instructions. All processors have a two-level subroutine stack and on-board RAMs of 64 x 4 bits, except for the 1402, which has a 32 x 4 bit RAM.




C: Comparing Circuit L: Latches S: Synchronizing Circuit

Complete all-in-one microcomputers on a chip, all parts in the MN1400 family have on-board clock generators, and up to 64 x 4 bits of RAM. All units have a two-level subroutine stack and different amounts of I/O capability. The MN1400 provides 12 individually settable latched output lines on one of its ports, eight simultaneously settable lines on another output port, four more lines on another output port and two sets of four lines each on two input ports. The 1402 has two 4-bit input ports, two 4-bit output ports and one 5-bit output port. The 1498 has fewer ports since the program memory must be externally addressed—it has one 4-bit input port, one 4-bit output port and one 9-bit output port. Lastly, the 1499 has all the ports of the 1400 and in addition has the interface necessary to handle external memory.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | 11 bits (max) |
| Direct addressing range: | 2 k (max) |
| Instruction word size: | 8 bits |
| Number of basic instructions: | 57 to 75 |
| Shortest instruction/time (several commands): | 10 μs |
| Longest instruction/time (Branch/Jump): | 20 μs |
| Clock frequency (min/max): | dc/300 kHz |
| Clock phases/voltage swing: | 1/5 V |
| Dedicated I/O control lines: | 20 |
| Package: | 28, 40 or 64-pin DIP |
| Power requirements: | 5 V/100 mA |

### Hardware

| Model | Description | Price |
|---|---|---|
| MN1400 | CPU, 40-pin, 75 instructions | approx. $8 (1000 qty) |
| MN1402 | CPU, 28-pin, 57 instructions | same. |
| MN1498 | CPU, 40-pin, 68 instructions | consult factory |
| MN1499 | CPU, 64-pin, 75 instructions | $75. unit qty |

### Comments

**Both the MN1400 and 1499 have a set of 75 instructions** that are divided into four basic groups: 18 data transfer commands, 18 arithmetic and logic directions, nine I/O instructions, and 30 control commands. Both the 1402 and 1498 instruction sets are subsets of the 75 commands of the 1400.

**Support software** for the MN1400 family consists of a cross-assembler program for use on large computer systems. The cross-assembler contains error diagnostic and macro instructions, and is written in Fortran. Additional support is also available on minicomputers such as the PFL-16A made by Panafacom Ltd. Hardware simulation as well as editing and debug routines are available. There is no formal program library, but various application programs are available on request.

**Special instructions** in the MN1400 family include bit reset and bit set commands for data stored in memory as well as a wide choice of I/O commands. The built-in counter/timer is totally software controller—special instructions are used to preset the circuit or to enable or disable the counter.

**Hardware support** is performed by the MN1499, a system evaluator circuit. The 1499 requires external memory but to help debug programs it has a single-step control line that can be used to go through programs one line at a time.

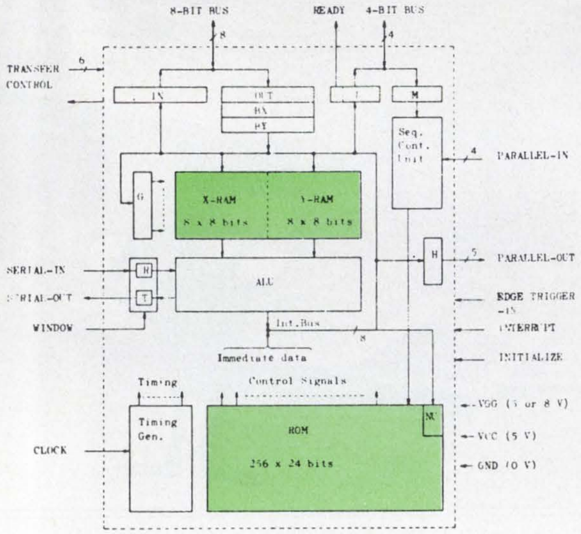
# 4-bit microcomputer, NMOS

## T3444

**Toshiba Transistor Works**
**1 Komukai Toshiba-cho Kawasaki-shi**
**Kanagawa-ken Japan**
**044-511-3111**

Alternate sources: None.

The T3444 is a general-purpose microprogrammable controller and is available either unprogrammed or in two preprogrammed versions: The T3444A is designed as a floppy-disc controller, and the T3444B as a digital cassette controller. All inputs and outputs are TTL compatible and both chips have a 4-bit data bus and the 8-bit command bus. Both buses have three-state capability.




The architecture of the T3444 revolves around two 8 × 8 bit data RAMs that feed in to the ALU. There are 16 lines for dedicated inputs and eight lines dedicated as outputs. The processor also has a separate serial I/O section as well as an on-board clock circuit.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | 8 bits |
| Direct addressing range: | Internal |
| Instruction word size: | 4 bits |
| Number of basic instructions: | N/A |
| Shortest instruction/time | N/A |
| Longest instruction/time | N/A |
| Clock frequency (min/max): | Dc/0.8 MHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | 24 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/200 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| T3444 | Controller, any version | $23. |

### Comments

**The software set** of the T3444 is user determined since the processor is microprogrammable. Program storage space consists of an on-board 256 x 24 bit control memory.

**Software support** consists of a microassembler in Fortran and in G-MAP (Honeywell Computer's assembly language). There is no program library.

**Special features of the software** include a cyclic-redundancy-check capability as well as special functions.

**Hardware support** includes a breadboard circuit consisting of about 110 TTL devices on a board. Program development proceeds by using PROMs in the TTL equivalent.

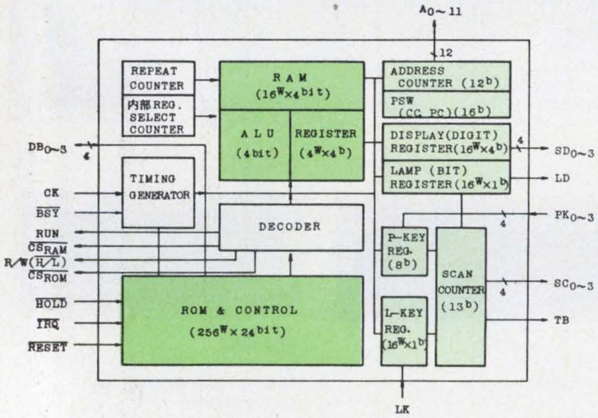
# 4-bit microprocessor, NMOS

## T3472

**Toshiba Transistor Works**
**1 Komukai Toshiba-cho Kawasaki-shi**
**Kanagawa-ken, Japan**
**044-511-3111**

Alternate sources: None.

This microprogrammable 4-bit processor is intended to provide up to a 16-digit numeric display and handle a 64-key input. It is a silicon-gate NMOS device, operates from a single 5-V supply, and its data bus is three-state. A large instruction set (67) includes advanced instructions, like variable-length (1 to 16 digits) decimal/binary arithmetic operations. All inputs and outputs are TTL compatible. A two-level interrupt and 12-bit address bus are other features.




The architecture of the T3472 is oriented for binary and BCD data manipulation and display. All I/O lines are TTL compatible and the data bus has three-state capability. Display control logic and the clock as well as the keyboard scan control circuitry are included on the processor chip.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | 12 bits |
| Direct addressing range: | 4096 words |
| Instruction word size: | 8 bits |
| Number of basic instructions: | 67 |
| Shortest instruction/time (Load immediate): | 33 μs |
| Longest instruction/time (Compare 16 bits): | 360 μs |
| Clock frequency (min/max): | Dc/1 MHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | 16 |
| Package: | 42-pin DIP |
| Power requirements: | 5 V/195 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| T3472 | Microprocessor | $13.00 |
| T3473 | Printer controller (for Seiko CR-101T) | $6.50 |
| T3538 | Printer controller (for Seiko CR-330) | $6.50 |
| T3474 | 16 kbit mask-programmable ROM | $9.50 |

### Comments

**The instruction set** of the T3472 contains a total of 67 commands divided up as follows: 17 data transfer commands, 17 arithmetic instructions, 11 logic operations, four I/O commands, nine branch instructions and nine control operations.

**Software support** for the T3472 consists of a cross-assembler written in Fortran. There is no program library available.

**Special features of the software** include the capability of instructions to handle variable length data (from 1 to 16 digits), and the capability to handle both binary and BCD arithmetic operations.

**Hardware support** for the T3472 consists of the EX-4/01, a board containing 4096 words of RAM, 4096 words of PROM, a control panel with numeric display and a keyboard.

CIRCLE NUMBER 43

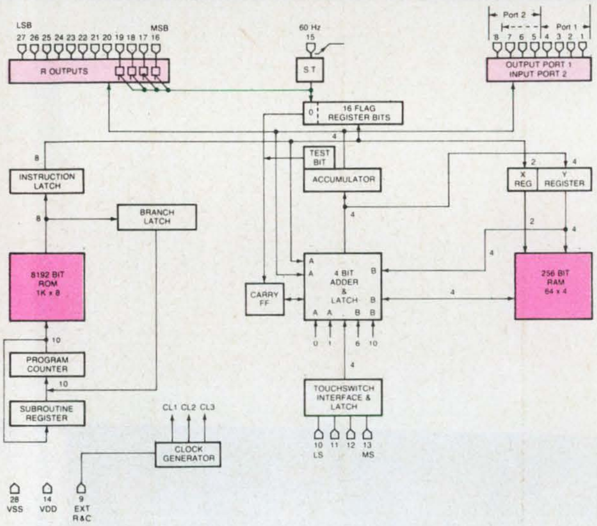
# 4-bit microcomputer, PMOS

## SX 200

Alternate sources: None.

**Essex Group Wire Assembly Division**
**Semiconductor Operations**
**564 Alpha Drive**
**Pittsburgh, PA 15238**
**(412) 963-9322**

A 4-bit PMOS microcomputer in a single 28-pin package, the SX 200, combines CPU with 1024 × 8 bits of ROM and 64 × 4 bits of RAM. In addition to data storage, there are 16 individually settable, resettable and testable flag bits for program control. The outputs are mask programmable via a PLA; some outputs are individually settable and resettable under program control and others output parallel data. Direct input is provided for capacitive touchplates.




The architecture of the SX 200 processor is typical of the small all-in-one microcomputers—the on-chip ROM feeds instructions to the ALU and to the flag register while the RAM provides the workspace. The processor contains its own clock and touch-switch interface to make a complete system using capacitive touchplates to enter data. The output section contains three ports—a 12-bit output port, a 7-bit output port and a 4-bit input port.

### Comments

**The instruction set** contains 41 basic instructions that all execute in one cycle. The instructions can be split into the following groups: three branch instructions, eight constant operations, two bit-manipulation operations, 20 register, accumulator and RAM operations, and eight control and I/O instructions.

**Software support** is provided by the company for the SX 200 in the form of assembly and high-level assembler and simulator programs. There is no program library available.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | 4 bits |
| Direct addressing range: | 1024 bytes (internal) |
| Instruction word size: | 8 bits |
| Number of basic instructions: | 41 |
| Shortest instruction/time (Any): | 20 $\mu$s |
| Clock frequency (min/max): | Dc/400 kHz |
| Clock phases/voltage swing: | 1/internal |
| Dedicated I/O control lines: | 24 |
| Package: | 28-pin DIP |
| Power requirements: | 10 to 18.5 V/25 mA |

### Hardware

| Model | Description | Price |
|---|---|---|
| SX 200 | 4-bit CPU<br>There are no support circuits available. | N/A |

**Special features of the software** start with the fact that all instructions require the same amount of time to execute. The 16 individually settable, resettable and testable flag bits greatly improve program control. Data can be input in BCD, thus simplifying many interfaces.

**Hardware support** consists of a programmable emulator that is used to verify the system and program design.

TEAR OUT

# OPTOELECTRONICS

# Selector Guide and Cross Reference

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**ALABAMA**
Argo and Co., Birmingham 35201; 205/787-4652
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Kierulff Electronics, Phoenix 85040; 602/243-4101

**ARKANSAS**
Carlton-Bates, Little Rock 72209; 501/562-9100

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Cramer Electronics, Irvine 92705; 213/771-8300
Cramer Electronics, Sunnyvale 94086; 408/739-3011
Elmar Electronics, Mt. View 94042; 415/961-3611
Hamilton Electro Sales, Culver City 90230; 213/558-2011
Hamilton/Avnet, Mt. View 94040; 415/961-0272
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Kierulff Electronics, Los Angeles 90022; 213/725-0325
Kierulff Electronics, Palo Alto 94303; 415/968-6292
Kierulff Electronics, San Diego 92123; 714/278-2112
Marshal, G. S., Company, El Monte 91731; 213/686-0141
Schweber Electronics (L.A. Div.) Costa Mesa 92626; 714/556-3880

**COLORADO**
Electronic Parts, Denver 80210; 303/744-1992
Hamilton/Avnet, Denver 80216; 303/534-1212

**CONNECTICUT**
Bond Radio Supply, Waterbury 06702; 203/757-0546
Cramer Electronics, N. Haven 06473; 203/239-5641
Hamilton/Avnet (Georgetown), Wilton 06829; 203/762-0361
Schweber Electronics, Danbury 06810; 203/792-3500

**FLORIDA**
Cramer Electronics, Hollywood 33020; 305/923-8181
Cramer Electronics, Orlando 32814; 305/894-1511
Hamilton/Avnet, Hollywood 33021; 305/925-5401
Schweber Electronics, Hollywood 33020; 305/927-0511

**GEORGIA**
Cramer Electronics, Norcross 30071; 404/448-9050
Hamilton/Avnet, Norcross 30071; 404/448-0800
Lykes Electronics, Norcross 30071; 404/355-2223
Schweber Electronics, Atlanta 30340; 404/449-9170

**ILLINOIS**
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Hamilton/Avnet, Schiller Park 60176; 312/671-6094
Newark Electronics Corp., Chicago 60624; 312/638-4411
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Hutch and Sons, Inc., Evansville 812/425-7201
Pioneer Standard, Indianapolis 46250; 313/478-2700

**IOWA**
Deeco, Inc., Cedar Rapids 52406; 319/365-7551

**KANSAS**
Hamilton/Avnet, Lenexa 66215; 913/888-8900

**LOUISIANA**
Lykes Electronics, Harvey 70059; 504/486-7441

**MARYLAND**
Arrow Electronics, Baltimore 21227; 301/247-5200
Cramer Electronics, Gaithersburg 20760; 301/948-0110
Hamilton/Avnet, Hanover 21076; 301/796-5255
Pioneer Standard (Washington), Gaithersburg 20760; 301/948-0710
Schweber Electronics, Rockville 20852; 301/881-2973

**MASSACHUSETTS**
Cramer Electronics, Newton Center 02159; 617/969-7700
Cushing, T. F., Inc., Springfield 01101; 413/788-7341
Gerber Radio, Dedham 02026; 617/329-2400
Hamilton/Avnet, Woburn 01801; 617/273-2120
Schweber Electronics, Waltham 02154; 617/890-7044

**MICHIGAN**
Hamilton/Avnet, Livonia 48150; 313/522-4060
Pioneer Standard, Livonia 48150; 313/525-1800
R.S. Electronics, Livonia 48150; 313/491-1000
Schweber Electronics, Troy 48084; 313/583-9242
Semiconductor Specialists, Farmington 48024; 313/478-2700

**MINNESOTA**
Cramer Electronics (Bonn), Edina 55435; 612/835-7811
Gopher Electronics, St. Paul 55113, 612/645-0889
Hamilton/Avnet (Minneapolis), Edina 55435; 612/941-3801
Schweber Electronics, Eden Prairie 55343; 612/941-5280
Semiconductor Specialists, Bloomington 55420; 612/854-8841

**MISSOURI**
Hamilton/Avnet, Hazelwood 63042; 314/731-1144
L-Comp, Kansas City 64120; 816/221-2400
Olive Industrial Electric, University City 63130; 314/863-7800

**NEBRASKA**
Scott Electronics, Lincoln 68504; 402/466-8221

**NEW JERSEY**
Arrow Electronics, Moorestown 08057; 609/235-1900
Arrow Electronics, Saddle Brook 07662; 201/797-5800
Cramer Electronics, Little Falls 07424; 201/785-4300
General Radio Supply, Camden 08102; 609/964-8560
Hamilton/Avnet, Cedar Road 07009; 201/239-0800
Hamilton/Avnet, Mt. Laurel 08057; 609/234-0483
Schweber Electronics, Somerset 08873; 201/469-6008

**NEW MEXICO**
Cramer Electronics, Albuquerque 87108; 505/265-5767
Hamilton/Avnet, Albuquerque 87117; 505/765-1500

**NEW YORK**
Arrow Electronics, Farmingdale 11735; 516/694-6800
Cramer Electronics, East Syracuse 13057; 315/437-6671
Cramer Electronics, Hauppauge 11787; 516/231-5600
Cramer Electronics, Rochester 14623; 716/275-0300
Hamilton/Avnet, East Syracuse 13057; 315/437-2641
Hamilton/Avnet, Rochester 14623; 716/442-7820
Hamilton/Avnet, Westbury 11590; 516/333-5800
Rochester Radio Supply, Rochester 14614; 716/454-7800
Rome Electronics, Rome 13440; 315/337-5400
Schweber Electronics, Rochester 14623; 716/461-4000
Schweber Electronics, Westbury 11590; 516/334-7590
Standard Electronics, Cheektowaga 14225; 716/685-4220

**NORTH CAROLINA**
Cramer Electronics, Winston-Salem 27102; 919/725-8711
Dixie Radio Supply, Charlotte 28203; 704/377-5413
Southeastern Radio Supply, Raleigh 27603; 919/828-2311

**OHIO**
Electronic Marketing Corp., Columbus 43212; 614/299-4161
Hamilton/Avnet, Cleveland 44143; 216/461-1400
Hamilton/Avnet, Dayton 45459; 513/433-0610
Hughes Peters, Inc., Cincinnati 45227; 513/351-2000
Hughes Peters, Inc., Columbus 43211; 614/294-5351
Pioneer Standard, Cleveland 44105; 216/587-3600
Pioneer Standard, Dayton 45404; 513/299-7273
REM Electronics, Warren 44482; 216/373-1300
Schweber Electronics, Beachwood 44122; 216/464-2970

**OKLAHOMA**
Oil Capitol Electronics, Tulsa 74145; 918/622-8520

**PENNSYLVANIA**
Almo Electronics Corp., Philadelphia 19114; 215/698-4021
Pioneer Standard, Horsham 19044; 215/674-5710
Pioneer Standard, Pittsburgh 15238; 412/782-2300
Rosen Electronics, York 17403; 717/843-3875
Schweber Electronics, Horsham 19044; 215/441-0600

**RHODE ISLAND**
Edwards, W. H. Company, Warwick 02888; 401/781-8000

**SOUTH CAROLINA**
Dixie Radio Supply, Columbia 29202; 803/779-5332

**TEXAS**
Hamilton/Avnet, Dallas 75240; 214/661-8661
Hamilton/Avnet, Houston 77042; 713/526-4661
Norvell Electronics, Dallas 75240; 214/233-0020
Schweber Electronics, Dallas 75240; 214/661-5010
Schweber Electronics, Houston 77036; 713/784-3600
Sterling Electronics, Dallas 75220; 214/357-9131
Sterling Electronics, Houston 77003; 713/627-9800

**TENNESSEE**
Industrial Electronics, Knoxville 37920; 615/573-7135

**UTAH**
Hamilton/Avnet, Salt Lake City 84119; 801/972-2800
Newark Electronics Corp., Salt Lake City 84115; 801/486-1048

**VIRGINIA**
Sterling/Meridian Electronics, Richmond 23220; 804/359-0221
Virginia Radio Supply, Charlottesville 22901; 804/296-4184

**WASHINGTON**
Almac/Stroum Electronics, Seattle 98108; 206/673-2300
Hamilton/Avnet, Bellevue 98005; 206/746-8750

**WEST VIRGINIA**
McJunkin Corporation, Nitro 24143; 304/348-4907

**WISCONSIN**
Marsh Electronics, Milwaukee 53214; 414/475-6000
Hamilton/Avnet, New Berlin 53151; 414/784-4510

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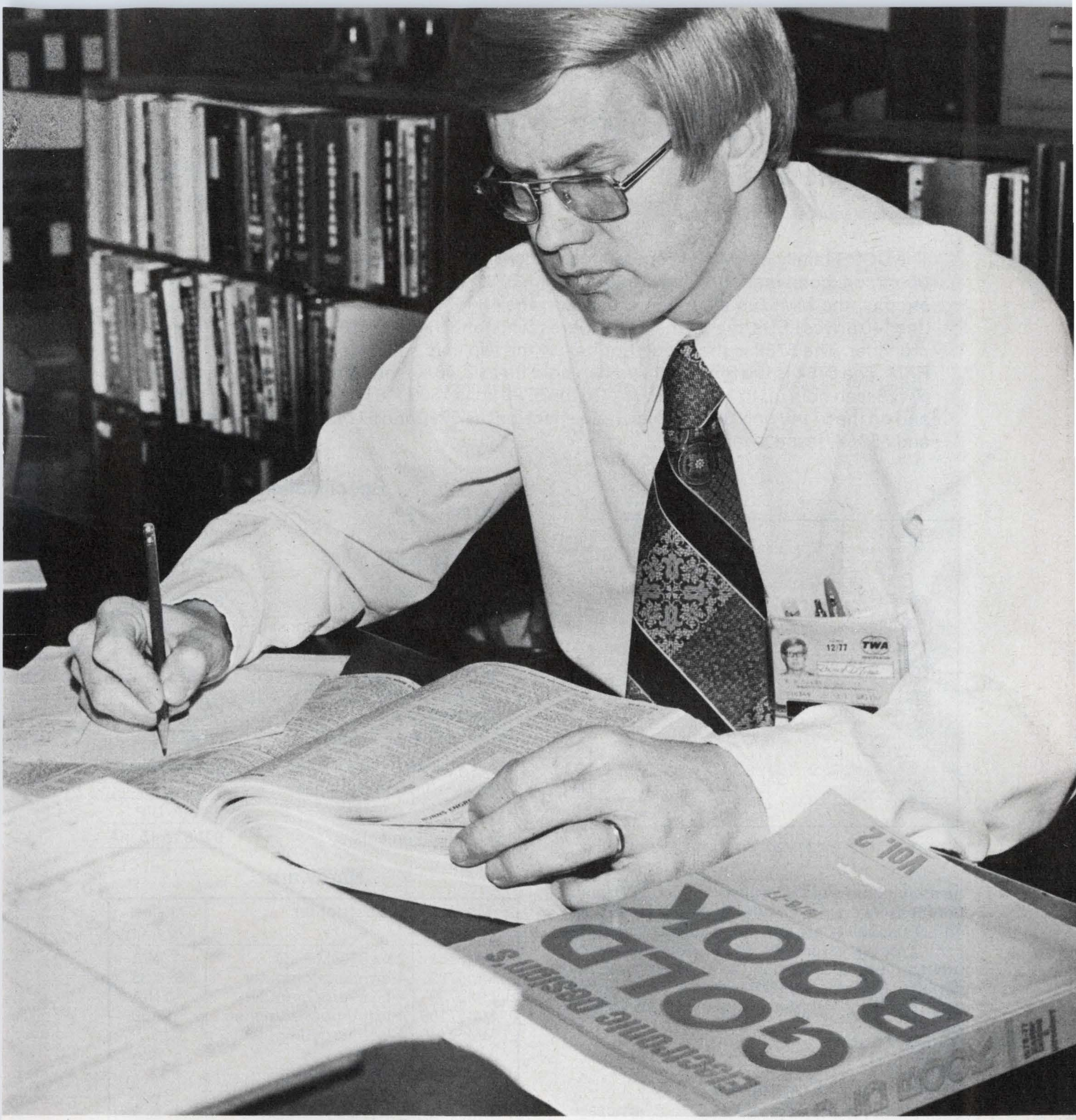
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Electronic Design's

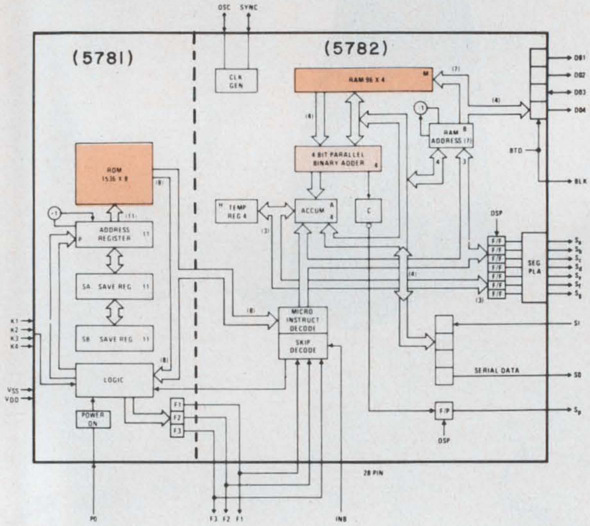
# 4-bit microcomputer, PMOS

## COPS series

Alternate sources: None.

**National Semiconductor, Inc.**
**2900 Semiconductor Dr.**
**Santa Clara, CA 95051**
**(408) 737-5000**

The COPS family of PMOS processor chips consists of four different processor circuits or circuit combinations—the MM5781 and 5782 combination processor and ROM circuits, the MM5799 all-in-one processor, the MM57140/57152 single-chip processor (the 140 drives LEDs, the 152 handles fluorescents) and the MM57109 single-chip number cruncher. The 5782 is the processor half of the two chip set and contains a 160 × 4 bit RAM. The 5781 is the ROM half and can hold up to 2048 × 8 bits (an expansion chip, the 57129, can hold up to 4096 × 8 bits). On the 5799 up to 1500 × 8 bits of ROM are available and on the 57140 only 630 × 8 bits. RAM space on the 5799 and 57140 decreases to 96 × 4 and 55 × 4, respectively.




The architectures of the devices in the COPS family of processors are similar. Variations in memory size and I/O capability are the major differences. Most of the processors provide BCD or seven-segment outputs plus all can handle a direct keyboard interface. Only the MM5782 requires an external clock oscillator all other circuits have internal clocks.

### Comments

**The instruction set** between all four processor models is compatible—the instructions of the smaller processors are a subset of the larger chips. The largest processor MM5799 offers 41 instructions that can be broken down as follows: 18 control and ALU commands, 10 I/O directions and 13 memory operations. The other processors have 36 and 33 (for the 57140 and 5782, respectively). The 57109 has 70 pre-programmed commands to handle calculations.

**Software support** for the COPS series consists of a cross assembler and simulator program available on an IMP-16 computer system. No program library is available.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | Internal |
| Direct addressing range: | Up to 4096 bytes |
| Instruction word size: | 8 bits |
| Number of basic instructions: | 33 to 41 |
| Shortest instruction/time (Single word): | 10 μs |
| Longest instruction/time (Double word): | 50 μs |
| Clock frequency (min/max): | 70/400 kHz |
| Clock phases/voltage swing: | 4 internal |
| Dedicated I/O control lines: | 11 to 24 |
| Package: | 28-pin DIP |
| Power requirements: | 9 V/8 to 15 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| MM5781 | 2 k x 8 ROM & I/O | N/A |
| MM5782 | 4-bit microcomputer | $14.35 |
| MM5799 | 4-bit microcomputer | N/A |
| MM57109 | 4-bit number cruncher | 12.00 |
| MM57140 | 4-bit microcomputer, LED | N/A |
| MM57152 | Same as 140 but fluoresc. | N/A |
| MM5785 | Interface to RAMs | N/A |
| MM5788 | Interface to printer | N/A |
| MM57129 | 4 k x 8 ROM & I/O | N/A |

**Special features of the software** include simple BCD data handling and serial as well as parallel data handling instructions. All instructions require either one or two clock cycles.

**Hardware support** includes the IMP-16P micro-based hardware and software development system, including a ROM simulation capability. Chips without ROMs are also available so that external RAM and PROM can be used for program development.

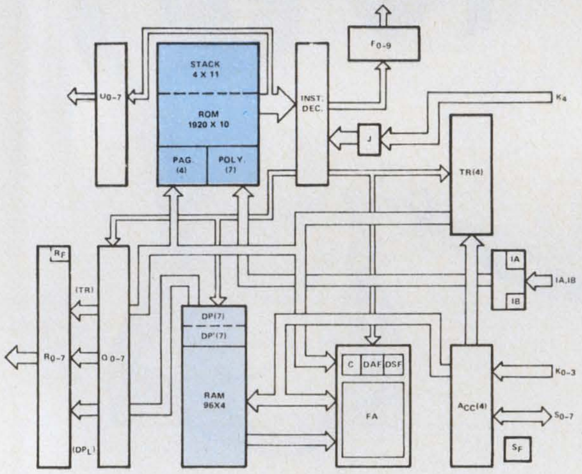
# 4-bit microcomputer, PMOS

## uCOM-42 (uPD548C)

Alternate sources: None.

**NEC Microcomputers, Inc.**
**5 Militia Dr.**
**Lexington, MA 02173**
**(617) 862-6410**

The uCOM-42 is a 4-bit single-chip microcomputer designed for electronic cash register and vending applications. Containing an on-chip ROM of 1920 × 10 bits and a 96 × 4 bit RAM, the processor still has 35 lines available for I/O operations. The I/O lines can handle an 8 × 4 key keyboard as well as an eight-digit LED display and electronic printer without any additional support circuits.




The architecture of the uCOM-42 is designed directly for the electronic cash register market and keyboard controllable appliances. The I/O structure handles an 8 × 4 keyboard, an 8-digit LED display and peripherals. The on-board RAM can also be expanded off the chip. All I/O lines are TTL compatible and all outputs can handle up to −35 V.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | 11 bits (internal) |
| Direct addressing range: | 1920 words (internal) |
| Instruction word size: | 10 bits |
| Number of basic instructions: | 72 |
| Shortest instruction/time (Add): | 10 μs |
| Longest instruction/time (Return from subroutine): | 20 μs |
| Clock frequency (min/max): | 100/200 kHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | 15 |
| Package: | 42-pin DIP |
| Power requirements: | −10 V/−30 mA |

### Hardware

| Model | Description | Price |
|---|---|---|
| uCOM-42 | Microcomputer (5000 qty) There are no specialized support circuits. | $5.50 |

### Comments

**The instruction set** of the uCOM-42 processor contains 72 instructions divided as follows: 11 accumulator manipulation commands, five load/store directives, five data pointer manipulation directions, four register manipulation instructions, three bit manipulation operations, seven skip and jump instructions, three subroutine commands, four interrupt directives, nine I/O operations, 20 port manipulation instructions and one no-operation command.

**Software support** for the uCOM-42 consists of a cross assembler that runs on the company's 8080A-based PDA-80 program development system. Also available is the PDA editor program. There is no program library available.

**Important software features** include the fact that all instructions require just a single cycle. And, many commands are multifunction and have auto increment and auto-decrement capability.

**Hardware support** comes in two forms—an evaluation chip or an evaluation kit. The chip is available so that external ROM or PROM can be used to prepare the program. It also has a hold line to stop operation so that instruction execution can be examined. The other aid is an evaluation kit that provides single-step, breakpoint and register display capabilities.

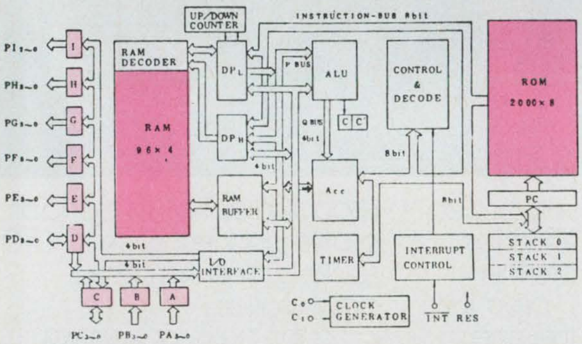
# 4-bit microcomputer, PMOS

NEC Microcomputers
5 Militia Dr.
Lexington, MA 02173
(617) 862-6410

## uCOM-43, uCOM-44, uCOM-45 (uPD546C, 547C, 550C)

Alternate sources: None.

The uCOM-43, 44 and 45 family of all-in-one 4-bit microcomputers is designed for dedicated controller applications. The major differences between the different models is the amount of memory space available on each chip—the 43 is the largest with 2000 × 8 bits of ROM and 96 × 4 bits of RAM. Next step down is the 44 with 1000 × 8 of ROM and 64 × 4 of RAM. The smallest chip is the 45, with a 640 × 8 ROM and a 32 × 4 RAM. Other differences are in the number of I/O lines and a timer included on the uCOM-43 chip.




The architecture of the uCOM 43, 44 and 45 all-in-one processors is the same except for varying amounts of ROM and RAM. All chips have an on-board clock circuit and have TTL compatible I/O lines. The largest circuit, the 43, has an on-board programmable timer, a three-level stack, a flag register and six working registers. The I/O ports are divided as follows: two 4-bit input ports, two 4-bit I/O ports, four 4-bit outputs and one 3-bit output.

### Comments

**The instruction set** consists of 80 commands for the uCOM-43 and each of the instruction sets for the 44 and 45 are just subsets of the 80. The 44 and 45 have 58 instructions in their repertoire. The major instruction set is broken down as follows: six arithmetic, 11 jump, branch and skip, 11 I/O, two timer, 26 register and memory manipulation, three comparison and 10 register exchange operations.

**Software support** is provided by a cross assembler that runs on the company's 8080A-based PDA-80 hardware and software development system. Also available is the PDA-80 editor program and a Fortran IV cross assembler for a 16-bit host computer. There is no program library available.

**Special features of the software** start with the fact that 73 of the 80 instructions require just a single byte. Six instructions provide multiple functions. There are also a total of 25 test-and-skip directions.

**Hardware support** for the uCOM-43, 44 and 45 starts with the uPD556D evaluation chip, which is the same as the uCOM-43 except that the address lines for the ROM are now available for external program memory. Also available is an evaluation kit that provides single-step, breakpoint and register display operations to aid program development.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | Internal |
| Direct addressing range: | Up to 2000 bytes |
| Instruction word size: | 8 bits |
| Number of basic instructions: | 80 (max.) |
| Shortest instruction/time (Clear accumulator): | 9.1 μs |
| Longest instruction/time (Return to subroutine): | 36.4 μs |
| Clock frequency (min/max): | 150/440 kHz |
| Clock phases/voltage swing: | 1/Internal |
| Dedicated I/O control lines: | 21 to 35 |
| Package: | 42-pin DIP |
| Power requirements: | −10 V/−30 mA |

### Hardware

| Model | Description | Price |
|---|---|---|
| uCOM-43 | 4-bit microcomputer | $5.50 |
| uCOM-44 | 4-bit microcomputer | 3.40 |
| uCOM-45 | 4-bit microcomputer | 2.70 |
| | All prices are for 50,000 qty purchases. | |
| | There are no support circuits available. | |

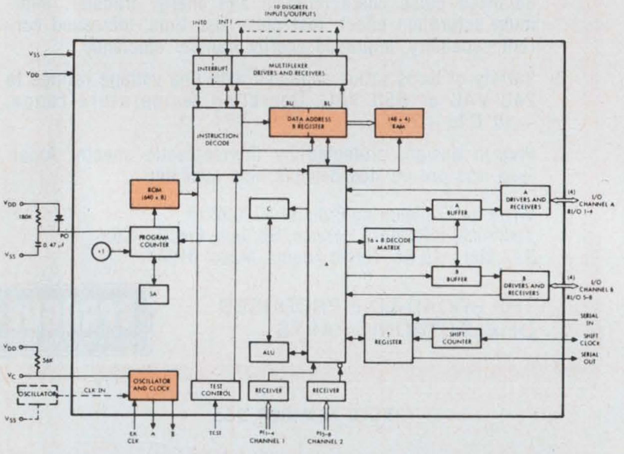
# 4-bit microcomputer, PMOS

## PPS-4/1 family

**Rockwell International**
**P.O. Box 3669**
**Anaheim, CA 92803**
**(714) 632-3729**

Alternate sources: AEG Telefunken.

A family of 4-bit, single-chip, microcomputers, the PPS-4/1 Models MM75, 76, 77 and 78 include CPU, RAM, ROM, I/O and clock circuitry on a single chip. On-board ROM ranges from 640 to 2048 bytes and on-chip RAM spans 48 to 128 4-bit words. Three special versions of the MM76 are also available—the E version with an expanded ROM, the D version with an a/d converter and the C model with a high-speed counter.




The architecture of the PPS-4/1 devices resembles that of a complete minicomputer—all the necessary circuits are included on a single chip. All chips except the MM77 and 78 have a 48 × 4 bit on-board RAM. The 77 and 78 contain 96 × 4 and 128 × 4 RAMs, respectively. All chips have one 8-bit bidirectional port as well as two conditional interrupt lines, except for the MM75 which has only one interrupt.

### Comments

**The instruction set** of the PPS-4/1 processors is divided into nine basic categories—RAM addressing commands, bit-manipulation directions, register-to-register operations, arithmetic instructions, ROM addressing commands, logic comparison instructions, I/O directions, conditional transfer operations and register/memory instructions.

**Software support** for the PPS-4/1 family consists of a Fortran IV cross assembler available either for direct purchase or on time-sharing networks (GE and Tymshare). Also available is the PPS MP Universal Assemulator that contains supervisors, assemblers, and a text editor as well as debug routines.

**Software features** include specialized instructions for the software controllable converter and counter in the MM76D and C versions, as well as a large number of general-purpose I/O commands.

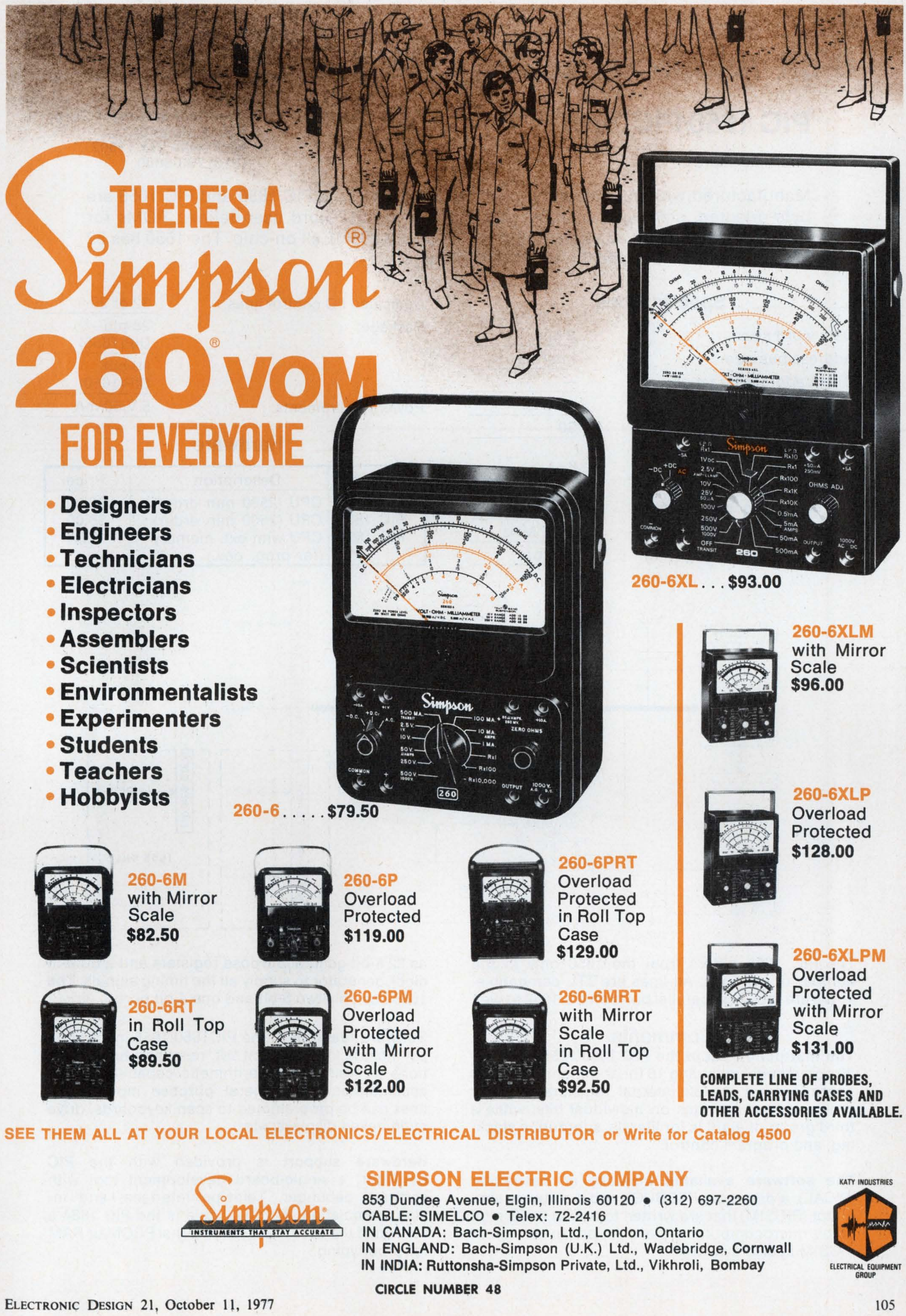
### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | Internal |
| Direct addressing range: | Internal |
| Instruction word size: | 8 bits |
| Number of basic instructions: | 67 to 69 |
| Shortest instruction/time (Most): | 12.5 $\mu$s |
| Clock frequency (min/max): | 40/120 kHz |
| Clock phases/voltage swing: | Internal |
| Dedicated I/O control lines: | 22 to 39 |
| Package: | 28 pin DIP or 42 and 52-pin QUILs |
| Power requirements: | 15 V/5 mA |

### Hardware

| Model | Description | Price (1000 qty) |
|---|---|---|
| MM75 | CPU with 640 bytes of ROM | $6.10 |
| MM76 | CPU with 640 bytes of ROM | 8.00 |
| MM76C | CPU with counter | |
| MM76D | CPU with a/d converter | |
| MM76E | CPU (expanded MM76) | |
| MM77 | CPU with 1344 bytes of ROM | 9.50 |
| MM78 | CPU with 2048 bytes of ROM | 10.75 |

**Hardware support** for the PPS-4/1 family consists of various processor modules that plug into the PPS MP Universal Assemulator—the complete resident development system for the family. There are also a wide number of support modules for the Assemulator—memory, I/O, personality and prototyping cards are available.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# 8-bit microcomputer, NMOS

## PIC 1650/PIC 1655

Alternate sources: None.

**General Instrument Corp.**
**600 W. John St.**
**Hicksville, NY 11802**
**(516) 733-3000**

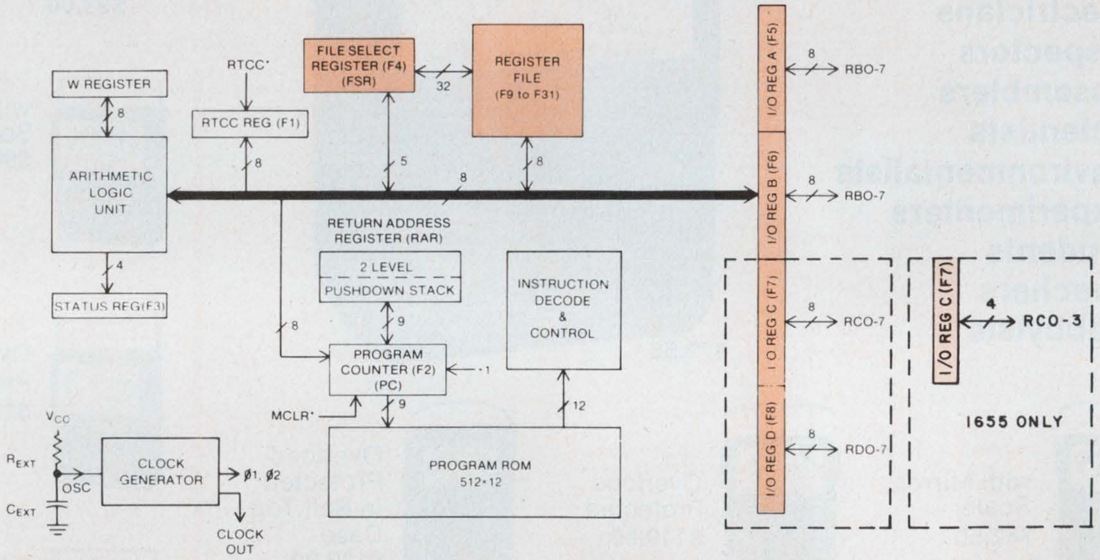
Manufactured with ion-implant, n-channel processing, the PIC 1650 and PIC 1655 are byte-oriented, stand-alone processors that include 512-word user-defined ROMs for program storage and 32 eight-bit internal registers (RAM), all on-chip. The 1650 has 32 user-defined I/O lines and the 1655 has 20 lines.

### Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | Internal |
| Direct addressing range: | — |
| Instruction word size: | 12 bits |
| Number of basic instructions: | 30 |
| Shortest instruction/time (Most): | 4 μs |
| Longest instruction/time (Program counter skips): | 8 μs |
| Clock frequency (min/max): | 0.1/1 MHz |
| Clock phases/voltage swing: | Internal |
| Dedicated I/O control lines: | 32 or 20 |
| Package: | 28-pin DIP(1655)<br>40-pin DIP(1650) |
| Power requirements: | 5 V/50 mA |

### Hardware

| Model | Description | Price |
|---|---|---|
| PIC 1650 | CPU (2500 min order) | $8.00 |
| PIC 1655 | CPU (2500 min order) | $6.00 |
| PIC 1664 | CPU with ext. memory (for prog. dev.) | N/A |




The PIC 1655 differs from the 1650 only in the number of I/O lines. All lines are TTL compatible. There are four 8-bit parallel ports on the 1650 as well as 32 8-bit general-purpose registers and a built-in clock generator to supply all the timing signals. The 1655 has only two 8-bit and one 4-bit ports.

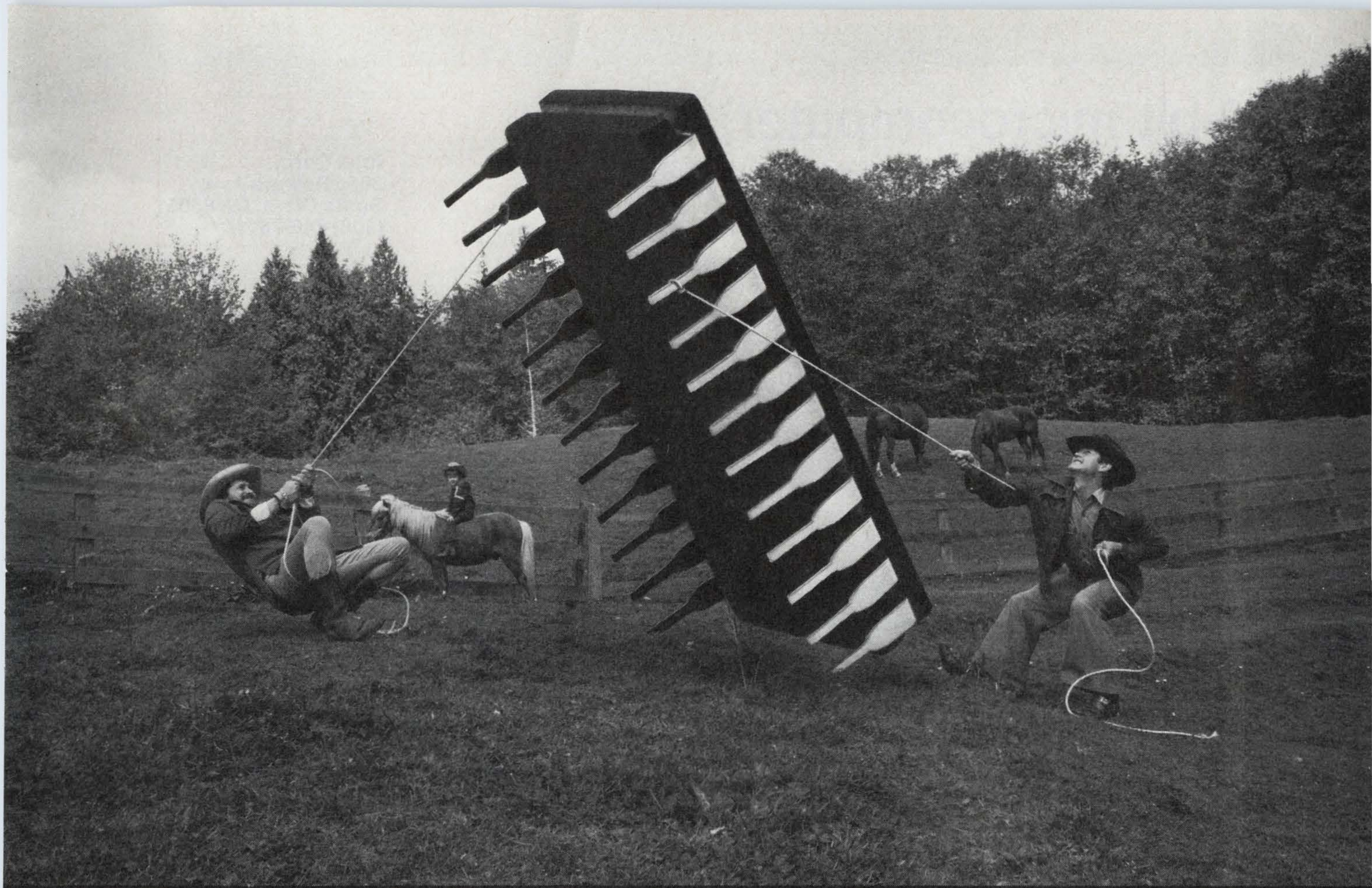
### Comments

**The instruction set of the PIC 1650/1655 contains** 30 commands, including 18 for arithmetic and logic operations on the 32 internal registers. Another group of four operates on individual bits, while a third group of eight is for literals, subroutine stacking, and program control.

**The software available** includes an assembler (PICAL), a debugger (PICBUG), and a software simulator (PICSIM) that are written to run on the Gimini 16-bit microcomputer system. A Fortran version of PICSIM is also available.

**Software features** of the PIC1650/1655 instruction set include individual bit set, reset and test operations as well as BCD arithmetic capability in the accumulator. The general purpose input/output lines can be programmed to scan keyboards, drive multiplexed displays, etc.

**Hardware support** is provided with the PIC Emulator, a single-board development tool with software debugger, Teletype interface, and in-circuit emulation. Also available is the PIC 1664 a version of the 1650 that uses external PROM or RAM for prototyping.



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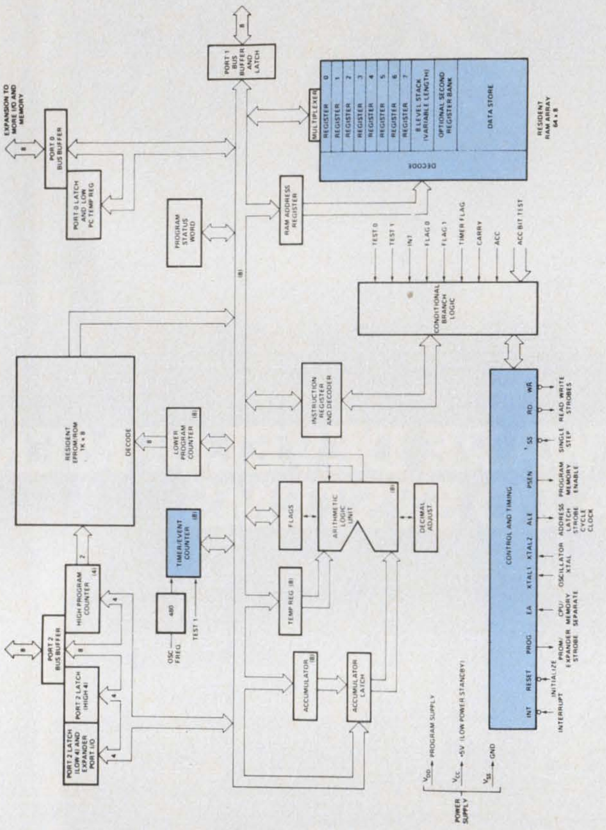
# 8-bit microcomputer, NMOS

## MCS-48 (8035, 8048 and 8748)

**Intel Corp.**
**3065 Bowers Ave.**
**Santa Clara, CA 95051**
**(408) 246-7501**

Alternate sources: Advanced Micro Devices, NEC and Signetics (Philips) are official second sources via mask exchange.

There are three versions of the basic processor available—the 8035, which is just a processor without any on-chip program memory; the 8048, which has the processor along with 1024 bytes of mask-programmable ROM on the same chip; and the 8748, which contains the processor and 1024 bytes of UV erasable PROM on the same chip. All three versions are made via an NMOS silicon-gate process and contain a 64 × 8 data RAM, 27 I/O lines, a counter/timer and an on-board clock generator in addition to the processor. And, all three versions of the processor are pin-compatible.



The basic architecture of the MCS-48 family is highly bus oriented, with almost every sub block tied into the bus. All three eight-bit ports provide latched outputs. If more program memory is needed than is on the chip, ports 0 and 2 can be used to output an address to external memory.

### Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | 12 bits |
| Direct addressing range: | 4096 words |
| Instruction word size: | 8 bits |
| Number of basic instructions: | 96 |
| Shortest instruction/time (50% of commands): | 2.5 $\mu$s |
| Longest instruction/time (remaining 50%): | 5 $\mu$s |
| Clock frequency (min/max): | 1/6 MHz |
| Clock phases/voltage swing: | Internal/TTL |
| Dedicated I/O control lines: | 27 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/65 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| 8035 | CPU without ROM | $13.55 |
| 8048 | CPU with mask-programmed ROM | consult factory |
| 8748 | CPU with UV PROM | $175.00 |
| 8155 | RAM, I/O & timer | 14.00 |
| 8205 | 1 of 8 binary decoder | 2.80 |
| 8212 | 8-bit I/O port | 2.90 |
| 8214 | priority interrupt | 4.65 |
| 8216 | Bidirectional bus drive | 2.75 |
| 8226 | Inverting bus driver | 2.75 |
| 8243 | I/O expander | 5.00 |
| 8253 | Programmable timer | 17.55 |
| 8259 | Interrupt controller | 17.20 |
| 8279 | Keyboard/display interface | 14.10 |
| 8355 | ROM & I/O expander | c.f. |
| 8755 | UV PROM & I/O | 125.00 |

### Comments

**The instruction set** of the MCS-48 family consists of 96 instructions split into 24 register operations, 26 accumulator operations, 23 conditional and unconditional transfers, 13 I/O control instructions and 10 other system control instructions.

**Software support** for processors includes a macro-assembler on paper tape or floppy disc, a resident text editor in the MDS development system and Debug software as part of the ICE-48 in-circuit emulator system. Also, MCS-48 programs are available through the company's Insite program library, which contains over 350 programs.

**Unique features of the software** include AND and OR operations directly to the I/O ports for bit set and reset operations. Accumulator bit test operations and indirect fetch for table look-ups are also possible.

**Hardware support** includes the Prompt-48, a bench-top stand-alone development system and the Intellec Microprocessor Development System (MDS), a full microcomputer based system with 16 k of RAM and 2 k of ROM and software and hardware interfaces for peripherals.

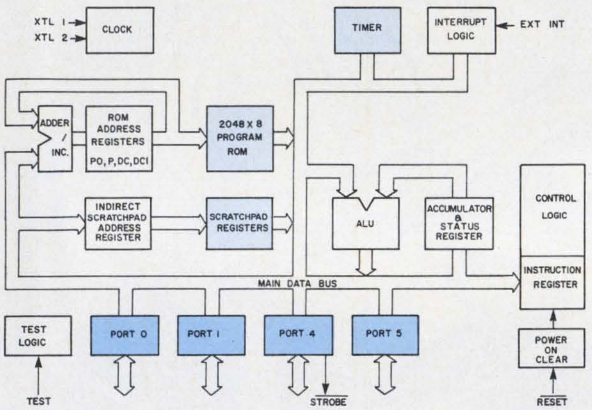
# 8-bit microcomputer, NMOS

## MK3870

**Mostek Corp.**
**1215 W. Crosby Rd.**
**Carrollton, TX 75006**
**(214) 242-0444**

Alternate sources: Fairchild and Motorola.

A complete microcomputer on a single chip, the MK3870, can execute the instruction set of the F8. The 8-bit device executes more than 70 instructions, allowing expansion into multichip configurations with software compatibility. Featured on-board are 2048 bytes of ROM and 64 bytes of scratchpad RAM. The processor operates from a single 5-V supply and contains 32 lines of bidirectional I/O and a programmable timer.




The architecture of the 3870 is identical to that of the original F8, with the extra features of ROM and RAM added to the original chip. Also included on the chip is an 8-bit timer and an 8-bit prescaler. The 3870 can form a complete processor system without any other additional circuits aside from the power supply. All lines are TTL compatible.

### Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | 11 bits (internal) |
| Direct addressing range: | 2048 words |
| Instruction word size: | 8,16, or 32 bits |
| Number of basic instructions: | 76 |
| Shortest instruction/time (Register reference): | 2 μs |
| Longest instruction/time (Subroutine call): | 13 μs |
| Clock frequency (min/max): | 1/4 MHz |
| Clock phases/voltage swing: | Internal |
| Dedicated I/O control lines: | 32 I/O lines plus two control lines |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/70 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| MK3870 | 8-bit microcomputer | $19.00 |
| MK3850N | F8 CPU | 10.75 |
| MK3853N | Static memory interface | 9.50 |
| MK3871N | Parallel I/O and timer | 9.50 |

### Comments

**The instruction set** of the 3870 is compatible with that of the F8 processor. There are 76 basic instructions, divided as follows: 15 accumulator reference, eight memory reference, 12 branch and jump, 13 address modification, 15 scratchpad memory reference and 13 miscellaneous control instructions.

**Software support** for the 3870 processor includes resident debug, edit and assembly programs, nonresident Fortran-IV cross assembler for 16-bit and larger minicomputers, and many ROM-based software packages. There is no general program library, but the factory can be consulted for specific program needs.

**Important features of the software** include compact instruction codes (60% of the instructions require just one byte), auto-incrementing and auto-decrementing are possible, register and memory pointers are available, the processor can perform relative addressing and all I/O instructions require a single byte.

**Hardware support** for the 3870 includes the F8 evaluation kit with 1024 bytes of RAM, a TTY monitor with breakpoint capability and a Fortran cross assembler. An assembler, editor and debug routine are also available on the company's SDB-50/70 software development board. The largest system is the AIM-70, a complete real-time emulation system that provides snapshot software in ROM.

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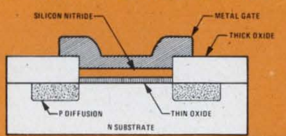


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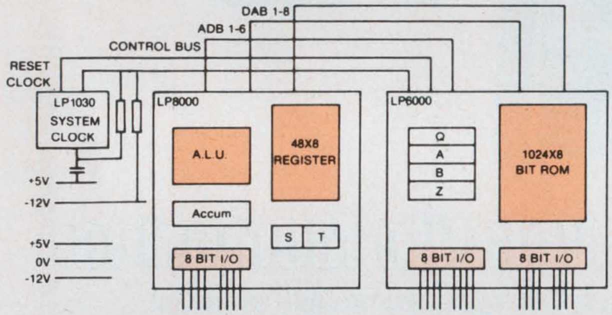
# 8-bit microcomputer, PMOS

## Series 8000

**General Instrument Corp.**
**600 West John Street**
**Hicksville, NY 11802**
**(516) 733-3000**

Alternate sources: AEG and SGS-ATES.

The Series 8000 logic processor system is a multiple-chip set—the LP8000 processor chip, the LP6000 control memory and the LP1030 clock generator. Able to access 16 kwords over its all-MOS-level buses the Series 8000 system offers 24 bidirectional I/O lines. There are 48 general-purpose 8-bit registers on the LP8000 as well as an 8-bit bidirectional I/O port. The LP6000 control memory contains 16 lines of bidirectional I/O in addition to the 1 k × 8 control program.




The architecture of the Series 8000 is based on a three-chip set—the CPU, ROM and clock generator. In the processor is an 8-bit ALU, a 48 × 8 register file, a four-word address stack and eight bidirectional I/O lines. The 8-bit data bus and 6-bit control bus combine to provide a 14-bit memory address.

### Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | Internal |
| Direct addressing range: | 16,384 bytes |
| Instruction word size: | 8 bits |
| Number of basic instructions | 51 |
| Shortest instruction/time (many): | 5 $\mu$s |
| Longest instruction/time (Load accumulator from module indirect) | 15 $\mu$s |
| Clock frequency (min/max): | 500/800 kHz |
| Clock phases/voltage swing: | 1/11 V |
| Dedicated I/O control lines: | 24 (3-chip syst.) |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/30 mA<br>−12 V/70 mA<br>(LP8000 only) |

### Comments

**The instruction set** consists of 48 basic commands that are divided as follows: 11 register operations, nine jump instructions and 31 accumulator operations (including Binary and BCD Add, logic OR, AND and Exclusive-OR, and Compare).

**Software support** for the Series 8000 is composed of a Fortran IV cross assembler and simulator that can run on many minicomputer systems or is available from various time-sharing vendors. There is no program library available.

**Special features of the software** include the many accumulator operations and the multiple position bit shifts possible when handling BCD arithmetic.

**Hardware support** consists of several modules that permit ROM or PROM to be used to develop the software. There is also a prototyping system available—the GIC 8000—that has resident hardware and software debug aids.

### Hardware

| Model | Description | Price* (100 qty) |
|---|---|---|
| LP8000 | 8-bit processor chip | $10.00 |
| LP6000 | 1 k × 8 ROM& 16 I/O lines | 10.00 |
| LP1000 | Memory interface | 8.50 |
| LP1010 | I/O buffer | 7.50 |
| LP1030 | 800 kHz clock generator | 2.50 |
| | *Main market emphasis is in Europe. | |

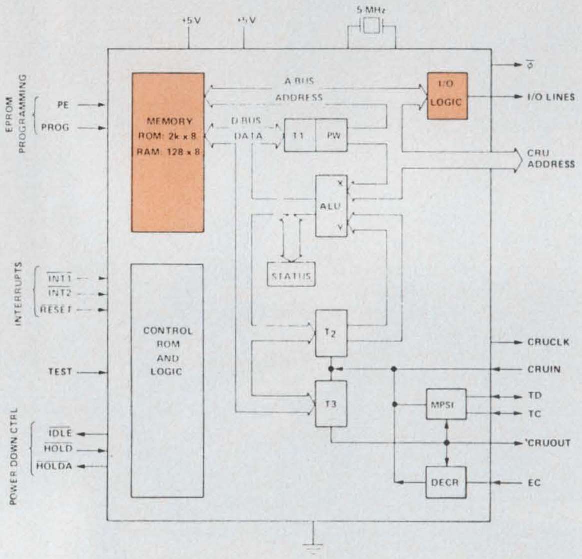
# 16-bit microcomputer, NMOS

## TMS 9940

**Texas Instruments Inc.**
**P. O. Box 5012, M/S 308**
**Dallas, TX 75222**
**(214) 238-2011**

Alternate sources: None.

A 16-bit CPU, with RAM, EPROM and I/O circuitry contained in a single 40-pin package. The TMS 9940 also contains a timer/event counter, a flag register, and reconfigurable I/O. Instructions are compatible with the TMS 9900 and, in addition, include two new instructions for manipulating BCD data and a single LIIM instruction to load an interrupt mask. Memory-to-memory architecture features multiple register files, in RAM, for faster response to interrupts and greater programming flexibility. The processor implements four levels of interrupts including the internal decrementer, which can be programmed as a timer or event counter.




The TMS 9940 is a complete 16-bit computer system on a single chip. On the chip are 2048 bytes of ROM or UV PROM, 128 bytes of RAM, as well as an event counter/timer, a flag register and up to sixteen reconfigurable I/O lines. Even the clock generator is included on the chip. All lines are TTL compatible and the I/O lines are software configurable as either inputs or outputs.

### Specifications

| | |
|---|---|
| Data word size: | 16 bits |
| Address bus size: | 15 bits |
| Direct addressing range: | 32,768 words |
| Instruction word size: | 16 to 48 bits |
| Number of basic instructions: | 68 |
| Shortest instruction/time (Jump): | 2 $\mu$s |
| Longest instruction/time (Divide): | 45.2 $\mu$s |
| Clock frequency (min/max): | Dc/5 MHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | 16 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/160 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| TMS 9940 | 16-bit all-in-one CPU | N/A |
| TMS 9901 | Programmable interface | $8.75 |
| TMS 9902 | Asynchronous interface | 7.50 |
| TMS 9905 | 8:1 multiplexer | 1.26 |
| TMS 9906 | 8-bit latch | 1.55 |
| TMS 9907 | 8:3 priority encoder | 1.01 |
| TMS 9908 | 8:3 priority encoder | 1.01 |

### Comments

**Software for the TMS 9940** consists of all the instructions available on the TMS/SBP 9900 except for four commands that aren't applicable to the all-in-one configuration. Also, three new instructions have been added to simplify the manipulation of BCD coded data and to simplify masking operations. The 9940 can handle four levels of interrupt, and includes an internal decrementer that can be programmed as a timer or event counter.

**Support software** for the TMS 9940 consists of assemblers, editors, simulators and debuggers. High-level languages will also be available shortly. There is also a program library available since most software is code compatible with the company's 990 series of minicomputers.

**The most outstanding features** of the software include the multiple register file capability and the flexibility it offers. The processor makes use of the minicomputer instruction set of the 990 series, including hardware multiply and divide commands. The software controllable counter/timer also provides a handy capability to implement timing loops.

**Hardware support** for the TMS 9940 includes all the support for the 9900—the TM 990 microcomputer modules, the PX 990 cassette-based prototyping system, and AMPL, a floppy-disc based development system. And, since most of the software is 990 code compatible, all the mini hardware is also at the designer's disposal.

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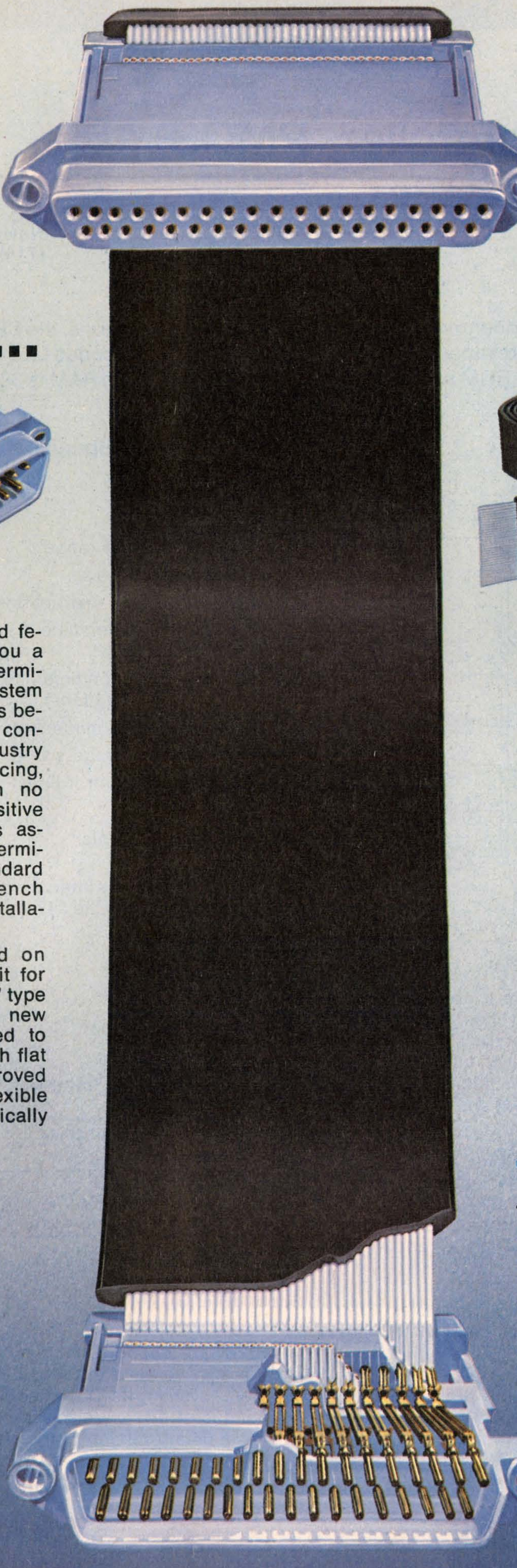

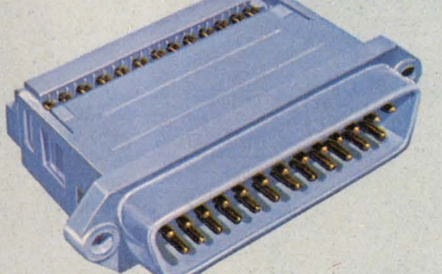

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**CIRCLE NUMBER 53**

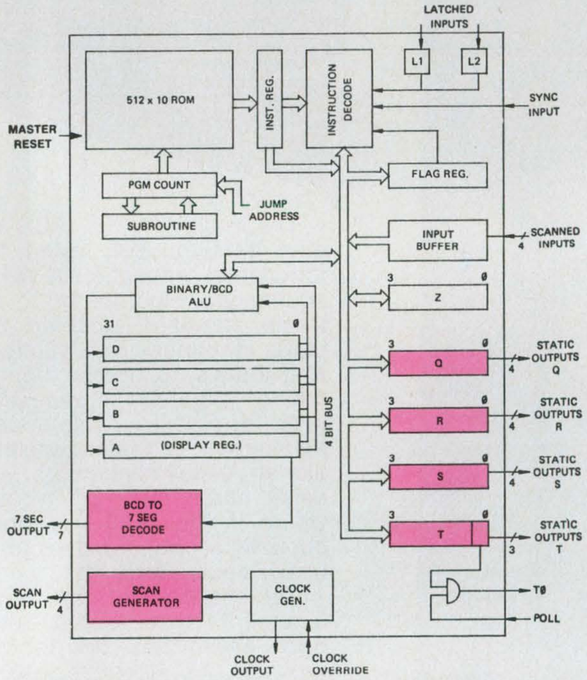
# 4-bit microcontroller, PMOS

## CR1872

**Western Digital**
**3128 Red Hill Ave.**
**P.O. Box 2180**
**Newport Beach, CA 92663**
**(714) 557-3550**

Alternate sources: None.

A low-cost 4-bit microcontroller for dedicated control applications, the CR1872 includes a direct interface for keyboard or thumbwheel switches and decoded LED segment driver outputs. The on-chip ROM holds 512 × 10 bits, and the on-chip RAM is 32 × 4 bits.




The stand-alone processor has scanned inputs and decoded outputs: seven input lines, 16 output lines, and LED segment driver outputs. All lines are compatible with TTL or CMOS logic families. In addition to the 512 × 10 bit on chip ROM, the 1872 has a 32 × 4 bit scratchpad RAM and on-board clock generator.

### Comments

**The instructions set** is broken into four groups: program control (6), conditions (14), I/O (5), and ALU (9). All instructions are optimized for dedicated control applications and BCD data handling and display.

**Software support** consists of Assembler, Editor, and Simulator programs which can run on PDP-11 minicomputers.

**The software set used by this processor is optimized** for dedicated controller applications. A version of the processor pre-programmed as a timer is available for evaluation.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | None* |
| Direct addressing range: | None* |
| Instruction word size: | 10 bits |
| Number of basic instructions: | 34 |
| Shortest instruction/time (Load Literal): | 1 cycle |
| Longest instruction/time (BCD/ALU operations): | up to 32 cycles |
| Clock frequency (min/max): | 5 kHz/150 kHz |
| Clock phases/voltage swing: | Internal or 1/5V |
| Dedicated I/O control lines: | 30 |
| Package: | 40-pin DIP |
| Power requirements: | 12 V/5 mA typ |

*The address bus is internal so the direct addressing range is limited to the 512 words of on-board ROM.

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| CR1872 | CPU<br>No other support circuits available. | $11.00 |

**Hardware support** includes a prototyping system that can be used in the SC/MP low-cost development system (LCDS) made by National Semiconductor. There is also a circuit card available that has a 64-pin version of the chip to permit external PROM connections for program development.

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CIRCLE NUMBER 54

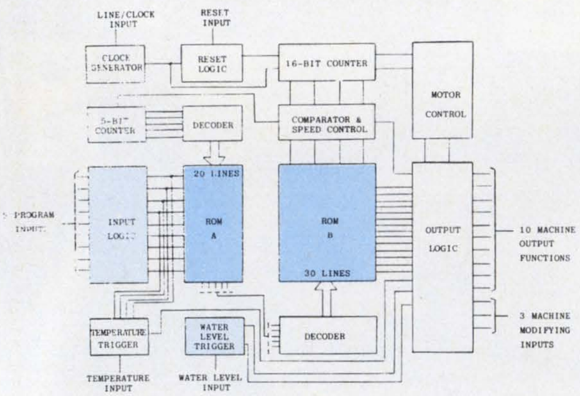
# 4-bit microcontroller, PMOS

## 7150

**ITT Semiconductors**
**74 Commerce Way**
**Woburn, MA 01801**
**(617) 935-7910**

Alternate sources: None.

The 7150 microcontroller is designed for low-cost control of large appliances such as dishwashers and washing machines. It is a dedicated controller and does no calculations. There are 15 possible control input lines and 10 machine control output functions. The circuit is available in either an 18, 24 or 28-pin DIP, depending upon the number of control lines needed by the application. With the on-board ROMs, up to 10 machine control functions of up to 20 program steps each, can be defined.




The architecture of the 7150 uses two ROMs to control the various output functions. There is no ALU since no data manipulation is required. However, there are two analog inputs to the processor that are used with an on-chip difference amplifier to form a temperature sensing circuit.

### Comments

**The instruction set** of the 7150 is strictly internal—all commands are predetermined by the manufacturer and the multiple program inputs determine the sequence of instruction execution.

**Software support** is nonexistent since the 7150 comes factory programmed.

**Unusual software features** include special subroutines and a capability to speed up programs by a factor of 64.

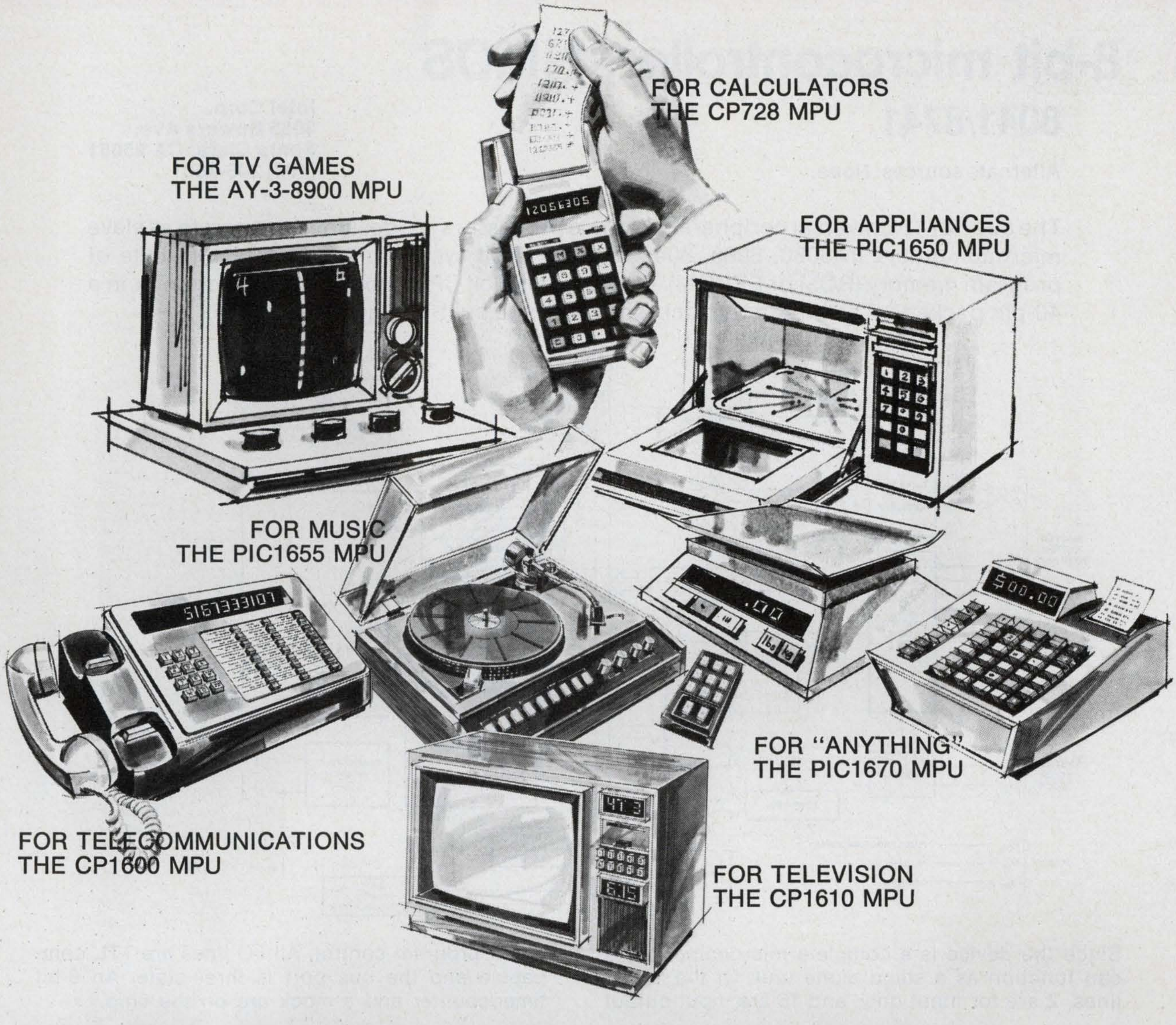
### Specifications

| | |
|---|---|
| Data word size: | Internal |
| Address bus size: | Internal |
| Direct addressing range: | Internal |
| Instruction word size: | Internal |
| Number of basic instructions: | N/A |
| Shortest instruction/time (Not applicable): | N/A |
| Longest instruction/time (Not applicable): | N/A |
| Clock frequency (min/max): | Dc/25 kHz |
| Clock phases/voltage swing: | 1/10 V |
| Dedicated I/O control lines: | 25 (max) |
| Package: | 18, 24 or 28-pin DIP |
| Power requirements: | −15 V/30 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| 7150 | Microcontroller | N/A |
| 7121 | Program positioner | N/A |
| 7122 | Display driver | N/A |

**Hardware support** is nonexistent. All that is available are the two support circuits for program position and numeric display.

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CIRCLE NUMBER 55

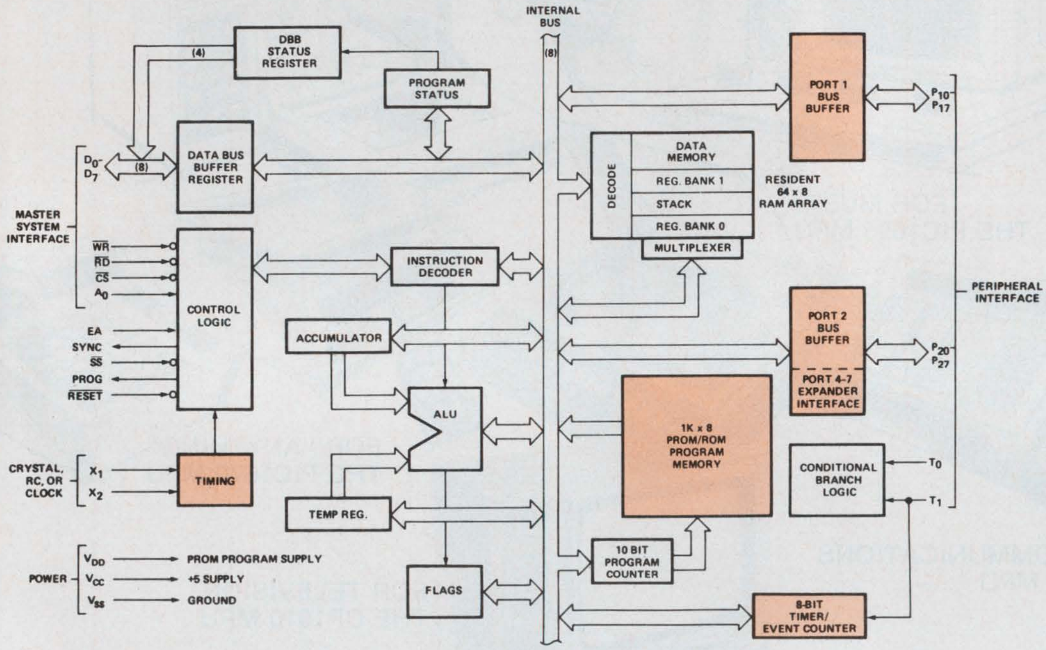
# 8-bit microcontroller, NMOS

## 8041/8741

Alternate sources: None.

Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 95051
(408) 246-7501

The 8041/8741 Universal peripheral interface processors are designed to operate as slave microcomputers in 8080, 8085, 8048 or other 8-bit systems. They contain 1 kbyte of program memory (ROM or EPROM), I/O ports, an 8-bit CPU, clock and timer/counter in a 40-pin package. The interface processor also has a built-in single-step mode.




Since the device is a complete microcomputer, it can function as a stand alone unit. Of the 18 I/O lines, 2 are for input only, and 16 are input-output under program control. All I/O lines are TTL compatible and the bus port is three-state. An 8-bit timer/counter and a clock are on the chip.

### Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | 10 bits |
| Direct addressing range: | 1024 words |
| Instruction word size: | 8 bits |
| Number of basic instructions: | 90 |
| Shortest instruction/time (Many instructions*): | 2.5 $\mu$s |
| Longest instruction/time (Many instructions): | 5 $\mu$s |
| Clock frequency (min/max): | 1 MHz/6 MHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | 18 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/65 mA |

* The instruction set is divided about 50/50 between 2.5 and 5 $\mu$s instructions.

### Comments

**Included in the set of 90 instructions** are 14 data moves, 28 accumulator and register operations, six flag, 20 branch and subroutine call, 12 timer and control and 10 I/O commands. All instructions are either one or two bytes and are executed in one or two machine cycles.

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| 8041 | ROM version of UPI | N/A |
| 8741 | UV PROM version of UPI | $156. |
| 8243 | I/O expander | |

**Support software** consists of a macro assembler that can be used on the company's Intellec Microprocessor Development System.

**Software features** allow asynchronous data, commands and status to be transferred to an external (master) processor. Both 8-bit I/O ports are software configurable to act as inputs or outputs on a line by line basis. The internal counter/timer is software controllable.

**Essentially the same hardware support** offered for 8080 systems is used with the 8041/8741. This includes the Intellec Microcomputer Development System (MDS) and the ICE-41 in-circuit emulator. When used as a slave unit in an 8080 based system, the device can perform keyboard scanning, printer control and display multiplexing.

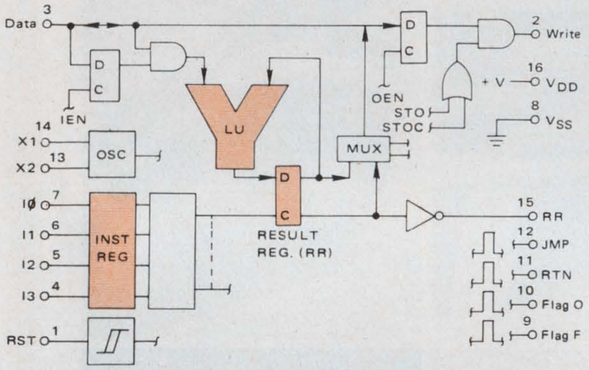
# 1-bit microprocessor, CMOS

## MC14500B ICU

Alternate sources: None.

**Motorola**
**5005 E. McDowell Rd.**
**Phoenix, AZ 85036**
**(602) 244-3716**

Designed as a programmable logic controller, the single chip, 1-bit CMOS industrial control unit replaces multi-bit processors or hardwired logic in decision-oriented tasks. Housed in a 16-pin package, the device accepts 16 four-bit instructions. Each instruction performs logical operations on data appearing on a 1-bit bi-directional data line. The main attribute of the device is its simplicity in control system applications.




A minimum system consists of the processor, an external memory, program counter, 8-channel data selector and an 8-bit addressable latch. Instruction lines are TTL compatible and the 1-bit bi-directional data line has three-state capability. On-chip there are three 1-bit registers that are directly addressable, and the clock oscillator.

### Specifications

| | |
|---|---|
| Data word size: | 1 bit |
| Address bus size: | Variable |
| Direct addressing range: | As determined by adress bus |
| Instruction word size: | 4 bits |
| Number of basic instructions: | 16 |
| Shortest instruction/time (All are performed in same time): | 1 $\mu$s |
| Clock frequency (min/max): | dc/1 MHz |
| Clock phases/voltage swing: | 1/supply voltage |
| Dedicated I/O control lines: | 4 |
| Package: | 16-pin DIP |
| Power requirements: | 3 to 18 V/2 mA |

### Comments

**Sixteen 4-bit instructions** comprise the entire set. There are seven logic instructions, five program control, two output and two no operation. All operations are performed at the bit level. Looping control structure is used, where the program counter feeding the external memory that inputs instructions to the processor wraps around after reaching its highest value and repeats the program.

**The idea of this processor is not to require the use of any additional software support.** Designed primarily as an industrial controller, the device is oriented towards a simple, repetitive control function.

**Time invarient software is the important feature** of this processor. This means that the processor can effect a conditional jump without parallel loading the program counter with the jump address. Whole blocks of instructions can be either turned on or off. This leads to the looping control structure in which the same sequence of commands are encountered with certain blocks of code being selectively enabled or disabled. In conventional systems the execution time of the program varies with the state of the input signals.

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| MC14500B | 1-bit processor | $4.88 |
| MC14099 | 8-bit addressable latch | 2.22 |
| MC14599 | 8-bit read/write addressable latch with master reset | 2.81 |
| MC14512 | 8-channel data select | 0.98 |

**No prototyping hardware** is available for this circuit. The design cycle for implementing a working system is intended to be so short as not to require any additional hardware or software. Particular emphasis is made of the fact that this processor is much easier to use than 4, 8 or 16-bit models.

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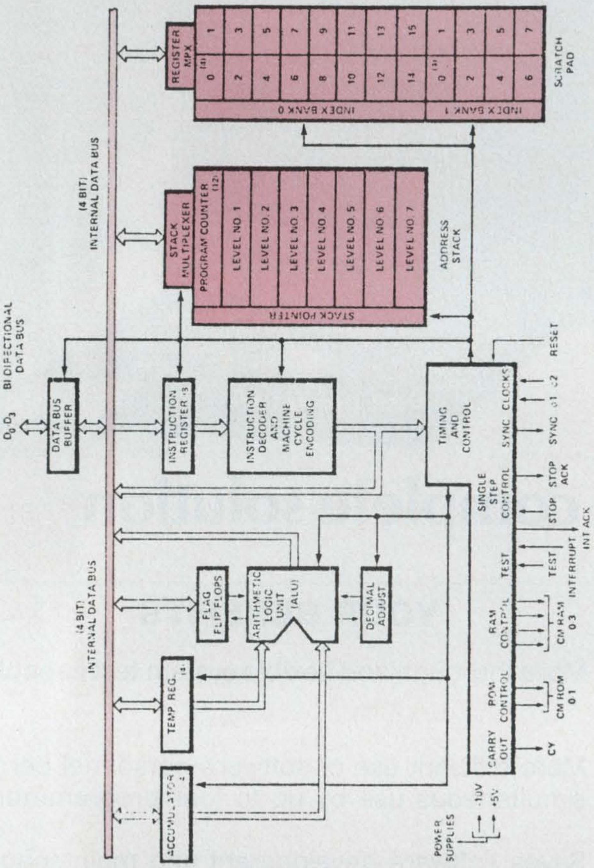
# 4-bit microprocessor, PMOS

## MCS-40 (4004 and 4040)

**Intel Corp.**
**3065 Bowers Ave.**
**Santa Clara, CA 95051**
**(408) 246-7501**

Alternate sources: National Semiconductor.

The MCS-40 microcomputer family includes the 4040 and 4004 central processing circuits and a comprehensive line of support chips. Both circuits are PMOS and are instruction compatible, but the 4040 is an enhanced device, with 14 more instructions than the 4004 for a total of 60 commands. Other differences between the CPUs include a larger address stack in the 4040 (seven levels instead of three), a larger scratchpad in the 4040 (24 instead of 16), and the 4040 also has interrupt and single-step capability.




The architecture of the MCS-40 processors is almost identical except for the expanded stack and scratchpad areas of the 4040 as compared to the 4004. A minimal system typically requires three chips—the CPU, a clock generator and a memory circuit.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | 12 bits |
| Direct addressing range: | 8192 words |
| Instruction word size: | 8 bits |
| Number of basic instructions: | 60 (4004: 46) |
| Shortest instruction/time (Add): | 10 $\mu$s |
| Longest instruction/time (Jump): | 20 $\mu$s |
| Clock frequency (min/max): | 0.5/0.75 MHz |
| Clock phases/voltage swing: | 2/15 V |
| Dedicated I/O control lines: | 8 |
| Package: | 24-pin DIP (4004: 16-pin DIP) |
| Power requirements: | 15 V/40 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| 4004 | 4-bit CPU | $5.00 |
| 4040 | Enhanced 4-bit CPU | 5.50 |
| 4003 | 10-bit shift register | 2.75 |
| 4265 | Programmable general-purpose I/O | 3.85 |
| 4269 | Programmable kbd/disp. | 7.75 |
| 4201A | Clock generator | 3.25 |
| 4008/9 | Memory interface ckts. | 6.50 ea |
| 4289 | Standard memory interface | 8.20 |
| 4002 | 320-bit RAM & 4 I/O lines | 4.45 |
| 4001 | 256 × 8 ROM & I/O | 10.00 |
| 4308 | 1024 × 8 ROM & I/O | 8.50 |
| 4316 | 2048 × 8 ROM | 16.90 |
| 4702A | 256 × 8 EPROM | 11.70 |

### Comments

**The instruction set** of 60 commands for the 4040 and 46 instructions for the 4004 are compatible—all 4004 instructions can run on the 4040. Instructions are broken into three groups—basic operations, machine-only instructions, and I/O and RAM commands.

**Software support** for the MCS-40 family consists of the MAC40 cross assembler and a 4004/4040 cross simulator (Interp/40) that are available on time-sharing systems and for in-house computer systems. There is also a program library containing over 50 programs.

**Important software features** include the BCD adjust instruction for decimal arithmetic and a register bank switch command for data save operations.

**Hardware support** for the MCS-40 family consists of the Intellec 4/Mod 40 hardware and software development system, with PROM resident monitor and peripheral interfaces. Also available are RAM memory boards and a designers kit.

# 4-bit, one-chip micro-computers

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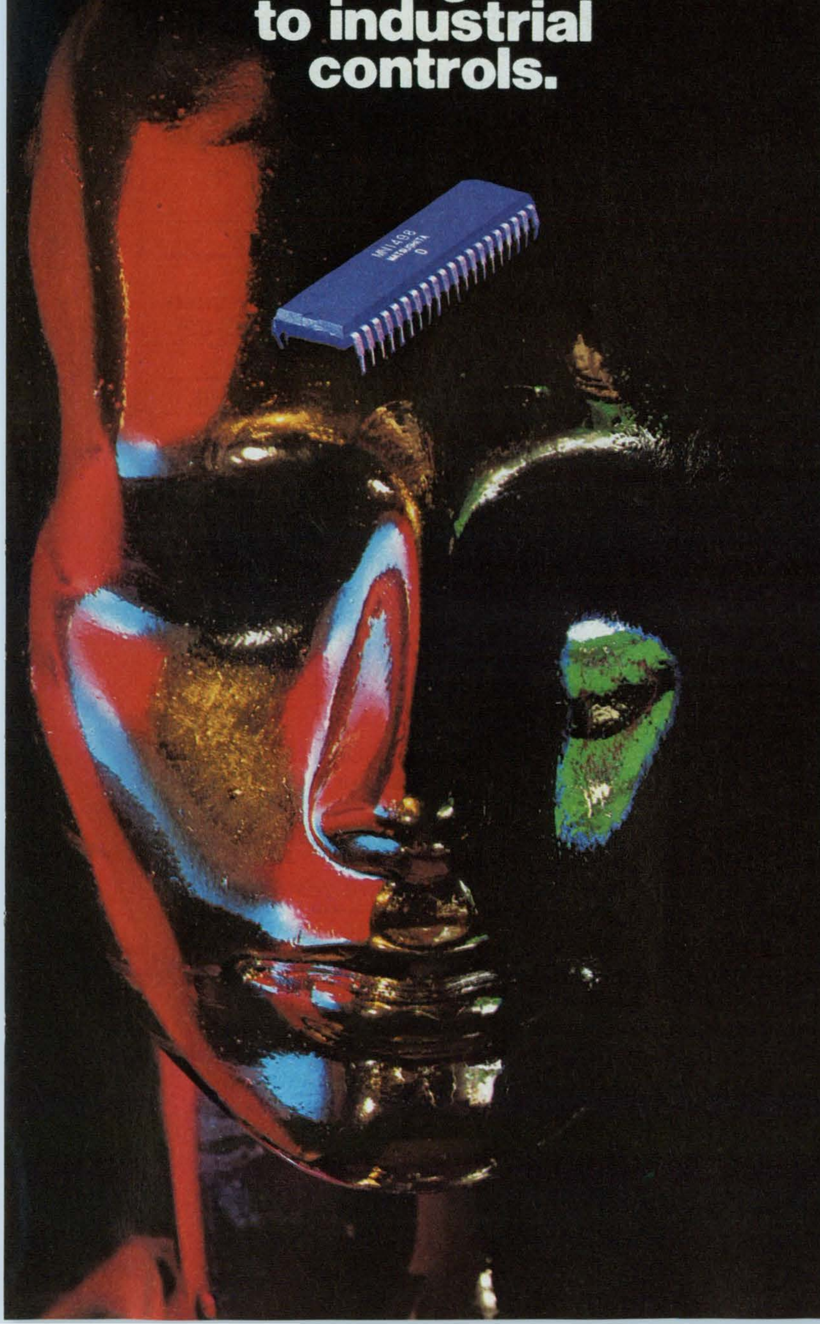
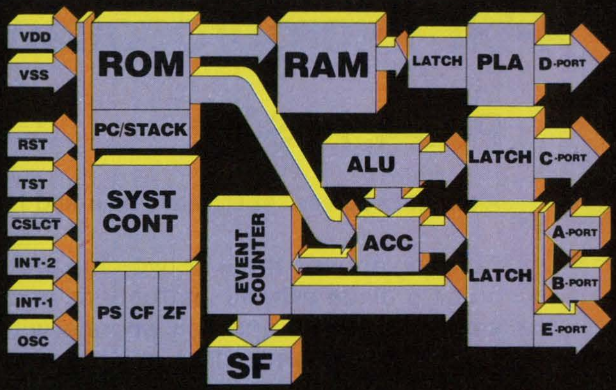


### Block diagram of MN1400 with on-chip, 1024x8-bit ROM.

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| Package | | MN1400 40-Pin Plastic DIP | MN1402 28-Pin Plastic DIP | MN1498 40-Pin Plastic DIP | MN1499 64-Pin Ceramic DIP |
|---|---|---|---|---|---|
| Power Supply | | +5V | +5V | +5V | +5V |
| Instruction Cycle Time | | 10μs | 10μs | 10μs | 10μs |
| Instruction Set | | 75 | 57 | 68 | 75 |
| Instruction Memory | Instruction ROM | Internal 1024 x 8 bits (8192 bits) | Internal 768 x 8 bits (6144 bits) | External 1024 x 8 bits (8192 bits) | External 2048 x 8 bits (16384 bits) |
| Total on Chip RAM | | 64 x 4 bits (256 bits) | 32 x 4 bits (128 bits) | 64 x 4 bits (256 bits) | 64 x 4 bits (256 bits) |

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CIRCLE NUMBER 58

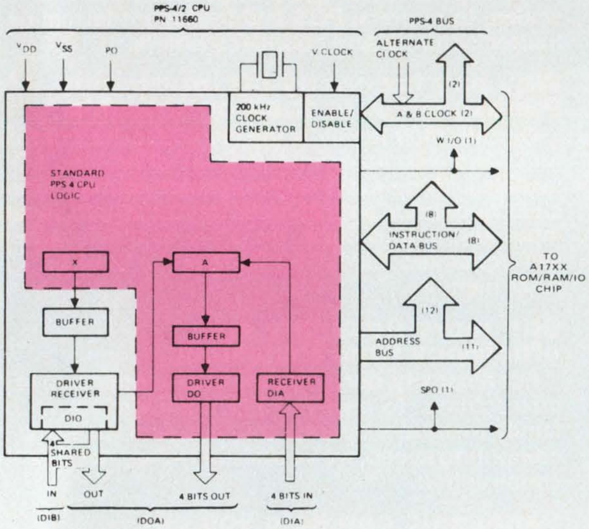
# 4-bit microprocessor, PMOS

## PPS-4, PPS-4/2

Rockwell International Microelectronic Devices
P.O. Box 3669
Anaheim, CA 92803
(714) 632-3729

Alternate sources: AEG Telefunken and National Semi.

Forming either a three or two-chip processor, the PPS-4 and PPS-4/2 central processor chips provide over 50 instructions and 12 dedicated I/O lines. The 4/2 CPU is a newer version of the 4 and can operate with an inexpensive 3.58 MHz crystal. The PPS-4 requires an external clock. Both processors, though, are totally instruction compatible and have 8-bit instruction/data buses and 11-bit address buses. The one major difference is that the PPS-4/2 CPU automatically floats all output lines when power is turned on; the PPS-4 doesn't. And, the 4/2 can directly drive low-power LED display segments.




The straightforward architecture of the PPS-4 and 4/2 revolves around the 4-bit accumulator and the three four-bit I/O buses. All lines are designed for direct MOS-level interfaces so to connect to other logic families buffer circuits must be used. The PPS-4 requires an external clock while the 4/2 just needs an external crystal.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | 12 bits |
| Direct addressing range: | 4096 words |
| Instruction word size: | 8 bits |
| Number of basic instructions: | 50 |
| Shortest instruction/time (Transfer): | 5 μs |
| Longest instruction/time (Load B long): | 10 μs |
| Clock frequency (min/max): | 199 kHz |
| Clock phases/voltage swing: | 4/12 V (PPS-4); Internal (PPS-4/2) |
| Dedicated I/O control lines: | 12 |
| Package: | 42-pin QUIL |
| Power requirements: | 17 V/26 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| PPS-4 | CPU | $18.15* |
| PPS-4/2 | CPU | 10.00* |
| 10706 | Clock generator | 7.45 |
| 10738 | Bus interface | 4.50 |
| 11049 | Interval timer | 8.50 |
| 10696 | General purpose I/O | 8.50 |
| 10930 | Serial data controller | 15.00 |

*Price as of Oct. 1. Peripheral chip prices were also cut on Oct. 1. Consult distributors for current cost.

### Comments

**The instruction set** contains a total of 50 commands that can be grouped as follows: 10 arithmetic and logic, 24 data transfer, six transfer, five skip, four I/O and one special address generation instruction.

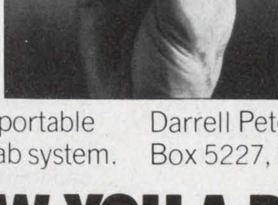
**Software support** for the PPS-4 and 4/2 includes a Fortran IV simulator and cross assembler for use on in-house computer systems and time-share networks as well as resident assemblers, supervisors, text editors and debug routines for use on the PPS MP Universal Assemulator hardware and software development system.

**Special features** of the software include the capability to perform an automatic memory address modification in addition to the basic data transfer instruction, and software controllable interrupts.

**Hardware support** for the PPS-4 and 4/2 starts with simple CPU modules designed to plug into the PPS MP Universal Assemulator. Other modules available as plug-ins include memory boards, I/O boards and prototyping modules.


Honeywell
101





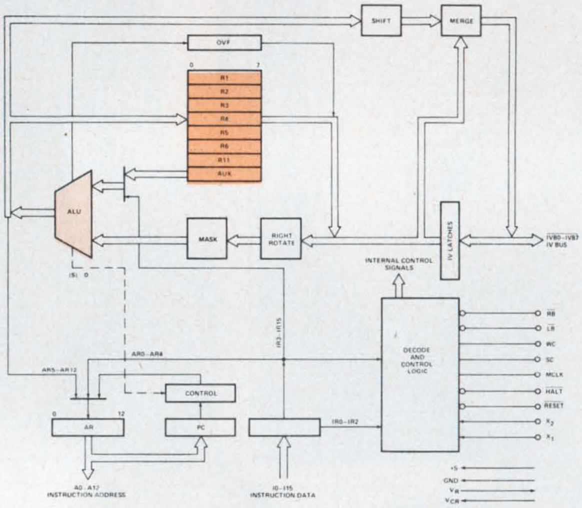
# 8-bit microcontroller, bipolar (STTL)

## 8X300

Signetics
811 E. Arques Ave.
Sunnyvale, CA 94086
(408) 735-8055

Alternate sources: None.

Featuring control-oriented instructions, the 8X300 is a fixed instruction microcontroller. Each of the eight 16-bit control instructions can be executed in 250 ns. The single-chip device handles 8-bit data and can execute data formats of one to eight bits at equal speed. Processor timing can be set via an external crystal or clock source.




The architecture of the 8X300 is designed so that several operations can take place simultaneously—shift, merge, rotate and mask. A minimal system contains the 8X300, some memories and several 8-bit I/O ports. All lines are TTL compatible and the 8-bit interface bus has three-state capability.

### Comments

**The instruction set** contains only eight instructions—Move, Add, AND, XOR, Execute, Nonzero transfer, Transmit and Jump. Input data can be rotated and masked while output data are shifted and merged—all within a 250 ns cycle time.

**Software support** for the 8X300 consists of a cross assembler. There is no program library available.

**Unusual software features** include the simplicity of operation and the identical 250 ns execution speed for each instruction. The circuit uses addressed I/O so the instructions can address up to 512 8-bit I/O ports directly from data bus.

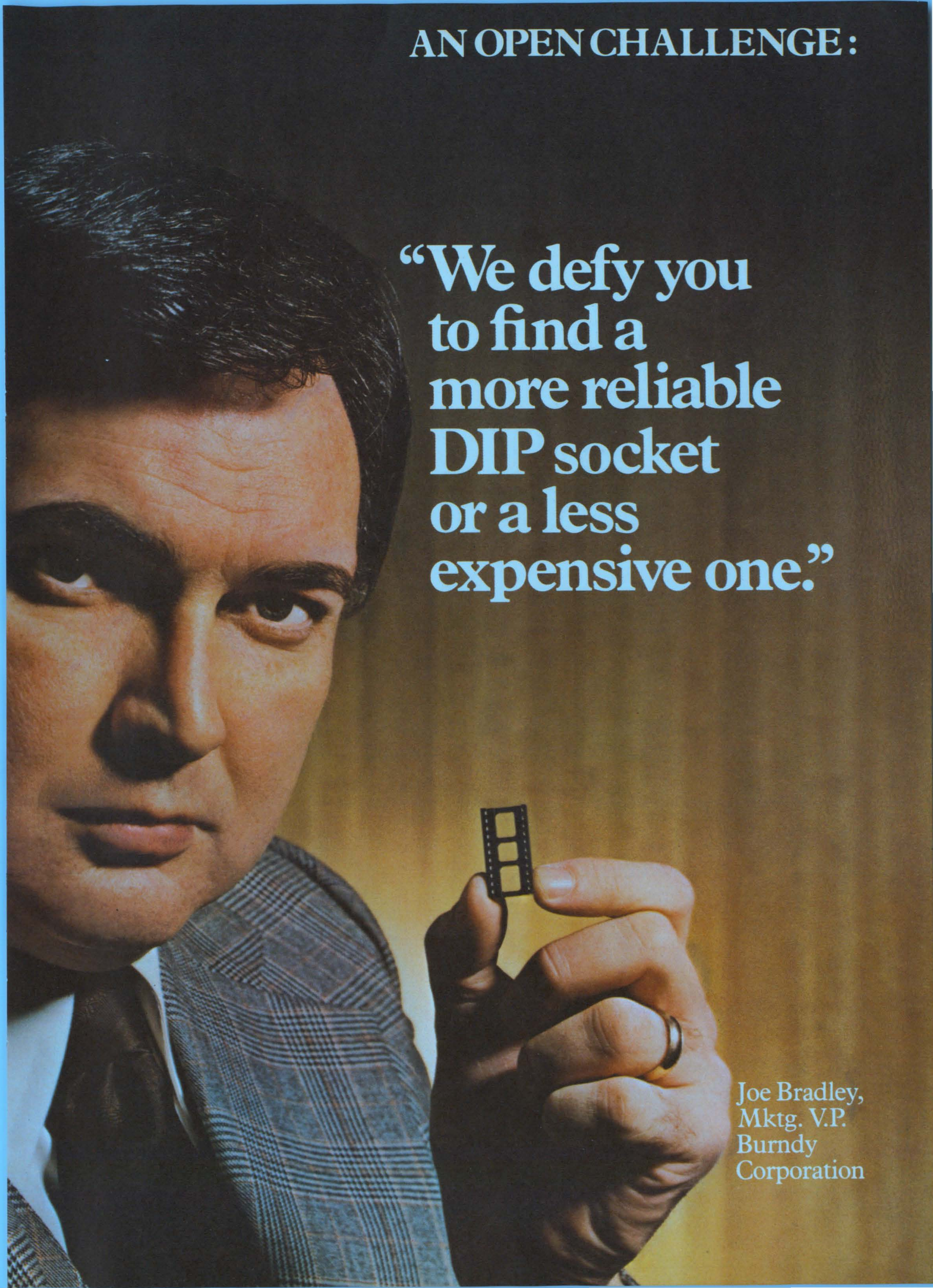
### Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | 13 bits |
| Direct addressing range: | 8192 words |
| Instruction word size: | 16 bits |
| Number of basic instructions: | 8 |
| Shortest instruction/time (All instructions): | 250 ns |
| Clock frequency (min/max): | Dc/4 MHz |
| Clock phases/voltage swing: | Internal or external TTL |
| Dedicated I/O control lines: | 8 |
| Package: | 50-pin DIP |
| Power requirements: | 5 V/450 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| 8X300 | 8-bit microcontroller | $48.75 |
| 8T32 | 8-bit programmable I/O port | 3.50 |
| 8T33 | 8-bit programmable I/O port | 3.50 |
| 8T35 | 8-bit programmable I/O port | 3.50 |
| 8T36 | 8-bit programmable I/O port | 3.50 |
| 8T39 | Bus extender | 5.40 |

**Hardware support** consists of the 8X300KT100SK, a designers kit and McSim, a development system produced by Scientific Microsystems, Mountain View, CA. McSim has an in-circuit emulation capability.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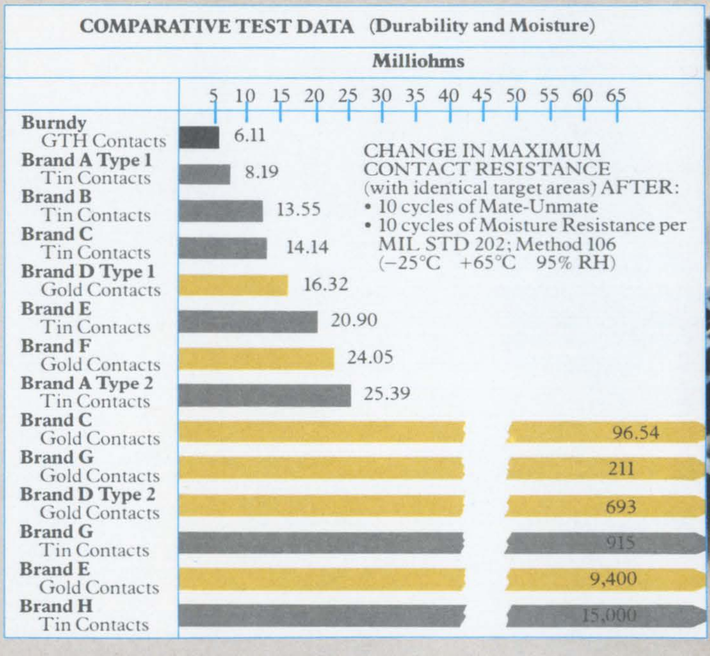
| TEST PERFORMED | MIN. | MAX. | AVG. |
|---|---|---|---|
| **GROUP 1** Mating Force (lbs./contact) | 0.600 | 0.730 | 0.643 |
| Contact Withdrawal Force (oz. w/.008" blade) | 2.500 | 8.100 | 4.940 |
| Insulation Resistance (600 VAC for 1 min.) | $2x10^6$ | $2x10^6$ | $2x10^6$ |
| Contact Resistance | 2.950 | 5.860 | 4.650 |
| **GROUP 2** Vibr. & Mech. Shock | 5.050 | 5.930 | 5.420 |
| Durability (50 cycles) | 5.050 | 6.750 | 5.520 |
| **GROUP 3** Insulation Resistance (5,000 megohms min.) | $>2x10^6$ | $>2x10^6$ | $>2x10^6$ |
| Ins. Res. after Moist. Res. (5,000 megohms min.) | $>2x10^6$ | $>2x10^6$ | $>2x10^6$ |
| **GROUP 4** Contact Resistance | 5.200 | 6.350 | 5.545 |
| after Corrosive Atmos. | 4.850 | 6.350 | 5.519 |

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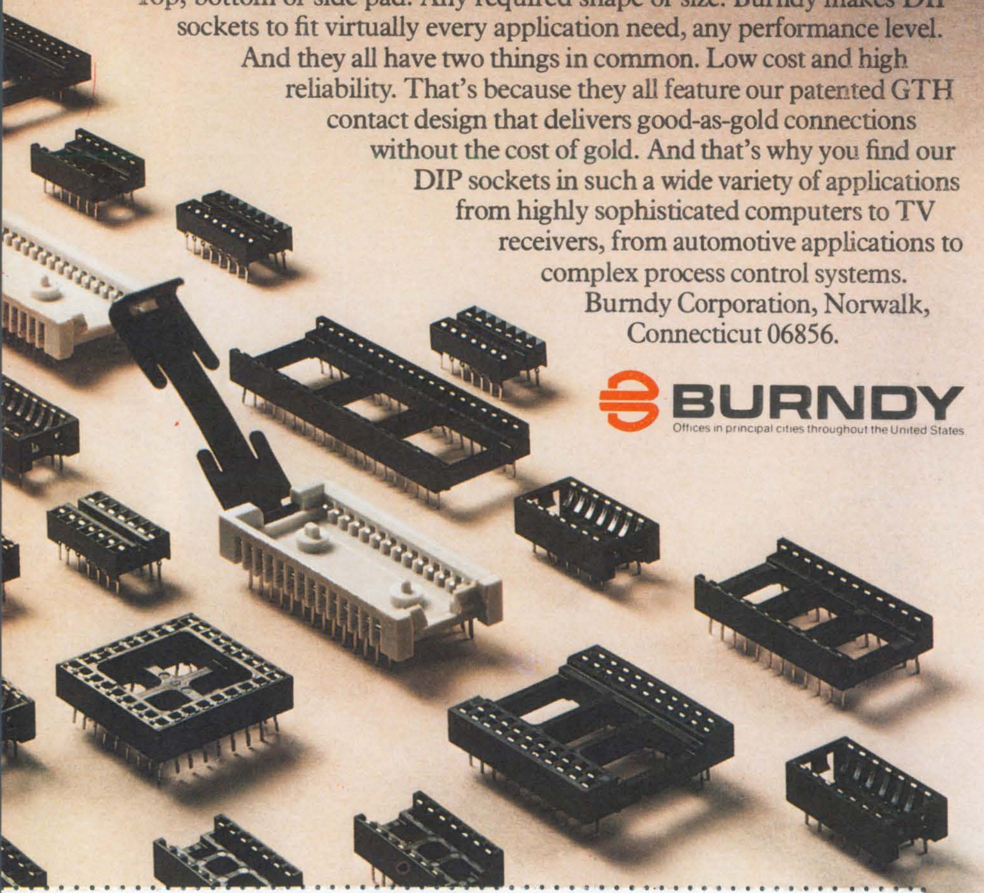

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Cramer Electronics, 214-661-9300
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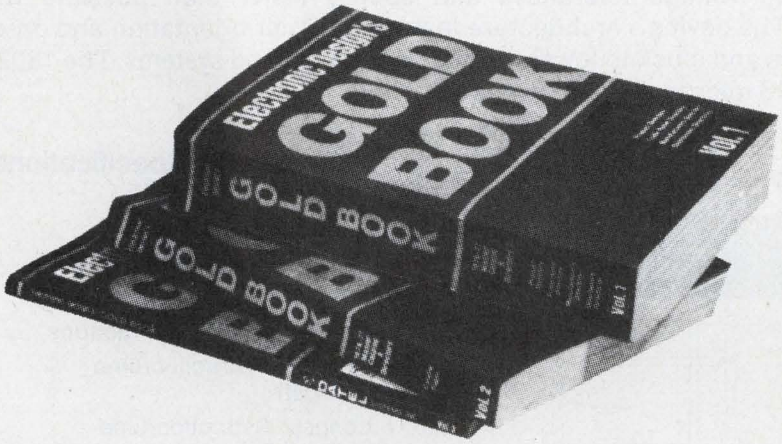


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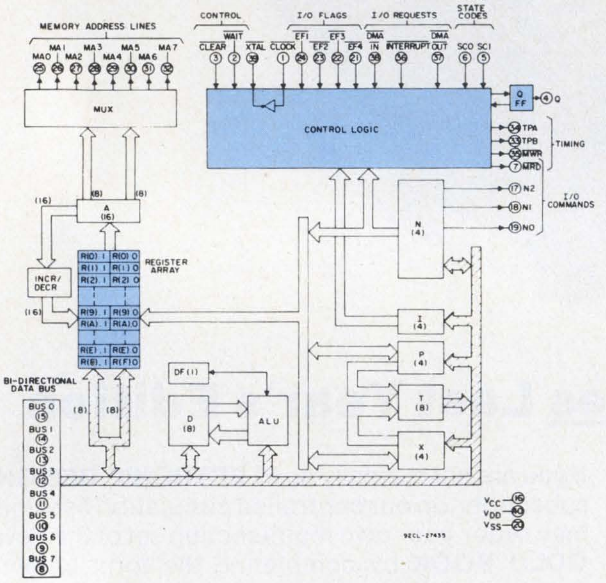
# 8-bit microprocessor, CMOS

## CDP 1802

**RCA Solid State Division**
**Box 3200**
**Somerville, NJ 08876**
**(201) 685-6731**

Alternate sources: Hughes Solid State Products, Solid State Scientific Inc.

Fabricated using CMOS technology, the 1802 offers static operation, high noise immunity, wide voltage tolerances and speeds faster than possible with NMOS construction. The device's architecture features register orientation and on-chip direct memory access and clock to lower the cost of memory and systems. The 1802 is still the only 8-bit CMOS microprocessor available.




The architecture of the 1802 revolves around the 16 x 16 bit register file that is used to simplify addressing and memory reference commands. Because of the on-chip register file and the built-in clock, a minimal system can be built around the processor and a single ROM.

## Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | 16 bits |
| Direct addressing range: | 65,536 words |
| Instruction word size: | 1 to 3 bytes |
| Number of basic instructions | 91 |
| Shortest instruction/time (Most): | 2.5 $\mu$s |
| Longest instruction/time (Long Branch): | 3.75 $\mu$s |
| Clock frequency (min/max): | Dc/6.4 MHz |
| Clock phases/voltage swing: | 1/supply voltage |
| Dedicated I/O control lines: | 9 |
| Package: | 40-pin DIP |
| Power requirements: | 4 to 12 V/1.6 mA (5 V) |

## Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| 1802 | Commercial CPU | $15.90 |
| | Industrial CPU | 19.50 |
| 1852 | 8-bit I/O port | 6.50 |
| 1853 | N-bit decoder | |
| 1854 | UART | 10.55 |
| 1856/57 | Memory & I/O bus Buffers/separators | 4.25 |
| 1858/59 | Memory latches decoders | 4.45 |
| 1861 | TV interface | N/A |

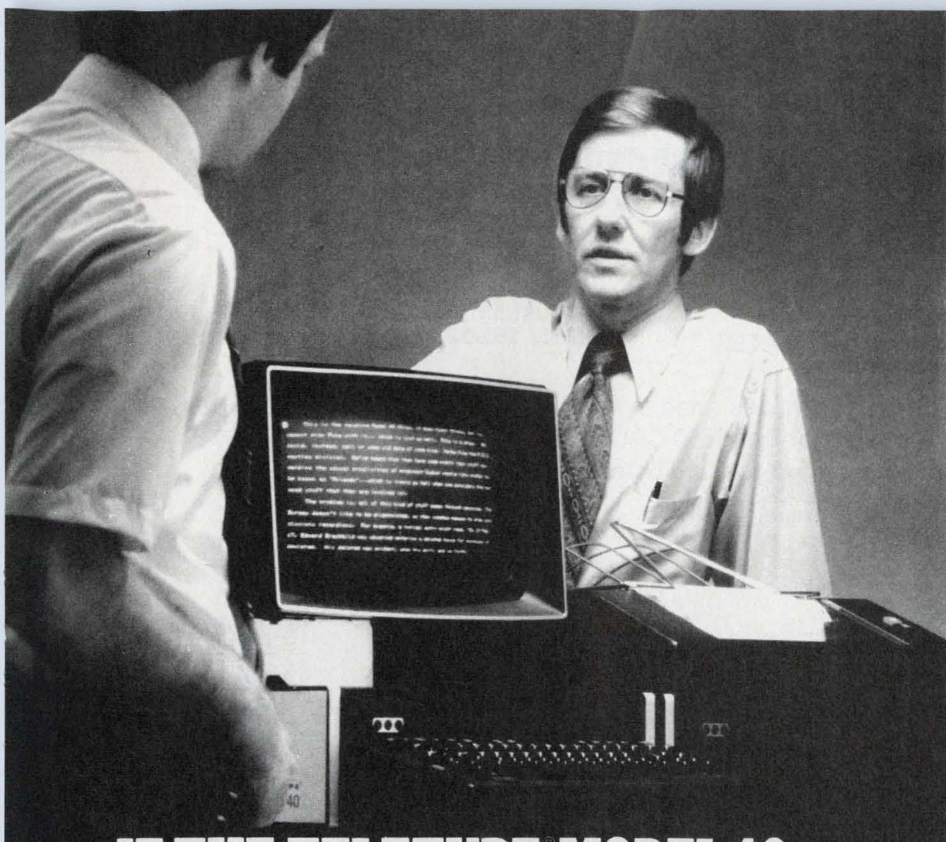
## Comments

**The 91 basic instructions** include 10 for control, seven for memory reference, seven for register operation, 12 for logic operations, 12 for arithmetic operations, 20 short branch instructions, eight long branch instructions, nine skip instructions, and 14 I/O instructions. On-chip program storage includes a 16 × 16-bit scratchpad RAM.

**Software support** includes arithmetic, resident editor and assembler, cross assembler/simulator, and firmware debug packages as well as a full floppy-disc based program development system. Also available is a high-level interpretive language.

**Features of the software** include simple 1, 2, or 3-byte instructions and simple timing loops for debugging. There is also a wide variety of branch and skip instructions from which to choose to permit rapid selection of a subroutine or program jump. A programmable serial port is also included on the chip to permit simple serial I/O without any specialized communications circuits.

**Hardware support** includes the Microtutor II learning tool, the COSMAC Development System for software development, and an evaluation kit for prototyping and breadboarding.



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For starters, we gave the model 40 product line its own diagnostic capability. To tell you quickly what's wrong. Then, to make it easy to fix, we used a modular design concept. The result is an average mean-time-to-repair of only 3/4 hour.

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The way we look at it, building something the best way humanly possible is only half our job. The other half is being ready for the unexpected.

For more information about the Teletype model 40 product line, write: Teletype, 5555 Touhy Ave., Skokie, IL 60076. Or call: 312/982-2000.

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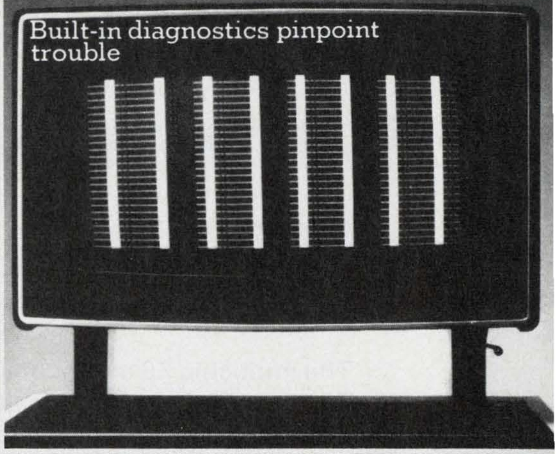
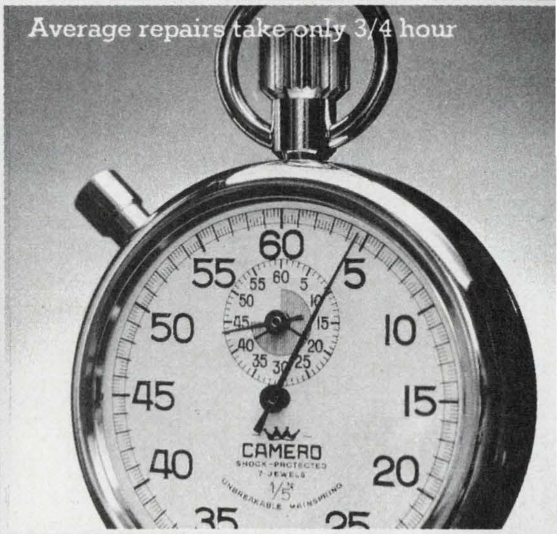
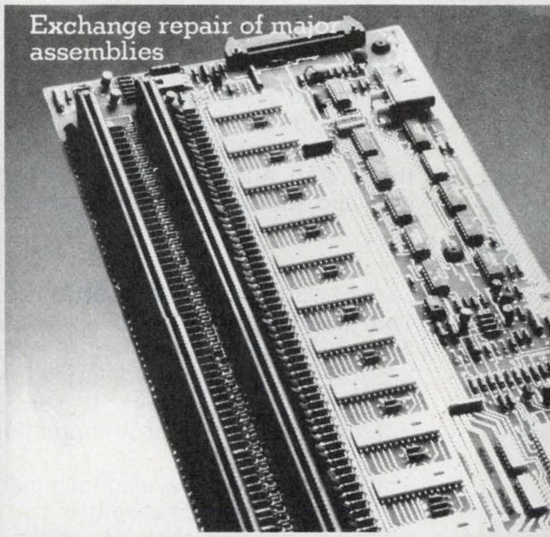


Built-in diagnostics pinpoint trouble

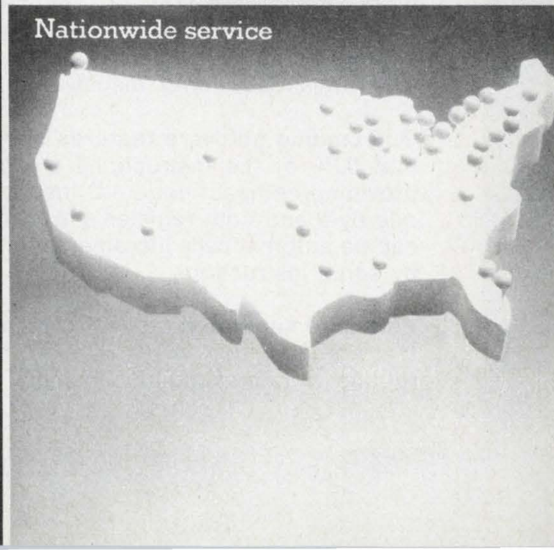


Average repairs take only 3/4 hour





Exchange repair of major assemblies



Nationwide service

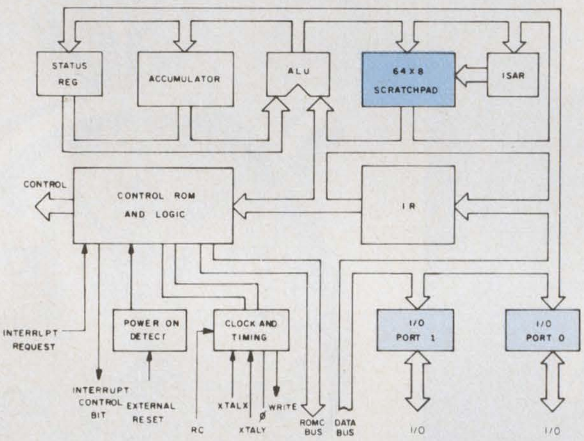
# 8-bit microprocessor, NMOS

## 3850

**Fairchild Semiconductor**
**464 Ellis St.**
**Mountain View, CA 94042**
**(415) 962-3816**

Alternate sources: Mostek, Motorola and SGS-ATES.

The multichip F8 microcomputer family is designed to handle I/O intensive applications. The minimal system typically consists of the 3850 CPU and one or more 3851, 56 or 57 program storage units, which can hold up to 2048 bytes of instructions and provide I/O lines and a programmable timer.




The architecture of the 3850 CPU provides a distributed format, thus permitting simple system expansions. The processor contains a 64 byte scratchpad RAM and 16 I/O lines. Any program storage unit added to the system brings 16 I/O lines, a counter/timer and other features depending on the version. All I/O lines are TTL compatible and the data and address buses have three-state capability.

### Comments

**The instruction set** contains a total of 76 basic instructions split as follows: 15 accumulator reference, eight memory reference, 12 branch and jump, 13 address modification, 15 scratchpad register reference and 13 control instructions.

**Software support** is available in many forms; there is a Fortran IV cross assembler that can run on 16-bit minicomputers, there are editor, assembler and debugger routines in the resident development system and ROM based programs, such as Fairbug, which has load, dump, display and store features.

**Outstanding software features** start with the fact that 60% of the instructions are one byte, thus providing compact code. I/O instructions are only one byte and both register and memory locations can be automatically incremented or decremented by some instructions.

**Hardware support** starts with the F8 evaluation kit that contains 1024 bytes of RAM, a TTY monitor routine with breakpoint capability and a Fortran cross assembler. Other hardware includes the SDB-50/70 software development board that has, in ROM, an editor, assembler and debugger. For in-circuit emulation the AIM-S1 system provides complete real-time device emulation.

### Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | 16 bits |
| Direct addressing range: | 65,536 bytes |
| Instruction word size: | 1 to 3 bytes |
| Number of basic instructions: | 76 |
| Shortest instruction/time (Add from scratchpad): | 2 $\mu$s |
| Longest instruction/time (Call to subroutine): | 13 $\mu$s |
| Clock frequency (min/max): | 0.1/2 MHz |
| Clock phases/voltage swing: | Internal |
| Dedicated I/O control lines: | 16 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/80 mA |
| | 12 V/25 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| F3850 | CPU, Commercial | $9.95 |
| F3850 | CPU, Industrial | 12.95 |
| F3850 | CPU, Military | 40.00 |
| F3851 | 1 k ROM, I/O & timer | 9.95 |
| F3852 | Dynamic memory interface | 7.45 |
| F3853 | Static memory interface, I/O and timer | 7.45 |
| F3854 | Direct memory interface | 5.95 |
| F3856 | 2 k version 3851 | 14.95 |
| F3857 | 2 k ROM plus F3851 | 14.95 |
| F3861 | Peripheral I/O with timer | 6.45 |
| F3871 | Same as 3861 but also does pulse width measurement | 9.50 |

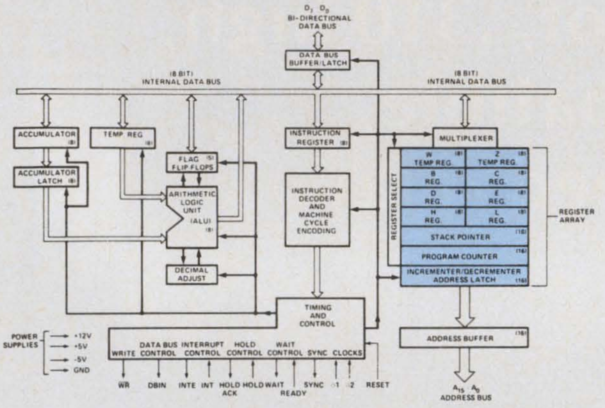
# 8-bit microprocessor, NMOS

## MCS-80 (8080A)

**Intel Corp.**
**3065 Bowers Ave.**
**Santa Clara, CA 95051**
**(408) 246-7501**

Alternate sources: Advanced Micro Devices, Mitsubishi, National Semiconductor, NEC Microcomputers, Siemens, Signetics (Philips) and Texas Instruments.

The 8080A is an 8-bit parallel processor designed for use in general-purpose computing applications. Fabricated with silicon-gate NMOS technology, the 8080A contains six general-purpose 8-bit registers, and 8-bit accumulator, four testable flag bits, an 8-bit parallel-processing arithmetic and logic unit, a 16-bit stack pointer and a 16-bit program counter. The processor can handle vectored interrupts and can directly address up to 512 I/O ports. Arithmetic and logic instructions can set or reset four flags and a fifth flag is used for decimal arithmetic only.




The typical 8080A system consists of a processor, a clock, a bus controller, some memory and a memory decoder. Both the data and address buses are TTL compatible and have three-state capability. All but the clock lines are TTL-compatible.

### Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | 16 bits |
| Direct addressing range: | 65,536 words |
| Instruction word size: | 8 to 24 bits |
| Number of basic instructions: | 78 |
| Shortest instruction/time (Add reg. to accum.): | 2$\mu$s, typ. |
| Longest instruction/time (Swap H&L with top of stack): | 9$\mu$s, typ. |
| Clock frequency (min/max): | 0.5/3 MHz |
| Clock phases/voltage swing: | 2/9 V |
| Dedicated I/O control lines: | None |
| Package: | 40-pin DIP |
| Power requirements: | 12 V/40 mA |
| | 5 V/60 mA |
| | −5 V/10 $\mu$A |

### Comments

**The 8080A has 78 basic instructions** divided into five groups: Data transfer, Arithmetic, Logic, Branch and Stack, and I/O and Machine control. There are also four addressing modes—direct, indirect, register and immediate. The move, load and store instruction groups can transfer either 8 or 16 bit data words between memory, the six working registers and the accumulator.

**Software support** for the 8080A includes a relocating macroassembler, a text editor and PL/M—all available on the company's own development system. There is also a program library (Insite) available to Intel customers that contains well over 200 programs submitted by users.

**The basic software** of the 8080A is designed for rapid stack manipulation and flexible jumps from the main program to subroutines. The ability to increment or decrement memory locations, the six general-purpose registers or the accumulator as well as register pairs or the stack pointer provides simple program looping capability.

**Hardware support** is available in several forms—from the low cost SDK-80 prototyping kit to the larger Microprocessor Development Systems in the Intellec family. Also available is a large range of 8080A-based computer boards from general-purpose CPU boards to multichannel analog-input boards. The large prototyping and development system, the Intellec-MDS offers the most flexibility—the system comes with a CPU, 16 k of RAM, 2 k of ROM, and software and hardware interfaces for terminals, printers and other equipment.

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| 8080A | CPU (commercial) | $13.10 |
| 8080A | CPU (MIL level C) | 31.60 |
| 8205 | 1-of-8 decoder | 2.80 |
| 8212 | 8-bit latch/buffer | 2.90 |
| 8214 | Priority Interrupt controller | 4.65 |
| 8216 | 4-bit bidirectional bus driver | 2.75 |
| 8224 | Clock driver | |
| 8226 | Inverting version, 8216 | 2.75 |
| 8228 | Bus controller | |
| 8251 | USART | |
| 8253 | Counter/timer | 17.55 |
| 8255 | Parallel I/O | 7.40 |
| 8257 | DMA controller | |
| 8259 | Interrupt controller | 17.20 |
| 8279 | Keyboard/disp. control | 14.10 |

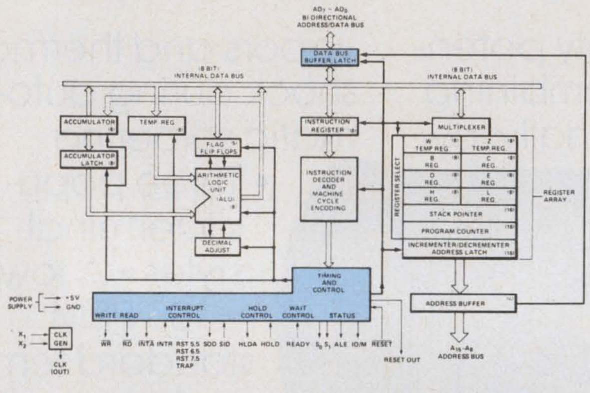
# 8-bit microprocessor, NMOS

## MCS-85 (8085)

Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 95051
(408) 246-7501

Alternate sources: Siemens, NEC and Advanced Micro Devices all by mask exchange.

The 8085 processor is a software-compatible upgrade of the 8080A processor. It offers two more instructions and has many of the peripheral circuits originally needed built right onto the same chip as the processor. With five levels of vectored interrupt, a serial I/O line and a clock speed of 3 MHz, the 8085 offers 8080A users a simple way to upgrade existing systems without loosing any software. And, since the clock is on chip, all signal lines are TTL compatible, with the address and data buses having three-state capability.




The basic architecture of the 8085 is the same as that of the 8080A. The only differences are the built-in clock generator, the built-in system control circuit and the multiplexed address/date bus structure to make available several pins for additional control.

## Comments

**The instruction set** of the 8085 contains all of the 8080A's instructions plus two more—RIM (read interrupt mask) and SIM (set interrupt mask)—for a total of 80 basic commands. The RIM and SIM instructions are used in conjunction with the interrupt capability built into the 8085 to provide four vectored interrupts, three of which are maskable.

**Available software support** for the 8085 includes all the existing 8080A software available through Insite—the company's user's software program library—and the many companies and private organizations that offer 8080A and 8085 software. An 8085 macroassembler can also be purchased, as well as PL/M when an MDS system with floppy disc is used.

**Special features** of the two new instructions permit the 8085 to handle serial inputs and outputs, and set up special masking bits to set or reset flags for the levels of vectored interrupts. Otherwise, all 8080A instructions can run on the 8085 without modification. The only adjustment that may have to be made is in any timing loops that use the 2 MHz clock frequency of the 8080A to compensate for the new 3 MHz clock.

**Hardware support** for the 8085 includes the ICE-85, an in-circuit emulator; the SDK-85 low-cost prototyping system; and the UPP 855 and EPROM programmer. Also, most of the development hardware available for the 8080A can be used to develop 8085 circuits and programs. The entire Intellec MDS microprocessor development system can be used, with just a few changes.

## Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | 16 bits* |
| Direct addressing range: | 65,536 bytes |
| Instruction word size: | 8 bits |
| Number of basic instructions: | 80 |
| Shortest instruction/time (Move data): | 1.3 μs |
| Longest instruction/time (Double add): | 5.2 μs |
| Clock frequency (min/max): | 0.5/3 MHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | None |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/170 mA |

* 8085 uses partially multiplexed address bus—eight lines are direct and eight are shared with the data bus.

## Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| P8085 | CPU (commercial temp) | $19.00 |
| D8085 | CPU (industrial temp) | 24.00 |
| P8155 | 256 byte RAM, I/O & timer | 18.00 |
| P8156 | Same as 8155 | 18.00 |
| P8355 | 2 kbyte ROM & 16 line I/O | consult factory |
| P8755-8 | 2 k UV EPROM & 16 line I/O | 125.00 |
| 8205 | 1 of 8 binary decoder | 2.80 |
| 8212 | 8-bit I/O port | 2.90 |
| 8214 | Priority interrupt | 4.65 |
| 8216 | Bidirectional bus driver | 2.75 |
| 8226 | Inverting version, 8216 | 2.75 |
| 8253 | Programmable timer | 17.55 |
| 8259 | Interrupt controller | 17.20 |
| 8279 | Kbd/display interface | 14.10 |

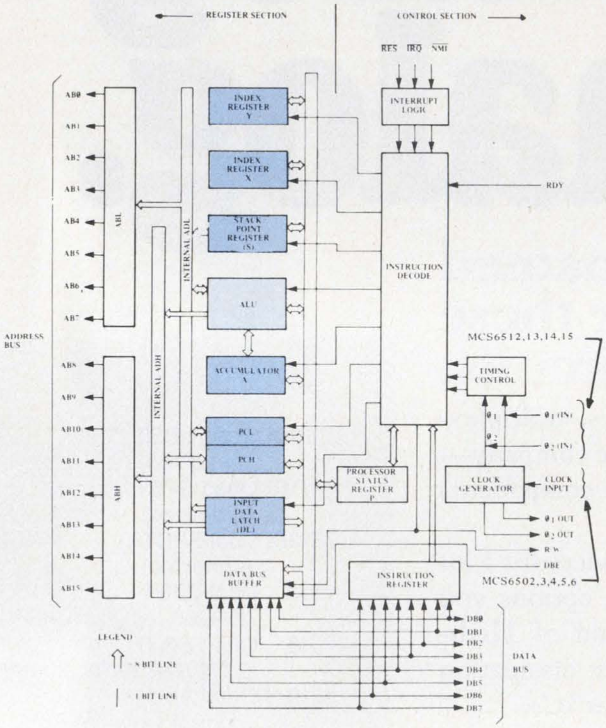
# 8-bit microprocessor, NMOS

## MCS 650X, 651X

**MOS Technology**
**950 Rittenhouse Rd.**
**Norristown, PA 19401**
**(215) 666-7950**

Alternate sources: Rockwell Microelectronic Devices and Synertek.

The 8-bit pipelined microprocessor is available in nine variants (10 from Rockwell). The 6502 family has an on-board one-phase clock while the 6512 family works with an external two-phase clock (for systems that need maximum timing control). Both families include models that can address 4, 8, and 65 kbytes (6502, 6515). Maximum operating frequencies are 1 MHz or 2 MHz (suffix A).




Note: 1. Clock Generator is not included on MCS6512,13,14,15
2. Addressing Capability and control options vary with each of the MCS6500 Products.

The architecture of the MCS6500 permits all registers to accept data from the data bus and transfer data back and forth since they are all connected to the same internal bus. A minimal system consists of the CPU and some memory (for a 651X system you also need a clock generator).

### Comments

**The instruction set** is memory-oriented with emphasis on convenient addressing of data in memory tables. The 56 instructions have the following addressing modes: accumulator immediate and absolute addressing, zero page indexed zero page, and indexed absolute addressing; implied and relative addressing; indexed indirect, indirect indexed, and absolute indirect addressing.

**Software support** includes a cross-assembler for PDP-8, 10, 11; a text editor, a debugger, a resident assembler, a math package, a Fortran compiler, a cross-emulator and Basic (cross and host).

**Outstanding software features** include: add and subtract in decimal mode with automatic correction, powerful addressing modes (indexed indirect and indirect indexed) and a Basic interpreter.

### Specifications

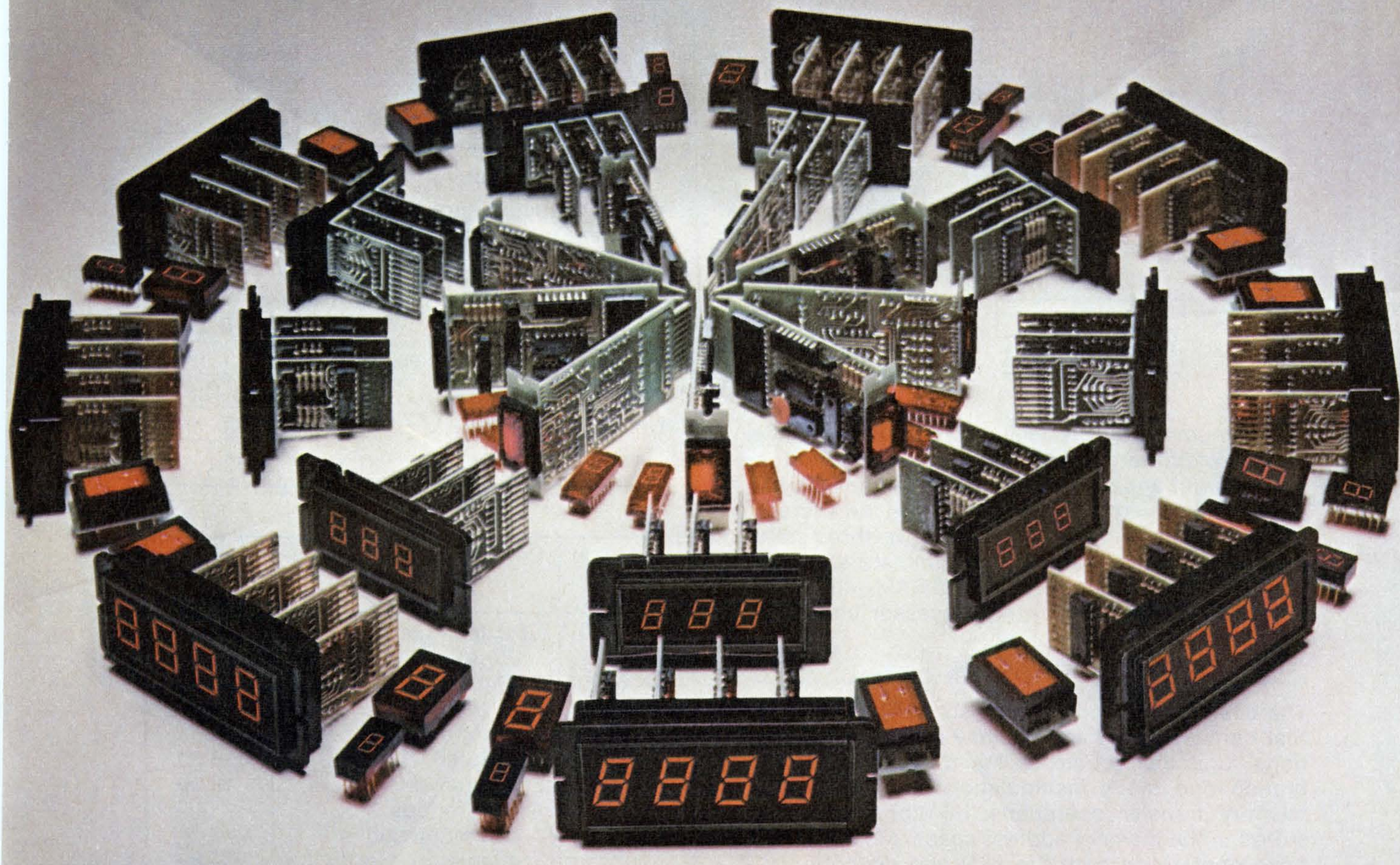
| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | 16 bits |
| Direct addressing range: | 65,536 bytes |
| Instruction word size: | 8 to 24 bits |
| Number of basic instructions: | 56 |
| Shortest instruction/time (Decrement register): | 1 μs |
| Longest instruction/time (Rotate memory): | 3 μs |
| Clock frequency (min/max): | 20 kHz/2 MHz |
| Clock phases/voltage swing: | 1/TTL or 2/5 V |
| Dedicated I/O control lines: | 3 |
| Package: | 28 or 40-pin DIP |
| Power requirements: | 5 V/140 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| 6502 | On-bd clock, 65 k, 40 pin μP | $10.90 |
| 6503 | On-bd clock, 4 k, 28 pin | 8.50 |
| 6504 | On-bd clock, 8 k, 28 pin | 8.50 |
| 6505 | On-bd clock, 4 k, 28 pin | 8.50 |
| 6506 | On-bd clock, 4 k, 28 pin | 8.50 |
| 6507 | Rockw, only, 8 k, 28 pin | 9.65 |
| 6512 | Ext. clock, 65 k, 40 pin | 10.90 |
| 6513 | Ext. clock, 4 k, 28 pin | 8.50 |
| 6514 | Ext. clock, 8 k, 28 pin | 8.50 |
| 6515 | Ext. clock, 4 k, 28 pin | 8.50 |
| 6520 | Peripheral interface adaptor (40-pin) | 6.55 |
| 6522 | 6520 plus 2 timers (16-bit) | 6.75 |
| 6530 | 16 I/O, 8 k ROM, 65 × 8 RAM, timer | 13.00 |
| 6532 | like 6530, but 128 × 8 static RAM | $12.75 |

**Hardware support** consists of the KIM-1 board (including a μP, hex keyboard, 6-digit display, 1 k × 8 RAM, 16 I/O lines and control program); KIM-2 (4 k RAM expansion); KIM-3 (8 k RAM expansion); KIM-4 (motherboard), TIM (a 6530 with monitor software for interfacing serial terminals). Also available is the MDT 650 development terminal.

# When you need LED readout displays or more than LED readout displays...



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CIRCLE NUMBER 65

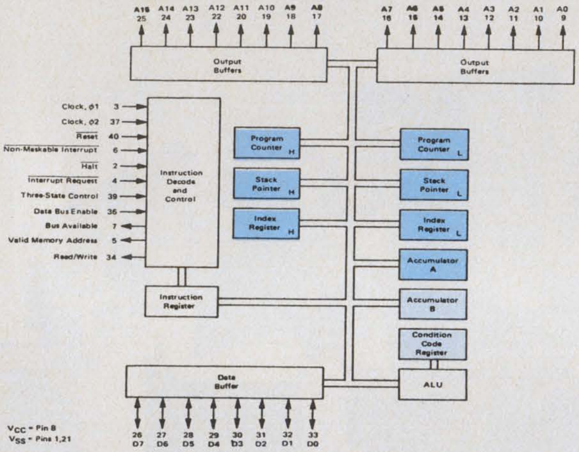
# 8-bit microprocessor, NMOS

## MC6800

Motorola, IC Div.
3501 Ed Bluestein Blvd.
Austin, TX 78721
(512) 928-2600

Alternate sources: American Microsystems, Fairchild, Fujitsu, Hitachi and Sescosem/Thomson CSF.

Designed as a general-purpose central processor, the MC6800 provides 8-bit computational capability with an instruction set of 72 commands. The processor has a bidirectional data bus, a full 16-bit address bus and can operate from a 5 V supply. There are three versions of the MC6800 available—the original MC6800 with a 1 MHz clock rate, the MC68A00 with a 1.5 MHz clock, and the MC68B00 with a 2 MHz clock. All versions are pin compatible.




A minimum system for the MC6800 will typically consist of the processor, some ROM and RAM, a clock circuit and some I/O circuits. All lines except the clock lines are TTL compatible and the address bus, data bus and R/W line also have three-state capability. The 6800 has two accumulators, but all stack space is in the user-supplied RAM—there are no auxiliary registers on the processor chip.

### Comments

**The basic instruction set** consists of 72 commands that contain binary and decimal arithmetic operations, logic instructions shift and rotate functions, branch and stack manipulation commands and memory transfer operations. I/O commands are stored in the memory address space. Most instructions operate on both the ALU and memory.

**The basic software support** includes an assembler, editor, macro-assembler, a disc-based operating system and several high-level languages—Basic and Fortran. The user program library contains more than 65 programs.

**Software features** include direct page memory addressing and relative branches that allow position independent code to be written. A read/modify/write instruction can be used to modify the contents of a memory location without bringing the contents into the accumulator.

**Hardware support** for the MC6800 comes in several forms. For the circuit designer there are several evaluation board systems available from Motorola and the alternate sources. And, for the program development engineer, the EXORciser system, consisting of a CPU board, a 2-k static RAM board, a 16-k dynamic RAM board, a baud-rate board, serial and parallel interfaces, a PROM programmer and a PROM/EPROM board can be used with the floppy-disc operating system. Also available is a user system evaluator (USE) that can help with the early prototyping efforts.

### Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | 16 bits |
| Direct addressing range: | 65,536 words |
| Instruction word size: | 8 bits |
| Number of basic instructions: | 72 |
| Shortest instruction/time (Load accumulator A): | 1 μs |
| Longest instruction/time (Software interrupt): | 6 μs |
| Clock frequency (min/max): | Dc/2 MHz |
| Clock phases/voltage swing: | 2/ Vcc− 0.6 to Vss+ 0.4 V |
| Dedicated I/O control lines: | 9 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/100 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| MC6800 | CPU (commercial), 25-up | $17.95 |
| MC6800 | CPU (industrial), 25-up | 49.00 |
| MC6800 | CPU (military), 25-up | 76.00 |
| MC6820 | Peripheral interface adapter | 6.60 |
| MC6840 | Programmable timer | 13.00 |
| MC6850 | Asynchronous communications adapter | 7.80 |
| MC6854 | Data link controller | 17.00 |
| MC6860 | 600 bps modem | 8.00 |
| MC6862 | 2400 bps demodulator | 13.15 |
| MC68488 | General purpose interface adapter | 14.00 |
| MC6843 | Floppy-disc controller, 25-up | 25.00 |
| MC6844 | DMA controller, 25-up | 23.50 |
| MC6845 | CRT controller, 25-up | 25.00 |

# How fast can you measure rise time, fall time and pulse width?


## Your way.

(About 5 minutes.)

**1.** Connect signal to scope. **2.** Adjust trace intensity. **3.** Adjust focus. **4.** Select VOLTS/DIV range. **5.** Select TIME/DIV range. **6.** Adjust vertical gain to fill screen for location of 10% & 90% points. **7.** Locate 10% point. **8.** Locate 90% point. **9.** Determine horizontal displacement between 10% & 90% points. **10.** Multiply displacement by horizontal scale factor.

That's RISE TIME. Only 9 more steps and you've got PULSE WIDTH and FALL TIME.

## Our way.

(About 5 seconds.)

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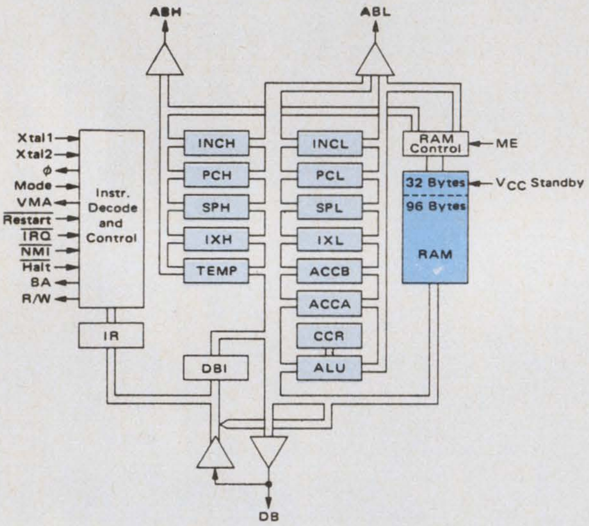
# 8-bit microprocessor, NMOS

## MC6802

Alternate sources: Fairchild and Hitachi.

**Motorola, Inc.**
**Integrated Circuit Div.**
**3501 Ed Bluestein Blvd.**
**Austin, TX 78721**
**(512) 928-2600**

A general-purpose central processor for the M6800 family, the MC6802 includes a crystal-controlled clock oscillator and 128 bytes of on-chip RAM, 32 bytes of which can be retained during power-off by using battery backup. Like the earlier MC6800, it operates from a 5-V supply, and has a bidirectional data bus, a 16-bit address bus and 72 instructions. Maximum clock rate is 4 MHz.




The architecture of the MC6802 resembles that of the MC6800 except that the 6802 includes the stack and the clock oscillator on the chip. A minimum system requires just two chips—the MC6802 MPU and the MC6846, a combination ROM and I/O timer.

### Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | 16 bits |
| Direct addressing range: | 65,536 words |
| Instruction word size: | 8, 16 or 24 bits |
| Number of basic instructions: | 72 |
| Shortest instruction/time (Load accumulator A): | 2 μs |
| Longest instruction/time (Software interrupt): | 12 μs |
| Clock frequency (min/max): | 1 MHz/4 MHz |
| Clock phases/voltage swing: | Internal |
| Dedicated I/O control lines: | 9 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| MC6802 | CPU (commercial), 25-up | $22.00 |
| MC6802 | CPU (industrial), 25-up | 45.00 |
| MC6846 | Combined ROM/timer | N/A |
| MC6820 | Peripheral interface adapter | 6.60 |
| MC6840 | Programmable timer | 13.00 |
| MC6850 | Asynchronous communications adapter | 7.80 |
| MC6854 | Data link controller | 17.00 |
| MC6860 | 600-bps modem | 8.00 |
| MC6862 | 2400-bps demodulator | 13.15 |
| MC68488 | General purpose interface adapter | 14.00 |
| MC6843 | Floppy-disc controller, 25-up | 25.00 |
| MC6844 | DMA controller, 25-up | 23.50 |
| MC6845 | CRT controller, 25-up | 25.00 |

### Comments

**The instruction set** contains 72 commands, including binary and decimal arithmetic operations, logic instructions, shift and rotate functions, branching commands and memory transfer operations. I/O commands are stored in the memory address space.

**Software support** offered includes an assembler, editor, macro assembler, a disc-based operating system and several high-level languages such as Basic and Fortran. The user program library contains over 65 programs.

**Software features** include direct page addressing of memory for shorter coding, and relative branches that allow position-independent coding. Read/modify/write instructions operate on memory without passing data through an accumulator.

**Hardware support** comes in several forms. Several evaluation-board systems are available from Motorola and other sources. A user system evaluator (USE) can aid prototyping. For program development, the EXORciser system can be used with a floppy-disc operating system. The EXORciser system includes a CPU board, a 2-k static RAM board, a 16-k dynamic RAM board, a baud-rate board, serial and parallel interfaces, a PROM programmer and a PROM/EPROM board.

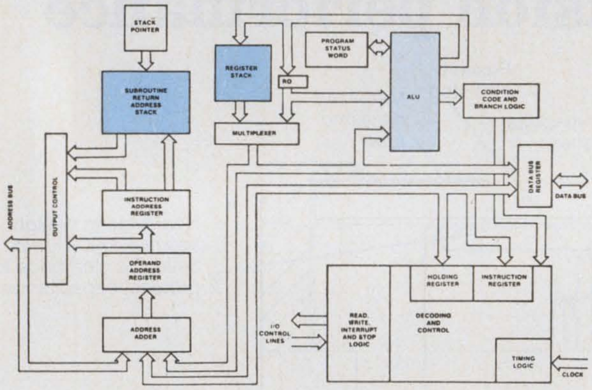
# 8-bit microprocessor, NMOS

## 2650

Alternate sources: Advanced Memory Systems and National Semiconductor.

**Signetics**
**811 East Arques Ave.**
**Sunnyvale, CA 94086**
**(408) 739-7700**

The 2650 family of microprocessors contains general-purpose devices that can address up to 32 kbytes of memory. There are several versions of the processor available—all pin and software compatible, but differing in clock speed. The 2650 has a maximum clock of 1.25 MHz, the 2650A a max of 1.5 MHz and the 2650A-1 a max of 2 MHz. Variable length instructions, seven general-purpose registers and three-state buses are among the processor's features.




The architecture of the 2650 is centered about the 8-bit ALU and a seven-word register stack. There is also another register stack on the chip to hold subroutine return addresses (it can hold up to eight 15-bit addresses). The 2650 has a single level of interrupt, requires a single-phase external clock and is TTL compatible on all lines.

## Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | 15 bits |
| Direct addressing range: | 32,768 bytes |
| Instruction word size: | 1 to 3 bytes |
| Number of basic instructions: | 75 |
| Shortest instruction/time (No operation): | 0.5 μs (A-1) |
| Longest instruction/time (Add absolute): | 2 μs (A-1) |
| Clock frequency (min/max): | Dc/2 MHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | 9 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/100 mA |

## Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| 2650 | 8-bit CPU, 1.25 MHz | N/A |
| 2650A | 8-bit CPU, 1.5 MHz | 13.50 |
| 2650A-1 | 8-bit CPU, 2 MHz | N/A |
| 2651 | Programmable communication interface | 13.70 |
| 2652 | Multiprotocol communications controller | 24.90 |
| 2655 | Programmable peripheral interface | 12.60 |
| 2656 | System memory interface | 19.70 |

## Comments

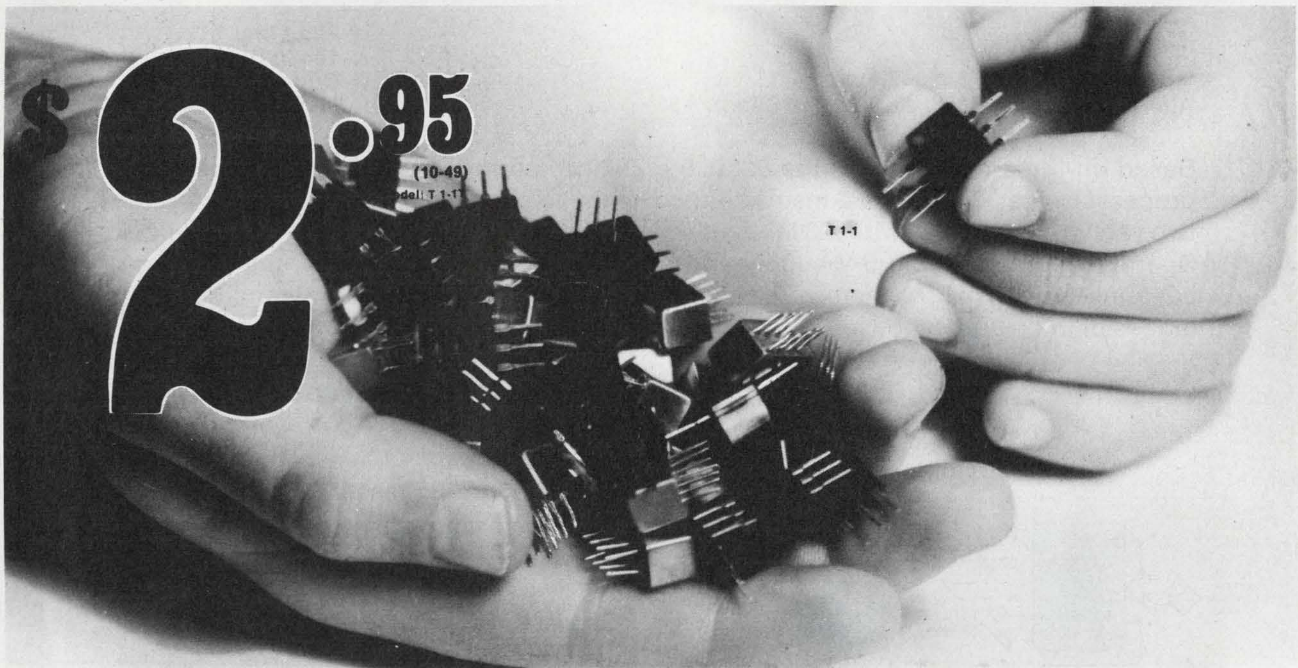
**The instruction set** for the 2650 family contains 75 commands, which are divided into 1, 2 and 3 bytes long operations. Instructions can be grouped as follows: 26 arithmetic and logic operations, 22 branch commands and another 26 that are I/O, program status and load/store instructions.

**Software support** for the 2650 processor family consists of a ROM-based editor and loader (PIPBUG) and several cross Fortran IV programs for assembly and simulation that run on 16 or 32 bit computers. There is also a high-level language, PLus, that permits PL-type programming.

**Strong points of the software set** include auto incrementing or decrementing of the index register for arithmetic indexed instructions, all of the branch commands except for indexed branching can be conditional and the I/O instructions are either one or two-byte commands.

**Hardware support** for the 2650 family consists of a prototyping kit, a pre-assembled processor card and the Twin, a dual-microprocessor hardware and software development system.

# RF TRANSFORMERS

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| Model | | | | | | |
|---|---|---|---|---|---|---|
| Metal Case | TMO 1-1 | TMO 1.5-1 | TMO 2.5-6 | TMO 4-6 | TMO 9-1 | TMO 16-1 |
| Plastic Case | T 1-1 | T 1.5-1 | T 2.5-6 | T 4-6 | T 9-1 | T 16-1 |
| Freq. Range, MHz | .15-400 | .1-300 | .01-100 | .02-200 | .15-200 | .3-120 |
| Impedance Ratio | 1 | 1.5 | 2.5 | 4 | 9 | 16 |
| Max. Insertion Loss | MHz | MHz | MHz | MHz | MHz | MHz |
| 3 dB | .15-400 | .1-300 | .01-100 | .02-200 | .15-200 | .3-120 |
| 2 dB | .35-200 | .2-150 | .02-50 | .05-150 | .3-150 | .7-80 |
| 1 dB | 2-50 | .5-80 | .05-20 | 1-100 | 2-40 | 5-20 |
| Price, Model TMO | $4.95 | $6.25 | $5.95 | $5.95 | $5.45 | $5.95 |
| (10-49) Model T | $2.95 | $3.95 | $3.95 | $3.95 | $3.45 | $3.95 |

**UNBALANCED PRIMARY & SECONDARY**

50 Ω / N×50 Ω

| Model | | | | | |
|---|---|---|---|---|---|
| Metal Case | TMO 2-1 | TMO 3-1 | TMO 4-2 | TMO 8-1 | TMO 14-1 |
| Plastic Case | T 2-1 | T 3-1 | T 4-2 | T 8-1 | T 14-1 |
| Freq. Range, MHz | .015-600 | .5-800 | .5-600 | .15-250 | .2-150 |
| Impedance Ratio | 2 | 3 | 4 | 8 | 14 |
| Max. Insertion Loss | MHz | MHz | MHz | MHz | MHz |
| 3 dB | .015-600 | .5-800 | .2-600 | .15-250 | .2-150 |
| 2 dB | .02-400 | 2-400 | .5-500 | .25-200 | .5-100 |
| 1 dB | .05-200 | | 2-250 | 2-100 | 2-50 |
| Price, Model TMO | $5.45 | $6.25 | $5.45 | $5.45 | $6.25 |
| (10-49) Model T | $3.45 | $4.25 | $3.45 | $3.45 | $4.25 |

**DC ISOLATED PRIMARY & SECONDARY CENTER-TAP SECONDARY**

N×50 Ω / 50 Ω

| Model | | | | | | | |
|---|---|---|---|---|---|---|---|
| Metal Case | TMO 1-1T | TMO 2-1T | TMO 2.5-6T | TMO 3-1T | TMO 4-1 | TMO5-1T | TMO 13-1T |
| Plastic Case | T 1-1T | T 2-1T | T 2.5-6T | T 3-1T | T 4-1 | T 5-1T | T 13-1T |
| Freq. Range, MHz | .05-200 | .07-200 | .01-100 | .05-250 | .2-350 | .3-300 | .3-120 |
| Impedance Ratio | 1 | 2 | 2.5 | 3 | 4 | 5 | 13 |
| Max. Insertion Loss | MHz | MHz | MHz | MHz | MHz | MHz | MHz |
| 3 dB | .05-200 | .07-200 | .01-100 | .05-250 | .2-350 | .3-300 | .3-120 |
| 2 dB | .08-150 | .1-100 | .02-50 | .1-200 | .35-300 | .6-200 | .7-80 |
| 1 dB | .2-80 | .5-50 | .05-20 | .5-70 | 2-100 | 5-100 | 5-20 |
| Maximum Amplitude Unbalance MHz | | | | | | | |
| .1 dB | .5-80 | 1-50 | .1-20 | 1-70 | 5-100 | 10-100 | 5-20 |
| .5 dB | .05-200 | .07-200 | .01-100 | .05-250 | .2-350 | .3-300 | .3-120 |
| Maximum Phase Unbalance Degrees MHz | | | | | | | |
| 1° | .5-80 | 1-50 | .1-20 | 1-70 | 5-100 | 10-100 | 5-20 |
| 5° | .05-200 | .07-200 | .01-100 | .05-250 | .2-350 | .3-300 | .3-120 |
| Price (10-49) | | | | | | | |
| Model TMO | $5.95 | $6.25 | $6.25 | $5.95 | $4.95 | $6.25 | $6.25 |
| Model T | $3.95 | $4.25 | $4.25 | $3.95 | $2.95 | $4.25 | $4.25 |

| | TMO-series | T-series |
|---|---|---|
| Primary Impedance: 50 ohms | .25 cu. inches | .02 cu. inches |
| Total Input Power: ¼ watt | .07 ounces | .01 ounces |

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CIRCLE NUMBER 68

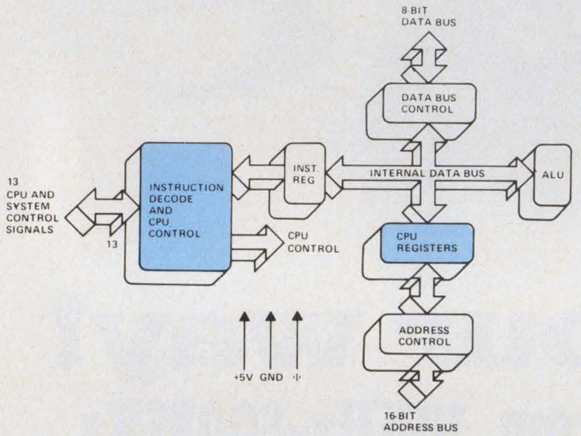
# 8-bit microprocessor, NMOS

## Z80-CPU

Zilog Inc.
10460 Bubb Rd.
Cupertino, CA 95014
(408) 446-4666

Alternate sources: Mostek, NEC and Sharp.

Based on the architecture of the 8080, the Z80 can perform the 78 instructions of that processor plus 80 additional instructions. The ion-implanted NMOS device is offered in two versions — the Z80 with 2.8 MHz maximum clock and the Z80A with a 4.5 MHz clock. Operating from a single 5-V supply and a single-phase external clock, the processor contains 17 internal registers and built-in dynamic RAM refresh circuitry and has three modes of interrupt response.




The architecture of the Z80 resembles that of the 8080A, except that there is a second bank of eight 8-bit registers that mirrors the eight registers in the 8080A. All timing generation is on the processor chip except the oscillator, and the Address bus is structured so that refresh addresses appear on the lower half of the bus to refresh dynamic RAMs. A minimal system consists of the processor, a clock source and some memory.

### Comments

**The instruction set of the Z80** contains all 78 op codes of the 8080A's instruction set as well as another 80 codes. Of the 158 total instructions, there are 21 8-bit Load commands, 20 16-bit Load commands, 14 Exchange, Block transfer and Search instructions, 17 Arithmetic and Logic commands for 8-bit operations, 11 instructions for 16-bit arithmetic and logic operations, 12 general-purpose arithmetic commands, 16 shift and rotate functions, nine Bit set, Reset and Test commands, 11 Jump instructions, seven Call/Return directives and 12 I/O operations.

**Software support** includes a macroassembler that can generate relocatable code, a linker that can link together program modules and generate a load module with absolute addresses, and several high-level languages—PL/M, PL/Z and Basic. Also available is a text editor and a file maintenance and debug routine that supports the floppy-disc based program development system.

**Special features of the instruction set** include the block-move operations that permit large sections of data held in memory to automatically be relocated.

### Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | 16 bits |
| Direct addressing range: | 65,536 words |
| Instruction word size: | One to three bytes |
| Number of basic instructions: | 158 |
| Shortest instruction/time (Load register to register): | 1 $\mu$s |
| Longest instruction/time (Set bit at address IX+d): | 5.75 $\mu$s |
| Clock frequency (min/max): | 5 kHz/4.5 MHz |
| Clock phases/voltage swing: | 1/5 V |
| Dedicated I/O control lines: | 5 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/90 mA (Z80A) |
| | 5 V/60 mA (Z80) |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| Z80 | CPU (commercial) | $ 24.50 |
| Z80 | CPU (military) | 165.00 |
| Z80A | 8-bit-commercial | 29.50 |
| Z80A | 8-bit-Mil | N/A |
| Z80-PIO | 2-port parallel I/O | 10.00 |
| Z80A-PIO | Higher speed version | 14.00 |
| Z80-CTC | Quad counter/timer | 16.00 |
| Z80A-CTC | Higher speed version | 20.00 |
| Z80-DMA | Two port direct memory access | 38.00 |
| Z80A-DMA | Higher speed version | N/A |
| Z80-SIO | Dual full-duplex serial I/O channels | N/A |
| Z80A-SIO | Higher speed version | N/A |

**Hardware support** provided for the Z80 includes a development system with in-circuit emulation capability, real-time debug and program storage modules. The system has a dual floppy-disc operating system and can be expanded to handle up to 64 kbytes of RAM and many interface options for terminals and printers.

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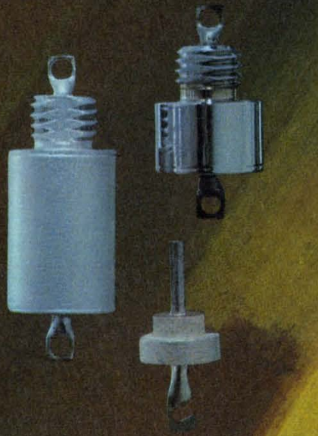

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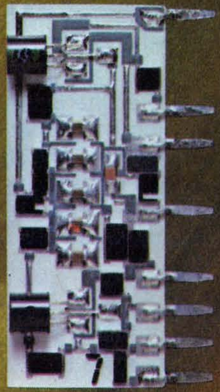

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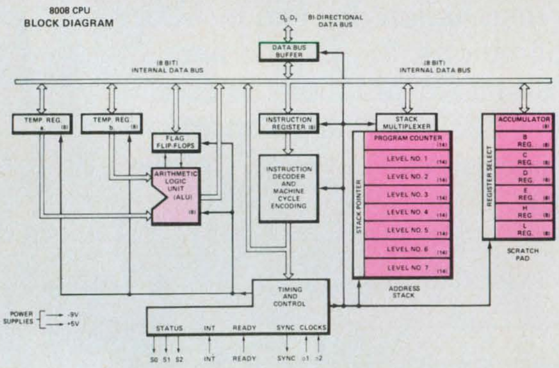
# 8-bit microprocessor, PMOS

## 8008, 8008-1

**Intel Corp.**
**3065 Bowers Ave.**
**Santa Clara, CA 95051**
**(408) 246-7501**

Alternate sources: None.
*Not recommended for new designs.*

The 8008 and 8008-1 were the first 8-bit single-chip microprocessors. There are currently just the two versions available—the 8008 has a 20 μs instruction time while the 8008-1 has a 12.5 μs cycle time. Either unit is a complete 8-bit parallel processor that can address up to 16 kbytes of memory, handle up to seven levels of subroutine nesting and respond to external interrupts. Most of the 48 instructions are oriented for data handling although addition, subtraction and logic operations are available.




The architecture of the 8008 family parts is similar to the 8080 which has superseded it. On the 8008 chip are a 7-word × 14-bit stack register, a 6-word x 8-bit scratchpad register and a parallel 8-bit ALU. An external clock is required along with some RAM or ROM to form a minimal operating system.

### Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | Multiplexed (8 bits and 6 bits) |
| Direct addressing range: | 16,384 bytes |
| Instruction word size: | 1, 2 or 3 bytes |
| Number of basic instructions: | 48 |
| Shortest instruction/time (Return): | 1.25 μs (8008-1) |
| Longest instruction/time (Call): | 37.5 μs (8008-1) |
| Clock frequency (min/max): | 333/500 kHz |
| Clock phases/voltage swing: | 2/11 V |
| Dedicated I/O control lines: | 4 |
| Package: | 18-pin DIP |
| Power requirements: | 5 V/20 mA<br>−9 V/40 mA |

### Comments

**The instruction set** for the 8008 family has 48 basic instructions that can be divided as follows: seven index register commands, 12 accumulator directions, 16 arithmetic, logic and shift commands, and 13 program counter, stack, I/O and machine instructions.

**Software support** for the 8008 family consists of the MCS-8 cross assembler, which is written in Fortran IV and can run on most 32-bit computer systems. Also available is an 8008 simulator that is written in Fortran IV.

**Software features** include the ability to access up to 16 kbytes of RAM or ROM with just an 8-bit data bus, the ability to handle up to seven nesting levels of subroutines and the capability to respond to externally generated interrupts.

**Hardware support** for the 8008 family is nonexistent since it is not recommended for new designs.

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| 8008<br>8008-1 | 8-bit microprocessor<br>8-bit microprocessor | $24.25<br>26.90 |

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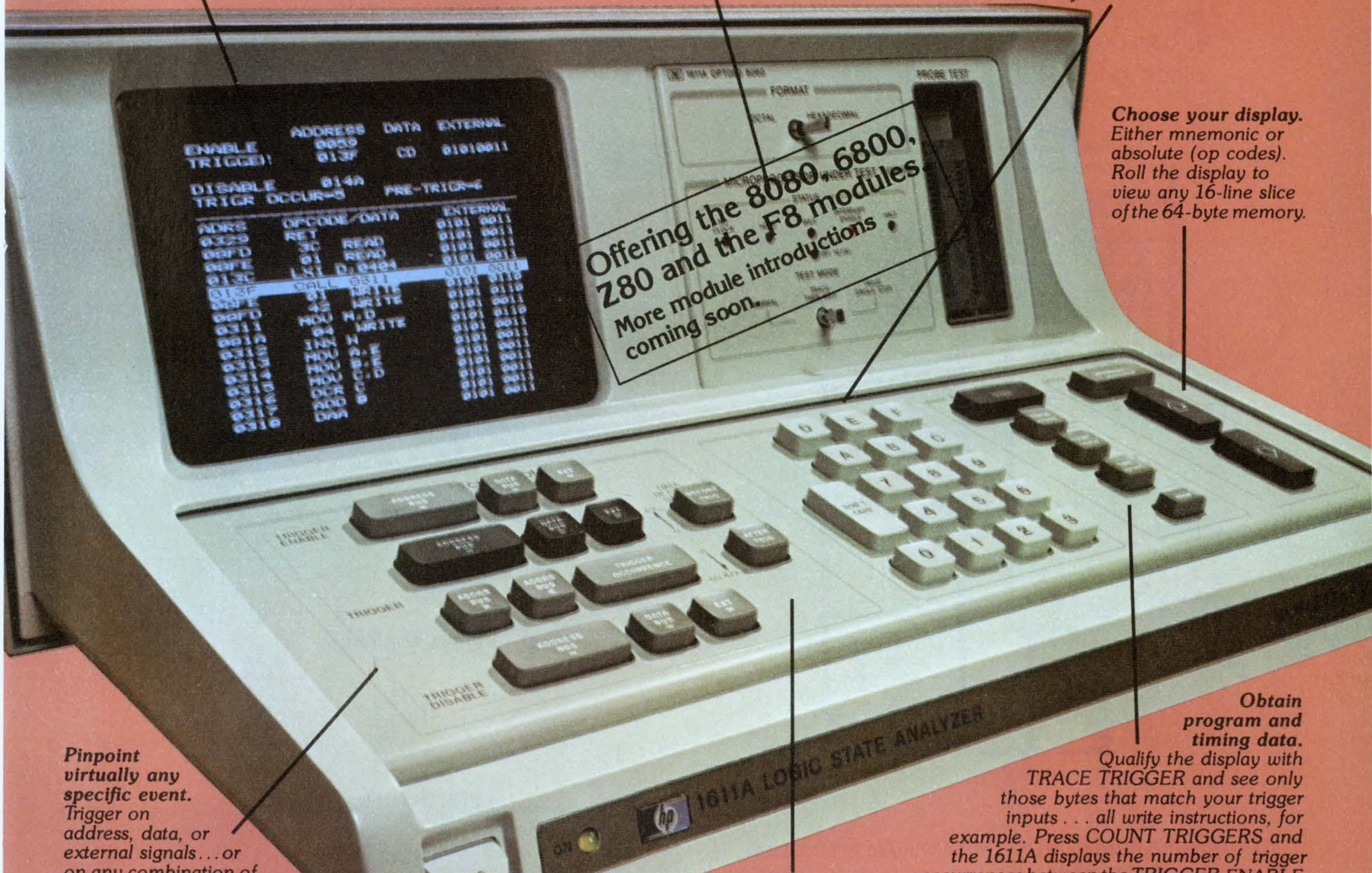


***Pinpoint virtually any specific event.*** *Trigger on address, data, or external signals... or on any combination of the three. You can also qualify the trigger by bracketing the address and opting to trigger on the nth occurrence of the trigger word. TRIGGER ENABLE and DISABLE keys act as arm and disarm circuits providing unparalleled pinpointing flexibility.*

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086/15

CIRCLE NUMBER 70

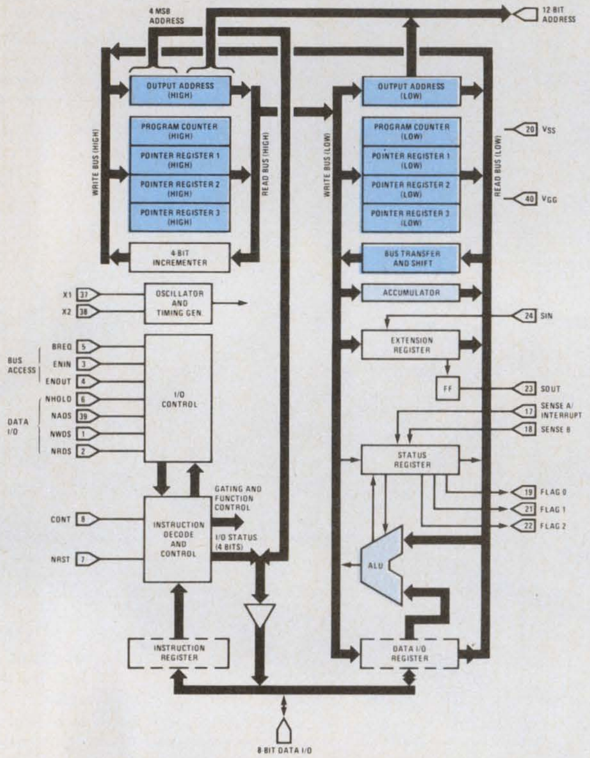
# 8-bit microprocessor, PMOS (SC/MP) or NMOS (SC/MP II)

National Semiconductor
2900 Semiconductor Drive
Santa Clara, CA 95051
(408) 737-5000

## SC/MP and SC/MP II

Alternate sources: Rockwell, Signetics and Western Digital for SC/MP II, none for SC/MP.

Both the SC/MP and SC/MP II are low cost 8-bit microprocessors intended primarily for simple control applications. The PMOS SC/MP costs under $10 but is limited to a 1-MHz maximum clock rate. The higher performance SC/MP II can operate at 4-MHz clock rates. Both versions have on-chip clock oscillators and timing generators.




The architecture of the SC/MP provides the processor with DMA capability as well as a simple cascadable structure that is handy for multiprocessing applications. On the chip is the clock circuit to simplify the timing requirements.

### Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | 12 bits |
| Direct addressing range: | 65,536 words |
| Instruction word size: | 8 and 16 bits |
| Number of basic instructions: | 46 |
| Shortest instruction/time (Shift, rotate, I/O): | 5 μs (NMOS)* |
| Longest instruction/time (Decimal add): | 23 μs (NMOS)* |
| Clock frequency (min/max): | Dc/1 MHz (PMOS); dc/4 MHz (NMOS) |
| Clock phases/voltage swing: | Internal |
| Dedicated I/O control lines: | 14 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/125 mA |
| *PMOS version requires double the time. | −7 V/135 mA |

### Comments

**The instruction set** of 46 commands breaks down into 24 single-byte instructions and 22 double-byte instructions. Single-byte instructions include those for an extension register, the pointer register, and for shift, rotate and serial I/O. Double-byte instructions include all memory operations.

**Software support** offered includes a high-level interpretive language, NIBL, written especially for the industrial user. Also available are conversational cross-assemblers that run on minicomputers. A Fortran cross-assembler is available on GE and National CSS time-sharing networks.

**Software features** include the ability to directly address up to 65 kwords with a 12-bit address bus and four bits siphoned from the data bus. SC/MP chips can be cascaded to simplify multiprocessing.

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| SC/MP | 8-bit CPU (PMOS) | $9.00 |
| SC/MP II | 8-bit CPU (NMOS) | N/A |
| DM8334 | 8-bit bit-addressable latch | 3.20 |
| DM8131 | 6-bit unified bus comparator | 2.56 |
| DM8546 | Three-state, 8-bit, I/O shift register | 3.84 |
| MM5307 | Baud-rate generator/ programmable real-time clock | 12.00 |
| DS8692, 8693,8694 | Seiko-printer interface set | N/A |

**Hardware support** for the SC/MPs comes in several forms. For low cost, the SC/MP kit provides a minimal system with a TTY interface. A portable terminal, the SC/MP keyboard kit, permits simple program entry and development. More extensive support comes from application cards (CPU, RAM and ROM/PROM) and a complete stand-alone development system (LCDS).

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SYSTRON DONNER

CIRCLE NUMBER 71

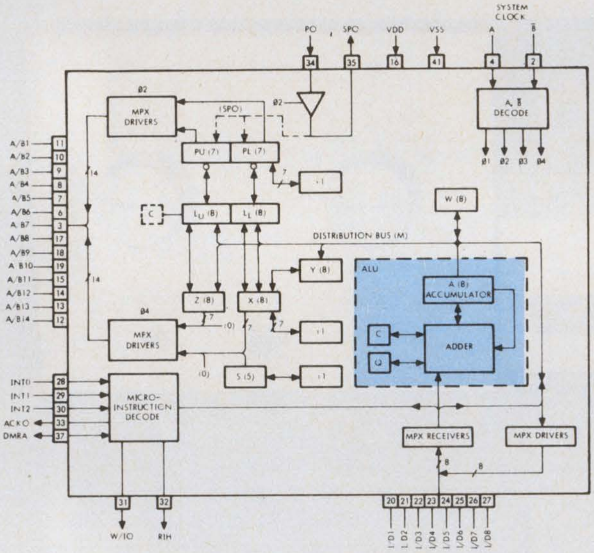
# 8-bit microprocessor, PMOS

## PPS-8, PPS-8/2 (P/N 11806)

Rockwell International
P.O. Box 3669
Anaheim, CA 92803
(714) 632-3729

Alternate sources: AEG Telefunken.

Eight-bit parallel processing systems, the PPS-8 and PPS-8/2 form minimum microcomputers with five and two-chip sets, respectively, and are software compatible. The CPU chip can handle both prioritized interrupts and direct memory accesses.




The architecture of the PPS-8 processor is designed to handle both binary and BCD arithmetic. An external two-phase clock must be used, but inside the chip the clock is expanded into four-phase dynamic logic. A minimal system configuration consists of the CPU, a clock and the necessary memory and I/O circuits.

### Specifications

| | |
|---|---|
| Data word size: | 8 bits |
| Address bus size: | 14 bits |
| Direct addressing range: | 16,384 bytes |
| Instruction word size: | 8, 16, 24 bits |
| Number of basic instructions: | 109 |
| Shortest instruction/time (Many): | 4 μs |
| Longest instruction/time (Some): | 15 μs |
| Clock frequency (min/max): | 199/256 kHz |
| Clock phases/voltage swing: | 2/MOS |
| Dedicated I/O control lines: | 15 |
| Package: | 42-pin QUIL |
| Power requirements: | 17 V/35 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| PPS-8 | CPU | $20.00* |
| PPS-8/2 | CPU | $11.25* |
| 10706 | Clock generator | $ 7.45 |
| 10738 | Bus interface | $ 4.50 |
| 11049 | Interval timer | $ 8.50 |
| 10817 | DMA controller | $18.75 |
| 10453 | Parallel data controller | $15.00 |
| 10936 | Floppy disc controller | $40.00 |
| 10696 | General purpose I/O | $ 8.50 |
| 10930 | Serial data controller | $15.00 |

*Price as of Oct. 1. Peripheral circuit prices have been cut as well. Consult distributors.

### Comments

**The instruction set** of the PPS-8 family consists of 24 data transfer commands, 10 stack operations, 13 arithmetic and logic instructions, six increment/decrement operations, 23 branch/skip commands, 21 register operations, four I/O instructions and eight bit-manipulation directions.

**Software support** for the PPS-8 family consists of a Fortran IV cross assembler and a Fortran IV simulator. There is also a software development system, the PPS MP Universal Assemulator, that does program assembly, debug, emulation and even incoming device testing.

**Software features** include BCD arithmetic capability as well as dedicated I/O instructions. Software controlled DMA transfers of up to eight prioritized channels at 256 kbytes/s are possible. There is also a 5-bit stack pointer available to address the subroutine stack.

**Hardware support** includes a floppy-disc based program/hardware development system, the PPS MP Universal Assemulator. There are also many peripheral interface cards and memory support products available.

# 1976:

## Shugart introduces minifloppy,® the first miniature floppy.

# 1977:

## Shugart reduces minifloppy prices by 15%.

Experience pays. When Shugart introduced the first miniature floppy, OEM's and end-users gained floppy access speed and reliability at a cost competitive with cassettes. The value was obvious to OEM's. Wang Laboratories. North Star. ICOM (Pertec). Southwest Technical. Intelligent Systems. All are buying quantities of Shugart minifloppy drives and going after new markets.

Now, with minifloppy deliveries approaching 10,000 units, Shugart does it again. High volume production expertise allows the impossible—a 15% reduction in price.

What's coming next from Number 1? Now you can reach data in milliseconds with our field-proven spiral cam actuator. Depend on a reliability of 8000 Power-On-Hours MTBF. Gain a two orders of magnitude improvement in error rate compared to cassettes. And record your data safely with the industry accepted high margin 35 track format.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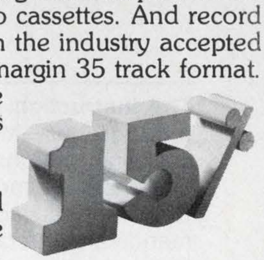
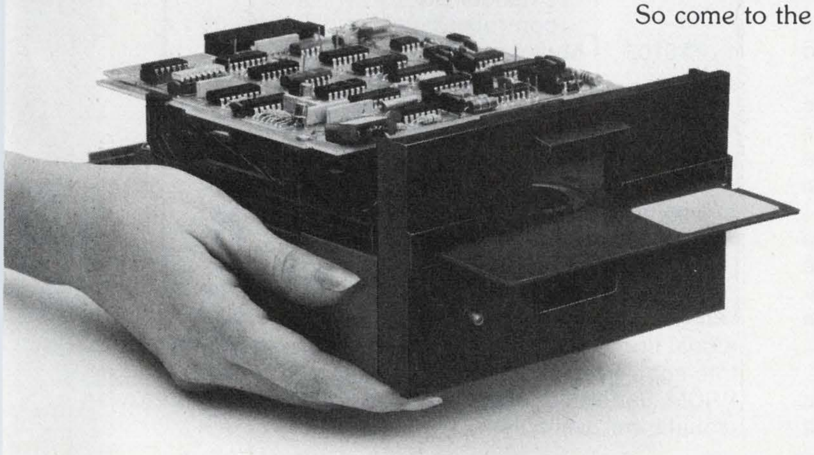



So come to the people who started the minifloppy revolution. Shugart.

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™ ministreaker is a Shugart trademark

CIRCLE NUMBER 72

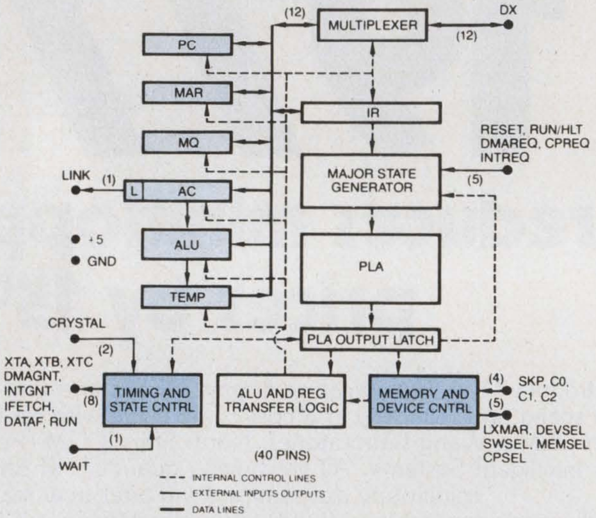
# 12-bit microprocessor, CMOS

## IM 6100

**Intersil, Inc.**
**10900 N. Tantau Ave.**
**Cupertino, CA 95014**
**(408) 996-5000**

**Alternate sources: Harris Semiconductor.**

Able to emulate the Digital Equipment Corp. PDP-8 minicomputer's instruction set, the IM 6100 processor provides the user with a wealth of readily available software. The CMOS processor can also operate from a single supply and, since it draws only about 2 mA (at 5 V and 4 MHz) it is ideal for portable equipment design. The processor's architecture is also very similar to that of the PDP-8, with the only major difference in the bus—the IM 6100 doesn't use the DEC patented Unibus structure and timing.




The architecture of the IM 6100 resembles that of the PDP-8 minicomputer. Signals are available that can help create a front panel so that the processor can be manually controlled. The processor's on-board crystal-controlled clock can be driven by an external source.

### Specifications

| | |
|---|---|
| Data word size: | 12 bits |
| Address bus size: | 12 bits |
| Direct addressing range: | 256 words |
| Instruction word size: | 12 bits |
| Number of basic instructions: | 80 |
| Shortest instruction/time (AND, OR, Jump, etc.): | 2.5 $\mu$s |
| Longest instruction/time (Autoindexed increment and skip if zero): | 5.5 $\mu$s |
| Clock frequency (min/max): | Dc/8 MHz (10 V) |
| Clock phases/voltage swing: | 1/CMOS or TTL |
| Dedicated I/O control lines: | 24 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/2.5 mA or 10 V/10 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| IM 6100 | 12-bit CPU (commercial) | $15.00 |
| IM 6100 | Industrial grade CPU | 16.50 |
| IM 6100 | Military grade CPU | 52.80 |
| IM 6101 | Programmable parallel interface element | 8.65 |
| IM 6102 | Memory extender/DMA controller/timer | 15.00 |
| IM 6103 | Multimode latched port | 10.00 |
| IM 6402 | CMOS UART (16x clock) | 4.00 |
| IM 6403 | CMOS UART (xtal clock) | 4.00 |
| IM 6312 | 1 k x 12 mask ROM | 27.90 |
| IM 6512 | 64 x 12 CMOS RAM | 5.00 |
| IM 6603 | 1 k x 4 CMOS UV EPROM | 25.00 |

### Comments

**The instruction set** of the IM 6100 is divided into three groups—Memory reference instructions, Operate instructions, and Output transfer instructions. There are six memory reference instructions, with three addressing modes each. Another 62 commands are Operate instructions and the remaining 12 instructions are I/O transfer commands.

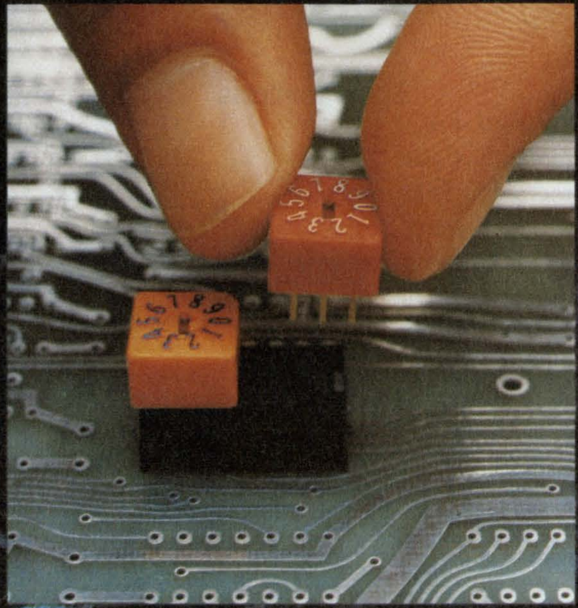
**Software support** offered includes an extended software package containing loaders, editors, assemblers, debuggers and a floating point arithmetic program. Also available is FOPAL, a Fortran cross assembler, FOCAL, a high-level interpreter and the DECUS program library with over 1000 programs.

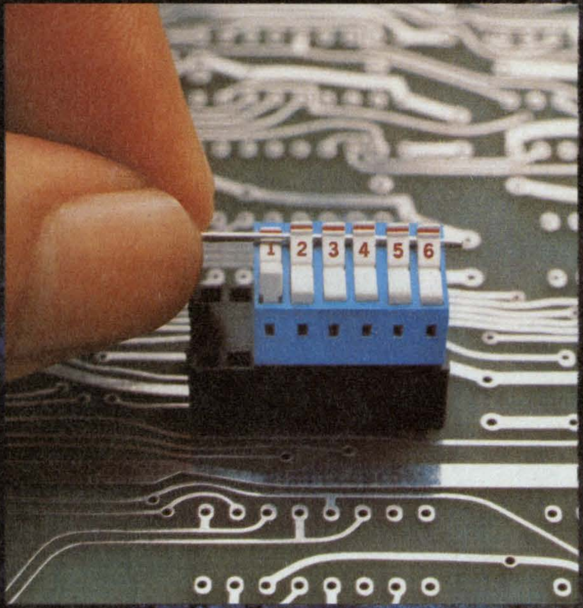
**The most important software features** include the code-compatibility with the PDP-8 and the flexible addressing modes. And, some of the Operate instructions can be combined with other Operate commands to make multifunction instructions.

**Hardware support** for the IM 6100 ranges from a single-board learning system—the Intercept Jr.—to a dual floppy-disc based development system—the Intercept. Plug-in boards, including 1 k RAM, 2 k PROM, Serial I/O, cassette interface, and parallel I/O circuits are available.

# MICRO / MINI

## DIP SWITCH / DIP SWITCH






MICRO-DIP...10 and 16 position miniature binary coded DIP switch designed to be mounted directly to PC Boards. Ideal for address encoding, pre-setting, PCB programming...every area of digital electronics.

Packaged in a color coded, glass-filled nylon housing with terminals on .100 x .300 centers. It occupies only one half of a standard 14-pin DIP socket.

Screwdriver slot is rotated in either direction to desired setting. Gold contacts protected by dust-seal design.

Positive detenting 10 position BCD, 16 position binary with separate common to not true bits, repeating 1 and 2 pole codes. Guaranteed life of 10,000 detent operations. Operating temperature range of −10°C to +85°C, contact resistance of 25 milliohms max. initial.

One year warranty.

MINI-DIP...new from EECO. Form A and C contact arrangements ideal for positive on/off switching and programming.

Easily actuated, positive wiping, gold contacts are packaged in a dust free glass-filled nylon housing.

Interference-fit of terminal pins and one piece housing prevent contamination. Larger cross section pins allow positive insertion into sockets and P.C. Boards.

New locking design in which .035 diameter locking rod is inserted through rockers, insures against accidental actuations.

Guaranteed life of 50,000 cycles. Operating temperature range −10°C to +85°C, contact resistance 25 milliohms max. initial.

Standard .100 x .300 centers allows retrofitting of other major brands of DIP switches. Available in 2-10 station Form A, 1-5 station Form C contacts.

One year warranty.

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CIRCLE NUMBER 73

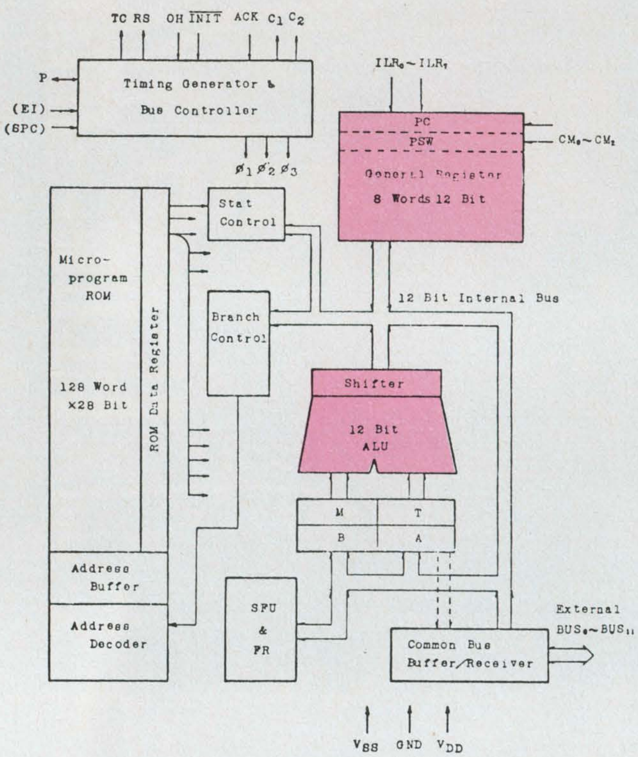
# 12-bit microprocessor, PMOS

## T3190

Alternate sources: None.

**Toshiba Transistor Works**
**1 Komukai Toshiba-cho Kawasaki-shi**
**Kanagawa-ken, Japan**
**044-511-3111**

The 12-bit microprogrammed parallel processor has machine instructions such as multiply and divide. Other features include asynchronous read/write, DMA capability, eight-level prioritized interrupt and seven addressing modes.




The T3190 has a three-state data/address bus and an eight-word register stack. The minimum system requires a processor, the MM111C RAM, TMM121C PROM, T3416 memory control unit, T3418 I/O control unit, and a 3220 general-purpose I/O register.

### Specifications

| | |
|---|---|
| Data word size: | 12 bits |
| Address bus size: | 12 bits |
| Direct addressing range: | 4096 words |
| Instruction word size: | 12 bits |
| Number of basic instructions: | 21 |
| Shortest instruction/time (Load register): | 6.6 $\mu$s |
| Longest instruction/time (Divide): | 104 $\mu$s |
| Clock frequency (min/max): | 0.63/2 MHz |
| Clock phases/voltage swing: | 3/Internal |
| Dedicated I/O control lines: | None |
| Package: | 36-pin DIP |
| Power requirements: | 5 V/140 mA<br>−5 V/35 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| T3190 | 12-bit $\mu$P | $47.00 |
| T3219 | Interrupt latch unit | 13.00 |
| T3220 | Gen-purp. I/O register | 15.00 |
| T3269 | Bidirectional driver | 12.00 |
| T3416 | Memory control unit | 16.00 |
| T3418 | I/O control unit | 13.00 |
| T3445 | DMA control unit | 28.00 |
| TMM111C | 128 × 4 static RAM | 8.50 |

### Comments

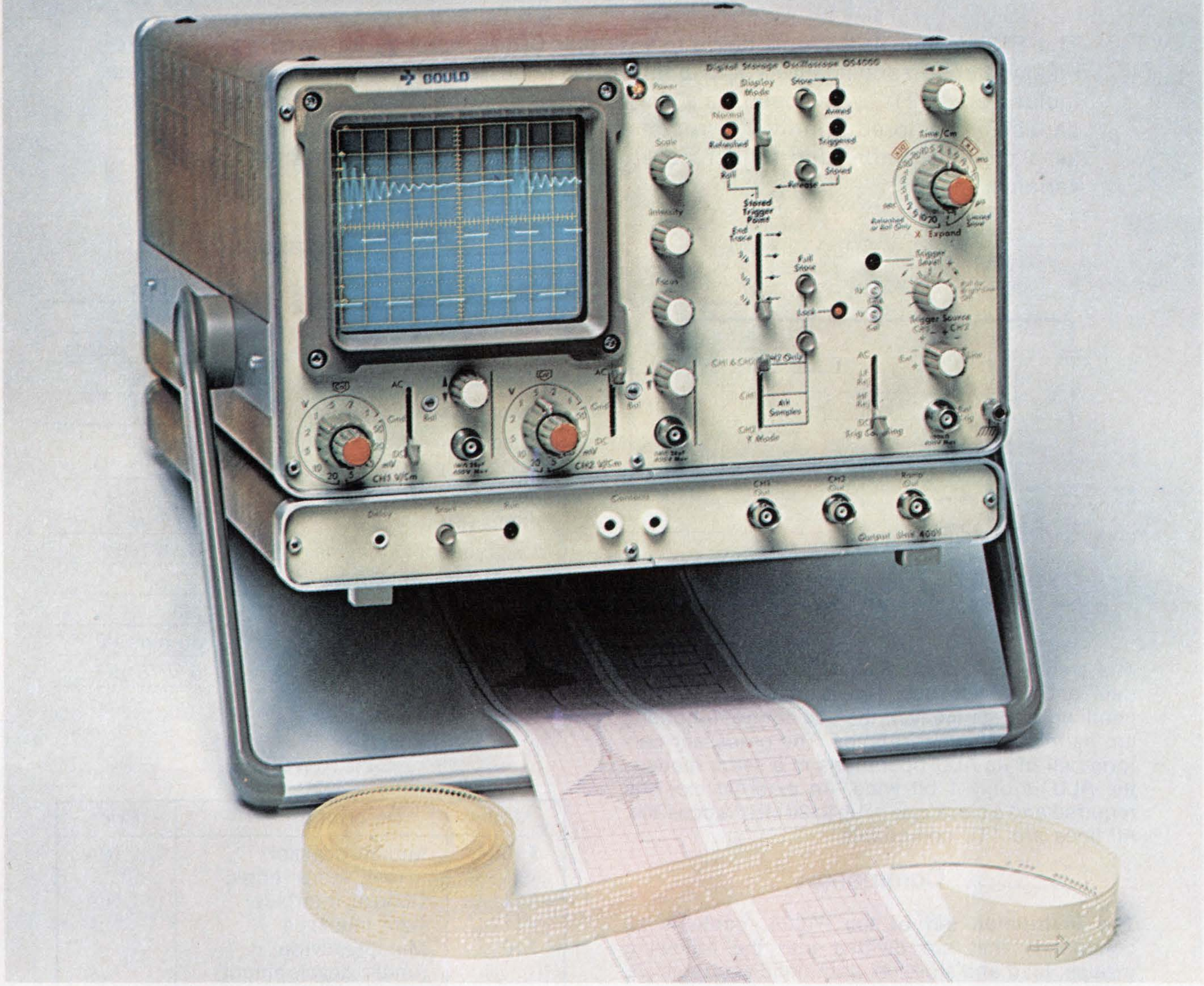
**The instruction set** consists of three data transfer instructions, nine logical instructions, seven arithmetic instructions including multiply and divide, and two branch instructions.

**Software support** consists of a cross-assembler and simulator written in Fortran VI, a self-assembler and a software package including debug and PROM program. Floating-point arithmetic package and over 50 other programs are available.

**Software features** of the T3190 include hardware multiply and divide capability as well as multi-bit rotates.

**Hardware support** includes EX-0 (a single-board computer containing 512 words of RAM, 3.5 kwords of PROM and a control panel); EX-1 (a single board with 4 k RAM or PROM, TTY interface and a control panel); EX-12/5 (a single board with 2 k of RAM, 2 k of PROM and a control panel); and EX-12/10 (a single board with 2 k of RAM, 2 k of PROM, a TTY interface, a DMA controller and a control panel).

# Gould OS4000
## Unlimited storage, plus hard copy option



The OS4000 dual trace storage oscilloscope gives you unlimited storage time, providing a unique capability for examining waveforms. It is ideal for displaying and recording transient waveforms for medical, electrical, vibration, dynamic testing and pulse testing applications. In addition you get the full capability of a conventional DC to 10MHz dual trace oscilloscope.

Digital storage provides non-flicker viewing of ultra-low frequencies plus simultaneous viewing of stored and real-time signals, and allows examination of single events prior to as well as after the trigger point. By using the 4001 manual or 4002 automatic output options you can have hard copy output on any X-Y or T-Y recorder. Digital output also provided.

For full details on the OS4000 and the 4001/2 Output Options write: Gould Inc., Instruments Systems Division 3631 Perkins Avenue, Cleveland Ohio 44114. Or call the number below.
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GOULD


# Gould Oscilloscopes
## They have a name for reliability

CIRCLE NUMBER 74

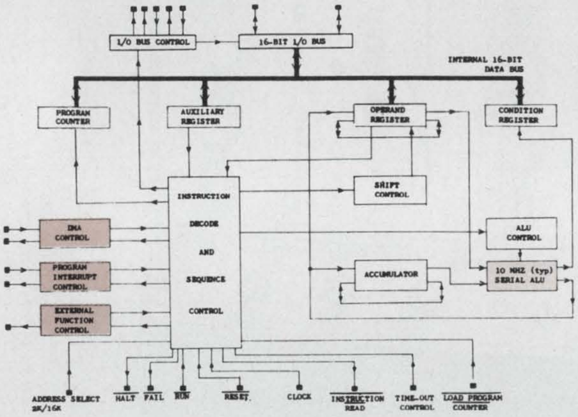
# 16-bit microprocessor, bipolar

## F100-L

**Ferranti Limited**
**Western Road, Bracknell**
**Berkshire RG12 1RA, England**
**(0344)3232**

Alternate sources: None.

The F100-L and its support chips use bipolar CDI technology and was developed to meet defense specifications and operate over the full MIL temp range. Its features include an 8 MHz cycle speed via a single-phase clock; multiple direct memory access capability; vectored priority interrupts; and the ability to call external hardware, such as a multiply/divide chip (under development). The 29 basic instructions yield 110 variants.




The architecture of the F100-L uses a multiplexed data and address bus. However, to simplify the handling of data many of the bus control functions are handled by support chips. The processor performs all of its ALU operations in a serial mode—the ALU is only 1 bit wide. An external clock is required and a clock rate of up to 20 MHz is possible. All lines are TTL compatible.

### Specifications

| | |
|---|---|
| Data word size: | 16 bits |
| Address bus size: | 16 bits |
| Direct addressing range: | 32,796 words |
| Instruction word size: | 16 bits |
| Number of basic instructions: | 29 |
| Shortest instruction/time (Uncond. jump): | 0.94 $\mu$s |
| Longest instruction/time (Jump using stack): | 5.75 $\mu$s |
| Clock frequency (min/max): | Dc/8 MHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | 10 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/75 mA |

### Hardware

| Model | Description | Price |
|---|---|---|
| F100-L | Microprocessor (MIL temp range) | N/A |
| F111-L | Control interface | N/A |
| F112-L | Data interface | N/A |
| F101-L | Multiply-divide (under development) | N/A |

### Comments

**The instruction set** of the F100-L contains 29 commands that are divided into the following groups: load and store (2), arithmetic and logic (7), shifts (6), bit manipulation (2), jumps (10), and machine control (2). The processor also has four addressing modes—direct, pointer indirect, immediate data and immediate indirect.

**Software support** for the F100-L is available on many levels. Programs can be written in F100-L assembly language or in a real-time high-level language called Coral 66. There are several cross-software products—a simulator, an assembler and a linking editor—all written in Fortran IV and available on time-sharing networks or for in-house use.

**Special features of the software** include the ability to transfer control to another "slave" processing chip, individual bit set and reset instructions and the indirect addressing modes.

**Hardware support** consists of several chips to simplify direct memory accesses and control of peripheral devices. There are also some microcomputer systems available that can be used for prototyping or the final system. Available are a 13-slot card cage with power supply, a processor card, RAM cards, ROM cards, specialized interfaces and prototyping cards.

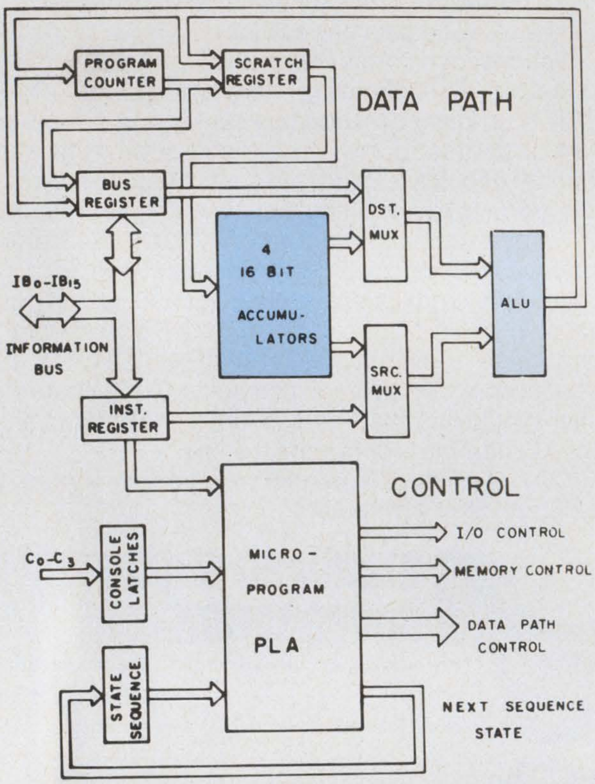
# 16-bit microprocessor, I³L

## 9440

**Fairchild Camera and Instrument Corp.**
**464 Ellis Street**
**Mountain View, CA 94042**
**(415) 962-5011**

Alternate sources: None.

The 9440 is a 16-bit microprocessor fabricated with the company's proprietary Isoplanar $I^2L$ process ($I^3L$). Housed in a 40-pin DIP, the processor requires less than a watt. All of the 9440's software is instruction compatible with the Nova minicomputer series made by Data General Corp. Up to 63 peripheral I/O devices can be serviced via the programmed or interrupt driven I/O.




The architecture of the 9440 varies considerably from that of the Nova although the $\mu$P can perform the same instructions. The 9440 uses a 4-bit ALU to process data and has an on-board clock generator that just needs an external crystal. Three-state outputs are included on the data/address bus, otherwise all lines are TTL compatible.

### Specifications

| | |
|---|---|
| Data word size: | 16 bits |
| Address bus size: | 15 bits |
| Direct addressing range: | 32,768 |
| Instruction word size: | 16 bits |
| Number of basic instructions: | |
| Shortest instruction/time (Jump to subroutine): | 1.12 $\mu$s |
| Longest instruction/time (Increment and skip if zero): | 3 $\mu$s |
| Clock frequency (min/max): | Dc/10 MHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | 4 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/150 mA<br>1 V/200 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| 9440 | 16-bit microprocessor There are currently no special support circuits available. | N/A |
| 9441 | Memory control unit | N/A |
| 9442 | I/O control unit | N/A |
| 9443 | Hardware multiply/divide | N/A |

### Comments

**The instruction set** of the 9440 contains all the Nova 1200 minicomputer commands. Basic operations include arithmetic and logic commands, memory reference operations, flag or bit test directions, I/O instructions and branch operations.

**Software support** includes resident diagnostics, assemblers, compilers, editors, operating systems, high-level languages such as Basic and Fortran, and stand-alone software. There is no program library available from Fairchild, but many companies offer code-compatible Nova software.

**Special features of the software** include the various addressing modes—absolute addressing of page zero, and three relative addressing modes using one of the multiple accumulators or program counter.

**Hardware support** for the 9440 has not yet been defined. However, expected aids will consist of full development systems and hardware debugging tools. Many companies offer Nova hardware.

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## KJL-SERIES I AND KJ SERIES II (SCOOP PROOF, LOW PROFILE) CONNECTORS...DESIGNED TO MIL-C-38999 WITH CANNON'S NEW HIGH STRENGTH RETENTION SYSTEM "SUPER CAESAR™"

- High contact density
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- Crimp snap-in contacts in the *NEW* SUPER CAESAR™ rear release contact retention assembly.

ITT Cannon's KJL and KJ miniature circular connectors are environment-resistant and designed to meet the critical performance and design requirements of MIL-C-38999. Engineered for high density circuitry capabilities, these connectors are designed to operate at temperatures ranging from −85°F to +392°F. They are readily adaptable to both commercial and space age requirements where size, weight, low-profile/scoop proof design and high reliability are key factors. KJL/KJ connectors are offered in nine shell sizes. A total of 59 contact arrangements are available that will accommodate from 3 to 128 contacts using AWG wire sizes 16 through 28. Contacts are of high conductivity copper alloy with gold plated finish.

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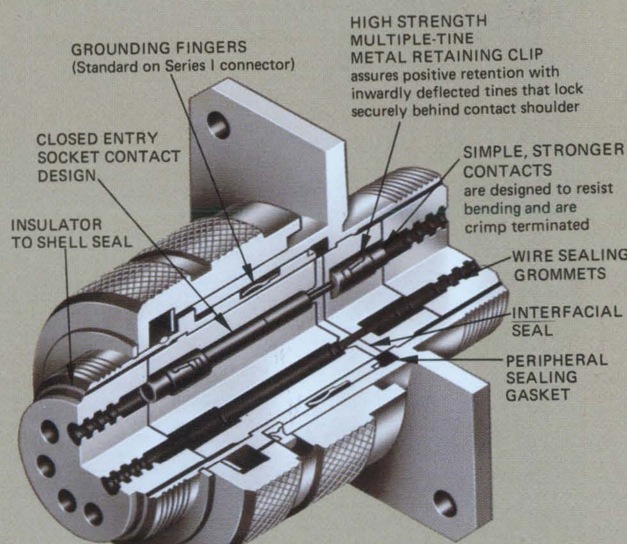
Contact retention is provided by the newly developed SUPER CAESAR™ rear release contact assembly. SUPER CAESAR more than meets the MIL Specs, for contact retention. The assembly features a multiple-tine metal retaining clip housed in a monobloc plastic insert. Contacts are inserted, released, and extracted from the rear of the connector, offering lower installation and maintenance costs to the user.

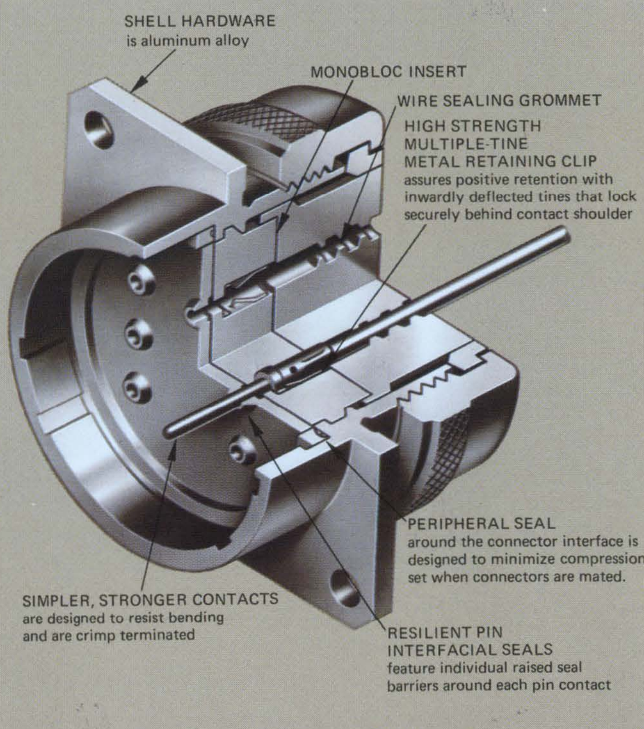
Monobloc (one-piece) inserts are made of strong, durable plastic. Pin contact cavities in the insert are constructed with a closed-down effect. This feature offers superior pin stability and positive axial alignment of the contacts. Lead-in chamfers in the socket front insert face provide for positive contact mating. The shells also feature five-keyway shell polarization to assure alignment during engagement. A three-point bayonet lock coupling provides fast connect and disconnect. Complete environmental sealing is accomplished by an interfacial seal, with individual raised tapered sealing barriers around each pin contact; a peripheral seal, and a multiple-ripple wire sealing grommet. Hermetic shell styles are also available.

For further information, please contact your nearest ITT Cannon sales office or write to 666 East Dyer Road, Santa Ana, CA 92702. Telephone (714) 557-4700.

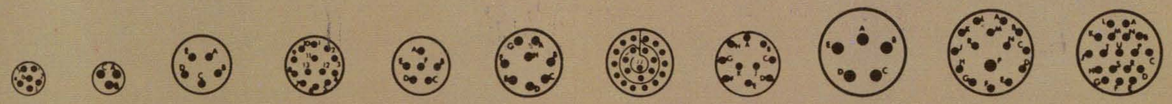
## KJL SERIES I



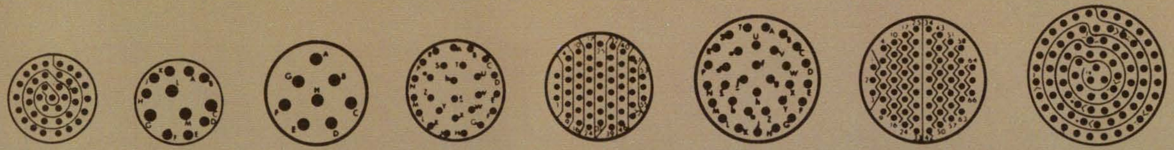

## KJ-SERIES II



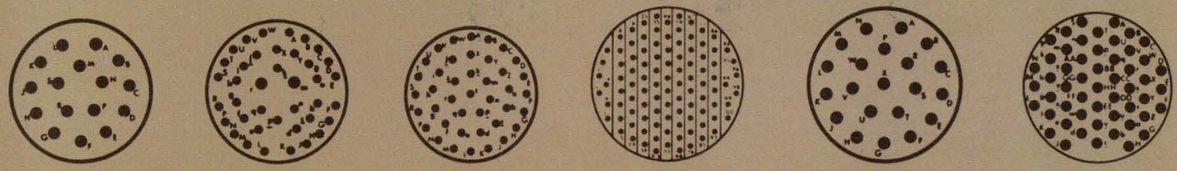
## CONTACT ARRANGEMENTS KJL-SERIES I (ENGAGING VIEW PIN INSERT)



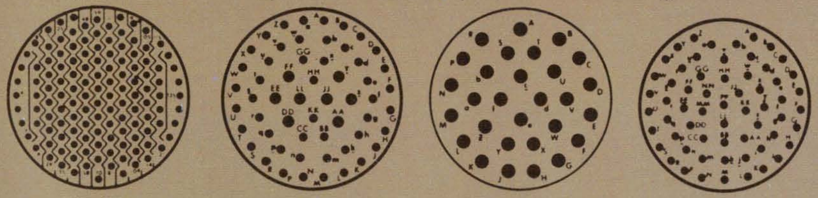
| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 9-35 | 9-98 | 11-5 | 11-35 | 11-98 | 13-8 | 13-35 | 13-98 | 15-5 | 15-15 | 15-18 |
| 6 #22D | 3 #20 | 5 #20 | 13 #22D | 6 #20 | 8 #20 | 22 #22D | 10 #20 | 5 #16 | 14 #20, 1 #16 | 18 #20 |
| M | I | I | M | I | I | M | I | II | I | I |



| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 15-35 | 15-97 | 17-8 | 17-26 | 17-35 | 19-32 | 19-35 | 21-35 |
| 37 #22D | 8 #20, 4 #16 | 8 #16 | 26 #20 | 55 #22D | 32 #20 | 66 #22D | 79 #22D |
| M | I | II | I | M | I | M | M |



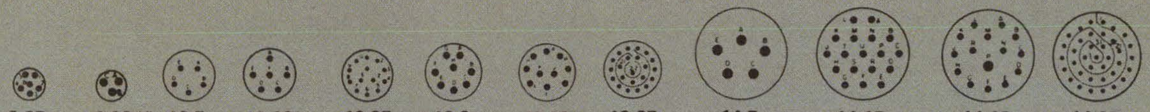
| | | | | | |
|---|---|---|---|---|---|
| 21-16 | 21-39 | 21-41• | 23-35 | 23-21 | 23-53 |
| 16 #16 | 37 #20, 2 #16 | 41 #20 | 100 #22D | 21 #16 | 53 #20 |
| II | I | I | M | II | I |



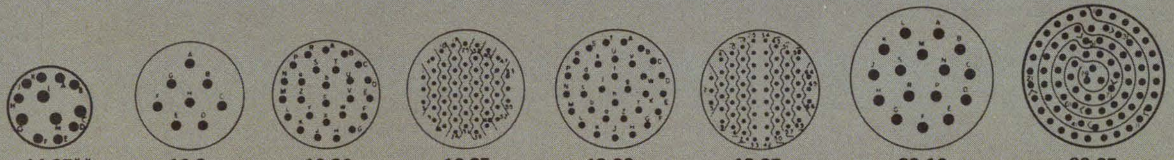
| | | | |
|---|---|---|---|
| 25-35 | 25-4 | 25-29 | 25-61 |
| 128 #22D | 48 #20, 8 #16 | 29 #16 | 61 #20 |
| M | I | I | I |

LEGEND
Shell Size . . . . . . . 9-35
No. of Contacts . . 6# 22D
Service Rating . . . M

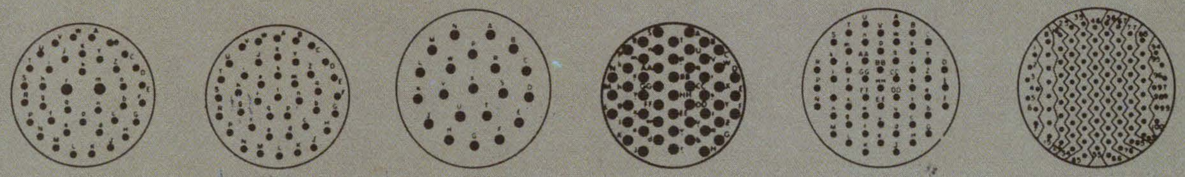
## CONTACT ARRANGEMENTS KJ SERIES II (ENGAGING VIEW PIN INSERT)



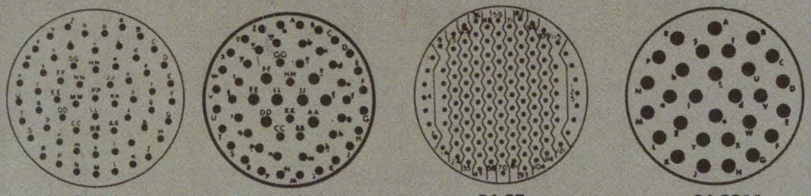
| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 8-35 | 8-98** | 10-5 | 10-98•** | 10-35• | 12-8** | 12-98• | 12-35• | 14-5 | 14-15 | 14-18• | 14-35• |
| 6 #22D | 3 #20 | 5 #20 | 6 #20 | 13 #22D | 8 #20 | 10 #20 | 22 #22D | 5 #16 | 1 #16, 14 #20 | 18 #20 | 37 #22D |
| M | I | I | I | M | I | I | M | II | I | I | M |



| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 14-97** | 16-8•** | 16-26 | 16-35• | 18-32 | 18-35• | 20-16 | 20-35• |
| 8 #20, 4 #16 | 8 #16 | 26 #20 | 55 #22D | 32 #20 | 66 #22D | 16 #16 | 79 #22D |
| I | II | I | M | I | M | II | M |



| | | | | | |
|---|---|---|---|---|---|
| 20-39 | 20-41 | 22-21 | 22-53** | 22-55 | 22-35 |
| 37 #20, 2 #16 | 41 #20 | 21 #16 | 53 #20 | 55 #20 | 100 #22D |
| I | I | II | I | I | M |



| | | | |
|---|---|---|---|
| 24-61 | 24-4** | 24-35• | 24-29** |
| 61 #20 | 48 #20, 8 #16 | 128 #22D | 29 #16 |
| I | I | M | I |

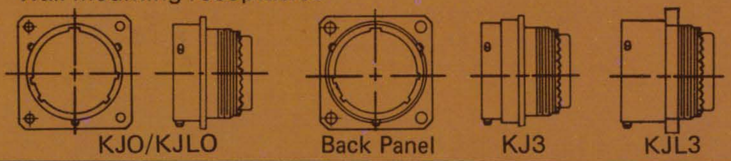
LEGEND
Shell Size . . . . . . . 10-5
No. of Contacts . . 5# 20
Service Rating . . . I

• Indicates layouts are available in all shell styles, including MS27499, MS27508, KJ2E and KJ5E

**Pin insert only

## CONFIGURATIONS KJL AND KJ SERIES I AND II

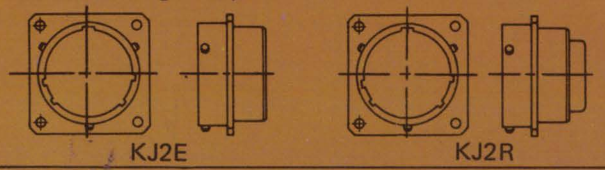
Wall mounting receptacles



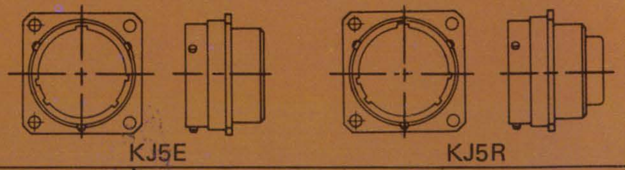

Available in shell sizes

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | (KJ Series II) |
| 9 | 11 | 13 | 15 | 17 | 19 | 21 | 23 | 25 | (KJL Series I) |

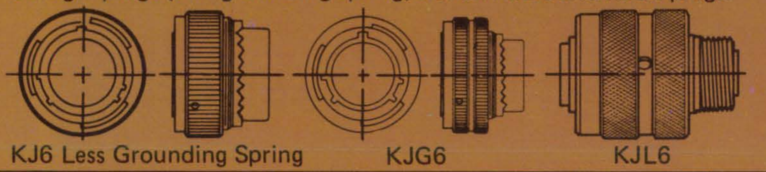
Box mounting receptacles



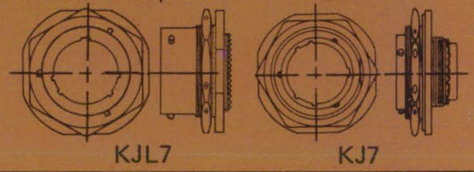

Back panel configurations



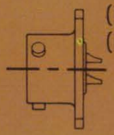

Straight plugs (RFI grounding spring, std. on KJL 6 and KJG6 plugs.




Jam nut receptacles

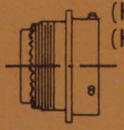



Hermetic receptacles



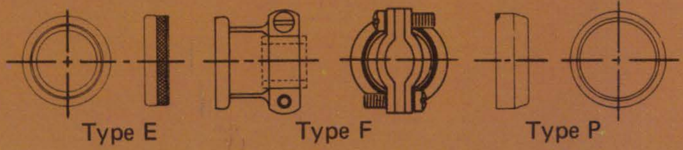
(KJY-series II)
(KJLY-series I)

Filter receptacles



(KJJ-series II)
(KJJL-series I)

Backshell accessories




## ACCESSORIES

Shown here are accessories for the new KJL and KJ series. The clean design of the crimp snap-in contacts meets MIL spec requirements. The contacts are made of high conductivity copper alloy and are available in sizes 16 thru 22D. Contact size 16 will accommodate AWG wire sizes 16, 18 & 20. Contact size 20 will accommodate AWG wire sizes 20, 22 & 24. Contact size 22D will accommodate AWG wire sizes 22, 24, 26 & 28.

Wire sealing plugs meet MS27488 standards. The plugs are color coded according to size for easy identification. Both contacts and wire sealing plugs may be ordered separately.

## TOOLS

A complete line of MS and ITT Cannon crimping, insertion and extraction tools are available for the KJL and KJ connectors. All of the tools are precision instruments produced from the finest materials and are designed for long life and trouble-free service.

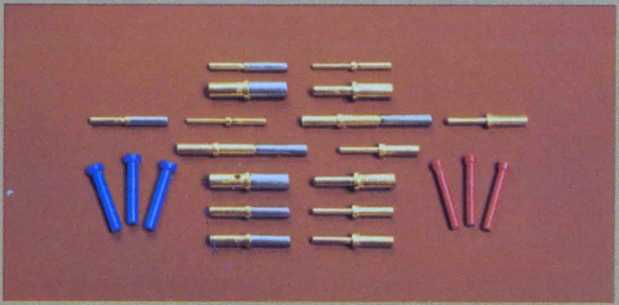
Insertion and extraction tools may be ordered for both series. These rugged tools are maintenance-free and are color coded for quick contact size identification.

The insertion tools have a single color band to indicate tool size. Extraction tools are coded with two color bands, one to indicate tool size, and one to indicate removal tool.

## AVAILABILITY **Cannon's got it**

ITT Cannon Electric products and engineering services are available throughout the world. Distributors across the United States maintain comprehensive inventories for immediate off-the-shelf delivery; most are Cannon Authorized Plug Specialists (CAPS®). CAPS distributors operate local assembly centers set to our factory standards. More specialized orders are expedited at the factory level.

Contacts



| Series | Cannon Contact | Size | Description | MS Contact* |
|---|---|---|---|---|
| KJL | 021-1251-001 | 16 | Socket | MS27490-16 |
| KJL | 031-1250-001 | 20 | Socket | MS27490-20 |
| KJL | 031-1147-007 | 22D | Socket | MS27490-22D |
| KJ | 031-1123-016 | 16 | Socket | MS27491-16 |
| KJ | 031-1124-020 | 20 | Socket | MS27491-20 |
| KJ | 031-1147-000 | 22D | Socket | MS27491-22D |
| KJL/KJ | 030-1995-016 | 16 | Pin | MS27493-16 |
| KJL/KJ | 030-1997-020 | 20 | Pin | MS27493-20 |
| KJL/KJ | 030-2042-000 | 22D | Pin | MS27493-22D |

*Specification MIL-C-39029/56;/57;/58.

For full details on the KJL/KJ series connectors contact product manager Circulars Division. ITT Cannon Electric, 666 East Dyer Road, Santa Ana, Calif. 92702. *Toll-free, 24-hr. (800) 854-3573; in Calif., (800) 432-7063.*

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Ms. Herold uses the GOLD BOOK about 15 times a week. Among other purchases, she has recently ordered 300,000 resistors, 20,000 sockets, solder bars, a wave soldering machine and an axial forming machine through its use.

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# IF IT'S ELECTRONIC...IT'S IN THE GOLD BOOK!

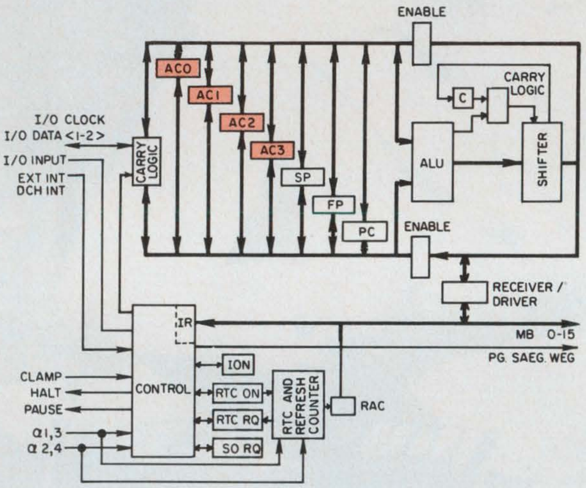
# 16-bit microprocessor, NMOS

## mN601 (microNova)

Alternate sources: None.

**Data General Corp.**
**Route 9**
**Southboro, MA 01772**
**(617) 485-9100**

Full Nova minicomputer 16-bit architecture and instruction set is included in a single 40-pin silicon-gate NMOS chip. Subroutine calls can be handled with Save and Return instructions. The processor performs 16-bit hardware multiply and divide, and is provided with hardware stack and frame pointers with stack overflow protection. System memory support can control up to 32 kwords of RAM/PROM, with integral hidden refresh and control logic for dynamic RAMs.




Included in the basic chip set are the mN601 microprocessor, mN640 clock driver and the mN629 I/O transceiver. All I/O lines are decoded for I/O interfacing and are not available for control purposes. The lines are open-collector TTL compatible. Four 16-bit registers in the CPU can act as source or destination accumulator.

### Comments

**There are 72 basic instructions** that are broken into six groups: Memory-reference, six instructions; Arithmetic and logic, 10 instructions; Input/output, 11 instructions; Stack manipulation, 12 instructions and Central processor control, nine instructions. The microNova instructions are code-compatible with existing Nova minicomputers, thus permitting simple processor upgrades.

**The choice of available software** is very wide since most Nova software will run on microNova systems. For program development, assemblers, text editors, library file editors and relocatable loaders are available. For disc-based development systems, high-level languages such as Basic and Fortran IV are available in addition to the disc-operating system. Most disc-based systems come with a program library that includes logarithmic, exponential, trig, array handling and character-formatting routines.

**Software features** include 16-level interrupt and Save and Return instructions for subroutine calls, and 16-bit hardware multiply and divide. Stack capability control is handled with hardware stack and frame pointer registers. The processor can also handle direct memory accesses via a control line.

### Specifications

| | |
|---|---|
| Data word size: | 16 bits |
| Address bus size: | 15 bits |
| Direct addressing range: | 32,768 words |
| Instruction word size: | 16 bits |
| Number of basic instructions: | 72 |
| Shortest instruction/time (Add): | 2.4 μs |
| Longest instruction/time (Divide): | 59.04 μs |
| Clock frequency (min/max): | dc/8.3 MHz |
| Clock phases/voltage swing: | 2/14 V |
| Dedicated I/O control lines: | None |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/20 mA |
| | 10 V/60 mA |
| | 14 V/30 mA |
| | 4.25 V/0.25 mA |

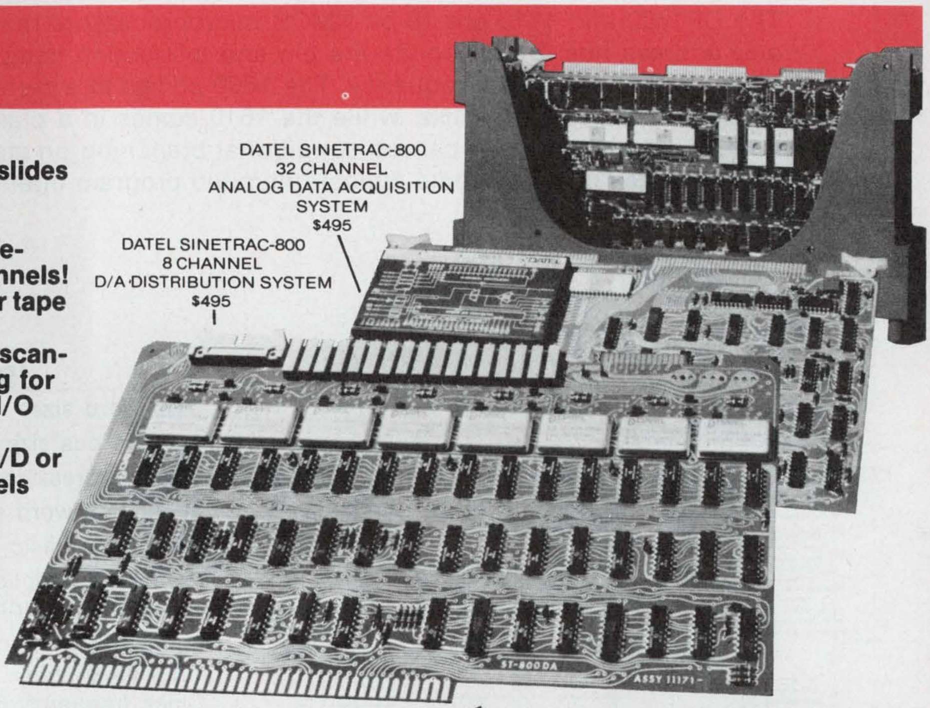
### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| mN601 | CPU | $114.95 |
| mN603 | I/O controller | $70.00 |
| mN606 | 4-k dynamic RAM | $13.00 |
| mN629 | CPU I/O Transceiver | $30.00 |
| mN634 | Octal bus transceiver | $10.00 |
| mN506 | Quad sense amp | $12.00 |
| mN636 | I/O controller transceiver | $10.00 |
| mN638 | Memory clock driver | $7.00 |
| mN640 | I/O & CPU clock driver | $7.00 |

**Memory support hardware** is provided by the following units: Models 8567 to 8570, PROM boards (512 to 4 kwords); Model 8572 (4 k RAM); and Model 8573 (8 k RAM). A PROM programmer board, Model 8574 is also available. Diskette subsystems include the single-drive Model 6038 and the dual-drive Model 6039. Interfacing is provided by the 4210 general purpose interface board and the 4207 asynchronous interface board.

# Datel's 8080 A/D-D/A Advantage

## SINETRAC 800

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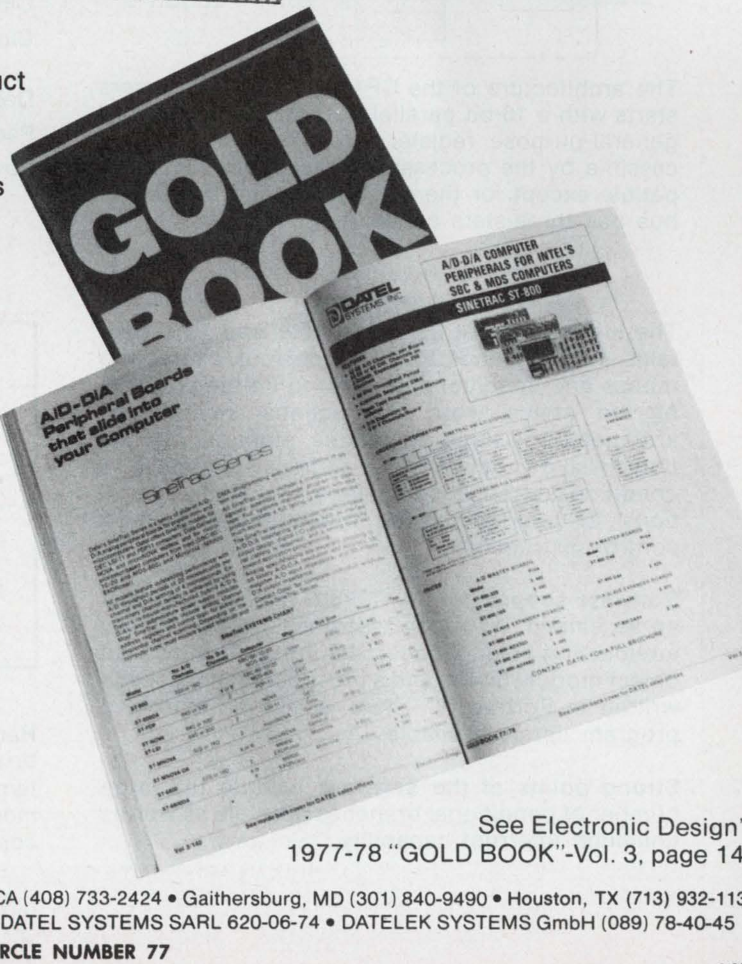


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CIRCLE NUMBER 77

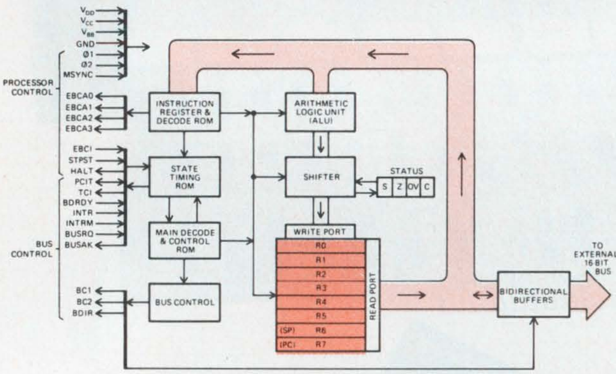
# 16-bit microprocessor, NMOS

## CP1600, CP1610

**General Instrument Corp.**
**600 W. John Street**
**Hicksville, NY 11802**
**(516) 733-3000**

Alternate sources: EM&M Semiconductor and ITT Semiconductor.

The CP1600 and 1610 are 16-bit NMOS microprocessors that use a multiplexed data and address bus. Both circuits are pin and instruction compatible and only differ in package and operating frequency. The 1600 comes in a ceramic DIP and operates at clock frequencies to 5 MHz, while the 1610 comes in a plastic DIP and operates to 2 MHz. Either processor can do conditional branching on status word or 16 external conditions as well as handle almost unlimited program interrupts and DMA requests.




The architecture of the CP1600 family processors starts with a 16-bit parallel ALU and an eight-word general-purpose register file that is directly accessible by the processor. All lines are TTL compatible except for the clock lines, and the 16-line bus has three-state capability.

## Specifications

| | |
|---|---|
| Data word size: | 16 bits |
| Address bus size: | 16 bits |
| Direct addressing range: | 65,536 words |
| Instruction word size: | 10 bits |
| Number of basic instructions: | 87 |
| Shortest instruction/time (Control group): | 1.6 μs (5 MHz) |
| Longest instruction/time (Jump group): | 4.8 μs (5 MHz) |
| Clock frequency (min/max): | Dc/5 MHz |
| Clock phases/voltage swing: | 2/10 V (nominal) |
| Dedicated I/O control lines: | 10 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/12 mA |
| | 12 V/70 mA |
| | −3 V/0.2 mA |

## Comments

**The instruction set** for the CP1600 and 1610 contains 87 commands that provide four addressing modes and conditional branching on the contents of the status word. Instructions include: 20 arithmetic and logic operations, eight I/O instructions (also including all four addressing modes), 18 conditional branch commands, six Jump operations, 28 internal register operations and seven control instructions.

**Software support** for the CP1600 family consists of an assembler, a "super assembler," a text editor, a relocating linking loader, diagnostic routines, an object module linker, and a cross software package written in Fortran IV. There is also an extensive program library available.

**Strong points of the software** include the large number of conditional branches possible as well as unlimited interrupt capability.

## Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| CP1600 | 16-bit CPU, 3.3 MHz | $38.50* |
| CP1600A | 16-bit CPU, 5 MHz | N/A |
| CP1610 | 16-bit CPU, 2 MHz | $8.00 |
| DAC1610 | Dual d/a converter | 4.00 |
| IOB1610 | Input/output buffer | 4.60 |
| MUX1610 | 18-channel analog mux | 2.95 |
| RO-3-5120 | 512×10 bit ROM | 8.17* |
| RO-3-20480 | 2048×10 bit ROM | 16.50 |
| | * 1000 qty price | |

**Hardware support** consists of a wide array of circuit boards, cage assemblies and even complete systems. Memory, interface, I/O, CPU and console modules are available for the Gimini microcomputer.

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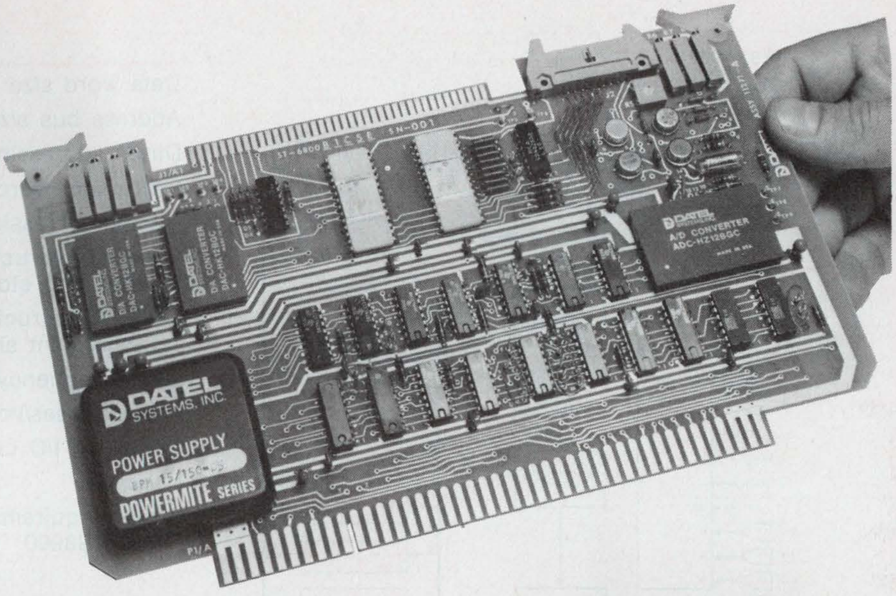


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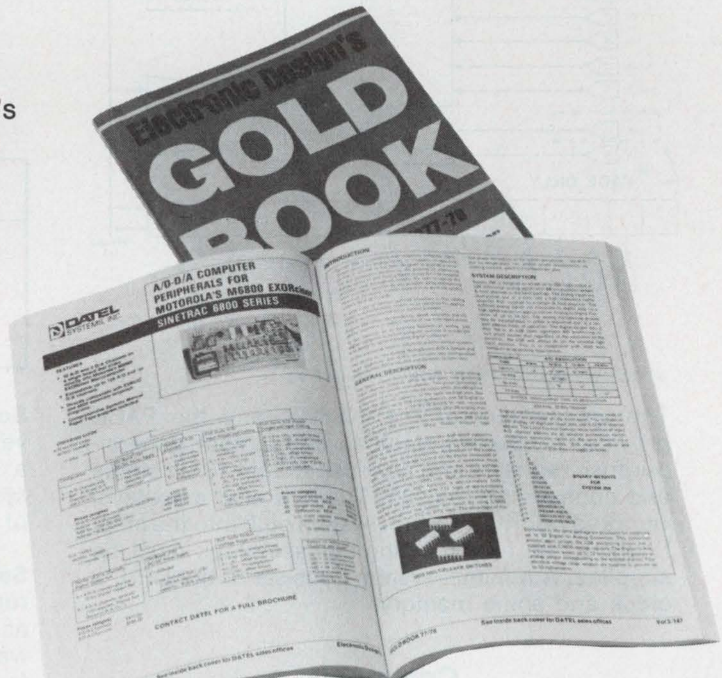


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CIRCLE NUMBER 78

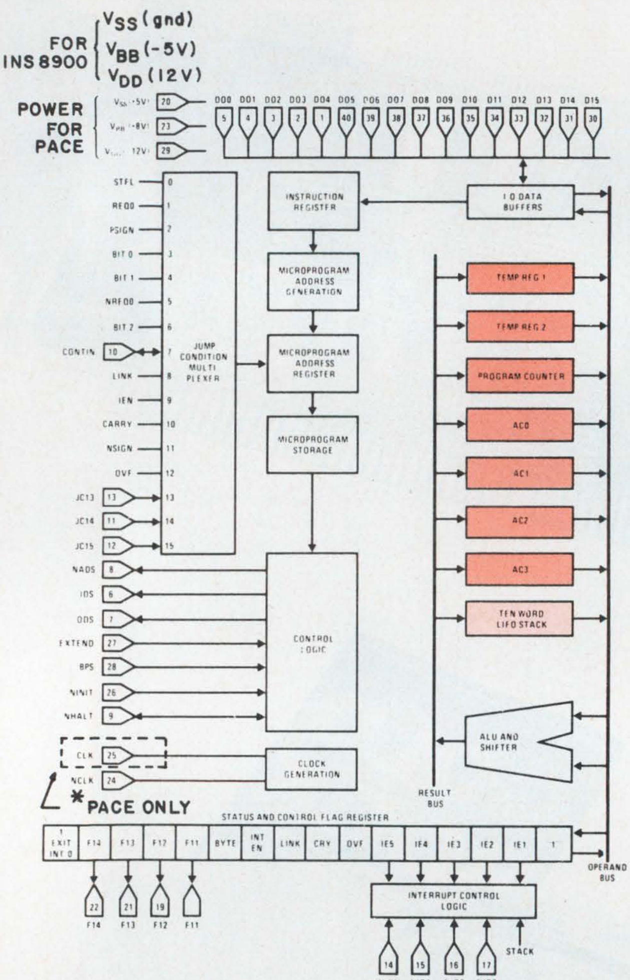
# 16-bit microprocessor, NMOS or PMOS

## INS8900 (successor to PACE)

**National Semiconductor**
**2900 Semiconductor Dr.**
**Santa Clara, CA 95051**
**(408) 737-5000**

Alternate sources: None.

Architecturally similar to the PACE PMOS microprocessor, the INS8900 is intended to supersede the PACE. The 16-bit word size and flexible instruction set give the processor minicomputer-like computational power. Features include an on-chip 10 word stack, indirect addressing, a choice of 8 or 16-bit word operation and memory-mapped I/O.




✱ ON INS 8900 THIS PIN IS $V_{CC}$(5V)

The architecture of the INS8900 and the PACE provides a 10-word stack as well as four general-purpose registers and an independent 16-bit status and control flag register. There is also a six-level vectored priority interrupt system built into the chip. However, an external single-phase clock must be supplied. A minimal system consists of the CPU, a clock and some memory.

### Comments

**The instruction set** of the INS8900 contains 45 commands that can be divided into 12 arithmetic and logic operations, 10 memory reference commands, 13 branch and skip instructions and 10 register operations.

### Specifications

| | |
|---|---|
| Data word size: | 8 or 16 bits |
| Address bus size: | 16 bits |
| Direct addressing range: | 65,536 |
| Instruction word size: | 8 or 16 bits |
| Number of basic instructions: | 45 |
| Shortest instruction/time (Load and store): | 8 μs |
| Longest instruction/time (Decrement and skip if zero): | 16 μs |
| Clock frequency (min/max): | 1.5/2 MHz |
| Clock phases/voltage swing: | 1/12 V |
| Dedicated I/O control lines: | 7 |
| Package: | 40 |
| Power requirements: for INS8900 | 5 V/10 mA |
| | 12 V/50 mA |
| | −5 V/0.2 mA |
| for PACE: | −12 V/40 mA |
| | −8 V/0.1 mA |
| | 5 V/85 μA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| INS8900 | Microprocessor | $19.95 |
| PACE | Microprocessor | 19.95 |
| | There are no specially designed interface circuits. | |

**Software support** for the INS8900 includes conversational assemblers, a Fortran cross assembler, a Basic interpreter and a floppy-disc operating system. There is also a user's group that has a library of over 50 programs.

**Software features** include multilevel priority interrupts, four separate flag outputs, three jump inputs and simple stack manipulation commands. Software also determines whether the processor performs the operations on either 8 or 16-bit data.

**Hardware support** for the INS8900 includes CPU card, a floppy-disc operating system, a low-cost development system and an in-circuit emulator to simplify hardware debugging.

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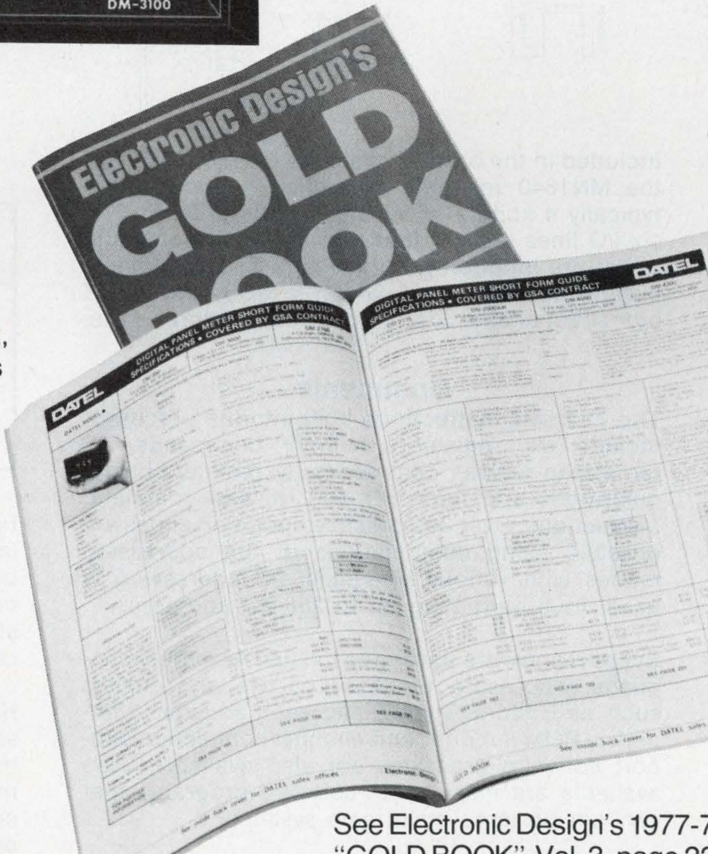


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**CIRCLE NUMBER 79**

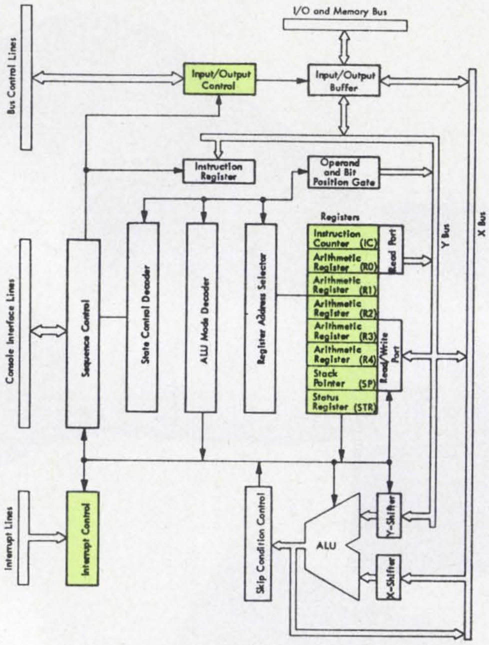
# 16-bit microprocessor, NMOS

## MN1610

**Panafacom**
**6-17-15 Shinbashi Minatoku**
**Tokyo, Japan**
**03-438-0311**

Alternate sources: None.

A high-speed 16-bit parallel processor, the MN1610 has 33 basic instructions. Also included are five arithmetic registers, two of which may be used as index registers. The processor has six addressing modes, a three-level multi-interrupt control, and a bus priority control function for DMA.




### Specifications

| | |
|---|---|
| Data word size: | 16 bits |
| Address bus size: | 16 bits |
| Direct addressing range: | 65,536 words |
| Instruction word size: | 16 bits |
| Number of basic instructions: | 33 |
| Shortest instruction/time (Add): | 3 μs |
| Longest instruction/time (Increment memory and skip): | 12 μs |
| Clock frequency (min/max): | 100 kHz/2 MHz |
| Clock phases/voltage swing: | 2/12 V |
| Dedicated I/O control lines: | 6 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/60 mA |
| | 12 V/55 mA |
| | −3 V/200 mA |

Included in the basic chip set are the MN1610 CPU, the MN1640 real-time controller, and memory—typically 4 kbits of RAM and 8 kbits of ROM. The six I/O lines include four that are output-only and 2 that are input-only. All lines are TTL compatible except the clock input, which is MOS, and the 16 bidirectional data/address bus lines are three-state.

### Comments

**The 33 basic instructions** built into the processor include six register-to-memory commands, 12 register-to-register commands, 12 register change operations and three I/O and register command instructions. Over 345 possible operation codes are possible using combinations of the addressing modes with various operands. I/O addressing is used, thus permitting up to 256 I/O addresses.

**Support software packages** include Assembler language processors, Linkage Loaders, and utilities such as Editors, Tracer, and self-debugger. Simulator, ROM support, and channel connection support software programs are also available. Also available are many cross-software programs that can run on large mainframe systems.

**Software features** include five addressing modes that provide the processors with a flexible programming structure. There are also three levels of multiple interrupt possible by using information held in the program status word. The register to register operations permit many byte manipulation and byte comparison operations. And, bit manipulation instructions permit individual bits in a word to be set, reset or tested.

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| MN1610 | CPU | $35.00 |
| MN1630 | 8-bit subchannel adapter | 15.00 |
| MN1640 | Real-time controller | 15.00 |
| MN1650 | DMA channel controller | 20.00 |

**Hardware support** for the MN1610 ranges from small circuit cards that contain the processor, memory and I/O functions to full blown minicomputer-like systems with front panels and complete machine control. Also available are memory cards, I/O cards, Process control cards, and DMA control cards. The complete system with programmers panel, the L-16A, is available in a 6 or 12-card cabinet.

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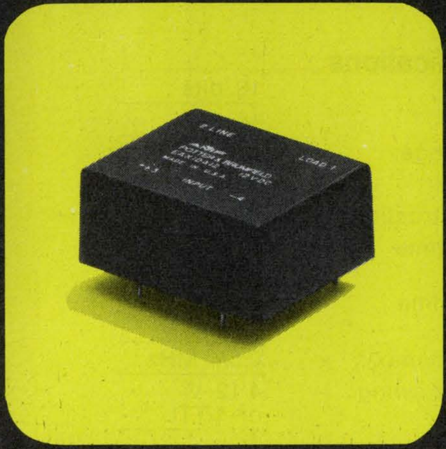

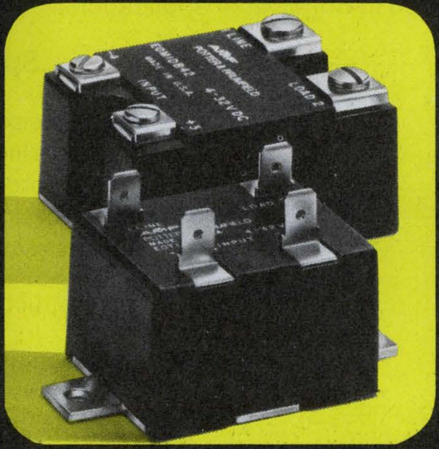

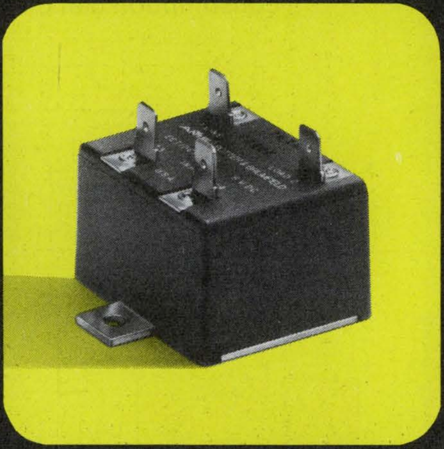

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Expected life greater than 100 million operations. Temp. range: storage, −40°C to +85°C. Operating ambient, −10°C to +55°C.

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Expected life greater than 10 million operations. Operating ambient, −10°C to +55°C.

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CIRCLE NUMBER 80

# 16-bit microprocessor, NMOS
# 16-bit microprocessor, I²L (bipolar)

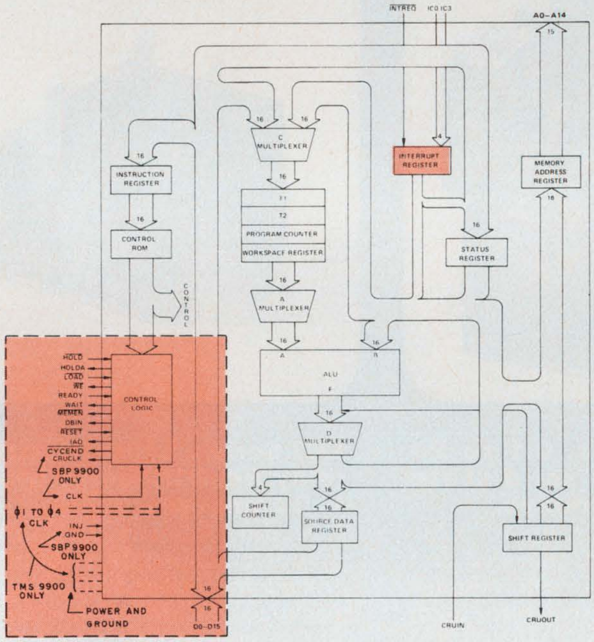
**For NMOS version:**
**Texas Instruments**
**P.O. Box 1443, MS-653**
**Houston, TX 77001**
**(713) 494-5115**

**For I²L version:**
**Texas Instruments**
**P.O. Box 5012, MS-308**
**Dallas, TX 75222**
**(214) 238-2011**

## TMS-9900/SBP-9900

Alternate sources: American Microsystems for the TMS-9900, none for the SBP-9900.

Both the TMS-9900 and SBP-9900 are 16-bit microprocessors with separate data and address buses. The TMS version is a silicon-gate NMOS device that can operate at speeds of up to 3 MHz and requires a four-phase clock input. It's twin, the SBP unit, is an I²L equivalent that can operate at 2 MHz clock rates, but it requires just a single-phase clock input. The I²L unit also permits the supply current to be adjusted so that power consumption can be reduced in noncritical applications.




The 16-bit memory-to-memory architecture of the 9900 μPs permits flexible register files to be set up in memory. A minimal system consists of the CPU, a clock generator and the necessary memory.

### Specifications

| | |
|---|---|
| Data word size: | 16 bits |
| Address bus size: | 15 bits |
| Direct addressing range: | 32,768 words |
| Instruction word size: | 16 to 48 bits |
| Number of basic instructions: | 69 |
| Shortest instruction/time (Branch): | 2 μs |
| Longest instruction/time (Divide): | 31 μs |
| Clock frequency (min/max): | 0.5/4 MHz |
| Clock phases/voltage swing: | 4/12 V or 1/TTL |
| Dedicated I/O control lines: | 3 |
| Package: | 64-pin DIP |
| Power requirements: | 5 V/75 mA |
| | −5 V/0.1 mA |
| | 12 V/40 mA |
| | or variable for I²L version |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| TMS9900 | 16-bit CPU (NMOS) | $70.58 |
| SBP9900 | EJ version (−40 to +84) C range) | 193.00 |
| SBP9900 | MJ version (−55 to +125 C range) | 386.00 |
| SBP9900 | NJ version (MIL 883) | 424.60 |
| TMS9901 | Programmable interface | 8.75 |
| TMS9902 | Asynchronous interface | 7.50 |
| TMS9904 | Clock driver | 5.42 |

### Comments

**The minicomputer-like instruction** set of 69 commands provides 26 arithmetic, logic and data manipulation instructions; 14 internal register to memory operations; five data transfer commands; and 24 control functions. Instructions include binary multiply and divide as well as provisions for 16 prioritized interrupts and programmed and DMA I/O capability.

**Support software** for the 9900-series μPs includes assemblers, editors, simulators, debuggers and high-level languages such as PL/9900, Basic and Fortran. There is also a program library available since all software is code compatible with the larger 990 minicomputer systems.

**The most outstanding features** of the software include the multiple register file capability and the flexibility offered by the dual bus structure. The processors use addressed I/O and has three software controlled lines—a Hold/Hold Acknowledge, a Ready/Wait, and an Interrupt line.

**Hardware support** for the processors includes a series of 990 modules containing central processor cards and memory cards, the PX990 cassette-based development system and AMPL, a floppy-disc based software and hardware development system.

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CIRCLE NUMBER 81

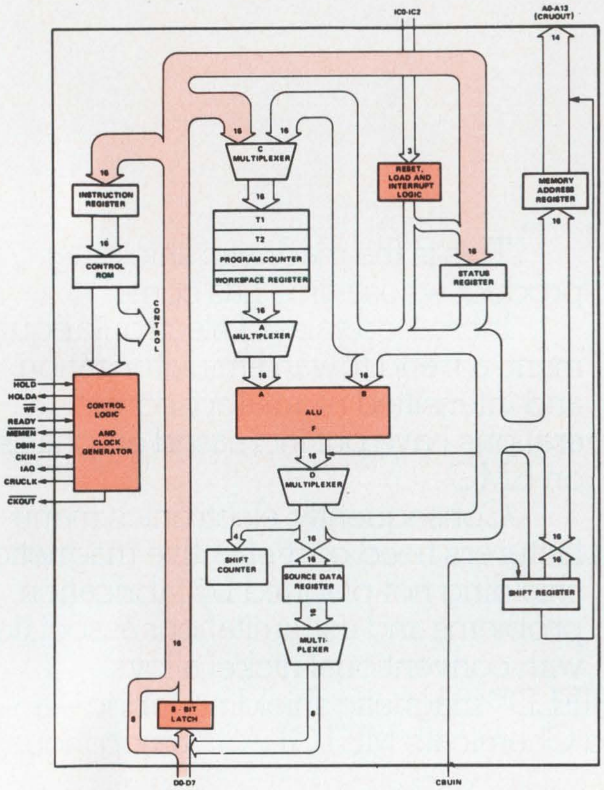
# 16-bit microprocessor, NMOS

## TMS 9980

**Texas Instruments Inc.**
**P.O. Box 5012, M/S 308**
**Dallas, TX 75222**
**(214) 238-2011**

Alternate sources: None.

Software compatible with the TMS 9900 series of microprocessors, the 9980 incorporates a 16-bit CPU with an 8-bit data bus and an on-chip clock in a single 40-pin package. The separate bus structure simplifies system designs, and memory-to-memory architecture features multiple register files, in memory, for faster response to interrupts. Adding memory forms a working minimum system.




The TMS 9980 is almost identical in architecture to the TMS/SBP 9900. The only difference is that the 9980 uses an 8-bit data bus instead of a 16-bit, a 14-bit address bus instead of a 15 bit and has fewer levels of prioritized interrupt. And, the 9980 has its clock generator built onto the same chip .

### Specifications

| | |
|---|---|
| Data word size: | 16 bits* |
| Address bus size: | 14 bits |
| Direct addressing range: | 8192 words |
| Instruction word size: | 16 to 48 bits |
| Number of basic instructions: | 69 |
| Shortest instruction/time (Branch): | 4.8 μs |
| Longest instruction/time (Divide): | 54.4 μs |
| Clock frequency (min/max): | 1 MHz/2.5 MHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | 11 |
| Package: | 40-pin DIP |
| Power requirements: | 12 V/50 mA |
| | 5 V/50 mA |

*Memory is organized in byte format; two sequential bytes form one data word.

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| TMS 9980 | CPU | $30.62 |
| TMS 9901 | Programmable interface | 8.75 |
| TMS 9902 | Asynchronous interface | 7.50 |
| TMS 9905 | 8:1 multiplexer | 1.26 |
| TMS 9906 | 8-bit latch | 1.55 |
| TMS 9907 | 8:3 priority encoder | 1.01 |
| TMS 9908 | 8:3 priority encoder | 1.01 |

### Comments

**The minicomputer-like instruction set** of the TMS 9980 is identical to that of the TMS/SBP 9900 processors. Included are 26 arithmetic, logic and data manipulation instructions, 14 internal register to memory operations, five data transfer commands and 24 control functions. Instructions include binary multiple and divide as well as provisions for four levels of prioritized interrupt. The processor also has programmed DMA and I/O capability.

**Software support** for the TMS 9980 consists of assemblers, editors, simulators, debuggers and high-level languages such as PL/9900, Basic and Fortran. There is also a program library available.

**The most outstanding features** of the software include the multiple register file capability and the flexibility offered by the dual bus structure. The processor uses addressed I/O and has several lines that control I/O operations—the Hold, Hold Acknowledge, Ready, Wait, Interrupt Control and Control Register lines.

**Hardware support** for TMS 9980 development includes all the support for the 9900—the TM 990 microcomputer modules, the PX 990 cassette-based prototyping system and AMPL, a floppy-disc based development system.

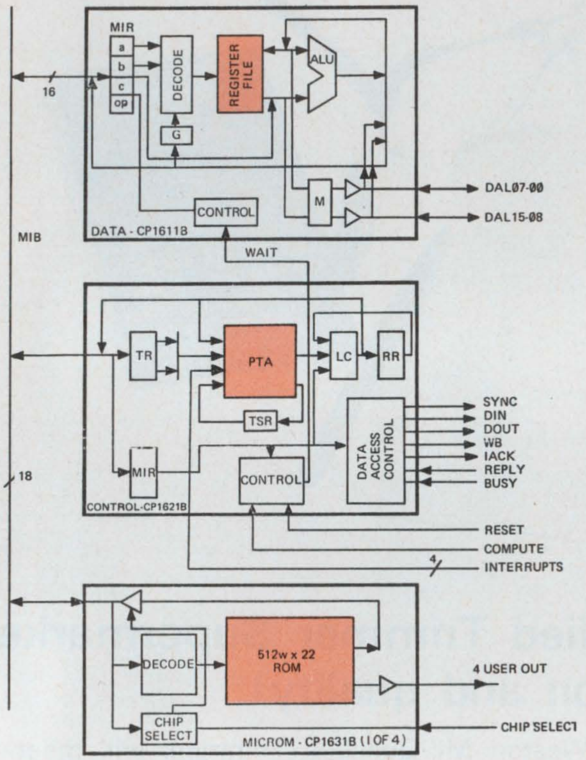
# 16-bit processor set, NMOS

## MCP-1600/WD-16

Alternate sources: None.

**Western Digital Corp.**
**3128 Red Hill Ave., Box 2180**
**Newport Beach, CA 92663**
**(714) 557-3550**

Available as either an unprogrammed chip set (MCP-1600) or as a preprogrammed processor (WD-16), the multiple-chip processor can perform either 8 or 16-bit operations. Both sets consist of a data-processing circuit (CP1611B), a control circuit (CP1621B), and several microprogram-control ROMs (CP1631Bs). The programmed chip set resembles the LSI-11 minicomputer made by Digital Equipment Corp. in both architecture and instruction set.




The basic chip set consists of a data-manipulation chip containing an 8-bit ALU and 26 8-bit registers. The 16 registers can be set up to act as program counter, stack pointer, accumulator and general-purpose 8 or 16-bit registers. A typical minimal system consists of a data chip, a control chip, two to four ROM chips, a clock generator and buffers.

### Specifications

| | |
|---|---|
| Data word size: | 8 or 16 bits |
| Address bus size: | 16 bits |
| Direct addressing range: | 65,536 words |
| Instruction word size: | 2 to 6 bytes |
| Number of basic instructions: | 116* |
| Shortest instruction/time (load condition codes): | 2.1 μs |
| Longest instruction/time (Floating point div.): | 780 μs |
| Clock frequency (min/max): | 2/3.3 MHz |
| Clock phases/voltage swing: | 4/12 V |
| Dedicated I/O control lines: | None |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/50 mA |
| | -5 V/0.5 mA |
| | 12 V/35 mA |

*Or 99 in the programmed version

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| WD-16 | CPU chip set | N/A |
| FD1771 | Floppy-disc controller | $60.00 |
| TR1602 | UART | 7.00 |
| TR1863 | UART (5-V only) | 8.55 |
| BR1941L | Baud-rate generator | 7.50 |
| UC1671 | Astro (mux'd address) | 30.00 |
| UC1971 | Astro (chip select) | N/A |
| TR1953 | USART (Intel 8251 equiv) | 10.00 |
| TR1923 | BOART (async only) | 8.00 |
| SD1933 | Synchronous data-link controller (1 to 9) | 55.00 |
| DM1883 | DMA controller | N/A |
| FR1502 | FIFO buffer (40 x 9) | 16.00 |
| CG1921J | Clock generator (4 φ) | 7.50 |

### Comments

**The WD-16 instruction set** consists of 16 branch commands, 16 register-only operations, five floating-point arithmetic instructions, eight block-move directions, three supervisory commands, 16 single-operand word operations, 16 single-operand byte operations, 12 double-operand instructions word and byte), and eight different addressing modes. There are no dedicated I/O instructions since the processor uses memory-mapped I/O. Software includes vectored interrupts with a 16-bit priority mask, hardware multiply/divide, floating-point arithmetic and up to 16 Mbyte addressing.

**Available software** includes an assembler, editor, simulator, and debugger that are intended to run on a disc-based PDP-11/05 system from DEC. Single-user software, floppy-disc based, without higher-level languages, is available in source form.

**Software features** include hardware register-save/restore, vectored-interrupt overhead consisting of two op codes, and program-counter-relative addressing. Supervisory calls automatically save registers or do a tabled jump. The floating-point format uses an 8-bit exponent and a 40-bit mantissa.

**Prototyping hardware** includes a two-board CPU set that is S-100 bus compatible, as well as a single-board floppy-disc controller (also S-100 bus compatible) that has on-board PROM-based software and a DMA controller. A microprogramming development system consisting of a CPU, writable control store and memory boards is available.

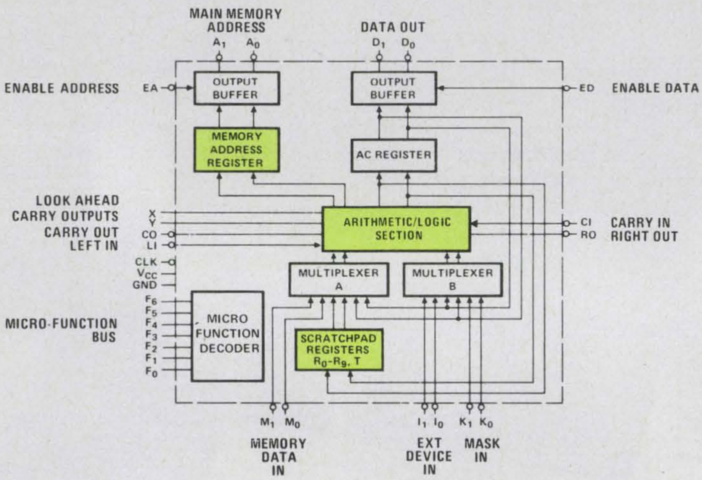
# 2-bit processor slice, Schottky-TTL

## Series 3000

Alternate sources: Signetics.

**Intel Corp.**
**3065 Bower Ave.**
**Santa Clara, CA 95051**
**(408) 246-7501**

The Series 3000 bipolar bit slices are two-bit microprogrammable processor sections that contain a multifunction arithmetic and logic unit, some working registers and the necessary control logic. The processor chip, the 3002, can be cascaded to form an n x 2 bit system. The multiple buses that act as inputs and outputs make the processor readily adaptable to many high-speed controller applications.




A minimal system for the Series 3000 is hard to define since the user determines the processor word length and the amount of microprogram storage needed. A typical 16-bit machine application, though, might require about 25 to 35 devices. The processor's architecture revolves about the ALU and 11 general-purpose registers. All operations are controlled by the function bus, which accepts the microprogram control words and selects both operands and the ALU operation to be performed.

### Specifications

| | |
|---|---|
| Data word size: | 2 bits |
| Address bus size: | On microprogram controller |
| Direct addressing range: | 512 words on 3001 |
| Instruction word size: | 7 bits |
| Number of basic instructions: | Over 40 |
| Basic ALU instruction execution time: | 150 ns |
| Clock frequency (min/max): | Dc/6.67 MHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | User defined |
| Package: | 28-pin DIP |
| Power requirements: | 5 V/190 mA |

### Hardware

| Model | Description | Price (qty.) |
|---|---|---|
| D3002 | 2-bit processor slice | $13.35 |
| D3002M | MIL version of slice | 48.15 |
| D3001 | Microprogram controller | 8.80 |
| D3001 | MIL version | 26.75 |
| D3003 | Look-ahead carry gen. | 6.60 |
| P3212 | Hex buffer | 2.90 |
| P3214 | interrupt controller | 4.65 |
| P3216 | Hex bus driver | 2.75 |
| P3226 | Hex bus driver | 2.75 |

### Comments

**The instruction set** of the 3002 central processing element consists of over 40 Boolean and binary operations, all controlled by the 7-bit input to the function bus. Each 3002 has five independent two-line buses that accept data from external memory (M bus), transfers data from an I/O device (I bus), function as a microprogrammed mask (K bus), act as a memory address bus (A bus) and function as a data bus (D bus).

**Software support** for the Series 3000 consists of CROMIS, a cross microassembler written in Fortran IV and available for use on a 16-bit or larger computer system. There is no general program library available for the family.

**Software features put** the various I/O buses to good use. For instance, output buses A and D often present address and data to external main memory during the same microcycle. Also, operations such as byte swapping can be done in fewer cycles than with other processors by taking advantage of the D and M bus manipulation commands.

**Hardware support** for the series 3000 consists of the Intellec MDS 800 system with the following options: ICE 30, an in-circuit emulator; ROM SIM, a ROM simulator; and a PROM programmer. There is also a chip set available for the designer to begin breadboarding his circuit.

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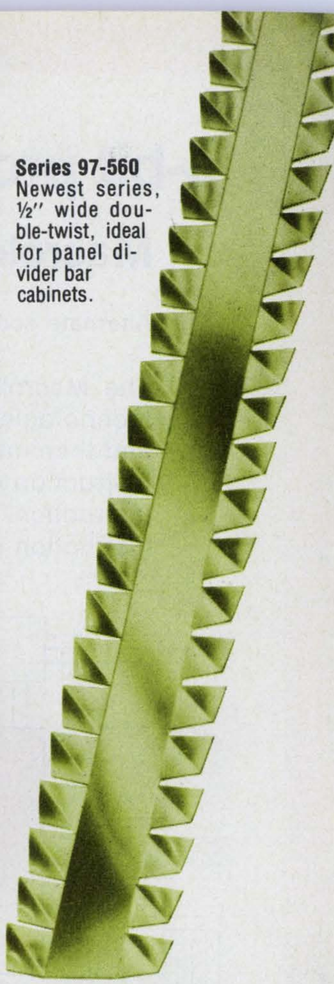

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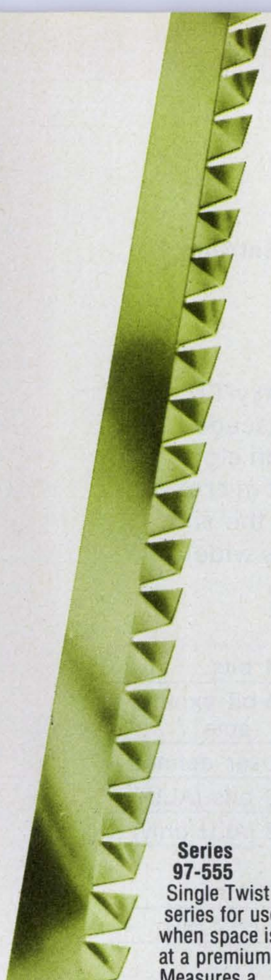

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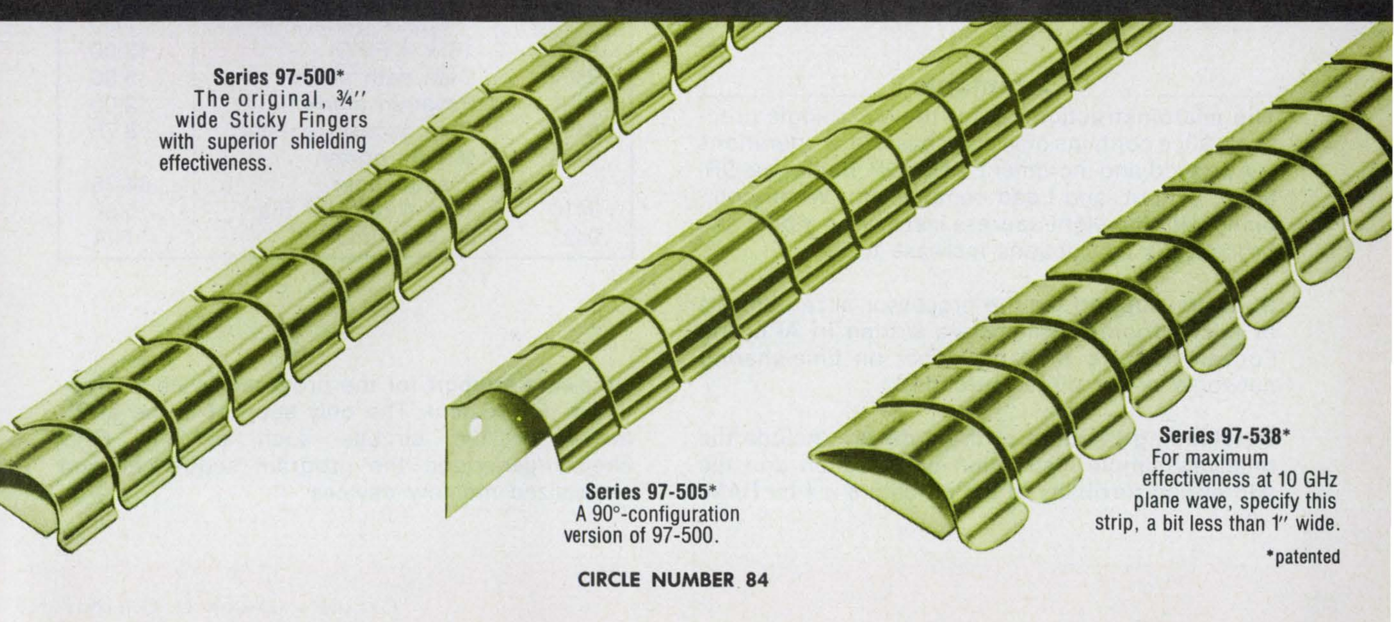

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CIRCLE NUMBER 84

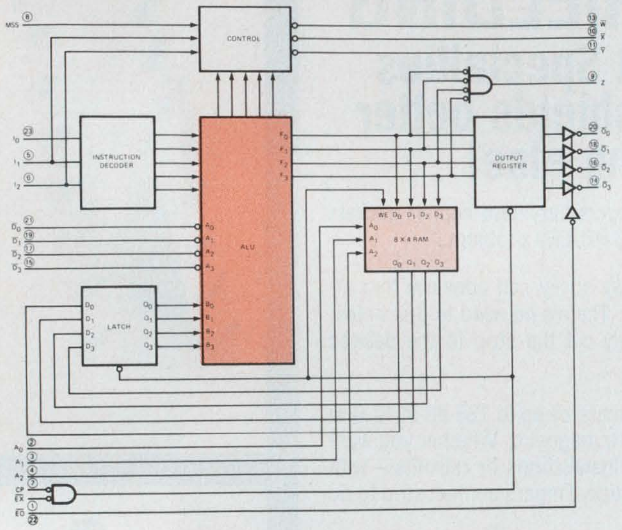
# 4-bit processor slice, CMOS or STTL

## Macrologic (9405A, or 34705)

**Fairchild Camera and Instrument Corp.**
**464 Ellis Street**
**Mountain View, CA 94042**
**(415) 962-3955**

Alternate sources: Signetics.

The Macrologic 4-bit processor slice is available in either CMOS or Schottky-TTL technologies. The ALU sections, 9405A for STTL and 34705 for CMOS, can be cascaded and then microprogrammed to form a complete digital processor. Containing an eight instruction ALU and an 8 × 4 bit RAM bank, the processor slice can operate at micro-instruction rates of 10 MHz. A total of 64 microinstructions are possible via the six instruction code lines. The processor comes in a 24-pin "skinny" DIP (400 mils wide).




### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | 4-bit expandable |
| Direct addressing range: | User defined |
| Instruction word size: | 6 bits (ALU) |
| Number of basic instructions: | 8 (ALU only) |
| Shortest instruction/time (any microinstruction): | 100 ns |
| Clock frequency (min/max): | Dc/12 MHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | User defined |
| Package: | 24-pin DIP |
| Power requirements: | 5 V/160 mA |

The architecture of the Macrologic slices is such that the chips can be cascaded to make an n × 4 bit processor. Carry outputs are provided for carry-lookahead operation and three status signals are also available—accumulator zero, negative or overflow. The four data output lines have three-state capability. A minimal system is hard to define, but a typical organization might use 30 to 50 chips.

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| 9405A | 4-bit processor slice from— | $12.00 |
| 34705 | CMOS version of 9405A | 15.31 |
| 9401 | Cyclic redundancy check generator | 7.80 |
| 9403 | 16 x 4 FIFO | 13.00 |
| 9404 | Data path switch | 3.90 |
| 9406 | Program stack | 12.00 |
| 9407 | Data access register | 8.75 |
| 9408 | Microprogram sequencer | 34.75 |
| 9410 | 16 x 4 register file | 5.50 |
| 9423 | 64 x 4 FIFO | N/A |

### Comments

**The microinstruction set** for the Macrologic processor slice contains only eight basic ALU operations—Add, Add and increment, AND, OR, Exclusive-OR, Load, Output, and Load complement. When combined with the eight address instruction inputs, the processor's instructions increase to 64.

**Software support** for the processor slice consists of microprogram assemblers written in APL and Fortran that are available either on time-sharing networks or for direct purchase.

**Outstanding features of the software** include the relatively simple instruction organization and the addressing flexibility of the on-chip 8 x 4 bit RAM.

**Hardware support** for the processor slice is practically nonexistent. The only support is the availability of the circuits such as the CRC checker/generator, the program sequencer and specialized memory devices.

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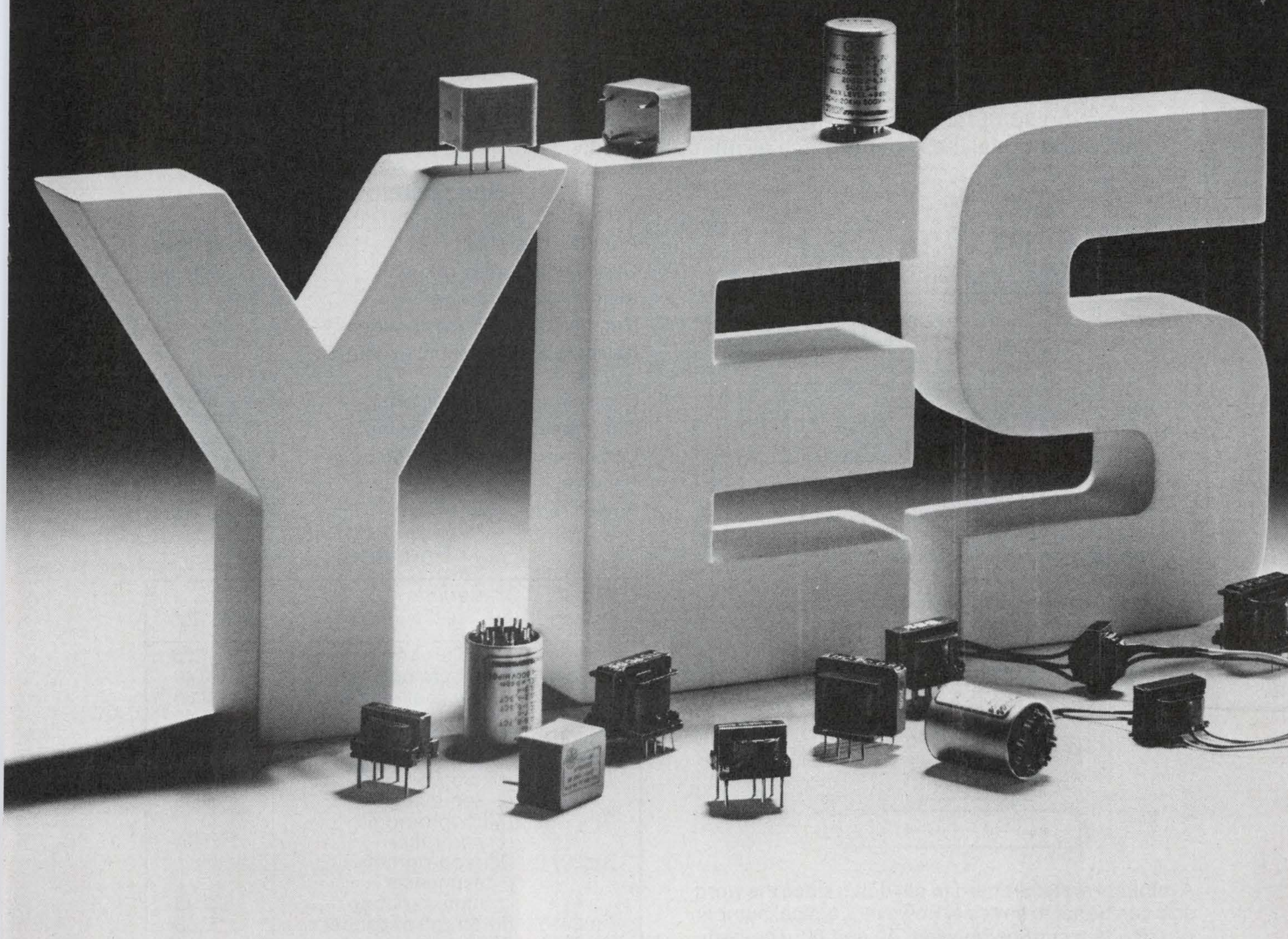


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**CIRCLE NUMBER 85**

**TRW UTC TRANSFORMERS**

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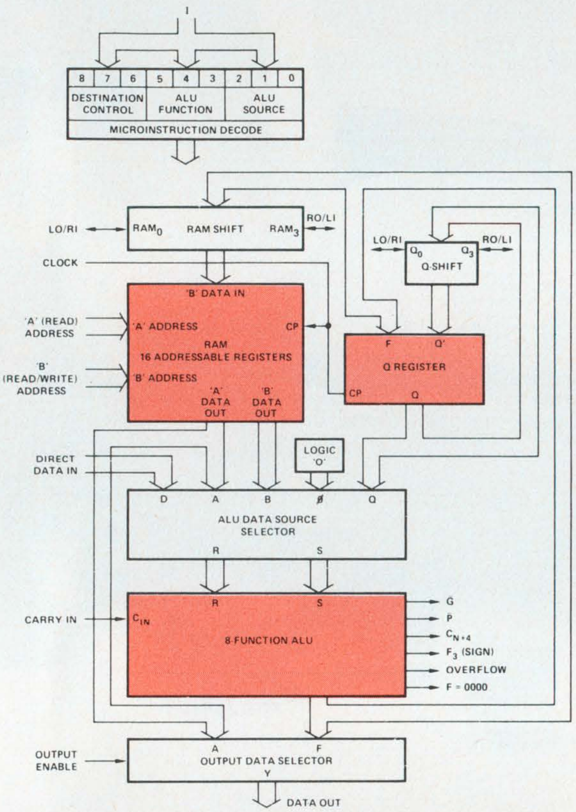
# 4-bit processor slice, Schottky TTL

## Am2901A

Advanced Micro Devices
901 Thompson Place
Sunnyvale, CA 94086
(408) 732-2400

Alternate sources: Fairchild, Monolithic Memories, Motorola, National Semiconductor, Raytheon, Sescosem, and Signetics

The Am2901A has become the "industry standard" 4-bit bipolar processor slice. It consists of a 16 word × 4 bit two-port RAM, a high-speed arithmetic and logic unit and the necessary shifting, decoding and multiplexing circuitry. Any number of 2901A slices can be cascaded to make a processor with a word length of n × 4. There are many support circuits available, and also the widest number of second sources for any bit-slice device. *Coming soon from AMD is an enhanced version of the 4-bit slice, the 2903, which will have additional instructions such as multiply and divide.




A minimal system is hard to pin down since the word size can be set to any size. However a typical number of circuits would be between 40 and 60. The high-speed ALU in the 2901A can perform its operations on two 4-bit input words, one from a two-input multiplexer and the other from a three-input mux.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | User defined |
| Direct addressing range: | User defined |
| Instruction word size: | 9 bits |
| Number of basic instructions: | 8 |
| Basic ALU instruction execution time: | 110 ns typ. |
| Clock frequency (min/max): | dc/15 MHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | 4 flag lines |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/160 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| Am2901A | 4-bit processor slice | $14.70 |
| Am2901A | MIL version | 71.40 |
| Am2902 | Carry look-ahead | 2.65 |
| Am2905 | Bus interface ckt. O.C. | 5.40 |
| Am2906 | Bus interface ckt. O.C. | 7.45 |
| Am2907 | Bus interface ckt. O.C. | 4.75 |
| Am2909 | Microprogram sequencer | 5.95 |
| Am2910 | Microprogram controller | N/A |
| Am2911 | Microprogram sequencer mini version | 3.95 |
| Am2913 | Interrupt expander | 2.53 |
| Am2914 | Vectored interrupt controller | 29.95 |
| Am2918 | One-by-two-port register | 3.08 |
| Am29LS18 | Low power Am2918 | 2.60 |
| Am2919 | Another version, 2918 | 3.10 |
| Am2930, 31 & 32 | Program control units | N/A |
| Am29803 | 16-way branch control | 4.95 |
| Am29811 | Instruction controller | 3.25 |

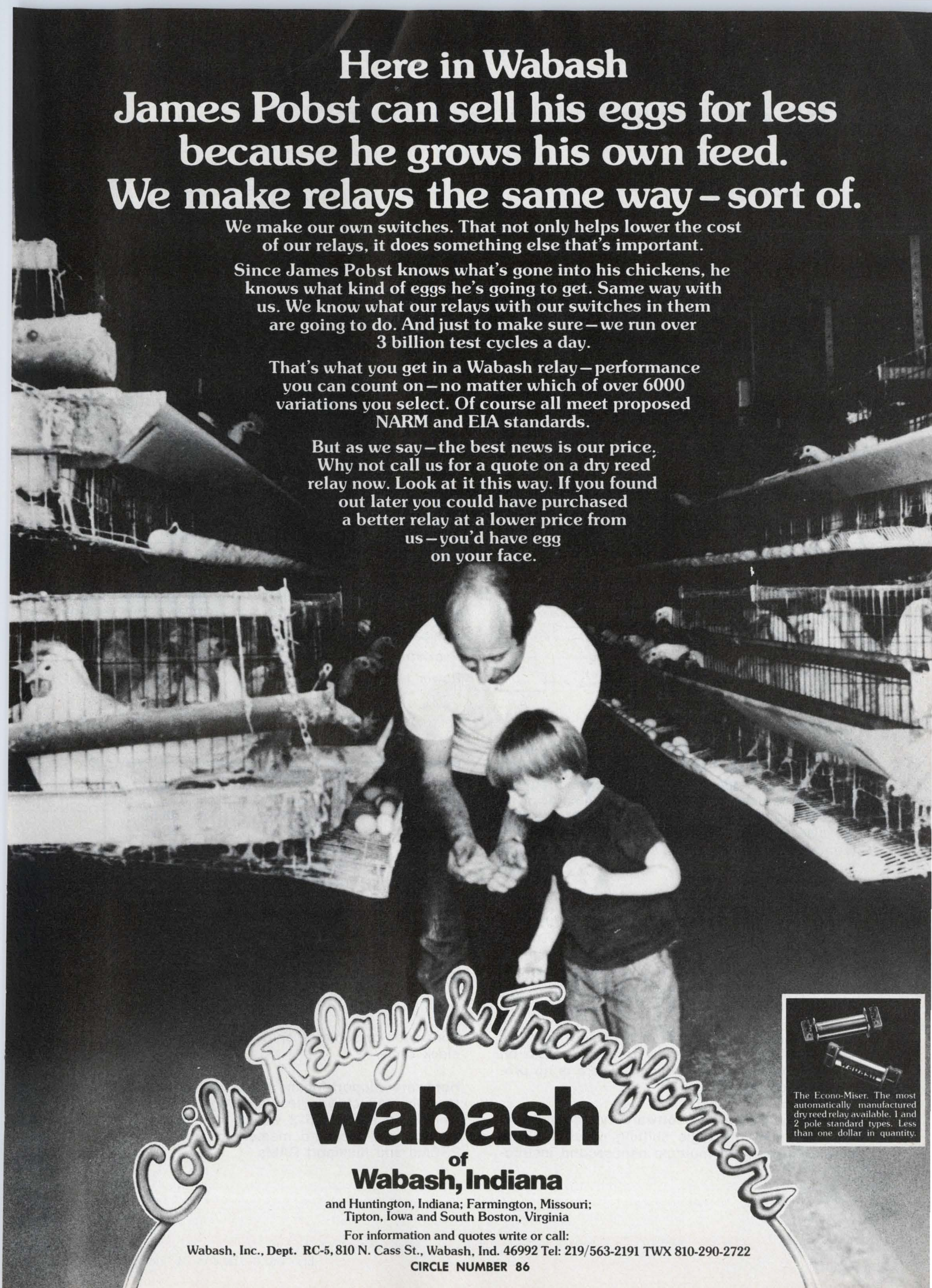
### Comments

**The instruction set** of the 2901A bit slice permits many variations, as determined by the way the nine-bit instruction word is set up. The ALU itself only has eight possible basic operations, but there are also eight source operands and another eight destination codes, for 256 operations.

**Software support** for the 2901A bit slice consists of three programs—AMDASM/TS, a time-shared microprogram assembler; AMDASM/80, a microprogram assembler that can run on the Intel Microprocessor development system; and AMDASM/29, a resident assembler for the System 29 microprogram development system made by AMD.

**Software features** include the two register organization of the 2901A, making possible a wide number of instruction combinations. There are four status flags—carry, overflow, zero and sign—that can function as outputs and there is also a left or right shift operation available that is independent of the ALU.

**Development hardware** includes the Am2900K1, a learning and evaluation kit. Also available is the System 29 microprogramming system.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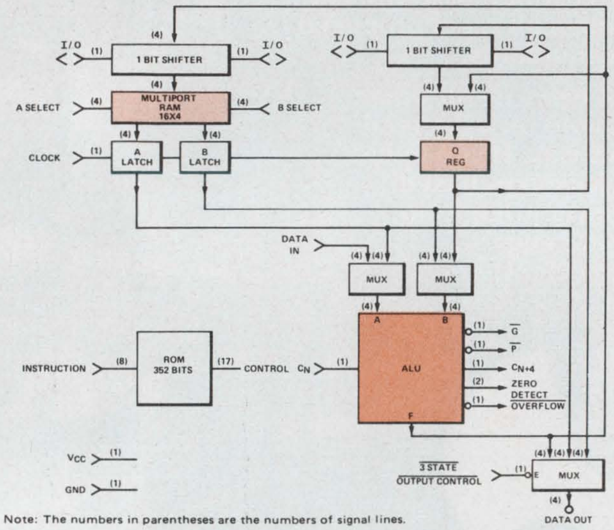
# 4-bit processor slice, bipolar (STTL)

## 5701/6701

**Monolithic Memories, Inc.**
**1165 E. Arques Ave.**
**Sunnyvale, CA 94086**
**(408) 739-3535**

Alternate sources: ITT Semiconductor.

A 4-bit slice of a digital processor on a single chip, the 5701/6701 provides 36 instructions and has 16 directly addressable, two-port accumulators, a separate scratchpad register bank and a 175 ns cycle time. The slices can be cascaded with full carry look-ahead and they have a low fan-in input bus and a three-state output bus.




Note: The numbers in parentheses are the numbers of signal lines.

The architecture of the 5701/6701 bit slice includes a 16 word x 4 bit dual-port RAM as well as a 36 instruction ALU and a single 4-bit working register that can be used as a second accumulator or as an extension to permit an 8-bit result. On the chip are also some microprogrammed ROMs that determine the operation of the ALU for each incoming instruction.

### Comments

**The microprogram instruction set** of the 5701/6701 processor slices contains 36 instructions. The instructions include addition, subtraction, transfer or decrement or increment, AND, OR, Exclusive-OR, Invert and 2's complement, all with various combinations of internal registers.

**Software support** consists of a Fortran IV cross assembler that is designed to run on 16 and 32-bit minicomputers and mainframes. There is no program library available.

**Special features of the software** include overflow detection and the logic shifting capability. The slices can perform multiple nanosecond instructions such as subtract, shift and store in just one clock cycle.

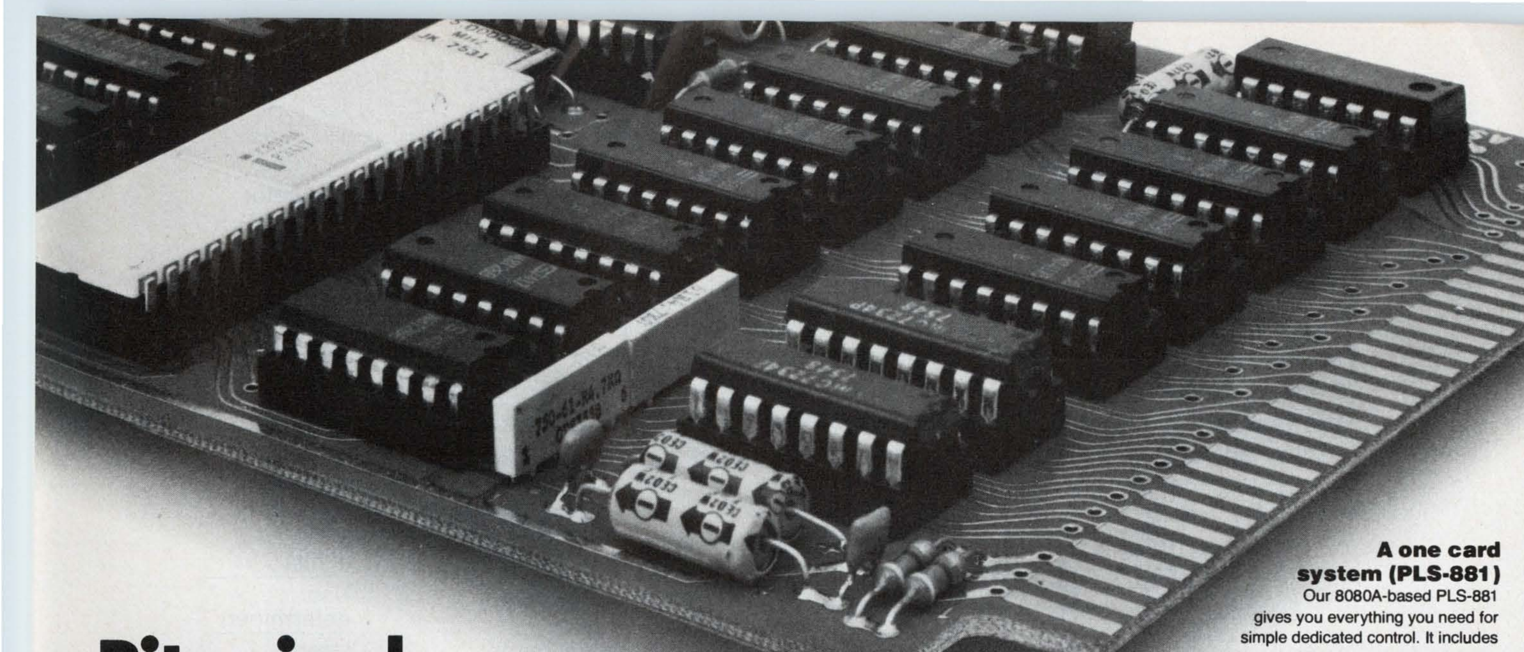
**Hardware support** for the processor is minimal—the only products are the microprogram controller, which can address 512 words of microprogram storage, and standard memory circuits such as PROMs and multiport RAMs.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | User defined |
| Direct addressing range: | User defined |
| Instruction word size: | 8 bits (internal) |
| Number of basic instructions: | 36 |
| Shortest instruction/time (5701 or 6701): | 175 or 230 ns |
| Clock frequency (min/max): | Dc/5.2 MHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | User defined |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/280 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| 5701 | 4-bit slice (MIL) | $ 56.50 |
| 6701 | 4-bit slice (commercial) | 26.15 |
| 57110 | Microprogram controller (MIL version) | 28.00 |
| 67110 | Microprogram controller (commercial version) | 14.00 |



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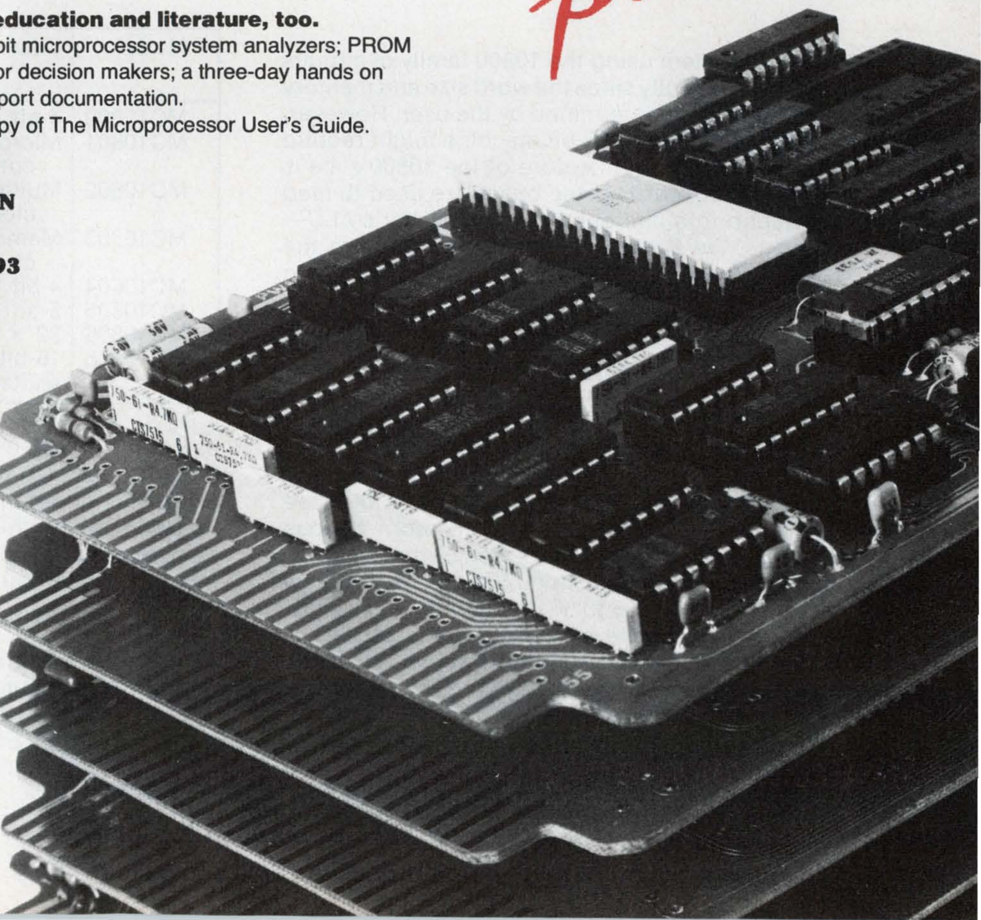


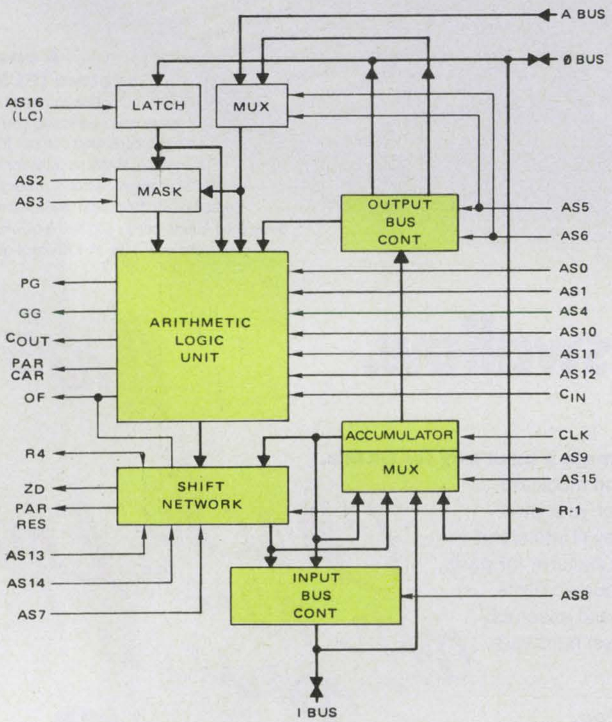
# 4-bit processor slice, ECL

## MC10800

**Motorola Semiconductor**
**5005 E. McDowell Rd.**
**Phoenix, AZ 85036**
**(602) 244-6900**

Alternate sources: None.

The MC10800 family of ECL processor circuits offers the highest speed processing of digital data in LSI form. With a full family of support devices and ECL logic elements, high-performance digital processors with n × 4 bit word lengths can be designed around the family of parts. Most of the devices in the family are housed in a special 48-pin quad in-line package to get the density desired without using large packages.




A minimal system using the 10800 family of circuits is difficult to specify since the word size and memory requirements are determined by the user. However, a typical system for a 16-bit machine might require 25 to 40 devices. Architecture of the 10800 slice is very straightforward. Three buses are used to feed information into and out of the processor's ALU—the A bus, the Ø bus and the I bus—of which the A bus is input only. And, there are no on chip registers aside from the accumulator and latches for the Ø bus, so external registers must be used.

### Comments

**The instruction set** of the 10800 processor chip can perform logic operations, binary arithmetic, and BCD arithmetic on combinations of one, two or three variables. These variables are the A bus, the output bus latch and the accumulator. Various select lines on the processor also control the routing of data within the chip. Simple instructions typically execute in 25 to 50 ns—about twice as fast as the other available bit-slice processors.

**At this time there is no support software** for the 10800 family except for a programming handbook that shows how to develop a microprogram. And, there is no library of user programs yet available.

**The 10800 family of bit slice processors is the only one to include BCD arithmetic capability** as well as normal binary. It also includes a 9's complement circuit to simplify the BCD calculations. The overall instruction set of the 10800 bit slice has so many variations since the 10 basic ALU operations can be performed on combinations of one, two or three inputs, that the total number of possible instructions is more than 1000 variations.

**At this time there are no prototyping systems or program development aids** available for use with the 10800 family. However, boards compatible with the company's EXORciser (the M6800 microprocessor development system) will be available shortly.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | User determined |
| Direct addressing range: | User determined |
| Instruction word size: | User determined |
| Number of basic instructions: | About 10* |
| Basic ALU instruction execution time: | 30 to 50 ns |
| Clock frequency (min/max): | Dc/10 MHz |
| Clock phases/voltage swing: | 2/MECL 10,000 |
| Dedicated I/O control lines: | User determined |
| Package: | 48-pin QUIL |
| Power requirements: | −5.2 V/ 240 mA |
| | −2 V/199 mA |

*for ALU only

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| MC10800 | 4-bit processor slice | $30.00 |
| MC10801 | Microprogram controller | 50.00 |
| MC10802 | Multiphase clock source | 15.00 |
| MC10803 | Memory interface circuit | 40.00 |
| MC10804 | 4-bit ECL/TTL shifter | 4.00 |
| MC10805 | 5-bit ECL/TTL shifter | 4.75 |
| MC10806 | 32 × 9 bit register | 62.00 |
| MC10808 | 16-bit programmable shifter | 25.00 |

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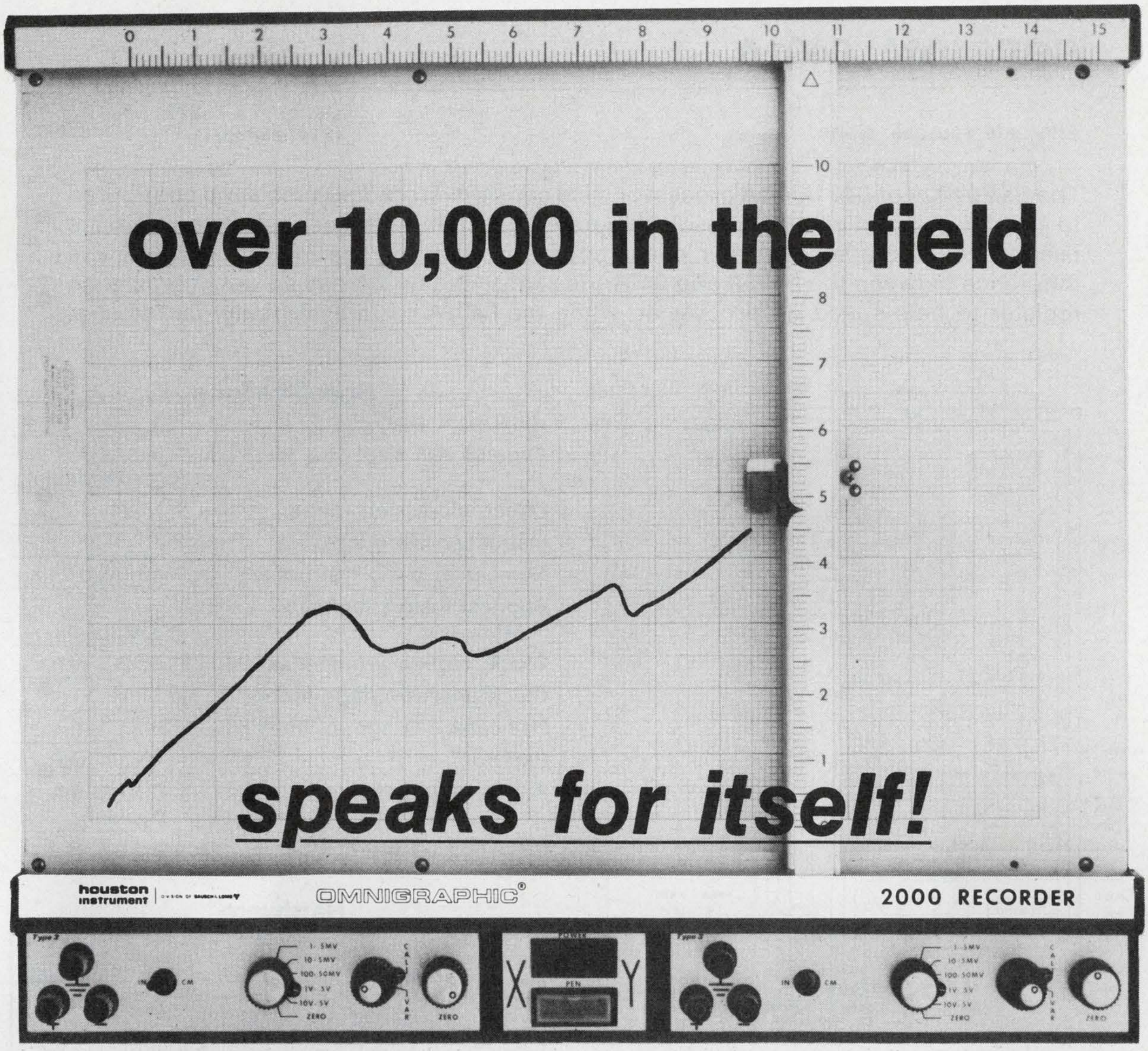


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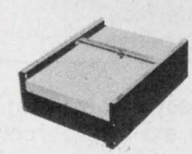
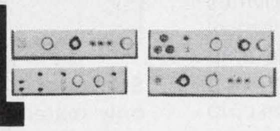
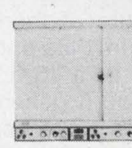
1  +1  = 3 

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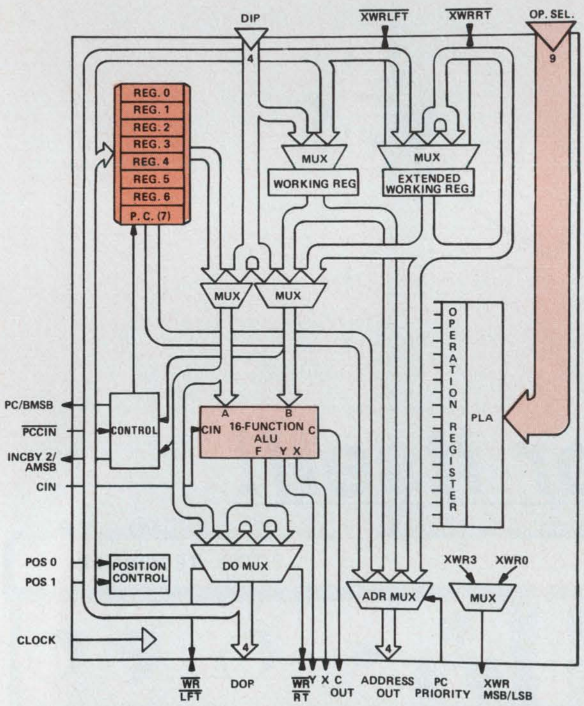
# 4-bit processor slice, bipolar ($I^2L$)

## SBP0400A, 0401A

**Texas Instruments**
**P.O. Box 5012, M/S 308**
**Dallas, TX 75222**
**(214) 238-2011**

Alternate sources: None.

The SBP0400A or 0401A 4-bit processor slice can be microprogrammed and configured to build any size digital processor. Integrated injection logic technology permits the user to define the speed/power consumption by adjusting the injector current. The difference between the 0400A and 0401A is slight—the 0400A has an on-chip pipeline register to help speed up processing while the 0401A requires an external register.




The architecture of the processor slice provides separate data in, data out, address out and control ports, as well as a 16 function ALU. On the chip are an eight-word general register file, two 4-bit working registers, dual scaled-shifters (with on chip handling of end conditions) and a factory programmable logic array that generates on-chip control signals. A minimal system is hard to specify since it depends on word size and control options. A typical system might contain 30 to 50 chips.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size: | 4 bits (expandable) |
| Direct addressing range: | N.A.* |
| Instruction word size: | 13 |
| Number of basic instructions: | 16 (ALU) |
| Shortest instruction/time (All): | 350 ns |
| Clock frequency (min/max): | Dc/3.3 MHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | 5 |
| Package: | 40-pin DIP |
| Power requirements: | 5 V/40 mA (typical) |

*Depends on the number of cascaded slices

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| SBP0400A | 4-bit slice (pipelined) | $14.62 |
| SBP0400A | MIL temp version | 43.85 |
| SBP0401A | 4 bit slice (unpipelined) | 14.62 |
| SBP0401A | MIL version | 43.85 |
| | No special interface circuits are needed | |

### Comments

**The micro-instruction set** of the SBP0400A/0401A can execute any of the 512 possible micro-instructions within a single clock cycle. Operand modifications or combinations via eight arithmetic or logic operations are possible in the ALU as well as combinations of ALU instructions with other commands.

**Software support** is practically nonexistant. The only material available as an aid to programming is the "Bipolar Microcomputer Components Data-Book," in which SBP0400A/0401A programming is explained. There is no program library available.

**Outstanding software features** include the availability of pipelined or unpipelined architecture to suit the design. The slices have an independent program counter with unjammable access controls and a relative position control to define the slice rank in n-bit applications.

**Hardware support** for the SBP0400A/0401A consists of the LCM-1000 series of microprogrammable prototyping modules as well as standard TTL and MOS circuits.

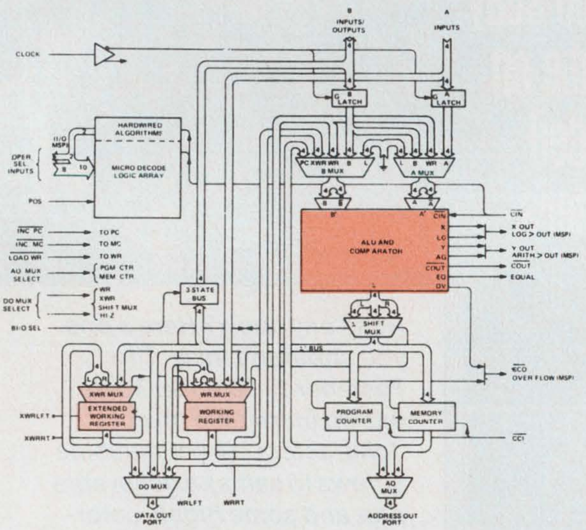
# 4 bit processor slice, bipolar (STTL)

## SN74S481

Alternate sources: None.

**Texas Instruments**
**P.O. Box 5012**
**Dallas, TX 75222**
**(214) 238-2011**

The SN74S481 4-bit microprogrammable processor slice is available in either Schottky-TTL or low-power Schottky-TTL technology. It can be used to build a processor with almost any word size. Both versions have fully parallel I/O ports and memory address ports as well as on-chip circuits that define the slice rank and perform sign-bit protection and fill in.




Architecture features of the 74S481 include fully parallel dual input and output ports, a full function ALU with look-ahead carry, magnitude and overflow decision capabilities, a double-length accumulator and dual memory address generators on chip. A typical system consists of 30 to 50 circuits.

### Comments

**The instruction set** of the processor's ALU consists of only 16 arithmetic and logic commands. But also included in the chip are macroprogrammable multiply and divide algorithms and multidirectional data flow control. There are 24,780 unique operations possible, including automatic CRC update.

**Software support** for the 74S481 family is minimal. There are no programming languages or aids to the designer except for the company's "Bipolar Microcomputer Components Data Book," which describes how to work with the processor slices.

**Important software features** include the preprogrammed multiply and divide operations for double precision signed or unsigned numbers, cyclic redundancy character accumulation instructions to help in error prevention, and simultaneous one clock compound operations.

### Specifications

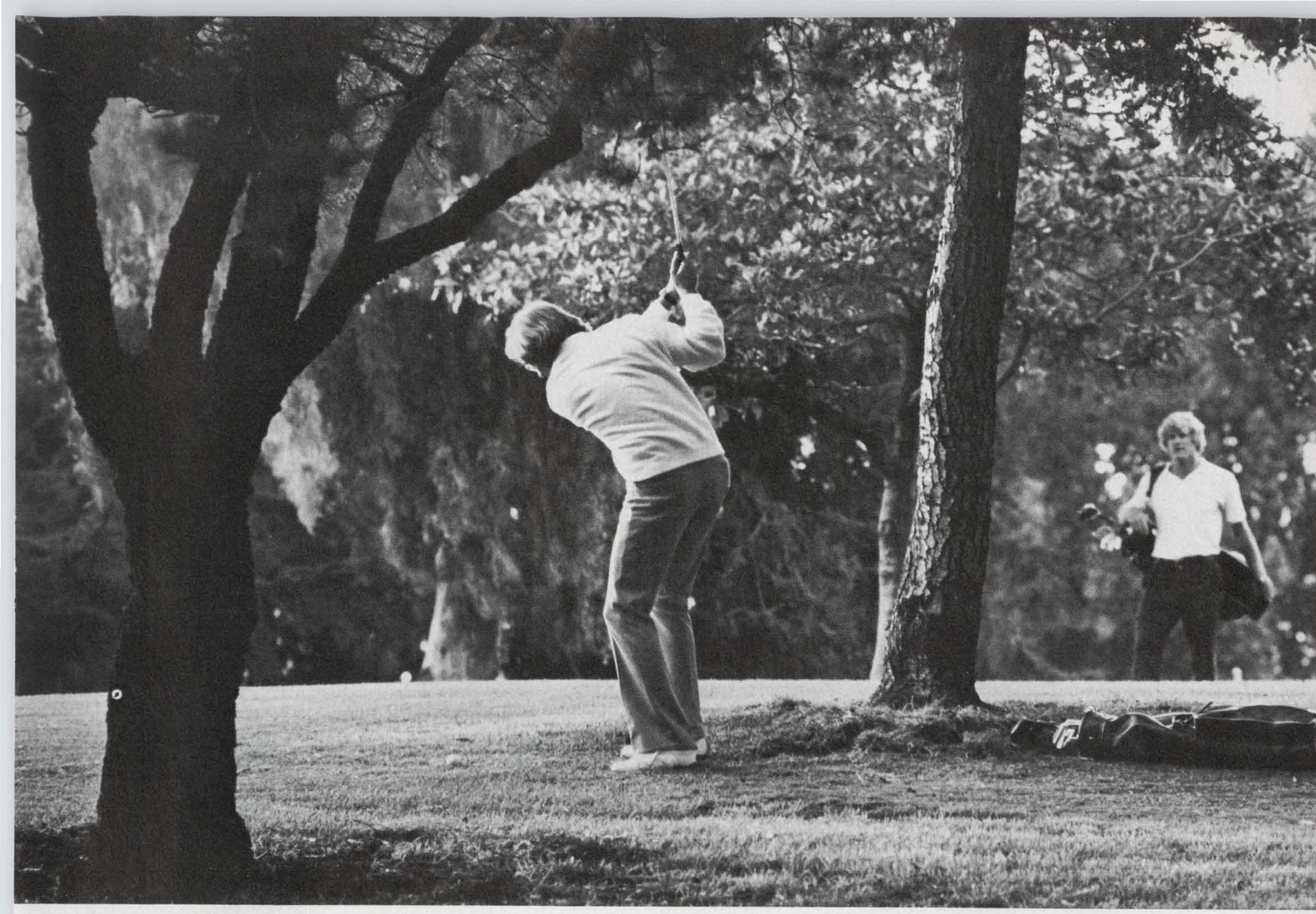
| | |
|---|---|
| Data word size: | 4 bits |
| Address bus size | 4 bits (expandable) |
| Direct addressing range: | N.A.* |
| Instruction word size: | N.A. |
| Number of basic instructions: | 16 (ALU) |
| Shortest instruction/time (microinstruction): | 67 ns |
| Longest instruction/time (signed integer divide): | 200 to 250 ns |
| Clock frequency (min/max): | Dc/15 MHz |
| Clock phases/voltage swing: | 1/TTL |
| Dedicated I/O control lines: | 8 |
| Package: | 48-pin QUIL |
| Power requirements: | 5 V/200 mA |

*Depends on the number of cascaded slices.

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| 74S481 | 4-bit slice (plastic) | $19.60 |
| 74S481 | 4-bit slice (ceramic) | 29.25 |
| 74S481 | 4-bit slice (MIL) | 87.75 |
| SN74S482N | 4-bit controller | 6.30 |
| SN74S330N | 12-In, 50-Term, 6-Out FPLA | 9.00 |
| SN74S225N | 16-word-by-5-bit FIFO | 4.50 |
| SN74S226N | Quad bus transceiver | 2.25 |
| SN74S182N | Carry look-ahead | 2.91 |
| SN74S240N | Octal inv/buffer | 4.20 |
| SN74S241N | Octal buffer/driver | 4.20 |
| SN74S373N | Octal transparent latch | 4.72 |
| SN74S374N | Octal D-type register | 4.72 |

**Hardware support** is minimal at present. In 1978, evaluation processor modules that duplicate the TI 990 minicomputer's instruction set will be available.



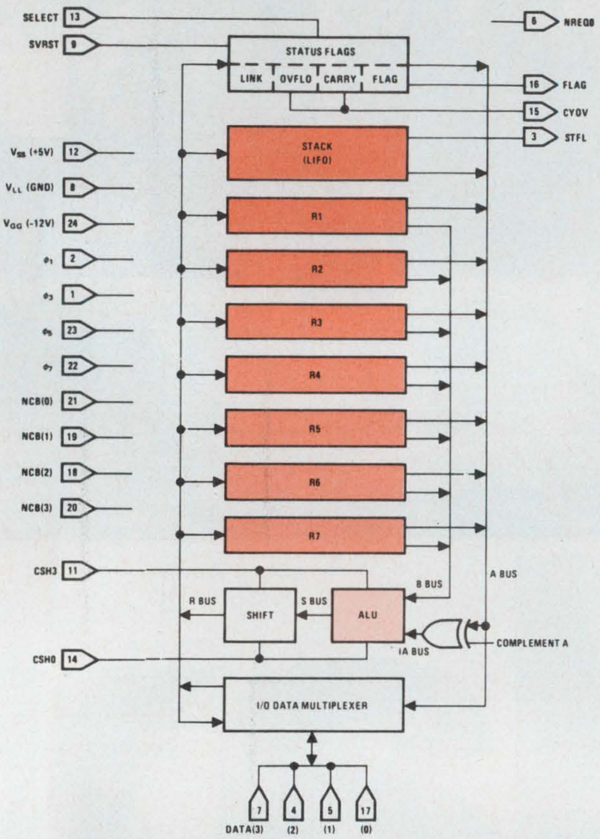
# 4-bit processor slice, PMOS

## IMP-8, 16 (00A/520)

Alternate sources: None.

**National Semiconductor**
**2900 Semiconductor Drive**
**Santa Clara, CA 95051**
**(408) 737-5000**

The IMP series of 4, 8 and 16-bit processors is built around a 4-bit PMOS slice (P/N 00A/520) that can be cascaded. The slice, called a register and arithmetic unit (RALU), combines with control ROM circuits (CROMs) to form a complete microcomputer. Contained in the RALU are a seven-word × 4-bit general register bank, a status register, and a 16-word × 4-bit last-in first-out stack, as well as a multifunction ALU.




The architecture of the IMP processor family is split into three basic chips. On the RALU are all the RAM registers, counters and control logic (including the ALU). The CROM holds the microprogram for the macroinstructions while the interface logic circuit provides the flags, condition-jump controller, program counter and program-counter stack. All circuits interface directly via MOS level buses and require a four-phase nonoverlapping clock.

### Comments

**The macroinstruction set** of the IMP processor slice contains 42 commands including 16 register operations, two flag instructions, 13 memory reference operations, five branch commands and six increment/decrement and I/O instructions. The IMP-16L processor has 17 optional instructions including multiply and divide and bit operations.

**Software support** for the IMP family consists of resident and cross assemblers. Resident software can run on any of the IMP systems since all processors share the same set of commands. The cross software is written in Fortran IV and can run on many 32-bit computers. Also available are diagnostic, loader and debug programs.

**Software features** include the compatibility of instructions from the smaller processors to the largest and the flexibility of defining your own instruction set by the control program in the CROM.

**Hardware support** for the IMP processor family consists of several processor cards built around the RALU and CROMs as well as full microcomputer systems—the IMP-16L or IMP-16P. Memory cards, I/O cards and card cages are available.

### Specifications

| | |
|---|---|
| Data word size: | 4 bits (ALU) |
| Address bus size: | 4, 8 or 16 bits |
| Direct addressing range: | Up to 65,536 words |
| Instruction word size: | 23 bits (CROM) |
| Number of basic instructions: | 42 |
| Shortest instruction/time (nonmemory reference): | 12 μs (average) |
| Longest instruction/time (memory reference): | 20 μs (average) |
| Clock frequency: | 5.17 MHz max. |
| Clock phases/voltage swing: | 4/16 V |
| Dedicated I/O control lines: | 4 |
| Package: | 24-pin DIP (RALU) |
| Power requirements: | 5 V/40 mA<br>−12 V/40 mA |

### Hardware

| Model | Description | Price (100 qty) |
|---|---|---|
| 00A/520 | 4-bit RALU | $22.00 |
| 8A/521D | 8-bit wide control CROM | 40.00 |
| 16A/521D | 16-bit wide control CROM | 27.50 |
| IMP-16A/523D | Power I/O CROM (25-up) | 40.50 |
| IMP-16A/524D | Arithmetic CROM (25-up) | 40.50 |

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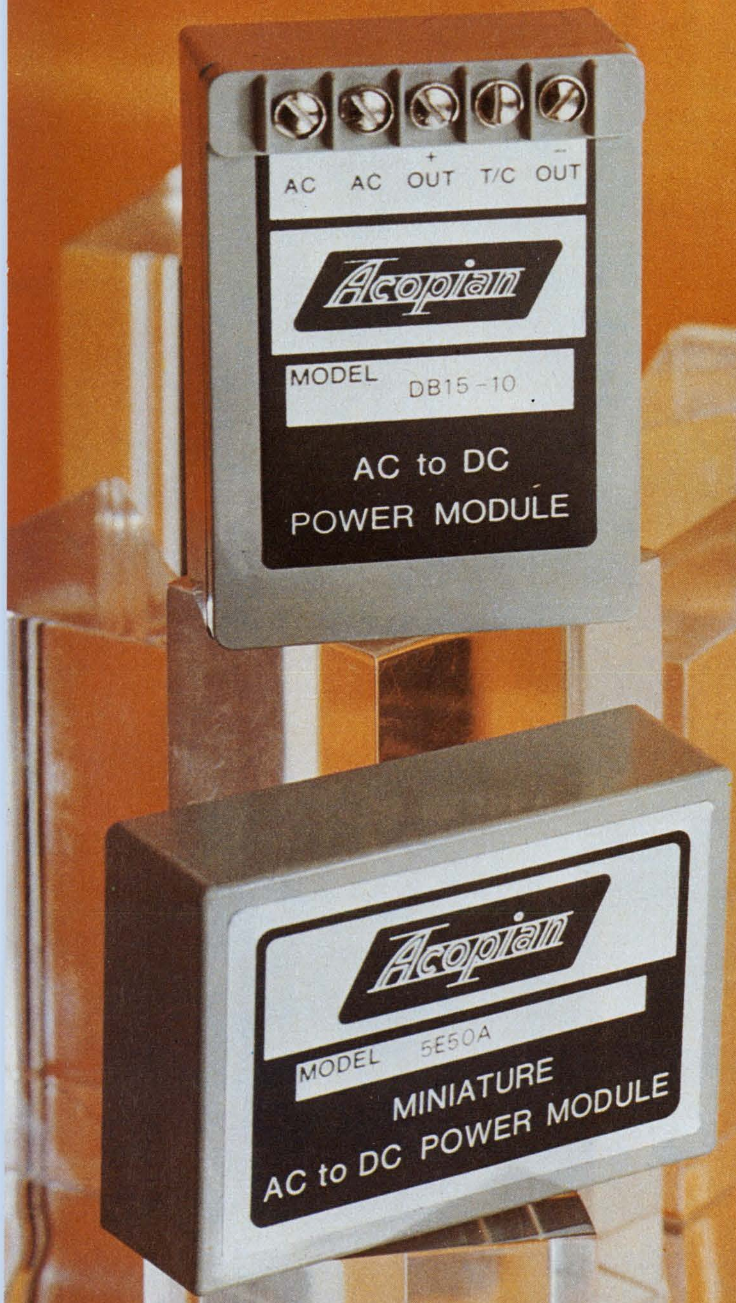


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| 5 | 2.0 | .25 | .05 | 1 | 115 | 5EB200 | EB-20 |
| 5 | 2.5 | .25 | .05 | 1 | 130 | 5EB250 | EB-20 |
| ±12 | .100 | .05 | .05 | 1 | 55 | DB12-10 | EB-10 |
| ±12 | .150 | .05 | .05 | 1 | 65 | DB12-15 | EB-10 |
| ±12 | .200 | .05 | .05 | 1 | 75 | DB12-20 | EB-10 |
| ±12 | .300 | .05 | .05 | 1 | 105 | DB12-30 | EB-13 |
| ±12 | .350 | .05 | .05 | 1 | 110 | DB12-35 | EB-13 |
| ±12 | .500 | .1 | .05 | 1 | 135 | DB12-50 | EB-20 |
| ±15 | .100 | .05 | .05 | 1 | 55 | DB15-10 | EB-10 |
| ±15 | .150 | .05 | .05 | 1 | 65 | DB15-15 | EB-10 |
| ±15 | .200 | .05 | .05 | 1 | 75 | DB15-20 | EB-10 |
| ±15 | .300 | .05 | .05 | 1 | 105 | DB15-30 | EB-13 |
| ±15 | .350 | .05 | .05 | 1 | 110 | DB15-35 | EB-13 |
| ±15 | .500 | .1 | .05 | 1 | 135 | DB15-50 | EB-20 |

**PCB Mounting**

| Nominal Output Voltage | Output Current Amps. | Regulation Load ±% | Regulation Line ±% | Ripple mv RMS | Price | Model | Case Size |
|---|---|---|---|---|---|---|---|
| 5 | .250 | .05 | .05 | 0.5 | $ 39 | 5E25 | ES-10 |
| 5 | .500 | .1 | .05 | 1 | 49 | 5E50A | EL-10 |
| 5 | 1.0 | .2 | .05 | 1 | 69 | 5E100 | EL-13 |
| 5 | 1.5 | .3 | .1 | 1 | 98 | 5E150 | EL-13 |
| 5 | 2.0 | .15 | .05 | 1 | 110 | 5E200 | EL-20 |
| 5 | 2.5 | .15 | .05 | 1 | 125 | 5E250 | EL-20 |
| ±12 | .025 | .1 | .05 | 1 | 24 | D12-03 | ES-10 |
| ±12 | .050 | .1 | .05 | 1 | 39 | D12-05 | ES-10 |
| ±12 | .100 | .05 | .05 | 1 | 49 | D12-10A | EL-10 |
| ±12 | .150 | .05 | .05 | 1 | 59 | D12-15A | EL-10 |
| ±12 | .200 | .05 | .05 | 1 | 69 | D12-20 | EL-10 |
| ±12 | .300 | .05 | .05 | 1 | 98 | D12-30 | EL-13 |
| ±12 | .350 | .05 | .05 | 1 | 105 | D12-35 | EL-13 |
| ±12 | .500 | .1 | .05 | 1 | 130 | D12-50 | EL-20 |
| ±15 | .025 | .1 | .05 | 1 | 24 | D15-03 | ES-10 |
| ±15 | .050 | .1 | .05 | 1 | 39 | D15-05 | ES-10 |
| ±15 | .100 | .05 | .05 | 1 | 49 | D15-10A | EL-10 |
| ±15 | .150 | .05 | .05 | 1 | 59 | D15-15A | EL-10 |
| ±15 | .200 | .05 | .05 | 1 | 69 | D15-20 | EL-10 |
| ±15 | .300 | .05 | .05 | 1 | 98 | D15-30 | EL-13 |
| ±15 | .350 | .05 | .05 | 1 | 105 | D15-35 | EL-13 |
| ±15 | .500 | .1 | .05 | 1 | 130 | D15-50 | EL-20 |

**Input Voltage:** 105-125 Vac, 47 to 420 Hz, single phase.

**Output Voltage Setting:** Single output models are factory preset to within ±2% of nominal output voltage, and may be more precisely trimmed to the nominal voltage rating with an external trim resistor. Dual models are set to within ±1% of their nominal ratings, and are not trimable.

**Polarity:** Either positive or negative terminal of a single output module may be grounded. Dual output modules have a positive/common/negative output terminal configuration.

**Ambient Operating Temperature:** −20 to +71°C. (Model 5E150 and 5EB150, 0 to +71°C.) No derating required.

**Temperature Coefficient:** 5-volt models, .03%/°C; dual output models, .015%/°C.

**Impedance:** 0.07 ohm at 1 kHz, 0.2 ohm at 10 kHz (approx.).

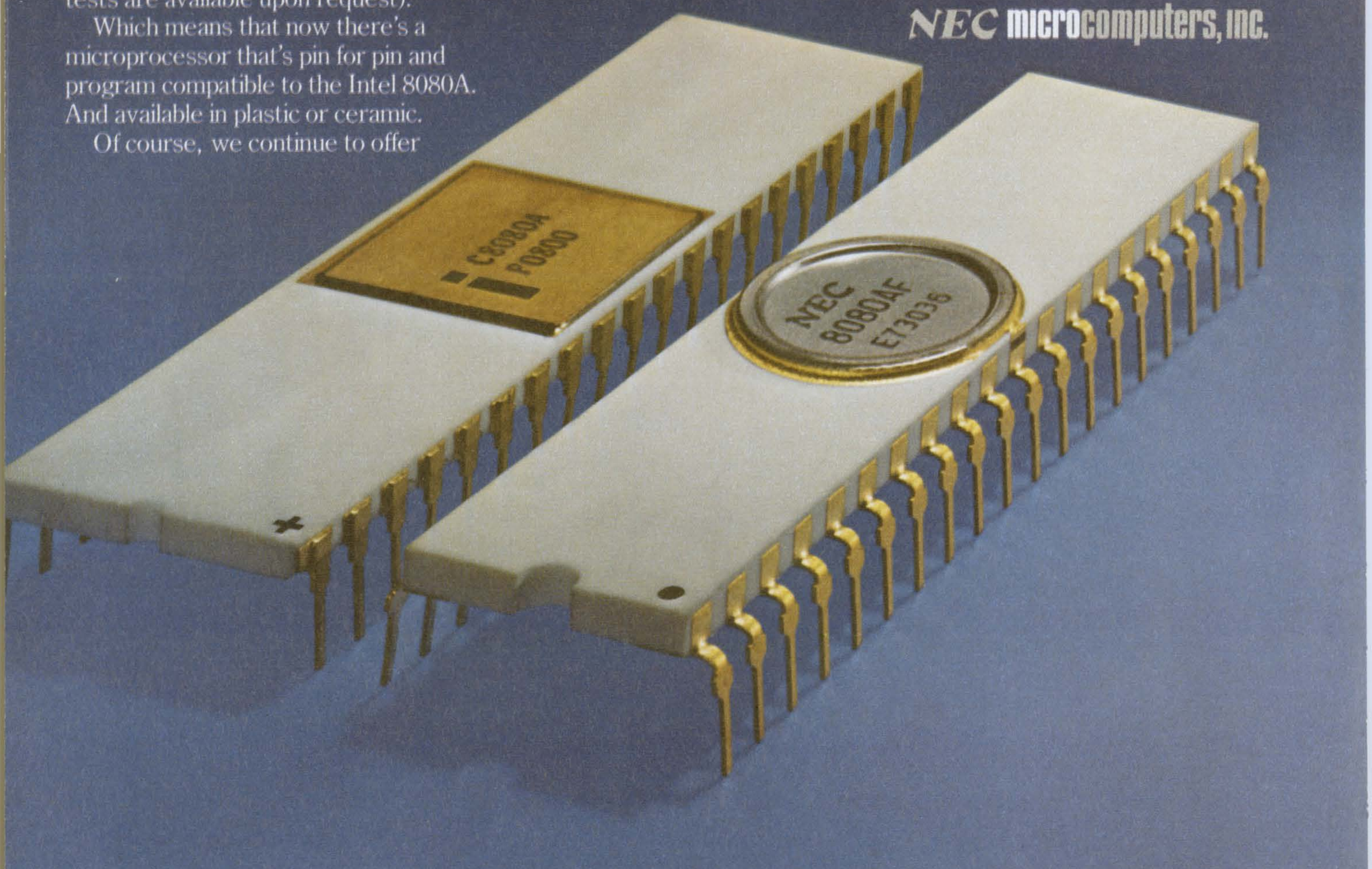
**Optional 230 Volt Input:** To order, add suffix "-230" to model number and $10.00 to price.

**Case Sizes and Weight:**
EB-10: 3.5″ x 2.5″ x 1.375″ (1 lb)
EB-13: 3.5″ x 2.5″ x 1.625″ (1 lb 5 oz)
EB-20: 3.5″ x 2.5″ x 2.375″ (2 lb 1 oz)
EL-10: 3.5″ x 2.5″ x 1″ (15 oz)
EL-13: 3.5″ x 2.5″ x 1.25″ (1 lb 3 oz)
EL-20: 3.5″ x 2.5″ x 2″ (2 lb)
ES-10: 2.3″ x 1.8″ x 1″ (7 oz)

**Other models available from 1 to 75 volts. Send for complete information.**

Acopian Corp., Easton, Pa. 18042 Tel: (215) 258-5441

CIRCLE NUMBER 271



C8080A
P0800
NEC
8080AF
E73036

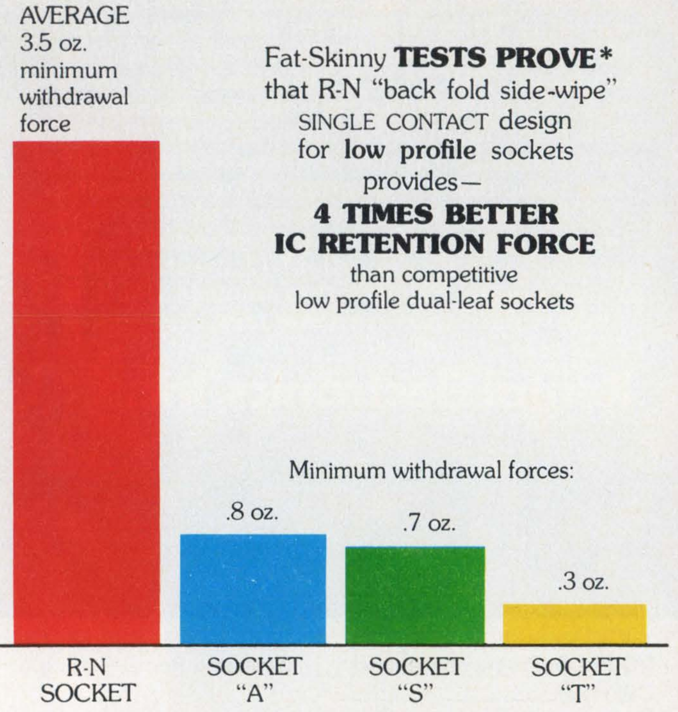
# TEST DATA

## low profile

Fat-Skinny **TESTS PROVE*** that R-N "back fold side-wipe" SINGLE CONTACT design for **low profile** sockets provides—

**4 TIMES BETTER IC RETENTION FORCE**

than competitive low profile dual-leaf sockets




* In "Fat-Skinny test," withdrawal forces are measured using the smallest size (.008") lead **after** insertion of **largest** size (.012") lead.

**Representative NORMAL FORCE Test Scores for 10 R-N ICL low profile sockets**

| TEST SOCKET | NORMAL FORCE * |
|---|---|
| 1 | 410 grams |
| 2 | 465 grams |
| 3 | 480 grams |
| 4 | 465 grams |
| 5 | 395 grams |
| 6 | 425 grams |
| 7 | 465 grams |
| 8 | 395 grams |
| 9 | 410 grams |
| 10 | 425 grams |

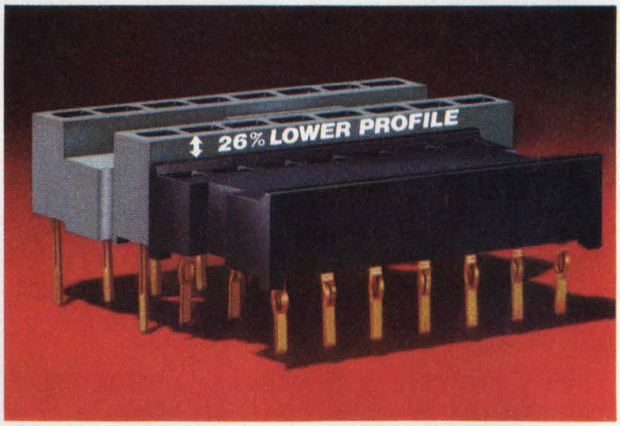
**AVERAGE—430 grams**

**This force is 4 to 5 times greater than average dual contact socket** NORMAL FORCE

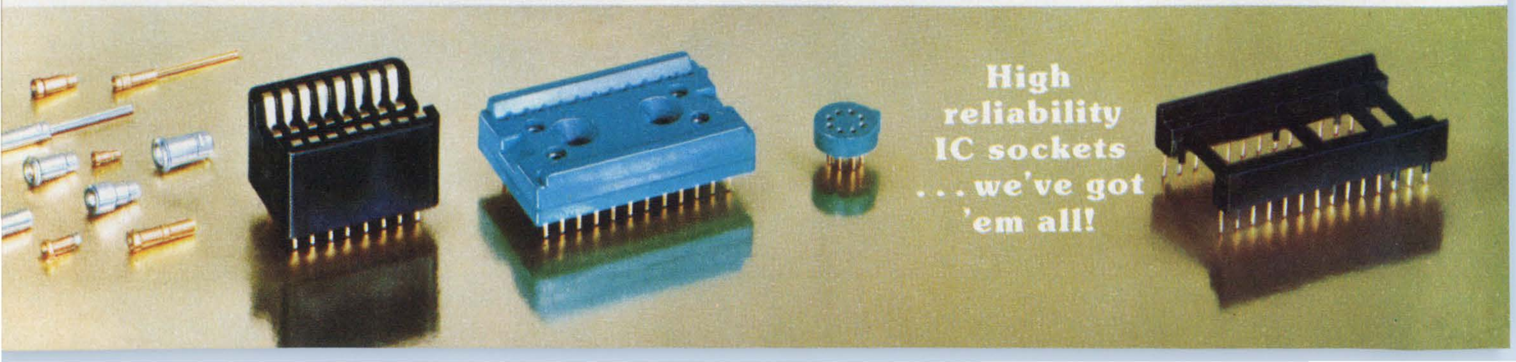
* NORMAL FORCE means force perpendicular or at right angles to IC lead. The single ICL contact exerts this kind of force against the IC lead when inserted into the socket.

## "...TWO contacts are not more reliable than ONE!"

Surprisingly, a **low profile** (.150" high) DIP socket is a different breed of cat when it comes to engineering in contact reliability. Most standard DIP sockets have dual contacts. (R-N's dual "side-wipe" contacts are among the most reliable in the industry.) But, when you **shorten the contact length** to achieve the "low profile" you lose a great deal of contact force and IC retention strength. So, to achieve effective low profile socket reliability you must **redesign the contacts** and make them out of the **strongest contact material available.**




Low .150" profile of ICL socket reduces board density by 26%.



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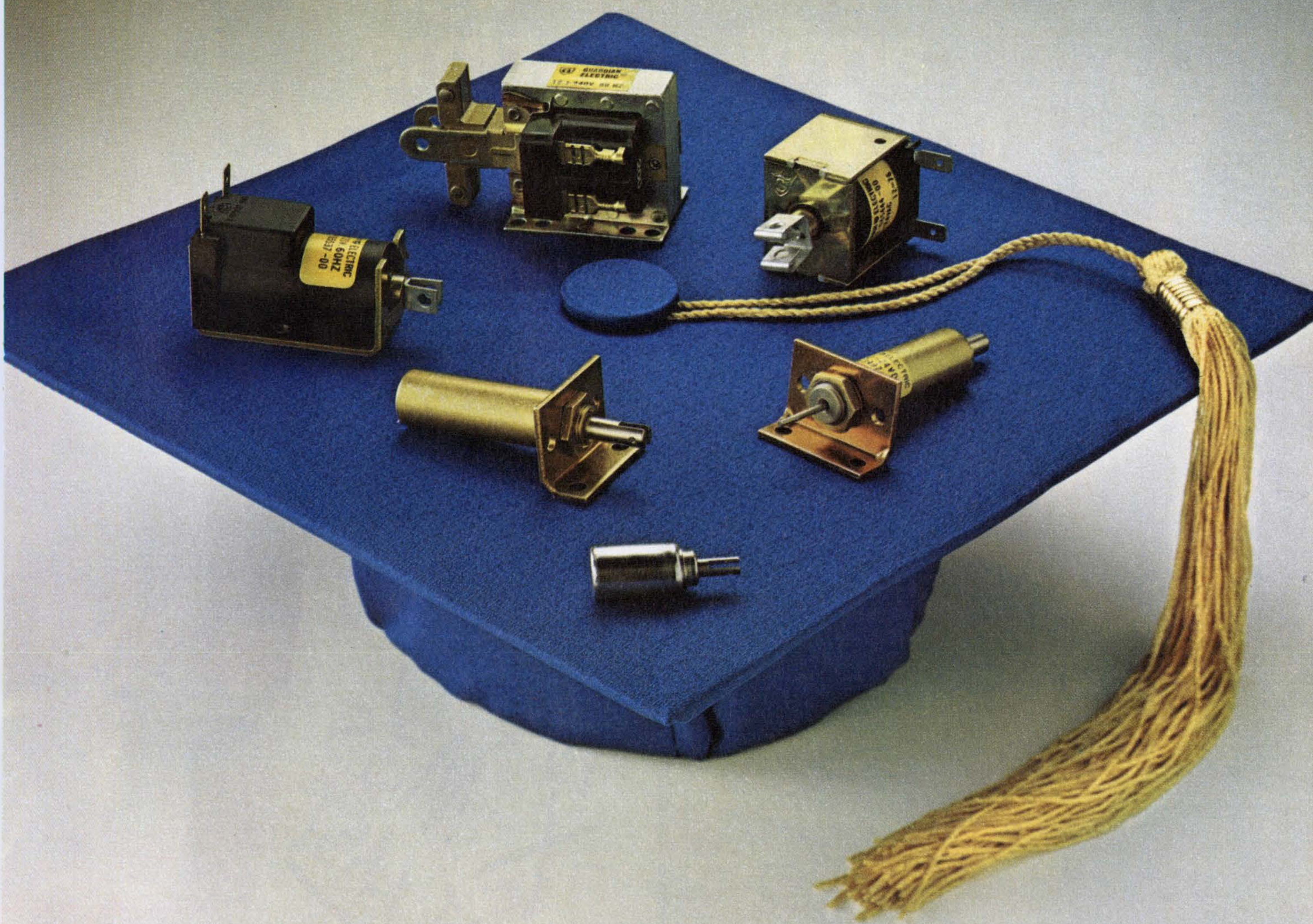
**TOLL FREE NUMBERS: Outside California** 800-227-0280; **Outside New Jersey** 800-631-7030; **Outside Maryland** 800-638-0838; **Outside Illinois** 800-323-2513.

CIRCLE NUMBER 274

# Group portrait: The Class of '77



**Guardian solenoids are made in all sizes and shapes: Box frame, U-frame, laminated and tubular . . . push 'n pull . . . AC 'n DC. But, it's the WAY they're made that puts them in a class by themselves.**

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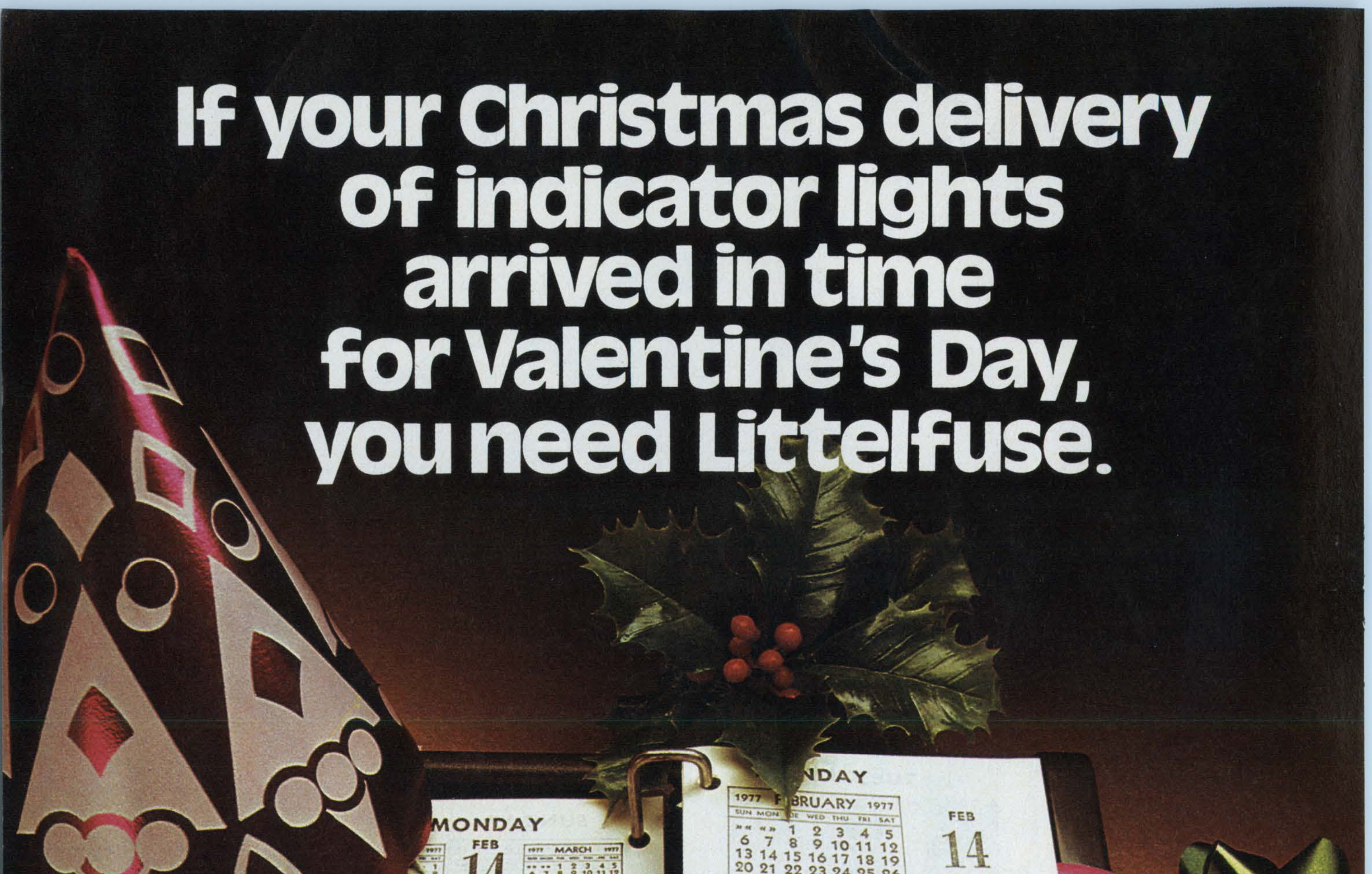


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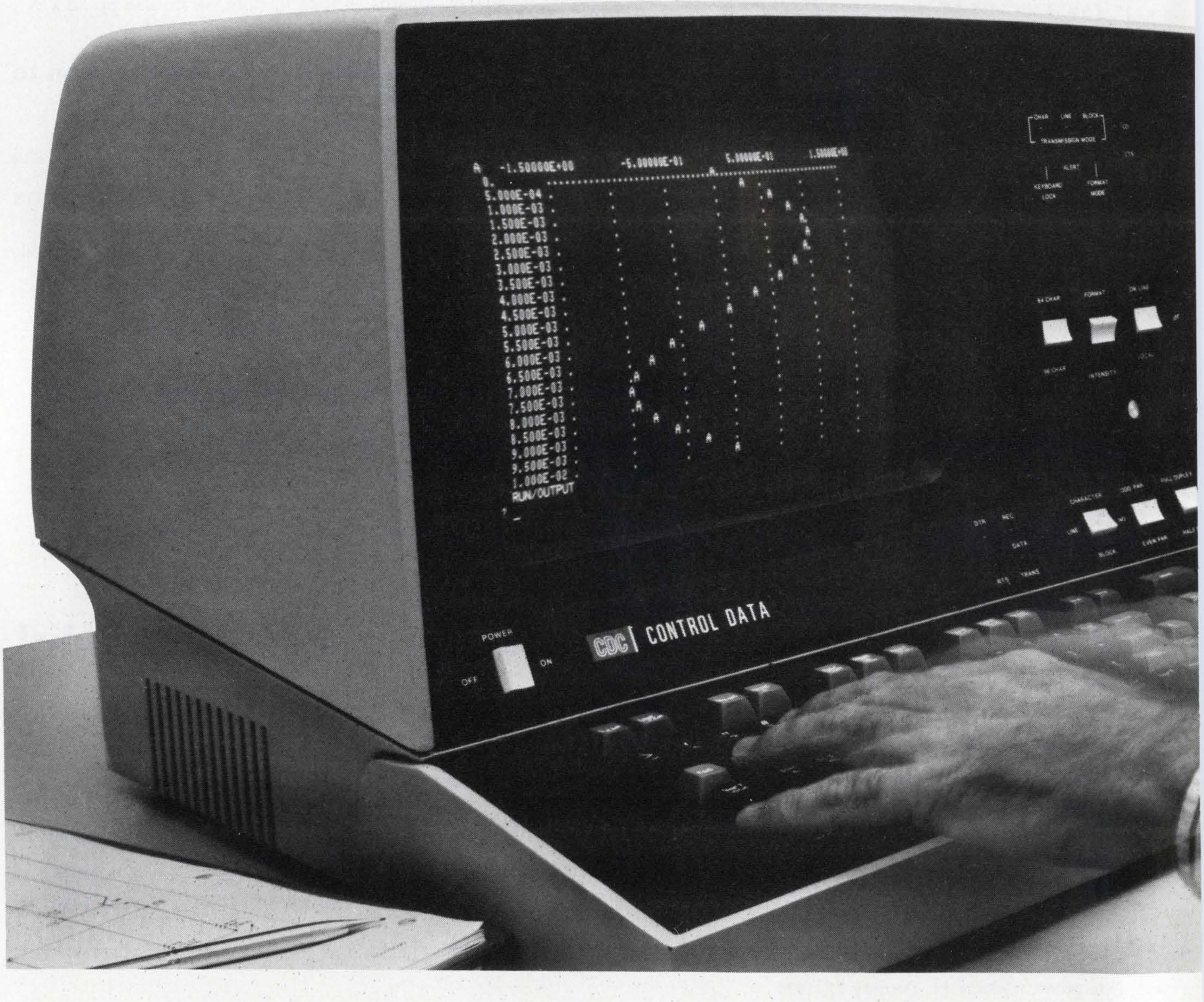


# FOCUS on Floppy-Disc Drives

In a floppy-disc drive, the medium spins while the head stays put. But dive into the specs on the 30 available models, and your head may end up spinning.

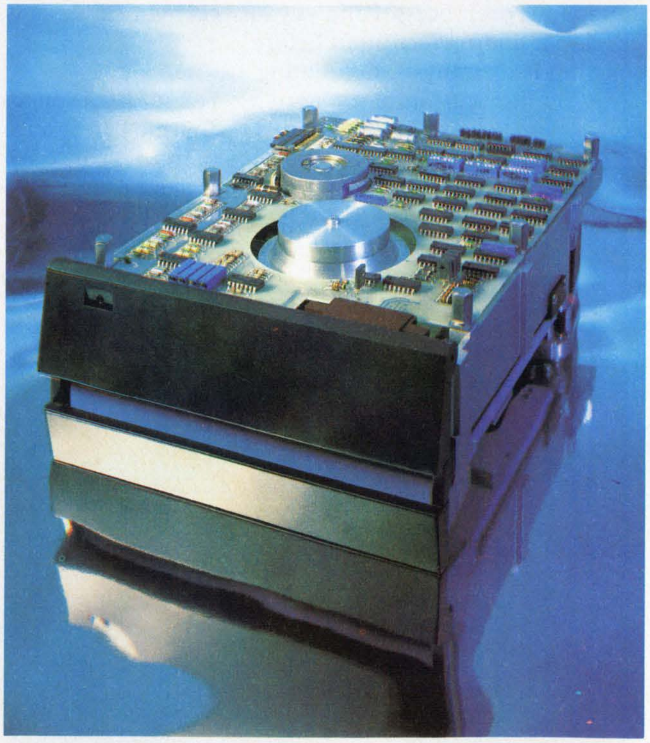
To select the right floppy drive for your job, you have to choose from a wide range of capacities and transfer rates, decide on a hard-sectored or soft-sectored format, satisfy yourself of the reliability of the unit you choose, and match it with an appropriate controller, interface, and software. You also must consider your company's requirements for tomorrow.

You face a choice between 8-in. and 5-1/4-in. diskettes, single and double density, single and double-sided recording, tunnel or straddle erase, and (soon) single and double-track density. You have to pick a head that's crowned or flat, ceramic or ferrite, single or double, and that's moved by a voice coil, a traditional lead screw or the newer metal band.

Is your head spinning yet? You're still not out of the woods. There are many conflicting manufacturer's claims to evaluate. You may find three "fastest" actuators, four "best" heads, maybe eight "smartest" door interlock systems.

Then come the not-so-technical headaches. Keeping in mind cost and vendor reliability. Second-guessing the next IBM move and its impact on what's available. Comparing drive mechanical details: "If this snap-action switch got designed *out* of two other brands after a few months of field use, do I want it in mine? Does it really harm the diskette envelope? Why did two manufacturers replace the switch with a LED-photodiode assembly?"

With so many different floppy designs, the performance picture hasn't stabilized by a long shot. For example, a half-dozen vendors have followed Shugart with two-headed standard floppies that double the on-line capacity of their units. More changes can be expected as soon as IBM tips its hand on double-track



**This double-sided, double-density IBM-compatible Mayflower 700** from MFE measures 30% smaller than competition, and multiplies media life by four. Dc-motored 750 version claims a high 10,000-h MTBF and low power—30 W. The 700 and the 750 are the first floppy products of MFE, an established cassette builder.

**Dave Barnes**
Western Editor

density in January, 1978.

Right now, many drives have built-in provisions for double track. They use two (in one case, three) stepper increments to do a one-track move. There is no guarantee that this will completely satisfy the new IBM format. But there's hope. Although many drives are used to record non-IBM-compatible formats, IBM compatibility is still the watchword for factors as basic as the track geometry itself.

As if waiting for double-track standards weren't enough, rumor now has it that IBM will soon bring out a 3-1/2-in. micro-sized floppy. Indeed, *no* part of floppy-disc technology is standing still. Look at the frame—a component that few electronic designers normally consider very exciting. Manufacturers have been stamping them out of aluminum or steel for years —drilling a few holes, and going on from there.

Now Memorex has introduced a plastic chassis. It's molded in one piece of extra-rugged fiberglass-reinforced polyester (FRP), which gives you lighter weight and tolerances that may be unachievable with aluminum or steel.

FRP can also save money, since the molding process incorporates a large number of inserts, holes, bosses and gussets without any per-unit labor expense.

But along with the new benefits, are there any new problems? Will the electrical shielding of the old metal chassis be missed? Or the magnetic shielding of the steel one?

The floppy disc field is only five years old. But the typical design you'll look at is one or two years old at the most, and may have been redone to correct the faults or limitations of the first-generation design.

### A child of diversity

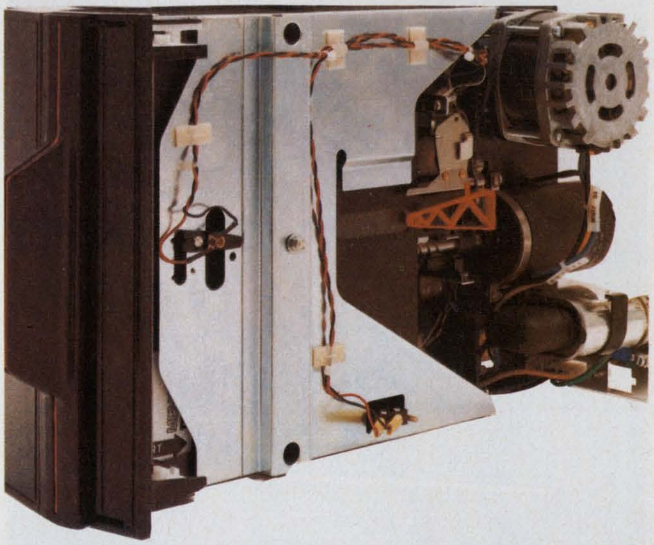
But aren't all floppy drives based on an IBM standard format, and therefore alike? In format, yes. In construction, dependability, and performance, no.

Innovations and variations in design have come from a dozen noncaptive manufacturers, which are still manufacturing floppy drives for OEM use, from three or four that have stopped manufacturing floppies, and from suppliers like IBM, Burroughs and Sycor, which build floppies for only their own products.

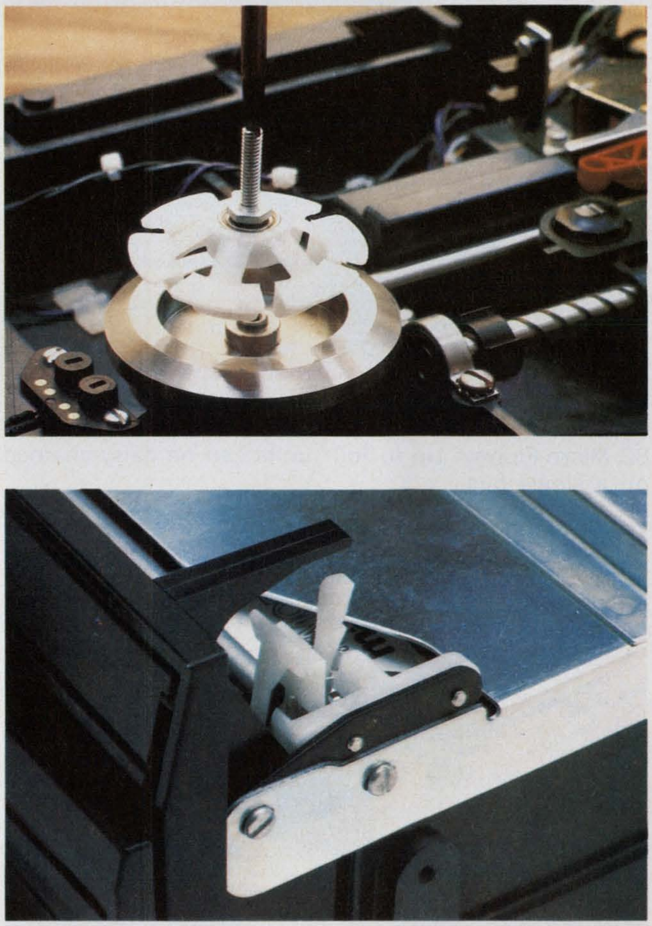
What was a single, well-defined product five years ago has been superseded by a broad spectrum of competing products, each bringing something a little different to your search party. Tables 1, 2, and 3 tell the growth story.

Before you can simply run a finger down the charts and pick a winner, you have to examine the whole range of available products. You should also be aware of spec tricks and be ready to visit and grill every prospective supplier.

Table 1 shows the tremendous range of floppy-disc drives with integration levels defined along the horizontal axis of the chart, and data capacities along



**The light, rigid chassis** of the Model 550 from Memorex, molded from fiberglass-reinforced polyester, meets tight tolerances that steel and aluminum can't. Its design permits factory upgrading to the recently introduced dual-head 552 version.

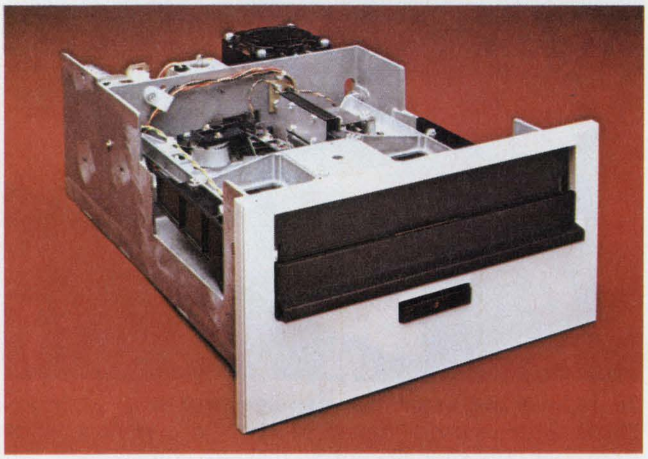


**To reduce the usual disc-damage problems,** Memorex 550/552 drives use a "balanced-velocity" clamping design (top) that cuts slippage during diskette engagement, and a door-controlled latch/eject mechanism (bottom) that pops media in and out and is interlocked to prevent the door from closing on a diskette that's not fully in.



**Seeking guaranteed interchangeability of diskette media,** Tri Data departs from industry standards with its floppy drives for the Flexifile 10 (left) and 11 (right). Track width is triple the industry standard, though the 8-in. medium affords only 32 tracks, 98 kbytes of storage and 40 kbytes/s transfer with 100-rpm operation.

**Dual-index and file-protect sensors** permit recording of data on both sides of a microdiskette on the Wangco Model 82 Micro-Floppy. Up to four units can be daisy-chained on a single bus.



**A double-sided, double-density floppy-disc drive,** the SA 850 from Shugart Associates is plug-compatible with the company's standard 800.

the vertical axis. At the right-hand side of the chart are some of the quasistandard specs for most of the products in each capacity level. The arrow at the left reminds you that it all began with the standard floppy, from which came the smaller-capacity minifloppy as well as the larger-capacity combinations of double-density, double-head, and (soon) double-track.

Examine the integration levels. No doubt if you're designing for volume production, you will end up buying basic floppy-disc drives with read-write and motion-control electronics and little else (level 1 or 2). These days, you'll probably evaluate several existing controllers before seriously thinking about building your own.

Perhaps, however, you can get your project off the ground six months sooner by buying a complete ready-to-go floppy-storage subsystem. It can "front" for you in system-level tests, while you engineer your production version to be functionally similar but much more cost-effective. To determine if this two-pronged approach makes sense, you may want to look at complete, packaged floppy subsystems as well as bare drives. Talk with the system builders. They're old hands at evaluating and comparing basic drives.

Use Tables 2 and 3 to complete the overview of available products. Get in touch with vendors early in the design and stay plugged in on spec changes and new product announcements.

Now to the specs.

### Digging into the data sheets

One question you'll surely ask: How long do diskettes last? Most manufacturers specify track life as 3-million to 5-million passes (rotations) per track, and their accompanying literature smoothly assures you that the early problems with media life have been solved for the most part.

But once you do the arithmetic and discover that even a low diskette speed of 360 rpm (low compared with the 1800 to 3600 rpm of fixed-head discs) translates to more than a half-million passes per day, you don't feel so assured.

A track can wear out in as little as six 24-hour days.

No problem, if the wear is distributed among the 77 tracks of a standard floppy, and if no diskette spends too much time on the system, and if the heads aren't loaded against the medium when data aren't being accessed.

But some designs locate frequently used information, such as the software-operating system and key subroutines, on a few heavily used tracks of the disc. And heavy usage of a few tracks and light usage of others is determined by software, and seldom by the hardware design engineer.

Diskettes themselves can be dented, damaged, or devoured by media sensors and faulty clamping mechanisms, and made vulnerable to damage by doors that either aren't locked or aren't interlocked. Improved designs have been triumphantly announced—only to be recalled as quietly as possible when unexpected bugs developed. Don't count on the data sheet to show you that the mechanical arrangements are foolproof.

Many data sheets crow about "the unit's superior head design" which is said to give "the extremely low head/media wear." But few mention the head-loading force, let alone specify that it is a controlled quantity.

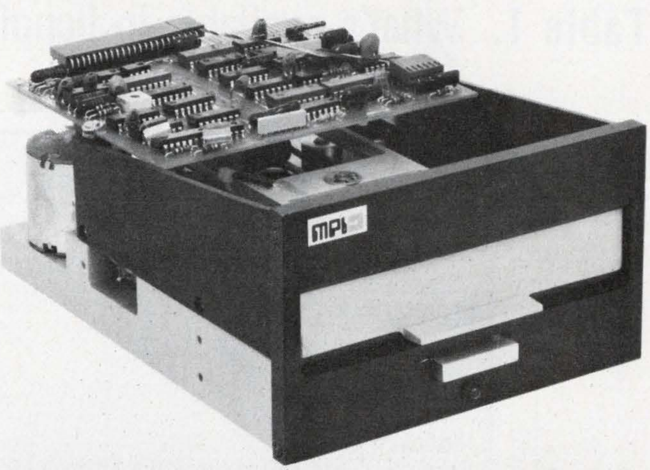
Shugart's design improvements in the 850/851 two-head band design allow the company to lower head loading from 15 to 8 grams. The result? A longer media and head life. The vendor should specify the force at which his heads are set, and guarantee it over all units. How much, for example, will that force vary on a single-sided unit as the head-load pad wears out?

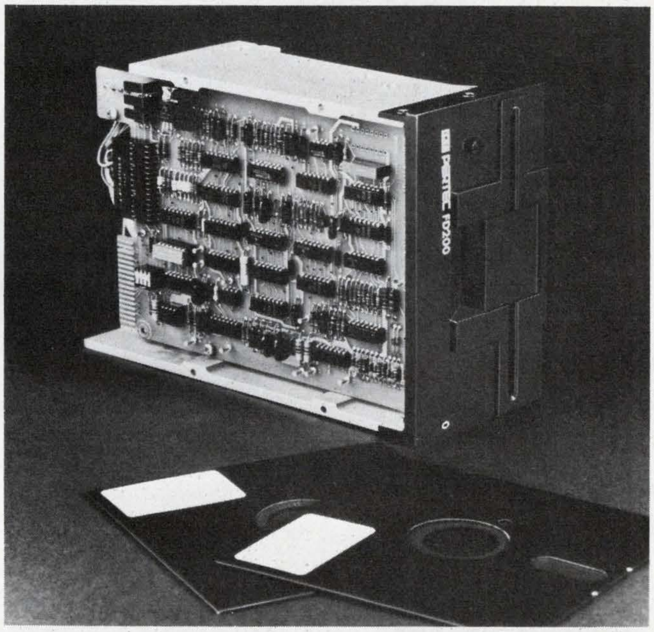
### Your pad or mine?

Even though data sheets say "no maintenance required," head load pads on a single-sided unit need to be replaced after 1000 to 2000 hours. And while dual-head designs eliminate the little pad holding the medium against the head, some new designs use big "squeegee" pads to help clean the disc and put the medium in tension. Check how often the pad must be replaced.

Check access times, too. Be sure to ask for maximums. Find out also if the "average" access includes settling time—it usually doesn't. The "average" is usually a third (not a half) of the maximum access time, although average latency is half the maximum rotational period. Vendors are inconsistent, but at least the numbers not shown on the data sheets are readily available.

Remember to question "hours" at every appearance on a data sheet. Head life and service life are stated




**A micro-sized drive (top)** from MPI is the only minifloppy to use a metal-band actuator. Its track-to-track time is 5 ms. Pertec's micro-sized floppy (bottom) boasts the same dimensions, mounting holes, interface signals, and voltage requirements as the Shugart SA400.

in hours. What is meant? During power-on hours (POH), the drive is active only a small fraction of the time. What fraction is the manufacturer assuming?

Whether or not the drive manufacturer sells formatter/controllers specialized to his unit, ask him who else does. Ask how his electronics mates with the Western Digital 1771 controller chip, the NEC 372D, the SMSFDO 300, the Motorola MC 6843, the Intel 8271 or whichever ones pertain to your work. Request design examples and ask him to put you in touch with people who are using those controllers with his drives.

The controller determines how you'll handle double density—but the drive capabilities have to match. The encoding and decoding for modified frequency modulation (MFM) or modified modified frequency modulation ($M^2FM$) or group-coded recording (GCR) are normally done in the controller. Discussion abounds as to which scheme is theoretically the best. Find out who's successful with each method for each drive

## Table 1. What's available in floppies

| | | Diskette media only | Drive with electronics | Dual with electronics | Level 1 or 2 drive, plus controller | Level 3 drive, plus interface | Level 4 hardware, plus software |
|---|---|---|---|---|---|---|---|
| | | Level 0 | Level 1 | Level 2 | Level 3 | Level 4 | Level 5 |
| Larger capacity: Double-sided & double-density floppy disk | Level 4 | See "Need More Info (Media)" | See Table 2 | Example: PerSci 277 and 297 dual drives are comparable in size to most single drives; four 2-diskette duals fit vertically across 19" rack. | Available from many vendors, Tables 2, 3. | Available from some vendors of each group | See "Need More Info (Systems)" |
| "Flippy"® or double-sided floppy disk | Level 3 | | | | | | |
| Single-sided double-density floppy disk | Level 2 | | | | | | |
| ORIGINAL FLOPPY: Standard floppy disk | Level 1 | | | | | | |
| Smaller capacity: Mini-floppy® or Micro-floppy® disk | Level 0 | | See Table 3. | N.A. | | | |

DD — Double-density (MFM, M²FM or GCR) FO — Flip-over: 2-side recording with 1 head 2 HD — Two-head: 2-side recording with 1 head on each side, full capacity on-line.

you're considering. The bandwidth of the heads and electronics also affect your choice.

### Don't forget dirt

A well-known and valuable feature of the floppy is that it doesn't have to operate in a "clean room." But how much dirt is acceptable? Data sheets list temperature and humidity limits but fail to consider the amount of dirt in the air. So beware.

Unless you can find it in print, the manufacturer isn't promising a floppy that will tolerate dirt. At least one vendor, Innovex, does have an enclosed filtered-air environment.

Until recently, most floppy applications have had no major dirt/dust problems, since the diskette stayed wrapped in an envelope lined with a dirt-removing material. Constant burnishing by the freshly cleaned medium cleans the heads, too.

But now a new component that is potentially dirt-sensitive has been introduced in some drives. Several vendors are offering metal-band actuator designs as the least expensive way to reduce track-to-track motion times. A metal band wrapped around a capstan replaces the traditional lead screw as the element transferring the motion from the stepping motor to the head assembly.

However, dirt buildup on the metal band may affect reliability by changing the effective radius of the capstan. So, more dirt means more head motion when the capstan rotates—and more track separation. Even a few-thousandths buildup across the 77 tracks of a standard floppy can cause real problems, some experts warn.

Memorex and General Systems International have so far avoided a dirt hassle—no band. They have stayed with the lead screw, and made it play at 3 ms, the same as most metal-band actuators.

In the current Shugart product line, the single-head Models 800 and 801 use a lead screw. The dual-head Models 850 and 851 use a metal band and feature a decrease from 8 ms to 3 ms of track-to-track time. But too many changes are involved to upgrade an existing single-head model to dual-head.

Both Memorex and General Systems International claim to have a higher commonality of parts between their single-head and dual-head models than Shugart. Memorex will upgrade its single-head Model 550s to Model 552s for dual-head double-sided recording at the factory. GSI discourages such modifications because too many changes are needed, including head-loading hardware as well as the head carrier, but points to an 85% commonality of spare parts between its single-head FDD110s and double-head FDD220s.

Typical Storage Specs

| Capacity vs. Sectoring | No. of Tracks | Transfer Rate | Media Size |
|---|---|---|---|
| Kilobytes | Count | Kilobytes/sec. | Package |
| 1600 Hard 972 Soft (DD + FO or ZHD) | 77 per side | 500 | 8″ x 8″ envelope |
| 800 Hard 486 Soft (FO or ZHD) | 77 per side | 250 | |
| 800 Hard 486 Soft (DD) | 77 | 500 | |
| 400 Hard 243 Soft | 77 | 250 | |
| 498.8 if DD & FO 218.8/249.4 if DD or FO 124.7 if 40 tk 109.4 basic | 35 (40 opt.) | 125 (250 if DD) | 5¼″ x 5¼″ envelope |

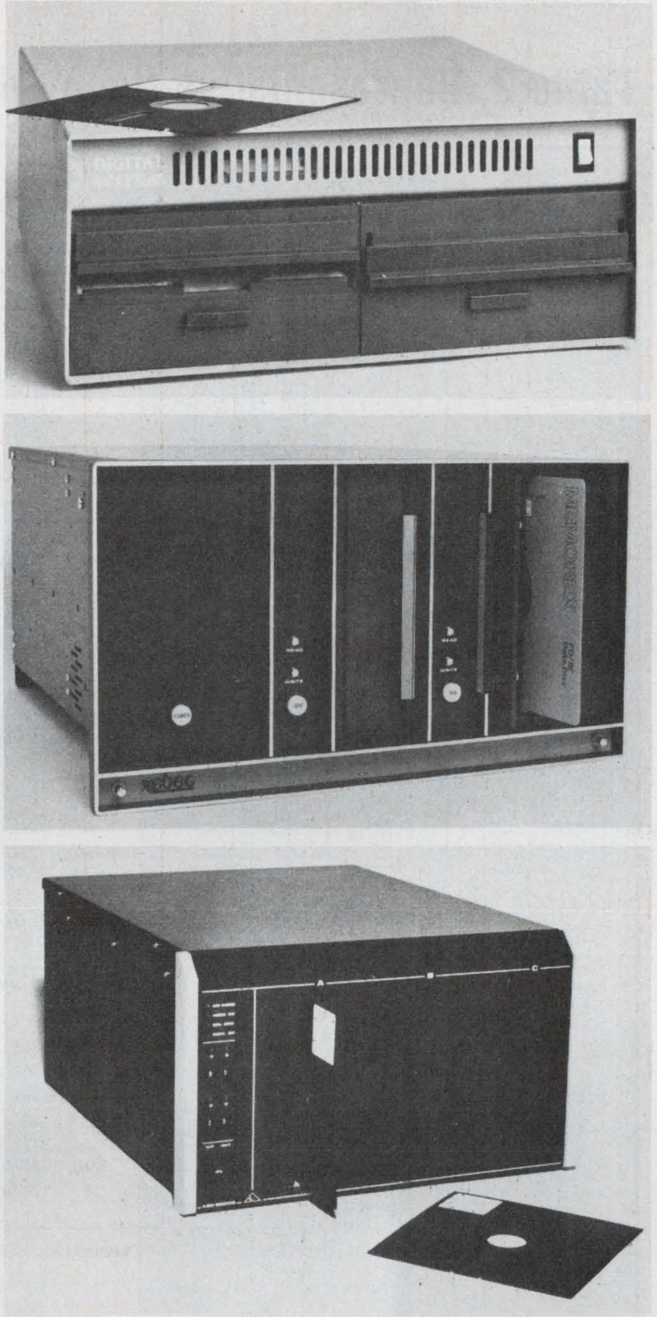
Speaking of upgrades, how well can you foresee those your product may need later? And what do the manufacturers promise? Will you have to discard your floppies or merely modify them when double-track or some other change comes out? Data sheets seldom clear up such questions.

### Get thee to a factory

For this reason and because many of the floppy-drive designs—and companies—are new, visits to the vendors' plants are valuable. Go with the idea of extensively questioning and examining the field performance of the unit you're considering, and the modes of failure. Down-to-earth discussions with satisfied—and dissatisfied—users of the products are also a must.

Put tough questions to every manufacturer you are considering, such as: "Is your mean-time-between-failures spec measured or calculated? If it is not based on field data, just how is it calculated?" Several data sheets candidly state that MTBF figures are calculated; that is, they are theoretical figures derived on paper from formulas—not factual data based on the real longevity of drives used in the field. Other manufacturers are not so candid; they omit the word "calculated." One even heralds "our MTBF rating," as if some outside authority had bestowed the 9000-hour figure after it was earned.

Keep your questions coming: "May I see the data that are the basis of your 0.5-hour mean-time-to-repair (MTTR) specification? What are the main failure modes of the model I am considering? If I sat down at your bench right now, how long would it take you to train me to repair all the kinds of failures that come up? *(continued on page 202)*



**Complete floppy-disc systems** offer both hardware and software systems. Digital Systems' FDS-1 (top) includes one or two Shugart drives, an IBM-compatible controller, an Altair-IMSAI S-100 interface, and cables for connecting with Z80/8080 systems. Various Xebec models (middle) interface PerSci, Shugart, and Memorex drives to PDP8, PDP11, LSI 11, Nova, and Eclipse computers. Advanced Electronics Design (bottom) ties Memorex, Shugart (shown) and Pertec units to those five computers.

(continued from page 201)

# Table 2. Representative floppy drives

**Notes: accept 8-inch square diskettes, access to 1.6 megabytes.**

| Company | Model No. | Model Designation | Capacity level and options (see Table 1) | Integration level (see Table 1) | Motor type | Head actuator | MTBF (hrs.) | MTTR (min.) | No. of Heads | Head life (wks.) | Track Life (days) | Read errors, recoverable | Read errors, unrecoverable | Seek error rate | Motion times (ms.) latency (av.) | headload | access, tk-tk | access, (av.) | settling | Units in rack width | Weight (lb.) | Special features |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Calcomp | 142M | Floppy Disk Drive | 1, 2 | 1 | AC | V leadscrew | note 1 7000 | <30 | 1 | note 2 DES 5 yr. or 30,000h | note 7 ? | $10^{-9}$ | $10^{-12}$ | $10^{-6}$ | 83 | 30 | 6 | — | 10 | 3E | 16 | Daisy chain, good read margins. |
| | 143M | " " " | 4MFM | 1(3) | AC | " | " | " | 2 | " | ? | " | " | " | 83 | 30 | 6 | — | 10 | 3E note 3 | 16 | Unique flat heads, opt'l. 1143M controller. |
| Control Data | 9400 | " " " | 1 | 1(3) | AC | Leadscrew | 4000 | 30 | 1 | SVC 5 yrs. | — | $10^{-9}$ | $10^{-12}$ | $10^{-6}$ | 83 | 60 | 10 | 270 | 10 | 3 | 12 | 9474 subsystem |
| | 9404 | " " " | 1, 2 | 1(3) | AC | " | 4000 | 30 | 1 | or 30,000h | — | " | " | " | " | 60 | 10 | 270 | 10 | 3 | 12 | interfaces 9404 |
| | 9406 | " " " | 4 | 1(3) | AC | Band (note 9) | 8000 | 30 | 2 | " | — | " | " | " | " | 40 | 3 | 91 | 10 | 3 | 12 | & 6's with 8080. |
| General Systems Int'l. | GSI-110 | Flexible Disk drive | 2 | 1(3) | AC | Leadscrew | 6000 | 20 | 1 | SVC 5 yrs. or 30Kh | 7 | $10^{-9}$ | $10^{-12}$ | $10^{-6}$ | 83 | 35 | 6 | 156 | 14 | 4 | 13 | >55% read resolution on track 76. |
| | FDD-200 | Flexible Disk drive | 4MFM, $M^2FM$ | 1(3) | AC | Leadscrew | 6000 | <20 | 2 | SVC 5 yrs. or 30Kh | 7 | $10^{-9}$ | $10^{-12}$ | $10^{-6}$ | 83 | 35 | 3 | 128 | 14 | 4 | 11 | 3-bearing stepper, shielded pc |
| Innovex Corp. | 200, 400 Series | Floppy disk drive | 1, 2 | | AC | Leadscrew | >8500 | <30 | 1 | >15Kh typ. | 7 | $10^{-9}$ | $10^{-12}$ est. | $10^{-6}$ | 83 | 30 | 8 | — | 8 | 4E | 14 | Filtered air, 35% better read margins. |
| | 600 Series | Double-sided disk drive | 4 | | (In development) | | | | 2 | — | — | — | — | — | — | — | — | — | — | — | — | |
| MFE | 500 Series | Mayflower single-sided drive | 1, 2 | | (In development) | | | | 1 | | | | | | | | | | | | | |
| | 700 Series | Mayflower Double sided drive | 4MFM $M^2FM$ | 1 | AC or DC models | Band | >10,000 if DC motor | — | 2 | $4x10^7$ passes (note 5) | >10 | $<10^{-9}$ | $<10^{-12}$ | $<10^{-6}$ | 83 | 35 | 3 | — | 15 | 4 | 10 | Smallest, lowest power in DC version. |
| Memorex Corp. | 550 | OEM floppy | 1, 2 | 1 | AC | Leadscrew | 9000 | 30 | 1 | — | 10 | $10^{-9}$ | $10^{-12}$ | — | 83 | 35 | 6 | — | 10 | 4 | 10.7 | FRP frame, power saver on stepper. |
| | 552 | OEM dual-head floppy | 4MFM $M^2FM$ | 1 | AC | Leadscrew | 9000 | 30 | 2 | — | 10 | $10^{-9}$ | $10^{-12}$ | — | 83 | 35 | 3 | — | 10 | 4 | 10.7 | Factory can upgrade 550 to 552. |
| Micro Peripherals Inc. | B82 | Flexible disk drive | 1, 2, 4 | 1 | AC or DC | Band | 8000 | 30 | 2 | DES 5 yr. (note 2) | 7 | $10^{-9}$ | $10^{-12}$ | $10^{-6}$ | 83 | 35 | 3 | 91 | 15 | 3 | 10 | Compatible with Shugart, 30% less parts. |
| Per Sci, Inc. | 70 | Single floppy | 1, 2 | 1(3) | DC | Voice-coil | 6000 | 20 | 1 | DES 5 yrs. or 15Kh | 7 | $10^{-9}$ | $10^{-12}$ | $10^{-6}$ | 83 | 40 | 10 | 33 | 0 | 4 | 15 | 1070 controller available (all models) |
| | 277 | Dual floppy | 1, 2 | 2(3) (note8) | " | " | " | " | 2 (note 8) | " | " | " | " | " | " | " | " | 33 | 0 | 4 | 20 | Holds 2 independent diskettes. |
| | 297 | Two-sided dual floppy | 4 | 2(3) (note8) | " | " | | | 4 | | | | | | " | 35 | " | 33 | 0 | 4 | 22 | All models have motor to insert disk & push-button to eject |
| Pertec, Inc. | FD400 | Flexible disk | 1 | 1 | DC | Leadscrew | >10,000 | — | 1 | 20Kh | 10 | $10^{-9}$ | $10^{-12}$ | — | 83 | 40 | 10 | — | 20 | 4 | 14 | 3 steps/tk., ferrite heads. |
| | FD5X0 | " | 1(2) | 1 | AC | " | " | — | 1 | " | 10 | " | " | — | 83 | 40 | 10 | — | 20 | 4 | 14 | Steel chassis, DD optional. |
| | FD511 | " | 1, 2 | 1 | AC | " | " | — | 1 | " | 10 | " | " | — | 83 | 40 | 10 | — | 20 | 4 | 14 | Daisy chain, and extra control lines. |

| Company | Model No. | Model Designation | Capacity level and options (see Table 1) | Integration level (see Table 1) | Motor type | Head actuator | MTBF (hrs.) | MTTR (min.) | No. of Heads | Head life (wks.) | Track Life (days) | Read errors, recoverable | Read errors, unrecoverable | Seek error rate | Motion times (ms.) latency (av.) | headload | access, tk-tk | access, (av.) | settling | Units in rack width | Weight (lb.) | Special features |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Remex | RFD1000 | " | 1, 2MFM | 1(3-5) | AC | Stylus ball | — | — | 1 | >30Kh | >10 | $<10^{-9}$ | $<10^{-12}$ | — | 83 | 50 | 6 | 176 | 24 | 3E | 15 | PDP 8/11 interfaces available. |
| Shugart Associates | SA800 | Diskette storage drive | 1, 2 | 1(3) | AC | Leadscrew | 5000HD 8000TYP | 30 | 1 | 15Kh | 7 | $10^{-9}$ | $10^{-12}$ | $10^{-6}$ | 83 | 35 | 8 | 260 | 8 | 3E | 13.0 | Industry std. Controllers available. |
| | SA850 | " " " | $4M^2FM$ | 1(3) | AC | Band | " | 30 | 2 | " | 7 | $10^{-9}$ | $10^{-12}$ | $10^{-6}$ | 83 | 35 | 3 | 91 | 15 | 3E | 13.0 | 8 gm head load force, down from 15. |
| Wangco, Inc. | 76 | Diskette drive | 1, 2 | 1(3) | AC | Uni-ball | 5000 | 30 | 1 | DES 5 yrs. | N.A. | $10^{-10}$ | $10^{-12}$ | $10^{-6}$ | 83 | 16 | 6 | 168 | 14 | 3E | 13 | |
| | 276 | Dual head diskette drive | 4 | 1 | AC | Uni-ball | 8000 | 30 | 2 | DES 5 yrs. | N.A. | $10^{-9}$ | $10^{-12}$ | $10^{-6}$ | 83 | 35 | 3 | 90 | 15 | 3E | 13 | |

# Table 3. Representative micro/mini/floppies

**Note: accept 5.25-inch-square diskettes, hold 109.4 kilobytes on 35 tracks, one side up to 498.8 kilobytes if options incl. 40, DD, FO } double for DD (double-density) (MFM,$M^2$FM) and/or double (again) if FO (flip-over recording)**

| Company | Model No. | Model Designation | Capacity level and options (see Table 1) | Integration level (see Table 1) | Motor type | Head actuator | MTBF (hrs.) | MTTR (min.) | No. of Heads | Head life (wks.) | Track Life (days) | Read errors, recoverable | Read errors, unrecoverable | Seek error rate | Motion times (ms.) latency (av.) | headload | access, tk-tk | access, (av.) | settling | Units in rack width | Weight (lb.) | Special features |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pertec, Inc. | FD200 | Micro-sized | 0, 40, DD, FO | 1(5) | DC servo | Cam | — | — | 1 | 20Kh | 6 | — | — | — | 100 | 35 | 25 | ? | 10 | — | 3.2 | |
| Shugart Associates | SA400 | Minifloppy | 0 | 1(3) | DC | Cam | 8000 (note 6) | 30 | 1 | ? | 6 | $10^{-9}$ | $10^{-11}$ | $10^{-6}$ | 100 | 75 | 40 | 463 | 10 | — | 3 note4 | |
| Micro Peripherals Inc. | B51 | Micro-sized | 0, 40, DD | 1 | DC servo | Band | 10,000 | 30 | 1 | DES 5 yrs | 6 | $10^{-8}$ | $10^{-10}$ | $10^{-6}$ | 100 | 35 | 5 | 75 | 15 | — | 3.0 | Patented disk clamp, eject, band. |
| Wangco, Inc. | Model 82 | MicroFloppy™ | 0, 40, DD, FO | 1(3) | DC servo | Leadscrew | 8500 | 30 | 1 | Des. 5 yrs. | N.A. | $10^{-9}$ | $10^{-12}$ | $10^{-6}$ | 100 | 60 | 30 | 370 | 20 | — | 3.5 | 8201 microcontroller available. |

Notes:

1. MTBF figures are sometimes labeled "calculated" or "normal operations".
2. If head life is not stated, "DES" (design life) or "SVC" (service life) spec is quoted in this column.
3. "E" means estimated, where not stated by manufacturer. If H< 4.38, 4-wide is assumed.
4. Weight is "nominal", according to Shugart.
5. MFE quotes head life as >40x10[6] wear revolutions (>80 days of 24 hrs with heads loaded — absolute worst case, this is >11 weeks). Normal usage makes heads last much longer, since heads contact media a small fraction of POH (power-on hours). But all manufacturers leave "normal usage" undefined.
6. MTBF is 8000 power-on hours, but spindle motor is assumed to be on only 25% of those hours.
7. ED has quoted media life per track in terms of worst-case 24-hour days. Thus 3.5x10[6] wear passes becomes 7 days. Normal usage makes media last much longer, if duty cycles are low.
8. PerSci 277 and 297 are about the same size as most single-diskette drives, but each holds two independent diskettes, usable simultaneously.
9. CDC9406 was shown at NCC with leadscrew, but band is used in production units.

*(continued on page 204)*

*(continued from page 203)*

"How many repair people have you trained this way? How many are within service distance of my customers' locations? What tools and equipment will such a serviceman need, and how big a stock of parts? How do I test to ensure that I am reading $10^9$ bits per soft error and $10^{12}$ bits per hard error? Can I test every unit to this spec? If not, how and when do I apply the spec?"

In a standard-density floppy, the data transfer rate is 250 kilobits per second. Figuring 10 bits per byte, reading or writing $10^9$ bits takes 400 seconds or 6-2/3 minutes and $10^{12}$ bits takes 111 hours.

But suppose soft errors start cropping up more often than every 6 minutes—and hard errors more often than every 111 hours. Certainly, the burden of proof will be on you to show that you are maintaining and operating the unit correctly.

But what kinds of records will the manufacturer expect to see before he will even consider that it is *his* problem? How will you demonstrate to him that the "bug" is in the heads or electronics that he supplied, not in some infrequent glitch in your digital controller? Must you prove that you have never operated his floppy drive outside the temperature and humidity ranges he specified?

Does his spec apply only when you are using diskette media carrying his brand name? Or only when the diskette is recorded on his make of drive? Or only when it is recorded on the same drive that's reading it?

Find out if the manufacturer will work with you to correct any failures of *his* floppy drive in *your* system. He may plan to defend his unit by excluding your system as an unknown situation, and proving his drive meets specs in the environment at his factory. Perhaps previous customers have charged that the units were not meeting the MTBF, MTTR, or reliability specifications. How were these challenges resolved?

Apply hard questioning to burn-in and production testing as well. Does the manufacturer do margin testing? If so, how? In one method, specially prepared diskettes at Shugart contain track segments that are radially displaced by 1 to 10 mils, in 1-mil increments. Units that cannot read tracks displaced by ±0.008 in. don't get shipped. This provides an effective margin test on the read electronics.■■

## Need more information?

The products cited in this report don't represent the manufacturers' full lines. For additional details, circle the appropriate number on the Reader Service Card. For data sheets and more vendors, consult ELECTRONIC DESIGN's GOLD BOOK.

### Floppy drives

Calcomp, 2411 W. LaPalma, Anaheim, CA 92801. (714) 821-2011. (Joel Levine) **Circle No. 361**

Control Data, P.O. Box 12313, Oklahoma City, OK 73112. (405) 946-5421. (Terry Hardie) **Circle No. 362**

General Systems International, 1440 Allec St., Anaheim, CA 92085. (714) 956-7183. (Mike Krunic) **Circle No. 363**

Innovex Corp., 75 Wiggins Ave., Bedford, MA 01730. (617) 275-2110. (Gary Bloch) **Circle No. 364**

MFE, Keewaydin Dr., Salem, NH 03079. (603) 893-1921. (Jim Bartley) **Circle No. 365**

Memorex Corp., San Tomas & Central, Santa Clara, CA 95052. (408) 987-1396. (Bob Erdman) **Circle No. 366**

Micro Peripherals, 8724 Woodley Ave., Sepulveda, CA 91343. (213) 894-4076. (Keith Ullal) **Circle No. 367**

PerSci, Inc., 4087 Glencoe Ave., Marina Del Rey, CA 90291. (213) 820-3764. **Circle No. 368**

Pertec, 9600 Irondale Ave., Chatsworth, CA 91311. (213) 999-2020. (Bob Conti) **Circle No. 369**

Remex (Ex-Cell-O), 1733 E. Alton St., Irvine, CA 92714. (714) 557-6860. (David Kolstrom) **Circle No. 370**

Shugart, 415 Oakmead Pkwy., Sunnyvale, CA 94086. (408) 733-0100. (George Sollman) **Circle No. 371**

Wangco, 5404 Jandy Place, Los Angeles, CA 90066. (213) 390-8081. (George Toor) **Circle No. 372**

### Systems

Advanced Electronics Design, Inc., 440 Potrero Ave., Sunnyvale, CA 94086. (408) 735-3555. (Jerry Kennedy) **Circle No. 373**

Charles River Data Systems, Inc., 235 Bear Hill Rd., Waltham, MA 02154. (617) 890-1700. (Wm. Nimee) **Circle No. 374**

DTC (Data Terminals & Communications), 1190 Dell Ave., Campbell, CA 95008. (408) 378-1112. (Herb Martin) **Circle No. 375**

Data Systems Design, Inc., 3130 Coronado Dr., Santa Clara, CA 95051. (408) 249-9353. (George Fink) **Circle No. 376**

Digital Systems, 6017 Margarido Dr., Oakland, CA 94618. (415) 428-0950. (John Torode) **Circle No. 377**

Echo Science Corp., 485 E. Middlefield Rd., Mountain View, CA 94043. (415) 961-7145 (Bill Nichols) **Circle No. 378**

Gnat Computers, Inc., 7895 Convoy Court, Unit 6, San Diego, CA 92111. (714) 560-0433. **Circle No. 379**

Mupro, Inc., 424 Oakmead Pkwy., Sunnyvale, CA 94086. (408) 737-0500. (Donald Pantle) **Circle No. 380**

North Star Computers, Inc., 2465 Fourth St., Berkeley, CA 94710. (415) 549-0858. **Circle No. 381**

Peripheral Vision, P. O. Box 6267, Denver, CO 80206. (303) 777-4292. (John Taylor) **Circle No. 382**

Scientific Micro Systems, 777 E. Middlefield Rd., Mountain View, CA 94043. (408) 964-5700. **Circle No. 383**

Sykes Datatronics, Inc., 375 Orchard St., Rochester, NY 14606. (716) 458-8000. **Circle No. 384**

Tri-Data, 800 Maude Ave., Mountain View, CA 94043. (415) 969-3700. (Herm Levin) **Circle No. 385**

Western Telematic, Inc., 2435 Anne St., Santa Ana, CA 92704. (714) 979-0363. **Circle No. 386**

Xebec Systems Inc., 2985 Kifer Rd., Santa Clara, CA 95051. (408) 988-2550. (Bob Sigal) **Circle No. 387**

### Media

BASF Systems, Crosby Dr., Bedford, MA 07130. (617) 271-4000. (John Healion) **Circle No. 388**

Control Data Corp., 11615 "I" St., Omaha, NE 68137. (402) 333-0850. (J. D. Grimshaw) **Circle No. 389**

Dysan Corp., 2388 Walsh Ave., Santa Clara, CA 95050. (408) 247-4109. (Wm. Harry) **Circle No. 390**

EM&M Media Products, 1020 Timothy Dr., Santa Clara, CA 95133. (408) 298-7090. (Jack Smyth) **Circle No. 391**

IBM Information Records Div., Rt. 522, Ridge Rd., Princeton, NJ 08540. (201) 329-1000. **Circle No. 392**

ITC (Information Terminals Corp.), 322 Soquel Way, Sunnyvale, CA 94086. (408) 245-4400. (Bob Katzive) **Circle No. 393**

K-Tronic Inc., 3260 Scott Blvd., Santa Clara, CA 95051. (408) 246-6830. (Ron Rader) **Circle No. 394**

Memorex Corp., San Tomas and Central Expwy., Santa Clara, CA 95052. (408) 987-1000. **Circle No. 395**

3M Co. Headquarters, 3M Center, St. Paul, MN 55101. (612) 733-1100. **Circle No. 396**

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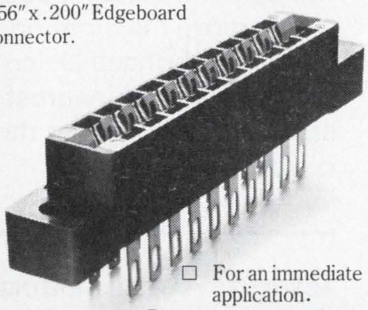

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### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | 24V |
| Operating Voltage | 16V |
| Peak Current | 3A |
| Storage Temperature | −55°C to 150°C |
| Power Dissipation | 22W |

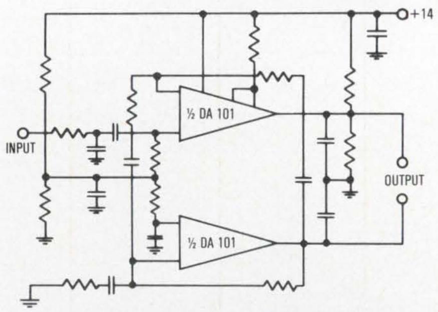
### ELECTRICAL CHARACTERISTICS

| | TYPICAL |
|---|---|
| $V_{CC}$ = 14V dc | |
| $I_{idle}$, $P_{out}$ = 0W | 40mA |
| Differential Input Bias Current | 0.80 μA |
| Open Loop Gain | 90dB |
| Power Out @ 5% Distortion | |
| 4Ω Bridge | 6W |
| 4Ω Non-bridge | 3.5W |

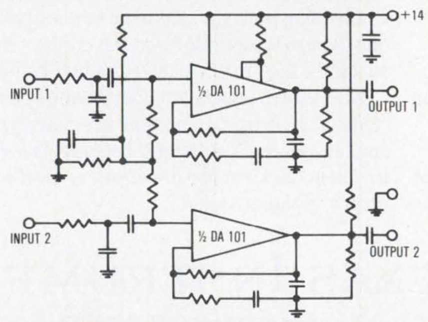
### THERMAL CHARACTERISTICS

| | |
|---|---|
| Thermal Resistance, $R\theta_{JC}$ (Typical) | 4° C/W |

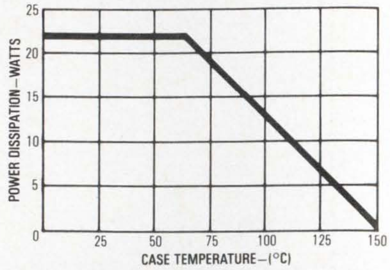
### AUDIO BRIDGE CIRCUIT



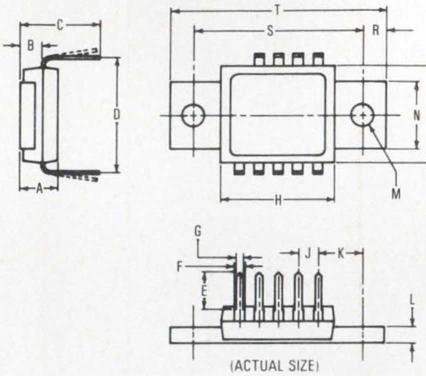

### TWO SEPARATE AMPLIFIERS CIRCUIT




### DERATING CURVE




### DIMENSIONS AND CONNECTIONS




(ACTUAL SIZE)

| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | | .220 | | 5.59 |
| B | .127 | .133 | 3.22 | 3.38 |
| C | .423 | .443 | 10.746 | 11.254 |
| D | .628 | .632 | 15.95 | 16.05 |
| E | .215 | .225 | 5.463 | 5.717 |
| F | .044 | .048 | 1.13 | 1.21 |
| G | .015 | .019 | 0.39 | 0.47 |
| H | .644 | .650 | 16.37 | 16.52 |
| J | .095 | .105 | 2.413 | 2.667 |
| K | .275 | .285 | 6.983 | 7.237 |
| L | .086 | .096 | 2.183 | 2.437 |
| M | .122D | .128D | 3.10D | 3.25D |
| N | .369 | .379 | 9.373 | 9.627 |
| P | .539 | .549 | 13.693 | 13.947 |
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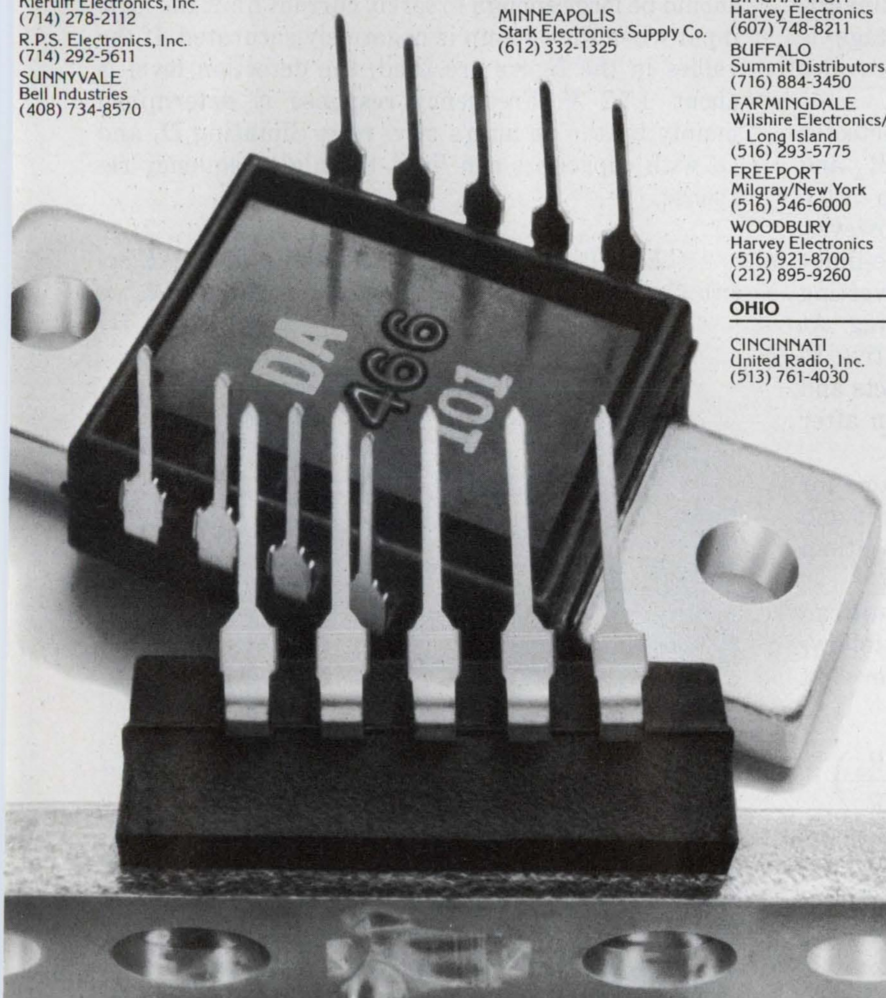


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# Circuit detects and remembers bipolar analog signals

The circuit in the figure can detect an analog signal of either polarity, then remember that the event occurred. It is also simple to design, easy to reset and TTL-compatible.

With no input signal, diodes $D_1$ and $D_2$ of the circuit conduct. Approximately +0.6 V and −0.6 V are applied, respectively, to the inverting and noninverting connections of an op amp. Either voltage is sufficient to saturate the op amp, which then provides a negative output.

If a positive-input signal is applied to the detector circuit, the signal current through resistor $R_A$ and diode $D_1$ doesn't appreciably change $D_1$'s drop of 0.6 V. The signal current through $R_{A1}$ and $R_{B1}$, however, causes $D_2$ to stop conducting. When the positive-input signal rises sufficiently, the op amp's noninverting input becomes more positive than the inverting. At this point the op amp switches from negative to positive saturation. Simultaneously, $D_3$ conducts and holds the op amp in positive saturation, even after the input signal is removed.

The detector circuit performs almost the same for negative-signal inputs, except that $D_1$ turns off and the inverting input then becomes more negative than the noninverting.

When the input signal is removed, the circuit can be reset by grounding the Reset terminal. The following expression determines the input-signal level at which the detector changes state:

$$|e_{in}| = |V_d|\left(1 + \frac{R_a}{R_b}\right) + |V_{cc}|\left(\frac{R_a}{R_b}\right),$$

where $V_d$ = diode-voltage drop,
$V_{cc}$ = power-supply voltage,
and

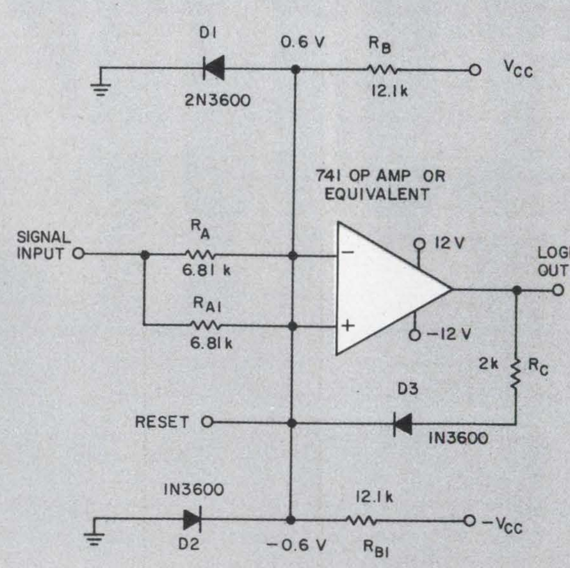
$$\frac{R_a}{R_b} = \frac{R_A}{R_B} = \frac{R_{A1}}{R_{B1}}.$$

The expression ignores the effects of op-amp offset voltage and current, assumes that $V_d$ remains constant with variation in the level of input signal, and also that the signal-source impedance is very low. Particularly if $|V_{cc}|$ is large relative to $|V_d|$, the effects of diode variations are minimized.

If the op amp is supplied with +5 V and −12 V, only a series output resistor is needed to provide direct interfacing with TTL logic. The series resistor should be large enough to safely current limit the logic input when the op amp is negatively saturated. If the values in the figure are used, the detection level is about ±7.7 V. Frequency response is determined mainly by the op amp's slew rate. Shunting $D_1$ and $D_2$ with capacitors can limit the high-frequency response.

*C.E. Musser, Jr., Design Engineer, General Electric Co., P.O. Box 5000, Binghamton, NY 13902.*

CIRCLE NO. 311




**A positive analog input provides a positive logic-level output** that remains after the signal passes. Similarly, a negative input provides a remembered positive-level output.

# Test digital circuits in step-by-step or continuous modes driven by the tested system's clock

Testing complex logic circuits with continuous low-frequency clock pulses is usually inadequate, because you can't stop the action and normal operating-clock specifications aren't employed. A better way is to give the circuit one pulse out of a string of pulses from the system's high-frequency clock, and study the results step-by-step during both HIGH and LOW intervals of the pulse period.

The simple circuit in the figure provides you with four test modes:

1. A single pulse with a normal pulse width, chosen from the system's clock-pulse train.
2. A single pulse with a full-period width.
3. A single pulse whose high polarity is sustained during an arbitrary length of time and switched off synchronously with the clock train.
4. A normal clock-pulse train.

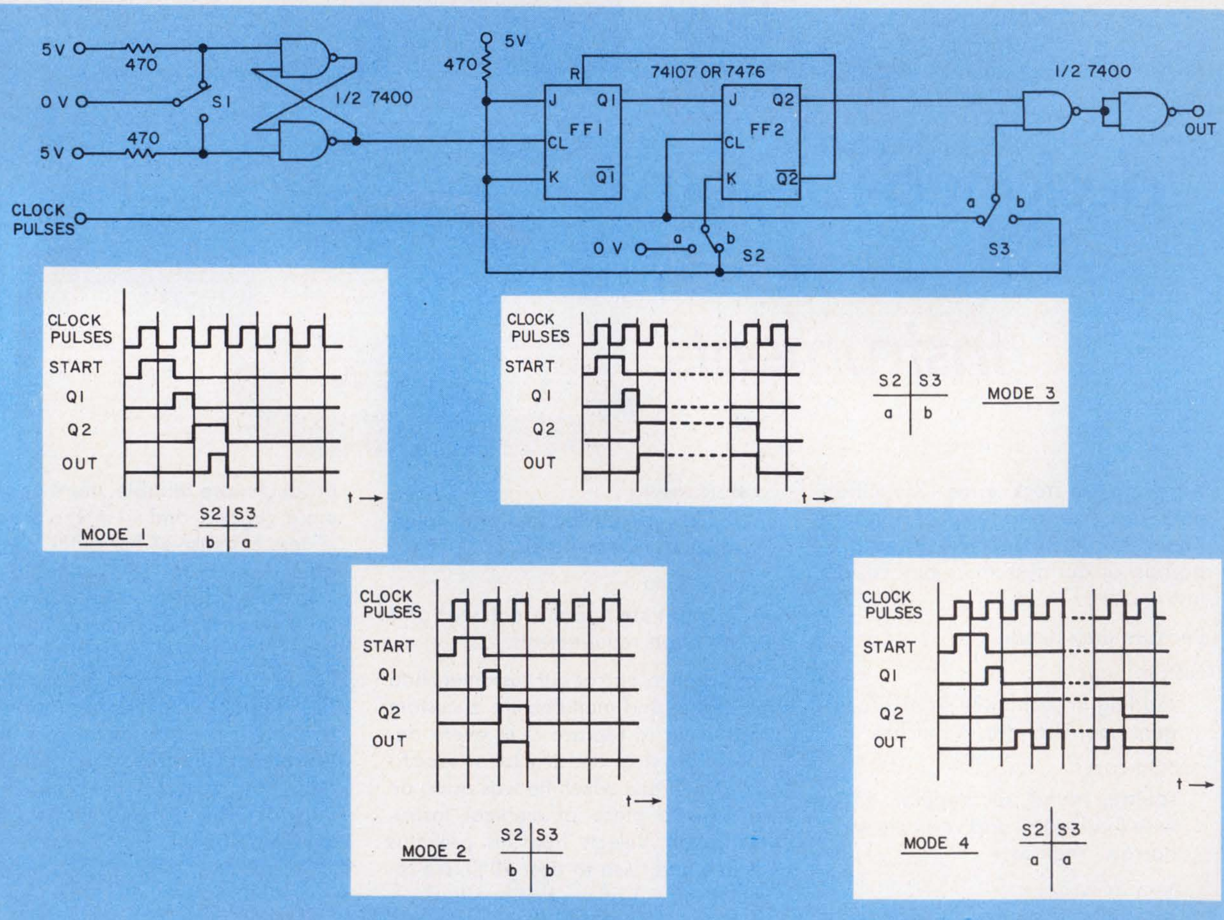
The circuit uses just two JK flip-flops and four NAND gates. When pushbutton switch $S_1$ is pressed and released, $FF_1$ sets. At the next clock pulse, $FF_2$ sets since $J_2$ is HIGH and $K_2$ is either 0 or 1. Output $Q_2$ resets $FF_1$ via $FF_1$'s clear input. This sequence is common to all modes. The sequence, thereafter, depends on the positions of switches $S_2$ and $S_3$.

If $S_2$ and $S_3$ are set as shown, the output $Q_2$ is NANDed with the clock pulses to obtain Mode 1. Since $J_2 = 0$ after $FF_1$ resets, and $S_2 = 1$, $FF_2$ will be reset after one pulse. If $S_3$ is switched the opposite way, the output pulse has a pulse with a full-period width (Mode 2). With both $S_2$ and $S_3$ opposite the positions shown, $FF_2$ stays in the set condition with the ouput HIGH until $S_2$ is set back. At the next clock pulse, $FF_2$ resets (Mode 3).

Mode 4 is obtained with $S_3$ as shown and $S_2$ opposite.

*C. van Holten, Senior Engineer, Dept. of Applied Physics, University of Technology, Delft 2208, The Netherlands.*

CIRCLE NO. 312




**Four modes of testing can be obtained** by setting switches $S_2$ and $S_3$ in the four possible position combinations. Pushbutton switch $S_1$ starts the test cycle, which is then driven by the system clock.

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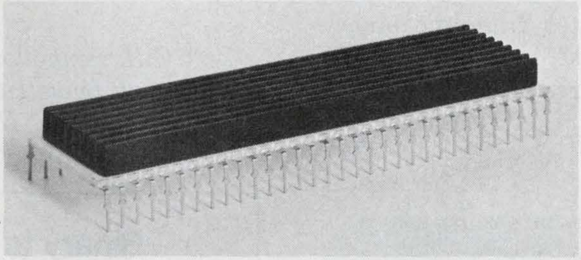

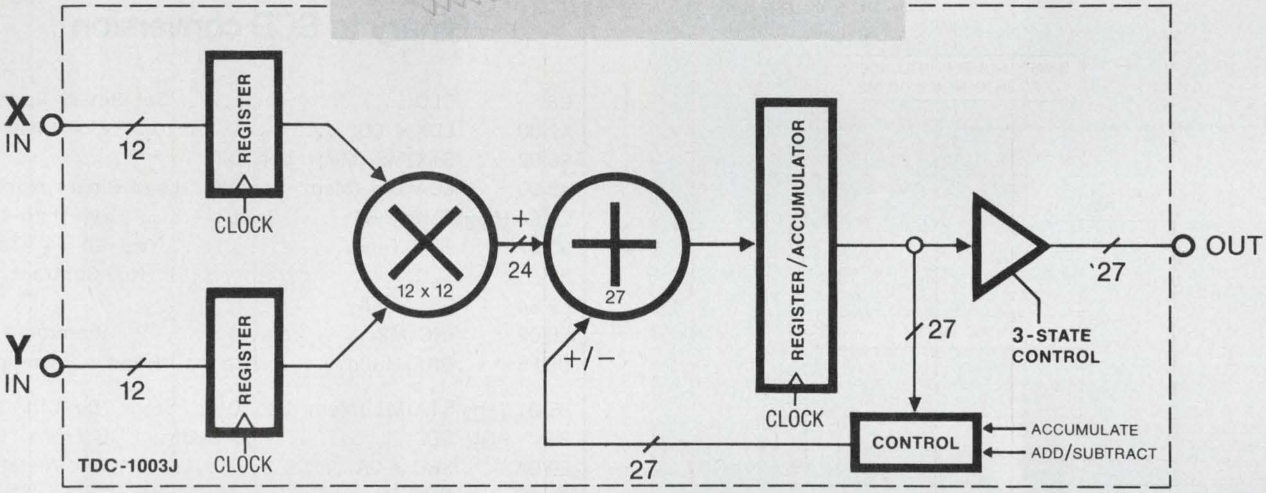


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# Binary-to-BCD conversion for $\mu$Ps packs the units and tens into one byte

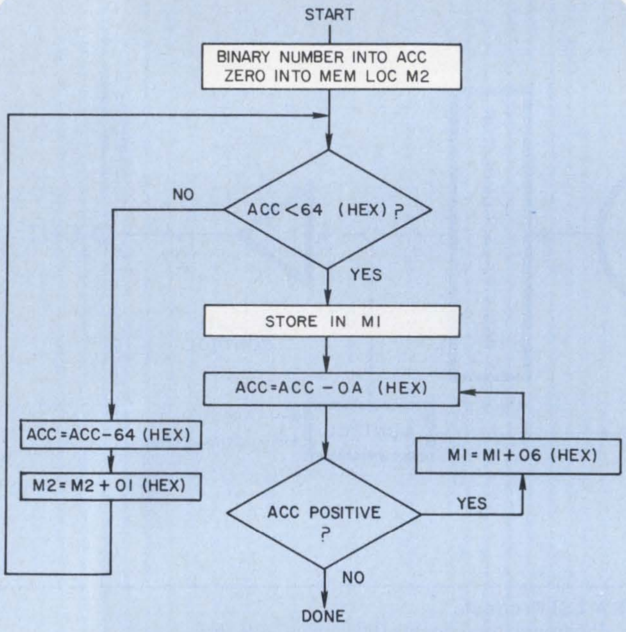
An assembly and machine-language program written for MOS Technology's 6502 $\mu$P converts 8-bit binary numbers into two BCD numbers. Also it stores the BCD tens and ones digits within one 8-bit byte of memory.

The general flow chart shown is applicable to most microprocessors. The first operation checks the binary number's value. If the number is 100 (64 hexadecimal) or larger, then 100 is subtracted from the binary number, and memory location $M_2$ is incremented by 1. This process repeats until the result falls below 100. If the maximum binary number never exceeds 99, this operation can be omitted.

If the binary number is less than 100, or becomes less than 100 in the first step, the program stores it in memory location $M_1$. This location is incremented by six for every 10 bits of the binary number. Upon completing the program loops, $M_1$ holds the tens and ones digits as two BCD numbers within one byte of memory, while $M_2$ contains the hundreds digit.

*Bert G.H. Penhollow, Manager of Electrical Engineering, Colt Industries, Quincy Compressor Div., 217 Maine St., Quincy, IL 62301.*

CIRCLE NO. 313




**When the binary-to-BCD conversion is complete, $M_1$ contains the tens and ones digits** within a single byte in BCD, while $M_2$ contains the hundreds digit.

## Binary to BCD conversion

```
D8          CLD...................... Set Binary Addition
A2 00       LDX # 00.......................... Clear M2
86 02       STX M2 (Mem. Loc. 02)
A5 00       LDA Bin (Mem. Loc. 00). Load Binary Number
C9 64 Hund  CMP # 64................... Less Than 100?
90 07       BCC Tens................ Yes, Go To "Tens"
38          SEC....................... No, Subtract 100
E9 64       SBC # 64
E6 02       INC M2....................... Increment M2
D0 F5       BNE Hund........ Go To "Hund", Recompare

85 01 Tens  STA M1 (Mem. Loc. 01).. Store "Bin" In "M1"
38    AGN   SEC................ Subtract 10 From "Bin"
E9 0A       SBC # 0A................. Is "Bin" Negative?
30 0B       BM1 Done............... Yes, Go To "Done"

AA          TAX.................................... No
A5 01       LDA M1
18          CLC
69 06       ADC # 06................... Add 6 To "M1"
85 01       STA M1
8A          TXA
D0 F0       BNE AGN.............. Loop Back To "AGN"

60    Done  RTS
```

**IFD Winner for June 7, 1977**

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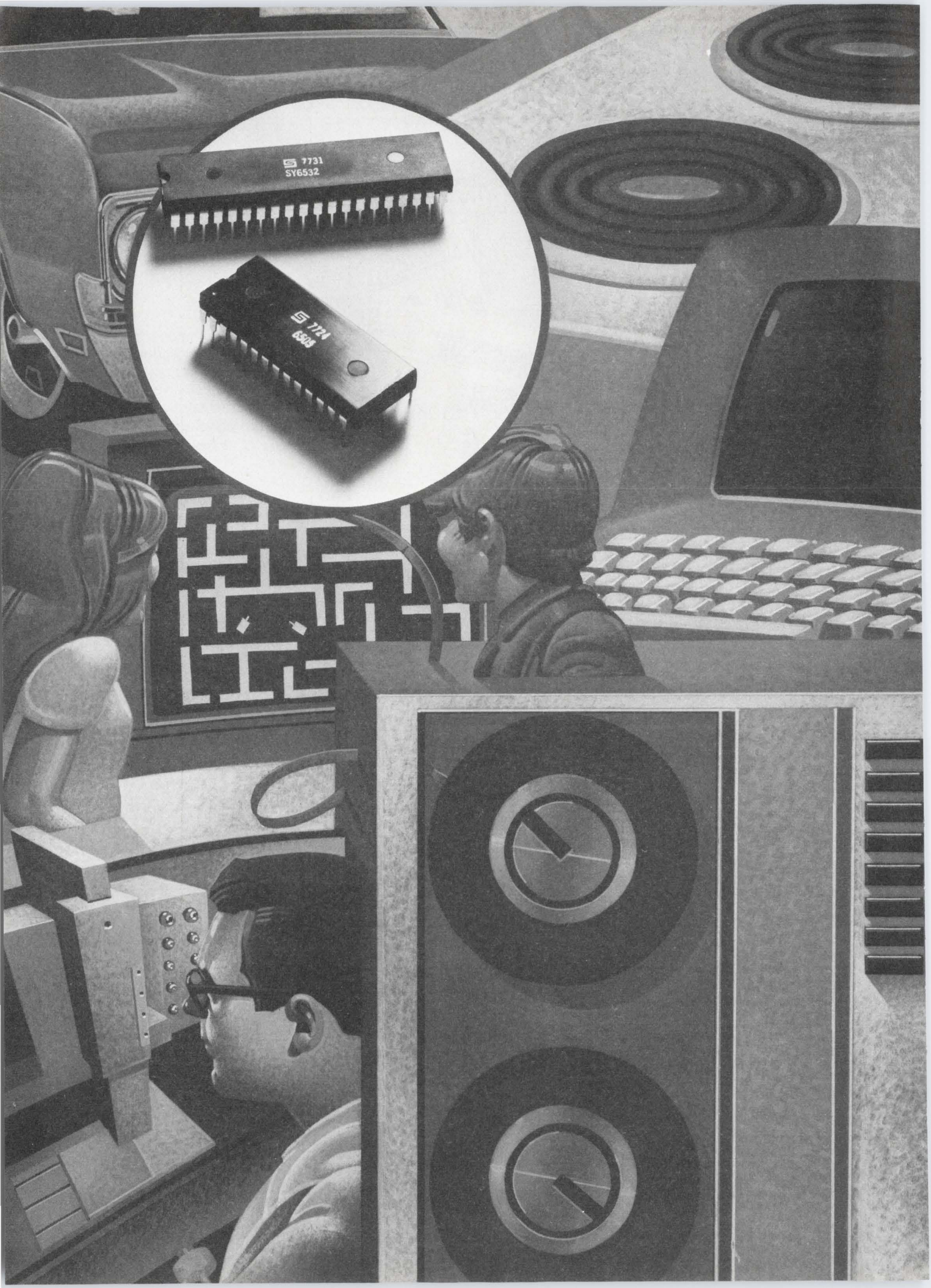
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## GaAs high-frequency performance gets a boost

A gallium-arsenide FET with substantially improved high-frequency performance has been developed by Hitachi's Central Research Laboratory in Kokobunji, Japan.

The high-frequency performance of a FET greatly depends on how small its gate length is. Earlier Hitachi GaAs FETs with submicrometer gate lengths operate with low noise at X-band frequencies. But the researchers who developed those FETs have upped the frequency with a technique called intentional side etching.

A gallium-arsenide FET with a gate length of only 0.5 $\mu$m, has an unusually low noise figure of 2.1 dB at 12 GHz, with 7.6 dB gain. So the device is suitable for operation at frequencies above X-band.

The new FET is formed on a high-purity, p-type buffer layer upon which is created, by vapor-phase epitaxy, an n-type active layer with a typical carrier concentration of 2 to $3 \times 10^{17}$ $cm^{-3}$. Source and drain ohmic contacts are formed on the n-type layer, and a gate region is etched. A titanium layer 0.15-$\mu$m thick is then evaporated and a layer of gold 0.4 $\mu$m thick is added.

A stream of argon ions then mill the gold layer, leaving only a gate pattern of gold, 1 $\mu$m long and 300 $\mu$m wide.

The titanium layer, whose milling rate is half that of the molybdenum used for the earlier devices, protects the GaAs layer from damage from the ion beam. The gate pattern is then protected by photoresist. The titanium layer is etched with hydrogen fluoride and nitric acid.

The effective gate length is determined by intentionally etching the side of the titanium layer. The etching rate is about 0.4 $\mu$m/min. The usual difficulties of etching titanium, which rapidly accumulates layers of surface oxide, are eliminated by the ion-milling process, which leaves the titanium with a clean surface. Consequently, the etching is easy to control, and 0.5 $\mu$m patterns can be reproducibly obtained.

## Data lines and points traced with thermal head

With a thermal writing head, a new system of producing chart-recorder traces can form data points and lines like those of pen recorders, but without the problems plaguing pen-and-ink mechanisms. The method results from a four-year development program at the Industrial Instruments Div. of Smith Industries, Ltd. in London. It can be adapted to microprocessor outputs that drive chart recorders capable of printing alphanumerics as well as conventional traces.

The thermal head is combined with thermally sensitive chart paper to produce multicolor traces. The head, a thin, multisegment line, is formed on a thick-film circuit and held in contact with the heat-sensitive paper by a free-floating roller.

The head is 256 mm (10 in.) long, with 250 writing segments on 1-mm centers. As a result, 250 points are produced along the writing axis of the recorder. Current pulses address the individual segments to raise the temperature of the paper at those points.

Color shades depend on how much thermal energy is coupled into the paper at the writing points. The chart paper is treated with a color-forming chemical and an acid coating. When a resistive writing point is addressed for a few milliseconds, the temperature rise mixes the chemicals and changes the color at that point. The color changes as the temperature rises. Temperature differentials of 30 C are sufficient to produce easily distinguishable color differences.

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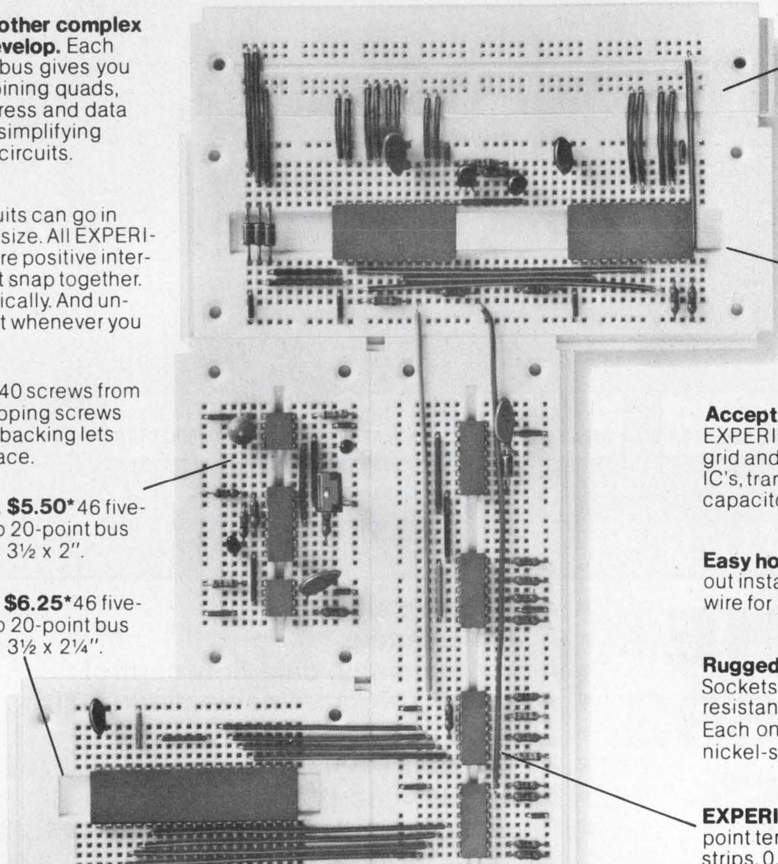

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†U.S. Patent No. D235,554

*Manufacturer's recommended resale.



CIRCLE NUMBER 123

# *New products*

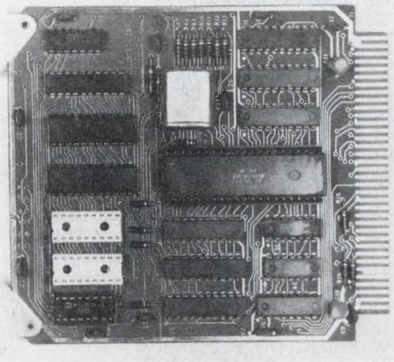
## EPROM programmer is accessory for MMD-1

*E & L Instruments, 61 First St., Derby, CT 06418. Richard Vuillequez (203) 735-8774. $222 assembled, $166 kit form.*

A programmer, MMD-PP, for the 1702A electrically-programmable and UV-erasable ROM is an accessory for the Mini-Micro Designer (MMD-1) training and development microcomputer. By sharing MMD-1 circuitry under the control of its PROM, the MMD-PP can program a 2048-bit EPROM in about 4 min. A 1702A EPROM inserted in an MMD-PP socket will accept data from any block of MMD-1 memory as well as any PROM designated as master. For convenience and speed, the data stored in any master can be transferred to a section of RAM within the MMD-1 for modification or editing before it is used to program a new EPROM.

**CIRCLE NO. 301**

## Central processing unit needs no support logic

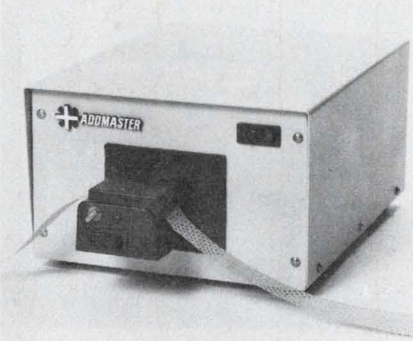


*MilerTronics, 303 Airport Rd., Greenville, SC 29607. Michael Webb (803) 242-9232. $275; 4 wks.*

Model PDC-100 is a SC/MP II central processing unit. It is self-contained and has on-board RAM and PROM and is able to run without any supporting logic or cards. It can also control memory and I/O cards in bus-type systems. Features are: SC/MP II CPU chip, 256 bytes of RAM, up to 1024 bytes of bipolar PROM, address decoder for system control, crystal controlled clock, 600 ns/microcycle, and 15-card fanout.

**CIRCLE NO. 302**

## Paper-tape reader has large capacity




*Addmaster, 416 Junipero Serra Dr., San Gabriel, CA 91776. (213) 285-1121. $625-$725.*

Model 612, a stand-alone paper-tape reader, has greater capacity than earlier models. Ability to read 5 to 8-level tape and to transmit 7 to 11 frames per character at 50 to 9600 baud are among the features. Others include starting and stopping on character at all speeds, choice of manual control or X-on, X-off, and even, odd or no parity. RS232, current loop or parallel outputs are available, as is a choice of desk-top or rack mounting.

**CIRCLE NO. 303**

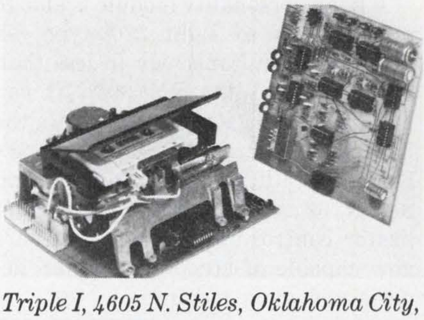
## Interactive computing done in a small system

*PolyMorphic Systems, 460 Ward Dr., Santa Barbara, CA 93111. Toby Bradley (805) 967-0468. From $3250.*

System 8813 is a compact complete disk-based microcomputer. The central unit includes 16 kbytes of RAM and room for three mini-floppy disk drives. Included in the package is a video monitor, keyboard with cable, and complete system software on diskette. Software allows the system to work immediately, running applications in either assembly language or in fully extended Basic. The high-speed video display exhibits produces graphics and alphanumerics.

**CIRCLE NO. 304**

## Read/write amps go with cassette transports

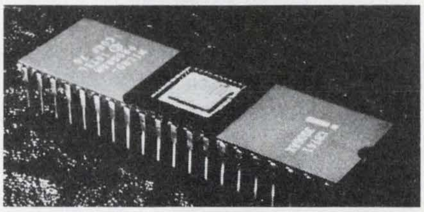


*Triple I, 4605 N. Stiles, Oklahoma City, OK 73118. (405) 521-9000. $119.50.*

Digital read/write amplifiers are available for the family of remote-controlled Phi-Deck cassette transports. They come in one or two channel versions, as well as read/write, read only, and write only. Reading or writing of 1600 flux reversals per inch densities can be done at tape speeds to 20 in/s. This allows data transfer rates of 16 kbit/s.

**CIRCLE NO. 305**

## Slave μC boosts processing power



*Intel, 3065 Bowers Ave., Santa Clara, CA 95051. Rob Walker (408) 246-7501. See text.*

Universal Peripheral Interface components, UPI-41, are single-chip slave microcomputers used to boost the processing power and control flexibility of 8-bit microprocessors such as the 8080A, 8085 and 8048. They are offered in two interchangeable versions along with an I/O expander. The 8041 UPI contains a mask-programmed ROM. The 8741 UPI contains an EPROM in place of the 8041's ROM, and is used to expedite system development. Each 8243 I/O expander unit contains 16 I/O lines. The 8741 is available from stock at a single unit price of $250, and the 8243 is $8 for a single unit in a plastic package. The 8041 is custom manufactured.

**CIRCLE NO. 306**

## Gang module programs eight 2708-type EPROMs

*Pro-Log, 2411 Garden Rd., Monterey, CA 93940. (408) 372-4593. $895; stock.*

A gang personality module is able to program up to eight 2708-type 8-k EPROMs simultaneously in less than 3 min. Called the PM 9051, it can program, duplicate, list and verify the EPROMs. It works with both Pro-Log's Series-90 PROM programmer and Series 92 PROM programmer/Duplicator control units. These units are now capable of accepting regular, generic and gang modules.

**CIRCLE NO. 307**

## Multiple port board has four serial interfaces

*Intel, 3065 Bowers Ave., Santa Clara, CA 95051. Rob Walker (408) 246-7501. $650 (unit qty); stock.*

Complete computer hardware systems with multiple communications channels can be built with two circuit boards. It's possible with the SBC 534 four-channel communications expansion board. The board adds four programmable serial data channels plus 16 lines of parallel I/O that interface a Bell Model 801 automatic calling unit or other RS-232C-compatible devices. The board measures 6.75 × 12 in. and plugs into a 0.5 in. SBC chassis card slot. All basic functions are software-programmable. Each data channel provides half or full-duplex operation and contains a programmable baud rate generator, programmable USART, RS-232C interface and sockets for optically isolated, 20-mA current loop interfaces. Operating modes (synchronous or asynchronous), data formats and other functions are also individually programmable. In addition, baud rates can be selected and changed with software. The rates are derived from an on-board crystal oscillator. Any frequency from 18.75 Hz to 614.4 kHz can be obtained by using the interval timers. Typical baud rates range from 4850 to 38,400 in the USART synchronous operating mode and from 75 to 9600 baud in the asynchronous mode. The board requires +5, +12, and −12 V supplies and draws 1.9 A, 275 mA and 250 mA, respectively.

**CIRCLE NO. 308**

## Programmable calculator has full program editing


*Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, CA 94304. (415) 493-1501. P&A: see text.*

The HP-29C, a handheld calculator, features 98 fully merged program steps, which typically hold 175 separate operations. It also has full program editing functions and continuous memory. Priced at $195 it offers three subroutine levels, 10 addressable labels, indirect addressing, and insert/delete editing. The 29C also is equipped with the standard programming functions of backstep, single step, pause, and a total of 10 decision tests. The continuous memory feature makes possible virtually permanent storage of the user's program. CMOS memory chips allow programs and data to be retained in memory for long periods after the calculator has been turned off, with little battery drain. The HP-29C comes with a 204-page owner's handbook, as well as a separate 164-page applications book.

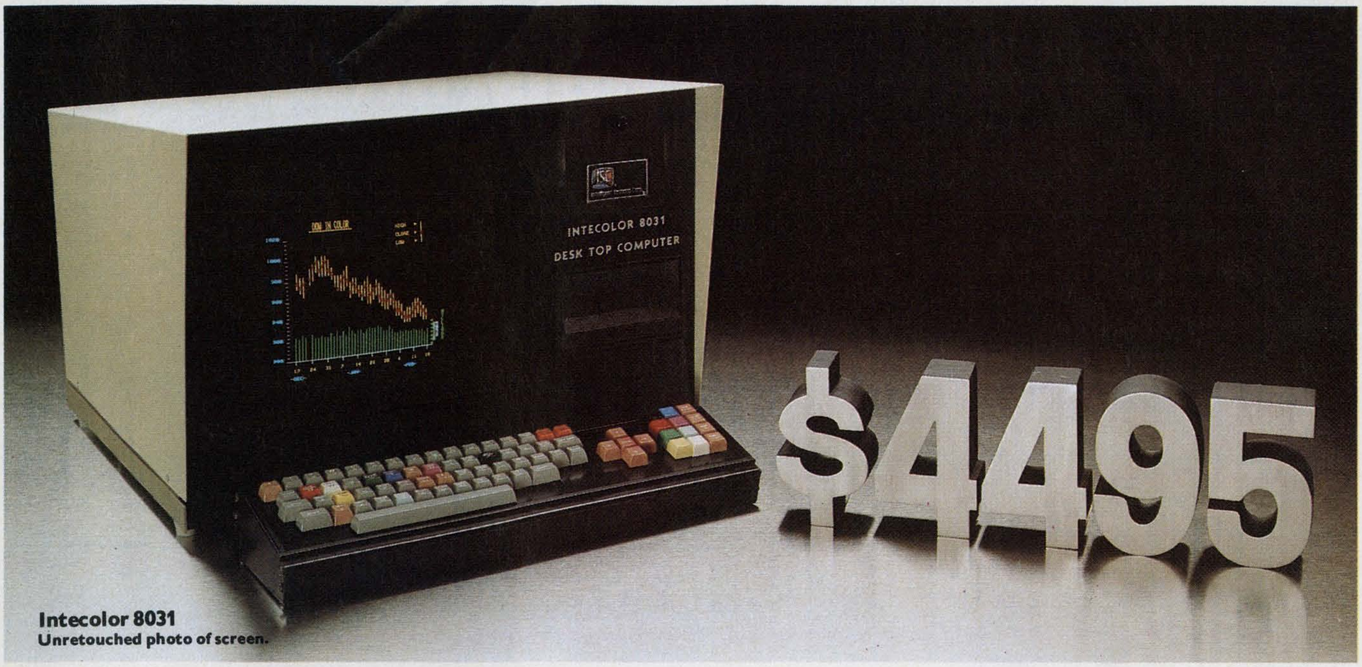
**CIRCLE NO. 309**

## Develop and debug Z80 programs for μCs

*Zilog, 10460 Bubb Rd., Cupertino, CA 95014. Dave West (408) 446-4666. $2850.*

The Z80-PDS program development system provides complete support for developing and debugging Z80 microcomputer programs. The standard unit includes a floppy-disc drive with up to 300 kbyte of on-line data storage, internal memory of 3 kbyte of PROM and 16 kbyte of RAM, and serial I/O with RS-232 or strappable current loop interface. It is expandable via options to provide additional I/O or terminal capability and can also be used as a general-purpose computer.

**CIRCLE NO. 310**




**Intecolor 8031**
**Unretouched photo of screen.**

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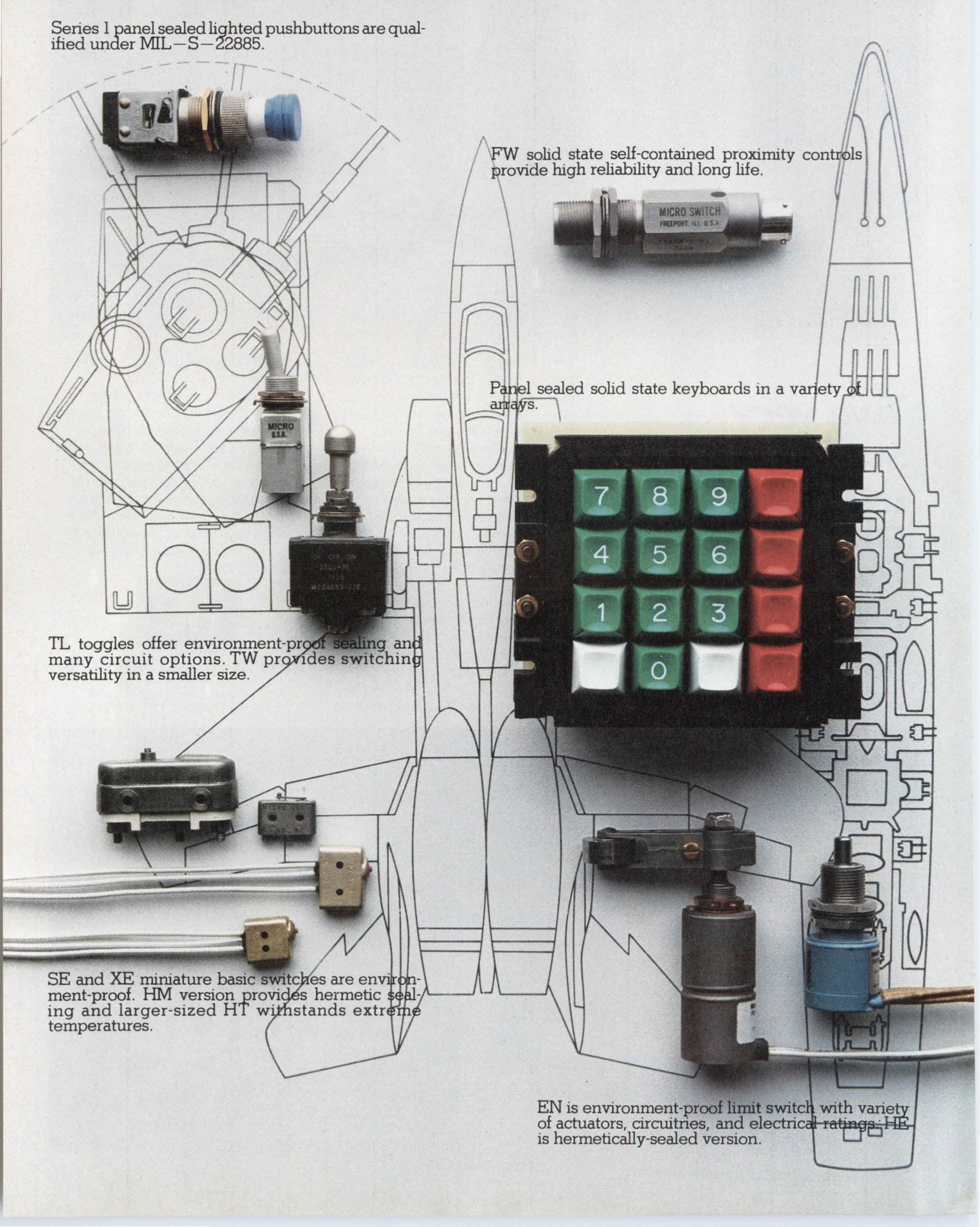
**Intecolor 8051**
**Unretouched photo of screen.**

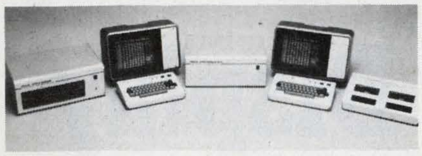


CIRCLE NUMBER 124

# How to defend against attack by air,



## Two engineers can work on dual microcomputer



*Futuredata Computer, 11205 S. La Cienega Blvd., Los Angeles, CA 90045. Bob Scharf (213) 641-7700. $5850; 4 wk.*

Microsystem 10/10 consists of two complete tape-based systems including two high-speed CRTs, two keyboards, two dual-tape units, operating software and manual. Each operator has full access to the system's editing, debugging and assembling capability. One half of the system can be dedicated to 8080; the other to 6800 or Z80 and either operator can switch processors by changing PC boards. The system provides two 8-in. floppy-disc based systems, each with 16 kbyte of RAM.

**CIRCLE NO. 314**

## Portable terminal system has built-in LINC tape

*Computer Operations, 9700 B Palmer Highway, Lanham, MD 20801. Michael Keating (301) 459-2100. $3850 (unit qty); stock.*

The Serial Box, a portable, interactive terminal, can interface to any mini/microcomputer via an RS-232 or current loop port at selectable data transmission speeds from 110 to 9600 baud. The Model CO-4420 consists of a 1 Mbyte direct-access LINC tape drive, a full ASCII keyboard, a 40-character plasma display, an RS-232 port and a microprocessor controller, all contained in a 23-lb case. Also available without display or keyboard the unit adds direct-access mass storage capability to any system via a second RS-232 or current-loop port.

**CIRCLE NO. 315**

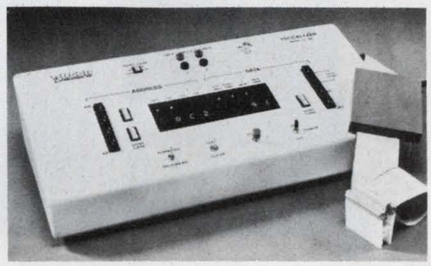
## 4-bit microcomputers are for consumer products

*NEC Microcomputers, 5 Militia Dr., Lexington, MA 02173. (617) 862-6410. $2 to $8 (large qty); stock.*

There are 4 members in the uCOM-4 family of 4-bit LSI microcomputers. Each member includes an ALU, user-specified masked ROM, RAM, and multiple I/O lines. ROM capacity ranges from 640 x 8 bits to 1920 x 10 bits. Each type has a powerful applications-oriented instruction set with multi-function instructions.

**CIRCLE NO. 316**

## Microprocessor analyzer handles 8080 and 6800 $\mu$Ps



*Yucca International, 14415 N. Scottsdale Rd., Scottsdale, AZ 85260. (602) 991-1491. $875; 30 days.*

The YA-20, a $\mu$P logic analyzer, is intended to help debug systems using 8-bit processors like the 6800 and 8080. Up to 128 30-bit data words can be trapped and stored at any address, data or user input in the program. The YA-20's selective trapping feature permits "write only" selection and VMA selection for 6800 $\mu$Ps; DBI for 8080s. A stepping switch and forward-reverse switch allow instructions to be read a data word at a time (32 words back, 96 words ahead) on hexadecimal LED displays. User inputs and MPU status are reported by LED indicators. Data trapping can be delayed up to 256 times past trigger point using the units pass counter feature. Trigger can be generated by a selected address on the bus, by a selected data word, by any combination of address, data or external inputs, or an external trigger can be used. "Don't care" selection switches are provided for all address, data and user inputs. A BNC connector allows optional scope display synchronized by the analyzer. A clip-on probe, provided for either 6800 or 8080 $\mu$Ps at no extra cost, has a 10-M$\Omega$ input impedance. Probes for other $\mu$Ps are available. Housed in an 18 × 9 × 4 in. metal cabinet, the VA-20 needs only 115 V ac to operate.

**CIRCLE NO. 317**

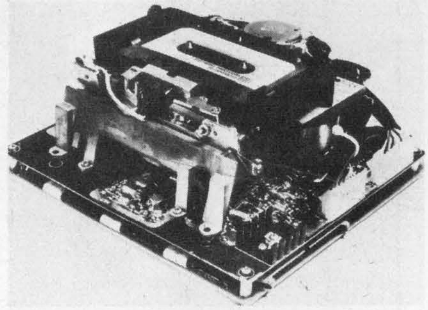
## Memory emulation unit programs and debugs

*M&E Assoc., 10439 N. Stelling Rd., Cupertino, CA 95014. Michael Maples (408) 739-5168. $5995; 30-60 days.*

A Z80 based development system combines the power of a special assembler with a memory emulation module. The assembler allows the insertion of any instruction mnemonic, including multibyte instructions, like those of the Z80. The assembler's symbol table can be set for an 8080, F80, 6800, F8 and 6502, to generate the appropriate code. The object code is loaded into the emulator memory space where it can be executed by the target processor. Any target microcomputer system with a standard 2708 EPROM can be programmed and debugged using breakpoints. Once a program is debugged the EPROM can be debugged via an RS232 link.

CIRCLE NO. 318

## Cassette storage system handles over 1 Mbyte



*Triple I, 4605 North Stiles, P.O. Box 18209, Oklahoma City, OK 73118. Jack Morrow (405) 521-9000. For one transport and controller: $375 (unit qty); stock.*

The GCR cassette system is a magnetic tape data storage and retrieval system. It can control up to four of the company's Phi-Deck cassette transports and access any of over one million 8-bit bytes within 20 seconds. Each deck is fully controlled to prevent tape breakage. A 4 to 5 bit translation scheme, called Group Coded Recording, allows higher packing densities with a soft error rate of less than one bit in $10^8$. This system operates at 1600 flux changes per inch, yielding a data transfer rate of 800 bytes per second at a tape speed of five inches per second.

CIRCLE NO. 319

## Electrostatic printer also does graphics

*Axiom, 5932 San Fernando Rd., Glendale, CA 91202. Simon Harrison (213) 245-9244. $795 (unit qty); 30 days.*

The EX-810, a full-graphics plotter, can print 8192 dots per second with up to 512 dots per row. It can also function as an 80 column alphanumeric printer with a speed of 160 characters per second. Specifically designed to be driven by an 8-bit $\mu$P with a minimum software overhead, the unit is equipped with a TTL compatible controller which takes care of all the internal timing functions necessary to drive the printhead and advance the paper. Printout is initiated by a single input command, which causes an 8-track nonimpact printhead to move across the printing field in about 240 ms with a speed uniformity better than 0.1%. Margin and printhead position marker signals are fed back to the user's microcomputer and may be used to synchronize an 8-bit scanning raster to the printhead driver input. The uniform speed of the printhead also allows the user to vary the horizontal dot resolution by generating an external timing cycle for the input raster. A complete self-contained unit with case, power supply, paper holder, infrared low-paper detector and bell, the EX-810 measures just 9.625 × 4 × 10.875 in. and weighs 12 lb (with 240 ft roll of 5 in. wide electrosensitive paper).

**CIRCLE NO. 320**

## Prototyping tool makes development easy

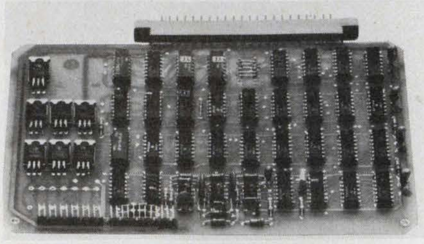
*RCA, Box 3200, Somerville, NJ 08876. (201) 685-6423. $2900.*

An interactive prototyping tool, CDP18S005, facilitates the development of software and hardware using the RCA 1800 family of microprocessors. The system uses a CPU and includes a RAM resident editor and assembler. Space is available for additional I/O devices. Also included are power supplies, clock, controls, display, and seven plug-in PC modules containing a CPU, control, address latch and bank select, 4-kbyte RAM, ROM/RAM, I/O decode and terminal interface. Only a data terminal is needed to make the system operational.

**CIRCLE NO. 321**

# How to get more mileage from discrete components.

## Printer controller handles 15 column copy



*Sheldon Sodeco Printer Corp., 4 Westchester Plaza, Elmsford, NY 10523. Peter Engstron (914) 592-4400. $180 for the controller (unit qty), $104 for the PR1501 (100 qty); stock.*

A printer control interface, Model 4-621-9200, is designed for use with the company's PR1501-01 alphanumeric impact printer. The printer can produce 15 columns, in two colors, at speeds up to 90 lines per minute. The interface, assembled on a 5.5 × 7.5 printed-circuit board accepts an ASCII input code and provides a 15-column line buffer, ROM character generator, timing control, and solenoid drive circuits to completely control the PR1501 printing mechanism. Input commands for start load, load data, busy, start print, paper feed and ribbon shift are provided by the interface. Units are supplied with an edge connector and complete documentation.

CIRCLE NO. 322

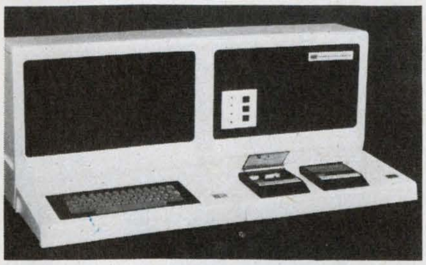
## Mass memory system holds up to 14 Mbits

*Monolithic Systems, 14 Inverness Dr. East, Englewood, CO 80110. Robert Billhimer (303) 770-7400. P&A: See text.*

A 14 Mbit semiconductor RAM memory, contained in a 5.25 in. high RETMA rackmount chassis is designed around 16 k dynamic RAMs. The MSC 2601 contains its own power supplies, forced air cooling, and cards for timing and control, address buffer, and termination and register. Bit lengths of the memory array cards can be arranged to meet the requirements of the user. Addressing, data input and data output buses are arranged to permit addressing up to eight, 768 kword modules. The MSC 2601 is priced at less than 0.25¢/bit in OEM quantities and delivery with a custom-designed I/O is 45 days.

CIRCLE NO. 323

## Micro system needs no professional programmer



*Information Control, 9610 Bellanca Ave., Los Angeles, CA 90045. (213) 641-8520. $4875-$6950.*

A system designer's task is simplified by the use of the Micro-Command system. Unique features are: complete hardware/software package for development of either 8080 or Z80 based systems without CPU change; light pen for interactive I/O; "menu-oriented" software. The lower-cost option has dual-cassette tape storage.

**CIRCLE NO. 324**

## Controllers for diskette drives handle 2 Mbytes

*Intel, 3065 Bowers Ave., Santa Clara, CA 95051. Rob Walker (408) 246-7501. $1290 (unit qty); stock.*

A self-contained, programmable controller, the SBC 202, handles up to 2 Mbytes of floppy-disc mass storage. The controller interfaces SBC 80 Single Board Computers and System 80 packaged OEM computers with most types of double-density diskette drives. Multiple SBC 80 and System 80 computers can share mass storage resources and process concurrently. Moreover, multiple controllers can be used on the Multibus. Major features of the SBC 202 include: direct memory access, complete cyclic redundancy checking, recording in a high-density, soft-sectored format, and pre-programmed to simplify computer programming. The recording format allows up to 500 kbytes to be stored on each diskette and the controller can handle up to four drives. Two 6.75 × 12-in. boards are needed to build the controller: A channel board, containing an 8-bit bipolar processor, decodes commands, fetches parameters from system memory, and controls the operations. And an interface board handles communications between the drives and central processor, and implements all DMA and CRC operations.

**CIRCLE NO. 325**

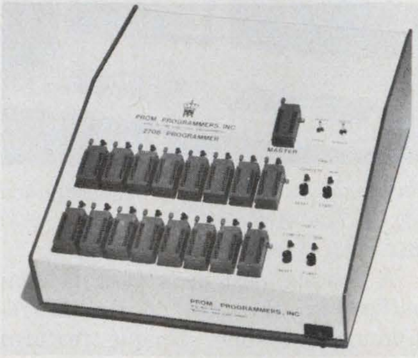
## Hand-held terminal interfaces μCs

*RCA, Box 3200, Somerville, NJ 08876. (201) 685-6423. $140.*

Packaged in the size and shape of a pocket calculator, the Microterminal CDP18S021 is a low-power, nonhard-copy alternative to the conventional teletypewriter data terminal. It provides a convenient means of controlling a COSMAC microprocessor-based system, reading and modifying memory, and providing hexadecimal I/O capability. It is suited for use with the COSMAC evaluation kit CDP18S021 or the development system, CDP18S005. But it can be designed into user-built systems to provide control, communications and debugging functions.

**CIRCLE NO. 326**

## 16-gang programmer can verify PROMs



*PROM Programmers, 601 Nandell Lane, Los Altos, CA 94022. (415) 948-0450. $2995; 30 days.*

A 16-gang programmer programs and verifies PROMs of the 2708 or 2716 families. It will program the first tier of eight sockets while loading the second row and then program the second row while unloading and loading the first. A toggle switch allows all 16 sockets to be programmed at the same time.

**CIRCLE NO. 327**

## Fortran compiler is made for minifloppy/μC

*GNAT Computers, 7895 Convoy Ct., San Diego, CA 92111. Frank Adams (714) 560-0433. $3990 (system); stock to 30 days.*

A Fortran compiler is available for the GNAT minifloppy/microcomputer system. The compiler includes all ANSI standard Fortran, X3.9-1966, except for double precision and complex numbers. A relocating assembler, a linking loader, and the Fortran library are included. The Fortran functions are implemented with 32-bit floating-point arithmetic. Integers are implemented with 16-bit numbers. The system includes a 1.3-μs CPU, 32-k RAM, 2-k PROM on 16-k ROM module, serial/parallel I/O, disk interface and control, front panel, and minifloppy disk drive.

**CIRCLE NO. 328**

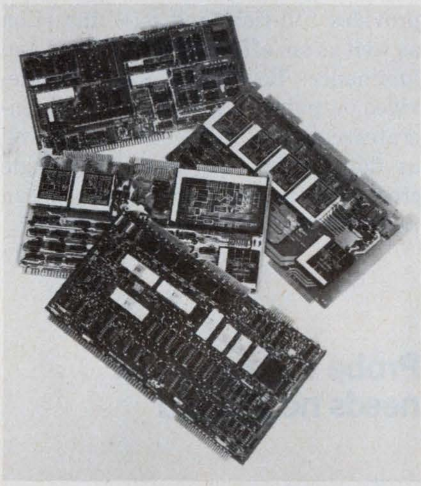
## $\mu$P controller allows high speed plotting

*Zeta Research, 1043 Stuart St., Lafayette, CA 94549. Ralph Manildi (415) 284-5200. $2500; 30-45 days.*

A microprocessor interface (MPI) controller, model MPI-DGV, plugs directly into a minicomputer's backplane and does much of the computer's work using Zeta's Graphic Machine Language (GML) software. The combined effort of this distributed computing allows high speed plotting, with minimal host CPU time at the computer's lowest priority, with any Zeta plotter.

**CIRCLE NO. 329**

## Analog boards for SBC-80 systems need just 5 V



*Intel, 3065 Bowers Ave., Santa Clara, CA 95051. (408) 246-7501. From $395 to $1125; stock.*

Three analog I/O subsystems and an optically isolated digital I/O subsystem have been added to the SBC-80 single board computer family. The SBC 732 analog combination I/O board, contains 8 differential/16 single-ended analog inputs (expandable to 16/32 inputs) and two digital-to-analog conversion channels; the SBC 711 analog input-only board, has the same number of inputs as the SBC 732's input section; the SBC 724 analog output-only board, offers four d/a converter channels; and the SBC 556 optically isolated I/O board, contains digital interfaces for 48 I/O lines and sockets for the user's choice of opto-isolators, drivers and terminators. All plug-in boards are 6.75 × 12 in. and operate from a +5-V power supply.

**CIRCLE NO. 330**

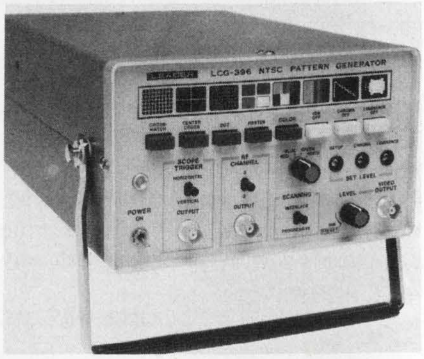
## Process control system is $\mu$P based

*Digitek, 5950 6th Ave. S., Seattle, WA 98108. Frank Mauger (206) 762-3933. $15,000; 12 to 16 wk.*

A microprocessor-based process control system includes a complete software package for supporting up to 16 control loops and 16 additional inputs with alarm limits. Programming is done in Basic with some subroutines written in assembly language. Features include manual or automatic mode operation, flow totalization, cascade effect, high and low alarms for limit detection and trend logging and display.

**CIRCLE NO. 331**

## Color-pattern generator provides all TV signals




*Leader Instruments, 151 Dupont St., Plainview, NY 11803. Pat Redko (516) 822-9322. $900.*

The LCG-396 color-bar generator provides all signals necessary for testing or aligning any TV equipment. It provides full-field and IQW insertion as well as on/off control of chrome and luminance. Both fixed and variable-video outputs are available and it generates eight precision color bars as well as dot, crosshatch, centerline single crosshatch and white, red, blue, green rasters.

CIRCLE NO. 332

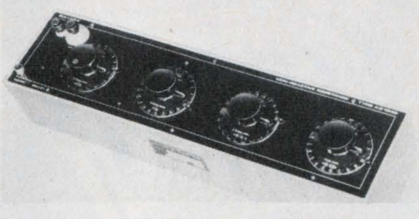
## Probe voltage tester needs no ground


*Mono-Probe, 5471 Huntington Dr., Los Angeles, CA 90032. Dan Tucker (213) 222-7222. $39.95.*

Hand-held, with a single probe, the Trouble Shooter tester detects 120, 240 and 480 V and produces both light and sound signals. An auxiliary probe allows continuity testing.

CIRCLE NO. 333

## Resistance box offers 0.005-Ω resolution



*James G. Biddle, Plymouth Meeting, PA 19462. (215) 646-9200. $280-$345.*

High resolution of 0.005 Ω is obtained with the ac/dc decade resistance box. Features include: silver-faced contacts with laminated-copper brushes, very low self-inductance and capacitance, and full shielding. Seven models are available, two with steps of 0.005 Ω.

**CIRCLE NO. 334**

## Hf receiver tunes the 5-kHz to 30-MHz range

*Watkins-Johnson, 700 Quince Orchard Rd., Gaithersburg, MD 20760. (301) 948-7550.*

Featuring a seven-digit LED-readout display, the WJ-8718 hf receiver tunes across the 5-kHz to 30-MHz range in four switch-selectable steps. A built-in frequency synthesizer provides 10 Hz of resolution over the entire range. It can detect AM, FM, CW, ISB, LSB, and USB emissions. Five i-f bandwidths cover 0.3 to 16 kHz and are front-panel selectable.

**CIRCLE NO. 335**

## Rf field measures silicon-wafer resistance

*ADE, 127 Coolidge Hill Rd., Watertown, MA 02172. Virginia Regal (617) 923-2180. $5360; stock.*

Slice resistivity of silicon semiconductor wafers are measured by the 6035 MicRhoSense, a noncontact gauging system using an rf field. Readout is metric or English and separate high/low LEDs can be set for production sorting. Resistivity range is 0.001 to 99.9 Ω-cm.

**CIRCLE NO. 336**

## Power meter provides accurate rf measurement

*Narda Microwave, Plainview, NY 11803. (516) 433-9000. $425.*

Having a 30-dB dynamic range, the hand-held, battery-operated power meter makes accurate measurements in the 10-MHz to 13.7-GHz range. The Model 8401 is available with interchangeable 50-Ω mounts covering a full-scale power range of 0.1 to 100 mW. Also available is a 75-Ω mount for CATV use with a range of 1 to 10 mW. Full scale accuracy is ±3%.

**CIRCLE NO. 337**

*COMPONENTS*

## Hall-effect switch replaces mechanicals

*Texas Instruments, P.O. Box 5012, Dallas, TX 75222. Dale Pippenger (214) 238-3527.$0.36; stock.*

A bipolar magnetically activated switch, the TL170 uses the Hall effect for sensing a magnetic field. It performs electrical switching with hysteresis. Operation is with an input magnetic field of 700 Gauss and it provides a switching hysteresis of 200 Gauss. Action is bipolar with minimum field density of ±350 Gauss over 0 to 70 C.

**CIRCLE NO. 338**

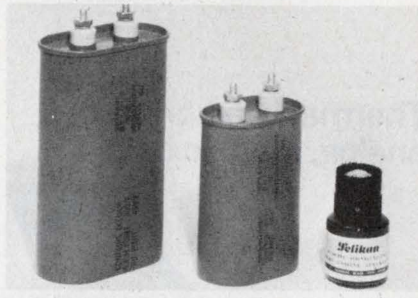
## Freq-sensitive relay accepts any waveshapes


*Solid State Electronics, 15321 Rayen St., Sepulveda, CA 91343. Edward Politi (213) 785-4473.*

Contacts on the Model-471 frequency-sensitive relay will pull in when the input frequency is within ±5% of the specified value, regardless of wave shape. Sine, square, triangular waves, and pulses will actuate the device, which comes in versions from 50 Hz to 100 kHz. The contacts are an isolated spdt, form-C reed relay rated at 0.25 A, 28 V dc, 3 W max. A screwdriver adjustment is provided for fine setting of the closure frequency. Power-supply requirements are 28 V dc at 20 mA, and the operating temperature range is from −30 to +80 C. Hermetic sealing of the can allows the unit to operate in 100% relative humidity environments up to 90 C. The relay was designed to meet the requirements of MIL-E-5272.

**CIRCLE NO. 339**

## Ecologically sensitive? Use this capacitor

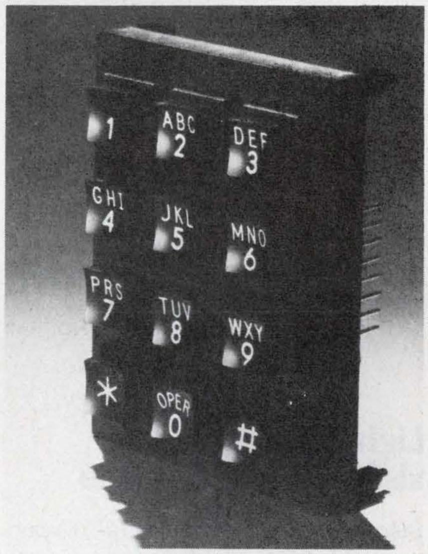


*Sprague Electric, North Adams, MA 01247. (413) 664-4411.*

Commutating capacitors, designed for ecologically sensitive applications, use a nontoxic biodegradable impregnant having a flash point of 430 F. The 365P paper capacitors are rated at 200 and 300 V ac and the 366P dual-dielectric, paper-polypropylene types are rated at 400, 500, 700 and 800 V ac.

**CIRCLE NO. 340**

## Look-alike keyboard matches Bell models

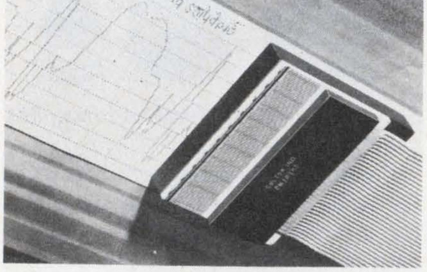



*Chomerics, 77 Dragon St., Woburn, MA 01801. Rick Seeger (617) 935-4850. $2.00 (OEM-qty).*

Western Electric's standard Touch-Tone keyboard is duplicated by the model-LT telephone keyboard. Key centers of 0.66 in., 10-12 oz. operating force and 0.125 in. key travel exactly match Bell System models. The units also feature built-in overtravel and mechanical hysteresis. Available with single-pole or Touch-Tone row/column encoding, matrix encoding can be provided with either one or two commons, or with none. Termination is by means of a flexible tail, or cylindrical pins that accept a variety of connectors and allow soldering.

**CIRCLE NO. 341**

## Thermal head prints analog, graphic data



*Gulton Ind., 212 Durham Ave., Metuchen, NJ 08840. (201) 548-2800. $75.75 (100-499 qty); stock-8 wks.*

Thick-film, dot-matrix thermal printheads allow simultaneous printing of analog, graphic and alphanumeric data. Each printhead in the DM10101 contains 101 dot elements, with the 101st dot used for applications requiring both a zero and 100th data point. The DM1099 contains 99 dot elements and is used with the DM10101 for data expansion. Fixed-head operation makes possible the design of graphic printers with higher speed and simpler mechanisms than conventional moving head printers. The units are supplied with a soldered cable and are mounted onto a standard Gulton heatsink for ganged operation.

**CIRCLE NO. 342**

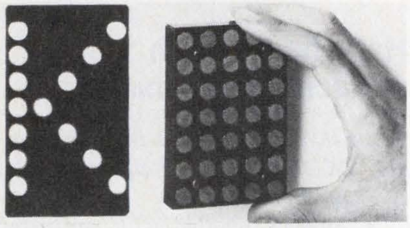
## Light-pipe digit LEDs visible over wide angle

*Litronix, 19000 Homestead Rd., Cupertino, CA 95014. Dick Tetschlag (408) 257-7910. $1.25/digit (1000-qty); stock.*

Using light-pipe digits, the DL-700 LED displays are visible over a viewing angle of nearly 180°. Available in 1, 1-½ and 2-digit DIPs, the units use 0.5-in. LED digits. Also available are 2 to 6-digit modules with PC board edge connectors. All displays operate from 5-V dc, feature a decimal point after each digit, and have common-anode or common-cathode terminals. DIP-packaged digits can be butted end to end to create displays of any length with equal spacing between digits. Units come with either a red plastic cap or a clear plastic cap suitable for use behind a transparent red window.

**CIRCLE NO. 343**

## LED-matrix display is easily readable

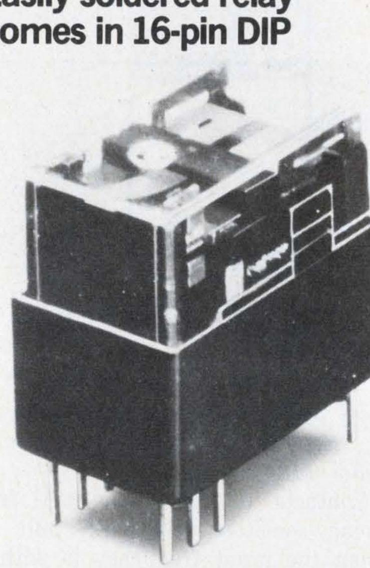


*Chicago Miniature Lamp, 4433 N. Ravenswood Ave., Chicago, IL 60640. George Neeno (312) 784-1020. $60/1, $40/100; stock.*

The Datablox display generates 4 × 3-in. alphanumeric digits and uses 35 high-intensity LEDs mounted in individual reflectors. The digits have a brightness and visibility, with wide-angle viewing, which make them readable at distances of 2 00 ft in normal office lighting. Compatible with solid-state drives, they are ca pable of generating the full 64-character ASCII set. They are offered in red and yellow.

**CIRCLE NO. 344**

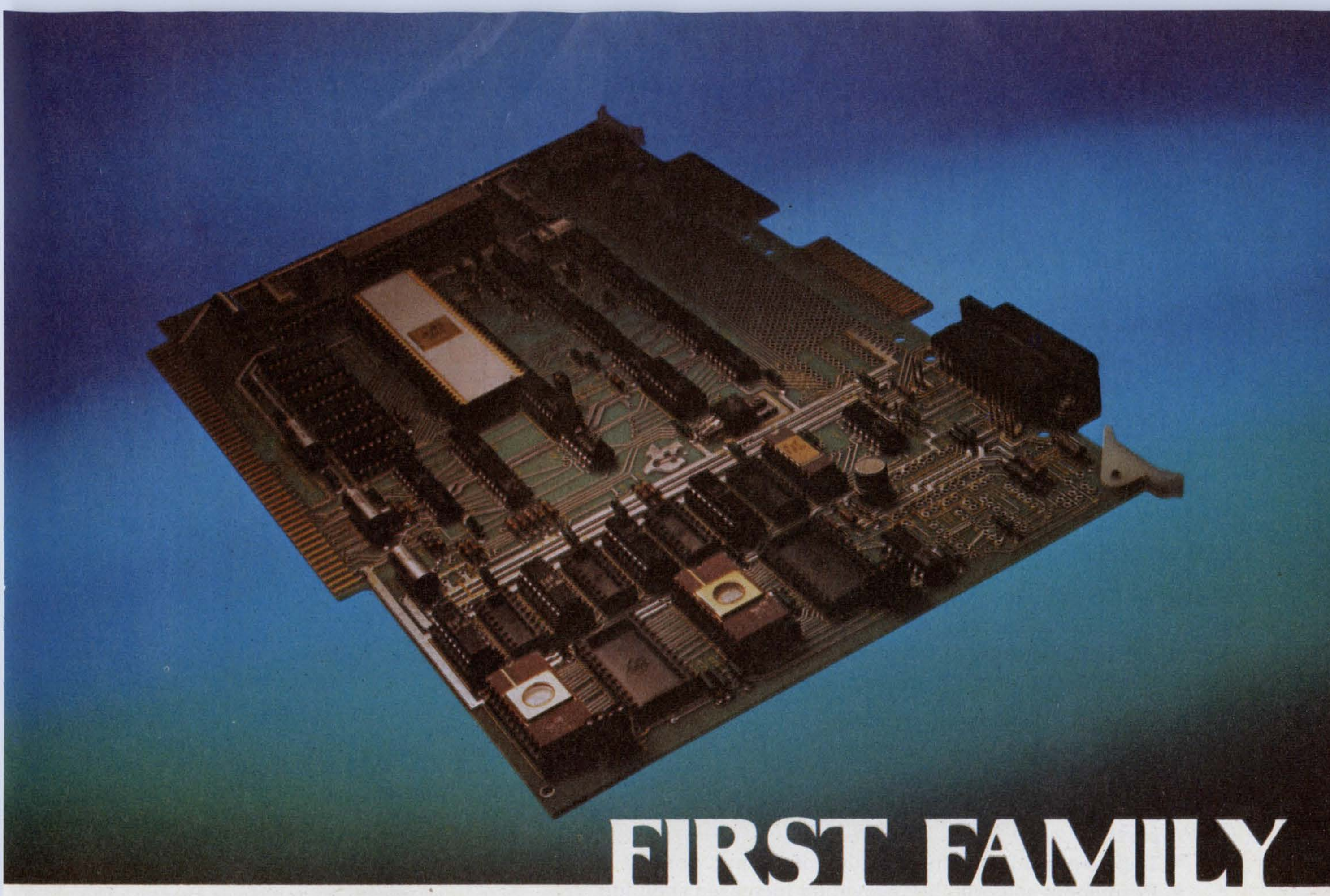
## Easily soldered relay comes in 16-pin DIP



*Arrow-M, 250 Sheffield St., Mountainside, NJ 07092. (201) 232-4260. $0.75 (1000-qty); stock-90 days.*

Molded construction in the HB-series miniature relays prevents solder-flux inflow to the mechanism. Packaged in a DIP-matching 16-pin IC socket, the mechanism contains only 7 parts. Operating power ranges from 230 to 360 mW in units containing a 1C contact arrangement, and from 370 to 576 mW for 2C contact units. The devices are rated 125-V ac, 30-V dc and can switch a maximum of 2A. Mechanical life of the silver-nickel contacts is rated at 10-million operations.

**CIRCLE NO. 345**




# First low-cost, 16-bit μP modules. For OEMs. From Texas Instruments.

The new TM 990 Series from Texas Instruments. Fastest, easiest way to get a microprocessor-based design to market. Ideal for μP evaluation. And a cost-effective production alternative.

First in TI's new series: TM 990/100M. A TMS 9900 microprocessor, I/O circuits, 1K x 16-bit EPROM and 256 x 16-bit RAM on a single 7½" x 11" board. Pretested and ready to go.

The EPROM, which includes a self-contained software monitor (TIBUG™), is expandable to 4K x 16 bits. The RAM to 512 x 16 bits. Also on board: 16 lines of programmable parallel I/O, TTY current loop or RS 232 terminal interface. Two programmable interval timers; 15 external hardware interrupts. Plus a user prototyping area. All control, address and data lines are fully available to facilitate expansion to extremely large systems.

**Leadership price**

At a single unit price of $450.00, the TM 990/100M is an economical means for checking out what TI's 9900 microprocessor can do. And at a 50-piece price of $315.00, it is attractive for production runs.

**More modules coming**

A TMS 9980-based CPU module. A ROM/RAM memory expansion module. An I/O expansion module. A microterminal for data entry/display. A line-by-line assembler in EPROM.

**9900 First Family compatibility**

The TM 990 Series modules are supported by the new advanced AMPL™ software development system. And are fully compatible with all members of TI's 9900 First Family. So you can move to the TMS 9900 components level. Or to TI's 990/4 microcomputer. Easily. Economically.

**Order the TM 990/100M today** from your TI distributor. Or for details, write Texas Instruments Incorporated, P.O. Box 1443, M/S 653, Houston, Texas 77001.

TEXAS INSTRUMENTS

INCORPORATED

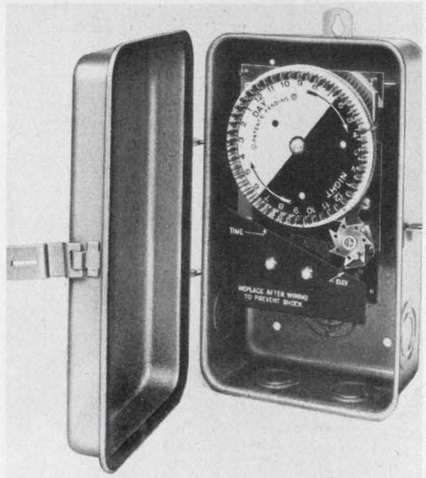
CIRCLE NUMBER 139



93141

*COMPONENTS*

## Synchronous motor drives program time switch



*Zenith Controls, 830 W. 40th St., Chicago, IL 60609. (312) 247-6400.*

The synchronous-motor-driven 2400 program time switch provides 24-h on-off control for electrical equipment. A 24-h dial includes 96 self-contained clips for on-off operation in 15-min increments, or multiples thereof. The UL listed timer has an spdt snap-action contact rated at 20 A, noninductive to 480 V ac. Available is a time delay option which provides a 0-2 min. adjustable delay for staggered starting of heavy loads. A snap-in bracket is supplied for panel mounting, or in an enclosure. Dimensions are 6-½ in (W), 9-⅜ in. (H), and 3-¾ in. (D).

CIRCLE NO. 346

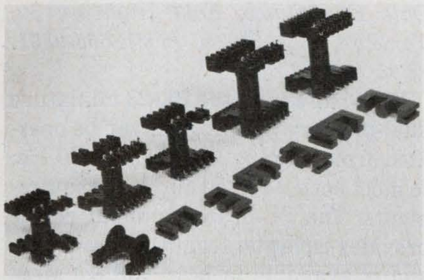
## Photoelectric controls offer plug-in functions

*Autotron, 3629 N. Vermilion, Danville, IL 61832. (217) 446-0650.*

Compact self-contained LED photoelectric controls, the R series, feature a variety of plug-in function cards to control or alter logic functions. Also available as a plug-in is a 10-A DPDT relay. The complete retroreflective control unit with recessed glass lens is housed in a 57-in³ package. Shielding from electrical noise is provided by a die-cast aluminum case that is gasket sealed. The units can operate over a distance of 35 ft and transmit a modulated infrared beam that is immune to sunlight or other ambient light.

CIRCLE NO. 347

## Ferrite E cores have round center legs

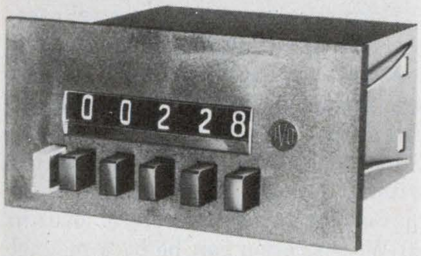


*Siemens, 186 Wood Ave. S., Iselin, NJ 08830. Martin Weitzner (201) 494-1000. See text; stock.*

A line of round-center-leg ferrite E cores are available for use in switch-mode power supplies. They are in the EC35, EC41, EC52 and EC70 configurations. The cores may be obtained with glass-fiber-reinforced-plastic bobbins. The bobbins have pins inserted for either vertical or horizontal mounting. Prices in OEM quantities range from about $.50 to $1.60.

**CIRCLE NO. 348**

## Counter subtracts from 5 predetermined digits

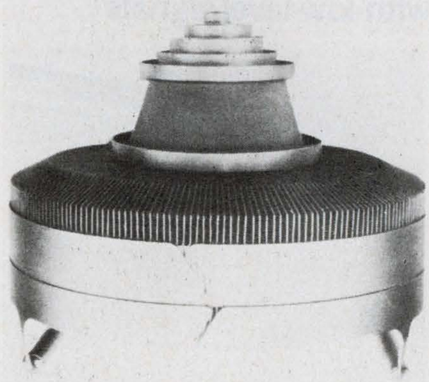



*IVO Industries, P.O. Box 36, Neptune, NJ 07753. James Tannar (201) 922-3600.*

Set up a predetermined count with pushbuttons and the spdt switch operates when the count reaches zero. The count speed of the FS228/FS229 series is 10 cps and the power rating is 4 W. Reset is pushbutton or, optionally, pushbutton plus electrical. Automatic recycling can also be provided. Operation is on 24 V dc and 24, 115 and 220 V ac.

**CIRCLE NO. 349**

## FM broadcast tube has 25-kW rating



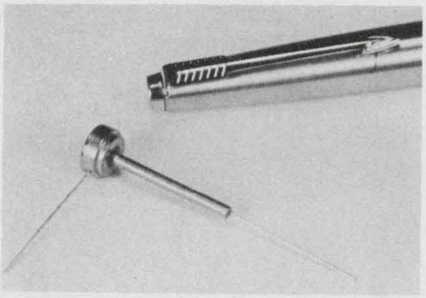
*RCA, New Holland Ave., Lancaster, PA 17604. (717) 397-7661. $900; 8 wk.*

For use in high-gain, high-efficiency FM service, the 4695 beam-power tube gives 25 kW of useful power output at 20-dB gain and 80% over-all plate efficiency. A plate supply of 10 kV and only 300 cfm of cooling air is required. Rated for full output to 230 MHz.

**CIRCLE NO. 350**

*COMPONENTS*

## Wet switch is compatible with low-level signals



*Signal Systems Int., Monmouth County Airport, Farmingdale, NJ 07727. Angelo Ghio (201) 938-3535. $2.00; stock.*

Hermetically sealed in a steel case, the WS101 switch is compatible with low-level solid-state circuits. Contacts are mercury film and there are no interfaces between closed contacts. Nanowatt signals are transmitted without loss or distortion. When required, the switch can control loads to 20 W. Operation can be by a magnet or the field of an electromagnetic coil.

**CIRCLE NO. 356**



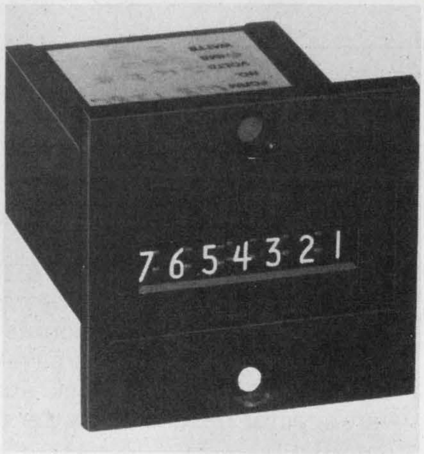
## Dual-primary transformer meets US, European specs

*Dale Electronics, East Highway 50, Yankton, SD 57078. (605) 665-9301. $2.95 (100-qty); stock.*

Rated at 4.5-W, the PL-23 miniature dual-primary transformer can be operated from 115 or 230-V ac, 50/60 Hz, to meet both US and European requirements. The PC-board-mounted device provides isolation from the power line and is available in both voltage step-up or step-down models. Output voltages range from 8 to 230-V ac with series-connected secondaries and 4 to 115-V ac when parallel connected. Designed to operate over the temperature range from -55 to 105 C, the unit produces a maximum temperature rise of 25 C at rated operating voltages and loads. In addition to the basic plug-in mounting style, models are available with mounting frames for tab and screw attachment to the PC board.

**CIRCLE NO. 357**

## Use compact counter in small panel cut out

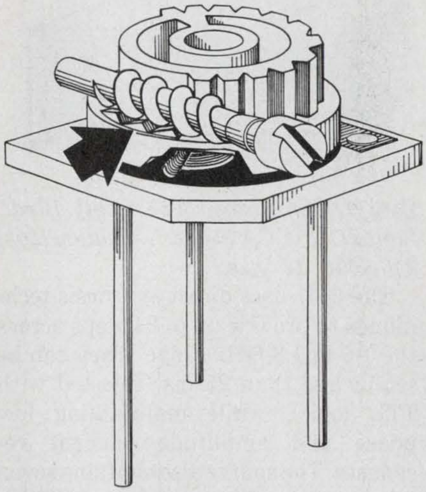



*Veeder-Root, 70 Sargeant St., Hartford, CT 06102. A. Patricelli (203) 527-7201. $16.20 (7 digit), (1-qty).*

Requiring a panel cut out of only 1.63 × 1.14 in., the series 7286 electric counter is designed for warranty recording, metering and other tamper-proof applications. The non resettable totalizers are available in either 12 or 24-V-dc models, and record impulses at up to 600 counts per min. Power may be applied continuously, with 2.5-W dissipation. The units come with either six or seven white-on-black figures and operate over a temperature range of 0 to 40 C. The case, of modified polyphenylene oxide, is ultrasonically welded around the counter frame and component parts.

**CIRCLE NO. 358**

## Ratchet actuator system in multiturn trimmer



*Bourns, 1200 Columbia Ave., Riverside, CA 92507. (714) 781-5122. $7.48 (prod. qty); stock.*

Using a simplified worm-gear actuator drive, the RJR26 trimpot offers extended life operation by reducing wear on internal parts. A specially designed set of ratchet teeth drops the rotor into an idling position at the element end-point. Setability is enhanced, since minimal backlash occurs when reversing the direction of the worm gear. The trimmer uses a cermet element covering a standard resistance range of 10 Ω to 1 M Ω, ±10%, with closer tolerances available. Power rating is ¼W at 85 C, and the operating temperature range is from −65 to 150 C. The device has been qualified to MIL-R-39035, and an industrial model, the 3262 is also available.

**CIRCLE NO. 359**

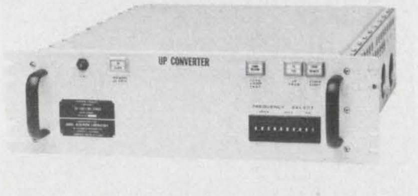
## Temperature switches use ceramic elements

*Midwest Components, Port City & Keating Blvds., Muskegon, MI 49443. (616) 777-2605.*

Miniature temperature switches use an electro-ceramic element instead of a bimetallic switch. The hermetically sealed sensors are corrosion and explosion proof. Switches may be specified as normally open, normally closed or a combination of both in an SPDT switch configuration. Fast response time is achieved by packaging the devices in a small (0.25×0.5 in.) case. At full rated load, the switches can perform 3-million operations. Switch temperatures from −5C and up are available.

**CIRCLE NO. 360**

## Up-converter suitable for digital, FDM signals

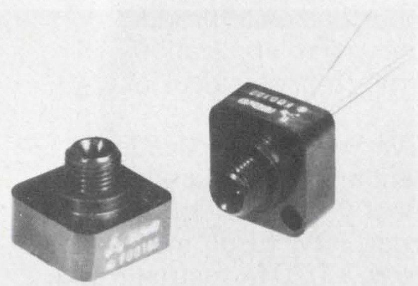



*California Microwave, 455 W. Maude Ave., Sunnyvale, CA 94086. C. Starnes (408) 732-4000.*

The Model CV-3473 up-converter converts signals from a 70-MHz or 700-MHz band to an output between 7.9 and 8.4 GHz. Low phase noise makes the converter suitable for systems with digital and/or FDM signals. Equalized filters minimize group delay distortion in FM and pulse modulated systems. The CV-3473 has a self-contained frequency synthesizer, eliminating mechanical adjustments. The synthesizer's 10-Hz tunability reduces the search requirements of modems.

CIRCLE NO. 355

## Fiber-optics receiver boasts 1-ns rise time

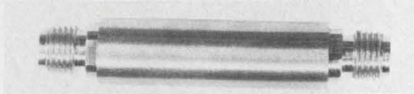


*EG&G Inc., 35 Congress St., Salem, MA 01970. E Danahy (617) 745-3200. Stock.*

In the FOD-100 fiber-optics receiver, designed for optical communications and data transmission, high light-collection efficiency is combined with maximum operating bandwidth. The receiver has a convenient fiber interface, a 5.1-mm$^2$ receiver area, a responsivity of 0.65 A/W min at 904 nm, a spectral range of 350-1100 nm, and a rise time of 1 ns max. It uses a high-speed, high-sensitivity silicon photodiode, the FND-100, which is also available separately.

CIRCLE NO. 397

## Octave-band equalizer in featherweight class



*Cascade Microwave, 3125 S. 208th St., Seattle, WA 98188. (206) 842-2100. 6 wks.*

This miniature equalizer with 0.8 dB band-edge loss covers an octave, up to 18 GHz, with a max VSWR of 1.3:1. Nominal attenuation is 3 dB at band center, but other values are available. The equalizer weighs 0.5 oz and measures 0.34 in. dia × 1.7 in.

CIRCLE NO. 398

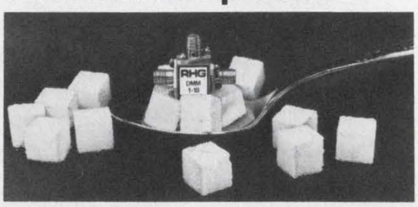
## 5-W power output available at 4.2 GHz

*California Eastern Laboratories, Inc., One Edwards Court, Burlingame, CA 94010. (415) 342-7744. From $150 (10-99 qty).*

A series of microwave power transistors with a "stepped electrode" structure provides high power, gain, efficiency and reliability. The NE4200 Series consists of three devices, the NE4201 (1.5 W, 8 dB gain at 4.2 GHz); the NE4203 (3 W, 5 dB gain at 4.2 GHz); and the NEM4205 (5 W, 4 dB gain at 4.2 GHz). The NE4201, NE4203 are available with or without internal matching, while the NEM4205 requires external matching.

CIRCLE NO. 399

## 'Sugar cube' mixer sweetens MW problems

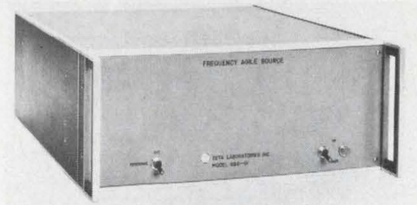



*RHG Electronics, 161 E. Industry Court, Deer Park, NY 11729. S. Wolin (516) 242-1100. $295; stock.*

The 1/8 in$^3$ Model DMM1-18 double-balanced mixer is the smallest possible size that permits the use of flange-mounted SMA connectors. Because of its light weight (1/3 oz) the "sugar-cube" mixer can be cable supported, which reduces mechanical problems and simplifies system packaging. Conversion loss for the 1 to 18 GHz mixer is typically 7 dB with +8 dBm LO power and i-f response from dc to 350 MHz.

CIRCLE NO. 403

## Frequency-agile source sports eight outputs

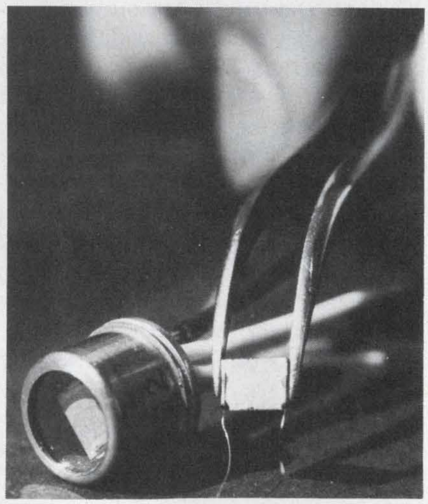


*Zeta Laboratories, 3265 Scott Blvd., Santa Clara, CA 95051. C. Dudley (408) 246-6001. 12 wks.*

The 6641 uses direct synthesis techniques to provide up to 24 steps across the 1.6 to 1.8-GHz range. They can be set in less than 25 ms (selected with TTL logic), while maintaining low phase and amplitude-transient responses. The source also contains seven other output frequencies for COHO, 2nd LOs, clock, and chirp driver, which provide all the signals needed in a frequency-agile radar system. Each output has at least 20 mW of power.

CIRCLE NO. 404

## Infrared detector has built-in refrigeration



*Sanders Associates, Daniel Webster Highway S., Nashua, NH 03061. J. Joyce (603) 885-2810. $200; 3 wks.*

Thermoelectrically cooled lead-sulfide infrared detectors provide high sensitivity and long-term stability for such applications as smoke and moisture detectors. The TO-5-TE lead-sulfide detectors are packaged in standard transistor cans and are hermetically sealed. Because the lead sulfide is cooled to about −20 C, a detectivity (D*) of 2.5 to 5.0 × $10^{11}$ cm-Hz$^{1/2}$ -W$^{-1}$ and a responsivity of 1 × $10^6$ V/W are possible. Each unit incorporates a calibrated monitoring thermistor.

CIRCLE NO. 448

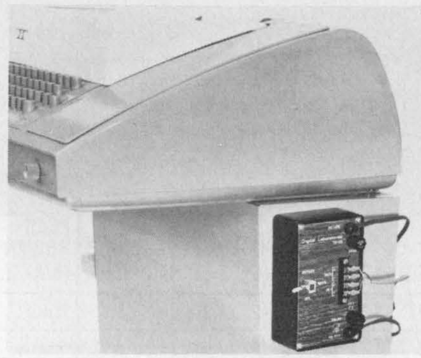
## Photon counting done at high speed

*Pacific Photometric Instruments, 5675 Landregan St., Emeryville, CA 94608. Fred Weekes (415) 654-6585. $685; 3 wk.*

An amplifier/discriminator for use in photon counting (Model AD6) couples a photomultiplier tube to a high-speed counter. The unit has a gain of 100 and 5-ns rise time. Variable-threshold and simultaneous positive (TTL-compatible) and negative (NIM-compatible) outputs are provided. 1.3 lb—3 × 11¼ × 1½ in.

**CIRCLE NO. 449**

## Teletypewriter control stops spurious prints



*Digital Laboratories, 600 Pleasant St., Watertown, MA 02172. W. Kahn (617) 924-1680. $175.*

Model TR 20, a smart motor control, allows a teletypewriter to print and punch paper tape without producing junk characters during an on-off cycle. The unit stores six-characters and so provides a 0.6-s delay for the motor to speed up and print. No programming changes or lead-in characters are required. The module mounts by magnet to the pedestal and connects to the motor through a fuse-plug. A bypass switch permits standard-keyboard operation. An adjustable timer provides up to 20-s turn-off delay. In the event of an unexpected delay between transmitted characters no data is lost. 6 × 3.5 × 3 in.

**CIRCLE NO. 450**

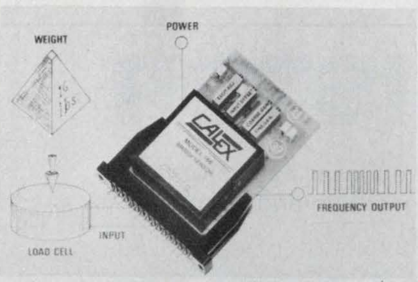
## Board for custom logic supplies mini signals

*Interconnection Technology, P.O. Box 126, Accord, MA 02018. (617) 749-5605. See text 2 to 3 wks.*

Three interface modules: N 102-P ($475), N 103-P ($550) and N 104-P ($690) for Data general, DDC and Keronix minicomputers provide the handshake logic required to interface custom circuitry to the computer. In addition, each unit provides wire-wrap pins for mounting up to 114 IC sockets or the ICs themselves. The single-card unit fits into a mainframe slot. Combinations of devices with from 14 to 40 pins are accommodated. You also get up to 100 I/O connections via a ribbon-cable connector. The 102 is the basic model, the 103 has I/O registers and the 104 adds data-channel-control logic to the 103.

**CIRCLE NO. 541**

## Bridge sensor outputs directly to processor

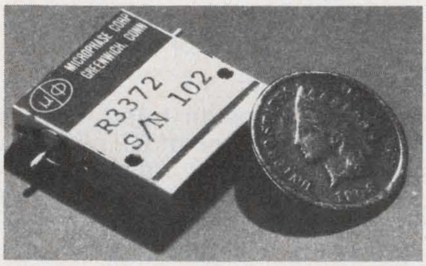



*Calex Mfg., 3305 Vincent Rd., Pleasant Hill, CA 94523. Ron Kreps (415) 932-3911. $98 (1-9 qty); stock.*

A complete bridge instrumentation system is contained in the Model 166 frequency-output, strain-gauge amplifier. The small (2 × 2 × 0.6) module has an adjustable bridge power supply, differential instrumentation amplifier, v/f converter and optically isolated output stage. To implement a complete weighing system all that must be added is an external power source and a load cell. The output of the module can be fed directly to a microprocessor or digital display. Gain of the differential amplifier is adjustable from 10 to 1000 and input impedance is 10 MΩ. The input stability of the amplifier is typically ±0.5 μV/°C and the output is rated at ±10 V at 5 mA, while the frequency output ranges from 0 to 10 kHz.

**CIRCLE NO. 542**

## Miniature filter passes 6 to 18 GHz at low loss




*Microphase, P.O. Box 1166, Greenwich, CT 06830. Craig Snyder (203) 661-6200. $450; 12 wk.*

High-pass filter module, Model R3372, passes 6 to 18 GHz with less than 1-dB insertion loss and a nominal VSWR of 1.6:1. Skirt selectivity is greater than 50 dB within 8% of the cut-off frequency. The unit can be PC or stripline mounted and is 0.9 × 0.8 × 0.25 in.

CIRCLE NO. 543

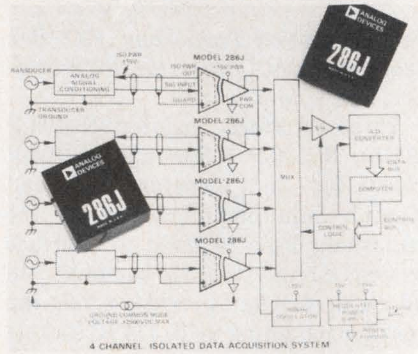
## Controller board fits into the computer

*Rianda Electronics, 2535 Via Palma, Anaheim, CA 92801. (714) 995-6552. $2950; 30 days.*

The 260X controller crams eight asynchronous communication channels, a parallel line-printer interface, a real-time clock and a TTY port onto one PC board. The controller occupies one slot in a Data General computer chassis. The unit comes with a cable set for the communication channels, TTY and line printer. The communication channels are software compatible with the Data General 4060 asynchronous multiplexer; the line printer is software compatible with the Data General 4034/4193 printer controler; the real-time clock and TTY are software compatible with the Data General 4008 and 4010 respectively. The asynchronous multiplexer permits baud-rate selection, word-length selection, parity determination and RS232-C or 20-mA I/O on a per channel basis. The line-printer controller interfaces to many popular line printers.

CIRCLE NO. 544

## Isolation amp drives multichannel system




*Analog Devices, Route 1 Industrial Park, Norwood, MA 02062. Joseph Codispoti (617) 329-4700. $59; stock.*

Up to eight of the 286J isolation amplifiers can be driven by one synchronizing oscillator. Total ground-loop isolation and protection from common-mode potentials of 2500 V is provided. Nonlinearity of ±0.05% at 10-V pk-pk output makes the device suitable for systems requiring 10-bit accuracy. Input drift is less than ±10 $\mu$V/°C at a gain of 100 and gain stability is 0.001%/1000 h and 0.01%/°C.

CIRCLE NO. 545

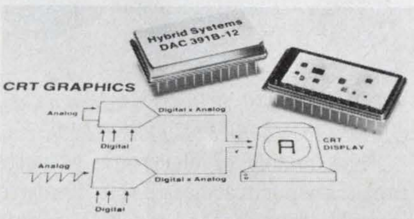
## Speed controls match dc motors

*Minarik Electric, 232 E. Fourth St., Los Angeles, CA 90013*

Series SLF adjustable speed controls are precisely matched to the operating characteristics of Bodine's popular 130-V-dc PM motors (frames 32D3-, 32D5-, 42D3- and 42D5BEPM). Features of the controls include choke and capacitor filtering; temperature, IR and line-voltage compensation; line starting and stopping; max and min-speed adjustment; smooth motor acceleration; full-wave field and armature supply (permits operating shunt motors); and current limiting. Speed regulation is 2% typ. The controls use 115-V-ac 50/60-Hz input. The 1/8-hp model draws 3 A and delivers 0 to 130 V dc at 1.2 A to the armature and 100 V dc at 0.5 A to the field. Ratings for the ¼-hp models are identical except that they draw 4.5 A and deliver 2.2 A to the armature.

**CIRCLE NO. 546**

## Fast d/a converter multiplies 12 bits




*Hybrid Systems, Crosby Dr. Bedford Research Park, Bedford, MA 01730. L. Lauenger (617) 275-1570. From $129 (1-9 qty); stock to 4 wks.*

Setting time of 200 ns to 0.01% of full scale is featured in the DAC391 Series of two-quadrant 12-bit multiplying d/a converters. Differential linearity of 0.0125% of full scale and transfer linearity of ±1/2 LSB are also noteworthy in the hybrid unit. The devices accept TTL or DTL logic levels and deliver current outputs of 0 to +5 mA for binary-coded inputs and ±2.5 mA for offset-binary-coded inputs. The output compliance potential is 0 to +1.0 V (unipolar) and ±1 V (bipolar). For applications requiring outputs of 0 to −10 V and ±5 V, provisions are included for connection of an external op amp. Commercially processed versions operate from 0 to 70 C or −25 to +85 C. Mil versions operate from −55 to +100 C. Metal, 24-pin, DIP.

**CIRCLE NO. 547**

## Thirteen components in single IC panel meter

*International Microtronics, 4016 E. Tennessee St., Tucson, AZ 85714. Otto Fest (602) 748-7900. $39 (100-qty) 5-V units.*

A 3-1/2 digit DPM, B500, contains a single IC, seven passive components and the display—for a total of thirteen parts. The meter is bipolar, differential, autozero, accepts 200-mV to 1000-V inputs and operates from either 5-V-dc or 115/230-V-ac power sources. A 0.5-in.-high red LED is used in the display. Power consumption is 200 to 800 mW. The B500 units are successors to the Series 500, the first $49 digital panel meters. Models containing a liquid crystal display will be available in the near future.

CIRCLE NO. 548



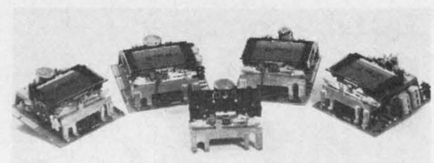
## Instrumentation amp hardly drifts

*Dynamic Measurements, 6 Lowell Ave., Winchester, MA 01890. (800) 225-1151 From $79; stock*

Max input-offset drifts of only 15-pA/°C and 0.25-μV/°C are features of the 1313 instrumentation amp. Also, offset voltage changes only 50 mV over the 1-to-1000-gain range, and maximum gain nonlinearity is 0.01%. The amp delivers ±10 mA at ±11 V, and the min output-slew rate is 1 V/μs. Bandwidth is 75 kHz at 1000 gain. Input range: ±10V; min common-mode impedance: $10^{10}\Omega$. Input bootstrapping produces a min common-mode rejection of 114 dB at 120 Hz, and virtually eliminates power-supply variation problems. The 1.5 × 1.5 × 0.375 in. metal package is pincompatible with both Datel's 201C and DMC's 351 and 1308 families.

CIRCLE NO. 549

## Cassette transports are for audio applications



*Triple I, 4605 N. Stiles, Oklahoma City, OK 73118. (405) 521-9000. $124.*

Five models of electronic cassette-tape transports are available. Features include four-motor control, remote control, fast start/stop, rewind in less than 30 s and speeds from 0.4 to 20 ips. Options such as tab sensing, counter for position reference, and cassette-in-place sensing can be provided.

CIRCLE NO. 550

## 150-W transient voltages suppressed by zener

*Unitrode, 580 Pleasant St., Watertown, MA 02172. Roy Selinger (617) 926-0404. See text; 4-6 wk.*

The UZ306 series of zener transient-voltage suppressors can dissipate 3 W (steady-state) and 150 W (transient) for 1 ms. Standard voltages include the 6.8 to 400-V range. All devices feature low leakage and clamping-voltage ratios. Transient-response time is $1 \times 10^{-12}$ s. At 1-k quantity, prices range from $0.70 to $1.05; at the 10-k level, prices are $0.36 to $0.55.

CIRCLE NO. 551

# the only one of its Kind

...AN ALTERNATIVE TO NICKEL CADMIUM


**6 volt ½ ampere hour**
1.92" length
1.00" width
2.00" height
4.8 ounces

***THE NEW IMMOBILIZED ELECTROLYTE TECHNOLOGY THAT'S MORE RELIABLE THAN GEL***

- No memory conditioning required
- No cell reversal
- Less expensive
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**Commercial Products Department. ED**
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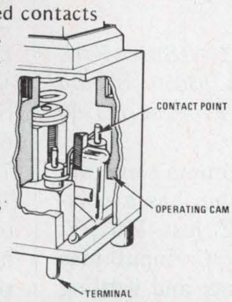
**Telephone (417) 776-2258**

CIRCLE NUMBER 149

## SWITCHES FOR KEYBOARDS

We offer the following for OEM's producing their own keyboards.
- Keyswitch sizes for 5/8" or 3/4" centers
- Gold Bar mechanical contacts or sealed contacts
- Front panel relampable lighted models
- Single and double pole contacts including NC
- Alternate action models
- Doubleshot molded keytops for 3/4" or 5/8" mounting
- Easy change legend systems
- 100,000 pc. quantity prices as low as $0.21 each

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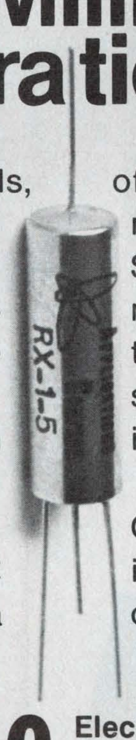
CIRCLE NUMBER 152

# 50 Million operations

With TTL loads, our new reed relay offers maximum contact resistance of 0.12 ohms, after more than 50 million operations. And a contact resistance delta of 0.01 ohms, maximum. Sticking and missed operations are essentially eliminated.




Call or write for information on the RX-1.

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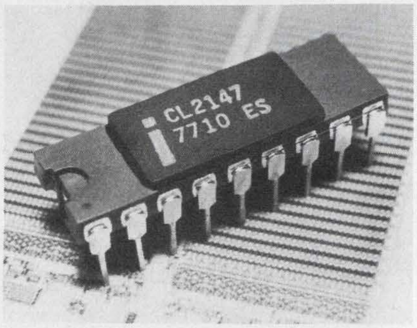
CIRCLE NUMBER 153

## Static 4-k RAMs access in less than 55 ns




*Intel, 3065 Bowers Ave., Santa Clara, CA 95051. Rob Walker (408) 246-7501. From $37.50 (100 qty); stock.*

The 2147 family of high-speed, 4096-bit static RAMs has a typical access time of 45 ns. And, a low-power standby mode automatically reduces average device power consumption to a fraction of the active power. The low-power mode is unique in that it does not reduce RAM operating speed, data throughput, and does not require clocking or complex power-switching techniques. The basic 2147 design has a typical access time of 45 ns but guaranteed times are 55 ns for the 2147-3 and 70 ns for the 2147. These speeds are guaranteed over 0 to 70 C and the standard power supply tolerance of 5 V ±5%. Typical active dissipation is 500 mW for the 2147 and 600 mW for the 2147-3, and worst-case is 800 and 900 mW, respectively. The standby mode reduces typical dissipation to 50 and 75 mW, respectively. The 2147s come in 18-pin DIPs and the three-state data outputs typically sink 25 mA and source 15 mA at TTL levels.

**CIRCLE NO. 552**

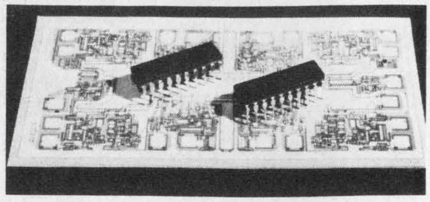
## Low-offset FET op amps slew at 45 V/μs

*Precision Monolithics, 1500 Space Park Dr., Santa Clara, CA 95050. Shelby Givens (408) 246-9222. From $2.50 (100 qty); stock.*

With a 45 V/μs minimum slew rate the OP-17 BiFet op amp has a maximum input offset of just 500 μV. Offset drift is 5 μV/°C. Input bias currents are 11nA, max and settling time of the output is 400 ns to 0.1%. The OP-17 comes in an 8-lead T0-99 case and is pin-compatible with the LF157A series of op amps.

**CIRCLE NO. 553**

## Octal latch and register interfaces μPs

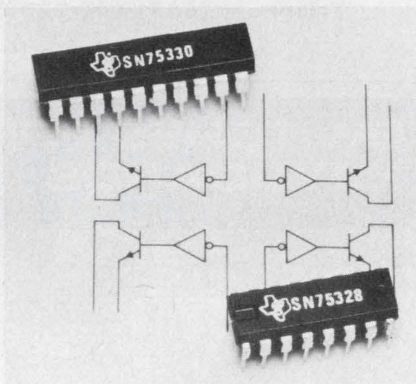


*Monolithic Memories, 1165 E. Arques Ave., Sunnyvale, CA 94086. Ray Gouldsberry (407) 739-3535. $4.60; stock.*

Two bipolar parts, a latch (SN74S373) and a register (SN74S374) feature three-state outputs to drive the high capacitance and low impedance of long buses connecting processor, controller and I/O subsystems. Either device can be used with a 4-bit microprocessor slice, and a pair of them will work with a 16-bit processor system.

**CIRCLE NO. 554**

## Quad memory drivers handle 600 mA/output




*Texas Instruments, P.O. Box 5012, Dallas, TX 75222. Dale Pippenger (214) 238-2011. From $2.47 (100 qty); stock.*

The SN75328 and SN75330 each contain four 600-mA memory drivers that can handle core or bubble memories. They operate from two power supplies —one a 5 V, the other can be 4.75 to 24 V. The drivers can function individually as either source or sink. The SN75328 driver comes in 16-pin plastic or ceramic DIP packages while the 75330 comes in a 20-pin package. In the 75328 the base drive of all four of its output transistors is provided by connecting an external resistor between the second supply and Node R on the chip. On the SN75330 the base drive of each individual output transistor can be separately set. Both devices operate from 0 to 70 C.

**CIRCLE NO. 555**

## Analog shift-registers provide 185-bit delays

*American Microsystems, 3800 Homestead Rd., Santa Clara, CA 95051. (408) 246-0330. $7.05 (100-999).*

Requiring a two-phase symmetrical clock input, the S10110 analog shift register provides a delay depending on the clock frequency. The S10111 part is similar, but saves outboard circuitry by requiring only a one-phase clock input.

CIRCLE NO. 556

## Power Schottky diodes deliver up to 75 A

*Motorola, P.O. Box 20912, Phoenix, AZ 85036. Cliff Peterson (602) 244-6900. From $3.45 (100-qty); stock.*

Designed specifically for high-current switching applications, the MBR7520 series of Schottky rectifiers covers a forward current range from 25 to 75 A, with reverse voltage ratings up to 45 V. There are 17 devices in the series and they can operate at junction temperatures of 150 C. For most devices in the series, the dV/dt ratings are 1000 V/$\mu$s. Units on test at a forward current of 70 A, a voltage of 45 V and a case temperature of 100 C have been hit with 8.3 ms pulses of 1300 A (one every minute) with no failures. DO-4 or DO-5 stud packages.

CIRCLE NO. 557

## Schottky paramp varactor is used in X to K-band

*Alpha Ind., 20 Sylvan Rd., Woburn, MA 01801. Jerry Hill (617) 935-5150. $300-$500 (1 to 9).*

GaAs Schottky paramp varactors, DVS 6680, are for use in low-noise parametric amplifiers from X to K-band. These varactors have $f_{CO} > 800$ and $C_{JO}/C_{J3} > 1.85$. $C_J$ is typically 0.15 pF. Only 20 mW of pump power is needed. Diodes are offered in the 290, 324, and 328 low-parasitic package styles. Diode series resonance is approximately 50 GHz and parallel resonance is to 100 GHz in the 328 package outline.

CIRCLE NO. 558

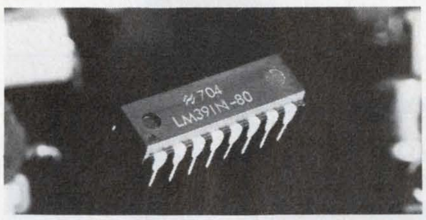
## 3-1/2 digit a/d's have LCD or LED drive outputs

*Intersil, 10710 N. Tantau Ave., Cupertino, CA 95014. S. Osgood (408) 996-5000. 100-qty prices: $9.80 (7106), $9.25 (7107). Also evaluation kits are available: $24.95 (LED), $29.95 (LCD); stock.*

Two low power CMOS a/d converters provide outputs for a 3-1/2 digit display. Both units provide parallel, seven-segment outputs/ and are housed in 40-pin DIPS. The ICL 7106 is designed to directly drive an LCD, including backplane drive, while the ICL 7107 will directly drive instrument size, LED displays without buffering. Only seven additional passive components, a display and a power supply are needed to form a complete digital voltmeter with automatic zero correction and automatic polarity. True ratiometric readings can be done over a full scale input range from under 200 mV up to 2 V.

**CIRCLE NO. 559**

## Replace hi-fi discretes with IC power driver




*National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051. Bill Gross (408) 737-5621. $2; stock.*

The LM391 monolithic IC can drive external power transistors in 10 to 75-W power amplifiers. It is capable of direct operation from a ±40-V supply. Total harmonic distortion is less than 0.05% over the entire audio band. Wideband noise is 3 $\mu$V at the input.

**CIRCLE NO. 560**

## 8-kbit erasable PROM cuts $\mu$C power drain

*Intel, 3065 Bowers Ave., Santa Clara, CA 95051. Rob Walker (408) 246-7501. $26.60; stock.*

Operating on a 5-V TTL power supply, the 2758 EPROM avoids the need for special MOS supplies. It reduces active power dissipation by more than 50% and a standby mode can be used to reduce dissipation by more than 80%. Storage is 1 kbyte and access time is 450 ns.

**CIRCLE NO. 561**

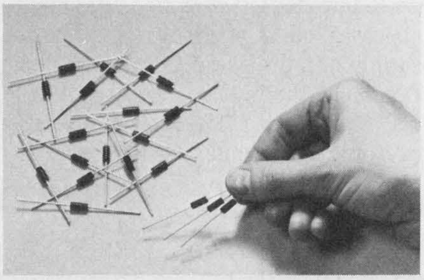
## Precision v/f converter also converts f/v

*Teledyne Semiconductor, 1300 Terra Bella Ave., Mountain View, CA 94043. Michael Paiva (415) 968-9241. $3.70/(1000 qty); stock.*

The 9400 is a low-cost v/f converter which also functions as an f/v converter. It combines bipolar and CMOS technology on a singlechip, interfaces with all logic families, and comes in a 14-pin plastic or ceramic DIP. Operation is from 10 Hz to 100 kHz in v/f applications, with 0.01% typical linearity to 10 kHz. Both pulse and square-wave outputs are provided. The device operates on a single or dual power supply and draws only 1.6 mA. In the f/v mode, the 9400 operates from dc to 100 kHz, with 0.1% typical linearity over the full range.

**CIRCLE NO. 562**

## Zener diodes now come with 2.5 and 5-W ratings

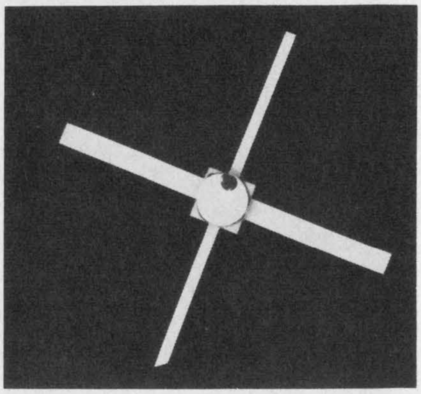


*American Power Devices, 7 Andover St., Andover, MA 01810. Robert Dimodana (617) 475-4074. For 1000 qty lots: $0.24 (2.5 W) $0.30 (5 W), 3 wks.*

Zeners with power ratings of 2.5 W—the 1N5008 series—are available in 42 voltage ratings from 3.3 to 82 V with 5% and 10% tolerances. Also available is a 5-W series—the 1N5333—with 43 voltage ratings from 3.3 to 82 V in 5%, 10%, and 20% tolerance versions. The silicon-oxide-passivated diodes are encased in axial-leaded transfer-molded packages.

**CIRCLE NO. 563**

## Bipolar transistor has 2.8-dB NF at 4 GHz

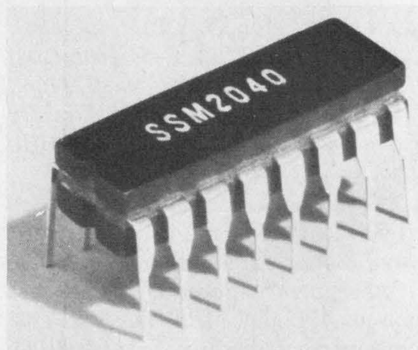


*Avantek, 3175 Bowers Ave., Santa Clara, CA 95051. William Berridge (408) 249-0700. Stock.*

The AT-4680 bipolar microwave transistor is optimized for low noise-figure, small-signal amplification at frequencies up to 6 GHz. NF is 2.8 dB, with 8.5-dB associated gain, at 4 GHz. At 2 GHz the typical NF and gain are 1.8 dB and 13.6 dB, respectively, and at 1 GHz they are 1.4 dB and 17.7 dB. The device is housed in a 70-mil square, metal/ceramic strip-line package.

**CIRCLE NO. 564**

## Volt-controlled filter has 4 tracking sections




*Solid State Music, 2102A Walsh Ave., Santa Clara, CA 95050. John Burgoon (408) 246-2707. $10; stock.*

The SSM2040 monolithic voltage-controlled filter contains an exponential generator, four voltage-controlled amplifiers and four high-impedance buffers. The combination provides four flexible tracking filter sections. It operates from ±15 V. Signal-to-noise ratio is better than 75 dB and distortion is less than 0.1%. The control rejection characteristic is guaranteed over the filter's 10,000:1 sweep range.

**CIRCLE NO. 565**

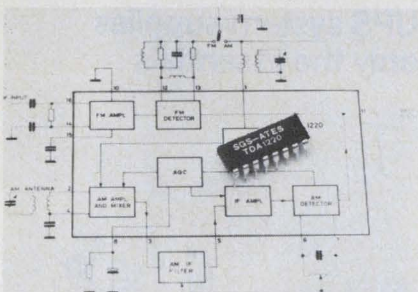
## One-chip converter drives and converts for DPM

*National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051. Jerry Zis (408) 737-5225. See text.*

A single CMOS chip, the ADD3501, includes all conversion and drive circuitry for a 3½ digit DPM. The device, in a 28-pin dual-in-line package, uses a pulse modulation analog-to-digital technique, integrating the input signal to obtain a high immunity to noise. Accuracy is ±0.05% +0−1 count for a 0-to-70-C temperature range. The output can drive 0.5 and 0.7-in. LED displays. Overflow indication is provided. 100 qty prices: $9.95 (plastic package), $10.95 (ceramic).

**CIRCLE NO. 566**

## AM/FM receiver circuits need few external parts

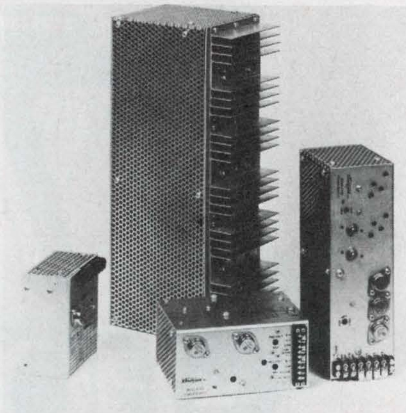



*SGS-ATES Semiconductor, 70 Massasoit St., Waltham, MA 02154. Ruben Sonnino (617) 891-3710. 1 to 99 qty: $1.95 (1220), $3.50 (1230); samples from stock.*

The TDA1220 and TDA1230 are radio receiver circuits. Available in a 16-pin DIP, the TDA1220 is a complete AM-FM system for portable radios. It includes i-f FM amplifier, limiter and fm detector in the FM section and rf-AM amplifier, mixer, local oscillator, i-f amplifier and detector in the AM section. The supply voltage can vary between 4 and 18 V and AM-FM selection is done with a dc switch. In the FM mode, the circuit has a 30 $\mu$V sensitivity, an AM rejection of 60 dB and a signal-to-noise ratio of over 60 dB. In the AM mode less than 1% distortion is present and an AGC range exceeding 80 dB is available. The TDA1230 is intended for monophonic AM/FM radios and includes a complete sub-system for amplification and detection of FM i-f signals. Also included is a 4 W power amplifier. The TDA1230 comes in a fin-DIP package.

**CIRCLE NO. 567**

## Low-cost supplies cover wide range

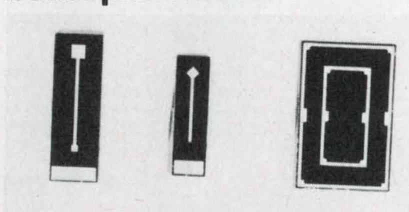


*Deltron Inc., Wissachickon Ave., North Wales, PA 19454. (215) 699-9261. See text, 6 wks.*

Prices range from $40 to $233 in 10-piece qty for 78 single and multiple-output supplies with nominal ratings of 5 to 32 V at from 1 to 35 A. Units in the OEM series deliver up to 277 W. Other features include: a heavy-duty barrier block for input and output connections, remote sensing and programming capabilities. Overvoltage protection is standard on certain models and an option for all others. All units are said to be, drop-in electrical and mechanical replacements for the corresponding supplies from ACDC.

**CIRCLE NO. 568**

## Small solar cells boast passivation



*Dionics, 65 Rushmore St., Westbury, NY 11590. Manny Sussman (516) 997-7474. See text; stock.*

Miniature silicon solar cells, types PK104/PK105/PK106, have protected junctions (oxide-passivated) with both contacts on the top surface. They are provided as individual chips which may be assembled into arrays. The open-circuit output is 0.5 V with output currents ranging from 0.47 to 1.8 mA depending on type. Prices are from $.18 to $.50 each, depending on type and quantity.

**CIRCLE NO. 569**

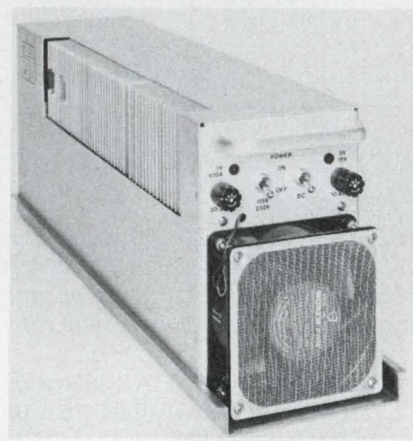
## Protect 3$\phi$ lines with plug-in monitor

*Amtron, P.O. Box 2783, Norman, OK 73069. David Donaghe (405) 364-6143. $38-$49.50; stock.*

Continuously monitoring 3$\phi$ power lines, the plug-in unit opens contacts when it senses a lost phase, low voltage, phase reversal or phase-angle shift. It is offered in three adjustable-voltage ranges: 85 to 125 V (3P120); 160 to 240 V (3P240); 340 to 480 V (3P480). A failure indicator lamp is provided.

**CIRCLE NO. 570**

## UPS system supplies only the essentials

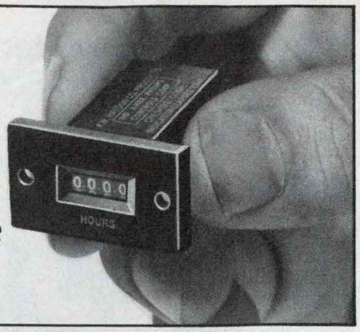


*Trio Labs, 80 Dupont St., Plainview, NY 11803. P.Bauer (516) 681-0400.*

Model 692 is a switching power supply, with partial UPS capabilities, that allows a system to stay on at reduced capacity until the ac input returns. Operating with ac-line power the supply provides the following typical outputs: 5 V at 100, 5 V at 18 A and 12 to 15 V at 6.5 A. When the ac input is removed, a battery takes over and supplies the input for the two lowest power outputs. Specifications include: ±0.2% static regulation for the worst combination of ac or dc inputs and load; ±2% dynamic regulation for a 50% load change; 50-mV pk-pk ripple; overvoltage crowbars; overcurrent foldback; line-dropout immunity; and power-fail signal. 8 × 5.25 × 23 in.

**CIRCLE NO. 571**

# Smallest industrial direct digital readout Elapsed Time Indicator?




## The only big thing about it is its easily read 4-digit hourly display

Our Series 49200 Elapsed Time Indicator is the smallest industrial direct digital readout ETI we've ever made. It may be the smallest anyone has ever made. It measures a mere 37⁄64" sq. x 1¼" long—a real space-saving way to monitor operating time in business machines, computers, peripherals and other equipment where space is limited. Despite its small size, it's exceptionally accurate, and the .075" high 4-digit hourly display is readily legible. An automatic tamper-proof latching memory stores elapsed time indications that can't be lost in event of power failure. Where size is important, the Series 49200 can be one of your best values ever. It's powered by a 1W synchronous motor, 115V ac, 60 Hz. Front or side readout. Surface or through-panel mount.

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NORTH AMERICAN PHILIPS CONTROLS CORP.

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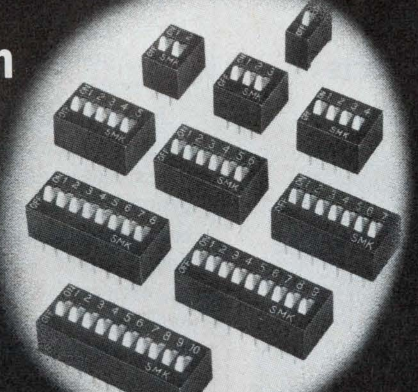
**FOR INFORMATION, CIRCLE 166**
**FOR IMMEDIATE, CIRCLE 167**

# DIP Switch Line from SMK




**The JS-8722 Series** is a complete line of DIP Switches, from 1 to 10 positions, featuring sealed construction to prevent flux contamination during wave soldering. A clip-type wiper design assures positive 2-sided contact to provide excellent shock and vibration characteristics.

Available in SPST configuration, the switches are rated at 24V DC at 300mA switching, resistive load, and will operate from −20°C to +60°C.

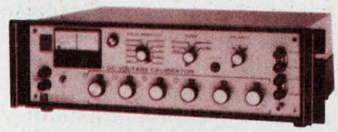
Typical price for a 4 position DIP Switch in 100 piece quantity would be $1.16 each.

SMK SMK Electronics Corporation of America
118 East Savarona Way Carson, California 90746
Tel: (213) 770-8915

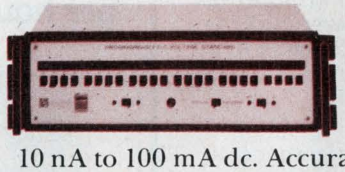
**CIRCLE NUMBER 60**

# We're Second only to the N.B.S.

## SOURCES — REFERENCES CALIBRATORS — STANDARDS

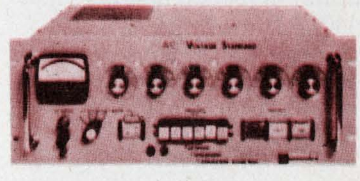


**DC Voltage** and **Currents Standards** in 12 models from ± 10 nV to ± 1100 Vdc. Differential Voltmeter optional. Current 10 nA to 10 Amps. Prices from $695. Circle # 208



**Programmable DC Standards** from ± 0.1 μV to ± 200 Vdc, current from 10 nA to 100 mA dc. Accuracy ± 0.005%. Prices from $1595. Circle # 209

**AC Voltage** and **Current Sources** 10 μV to 1100 Vac @ 50 VA burden. Current 1 μA to 10 Amp ac. Frequency 50 Hz to 1000 Hz. Price $3695. Circle # 210

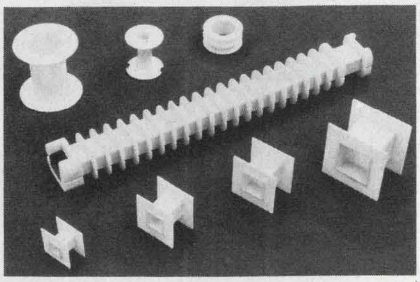


Circa 1962

**Electronic Development Corp.**
11 Hamlin Street, Boston, Mass. 02127
(617) 268-9696

*PACKAGING & MATERIALS*

## Glass-silicone bobbins withstand 180 C

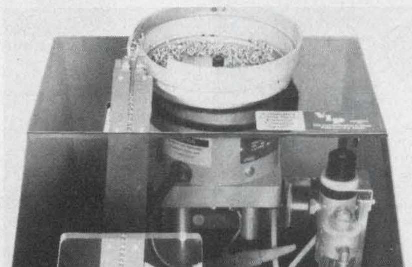


*Stevens Products Inc., 128 N. Park St., East Orange, NJ 07019. (201) 672-2140.*

Open-stock tooling is available for thousands of sizes of bonded glass-silicone, Class-180-C coil bobbins. Bobbin cores are cut to length from 18-in. long, convolutely wrapped tubes, molded in thicknesses from 0.02 in. and then sandblasted outside. Tubing meets MIL-P-997B specs. Flanges are fabricated from NEMA Grade G7 glass-silicone sheet stock, sanded on both sides and tap fitted over the ends of the core with a 0.015-in. offset for bonding of both sides.

**CIRCLE NO. 800**

## Crimp 1200 contacts per hour

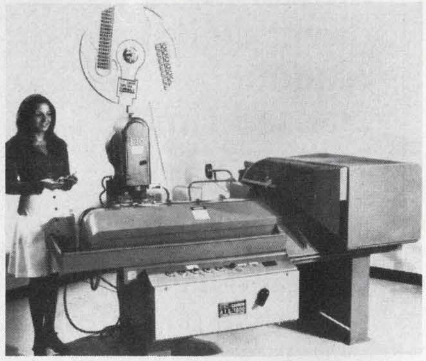


*VIP Industries, 246 Knickerbocker Ave., Paterson, NJ 07503. Ed Nemeth (201) 345-5800.*

An automated contact and eyelet crimper produces more than 1200 crimped wires per hour. It orients, positions, feeds and crimps a variety of eyelets, contacts, pins and receptacles onto stripped wire. The system accepts wire gauges from #26 to #10.

**CIRCLE NO. 801**

## Lead terminator does 3000 per hour



*Cannon Electric, 29000 Aurora Rd., Solon, OH 44139. Allen Gath (216) 248-8800. 12 wk.*

Open or closed-barrel terminals can be automatically put onto leads at speeds up to 3000/h with the Model ATS/1000. Lead lengths from 3½ to 199 in. can be handled. When connected to the Artos CS6-CTO wire-cutting/stripping machine, it measures, cuts, strips and terminates the wires automatically. Wire sizes from #22 to #10 are accommodated.

**CIRCLE NO. 802**

## High capacity dip board speeds μP system design

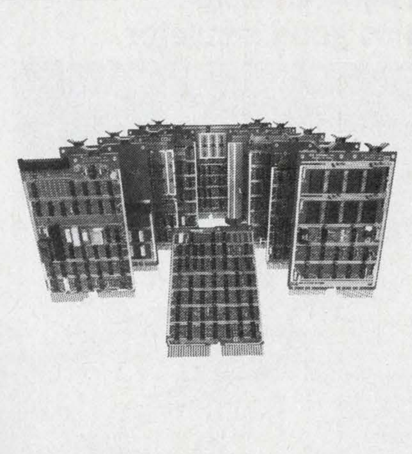
*Vector Electronic Co., 12460 Gladstone Ave., Sylmar, CA 91342. (213) 365-9661. See text.*

Four new high capacity DIP circuit cards provide a combination of board sizes, convenient power-bus and ground-plane organization and edge connector configurations that speed development of microprocessor, memory, or interface systems. Unlike other cards with restrictive bus patterns, the new Vectorcards accept all DIP sockets with 0.1 in. by 0.3, 0.4, 0.6, and 0.9-in. lead spacing, and with up to 64 pins. Two 4.5 in. wide × 6.5 in. long boards, designated 4493 and 4494 accommodate any combination of DIPs up to a maximum of 42. For more extensive systems the model 4493-1 and 4494-1 boards which are 4.5 in. wide and 9.6 in. long can be used. These boards accept up to 60 ICs. A full ground plane is provided on the component side and a power plane is provided on the wiring side. Power supply conductors are placed less than one quarter inch from any DIP lead. The board design provides an optional area for mounting either DIPs or a low-profile heat sink and two regulators in TO-220 packages.

**CIRCLE NO. 803**

# MDB SYSTEMS presents... The LSI-11 Connection

**GP Logic Modules · Peripheral Controllers · Communications Interfaces · Special Purpose Modules · Accessory Hardware**
**Plus: DEC's own LSI-11 Microprocessor Module.**



Here are some MDB Systems connections to LSI-11 microprocessors:

- ☐ General Purpose Interfaces:
  Parallel for programmed I/O and DMA.
  Do-it-yourself dual and quad wire wrap for any DIP design.
- ☐ Device Controllers for most major manufacturer's
  Printers
  Card equipment
  Paper tape equipment
  Plotters
- ☐ Communications/Terminal Modules
  Asynchronous Serial Line
  Synchronous Serial Line
- ☐ MDB Backplane/Card Guide Assembly (8 Quad slots)
  Rack mount chassis 5¼" front panel.
- ☐ Special Purpose Modules and Accessories
  System monitoring unit provides front panel switch addressing, power on/off sequencing; line frequency clock.
- ☐ Bus extenders/terminators.
  E-PROM and PROM modules.
  Bus connectors for backplane assemblies.

MDB Systems products always equal and usually exceed the host manufacturer's specifications and performance for a similar interface. MDB interfaces are software and diagnostic transparent to the host computer. MDB products are competitively priced; delivery is usually within 14 days ARO or sooner.

MDB also supplies interface modules for DEC PDP*-11 Data General NOVA* and Interdata minicomputers.

MDB
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1995 N. Batavia St., Orange, California 92665
714/998-6900 TWX: 910-593-1339

*TMs Digital Equipment Corp. & Data General Corp.

**CIRCLE NO. 285 FOR LSI-11: 286 FOR PDP-11: 287 FOR NOVA: FOR INTERDATA 288**
**"See us at Systems '77 Munich."**

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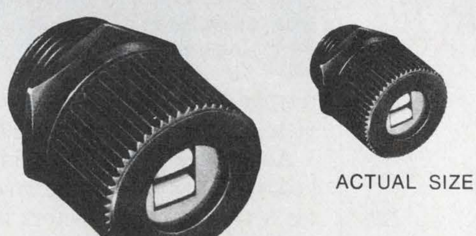
# New Mini Lo-Power BITE Indicator for Computers



ACTUAL SIZE

**Qualified to MIL-I-83287/04.** This patented manually-resettable magnetic latching indicator requires only 50 milliwatts pulse power to operate. It is ideal for direct interface with TTL logic. The indicator changes from all-black to red or white display upon application of a pulse width of 25 milliseconds, latches and holds until reset by rotating the knob 60°. The Minelco MI51LP is available in 1.5 to 28v dc. Operating temperature range is −60°C to +125°C. **Write or call for details.**

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CIRCLE NUMBER 213



*PACKAGING & MATERIALS*

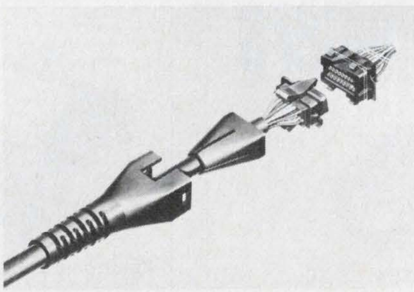
## Thermal paste also good insulator


*Wakefield Engineering, 77 Audubon Rd., Wakefield, MA 01880. (617) 245-5900. See Text.*

An easy-to-spread thixotropic paste, Delta Bond 155, provides high heat transfer, low shrinkage and a coefficient of thermal expansion comparable to that of copper and aluminum. It bonds to a wide variety of substrates and resists severe temperature cycling. When used to form thermally conductive joints between heat sinks and power devices, the paste also serves an an electrical insulator. Kits containing resin and hardner are priced at $3.95 in quantities of 1 to 9.

CIRCLE NO. 804

## Mini-connectors disconnect fast

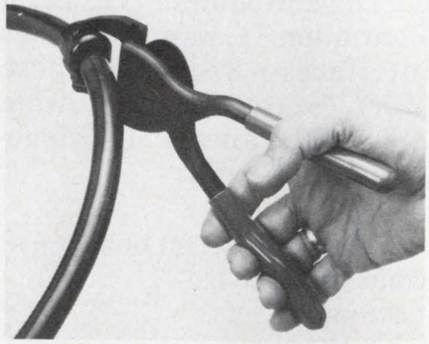


*TRW Cinch, 1501 Morse Ave., Elk Grove Village, IL 60007. Oscar Rothchild (312) 439-8800. $3 (10,000 qty.).*

A miniature, high-reliability, quick-disconnect system, Dura-Lok, can have up to 24 contacts in a cross-section of 0.95 × 0.65 in. Primarily for cable-to-panel use, the connector also connects cable-to-cable. It accepts cable of 22 to 26 AWG, solid or stranded wire. The replaceable crimp-type contacts snap into the insulator. The connector halves mate with a positive, audible action. Rating is 5 A.

CIRCLE NO. 805

## Assembly pliers install strain-relief bushings

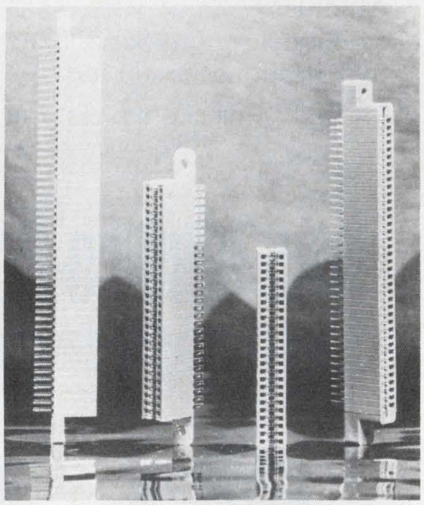


*Heyman Mfg., P.O. Box 160, Kenilworth, NJ 07033. (201) 245-2345.*

Installation of larger-size strain-relief bushings can be done with the #30 pliers. It provides a leverage ratio of 10:1 and is adjustable for the sizes that assemble into mounting holes with diameters from 7/8 to 1-13/16 in.

CIRCLE NO. 806

## Wide variety offered by cut-to-length connectors



*Amphenol, 2875 S. 25th Ave., Broadview, IL 60153. (312) 345-9000.*

A mix-and-match capability that keeps pace with manufacturers' needs for a variety of connectors is possible with new cut-to-length connectors being offered by Amphenol. From 15 basic components a total of 40,800 different connectors can be produced. The connectors provide as many as 85 contacts on each side. The contacts can be single or double sided with spacings of 0.1 in. and 0.156 in. They are made of a high tensile material and come with one of three gold plating thicknesses—0.5 microns, 0.76 microns and 1.2 microns. Five tail styles and four contact configurations are available for each spacing version.

CIRCLE NO. 807

## Plug-in generates data at top speed

*Tau-Tron Inc., 11 Esquire Rd., North Billerica, MA 01862. (617) 667-3874. $3300; 8-10 wks.*

The MG-15 is a quarter-size plug-in module providing a serial data output at clock rates up to 500 megabits. Front-panel toggle switches program the 15 or 16 bit word. The 1-V output may be selected as RZ or NRZ.

CIRCLE NO. 808

## Desk-top printer handles 1200-baud data

*Scope Data, 3728 Silver Star Rd., Orlando, FL 32808. Walt Plyter (305) 298-0500.*

An electrosensitive nonimpact high-speed printer, the COMM 1200 handles 1200-baud data transmissions continuously and operates asynchronously at speeds up to 300 cps. The desk-top or pedestal-mounted unit is 19 × 14 × 6 in. and weighs 25 lb. Roll-type electrosensitive paper 8½-in. wide and 300-ft long is used. ASCII coding is standard with APL, EBCDIC and BAUDOT optional.

CIRCLE NO. 809

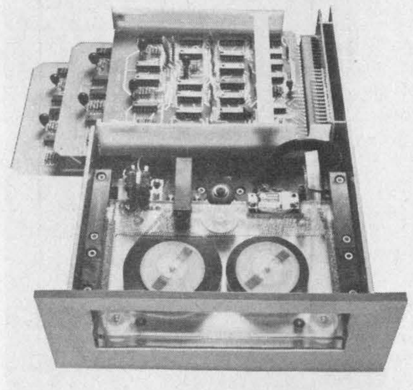
## Indexed tables enhance disc-storage accuracy

*Mohawk Data Sciences, 1599 Littleton Rd., Parsippany, NJ 07054. J. Santoro (201) 540-9080. No charge.*

A software enhancement for the System 1200/2400 product line permits users to create and store on disc index-sequential tables as large as 17.5 megabytes. The new feature allows users to create and store off-line as many as 64 tables with entries of up to 122 characters. Indexed tables improve accuracy because any field can be verified simultaneously against as many as four separate tables.

CIRCLE NO. 810

## Cartridge recorder is ANSI/ECMA compatible

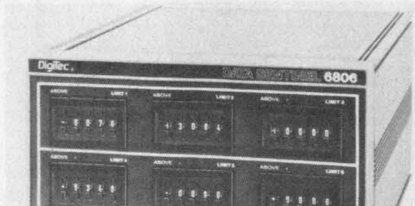


*Raymond Engineering, 217 Smith St., Middletown, CT 06457. Charles Gould (203) 632-1000. $1250-$1400.*

Used with ¼-in. data cartridges, the model 64/3 Raycorder tape drive is fully ANSI/ECMA compatible. It provides automatic search to load point on command, and external program capability for drive-select codes when up to four drives are operated from a single controller. Data format is serial NRZ, at 48 kbits/s. Block detection allows block count/search operations. An optional PC card provides 8-bit parallel data transfer over a bidirectional data bus. Error detection during both read and read-while-write is also provided, as is complete status reporting.

CIRCLE NO. 811

## Comparator indicates 6 levels of alarm




*United Systems, 918 Woodley Rd., Dayton, OH 45403. Mike Elovitz (513) 254-6251. $895; stock.*

Providing six distinct levels of alarm indication, the 6806 Data Sentinel is half-rack size and weighs 6 lb. Each of the six setpoints has its own thumbwheel switch to assign alarm levels from 00000 to ±19999. A front-panel indicator shows when a limit is exceeded. Each alarm output is through spdt contacts having 2-A (resistive) ratings.

CIRCLE NO. 812

# Diskettes.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**ITC—Far East**
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Tokyo, Japan
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Telex: J 47879

CIRCLE NUMBER 219

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COOL
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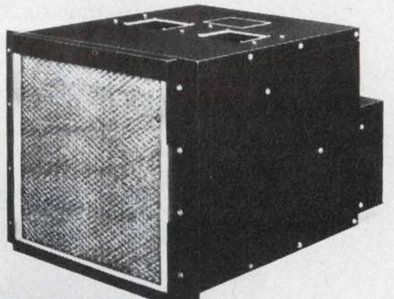
MACHINE
TOOL
SYSTEMS



# McLEAN 6000 BTU AIR CONDITIONER

This compact 19" rack-mounted "LOBOY" provides longer life, more reliability and better performance for electronic equipment. Easy to install. Operates on 115 volts, 60 Hz, draws 12 amps max., weighs only 135 lbs. Centrifugal blowers circulate cool air over entire coil/fin surface for uniform airflow. Constant clean air in contact with electronics. 20,000 hours continuous duty assured in ambients to 125°F.

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CIRCLE NUMBER 220

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CIRCLE NUMBER 221

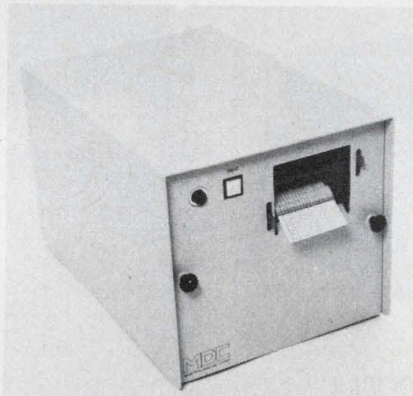
## Programmable processor has high throughput rate

*Stein Associates, 28 Bear Hill Rd., Waltham, MA 02154. Ralph Jackson (617) 891-4700.*

Modular-multiprocessor design enables the AR-10 high-speed processor to operate with high throughput rates and system bandwidth. The FFT-execution time (1024-point complex) ranges from 1.45 to 8.5 ms. Subprocessors operate in parallel and are interconnected by the AR/BUS which performs DMA transfers without cycle stealing. A cross-assembeler and linker written in ANSI Fortran, combined with hidden pipeline operations allows programming with the ease of a minicomputer. The processor has an AR/SCAN panel, which allows operational analysis and program debugging by trapping and displaying data, addresses or other program parameters in any of the subprocessors while the program operates at full speed.

**CIRCLE NO. 813**

## Instrumentation printer has serial interface

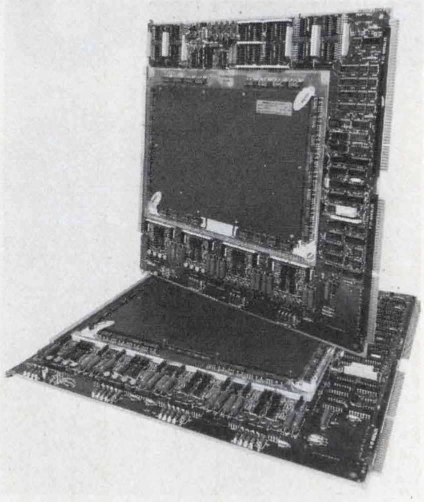



*Master Digital, 1308-F Logan Ave., Costa Mesa, CA 92626. Michael Campo (714) 751-8271. $595; stock to 4 wks.*

RS 232 and 20-ma current loop serial interfaces are available for the MDC 300 Series instrumentation printers. The general-purpose printers are packaged for bench-top or rack mounting. Up to 21 columns of numeric and limited alphabetical data can be printed at 3 lines/s. Features include two-color impact printing, low noise, 100% duty cycle and a printing mechanism with a life of five million lines. Options include: Date/time clock, event counter and low-paper indicator.

**CIRCLE NO. 814**

## 32-k byte add-in memory is totally transparent

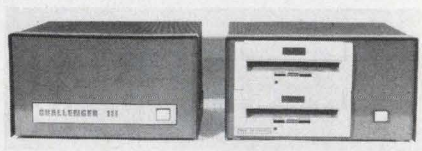


*Ampex, 200 N. Nash St., El Segundo, CA 90245. Clyde Cornwell (213) 640-0150. $1725; stock.*

A 32-k byte add-in memory, the ARM-3, is totally transparent and pin-compatible with the Data General Nova 3 computers. It offers 800-ns full-cycle operation in 16-k modules. Temperature-independent cores provide more uniform performance and wider operating margins over the temperature ranges found in industrial environments. The module operates in any address field and is completely software and hardware compatible with all models of DG's Nova 3.

**CIRCLE NO. 815**

## Triple processor board runs published software



*Ohio Scientific, 11681 Hayden, Hiram OH 44234. (216) 569-7905.*

Challenger III is a triple-processor-CPU board that runs almost all published software for microprocessors, including the 6800, 6502, 8080 and Z-80 programs. It uses the OS-65D disc operating system, and a 74-Mbyte-disc option makes mass data storage possible. Another option is a software-processor-status switch for writing multiple programs. Also included is a 1-Mbyte pager and user-programmable vectors for both the 6502 and 6800 that allow real-time multitasking.

**CIRCLE NO. 816**

# Design aids

## Data communications

A wall-mountable chart provides circuit and operational details for both RS-232C and current-loop data communication. Termiflex.

**CIRCLE NO. 817**

## Stepping-motor technology

For those who like to hear it, there's a 15-minute cassette tape to go with a 52-page "Design Engineers' Guide to DC Stepping and AC Synchronous Motors." The package costs $5. Superior Electric, Briston, CT 06010.

**CIRCLE NO. 818**

## Slide rule

The metric/inch gear computer, a pocket slide rule, indicates 18 different gear functions, inch gear data on one side and metric on the other. PIC Design Div., Benrus Corp.

**CIRCLE NO. 819**

## Process control tables

Conversion tables and engineering data useful in process control are found in a 20-page handbook. The Foxboro Co.

**CIRCLE NO. 820**

## Motor controls

"Selection Guide to Solid State Motor Speed Controls" details each model, giving a full description, dimensions, ratings (amps and voltage), type of mounting, standard and optional features, and typical applications. KB Electronics.

**CIRCLE NO. 821**

## Intelligent terminals

A guide presents the company's intelligent-terminal line in summary form. Included are two charts. The first details the relationship among the standard intelligent terminals in its stored-program-display (SPD) product line. The second chart gives the basic hardware and software characteristics. Incoterm.

**CIRCLE NO. 822**

# Application notes

## Linear LSI products

A 176-page handbook, "Siliconix LSI Design Catalog," provides PC-board layouts, parts lists and construction tips for building prototype systems. Included are application notes, which describe IC functions, operating characteristics and design considerations. Siliconix, Santa Clara, CA

**CIRCLE NO. 823**

## X-Y recorders

How to evaluate X-Y recorders based upon acceleration and slewing-speed specs is shown in a four-page note. Hewlett-Packard, Palo Alto, CA

**CIRCLE NO. 824**

## Data processing

"Distributed Data Processing: The Practical Alternative" describes the advantages of the newest computer phenomenon and how DEC Datasystems can match resources to evolving needs. Digital Equipment, Northboro, MA

**CIRCLE NO. 825**

## Instrumentation

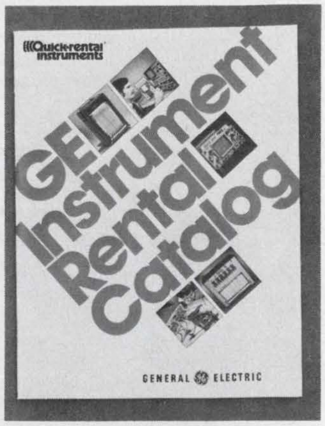
Four application notes are available from Fluke. For the 40-page "System Use of the Fluke Model 8500A," CIRCLE NO. **828**; for the four-page "A Practical Comparison of Average vs True Rms Ac Measurements," CIRCLE NO. **829**; for the 12-page "Models 6010A & 6011A Signal Generators," CIRCLE NO. **831**; and for the 12-page "80T-150 Temperature Probe," CIRCLE NO. **830**. John Fluke Mfg. Co., Mountlake Terrace, WA

## 8085-based $\mu$Cs

A 288-page manual covers operation, specifications and applications of the 8085 and other basic MCS-85 components, general-purpose and dedicated-function peripherals, and standard RAM and ROM components used to expand the system. Copies are $5. Send check or money order to Intel, Literature Dept., 3065 Bowers Ave., Santa Clara, CA 95051

**INQUIRE DIRECT**

# *New literature*




## Test instruments

A 68-page catalog provides detailed descriptions of many of the more than 12,000 electrical and electronic test instruments available for rent. General Electric, Schenectady, NY

**CIRCLE NO. 832**

## Microwave control devices

A 43-page microwave solid-state control-devices catalog features switches, attenuators, limiter and video filters. There are also sections on processing and testing and design-oriented application notes for making rf and video tradeoffs. Crown Microwave, N. Billerica, MA

**CIRCLE NO. 833**

## Connector caps

Product information is available on connector caps for power resistors, with spring fingers made of beryllium-copper and available with or without straps. Carborundum, Niagara Falls, NY

**CIRCLE NO. 834**

## Logic-circuit testing

A 350-page handbook includes chapters on microprocessor testing and field-service testing, describes available programming testing and fault-isolation techniques, and explains how to calculate the optimum comprehensiveness for test programs, how to assign priorities for boards to be programmed, and how to prepare financial analyses. $95 to $165. Omnicomp, Phoenix, AZ

**INQUIRE DIRECT**

## Keyboard modules

Sloped and stepped Hall-effect keyboard modules that may be used as single units, panel arrays or as keyboards are described in an eight-page product sheet that also lists features and typical applications. Honeywell, Freeport, IL

**CIRCLE NO. 835**

## Microcircuits

A step-by-step guide for OEMs to incorporate custom microcircuits in such fields as appliances, autos, communications, business machines, instruments, process controls, and machine tools is provided in a 24-page illustrated brochure. American Microsystems, Santa Clara, CA

**CIRCLE NO. 836**

## Photoelectric sensors

A four-page short-form catalog briefly outlines subminiature photoelectric sensors with electronic controls, including special systems and bar-code reading equipment. Skan-A-Matic, Elbridge, NY

**CIRCLE NO. 837**

## Power relays

Hermetically sealed power relays are described in a two-page bulletin that features diagrams of the internal wiring, operating characteristics and specs as well as ordering information and module dimensions. Struthers-Dunn, Pitman, NJ

**CIRCLE NO. 838**

## Flat cable

Basic data on the advantages of using flat-cable systems, as well as information on types of flat cable and terminations available are offered in a flat-cable design guide. Institute of Printed Circuits, Evanston, IL

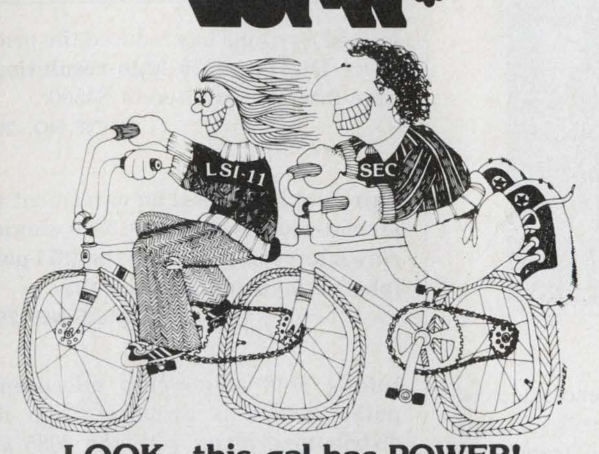
**CIRCLE NO. 839**

## FETs and linear ICs

A 42-page selector guide offers specs, prices and competitive substitution information for JFETs, MOSFETs, some linear ICs, a smoke-detector circuit and new MOS power FETs. Siliconix, Santa Clara, CA

**CIRCLE NO. 840**

# Our love affair with LSI-11*

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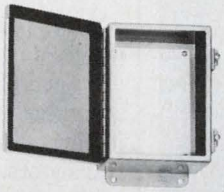
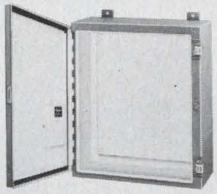
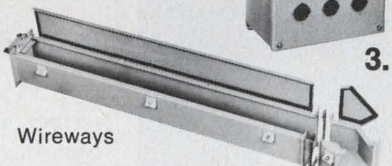




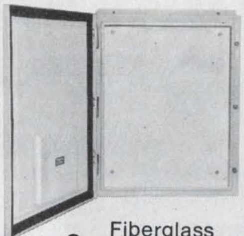
**2.** JIC-type boxes

**3.** Pushbutton enclosures



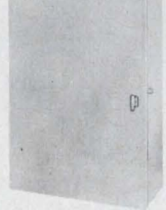
**4.** Wireways

**5.** Consoles and consolets



**6.** Fiberglass enclosures

**7.** Cutout and pull boxes



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CIRCLE NUMBER 241

*NEW LITERATURE*


## Semi products

A 148-page cross-reference and product guide lists and describes transistors, complementary-pair transistors, zener diodes, diodes, color-TV crystals, integrated circuits and field-effect transistors. P.R. Mallory, Indianapolis, IN

CIRCLE NO. 841

## Recording instruments

A 16-page illustrated catalog describes a line of analog and digital recording instruments and systems. It includes key performance specifications for industrial, scientific and biophysical measurements. Gould, Cleveland, OH

CIRCLE NO. 842

## Electronic hardware

A short-form catalog contains detailed specifications, ordering data and prices on cable plugs, socket and terminal strips, transistor and IC sockets, and adapter plugs and covers. SAMTEC, New Albany, IN

CIRCLE NO. 843

## Analyzing instruments

Instruments and systems for analyzing audio-frequency spectra, distortion, frequency response and very-low-frequency phenomena are illustrated in a 16-page brochure. Spectral Dynamics, San Diego, CA

CIRCLE NO. 289

## Metal tubing

Information on available sizes, materials and types of small metal tubing is available in Spec Sheet 100. Handy & Harman, Norristown, PA

CIRCLE NO. 290

# Bulletin board

**United Systems** has reduced the price of its **DigiTec 8320 high-resolution, time-interval counter** to $4500.

CIRCLE NO. 295

**Fairchild** has signed an agreement to **second-source Mostek's 3870 single-chip microcomputer and the 3871 peripheral input/output circuit.**

CIRCLE NO. 296

**Intel's 8748 single-chip microcomputer system** is available from its distributors, along with the 8035 μC and the 8243 I/O expander.

CIRCLE NO. 297

**Burr-Brown** has cut the price of its **Model 4341 true-rms-to-dc converter** up to 20%.

CIRCLE NO. 298

**Solitron Devices** has reduced prices on its **npn power-transistor families.** The 10,000-qty prices are: 2N3054, $0.35; 2N3055, $0.49; 2N3771, $0.82; 2N3772, $0.74 and 2N3773, $1.50

CIRCLE NO. 299

**Raytheon Data Systems** has added IBM 360/20 remote job-entry enhancement to its **PTS-1200 distributed-systems line.**

CIRCLE NO. 351

**Hewlett-Packard** has reduced prices up to 39% on its **light-emitting-diode lamps.**

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**Silicon General's 7800A series of positive fixed-voltage regulators** are interchangeable with the industry-standard SG7800, SG140/340 devices. Using on-chip trimming of output voltage, accuracy can be held to within 1.5%.

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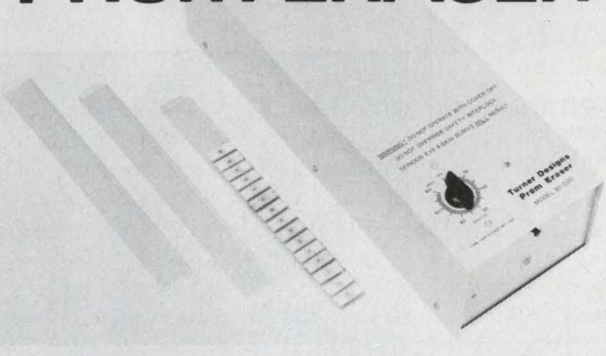
With its support capability for the TMS 9900 μP, the **Tektronix 8002 microprocessor lab** adds the first 16-bit device to the growing family of μPs for which it provides complete software/hardware design, emulation and debug capabilities.

CIRCLE NO. 354

# PROM ERASER

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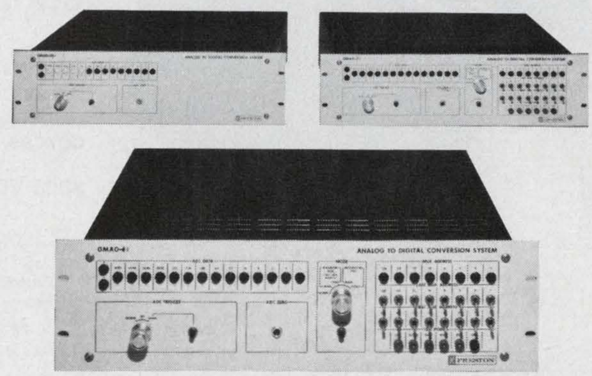
# Here's Preston's answer to "do-it-yourself" card-module ADCs:



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For complete specifications on the GMAD-4, plus detailed timing and interconnection data, ask for your copy of Preston's 12 page GMAD-4 brochure. And if you need information on the other GM Series ADCs that cover the range of conversion speeds from 10 microseconds to 100 nanoseconds, we'll send it along, too.

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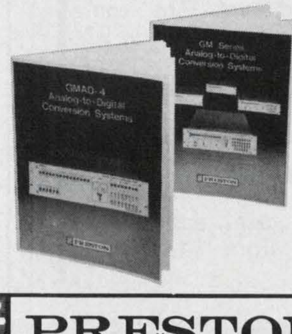


**PRESTON**

**CIRCLE NUMBER 245**

# Across the desk

*(continued from page 7)*

Sure you'll be a great designer someday. Engineers don't dress so conservatively any more.

Sorry. That's Michelangelo Merisi's (Caravaggio) "The Fortune Teller," which hangs in the Louvre in Paris.

## More capabilities than you think

The second paragraph of your article on "Bit-oriented Protocols..." (ED No. 12, June 7, 1977, p. 36) contained a serious misrepresentation of the capabilities of Digital Equipment Corporation's DDCMP protocol.

While it is true that DDCMP is a byte-oriented protocol, it has all the advantages listed for SDLC, and then some.

To be more specific,

1. DDCMP is independent of line characteristics. It runs on full duplex lines quite as successfully as on half-duplex. It also runs on asynchronous lines as well as synchronous—something the bit stuffing SDLC protocol cannot do.

2. DDCMP does lend itself to LSI implementation, and is in fact totally implemented in the microcode of Digital's standard DMC-11 line controller.

3. There are no line turnarounds with DDCMP on full-duplex links. In fact the multiacknowledge feature (one ACK message can acknowledge many data messages), coupled with an ability to acknowledge messages received within control headers of messages being transmitted, makes DDCMP ideal for use over satellite links, where long-line turnaround delays have traditionally been a problem.

4. Error checking is ensured by a CRC16 polynomial, transmitted with both the control information and the user data. The chances are that successful aliasing (an undetected error) on a 9600-baud link would not have occurred had DDCMP been running on it continuously since the start of this century.

In conclusion, future communications probably will not all be "bit-oriented." Rather, it will all be independent of line characteristics, as DDCMP and, to a lesser extent, SDLC are today.

*Ron Kleinman*

Digital Equipment Corp.
2656 Walsh Ave.
Santa Clara, CA 95050

## Give and take

You really know how to hurt a guy!

Not too long ago, I found your "Dear Deer," editorial (ED No. 11, May 24, 1977, p. 51) helpful in driving a salesman out of my office. He had made many claims for the quality of his product, one of which was that his foundry was "OSHA-approved." This really has little to do with the quality of the product. When he repeated it for the third time, I quickly rummaged through my stack of ELECTRONIC DESIGNS, found your editorial and handed it to him. Our meeting drew rapidly to a close.

But in "Time for Decisions" (ED No. 13, June 21, 1977, p. 51), you take poor little me to task. Thanks for the advice. I will try to do better.

*Roy E. Crocker*

CBC Inc.
167 Hamakua Dr.
Kailua, Oahu, HI 96734

## A big wow

I read George Rostky's editorials faithfully and have been meaning to write for some time. But "Time for Decisions" (ED No. 13, June 21, 1977, p. 51):

WHOOPS

It's pasted on the wall to the left of my desk. Right where I can see it—every morning. Lest I forget.

*John S. Simonton, Jr.*
*President*

PAIA Electronics, Inc.
P.O. Box 14359
Oklahoma City, OK 73114

## New Books

**Displays for Man-Machine Systems**—IEE Conference Publication, April 1977, The Institution of Electrical Engineers, PO Box 8, Southgate House Stevenage, Herts. SG1 1HQ, England. UK £8.30, 1441 p. overseas £9.70.

CIRCLE NO. 251

**6800 Programming for Logic Design**—A. Osborne, Osborne & Associates, Inc., P. O. Box 2036, Berkely, CA 94702, 314 p. $7.50

CIRCLE NO. 233

**Electronic Communications**—D. Roddy and J. Coolen, Prentice-Hall Inc., Englewood Cliffs, NJ 07632, 706 p. $19.95

CIRCLE NO. 256

**Introduction to Circuit Synthesis and Design**—G. C. Temes and J. W. LaPatra, McGraw-Hill Book Co., 1221 Avenue of the Americas, New York, N.Y. 10020, 598 p. $21.50

CIRCLE NO. 257

**A User's Handbook of Semiconductor Memories**—E. R. Hnatek, John Wiley & Sons, Inc., 605 Third Ave., New York, NY 10016, 652 p. $29.50

CIRCLE NO. 258

**Digital Filters**—R. W. Hamming, Prentice-Hall Inc., Englewood Cliffs, NJ 07662, 226 p. $17.95

CIRCLE NO. 259

**Applying Microprocessors**— edited by L. Altman, S. E. Scrupski, McGraw-Hill Book Co., 1221 Avenue of the Americas, New York, NY 10020, 191 p. $15

CIRCLE NO. 277

**MOS/LSI Databook—National Semiconductor,** 2900 Semiconductor Drive, Santa Clara, CA 95051, 714 p. $4

CIRCLE NO. 278

**Logical Design Using Integrated Circuits**— W. D. Becher, Hayden Book Co., 50 Essex St., Rochelle Park, NJ 07662, 320 p. $17.95

CIRCLE NO. 279

**Power Transistor and TTL Integrated-Circuit Applications**—Texas Instruments, P. O. Box 5012, Dallas, TX 75222, 248 p. $16.50

CIRCLE NO. 280

**Microprocessor Basics**—edited by M. Elphick, Hayden Publishing Co., 50 Essex St., Rochelle Park NJ 07662, 215 p. $9.95

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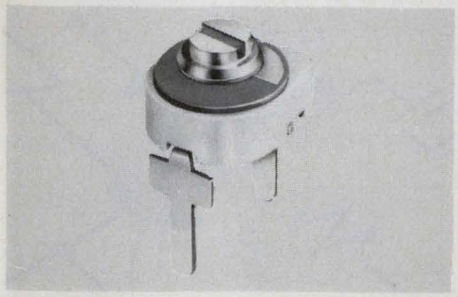

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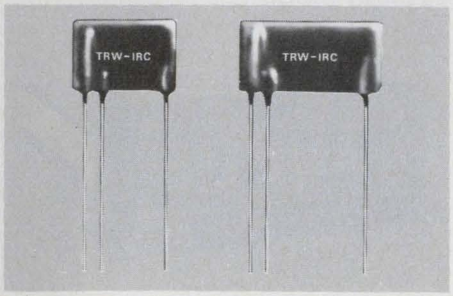
TRIMMER CAPACITORS **181**

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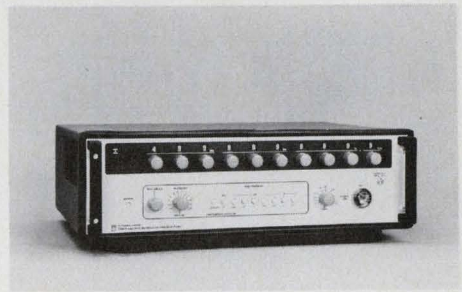
HIGH VOLTAGE RESISTORS **184**



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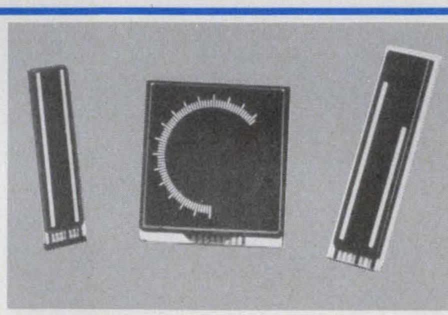
MAGNETIC SHIELDING **182**



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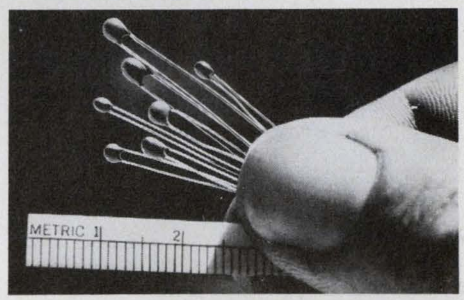
BAR GRAPHS **185**

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THERMISTOR **188**

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WL TWO-CIRCUIT LIMIT SWITCHES **183**

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E3N PHOTOELECTRIC SWITCHES **186**

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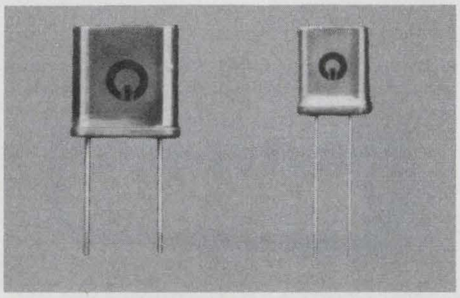
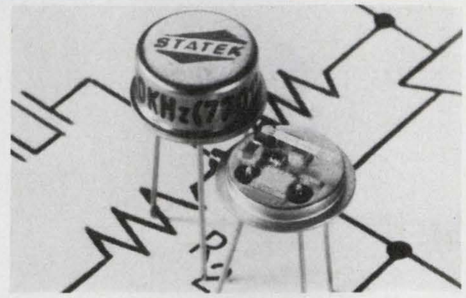


**HIGH STABILITY LOW COST QUARTZ CRYSTAL** for $\mu$-processor and clock oscillator. Accuracy is ±0.002% at 25°C, Frequency change over −10 to +55°C is within ±20ppm. 1.000, 1.8432, 2.000, 2.097152, 2.4576, 3.2768, 4.0000, 5.0000, 5,0688, 5.1850, 5.7143, 6.5536, 10.0000, 18.0000, 18.4320, 20.0000, 22.1184 Immed. Dlvy. $1.85 ea. 10 MHz up in HC-18/u; (Min. 100 pcs.) Q-MATIC CORP., 3194-D Airport Loop Dr., Costa Mesa, CA 92626, (714) 545-8233, Telex 678389

CRYSTAL 190

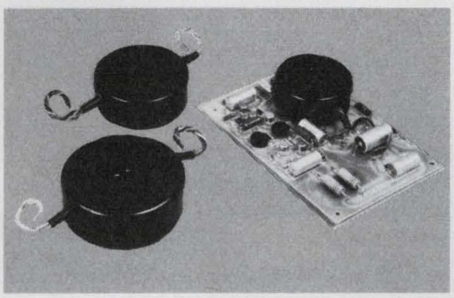

**Digital AC line monitor Model 37DLM** is designed to measure voltages associated with AC power lines or systems. It offers accuracy of 1/2% and ease of readability at distances to 20 feet. Ranges are 200 or 400 volts with 0.1 volt resolution or 600 volts with 1 volt resolution at frequencies from 45 Hz to 20 kHz. Prices start at $164 (discounts to OEM). Availability 3-4 weeks. GRALEX INDUSTRIES, 155 Marine Street, Farmingdale, N.Y. 11735 (516) 694-3607

DIGITAL PANEL METERS 193



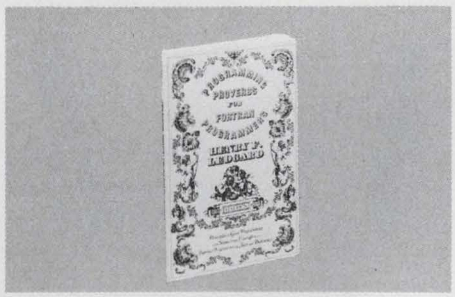

**CMOS Crystal Oscillators in Low profile TO-5.** Frequency range is 10 kHz to 300 kHz (divided outputs to 1 kHz, low as one cycle per month available). Low milliamp current consumption. Accuracy ±0.01%. Shock 1000 g. Hybrid thick and thin film chip and wire design is rugged and ideally suited for portable equipment. Details in Gold Book & EEM * STATEK CORP * 512 N. Main, Orange, Ca. 92668 * (714) 639-7810 * Telex 67-8394.

CRYSTAL OSCILLATOR 196



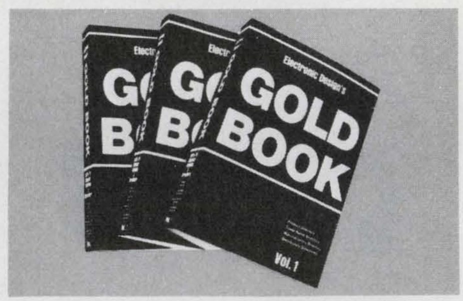
Off-the-shelf, in any quantity, toroidal line transformers are available with 75 most commonly used (6 to 40V) secondaries, 2 x 115V primaries, in 15, 30, 50, 90 and 130VA ratings. Toroids can solve your problems — they have an 8:1 smaller hum field — are 50% lighter — with 50% smaller volume over electrical equivalents — and fully encapsulated in resin filled tough thermoplastic shells. High efficiency saves power, cuts temperature. Green-Shaw Co. Inc., 70 Bridge Street, Newton, MA. 02195 Tel: (617) 969-8900.

TOROIDAL TRANSFORMERS 191



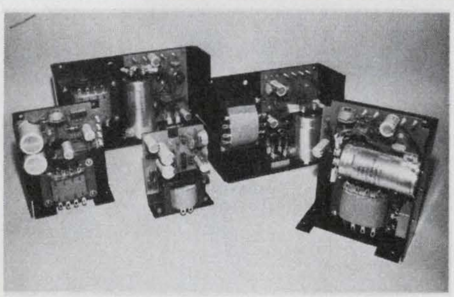
**PROGRAMMING PROVERBS FOR FORTRAN PROGRAMMERS,** H. F. Ledgard. These 26 unique "proverbs," or rules and guidelines, are specially designed to help FORTRAN programmers upgrade the quality of their work. Comes with many sample programs. #5820-9, 144 pages, $6.95 . Circle the Info Retrieval Number to order 15-day exam copy. When billed, remit or return book with no obligation. Hayden Book Co., 50 Essex Street, Rochelle Park, N.J. 07662.

PROGRAMMING PROVERBS 194



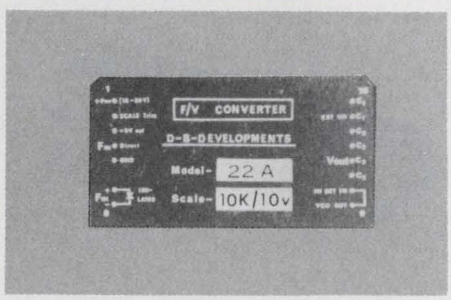

**THE '77-'78 GOLD BOOK IS NOW OFF THE PRESS.** Contains 2,496 pages of up-to-the-minute information about the entire electronics industry. Complete with Product, Trade Name, Manufacturers, Distributors Directories and Catalogue Compendium. Price: $30–U.S., Canada and Mexico. Other countries $40–Overseas postage included. To order, send check or company purchase order to GOLD BOOK, Dept. #437-R, Hayden Publishing, 50 Essex St., Rochelle Park, NJ, 07662.

'77-'78 GOLD BOOK 197



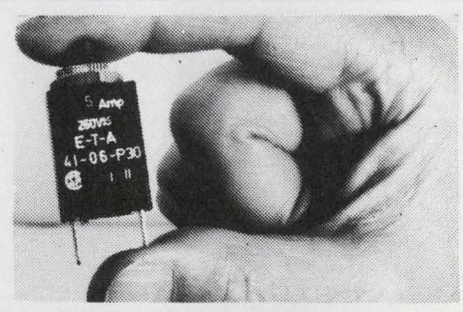
**45 different Open Frame Power Supply models** are available with outputs ranging from 5Vdc to 24Vdc and 500 mA to 15 Amps. Regulation is ±0.05% for line and ±0.15% for load. Ripple and noise is less than 5mV max P-P. Standard on all models is a 110/220Vac transformer. Units have a 5 year warranty. COMPUTER POWER SOURCE, INC., 370 Park Ave., Worcester, MA 01610. Contact: Steve Banks 617-752-8972

POWER SUPPLIES 192



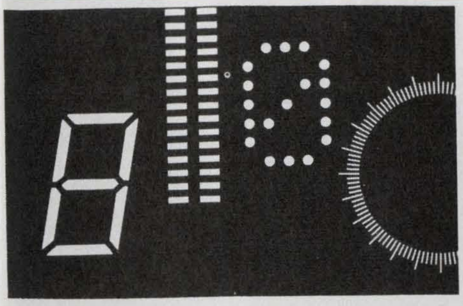

**NEW, RIPPLE-FREE F/V CONVERTER.** A new Design Technique combines ripple-free conversion with fast response. Self-contained (models 22A,B) 10 Khz modules offer linearities to 0.005%, slew rates of 2.5volts/millisec, and a residual ripple of less than 1/2 mv peak to peak. Single (10-16v) and dual (± 15v) supply operation available. Four decade dynamic frequency range — 2" x 1 1/2" x 1/2". A basic F/V building block that works. D-B-Developments, 7709 Kilbourne Rd, Rome, NY 13440 (315) 339-1265

RIPPLE-FREE F/V CONVERTER 195



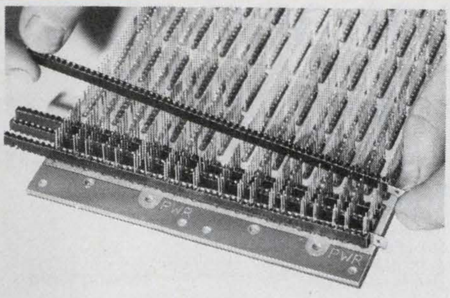

**Overcurrent Protector,** manual reset eliminates fuse replacement. Convenient panel mounting. 19 fractional ratings from 0.1 to 5 amp. Other models up to 400 amp. Trip-free and fool-proof, UL and CSA approved. High quality, low cost $1.39 ea. in 1000 lots. E-T-A Products Co. of America, 7400 N. Croname Rd., Chicago, Ill. 60648. Tel: (312) 647-8303. Telex: 253780.

CIRCUIT BREAKER 198



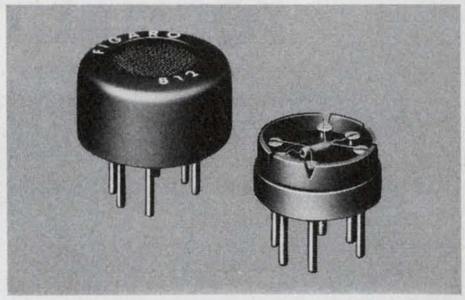
**Power converters for gas discharge displays** DC-to-DC power supplies convert low DC line voltages of 5, 9, 12 or 15 volts to nominal 200 or 250 volt DC levels required to activate gas discharge displays (multi-segment, matrix or bar graph). Ideal for battery powered applications. Ask about custom designs and cost-efficient models for high-volume users. For PC board mounting. ENDICOTT COIL CO., INC., 31 Charlotte Street, Binghamton, N. Y. 13905 (607) 797-1263.

DC-to-DC CONVERTER 199



**QUIK/STRIP BY ROGERS.** Fast, low-cost system for connecting in-line pins on DIP socket boards and connector arrays. Shock and vibration resistant. 18 gauge current capacity. Can be used on pin densities as high as .100" x .100" and be stacked two or more high. Write or call for details. Rogers Corporation, Chandler, AZ 85224. Phone: (602) 963-4584. (EUROPE: Mektron NV, Gent, Belgium; JAPAN: Nippon Mektron, Tokyo.)

QUIK/STRIP 202



**FIGARO GAS SENSOR TGS** is a gas sensitive semiconductor. When combustible gas is absorbed on the sensor surface, a marked decrease of electrical resistance occurs. Major features of the sensor include high sensitivity, long term reliability and low cost. The applications are: GAS-LEAK ALARM, AUTOMATIC FAN CONTROL, FIRE ALARM, ALCOHOL DETECTOR, etc. Figaro Engineering Inc., North America Office-3303 Habor Boulevard, Suite D-8, Costa Mesa, Calif. 92626 Tel: (714) 751-4103 Telex: 678396

GAS SENSOR 205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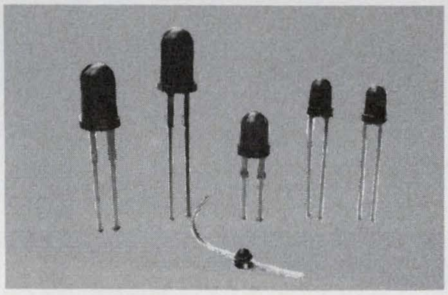
INDUSTRIAL PRESET COUNTER 200



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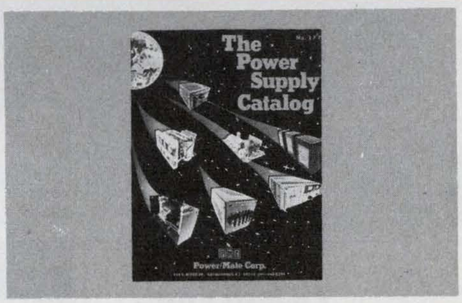
ULTRA BRIGHT LED's 203

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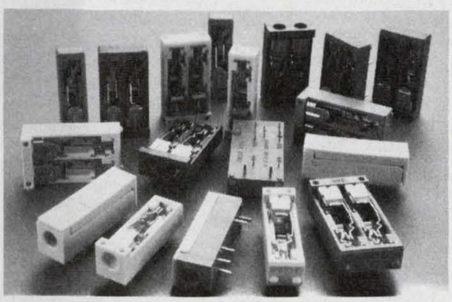
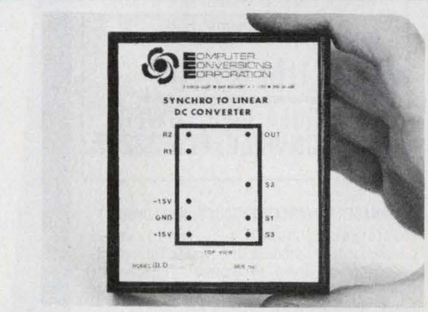
SWEEP GENERATOR 201



**NEW PCB-JACKS,** designed for PC-board mounting, are 1/2 the size of conventional Bantam jacks, 1/3 the size of Long-frame jacks. Solder them directly to the PC-board and eliminate connecting wires and mounting hardware. Compatible with Bantam plugs. ADC Products, 4900 W. 78th, Minneapolis, MN 55435. (612) 835-6800.

PC-BOARD JACKS 204

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SYNCHRO TO LINEAR DC 207

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|---|---|---|
| Oct. 7 | **Sept. 23** | Oct. 25 |
| Oct. 21 | **Oct. 7** | Nov. 8 |
| Nov. 4 | **Oct. 21** | Nov. 22 |
| Nov. 18 | **Nov. 4** | Dec. 6 |
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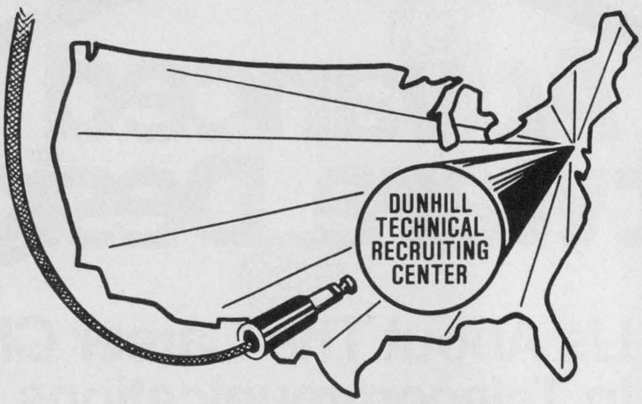


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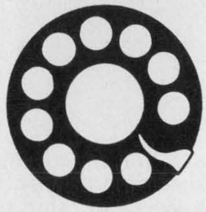

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Sony Corporation of America, the largest supplier of video equipment in the world, is expanding its technical staff to service broadcast and industrial users of state-of-the-art video equipment. We are looking for engineers with strong technical backgrounds and maintenance experience with video products such as VTRs, studio color cameras, time-base correctors, and related signal-processing equipment.

Job openings as follows:

**MANAGER OF INSTALLATION AND SERVICE:** Direct a staff of product engineers in providing full support of all broadcast product lines. Formulate procedures to ensure that all installations are carried out according to spec and provide technical guidance to see that field people are properly trained and equipped to maintain the product with a high degree of efficiency. Candidate should possess an EE degree, have proven ability to manage a technical group and have several years of direct involvement in servicing broadcast customers.

Location — N.Y.C. area

**VTR PRODUCT ENGINEERS:** Assume complete product-support responsibility for specialized video tape recorders. Evaluate field problems, prepare service literature in rough form for engineering change notices, field modifications and service bulletins. Train regional engineers to understand and maintain new products. Candidates should possess an EE degree and have thorough technical knowledge of studio-type recorders and maintenance procedures with at least three years of direct maintenance experience.

Location — N.Y.C. area

**COLOR-CAMERA PRODUCT ENGINEERS:** Assume complete product-support responsibility for state-of-the-art ENG. cameras. This includes follow-up on field and application problems, training of field people and the generation of technical support literature such as service/modification bulletins and engineering change notices. Candidates should possess an EE degree and have in-depth knowledge of modern multiple pick-up tube cameras amd alignment techniques with a minimum of three years experience in direct maintenance.

Location — N.Y.C. area

**VIDEO ENGINEERS.** Work with customers to service video equipment at customer's location and on the bench in regional service labs. Provide on-site training for customer technicians. Candidates should possess an associate degree or equivalent, have an in-depth knowledge of video and VTR systems, and have a minimum of three years direct maintenance experience.

Locations — N.Y.C., Los Angeles, Chicago, Dallas, Atlanta

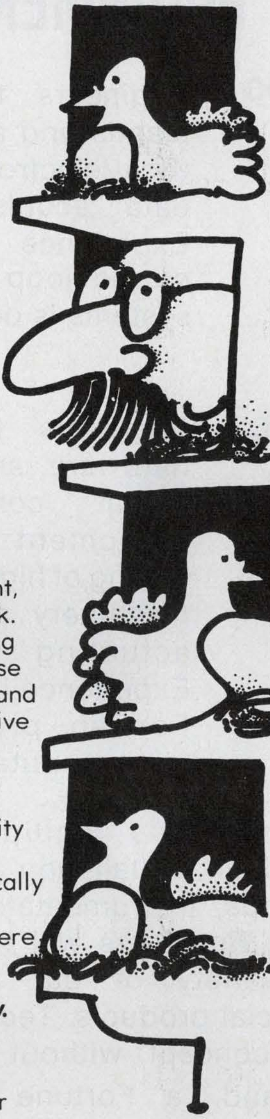
All positions offer excellent salaries and growth potential. Employment benefits are fully paid by the company and include family-coverage hospitalization, pension plan, profit sharing, life insurance and tuition refund.

This may be your opportunity to join a technically-oriented team in which the opportunities to move forward professionally are better than can be found in most areas of the profession today.

**Send your resume in complete confidence to Mr. Jerry McGinty at:**

## SONY
**CORPORATION OF AMERICA**
**47-47 Van Dam Street, Long Island City, N.Y. 11101**
*an equal opportunity employer m/f*

# Engineers... are you pigeonholed?



We won't keep you pigeonholed in the same old assignment, year after year. After all, variety is the spice of a life's work. And we have a commitment to it. We make our living selling variety: command and control systems, complete air defense systems, radar systems, sonar systems, computer systems and much more. We're part of a company of 36,000 people, active in more than 550 major product areas in 80 technologies. Plenty of room for developing interests, plenty of room for growth.

Our Systems Division engineers enjoy technical diversity because of our program variety, and growth opportunities that we're steadily expanding. They benefit from the technically oriented management which put us on our strong growth curve. And they enjoy a good professional environment, where many of our people wear 10, 15, and 20 year service pins.

**Any more good news? Well, yes. We're hiring *now*.**

**For quick action, reach for your phone instead of your resume...** call M. F. Duggins collect (714) 871-4080, Ext. 5410 between 8 A.M. and 4 P.M. Monday through Friday. Or send your resume to: Professional Employment—Ground Systems Group C, 1901 W. Malvern, Fullerton, CA 92634.

U.S. citizenship required • Equal opportunity M/F/HC employer

**HUGHES**

HUGHES AIRCRAFT COMPANY

**Communications System Engineers.** Must understand hardware/software interaction, signal processing, spread spectrum.

**Senior Systems Engineers.** Tactical, strategic system application of radar, sonar communications, electro-optical software, data processing and command and control technologies.

**Communication Analysts.** Lead/direct application of systems theory, applied math, estimation, probability to communication system problems.

**Data Processing and Software Analysts.** System level data processing architecture analysis, design, performance evaluation for multisensor systems.

**Display System Engineers.** Long term opportunity to lead display product definition/selection for military C&C Systems.

**Radar Systems Engineers.** Lead/direct radar system conceptual design/analysis. Integration of radar, weapon, command and control systems.

**Senior Air Defense Engineers.** BSEE, Math or Physics, project management experience in real-time hardware software systems.

**Hardware System Engineers.** Large scale data processing, peripheral, display systems design, specification, integration checkout.

**Systems Analysts.** Systems Theory, applied math background. Variety of problems requiring modern analysis techniques.

# Advertiser's index

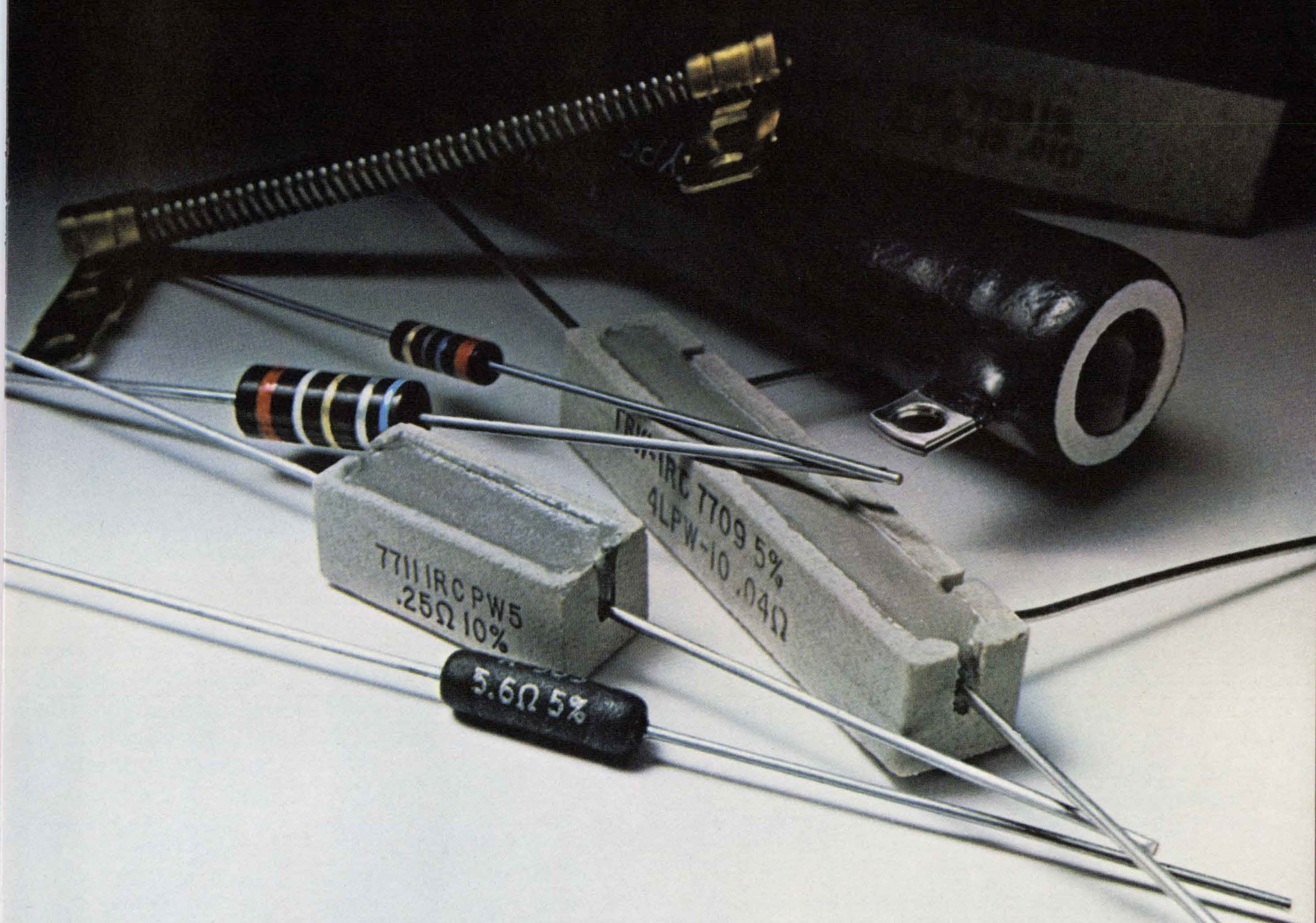
**Advertisers in non-U.S. edition*

# Product index

**Information Retrieval Service.** New Products, Evaluation Samples (ES), Design Aids (DA), Application Notes (AN), and New Literature (NL) in this issue are listed here with page and Reader Service numbers. Reader requests will be promptly processed by computer and mailed to the manufacturer within three days.

What's TRW up to now?

# Wirewounds that save.




For pennies you can buy circuit protection with our BWF series resistors, perhaps saving your company a bundle later. U.L. approved, they will fail safe under specified overload conditions.

And when it comes to cost and reliability, our molded BW and ceramic PW series are standards for 1-22W general purpose applications.

For higher power we've introduced new PW styles in 30, 40 and 50W ratings. Integral mounting brackets boost power dissipation up to 30%.

And, if it's good sense you're after, our 4LPW series is designed for current sensing and feedback circuits. Available in 5 ratings from 3 to 15W, with 2 or 4 leads, and resistance values as low as .01Ω.

For standards in all types of resistors, contact your local TRW distributor. Or TRW/IRC Resistors, 401 N. Broad St., Philadelphia, Pa. 19108. (215) 922-8900, Dept. W.

**TRW IRC RESISTORS**

*ANOTHER PRODUCT OF A COMPANY CALLED TRW*

**CIRCLE NUMBER 231**

With new solid-state options . . .

# RCA helps you make discoveries in power design.

New devices. New packages. New parameters. All from the Powerhouse, your source for the widest choice in SCRs and Triacs. They offer you the latest ways to improve design, reduce costs and increase performance.

**A new way to heat.** Solid-state induction heating is now entirely feasible, thanks to our new 40A asymmetrical SCR (ASCR). The RCA S7310 gives you 40 kHz frequency, high voltage and current. Plus high di/dt and dv/dt capability. No need for 50/60 hertz transformers and other bulky parts.

**A new way to switch.** Now you can design-out some of the problems you've had with big dc relays—such as too much cable bulk in cars. Use our new plastic G4000 Series gate turn-off SCRs (GTOs)—they can switch up to 15 amps with as little as -6V gate turn-off voltage.

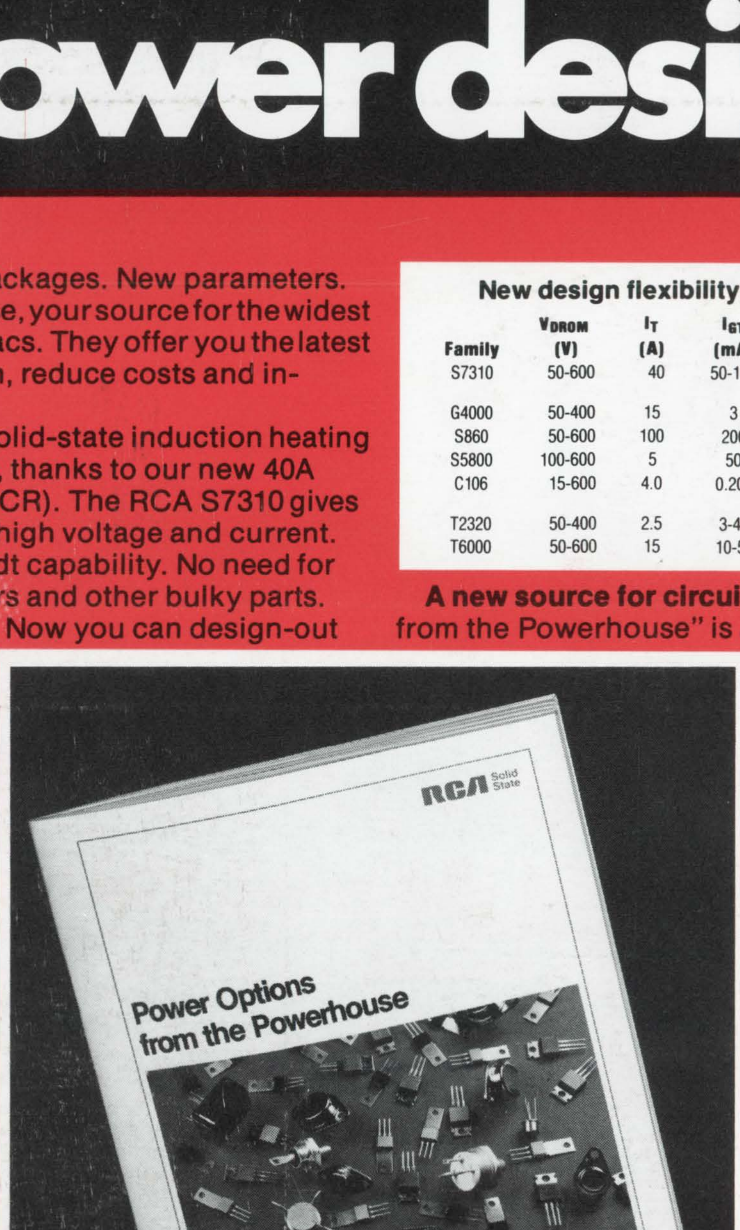
**A new source for the C106.** This popular 4A general purpose SCR and corresponding sensitive-gate triac are now available from RCA. In the economical, easily mounted 3-lead Versatab package.

**New design flexibility for you. From RCA.**

| Family | $V_{DROM}$ (V) | $I_T$ (A) | $I_{GT}$ (mA) | Description | Pkg. |
|---|---|---|---|---|---|
| S7310 | 50-600 | 40 | 50-100 | Fast Asymmetrical SCR | TO-48 |
| G4000 | 50-400 | 15 | 3 | Gate Turn-off SCR | TO-220 |
| S860 | 50-600 | 100 | 200 | Gen. purpose SCR | ½" stud |
| S5800 | 100-600 | 5 | 50 | Fast switching SCR | TO-220 |
| C106 | 15-600 | 4.0 | 0.200 | 4-amp gen. purp. SCR | TO-202 |
| T2320 | 50-400 | 2.5 | 3-40 | Sensitive-gate triac | TO-202 |
| T6000 | 50-600 | 15 | 10-50 | Gen. purpose triac | TO-220 |

**A new source for circuit ideas.** "Power Options from the Powerhouse" is a new designer's guide to the selection of optimum RCA solid-state devices for power circuits. It's arranged by application, with over 40 circuits shown. This makes it easy for you to choose the type best suited to the job.

For your free copy, contact RCA Solid State headquarters in Somerville, NJ; Sunbury-on-Thames, Middlesex, England; Quickborn 2085, W. Germany; Ste.-Anne-de-Bellevue, Quebec, Canada; Sao Paulo, Brazil; Tokyo, Japan.




**RCA Power experience is working for you.**

RCA

CIRCLE NUMBER 232