66-MBYTE/S BUS EASES MULTIPROCESSING

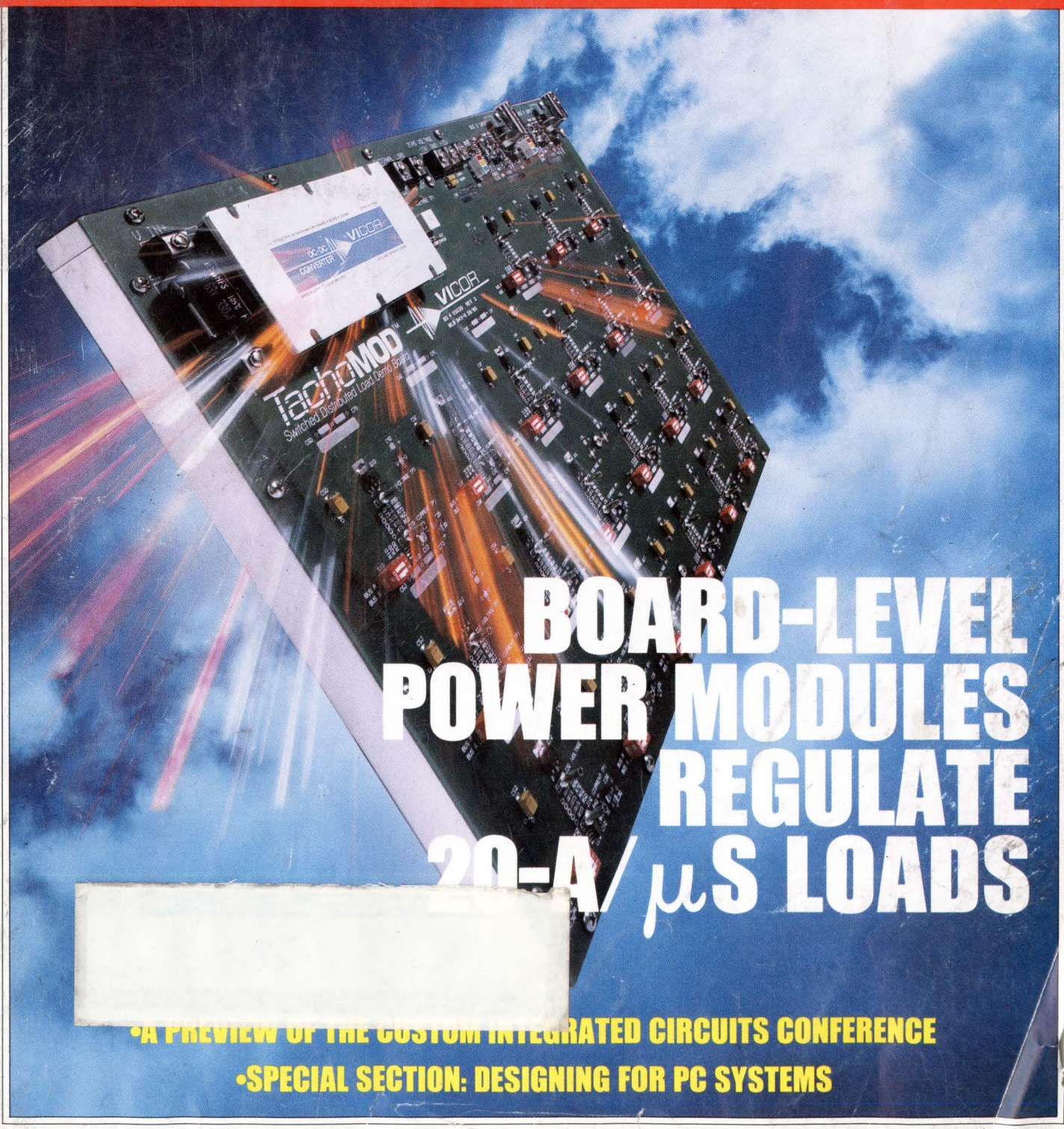
UNDERSTANDING BIT-ERROR-RATE TESTING

FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

ELECTRONIC DESIGN

A PENTON PUBLICATION U.S. $5.00

MAY 9, 1991



BOARD-LEVEL POWER MODULES REGULATE 20-A/μS LOADS

•A PREVIEW OF THE CUSTOM INTEGRATED CIRCUITS CONFERENCE

•SPECIAL SECTION: DESIGNING FOR PC SYSTEMS

Knock-your-socks-off PLD software on a shoestring budget.

Who says you can't afford the world's best PLD development tools? Data I/O®'s industry-standard design software and programming solutions are more powerful—and more affordable—than ever before. So now the best tools on the market are also the best value.

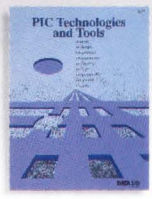
NEW ABEL™-4 marks a major milestone in PLD software. The leader in device support, ABEL-4 automatically identifies which PLDs match your design needs with new SmartPart™ intelligent device selection. New optional device fitters automatically assign pins and configure macrocells for complex device architectures. And an all-new user interface speeds the entire PLD design process.

A major new version of the leading schematic capture software, **NEW FutureNet®-5,** redefines "ease-of-use" with pop-up menus, extensive dialog boxes and a fast symbol browsing feature.

To make designing for testability practical, choose **NEW PLDgrade.™** This inexpensive fault grading software helps you optimize your design for testability before production.

And the affordable **NEW 2900 Programming System** brings the cost of high-performance programming down to earth. Its innovative technology makes programming any PLD—even surface-mount devices—fast and easy.

CALL TODAY for your FREE tutorial on designing with PLDs—a $12.95 value.



1-800-247-5700

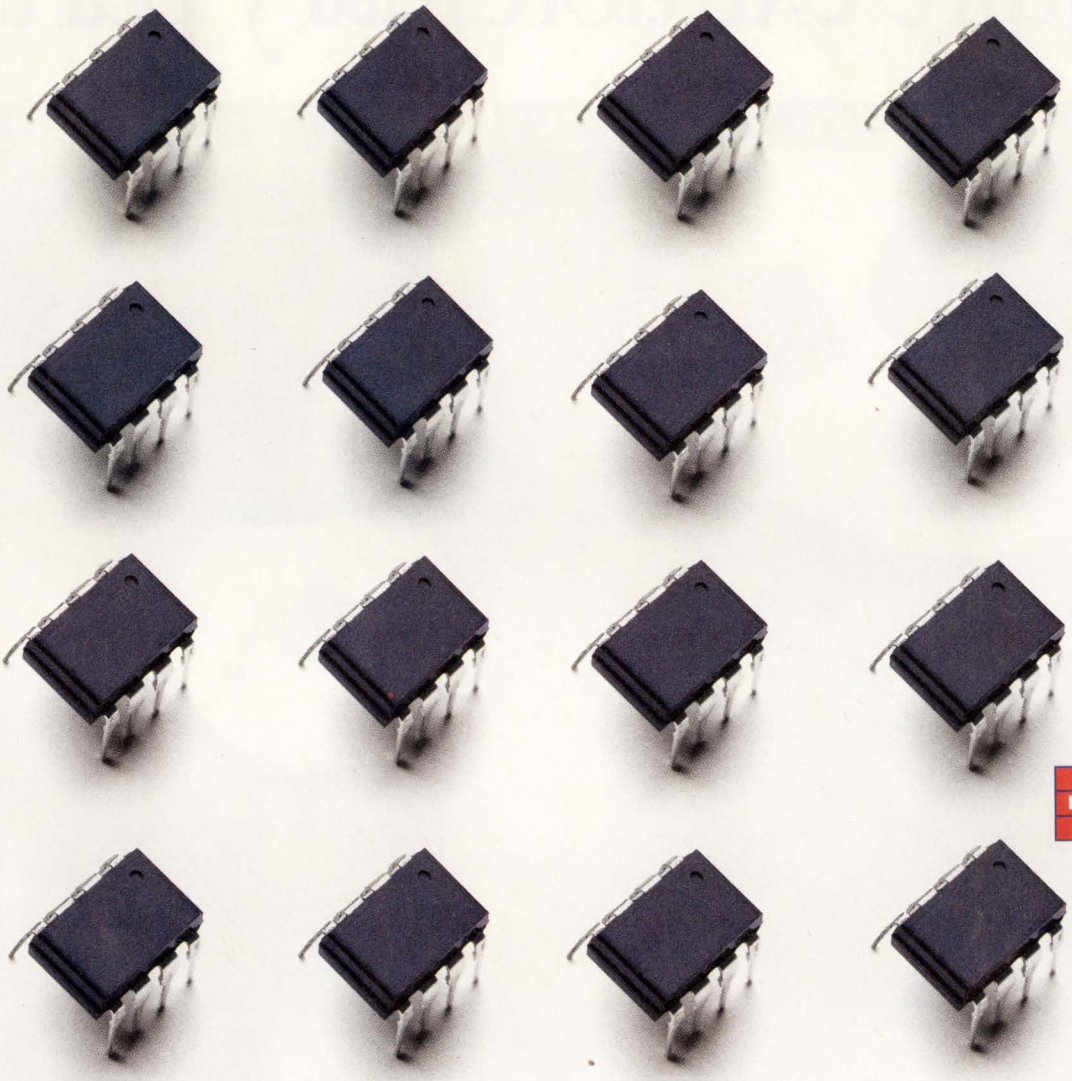
The Personal Silicon Experts

DATA I/O Corporation

ata I/O Corporation 10525 Willows Road N.E., P.O. Box 97046, Redmond, WA 98073-9746, U.S.A. (206) 881-6444/1-800-247-5700
ata I/O Canada 6725 Airport Road, Suite 302, Mississauga, Ontario L4V 1V2 (416) 678-0761
ata I/O Europe World Trade Center, Strawinskylaan 633, 1077 XX Amsterdam, The Netherlands + 31 (0)20-6622866
Data I/O Instrumatic Electronic Systems Vertriebs GmbH Lochhamer Schlag 5A, 8032 Graefelfing, W. Germany, + 49 (0)89-858580
Data I/O Japan Sumitomoseimei Higashishinbashi Bldg., 8F, 2-1-7, Higashi-Shinbashi, Minato-Ku, Tokyo 105, Japan
011-81-3-3432-6991/Telex 2522685 DATAIO J

©1991 Data I/O Corporation

No two alike.



Authorized
HALL-MARK ELECTRONICS
HAMILTON/AVNET ELECTRONICS
Lex Electronics
Distributors

While HP's high-performance plastic optocouplers may all look alike, the similarity is only skin deep.

Because as the largest optoelectronic supplier in the U.S. and one of the world's leading suppliers of optocouplers, we can actually offer you five completely different lines of plastic devices with an equally wide range of performance options.

Such as an innovative dual-channel design that combines a photon-emitting diode with a high-speed photon detector to produce data rates up to 40 MBd.

You also get high-output gain from low-input current or high-speed logic gates. Wide Vcc from 4.5 to 20 volts. And a unique AC/DC interface.

Plus, they're compatible with TTL, STTL, LSTTL, and, in many cases, CMOS logic families.

All of which makes HP's optocouplers the ideal solution for problems caused by ground loops and induced common mode noise.

No wonder HP sets the standard for quality, reliability, and innovation. To find out more about HP's optocouplers, call **1-800-752-0900, ext. 2324.** You'll soon see why there's nothing quite like working with the best.

There is a better way.

HEWLETT PACKARD

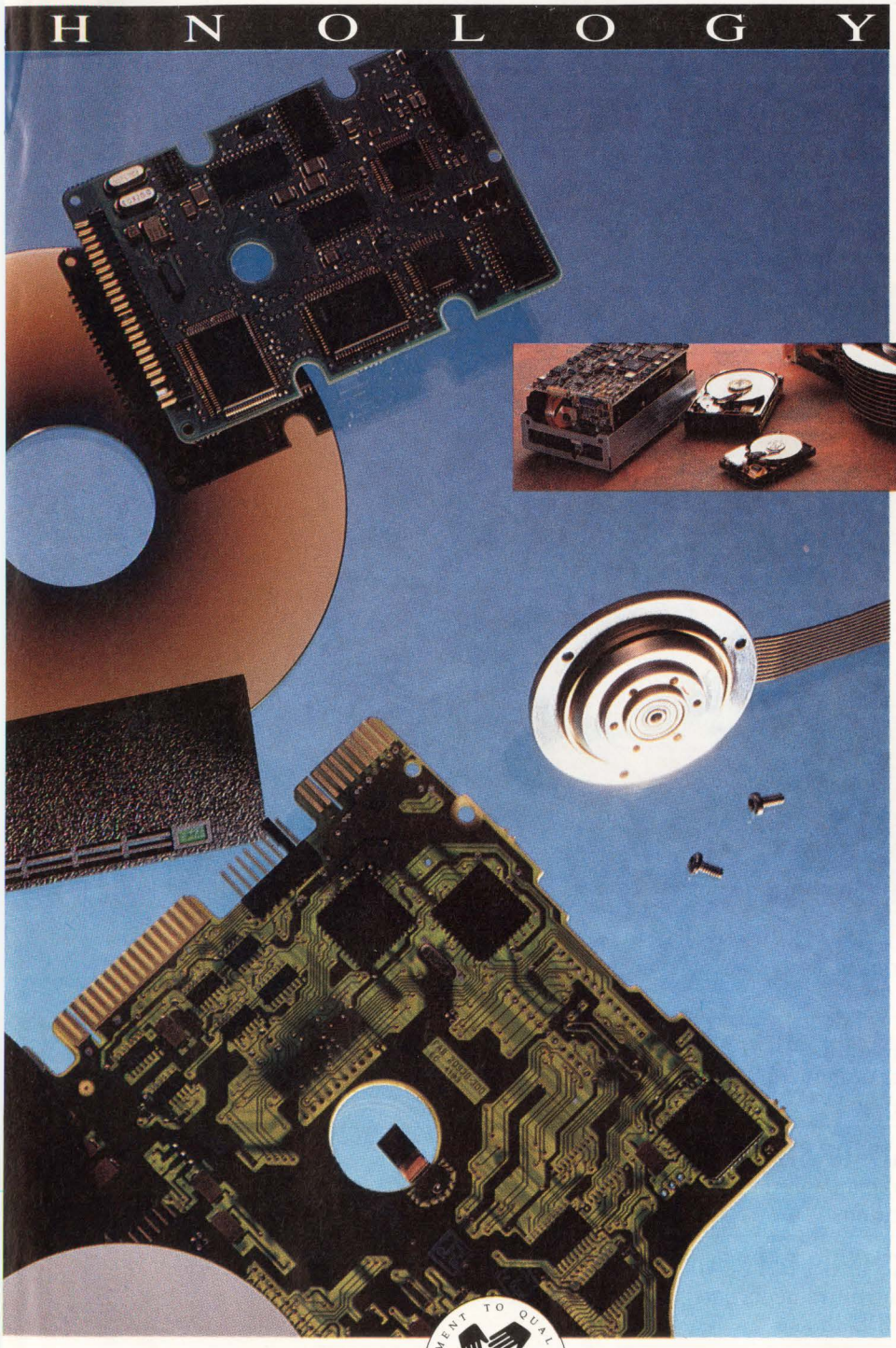
CG08907A

CIRCLE 148

Extraordinary disc drives require extraordinary parts.

Seagate and the Seagate logo are registered trademarks of Seagate Technology, Inc.
© 1991, Seagate Technology, Inc.

H N O L O G Y



Today's disc drives are smaller in size and larger in capacity than ever before due to advances in component technology. By designing and manufacturing most of the components ourselves—a concept called vertical integration—we can control the technology, cost, availability and quality of these critical parts.

Technically speaking, no one builds more advanced thin-film discs and recording heads than Seagate. These core technologies help us put 3 gigabytes of storage in a box the size of a toaster. And because we design our own components, we can bring our new products to market faster.

Of course, a key consideration in building our own parts is the cost. By controlling the manufacturing process down to the component level, we can have a significant impact on the cost of our finished products. The end-result is a better value for the customer without sacrificing quality or performance.

In terms of availability, it's important to know that Seagate shipped over 7 million disc drives last year alone. With volumes like these, building our own components helps us avoid the parts shortages that often plague other disc drive manufacturers.

Most importantly, vertical integration allows us to maximize the quality of every component we produce. With the industry's most advanced equipment and testing techniques, we consistently turn out components and finished products that are beyond reproach.

Obviously, it takes an extraordinary capital investment to pursue this strategy. But the disc drive companies who control their critical component production will be better able to control their own destinies, as well as those of their customers.

For more information on our complete line of high-performance disc storage products, contact your authorized Seagate distributor. Or call Seagate at 800-468-DISC, or 408-438-6550.

A COMMITMENT TO QUALITY

Seagate

The first name in disc drives

CIRCLE 162

MAY 9, 1991 VOL. 39, NO. 9

ELECTRONIC DESIGN

TECHNOLOGY ANALYSIS **47 CICC ACCENTS GLOBAL ASIC TECHNOLOGY**
Papers from over 30 countries describe the latest in analog and digital ASICs and design software.

COVER FEATURE **59 DC-DC CONVERTER HANDLES DISTANT 200-A/μS LOADS**
Power module exiles effects of inductance and capacitance that lie between it and loads changing at 200 A/μs.

DESIGN APPLICATIONS **71 ENSURE THE ACCURACY OF BIT-ERROR-RATE TESTS**
To properly evaluate digital transmission systems, users must understand their BER tester's specifications.

PRODUCT INNOVATIONS **135 FAST BUS NETWORKS CPUS, DSPS FOR MULTIMEDIA SYSTEMS**
Take on real-time control and multimedia needs with a 66-Mbyte/s bus that couples multiple DSP and CPU chips.

140 ICON-BASED SOFTWARE LETS ENGINEERS BE ENGINEERS
A visual engineering environment frees engineers from the chore of programming test controllers.

14 EDITORIAL

18 TECHNOLOGY BRIEFING
Europe is getting ready for HDTV

25 TECHNOLOGY NEWSLETTER
- Software manages VHDL source-code creation
- Light beam accelerates pattern recognition
- Supercomputer sets speed record
- GPS receiver fits in hand
- Joint wafer-bonding pact reached
- Laminate safe for environment
- 28-pin PGA has MIL memories
- Mixed-signal ASICs get 0.7-μm 2-poly CMOS

31 TECHNOLOGY ADVANCES
- Overhauled Transputer architecture ups throughput to over 200 MIPS, 25 MFLOPS
- Advanced circuit/process lets high-side MOSFET/IGBT driver IC also sense current
- Chips/pulse transformer build HV high-side drivers
- Simple liquid-phase epitaxial process yields 22.3%-efficient GaAs solar cells

PC DESIGN SPECIAL EDITORIAL SECTION
87 PC Design Newsletter
91 The PC as an EDA platform: Is the PC up to the task?
101 Build a speedy low-cost graphics accelerator in hardware
110 PC Design Products

Certificate of Merit
Winner, 1988
Jesse H. Neal Editorial
Achievement Awards

Cover: Jook Leung

117 IDEAS FOR DESIGN
- Voltage limiter is adjustable
- Keep Spice accuracy above 1 MHz
- Develop ISA BIOS on a PC

127 QUICK LOOK
- Perspectives on Time-to-Market: Graphing the project
- Smart pressure transmitters—a booming market
- Multichip modules reshape packaging
- Free software for programmable logic design

133 PEASE PORRIDGE
What's all this "SMWISICDI" stuff, anyhow?

NEW PRODUCTS
145 Digital ICs
Second-generation Max family boosts density fivefold
Revamped versions of 29000 RISC CPU up performance, trim cost
Midrange-density FPGAs deliver more features
153 Communications
156 Analog
ADC with 574 footprint samples and converts signal in 10μs
160 Computer-Aided Engineering
163 Instruments
165 Components
166 Power

175 INDEX OF ADVERTISERS

177 READER SERVICE CARD

Correction: In the Special Report "High-resolution ADCs up dynamic range in more applications," Apr. 11, p. 65, we neglected to mention that the Micro Networks MN6400 family of 16-bit ADCs also guarantees 16-bit differential and integral linearity, as well as no-missing-code operation, over its operating-temperature range. Ed.

COMING NEXT ISSUE
- Special Report: Meeting the standards of image-compression algorithms
- Technology Analysis: The technology of downsizing hard-disk drives
- Using undersampling techniques to simplify digital radio
- First details on a new image-processing IC
- A new gate-level simulation accelerator
- New design package for PLDs
- Designing with a new combination RAM and PLD
- PIPS Special Section: Power, Interconnections, Passives, Switches & Relays
  - Focus on Passive Components
  - Computing EIA-standard component values
  - Selecting the proper shielded connector
  - Controlling the taper of variable resistors
- PLUS:

Pease Porridge
Ideas for Design
Technology Advances

ELECTRONIC DESIGN (USPS 172-080; ISSN 0013-4872) is published semi monthly by Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $75 U.S., $140 Canada, $230 International. Second-class postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204.

Printed in U.S.A. Title registered in U.S. Patent Office. Copyright © 1991 by Penton Publishing Inc. All rights reserved. The contents of this publication may not be reproduced in whole or in part without the consent of the copyright owner.

Permission is granted to users registered with the Copyright Clearance Center Inc. (CCC) to photocopy any article, with the exception of those for which separate copyright ownership is indicated on the first page of the article, provided that a base fee of $1 per copy of the article plus $.50 per page is paid directly to the CCC, 27 Congress St., Salem, MA 01970 (Code No. 0013-4872/91 $1.00 + .50). Copying done for other than personal or internal reference use without the express permission of Penton Publishing, Inc. is prohibited. Requests for special permission or bulk orders should be addressed to the editor.

For subscriber change of address and subscription inquiries, call (216) 696-7000.

POSTMASTER: Please send change of address to ELECTRONIC DESIGN, Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543.

IN THE TIME IT TAKES COULD ROUTE THE WO

Believe it or not, it only takes about 150 seconds to place and route a Xilinx FPGA.

Chances are: it'll take you longer to read this ad.

THE FIRST AND STILL THE FASTEST.

At Xilinx we invented the FPGA. And we've led the industry ever since.

With the fastest, highest performance FPGAs available anywhere.

Today, we offer system clock speeds of 60 MHz.

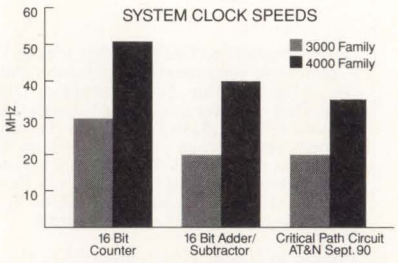
We're also the first programmable logic company to offer you on-board RAM.

Making our newest FPGAs ideal for everything from FIFOs to register stacks.

What's more, we're the only programmable logic company that provides you with on-chip wide decode.

And that's just the beginning.

Because as formidable as our hardware may seem, it's only half the story.



As measured by typical design benchmarks, the XC3000 family is the industry's fastest FPGA. Or at least it was until we introduced the 4000 family.

NEW ENHANCED SOFTWARE PROVIDES PUSH BUTTON SOLUTION.

Device speed alone doesn't determine the fastest, highest-performance logic device.

When you're designing, the clock on the wall is every bit as important as the clock speed of the chip.

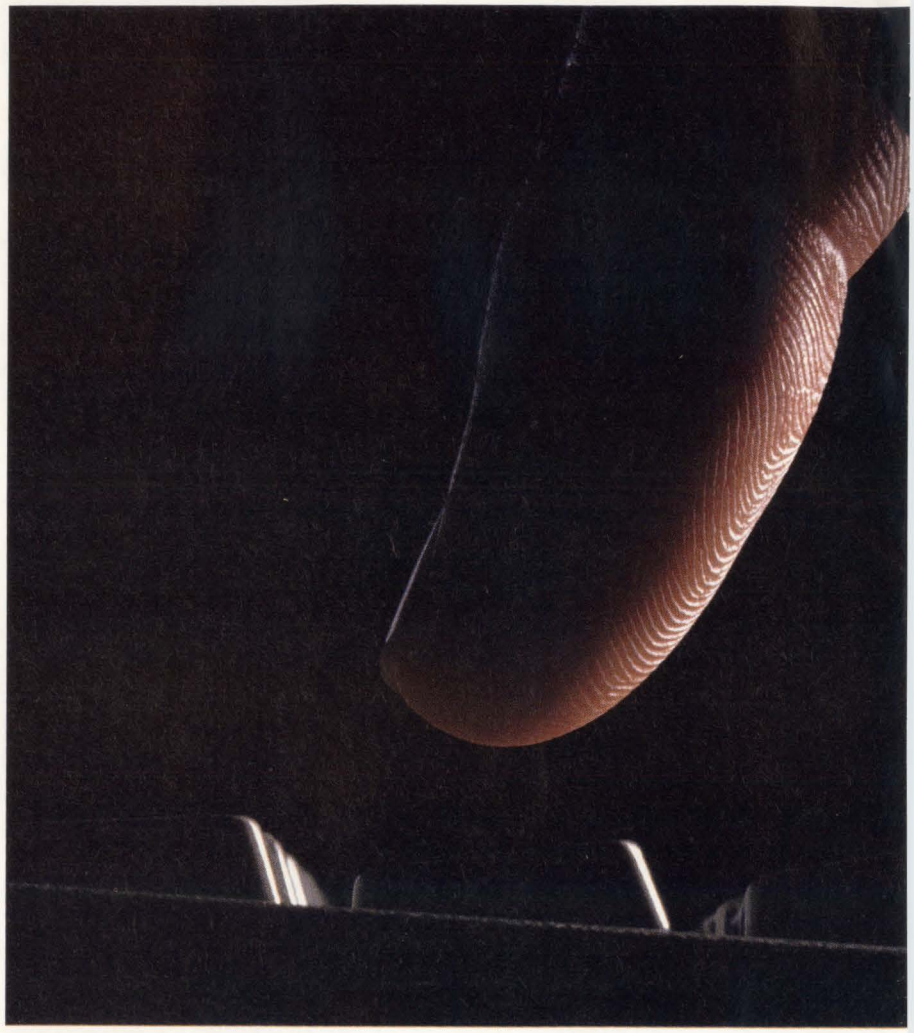
So to make Xilinx FPGAs even faster and easier to program, we've redesigned our software.

This is no mere upgrade. It's a major rewrite.

Our new version of XACT now comes with 200 soft macros. And fifty hard macros.

Providing automatic placing and routing for virtually all designs.

With greater than 90% gate utilization.



Our new push-button software makes programming other logic devices seem positively tedious.

If you've worked with Xilinx FPGAs before, you'll see improvements even before you start to place and route your design.

If you've never worked with Xilinx FPGAs before, you'll find every other logic device to be positively tedious by comparison.

WHEN IT COMES TO SYSTEM TESTING, WE PASS WITH FLYING COLORS.

Our newest FPGAs offer you yet another competitive advantage that's exclusive to Xilinx.

© 1991 Xilinx, Inc. 2100 Logic Drive, San Jose, CA 95124. Europe, 44 (932) 349401. Japan, 81 (3) 297-9191. Asia, 852 (3) 721-0900. Xilinx is a trademark and The

TO READ THIS AD, YOU RLD'S FASTEST FPGA.

The industry's first on-chip JTAG boundary scan for easy testing of PC boards and device I/Os.

This unique Xilinx offering improves overall system testability and dramatically reduces board test costs. It's a major boost for those designing high-density, surface mount systems or complex, multi-layer PC boards.

We told you we'd save you time and money.

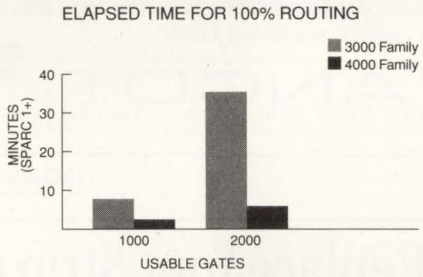
IF AT FIRST YOU DON'T SUCCEED, IT'S EASY TO TRY AGAIN.

As you well know, when you're designing a system, changes keep coming fast and furious.

Which is why Xilinx FPGAs are designed to be reprogrammed quickly an unlimited number of times.

And not only do our FPGAs save you an enormous amount of time early on, they also save you time later when you need to make those "last minute" enhancements.

It's one more way we make it easier for you to get your product to market as fast as possible. First time. Every time.



New algorithms have reduced place and route times by a factor of four.

GETTING AN EDGE OVER YOUR COMPETITORS IS JUST A PHONE CALL AWAY.

If you've read this far, you could have already placed and routed one of our FPGAs.

So don't delay. No other programmable logic company can offer you the many exclusive features of Xilinx FPGAs.

Call 1-800-255-7778. Or in California, 408-559-7778. And we'll send you more information on how our FPGAs can give you the competitive edge.

But you'd better hurry.

Some of your competitors have already finished reading this ad.

XILINX

The Programmable Gate Array Company.℠

Programmable Gate Array Company is a service mark of Xilinx, Inc. All other trademarks or registered trademarks are the property of their respective holders.

CIRCLE 141

SCSI INSTRUMENTS

ANCOT's SCSI instruments are powerful, easier to use, and cost less. Proven in use worldwide, Ancot's portable equipment travels from bench to field and back again without ever slowing down. They are time and labor saving instruments, for design, manufacturing, repairing, and inspection applications.

Call today for product data sheets, demo disc, or to make arrangements for a free evaluation unit in your facility.

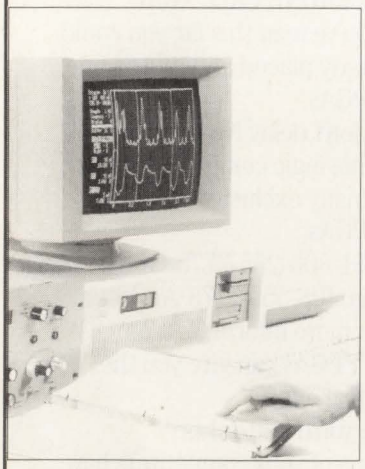
ANCOT CORPORATION

☎[415] 322-5322
fax: (415) 322-0455
115 Constitution Drive
Menlo Park, CA 94025

CIRCLE 85

Replace Your Strip Chart Recorder

With New PC-Based Chart Recorder
Low Cost - More Effective



- No paper purchase or storage cost
- **Transient or continuous recording**
- No mechanical moving parts - reliable
- Direct measurement of time, amplitude, area
- Higher frequency response - to 1 MHz
- Calibration and Engineering Unit conversion
- Higher resolution: >0.1% accuracy
- Markers during acquisition
- Portable or DC operation available
- **Anti-Aliasing Filter**
- Programmable Gain Amplifier
- No programming required
- Post-acquisition analysis of data (FFT, Digital Filters)

RC Electronics Inc.

6464 Hollister • Goleta, CA 93117
(805) 685-7770 • FAX: (805) 685-5853

CIRCLE 86

ELECTRONIC DESIGN

Editor-in-Chief: Stephen E. Scrupski

Executive Editor: Roger Allan

Managing Editor: Bob Milne

Senior Editors: Frank Goodenough, Milt Leonard, John Novellino

Technology Editors:
Analog & Power: Frank Goodenough
Communications & Industrial: Milt Leonard (San Jose)
Components & Packaging: David Maliniak
Computer-Aided Engineering: Lisa Maliniak
Computer Systems: Richard Nass
Semiconductors: Dave Bursky (San Jose)
Test & Measurement: John Novellino

News Editor: Sherrie Van Tyle

Field Bureaus:
West Coast Executive Editor: Dave Bursky (San Jose)
Boston: Lawrence Curran
Dallas: Jon Campbell
Frankfurt: John Gosch
London: Peter Fletcher

Chief Copy Editor: Roger Engelke, Jr.

Contributing Editors: Ron Kmetovicz, Robert A. Pease

Editorial Production Manager: Lisa Iarkowski

Editorial Support Supervisor: Mary James

Editorial Assistant: Ann Kunzweiler

Editorial Secretary: Bradie Guerrero

Editorial Offices: (201) 393-6262

Advertising Production: (201) 393-6093 or FAX (201) 393-0410

Production Manager: Michael McCabe
Production Assistants: Donna Marie Bright, Lucrezia Hlavaty, Eileen Slavinsky

Circulation Manager: Robert Clark

Promotion Manager: Clifford Meth

Reprints: Helen Ryan 1-800-835-7746

Group Art Director: Peter K. Jeziorski

Computer Systems Administrator: Anne Gilio Turtoro

Published by Penton Publishing
Vice President-Editorial: Perry Pascarella
Group Editorial Director: Leland Teschler

Publisher: Paul C. Mazzacano

You'll like the feeling of our new digital troubleshooting scope.

Now there's a 100 MHz digital scope that handles just like analog.

Digital oscilloscopes have certain advantages that are hard to overlook. But for troubleshooting, many engineers still prefer analog scopes. Simply because they like the way they handle.

The HP 54600 changes that. It *looks* like a 100 MHz analog scope. All primary functions are controlled directly with dedicated knobs. And it *feels* like one.

The display responds instantly to the slightest control change.

But when it comes to troubleshooting, the HP 54600's digital performance leaves analog and hybrid scopes in the dust. At millisecond sweep speeds, the display doesn't even flicker. Low-rep-rate signals are easy to see without a hood. It has all the advantages that only a true digital scope can provide. Like storage, high-accuracy, pretrigger viewing, hard copy output, and programming. And since it's one of HP's basic instruments, the HP 54600 gives you all this performance at a very affordable price. Only $2,395* for a 2-channel scope; $2,895* for the 4-channel version.

So, if you need the power of a digital scope, but like the feel of analog, call **1-800-752-0900.** Ask for **Ext. 2282,**† and find out how well the HP 54600 handles your troubleshooting needs.

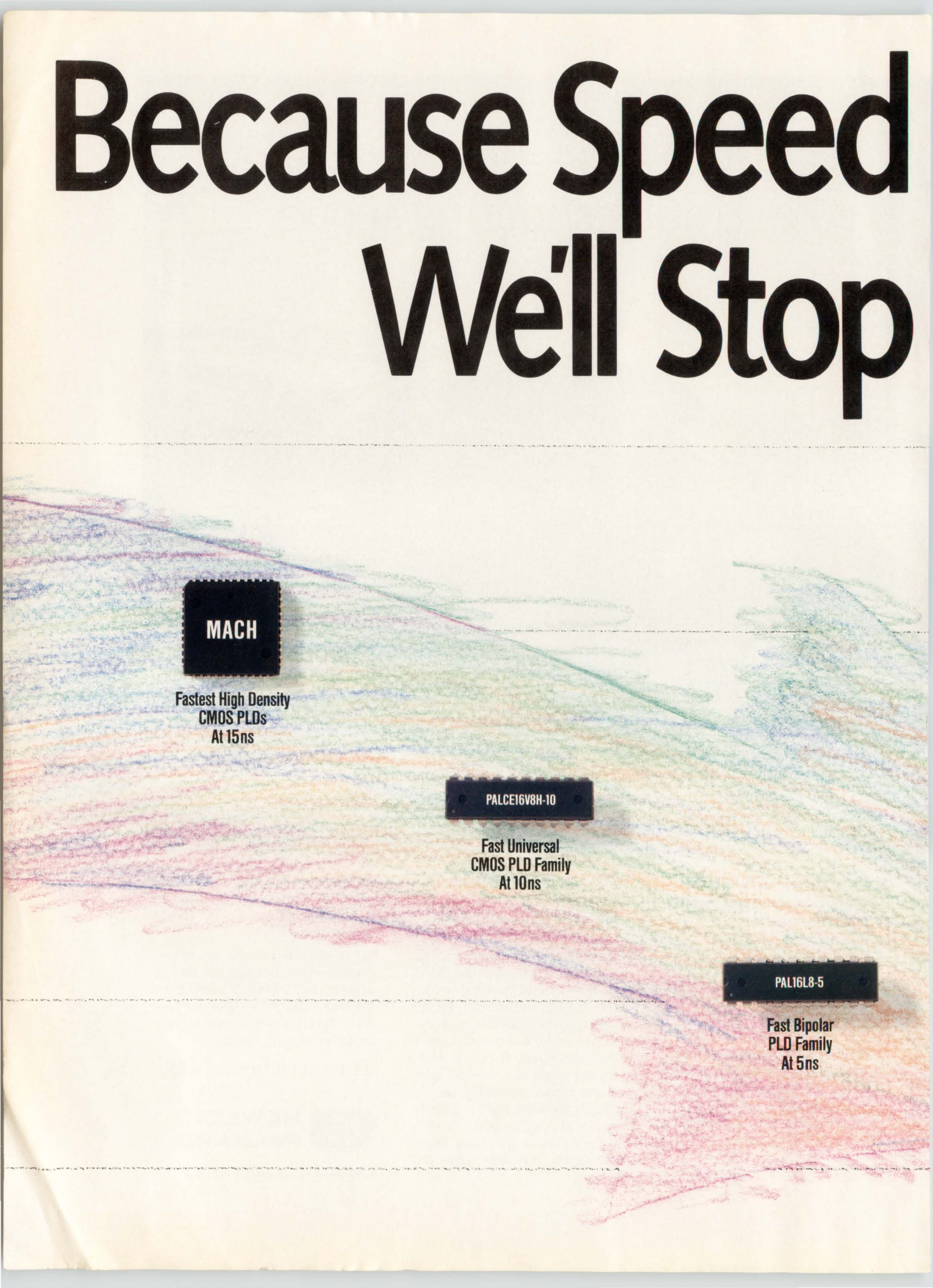
There is a better way.

HEWLETT PACKARD

* U.S. Prices only.
† In Canada, call 1-800-387-3867, Dept. 428.

©1991 Hewlett-Packard Co. TMCOL107A/ED

Because Speed We'll Stop



Is Everything. At Nothing.

Whatever kind of PLD you need, the fastest comes from AMD.

We'd love it if all our work amounted to "zero." As in zero delay. And we're not far off.

Not surprising—because AMD invented the PAL® device. That's why we know programmables better. And offer you the most choices of the best devices.

Say you want speed, but can't sacrifice density. Don't. Use our new MACH™ products (Macro Array CMOS High-density) that give you up to 3600 gates and 15ns performance. They're two to three times faster than the competition and cost 40% less.

For more speed, along with low power consumption, try our new 10- and 15-nanosecond CMOS PLDs. Use our 16V8-10s and 20V8-10s anywhere you'd use a GAL® device. Or choose the ever-popular AMD-invented 22V10, at 15ns.

Faster still are our seventh generation bipolar PAL devices. Complete families of 16L8-5s, 20L8-5s, and the 22V10-10s. And for real speed freaks, we're now shipping a 4.5ns bipolar PAL device—the world's fastest TTL programmable logic.

Along with all this speed, we're providing equally fast delivery. In quantity. In fact, we deliver more programmable logic devices than all our competitors combined.

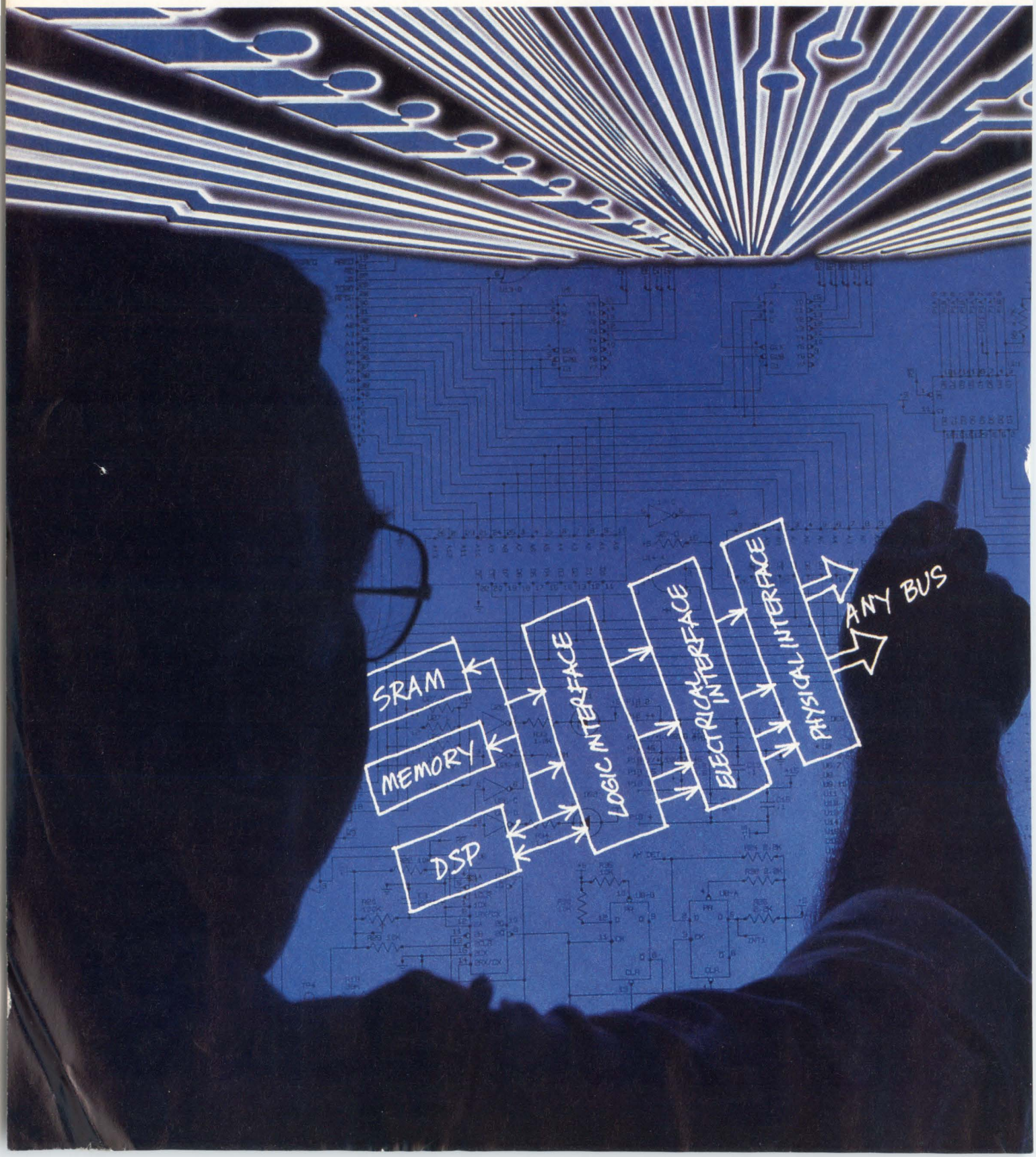
For details, call AMD now at **1-800-222-9323.** And let nothing stand between you and your need for speed.

Advanced Micro Devices

901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088 © 1991 Advanced Micro Devices, Inc.
MACH is a trademark and PAL is a registered trademark of Advanced Micro Devices.
GAL is a registered trademark of Lattice Semiconductor.

CIRCLE 149

Bringing high performance FPGAs



to a higher quality.

That's AT&T "Customer*izing*."

The ATT3000 Series FPGAs deliver 125 MHz toggle rates. Provide 2000 to 9000-gate densities. Support you with a high volume manufacturing capability. World class submicron wafer fabrication and packaging facilities that assure volume delivery of high performance products for telecomm, datacomm, workstation and graphics applications. The same wafer fabrication area that makes our standard cells an industry leader. That's what we mean by "Customer*izing*." To speed your design in, the XACT* design implementation system includes 3rd party interface, schematic capture and simulation software. And, while all AT&T FPGAs utilize low-power CMOS technology and are 100% factory pre-tested, our ATT3000 Series devices also offer selectable configuration modes and are pin-for-pin compatible with the XILINX* XC3000 family. For more information on how the ATT3000 Series can extend your system's performance, meet your most demanding specifications and achieve your cost objectives, call AT&T Microelectronics at **1 800 372-2447, Ext. 634.** In Canada, call **1 800 553-2448, Ext. 634.**

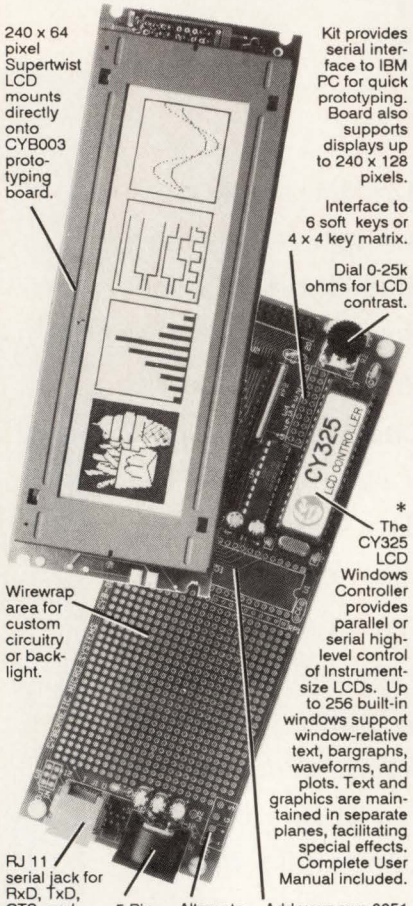
*Registered trademarks of Xilinx, Inc. © 1991 AT&T.

AT&T
Microelectronics

CIRCLE 113

LCD Proto Kit

Everything you need to start your LCD application .... create complex screens in just a few hours!



Kit also includes:

$495 - Kit
Popular LCD Starter Kit.

MC VISA AMEX

($595 pre-assembled & tested)

*The CY325 40-pin CMOS LCD Controller IC is available from stock @ $75/singles, $20/1000s (Surface mount also avail in qty.)

CyberneticMicroSystems

Box 3000 • San Gregorio CA 94074
Tel: 415-726-3000 • Fax: 415-726-3003

CIRCLE 107

REMINISCING ABOUT A NEW COMPUTER

Recently, the thought struck me as to why, about 20 years ago when radios became so inexpensive, some stations didn't offer free fixed-tuned radios to select listeners. The result would have been a captive, high-quality audience. The marketing concept is somewhat akin to giving away a razor, but selling the razor blades. Because such radios would be tuned to only one station, they would not need a variable tuning capacitor, reducing their cost even further. The radio broadcasters, after all, made their money on commercials—the software—while the hardware was only the vehicle necessary to complete the transaction.

I was reminded of these thoughts by Hewlett-Packard's introduction of its $699 Model 95LX pocket computer, which includes a built-in copy of Lotus 1-2-3. I recently bought a copy of Lotus 1-2-3 for somewhere around $300, but there's still the tiresome task of shifting out of my word-processing program and into Lotus 1-2-3 whenever I want to do some budget work rather than editorial work. Now, for not a heck of a lot more, I could have a dedicated piece of hardware to run that program anytime or anywhere (the computer weighs 11 oz. and measures 6.3 x 3.4 x 1 in.) I would want to do so.

The fact that I (taking the role of a typical computer user) would even consider buying a computer to run a single software program shows how far the computer industry has come since the original IBM PC was launched about a decade ago. The HP computer will do other things besides run the Lotus program—it has a calculator function, phone and address storage, and handles text—but the point is that even if it did not, it would still be an interesting, single-function package.

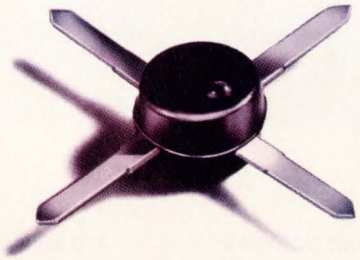
This is by no means a pitch for HP or its new computer. Only the market can, and will, decide whether this is the right product at the right time in the highly competitive pocket-computer market. But it does highlight some basic, ongoing trends in the electronics industry.

For one, it demonstrates software's relatively constant value while hardware costs continue to decline (nevertheless recognizing the obvious necessity of having the hardware to run the software). Looked at another way, it also demonstrates the importance of identifying a customer need before committing to the design and manufacture of a product. And finally, it demonstrates how smart design teams can better exploit the flexibility of VLSI to tailor hardware to solve those specific user problems.

Stephen E. Scrupski

Editor-in-Chief

99¢ from



dc to 2000 MHz amplifier series

SPECIFICATIONS

MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	•MAX. PWR. dBm	NF dB	PRICE Ea.	$ Qty.
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

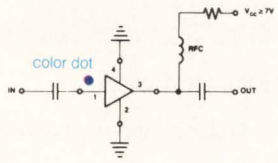
NOTE: Minimum gain at highest frequency point and over full temperature range.
• 1dB Gain Compression
□ +4dBm 1 to 2 GHz

Unbelievable, until now…tiny monolithic wide-band amplifiers for as low as 99 cents. These rugged 0.085 in.diam.,plastic-packaged units are 50ohm* input/output impedance, unconditionally stable regardless of load*, and easily cascadable. Models in the MAR-series offer up to 33 dB gain, 0 to +11dBm output, noise figure as low as 2.8dB, and up to DC-2000MHz bandwidth.

*MAR-8, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1

designers amplifier kit, DAK-2

5 of each model, total 35 amplifiers only $59.95



Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each.†

Size (mils)	Tolerance	Temperature Characteristic	Value
80 × 50	5%	NPO	10, 22, 47, 68, 100, 220, 470, 680, 1000 pf
80 × 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 × 60	10%	X7R	.022, .047, .068, .1μf

† Minimum Order 50 per Value

☐ Designers kit, KCAP-1, 50 pieces of each capacitor value, only $99.95

finding new ways...
setting higher standards

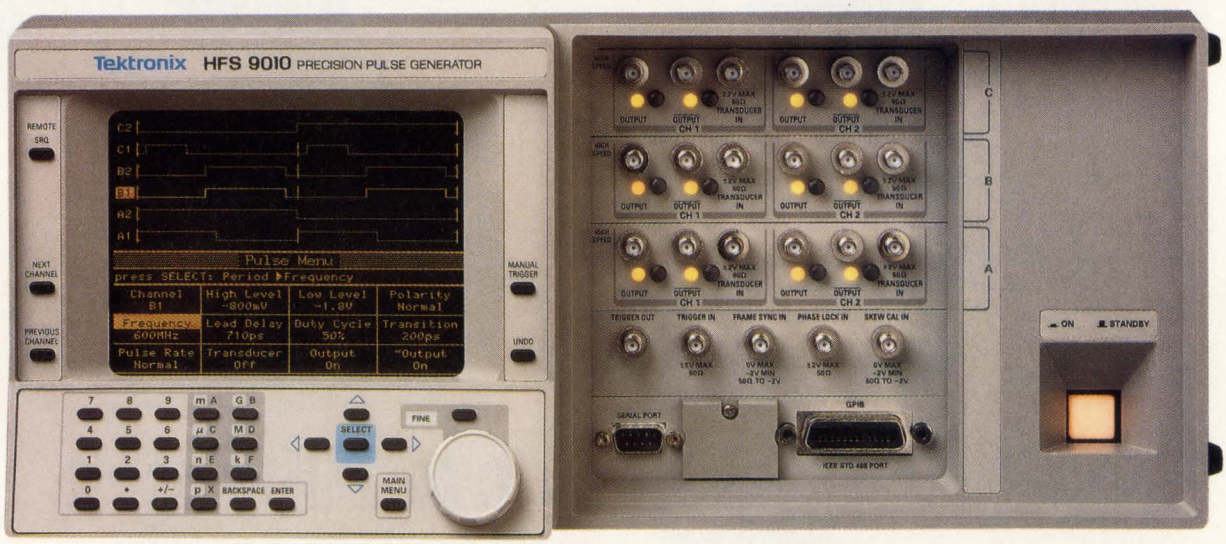
Mini-Circuits

A Division of Scientific Components Corporation
P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500
Fax (718) 332-4661 Domestic and International Telexes: 6852844 or 620156

CIRCLE 173

C113-Rev. D

Making



You're looking at the biggest news in signal sources in years: two new families of pulse generators from Tektronix.

You can already see one reason why Tek's new pulse generators are stirring up so much interest: their what-you-see-is-what-you-get user interface vastly simplifies your life.

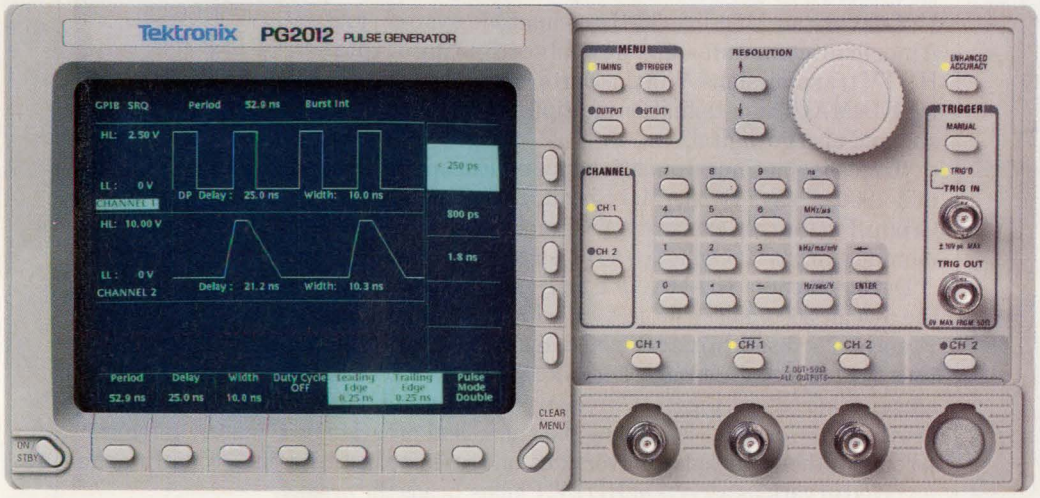
Now you can stop piecing the big picture together from one-line LEDs, blinking error lights and trial-and-error iteration. Tek's new scope-like display lets you set up and modify a whole set of parameters at once, with a true representation of your pulses and instant, visual feedback.

You name your application and logic technology: Tek has a signal source to match. For the first time, you can choose channel capacities from one to *six* channels, or rep rates from 50 MHz to a remarkable 600 MHz. Choose tools designed for logic, fast logic, or *mixed* technologies. Vary transition times from 200 ps to 10 ms. Test complex timing relationships with ease.

Add to all this our popular pulse generator plug-ins from Tek TM500/

Copyright © 1991, Tektronix, Inc. All rights reserved. 85A186-135

Waves.



5000 modular instrumentation, and you can see why we're making waves!

Easier to use, more precise and more expandable, Tek's new pulse generators are doing for signal sources what DSOs have done for measurements.

Contact your Tek sales office for a demonstration, or call for more information.

1-800-426-2200

One company measures up.

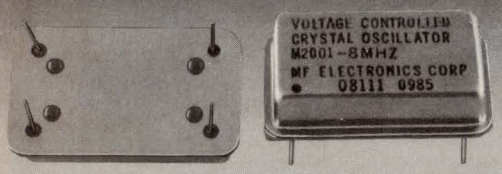
Tektronix®
COMMITTED TO EXCELLENCE

CIRCLE 139

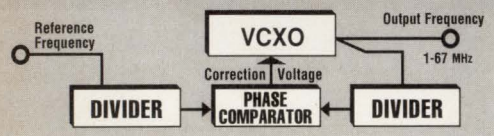
MF ELECTRONICS CORP.

VCXO's and PHASE-LOCKED-LOOP-VCXO

VCXO's Series M2000
1MHz to 67 Mhz



These VCXO's are used to replace a distorted incoming reference signal (e.g. 1.544 MHz, T1), with a stable crystal-controlled signal of the same or any multiple frequency, from 1 to 67 MHz.

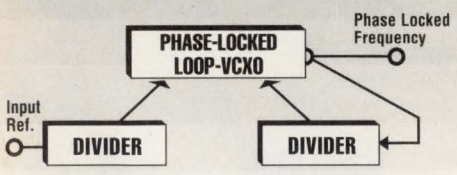


With MF VCXO's, since the specification is computer-tested over the full operating temperatures, you can be assured that the specified frequency- deviation is what you get for capture range.

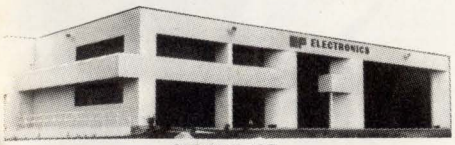
	Control Voltage	Deviation
M2001	0.3 to 10V	±175 ppm
M2002	0.3 to 4V	± 75 ppm
M2003	0.3 to 10V	±175-300 ppm
M2004	0.3 to 4V	±125 ppm
M2005	1.0 to 4V	± 75-300 ppm
M2006	0 to 5V	±150 ppm
M2007	0.5 to 4.5V	±125-250 ppm

PHASE-LOCKED LOOP-VCXO'S
Series M2010, M2015

This is the complete loop, including the phase-comparator and the VCXO, in just one package. Add the dividers to match the frequencies. Oscillators from 10 to 30MHz.



	Frequency Range
M2010	±125 ppm
M2015	±150 ppm

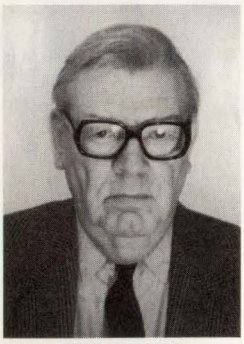


CIRCLE 137

Headquarters and manufacturing plant: 36,000 sq. feet

MF ELECTRONICS CORP.
10 Commerce Drive
New Rochelle, NY 10801
914-576-6570 Fax: 914-576-6204

EUROPE IS GETTING READY FOR HDTV



JOHN GOSCH
FIELD EDITOR

Regular high-definition TV picture transmissions in Europe are probably still several years off, but the television industry—TV set makers, studio-equipment manufacturers, broadcasters, and program producers—is getting set for the new TV era that begins in 1995.

By now, the Europeans have buried all hopes for a global HDTV standard. The Japanese, who were the first to demonstrate the new medium to a broad audience during the 1988 Olympics in Seoul, have their MUSE (multiple sub-Nyquist encoding) standard, an 1125-line/60-Hz system that's incompatible with existing TV sets. The U.S. favors an 1150-line/60-Hz-compatible system, and American companies are now investigating digital HDTV transmissions. Will the Europeans, who have opted for the 1250-line/50-Hz HD-MAC (high-definition multiplexed analog components) standard, follow suit and also go digital?

"Unless something dramatic happens, Europe won't see digital HDTV by the mid-1990s," says Sönke Mehrgardt, technical director, ITT Semiconductors Group, Freiburg, Germany. "Work on the HD-MAC standard has gathered such momentum that it cannot be stopped to pursue another approach."

Development of HD-MAC is a truly pan-European effort. Major participants in the 6-year, $600-million project, called Eureka 95, are Philips of the Netherlands, France's Thomson, Nokia of Finland, and Broadcast Television Systems, a joint venture of Philips and Germany's Robert Bosch. The first three firms are designing, among other things, the HDTV receivers with the new 16:9 picture format. BTS, of Darmstadt, Germany, is building the studio and program production equipment. About 35 other companies, universities, and research institutes in 10 countries, are involved in various aspects of HDTV. Philips heads the project.

Eureka 95 is now well into its second phase, which will last until the end of 1992. After that, the industry will gear up for volume production of HDTV equipment—receivers, video-disk players, professional cameras, video-tape recorders, mixers, and the like—conforming to the 1250-line/50-Hz European standard. By 1995, the HDTV infrastructure will be in place and the 16:9 sets will be ready for consumers to buy. Significantly, the HD-MAC system is compatible with present TV technology. This means that today's receivers can still be used. But, of course, there won't be the high-definition pictures of HDTV.

Meanwhile, trial HDTV broadcasts have been held in several countries using HD-MAC signals sent over a direct satellite-transmission path. The industry is preparing for large-scale trials next year. These will be held during the 1992 Winter Olympics in Albertville, France; the Summer Olympics in Barcelona, Spain; and the World Exhibition in Seville, Spain. Viewers will see, on pre-production HDTV receivers installed at public demonstration centers throughout Europe, from 8 to 10 hours of sports and cultural programs a day.

Pointing to Europe's progress in HDTV since 1986, when the first tentative engineering research proposals were made, Peter Bögels, a Philips executive and president of the Eureka 95 directorate, says "although we haven't yet delivered as much HDTV equipment to studios as the Japanese have, we're on an equal footing as far as system quality is concerned, and even ahead when it comes to transmission quality."

Europe's HDTV project is advancing not only TV-receiver and studio-equipment design, it's also pushing chip technology. At ITT Semiconductors, which is designing half of the HDTV receiver's signal-processing circuitry, engineers have come up with an HD-MAC decoder that integrates more than 200,000 transistors. This already accounts for half of the company's share. The firm is now delivering the decoder chips as samples to Philips, Thomson, and Nokia for application in the pre-production HDTV receivers they're building.

Innovative but unreliable software solutions can play havoc with how you spend your time.

© 1991, AT&T. All Rights Reserved.

The sundial was innovative in its day, but since the sun didn't always shine, not very dependable.

Software that's less reliable than it should be isn't much better for your business than a sundial would be to tell time. Because software that causes delay and confusion wastes time, effort, money and energy.

GENTEST™ *software is a fully automatic test generator/fault simulator. It provides high fault-coverage for sequential logic in full, partial, and non-scan circuits. It also handles IDDQ techniques.*

TAPDANCE™ *software checks circuit designs for conformance to the IEEE Standard Test Access Port and Boundary-Scan Architecture 1149.1*

That's why every piece of software we offer has been thoroughly tested and used internally by AT&T before it's marketed. And to make sure it's right for businesses of all types and sizes, it's priced competitively as well.

To learn more about what we offer and how it can help your business, call 1 800 462-8146 and ask for "The AT&T Software Licensing Catalog." It's free. Or FAX: 1 908 580-6355. If you prefer, you can write: AT&T Software Licensing Manager, 10 Independence Blvd., Room 3A36, Warren, NJ 07059.

THE INTELLECTUAL PROPERTY DIVISION

Innovation you can depend on.

AT&T

CIRCLE 109

FILTERS

F132-1 REV. ORIG.

dc to 3GHz from $11.45

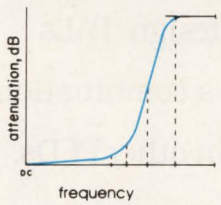
lowpass, highpass, bandpass, narrowband IF

- less than 1dB insertion loss • greater than 40dB stopband rejection
- 5-section, 30dB/octave rolloff • VSWR less than 1.7 (typ) • meets MIL-STD-202 tests
- rugged hermetically-sealed pin models • BNC, Type N; SMA available
- surface-mount • over 100 off-the-shelf models • immediate delivery

low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	(loss>40dB) Max.	(loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

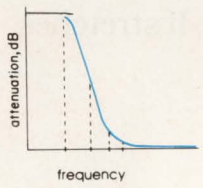
LOW PASS



high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	(loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

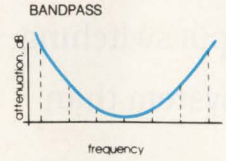
HIGH PASS



bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	PASS BAND, MHz (loss <1dB) Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	(loss > 10 dB) Max. F4	(loss > 20 dB) Min. F5	(loss > 20 dB) Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

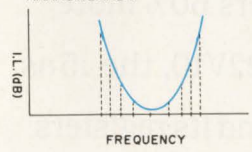
BANDPASS



narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

NARROWBAND IF



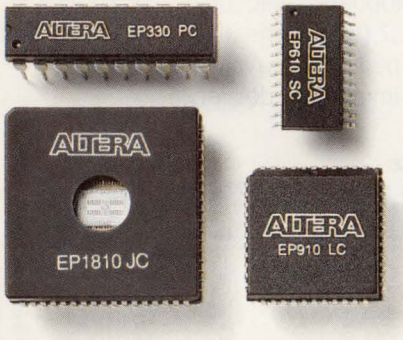
Mini-Circuits

P.O. BOX 350166, Brooklyn, New York 11235-0003 (718) 934-4500 FAX (718) 332-4661 TELEX 6852844 or 620156 **WE ACCEPT AMERICAN EXPRESS**

F132-2 REV. ORIG.

CIRCLE 163

OUR CLASSIC™ EPLDs CUT M



They also cut your product costs, with prices low enough to impact your bottom line.

As for logic delays, we've cut them down to a remarkably low 12ns.

So now you can cut something from your design: PAL®s and GAL®s. Because our Classic parts give you a combination of speed, density and flexibility you won't find in other PLDs.

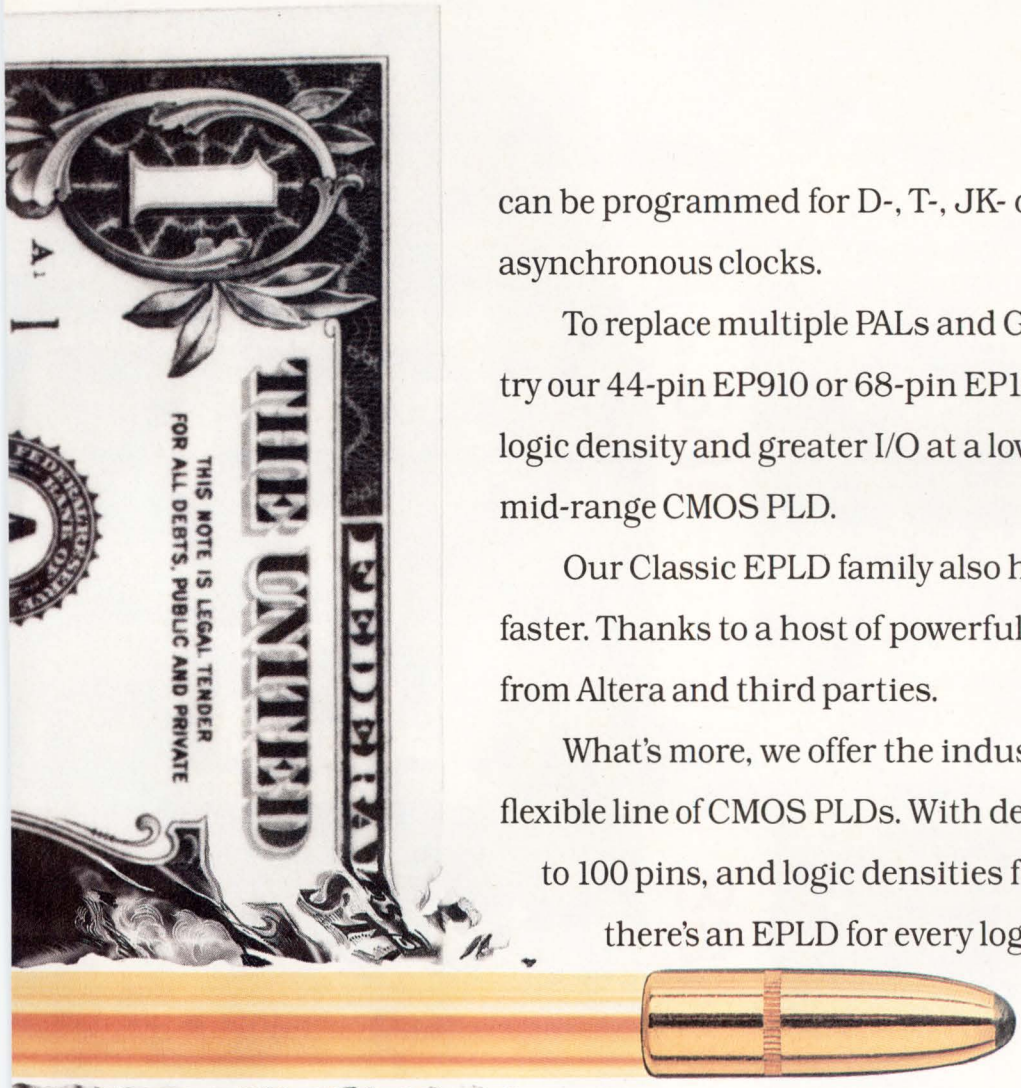
All of which helps you cut the time it takes to produce a superior design.

For example, our 20-pin, 8-macrocell EP330 is the perfect replacement for over 20 types of PALs and GALs. It stretches

counter frequencies to 125 MHz while sipping one-fourth the power of a standard PAL. And its quiet output switching circuitry allows the EP330 to run faster in-system than a 10ns 16V8.

Our 24-pin, 16-macrocell EP610 delivers 60% more logic density than a 22V10. And unlike a 22V10, the 15ns EP610 consumes a mere 20μA in standby. And its registers

MORE THAN LOGIC DELAYS.



can be programmed for D-, T-, JK- or SR-operation or for asynchronous clocks.

To replace multiple PALs and GALs with a single chip, try our 44-pin EP910 or 68-pin EP1810. Both offer superior logic density and greater I/O at a lower cost than any other mid-range CMOS PLD.

Our Classic EPLD family also helps you get to market faster. Thanks to a host of powerful logic development tools from Altera and third parties.

What's more, we offer the industry's broadest, most flexible line of CMOS PLDs. With devices ranging from 20 to 100 pins, and logic densities from 8 to 192 macrocells, there's an EPLD for every logic design task.

So call Altera today at (408) 984-2800 for more information. And discover programmable logic that's a cut above the rest.

ALTERA

2610 Orchard Pkwy., San Jose, CA 95134-2020 (408) 984-2800/Fax: (408) 248-6924

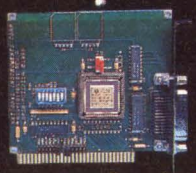
Classic is a trademark of Altera Corporation. Other brands or products are trademarks of their respective holders. © 1991, Altera Corporation.

CIRCLE 151

Ask about our 488.2 Upgrade Program

NAT4882 *The Only* Way to Reach Full 488.2 Compatibility

PC/XT/AT



CIRCLE 119

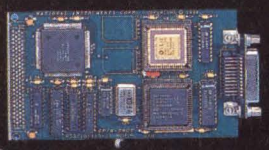
- Industry Standard
- 7210/9914 Compatible

PC AT

CIRCLE 120

- The New Industry Standard
- 16-bit speed

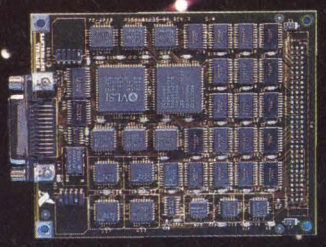
Sun SPARCstation SBus



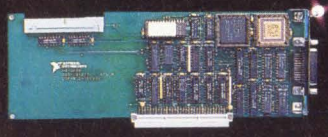
CIRCLE 121

DECstation TURBOchannel

CIRCLE 122



Macintosh NuBus



CIRCLE 123

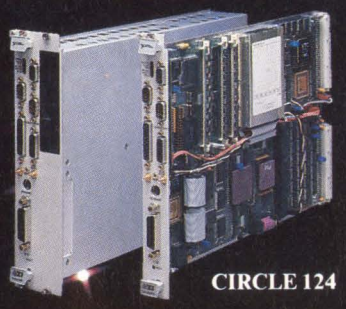
IEEE-488.2

Turbo488

1 Mbyte/sec READS

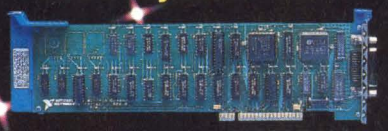
1 Mbyte/sec WRITES

VXI Embedded Controllers



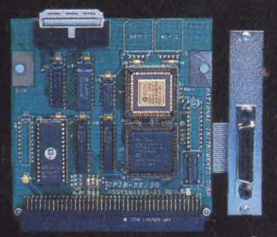
CIRCLE 124

IBM PS/2 and RISC System/6000



CIRCLE 125

Macintosh SE/30



CIRCLE 126

Continuing Unchallenged Leadership

NATIONAL INSTRUMENTS®

The Software is the Instrument®

Call for a *FREE* Catalog

(512) 794-0100

(800) IEEE-488 (U.S. and Canada)

6504 Bridge Point Parkway
Austin, TX 78730

SOFTWARE MANAGES VHDL SOURCE-CODE CREATION

A complete design environment that creates and manages source code in a VHDL-based design methodology promises to simplify the designer's job. The VHDL Design Assistant, from Ascent Technology Inc., San Jose, Calif., consists of three programs that provide design management, a VHDL specific source editor, and a source browser. The browser views a VHDL design as a data base and permits various inquiries that assist designers in understanding and maintaining VHDL designs on a logical level. The software employs built-in knowledge of the language standard to ease text and graphics creation, as well as assisting the analysis, maintenance, and documentation tasks in a typical product. The Source Manager portion of the software manages a design on a larger file and library basis. It supports the notion of design sets, a concept that precisely captures all sources required for a particular design. The Source Editor offers a mixed-structure/text-editing mode to create and modify the VHDL sources. The first release of the software is slated for late this quarter. Other software modules that will be released later include a state-machine editor, a Petri-net editor, and a VHDL architecture editor. *DB*

LIGHT BEAM ACCELERATES PATTERN RECOGNITION

A system that compares up to 1000 stored images with a video scene in just 1 second promises better robotic vision, improved security, and more-accurate weapon systems. Initially developed for missile-guidance systems, the acousto-optic image correlator compares images and determines whether or not a designated pattern or target is within all of the images. When a match occurs, it provides a simple dot representation of the match on a CRT. Researchers at Sandia National Laboratories, Albuquerque, N.M., have developed a functioning model of this hybrid optical processor prototype that stores up to 256 digitized patterns (templates)—representations of different objects or the same object in different rotations and sizes. To perform the comparison, the processor performs millions of multiplications in parallel to determine the closest match. Employing optics for the correlator improves the speed because of the inherent parallelism of optics and the high information capacity of light. Furthermore, the optics enable the system to be very compact while consuming only about 100 W—about 1/10 the power of an all-electronic system that might come close in throughput, but would fill an entire room with equipment. Images are captured with a video camera and compared by scanning them into the correlator using an acousto-optic device. Templates are stored in memory and introduced into the processor by a laser-diode array. The image propagates along the length of the accousto-optic device, and during propagation is compared with the reference template. The signal is then re-imaged onto a charge-coupled device sensor array and displayed on a monitor. A white dot indicates the presence and location of a match. Contact K. Terry Stalker, (505) 844-8143. *DB*

SUPERCOMPUTER SETS NEW SPEED RECORD

Scientists running the Linpack benchmark routine on the massively parallel Connection Machine-2 (CM-2) from Thinking Machines Corp., Cambridge, Mass., have achieved computing speeds of 5200 MFLOPS. The benchmark is the standard by which supercomputing speed has been measured since the early 1980s. Thinking Machines claims this establishes a new speed record for conventional supercomputers. The CM-2 utilizes 64,000 processors. The scientists say that later this year the same results will come from a Fortran 90 program. *RN*

RECEIVER TAKES GPS NAVIGATION IN HAND

A palm-size Global Positioning System receiver, relying on gallium arsenide chips and application-specific ICs, could find its way into consumer electronic products by the end of the year. Rockwell Communications Systems' 2.6-by-4.0-in. NavCor V module has five channels, enabling it to take a reading accurate to within 25 m in about 30 seconds. That compares with the two minutes it takes a typical two-channel receiver, says the Dallas company, a division of Rockwell International. Aimed at OEMs, the module consists of four custom ICs and four memory chips. By adding an antenna, LED readout, application processor, and more memory to the module, engineers can develop a compact auto, truck, or marine navigation system. The NavCore V receiver could also be used in a handheld navigation device for cyclists and hikers. The module's front end is a gallium arsenide receiver RF/IF that packs 1291 components into a 1/8-in.^{2} space. Rockwell's DSP chip has 250,000 tran-

We aced readir
Now test us

Mixed-Signal IC Solutions

It's no secret that we've become the channel experts in the disk drive IC market. But we're much more than that.

We offer the industry's most highly integrated and comprehensive family of custom and standard mixed-signal ICs. Not only for read/write functions, but also for pulse detection, data recovery, head positioning, motor speed control and programmable filters. Not to mention a wide range of bus interface ICs.

Our Mixed-Signal Integrated Circuits —MSICs™— have been successful in boosting disk drive performance while greatly reducing space, power and cost demands.

Test our broad portfolio of processing capabilities and you'll see how closely we'll match our technology to your

ıg and writing. on the rest.

specific needs.

Inside our world-class wafer fabrication facilities we meet high-volume product demands. We deliver on time. And with industry-leading reliability.

Believe it. Reading and writing are only chapter one of our story. Whatever your disk drive needs, we can pass the test. Just ask your nearest Silicon Systems representative. Or call us for literature package SPD-7.

CIRCLE 114 for Product Info
CIRCLE 115 for Career Info

Silicon Systems, Inc.,
14351 Myford Road, Tustin, CA 92680
Ph 1-800-624-8999, ext.151 Fax (714) 669-8814
European Hdq. U.K. Ph (44) 79881-2331 Fax (44) 79881-2117

Silicon Systems®
A TDK Group Company

sistors. The receiver, which sells for $450 in small quantities, is scheduled for delivery in the fourth quarter. Sales of the module, which was developed from a military GPS product, could reach $1 billion in four years, the company says. *SVT*

UNITRODE, MOTOROLA JOIN FOR WAFER BONDING

When direct-wafer bonding was first described at an IEDM conference about five years ago, it sounded so easy: Hold the oxide surfaces of two wafers together with light pressure at 700°C in an oxygen atmosphere. With this technique, you could build low-cost silicon-on-insulator (SOI) starting material that's ideal for high-voltage ICs. Bond the silicon surfaces and costly, thick epitaxial layers need not be grown for high-voltage discrete parts. However, only Toshiba and Unitrode presently offer devices built from bonded wafers. Now Unitrode Corp., Billerica, Mass., and Motorola, Phoenix, Ariz., have joined forces in a technology partnership to develop a proprietary technique to manufacture direct-bonded wafers. Their goal is to develop a facility that can supply both companies with these wafers for further processing. Additional applications for the technology include VLSI circuits, power and high-voltage ICs, fast analog ICs, and a variety of analog and mixed-signal ICs and sensors. The technology not only raises device performance, but also increases design flexibility, speed, and packing density (particularly for bipolar devices). *FG*

LAMINATE MATERIAL IS ENVIRONMENTALLY CLEAN

A new paper phenolic copper-clad laminate for use in pc-board fabrication offers a number of advantages over materials now available for pc-board manufacture. Developed at the Industrial Laminates Group of the Philips Plastics and Metalware Factories Div. in the Netherlands, the LC470 laminate is friendly to the environment because it's free from antimony (Sb), chlorine (Cl), and bromine (Br). This contrasts with the material FR2 that contains such chemicals, which companies around the world have been marketing for more than 20 years. The absence of Sb, Cl, and Br in LC470 leads to a drastic reduction of harmful pollution when waste material is disposed of or burned. Pressure against pollution is growing, and in some European countries, environmental activists are clamoring for manufacturers of end-user equipment—for example, TV sets—to take back the equipment at the end of its life-cycle for disposal. An additional feature of LC470 is that, when heated, it doesn't give off the irritating smell of present laminates. What's more, the new Philips laminate can be cold-punched, which means that manufacturers of pc boards need not worry about expansion and shrinkage of the material when punching. The Dutch company expects approval by Underwriters Laboratories (UL) in the U.S. by the end of May. *JG*

28-PIN PGA PACKAGE CONTAINS MIL MEMORIES

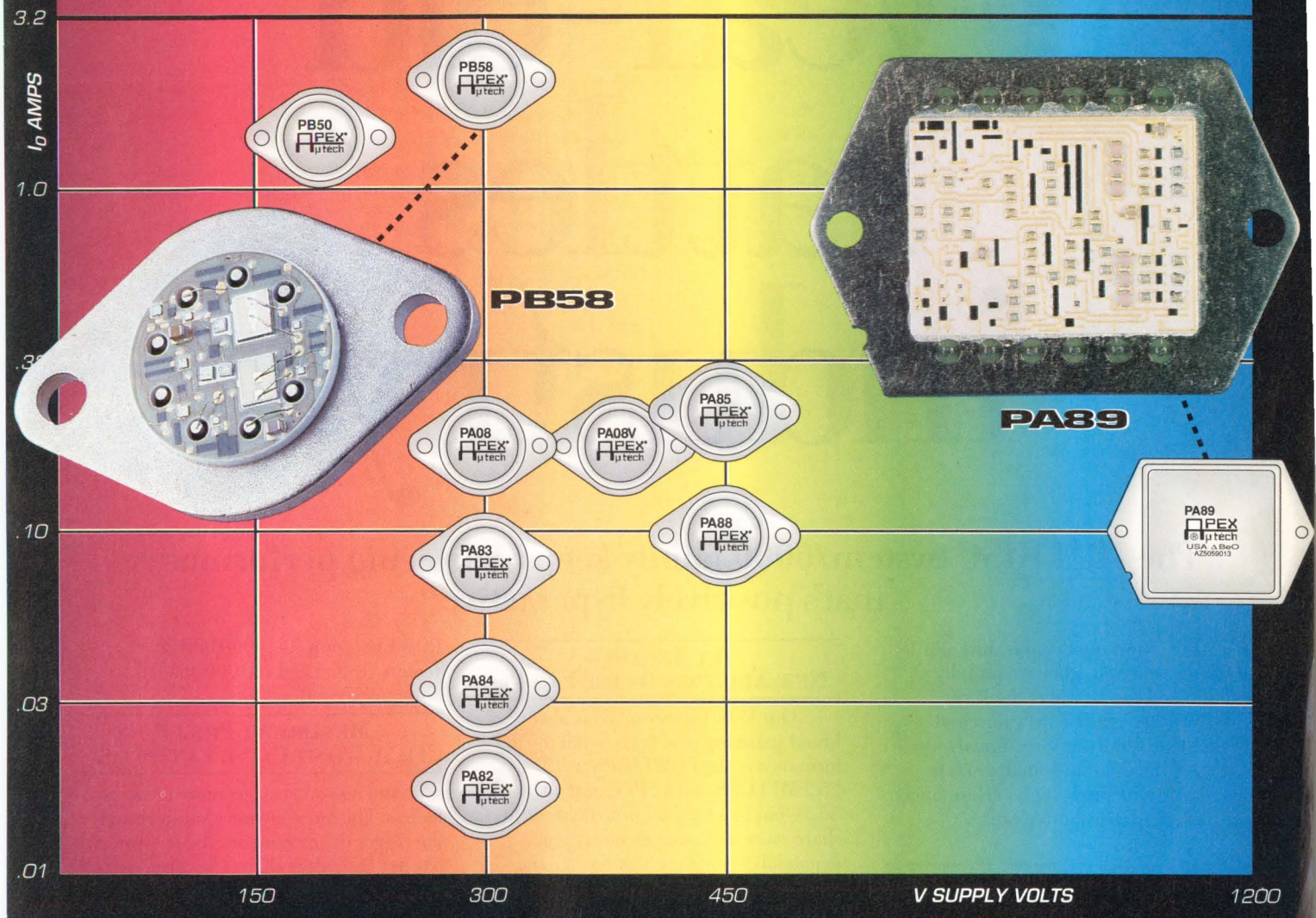
A low-profile, 28-pin grid-array package has been developed for avionics and military EEPROMs ranging in density from 16 to 256 kbits. The package, built by Seeq Technology Inc., San Jose, Calif., has been qualified to MIL-STD-883C Rev C requirements, and its outline has been submitted to JEDEC for standardization. Its dimensions are 0.550 by 0.650 in.; height from the pc board is typically 0.141 in. including standoff. The hermetically sealed PGA uses a solder-sealed gold lid for high-vibration and high-shock environments. Call Rich Norris at (408) 432-7400, ext. 5040. *DM*

MIXED-SIGNAL ASICS GET 0.7-μM 2-POLY CMOS

By moving from a single- to a double-polysilicon CMOS process for its 0.7-μm mixed-signal standard-cell library, NCR, Fort Collins, Colo., more than doubled the performance of its analog cells over those built on its single-polysilicon 1.5-μm process. This double-polysilicon submicron analog process exhibits lower capacitive parasitics, which in turn permits greater operational efficiency in the analog portion of a mixed-signal IC. As a result, future cells in the library can include 5-MHz bandwidth rail-to-rail op amps; 2-μs settling time, rail-to-rail, voltage-output 8-bit DACs; and 5-μs 8-bit successive-approximation ADCs. NCR's process requires only one mask step more than its single-polysilicon process, yet it can build 80-MHz video DACs and 125-MHz clock synthesizers. Essentially, the process achieves mixed-signal performance levels associated with bipolar and biCMOS processes, but at significantly lower cost. All new analog cells will be added to NCR's kit-part program, which permits customer breadboarding with DIP packages. The cells will be added to its CAE/CAD-tool library as well. For additional information, call 1-(800) 334-5454. *FG*

FOR THE FULL SPECTRUM OF

HIGH VOLTAGE AMPLIFIERS



...TURN TO APEX MICROTECHNOLOGY

QUALITY BY DESIGN

▲ FOR APPLICATIONS ASSISTANCE CALL 1-800-421-1865

▲ TO PLACE AN ORDER, CALL (602)742-8601

APEX® µtech
DEDICATED TO EXCELLENCE

APEX MICROTECHNOLOGY CORPORATION
5980 N. SHANNON ROAD, TUCSON, ARIZONA 85741

TECHNICAL SEMINAR — IMPROVE YOUR APEX µtech ANALOG POWER

BEGINNING MAY 1991

THE APEX TECHNICAL SEMINAR
IMPROVE YOUR ANALOG POWER

CALL **1-800-421-1865** FOR SCHEDULED DATES IN YOUR AREA

▲ CALL 1-800-448-1025 TO RECEIVE A COPY OF THE HIGH PERFORMANCE AMPLIFIER HANDBOOK

CIRCLE 196

Screaming 1-year-old rattles industry.

The IBM RISC System/6000 family keeps delivering performance that's positively hyperactive.

Talk about precocious. Just a little over one year ago, when we proudly announced the arrival of the RISC System/6000™ POWERstations and POWERservers, they were already way ahead of the other kids in their class, delivering amazingly high performance for their diminutive price range.

	Hardware Price	MFLOPS	SPECmarks™
POWERstation 320H	$17,972	11.7	32.4
SPARCstation 2	$14,995	4.2	21.0
DECstation 5000	$19,395	3.7	18.5

Now, we're introducing the new RISC System/6000 POWERstation 320H. It runs 11.7 MFLOPS* and 32.4 SPECmarks.* If you already have the original POWERstation 320, you can upgrade it now to the even more spectacular performance of the 320H.

Yet Another New Addition To The Family.

Our POWERserver 950 is also brand spanking new. It gives you the performance of the POWERserver 550—25.2 MFLOPS and a SPECmark of 56.3—but in a rack-mounted system, to share more disk storage, power and expandability with others. And all the models in the UNIX®-based RISC System/6000 family can now add disk expansion units for up to quadruple their previous maximum fixed disk storage. This yields up to 22.2GB on the POWERserver 950.

A New Box Of Crayons.

Then there's the POWERgraphics GTO graphics subsystem. It can attach to any model in the RISC System/6000 family, to deliver super graphics performance previously available only in the POWERstation 730—990,000 3D vectors/second and 120,000 shaded polygons/second.

Memory At Prices That Won't Cause Tantrums.

And now you can get more memory for less. The more memory you buy, and the bigger the increments, the less you pay per MB. After all, just because we're a year old doesn't mean we don't know the value of money. Especially yours.

To find out more about the RISC System/6000 family, call 1 800 IBM-6676, ext. 878. And if you think this one-year-old is a handful now, just wait until the terrible twos.

CIRCLE 93

For the Power Seeker.

*SPECmark is a geometric mean of the ten SPECmark tests. MFLOPS are LINPACK double precision where n=100. AIX XL FORTRAN Version 2.1 and AIX XL C Version 1.1 compilers were used for these tests.

IBM and AIX are registered trademarks and RISC System/6000 is a trademark of International Business Machines Corporation. UNIX is a registered trademark of UNIX Systems Laboratories, Inc. SPECmark is a trademark of Standard Performance Evaluation Corporation. HAGAR THE HORRIBLE Character(s) ©1991 King Features Syndicate, Inc. ©1991 IBM Corp.

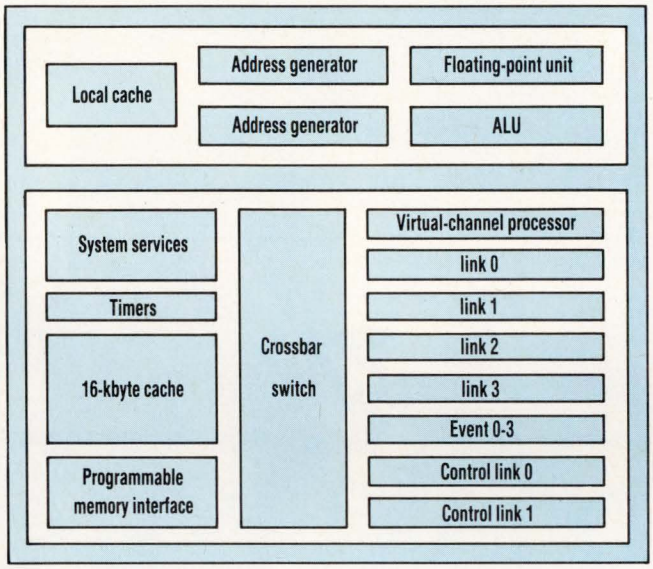
IBM®

OVERHAULED TRANSPUTER ARCHITECTURE UPS THROUGHPUT TO OVER 200 MIPS, 25 MFLOPS

The latest generation of processor chips can be likened to the body-builder stereotype—big, powerful, and good for crunching numbers, but limited when it comes to communicating. That analogy forms the foundation of both the old as well as the latest Transputer family members developed by Inmos Ltd., Bristol, U.K. According to Inmos, a processor should be finely balanced between multiple-task processing power and communications, as did the first generations of Transputers with their multiple serial ports, on-chip RAM, and integer and floating-point units.

Not only does the just-disclosed T-9000 Transputer achieve such a balance, but it does so with a vengeance, delivering between 200 and 250 MIPS and 25 MFLOPS of processing horsepower along with four 100-Mbit/s on-chip communication links *(see the figure)*. Target applications include real-time video imaging for high-definition television, industrial inspection, and multimedia office systems.

A T-9000 could transport and simultaneously process up to four image-transmission channels with a combined bandwidth of 80 Mbytes/s, and at the same time carry out such tasks as image compression, edge detection, or color conversion. Telecommunications usage covers areas like network protocol conversion and multiplexing. One such example is a network interface card that can multiplex 10 Ethernet channels onto a fiber distributed data interface (FDDI) wide-area network.



To obtain the multihundred MIPS throughput, designers at Inmos redesigned the Transputer's internal microarchitecture, exploiting architectural enhancements, instruction parallelism, and silicon-processing improvements developed over the last few years. The chip will employ a submicron three-metal-layer CMOS process that the company has already qualified for other products.

Presently, Inmos has the T-9000, which will be encased in a 208-pad leadless ceramic surface-mounted package, running as a series of "breadboard" modules and simulations. The first complete chips will be sampled in the next quarter, with production slated for the first quarter of 1992. But even with the major redesign, software compatibility with previous Transputer family members was kept intact. And Inmos designers retained the phase-locked clock-multiplication scheme that generates a high-speed 50-MHz clock on chip, from a simple 5-MHz off-chip synchronization clock signal. That helps keep pc-board layout requirements very simple.

The process can still reach higher speeds according to Ian Pearson, Inmos technical director. He claims that future versions will be able to internally clock at up to 70 MHz. In the meantime, one of the working silicon "subcomponents" belonging to the T-9000 is its on-chip memory—16 kbytes of fast static RAM. The RAM can be configured via software to form either a very efficient low-power cache or main program memory, or partitioned as half and half.

The RAM is organized as four independent banks of 4 kbytes each, and each bank can be accessed independently and simultaneously in one 20-ns clock cycle. When configured as a fully associative cache, a bank holds 256 lines, with each line containing four words. The cache operates in a write-back mode with random replacement for fast throughput and high hit rate while keeping power consumption down to a minimum. According to Clive Dyson, project design team leader, the memory can deliver data to the chip's pipelined processor at an aggregate rate of up to 800 Mbytes/s using its four 32-bit buses.

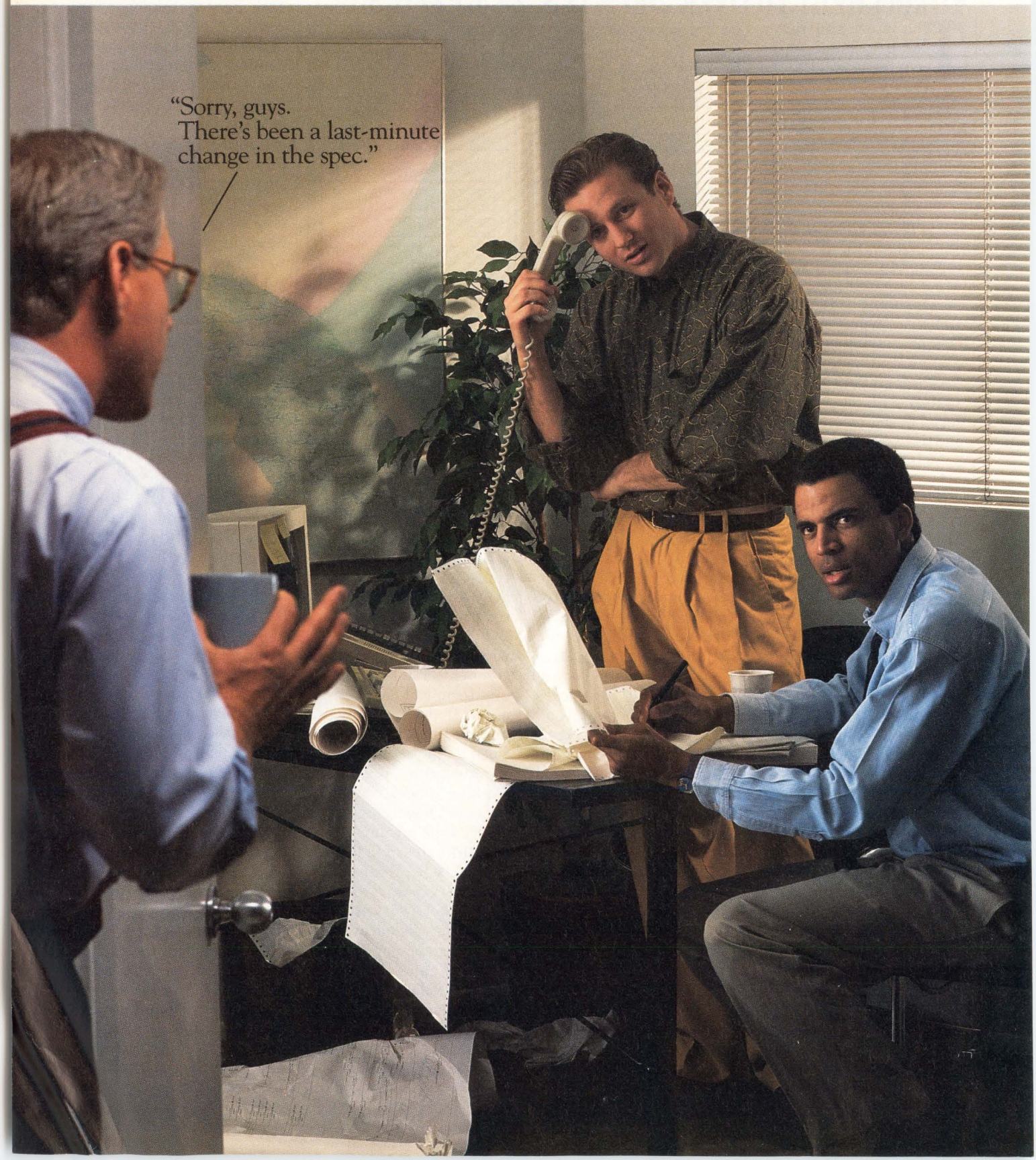
The pipeline needs data at that rate. It has five stages, each with its own local workspace memory and cache. A 32-instruction fetch-ahead buffer and instruction grouper feeds the pipeline. The grouper is implemented in hardware with a hardwired lookup table. The table lets it know which of the instructions waiting execution can be grouped together for simultaneous processing.

"The grouper puts together groups of instructions that require the same number of clock cycles to execute," explains Dyson. "Best case is four instructions per group. Further along the pipe, two such groups can themselves be grouped for a maximum of eight instruction executions per cycle."

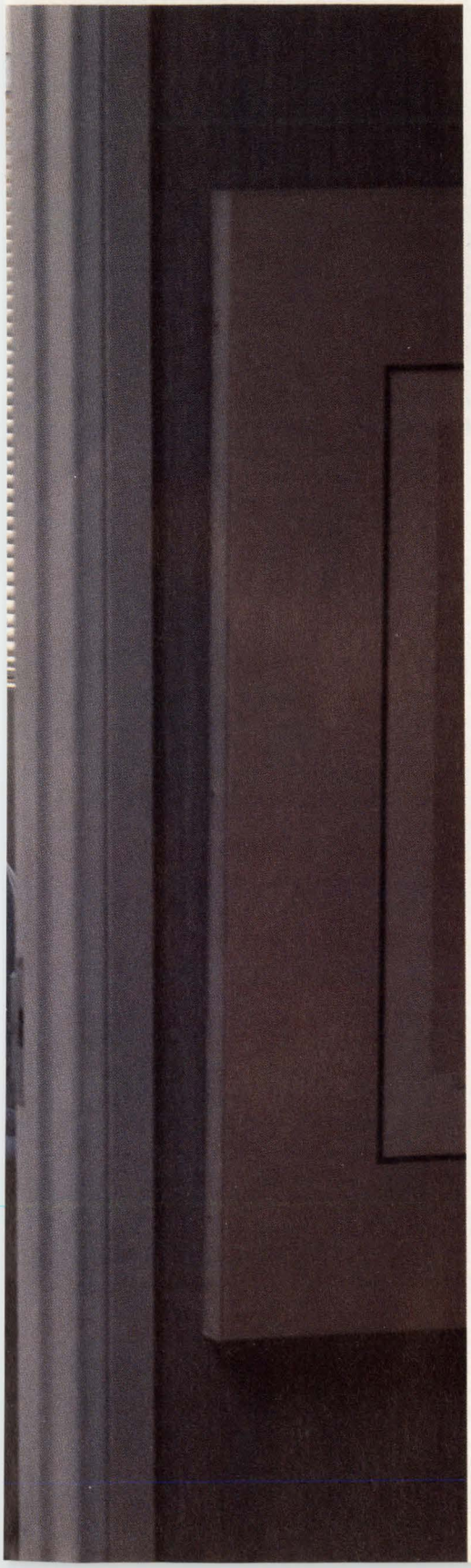
Two independent arithmetic processors take over at the end of the pipe—one for 32-bit integer operations, the other for full IEEE-754-compliant 64-bit floating-point math. Floating-point 32- or 64-bit additions require just two cycles. Similarly, just two cycles are needed for 32-bit multiplications. Multiplying two 64-bit numbers adds one clock cycle, while

IN THE ERA OF MegaChip™ TECHNOLOGIES

Sometimes you need easy-



ASIC. TI FPGAs.



These are the gate arrays you design at your desk. And redesign until they're exactly right. Then it's on to silicon — fast. Our free interactive diskette will show you just how easy *easy* can be.

Even when you hit last-minute changes, have a sudden inspiration or are simply intent on getting the job done, field programmable gate arrays (FPGAs) from Texas Instruments can speed your design from start to finish.

Our FPGAs are channeled devices, which gives them their true gate array characteristics. They combine the time-to-market advantages of programmable logic devices (PLDs) with the densities of gate arrays. You have a choice of 1,200 or 2,000 equivalent gate complexities, with 4K and 8K densities coming. And military versions are available too.

Throughout the design cycle, you are in complete control, minimizing risk and avoiding nonrecurring engineering costs.

Accelerated development

Our advanced development environment, the TI Action Logic™ System (TI-ALS), lets you design and redesign at your desk. You use TI-ALS to validate, automatically place and route, analyze, program, test and debug — all *within hours*.

You can always see what's going on within your design. Only the unique antifuse architecture allows 100% observability of internal nodes. And you can achieve gate utilizations of up to 90%.

TI-ALS operates on '386 personal computers or popular workstations running familiar CAE tools. You can program in minutes using our Activator™ hardware.

Unmatched service and support

From hands-on workshops at our Regional Technology Centers to a global network of sales offices and distributors, only TI can meet your FPGA needs across the country and around the world.

What's more, you can pick up the phone and talk with our FPGA applications specialists during regular working hours (CST). Just dial our FPGA Help Line — 1-214-997-5492.

To see how easy *easy* can be, call 1-800-336-5236, ext. 3712, for our free interactive diskette

It will show you why our FPGAs are easy-ASIC and will introduce you to system design advantages that you can achieve quickly and efficiently.

The diskette runs on any MS-DOS® PC with an EGA or VGA graphics card, and we'll include the diskette with our FPGA DataFile. Just call the number above or complete the return card.

™ MegaChip is a trademark of Texas Instruments Incorporated.
Action Logic and Activator are trademarks of Actel Corporation.
® MS-DOS is a registered trademark of Microsoft Corporation.
© 1991 TI 08-1041

TEXAS INSTRUMENTS

32-bit division and square-root operations each require eight clock cycles. A "virility" benchmark done by the company shows that just one processor can run a 1024-point, double-precision, floating-point, complex fast Fourier transform in 2 ms. This is accomplished using a program written in a high-level language, such as Fortran, compiled and run without any special tuning.

Blazing pipeline and calculation speed aren't compromised by communications, Dyson asserts, because a dedicated virtual communications processor takes care of routine interconnection chores, like labeling packets, interrogating processes waiting for input data, setting up a process to receive fresh data, and looking after handshaking between processes. The four communication links each require just four pins and drive 100-Ω transmission lines. Signals can be sent over distances of up to 10 m for board-to-board or inter-rack communications.

Each of the serial links on the T-9000 can be set up to service up to 64,000 duplex "virtual" channels using a packet-multiplexing protocol, thus allowing an almost unlimited number of communication processes to be concurrently executing. The links are designed to directly interconnect the processors to give full linear scalability.

"System processing power increases in direct proportion to the number of CPUs used," says Paul Strzelecki, marketing director. That rule, he claims, holds true even for systems with thousands of processor nodes.

The chip's main functional blocks interconnected by what Dyson terms a "crossbar" network of 32-bit buses. He depicts it as four vertical buses that interconnect the four on-chip memory segments with the memory interface. A CPU pipeline, a virtual communication processor, and a hardware system scheduler cross-connect with all four main buses, each with their own 32-bit buses.

Other external connections include two more communications links for system control, and an event or interrupt pin. The control links are completely separate from the program communications links. They provide an independent communications network that can be used to load code, carry out hardware debugging, monitor a running system for errors, and perform diagnostic functions. Another system simplifier included on the chip is a programmable memory interface that allows the chip to handle any or all of four memory types—DRAM, SRAM, VRAM and EPROM. Using external drives, the processor can address up to 4 Gbytes. The interface can address up to 8 Mbytes of low-cost two- or four-wait-state DRAM without external buffering.

Programming has been made simple too, claims Strzelecki. Because the processor is binary-compatible with earlier Transputers, it can deliver a ten-fold performance boost over older Transputers when running existing software. New compilers, though, that can take full advantage of the new chip's abilities, are available for C, C++, Fortran, and Ada programming languages. A Postscript compiler is also available. Contact Paul Strzelecki at Inmos U.K., (44) 0628 890900, or Inmos U.S. at (602) 867-6100.

DAVE BURSKY AND PETER FLETCHER

ADVANCED CIRCUIT/PROCESS LETS HIGH-SIDE MOSFET/IGBT DRIVER IC ALSO SENSE CURRENT

Advancements in circuit techniques and processing have allowed International Rectifier Corp., El Segundo, Calif., to develop high- and low-side driver ICs that not only offer undervoltage-lockout protection, but a number of other self-protection features. One of the features involves the ability to sense, and thus limit, switch current. The high-side (IR2125) driver is fabricated on a 500-V CMOS/DMOS process that builds bipolar and CMOS transistors; the low-side driver is fabricated on a similar 20-V process *(see the figure)*. While the circuit shown is driving a current-sensing FET, a standard FET or an IGBT can also be driven.

The pair represent the second and third members of IR's family of MOSFET drivers, which started with the IR2110. Also built on the 500-V process, the IR2110 provides both low- and high-side drive, but switch protection is limited to undervoltage-lockout protection. The new power MOSFETs and their insulated-gate bipolar-transistor (IGBT) kin are finding much use in large, off-line, switching power supplies and motor-control systems that use half- and full-bridge circuits *(see "Chips/Pulse Transformer Build HV High-Side Drivers," p.36)*.

To turn on a high-side FET switch, its gate must be pulled 10 to 20 V above its source, which, when the FET is on, is essentially at the high-voltage rail. As a result, the high-side driver for each FET must operate from a floating 10-to-20-V supply (V_B, pin 8) whose minus terminal is tied to that FET's source. The driver must increase the 5-V, TTL/CMOS input control signal (pin 2) to between 10 and 20 V, then level-shift it so logic low is at the potential of the FET's source (V_S, pin 5). Low-side drivers need only increase the amplitude of the drive signal.

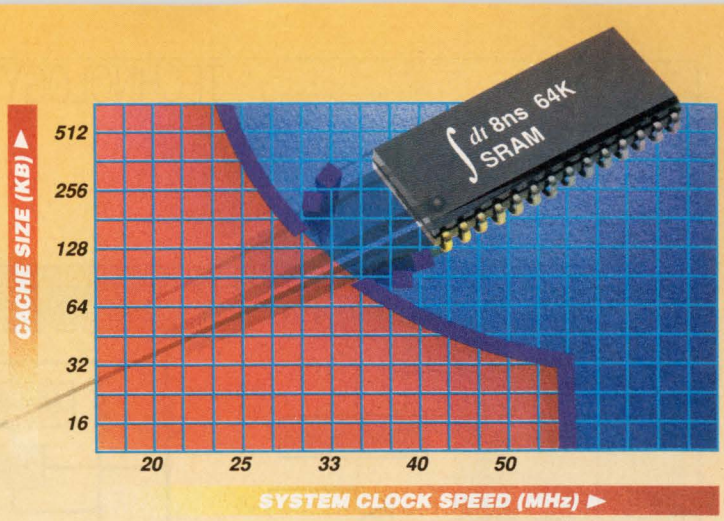
The IR2125 employs a bootstrap supply for its floating drive voltage V_B. That voltage is developed from the chip's power rail V_{CC} (pin 1), using the bootstrap diode and capacitor as the FET switch turns off and on. On- and off-chip circuits, operating at high voltage, are highlighted in the figure.

The input logic-control signal feeds a comparator with hysteresis, which in turn feeds a pulse generator through the shutdown latch. If V_{CC} is below 8 V or above 20 V, which is the over/undervoltage (OV/UV) detector's typical trip point, the circuit shuts off the FET switch by blocking the input signal in the

Smash the Cache Barrier

IDT's 64K BiCEMOS™ TTL I/O Static RAMs are the ideal solution for high-density cache systems, and are the perfect match for optimizing the high-performance needs of RISC and CISC processors. These 8ns and 10ns SRAMs provide the highest system speed without sacrificing system chip count or increasing power consumption.

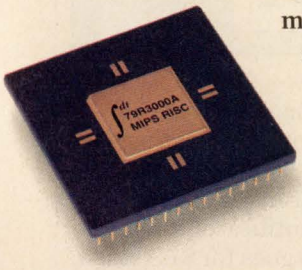
Smash the barrier to efficient cache operation at the highest clock speeds. Call today and ask for **Kit Code 8041** for free samples of our new 16K x 4 and 8K x 8 TTL SRAMs.



COUNT ON IDT

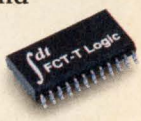
35MIPS RISC COMPONENTS AND MODULES

R3000A, the most MIPS at any MHz. The R3051 integrates CPU, cache, and buffers on one chip. RISC modules, eval. boards, and software complement our family of **mips**™-based RISC products. Your **RISC** solution is a phone call away!



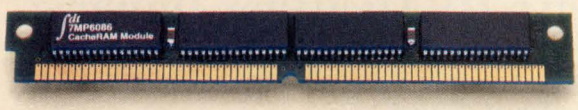
4ns LOGIC: WORLD-CLASS SPEED

The industry leader. FCT-AT and FCT-CT CEMOS families achieve the fastest speeds with 40% less noise. Everything you need for high-performance designs can be found in the ***Logic Data Book.***



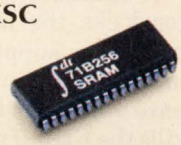
HIGHEST-PERFORMANCE MEMORIES

Fast FIFOs, dense dual-ports, BiCEMOS ECL, and modules for every system. Over 120 of the fastest FIFOs and multi-port memories. 5ns ECL SRAMs, as well as standard and custom memory modules. Get the specs in the ***Specialized Memories Data Book.***



12ns 256K SRAMS

Fastest cache solutions for RISC and CISC processors. More than 36 ultra-high-speed sub-micron SRAMs for 33MHz processing and beyond. Read all about them in the ***SRAM Data Book.***

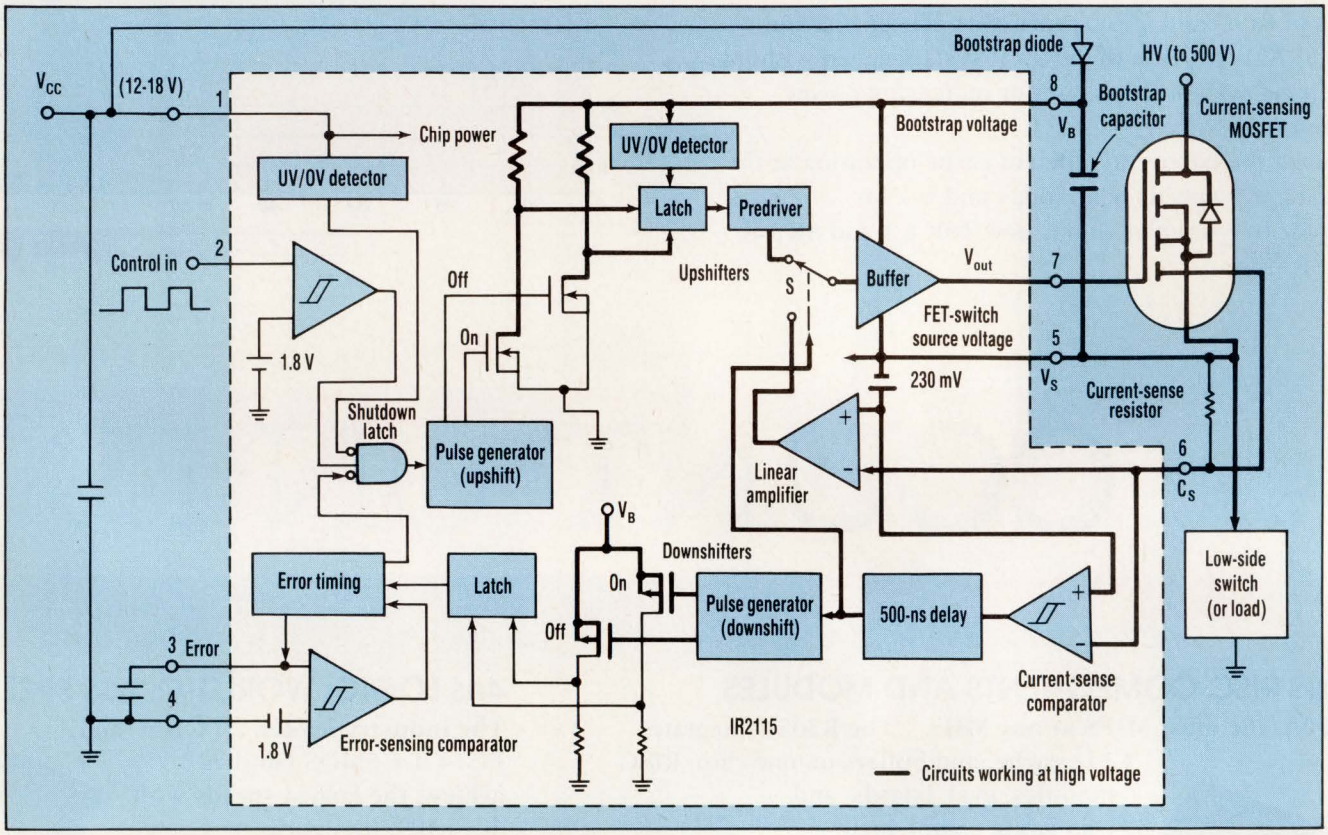


Call today for your new IDT data books with complete technical specifications and application information.

When cost-effective performance counts.

(800) 345-7015 • FAX: 408-492-8454

Integrated Device Technology, Inc.



latch. The pulse generator puts out narrow On and Off pulses triggered respectively by the input signal's rising and falling edges. A pair of 500-V n-channel DMOSFETs shift the pulses to the level of the floating rail. There they Set and Reset an RS latch working off the rail.

A second UV/OV detector locks the latch if the bootstrap supply exceeds its high or low limits (if gate voltage is too high, it kills the FET; if too low, the FET can go into a linear operating region resulting in excessive power dissipation). The latch feeds a predriver and a CMOS buffer that puts out peak currents of 1 A in pull-up and 2 A in pull-down modes. Driving a capacitance of 3300 pF, the buffer typically provides rise and fall times of 43 and 27 ns, respectively.

When the voltage across the user-selected current-sense resistor exceeds the 230-mV threshold of the current-sense comparator, the comparator fires. After a 500-ns delay (to avoid false triggering by spikes when the FET switches), switch S between the predriver and the buffer moves to the output of a linear amplifier, forming a negative-feedback loop composed of a buffer, FET switch, and amplifier. The gate-drive voltage V_{out} settles to a lower value, which limits the FET's current to its original preset value.

The output of the 500-ns delay is also downshifted to the low-voltage level by a circuit like that of the upshifters. However, it uses 500-V p-channel (instead of n-channel) FETs to drive the latch. The output of the latch feeds the error-timing circuits. These circuits and the error comparator perform a number of FET-switch protection functions, including linear-mode timing. If the FET is shorted, they determine the type of short (hard or pulsed), perform cycle-by-cycle external shutdown, and provide a status output flag on pin 3. With the exception of level-shifting circuits and the need for a floating supply, the high- and low-side switches are functionally similar.

The drivers come in 8-pin plastic DIPs rated for operation from –40 to +150°C. In quantities of 1000, the IR2125 goes for $4.80 each. The IR2121 costs $2.48 each in similar quantities. For additional information, call Arnold Alderman, 1-(800) 245-5549.

FRANK GOODENOUGH

CHIPS/PULSE TRANSFORMER BUILD HV HIGH-SIDE DRIVERS

Though low-side driver ICs for power MOSFETs and insulated-gate bipolar transistors (IGBTs) continue to grow in numbers, high-side drivers needed in full- and half-bridge plus many control applications are few and far between. Moreover, those becoming commercially available are limited to a differential input-to-output rating of a few hundred volts because of the semiconductor process on which they're fabricated *(see "Advanced Circuit/Process Lets High-Side MOSFET/IGBT Driver IC Also Sense Current," p. 34).*

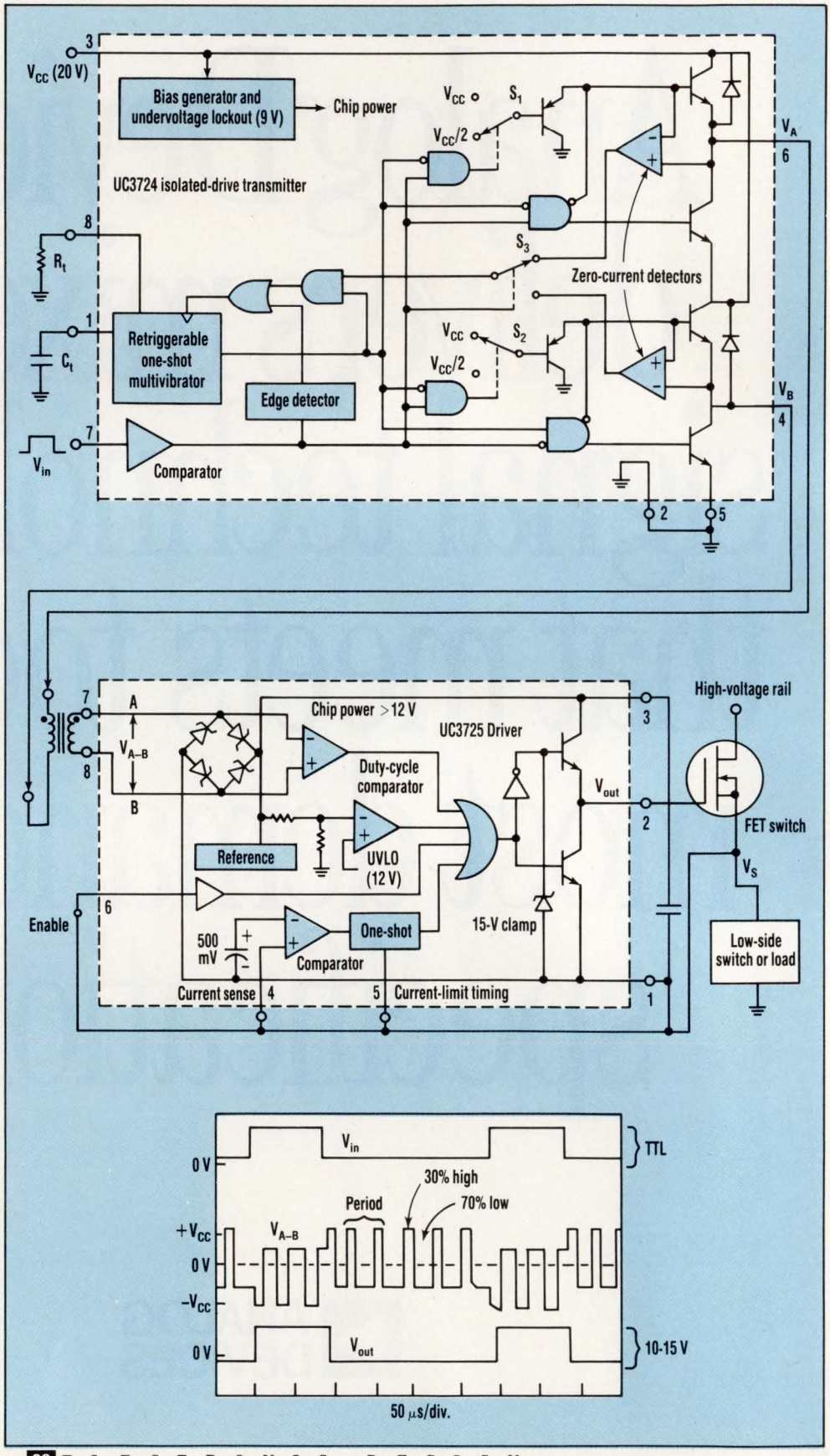
Analog Devices delivers mixed-signal technology that meets today's most demanding specifications.

ANALOG DEVICES

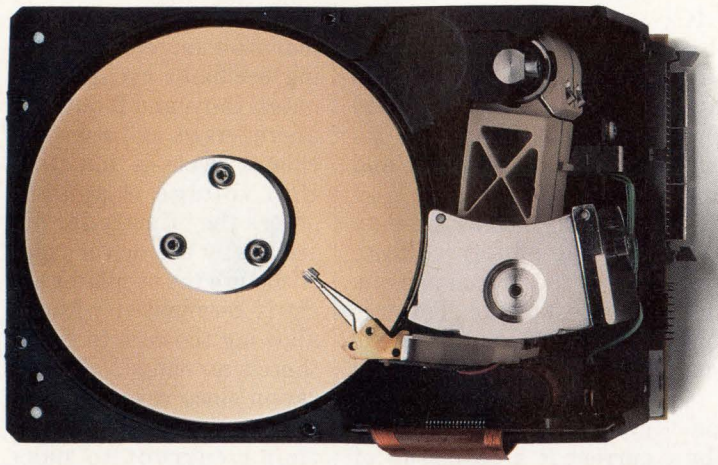
But in many applications, particularly motor controls and uninterruptible power supplies (UPSs), the FET switches run directly off the rectified ac lines. For reliable performance, they require drive circuits that supply up to several thousand volts of input-to-output true galvanic isolation. No one wants to see even a tiny fraction of those voltages sneak into a host computer. However, until now, only complex, costly, and relatively unreliable multidevice discrete solutions have done the job.

To answer that problem, Unitrode Integrated Circuits Corp., Merrimack N.H., developed a high-side-driver chip set that transfers the isolation job to a single, inexpensive (under 35 cents each in volume), small pulse transformer. One chip, the UC3724, sits at input-control-signal (logic) potential. The other, the UC3725, floats at the FET's source voltage V_S. That is, the chip's "ground" pin is connected to the FET's source pin *(see the figure)*.

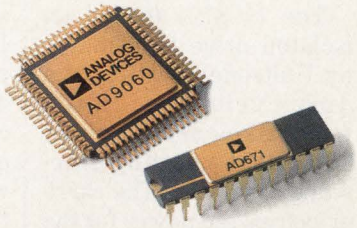
The transformer carries both the On-Off command for the FET switch and continuous operating power for the high-side chip, while providing isolation limited only by its insulation. Neither IC "sees" the high voltage. As a result, the ICs can be built on a low-cost 40-V bipolar process. Power transfer goes on regardless of whether or not commands are being transmitted. Many alternative techniques that generate floating high-side drive power require that the supply be "refreshed" (by switching action at some minimum rate) when



Faster.

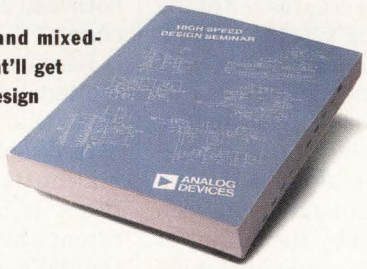


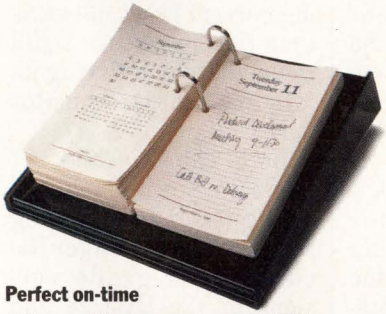
In the disk drive market, you've got to be fast – in both performance and time-to-market. That's why seven of the top 10 disk manufacturers rely on Analog Devices for mixed-signal components.



AD9060 & AD671 – The fastest 10-bit and 12-bit monolithic A/D converters, respectively. The AD9060 guarantees encode rates up to 75 MSPS for unparalleled dynamic performance. The AD671 is twice as fast as any other 12-bit monolithic, converting in under 0.5 μs, thanks to our high-speed mixed-signal ABCMOS process.

Tap into 25 years of experience at our high-speed and mixed-signal design seminars. You'll learn new techniques that'll get your applications to work more quickly, and you'll get design manuals that put all this information right at your fingertips.





AD9712 – The only 12-bit, 100 MHz D/A converter on the market. Ideal for high-speed video and direct digital synthesis, its low glitch and low harmonics combine to deliver a spectrally pure output waveform.

Perfect on-time delivery – it's our goal and at 97% we're getting close, thanks to our continuous improvement process based on Total Quality Management. Over 150 TQM teams make the customer and quality improvement the focus of our entire organization. A focus that gets translated into not just catchy slogans, but real action.

Our Spectrum CAD Tool is 100 times faster than traditional SPICE programs, so it makes quick work of mixed-signal ASIC design cycle time.

ADSP-2101 – Talk about fast – this DSP microcomputer executes a 1024-point FFT in only 2.26 ms. That's faster than other DSPs that operate at almost twice the clock rate. And since our entire ADSP-2100 family is code compatible, your code will run fast on all of our DSPs.

Today, Analog Devices offers more high-performance mixed-signal components than anyone else. And we get them to you fast. So if you want mixed-signal ICs that'll help you design faster performing products, from a company that'll help you get your product to market faster, call us at 1-800-262-5643.

ANALOG DEVICES

CIRCLE 165

functional switching isn't underway. Otherwise a startup time is required.

The UC3724 (called an isolated drive transmitter by Unitrode) consists of a duty-cycle modulated fixed-frequency (to about 600 kHz) rectangular-wave oscillator. The carrier carries the power for the UC3725 driver; its modulation carries the command signal. The TTL input to the transmitter (V_{in}, pin 7) switches the oscillator's duty cycle between two possible formats (for example, between 30-70% and 70-30%). That is, when the TTL input is logic low, each oscillator output cycle is logic high 30% of its period, and logic low 70% of the time. When the input is logic high, each oscillator cycle is high 70% of its period, and low 30%.

Usually, when a train of rectangular pulses with other than 50% duty cycle (such as those just described) is passed through a transformer, the average magnetizing current isn't zero and the transformer's core will saturate. This oscillator's unique design prevents such saturation by ensuring that its magnetizing current decreases to zero between each output cycle. Average voltage across the transformer is always zero, even under the transient conditions caused by input command changes, so core saturation is virtually impossible.

After passing through the transformer, the portions of the waveform with different duty cycles are level-shifted relative to each other, and to $\pm V_{CC}$ *(see the waveforms)*. The duty-cycle comparator in the UC3725 driver examines the waveform V_{A-B} (between A, pin 7; and B, pin 8), and in just one cycle detects the level shift. It creates V_{out} (pin 2), a 10-to-15-V version of the TTL input signal. The Schottky-diode bridge rectifies the carrier to provide chip power. A second comparator with programmable off time (at pins 4 and 5) can implement overcurrent protection. The enable input (pin 6) adds additional control and protection flexibility.

The retriggerable one-shot's pulse width (set by R_t and C_t) creates 1/3 of the oscillator's total period, and the transformer core's reset time creates 2/3 of the its period. Working together, they form a free-running multivibrator. Assume the one shot has been triggered by the output of one of the zero-current detectors (a comparator). The full supply voltage is applied to the transformer primary; one output (assume A) is high, the other (B) is low. Transformer magnetizing current in the primary winding rises linearly at a rate (di/dt) determined by the inductance and the applied voltage:

$$di/dt = \frac{-V_A - V_B}{L_{primary}} \ (A/s)$$

When the one-shot times out, the logic circuits switch the low output (B) high with S_2 (letting its catch diode conduct), and the high output (A) to $V_{CC}/2$ with S_1. The action puts half the supply voltage across the primary in the reverse direction. Power is only transferred to the secondary circuit when full voltage is across the primary, during which time its current is a composite of both load and magnetizing current.

Because the load current is interrupted when the polarity is reversed and halved, only a decreasing magnetizing current flows. It falls at half the rate at which it's increased, thus taking twice as long to drop to zero. This resets the core and prevents its saturation. Output A's zero-current detector senses zero magnetizing current and triggers the one-shot, initiating another oscillator cycle. If a continuous high is commanded, the waveforms driving outputs A and B are interchanged, again reversing the magnetizing current.

When the input command is changed, the existing oscillator cycle terminates, the A and B outputs are reversed, and a new oscillator cycle is initiated. Full voltage is applied across the primary for detection by the driver chip. Although the oscillator cycle is terminated without allowing the core to reset, there's no danger of saturation since reversing the outputs forces the magnetizing current to pass through zero before increasing in the opposite direction. Because the one-shot cycle was terminated early (by the change in command), the magnetizing current is actually less than the current for a full cycle, thereby reducing its fall time and the oscillator period.

Both chips in the set come in 8-pin DIPs. In quantities of 1000, pricing starts at $1.75 each for the commercial-grade versions of the UC3724 and UC3725. For additional information, call Joe Pappalardo at (603) 424-2410.

FRANK GOODENOUGH

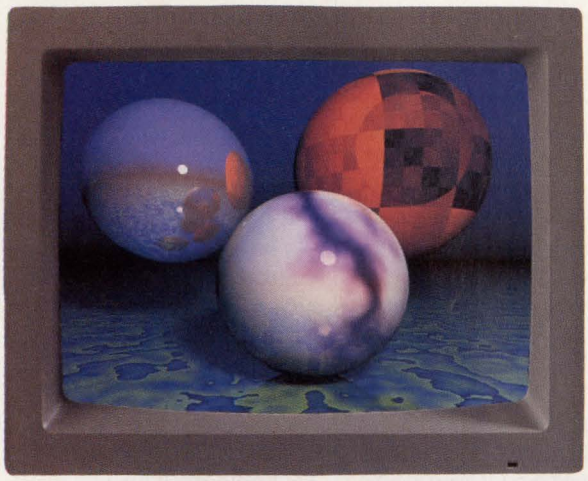
SIMPLE LIQUID-PHASE EPITAXIAL PROCESS YIELDS 22.3%-EFFICIENT GaAs SOLAR CELLS

In worldwide solar-cell development efforts, the name of the game is high efficiency at low cost. That is, getting the most from the solar-to-electrical energy conversion process at a practical cost level. Now, as part of a government-financed project, researchers at the Fraunhofer Institute for Solar Energy Systems in Freiburg, Germany, have fabricated gallium arsenide solar cells with 22.3% efficiencies with a simple process.

A small production run of 35 laboratory-type GaAs cells, which use a relatively simple technology, showed good yields. The 1-cm^2 cells checked in with efficiencies that were fairly constant between 20% and 22%.

Although the highest for a research group in Europe, the efficiency of 22.3% is by no means a world record, the Freiburg institute says. The highest reported figure for GaAs solar cells is 25.7%, and it was achieved by a group at the Solar Energy Research Institute (SERI) in Denver, Colo. However, the 0.25-cm^2 SERI cells were made with a relatively expensive layer technique involving a metal organic chemical-vapor-deposition (MOCVD)

Better.



Picture this – a PC monitor that offers the same color and clarity as a high-end engineering workstation costing as much as 20 times more. Our pin-compatible RAM-DAC is literally redefining the low end of the PC monitor market.

Marball. Original image courtesy of University of California, Davis.

'Try, try again' is a costly way for manufacturers to find the best design solution. So to help our customers find answers to tricky problems the first time around, technical application engineers are just a phone call away. In some instances, they're even located right on the customer's premises.

After analyzing semiconductor suppliers, many of the leading oscilloscope and spectrum analyzer manufacturers chose Analog Devices for their mixed-signal components. One reason is our ability to deliver high performance at high levels of integration – for example, our AD640, which replaces a chain of discrete log-amps for higher accuracy.

With our motion control ICs, several major aircraft companies are staying right on course. High reliability and accuracy are hallmarks of our 2S80, AD598 and the rest of our nearly 400 defense-qualified products.

Today, Analog Devices offers a better line of high-performance mixed-signal components than anyone else. And no one has a better record for reliability, or more experience in analog, DSP and mixed-signal ICs. If you want mixed-signal components that'll help you design better products, the best thing to do is to call us at 1-800-262-5643.

Continuous Edge Graphics is a trademark of Edsun Laboratories.

ADSP-2111 – Better integration on the best architecture in the industry. Adds an 8/16-bit host port to the two serial ports, timer, hardware companding and memory already on the ADSP-2101. And like all our DSPs, it's got fast, flexible arithmetic, wide dynamic range and a single cycle fetch of two operands (on- or off-chip). Plus it's code-compatible with the rest of our DSP family, so what's written today will be useful tomorrow.

ADV7141 – Our new Continuous Edge Graphics™ RAM-DAC gives users of standard low-end color monitors better graphics on their PCs. Graphics that are virtually the same as those produced on expensive engineering and scientific workstations. It does this by eliminating jagged edges, providing photo-realistic colors and shading, and displaying text comparable to a 300-dpi laser printer.

AD75028 – This custom ASIC passes the test for a top automatic test equipment manufacturer. Serving the function of 21 separate 12- and 8-bit D/A converters and providing on-chip static RAM, it also has seven channels of level setting (other monolithics only have four), and can automatically remove gain and offset errors.

ANALOG DEVICES

CIRCLE 166

process.

The Fraunhofer cells, by contrast, use a simpler and environmentally cleaner process based on liquid-phase epitaxy. The institute thinks that the 22.3% efficiency for its cells isn't the limit achievable with this process. By optimizing the cell construction, it hopes to push the efficiency to 23%.

After silicon, GaAs is the second most important material for high-efficiency solar cells. Compared to silicon, though, GaAs has higher light absorption. Therefore, the thickness of the cell's active area need be only a few nanometers. For silicon-based solar cells, on the other hand, that thickness must be from 60X to 100X higher.

Other advantages that GaAs has over silicon is that its theoretical-limit efficiency is higher. Also, GaAs cells can operate at higher temperatures as they exist, such as when the sunlight is concentrated onto the cell. Furthermore, because they're less sensitive to cosmic rays, GaAs cells can be used to supply energy to satellites in outer space.

For terrestrial photovoltaic applications, GaAs is an interesting material for tandem and concentrator solar-cell systems. Tandem systems consist of two cells, one atop the other. Each cell is adapted to a different solar-spectrum region so that sunlight can be better exploited than is possible with one cell.

In concentrator systems, a mirror or lens arrangement focuses the sunlight onto the cell. This scheme calls for just a fraction of the cell area that's needed for non-concentrating solar-cell systems.

Currently, the Fraunhofer institute is refining its liquid-phase epitaxy technique so that it can be used to fabricate cells larger than 1 cm^2 and in larger production runs. Other work involves experiments in depositing GaAs onto silicon and germanium substrates, also by epitaxial methods.

This work aims at lighter and less expensive GaAs solar cells. Also, by cutting GaAs material consumption to a minimum, any environmental damage is limited. The environment is further protected because GaAs solar cells are used only for special applications—for example, in satellites and in concentrator-cell systems.

The four-year development effort at the Fraunhofer Institute for Solar Energy Systems (the work ends in 1992) is fully financed under a $3 million contract from the German Ministry for Research and Technology. The institute is carrying out its work in cooperation with research groups in the industry and at the University of Stuttgart, Germany.

JOHN GOSCH

What's more paralyzing is the way he gets treated.

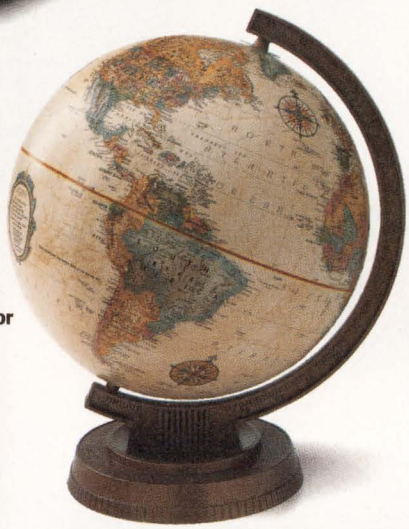
The hardest part about having a disability is being constantly reminded that you have one. Sometimes that happens when people stare at you. Or point at you. Or don't even think of including you in every day activities. Maybe it's time to start treating people with disabilities like people.

Easter Seals®

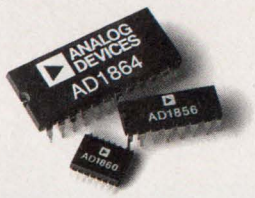
Cheaper.

More gadgets for less money, and make it work better – that's the only way to survive in consumer electronics, the most competitive market there is. That's why three of the top five Japanese electronics firms rely on us to meet their mixed-signal needs in applications ranging from CD players to video cameras.

We're far from your local component boutique. Over half of our $540 million in revenues comes from international sales. And with manufacturing and stocking facilities on just about every continent, getting products to you quickly is a snap. Plus multiple manufacturing facilities allow us to take advantage of the right talent and processes for the job at hand.



With billions of dollars in annual sales at stake, the video game market is anything but child's play. One leader in this market found that with our DSP they could create more realistic and interactive games. As a result, they're driving away with a bigger share of the market.



SOUNDPORT DACs – We've made these DACs cost-efficient by making them complete with output amplifier, reference and digital logic interface. Perfect for high-fidelity digital audio and multi-media applications, these mixed-signal ICs achieve SNRs as high as 108 dB and THDs as low as 0.0025%.

AD712 – If you're working in professional audio and compact disc applications, you'll like the sound of this – an IC that combines two high-performance op amps in one compact package. You get low offset voltage and low input bias currents coupled with superb transient response, ambience, clarity and dynamic range.

ADSP-2105 – High performance DSP at an incredibly low price. So low, in fact, you can now consider DSP in a host of new applications. And since it's pin-compatible with the ADSP-2101, and code-compatible with all of our other DSP processors, upgrading is easy and inexpensive.

Today, Analog Devices offers more cost-effective solutions to your high-performance mixed-signal needs than anyone else. Solutions that are surprisingly affordable, whether they're available off the shelf or developed for a specific application. To find out more about how we can help you develop products more efficiently, or for a free copy of our recent Mixed-Signal Technology white paper, call us at 1-800-262-5643.

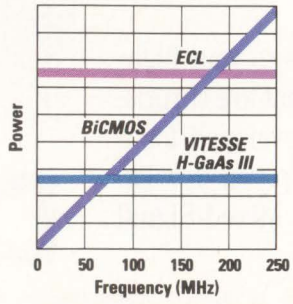
ANALOG DEVICES

Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106. Headquarters: (617) 329-4700. Offices and applications support available worldwide.

CIRCLE 167

© 1990 Vitesse Semiconductor, Inc. The GaAs Company is a trademark of Vitesse Semiconductor, Inc.

ONE MILLION TRANSISTORS AND



We're talking better than the best ECL performance at a fraction of the power. And for high frequency designs, Vitesse GaAs chips are lower power than BiCMOS.

Our prices won't sink your budget either– our GaAs chips can give you better performance for your dollar than BiCMOS.

THE BLINDING SPEED OF GaAs.

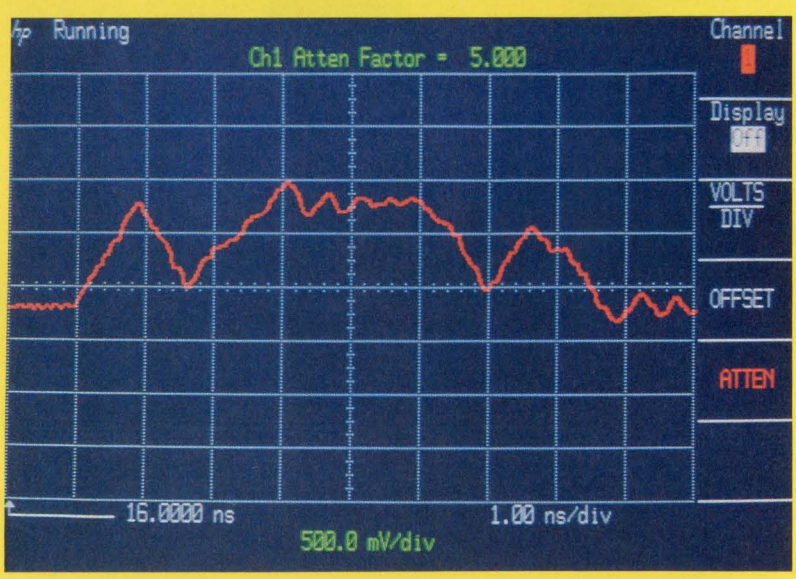
For more information on our ASIC and standard products with integration levels up to 350K gates, call Vitesse at (805) 388-7455. And leave the competition in your wake.

FX Arrays	Raw Gates	Usable Gates	Availability
FX100K	102,000	Up To 70,000	Now
FX200K	195,000	Up To 137,000	Now
FX350K	353,000	Up To 177,000	Summer 1991

VITESSE
The GaAs Company.™

CIRCLE 168

REMEMBER WHEN SQUARE WAVES WERE SQUARE?



Typical Digital Waveform, circa 1990
Clock rate > 100 MHz
Rise/Fall Time < 0.5 nsec.
Equivalent microwave signal > 1GHz

THAT WAS THEN. THIS IS NOW.

If you're designing today's high speed digital ICs, circuits or systems, you're probably looking at clocks of 100 MHz or faster, with signal components exceeding 1GHz. At these speeds, digital signals assume the characteristics and problems of microwaves.

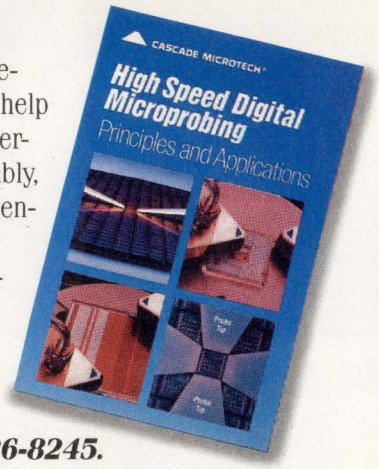
Welcome to the future.

At Cascade Microtech we offer high speed T&M solutions based on measurement technologies bred and proven in microwaves, and now available for today's digital world.

Our high frequency microprobing equipment and computer-aided test software will let you accurately characterize circuits, devices, packages, and even boards. *At their full operating speeds.* So you can quickly eliminate timing skew, degraded signal edges, ground bounce, and other high speed problems.

Free Booklet

To introduce you to high frequency microprobing, and help *you* create products that perform better and more reliably, we've prepared a comprehensive booklet, *"High Speed Digital Microprobing: Principles and Applications."*



For your free copy, use the reader service card, write, or call Jerry Schappacher at ***(503) 626-8245.***

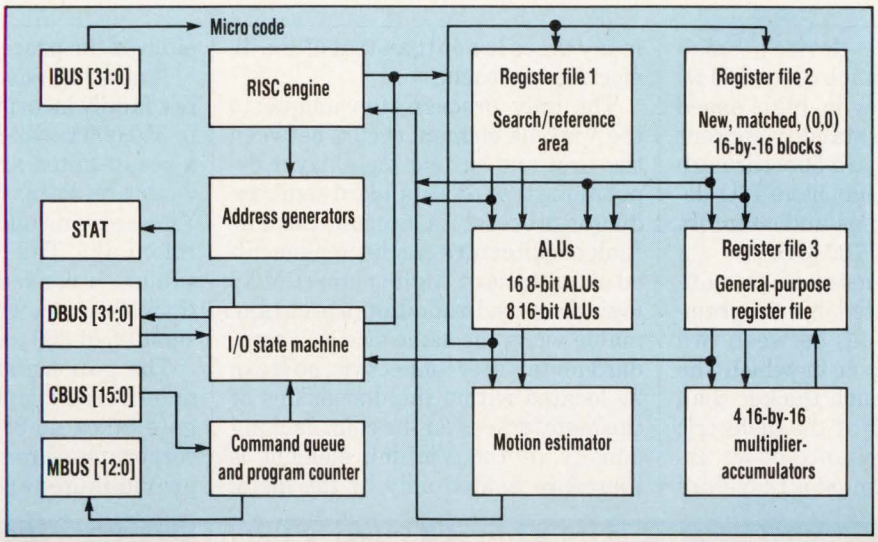
CASCADE MICROTECH®

14255 SW Brigadoon Ct.
Beaverton, Oregon 97005

Come See Us At CICC, Booth Number 19

© 1990 Cascade Microtech, Inc.

CIRCLE 116 Information Only
CIRCLE 108 Have a sales engineer contact me now



1. THREE INTERNAL REGISTER FILES, a motion estimator, multiplier-accumulators, and ALUs are among the major functional units of Integrated Information Technology's Vision Processor. The chip is powered by a 16-bit RISC engine.

PAPERS FROM OVER 30 COUNTRIES DESCRIBE THE LATEST IN ANALOG AND DIGITAL ASICS AND DESIGN SOFTWARE.

CICC ACCENTS GLOBAL ASIC TECHNOLOGY

LISA MALINIAK

With ASICs permeating every area of electronics, the Custom Integrated Circuits Conference (CICC) is distinguishing itself as an important international industry event. This year's conference offers the latest ASIC technology from all over the world, with more than 170 papers, almost half of which are from 30 countries outside the United States. The conference, being held in San Diego, May 12–15, covers a wide swath of technology: design automation; digital-signal-processing applications; fabrication technology; device, circuit, and system modeling and simulation; analog circuits; telecommunications applications; interfaces and packaging; and design-for-test. Many of the devices described are standard ICs developed by semiconductor manufacturers, which highlights the growing trend toward using ASIC methodologies to create commercial chips *(see "IC design adopts ASIC techniques," p. 48).*

A session on new hardware products spotlights high-speed, high-density, low-power, CMOS field-programmable gate arrays (FPGAs) based on an antifuse technology called ViaLink. The technique, developed by QuickLogic Corp., Santa Clara, Calif., fabricates devices using a direct metal-to-metal program-

ming element. The device's small size and low-impedance (under 50 Ω) interconnect results in high speed and density with a standby current below 5 mA. There are 500- through 4000-gate devices that have I/O delays of less than 15 ns and counters that operate at over 100 MHz.

The ViaLink element is an antifuse structure created in a programmable via that resides between two metal layers. The via in which the link is formed is much thicker than the insulating layer of the dielectric antifuse. The capacitance of an unformed ViaLink element is therefore many times lower than that of the dielectric approach.

The only process step unique to the ViaLink element occurs between the first and second metal-layer deposition steps of a standard semiconductor process. As a result, the ViaLink architecture can be implemented on a standard, high-volume CMOS logic process. In addition, a programmable via is the same size as a standard metal-interconnect via, so it can be located within the dimensions of the metal traces on the chip. Packing density of the ViaLink element is therefore limited only by the metal pitch of the process.

A new high-density GaAs gate-array family incorporates from 100,000 to 350,000 raw 2-input NOR gates in a sea-of-gates architecture. The devices are discussed in a paper from Vitesse Semiconductor Corp., Camarillo, Calif. The high-density arrays exhibit unloaded gate delays less than 50 ps at a worst-case power dissipation of 250 μW.

The gate-array cell contains two unbuffered 2-input NOR gates. One gate takes up 380 μm^2. This cell incorporates three changes from the previous-generation GaAs chan-

IC DESIGN ADOPTS ASIC TECHNIQUES

Worldwide competition in electronic markets is forcing standard-IC developers to adopt ASIC design techniques. These techniques include capturing designs at the gate level or higher, using synthesis to map higher levels of design into library elements, and using chip-level timing simulation and analysis. These techniques let chip designers focus on functionality and floor plan, while leaving the specific implementation and layout details to the software. Although these methods make it easier for standard-part designers to quickly frame and finish chip designs, custom integrated-circuit design techniques are still critical for creating cell libraries.

ASIC design techniques improve productivity and time to market, but they don't remove the market pressures on the off-the-shelf products. Standard-part die must be as small as possible to improve yield and minimize manufacturing cost. They must also operate as fast as possible to be competitive. Consequently, custom IC design is more focused on creating fast, dense circuit blocks for the libraries that support the ASIC techniques.

Custom design of digital libraries involves using some manual editing techniques. This may mean "polygon pushing" for ultra-dense cells like dynamic random-access memories. Alternatively, compilers and symbolic layout editors may be utilized for blocks with a higher percentage of digital logic circuitry.

Comprehensive verification and characterization of the library cells is also included in custom design. Characterization supplies the performance data that allows ASIC design tools to make the best trade-offs when using and laying out the cells.

IC design tools are changing to reflect their new cell-level responsibilities. Most important is complete integration of the tools used to create and verify the cells. Layout tools must be meshed with simulation tools to speed the iterations of cell layouts needed to balance multiple parameters, such as speed, power, and size. Custom cell design can't slow down the higher-level processes, like synthesis and automatic layout.

Tool integration also extends into system-level design and analysis. With systems implemented largely on dense chips, it's important to use the chip design database for system simulation and analysis. For example, cell characterization data is the basis for chip-wide timing results, which can then be applied quickly and accurately to system-level timing analysis. Integration of the IC tools within the system-level design environment augments the design-cycle reductions of the ASIC techniques.

These custom design capabilities rely heavily on the integrated-circuit design database technology. Specifically, integrating the chip and system tools is a result of object-oriented programming techniques. In this case, the design environment can rely on the database to automatically keep track of library cells, their many views (graphical, physical, and electrical), and instances of where the cells are used within the entire system design.

IC manufacturers still need IC design tools that can deliver the economics required for standard parts, namely small die size for economical manufacturing. At the same time, however, these IC design tools must support some of the characteristics typically associated with ASIC design tools, like high-level synthesis, design reuse, process independence, and a place within the context of systems design. With this capability in place, designers of digital integrated circuits can adopt the techniques that improve both their productivity and their design's competitiveness.

Contributed by Peter Rip, vice president of marketing for the IC Group at Mentor Graphics Corp., Wilsonville, Ore.

neled arrays to improve the performance. First, the sea-of-gates architecture enables macros to be placed closer together, yielding shorter net lengths. Also, the FET currents were cut in half, reducing the power dissipation by a factor of two. Finally, process improvements, including a gate-length reduction from 0.8 μm to 0.6 μm, produced a 30% overall speed improvement.

The architecture consists of a continuous array of core cells surrounded by I/O buffers and pads. Macrocells are placed in columns, with unused columns used for vertical routing tracks. Megacells can span multiple columns, which reduces both area and interconnect capacitance. Clock distribution is accomplished with a fixed clock tree.

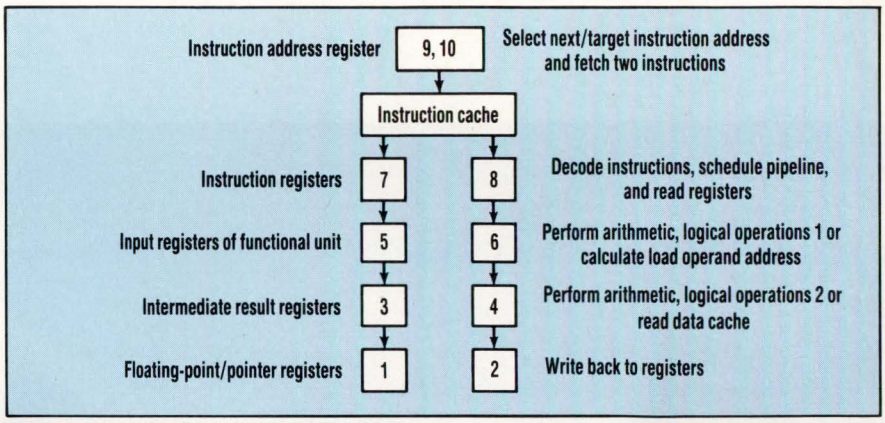
Neural networks are the subject of a paper being presented in the FPGA architecture and applications session. The paper, from the IBM Almaden Research Center, San Jose, Calif., describes Ganglion, the hardware implementation of an interconnected, digital, feed-forward artificial neural net on one VME card. Ganglion, which relies heavily on FPGAs, performs 4.48 billion interconnections/s. The system makes novel use of the reprogrammability of FPGAs to reconfigure and adapt to different problems.

Ganglion designers strove for rapid prototyping and low cost for limited card production. They built most of the system from Xilinx programmable gate arrays. The Xilinx reconfigurable arrays furnished density without the cost and lengthy design cycles of full-custom circuits.

Hidden Layers

The network has one hidden layer. The input layer consists of twelve channels, the hidden layer has fourteen units, and the output layer contains four units. Units of different layers are fully interconnected.

The input layer doesn't do any processing, but simply buffers the input data. Units in the other layers first form a weighted sum of their inputs. Eight-bit unsigned inputs are multipled by 8-bit signed integer weights to produce 16-bit signed products.



2. A FIVE-STAGE PIPELINE helps the Matsushita processor execute two instructions in parallel. Instructions are fetched, loaded, decoded, and executed. The last stage writes back results.

The twelve products and a 16-bit signed, unit-specific bias value are accumulated into a 20-bit result.

Next, the 20-bit sum gets scaled to an 11-bit value. It's then passed through an arbitrary activation function that's implemented as a look-up table in a 2-kbyte PROM, producing each unit's 8-bit output.

British Telecom Research Laboratories, Martlesham Heath, United Kingdom, is also presenting a paper on neural networks. The paper details a CMOS integrated circuit that implements very-large, digital, multilayer perceptron neural networks. A back-propagation algorithm helps with on-chip training, and using pseudo-random noise allows for training with coarsely quantized weight values.

The chip, which is fabricated using a 0.7-μm double-metal CMOS process, measures 9 mm by 11 mm. It has 750,000 transistors and contains eight 20-MHz neural processors. Target performance exceeds 20,000 MIPS for a 1000-neuron network. That type of speed will support complex networks that are trained and used in real-time image- and signal-processing applications.

Pseudo-random noise generators allow for training with reduced word-length weights; a noise component is added to weight-update values during training. Independent, automatic weight ranging and scaling at each neural processor prevents weight saturation.

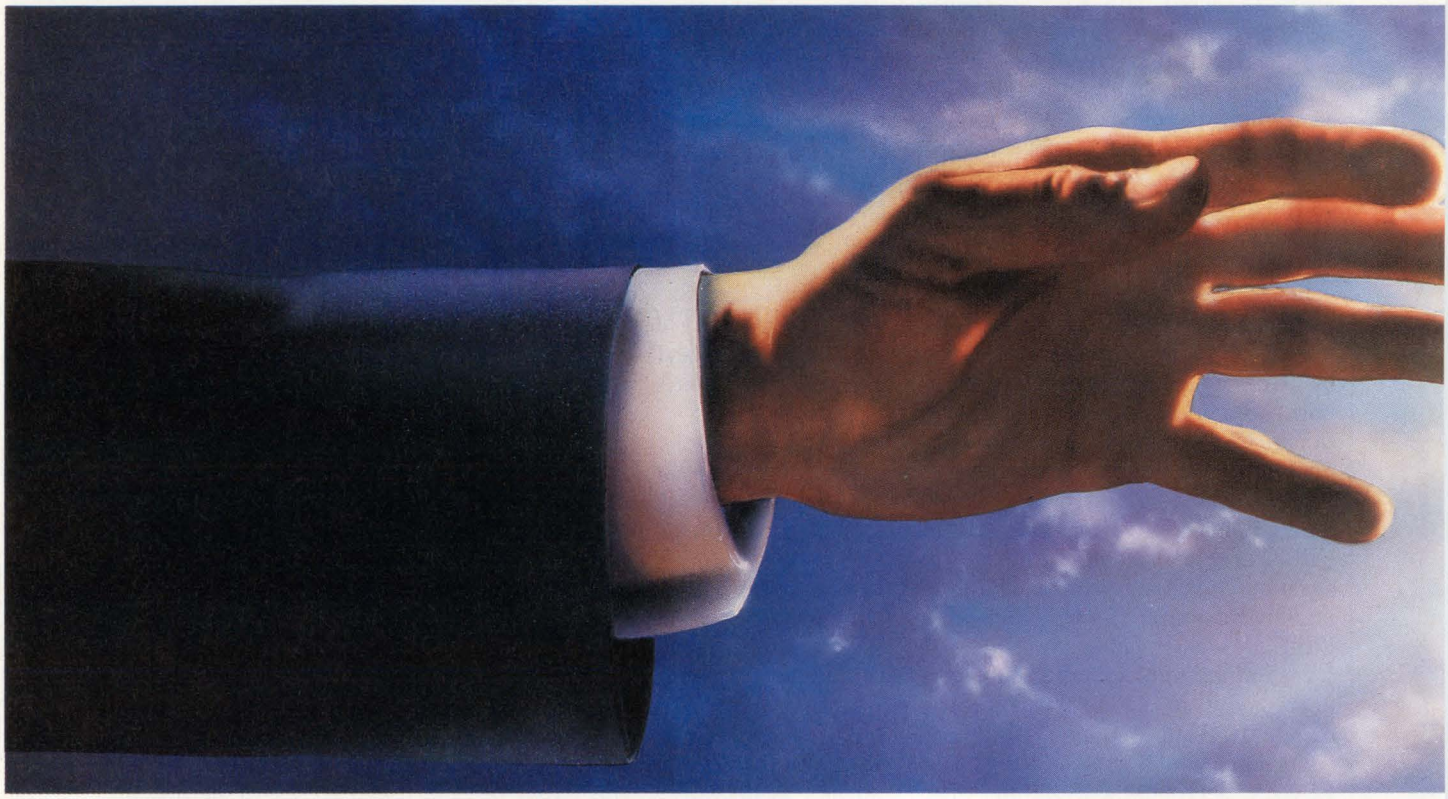
Each of the eight neural processor on the chip have 8 kbits of associated weight storage. The storage can be configured as 512-by-16-bit or 1024-by-8-bit weights. Neural processors can have 8192 connections by selecting different memory blocks. Unused processors on the same chip are bypassed completely. This feature is also used to exclude faulty elements to imrove yield.

The basic structure of the device is a linear array of neural processors that can be cascaded to form large networks. Network configuration and layer boundaries are defined at initialization. Each processor acts autonomously, synchronized by a global clock.

Forward relaxation is achieved by passing the input data serially through the network. When the input arrives at each neuron, it's multiplied by the appropriate connection weight and the result is added to the accumulator. After all the inputs have been presented to each neuron in that layer, the accumulated sum of input-weight products is applied to a sigmoidal, nonlinear activation function to produce the inputs for the network's next layer. This process continues until the final layer is reached. At this point, the values produced are the output values of the net. They are serially clocked out of the network, passing unchanged through any unused neurons.

Real-time image processing is the focus of a paper from Integrated In-

SIEMENS



Global Reach.

Siemens provides an extensive range of reliable advanced semiconductors for companies that manufacture and market worldwide.

For organizations with worldwide marketing and manufacturing interests, it is essential to have a global supplier who is responsive to your needs.

Innovative 8-bit microcontroller designs.

Siemens is that partner, with the worldwide products, services and accessibility which has made us a leader in supplying solutions to organizations with global requirements.

With 197 manufacturing plants in 37 countries, Siemens provides world-class service, support, and manufacturing capabilities. And we back this commitment with over $40 billion in financial strength, as well as quality components, from the most common to the most technologically advanced ICs on the market. Complete with the European content you need to stay competitive in the World Market of 1992.

Temperature and voltage protected power transistors.

Siemens has a reputation for innovative, reliable products spanning a variety of markets. And our latest advancements prove that we're keeping that innovation alive, supplying state-of-the-art solutions which can put the answer to your IC problem within reach.

Siemens offers the most comprehensive communication IC family in the world, which includes innovations such as the industry's first single-chip solution in CMOS for echo cancellation circuit functions in ISDN. And all our

© 1991 Siemens Components, Inc. M11A 012. IOM is a registered trademark of Siemens AG.

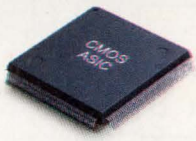
communication ICs feature ISDN Oriented Modular Architecture (IOM®), the de facto industry standard pioneered by Siemens. Providing you with complete IC solutions which ease the incorporation of data, speech and graphics.

High-integration echo cancellation transceiver for ISDN.

We're also the only European DRAM manufacturer, providing high-quality 1-Mb and 4-Mb DRAMs. They're available worldwide and in volumes which have doubled since 1989. In fact, we're becoming one of the world's leading DRAM suppliers, and are continuing to develop advanced DRAM technology with our 16-Mb and 64-Mb DRAM programs.

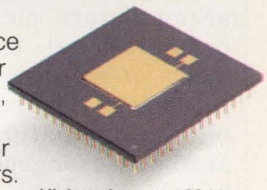
Reliable 1-Mb and 4-Mb DRAMs.

Siemens CMOS ASIC technology features both Sea-of-Gates and standard-cell product families. Our 1.5, 1.0 and sub-micron technologies are compatible with Toshiba even at the GDS2 database level, for true alternate sourcing worldwide. And they're fully supported by our ADVANCAD and industry-standard workstations and simulators, as well as the best service in the industry.



ASIC solutions in both Sea-of-Gates and standard-cells.

Plus, we supply the MIPS RISC microprocessor family, the only 32-bit CMOS microprocessors with five certified sources. Our superior manufacturing processes produce devices with lower power dissipation, and finer performance within your design parameters. And we're the sole European supplier for these devices, which are ideal for workstations, file servers and multiprocessor systems, as well as embedded control applications.



High-performance 32-bit RISC microprocessors.

For details on our world-class products, call **(800) 456-9229**. Or write:

Siemens Components, Inc.
2191 Laurelwood Road
Santa Clara, CA 95054-1514.

Ask for literature package M11A 012.

Siemens
World Wise, Market Smart.

CIRCLE 143

formation Technology, Santa Clara, Calif., which describes a 50-MHz chip called the Vision Processor. It's a microcoded motion video compression and decompression digital-signal-processing (DSP) chip. The Vision Processor is suitable for many consumer and desktop multimedia applications. Every second, the digital processor can perform 8×10^8 16-bit multiply, shift, and accumulate operations; 8×10^8 pixel absolute-difference operations or 4×10^8 16-bit addition-subtraction operations; and 8×10^8 sum-of-difference operations.

Vision Processor's major functional units are three multiported internal register files, parallel reconfigurable ALUs, a motion estimator, parallel MACs, a RISC engine, address generators, and an I/O controller *(Fig. 1)*. External static RAMs are used for microcode reconfigurability. To reduce the number of microcode pins, the code is double-pumped at twice the chip's operating frequency. By changing the microcode, users can easily implement many current and future video-compression standards.

Four parallel 16-by-16-bit multipliers and 24-bit accumulators meet the computational requirements of the discrete cosine transform. The multiplier-accumulators can also be used for general filtering operations, which include rounding and overflow-clamping stages. Multiple shifters perform efficient block floating-point operations.

The 16-bit RISC engine has only eight instructions. These instructions perform many serial operations of the compression algorithms that aren't suited for the parallel structure of the main datapath. The RISC processor can run in parallel with the main datapath.

Also aimed at high-speed computing is an 80-MFLOPS 64-bit microprocessor for parallel-computing applications, which executes two instructions during its 25-ns cycle time, including the combination of 64-bit floating-point add and multiply instructions. The chip, which was developed at the Semiconductor Research Center at Matsushita Electric Industrial Co. Ltd., Osaka, Japan, has five independent execution units.

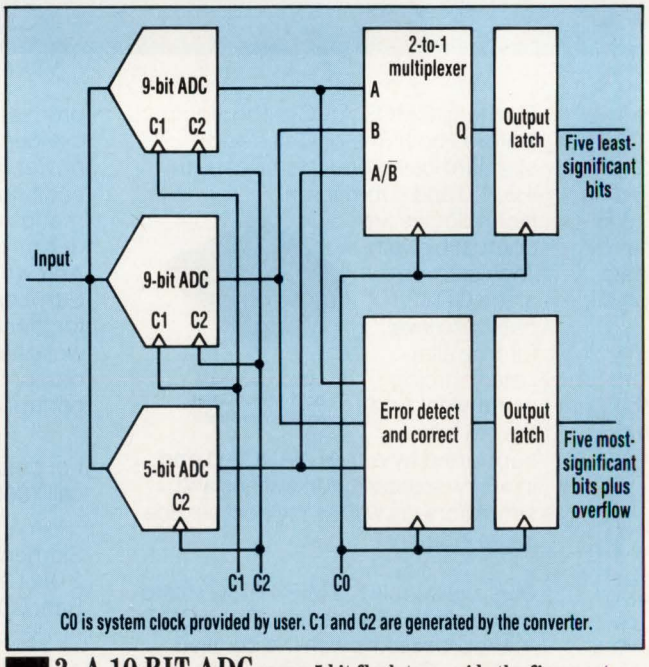
Three factors are largely responsible for the 80-MFLOPS performance. First, the device was built from a two-instruction-parallel type of superscalar architecture that includes a five-stage pipeline. Also, a path-selection structure improves the operation speed of floating-point arithmetic units. Finally, the I/O bottleneck common in these chips was relieved by on-chip data and instruction caches, plus double-size instruction and data ports.

The well-oiled pipeline keeps instructions flowing *(Fig. 2)*. In the first stage of the five-stage pipeline, two instructions are fetched from the instruction cache. They're loaded into two instruction registers of the instruction decoder and pipeline scheduler at the beginning of the second stage. They're then decoded into control signals for the execution units or two register files, floating-point register, and pointer register. In the third and fourth stage, each instruction is executed by one or two of the five execution units. The fifth stage is assigned to write-back operation of the results to register files.

Data Conversion

In a session focusing on data-conversion circuits, a paper jointly written by Vanguard Semiconductor, Milpitas, Calif., and California Micro Devices, Tempe, Ariz., explains a 12-bit video biCMOS track-and-hold amplifier that uses analog calibration. A charge-cancellation circuit combined with feedthrough suppression in a closed-loop architecture results in 12-bit accuracy. For a 4-V full-scale input voltage and 50-Ω output load, the track-and-hold settles to within 1 mV of its final value in 42 ns.

Also in that session, researchers from Tektronix Inc., Beaverton, Ore., describe a 10-bit, 75 Msample/s analog-to-digital converter. The converter uses multiple subranging digitizers to eliminate metastable states and increase sample speed. It measures 4.3 mm by 6.6 mm, and dissipates 2.5 W from a 5-V supply. The device consists of input buffer amplifiers, two 9-bit dual-rank ADCs, a 5-bit flash ADC, error-correction logic, and multiplexing circuitry *(Fig. 3)*. The 9-bit converters use a high-speed, low-gain subranging topology. Two quantizers are offset so that an active region of one converter overlaps a digital-to-analog converter cutpoint zone of the second converter. A multiplexer selects the active converter for a given sample, producing the five least-significant bits of the system. This architecture elimi-



3. A 10-BIT ADC uses a 5-bit flash to provide the five most significant bits of the system. Developed by Tektronix, the converter's flash section also supplies information to the multiplexer to select between two 9-bit converters that supply the five least significant bits. In addition, data from the 9-bit converters is used by logic to detect any possible error in the least-significant bit of the 5-bit first-rank flash, and correct the error.

ATMEL GATE ARRAYS OPEN TO THE PUBLIC

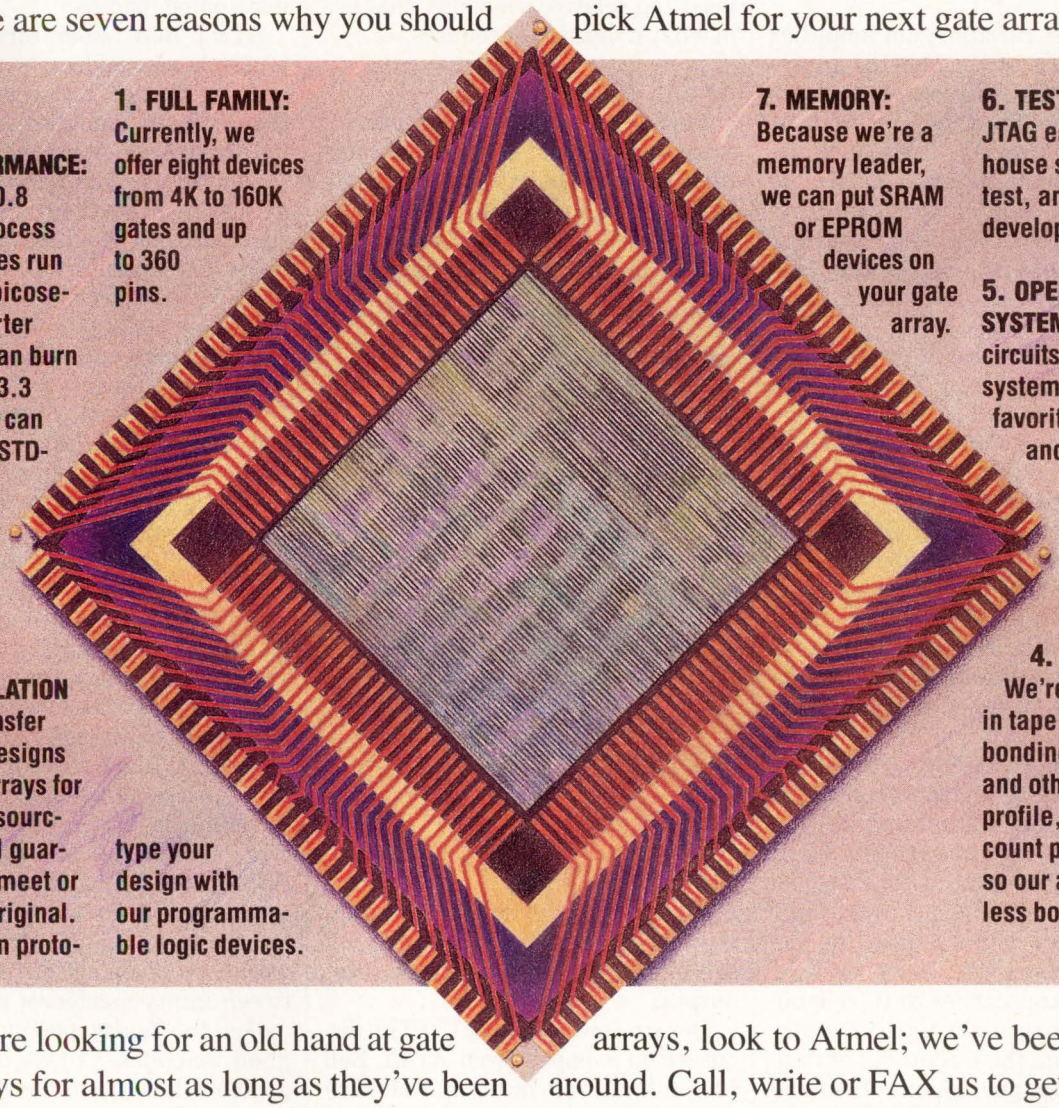
Atmel engineers have been successfully making gate arrays for some of the world's biggest computer makers for more than a decade. That's some 650 different personalizations. Now we are offering our latest generation to the public.

Here are seven reasons why you should pick Atmel for your next gate array.

1. FULL FAMILY: Currently, we offer eight devices from 4K to 160K gates and up to 360 pins.

2. PERFORMANCE: We use a 0.8 micron process so our gates run fast (260 picosecond inverter delays), can burn less fuel (3.3 Volts) and can meet MIL-STD-883C.

3. TRANSLATION EASE: Transfer existing designs into our arrays for alternate sourcing. Atmel guarantees to meet or beat the original. Or, you can prototype your design with our programmable logic devices.



4. PACKAGES: We're a leader in tape automated bonding (TAB) and other low-profile, high-pin-count packages, so our arrays use less board room.

5. OPEN DESIGN SYSTEM: We make circuits, not design systems. Use your favorite hardware and software.

6. TEST PROOF: JTAG eases in-house system test, and cuts test development time.

7. MEMORY: Because we're a memory leader, we can put SRAM or EPROM devices on your gate array.

So, if you're looking for an old hand at gate arrays, look to Atmel; we've been making great arrays for almost as long as they've been around. Call, write or FAX us to get our latest gate array literature.

ATMEL®

The people who make the difference.

ATMEL CORPORATION
2125 O'Nel Drive
San Jose, CA 95131

Tel. 1-800-292-8635
Tel. (408) 441-0311
FAX (408) 436-4200

CIRCLE 98

nates possible metastable states due to DAC switchpoints.

A 5-bit flash converter provides the five most-significant bits of the system. It also provides information used by the multiplexer to select between the two 9-bit converters. Data from those converters is used to detect and correct any error in the least-significant bit of the 5-bit first-rank flash.

A 50-MHz variable-gain amplifier is the subject of a paper being presented by the Integrated Circuits and Systems Lab at the University of Calif., Los Angeles. The CMOS device attains a 30-dB range of variable gain with a 50-MHz bandwidth, requires one 5-V supply, and dissipates 150 mW. Applications for the variable-gain amplifier include disk-drive read channels.

In the analog-circuit applications session, a paper from Texas Instruments, Villeneuve-Loubet, France, summarizes new design techniques and measured performances of a 5-V CMOS line circuit that uses oversampled audio converters and a dc-feed controller. It includes 96-dB DACs and 100-dB ADCs. The ADC is a second-order switched-capacitor delta-sigma modulator sampled at 2.048 MHz. The oversampled DAC is embedded in a switched-capacitor low-pass filter.

The dc-feed controller synthesizes adjustable line characteristics. It sets line battery voltage and feed impedance. A line-interface circuit feeds the controller with a scaled-down line voltage, and converts controller-output voltage into the dc-feed current.

Possible approaches to IC reliability simulation are the topic of another paper from the University of California. This paper, which is from the Electronics Research Lab in Berkeley, uses the Berkeley Reliability Simulation Tool (Bert) to illustrate the issues. Bert considers such factors as hot carriers, oxide time-dependent dielectric breakdown, and electromigration. Additional reliability models for bipolar transistor degradation and ESD protection circuits are being implemented into the simulation tool.

The tool simulates circuit reliability and failure rate with the speed of typical Spice simulations. Consequently, design-for-reliability adds only a small effort to the routine process of design for performance. The reliability models must be simple, yet accurate and general enough to pinpoint major reliability weak spots in a circuit. They must also predict at least the relative reliability changes in what-if design procedures.

Weak Points

Bert can simulate the waveforms after hot-carrier induced degradation; the failure rate due to oxide wear-out, including the effect of any proposed burn-in; the failure rate due to electromigration; or issue a layout advisory if the circuit layout is provided. Weak points in the circuit are highlighted by graphic or print output.

THE BERKELEY RELIABILITY SIMULATION TOOL CONSIDERS SUCH FACTORS AS HOT CARRIERS AND DIELECTRIC BREAKDOWN.

Design-for-testability (DFT) is discussed in a paper from AT&T Bell Laboratories, Princeton, N.J. The testing of mixed-signal devices is a complex problem because very few internal signals are accessible. A potential solution is an analog DFT framework that offers structured access to the analog subsystems in a mixed-signal device, enhances observability and controllability, and simplifies test and diagnosis.

Three analog DFT schemes for testing the analog portion of a mixed-signal device are explained as an example of a framework that meshes analog testing with digital DFT. The schemes are multiplexer-based DFT, analog-bus-based DFT, and scan-path-based DFT. In the analog test mode, the various configurations of multiplexers and switches employed in the three schemes are manipulated by the control signals to test analog macros.

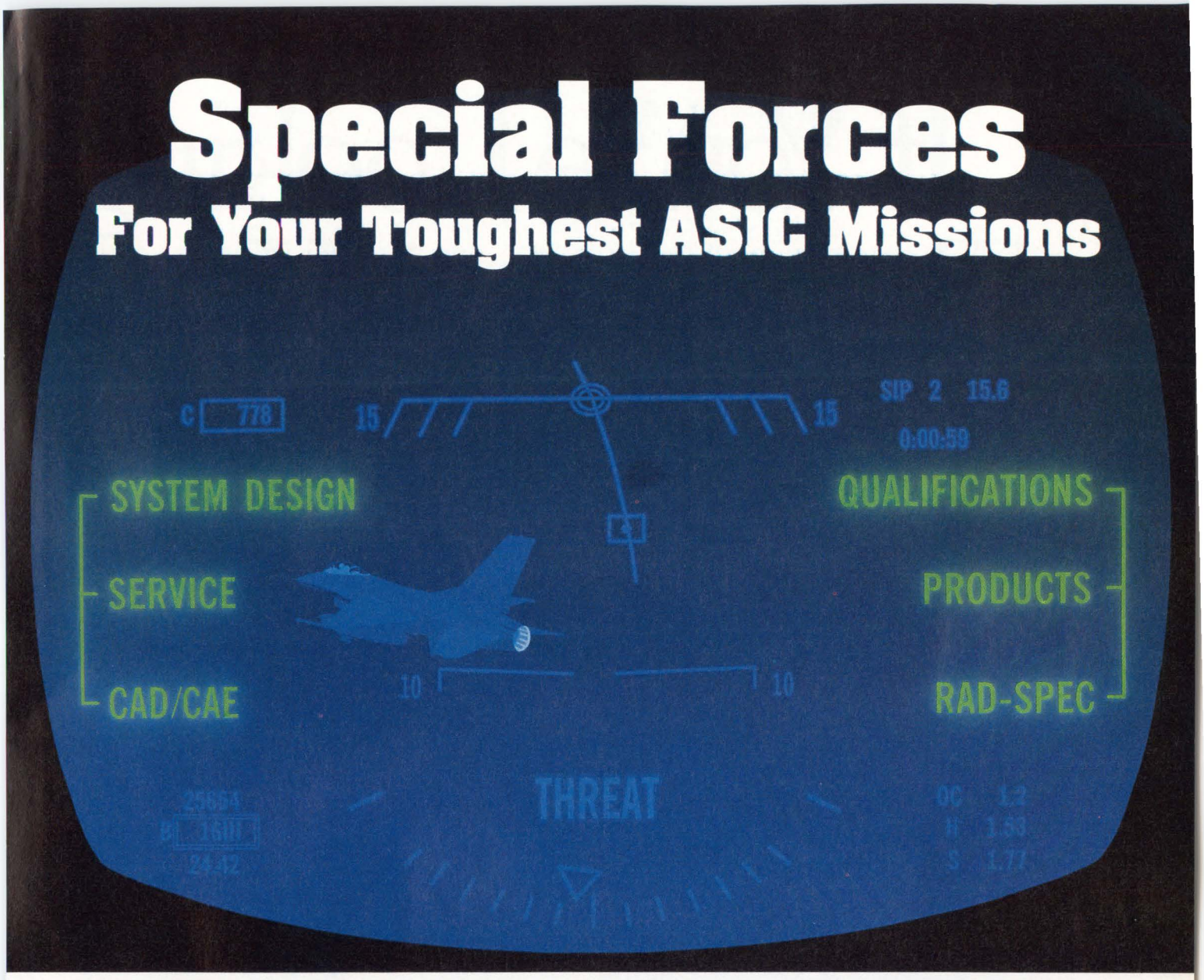
AT&T Bell Laboratories, Princeton, N.J., also addresses test in a paper describing the architecture of the Gentest Sequential Test Generator. Gentest creates test vectors for sequential circuits described at the net-list level, without the need for such testability features as scan. For moderate-size circuits (30k–50k gates), the overhead of such techniques is unacceptable. With Gentest, test generation requires no designer involvement.

There are four major enhancements to the algorithm beyond other test generators. First, the Split data structure reduces the complexity of the choice process by dealing with two 3-value algebras (for the good and fault machine), instead of one 9-value algebra. Also, Gentest's Back algorithm employs a drivability measure that orders outputs and fault-propagation paths to guide the test generator in driving a fault effect to an output. In addition, a set of flip-flop functional-level models handles different clocking regimens. Finally, the Proofs fault-simulation algorithm picks up faults detected as a by-product of the vectors generated for the target fault. The algorithm works by keeping differences between faulty machines, not just between the faulty machine and the good machine. Consequently, the good-machine state doesn't have to be stored, saving a considerable amount of memory. The Proofs algorithm was measured running ten times faster the concurrent fault simulation.□

How Valuable?	Circle
Highly	529
Moderately	530
Slightly	531

Special Forces

For Your Toughest ASIC Missions



Qualifications: From JAN Class B QPL through 883 Levels B and S, UTMC's SystemASICs℠ are qualified for the toughest missions. In fact, our 1.5-micron UTD is the only readily-available JAN QPL gate array and our 1.2-micron UTE-R is available to 883 levels B and S.

Products: With up to 50,000 usable gates and 256 I/Os, SystemASICs are the most capable arrays available. Their tours of duty include the NASA/JPL Mars Observer.

CAD/CAE: Be prepared with SystemASIC toolkits to map out the design, simulation, and verification of your ASICs on Mentor Graphics® and Valid workstations. SystemASIC CAD/CAE helps you evade risks and capture the objective faster.

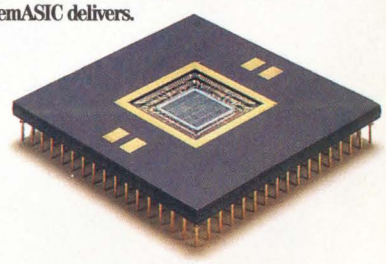
System Design: Our team of veterans helps you sweep through difficult systems design and keep your program on course. Tactical support includes SystemASIC Megafunctions — like RAM, 1553 bus interfaces, and RISC processor.

RAD-SPEC℠: Outflank special screening with RAD-SPEC SystemASICs, guaranteed to meet MIL-M-38510 radiation levels with off-the-shelf pricing and delivery.

Service: SystemASIC deploys your ASICs faster, with less risk. Whatever the challenge — system design, special screening, packaging, or delivery schedule — UTMC's SystemASIC special forces deliver. No wonder that customers like Honeywell and Rockwell have given UTMC special vendor service awards.

The SystemASIC mission: Deliver semicustom solutions for the toughest ASIC assignments. Beyond high-rel, SystemASIC unites products, technology, qualifications, and support geared specifically to meeting aerospace and defense requirements. And SystemASIC means more than products; it means methodologies to get ASICs from concept through production on-time and with minimal risk, and the total commitment of people to see the mission through. Our forces are fully equipped to handle your objective, with a MIL-STD-976 certified facility, in-house radiation testing, environmental screening, and high-pincount packaging and automated testing. SystemASIC products are supported by the latest Mentor and Valid toolkits and qualification through JAN Class S. So call in the SystemASIC special forces. **When the going gets tough, SystemASIC delivers.**

For more information on SystemASICs, call: 1-800-MIL-UTMC
1575 Garden of the Gods Rd.
Colorado Springs, Colorado 80907



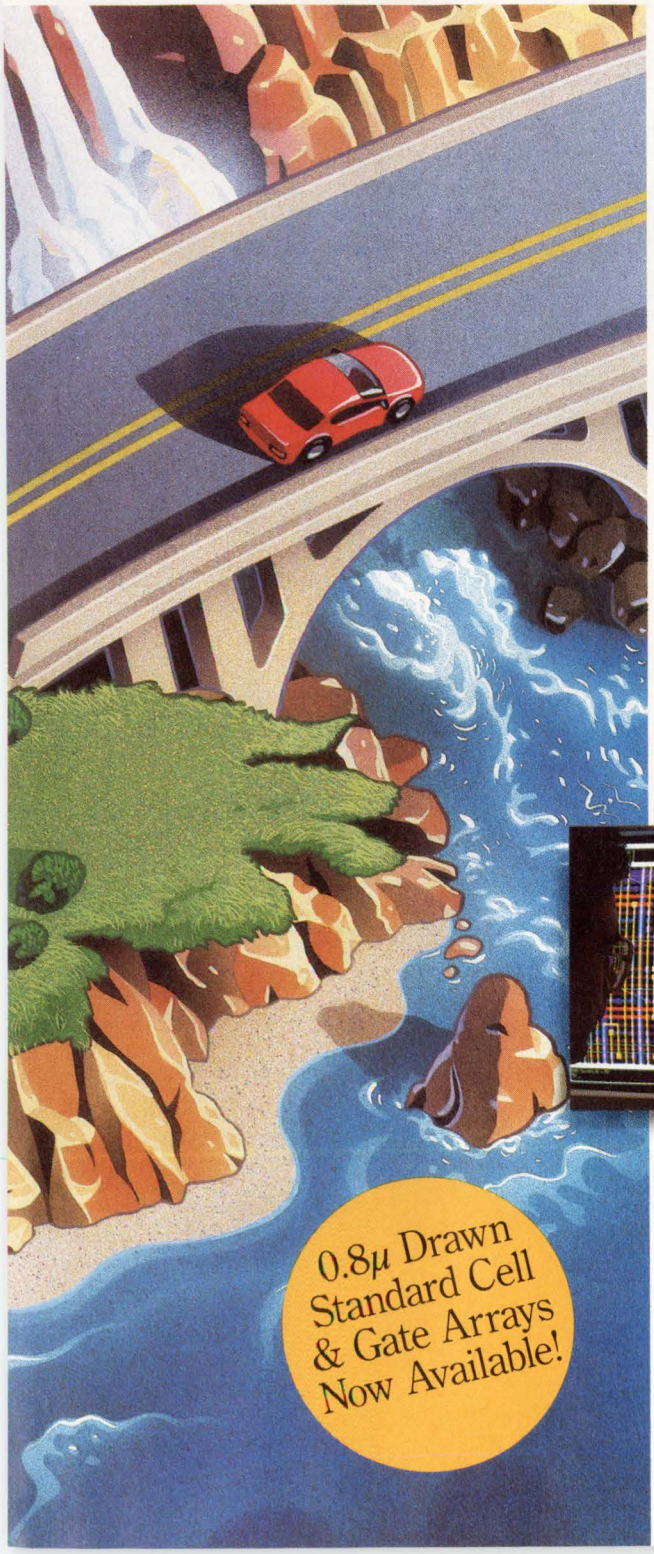
UNITED TECHNOLOGIES MICROELECTRONICS CENTER

DEDICATED TO AEROSPACE AND DEFENSE

CIRCLE 147

If You're Looking Turnaround, Head

For Fast Gate Array Straight For Toshiba.

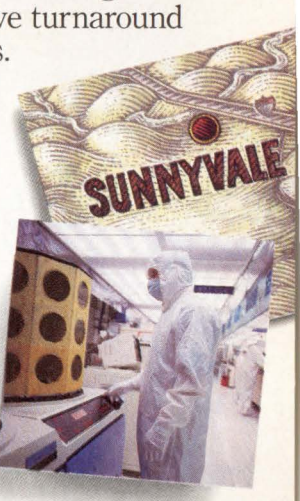


Engineering samples in just 8 working days: How's that for a time-saving shortcut? Now you can tap into Toshiba's advanced CMOS process and enormous ASIC manufacturing capacity and also get one of the most aggressive turnaround times in the business.

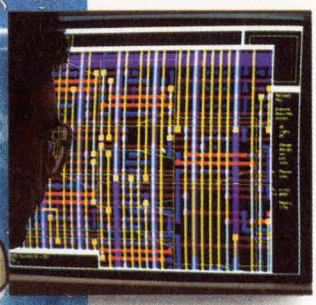
We've geared up our Sunnyvale, CA fab facility to provide accelerated response for both engineering samples and production volumes of high performance gate arrays.

Give us 8 working days and we'll support your aggressive development schedules for up to 68,000 raw gates in high speed, 1.0 micron gate array. Or we will make larger designs of up to 172,000 raw gates in 15 working days.

We can get your project off to a rolling start with the Toshiba Design Environment. It covers the full CAD spectrum and is compatible with the major EWS including AIDA, Cadence, Dazix, HILO, HP, IKOS, Mentor, Synopsys, VALID, Verilog and Viewlogic.*



Local fab line speeds prototyping and supports production volumes, too.



The Toshiba Design Environment supports the major EWS.

No one knows more than Toshiba when it comes to high volume production of high performance ICs. That's why it makes sense to head for our gate array expressway.

There's no faster route to success.

For technical literature, call 1-800-321-1718

Sales Offices: *Deerfield, IL 708-945-1500; Burlington, MA 617-272-4352; Sunnyvale, CA 408-737-9844; Tustin, CA 714-259-0368; Richardson, TX 214-480-0470; Norcross, GA 404-368-0203; Portland, OR 503-629-0818*

In Touch with Tomorrow

TOSHIBA

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

*AIDA, Cadence, Dazix, HILO, HP, IKOS, Mentor, Synopsys, VALID, Verilog and Viewlogic may be registered trademarks by others.

© 1990 Toshiba America Electronic Components, Inc.

MAS-90-035

CIRCLE 156

NOW SHIPPING

Once again, Lattice leads the market with the world's fastest CMOS 22V10. The 10ns, **GAL22V10B-10.** Thanks to our E²CMOS® technology, this GAL® device runs at a cool 90mA typical Icc. And it's 100% tested. When it comes to high performance and high quality, no one can match the Lattice family of leading-edge, E²CMOS GAL devices.

To have a free sample and a GAL Data Book shipped to you, just call **1-800-FASTGAL.** Ask for Department 304.

Lattice®
Semiconductor Corporation

5555 Northeast Moore Court • Hillsboro, Oregon 97124

Leader in E²CMOS PLDs.™

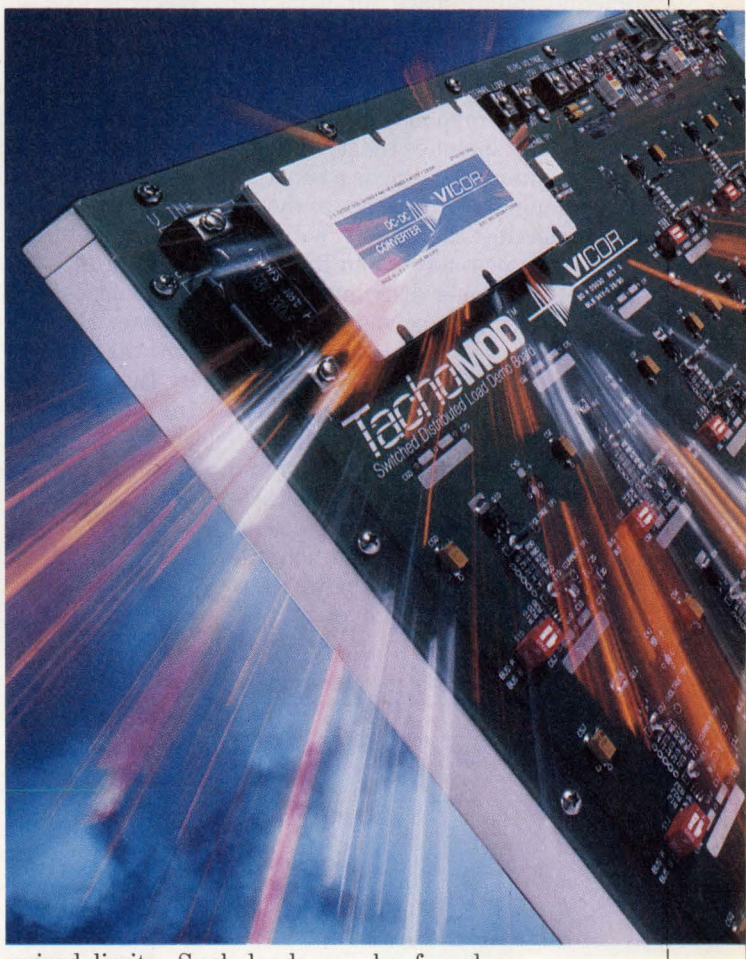
Copyright © 1991, Lattice Semiconductor Corporation. GAL and E²CMOS are registered trademarks of Lattice Semiconductor Corporation.

CIRCLE 157 FOR LITERATURE

POWER MODULE EXILES EFFECTS OF INDUCTANCE AND CAPACITANCE THAT LIE BETWEEN IT AND LOADS CHANGING AT 200 A/μS.

DC-DC CONVERTER HANDLES DISTANT 200-A/μS LOADS

FRANK GOODENOUGH



Most electronic loads require stiff dc-voltage sources, typically regulated to within ±5%. A wide range of power supplies do a fine job meeting that need, as long as the load changes slowly. These supplies also work well for fast transients whose magnitudes represent only a small percentage of the total rated supply current.

But with system-clock speeds climbing beyond 50 MHz, and an increasing number of applications featuring pulsed-load current slew rates that exceed 5 to 100 A/μs, today's power supplies can hardly keep up. Vicor feels it now has an answer to this problem with a newly developed family of modular dc-dc converters called TachoMods. The TachoMods are based on the company's earlier VI-200 family.

The new converters guarantee that during a 10-to-90% load change, at 200 A/μs, the maximum voltage deviation *at the point of load* is less than ±5%. The TachoMods eliminate the effects of parasitic inductances by removing capacitance from the converter's output filter. A patent has been applied for this technique. The more common TachoMod specifications are similar to those of the other VI-200 family members *(see the table)*. Dynamic-response specifications, however, put the TachoMods in a class by themselves.

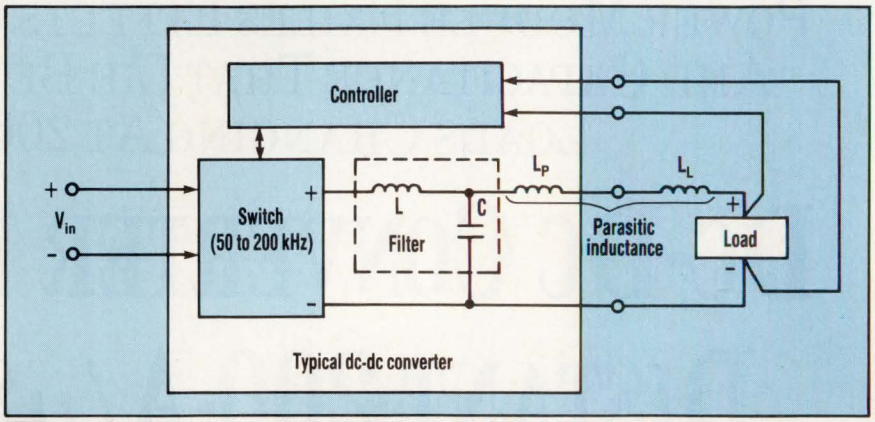
Internal and external parasitic inductances prevent conventional switching power supplies from handling rapidly switching high-current loads. That is, they can't keep the supply rail's voltage—at the load or sometimes at the terminal—even close to the required limits. Such loads can be found on large high-speed computer memory boards containing several hundred CMOS DRAMs; in large, high-resolution video CRT displays; and in radar transmitters and laser drivers. In a conventional supply, only the output capacitor handles fast changes. The feedback loop and its voltage source are left to handle slow changes.

For years, radar systems have needed sup-

200-W 20-A/μS DC-TO-DC CONVERTER MODULE

plies like the TachoMods. It has appeared more recently in systems where high-power lasers are driving optical-fiber transmission lines. And it's just now rearing its ugly head in computers. Though the TachoMod was developed for computer applications, it should be a boon to anyone with a large and fast pulsed load that's located more than a few microinches from the load's voltage rail.

CPU, memory, and related pc boards are contained in one or more racks in traditional computer systems. The power supply, on the other hand, resides in a corner where someone found space for it as the rest of the system was being finished. The dynamic performance of such equipment is truly limited by the transient response of its power system. This includes the power supply's output impedance as a function of frequency, the reactance of the cable connecting the supply with the computer's pc boards, and the reactance of the power-distribution runs on the boards themselves.



1. IN A TYPICAL SWITCHING POWER SUPPLY, parasitic inductance between the internal filter and the load limit the supply's ability to "hold up" the voltage at the load, when the load is exposed to transients of more than a few hundred mA/μs.

PURGE PARASITES

Even now, to reduce the parasitic resistances and reactances typically occurring between the regulator and the pc board, distributed power systems are replacing a single, massive switching regulator. In addition, the transient response of the power supply itself has been improved by raising switching frequencies to over 1 MHz, which in turn can quicken the control-loop's response time. However, even the best distributed-power architectures haven't kept up with the transient-response needs of new and next-generation systems.

Raising switching speeds has made it possible to improve loop response. However, the core issue is now the parasitic inductance created by the converter's output pins and the metal traces between the converter module and the load—high-speed logic or memory devices that often completely cover a 2-ft.-by-2-ft. board.

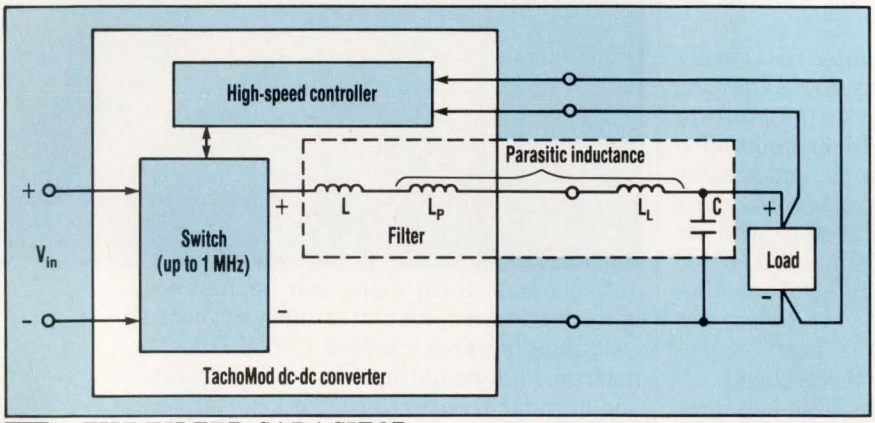
The traditional solution has been to populate the pc board with large numbers of low-ESR (equivalent-series-resistance) capacitors with one or more located at each chip. These capacitors (usually tantalum) are expensive, they take up valuable board space, and don't have a reputation for reliability. Now, with Vicor's TachoMod, a virtually instantaneous load change by a multitude of computer chips is no longer inconsistent with tight voltage regulation at every chip site.

The heart of typical switching power supplies and board-mounted dc-dc converters consists of switching circuitry that delivers pulses of voltage, V_s, to a choke input LC filter *(Fig. 1)*. The supply's breakpoint frequency

$$\frac{1}{2\pi\sqrt{LC}}$$

is set well below the converter's switching frequency. The filter delivers the average value of the pulsating waveform to the load connected across the filter and attenuates the waveform's large, time-varying component, essentially eliminating the ripple from the dc output voltage. The circuit's controller senses the voltage across the load and maintains it at a constant average value, within limits, as the source and load change.

The filter's capacitor also stores energy to minimize output-voltage variation in response to sudden load-current changes. In principle, the peak-voltage change in response to large load-current changes can be controlled by correctly sizing the ca-



2. THE FILTER CAPACITOR in Vicor's TachoMod converter has been removed from inside the converter to the load. The parasitic inductances of the output pins and the board's wiring are lumped with the filter's inductor. The capacitors at the load sites can now keep the voltage within regulation specifications—under 10%-to-90% load transients slewing at 20 A/μs.

pacitor. It's typically not an easy task because parasitic inductance lies between the capacitor and the load. The value of this parasitic inductance depends on the geometry of the connections between the capacitor and the converter's terminals, and the connections between the terminals and the load. Inductance L_p lies inside the converter, inductance L_l outside.

When the load current changes rapidly, a voltage drop equal to the total parasitic inductance, $L_p + L_l$, multiplied by the current's rate of change (Ldi/dt), develops across $L_p + L_l$. Because the voltage across the capacitor can't change instantaneously, the voltage at the load is reduced by the voltage drop across the inductances. That drop can be significant. For example, a di/dt of 20 A/μs produces a 2-V drop across 100 nH. In a 5-V system, that represents a 40% drop in voltage. A more acceptable voltage change of 0.1 V (2%) demands a total parasitic inductance of less than 5 nH, which is less than the inductance produced by a 0.1-in.-diameter loop of wire.

As noted earlier, the traditional technique used to "hold up" the voltage at the load consists of adding massive amounts of "bypass capacitance" across it, as close to the load as possible. This approach may appear to address the problem, but it creates three more. First, increasing the total filter capacitance degrades the response time of the converter. Second, too much capacitance may also cause closed-loop converter instability. Finally, if small amounts of external capacitance are used, a rapid change in load current causes the load voltage to ring. Ringing associated with the circuit loop formed by the external and internal capacitors and the parasitic inductances can be large enough in amplitude (relative to the nominal load voltage) to potentially interfere with system operation or even damage devices.

TachoMod SPECIFICATIONS

(Unless noted otherwise, specifications are at a baseplate temperature of 25°C, nominal line voltage, and 75% load current.)

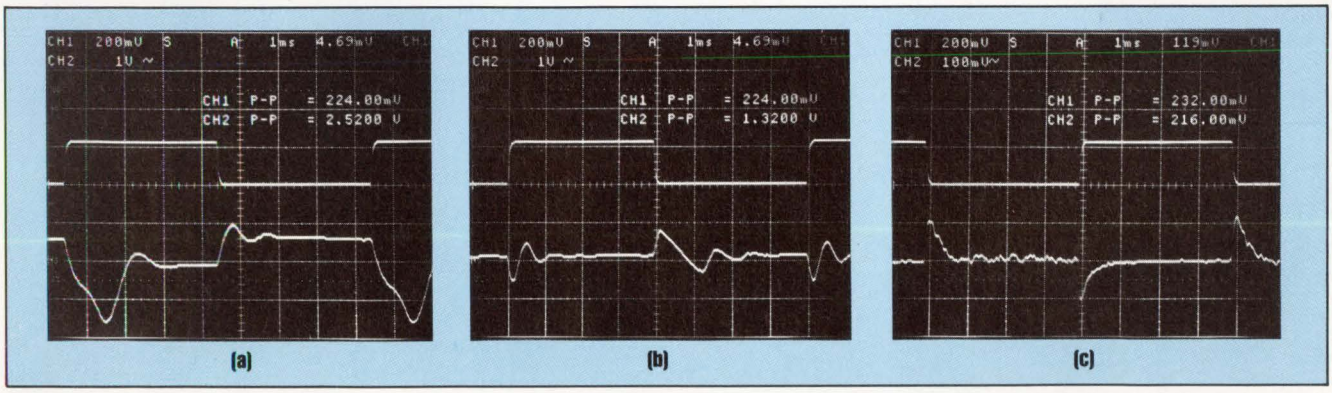
Output set-point accuracy	±1%
Line and load regulation	±0.5% maximum
Drift with temperature	0.02%/°C
Efficiency	80% to 90%
Input isolation to baseplate	3750 V rms minimum
Output isolation to baseplate	500 V rms minimum
No-load dissipation	2 W maximum
Dimensions	4.6 in. × 2.4 in. × 0.5 in.
Operating temperature (baseplate)	0°C to 85°C
Nominal dc input-voltage ranges	12, 24, 36, 48, 150, 300 V
Nominal dc output voltages	2-95 V
Output-power ratings (power rating determines current rating)	50, 75, 100, 150, and 200 W

Inside Outside

Vicor's new proprietary power-distribution architecture, as noted earlier, removes the output capacitor and relies on small amounts of bypass capacitance at one or more load sites *(Fig. 2)*. Now all of the parasitic inductances are, in effect, lumped into the filter's inductance (of which they represent only a small part), and they actually perform some of the filtering. Because the current flow's rate of change is no longer limited in the parasitic inductances, external capacitance at the load can be charged rapidly.

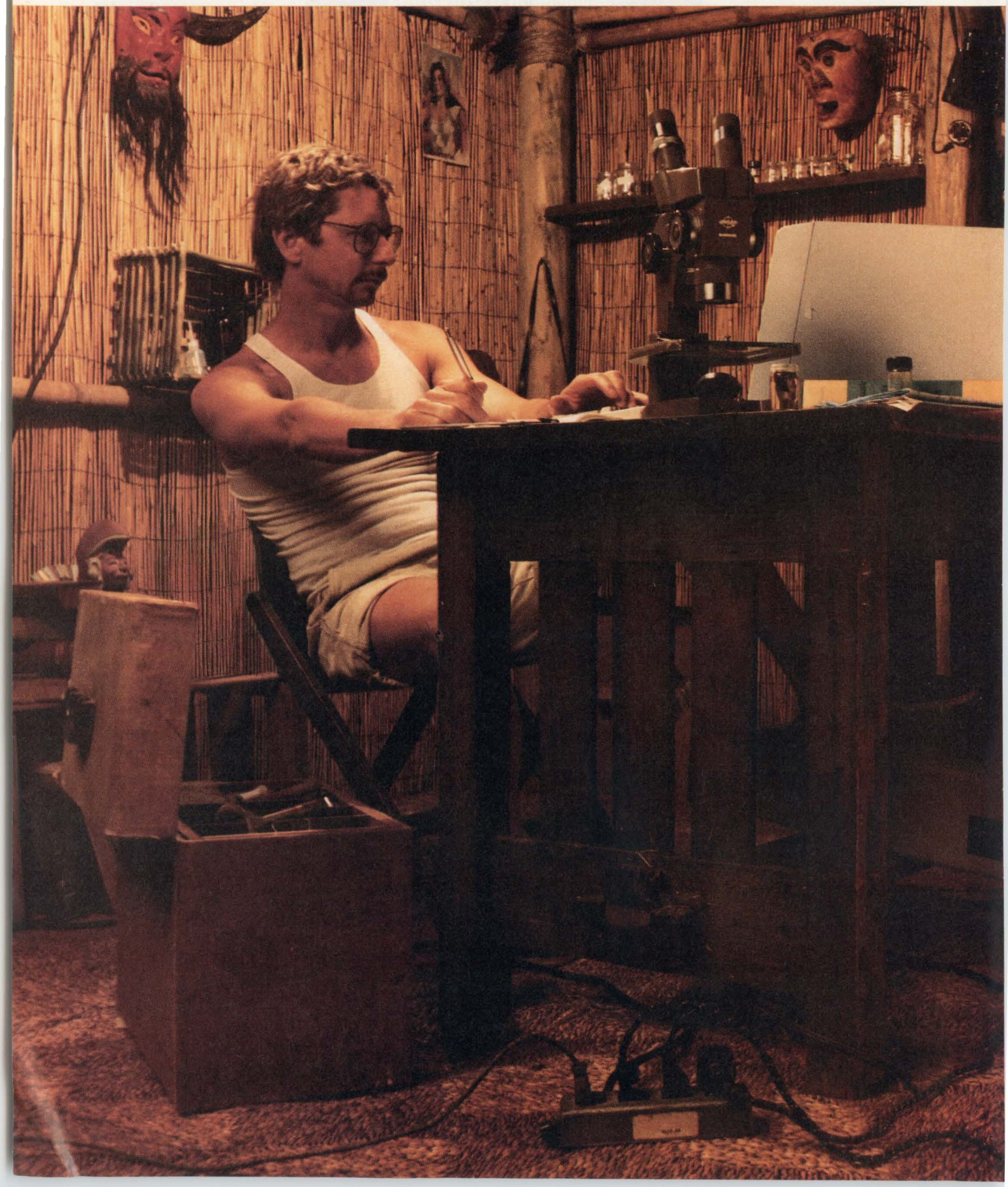
The value of the external capacitance need only be enough to eliminate the ripple and limit the maximum output-voltage deviation associated with worst-case load changes. In most computer-logic, or memory-board, applications, the new converters can rely on the energy stored in the distributed capacitors found on the boards. A static load current of 10 to 100 μF/A represents a good rule of thumb for estimating capacitor size.

A number of examples can illustrate the savings in capacitor usage offered by these converters. A typical 100-W, pulse-width-modulator design operating at 50 kHz is one such example. The following additional assumptions should be made: The converter has an output voltage of 5 V, a filter inductor of 50 μH, and the output must be kept within 0.2 V (4%), for a 20-A instantaneous step-current change. About 10,000 μF of capacitance would be needed to "hold up" the voltage. The minimum output would occur about 200 μs after the current step. That much capacitance would reduce the converter's first breakpoint frequency to

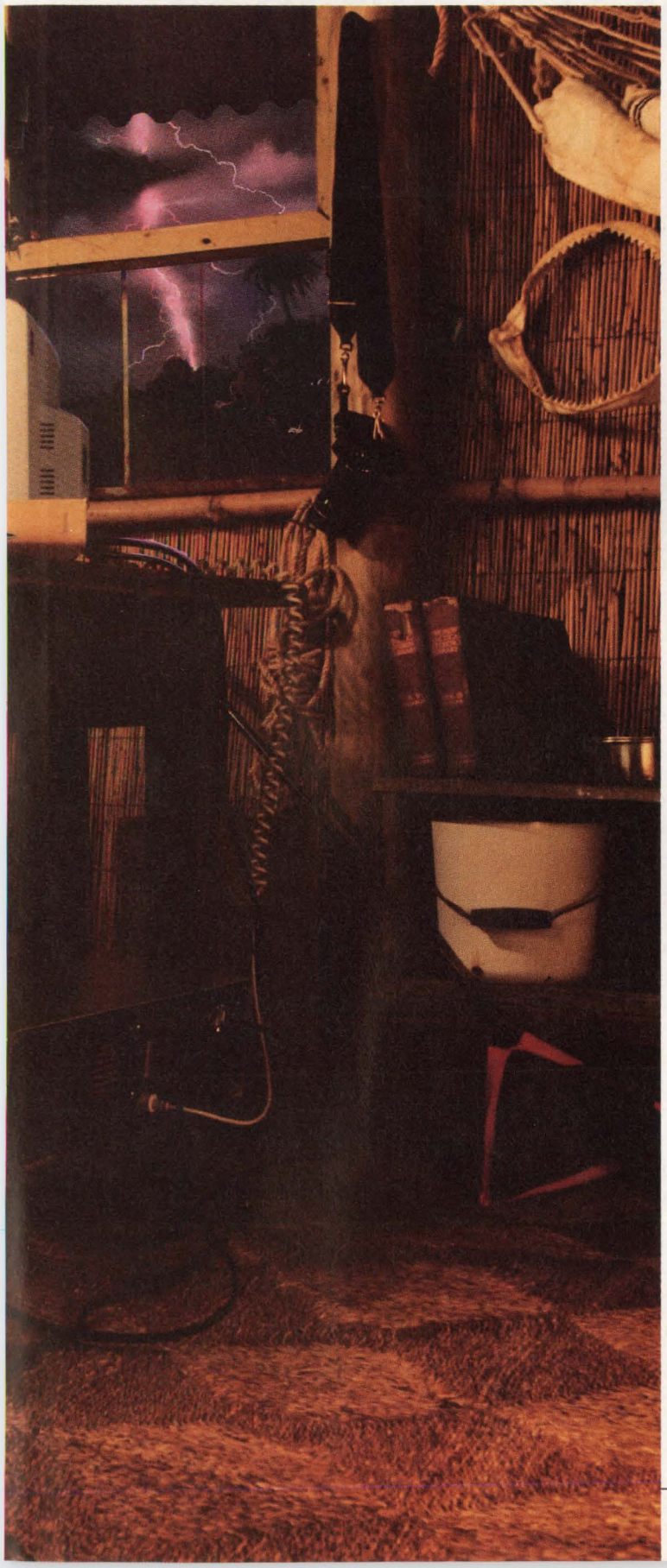


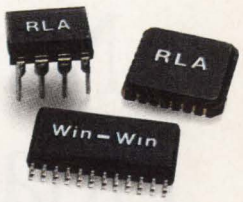
3. WHEN SUBJECTED TO 3-TO-27-A load changes slewing at 20 A/μs (the top waveform in figures a through c), a bench supply's output changed 50% and took 2.8 ms to settle (a, bottom), and a fast-response module's output changed 26% and took 3.2 ms to settle (b, bottom). The TachoMod's output, on the other hand, changed just over 4%, settling in 0.8 ms (c, bottom). Note the change of scale in the bottom waveform of (c).

From Outer Space to Your Place,



We're Your Best Defense.





By putting our military experience to work in high-volume, low-cost applications, we're giving new meaning to the term *National Defense*. Our Power Supply Supervisory Chips are a good example.

These Raytheon Linear Arrays *(RLAs)* act as a computer's early warning system. They monitor internal voltage levels to 0.3% accuracy—and signal a shut down before power surges can fry the system.

It's "Defense Technology" with a peaceful purpose. And it's helping take computers into places they've never been.

Our RLAs have business benefits, too. If you can't decide between a custom or semicustom device, don't. Our *Win-Win* program lets you get to market quickly with a semicustom array, then shift to full custom as sales increase.

Win-Win is fast, flexible, and makes good business sense because it eliminates the risk of getting into a full custom array before you're really ready.

Raytheon is committed to analog technology. From our design kits and engineering support to our fab and plastic assembly facility. We have the experience it takes to help you develop creative, cost effective solutions.

Find out how. Call **1-800-722-7074** for our new analog brochure.

Raytheon Company, Semiconductor Division.
350 Ellis St. Mountain View, CA 94039.

CIRCLE 152

Raytheon

Where quality starts with fundamentals

National Semiconductor

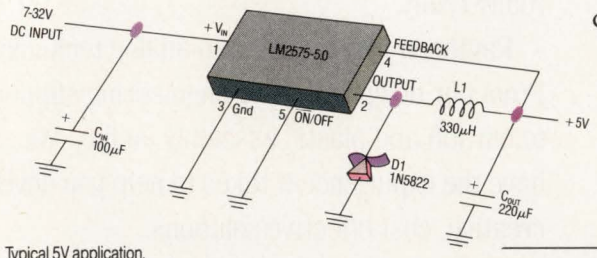
National's Simple Switcher.™ Finally, simple means just that.

THE LM2575/LM2577 FAMILY OF SWITCHING REGULATORS. EASY TO USE, AND JUST AS EASY TO PAY FOR.

No matter how you're doing it now, our Simple Switchers will change the way you use regulators.

No more losing valuable design time to tedious inductor selection. No more parting with precious board space to accommodate as many as 10 extra components. And no more expensive DC-to-DC converters.

Instead, we offer our monolithic LM2575 step-down (buck) and LM2577 step-up (boost) regulator families, in 5V, 12V, 15V and adjustable versions. They're a lot easier to use than a traditional switching regulator, and cost about one-fifth as much as a DC-to-DC converter.



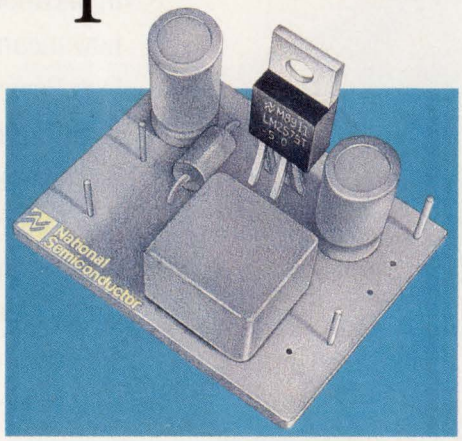
Typical 5V application.

Now you can save design time, board space *and* money.

MINIMUM DESIGN EFFORT.

Designing a reliable, efficient, power supply used to be complex and tedious. No more. Our LM2575 Simple Switcher requires only four external components—

Simple Switcher is a trademark of National Semiconductor Corporation. ©1990 National Semiconductor Corporation.



National's LM2575 Simple Switcher requires just four external components.

an inductor, a diode, and two capacitors—and selecting them is a breeze.

Take the inductor: We provide a nomograph right in the datasheet, along with tables associating inductor codes with their corresponding values and manufacturers. You simply look up the inductor value required by your application. Then you can purchase the inductor (as well as the capacitors and the diode) right off the shelf. And you put them to work with a simple, three-step design process.

MAXIMUM SYSTEM PERFORMANCE.

There's nothing commonplace about the Simple Switcher's performance. For example, the LM2575T-5.0 features a 5V output capable of driving a 1A load with impressive line and load characteristics. Operating at 82% efficiency (compared to 40-50% for a linear regulator), it will help your system consume less power.

And you won't have to sacrifice the quality and reliability you've come to expect from a National three-terminal regulator: current limit, thermal shutdown and a guaranteed system output voltage tolerance (±3%). If you're looking for MIL-STD-883B Rev. C-compliant devices, we offer the LM1575 and LM1577, scheduled for qualification later this year.

ONE SIMPLE PHONE CALL.

This is a power solution that won't try your patience or test your budget. If you'd like to know more, give us a call. We'll even send you a complete Simple Switcher design aid kit, with an optional PC-DOS-compatible design diskette. In the U.S., call **1-800-624-9613, Ext. 25.** In Canada, call **1-800-548-4529, Ext. 25.** Or write us at **National Semiconductor, P.O. Box 7643, Mount Prospect, Illinois, 60056-7643.**

PART	APPLICATIONS	SWITCH CURRENT	PACKAGES
LM2575-5.0	STEP-DOWN	1A	K,T
LM2575-12	STEP-DOWN	1A	K,T
LM2575-15	STEP-DOWN	1A	K,T
LM2575-ADJ	STEP-DOWN	1A	K,T
LM2577-12	STEP-UP, FLYBACK, FORWARD CONVERTER	3A	K,T
LM2577-15	STEP-UP, FLYBACK, FORWARD CONVERTER	3A	K,T
LM2577-ADJ	STEP-UP, FLYBACK, FORWARD CONVERTER	3A	K,T

The Simple Switcher family. K=TO-3 T=TO-220

We can't make it any simpler.

National Semiconductor

225 Hz. Maximum rate of current change through the inductor would be a mere 0.1 A/μs.

By moving to a zero-current switching converter (such as a standard VI-200 module) running at about 1 MHz, the inductor drops (by a factor of 25) to 2 μH and the capacitor (by a factor of 5) to 2000 μF. For a similar step-sized load change, the maximum voltage deviation would occur within 8 μs of the change, the first breakpoint is at 2.5 kHz, and the current can slew at 2.5 A/μs. Finally, by moving to a TachoMod also switching at 1 MHz and still employing 2000 μF of capacitance (but at the load), the maximum deviation runs a mere 0.005 V (0.1%) and occurs in a quick 1 μs. That's about the settling time expected from a pretty good IC op amp for a modest 10-mA output-current change *(for a detailed analysis of these converter architectures and their calculations, ask Vicor for a copy of "Beyond Distributed Power" by Jay Prager, their vice president of system engineering).*

The Real World

These calculations are theoretical approximations. Translating these calculations into a pc board filled with, say, 200 CMOS DRAMs, using a TachoMod can eliminate the need for nearly 100 tantalum capacitors. Translated into dollars, eliminating the capacitors can drop the board's power-system cost from about $1.00 a watt to about 75 cents a watt. That doesn't take into account the value of the space saved, which, of course, can be used to hold more ICs. As noted earlier, the low-ESR tantalum capacitors don't have a reputation for reliability. When they fail, they usually short out, putting a heavy strain on the power module while shutting down the system. The VI-200 series modules, on the other hand, have demonstrated in-the-field mean-time-between-failures of a million hours.

So now you have the world's fastest-settling power converter—how do you prove it to yourself, or to potential customers? It becomes a particularly difficult task for distributed load applications, such as logic and memory boards. Here's the proof: To build a "convincer," Vicor's senior application engineer, Charles Skoolicas, loaded a multilayer pc board, 12-in. wide by 18-in. long, with 21 power MOSFET "cells,"

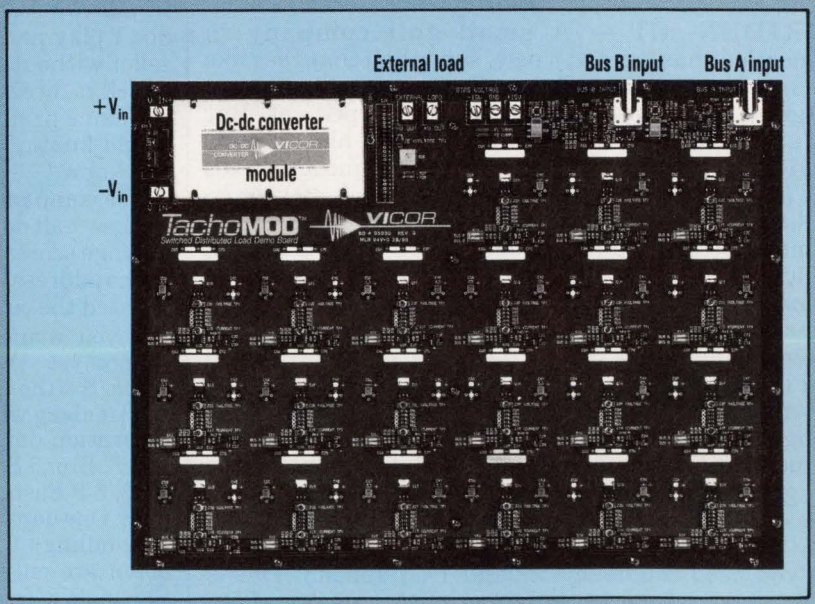
THE CONVINCER

To demonstrate and test their fast-responding TachoMod dc-dc converters, Vicor designed a special-purpose analog computer. Essentially a simulator, this continuously variable, high-speed, dynamic distributed load is built on a 2-ft.^{2} multilayer pc board. It consists of 21 programmable cells and a socket for a VI-200 family converter module. Each cell consists of an IRFR110 power MOSFET rated at 100 V and 5 A, programming circuitry to drive the FET's gate, and current-sensing circuits. Hooked to a supply, the simulator board's loads change at rates of up to 420 A/μs.

A VI-200 series module (original or TachoMod) is plugged into the socket in the upper left-hand corner and a dc-voltage source is applied to terminals on its left. Because the converter's basic specification is for a 10%-to-90% load change, a 10% dc preload (a resistor) is added externally at terminals on the top edge. The preload will vary with the output-current and voltage ratings of the particular module being tested.

Pulse generators are connected to bus A and/or B (top right-hand corner). The amplitude of the generator waveforms applied to the MOSFET gates represents the set point of a feedback loop that controls the current's magnitude through each FET at between 0 and 5 A. The current waveform duplicates the gate-voltage waveform. DIP switches at each cell select a drive signal from bus A, bus B, both, or neither. Consequently, each cell's current can be set from 0 to 5 A. By selecting from 0 to 21 cells, up to 105-A pulsed, or 27-A steady state, can be programmed.

This board isn't a one-of-a-kind marketing tool. It will be put into customers' hands, for module evaluation, incoming inspection, and test. Provisions have been made on the board for adding capacitors that represent those found in specific applications.



200-W 20-A/μS DC-TO-DC CONVERTER MODULE

leaving just enough room to plug in a Vicor module. Each cell is a programmable, 0-to-5-A load. The complete board can provide pulsed dynamic load changes up to a maximum of 125 A at over 400 A/μs. *(see "The convincer," p. 65).*

To demonstrate the TachoMod's dynamic capability, the board was used to compare the performance of a typical switching bench supply and a standard VI-230-CV module (48-V dc input, 5-V output, at 150 W and 30 A) with a similarly rated TachoMod (VI-230-CV-TM). In each of three cases *(Figs. 3a, 3b, and 3c)*, the load was changed from 3 to 27 A at 20 A/μs, which is the top waveform in each figure. All of the voltage waveforms were taken at the cell in the lower right-hand corner of the board (as far away as possible from the supply terminals).

The bench supply was connected to the board's preload terminals with about a foot of wire. Its output changed 2.5 V pk-pk, and took 2.8 ms to settle back to 5 V. The standard Vicor module changed 1.32 V pk-pk and settled in 3.2 ms. The TachoMod's output varied a mere 216 mV (note change of vertical scale), or about 4.3%, and it settled in 0.8 ms.

SPECIFICATIONS

TachoMOD specifications need a little comment. TachoMODs are available with virtually any standard dc output voltage (2, 3.3, 5, 12, 15, 24, 28, 48 V); other outputs are available on request. Input-voltage ranges are specified with three numbers: the input dc voltage representing the minimum expected ac-line voltage, the dc voltage representing the nominal ac-line voltage, and the dc voltage representing the maximum expected ac-line voltage. For example, modules specified for a nominal 12-V input are rated with inputs between 10 and 20 V. Two types of 24-V input modules are available, those that meet their specifications from 21 to 32 V and those that can handle 18 to 36 V at the input. The 48-V-input modules for telecomunications are similar; one class handles 42-to-60-V inputs, the other handles 36 to 76 V. At the high-voltage end, modules running off the rectified 115- and 220-V ac lines produce 100 to 200 V and 200 to 400 V, respectively.□

PRICE AND AVAILABILTY

Pricing for the TachoMod modules, in quantities of 1000, ranges from $90 each to $150 each, depending on power rating. Small quantities are available from stock.

Vicor Corp., 23 Frontage Rd., Andover, MA 01810; Renee Catalano Lucas, (508) 470-2900. CIRCLE 514

HOW VALUABLE?	CIRCLE
HIGHLY	532
MODERATELY	533
SLIGHTLY	534

Advertisement

Small Company's New Golf Ball Flies Too Far; Could Obsolete Many Golf Courses

Pro Hits 400-Yard Tee Shots During Test Round

Want To Shoot An Eagle or Two?

By Mike Henson

MERIDEN, CT — A small golf company in Connecticut has created a new, super ball that flies like a U-2, putts with the steady roll of a cue ball and bites the green on approach shots like a dropped cat. But don't look for it on weekend TV. Long-hitting pros could make a joke out of some of golf's finest courses with it. One pro who tested the ball drove it *400 yards,* reaching the green on all but the longest par-fours. Scientific tests by an independent lab using a hitting machine prove the ball out-distances major brands dramatically.

The ball's extraordinary distance comes partly from a revolutionary new dimple design that keeps the ball aloft longer. But there's also a secret change in the core that makes it rise faster off the clubhead. Another change reduces air drag. The result is a ball that gains altitude quickly, then sails like a glider. None of the changes is noticeable in the ball itself.

Despite this extraordinary performance the company has a problem. A spokesman put it this way: "In golf you need endorsements and TV publicity. This is what gets you in the pro shops and stores where 95% of all golf products are sold. Unless the pros use your ball on TV, you're virtually locked out of these outlets. TV advertising is too expensive to buy on your own, at least for us.

"Now, you've seen how far this ball can fly. Can you imagine a pro using it on TV and eagle-ing par-fours? It would turn the course into a par-three, and real men don't play par-three's. This new fly-power forces us to sell it without relying on pros or pro-shops. One way is to sell it direct from our plant. That way we can keep the name printed on the ball a secret that only a buyer would know. There's more to golf than tournaments, you know."

The company guarantees a golfer a prompt refund if the new ball doesn't cut five to ten strokes off his or her average score. Simply return the balls — new or used — to the address below. "No one else would dare do that," boasted the company's director.

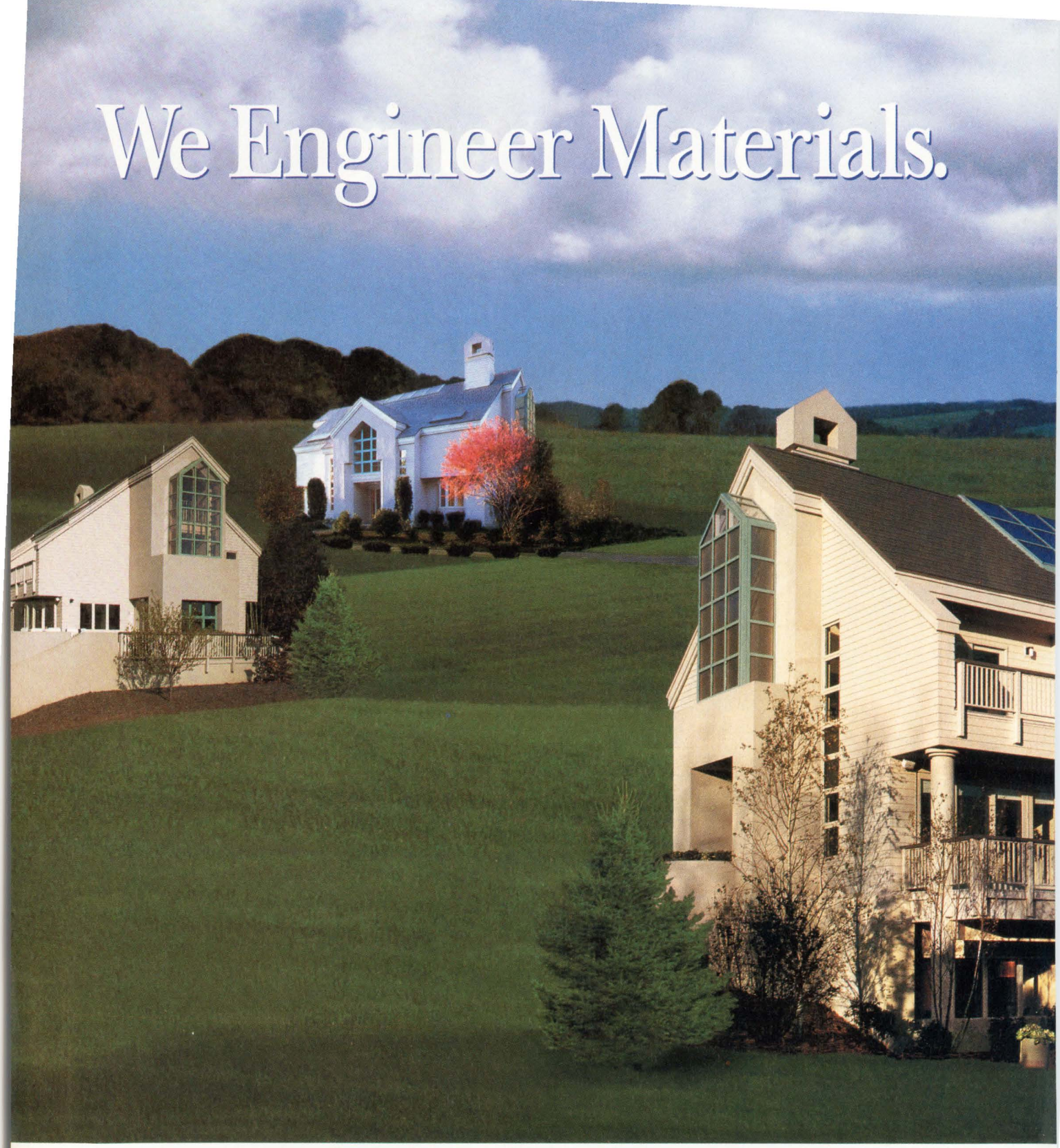
If you would like an eagle or two, here's your best chance yet. Write your name and address and "Code Name S" (the ball's R&D name) on a piece of paper and send it along with a check (or your credit card number and expiration date) to National Golf Center (Dept. S-58), 500 S. Broad St., Meriden, CT 06450. Or phone 203-238-2712, 8-8 Eastern time. No P.O. boxes, all shipments are UPS. One dozen "S" balls cost $24.95 (plus $3.00 shipping & handling), two to five dozen are only $22.00 each, six dozen are only $109.00. You save $55.70 ordering six. Shipping is free on two or more dozen. Specify white or Hi-Vision yellow.

© Bost Enterprises, Inc. 1991

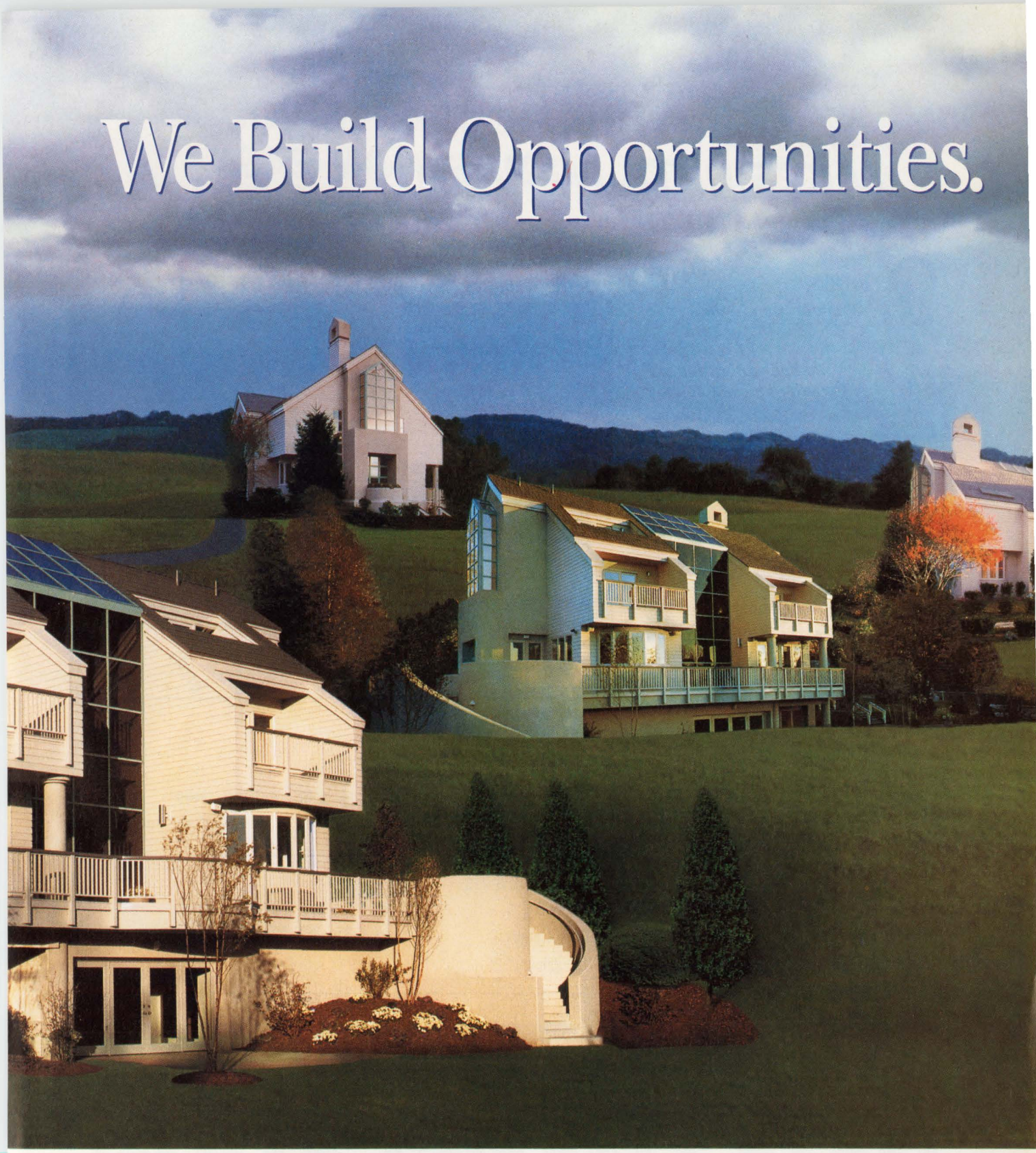
Power House.

A Living Commitment
To Construction Technologies.

We Engineer Materials.



GE Plastics' Living Environments concept house is open for business. Exploring exciting new directions in Building & Construction and a spectrum of related industries—Appliances, Electronics, Lighting, Plumbing, Heating—with more than 50 partner companies. Driving productivity with advanced materials and systems. Creating tomorrow's more efficient, affordable homes. An unprecedented commitment of technology and resources— only from GE.



For a House Tour Brochure and more information on the Living Environments program, call **(800) 845-0600.**

GE Plastics

CIRCLE 106

SOFTWARE CONFIGURABLE BOARD MAKES DATA ACQUISITION EASY

"With our 'Hands-Off' DT2831 board series for the PC AT, all set up and calibration is automatic via software."

–Fred Molinari, President

Total software control–No pots! No jumpers!
- Configuration of all board functions
- Self-calibration
- Gain and offset correction
- Independent selection of gains, sampling rates, DMA channels, and interrupts

Up to 250kHz gap-free data transfer

Simultaneous A/D, D/A

Up to 256 input channels with expansion panel

Two 16-bit counter/timers (AM9513)

Eight lines of digital I/O

Maximum noise immunity with shielded connector and analog modules

FREE software
- Drivers and subroutine library
- C, Pascal, BASIC and FORTRAN support

Application software available
- GLOBAL LAB™ *Data Acquisition*
- Leading software packages including LABTECH NOTEBOOK

Quantity pricing available

FAST 5 day delivery

HIGH PERFORMANCE FEATURES

	DT2831	DT2835	DT2831-G	DT2836	DT2837
ANALOG INPUTS					
Channels	16	16	16	16	16
Resolution (bits)	12	12	12	16	16
Sampling Rate	50kHz	50kHz	250kHz	30kHz	30kHz
Gain	1,2,4,8	1,10,100,500	1,2,4,8	1,2,4,8	1,10,100,500
ANALOG OUTPUTS					
Channels	2	2	2	2	2
Resolution (bits)	12	12	12	16	16
Throughput	130kHz	130kHz	130kHz	100kHz	100kHz

Call for FREE Catalog

(508) 481-3700

In Canada, call (800) 268-0427

DATA TRANSLATION®

World Headquarters: Data Translation, Inc., 100 Locke Drive, Marlboro, MA 01752-1192 USA, (508) 481-3700, Fax (508) 481-8620, Tlx 951646
United Kingdom Headquarters: Data Translation Ltd., The Mulberry Business Park, Wokingham, Berkshire RG11 2QJ, U.K., (734) 793838, Fax (734) 776670, Tlx 94011914
Germany Headquarters: Data Translation GmbH, Im Weileren 10, 7120 Bietigheim-Bissingen, Germany 7142-54025, Fax 7142-64042
International Sales Offices: Australia (2) 699-8300; Belgium (2) 466-8199; Brazil 11 240-0598; Canada (416) 625-1907; China (1) 513-7766 x1222; Denmark 2 274511; Finland (0) 3511800; France (1) 69077802; Greece (1) 361-4300; Hong Kong (5) 448963; India (22) 23-1040; Israel 52-545685; Italy (2) 82470.1; Japan (3) 502-5550, (3) 5379-1971; Korea (2) 718-9521; Netherlands (70) 399-6360; New Zealand (9) 415-8362; Norway (2) 53 12 50; Poland (22) 580701; Portugal 1-7934834; Singapore 338-1300; South Africa (12) 803-7680; Spain (1) 555-8112; Sweden (8) 761 78 20; Switzerland (1) 723-1410; Taiwan (2) 3039836

GLOBAL LAB and **(HSI)***Color* are trademarks and Data Translation is a registered trademark of Data Translation, Inc. All other trademarks and registered trademarks are the property of their respective holders.

CIRCLE 112

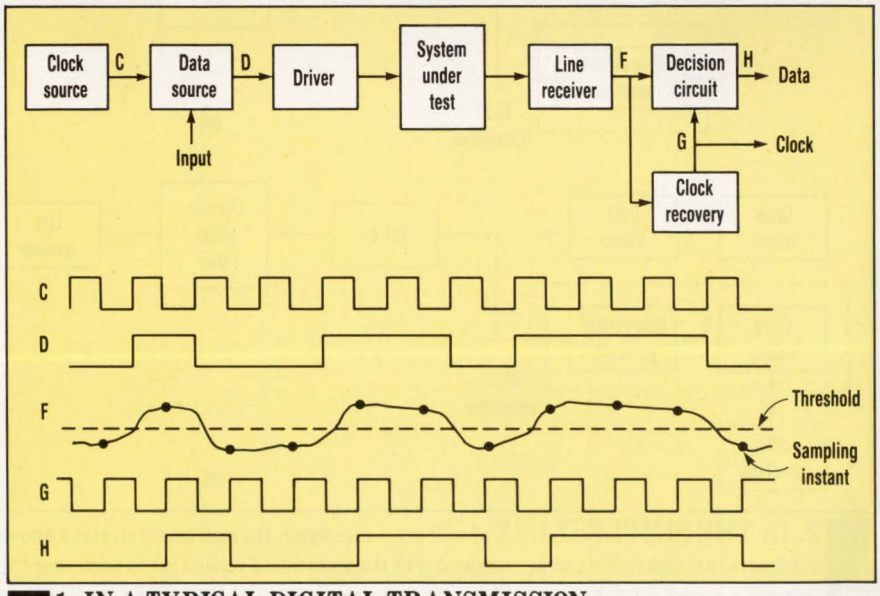
ENSURE THE ACCURACY OF BIT-ERROR-RATE TESTS

TO PROPERLY EVALUATE DIGITAL TRANSMISSION SYSTEMS, USERS MUST UNDERSTAND THEIR BER TESTER'S SPECIFICATIONS.

A critical element in a digital transmission system is how error-free its transmissions are. This measurement is made by a bit-error-rate tester (BERT), which replaces one or more of the system's components during a test transmission. A BERT must be able to mimic normal and stress conditions and must not be the first component to fail when the system is stressed. Moreover, a BERT's data pattern and clock quality typically differ from those of the system under test. Consequently, users must know how to obtain and understand these important specifications to ensure an accurate picture of their system's capabilities.

A digital transmission system includes a data source—such as computer memory, a voice digitizer, or a multiplexer—that originates a digital signal, D *(Fig. 1)*. A clock source produces a clock signal, C, that times the occurrence of each bit in the digital signal. A driver, which may be a power amplifier, a laser diode, an RF modulator, or a tape head, prepares the signal for the system under test. The system under test can be a transmission line with repeaters, or an optical fiber link, microwave radio link, or digital tape recorder. The received signal, F, exhibits the noise and pulse dispersion that the transmission system adds to the digital signal.

If the noise and distortion are within limits, the decision circuit can correctly decide whether the original bit was a 1 or a 0. The circuit does this by comparing F (at sampling instants determined by clock signal G) with a threshold halfway between the two levels *(Fig. 1, again)*. If no errors are made in the decision process, H is a delayed replica of the original data signal D. A clock-



1. IN A TYPICAL DIGITAL TRANSMISSION system, the data signal, D, is corrupted by noise and pulse dispersion. As a result, the received signal, F, is distorted.

DAN WOLAVER and JAMES HANLEY
Microwave Logic, 20 Cummings Rd., Tyngsboro, MA 01879; (508) 649-6099.

BIT-ERROR-RATE TESTING

recovery circuit generates G from information in data signal F.

A malfunction in any system component can cause the recovered data to differ from the original data. The primary job of a BERT is to determine the system's error rate rather than to isolate the faulty component. But for the sake of convenience, the BERT may replace the clock source in the transmitter or the receiver. In this case, some fault isolation may be possible by comparing the performance of the system clock sources with that of the BERT. But for the comparison to be meaningful, users must understand the timing jitter specifications of both units.

To measure the system's error rate, the test set performs one or more of the following pairs of functions: data-pattern generation and error monitoring, clock generation and recovery, and jitter generation and measurement. Which functions are used depends on how the BERT is connected in the system.

The simplest measuring technique is to replace the system's data source with the BERT's data-pattern generator and have the BERT receiver monitor the recovered signal for errors *(Fig. 2a)*. Data signal D then becomes D′. The data-pattern generator can mimic typical traffic by creating pseudorandom patterns, or it can stress the system by outputting fixed patterns stored in memory.

Supplying Data Patterns

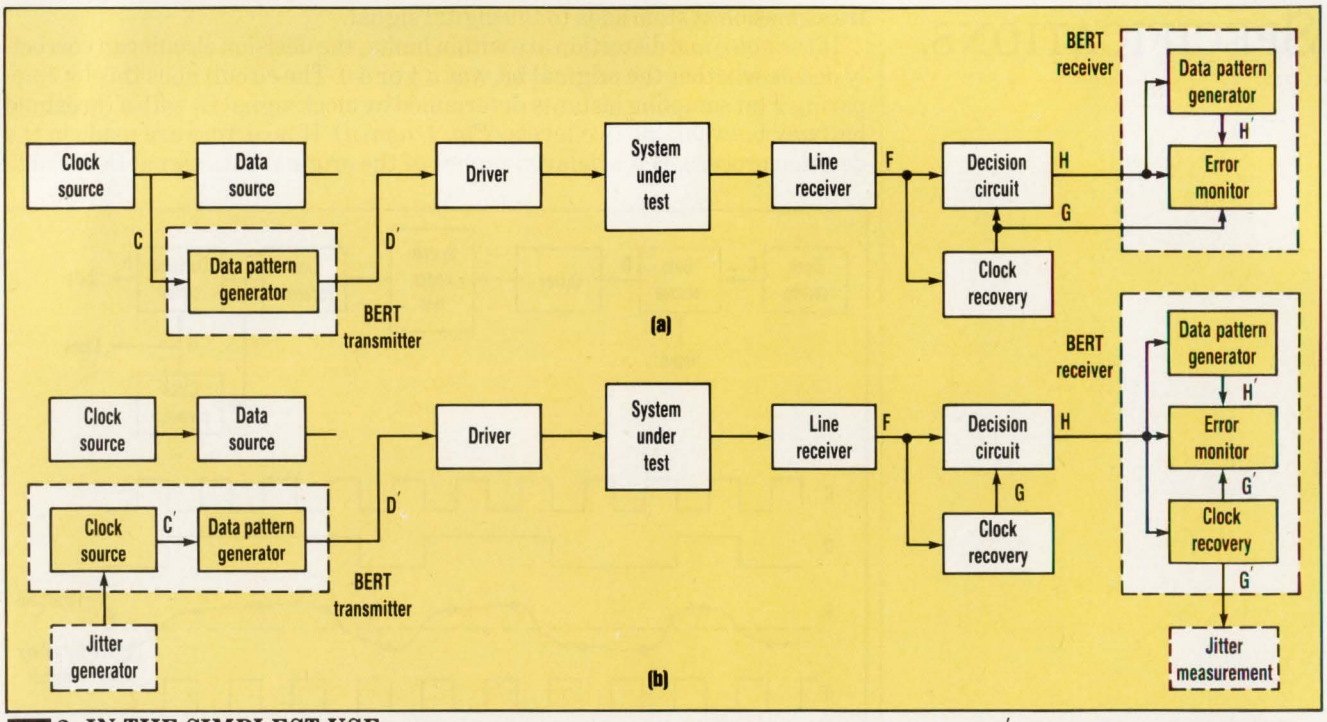
To monitor the transmission, the BERT receiver generates its own data pattern, H′, which is the same as the desired data, D′. The BERT receiver compares the received signal, H, with H′, and looks for errors. The tester records the total number of errors, the ratio of errors to bits (the bit error rate), the number of "errored" seconds (ES), and the ratio of ES to total seconds.

To make a valid comparison, the BERT receiver must synchronize H′ with H. Accomplishing synchronization depends on whether the data is a fixed or pseudorandom pattern.

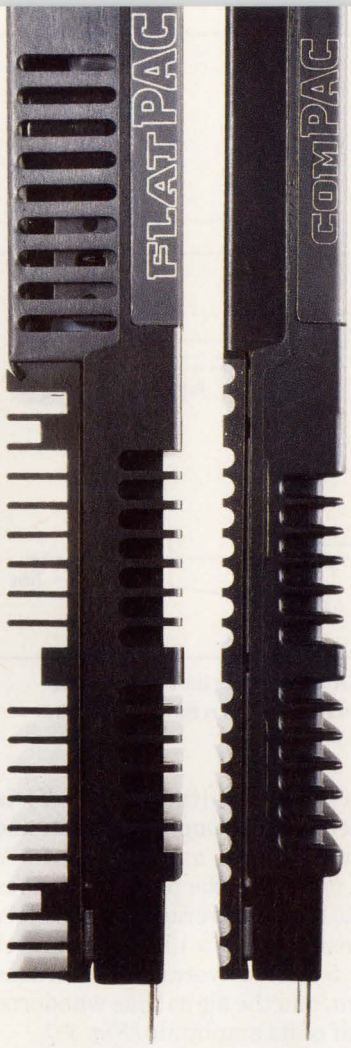
Sometimes it's convenient for the BERT to supply its own clock signals for its transmitter and/or its receiver. For instance, the system clock may be unavailable in a field situation, or the test engineer may want to avoid the trouble of providing and phasing the clock at the BERT receiver. In this case, the BERT's transmitter clock is C′, and its receiver clock is G′ *(Fig. 2b)*. In laboratory applications, it's common for the BERT to provide a wide range of clock frequencies.

The BERT's clock source and clock-recovery circuit must be as good as their counterparts in the system under test. The source must introduce negligible timing jitter, because phase jitter in C′ causes phase jitter in the recovered clock signal, G, relative to the received data signal, F. Likewise, the BERT's clock-recovery circuit must tolerate at least as much jitter as the system's recovery circuit without causing errors. Clock-source phase jitter and receiver jitter tolerance are discussed in detail later in this article.

Although the BERT clock source should be essentially jitter-free to test the digital transmission system under normal conditions, users may wish to stress the system at times. In



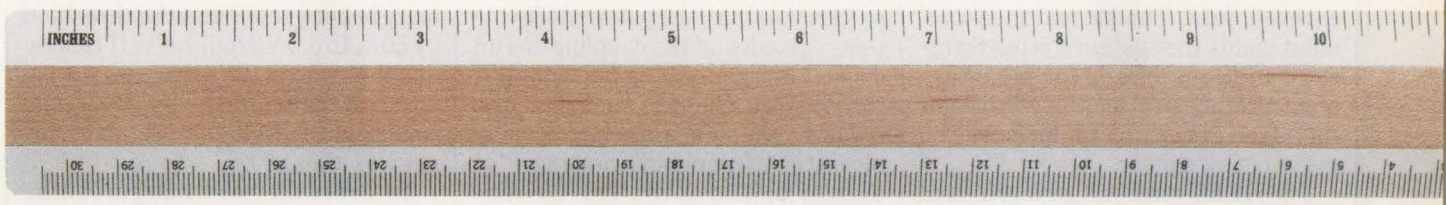
2. IN THE SIMPLEST USE of a bit-error-rate tester, the instrument creates a known data signal, D′. At the receive end, the BERT duplicates that signal so it can be compared with the transmitted version (a). In some cases, the BERT may supply the system clock signal and even add a known jitter that can be measured at the receive end (b). If the BERT supplies the clock, the instrument's clock source and clock recovery-circuit must be at least as good as their counterparts in the system under test.



Up To 600 Watts Per Inch

Our expanding family of compact, configurable, power systems combine the flexibility of a custom supply with the availability of standard catalog products . . . in low profile, compact packages that let you pack the most power into the least amount of space. And they meet the specialized input voltage, noise and transient requirements of major worldwide markets. Think of them as a universal solution for most of your system power requirements . . . AC or DC input . . . in computer, telecom or vehicular applications . . . up to 600 Watts.

FlatPAC™ is the industry benchmark for power density in off-line applications. And now, ComPAC™ sets the standard for DC input supplies . . . in a package less than one inch tall! Both offer unprecedented flexibility in configuration along with instant availability . . . in a fraction of the space required by conventional switchers. Just define your requirements . . . we utilize our high frequency, high power-density converters to quickly configure a FlatPAC or ComPAC specific to your needs.



You benefit from the proven field performance, high efficiency and inherently high reliability of our component-level power converters, without sacrificing any of the features you need: off-line inputs for worldwide application; nominal DC inputs from 24 to 300 VDC; surge limiting; safety agency recognition; EMI/RFI to FCC/VDE, British Telecom, Bellcore or MIL-STD-461; totally isolated and trimmable outputs; AC OK and DC OK status signals . . . and more.

FlatPAC™ AC Input		ComPAC™ DC Input
110/220 VAC	**Voltage Inputs**	24, 28, 48, 270, 300 VDC
1, 2, or 3	**Number of Outputs**	1, 2, or 3
2 to 95 VDC	**Output Voltages**	2 to 95 VDC
Up to 600 Watts	**Output Power**	Up to 600 Watts
1.37"	**Height**	1"
FCC Part 15, Class A VDE 0871, Class A IEEE Std 587-1980	**Applicable Specifications**	Bellcore (24/48 V) British Telecom (24/48 V) FCC/VDE, Class A (300 V) MIL-STD-461 C (28/270 V) MIL-STD-704A

You don't have to choose between costly and risky custom development or bulky catalog supplies. Call us to discuss FlatPAC and ComPAC . . . the new standards that make customs obsolete.

Does your power supply measure up?
Call VICOR EXPRESS for a *free ruler*
at **1-800-735-6200** or **508-470-2900** at ext. 265

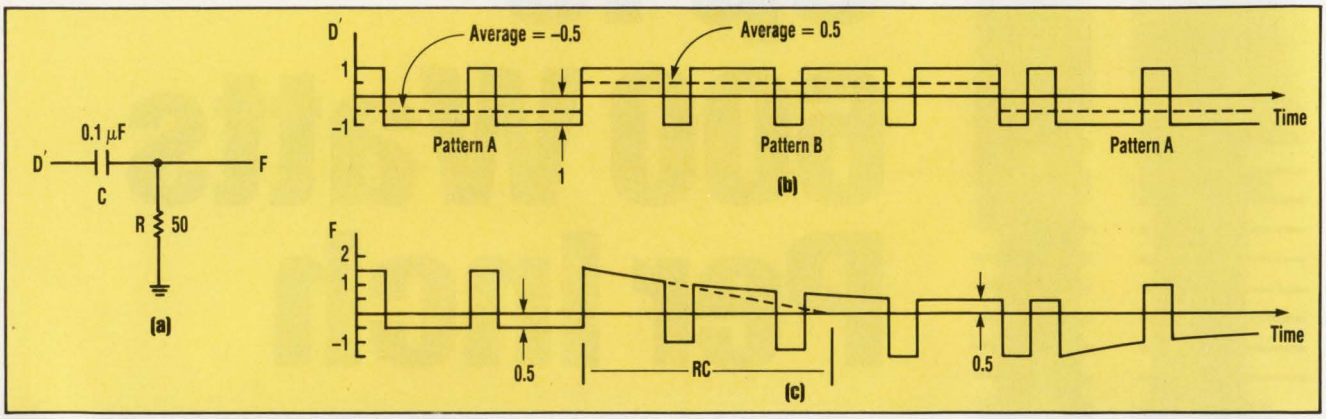
VICOR

Component Solutions For Your Power System
23 Frontage Road, Andover, MA 01810

Common Stock Traded on NASDAQ under **"VICR"**

CIRCLE 131

BIT-ERROR-RATE TESTING



3. MOST TRANSMISSION SYSTEMS use ac coupling (a). Consequently, a bit-error-rate tester can measure the system's noise margin by generating signal patterns with an unbalanced number of 1s and 0s (b). The result is baseline wander, which reduces the margin between the received signal, F, and the threshold (c).

that case, the BERT must generate controlled jitter. To do so, some BERTs have a jitter generator that can sinusoidally modulate the phase of the clock source *(Fig. 2b, again)*.

On the receive end, the BERT monitors the effect of the controlled jitter in two ways: First it looks for an increased error rate, then it measures the jitter remaining in the recovered data. The second measurement yields the system's jitter-transfer function. The jitter-measurement circuit can also be used without the jitter generator to measure the system's own jitter.

The BERT transmitter's principal task is to send a data pattern to the transmission system. The most general scheme is a repeating pattern that can be as short as 8 bits or as long as thousands of bits. Users can design the pattern to exercise the system in a number of ways, including noise margin and clock-recovery stressing.

Noise-Margin Stressing

The quality of signal F determines whether the digital transmission system decides correctly between a logic 1 and a logic 0. That quality depends on the noise margin, which is the separation between F and the logic threshold at the sampling point. Any distortion (usually due to a nonflat frequency response in the linear channel) reduces the noise margin. If the noise margin is large, the error rate is essentially zero and doesn't indicate the margin.

A BERT, however, can measure the noise margin by reducing it in a controlled way until the error rate is significant. The measurement uses what's called baseline wander. Most transmission systems are ac coupled to suppress the effects of biasing and dc offsets *(Fig. 3a)*. As long as the number of 1s and 0s in the data pattern is equal, the pattern's dc content is fixed, and the coupling circuit doesn't block anything important. If the balance changes at a low frequency, the coupling circuit may block that frequency, causing F to wander up and down. This baseline wander reduces the noise margin.

Properly designed transmission systems ensure that data patterns have no frequency components below the coupling circuit's cutoff, essentially eliminating baseline wander. But a BERT can purposely introduce some baseline wander to measure the noise margin.

An example is an input signal D′ that starts with a 10001000 pattern and switches to a 11101110 pattern. During the first imbalanced pattern, the average voltage, −0.5 V, is blocked by the coupling circuit, and the output F has an average of 0 V *(Fig. 3b)*. When the pattern changes to 11101110, D′ averages 0.5 V. After a transient with a time constant of RC = 5 μs, the average of F returns to zero, and the signal has wandered by half of its amplitude *(Fig. 3c)*.

TABLE 1: DATA PATTERNS FOR NOISE MARGIN STRESSING

Pattern A	Pattern B	Margin reduction
1100110011001100	1100110011001100	0 %
1000110011001100	1110110011001100	12.5
1000110010001100	1110110011101100	25.0
1000100010001000	1110111011101110	50.0

This baseline wander reduces the margin between F and the threshold by 50%, to 0.5 V from 1.0 V. If this reduction causes the error rate to become measurable—say 10^{-6}—the conclusion is that the original margin was about 50%.

To stress the noise margin continuously, the tester alternates between 10001000 (pattern A) and 11101110 (pattern B) at a frequency below the ac coupling circuit's cutoff frequency. Each pattern continues long enough for the circuit's transient to die out. A duration of 3.14 time constants, or πRC, is sufficient. Therefore, the complete fixed pattern stored in memory has a period of at least 2πRC. The frequency of the pattern is at most $1/2\pi$RC, which is the cutoff frequency, f_L, of the coupling circuit.

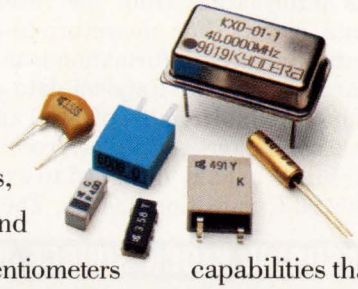
Then if the bit rate is f_c, the number of bits in the fixed pattern is:

$$N \geq f_c/f_L$$

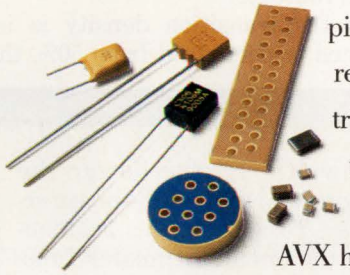
For example, if f_L = 32 kHz and f_c = 1 Gbit/s, the fixed data pattern must be at least N = 1 Gbit/s/32 kHz = 31,200 bits long.

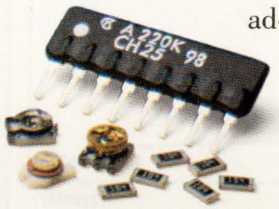
Users can create different stress

AVX would like to make a little noise about their expanded product line.



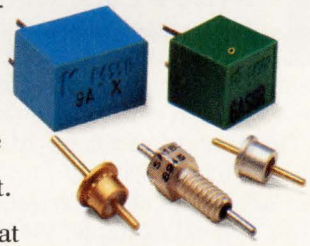
Feedback has been tremendous. Since we added clock oscillators, piezo devices, resonators and trimmer potentiometers to an already extensive line of capacitors, AVX has people everywhere talking. Because the company that wrote the book on passive components has added another chapter.



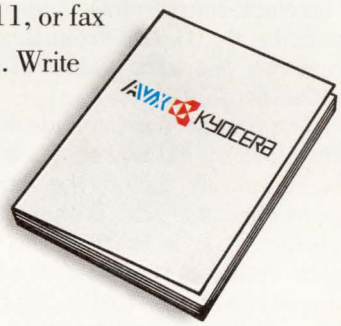


Through our association with Kyocera, AVX has firmly established itself as the undeniable leader in passive components. And with a network of local, national and international distributors, we give you access to any part you need. Anytime. Anywhere.

Ours is an industry where thinking globally is not just the key to victory, but to survival. That's why we've created distribution capabilities that offer solutions. No matter where you are. Or what you need. Plus the firm commitment to world-class quality, service, technology and manufacturing you've always come to expect. From the company that always makes sound decisions. AVX.



For more information about the AVX/Kyocera product line, contact AVX Corporation today by calling (803) 448-9411, or fax us at (803) 448-1943. Write to AVX Corporation, 17th Avenue South, P.O. Box 867, Myrtle Beach, SC 29577.



"Beep. Buzz. Ring. Tick. Hum."

AVX CORPORATION
A KYOCERA GROUP COMPANY

CIRCLE 132

BIT-ERROR-RATE TESTING

levels by combining the above patterns with patterns that have an equal number of 1s and 0s, thus causing no stress in a system with ac coupling. For example, the pattern 11001100 won't change the dc content or noise margin. By combining various amounts of this balanced pattern with the previous unbalanced patterns, users can stress the system to varying degrees, up to 50% *(Table 1)*. Other patterns, such as 1000000010000000, stress the noise margin by more than 50%, but they also stress the clock-recovery circuit, which may be undesirable.

Users who want to stress the clock-recovery circuit can do so by varying the transition density. This is because the system's receiver gets its information from the received data signal. For nonreturn-to-zero data, the clock information is in the data transitions. Random data contains an equal number of 0-to-1 and 1-to-0 transitions, and a clock-recovery circuit is usually designed to expect this 50% transition density. The circuit may have trouble with either a greater or a lesser density.

The simplest fixed pattern with a 50% transition density is again 11001100. The patterns in Table 1 that stress noise margin by varying the balance of 1s and 0s also maintain a 50% transition density. Similarly, patterns that stress the clock-recovery circuit by varying transition density should keep the 1s and 0s in balance *(Table 2)*.

As the transition density is increased or decreased from 50%, the

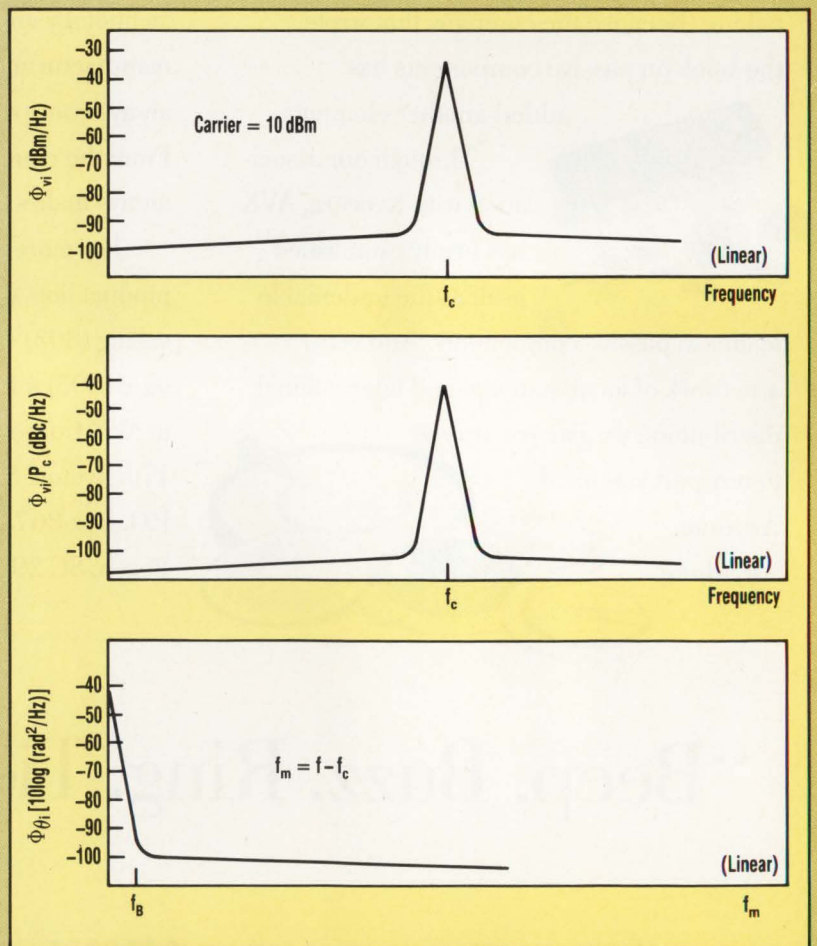
MEASURING CLOCK-SOURCE JITTER

Test engineers can characterize a clock source's phase jitter, θ_i, by using a spectrum analyzer to measure Φ_{vi}, which is the source's power spectral density at voltage v_i.[2] The amount of phase jitter is indicated by the width of the spectrum about the clock frequency, f_c. In a typical example, the peak spectral density is about –30 dBm/Hz *(Fig. A, top)*. (Most spectrum analyzers display power spectral density directly in dBm/Hz.) From Φ_{vi}, users can calculate the clock-source phase's spectral density, $\Phi_{\theta i}(f)$, and from this determine the rms value of the phase error, θ_e.

The first step is to divide Φ_{vi} by the clock signal power, P_c, which is commonly called the carrier power because jitter is phase modulation. If P_c is 10 dBm, the division reduces the peak spectral density to about –40 dBc/Hz *(Fig. A, middle)*. The units change because the level is now relative to the carrier.

Finally, $\Phi_{\theta i}$, the spectral density of the clock phase, is obtained by shifting Φ_{vi}/P_c so its peak is at the origin *(Fig. A, bottom)*. The relationship is $\Phi_{\theta i}(f_m) = \Phi_{vi}(f)/P_c$, where f_m is the offset frequency from the carrier frequency, f_c; that is, $f_m = f - f_c$. The units dBc/Hz now have the interpretation 10log(rad²/Hz). For example, 10log(rad²/Hz) = –90 corresponds to 10^{-9} rad²/Hz.

To keep the clock edge in the center of the eye pattern, the clock recovery circuit tries to track θ_i. The wider the circuit's bandwidth, f_B, the better the tracking and the less the phase error, θ_e. To analyze this relationship, the circuit's transfer func-



A. IF THE BERT MANUFACTURER doesn't supply information on clock-source jitter, users can find $\Phi_{\theta i}$, the spectral density of the clock-source jitter, bottom. First, they measure the source's power spectral density, Φ_{vi}, top. Then they divide that curve by the clock signal power, P_c, middle.

BIT-ERROR-RATE TESTING

clock-recovery circuit will fail and the error rate will become significant. A well-designed clock recovery will typically tolerate transition densities between 100% and 25% without causing errors.

DATA PATTERNS STORED

Fixed patterns can also be designed to simulate valid line formats in telecommunications. One such format is DS2, the third level in the North American digital hierarchy at 6.312 Mbits/s. The DS2 frame is 1176 bits long, organized into 24 groups of 49 bits. The first bit in each group of 49 is a framing bit or a control bit, and the rest are data bits. A BERT transmitter can generate such a pattern to test terminal equipment that looks for the framing and control bits.

Fixed data patterns are stored in the BERT transmitter. User-defined patterns are stored in RAM, and manufacturer-provided patterns are stored in ROM. For example, the Microwave Logic gigaBERT-660 offers 6480-bit and 19,440-bit SONET frame patterns on ROM as options.

The BERT receiver must be programmed to produce the same data pattern as the transmitter. The receiver synchronizes its pattern, H′, to the received data pattern, H, on the basis of error rate. If the error rate is greater than some set level, say 10^{-2}, H′ is shifted one bit by dropping a clock pulse. This continues until the synchronization is achieved, as indicated by an error rate less than 10^{-2}.

Another type of pattern, a pseudorandom bit sequence (PRBS), simulates live traffic. A PRBS has all of the properties of a random sequence but is periodic. A fixed pattern could be programmed to produce a PRBS, but a simple circuit can generate a pattern millions of bits long with only 20 to 30 bits of memory. Common pattern lengths are $N = 2^7 - 1$, $2^{15} - 1$, and $2^{23} - 1$.

PRBS patterns can stress the noise margin and the clock recovery as fixed patterns do. But it's done randomly, somewhat like live traffic. When averaged over the whole sequence, the number of 1s and 0s is almost equal (actually different by one), and transition density is 50%. Over a short term, though, the averages can be very different, stressing both noise margin and clock recovery for periods of time.

To stress the noise margin, the PRBS spectrum must have components below the coupling circuit's cutoff frequency, f_L. For example, a 23-stage PRBS generator with a bit rate, f_c, of 44.7 Mbits/s has a pattern length of $2^{23} - 1 = 8{,}388{,}607$ bits. The fundamental frequency, f_F, is $f_c/8{,}388{,}607 = 5.33$ Hz. If $f_L = 32$ kHz, thousands of the pattern's spectral components are removed. The fraction of power removed is given by $\pi f_L/f_c$, and the square root of that figure is the rms error as a fraction of the signal level:

$$\text{rms error} = \sqrt{\pi f_L/f_c} = 0.047.$$

This error appears as Gaussian noise with an rms value that is 4.7% of the noise margin. The more spectral components below the cutoff frequency, the more Gaussian the

tion from θ_i to θ_e can be assumed to be θ_e/θ_i. The magnitude squared of this function typically has the form:

$$|\theta_e/\theta_i|^2 = f_m^2/(f_m^2 + f_B^2)$$

A plot of this function shows that below f_B, the response rises at two decades per decade, leveling off at unity above f_B *(Fig. B)*.

The spectral density of θ_e is:

$$\Phi_{\theta e} = \Phi_{\theta i}|\theta_e/\theta_i|^2$$

The spectral density of θ_i, meanwhile, is:

$$\Phi_{\theta i}(f_m) = (f_B/f_m)^2\,\Phi_{\theta e}(f_B)$$

and usually descends at two decades per decade. In the example case, $\Phi_{\theta i}(f_m)$ drops from 10^{-9} to 10^{-11} rad²/Hz as f_m rises from f_B to $10f_B$ *(Fig. B, again)*.

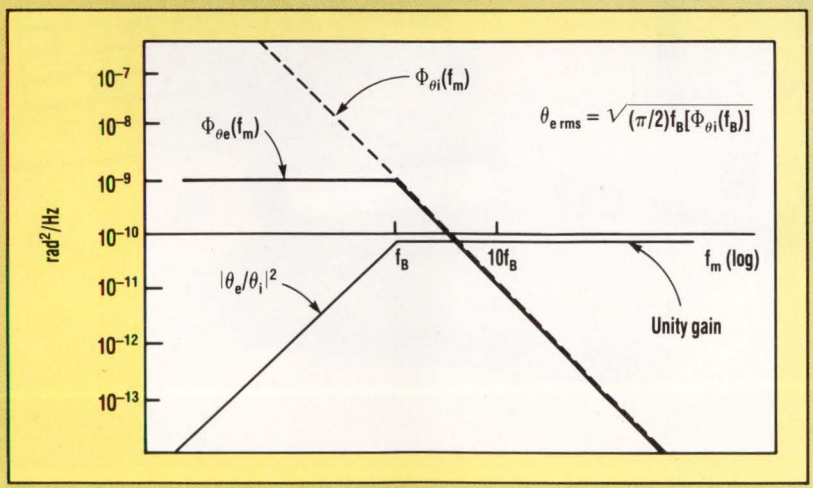
Finally, $\Phi_{\theta e}(f_m)$ can be calculated as:

$$\Phi_{\theta e}(f_m) = \Phi_{\theta i}(f_B) f_B^2/(f_m^2 + f_B^2)$$

This curve is flat below f_B at the level $\Phi_{\theta i}(f_B)$ and descends at two decades per decade above f_B *(Fig. B, again)*. The mean-square value of θ_e is the area under $\Phi_{\theta e}(f_m)$, which can be shown to be $(\pi/2)f_B\Phi_{\theta i}(f_B)$.[3]

Therefore, the rms value of θ_e in radians is:

$$\theta_{e\,rms} = \sqrt{(\pi/2)f_B\,\Phi_{\theta i}(f_B)}$$



B. THE SPECTRAL DENSITY, $\Phi_{\theta e}$, of the phase error is the product of the spectral density, $\Phi_{\theta i}$, of the clock phase and the phase transfer function, which is the magnitude squared of θ_e/θ_i (the rms value of the phase error divided by the clock source phase jitter). The rms phase error, $\theta_{e\,rms}$, is the square root of the area under $\Phi_{\theta e}$.

Motorola's In Real

© 1990 Motorola, Inc. Motorola Computer Group is a member of Motorola's General Systems Sector. VMEexec is a trademark of Motorola, Inc. All other product or brand names mentioned are trademarks or registered trademarks of their respective holders.

88open COMPATIBILITY CERTIFIED

Malcolm Baldrige National Quality Award

-Time, Big-Time.

One glance at the full array of options Motorola offers in real-time, and you'll see why it's become the developer's platform of choice. For both target and host environments, no other single vendor has anything like it.

One reason is our long-time experience with real-time technology, beginning with our pioneering work back in 1980. Another is the broad spectrum of our product line, which includes ICs, boards, systems, and software. In short, Motorola has everything you need to build real-time applications ranging from simulation to industrial automation to imaging and more.

CISC RISC

Yet another reason to choose Motorola is our unending commitment to open standards. Our real-time platform gives you standards-based choices at various levels of integration. The centerpiece of this non-proprietary approach is VMEexec,™ our wide-open, totally integrated development environment. VMEexec allows you to use standard UNIX® interfaces to write a single set of application code, and then reuse it for other projects. Better still, you can combine any software product that conforms to these standards. VMEexec includes a high-performance real-time executive, a strong run-time connection to UNIX-based systems, flexible and efficient real-time I/O and file systems, as well as powerful development and debug capabilities. And because VMEexec is integrated with the hardware, you can begin software development even before the hardware is available.

If you're thinking about real-time, you should be thinking about time to market, and that's all the more reason to think Motorola. Especially when you consider that we can help speed product integration by serving as a single source for boards, software and systems. Add to that the industry's best applications expertise and design support, ranging from small embedded control systems to multi-processor simulation. Then factor in Six Sigma quality control. And remember that Motorola gives you the industry's only true migration path from CISC to RISC in both the development and run-time environments.

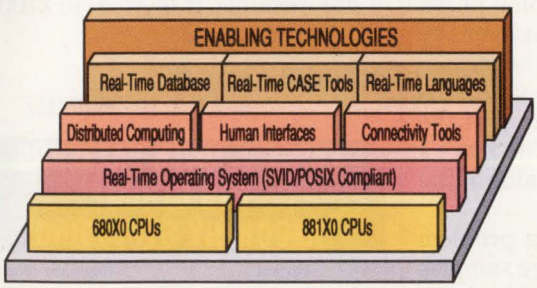
Right now, Motorola real-time systems are hard at work in critical applications worldwide.

Give us a call today at **1-800-624-8999**, ext. 230, and put the real-time resources of Motorola on your side. We think you'll find the benefits are very big, and very real.

We Do Real-Time Full-Time.

At Motorola, we've dedicated an entire division solely to real-time development systems. Our real-time system architecture begins at the microprocessor level in either CISC or RISC, and extends all the way to the end-user. Today, you can use VMEexec to port UNIX applications to an SVID-compliant (and soon, POSIX-compliant) real-time environment, and vice versa. And they can be used for run-time capabilities as well as for development. Several human interfaces are available for UNIX, including Motif, X.11 and DeltaWINDOWS.™ As for networking, Motorola supports all popular protocols, including TCP/IP, NFS, SNA, OSI, and X.400. We also offer database and CASE tools, and you can work in C, LISP, FORTRAN, ADA, BASIC, COBOL, and PASCAL. Put it all together, and you will discover only one company gives you the full story on real-time, and that's Motorola.

INTEGRATED REAL-TIME PLATFORM



MOTOROLA
Computer Group

CIRCLE 158

BIT-ERROR-RATE TESTING

noise is. However, if the PRBS pattern length was $2^7 - 1$, the fundamental would be 350 kHz, which is greater than f_L. The noise margin wouldn't be stressed, and the formula for rms error wouldn't hold.

Similarly, a PRBS pattern will stress the clock-recovery circuit if the pattern's fundamental is within the circuit's bandwidth, f_B. If it is, the pattern introduces random jitter in the recovered clock. The jitter's magnitude depends on f_B and on offsets within the circuit.[1]. The rms jitter isn't a function of the PRBS pattern length, but the peak jitter increases with pattern length.

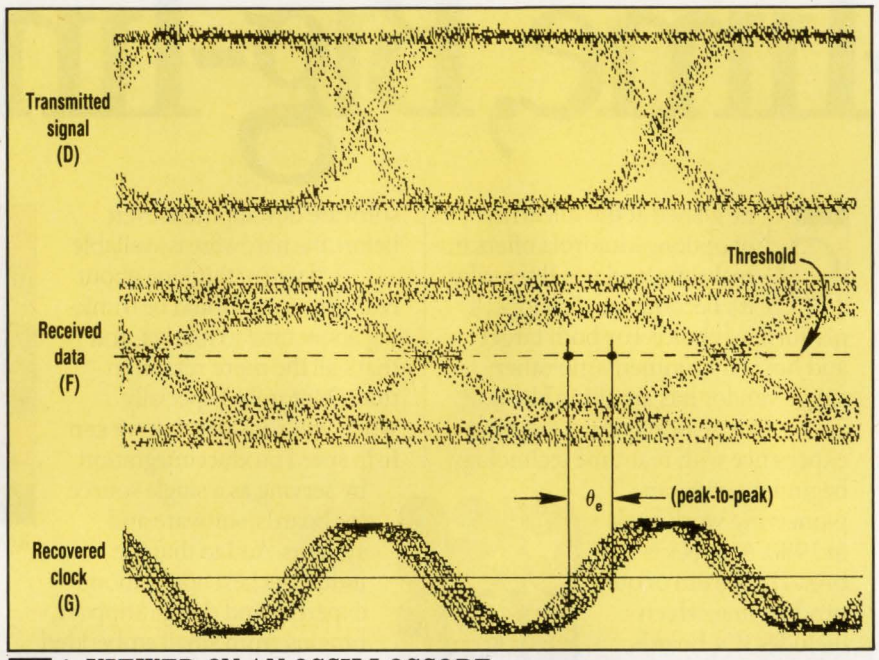
EXAMINING JITTER

An important factor in a data transmission system is jitter. Ideally, all clock and data signals in the system have a constant frequency with no phase modulation. In practice, a clock source has some phase modulation, or jitter, and noise and imperfect equalization introduce additional jitter. The following discussion examines clock-source jitter alone, assuming that noise and distortion contribute no jitter.

If the received data waveform, F, is viewed on an oscilloscope synchronized to that data, the 1s and 0s overlap to produce an "eye" pattern *(Fig. 4)*. If the transmitter clock source has phase jitter θ_i, the received data signal, F, has the same jitter. But the eye pattern doesn't display this jitter because the scope is synchronized to the data.

In general, θ_o, which is the phase of the recovered clock signal, G, cannot track θ_i exactly, so some phase error ($\theta_e = \theta_i - \theta_o$) exists between the clock and the data. With the oscilloscope synchronized to the data, this error is seen as a broadening of the recovered clock's trace. The trace's width is the peak-to-peak value of the phase error jitter.

Phase error can cause a problem when the clock's rising edge samples the received data to see if it's above or below the threshold. If the phase error is too great, the rising clock edge approaches the sides of the data eye pattern, and the transmission system's decision circuit makes errors.



4. VIEWED ON AN OSCILLOSCOPE synchronized to the received data, phase error, or jitter, θ_e, shows up as a widening of the recovered clock's waveform.

If $\Phi_{\theta i}(f)$ and f_B are known, the rms phase error can be calculated:

$$\theta_{e\,rms} = \sqrt{(\pi/2) f_B \Phi_{\theta i}(f_B)} \qquad (1)$$

where $\Phi_{\theta i}(f_B)$ is the spectral density of the clock-source phase jitter (*see "Measuring clock source jitter," p. 76.)* BERT manufacturers sometimes specify the clock's single-sideband noise density, $\Phi_{vi}(f)$, at an offset frequency of 10 kHz, which is also the value of $\Phi_{\theta i}(10\text{ kHz})$. From this figure, the value of $\Phi_{\theta i}(f_B)$ can be approximated by:

$$\Phi_{\theta i}(f_B) = (10\text{ kHz}/f_B)^2 \Phi_{\theta i}(10\text{ kHz}).$$

For example, if $\Phi_{vi}(f_c + 10\text{ kHz})$ is –84 dBc/Hz, then:

$$\Phi_{\theta i}(10\text{ kHz}) = 10^{-84/10} = 2.5 \times 10^{-9}\text{ rad}^2/\text{Hz}$$

TABLE 2: DATA PATTERNS FOR CLOCK RECOVERY STRESSING

Pattern	Transition density
1010101010101010	100%
1010110010101100	75
1100110011001100	50 (normal)
11001110001100111000	40
11100011100011100	33
11100011100011110000	30
1111000011110000	25

and for $f_B = 16$ kHz,

$$\Phi_{\theta i}(f_B) = (10\text{ kHz}/16\text{ kHz})^2 \times (2.5 \times 10^{-9}) = 10^{-9}\text{ rad}^2/\text{Hz}.$$

If the BERT manufacturer supplies no information on clock-source jitter, the user must measure the spectral density.

Once f_B and $\Phi_{\theta i}(f_B)$ are known, the rms phase error $\theta_{e\,rms}$ can be calculated from Equation 1. Typical spectral density for the Microwave Logic gigaBERT-660 clock source at $f_c = 70$ MHz and $f_B = 16$ kHz is 10^{-9} rad^2/Hz. For these specifications, Equation 1 yields an rms phase error of 0.005 rad, or about 0.0008 UI (unit intervals), where 1 UI = 2π rad. Because the width of the eye pattern in this example is on the order of 1 UI, the phase error has a negligible effect on system performance.

JITTER TOLERANCE

In general, the noise and imperfect equalization of the transmission system itself introduce much more jitter than the clock source does. If the jitter, θ_i, of the received data exceeds the receiver's jitter tolerance, the receiver will begin making errors. When the BERT is recovering its

CIRCLE 130 →

BIT-ERROR-RATE TESTING

own clock, the instrument receiver's jitter tolerance must be greater than the system receiver's for all waveforms. Otherwise, the BERT will report an incorrectly high error rate.

It's impossible to check all waveforms. Fortunately, however, if the BERT receiver has a higher jitter tolerance for sinusoidal jitter at all jitter frequencies, f_m, then it has a higher jitter tolerance for all jitter waveforms.

The maximum data phase jitter, θ_i, that a receiver can tolerate depends on the maximum phase error, $\theta_{e\,max}$, between the data and the clock that the receiver can tolerate. The first failure may be the setup time when the decision circuit samples the data with the clock.

Or the clock-recovery circuit may fail to maintain lock if θ_e is too great. In any case, $\theta_{e\,max}$ is generally between 0.3 and 1.0 UI peak-to-peak. If the system's $\theta_{e\,max}$ is unknown, it can be measured.

The transfer function from θ_i to θ_e is:

$$|\theta_e / \theta_i| = f_m / (f_m^2 + f_B^2)^{1/2} \qquad (2)$$

where f_m is the frequency of the sinusoidal jitter *(Fig. 5)*. Then the maximum data jitter a receiver can tolerate is

$$\theta_{i\,max} = \theta_{e\,max} / |\theta_e / \theta_i|$$

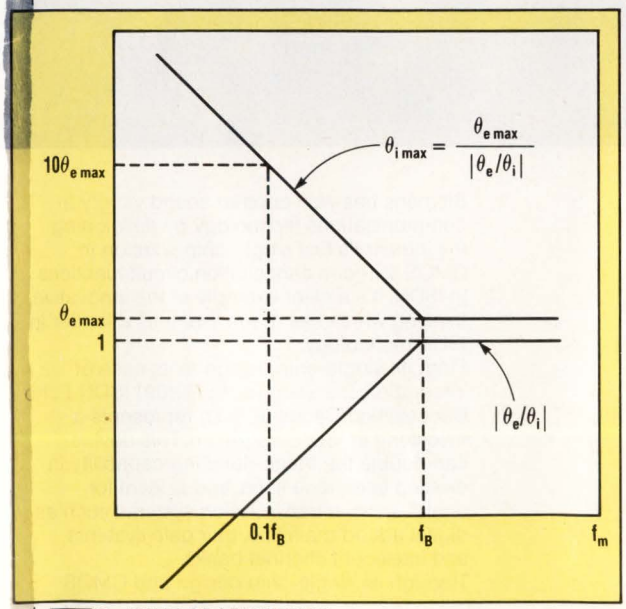
Below f_B, $\theta_{i\,max}$ descends at one decade per decade. Above that frequency (where the clock recovery can't follow the data jitter), $\theta_{i\,max} = \theta_{e\,max}$.

For proper operation, the BERT receiver's jitter tolerance curve must lie above that of the system receiver. The plot in Fig. 5 shows that this condition is satisfied if the BERT receiver has a larger f_B and larger $\theta_{e\,max}$ than the system receiver. The plot offers a quick and simple check if these parameters are known. If not, the jitter tolerance curves must be measured using a calibrated jitter generator, which some BERTs provide.

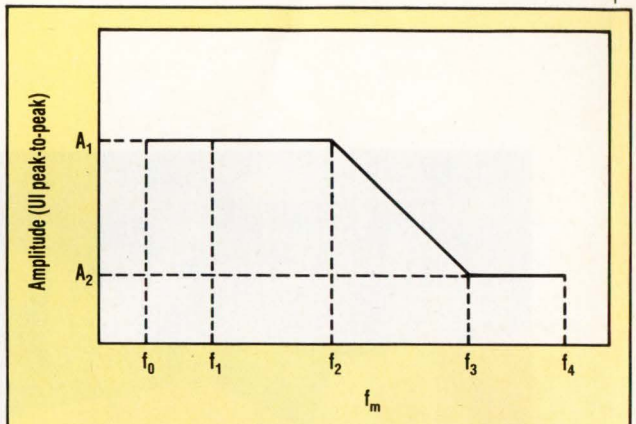
A BERT designed to supply jitter has a sinusoidal generator that modulates the clock phase *(Fig. 2b, again)*. Both the frequency, f_m, and the amplitude, A, of the phase are selectable over certain ranges. CCITT Recommendation O.171 specifies the minimum ranges, which depend on the bit rate of the system under test. The range of f_m is from f_0 to f_4, and the range of the amplitude depends on f_m. At low frequencies, the bit-error-rate tester must generate higher amplitudes than are needed at high frequencies *(Fig. 6)*.

A BERT designed to measure jitter has a phase demodulator connected to the recovered clock. Once again, the CCITT specifies the jitter frequencies and amplitudes that should be covered. The range of f_m is from f_1 to f_4; the amplitude depends on f_m.

The BERT's jitter generation and jitter measurement specifications should be somewhat higher than the maximum jitter that a system can typically tolerate. As a result, a BERT with jitter generation can find a receiver's $\theta_{e\,max}$ by setting $f_m = f_4$ and increasing A until the receiver begins to make errors. In addition, the clock-recovery bandwidth, f_B, can be estimated by lowering f_m until the jitter tolerance begins to exceed $\theta_{e\,max}$.



5. THE MAXIMUM sinusoidal data jitter that can be tolerated, $\theta_{i\,max}$ depends on the maximum tolerable sinusoidal error jitter, $\theta_{e\,max}$, and the clock recovery bandwidth, f_B.



Bit rate	f_0	f_1	f_2	f_3	A_1	A_2
1.544 Mbit/s	2 Hz	200 Hz	4 kHz	40 kHz	10 UI	0.5 UI
2.048	2	2400	45	100	10	0.5
6.312	2	1600	32	160	10	0.5
8.448	2	400	8.5	400	10	0.5
32.064	2	1600	32	800	10	0.5
34.368	2	1000	20	800	10	0.5
44.736	2	3200	100	4500*	16	0.5
139.264	2	500	10	3500	10	0.5

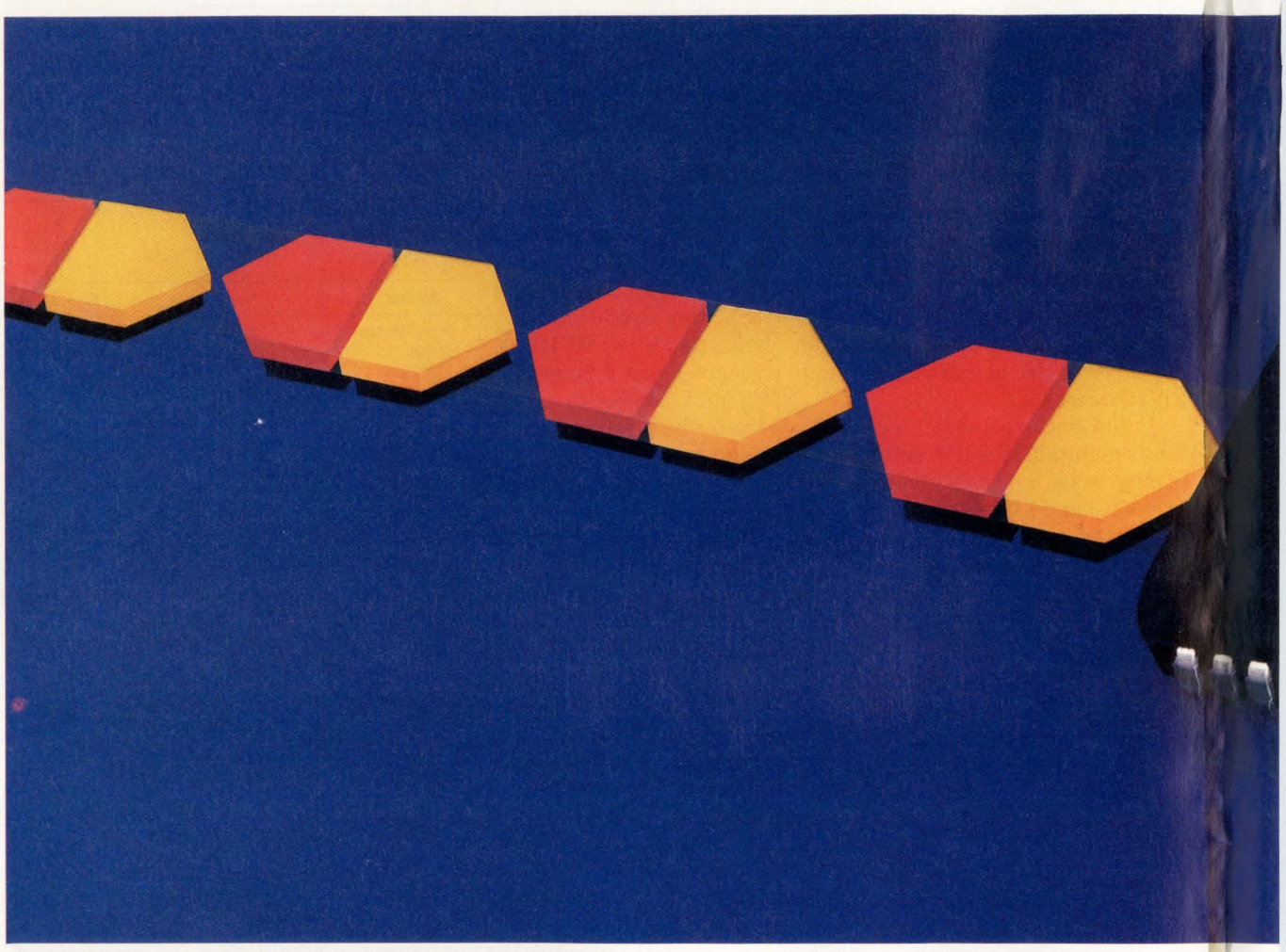
*In practice only 1120 kHz instead of 4500 kHz.

6. THE RANGE OF JITTER frequencies and amplitudes that a BERT should generate (shown in this graph) are specified by CCITT Recommendation O.171.

BERT AFFECTS ACCURACY

Several BERT characteristics can affect the accuracy of system measurements. For instance, a BERT transmitter may have a very jittery clock source, such as an open-loop voltage-controlled oscillator. If so, the system will have a higher error rate or less margin than when the system's clock source is used. Measuring the clock-source spectral density and calculating $\theta_{e\,rms}$ will uncov-

SIEMENS



Sound Strategy.

Siemens announces a single-chip echo cancellation U-interface device for ISDNetworks of all sizes. From switching to transmission, a clearly superior solution. Berlin to Iselin.

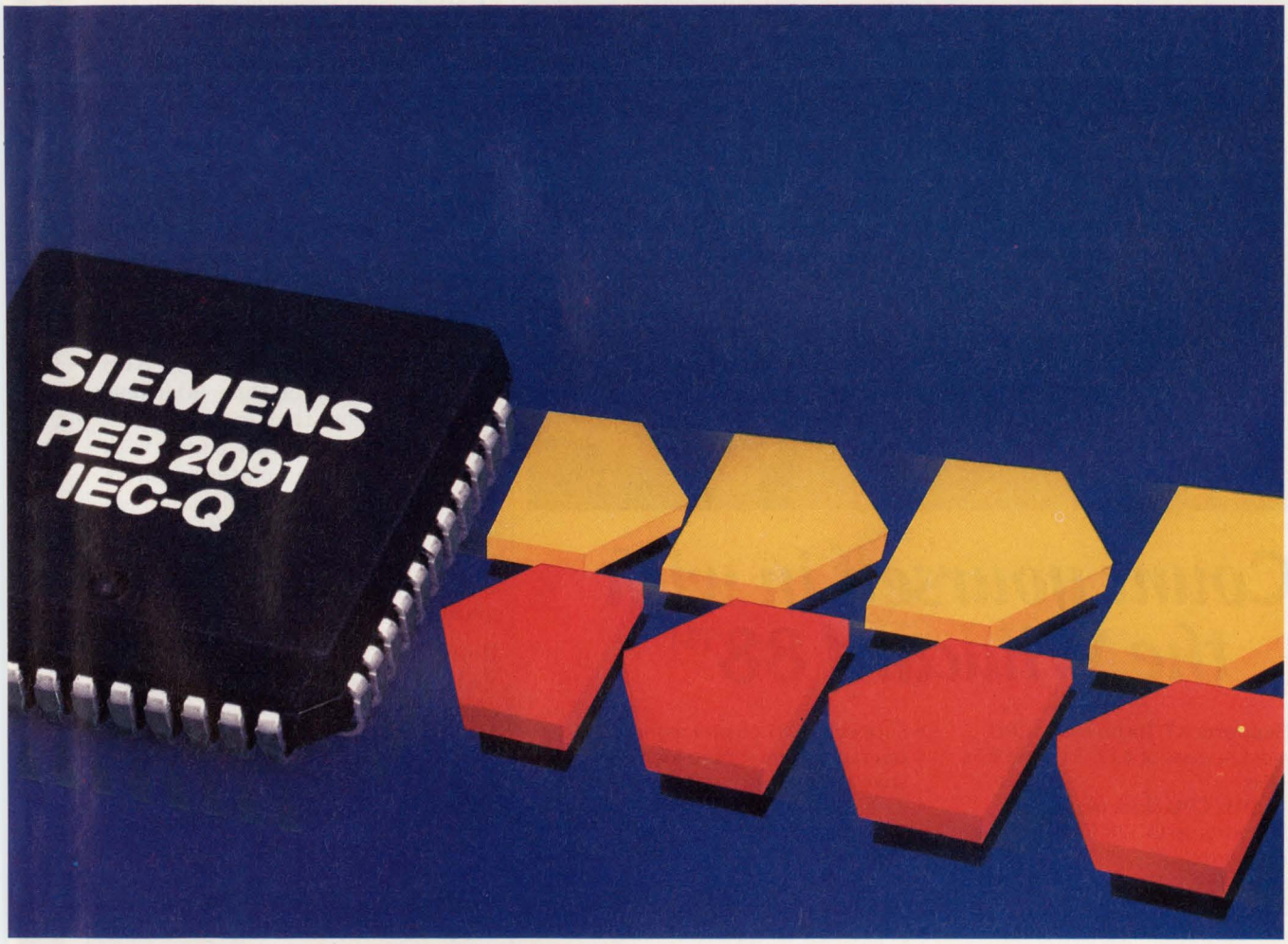
Siemens has won another sound victory in communications technology by developing the industry's first single-chip solution in CMOS for echo cancellation circuit functions in ISDN. It's a clear example of the innovative thinking which has made Siemens a leader in ISDN technology.

From its single-chip design to its ease of integration, the Siemens PEB 2091 ISDN Echo Cancellation Circuit (IEC-Q) represents a milestone in ISDN realization. This device can double the traffic-handling capability in existing telephone lines, and is ideal for applications in transmission systems such as digital added main line, pair gain systems and intelligent channel banks.

Through its single-chip design and CMOS

The best address for Siemens Semiconductors:

(A) **Wien,** Tel. (0222) 71711-5661 (AUS) **Melbourne, Vic. 3121,** Tel. (03) 4207111 (B) **Bruxelles,** Tel. (02) 536-2111 (BR) **São Paulo-SP,** Tel. (011) 833-2211 (CDN) **Mississauga L5T 1P2,** Tel. (416) 564-1995 (CH) **Zürich,** Tel. (01) 495-3111 (D) **Berlin 10,** Tel. (030) 3993-0; **Düsseldorf 1,** Tel. (0211) 399-0; **Frankfurt 1,** Tel. (069) 797-0; **Hamburg 1,** Tel. (040) 2889-0; **Hannover 81,** Tel. (0511) 877-0; **München 80,** Tel. (089) 9221-4391/4138; **Nürnberg 1,** Tel. (0911) 654-0; **Stuttgart 1,** Tel. (0711) 2076-0 (DK) **Ballerup,** Tel. (44) 774477 (E) **Madrid,** Tel. (01) 5554062 (F) **Paris,** Tel. (1) 4922-3810 (GB) **Sunbury on Thames,** Tel. (0932) 752615 (GR) **Amaroussio/Athen,** Tel. (01) 6864-111 (HK) **Hongkong,** Tel. 5-8330222 (I) **Milano,** Tel. (02) 6766-4241 (IND) **Bombay 400018,** Tel. 4938786

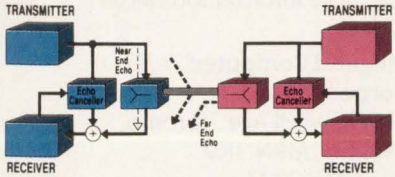


M12A006

technology, the advanced PEB 2091 reduces space requirements and software overhead, and has lower power consumption requirements than any other design. And it supports ISDN Oriented Modular (IOM) architecture, the de facto standard for ISDN, which makes installation simple, and enables it to work in tandem with the most advanced ICs available.

Building upon the most comprehensive line of ISDN ICs in the industry, the PEB 2091 sends a clear signal that Siemens is continuing to take great strides in telecommunications.

Siemens was the first company to design a two-chip U-interface transceiver for the 4B3T block code used in Europe, and developed the first single-chip device for the 2B1Q code established in North America.



Siemens uses CMOS technology to provide a superior echo cancellation solution with the lowest power consumption requirements.

And the PEB 2091 meets the requirements of the American National Standard for Telecommunication.

Our unsurpassed line of ISDN ICs are complemented by a wide array of microprocessors, microcontrollers, DRAMs, optoelectronic devices, and more. So you can count on Siemens to provide the best solution for all of your IC applications, and telecommunication products which reflect the sound thinking that has made Siemens a leader in ISDN.

For details, call (800) 456-9229, or write Siemens Components, Inc., 2191 Laurelwood Road, Santa Clara, CA 95054-1514. Ask for literature package M12A006.

(IRL) **Dublin,** Tel. (01) 302855 (J) **Tokyo 100,** Tel. (03) 201-2401 (N) **Oslo 5,** Tel. (02) 633000 (NL) **Den Haag,** Tel. (070) 3333333 (P) **Alfragide,** Tel. (01) 4183311 (RA) **Buenos Aires,** Tel. (01) 300411 (RC) **Taipei,** Tel. (02) 5234700 (ROK) **Seoul,** Tel. (02) 275-6111 (S) **Kista,** Tel. (08) 7033500 (SF) **Helsinki,** Tel. (9) 051051 (SGP) **Singapore 0513,** Tel. 7760044 (TR) **Istanbul,** Tel. (01) 1510900 (USA) **Iselin,** Tel. (201) 906-4300 (Discrete); **Santa Clara,** Tel. (408) 980-4500 (ICs); **Cupertino,** Tel. (408) 725-7910 (Opto) (ZA) **Johannesburg,** Tel. (011) 407-4111

TopTech Semiconductors Siemens

CIRCLE 154

Count yourself in with the Wildcard 88™

- **Supports XT Turbo** mode CPU clock speeds of 4.77, 7.15 and 9.54 MHz
- **10 MHz CPU** clock frequency
- Supports up to 32K Bytes of onboard BIOS EPROM
- Small 2″×4″ form factor
- Bios available for easy integration
- Onboard DRAM controller for easy system design
- Onboard bus controller supports XT I/O channel
- Supports 8087 co-processor operation (with socket) for high speed numeric data processing
- Reduces XT parts count by 75%
- Supports up to 640K of system DRAM
- Onboard sound generator supports speaker control
- Improves total system reliability
- Reduces overall system costs and factory overhead
- Onboard Keyboard Controller

Megatel is expanding the Wildcard family to offer you more development flexibility.

The Wildcard family offers the lowest cost, smallest footprint solution for your XT class system. It integrates all functions of the IBM PC, XT® motherboard minus DRAM and DRAM drivers. All on a circuit card the size of a business card. For more information call us today.

Megatel Computer Corporation
125 Wendell Ave., Toronto, Ontario M9N 3K9
(416) 245-3324
FAX (416) 245-6505

Wildcard 88™ is a trademark of Megatel Computer Corp. IBM PC, XT are registered trademarks of IBM Corp.

megatel

CIRCLE 80

DESIGN APPLICATIONS

BIT-ERROR-RATE TESTING

er this problem.

Another snag may be that a BERT receiver has a very narrowband clock-recovery circuit, such as a crystal-controlled phase-locked loop. The small f_B will probably make the BERT less tolerant of jitter than the system it's testing. In high-jitter situations, therefore, the BERT will report a higher bit error rate than the actual rate. A BERT transmitter with jitter generation can measure its own receiver's jitter tolerance and that of the system to see which is greater.

The question of whether a BERT data pattern fairly represents live traffic is more difficult to answer. Experience indicates that long PRBS patterns (N greater than 14) stress the system more than most live traffic does. But it's the rare traffic with unusually stressing patterns that is most interesting. Therefore, the best users can do is to anticipate these patterns and generate them with fixed patterns from the BERT transmitter.□

References

[1]D.H. Wolaver, *Phase-locked loop circuit design* (Englewood Cliffs: Prentice-Hall, 1991), Chapter 10.
[2]"Phase noise characterization of microwave oscillators," Product Note 11729C-2, Hewlett Packard Associates, Palo Alto, Calif., September, 1985.
[3]B.P. Lathi, *Modern digital and analog communications systems* (Philadelphia: HRW 1983), Chapter 5.

Dan Wolaver, a consulting electrical engineer, received a BSEE from Rensselaer Polytechnic Institute, Troy, N.Y., and an MSEE and PhD from Massachusetts Institute of Technology, Cambridge.

James Hanley, vice president of marketing at Microwave Logic, received BSEE and MSEE degrees from the University of Illinois, Urbana.

How Valuable?	Circle
Highly	535
Moderately	536
Slightly	537

The secret to better Ethernet is NICE. And simple.

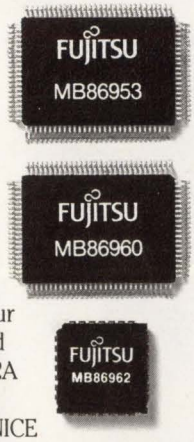
Introducing NICE.™ The new MB86960 Network Interface Controller with Encoder/Decoder from the Advanced Products Division of Fujitsu Microelectronics.

With the unveiling of NICE, Ethernet LAN technology reaches a new level of integration.

Now LAN system designers can have an Ethernet controller, buffer management unit and 10 Mbit per second Manchester encoder/decoder on a single chip. So you can now develop high-performance LAN boards more cost effectively than ever before.

For instance, design adapter cards for high-performance buses using just two Ethernet chips instead of the usual three. Simply combine NICE with our new MB86962 10BASE-T transceiver, the most advanced solution for twisted-pair needs. Or choose our MBL8392A if you need a coax interface.

And used with our MB86953 PC Bus Interface Unit, NICE can further reduce costs and complexity when developing PC XT/AT® adapter cards. Replacing the need for up to ten separate parts.



All in all, NICE has some impressive features to enhance your LAN's entire performance. Such as a data bus transfer rate of 20 Mbytes per second. A low-power standby mode. And bus compatibility for most standard microprocessors.

But what's really nice is our understanding of the marketplace. As Fujitsu's American arm, we know what it takes to get you there a lot faster. With greater cost effectiveness.

So now that the secret is out, call us at 1-800-866-8608. And discover NICE. The world's most advanced, highly-integrated Ethernet solution.

FUJITSU

Delivering the Creative Advantage.

NICE is a trademark of Fujitsu Microelectronics, Inc. XT and AT are trademarks or registered trademarks of IBM Corp. © 1991 Fujitsu Microelectronics, Inc.

FUJITSU MICROELECTRONICS, INC., Advanced Products Division. 77 Rio Robles, San Jose, CA 95134-1807.

CIRCLE 159

Strength In Numbers

The power of dual platforms – more than a promise.

The leading electronics design automation solutions are available today on two industry-leading platforms.

Now DAZIX customers will benefit from products that reside on both Sun and Intergraph workstations. Robust solutions for the entire design process. Plus, an open-system framework that integrates Intergraph, DAZIX, and Sun products – as well as other leading EDA tools – in a simultaneous engineering environment.

Billion-dollar backing.

Intergraph's financial strength gives DAZIX customers an added benefit – confidence. The confidence that comes from a partnership with the only EDA company that is part of a billion-dollar computer graphics corporation. Ranked No. 3 in worldwide EDA sales. With an installed base of 13,000-plus EDA seats and capabilities developed over more than 22 years of providing integrated graphics solutions around the globe.

DAZIX customers are assured of continued product development and excellent support. Not just today and tomorrow, but into the future.

To learn more about our numbers, call us. In the United States, 800-239-4111. In Europe, 33-1-4537-7100. In the Asia-Pacific area, 852-8661966.

CURRENTLY SUPPORTED WORKSTATIONS INCLUDE:

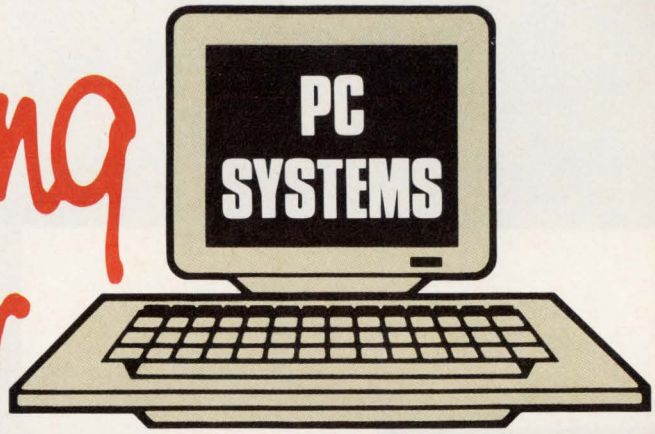
- SPARCstation 2
- SPARCstation IPC
- SPARCstation 1+
- SPARCstation 1
- SPARCsystem 330
- SPARCsystem 470
- InterPro 2020
- InterAct 2020
- InterPro 6040
- InterAct 6040
- InterPro 6240
- InterAct 6240

DAZIX®
An Intergraph Company

Intergraph® and DAZIX® are registered trademarks of Intergraph Corporation. Other brands and product names are trademarks of their respective owners. Copyright 1991 Intergraph Corporation, Huntsville, Alabama 35894-0001. DDAD029A0.

CIRCLE 181

Designing For PC SYSTEMS



Flash Chip Adds Block-Erase Capability

FLASH MEMORY TECHnology will take a step forward with the 28F001BX chip from Intel Corp., Santa Clara, Calif. Its multisize block-erasure capability suits it for updatable BIOS in PCs and updatable firmware in minimum embedded applications.

The 1-Mbit device features an 8-kbyte boot-block section with a hardware-lockout feature to ensure data security and reliability within that block. The boot section is used to recover code storage. Other memory segmentation includes two 4-kbyte parameter blocks and one 112-kbyte main block. The memory chip is organized as 128 kbits by 8 bits and is offered in either 120- or 150-ns-access speeds. The chip is available in two configurations, making it compatible with microprocessors and microcontrollers that boot from high or low memory.

The device can be a replacement for EPROM, EEPROM, or battery-backed static RAM. Its deep power-down mode lowers power consumption to 10 μW when the device isn't in direct use, a crucial feature in portable applications. The blocking scheme of the 28F001BX allows BIOS updates in the main and parameter blocks. The automated erase-and-write capability simplifies device interface and frees the microprocessor to perform other tasks while the flash chip is being programmed or erased. Call Intel at (800) 548-4725. **CIRCLE 510**

Embedded DOS Needs Only 15 Kbytes Of RAM

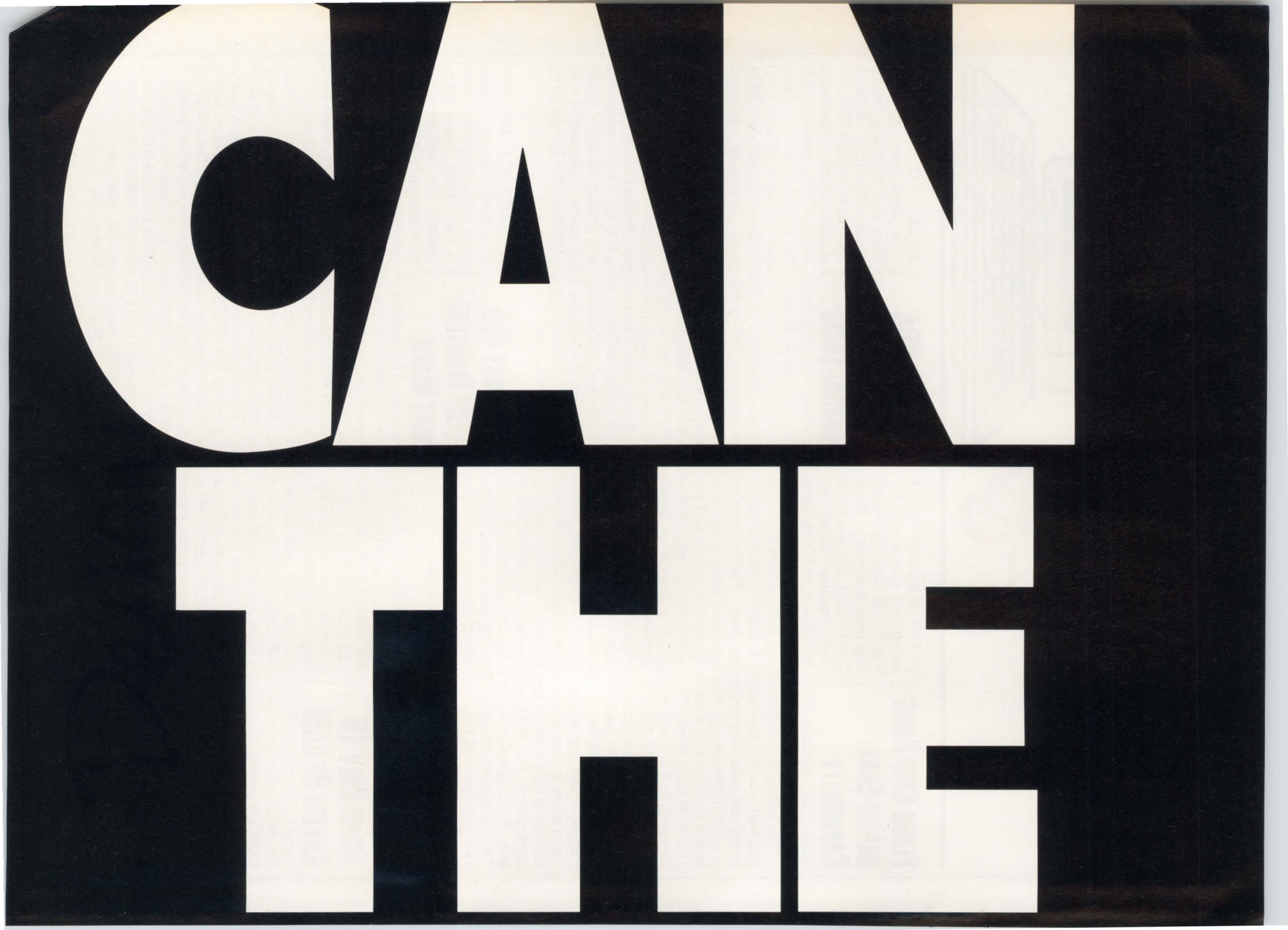
FUNCTIONALLY EQUIValent to disk-based DOS 3.21, the ROM-based MS-DOS 3.22 allows diskless embedded systems to offer full MS-DOS compatibility. The software, by Annabooks Inc., San Diego, Calif., and licensed for distribution from Microsoft Corp., executes out of ROM and requires just 15 kbytes of system RAM (that's 40 kbytes less than the disk-based version) and can be housed in 62 kbytes of ROM space. Licensees to Annabooks can then ship MS-DOS 3.22 in ROMs embedded in their systems. As part of the license, users receive source code for the IO.SYS files so that customized I/O drivers can be written if the system requires a nonstandard interface. A developer's kit containing utilities to create a ROM image file after customization, and ten licenses for MS-DOS 3.22, sells for $595. Additional licenses can be purchased. Contact Jon Choisser, (619) 271-9526. **CIRCLE 507**

High-End VGA Chip Packs All Control Logic

ABLE TO HANDLE video clock rates up to 75 MHz and providing noninterlaced-monitor refresh rates up to 70 Hz, a VGA-level video controller developed by Western Digital Corp., Irvine, Calif., provides IBM XGA-compatible images. The WD90C30 not only produces 1024-by-768-pixel images with up to 256 colors, but can also supply up to 65,536 colors with standard VGA resolutions of 640-by-480 pixels. To ensure high-speed video-data transfers, the chip will offer a 16- or 32-bit memory-interface option and can support fonts with 6 to 16 dots and 132-column text modes. An eight-level-deep FIFO buffer on the memory interface offers some elasticity so that data can be fed into the controller at the bus' maximum rate. When combined with a clock synthesizer (such as the ISC90C63 from ICS Inc.), some wide-word DRAMs, and a palette digital-to-analog converter, a compact board, or a display block can be implemented with less than half-a-dozen chips. Contact John Burger, (714) 932-7312. **CIRCLE 508**

Low-Cost 486 Sheds Floating-Point Math

BECAUSE ALL APPLICAtions don't require floating-point math, Intel Corp., Santa Clara, Calif., has opted to remove the floating-point math unit on its 80486 microprocessor. That enables the company to reduce the chip price considerably and offer system designers a more price-competitive performance upgrade to the 80386DX. The 486SX still offers the full 32-bit bus structure of the standard 486, unlike the reduced bus 386SX, which has a 16-bit data bus rather than the 386DX's full 32-bit bus. To add floating-point capability to systems that incorporate the 486SX, Intel designers created the 487SX. During system design, Intel suggests that an upgrade site/socket be allocated on the pc board so that the 487SX can be plugged in. The 487SX, however, is nothing more than a full 486DX processor with a new package. The 486SX will initially be offered in 20-MHz versions, which makes it possible for the chip to deliver, at a lower cost, a throughput about 135% that of a 33-MHz Intel 386DX CPU with external cache. In lots of 1000, the 486SX sells for $258, while the 487SX has a suggested retail price of $799 in single-unit lots. For more information, contact Intel at (408) 765-8080. **CIRCLE 509**


CAN
THE

Too many oscillator "cans" can litter your board or trash a design altogether.

But no more.

Now, just a single frequency generator from Avasem can replace up to 20 crystals and crystal oscillators. So you can free-up needed board space, reduce power, and drastically lower component costs.

AV9127 Motherboard Frequency Generator. Actual size.

Speeds of up to 110 MHz make our family of frequency generators perfect for motherboards and video graphics. And with power-down features, they're also ideal for laptops.

Our expertise in analog ASICs allows us to quickly customize a frequency generator for just about any application.

So for more information and a free sample, call us toll free now at 1-800-3AVASEM or 408-297-1201. Or write to Avasem, 1271 Parkmoor Ave., San Jose, CA 95126.

And can the can for good.

AVASEM

CIRCLE 127

It's the fastest electrostatic plotter ever built.

Buckle your seat belt and return your tray-table to the full upright position. Because with CalComp's new 68000 Series, 400 dpi color electrostatic plotter, you're going to fly.

Humming under the slick new skins is the latest high performance, RISC-based CPU–processing data faster than ever before.

Plotting speed is awesome too–a head-spinning 2.0 ips.

And with its standard 4:1 mux, concurrent overlap loading–for simultaneous plotting and data processing–and auto take-up reel, the 68000 can speed along virtually non-stop, completely unattended.

Of course, you can run in cut-sheet mode, too.

Plot quality is extraordinary. You get the sharpest lines and most vibrant colors because the system automatically optimizes plotting speed to plot density, and because CalComp's EnviroClean™ Toner System's Auto Replenisher continuously monitors and maintains consistent color density of the toner.

Even with all the high performance features, the 68000 Series is easy to run and maintain. You command all its features from a simple, four-button control panel. And you have front access to toner and media.

Reliability is excellent. And CalComp supports you with a **1-year on-site warranty** and a full line of supplies.

A quick call is all it takes to find out more about the fastest electrostatic plotter: call **800-932-1212.** In Canada, call 416-635-9010.

We're expecting to hear from you.

We draw on your imagination.™

CalComp
A Lockheed Company

CalComp, P.O. Box 3250, Anaheim, Ca 92803. ©1991 CalComp. EnviroClean and We draw on your imagination are trademarks of CalComp.

CIRCLE 96 For Dealers CIRCLE 97 For End Users

The PC as an EDA platform: Is the PC up to the task?

Compared to workstations, the biggest difference is not raw computing power, but the available EDA software.

BY JOHN DURBETAKI
OrCAD, 3175 N.W. Aloclek Dr., Hillsboro, OR 97124; (503) 690-9881.

As technology races forward at dizzying speeds, every aspect of the design process is being challenged. Even though designs are becoming more complex, there's pressure for engineers to reduce design cycles. As this trend continues, today's engineer must ask himself, "Are the electronic-design-automation (EDA) tools, and specifically personal computers, up to the task?" The answer is a qualified yes: The PC is extremely well-suited in certain areas.

Determining what PCs can and can't handle isn't a function of performance, but rather a function of whether the EDA applications software exists and if the particular application can handle the design complexity. In addition to the applications' basic capabilities, the requirements of the design environment must be reviewed to determine workgroup needs, individual needs, and management needs. The design environment can be specified only with a thorough understanding of all the competing needs.

	IC	ASIC	Board
Complex	> 10k gates Mixed signal	> 10k gates	> 16 layers > 32 in. per side
Simple	< 10k gates	< 10k gates	< 16 layers < 32 in. per side

1. Design tasks can be partitioned into three broad categories: IC, ASIC, and board. In each category, there's both simple and complex design.

For example, consider three broad categories of design tasks: IC design, ASIC design, and board design *(Fig. 1)*. Each category can also be partitioned by design complexity: simple and complex. The terms simple and complex cover all aspects of the design category, such as component or gate count, operating conditions, and technology. They also generally reflect the dividing line between the EDA tool requirements in specific areas.

The characteristics of each area in the figure are meant to be general, even though some specific values have been assigned. For instance, a small gate-count IC in an exotic new technology might require using tools typically employed for complex design. Similarly, some tools usually associated with simple designs may be used to design a more complex system by partitioning the design into subsystems. As with any analysis of an object and its boundary conditions, each situation must be carefully reviewed to determine the tools best suited for its design.

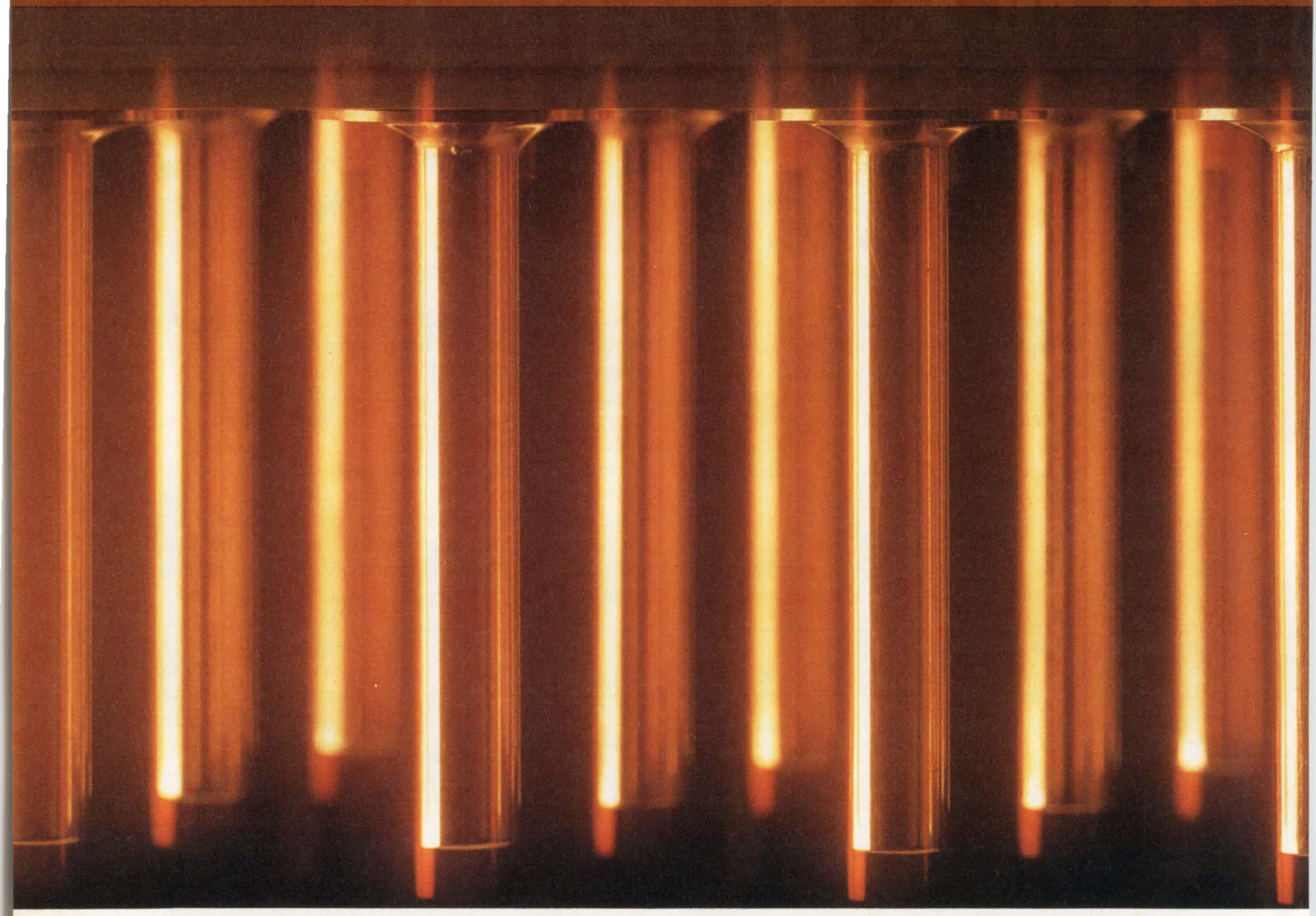
Now consider the relative share of design starts in each of the three categories. This reveals a strong dominance of design classification by design category *(Fig. 2)*. For instance, most IC designs are complex because simple designs are probably more quickly and correctly implemented as ASICs. Moreover, the dominance in ASIC designs is shifting toward complex designs as greater integration occurs and better tools become available. Simple designs dominate in the board area because component densities aren't growing faster than the tools and technology can handle. In addition, as greater integration occurs in the IC and ASIC areas, the component count may actually decline.

Many more board designs than IC and ASIC designs exist. Although the number of IC and ASIC designs is currently growing at a higher rate than board designs, this rate will begin to slow down. After all, every IC and ASIC must be placed on a board at some point. Considering that many designs contain no ASICs or custom ICs, the relationship between pc-board and IC and ASIC designs will stabilize at a 75% to 25% ratio.

Different tools exist for simple and complex IC, ASIC, and board design because there's no such thing as a universal EDA tool. Even though the tool suppliers would like everyone to believe their tools can do it all, reality is that they can't. Just as a Swiss Army knife can remove a splinter from a finger, yet wouldn't be recommended for open heart surgery, a tool that's designed for board layout isn't suited for IC layout. Conversely, a tool supporting the development of a 1-million transistor IC uses a database that exceeds the needs of the designer of a wall thermostat. Similarly, an analog simulator is a poor choice of tool to check the logical function of a PLD design. Tools are specialized so that they may perform the task demanded of them with a greater degree of precision, performance, or quality. As tasks become more sophisticated, tools become less generalized.

Today, the computing platform is split into two broad categories—personal computers and workstations. The

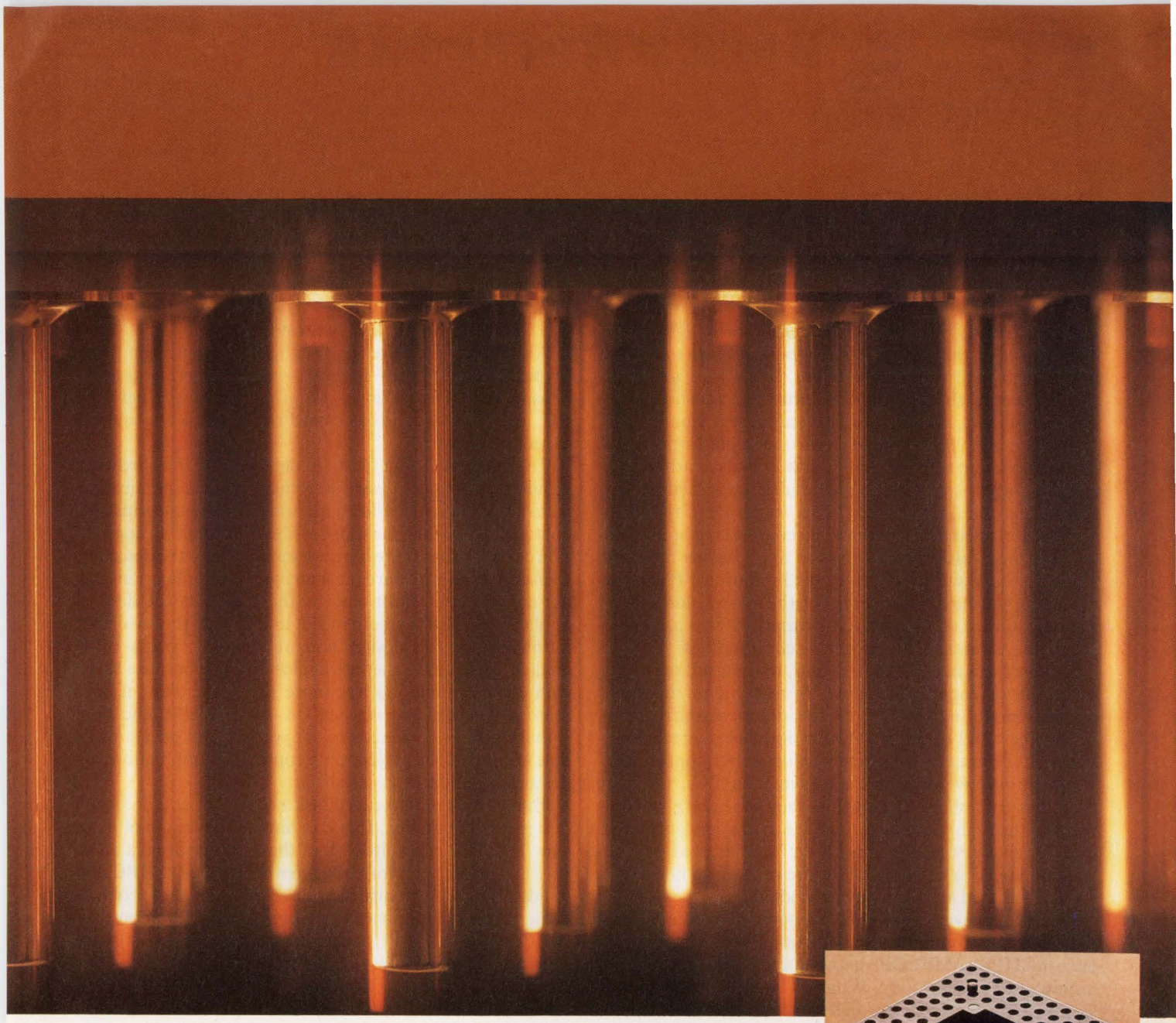
Helping production cope with the pressures of high pincount packages.



THIS IS AMP TODAY.

*J. B. Cullinane, "A User's Evaluation of Pin Grid Array Sockets", *Connection Technology*, June 1990.

AMP is a trademark of AMP Incorporated.

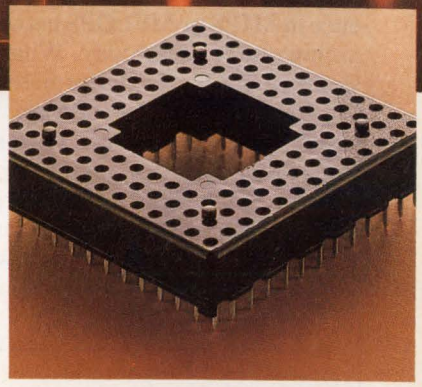


As PGA pincounts go up, so do the insertion/withdrawal forces required to socket them. When counts reach about 121, conventional socket contacts put your total insertion force in the 28 to 50 pound range—hardly conducive to efficient manufacturing.

Not so with AMP LIF PGA sockets. We use a dual-beam contact, and we stagger contact row heights to reduce insertion force requirements dramatically. For the same 121-pin package, our socket design requires an average 13.1 pounds insertion force*, 50-75% lower than conventional sockets. This can make a significant difference in everything from operator fatigue and device stress to board integrity and ease of field service.

And our exclusive design provides excellent normal contact force as well—the contacts utilize a long beam geometry, providing ample deflection with no compromise between normal force and insertion/extraction force.

Sizes: 10x10 to 25x25, with quick turnaround on special patterns. For more information, call the AMP Product Information Center at 1-800-522-6752 (fax 717-561-6110). In Canada call 416-475-6222. AMP Incorporated, Harrisburg, PA 17105-3608.



Dual-beam contact LIF PGA

AMP

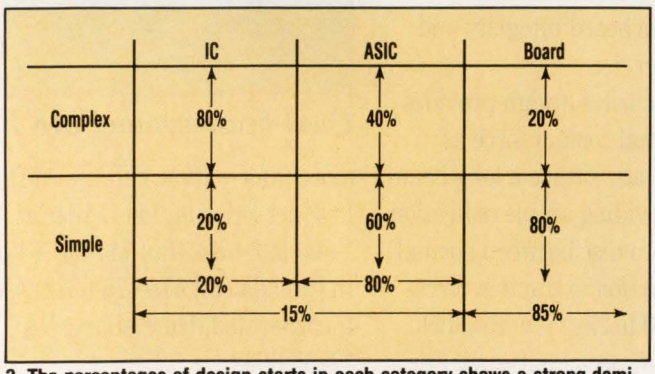
CIRCLE 90

distinction between the two isn't the processor, operating system, graphics support, memory, or supplier, but rather in the way the machine is used. A PC is used by an individual in primarily singular tasks. It may communicate to other PCs or storage areas, but these actions are to support the user's work as an individual. On the other hand, the workstation basically performs group-related tasks. The group interaction of the members is supported by the environment, both hardware and software. Integrating group activities occurs throughout the entire relationship of the group members, and often must occur in real time.

Until recently, categorizing a particular platform as a PC or a workstation was fairly simple. A PC was a rather limited computing platform that had small storage facilities and limited graphics capabilities, supported little of the intensive numerical analysis required by engineering professionals, and had fairly basic software applications often designed to cope with the platform's limitations. It was designed for the masses, supported by the masses, and used by many sectors of the work force. Primarily it was used in offices, laboratories, and engineering communities.

A workstation, on the other hand, was considered to be a much more capable machine. Workstations supported higher computing throughput in numerical analysis and other areas, had larger storage facilities, used virtual operating environments, and had sophisticated applications. Workstations were more expensive than PCs, often by thousands of dollars. In addition, they were designed to be used by the highly computer literate, had applications and operating environments that were complicated and required extensive training, and more often than not were a resource shared among many individuals.

Today, however, these easily recognized traits no longer distinguish the computing platforms. There's little difference in MIPS or MFLOPS between each of the major CPU architectures used today. What difference exists is easily stamped out by the performance differences attributed to the EDA application software. There are machines marketed as PCs and others as workstations that all use the same CPU chip, such as the Apple Macintosh, the Atari Amiga, and the HP/Apollo workstation. In addition, both can be configured with large hard disks, tape backup systems, CD ROM drives, and network interfaces.



2. The percentages of design starts in each category shows a strong dominance of design classification by design category.

Large strides have been made toward better operating environments and graphical user interfaces. Graphics support on PCs has improved in both resolution and drawing performance. On both the PC and the workstation, better human interfaces simplify the human-machine interaction. Examples of this are Windows on the IBM-compatible PC and Open Look on the Sun Sparcstation.

Also, the price difference is negligible between comparably featured systems. While PCs are still generally less expensive than workstations, the price differential between PCs and workstations has closed rapidly and the trend is expected to continue.

The most important factor in determining the hardware required to support design automation is the application software. If an application supports various platforms and configurations, then the range of choice is set. If an application doesn't support the hardware available to the designer, then either the hardware must change, the applications under consideration must change, the vendor of the desired application must be convinced to support the available hardware, or the design and/or design process must change. Most often the last choice is made because there isn't enough money to buy more hardware. Few, if any, reasonable alternative applications are available, and even if the vendor is convinced to support the designer's available hardware, the project time constraints don't allow the designer wait for the application.

Today, PCs can do every task needed for simple board design *(Fig. 3)*. In fact, they can handle the design of most simple ASICs, and a little bit of the complex area in all of the categories. Therefore, the answer that yes, the PC can handle EDA tasks, is qualified based on the type of problem being tackled. For instance, no designer doing a complex ASIC would use a PC today because no EDA software tools are equal to the task.

Generally speaking, the PC has enough horsepower to do most, but not all, electronic design tasks. For instance, a Spice simulation of a 1-million-transistor IC can't be done on a PC. That type of job probably can't even be done on a workstation, but would need the power of a bigger computer. The difference between the PC and the workstation, however, is that the workstation has a link to that bigger computer and the PC generally doesn't.

The chart in Fig. 3 shows which machine dominates in each category of design tasks. For example, workstations can be used to design simple boards even though PCs dominate that area. Today, it's primarily software that situates particular platform-application combinations. Just a few years ago, the hardware would have been the determining factor because PCs had characteristically small resources and low performance, especially to support EDA tools.

A major demand placed on the hardware and software tools stems from the particular design category of the six that were previously discussed. In IC and ASIC design, especially in complex designs, integration occurs throughout the design. A great deal of integration, however, occurs at the end of the design. ASIC and IC integration means connecting various circuits at the transistor level within a product that isn't easily modified. In board design, which

Five ways to look at 100 MHz. Starting at $2295!

Just check the choices in our line-up of five 100 MHz oscilloscopes:

- **GPIB Programmability**
- **Hardcopy Documentation**
- **100 MS/s Single-shot**
- **Automatic Measurements**

Name your application, we'll provide the solution.

Tek gives you the perfect blend of modern analog real-time and digital technologies in 100 MHz oscilloscopes. Whether it's hardcopy output from a fully programmable real-time scope, automatic measurements specified to .001%, or 100 MHz, 100 MS/s single-shot performance, no one has the choices Tek does. To see it all, call your Tek rep or **1-800-426-2200.** The closer you look, the more you'll appreciate Tek.

VISA MasterCard

One company measures up.

Tektronix®

COMMITTED TO EXCELLENCE

Copyright © 1991 Tektronix, Inc. All rights reserved. BOB-137

CIRCLE 99

So would you like the number

Yes, it's true some design teams see us as the emergency number of development systems providers.

Many more, however, use Applied Microsystems more productively by calling us in earlier—at the start of their embedded systems project.

Out of our experience comes tools and support to help your design team work like a team.

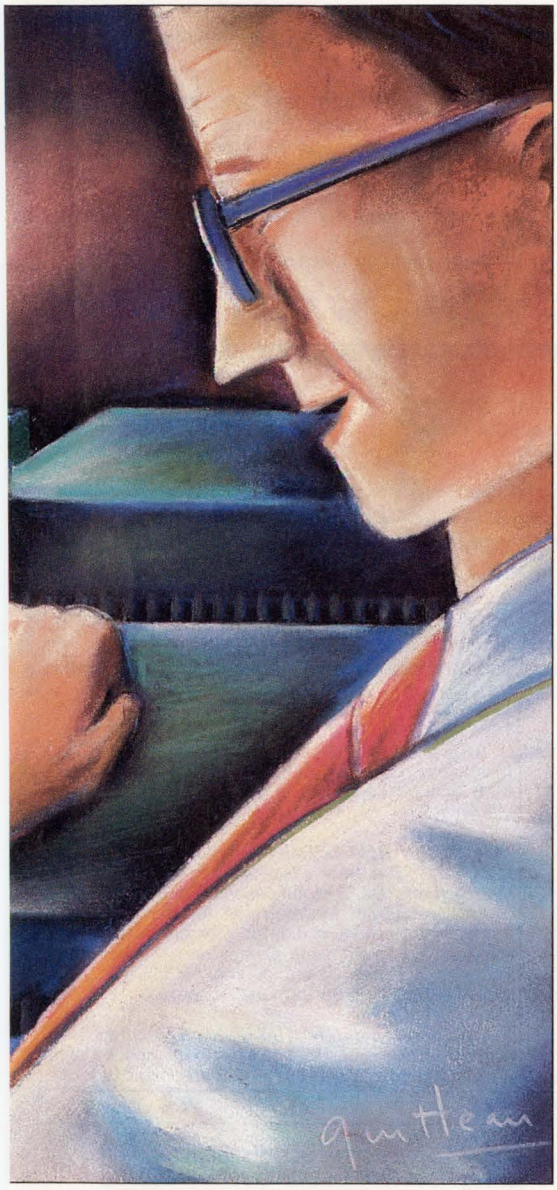
Long before the sirens ever begin to sound.

Development systems for today's embedded systems.

It's getting much more complicated in there. Like, several megabytes of code

©1991 Applied Microsystems Corporation, P.O. Box 97002, Redmond, WA 98073-9702 USA. All rights reserved. AMC-25. Other names indicated by ® and ™ are registered trademarks of their respective holders.

for Applied Microsystems?



in a 32-bit design. Which means more engineers to write it, often within very different, even mismatched environments.

Our modular development system architecture helps bring your design together by integrating your computer environment with our high performance emulators, debuggers, simulators and compilers.

We even offer a networked system for Sun® setups. And a common interface for all our systems for easier 16- or 32-bit development.

All so your design team can begin working like a real team.

We work with the processors you work with most.

Megahertz for megahertz, our tools run with the best, such as the powerful 68020/030 or i960™CA microprocessors.

In fact, we have alliances with Motorola®, Intel®and others. This enables us to deliver fully tested, compatible development systems sooner to support your processor's unique features.

Moreover, supporting your development efforts is our only business. So unlike others who just dabble in development, we have to be better at it.

Which may explain why companies have called upon us to set up over 15,000 development systems worldwide.

Call before your development days are numbered.

It's never too early to talk with us about your upcoming design projects.

In fact, you can start now by calling for our brochure on what you should expect from a development systems company (and can't afford not to get).

Just call 1-800-343-3659 (in Washington, 206-882-2000).

And of course, we'll be happy to take your emergency calls, too.

Applied Microsystems Corporation

Where it all comes together.

For the name of your nearest distributor in Europe, call 44-(0)-296-625462. Europe Fax 44-296-623460. Or contact Applied Microsystems Corporation, Ltd., AMC House, South Street, Wendover, Aylesbury, Bucks, HP22 6EP, United Kingdom. **In Japan, call 03-493-0770.** Japan Fax 03-493-7270. Or contact Applied Microsystems Japan, Ltd., Nihon Seimei, Nishi-Gotanda Building, 7-24-5 Nishi-Gotanda, Shinagawa-KU, Tokyo T141, Japan.

CIRCLE 146

Silicon Valley Personal Computer Design Conference

The Conference on New Architectures and Technology for the Design of Personal Computers

SVPC®

July 8-10, 1991
●
Red Lion Hotel
San Jose, California

SVPC'91 is the only technical conference dedicated to the design of hardware and software for personal computers systems, providing design engineers with SOLUTIONS to many difficult system design and integration problems. Over 100 technical presentations and 10 tutorials will be delivered by well-known professionals amassed from all levels of the personal computer industry, worldwide. SVPC'91 will bring together hundreds of designers and strategic planners to advance the state-of-the-art in desk top computer systems design.

The conference is structured such that the first day, July 8th, will provide 10 four-hour tutorials - 5 in the morning and 5 in the afternoon. The remaining 2 days will present, in 3 parallel technical session tracks, over 100 speakers describing innovative design approaches to implementing high performance desktop and portable systems.

Coffee break refreshments as well as lunches are included in the conference registration. Vendor exhibits showing the latest components for system designers will be open for 2 hours starting at noon on Tuesday & Wednesday. A reception in the exhibits area will be held Tuesday evening.

Monday, July 8th -TUTORIALS- (1 through 5; 8:00 AM - 12:00 PM) (6 through 10; 1:00 PM - 5:00 PM)

TUTORIAL 1 Basic Approaches to PC Caches Intel Corp.	TUTORIAL 2 Portable System Design Issues Intel Corp.	TUTORIAL 3 Multifunction Peripherals National Semiconductor	TUTORIAL 4 Basics of SCSI-1 & SCSI-2 NCR Corp.	TUTORIAL 5 Designing with High Speed PLD Intel Corp.
TUTORIAL 6 BIOS Design Award Software	TUTORIAL 7 Portable Power Technology Gates Energy Products	TUTORIAL 8 Data/Image compression Oak Technologies & Adv. Hardware Architectures	TUTORIAL 9 Integrating SCSI with CAM Ballard Synergy	TUTORIAL 10 Bringing Technology to Market Regis McKenna, Inc.

Tuesday, July 9th, 8:00 AM -OPENING KEYNOTE and TECHNICAL SESSIONS-
"Beyond the Single Chip PC" - Gordon Campbell, CEO, Chips & Technologies Inc.

TRACK I

- DISPLAY BASICS -
CRT Display Technology Directions; Advances in Video RAM Architectures; Advances in RAMDACs and Color Palettes; Where to Put Intelligence in Graphics.

- HIGH PERFORMANCE DISPLAY CONTROLLERS -
Understanding VGA Benchmarks; Implementing Advanced Features in VGA Systems; VRAM-Based Ultra-VGA Controllers; Bringing Workstation Graphics to PCs; Implementing 3D Graphics on a PC Add-in Card.

Above papers by: AT&T Microelectronics; Chips and Technologies; Information Associates; Inmos; NCR; Oak Technology; TI; Yamaha Systems Technology Div..

TRACK II

- MOTHERBOARD DESIGN ISSUES -
PC Chip Set Market Trends: Challenges and Opportunities; Designing High-Integration EISA Motherboards; Implement Compact EISA-Based Systems; A CPU-Speed-Independent Micro Channel Motherboard.

- BIOS AND SYSTEM PERFORMANCE ISSUES -
BIOS Architectural Support for New Chip Sets; Flash Memory: The Ideal BIOS Storage Device; Memory Subsystem Architectural Options; An Algorithm for Dynamic Memory Management; A New Enhanced-Mode DRAM for PC-based Workstations; Smaller, Faster, Cheaper, and Hotter: Thermal Problems and Cooling Solutions.

Above papers by: Intel; NMB; Opti; Phoenix; TI; Toshiba.

TRACK III

- BATTERY-POWERED SYSTEM ISSUES -
Designing Low Voltage Systems; Battery Technology: Current Status and Projections; Clock Synthesis for Laptops; Battery System Management.

- LAPTOP SYSTEM DESIGN APPROACHES -
ROM BIOS: The Best Place for Laptop Power Management; BIOS Modifications/Enhancements for Transparent Power Management for the i386SL; Power Management in Laptop Computers; Power Management in Portable Computers; Managing Power in Systems Based on the AM386DXL; Implementing High-Performance Laptops.

Above papers by: AMD; AT&T Microelectronics; Avasem; Benchmarq Microelectronics; Gates Energy Products; Intel; Phoenix; TI; VLSI Technology.

12:00 PM through 2:00 PM LUNCH AND EXHIBITS OPEN

- ACCELERATING GRAPHICS -
Accelerating 3D Graphics on a PC; Implement an Accelerated Windows Graphics Controller; Apply Multiple Processors to Accelerate GUIs; Accelerate GUIs With Smart Bus Control.

- MULTIMEDIA HARDWARE APPROACHES -
Adding Video to PC Graphics; Low-Cost Approaches to Video Compression; Integrating DSP into PC Systems; Developing Application Processors for Multimedia; Implementing Systems with DVI Technology.

Above papers by: Chips and Technologies; Intel; Inmos; Philips Components (Signetics); TI; Spectrum Signal Processing; Weitek.

- ADVANCED CACHE SUBSYSTEM DESIGN -
Choosing the Right Cache Architecture for PC Applications; 50-MHz Cache Solutions; Hardware-Level Concurrency in a 386/486 Write-Back Cache; Managing Cache Coherency; in Multiprocessing Systems.

- IMAGE AND VOICE I/O -
Apply Sampled-Data Storage for PC Analog I/O; Designing High-Speed Modems; Modular Modem Design - A Flexible Solution; Image Communications With PCs; Designing A Combination PC-Fax, Modem, and Voice-Mail Card.

Above papers by: AT&T Microelectronics; Chips and Technologies; Intel; Information Storage Devices; Mosel; National Semiconductor; Opti; TI; Yamaha Systems Technology Div.

- PORTABLE SYSTEM DESIGN ISSUES -
Designing a Two-Chip Notebook PC; Creating State-of-the-Art Notebook Computers; Building a Single-Board SPARC-based Laptop/Desktop Computer; Combining the EISA Bus and the M88000 RISC to Build Single-Board Systems; Memory Management Techniques for Laptops.

- 4:00 PM Panel Discussion -

Above papers by: Chips and Technologies; LSI Logic; Motorola; Oak Technology; VLSI Technology.

5:00 PM EXHIBITOR RECEPTION/EXHIBITS OPEN

Technical Sessions continued on next page

Sponsored by SysTech Research in cooperation with Electronic Design (a Penton publication), Intel Corp., NCR Corp., NMB Technologies, and Yamaha Systems Technology Div.

Wednesday, July 10th, 8:00 AM -OPENING KEYNOTE and TECHNICAL SESSIONS-
"The 10 PCs You'll Never See" - Mike Aymar, VP & General Manager, Microcomputer Div., Intel Corp.

TRACK I

- FLAT PANEL BASICS -
Flat Panel Design Options; Flat Panel Displays for Portable Systems; CGA Graphics for Handheld/Low-end Portables; Controlling Full-Color VGA Flat Panels.

- DEALING WITH GUIs -
A High-Speed Video Digitizer for the Apple Macintosh; System Software Needs of the new Operating Environments: OS/2 and Windows; Designing a CAD Toolkit to Run Under Windows; Developing FAX Communication Interfaces Under Windows; Creating Multifunction User Interfaces; Controlling Instruments Through Windows.

Above papers by: Chips and Technologies; Gebala Systems; Information Associates; QuickLogic; Logical Services; National Semiconductor; Phoenix Technologies; Stanford Resources.

TRACK II

- EXPANSION-BUS ISSUES -
EISA Add-on Card Design - Shaking the AT Mentality; System Design Issues for Intelligent EISA/MCA Cards; A RISC-based I/O Processor for PC Architectures; Increasing I/O Performance in PC Architectures; An Extended Local Bus Architecture for Better System Performance.

- HIGH-PERFORMANCE SYSTEM ISSUES -
Clock Distribution for High-Performance PCs; Care and Breeding of High-Speed Clocks; Applying System-Level Simulation When Designing ASIC Based PC Systems; Streamlining High-Speed System Design With Transmission Line Analysis; Computer-Aided Prototyping For Concurrent PC System Design.

Above papers by: Bull-Micral; Chips and Technologies; EliteGroup Computer Systems; Intel; Quantic Laboratories; QuickTurn Systems; Silicon Systems; Texas Instruments; VLSI Technology.

TRACK III

- NETWORKING -
Putting FDDI on a PC-AT Half-Card For Single Attachment Stations; Interface Ethernet to the EISA Bus; Customizing a LAN Controller For a Single-Chip Solution; Direct Bus Mastering in PCs Improves LAN Performance; Take Advantage of Specialty Memories When Building LAN Interfaces.

- DATA COMMUNICATIONS AND MASS STORAGE -
Employ Serial Packet Controllers for Flexible Protocol Control; Designing Appletalk-Compatible Serial Interfaces; Large Capacity Back-up Systems for Networked PCs/Workstations; Magnetic and Optical Drive Technology: Current Status and Future Directions; Flash Memory: The Optimal Technology for Solid-State Disks; SCSI RAID Subsystems for Redundant, High-Performance Mass Storage.

Above papers by: AMD; Intel; Integrated Device Technology; Maxtor; NCR; Plus Logic; PureData Research/USA; R-Byte; Silicon Systems; Zilog.

12:00 PM through 2:00 PM LUNCH AND EXHIBITS OPEN

- DISPLAY SUBSYSTEM DESIGN -
Local Bus Support for Video Systems; Selecting the Right Bus Interface for Video; Get High-Performance Graphics with Reprogrammable Logic; Developing Low-Cost Bus and Video Timing Control for Apple Macintoshes.

- I/O DEVICE DESIGN -
Reconfigurable Monitor Design Considerations; Designing High-Speed Control Logic With Reprogrammable Logic; Low-Cost Closed-Loop Controllers For Better Printer Accuracy; Designing Custom Keyboards and Interfaces; Evaluating and Testing Keyboards for PC Compatibility.

Above papers by: Cirrus Logic; Highgate Design; Hewlett Packard; HTE/HiTech Equipment; Oak Technologies; Micron Technology; NMB Technologies; Radius and Xilinx.

- APPLYING PROGRAMMABLE LOGIC -
Design Flexible Micro Channel Interfaces with Programmable Logic; Consolidating System Logic With PLDs; High-Density PLDs Simplify System Design; Apply FPGAs To Simplify Add-in Card Logic.

- EMBEDDED PCs FOR REAL-TIME SYSTEMS -
Real-Time Operating Systems for High-Performance Desktop PCs; Turning the PC into a Real-Time Machine; Using the PC/AT Architecture in Embedded Systems; Designing A Real-Time I/O Controller Card for the PC; Linking the Macintosh and VME environments for Real-Time Applications.

Above papers by: Actel; Altera; Ampro Computers; Intel; Lattice Semiconductor; Lynx Real Time Systems; Ready Systems; Nauchny Center, Moscow, USSR; YARC Systems Corp.

Technical Program subject to change

- MASS-STORAGE CONTROL -
SCSI Host Adapter Performance Trends - Using Intelligent OS Caches; Designing an Optimized SCSI Host Solution; Designing RISC-based Caching SCSI Disk Controllers; Tuning Storage Subsystem Drivers for Multi-Threaded Operating Systems.

- MASS STORAGE -
Optimization of I/O Subsystems in an EISA-Based File Server; Write Caching - New Drive Caching Schemes for Higher Performance; Applying the Power-Saving Modes Embedded in Low-Power IDE Disk Drives; System Compatibility Software Design for PCMCIA/JEIDA Memory Card Applications; PCMCIA System Interface Overview for Memory Cards.

Above papers by: Adaptec; Chips and Technologies; Databook; Intel; Interphase; Maxtor; Quantum; Storage Dimensions; VLSI Technology.

FOR MORE PROGRAM INFORMATION CONTACT: Dave Bursky, Chairman SVPC'91 Technical Program. Voice: 408/441-0550, Email: 76366.553@Compuserve.com

FOR EXHIBIT INFORMATION CONTACT: Ken Majithia, General Chairman SVPC'91 Voice: 408/924-3930, FAX: 408/997-8265, Email:majithia @calstate.bitnet

FOR HOTEL RESERVATIONS:
Call or FAX the Red Lion Hotel and ask for special SVPC'91 rates
Voice: 408/453-4000
FAX: 408/437-2899

REGISTRATION APPLICATION FORM

(Please retain a copy for your records)

	Before 5/24/91	Before 6/23/91	At the door registration	Registration Amount *
Monday, July 8, 1991 **(Select Two Tutorials) Circle One PM & One AM: (1) (2) (3) (4) (5) PM: (6) (7) (8) (9) (10)** . . . . . (Includes Short Course Handout Notes, Coffee Break Refreshments, Lunch, and Tuesday Evening Reception)	$225	$250	$275	$_____
Tuesday, Wednesday, July 9, July 10, 1991 **(All Technical Sessions, No Tutorials)** . . . . . (Includes Conference Proceedings, Coffee Break Refreshments, Lunches, Exhibits and Reception admission)	$295	$345	$400	$_____
Three Day Package: Monday - Wednesday, July 8-10 **(Two Tutorials & All Technical Sessions) Circle One PM & One AM: (1) (2) (3) (4) (5) PM: (6) (7) (8) (9) (10).** . . . (Includes all materials of both Short Course and Technical Sessions as described above)	$350	$395	$450	$_____
Extra Proceedings (at conference, if mailed add $15 postage and handling fee)	$95	$125	$150	$_____

* **A $50 processing fee will be charged for registrations cancelled before June 23, 1991. No refunds after June 23.**
** **Deduct 10% from the total cost if registering 5 or more persons from one company with one company check. This option voids all other discounts.**

TOTAL ENCLOSED ** $_____

Name_____ Telephone_____ FAX_____

Company_____ Mail Stop _____ Email_____

Address_____ City_____ State_____ Zip_____

Make checks payable to SysTech Research and mail with a copy of this completed form to: SysTech Research, 1248 Olive Branch Lane, San Jose, CA 95120

Charge to my ☐ MasterCard ☐ VISA MO. YR.

Account # Exp. Date

Signature _____

includes system design using a number of boards, integration occurs primarily at the beginning of the design cycle. Here, the interfaces between the boards or subsystems are defined. Some integration occurs at the end when the completed subsystems are connected and verified, but most integration is at the beginning.

When the work group requires real-time integration of the design, as in the case of complex IC and ASIC designs, highly integrated hardware and software tools are needed to improve productivity because the group's interaction has such a great impact on the design, schedule, performance, quality, and other aspects. When the group is small, or when the design contains a defined module-interface specification, group interaction has a much smaller impact than individual productivity.

This doesn't mean that group- and personal-oriented tools, both hardware and software, shouldn't be employed in some areas of design. After all, it's not the tool that determines which type of tool should be used, but rather the task to be accomplished. Tools are often thought of as the end rather than the means to the end, perhaps because they were so difficult to operate. The design process and its relationship to the tools is changing, however, as the hardware and software tools change.

What, then, is needed for the PC to start handling more complex tasks? The applications, operating systems, and network software have to change. They must all move toward supporting a group work environment. For example, the network software must let the applications talk to each other across the network in a sophisticated manner. Today, the PC is inappropriate for handling some tasks because they aren't individual-oriented tasks.

Some tasks are group-oriented because of how the system is put together, and how the people who work at developing that system interact. A multitasking operating environment is needed for group-oriented design because it lets people share work and information. This is possible on the PC today, but there's much room for improvement. Also, large design groups need to interact with the database. And designers need more than just the ability to run an application; they need to develop new applications and to run applications that may require more computing resources than they have on their desk.

For these reasons, the network is becoming just as important as the computer. Each designer needs his own machine, but must interact with all of the other individuals. This setup requires an operating system with interconnectivity and interfacing, requirements that DOS doesn't handle well. DOS is a one-person, one-machine, one-task system. Windows 3.0, considered by many to be the successor to DOS, is a step in the right direction but presently isn't up to task to solve all of the problems with DOS. For example, to use the 32-bit operating mode of the 80386 and 80486, the application developer must resort to using clumsy and often poor-performing DOS extenders to fit 32-bit applications into a 16-bit operating environment. Therefore, when the application developer is faced with large data spaces, natural and native support for this problem aren't available. Fortunately, this PC limitation occurs only in the complex, not the simple, design area.

	IC	ASIC	Board
Complex	Workstation	Workstation	Workstation PC
Simple	Workstation PC	Workstation PC	PC

3. This chart, which illustrates the dominating platform in each of the categories, shows that PCs are suitable for many design tasks.

Frameworks are important to this discussion because they manage the design process and the applications used in those processes. Applications are the key to making the PC succeed as an EDA platform. Therefore, the more that the framework and the applications can remove the burden of the tedious tasks, (such as integrating and interfacing tools), the more the productivity is enhanced. Frameworks, of course, need time to mature and develop. It's such a large and complicated task that the industry can't develop a solution all at once. Using the goals and standards now being developed by the CAD Framework Initiative, implementation will be many years away.

Although things like frameworks are the means to the end, they certainly aren't the end. And there are more tasks to be solved beyond those the frameworks will solve. One set of tools can't meet the needs of both group- and personal-oriented environments now, but large strides have been and will continue to be made toward both group and individual productivity. The goal is being approached from a number of different angles. Rapid progress will continue as long as standards and practices allow room for experimentation and change. This sounds quite disconcerting to the users that endure every change. It would be wonderful if anyone could design the product that doesn't need to change, but it hasn't happened yet and it's not likely to happen. But all isn't as discouraging as this last statement indicates. The progress made in design automation has shown many improvements. Future design environments will see just as dramatic improvements.

John Durbetaki, chief executive officer of OrCAD, received a BEE from the Georgia Institute of Technology, Atlanta.

HOW VALUABLE?

HIGHLY CIRCLE 541
MODERATELY CIRCLE 542
SLIGHTLY CIRCLE 543

Designing For PC SYSTEMS

Build A Speedy Low-Cost Graphics Accelerator In Hardware

An Efficient Design Puts Repetitive Functions In Hardware For Fast Operation.

BY PHIL MATTISON

VLSI Technology Inc., 8375 S. River Pkwy., Tempe, AZ 85284; (602) 752-6174; Fax (602) 752-6000.

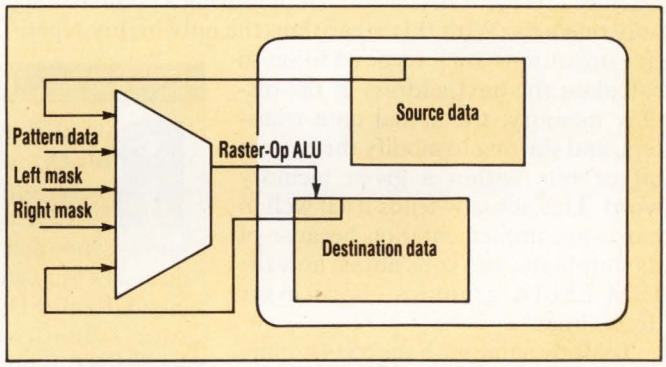
The surging popularity of user-friendly interfaces with bit-mapped graphics continues to push designers to improve graphics performance and trim hardware cost. And, thanks to technology advances, the chips that induce graphics in workstations and PCs keep growing more powerful, more compact, and less expensive. These hardware developments mean that designers can build a high-performance, low-cost graphics subsystem using off-the-shelf components, such as VLSI Technology's Raster-Op ALU chip, and a graphics controller, like Texas Instruments' TMS34061 chip.

Understanding today's graphics hardware depends on knowing some graphics history. Early PC graphics adapters, such as the Color Graphics Adapter (CGA), were simple bit-mapped display controllers without hardware-assisted drawing functions. To speed certain drawing operations, the Enhanced Graphics Adapter (EGA) incorporated bit-masking and color-compare functions.

The Video Graphics Array (VGA) went a step further by arbitrating automatically between CPU and CRT controller access to display memory. This arbitration relieved the software of polling for a vertical retrace interval, thus avoiding "snow" on the display caused by CPU access during active video intervals. This did little to improve performance, however, because the processor still had to wait for a retrace interval.

The first departure from this architecture came with IBM's 8514A chip, the first truly independent graphics coprocessor. The 8514A coprocessor includes a line-drawing engine, which implements Bresenham's line-drawing algorithm in hardware, as well as automatic bit-block transfers (BitBLTs). Texas Instruments' 34010 family supplies similar functions but with more flexibility. The 34010's low-level graphics functions are programmable while the 8514A has a fixed function set. Both chips can operate independently of the host CPU. If software exploits this capability, the independent operation can afford parallel processing. Unfortunately, the 8514A's software drivers don't take advantage of independent operation—they simply wait for each operation to finish.

To attain independent operation, designers use a wide variety of schemes in non-PC graphics subsystems, from window priority controllers to completely independent display list processors. To supply more display-memory bandwidth to the CPU, many makers of after-market, or clone, VGA equipment added FIFO data buffers and dual-port video DRAM, among other components.



1. In a graphics subsystem, source, destination, and pattern data may be combined and modified by mask information in the Raster-Op ALU. Pattern data can be stored in an internal register or be read from memory.

Designers of graphics subsystems must make trade-offs between cost and performance. Analyzing the software that drives the system is the best way to identify graphics functions for which hardware enhancement yields the greatest performance increase relative to cost. Highly repetitive low-level functions are usually the best candidates for hardware enhancement. In the single-user world, the most common graphics-related applications are computer-aided design and desktop publishing.

The most routine graphics operations are line drawing and BitBLTs. Almost any bit-mapped screen display can be drawn using these two operations, and the algorithms for their implementation are well-defined. Of course, other more specialized drawing operations exist, such as ellipses or circles and arcs (actually just special cases of the ellipse). These are less common, and although the ellipse algorithm isn't much more complex than the line-drawing algorithm, it can be implemented using short line segments.

If there's no special hardware to enhance drawing operations, the two factors that have the most effect on drawing speed are the efficiency of the drawing algorithm and display memory's accessibility to the CPU. As noted, CPU accessibility was already addressed in many after-market VGA products. The venerable basic drawing algorithms are probably about as refined as they're ever likely to be.

Line drawing is almost always implemented using Bresenham's algorithm, which involves calculating a pair of increment/decrement values and an initial accumulator value, and then stepping a pointer along the X or Y axis. A pixel is plotted at each location, and depending on the value in the accumulator, the other axis pointer is advanced.

The accumulator is incremented or decremented depending on whether the minor axis pointer was incremented. The relative frequency with which the value in the accumulator crosses zero determines the line's slope. Lines can be plotted at any angle this way. Horizontal and vertical lines represent the trivial case of moving a pointer along only one axis. With this algorithm, the only highly repetitive operations are integer addition to calculate the next address in the display memory, the actual data transfers, and shifting to modify the correct bit or bits within a given memory word. This actually lends itself well to hardware implementation because of its simplicity, and is, as noted, how the IBM 8514A graphics coprocessor draws lines.

To draw a line with the 8514A chip, the software must calculate the initial accumulator value and increment values, load registers with these values, and write a control word to start the drawing engine. Another common operation is the BitBLT, which simply involves moving memory words from one rectangular region to another and possibly combining or modifying them. This may be completely within display memory or between display memory and some other memory, such as CPU memory. In many cases, display memory appears simply as a special area within the CPU address space, so there's nothing unique about such transfers. If the boundaries of the source and/or destination regions of a BitBLT don't fall on memory word boundaries, it becomes necessary to concatenate and shift the data, and possibly mask it at the boundaries.

It may be desirable to perform logical operations between source and destination data, which introduces other special cases that must be handled. Here the programmer is faced with a trade-off. If the BitBLT is to be implemented as one routine, it's necessary to place some kind of selection procedure within the innermost loop so that the right operation is performed. Even if this is only an indirect jump, the performance may suffer because it's so repetitive. The other alternative is a complete BitBLT routine for each function desired, but that's at the cost of memory space and flexibility. A third alternative—self-modifying code—is generally shunned these days because of its nasty debugging nature.

BitBLT is probably the best candidate for hardware acceleration because it affects the maximum number of pixels. To draw a diagonal line across a rectangle M by N pixels requires modifying only the number of pixels in the major axis. A BitBLT requires modifying a number of pixels equal to M times N. Naturally, the extent to which hardware enhancement is used depends on the intended market. If a designer wants to fill the entire gap between high-end PC systems and low-end workstations, the obvious target is

PROGRAMMING THE RASTER-OP CHIP

Registers in the VL16160 Raster-Op ALU need be loaded only once to perform a BitBLT operation using any logical function over any block of data *(see the figure)*. The VL82C164 Quad Raster-Op ALU consists of four identical sections. The VL68C160 Single Raster-Op ALU is identical except that the pattern-input register can't concatenate and shift.

The actual processing of data involves only address calculation and read/write access to the frame buffer. Calculating the values for the shift and mask registers is essentially the same as for a strictly software implementation. In addition, the shift value register also has a bit that controls the direction of processing. This doesn't mean that it controls the direction of shift for aligning source data to the destination. It controls only whether source data words are concatenated from right to left or left to right.

Conceptually, source alignment is always done by shifting a 32-bit value (composed of the current data word concatenated with the previous data word) to the right by a bit count specified in the shift value register and by extracting the rightmost 16 bits. The amount of shift is determined by finding the horizontal distance of the block transfer in pixels, dividing by the word size, and taking the remainder. The mask registers are used when the destination's left and/or right boundaries don't fall on word boundaries in memory. Each bit set to a one in a mask register allows the corresponding bit of the desti-

TABLE 1.

Strobe	Width	Op-Count	Row	Column	Mask
LS	3	3	1	1	unknown
LD	3	2	1	1	1
AO	3	2	1	1	1
LS	3	2	1	2	1
LD	3	1	1	2	none
AO	3	1	1	2	none
LS	3	1	1	3	none
LD	3	0	1	3	none
AO	3	0	1	3	none
LS	3	0	1	4	none
LD	3	3	1	4	2
AO	3	3	1	4	2
LS	3	3	2	1	2
LD	3	2	2	1	1
AO	3	2	2	1	1
and so forth					

TABLE 2.

Pattern	Source	Destination	Function bit	
0	0	0	0	(LSB)
0	0	1	0	
0	1	0	0	
0	1	1	0	
1	0	0	0	
1	0	1	1	
1	1	0	1	
1	1	1	1	(MSB)

the mid-range point for both price and performance. A more rational tactic is to improve performance as much as possible with a minimal increase in cost.

The more software functions are moved into hardware, the less performance gain is available from each hardware dollar. When implemented in hardware, only the simplest, most repetitive functions can offer significant performance gains without major cost increases. A good example is the character generator incorporated into even the most primitive display adapters. Only in recent years has the traditional hardware character generator been considered inadequate for many applications. Interestingly, the BitBLT function replaces the hardware character generator.

The BitBLT algorithm for a rectangle with corners at (X1,Y1) and (X2,Y2) looks something like this:

Calculate horizontal word count: Abs(X2–X1)/word width

Determine shift value: Remainder(Abs(Xsource–Xdestination)/word width)

Set right and left mask values (for nonaligned boundaries)

For each row,

Concatenate first- and second-source memory words

Shift concatenated data

Mask shifted source data

Combine source with destination data using desired function

Write new destination word

nation data to remain unchanged.

The mask-1 register masks the first word in a scan, and the mask-2 register masks the last word in a scan. The relationship between the width register and the op counter that controls the mask registers goes as follows:

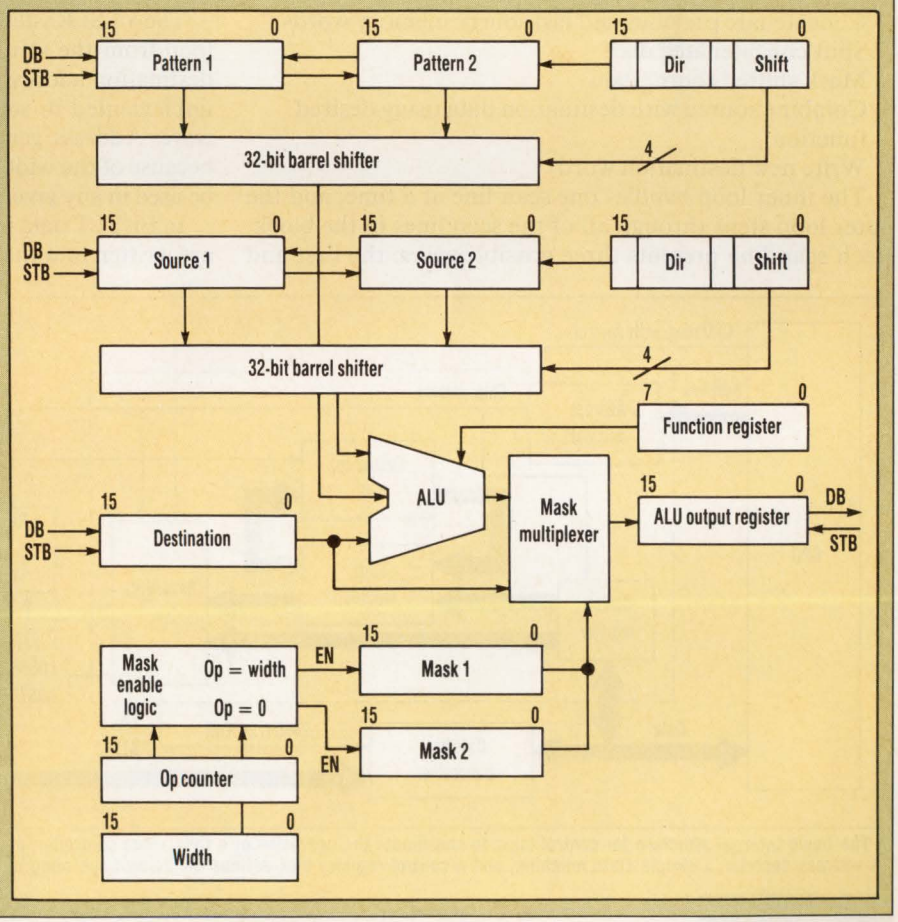
At the beginning of the destination strobe, the op counter is compared with the width register. If they're equal, mask 1 will be applied to the destination data on the next output, and the op counter will be decremented. If the op counter is zero, mask 2 will be applied to both the destination data on the next output and the op counter loaded with the value in the width register.

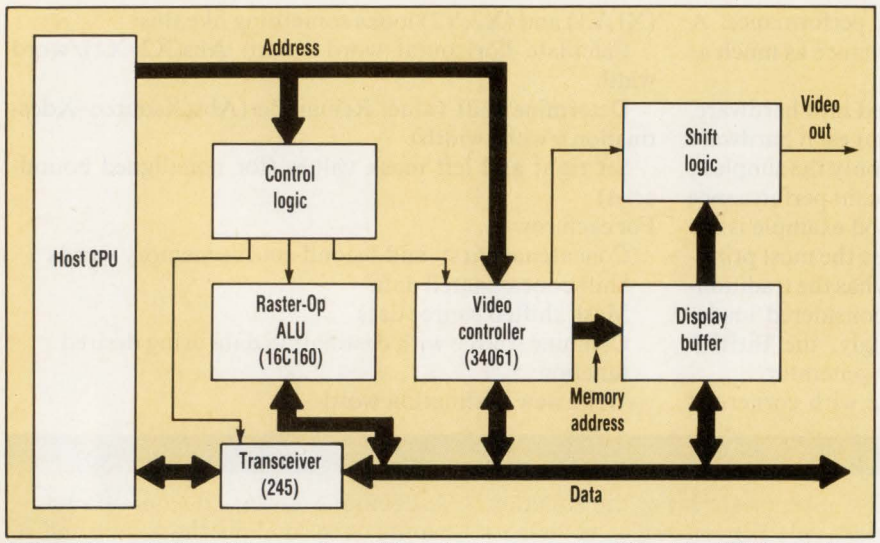
In all other cases, the op counter will be decremented, but no mask will be applied to subsequent output. The width register should be programmed with the number of words to be transferred for the scan line, including masked words, minus one.

The op counter should be initialized to the same value. The sequence for a block of data four words wide, first and last words masked, second and third words unmasked is illustrated in *Table 1*.

The only remaining register that requires initialization is the function decoder. The internal ALU is actually a group of 16 one-of-eight selectors, controlled by bits from the source, pattern, and destination registers. The desired output for any given combination is programmed by setting a one or zero in the appropriate bit of the function register. For example, to implement the function (source + destination) * pattern, the truth table would be used *(Table 2)*.

The value programmed into the function register then would be E0 hex. If the pattern in this example was alternating ones and zeros (say 5555 hex) and inverted on each successive scan, the net effect would be to combine the source and destination images and convert any solid pixel areas to a sort of halftone. A typical programming technique is to define the required function values in advance for each type of BitBLT anticipated and simply to select the function codes from a table as needed.





2. The video controller in this example graphics subsystem generates all the video DRAM control signals and multiplexes the row and column addresses.

For intermediate memory words,
Concatenate next and previous source memory words
Shift concatenated data
Combine source with destination using desired function
Write new destination word

Concatenate previous and last source memory words
Shift concatenated data
Mask shifted source data
Combine source with destination data using desired function
Write new destination word

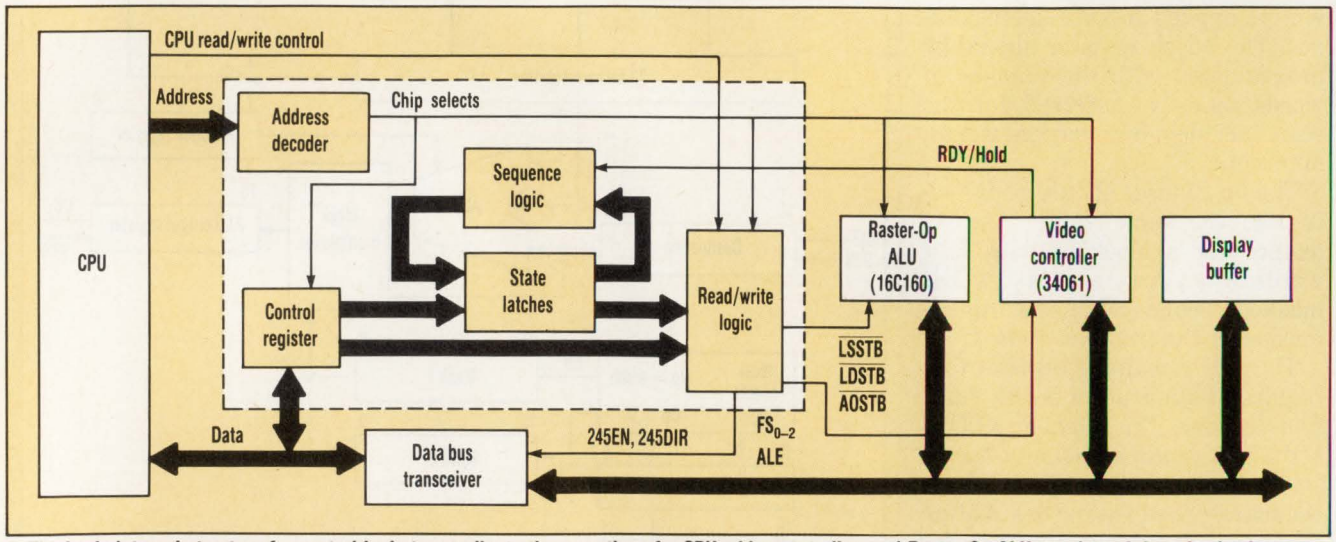
The inner loop handles one scan line at a time, and the outer loop steps through all of the scan lines in the block. Each scan line presents three possible cases: the first and last bytes, which may or may not have to be masked; and the intermediate bytes, which are simply shifted for alignment and written to or combined with the destination.

Much more complex is a general-purpose routine that handles copying over the destination and logical combinations, such as AND, OR, XOR. It also incorporates a second source of data for such things as background patterns. Using multiple bit planes as separate image planes or as encoders for color information further compounds the complexity.

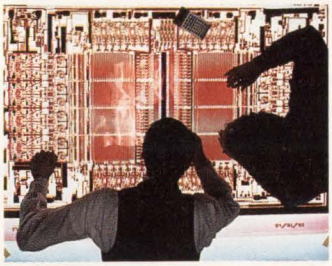
A good hardware solution should implement the algorithm's inner loop so that the most repetitive operations are done with the most speed. A high-speed data path is necessary so that the system can use the full bandwidth of display memory. The hardware should apply masking at the boundaries automatically because this decision process is part of the algorithm's inner loop. As always in hardware design, including more functionality involves a trade-off between flexibility and complexity. As a result, designers must carefully consider the potential applications.

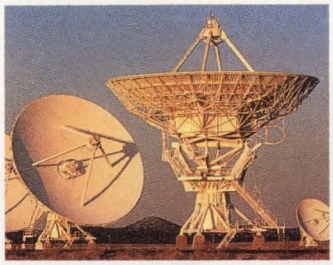
The VLSI Raster-Op chips incorporate most of the inner loop from the sample algorithm. Generating source and destination addresses must be done externally and can be implemented in software or with relatively simple hardware. Address generation is left as an external function because of the wide variety of memory schemes that could be used in any given display system.

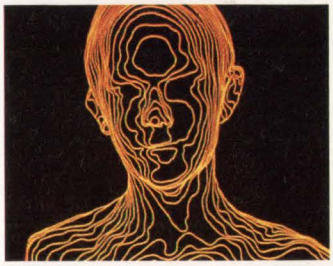
In BitBLT data flow, source and destination data words are written into the chip's internal registers, and the ALU



3. The basic internal structure for control logic to coordinate the operation of a CPU, video controller, and Raster-Op ALU consists of three basic elements: an address decoder, a simple state machine, and a control register that defines the current operating mode.







WHO NEEDS THE SIGNAL PROCESSING WORKSYSTEM?

Anyone involved in DSP and communications design can benefit from the Signal Processing WorkSystem.® Because SPW™ is the only complete, integrated CAE software tool for signal processing design, simulation, analysis and implementation.

Satellite communications. Modems. Mobile radios. Cellular phones. Radar. Sonar. Speech encoding. Voice processing. Image processing. Digital audio. Multimedia. Automotive electronics. Robotics. Neural nets and pattern recognition. Data compression. HDTV. Biomedical instrumentation. All these and much more can be designed using SPW on industry-standard platforms from Sun, DEC and HP/Apollo.

That's why over 200 of the world's leading telecommunications, aerospace and electronics companies around the world now use SPW.

With SPW you first create a high-level, hierarchical design using its extensive libraries of DSP and communications function blocks, as well as your own custom blocks. SPW then automatically converts your design into an error-free simulation program that can accept real-world signals and parameters for accurate design analysis.

SPW also provides several optional paths to implementation, including bit-accurate fixed-point simulation, VHDL generation, logic synthesis and other ASIC/PCB support. A code generation system produces generic-C for fast prototyping on any DSP platform, links SPW to DSP chips from AT&T, Motorola and TI, and supports boards from leading vendors.

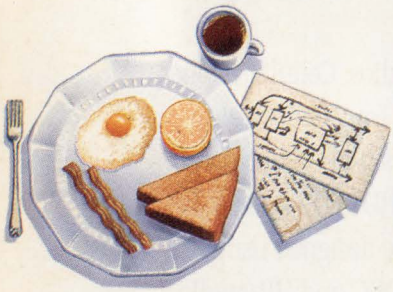
To preview the Signal Processing WorkSystem, call (415) 574-5800 for a free video demonstration tape. In fifteen minutes, you'll see how SPW can save hundreds of hours and thousands of dollars in DSP design.

COMDISCO®
SYSTEMS, INC

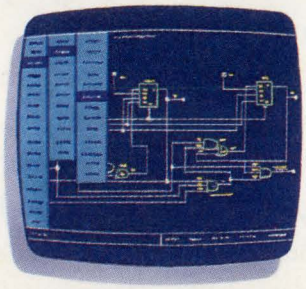
919 East Hillsdale Blvd., Foster City, CA 94404 (415) 574-5800

CIRCLE 142

Be Brilliant At In Productio

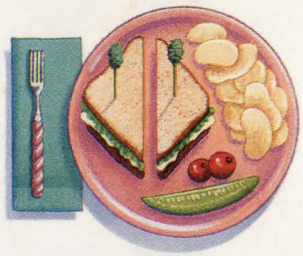


7:05 am: Breakfast
Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



8:50 am: Design
You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.

11:00 am: Place & Route
You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm: Lunch
Remember lunch? Normal people actually *stop working* and have a nice meal—right in the middle of the day! With Actel's logic solution, this could become a habit.

Actel Field Programmable Gate Array Systems.

They're a feast for your imagination.

Actel's ACT™ 1 arrays bring you a completely new approach to logic integration. Not just another brand of EPLD, PAL® or LCA™ chips. But true, high density, desktop configurable, channeled gate arrays.

They're the core of the Action Logic System, Actel's comprehensive design and production solution for creating your own ASICs. Right at your desk. On a 386 PC or workstation. With familiar design tools like Viewlogic,™ OrCAD,™ and Mentor.™

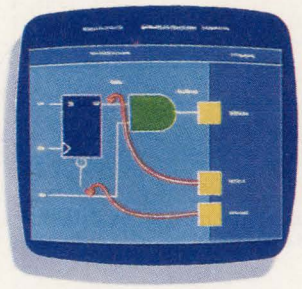
And do it in hours instead of weeks. Even between meals.

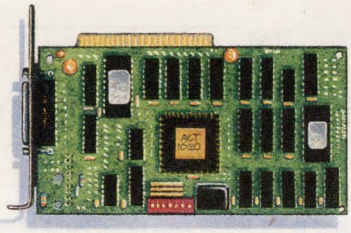
How? With features like 85% gate utilization. Guaranteed. Plus 100% automatic placement and routing. Guaranteed. So you finish fast, and never get stuck doing the most

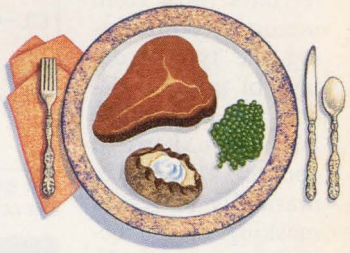
Actel FPGA Product Family		1010A	1020A
Equivalent Gates	Gate Array	1200	2000
	PLD/LCA	3000	6000
User I/O		57	69
System Clock (MHz)		20-40	20-40
Availability		NOW	NOW
Technology (micron)		1.2	1.2

CIRCLE 117

Breakfast And n By Dinner.







1:15 pm: Program
You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure." Take a very quick coffee break while your design becomes a reality.

1:25 pm: Test
You do a complete, real-time performance check, with built-in test circuits that provide 100% observability of all on-chip functions. *Without* generating any test vectors.

4:00 pm: Production
Your pride and joy is designed, created, tested, and off to the boys in Production. And you're finished *way* ahead of schedule! Better think of something to do until 5:00.

6:00 pm: Dinner
Remember dinner? Normal people actually *go home* and eat with their families. On your way, start thinking about how Actel's logic solution can help you be brilliant tomorrow.

tedious part of the job by hand.

Design verification is quick and easy with our Actionprobe™ diagnostic tools, for 100% observability of internal logic signals. Guaranteed. So you don't have to give up testability for convenience.

In fact, the only thing you'll give up is the NRE you pay with full masked arrays. You can get started with an entry level Action Logic System for under $5000. Guaranteed.

And Actel FPGAs are even 883 mil-spec compliant.

You can be brilliant right now with 1200- and 2000-gate devices, and a whole new family of 8000-, 4000- and 2500-gate parts are on the way. Call **1-800-227-1817, ext 60** today for a free demo disk and full details about the Action Logic System.

It could make your whole day.

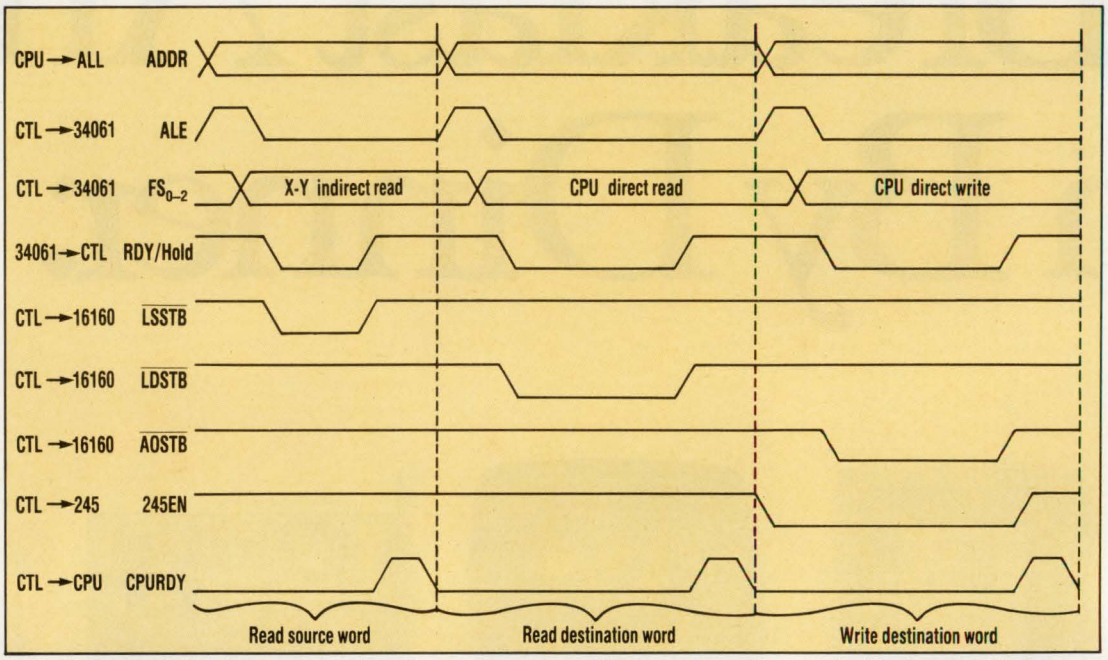
Actel

Risk-Free Logic Integration

You loved ACT 1. Now catch ACT 2.
Phone 1-800-227-1817, ext 62 to reserve a place at the Actel FPGA Technology Seminar coming soon to your area.

© 1990 Actel Corporation, 955 E. Arques Ave., Sunnyvale, CA 94086. ACT, Action Logic, Activator, and Actionprobe are trademarks of Actel Corporation. All other products or brand names mentioned are trademarks or registered trademarks of their respective holders.

output data is written back to the destination region *(Fig. 1)*. Pattern data may be stored in an internal register, as in the VL16160 single Raster-Op ALU chip. Or it may be read from a separate block of memory, as in the VL82C164 Quad Raster-Op chip. Both ICs have direct strobes to all registers that transfer data to or from memory, eliminating the typical delays of address decoding. Both have an internal word counter that automatically activates masking at the beginning and end of a scan-line transfer.



4. A BitBLT cycle timing diagram shows the cycle sequence generated by the state machine contained in the control logic. The notations to the left of each signal name show the devices that generate and receive the signal.

The counter, which instantly concatenates and shifts source data to align with the destination, transfers data left-to-right or right-to-left. This enables a source block to be transferred to an overlapping destination without corrupting the source. Both can do a bit-wise combination of source, pattern, and destination data using any of 256 possible three-operand Boolean functions. Therefore, 256 functions are possible because a three-input truth table has eight possible states, and the output for each state can be defined as either true or false, thus $2^8 = 256$.

In a design example of a graphics subsystem, a single-plane, two-color display can be implemented using the VL16160 single Raster-Op ALU for simplicity *(Fig. 2)*. The scheme could easily be expanded to use multiple bit planes and one or more VL82C164 Quad Raster-Op chips. The TMS34061 video controller was selected because it can generate X-Y addresses automatically for display memory. The control logic, which can be implemented in a programmable logic array, contains a simple sequencer to control display-memory access during BitBLT operations. Each cycle consists of source-read, destination-read, and destination-write operations.

The ALU handles data manipulation, such as shifting, masking, and logical operations. The TMS34061 video controller generates source addresses, and the host CPU calculates destination addresses. This is because in X-Y addressing mode, the TMS34061 chip updates the address after each access automatically, and the destination requires a read-modify-write operation. The modify portion of the cycle actually occurs within the VL16160, so the CPU need execute only a read, immediately followed by a write, to the same location.

The control logic must generate signals to govern the following operations: host register access to the VL16160 and the TMS34061; host access to display memory; host indirect X-Y access to display memory (where the video controller generates the address); and BitBLT cycle sequencing. The first three are fairly simple and consist primarily of address decoding. The BitBLT cycle sequencer, once started, successively generates one X-Y indirect cycle followed by two host direct cycles.

The video controller's three inputs (FS_{0-2}) select what type of access is to be performed during a read or write cycle. The control logic simply generates the correct access code for each cycle in sequence. The video controller would ordinarily require some sort of external register or logic to generate this code anyway. So it's fairly simple to expand it into a three-step sequencer. The Raster-Op chip has a set of address lines (A_{0-3}) that select which register to access when the CPU programs the chip. The chip also has a set of direct strobe signals (LSSTB, LDSTB, and AOSTB) that access the source input register, the destination input register, and the ALU output, respectively.

The video controller uses one Read Write input signal with a separate strobe, while the Raster-Op chip has separate Read and Write strobes. All of these signals, plus Chip Selects on both chips, should be generated by the control logic. Exactly how this is implemented depends somewhat on the type of host CPU. However, here are a few guidelines for the BitBLT cycle where the host, Raster-Op, and video controller must interact.

To initiate a BitBLT operation, a code is latched in the

control logic to indicate register access. The Raster-Op and video controller are then programmed for the intended operation. This involves setting the mask registers, op counter, and width register in the Raster-Op, and initializing the X-Y addressing registers in the video controller *(see "Programming the Raster-Op chip," p. 102)*.

Another code is then written to the control logic register to initialize the BitBLT cycle sequencer. The BitBLT then proceeds as follows: The CPU reads a word from display memory. The control logic causes the video controller to execute an X-Y indirect read from the source region defined by the X-Y address, and then increments the address. When the Ready signal from the video controller indicates the data is valid, it's strobed into the Raster-Op source register. The CPU then reads another word from display memory. The control logic causes the video controller to execute a CPU direct read from the destination word defined by the CPU address.

When the Ready signal from the video controller indicates the data is valid, it's strobed into the Raster-Op destination register. The CPU then writes a word to display memory at the same address. The control logic causes the video controller to execute a CPU direct write to the destination region defined by the CPU address. But it blocks the data from the CPU by disabling the 245 transceiver, enabling the output of the Raster-Op ALU instead. This read-write operation occurs at the same address in the destination. As a result, any read-modify-write instruction of the host CPU can be used, such as a register to memory add instruction. A row of pixels can, therefore, be processed by a very tight program loop. The loop would consist of a read from any display-memory address followed by an auto-increment or auto-decrement read-modify-write instruction to the destination address.

At the end of each row, the source and destination addresses are adjusted for the beginning of the next row. The BitBLT software algorithm would now look more like the following:

```
Calculate horizontal word count: Abs(X2-X1)/word
width
Determine shift value: Remainder(Abs(Xsource-Xdestin-
ation)/word width)
Set right and left mask values (for nonaligned boundaries)
Store calculated values into Raster-Op chip
Initialize video controller mode registers
For each row,
  Set initial destination pointer
  For each memory word,
    Read (any) display location
    Read-modify-write destination word (Auto Incre-
ment/Decrement)
```

The design example uses the CPU to direct display-memory access but does the data manipulation in the Raster-Op ALU and part of the address generation in the video controller. As a result, the hardware can be very simple yet offer a significant speed increase over a strictly software implementation. A functional block diagram shows how control logic coordinates the CPU, video controller, and Raster-Op ALU *(Fig. 3)*.

Three memory cycles make up the three-step BitBLT cycle *(Fig. 4)*. The clock isn't shown because the actual number of clock cycles between events depends on the system's operating speed. The TMS34061 operates synchronously, so the clock speed must be defined in terms of the video controller's requirements. The VL16C160 is an asynchronous device. So if its minimum timing requirements aren't violated, signal timings can be more flexible, and therefore easily adapted to the video controller. An active high CPURDY signal tells the CPU when each memory cycle is finished.

Depending on the processor, another handshake protocol may be required. The Address Latch Enable (ALE) signal, a required input to the 34061 video controller, initiates each memory cycle. RDY/Hold, an output from the 34061 controller, indicates the end of each video DRAM cycle. The timing diagram shows back-to-back memory cycles that can be realized if the host CPU keeps the destination address in one of its registers and if it has a large enough instruction pipeline, or operates out of cache memory.

Unfortunately, the design example neglects one consideration. Much development for IBM-compatible PC graphics has been swayed by the need to remain compatible with a large base of existing software. But more and more users realize that older software can't fully exploit the computing power of today's machines. Speed and efficiency of graphical representation makes up a bigger part of the total useful computing power of a given machine.

Many users are bewildered by the growing numbers of hardware variations caused by the lack (or breakdown) of standardization. Designers of new equipment had to conform to de-facto standards while pressure for innovation kept increasing. Changes are in the wind, though.

And when the dust finally settles, the landscape will doubtlessly be dotted with various systems. They won't necessarily be compatible but will be targeted to their intended markets. The design example would require special drivers or fully custom software to realize its potential. This, however, would make it only marginally useful in the standard PC-compatible environment. Fortunately, as the horizon continues to broaden, hardware solutions like this will find niches.

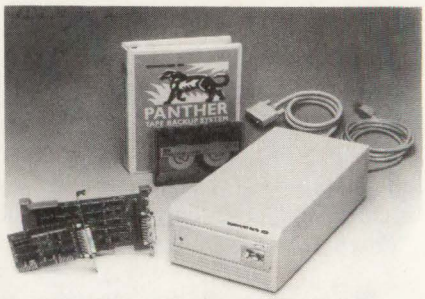
Phil Mattison, product development engineer at VLSI Technology's Logic Products Div. studied computer science at Arizona State University and business administration at the University of Phoenix.

HOW VALUABLE?

HIGHLY	CIRCLE 538
MODERATELY	CIRCLE 539
SLIGHTLY	CIRCLE 540

▼ BACK UP 525 MBYTES IN LESS THAN 45 MIN.

Users of PC/XT/AT, PS/2, and compatible computers can now back up 525 Mbytes of data in less than 45 min. The Panther 1/4-in. tape drive, from Tandberg Data Inc., can be housed either internally or externally. It uses a DC 6000 or equivalent tape media. The backup system can be connected in DOS, OS/2, Unix, Prologue, Pick, Novell, and LAN Manager environments. The drive's MTBF is 80,000 hours, and it boasts error rates of less than 1 in 10^{15} bits. The external systems are housed in 3-1/2-by-6-1/2-by-14 in. cabinets. The internal models fit in standard half-height drive slots. An external 525-Mbyte drive sells for $2695.



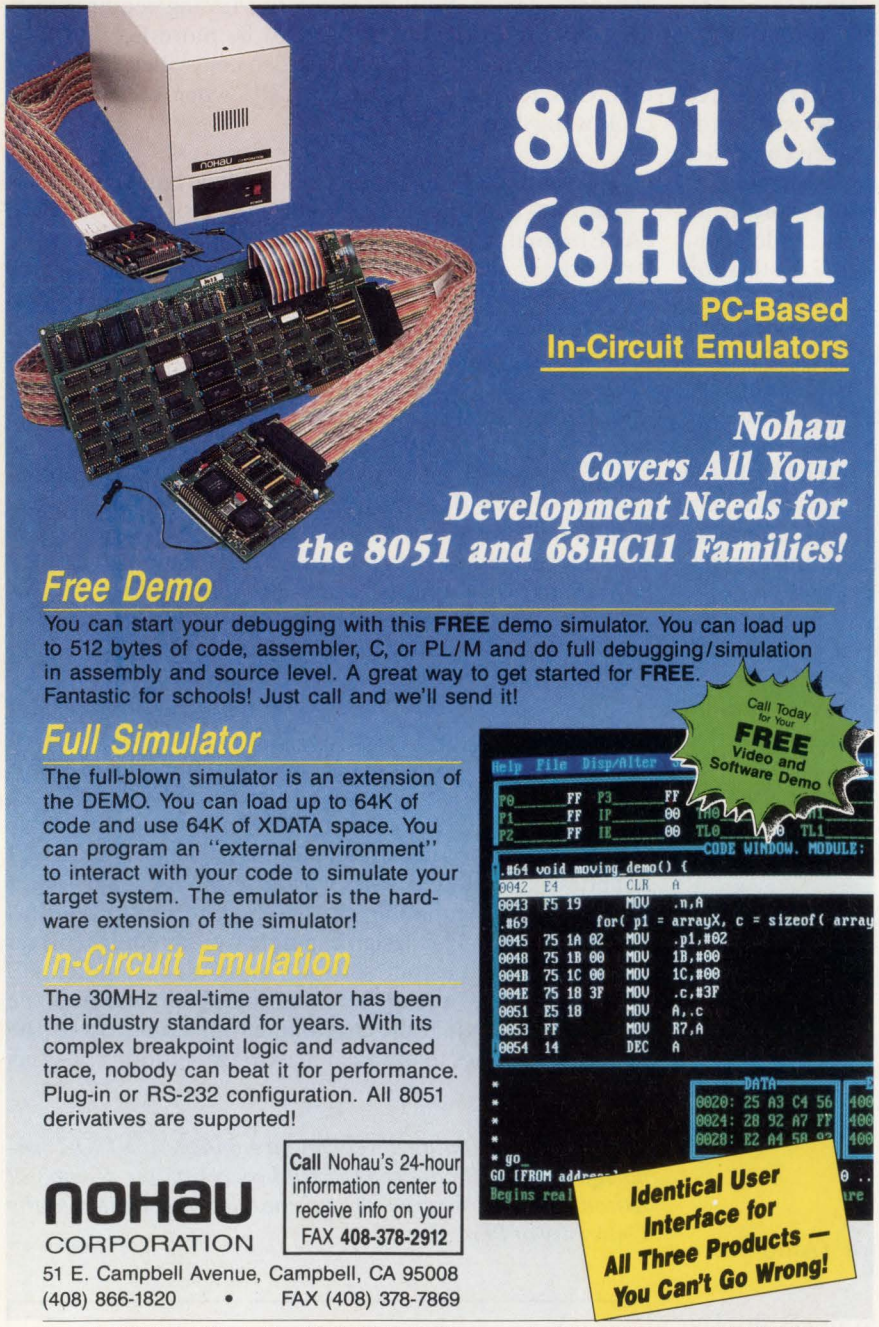
Tandberg also announced that the data-transfer rate of its 1-Gbyte drive has increased by 50%. The TDC 4100 1/4-in. drive now backs up at 300 kbits/s. With the new rate, 1 Gbyte of data can be backed up in under an hour. The 4100 meets Quarter Inch Cartridge (QIC) development standards for backward reading and writing of previous formats. It comes with SCSI and SCSI-II interfaces, which can operate in asynchronous or synchronous modes. In OEM quantities, the 4100 costs less than $700.

Tandberg Data Inc.,
2649 Townsgate Rd., Suite 600
Westlake Village, CA 91361
(805) 495-8384.
▶ CIRCLE 551

▼ INPUT IMAGES FROM NONSTANDARD CAMERAS

The VisionPlus-AT family of frame-grabber boards has a new member, the Variable-Scan Frame Grabber (VFG). This entry-level board links with nonstandard sensors, such as line-scan, area-scan, digital, and high-resolution cameras. The VFG contains a 1024-by-1024-by-12-bit image memory that can store one high-resolution image or multiple lower-resolution images. The images can be displayed in pseudocolor on standard RGB monitors. The board is built around the VisionBus, a real-time video bus for processing and memory expansion. A software library of over 200 subroutines ranging from register-level functions to convolutions and filters is available. The VFG costs $3995. An initial license for the software library sells for $1000. Source code is also available.

Imaging Technology Inc.
600 West Cummings Park
Woburn, MA 01801
(617) 938-8444
▶ CIRCLE 552



Australia (02) 654 1873, Austria (0222) 38 76 38, Benelux +31 1858-16133, Canada (514) 689-5889, Czechoslovakia 0202-2683, Denmark (42) 65 81 11, Finland 90-452 1255, France (01)-69 41 28 01, Germany 08131-25083, Great Britain 0962-73 31 40, Hungary (1) 117 6576, Israel (03) 48 48 32, Italy (011) 771 00 10, Korea (02) 784 784 1, New Zealand (09) 392-464, Portugal 01-80 9518, Sweden, Norway 02 649050, Singapore (065) 284-6077, Spain (93) 217 2340, Switzerland (01) 740 41 05, Taiwan (02) 7640215, Thailand (02) 281-9596, Yugoslavia 061-57 19 49.

CIRCLE 84

Picture your flat panel display using Cirrus Logic controller chips. They actually add colors to your display capabilities for more realistic shading.

The same panel looks flat without our enhanced VGA capabilities. And it will lose face faster without our optimized power management system.

How To Avoid Losing Face On Your Color LCD Display.

Face it. The first thing everybody notices about your newest laptop is the display quality. Is it bright? Are the images clear and well modeled? Are the colors vivid?

With Cirrus Logic LCD VGA controllers, your answer is yes. Which is why we're the leading supplier of display controller chips in the laptop and notebook market.

For life-like 3-dimensional imaging, Cirrus Logic color LCD controllers offer technology leadership for your color products. With direct support for the latest active-matrix color LCD panels. Our controller chips do more than support your panel's color capabilities — they enhance it with full VGA color support and a fuller color palette. To give you color so good it competes with CRT quality.

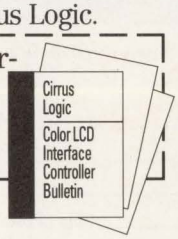
Our monochrome solutions give you displays that *PC Magazine* called "the stars of our VGA color-mapping tests"* with up to 64 shades of gray. And with a lower dot clock rate, your power consumption is lower than other solutions for longer battery operation.

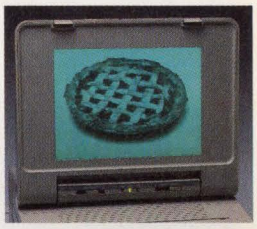
Cirrus Logic LCD controllers are fully compatible with the popular PC video standards and will work with LCD, plasma, or electroluminescent displays.

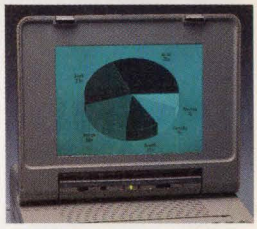
Simplify your design job. A higher level of integration gives you all this in the smallest form factor available. We also supply software and hardware design notes and full design support. You get the results you want quickly and easily.

Design a more competitive product. One that looks better — and makes you look better. That lasts longer on a battery. Use the display solutions from a proven technology leader in laptop and motherboard VGA: LCD controller chips from Cirrus Logic.

Get the picture. Get more information on LCD controllers.
Call 1-800-952-6300, ask for dept. LL34







Cirrus Logic monochrome LCD controllers will also make everything from realistic scanned images to business charts look tastier.

CIRRUS LOGIC

C L O S I N G T H E G A P

©1991 Cirrus Logic, Inc., 3100 West Warren Avenue, Fremont, CA 94538 (415) 623-8300; Japan: 462-76-0601; Singapore: 65-3532122; Taiwan: 2-718-4533; West Germany: 81-52-2030/6203
Cirrus Logic and the Cirrus Logic logo are trademarks of Cirrus Logic, Inc. All other trademarks are registered to their respective companies. * PC Magazine, March13,1990, p. 204.

Join Best Western's Gold Crown Club...

and the rewards can be yours.

Best Western's Gold Crown Club – it's easier than ever to earn points* redeemable for valuable awards at nearly 1900 Best Western locations in the U.S., Canada, Mexico and the Caribbean.

Just look at the values! Here's what you can earn:

• Room nights at Best Westerns in the U.S., Canada, Mexico and the Caribbean • U.S. Savings Bonds (gift certificates for non-U.S. residents) • General Rent-A-Car Certificates • Gourmet Dining Certificates

Start earning points today. There's no cost to join! Make your Gold Crown Club membership a necessary part of your travel plans.

Discover America

Best Western INDEPENDENT WORLDWIDE LODGING

Each Best Western is independently owned and operated.

Here's my application. Please enroll me in your Gold Crown Club today, at no cost to me.

Name _____

Company _____ Phone _____ Ext. _____

Please mail to my _____ Home _____ Business address

Address _____ City _____

State / Province _____ Zip / Postal Code _____ Country _____

Mail to: Best Western International, Inc. Gold Crown Club
P.O. Box 3858, Holliston, MA 01746

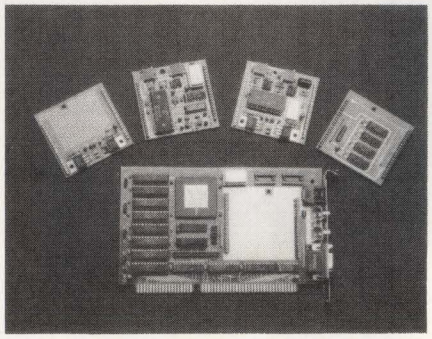
*Gold Crown Club Points are awarded for rooms purchased at the regular rate. Points will not be awarded for discounted room rates.

CIRCLE 1

PC DESIGN PRODUCTS

▼ DSP BOARD PEAKS AT 25 MFLOPS

Based on AT&T's DSP32C floating-point digital-signal processor, the AC5-AO DSP board offers a peak performance of 25 MFLOPS. Built with an ISA interface, the board includes 64 kbytes of zero wait-state RAM. It's I/O mapped and uses an on-board DMA controller to achieve



ISA bus transfer rates as high as 2.5 Mbytes/s. For added flexibility, the AC5-AO features a daughterboard area that can accommodate various standard or custom daughterboard options. These include data acquisition, a serial interface, and a Codec. A 25-MHz version of the AC5-AO costs $1195 and is available now from stock. Daughterboards start at $95. Software development tools are also available.

Communication Automation and Control Inc.
1642 Union Blvd., Suite 200
Allentown, PA 18103
(215) 776-6669
▶ CIRCLE 553

▼ INDUSTRIAL CHASSIS FEATURE 200-W SUPPLIES

A family of low-priced industrial chassis for PC-based data-acquisition and control systems features a 200-W power supply and 18-gauge steel construction. They also include a four-layer backplane that accepts any PC/XT/AT-compatible half-size card. The chassis can be either rack or panel mounted. The family includes the CH4516, CH4512, CH4510, and CH4506. They contain 16, 12, 10, and 6 slots, respectively. Prices range from $325 to $449, with a full-card option available for $100.

Ann Arbor Technologies Corp.
P.O. Box 3083
Ann Arbor, MI 48106
(313) 995-1360
▶ CIRCLE 554

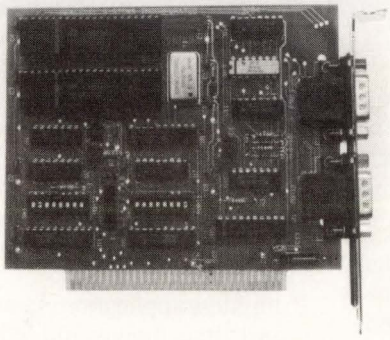
▼ 9600-BPS MODEM COSTS UNDER $700

The 9600etc/e external modem uses the CCITT V.32 full-duplex protocol for 9600-bps communication, V.42 error control, and V.42bis data compression—all available for just $699. By adopting the V.32 modulation, the modem ensures complete compatibility with a growing installed base of 9600-bps modems. Combining V.32 protocol with V.42bis enables the 9600etc/e to transmit and receive

data at speeds up to 38,400 bps while still maintaining 100% accuracy. In addition, the modem is fully backward compatible, with modems following 4800-, 2400-, 1200-, and 300-bps standards. It contains push-button access to frequently used commands, such as speed select, modem diagnostics, auto answer, and data mode.

ATI Technologies Inc.
3761 Victoria Park Ave.
Scarborough, Ontario, Canada
M1W 3S2
(416) 756-0718
▶ CIRCLE 555

▼ ADD TWO SERIAL PORTS TO A PC



Users can now get two additional serial ports for modems, printers, terminals, or other peripherals. The Comm+232 board is a two-channel serial I/O interface for IBM PC/XT/AT and compatible computers. The board is designed specifically for users of Microsoft Windows 3.0, which allows for four communications ports.

The board has selectable addresses and a special switch-port feature that enables it to emulate two COM1 or COM2 serial ports for software requiring either of those two ports. The switch-port software is also included. The Comm+232 is priced at $169 and is available immediately from stock.

Sealevel Systems Inc.
P.O. Box 1808
107 S. Pendleton St.
Easley, SC 29640
(803) 855-1581
▶ CIRCLE 556

The Right Choice Could Save You $25,000.

HTBasic from TransEra will turn your PC into a scientific workstation at a fraction of the cost. A *real* alternative to a high-priced dedicated workstation, a PC with HTBasic gives you the capabilities you need for complex scientific/engineering applications, while retaining compatibility to run and share data with standard PC software.

The savings don't end with the workstation itself. With an HTBasic system, you can use industry-standard printers, graphic output devices, and networking systems. You get the flexibility you need to lay out the system you want without being tied to limited offerings from one supplier.

HTBasic is a state-of-the-art language which gives you a number of advanced scientific/engineering features not found in other BASIC packages.

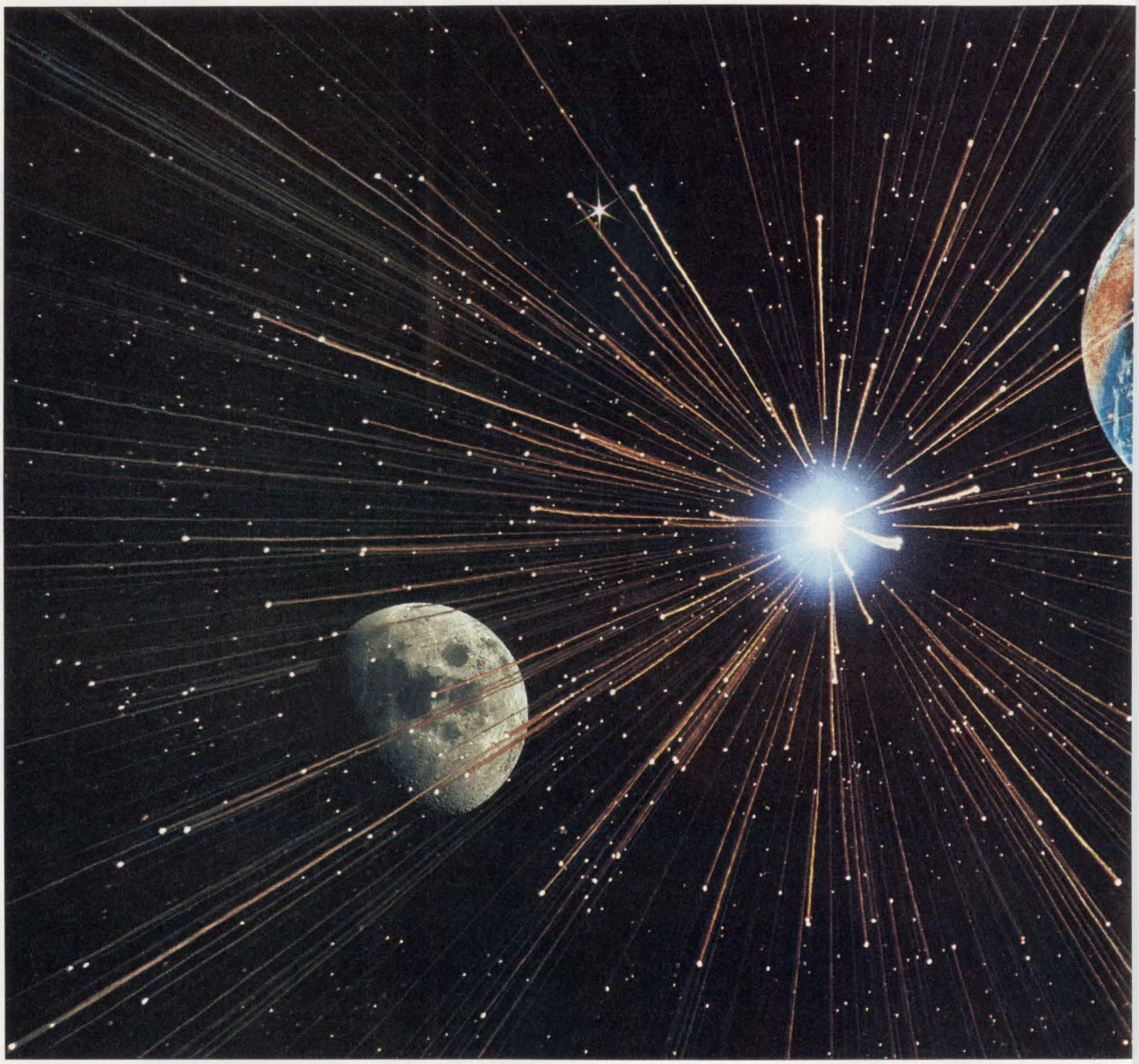
Features such as data acquisition and IEEE-488/RS-232 instrument control syntax, COMPLEX arithmetic, matrix mathematics, complete HP-style graphics, a comprehensive on-line help facility, and many more, add up to increased productivity for all levels of users.

The right choice for your next engineering workstation is a PC with HTBasic. Call or write us today for more information.

TransEra
Engineering Excellence for 15 Years™
3707 N. Canyon Road Provo, UT 84604
(801) 224-6550 Fax (801) 224-0355

CIRCLE 155

Challenging the limits of is the core of our success.



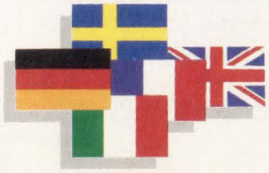
For NCR, it's defined by the very things that drive our industry. The changing technology that is the core of what we do. And people who join you in a partnership and provide service that actually exceeds customer expectation.

Because our designers avidly pursue new ideas, they can help make the complex a bit simpler.

And when your challenge is to design a system that goes beyond known boundaries – they will provide myriad resources to help you push that design to the limit.

Those resources include industry-leading products like mixed-signal ASICs, Ethernet and SCSI, already considered standards. Or, when your latest design requires a custom solution, these products become the cores for unique devices – providing ever-increasing levels of integration in ever-decreasing space. Moreover, because you can design systems at higher levels of abstraction... you're free to explore a universe of limitless applications... and still save time, money and reduce the

North American Sales Headquarters
1731 Technology Drive, Suite 600
San Jose, California 95110
1-800-334-5454



European Sales Headquarters
Gustav-Heinemann-Ring 133
8000 Munchen 83
Germany
49 89 632202

our universe

© Copyright NCR Corporation, 1991.

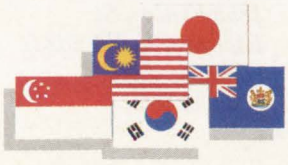
risks associated with new product introductions.

And your design, when completed, will test and perform exactly as agreed. After all, your success, and ours... depends on it.

For more information, call NCR Microelectronics Division: 1-800-334-5454.

NCR

Semiconductors

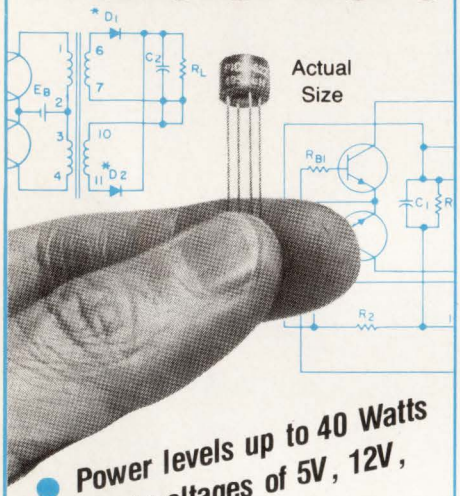


Asia/Pacific Sales Headquarters
35th Floor, Shun Tak Centre
200 Cannaught Road
Central Hong Kong
011-85-2-859-6044

CIRCLE 110

ULTRA-MINIATURE

DC-DC Converter Transformers



- Power levels up to 40 Watts
- Input voltages of 5V, 12V, 24V and 48V
- Standard output voltages up to 300V (special voltages can be supplied)
- Can be used as self-saturating or linear switching applications
- Operation over ambient temperature range from −55°C to +105°C
- All units meet MIL-T-27 (TF5S40ZZ)
- Secondary can be connected for full-wave or dual bridge
- All units are magnetically shielded
- Schematics and parts list provided with transformers
- Delivery-stock to one week

SEE EEM, THOMAS REGISTER OR SEND DIRECT FOR FREE PICO CATALOG

PICO Electronics, Inc.

453 N. MacQuesten Pkwy. Mt. Vernon, N.Y. 10552

Call Toll Free **800-431-1064**

IN NEW YORK CALL **914-699-5514**

Send for PICO's new catalog featuring Ultra Miniature Transformers/Inductors/ DC-DC Converters

CIRCLE 81

PC DESIGN PRODUCTS

▼ OPTICAL MOUSE SLIMS DOWN CONSIDERABLY

An extremely small, lightweight, and accurate mouse is now available for IBM PCs and compatibles. The Little Mouse has a base resolution of 300 counts/in., variable to 30,000 counts/in. It's compatible with Microsoft and PS/2 protocols and works with Windows 3.0.

The accuracy of the two-button mouse comes from its built-in M-5 optical technology. There are no moving parts, and no cleaning, maintenance, or adjustment is ever required. The input device has an MTBF of more than 20 years. It comes bundled with four "mouseable" software applications. The Little Mouse sells for $149.95 and is available now.

Mouse Systems Corp.
47505 Seabridge Dr.
Fremont, CA 94538
(415) 656-1117
▶ CIRCLE 557

▼ TRANSFER DATA 100 TIMES FASTER ON A 386-BASED PC

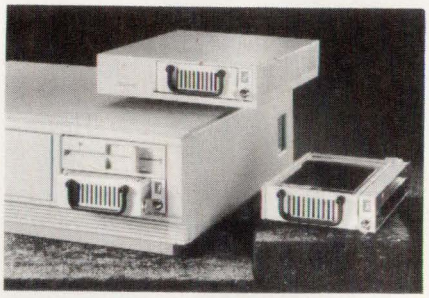
Using the CoStar AT bus accelerator-coprocessor board with 80386-based PCs, applications can run up to 100 times faster than without the board. The accelerator's interface architecture effectively overcomes the data-transfer bottleneck that's typically associated with the AT bus.

The CoStar couples an Intel i860 RISC microprocessor to the existing 386SX chip. This combination enables the PC to run math-intensive scientific and engineering applications that previously required a supercomputer. The board permits data-transfer rates up to 33 Mbytes/s and it's optimized to allow both CPUs to run at their maximum speed at all times. The high speed can also be attributed to the board's efficient virtual-memory capabilities and the high-speed local memory. Available now, the CoStar ranges in price from $3995 to $5995, depending on the processor speed (33 or 40 MHz) and the amount of memory included with the board.

TekStar Systems Corp.
P.O. Box 585
2415 Parview Rd.
Middleton, WI 53562
(608) 836-7890
▶ CIRCLE 558

▼ REMOVABLE HARD DISK BOLSTERS SECURITY

Designed for security-sensitive computer applications or for multiple users sharing one system, the Data Express 5-1/4-in. removable hard-disk drive fits into a standard half-height drive slot. The drive supports most standard interfaces, including AT,



SCSI, and ESDI. The Data Express comes with a receiving frame that installs into the drive slot and a drive carrier that acts as a removable drawer within the receiving frame. A 3-1/2-in. drive can also be mounted in the drive carrier. The drive has a maximum storage capacity of 450 Mbytes, suiting it for any type of PC or workstation. Prices for the Data Express subsystem start at $315.

Kingston Technology Corp.
3023 S. Harbor Blvd.
Santa Ana, CA 92704
(714) 545-6887
▶ CIRCLE 559

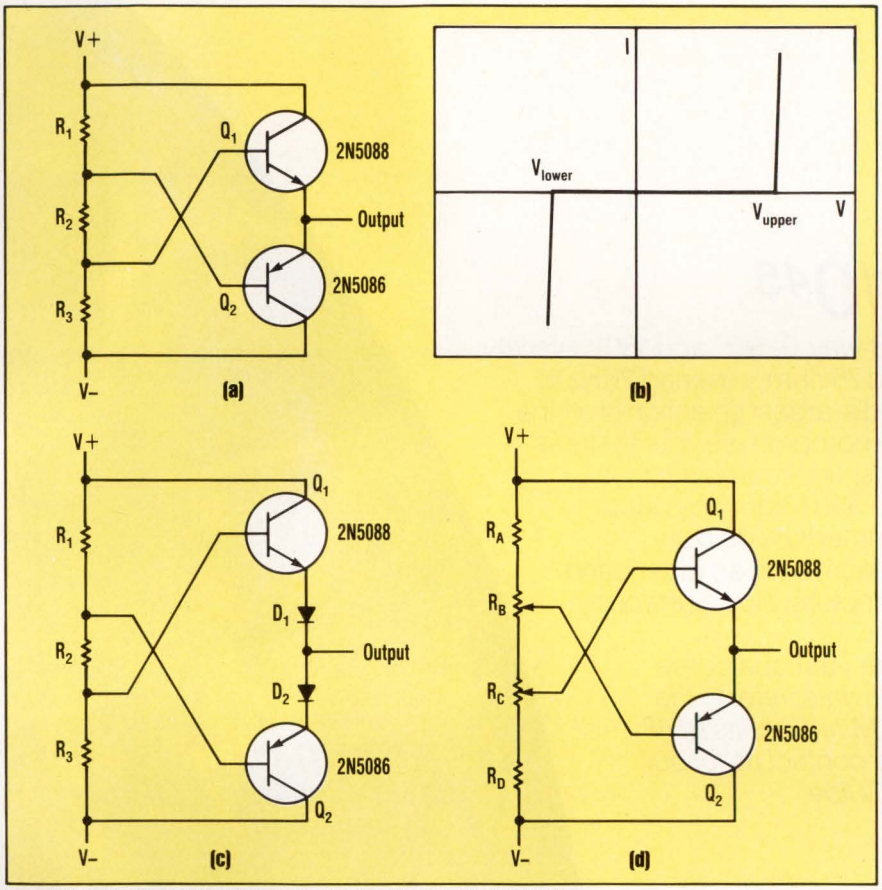
▼ TURN GRAPHICS INTO NUMBERS

Designed for the Apple Macintosh, digiMatic is a tool that actually turns graphics into numbers. The software converts any graphical information into useful, editable numerical data quickly and easily using the computer's mouse. The extracted data can then be saved as tab-delimited text or in the Mac's PICT2 format for use in other programs. The tool automatically maps the screen size of any monitor in pixel units, giving programmers rapid determination of window and region coordinates for pasting into code and resources. The digiMatic software, which runs on any Macintosh computer, sells for $229.

FEB Software
4855 Finlay St.
Richmond, VA 23231
(804) 222-2215
▶ CIRCLE 560

CIRCLE 521 VOLTAGE LIMITER IS ADJUSTABLE

MICHAEL J. ENGLISH
National Semiconductor Corp., 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052; (408) 721-5000.



THIS CIRCUIT LIMITS SIGNAL LEVELS to specific amplitudes without using Zener diodes (a). The circuit's V-I characteristic resembles a circuit containing Zeners connected back-to-back (b). Adding two diodes removes the 8-V pk-pk limitation (c). By replacing the three resistors of the original circuit (a) with two fixed resistors and two potentiometers, users can easily adjust the limiting level (d).

Signal levels must often be limited to specific amplitudes in various applications, such as test systems and pulse generators. Voltage limiting also plays an important role in input-overvoltage and electrostatic-discharge protection. This circuit functions as a programmable two-quadrant voltage limiter *(see the figure, a)*.

The circuit's V-I characteristics resemble a pair of Zener diodes connected back-to-back *(see the figure, b)*. This implementation's advantage is that the voltage limits can be set or adjusted to any level within the allowed signal range. The clipping levels aren't constrained to standard Zener voltages and tolerances.

The clipping levels are given by:

$$V_{upper} = V_- + (V_+ - V_-)(R_2 + R_3)/(R_1 + R_2 + R_3) + V_{be}(Q_2) \text{ and}$$

$$V_{lower} = V_- + (V_+ - V_-)(R_3)/(R_1 + R_2 + R_3) - V_{be}(Q1).$$

The maximum peak-to-peak range between limiting levels must be less than the lowest BV_{ebo} of the transistors used. This is because the transistors' emitter-base junctions are reversed biased for signals between the limit values. For the devices shown, the limit is about 8 V pk-pk. This limitation in peak-to-peak range can be overcome using two diodes with higher breakdown voltages *(see the figure, c)*. The clipping levels must be modified to include the diodes' added forward voltage drop.

Replacing R_1, R_2, and R_3 with two fixed resistors and two potentiometers allows simple level adjustment *(see the figure, d)*.□

CIRCLE 522 KEEP SPICE ACCURACY ABOVE 1 MHz

STEVEN C. HAGEMAN
Calex Mfg. Co. Inc., 3355 Vincent Rd., Pleasant Hill, CA 94523; (415) 932-3911.

Simple equivalent circuits of common discrete ceramic capacitors and film resistors can greatly enhance the accuracy of Spice simulations when frequencies exceed 1 MHz or the transient step interval is less than 1 μs. One equivalent circuit is for a 1/4-W film resistor *(Fig. 1a)*. The model includes shunt capacitance and equivalent series inductance (ESL) effects. The ESL and capacitance are more products of the package size than resistor value, so the nominal values shown work for all values of 1/4-W composition or film resistors.

In a second circuit representing a ceramic capacitor, the ESL and equivalent series resistance effects are simulated *(Fig. 2a)*. The nominal values given are good for small 100-pF types up to 0.2-in., 1-μF square types, with little loss in accuracy. PSpice net lists are generated for the two subcircuits *(Figs. 1b and 2b)*.

The impedance characteristics of

THE WORLD'S LARGEST SELECTION OF
POWER SPLITTERS/ COMBINERS

2 KHz to 8 GHz *from* $10.45

With over 300 models, from 2-way to 48-way, 0° 90° and 180° a variety of pin and connector packages, 50 and 75 ohm, covering 2KHz to 8000MHz, Mini-Circuits offers the world's largest selection of off-the-shelf power splitter/combiners. So why compromise your systems design when you can select the power splitter/combiner that closely matches your specific package and frequency band requirements at lowest cost and with immediate delivery.

And we will handle your "special" needs, such as wider bandwidth, higher isolation, intermixed connectors, etc. courteously with rapid turnaround time.

Of course, all units come with our one-year guarantee.

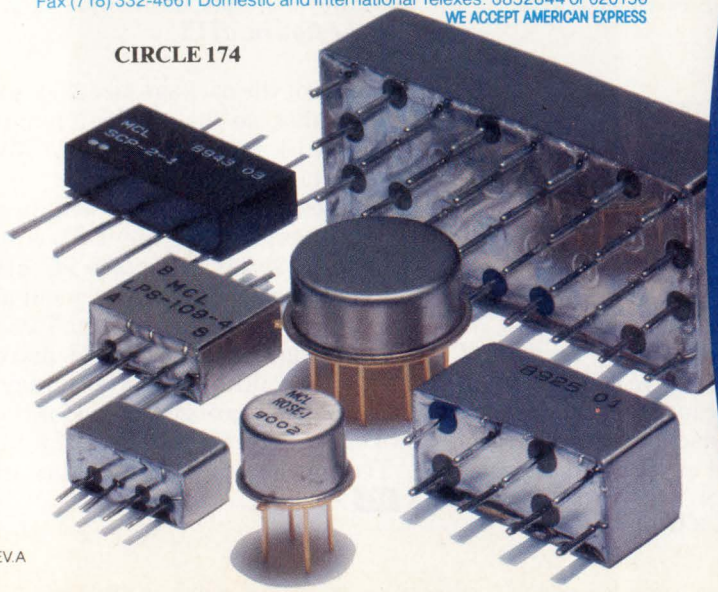
For detailed specs and performance data, refer to the MicroWaves Product Directory, EEM or Mini-Circuits RF/IF Signal Processing Handbook, Vol. II. Or contact us for our free 68-page RF/IF Signal Processing Guide.

finding new ways ...
setting higher standards

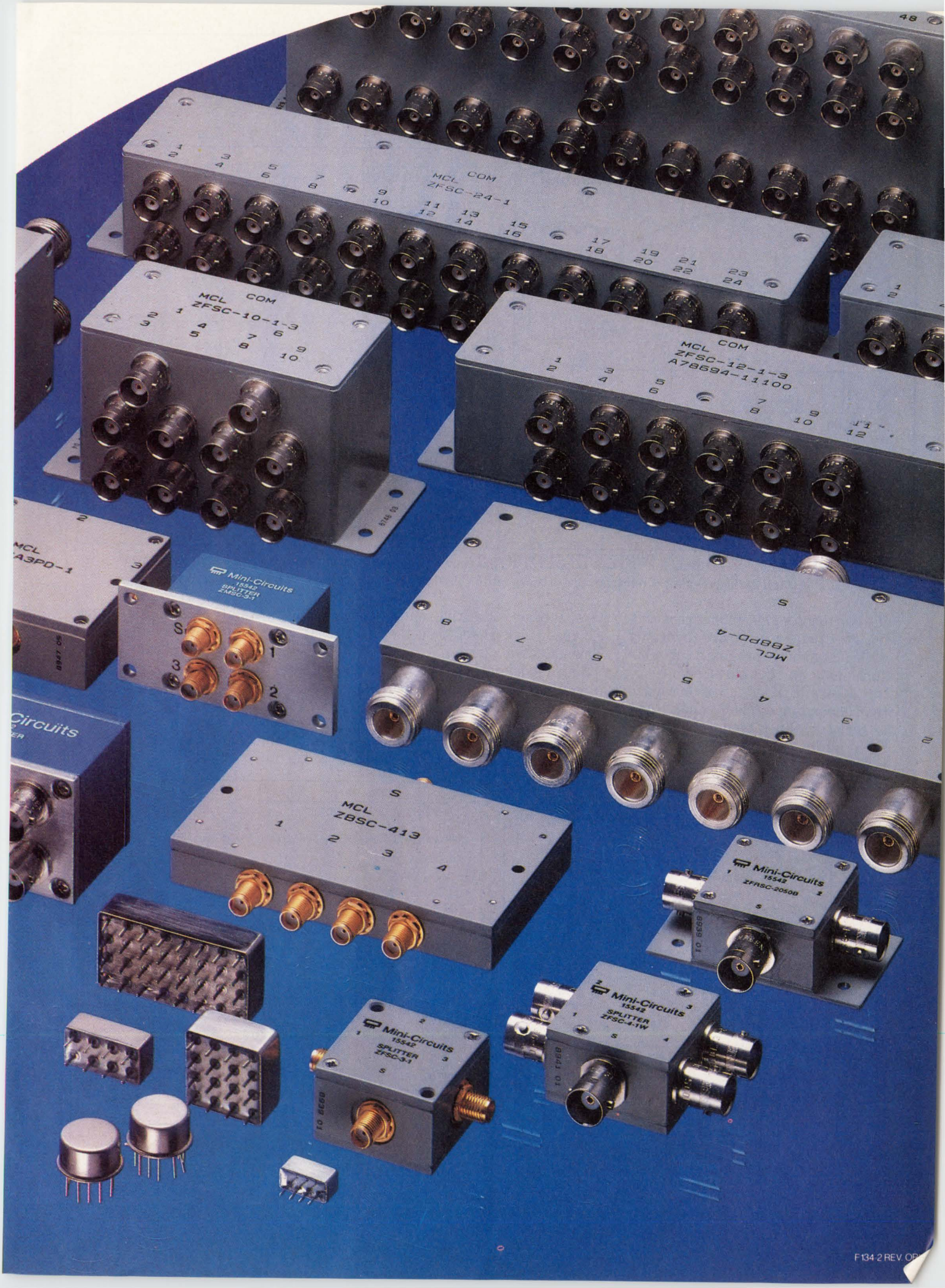
Mini-Circuits

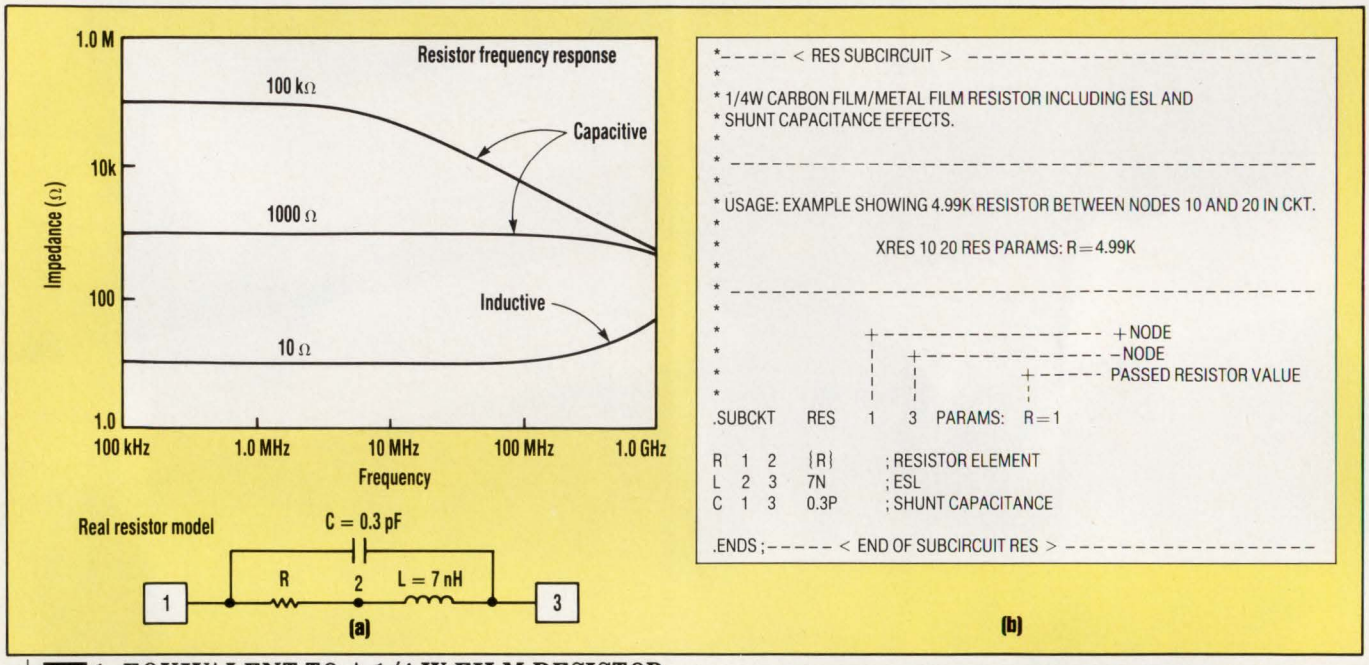
A Division of Scientific Components Corporation
P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500
Fax (718) 332-4661 Domestic and International Telexes: 6852844 or 620156
WE ACCEPT AMERICAN EXPRESS

CIRCLE 174



F134-1 REV.A

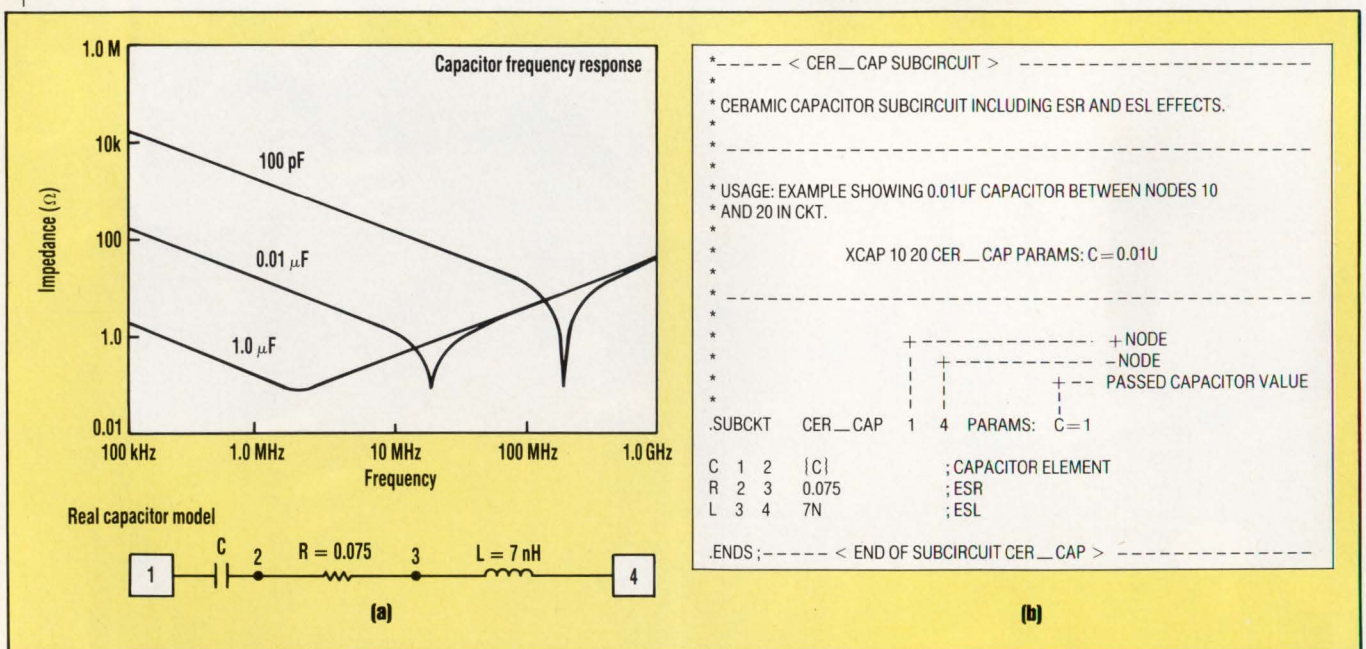

MCL COM
ZFSC-24-1
MCL COM
ZFSC-10-1-3
MCL COM
ZFSC-12-1-3
A78694-11100
Mini-Circuits
15542
SPLITTER
ZMSC-3-1
MCL
ZBSC-413
Mini-Circuits
15542
ZFRSC-2050B
Mini-Circuits
15542
SPLITTER
ZFSC-4-1W
Mini-Circuits
15542
SPLITTER
ZFSC-3-1



1. EQUIVALENT TO A 1/4-W FILM RESISTOR, this circuit includes shunt capacitance and equivalent series inductance (ESL) effects (a). The higher values of resistance tend to be capacitive while the lower values act inductive at high frequencies (b).

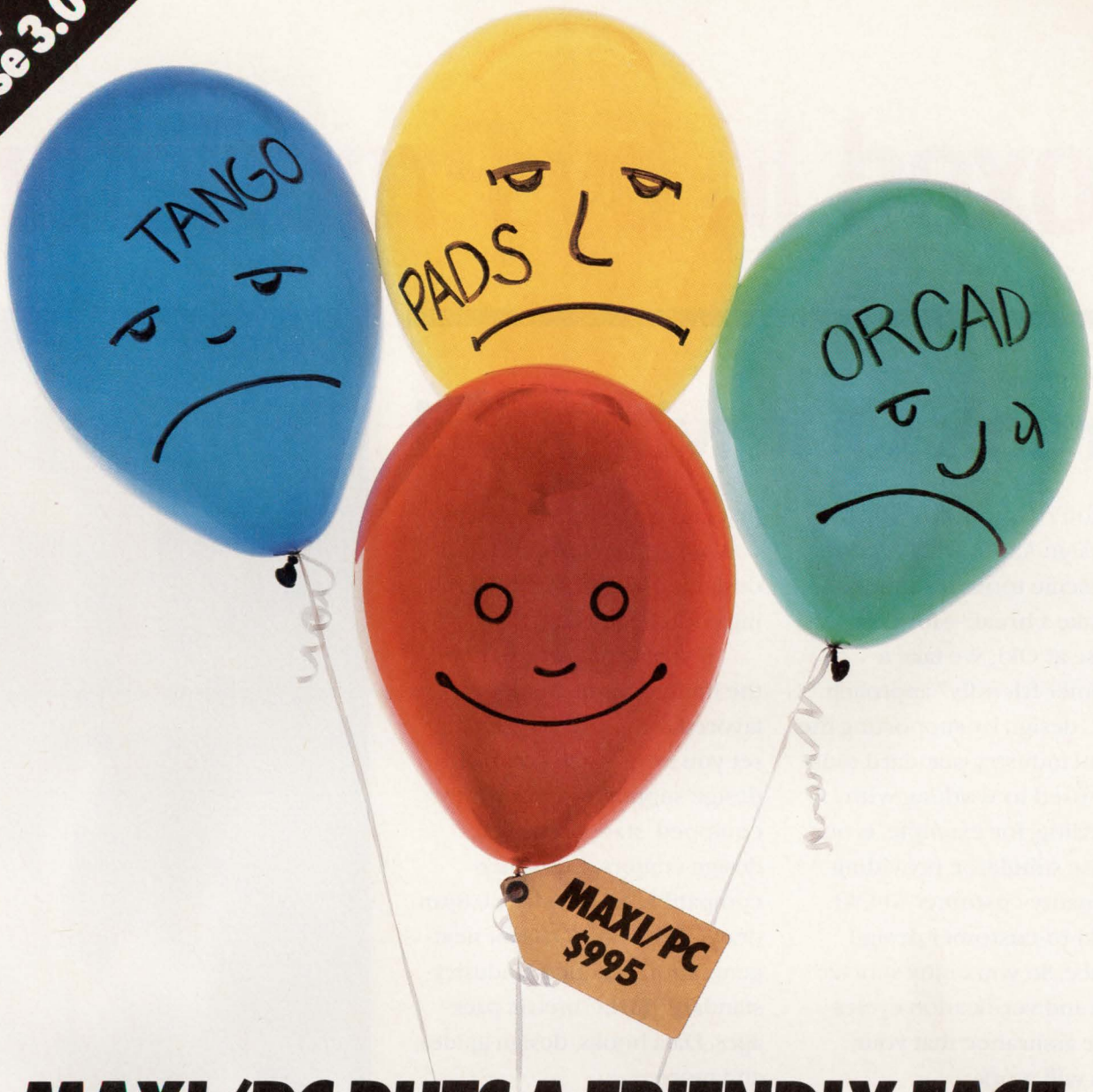
the two macromodels for several values of resistance compare favorably with actual network-analyzer measurements on real parts. The resistors look either inductive or capacitive, depending on their value. Higher resistor values tend to be capacitive, while the lower values act inductive at high frequencies. Capacitors appear capacitive until their self-resonance point, then they become inductive.

Both models assume about a 0.1-in. lead length. If the layout has longer trace runs to the components, about 10 nH/in. of lead length should be added. It's most convenient to use these models as subcircuits. PSpice has a parameter-passing feature that can be employed with subcircuits to pass the actual capacitor or resistor value to the subcircuit. The subcircuits can be used with standard Berkeley Spice by making a separate subcircuit for each component value handled in the simulation.□



2. THIS CERAMIC CAPACITOR MODEL is simulated with the ESL and equivalent series resistance effects (a). The model's characteristic impedance compares favorably with actual network analyzer results on real parts (b).

NEW Release 3.0



MAXI/PC PUTS A FRIENDLY FACE ON PCB CAD

Unlike some people, you'll be smiling when you see how easy to use new MAXI/PC is. A new, proactive user interface saves you *hundreds* of keystrokes in a typical design because it anticipates your next move and logically defaults to the most likely action. MAXI/PC's OSF/Motif™ style interface has clear, logical menus integrated across all functions. It's easy to learn and much easier and more productive to use than the competition.

Nice To Your Budget

MAXI/PC gives you an incredible amount of design power for the money. Rich with features, it's capable of handling multi-layer, double-sided, surface mount boards. You get schematic capture, layout, automatic routing, and manufacturing outputs. All backed by a 30 day, no questions, money back guarantee. All for $995.

Powerful capabilities include:

- 5,000+ part library
- Hierarchical design
- Automatic placement
- Automatic gate and pin swap
- Automatic routing
- Automatic component rename
- Automatic part/component replacement
- Back annotation
- Hotline support

From A Good Family

Racal-Redac is the only EDA vendor to offer a smooth growth path, with data migration from MAXI/PC, to the more powerful PC-based CADSTAR, to high end, workstation-based VISULA EDA. Make yourself smile, get MAXI/PC.

Call today to order MAXI/PC!

1-800-356-8352

MAXI/PC

PCB CAD SOFTWARE

RACAL-REDAC

238 Littleton Road, P.O. Box 365
Westford, MA 01886-9984, USA
Fax: (508) 692-4725

RACAL

OrCad, PADS, and Tango are trademarks of their respective companies.

CIRCLE 111

Boxed In by Proprietary

Break Out with Oki

If you're trapped trying to design ASICs with vendor-specific tools, it's time to make a break—for Oki. Because at Oki, we take a "customer-friendly" approach to ASIC design by supporting the range of industry-standard tools you're used to working with.

Verilog, for example, is our in-house simulator, providing high-quality customer-to-Oki and Oki-to-customer design interface. So you enjoy shorter design and verification cycles and the assurance that your design will work.

Is your ASIC design platform workstation- or PC-based? No matter. With Oki, you get across-the-board hardware, software, and operating system support for DAZIX, Mentor, Valid, Viewlogic, and others. Just choose the environment you're familiar with, and start designing. There's no relearning effort required.

If you're ready to escape the limitations of vendor-favored tools, Oki is ready to set you free—with complete design support: 24-hour, fully-equipped, state-of-the-art design centers. Customer-compatible tools. A true 0.8μm drawn family of SOGs for next-generation products. Industry-standard JEDEC metric packages. Data books, design guides, and more.

Make a break for the design freedom you've been longing for. Call **1-800-OKI-6994**.

Apollo, Cadence, DAZIX, DEC, Digital, DNIX, DOMAIN, GED, HP, IDEA, LOGICIAN, Mentor Graphics, PC-DOS, RapidSIM, Sun, Sun OS, Synopsys, ULTRIX, Valid, ValidSIM, Verilog, Viewlogic, and Workview are trademarks of others.

Transforming technology into customer solutions.

ASIC Tools?

Oki ASIC Design Tool Support

Vendor	Platform	O.S. & Application	Design Kits
Cadence	Sun-4	Sun OS 4.0.1 Verilog 1.5C	SOG: 0.8μm
DAZIX	LOGICIAN Sun 386i Sun-4	DNIX 5.03, Sun OS 4.0.1 Digital Application 6.1 Digital Application 6.3	GA: 1.2μm SOG: 1.0μm, 0.8μm SC: 1.5μm, 1.2μm
Mentor Graphics	HP/Apollo DN3XXX DN4XXX	DOMAIN/OS 10.1 IDEA Series 7.0	GA: 1.2μm SOG: 1.0μm, 0.8μm SC:1.5μm, 1.2μm
Synopsys	Sun-4	Sun OS 4.03 *Interface to Mentor, Valid, Viewlogic	SOG: 1.0μm, 0.8μm
Valid	Sun-4 Sun-3	Sun OS 4.0.1 GED, ValidSIM, RapidSIM	GA: 1.2μm SOG: 1.0μm, 0.8μm SC: 1.5μm, 1.2μm
	DEC Station 3100	ULTRIX ValidSIM GED	GA: 1.2μm SOG: 1.0μm, 0.8μm SC: 1.5μm, 1.2μm
Viewlogic	Sun-4	Sun OS 4.0.3 Workview 4.0	GA: 1.2μm SOG: 1.0μm, 0.8μm SC: 1.2μm
	PC386	DOS 3.3 Workview 4.0	GA: 1.2μm SOG: 1.0μm, 0.8μm SC: 1.2μm

OKI Semiconductor

785 North Mary Avenue
Sunnyvale, CA 94086-2909

CIRCLE 128

CIRCLE 523

DEVELOP ISA BIOS ON A PC

BARTON BUEHLER
4610 Huron Ave., San Diego, CA 92117; (619) 276-8738.

When developing BIOS for PC/XT (ISA) systems, having a 64-kbyte block of nonvolatile memory above DOS DRAM would be useful. One low-cost approach to obtaining this block is to remove one chip of a 64-kbyte block of memory while leaving an identical block above intact. Many full motherboard versions of the PC/XT are configured as:

4th bank - 64 kbytes
3rd bank - 64 kbytes
2nd bank - 256 kbytes
1st bank - 256 kbytes

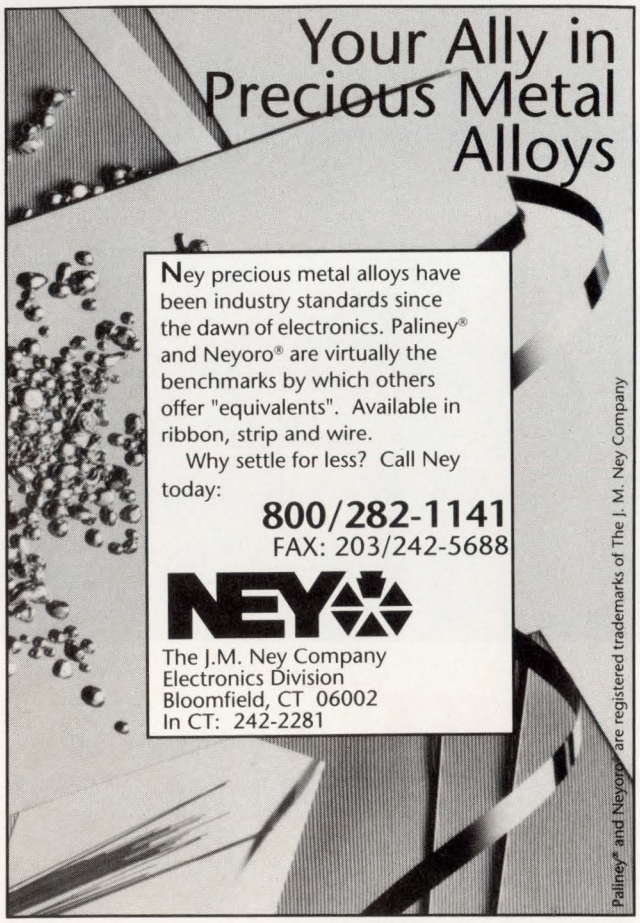
When the third bank of 64-kbyte chips is disabled by removing one chip from its bank (not a parity chip), the fourth bank is still refreshed as though nothing had happened. Upon boot up, the resident BIOS checks memory and hands the system over to DOS as a 512-kbyte DRAM machine. Thus, the fourth bank of DRAM is available as pseudo-static RAM and can be read from or written to using a DOS version that contains the Debug program. It will survive all but a power reset.

When the prototype BIOS is compiled, assembled, linked, and turned into a binary image, the Debug program should be used to load and jump to the new BIOS. Using this method, EPROMs need only be burned to replace the resident BIOS after the many revisions produce an acceptable BIOS. The time-consuming task of burning EPROMs for each cycle of the BIOS development is thus avoided. This concept of having memory available above DOS DRAM applies equally well for any embedded control program that requires less than 64 kbytes of executable code.□

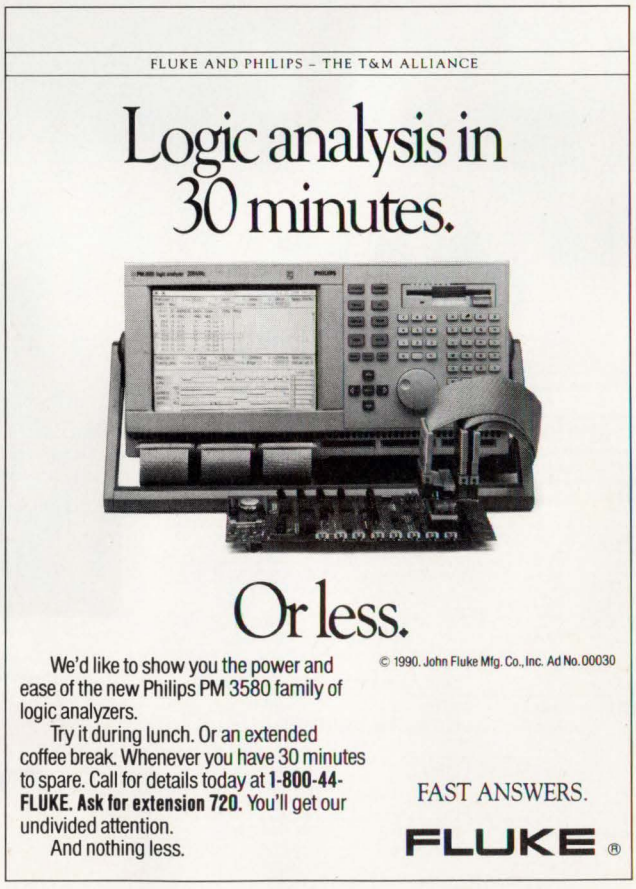
IFD WINNER

IFD Winner for December 27, 1990

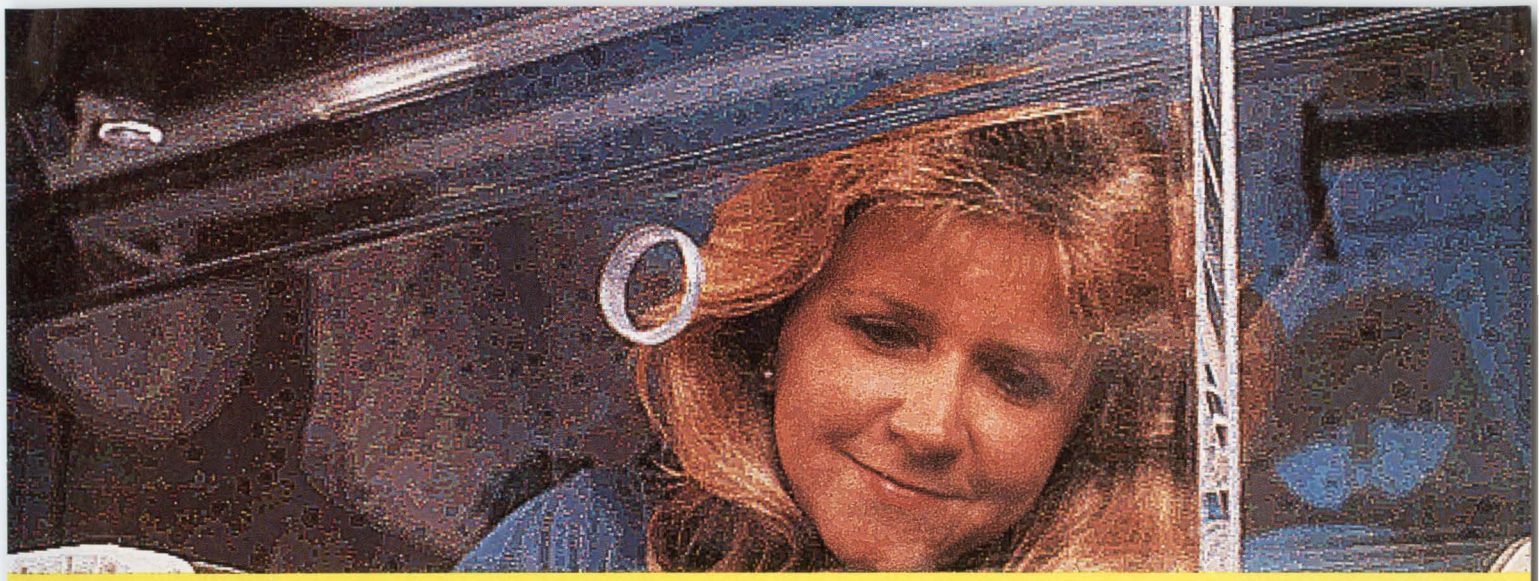
M.S. Nagaraj, ISRO Satellite Centre, Digital Systems Div., Airport Rd., Vimanapura P.O., Bangalore 560017 India. His idea: *"Op Amp Regulates Its Own Supply."*



CIRCLE 82



CIRCLE 129



Your business is safe with us.

Especially when it's serious business.

Small business is just as serious as big business. That's why, since developing the first data cartridge, we've continued to offer virtually every size and format data cartridge you'll need to help protect your business data—from 20 megabytes to 1.35 gigabytes.

No wonder more business protects important information on 3M brand diskettes and data cartridges than any other brand in the world. Call 1-800-888-1889 ext.8 to find out more.

Innovation working for you™

All data cartridges require a compatible drive. ©3M 1991.

3M | Worldwide Sponsor 1992 Olympic Games

36USC380

CIRCLE 2

ALMOST EVERYTHING ABOUT SUN MICROSYSTEMS' FUTURE WORKSTATIONS IS UNDER WRAPS

Everything, that is, except that Sun is using Mentor Graphics IC design tools to create revolutionary chips with record levels of performance.

Workstation details will have to wait for the product announcements, which won't be long since Mentor Graphics IC design solutions accelerate the entire IC design process — from concept to layout to verification. These solutions boost productivity to help market leaders like Sun stay one step ahead of their competition.

Mentor Graphics delivers the most powerful tools and the most flexible design environment, all created to the industry's most stringent software standards. The proof of our technology leadership lies in hundreds of CMOS, bipolar and GaAs chips and tens of thousands of custom and ASIC library cells. Created by organizations like Apple Computer, Motorola DSP Operations, Thomson TMS, Texas Instruments, and, of course, Sun. All using Mentor Graphics IC design tools.

Best of all, Mentor Graphics provides more than just tools. Our total solution includes the design environment, customized training, hot-line support, IC design expertise, and consulting services to maximize your productivity. Our commitment to customer success is another reason companies like Sun choose us.

To learn how Mentor Graphics can commit to your IC design success, call toll-free **1-800-547-3000,** or **1-503-685-8000.** Ask for Dept. 402. Or send us a fax at **1-503-685-8001.**

Mentor Graphics®

Changing The Way The World Designs. Together.

ELECTRONIC DESIGN

QUICK LOOK

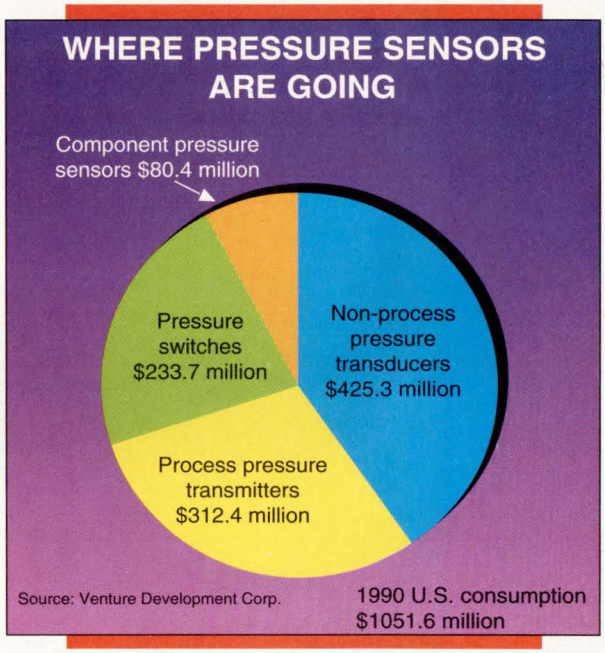
EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Process-control jobs are absorbing more and smart pressure transmitters. As a consequence, the market is booming for these smart devices, which include self-diagnostics, electronic re-ranging, and, for some, digital outputs. Prices are dropping too—some smart devices now go for less than traditional transmitters. These predictions come from Venture Development Corp.

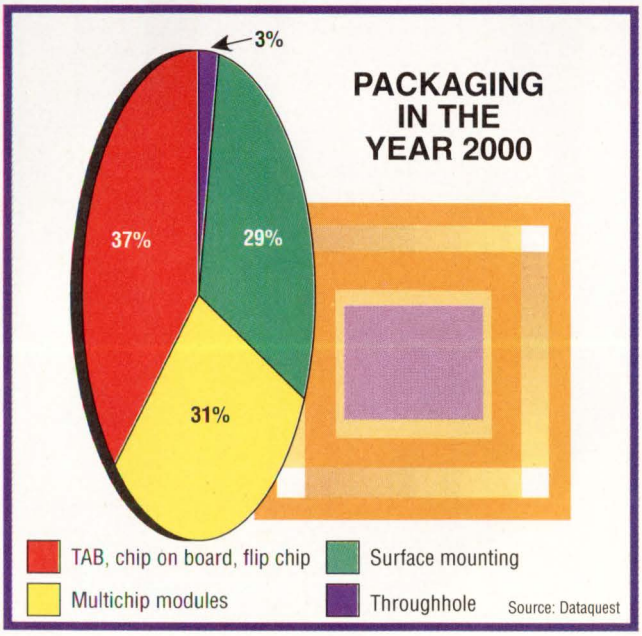
The Natick, Mass., market researcher says the total U. S. market for pressure sensors, transmitters, and switches amounted to $1.05 billion last year. In terms of market segments, the pressure-switch sector shipped $233.7 million worth of product last year. The pressure transducer and transmitter sectors combined for a total of $827.9 million. Another $13.6 million in switches was exported; $280.5 million worth of transducers and transmitters was shipped last year.

Smart devices snared 30% of the market in 1990, up from 20% the year before. And the market for smart transmitters is expected to grow 12.2% a year over the next five years. U. S. sales of pressure transmitters for process control amounted to $312.4 million last year. About half of the pressure transmitters used variable capacitance. Another 10% of the transmitters relied on ion-implanted semiconductors with this figure expected to increase; nonetheless, semiconductors can be used only in jobs below 150°C (300°F).



EYECATCHER

As ICs get smaller and faster, their packaging is changing. Multichip modules will account for $18 billion in revenues in 1995, forecasts market researcher Dataquest. By the year 2000, MCMs will house one-third of ICs while throughholes will account for just 3%.



DID YOU KNOW?

. . . that world semiconductor shipments should increase 12.5% this year, on the heels of a scant 1.5% increase in 1990. The world market should amount to $55.7 billion in 1991. Part of the momentum comes from countries like Hong Kong, where electronics exports are expected to increase 7% in 1991, compared with 5% last year. Orders are up 10% compared with the same period last year.

SIA, Hong Kong Economic & Trade Office

. . . that the typical U. S. manufacturer invests 20 to 25% of its operating budget finding and fixing mistakes.

BusinessWeek

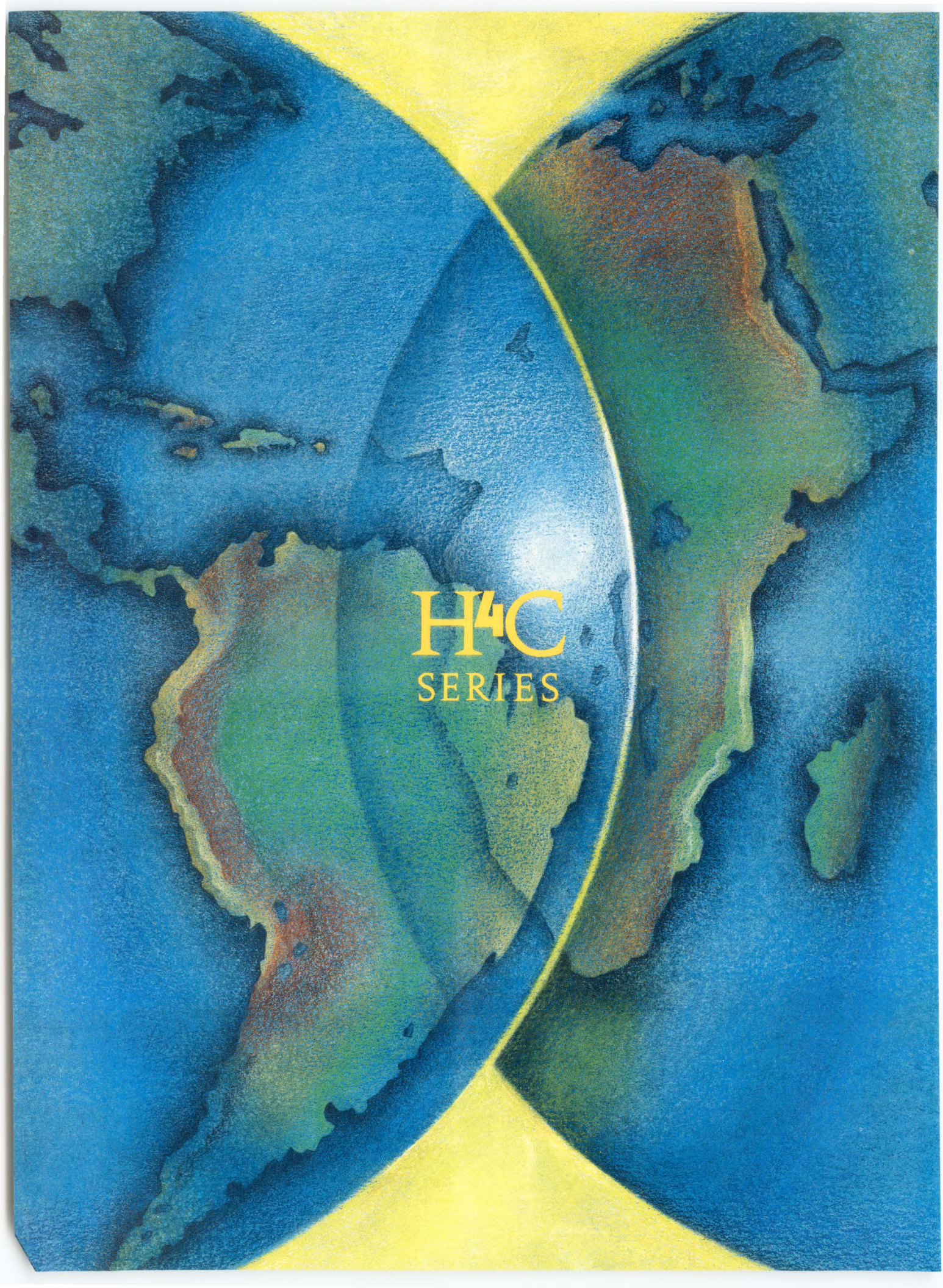
. . . that in fiscal 1988, the U. S. spent 0.2% of its research funds on industrial technology, compared with 4.8% by Japan, and 14.5% by West Germany. That year, the U. S. spent 65.6% of its research money on defense, compared with 4.8% by Japan and 12.5% by West Germany.

U. S. Council on Competitiveness Report

. . . that 26% of U. S. companies reported having computer viruses on their PCs as of January. In the same quarter of last year, about 10% of companies reported a computer virus.

Certus International Corp.

. . . worldwide, compatible high-definition TV should be a reality by the year 2010, according to 70% of engineers surveyed by the Gallup Organization for the IEEE. About 33% said that superconductivity would find practical application in power and transportation by 2010.


H4C
SERIES

The Best of Two Worlds in One New System Solution.

Motorola's H4C Series™ combines unprecedented speed/power and density with unique system-level design implementation in one CMOS Array.

If you want the density advantages of cell-based architectures plus the economy and cycle time of high-performance custom gate arrays, you've just found the best of two worlds in one system solution. It's Motorola's new generation state-of-the-art CMOS ASIC technology, the H4C Series™ of Customer-Defined Arrays.™

The new fabrication process of the H4C Series provides 180 picosecond performance in densities typically ranging from 19,000 up to 222,000 usable gates, and supports the speed requirements of 60 MHz processors with a power dissipation of only 3μW/Gate/MHz.

Array	Available Gates	Usable Gates (70%)	I/O Wirebond/Tab
H4C027	27,000	19,000	160/188
H4C035	35,000	24,500	176/208
H4C057*	57,368	40,000	216/256
H4C086	86,000	60,000	260/304
H4C123*	123,136	86,000	340/360
H4C161	161,000	113,000	344/404
H4C195*	195,452	136,800	376/444
H4C318	318,000	222,500	464/556

H4C SERIES

*Now available. Other Series devices planned for future announcement.

System-Level Design

One of the H4C Series' system-level design features is the Customer Defined Architecture. CDA enables versatile, efficient system-level design in which large, fully-diffused architectural blocks like RAM, and in the future, microprocessors and arithmetic functions, are embedded in the Array. High-speed, user-configurable RAMs are structured to easily integrate with user-defined BIST circuitry. Optimized SRAM is available in several hundred thousand single and dual port configurations of up to 256K bits.

Additionally, Motorola's proprietary digital PLL clock skew control macros facilitate high-speed inter-chip synchronous communication. And, a variety of design-for-test features, including JTAG in the I/O periphery and ESSD/LSSD scan macros, is included.

What brings all these system design features to your fingertips is our work-station based Open Architecture CAD System™ which creates an environment where leading edge design tools work together in harmony.

System Solutions

- Tight Process Distribution
- Digital PLL Clock-Skew Mgt.
- Design-For-Test Scan Macros
- JTAG (IEEE 1149.1) Boundary Scan
- Embedded Megafunction Blocks
- Clock Tree Synthesis
- User-Defined Memorist™ SRAM Compiler

The H4C Series meets the challenges of the most demanding applications by combining advanced sub-micron technology with Motorola's unique battery of system-level design solutions. It's the best of two worlds in one system solution. And it's available only from Motorola.

MOTOROLA

MOTOROLA and Ⓜ are registered trademarks of Motorola Inc.

To: Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036

Please send me a copy of the Motorola Semiconductor Technical Data Booklet on the H4C Series CMOS Arrays and the CDA™ Architecture 489ED050991

Name _____

Title _____

Company _____

Address _____

City _____

State _____ Zip _____

Call me (_____) _____

QUICKLOOK

BEST SELLERS

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

1. *C Language Algorithms for Digital Signal Processing* by Paul Embree. Prentice-Hall, 1990. ***$50.***
2. *Circuits Interconnections and Packaging for VLSI* by H. B. Bakoglu. Addison-Wesley, 1988. ***$43.25.***
3. *Digital Communications* by John Proakis. McGraw-Hill, 1989. ***$56.95.***
4. *IC Op Amp Cookbook*, third edition by Walter Jung. Howard Sams & Co., 1986. ***$24.95.***
5. *Mixed Mode Simulation* by Resve Saleh. Kluwer Academic Publishers, 1990. ***$59.95.***

COMPUTER SCIENCE:

1. *Programming Windows*, second edition, by Charles Petzold. Microsoft Press, 1990. ***$29.95.***
2. *Resedit Complete*, with disk, by Peter Alley. Addison-Wesley, 1991. ***$29.95.***
3. *C Programming Language*, second edition, by Brian Kernighan and Dennis Richie. Prentice-Hall, 1989. ***$32.***
4. *Programming Perl* by Larry Wall. O'Reilly & Associates, 1990. ***$24.95.***
5. *Word for Windows Companion* by Mark Crane. Microsoft Press, 1990. ***$26.95.***

This list is compiled for *Electronic Design*'s Quick Look section by Stacey's Bookstore, 219 University Ave., Palo Alto, CA 94301; phone (415) 326-0681; fax (415) 326-0693.

QUICK NEWS: EDUCATION

More than other occupations, engineering is a learning profession. Engineers have to become and remain students. Rapid changes in technology amplify the need to keep learning. Courses on videotape can be rented or purchased. One source is the Office of Continuing Engineering Education at the University of Illinois in Urbana-Champaign. Each course has a recommended text; printed notes supplement many courses. Courses may be previewed free for two weeks. Write for a free catalog to the Office of Continuing Education, University of Illinois at Urbana-Champaign, 422 Engineering Hall, 1308 W. Green St., Urbana, IL 61801; (217) 333-6634.

QUICK NEWS: THE PROFESSION

American Engineer, a newsletter from the American Engineering Association, aims to boost engineers' status as professionals and promote engineering employment. The AEA has a goal of 50,000 members by the end of the year. Regular membership is $20; professional membership, $50; and sponsoring membership. $100. All members receive a copy of *American Engineer*, the AEA's monthly publication, which has articles on employment and publishes engineers' opinions. For more information or to join, contact the AEA, P. O. Box 820473, Ft. Worth, TX 76180-0473.

KMET'S KORNER

...Perspectives on Time-to-Market

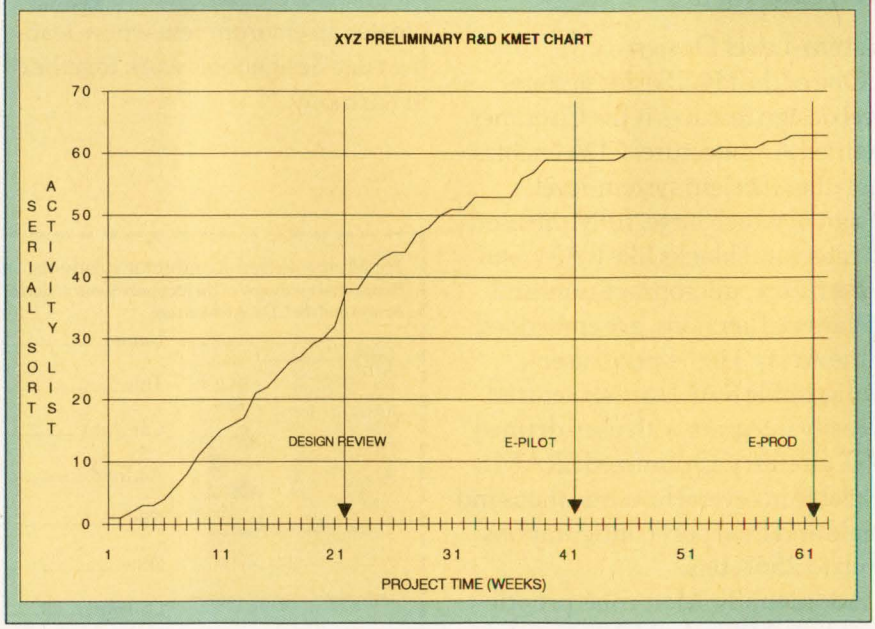
BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458, fax (408) 253-6085

Now that the team has modeled its concurrently engineered new product-development effort, how does it know if the plan is any good? To help answer this question, I've developed a graphical technique that's very useful.

To apply the technique, you simply sort the project's database and arrange task information by completion date. In effect, you produce a to-do list for the entire project from the task data, arranged by the date work should be completed. The next step is to produce a graph of this information called the KMET chart. The chart is produced by having time on the X-axis and cumulative task completion on the Y-axis *(see the figure)*.

In the chart, 63 tasks exist over about 61 weeks. Besides cumulative task count over time, the graph provides key milestone information and, possibly most important, discloses information about the underlying network through the slope of the line. The entire plan is graphically summarized on a single piece of paper. As you review the figure, can you see problems with the plan being represented by this chart?

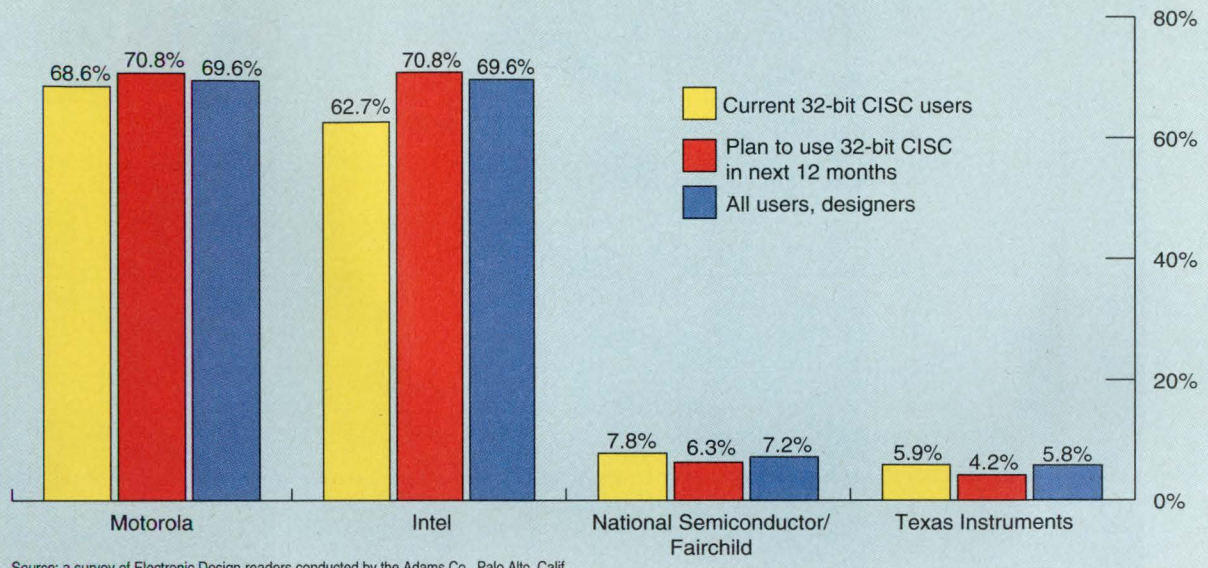
In the next column, I'll discuss using the KMET chart as a plan analysis and decision-making tool. In the meantime, produce a KMET chart of your own for a project you have in a database and then study the results.



QUICKLOOK

MICROPROCESSOR SURVEY

NAME THE LEADING VENDORS OF 32-BIT CISC MICROPROCESSORS



Source: a survey of Electronic Design readers conducted by the Adams Co., Palo Alto, Calif.

OFFERS YOU CAN'T REFUSE

PLDshell, a software tool for programmable logic design, is free from Intel Corp. The software supports Intel's microcomputer PLDs and other standard devices. PLDshell is a menu-driven shell under which editors, compilers, and programmer software can be run. The software also includes the company's integrated compiler, PLDasm, which compiles designs for microcomputer PLDs using an expanded syntax compatible with PALASM2. PLDasm, which can import other design files, has functional simulation to enable engineers to spot design mistakes early.

Available at the end of this month, PLDshell can be obtained by calling a local Intel sales office or the company's literature center at (800) 548-4725. Or write for Intel Literature Packet IP78, P. O. Box 7641, Mount Prospect, IL 60056-7641. Outside the U. S., contact the nearest Intel sales office.

Johns Hopkins University is offering a $10,000 grand prize for the best ideas, systems, devices, or computer programs to help disabled people. In addition, more than 100 other awards will be given. The contest categories are employment, independent living, education, and leisure. As a follow up to the competition, the university will act as a liason with manufacturers to have winning entries commercially produced and into the hands of those who need them.

Entry deadline is Aug. 23, 1991. For more information, write to Personal Computing to Assist Persons with Disabilities, P.O. Box 1200, Laurel, MD 20723.

A free disk demonstrates software that can specify, modify, and check timing requirements for digital circuits. With Chronology Corp.'s TimingDesigner, engineers can solve timing design problems by creating and analyzing timing diagrams. These diagrams, created before a schematic is drawn, can save many hours in the design phase and help avoid costly design errors that crop up when manufacturing begins. Contact the company at 2849 152nd Ave., Redmond, WA 98052-5516; (202) 869-4227.

The basics of EMI/RFI in electronic cabinets will be covered in a seminar by Equipto Electronics Corp. The seminar deals with meeting FCC and military EMI/RFI specifications as well as with Tempest concerns. For more information, contact the company at 351 Woodlawn Ave., Aurora, IL 60506-9988; (708) 897-4691; fax (708) 897-5314.

Five articles on designing embedded systems are free from Applied Microsystems Inc. Articles are written by the company's field application engineers, based on a collective experience with 12,000 systems.

The Basics of High Speed Design deals with fundamentals of high-speed digital design. *Networked Embedded Design Development Systems* covers getting the most out of development environments with efficient networks. Five types of transparency are covered in *Transparent Connections for Embedded Microprocessor Systems Design Tools.*

Event Monitor System for ES 1800 Emulators describes the features of an event-monitor system. *Programming the 8018X/80C18X Peripheral Control Block* offers engineers practical examples of how to set up the peripheral control block relocation and chip select registers. Copies are available from the company at 5020 148th Ave. N. E., P. O. Box 97002, Redmond, WA 98073-9702; (800) 343-3659 or (206) 882-2000.

Free seminars on designing with Intel Corp.'s i960 embedded processors will be held in two dozen U. S. cities from May 21 to June 27. Design examples will be given for a low-cost 16-bit external bus i960 SA/SB. Seminars run from 9 am to 12:30 pm. For cities and dates, call (800) 548-4725.

The SPARCs are going to fly.

We put SoftBench on Sun. So you can put your CASE on autopilot.

SoftBench automates all those tedious, repetitive tasks in the software development process. This gives your developers more time to think and speeds up the project life cycle, while reducing errors and rework. And now it runs on Sun SPARCstations, as well as HP and Apollo workstations.

A tool integration platform, with its own set of tools, SoftBench provides distributed computing services, tool communication, and a common user interface that's easy to learn and use. Add Encapsulator, and you can integrate your favorite CASE tools. Now and in the future. Without even having to change source code.

SoftBench will make your software development process far more efficient, cost-effective and accurate than ever before. It will protect your present and future hardware and software investments, too.

Call **1-800-637-7740, Ext. 2196** for complete product information. And get the best CASE environment under the Sun.

HEWLETT PACKARD

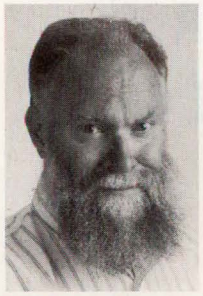
CIRCLE 89

© 1991 Hewlett-Packard Company CSSE001

WHAT'S ALL THIS "SMWISICDI" STUFF, ANYHOW?

A long time ago, I went out to dinner with Dave Ludwig, an old friend of mine from Massachusetts. We went to a fancy Italian restaurant. After we had ordered our entrées, the waiter asked, "Would you like a salad?" I declined, but Dave said he would like one. "What would you like in your salad?" Dave said lettuce and tomatoes.

In a few minutes the salad arrived. Yes, it had lettuce and tomatoes. It had three kinds of lettuce, and tomatoes and chick-peas and croutons and onion slices and green onions and Italian cherry peppers and slices of hard-boiled egg, and three kinds of salad dressing on the side. I sat there with barely suppressed astonishment, and Dave just sat there with a quiet, resigned smile. After the waiter departed, Dave explained: There was no point in complaining or griping or hollering, because at the best, the manager or the headwaiter would just come over and say, "Hey, you don't have to eat anything you don't want, and you don't have to pay for anything you don't want, so, what's your complaint? Show Me Where It Says I Can't Do It." And he explained that he was an aficionado of these kinds of stories, which we will of course abbreviate to "SMWISICDI."



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

He pulled a faded clipping from his pocket. The newspaper story was about the advantages of home ownership. "If you own your own home, you can play the piano at midnight." I thought about it. I said, "Dave, I can't play the piano worth a darn. But this story says that I can play the piano at midnight if I own my own house."

Dave smiled and agreed. "You just *think* you can't play the piano. But, have you ever tried at midnight?" I had to admit that I had not. But, one of these days, I will try playing at midnight, to see if I'm any better than at any other time. What I suspect is that at 12:00:02, I'll suddenly be a rotten pianist again.

Now I, too, have gotten interested in SMWISICDI stories. In fact, last week I mailed 5 ounces of SMWISICDI stories and clippings to Dave. For example, I clipped out a story about how the Israeli Army solved the problem of what to do when Palestinians throw stones at the soldiers. The Israeli Military invented an automated stone thrower to retaliate. An eye for an eye, a tooth for a tooth—and a rock for a rock? What if the U.S. Army sent out a Request For Quote on developing, manufacturing, and deploying a rock-thrower? What if Jack Anderson got wind of this, and confronted the Joint Chiefs of Staff? They would just tell him, "Show Me Where It Says I Can't Do It."

Last week, Wanda Garrett, our senior applications engineer for amplifiers and regulators, got a phone call from an unhappy customer. He had used one of our ICs to design a switching regulator, and it didn't work well at all. The output had glitches and burps and excessive ripple and noise. The regulation was poor, the loop stability was rotten, and the efficiency wasn't even very good.

After a lot of inquiry, Wanda discovered that this person had built up the switcher on one of those solderless breadboards. OHHH!! Patiently, Wanda explained, that is exactly what you expect when you use one of those solderless beasts. The inductances are awful, the capacitances will cause crosstalk between adjacent buses, and if you try to build a switching-type regulator, *of course* it will work badly. And the customer replied, "SMWISICDI."

Now, Wanda was a little taken aback. She had to admit, of all the things that we might have told people they should not expect to work, this was one that we didn't *specifically* warn against. But, to put the shoe on the other foot, she asked, "Where does it say you *can* do this?" And the customer replied that in the solderless breadboard's promotional brochure, it says, "Ideal for high-frequency and high-speed/low-noise circuits." Wanda observed that was probably not quite true—neither for linear circuits, fast digital circuits, fast ADCs, nor switchers. Then she pointed out to the customer that the LM2575 data sheet does spell out: "As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients that cause problems. For minimum stray inductance and ground loops, the length of the leads indicated by heavy lines should be kept as short as possible. Single-point grounding or ground-plane construction should be used for best results."

So we really *did* tell every customer that you need a good layout, right in the data sheet. Of course, if the customer *believes* that solderless breadboards are really great for high-frequency circuits, then we have a problem—which Wanda was able to resolve and explain. The solderless breadboards do cause many troubles.

First of all, most fast ICs, whether linear or digital, require a good ceramic power-supply bypass capacitor, right close to the IC. But with those long buses inside a solderless breadboard, it's hard to get a bypass capaci-

tor with less than 3 or 4 inches of loop. That won't help a switcher or any other fast circuit. Then, the capacitance between adjacent buses—typically 2 to 4 pF, depending on the size—is going to cause stray coupling that will probably make the circuit unhappy. That's my experience. Furthermore, when you have a switching transistor turning off, its collector or drain can easily slew at 600 V/μs or more. If your "catch" diode is spaced more than an inch from the inductor and transistor, the L di/dt can cause dozens of volts of overshoot, which may overstress the switching transistor (exceeding its voltage ratings), not to mention generating some horrible spikes in the air.

And those white slabs—they are *not* Teflon. They aren't polystyrene or polyethylene, either. They are made of nylon, or something similar, so the leakage can be pretty bad on a warm or humid day. Even worse, if you push a whole lot of wires into those little solderless connectors, the little scraps of solder will get scraped off until there's a whole pile of solder scraps hidden inside. Then they can start making intermittent short-circuits between adjacent buses—won't *that* be fun to troubleshoot.

So Wanda explained all of these reasons not to use a solderless breadboard for making a switcher. She sent the customer a little PC board that was neat and compact to help him get a prototype of the circuit working—one of the LM2575 "Simple Switchers." Note, we normally think that these "Simple Switchers" cannot miss—they're very easy to apply. But, if you try to build it on a solderless breadboard, even a simple circuit can be hurt—ruined—by the strays of a poor layout. Simple, yes. But foolproof and tolerant of a truly bad layout? No.

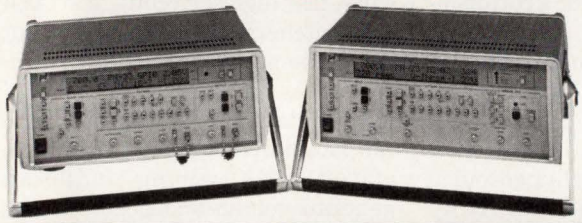
Then she warned the rest of us Applications Engineers that customers might be having trouble when using solderless breadboards, ultimately complaining "SMWISICDI." I'm just passing on this warning to you readers.

Finally, Wanda said she was going to try to put a disclaimer in our linear databooks and applications handbooks, that the "solderless breadboards" are unsuitable for any applications other than medium-speed, medium-impedance-level, and medium-precision circuits. It may sound silly, but I know that she'll find a way to put in a caution flag where it's appropriate. I mean, Wanda is the Czarina of Linear Data Books. She can put anything she wants in there. Show Me Where It Says She Can't Do It!

All for now. / Comments invited! /
RAP / Robert A. Pease / Engineer

ADDRESS:
Mail Stop C2500A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

Jump To Light Speed



gigaBERT™

Today's ultra-high speed digital transmission systems demand Bit Error Rate Test Systems with matching performance. To meet this need, Microwave Logic has developed the **gigaBERT** series of test sets. Operating in ranges from 1 Mb/s to 2.7 Gb/s, **gigaBERTs** are the ideal test and development tools for SONET systems, GaAs/ECL based circuitry, ultra-wide band optical LAN/FDDI, satellite communications and digital microwave systems.

The **gigaBERT - 660, 1400 and 2700** systems are high-speed digital pattern generators and companion error measurement detectors operating over a range of 1 Mb/s to 2.7 Gb/s. Featuring **"Four Function Auto Search Synchronization", gigaBERTs** provides painless error rate measurement and automatic clock timing, data-synchronization, pattern and polarity selection.

Jump to light speed with gigaBERTs!

For more information on the **gigaBERTs** family call or write:

Microwave Logic
20 Cummings Road
Tyngsboro, MA 01879
Tel: (508) 649-6099
Fax: (508) 649-4722

CIRCLE 91

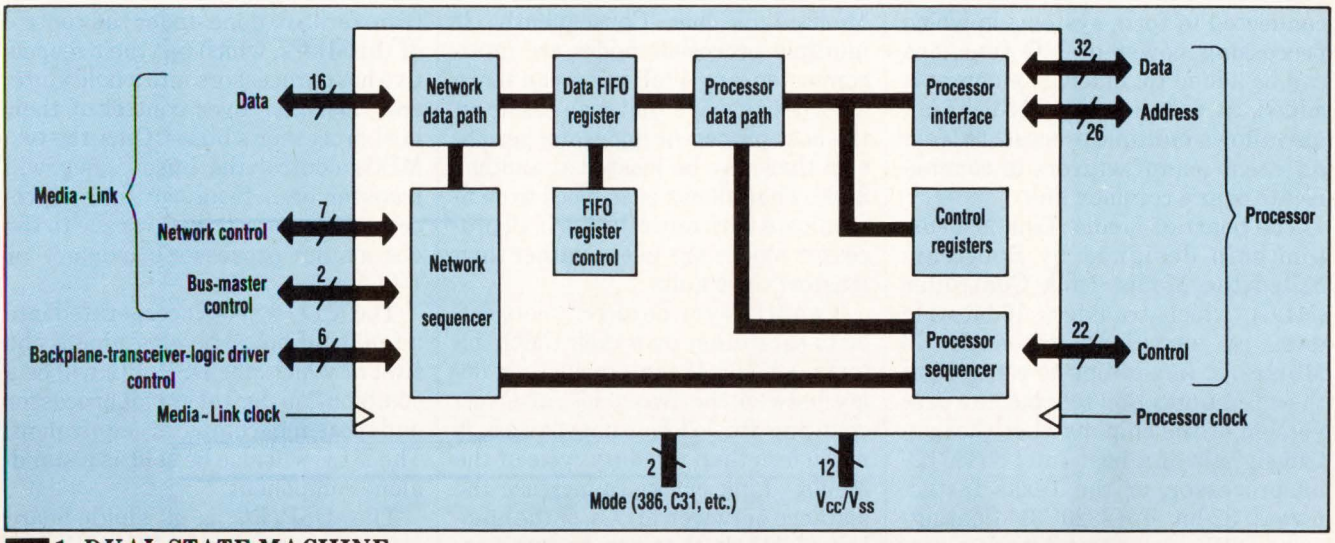
"EXCESS INVENTORY EDUCATES KIDS"

Peter Roskam,
Executive Director, EAL

Let EAL turn your obsolete inventory into scholarships for needy kids.

Every year deserving kids miss the opportunity to attend college because they lack the necessary funds. EAL helps these kids by bartering donated excess corporate inventory and services for tuition credits with cooperating colleges and universities. The result is a three-way win: the kids receive a college education, the schools enroll more students, and corporations invest in a qualified future workforce, generate great PR and possibly gain tax advantages.

If you have excess inventory or services to donate we'll put it to work for deserving students, colleges and your company. **Call EAL at (708) 690-0010.**



1. DUAL STATE-MACHINE sequencers on the Media-Link Controller from Spectrum Signal Processing supply every interface function required to tie the host processor or DSP chip to the 25-line Media-Link bus. Data is transferred over the bus at up to 66 Mbytes/s.

TAKE ON REAL-TIME CONTROL AND MULTIMEDIA NEEDS WITH A 66-MBYTE/S BUS THAT COUPLES MULTIPLE DSP AND CPU CHIPS.

FAST BUS NETWORKS CPUS, DSPS, TO BUILD MULTIMEDIA SYSTEMS

DAVE BURSKY

As the need for digital-signal-processing (DSP) functions within a desktop computer increases, so does the need for closely coupling the host CPU with coprocessor cards and digital-signal processors on motherboards. This increased DSP need is caused by a host CPU having to handle everything from modem communications to multimedia presentations. Tight coupling, however, may limit system expandability and may not even let the DSP chip use the system's resources.

By adding a second system bus dubbed the Media-Link, Spectrum Signal Processing overcomes the bottlenecks in most DSP systems. The new bus forms a high-speed interconnection system that permits DSP chips, a host processor, and I/O peripherals to communicate together over a high-speed bus, independent of the host-system bus. As a result, multiple processors can be inter-

connected to form systems in which processing power or I/O functions can be added to, much as memory is added to a computer. Media~Link also allows multiple processors from different manufacturers to communicate over a common link.

The heart of Media~Link is a custom chip designed by Spectrum called the Media~Link Controller (MLC), which transfers 16-bit-wide data at sustained rates of 66 Mbytes/s. In addition to controlling the interconnection scheme, the first version of the chip matches the control signals of a host Intel 80386 32-bit processor, or the Texas Instruments 32-bit TMS320C31 floating-point DSP chip (selectable via a control pin). The on-chip logic permits a direct connection to the desired processor and keeps the interface very simple—a two-chip solution results if no off-chip memory is needed. The noncompeting message-passing communication protocol used by the chip provides predictable responses for real-time applications—a critical requirement for many industrial control or measurement systems.

Any subsystems connected to an MLC can access the resources of any other system tied into the 25-line (16 data and 9 control lines) Media~Link bus. Consequently, if multiple processor nodes are interconnected, any or all nodes can share a hard-disk drive that may reside on the host-processor node, or a peripheral that may be located at another node. That allows each block to communicate with any other as if all processor blocks are peers, rather than master/slave units.

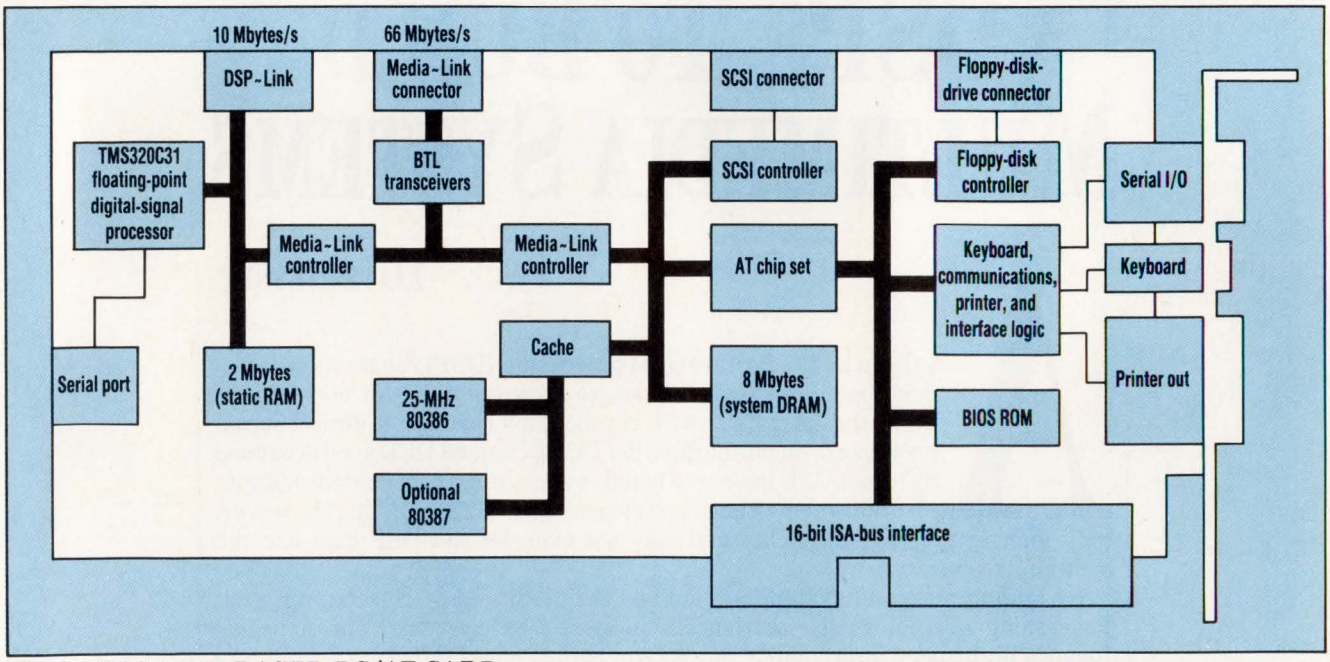
Two MLCs can be directly connected to each other over their CMOS interface buses if the propagation delay betwen the two chips, after accounting for loading impedances, is much less than the duty cycle of the Media ~ Link clock. To increase the distance betwwen MLCs, or the number of MLCs that can be interconnected, bus-transceiver-logic (BTL) buffers should be used to create a Media ~ Link backplane. The BTL transceivers allow data to be tansferred across the backplane at higher data rates than TTL circuits, without the reflection propagation delays that are normally associated with a TTL bus.

The bus thus provides a high-speed interprocessor communication path that allows data to be copied from a source processor's memory or I/O space to a destination processor's memory or I/O space. The transfers are done under the control of the MLCs, which put their respective host processors into a hold state, and then take over control of their host processor's buses. Once the two MLCs control the buses, they will transfer data from the source processor's memory or I/O space to the destination processor's memory or I/O space.

The MLC will be incorporated into a family of board-level products, the first of which, the DSP/PC, will be a combination digital-signal processor and personal-computer equivalent. The MLC will also be sold as a stand-alone component.

The DSP/PC is a single-board computer intended for PC/AT industry-standard-architecture (ISA) passive backplanes. The card includes standard peripheral interfaces for hard- and floppy-disk drives, a keyboard, and a serial port, as well as a real-time operating system and Microsoft Windows 3.0 drivers for quick startup and relatively easy programming.

All data-transfer overheads are managed by the MLC. That leaves the host and DSP nodes to go about processing data independent of each other. Based on the memory-to-memory transfer of packetized data



2. THIS 80386-BASED PC/AT CARD with floating-point DSP capability employs two Media~Link Controller chips, so that the DSP chip can talk to the PC. The two controller chips on the DSP/PC card also provide a 66-Mbyte/s gateway for further expansion.

What makes good designers great?

Top down design with System HILO™ 4.

It enhances design productivity through Language Driven Design.

It simplifies design with Source-Level Debug and an X-windows graphic interface.

Its FASTCELL™ ASIC libraries simulate submicron technology accurately. And up to eight times faster than traditional gate-level modeling while using less memory.

It has outperformed golden simulators in accuracy in several benchmarks at ASIC foundries.

It's the ideal core simulation toolkit to support a concurrent engineering environment, with simulation for logic verification, worst case timing, fault grading, and non-intrusive ATPG.

Find out more about how System HILO 4 can help you become a great designer.

Call 1-800-4-GENRAD in the U.S., or the GenRad office nearest you in Austria, Canada, England, France, Germany, Italy, Japan, Singapore, Switzerland.

GenRad

A New Way of Thinking

CIRCLE 92

through DMA channels, the MLC works in a manner similar to that of the Multibus II message-passing coprocessor that packetizes data for transmission over the Multibus. The MLC employs dual control sequencers to handle the Media-Link bus and processor interfaces *(Fig. 1)*. The on-chip logic handles all functions, such as setting priorities, establishing a connection, address generation, and error detection. These features are particularly handy for real-time applications of DSP chips. They also let each DSP chip have as much local static RAM as needed—one chip need not share the memory with another.

The MLC, which is a two-port device, ties a CPU or DSP chip to the Media-Link bus. The MLC thus serves as the common gateway to the bus. When a data transfer occurs, the originating processor sets up a description block with the parameters of the data to be sent, including the destination processor, a pointer to the data, and the length of the data block. The MLC is then activated, the processor bus stops, and the data is transferred to the destination processor under control of the MLC's DMA circuitry. The destination MLC then responds, notifying its processor that data has been received, as well as the data's origin, location, and length.

The custom MLC chip keeps system component count to a minimum—all that's needed is the MLC, the digital-signal processor, and the desired off-chip memory and peripheral functions. In addition to the CMOS logic used for the MLC, the bus interface is implemented with backplane transceiver logic so that data rates over the bus can keep up with the data rates for real-time full-motion video—an essential element of a multimedia system. The chip (and thus any board that includes it) should support real-time DSP operating systems, such as the open-signal-processor architecture (OSPA) from Spectron Microsystems Inc., Santa Barbara, Calif., and the Windows 3.0 user interface. A number of off-the-shelf applications, written under OSPA, will soon be released for fax, modem, JPEG (Joint Photographic Experts Group), and MUSICAM (masking pattern adaptive universal subband integrated coding and –multiplexing) control. MUSICAM is the audio portion of MPEG (Moving Picture Expert Group).

A typical MLC chip application will involve tying a host computer to multiple DSP chips, maximizing system throughput. At 66 Mbytes/s, the transfer rate of Media-Link is faster than most commercial buses, like the PC/AT ISA, Micro Channel, extended ISA, VMEbus, and Multibus II. A typical host system might consist of a single-board ISA computer system with a CPU, a DSP chip, and two MLC chips *(Fig. 2)*.

The computer portion incorporates a 32-bit PC-compatible processor, such as an 80386 (and optional 80387), with 8 Mbytes of dynamic RAM and cache. It also contains an MLC chip, a BIOS ROM, a dual floppy-disk controller, and a Small Computer System Interface controller. In addition, a real-time clock, keyboard, parallel, and dual serial interfaces are included. The DSP portion might consist of the 320C31 DSP chip, up to 2 Mbytes of local static RAM, a serial port, and a local expansion bus, the DSP-Link. Spectrum has provided DSP-Link for several years as an inexpensive way to add medium-speed (10-Mbyte/s) peripheral functions. The two MLC chips are connected directly to each other; they don't have to communicate through the BTL buffers. The 66-Mbyte/s bus is tapped off the chip-to-chip connections, with BTL transceivers supplying the high-speed buffering.

Able to run any PC software, the DSP/PC card can operate as a DOS-compatible system running Microsoft Windows 3.0, while the DSP chip could run the SPOX operating system developed by Spectron Microsystems. The SPOX system is one element of Spectron's OSPA, a framework for DSP applications that the company is trying to establish as a standard software interface. Applications developed under OSPA will run unaltered on Media-Link-based hardware. Some application software packages now being developed include multimedia programs for JPEG and MUSICAM, a Windows 3.0 interface, and AutoCAD.

To handle some of the multimedia applications, Spectrum defined a multimedia adapter that combines a VGA graphics output plus a TMS 320C31 DSP chip with analog-to-digital and digital-to-analog converters for audio input and output. The card will plug into the ISA bus and provides a Media-Link expansion bus. Also coming is a Media-Link DSP expansion card that contains four additional TMS320C31s, each with up to 1 Mbyte of local static RAM. The card provides up to 132 MFLOPS of computing power.

Additional hardware being developed at Spectrum includes a 386 motherboard adapter that permits users to retrofit exiting PC/AT 386 motherboards with Media-Link capability. The adapter plugs into the 80386 socket and the 80386 drops into a socket on the adapter card. That gives the MLC access to all of the CPU's signals and enables the controller to provide a local 66-Mbyte/s bus. A Media-Link prototyping card that contains the 320C31 portion of the DSP/PC card is also in the works. It has a prototyping area instead of the 80386 PC/AT logic.□

PRICE AND AVAILABILTY

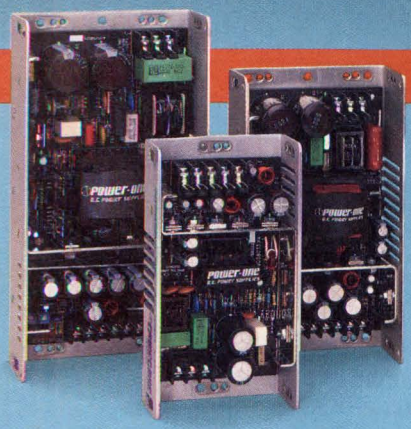
Samples of the Media-Link controller chip will be available in the early fourth quarter. The chip, to come in a 144-lead plastic quad-sided flat package, will sell for about $50 in 1000-unit lots. For large-volume users, licenses to manufacture the chip can be purchased. The DSP/PC 80386-based card will be available in the same time frame, debuting at about $3500 in small quantities. The other cards will be released in the fourth quarter of this year and through the first half of 1992. Software from Spectron will be available in the fourth quarter of this year.

Spectrum Signal Processing Inc., 3700 Gilmore Way, No. 301, Burnaby, British Columbia, V5G 4M1 Canada; Dan Cordingley, (604) 438-7266. **CIRCLE 511**

Spectron Microsystems Inc., 600 Ward Dr., Santa Barbara, Calif., 93111; David Wong, (805) 967-0503. **CIRCLE 512**

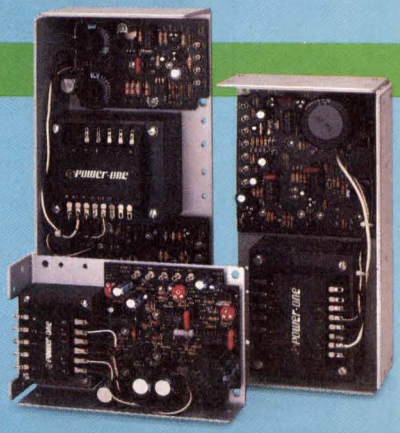
HOW VALUABLE?	CIRCLE
HIGHLY	544
MODERATELY	545
SLIGHTLY	546

POWER-ONE
D.C. POWER SUPPLIES
Not Only The Best...The Best Selection, Too



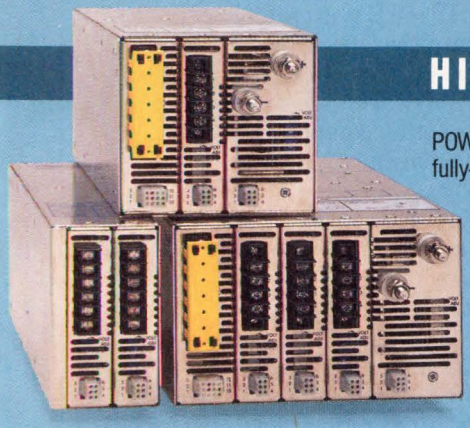
SWITCHERS

POWER-ONE'S International Switcher Series incorporates the latest state-of-the-art switching technology while providing POWER-ONE's traditional high quality at low prices. With certification to the world's toughest safety agency requirements, the series is especially suited for products sold not only domestically, but internationally as well. **• 85 models. . .40 watts to 400 watts • Efficient. . .reliable. . .economical • VDE construction • Up to 5 fully regulated outputs • Full international safety and EMI approvals**



LINEARS

POWER-ONE'S International Linear Series is the world's undisputed leader in versatile, cost-effective linear power supply products. A long-time favorite of designers and engineers worldwide, the series is the most widely purchased power supply line through distribution in the industry. The most popular voltage and current combinations are available in a wide variety of off-the-shelf standard models. **• Popular industry standard packages • 77 models. . . 6 watts to 280 watts • ±0.05% regulation • Up to 4 fully regulated outputs • Worldwide safety approvals**



HIGH POWER

POWER-ONE'S International High Power Series is the industry's only true fully-modular high power product line. Specify a power system that meets your exact requirements from a wide selection of single, dual and triple output plug-in power modules. Virtually any combination of output voltage and current rating can be delivered from stock. **• 500 watts to 1500 watts • Fully modular construction • Up to 15 fully regulated outputs • UPS battery backup option • Paralleable outputs with current sharing**

TOLL-FREE LITERATURE HOT-LINE: (800) 678-9445

POWER-ONE offers one of the largest selections of switcher, linear, and high power standard models in the world. So, whatever your D.C. power supply requirement calls for, make POWER-ONE your first choice and be sure you're getting the best—not only in quality, but selection and value as well. Call today for our new 1990 catalogs.

"Innovators in Power Supply Technology"

POWER-ONE
D.C. POWER SUPPLIES

POWER-ONE, INC.
740 Calle Plano • Camarillo, CA 93012-8583
Phone: (805) 987-8741 • (805) 987-3891
TWX: 910-336-1297 • FAX: (805) 388-0476

CIRCLE 140

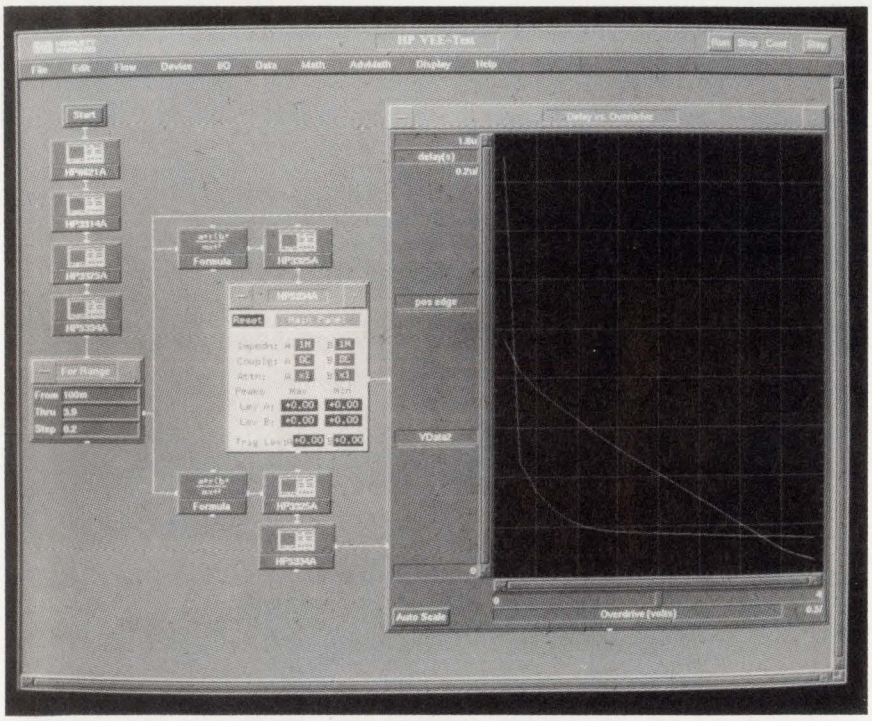
ICON-BASED SOFTWARE LETS ENGINEERS BE ENGINEERS

A VISUAL ENGINEERING ENVIRONMENT FREES ENGINEERS FROM THE CHORE OF PROGRAMMING TEST CONTROLLERS.

JOHN NOVELLINO

Computerization has been a boon to design engineers performing test and measurement tasks integral to the product development process. But computerization isn't without its downside. As products—and testing—became more complex, some engineers wondered whether they were hardware designers or computer programmers.

The result has been a number of object-oriented, icon-based programming tools that let designers concentrate more on the test at hand and less on the programming task. The Hewlett-Packard visual engineering environment (VEE) software takes this concept to the ultimate level, completely freeing users from the need to know any high-level-language syntax, semantics, or rules. Designers merely link the HP VEE icons into an intuitive block diagram on the display. The software then executes the completed block diagram *(see the figure)*.



THIS HP VEE-TEST APPLICATION measures a comparator's delay versus overdrive voltage. The icons on the left make up the block diagram that the software executes. The results are displayed on the XY plot. Clicking the mouse on an instrument icon brings up the full soft front panel, as shown for the HP 5334A.

The VEE consists of two products aimed at a wide range of computer-aided prototyping, experimentation, and testing. HP VEE-Engine is general-purpose software that analyzes and presents data either collected from a file or generated mathematically. An expanded version, HP VEE-Test, is intended specifically for instrument control. It includes icons that allow data collection from more than 170 HP instruments, as well as from non-HP instru-

The Management Collection

Books selected to help you approach difficult business situations more knowledgeably.

Order your review copies now!
Call toll-free 800-321-7003
(in Ohio 216/696-7000)

LEADERSHIP

R75 Surviving the Crisis of Change — Honing Your Management Skills

In today's fast-paced business world it is not always easy to find the best answers to difficult questions. This series of forty articles is a collection of Industry Week's best information dealing with change that affects managers' professional as well as personal lives. You'll learn how to gain control over difficult problems that you encounter every day. Articles include . . . Expand Your Career by Expanding Yourself; The Politic Game; Surviving a Takeover; When Values Collide; and many more.

124 page .... softbound $22.50

R85 How to be a Better Leader

Frederick Herzberg, Daniel Yankelovich, Charles Day, Perry Pascarella and others in classic articles about the changing expectations of today's workforce and how to deal with them. Included are: Selecting Your Management Style, Dealing With Your Subordinates, Motivating Your Workers, and more.

98 pages . . . softbound $17.50

R09 Your Toughest Tests As A Manager

This book guides you in assessing your own management skills and helps you to develop the strong leadership capabilities you need to be a more effective manager. Articles include: Developing a Flexible Management Style, Motivating Without Manipulating, Handling Creative Staff Members, Dealing With Conflict, Delegating Without Losing Control, and many more.

57 pages . . . softbound $15.00

R87 the Unhealthy Executive and Some Practical Cures

Managing in an age of anxiety can drive executives into dangerous responses. This book keys on emotional awareness. It shows you how to recognize potential problems and how to deal with them.

72 pages . . . softbound $16.00

R89 Future Focus: Advancement and Leadership Strategies

Should you plan your career — or just let it happen? Are you using strategies that build success or deter advancement? These are a few of the topics you'll find discussed in a series of articles ranging from career planning to executive management skills.

117 pages ... softbound ... $18.00

MOTIVATION

R88 Herzberg on Motivation

What can the manager do for himself and for his subordinates to overcome the "burnout" caused by the increasing abstraction of work and work relationships? Why is scientific management not the answer to increasing productivity? This book answers all these questions plus many more . . . from problems that might surface in trying to make participative management work to effective leadership in a period of psychological depression . . . this book has it all.

80 pages ..... softbound
third printing $22.50

LEGAL

R80 Right Off The Docket

This book is an invaluable reference source of more than 140 industrial accident and occupational illness claims. The index provides a cross-reference for each case by type of injury and the judicial ruling set forth so that you can quickly turn to those cases of particular interest.

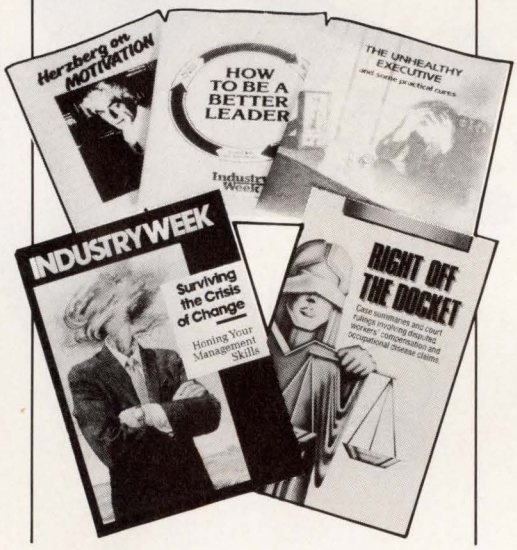
130 pages . . . softbound $10.00

MANUFACTURING

R72 Strategic Manufacturing

This complete series of twenty-four articles analyzes some of the key issues management must face in developing effective strategies in the years ahead. The articles discuss "how" to link manufacturing with all of the functional departments of an organization so they work with a broad, corporate view of their goals. Articles include . . . Ten Ways to Mismanage Technology; Learning From Foreign Strategies; CIM . . . Walking Through Fire; Challenging Tradition; and much more.

94 pages .. softbound .. $19.50



FINANCE & ACCOUNTING

X38 Managerial Accounting for Non-Financial Managers

You'll work as a company controller in this programmed learning course. You'll learn to properly record all the company's business transactions . . . sales, inventory purchases, operating expenses, depreciation, equity changes, disposal of assets. When the company's fiscal year ends, you'll prepare the annual report, balance sheet, income statement, and the statement of source and application of funds. When you've finished the course, you'll understand better the role of accounting and how to use the information accounting gives you to be a more effective manager.

Two volumes—course book and workbook $27.50

X29 How To Read a Financial Report

Written in programmed learning format, this book will review the accounting process, tracing the steps from the actual sale to the appearance of the transaction on the financial statements. Then you'll learn how to assess financial position and performance of your company through the use of ratio analysis—analyzing liquidity, activity, profitability, and coverage ratios.

140 pages .. spiral bound .. $19.50

BUSINESS STRATEGY

R70 Strategic Management

Getting a fix on your competitive position, Establishing a clear purpose for the corporation, Meshing the corporate purpose with the individual goals of your people, and Getting their commitment. This collection of ten articles will help show you ways to foster greater vision of your corporate purpose and techniques for combining the human and technological factors needed for good decision-making.

34 pages . . . softbound $7.00

To order these books, just fill out the coupon below and mail to:

Penton Education Division
1100 Superior Avenue
Cleveland, Ohio 44114

Please send the books indicated. I understand that I can review them for 15 days and, if not satisfied, return them for full refund or credit.

Item #	Quantity	Item #	Quantity
R09		R87	
R70		R88	
R72		R89	
R75		X29	
R80		X38	
R85			

Orders under $15.00 must be prepaid.

☐ My payment is enclosed for postage-free shipment in the U.S. and Canada.
☐ Bill my company and include postage and handling charges. My purchase order is enclosed.
Charge my ☐ Mastercard ☐ Visa ☐ American Express Card
Account No. _____ Exp. Date _____
Name _____
Company _____
Address (not P.O. Box) _____
City _____ State _____ Zip _____
Signature _____

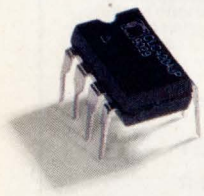
Penton Education Division
1100 Superior Avenue • Cleveland, Ohio 44114

Because you're thinking fast...

Our new high-speed op amps take voltage feedback to a new level.

You've trusted Comlinear for the best current feedback op amps since 1982, when we introduced the technology. But sometimes you prefer voltage feedback. So now, we've put our knowledge, experience--and innovation--to work there too. With outstanding results.

4X the slew rate, 1/5th the power and unity-gain stable.

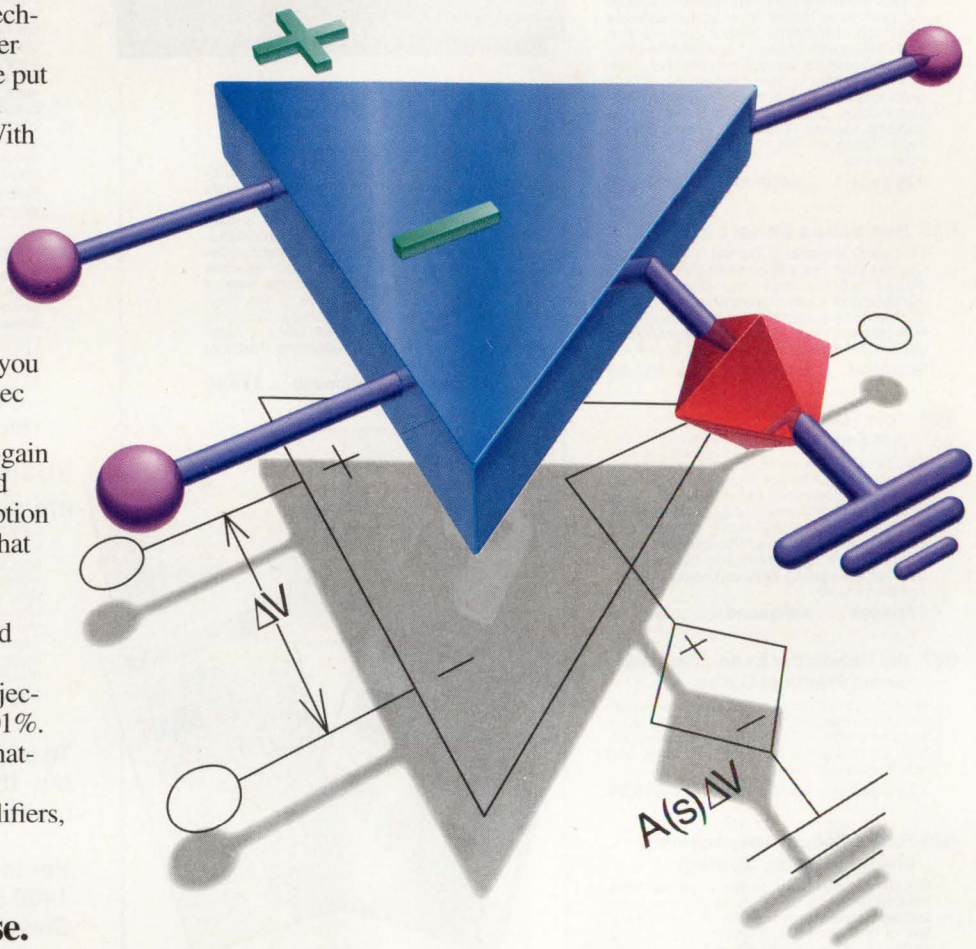


Our new CLC420 gives you a fast 1100V/µsec slew rate and 300MHz unity-gain bandwidth. And power consumption is just 40mW @±5V. Compare that to the voltage feedback op amps you're now using.

On top of that, you get matched inputs, low input bias and noise currents, high common-mode rejection, and fast 18ns settling to 0.01%.

All that makes the CLC420 a natural for active filters, differential amplifiers, transimpedance amplifiers, and DAC post-amps.

CIRCLE 187



High gain and low noise.

Another new voltage feedback op amp is the CLC422. It delivers a 300MHz bandwidth at A_V=32 with voltage noise of just 2nV/√Hz.

Call today and see how these new voltage feedback op amps can help you set new performance levels of your own.

CIRCLE 188

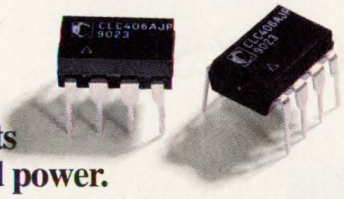
Comlinear Corporation

Solutions with speed

4800 Wheaton Drive
Fort Collins, CO 80525
(303) 226-0500
1-800-776-0500 (USA)

©1991 Comlinear Corporation

Consider these high-level current feedback amplifiers.

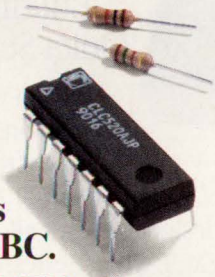


Fast op amp cuts cost and power.

For only $4.25* ea. (1000s) the CLC406 provides 160MHz small-signal bandwidth ($2V_{p-p}$) at only 50mW power dissipation (±5V). It's your low-cost answer for remote-site applications, video systems, or driving/buffering fast data converters.

*U.S. price only

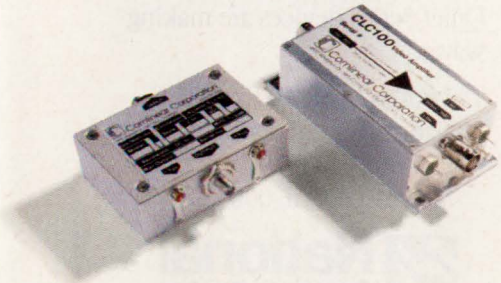
CIRCLE 189



Now, high-speed AGC is easier than ABC.

Take the new CLC520, add ±5V and two resistors, and you have a total high-speed AGC solution for fast variable-gain applications. 160MHz small-signal and 100MHz gain-control bandwidth—with a 40dB range from max. gain—give you a very flexible solution in a single 14-pin DIP.

CIRCLE 190



Modular amplifiers... ready to go.

For bench or system use, this family of dc-coupled modular amplifiers gives you complete amplifier solutions. Including PMT amps, cable drivers, post-amps, very-low-distortion amps, or amps with gain and I/O impedances that you can select.

CIRCLE 191

ENGINEERING SOFTWARE

ments through direct I/O elements.

HP tried to make the VEE software as easy as possible to use, while still maintaining functionality. The result is a comprehensive set of icons chosen to simplify data collection, analysis, and presentation. Users choose from among engineering elements, such as virtual sources, accumulators, and timers, and then define the data flow by linking these elements into a block diagram. All icons are named, making them easy to recognize and intuitive to use.

"Overhead" steps are eliminated. For example, the details of creating, appending, opening, reading, writing, and closing a file are handled transparently by the VEE software, rather than requiring a separate icon for each operation. In addition, the procedure for sending sequences of strings and numbers to an instrument is simplified. Instead of converting all numbers to strings and concatenating the whole sequence, users specify the numbers and strings in one transaction. The VEE-Test then converts and concatenates the numbers automatically.

To further help users who are unfamiliar with programming techniques, HP VEE accommodates a large number of interchangeable data types. In addition, all objects accept any data type without user intervention. For instance, users can supply a time-domain waveform to a spectrum-display icon, which needs frequency-domain data. HP VEE will automatically run a fast Fourier transform on the input to make the conversion.

Users can collect data from HP-UX files, standard in (a Unix communication method), communication programs, and programs written in C, Pascal, and Fortran (HP-UX is based on and fully complies with AT&T's Unix system). HP VEE-Test accepts data from HP Basic/UX programs and named pipes (Unix data-transfer techniques), in addition to instruments. During setup or when external sources are unavailable, the software's internal data generators can supply simulation signals. The HP-IB (IEEE-488), RS-232, and general-purpose input-output (GPIO) interfaces are supported.

Analysis icons include most math functions, calculus, regression analysis, probability, statistics, and others. Some of the engineering functions available are FFTs, data filtering, digital-signal processing, and distributions.

To increase flexibility in more complex applications, HP VEE has several flow-control objects, including repeat and conditional objects. Moreover, standard objects can be grouped into customized modules called UserObjects. Users can choose from XY or Y plots, strip or polar charts, complex planes, waveforms, and several frequency plots to present their data.

In the debugging mode, four features help users troubleshoot their applications. Line Probe shows which objects are connected by a specific line, as well as the type and value of data flowing through the line. Show Data Flow and Show Execution Flow allow users to see the data flow or the sequence in which objects are executed. Finally, users can set breakpoints at specified points to stop execution for examination.

The completed application can be viewed in two ways. The detail view shows every icon. The panel view lets users display only a desired subset of icons—input and output devices, for example. This feature creates a simplified interface that can be secured to prevent unauthorized access.

HP VEE-Engine and VEE-Test run on HP 9000 Series 300 or 400 systems with HP-UX 7.0 and X Windows. Minimum RAM needed is 8 Mbytes.□

PRICE AND AVAILABILTY

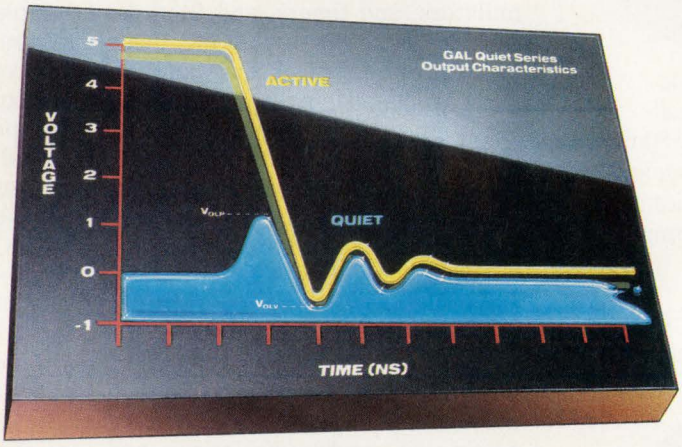
HP VEE-Engine (HP E2100A), the general-purpose analysis and presentation software, costs $995. HP VEE-Test (HP E2110A), which adds instrument I/O and control functions, is priced at $5000. Delivery is in 4 weeks.

Hewlett-Packard Co., Measurement Systems Operation, P.O. Box 301, Loveland, CO 80539; (800) 752-0900. CIRCLE 513

HOW VALUABLE?	CIRCLE
HIGHLY	547
MODERATELY	548
SLIGHTLY	549

National Semiconductor

Introducing the wave of the future. The industry's first and only low-noise GAL devices.



Silencing device noise with our new GAL® Quiet Series™ family.

The tide of events for CMOS-based logic is sure to change course with the introduction of our new GAL Quiet Series devices. Because now you can design in high-speed logic devices without having to design out noise.

Through our advanced proprietary circuitry, we keep noise to a bare minimum. Our GTO™ (Graduated Turn-on Output) circuit, which retards the output buffers, results in smoother edge rates, diminished output undershoot, and greatly reduced ground bounce (V_{OLP} max of 1.5V).

What's more, these devices utilize unique ground and power buses, which effectively isolate inputs from output noise and improve dynamic threshold.

	V_{OLP}	V_{OLV}	V_{ILD}*	V_{IHD}**
National	1.18	−.62	1.40	1.78
Competitor A	2.06	−.66	1.10	1.83
Competitor B	1.58	−.66	1.39	1.62
Competitor C	1.46	−1.08	1.09	1.56

*V_{ILD}—Dynamic Input threshold low **V_{IHD}—Dynamic Input threshold high

Minimizing system noise.

Not only will our high-speed GAL QS devices improve your system performance, they'll reduce your overall system noise. And that means extraneous noises like Electromagnetic Interference (EMI), crosstalk, and ringing, the effects of which often result in false clocking.

Delivering higher speeds at 1/2 and 1/4 the power.

What more would you want in a GAL device other than high speed and low noise? Our answer is less. That's why we offer reduced-power versions of our 15ns devices. Which means now you can get half- and quarter-power GAL devices —in either 20- or 24-pin DIP and PLCC packages —that draw a max I_{CC} of 90mA and 55mA respectively at 15MHz.

Building on our Quiet Series heritage.

When we designed our low-noise GAL devices we talked to the experts. National's team of ACMOS logic designers. After all, they invented FACT Quiet Series, which is globally accepted as *the* quiet standard. And now standard on our new GAL devices.

Riding the crest with National.

For samples, call or write us today. And find out why our new GAL Quiet Series devices are making waves.

1-800-NAT-SEMI, Ext. 125
National Semiconductor Corp.
P.O. Box 7643
Mt. Prospect, IL 60056-7643

National Semiconductor

Quiet Series and GTO are trademarks of National Semiconductor Corporation.
GAL is a registered trademark of Lattice Semiconductor.
©1991 National Semiconductor Corporation

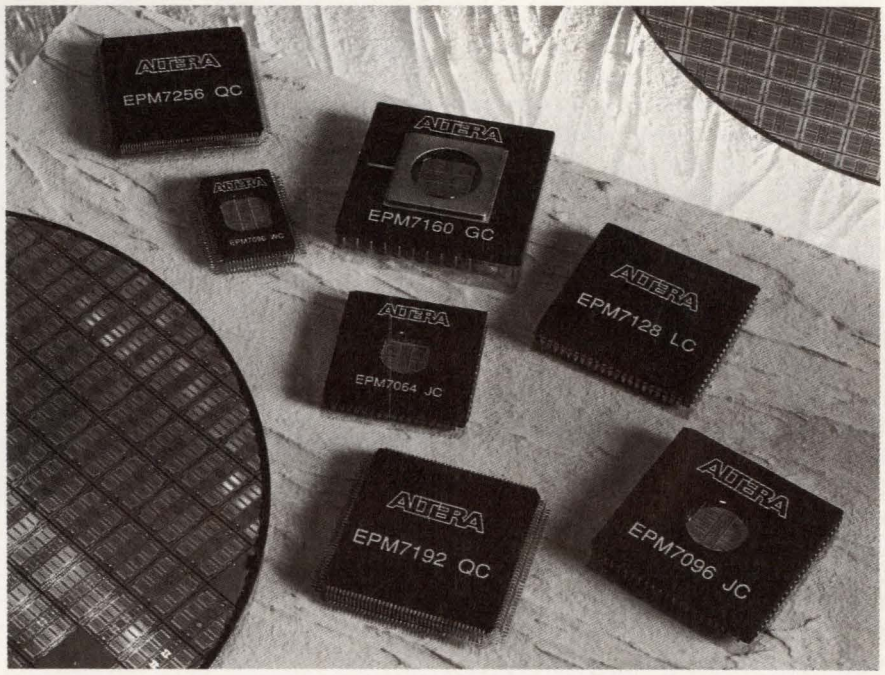
SECOND-GENERATION MAX FAMILY BOOSTS DENSITY FIVEFOLD

DAVE BURSKY

With multiple architectural enhancements put to work, the Max 7000 family of ultraviolet-erasable programmable-logic devices gives designers from 4000 to 40,000 available gates—up to five times more than most other high-density programmable chips. Furthermore, not only will the chips offer some of the highest complexities for PLDs, but they'll have some of the shortest logic-propagation delays—as short as 15 ns from one input, through the array, and to an output for complex parts. In all, Altera plans to offer ten members in the family, with pin counts ranging from 68 to an industry high of 288 pins for PLDs.

To achieve the short delays and permit global clock speeds of 70 MHz, designers developed a low-skew programmable interconnect array that keeps skew to less than 2 ns. They also developed an enhanced macrocell that supports complex logic functions with up to 32 product terms. In addition, the macrocell library and design tools enable users to select various speed and power options for the cells to optimize the logic path during chip configuration. This power-saver feature allows individual logic macrocells to operate at full power with the shortest delay, or at one quarter the power with moderate speed (the speed penalty is less than 10 ns). Because only speed-critical paths need to run at full power, company designers estimate this can reduce overall chip power consumption by 20 to 50%.

The macrocells include a new logic structure Altera refers to as parallel logic expanders. Expanders permit complex logic functions to be implemented without incurring significant additional gate delays. Macrocells can borrow product terms from adjacent macrocells when complex functions of more than 5 product terms are needed. Incremental delays to build the complex functions are less than 2 ns per macrocell.



One key aspect to improving the overall array speed was the removal of the EPROM configuration elements from the direct signal path. By removing them, signal propagation delays are shortened by more than 10 ns when compared to the previous Max 5000 family. Between any two logic array blocks, there's only a fixed delay, which is unlike the Max 5000, which had a variable routing delay.

In the array's I/O control block, the I/O pins are decoupled from the macrocells so that the I/O pin and macrocell can be used independently of each other. Configurable registers in the macrocell can be set as D, T, S-R or J-K flip-flops, and have a programmable Clock Enable line. Global control signals feeding the register include Clock, Clear, and Output Enable.

In some speed comparisons of circuit functions implemented in the already available Max 5000 series and the forthcoming Max 7000 series, Altera examined the performance of four blocks—a 16-bit counter, a 16-bit adder, a 16:1 multiplexer, and a 16-bit decoder. The counter exhibited a 40% speed improvement, while the other three showed a 120 to 140% speed boost when implemented with the Max 7000 devices.

Software support for the Max 7000 series will be provided by the company's Max+Plus II design software package that operates on a PC under Microsoft's Windows 3.0 graphical environment. Data entry can be done through schematics, waveforms, or Altera's hardware-description language. As part of the toolset, a compiler can automatically minimize the logic and synthesize an optimal fit of the design to the Max architecture.

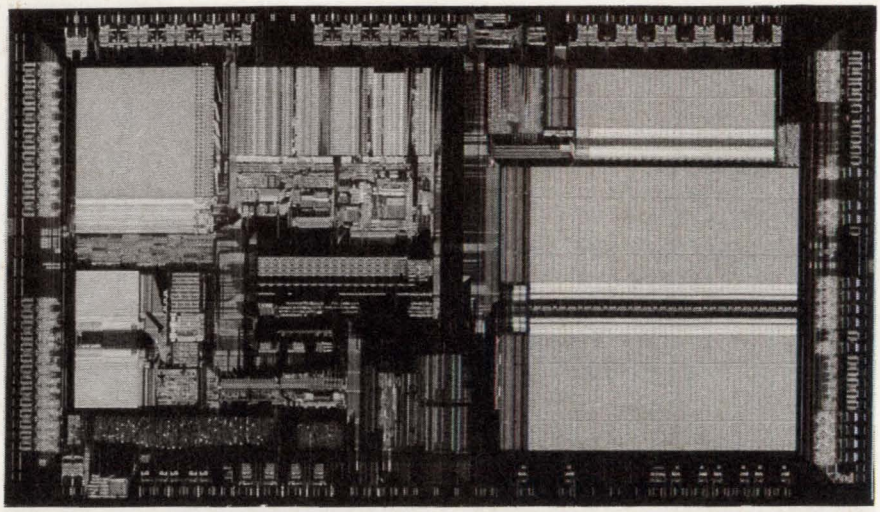
Max 7000 series devices will come in a reprogrammable, windowed, ceramic package, and in a one-time-programmable plastic package. Depending on chip pin count, the package options include PGAs, PLCCs, and PQFPs. The first two devices—the 10,000-gate EPM7256 and the 4000-gate EPM7096—will be sampled in the fourth quarter of this year, with the others to follow during 1992.

Altera Corp., 2610 Orchard Parkway, San Jose, CA 95134; Stan Kopec, (408) 984-2800. **CIRCLE 301**

REVAMPED VERSIONS OF 29000 RISC CPU UP PERFORMANCE, TRIM COST

DAVE BURSKY

A pair of additions to the Am29000 family of 32-bit RISC processors gives designers both higher-performance and lower-cost options for applications employing the RISC CPUs. For higher-performance, Advanced Micro Devices created the 29030, which replaces the small branch-target-cache (BTC) memory with an 8-kbyte instruction cache. Not only does that improve processing throughput, but it eliminates one of the three 32-bit buses the original 29000 requires. That, in turn, allows the chip to be housed in a smaller (144-lead PGA or PQFP) and less-costly package. The other chip, the 29035, is pin-compatible with the 29030, but has only half the cache (4 kbytes). That cache is also simpler: It's direct-mapped rather than two-way set-associative to reduce chip complexity, thus lowering the price.



The BTC was replaced with the two-way set-associative 8-kbyte instruction cache to reduce the number of off-chip instruction accesses needed for programs or program loops that exceeded the size of the BTC on the older chip. The cache is accessed in the same pipeline stage as was the BTC, As a result, instruction response timing is identical to that in the previous chips. The store array, tag array, and valid array portions of the cache are all accessible under program control. That permits all entries to be read or written to ease testing or allow specific patterns to be preloaded. A control register also enables the cache to be left unlocked or be locked when portions of the contents must be write-protected, or be enabled or disabled. Half or all of the cache can be locked. When half is locked, the other half becomes a direct-mapped cache suitable for applications that require time-critical code to always be cached.

The bus protocol of the 29030 was designed to run with clock frequencies of more than 50 MHz, but without requiring large amounts of high-speed external memory. To ease system design, the input clock can be a TTL signal with a duty cycle that can range from a 30:70 to a 70:30 ratio and runs at the same frequency as the internal clock frequency of the processor. A proprietary clocking scheme allows the chip to use high-frequency clocks without undue silicon costs. A bidirectional Memory Clock signal on the processor is used as the timing marker for all setup and hold requirements for memory accesses. The signal can be either a copy of the Input Clock signal or a divide-by-2 version of the Input Clock signal, based on the state of a Division control pin. Consequently, the memory bus can be run at either full clock speed, or at half the speed (for example, when a 25-MHz system is upgraded with a 50-MHz CPU module, and the memory subsystem must stay at the older clock rate).

Some new protocols are adopted by the 29030 for single and burst-mode accesses. Those activities are controlled by the Request and Burst signal pins which are used together to indicate which of four different accesses is being performed on external memory. Additional support for narrow ROM, Page mode, and interleaved memory gives designers more flexibility for optimizing system cost. An output line also gives the outside world a signal to indicate whether or not the processor is performing an 8- or 16-bit access. The CPU also knows how many bytes or 16-bit words to transfer.

As part of the new bus structure on the 29030, AMD designers included support for the JTAG IEEE P1149.1 standard for boundary-scan testing, to aid in system board testing. Future extensions of boundary-scan technology will make even more extensive use of the boundary-scan test features for internal testing, so that a high level of fault coverage can be obtained.

Initial versions of the 29030 will run at external clock frequencies of 25 MHz. The simpler 29035 will initially come in 16- and 20-MHz versions and will only be available in the 144-lead plastic quad-sided flat package. In lots of 1000, the PGA 25-MHz version of the 29030 sells for $147, the 33-MHz version will go for $184, and a 40-MHz version will be released in the latter half of this year. Pricing for the 16-MHz version of the 29035 goes for just $76 each in 1000-unit lots. Samples of the 25-MHz 29030 are available from stock, while samples of the 29035 will be available in the third quarter.

Advanced Micro Devices Inc., 5204 E. Ben White Blvd., Austin, TX 78741; (512) 462-4840. **CIRCLE 302**

MIDRANGE-DENSITY FPGAs DELIVER MORE FEATURES

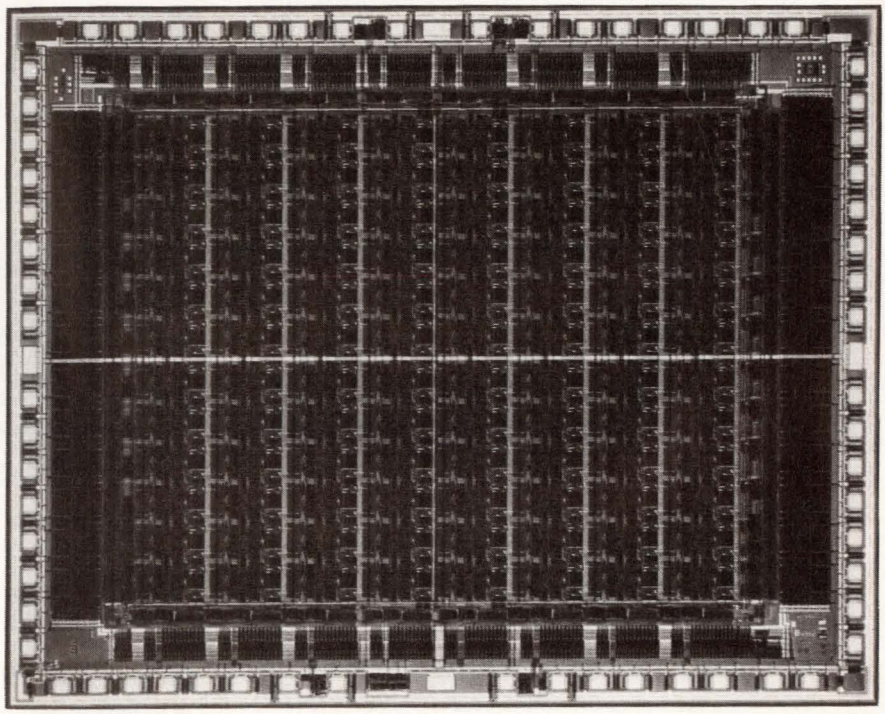
DAVE BURSKY

Right on the heels of Altera's Max 7000 family of high-density PLDs comes a family of high-density field-programmable gate arrays. The QuickLogic family of pASIC chips will range in usable gate counts from about 500 to 4000, with minimum pin-in-to-pin-out propagation delays of about 15 ns, with most of that time consumed by the I/O buffers. Internally, such functions as 8-bit counters can run at over 100 MHz, and larger 16- or 32-bit counters can hit 90 MHz and higher. In contrast, the company claims most other FPGAs can't obtain counter speeds of more than about 50 MHz.

The CMOS logic typically consumes just 25 mW during standby, and about 1 W when clocked at full speed. The programming approach employed is based on a new, antifuse programming element that requires much less area than the structure employed by Actel Corp., the only other company that employs antifuses. The resulting areas of the pASIC chips are much smaller than those of similar capacity from Actel.

Not only are the fuses smaller, but their resistances are lower—just 50 Ω (typical) versus several hundred. That low resistance value and the small size also help keep circuit performance high and power consumption low. Parasitic losses can be kept to a minimum. The ViaLink fuse material is deposited into small window regions (vias) etched in the dielectric layer that separates the two metal interconnection layers. When a programming voltage is applied to the two metal layers, a short-circuit path is formed in the filled-in window region between the two conductors.

Each pASIC consists of a regular array of logic cells, with each containing the equivalent of 30 gate-array gates, of which 12 can be used in any typical application. Contained in each cell are AND gates, multiplexers, and a register element, all interconnected by the metallization grids



and the ViaLink antifuses. Logic functions up to 14 inputs wide, including arithmetic, counter, data path, state-machine and "glue"-type gates, can all be implemented.

In the QL8X12, one of the smaller arrays in the family, there are 96 cells, or 1152 usable gates. The chip is referred to as a 1000-gate device. The chip comes in a 68-lead package. In the design stage are two other chips, the QL12X16 and the QL16X24, which pack 192 and 384 logic cells, respectively. The first comes in an 84-lead package, while the largest one employs a 160-lead package. The 192-cell chip packs about 2000 equivalent gates, while the 384-cell chip has about 4000 equivalent gates. All chips have built-in serial-scan-path circuitry to ease the testing problem and allow automatic-test-vector generation.

A set of design tools—the pASIC Toolkit 3.0—support the development of configuration patterns. The tools run under the Microsoft Windows 3.0 graphical user interface on PCs. Circuit designs can be captured with ECS, a graphical schematic-entry tool from the CAD/CAM Group Inc., Cupertino, Calif., and simulated with X-SIM a tool from Silicon Automation Systems Inc., San Jose, Calif. Both tools are included in the toolkit. A design library with over 200 macrocells covers most frequently used blocks, including popular 7400-series TTL. The SpDE (seamless ASIC design environment) has an open, ASCII interface that allows third-party tools to easily be added. In addition, QuickLogic plans to port their tools to the Sun SparcStation family. The toolkit also includes automatic placement and routing software, a physical viewer/editor, a delay modeler, and a device programmer, all for $3995.

Samples of the 1000-gate QL8X12 will be ready in the third quarter, with full production slated for the fourth quarter. In 1000-unit lots, the chip will sell for $75 each.

QuickLogic Inc., 2933 Bunker Hill Lane, Santa Clara, CA 95054; David Laws, (408) 987-2000.

CIRCLE 303

advertisement

CAE Technology Report

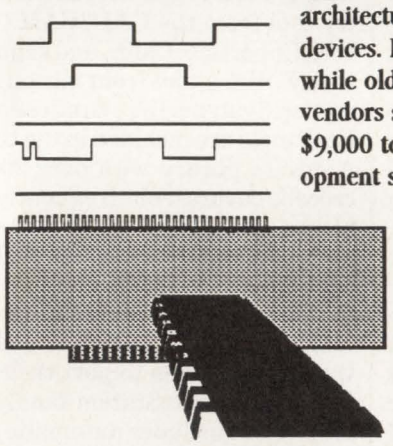
May 1991
Vol. 3, No. 5

Upgrades for Mentor, OrCAD and Viewlogic

SUSIE Concurrent Designer™ has been upgraded with interfaces to Mentor™, OrCAD™ and Viewlogic™. This allows these popular data entry tools to work directly with the real-time SUSIE simulator. Designs take only seconds to load. Operating in real time, SUSIE allows for instant design and test vector modifications without any compilations. All changes to JEDEC, hex files, FPGA designs, IC technologies, etc., can be performed while simulation is in progress. Equipped with a software accelerator, SUSIE allows the designer to select any design section and simulate at a speed that is totally independent of the design size. This has created a renewed user confidence about board level simulation. The SUSIE simulator is an excellent upgrade of Mentor, OrCAD and Viewlogic CAE tools that pays for itself typically within the first sixty days. **CIRCLE 101**

FPGA Competition Shifts to CAE Tools

With more entrants into the FPGA field, the product differentiation is becoming vague. For this reason, the new FPGA vendors stress the design environment and applications over the architecture of their devices. For example, while older FPGA vendors still push the $9,000 to $12,000 development systems, there are rumors that newer entrants, like PLUS LOGIC, will be announcing highly advanced simulation tools for under $500.



Even more important, these new CAE tools will take only hours to learn and will be easy to use due to their real-time interactive operation. Also, simulation of multiple FPGAs at the board level in excess of 200,000 gates will be possible with optional software.

■ ***SUSIE*** (Standard Universal Simulator for Improved Engineering) and ***Concurrent Designer*** are trademarks of ALDEC Co., Inc. Newbury Park, California, USA. **TEL: (805)499-6867 FAX: (805)498-7945. To obtain a free working model of these tools please contact ALDEC.**

Xilinx™, ACTEL™ Forge Ahead

With a growth rate of over 50% per year, field programmable gate arrays (FPGAs) have drawn so much attention from semiconductor vendors that most of them will have FPGA parts ready by the end of 1991. However, it is expected that Xilinx and Actel will retain their technological leadership, particularly now that designing with these parts has become quick and simple. Thanks to real-time SUSIE development tools from ALDEC one can simulate these parts at chip and board level with an accuracy of 10 picoseconds. Since SUSIE allows for selective circuit simulation, you can simulate the FPGA parts cell-by-cell, section-by-section, IC-by-IC and/or any combination thereof. This dramatically speeds design development over the previously employed methods. **CIRCLE 102**

Cost - A Leading CAE Factor

With purse strings still tight, many CAE vendors find that their lower cost products are moving faster. Designers are particularly buying products that automatically create design documentation, handle archives and do other basic chores at affordable prices. For example, SUSIE simulator ($995) which allows designers to save, print, and archive design revisions, test vector files, error conditions, etc., is being purchased in greater numbers. Perceiving this shift to low-cost CAE environments, some workstation CAE vendors are talking to the PC CAE vendors about tool integration and licensing. This recession has considerably helped high performance PC-based CAE to gain ground on the expensive workstation-based CAE tools.

Real Cost of CAE Tools

Experienced CAE users are much more careful in selecting CAE tools than novices. While novices look primarily at price and features, the experienced users focus mainly on ease of use, because the data base built around any CAE tool may quickly represent ten times the value of the CAE purchase price. Tools that work in real-time save the most. They save at least four to ten times more than those working in batch mode because: they are free of any software compilations and designers are much more effective when they debug designs in real-time. SUSIE, the logic simulator that is resold by most CAE vendors, is the only existing real-time simulator. It provides the most cost effective design environment available today. **CIRCLE 105**

Actel, Xilinx, Mentor, PlusLogic, ViewLogic and OrCAD are trademarks of their respective holders.

GRAPHICS PROCESSOR ACCELERATES X-WINDOWS

Providing hardware support to accelerate such common graphics operations as bit-block transfers (BitBLTs), line drawings, polygon fills, clipping, and more, the MB86990 graphics system processor ties into most RISC and CISC CPUs. The chip, jointly developed by Fujitsu and AFE Displays Ltd., Birmingham, U.K., operates at clock rates of 40 MHz and offloads the host processor from the graphics computations.

The graphics processor can support 8, 24, or 48 bits/pixel, including a 16-bit Z buffer and an 8-bit transparency buffer, and addresses a 96-Mbyte memory space. Image maps of up to 4096-by-4096 pixels can be supported by the large memory space. Direct interfaces for either video RAMs or standard dynamic RAMs enable the designer to effect various cost/performance tradeoffs. An on-chip programmable video-timing controller handles just about any CRT parameter, and supplies the synchronization and blanking control signals.

Triple on-chip FIFO buffers keep all of the video data buffered so that both the host-system and video-RAM interfaces can operate at maximum transfer rates. When running at 40 MHz, the chip can transfer 32 Mpixels/s (8-bit pixels) for BitBLTs and 200 Mpixels/s for screen fills. Development tools for the GSP include a software emulator, both 2D and 3D graphics libraries, C source examples, example X-windows R-4 drivers, a sample pixrect driver for Sun's low-level graphics library, and an S-bus evaluation board for use on Sun SparcStation platforms. Samples of the chip sell for $300 in 100-unit quantities and are available immediately.

***Fujitsu Microelectronics Inc.**, Advanced Products Div., 77 Rio Robles, San Jose, CA 95134-1807; Martin Booth, (408) 456-1160.* CIRCLE 304

■ *DAVE BURSKY*

ENHANCED CPU MODULE PUSHES RISC TO 40 MHz

The second-generation RISC CPU module from LSI Logic, the Ngine RPM3330, gives system designers a complete CPU, cache, and floating-point subsystem that can run at clock speeds of 33 or 40 MHz. At those speeds, the module delivers throughputs of 27 and 35 MIPS, respectively. The RPM3330 is also pin-compatible with the 20- or 25-MHz RPM3310 module released last year.

The 3330 incorporates the LR3000A CPU as well as the LR3230 enhanced read/write buffer chip, the LR3010A floating-point coprocessor, and dual caches, each comprising 64 kbytes of fast SRAM (double the size of caches in the RPM3310). Enhanced features of the LR3000A MIPS RISC processor include hardware cache invalidation control. That feature simplifies the implementation of multiprocessor systems and helps ensure cache integrity.

Using 3.5-in.^{2} modules can greatly simplify system design because they eliminate many of the complex timing concerns associated with implementing RISC-based systems. At 33 MHz, the subsystem dissipates about 25 W and requires an airflow of 150 linear ft./min. to keep the ambient to 50°C.

In addition to the 33- and 40-MHz modules, LSI will also sell the enhanced R/W buffer chip, the LR3230. That chip contains a nine-word write buffer, full-parity generation, multiprocessor support, and a reset-initialization controller. An optional byte-gathering feature is also included. Furthermore, the chip incorporates a Block-Match capability that lets it resolve read/write conflicts quickly. Block sizes can be programmed for 4 to 32 words.

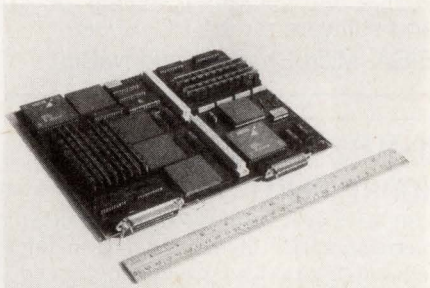
Prices for the 33- and 40-MHz versions of the RPM3330 in 100-unit lots are $2375 and $3165, respectively. For 1000-unit quantities, the cost drops to $1550 and $1975, respectively. Module samples will be available in the fourth quarter of this year. The LR3320 buffer chip comes in a 223-lead ceramic PGA package. In 1000-unit lots, the 33- and 40-MHz versions sell for $175 or $228, respectively. Samples of the chip are available immediately.

***LSI Logic Corp.**, 1551 McCarthy Blvd., Milpitas, CA 95035; Pamela Aratani, (408) 954-4655.* CIRCLE 305

■ *DAVE BURSKY*

ENHANCED SPARC CPU PACKS FPU, CUTS SPACE

Merging a floating-point math unit on the same chip as the Sparc integer unit lets the W8701 Sparc processor chip from Weitek replace two-chip combo (integer



plus floating-point) units. The W8701 chip implements version 7.0 of the Sparc architecture while maintaining software compatibility with other Sparc processors. Versions of the chip are available for clock speeds of 25, 33, and 40 MHz.

A 136-register, general-purpose register file allows the W8701 integer plus floating-point unit to implement eight sets of register windows plus eight nonwindowed global registers. Also on the chip are 32, 32-bit floating-point registers that can be paired to hold 16 double-precision numbers. The chip will be housed in a 207-pin PGA package. The 33- and 40-MHz versions of the chip sell for $240 and $264 each, respectively, in 5000-unit quantities.

And, to simplify Sparc-based graphics systems or any other system requiring high-performance 2D graphics, Weitek designed the W8720, a highly integrated graphics controller. The chip packs local buffer memory and video-control logic, as well as hardwired support for such functions as polygon fills, bit-block transfers, and logical raster operations. Speed can be improved about tenfold by using the W8720 instead of the dumb frame-buffer 2D color graphics typically implemented on other Sparc-based systems. The chip comes in a 208-lead quad-sided flat package and sells for $160 in 1000-unit lots.

***Weitek Corp.**, 1060 E. Arques Ave., Sunnyvale, CA 94086; (408) 738-8400.* CIRCLE 306

■ *DAVE BURSKY*

IEEE-488

Control any IEEE-488 (HP-IB, GP-IB) device with our cards, cables, and software for the PC/AT/386, EISA, MicroChannel, and NuBus.

using an optimized single-polysilicon single-metal CMOS EEPROM process that's simpler and more reliable than the processes used by other gate-array logic makers. Other benefits of the new process are a threefold improvement in electrostatic-discharge protection, increased data retention, and better switching-noise immunity. Available now, the GAL16V8S-20EB1 offers preload and power-on reset of all registers, a 100% final-programming yield, and data retention exceeding 20 years.

SGS-Thomson Microelectronics, I-20014 Agrate Brianza, Italy; (0039) 39-6555-597. CIRCLE 308

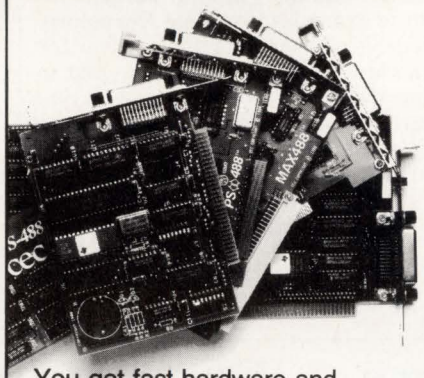
30-MHz Controller Boosts 8-Bit Systems

A 30-MHz version of the popular 80C51 microcontroller meets the increasing demand for greater processing speed in embedded-controller applications. Up to now, the maximum clock frequency for an 80C51 has been 24 MHz. Together with the 80C51's existing features—such as comprehensive bit handling, instruction set, two 16-bit timer-counters, and binary and BCD arithmetic—the 30-MHz clock frequency suits the PCB80C51BH-5-30 for a wide range of low-cost, high-performance embedded-control applications. The new microcontroller executes nearly 60% of its instructions in 0.4% μs, and 40% of them in 0.8 μs. Multiply and divide instructions execute in just 1.6 μs. At full speed, the device consumes 44 mA at 5.5 V. Power-down and idle modes reduce current consumption to 10.8 mA and 50 μA, respectively. Samples of the PCB80C51BH-5-30 are available now, and volume quantities can be delivered within 10 weeks. The device costs about $3.50 each in quantities of 10,000.

Philips Components, P.O. Box 218, NL-5600 MD Eindhoven, the Netherlands; (0031) 40-724324. CIRCLE 307

PLD Operates At Supply Currents Of Just 27 mA

The popular GAL16V8, an electrically erasable programmable-logic device that can emulate most types of 20-pin PLDs, is now available in a very-low-power version. It has a maximum supply current of only 27 mA that consumes only one-eighth the power of bipolar programmable-array-logic parts. The new GAL16V8S-20EB1 has a maximum propagation time of 20 ns. The low-power consumption is achieved by



You get fast hardware and software support for all the popular languages. A software library and time saving utilities are included that make instrument control easier than ever before. Ask about our no risk guarantee.

Fast Logic Sequencer Runs At 62 MHz

The fastest programmable-logic sequencer released by Philips-Signetics, the PLUS405-55, can be clocked at up to 62 MHz—about 20% faster than previously released sequencers from the company. A speed upgrade to the company's PLUS405 architecture, the 28-pin chip has 16 inputs and 8 J-K registered outputs. It accepts two external clock sources, and has two Complement Arrays so that If-Then-Else transitions can be implemented with one product term. The chip also has an asynchronous-register-initialization feature that allows each register to be individually programmed to generate a specific Preset-Reset pattern, allowing the chip to be asynchronously initialized to any known condition. The sequencer is supported by both the Snap tool package offered by the company and a simpler software package, Slice, that does entry-level implementation. In 1000-unit lots, the plastic DIP version of the chip sells for $17.65.

Philips Components, Signetics Company, 811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088-3409; Kate Douglas, (408) 991-5078. CIRCLE 309

EISA Chip Set Trims IC Count/Space

A second-generation chip set for extended-industry-standard-architecture-(EISA)-based motherboards, the 82350DT is a superset of Intel's 82350 chip set released in 1990. The new set lets system designers assemble an EISA system with 43 devices—less than half the number needed for the first chip set—on an 8.5-by-12-in. board. This reduced chip count and thus cost, coupled with the simultaneous release of the reduced-cost 80486SX CPU, will let system designers implement low-cost EISA-based systems. The chip set's modular architecture enables the same platform to be used for 386DX, 486DX, or 486SX CPUs. The 82350DT consists of three of the original chips—the integrated system peripheral, the EISA bus controller, and the EISA bus buffer—plus a DRAM controller, an advanced data-path circuit, and a local I/O controller. In 1000-unit lots, the chip set sells for $200.

Intel Corp., 3065 Bowers Ave., Santa Clara, CA 95052-8131; (408) 765-8080. CIRCLE 310

Free:
Informative catalog 800-234-4232
Applications help (617) 273-1818

cec

Capital Equipment Corp.
Burlington, MA. 01803

CIRCLE 87

The FS700 LORAN-C frequency standard

10 MHz cesium stability

$4950

Cesium long term stability at a fraction of the cost

Better long-term stability than rubidium

Not dependent on ionosphere position changes, unlike WWV

Complete northern hemisphere coverage, unlike GPS.

The FS700 LORAN-C frequency standard provides the optimum, cost-effective solution for frequency management and calibration applications. Four 10 MHz outputs from built-in distribution amplifiers provide cesium standard long-term stability of 10^{-12}, with short-term stability of 10^{-10} (10^{-11} optional). Reception is guaranteed in North America, Europe and Asia.

Since the FS700 receives the ground wave from the LORAN transmitter, reception is unaffected by atmospheric changes, with no possibility of missing cycles, a common occurrence with WWV due to discontinuous changes in the position of the ionosphere layer. Cesium and rubidium standards, in addition to being expensive initially, require periodic refurbishment, another costly item.

The FS700 system includes a remote active 8-foot whip antenna, capable of driving up to 1000 feet of cable. The receiver contains six adjustable notch filters and a frequency output which may be set from 0.01 Hz to 10 MHz in a 1-2-5 sequence. A Phase detector is used to measure the phase shift between this output and another front panel input, allowing quick calibration of other timebases. An analog output with a range of ±360 degrees, provides a voltage proportional to this phase difference for driving strip chart recorders, thus permitting continuous monitoring of long-term frequency stability or phase locking of other sources.

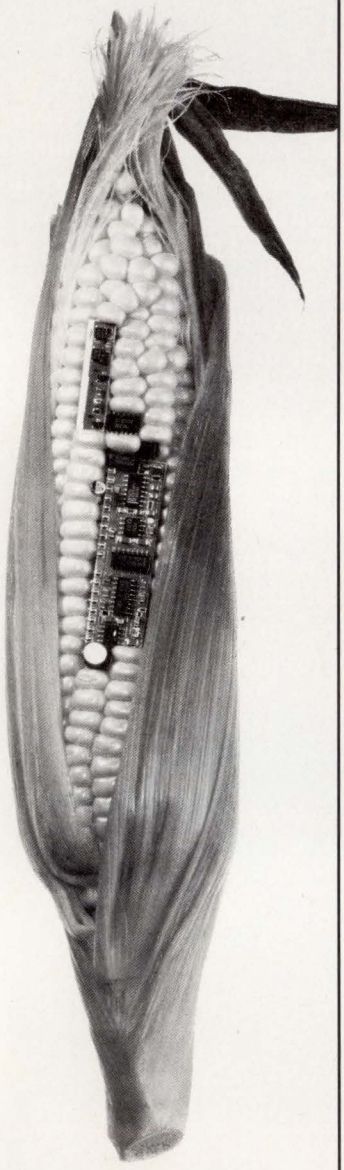
FS700: The optimum frequency management system

STANFORD RESEARCH SYSTEMS

1290 D Reamwood Avenue ▪ Sunnyvale, CA 94089 ▪ Telephone: (408) 744-9040
FAX: 4087449049 ▪ Telex: 706891 SRS UD

CIRCLE 136

Hybrids you can bet the farm on.



Send us your design parameters and in 6 weeks tops we'll get you a hybrid prototype up to 10 times smaller than conventional circuits, yet able to meet your biggest performance and reliability demands. Call 1-800-622-5574. In today's hybrid field, we're the pick of the bunch!

10575 SW Cascade Blvd. Portland, OR 97223
(503) 684-5657 FAX (503) 620-8051

PACIFIC HYBRID MICROELECTRONICS

We do small miracles.™

Copyright © 1990 Pacific Hybrid Microelectronics

CIRCLE 83

STANDARD-CELL FAMILY INCLUDES V-SERIES CPU

Although standard-cell vendors are plentiful, the CB-C7 standard-cell family from NEC is the only one, aside from Intel, offering 8088- and 8086-compatible CPU cores (the V20H and V30H, respectively). Employing a 0.8-μm (drawn) CMOS fabrication process, the cells can be combined to deliver chips with complexities of up to 180,000 gates and as many as 350 I/O lines.

Typical gates have propagation delays of 340 ps and dissipate just 8 μW/gate/MHz. Two implementation options will be available with CB-C7. The first offers the shortest turnaround time (about 6 weeks), and places the standard cells on a sea-of-gates array. Although not as dense as a full-custom chip, only metal-mask-related layers need be fabricated to complete the design. If customers can wait two weeks longer, a fully customized and smaller chip can be created.

The CB-C7 cell library is compatible with the company's previously released CMOS-7 library, and thus provides a direct migration path for existing designs. Many popular standard "mega" functions are included in the library—the 8088- and 8086-compatible CPUs, a programmable DMA controller, USART, interval timer, system bus controller, and a 765-type floppy-disk controller. Also available are compilers to generate custom-sized blocks of RAM and ROM.

Supporting the chip designer is NEC's OpenCAD Design System, which offers a complete front-to-back unified design environment based on popular commercial design tools, as well as a few proprietary tools. Initial prices for the chips will range from 0.06 to 0.1 cents/usable gate, depending on complexity, package, and quantity. The libraries are available immediately and designs will be accepted for production in the third quarter of this year.

***NEC Electronics Inc.**, 401 Ellis St., Mountain View, CA 94039; Al Chiang, (415) 965-6539.* CIRCLE 311

■ *DAVE BURSKY*

CROSSPOINT SWITCH MOVES NRZ DATA FAST

Letting data flow through it at 1.2 Gbits/s for non-return-to-zero-coded signals, a 32-by-32 crosspoint switch can also be used in groups of four without any additional support components to implement 64-by-64 crosspoint switches. The S2024 Crossbow switch, developed by Applied MicroCircuits, also offers full broadcast capability. This capability permits any of its 32 input lines to be connected independently to any or all of its 32 output lines.

Even though the chip is implemented internally with 10K-family ECL circuits, all addressing inputs and control lines are TTL-compatible to simplify the interfacing to microprocessors. A complete reconfiguration of the dataflow paths requires only 4 ns, and the reconfiguring does not disturb existing switch operations.

The chip has transparent and synchronous operating modes, providing maximum flexibility across a wide range of applications. The transparent mode allows the full-speed, 1.2-Gbit/s throughput, while the synchronous mode drops the data rate to half that figure—to 600 Mbits/s.

The high data rates suit the chip well for handling many diverse applications: digital video, digital demultiplexing, microwave or fiber-optic data distribution, data communications and telecommunications switching, and high-speed automatic test equipment.

The 9-W power consumption of the S2024 switch may seem high, but that dissipation figure is still only about half the power of the best alternative solutions. Finally, clock inputs for the chip can be set as single-ended or differential.

Housed in either a 251-lead pin-grid array package or a 196-lead chip carrier, the S2024 employs most of the unused leads for power and ground connections. Both military and commercial versions of the chips are available. In 1000-unit lots, the 196-lead chip-carrier version sells for $389 each.

***Applied MicroCircuits Corp.**, 6195 Lusk Blvd., San Diego, CA 92121; Mike Orenich, (619) 450-9333.*

CIRCLE 312

■ *DAVE BURSKY*

CHIP SET POWERS V.32 MODEMS IN LAPTOPS AND PORTABLES

Modem and personal-computer designers can now tuck a V.32 modem into their designs by using a three-chip, surface-mountable data pump that typically consumes just 450 mW while operating and 50 mW in the sleep mode. The DSP16A-V32 chip set from AT&T Microelectronics consists of the company's 16-bit fixed-point DSP16A digital-signal processor, the T7525 linear codec, and an interface controller. V.32 is a 2- or 4-wire full-duplex telecommunication standard for public-switched or private networks.

Housed in a 28-pin SOJ package, the T7525 linear codec on the telephone-line side of the data pump serves as the analog front end and has 12-bit linearity that provides over 60 dB of echo cancellation from a digital echo canceler. The ROM-coded DSP16A performs signal-processing and control functions required to implement V.32 performance specifications. Interfaces to a V.24 port, multiplexed and nonmultiplexed microprocessor buses, and an eye-pattern interface outlet, are supplied by the data-pump controller. That controller is packaged in a 68-pin plastic leaded chip carrier.

In addition to V.32, the data-pump chip set supports V.22bis, V.22, V.23, Bell 212A, and Bell 103 modem standards. As a result, modems made with the chip set will be compatible with 9600-, 4800-, 2400-, 1200-, 600-, and 300-bit/s modems. With data compression (V.42bis/V.42 standard), a 38,400-bit/s data rate is possible. For communication with facsimile machines, AT&T will add V.29, V.27ter, and V.21 CH2 standards to the chip set later this year. The DSP16A-V32 chip set is available now for a price of $70 each in quantities of 10,000.

AT&T Microelectronics, *Dept. 52AL300240, 555 Union Blvd., Allentown, PA 18103; (800) 372-2447.* **CIRCLE 313**

■ *MILT LEONARD*

CHIP SET IMPLEMENTS TAPELESS TELEPHONE-ANSWERING MACHINES

In addition to performing all of the functions for featurephones and cordless telephones, the D6005 chip set from DSP Group stores telephone messages on solid-state memory. This approach breaks away from conventional telephone answering devices (TADs) that use audio tape to store messages.

The chip set consists of the D6005-11 digital-signal processor that executes speech compression, storage, and other TAD and telephone functions, and the D6005-71 ASIC to handle the memory and host interface. It als consists of the D0000-26 codec for analog-to-digital and digital-to-analog signal conversions, and from 1 to 16 audio-grade RAMs (ARAMs) for message storage.

The D6005 chip set has the capability to address up to 16 Mbits of memory, which is equivalent to 26 minutes of storage time or 50 30-second messages. Other features include instantaneous message retrieval, playback, and repeat; message skip and offset; selective erasure; date and time stamping; and voice-activated recording.

Like cassette-based TADs, products designed with the D6005 chip set can also have such features as a secret mailbox, private incoming messages, message-transfer capability, multiple outgoing messages, and voice instruction.

To support featurephones and cordless telephones, the D6005 chip set offers dual-tone multifrequency (DTMF) receive and transmit capability, permitting remote activation of all TAD functions from a cordless telephone. Remote TAD operation is also supported by the D6005 chip set's near-end echo-cancellation capability.

The digital-signal processor, ASIC, and codec circuits have a total maximum power dissipation of 1.09 W. The D6005 chip set, with a complement of four ARAMs (7 minutes of recording time), is available now for under $30 each in volume.

DSP Group, Inc., *4050 Moorpark Ave., San Jose CA 95117, (408) 985-0722.* **CIRCLE 314**

■ *MILT LEONARD*

PICO
DC-DC CONVERTERS
Wide Input Range
5 to 72V DC

Regulated
5 Watt to 30 Watt

- 386 Standard Models
- Single, Dual and Triple Output
- Output Voltages of 5, 9, 12, 15, 24, 28 and 48 Volts DC Standard
- Ambient Temperature Range −25°C to +70°C with No Heat Sink or Electrical Derating
- All Units Shielded
- 500V DC Isolation Input to Output
- New PLR Series Features .300" ht.
- New NR Series, up to 30 Watts-50 Models-30 Triple Outputs

OPTIONS AVAILABLE
- Expanded operating temp (−55°C to +85°C)
- Stabilization Bake (125°C ambient)
- Temperature Cycle (−55°C to +125°C)
- Hi Temp, full power burn in (100% power, 125°C case temp)

Delivery—stock to one week

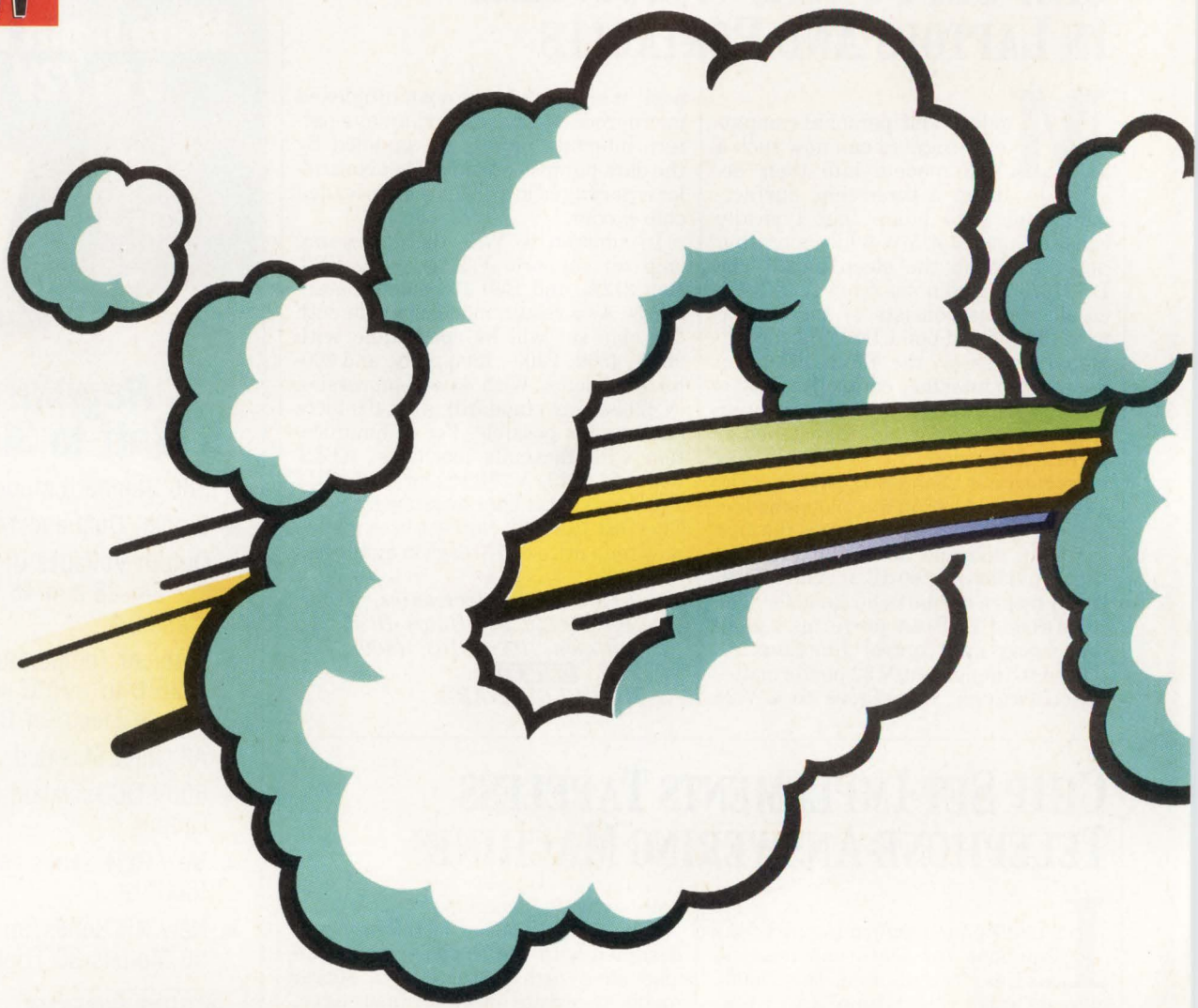
SEE EEM, THOMAS REGISTER OR SEND DIRECT FOR FREE PICO CATALOG

PICO Electronics, Inc.
453 N. MacQuesten Pkwy. Mt. Vernon, N.Y. 10552
Call Toll Free 800-431-1064
IN NEW YORK CALL 914-699-5514

PICO also manufactures over 800 standard DC-DC Converters, AC-DC Power Supplies and over 2500 Miniature Transformers and Inductors

CIRCLE 81

SAMSUNG NOW



(ACTUAL SCHEMATIC OF OUR NEW

At 10 nanoseconds, the new BiCMOS 64K SRAMs from Samsung are the fastest made.

So fast you might think you couldn't even see them.

But see them you can. As one of the world's true manufacturing giants, we can assure you of extremely reliable, high-quality chips—*now*.

Adding to our current line of ultra-fast 8Kx8 and 16Kx4 SRAMs, we'll soon introduce an innovative BiCMOS 256K family—also tremendously fast, and featuring address latches for still-higher performance.

The Samsung BiCMOS parts will soon be joined by fast SRAMs in the 1-meg density. All

THE SAMSUNG BiCMOS SRAMs

Part Number	*Org.*	*Packages*	*Speed*
KM68B65	8Kx8	SOJ, DIP	10,12,15,20 ns
KM64B65,66,67*	16Kx4	SOJ, DIP	10,12,15,20 ns

10-NANOSECOND 64K SRAM.)

of which will join our remarkable *existing* line of SRAMs. These currently produced parts include fast SRAMs up to 256K, and slow SRAMs up to 1 meg.

What all these things tell you is that, at Samsung, we're continuing to build on a genuine commitment to the SRAM market. And that's extremely significant for your access to supply.

For data sheets on the fastest 64K BiCMOS SRAMs made, call 1-800-423-7364 or 408-954-7229 today. Or write to SRAM Marketing, Samsung Semiconductor, 3725 No. First St., San Jose, CA 95134.

We'll send you the *real* block diagram.

SAMSUNG Semiconductor

** 16Kx4 available Q2.* *© Samsung Semiconductor, Inc., 1991.*

CIRCLE 138

ADC With 574 Footprint Samples And Converts Signal In 10 μS

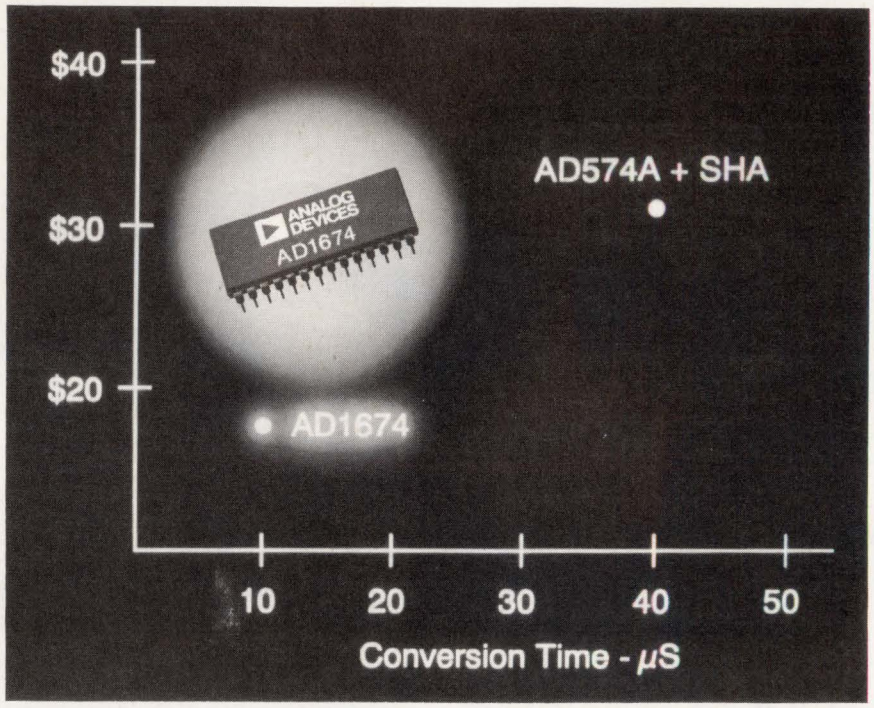
FRANK GOODENOUGH

The standard 574 analog-to-digital converter, originated by Analog Devices a dozen years ago, is now available in various forms with many specifications from, at last count, nine suppliers. The original device required two chips and for years was only available in ceramic packages. With their latest version—the AD1674—Analog Devices is now topping all known 574-type ADCs in both price and performance.

At $18 each in hundreds, the ADC goes for 80% of a basic AD574A and 70% of an AD674A. However, conversion times of the AD574A and AD674A run a minimum of 35 and 15 μs, respectively. The AD1674 does it in 10 μs—a conversion rate of 100 kHz. And, unlike previous versions, a user-transparent, true sample-and-hold amplifier (SHA) sits on the ADC's front end. The ADC's conversion rate is the SHA's sampling rate. The SHA's 1-MHz bandwidth ensures 12-bit operation to Nyquist frequencies. Its unique circuit was the subject of a technical presentation at this year's International Solid State Circuits Conference (ELECTRONIC DESIGN, *Feb. 14, p. 68).*

Like most sampling ADCs, dynamic (ac) specifications are provided, and guaranteed at that. Not only does the AD1674 maintain the 574's footprint, but works with all current 574 software operating in the standalone mode. While operating in the full-control mode, minor timing changes are needed.

All 574 family converters are general-purpose ADCs designed to run off ±15-V or ±12-V rails plus a 5-V digital line. Other family traits include user selection of one of four input-voltage ranges (±5, ±10, 0-10, and 0-20 V) by pin-strapping, and a parallel three-state digital output, which is software-programmable to provide any mix of three 4-bit nibbles. As a result, it adapts easily to a wide range of signals and to 4-, 8- or 16-bit microprocessor buses.



Devices for all three standard-temperature ranges are available with an integral nonlinearity (INL) over temperature of ±1 LSB maximum. Prime grades for the commercial and extended-industrial range offer ±1/2-LSB INL maximum. All five grades guarantee no-missing-code operation to 12 bits over temperature.

The lower-grade commercial AD1674J, over temperature and in a 28-pin plastic double-width DIP, offers a sampling rate of 100 kHz minimum, a 10-kHz minimum input signal, maximum offset drift of ±2 LSBs, maximum full-scale error of ±6 LSBs, and maximum signal-to-(noise + distortion) (s/n + d) ratio of 69 dB (11.2 bits). Total harmonic distortion (THD) is –82 dB (13.3 bits) maximum, peak harmonic component is –82 dB (13.3 bits) maximum, and intermodulation distortion (IMD) is –80 dB maximum (with 9.08- and 9.58-kHz inputs). Power dissipation is 575 mW maximum.

If a SHA is needed ahead of a 12-bit ADC, such as the 3-μs AD7672, the AD1674's SHA—the AD781—is available in an 8-pin miniDIP. The hold capacitor is on-chip. Its acquisition time is just 700 ns maximum to 0.01%, and aperture jitter is just 75 ps maximum.

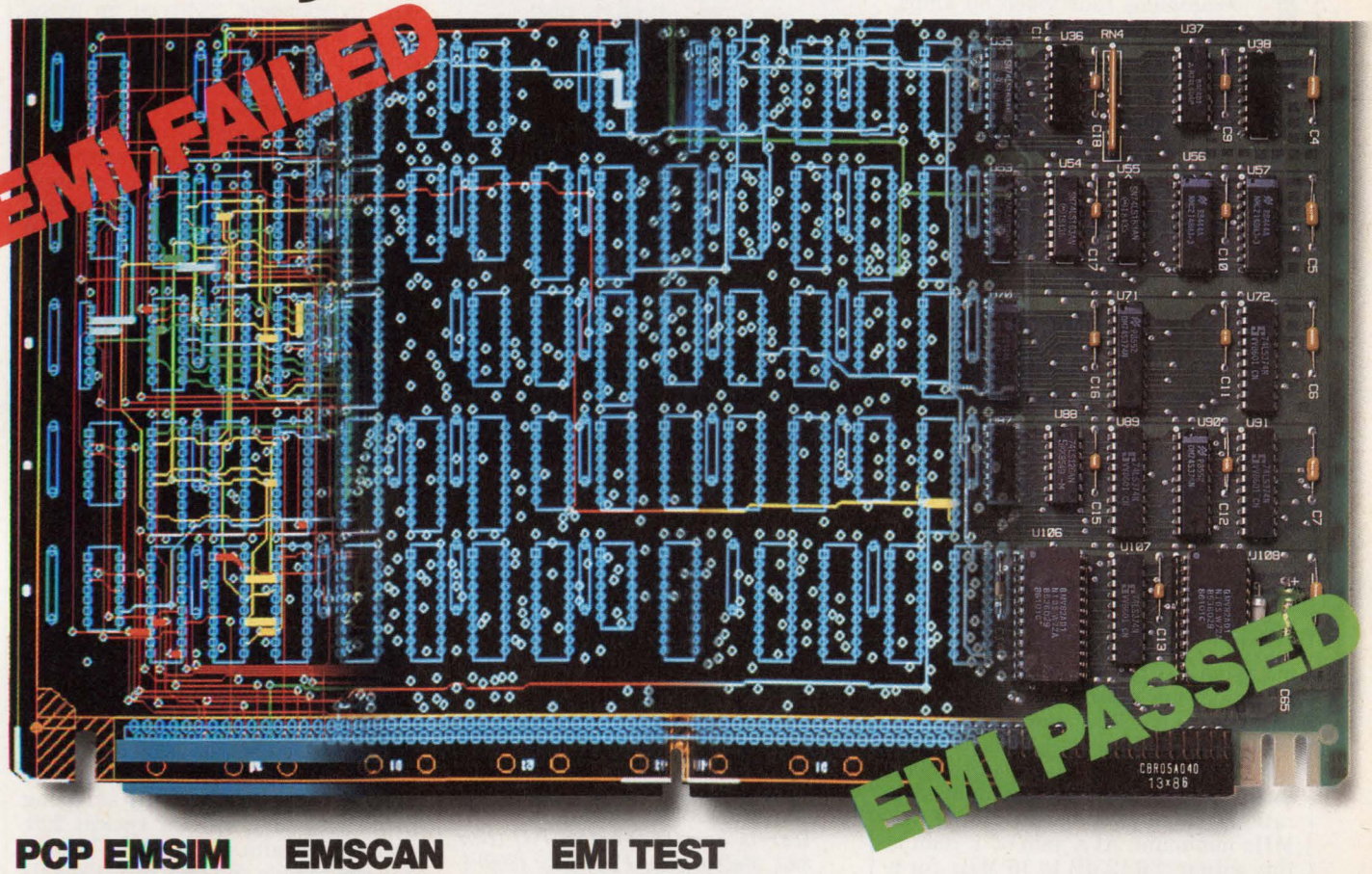
Unlike most SHAs, dynamic specifications are provided. While sampling at 500 kHz and with a 10-kHz input, THD runs –80 dB maximum, and s/(n + d) ratio runs –72 dB. Typical THD (while sampling 10-, 50- and 100-kHz inputs) runs –90, –73, and –68 dB, respectively. Sampling similar signals, typical s/(n + d) runs 78, 73, and 67 dB, respectively. IMD usually runs –77 dB.

Pricing for the AD1674, in hundreds, ranges from $18 to $70 each. In similar quantities, the commercial-grade AD781 can be had for $6 each, the extended-industrial grade for $7.40 each, and the mil-grade SHA for $20 each. Small quantities of each are available from stock.

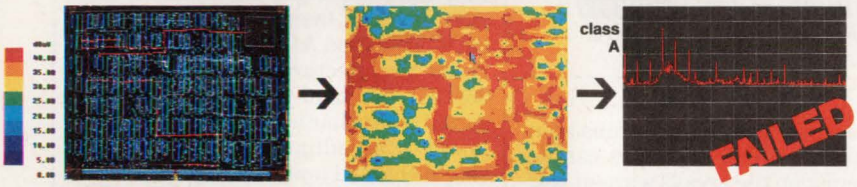
Analog Devices Inc., 181 Ballardvale St., Wilmington, MA 01887; Applications Engineering, (617) 937-1428 **CIRCLE 315**

Minimize EMI During PCB layout before you build it!

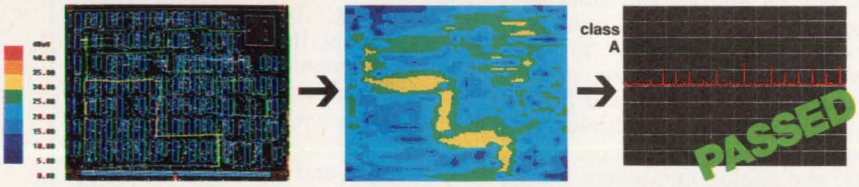
Get your product to market fast and save time and money in the process! Now you can optimize your circuit boards early in the design cycle before hardware prototyping with a simulation tool developed by Bell-Northern Research for Northern Telecom. As a complement to the circuit board design system CBDS, PCP EMSIM allows designers to select, position and route components for minimum EMI emissions, decreasing the risk of failing government regulations, such as FCC, CISPR and VCCI.



PCP EMSIM **EMSCAN** **EMI TEST**



Hot traces (shown in red) identified early at the layout stage with PCP EMSIM indicate that this board design will likely fail EMI radiated emission tests. As shown here, subsequent board testing on the EMSCAN hardware scanner and open field tests confirm the PCP EMSIM results.



Optimizing component selection, placement, and routing using PCP EMSIM enables you to reduce EMI before costly hardware prototyping. Scanning the revised prototype board on EMSCAN confirms the reduction in EMI, which is again verified by open field tests.

Marubeni
INTERNATIONAL ELECTRONICS CORPORATION

For complete technical details, call or fax us today.

20 William Street
Wellesley, MA 02181
Tel. (617) 237-2115
Fax (617) 237-1046

Come and see PCP EMSIM & EMSCAN at **Booth 1361**

DESIGN AUTOMATION 28th CONFERENCE

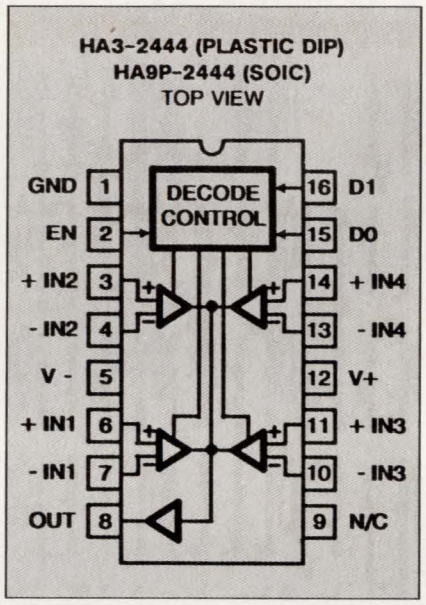
PCP EMSIM, EMSCAN and CBDS are trademarks of Northern Telecom Limited.

CIRCLE 179

16-Pin IC Looks Like 4 Video Op Amps Feeding A Multiplexer

Cramming four video op amps, each with its own functional pair of differential inputs, a multiplexer to connect one of them to an output, two address inputs for the multiplexer, plus an enable/disable input, may seem topologically impossible. Not for the Harris HA-2444. As a black box, this device looks like four op amps connected to a four-input analog multiplexer, offering a high-impedance state in which none of the op amps are connected to the output. Unlike similar devices that are limited strictly to multiplexing, each op amp can be given its own unique feedback circuitry to control gain, bandwidth, or function *(see the figure)*. For example, one op amp can sum (linearly mix) several signals, a second can perform integration, while the third and fourth act as a comparator and buffer. The high-impedance output state permits multiple HA-2444s to be wire-ORed (connected in parallel) when more than four signals must be conditioned and multiplexed.

Small-signal (±100-mV) unity-gain bandwidth is typically 45 MHz. Open-loop gain at dc typically runs 76 dB. Operating from ±15-V rails, the output can put ±11 V across 1 kΩ and ±2 V across a more typical 75-Ω video load. Reflecting a 120-V/μs minimum slew rate is full-power bandwidth of 3.8 MHz minimum. At a gain of 1, gain is flat within ±0.12 dB to 10 MHz for a 200-mV rms input. Typical differential-gain and phase run 0.03% and 0.03°, respectively. Chrominance gain and luminance delay run 0.1 dB and 7 ns, respectively. An enabled HA-2444 switches from one channel to another in a maximum of 100 ns. The application of an enable pulse connects a selected channel to the output in a similar time. Applications range from simple video-channel selection to use as a programmable-gain amplifier with four selectable gains for one signal.



***Harris Semiconductor**, P.O. Box 883, Melbourne, FL 32901; (800)-4-HARRIS, ext. 1221.* CIRCLE 316

■ *FRANK GOODENOUGH*

High-Speed Analog Arrays Get Macros

If a relatively small, high-speed, semi-custom analog IC at low cost is needed, a dielectrically isolated Sipex SP2000 tile array may be the way to go. The company is now announcing a library of over 25 macros and two new tiles, creating a family of three: the SP2101/04/07 with 4, 12, and 20 tiles, and 26, 46, and 54 bonding pads, respectively. Each tile holds 16 vertical npn and 16 vertical pnp small-signal transistors with f_ts of 1000 and 600 MHz, respectively. Each array also contains additional (larger), vertical npns and pnps (currents to 100 mA), as well as thin-film resistors, capacitors, and conventional and Zener diodes. Each transistor is isolated in its own silicon-dioxide tub, and good vertical pnp transistors are available; thus, designers can design circuits on the arrays without worrying about dc and ac parasitics or working with only npn transistors. Macros, which take from one to two tiles, include general-purpose, precision, wide-band (300-MHz), and high-gain (125-dB) op amps; multiplexing amplifiers; sampling amplifiers; comparators; and analog multipliers. Also included are references, charge pumps, and even logic gates. By year's end, most macros will be available as kit parts for breadboarding. Typical NRE cost runs under $19,000 and includes prototypes in about 8 weeks after completion of design and layout.

Sipex Corp., 22 Linnell Circle, Billerica, MA 01821; Tim Maniwa, (408) 942-4484. CIRCLE 317

DIP Holds 4 Op Amps Plus A Reference

The TDC4614 is designed to create up to four precision low-impedance voltage sources. This 16-pin DIP contains four, independent 324-type op amps plus an adjustable output (1.2 to 6.3 V) bandgap reference. Its cohort, the TDC4611, contains just one op amp and a reference in an 8- or 14-pin DIP. Many flash ADCs offer improved linearity if one or more taps on their resistive divider are each driven by a precision voltage, a natural application for the TDC4614. Many additional flash and other types of ADCs require a positive and a negative reference. Alternatively, the IC can provide any mix of four different positive or negative reference voltages for any mix of DACs or ADCs. Available in commercial and military grades, pricing starts at $1.20 each for the commercial TDC4611 and $1.75 each for the TDC4614, both in quantities of 100.

TRW LSI Products Inc., P.O. Box 2472, La Jolla, CA 92038; Dan Watson (619) 457-1000. CIRCLE 318

8-Bit ADCs Sample 300-kHz Sinewaves

Designed to replace their original 10-year-old, industry-standard ADC0820, National Semiconductor's new families of 8-bit ADCs and data-acquisition systems convert in 500 ns. Of more importance, because they're truly sampling converters, they offer a typical full-power bandwidth of 300 kHz. That is, they can sample and digitize a 300-kHz sine wave. At their heart lies a patented, 8-bit/500-ns ADC employing a multistep architecture. The ADC08061/062/064/068 family offers 1, 2, 4, and 8 signal input channels, respectively, followed by a multiplexer (except for the single-channel unit), a sample-and-hold amplifier, and an ADC. The ADC08161/162/164/168 are identical devices, except that all have a 2.5-V bandgap reference. Four grades provide total unadjusted errors of ±1 and ±1/2 LSB for both industrial and military use. Packaging includes: 20-pin PLCCs, DIPs, and wide-body SOICs for 1- and 2-channel devices; 24-pin DIPs and wide-body SOICs for the 4-channel device; and 28-pin PLCCs, DIPs, and wide-body SOICs for the 8-channel units. In quantities of 100, the ADC starts at $9.90 each.

National Semiconductor Corp., P.O. Box 58090 Santa Clara, CA 95052-8090; Kay Hoang, (408) 721-2302. CIRCLE 319

Our 3-and-3 Process Could Write The Declaration Of Independence On A Matchbook.

If you're having problems fitting eloquent concepts into small packages, come to Praegitzer Industries. We are one of the few manufacturers offering production levels of 3-and-3 and 5-and-5 printed circuit boards. Our fine-line processes mean smaller interconnects.

Fewer layers. Denser boards. Better products. And fine lines are just part of our design, fabrication, and assembly services. *To get you started, we will even rebate your prototype, NRE and tooling costs!* Call **1-800-875-2522** to learn more.

Praegitzer Industries

The Fine Line in Printed Circuits

1270 Monmouth Cut-Off, Dallas, Oregon 97338-9532

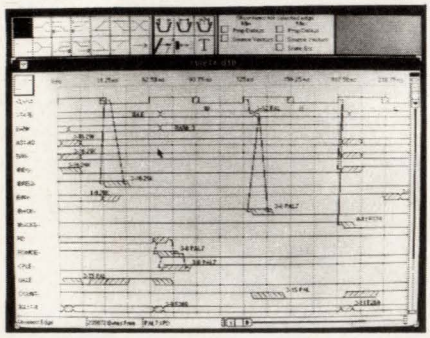
CIRCLE 133 FOR LITERATURE

CIRCLE 135 FOR BROCHURE

TIMING-DIAGRAM SOFTWARE ADDS TEST-VECTOR GENERATION

The Test Vector Generator is the newest enhancement to the dV/dt Timing Diagram Accelerator, a pre-schematic-capture tool that lets designers create timing diagrams. With Test Vector Generator, designers can convert dV/dt waveforms to various programmable-logic-device (PLD) test-vector formats, and can covert test vectors into dV/dt waveforms.

Currently, the Test Vector Generator will translate into the following PLD formats: Data I/O's Abel, Capilano Computing Systems' MacAbel, Logical Devices' CUPL, Accel Technologies' TangoPLD, Orcad's Orcad/PLD, AMD's Palasm, and Omation's Schema PLD. Other PLD formats will be added.



Users create test vectors by first establishing dV/dt standard-format test-vector files. Using the conversion utility, they then convert the standard vectors to the PLD format of choice. Also, dV/dt Timing Diagram Accelerator can import dV/dt standard-format test-vector files to create waveforms on the screen. Users can customize test-vector format outputs with the necessary file specifications in the Test Vector Generator manual.

The dV/dt Test Vector Generator runs on PCs and Macintosh computers. It's shipping now for $495, or for $995 when bundled with the Timing Diagram Accelerator.

***Doctor Design Inc.**, 5415 Oberlin Dr., San Diego, CA 92121; (619) 457-4545.* CIRCLE 320

■ *LISA MALINIAK*

PCB SCREENING TOOL CHECKS FOR SIGNAL INTEGRITY

Version 2.0 of the BoardScan pc-board screener from Quantic Laboratories now calculates signal-integrity parameters. BoardScan is a circuit-simulation tool that screens pc boards and determines critical nets where crosstalk and signal-integrity problems are likely to occur. The signal-integrity calculations uncover complications due to such factors as time delays, overshoots, undershoots, settling time, noise margins, and functional violations.

BoardScan features an interactive database facility that lets users add, delete, substitute, and browse through the component library within the user interface. The component library includes over 4000 components covering a range of logic technologies, such as Fast and HCT.

Crosstalk between nets is calculated with a high-order boundary-element field solution. Routed nets are coupled automatically, and the crosstalk values are detailed in a net report. Users input circuits to the screener through an interface file that's already integrated with tools from such companies as Mentor Graphics, Racal-Redac, and Valid Logic Systems.

Once BoardScan identifies the critical nets, they can be further analyzed by the company's Greenfield Version 3.0 system-level simulator. Greenfield can simulate circuits with multiconductor, coupled, transmission lines. It includes a schematic and graphics editor for interconnection and editing of system components.

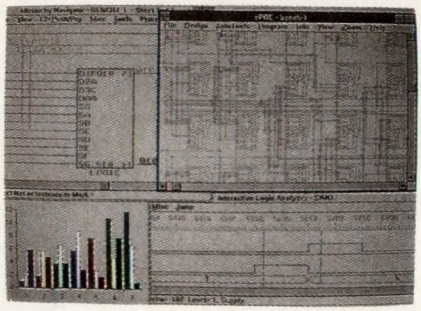
Both BoardScan Version 2.0 and Greenfield Version 3.0 run on a variety of Unix platforms. Pricing for BoardScan and Greenfield starts at $17,000 and $24,500, respectively.

***Quantic Laboratories Inc.**, Suite 200, 281 McDermot Ave., Winnipeg, Manitoba, Canada R3B 0S9; (204) 943-2552.* CIRCLE 321

■ *LISA MALINIAK*

Correction: On page 109 of our March 14 issue, the phone number of Lewis Systems Inc., Irving, Texas was incorrectly listed. The number should have read (214) 438-2177.

FPGA DESIGN SOFTWARE RUNS UNDER WINDOWS 3.0



The pASIC Toolkit 3.0 is a set of tools for designing, simulating, programming, and testing QuickLogic field-programmable gate arrays on a PC. It combines the Engineering Capture System from the CAD/CAM Group and the X-Sim simulator from Silicon Automation Systems with the pASIC architecture-optimized tools from QuickLogic. All of the software runs under Microsoft Windows 3.0. The toolkit contains all of the software and hardware needed to build custom designs with QuickLogic's devices, except for the personal computer. A notebook-sized Designer Programmer performs both device programming and functional testing with ATVG and user-generated vectors. Cables, connectors, and an antistatic wrist strap are also included. The pASIC Toolkit 3.0 is shipping now for $3995.

QuickLogic Corp., 2933 Bunker Hill Ln., Santa Clara, CA 95054; (408) 987-2000. CIRCLE 322

IMPROVED SOFTWARE EASES BOARD DESIGN

The newest release of the Auto-Board System features enhancements that ease the task of board design. Schematic capture was improved with pull-down menus for invoking edit commands and inserting symbols. In addition, a reorganized symbol library has multiple-section parts that can be inserted as a unit and then moved individually. The layout and routing module now has forward annotation for recognizing new parts added to the schematic or net list, and a viewport that lists parts for selection during placement. Auto-Board System was restructured so that placement and routing tools can be added incrementally. It runs on PCs and Macintosh computers, and costs between $295 and $3200.

The Great SoftWestern Co. Inc., 919 S. Carroll Blvd., Suite 103, Denton, TX 76201; (817) 383-4434. CIRCLE 323

UPGRADE KIT BOOSTS MODELER'S PERFORMANCE

Users can push the speed of their Logic Modeling LM-1000 hardware modelers with an upgrade kit from the company. The upgrade improves the speed of the LM-1000 by up to a factor of six, enabling a large number of designers to run more complex simulations and faster fault simulations. The kit consists of a 68040-based CPU board and software. An improved network server helps boost overall performance, and a larger CPU memory increases fault-simulation capacity by as much as a factor of ten. In addition, the new software includes enhanced hardware-modeling algorithms. LM-1000 users can install the upgrade in the field. With the upgrade, the LM-1000 becomes identical to the company's new LM-1200 modeler. The upgrade kit will be available in June for $19,000.

Logic Modeling Systems Inc., 1520 McCandless Dr., Milpitas, CA 95035; (408) 957-5200. CIRCLE 324

PSPICE ADDS FEATURES FOR BETTER ANALYSIS

The improved 4.05 version of PSpice now offers more features, including Sun network licensing and pulse-width-modulator models. Parts sessions can be frozen and rerun at a later time. In addition, the number of states for digital simulation has increased from 28 to 246,528. This is due to the increase in the number of input levels from three to five, and an increase in the number of output strengths from 4 to 64. Optional power-supply pins were added to all of the parts in the digital library, giving users the ability to have more than one power supply in the circuit. The PSpice software runs on personal computers, Macintosh computers, and several Unix workstations. Pricing ranges from $950 to $5400, depending on the platform. Such options as digital simulation are sold separately.

MicroSim Corp., 20 Fairbanks, Irvine, CA 92718; (800) 245-3022 or (714) 770-3022. CIRCLE 325

ALTERA PLD SOFTWARE RUNS ON SUN COMPUTERS

Users of Altera's erasable, programmable-logic devices (EPLDs) can now do their designs on a Sun workstation. The PLS-SN software is a set of EPLD design tools for the Sun Sparcstation and Sun 3 computers. In addition, Altera has an agreement with Valid Logic Systems to provide an EDIF-based interface between the Altera tools and Valid's digital design environment. PLS-SN contains the Altera programmable logic-synthesis technology and a bidirectional EDIF 2 0 0 interface. Users can input a design with a variety of workstation-based schematic-entry tools. Also, they can use the Altera HDL to input a design behaviorally employing any workstation text editor. System-level verification is performed with an EDIF net list that has post-synthesis routing and delay information. This file can be read by any standard EDIF net-list reader. PLS-SN includes the Max+Plus compiler, EDIF net-list reader and writer, and simulation libraries for Valid Logic Systems and Viewlogic Systems. It's shipping now for $9995.

Altera Corp., 2610 Orchard Pkwy., San Jose, CA 95134-2020; (408) 984-2800. CIRCLE 327

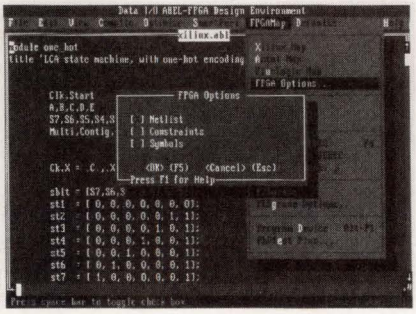
ABEL DESIGN SOFTWARE OFFERS COMPLETE FPGA SOLUTION

Designers working with field-programmable gate arrays (FPGAs) can use ABEL-FPGA design software from project start to finish. The software, which is based on the ABEL design software, offers design entry, optimization, device fitting, and logic synthesis for all current FPGAs.

FPGA-specific capabilities include a DOS extended parser for handling the arrays' larger logic modules. Also, extended ABEL-HDL features generate place-and-route constraints for FPGA architectures. Optimization features include criteria for net-list generation based on specific FPGA architectures. New menu features support the FPGA design flow.

ABEL-FPGA is built around device fitters, which are optimization programs that manipulate logic descriptions to best use specific device characteristics. In addition to the traditional pin and node assignments, macrocell configuration, and control-term configurations done by all fitters, the ABEL-FPGA device fitters automatically perform logic transformation, logic partitioning, and signal placement and routing tasks.

Behavioral entry can take the form of state machines, high-level equations, or truth tables. The software's output includes vendor-specific net lists and vendor-specific constraint files. As a result, the same design can be migrated between multiple FPGA vendors. In addition, ABEL-FPGA automatically creates schematic symbols that can be used with schematic-capture tools to integrate the ABEL-designed behavioral models into the rest of the system design.



ABEL-FPGA costs $7995 for the IBM/XT and /AT, Compac 386, IBM PS/2 Models 70 and 80, and compatibles. Site licensing and box-of-5 and box-of-10 quantities are available. Delivery is in 2 to 4 weeks.

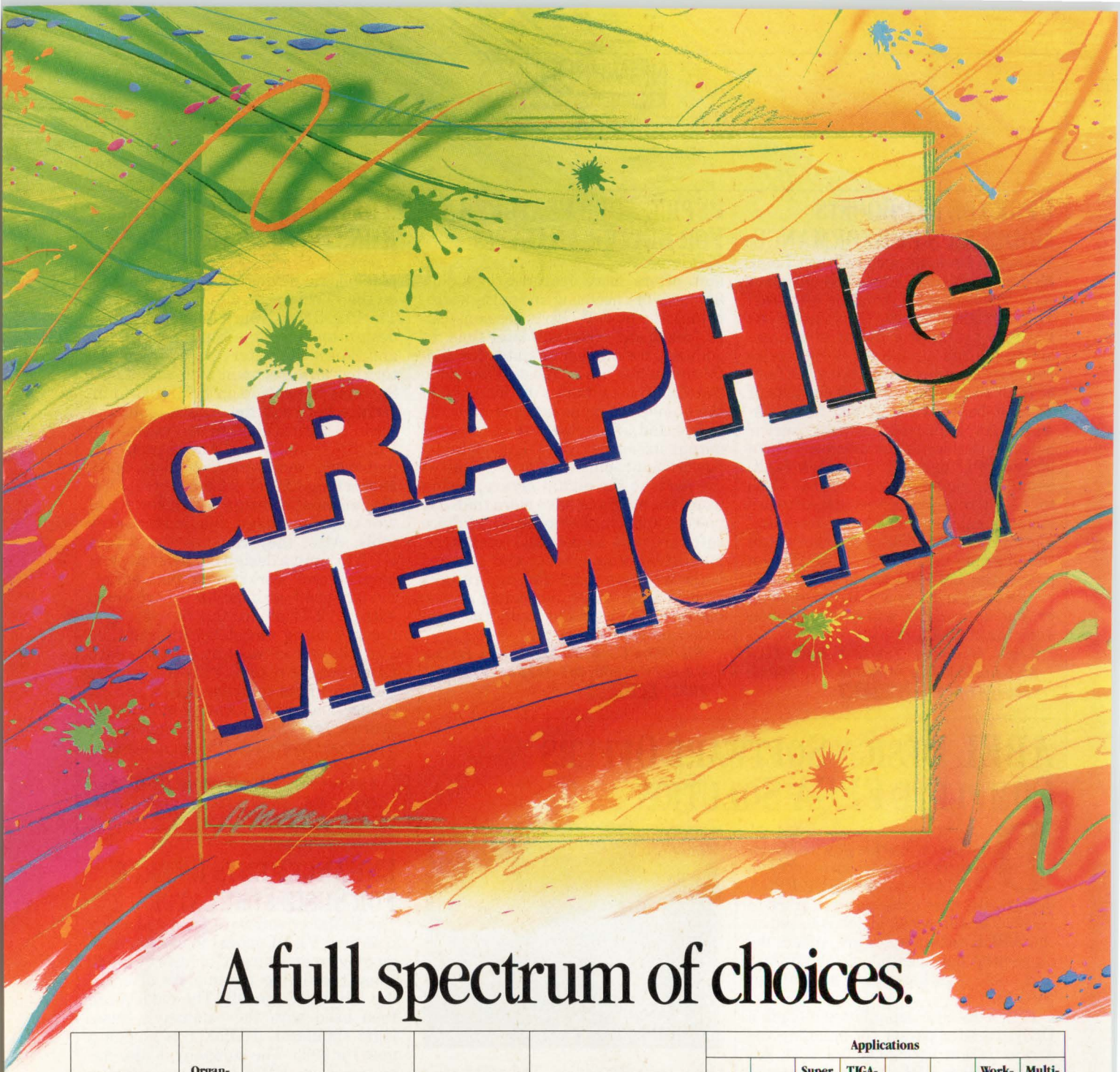
Data I/O Corp.*10525 Willows Rd. N.E., Redmond, WA 98073-9746; (206) 881-6444.* CIRCLE 326

■ *JOHN NOVELLINO*

ENHANCEMENTS EMERGE FOR SUSIE SIMULATOR

The ICMaker software from Aldec is a real-time VHDL-model generator that quickly creates new IC models by modifying the timing parameters of existing VHDL IC models. The models are then used with the company's Susie logic simulator. ICMaker is shipping now for $995. The company is also announcing an EDIF interface between the Susie 6.0 simulator and Mentor-generated schematics. Susie 6.0 and the Mentor interface are being sold together for $9995. Finally, XNF/VT is a Xilinx cell library that allows for real-time simulation of multiple Xilinx parts at the system level using the Susie 6.0 simulator. The cell library is written in VHDL. With XNF/VT and Susie 6.0, users can display cells from different Xilinx parts on the same screen. In addition, users can observe in real time how a change in one cell affects the operation of cells in other Xilinx parts. The XNF/VT cell library includes the 2000, 3000, and 4000 series parts. It's shipping now for $1995.

Aldec Co., 3525 Old Conejo Rd., Newbury Park, CA 91320; (805) 499-6867. CIRCLE 328



A full spectrum of choices.

Device	Organ-ization	Speed (ns)	Package	Micron Part #	Availability	Applications							
						VGA	8514	Super VGA	TIGA-340™	XGA	MAC®	Work-station	Multi-media
1 Meg DRAM	x4*	70 – 100	DIP, ZIP, SOJ	MT4C4256	Now	●		●					
	x16*	80 – 100	ZIP, SOJ	MT4C1664/65/70	Now	●	●	●		●			
4 Meg DRAM	x16*	60 – 100	SOJ, TSOP	MT4C16256/7	Samp. Q4 '91; Prod. 1H '92		●	●		●			
256K VRAM	x4	100 – 120	DIP, ZIP	MT42C4064	Now	●	●	●	●		●	●	
1 Meg VRAM	x4	80 – 120	ZIP, SOJ	MT42C4255/6	4255 Now; 4256 Q4 '91		●	●	●	●	●	●	●
	x8	80 – 120	ZIP, SOJ	MT42C8127/8	8127 Now; 8128 Q4 '91		●	●	●	●	●	●	●
2 Meg VRAM	x8	70 – 100	SOJ	MT42C8256	Samp. Q4 '91; Prod. 1H '92			●	●	●	●	●	●
1 Meg Triple-Port DRAM	x4	80 – 120	SOJ	MT43C4257/8	Now							●	●
	x8	80 – 120	PLCC	MT43C8128/9	Now							●	●

*Also in low power versions.

© Micron Technology, Inc. 1991

MICRON TECHNOLOGY, INC.

2805 E. Columbia Rd., Boise, ID 83706 (208) 368-3800

CIRCLE 95

RF TESTERS EVALUATE EUROPEAN CELLUAR PHONE SYSTEMS

The HP 8922A transceiver test set and HP 8922B base-station test set are multifunction instruments aimed at the new Pan-European digital cellular telephone system. The HP 8922A contains all instrumentation needed to test the RF characteristics of the system's mobile units. The HP 8922B adds the ability to synchronize base stations to system clocks, as well as a large memory and state machine, which are needed to test base stations.

For transmitter measurements, the testers have a frequency-agile local oscillator, coherent data demodulator, pulse demodulator, FM demodulator, and pulse-power meter. A global-method analyzer tests phase and frequency error. Modulation-spectrum measurements are made by a fully synchronized spectrum analyzer. The instruments use high-speed DSP algorithms for fast results.

In addition to these system-specific functions, the testers have several general-purpose instruments. They include a digital oscilloscope, CW frequency counter and power meter, ac voltmeter, 1-kHz distortion meter, audio-frequency counter, and synthesized audio source.

The units contain an Instrument Basic controller that can also control external instruments. Users can write programs and save them on compact memory cards for later reuse. The instruments accept pass/fail limits for many measurements. If the limits are exceeded, the test set will alert the user. For manual operation, one knob controls screen displays and data entry. A CRT displays measurements and user-definable parameters simultaneously.

The HP 8922A costs $60,000, and the HP 8922B is priced at $70,000. Estimated delivery is 14 weeks after receipt of an order.

Hewlett-Packard Co.*Spokane Div., TAFC-34, Spokane, WA 99220-4034; (800) 752-0900.* **CIRCLE 329**

■ *JOHN NOVELLINO*

TEST SOFTWARE OFFERS VERY-HIGH FAULT COVERAGE

The CX-Test software combines with CrossCheck's patented on-chip test structures to efficiently create fully testable ASICs without the performance and functionality trade-offs typical of ASIC test development. With the fault simulation and test vectors supplied by CX-Test, typical fault coverage is 95% to 99%, depending on the ASIC design.

The software works with all types of designs, including synchronous and asynchronous, and chips with RAM or ROM. Gate counts of 10,000 to 100,000 are accommodated. CrossCheck says that CX-Test speeds test-writing time by a factor of 30 to 50 times, compared with other development methods. In addition to the commonly used stuck-at-zero and stuck-at-one faults, CX-Test covers actual manufacturing defects that may escape detection by other test techniques. These defects include open and shorted FETs, open and shorted interconnects, and bridging nets.

The CrossCheck approach to testability fits transparently into the ASIC design flow, requiring no change in established methodologies or tools and no insertion of dedicated test logic into the design. The ASIC manufacturer embeds the on-chip test structures in the base array and library without any intervention by the designer. CX-Test is designed to integrate into popular CAE environments. Presently, the software is available for use with Verilog from Cadence Design Systems and LSim from LSI Logic Corp. The release of CX-Test follows the recent introduction of LSI Logic's FasTest family of 100K HCMOS gate arrays, which are based on the CrossCkeck embedded test structures.

Initially, CX-Test will be available in the ASIC design centers of chip makers that are CrossCheck partners. It's available now at LSI Logic design centers. Call Bill Alexander at (408) 433-4554. CrossCheck is scheduled to market CX-Test directly to ASIC designers during the second half of 1991.

CrossCheck Technology Inc., *2833 Junction Ave., Suite 100, San Jose, CA 95134; (408) 432-9200.* **CIRCLE 332**

■ *JOHN NOVELLINO*

DEVELOPMENT SYSTEMS OFFER VERSATILITY

A family of microprocessor emulation and development systems offers hardware and software solutions for developers of various microprocessor-based systems. The low-cost Zaxpak 1000 products, which are based on the ICD emulator series, run in standalone mode or under control of most personal computers or workstations. The high-performance Zaxpak 2000 systems are based on the ERX line of emulators, which include a PC/AT bus interface. The Zaxpak 2000 Plus adds its own 386SX 16-MHz host to the 2000-series hardware. Systems come with an emulator, cables, and required software. For Ethernet environments, the Axispak includes Ethernet interface hardware and software. Zaxpak systems are available for immediate delivery at prices starting at about $3700.

ZAX Corp., 2572 White Rd., Irvine, CA 92714; (800) 421-0982 or (714) 474-1170. **CIRCLE 330**

SOFTWARE WRITES CODE FOR PC INSTRUMENTS

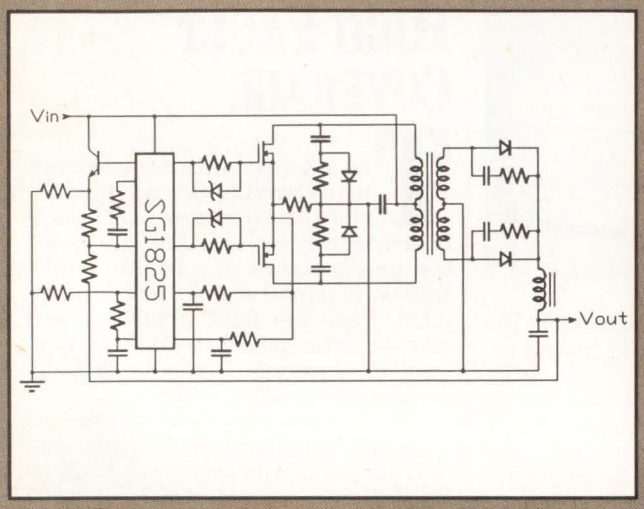
Working together with Burr-Brown's PCI-20026S-1 general-purpose software drivers, the SmartCoder software package simplifies programming of custom data-monitoring applications. The software supports all of the company's PC/XT/AT Personal Computer Instrumentation (PCI) boards, carriers, and modules. Users need not know the internal details of the hardware or the function of the drivers. Instead, they select menu items that represent information about the application and the installed hardware. SmartCoder then writes source code that initializes the hardware, configures the channels, and performs the needed analog, digital, and counter-timer tasks. SmartCoder is available from stock on 3-1/2- or 5-1/4-in. diskettes at a price of $95.

Intelligent Instrumentation/Burr-Brown, 1141 W. Grant Rd., MS-131, Tucson, AZ 85705; (602) 623-9801. **CIRCLE 331**

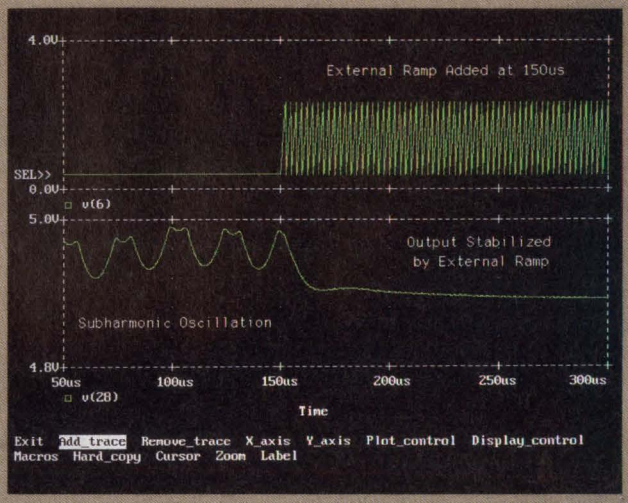
PSpice

MicroSim Corporation

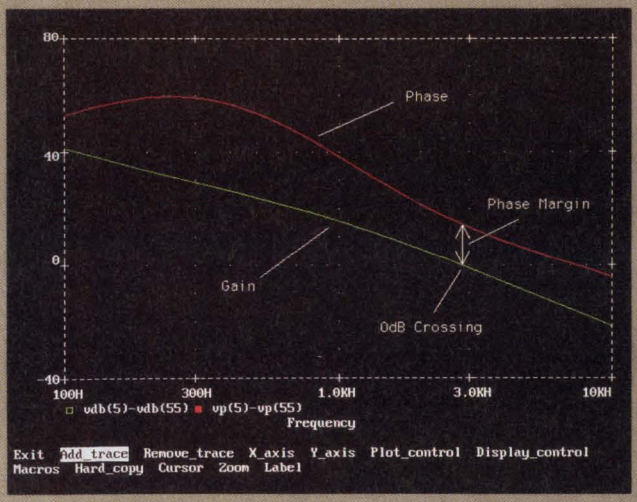
The Standard for Circuit Simulation Switch-Mode Power Supply Design



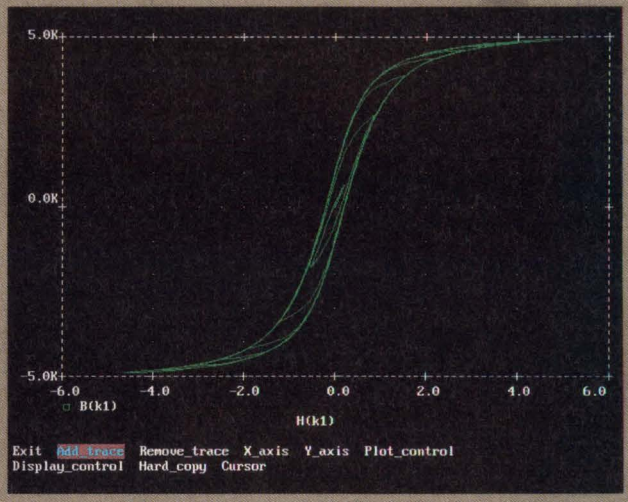
Current mode power supply schematic.



Power supply simulated using mixed analog/digital simulation. Plot shows subharmonic oscillation being suppressed by external ramp.



Simulation using the Vorperian switch model to examine the stability of a power supply.



Hysteresis curve of transformer.

A cycle by cycle simulation of switch-mode power supplies is recognized as a difficult simulation task for SPICE-based simulators, which must cope with timings that can span 4 orders of magnitude. This problem invariably results in very long simulation times, but is improved considerably by MicroSim's approach of building the controller macromodel chips so that a significant section is simulated in the digital domain. PSpice's behavioral modeling and mixed analog/digital simulation capability makes this possible.

PSpice is available on the IBM-PC (running DOS or OS/2); Macintosh II; Sun 3, Sun 4, and SPARCstation; DECstation 2100, 3100, and 5000; and the VAX/VMS families. In addition to the PWM macromodels, the PSpice library contains over 3,500 analog and 1,500 digital parts which can be used in a variety of applications. Our technical staff has over 150 years of combined experience in CAD/CAE, and our software is supported by the engineers who wrote it.

For further information about the PSpice family of products, call us at (714) 770-3022, or toll free at (800) 245-3022. Find out for yourself why PSpice has become the standard for circuit simulation.

20 Fairbanks • Irvine, CA 92718 USA • FAX (714) 455-0554

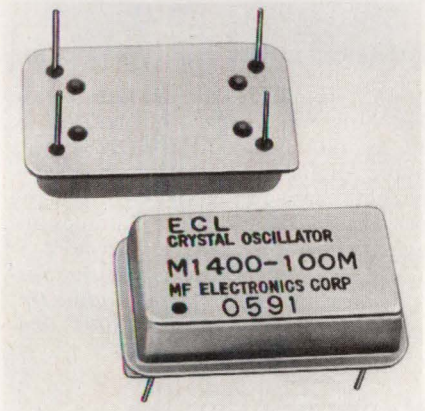
PSpice is a registered trademark of MicroSim Corporation. All other brands and product names are trademarks or registered trademarks of their respective holders.

CIRCLE 94

ECL Clock Oscillator Is First With Enable/Disable

Until now, unlike HCMOS and TTL types, ECL clock oscillators have been unable to perform tristate functions. But the M1900 ECL crystal oscillator offers a tristate enable/disable function that lets the clock be shut off by logic control.

The M1900 oscillator's enable/disable function is activated by logic levels on an input pin. Activation of this pin is achieved by applying a logic "1," which turns off the oscillator. At the same time, this causes the device's output pin to be ECL logic "0." An external ECL signal may then be applied by a tester to the oscillator output node, which will follow the tester. Because of the wired-OR capability of ECL logic, this achieves the same effect as the HCMOS tristate.



In many applications, the clocking speed must be changed by selecting one or two or more active clock oscillators on a board. In TTL and HCMOS, this is done by tristating. ECL applications have in the past had to use AND/OR gates for this function. But with the M1900 oscillator, the outputs of several oscillators may be tied together while only one is enabled.

The M1900 oscillator comes in frequencies from 10 MHz to 225 MHz. Packaging is a four-pin, dual-in-line metal case. Delivery is from stock. Call for pricing.

***MF Electronics Corp.**, 10 Commerce Dr., New Rochelle, NY 10801; (914) 576-6570.* CIRCLE 333

■ *DAVID MALINIAK*

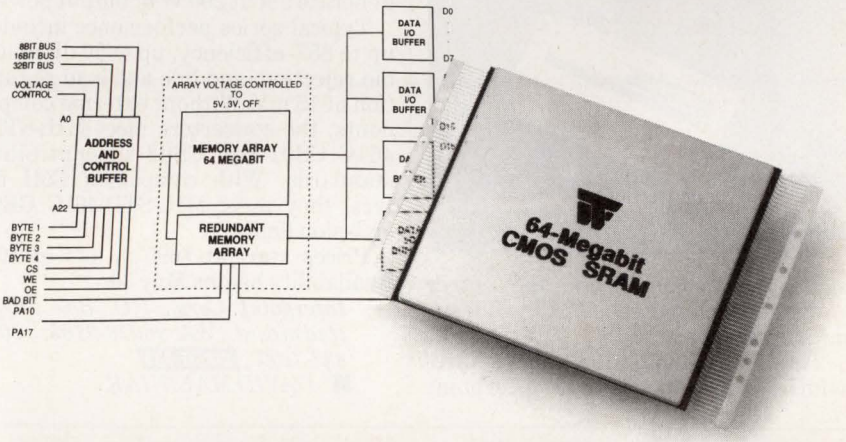
Desktop Display Enhances Efficiency

A desktop display system brings up to 24 characters on each of four lines directly to an individual's desk or workstation. The bright-orange, 0.4-in.-high characters can be read from up to 20 feet away and at a 150° angle. The model DT2404 display comes with an RS-232 interface and power supply. Other features include bottom-line scrolling and an audible-alarm option. Pricing is $800 per unit. Small quantities are delivered from stock.

Telegenix Inc., P.O. Box 5550, Cherry Hill, NJ 08034; (800) 424-5220.

CIRCLE 334

64-MEGABIT CMOS SRAMs



Big Memory, Small Package!!

Here's 64-Megabits of CMOS SRAM memory we've just packed into a 120-pin 3″ x 3.5″ x 0.32″ ceramic flatpack. Just right for designs that need a lot of memory, space is scarce, and temperature is a factor.

Look at these key features.

- User Configurable to:
  8-Meg x 8,
  4-Meg x 16, or
  2-Meg x 32
- 150ns Read/Write Time, Max.
- Low Power
  5 Volt Operation
  120mA Operating Current
  1mA Data Retention Current
- Internal Memory Redundancy Correction Mode
- Temperature Ranges
  Military: −55°C to +125°C
  Industrial: −40°C to +85°C
- Screening and Burn In to Military Standards Are Available Options

If that's not enough memory, these modules can be combined to get you into the Gigabit range and beyond.

And, if you're after non-volative memory, we have that too. We have an 8-Megabit Flash PROM in a 34-pin package, and we're working on a new 128-Megabit Flash PROM in a 3″ x 3.5″ flatpack. We also have a large selection of SRAMs and EEPROMs to fit almost every memory size and package requirement.

More? Yes, much more. We're designing memory systems in the terabit regions, and if you're looking for a complex single-package system, a supercomputer array, or a totally defined multi-package management information system, give us a call. Your imagination or ours, we'll make it happen.

CERTIFIED TO MIL-STD-1772

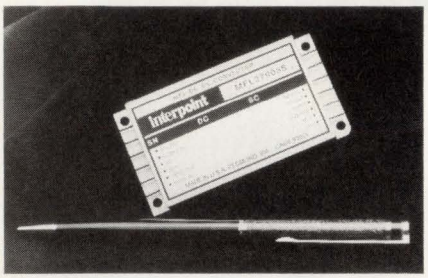
White Technology, Inc.

A wholly owned subsidiary of Bowmar Instrument Corporation
4246 E. Wood Street • Phoenix, Arizona 85040
Tel: (602) 437-1520 • FAX (602) 437-9120

CIRCLE 88

DENSE, HIGH-REL DC-DC CONVERTER SPORTS CURRENT-SHARING ABILITY

Until now, true high-reliability dc-dc converters have been available only in power levels below 70 W. For higher-power applications, designers have had to settle for "pseudo-military" or "ruggedized industrial" converters that don't span the full military-temperature range and can't pass military qualification. Interpoint's MFL series, however, is a true high-rel unit that uses current



sharing to nearly triple the power range for military/aerospace-grade dc-dc converters.

Thanks to a high-frequency pulse-width-modulation design, Interpoint claims a record power density for its individual MFL converters—up to 40 W/in.^{3}. Case measurements are 3 by 1.5 in. with a height of just 0.385 in. The parts are designed for either 28- or 270-V dc input (per MIL-STD-704D), and provide outputs of 5, 12, 15, 28, ±12, or ±15 V at up to 65 W per unit. The modules' input range is 16 to 40 V dc.

The 65-W rating is within the ballpark of other regulators. What sets the MFL Series apart is its current-sharing capability. Three MFL units in parallel generate about 200 W of output power.

Typical series performance includes up to 85% efficiency, up to 50 dB of audio rejection, and line and load regulation of 15 mV. Without external components, the converters meet MIL-STD-461C CS01 and CS02 susceptibility standards. With companion EMI filters, they meet MIL-STD-461C CE03 emission limits.

Prices start at $690 in lots of 100. Availability begins May 30.

Interpoint Corp., P.O. Box 97005, Redmond, WA 98073-9705; (206) 882-3100. **CIRCLE 335**

■ *DAVID MALINIAK*

LOW-NOISE SUPPLIES PRESENT DUAL RANGES

Intended as part of the core instrument set for design, test, and service engineers are the HP E3610A and E3611A benchtop dc power supplies. The supplies feature dual-range outputs and CV/CC operation as well as ripple and noise under 200 μV rms. Ranges are 8 V/3 A and 15 V/2 A for the '10A, and 20 V/1.5 A and 35 V/0.85 A for the '11A. Other features include separate digital displays for voltage and current readout, a CC-set button for setting the supplies' current level without having to short the output, and mode-indicator LEDs. List prices are $300 each. Units are available now.

Hewlett-Packard Co., 19301 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900. **CIRCLE 336**

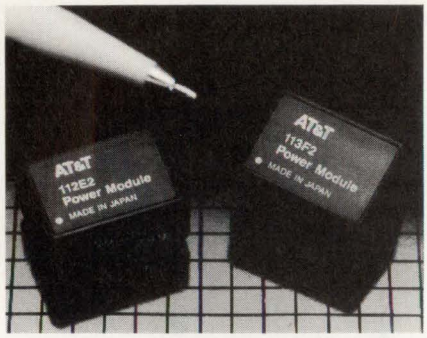
40-W SUPPLY OFFERS THREE OUTPUTS

A 40-W, triple-output supply measuring just 3 by 5 by 1.35 in. has been added to the International MAP family. The line now offers 27 models in a power range spanning 40 to 130 W. The MAP40-3000 has outputs of +5 V at 3 A, +12 V at 2.5 A, and –12 V at 0.5 A. Automatic ac-input selection permits worldwide operation over the range of 90 to 264 V ac. Onboard FCC and VDE filtering meet the Class B conducted-emissions requirements. The supply features tight load regulation of ±0.5% for the main output and ±1% for the others. Output noise and ripple is less than 1% peak to peak over a 20-MHz bandwidth. Pricing varies with quantity ordered. Delivery is from stock.

Power-One Inc., 740 Calle Plano, Camarillo, CA 93010-8583; (805) 987-8741. **CIRCLE 339**

TINY POWER MODULES RUN FROM +5-V INPUT

Two series of power modules deliver highly reliable power to digital and communications applications. The 112- and 113-Series modules are non-isolated switching regulators that operate from a +5-V dc input. Output voltages



of +12, 15, and 25 V are provided by the 112-Series units, while outputs of –5, 12, 15, and 130 V make up the 113-Series units. Minimal external filtering components are required. In lots of 100, the price is $28.60 per module. Samples are available now.

AT&T Microelectronics, Power Systems Business Unit, 3000 Skyline Dr., Mesquite, TX 75149; (800) 526-7819. **CIRCLE 337**

MODULES GIVE 3.3 V OUT FOR 7-TO-35 V IN

Have some of your CMOS ICs moved to 3.3 V, thus requiring a stiff, clean, 3.3-V bus to run them off? If you possess a 7-to-35-V source, Modupower's MP7008 can provide up to 1 A of line- and load-regulated 3.3 V. The MP7101 supplies the same current at a regulated 3.3 V from a 4.5-to-10-V rail. These low-cost 1.5-×-1-×-0.5-in. encapsulated modules are non-isolated dc-dc converters that offer high efficiency (over 80%). Unlike most other modules, these offer self-protection in the form of current-limiting and thermal shutdown. In addition, a shutdown pin, usually connected to ground, is provided. In the case of an external fault detected by a watchdog circuit, or to reduce power, pulling the pin to 5 V reduces the output voltage to zero and the quiescent current to 500 μA. Initial voltage is within 5% of 3.3 V and regulation is within ±5% over specified line and load changes. Quiescent current is 20 mA and output ripple 50 mV pk-pk. In quantities of 1000, the converters run $16 each.

Modupower Inc., 374 Turquoise St. Milpitas, CA 95035; Art Fury, (408) 263-6115. **CIRCLE 338**

EMPLOYMENT OPPORTUNITIES

ELECTRONIC-ELECTRICAL ENGINEERS. Nationwide Design/Project/QC/Mfg., Power, Software/Systems, Controls, Circuits, Equipment, Test, Communications, etc. Contact: John Longberry, **Longberry Employment,** 913 Main Place, P.O. Box 471, Niles, OH 44446. (216) 652-5871.

CONSULTANTS

PRODUCT ENGINEERING & Mfg., Inc.
Over 25 Years Of Experience
We can save you TIME and MONEY, YOU do the ELECTRONICS and we'll do the REST
CONTRACT DESIGN & PROTOTYPING
- **ENCLOSURES**
- **INDUSTRIAL DESIGN**
- **MECHANISMS**
- **AutoCAD – AutoPCB**

MANASSAS, VA **703-754-1508**

Looking for
ELECTRONICS ENGINEERS & ENGINEERING MANAGERS?

More than
165,000
Read
ELECTRONIC DESIGN
Twice Monthly

To reach them with a recruitment ad in the Professional Opportunities section

Contact:
Penton Classifieds at 216-696-7000, ext. 2520

EMPLOYMENT OPPORTUNITIES

Engineering

WARM UP TO FLORIDA.
And heat up your career with an industry leader.

Situated between the shores of Daytona Beach and metropolitan Orlando, talented professionals set the pace at **Sparton Defense Electronics**, a Fortune 900 company involved in the design and high volume manufacture of expendable submarine tracking devices.

The following opportunities are currently open to qualified design engineering personnel for exploration:

- **BSEE's** (no EET degrees) with 2 to 4 years current experience in board level audio/voice frequency (0-20 kHz) analog product design for a high volume manufacturer. Background must include microprocessor programming (i.e., 6800/assembly) and exposure to SMT (surface mount technology). U.S. citizenship required for clearance.
- **BSEE's** (no EET degrees) with 5 years current RF (UHF/VHF) experience specifically in a.m. receivers and multichannel synthesized f.m. transmitters. Small stowable antenna design is highly desirable. U.S. citizenship required for clearance.
- **BSME's** (no MET degrees) with 2 to 5 years current experience in the design of injection molded plastic, die cast metal, and stamped metal parts for a high volume/low cost manufacturer. Solid experience in finite element analysis (FEA) and knowledge of design for assembly (DFA) concepts is highly preferable. Tooling vendor interface and production floor support backgrounds are necessary. U.S. citizenship is required for clearance.

As a team member of **Sparton Defense Electronics**, expect a stimulating, career-building technical challenge, a high quality lifestyle with a low cost of living, no state income tax, proximity to exciting Florida attractions, and a fine compensation package that rewards your skill, knowledge, imagination, and performance. Relocation package is available. For prompt, confidential consideration, please present your credentials with salary expectations to:

SPARTON
DEFENSE ELECTRONICS
ATTN: Mr. John S. Gould, Employment Manager
5612 Johnson Lake Road
DeLeon Springs, Florida 32130

NO AGENCIES PLEASE/NO PHONE CALLS PLEASE/EEO-M/F/H/V

BUSINESS SERVICES

HARDWARE AND SOFTWARE DEVELOPMENT SERVICES
- We specialize in developing microprocessor/FPGA based products/systems and embedded software development.
- Custom Windows V3.0 and networking software development.
- Can help with part of or handle the entire project.
- Full Microprocessor Development Systems, I²ICE, CAD/CAM, and PCB layout system.
- Development for LAN, Multibus, VME, PC, MCA, and STD.

Applied Computer Techniques, Inc.
Tel. (407) 851-2525 Incorporated 1978

FAX YOUR ORDER!
To Advertise in Penton Classifieds,
FAX: (216) 696-1267

LITERATURE

High Tech with Low Risk
John D. Trudel's new guide to increased product success rates and improved profits. "Highly Recommended," Steve Scrupski, Electronic Design, $18.45 from: **Eastern Oregon State College RSI - La Grande, OR 97850 503/962-3755.**
Satisfaction guaranteed.

THE LARGEST FAMILY OF 1MEG SRAMS.

AND MORE ON THE WAY.

Sony's family of 1-Meg SRAMs gets larger and larger all the time.

Our newest additions will include an industrial-grade temperature range, synchronous ASM (Application Specific Memory), and a low, 3-volt power requirement.

We've also adopted all of the industry's most popular package styles, making our family more compatible with all of your PCB designs.

And with the full support of two production facilities – plus another one due soon in San Antonio, TX – we'll be producing more 1-Meg SRAMs than ever.

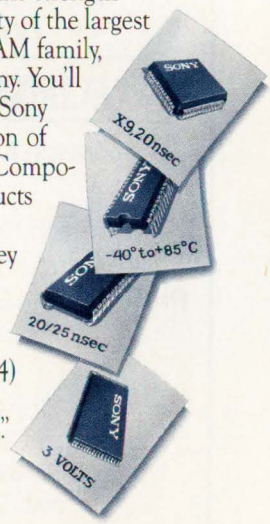
If you still can't find the right high-density SRAM, we've got your answer – a full team of designers in the USA, armed with 0.8-micron CMOS technology. And they're ready now to discuss your needs.

So, for the strength and security of the largest 1-Meg SRAM family, look to Sony. You'll find us at Sony Corporation of America, Component Products Company, 10833 Valley View St., Cypress, CA 90630. For details, call us at (714) 229-4190, FAX us at (714) 229-4285, or write to us "Attn: Communications."

Sony 1 Megabit SRAM Family Tree

	Model	Speed (ns)	Packaging	Data Retention Current	Special Features	Availability
128Kx8	CXK581000P	100/120/150	DIP 600mil	L/LL	B/X	Now
	CXK581000M	100/120/150	SOP 525mil	L/LL	B/X	Now
	CXK581100TM	100/120/150	TSOP	L/LL	B/X	Now
	CXK581100YM	100/120/150	TSOP (reverse)	L/LL	B/X	Now
	CXK581001P	70/85	DIP 600mil	L/LL		Now
	CXK581001M	70/85	SOP 525mil	L/LL		Now
	CXK581020SP	35/45/55	SDIP 400mil			Now
	CXK581020J	35/45/55	SOJ 400mil			Now
128Kx9	CXK77910J	20	SOJ 400mil		Sync ASM	2H '91
256Kx4	CXK541000J	25/30/35	SOJ 400mil			2H '91

L = Low LL = Low, Low B = 3 Volt X = Extended Temperature



SONY

Sony is a registered trademark of Sony Corporation.

CIRCLE 144

DIRECT CONNECTION ADS

ELECTRONIC DESIGN

DIRECT CONNECTION ADS
New Products/Services Presented By The Manufacturer.
To Advertise, Call JEANIE GRIFFIN At 201/393-6080

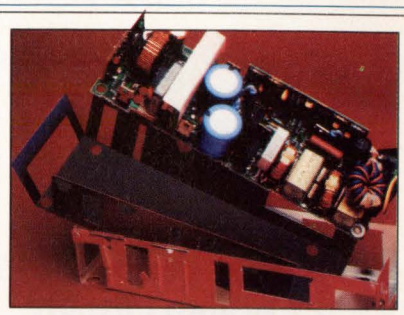
Little Giant™
New! Tiny Giant™
C Programmable Controllers

We have miniature controllers with parallel I/O, solenoid drivers, A/D and D/A converters, clock, watchdog, LCD interface, RS485 serial, built-in power supply and much more! Use them to control anything. Our $195 interactive Dynamic C™ development system makes software development easy. These units have high performance and serious software support. We also have design-your-own-board core modules as low as $59.

$159
(Tiny Giant Digital, qty. 1)

Z-World Engineering
1340 Covell Blvd., Davis, CA 95616 USA
(916) 753-3722
Regular Fax: (916) 753-5141
Automatic Fax: **(916) 753-0618**
(Call from your fax, hear computer voice, use touchtone dial to request desired data sheets.)

Z-WORLD ENGINEERING **CIRCLE 282**



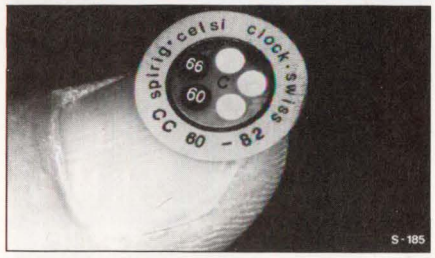
SAVE MONEY
With Lexan® FR700 Film For Barrier Insulation

• UL94 V-0 rated at .010" • High heat resistance of 275°F • Excellent dielectric strength • Easy fabrication–sharp folds, intricate die-cut shapes • Competitively priced • Call for free information: **(800) 451-3147**

GE Plastics
Structured Products

® Registered Trademark of GE.

GENERAL ELECTRIC **CIRCLE 263**



Put a low cost CelsiClock® temperature monitor on any surface.

The temperature indicating spots turn permanently black when the surface to which the CelsiClock® is affixed reaches the specific "switch" temperature level of that spot. Available in multiple sequenced temperature increments from 40°C up to 260°C. Free samples on inquiry.

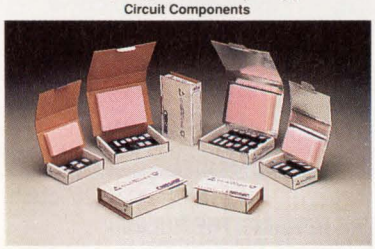
CELSI®, the reliable "Temperature Watchdog" from

SAT Solder Absorbing Technology Inc., a Spirig Company
144 Oakland St., Springfield, MA 01108
(413) 788-6191 TOLL FREE (800) 628-8862
FAX: (413) 788-0490

SOLDER ABSORBING TECHNOLOGY **CIRCLE 251**

CHIPSHIP™

For Safely Shipping and Transporting your Circuit Components



These double folded, crushproof, shock and vibration resistant IC mailers with ESD protection are a low cost, time saving solution for transporting small quantities of components. Complete with bonded anti-static foam cushioning and high grade conductive foam inserts, they are available with and without EMI/RFI foil lining.

Model	Size	IC Capacity 8 pin	16 pin	28 pin	40 pin	Features	Prices (10-49)
ChipShip™ **800**	5 1/2" x 3" x 1 1/2"	55	26	7	5	Standard	$ 2.95
ChipShip™ **850**						Foil Lined	$ 3.95
ChipShip™ **900**	6 1/2" x 4 1/2" x 1 1/2"	120	70	19	12	Standard	$ 3.60
ChipShip™ **950**						Foil Lined	$ 4.95

i TOI ENTERPRISES P.O. Box 59, Newton Highlands, MA 02161
TEL: (617) 332-1010

iTOI ENTERPRISES **CIRCLE 275**

CHIPSAFE™

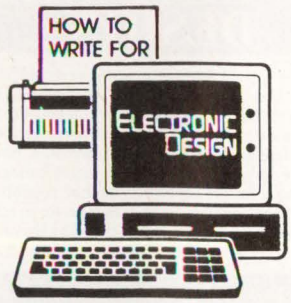
For Safely Storing, Organizing, Archiving and Transporting Your IC Components

Our handsome, Crushproof, Dust-Tight, Snap-fastened IC Storage albums with ESD protection are the perfect solution for physically and electrically protecting your library of IC MASTERS, MODS, REVS and samples. In stock for immediate delivery.

Product	Model	Size	Chip Capacity (DIP) 8 pin	16 pin	28 pin	40 pin	Features	Prices (1-4)
ChipSafe™	100	7" x 10"	528	264	76	56	Maximum IC storage	$ 16.95
ChipStore™	200	7" x 10"	264	132	38	28	Combination IC & diskette storage	$ 16.95
			5	5	1/4" diskettes			
ChipCarry™	300	5" x 6"	120	70	19	12	Briefcase size IC storage	$ 12.95
ChipPocket™	400	3" x 4"	55	26	7	5	Shirt pocket size	$ 6.95

i TOI ENTERPRISES P.O. Box 59, Newton Highlands, MA 02161
TEL: (617) 332-1010

iTOI ENTERPRISES **CIRCLE 276**



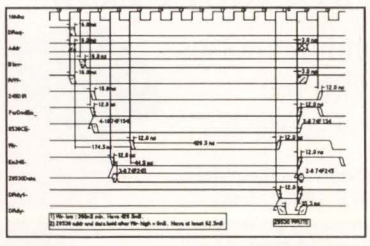
ELECTRONIC DESIGN AUTHOR'S GUIDE

Thinking of writing a technical article for publication in Electronic Design? This 12-page brochure contains just about everything you need to know about the process: submitting the outline, tips on writing the manuscript, preparing the artwork, and more.

ELECTRONIC DESIGN
611 Route #46 West
Hasbrouck Heights, NJ 07604

ELECTRONIC DESIGN

CUT DESIGN TIME IN HALF!



dV/dt® Timing Diagram Accelerator

POWERFUL FEATURES INCLUDE:

- "What-if" analysis
- Calculation of critical edge timing
- Display and verification of IC timing requirements
- And many more features...all for **ONLY $695!!**

"I use dV/dt quite a bit. It's a terrific product that saves me weeks of design time!" Tony Radice, General Instrument

CALL FOR A FREE EVALUATION PACKAGE

Phone **619-457-4545** Fax **619-457-1168**
Doctor Design • 5415 Oberlin Drive • San Diego • CA • 92121

DR. DESIGN **CIRCLE 259**

Telecom Solutions from Teltone

S.I.T. & International Tone Detector

M-984 is a low-power 14-pin CMOS DIP that detects S.I.T.s (special information tones), OCC (other common carrier), dial tone (400 Hz), as well as many international call progress tones.

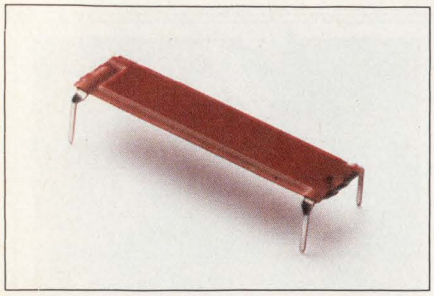
- Single 5-volt supply needed
- 3.58 MHz time base
- 30 dB dynamic range
- Tri-statable outputs

1-800-426-3926
Or: 206-487-1515 Fax: 206-487-2288

TELTONE®
INNOVATING SOLUTIONS
In Telecom Interface Components

Teltone Corporation, 22121-20th Avenue SE, Bothell, WA 98021

TELTONE **CIRCLE 267**



SIMPLIFY BOARD LAYOUT

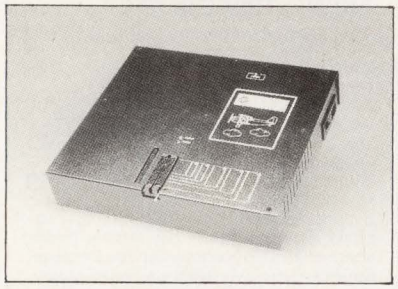
MICRO/Q 1000 ceramic decoupling capacitors share board mounting holes with IC pins to simplify board design. Now add more active devices with increased density in the same space, or design the same package on a smaller board.

Send for your free information.

ROGERS CORPORATION
2400 S. Roosevelt St.
Tempe, AZ 85282. Phone: (602) 967-0624

ROGERS CORP. **CIRCLE 269**

NEW, POWERFUL, UNIVERSAL



PILOT-U40 is our second generation 40-pin universal programmer, following the very successful and popular Sailor-PAL line of programmers. Programs PALs, GALs, PROMs, E/EPROMs, micros, AMD MACH-110, etc, etc. 28-pin and 32-pin versions also available. Industrial quality. $1,095 to $2,495. Satisfaction guaranteed.

408-243-7000, 800-627-2456, Fax 408-736-2503

ADVIN SYSTEMS INC.
1050-L E. Duane Ave., Sunnyvale, CA 94086

ADVIN SYSTEMS **CIRCLE 270**

Electronic Enclosures Catalog on Free PC Diskette

Modular electronic enclosures can be easily specified on any IBM compatible PC using a new, free program. Selections include vertical racks and slope front consoles for standard or EMI/RFI shielded requirements. Work stations and instrument cabinets are also included. Printout can be Faxed or mailed for quotation or order.

Equipto Electronics Corporation, 351 Woodlawn Ave., Aurora, IL 60506-9988, Phone: (708)897-4691, Fax: (708)897-5314

EQUIPTO ELECTRONICS **CIRCLE 273**

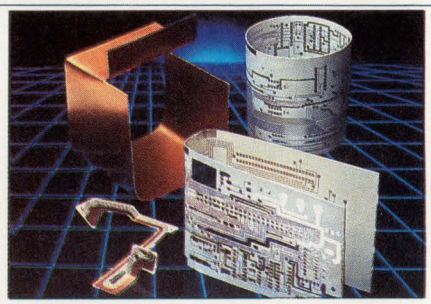
RELIABILITY PREDICTION SOFTWARE

ARE YOUR PRODUCTS RELIABLE?

The RelCalc 2 Software Package predicts the reliability of your system using the part stress procedure of MIL-HDBK-217E, and runs on the IBM PC and full compatibles. Say goodbye to tedious, time consuming, and error prone manual methods! RelCalc 2 is very easy to use, and features menu windows, library functions, global editing for what-if? trials, and clear report formats. Try our Demo Package for $25.

T-CUBED SYSTEMS, 31220 La Baya Drive # 110, Westlake Village, CA 91362. (818) 991-0057 • FAX: (818) 991-1281

T-CUBED SYSTEMS **CIRCLE 271**



WE'RE BENDING THE RULES FOR CIRCUIT DESIGNERS

BEND/FLEX™, the bendable circuit board material that's flexible enough to bend into any multi-plane shape. Eliminates stiffener boards, flexible hardboard connectors, and may reduce the cost of two - and three - plane interconnection systems by as much as 30%!

ROGERS CORP.
COMPOSITE MATERIALS DIVISION
One Technology Drive, Rogers, CT 06263

BEND/FLEX™ **CIRCLE 261**

The world's broadest line of EL flat panel displays.

PLANAR 503-690-1100

PLANAR **CIRCLE 278**

Design PLDs with ABEL-PLD, now just $495.*

FREE ABEL-PLD start-up kit!

- 150 PLD architectures supported (over 4000 devices)
- Uses ABEL™ Hardware Description Language (ABEL-HDL™)
- Intelligent synthesis and optimization
- Upgradable to full-featured ABEL

Call for your FREE ABEL-PLD start-up kit!

1-800-247-5700

*U.S. list price only. Limited-time offer.

DATA I/O Corporation

DATA I/O CORP. **CIRCLE 255**

Program PLDs and memories with the low-cost 212.

Now supports the 27C4001, 87C51 and 22CV10!

- Supports more than 450 CMOS devices
- Memory cards for easy updates
- Extensive editing capabilities
- Compatible with JEDEC standard programming files

Call for your FREE 212 15-day trial!

1-800-247-5700

DATA I/O Corporation

DATA I/O CORP. **CIRCLE 256**

PC KEYBOARD DESIGN

This book will tell you how to use the keyboard port as an input for your embedded system. It defines the protocol between the keyboard and computer for both the XT and the AT, and describes methods for the detection, debounce, and buffering of keyswitches. Schematics cover the hardware design, and the accompanying diskette contains source code for the keyboard's internal controller. The hardware and firmware design example is for an automatic teller application. PC Keyboard Design, by Gary Konzak, is $249.

FREE We'll include a free copy of the pocket-sized **XT-AT Handbook by Choisser and Foster** with each AT Bus Design book if you tell us where you saw this ad. Of course, this $9.95 value is also available by itself. Or buy five or more for only $5.00 each.

VISA **800-462-1042** MasterCard
619-271-9526
AMERICAN EXPRESS

Annabooks
12145 Alta Carmel Ct., Suite 250
San Diego, CA 92128

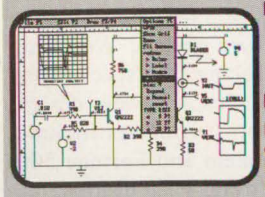
FAX 619-592-0061
Money-back guarantee

ANNABOOKS **CIRCLE 252**

DIRECT CONNECTION ADS

Analog Circuit Simulation

Completely Integrated CAE from $95



From Schematic Entry through SPICE Simulation to Post Processing

IsSPICE $95, the complete SPICE program, runs on all PC's.

IsSPICE/386 $386, The fastest PC based SPICE program available. Has virtually no circuit size limitations.

SPICENET $295, a schematic editor for any SPICE simulator. Generates a complete SPICE netlist.

INTUSCOPE $250, a graphics post processor that performs all the functions of a digital oscilloscope.

PRESPICE $200, extensive model libraries, Monte Carlo analysis, and parameter sweeping.

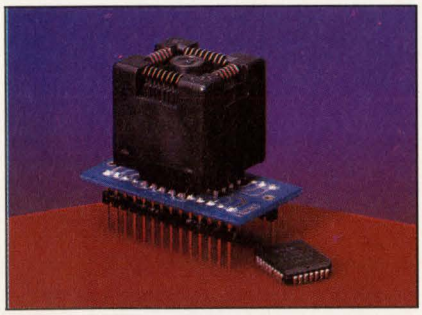
Please Write or Call

intusoft

P.O. Box 6607
San Pedro, CA
90734-6607

(213) 833-0710
30 Day Money
Back Guarantee

INTUSOFT **CIRCLE 272**



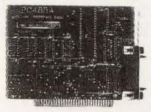
PAL/PROM Programmer Adapters

- Any EPROM programmer designed for DIPs can be converted to accept LCC, PLCC, and SOIC sockets in seconds!
- To program, just insert an Adapt-A-Socket™ between the programmer's DIP socket and the circuit to be programmed.
- Designed to fit all types of EPROM programmers, including Data I/O 120/121A, Stag, Logical Devices, etc.
- Quick turnaround on custom engineering services, if needed. For a free catalog, contact:

Emulation Technology, Inc.
2344 Walsh Ave. Santa Clara, CA 95051
Phone: 408-982-0660 FAX: 408-982-0664

ET

EMULATION TECHNOLOGY **CIRCLE 262**



LOW COST INTERFACE CARDS FOR PC/XT/AT

RS-485/422 Card [PC485] $95/125

- Serial Async. Communication up to 4,000ft; 2 or 4 wires; NS16450 UART;
- COM1-4; Max. Baud Rate 56KB. **High speed version (256KB) - $165.**
- **Dual drivers/receivers;Handles 64 devices;**Compatible with most comm S/W.
- DB9 or phonejack. **Sample programs included.** Optional sourcecode - **$150**

Dual-Port RS-485/422 [PCL743] $175

- Two independent channels/UARTs; 2 or 4 wire operation. Max. Baud 56KB.
- Dipswitch configurable as COM-4 (IRQ2-7). On board terminator resistor.

IEEE-488 Card [PC488A/C] $145/445

- Includes **DOS Device Driver** and sample Communication program in **BASIC.**
- Additional sample programs in **C, Pascal & Assembly - $50.**
- **Selectable IRQ (1-6). DMA** channel **1** or **2.** Up to **four boards** per computer.
- Compatible with most **IEEE-488 Software packages** for IBM-PC.
- I/O Addresses and Control registers compatible with NI's **GPIB-PCIIA**
- PC488C card version with Built-In Bus Analyzer hardware and software

Stepper Motor Card [PCL838] $395

- Capable of independent and simultaneous control of up to **3 stepper motors.**
- **Programmable speed** from 1 to 10,000 pps; Steps per command 1 to 65535.
- **DIP switch selectable** I/O port base address and wait state. 24 bit TTL I/O port
- Crystal based timing; **All control signals opto-isolated.**

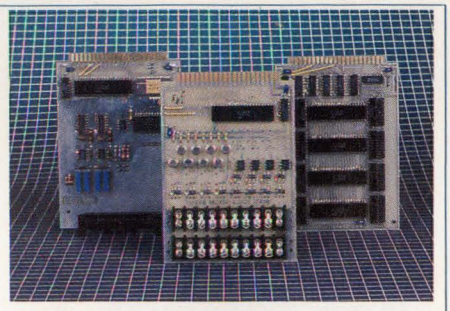
144 Bit Digital I/O [PCL722] $345

- 144 lines (24 bits x 6 ports) of TTL compatible digital I/O. Output buffers sink 24mA, source 15mA.Interrupt handling capability. Opto-22 module compatible.

MC / VISA / AMEX *Call today for datasheets!*

B&C MICROSYSTEMS INC.
750 N. Pastoria Ave., Sunnyvale, CA 94086 USA
TEL: (408)730-5511 FAX: (408)730-5521

B&C MICROSYSTEMS **CIRCLE 254**

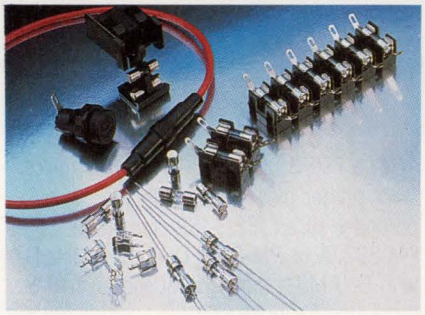


6800/6809 MICRO MODULES.

OEM 6800/6809 MICRO COMPUTER MODULES for dedicated control and monitoring. Interfaces for sensors, transducers, analog signals, solenoids, relays lamps, pumps, motors, keyboards, displays, IEEE-488, Serial I/O, floppy disks.

WINTEK CORPORATION,
1801 South Street. Lafayette, IN 47904-2993.
(317) 742-8428 or (800) 742-6809

MICRO MODULES **CIRCLE 260**

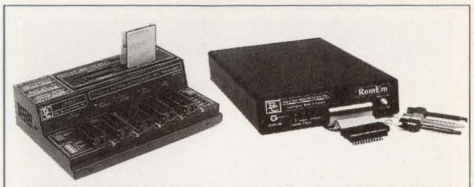


2AG FUSES AND ACCESSORIES

SPACE SAVING subminiature fuse is 1/4 the volume of standard 3AG fuse with same operating characteristics thru 10 amperes in Slo-Blo® or Fast acting designs. Can be supplied board washable. Complete line of accessories include panel-mount and FLIP-TOP fuseholders, mounting blocks, PC Board fuse clips, in-line fuseholders, ideal for applications requiring space-saving, economical circuit protection.

Call Littelfuse (708) 824-0400 or FAX (708) 824-3024.

LITTELFUSE **CIRCLE 266**



RS232 EE/EPROM, MICRO & MEMORY CARD PROGRAMMER $345/495

- Programs **EE/EProms, Flash Eproms, ZPRams, Intel Micros, Memory Cards.**
- **Stand-Alone Mode** for EE/EProms and Memory Card Duplication / Verify.
- All 24/28/32 pin EE/EProms to **8 MBits** (upgradeable to **32 Megabits**). Micros:8741/A,-2/A,-4,-8,-9,-51,-C51,-C51FA/B,-52,-53,-55,-C521,-C541,9761.
- Accepts dedicated modules: **Memory Card Programming Module** (Seiko/Epson) - $145, **Eraser/Timer Module** - $50, **Gang Module** (4 sockets) - $145. Simultaneously duplicates up to 5 devices in stand-alone mode (with Gang).
- Can be operated with any computer containing an **RS-232 serial port.**
- **User friendly Menu-Driven Interface Program for IBM-PC** or compatible.
- **Full 1 year warranty.** Customer support via voice line, fax or **dedicated BBS.**

INTELLIGENT ROM EMULATOR $395

- Emulates **2716** through **27512** EProms with a single unit. **Access time 120ns.**
- Connects to the **standard parallel printer port** via a standard printer cable.
- User friendly software. Command set includes: **Load**(data), **Write**(data), **Display**(memory),**Type**(of EProm),**Edit**(memory),**Fill**(memory),**Calculator, Reset**(target system),**Activate**(debugging feature),**Monitor**(selected feature).
- **Address Compare with Halt output, Address Snapshot, Trigger input.**
- **Fast data loading via parallel printer port (64k bytes in less than 10 sec).**
- **Cascadable up to 8 units.**Includes target cable with Trigger/Reset/Halt clips.
- CMOS (stand-alone) model with rechargeable NiCad battery backup: **$495**

MC / VISA / AMEX *Call today for datasheets!*

B&C MICROSYSTEMS INC.
750 N. Pastoria Ave., Sunnyvale, CA 94086 USA
TEL:(408)730-5511 FAX: (408)730-5521

B&C MICROSYSTEMS **CIRCLE 253**

FREE! 120 Page Catalog

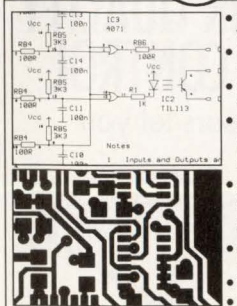
"Optics for Industry"

ROLYN OPTICS supplies all types of "Off-the-Shelf" optical components. Lenses, prisms, mirrors, irises, microscope objectives & eyepieces plus hundreds of others. All from stock. Rolyn also supplies custom products & coatings in prototype or production quantities. Write or call for our free 120 page catalog describing products & listing off-the-shelf prices. **ROLYN OPTICS CO.**, 706 Arrowgrand Circle, Covina, CA 91722, (818) 915-5707 & (818) 915-5717. TELEX: 67-0380. FAX: (818) 915-1379.

ROLYN OPTICS **CIRCLE 283**

PCB and SCHEMATIC C.A.D.

EASY-PC ($195) **EASY-PC**



- **Runs on PC/XT/AT/286/386 with Herc, CGA, EGA, VGA.**
- **Design Single sided, Double sided and Multilayer boards.**
- **Provides Surface Mount support.**
- **Standard output includes Dot Matrix / Laser / Inkjet Printer, Pen Plotter, Photo-plotter and N.C. Drill.**
- **Award Winning EASY-PC is in use in over 7500 Installations in 50 Countries World-wide.**
- **SUPERBLY EASY TO LEARN AND USE.**
- **Not Copy Protected.**
- **Dealers Wanted.**

Additional Libraries and Gerber Import available!

For full info', write, fax, call or use Inquiry # **1**

BRITISH DESIGN AWARD 1989

Number One Systems Ltd.
REF: EDUS, HARDING WAY, ST.IVES, HUNTINGDON, CAMBS, ENGLAND, PE17 4WR.

Telephone:	Fax:	
USA: 011-44-480-61778.	USA:011-44-480-494042	AMEX,VISA,
Intnl:- +44-480-61778	Intnl:- +44-480-494042	MasterCard
UK :- 0480 61778	UK :- 0480 494042	Welcome

NUMBER ONE SYSTEMS LTD. **CIRCLE 265**

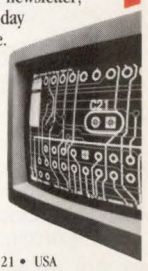
"Tango gives us more than just great CAE/CAD tools."

"We love using every one of the programs in the Tango design suite. But owning Tango tools means more than getting high performance and quality output at an affordable price. It also means getting that extra measure of value with ACCEL's excellent service and support."

Manfred Koch
President, O.E.M. manufacturer

With each Tango design tool for schematic entry and PCB and PLD design, you'll get: thorough documentation; friendly customer service; affordable updates; reliable technical support; BBS; user newsletter; and a 30-day guarantee.

Tango®



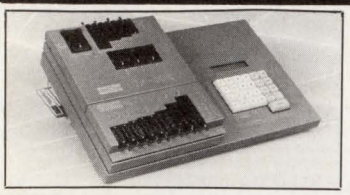
See for yourself. Call today for information or a **free** evaluation package.

800 488-0680
619 554-1000 • FAX: 619 554-1019

ACCEL Technologies, Inc.
6825 Flanders Drive • San Diego, CA • 92121 • USA
Contact us for the representative nearest you.

ACCEL TECHNOLOGIES **CIRCLE 274**

DESIGN & PROGRAM PLDs



BYTEK PLD MULTIPROGRAMMER® *plus*
FREE PLD design Software - **$2495.00**

- Program PLDs up to 40-pin. (44-68 pin opt.)
- Micro Disk Drive for easy library updates.
- Stand-alone with extensive editing.
- RS232 & Parallel ports for high speed transfer.
- Intelligent Synthesis & Optimization.
- Choice of Design Entry: High Level Equations, Truth Tables or State Diagrams.

Memory Programmers from $495.

Call now: 1-800-523-1565

BYTEK Corporation
543 NW 77th St., Boca Raton, FL33487
(407) 994-3520 FAX: (407) 994-3615

BYTEK CORPORATION **CIRCLE 257**

COAX/TWINAX/TRIAX INTERCONNECT COMPONENTS AND ACCESSORIES

Trompeter's 80-page **T18 Catalog! 1000+** interconnect components and cables. Indexes for **Broadcast, Telecom** and **Military** applications and a quick Reference Product Guide. Technical paper **"Electronic Systems Wiring and Cable".** Cable Tables expanded to 800+ cables. **Our newest products!** Quality connectors, patching products, cables and cable assemblies. **New look! Easier to use!**
Trompeter Electronics, Inc.
31186 La Baya Drive,
Westlake Village, CA 91362-4047
Phone (818) 707-2020 Fax (818) 706-1040

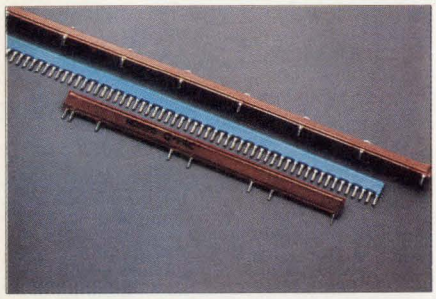
TROMPETER **CIRCLE 285**

NEED ENGINEERING SUPPORT?

Let GNOSTECH help develop your next hardware or software product. We are an engineering consulting firm specializing in custom electronics, software, design and development. Customers include both the government and Fortune 500 companies with world wide distribution. Our experience includes: Data Acquisition and Analysis, Real Time Simulation and Process Control. Our specialty is customer satisfaction. Call or write for more info:

Gnostech Inc.
650 Louis Drive, Suite 190
Warminster, PA 18974
(215)443-8660

GNOSTECH **CIRCLE 279**



SAVE SPACE WITH Q/PAC® COMPONENTS

- Provide built-in capacitance
- Eliminate decoupling capacitance
- 4-layer board quietness, 2-layer economy
- Vertical or horizontal mounting

Send for Rogers Q/PAC® Application Bulletin

Rogers Corp., 2400 S. Roosevelt St.
Tempe, AZ 85282 602/967-0624

ROGERS CORP. **CIRCLE 258**

FREE Color Printer with purchase of DSO

Get a FREE high-quality 9-pin graphics color printer plus cables with the purchase of an IEEE-488 compatible PM 3320A or PM 3323 DSO (300 MHz B/W with 500 MS/s sampling speed and 10-bit resolution for <$9,250.**)

Call **800-44-FLUKE, ext. 77** today!

FLUKE®

*Offer good through July 31, 1991.
**U.S. list price only.

JOHN FLUKE **CIRCLE 284**

NEW! **iceMASTER™** COP8 8051 68HC11

YOUR WINDOW TO EMULATION PRODUCTIVITY

- **Easy to learn & use**
- **Windowed interface -- user configurable**
- **FAST! Download -- < 3 sec. typ. at 115KB**
- **Source Level debug**

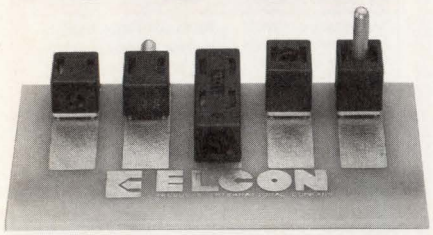
- **A 4K frame trace buffer** with advanced searching capabilities.
- **Hyperlinked On-line help** guides you through the emulation process.
- **iceMASTER** connects easily to your PC, requires no disassembly, or expansion slots. Works on any PC (DOS or OS/2), MicroChannel or EISA. Even laptops!
- **Supports more than 50 different 8051 family derivatives.** M68HC11 support will be available early in 1991.
- **Try iceMASTER risk free!** Satisfaction Guaranteed or return for a full refund! *
- **RENTALS AVAILABLE!** Ideal for consultants and researchers!
- **Call today for free demo disk and ask about a free 8051 Macro Assembler! (800) 638-2423**

MetaLink Corporation
MetaLink Corporation P.O. Box 1329 Chandler, Az 85244-1329
Phone: (602) 926-0797 FAX: (602) 926-1198 TELEX: 4998050MTLNK
* With 10-day trial period

FREE ASSEMBLER

METALINK **CIRCLE 277**

ICCON™



BOARD LEVEL, HIGH-CURRENT CONNECTORS

- High current, low voltage drop
- Power distribution applications
- Board-to-board configurations
- Blind mate capability
- Standard DIP footprint
- Parallel or perpendicular modules

ELCON PRODUCTS INTERNATIONAL COMPANY
P.O. Box 1885, Fremont, CA 94538
PH. (415) 490-4200 • FAX (415) 490-3740

ELCON **CIRCLE 281**

Figaro sensors let you KEEP IT FRESH:

Automatic air cleaning begins with accurate, *continuous* measurement of air quality. Figaro gas sensors are available to meet your most demanding applications.

Write or call for further information:

FIGARO USA, INC.
1000 Skokie Blvd., Ste. 575, Wilmette, IL 60091
Phone: (708) 256-3546 Fax: (708) 256-3884

FIGARO **CIRCLE283**

YOUR AD HERE

Here's all you have to do:

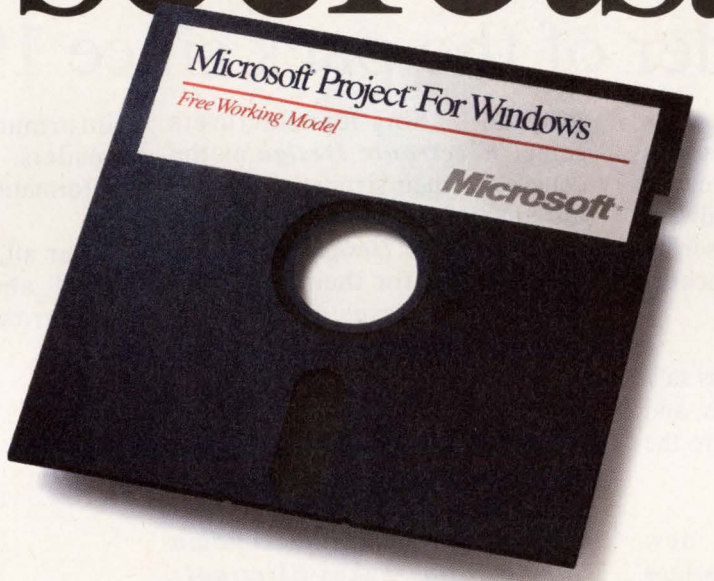
- Send a B/W or 4C glossy photo.
- Include 13 lines of copy. (37 characters per line)
- Write a headline of 32 characters or less.

We do all the rest.
No production charges.

We also accept camera-ready art.
Ad size $2\frac{3}{16}$″ wide × 3″ deep.

ELECTRONIC DESIGN

We're giving away our management secrets.



More project managers are turning to Microsoft® Project for Windows™, the number one management package*.

Probably because Microsoft Project for Windows wouldn't be any different if you'd planned it yourself.

Work with data easily. Create customized filters, tables, even output. Manipulate PERT and Gantt charts by clicking and dragging.

See for yourself. Just give us a call at (800) 541-1261, Dept. P96, and we'll send you a free working model.

Microsoft®
Making it all make sense™

Project for Windows has been given top honors in PC World, InfoWorld, Software Digest *and* PC Magazine. *Offer good until June 30, 1991 or while supplies last. The first working model is free, not including shipping and handling; additional models are $9.95 plus applicable sales tax and shipping and handling. Offer good only in the 50 United States. In the U.S., call (800) 541-1261, Dept. P96. For information only: In Canada, call (416) 568-3503; outside the U.S. and Canada, call (206) 936-8661.* *© 1991 Microsoft Corporation. All rights reserved. Microsoft and the Microsoft logo are registered trademarks and Windows and* Making it all make sense *are trademarks of Microsoft Corporation.*

Get your technology news where the rest of the world does... first!

Electronic Design: Leader of the pack since 1952

Electronic Design* is the industry's most-often quoted electronics publication.** There's a good reason for this: ***Electronic Design is always the first to report on and describe new technologies as they occur. We're proud of this reputation.

Lots of engineering publications talk about new products, new issues, and new technology. New items are the essence of news reporting.

But when you read about new technology or new implementations of technology in an electronics magazine - *any* electronics magazine - it's likely that the story was first discussed in ***Electronic Design.***

Why do leading manufacturers select ***Electronic Design*** as the vehicle for their significant product introductions? Because they know that ***Electronic Design*** is the ideal environment for their important debuts. Each issue contains the latest information on tools and techniques to help shorten the design cycle, helping our readers to incorporate the latest products and technology into their designs.

Proven leadership in circulation and editorial makes *Electronic Design* *the* source of critical design information for 165,000 global readers. And we're first with the information you need in your job.

After all, why should you wait and read about it somewhere else tomorrow?

YES!
I want my technology news as it happens.

YES! I want my technology news as it happens.
Please begin my subscription to *Electronic Design* immediately.

1 year, 24 issues for $85.00.

Name:_____
Address:_____
City :_____ State:_____ Zip:_____

For subscriptions to Canada, add $75.00; foreign subscriptions, add $145.

Send to: Penton Publishing, P.O. Box 95759
Cleveland, Ohio 44101; attn: Juanita Roman

ELECTRONIC DESIGN

INDEX OF ADVERTISERS

A

ACCEL Technologies 171
Actel 106-107
Advanced Micro Devices 10-11
Advin Systems 170
Aldec 148
Altera 22-23
AMP 92-93
Analog Devices 37, 39, 41, 43
Ancot 8
Annabooks 170
Apex Microtechnology 29
Applied Microsystem 96-97
Atmel 53
AT&T 12-13*, 19*
Avasem 88-89
AVX 75

B

B&C Microsystems 171
Best Western 112

C

CalComp 90
Capital Equipment Corp. 150
Cascade Microtech 46
Cirrus Logic 111
Comdisco 105
Comlinear 142-143
Cybernetic Micro Systems 14
Cypress Semiconductor ..... Cover IV

D

Data I/O ..... 170, Cover II
Data Translation 70
Direct Imaging 112A-B*
Doctor Design 169

E

Elcon Products International 172
Emulation Technology 171
Equipto Electronics 170

F

Figaro 172
John Fluke Mfg. 124, 172
Fujitsu Microelectronics 85

G

GE Plastics 67-69-169
GenRad 137
Gnostech 172

H

Hewlett-Packard Co. 1, 9, 132

I

IBM 30
Integrated Device Technology 35
Intergraph 86
Intusoft 171
iTOI 169

L

Lambda Electronics 80A-80J*
Lattice Semiconductor 58
Little Fuse 171

M

Marubeni 157
Megatel Computer 84

Mentor Graphics 126
Metalink 172
MF Electronics 18
Micron Technology 162
MicroSim 168
MicroSoft 173
Microwave Logic 134
Mini-Circuits Laboratory, a Div. of Scientific Components Corp. ..... 15, 20-21, 118-119, Cover III
Motorola Computer 78-79
Motorola Semiconductor 128-129

N

National Golf Assoc. 66
National Instruments 24
National Semiconductor 64, 144
NCR Semiconductor 115
J.M. Ney 124
Nohau 110
Number One Systems 171

O

OKI Semiconductor 122-123
Omation 169

P

P-CAD 160A-160B
Pacific Hybrid 152
Philips Test & Measurement 19**, 55**
Pico Electronics, Inc. 116, 153
Planar 170
Power-One 139
Praetzger 159

R

Racal-Redac 121
Raytheon 62-63
RC Electronics 8
Rogers Corp. 170
Rolyn Optics 171

S

Samsung Electronics 12-13**
Samsung Semiconductor 154-155*
Seagate Technology 2-3
Siemnes AG 82-83
Siemens Components 50-51
Silicon Systems 26-27
Silicon Valley 78-79
Solder Absorbing Technology 169
Sony 164
Stanford Research 151

T

T-Cubed Systems 170
Tektronix 16-17, 95
Teltone 169
Texas Instruments 32-33
3M 125
Toshiba 56-57
TransEra 113
Trompeter 172

U

UTMC 55*

V

Vicor 73
Vitesse Semiconductor 44-45

W

White Technology 165
Wintek 171

X

Xilink 6-7

Z

Z-World Engineering 169

* Domestic Advertiser Only
** International Advertiser Only

The advertisers index is prepared as an extra service. Electronic Design does not assume any liability for omissions or errors.

ELECTRONIC DESIGN

Chairman and CEO: Sal F. Marino
President and COO: Daniel J. Ramella
President, Electronics Group: James D. Atherton

Advertising Sales Staff

Publisher: Paul C. Mazzacano
Hasbrouck Heights, NJ; (201) 393-6060
San Jose, CA; (408) 441-0550

National Sales Manager: Andrew M. Dellins
San Jose, CA; (408) 441-0550

General Manager, European Operations: John Allen
Four Seasons House
102B Woodstock Rd., Witney, Oxford OX8 6DY England
Phone: 0993-778-077 FAX: 44-993-778-246

Hasbrouck Heights: Judith L. Miller, Robert Zaremba
Sales Support Supervisor: Betsy Tapp
611 Route # 46 West, Hasbrouck Heights, NJ 07604;
Phone: (201) 393-6060 TWX: 710-990-5071

Boston: Ric Wasley
400 Fifth Ave., Waltham, MA 02154;
Phone: (617) 890-0891 FAX: (617) 890-6131

Colorado: Lou Demeter (408) 441-0550

Chicago/Midwest: Russell Gerches
Sales Assistant: Susan Johnson
2 Illinois Center Bldg., Suite 1300
Chicago, IL 60601; (312) 861-0880
FAX: (312) 861-0874

Arizona: James Theriault (408) 441-0550

Los Angeles/Orange County/San Diego: Ian Hill
Sales Coordinator: Debi Neal
16255 Ventura Blvd., Suite 300
Encino, CA 91436; (818) 990-9000
FAX: (818) 905-1206

Pacific Northwest: Bill Giller (408) 441-0550

San Jose:
Lou Demeter (408) 441-0550
Bill Giller (408) 441-0550
James Theriault (408) 441-0550
Sales Administrator: Amber Hancock
2025 Gateway Pl., Suite 354
San Jose, CA 95110; (408) 441-0550
FAX: (408) 441-6052 or (408) 441-7336

Texas/Southeast: Bill Yarborough
12201 Merrit Dr., Suite 220, Dallas, TX 75251;
(214) 661-5576 FAX: (214) 661-5573

Direct Connection Ad & DAC Sales Representative:
Jeanie Griffin (201) 393-6080

Canada: Tony Chisholm
Action Communications
135 Spy Court, Markham, Ontario L3R 5H6
Phone: 416-477-3222 FAX: 416-477-4320

Netherlands: W.J.M. Sanders, S.I.P.A.S.
Oosterpark 6-P.O. Box 25
1483 DeRyp, Holland Phone: 02997-1303
Telex: 13039 SIPAS NL Telefax: (02997)-1500

France, Belgium, Spain: Claude Bril
IMS Paris, c/o IDG Communications France
Cedex 65, 92051 Paris la Defense—France
Phone: 33 149 047 900 FAX: 33 149 047 878

Germany, Austria, Switzerland: Friedrich Anacker
InterMedia Partners GmbH
Katernberger Strasse 247, 5600 Wuppertal 1
West Germany Phone: 02-02-711-091/92

Hong Kong: Tom Gorman, China Consultant Intl.
Guardian Hse, Ste 905
32 Oi Kwan Road, Happy Valley, Hong Kong
Phone: 852 833 2181 FAX: 852 834 5620

Israel: Igal Elan, Elan Marketing Group
22 Daphna St., Tel Aviv, Israel
Phone: 972-3-6952967 FAX: 972-3-268020
Toll Free in Israel only: 177-022-1331

Italy: Cesare Casiraghi, Casiraghi Cesare, S.A.S.
Via del Colli 1, 22070 Guanzate, Como, Italy
Phone: 39 31 976 377 FAX: 39 31 976 382

Japan: Hirokazu Morita, Japan Advertising Communications
New Gunza Buiding 3-13
Gunza 7-chome, Chuo-Ku, Tokyo 104 Japan
Phone: 011-81-3-3571-8748 FAX: 011-81-3-511-8710

Korea: Young Sang Jo, Business Communications Inc.
K.P.O. Box 1916, Midopa Building 146,
Dangju-Dong, Chongo-Ku, Seoul, Korea
Phone: 011-82-2-739-7840 FAX: 011-82-2-732-3662

Singapore, Australia, New Zealand: Omer Soker
Media Development Ltd., 17B Washington Plaza
230 Wanchai Road, Hong Kong
Phone: 834-5978 FAX: 893-9411

Taiwan: Tomung Lai, United Pacific International
No. 311 Nanking E. Rd., Sec. 3
Taipei, Taiwan R.O.C. Phone: 011-886-27-150-751
FAX: 011-886-27-169-493

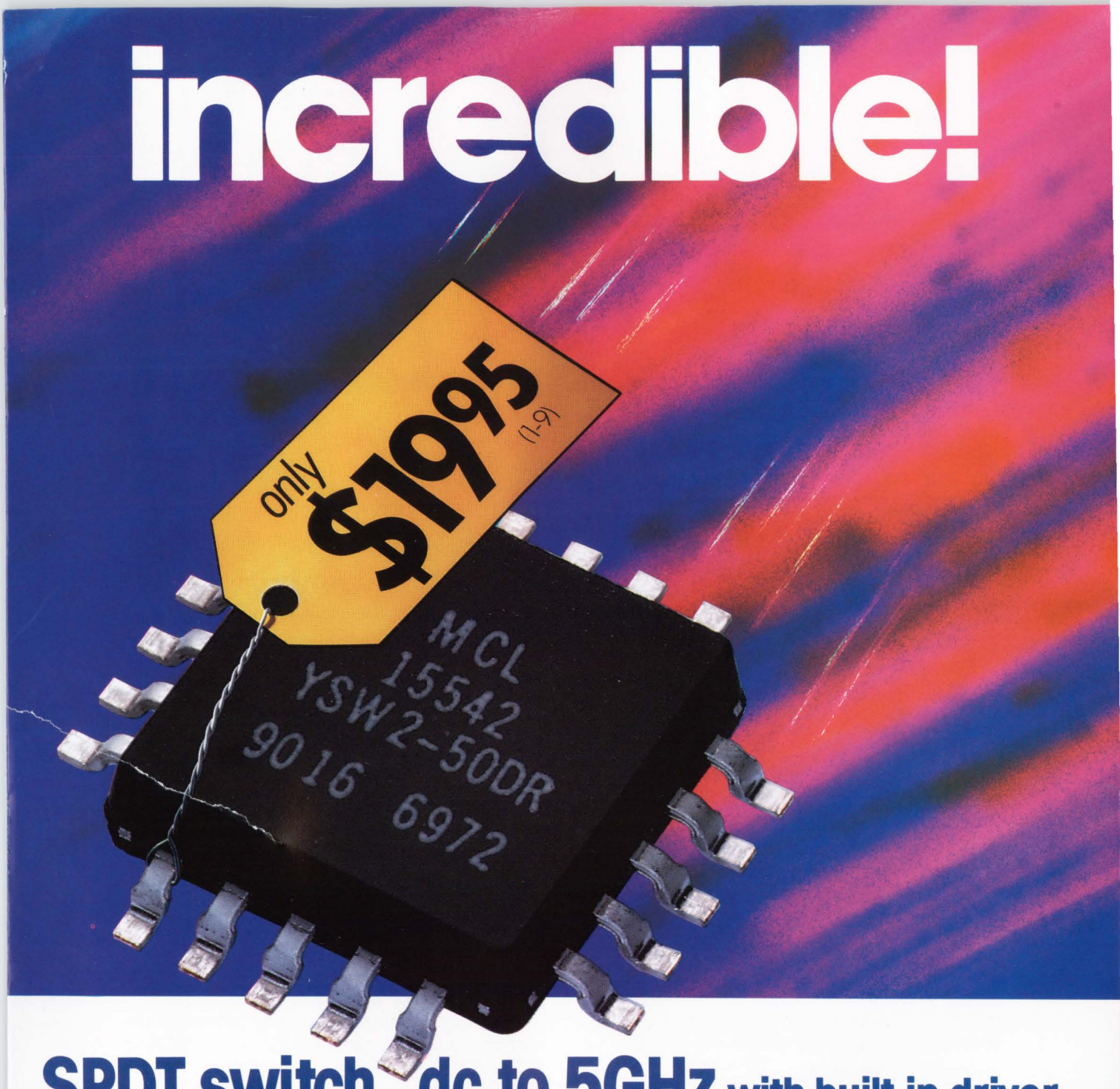
United Kingdom: John Maycock
Huttons Buildings, 146 West St.
Sheffield, England S1 4ES Phone: 742-759186

If you had to choose only
one technical magazine...
Your choice would be
ELECTRONIC DESIGN.

...FIRST with new technology
...FIRST with Ideas for Design
...FIRST with new products
...FIRST on your must-read list

ELECTRONIC DESIGN . . .
Written by engineers for engineers, worldwide

incredible!



SPDT switch dc to 5GHz with built-in driver

Truly incredible... a superfast 3nsec GaAs SPDT reflective switch with a built-in driver for only $19.95. So why bother designing and building a driver interface to further complicate your subsystem and take added space when you can specify Mini-Circuits' YSW-2-50DR?

Check the outstanding performance specs of the rugged device, housed in a tiny plastic case, over a -55° to +85° C span. Unit-to-unit repeatability for insertion loss is 3-sigma guaranteed, which means less than 15 of a 10,000-unit production run will come close to the spec limit. Available for immediate delivery in tape-and-reel format for automatic placement equipment.

New... ZYSW-2-50DR Connector Version (SMA) available, $59.95 (1-9)

SPECIFICATIONS

YSW-2-50DR / ZYSW-2-50DR	dc-500MHz	500-2000MHz	2000-5000MHz
Insertion loss, typ (dB)	0.9	1.3	1.4
Isolation, typ(dB)*	50	40	28
1dB compression, typ (dBm @ in port)	20	20	24
RF input, max dBm (no damage)	22	22	26
VSWR (on), typ		1.4	
Video breakthrough to RF, typ (mV p-p)		30	
Rise/Fall time, max (nsec)		3.0	

PRICE YSW-2-50DR $19.95 (1-9)
ZYSW-2-50DR $59.95 (1-9)

*typ isolation at 5MHz is 80dB and decreases 5dB/octave from 5-1000 MHz

finding new ways...
setting higher standards

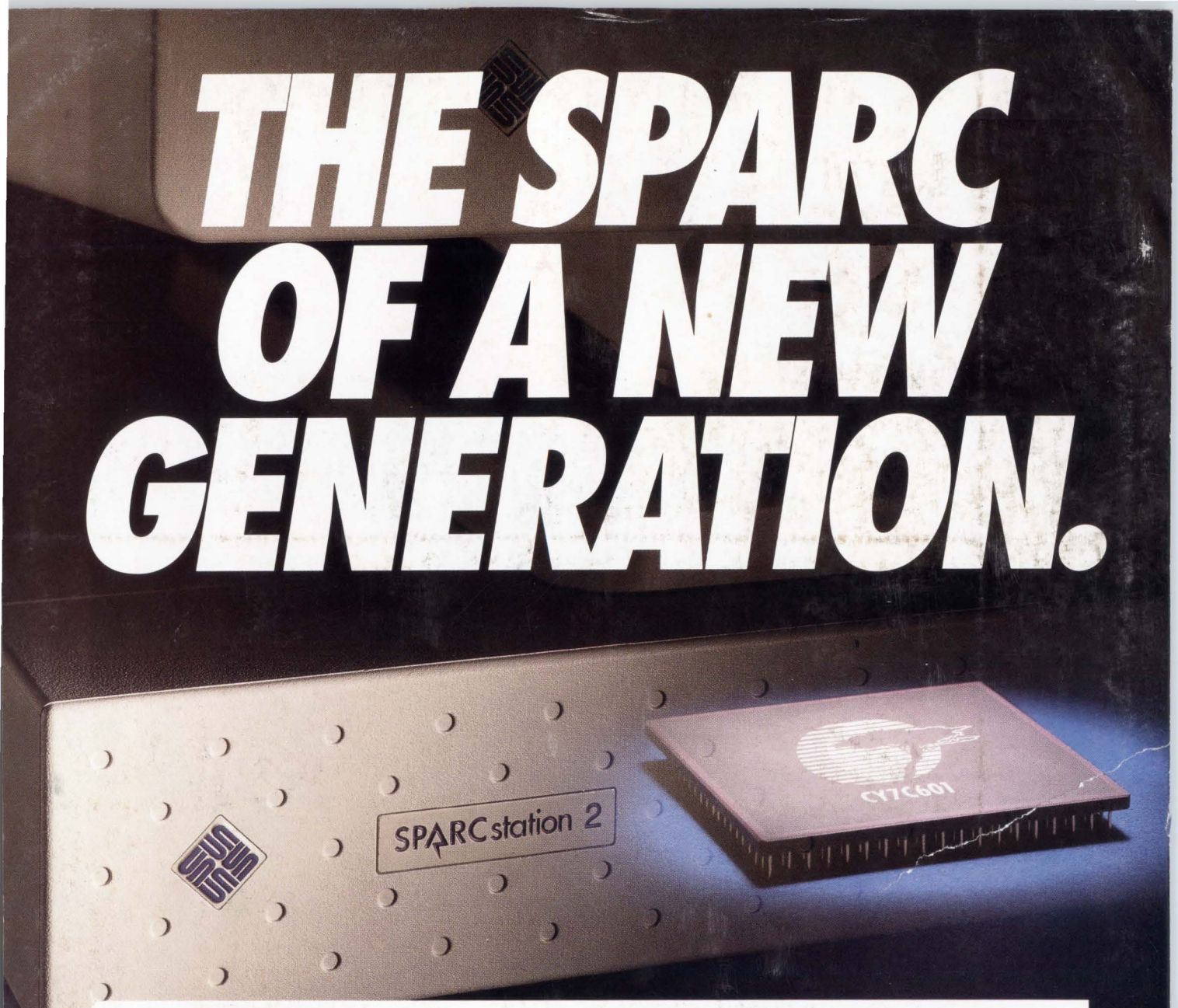
Mini-Circuits WE ACCEPT AMERICAN EXPRESS

CIRCLE 164

P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 Telexes: 6852844 or 620156

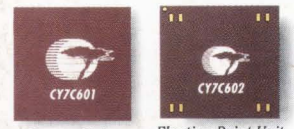
F141 REV.A

THE SPARC OF A NEW GENERATION.



A new generation of performance.

The new SPARCstation™2 from Sun Microsystems delivers almost twice the CPU performance of previous generations – the highest performance in its class.



Integer Unit

Floating Point Unit

Cache Storage Units

Cache Controller and Memory Management Unit

The complete SPARC chipset, designed by our ROSS Technology subsidiary, is now available for high-volume applications.

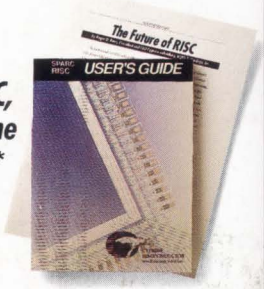
The reason for this blazing speed: The highest-performance CMOS SPARC® available. The CY7C601, 32-bit SPARC microprocessor and CY7C157 16K x 16 Cache Storage Units from Cypress Semiconductor. Cypress 0.8 micron CMOS gives the CY7C601 SPARC RISC microprocessor 40 MHz clock rates and a sustained throughput of 29 MIPS.

Next generation compatibility.

Because they're SPARC chips, they're completely compatible with over 2100 SPARCware™ products. They offer true scalability into a wide spectrum of applications. And a growth path for future high-performance products.

Get this level of performance, potential, and compatibility for your next-generation products.

The Cypress SPARC.



For the whole story on RISC, call the Cypress Hotline at 1-800-952-6300.* Ask for dept. C3M.

CYPRESS SEMICONDUCTOR

*1(800)387-7599 in Canada. (32)2 672-2220 in Europe. ©1990 Cypress Semiconductor, 3901 North First Street, San Jose, CA 95134. Phone: (408) 943-2600. Telex: 821032 CYPRESS SNJ UD, TWX: 910-997-0753. SPARC is a registered trademark of SPARC International, Inc. SPARCstation and SPARCware are trademarks of SPARC International, Inc., licenced exclusively to Sun Microsystems, Inc. Products bearing the SPARC trademark are based on an architecture developed by Sun Microsystems, Inc.