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New Transceivers Use Small 0.1µF Capacitors

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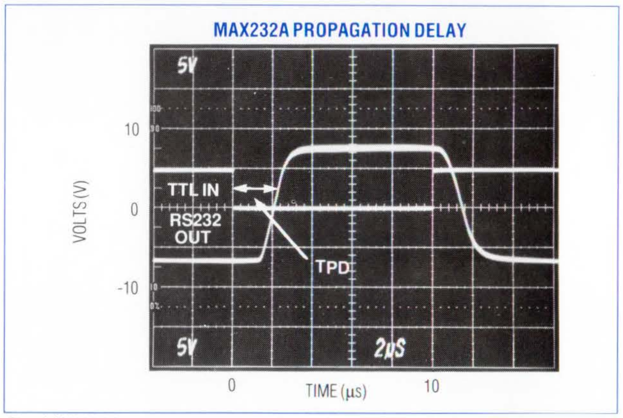

The MAX232A improves propagation delay and symmetry.

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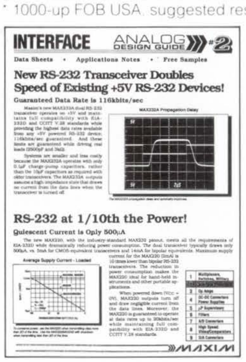
MAX232A	116	0.1	10	No	**Guaranteed 116kbits/sec Data Rate**	$2.65
MAX233A	116	none	10	No	**MAX232A with no External Capacitors**	$4.21
MAX242	116	0.1	10	Yes	**MAX222 + Receivers Active in Shutdown**	$2.65
MAX243	116	0.1	10	No	**Simplifies Cabling–No Jumpers**	$2.65

* 1000-up FOB USA, suggested resale



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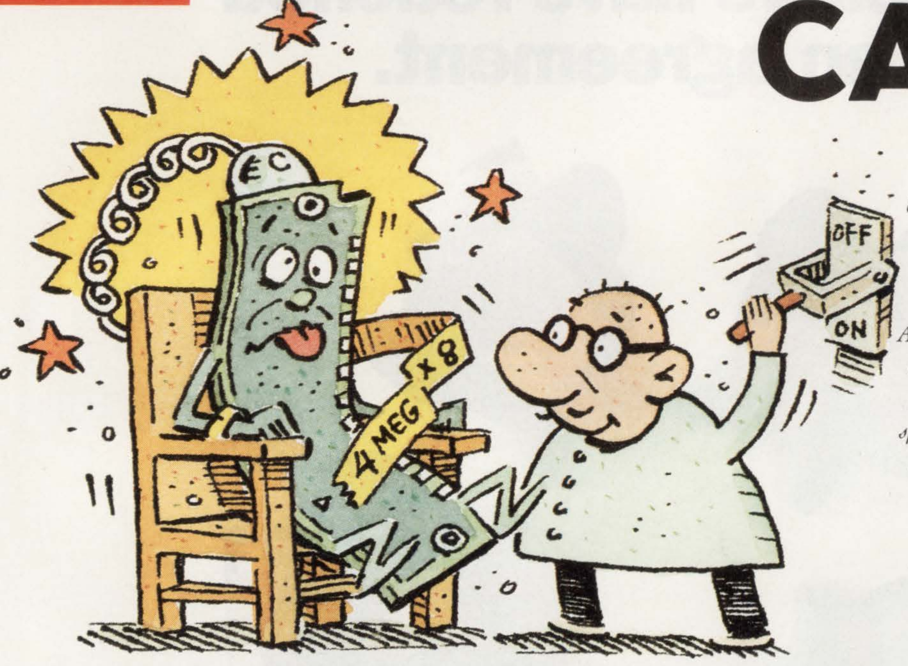

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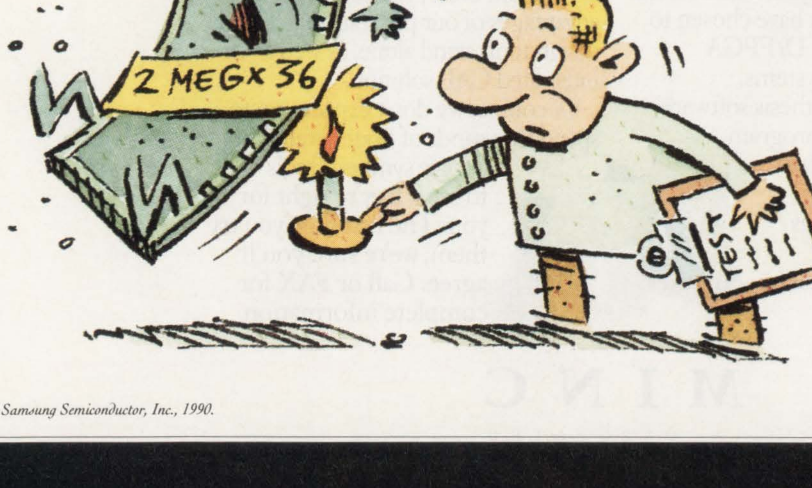

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AUGUST 22, 1991 VOL. 39, NO. 16

ELECTRONIC DESIGN

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- First details on a new multimedia IC
- Special Section: Designing PC systems
- What's new at Buscon/East
- Special Section: Computer Bus/Board Designer's Guide
- A preview of the European Solid-State Circuits Conference
- Reducing metastability in CMOS circuits
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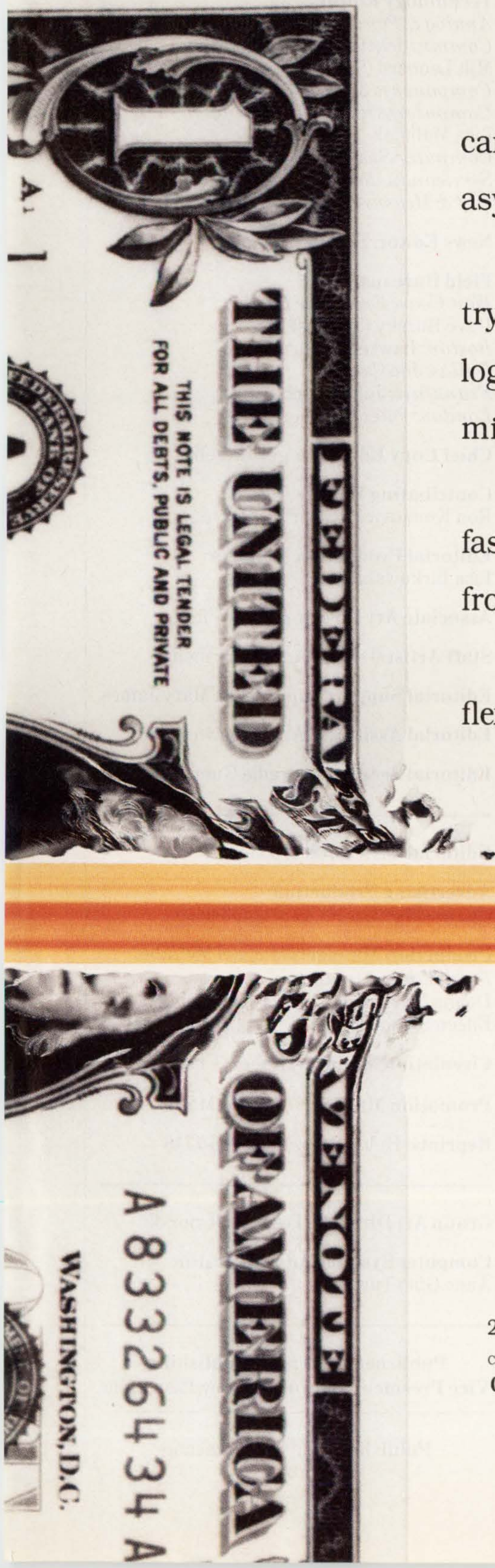

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MACH 120*	1200	48	15ns	50 MHz	68	MASC 120
MACH 220*	2400	96	15ns	50 MHz	68	MASC 220
MACH 130	1800	64	15ns	50 MHz	84	MASC 130
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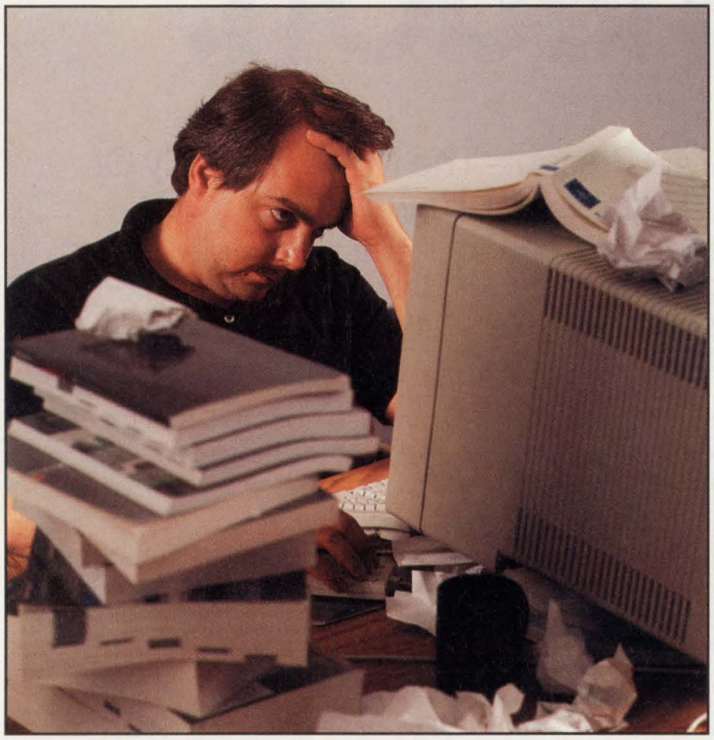

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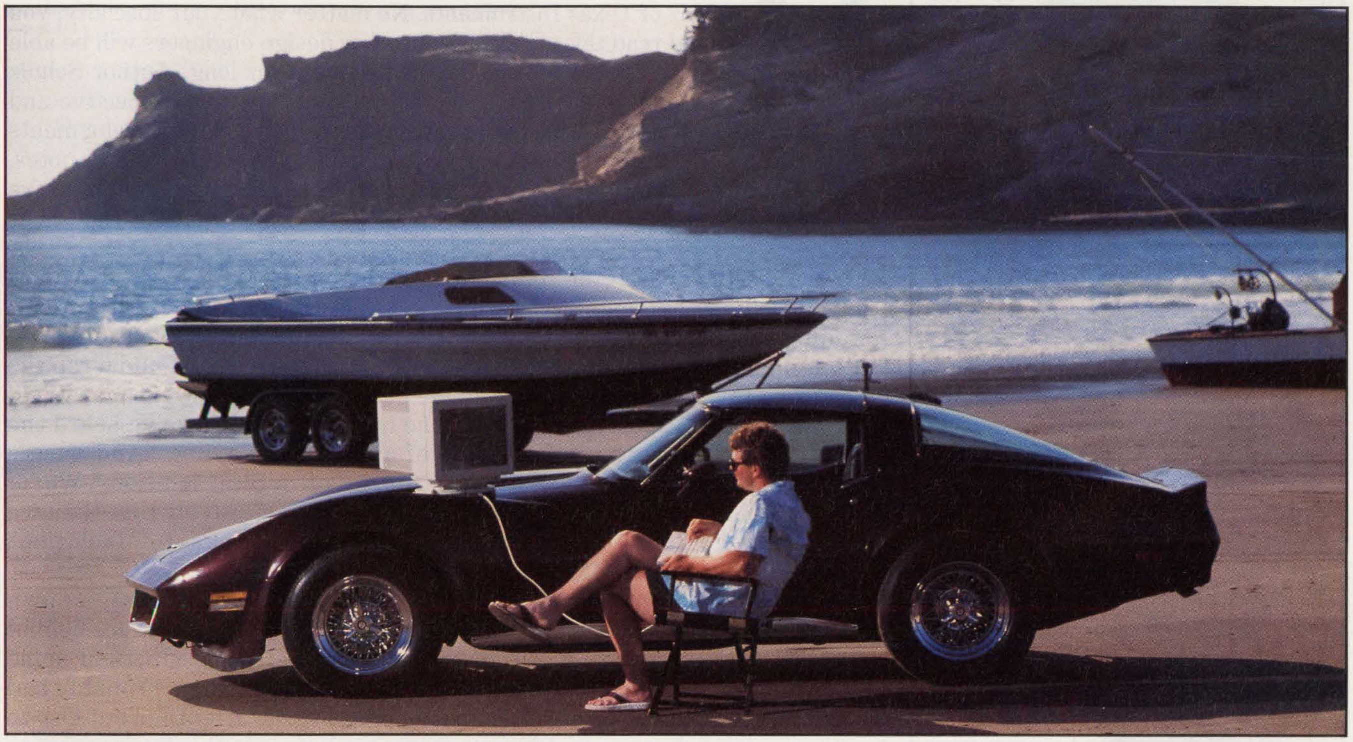

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CIRCLE 158 FOR U.S. RESPONSE CIRCLE 159 FOR RESPONSE OUTSIDE THE U.S.

EDITORIAL

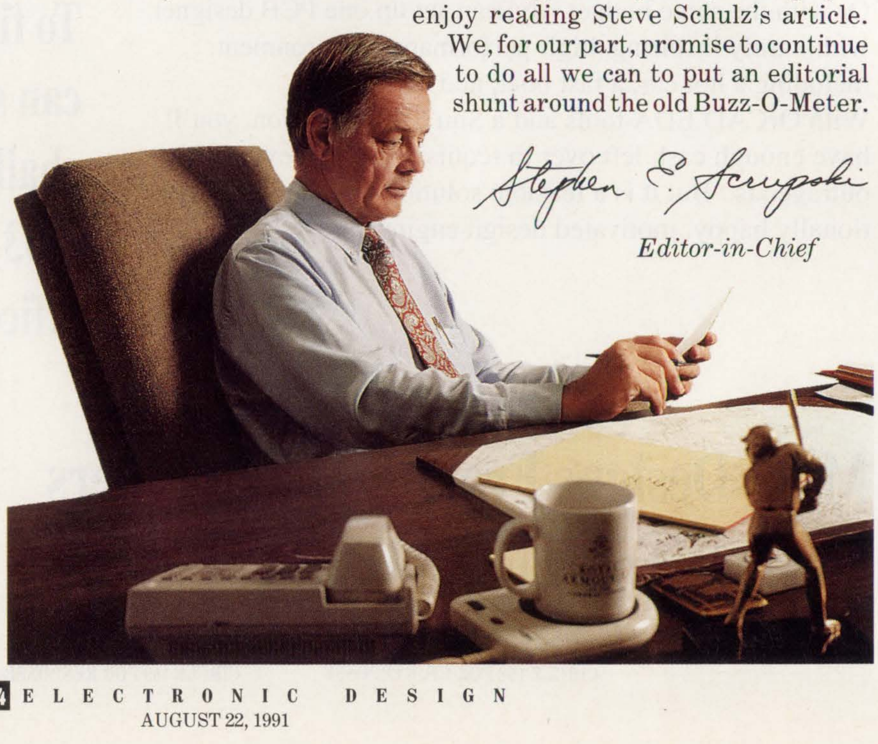
Reducing The Buzz-O-Meter Reading

One of this issue's highlights is the informative and interesting article on page 71, "Frameworks: Debunking the Myths," by Steven E. Schulz of Texas Instruments. No matter what your specialty, you should read this article, because few design engineers will be able to exist totally outside a CAE design environment for long. Author Schulz discusses the industry's latest buzzwords, putting them in perspective and cutting through the marketing hype that surrounds many of the developments in computer-aided engineering tools today. In one section of the article he notes, "If you've glanced at any industry magazine in the last two years, you're probably aware that OODB ranks very high on the Buzz-O-Meter, right next to C++."

Schulz's Buzz-O-Meter comment is right on the money. However, if anyone thinks that engineers reading industry magazines have it difficult wading through a morass of buzzwords, he should know that editors have it tougher—we deal every day with words or phrases that would wrap the needle on the Buzz-O-Meter around the peg at least a couple of times. We'd rather not think about, for example, the number of times we've heard the quiet, confident, authoritative voice of a marketer saying, "And what's more, this development (you name it) represents a total solution." We, of course, must indicate our understanding by nodding gravely (but then we sometimes must decide how to handle another competitor's "total solution" we heard about yesterday).

Still, doesn't every profession have its own colorful language, its own lingo? What's really important is the ability to grasp the significance behind those words and phrases. Although they may be the products of some marketer's fertile imagination, each one, when it was coined, probably had some technical basis. It was intended not only to grab attention, but also to convey some information. After all, many marketers in this business were engineers first. The problem, however, arises when a buzzword takes on a life of its own. The original technical basis is forgotten as vendor after vendor broaden the scope of its meaning—without broadening the scope of his product.

This may be an excellent way to cut a product's time-to-market to zero, but it's clearly not a contribution to technology. In any case, we hope you enjoy reading Steve Schulz's article. We, for our part, promise to continue to do all we can to put an editorial shunt around the old Buzz-O-Meter.



Stephen E. Scrupski

Editor-in-Chief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LRMS-2L	800-1000	DC-200	+3	6.6	24	6.95
LRMS-1	0.5-500	DC-500	+7	6.4	45	6.25
LRMS-1W	2.0-750	DC-750	+7	5.8	45	6.75
LRMS-2	5-1000	DC-1000	+7	6.8	38	6.95
LRMS-2D	5-1000	DC-1000	+7	6.8	40	7.25
LRMS-2U	10-1000	10-1000	+7	6.5	46	11.45
LRMS-5	5-1500	DC-1000	+7	6.0	41	13.95
LRMS-11A	1400-1900	40-500	+7	7.0	25	16.95
LRMS-1LH	2.0-500	DC-500	+10	5.8	47	7.95
LRMS-2LH	5-1000	DC-1000	+10	6.6	40	8.95
LRMS-5LH	10-1500	DC-900	+10	5.4	38	14.95
LRMS-1MH	2.0-500	DC-500	+13	5.7	44	8.95
LRMS-2MH	5-1000	DC-1000	+13	6.6	44	9.95
LRMS-5MH	10-1500	DC-900	+13	5.8	46	15.95
LRMS-1H	2.0-500	DC-500	+17	6.3	44	10.95
LRMS-2H	5-1000	DC-900	+17	7.2	36	11.95
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TECHNOLOGY IS KEY TO COMPETITIVENESS

JOHN NOVELLINO
TEST & MEASUREMENT

The competitiveness of U.S. industry is like that old cliché about the weather: Everybody talks about it, but nobody does anything about it. Hopefully, this similarity will end now that industry has some well thought out findings and recommendations from the Council on Competitiveness. Interestingly, in a two-year study of U.S. industrial competitiveness, the Council chose to focus on technology. The electronics industry didn't fare well in the study. Nor did a category critical to our industry–engineering and production technologies.

The Council was founded in 1986 as a nonprofit, nonpartisan organization of chief executives from business, higher education, and organized labor. The group released its conclusions this spring in a report entitled, *Gaining New Ground: Technology Priorities for America's Future.* Council Senior Associate David W. Cheney recently discussed the findings and recommendations in his keynote address at the Test Engineering Conference in Atlanta.

Cheney, who was the assistant director for the report, offered three basic conclusions. First, several generic technologies form the basis of the defense and civilian sectors of the economy. Included are electronic components in general and IC production and test equipment. Second, the U.S. is losing ground in these technologies. Finally, although the reasons for our decline are complex, they can be pinpointed in distinct patterns of strength and weakness.

The two areas of greatest concern to our industry are electronic components and engineering and production technologies. In the components arena, which includes hardware used in various types of electronic equipment, the U.S. is doing fairly poorly, said Cheney. The report breaks engineering and production into three subcategories. The first includes such technologies as scientific instruments, CAE, and systems engineering. The second is what the Council called commercialization and production systems. Cheney noted that these areas are essential to our success but, unfortunately, are among our greatest weaknesses. The third subcategory is process equipment, including robotics and IC fabrication and test equipment. The U.S. is also shaky in many of these manufacturing technologies, he said.

A number of factors are to blame, including government funding that stresses basic research over support for "precompetitive applied R&D," said Cheney. Also, we have underemphasized manufacturing. "Our best engineers have often gone into product rather than process engineering," he said. "Much of our weakness in electronic components is due to weaknesses in low-cost, high-quality manufacturing."

The remedies recommended in the report assign supporting roles to government and the universities. Government must boost precompetitive research and create an economic and regulatory environment that encourages investment in technology. The universities must perform some of the industry's fundamental research requirements and produce graduates who meet industry's needs. Needless to say, though, the primary responsibility falls on the shoulders of industry.

A key recommendation for U.S. industry is cooperative relationships, particularly between suppliers and final product manufacturers. "We believe that U.S. industry needs to develop new patterns of cooperation in precompetitive technology while maintaining vigorous competition in product development," says Cheney. "U.S. industry should establish more effective technology networks to cooperate in technology. Industry organizations have focused on regulatory issues and lobbying. In general, they have not been very active in technology."

The Council has proposed some good ideas. It's time to stop talking about regaining our competitive edge and take some action that will restore it.

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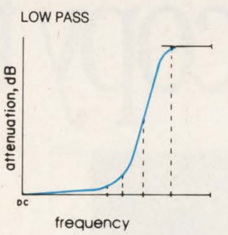
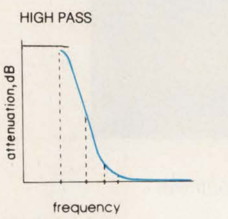


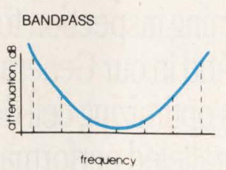
low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	STOP BAND, MHz (loss>40dB) Max.	Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45



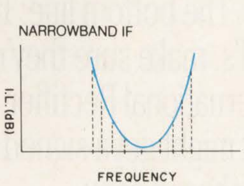
high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	(loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95



bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	Max. F4	(loss > 20 dB) Min. F5	Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95



narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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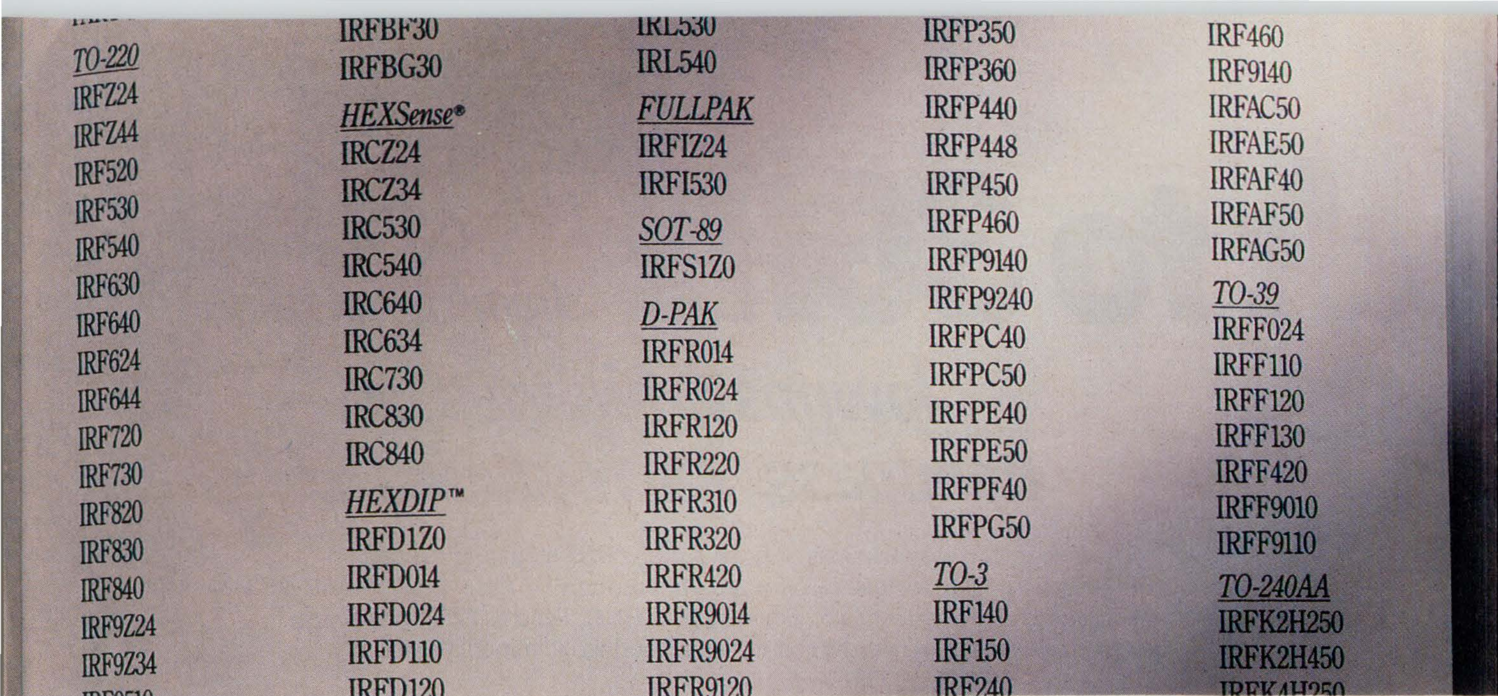
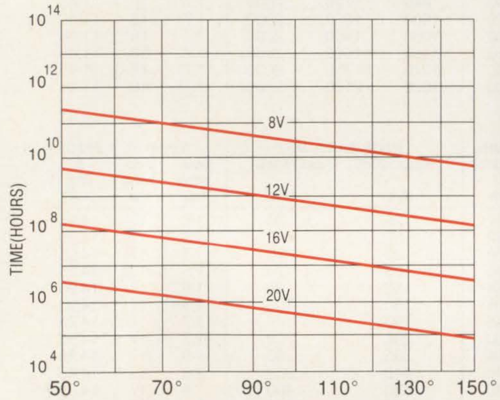
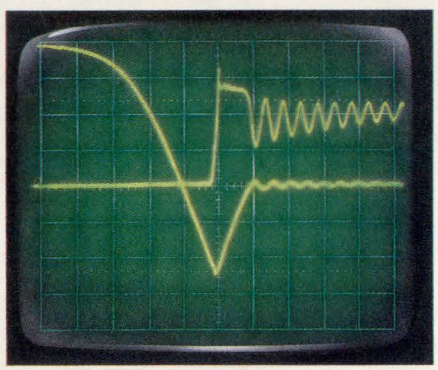


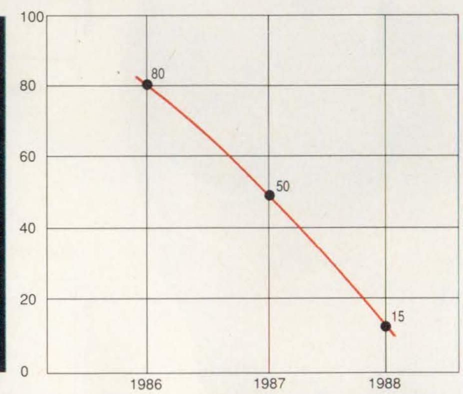
They can copy these numbers. But they can't copy these.



Gate stress TO-220 time to failure



HEXFET IRF530 under avalanche



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CIRCLE 132 FOR U.S. RESPONSE **CIRCLE 133 FOR RESPONSE OUTSIDE THE U.S.**

Electronic Mirror Reflects Laser Light

A semiconductor device fabricated by strained-layer epitaxy can receive and reflect light waves generated by a laser. The unusual property of the device, called a reflectance modulator, allows the construction of optical reflectors that operate under electrical control and reflect light at a wavelength of 1060 nm—the wavelength of most low-cost industrial lasers. Developed at Sandia National Laboratories, Albuquerque, N.M., the strained-layer-superlattice device could find its way into the high-power transmit/receive units of phased-array and synthetic-aperture radars. The modulator can impress the microwave signal information onto a laser signal so that the data can be processed at a common, remote location. Prior to this development, reflectance modulators had been limited to operating at about 870 nm (gallium-arsenide wavelengths). However, by straining the lattice structures and using lattice-mismatched quantum wells in a stable structure, the wavelength of the light reflected can increase to 1060 nm. The superlattice layers formed by molecular-beam epitaxy consist of alternating layers of indium-gallium-arsenide and aluminum-gallium-arsenide. That region forms the quantum-well resonator, and is then surrounded by thicker layers of InGaAs and GaAs that form the mirrors for the quantum-well resonators. Contact Ian Fritz, (505) 844-7789. *DB*

Klystron Delivers 40 kW For UHF Transmitters

An air-cooled depressed-collector klystron puts out 40 kW for UHF transmitters. Its developers at Philips Semiconductors, Eindhoven, The Netherlands, claim that it's the highest power yet for an air-cooled tube. The YK1283 has a frequency range from 470 MHz to 810 MHz, features high efficiency—its figure of merit is up to 130%—and has high reliability and long life. The forced-air-cooled klystron, of metal-ceramic construction, focuses electromagnetically. Four continuously tunable external cavities are fitted with digital frequency indicators. Aside from the depressed collector, the YK1283 has a high-stability dispenser-type cathode and a nonintercepting annular beam-control electrode for low-voltage beam modulation. *JG*

ISDN Spreads Through The Golden State

Growing interest in Integrated Services Digital Network (ISDN) services in California is prompting Pacific Bell, a subsidiary of the Pacific Telesis Group, to step up its deployment of the technology, which it offers as Centrex IS (Integrated Systems). The company cites two reasons for the increased interest. First, business organizations are becoming more aware of the benefits of ISDN for desk-to-desk networking, file transfer, remote LAN access, personal-computer LAN bridging, Group IV facsimile, and customer-service call management. The second reason is new ISDN-based applications, such as Pacific Bell's RealtyLink, are finding homes in a variety of new markets among business and residential customers, and manufacturers of central-office switches, ISDN terminal equipment, and computer-software developers. The multichannel RealtyLink connects all participants in a transaction for exchange of voice, data, and images. *ML*

European Business Radio Arrives

The Commission of the European Community has officially designated frequencies from 880 to 890 MHz, and 933 to 935 MHz, for Digital Short Range Radio (DSRR). The announcement heralds the arrival of business citizens-band radio in Europe. The frequencies will be available, without license, for point-to-point communications over distances up to about 6 km maximum, depending on antenna height. DSSR uses a trunking scheme, in which a pair of handheld transceivers can grab an available channel for the transceivers' exclusive use during a conversation to ensure security. DSRR radios will be available soon from Motorola-Storno and Philips. *PF*

CAN Hits The Road In Mercedes-Benz Autos

The long-awaited CAN (controller area network) protocol for networked electronic controllers in road vehicles will first appear in the Mercedes-Benz S-Class autos now in production. CAN chips are currently available from several major semiconductor manufacturers. As a transmitter, the chip sends messages over the network data bus in a standard format specified by the CAN protocol. As a receiver, it determines the source, content, validity, and priority of messages on the bus, and routes information to the host processor as needed. The International Standards Organization is planning to introduce CAN as the sole standard for high-speed control systems. In the U.S., the J1939 Control and Communications Network Subcommittee of the Society of Automotive Engineers adopted CAN as the architecture for its proposed recommended practice. *ML*

IBM Takes Aim At The Big Picture

Visualization chores call for crunching a mountain of data. Developed in just two years, IBM Corp.'s Power Visualization System is essentially a supercomputer dedicated to turning data into 3D images. At the system's core is a server that runs up to 32 Intel i860 microprocessors in parallel. So equipped, the system can calculate 2.5 Gflops, outrunning minisupercomputers and high-end scientific workstations. It supports up to 1 Gbyte of shared memory. Storage in disk arrays handles up to 170 Gbytes. The High-Performance Parallel Interface, which affords connections to mainframe and supercomputers, shuttles 100 Mbytes/s. The system, available in late November, ranges in price from $600,000 to $2 million. A scaled-down version of the visualization software for IBM's RISC System 6000 workstations will be available in late December for $5,900. *SVT*

Voice System Recognizes 100 Kwords

A presentation by Tokyo-based Fujitsu Ltd. at this year's ICASSP in Toronto, Canada, revealed a major breakthrough in voice-recognition technology. Given about 200 training words, a Fujitsu system can teach itself to distinguish between 100,000 words. Prior systems used in Japanese factories to recognize product names could only recognize about 1000 words. Fujitsu's approach analyzes the sound segments of a word, instead of treating the whole word as a unit. Operating on a base of 200 words, the system builds a network of sound discriminations fine enough to identify 100,000 words. A second major advance is the speech at which the system can cross-reference the speech data and find a word in its vocabulary. That speed is 50 times faster than conventional voice-recognition systems. For more information, contact Fujitsu News Center, Michael Solomon Assoc., 400 Madison Ave., Suite 1501, N.Y., NY 10017. (212) 755-7680. *ML*

U.K. VME-Board Maker Gets NATO Approval

Radstone Technology plc, Towcester, Northampton, United Kingdom, says it has become the first manufacturer of off-the-shelf military-specification VMEbus systems to gain NATO AQAP-13 approval for software-quality standards. The standard of the U.K. Ministry of Defense applies to all software and firmware produced for military applications. Its approval complements AQAP-1 registration relating to hardware. AQAP-13 requires that all aspects of software quality are documented and audited—from software design, through coding, test, and configuration control, to dispatch. Documentation is available to customers worldwide, enabling them to test these quality assurance procedures against their own standards. *PF*

First MNP 10 Data/Fax Modems Ready To Debut

Rockwell International's Digital Communications Div., Newport Beach, Calif., is ready to ship the first MNP 10 data/fax modem chip sets. MNP 10 is the adverse-channel protocol necessary for cellular, portable, and other poor-quality land-line applications. Initial products with MNP 10 enhancements are the RC2324AC data modem for V.42 and V.42bis applications, and the RC9624AC data/fax modem with send and receive, 9600-baud facsimile capabilities. MNP 10 options are also planned for the single-package, low-cost V.32 family, including the RC96AC data/fax modem and the RC144AC data/fax modem operating at 14.4 kbaud (V.32bis). Future dial-up products are also slated to have the MNP 10 option. For more information, call the DCD technical documentation voice-mail system 1-800-854-8099, or 1-800-422-4230 in California. *ML*

Mac Board To Boost FP Math 10X

An add-in board for the Apple Mac II family with the floating-point capacity equivalent to more than ten Mac IIfxs is under development at Division Ltd., Chipping Sodbury, Bristol, U.K. The MacWatt uses an Intel i860 processor to achieve a peak performance of over 40 MIPS, and a Linpack benchmark of 10.7 double-precision MFLOPS, making it useful for computational physics and chemistry, finite-element analysis, and advanced-graphics applications. A video board (the DVHSP) with multiple i860s running in parallel can provide even more computational power (like 35,000 Z-buffered, Goraud-shaded, 100-pixel polygons/s) for high-speed graphics rendering. The MacWatt board has a choice of i860 processor speed (25, 33, or 40 MHz) and carries up to 16 Mbytes of DRAM. A dedicated communications processor carries out high-performance NuBus I/O in parallel with the i860 running the applications program. Software supported includes a dNIX860 run-time kernel and handling-system facilities. Development tools include fully optimizing ANSI C and Fortran 77, a macro assembler and linker, and a symbolic debugger. The board has expansion slots for an additional processor, specialized I/O, and graphics modules, and will come bundled with a library of development tools and a compiler. *PF*

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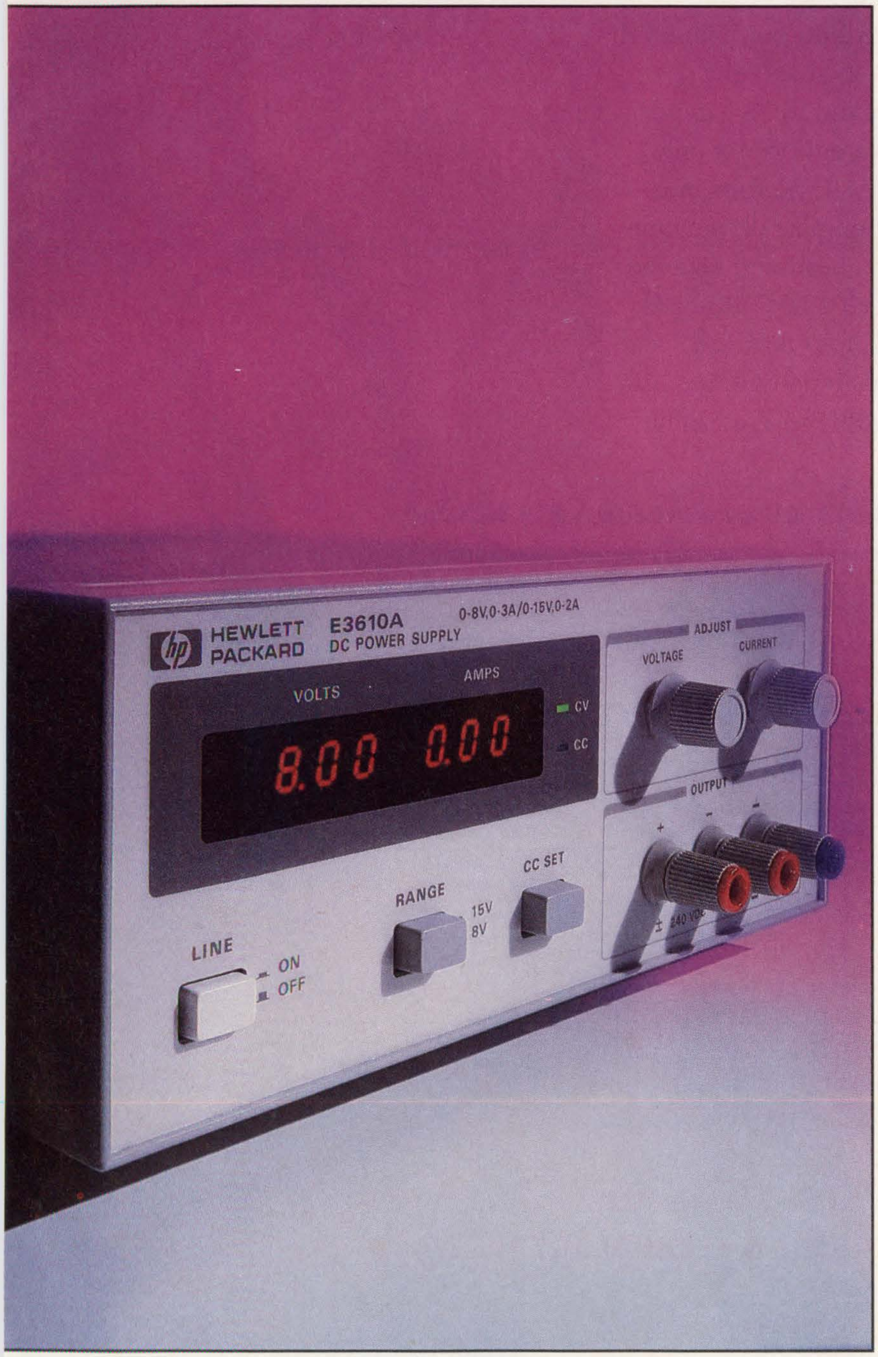

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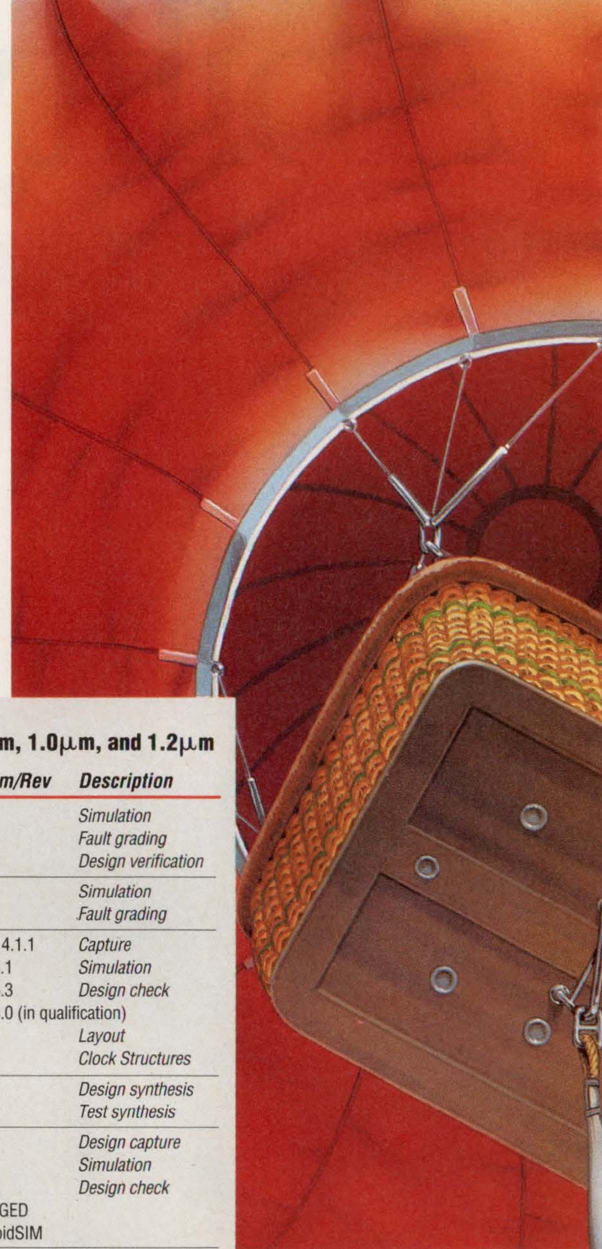

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IKOS		4.0 up	*Simulation* *Fault grading*
Mentor Graphics	HP/Apollo DNx Series HP9000 Sun/SPARC Solbourne	DNIX 5.03, Sun OS 4.1.1 Digital application 6.1 Digital application 6.3 Digital application 8.0 (in qualification) Parade	*Capture* *Simulation* *Design check* *Layout* *Clock Structures*
Synopsys	Sun/SPARC Interface to Mentor, Valid, Viewlogic	Sun OS 4.1.1	*Design synthesis* *Test synthesis*
Valid	Sun/SPARC Sun-3 DECstation 3100 IBM RS6000	Sun OS 4.1.1 GED, ValidSIM, RapidSIM ULTRIX, ValidSIM, GED GED, ValidSIM, RapidSIM	*Design capture* *Simulation* *Design check*
Viewlogic	Sun/SPARC PC386	Sun OS 4.1.1 Workview 4.0 DOS 3.3, Workview 4.0	*Design capture* *Simulation*

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CIRCLE 98 FOR U.S. RESPONSE CIRCLE 99 FOR RESPONSE OUTSIDE THE U.S.

COMPLEMENTARY BICMOS PROCESS WITH EEPROM ATTACKS MIXED-SIGNAL ASICS

A new modular 10-to-22-mask process provides virtually any kind of silicon transistor a mixed-signal ASIC. Developed by Exar Corp., San Jose, Calif., the devices can range from simple n- and p-channel MOS transistors to high-speed vertical npns and pnps, and include EEPROMs with floating gates. Exar, claims that its E^2CBiCMOS process is the first to offer such a full mix of capability. It permits adding nonvolatile memory to high- and low-voltage, and high- and low-speed, analog and digital circuits, and builds p- and n-channel MOS transistors that sustains 40 V in open-drain output stages. Polysilicon resistors can also be laid down atop oxide and pinned out to high voltages.

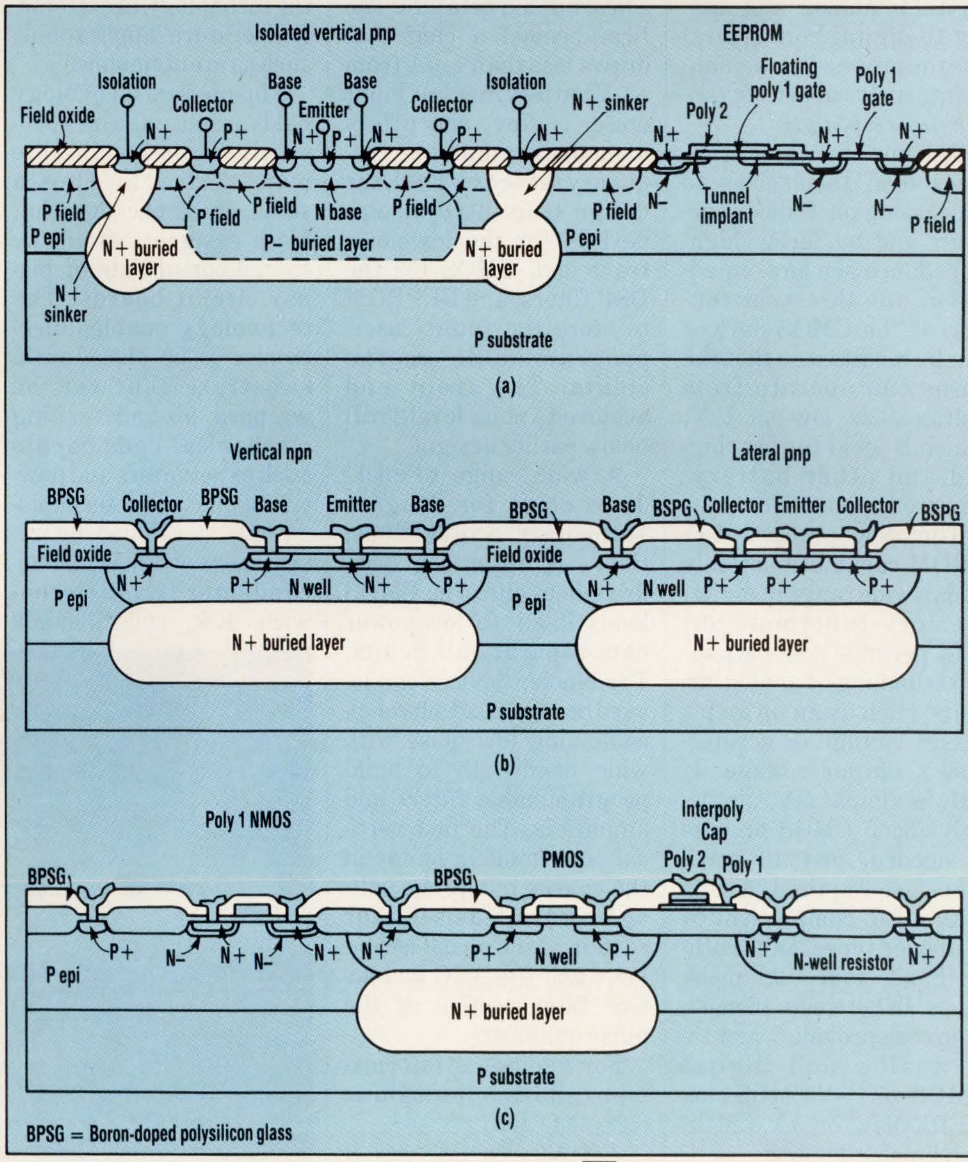
A modular process is ideal for building a wide range of ASICs because whatever the performance or feature needed, it's available. On the other hand, customers don't have to pay for processing they don't need in a modular process. Also, when chips are redesigned for purposes of upgrading or cost cutting, process changes can be made without affecting unaltered circuits. Designers can pick the mix of transistors that will do the job most economically.

Based on 2-μm, double-polysilicon, double-metal, the process can be scaled to operate from 3 to 18 V of maximum supply rails. Exar is now migrating the technology to a 1.6-μm process, to be available by the end of the year.

Modularity is achieved by using common process modules during fabrication and a minimal addition of thermal steps (such as diffusion). Consequently, device characteristics aren't changed when adding (or subtracting) device types. New devices are created with mask and implant steps without adding thermal steps. If additional thermal steps are required, they're performed in a sequence that ensures they won't impact device characteristics.

Designers needing fast complementary circuits for high-speed/wideband analog circuitry can avail themselves of 18-V vertical pnps with f_ts of 700 MHz *(see the figure, a)*. Vertical npns with f_ts of 1.5 GHz are also possible *(see the figure, b)*.

The process can be used to create an op amp or other analog circuit with performance previously unavailable from mixed-signal IC technologies. If you need more bandwidth but still want complementary circuits and can settle for 5-V rails, a finer-geometry vertical pnp sporting an f_t of 1.5 GHz, and a sibling npn with an f_t of 4 GHz, are possible. If you're willing to work with all npns for high-speed circuitry, lateral pnps are available for dc circuits from a non-complimentary version of the process. The bipolar transistors also build good refer-



ences and combine low-input noise with high-current output drive while minimizing silicon area.

For dense logic, analog switches (or multiplexers), switched-capacitor circuits, or low-bias-current op amps, CMOS transistors can be added *(see the figure, c)*. Or, if bipolar-transistor attributes aren't needed, analog circuits with or without logic can use a less-complex (lower-cost) all-CMOS version of the process. In either version, the switch-capacitor circuits (filters and digital-to-analog and analog-to-digital converters) use the process' high-quality interpoly capacitors *(see the figure, b, again)*.

The low-bias current devices lend themselves to processing photodiode currents and buffering high-impedance sensors. In addition, the threshold voltage of the CMOS devices can be modified so that the chips can operate from voltages as low as 1 V, which is ideal for hearing-aid and other battery-powered applications.

The new process' EEPROM capability not only adds a wide range of digital memory functions, but also permits post-packaging trimming of analog circuits, such as an op amp's offset voltage or a reference's output voltage. If only a simple 5-V, single-polysilicon CMOS process is needed, just 10 mask steps are required. A chip with a full complement of all device types, on the other hand, takes 22 mask steps. In between, 16 mask steps can provide 5- and 15-V analog and digital CMOS, or 15-V CMOS plus EEPROMs, or 5-V CMOS and bipolar devices.

The final wafer cost increases only 40% from a basic 16-mask process to a 22-mask version. The increase is 60% from the simple 10-mask process to 22 masks.

The process is presently used in beta sites for internal custom and semicustom designs. Ultimately, it will be the basis of a mixed-signal standard-cell library, which with software tools can be put in the hands of customers.

Starkey Laboratories Inc., Eden Prairie, Minn., which builds hearing aids that go into the ear canal, is a hearing-aid beta site. The firm needed a chip that draws less than 1 mA from a 1-V battery, has low input noise, is tiny, and offers user-programmable frequency response. The Exar design team used bipolar devices for the low-noise front end, CMOS for the DSP filters, and EEPROM to store the filters' user-programmable coefficients. The front end achieved a noise level 25 dB below earlier designs.

A wide range of disk-drive chips for Seagate Technology, Scotts Valley, Calif., represents a disk-drive beta site. The CMOS lends itself to low-power data-separation circuits. The bipolar devices can be used in the read channel, combining low noise with wide bandwidth to build programmable filters and amplifiers. The fast vertical pnps come in handy in the charge pump, the voltage-controlled-oscillator section of the phase-locked loop, and the AGC and active filter section of the pulse qualifier.

For additional information, call Ilhan Refioglu at (408) 434-6400.

FRANK GOODENOUGH

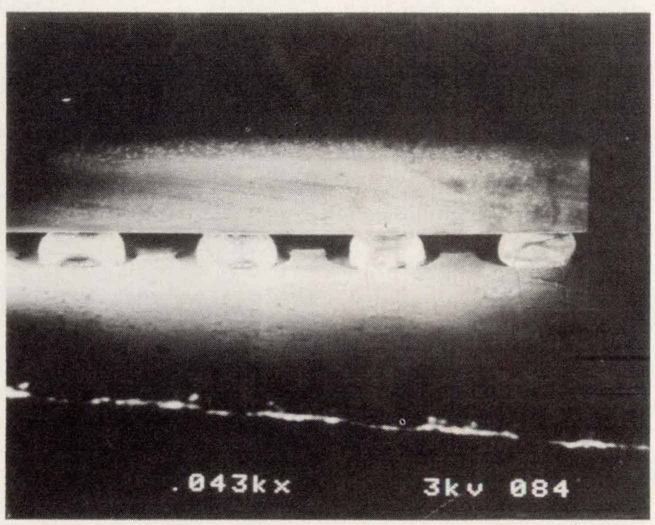
FLIP-ON-FLEX ASIC PACKAGE LIFTS PLANAR-BOARD BURDEN

Cutting down the size and weight of electronic subassemblies is always a key concern for designers. But doing so in an assembly that must withstand temperature extremes is a challenge unto itself. Now, a joint research effort has yielded a technology for mounting flip-chip ASICs on flexible circuitry. Not only that, the qualities inherent in the flex-circuit material lends the technology to extreme-temperature applications, such as in automobiles.

Flip-on-flex technology holds promise as a inexpensively mass-producible means of achieving a small, light package that frees designers from the spatial constraints of planar circuit boards. The technology enables electronics to be placed on a substrate that can be wrapped around limiting mechanical components such as actuators and power supplies. The technology was developed by researchers at Cherry Semiconductor, East Greenwich, R.I., and Sheldahl Inc., Northfield, Minn., and is the subject of a joint paper that promises to be among the highlights of the Surface Mount International Conference, which runs from Aug. 25-29 in San Jose, Calif.

"The goal is to make flip-chip technology available to a greater audience," said Barbara Gibson, an applications engineer in Cherry Semiconductor's Semicustom Group. "We've gotten to the level of SMT, and you can't get much smaller if you're going to retain the traditional concept of a package. So the next logical leap is to get rid of the package."

Flip chips, which are unpackaged silicon die whose bonding pads take solder bumps instead of wire ball bonds, have traditionally been attached to palladium silver or copper traces on ceramic substrates. Ceramic was used because of the 320°C temperatures involved in reflowing the chips' tin-lead solder bumps. Also, the thermal coefficient of expansion (TCE) of the substrate and



silicon had to be similar enough to prevent the mechanical forces produced by temperature cycling from rupturing the solder joints.

That's where Sheldahl's Novaclad, a high-temperature, adhesiveless polyimide-copper laminate, comes in. Because there's no adhesive layer bonding the copper foil and polyimide dielectric, the substrate is more resistant to solvents and moisture. But its key attribute when serving as a flip-chip substrate is its dimensional stability. Also, by carefully matching the TCE of the specific polyimide film with that of the copper film, the result was a very dimensionally stable laminate. The material permits the copper layer's full thermal properties to be used.

In developing the attachment process, the two companies' researchers chose a flip chip with an asymmetric bump pattern, which would be more likely to show joint fatigue *(see the figure)*. As joint fatigue occurs, microfractures appear and get worse with each additional thermal cycle until the interconnection breaks.

The next step for the Sheldahl and Cherry Semiconductor researchers was to define the assembly process. Initially, it was assumed that a solder paste for the flex circuit should have a similar composition to that of the solder bump on the flip chip. The high lead content of this paste drove the reflow profile over 300°C. It was soon found, however, that the solder mask wouldn't tolerate such high temperatures. That prompted the move to a eutectic solder alloy, which reduced the maximum reflow temperature to 225°C, eliminated mask degradation, and still formed visually acceptable solder joints. The eutectic alloy also proved to be compatible with existing surface-mounting procedures.

Test assemblies were built and subjected to a three-part analysis involving electrical, physical, and visual testing. All of the interconnections on each assembly were tested for electrical connectivity, and all showed good connectivity on each joint. No significant problems turned up after examining the samples with a scanning electron microscope.

Still other samples were subjected to shear testing, in which a cantilevered arm applies a known force parallel to the substrate-chip interface. Basically, the idea is to find out how much force it takes to knock the chip off the substrate. The flip chips mounted on Novaclad required an average of 1.6 kg of shear force to dislodge them from the flexible material. The same chip, mounted on a ceramic substrate, took a nominal 1.3-kg force to be removed. Thus, it was shown that the flip-on-flex attachment is stronger than that formed using a high-temperature solder and a ceramic substrate.

Once the process was defined, the researchers set out to automate it. Doing so would provide repeatability for test-sample production as well as prove that the process was viable for future application. The work involved stenciling, automated die placement, and infrared reflow. Thanks to the dimensional stability of the Novaclad substrate, registration of paste proved to be possible on multi-circuit arrays. Component placement was done using standard high-speed optical surface-mounting equipment. After component placement, the panels were fed by conveyor into an IR-reflow oven. A few trial runs produced samples for thermal testing.

One-third of the automated-process samples were coated with a low-stress epoxy encapsulant. All of the assemblies were placed in an air-to-air thermal chamber and cycled between –65 and +150°C, remaining for 20 minutes at each temperature and spending 20 seconds in transit between chambers. The results were that intermittent contacts arose in several of the unencapsulated samples between 50 and 100 thermal cycles. After 200 cycles, 75% of the uncoated samples had intermittent contacts. In contrast, the encapsulated samples passed through 1000 thermal cycles with no intermittent contacts.

The intent for the assembly process was to make it as straightforward as possible, Gibson said. "We used readily available commercial equipment. There are no special requirements. We've just taken standard technology and applied it in a very thoughtful manner," she explained. "We wanted to develop a process that wouldn't be foreign to a hybrid-assembly house." The only caveat, according to Gibson, is that the two companies have no handle as yet on the technology's limitations.

According to Gibson, only single-layer circuitry has been done using the Novaclad material, but there's no reason why multilayer circuits can't be constructed. Placing components on both sides of the material is also a possibility, she said. At present, researchers are working with 16-mil pitches on the flex circuitry, but that's likely to come down in the future. Similarly, bump counts are just now moving from 14 to 18, but Gibson sees counts in the 20s as relatively unchallenging. The company's commercial intentions for the assembly technology include the control electronics in 1.8-in disk drives, which are extremely volume-limited assemblies. Other foreseeable applications include automotive tasks both under the hood and inside the passenger compartment.

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IC CONTROLLERS RUN UNIVERSAL OFF-LINE SWITCHERS THAT NEED NO ISOLATED FEEDBACK FROM THE OUTPUT TO INPUT.

ICs BUILD OFF-LINE ISOLATED SWITCHERS

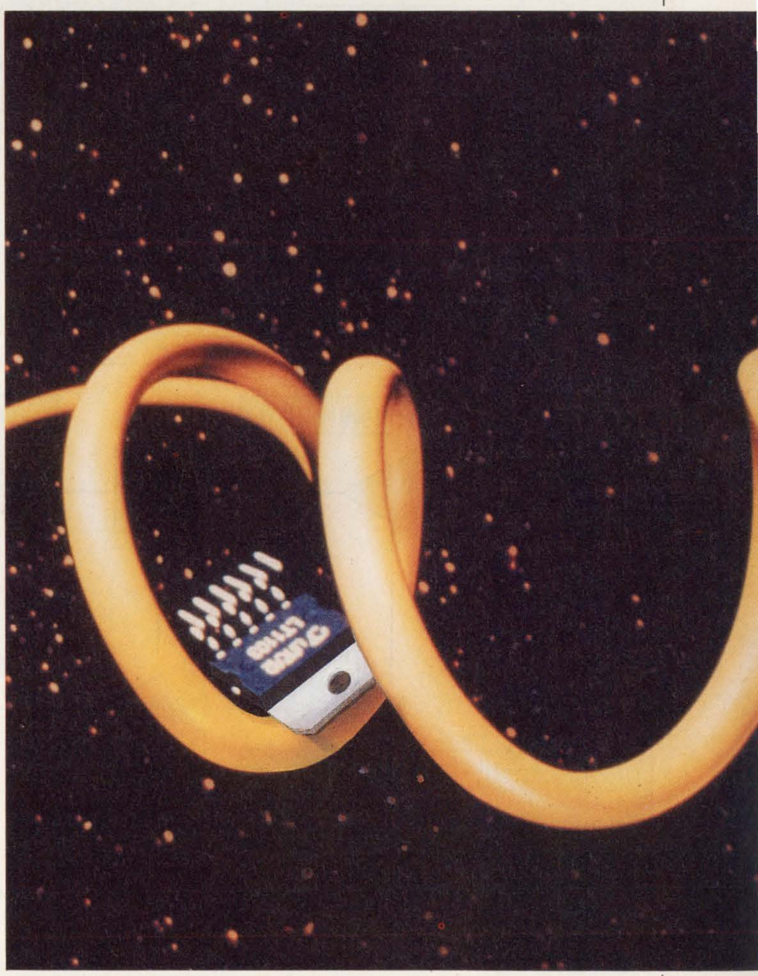
FRANK GOODENOUGH

Every electronic system requires a power supply, yet its design often seems to be left to the last minute. But power-supply design isn't all that simple, particularly if the supply is of the switching type and tight regulation specifications are required. A specialist is usually needed in this case with attendant cost and time-to-market problems.

Now a pair of controller ICs, the LT1103 and LT1105 from Linear Technology, are altering that scenario. These "do-it-yourself" devices allow even a system designer with no power-supply experience to easily and quickly build a 100-W, universal, off-line switching-regulator supply having 1% line and load regulation. All that's needed besides the controller IC are a power MOSFET, a transformer, diodes, and a handful of passive parts *(see the figure)*. Moreover, no negative feedback is required across the isolation barrier from output to control circuitry. As a result, system designers now have the advantages of quicker time-to-market, lower product cost, smaller product size, and lower power dissipation.

Using the LT1103 and LT1105, engineers can create "custom" dc-dc converters. They can put them on their own pc boards close to where a regulated dc voltage is needed. Such supplies save time, space, and dollars, and give the system designer added management control of distributed power. The controllers can handle voltages limited only by the rating of the power FET, and 1000-V FETs are now available.

Distributed power represents a growing trend in system-power management. Here,



the ac power line is rectified, filtered, isolated, and often preregulated by a central supply. The supply's output, ranging anywhere from 24 to several hundred volts, is distributed throughout the system to pc boards or other subsystems. Within each subsystem, dc-dc converters (switching regulators) provide the required subsystem voltages. High voltages are distributed to increase efficiency by cut-

OFF-LINE IC SWITCHING-REGULATOR CONTROLLERS

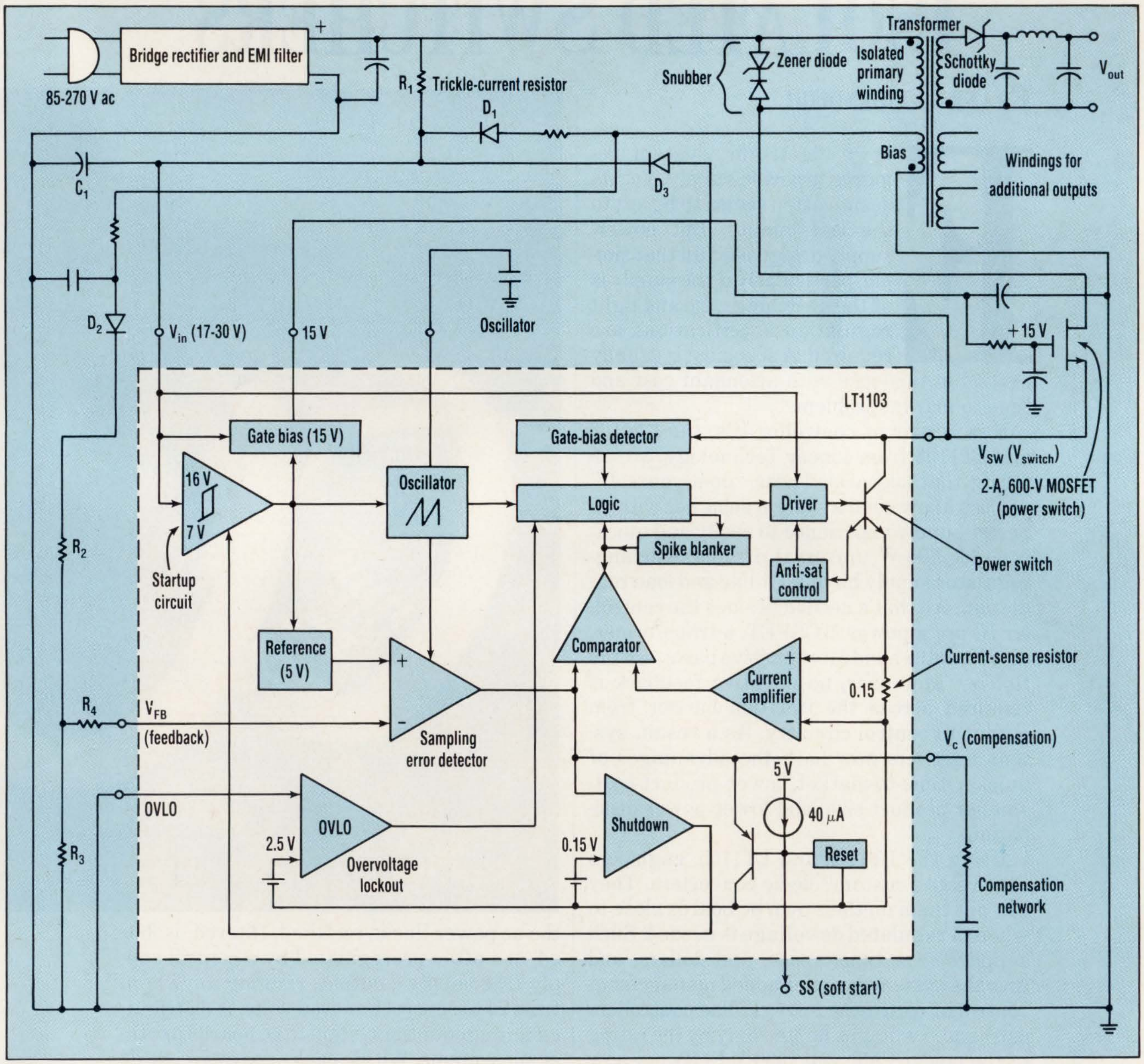
ting IR losses in the cabling, and to significantly cut copper costs and the space required for the cabling.

A power supply using the LT1103 or LT1105 controller ICs can run off domestic or international ac power lines over a range of 85 to 270 V ac. The transformer provides input-to-output voltage isolation and powers the chip. It also supplies the negative feedback for control while offering tight line and load regulation. The chips are the first controllers with that mix of performance and features.

To put it another way, when operating in the fully-isolated flyback mode, the supply achieves line and load regulation within 1% without bringing negative feedback from the output across the isolation barrier. This contrasts with most isolated off-line supplies that require an optoisolator to provide feedback from the output to the input of the controller's error amplifier. Isolators, however, drift with time and temperature, which results in variations in loop gain and stability. Moreover, the additonal components crossing the isolation barrier reduce supply reliability.

The LT1103 is rated for up to 100 W of power. If more than 100 W of power is needed, the LT1105 can drive/control higher-current FETs to build higher-power switchers with similar features and performance.

Unlike most controllers, the



NO NEGATIVE FEEDBACK is needed across the isolation barrier in the LT1103/1105 off-line switching-regulator controller IC, which provides 1% line and load regulation for an isolated load. Instead, the IC uses the amplitude of the flyback pulse at the output of the transformer's bias winding.

OFF-LINE IC SWITCHING-REGULATOR CONTROLLERS

LT1103 doesn't drive the FET's gate from zero to a positive voltage to turn it on. Rather, operating in what's called a common-gate configuration, the chip holds the FET's gate at +15 V dc. The collector of the chip's npn power switch connects to the FET's source, and its emitter connects to ground. When the npn switch is turned on at the start of a pulse-width-modulated (PWM) cycle, it connects the FET's source to ground, putting 15 V between the FET's gate and source and turning the FET on hard. Because all of the FET's current flows through the chip's 2-A maximum power switch, maximum power from an LT1103-based power supply is a function of that current and the voltage applied to the FET's drain, which is about 100 W.

The higher-power (over 100 W) LT1105 can control virtually any power FET. The 1105 contains a second npn power transistor located between the collector of its power switch and the chip's +15-V rail to form a 1-A totem-pole output with push-pull-driven pull-up and pull-down transistors. It drives the gate capacitance of virtually any power FET, switching it between ground and +15 V at rates up to 200 kHz, and turning the FET on and off in under 100 ns.

With the LT1103 and LT1105, designers can build constant-frequency PWM, current-mode switchers. The IC's npn switch is turned on at the start of each oscillator cycle, which then turns on the external power-FET switch in series with it *(see the figure, again)*. The switch's current is sensed by a 0.15-Ω on-chip resistor between the emitter of the npn switch and ground. The voltage across the resistor is amplified by the current amplifier and applied to the comparator. The comparator trips when the output of the current amplifier exceeds the voltage on the control/compensation pin, V_C, turning the switch off. During normal operation, V_C is the output of the sampling error amplifier. The output, in turn, is a function of the supply's output voltage, except for the first 750 ns after the switch is turned on. That's because when the switch turns on, current spikes caused by external parasitic capacitance and diode-stored charge may trip the comparator early. A blanking circuit (on the comparator output) prevents tripping during the first 750 ns of each cycle.

Boot It Up

Before going into detail about the sampling error amplifier and how it gets its feedback signal, let's boot up the circuit and move backwards through the control loop. Yes, switchers (not just PCs) get booted up. That's because it's inefficient and impractical to power a switching-regulator controller from a high-voltage dc source, such as the rectified ac line. Therefore, most transformer-based switchers incorporate a low-voltage auxiliary winding on the transformer-inductor to power the controller, and drive the external power switch once the circuit is running *(see the figure, again)*. However, the controller needs bootstrap circuitry to get it going.

When power is first switched on, the chip is fed a trickle current of about 1 mA through resistor R_1 from the high-voltage source to the V_{in} pin. This current charges the regulator-input filter capacitor C_1 until V_{in} reaches 16 V. During this period, the chip's quiescent current runs about 200 μA. The startup circuit keeps all of the internal voltage regulators off and the circuit doesn't try to switch. Dissipation in the trickle resistor runs under 1/2 W. When V_{in} reaches 16 V, the internal 5- and 15-V linear regulators turn on and switching begins. If enough rectified-dc power is received from the auxiliary winding via diode D_1 to keep V_{in} above 12 V, the switching continues: The boot-up is successful.

If V_{in} drops below 12 V, the FET-drive detection circuit locks out the switching. V_{in} continues to fall as the IC's operating current (about 18 mA) discharges the capacitor. Once V_{in} drops below 7 V, the regulators turn off, the chip returns to the dormant state, and the bootstrap operation starts up again. Such a "burp-start" mode indicates a fault condition or an incomplete power-feedback loop.

The LT1103/1105 also contains soft-start (SS) circuitry, which can force the supply to come up to voltage and charge the capacitor on its output without drawing large surge currents. The SS feature is implemented with the 40-μA current source connected to the SS pin, the pnp clamp connected between the SS pin and V_C, and a capacitor to ground on the SS pin (not shown in the figure). However, unlike the circuitry of most controllers, internal circuits in the chip perform a similar function. Still, the soft-start circuit is there if a longer startup time is required. The V_C and SS pins also enable users to program a switch-current limit below 2 A. During normal operation, V_C is between 1.25 and 4.25 V, which represent low and high currents, respectively.

Bringing the V_C pin below +150 mV activates the chip's shutdown circuit, putting it in a "sleep" mode. When shutdown is activated, SS is reset to 0 V and the quiescent current drops to 200 μA. A current of 400 μA must be pulled from V_C until the internal regulators turn off, after which just 50 μA keeps it asleep.

Flyback Isolated

Just where does the sampling error amplifier get its negative feedback from? How does it know what the supply's output voltage is doing? When operating in the "isolated-flyback" mode, the feedback pin gets its input to the error amplifier from the flyback pulse on the auxiliary winding. Though this technique has been used, regulation was limited to between 5% and 10%. The feedback circuitry in the LT1103 and LT1105 correct for four error sources: the spike on the leading edge of the flyback pulse, the droop in the dc level of the pulse, imperfect coupling between transformer windings, and parasitic resistances in the windings and the diodes.

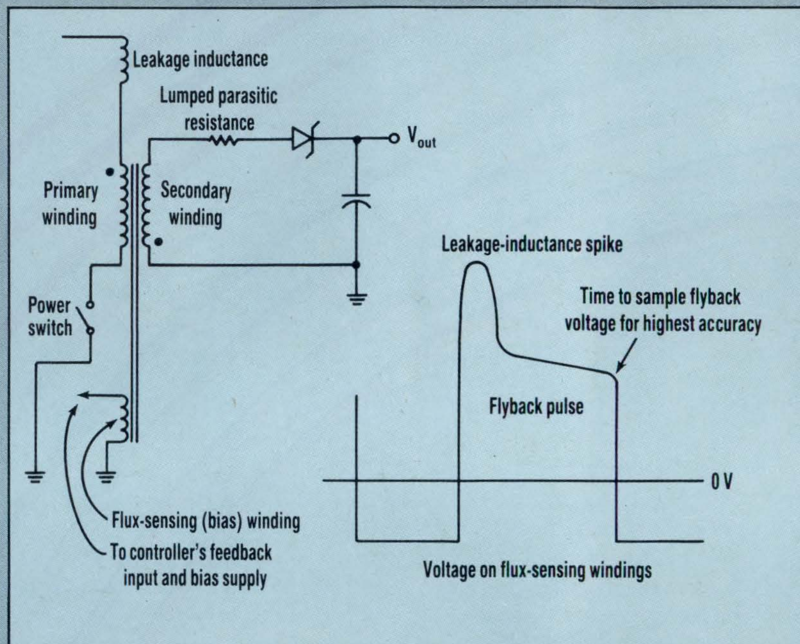
When the power switches (internal npn and external FET) are turned on, the primary winding of the transformer sees the dc input voltage while the secondary and auxiliary windings (also called bias or boot-

SWITCHING SUPPLY INPUT-TO OUTPUT ISOLATION SIMPLIFIED WITH FLUX SENSING

About a half dozen common switching-regulator topologies currently exist (ELECTRONIC DESIGN, *July 25, p. 53)*. But when people are involved, whether operation is from the ac line or some other lethal source, the topologies used are reduced to just two in most situations—flyback and forward. Each topology lends itself to turning the inductor into a transformer to provide isolation between the high voltage and the load and human or semiconductor host.

However, to have regulation, the feedback loop from the output/load back to the controller must be closed. In most cases, flyback and forward topologies require some scheme to bring a signal, representing a direct function of the output voltage, back across the isolation barrier to the controller. While various schemes, such as modulation and chip sets with the reference on the load side of the barrier, have been tried (both of which need an additional transformer), the most common approach employs an optoisolator. Optoisolators introduce errors over time and temperature. They as well as other schemes also represent one or more extra components that must cross the barrier. With multiple devices determining a supply's input-to-output isolation, the supply itself must usually be submitted for regulatory agency (UL, VDE) approval.

If all of the isolation can be provided by one transformer winding, agency approval may be limited to the transformer. Using a technique called flux sensing, the flyback topology lends itself to such a situation. If the turns ratio (N) between the sense and secondary windings of the transformer and the value of the flyback voltage are known, the output voltage should be known *(see the transformer-circuit figure)*.



However, a large spike caused by the leakage inductance occurs on the leading edge of the flyback waveform when the switch turns off. This spike is a function of coupling between the primary and secondary windings and load current. The poorer the coupling and the greater the load, the higher the spike—and the longer it lasts. In a "real" transformer, perfect coupling is impossible. And to get the high-voltage isolation required for agency approval, coupling must be sacrificed. A large, nasty, spike results and the peak-detected output of the sense winding carries a large error, lowering output voltage and dropping load regulation to as low as 8%.

In addition, after the leakage-inductance spike dissipates, the flyback pulse sags due to parasitic resistance in the secondary winding, the output diode, and the capacitor, as well as nonlinear behavior of the transformer. Blanking circuits enable the LT1103/1105 to ignore the spike, increasing the accuracy to about 5%. The accuracy is further improved to about 3% by sampling the flyback pulse just before it collapses to zero (discontinuous mode) or just before the switch turns on (continuous mode). At this time *(the "time to sample the flyback voltage")*, voltage from the sense winding is related to the output by:

$$V_{sense} = \frac{V_{out} + V_F + (I_s)(R_p)}{N}$$

where V_{out} = the output voltage, V_F = diode forward voltage, I_S = secondary current, R_P = parasitic transformer secondary resistance and diode resistance, and N = secondary-to-sense-winding turns ratio.

Circuitry sensing switch current compensates for the errors defined by the last term in the equation, representing secondary parasitics. It pumps current into the feedback pin proportional to load current, bringing regulation to within better than 1% over nominal line and load changes.

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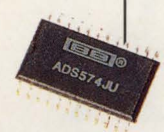

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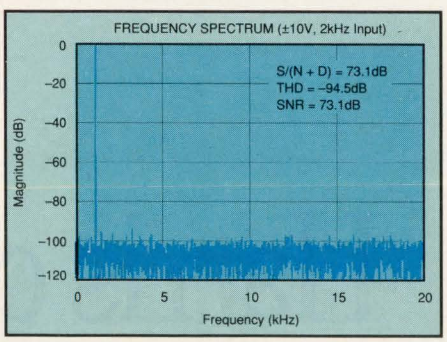

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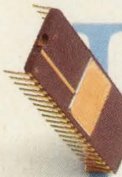

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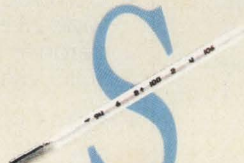

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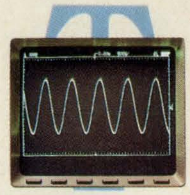

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strap windings) go to negative voltages that reflect the turns ratios. Current flows only in the primary as the transformer stores energy. When the switches turn off, the voltage across them increases (the flyback voltage) until the energy in the transformer's leakage inductance dissipates. The flyback voltage is clamped by the diode plus the Zener-diode snubber network across the primary.

The energy stored in the transformer transfers through the secondary and bias windings to the windings' outputs. The voltages across the primary and bias windings are set by the dc output voltage and the turns ratio after the energy in the leakage inductance dissipates. This relationship holds until the energy in the transformer drops to zero or the switches turn on again. Both cases result in the voltage across the other windings dropping to zero or going negative.

The sampling error amplifier takes advantage of the fact that the voltage across the bias (auxiliary) winding, during at least a portion of switch off time, is directly proportional to the dc output voltage of the secondary winding. The output of the bias winding is passed through diode D_2 and divided down by R_2 and R_3 and applied to the feedback pin. D_2 prevents the feedback pin from being pulled negative and forward-biasing the chip's substrate when the output of the winding goes negative. The first 1.5 μs of the flyback pulse is blanked in order not to sense the leakage-inductance spike on the flyback pulse's leading edge *(see "Switching-supply input-to-output isolation simplified with flux sensing," p. 40).*

After the 1.5-μs blanking period, the first stage of the error amplifier tracks the difference between 4.5 V and the feedback voltage V_{FB}. This is done until it drops rapidly because the energy in the transformer is being used up, or the switches turning on again. The error voltage (4.5 V – V_{FB}), just prior to this time, is at its most-accurate value. The voltage is sampled, held, buffered, and applied to the second stage of the error amplifier. When the switches turn on, the second-stage sample-and-hold amplifier samples the held and buffered error signal for 1.5 μs and holds it for the rest of the period. The droop rate in the hold mode determines the controller's minimum operating rate, which is about 10 kHz. The held voltage is converted to the current output of the error amplifier that drives the V_C pin.

Tricks Of The Trade

At the heart of innovation in analog design lie circuit tricks. One form of such tricks (long used by Carl Nelson, the chips' designer in his earlier switching-regulator ICs) includes handling multiple tasks with one circuit or pin. For example, the V_C pin not only sets the current limit and shuts down the chip, but an RC network from the chip to ground also frequency compensates (stabilizes) the feedback loop.

Fixing three additional error sources to achieve true 1% regulation represents a second example of such single-solution design. Imperfect coupling between the secondary and the bias windings, and parasitic resistance in the windings and in the diodes, cause errors in the output voltage as the load current increases. Therefore, additional circuits force a small current, proportional to the peak switch current, into the feedback pin to provide first-order output-load compensation. This current increases at a rate of 15 μA/A of switch current. This compensating current, passing through the external resistor R_4 in series with the V_{FB} pin, generates a linear decrease in the feedback voltage corresponding to the increase in switch current.

The chip's sawtooth oscillator needs just one capacitor between the oscillator pin and ground. A 400-pF device results in a nominal switching frequency of 100 kHz. Though the oscillator and the rest of the IC's circuit (and, of course, the power MOSFETs) will run at higher frequencies, 200 kHz remains a practical upper limit to maintain line and load regulation while still exploiting the smaller inductors and capacitors permitted by the high frequency (relative to say 40 kHz).

As noted previously, the LT1103 is designed to drive an external power FET from the switch-voltage pin V_{SW} in the common-gate (cascode) configuration. The technique offers the advantage of sensing switch current on-chip in place of an external, expensive, low-value, sense resistor (the LT1105 requires a sense resistor). The technique requires biasing the FET's gate at a voltage high enough to guarantee that it is on when its open-collector source drive is on. A total of 15 V is provided. That's enough to take care of the 10-V drive specification from the FET's data sheet, plus 1 V for typical saturation voltage, and sufficient spare voltage to handle temperature effects and process tolerances. The gate-drive circuit sources 30 mA into a capacitive load without stability problems, and its on-chip current limit takes over at 70 mA. If V_{in} drops below 17 V, the 15-V output also drops. Running about 2 V lower, it tracks the decreasing V_{in} until the chip shuts down. Because of the gate-bias detector circuit, the startup window is reduced to 6 V, and to 4 V when biased from the 15-V rail, when the gate is biased from V_{in} (which it can be). In the LT1105, the gate-bias detector is connected to the 15-V rail.

Loop De Loop

A special circuit senses V_{SW} just prior to turning on the switch. It's tied to the FET's source and should represent the bias voltage on the gate when the switch is off. When the FET switch first turns off, its drain potential increases due to flyback action until it's clamped by the snubber network. The source voltage also increases due to flyback action, parasitic capacitive coupling within the FET, and parasitic lead inductance. An extra diode, D_3, from the source to either the gate or to the V_{in} pin (as shown in the figure) prevents fault conditions that could damage the FET. The diode clamps the source to one diode drop above the source or V_{in} limiting gate-source reverse bias.

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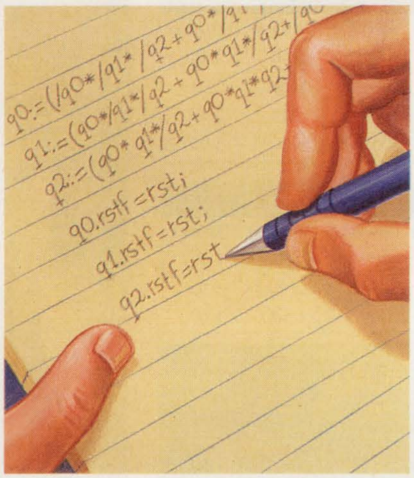

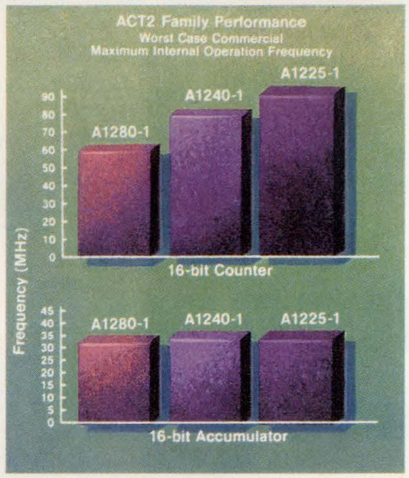

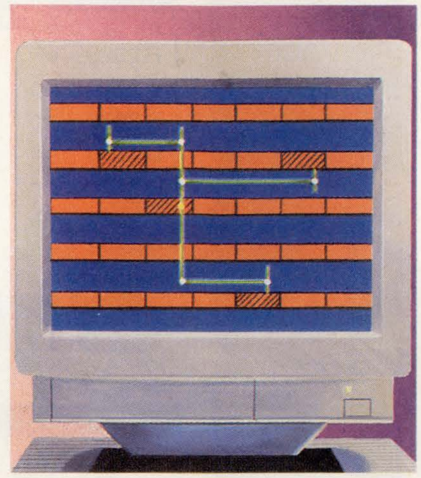

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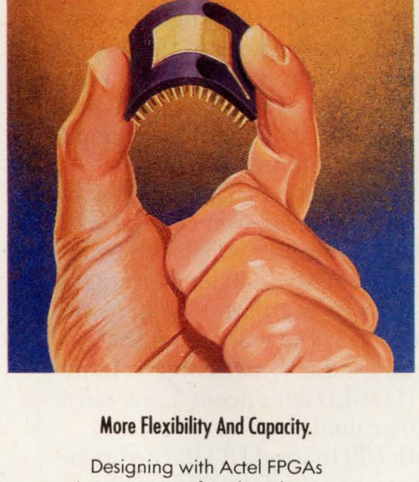

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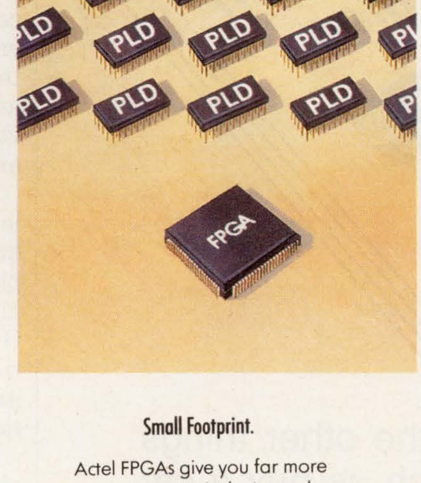

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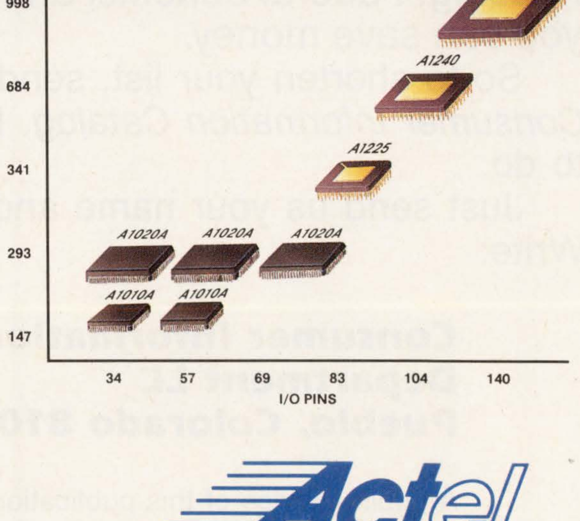

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Both LT1103 and LT1105 controllers also contain an overvoltage lockout (OVLO) circuit, which can be implemented with a divider from the high-voltage regulator input to the OVLO pin. If the voltage on that pin rises above 2.5 V, switching is inhibited. If OVLO isn't needed, the pin is tied to ground.

Both LT1103 and LT1105 are available in two packages, the former in 7- and 11-pin power SIPs, and the latter in 8- and 14-pin DIPs. The LT1103 in the 11-pin SIP provides all of the controller's features, while the 7-pin model (which is the same size as a TO-220) lacks the SS, OVLO, and reference pins and functions. Similarly, the 14-pin LT1105 is full-featured, while the 8-pin model is shy of SS, reference-output, and OVLO features. SS can be initiated at the V_C pin with external active devices.□

PRICE AND AVAILABILTY

The LT1103 and LT1105 controllers are for operation over the commercial temperature range of 0 to 70°C. However, the chips will take the military temperature range. For example, they can be used in chip and wire hybrids. In quantities of 1000, the LT1103 goes for $6.50 each in the 11-pin SIP and $5.10 each in the 7-pin SIP. Its companion LT1105 goes for $4.25 each in the 8-pin DIP. Pricing isn't available for the 14-pin DIP version.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487; Bob Scott, (408) 432-1900. **CIRCLE 511**

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MODERATELY	526
SLIGHTLY	527

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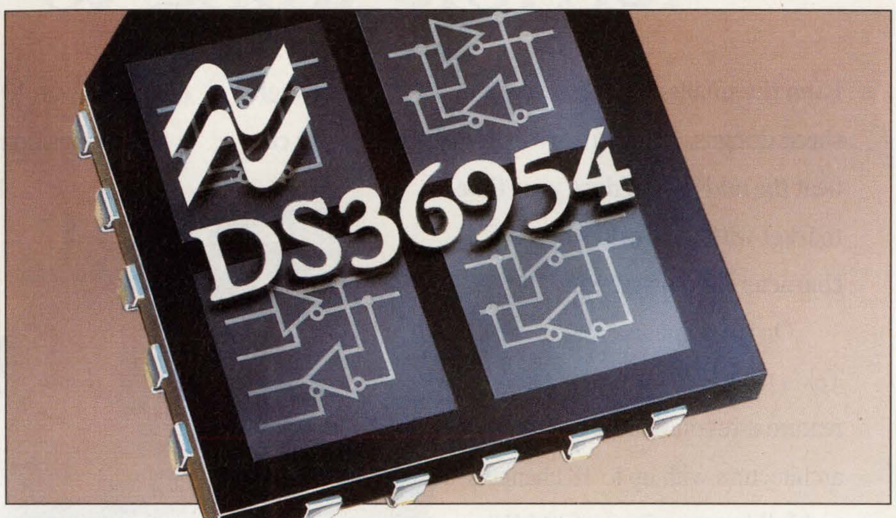

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	Min. (ns)	Typ. (ns)	Max. (ns)
DRIVER			
t_{PLH}	9	15	19
t_{PHLD}	9	12	19
t_{SKD}		3	6
RECEIVER			
t_{PLH}	9	14	19
t_{PHLD}	9	13	19
t_{SKD}		1	3

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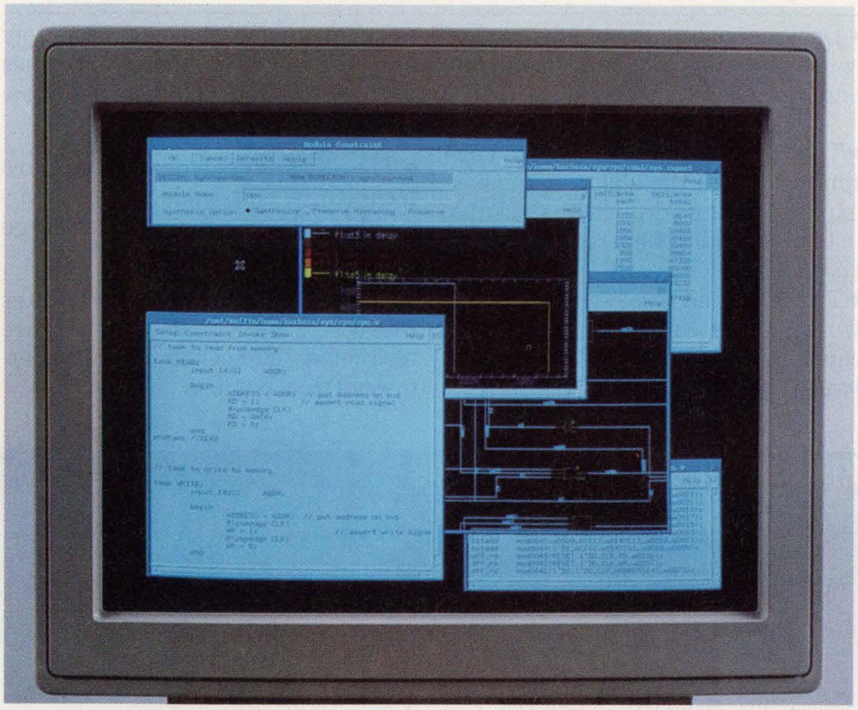


LISA MALINIAK

TOP-DOWN DESIGN IS FUELING THE DEMAND FOR SYNTHESIS THAT'S TIGHTLY INTEGRATED WITH THE OVERALL ENVIRONMENT.

SYNTHESIS TOOLS MOVE INTO THE MAINSTREAM

The electronics industry is seeing a considerable upswing in synthesis vendors and products. Many vendors have entered the market, while others have added to their existing offerings. Why? Because engineers are finally accepting the idea of software designing their circuits. Activity in the synthesis market is fed by designers' interest in top-down design, a methodology that becomes appealing as complexities increase and time-to-market times decrease.

Top-down design methodology, in which engineers start a design at a high level of abstraction, is built around synthesis technology. There are different levels and types of synthesis. Basically, any type of synthesis provides an automated link between levels of abstraction. For instance, hardware-description-language (HDL) synthesis is the process of turning an abstract text description of a design into gates. The most popular HDLs are VHDL and Verilog. State machines, Boolean equations, and truth tables are other ways of detailing a circuit that needs to be created.

In an HDL-based design methodology, a textual representation is first verified, then synthesized into gates, and verified again before being handed off to physical design. HDL synthesis contains two elements: translation and optimization *(Fig. 1)*. Translation turns the register-transfer-level (RTL) description into a gate-level design, and optimization does technology-specific design transformations to meet area and speed goals set by the user.

Circuits can also be synthesized from an HDL used to express a circuit's behavior. Behavioral description is a level of abstraction higher than an RTL description. The difference between the two is that a behavioral description has no implied architecture in its representation, while an RTL level description has a definite, implied architecture.[1]

In addition to the gains brought about by creating a circuit at a high level of abstraction, there are many other advantages to synthesizing a design from an HDL:

- Designers are more productive because they don't have to manually enter gate-level descriptions.
- The combination of automated optimization and the ability to quickly explore design alternatives results in higher-quality final results.
- The pre- and post-synthesis network models will be equivalent because of the automated bridge between the RTL and gate levels.
- Designers don't have to intimately know each ASIC vendor's libraries because the technology-specific aspects of the design are automatic.
- The high-level descriptions are technology independent and retargetable, allowing for an easy change of vendor.
- Synthesis from an HDL facilitates reuse because RTL descriptions are technology-independent and easier-to-read than net lists.[2]

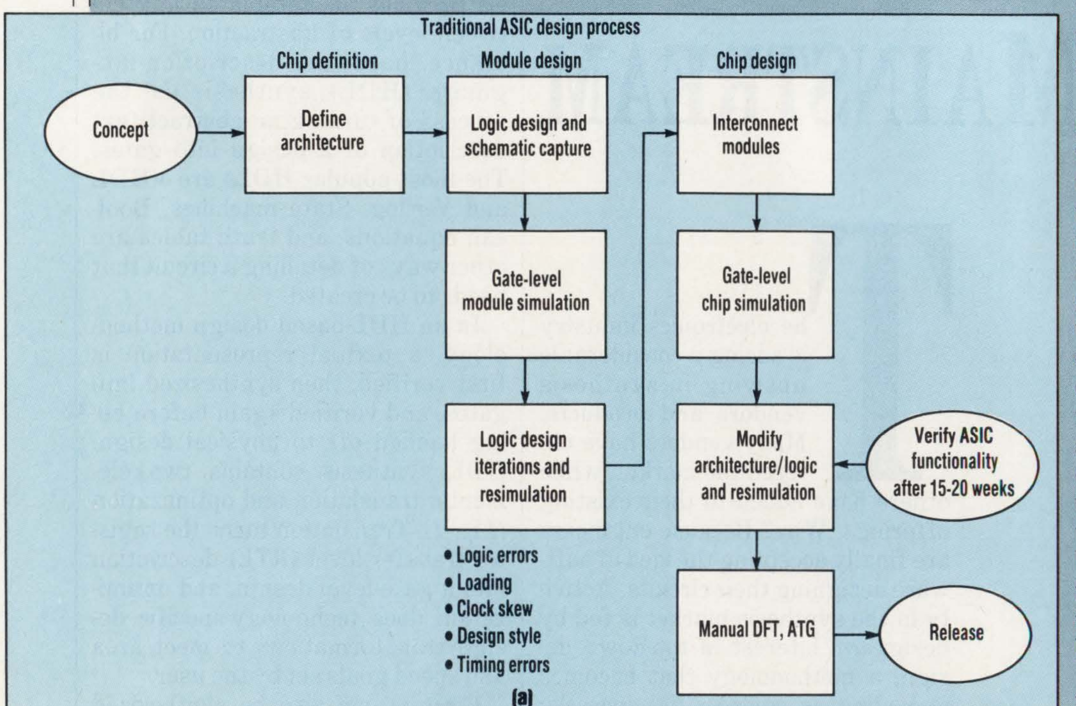
LINKING SYNTHESIS AND SIMULATION

As ASIC complexity exceeds 50,000 gates, traditional gate-level schematic entry can no longer keep pace—the design becomes unmanageable. Top-down design promises engineers the ability to quickly and efficiently describe and simulate complex ASICs. Using VHDL-based synthesis and simulation tools, engineers can cash in on that promise.

Designers can use VHDL to specify a system, board, or IC; verify the functionality of their hardware through simulation; and then, with a minimum of manual effort, complete the design using synthesis. Combining VHDL synthesis and simulation in one environment greatly improves engineering productivity. It also ensures that all components of the system, board, or ASIC will work together, improving the product's time-to-market.

A comparison of the traditional and VHDL-synthesis-based approaches to design illustrates the differences between the two. A traditional methodology for ASIC design uses schematic capture for design description and gate-level simulation for verification. On the other hand, the language-based approach includes behavioral-level simulation, and architectural-logic and test synthesis for implementation.

In the traditional approach, chip architecture is selected early and the design is developed block by block *(Fig. a)*. After each module is implemented and verified at the gate-level, one full chip-level simulation is used to verify overall ASIC functionality. Finally, the entire ASIC design is reviewed for testability, with modifications made as required.



(a)

With this methodology, the later the stage at which errors are found, the greater the loss of time and effort in correcting them. Because the designer is working at the gate level throughout this process, the entire chip's functionality can only be verified at the full-chip simulation stage. If the design doesn't meet its objectives (or worse, if it meets the ASIC specifications but still doesn't "play" in the system), all or part of the design process must be redone.

In contrast, today's VHDL-synthesis-based

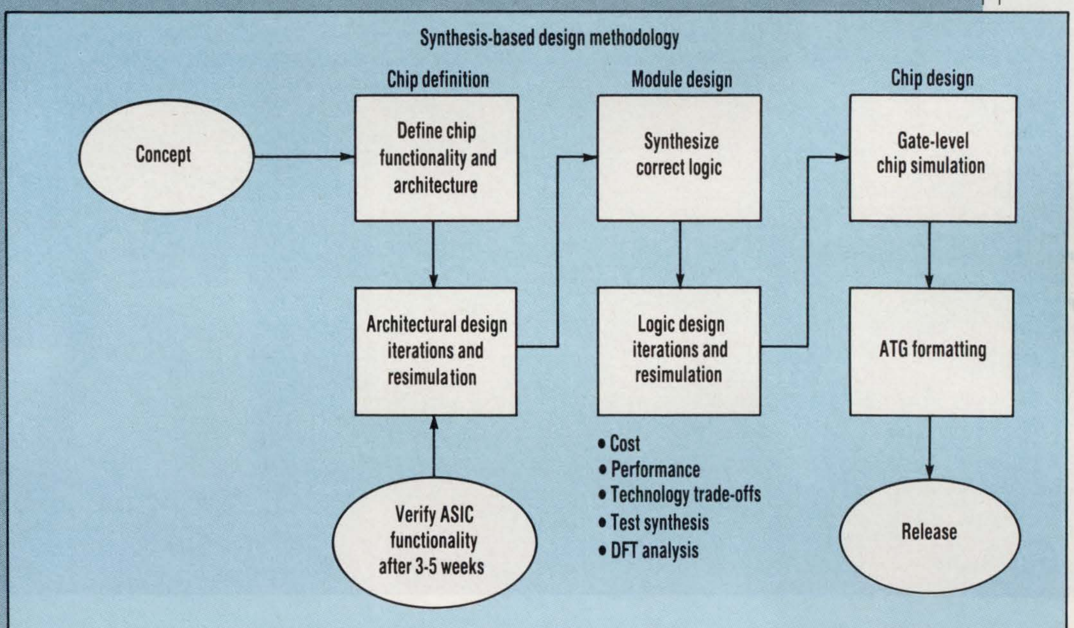
However, despite their successes, synthesis tools do have some problems. For instance, how do engineers test gates that they didn't create? What types of difficulties crop up when synthesis vendors use different subsets of VHDL? And how are graphically-oriented hardware designers supposed to adapt to textual HDLs?

Testability is a key issue. As designs get larger, building testable designs and generating test vectors for them will be crucial. Today, though, it may not be as critical as some people make it out to be, depending on how engineers use synthesis. For instance, if engineers enter a large description into the synthesis tool and come up with an extremely large gate-level design, then test vectors will be absolutely necessary. But if they synthesize block by block using test vectors that can be simulated, it's not a big problem.

In addition, engineers must decide whether or not they want to pay the overhead resulting from synthesizing test structures. For example, a test methodology like full scan will use up silicon area because of the scan elements that are inserted.

Another potential problem with synthesis tools is that they all support varying subsets of VHDL. In fact, an IEEE committee is currently working on standardizing a subset of VHDL for synthesis. Because many constructs in VHDL can't be

design methodology enables engineers to develop a model of the ASIC and the environment of the target system if desired, so that chip functionality can be verified early-on in the design process with a VHDL simulator *(Fig. b)*. Graphical user interfaces tuned to VHDL standards and the designer's need to manage a large number of VHDL processes, packages, variables, and signals will help speed the transition of new users from the graphical capture of gates to language-based hardware design. Once the system specification has been completed and functionality verified, the design of its ASIC components may begin.



(b)

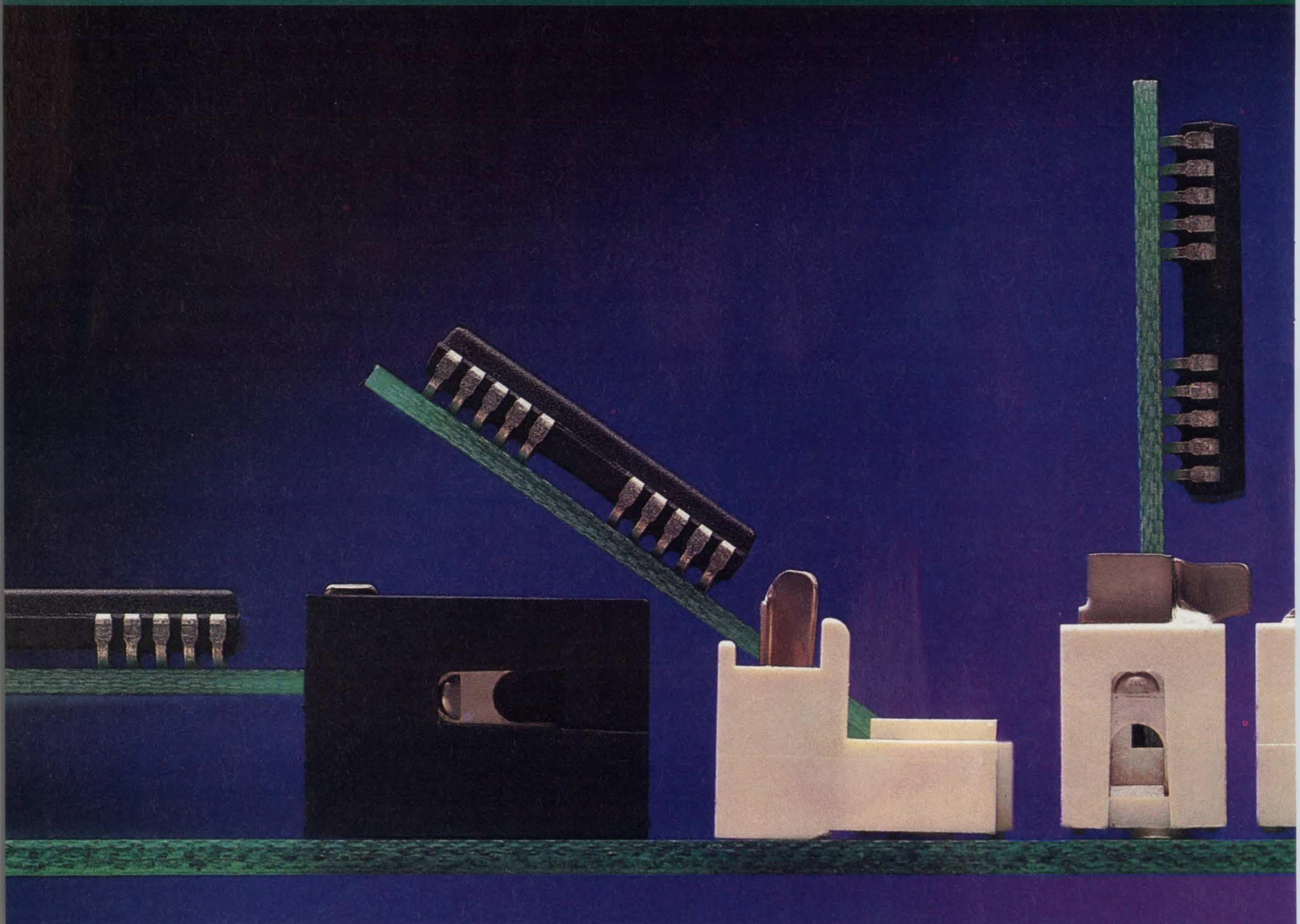
Optimizing an RTL structure from a VHDL behavioral description, called micro-architectural synthesis, is more than just translation from VHDL to RTL. Micro-architectural synthesis optimizes the use of ALUs, registers, multiplexers, and control logic the same way logic-optimization tools optimize the use of gates, flip-flops, and buffers. When combined with an ability to create state machines and data paths from a unified design description (from a single process in the case of VHDL), micro-architectural synthesis minimizes the restrictions on design style for system specification, and enables the use of compact design descriptions.

Following micro-architectural synthesis (or beginning with an RTL structure if not using high-level synthesis tools), detailed logic is synthesized automatically, balancing cost, performance, silicon utilization, and other technology trade-offs as defined by the user. Test synthesis adds test logic and ensures that the design will be testable.

Though the final gate-level simulation of the entire design is still required, its purpose is to verify the design's readiness for release to layout. The idea isn't only to build the ASIC correctly, but to build the correct ASIC. A design environment that combines VHDL synthesis and simulation enables designers to rapidly describe and then verify their ASICs in a system environment without generating gate-level designs, either manually or through logic synthesis and other commercially available tools.

Contributed by Steve Deutsch, technical director of the ASIC product group for Racal-Redac.

Now you know all the angles.



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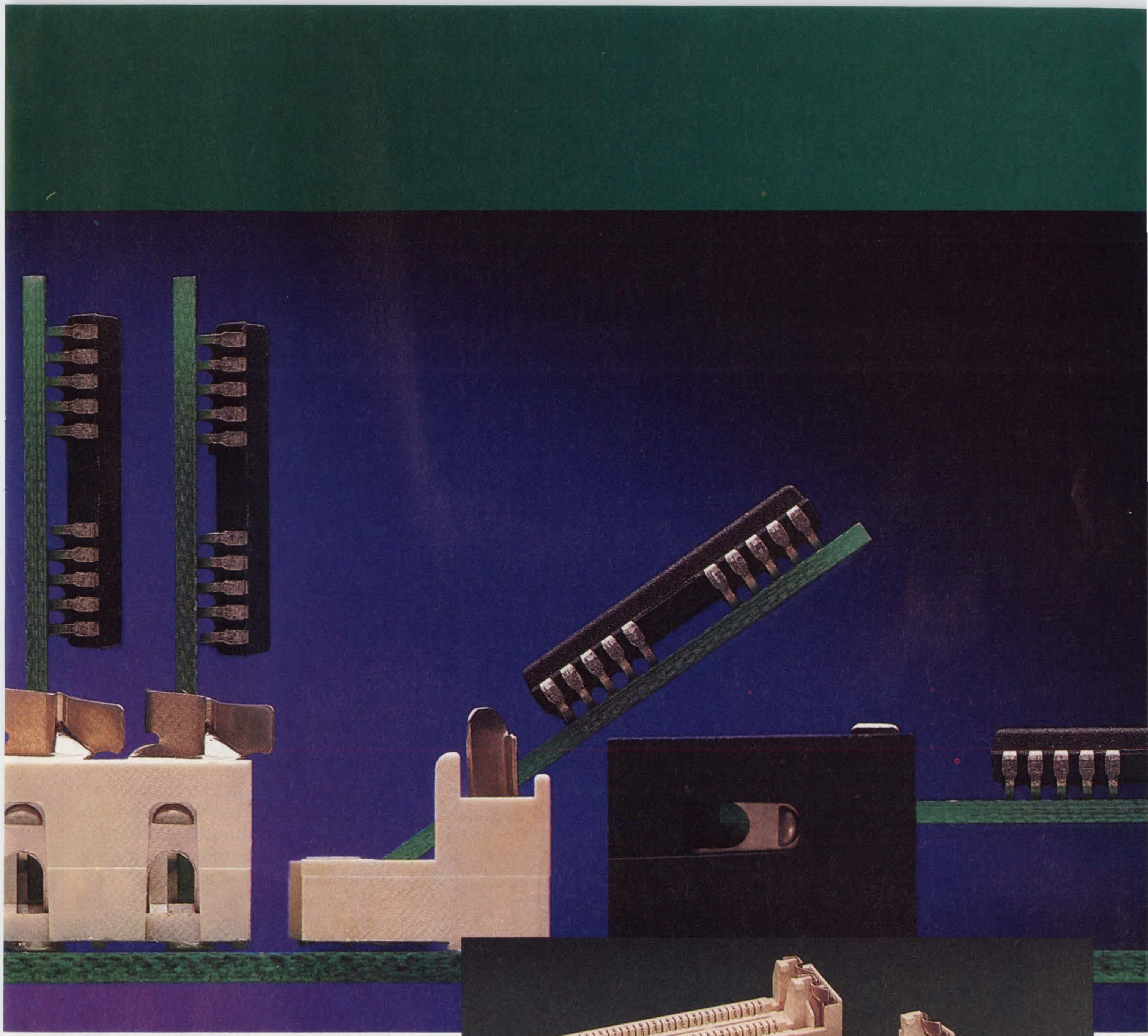
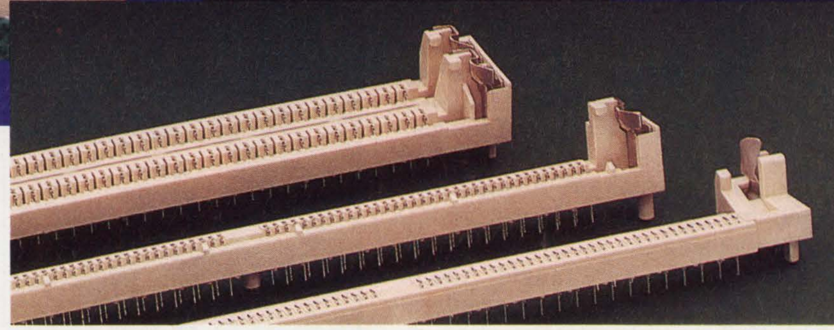




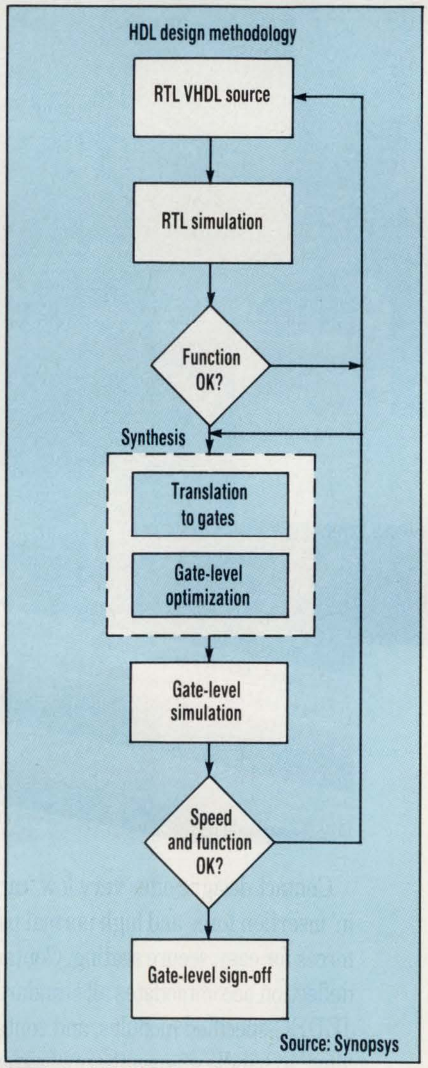
synthesized, each vendor chose a different group of constructs for their tool. For instance, Jeff Fox, vice president for ASIC tools for Racal-Redac, claims that Racal's synthesis tool accepts a fairly large subset of VHDL. Because of that, says Fox, users can mix behavioral, data-flow, and structural descriptions. In addition, Racal supports such VHDL constructs as "while" and "runtime" loops.

The support of various VHDL subsets currently doesn't pose a problem for most synthesis users because there doesn't need to be portability between synthesis tools. Usually, engineers only employ one vendor's synthesis tool. But as the market matures and engineers do use more than one tool, portability could pose the same problem it does with VHDL simulators. VHDL simulators all support different subsets, causing a problem with model portability. That's because engineers might need to simulate a model built with language constructs not supported by their present simulator.

One stigma has plagued HDL-based synthesis from its beginning: How do graphically-oriented hardware engineers adapt to designing with a high-level language? According to Robert Mendes da Costa, director of marketing for the Design Synthesis Div. of Mentor Graphics Corp., there's a segment of the market that will adopt language-based design methodology. A significant number of people, however, wish to design using the same methodology in which they were taught. And today's designers innovate graphically. For example, state-machine descriptions, parametrizable macro functions, data-flow descriptions, and functional-block descriptions appeal to the majority of the market. There are lots of productivity benefits to a graphical approach.

That's not to say HDLs aren't a good method for describing a design. Engineers may even mix input methods in many of today's tools. In this type of situation, however, integrating synthesis with the overall design environment becomes crucial. Say an engineer has a state-machine description in graphics and a VHDL description for a controller in one design. The environment must have synergy between what can be captured, simulated, synthesized, and tested. This mixed design-entry methodology starts to demand much tighter integration among tools.

Integration is also important for overall productivity. But, as Jeff Lewis, group marketing manager for HDL products at Synopsys Inc. points out, there are varying levels of where integration is necessary because of where the iteration loops occur. Simulaton is one area where a strong bond is necessary. For example, engineers designing with a non-integrated product may find out that certain VHDL constructs they were using for simulation aren't synthesizable. This wouldn't happen if the simulator and synthesis tool were closely coupled. Also, libraries supported by a simulator might not be supported by a synthesizer, and the timing specifications for simulation libraries may be different from those of the synthesis libraries. A design environment with that much disparity creates lots of errors and wastes much time. "The best type of top-down design environment is one where designers don't see the synthesis tool, and that requires integration," according to Mentor's Robert Mendes da Costa.



1. AN HDL-BASED design methodology includes the development of a design description, that description's validation, a synthesis step, and a final verification step. It's easy to see that synthesis is at the heart of this top-down design style.

In addition to simulation, synthesis should be closely coupled to back-end tools, like those for IC and board layout. Prasad Subramaniam, supervisor of the CAD external service group, explains that there's a lot of feedback from those tools that can help the synthesis tool when it's taking another crack at a design.

Also, users who decide to buy point tools are going to be spending much time and money making them talk to each other. To ease this problem, many vendors will concentrate on creating higher levels of integration between synthesis and the rest of the design cycle *(see "Linking synthesis and simulation," p. 52).* The total design-iteration time from design specification to gate-level simulation comes into play when users are deciding to buy tightly-integrated tools. Abrar Ahmed, product manager for Mentor's Design Synthesis Div., explains that "point tools may be fast, but when they have to share data with another tool, it adds long delays into the total iteration time. This is a problem because the mainstream designer is more focused on solutions than making point tools work together."

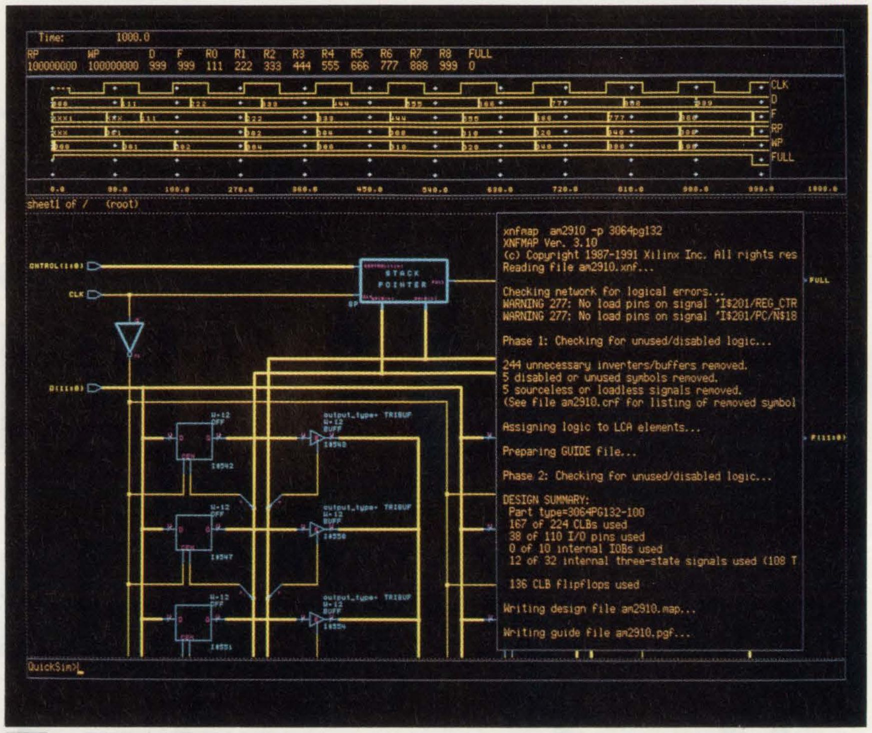
Vantage Analysis Systems Inc., Fremont, Calif., is addressing the integration problem with its Vantage Synthesis Associate Program (VSA). VSA is a consortium of synthesis

vendors working with Vantage to verify that its synthesis tools work correctly and efficiently with the Vantage VHDL simulator. The increasing number of VHDL synthesis products makes it important for engineers to know how much of the VHDL language the synthesis tool covers. With VSA, users gain assurance that there's sufficient interoperability between the simulator and synthesis tools. The primary effort of VSA is to verify the interfaces between the simulator and synthesis tool by checking that the synthesis tool reads and writes VHDL correctly. VSA Program members include Compass Design Automation, Dassault Electronique, Exemplar Logic, LSI Logic, Mentor Graphics, Racal-Redac, and Teradyne. Because Vantage is already a member of Synopsys CAE Partners Program, there was no need for Synopsys to join VSA. Vantage has received many of the synthesis tools and will perform most of the validation work.

The growth of the synthesis market shows that designers are beginning to reap the rewards of synthesis technology. While the synthesis market has been and is currently dominated by Synopsys, new product offerings from different vendors will challenge its synthesis leadership. Synopsys offers the Design Compiler synthesis product, as well as the ECL Compiler for ECL designs and the Test Compiler to synthesize test structures.

Synopsys released the latest version of its Design Compiler at the Design Automation Conference (DAC) several months ago. According to the company, the most important aspect of this upgrade was the tighter integration with other design tools, which produces a smoother flow of data throughout the design cycle. For example, Version 2.2 of the Design Compiler now has a transparent interface to the Zycad accelerators.

Version 2.2 establishes a much tighter joint between the company's synthesis tools and its VHDL System Simulator. As a result, the Design Compiler family can write VHDL timing reports that can be read directly by the simulator for



2. THE SCHEMATIC in the lower left of the screen is being built graphically from large functional blocks using Mentor's AutoLogic Blocks tool. For example, the stack pointer is a state machine with 10 states and 100 gates. Approximately 1300 gates are contained in this schematic.

gate-level simulation with synthesized logic timing.

There are also links to physical-layout data from such place-and-route tools as the Gate Ensemble product from Cadence Design Systems Inc. Chip-layout data may be back-annotated into the synthesis tools for timing verification, enabling engineers to confirm that the post-layout timing parameters meet or exceed those specified during the synthesis process.

A new source-to-gate linkage connects a synthesized structural schematic with the associated HDL source code. The link simplifies the transition between the RTL and gate levels when tracking problems in a design. Engineers can highlight synthesized modules and structural elements by selecting a statement or group of statements in the original HDL source code. Conversely, selecting a structure will highlight the appropriate HDL code.

Valid Logic Systems Inc. and LSI Logic Corp. have both integrated the Synopsys tools into their design environments. The Synopsys tool is tightly integrated within Valid's recently announced top-down design environment. It includes the company's VHDL simulator and Concept compound-capture tool. With Concept, users can enter a design with graphics or text. The graphics are automatically converted to VHDL text. In addition, Concept will instinctively determine whether or not a VHDL description is ready for synthesis by the Synopsys tool. Although the Synopsys synthesizer works well in this environment, Valid has plans to acquire its own synthesis technology in the near future.

LSI Logic uses the Synopsys synthesis tool with some of its own technology in the company's Silicon 1076 product, a concept-to-silicon, top-down design system based on VHDL. In the system, a Synthesis Manager prepares data for three synthesis products that create gate-level net lists from RTL code. The Logic Block Synthesizer generates speed- or area-optimized gate-level net lists of logic functions from pa-

rametrized procedure calls in the VHDL RTL code. The Memory Compiler generates fast memory structures from parametrized calls in the RTL code. Finally, the RTL Synthesizer synthesizes the rest of the RTL code into a gate-level net list. It then optimizes the complete net list for speed and area.

Mentor Graphics hopes to be the synthesis leader by 1993. According to the company, it will do that by providing customers with the best top-down environment in the market based on its AutoLogic synthesis technology and tight integration with the rest of its design tools. For example, a common compiler for the Mentor simulation and synthesis tools ensures correct interpretation of a model. This is important because two separate compilers with two separate tools introduces inaccuracies into the model, possibly producing a bad design once it's synthesized.

The Mentor products currently available include AutoLogic, AutoLogic Blocks, and PLDSynthesis. AutoLogic is a logic-synthesis and optimization tool for ASIC and IC designers. It can create and optimize circuits from such inputs as state machines, graphical high-level macro functions, schematics, net lists, PLA tables, and Boolean descriptions. AutoLogic Blocks is an option to the AutoLogic product that lets engineers specify designs in graphical high-level macro functions, state machines, or Boolean equations *(Fig, 2)*. These descriptions are then synthesized with the AutoLogic product. PLDSynthesis generates and fits designs into programmable logic.

Three other synthesis products will be available from Mentor by the end of the year. AutoLogic FPGA is an option to AutoLogic that provides architecture-specific optimization for Actel, Altera, and Xilinx field-programmable gate-array (FPGA) families. AutoLogic VHDL synthesizes circuits from VHDL descriptions. Design Architect integrates a schematic editor, a symbol editor, a VHDL editor, and a compiler into a unified environment. Future announcements include a product to address test synthesis.

FPGA synthesis is also available from Exemplar Logic Inc. The Exemplar Release 1.0 software package includes tools for compilation, synthesis and optimization, architectural analysis, and library and schematic generation. Users can compare speed and area results for various FPGA architectures. The system can also analyze CMOS gate-array architectures.

The system accepts VHDL, net lists, CUPL, PLA truth tables, Palasm, and Open ABEL as inputs. It then synthesizes the input into an internal logic format that's optimized for a specific FPGA or ASIC device architecture. The final output is either a vendor-specific or EDIF net list.

Release 1.0 is based on three core-optimization algorithms. One provides limited fan-in optimization for the Xilinx FPGA architecture. Another handles multiplexer-based optimization for the Actel architecture. And the third offers fast CMOS mapping for retargeting designs to ASICs.

Cadence Design Systems announced its synthesis technology early this year. The technology is found in the form of two products, the HDL Synthesizer and Optimizer. The Synthesizer works from Verilog input now, but will support VHDL by the end of the year. It automatically partitions a design by recognizing relationships between circuit elements. A trade-off curve shows constraint-based implementation alternatives early on. The Optimizer provides optimization and mapping for gate-level designs created by the Synthesizer.

HDL Synthesizer and Optimizer were developed as an integral part of the company's front-to-back design system for ICs, ASICs, and programmable logic. Thus, only one library is used by all of the design tools (simulation, synthesis, timing analysis, and fault simulation). In addition, the common delay-calculation capability ensures accuracy and consistency between design and analysis tasks. And tight integration with the rest of the design environment facilitates forward and backward transfer of data. According to Jacqueline Taylor, Cadence's product marketing manager, the company is focusing considerable energy on creating a very tight fit between the simulation and synthesis technology. It wants to ensure that there's lots of flexibility to how the designer can describe a circuit at a high level and still get fast simulation results and then synthesize that description.

The SilcSyn VHDL System from Racal-Redac integrates three kinds of synthesis: architectural, logic, and test. Architectural synthesis is for behavioral design and high-level op-

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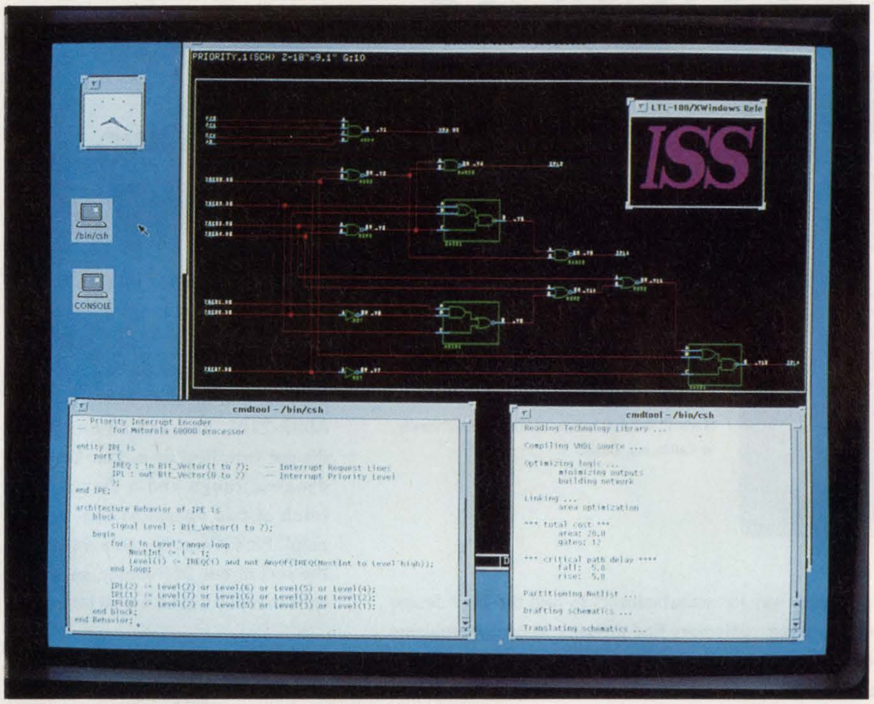

3. SYNTHESIS AND OPTIMIZATION are performed by the Unix-based LS-2000 tool from Integrated Silicon Systems. It can synthesize from a high-level description or optimize an existing design for speed and area.

timization. Logic synthesis optimizes the design for speed and area in gate-array and standard-cell libraries. Finally, test synthesis designs circuits for testability and test-pattern generation. In addition, the SilcSyn product meshes tightly with Racal-Redac's recently-announced VHDL 2000 simulator.

Two different types of synthesis technology are available from Viewlogic Systems Inc. The company's VHDL Designer product features gate-level schematic generation from VHDL inputs. Users can simulate the design before and after it's synthesized. The Retargeter is a technology retargeting tool. It can combine existing PLD designs, optimize for speed and area, and retarget them into an FPGA or ASIC.

One big advantage to the Viewlogic synthesis technology, says Raymond McCann, the company's synthesis marketing manager, is how tightly it's integrated with the rest of Viewlogic's CAE environment. He points out that the tight integration is exemplified in the way the Viewlogic tools generate live, workable schematics. Some other tools synthesize a design, and then run the results through a schematic-generation program, resulting in a picture of the schematic. But with the Viewlogic Viewgen product, users generate a live schematic that can be edited and is an entire database of its own. In addition, Viewgen also highlights the critical design path.

French Synthesis

The synthesis technology from Dassault Electronique was first used by the company internally in 1986, yet it's only been marketed for a little over a year. The product, called Frenchip, synthesizes all types of logic. In addition to the Boolean techniques of two-level minimization and factorization, Frenchip uses specialized algorithms to synthesize structured logic, such as adders, comparators, and multipliers.

Frenchip supports top-down design based on hierarchical block diagrams. Using this approach, engineers can break down their designs into lower levels and write behavioral models for basic blocks. The blocks correspond to logical functions that are familiar to engineers, like state machines, multiplexer trees, and counters. The software assembles blocks hierarchically, and can integrate blocks designed outside the synthesis product. It also synthesizes test structures, and supports internal-scan, boundary-scan, and built-in self-test (BIST) functions. The system includes tools to distribute clock signals and to insert the ASIC pad ring.

Once individual blocks are synthesized, Frenchip calculates the loading of interblock nets, taking into account statistical wire loading. Then, where needed, it resizes components, inserts buffers, and builds buffering trees. Working hierarchically, it builds the complete chip with no gate-count limitation.

Teradyne Inc. has integrated the Frenchip tool into its new top-down design environment called the MultiSim Architect. In addition to the synthesis tool, the environment consists of the Vantage VHDL simulator, and Teradyne's timing-analysis and test-vector-generation software. One major reason Teradyne chose the Dassault tool was because of it's test-synthesis capabilities. The company claims that MultiSim Architect will cover complete ASIC design, from design to test.

AT&T announced its synthesis technology at DAC this year. High-Level Design System has a performance-driven synthesizer that optimizes ASIC performance through full-chip resynthesis, buffer insertion, and cell-replacement algorithms. This technology should pave the way for FPGA to gate-array or standard-cell migration and vice-versa. These same resynthesis techniques can optimize area or performance within one-chip technology.

The system also has behavioral and structural synthesizers, a macrocell compiler, a net-list-to-schematic generation module, a simulator, a waveform-display module, netlist compilers, and an EDIF 2.0 netlist interface. These modules work efficiently with 50- to 100-kgate ASICs, and are oriented toward optimizing the capture, behavioral simulation, verification, and synthesis phases of IC design.

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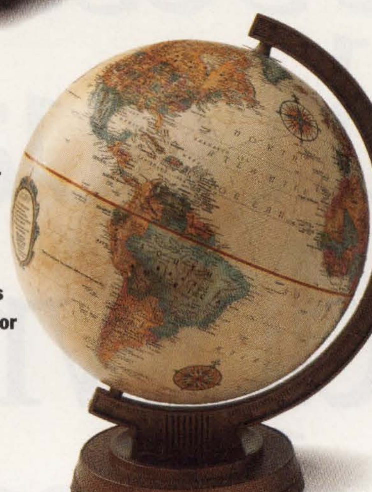

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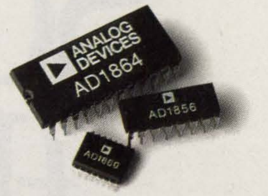

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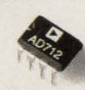

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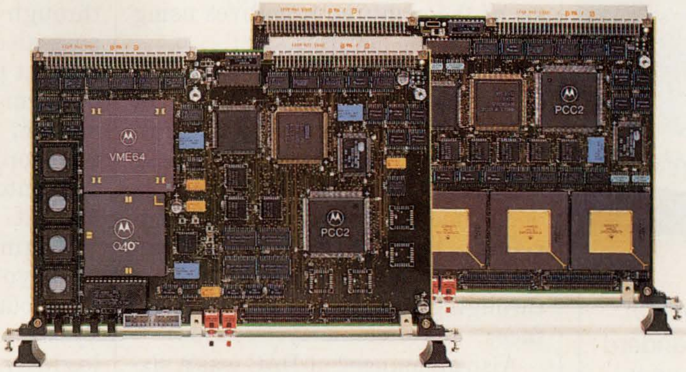

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Behavior-level circuit descriptions in either C or VHDL are turned into optimized gate-level descriptions by the behavioral-synthesizer module. Capture and synthesis of functional primitives, such as state machines, ALUs, counters, and registers, at the RTL level is performed by the Structural synthesizer. It also creates C models to specify each one's behavior, and provides logic synthesis of the captured primitives using standard-cell libraries.

The core synthesis engine is based on an intensely enhanced version of Berkeley's MIS. It's closely integrated with a fast and accurate timing analyzer that can support multiple delay models. Integrated constraint-capture, hierarchy-viewing, and traversal functions are available through graphical and textual interfaces.

Also announced at DAC was a six-year agreement between AT&T and Dazix, an Intergraph Co., to jointly develop and market synthesis technology. Dazix will market products for C and VHDL synthesis, test synthesis, structural synthesis, and timing-driven synthesis within its Simultaneous Engineering Environment. In addition, Dazix and AT&T will begin developing and integrating advanced behavioral synthesis tools.

ASIC Synthesizer is the synthesis product from Compass Design Automation. The company claims it's the only synthesis technology available today that has the compilers and ASIC libraries to create an entire ASIC chip, including the pad ring, from an HDL input. It accepts either Verilog or VHDL as input. The input description includes all of the information needed to make a complete chip, such as memory elements, datapaths, control and random logic, pad-ring description, as well as the specific performance criteria.

The tool first checks the HDL input for construct errors and syntax problems because some constructs may not be synthesizable. It also evaluates the HDL description to determine which of its design tools best suits the performance criteria. These tools include the Logic Synthesizer, Datapath Compiler, and memory compilers. ASIC Synthesizer then synthesizes the design using those tools.

Before the actual synthesis process is run, users can specify whether or not the run should include the physical layout of the design. If the run is a first attempt, for instance, users may want to do a simulation before running the complete chip through physical-design tools. Compass also automates the test-development process with compilers that perform automatic test-vector generation, scan and functional block isolation, probabilistic fault grading, and automatic test-program development.

Engineers just getting started with synthesis may want to consider the products from Integrated Silicon Systems Inc., a set of two low-cost logic-synthesis and optimization tools for standard cells, gate arrays, and FPGAs. Instant Logic version 2.2 runs on 80386- and 80486-based PCs, and costs only $995. It can synthesize logic net lists from truth tables, Boolean equations, or state machines, and can optimize existing logic net lists for speed or size. Instant Logic also works with language compilers, such as CUPL and ABEL, so that engineers can convert existing PLDs into optimized ASICs.

The company also offers a more advanced synthesis product for Unix platforms called LS-2000, which costs $4995 *(Fig. 3)*. LS-2000 has hierarchical design capability and more advanced synthesis and optimization algorithms than does Instant Logic. Both products will add support for Verilog and VHDL inputs in the near future.□

References:

[1]Carlson, Steve, *Introduction to HDL-based Design Using VHDL*. Mountain View, Calif.: Synopsys Inc., 1990, p. 2-3.

[2]Carlson, p. 4.

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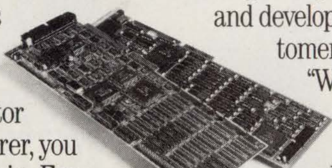

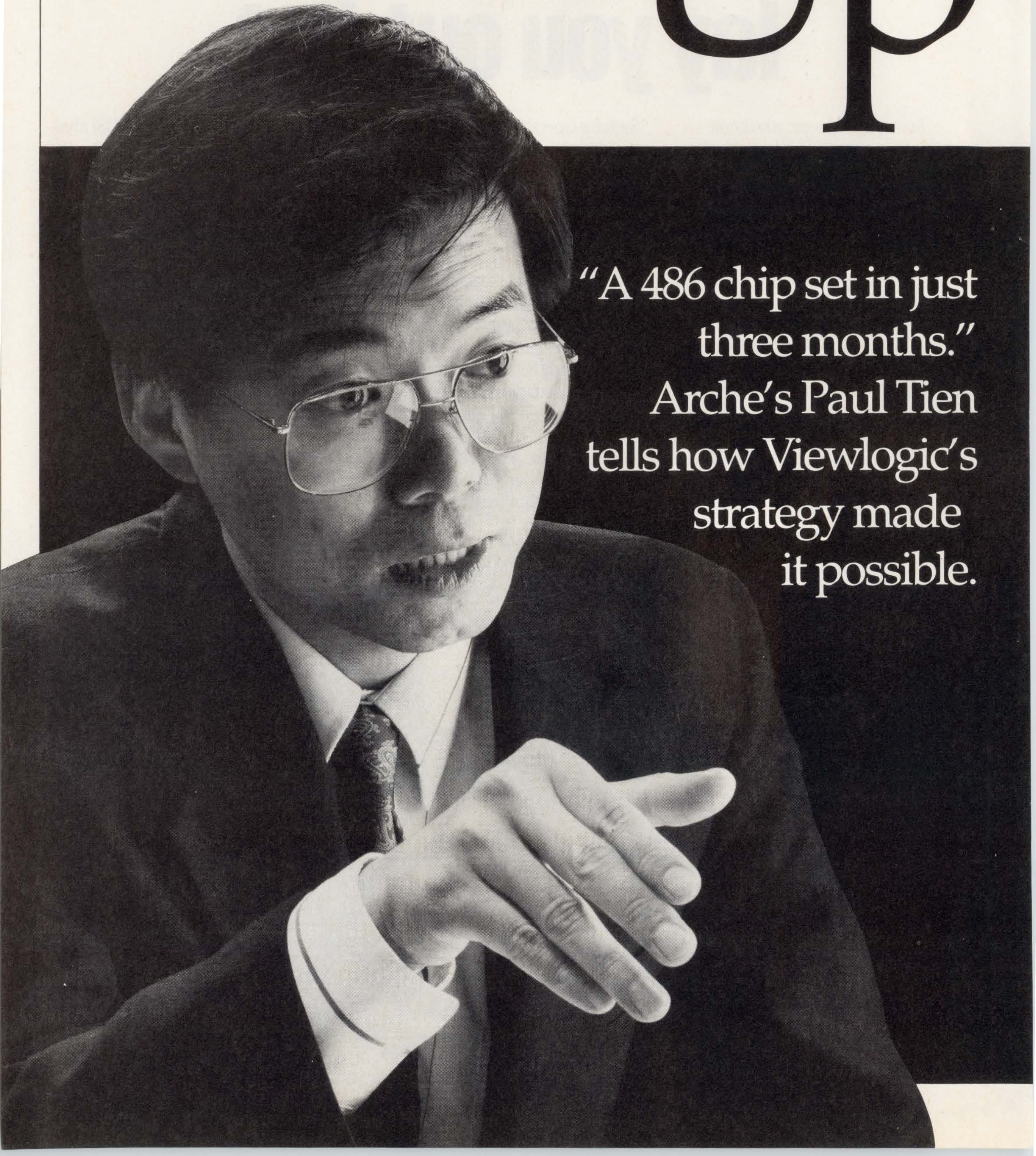
"Up
"A 486 chip set in just three months."
Arche's Paul Tien tells how Viewlogic's strategy made it possible.

FRAMEWORKS: DEBUNKING THE MYTHS

A LOOK AT CAE-ENVIRONMENT BASICS AND TRADE-OFFS LEADS PAST THE HYPE TO A FAIR EVALUATION OF THE SOFTWARE'S CAPABILITIES.

One of the most fascinating aspects of the CAE industry is how quickly a new buzzword finds its way into vendors' glossy literature. The pamphlets unabashedly claim years of market leadership long before the rest of us have settled on a workable definition for the term.

Such is the case with one of the hottest buzzwords around—yes, that's right—framework. If you're a CAE vendor competing for market share, you've just got to have one. Or at least appear to have one. In glossy brochures, customers find myriads of vague descriptions accompanied by colorful screen shots, none of which seem particularly similar to (or different from) each other. From my years of involvement in analysis of CAE vendors to aid strategic planning efforts, I've amassed file drawers of CAE propaganda. Nonetheless, a closer study of framework technology suggests that it will be a key component of CAE environments in the coming years.

Recently, I was amused by a typical CAE brochure espousing the virtues of standards and openness. The vendor claimed that "we support industry standards—only better!" Are frameworks truly "open" or "standard," or do they merely represent the latest marketing ploy? What is a framework? Why does anyone need them?

In the mid-1980s, as CAE tools flooded the market, it seemed engineering productivity fell behind the tools' price tags. The increasing "islands of automation" left users on their own. Vendors had proprietary tools and interfaces that ran on proprietary platforms. The industry needed a structure to handle communication—to the data, to the tools, and to the user. The *tool* orientation began to yield to *process* orientation, which focused on optimizing the entire design process. In this environment, the framework was born.

A framework may be defined as a software infrastructure that provides a common environment for the communication and integration of tools in a process. The tools share the resources of the framework, blurring the traditional concept of a "tool." Ultimately, the engineer doesn't care about tool interfaces

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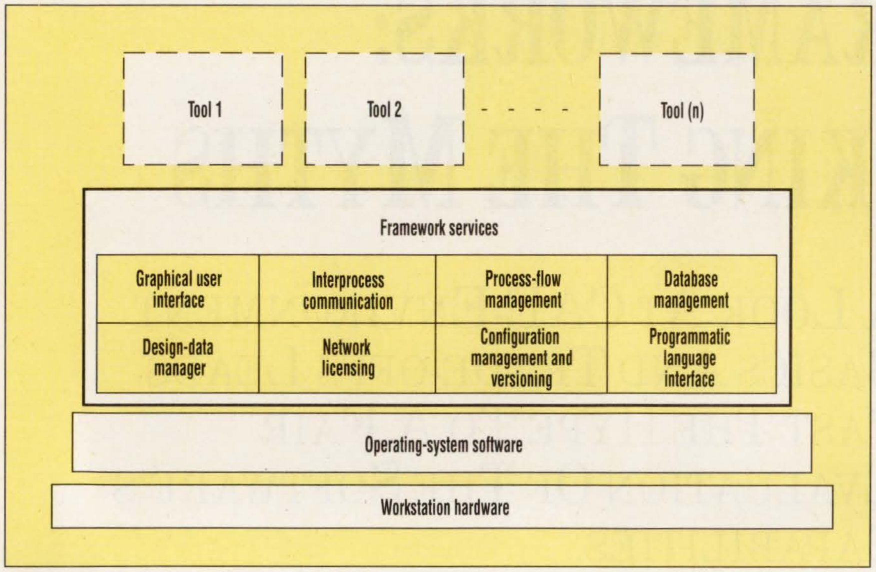
UNDERSTANDING FRAMEWORKS



1. FRAMEWORKS PROVIDE discrete services that interface with the operating system and the tools. Chief among these services is a common user interface.

or even the tools themselves. His sole concern is the results. Therefore, much of a framework's value can't be seen directly. Rather, it's embodied in its effectiveness at meeting quality and cycle-time objectives.

The definition of a framework is vague, so I prefer to think in terms of the services it offers to the tools and the user *(Fig. 1)*. The most conspicuous (and perhaps best-known) service is a common user interface (CUI), which handles keyboard and mouse input to an application in a consistent manner. Nearly all frameworks available on workstations today use a *graphical user interface* (GUI) for this task, such as Motif or Open Look, giving a slick appearance to forms, icons, and gadgets. Meta-functions that operate across tools, such as window sizing, pop-up menus, and on-line help, can share the same graphical appearance regardless of the tool.

Interprocess communication (IPC) allows tools to communicate with each other directly, without the need to access disk files. IPC is used to highlight a selected signal name in multiple tools, or to run some particular task whenever a design is modified. The tools need not reside on the same workstation, or even in the same workgroup. A well-planned methodology built around this concept might permit multiple engineering disciplines to perform parallel design analyses (perhaps automated) without interrupting the primary designer's train of thought.

Process-flow management helps users to properly sequence and invoke tools that use related design data. The mechanics of process-flow management are quite simple, using timestamps on files or ASCII strings extracted from reports. Typically, it's much more difficult to program the rule base upon which the decisions are made. The actual relationships and dependencies among tools are often company-specific, calling for some internal effort to exploit this feature.

Database management stores and retrieves data for the tools using a common database. A common database doesn't need an identical record structure across all tools, but it should provide a standardized means of accessing the data. Several frameworks include databases that recognize whether the most recent version of data resides in memory or on disk, and will handle all paging of data as the tool requests it from the framework. The trade-offs between object-oriented databases (OODB) and relational-database (RDB) technology that must be considered carefully concern their respective performance and/or capacity and adaptability to changing needs. In general, relational databases are better for static data while object-oriented databases may be better for dynamic data types.

A *design-data manager* can complement the database aspects of the framework by giving a users a view into his data on the system. The data is shown grouped in logical clusters that match the engineer's natural way of thinking. Often, the utilities appear as hierarchical, icon-based trees of design data along with icons for available tools.

Network licensing acts as an application broker to a group of workstations within a given network, permitting a tool's authorization key to be "checked out" for use by another workstation. This can be a cost-saving feature for certain high-cost tools that are used occasionally across many nodes. Frameworks adopted this capability from standalone licensing products that have existed for several years.

The importance of *configuration management and version control* has grown in proportion to the complexity of design data and application side files. These functions are critical for frameworks with internal database manipulation, such as an OODB. The versioning must be accurately reflected within special files used by the database manager. These files, containing metadata about the design, are created when a design is imported into its known environment.

A *programming language* is usually included to customize the framework for a particular use. The language may control loosely-coupled interfaces or redefine pop-up menus and forms. Programming is generally required to support custom process-flow management. Most CAE vendors rely on their proprietary languages for all in-house tool integration functions.

Overall, the common goal of these services is to improve productivity by freeing the user from the tedious details of data management and low-level interaction. This isolation-layer

UNDERSTANDING FRAMEWORKS

concept isn't new—consider the example of an operating system. I expect frameworks to become the operating system of the 1990s for engineering tools. If you doubt that a framework approach might ever be considered an operating system, just take a close look at the success of Windows 3.0!

Now to introduce yet another buzzword: concurrent engineering (CE). Most definitions of CE seem to agree on phrases like "simultaneous, parallel design process," "top-down design," and "multi-disciplinary team." It should be emphasized that CE isn't a product, it's a philosophy. The concepts are deeply rooted in the quality, cost, and time-to-market pressures underscored in our current business environment. One tenet of electrical design automation is to move all known design and process constraints to the front of the verification stage, where errors may be corrected faster and more cost effectively by orders of magnitude. This approach is fully consistent with the goals of CE.

Experts on CE generally agree that the four key components of CE are organization, methodology, communication, and requirements. Frameworks provide enabling technology for improved design-data communication, but CE clearly involves much more than what a framework can provide. The full benefit of frameworks (or design automation, for that matter) can only be achieved after a carefully chosen methodology has been defined, communicated, and implemented.

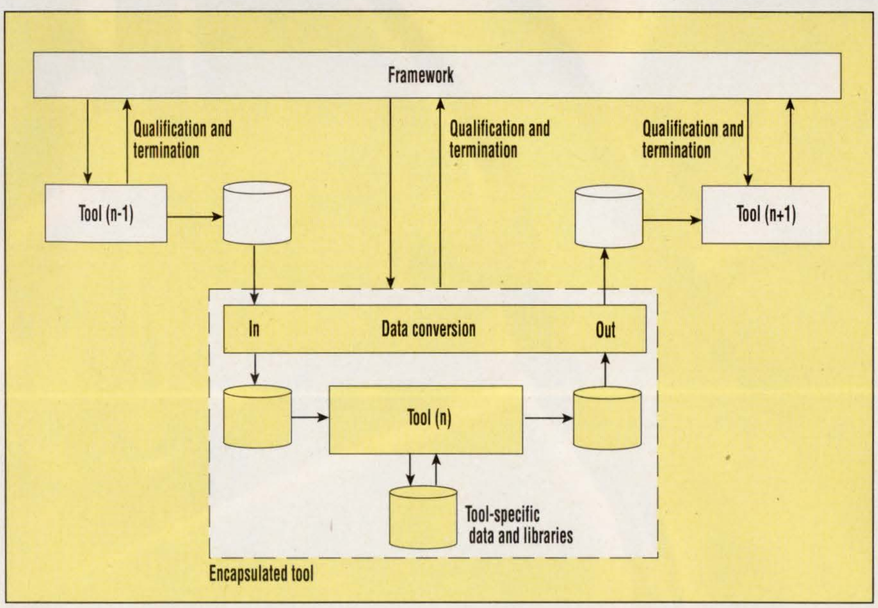
Imagine that you're attending a demonstration by a new upstart CAE company, Me-Too Systems Inc. The factory representatives mention that their new product, Speedy-Sim VHDL, is already integrated with a variety of vendor toolsets, including integration under Eagle—the soon-to-be-released framework from Monolithic Design Systems, their archrivals. How can this be? Is framework integration really that quick and simple?

There's a substantial difference between tool integration, which generally requires custom modification to the code, and tool encapsulation, which can often be done using file-based interfaces. It may be possible for your company to encapsulate Me-Too's new product into Monolithic's framework, once all data flows, such as inputs, outputs, and dependencies, are clearly understood. This would offer macro-level process control for tool invocation, near-transparent data feeds, and perhaps management of files needed and/or produced by Speedy-Sim VHDL. However, the required user interface, database access, and system resources (such as X-windows or Sunview) will remain the same as before. Only planned cooperation between code developers at Me-Too and Monolithic can truly integrate the two separate products into one unified environment.

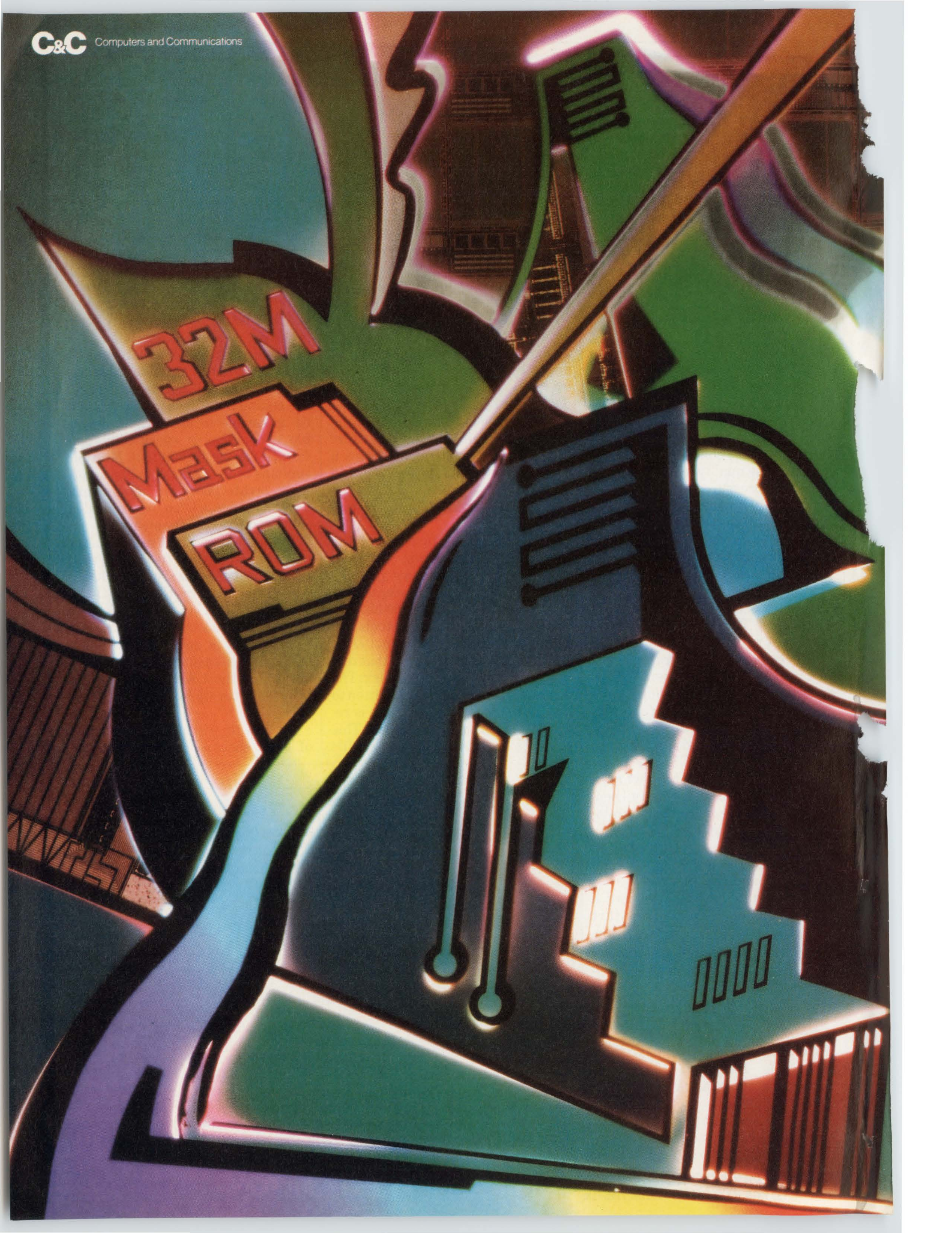
Although integration brings the fastest communication between tools, encapsulation may be adequate for many environments. Often, the framework controls the invocation and sequencing of tools, including the encapsulated tool *(Fig. 2)*. But the process of using that tool in a design flow is more complex. The outputs from tool (n–1) are written to disk as usual, but the file data is reformatted for input to tool (n). This requires the ability to extract file data from tool (n–1), as well as detailed knowledge of tool (n)'s data-input structures. Once the conversion is made, tool (n) may be loaded. No framework services are available during tool execution, such as interaction with other tools (as with IPC). Upon exit, a second converter must reformat the output for use by tool (n+1). Encapsulation of many tools proceeds in a similar fashion. For each encapsulated tool, there may be specific libraries or side files required. Data will not be written to the common database, and will not be accessible to other tools unless file conversion is specifically performed for the second tool. Multiple versions of the same data can sometimes create problems in determining which files to keep for archival or configuration management.

If you've glanced at any industry magazine in the last two years, then you're probably aware that OODB ranks very high on the Buzz-O-Meter, right next to C++. Today's frameworks are based on either object-oriented or relational database technologies, each claiming to be superior for the CAE process. What differentiates these two database approaches?

Let's begin with an understanding of how each is organized. RDBs



2. IN THIS EXAMPLE of a tool's encapsulation under a framework, the framework controls the invocation and sequencing of tools. Conversion of data and tool-specific libraries may be required.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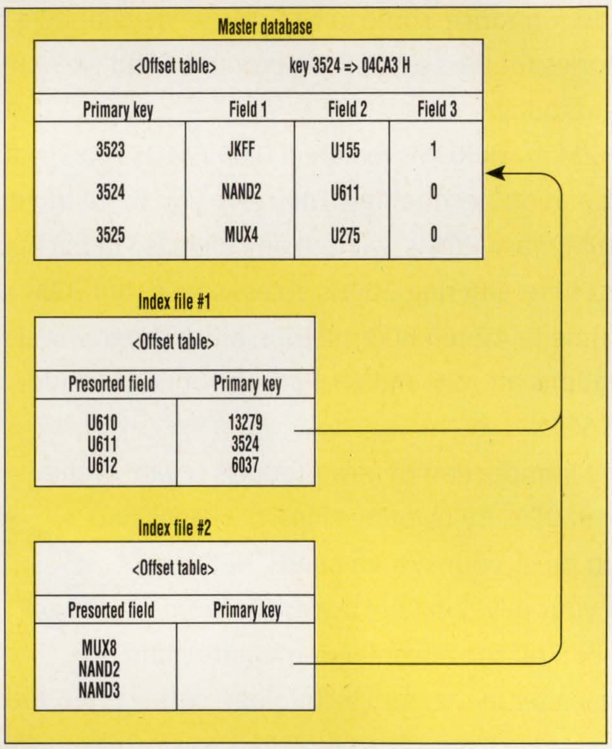
store data in records (also known as tuples) comprising multiple fields. A primary key field guarantees one-to-one mapping with the records entered. Any field may be searched and reported, but sorting may take a long time. Therefore, it's common for additional index files to be created that relate back to the master *(Fig. 3)*. Each index is presorted and filtered in one or more specific fields so as to provide quick, efficient access to the related information in the master database. These index files take a while to build and are usually created in a batch operation. To speed up random access, an offset table in the file header may point to a desired record. It's also common to use a structured query language (SQL) to extract data based upon a set of rules and dependencies. These access languages are relatively fast and efficient.

Object-oriented databases don't use the same record/field format. Instead, they treat information hierarchically, with certain data types belonging to other data types *(Fig. 4)*. This hierarchy extends in n dimensions to accommodate the complex relationships found in simulation of real-world properties. OODBs are characterized by classes, methods, and attributes associated with an instance of a given object type. An object consists of groupings of hierarchical data along with the operations that may be performed on them. The actual value of a property attached to an object need not be embedded into one flat file. OODBs generally use larger quantities of smaller files, each of which may contain one or more objects. Thus, changing one value of any property occurs almost instantaneously, which is much faster than rebuilding an entire RDB.

In addition, OODBs can improve interactive speed by sharing in-memory structures while manipulating data between applications. Persistent objects may be thought of as permanent variables that remember their values upon program reentry. Disk storage of persistent objects may simply mirror the binary in-memory structure. This eliminates massive reformatting of data during disk reads or writes. Tools using an OODB may not even be aware of the existence of a disk other than declaring certain objects as "persistent." Most problems with OODBs arise from a lack of programming experience (mostly in C++) or from performance problems stemming from excessive disk activity.



3. RELATIONAL DATABASES access data based upon a primary key and a set of presorted fields. Any field may be sorted, but doing so may take some time. One way around this problem is to create additional index files that relate back to the master.

As mentioned previously, RDB technology is best suited for static data, and OODB technology is best suited for dynamic data. Both technologies have disadvantages related to the way in which the data is organized and stored. Although CAE data is a mixture of static and dynamic data, most data consists of static information, such as internal part numbers or component-delay values. But as clock rates rise and concurrent-engineering concepts take shape, more accuracy will be required to use dynamic data that changes with the design's evolution. This is a primary driving force toward using OODB in CAE tools.

One goal for both frameworks and concurrent engineering is global optimization, in which small trade-offs in performance, reliability, size, cost, and other factors result in the best overall design. In reality, this goal calls for major cultural changes within most organizations, as well as more specific, rule-based tools that make estimates based upon a design's current state. One CAE framework uses a spreadsheet metaphor to program such rules directly into a flexible tool to support "what-if" analysis. Threshold violations can then be monitored using graphical gadgets like meters, LEDs, or thermometers. The key to this capability is straightforward access to the database from within the cell expressions. An entire new breed of "meta-tools" such as these can be expected to evolve over the next several years. The underlying idea of mathematical or Boolean calculations derived from simple design-database access will be a significant impetus toward global optimization.

If you thought that CAE tools had expanded to consume the maximum possible amount of system resources, think again. Frameworks are additional overhead layers that need lots of processing power, RAM, and disk space to themselves. The extra checks on design rules, database integrity, and so forth all eat up their share of clock cycles. Slower tool invocations should be more than offset by the benefits gained in total simulation-cycle time and support of a desired methodology.

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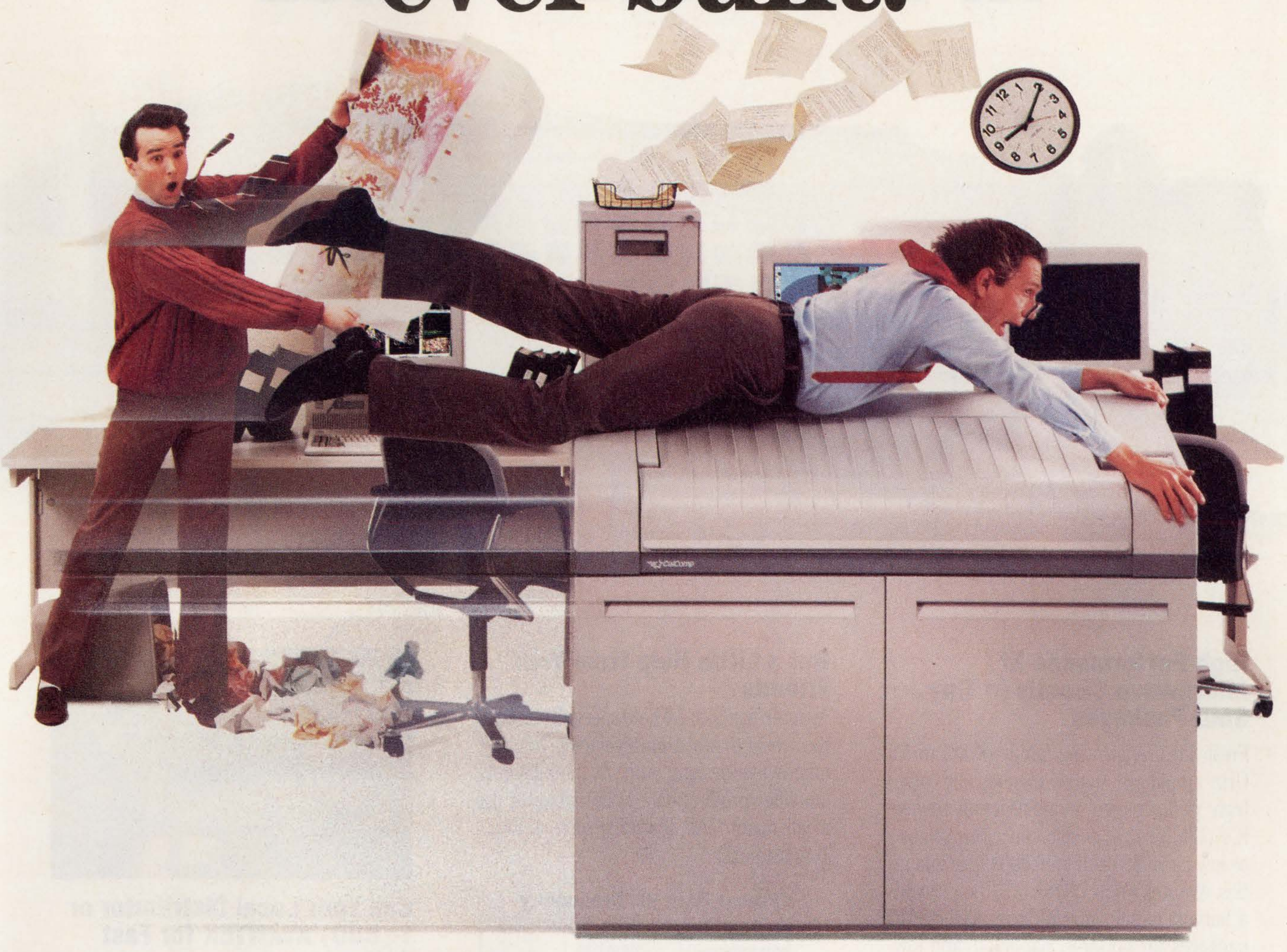

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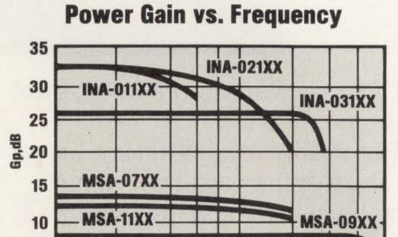

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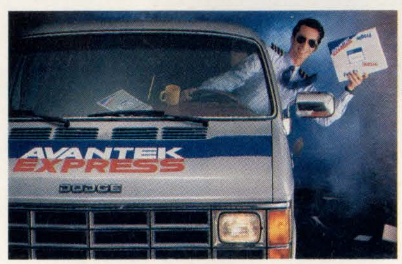

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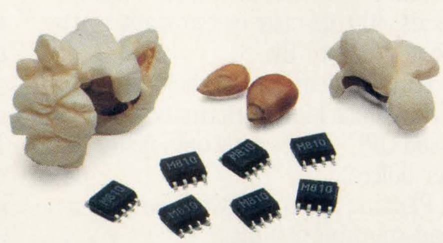

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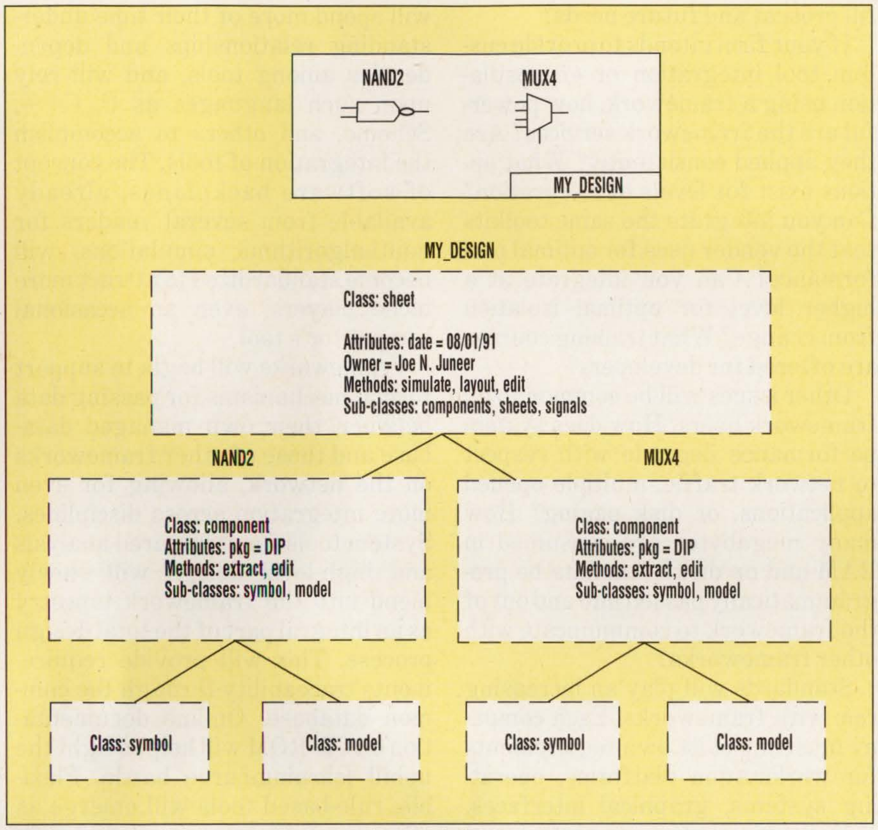

4. OBJECT-ORIENTED DATABASES dynamically arrange data using classes, attributes, and methods in a hierarchical relationship. Because they can share in-memory structures while manipulating data between applications, these databases boost speed.

dors formed the CAD Framework Initiative (CFI) to remove traditional CAD and CAE tool integration barriers. Among the more than 40 organizations represented are tool and workstation vendors, semiconductor suppliers, and end users. Although progress is in the early-definition stages, CFI promises to provide the first truly open protocols for tool communication and bring users one step closer to vendor independence. Achieving vendor independence has been the holy grail of CAE. Even standards accepted throughout the industry are subjected to various forms of distortion, including subset dialects, supersets, and good-old-fashioned ambiguity. Frameworks provide the enabling technology for vendor independence, but solid commitment must come from the CAD/CAE industry to achieve this lofty goal. CFI is an excellent means to that end.

Because frameworks aren't stand-alone tools, many factors must be considered when evaluating framework capabilities, including the intended use within your company. There are essentially three alternatives: (a) try to buy a prepackaged framework complete with all desired tools and interfaces; (b) purchase a do-it-yourself framework product and roll your own tool interfaces; or (c) add new tool interfaces to a prepackaged environment. The following addresses just a few key issues to consider for any evaluation.

If the product is purchased as part of a CAE toolset, what features are provided with the framework and how thoroughly are those features used by the tools themselves? Can the framework services be accessed for tool customization, such as pop-up menus, icons, or supplemental programs to perform company-specific tasks? And if you look beyond the tool capabilities to the overall process flow, does the framework fill present and future needs?

If your firm intends to provide custom tool integration or encapsulation using a framework, how powerful are the framework services? Are they applied consistently? What options exist for levels of integration? Can you integrate the same toolkits that the vendor uses for optimal performance? Can you integrate at a higher level for optimal isolation from change? What training courses are offered for developers?

Other issues will be common to all framework users. How does system performance degrade with respect to network traffic, multiple opened applications, or disk paging? How many megabytes are consumed in RAM and on disk? Can data be programmatically passed into and out of the framework to communicate with other frameworks?

Standards will play an increasing role with frameworks. Each company must select its own requirements for workstation platforms, operating systems, graphical interfaces, X.11 requirements, network protocols, common databases, and many other factors. As CFI evolves, so will the standards for extension languages, IPC mechanisms, file formats, and so on.

If any framework candidates survive such scrutiny, then it's time to arrange for in-house evaluations using real tools, real design scenarios—even real engineers! Most vendors will allow at least 60 days for evaluations, so take the time to develop a formal plan with clear objectives. Give serious consideration to how the framework would be used in your current business climate and to how it might be stressed over the next three to five years. Also, research the vendor for financial stability and trends, future direction, and your firm's ability to influence the product's future direction.

As frameworks begin to take on the real challenges facing them, their true place in CAE history will become evident. I expect it will take several years for CFI to forge a "plug-and-play" tool environment among cooperating vendors, but it'll be well worth the wait. Developers will spend more of their time understanding relationships and dependencies among tools, and will rely upon such languages as C, C++, Scheme, and others to accomplish the integration of tools. The concept of software backplanes, already available from several vendors for multi-algorithmic simulations, will become standardized to attract more niche players, even an occasional competitor's tool.

Frameworks will begin to support formal mechanisms for passing data between their own managed database and those of other frameworks on the network, allowing for even more integration across disciplines. System tools for structured analysis and high-level design will slowly blend into the framework tapestry as an integral part of the total design process. This will provide requirements traceability through the common database. On-line documentation on CD-ROM will help to fight the uphill learning-curve battle. Flexible, rule-based tools will emerge as common engines for monitoring critical design parameters, without the need for brute-force recalculation of every last detail. The soon-to-evolve structured approach to design can lead to reusable design fragments, all categorized by the database in ways that can be queried and referenced by designers on demand.

The time is right for the CAE industry to tackle its communication and interface problems head-on and tear down the walls of proprietary interfaces and dialects that have made "full CAE solutions" so difficult for users to create.☐

Steven E. Schulz, member of the Group Technical Staff and CAE systems engineer in the Automation and Engineering Technology division of Texas Instruments, Plano, Texas, holds a BSEE from the University of Maryland.

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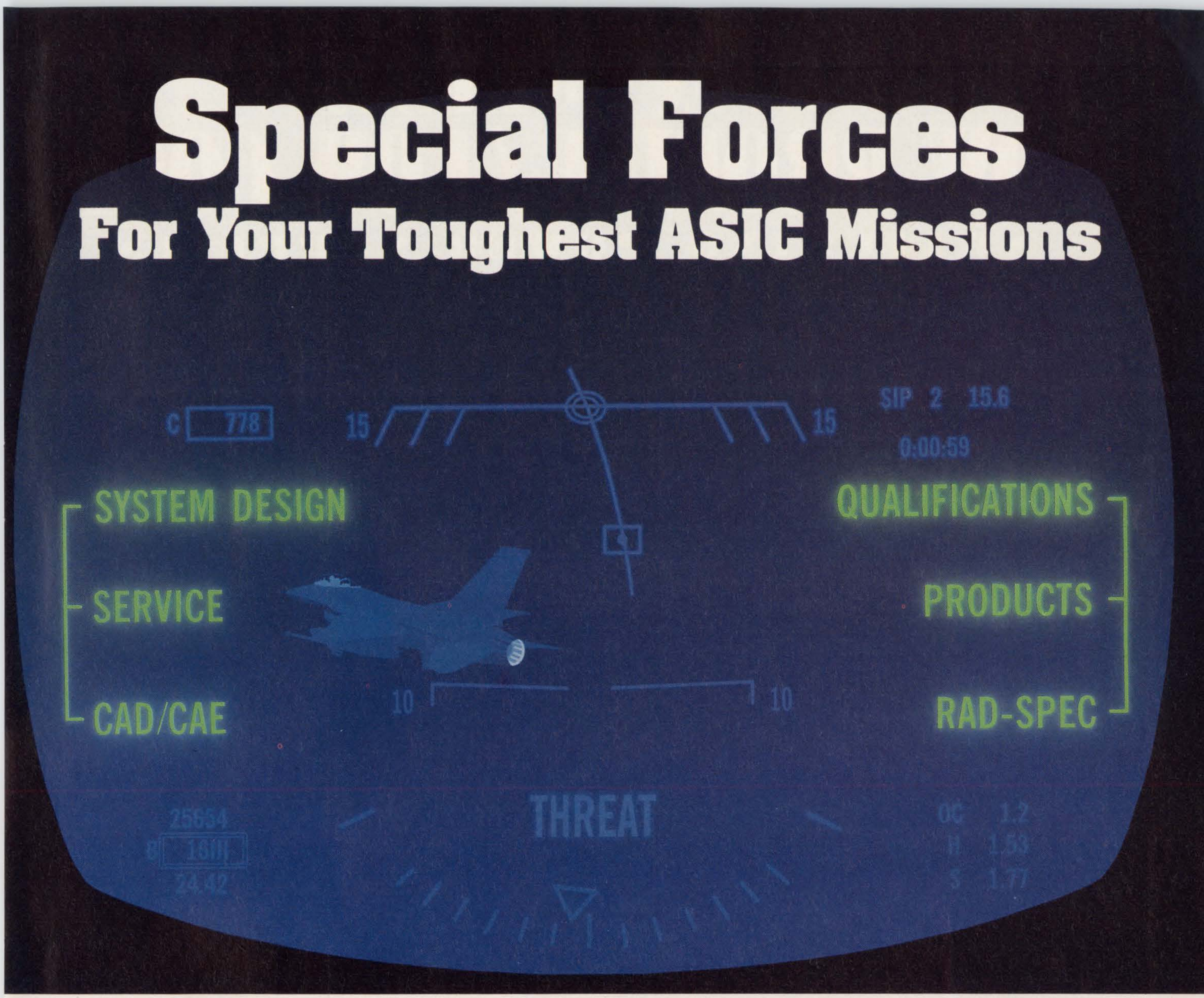

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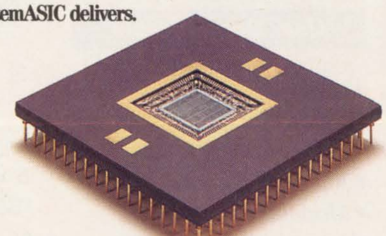

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2x4.5x9"	250W	5V/30A	12-15V/10A	12-15V/3A	5-15V/3A	
2.5x5x10"	400W	5V/50A	12-15V/15A	12-24V/3.5A	5-15V/6A	
2.5x5x10"	400W	5V/50A	12-15V/15A	12-24V/3.5A	2-6V/6A	
2.5x5x11"	400W	2-6V/60A	5-15V/12A	5-15V/12A	2-6V/12A	
2.5x5x11"	400W	5-15V/24A	5-15V/12A	5-15V/12A	2-6V/12A	
2.5x5x11.5"	500W	5V/70A	12-15V/15A	12-24V/3.5A	5-15V/6A	
2.5x5x11.5"	500W	5V/70A	12-15V/15A	12-24V/3.5A	2-6V/6A	
3x5x14.25"	600W	5V/80A	5-24V/10A	5-24V/10A	5-24V/5A	5-24V/5A
3x5x14.25"	600W	5V/100A	5-24V/10A	5-24V/5A	5-24V/5A	
3x8x14.25"	1000W	5V/150A	5-15V/20A	5-15V/10A	5-15V/10A	5-24V/10A

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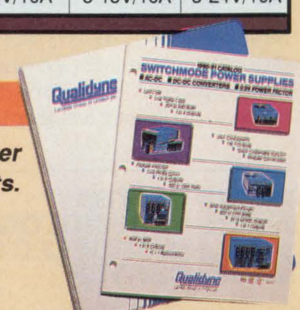

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CIRCLE 166 FOR U.S. RESPONSE CIRCLE 167 FOR RESPONSE OUTSIDE THE U.S.

Increased functionality enhances DMMs

New technology makes an old stand-by more powerful and economical.

BY JOHN NOVELLINO

The digital multimeter (DMM) field may be mature, but it certainly isn't stodgy. As with most test and measurement instruments, the ubiquitous (or nearly so) DMM has experienced a growth in functionality and analysis capability. Increased use of microprocessors makes this higher performance possible, while holding prices at or below those of older, less capable units.

The dynamics of the DMM are changing some of the traditional ways users look at the range of available instruments. The conventional categories are handheld, bench, and system instruments. But some handheld DMMs, which are usually thought of as troubleshooting aids for field technicians, have become capable enough to intrude on the domain of the low-end bench instruments.

On the other hand, the distinction between high-end bench instruments and system units is even more blurred. Many engineers are using system instruments in benchtop applications—that is, setting up the measurement with front-panel controls rather than through a computer interface. These users often need the increased accuracy and resolution typical of system DMMs. In addition, they usually want that interface capability for future use.

In fact, computer interfaces are now offered on many DMMs that would typically be considered bench instruments. "At the higher end, we may never come out with an instrument without IEEE-488 on it," says Gary Pinkerton, marketing manager at Keithley Instruments. "It's not even worth offering the option of not having IEEE-488, even though many customers put the instrument on the bench and don't use the bus. They want to know that if they do want to automate that test in a lab environment, they have the ability to do it."

Although the IEEE-488 bus is still the most popular link, users are increasingly interested in the RS-232 interface. It's not that an RS-232 serial port is any easier to use than the IEEE-488 bus. Rather the RS-232 connection is seen as an economical way to set up a mini-system. Most engineers already have computers with serial ports, making them suitable for instrument control.

Users' changing needs are reflected in movement away from the "vanilla-flavored, one-size-fits-all meters of the past," according to David Haug, a product planner at John Fluke Mfg. Co. "There's a trend toward higher-performance, higher-cost instruments with more features. And then there's a lot of growth at the other end, in instruments with more basic performance," he says. "The trend is toward the two ends, and I guess you'd call it a thinning out in the middle."

As widespread as DMM use has been in the past, the instruments are even more popular now, says Keithley's Pinkerton. And users are getting more for their money than ever before. "DMMs have a lot more functionality in them for a lower price, as most every other product has," notes Pinkerton. "But they've also taken on the functional capability of other products."

For instance, many units now include a reasonably good frequency counter. Also, peak detection, a feature that's usually found in digital oscilloscopes, is now available in a number of DMMs at a much lower cost than an oscilloscope. Some manufacturers are even adding switch matrix cards to their DMMs.

"We found that a lot of our customers need to do multiple-point testing, and plugging a switch card into the DMM lowers their development cost and time considerably," notes Pinkerton. "Ease of use is also significantly better because they have only one instrument to work with."

Today, users can also purchase more performance for the DMM dollar. Engineers who had to settle for 4-1/2-digit resolution a few years ago can now afford to replace that instrument with a 5-1/2- or 6-1/2-digit unit. This price performance improvement is especially important in applications where measurement speed is critical, because resolution is typically traded off for increased speed.

Microprocessors are largely responsible for the DMMs' boost in functionality. As is the case in digital oscilloscopes, more and more DMMs include multiple processors. One device may act as a CPU. A separate microprocessor may be used to ensure that data transfers over the bus are as fast as possible. A third device might be needed to run a more complex, multiline display. By using several dedicated processors, the DMM can perform its newly acquired functions without compromising speed.

Of course, the first consideration when choosing a DMM is whether its performance matches the intended application. The basic specifications include ranges, accuracy, and resolution, plus bandwidth for ac measurements. "Users of high-performance DMMs are much more likely to dive into the specification sheet," says Keithley's Pinkerton. "If it doesn't have that 20 ppm of accuracy on dc, they're not going to look at it." At the high end of the system line, however, users must also look at several other factors, such as the instrument's "intelligence," speed, and trigger capability.

Because a high-end system DMM will most likely be linked to a computer, the instrument's intelligence is important to the overall system performance, according to Dixon Hill, Hewlett-Packard's product manager for DMMs. Users should know how many commands the meter can handle. They should also know whether part of their measurement program can be downloaded into the instrument so that it can run without repeated communication with the host computer, says Hill.

The DMM's cost may be a small fraction of a total measurement setup's price, including the software cost. Therefore, the test engineer needs a DMM that has predictable performance and will behave well on the bus. "They want an instrument that works cleanly on the bus, one that doesn't hiccup or lose commands," says Fluke's Haug. Most major manufacturers offer clean instruments with logical command structures.

Using dedicated processors allows a DMM to perform its newly acquired functions without compromising speed.

The DMM's own speed specifications are the next concern. There are two factors: the instrument's basic measurement speed and how fast the DMM can make function/range changes. The latter is particularly important in automated test setups that will make measurements over a wide range of values or even among different parameters. Together, instrument speed and intelligence will determine the DMM's effectiveness in a system environment.

Finally, a user looking at high-end DMMs should examine the instruments' trigger capabilities. Sophisticated test programs may require multilevel trigger conditions to capture measurements at the desired time or location on a waveform.

Although ease of use is a concern for all test engineers, it's not usually a prime criterion for top-of-line system DMMs. "I think that people are willing to give up some ease of use on the high end for more measurement sophistication," says Hill.

But at the next tier, the middle-level system DMMs, users expect more ease of use. "I don't need all that speed and sophistication and maybe not the linearity and the stability that I need on the high end," explains Hill. "But I want something more than just the basic product." Though their specifications will be a little looser, these middle-level instruments can include such features as internal switch cards and the ability to download subroutines.

On the other hand, low-end system DMMs consist of "workhorse products" that make the standard voltage, current, and resistance measurements, says Hill. Engineers using these instruments typically make lots of measurements from the front panel, even though the meters can be linked to computers and used in a rack-mounted system. Hill notes that feedback from buyers of HP's entry in this category, the HP 3478, shows that 70% of them are used on benches rather than in systems.

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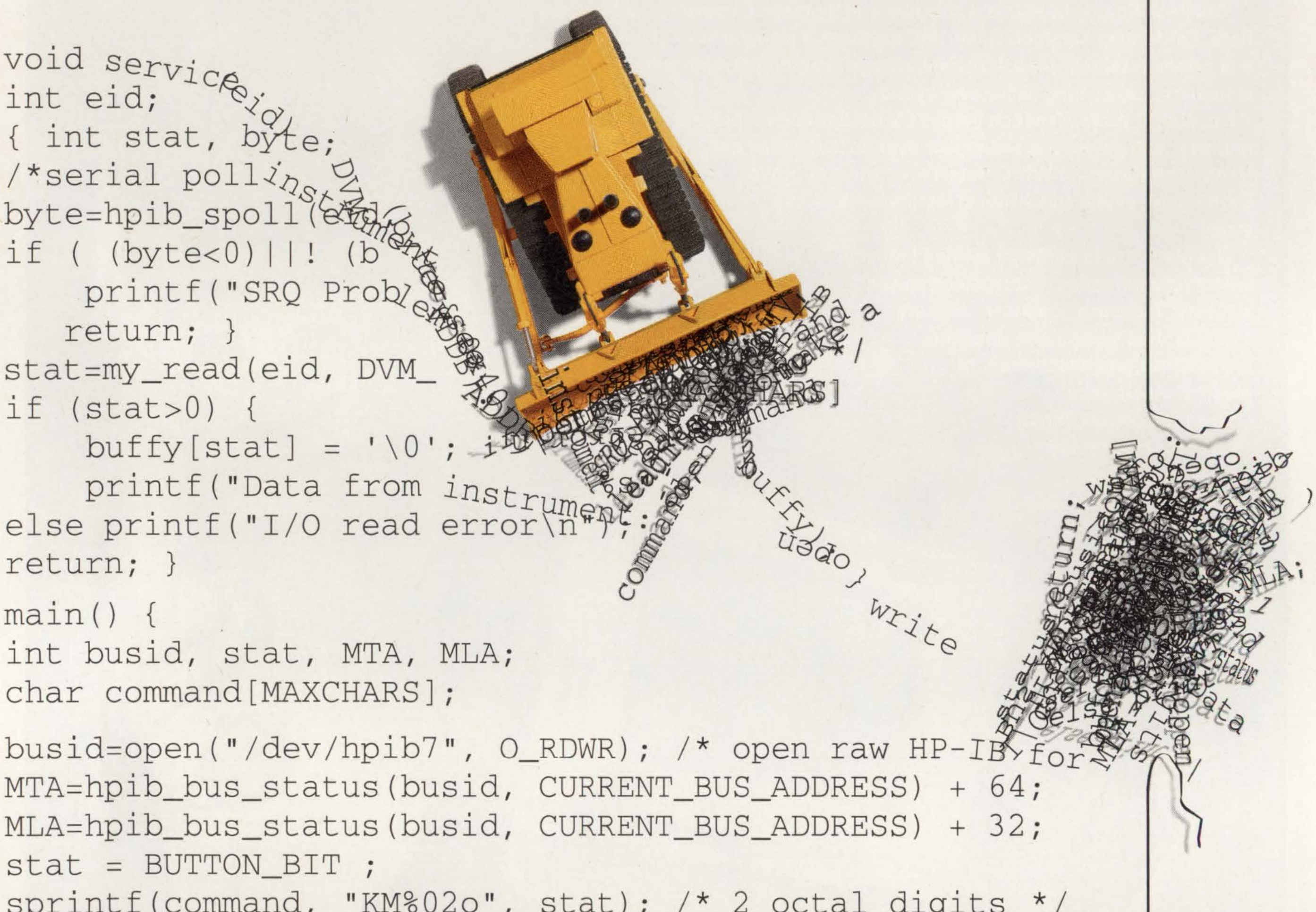

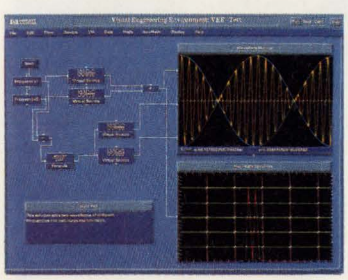

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Wring The Most Performance From Your DMM

Users must learn how to take advantage of today's more powerful DMMs.

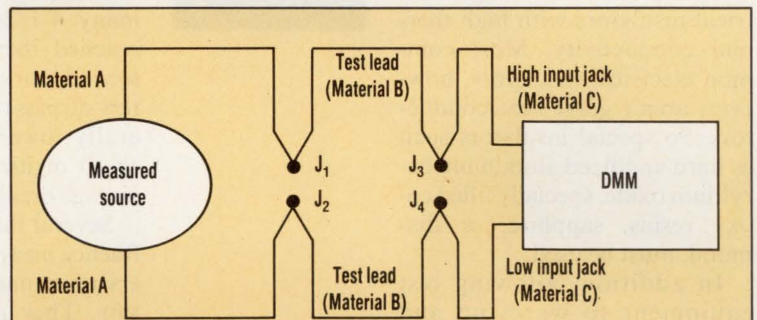
BY DALE CIGOY

Keithley Instruments Inc., 28775 Aurora Rd., Cleveland OH 44139; (216) 248-0400.

Modern digital multimeters (DMMs) offer more sensitive measurements and more sophisticated features than ever before. The measurement realm of the DMM now includes lower voltages (microvolt to nanovolt), lower currents (nanoamp), and higher resistances (100 MΩ). The instruments make these measurements with a wide variety of speed options, resolutions, filters, noise reduction techniques, programmable integration, internal memory, and multiplexing features. But to take advantage of these exceptional specifications and features, users must employ new techniques. Simply connecting test leads to a circuit may not be enough to obtain the specified accuracy.

For potentials greater than a few millivolts, dc voltage measurements can be made by setting the voltmeter to the proper range, connecting the input leads across the potential in the circuit, and reading the display. But a number of applications—including thermocouple measurement, superconductivity, and standard-cell comparisons—involve measurements in the sub-millivolt range. Achieving the needed accuracy and resolution at these lower voltages requires not only higher-performance DMMs, but also more sophisticated techniques.

Resolution isn't the only factor to consider when measuring voltages at this level. A 6-1/2-digit DMM with a 200-mV range could resolve 200.0000 mV. The least significant digit on the display is 100 nV. On the other hand, 7-1/2-digit and 8-1/2-digit DMMs typically offer a sensitivity of 10 nV. So the resolution of an 8-1/2-digit meter is 100 times that of a 6-1/2-digit meter, but the sensitivity is only better by a factor of 10. The result is an effective resolution lower than the specified resolution on the most sensitive range *(Table 1)*. On higher voltage ranges the difference isn't as noticeable.



1. If the circuit test points, test leads, and DMM input jacks are made of dissimilar materials, four thermocouple junctions result. Temperature gradients across these junctions can cause measurement inaccuracies.

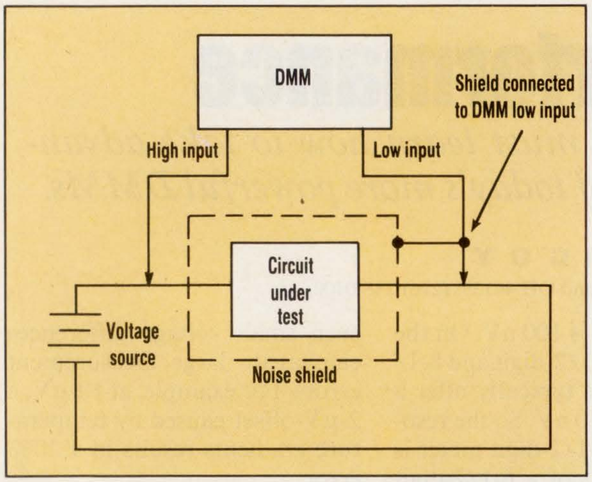
The effect of the test setup must also be considered. For low-voltage measurements, thermoelectric voltages are the most common source of error. These voltages occur when conductors made of dissimilar materials are joined together and a temperature gradient exists between them. For example, if the circuit test points, the test leads, and the DMM input jacks are of dissimilar materials, four thermocouple junctions are created. Differential heating of junctions J_1 and J_3 with respect to J_2 and J_4 generates thermal voltages that appear in series with the source's voltage *(Fig. 1)*.

In the sub-millivolt range, even small voltage differences can create large measurement errors. For example, at 10-μV, a 2-μV offset caused by temperature gradients results in a 20% error.

A copper-to-copper junction has the smallest thermoelectric potential. But a typical junction of a test lead made of stranded copper wire and a beryllium-brass jack could produce several microvolts of offset. Therefore, constructing test setups with conductors of similar materials would be an ideal solution.

If this isn't possible, other steps can be taken. For instance, low-thermal cadmium-tin solder has a thermal EMF 10 times lower than that of lead-tin solder. In addition, connections made by crimping copper sleeves and lugs results in cold-welded copper-to-copper junctions that generate even less thermal EMF *(Table 2)*.

Obviously, temperature gradients within the test setup should be minimized. Test leads, cables, and fixtures should ideally reach thermal equilibrium with the DMM and



2. A simple but effective shielding technique is to enclose the circuit under test in a metal box, which is connected to the low input jack.

other test instruments. One technique is to place all junctions in close proximity and provide good thermal coupling to a common, massive heat sink. Coupling must be through electrical insulators with high thermal conductivity. Most common electrical insulators, however, aren't good heat conductors. So special insulators such as hard anodized aluminum, beryllium oxide, specially filled epoxy resins, sapphire, or diamond, must be used.

In addition, allowing test equipment to warm up and reach thermal equilibrium in a constant ambient temperature minimizes thermal EMF effects. When the test system is in thermal equilibrium, any remaining thermal EMF will be relatively constant with respect to time. Therefore, it can be compensated by zero controls on the instrument. To keep the ambient temperature constant, equipment should be kept away from direct sunlight, air-conditioning ducts, and similar sources of hot or cold air. Wrapping connections in insulating foam, such as polyurethane, also minimizes temperature fluctuations due to air movement.

To summarize, engineers can diminish thermal effects in high-performance DMMs by following some simple rules. The high- and low-connection test lead wires should be made of the same material, the temperature differentials across the measurement system should be lessened, and the DMM should be allowed to stabilize on the required range for about five minutes. Moreover, the proper measurement range should be used to avoid overloading the attenuator components. Users should also periodically inspect connections and remove copper oxide or other corrosion products that will create thermal EMFs.

As mentioned earlier, today's DMMs run much faster than their counterparts of just a few years ago. A typical 4-1/2-digit multimeter in the early 1980s could make fewer than 10 readings per second. In the late 1980s, speed increased to about 100 readings per second. Today, many 4-1/2-digit meters have reached the 1000 reading per second mark. In fact, some meters surpass this, but they're generally lower-resolution, high-speed digitizers such as digital storage oscilloscopes.

Several factors, however, influence measurement speed. Users must understand these factors. They must also comprehend how the measurement setup affects them and, therefore, the actual measurement speed that can be attained.

One important consideration is analog settling time. Because connecting a multimeter to a device under test causes a step change in the measurement circuit, a transient with the standard RC time constant will result. The resistance is typically the input resistance of the multimeter and other stray resistance. The capacitance is distributed capacitance due to the multimeter, the cabling, and other components. For an accurate reading, several time constants must elapse between the connection of the instrument and the measurement conversion.

Filter settling time must also be considered. Because any filtering done by the multimeter is subject to transients in the measurement circuit, the input filter must stabilize before an accurate measurement can be made. Finally, once the signal and filter have stabilized, the analog-to-digital conversion time will affect the time required to make a measurement.

To take advantage of a DMM's high specified measurement speed, users must configure the meter in certain functions and modes. In general, the top speeds are attainable only at the meter's lower resolutions and only when storing data into internal memory.

As noted, the status of the measurement filter, whether analog or digital, affects the DMM's speed. And users should know that the filter may be enabled without their knowledge. For example, some meters have an internal filter in addi-

TABLE 1: SPECIFIED VERSUS EFFECTIVE RESOLUTION

Specified resolution	Performance	Sensitivity	Noise floor	Effective resolution*
$5^1/_2$	Low	1 μV	10 μV	$4^1/_2$
$5^1/_2$	Typical	1 μV	5 μV	$5^1/_2$
$5^1/_2$	Best	100 nV	2 μV	$5^1/_2$
$6^1/_2$	Low	1 μV	10 μV	$5^1/_2$
$6^1/_2$	Typical	100 nV	3 μV	$6^1/_2$
$6^1/_2$	Best	100 nV	2 μV	$6^1/_2$
$7^1/_2$	Low	100 nV	4 μV	$5^1/_2$
$7^1/_2$	Typical	10 nV	1.2 μV	$6^1/_2$
$7^1/_2$	Best	10 nV	800 nV	$6^1/_2$
$8^1/_2$	Low	100 nV	1 μV	$6^1/_2$
$8^1/_2$	Typical	10 nV	200 nV	$7^1/_2$
$8^1/_2$	Best	10 nV	100 nV	$7^1/_2$

*Usable resolution without the noise floor tion to a "front-panel" filter. An indicator light normally shows whether the front-panel filter is enabled.

An internal filter, which is usually enabled in the high-resolution modes, ordinarily doesn't have a front-panel indicator. In fact, users may not know that the meter has an internal filter or when it's enabled unless they check the instrument's instruction manual. As a result, high-resolution readings are typically slower than low-resolution readings. But an enabled filter will slow down both high- and low-resolution measurements.

DMMs use several types of analog-to-digital converters (charge balance, dual slope, recirculating remainder, etc.), although most are variations on the integrating converter. The integrating ADC cycle includes several phases:

1. During the *reference phase*, the converter checks the reference voltage.
2. In the *signal phase*, the device integrates the signal in the prescribed time.
3. In the *zero phase*, it checks the value of zero for offset correction.
4. Finally, the converter takes all of the data from each phase and *calculates* the reading.

Normally, the DMM uses a multiplexing scheme to route signals through these phases. Some meters let users eliminate the reference and zero phases, which increases the conversion speed considerably. However, if the reference and zero aren't checked on each conversion, the measurement may drift over a period of time. For fast reacting experiments, this usually isn't a problem. To optimize performance, users should stabilize the circuit by allowing the multimeter to warm up and reach thermal equilibrium. At thermal equilibrium, there's less drift on the measurement.

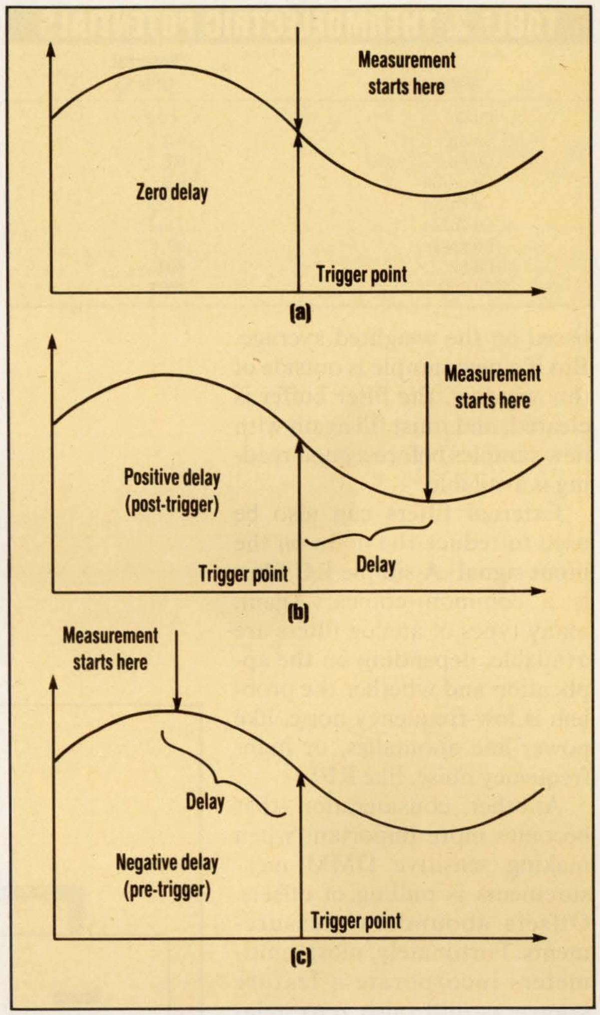
External interference, or noise, at the DMM's input can also adversely affect measurements. The general term for electromagnetic interference over a wide range of frequencies is radio-frequency interference (RFI). RFI can be particularly troublesome at low signal levels, but a severe RFI problem can also affect measurements at high signal levels. The high input impedances of high-end DMM's—10 GΩ on some ranges—aggravate RFI problems.

RFI is caused by such sources as radio or TV signals and some types of electronic equipment, including microprocessors and high-speed digital circuits. Interference also results from impulse sources, like arcing high-voltages. Even ac line voltages can cause interference in some environments.

Shielding is a good way to stop electromagnetic fields from interfering with the measurement. Shields can be built to enclose the circuit being measured, the measuring instrument, and even the person running the experiment. Generally, however, shielding the circuit under test and the measurement equipment is sufficient.

A simple metal box enclosing the circuit under test is probably the easiest shielding technique. The box can be built as an extension of the meter's low-input connector, with that lead connected to the metal shield *(Fig. 2)*. If circuit low is not floating above ground, the shield may also be connected to earth ground for safety purposes. Using a coax cable to surround the DMM's high input is also a good idea.

Noise that does get to the input can be filtered by either internal or external filters. Numerous filter types can be used—weighted average, running average, and exponential filters, for example. Each type has its own special attributes, so filters should be chosen based on



3. Some more sophisticated DMMs include a trigger delay feature. Users can then start the measurement at the trigger point (a), after the trigger (b), or before the trigger (c).

the characteristics of the signal from the circuit under test.

As noted, however, filters decrease measurement speed and reduce response time. The effect on measurement speed depends on the type of filter employed. For example, a running-average filter averages a number of samples to get one "good" reading. The filter buffer must fill before the readings are averaged. This delays the first good reading, but after the filter buffer is full, the meter runs at the programmed speed.

To hasten the response to large step changes, some filters place a "window" around the displayed average. As long as the new samples being stored in the filter buffer are within this window, the displayed value is

TABLE 2: THERMOELECTRIC POTENTIALS

Materials	Potential (μV/°C)
Cu-Cu	<0.2
Cu-Ag	0.3
Cu-Au	0.3
Cu-Cd/Sn	0.3
Cu-Pb/Sn	1 to 3
Cu-Cu/Zn	1 to 3
Cu-Kovar	40
Cu-Si	400
Cu-CuO	1000

based on the weighted average. But if a new sample is outside of this window, the filter buffer is cleared, and must fill again with new samples before a good reading is available.

External filters can also be used to reduce the noise on the input signal. A simple RC filter is a common choice. Again, many types of analog filters are available, depending on the application and whether the problem is low-frequency noise, like power-line anomalies, or high-frequency noise, like RFI.

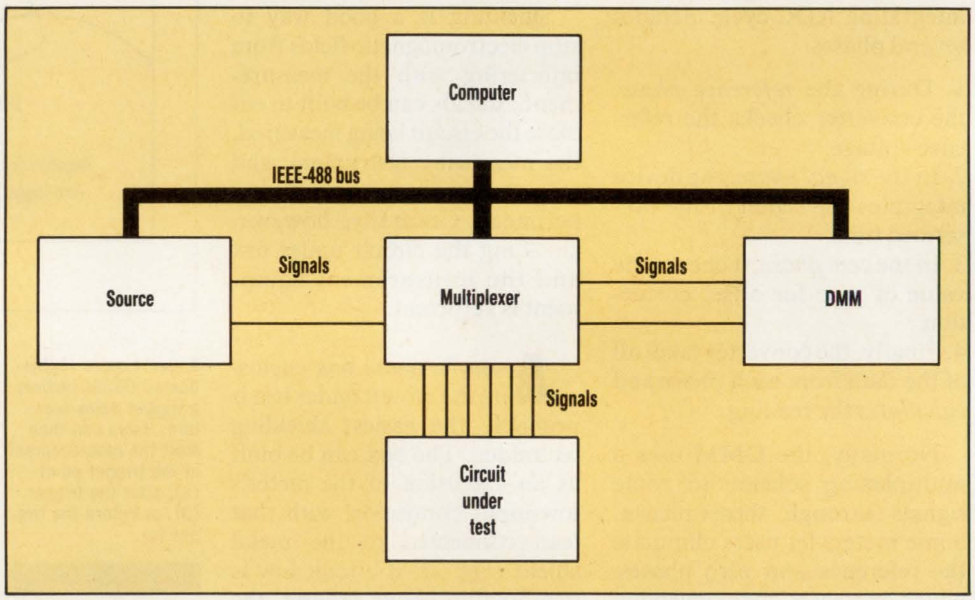
Another consideration that becomes more important when making sensitive DMM measurements is nulling of offsets. Offsets abound in measurements. Fortunately, most multimeters incorporate a feature known as null (also zero, relative, or suppress), which "nulls out" the offset of the measurement circuit. Users must exercise care when they want to check the null with such factors as time and range.

The simplest explanation of offsets and how they are nulled may be for low-resistance measurements. Shorting the test leads together shows the test-lead resistance on the display. Using the null feature cancels the test-lead resistance and subtracts this "offset" from every subsequent reading. The process is similar for other DMM measurement functions: dc and ac voltage, and dc and ac current. Some meters, however, require that the null feature be used for each range to achieve specified accuracy.

The procedure to ensure that offsets are properly nulled is fairly standard:

1. Disable the null feature.
2. Select the range that will be used.
3. Connect the test leads to the DMM input. If four-wire resistance measurements are to be made, short all four wires together at the measurement point. Allow the thermal EMFs to stabilize. For higher-resolution meters (6-1/2 digits and above), Kelvin test leads or shielded leads should be used where appropriate.
4. Enable the null feature.
5. Remove the short and connect the test leads to the signal or resistance to be measured.

Although each step of this procedure is important for proper zeroing, it's especially critical to allow the reading to stabilize. Otherwise, the measurement could drift over time, because the zero value would remain constant but the offset would still be changing.



4. For more complex or repetitive measurements, a systems approach may be best. Typically, the DMM and other instrumentation is connected to a computer that acts as a controller.

A relatively new feature found on more sophisticated DMMs is pre- and post-trigger capability. In the past, this feature was exclusive to digital storage oscilloscopes (DSOs). But the speed of high-end DMMs has increased to where they resemble a DSO, although with a much lower bandwidth. As a result, users can set the meter to trigger at a certain point on the input signal, but either delay the meter from starting the analog-to-digital conversion or analyze the signal just prior to the trigger.

The relevant parameter is the trigger delay, which tells the instrument where to begin storing readings relative to the trigger point. If the trigger delay is zero, no delay occurs. If the parameter is negative, then pre-triggering will occur and the meter will store readings taken just before the trigger point. If the parameter is positive, post-triggering is in effect and the measurement sequence begins at a programmed time after the trigger *(Fig. 3)*.

Finally, engineers involved in test and measurement should consider a systems approach to DMM setups. Although virtually any measurement can be made manually using simple instruments, in some cases it takes a considerable amount of work. Often, a systems approach—connecting instruments together through the IEEE-488 bus and using a computer as a con-

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■ DMM CAPABILITIES ■

troller—is a better solution.

For instance, data obtained from such a setup can be stored, modified, used in calculations, and output to other devices. Not only can the automated system collect data much faster than a manual system, the computer's data-processing ability can eliminate the need for manual computations.

Also, eliminating the laborious, time-consuming task of setting instruments by hand should reduce the number of mistakes. Carefully written software can virtually eliminate errors. And with the proper software, repetitive test procedures can be completely automated. This is especially useful in production testing, when many components or assemblies must be tested. Once a test procedure is automated, little operator skill is required to perform complex tests. Typically, only a simple go/no-go signal is needed.

In general, the systems approach requires the user to think through the measurement sequence, connections, and accuracy requirements. A key consideration is selecting the appropriate instruments. Although systems vary from application to application, they generally involve connecting all devices to one bus, with the inputs and outputs in the appropriate locations *(Fig. 4)*. Though various instrumentation buses have been developed, the IEEE-488 bus is the most widely used for multimeters.

Dale Cigoy, an applications engineer at Keithley Instruments, received his bachelor's degree in electronic engineering technology from Capitol College, Laurel, Md.

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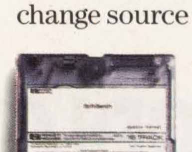

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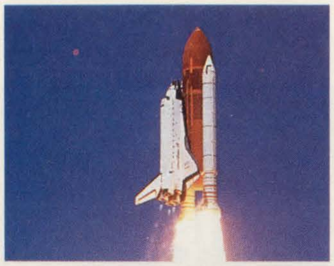

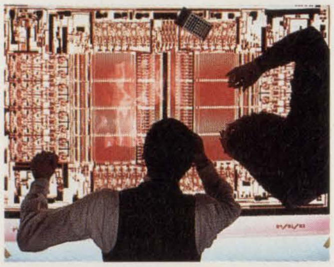

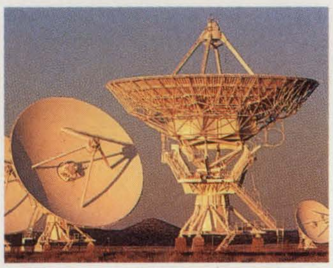

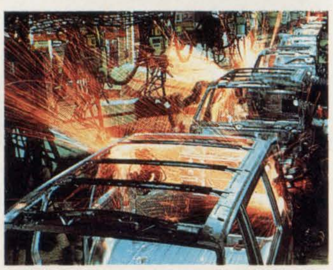

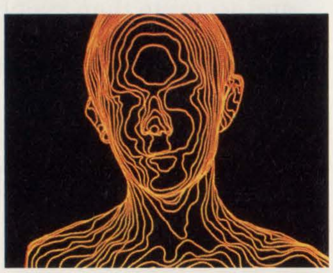

DIGITAL MULTIMETERS

Manufacturer	Model/Price	Digits/ Frequency[1]	Dc volts/amps Accuracy[2] (V/A)	Dc volts/amps Max (V/A)	Ac volts/amps Accuracy[2] (V/A)	Ac volts/amps Max (V/A)	Resistance Accuracy[2]	Resistance Max (MΩ)	Remarks
American Reliance Inc. 9952 E. Baldwin Pl. El Monte, CA 91731 (800) 654-9938 (818) 575-5110	160H/ $89.95	3 1/2/ 50–1000 Hz	0.5%	1000/10	1%	750V/10	0.5%	20	
	3000/ $129.95	3 3/4/ 50–1000 Hz	0.5%	1000/20	1%	750/20	0.3%	40	
	170NL/ $149.95	3 1/2/ 50–1000 Hz	0.1%	1000/10	0.5%	750/10	0.25%	20	True RMS.
	3010/ $149.95	3 3/4/ 50–1000 Hz	0.25%	1000/20	1%	750/20	0.3%	40	4-MHz counter.
	250NL/ $199.95	4 1/2/ 50–1000 Hz	0.05%	1000/10	0.5%	750/10	0.1%	20	True RMS.
	3100/ $199.95	3 3/4/ 50–1000 Hz	0.25%	1000/20	1%	750/20	0.3%	40	400μA and 4 mA ranges; drop proof.
	700T/ $199.95	4 1/2/ 50–1000 Hz	0.05%	1000/10	0.5%	750/10	0.1%	20	True RMS; 200-kHz counter.
	3200/ $229.95	3 3/4/ 50–1000 Hz	0.25%	1000/20	1%	750/20	0.3%	40	Contamination- and water resistant.
	3130/ $239.95	3 3/4/ 50–1000 Hz	0.25%	1000/20	1%	750/20	0.3%	40	4-MHz counter; capacitance measurement.
Analogic Inc./Data Precision 8 Centennial Dr. Peabody, MA 01961 (508) 977-3000	DP100/ $595	5 1/2/ 20 Hz–50 kHz	0.003%/ 0.05%	450/2	0.25%/0.6%	450/2	0.007%	20	True RMS; 25-MHz counter; RS-232; digital filter; 4-wire resistance.
Beckman Industrial Corp. 3883 Ruffin Rd. San Diego, CA 92123-1898 (619) 495-3200	DM27XL/ $109	3 1/2/ 45 Hz–500 Hz	0.5%±1/ 0.75%±1	1000/10	1.2%±3/ 1.8%±4	750/10	1.2%	2000	20-MHz counter; capacitance measurements.
	RM2725/ $149	4/ 45 Hz–30 kHz	0.25%±3/ 0.75%±8	1000/10	2.5%±8/ 1.7%±8	750/10	0.5%±1	40	True RMS.
	HD153/ $169	3 1/2/ 45–1000 Hz	0.25%±1/ 0.75%±1	1500/10	0.75%±3/ 1.5%±2	1000/10	0.5%±2	20	Transient, overload protection; waterproof.
	HD110/ $209	3 1/2/ 45–5 kHz	0.25%±1/ 0.75%±1	1500/10	0.75%±3/ 1.5%±3	1000/10	0.5%±1	20	Same as HD153.
B&K Precision 6470 W. Cortland St. Chicago, IL 60635 (312) 889-1448	2703/ $44	3 1/2/ 50–500 Hz	0.8%	1200/10	1%	850*/10	1%	20	Diode test; *RMS.
	2802B/ $64	3 1/2/ 40–500 Hz	0.7%	700/ N.A.	2.3%	700*/N.A.	2%	20	Probe style; diode test; data hold; *peak.
	2704/ $65	3 1/2/ 50–500 Hz	0.5%	1200/10	1%	850*/10	1%	20	Capacitance diode, transistor tests; *RMS.
	2701/ $69	3 1/2/ 40–500 Hz	0.5%	1100/ 0.25	1.25%	1100*/ 0.25%	0.75	2	*RMS.
	2905/ $79	3 1/2/ 40–1000 Hz	0.5%	1200/10	1.25%	850*/10	0.7%	20	Capacitance, diode, transistor tests; *RMS.
	340A/ $95	3 1/2/ 50–60 Hz	N.A.	N.A.	1%	850/300	1%	0.002	Data hold; ac clamp meter.
	2860/ $99	3 1/2/ 40–500 Hz	0.5%	1200/20	1.25%	750*/20	0.75%	20	Diode test, *RMS.
	2906/ $99	3 1/2/ 40–1000 Hz	0.25%	1200/10	1%	850*/10A	0.5%	20	Diode, transistor, temperature tests; *RMS.
	2911/ $99	3 3/4/ 45–1000 Hz	0.5%	1200/10	2%	850*/10	1%	40	Diode testk; bar graph; *RMS.
	377/ $99	3 1/2/ 50–500 Hz	0.5%	1000/10	1%	750*/10	1%	2000	200-kHz counter; *RMS.
	350A/ $120	3 1/2/ 40–500 Hz	0.5%	1200/ 1000	1.2%	850/1000	1.2%	0.2	Clamp meter; peak and data hold; diode test.
	388-HD/ $129	3 1/2/ 40–1000 Hz	0.5%	1200/20	1.25%	800*/20	0.75%	2000	200-kHz counter; *RMS.
	2912/ $149	3 3/4/ 40–500 Hz	0.3	1200/10	1	850*/10	0.3	40	400-kHz counter; *RMS.
	2940/ $160	4 1/2/ 40 Hz–5 kHz	0.05	1200/20	0.75	850/20	0.1	20	Diode test; data hold; 200-kHz counter.

(see p. 102 for key) *(continued on p. 96)*

▼ SCSI TESTER STRESSES TARGET DEVICES

The INI-350 SCSI initiator/error generator performs comprehensive stress tests on all types of SCSI targets, including disk and tape drives, printers, and processors. The system works with SCSI-1 and SCSI-2 devices, executing standard commands as well as custom commands or command formats. Using an NCR 53C700 SCSI chip, the INI-350 handles transfer rates up to 6 Mbytes/s in synchronous mode and 5 Mbytes/s in asynchronous mode. The instrument can generate a wide variety of error conditions to test the full range of hardware or software conditions in the target and to simulate awkward initiator timings. The INI-350 is available now at a price of $4900.

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▼ DEBUG TOOL OFFERS GRAPHICAL INTERFACE

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DIGITAL MULTIMETERS

Manufacturer	Model/Price	Digits/ Frequency[1]	Dc volts/amps Accuracy[2] (V/A)	Dc volts/amps Max (V/A)	Ac volts/amps Accuracy[2] (V/A)	Ac volts/amps Max (V/A)	Resistance Accuracy[2]	Resistance Max (MΩ)	Remarks
B&K Precision 6470 W. Cortland St. Chicago, IL 60635 (312) 889-1448	2907/ $195	3½/ 40–1000 Hz	0.1	1200/10	0.75	850*/10	0.2	20	*True RMS; capacitance diode, logic tests.
	2832/ $195	3½/ 45–500 Hz	0.5	1000/20	1	1000*/20	0.75	20	Capacitance, diode tests; *RMS.
	2945/ $259	4½/ 40 Hz–5 kHz	0.05	1200/20	0.75	850/20	0.1	20	*True RMS; diode test; 200-kHz counter.
	2831A/ $295	3½/ 40 Hz–40 kHz	0.1	1200/20	0.5	1000*/20	0.2	20	Diode test; ac voltage to 40 kHz; *RMS.
	2833/ $356	4½/ 40 Hz–50 kHz	0.05	1000/20	0.5	1000*/20	0.1	20	*True RMS; 200-kHz counter; diode test.
Datron Instruments Ltd. (Wavetek) Hurricane Way Norwich Airport Norwich, Norfolk NR6 6JB UK 011-44-603-404824	1362/ $4065	6½/ 10 Hz–1 MHz	0.003%+2/ 0.03%+10	300/1	0.04%+100/ 0.03+10	300/1	0.004%+3	10	VXI module; true RMS.
	1062/ $4945	6½/ 10 Hz–1 MHz	0.002%+1/ 0.01%+4	1000/1	0.025%+10/ 0.2%+100	1000/1	0.003%+1	10	True RMS; up to 200 readings/s.
	1271/ $6040	8½/ 1 Hz–1 MHz*	0.0007%+0.25/ 0.005+2	1000/1	0.006%+10/ 0.02+100	1000/1	0.001%+0.5	1000	*Opt.; true RMS; self calibration; GPIB.
	1281/ $9625	8½/ 1 Hz–1 MHz	0.0003%+2/ 0.0025%+2	1000/1	0.006%+10/ 0.02%+100	1000/1	0.0006%+2	1000	True RMS; self calibration; GPIB.
Extech Instruments Corp. 150 Bear Hill Rd. Waltham, MA 02154 (617) 890-7440	380501/ $79	3½/ N.S.	0.5%/1.2%+1	1000/20	1.2%+5/ 2.5%+5	750/20	2%+2	20	
	380165/ $89	3½/ 50–500 Hz	0.5%+1/1%+1	1000/10	1%+4/ 2.5%+4	750/10	5%±10	2000	Includes logic probe.
	380166/ $99	3½/ 50–500 Hz	0.5%+1/1%+1	1000/10	1%+4/ 2.5%+5	750/10	5%±10	2000	Includes type K thermometer.
	ACA-Clamp On/ $99	3½/ 10–1999 Hz	0.5%/N.A.	1000/ N.A.	1.5%/ 2%+4	750/300	N.A.	N.A.	
	380168/ $109	3½/ 40–400 Hz	0.5%+1/1%+1	1000/20	1%+4/ 2.5%+4	750/20	3%+1	20	Drop-proof to 4 ft.
	380196/ $119	3½/ N.S.	0.5%/1.5%	1000/20	1.5%/ 2.5%	750/20	3%	20	Analog arc display; extra large LCD.
	380198/ $139	3½/ N.S.	0.5%/1.5%	1000/20	1.5%/ 2.5%	750/20	3%	20	
John Fluke Mfg. Co./ Philips Test & Measurement P.O. Box 9090 Everett, WA 98206 (800) 443-5853 (206) 347-6100	70/ $69	3¾/ 45–1000 Hz	0.5%+1/ N.A.	1000/ N.A.	2%+2/ N.A.	750/ N.A.	0.5%+1	32	Bar graph; auto-ranging; diode, capacitance tests.
	73/ $99	3½/ 45–1000 Hz	0.7%+1/N.S.	1000/10	3%+2/ 3%+2	750/10	3%+1	32	Bar graph; auto-ranging.
	75/ $139	3½/ 45–1000 Hz	0.5%+1/ 1.5%+2	1000/10	2%+2/ 3%+2	750/10	2.5%+1	32	Diode, continuity tests; bar graph; auto-ranging.

(see p. 102 for key) *(continued on p. 97)*

DIGITAL MULTIMETERS

Manufacturer	Model/Price	Digits/ Frequency[1]	Dc volts/amps Accuracy[2] (V/A)	Dc volts/amps Max (V/A)	Ac volts/amps Accuracy[2] (V/A)	Ac volts/amps Max (V/A)	Resistance Accuracy[2]	Resistance Max (MΩ)	Remarks
John Fluke Mfg. Co./ Philips Test & Measurement P.O. Box 9090 Everett, WA 98206 (800) 443-5853 (206) 347-6100	21/ $139	$3^{1}/_{2}$/ 45–1000 Hz	0.5%+1/ 1.5%+2	1000/10	2%+2/ 3%+2	750/10	2.5%+1	32	Diode, continuity tests; bar graph; auto-ranging.
	77/ $165	$3^{1}/_{2}$/ 45–1000 Hz	0.3%+1/ 1.5%+2	1000/10	2%+2/ 3%+2	750/10	2%+1	32	Diode, continuity tests; bar graph; auto-ranging.
	23/ $165	$3^{1}/_{2}$/ 45–1000 Hz	0.3%+1/ 1.5%+2	1000/10	2%+2/ 3%+2	750/10	2%+1	32	Diode, continuity tests; bar graph; auto-ranging.
	79/ $185	$3^{3}/_{4}$/ 45–1000 Hz	0.3%+1/ 0.5%	1000/10	1%+2/ 1.5%	750/10	0.4%+1	32	20-kHz counter; bar graph.
	29/ $185	$3^{3}/_{4}$/ 45–1000 Hz	0.3%+1/ 0.5%	1000/10	1%+2/ 1.5%	750/10	0.4%+1	32	Same as Model 29.
	83/ $215	$3^{3}/_{4}$/ 45 Hz–5 kHz	0.3%+1/ 0.4%+2	1000/20	1%+3/ 1.2%+2	1000/20	0.4%+1	40	Diode; capacitance tests; 200-kHz counter.
	25/ $225	$3^{1}/_{2}$/ 40 Hz–30 kHz	0.1%+1/ 0.75%+2	1000/10	0.05%+3/ 1.5%+2	1000/10	0.2%+2	32	Diode, continuity, conductance tests; auto ranging.
	27/ $225	$3^{1}/_{2}$/ 40 Hz–30 kHz	0.1%+1/ 0.75%+2	1000/10	0.5%+3/ 1.5%+2	1000/10	0.2%+2	32	Same as Model 25 plus min./max. and relative.
	85/ $255	$3^{3}/_{4}$/ 45 Hz–20 kHz	0.1%+1/ 0.2%+2	1000/10	0.5%+2/ 0.6%+2	1000/10	0.2%+1	40	Diode, capacitance, duty cycle, capacitance tests.
	37/ $269	$3^{1}/_{2}$/ 40 Hz–30 kHz	0.1%+1/ 0.75%+2	1000/10	0.5%+3/ 1.5%+2	1000/10	0.2%+1	32	Diode, continuity tests, min./max. modes.
	87/ $300	$3^{3}/_{4}$/ 50 Hz–20 kHz	0.1%+1/ 0.2%+2	1000/20	0.7%+4/ 1%+2	1000/20	0.2%+1	40	Diode, capacitance tests, 200-kHz counter.
	PM2518/ $300	4/ 40 Hz–40 kHz	0.1%+0.02%/ 0.5%+0.1%[3]	1000/20	0.5%+0.1%/ 0.06% + 0.3%[3]	1000/20	0.3%+0.1%[3]	100	Diode, continuity tests, bar graph.
	8024B/ $344	$3^{1}/_{2}$/ 45 Hz–5 kHz	0.1%+1/ 0.75%+1	1000/2	0.75%+2/ 1.5%+1	750/2	0.15%+1	20	Diode, conductance tests; peak hold; temperature.
	PM2618/ $350	4/ 40 Hz–10 kHz	0.07%+0.02%/ 0.4%+0.1%[3]	1000/20	0.4%+0.1%/ 0.6%+0.3%[3]	1000/20	0.2%+0.1%[3]	100	200-kHz counter; 10-MHz logic detection.
	8062A/ $359	$4^{1}/_{2}$/ 20 Hz–30 kHz	0.05%+2/ 0.3%+2	1000/2	0.5%+10/ 0.75%+10	750/2	0.1%+2	300	Diode, continuity tests; true RMS.
	8010A/ $359	$3^{1}/_{2}$/ 45 Hz–50 kHz	0.1%+1/ 0.3%+1	1000/10	0.5%+2/ 1%+2	750/10	0.5+1	20	True RMS; diode, conductance tests.
	8025B/ $380	$3^{1}/_{2}$/ 40 Hz–30 kHz	0.2%+1/ 0.75%+2	1000/10	0.5%+3/ 1.5%+2	1000/10	2%+10	32	Diode, continuity tests; min./max., relative.
	8012A/ $389	$3^{1}/_{2}$/ 45 Hz–50 kHz	0.1%+1/ 0.3%+1	1000/2	0.5%+2/ 1%+2	750/2	0.2%+1	20	Diode, conductance tests; true RMS.
	86/ $399	$3^{1}/_{2}$/ 45 Hz–5 kHz	0.3%+2/ 1%+2	1000/20	1.5%+5/ 1.5%+5	1000/20	1%+20	400	Duty cycle, RPM, pulse width; 200-kKz counter.
	8060A/ $429	$4^{1}/_{2}$/ 20 Hz–100 kHz	0.04%+2/ 0.2%+2	1000/2	0.2%+10/ 0.75%+10	750/2	2%+3	300	Same as 8062A.
	PM2718/ $430	4/ 40 Hz–100 kHz	0.04%+0.02%/ 0.4%+0.1%[3]	1000/20	0.3%+0.1%/ 0.4%+0.3%[3]	1000/20	0.15%+ 0.05%[3]	100	Same as PM2618 plus data hold.
	88/ $459	$3^{1}/_{2}$/ 45 Hz–5 kHz	0.15%+2/ 0.8%+2	1000/20	1.5%+5/ 1.5%+5	1000/20	1%+20	400	Same as Model 86 plus smoothing, low-ohms.
	8050A/ $479	$4^{1}/_{2}$/ 20 Hz–20 kHz	0.03%+2/ 0.3%+2	1000/2	0.5%+10/ 1%+10	750/2	0.25%+3	20	Diode, conductance tests; true RMS; dBm function.
	45/ $635	5/ 20 Hz–20 kHz	0.02%+2/ 0.05%+2	1000/10	0.08%/ 0.5%+10	750/10	0.05%+2	100	True RMS; diode, continuity tests; 1-MHz counter.
	PM2525/ $795	$5^{1}/_{2}$/ 20 Hz–100 kHz	0.02%+0.01%/ 0.1%+0.05%[3]	2000/10	0.2%+0.1%/ 0.4%+0.15%	2000/10	0.1%+ 0.05%[3]	2	True RMS; capacitance, time, continuity tests.
	8840A/ $875	$5^{1}/_{2}$/ 20 Hz–100 kHz	0.004%+4/ 0.04%+4	1000/2	0.14%+100/ 0.4%+200	700/2	0.01%+3	20	True RMS opt.; up to 100 readings/s.
	8842A/ $1095	$5^{1}/_{2}$/ 20 Hz–50 kHz	0.0025%+2/ 0.05%+4	1000/2	0.07%+80/ 0.4%+200	700/2	0.005%+3	20	True RMS opt.; up to 100 readings/s.

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DIGITAL MULTIMETERS

Manufacturer	Model/Price	Digits/ Frequency[1]	Dc volts/amps Accuracy[2] (V/A)	Dc volts/amps Max (V/A)	Ac volts/amps Accuracy[2] (V/A)	Ac volts/amps Max (V/A)	Resistance Accuracy[2]	Resistance Max (MΩ)	Remarks
John Fluke Mfg. Co./ Philips Test & Measurement P.O. Box 9090 Everett, WA 98206 (800) 443-5853 (206) 347-6100	PM2534/ $1095	3½-6½/ 40 Hz–5 kHz	0.005%+0.0013%/ 0.15%+0.01%[3]	300/3	0.04%+ 0.02%/ 0.2%+0.1%[3]	300/3	0.02%+ 0.0033%	300	Up to 100 measurements/s; GPIB programmable using English commands.
	PM2535/ $1395	3½-6½/ 40 Hz–5 kHz	0.005%+0.0013%/ 0.15%+0.01%[3]	300/3	0.04% + 0.02%/ 0.2%+0.1%[3]	300/3	0.02%+ 0.0033%	300	Same as PM2534 plus advance data collection, control, and processing.
	8840A-AF/ $1525	5½/ 20 Hz–100 kHz	0.004%+3/ 0.04%+4	1000/2	0.14%+100/ 0.4%+200	700/2	0.01%+3	20	Up to 100 readings/s; true RMS; dc voltage ratio.
	8920A/ $2195	3½/ 10 Hz–20 kHz	N.A.	[4]	0.5%+/N.A.	700/N.A.	N.A.	N.A.	True RMS; ac or ac + dc; dB measurements.
	8921A/ $2195	3½/ 10 Hz–20 kHz	N.A.	[4]	0.5%+/N.A.	700/N.A.	N.A.	N.A.	Same as 8920A but without recorder output.
	8922A/ $2295	3½/ 2 Hz–11 kHz	N.A.	[4]	0.5%+/N.A.	700/N.A.	N.A.	N.A.	Same as 8920A with lower-frequency capability.
	8520A/ $3795	5½/ 10–1000 Hz	0.005%+1/ N.A.	1000/ N.A.	0.1%+ 0.03%[3]/ N.A.	650/N.A.	0.007%+2	10	Max.-min., limits tests; GPIB standard.
	8505A/ $3995	7½/ 10 Hz–1 MHz	0.001%+8/ 0.03%+10	1000/1	0.1%+ 0.012%[3]/ 0.06%+9	1000/1	0.003%+0.8	100	Current, ac voltage, and resistance opt.
	8522A/ $5885	5½/ 10 Hz–1 MHz	0.005%+1/ N.A.	1000/ N.A.	0.1%+ 0.03%[3]/ N.A.	650/N.A.	0.007%+2	10	Same as 8520A but with parallel and BCD interface.
	8506A/ $7995	7½/ 10 Hz–1 MHz	0.0006%+60/ 0.03%+10	1000/1	0.016%/N.A.	500/N.A.	0.003%+0.8	100	Thermal RMS for ac voltage.
Hewlett-Packard Co. 19310 Pruneridge Ave. Cupertino, CA 95014 (800) 752-0900	E2373A/ $99	3½/ to 500 Hz	0.5%+2/ 1%+2	1000/10	1.2%+4/ 2%+5	750/10	0.7%+1	30	Diode test; auto-ranging.
	E2377A/ $169	3½/ to 1000 Hz	0.3%+2/ 1%+2	1000/10	1%+3/ 2%+5	750/10	0.7%+1	30	Data hold; rugged version (E2378A), $189.
	HP 3468A/B/ $910	3½-5½/ 20 Hz–300 kHz	0.0072%+2/ 0.14%+6	300/3	0.26%+102/ 1%+163	300/3	0.011%+2	30	True RMS; auto ranging.
	HP 3478A/ $995	5½/ 20 Hz–300 kHz	0.004%+2/ 0.11%+40	300/3	0.2%+70/ 0.72%+163	300/3	0.011%+2	30	True RMS; auto ranging; up to 90 readings/s.
	HP 3466A/ $1770	4½/ 20 Hz–100 kHz	0.03%+1/ 0.15%+2	1200/2	0.3%+20/ 0.9%+35	1700/2	0.03%+1	20	True RMS; diode test; auto ranging.
	HP 3457A/ $3260	3½-6½/ 20 Hz–100 kHz	0.0017%+6/ 0.02%+104	300/1.5	0.13% + 2800/ 0.25% + 2800	300/1	0.0035%+6	3000	True RMS; 1.5-MHz counter; up to 1350 readings/s.
	HP 3437A/ $5060	3½/ to 1 MHz	0.05%+1.6/ N.A.	10/N.A.	N.A.	N.A.	N.A.	N.A.	System voltmeter; provides trigger delay.
	HP 3456A/ $6060	3½-6½/ 10 Hz–250 kHz	0.0015%+2/ N.A.	1000/ N.A.	0.08%+73/ N.A.	1000/N.A.	0.003%+2	1000	True RMS; up to 330 readings/s.
	HP 3458A/ $6595	8½/ to 10 MHz	0.0004%/ 0.0015%	1000/1	0.09%/ 0.03%	1000/1	0.001%	1000	10-MHz counter; up to 100,000 readings/s.
	HP 3455A/ $8100	5½-6½/ 30 Hz–1 MHz	0.005%+3/ N.A.	1000/ N.A.	0.05%+50/ N.A.	1000/N.A.	0.0035%+5	0.01	True RMS; integrating system voltmeter.
Keithley Instruments Inc. 28775 Aurora Rd. Cleveland, OH 44139 (216) 248-0400	169/ $280	3½/ 45 Hz–5 kHz	0.25%+1/ 0.75%+1	1000/2	1%+5/ 1.5%+1	1000/2	0.2%+1	20	400-V input protection.
	175/ $495	4½/ 20 Hz–100 kHz	0.03%+1/ 0.15%+2	1000/10	0.5%+20/ 0.8%+20	750/10	0.05%+1	200	100-point memory; digital calibration.
	179A/ $540	4½/ 45 Hz–20 kHz	0.04%+1/ 0.2%+2	1200/20	0.5%+15/ 1%+15	1000/20	0.04%+1	20	1-nV sensitivity; 15-μV pk-pk noise.
	197A/ $659	5½/ 20 Hz–100 kHz	0.011%+2/ 0.1%+15	1000/10	0.35%+100/ 0.8%+100	750/10	0.018%+2	220	150 readings/s; 500-point memory.

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Since other 12-bit ADCs need four times the space to go half as fast at twice the price, we use the term 'competition' lightly.

Maybe we are being a little boastful when we say that compared to the AD671, every other 12-bit monolithic A/D converter is a lightweight. But see if you don't agree.

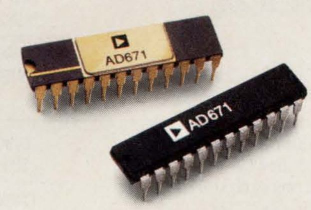
The AD671 comes in a 24-pin skinny DIP package. (Other A/D converters are in double- and triple-wide DIPs, taking up to four times as much space on your board.)

The AD671 has a true conversion time of 500ns. (Making it twice as fast as the nearest 'competitor'.)

The AD671 costs only $65. (You can expect to pay at least double that amount for any other 'comparable' ADC.)

And the AD671 doesn't have calibration cycles, complicated interfaces, or specs that can't hold up over temperature and power supply variations. (But if you like these things, you can get them with other ADCs.)

To find out more about the A/D converter that has more weight behind it, get a data sheet on the AD671 by contacting Analog Devices at 1-800-262-5643. Or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.



AD671 500 ns A/D CONVERTER.

The AD671 is the fastest 12-bit monolithic A/D converter, converting in under 500 ns while consuming less than 500 mW. It accepts standard input signals of 0 to +10 V, 0 to +5 V or ±5 V, and it outputs data in offset/straight binary or two's complement format. The AD671 offers the right combination of speed and resolution for imaging applications using charge coupled devices, infrared detectors or photomultiplier tubes, while its accuracy is ideal for multichannel data acquisition systems and communications systems.

ANALOG DEVICES

CIRCLE 90 FOR U.S. RESPONSE

CIRCLE 91 FOR RESPONSE OUTSIDE THE U.S.

Analog Devices, One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106. Distribution, offices and applications support available worldwide.

DIGITAL MULTIMETERS

Manufacturer	Model/Price	Digits/ Frequency[1]	Dc volts/amps Accuracy[2] (V/A)	Dc volts/amps Max (V/A)	Ac volts/amps Accuracy[2] (V/A)	Ac volts/amps Max (V/A)	Resistance Accuracy[2]	Resistance Max (MΩ)	Remarks
Keithley Instruments Inc. 28775 Aurora Rd. Cleveland, OH 44139 (216) 248-0400	177/ $745	4½/ 45 Hz–20 kHz	0.03%+1/ 0.2%+1	1200/2	0.5%+15/ 0.2%+1	1000/2	0.04%+1	20	
	199/ $995	4½-5½/ 20 Hz–100 kHz	0.006%+2/ 0.05%+15	300/3	0.15%+200/ 0.007%+2	300/3	0.008%+3	300	$1395 with 8-channel scanner.
	195A/ $1195	3½-5½/ 20 Hz–50 kHz	0.025%+6/ 0.01%+0.5	1000/2	0.3%+200/ 0.04%+10	700/2	0.025%+5	20	1000 readings/s.
	196/ $1395	3½-6½/ 20 Hz–100 kHz	0.0038%+20/ 0.05%+5	300/3	0.15%+100/ 0.6%+100	300/3	0.007%+2	300	100-point data logger; relative references.
	193A/ $2795	3½-6½/ 20 Hz–100 kHz	0.003%+20/ 0.09%+10	1000/3	0.35%+300/ 0.6%+300	700/2	0.005%+20	220	1000 readings/s; second channel opt.
Leader Instruments Corp. 380 Oser Ave. Hauppauge, NY 11788 (800) 645-5104 (516) 231-6900	856/ $800	4½/ 40 Hz–100 kHz	0.05%±2/ 0.7%±2	1000/3	0.4%±30/ 1.7%±40	750/3	0.07%±2	30	True RMS, dBm and dB relative.
	LCD 100/ $925	3½/ 40–500 Hz	0.35%±3/ 1%±3	1000/ 0.320	1%±5/ 1.5%±3	750/0.320	0.4%±3	32	Also a 3-Msample/s 1-ch. DSO.
	300/ $1995	3½/ 40–500 Hz	0.35%±3/ 1%±3	1000/ 0.320	1%±5/ 1.5%±3	750/0.320	0.4%±3	32	Also a 30-Msample/s 2-ch. DSO, data logger, and logic scope.
Protek P.O. Box 59 Norwood, NJ 07648 (201) 767-7242	D-906/ $29.95	3½/ 40–500 Hz	0.7%/1.5%	200/10	1.2%/N.A.	500/N.A.	1.5%	2	Overload protection.
	D-930A/ $35	3½/ 40–500 Hz	0.75%/1%	500/0.2	1.2%/1.2%	500/0.2	1%	20	Diode test, data hold, auto ranging.
	D-902/ $39	3½/ 40–500 Hz	0.5%/0.5%	1000/10	1.2%/N.A.	750/10	1%	20	
	D-903/ $39	3½/ 40–500 Hz	0.5%/0.75%	1000/2	1.2%/N.A.	750/N.A.	0.75%	2	Diode test.
	D-935A/ $40	3½/ 40–500 Hz	0.75%/N.A.	500/ N.A.	1.2%/N.A.	500/N.A.	1%	20	Diode test; data hold.
	D-927/ $69	3¾/ 40–500 Hz	0.3%/0.5%	1000/4	0.5%/1%	750/20	0.5%	40	Bar graph; capacitance test; auto ranging.
	D-990/ $69.50	3½/ 40–500 Hz	0.5%/0.75%	1000/10	0.75%/1%	750/10	0.75%	20	Bar graph; auto ranging; data hold.
	D-945/ $89	4½/ 40–500 Hz	0.05%+2/ 0.3%+2	1000/10	0.05%+10/ 0.75%+10	750/10	0.2%+5	20	Diode test; overload protection.
	D-910F/ $99.50	3½/ 40–500 Hz	0.5%/0.5%	1000/20	0.5%/0.75%	750/20	approx. 0.3%	20	Diode, capacitance tests; 200-kHz counter.
	D-981/ $130	3¾/ 40–500 Hz	0.3%/1.5%	1000/10	1.2%/1.5%	750/10	0.7%	40	Bar graph; capacitance test; 1-MHz counter.
	D-4500E/ $149	4½/ 40–500 Hz	0.05%/0.3%	1000/20	0.5%/0.75%	1000/20	0.2%	20	Diode, capacitance tests; 200-MHz counter.
Simpson Electric Co. 853 Dundee Ave. Elgin, IL 60120-3090 (708) 697-2260	487/ $199	3¾/ 15 Hz–20 kHz	0.1%+1/ 0.75%+1	1000/10	0.5%+2/ 1.2%+2	750/10	0.2%+1	30	Bar graph; data and peak hold; auto-ranging.
	470/ $200	3½/ 45–1000 Hz	0.15%+1/ 1%+1	1000/10	1%+5/ 2%+5	750/10	2%+2	20	Diode test.
	488/ $239	3¾/ 14 Hz–20 kHz	0.1%+1/ 0.75%+1	1000/10	0.75%+3/ 1.5%+4	750/10	2%+1	30	True RMS; auto-ranging; data and peak hold.
	463/ $260	3½/ 20 Hz–20 kHz	0.1%+1/ 0.5%+2	1000/2	0.5%+2/ 0.5%+2	750/2	0.25%+2	20	Battery or ac operation; overload protection.
	461-2R/ $290	3½/ 20 Hz–50 kHz	0.1%+1/ 0.5%+2	1000/2	0.5%+2/ 1%+2	750/2	0.25%+2	20	True RMS; battery or ac operation.
	474/ $300	4½/ 45–1000 Hz	0.03%+2/ 1%+1	1000/10	1%+5/ 2%+5	750/10	0.4%+2	20	Diode test.
	467-2/ $310	3½/ 20 Hz–100 kHz	0.1%+1/ 0.5%+1	1000/2	0.5%+5/ 1.5%+5	750/2	0.25%+1	20	True RMS; differential peak hold; bar graph.

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▼ ANALYZER MEASURES MICROWAVE TRANSITIONS

The HP 71500A microwave transition analyzer measures amplitude and phase as a function of time, frequency, and power for signals from dc to 40 GHz. The two-channel, sampler-based instrument measures rise and fall times as fast as 25 ns, settling times, and transitions of switched and RF pulses. Other measurements include on-off ratio, delay, switching time, isolation, and peak and average power. The HP 71500A is part of the HP 70000 modular measurement system. A complete instrument, the HP 71500A, costs $42,900. The HP 70820A microwave transition-analyzer module costs $32,500, and the HP 70004A color display and mainframe costs $10,400. Delivery is in 12 weeks.

Hewlett-Packard Co.
19310 Pruneridge Ave.
Cupertino, CA 95014
(800) 752-0900
▶ CIRCLE 497

▼ SYSTEM DEVELOPS 680X0 CODE ON VAX/VMS HOSTS

An enhanced software development package and a high-performance emulator system form an integrated tool chain for engineers developing Motorola 680X0 code on VAX/VMS hosts. The software, Validate/XEL, features enhanced Status and Set Status commands, a scrollable viewport, better context-sensitive help, command history, command aliases, macro capability, reduced object-module load times, and the ability to call routines in target memory from macros. The EL1800 emulator supports all 68000 microprocessors with an event monitor system, a sophisticated breakpoint and triggering system, and up to 2 Mbytes of RAM overlay memory. Systems are available immediately starting at $35,000.

Applied Microsystems Corp.
5020 148th Ave. N.E.
Redmond, WA 98073-9702
(206) 882-2000
▶ CIRCLE 498

▼ NOTEBOOK ADDS NUMEROUS CAPABILITIES

Labtech Notebook/XE is an extended edition of the widely used general-purpose data-acquisition, analysis, and control software. Additional capabilities in the DOS, Windows 3.0, and OS/2 versions of Notebook/XE include multiple real-time screen displays, additional windows per screen, larger setup capabilities, more display types, support for remote instrumentation and extended memory, and CGI graphics drivers that free up more memory. In its Unix and VMS versions, Notebook/XE takes advantage of X-Windows, so multiple users on X-servers can access the software and I/O hardware. Labtech Notebook/XE is available within 2 weeks, starting at $2495 for the DOS version.

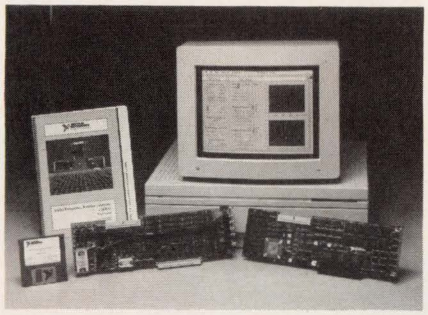
Laboratory Technologies Corp.
400 Research Dr.
Wilmington, MA 01887
(508) 657-5400
▶ CIRCLE 499

DIGITAL MULTIMETERS

Manufacturer	Model/Price	Digits/ Frequency[1]	Dc volts/amps Accuracy[2] (V/A)	Dc volts/amps Max (V/A)	Ac volts/amps Accuracy[2] (V/A)	Ac volts/amps Max (V/A)	Resistance Accuracy[2]	Resistance Max (MΩ)	Remarks
Simpson Electric Co. 853 Dundee Ave. Elgin, IL 60120-3090 (708) 697-2260	464-4/ $360	$3\frac{1}{2}$/ 20 Hz–100 kHz	0.1%+1/ 0.5%+1	1000/10	1%+5/ 1.5%+5	750/10	0.5%+1	20	True RMS; diode test; overload protection.
	460-6/ $500	$4\frac{1}{2}$/ 20 Hz–100 kHz	0.07%+1/ 0.75%+1	1000/10	1.0%+35/ 1.5%+35	750/10	0.15%+5	20	True RMS; diode test; dB readings; pulse detection.
Tektronix Inc. P.O. Box 500 Beaverton, OR 97077 (800) 426-2200 (503) 627-7111	DM250/ $135	$3\frac{1}{2}$/ 40–500 Hz	0.5%+1/ 1.5%+3	1000/10	1.25%+5/ 2.5%+5	750/10	1.5%+5	20	Diode test; analog bar graph; data hold.
	DM251/ $199	$3\frac{3}{4}$/ 40–1000 Hz	0.3%+2/ 0.8%+4	1000/10	0.7%+5/ 1%+5	750/10	1.5%+5	40	100 Hz–1 MHz counter; analog bar graph.
	DM252/ $219	$3\frac{3}{4}$/ 40–1000 Hz	0.1%+2/ 0.8%+4	1000/10	0.5%+5/ 1%+5	750/10	1%+5	40	100 Hz–1 MHz counter; analog bar graph.
	CDM250/ $345	$3\frac{1}{2}$/ 45–500 Hz	0.5%+1/ 1%+3	500/10	1%+4/ 1.5%+4	500/10	1.5%+5	20	
Yokogawa Corp. of America 2 Dart Rd. Newnan, GA (404) 253-7000	7551/ $895	$5\frac{1}{2}$/ to 100 kHz	0.005%+3/ 0.07%+20	1000/2	0.2%+100/ 0.5%+200	700/2	0.011%+5	200	Memory card; GPIB or RS-232C.
	7552/ $995	$5\frac{1}{2}$/ to 100 kHz	0.005%+3/ 0.07%+20	1000/20	0.2%+100/ 0.5%+200	700/2	0.011%+5	200	True RMS; memory card; GPIB or RS-232C.
	7561/ $1195	$6\frac{1}{2}$/ N.A.	0.003%+15/ 0.05%+20	1000/2	N.A.	N.A.	0.009%+30	200	Memory card; GPIB or RS-232C.
	7562/ $1295	$6\frac{1}{2}$/ to 100 kHz	0.003%+15/ 0.05%+20	1000/2	0.15%+100/ 0.8%+200	700/2	0.009%+30	200	True RMS; memory card; GPIB or RS-232C.
	7563/ $1995	$6\frac{1}{2}$/ N.A.	0.003%+10/ N.A.	200/ N.A.	N.A.	N.A.	0.005%+25	20	12 thermocouple inputs; platinum RTD inputs.

[1] Response range for ac measurements.
[2] Percent or percent and digits. Best long-term accuracy, regardless of range.
[3] Percent of reading plus percent of range.
[4] Measures dc in ac + dc mode.
N.A.: Not applicable.
N.S.: Not specified.

▼ BOARDS MAKE MAC II AN AUDIO SIGNAL ANALYZER



The Audio Frequency Fourier Analyzer (AFFA) is a Macintosh II-based 2-channel, dual-display signal analyzer. The analyzer includes the NB-DSP2300 digital-signal processing board, the NB-A2100 audio-frequency data-acquisition board, and the LabView 2 graphical software system. Full-power bandwidth is dc to 20 kHz, with an amplitude flatness of ±0.015 dB. Frequency accuracy is within 0.01%. The AFFA kit ($7495) includes a run-time LabView system for engineers who need an operate-only, standalone analyzer. The kit with the full LabView development system costs $8995. The AFFA VI manuals alone cost $495.

National Instruments Corp.
6504 Bridge Point Pkwy.
Austin, TX 78730-5039
(800) 433-3488 or (512) 794-0110
▶ **CIRCLE 500**

▼ SOFTWARE INTEGRATES DEVICE-ANALYSIS SYSTEMS

The Integrated Diagnostic Environment (IDE) is a fully-integrated software environment that brings together systems and equipment used in device analysis. The package works with electron-beam and focused-ion-beam systems, microprobers, scanning electron microscopes, emission microscopes, laser-cutting systems and other equipment. All systems can be placed under workstation control, connected by a common Ethernet backbone and using one software interface and one set of operating procedures. Cost depends on configuration, but typical systems start at $40,000. Delivery is within 90 days.

Schlumberger Technologies
1601 Technology Dr.
San Jose, CA 95110-1397
(408) 437-5129
▶ **CIRCLE 501**

▼ BOARD TESTER SUPPORTS MANY PROCESSOR TYPES

With support for almost 90 microprocessors, the 9100FT Troubleshooting TestStation tests loaded pc boards incorporating the latest RISC, CISC, and DSP devices. The instrument employs emulative testing, which emulates the microprocessor in the unit under test (UUT). Six standard techniques are used: signature analysis, logic-level detection, frequency and event counting, pulsing, and vector driving. The 9100FT can connect to the kernal in two ways—through a memory interface pod that can be easily reconfigured for different microprocessor types, or through a microprocessor-specific interface pod. Either method enables the 9100FT to gain control of the UUT's bus. A typically configured 9100FT Troubleshooting TestStation costs less than $50,000. Delivery is within 6 weeks.

John Fluke Mfg. Co. Inc.
P.O. Box 9090
Everett, WA 98206-9090
(800) 443-5853 or (206) 347-6100
▶ **CIRCLE 502**

▼ SYSTEM EMULATES 80C186/C188 AT 16 MHZ

The Zaxpac 2000 for the 80C186/C188 microprocessors offers 16-MHz real-time emulation with enhanced mode support. The ERX emulator that forms the basis of the system also supports the 80C187 coprocessor chip. Composed of an emulation module (boardset) and a personality module, the ERX emulator can be configured to plug into an IBM PC/AT or compatible. This arrangement takes advantage of the high-speed parallel interface offered by the AT bus. The emulator is available with the Paradigm Systems Debug/ERX interface, which is a customized implementation of Borland International's Turbo Debugger. The Zaxpak 2000 for the 80C186/C188 costs $14,785 with Debug/ERX. The system costs $12,990 with the ER-ICE symbolic debug software interface in place of the Debug/ERX software.

Zax Corp.
2572 White Rd.
Irvine, CA 92714
(800) 421-0982 or (714) 474-1170
▶ **CIRCLE 503**

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SPECIFICATIONS

Price (1-9 qty)	Model	Type	Price
	YSW-2-50DR (pin)	Absorptive	$19.95
	ZYSW-2-50DR (connector)	Absorptive	$59.95
	YSWA-2-50DR (pin)	Reflective	$23.95
	ZYSWA-2-50DR (connector)	Reflective	$69.95

Frequency, (MHz)	50	100	dc-500		1000	500-2000		2000-5000	
Insertion loss, typ(dB)			0.9	1.1		1.3	1.4	1.4	1.9
Isolation, typ (dB)	65	54	50		37	40		28	
	63	60		42	37		31		20
1dB compression, typ (dBm @ in port)			20	18		20	20	24	22.5
RF input, max dBm			22			22		26	
(no damage)			20 ("off" port), 24 (total)						
VSWR (on), typ			1.4	1.25		1.4	1.35	1.4	1.5
Video breakthrough to RF, typ(mV p-p)			30	30		30	30	30	30
Switching speed, typ (nsec)			3.0	3.0		3.0	3.0	3.0	3.0

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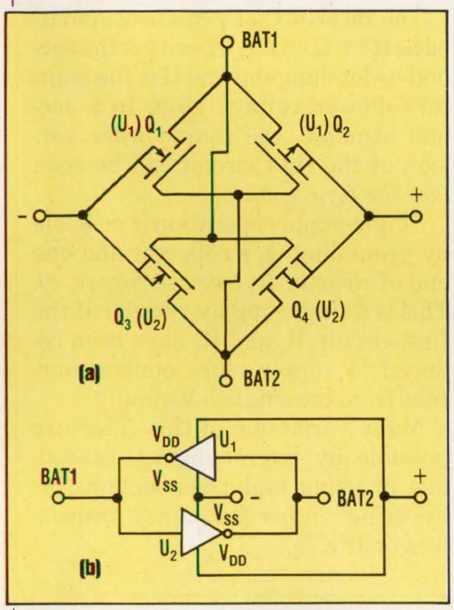
CIRCLE 150 FOR U.S. RESPONSE **CIRCLE 151 FOR RESPONSE OUTSIDE THE U.S.**

F141 REV. B

CIRCLE

521 ACTIVE BRIDGE USES CMOS GATES

DAVE CUTHBERT
Tektronix Inc., P.O. Box 500 W3/100, Beaverton, OR 97077; (503) 690-7036.

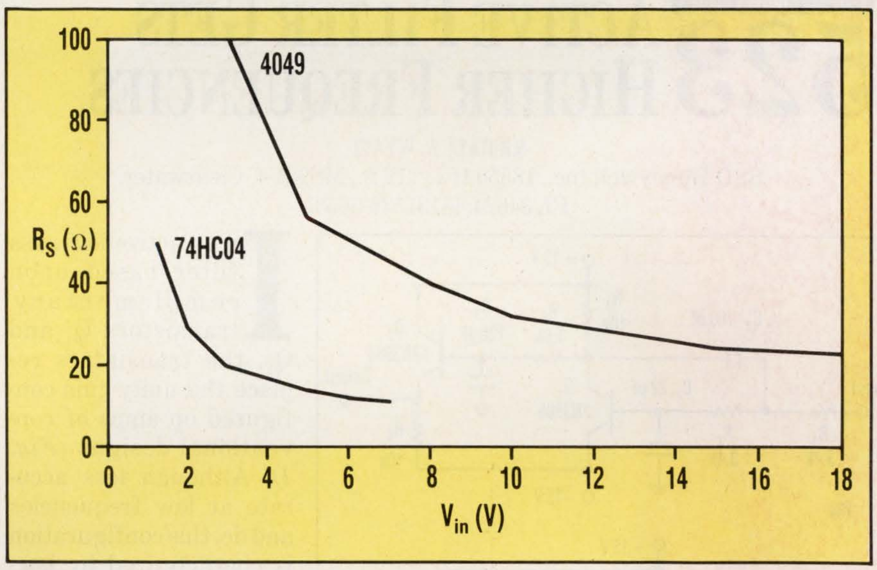


1. TWO CMOS HEX inverter chips are configured to form an active bridge, thus supplying the correct polarity to the circuit (a). In a simplified schematic, it can be seen that when BAT1 is positive and BAT2 is negative, transistors Q_2 and Q_3 are on; when BAT1 is negative and BAT2 is positive, transistors Q_1 and Q_4 are on (b).

This bridge circuit, using two CMOS hex inverter chips, ensures that a battery supplies the correct polarity, regardless of how the terminals are connected *(Fig. 1a)*. All six gates are paralleled in inverter U_1 to form one low-impedance inverter. Inverter U_2 is connected in the same configuration.

A simplified schematic shows that when BAT1 is positive and BAT2 is negative, FETs Q_2 and Q_3 are on *(Fig. 1b)*. When BAT1 is negative and BAT2 is positive, transistors Q_1 and Q_4 are on.

Inputs of 1.5 to 7 V can be used if the circuit is built with 74HC04 chips. Using 4049 chips boosts the allowable voltage ranging up to 3 to 18 V *(Fig. 2)*. The bridge can also be employed as an active rectifier for square-wave signals.☐



2. TWO DIFFERENT CHIPS CAN BE USED FOR DIFFERENT voltage ranges, 74HC04s or 4049s. The bridge resistance is graphed against the varying supply voltages.

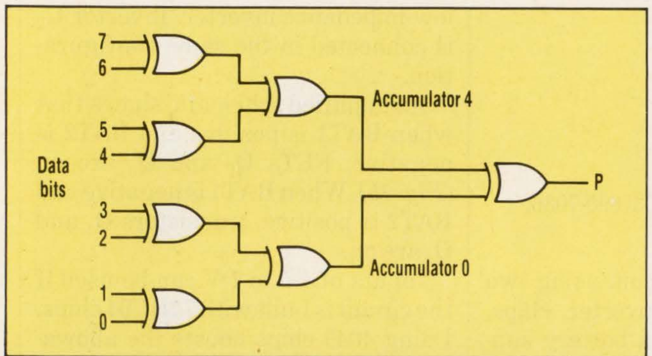
CIRCLE

522 GENERATE PARITY FOR 6805 CHIP

NOOR SINGH KHALSA
EG&G Inc., P.O. Box 809, MS E-1, Los Alamos, NM 87544; (505) 667-0200.

The full-duplex, asynchronous serial communication port of the Motorola 68HC05 family of low-cost, single-chip static microcontrollers contains an optional ninth bit that can be employed as a parity bit. However, the microcontroller doesn't contain a parity flag for the accumulator. One possible way to generate parity for the microcontroller is to shift and count carries. Another method, one that's faster and less time-variant, is a software implementation of the old 9-bit odd/even TTL parity-generator-checker IC, the 74180 *(see the figure)*. Using this procedure, alternate

```
PARITY:  STA    TEMP1    ; Save a copy of the data byte in local RAM
         LSRA            ; Shift Accumulator once
         EOR    TEMP1    ; Exclusive OR even bits with odd bits
         STA    TEMP1    ; Save a copy of the intermediate result
         LSRA            ; Shift Accumulator twice
         LSRA
         EOR    TEMP1    ; Exclusive OR alternate intermediate bits
         AND    #$11     ; Mask off all but bit 4 (parity of upper
                         ; nybble) & bit 0 (parity of lower nybble)
         BEQ    P2       ; If both bits are zero, parity is zero. Z flag = 1
         EOR    #$11     ; XOR with 11H. If both bits are 1, parity is zero
P2:      RTS             ; Otherwise Acc has a value of 01H or 10H, Z = 0
```



A SOFTWARE IMPLEMENTATION **of a 74180 chip generates parity for a 6805 microcontroller. The program exclusive ORs alternate bits in succession.**

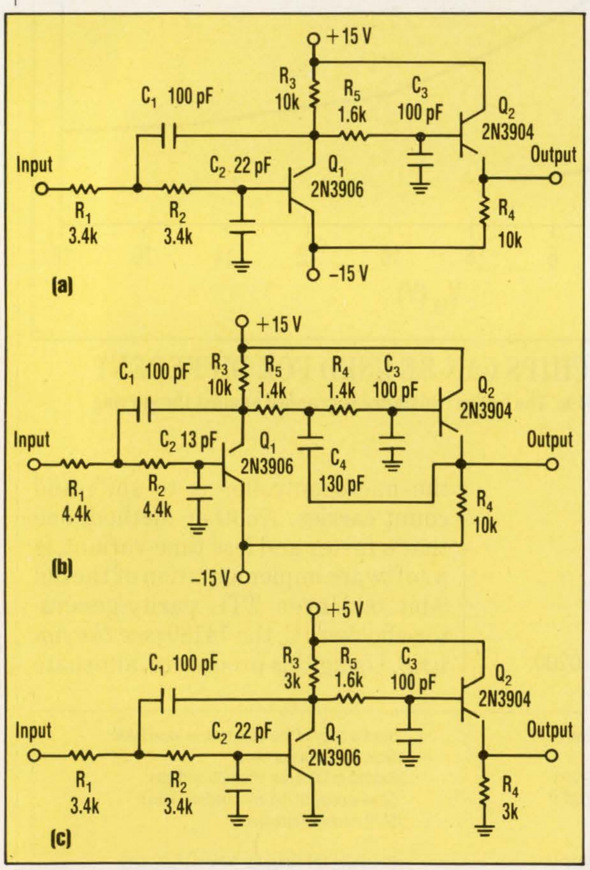
bits are exclusively ORed in succession.

The parity routine that's shown generates one parity bit for the byte in the microcontroller's accumulator. The routine requires one temporary storage register in the local RAM (TEMP1). If the parity bit is zero, then the routine returns with a zero flag.□

CIRCLE 523

ACTIVE FILTER GETS HIGHER FREQUENCIES

MICHAEL A. WYATT
SSO Honeywell Inc., 13550 Hwy. 19 S., MS931-4, Clearwater, FL 34624; (813) 539-5653.



THE 1-MHZ **low-pass filter has Q_1 as the second-order section and Q_2 as the first-order section (a). Modifications make a fourth-order filter (b). Grounding Q_1's collector and one end of R_4 allows one supply (c).**

In an active low-pass filter based upon complementary transistors Q_1 and Q_2, the transistors replace the unity-gain-configured op amps of conventional designs *(Fig. 1)*. Although less accurate at low frequencies and dc, this configuration is characterized by low-cost, high-frequency operation and good power-supply flexibility. These features aren't easily attained with conventional op amp designs.

Each transistor is connected as an emitter follower, with resistors R_3 and R_4 setting the nominal emitter currents. The V_{be} rise in Q_1 (pnp) is offset by the V_{be} drop in Q_2 (npn). This supplies a first-order cancel of the V_{be}'s (and temperature coefficients) in Q_1 and Q_2, and makes it possible to operate at dc with reasonable accuracy.

One example features a 1-MHz third-order low-pass VCVS filter design with Q_1 as the second-order section and Q_2 as the first-order section *(see the figure, a)*. For an accurate filter response, the ratio of C_2/C_1 needs "predistortion" in the second-order sections to compensate for the less-than-unity voltage gain of the sections' emitter follower.

The ratio of C_2/C_1 can be calculated as $(\zeta^2 + G - 1)$, where ζ is the second-order damping and G is the emitter-follower voltage gain. In a second example, the fourth-order version of the first circuit can be seen *(see the figure, b)*.

Single-supply operation is possible by grounding Q_1's collector and one end of resistor R_4 *(see the figure, c)*. This is a single-supply version of the first circuit. R_3 and R_4 have been reduced to supply more emitter current from the single 5-V supply.

Many variations of this filter are possible by interchanging, cascading, or using high-pass sections, or by using higher-frequency transistors or JFETs.□

IFD WINNER

IFD Winner for March 28, 1991

David Cuthbert, Tektronix, Inc., TV Waveform Displays Div., M.S. W3 100, P.O. Box 500, Beaverton, OR 97077. His idea: *"Get Negative Rail Using CMOS Gates."*

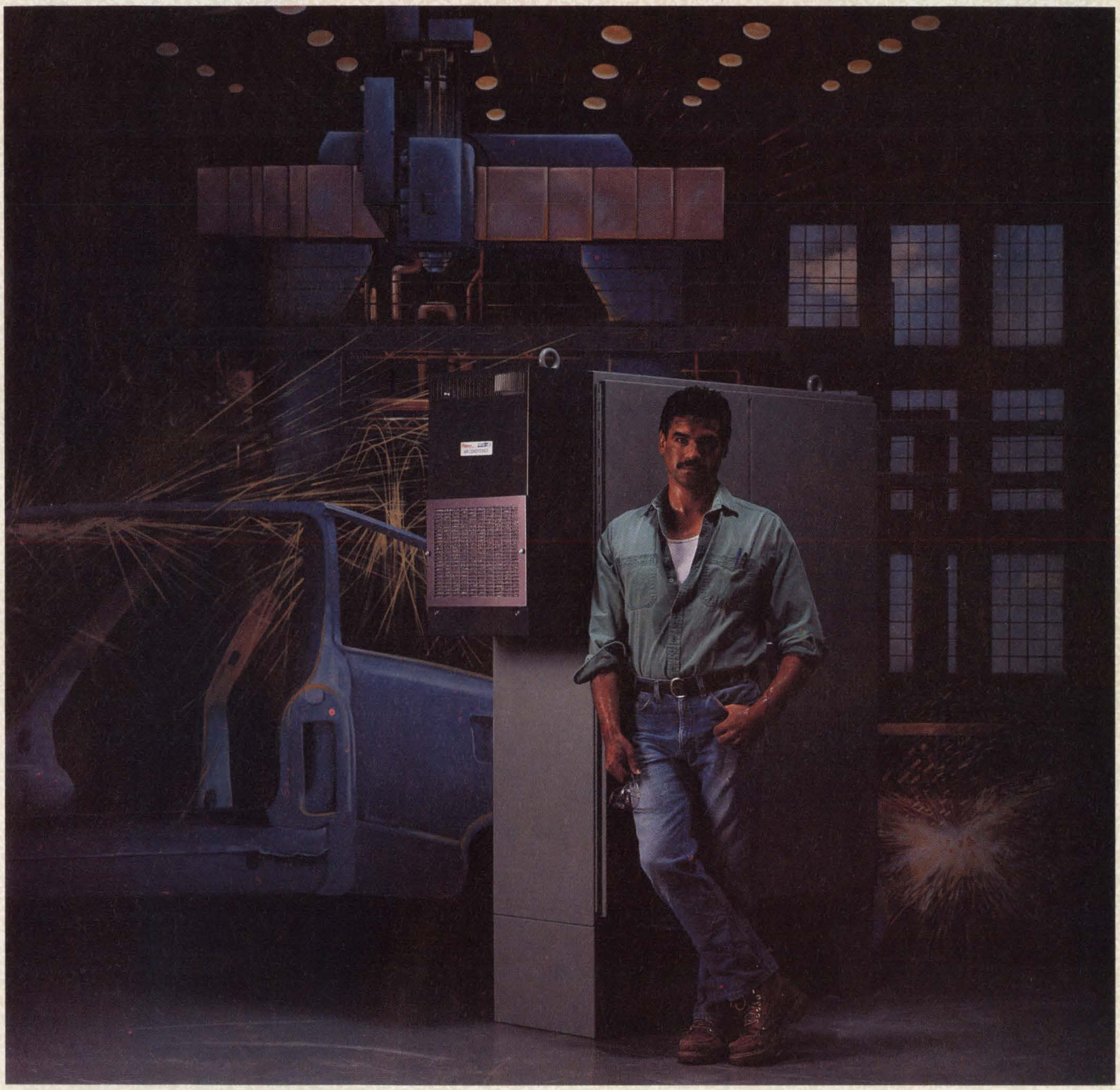
IFD Winner for April 11, 1991

Jim Williams, Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 954-8400. His idea: *"Distortion Stays Under 9 PPM."*

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award and becomes eligible for a $1,500 Idea-of-the-Year award.

If Your Controls Can't Take The Heat, You Will.



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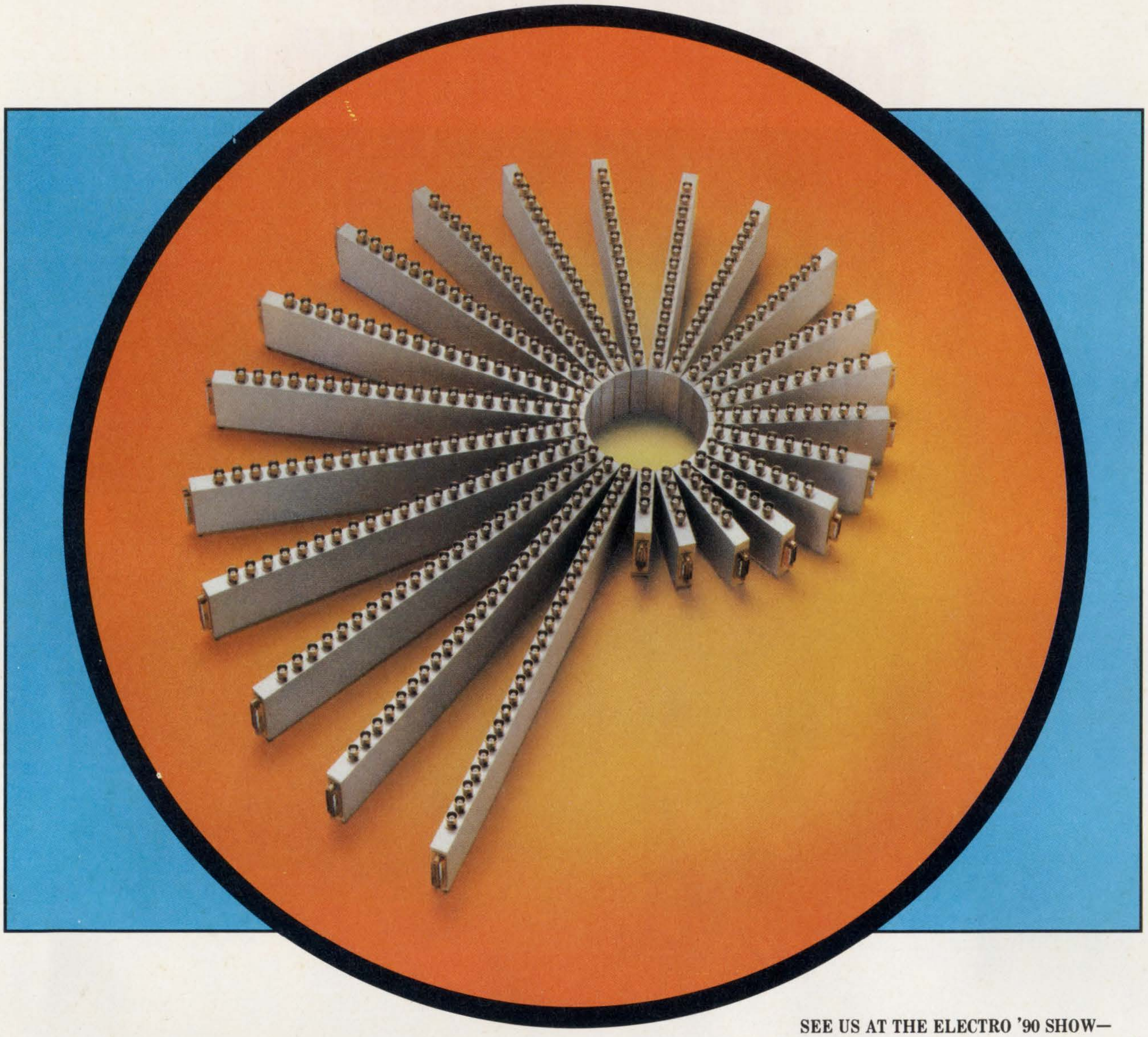
CIRCLE 130 FOR U.S. RESPONSE

CIRCLE 131 FOR RESPONSE OUTSIDE THE U.S.

NEED BROAD-BAND COAXIAL RELAYS? FROM 2 TO 24 THROW, MATRIX HAS THE ANSWER



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CIRCLE 142 FOR U.S. RESPONSE

CIRCLE 143 FOR RESPONSE OUTSIDE THE U.S.

ELECTRONIC DESIGN QUICK LOOK

EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Semiconductor companies based in the U.K. can relax a little. The recession may not be over just yet, but at least it won't get worse, according to forecasts from the Electronic Components Industries Federation. Growth in 1991 will amount to about 1.9%, to make a total available market (TAM) of £1220 million (or $2.074 billion US at an exchange rate of 1£ = $1.70 US).

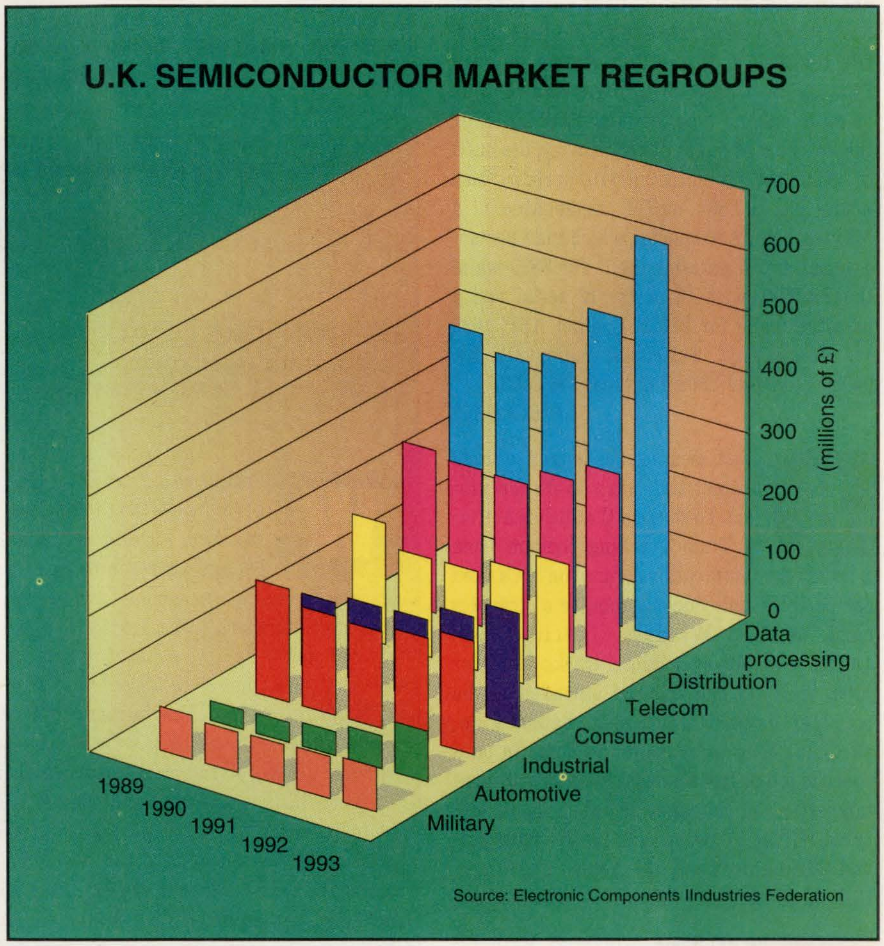
That's roughly equal to the world average for growth in semiconductors. The 2% uptick improves on last year's 6.6% downturn in the U. K. and falls far short of 1989's 11% growth, for a best-ever total available market in the U. K. of £1282 million. The London component industry trade association predicts halcyon days to return to the British market in the next twelve months, forecasting growth of 16.4% in 1992 and 19.7% in 1993.

Weak demand and price pressure on DRAMs hindered 1990 sales of integrated circuits. But a 9.9% fall in the value of discrete components sales is a sobering indication of the problems the U.K. manufacturing industry faces, says the ECIF. Countering that are increasing memory needs of Windows 3 users and use of laser printers with up to 8 Mbytes of built-in memory. These trends are buoying street prices and demand for DRAMs. Memory earnings are expected to rise by 2.7% in 1991 to £300 million.

Memory chips will account for more than 30% of semiconductor sales by 1993, topping £500 million a year. Microprocessors are hot in the U.K., with sales growth in 1991 slated to rise by 3.4%. to £245 million; 32-bit processors are the driving force behind this market, which will grow at twice the rate of the U.K. semiconductor market as a whole, reaching £385 million in 1993.

Longer term, the consumer electronics sector is holding up, with the U.K. now a net exporter for color TVs, and with direct satellite broadcast (DSB) receivers expecting a sales boost from the 1992 Olympic games. Consumer semiconductor sales will rise by 19.7% between 1991 and 1992 to £158 million.

The automotive sector is strongest for U. K. chip sellers, with a staggering 38% growth predicted for the next 12 months. But in dollar (or pound sterling) terms it's the smallest sector at just £54 million in 1992. By 1993, though, sales of chips for automobiles will overtake sales of military-grade devices.



Military products now account for less than 5% of U.K. semiconductor sales and that share is declining fast. Data processing is still the shining star of the U.K. semiconductor market accounting for more than 35% by value at £503 million in 1992. Non-keyboard embedded computers that conform to standard PC architectures are broadening the marketplace.

The telecommunication sector has been flat, with order cutbacks by British Telecom. But new communication services are expected to stimulate demand for ISDN and mobile terminal equipment such as pocket telephones, videotelephones, and facsimile terminals. In addition, mobile communications are pushing demand for microwave discrete components.

Exchange rate fluctuations over the last three years mean that when pounds sterling are converted to dollar values at prevailing rates, a different impression of the U.K. market emerges. In 1990, the sterling value of the market was 6.6% less than 1989; when converted to dollars, 1990 didn't look too bad with a 1.9% increase. The currency markets worked the other way round in 1990 and 1991 and although the market grew by 1.9% in pounds sterling, converting to dollars shows a 3.2% decline.—*Peter Fletcher*

QUICKLOOK

HOT PC PRODUCTS

A low-cost alternative to sharing printers and plotters by local-area networks, the Port Authority from ASP Computer Products has 16 ports for linking PCs to printers and plotters. The three models have a variety of serial and parallel port combinations; each port can have its own baud rate and values for end-of-file timeout. With the Port Authority, most PCs can be linked to printers and plotters using telephone-type, modular RJ12 cables. If the designated ouput device is busy, the buffer spools the job until the path is clear. Each model has a 256k buffer, expandable to 4 Mbytes. The PA800 model, which has 8 ports—4 serial and 4 parallel—sells for $895 while the PA1600, with 16 ports—12 serial and 4 parallel—sells for $1375. Contact ASP, 1026 W. Maude Ave., Suite 305, Sunnyvale, CA 94086; (408) 746-2965; fax (408) 746-2803. CIRCLE 451

Sometimes it takes longer to track project time than to do the project. To remedy that, a Job Activity Time Tracking System from Bolvad Communications runs on PCs and compatibles and doesn't require a graphics card. With a Windows-like interface, JATTS's employee module tracks time for jobs; the data can then be uploaded to the manager module, which also enables a department head or manager to home in on a specific job or track a department. To prevent tampering, the manager module has a security check. The software sells for $75 from Bolvad Communications, 139 Ashley Ct., Cherry Hill, NJ 08003; (609) 428-4315. CIRCLE 452

The HTBasic Advanced Math Library is a collection of fast compiled subroutines for use in signal processing and numerical analysis. The library can be called from a PC-based engineering Basic. Routines include probability density functions, curve fitting, fast Fourier transforms, digital filtering and windowing, built-in waveforms, root finding as well as Bessel and relation functions. HTBasic, compatible with HP 9000 Series Basic, offers HP-style IEEE-488.2 commands, data-acquisition and RS-232 instrument control statements, along with screen, plotter, and printer graphics. The library, available for $400 in the U. S., requires the DOS 386 version of HTBasic, which sells for $925.

Contact TransEra, 3707 North Canyon Rd., Provo, UT 84604; (801) 224-6550; fax (801) 224-0355. CIRCLE 457

OFFERS YOU CAN'T REFUSE

The National Institute of Standards and Technology awards $20 million in grants to develop promising generic technologies. Open to individual companies or joint ventures, the NIST Advanced Technology program isn't restricted to any field of technology. Deadline for proposals is 3 pm EDT Sept. 25. Contact the Advanced Technology Program, A430 Administration Bldg., NIST, Gaithersburg, MD 20899. CIRCLE 453

A monthly technical brief on fuzzy logic theory and its appplication to problems is free from The Huntington Group. The group specializes in real-time, embedded processor and fuzzy logic systems. Free to U. S., Canadian, and Mexican residents, the brief costs international subscribers $10 per year to cover postage. Contact The Huntington Group, 883 Santa Cruz Ave., Ste. 27, Menlo Park, CA 94025; (415) 325-7554. CIRCLE 454

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458, fax (408) 253-6085

Working with inexperienced people on a project is the norm rather than the exception at most companies. For instance, you add individuals to the project team who are straight out of college. Or you hire someone from another company. Or perhaps, the team absorbs those workers moving from one job to the next. You also may have to accommodate a career person who just invested in retraining. Or you have to make room for a manager who did such a fine job on that last project that he or she was just promoted to work in an area that offers more challenge—your area.

To gain effective job performance, you must take into account the diverse distribution of individual talents. Dealing with inexperienced workers is an opportunity to put results from the definition and planning phases to use during the execution phase.

The definition can help communicate the reason for the project and the general direction the team will follow to achieve its objectives. To people doing something for the first time, knowing where they fit in and why their work makes a difference really helps. This information can contribute to generating that "can do" spirit within a team. The team's enthusiasm, dedication, and cooperation can be built around a common motivational vision of the future. In so doing, the stage is set for having the team focus on the tasks at hand, building experience and expertise that benefits the execution phase, while discouraging nonproductive actions.

The plan and, in particular, the to-do lists, serve to set in concrete the expected output from each individual as a function of time over the execution phase. This ordered list tends to communicate to the team member the exact nature of the job. With the activity assignment report, it becomes very clear what must be performed and when it should be completed. For people new to their jobs, this can be the road map to success as they track their progress against the plan and share the results with their manager.

Individually, or with management cooperation, the individual can look for areas of improvement to accelerate work that is lagging behind the scheduled completion date. The impact that late completion of one task has on others can be directly measured. Corrective actions can be synthesized to keep work on schedule. In all, this produces a win-win situation by placing focus on the *right* task at the *right* time.

In certain cases, it becomes clear to the individual and the management team that the appropriate assignment has not been made. Having a good plan makes it possible to make the necessary adjustments. Early detection of task delay (in most cases, it can be observed in a matter of a few weeks) makes it possible to take this action before affecting the scheduled completion date of major project/program milestones.

QUICKLOOK

TIPS ON INVESTING

Have fluctuating market prices caused you to invest at the high and sell at the low? Have you ever planned an investment and delayed it because of timing concerns? If you are like many engineering investors today, you would like to participate more actively in the financial markets, but you're not sure of the right time to invest. And when you think the time is right, it may not be convenient for you to contact your broker or otherwise invest. Or perhaps you don't have enough assets to invest.

Many mutual fund companies offer a program that can help take the market timing worry out of investing and make it more convenient too: the systematic investment plan. With it, you make regular investments, usually monthly or quarterly, of a set amount in the mutual fund(s) of your choice. The plan can:

Build wealth. A systematic investment plan is a disciplined, long-term strategy that can help you build your investment over time so that you may enjoy the compounding power of an increasing investment base. It is unrealistic for many individuals to invest, for example, $100,000 at once. Investing a smaller amount, however, and adding to it regularly still allow you to take advantage of the market's growth potential.

Since the dividends and capital gains produced by a mutual fund's underlying securities are paid out in proportion to the number of shares owned, shareholders who invest several hundred dollars get the same return per dollar as those who invest hundreds of thousands. Of course, the total value of any earnings keeps growing as you invest more.

Reduce volatility. Systematic investing helps reduce the possibility of making a lump sum investment at the wrong time—when the price is at a high. Smaller regular monthly or quarterly investments give you a lower average cost per share over the long term, or *dollar-cost averaging.* An example below, though not showing actual performance, illustrates how dollar-cost averaging can help turn a fluctuating market into an advantage:

Monthly investment	*Share price*	*Shares acquired*
$500	$10	50
$500	$5	100
$500	$10	50
Total $1,500	$25	200

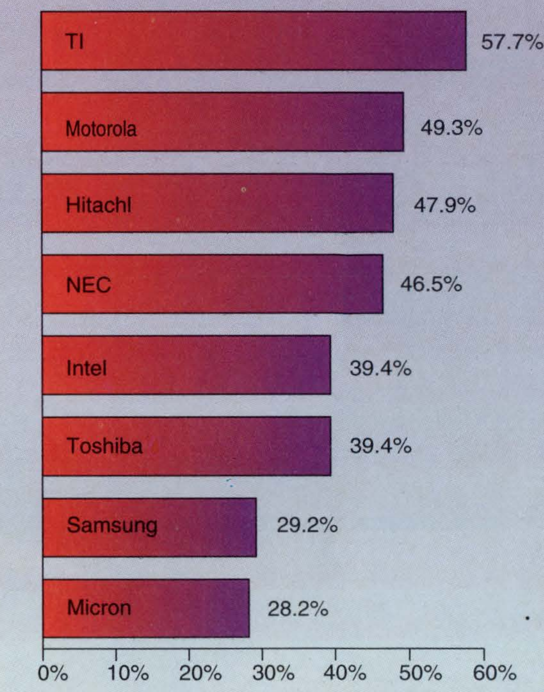
Average cost per share: $7.50	($1,500 invested divided by 200 shares acquired)
Average price per share: $8.33	($25 divided by 3)

You can see how a systematic investment plan may help you reduce volatility by smoothing out the market's highs and lows and also help you work toward your long-term goals. Because a systematic investment plan involves continuous investment throughout periods of fluctuating price levels, you should consider your financial ability to meet your systematic investment schedule before you decide to participate. Although no formula can protect against losses in a declining market or ensure profits, systematic investing can be a valuable part of your overall investment strategy. The time to invest is when you have ready assets.

Henry Wiesel is a financial consultant with Shearson Lehman Brothers, 1040 Broad St., Shrewsbury, NJ 07702; (800) 631-2221 or (800) 221-0073 in N. J. Wiesel invites readers' questions and comments.

DRAM SURVEY

WHICH VENDORS SUPPLY YOUR DRAMs?



Source: a survey of Electronic Design readers by Penton Publishing Inc.

Percentages total more than 100% because readers gave multiple answers.

QUICK NEWS: EDUCATION

A series of Japanese language courses help engineers translate and understand Japanese printed materials without leaving work. By audiographic teleconferencing, voice and computer screens of text, data, and graphics are transmitted live to remote locations with ordinary phone lines.

Students talk with the instructor and use an electronic pen to create or annotate materials on a PC. Basic Technical Japanese I introduces most of the grammar needed for reading in the sciences and engineering and covers 140 of the most often used kanji in these areas. Basic Technical Japanese II completes the grammar necessary for reading technical documents and covers 225 more kanji. Contact Jim Davis, Department of Engineering, Professional Development, Room 4, General Engineering Building, 1527 University Ave., Madison, WI 53706; fax (608) 262-6707. CIRCLE 455

Local-area networks are the focus of a two-day seminar from the Data Tech Institute that covers physical and protocol aspects of networks, standards, inconnectivity, gateways, hosts, servers, and user devices. It also deals with criteria for selecting a network, along with implementation considerations, product evaluations, and cost comparisons. The network course will be held in Morristown, N.J., Sept. 11–12; St. Louis, Mo., Sept. 18–19, and other locations around the U.S. Fee is $795. Contact Data Tech Institute, P. O. Box 2429, Clifton, NJ 07015; (201) 478-5400; fax (201) 478-4418. CIRCLE 456

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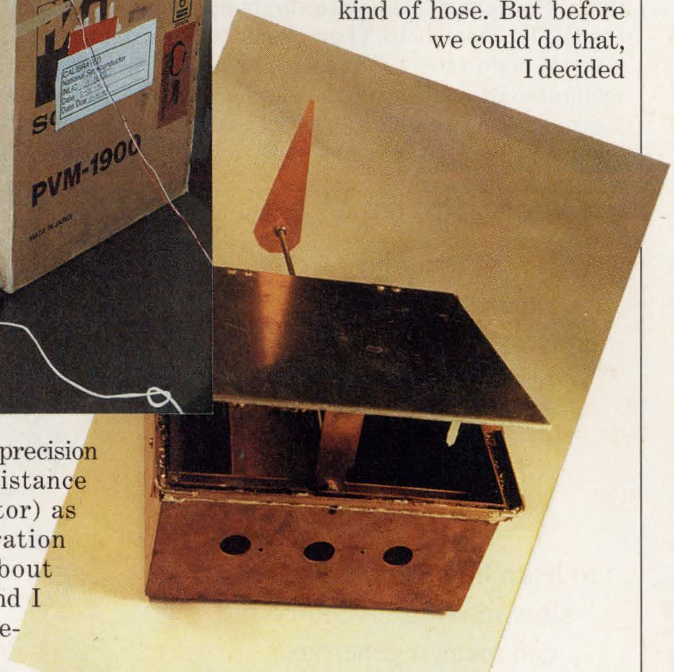
What's All This Box Stuff, Anyhow?

There are many things I do with cardboard boxes. I stow papers in some of the nice boxes we get our Xerox paper in, and we stow circuits and parts in other boxes. And when people complain that our printers are running too loud, we glue some foam rubber inside a big box and clap it over the printer. That usually makes 13 to 18 dB of improvement. The complaints are hushed, along with the printer noise.

But that's not the box I want to talk about today. I want to talk about the big (5 cubic-feet of volume) cardboard box with the Calibration Stickers on it. Most days, this box sits up on top of a tall cabinet, but about once a month we pull it down and put it to work.

BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

About 5 years ago, we introduced a new temperature sensor IC, the LM34. It comes in a small TO-46 hermetic transistor package, and also in TO-92 plastic. And we had the production parts meeting an accuracy spec of ± 1° F, on a decent fraction of production. But how do you test a temperature sensor? And, how do you calibrate the tester? You calibrate a voltage detector by putting the same voltage into two units and making sure that you get the same answer from them. So, with a temp sensor, you have to put two (or more) parts in the same temperature environment and make sure they all give the right answer. In our case, we had several kinds of temp sensors, with a precision platinum RTD (Resistance Temperature Detector) as our primary calibration standard. It cost about $800 15 years ago, and I shudder at today's replacement cost.



So we put a little centrifugal blower to blow air through a piece of corrugated plastic hose and over some of the ICs and also over one or more of our precision calibrated platinum thermometers. We set up two sockets side-by-side so we could put in two units and cross-compare them with quicker response, because devices in the same package will have about the same time-constant.

After a few days, one of the technicians was trying to take some precise data in order to give them to other engineers as "Golden Units." The technician griped that he was getting inconsistent results–and they seemed to be related to when the parts were not shoved all the way down in the socket. Well, the I × R drop could change a little–but this part only drew 55 *microamperes*, and the IR drop could only be 100 nanovolts, whereas we were seeing 300 microvolts–equivalent to 0.03 degrees, for less than an eighth of an inch of movement.

We finally set up some parts with long leads, eschewing the socket, and moved the device under test around in the airstream. We found that there were temperature *gradients* in the air flow coming out of the tube. We tried a longer hose, but that did not make the gradients much better. We thought about using a different kind of hose. But before we could do that, I decided to try a big box for the air to stir around in, to circulate and mix and swirl. Then, after a while, the air poured out onto the DUT's sockets. When we looked for gradients, they were gone, at the level of 0.003°F. So we taped the whole thing together securely. But one day we saw somebody trying to take some cardboard boxes away to make the lab look neater. We realized we had to make sure *our* box would be recognized as valuable. So we made up a big Calibration Sticker and

PEASE PORRIDGE

slapped one on all four sides .

Now, we could have had a stirred oil bath, but that's messy and bulky, and the settling time isn't really much faster than moving air. And when you can use a big leftover cardboard box, the price is right, and it's more fun, too.

Could we have perhaps used a somewhat *smaller* cardboard box? Maybe, but we would have to do a calibration on it, and that wouldn't be worth the effort.

Now, around room temperature, this cardboard box is fine, but at hot and cold temperatures, we normally use a little oven. But everybody knows there are terrible gradients when you run it at 125°C, or –55°, or even at room temp! So we put in a box to surround the DUTs. Small help. Then we added a metal plate (about 1/8-in.-thick aluminum) so we could strap the platinum thermometer (we had a compact one, about 8 in. long) to the same plate that the DUTs were set into. Still, there were errors. The hot air coming from the oven's duct would blow on one corner of the box and heat it worse than another side of the box. And the whole process was quite slow if you kept the box cover closed. If you want to guess how many hours of tests we ran to discover which parts really had what error at what temperature, it was *plenty*.

We finally boiled the testing problem down to two problems–we had to get a quick response when we changed the temperature, as if the box were open, and we had to get minimum gradients when we were near the final temperature. We solved the problems with a box in a box. The outside box had some small slits and baffles, so the oven's air could not blow directly on the inner box. Then we put a lever on the cover so we could open the cover to get fast response for 98% of the temperature change. After that, we turned the lever and closed the cover to get a nice slow settling

And all it took was a box inside a box, inside the oven. Could we have used cardboard for that? Well, in concept we could have, but it would get pretty flaky after just a few hours at 125°C, so of course we used copper-clad material, which was reasonably stable and easy to work with (the covers did keep warping a little bit, and we had to keep flattening them out). When the boxes were closed, the gradients between the metal plate, the 25 parts mounted in it, and the platinum sensor were really quite acceptable, <0.05°F.

All for now. / Comments invited! /
RAP / Robert A. Pease / Engineer

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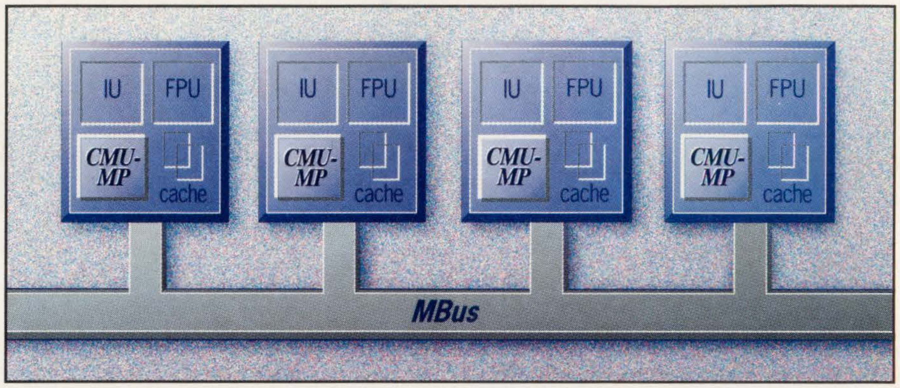

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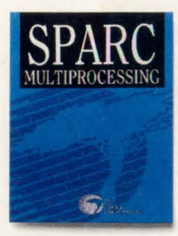

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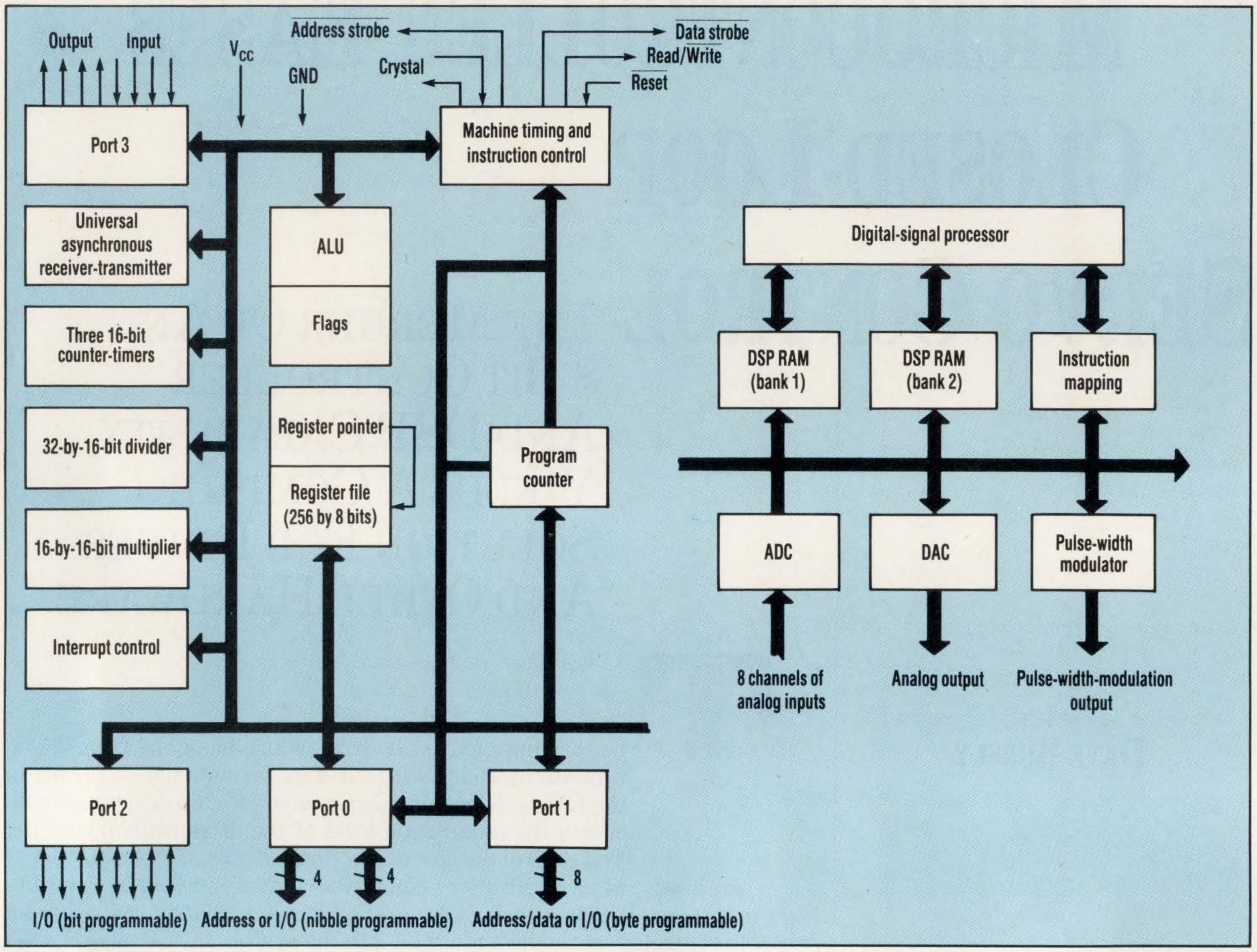
DAVE BURSKY

The shrinking hard-disk drive, which has gone from 3.5-in. formats to 2.5-in., with sub-2-in. formats not so far off in the future, is pushing disk-controller-chip designers to increase the integration level of the drive control circuits. The control designers are further stressed because most of the small drives embed the control and interface circuits right in the drive, unlike previous generation systems that typically used a separate controller card which plugged into the system bus. Designing the highly integrated controllers used for such systems often requires knowledge spanning several areas of expertise—knowledge that often goes beyond the level any one company can accumulate.

By pooling their engineering teams to work in parallel with each other, two companies, Oak Technology Inc. and Zilog Inc., are taking on the drive-control area. They've jointly defined a two-chip combination that can replace most of the digital logic and some of the analog circuitry typically found in a hard-disk drive.

Zilog will combine its high-integration microcontroller expertise with digital-signal processing to handle internal spindle control of the hard-disk drive and the read/write head servo control. Oak Technology will handle the data-path interface from the recovered serial data stream to the parallel integrated-device electronics (IDE) interface. The Oak Technology circuit will also include Reed-Solomon error checking and correction, buffer-control logic for a large off-chip DRAM-based buffer, power-management circuitry, and interrupt-handling capability. The combination of the two chips will produce the highest-integration commercial solution for hard-disk-drive control. Zilog expects to sample its controller this quarter, while Oak plans to have samples ready near the end of the year.

The Zilog Z86C94 microcontroller combines a Z8 CPU core, a 16-bit auxiliary DSP block, 8-bit analog-to-digital and digital-to-analog converters, a serial peripheral interface, and a pulse-width modulator *(Fig. 1, left)*. That combination of features suits the controller for applications required in disk and tape drives, such as digital closed-loop servo control. It also suits it to applica-



1. DEDICATED MULTIPLIER and divider logic on the Z8 controller core give the basic CPU a good computation speed (left). However, for closed-loop servo control systems in such applications as disk drives, even faster computations are required. Consequently, a dedicated block of logic optimized for digital-signal processing was added to the control chip (right). The block features a single-cycle multiplication capability, multiple memory banks, and a multichannel analog-to-digital converter.

tion in voice/data processing, automotive systems, and high-end consumer products. The combination of DSP hardware for fast numeric computations (including a hardware multiplier circuit) and fast ADCs and DACs provides engineers with plenty of design margin with which to implement the closed-loop servo.

The Z8 CPU core already contains an enhanced-computation capability. Its hardware multiplier can perform a 16-by-16-bit multiplication in a mere 1.7 μs, or a 32-by-16-bit division in just 2 μs. Still, even shorter computation times are needed for some embedded control applications.

To maximize the chip for such computations, a block of logic optimized for digital-signal processing was incorporated on the chip. That DSP block, an offshoot of a DSP core macrocell Zilog licensed last year, serves as a slave processor to the Z8 CPU core.

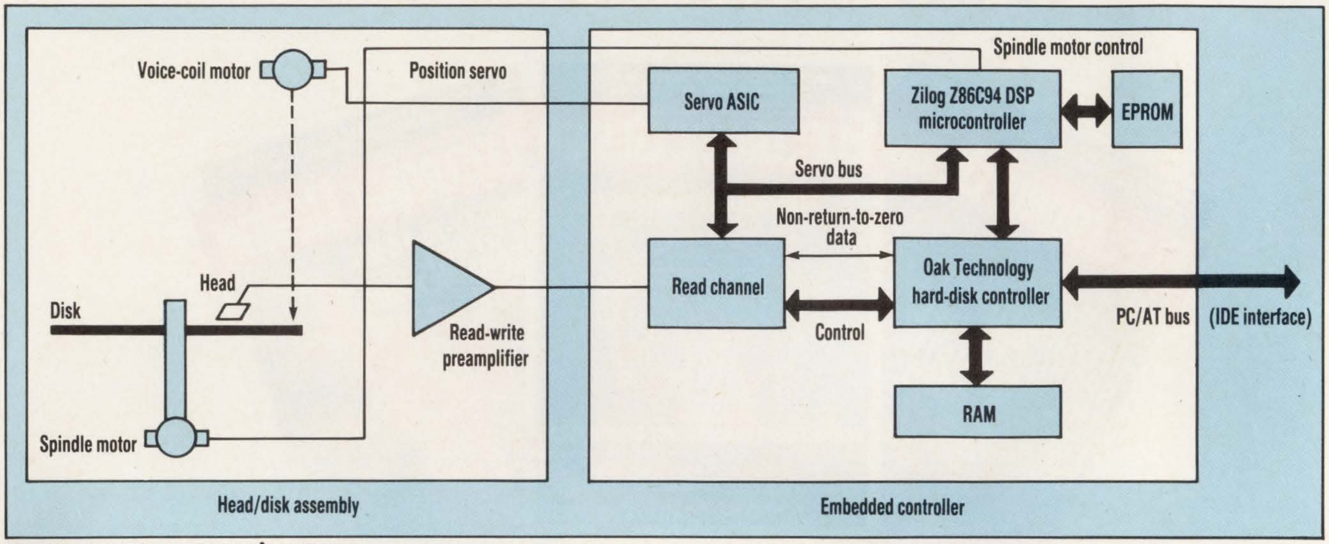
SELF-CONTAINED RAM

The DSP block has its own 128 bytes of RAM for use as program storage, and another 256 bytes (128 words) of RAM storage for related data *(Fig. 1, right).* The data-storage area in the DSP block is set up as two banks of RAM, each containing 64 words—ideal for handling data and coefficients. Of those 256 bytes, 208 are also mapped into the Z8 CPU's address space to simplify parameter passing.

The streamlined DSP block executes most instructions in just one clock cycle. Thus, a 16-by-16-bit multiplication and accumulation pipelined operation is completed in just one cycle. Six clock cycles is all it takes to complete a scalar 16-by-16-bit mulitplication and accumulation operation. For a system with a 10-MHz clock, that translates into a time of 100 to 600 ns.

As many as eight channels of analog inputs can be sampled and then digitized and fed to the Z8 CPU core or the DSP block. To achieve a 2-μs conversion time, a half-flash converter architecture was used on the chip. The output DAC circuit has a

HIGH-PERFORMANCE DISK-DRIVE CONTROL



2. WITH TODAY'S BEST integration efforts, the main chip count in a disk drive can be reduced to four logic chips plus memory. In addition to the combination controller and DSP unit from Zilog, and the data-path controller from Oak Technology, two other chips comprise the typical complement embedded in the disk drive: a servo chip for the head movement, and a read-channel chip to link to the head.

settling time of about 3 μs and includes a 4-bit digitally-controlled gain stage. The pulse-width-modulator output, which can be used to control motors, can operate at frequencies as high as 40 kHz.

The Z8 CPU core employed in the 86C94 microcontroller IC is more than just the CPU. Along with the

basic instruction processor, it includes a number of system resources. The chip has three 16-bit counter-timer circuits (two of which have 6-bit prescalers, one has a 4-bit prescaler). One of the counter-timer circuits also has five capture and three compare registers, which should simplify the task of timing interface.

There are also 25 I/O lines on the 86C94 microcontroller IC that permit the microcontroller chip to control many system aspects. For program and data storage, the chip can address 64 kbytes of external memory. In addition, the chip contains a 256-byte register file with 236 general-purpose registers.

ON-CHIP OSCILLATOR

To help minimize system complexity, an on-chip oscillator lets the circuit run from a crystal or be driven by an off-chip clock. Dual serial interfaces are included on the chip for communications. One of those ports is fully asynchronous, and enables the chip to communicate with most system consoles. The other port, a simpler, synchronous serial interface is available to serve as a low-pin-count chip-to-chip communications bus.

Like the Oak Technology chip, the microcontroller chip includes three power modes that make it possible for the chip to serve in power-sensitive applications, such as laptop computers.

In today's disk drives, the state of the art in analog integration will still require some power control for the spindle motor and some high-quality analog circuitry for the read-channel data recovery. However, combining the 86C94 microcontroller IC and the controller from Oak Technology will trim the chip count to just four chips (not counting the buffer- or program-storage memory chips).

That low chip count would solve the space problems with 3.5-in. and even most 2.5-in. disk drives *(Fig. 2)*. As semiconductor IC processing technology improves and the blocks get implemented in a submicron CMOS process, the Zilog and Oak Technology chips could eventually merge into a single control chip.□

PRICE AND AVAILABILTY

The Zilog Z86C94 microcontroller comes in either an 84-lead plastic-leaded chip carrier or an 80-lead plastic quad-sided flat package. In lots of 1000, the controller starts at $15 each. At present, prices haven't been set for the host-control chip from Oak Technology.

Oak Technology Inc., 139 Kifer Ct., Sunnyvale, CA 94086; Scott Alberts, (408) 737-0888. **CIRCLE 512**

Zilog Inc., 210 Hacienda Ave., Campbell, CA 95008; Paul Vroomen, (408) 370-8000. **CIRCLE 513**

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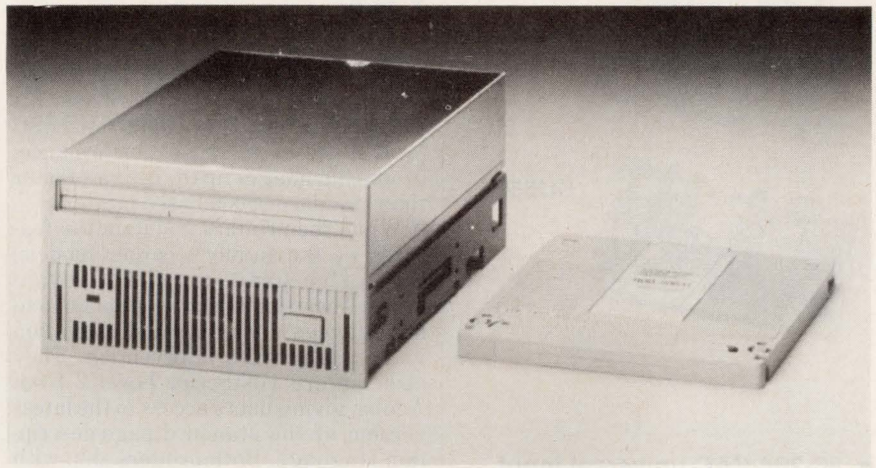
FAST-SPINNING OPTICAL-DISK DRIVE SUSTAINS 1-MBYTE/S DATA READS

DAVE BURSKY



Delivering the highest sustained transfer rate of any optical-disk drive, the Ricoh RO5031E can deliver data at a sustained rate of 1 Mbyte/s to the host interface, and at SCSI-1 or SCSI-2 data rates in bursts of up to 256 kbytes. The magneto-optical drive achieves some of the speed thanks to an increased spindle speed of 3600 rpm—that's twice the speed of previous-generation read-write optical drives. However, the drive is also backwards- compatible with the previous-generation drives because it includes a half-speed mode that drops the spindle rotation speed to 1800 rpm.

In addition, the drive achieves an average access time of just 37 ms—that's a third or less the access time for most other optical drives. The average seek time is also an impressive 28 ms. To get the short access time, the drive employs a new single-step direct-seek head-movement scheme and a split-head optical system. Storing up to 650 Mbytes per optical disk (up to 297 Mbytes/side, formatted), the fully ISO-standard-compatible drive now lets rewritable optical media take a place in a computer system's main storage hierarchy. Previous optical drives were too slow and were often relegated to secondary storage.

Although the drive can read data at 1 Mbyte/s, data can be written to the disk at only half that speed—500 kbytes/s. The reason for the 50% reduction in transfer rate is the two-pass approach required by the magneto-optic storage technique, which erases the disk on the first pass and then writes the new data on the second pass. If the verify option is selected, the drive would require a third pass to read the written data to verify that the data were written correctly. Consequently, the drive's transfer rate decreases to 333 kbytes/s.

A large built-in dual-ported RAM buffer of 256 kbytes can send data files of up to that amount in bursts across the drive's embedded SCSI interface. That interface can handle SCSI-1 or SCSI-2 protocols and commands, and will allow burst transfers at effective rates of up to 4 Mbytes/s.

To get the short access time, Ricoh designers came up with the direct-seek scheme. The scheme lets the optical head refer to the actual grooves on the media by using track-cross signals. By counting the crossings, the head can be moved directly to the desired track position.

In previous drives, the access procedure was a two-step process consisting of a coarse seek and a fine seek. And the coarse and fine seeks were referenced to an off-disk scale embedded in the carefully aligned drive.

Another improved feature is the split-head optical system. The moving portion of the head now contains only the objective lens and the mirror prism portions of the optical system, rather than the entire optical system. That split of the head reduces its weight to just 35 grams, versus about 100 grams in previous optical drives. Less weight means faster movement and shorter access times.

One negative aspect of the split optics is that a more powerful laser diode is needed because the disk surface is now further away from the originating point of the beam. The higher-power laser diode, in turn, requires forced-air cooling to minimize the heat build up in the small confines of the drive.

Furthermore, the optics are kept in a dust-proof sealed environment that's separate from the electrical portion of the system. This improves data integrity and prevents ambient air from being swept past the optical head by a small built-in cooling fan. Thus, the drive can boast an error rate of just one bit out of every 10^{12} bits read. The RO5031E drive also has an MTBF of over 30,000 hours. In addition, optical data cartridges are available from Ricoh. The cartridges have a guaranteed lifetime of more than 10 years and can handle over 10 million erase and write cycles.

In single-unit quantities, the magneto-optic drive sells for \$3990, including power supply and one optical data cartridge. OEM discounts will be available. The drive will also be sold as an external storage device in a case with power supply. Optical disks will sell for \$230 each in small quantities. Along with the introduction of the new drive, the company reduced prices for its existing optical drive, the RO-5030EII, from \$3900 to \$3450. Samples are available from stock.

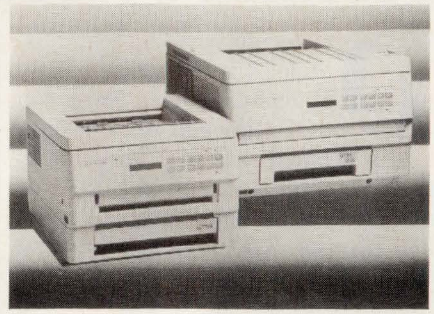
Ricoh Corp., File Products Div., 5150 El Camino Real, Ste. C-20, Los Altos, CA 94022; Ken Yokoo, (415) 962-0443. **CIRCLE 571**

HIGH-PERFORMANCE LASER PRINTERS BASED ON RISC

Two new additions have been made to Texas Instruments' microLaser printer family, the microLaser Turbo and the microLaser XL Turbo. Both models are built with RISC processors to increase performance, producing images up to six times faster than standard 68000-based printers.

While the printers maintain the features of the family's earlier models, they offer some significant advantages. These include intelligent switching between interfaces and emulation without any user intervention. They also feature PostScript Level 2 from Adobe, giving users access to the latest version of the standard page-description language. Both printers ship with 35 PostScript fonts. Also included is PCL 4 emulation, giving users the benefit of both PostScipt and HP LaserJet Series II compatibility.

The difference between the Turbo and the XL Turbo is in the printing speed. The Turbo is capable of 9 pages/minute, while the XL Turbo can do 16

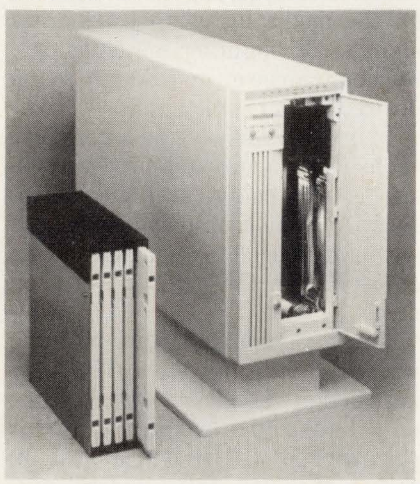


pages/minute. Both models come with 2.5 Mbytes of RAM (2 Mbytes on the processor board and 0.5 Mbytes on the main controller board). Up to 8 Mbytes can be added. More fonts can be accessed by attaching an external disk drive through a SCSI interface. Both models will be available in September. The microLaser Turbo sells for $3199; the XL Turbo costs $5199.

Texas Instruments Inc., *Information Technology Group, P.O. Box 202230, ITG-9122, Austin, TX 78720; (800) 527-3500.* **CIRCLE 572**

■ *RICHARD NASS*

12-IN. OPTICAL DRIVE HOLDS 28 GBYTES



By employing a five-cartridge magazine in a 12-in. optical drive, users can store up to 28 Gbytes of data. The LF4500 RapidChanger's high-speed disk changer requires less than 3 seconds to exchange cartridges. To meet the needs of changing environments, cartridges can be moved between single- and multiple-cartridge standalone drives and jukebox configurations. The RapidChanger is designed to fill the gap between the single-cartridge drive and the jukebox. It employs a sliding magazine rather than the conventional elevator mechanism used in other multiple-cartridge systems. The magazine slides laterally within the drive housing. The RapidChanger offers an 80-ms access time and transfers data at 700 kbytes/s. It's available with a pedestal or in a 19-in. rack-mount configuration.

Laser Magnetic International Co., 4425 ArrowsWest Dr., Colorado Springs, CO 80907; (719) 593-4269. **CIRCLE 573**

8-IN. DISK TRANSFERS 27 MBYTES/S

High-volume data-processing bottlenecks are eliminated by the Sabre Parallel Transfer Disk (PTD) from Seagate Technology. The 8-in. drive transfers data at 27 Mbytes/s and has a storage capacity of 2.3 Gbytes. The high data-transfer rate is achieved by simultaneously employing nine read/write heads. The drive's average seek time is 12 ms. The Sabre PTD, which is available now, was jointly developed by Seagate and Cray Research Inc. Cray recently announced a proprietary implementation of the Sabre PTD.

Seagate Technology, 920 Disc Dr., Scotts Valley, CA 95066; (408) 438-6550. **CIRCLE 574**

VXI FUNCTION GENERATOR FEATURES SWEEP MODES

The Model 1370 programmable sweep/function generator covers 0.01 Hz to 12 MHz in a one-slot C-size VXIbus module. The instrument works as a continuous, triggered, burst, or gated signal source, producing sine, triangle, square, square-complement, dc, or external-width waveforms. Sweeping can be either linear or logarithmic. The unit can send or receive triggers from any of the eight VXIbus TTL trigger lines. Output levels range from 100 mV to 10 V pk-pk into 50-Ω, and 200 mV to 20 V pk-pk into an open circuit. Users can program the offset to vary the waveform baseline from –5 to +5 V into 50 Ω, or to vary the dc output in the dc mode. The unit runs the Standard Commands for Programmable Instruments (SCPI). The Model 1370 costs $2695, with delivery in 4 to 6 weeks.

Wavetek San Diego Inc., 9045 Balboa Ave., San Diego, CA 92123; (800) 874-4835. CIRCLE 575

DESIGN-TO-TEST SOFTWARE OFFERS NEW FEATURES

TDS Release 4.0 offers a significantly improved graphical interface and new WaveBridge modules with advanced tester features and flexible support for a wide range of test-program-generation methods. The TDS design-to-test software also includes menu software, enhancements to Verilog input and output converters, increased performance, and expanded network licensing. The WaveBridge modules convert simulation data from one or more waveform databases into a structured form. Then they analyze the data and report problems that would prevent the target tester from reproducing the waveforms. WaveBridge runs 300% faster than previous software. The graphical interface, WaveMaker, interactively displays test-compatibility reports and pinpoints problems, allowing users to create, capture, display, analyze, and modify digital stimulus and response data. The Verilog input converter now reads Verilog VCD files, and the output converter produces Verilog VHDL stimulus files. TDS Release 4.0, which is available now, starts at $20,000, depending on configuration. Upgrade options start at $10,000.

TSSI, 8205 S.W. Creekside Pl., Beaverton, OR 97005; (800) 642-9281 or (503) 643-9281. CIRCLE 576

BOARD OFFERS IEEE-488 LINK FOR OEM USE

The Personal488/OEM-P is designed for OEMs who want to integrate an IEEE-488.2 interface into their products. The hardware-software package features C-linkable libraries of IEEE-488.2 functions, DMA and interrupt-driven I/O capability, 8- and 16-bit hardware options, and high-performance RS-232 support. The Personal488/OEM-P development kit includes an I/O adapter board that fits into a half-size PC bus expansion slot, a software interface consisting of a linkable library of Microsoft C routines, and complete documentation. The 8- and 16-bit development kits cost $795 and $895, respectively. OEM pricing for 100-unit quantities is $195 and $295 each, respectively.

IOtech Inc., 25971 Cannon Rd., Cleveland, OH 44146; (216) 439-4091. CIRCLE 577

RUN-TIME TOOL DEBUGS 80386SX SOFTWARE

The CodeTAP 386 SX run-time software development tool is designed to transparently debug software programs running on the Intel 80386SX microprocessor. The system differs from other run-time tools, such as software monitors, in its ability to monitor and control execution in the target without using target memory or I/O capability, or requiring prior-code changes. Code can be generated by a variety of popular compilers with additional support. The ability to debug using original source code enhances productivity. CodeTAP 386 SX allows engineers to single-step through all modes, both protected and real, and the difficult code in between. A windowed, mouse-driven interface makes it easy to oversee target operations. The system operates at full clock speeds. The use of custom gate array technology allows full access to data structures, arrays, dynamic variables, and access and execution breakpoints. The complete tool chain consists of a Target Access Probe for the 80386SX, an RS-232 communications adapter, a windowed source-level debugger, and software. The system works with PC/AT and compatible hosts. CodeTAP 386 SX is available now with a starting price of $5995.

Applied Microsystems Corp., 5020 148th Ave. N.E., Redmond, WA 98073-9702; (206) 882-2000. CIRCLE 578

TEST MODULE SPEEDS ACQUISITION, ANALYSIS

The HMX10 high-speed digital measurement system adds 200-MHz digital data acquisition and comprehensive digital analysis capabilities to the SigmaSeries and Advance Functional TestStations. When combined with the Spectrum functional test and diagnostic software, the HMX10 increases diagnostic resolution and reduces program development time for testing complex digital and mixed-signal boards.

To acquire a waveform from the desired node on a unit under test (UUT), the HMX10 samples asynchronously in several modes up to 200 MHz and synchronously in several modes up to 40 MHz. The system then analyzes the waveform by comparing it to an arbitrary but predefined list of criteria called measurement steps. Access to UUT nodes is through manual probing or test-fixture connections through multiplexer pods.

Interactive software menus ease HMX10 setup and operation. Users first select the sources for the input, start, trigger, and stop functions. Then they specify the input threshold level. Finally, they define the number of iterations and the number of edges in each sample.

A Waveform Display Window helps operators acquire waveforms interactively, learn or verify a board's nodal-operating characteristics, and build a database of reference waveforms. The Editor Window specifies measurement criteria and saves them in a database. Once defined, the measurements can be run interactively or with the Spectrum fault dictionary for automatic diagnosis.

The SigmaSeries HMX10 is available on a 6-week delivery schedule at a list price of $9995.

***John Fluke Mfg. Corp.**, P.O. Box 9090, Everett, WA 98206; (800) 443-5853.* **CIRCLE 579**

■ *JOHN NOVELLINO*

TIMING GENERATOR ADDS PRECISION TO VXI SETUPS

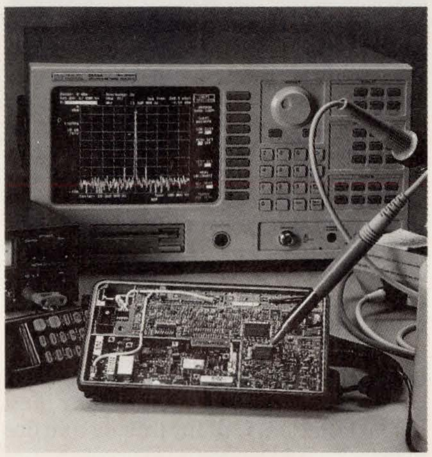
With 5-ns resolution over a 5-kHz to 20-MHz range, the Model 6459 provides a high-precision timing generator for VXIbus test systems. The generator, housed in a one-slot C-size module, outputs up to eight timing strobes that are sourced onto the VXI local bus. The system's digital test modules can select these signals for use as stimulus, response, or stimulus-data formatting timing waveforms. The function of each timing waveform can be assigned to separate channels or groups and data-format waveforms. The 6450 Series test executive firmware will automatically allocate the strobes without programmer intervention. The Model 6459 costs $5900, and delivery is within 16 weeks after receipt of an order.

Racal-Dana Instruments Inc., 4 Goodyear St., Irvine CA 92718; (800) 722-3262. **CIRCLE 580**

ONE UNIT DOES SPECTRUM, NETWORK ANALYSIS

A combination spectrum/network analyzer performs frequency, distortion, phase, group-delay, return-loss, and impedance measurements over a 10-Hz to 150-MHz range. The HP 3589A offers the capabilities of a dedicated spectrum and network analyzer for the cost of a spectrum analyzer alone. The company introduced a pair of 50- and 75-Ω S-parameter test sets to be used with the analyzer.

The HP 3589A's time-gated, spectrum-analysis option facilitates measurement of burst or time-varying signals, which are common in applications like communications, disk drives, and optoelectronics. By making readings only during the desired portion of a signal, this option allows standard measurements (noise level, signal-to-noise, and distortion) on difficult dynamic signals. Also, new functions make it easy to interface the HP 3589A with down-converters, high-frequency analyzers, and receivers by correcting for phenomena like frequency inversion.



The analyzer makes measurements in 50- and 75-Ω environments and offers group-delay, polar, and Smith-chart formats. For audio or broadband analysis, the analyzer performs log sweeps and includes a 1-MΩ input. The S-parameter test sets add complete 2-port-analysis capability.

A standard PC keyboard can be used to program the instrument using HP Instrument Basic. A built-in 3-1/2-in. disk drive saves test results, measurement states, and programs.

Prices for the HP 3589A analyzer start at $21,750, with delivery estimated within 2 weeks. The HP 35689A and HP 35689B 50- and 75-Ω test sets cost $3650 and $4000, respectively.

***Hewlett-Packard Co.**, 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900.* **CIRCLE 581**

■ *JOHN NOVELLINO*

MULTIFUNCTION COUNTER OFFERS 0.5-PPM TIMEBASE

The Model 1856 counter measures frequency, period, average period, and total counts over a 5-Hz to 1.3-GHz range. For improved accuracy and repeatability, the unit includes a temperature-compensated crystal-oscillator timebase. The timebase features 0.5-ppm stability at 23°C, ±5°C; and 1-ppm stability from 0 to 50°C. Sensitivity at 1.3 GHz is 50 mV. For accurate very-low-frequency measurements, the Model 1856 uses period measurement. The period-function's range is from 0.285 μs to 0.2 seconds. In the totalize mode, the unit counts up to 99,999,999 pulses from 5 Hz to 10 MHz. The counter exceeds FCC requirements for adjusting transmitter frequency. The Model 1856 counter is available at a suggested list price of $485.

***B+K Precision**, 6470 W. Cortland Ave., Chicago, IL 60635; (312) 889-1448.* **CIRCLE 582**

COMPACT UNIT EXTENDS IEEE-488 BUS TO 300 M

IEEE-488 users can extend their bus system to 300 m without compromising performance or modifying application programs by using a pair of GPIB-130 bus extenders. The expanded system can handle up to 28 devices, 14 attached to each extender. The compact unit (94 by 76 by 24 mm) maintains the ability to respond to parallel poll commands to the full 300 m. Data transfers in the buffered mode are made at 900 kbytes/s, regardless of cable length. In the unbuffered mode, which uses IEEE-488 handshaking to confirm each byte at the sender and receiver, transfer rates reach 790 kbytes/s at 5 m and decrease to 140 kbytes/s at 300 m. The GPIB-130 is available immediately at a price of $995.

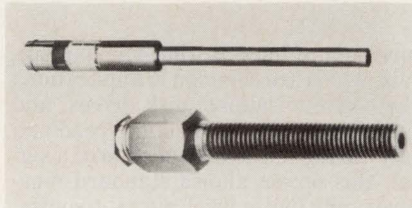
***National Instruments**, 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488 or (512) 794-0100.* **CIRCLE 583**

POWER RECTIFIERS COME IN SMT PACKAGES

Two plastic surface-mounted packages house power Schottky and ultra-fast rectifiers. The 1-A package contains the MURS105T3 series of ultra-fast rectifiers with ratings from 50 to 600 V. The 3-A package carries the MURS305T3 series of rectifiers, also rated from 50 to 600 V, and the MBRS320T3 series of Schottky rectifiers rated from 20 to 40 V. A low-V_f (0.395 V) version of the Schottky device is available. The rectangular devices are easier to handle than conventional leadless diode packages and come on tape and reel for automated assembly. Pricing for the Schottky devices ranges from $0.78 to $1.12 in the 1-A package and from $1.02 to $1.08 in the 3-A package. Ultra-fast rectifiers range from $0.74 to $0.94 in the 1-A package and from $0.96 to $1.16 in the 3-A package. All pricing is for quantities of 2500. Delivery is from stock to four weeks.

Motorola Inc., 5005 E. McDowell Rd., Phoenix, AZ 85008; Larry Baxter, (602) 244-5757. **CIRCLE 584**

PROXIMITY SENSOR WITHSTANDS HIGH SHOCK

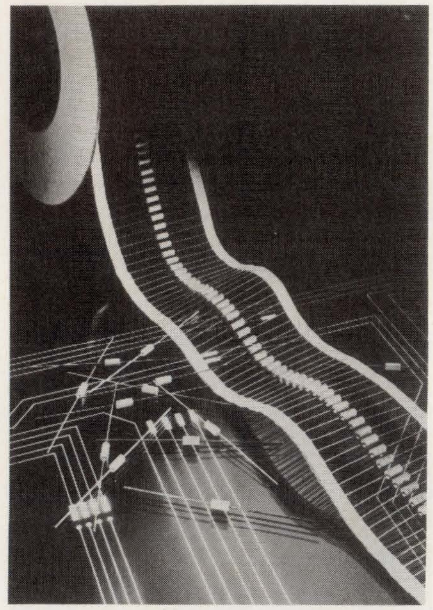


An inductive proximity switch now comes housed in an extra-thick, hardened-steel mechanical housing that withstands physical contact. The "banking screw" is a rugged device that incorporates an electronic switching output that's protected against excessive shock loads. Sensor life is prolonged by preventing wear and cracking of the brittle ferrite core, which would destroy the circuit's integrity. Typical applications include use in X-Y mechanical slides. Call for pricing and delivery.

Baumer Electric Ltd., 122 Spring St., C-6, Southington, CT 06489; (203) 621-2121. **CIRCLE 585**

TIME-DELAY FUSE SAVES BOARD SPACE

Time-delay performance in a space-saving subminiature molded package is featured in the Pico III Slo-Blo fuses. Available in ratings of 1/2 A through 7 A at 125 V, the fuses are well suited for applications with an inrush current



that would typically open a fast-acting fuse. The time-delay feature helps solve the problem of nuisance fuse blowing. The fuse's high lead-pull strength means greater durability during installation. Call for pricing and delivery.

Littelfuse Inc., 800 E. Northwest Hwy., Des Plaines, IL 60016; (708) 824-1188. **CIRCLE 586**

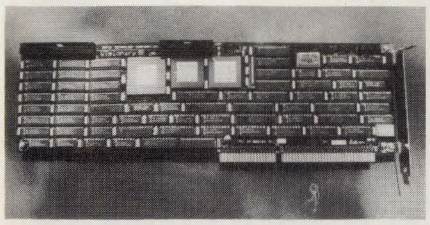
RF POWER TRANSISTORS IN SOT-223 PACKAGES

Claimed as the world's first RF power transistors in a standard SOT-223 surface-mounted package, the BLT50, BLT80, BLU56, and BLU86 are all capable of dissipating 1 W. The devices save considerable pc-board area and assembly time for such equipment as pocket and handheld cellular and portable mobile radios. The BLT50 and BLU56 are optimized for use at 470 MHz and voltages of 7.5 V and 12.5 V, respectively. The BLT80 and BLU86 are for use in 900-MHz equipment and are also rated at 7.5 and 12.5 V, respectively. Pricing is in the $1.30 range for lots of 1000. Delivery is in 8 to 12 weeks.

Philips Components, Discrete Products Division, 2001 W. Blue Heron Blvd., Riviera Beach, FL 33404; (407) 881-3308. **CIRCLE 587**

GET FULL-MOTION SPEEDS OF 30 FRAMES/S

Built around the LSI Logic JPEG chip set, the Visionary real-time JPEG compression board achieves CCIR-601 resolution at full-motion speeds of 30 frames/s. The board connects to a vid-



eo-capture card, enabling real-time video data or stills to be privately exchanged between the LSI chips and the frame buffer. This avoids any bottlenecks associated with the ISA bus. Visionary and an appropriate frame buffer can replace an analog video disk to reduce the cost and complexity. The board and its associated software run under DOS or Windows 3.0.

Rapid Technology Corp., Amherst Commerce Park, Suite 43, 4226 Ridge Lea Rd., Amherst, NY 14226; (716) 833-8533. **CIRCLE 588**

IMAGE-COMPRESSION CARD RUNS REAL TIME

An AT-bus add-in card, compatible with the Joint Photographic Experts Group standard for image compression, can compress color or gray-scale video images by factors as high as 100:1. The Vidcom board accepts NTSC or PAL video signals from TVs, VCRs, Camcorders, etc. It first digitizes the images and then compresses them with its on-board CL550B compression processor chip (built by C-Cube Microsystems). The board can transfer uncompressed data at a rate of 27.65 Mbytes/s to the hard-disk subsystem; however, such a rate can't be handled by the AT bus. When compressed using an 80:1 ratio, the data rate drops to just 345.6 kbytes/s—a very manageable transfer rate for most hard-disk drives. Both real-time compression and decompression can be done by the board, which delivers an NTSC analog signal to its output connector. Image resolutions can be as high as 8192 by 8192 pixels by 24 bits. The Vidcom card connects with a cable to a standard VGA card and overlays its output onto the VGA display. Available next quarter, the card sells for $995 in single units.

Specom Technologies Corp., 3673 Enochs St., Santa Clara, CA 95051; (408) 736-7832. **CIRCLE 589**

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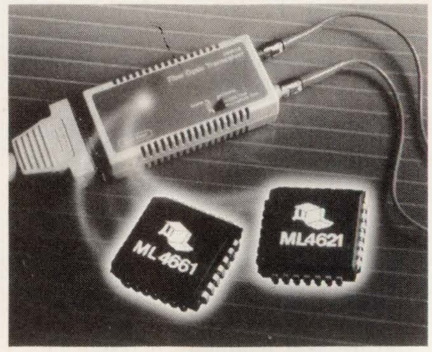
CHIP SET SIMPLIFIES FIBER TRANSCEIVERS

A two-chip transceiver chip set for fiber-optic-based Ethernet local-area networks lowers the cost of implementing the IEEE 802.3 fiber-optic interrepeater link (FOIRL) standard. The FOIRL standard allows Ethernet links to extend the distance between repeaters to as much as 1000 m, broadening the area covered by an Ethernet network.



The two chips consist of the ML4661 FOIRL transceiver and the ML4621 fiber-optic quantizer. Together, the chips provide all of the functions required to implement an internal or external IEEE 802.3 FOIRL medium-attachment unit. The 4621 can be directly connected to standard Manchester encoder/decoder chips or an attachment-unit-interface cable.

The transmitter section of the ML4661 can directly drive a fiber-optic LED. Support functions, such as jabber, 1-MHz idle-signal generation, and signal-quality-error (SQE) test, are all integrated on the chip as well. Five network-status LED drivers are available to control the indicator. The receiver portion accepts an ECL input coming from the ML4621 quantizer chip. Logic removes the 1-MHz idle signal and the attachment-unit-interface output is activated when the receive squelch criteria is exceeded. A link-monitor function is also included to provide a warning signal if light levels are too low.

Both chips operate from a 5-V supply and are housed in 28-lead plastic leaded chip carriers. In 1000-unit lots, the ML4661 goes for $21 apiece, while the ML4621 sells for $6.50 each. Both are available from stock.

Micro Linear Corp., *2092 Concourse Dr., San Jose, CA 95131; Charles Yager, (408) 433-5200.*

CIRCLE 590

■ *DAVE BURSKY*

HIGH-DENSITY CAM BOOSTS LAN THROUGHPUT

The PNC1480 contents-addressable memory (CAM) is designed to eliminate throughput bottlenecks in the address-filtering operations of bridges, routers, and gateways of high-speed LANs. Configured as 1 kword by 64 bits, the memory chip uses a logic comparator within each memory-bit cell to produce a constant search time of 100 ns or less.

Individual bits and words in the PNC1480 CAM can be masked for comparison. The 64-bit field width can be partitioned as areas of CAM and RAM on 16-bit boundaries.

For use in gateways, on-chip logic on the PNC1480 CAM automatically converts data between Ethernet and token-ring formats. Cascaded devices can be addressed as one large CAM, or as specific CAMs in a chain. The 5-V CMOS device has TTL-compatible inputs and outputs, and comes in a 28-pin DIP or a 44-pin PLCC. Pricing is $70 each in quantities of 100.

GEC Plessey Semiconductors, 1500 Green Hills Rd., Scotts Valley, CA 95066; (408) 438-2900. **CIRCLE 591**

10BASE-T TRANSCEIVER CONSERVES POWER

A CMOS 10Base-T transceiver draws a typical 35 mA, compared with the 350 mA required by equivalent bipolar devices, and just 250 μA in a power-down mode. In external asynchronous media-attachment-unit (MAU) applications, the 83C94 transceiver is used on a circuit board outside the data-terminal equipment and connected through a standard Ethernet auxiliary-unit interface (AUI). AUI signals transmit and receive data, and report collisions. LED outputs on the 83C94 indicate MAU functions, such as transmit, receive, link integrity, jabber, collision, and autopolarity detection and correction. In embedded applications, the chip functions with a data-link controller as a Manchester code converter. With surface-mount packaging, Seeq's chip-set solution occupies about 3.4 in.^{2} of board space. The 83C94 is available now in a 28-pin DIP or PLCC for $9.75 each in lots of 1000.

Seeq Technology Inc., 1849 Fortune Dr., San Jose, CA 95131; (408) 432-7400. **CIRCLE 592**

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New brochure presents high-performance ceramic resistors designed to exceed performance of conventional film, composition and wire-wound resistors. Designed for higher voltages, energies or frequencies, Carborundum non-inductive bulk ceramic fixed resistors are available in three types: AS--high voltage/energy for capacitor crow bar circuits, pulse-forming networks, impulse voltage generators, snubber circuits; A--high resistance for grounding resistors, voltage dividers; SP--high-power/frequency loads for parasitic suppression, current limiting, snubber circuits.

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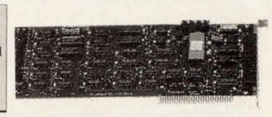

12 Bit A/D & D/A [PCL711S] $295

- **A/D converter**: 8 single-ended channels; Uses **AD574** device; Conversion time is less than **25µsec; ** Input range: ±**5V**; Software Trigger Mode only.
- **D/A converter**: 1 channel; 12 bit resolution; 0 to **+5/10V** Output Range.
- **Digital I/O**: 16 In/Out(TTLcompatible); External Wiring Terminal Board incl.
- **Utility Routines** and **Demo/Sample Programs** for **BASIC** and **Quick-BASIC**.

12 Bit A/D & D/A [PCL812] $395

- **A/D converter**: 16 single ended inputs; Uses AD574; Conversion time less than 25µsec; Built-in programmable pacer; Input Ranges: ±10V, ±5V, ±1V.
- **D/A converter**: 2 channels; 12 bit resolution; Output Range 0-5V.
- **Digital I/O**:16In/Out(TTLcompatible); **Programmable Counter/Timer** (8254).
- **DMA** and interrupt capability. Utility software and sample program in BASIC.

Fast 12 Bit A/D/A [PCL718] $785

- **A/D converter**: 16 single ended or 8 differential channels; 12 bits resolution; Programmable scan rate; Built-in Interrupt and DMA control circuitry. Conversion speed **60,000 smpls/sec** (standard), **100,000 smpls/sec** (optional).
- Input Ranges:Bipolar : ±10V, ±5V, ±2.5V, ±1V, ±0.5V; Unipolar:10,5,2,1V
- **D/A converter**: 2 channels; Resolution: **12 bits**; Settling time: **5µsec**; ±5V
- **Digital I/O**:16In/Out(TTLcompatible); **Programmable Counter/Timer** (8254).
- **Software:** Utility software for BASIC & QuickBASIC included. Supported by **LabDAS, ASSYST, LABTECH, UnkelScope.**

6 Channel 12 bit D/A [PCL726] $495

- **Output Ranges**: 0 to +5V, 0 to +10V, ±5V, ±10V, or sink 4-20mA.
- Settling time: **70µS**. Linearity: **±1/2bit.** Voltage output drive capacity: **±5mA.**
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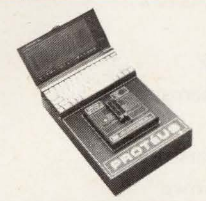

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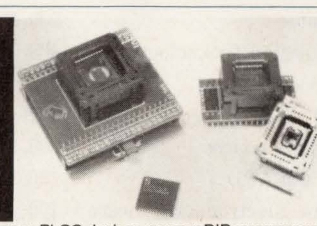

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