ELECTRONIC DESIGN

FEBRUARY 6, 1992

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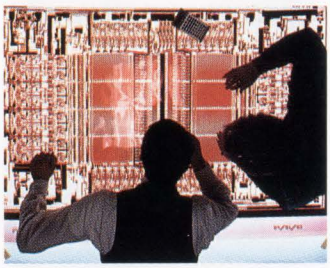

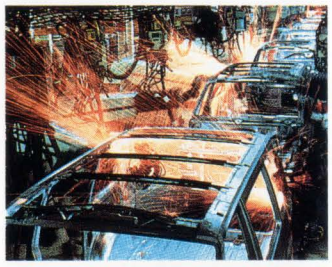

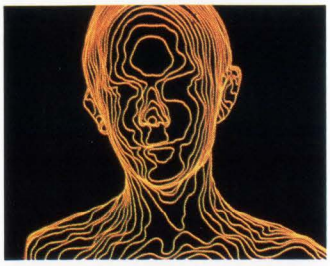

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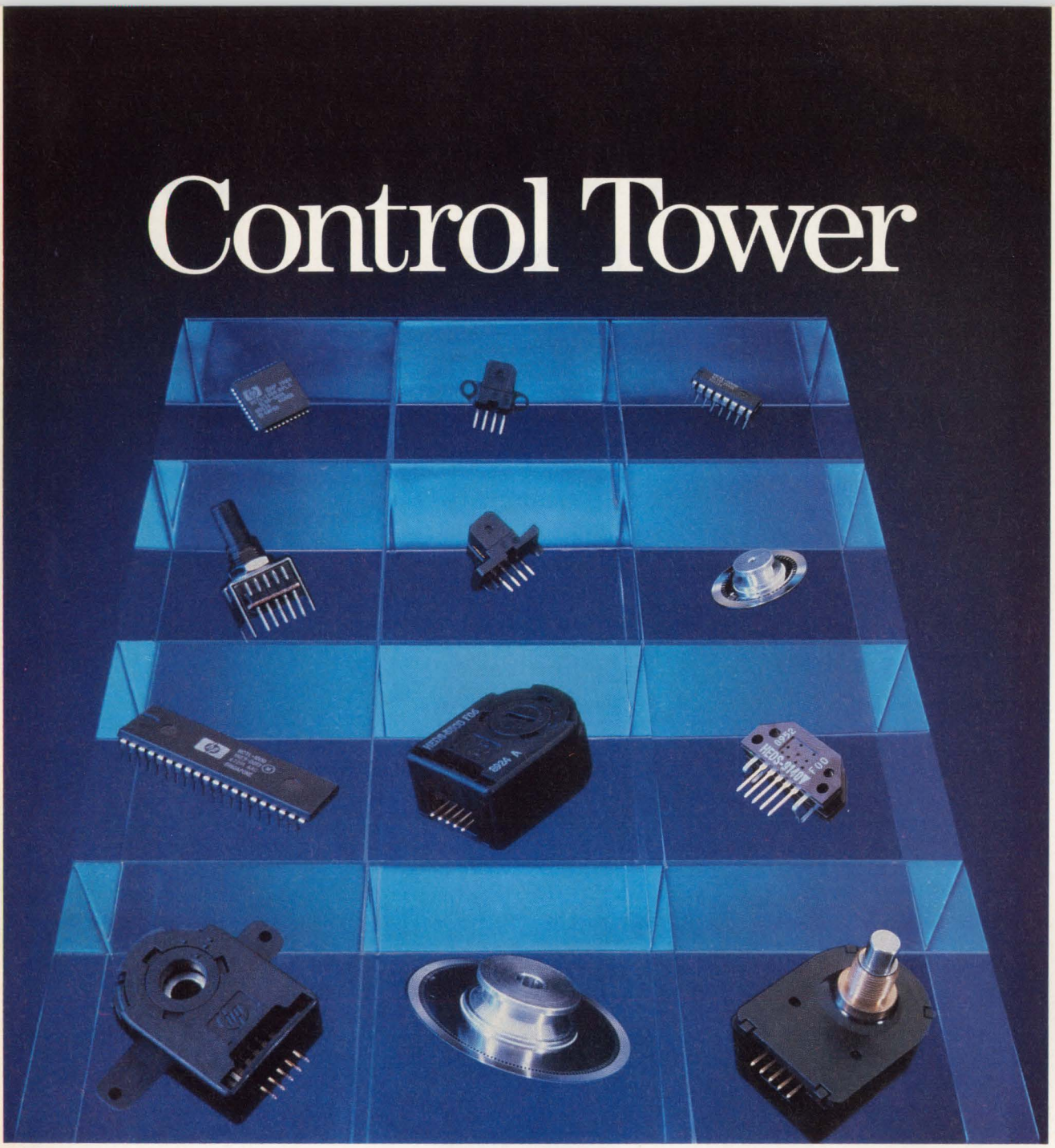

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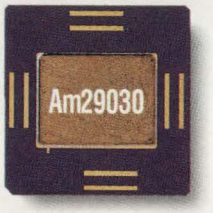

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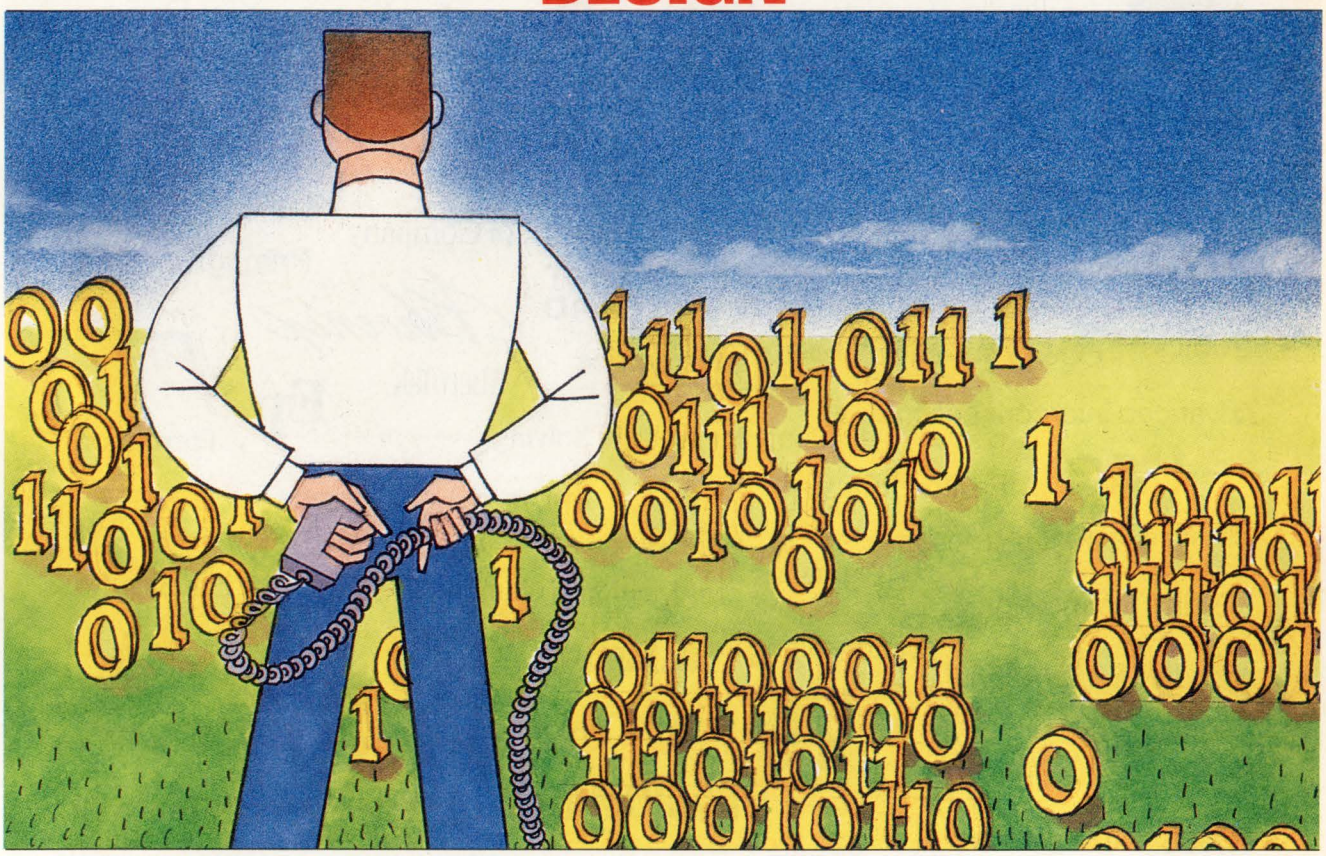

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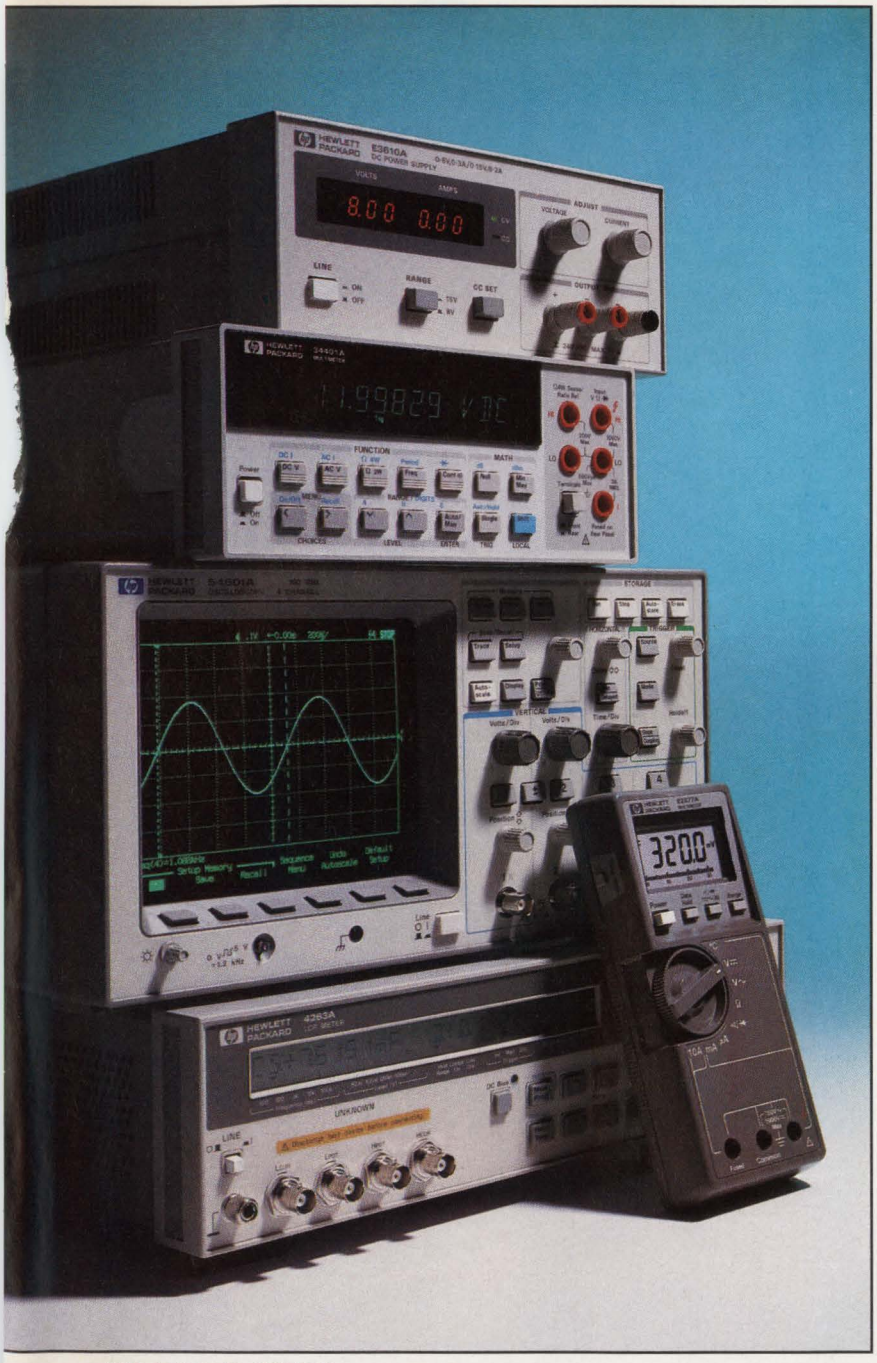

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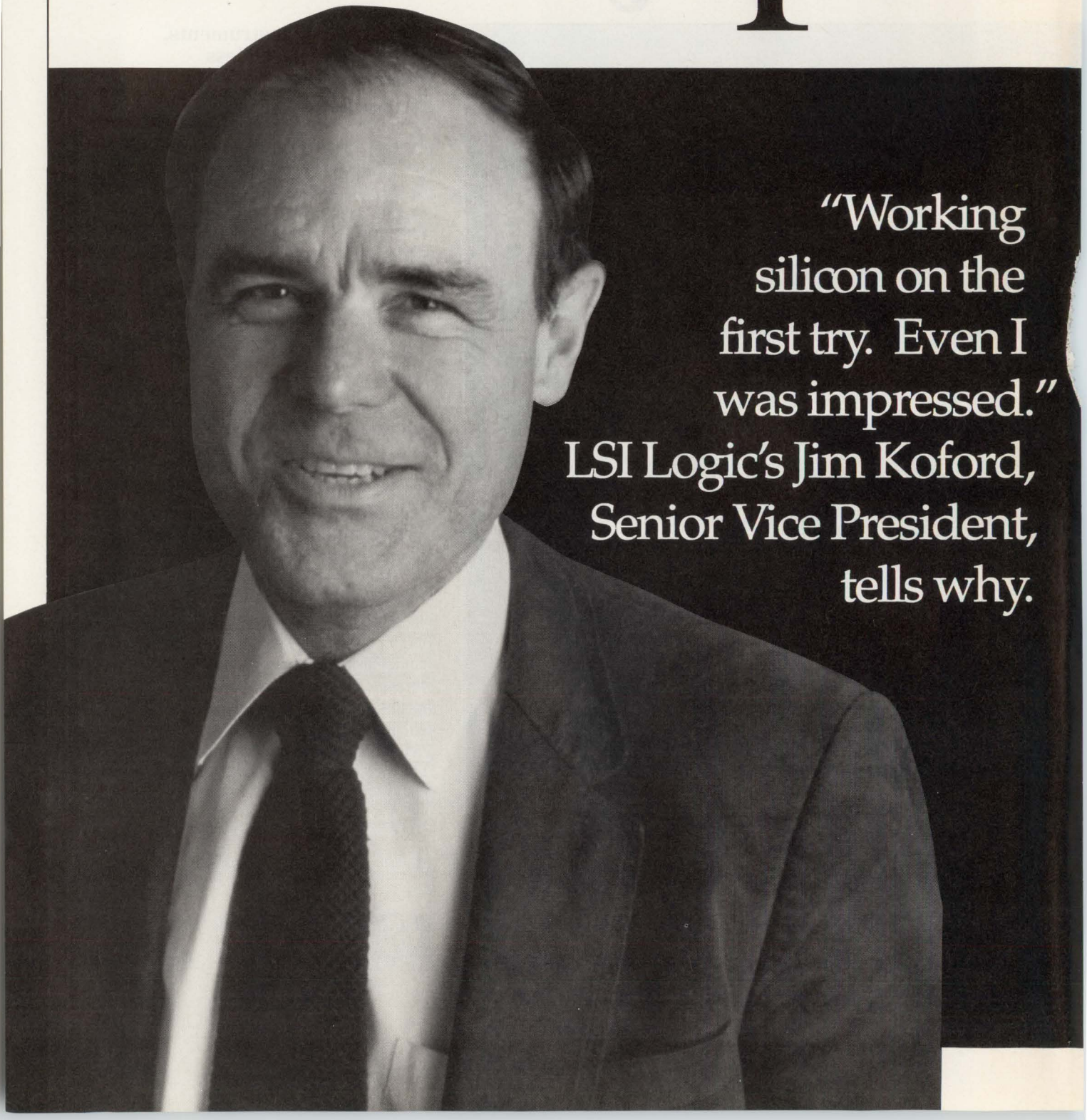

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CIRCLE 1

No Monopoly On Ingenuity

I can recall, back in the late 1960s, interviewing a Japanese engineer working at Bell Labs here in New Jersey about a gallium-arsenide Gunn-effect-based device. It generated signals whose wave shape was determined by the physical shape of the device itself – make the device as a triangle, and you got triangular waveforms. When I asked how he created the precise shapes of the tiny devices (less than 40 mils on a side), he answered "Good old Japanese ingenuity." (Actually, he created the devices with painstaking shaping on a grinding wheel.) That being the 1960s, and being steeped in tales of Yankee ingenuity, I got a chuckle out of his turn of phrase, and essentially wrote it off as just that – a clever turn of phrase. Boy, did I have a lot to learn.

Looking back on this incident, I regret not picking up on those early signs of what has become a major force in the electronics industry: Japanese ingenuity. But it was more than simple (or not-so-simple) ingenuity that accounted for the rise of Japanese products. It also was a focus on quality in mass production. Japan stepped into the U.S. semiconductor market spotlight back in the late 1970s, when a Hewlett-Packard engineer issued a report stating that Japanese-made dynamic-memory chips were of higher quality than comparable U.S.-made devices. The rest of the U.S. computer makers eventually agreed with that assessment, and now the commercial DRAM market is being driven by Japan's semiconductor industry.

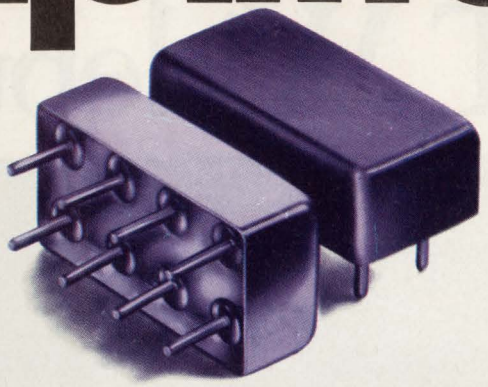
A similar trend occurred in automobiles – first, a recognition of quality by customers, and then a major sales impact in the U.S. Though Electronic Design doesn't focus on the automotive industry, I can't help commenting on the recent presidential trade mission to Japan. There's an American tradition of calling 'em like you see 'em; so, from what I see, the leaders of the big three U.S. car manufacturers have no one to blame but themselves for their present predicament. They lost a large portion of the U.S. market because they didn't respond to customer preferences for reliable, economical cars. As for exports to Japan, how could they expect to sell large numbers of traditional American left-side steering wheel cars – cars designed to drive on the right side of the road – in a country that drives on the left side of the road? Unless we're missing something, it doesn't seem to take much ingenuity to figure that one out.

What all of this shows is that neither the U.S., Japan, nor Europe can monopolize ingenuity. But it does take good, forward-looking management, beginning right at the top, to harness that ingenuity and to set up the manufacturing organization to produce quality products.

Stephen E. Scrupski

Editor-in-Chief

rugged plug-in amplifiers



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MAN-1AD	5-500	16	.05	+6	7.2	41	12/85	24.95
MAN-2AD	2-1000	9	0.4	-2	6.5	28	15/22	22.50
MAN-11AD	2-2000	8	0.5	-3.5	6.5	22	15/22	29.95

††Midband $10f_L$ to $f_{U/2}$, ±0.5dB † 1dB Gain Compression ◊Case Height 0.3 in.
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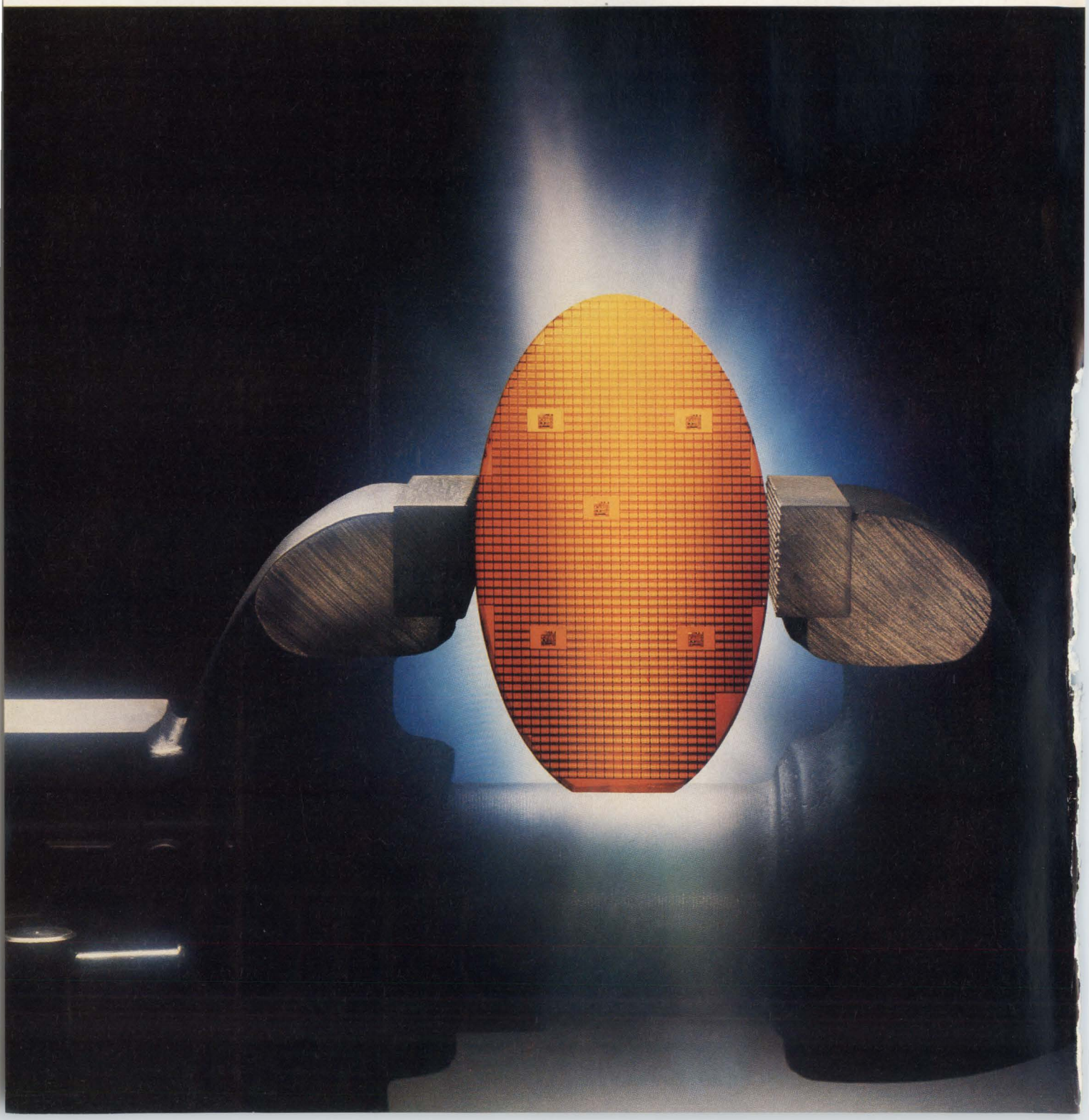

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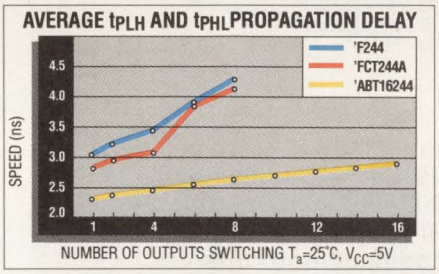

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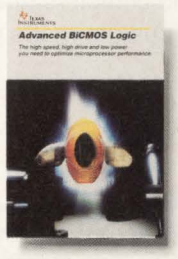

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08-1139

WILL VHDL BE A MISSED OPPORTUNITY?

LISA MALINIAK
COMPUTER-AIDED ENGINEERING

Any future prosperity in the electronic-design-automation (EDA) industry hinges on developing standards. Users need tools and data that are interchangeable. Proprietary tools don't offer any practical way to integrate systems from different suppliers, and designers can't exchange data between them in a meaningful manner. What results is redundant work, uncomparable data, uncertainties, and other headaches. VHDL, an IEEE standard since 1987, has the capability to secure the software and data interchangeability that users seek. Yet the EDA industry has hesitated in embracing VHDL, which adversely affects both vendors and users.

Industry studies and surveys continue to reveal that users want standards. For instance, an EDA survey commissioned by ELECTRONIC DESIGN each year showed that in 1990 and 1991, compatibility was the first concern of 90% of those designers questioned. In addition, almost 80% listed adherence to industry standards as their major interest when selecting design software.

When VHDL was made a standard, EDA companies responded with public support. But they pointed at the language's shortcomings and made comparisons to their own hardware description languages (HDLs). Most vendors took a wait-and-see attitude, and expended little effort to make practical and useful VHDL products.

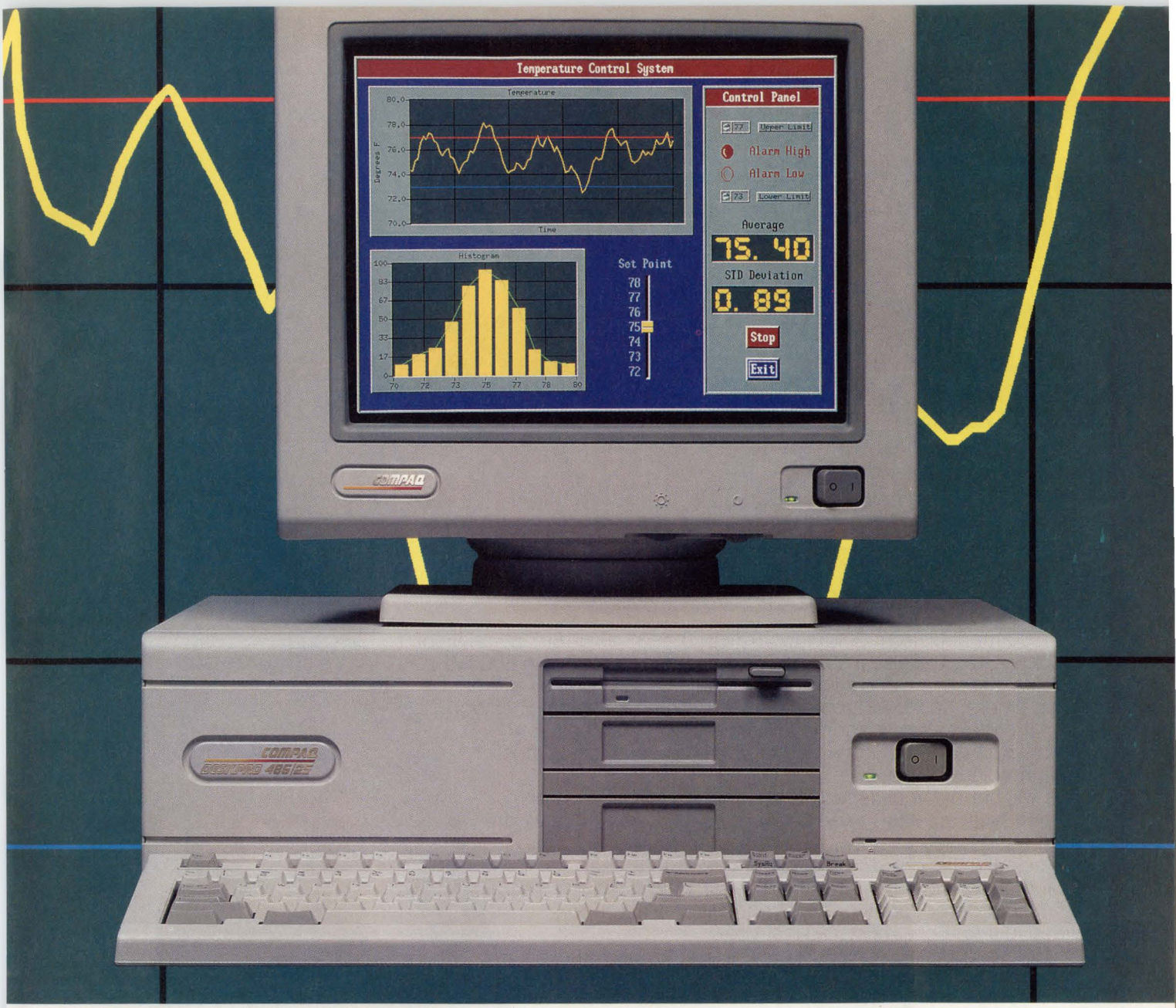
This lack of serious effort to develop tools, create innovative ways to blend VHDL with known design approaches, write utilities to convert proprietary HDL code into VHDL, and spread education has had negative repercussions on the language and the industry. Jan Geusens, vice president of Ascent Technology Inc., a San Jose, Calif.-based company involved with many popular HDLs, maintains that "the industry has done a great disservice to itself and its customers." He explains that many of today's problems with the language exist because vendors didn't quickly and totally adopt VHDL.

VHDL could have been the justification and investment motivation for a new wave of innovative EDA systems. "That opportunity has been missed, or at least the window of opportunity is closing unless the industry does something now, and fast," states Geusens."VHDL is exposed to the danger of becoming another interesting experiment."

One complication arising from the industry's hesitation is that the international competitors of the U.S. electronics industry have caught up with their rivals in VHDL support. European manufacturers, in particular, are strongly driven by standards in their product planning. The U.S. lost at least two years of their head start due to the lack of products and support. In addition, the international contribution to the standard can result in marginally compatible derivatives or "flavors" of VHDL, which in turn defeats the goal of a standard. Geusens points out that VHDL could turn into another case of the U.S. having a good concept, but other countries reaping the benefits.

To speed VHDL's acceptance, U.S. companies must develop products that are attractive because of their performance, and not just because they're based on VHDL. And vendors must offer migration paths for customers from whatever proprietary languages they're using. Isolated point tools are inadequate because engineers don't want to trash their existing designs.

In addition, VHDL will never become the industry standard if companies continue to offer VHDL-based products while promoting their own proprietary software. Although the last few years have seen EDA vendors and users push for the standard, the industry must do more to quickly and fully adopt VHDL because the lack of a standard inhibits industry growth. "Whether it's the best language or not," remarks Geusens, "VHDL is established and has the capability to unite EDA vendors and users alike."



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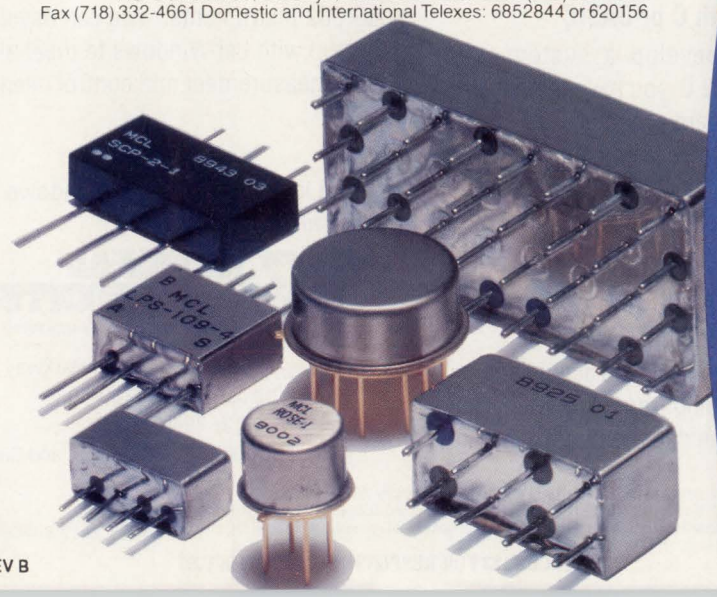

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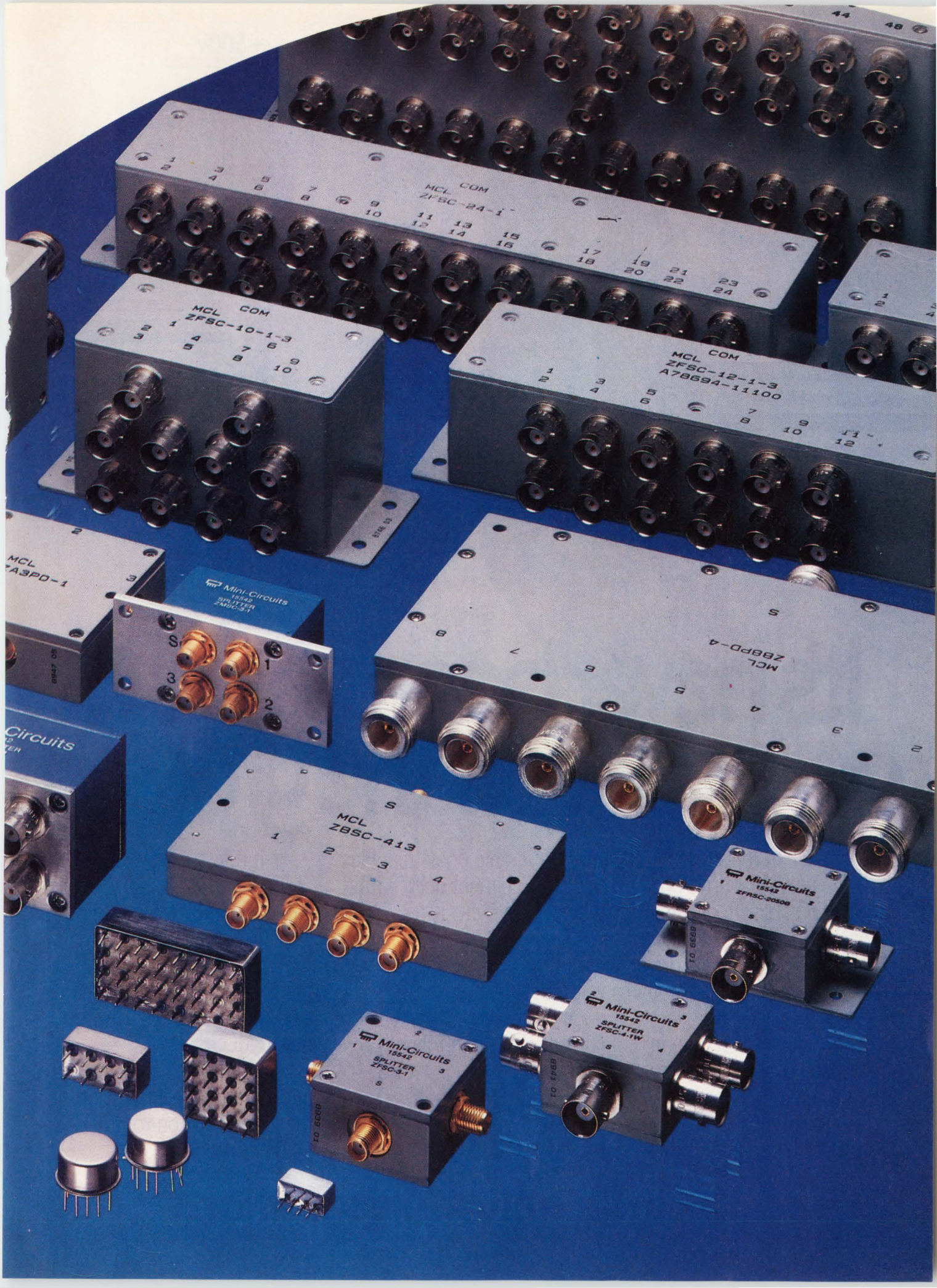
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ZA3PD-1
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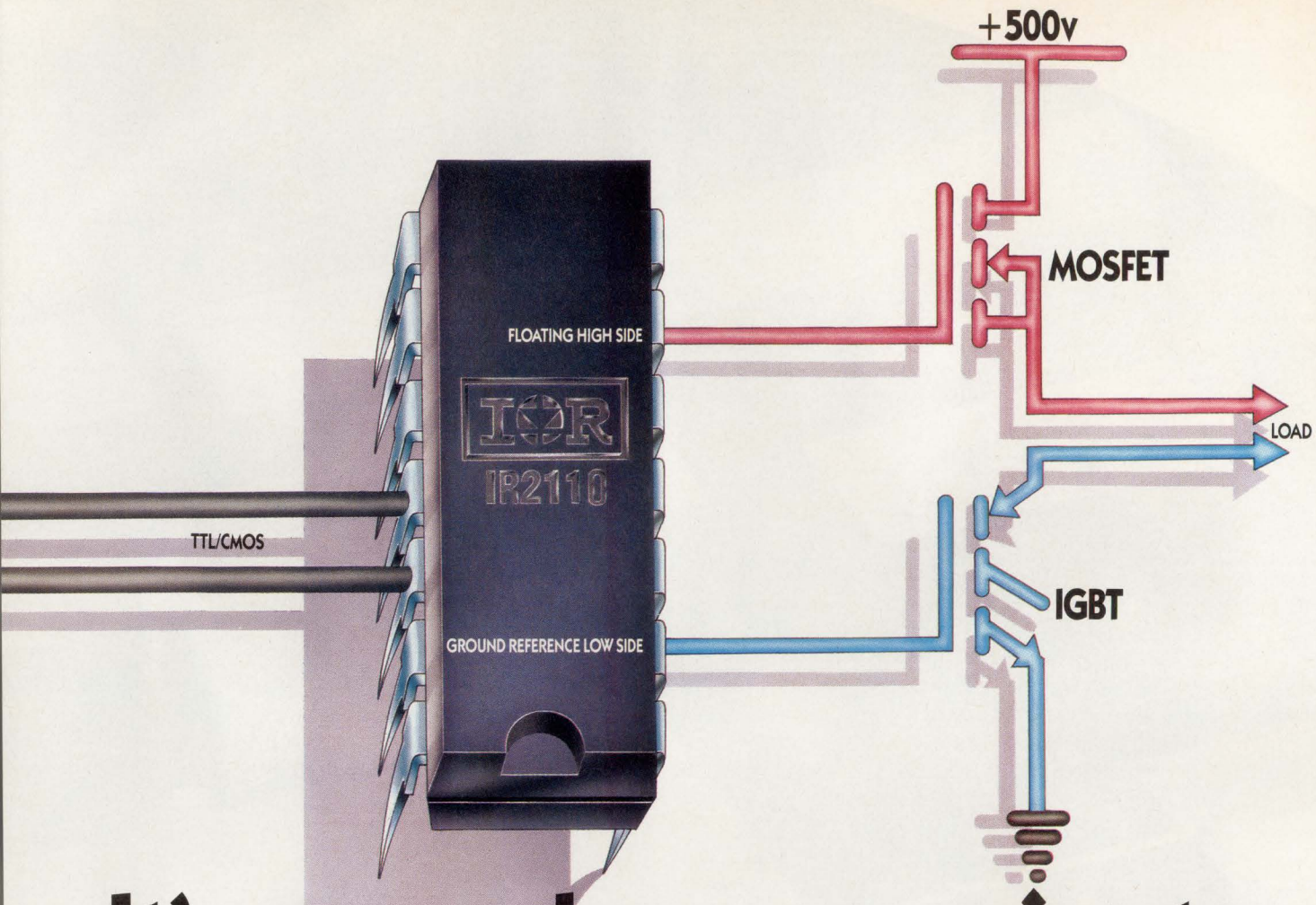

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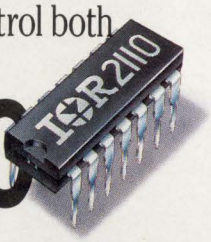

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ENHANCED ISDN MOVES TO PACIFIC BELL SWITCHES

An agreement between Pacific Bell, a subsidiary of San Francisco-based Pacific Telesis Group, and Northern Telecom Inc., headquartered in Nashville, Tenn., marks a major step toward converting Pacific Bell's telephone network to new national standards for the integrated services digital network (ISDN). Beginning in early 1993, Pacific Bell will incorporate the new standard in its DMS-100 central-office switches, which are produced by Northern Telecom. This move will eliminate the problems associated with existing ISDN standards that allow broad interpretations to lead to noncommunicating proprietary systems and equipment. The new standards will mean universal compatibility between both existing and new products and services. Over the next six years, Pacific Bell will order 112 ISDN modules containing Northern Telecom's National ISDN One-compliant hardware and software. When completed, the enhanced technology will be available to some 2.5 million customers. *ML*

PROPOSAL PUTS TINY PCS IN EMBEDDED APPLICATIONS

A proposed extension to the IEEE-P996 AT-bus specification defines the PC/104 form factor for a family of compact modules. The family offers PC compatibility in places where PC cards simply didn't fit, such as embedded environments. The 3.6-by-3.8 boards, which provide a unique self-stacking "stack-through" header, contain two bus connectors, a 64-pin P1 type and a 40-pin P2 type. With the proposal, designers can build lower-cost and reduced-power systems by eliminating backplanes and card cages. A typical power consumption of about 1 or 2 W will result from the 6-mA bus-drive requirement. The PC/104 specification is based on Ampro Computers' MiniModule form factor, originally designed as a daughterboard expansion module for the company's Little Board family of single-board computers. The twelve-member PC/104 Consortium includes Ampro Computers, Automation Instruments, BG Technologies, Diamond Systems, DMS Systems, Enclosure Technologies, IOTech, Quantum Software Systems, Real Time Devices, Reflection Technology, Voice Connexion, and Xecom. For more information, call Rick Lehrbaum, Consortium Chairman, at (408) 245-9348. *RN*

FAST-ACCESSING DRIVE HOLDS 1.24 GBYTES

Through a combination of a low-mass actuator, a high rotational speed (6300 rpm), and a novel digital-hybrid servo mechanism, a 3.5-in. full-height disk drive achieves the industry's shortest average access time of just 8.5 ms. The digital-hybrid servo lets designers increase the number of tracks per inch, enabling the drive to pack the highest level of formatted storage for a 3.5-in. unit—1.24 Gbytes. With the disk's high rotational speed, data can transfer between the disk and the read/write heads at 44 Mbits/s. Moreover, the high speed keeps the rotational latency to just 4.76 ms, also one of the shortest times in the industry. Designers at Maxtor Corp., San Jose, Calif., have also applied a higher level of silicon integration to the drive's internal controller than seen in previous Maxtor storage products. An internal 256-kbyte cache provides a buffer between the read channel and the 10-Mbyte/s SCSI-2 byte-wide system interface. The cache can be split into multiple segments and can implement a read-ahead algorithm to maximize performance, especially when the SCSI tag-queuing commands are employed. Furthermore, through the drive's internal firmware, the cache can be tuned to optimize its use in various applications. Samples of the drive sell for $1795 and are available immediately. *DB*

PROGRAMMABLE FILTER NEEDS NO MULTIPLIERS

An innovative approach to digital filtering lets a single-chip filter provide full programmability of its pulse response without the need for a chain of on-chip expensive, high-speed multipliers. Developed by SGS-Thomson Microelectronics in Milan and Paris, the MH27HC68 operates at up to 40 MHz, suiting it for HDTV, video conferencing, and other applications requiring real-time video signal filtering. The chip addresses video-filtering applications that require only static programming of the filter response. Because filter coefficients are never reprogrammed during operation, the product of the filter coefficient and a given input signal magnitude will always have the same value. By storing this value as a precomputed entry in a lookup table, the M27HC68 eliminates the continuous recalculating of the input-sample and filter-coefficient products. The filter function is implemented as a transposed configuration, with the input sample being applied to 16 EPROM 256-word lookup tables simultaneously. The table outputs, which are the precomputed products of the input sample and the filter coefficients, are transferred in parallel to the arithmetic unit that contains a chain of 32 22-bit adders and 62 22-bit-wide registers. The M27HC68 is built with a 1.2-μm CMOS process. Custom versions may be developed or integrated into ASICs to meet particular requirements. *JG*

SIMULATION MODEL BACKS 68302 PROCESSOR

The 68302 multiprotocol communications processor from Motorola Inc., Austin, Texas, is now supported by the 302 SmartModel behavioral-level simulation package developed by Motorola and Logic Automation Inc., Beaverton, Ore. The simulation model enables hardware designers to develop, debug, and optimize the hardware operation of 302-based board- and system-level designs for a shorter time-to-market. Advanced modeling features include timing checks that look for undefined interrupts, uninitialized registers, illegal conditions, and timing violations. VHDL interoperability allows designers to mix models from multiple sources. The 302 SmartModel is available for a one-time $4000 licensing fee paid to Motorola. Also required is a SmartModel Library license purchased separately from Logic Automation. For more information, contact Trey Oprendek at Motorola at (512) 891-3434, or Diane Landers at Logic Automation at (503) 690-6900. *ML*

PC MOTHERBOARD LOGIC IC TRIMS POWER DRAIN

Although single-chip PC motherboard logic implementations for 80386SX systems have already been done, most are targeted at desktop systems. And they don't include any power-saving features. A forthcoming logic chip, which operates from as low as 2.7 V and offers four slow-clock options as well as a sleep mode, can considerably reduce average system power consumption. This is especially so when coupled with the AM386SXLV version of the 80386 from Advanced Micro Devices Inc., Austin, Texas. The HT22LV motherboard logic chip from Headland Technology Inc., Fremont, Calif., operates at system clock frequencies of up to 20 MHz and permits systems to select a clock division ratio of 2, 4, 8, or 16 to conserve power during operation (many applications, such as word processing or modem control, don't require that the processor run at maximum speed). The sleep mode allows the system to mostly power-down during long periods when the keys aren't depressed, afeature that resembles a bookmark. With the chip's "bookmark" operation, users can stop what they're doing and then re-open the system to where they left off. Housed in a 208-lead package, the logic chip supports 8- or 16-bit system BIOS and 4 Mbytes of DRAM. It sells for $30 each in lots of 1000. Contact Ken Plewa, (510) 623-7857. *DB*

FAST RISC PROCESSOR FITS CAR CONTROLS

With the development of a car signal processor (CSP), a universal signal processor can now execute and monitor a wide range of real-time in-car control applications. Examples of such tasks include anti-blocking, active shock absorption, wheel-slip control, and fuel injection. The heart of the CSP, developed by the ITT Semiconductors Group in Freiburg, Germany, is an 80-MIPS microcontroller using a RISC architecture and operating with an effective computing power of 32 MIPS. It's surrounded by a standard periphery optimized to meet automotive requirements. The CSP handles twenty-four 10-bit analog inputs and has eight 16-bit outputs that can be flexibly adapted to the desired control task via software. The 1.2-μm CMOS IC is supplied in a 68-pin PLCC package and is available as engineering samples. *JG*

MPU-ASIC COMBO EASES LASER-PRINTER DESIGN

Through an agreement with Advanced Micro Devices, Sunnyvale, Calif., Destiny Technology Corp. can port their line of printer-controller ASICs to AMD's Am29200 microcontroller. Destiny, located in Milpitas, Calif., announced its edge-enhancement technology (EET) and raster-image-device-accelerator (RIDA) controller ASICs last year. "This is a further customization of an embedded MPU for the laser-printer market. And it's an additional integration step beyond what Intel has done with their 82961KA," claims David Larrimore, vice president of marketing for Destiny. Instead of using a processor chip, an interface part, and a printer controller, the AMD-Destiny solution requires just the Am29200 and the Destiny ASIC. Designers will get similar results from using a two-chip solution, the i960 plus the 82961KA, or a one-chip solution, AMD's Am29200.

This solution follows a trend toward distributed processing, which is to incorporate as much of the common core functionality as possible on to the system board or the MPU. More detailed functions, which requires a specialized piece of hardware or firmware like EET or RIDA, can then fit onto the system board more easily. As distributed processing becomes more of a factor in printer controllers, the software that drives the hardware and even the hardware itself becomes more tightly integrated. The combination of reduced board space and the price-performance level of the Am29200 suit it for next-generation laser printers. *RN*

THREE *of a* KIND

A Winning Hand of Power Amplifiers

PA04

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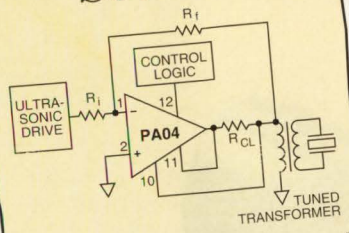
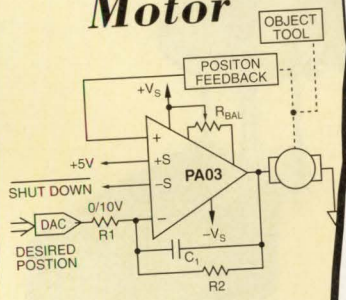


The combination of voltage rating of up to 200V, current up to 20A, and a power bandwidth of 90KHz makes PA04 ideal for sonar transducer drive. Resonant output circuits improve efficiency and power output. 100+ pricing is $168.00.

PA03

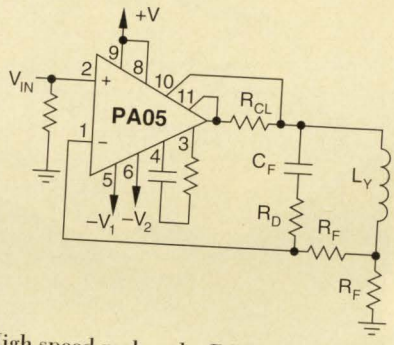
Motor



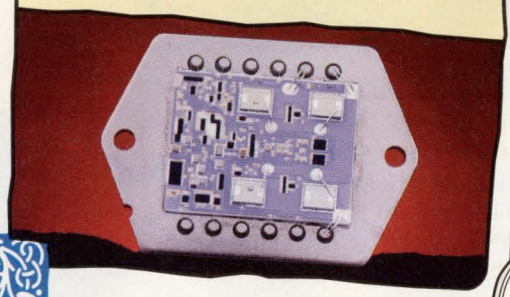
Super power describes the PA03. With 500W of internal power dissipation, a 150V supply and ±30A of output current, the PA03 is a complete high power motor drive solution. 100+ pricing is $320.00.

PA05

Deflection



High speed makes the PA05 operational amplifier **the** choice for deflection applications. Combining a 100V/µs slew rate with a 100V supply, ±30A output current, thermal protection, and a 360kHz power bandwidth, makes the PA05 a cost effective solution. 100+ pricing is $189.00.



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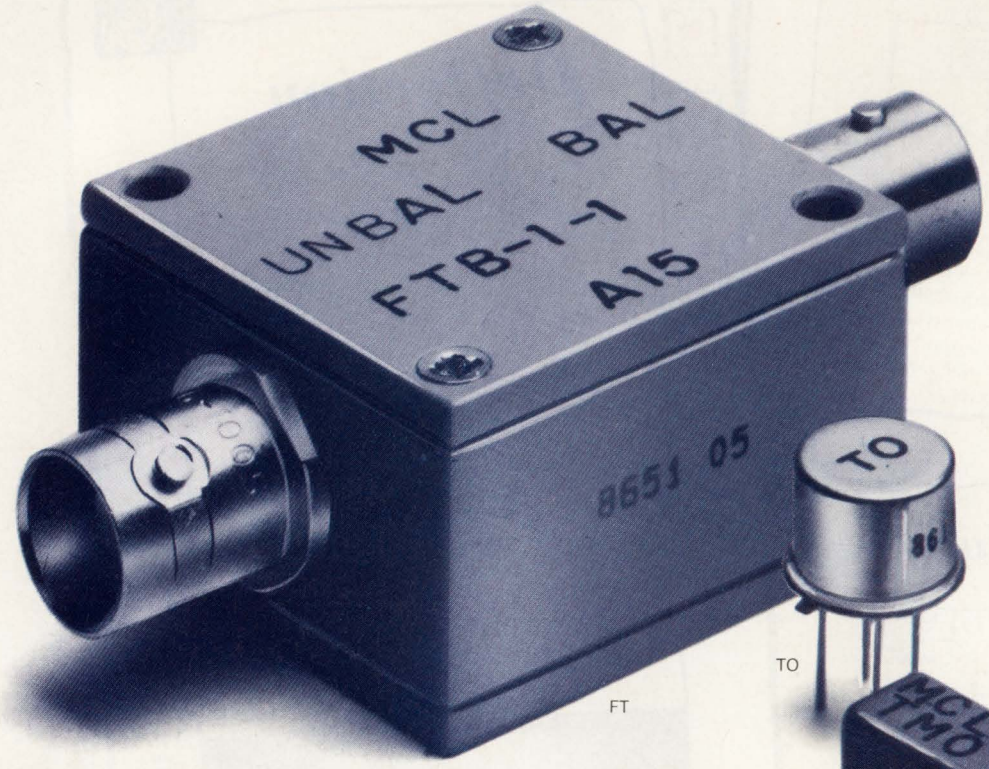

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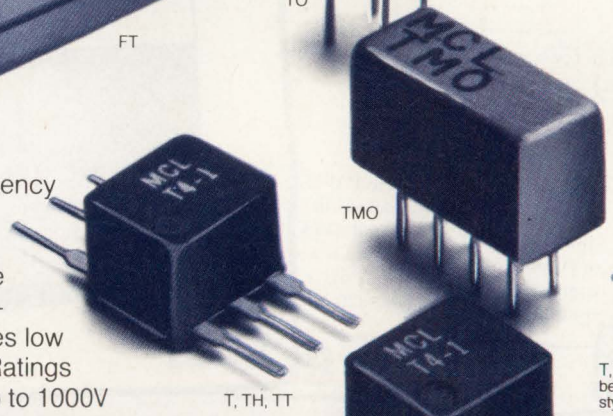
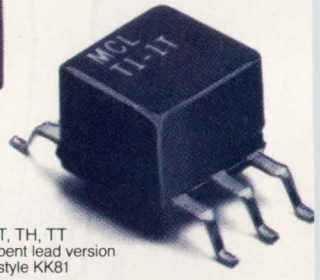
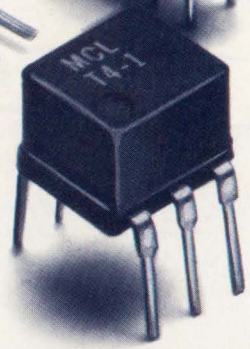


TMO

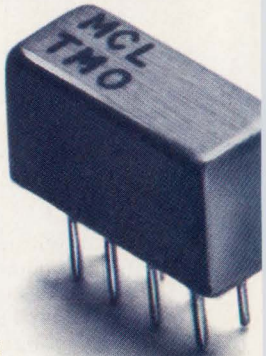
T, TH, TT



T, TH, TT
bent lead version
style KK81



T, TH, TT
bent lead version
style X 65



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FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
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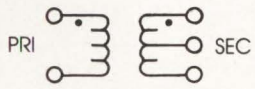
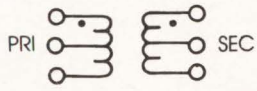
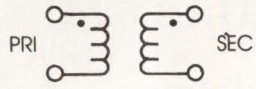
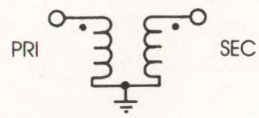
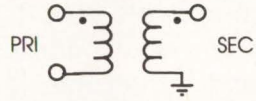
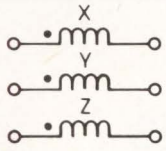
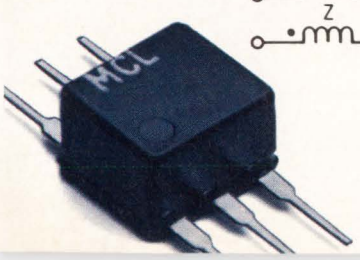
case style number see opposite page		MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	INSERTION LOSS 2dB MHz	INSERTION LOSS 1dB MHz	PRICE $ Qty. (1-9)
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
		T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	.2-350	.2-350	.35-300	2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
		T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
	TMO	TMO1-1T	1	05-200	.05-200	.08-150	.2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	8.45
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
		TT1.5-1	1.5	.075-500	.075-500	.2-100	1-50	5.95
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
	TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
		T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65
		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
		T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
		T36-1	36	.03-20	.03-20	.05-10	.1-5	6.95
	TO	TO-75	1	10-500	—	10-500	40-250	6.95
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
		T9-1H	9	2-90	2-90	3-75	6-50	6.45
		T16-H	16	7-85	7-85	10-65	15-40	6.45
	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
		TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-8	8.45
		†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
		†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
		TMO16-1	16	.3-120	.3-120	.7-80	5-20	7.95
D 	T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
		T3-1	3	.5-800	.5-800	2-400	—	4.45
		T4-2	4	.2-600	.2-600	.5-500	2-250	3.95
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
	TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
		TMO3-1	3	.5-800	.5-800	2-400	—	8.45
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95
E 	FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
		■FTB-1-75	1	.5-500	.5-500	5-300	10-100	36.95
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95



■ Denotes 75 ohm models

* FOR A AND B CONFIGURATIONS

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0.5 dB over entire frequency range

Maximum Phase Unbalance
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5.0° over entire frequency range

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CIRCLE 117 FOR RESPONSE OUTSIDE THE U.S.

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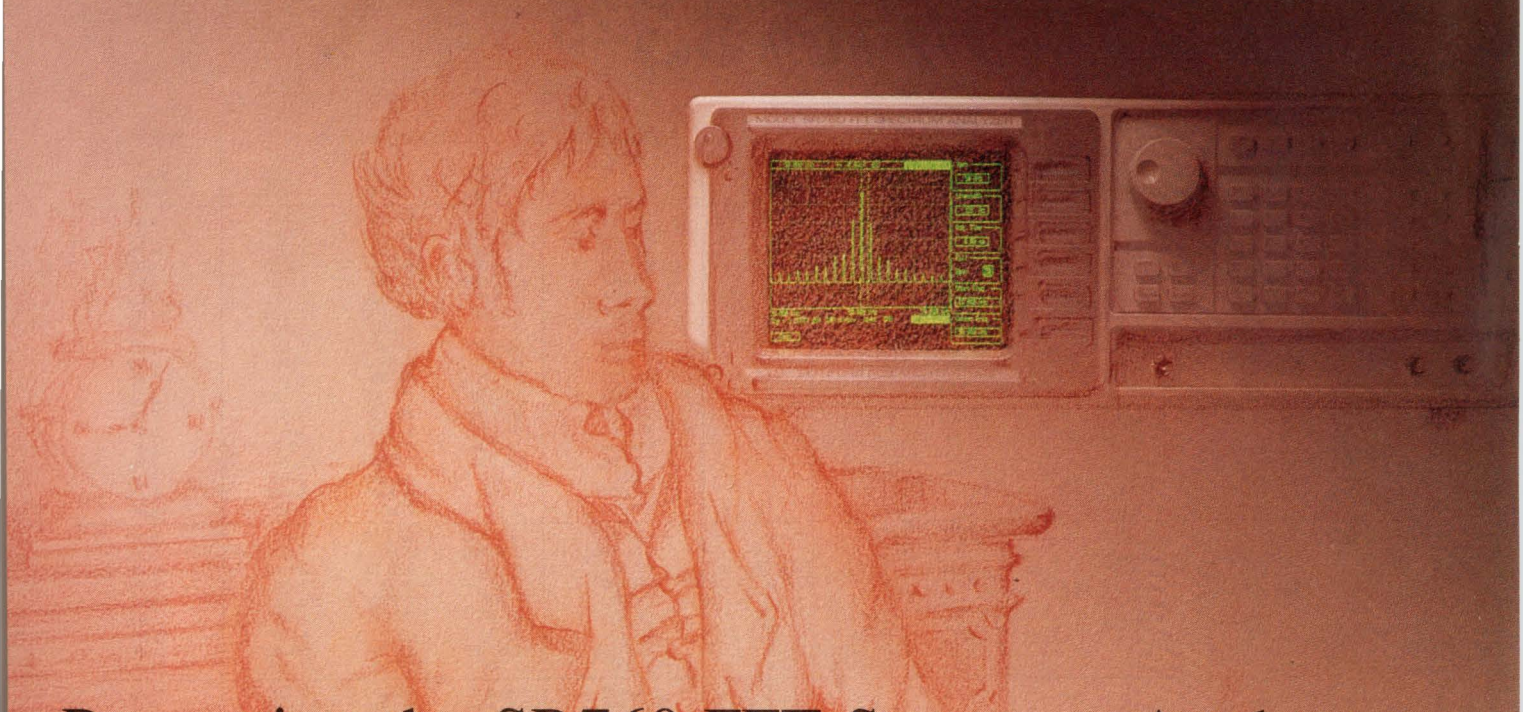

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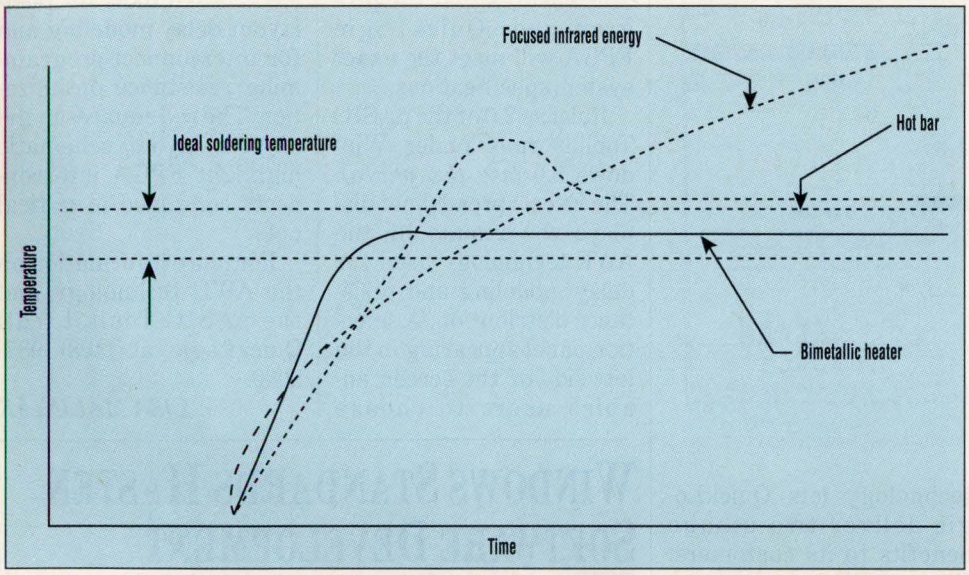


SOLDERING-TECHNOLOGY GAINS IMPROVE CABLE ASSEMBLIES

The integrity of high-speed signals traveling from board to board depends on many variables, a significant one being the quality of solder joints in the cable assemblies linking those boards. A new soldering process for automatic cable-assembly terminations is expected to significantly advance solder-joint quality toward six-sigma levels.

Scientists at AMP Inc., Harrisburg, Pa., have devised a soldering technology that relies on a combination of electrical and metallurgical phenomena to maintain temperatures across the heater strip within a narrow range, independent of thermal load and application time. Because the strip can't overheat or underheat, the result is uniformly high-quality solder joints.

In conventional hot-bar soldering of cable assemblies, a heater bar typically comes in contact with a linear array of stripped wires. Direct current heats the bar enough to melt the solder and form joints. The heater then shuts off to let the solder set before the assembly moves to the next manufacturing stage.

The temperature-time curve for each joint depends on such variables as the physical contact of the hot bar with the wire, the heating current, and ambient conditions. Overheating can damage connector parts while underheating causes poor solder joints.

The process takes advantage of a magnetic material's change in permeability as temperature increases. The heater strip consists of a bimetallic strip of a magnetic material over a nonmagnetic material. The magnetic material has a Curie temperature somewhat higher than the solder's melting point. Power comes from an RF constant-current source, which allows the skin effect to be exploited in order to control the heater strip's temperature.

Direct currents flow throughout the entire cross section of a conductor, but high-frequency currents flow only in a narrow band near the conductor's surface. As frequency increases, the current becomes confined to an increasingly narrow band. The depth of the band is referred to as the "skin depth." For a magnetic material, the skin depth depends directly on the electrical resistivity and inversely on the frequency of the current source and the magnetic permeability.

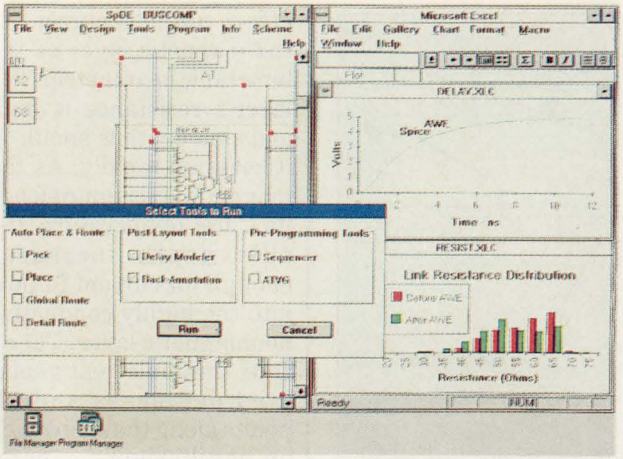
With power on, the skin effect confines current to the magnetic layer of the bimetallic heater strip. The layer's resistance is high and skin depth is small, so it heats up rapidly. As the magnetic layer approaches its Curie temperature, the skin depth increases enough for current to flow into the highly conductive nonmagnetic layer. Therefore, the Joule heat generated decreases and all points along the strip reach an equilibrium temperature—the Curie temperature of the magnetic layer. The current shifts from layer to layer as thermal loads change, maintaining this temperature independently at every point along the heater's length.

The maximum temperature of the strip, then, is fixed by the Curie temperature of the magnetic layer. That value is determined by the composition of the magnetic material. The result is a temperature-time curve that compares favorably with that of hot-bar and focused-infrared soldering *(see the figure)*. AMP plans to expand the use of the technique to other connector lines to take advantage of its improved consistency.

DAVID MALINIAK

WAVEFORM ANALYSIS YIELDS ACCURATE FPGA TIMING

Accurate characterization of interconnect resistance and capacitance effects become critical as field-programmable-gate-array (FPGA) speeds approach 100 MHz. At that speed, the analog details of the digital-signal waveforms become an issue, and signal characterization must be done in terms of waveform calculations as opposed to the more traditional delay calculations. That's because delay RC tree models can describe FPGA circuit interconnects to only a first-order approximation. However, a new technique called As-



ymptotic Waveform Evaluation (AWE) describes FPGA circuit interconnects to an nth-order approximation. As a result, simulations of the same run time as previous techniques produce far more accurate results.

The AWE technique was developed by Professors Lawrence T. Pillage of the University of Texas at Austin and Ronald R. Rohrer of Carnegie-Mellon University, Pittsburgh, Pa. It uses moment-matching approximations to efficiently evaluate the delays caused by distributed resistance and capacitance. For large interconnects, the AWE technique yields results that are as accurate as Spice simulations, while reducing simulation computing time by orders of magnitude. AWE employs frequency-domain techniques to successively converge on the actual waveform, similar to the Spice time-domain analysis that serially evaluates the waveform in small increments of time.

QuickLogic Corp., Santa Clara, Calif., is the first company to apply AWE analysis in a commercial product—the pASIC Toolkit Release 2.0. The AWE technology lets QuickLogic deliver two unique benefits to its customers. First, AWE can increase overall FPGA speed by optimizing the programming sequence of the interconnects. To accomplish this, AWE first identifies the most heavily loaded nets in an FPGA design. Then the device interconnects that make up these nets are identified and targeted for programming in a specific sequence that provides the lowest possible resistance values. Thus, the highest possible operating frequency is obtained. Maximum performance is available when these links are programmed in the range of 30 to 50 Ω. Most users will see a 20-25% FPGA speed increase with AWE technology.

A second customer benefit from AWE technology is the precision of the timing simulations. The AWE technique is used in the pASIC Toolkit to provide the most accurate timing models possible for the back-annotation of delay information into the timing simulator. The accurate timing models allow users to establish the precise system-level performance available from the FPGA. This ensures that the programmed QuickLogic FPGA will meet the exact system specifications.

Release 2.0 of the pASIC Toolkit runs under Windows 3.0 *(see the photo)*. The Excel spreadsheet displays the results of the AWE technology used for delay modeling and resistance distribution. A selection panel appearing in the left side of the screen enables users to choose AWE-based tools for post-layout delay modeling and for interconnect-programming resistance optimization. The red squares in the physical-layout schematic highlight FPGA interconnects contained in critical nets.

For more information on the AWE technology and the pASIC Toolkit, call QuickLogic at (408) 987-2000.

LISA MALINIAK

WINDOWS STANDARDS HASTEN SOFTWARE DEVELOPMENT

The role of software in image processing and data acquisition continues to grow as developers migrate toward Microsoft Windows 3.0 for their development environment. Now software development and operation using Windows has taken another step forward with the creation of DT-Open Layers, an open software architecture devised by Data Translation, Marlboro, Mass., that simplifies software development. Open Layers, which is offered free of charge to the public, consists of integrated, modular programming interface specifications. The company also offers a series of applications that conform to Open Layers called Global Lab. The applications include data acquisition, image processing, function libraries, and device interfaces.

The architecture removes the software's hardware dependence. By supporting one Open Layers-compliant board, it allows other boards to be added in the future, almost transparently. This is achieved by taking advantage of Windows' dynamic link libraries.

Open Layers speeds software development: The company defined all of the interfaces between application function libraries and their respective device interfaces. By coding any one of those layers, a new application could easily be integrated with existing code and conform to the standard. In addition, such tools as interpreted-C scripting at the application layer are provided so that designers can prototype their applications before using the libraries.

Within the applications programming interface (API), which is the interface between the applications and the function libraries, the function calls are defined. Function calls assist in board configuration, such as setting up the acquisition speed or number of channels for a data-acquisition board. For an image-processing board, things to configure include the type of input signal and display type.

Open Layers defines function calls for such operations as acquiring, dis-

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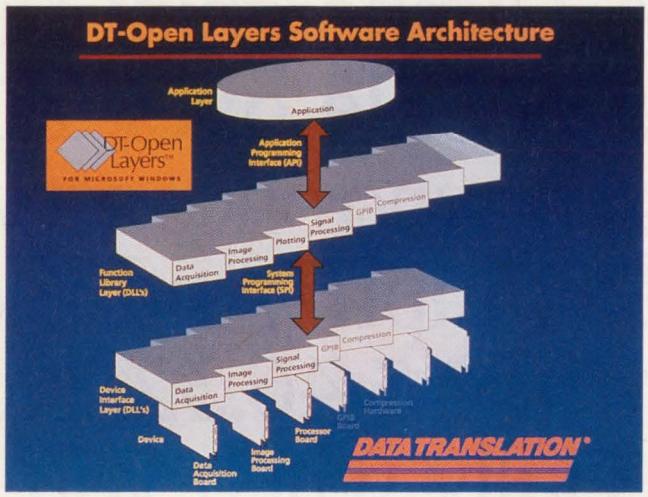
playing, or storing data, and for protocols of buffer management and data locations. For example, if data is acquired using a data-acquisition board and a fast Fourier transform (FFT) is to be performed with a processor board, the processor board can find the data by invoking the buffer-management function once the data-acquisition board acquires and stores the data. Similarly, with an image-processing board, the data is acquired and stored in memory using the Open Layers protocols. A compression board then can access the data.

The System Programming Interface (SPI) defines the device interfaces as well as the interface between function libraries,



which are hardware independent. It contains the protocols for allocating devices in terms of whether the device is being used by a particular library or application. For example, if an FFT board is being implemented, it allocates the processor board to the appropriate library to perform the FFT. After completion, the processor board is released for use by another application.

The SPI also allocates the memory assignments for all devices. Then the board configuration and other functions are performed by the device control (this is automated by Open Layers).

Open Layers consists of three levels—the application layer, the function-library layer, and the device-interface layer. Data-acquisition and image-processing libraries are supplied at the function-library layer. Plotting and signal-processing libraries will be offered in the future. In addition, GPIB and compression libraries are available from third parties. Data Translation will provide the device interfaces for the company's boards as well as the function libraries. Third parties

could design signal-processing-device interfaces that would operate directly with Data Translation's signal-processing function library.

Windows introduces a method of modularization, one that's standardized when Open Layers is used. Windows essentially acts as a traffic cop, controlling all communications between the application, the function library, and the drivers. The operating system allows for and encourages the invocation of dynamic linking, which makes it easy to add new applications, function libraries, and drivers almost at will. And existing software needn't be recompiled and relinked to be joined with new software: Windows provides the linking mechanism between each of those. For example, new hardware could be added to a system by simply loading the new driver interface.

Seeing Windows' modularization methods, Data Translation realized that the dynamic-linking capability would be a key element if Windows is to be used effectively. The standard was thus adopted so that designers don't have to be concerned with those interfaces. And because future software and hardware will fit into the same structure with very little, if any, change, simple software upgrades can be made.

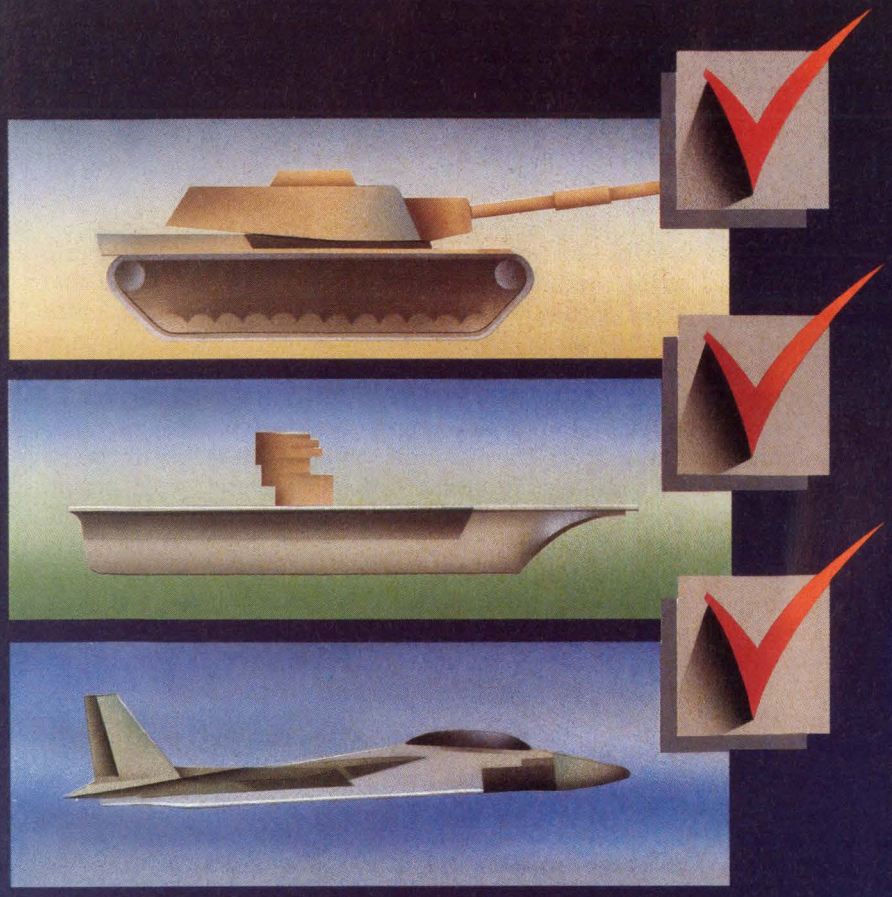
The company is targeting three classes of customers—end users, developers, and OEMs. Each class of users interacts with the various layers and interfaces of Open Layers in a different way. End users wanted applications optimized for themselves, which allowed future hardware additions without requiring changes to their application. It's not important how it gets implemented, just as long as they can add hardware later.

Developers want to be able to customize their applications with the knowledge that those applications will work with the function libraries, SPI, and drivers supplied by the hardware manufacturers. Using Open Layers, they set a software standard to ensure that their applications can simply plug into the function libraries and hardware support, and that they have full compatibility.

OEMs have needs at all three levels. At the application level, they want to do quick prototyping. Scripting capabilities were included to permit relatively fast prototype development of application software, so that a "test run" could be performed before production starts. The API's specifications allow the OEMs to do a test run, and encourages them to interface with the function libraries.

For more information on DT-Open Layers, call Data Translation at (508) 481-3700.

RICHARD NASS



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BUSCON '92 WEST: MEZZANINE BUSES RIDE A NEW WAVE OF POPULARITY

LESS-STRICT SPECIFICATIONS PERMIT MEZZANINE MODULES TO ADD FUNCTIONALITY WITHOUT THE TRADITIONAL TRADE-OFFS.

RICHARD NASS

When the doors swing open at the Long Beach Convention Center in California for this year's Buscon '92 West show, being held Feb. 4-6, attendees will encounter a technical program and exhibits with a wide range of computer-technology subjects. One particular topic that's sure to pique interest is the use of mezzanine buses, an approach that adds flexibility and allows customization of computer boards.

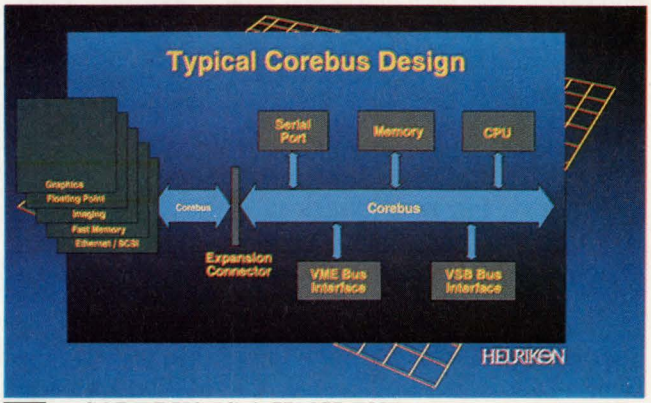
Computer-board makers always seek out ways to differentiate their boards from the competition. One approach is to incorporate a mezzanine bus that can accommodate different daughterboard modules for almost any application. The performance trade-offs are minimal and there's a significant cost savings over designing full-size boards.

Users continually demand more performance, functionality, and customization on their boards, thus putting manufacturers at a disadvantage. A board customized for one user may not suit another, or it may have more functionality than is required, raising the cost. Mezzanine boards can solve this problem: By adding a mezzanine board to a general-purpose CPU board or a single-board computer, users can get the customization they desire, without the overkill.

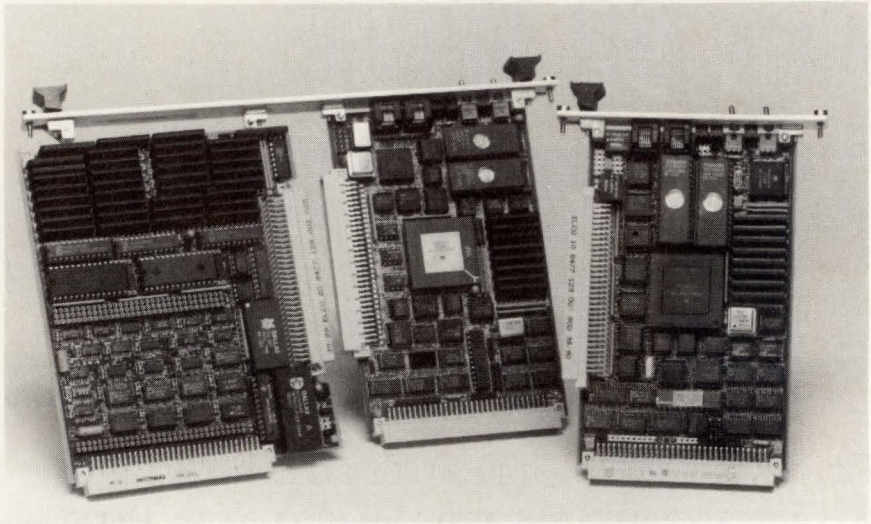
Mezzanine boards perform many functions. They offer a finer grade of modularity when building a system in terms of memory, I/O, etc. They can also be a mechanism to implement custom interfaces rapidly and inexpensively. The modules have adapted long-standing architectures, such as VME, STD, and Multibus I and II, to new applications. They offer an easy integration path for multiprocessing on a standard bus without paying the typical performance and cost penalties associated with the standard buses.

Boards for almost all standard buses are now being built with some type of expansion capability. Some of the functions supplied by mezzanine boards include serial and parallel I/O, memory expansion, SCSI ports, networking, video controllers, and communications. In addition, customized modules can be built for unique functions.

The CPU board is typically used as the baseboard, and the mezzanine boards help to evolve the platform. Board makers discovered that CPU technology is progressing at a much faster pace than I/O technology. Therefore, users can keep their I/O functionality and just upgrade the CPU. From the users' point of view, they can buy base platforms and then add whatever modularity is



1. COREBUS IS A HIGH-END synchronous mezzanine bus from Heurikon that features a 50-MHz clock speed and a maximum bandwidth of 200 Mbytes/s. The bus can handle graphics, networking, and floating-point operations. It also supports four interrupt lines, each with a separate Acknowledge signal.



2. WITH THE 3U CARDS' MXBUS CONNECTOR mounted on the side, two cards can be joined together to fit into a 6U slot. The proprietary structure from Mizar contains a family of modules ranging from simple I/O ports to complex parallel-processor expansion modules.

needed to support those baseboards, whether it's I/O, memory, disk storage, or communications.

Another advantage to using mezzanine boards is that an extra slot isn't taken up because they become part of the baseboard. And the end-users win because they can buy a low-cost mezzanine board for a fraction of what a full-sized board containing the same functionality would sell for.

Low, Mid, And High

Mezzanine buses can be loosely divided into three categories: low-end, mid-range, and high-end. Each type has its pluses and minuses, with the application dictating the appropriate one to implement. Some buses could be placed into more than one category. Low-end boards add some simple I/O functionality. They're basically inexpensive, but their functionality is somewhat limited. Examples of this type of implementation include SBX from Intel Corp., Hillsboro, Ore., and Industry Pack from Green Spring Computers, Menlo Park, Calif.

Industry Pack boards use a 2-in.^{2} module with a low-cost interconnect scheme. The bus doesn't operate at a high speed and a minimum number of data and address lines are used. In addition, some interrupts are handled. Silicon requirements for the interface can be managed by a few gates or a PAL.

The mid-range mezzanine bus enables the use of some memory or other higher-functionality I/O, such as SCSI, Ethernet, or alternative communication ports. These modules require more data, address, and control lines because a semi-intelligent microcontroller is synchronized to the local bus. This type of circuitry can generate some interrupts and allow some direct-memory access. Examples of mid-range mezzanine buses include SBus from Sun Microsystems, Mountain View, Calif. and DBUS-68 from Matrix Corp., Raleigh, N.C.

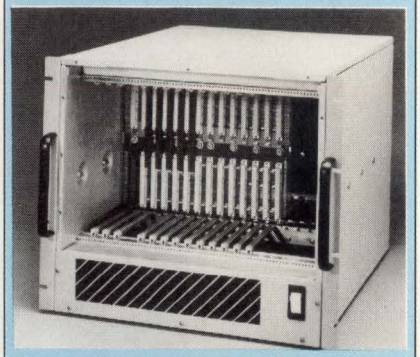
A full-function or high-end mezzanine bus can contain some intelligent devices and a sophisticated interface. Two examples of the high-end mezzanine bus are Corebus from Heurikon Corp., Madison, Wis., and FLXibus from Force Computers, Campbell, Calif., both of which are multiprocessing buses. SBus almost fits into this category because it's modules can contain reasonably-intelligent devices, but the bus can't be controlled from the mezzanine.

Corebus appears on both RISC and CISC CPU baseboards from Heurikon. To interface both high-speed modules (such as zero-wait-state memories) and slower peripheral modules (such as disk controllers), Corebus contains synchronous and peripheral buses. The synchronous bus features a 50-MHz clock speed and a maximum bandwidth of 200 Mbytes/s *(Fig. 1)*. Using the bus' two-wire handshake, masters can control all key timing parameters. There's also support for four interrupt lines, each containing a separate Acknowledge line.

FLXibus uses 32-bit data and address lines decoupled from the processor-to-memory bus. It offers VMEbus master and slave capabilities and is fully compatible with the 68020 asynchronous interface. The FLXi daughterboards designed by Force are called Eagle modules. They come equipped with an ASIC to handle the FLXi interface and some other logic to make the modules in-

Backplane Holds Both AT, VME Cards

Standard PC/AT boards can be mixed with high-performance VME boards in the N6280 AT/VME backplane. The industrial-grade enclosure mounts in a 19-in. rack and has positive locking for both types of cards. A 750-W power supply and two high-volume exhaust fans give the N6280 the power and cooling needed



to support a twenty-board system in a factory environment. Prices start at $4000, with OEM discounts available.

Nissho Electronics Corp., *Inwood Park, Suite 200, 17320 Red Hill Ave., Irvine, CA 92714; (714) 261-8811.* **CIRCLE 571**

■ *Booth 626*

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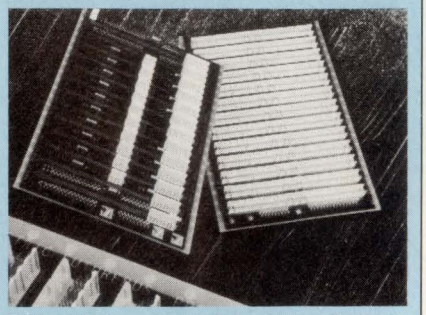
FUTUREBUS+ BACKPLANE SUITS HIGH-SPEED APPLICATIONS

A 13-slot, 16-layer backplane from BICC-VERO complies with Profile F of the Futurebus+, IEEE P896.2 specification. The spec supports a 128-bit data bus with central arbitration. Skew is minimized by the surface-mounted 33-Ω resistors and high-speed capacitors that are arranged to exactly match the length of each signal trace. The capacitors supply local high-speed charge storage to each line. Further protection from ground-bounce effects is made possible by combining multiple power and ground planes with a ground-tracking pattern. Conforming mechanically to IEEE 1301.1, the backplane is 300-mm high and supports hard-metric Futurebus+ 265-by-288-mm daughterboards. Power for the 5-, 3.3-, 2.1-, and



0-V rails is supplied to the backplane through the company's LOMET connector, which offers a low-impedance interconnect to the multiple power and ground planes. The backplane costs about $2000.

BICC-VERO Electronics Inc., *1000 Sherman Ave., Hamden, CT 06514; (203) 288-8001.* **CIRCLE 572**

■ *Booth 618*

terchangeable. Force currently offers modules for a host of applications, including the recently announced Eagle-10 and -11 boards with Ethernet and SCSI interfaces.

STRICTLY FORMAL

The specifications for a system bus, such as Multibus or VME, are very formal, in terms of timing and conformance to the standard. "Anytime you introduce formality into electronic interfaces, you introduce a certain level of performance degradation because there are a lot of timing issues that everyone has to conform to," says Ray Alderman, technical director of the VFEA International Trade Association (VITA), Scottsdale, Ariz. In a local or mezzanine interface, the guidelines aren't that formal. This aspect becomes significant when a board maker is building a board for a specific customer. Custom-application boards are easier to build, allowing them to reach the market faster.

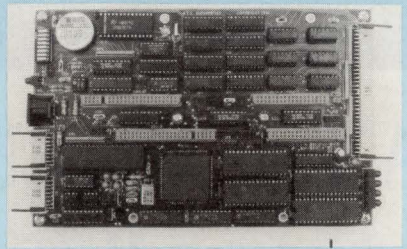
Mezzanine buses simplify some of the tasks that would otherwise be difficult to implement on a system bus. One example involves using multiple processors. On the system bus, it's difficult to work out the interprocessor communications, such as how data will be shared, how tasks will be assigned, and how the processors will be synchronized, among other considerations. Adding a second processor doesn't necessarily supply twice the processing power. If the first processor can produce at 90% of its potential (bus-overhead issues sap some of the power), the second adds about 70 to 80% because it must arbitrate for the bus and exchange data. Plus there's twice as much overhead. The power supplied by each additional processor diminishes as more are added. This varies from bus to bus because different buses contain different levels of overhead.

Mezzanines alleviate this problem because there are very few standard-related restrictions on the bus. Consequently, mezzanine buses like Corebus, FLXibus, and, to some degree, SBus are turning up with multiprocessing configurations. These buses permit multiprocessor integration, saving time and reducing complexity when compared to doing the same implementation over the system bus. "Mezzanines are an enabling technology for multiprocessing and solve the bottleneck problems associated with the system bus," adds Alderman.

Quite often, a mezzanine architecture is configured around a processor. If an Intel processor is used, timing and gating obstacles must be overcome. For most cases, some type of state machine would be required. If it's a Sparc processor, then SBus becomes a wise mezzanine choice because most of the timing work is already done. In addition, many companies have laid most of the groundwork needed to implement Motorola 68000-based processors.

EXPANDABLE SBC RUNS WITHOUT A BUS

Designed for embedded applications, the SBX-C186EB 16-bit single-board computer (SBC) lets engineers design custom products without expensive and complicated bus systems. Although the SBC contains no bus, it can be expanded through four on-board iSBX connectors. The board is built with an 80C18616-bit processor and an 80C187 coprocessor, both running at 16 MHz. On-board functions include a real-time clock, an interrupt controller, five 16-bit counter-timers, and 32 parallel I/O lines. Prices start at $425.



Connector kits, mounting hardware, and power supplies are available.

R.L.C. Enterprises, *4800 Templeton Rd., Atascadero, CA 93422; (805) 466-9717.* **CIRCLE 573**

■ *Booth 802*

Radstone Technologies, Montvale, N.J., based its two mezzanine architectures, PEX (Processor EXtension) and APEX (Advanced PEX), on the 68000 interface. The signal conventions used on a PEX board offer easy integration into the 68000-family environment because the interface's predefined signals are optimized for this architecture. Little or no conditioning of the interface signals is needed. The PEX interface implements the data and address paths in a non-multiplexed fashion, reducing the complexity of the on-board module and increasing the bus' throughput. Because the processor handles the module's control and data movement, the PEX interface is implemented as a slave interface. This lessens the bus' complexity because no arbitration circuitry is needed on the module or the baseboard.

APEX implements full 32-bit data and addresses to efficiently move data over the mezzanine bus. It supports such processor features as dynamic bus sizing and caching to increase flexibility and performance. Another feature of APEX is that it can inform the processor as to whether the data residing on the bus should be cached. Because APEX implements a full master-slave interface, the module can gain access to resources, such as memory, on the baseboard.

Another reason for opting to implement one architecture over another can be pinpointed to the number of mezzanine modules that are already available. For example, Sun Microsystems claims that at least 70 companies currently build SBus modules. Hence, almost any function a user could need is available. The baseboard manufacturer needn't worry about building a new module for each customer.

At last count, 22 mezzanine buses were being implemented on the VMEbus. Twelve of those have been placed in the public domain (meaning anyone can use them without incurring any costs). Making them public, though, causes them to be somewhat rigid: The governing companies can't just change the specifications on a whim. VITA became the holder for every mezzanine specification that's in the open domain, but doesn't rule on or change them (VITA publishes a document containing the specifications for each mezzanine bus, which is available for $49). VITA looked into the possibility of standardizing one mezzanine bus for the VMEbus. But the idea was rejected after determining that different architectures are needed for the countless applications.

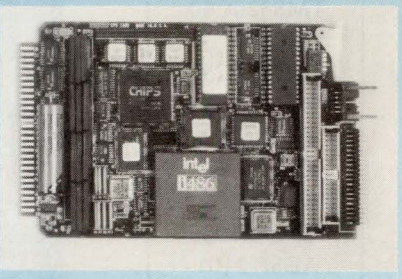
The twelve open architectures are: LEB (a mid-range bus) from Eltec, Germany; FLXibus (high-end); SAMbus (mid-range) from General Micro Systems, Montclair, Calif.; Industry Pack (low-end); Corebus (high-end); IV-XXXX (mid-range) from Ironics, Ithaca, N.Y.; DBUS-68 (mid-range); Omni (mid-range) from Omnibyte, West Chicago, Ill.; E-PAK and I/O PAK (mid-range) from Performance Technologies, East Rochester, N.Y.; EXMbus (mid-range) from RadiSys, Beaverton, Ore.; PEX (low-end) and APEX (mid-range); and SBus (high-end).

THREE-IN-ONE

The Modular Interface eXtension (MIX), from Intel, offers something that VME-based mezzanine buses don't—the ability to stack up to three daughterboard modules on one baseboard. The 386 and 486 MIX baseboards include everything needed to connect the boards to the Multibus II bus, including the controller logic. The maximum transfer rate across

STDBUS ADVANCES TO 486 LEVEL

Designed for industrial computing applications, the 7874 STDbus single-board computer (SBC) is based on Intel's i486 microprocessor running at 25 or 33 MHz. Full 32-bit data transfers can be made to the on-board RAM (4 to 16 Mbytes). The SBC operates with any STD I/O card that conforms to the STD-80 series specification for adding application-specific I/O functions. Microsoft's DOS 5.0 is included in the on-board ROM. Up to seven 80X86 CPU boards can be installed in the same backplane with the 7874. The board



comes with standard PC/AT peripheral devices, including a keyboard interface, two RS-232 serial ports, a parallel port, interrupt and DMA controllers, a counter-timer, and a battery-backed real-time clock. An optional VGA video board can be added. With 4 Mbytes of RAM, the 25-MHz board goes for $2995.

***Pro-Log Corp.**, 2555 Garden Rd., Monterey, CA 93940; (408) 372-4593.* CIRCLE 575

■ *Booth 104*

VME BOARD INTERFACES TWO MIL-STD-1553B BUSES

Two MIL-STD-1553B buses can be interfaced using the MBI-2, an advanced full-military-specification intelligent VME-based board from Radstone Technology. Key features of the MBI-2 include one or two dual-redundant MIL-STD-1553B buses, a master-slave VMEbus interface with high-speed DMA controllers, and a 68020 processor subsystem to handle all of the 1553B protocols. A second offering from Radstone, the single-slot FDDI-1 commercial FDDI controller, comes with separate data paths for control and processing elements. The board can hold up to 8 Mbytes of DRAM with 128 kbytes of FDDI buffer static RAM. Built with AMD's Supernet-2 chip set, the FDDI-1 offers concurrent 100-Mbit/s data transfers.

***Radstone Technology Corp.**, 20 Craig Rd., Montvale, NJ 07645; (201) 391-2700.* CIRCLE 574

■ *Booth 426*

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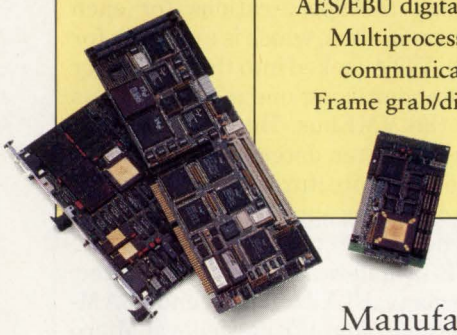
	Multiprocessing	DSP56156
	communications	DSP56001
	Frame grab/display	ADSP-21020
		ADSP-2101
		ADSP-2100
		DSP32C



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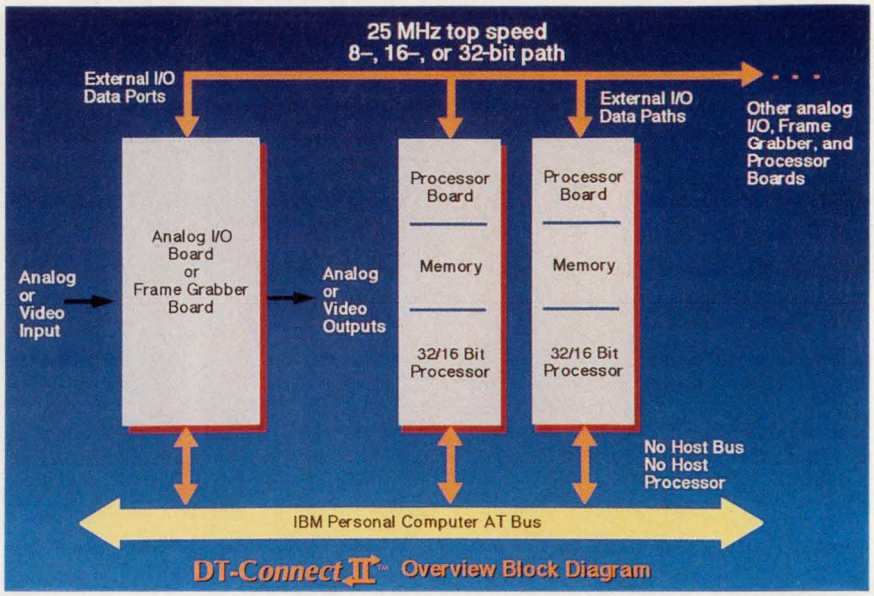
the MIX bus is about 22 Mbytes/s, compared to about 2 Mbytes/s across Intel's SBX bus. In addition to the modules offered by Intel, users can customize their baseboards by designing company-specific modules using Intel's module-development kits.

The recently introduced 486 MIX baseboard has expanded-memory addressability—up to 68 Mbytes using two memory modules. Intel will continue to proliferate the daughter modules. "When people seem to be running out of gas with the 486 board, we'll throw something faster at them from a processor point of view. People have yet to exhaust MIX's bandwidth, so that's not a problem yet," says Dick Binns, hardware marketing manager at Intel. The idea behind MIX was to disassociate CPU technology from I/O technology so they could evolve at their own paces.

The initial modules offered by Intel were about half the size of a Multibus II card. Later, users were permitted to implement full-size daughterboards by stacking them under the baseboard. The original half-size cards are stacked on top of the baseboard.

Multibus II contains built-in testing circuitry that was extended into the MIX architecture. Each module contains an EPROM containing the system tests. Consequently, those boards are tested in the same manner as the baseboard. Multibus II also contains the logic needed to identify what types of boards are connected to the bus. That interconnect access was also included in the MIX modules so that the modules will identify and include themselves in the baseboard's interconnect information. An agent on the bus can then determine if a MIX baseboard is present, where it resides, if MIX modules are attached to the baseboard, and what type of modules they are.

The Futurebus+ specification incorporates a mezzanine architecture. Users will be able to stack multiple modules on its Futurebus+ Small Computer Expandability Module (FSCEM) bus. These credit-card-size modules will boast a maximum operating speed of 250 MHz.



3. DESIGNED FOR THE PC/AT'S ISA architecture, DT-Connect II from Data Translation transfers data at speeds up to 100 Mbytes/s. This specification is logically and electrically compatible with its predecessor, DT-Connect, thus making it backward-compatible. Because the standard's 32-bit modes are symmetrical, any board can transfer data to and from any other board within the connection.

MIX and Onboard Modular Expansion (OME) from Siemens, Munich, Germany, also designed for the Multibus II environment, differ from SBX in the amount of available processing power. SBX is usually an extension of a base CPU board that's just looking for one extra feature. The MIX and OME boards are being relied on for independent functions, such as digital-signal processing or some high-performance I/O or communication application.

OME is similar in ability to MIX, but has a bandwidth of 40 Mbytes/s, compared to MIX's 22 Mbytes/s. It's not processor-specific and has been implemented on i860- and i960-based boards. In 1991, the number of MIX- and OME-based mezzanine boards grew by about 20%, from about 40 to around 50. SBX modules, now numbering around 200, increased by about 5 to 10%.

SBX has appeared on other buses besides Multibus. In fact, it's quite common on the STD bus. Computer Dynamics, Greer, S.C., offers SBX

SPARC COMPATIBLES ADD INTERNAL MBUS

Two Sparc-based VME boards, the SparcCards 2LC and 2SE, are compatible with the Sun Microsystems SparcStation 2, but contain an internal high-speed Mbus architecture. The two cards are fully VMEbus compliant, including address mapping for multiprocessing. The boards' integer performance is 30 MIPS at 40 MHz. The 2LC contains a 32-kbyte cache memory and 8 or 32 Mbytes of main memory, while the 2SE can hold 32 or 64 kbytes of cache and 8, 32, or 64 Mbytes of main memory. In addition, the 2SE has a built-in SCSI II controller and contains two SBus expansion slots. The 2LC sells for $5995, while the 2SE is priced at $7995.

***Themis Computers,** 6644 Owens Dr., Pleasanton, CA 94566; (415) 734-0870.* CIRCLE 576

■ *Booth 723*

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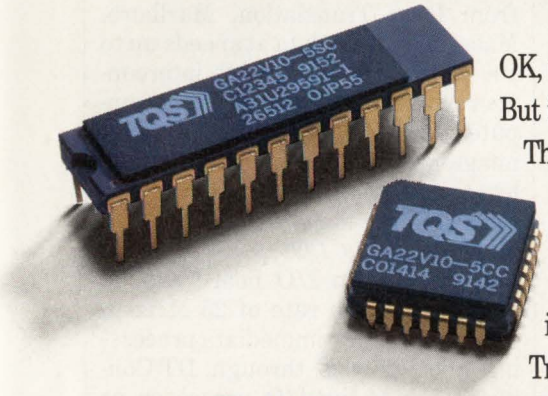

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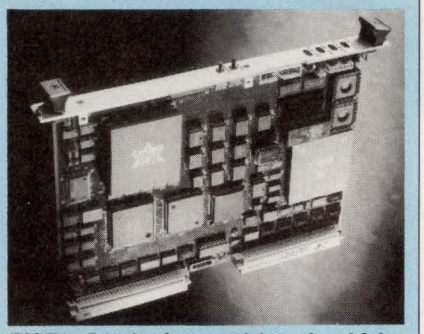
RISC-Based SBC Suits Compute-Intensive Tasks

Motorola's latest single-board computer is based on the company's 88110 symmetric superscalar RISC microprocessor, which operates three to five times faster than its 88100 processor. The single-slot 6U board's architecture enables the 88110 to operate at peak performance during all operations. The board can be used for SCSI II peripheral I/O, multiple users, and networking. The 3D-graphics execution units and enhanced floating-point capability of the 88110 suit the board for compute-intensive applications. Flexibility is maximized using an expansion mezzanine port and a standard VMEbus subsystem bus



(VSB). Limited quantities should be available by the middle of the year.

Motorola Computer Group, *2900 South Diablo Way, Tempe, AZ 85282; (800) 234-4VME.* CIRCLE 577

■ *Booth 502*

modules for video control, parallel I/O, and memory, as well as other applications. The company's recently released CDX-COM is a communications module that offers PC/XT/AT-compatible serial and parallel ports. Standard features include two serial communications ports; RS-232, RS-422, or RS-485 communications; an asynchronous baud rate to 115 kbaud; and a bidirectional parallel printer port.

A variation of the mezzanine bus is the MXbus from Mizar Inc., Carrollton, Texas. The proprietary MXbus is based on the company's family of 680X0 VME CPU modules that contain VMEbus master and slave interfaces, EPROM, DRAM, full four-level system controllers, serial I/O, and interrupt features. These boards were designed with a standard 16-bit expansion interface, but can be used with 32-bit CPU modules. Any 16-bit MXbus expansion card can be connected to a higher-speed 32-bit CPU module without requiring an expensive redesign.

Side By Side

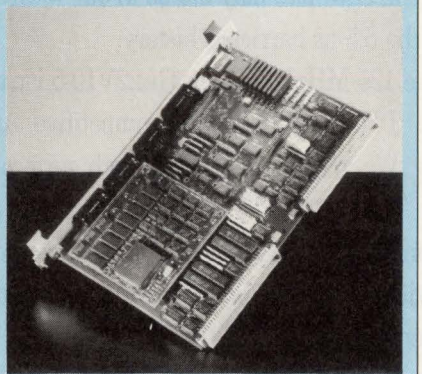
The expansion interface can be placed on the edge of a 3U VMEbus card. By plugging in a 3U "side card," both boards can fit into a standard 6U chassis *(Fig. 2)*. Current MXbus modules range from simple I/O ports to complex parallel-processor expansion modules.

Motorola's VME Subsystem Bus (VSB) is a secondary bus that offloads the VMEbus. The VSB lets a multiprocessor system functionally divide into local subsystems, with each processing one part of an application. By removing traffic from the VMEbus, overall system performance is improved. The Extensible VSB (EVSB) is a superset of VSB, with allowances for propagation delays. It allows a ribbon cable of up to one meter between the host, and as many as six EVSB modules. The downside to EVSB is that it takes up slots in the VME backplane or some other I/O area.

On the Industry Standard Architecture (ISA) bus, DT-Connect II from Data Translation, Marlboro, Mass., transfers data at speeds up to 100 Mbytes/s. The 32-bit interconnect scheme eliminates the host computer from the data-acquisition or image-processing loop *(Fig. 3)*. This lets time-critical data bypass the bottleneck in the host bus (ELECTRONIC DESIGN, *Dec. 19, 1991, p. 24)*. Data acquired from an I/O board can be transferred at a rate of 25 MHz to other boards for immediate processing and analysis through DT-Connect II. Up to five I/O, processor, or memory boards can be tied together.□

Choose AT&T Or TI Processors With DSP Board

Users can elect to use either one or two of AT&T's DSP32C or Texas Instruments' TMS320C31 processors in Burr-Brown's ZPB3400 floating-point DSP board. The processors are mounted separately on plug-in daughterboards. With the attached daughtercard, the ZPB3400 can supply 25, 33, 50, or 66 MFLOPS of performance, in addition to handling real-time data-input sample rates up to 10 MHz. Each processor has its own serial bus to allow for parallel processing of multiple data channels or serial processing of one data channel. The board can hold either 1 or 4 Mbytes of triple-ported DRAM. Data to and from the processors can be sent through the VMEbus, the input FIFO



buffers, or the high-speed serial port. Prices start at $4495.

Burr-Brown Corp., *P.O. Box 11400, Tucson, AZ 85734; (602) 746-1111.* CIRCLE 578

■ *Booth 912*

How Valuable?	Circle
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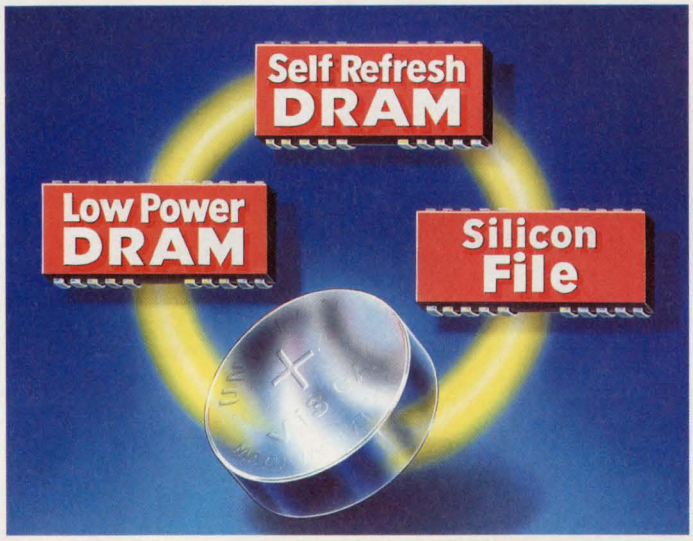
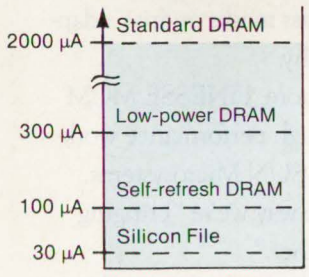
Moderately	525
Slightly	526

Low-power DRAMs

The Low-down on Memory Power



Memory devices are as varied as the applications they are designed for, but in this age of miniaturization and mobility they have one thing in common: power consumption must be rockbottom. Capacity, speed, price or package choice may be your highest priority, but you'll be glad to know that DRAM memories from NEC operate on an absolute minimum power supply.



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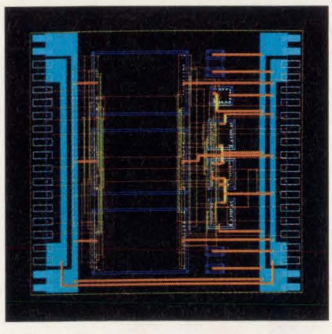

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MEMORY CONTROLLER TRIMS BUS-TRANSFER DELAYS AND BOOSTS CACHE EFFICIENCY BY MANIPULATING WIDE MEMORY WORDS.

ACCELERATE DRAM ACCESSES WITH CONTROLLER MODULE

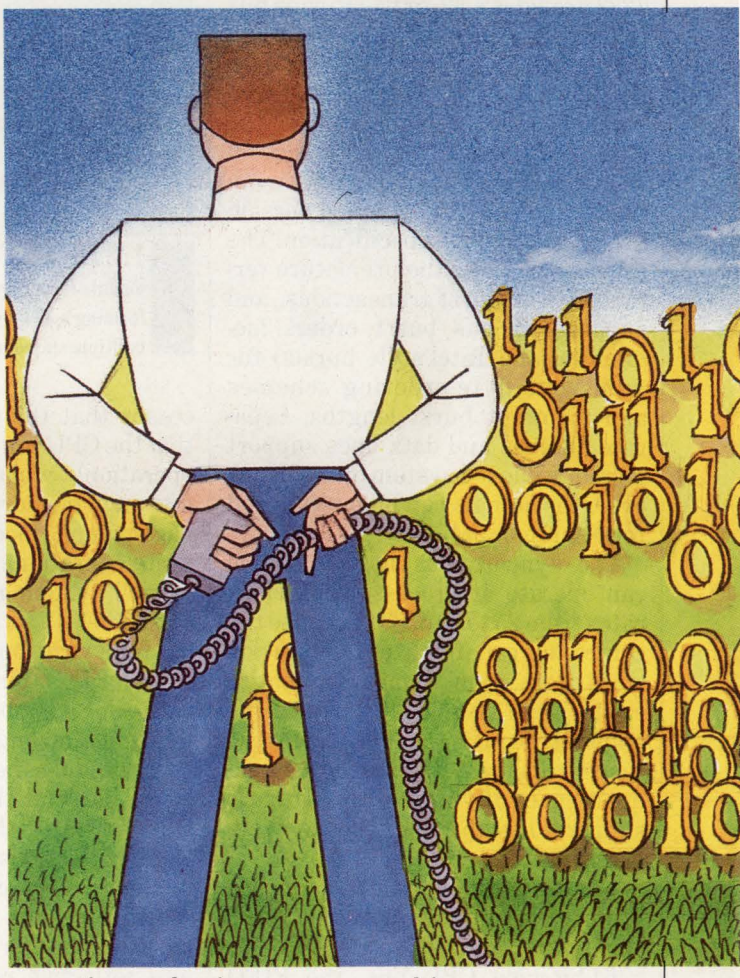
DAVE BURSKY

As the latest high-performance 32- and 64-bit microprocessor systems boost their clock rates to 30 MHz and beyond, on-chip first-level caches become a necessity to ensure that the processor receives a constant flow of data and instructions. The cache also acts as a buffer between the slower second-level cache or slow DRAM main memory and the host processor. Although the cache solves bus bottlenecks to the host processor, it creates another bottleneck between the cache and the main memory.

One way to reduce that bottleneck is by using a second-level cache. But that just pushes the bottleneck out one level. Other alternatives include the widening of the memory bus that connects the DRAM to the processor's first-level cache, or employing faster main memory. Currently, most system manufacturers opt for the wider buses to move more data every cycle.

At the DRAM-to-cache-controller interface, the bus is typically 128-bits wide, while 64-bit-wide buses are used between the cache controller and the cache. At the same time, larger second-level caches are being designed in—128 kbytes to 1 Mbyte is not uncommon. However, to tie the cache into the wide buses, designers must typically develop custom cache and memory controllers.

Because time-to-market and cost for high-performance systems have become key considerations, engineers at Cypress Semiconductor predesigned the memory controller, which comes in a multipackage module that handles several functions. These include word slicing and reassembly, DRAM system refresh with scrubbing, error detection and correction, and uniprocessor or multiprocessor system bus interfacing. There will be two versions of the 400-pin 7.8-in.^{2} controller—one for 32- or 64-bit processor buses (the CYM7232) and one for 64-bit CPU buses (the CYM7264). The 7232 performs error detection and correction on 32-bit words; the 7264 does 64-bit error correction and detection.



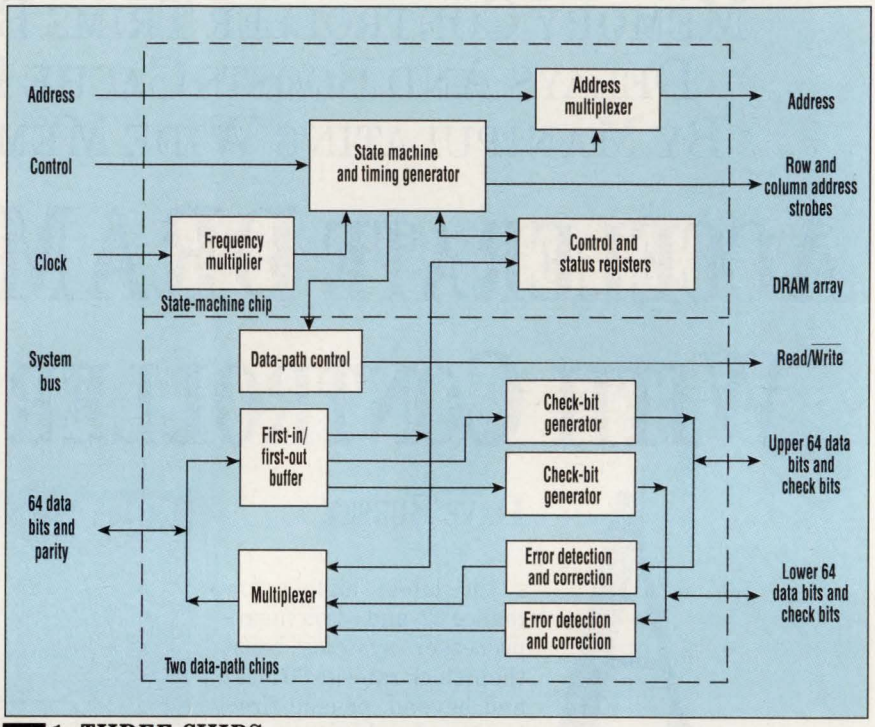
By using the wide main-memory words, the controller can match the peak burst-transfer

rate of the data from the DRAM array to that of the second-level cache. That's because it will supply words to the CPU at the maximum rate the CPU's internal cache can absorb the data. Furthermore, it allows relatively inexpensive DRAMs to be used—memory subsystems with 80-ns access times can be employed rather than expensive 50-ns DRAMs. Module applications range from high-performance workstations and multiprocessor compute servers, to massively parallel computing and video-graphics accelerators.

On the host-processor side, the 7232 provides a 32- or 64-bit-wide bus (plus parity bits for each byte and four parity bits for the address). On the DRAM side, there are seven check bits per 32-bit word. For the 7264, there are eight check bits on the DRAM bus interface. Both modules implement an extended version of the Sparc Mbus specification. The extensions allow the premature termination of burst transactions, and support various burst orders (sequential and Intel-style bursts) for numerous byte-ordering schemes and different burst lengths. Separate address and data lines support non-multiplexed system buses. However, the signals can be multiplexed for Mbus compatibility.

The synchronous host interface can operate at processor-bus clock rates from 25 to 50 MHz. Because the controller can fetch a 128-bit-wide word from main memory, an entire cache line of four 64-bit words can be transferred in 240 ns (two wide-word reads from the DRAM array). An address space of 4 Mbytes to 1 Gbyte is supported by the module's 36-bit address bus.

First-in/first-out buffers on the host-processor side of the data-path chip are eight 32-bit words deep. For a 64-bit-wide CPU bus, the FIFO buffers would be configured as 16-levels-deep by 64-bits wide. The outputs from the FIFO buffers are then reassembled, when necessary, into the 128-bit-wide words that are actually written to the DRAMs. Each time the processor writes to the external memory array, the FIFO buffers capture the data and tell the processor that the data is written (so that the CPU can go off to do another operation), while the actual write into main memory is done in a sort of background mode (typical posted-write operation). That improves the overall system responsiveness, because the CPU is rarely left idle waiting for a write operation to finish.



1. THREE CHIPS form the CYM7232 or 7264 DRAM accelerator and controller module from Cypress Semiconductor. Two of the three custom chips are identical, with each forming a 32-bit slice (7232 only; 64-bit paths in the 7264) of the data path. The third chip, a multiple-state-machine IC, controls the module's interfaces and word-transfer timing.

The FIFO buffers also support cache-line copyback and fill operations, minimizing a system's bus activity because the data can be sent as a line burst at the maximum FIFO transfer rate—20 ns/word for the 50-MHz versions. Reads and writes to the memory can be inhibited for multiprocessor support. Furthermore, inhibited reads can be turned into reflective reads, and inhibited writes may be turned into reads-for-ownership—operations ideal for multiprocessor support.

Reflective reads begin when a secondary cache in a multiprocessor system goes to main memory for a line fill. If the valid data is in another secondary cache rather than in the DRAM (stale data is in DRAM), the read from the DRAM must be inhibited by the secondary cache that owns the data. That secondary cache then supplies the data to the requesting secondary cache and writes the valid data into the DRAM.

Reads for ownership keep the system from stalling if requested data is not in a cache. The read-for-ownership operation does that by turning a write from a processor into a read by the cache to fill a cache line. When a CPU tries to write a byte into a line that turns out isn't in the cache (and doesn't know if the line is cacheable to start with), the cache must first read the line from DRAM and then write the data into the line.

Thus, the write operation for the byte is started, but at the same time the cache checks for the line. If the line isn't found, the byte-write operation is inhibited while the cache checks to see if the line is cacheable. If it is, the cache brings the line in and the byte is written into the line. If the line is not cacheable, the byte-write operation started at the beginning of the cycle continues and the

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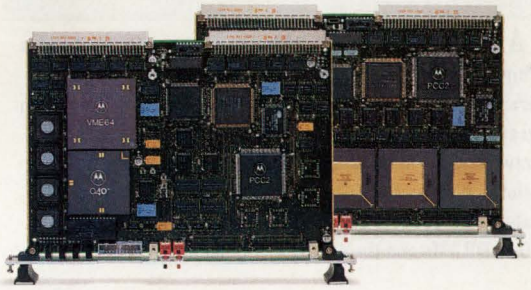

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byte is written directly to the main memory as a write-through cycle.

Single-byte and partial-word transfers are also permitted with the read-modify-write (RMW) DRAM cycle. The old word is accessed and combined with the new data under control of the address and size inputs. A new set of error-detection and check bits is generated, and the modified word is written back into memory. In the 7232, a RMW cycle takes place for all writes less than 32 bits. In the forthcoming 7264, a RMW cycle occurs for all writes less than 64 bits.

The 7232 multichip module subsystems consist of three 184-lead CMOS chips *(Fig. 1)*. Two of the chips are identical, and each forms a 32-bit-wide slice of the 64-bit host-processor data path. In the forthcoming 7264, there will also be two identical data-path chips that are interleaved to handle alternate words. These chips perform only 64-bit error detection and correction. Together, the two data-path chips form the 128-bit-to-64-bit, or 128-bit-to-32-bit (7232 only) data funnel for reads from the main DRAM to the system bus. In the other direction, the chips accept 32- or 64-bit words and concatenate them, check bus parity, and then feed a 128-bit-wide word to the DRAM array. A simple error-logging facility is available; errors will be logged by recording their syndrome values in a FIFO buffer and their burst address (or scrubbed address) location in a register. Interrupts will be generated to the CPU whenever an error occurs.

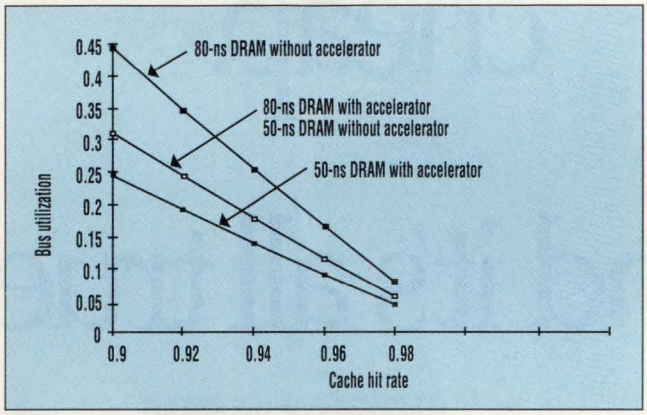
To perform those operations, the data-path chips include check-bit generators, error-detection-and-correction logic, the scrubbing data path for the DRAM background refresh, and a pipelined and buffered data multiplexer-demultiplexer *(Fig. 1)*. The third chip in the trio contains multiple state machines that control all of the operations—including DRAM refresh—and ensure a close coupling to the various microprocessor buses. Processor buses, such as the Sparc, the Motorola 88110 and 68040, the MIPS R4000, and the Intel i860 and i486, are all supported, along with their respective secondary cache memories.

To ensure proper system timing, the state machines on the control chip operate at high speed. Four of the state machines run at 100 MHz; eight others run at 50 MHz. Many programmable options exist on the controller chip to set up the DRAM refresh timing, the bus interface, the bus timing, and other aspects of the system. The clock's rising edge is used by the synchronous host side of the interface. Every system transaction is split into an address or control phase and one or more data phases.

When building high-performance systems, one goal is to minimize system bus utilization. That can be done by speeding up the transfer of data from the memory array to the processor or vice versa. Some system examples might better illustrate the performance impact of different-speed DRAMs and systems with and without the module. The simplest case could be a 50-MHz CPU with secondary cache and off-chip DRAM that accesses in 80 ns *(Fig. 2)*. That simple case results in a range of bus utilization from about 45% with a 0.90 cache hit rate to about 8% if the cache hit rate goes to 0.98.

More efficient bus utilization (lower utilization percentages) improves the ability of the bus to handle more processors before saturating—such as is needed in compute servers and symmetrical multiprocessor systems. However, in multiprocessor systems, the memory bus tends to be the weakest link. By reducing bus utilization, additional CPUs can be added without negatively impacting the performance of CPUs already in the system.

As faster 50-ns DRAMs are employed, the bus utilization improves by decreasing to a range of 31% with a cache hit rate of 0.9 down to about 6%, if the hit rate goes up to 0.98. By adding the accelerator to the DRAM subsystem, 80-ns DRAMs plus the CYM7232 would yield the same results as a system based on very expensive 50-ns DRAMs. Still higher-performance systems can be implemented by adding the accelerator to DRAM arrays that employ the 50-ns chips. Such a combination starts with less than a 25% bus utilization that has only a 0.9 cache hit rate and only about a 5% bus-usage level as the cache hit rate increases to 0.98.□



2. IN A TYPICAL, simple RISC-based system that only uses an on-chip cache and external DRAM, bus utilization changes considerably as the cache hit rate increases. Four cases are shown in the graph: using 80- and 50-ns DRAMs with and without the accelerator module. Matching performance can be achieved using the accelerator with 80-ns DRAMs or 50-ns DRAMs without the accelerator. The smallest bus utilization percentage is achieved using 50-ns DRAMs and the accelerator module.

PRICE AND AVAILABILITY

The CYM7232 and CYM7264 DRAM accelerator and control modules come as 400-lead pin-grid-array building blocks. They will be available in speed grades from 25 to 50 MHz. Prices peak at $327 apiece in lots of 100 for the 50-MHz versions. Samples will be available in the early second quarter. The 7264 is expected by midyear.

Cypress Semiconductor Corp., 3901 N. First St., San Jose, CA 95134; John Murphy, (408) 432-7100. **CIRCLE 511**

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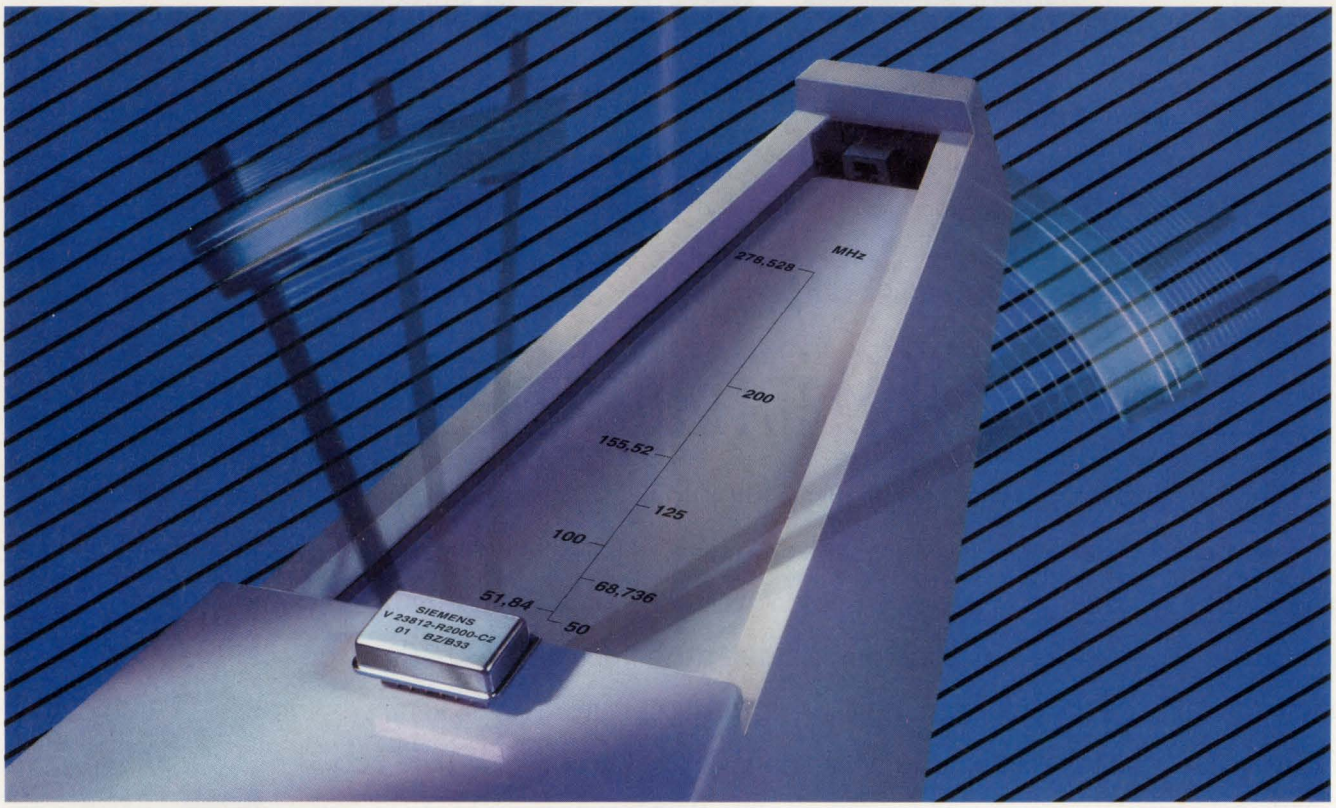

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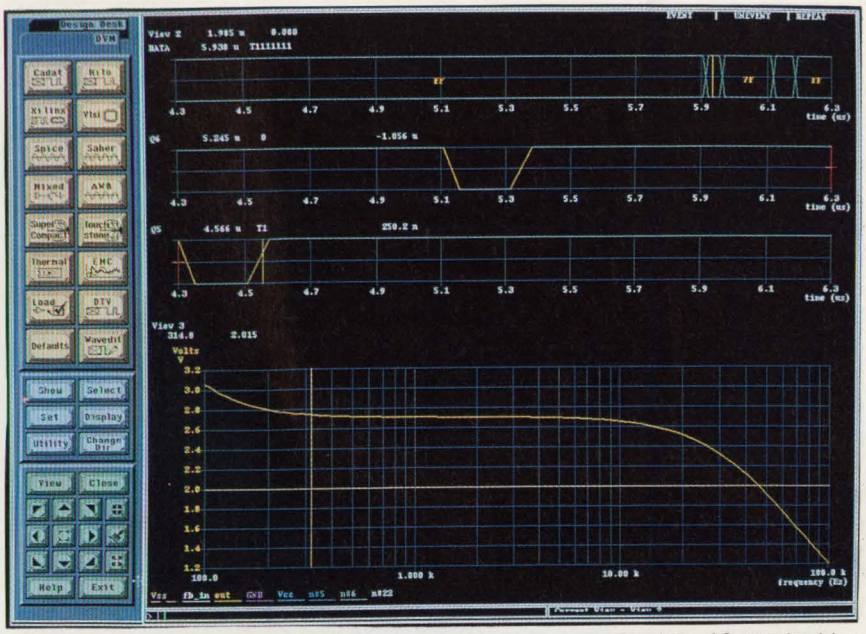


Courtesy of Computervision

SYSTEM SIMULATION STILL HOLDS PROMISE

LISA MALINIAK

MOST DESIGNERS PROFIT FROM SOME ELEMENT OF SYSTEM SIMULATION, BUT FEW PRACTICE IT IN PURE FORM.

It's the dream of both EDA vendors and users to one day eliminate prototypes and completely automate system design. As the EDA industry slowly inches toward that goal, system-level simulation is increasingly thrust into the spotlight. System-level simulation can range from modeling an entire multiboard system at the behavioral level to simulating every element in that system before any prototype is ever built. And though many design teams are practicing some degree of system simulation within that range, no design teams are creating products without building prototypes.

System-level simulation—simulating an entire system at a high level to verify that the architecture is correct—is typically done when a brand new system is being designed and lots of thought must be given to architectural issues. Very high-level simulation is possible with products like SES/workbench from Scientific and Engineering Software Inc., Austin, Texas. With SES/workbench, engineers can model hardware- and software-based systems at a high level, and simulate the complete system including the application software. Users can address design trade-off issues early on, before any architectural commitments are made. "The cost of making a bad decision is very steep," comments Doug Neuse, vice president of simulation software products for the company. "Our product helps answer strategic questions about what a product is going to be, not just it's implementation."

The practice of simulating a system at the low level to ensure it meets the specifications is driven by ASIC design and the need to get the ASICs working on a board. Most designs tend to be incremental, explains Steve Caplow, director of market development for Cadence Design Systems Inc., Lowell, Mass., so large amounts of simulation aren't usually necessary.

Although most of today's engineers would like to simulate anything and everything in a system,

most simulate only where they think a problem will occur *(Fig. 1)*. Systems consist of hardware, software, and firmware that may contain analog and digital components, ASICs, standard devices, programmable devices, memory devices, and peripherals. In addition, systems may have high-speed backplanes and complicated interfaces to the outside world that could in themselves be other systems. Engineers also need to simulate components like transducers, actuators, and sensors with their circuits, all in one environment *(see "Expanding simulation to meet total system needs," p. 56)*.

In many situations, a thorough system simulation entails modeling non-electrical effects. For instance, a communications engineer may want to model his entire system, including such mechanical components as antennas and fiber-optic cables. One useful simulator in that type of application is the Saber simulator from Analogy Inc., Beaverton, Ore. The Saber simulator can model components in many different disciplines, not just electrical, and have them simulated in one environment.

The benefits of system simulation are numerous. For instance, by using simulation, managers can compare the performance and functionality of systems designed by different design teams and vendors. Simulation also reveals chip behavior that surfaces only when the chip is installed in its working environment. In addition, simulation can attempt to model the behavior of a standalone chip by itself and on a board, the behavior of that board in a backplane, and that backplane's behavior in a system of boards and backplanes. One of the biggest benefits, says David Smith, vice president of engineering at Analogy, is that simulation not only helps engineers build a more correct design, but also helps them to better understand the design's boundaries and limits. In other words, simulation will indicate both when a product will and will not work.

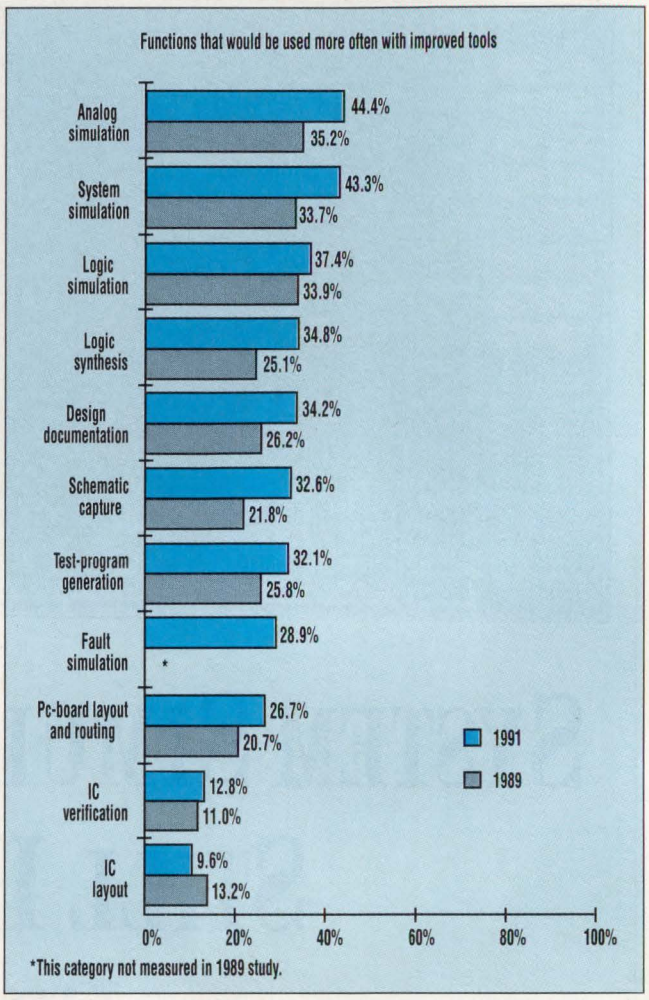
With today's complex designs, verifying a design with simulation before costly prototyping is nearly essential. Generally speaking, a 25k- to 30k-gate array can cost between $25,000 and $30,000, depending on the geometry and technology. A circuit board that contains several of these custom chips can become pricey. At that point, it's critical that the chips be verified within the target system before the designer commits to any silicon.

Also, most system designs are partitioned into several blocks and assigned to different design teams. Continually checking the interfaces between and within these blocks is critical. Very often, design teams create blocks that function perfectly as standalones, but malfunction when plugged together.

A different way to assess what simulation can do for engineers, points out Kuhoo Goyal, digital marketing manager for Dazix, Sunnyvale, Calif., is to look at what prototyping won't let engineers do today. For instance, there's no room for any form of "what-if" analysis with a prototype. Consequently, manufacturing variations can't be accounted for. Critical margins, such as voltage, power, timing, and thermal tolerances, can't be varied with prototypes. Although it's a good practice to get a prototype working in the lab, the engineers verifying a design with that prototype can't determine how close it came to failing. Nuances like that can't be uncovered with prototyping because the engineer is analyzing an already "manufactured" device or devices. In other words, there's no way to cover any type of manufacturing variation unless it's related to the particular device that's being used for the prototype.

David Hardman, product planning manager for Logic Automation Inc., Beaverton, Ore., also feels that prototypes fail in many areas where simulation succeeds. For example, engineers can't get to the internal workings of buried chips with prototypes. There's less observability, which means it's difficult to perform different types of analysis.

Although the benefits of simulation can be immeasurable, problems



1. RESULTS FROM a 1991 design-automation survey commissioned by *Electronic Design* show that users continually want to simulate more, but feel that they need better tools to do it. Almost half of those questioned wanted to perform system-level simulation, up from 33.7% in 1989.

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can abound for engineers trying to implement system-level simulation *(see "Simulation solves only part of the design-verification problem," p. 58).* The electronics industry faces a very big hurdle to full system simulation—the lack of simulation models for every device in the system. Ping Chao, co-founder of PiE Design Systems Inc., Sunnyvale, Calif., explains that there's a spectrum of options open to engineers, each with a different level of speed and flexibility. Such options include hardware modelers like those from Logic Modeling Systems Inc., Milpitas, Calif., and software models from third-party sources like Logic Automation Inc. The company carries over 13,000 software models, including their new Simubus model that simulates a VME bus, enabling engineers to verify if a board or boards meet VME specification.

Even though EDA vendors have provided users with many options, often they fall short. Kevin O'Leary, electronic CAE product manager for Computervision, Bedford, Mass., contends that the customers he has talked to can't get more than 75% of all the models they need. He adds that many times they can do other things to get around that, such as in-house modeling service.

However, engineers end up paying for these model options in terms of money, accuracy, and time. For instance, Kuhoo Goyal of Dazix points out that although hardware modelers have come a long way in performance, they're usually still the slowest segment of a system-level simulation. Also, because third-party modeling services provide behavioral models, fault simulations are limited to the I/O ports of devices, leaving the internal states unknown. According to Goyal, the model solution boils down to engineers "making up in time what they lose in accuracy."

For true system-level simulation to become a common-practice reality, silicon vendors must shoulder more responsibility in supplying models of their standard parts. Terry Strickland, test and simulation product marketing manager for Compass Design Automation, San Jose, Calif., explains that there are varying levels of model support among silicon vendors at the moment. ASIC vendors, he goes on to say, must begin offering hardware-description-language (HDL) models because that's the direction in which most engineers are headed.

Logic Automation's David Hardman points out that getting the models is only the beginning. Timing problems can arise when mixing models from different sources, creating yet another kink for engineers to iron out. And as systems run at higher clock rates and timing margins narrow, this kinks grows more ominous. Open Verilog International chairman Bruce Bourbon adds that because more of the simulation is being done at higher levels of abstraction, the interoperability of models described in different HDLs is also important.

With simulators like AdvanSIM

EXPANDING SIMULATION TO MEET TOTAL SYSTEM NEEDS

When electronic engineers conceive of system-level simulation, they most likely think of chips and pc boards. The fact is, however, that other portions of a system, like mechanical parts, can affect the way the electronics function. That's why Computervision, Bedford, Mass., is leveraging their strength in mechanical design tools to help electronic engineers address non-electronic problems.

The company's definition of system simulation extends well beyond the board level. It includes the backplane, enclosure, cabling, and so on. Kevin O'Leary, electrical CAE and framework product manager for the company, explains that Computervision is looking to standards and third parties to help with the lower-end ASIC simulation while they focus on the higher-end system problems. In addition, the company has a framework they believe can tie everything together in one user-friendly environment. Frameworks are useful because they make data accessible to all of the tools and they supervise design flow.

Computervision is helping engineers tackle such problems as the dynamics of the heat generated from multiple boards in a box. Their tools look at the problem mechanically, finding electronic problems that ignite from the physical side. For example, in the automotive industry, there's often interaction between the engine electronics. Components like spark plugs, however, aren't conducive to having pc boards anywhere nearby because of several factors, including noise and stress. Therefore, the Computervision system defines restrictions (where the board can and can't go) from the mechanical end.

Engineers must start looking toward larger-scale system simulation because even if their boards work when tested, they may not work when they're installed in, for example, an automobile. A sophisticated car or truck may have up to 25 pc boards in it, all wired together with lots of interaction going on through the wires. The system engineer must verify that the wires are connected correctly, or none of the boards may function properly.

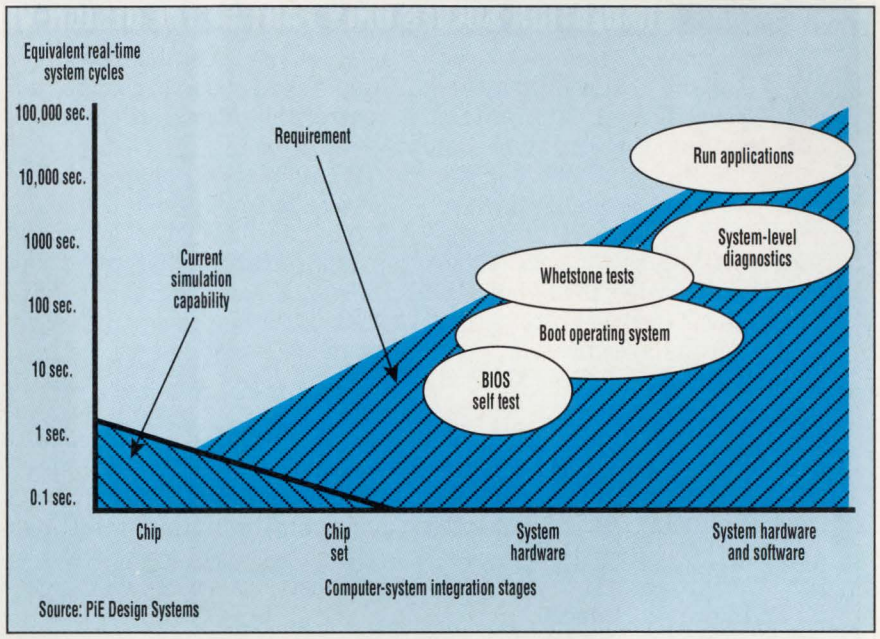
Computervision approaches this problem with a combination of its own wire-harness tool, the Analogy Saber simulator for analog portions and Racal-Redac's Cadat simulator for the digital portions, all tied together under a framework. The wire harness is the collection of wires that connects all of the boards and switches to the control system. Because an automobile prototype may take several months to build, and even then a wiring problem is hard to locate, this type of system-level simulation is critical for time-to-market success.

from Dazix, users can write their own simulation models in languages like C and VHDL, providing yet another angle for the user in terms of model resources. A key question is one of accommodation: Does the simulator to be used for system simulation accommodate any type of model, defined at any level of abstraction, without performance or accuracy degradation?

Whether an engineer writes his or her own models or buys them, explains Analogy's David Smith, the models need to be "appropriate to the questions that need to be answered." For example, a behavioral model won't help the engineer who's looking to verify detailed timing. To be useful, models must use the right level of abstraction. Engineers who write their own models can guarantee that the models are appropriate. If an engineer needs a microprocessor model, for example, he or she can build that model to suit his or her particular application and cut out unnecessary features. If the processor has four operating modes and only one is used in the application, there's no need to model all four. This type of tailored model saves the engineer much time.

Simulation performance can also become a big headache for engineers doing system simulation *(Fig. 2)* Performance is affected by both a host computer's processing speed and the available memory. Another factor, according to Jim Kenney, simulation product marketing manager for Mentor Graphics Corp., Wilsonville, Ore., is the amount of time a simulator takes to load in a design. This is especially true when an engineer is saving design changes often and must reload the data each time.

Actually, the simulator's speed in relation to the time spent by the engineer can be a relatively small portion of the overall simulation-verification cycle. For example, time spent on creating good test vectors that exercise the circuit require lots of time from the user. Also, the iterative cycle of changing, recompiling, and resimulating the circuit makes up a major component of the simulation cycle.



2. THIS GRAPH ILLUSTRATES why today's software-simulation approaches fall short when trying to verify a computer system. The simulator must perform almost 100 seconds of equivalent real-time system cycles just to boot the operating system.

Eliminating the system-simulation speed problem calls for software that allows for quick-turnaround "what-if" analysis. Basically, this implies the need for simulators that provide incremental compilation, and are tightly integrated with the design-entry and analysis environment so that quick viewing, analysis, and tweaking of circuit and signal values are possible. Another way engineers can keep down long simulation times is to model everything at a high level except for the areas they're most worried about. Those problem areas should be modeled in detail. In addition, compiled-logic technology like that used in Mentor Graphics' QuickParts product can help create models that use less memory and execute faster. Efficient use of simulation cycles that run only the most important cycles can also save time. And finally, the proven method of hardware acceleration is becoming a more frequently used simulation option despite its high price tag.

System simulation is often carried out at multiple levels. The level at which an engineer chooses to simulate basically depends on what he or she is looking for in the design. Today's engineer can perform either some or all of the system simulation at a high level of abstraction using a language like VHDL.

Historically, engineers have needed to perform "proof of concept" before they've actually been able to do it, notes Kuhoo Goyal of Dazix. Proving a concept involves levels of abstraction that go beyond the behavioral levels. Therefore, the engineer can verify a concept before any kind of system definition is even accomplished. Dazix, for instance, is one company that offers tools in this architectural realm. ForeSight, a rapid prototyping tool, verifies the system specification before any steps are taken to implement the specifications. Engineers can perform design exploration and design alternatives. And, traversing down the design hierarchy is automated with ForeSight by converting the design specifications into VHDL source code.

The behavioral level is often used to validate system specifications in the form of system blocks. Then, as these blocks are implemented, the engineer can verify a gate-level block's interaction with the other behavioral blocks. Actually, the implementation that the engineer decides

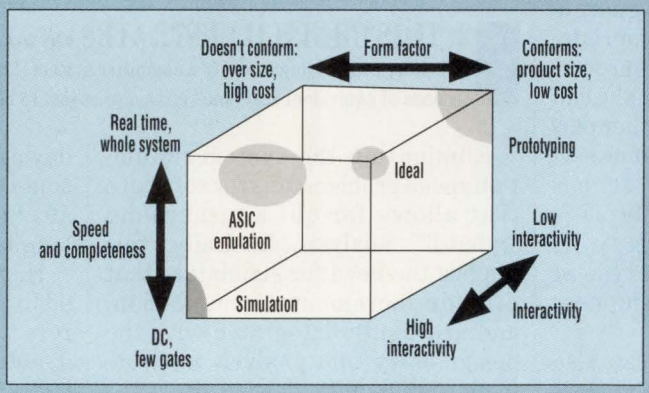
SIMULATION SOLVES ONLY PART OF THE DESIGN-VERIFICATION PROBLEM

Engineers often lose sight of the real requirements for solving a problem when the problem becomes known by its solution. One example of this is using software simulation to solve system design-verification problems. When simulation reaches the limits of it capabilities, there's still a great deal of system-verification work to be done before delivering final products to customers. Therefore, system designers must not depend solely on the capabilities of system simulation to verify designs. If that's the case, they'll pay a stiff penalty in time-to-market, which translates to lost profits and lower customer satisfaction.

Design verification begins during design creation, and continues until the final product is shipped to customers. In the late stages of the development cycle, design verification becomes the primary objective and the primary obstacle to time-to-market goals. Although simulation is a valuable tool during design creation, it has serious limitations when used for verification. It doesn't have enough speed and capacity to handle applications that have software-intensive hardware or need long periods of real-time operation during verification.

The system verification problem can be characterized by a 3D model *(see the figure)*. The speed-and-completeness axis represents the speed of operation and the portion of the system that can be modeled by the verification solution. Speed and completeness are key factors in determining how much real-time operation can be simulated in a reasonable period of time. The form-factor axis represents how well the solution fits the form of the final product's size, cost, power, and so on. The interactivity axis illustrates how easy it is to observe, change, and control the model during design verification.

All simulation is mapped to the lower-left-front corner of the design, and will slowly climb up the y axis toward higher speed and more system representation. Also, little movement will occur along the x axis toward the final product form. It's important to note that the y-axis scale isn't linear. If it were linear, the simulation solution would be just a specification on the model. Today's popular simulation tools can achieve speeds of a few cycles/s, yet most electronic systems operate in the MHz range. This represents a spread of more than six orders-of-magnitude.



Prototyping with ASIC prototype chips occupies the top-right-rear corner where maximum conformity, speed, and completeness are achieved, but where interactivity is at its most restrictive level. Debugging in silicon isn't tenable because engineers can't observe internal operations or make design changes. In spite of this, most design teams don't debug today's systems until well after the first prototype is built and the complete system is integrated with all of its hardware and software. A possible drawback, though, is extended product-delivery schedules.

The nirvana of design-verification solutions occupies the top-right-front corner. There, designers would have the speed, completeness, and form factor of the final product. They would also have the interactivity they need for an effective design-verification environment.

ASIC emulation can move the engineer closer to this nirvana by providing a solution that's further up the y axis than simulation. The spectrum of possibilities opened up by this technology can be referred to as computer-aided prototyping. Computer-aided prototyping combines design translation and optimization software with reprogrammable hardware to create hardware prototypes of ASIC designs. Engineers still have some level of interactivity, but speed of operation is within one or two orders-of-magnitude of real time. Entire systems can be modeled by emulating the ASICs and implementing the rest of the system with off-the-shelf components. In addition, computer-aided prototyping enables early system integration where the boards of the final product may be used as a test bed, and diagnostics, operating system, and applications can be fully verified on the system hardware before ASICs are fabricated in silicon.

System simulation combined with computer-aided prototyping gives designers a good way to verify their products before any silicon is created. Simulation is good for the early stages of design creation when changes are major and frequent. Later on in the design cycle, however, computer-aided prototyping can help integrate the system in hardware while still maintaining interactivity.

Contributed by Stephen Walters, director of marketing for Quickturn Systems Inc., Mountain View, Calif.

on can depend greatly on the behavior of the high-level description. In the final stage of verification, all of the blocks can be simulated together at the lowest level that time permits. David Smith of Analogy points out that "a lot of design is done at the high level, but design verification must be done at the low level."

Designing and simulating at higher levels is becoming more common as standards like VHDL are adopted and as synthesis tools gain the trust of engineers. Even without synthesis, system-level behavioral modeling and simulation are useful for numerous reasons. For example, if done properly, the test vectors verifying the device's behavior at the high level can and should be used in the gate-level verification as stimulus and as expected outputs.

Behavioral simulation, however, shields timing details from the engineer. Although behavioral simulation can have a concept of time, in theory it's mainly used to verify a system's behavior. For instance, behavioral simulation may answer the question of whether the bits toggle to the right values, instead of whether the bits toggle to the right values at the right time.

Compass Design's Terry Strickland agrees with that, adding that "the behavioral level will never eliminate the need for gate-level simulation." That's because the detailed timing information contained in lower-level ASIC models is critical for the standard timing analysis, which is key to system-level success. The required level of detail can come from a model of an ASIC that's had floor planning or has been placed and routed. Accurate timing analysis is needed because today's boards work at such high clock speeds.

Logic simulation can pass over problems just like behavioral simulations. Because logic simulation doesn't delve down into the transistor level, engineers can't see problems in the design caused by, say, ringing and noise.

Timing simulation, in terms of worst-case timing or static timing, is typically used when some implementation detail is defined. It's basically a post-synthesis process, used once the technologies and geometries of the parts are defined. However, timing simulation can also be performed at the data-path levels, prior to synthesis, when timing is implied along with the design's behavior. Timing simulation is always warranted for those engineers designing at the structural level. Manufacturing variations, including timing, power, and voltages, can be thoroughly explored by engineers with in-depth timing simulations.

The number of system-simulation passes that must be done throughout the design cycle depends on both the design and the designer. Factors that influence the amount of simulation passes include: what the engineer is trying to validate; the amount of attention being paid to manufacturing variations as they pertain to timing, temperatures, voltages, and so on; how much trust the engineer has in the results of a simulation run; and the amount of fault coverage that's satisfactory. The decision is really a trade-off, because engineers want to get the product to market quickly. But they also know that the

PROGRAMMABLE INTERCONNECT ADVANCES SYSTEM VERIFICATION

Verifying today's complex systems can be a significant limitation in engineering productivity and time-to-market. Current techniques, such as simulation, have varying degrees of functionality, form factor, and flexibility in interaction. The challenge for the 1990s is to develop new verification approaches that maximize all of these attributes.

Software simulation—the use of software models and test vectors to verify design behavior under conditions specified by the engineer—is undeniably the most flexible electronic-design-automation tool available to system designers for validating concepts. Despite this flexibility, though, simulation doesn't meet all the needs of today's engineers because it's far removed from the physical design.

A good step toward the ultimate solution is a flexible, hardware-based tool. The tool should have unlimited observability and changeability during the development phase of a project, and is a form, fit, and function physical duplicate of the final product. This latter requirement enables the tool to perform at, or near, actual performance; to be shipped to customers for evaluation; and even to be used as a final product in low-volume applications.

Aptix Corp., San Jose, Calif., is following that path with a new programmable-hardware technology. The company recently announced details of its proprietary interconnect architecture and field-programmable interconnect components (FPICs). The Aptix programmable-interconnect technology enables user-configurable component-to-component interconnection. It can interconnect several thousand universal connections per system.

Two field-programmable interconnect components initially use programming elements based on SRAMs and nonvolatile, one-time-programmable memory technologies. Both programming elements are packaged in a proprietary 1024-pin land-grid-array multilayer ceramic package.

The reprogrammable SRAM-based FPIC is aimed at systems requiring dynamic in-system programming. It has over one million transistors, and is processed in 0.8-μm CMOS technology. Programming is done using conventional memory-addressing techniques. The low-impedance, one-time-programmable interconnect version is optimized for higher speed as well as low cost. Programming and configuration software from the company universally interconnects any combination of pins.

more simulation iterations completed indicates the more fault-free the design will probably be.

Deciding on the correct number of system simulation passes actually ends up being a schedule-driven process, meaning that most engineers simulate as much as their development schedules will allow. A good rule of thumb is to perform some sort of simulation at every level of abstraction. After that, engineers should go through as many iterations as possible. In other words, every time a richer implementation detail is reached, the engineer should verify that the functionality matches the previous level of abstraction.

Verifying a diverse system usually involves various simulators, which poses a problem to both engineers and EDA vendors. EDA vendors have a tough job in hand: Making disparate simulators perform a perfect "handshake" isn't a simple task. For example, simulators have different logic-value systems. A simulator manager must map, on the fly, logic values from one simulator to another. There's also the question of how an analog simulator will represent a digital don't-care state. Moreover, each simulator that's used may have a different time wheel, and these must be synchronized.

Other issues that cause problems are how the user partitions a system over several simulators, how activities get scheduled between these simulators, and how the user debugs in a multi-simulation environment. "The compile environment is where the real problems are," notes Bill Fazakerly, chief technical officer of Ikos Systems Inc., Sunnyvale, Calif, "because simulator databases are not compatible." Vendors are trying to ease the problem with simulation backplanes, like those from Teradyne Inc., Santa Clara, Calif., and Mentor Graphics. The general industry consensus, though, is that much work still must be done in this field.

Some engineers who employ more than one simulator for a system actually use the simulators separately on different parts of the design. Then they try to get interaction between the simulators with the stimulus and results, instead of having them interact during the actual simulation run. Simulator interaction is definitely a problem. It's the opinion of David Hardman of Logic Automation that as system simulation becomes more of a common practice, engineers will migrate to simulators that handle a wider range of models, reducing the need for simulators to interact.

In fact, one key to success is to have very few simulators fully performing the system-level simulations. Digital simulators should be multilevel simulators that can simulate anything from the switch level to high behavioral levels. Analog simulators should be able to handle anything from the transistor levels to analog behavioral languages. Some simulators can take both analog and digital inputs. For example, Dazix has a single-engine, mixed-mode simulator that works with analog components and digital behavioral models.

A GOOD RULE OF THUMB IS TO PERFORM SOME SORT OF SIMULATION AT EVERY LEVEL OF ABSTRACTION.

The Contec Microelectronics simulator can handle both analog and digital portions of a design by modeling both portions with analog behavioral models. The analog behavioral representations of the digital components give more detailed time-domain waveforms than does logic simulation. In addition, the models are more than an order-of-magnitude faster than circuit simulation with comparable accuracy.

System-level simulation can have a significant effect on the final stages of a traditional design cycle (the prototype-debug stages) because it moves some of the knowledge usually learned at the breadboarding stage up into the design stage *(see "Programmable interconnect advances system verification," p. 59).* This results in a better prototype than if it had been built without any simulation. And, employing design-for-test (DFT) methodologies, fault simulations, and automatic-test-pattern-generation (ATPG) tools can help ensure smoother production runs. Another benefit is that simulation supplies engineers with test vectors for prototype stimulus, which eliminates a lengthy process in that verification stage. Without the simulation vectors, engineers are often stymied as to how to stimulate their prototype boards.

Despite the benefits, true system-level simulation is rarely performed today. System design in the computer and telecommunications industry rely heavily on simulation because time-to-market is such a critical factor for their success. Other industries, however, require much less simulation to be competitive.

Although the system-simulation process is riddled with problems, Terry Strickland of Compass Design Automation notes that "the people who need to do it have built their own systems with much pain and suffering." There's lots of work involved with integrating software tools. Strickland explains that Compass Design's ASIC Navigator product simplifies this task somewhat by automatically generating the ASIC information needed by a system-level tool. In general, however, there's simply no elegant way of tying everything together.

Old practices of trusting a prototype in a lab versus trusting an automation tool still prevail. There's also a lack of in-depth expertise in using existing automation tools for tasks as big as system-level simulation. Norm Kelly, vice president of engineering for Logic Modeling Systems Inc., Milpitas, Calif., does indeed feel that culture and knowledge are two barriers blocking the road to system-

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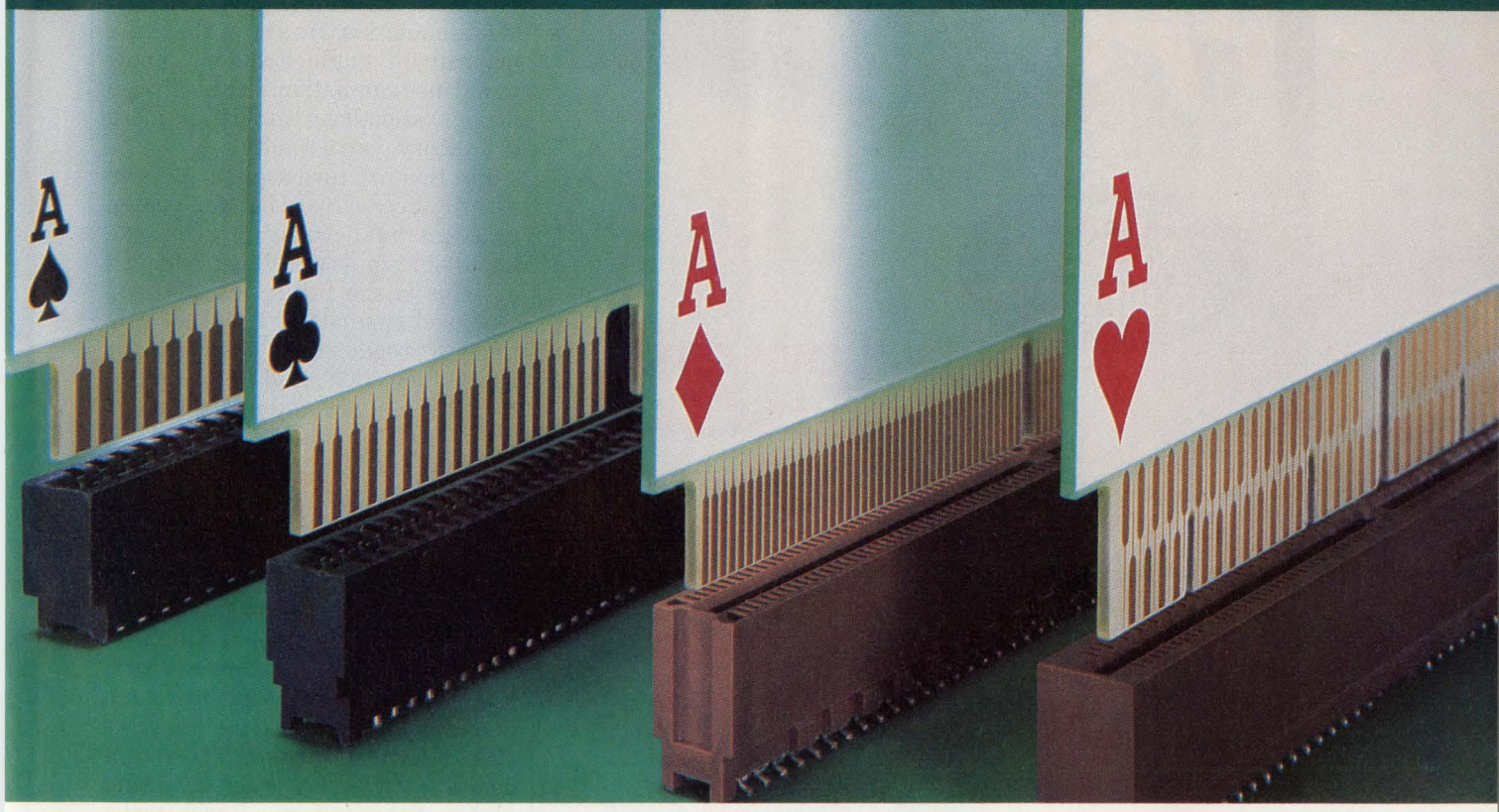

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level simulation. He states that "the majority of engineers don't know how to use simulation." These things make system-level simulation more of a theory than a reality.

But this will turn around, not necessarily because of changed design practices, but because it will become impossible to design these complex systems in the future without system-level simulation. As users continue to broaden their knowledge of automation tools, and as mandates from the military require designs be done using languages like VHDL, system-level simulations will become more common.

In the future, design teams will include the simulation of software in their system-level simulation. Few, if any, engineers can achieve that today. For example, a limited number of processor design teams perform low-level software (assembly or microcode) simulation in the realm of system-level simulation. Those that do use software in system-level simulation have performed such tasks as booting Unix.

Design teams at Intergraph Corp., Huntsville, Ala., have simulated the Clipper, a CPU for the company's workstations, running limited amounts of software. Hardware acceleration is being used to execute Unix instructions, and in turn to boot Unix. However, most design teams today have separate hardware and software development groups that perform actual hardware and software integration at the breadboard levels, after every piece is developed.

Simulating hardware running software is a high growth area for automation. EDA and CASE vendors need to provide more solid and integrated automated solutions. The abilities within VHDL, for example, that allow for text I/O, will let designers read ROM instructions from a file, emulating the behavior of the CPU processing actual microcode during "real" operations.□

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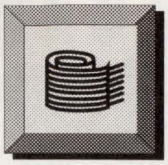

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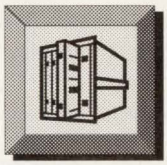

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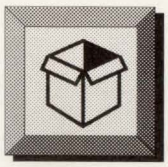

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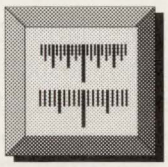

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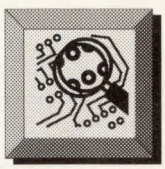

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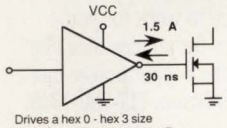

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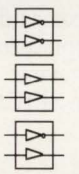
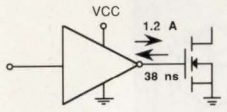
- Available in surface mount packages

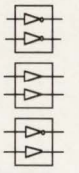


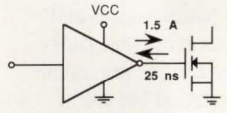


Drives a hex 0 - hex 3 size MOSFET; 400 pF to 3000 pF.

MIC1426/7/8 (Low Cost)

- Low cost predriver
- 38 nS into 1000 pF
- 4.75 V to 16 V supply
- 1.2 A peak output
- 8 Ω output impedance
- Available in surface mount packages

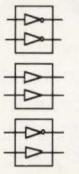


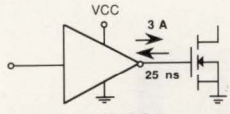


Drives a hex 0 - hex 3 size MOSFET; 400 pF to 3000 pF.

MIC4426/7/8 (Protected)

- Latch-up protected
- 25 nS into 1000 pF
- 4.5 V to 18 V supply
- 1.5 A peak output
- 7 Ω output impedance
- Withstands 5 V negative swing
- Available in surface mount and high temperature packages

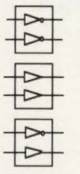


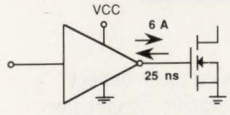


Drives a hex 4 - hex 5 size MOSFET; 6000 pF to 12000 pF.

MIC4423/4/5 (High Current)

- Latch-up protected
- 25 nS into 1800 pF
- 4.5 V to 18 V supply
- 3 A peak output
- 3.5 Ω output impedance
- Withstands 5 V negative swing
- Available in surface mount packages

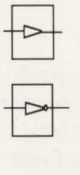


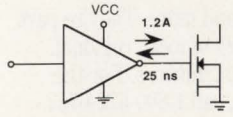


Drives a hex 6 - hex 7 size MOSFET ; 15000 pFto 16000 pF

MIC4420/4429 (Singles)

- Latch-up protected
- 25 nS into 10,000 pF
- 4.5 V to 18 V supply
- 6 A peak output
- 2.5 Ω output impedance
- Withstands 5 V negative swing
- Available in surface mount packages

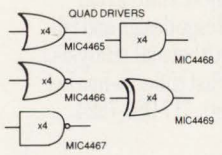




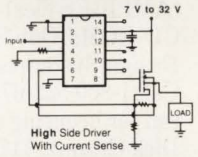
Drives a hex 0 - hex 3 size MOSFET; 400 pF to 3000 pF

MIC4465/6/7/8/9 (Quad)

- Latch-up protected
- 25 nS into 470 pF
- 4.5 V to 18 V supply
- 1.2 A peak output
- Available in surface mount packages
- Five logic choices

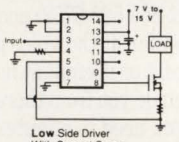


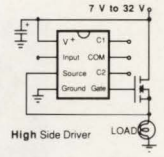
High Side, Protected MOSFET Drivers



MIC5010

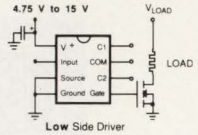
- Full Featured predriver
- Optional speed up caps
- 7 V to 32 V supply
- Internal charge pump
- 60 µS into 1 nF
- Over current sensing
- Fault flag output
- Surface mount packages
- Dynamic sensing threshold

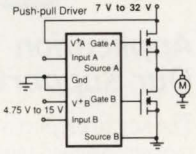




MIC5011

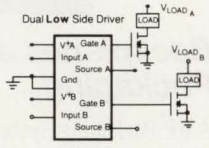
- Minimum parts count
- Optional speed up caps
- 4.75 V to 32 V supply
- Internal charge pump
- 60 µS into 1 nF
- Surface mount packages

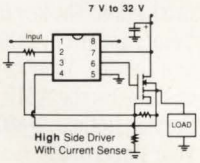




MIC5012

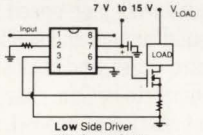
- Dual predriver
- Provides high and low side
- 4.75 V to 32 V supply
- Internal charge pump
- 60 µS into 1 nF
- Surface mount packages





MIC5013

- Over current sensing
- 7 V to 32 V supply
- Fault flag output
- Internal charge pump
- 60 µS into 1 nF
- Surface mount packages
- Dynamic sensing threshold



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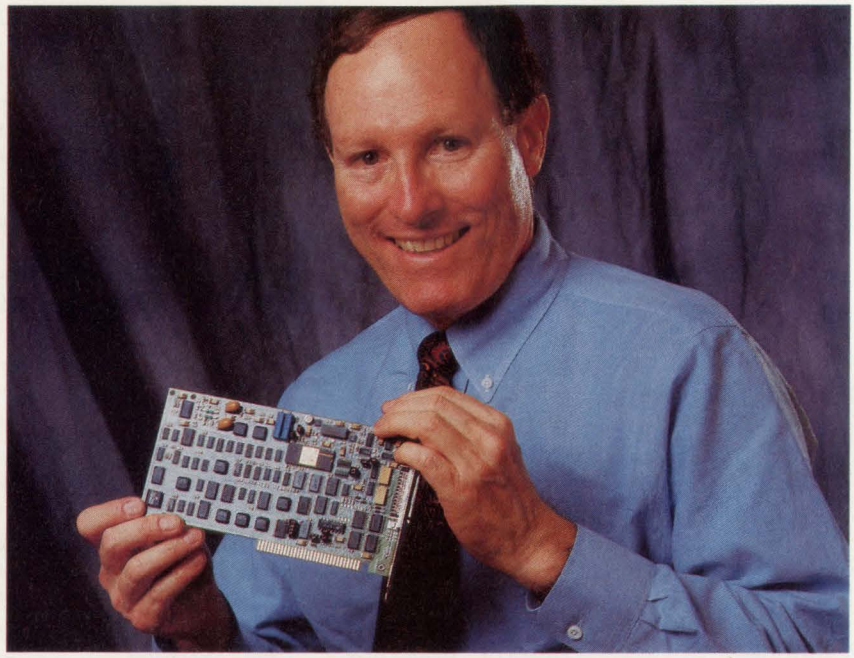

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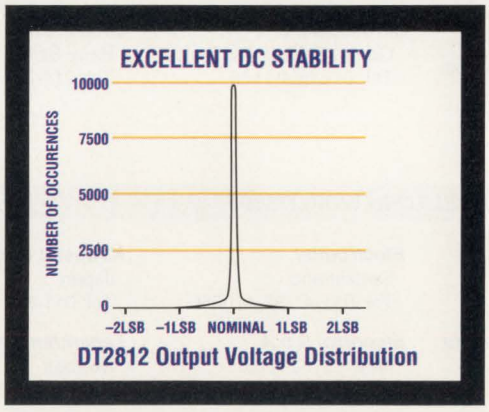

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CORRECTING POWER FACTOR AT THE INPUT TO SWITCHERS CAN BE FAR MORE EFFECTIVE THAN FIGHTING TO BOOST THEIR EFFICIENCY.

SOLVE SWITCHER PROBLEMS WITH POWER-FACTOR CORRECTION

PATRICK L. HUNTER
Unipower Corp.,
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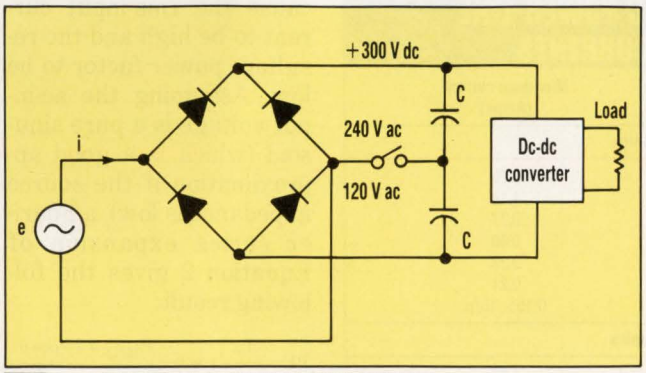
(305) 974-2442.

When specifying power supplies, system engineers always focus on the supplies' output end: voltages, currents, regulation, filtering, and output protection. Little concern is given to the input end, except perhaps to meet electromagnetic-interference (EMI) standards. With higher-power, off-line switching power supplies in wide use, new questions have arisen concerning the input end and its effect on the ac-power line and other electronic systems in the local environment. This article explores the subject of power factor at the input to switching power supplies, the problems it causes, and solutions to those problems.

Power factor is a well-known term in standard ac-circuit theory. It refers to the effect of a reactive load on an ac-power system. In a linear ac circuit with a purely resistive load, the ac current is in phase with the ac voltage, and the average power consumed by the load is the product of the rms (root mean square) voltage and rms current. For a linear load combining resistance and reactance, the current lags the voltage for an inductive reactance and leads the voltage for a capacitive reactance. The product of rms voltage and rms current gives a quantity called "apparent power":

$$\text{Apparent power} = P_A = E_{rms} \times I_{rms} \quad (1)$$



1. AN OFF-LINE SWITCHING power supply's input circuit has a full-bridge rectifier and storage capacitor. The circuit is a voltage doubler for 120-V ac input.

This quantity, however, isn't the average or "real" power,consumed by the resistive part of the load.

Real power is calculated as the average of the instantaneous product of voltage and current taken point by point over a full period of the source waveform:

$$\text{Real power} = P_R = \frac{1}{T}\int_0^T (e \times i)\, dt \quad (2)$$

and for a linear circuit:

$$P_R = E_{rms} \times I_{rms} \times \cos\theta = P_A \times \cos\theta \quad (3)$$

where θ is the phase angle between the sinusoidal voltage and current waveforms.

Power factor is a measure of how close apparent power is to real power, defined by the ratio:

POWER FACTOR AND SWITCHING POWER SUPPLIES

TABLE 1: EXAMPLES OF MAXIMUM POWER AVAILABLE FROM STANDARD AC OUTLETS

	15-A circuit			20-A circuit		
	1	2	3	1	2	3
VA available (UL)	1440	1440	1440	1920	1920	1920
Efficiency of supply	75%	90%	75%	75%	90%	75%
Efficiency of PFC	-	-	97%	-	-	97%
Total efficiency	75%	90%	73%	75%	90%	73%
Power factor	0.65	0.65	0.95	0.65	0.65	0.95
Maximum load power	702 W	842 W	995 W	936 W	1123 W	1327 W

$$\text{Power factor} = PF = \frac{P_R}{P_A} = \frac{\text{Real power}}{\text{Apparent power}} \quad (4)$$

$$= \frac{P_R}{E_{RMS} \times I_{RMS}}$$

$$= \cos\theta \text{ (for a linear load)}$$

If the load in an ac circuit is purely resistive, then apparent power and real power are identical, and power factor is its maximum value of 1.

A common problem that plagues ac-power systems is caused by a factory operating electric motors. The inductive component of the motors causes the ac current to lag the voltage, resulting in a low power factor. Assuming the load elements are linear, power factor can be corrected to near unity by connecting a bank of capacitors across the ac-power line at the factory.

Switching power supplies present a problem to ac-power systems that's quite different from motor loads. Here, the term "switching power supply" means an off-line switcher with an input rectifier and filter capacitor connected directly to the ac-power line, without an intervening transformer.

The input circuit of a switching power supply with the commonly used full-wave bridge rectifier and voltage-doubler circuit is shown *(Fig. 1)*. This circuit produces an average dc-output voltage of about 300 V with a 120-Hz ripple-voltage component. The switch, or jumper wire, lets the power supply operate from either 120- or 240-V ac nominal line voltage, with the circuit acting as a voltage doubler when operating from a 120-V ac input.

A switching power supply presents a nonlinear load to the ac-power line—one in which the input current isn't a sinusoid but rather a series of pulses *(Fig. 2)*. The current pulse lasts for a small portion of each half-period of the voltage, is non-symmetrical in shape, and may either slightly lead or lag the ac-input voltage depending on the impedance of the ac source. Also, the input-voltage waveform may be significantly clipped near the peaks, depending on the amount of ac-source impedance that is present.

The current pulse occurs because the filter capacitors remain charged to nearly the peak value of the ac-input voltage. During most of each half-period of input voltage, the rectifier diodes remain back-biased and no current flows. However, because the capacitors partly discharge during each half period, the input voltage exceeds the capacitor voltage for a short time near the peak of the voltage waveform.

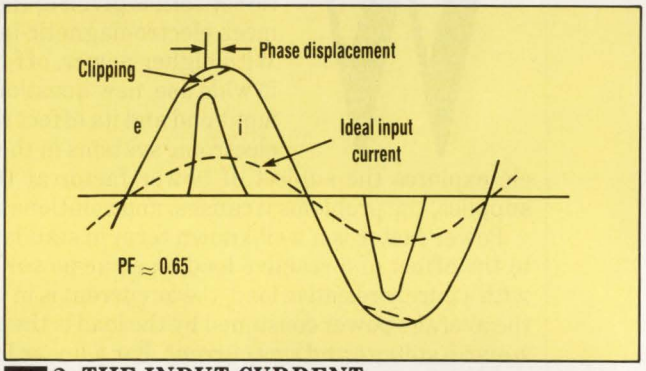
As the input voltage goes higher than the capacitor voltage, current begins to flow into the capacitor. After the capacitor is charged to near the peak value of the voltage and the voltage begins to decrease, the current falls back to zero.

Once the input-current waveform is examined, it's easy to understand the power-factor problem. The current pulse has a high peak value and is extremely distorted with respect to a sinusoidal waveform. It has high levels of harmonic currents, and a fundamental component that leads or lags the input voltage depending on source impedance.

These characteristics cause the rms-input current to be high and the resultant power factor to be low. Assuming the ac-input voltage is a pure sinusoid (which is a good approximation if the source impedance is low), a Fourier series expansion of Equation 2 gives the following result:

$$PF = \frac{I_F}{I_{RMS}} \cos\theta = \frac{E_{RMS} \times I_F \cos\theta}{E_{RMS} \times I_{RMS}}$$

$$= \frac{P_R}{P_A} \quad (5)$$



2. THE INPUT CURRENT of a switching power supply is a non-symmetrical pulse that occurs near the peak of the ac voltage. This pulse can cause clipping of the voltage waveform.

TABLE 2: IEC CLASS-A LIMITS ON 220/240-V AC POWER-LINE HARMONIC CURRENTS

Harmonic order (n)	Maximum current (Amps)
Odd harmonics	
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
$15 \le n \le 39$	$0.15 \times 15/n$
Even harmonics	
2	1.08
4	0.43
6	0.30
$8 \le n \le 40$	$0.23 \times 8/n$

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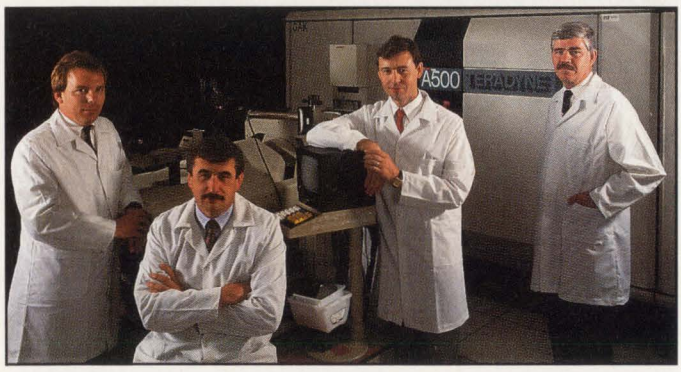

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POWER FACTOR AND SWITCHING POWER SUPPLIES

where I_F is the rms value of the fundamental frequency component of the input current, I_{rms} is the rms value of the total input current, and θ is the phase angle of displacement between the fundamental frequency component and the source voltage. I_{rms} is the square root of the sum of the squares of the fundamental plus all harmonic components of the input-current waveform.

Equation 5 states the power factor in terms of a distortion factor, I_F/I_{rms}, and a phase-angle factor, cos θ. The phase angle is generally small, so the dominant factor in switching power supplies is waveform distortion. If the source voltage is a near-perfect sinusoid, then the following statement is true:

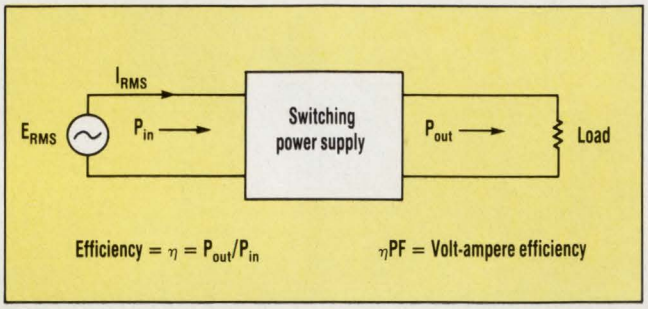
Only the fundamental component of input current contributes to the real (average) input power; the other harmonic components merely increase the magnitude of rms-input current and lower the power factor.

Typical Input Currents

To appreciate actual values of current for a typical switching power supply, consider a supply that operates from a 120-V ac source and delivers 1000 W to its load. The efficiency of such a supply is typically 75% and the measured power factor about 0.65. The rms-input current is about 17 A and the peak input current about 46 A.

Compare these current levels to those of an idealized power supply that doesn't distort the input current but has a purely resistive input with the same 75% efficiency. In this case, the power factor is 1.0, the sinusoidal input current is 11.1 A, and the peak input current is only 15.7 A. In the real-world example, rms-input current is 53% higher and peak-input current is 193% higher than the ideal.

It should be noted here that in making power-factor measurements, the current must be measured with a true-rms ammeter and the input power with an average-reading wattmeter.



3. VOLT-AMPERE efficiency, ηPF, is the figure of merit that determines the input current for a switching power supply.

An important figure of merit for switching power supplies is "volt-ampere (VA) efficiency." To understand this term, it helps to look at a power-supply diagram *(Fig. 3)*. From the figure:

$$PF = \frac{P_R}{P_A} = \frac{P_{IN}}{E_{RMS} \times I_{RMS}} = \frac{P_{OUT}/\eta}{E_{RMS} \times I_{RMS}} \quad (6)$$

where η is the efficiency of the power supply. Rearranging terms gives:

$$I_{RMS} = \frac{P_{OUT}}{[\eta PF]\, E_{RMS}} \quad (7)$$

The product of efficiency and power factor (ηPF), called VA efficiency, is the figure of merit that determines input current. Maximizing a power supply's ηPF minimizes input current.

In the previously discussed example of a 1000-W power supply, the efficiency is 75% and power factor is 0.65. Therefore:

$$\text{VA efficiency} = PF = 0.75 \times 0.65 = 0.4875 \quad (8)$$

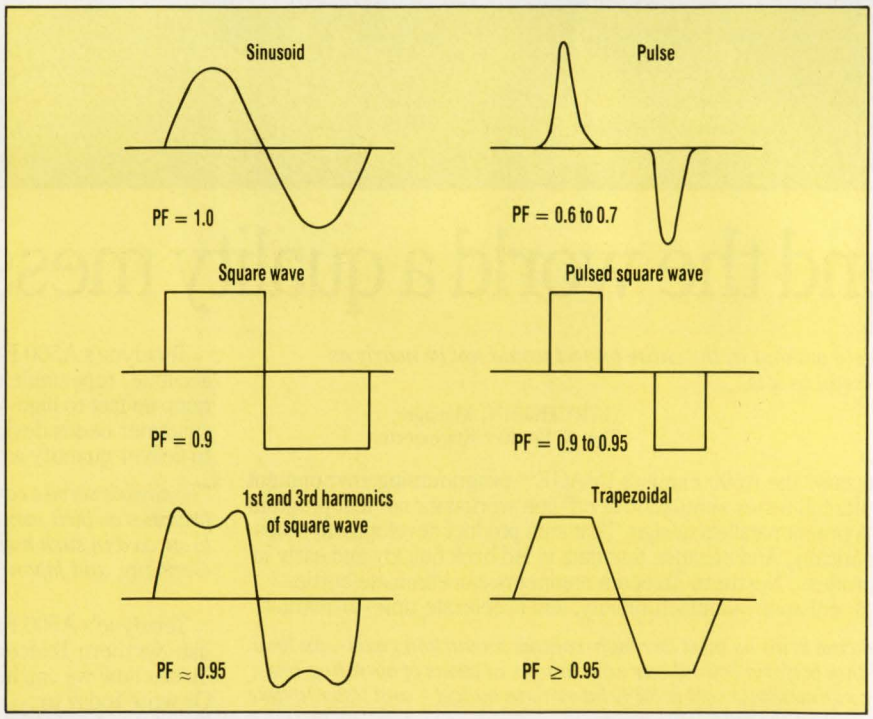
and

$$I_{RMS} = \frac{1000}{0.4875 \times 120} = 17.1 \text{ A} \quad (9)$$

which is the value that is given in the example.

Why PFC Is Needed

Safety-regulatory agencies, such as Underwriters Laboratories (UL), have safety limits on current levels for standard ac-service outlets. For standard 120-V ac, 15- and 20-A outlets, the rated load must be main-



4. MANY INPUT-CURRENT waveshapes yield a relatively high power factor, but the shape must be close to a sinusoid to also attain low harmonic currents.

POWER FACTOR AND SWITCHING POWER SUPPLIES

tained at 80% or less of the source rated current. This means maximum currents of 12 and 16 A, respectively, and maximum apparent power ($E_{rms} \times I_{rms}$) of 1440 and 1920 VA, respectively.

In the example of the 1000-W power supply in Equation 9, the input current was 17.1 A, giving an apparent power of 2052 VA. This exceeds the UL standard for both 15- and 20-A-service outlets.

Equation 7 can be used to solve the maximum power output of a switching power supply operating within UL limits from standard 15- or 20-A circuits. Assuming 75% efficiency and 0.65 power factor, the power available is 702 and 936 W, respectively.

To increase the output power from standard ac outlets, it's necessary to correct the power factor in a switching power supply. This substantially reduces peak and rms-input current, which makes it possible to achieve a much higher output power. Power-factor correction (PFC) is a much more effective approach than trying to boost efficiency. Component limitations make efficiencies of more than 75% impractical. On the other hand, boosting power factor to 0.95 and higher is a fairly simple task, resulting in 995 and 1327 W of output power, respectively, from 15- and 20-A outlets.

The various efficiencies and power factors of switching power supplies produce diverse results in terms of the amount of power that can be drawn from standard outlets *(Table 1)*. When a PFC circuit is added, its efficiency must also be considered as part of the total power-supply efficiency.

The low power factor caused by high rms-input currents in switching power supplies gives rise to a number of serious problems in electronic equipment. For one, equipment fuses and circuit breakers must be increased in size. Costly EMI filters must have higher current ratings. The distorted input-current waveform, which may cause interference with other equipment, may have to be further filtered to reduce harmonic frequencies. If the equipment is operated from an uninterruptible power supply (UPS) or standby generator, the size and cost of these items will increase. And finally, the input currents can cause problems in three-phase power systems.

TABLE 3: PASSIVE POWER-FACTOR CORRECTION

Advantages	Disadvantages
• Simple and rugged	• Large size and weight
• High MTBF	• High PF difficult
• Low EMI	• Frequency-dependent
	• Load-dependent
	• Narrow line-voltage range
	• Dual-voltage ranges are difficult to implement
	• May have large, circulating currents

TABLE 4: ACTIVE HIGH-FREQUENCY POWER-FACTOR CORRECTION

Advantages	Disadvantages
• High PF (0.97 to 0.99)	• Complex circuitry
• Very low harmonic distortion	• Double power conversion
• Wide line-voltage range (90 to 264 V ac)	• Reduced MTBF
	• Higher cost
• Wide frequency range	• Highest EMI
• Regulated high-voltage bus	• May require synchronization of converters
• Small magnetics	• Lower efficiency
• Holdup time constant with input-voltage change	

TABLE 5: ACTIVE LOW-FREQUENCY POWER-FACTOR CORRECTION

Advantages	Disadvantages
• High efficiency	• Holdup time changes with line voltage
• Simple circuitry	• Dc bus not regulated
• High MTBF	• Larger and heavier than HF method
• High PF (0.96-0.98)	
• Low EMI	
• Low harmonic distortion	
• Wide frequency range	
• Lowest cost	
• Moderate input-voltage range (90 to 132 V ac or 180 to 264 V ac)	

The International Electrotechnical Commission (IEC) has adopted standard IEC 555-2, which limits harmonic currents for equipment that operates on 220- or 240-V ac nominal line voltages. This standard is scheduled to become effective in Europe in 1992. Similar regulations may soon follow in the U.S., Canada, and other parts of the world. It's certain that emphasis on reducing harmonic currents will be a wave of the future.

Under IEC 555-2, a switching power supply with PFC would have to meet Class A limits on harmonic content, for which the third harmonic must be less than 2.3 A *(Table 2)*. A power supply without PFC that's within special waveshape requirements falls into Class D, which has a limit on the third harmonic of 1.08 A. These limits seriously curtail the amount of power that a switching power supply can deliver without PFC.

THREE-PHASE PROBLEMS

Switching power supplies with uncorrected power factor can cause difficult problems in three-phase power systems. For example, in a four-wire wye-connected system, loads throughout a building are connected from each phase to the neutral line. Under ideal conditions with each phase's load current sinusoidal, in phase, and equal, the currents in the neutral line cancel to give zero current. Even with a different load on each phase there is partial cancellation of the neutral line currents.

If, however, switching power supplies are on each phase, the distorted non-sinusoidal input currents don't cancel each other, but rather combine into a larger current. The third-harmonic currents generated in each phase load combine directly

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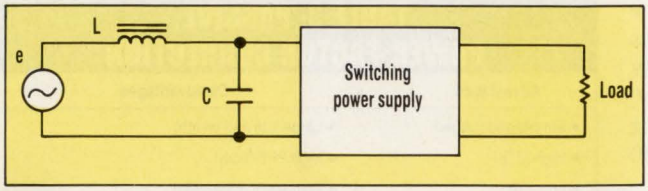
in-phase in the neutral wire. Uncorrected switching power supplies, therefore, have very high third-harmonic currents.

The result can be large currents in the neutral line that far exceed currents in the phase lines and therefore surpass the current rating in the neutral wire. Because the neutral line has no circuit protection, there may be overheating that can cause damage to the wire.

In such cases, circuit breakers or other protection devices on the phase lines fail to protect the wiring, sometimes setting off fires. PFC is a solution to this nasty problem in three-phase systems.



5. A PASSIVE power-factor-correction circuit can be a simple LC filter when the correction must be performed external to the power supply.

PFC METHODS

PFC in a switching power supply is accomplished by reshaping the distorted input-current waveform to approximate a sinusoidal current that's in-phase with the input voltage. The important question remains, though, of how good the reshaping must be to achieve a power factor of, say, 0.95 or higher.

Some indication of what must be done is shown in several potential current-waveform shapes with corresponding typical power factors *(Fig. 4)*. High power factors can be achieved by current waveforms that aren't very sinusoidal in shape. But undesirable harmonic currents is another factor to consider, and some of these waveforms are high in harmonic content.

There are several effective techniques for achieving a good input-current waveform with low distortion. Because the supply's output is smooth dc, the PFC circuit must store a minimum amount of energy to correct for instantaneous differences between input and output power functions.

The minimum amount of stored energy will depend upon the input-current waveform, the line frequency, and the load power, and will be independent of the intermediate switching frequencies that control the current waveform and process the power throughout.

PFC can be designed as a separate box between the ac-power source and the power supply or as an integral part of the input rectification and filtering process. The energy storage needed for PFC already exists in the high-voltage capacitor of the switching power supply. By coordinating the input-current waveshaping with rectification and energy storage, the highest performance is achieved at the lowest cost.

Three of the most-used techniques for PFC are passive correction, active high-frequency correction, and active low-frequency correction. These techniques are discussed in detail later on. Only single-phase-input power supplies are considered in this article.

As power levels move up to the multi-kilowatt range, three-phase systems become important, and PFC unique to these systems must be used. Those techniques, though, aren't discussed in this article.

PASSIVE PFC

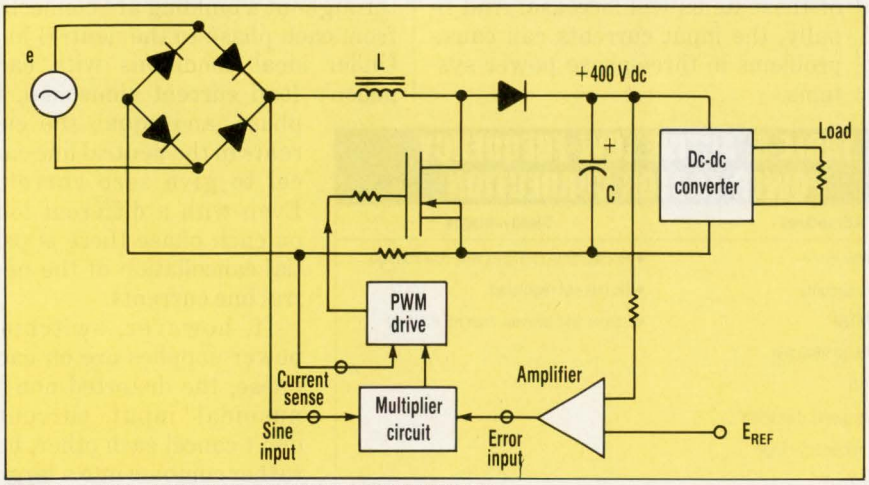
Passive PFC techniques shape the input-current wave by using a passive input filter consisting of inductors and capacitors. This method is effective as a front-end box, where the system already has an uncorrected power supply, and the engineer must implement PFC without changing the power supply *(Fig. 5)*.

Because it operates at line frequencies of 50 or 60 Hz, the passive filter requires relatively large inductors and capacitors to reduce the low-frequency harmonic currents. To produce power factors of 0.90 or greater, sophisticated filters are needed to properly smooth and attenuate harmonics.

Generally, such filters use resonant-pass or -trap circuits sensitive to both frequency and load. It's difficult to achieve power factors of 0.95 or higher with passive filters. Another problem is very large currents that may circulate in the filter.

Nevertheless, the passive filter can be an effective PFC solution in cases where line frequency, line voltage, and load are relatively constant. The advantages and disadvantages are summarized *(Table 3)*.

As discussed, active PFC is a better solution when compared with the passive method. The circuit is an integral part of the power-supply's



6. THE ACTIVE HIGH-FREQUENCY power-factor-correction circuit forces the input current to be sinusoidal. It also regulates the voltage going to the dc-dc-converter part of the power supply. Power factors from 0.97 to 0.99 are achieved.

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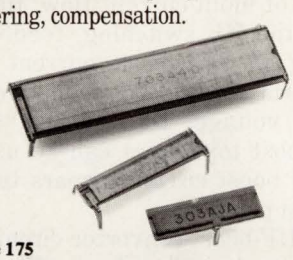

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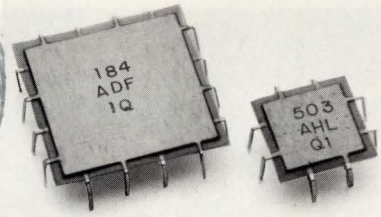
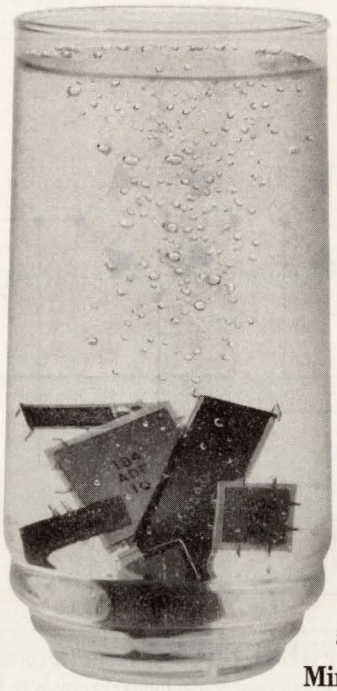


Circle 176



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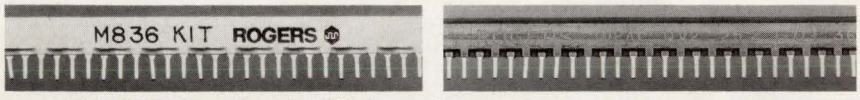

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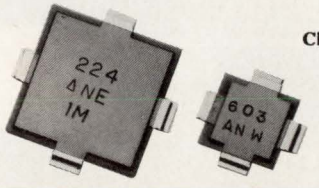
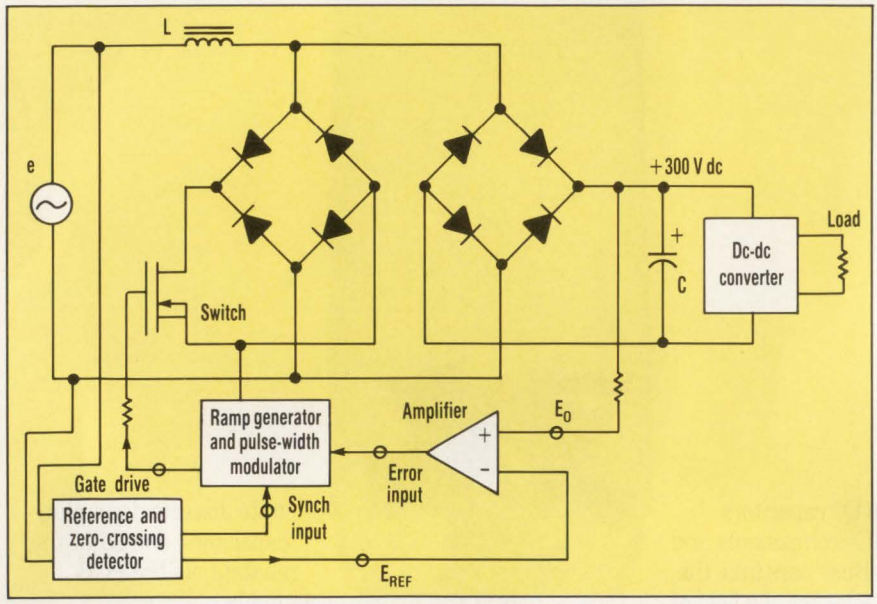


POWER FACTOR AND SWITCHING POWER SUPPLIES



7. THE ACTIVE LOW-FREQUENCY power-factor-correction circuit uses a switched inductor to produce a pseudo-sinusoidal input current with low harmonic currents. A pulse-width modulator controls the operation of the MOSFET switch. Power factors between 0.96 and 0.98 are realized.

front-end, performs much better, and is significantly smaller and lighter. Active high-frequency (HF) correction circuits typically operate at switching frequencies of 20 kHz to 100 kHz, far higher than the line frequency, to permit a large reduction in the size and cost of filter elements. HF-circuit functions include switch control of input-current flow, filtering of the HF switching, feedback sensing of the source current for waveform control, and feedback control of voltage. Buck, boost, and buck-boost topologies can be used, but the boost circuit appears to be the most popular.

The HF-boost-converter circuit is shown in simplified form *(Fig. 6)*. The rectified sinusoidal input voltage goes to a multiplier circuit, providing a current reference to the multiplier and a feed-forward signal proportional to the rms value of the line voltage. The boost converter's

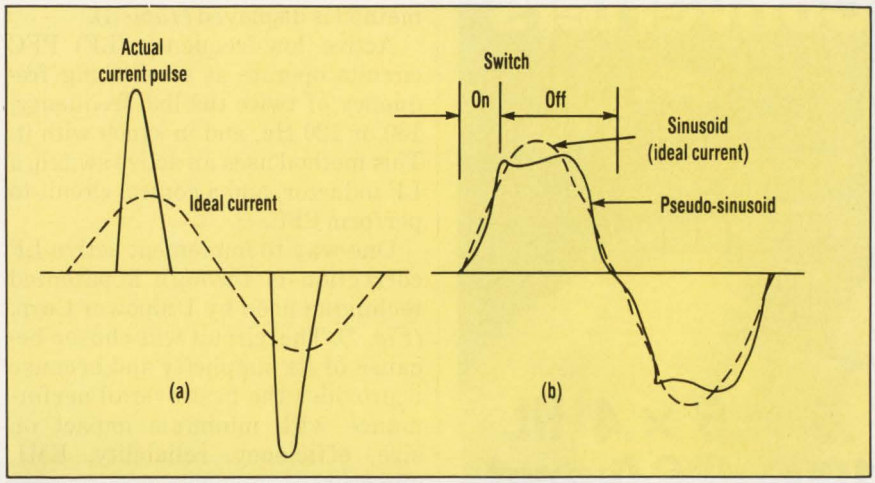
POWER FACTOR AND SWITCHING POWER SUPPLIES

filtered dc-output voltage is compared to a reference voltage E_{REF} and amplified.

The error signal is applied to the input of the multiplier. The multiplier's output follows the shape of the input voltage, with an average value inversely proportional to the rms value of the ac-input voltage. This signal is compared to the current-sense signal in the pulse-width-modulator drive circuit to shape the current waveform from the source and maintain a constant output of about 400 V dc.

This PFC circuit can be implemented using available ICs. The power supply, however, must process the total power twice—first through the HF-boost converter and then through the HF dc-dc converter. This serial power processing adds to complexity, reduces efficiency and mean time between failure (MTBF), and increases both size and cost. But the technique achieves a power factor of 0.97 to 0.99 with very low harmonic distortion, produces a regulated 400-V dc bus, and provides operation over a wide input-voltage range of 90 to 264 V ac.

A summary of the advantages and disadvantages of the active-HF



8. BOTH THE UNCORRECTED input current to a switching power supply (a) and the pseudo-sinusoidal input current produced by active LF power-factor correction (b) are illustrated.

POWER FACTOR AND SWITCHING POWER SUPPLIES

method is displayed *(Table 4)*.

Active low-frequency (LF) PFC circuits operate at a switching frequency of twice the line frequency, 100 or 120 Hz, and in synch with it. This method uses an active switch, a LF inductor, and a control circuit to perform PFC.

One way to implement active-LF correction is through a patented technique used by Unipower Corp. *(Fig. 7)*. This circuit was chosen because of its simplicity and because it provides the best overall performance with minimum impact on size, efficiency, reliability, EMI, and cost.

The MOSFET-switch circuit is driven into conduction at the zero crossing of the ac-source voltage, and current builds up in the inductor, L, from the ac source. At a controlled time after the zero crossing (typically 1 to 2 ms), the switch is turned off and the source current through L transfers to the output rectifier and filter circuit. The MOSFET switch is driven by a pulse-width-modulation (PWM) circuit that compares an error-feedback signal to a ramp signal that is synchronized by a zero-crossing signal.

The reference for the error amplifier is proportional to the rms value of the ac-line voltage, and the output voltage (about 300 V dc) is load-regulated by adjusting the conduction time of the MOSFET switch. The input-current waveform is enhanced by maintaining an optimum relationship between the magnitude of the ac-input voltage and the dc-output voltage.

The result is a pseudo-sinusoidal current waveform which gives a high power factor of 0.96 to 0.98 with low harmonic currents *(Fig. 8)*.

Power factor at rated load is relatively constant over line voltage ranges of 90 to 132 V ac or 180 to 264 V ac. These input ranges can be made switch-selectable, or autoranging techniques can be used to provide automatic switching.

This method is highly efficient, with lower total losses than the HF method. Its low component count also results in high MTBF. A summary of the advantages and disadvantages of the active LF method is given *(Table 5)*.

Other Considerations

While PFC certainly solves a difficult problem at the input end of a switching power supply, the systems engineer must also consider a few other items: PFC moderately increases the size and weight of the power supply, increases its cost by some 10 to 20%, and results in a slightly lower total efficiency because of losses in the PFC circuit. There's also a slightly lower MTBF caused by additional circuit complexity and components.

Moreover, in the case of three-phase power systems, a simple implementation of active PFC that maintains the current balance between phases is difficult to achieve. These obstacles are minor ones, however, when considering that in most applications, PFC solves a major problem associated with the ac-power source.

PFC will be used in switching power supplies more frequently in the future as equipment users and manufacturers better understand its benefits. Most interest today appears in the 1000-to-2000-W power range, because that's where benefits in using standard ac-power outlets are greatest. With the IEC 555-2 standard on the verge of being implemented in Europe for 220- and 240-V ac circuits, PFC takes on increasing importance. Undoubtedly, U.S. and Canadian regulations on harmonic line currents will be put in place. There will also be future interest in PFC at lower power levels as the negative effects of multiple smaller power supplies on ac-power lines is felt.□

Patrick L. Hunter, a founder of Unipower, is vice president and technical director. He holds BS and MS degrees in electrical engineering from Ohio State University, Columbus.

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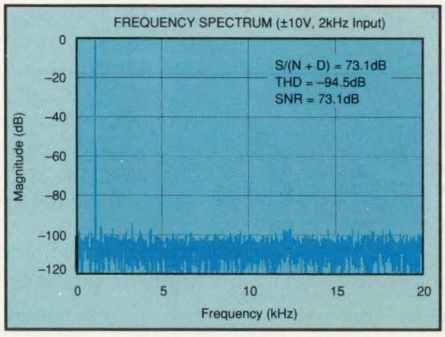

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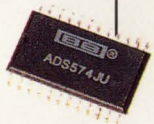

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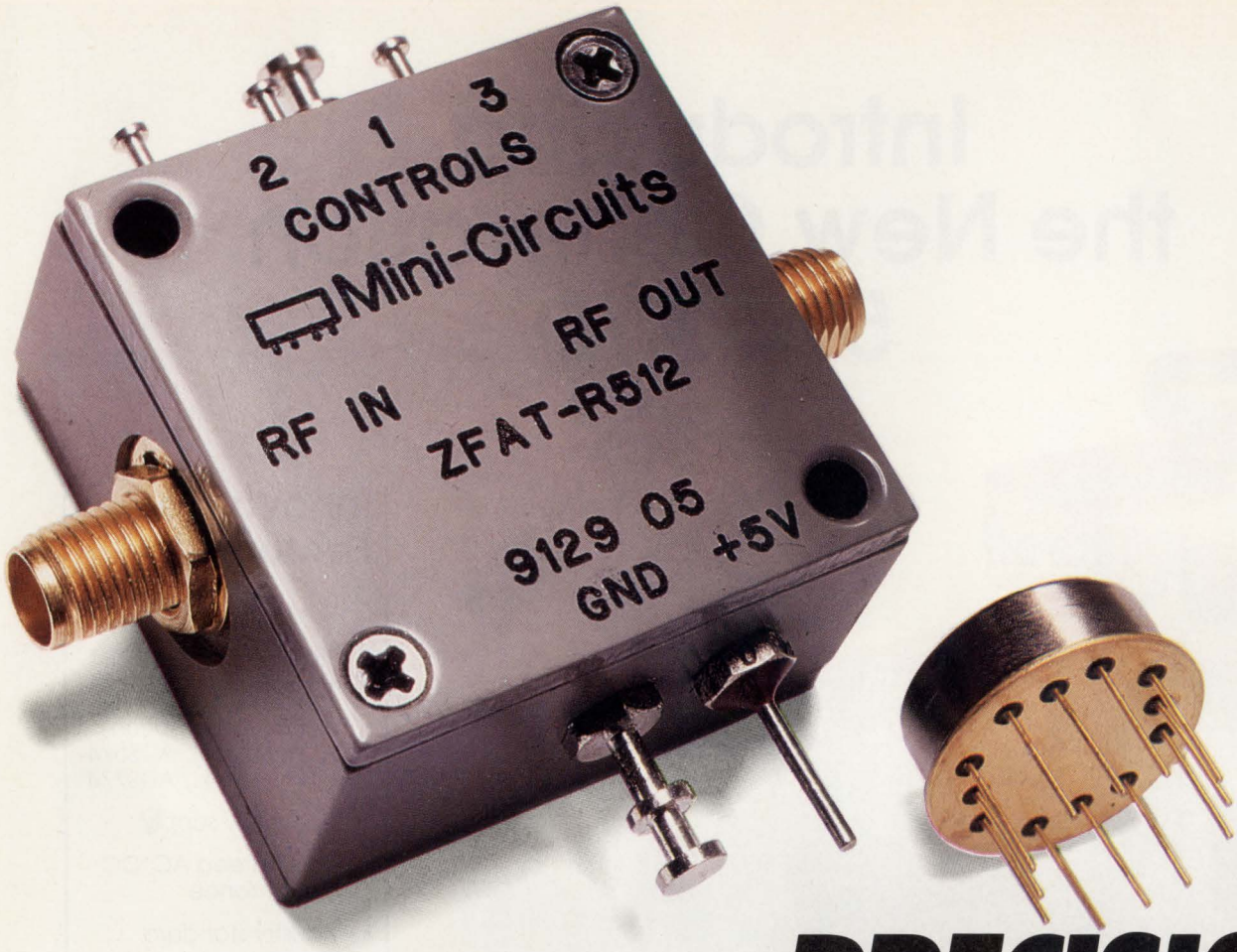

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CIRCLE

521

CABLE TESTER IS EXPANDABLE

NOOR SINGH KHALSA
EG&G Inc., P.O. Box 809,
Los Alamos, NM 87544; (505) 667-0213.

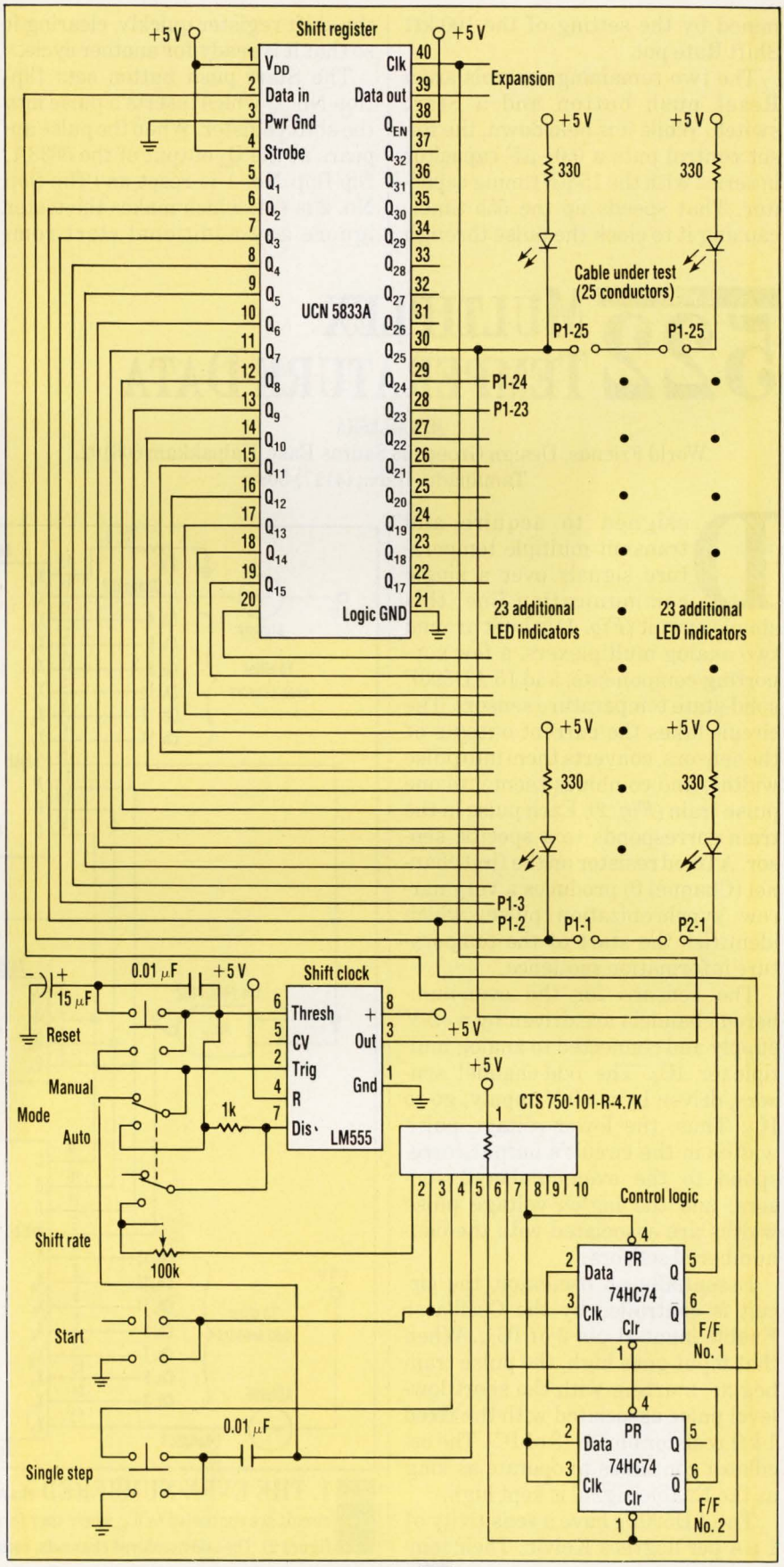
Cables can have almost any number of conductors. It is handy, therefore, to have a cable tester that can be readily expanded as necessary. Because of the 32-bit shift register at its heart, the basic tester can handle up to 32 conductors *(see the figure)*. However, the Data-out line of the UCN 5833A shift register allows additional UCN 5833As to be cascaded, so the tester can be expanded in 32-conductor increments.

The tester operates by propagating a single pulse through the shift register, turning on the LEDs in a LED array one at a time. One end of the cable under test is connected to the shift register outputs and their associated LEDs. The other end of the cable is connected to a second LED array. The LEDs at the shift register end of the cable light up to indicate which conductor is being energized. The LEDs at the other end turn on when there is continuity.

The pulse can be propagated through the shift register manually or automatically. In the manual mode, a 555 timer IC is set up as a monostable multivibrator, which clocks the shift register once for every push of the Single-step button.

When the Mode switch is set to Auto, the 555 operates as an astable multivibrator. It clocks pulses through the register at a rate deter-

THE SHIFT REGISTER at the heart of this cable tester has open-collector outputs that can drive LEDs. The 32-bit unit also has a Data-out line through which additional registers can be cascaded, so the tester can be expanded to handle very large cables.



mined by the setting of the 100-kΩ Shift Rate pot.

The two remaining controls are a Reset push button and a Start switch. While it is held down, the Reset control puts a 0.01-μF capacitor in series with the 15-μF timing capacitor. That speeds up the 555 timer, causing it to clock the pulse through the shift register quickly, clearing it so that it is ready for another cycle.

The Start push button sets flip-flop No. 1, which inserts a pulse into the shift register. When the pulse appears at the Q_2 output of the 5833A, flip-flop No. 1 is reset and flip-flop No. 2 is set, which makes the tester ignore any additional start commands until the test cycle is over—when the first pulse has propagated to the last shift register output.

Although the LEDs in the figure are shown as individual units, the tester built by the author actually used 10-element LED bar graphs (Hewlett-Packard HDSP4820s) for convenience.□

CIRCLE 522

MULTIPLEX TEMPERATURE DATA

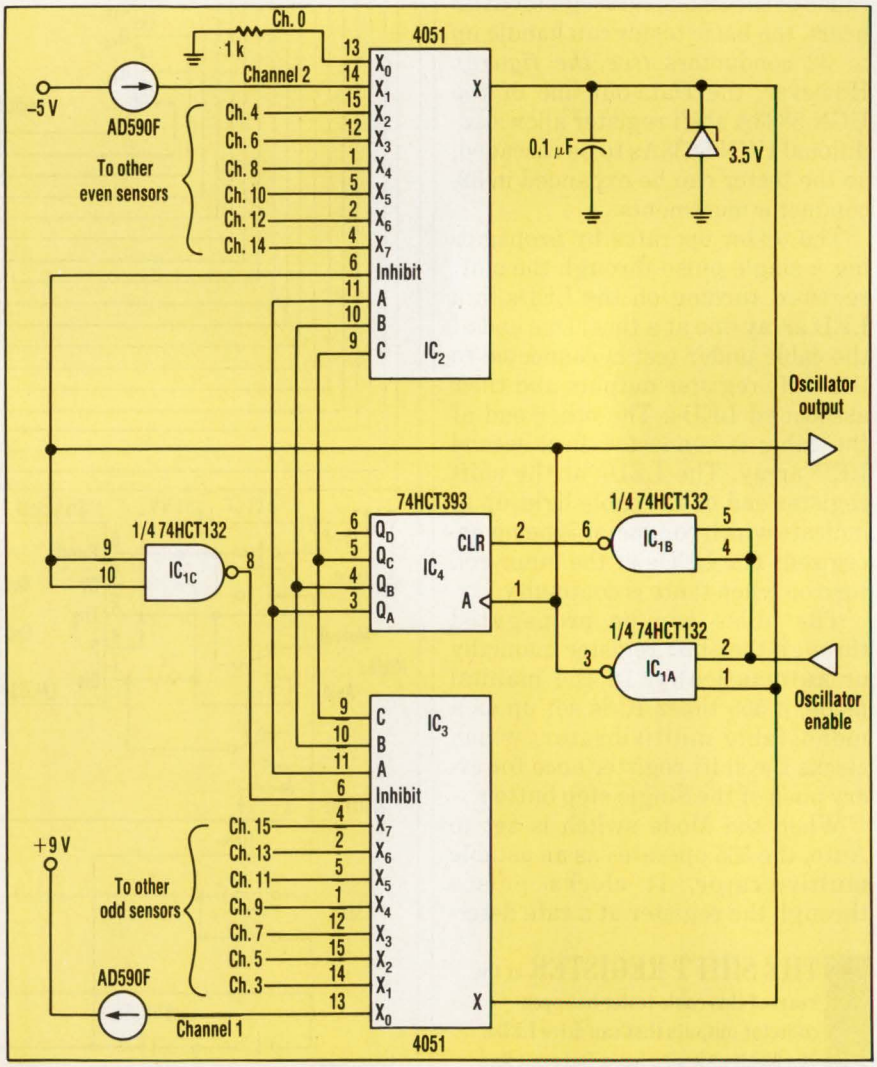
M. RAILESHA
World Friends, Design Group, 53 Sadras East, Kalpakkam 603102, Tamilnadu, India; (4117)-508.

Designed to acquire and transmit multiple temperature signals over a single communication line, this simple circuit *(Fig. 1)* is built around two analog multiplexers, a few supporting components, and 15 AD590F solid-state temperature sensors. The circuit takes the current outputs of the sensors, converts them into pulse widths, and combines them into one pulse train *(Fig. 2)*. Each pulse in the train corresponds to a specific sensor. A fixed resistor on the first channel (Channel 0) produces a very narrow synchronization pulse, which identifies the start of the temperature information sequence.

The sensors for the even-numbered channels are driven by a –5-V supply and connected to analog multiplexer IC_2. The odd-channel sensors, driven by a +9-V supply, go to IC_3. Thus, the lower-voltage pulse widths in the circuit's output correspond to the even-numbered sensors, and the higher-voltage pulse widths are associated with the odd-numbered sensors.

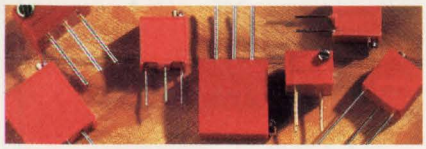
Essentially an oscillator, the circuit is controlled by the Oscillator Enable input at pin 2 of IC_{1A}. When that input goes high, the pulse train begins, starting with the short low-level pulse associated with the fixed 1-kΩ resistor on pin 13 of IC_2. The oscillator continues to operate as long as the Enable signal is kept high.

The AD590Fs have a sensitivity of 1 μA per degrees Kelvin. Their temperature-dependent current outputs are converted into voltage signals by the charge-collecting 0.1-μF capacitor at the (joined) outputs of the multiplexers. Over the course of each oscillator period, one of the odd-numbered sensing elements dumps charge onto the capacitor, and one of



1. THE EVEN-NUMBERED channels in this multiplexed temperature-sensing circuit are connected to IC_2, where they form the lower half of the output pulse train (see figure 2). The odd-numbered channels, connected to IC_3, make up the other half.

Wipers, collectors and screws can't help you trim circuit adjustment costs.



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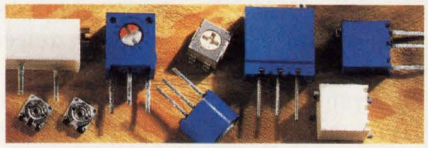

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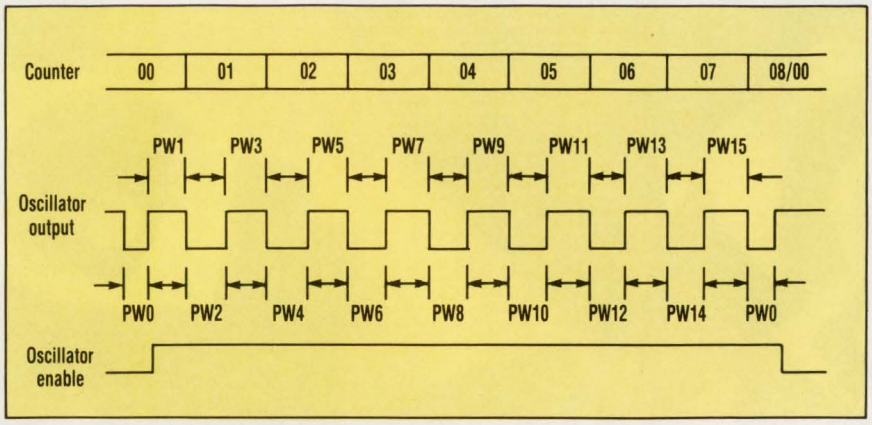


2. THE OUTPUT PULSE TRAIN consists of 16 consecutive pulse widths, 15 being proportional to the temperature of an individual sensor. The exception is the first pulse, designated PW0, which is distinguished by its narrowness. It serves as the synchronizing pulse to indicate the start of the train.

the even-numbered elements removes charge from it. The width of each pulse, therefore, is proportional to the temperature of its associated sensor element. Because the oscillator frequency is determined by the input threshold voltages of the 74HCT132 quad NAND gate (IC_1), it's essential that the power supply voltage for those components be well regulated.

The Zener diode provides overvoltage protection by clamping input pin 1 on IC_{1A} to 3.5 V.□

CIRCLE 523

MONITOR ACROSS ISOLATION BARRIERS

JAMES HENDEN
Continuum, Inc., 3150 Central Expy., Santa Clara, CA 95051;
tel.: (408) 727-3240; fax: (408) 727-3550.

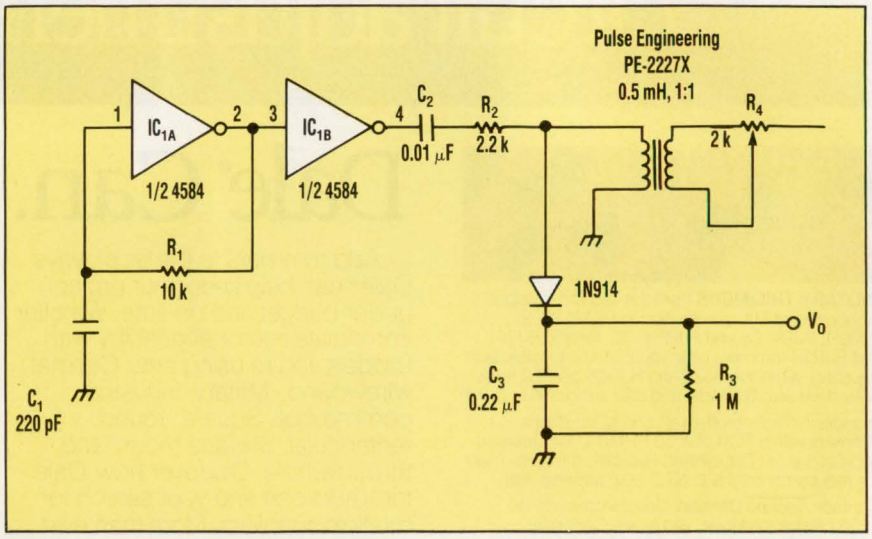
This simple yet effective circuit is designed to monitor switch closures or changes in a variable resistance across a galvanic isolation barrier *(see the figure)*. It exhibits a high degree of noise immunity and requires very little power.

Even more significantly, at least for some applications, it has no components on the monitored side of the isolation barrier except, of course, for the switch or pot. Therefore, if the signal under observation comes from a difficult environment—a high temperature, for example—the circuit could reasonably be expected to present fewer problems than one requiring active components or power on the monitored side.

Basically, the monitored resistance, R_4, combines with R_2 to form an ac voltage divider isolated by the transformer. It loads down the signal at the junction of R_2 and the transformer despite the lack of a common ground. The lower the value of R_4, the lower that voltage. Therefore, the output voltage, V_O, varies directly, though not quite linearly, with the monitored resistance (the component values in the diagram were chosen empirically to provide a roughly linear response for values of R_4 between about 400 Ω and 2 kΩ.)

The 4584 CMOS inverter, IC_{1A}, works with R_1 and C_1 to provide the ac drive signal, which is then buffered by IC_{1B}. Capacitor C_2 removes the dc component before passing the drive on to R_2 and the transformer. The output diode, capacitor C_3, and resistor R_3 serve to rectify and filter the voltage at the junction of R_2 and the transformer. The resulting output, V_O, is a dc voltage level in the range of approximately 0 to 1 V.

Variations on the basic circuit provide an economical means for transmitting different types of non-precision signals across isolation barriers. The tiny pulse transformer used in the circuit is sufficient to transfer a few dozen milliwatts of power across the barrier—enough to drive such components as a small light-emitting-diode display, an audible indicator, or a meter.□



NO ACTIVE COMPONENTS are required on the far side of the isolation barrier with this monitor circuit. The monitored resistance, R_4, loads down the voltage at the output end of R_2 despite the interposed transformer.

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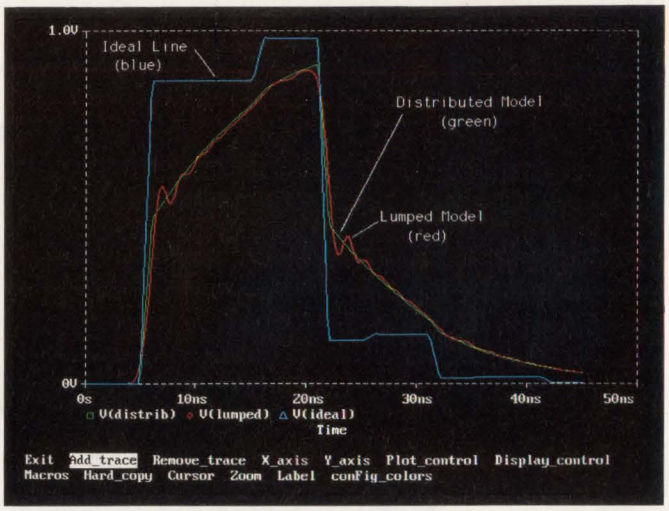

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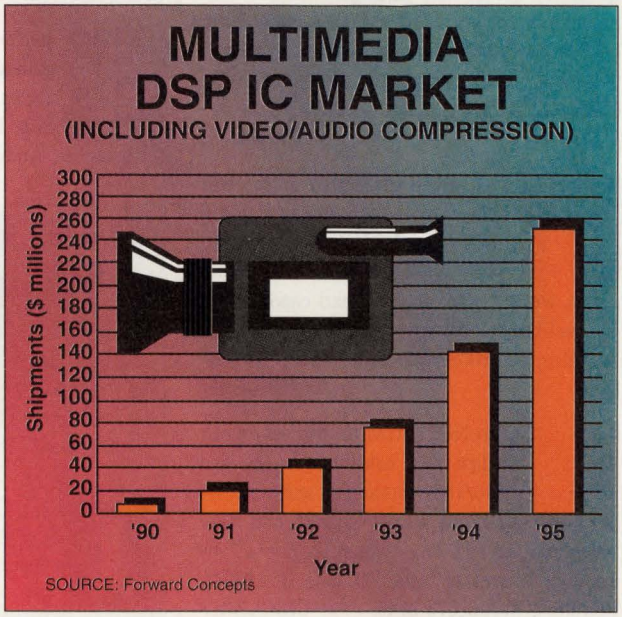
QUICK LOOK

EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Multimedia is creating excitement in the IC and systems markets. In its broadest sense, multimedia means imparting data through a combination of display imaging and sound from a single, integrated source. Training, education, teleconferencing, and public information kiosks are but a handful of areas where multimedia is expected to flourish. Besides microprocessors, some multimedia boards/systems contain digital signal processors. By 1995, DSP-based image compression chips will be found in most PCs and workstations, either as part of multimedia circuits or for compact image storage and transmission. Computer systems customized for audio-visual activity will have DSP circuitry for programmed or interactive image and sound manipulation.

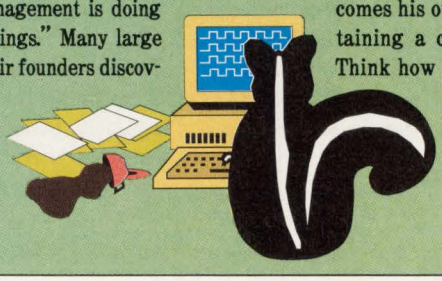
The compound annual growth rate for multimedia DSP chips—mostly ASICs—including video/audio compression, will amount to 99% between 1990 and 1995, according to Will Strauss, of Forward Concepts, a Tempe, Ariz., market researcher. That means $40 million worth of IC shipments this year will skyrocket to nearly $260 million in 1995. Strauss tempers his prediction by saying that the fast-moving multimedia area outdates projections quickly.



TALES FROM THE SKUNK WORKS

Without a leader, there can be no skunkworks. In every case I know of, personal leadership was absolutely critical to success. For instance, the name Kelly Johnson and Lockheed's skunk works are inseparable. The Manhattan project was an extraordinarily effective skunk works. History has judged dozens of scientists on the team as geniuses. At the top, following every detail to a degree his colleagues found mind-boggling, was a leader: Robert Oppenheimer. NASA put a man on the moon in nine years, thanks to a small core team—Wernher von Braun, George Muller, and George Lowe. Yet can you associate any names with NASA's recent debacles? Name for me, if you can, the central individual responsible for the Hubble telescope?

The conventional wisdom is that leaders are much too scarce to "waste" on isolated and risky endeavors such as a skunk works. Yet skunk works and closed loop teams don't consume leaders, they *produce* them. We have myriads of managers but few leaders. As both Peter Drucker and Warren Bennis say, "Management is doing things right; leadership is doing the right things." Many large companies are hacking through the jungles their founders discovered, measuring progress, and toiling onward. Some foreign leaders moved their companies from tractors to electronics, from ball bearings to semiconductors, and from cigarettes to software. Managing well doesn't help much if you are in the wrong jungle.



Unfortunately, our concept of leadership has become superficial. Stephen R. Covey reports that, until recently, U. S. literature on leadership focused on the "character ethic." A person's character was deemed fundamental to leadership ability. With the proper foundation, things like integrity, humility, fidelity, temperance, courage, justice, industry, perseverance, modesty, and the Golden Rule, one might, after years of work, develop leadership ability.

Today America has embraced the "personality ethic," and our leadership literature reflects this (e. g. Donald Trump's book). The basic thrust now is quick-fix influence techniques, charisma, power strategies, communication skills, and positive attitudes. These methods will not work for a skunk works, and many say that the major problem with our industry and political system is that we can no longer trust our leaders.

Running a skunk works is a *stewardship*, another almost forgotten concept. A stewardship is a job with a trust. The steward becomes his or her own boss, governed by a conscience containing a commitment to agreed-upon desired results. Think how much better our lot might be with seasoned, trustworthy, results-oriented leaders running our industry and our nation.

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A free demo of McCAD electronic design tools for the Mac is available from VAMP Inc. The software comes with either standalone, work-group, or front-end capabilities. Contact the company at 6753 Selma Ave., Los Angeles, CA 90028; (213) 466-5533; fax 466-8564. CIRCLE 452

FutureNet software for schematic design has continous zoom and undo/redo commands and supports EDIF. It works in DOS and Sun-based networked environments. For a free demo disk, contact Data I/O, P. O. Box 97046, Redmond, WA 98073-9746. CIRCLE 453

Strawberry Tree's Work Bench data-acquisition and control software needs no programming or user training. Obtain a free demo of the software by contacting Strawberry Tree, 160 South Wolfe Rd., Sunnyvale, CA 94086; (408) 736-1041; fax 736-1041. CIRCLE 454

Actel Corp. is offering its Action Logic System free in its university program for designing and programming the company's ACT 1 family of devices. Included in the package are ACT 1 macro libraries, place-and-route software, and a timing analyzer. The package is available on a 386 PC with Viewlogic and OrCAD libraries; the Apollo workstation using Mentor Graphics libraries; and Sun workstations with either Valid or Viewlogic libraries. The company is also supplying at no cost ten of its A1010A-PL68C 1200-gate devices with each system shipment. Actel will also supply additional devices to any university using Actel within a VLSI design course. Further information is available by contacting the company at 955 East Arque Ave., Sunnyvale, CA 94086; (408) 739-1010; fax 739-1540. CIRCLE 455

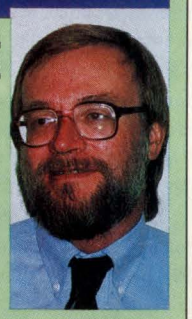
QUICK NEWS: EDUCATION

Interest in techniques for digital signal processing is growing as programmable VLSI devices and low-cost array processors have proliferated. A course from Learning Group International instructs designers in applying DSP techniques, using fast Fourier transform (FFT) algorithms, designing filters for real-time applications, and implementing filters in hardware and software. Participants receive Fortran source listings as part of the course material. With these programs, users can specify design parameters and produce complete, computer-designed digital filters. Courses will be held in various U. S. cities from February through July. For pricing and other information, contact Learning Group International, 1805 Library St., Reston, VA 22090-9919; (800) 421-8166, (703) 709-9019, East Coast, fax (703) 709-6405; (310) 417-8888, West Coast, fax (310) 410-1320. CIRCLE 456

A conference and exposition on CASE (computer-aided software engineering) has management/technical seminars on such topics as object-oriented analysis and design and comparison of CASE tools. CASE World will be held in Santa Clara, Calif. Feb. 18-20. Further information is available from Digital Consulting Inc., 204 Andover St., Andover, MA 01810; phone (508) 470-3880; fax 470-0526. CIRCLE 457

KMET'S KORNER

...Perspectives on Time-to-Market



BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

Let's focus on the interactive properties of measuring TTM and BEAR (break-even after release).

Measurement of TTM provides an overall indication of how well an organization can:

- Select product development alternatives from a large supply of potential opportunities.
- Effectively define products so that they can be cross-functionally and concurrently developed with minimal complication and delay.
- Swiftly plan the execution phase of the product-development effort so that full staff can be applied to get the job done in time to meet market requirements.
- Break out of the cerebral definition phase and actually do cross-functional, concurrent product development.
- For all its positive attributes, TTM and its measurement provide little information about how well a product will perform in the marketplace. Because of this limitation, it is necessary to add another dimension—measurement of break-even after release (BEAR).

Measuring BEAR makes visible how well a product development organization can:

- Create a product that is performance and cost competitive.
- Market the product to generate customer demand.
- Manufacture the product to respond to market demand.
- Convince a customer to spend money on the product.
- Distribute the product to satisfy customer expectations.

Should TTM be increased (more development time and money) to trim BEAR (more performance and less cost)? World-class product developers determine the answer in the definition phase as they control remaining TTM and BEAR. Balancing TTM and BEAR within the definition phase means that this issue is confronted and resolved about half way through the TTM interval. This is when to make trade-off decisions between product cost, product performance, development cost, and development time. The goal is not to statically balance TTM and BEAR—it's impossible. The elements need to be properly distributed so that the scale can be kept in balance. Doing the initial effort right makes the execution phase and the revenue phase snap into place.

Ron Kmetovicz will lead a Time-to-Market seminar entitled "Speeding New Ideas to the Marketplace" at Santa Clara University on March 19. Contact Elmer Luthman, center director, at (408) 554-4521; fax (408) 554-4571.

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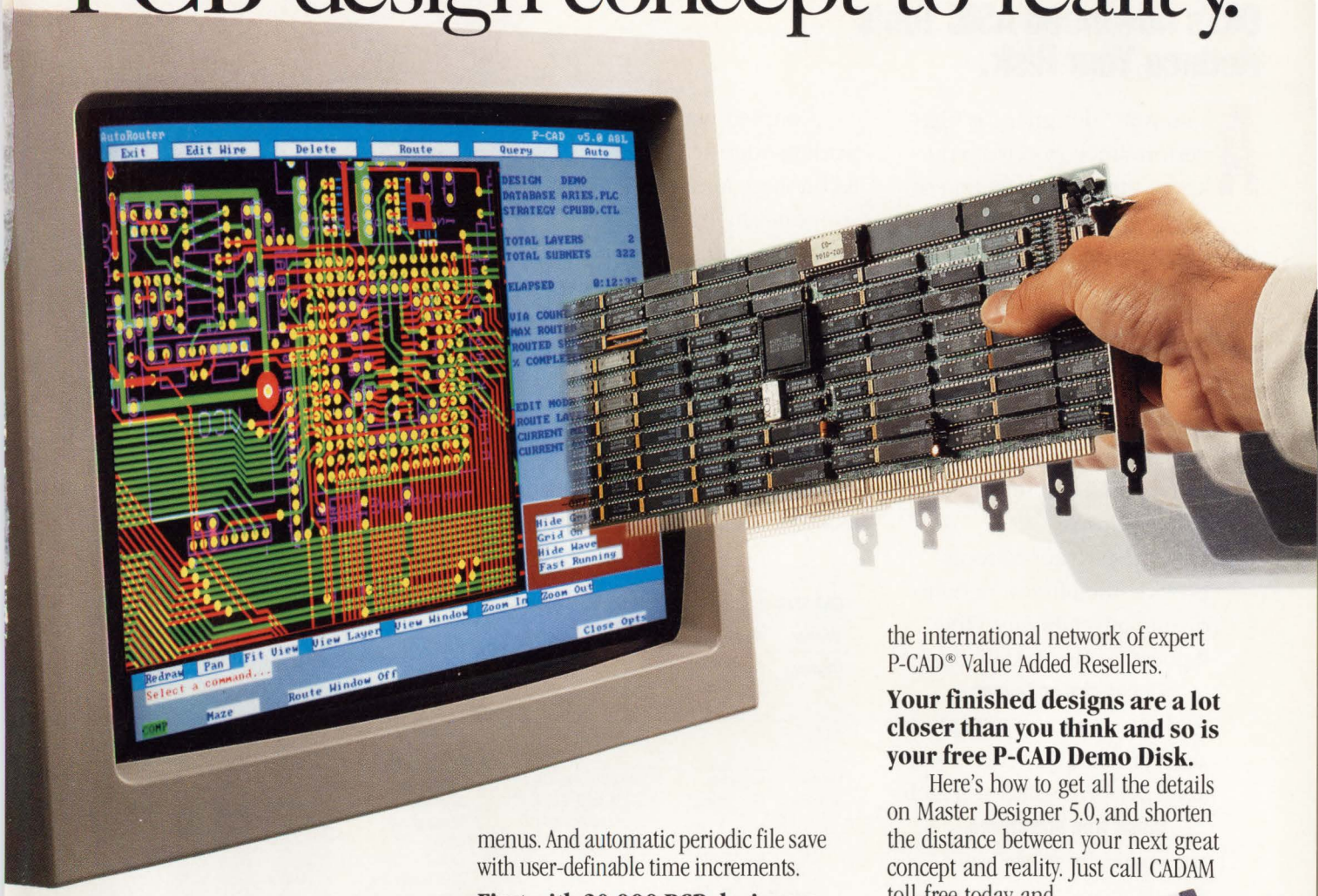

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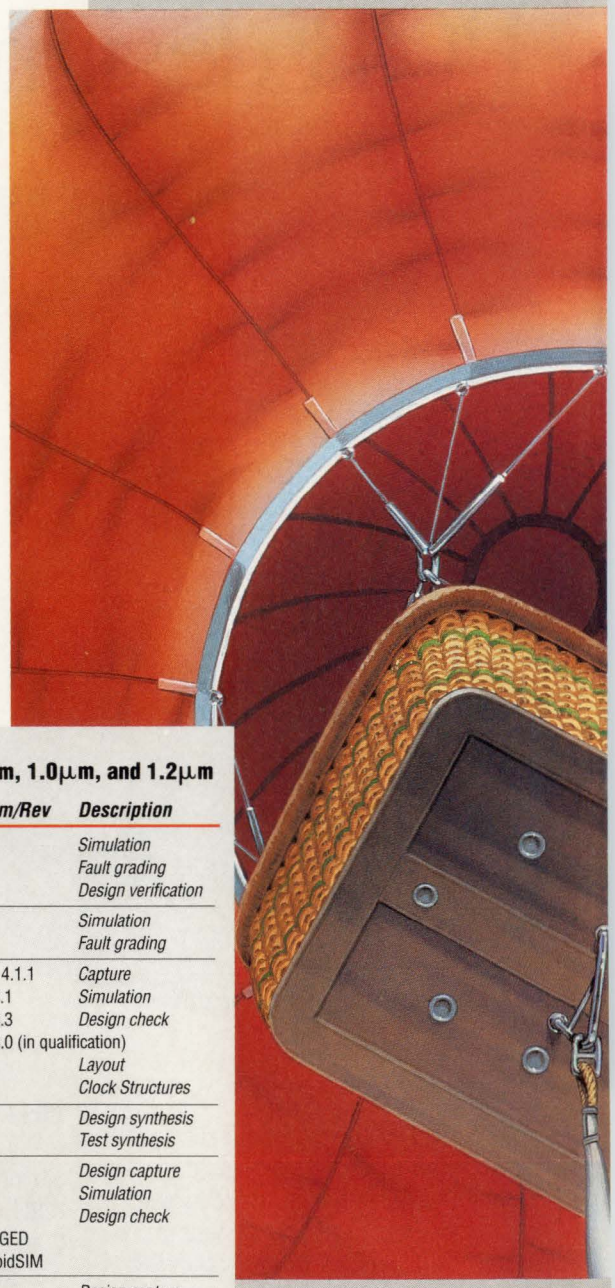

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IKOS		4.0 up	*Simulation* *Fault grading*
Mentor Graphics	HP/Apollo DNx Series HP9000 Sun/SPARC Solbourne	DNIX 5.03, Sun OS 4.1.1 Digital application 6.1 Digital application 6.3 Digital application 8.0 (in qualification) Parade	*Capture* *Simulation* *Design check* *Layout* *Clock Structures*
Synopsys	Sun/SPARC Interface to Mentor, Valid, Viewlogic	Sun OS 4.1.1	*Design synthesis* *Test synthesis*
Valid	Sun/SPARC Sun-3 DECstation 3100 IBM RS6000	Sun OS 4.1.1 GED, ValidSIM, RapidSIM ULTRIX, ValidSIM, GED GED, ValidSIM, RapidSIM	*Design capture* *Simulation* *Design check*
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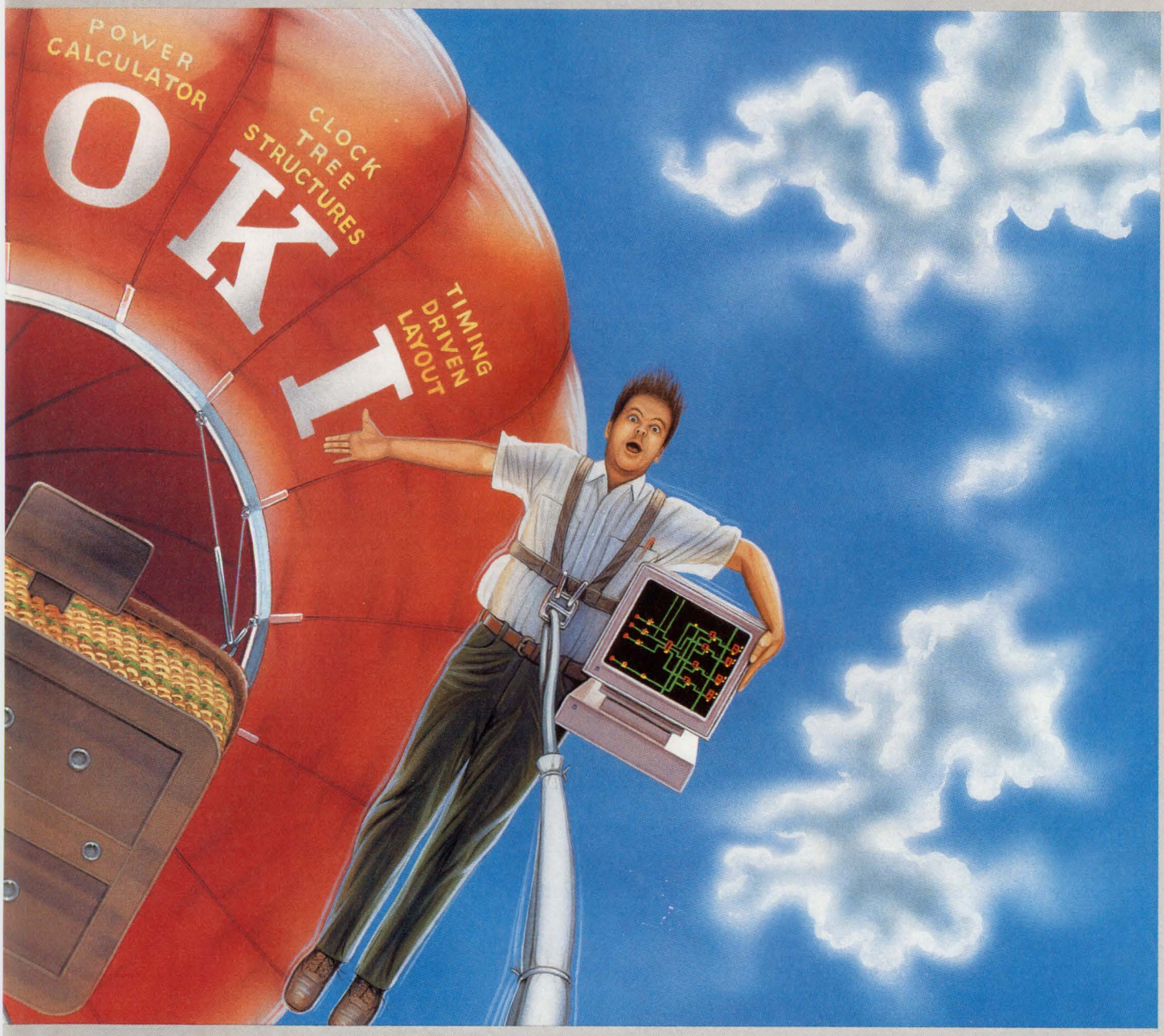

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KEYNOTE PRESENTATIONS:

Dr. Gordon Moore, Chairman of the Board and one of the founders of Intel Corp.

Roger Ross, President, ROSS Technology, a subsidiary of Cypress Semiconductor Corp.

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QUICKLOOK

ON THE JOB

As layoffs continue, finding a job is an increasing concern among engineers. The IEEE-USA's third edition of its two-volume employment guide is free to IEEE members who are unemployed, but not students. The first volume, *An Employment Guide for Engineers and Scientists,* is a practical manual for job hunters, including how to get started on a job search, strategies on coping with job loss, writing letters and resumes, establishing a personal network, preparing for interviews, and evaluating compensation packages. Salary information, drawn from the IEEE's annual salary survey, is included. The second volume lists by state hundreds of companies that employ engineers. Guides are sold through the IEEE Service Center at $14.95 (members) and $19.95 nonmembers by calling (800) 678-4333 and requesting IEEE catalog no. UH0186-7. For the free guide, written requests that include IEEE membership number should be mailed to IEEE-USA, 1828 L Street NW, Suite 1202, Washington, DC 20036.

QUICK NEWS

With an eye on data security, the federal government's standards body is working on guidelines to ensure the privacy of unclassified information in federal computer systems. The goal of a Digital Signature Standard (DSS) being developed by the National Institute of Standards and Technology (NIST) is to verify data integrity and the sender's identity. NIST is seeking comments from the public and federal, state, and local government users. Written comments, due Feb. 28, 1992, should be sent to the Director, Computer Systems Laboratory, Attn: Proposed FIPS for DS, B154 Technology Bldg., NIST, Gaithersburg, MD 20899. Contact Miles Smid at (301) 975-2938.

QUICK REVIEWS

Digital Video in the PC Environment, second edition, by Arch C. Luther is a guide to implementing digital interactive video on personal computers. As Luther points out, DVI makes possible the first systems that truly merge personal computers and television.

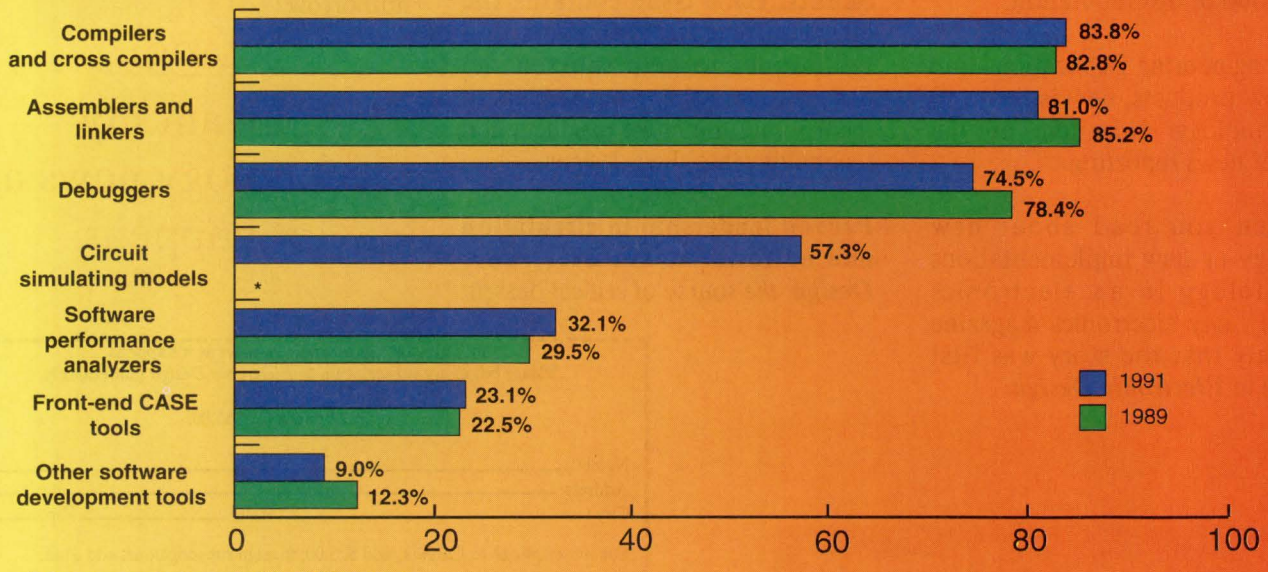
Among the skills needed to work with audio/video/computer systems are audio-, video-, and computer engineering, along with ability in graphics, script writing, creative writing, publishing, programming, and audio/video production and post production. Few readers, of course, have expertise in all these areas. Luther assumes only that readers have an electronics background and interest in the subject. Consequently, Luther gives an overview of these areas and shows how the various technologies come together in creating interactive systems and applications.

Besides covering the i750, Intel's DVI chip set, *Digital Video* discusses fundamentals in analog video, digital video, digital audio, optical storage, and, of course, programming. The book also deals with interfacing the i750 chip set and video compression technology. Although programming a digital-based system is crucial to making a DVI system perform, many developers of audio/video/computer applications aren't programmers. As a result, Luther separates the software discussions so that nonprogrammers may skip them. And new C language software examples, written in accordance with Intel's revision of DVI software architecture, are available on two disks for $24.95 in 3.5- or 5.25-in. format (Digital Video Software Offer, P.O. Box 6069, Alexandria, VA 33206-6069).

Luther, one of the developers of DVI technology, participated in developing the NTSC color TV standard, broadcast video recorders, and consumer VCRs. He holds 32 U. S. patents. With a list price of $29.95, the book is published by Intertext Publications, McGraw-Hill Book Co., New York, N. Y., 1991 (ISBN 0-07-039179-3).

CAD/CAE SURVEY

WHICH SOFTWARE DEVELOPMENT TOOLS DO YOU USE FOR CAD/CAE?



* Category not measured in 1989 survey

Source: a survey of Electronic Design readers conducted by the Adams Co., Palo Alto, Calif. (415) 325-9822 . Readers gave more than one answer to question.

WHAT'S ALL THIS DEAD CAR STUFF, ANYHOW?

Every year, in January, I compile a list of all the Dead Cars I've seen along the highways over the last calendar year. If you want to see a copy, send an SASE and I'll mail it. This year will be the 22nd annual list, going back to when I lived in Massachusetts in 1969. It lists every car according to their manufacturer, and sometimes by type.

For example, I try to keep the GMC cars separate from the Fords or the Chryslers, but I can't possibly segregate the Chevys from the Buicks – for all I know, they have the same engine anyhow.

BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

I do separate the Volkswagens from the Saabs, which was my original intention. Back in 1969, I was trying to show some of my buddies that the Saabs of that era were less reliable than VWs, even though the Saab engines had "only 7 moving parts." I found that there were lots of dead or abandoned Volkswagens along the roads, but there were also quite a few dead Saabs. It seemed that there were more Saabs than one would expect from the number of Saabs on the road. Over the years, I kept on listing all of the cars I saw, dead or abandoned, foreign or domestic.

Now, what's the significance of these lists? Do they prove that one car is more reliable than another? No, not really, because even though you could tell how many cars are registered in any state, that doesn't tell you the number being *driven*. But I have had a lot of fun keeping notes on the Dead Cars. And my friends find it amusing to look at these lists.

Just the other day, I was writing down the data for one dead Mercedes Benz and one abandoned Ford with a flat tire. My passenger asked, "You mean, every time you see an abandoned car, you write down a note?" I replied, "Sure... doesn't everybody?..."

In the last five years, I began to keep a list of the cars I saw with no brake lights. I carry an envelope that I can hold up to warn a driver, "YOU HAVE NO BRAKE LIGHTS". I really don't like to see cars driving around with no brake lights.

It's all too easy for them to collect an innocent car on their rear when they hit their brakes and the following driver can't make this out all that well. So an accident can happen, and in my neighborhood, insurance rates go up even though many of us have had no accidents at all.

On the other side of the placard it says "YOU HAVE ONLY ONE BRAKE LIGHT". After one brake light burns out, what happens next? The other one burns out, and the car is left with none. So I like to warn these guys to get their brake lights fixed. In 1990, I notified 69 cars that they had no brake lights, and 144 cars that they had only one brake light.

There were about six guys with no brake lights that got away – sometimes they turn off in traffic before I can catch up with them, or sometimes a light changes against me. I hate to let a car with no brake lights get away. Still, I think I'm doing something useful, even though my wife sometimes gripes that I beep my horn too much just to tell a guy he has only one brake light.

But think about this: A guy has only a right brake light. He starts to signal for a right turn. Then he hits his brakes. In many cars, the brake light and the blinkers are connected to the same bulb, so when he hits the brakes, no change occurs. In some cases, one brake light burned out is as bad as no brake lights at all.

What do I do about brake lights? On each of my four cars, I've rigged extra brake lights up high so that they're really noticeable to the drivers behind me. If 1 or 2 bulbs burn out, I still have a couple left. Best of all, I can look in my mirror and see if the extra bulbs light up when I hit the brakes, so I can tell if the brakes' pressure-switch is working. Now, with a broad pen and a blank envelope, or a piece of paper taped to an envelope, *you, too*, will be able to warn drivers: "YOU HAVE NO BRAKE LIGHTS" and "YOU HAVE ONLY ONE BRAKE LIGHT".

Just what kind of car do *you* drive, Pease, to get good reliability? Ah, yes, I drive a car with exactly the right amount of modern electronic, computerized equipment – a 1968 VW Beetle (my wife drives a newer car, a 1969 Beetle).

Now, as an engineer, I suppose I should say good things about all of the fancy electronic fuel injection and spark computers and diagnostic computers and Lambda sensors. But I get 31 mpg and the car goes just as fast as I want, and that's good enough for me. The bottom line is that I prefer a car that has proven itself by running reliably for 244,000 miles. In fact, until a couple months ago, it was still running on the original engine, and the original crank and pistons and cylinders (though it's true I had replaced the cylinder heads).

Sometimes I do connect a Heathkit electronic ignition system to minimize wear and tear on the breaker points. But right now it's on the blink, so I just

PEASE PORRIDGE

went back to the old conventional (Kettering) ignition system, points and coil and distributor and "condenser". I set my own timing and I adjust my own valves. That's one good thing about old, simple cars – if something does go wrong (which is rarely) you can fix it yourself.

Do you ever count your own car, Pease, when it's dead? Yes, but that's not very often. One time my coil burned out. One time my distributor got loose and lifted out of its spigot, and it took me a full hour to figure out that when the engine turned, there had to be a reason why the distributor and its rotor did not. Another time a fuel hose fell off, but I fixed that and got going quickly, so I only counted it as 1/2.

There are several cases where I count a car as 1/2. For example, if a guy with a Volvo is talking to a guy with a Datsun, and they both have their hoods up, I may count 1/2 Datsun, 1/2 Volvo, 1 Helper. I count people who are obviously helping out as a Helper, not as a Dead Car. If I'm not sure it's a Rabbit on the other side of the road on a rainy night, I may count 1/2 Rabbit and 1/2 Modern Boxy Car (1/2 Modbox). If I can't even tell if it was probably foreign or U.S.-made, it gets scored as "1 car".

Do I think that electronic systems are going to improve the reliability of vehicles? Well, maybe. I recall the story of one of the first trucks that had an anti-lock brake system. They were driving innocently down the road when a nearby driver keyed the transmitter on his CB radio and the truck immediately locked up all its brakes. It turned out somebody had decided it would *hurt* the reliability to add bypass capacitors across all of the sensors and the inputs of the sensor amplifiers.

That's what you learn from MIL-HDBK-217...remember? So when the transmitter went on, all of the amplifiers went berserk. Oh, the *amplifiers* were perfectly "reliable," but the system had not been engineered properly. It was a miracle that nobody was behind the truck when it locked up all its brakes.

Are the new electronic systems better for the environment? Maybe so. Maybe a new sedan can travel down the road emitting even less smog and emissions than my VW, so long as its computer is working right. But in 10 years, what happens when you can't get parts for the computerized systems? My car will still be running just fine. I think I'll stand pat.

After all, I have all of the tools and techniques I need to keep old VWs running forever. Forever? Well, there are old VWs around here that are over 35 years old, and if I can keep my good new beetles running 35 more years, they may outlive me. You would not want to bet that I can't keep them running. Meanwhile, if I see another VW broken down along the road, I stop and see if I can help.

Sometimes I have a tool or a gallon of gas, or the spare part they're in need of – a fan belt, or some points, or a clamp for a fuel hose. So I try to help solve their problem. If we can't figure out what's wrong, I leave them a SASE so they can write to me and explain what was the problem once they find out.

For example, one guy sent me a letter stating that the 1969 bus he had just bought was merely out of gas. The gas gauge was broken, but the previous owner, of course, had not warned him about that.

So, when I see a dead, abandoned, or broken-down car along the freeway, I score it. I categorize and count it. Now, if a guy is just changing a tire, or pouring in a spare gallon of gas, I list that problem, but I don't count the car as dead or abandoned. In 1990, I saw 24 people that ran out of gas, 139 with a flat tire, 211 pulled over by a cop, and 16 with a broken drive shaft (remember, none of my cars has a drive shaft). I counted 293.5 GMC cars, 146 VWs, and one Citroen. What are the corresponding totals for 1991? I'll let you know as soon as I have them all added up.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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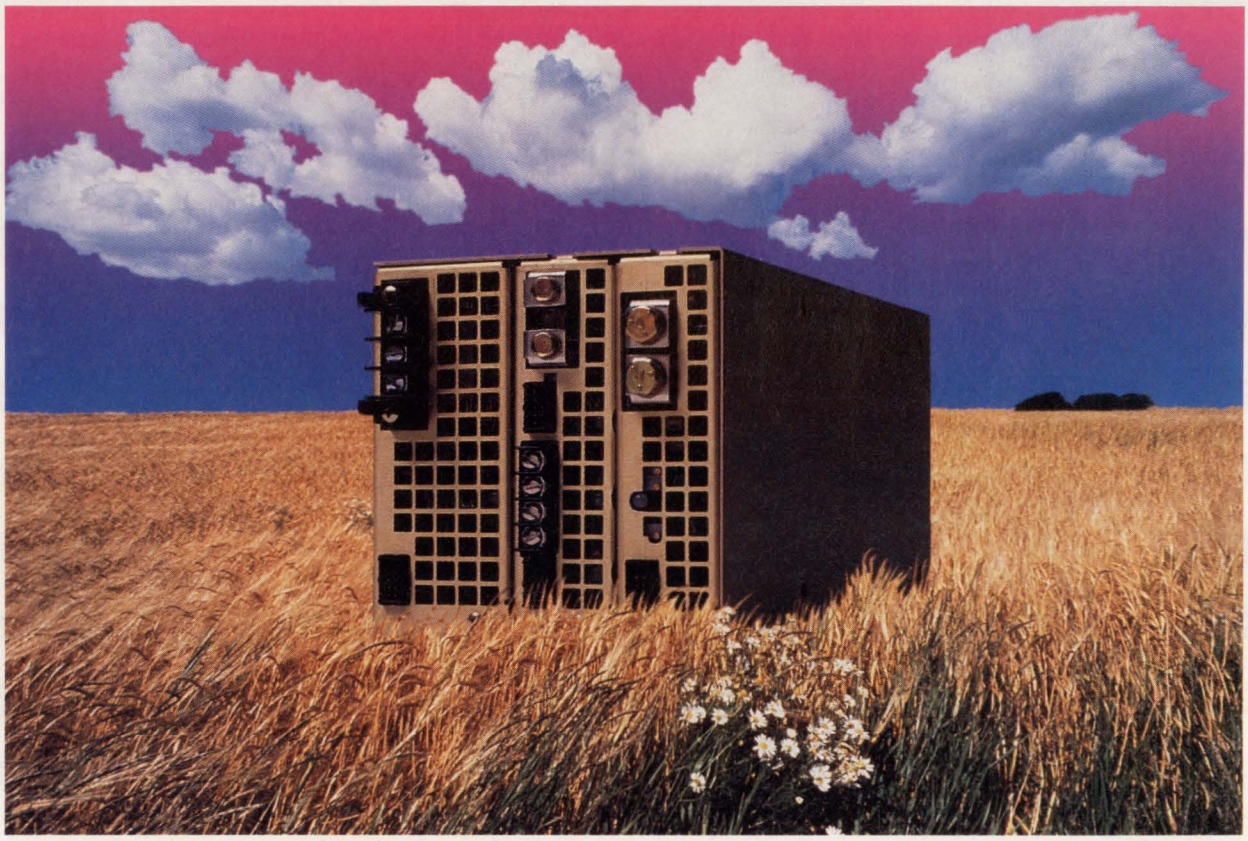

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CIRCLE 88 FOR U.S. RESPONSE

CIRCLE 89 FOR RESPONSE OUTSIDE THE U.S.

A Sextet Of Electromagnetic-Interference Testers Sports A Price/Performance Ratio And Modularity To Suit Any Budget.

Sophisticated Instruments Take On EMI Testing

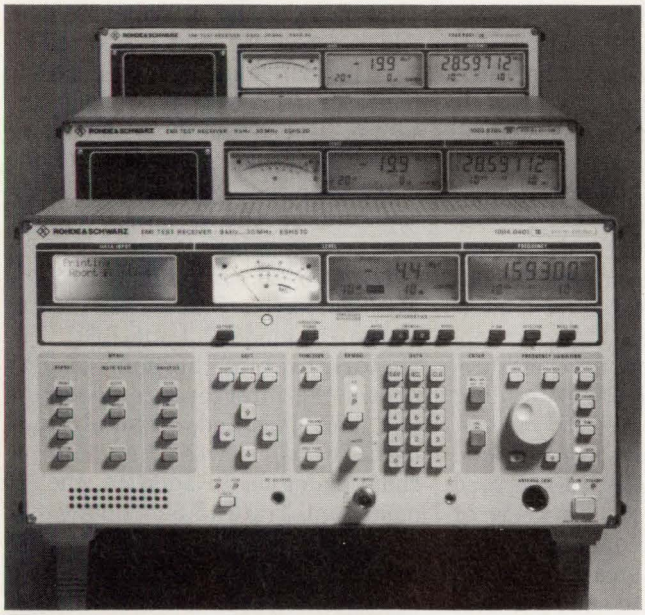
John Gosch

When the 12 countries of the European Community become a single market in 1993, West Europe will be a region where people, goods, and capital can move freely across national borders. It will also be a region with common, mutually recognized standards in all EC countries. One standard will apply to electromagnetic compatibility (EMC)—the ability of equipment or a device to function satisfactorily in its electromagnetic environment without introducing intolerable interference to anything in that environment. Consequently, if companies want to continue doing business in Europe's upcoming barriers-free market—with 345 million consumers, it will be the world's biggest—designers must make certain their equipment meets the new EMC standards, which will be effective sometime in the mid-1990s.

In light of this, Germany's Rohde & Schwarz has a new family of EMC testing instruments that sport what the company claims are "performance firsts." The ESHS/ESVS family combines dedicated commercial EMI testing capability with an exceptional price/performance ratio, setting new standards for EMI test receivers.

Until now, test engineers often used simple spectrum analyzers or manually tuned test receivers to determine the EMI profile of the equipment under test, and to ascertain that the interference did not exceed prescribed limits. But these types of instruments have their technical shortcomings, such as intermodulation problems at the receiver front end, which may lead to unpleasant surprises during final testing of the finished product.

This is where the new tester family comes in: Performing EMI measurements up to 1 GHz, the ESHS/ESVS testers deliver precise results in a matter of seconds and put out legally binding test protocols *(see "The importance of EMI testing," p. 96)*. Thanks to built-in microprocessors and sophisticated firmware, they sport automatic measuring capabilities, besides being manually operable. The testers handle measurements according to



DEDICATED TO EMI TESTING, this trio of instruments from Rohde & Schwarz with analog readouts covers the frequency range of 9 kHz to 30 MHz. The series ESHS includes the ESHS10 (front), ESHS20 (center), and ESHS30 (rear). The -10 unit employs a 4-line LCD, whereas the -20 and -30 use CRT displays. The -20 and -30 units also include a 3.5-in. floppy-disk drive, while the -30 unit also has a tracking generator for 2-port measurements, as well as an IF analyzer for assessing interference visually. Another series with three models, the ESVS, covers the frequency range of 20 MHz to 1 GHz.

SOPHISTICATED EMI TESTERS

THE IMPORTANCE OF EMI TESTING

Historically, EMC testing was considered a luxury because it required specialized equipment with high price tags. Though some might question the need for rigid EMC testing, there's a growing awareness of its importance. Immunity to electromagnetic interference is now considered a key characteristic of product quality. A number of sensational mishaps, such as airplane crashes, uncontrolled robot movements, and snags on automated production lines, were attributed to electromagnetic emissions from nearby equipment. Such events have highlighted the need for EMC testing.

Given the increasing sensitivity of the ever shrinking and faster ICs used today, even the slightest influence from electromagnetic waves must be ruled out. This is best accomplished by planning and designing EMC into the equipment at an early phase of its development. Measures to solve compatibility problems after the equipment is built are compromises, at best, and costly, as well.

such standards as the U.S.'s ANSI C63.2, Germany's DIN/VDE 0876, and Japan's VCC.

The new EMI tester family is available in two different series, each with three models. The ESHS10, 20, and 30 series cover the frequency range of 9 kHz to 30 MHz *(see the figure)*. The ESVS10, 20, and 30 series cover 20 MHz to 1 GHz. The two series differ mainly in configuration, operating features, and price.

Such modularity should especially suit the small budget-conscious company, as it allows for equipment expansion at a later date by adding models in the upper- or lower-frequency ranges, says Wolf E. Schreyer, Rohde & Schwarz's product marketing manager for EMI testers. Modularity also offers the advantage of using different models for different tasks at different locations. For example, while one tester measures interference voltage in a shielded room, the other checks field strength on the outside.

Even the least-expensive models, the ESHS10 and ESVS10, are tough to beat by competitive test set-ups, Schreyer asserts. Used with a coupling network and a plotter, they automatically put out detailed test reports showing whether the EMI limits that the different standards prescribe for the equipment under test are exceeded or not.

The two -10 models are the basis for the new tester family. Operated manually or automatically (with or without an IEC/IEEE-bus controller), they're used for routine EMI measurements, such as interference voltage, current and power checks, as well as field-strength determinations. In addition to external batteries, they can be powered from internal batteries, suiting them for mobile applications or for measurements under difficult grounding conditions. The -20 and -30 models, which boast enhanced operating and measuring capabilities, can be used for measurements on all kinds of equipment, from small electric tools to big computing systems.

Common for all models are controls, LCDs, and an analog pointer-type indicator familiar to any instrument operator. Frequencies are set in coarse, medium, and fine steps with a rotary control, or entered into the instrument via a keyboard. A 4-line LCD on the -10 models is for the man/machine dialogue, and two other LCDs for showing the selected settings and test results. The displays are easy to read both in bright light and (thanks to backlighting) shielded rooms.

While the controls and the indicator are used in manual operation, input keys call up the menus for automatic operation. The keys enter the start and stop frequencies, step sizes in the frequency scans, limit lines, transducer factors, printer and plotter configuration, and complex test routines.

The results are shown either by the analog indicator, or digitally on the appropriate LCD with 0.1-dB resolution and in the correct units—for example, in dBμV, dBμV/m, dBμA, or dBm. A built-in loudspeaker allows audible evaluation of interference, and a special mode helps to detect weak continuous-wave signals.

Of note is the analog indicator, which not only shows measured results in dB, but also serves as a trend indicator. Only with an analog indication is it possible to determine whether a measurement is being made near the noise floor or at the top end of the dynamic range, Schreyer explains.

The two -20 models (ESHS20 and ESVS20) have a CRT screen instead of the -10 models' 4-line LCD. The vector-graphics screen display shows the interference spectrum and limit lines and, on an alphanumeric basis, serves the man/machine dialogue. In addition, the -20 models integrate a 3.5-in. floppy-disk drive that records the measured results. It also stores the measuring routines or loads them into the tester. The two -30 models (ESHS30 and ESVS30) are similar to the -20 models except that they have a tracking generator for 2-port measurements, and an IF analyzer for assessing the interference visually *(see the table)*.

Europe's upcoming EMC standards reflect a radical change in how interference is assessed. The existing national norms, such as Germa-

ROHDE & SCHWARZ'S SERIES ESHS/ESVS EMI TESTERS

Feature	Model 10	Model 20	Model 30
RF analysis		X	X
3.5-in. floppy disk		X	X
CRT display		X	X
Tracking generator		X	X
IF analysis			X
Battery installable	X		
Battery operation	X	X	X
Analog readout	X	X	X
Digital display	X	X	X
Calibration generator	X	X	X

SOPHISTICATED EMI TESTERS

ny's VDE standards, define two classes of interference, narrowband, and broadband, and have different limits for each. But as electronics equipment proliferates, the equipment itself is growing as the main source of interference, and it becomes more difficult to distinguish between narrowband and broadband interference generated by an outside source, or by the equipment itself. So the present distinction (narrowband and broadband interference) will be abandoned when the new EMC standards are in force.

New standards will specify only average values and quasi-peak limits for interference. This means that both pulse and sinewave interference must be averaged or weighted. For this, the ESHS and ESVS testers use group-delay IF filters.

The new testers feature a number of innovations that clearly set them apart from competitive test set-ups. Among them are the parallel use of several measuring detectors, built-in intelligence in the form of firmware, the use of flash EPROMs for storing the firmware, fast frequency synthesis, and the output of a detailed test report.

In the patented parallel measuring scheme, the detectors for the peak, average, and quasi-peak display operate simultaneously. The weighted results are present after the first frequency scan and can then be further processed by the built-in intelligence or an external controller. Parallel use of detectors considerably cuts the measuring time and thus overall testing costs.

Rohde & Schwarz's engineers put much effort into developing the firmware, the built-in intelligence which specifies the tester's basic performance data. Even without controller support and with no extra software, the firmware allows fast measurements to be made with the average- and peak-value detectors. Using the limit lines, it also fixes the critical frequencies and, in the case of interference-voltage tests, permits repeat measurements at these frequencies to be performed with average- and/or quasi-peak detectors.

The firmware is stored in flash EPROMs and, with the aid of a PC, can be loaded from a floppy disk via the serial interface in 5 minutes. Therefore, the firmware can be modified easily, without opening the tester and replacing the EPROMs. This makes it much easier and faster to upgrade programs—even via international data transmission lines—or to correct and update them in case of errors.

For fast results, the testers use frequency synthesis with short settling times. At a frequency resolution of 10 Hz and 100 Hz for the ESHS and ESVS series, respectively, the synthesizers allow frequency jumps of any step length within 10 or 30 ms. At a 1-ms measuring time, it takes only 20 seconds to completely scan the 9-kHz-to-30-MHz frequency range and obtain results with the ESHS testers.

Given the importance of EMI measurements these days, the test report, or measuring protocol, should constitute a legally binding document. Consequently, in addition to the measured values, the protocol contains such information as designation and operating mode of the equipment under test, the specifications used, the tester settings, the test date, and the name of the test engineer. Test date and settings are recorded automatically; other pertinent test information is entered manually.

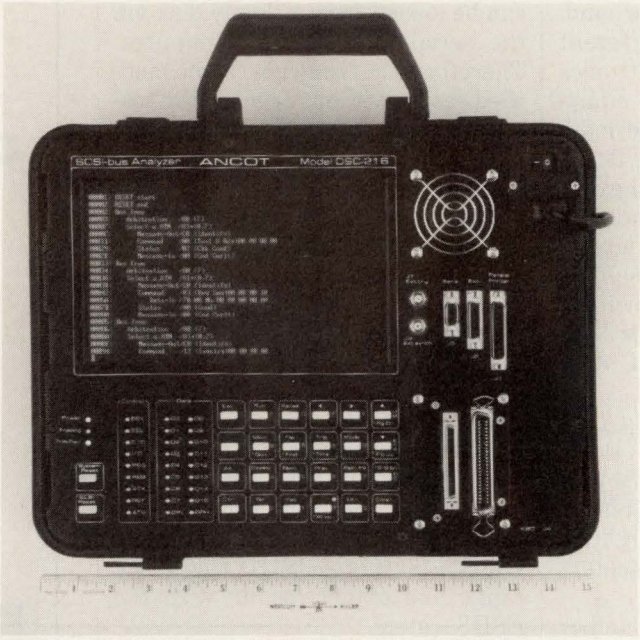
PRICE AND AVAILABILITY

Prices for testers marketed in the U.S. range from $20,830 for the ESHS10 (the simplest model) to $41,000 for the ESVS30 (the most sophisticated model). Accessories (prices are not included in the figures above) encompass coupling networks, such as artificial mains, current clamps, and power clamps, and measuring antennas for the higher frequencies.

In the U.S., Rohde & Schwarz, 4425 Nicole Dr., Lanham, MD 20706. Contact: Scott Elkins, (301) 459-0800. Rest of world: Rohde & Schwarz GmbH, Dept. 1EV, P.O. Box 80 14 69, D-8000 Munich 80, Germany. Phone: (0049)-89-41290 (ask for 1EV department).

CIRCLE 513

HOW VALUABLE?	CIRCLE
HIGHLY	541
MODERATELY	542
SLIGHTLY	543



1. THE DSC-216 SCSI BUS ANALYZER fits into a compact attache-style case. The display is an 80-character-by-24-line electroluminescent panel.

PORTABLE ANALYZER AUTOMATES SCSI TESTING

WITH 16-BIT-WIDE CAPABILITY AND 20-NS TIME STAMPING, THIS ANALYZER HANDLES THE FASTEST AND WIDEST SCSI BUSES.

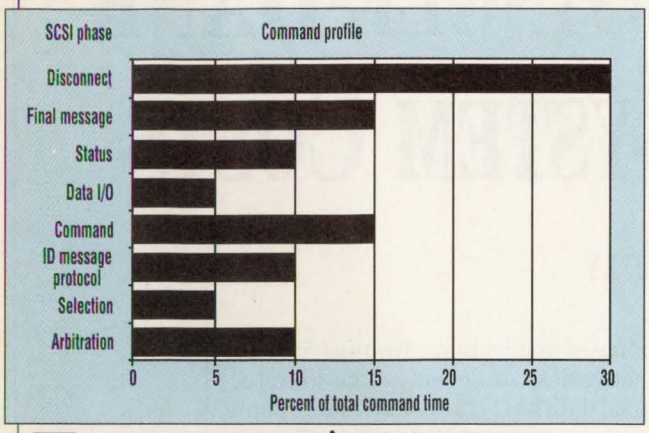
JOHN NOVELLINO

Automated measurements are becoming the norm rather than the exception these days. High-level automation has arrived for designers and integrators of SCSI bus peripherals in the form a SCSI bus analyzer that makes more measurements at faster speeds than previously available instruments.

The DSC-216 SCSI bus analyzer performs command profiling, histogram analysis, and data-transfer rate calculations. The instrument features time stamping with 20-ns resolution so it can capture all phase, handshake, and timing information for transactions at the full 10-MHz rate specified by SCSI-2 Fast. The DSC-216 also handles 16-bit wide transactions, making it possible to track data at the 20-Mbyte/s asynchronous or synchronous rate of SCSI-2 Fast and Wide specifications. An LED display covers the eight control lines as well as the 16 data lines, allowing users to monitor real-time activity at a glance. A SCSI reset key simplifies resetting of the bus.

All this capability fits into a highly portable 15-by-11-by-6-in. attache-case style package

AUTOMATED SCSI ANALYZER



2. THE ANALYZER'S COMMAND profiling capability helps users identify SCSI command overhead during bus utilization. The report shows the time spent on each phase of a SCSI command.

(Fig. 1). The unit's display is an 80-character-by-24-line electroluminescent panel. With the panel-mounted keyboard, users can select most functions with one keystroke. Another unique feature of the DSC-216 is the ability to trigger in or out to external instruments—such as oscilloscopes or logic analyzers—via two front-panel BNC connectors. An RS-232 port, an expansion port, and a printer port are included.

Users can connect virtually any SCSI system to the DSC-216. The front panel has connectors for Centronics-type 50-pin SCSI cables and 68-pin high-density SCSI cables. An optional interconnect adapter offers seven other types of high- and low-density connectors, including the DB-25 Apple device. All are interconnected, so designers or integrators can use them simultaneously.

Among the new reports supplied by the analyzer is the command profile. This function is particularly useful in comparing SCSI devices and the efficiency of SCSI chips. The report indicates the time spent on each phase of a SCSI command, with the results displayed numerically or in graphical form *(Fig. 2)*. This report quickly tells users which peripherals are taking the longest time to respond and eliminates the need to sift through the trace data and calculate the time spent on each phase.

Three types of data-transfer rates are calculated by the DSC-216. The *maximum burst* rate is calculated over a limited number of bytes within a block. This figure does not include overhead and is the maximum rate the device can support under ideal conditions. The analyzer also measures the *sustained* rate, which is the average speed per byte over multiple consecutive blocks—for example, 100 blocks of 512 bytes each. This is the maximum rate at which the device pair can communicate indefinitely. Finally, the *average throughput* is the transfer rate over a large number of small random transfers, which includes overhead. This figure is a realistic estimate of hardware's speed in an application program.

A powerful triggering system also eases the bus-analysis task. Users can select from 14 trigger conditions, including SCSI reset, select/reselect, select/reselect time out, status, command and status, parity error, and message. The conditions can also be used in combination. Besides starting a trace, the trigger can also stop a trace.

The DSC-216 has a deep trace memory—32k events in a circular buffer. A 128k-event memory is also available. Because the trace is event-driven, the analyzer captures 10-MHz data transfers and multisecond disconnects equally well.□

PRICE AND AVAILABILITY

The Model DSC-216 portable SCSI bus analyzer costs $8550 with the 32k-event memory and $9950 with the 128k-event memory. The optional interconnect board is $360. Delivery is 30 days after receipt of an order.

Ancot Corp., 115 Constitution Dr., Menlo Park, CA 94025; (415) 322-5322. **CIRCLE 514**

HOW VALUABLE?	CIRCLE
HIGHLY	544
MODERATELY	545
SLIGHTLY	546

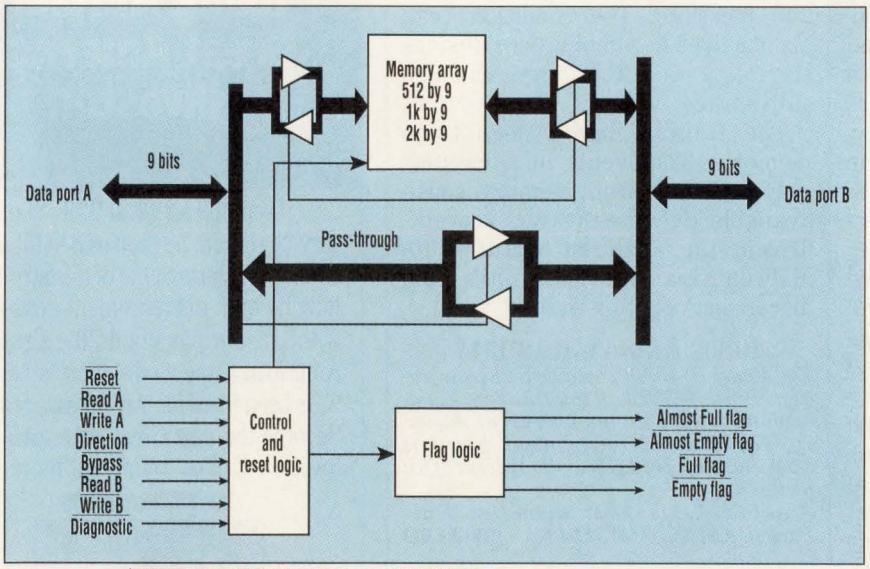
BIDIRECTIONAL SINGLE-BANK FIFOS TRIM SYSTEM COSTS

DAVE BURSKY

Serving as data buffers in a wide range of applications, first-in/first-out memories have appeared in a wide variety of densities and architectures to suit many uses. Bidirectional data buffers are extremely popular for storage and data-communication systems applications. However, to make a bidirectional FIFO buffer, a system designer must either connect two unidirectional FIFO chips in back-to-back fashion, or the FIFO chip designer must integrate two banks of storage on the substrate, almost doubling the chip area. Either approach increases system cost and might reduce the economic viability of the approach.

To keep the chip more cost effective, designers at Integrated Device Technology came up with an asynchronous sharing scheme that allows a single internal memory bank to serve both directions. That keeps the chip size to within a reasonable percentage of a unidirectional FIFO memory, and also keeps down cost. The company's new family of three devices differ only in storage density. The IDT7271, 7272, and 7273, are organized as 512-, 1024-, or 2048, 9-bit words, respectively.

The FIFO buffers can be accessed in just 25 ns. Although they are bidirectional, the control scheme allows data to flow in only one direction at a time. This limitation will probably not impact over 90% of the system designs, according to Mike Shamshirian, IDT's FIFO product manager. Most applications, he says, only require that data transfers be done in one direction at a time—disk-drive data buffers for example either accept data from the host system or hold data being read from the disk. Only in the highest-performance applications will simultaneous data transfers be required, and for those needs dual-bank FIFOs can meet the transfer requirements.



REQUIRING A SINGLE bank of memory, Integrated Device Technology's bidirectional FIFO chip uses a Direction pin to control the direction of data flow between Ports A and B. A memory bypass feature lets critical data skirt the memory array and the delay it imposes, thereby allowing time-critical data to immediately reach the opposite port.

Controlling data-flow direction is a direction pin, which sets the flow from Port A to Port B or vice versa. When that pin switches states, it changes the direction of the I/O buffers, resets the Read

and Write pointers, sets flags to their proper states, and disables the opposite direction's control signals. Port A, however, is predefined as the priority default port and can be used to control all accesses. Because data flows in one direction at a time, the port pins can be shared, thus keeping the package pin count to just 32 pins for either the DIP, plastic leaded chip carrier, or small-outline J-leaded cases.

As noted, the chip area of the single-bank bidirectional FIFO is almost 50% smaller than the dual-bank bidirectional FIFO. The smaller chip area lets the single-bank memory fit into smaller packages, such as the SOJ, which could not handle a larger-size chip. The smaller packages, in turn, lets the memory occupy less pc-board area so designers can reduce system size.

A bypass capability is built into the FIFO array. This feature allows critical data to bypass the delay imposed by going through the on-chip memory array, and flow directly from one port to the other *(see the figure)*. The memory also includes several flags, similar to flags on other FIFOs: There are fixed Full and Empty, as well as fixed Almost Full and Almost Empty. The almost flags have fixed offsets of eight bytes, which gives the system time to respond as system conditions change.

A Chip Reset signal allows the system to reset the contents of all pointers and flags, but leaves the contents of the memory unchanged. Consequently, certain operations can be set up as repeat loops, especially if the loop length doesn't extend to the full depth of the register. The memories also include a dedicated diagnostic pin that invokes a test mode that allows data written into one port to be read back by the same port. That permits the system to test the memory cells, and to ensure that data written into the chip is unchanged when read out. If a change occurs, memory cells may be defective and a diagnostic routine can notify the host system of a service need.□

PRICE AND AVAILABILITY

Samples of the single-bank bidirectional FIFOs will be available later this month for DIP and PLCC form, and next month for SOJ packages. In lots of 1000, the largest member of the family, the 2k-by-9 IDT7273L25, sells for $39.90 apiece (plastic DIP version). Prices for the smaller 1k-by-9 and 512-by-9 devices are $30.70 and $25.60 each, respectively, also in lots of 1000 and plastic DIPs.

Integrated Device Technology Inc., 3236 Scott Blvd., P.O. Box 58015, Santa Clara, CA 95052-8015; Mike Shamshirian, (408) 944-2082. CIRCLE 512

HOW VALUABLE?	CIRCLE
HIGHLY	547
MODERATELY	548
SLIGHTLY	549

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CIRCLE 192 FOR U.S. RESPONSE CIRCLE 193 FOR RESPONSE OUTSIDE THE U.S.

VGA Chip Ups Colors, Speeds Graphics With Local Bus Interface

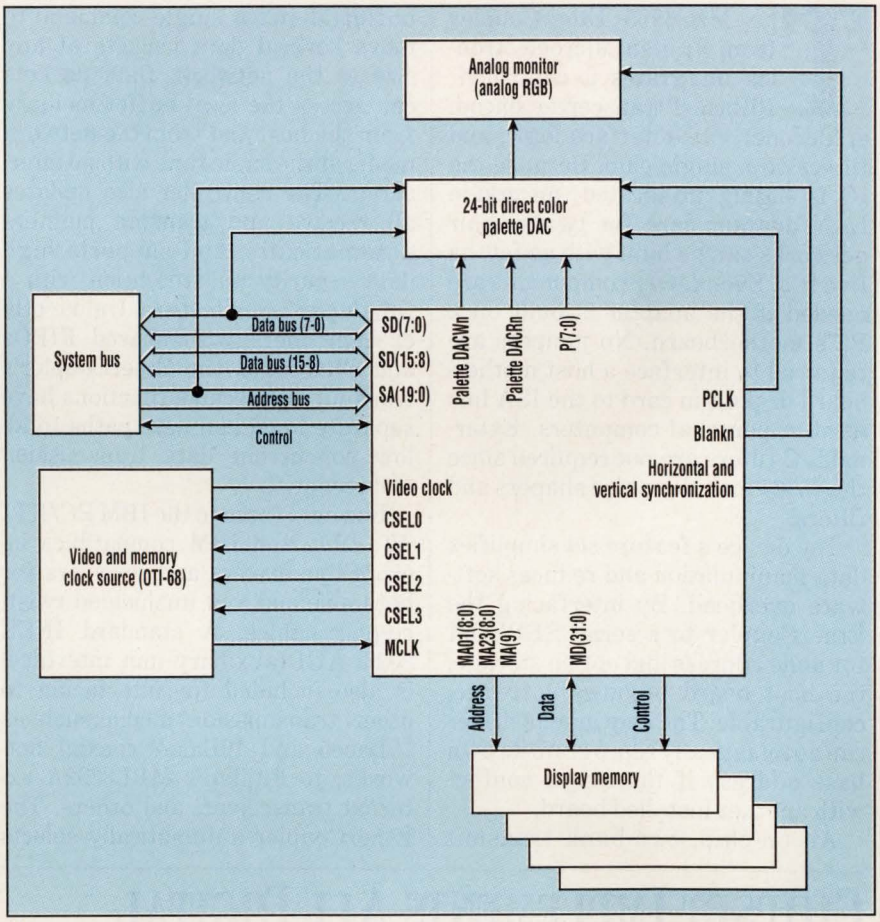
Dave Bursky

The OTI-087 graphics controller outperforms other VGA chips. It addresses up to 2 Mbytes of memory and implements a direct processor interface that bypasses the traditional AT-bus interface for VGA controllers. The Oak Technology circuit can provide 24-bit color (16.8 million colors) with a resolution of 640 by 480 pixels or deliver high-resolution 1024-by-768 non-interlaced, or 1280-by-1024 interlaced images, both with 256 colors.

An on-chip write-cache supports high-speed transfers over the local processor bus at maximum bus speed while a read-cache provides zero-wait-state bit-block-transfer operations for fast image movement on the screen. The local-bus interface also implements XT or AT bus control signals if the designer opts not to use the local-bus interface. However, by tying directly into the processor's system bus, the OTI-087 UltraColor control chip can transfer image data at CPU bus speeds of 33 MHz (80386 or 486 CPUs). That moves data into the video memory at speeds three to four times faster than by using the XT or AT expansion buses, which are usually limited to below 10 MHz.

The chip's video memory interface allows 8, 16, or 32-bit wide data paths to the display memory as well as the use of the fast page mode in standard DRAMs. Video clock rates of up to 80 MHz can be driven by the controller, and that allows CRT refresh rates of over 70 Hz (meet or exceed the Video Equipment Standards Association refresh standard) are supported by the controller.

On-chip foreground/background color expansion registers also help improve the speed of text output, especially when the chip employs the packed-pixel operating mode. The registers allow eight consecutive bytes to be expanded from one byte that contains the foreground and background bits. Hardware cursor support in the form of a 64-by-64 by 2-bits/pixel writable memory allows the user to download a custom cursor image and change it depending on the application or system user's mood. A 16-bit graphics latch permits true 16-bit operations in the planar modes and special 256-color pattern and fill modes improve the drawing speed of complex images.



In most VGA systems some configuration data must be provided to the video BIOS firmware. The OTI-087 can tie into a small serial, electrically erasable memory that provides non-volatile storage of software-alterable configuration settings.

Since the local bus interface is not a universal standard, Oak has worked with a number of chip-set suppliers to ensure that several PC motherboard chip sets would be fully functional with the VGA chip while minimizing the amount of glue logic needed to tie in the 087 controller. Some of the motherboard chip-set suppliers include OPTi Inc., Santa Clara, Calif., Elite Microelectronics Inc., San Jose, Calif., and VLSI Technology Inc., Tempe, Ariz. Oak has also developed true-color driver software as well as high-resolution drivers and a video BIOS. Software drivers are available for many popular application packages. An evaluation board is scheduled to be available this month. Housed in a 160-lead plastic quad-sided flat package, the controller will sell for $31 apiece in thousands. Samples are available now.

Oak Technology Inc., 139 Kifer Court, Sunnyvale, CA 94086; Brian Davis, (408) 737-0888. **CIRCLE 458**

10BASE-T ETHERNET LAN CHIP INTEGRATES KEY CONTROL FEATURES

MILT LEONARD

The MB86965 EtherCoupler from Fujitsu Microelectronics integrates a controller, 10Base-T transceiver, encoder/decoder, bus-interface logic, and filters on a single chip. Because the IC is highly integrated, an add-in LAN adapter card for twisted-pair networks can be built with as few as five ICs. Even fewer components are needed if the adapter is built on a PC's motherboard. No jumpers are required to interface a host motherboard or plug-in card to the ISA bus used in personal computers. External L-C filters are not required since the 86965 includes pulse shapers and filters.

The device's feature set simplifies data manipulation and reduces software overhead. By interfacing the EtherCoupler to a serial EEPROM for node address and option storage, the host board becomes software-configurable. The chip and its driver can automatically reprogram its own base address if there is a conflict with another installed board.

An on-chip, two-bank transmit buffer allows a single command to move several data packets of any size to the network. Data packets can access the local buffer memory from the host and from the network media at the same time with no interaction. The controller also updates all receive and transmit pointers automatically, and supports high data security and retention with a full-duplex architecture. Unlike other controllers with shared FIFOs and CRC logic, the EtherCoupler's transmit and receive functions have separate logic and data paths to allow concurrent data transmission and reception.

Bus interfaces to the IBM PC/XT/AT, ISA, and IBM compatibles include line drivers and receivers for both shielded and unshielded twisted-pair cables. A standard IEEE 802.3 AUI (auxiliary unit interface) is also included for interfacing to other transmission media such as 10Base5 and 10Base2 coaxial networks, to Fujitsu's MBL8392A external transceiver, and others. The EtherCoupler automatically selects the active media.

The chip is also software-compatible with Fujitsu's NICE MB86960 Ethernet LAN device and is supported on all popular PC network operating systems with the use of the company's node drivers. The driver set includes support for Novell's NetWare 286 IPX and 386 ODI, 3Com's 3+ Open, Microsoft's LAN Manager, Banyan's VINES, TCP/IP on DOS, Windows, OS/2 and UNIX, Netbios, and Network File System.

Packaged in a 160-pin plastic quad flat package, the controller is made with mixed-mode CMOS technology and operates from 5 V. Samples of the EtherCoupler are available now, along with evaluation boards and sample hardware designs. Production quantities will be available in the second quarter of this year. Prices begin at $30.60 and $24.45 each in quantities of 1000 and 10,000, respectively.

Fujitsu Microelectronics Inc., 77 Rio Robles Ave., San Jose, CA 95134-1807; Betsy Taub, (408) 456-1160. **CIRCLE 481**

CHIPSET IMPLEMENTS ALL-DIGITAL PHONE AND ANSWERING MACHINE

Intended to displace mechanical tape drives in telephone-answering machines, a chip set for integrated all-digital phones and answering machines from DSP Group stores both outgoing and incoming messages in dynamic RAM. The D6055A chipset is based on the company's proprietary Digital SpeakerPhone speech-processing algorithms running on the TMS320 digital-signal processor (DSP) from Texas Instruments Inc.

Besides the TMS320 DSP chip (64-pin PQFP), the chipset consists of an ASIC (80-pin PQFP), an analog I/O interface (16-pin DIP), and from 1 to 16 Mbits of audio RAM (ARAM). The combined chips and speech-processing algorithms eliminate the problems that are associated with common speakerphone operation—in particular, one-way communication, blocking, and word cut-off, to afford comfortable communications that can simulate regular two-way conversion.

Under control of a host microcontroller, the DSP provides voice-activated switching (VOX) functions, receive and transmit dual-tone, multiple-frequency signaling, line monitoring, speech compression, error coding, echo cancellation, and command decoding. The ASIC controls and refreshes the ARAM, and provides interfaces to the host processor, the analog I/O interface chip, and to external static RAM which stores calculation coefficients and phone numbers. The analog I/O interface performs A-D and D-A conversion, converts 14-bit linear code to 8-bit μ-Law PCM code, and interfaces to the analog front-end of the speakerphone. Computer-controlled digital storage allows for advanced features such as multiple mailboxes and message forwarding, enabling a speakerphone to perform as a personal voice-mail system.

The D6055A provides all the level detectors, attenuators, and switching control that are necessary for proper speakerphone operation. Detection sensitivity, path attenuation, and switching speed can be controlled by the host. Gain distribution between the transmit and receive paths is optimized to the inputs from the VOX level detectors.

These circuits control the transmit and receive paths to provide the half-duplex operation required in a speakerphone. Total loop-gain attenuation is programmable in 4-dB increments from 12 to 40 dB. Pricing for the D6055A chipset ranges from $18 to $25 each in high volume.

***DSP Group Inc.**, 4050 Moorpark Ave., San Jose, CA 95117; (408) 985-0722* **CIRCLE 482**

■ *MILT LEONARD*

PC ENCLOSURE STANDS UP TO HARSH ENVIRONMENTS

The A-bus is a toughened enclosure that offers a rugged and safe housing for industrial PCs. High-integrity shielding techniques, such as seam-welded construction, help deliver a system housing that can meet the most stringent electromagnetic compatibility standards. The enclosure is a 4U-high, 19-in. rack that comes ready to use with an integral backplane, power supply, and cooling fans. Different configurations are available, including six or twelve slots. The enclosure can be fitted with full RFI gasketing and high-attenuation cutoff air filters to supply immunity from noise and unwanted emissions. Some accessories are available, including a front-panel with a two-digit diagnostic display that links directly to the CPU card. This simplifies fault finding and maintenance.

Arcom Control Systems Ltd., Units 8-10 Clifton Rd., Cambridge, England CB1 4WH; (0223) 411 200. CIRCLE 460

COLD-FORMED PGA SOCKET SAVES COST

A line of precision cold-formed PGA sockets offer consistent performance and a cost-saving potential of up to 30% compared with screw-machined sockets. The Series MD sockets can be used interchangeably with screw-machined sockets and incorporate the company's Omni-Tact seamless beryllium copper, low-insertion-force, four-tine contacts to get a high-reliability contact system. Five of the most popular grid sizes from 11 by 11 to 11 by 17 are available, as well as eight of the higher volume footprints, with pin counts covering 68 to 168 positions. Electrical characteristics include a 10-mΩ bulk contact resistance, 3-A contact rating, and 2-pF contact-to-contact capacitance. Prices range from $0.010 to $0.018 per line in large lots. Delivery is from two to four weeks.

Mark Eyelet Inc., 63 Wakelee Rd., Wolcott, CT 06716; (203) 756-8847. CIRCLE 461

SURFACE-MOUNT MCM IS TWO-FACED

Higher levels of functionality in one package are now possible with a standard surface-mountable multichip-module (MCM) package. The package features dual-sided mounting capability for semiconductor die. The MCM features high-density, thick-film wiring technology that permits up to three conductor layers on each side of the ceramic substrate. Almost any type of IC may be mounted in the package. Housed in a 168-pin plastic quad flat pack, the MCM offers a lead pitch of 0.8 mm and measures 1.5 by 1.5 in. Power dissipation is up to 3 W with still air at 70°C. Samples are available in eight weeks with volume quantities in 12 to 16 weeks. NRE charges typically range from $5000 to $15,000.

Fujitsu Microelectronics Inc., IC Division, 3545 N. First St., San Jose, CA 95134-1804; (800) 642-7616. CIRCLE 462

USE THERMAL-TRANSFER PRINTER IN-HOUSE

A thermal-transfer printing system and a full line of label materials is available for OEMs requiring in-house, on-demand label printing. The system's Bradyprinter THT model 203 thermal-transfer printer produces clear identification for boards, wires, flat-ribbon cables, rating plates, and other general-use applications. The company's Thermatab labels accept high-density printing of bar codes, graphics, and text, and withstand chemicals, solvents, extreme temperatures, and repeated handling. Call for pricing and delivery information.

W. H. Brady Co., Industrial Products Div., P. O. Box 2131, Milwaukee, WI 53201; (800) 537-8791. CIRCLE 463

FINE-PITCH SOLDERING COMES TO ITS SENSES

A soldering system designed for fine-pitch surface-mounted work is available with a 0.010-in. stainless-steel soldering tip that heats up in less than 1 second. The MicroSol 9001 system's tool has a thermocouple at the tip that senses the temperature and controls the applied heat. The tip temperature, digitally displayed, is continuously adjustable from 400 to 800°F. A panel switch selects among touch-control, continuous, or idle operating modes. Pricing for the main unit starts at $625, and individual tips start at $24.50. Call for delivery information.

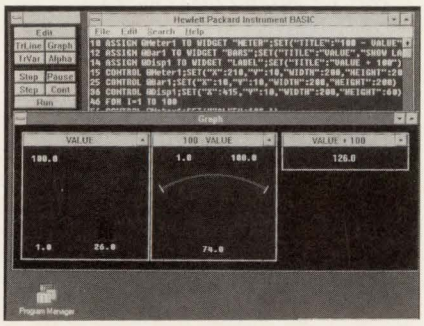
Analytic Technology, 15233 N. E. 90th St., Redmond, WA 98052; (800) 428-2808. CIRCLE 464

WINDOWS TOOLS SIMPLIFY TEST DEVELOPMENT

With its many I/O commands, HP Instrument Basic for Windows is the only Windows-based language designed specifically for measurement applications. The language combines an extensive command set with built-in tools for engineering graphics and user interfaces. The language can control both HP-IB (IEEE-488) and RS-232C instruments.

A companion product, HP-IB for Windows and DOS, supplies software utilities and interface hardware for instrument-control applications. The utilities complement many Windows and DOS programming languages, giving the user flexibility in test development.

A third product, HP ITG (Interactive Test Generator) II, provides an interactive graphical environment that speeds development of programs to control instruments, make measurements, and analyze and display data. The package includes a library of instrument drivers for 220 HP instruments. It also offers a menu-based driver-writing tool so users can quickly write drivers for other



instruments. HP ITG II supports Instrument Basic for Windows, Microsoft C, QuickC, and QuickBasic.

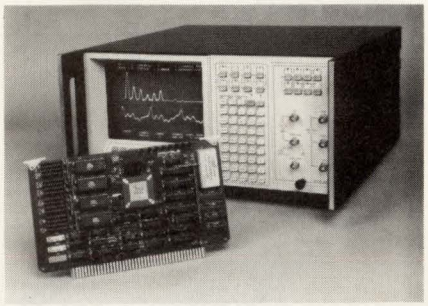
Instrument Basic for Windows (HP E2200A) costs $395. HP-IB for Windows and DOS (HP 82335B), which includes software utilities, documentation, and an HP-IB interface card, costs $525. HP ITG II (HP E2020B) goes for $1495.

***Hewlett-Packard Co.** Measurement Systems Operation, P. O. Box 301, Loveland, CO; (800) 452-4844.*

CIRCLE 465

■ *JOHN NOVELLINO*

DSP OPTION BOOSTS WAVE ANALYZER PERFORMANCE



A high-speed digital signal processor (DSP) option for the Model 6100 waveform analyzer increases the instrument's performance by a factor of more than 300. The Model 683 is a user-installable board that employs a 25-MFLOP, 32-bit floating-point DSP that is slaved directly to the Model 6100. Data is exchanged by fast direct memory access and simultaneous register transfers. The board can process time- or frequency-domain records as large as 32-kpoints in real time. The Model 683 works with any of the analyzer's more than 50 mathematical operations. It computes and displays an 8-kpoint FFT in milliseconds, and a computation-intensive 16K-by-16K cross-correlation analysis within 1 sec. The Model 683 costs $2995 and is available from stock.

Analogic Corp., 8 Centennial Dr., Peabody, MA 01961; (508) 977-3000.

CIRCLE 466

CARD SIMULTANEOUSLY SAMPLES 4 CHANNELS

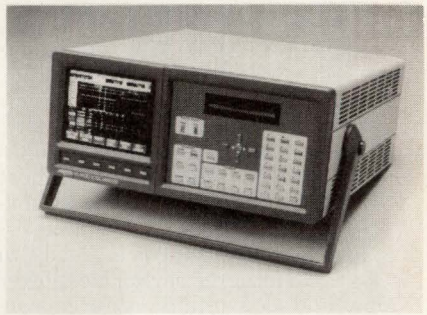
The PC-414A analog input board is suited for applications that need multiple analog channels sampled simultaneously. The board has four simultaneous sample-and-hold amplifiers multiplexed into a 1.5-MHz, 12-bit analog-to-digital converter. The unit runs in IBM PC/AT, PS-30, EISA, and compatible computers. In 4-channel mode each channel can be sampled at 250 kHz. Single-channel sampling can extend to 1.5 MHz. Total harmonic distortion is –72 dB. Optional software includes a windowed setup-and-go program and a source code library. PC-414A prices start at $1850 for single-unit quantities. OEM discounts are available. Delivery is from stock to 4 weeks.

Datel Inc., 11 Cabot Blvd., Mansfield, MA 02048; (508) 339-3000. CIRCLE 467

LOGIC ANALYZER GETS FAST CAPTURE SYSTEM

A new capture system, called Paladin, adds 200-MHz synchronous data capture and capability for 1-GHz synchronous timing analysis to the ML4400 logic analyzer. The system can be added to an existing ML4400 without degrading any other features.

Paladin's three operating modes offer the user flexibility. The basic mode provides 100 channels at 100 MHz or 50



channels at 200 MHz, both synchronously and asynchronously. This mode includes eight clock inputs with full Boolean, master-slave, or double-edge clocking. In the split mode Paladin offers 80 channels of 100-MHz synchronous data collection along with 20 asynchronous channels. In the high-speed mode the system supplies 10 asynchronous channels at 1 GHz and 20 asynchronous channels at 500 MHz. Multiple modules can be connected together.

Users can connect high-speed, coaxial, tip-compensated probes to the target system in several ways. Special probe connectors, which include the compensation elements, support hook connection, as well as one- or two-wire and socket connection. Channel-to-channel skew is less than 1 ns at 1 GHz. Each module comes with five active-element logic pods, each accommodating 20 data probes and two clocks. An available adapter allows the use of all microprocessor support packages for the ML4400 line. Paladin includes both classical and transitional clocks as well as a 24-bit time stamp.

Paladin, including 100 probes, costs $13,950. Base price for a complete analyzer system starts at $17,945.

***American Arium** 14281 Chambers Rd., Tustin, CA 92680; (714) 731-2138.* CIRCLE 468

■ *JOHN NOVELLINO*

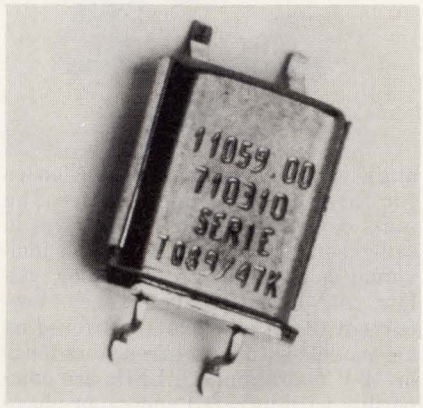
SURFACE-MOUNTED CRYSTALS AND OSCILLATORS REACH 300 MHz

A family of four surface-mounted crystals and oscillators have output frequencies from 625 kHz to 300 MHz. The devices have applications in telephone and radio communication products and in high-speed ECL and GaAs logic circuits.

Three of the family are fundamental quartz resonators, two of which, the HC-49 and TT-SMD lines, are produced from ultra-small AT-strip crystals. These devices are available from 3 to 50 MHz. The HC-49 comes in a metal SMD can and the TT-SMD comes in a plastic SMD package. The third quartz resonator, the HC-45, is made using the larger-but-higher-performance AT-cut crystal. Frequencies range from 3.579545 MHz (for TV color burst) to 300 MHz (for high-speed logic).

The HC-45 resonator is made by taking the AT-cut crystal form, extracting its ninth harmonic, and packaging it in what would typically be a through-hole metal can. The leads are cut and formed for surface mounting, and a clip is applied that permits mounting the device and soldering it flat on a pc board.

The fourth part, model CO-99100, is a complete, integrated SMD clock-oscillator circuit with an internal AT-cut crystal. The unit operates from 625 kHz to 24 MHz and is mounted in a 28-pin PLCC. It delivers a square-wave output with TTL fanout of 10, or 50 pF of high-speed CMOS loading.



Pricing in lots of 1000 is $0.70 for the HC-49, $0.90 for the TT-SMD, $0.75 to $0.95 for the HC-45, and $2.50 for the CO-99100. All are available from stock to 12 weeks.

***Raltron Electronics Corp.**, 2315 N.W. 107th Ave., Miami, FL 33182; (305) 593-6033.* CIRCLE 469

■ *DAVID MALINIAK*

SMD RESISTORS HAVE HIGH STABILITY

Available in values as low as 1 Ω, precision thick-film resistors in the new RC12 range from Philips Components feature excellent high-frequency performance, high stability and small case size. Their 1% tolerance, low temperature coefficient and availability in values of up to 1 MΩ suit them for use in a wide range of analog circuit applications where precision and surface-mount miniaturization need to be combined—for example, in hand-portable communication equipment and high-frequency test and measuring instruments.

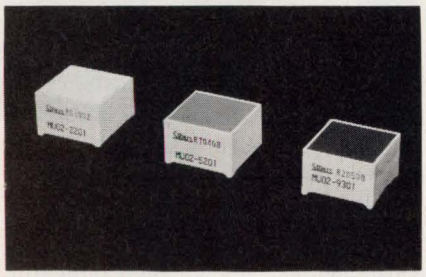
RC12 resistors are housed in an industry-standard 0805 package measuring 2.0 by 1.25 by 0.6 mm, and are available with temperature coefficients of 50 parts per million/°C or 100 ppm/°C for values above 10 Ω. Their low temperature coefficient, combined with good temperature tracking, allow them to maintain their precision in equipment that is subject to wide temperature variations. The RC12H type of resistors cover the resistance range from 1 Ω to 1 MΩ, while the RC12G types range in value from 100 Ω to 1 MΩ.

The RC12 resistors sell for around $1.10 per 100 devices in high-volume quantities. Delivery time is about six weeks after receipt of order.

Philips Components, Discrete Products Div., 2001 West Blue Heron Blvd., Riviera Beach, FL 33404-5099; (407) 881-3257 (Miriam Coleman).

CIRCLE 472

LED LIGHT BARS OFFER HIGH BRIGHTNESS



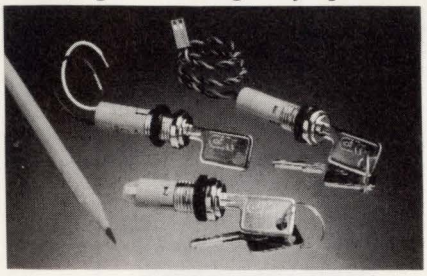
Super brightness, long life, and low power consumption are featured in a line of LED light-bar modules. Various combinations of shape, size, and color are available to suit many display applications. Brightness levels up to 42 mcd/unit are attainable. Package styles include square, rectangular, round, SIPs, and DIPs. Colors include red, orange, yellow, green, and pure green. Call for pricing and delivery.

II Stanley Co. Inc., 2661 Gates Ave., Irvine, CA 92714; (800) 533-5231.

CIRCLE 470

MINI POWER SWITCHLOCKS FIT 12-MM PANEL HOLES

A space-saving miniature power switchlock that fits 12-mm-diameter panel holes addresses the need for a small, good-looking key-operated



switch. The YM Series switchlock offers 0.110-in. quick-connect terminals or wire-lead terminations. Switch function is single-pole, single-throw on-off. Silver-plated contacts are rated for 4 A at 125 V ac or 28 V dc. Prices start at $5.71 in lots of 1000. Delivery is in six weeks.

C&K Components Inc., 15 Riverdale Ave., Newton, MA 02158-1082; (617) 964-6400. CIRCLE 471

PALMTOP LCD DISPLAY IS CGA-COMPATIBLE

A 640-by-200-dot, CGA-compatible LCD module is available for the fast-growing palmtop-computer market. The TCM-A9108 display features a metal bezel for ruggedness, measures just 215.0 mm wide by 99.0 mm tall by 6.3 mm deep, and weighs only 190 g. Dot pitch is 0.27 mm by 0.36 mm, which lends the display to alphanumeric characters as well as special characters, graphs, patterns, and charts. The display incorporates formulated-twisted-nematic, liquid-crystal technology and a 1/200 duty ratio for high contrast and fast response time. Average power consumption is 130 mW. Samples, available now, cost $240. Call for delivery and OEM pricing.

Epson America Inc., OEM Div., 20770 Madrona Ave., Torrance, CA 90503; (310) 787-6300. CIRCLE 473

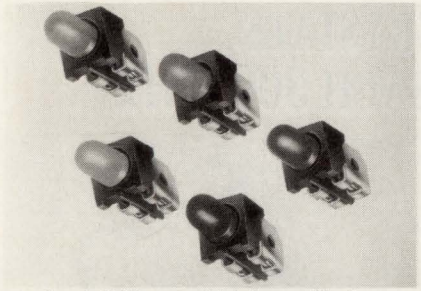
QUIET CERAMIC CAPS HAVE BEST ESR IN CLASS

A line of chip capacitors has the industry's best equivalent series resistance (ESR) in its price class, its manufacturer says. The MCH Series capacitors' NPO/C0G "A" dielectrics are fabricated with pure palladium electrodes and fired at higher temperatures than those of competing ceramic chips. Also, the chips are made in Class 10 cleanroom conditions with highly accurate electrode alignment. The chips come in 0805 and 1206 sizes with a capacitance range of 0.5 to 2700 pF for NPO dielectrics, and 680 pF to 0.22 μF for X7R dielectrics. Prices range from $15.80 to $45.10 in lots of 1000. Delivery is from stock to 10 weeks.

Rohm Corp., 3034 Owen Dr., Antioch, TN 37013; (615) 641-2020. CIRCLE 474

SURFACE-MOUNT LEDS HAVE HIGH BRIGHTNESS

A line of right-angle, surface-mounted LEDs features high brightness, wide-

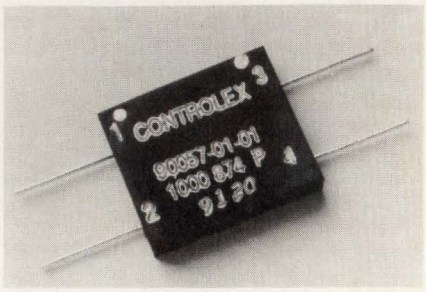


angle visibility, and high-profile lenses for through-panel applications. The units come in T-1 and T-1-3/4 sizes in red-green bicolor style and in five individual colors (red, green, amber, yellow, and blue). High-efficiency, low-current (2-mA) models are offered as are models with built-in resistors for 5- or 12-V operation. All LEDs are compatible with infrared and vapor-phase soldering, and have standoffs for easy cleaning. Pricing starts at $0.78 in lots of 1000. Small quantities are delivered from stock.

Industrial Devices Inc., 260 Railroad Ave., Hackensack, NJ 07601; (201) 489-8989. CIRCLE 475

SMD PULSE TRANSFORMER HANDLES 2500 V/μS

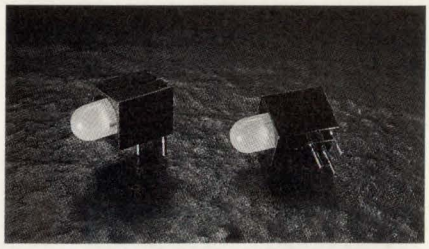
A family of low-profile pulse transformers occupies just 0.65 by 0.85 in., stands only 0.2 in. tall, and is suitable for either surface- or through-hole mounting. Thanks to a proprietary



winding geometry and a high flux-density core, the transformers support 2500 V/μs voltage changes while delivering rise times of under 100 ns. Applications are in dc-ac inverters, ac-power controllers, pulse-width modulators, and high-frequency power transformation. Typical pricing is in the $25 range for OEM lots. Delivery is from stock to 60 days.

Controlex Corp., 16005 Sherman Way, Van Nuys, CA 91406; (818) 780-8877. CIRCLE 476

BICOLOR INDICATOR SHUNS RED FOR YELLOW



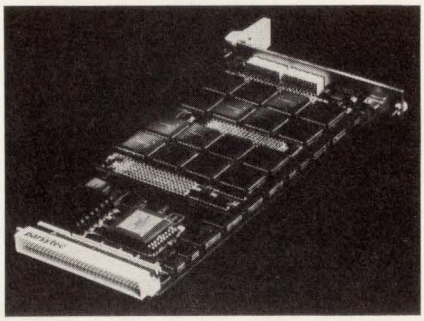
Not everyone needs a bicolor indicator in red and green—some applications call for "waiting" and "active" indication rather than go/no go. That's the need addressed by the Series 550-3605 three-leaded yellow-green indicator. The single right-angle, 5-mm package eliminates multiple lamp requirements and simplifies drive circuitry. One possible application might be a LAN-controller card that uses the indicator to signal that a channel is either available or in use. The LEDs are packaged in a black housing for optimal contrast ratio and increased visibility. Pricing is $0.97 in lots of 1000. Delivery is from stock to eight weeks.

Dialight Corp., Dept. C550-36, 1913 Atlantic Ave., Manasquan, NJ 08736; (908) 223-9400. CIRCLE 477

TRANSPUTER-BASED SYSTEMS GET EXPANDED I/O FUNCTIONS

With the introduction of the Transputer Imaging Processing (TIP) I/O architecture, users can combine unlimited scalability of a Transputer-based system with 100-Mbyte/s data distribution over each TIP broadcast bus. Multiple independent broadcast subsystems can be integrated into one system to increase the total I/O bandwidth required for any application. While the name denotes image processing, the TIP I/O architecture is suitable for any application requiring the increased bandwidth.

The TIP bus transmits data simultaneously, in parallel, to multiple Transputer nodes using the broadcast function. It can also function in a gathering mode for applications where distributed data must be accessed in total for display or subsequent processing. Using 48 T805 nodes and a TIP interface, 100-MFLOPS, 750-MIPS performance can be achieved. The balance between I/O and processing capabilities enables TIP-based systems to perform real-time processing and fast Fourier transforms over data channels.



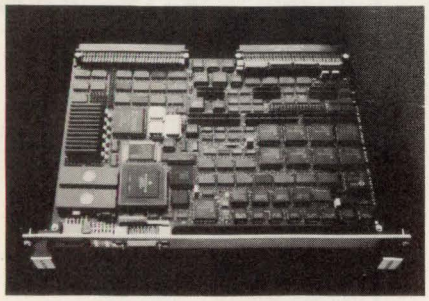
The TIP-based series of boards now includes the TIP-VPU/T8 T805 processor board, the TIP-MFG monochrome frame grabber, and the TIP-CGD color graphics display board. The TIP-VPU/T8 (1 Mbyte DRAM) sells for $4600, the TIP-MFG costs $5200, and the TIP-CGD is priced at $5800. Systems designed with the TIP technology start at $6950.

***Parsytec Inc.**, Bldg. 9, Unit 60/61, 245 W. Roosevelt Rd., West Chicago, IL 60185.* **CIRCLE 478**

■ *RICHARD NASS*

68030-BASED VMEBUS I/O BOARD HAS 18 RS-232 PORTS

Designed around a 68EC030 microprocessor, the HK68/VSIO VME serial interface board from Heurikon furnishes users with 18 RS-232 I/O ports. They are all based on



Zilog's Z85C30 serial I/O controller. Featuring a software controllable bit-rate generator, the Z85C30 supports asynchronous transfer rates up to 56 kbits/s and synchronous transfer rates up to 1 Mbit/s.

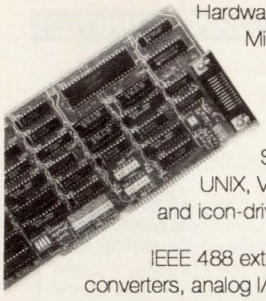
Sixteen of the I/O ports are accessed through the board's VMEbus P2 connector. They support sixteen asynchronous ports with four lines each or ten synchronous ports, each with six lines. The remaining two ports are accessed through the front panel and can be operated in either an asynchronous or synchronous mode.

The HK68/VSIO can hold up to 4 Mbytes of DRAM and up to 2 Mbytes of EPROM. It can operate either as a slave or a master on the VMEbus. It supplies a full VMEbus interface, including 32-bit addresses and data, seven bus interrupts, and system-level control functions. Plug-over module connectors are supplied to support custom serial I/O interfaces such as RS-422, RS-485, or V.35, or front-panel I/O. The board also features a user-programmable seven-segment display that can indicate the status of the system, board or CPU. With 1 Mbyte of RAM, the HK68/VSIO sells for $2195 and is available now.

***Heurikon Corp.**, 8000 Excelsior Dr., Madison, WI 53717; (608) 831-0900.* **CIRCLE 479**

■ *RICHARD NASS*

IEEE 488.2



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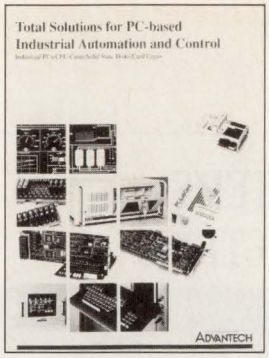

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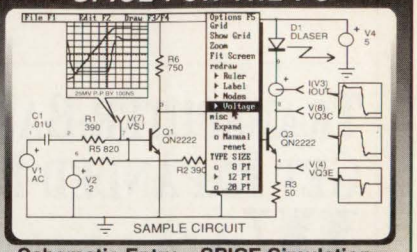

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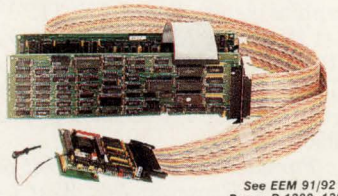

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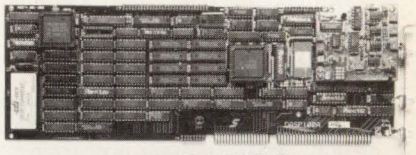

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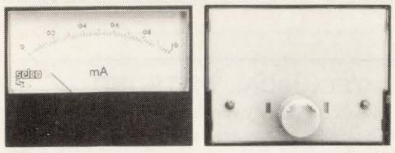

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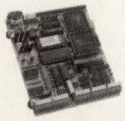

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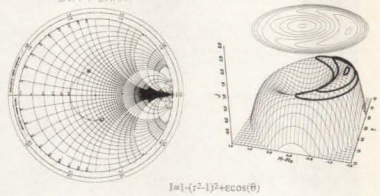

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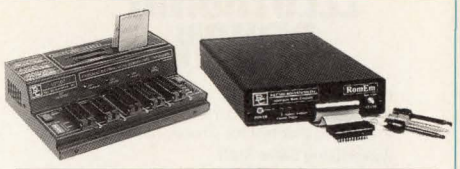

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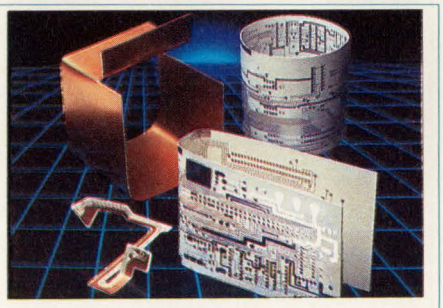

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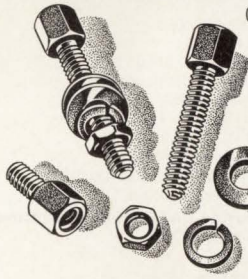

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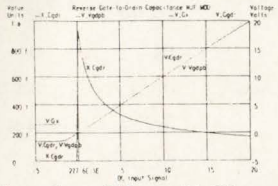

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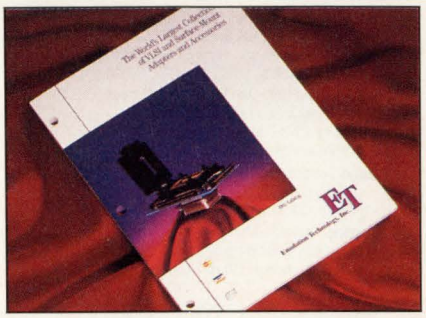

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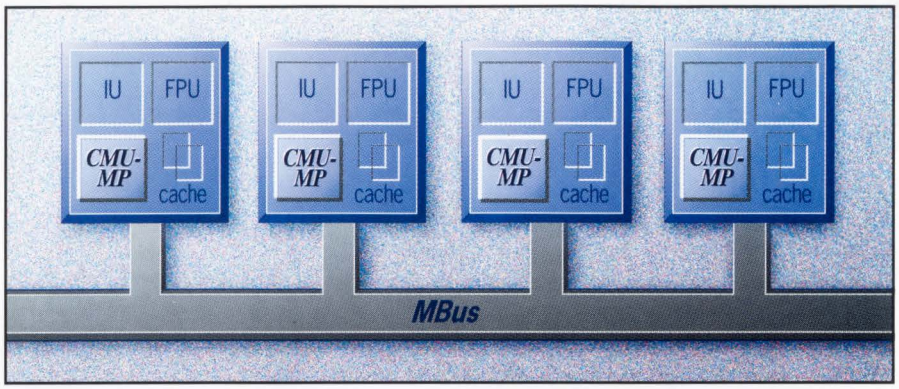

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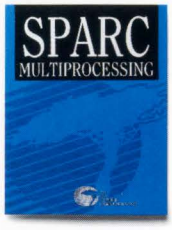

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