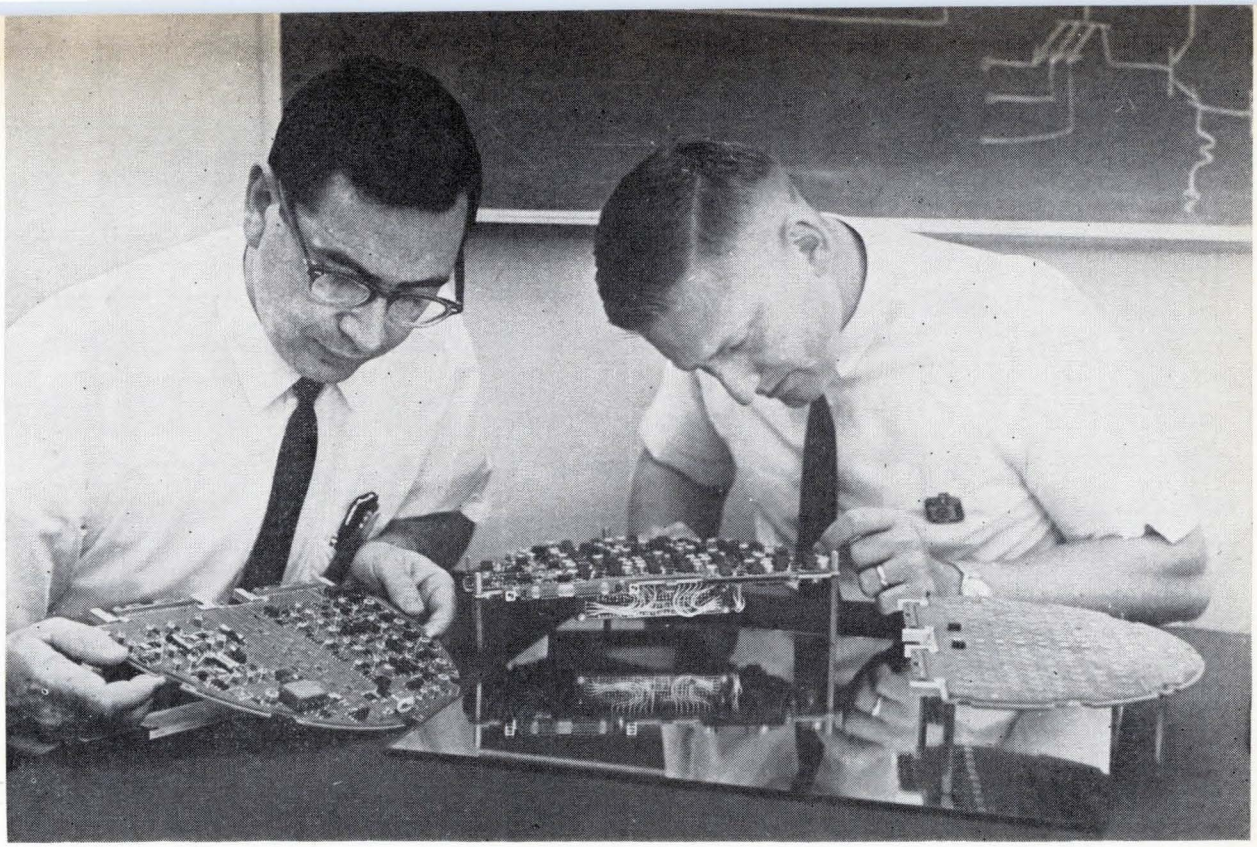

Three subassemblies constitute IBM's new mass production computer for varied aerospace applications.

Computers

The airborne 4 Pi computer: IBM aims at aerospace guidance

A low-cost computer now being mass-produced promises to replace traditional computers in guided missiles. Intriguing organization and the use of IC's contribute to its attractiveness

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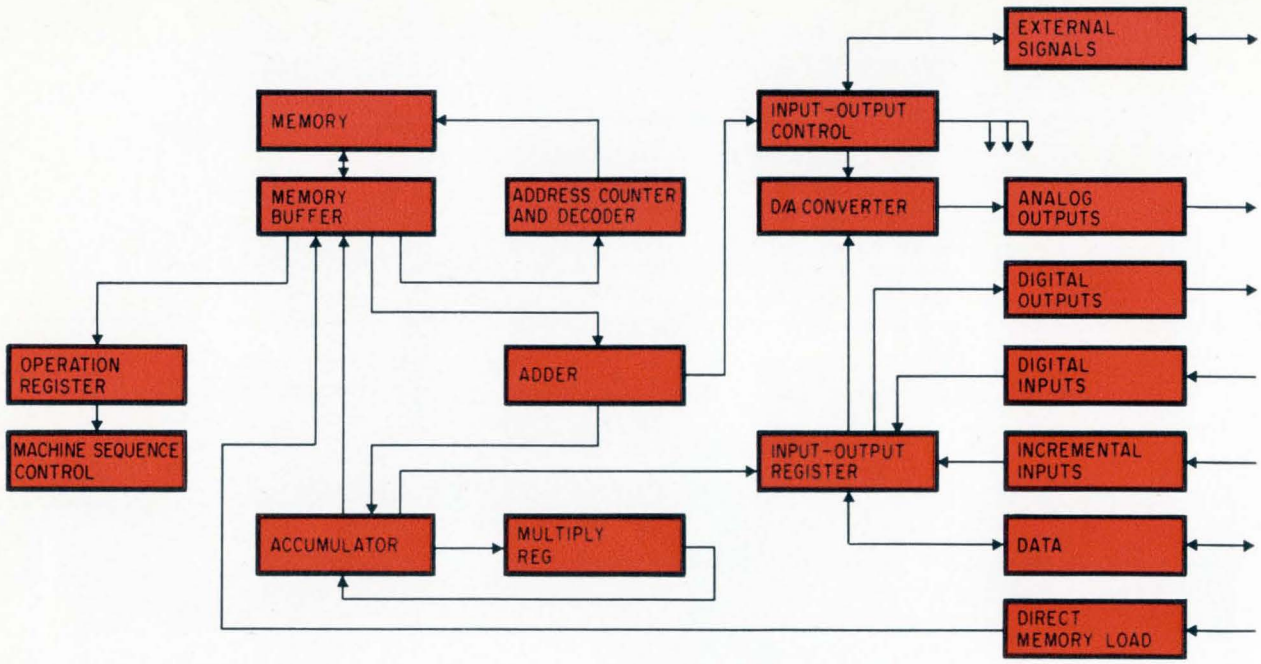
General-purpose digital computers have heretofore been too expensive and too large for use in expendable aerospace applications such as in the guidance system of a missile. But now they can compete with the special-purpose machines that have traditionally been used in such vehicles. The widespread availability of varied monolithic integrated circuits, new packaging techniques and high-speed core memories makes the competition possible. Mass production of logic circuits has cut the cost of such a general-purpose computer and the inclusion of IC's has reduced the size of the machine sharply.

Although special-purpose analog, hybrid analog and digital, and incremental computers have all been used in aerospace vehicles, the military would prefer a general-purpose machine instead because



This tactical-missile computer resembles many other computers and therein lies its special advantage. Previously computers for such applications were specifically designed.

the special-purpose one always requires unique design, and special software, testing and reliability data, and is difficult to reprogram. The Air Force has dropped special-purpose machines entirely in ground support applications, preferring off-the-shelf machines of general-purpose design because they have better reliability [Electronics, Sept. 19, 1966, p. 201].

An engineering model of a general-purpose machine, designed especially for aerospace use, has been built and evaluated by the International Business Machines Corp. as part of IBM's series 4 Pi program, which is as comprehensive in aerospace applications as IBM's System 360 is on the ground. The basic design of this machine will solve the kind of problems encountered in missile guidance, although it can be used in other applications with the addition of special input-output channels and different packaging. Such versions would be suitable for aircraft control and navigation.

IBM has built the 4 Pi machines with integrated circuits, but the logic organization can be easily implemented with large functional arrays when large-scale integration becomes feasible.

System architecture

Because the missile system imposes unusual requirements of size, weight, power, cost and maintainability, the computer design must be a compromise of system organization, instruction set and circuit layout. In addition, the design must be easy to modify because the over-all system will probably change during development.

Analysis of the guidance problem showed that system accuracies could be met with a 16-bit data word and that an erasable memory with direct access and a relatively small capacity was required. Instructions of both 8-bit and 16-bit lengths economize still further on the memory size, over a uniform 16-bit instruction format. Thus all data and instructions fit in a memory of only 1,024 eight-bit words.

Instructions are stored anywhere in the memory. Data is stored only in one block of 256 words, and the block is divided into four 64-word sectors. The sectors economize on the memory-addressing hardware, although this makes the programing awkward when data from different sectors is required.

A part of the 1,024-word main memory may be wired as an optional read-only memory. When so

Missile guidance computer characteristics

Type of computer	General-purpose processor with specialized input-output
Mode of operation	Serial arithmetic parallel program serial input-output
Arithmetic notation	Fixed point
Instruction word length	8 or 16 bits
Data word length	15 bits and sign
Number of instructions	15
Arithmetic speeds	
Addition	12 μsec
subtraction	12 μsec
Multiplication	140 μsec
Memory capacity	1,024 8-bit words
Memory cycle time	4 μsec
Input-output-control	6 inputs 8 outputs
Incremental counters	3
Data channels	One, serial
Channel speed	100 khz
Weight	10 pounds
Volume	0.27 cubic feet
Power	32 watts
Reliability	14,000 hours or more

wired, the read-only portion stores programs and subroutines that have been completely debugged. Instructions in the read-only memory aren't changed by temporary malfunctions or unusual conditions that arise during missile storage, testing or flight. In space vehicles particularly, the read-only memory is useful because it occupies little space and is highly reliable. In the larger models of the 4 Pi series [Electronics, Oct. 31, 1966, p. 42], and in general-purpose computers like IBM's System 360, the read-only memory controls the execution of programs but does not itself contain program instructions; the programer is not concerned with the read-only memory.

The set contains only eight instructions, each consisting of an operation code and a single address. All instructions have the same execution time except the multiply and shift instructions. Two of the eight instructions can be coded to perform different operations: the process input-output can initiate 31 different operations, and the transfer can cause either conditional or unconditional transfers (execution out of normal sequence) or a change in the memory sector being addressed.

Memory design

The core array is a single plane automatically fabricated and tested, containing 1,024 eight-bit words, expandable to 2,048 words. Additional planes can be stacked to build larger memories, up to 16,384 words. The larger memories, however, will not fit on a single page. Drive and sense electronics consist of monolithic and discrete components. The memory system cycle is 2.5 microseconds, but each active cycle is followed by a 1.5-μsec idle period to reduce power consumption; the total cycle is therefore 4 μsec.

The read-only memory is identical to a normal memory except that cores are removed from those locations which contain zeros. This arrangement has several advantages. The memory construction is essentially similar to a conventional system and can be fabricated on existing automatic equipment. Data can be written into as well as read from the memory during development, thereby allowing flexibility in the programing design. The memory with appropriate cores missing is truly unalterable, and cannot be affected by electrical transients or erroneous addressing. The same drive and sense circuitry can be used as with the normal memory; the memory addressing is also the same.

A memory of this type presents certain difficulties. For example, cores with hysteresis loops that are not square could generate unwanted outputs caused by noise from the slanting top of the square. To reduce this hazard the timing of the memory drivers is staggered and extra cores on the drive lines compensate for the noise.

Sensing and controlling

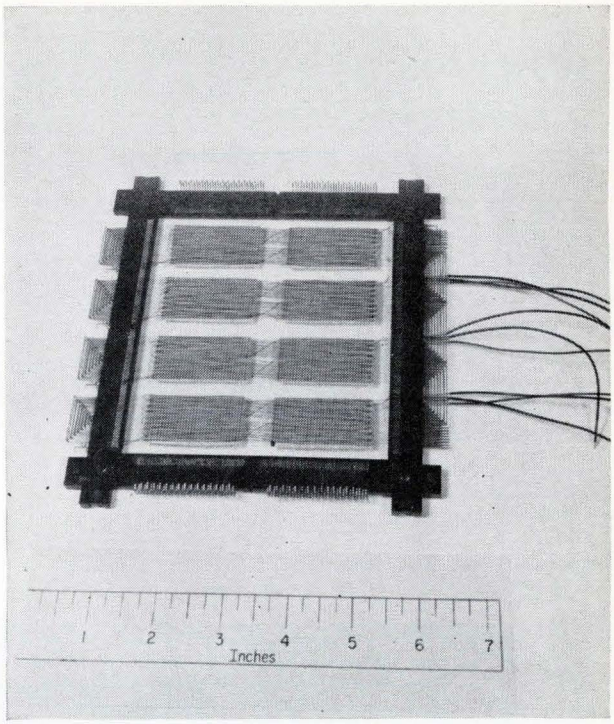
The input-output section of the guidance computer performs important functions:

- It decodes, buffers and amplifies control outputs and decodes and gates control inputs.
- It monitors the guidance processor, signals the occurrence of any program or power malfunctions and keeps track of real time.
- It accumulates input signals from the accelerometers for later processing, and works with external equipment during initialization and retargeting procedures.
- It assists in the alignment and torquing of the inertial platform and other control functions.
- It controls the sequence of power on-off to various subassemblies.

The specialized nature of these tasks require a mixture of digital and analog circuits using both discrete components and IC's in flatpacks. However, all circuits are mounted on a single multilayer board, as shown in the bottom table, p. 175.

All digital transmission line circuitry, all control circuitry, and most digital-analog conversion circuits are IC's packaged in 14-lead flatpacks. In most cases, analog IC's proved too costly to use.

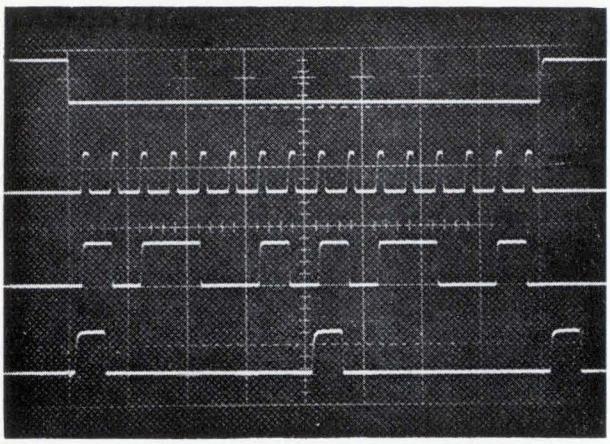
A major consideration with the multilayer boards



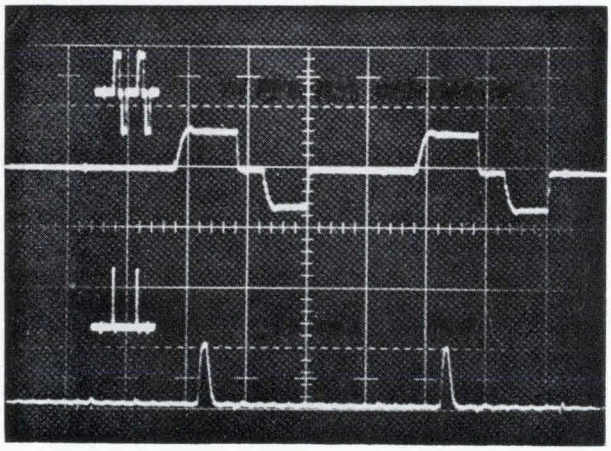
Memory array used in the tactical-missile computer is a single core plane that can hold 1,024 eight-bit words.

How fast the 4π works

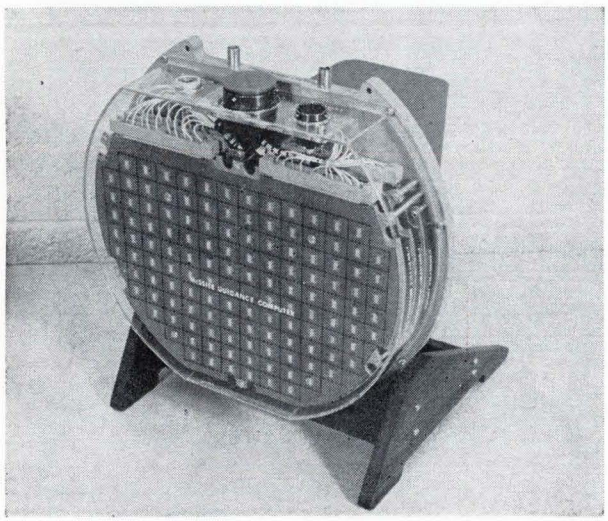
Instruction set	Time (μsec)
Clear and add	12
Add	12
Subtract	12
Multiply	140
Store	12
Shift (left or right up to 16 places)	20
Process input-output (31 codes)	12
Transfer (6 codes)	12



Data and timing waveforms from the computer are, from the top down, the instruction-execution cycle, the serial add shift operation, data from the accumulator, and the main computer timing pulse, once every 4 microseconds. The scales are 1 μsec per division horizontally, and 5 volts per division vertically.



Memory input and output waveforms show the drive current on the top trace and the sense amplifier voltage on the bottom. The vertical scales are respectively 0.5 ampere per division and 3 volts per division; both horizontal scales are 1 microsecond per division.



Three subassemblies are visible in this mockup of the computer. They are the central processor, the memory, and the input-output. The round shape is the cross section of the missile in which the computer will be used.

in the input-output subassembly was in designing them so the necessary voltages are provided to the various circuits, crosstalk is avoided between them, and at the same time the board design is kept simple. The logic circuits need only one power supply, +5 volts; power drivers, amplifiers and other special circuits, some of which are hybrid IC's or discrete-component circuits, sometimes require two or three voltages. But the board contains only a ground plane and one other voltage supply plane. The voltage plane is subdivided, one voltage connected to each subdivision, and the cans and flatpacks arranged on the surface of the board so that the necessary voltages are available and also that low-level logic circuits are well separated from high-current power drivers delivering as much as three amperes.

Three plates and a harness

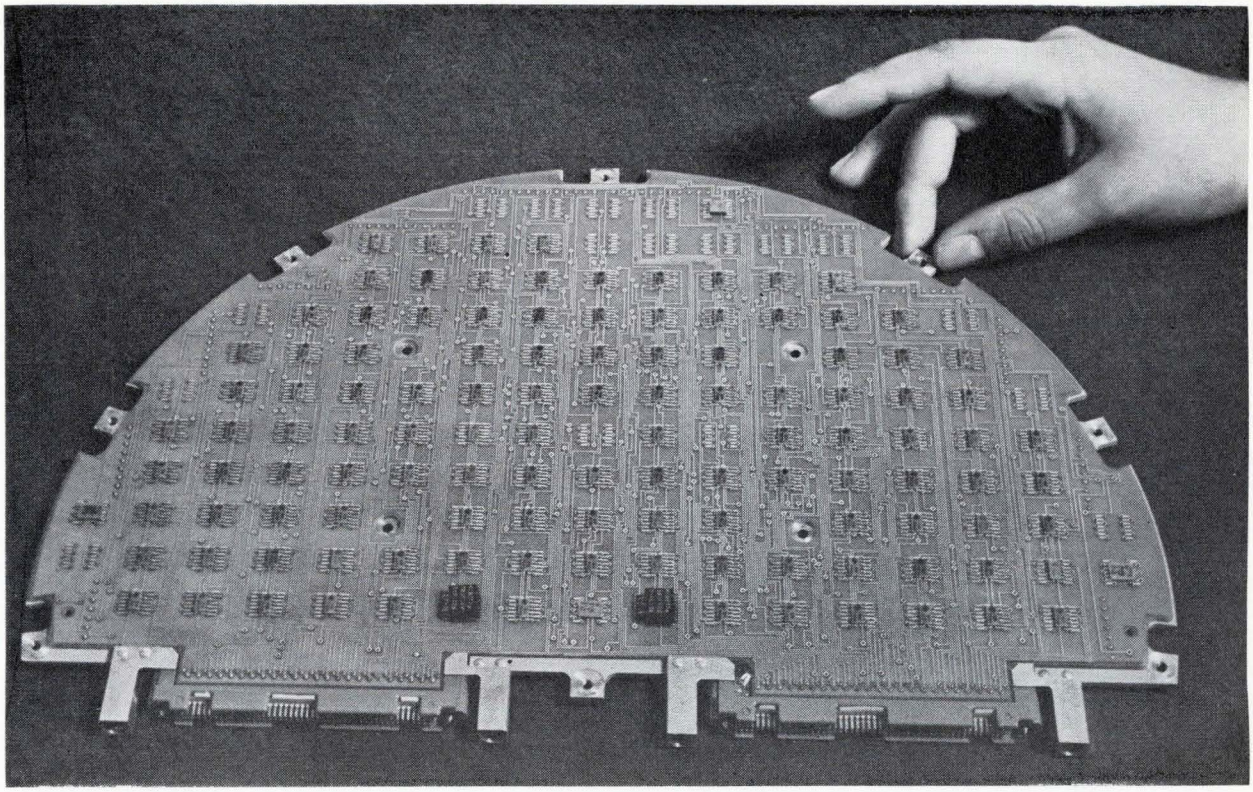
The computer, below left, contains three major subassemblies: the central processor, the memory, and the input-output. Each semicircular subassembly is made of two simple multilayer boards and a supporting aluminum plate that is both mechanical support and thermal conductor which is brazed to a cold plate. The shape of the computer is compatible with a specific missile configuration that is classified. Integrated-circuit flatpacks and discrete components are soldered to specified land patterns on the multilayer boards. The boards themselves contain two signal-wiring layers, one voltage distribution plane and one ground plane. All signal connections within a board are 0.010 inch wide and 0.025 inch apart. The two boards are insulated from and bonded to the aluminum supporting plates to form a page. Three pages make up the entire computer.

Putting all electronics associated with major sections of the computer on a single page minimizes the number of interpage wires and connectors and eliminates the need for a costly and complex backpanel. A simple wiring harness is used.

The unit is cooled by conduction through the page mountings to a cold plate; air at an inlet temperature of 70°F ±10° (21°C ±5°) cools the plate before the missile is launched. During the missile's relatively short flight, the calculated temperature rise is less than 1°F per minute.

The temperature specifications for the inertial platform are 30° to 60°C, and this range was chosen for the computer as well. Within this range, the memory power supplies do not need controls to vary their output with temperature, a significant cost reduction. Point-to-point temperature variation within the computer can be considerably greater. The monolithic IC's have a temperature range of 0° to 70°C. These circuits require temperature regulating controls, but the controls are cheaper than the extra cost of circuits with a wider range.

The memory subassembly is mounted closest to the cold plate because of its restricted temperature limits, while the other two subassemblies can be



Flatpack mounting and wiring details are visible in this view of the arithmetic and control subassembly.

placed next to the memory with either one in the middle. The entire unit is sealed with a O-ring gasket to keep out excessive humidity and dirt.

Heart of the computer

The central processor subassembly is a general-purpose unit that performs the basic arithmetic and control functions. The two multilayer boards making up this subassembly contain 243 standard 14-lead flatpacks. The basic structure of the board avoids signal crosstalk and provides some power supply decoupling; additional discrete decoupling capacitors are mounted around the page assembly. Connections between boards are provided by 100 feed-through pins along the edge of the boards. Two 98-pin connectors are mounted on the flat edge of the subassembly for connections to the memory, input-output pages, and external guidance equipment.

The computer is built with seven types of transistor-transistor logic (TTL) circuits. One consideration in the choice of an IC family was its applicability to other programs, since purchase in large volume saves money.

The logic requirements of the computer suggested a few additions to the standard TTL line, the most significant of which was two flip-flops on one flatpack. Sixty-three of these dual flip-flops are used in the design as registers, shifters and counters.

What lies ahead

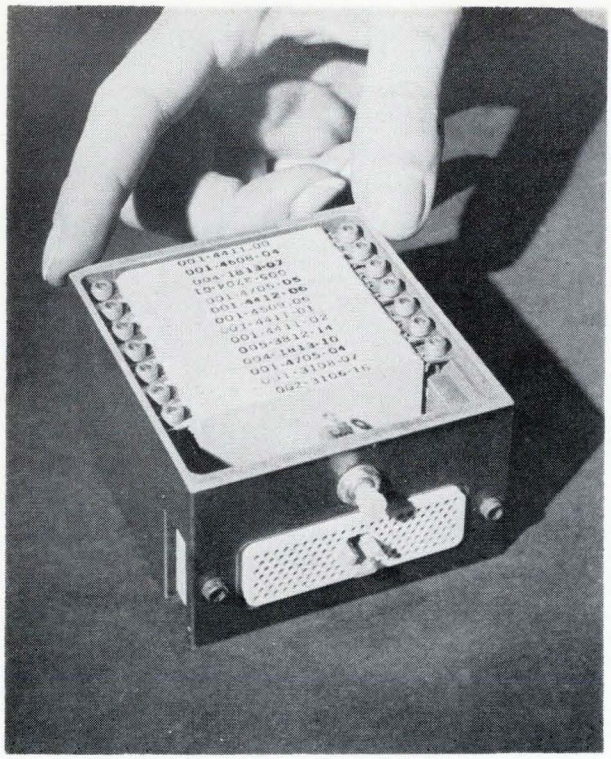
The logic circuits now used are nonfunctionally

T^2L circuit characteristics

Circuit delay (maximum)	25 nanoseconds
Power consumption (average)	10 milliwatts per gate
Power supply	5 volts ±10%
Fan-in	8
Fan-out	10
Signal levels, nominal	0 and +5 V
Noise margins (minimum)	400 millivolts
Temperature range	0 to 70° C

Counting the components

	Processor	Memory	Input-Output	Total
Integrated circuit flatpacks	243	56	34	333
Discrete semiconductor flatpacks	....	80	...	80
Transistors	....	76	59	135
Diodes	....	109	39	148
Resistors	....	288	98	386
Capacitors	12	79	33	124
Miscellaneous	....	68	1	69



Data-flow model of a digital computer built from multicircuit monolithic chips attached to thin-film interconnection networks.

packaged—that is, gates and storage elements are individually packaged in 14-lead flatpacks. Future missile guidance computers will unquestionably be built from large-scale functional monolithic circuits, to attain even lower cost and higher reliability. The repetitive nature of the processor design permits a functional packaging approach that could be implemented in either of two ways:

- Multicircuit monolithic chips can be attached to thin-film[1,2] interconnection networks on a passive substrate, which is integrally packaged in a pluggable, hermetically sealed package. This hybrid approach offers a good potential for handling specialized analog and memory electronic requirements.

A data flow model employing these techniques is in the photo shown above. More than 2,500 components occupy less than 16 cubic inches including the thin-film panels, chassis, backpanel, and connector.

- Large-scale integration (LSI) techniques[3] [Electronics, Feb. 20, p 123] with monolithic and thin-film process steps on an active substrate are packaged in large flatpacks containing 28 or more planar flat leads. Metal-oxide semiconductor devices with either fixed or programable interconnection patterns or bipolar transistor circuit cells with a fixed interconnection pattern appear feasible at this time.

The hybrid approach offers short-term advantages, since both the monolithic chips and interconnection networks can be individually pretested prior to integration. This approach does not rely on the nearly perfect yields that LSI would require.

Nevertheless, several Government agencies and private firms are trying to develop LSI with the ultimate goal being perhaps a "computer on a chip."[4] Current photomasking techniques permit as many as 1,200 to 1,800 gates to be fabricated on a single wafer. Typical aerospace computers require about 1,500 gates; therefore it seems numerically possible to build an entire computer on a single chip of silicon. However, current yields of circuit cells and film interconnections are too low to achieve the desired results; and packaging, interconnections, and thermal technology are not yet far enough along to make a single-wafer computer practical. At one semiconductor company, planners talk about putting 40,000 gates on a slice someday. Then a slice would have more than enough good gates for an aerospace computer.

In our opinion, large-scale integration of assemblies will be an evolutionary process. Arrays with 20 to 30 circuits per module will become common first; modules containing 200 circuits or more will be developed later.

These functional modules will require significantly fewer expensive operations than semiconductor manufacture now requires, such as testing, dicing and encapsulation. They will also make possible substantial size reduction, which will permit the inclusion of more circuits for greater capability in a given size. They will be substantially more reliable than the present circuits because of the reduced number of connectors, solder joints and wiring paths in the computer.

Other technological advances that will affect future missile guidance computer development are advances in memory, including electrically-alterable read-only memories, strap-down guidance systems that will require higher computer performance, high-density printed circuits and multilayer boards, and thick-film or thin-film microminiature passive components.

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The authors

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